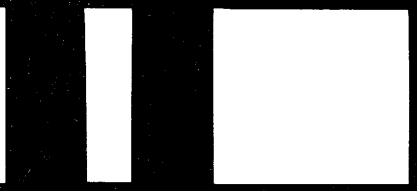
DESIGNING WITH MSI

Vol. 1



COUNTERS AND SHIFT REGISTERS

DESIGNING WITH MSI VOL. I February 1970

DESIGNING WITH MSI

VOL. I

COUNTERS AND SHIFT REGISTERS

Written by

LES BROCK

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AN INTRODUCTION TO DESIGNING WITH MSI

Medium Scale Integration (MSI) is the integrated circuit manufacturers' solution to the continually expanding requirements of the military and commercial industry for flexible integrated circuit subsystems.

ECONOMIC CONSIDERATIONS OF MSI

The economic concerns of the IC manufacturer, when considering a new MSI device, are little different from those he has had for all new products over the past six or seven years. The producer is still concerned with the volume of parts he can expect to sell. In order to achieve the volume levels required to maintain profitable operation, an MSI element must offer the end user *versatility* and applications flexibility.

A flexible design is achieved by partitioning high volume, complex systems, including: Central Process Units (CPU), Input/Output (I/O) and interface systems, computer peripheral systems, digital communications systems, process control systems, industrial control systems and display systems. Where recurring building blocks are identified, that function becomes a candidate for integration into a smaller, more universal subsystem. The design must provide the applications flexibility needed for use in all, or most, of these systems.

An alternate approach is to identify a specific function, common to many different types of high-volume systems, and integrate that function as an MSI element. One example of this type of MSI is the decoder/display drivers available for universally accepted read-out elements, such as NIXIE* tubes and seven-segment displays.

A second concern of the IC manufacturer is *yield.* The yield of a MSI device must be high enough to ensure not only availability, but competitive costs with a multiple, standard package solution of the desired function.

The *cost* of the MSI package is an important consideration, as it was in earlier days of the IC industry when the yield of assembled parts was relatively low. The use of solid molded packages and one pass bonding techniques of beam leads and flip-chips are areas where considerable effort is being expended to help reduce overall packaging costs.

The economic considerations of the potential MSI user are considerably more complex and subtle than those considerations facing the IC manufacturer. The systems house must consider three major areas in its decision to use MSI. The cost of a MSI solution as opposed to a multiple, standard package solution is the most complex consideration. A detailed examination should be carried out first.

A check list would include the *cost of piece parts,* which is generally higher for a new MSI circuit than for the multiple, standard package solution. However, while the MSI piece part cost is higher, other cost considerations may rule. The *cost of inserting each package* in a printed circuit board is of prime importance. The actual *number of printed circuit boards* required for each piece of equipment must be determined. Then the *number and cost of interconnects* on a board, and the associated board connectors must be considered on a board-by-board basis. Other considerations include the *cost of parts inventory* and the *cost of writing, negotiating and maintaining specification control drawings* on production devices.

The requirement to use *complex, high-frequency layout and decoupling techniques* to optimize MSI performance adds cost that would nearly be eliminated if a slower, non-current spiking logic form such as classic DTL, low-power TTL (8400) or Utilogic II were used. Section I of this applications handbook deals with this subject in detail.

Two other considerations facing the user are equally important. The *availability of production volumes* of an MSI circuit is the most important consideration the user faces in committing specific pieces of equipment to definitive production schedules. By nature of the circuit design definition required to provide the desired applications flexibility in a MSI device, a potential user is likely to be exposed to the function concept during the circuit design definition stage of the MSI product development. This exposure may come six to eighteen months before production quantities of the finalized functional block are expected to be available.

An intangible consideration for the user is the possible enhancement of sales appeal gained by an *equipment design incorporating state-of-the-art devices.* This consideration is particularly applicable to equipment sold into technology oriented markets.

PURPOSE OF THE APPLICATIONS HANDBOOK

The purpose of this handbook is to closely examine the MSI counters and shift registers available from Signetics. In addition, a series of applications is offered, which utilizes these MSI circuits in typical and useful system configurations.

Section I is devoted to developing a framework of general electrical and physical system design criteria. This section provides guidelines for avoiding the most prevalent MSI system malfunction mechanism – inadequate power supply and ground systems.

Section II examines, in detail, the asynchronous (ripple) counters and Section III deals with synchronous counters.

In Section IV, the use of various, general purpose shift and buffer registers is discussed from a systems viewpoint.

*A trademark of the Burroughs Corporation.

SECTION I

GUIDELINES FOR DESIGNING WITH MSI

TTL DESIGN TECHNIQUES

MSI circuits, including those in this handbook, are fabricated using classic TTL (Transistor-Transistor-Logic) circuit designs. An example of a classic TTL NAND gate design is shown in Figure 1-1.

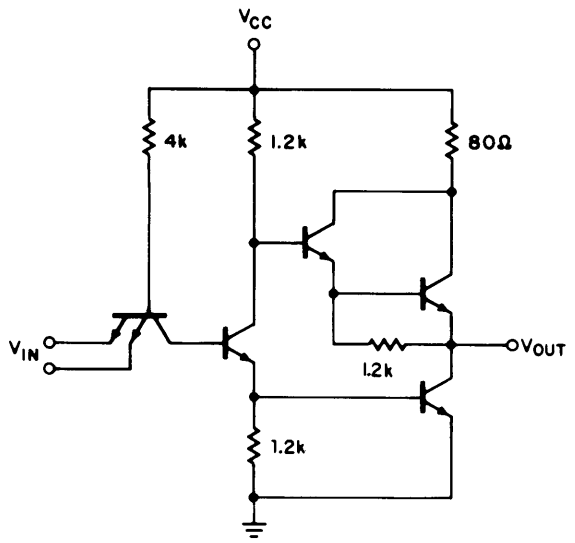


Figure 1-1. Classic TTL Design

Integrated circuit designers have found these design techniques to be ideal for implementing and producing more complex monolithic subsystems. Figure 1-2 provides an indication of the speed/power trade-off available to the designer using classic TTL configurations. The trade-off is achieved by varying the resistor values shown in the classic TTL NAND.

Internal design requirements for switching speed and fan-out allow the MSI circuit designer to keep the power consumption and die size within the design constraints of present packages while maintaining speed performance consistent with TTL.

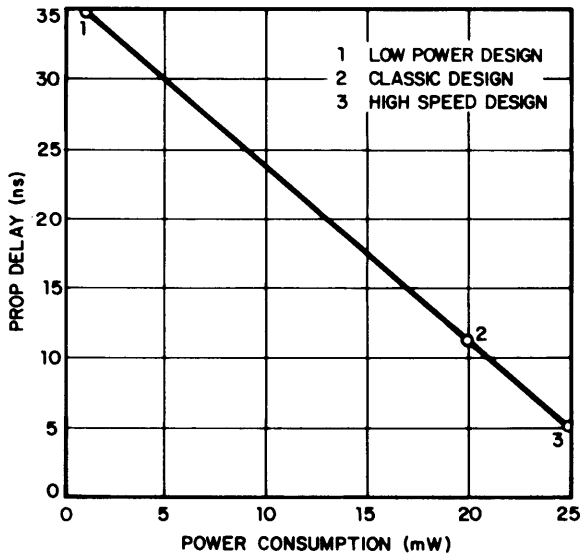


Figure 1-2. Speed Power Trade-Off in TTL Designs

A subsystem implementation of the speed/power trade-off is demonstrated in Figure 1-3. In this counter configuration, each binary operates at one-half the frequency of the preceding binary. Therefore, the designer may choose the high speed TTL configuration for the first binary, the classic TTL configuration for the second binary, and the low power design for the last two binaries. This design approach would result in an MSI counter with input clock rates above 50 MHz and the power consumption consistent with flat packages and military temperature range.

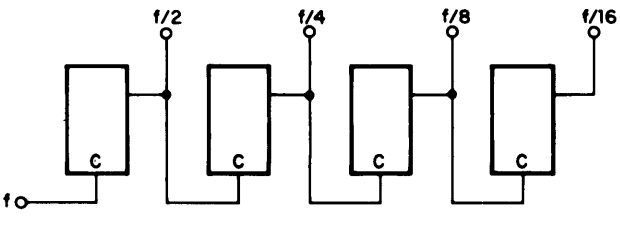


Figure 1-3. 4-Bit Binary Ripple Counter

Close consideration of internal fan-out requirements affords the MSI designer an opportunity to reduce component count and die area for a given logic function. Figure 1-4 shows a counter arrangement containing several AND-OR functions requiring a fan-out of one. The implementation of this function is shown in a standard package solution (Figure 1-5a) and in the MSI design (Figure 1-5b). Component count in the MSI design has been reduced to little more than one-third the standard package solution.

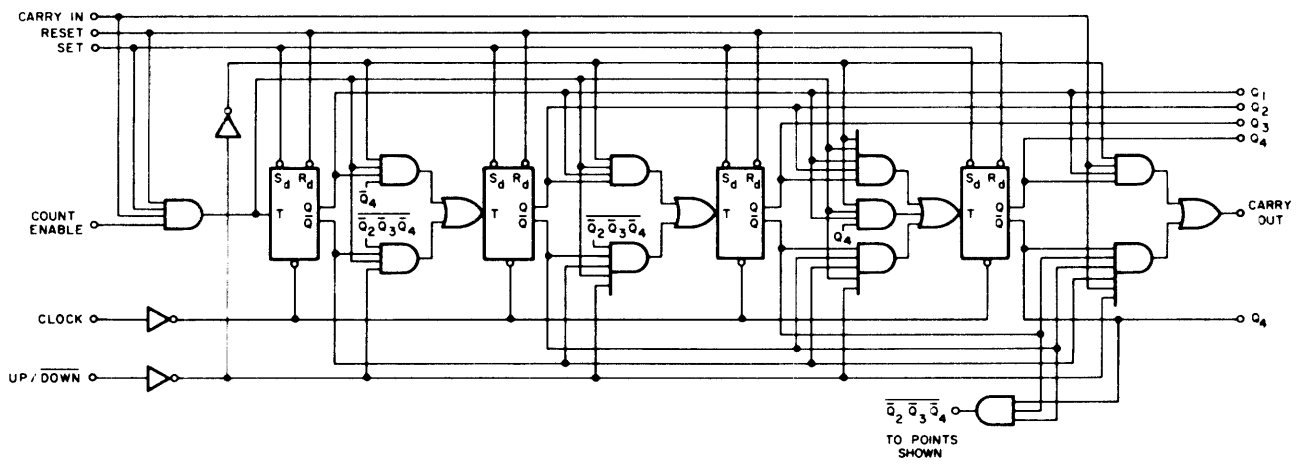


Figure 1-4. 8285 BCD Synchronous Up/Down Counter Logic Diagram

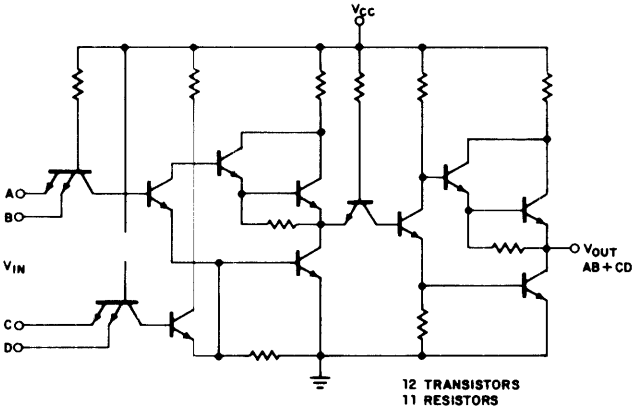


Figure 1-5a. Discrete Solution

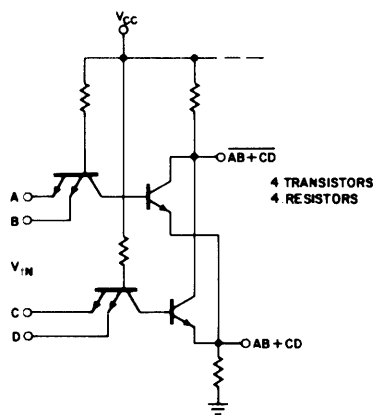


Figure 1-5b. MSI Solution

ELECTRICAL AND PHYSICAL SYSTEM DESIGN CONSIDERATIONS

Certain guidelines should be observed to ensure optimum system performance. Systems incorporating TTL elements such as gates, binaries and MSI circuits have inherent V_{CC} and GROUND transients attributable to the current spike produced by "totem pole" output structures. Figure 1-6 provides a synopsis of the commonly used totem pole structures which current spike.* MSI designs use similar structures to buffer outputs and inputs to increase fan-out and switching speed while reducing input loading.

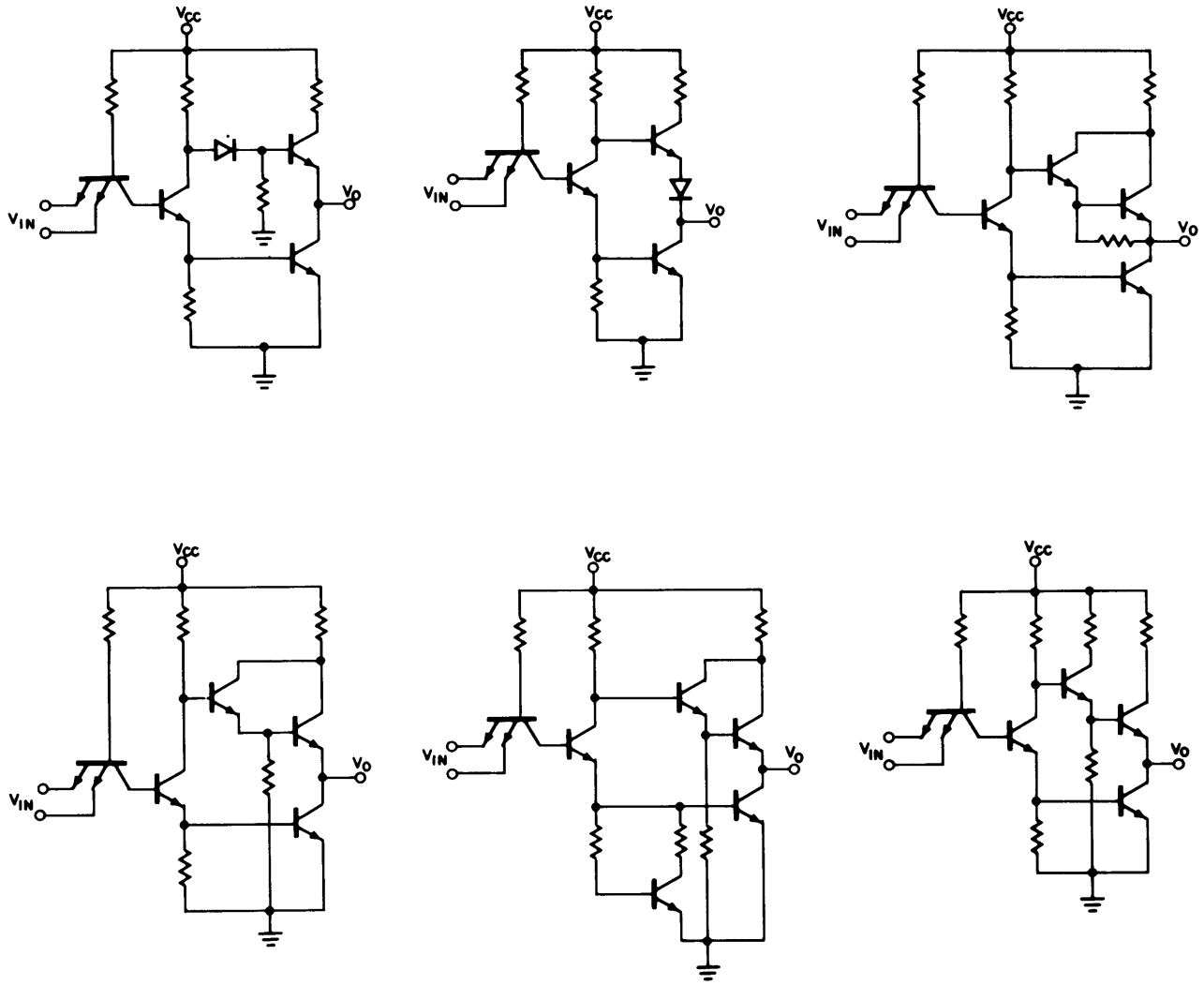


Figure 1-6. Common Totem Pole Output Structure

*See Appendix I.

DECOUPLING MSI

The current spike produced by the totem pole output structure during switching transitions can cause MSI subsystems to malfunction if V_{CC} is not adequately decoupled to GROUND. A capacitance of 2000pF or more, for each totem pole structure should be connected from V_{CC} to GROUND. The non-inductive capacitor (ceramic disc, tantalum slug, etc.) should be mounted with leads as short as possible and should be placed in close proximity to the MSI package to minimize lead length inductance. A properly designed printed circuit board should have the total required capacitance evenly distributed throughout the board. Example: A printed circuit board contains 25 packages averaging four totem pole structures per package. The total capacitance required is 25 packages x 4 totem pole structures x 2000pF or 0.2 μF. Ten 0.02 μF ceramic disc capacitors evenly distributed, satisfy the V_{CC} to GROUND decoupling requirements.

POWER SUPPLY AND GROUND DISTRIBUTION SYSTEMS

High-frequency distribution techniques should be used for V_{CC} and GROUND. These techniques should include a large ground plane to minimize DC offsets and to provide an extremely low impedance path to reduce transient voltage signals on the printed circuit board. The power supply should be -5V ±5% with R-F (1 GHz) bypassing. Catastrophic damage can occur if V_{CC} is not properly regulated.

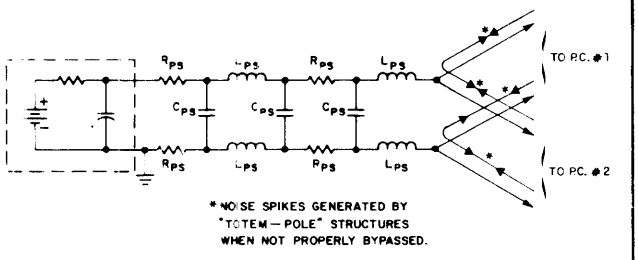


Figure 1-7. Power Characteristic Impedance

Power distributed from the main supply must, by necessity, come through a path which displays finite resistance (R_{PS}), inductance (L_{PS}) and capacitance (C_{PS}), as illustrated in Figure 1-7. The resistive component of the power lines is small, producing very little DC voltage drop at the V_{CC} and GROUND inputs to the printed circuit board. However, the inductance in the power lines can cause the noise generated by current spiking to be transmitted throughout the system on the V_{CC} and GROUND lines. If the printed circuit boards are adequately decoupled, the power line noise will be reduced significantly. In order to repel power line noise transmitted to a printed circuit board, ferrite beads may be placed on the incoming V_{CC} and GROUND lines as shown in Figure 1-8. A 10 μF tantalum capacitor, per 25 packages, connected from V_{CC} to GROUND should be placed on the printed circuit board in the position shown. In conjunction with the distributed ceramic disc capacitors, the approach will prevent most system malfunctions attributable to internally generated noise.

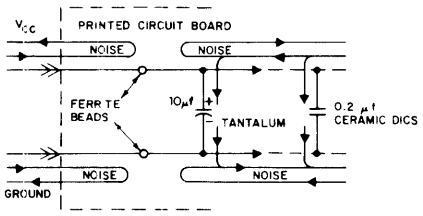


Figure 1-8. Ferrite Bead Isolation of Generated Noise

ISOLATION DIODES

NEVER REVERSE THE V_{CC} AND GROUND POTENTIALS. Catastrophic failure can occur if more than 100mA is conducted through a forward biased substrate (isolation) diode.

DISPOSITION OF UNUSED INPUTS

Electrically open inputs degrade AC noise immunity as well as the switching speed of an MSI circuit. To optimize performance, each input must be connected to a low impedance source. Unused inputs should be tied to V_{CC}, GROUND or a driving source. When paralleling an unused input with a driven input of the same multiple emitter transistor (MET), care should be taken to remain within the "1" level fan-out specifications for the driving source. The AND or NAND structures do not affect the "0" level fan-out of the driving source. When an unused input of an OR or NOR structure is commoned with a driven input, both the "1" and "0" level fan-out of the driving source are affected.

If fan-out of the driving source will be exceeded or if there is no convenient connection to an appropriate driven input, a second method of avoiding open inputs should be observed. Inputs which activate on "0" (AND and NAND) may be tied directly to V_{CC} or tied to V_{CC} through a current limiting resistor. To determine the requirements for current limiting, examine the input "latch-back" characteristic of the MET. This check is performed by grounding all but one of the emitters of the MET. Force 10mA into the ungrounded emitter and examine the "breakdown" characteristics on a curve tracer. If "breakdown" is greater than 6.0V and there is no evidence of latch-back or secondary break-

down, an unused input may be tied directly to V_{CC}. If the breakdown voltage or latch-back characteristic approaches 5.5V at 10mA, the input should be tied to V_{CC} through a current limiting resistor of 1 KΩ or more. More than one unused input can be tied to V_{CC} through a single resistor.

The 8200 series of MSI subsystems does not exhibit a latch-back characteristic. A current limiting resistor is required, however, if power supply transients can exceed 6.0V for longer than 1μsec. The power dissipated in the emitter junction during breakdown can destroy the junction. Current limiting provisions in accordance with the ABSOLUTE MAXIMUM RATINGS will ensure against catastrophic failure should breakdown occur.

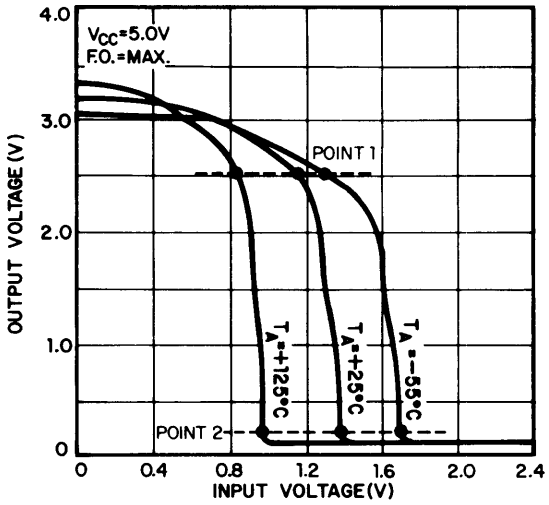


Figure 1-10. TTL Transfer Characteristic

INPUT CLAMP DIODES

MSI circuits contain input clamp diodes as shown in Figure 1-9. At the input, these diodes limit negative excursions which exceed -1V by providing a low impedance current source from GROUND through the forward biased diode clamp. The clamps are designed to minimize ringing which may be induced on interconnect wires in excess of six inches in length.

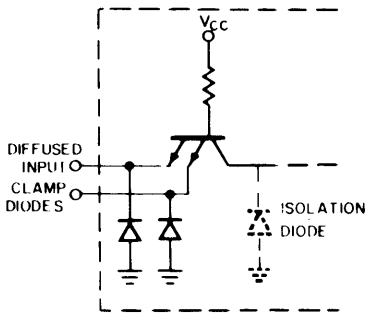


Figure 1-9. Input Clamp Diodes

SIGNAL PROCESSING

The rise and fall times* of all incoming data signals should be less than 200ns. The amplitude of incoming data signals should be 2.6V or greater. Figure 1-10 shows the transfer characteristic of the classic TTL gate. In the input threshold region, from point one to point two, the gate has approximately 25dB of gain. In this region, any discontinuity of the input waveform will be amplified more than 10 times at the output of the gate.

Should the input voltage remain in the threshold region (approximately 200mV wide) for more than 15ns, a typical TTL gate will oscillate as shown in Figure 1-11. The equivalent circuit in Figure 1-12 illustrates the potential oscillatory feed-back paths. The primary contributor to oscillation is the changing power supply voltage within the chip, caused by the current spiking which occurs during switching transitions. Since output voltage is directly proportional to V_{CC} and threshold voltage tends also to drop with lower supply voltage, the net effect is a positive feedback loop from output to input.

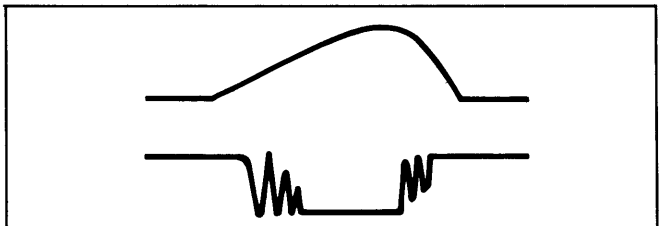


Figure 1-11. Typical TTL Gate Oscillation

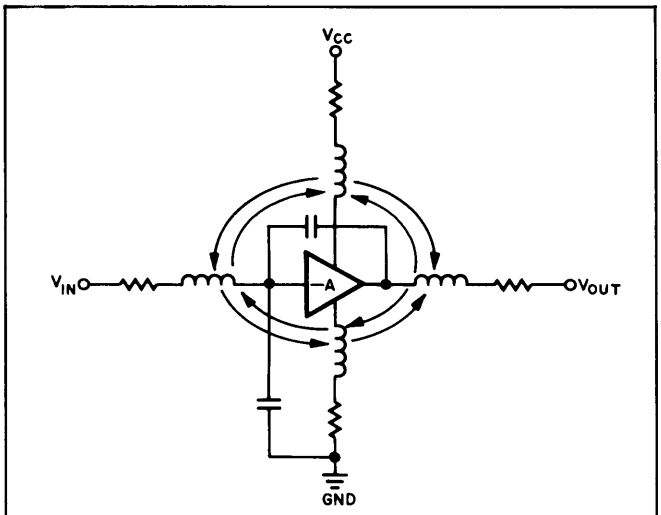


Figure 1-12. Potential Oscillatory Feedback Paths

*Rise and fall times are measured at the 10% and 90% points.

Whenever there is a question concerning the quality of incoming data signals, some signal shaping network should be used to ensure reliable system operation. Figures 1-13 and 1-14 provide suggestions for implementing adequate pulse shaping.

The output impedance of all driving sources should be less than 100Ω. A low source impedance minimizes capacitively coupled noise as well as the effects of a changing DC load observed in the input threshold region of the driven input. This load characteristic is shown in Figure 1-15 for a classic TTL gate.

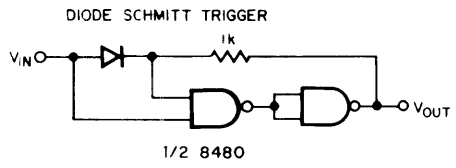


Figure 1-13. Signal Shaping Network

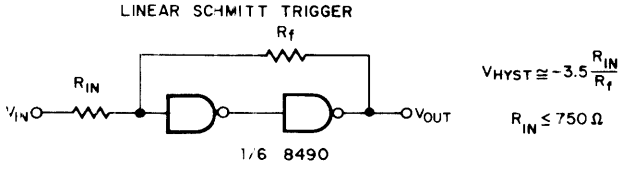


Figure 1-14. Signal Shaping Network

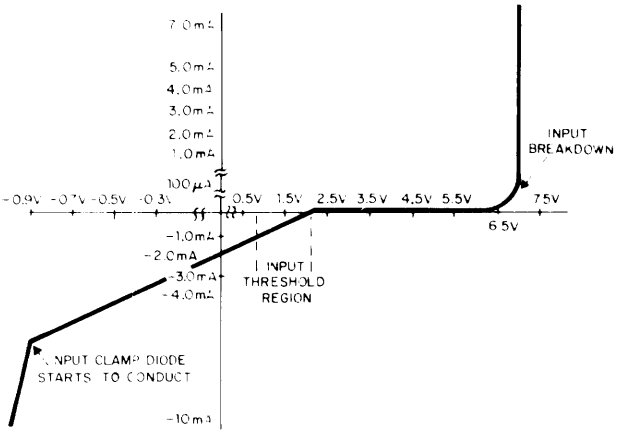


Figure 1-15. DC Input Load vs. Input Voltage

SECTION II

ASYNCHRONOUS MSI COUNTERS

Signetics offers a variety of asynchronous MSI counters. These counters have two things in common: 1) the output of one binary is connected to the Clock input of the following binary, in "ripple" fashion, and 2) each binary is clocked on the negative-going edge of the output transition of the preceding binary or the clock inputs. Thus, the N^{th} binary is activated on the falling edge of the output transition of the N-1 binary, as illustrated in Figure 2-1.

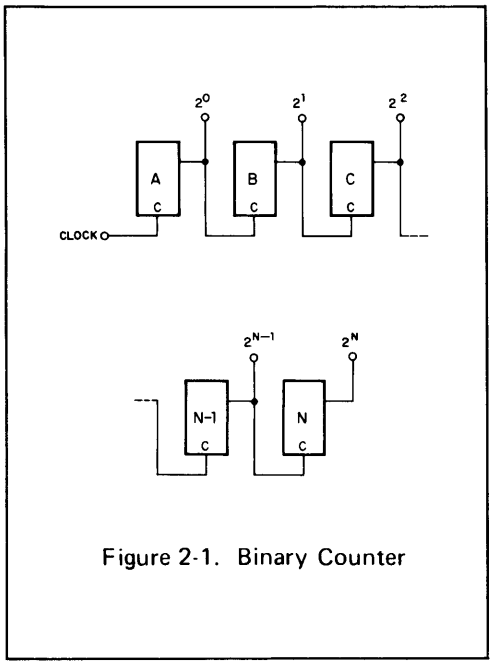


Figure 2-1. Binary Counter

Modified ripple counters have two or more binary clock inputs tied together. With proper gating of the information at the J-K inputs, a modified ripple counter can be designed to produce any desired binary counting sequence. The 8280 BCD Decade Counter (Figure 2-7) and the 8288 Divide-by-Twelve (Figure 2-17) are examples of modified ripple counters. All ripple and modified ripple counters are defined as asynchronous counters.

Asynchronous counters have two distinct advantages over other counter configurations. Power consumption can be minimized, utilizing the fact that each binary does not have to be operated at the incoming frequency. In a binary ripple counter, each binary operates at one-half the frequency of the preceding binary. Complexity and power consumption are reduced since little or no gating is required between binaries. The logic simplicity of these counter configurations allow small die sizes enhancing total yield. These advantages result in a relatively low price for asynchronous counters.

Asynchronous counters traverse intermediate output codes during single clock intervals. This characteristic is demonstrated for the 8281, 4-Bit Binary Ripple Counter in Figure 2-2. The traversed state(s) can last from 10 to 80ns depending on the next code in the output sequence. The intermediate codes and their approximate duration is shown in Figure 2-3 for a 4-Bit Binary Ripple Counter. The intermediate codes for modified ripple counters depend on the internal common clock connections and the internal gating. Each modified ripple counter must therefore be considered separately. An example of the intermediate output codes for the 8280, BCD Decade Counter is shown in Figure 2-4. Note that B-bit and D-bit of the 8280 are clocked simultaneously.

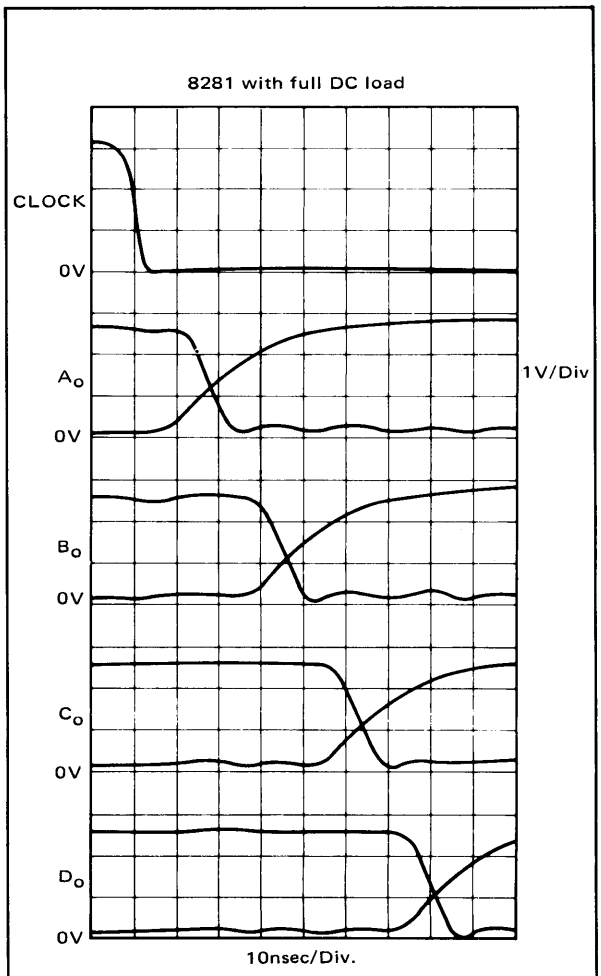


Figure 2-2. 8281, 4-Bit Binary Ripple Counter

CLOCK PULSE	DESIRED DECIMAL OUTPUT	INTERMEDIATE DECIMAL EQUIVALENT	WEIGHTED OUTPUT CODE				NUMBER OF INTERMEDIATE STATES	APPROX. DELAY TO DECODE DESIRED STATE
			A_O (1)	B_O (2)	C_O (4)	D_O (8)		
1	0		0	0	0	0	None	
2	1		1	0	0	0		
		0	0	0	0	0	One	40ns
3	2		0	1	0	0	None	
4	3		1	1	0	0		
		2	0	1	0	0	Two	60ns
		0	0	0	0	0		
5	4		0	0	1	0	None	
6	5		1	0	1	0		
		4	0	0	1	0	One	40ns
7	6		0	1	1	0	None	
8	7		1	1	1	0		
		6	0	1	1	0		
		4	0	0	1	0	Three	80ns
		0	0	0	0	0		
9	8		0	0	0	1	None	
10	9		1	0	0	1		
		8	0	0	0	1	One	40ns
11	10		0	1	0	1	None	
12	11		1	1	0	1		
		10	0	1	0	1	Two	60ns
		8	0	0	0	1		
13	12		0	0	1	1	None	
14	13		1	0	1	1		
		12	0	0	1	1	One	40ns
15	14		0	1	1	1	None	
16	15		1	1	1	1		
		14	0	1	1	1		
		12	0	0	1	1	Three	80ns
		8	0	0	0	1		
17	0		0	0	0	0		

Figure 2-3. 4-Bit Binary (16-State) Ripple Counter Output Sequence

CLOCK PULSE	DESIRED DECIMAL OUTPUT	INTERMEDIATE DECIMAL EQUIVALENT	WEIGHTED OUTPUT CODE				NUMBER OF INTERMEDIATE STATES	APPROX. DELAY TO DECODE DESIRED STATE
			A_O (1)	B_O (2)	C_O (4)	D_O (8)		
1	0		0	0	0	0	None	
2	1		1	0	0	0		
		0	0	0	0	0	One	40ns
3	2		0	1	0	0	None	
4	3		1	1	0	0		
		2	0	1	0	0	Two	60ns
		0	0	0	0	0		
5	4		0	0	1	0	None	
6	5		1	0	1	0		
		4	0	0	1	0	One	40ns
7	6		0	1	1	0	None	
8	7		1	1	1	0		
		6	0	1	1	0	Two	60ns
		12	0	0	1	1		
9	8		0	0	0	1	None	
10	9		1	0	0	1		
		8	0	0	0	1	One	40ns
11	0		0	0	0	0		

Figure 2-4. BCD Decade Modified Ripple Counter Output Sequence

In most applications of frequency division, intermediate codes are of no concern. Each output is considered separately, in terms of the number of activating (negative-going) pulses, and it produces in relation to the number of clock pulses observed at the clock input of the counter.

When decoding the outputs, in counting applications, care should be taken to ensure that the decoder is activated after the interval when intermediate codes may exist. An example of this decoding technique is shown in Figure 2-5.

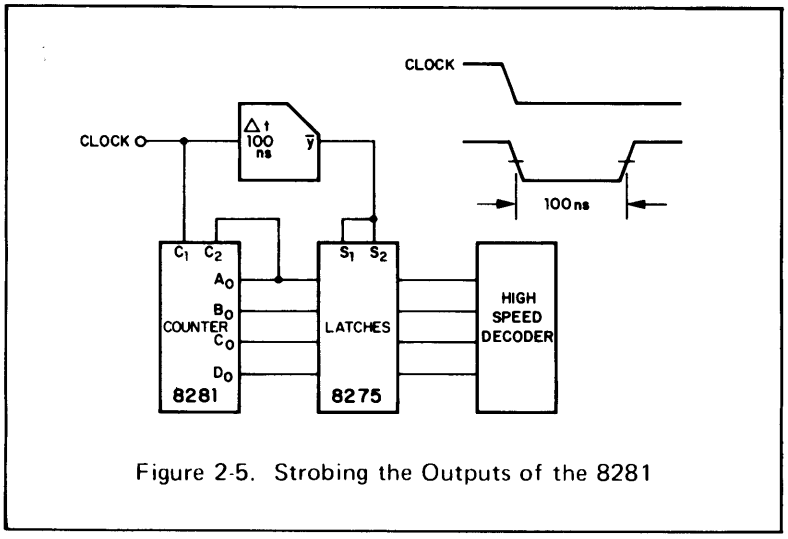
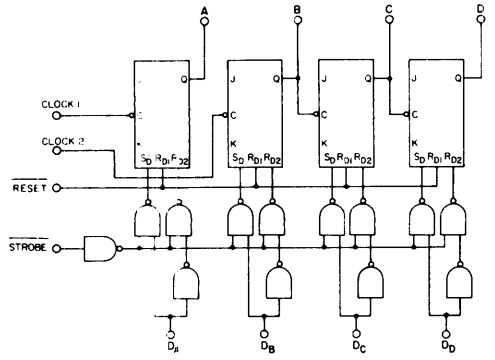


Figure 2-5. Strobing the Outputs of the 8281

OPERATION OF THE 8280 AND 8281

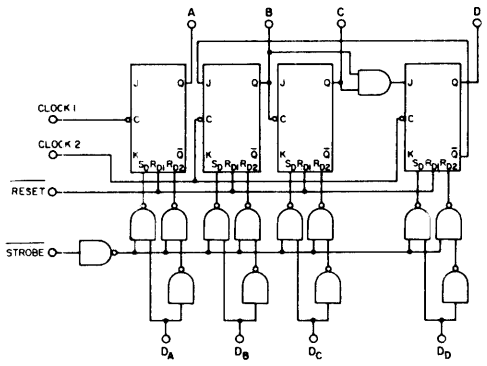
The logic diagram of the 8281 4-Bit Binary (16-State) Ripple Counter is shown in Figure 2-6. Figure 2-7 is the logic diagram of a modified ripple configuration, the 8280 BCD Decade Counter. Both counters consists of four presettable binary elements of the design shown in Figure 2-8a. The



A_{out} = 8.0mA C_{out} = 6.4mA
B_{out} = 6.4mA D_{out} = 6.4mA

Figure 2-6. 4-Bit Binary (16-State) Ripple Counter Logic Diagram of 8281

entire circuit schematic for the 8280 is shown in Figure 2-8b. The first binary is separated from the other three to provide applications flexibility. For example, the 8280 may be arranged as a BCD decade counter or as a Bi-Quinary (10-state) counter. The specifics of application flexibility will be discussed later in this section.



A_{out} = 9.6mA C_{out} = 6.4mA
B_{out} = 6.4mA D_{out} = 6.4mA

Figure 2-7. BCD Decade Counter Logic Diagram of 8280

Classic TTL design of these counters makes the input and output characteristics compatible with all popular DTL and TTL products available. The output switching transistor (Q7 of Figure 2-8) provides a "0" level fan-out of four (6.4mA at 0.5V) for each output. The A-bit is guaranteed to drive Clock 2 (an additional 1.6mA for the 8281 and 3.2mA for the 8280) while maintaining the fan-out of four rating. The active pull-up (Q6 of Figure 2-8) will source 200μA, while maintaining a 2.6V minimum "1" level.

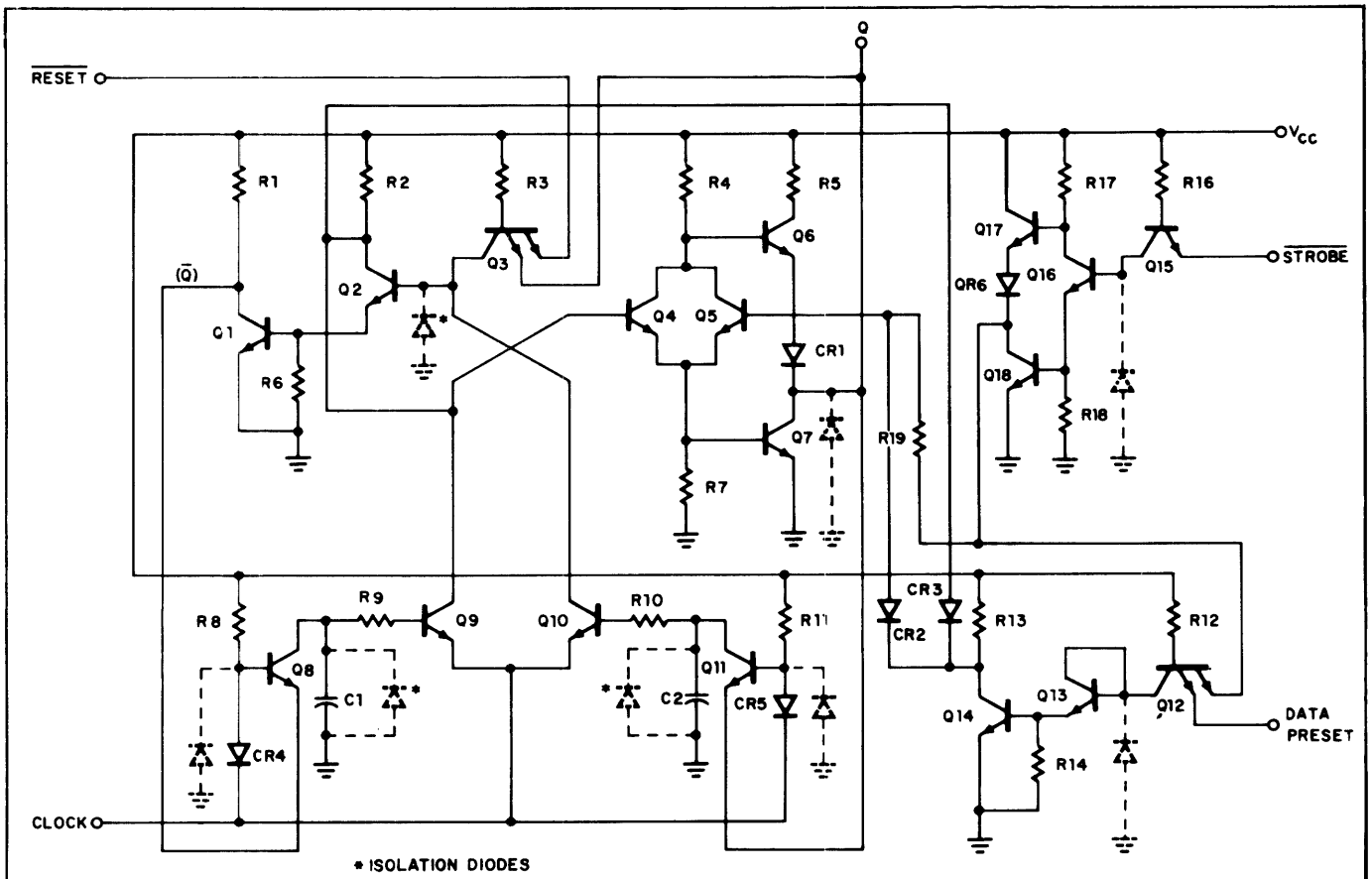


Figure 2-8a. Basic Circuit Schematic of the 8281

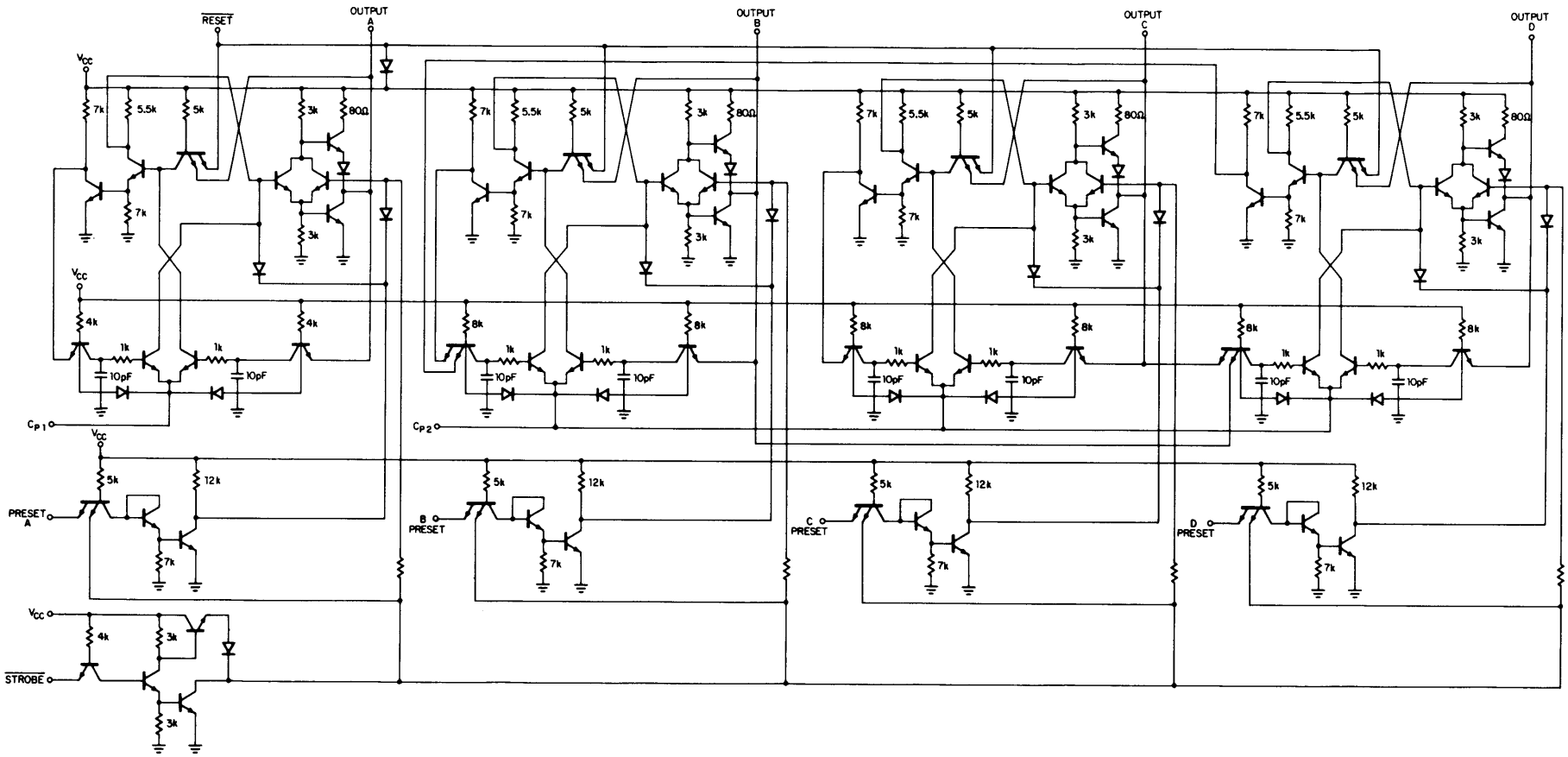


Figure 2-8b. Circuit Schematic of the 8280

The parallel preset inputs (D_A, D_B, D_C, D_D) are enabled by a "0" on the $\overline{STROBE}$ input, affecting a parallel data transfer to the respective counter outputs. The $\overline{STROBE}$ input is buffered to reduce its input load to 1.6mA. This asynchronous parallel entry system is direct coupled, and therefore, is sensitive to DC input voltage levels only. The preset capability allows either counter to be utilized as event counters, fixed quantity totalizers, arbitrary length frequency dividers, and as storage registers.

The 8280 and 8281 can also be reset or cleared to zero (all outputs go to "0") asynchronously. The direct coupled $\overline{RESET}$ input activates on "0" level. $\overline{RESET}$ is not buffered and represents a load of 5.0mA at "0".

A stored-charge clocking mechanism activates each binary on the negative-going edge of its clock signal. The first binary of each counter will accept clock (CLOCK 1) input repetition rates in excess of 30 MHz. The CLOCK 2 input for the B-, C- and D-bits will operate reliably at clock frequencies up to 20 MHz. The operating frequency of the last three binaries was reduced to decrease the total power consumption of the counters, while operating at frequencies consistent with most applications requiring Bi-Quinary or divide-by-five configurations.

System Design Implementation

In all applications of the 8280 and 8281, certain design practices should be followed to ensure optimum system reliability. The most prevalent system malfunctions are analyzed here in order of occurrence. The specific recommendations are extensions of the design criteria discussed in Section I.

Decoupling

Inadequate decoupling from V_{CC} to GROUND can cause system malfunctions. The 8280 and 8281 contain four outputs and one internal totem pole structure which current spike. A 0.01μF capacitor is required to achieve adequate decoupling. The ceramic disc capacitor should be placed as close as possible to the counter package.

Signal Processing/Clock Input Requirements

Each binary exhibits the clock characteristics inherent in stored-charge flip-flops. The change of state occurs on the negative-going edge of the clock pulse. The clock pulse amplitude should be 2.6V or greater with a minimum pulse width of 25ns at the 1.5V points. Because stored-charge binaries are AC coupled, activation of the CLOCK input is somewhat sensitive to the rate of fall (dv/dt) of the negative-going signal. Independent of pulse width, the clocking signal must fall from the 2.6V level in less than 75ns. The fall time is measured from the 90% to 10% points of the falling waveform.

Negative Excursions at the Clock Input

Should the CLOCK input signal exceed one diode drop below ground (-0.6V to -0.7V) both Q9 and Q10 (Figure 2-8) begin to turn on due to the availability of base drive through the isolation diodes. Turn on of Q9 and Q10 causes turn-off of Q4 and Q2, respectively. This condition forces both sides of the binary to "1" and erases the previously stored data. On recovery, the binary may arbitrarily store either "1" or "0", completely independent of the preceding state. Negative excursions at the CLOCK input are usually the result of long clock lines, and/or mismatched line impedances. Adequate protection for the clock inputs may be provided by buffering the incoming clock line or clamping the CLOCK input with a germanium diode. The germanium diode, connected between CLOCK and GROUND will provide a low impedance current source, clamping the CLOCK at approximately -0.3V.

Entering Parallel Data

The entry of preset data is accomplished by presenting the desired 4-bit output code at the appropriate parallel data input (D_A, D_B, D_C, D_D) and activating $\overline{STROBE}$ by applying "0".

In most system applications, special timing considerations are required when entering parallel data. Assuming that there is no activating (negative-going) pulse at CLOCK 1, a strobe interval of 50ns is sufficient to enter and hold parallel data when the resulting 4-bit output code is 1 1 1 1. However, should an activating signal occur at CLOCK 1 while $\overline{STROBE}$ is active or should the CLOCK of any of the bits be activated by a "1" to "0" transition at the output of the previous bit, a strobe interval of 250ns may be required. The typical strobe holding time under these conditions is 150ns. Although the counter outputs are held at a DC logic level, a clocking transition at any of the binary CLOCK inputs will cause a transient condition at the collector of Q_1 (the $\bar{Q}$ connection, Figure 2-8). $\overline{STROBE}$ and DATA inputs must remain stable for the duration of the transient condition to

ensure the desired output code will be retained. A representation of this transient condition is shown in Figure 2-9. The details of the transient conditions are discussed in the description of operation.

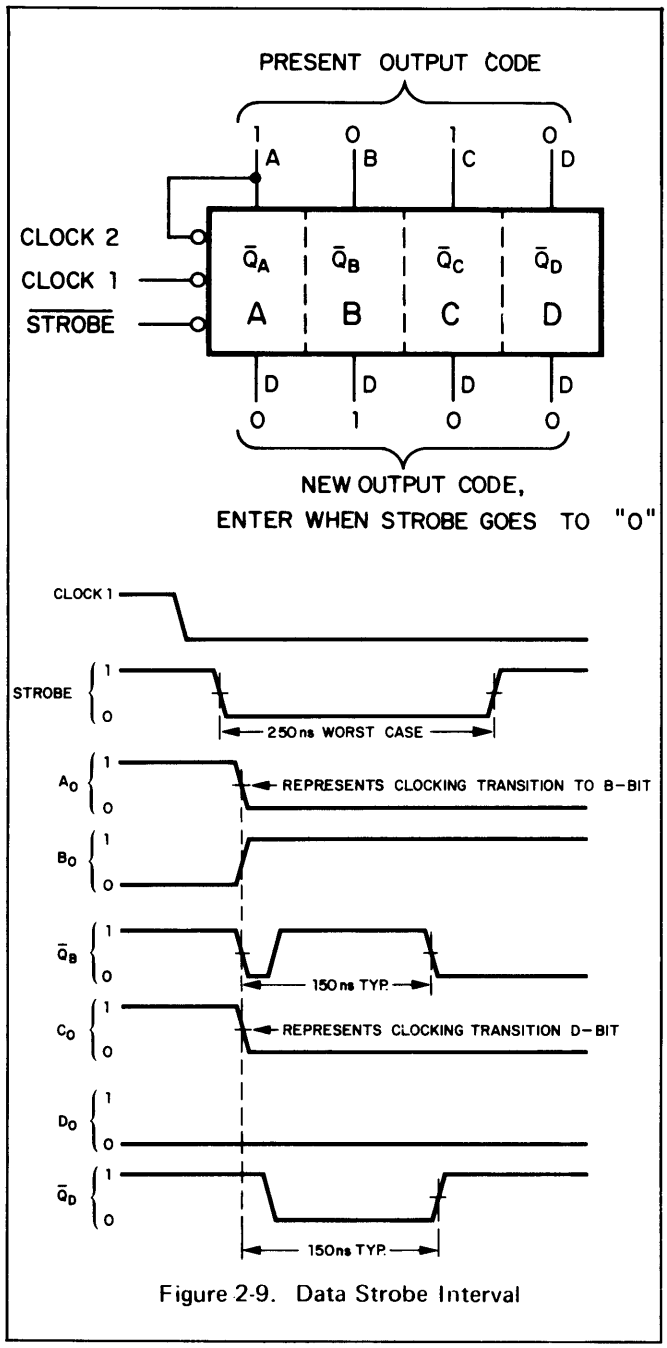
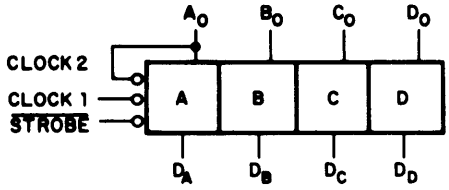


Figure 2-9. Data Strobe Interval

Parallel Entry of Undefined Codes

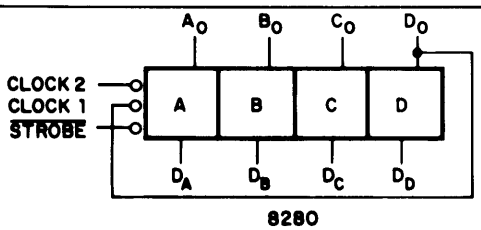
It is possible to enter parallel output codes which are not in the normal count sequence of the 8280 BCD Decade Counter. Specifically, the binary representation of 10, 11, 12, 13, 14 and 15 can be strobed into the counter. A maximum of two clock pulses will ensure that the counter has returned to an output code within the normal output sequence. Once the defined output code has been reached, the counter will continue a normal up-count as CLOCK is activated. Should binary 10 or 12 be entered, the counter will return to a normal output sequence at binary 4, after the second clock pulse. If binary 14 is entered, the 8280 will return to a normal output sequence at binary 0 after the second clock pulse. One clock pulse is required to return the count to a normal sequence at binary 4 when either binary 11 or 13 is entered. One clock pulse is sufficient to return the counter output to binary 0 if preset to binary 15. These sequences are summarized in Figure 2-10.



UNDEFINED BINARY PRESET	OUTPUT CODE A_O (1)	B_O (2)	C_O (4)	D_O (8)	DECIMAL OUTPUT SEQUENCE	NUMBER OF CLOCK PULSES	LOGIC STATUS OF OUTPUT CODE
10	0	1	0	1	10	0	Undefined Preset
	1	1	0	1	11	1	Undefined Count
	0	0	1	0	4	2	Defined Count
11	1	1	0	1	11	0	Undefined Preset
	0	0	1	0	4	1	Defined Count
12	0	0	1	1	12	0	Undefined Preset
	1	0	1	1	13	1	Undefined Count
	0	0	1	0	4	2	Defined Count
13	1	0	1	1	13	0	Undefined Preset
	0	0	1	0	4	1	Defined Count
14	0	1	1	1	14	0	Undefined Preset
	1	1	1	1	15	1	Undefined Count
	0	0	0	0	0	2	Defined Count
15	1	1	1	1	15	0	Undefined Preset
	0	0	0	0	0	1	Defined Count

Figure 2-10. Parallel Entry of Undefined Codes for 8280 Operating as BCD Decade Counter

When operating in the Bi-Quinary counting mode one activation of CLOCK 2 is required to return the 8280 to a defined output code. The six undefined codes which can be entered into the counter are summarized in Figure 2-11.



UNDEFINED PRESET ENTERED	BI-QUINARY OUTPUT B_O	C_O	D_O	A_O	DECIMAL OUTPUT SEQUENCE	NUMBER OF CLOCK PULSES	LOGIC STATUS OF OUTPUT CODE
10	1	0	1	1	10	0	Undefined Preset
	0	1	0	0	2	1	Defined Count
11	0	1	1	1	11	0	Undefined Preset
	0	1	0	0	2	1	Defined Count
12	1	1	1	1	12	0	Undefined Preset
	0	0	0	0	0	1	Defined Count
"5"	1	0	1	0	"5"	0	Undefined Preset
	0	1	0	1	7	1	Defined Count
"6"	0	1	1	0	"6"	0	Undefined Preset
	0	1	0	1	7	1	Defined Count
"7"	1	1	1	0	"7"	0	Undefined Preset
	0	0	0	1	5	1	Defined Count

Figure 2-11. Parallel Entry of Undefined Codes for 8280 Operating in Bi-Quinary (10-State) Mode

Resetting the 8280 and 8281

Reset holding time as shown for the 8281 in Figure 2-12. In this configuration, CLOCK 1 is activated ("1" to "0" transition) while $\overline{\text{RESET}}$ is active ("0"). The CLOCK 1 transition causes A_O to generate a pulse about 160ns wide. On the falling edge of A_O, CLOCK 2 is activated, causing a pulse of 140ns duration at the B-bit output. The B_O pulse clocks the C-bit which in turn clocks the D-bit. If more 8281s were cascaded (D_O of the first counter driving CLOCK 1 of the next counter), this pulse would continue to ripple through each bit in the chain. As with the $\overline{\text{STROBE}}$ input, the maximum duration of this pulse is 250ns. However, because the pulse is occurring at the Q output of each element, it ripples through the entire counter, one bit at a time. Therefore, the reset hold time may be as long as 250ns per bit. Under normal operating circumstances, with CLOCK 1 gated out when $\overline{\text{RESET}}$ is active, a maximum reset hold time of 750ns per counter may be required.

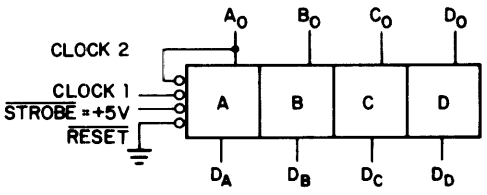
The 8280 requires 250ns less reset holding time per counter. Since the B- and D-bits of the 8280 are clocked from A_O, the worst case reset hold time is 500ns with CLOCK 1 gated out when $\overline{\text{RESET}}$ is active. Should CLOCK 1 receive an activating pulse with $\overline{\text{RESET}}$ active, 750ns maximum will be required to complete the reset operation. Details of the reset function are presented in the description of operation.

Maximum Capacitive Loading

When a capacitive load in excess of 100pF is placed on any output of the 8280 or 8281, that binary may fail to "latch" when clocked to "1". Should the binary fail to latch, the output will fall to "0" again, generally clocking the next binary. A common example of capacitive overload occurs when trying to drive a 1 megohm input to an oscilloscope from the D_O output through a 50Ω coaxial cable. The decade counter may count-up normally from zero to eight, then produce a narrow pulse at D_O. In this configuration, the effective capacitance load at the D_O output approaches 400pF. A 10:1 ten megohm probe provides an adequate solution.

Description of Operation

$\overline{\text{RESET}}$ and $\overline{\text{STROBE}}$ are inactive ("1") while the binary in Figure 2-8 is toggling normally. Assuming an initial condition of Q = "0" and $\overline{Q}$ = "1". C_1 will charge from V_{CC} through R8 and the base-collector junction of Q_8 when CLOCK goes to "1". At the same time, C_2 discharges through Q_{11} and the output transistor, Q_7. When CLOCK is returned to "0", the current through R8 (C_1 charge current) is diverted away from the base of Q_8 through CR4. The base drive for Q_{11} is also diverted, through CR5, and C_2 stops discharging. With CLOCK at "0", the emitters of Q_9 and Q_{10} are now low. C_2 has discharged however, and Q_{10} is without base drive and cannot conduct. C_1, which charged when CLOCK was high, now discharges into the clock line through R9 and the base-emitter junction of Q_9. This discharge current turns Q_9 on which, in turn, clamps the collector of Q_2 at "0" and hold Q_4 off. With $\overline{\text{STROBE}}$ at "1", Q_{18} has been on holding Q_5 off. When both Q_4 and Q_5 turn off, Q_7 turns off putting Q at "1". With $\overline{\text{RESET}}$ inactive, the current through R3 is diverted through the base-collector junction of Q_3 causing Q_2 to turn on. The turn-on of Q_2 reinforces the turn off of Q_4 and forces Q_1 on ($\overline{Q}$ to "0"). C_2 is allowed to charge from V_{CC} through R11 and the base-collector junction Q_{11} when the CLOCK goes to "1". With the emitter of Q_8 at "0", C_1 completely discharges through that transistor and Q_1 when the CLOCK goes to "1". It follows that on the next activating ("1" to "0" transition) edge of the CLOCK input, the binary will toggle to its original state $\overline{Q}$ = "1", Q = "0".



8281

RESET INTERVAL REQUIRED AFTER LAST CLOCKING TRANSITION

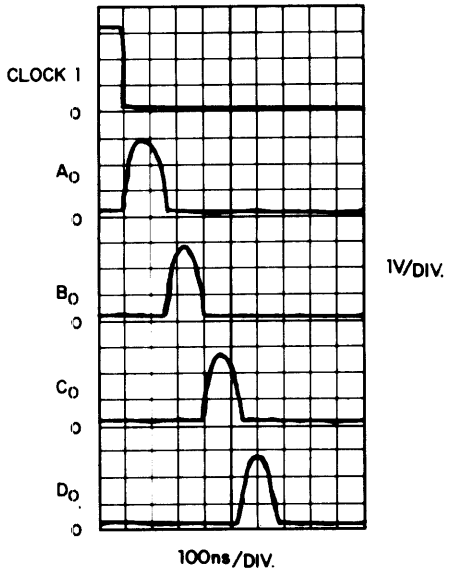


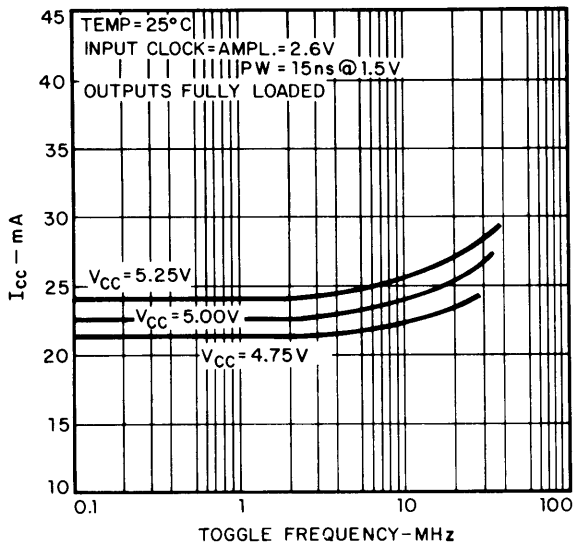
Figure 2-12. Reset Holding Time for 8281

In the normal operating mode, Q_8 of Q_{11} discharges its respective capacitor while the other capacitor charges. Should $\bar{Q}$ be held high by activating $\overline{RESET}$, C_1 can discharge only through R9 and the base-emitter junction of Q_9 when the CLOCK input goes from "1" to "0". This discharge path holds Q_9 on turning Q_4 off for intervals in excess of 120ns. The Q output, of course, goes to a "1" level for the time Q_9 is on. As demonstrated in Figure 2-12, the pulse will ripple through each successive binary in the 8281. Again, the B-bit and D-bit of the 8280 are clocked simultaneously reducing the maximum number of pulses to three.

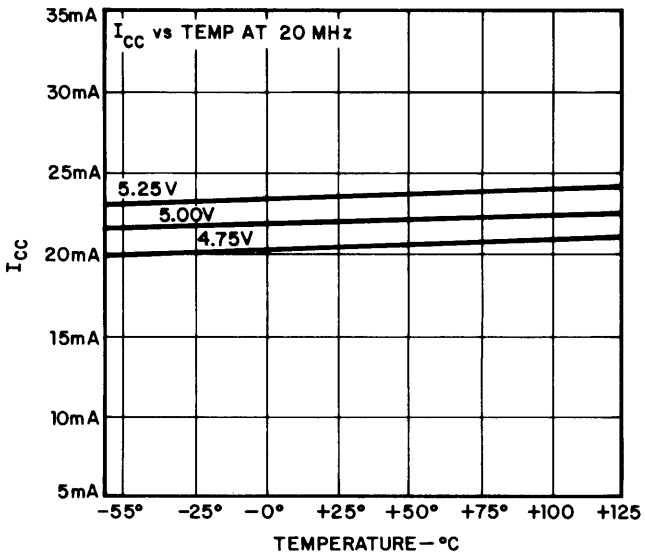
A similar pulse occurs internally at $\bar{Q}$ when Q is being strobed to "1" and a clocking transition occurs. However, since Q is being held at "1" and the $\bar{Q}$ output is isolated from the following binaries, there is no ripple of the pulse from one binary to the next.

AC Characteristics of the 8280 and 8281

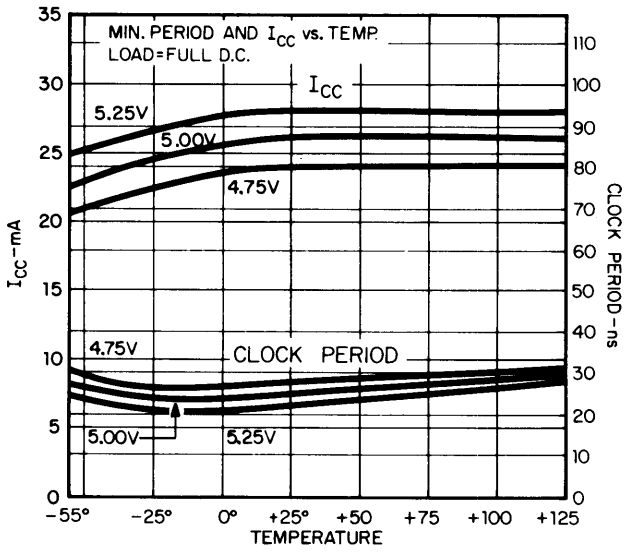
Some of the AC characteristics of the 8280 and 8281 are illustrated in Curves 2-1, 2-2 and 2-3. These curves show ONLY typical parameters and must not be construed as being guaranteed characteristics; however, assuming a possible deviation of up to ±25%, these curves demonstrate the rationale behind the guaranteed parameters.



CURVE 2-1: The variation of power supply current with clock frequency is shown for three values of V_{CC} (V_{CC} = 5.00V ±5%) and an ambient temperature of 25°C. All outputs are fully DC loaded.



CURVE 2-2: Shown is the variation of I_{CC} vs. temperature for V_{CC} = 5.00V ±5%. The clock frequency is 20 MHz. All outputs are fully DC loaded.



CURVE 2-3: This curve is a composite of two interdependent characteristics: the minimum period (max. freq.) and I_{CC} vs. temperature. This composite shows the variation with temperature of I_{CC} at the maximum frequency of operation with all outputs full DC loaded and for three values of V_{CC} (V_{CC} = 5.00V ±5%).

Although this data was taken only from the 8281, all general parameters are also characteristic of the 8280.

OPERATION OF THE 8290 BCD DECADE HIGH-SPEED RIPPLE COUNTER AND THE 8291 4-BIT BINARY HIGH-SPEED RIPPLE COUNTER

The 8290 BCD Decade Counter, Figure 2-13, and the 8291 4-Bit Binary (16-State) Ripple Counter, Figure 2-14, are pin-for-pin interchangeable with the 8280 and 8281, respectively. Three modifications have been incorporated to broaden significantly the scope of applications in which the spectrum of MSI ripple counters can be used. The modifications include guaranteed 40 MHz operation with typical frequency capability in excess of 70 MHz. The data strobe holding time has been reduced to 25ns maximum, with a typical requirement of 15ns. The reset holding time is 30ns maximum, while reset is typically accomplished within 20ns.

The design prevents clocking of any binary during the entry of asynchronous data ($\overline{\text{STROBE}}$ or $\overline{\text{RESET}}$ active). Activation of the asynchronous inputs put all J-K inputs at "0" preventing the toggle of any stage, should a clock pulse occur. Additionally, when the J-K terminals are held at "0", both clock capacitors discharge completely as seen in Figure 2-15. The $\overline{\text{RESET}}$ input dominates both CLOCK and $\overline{\text{STROBE}}$, while the $\overline{\text{STROBE}}$ input dominates CLOCK.

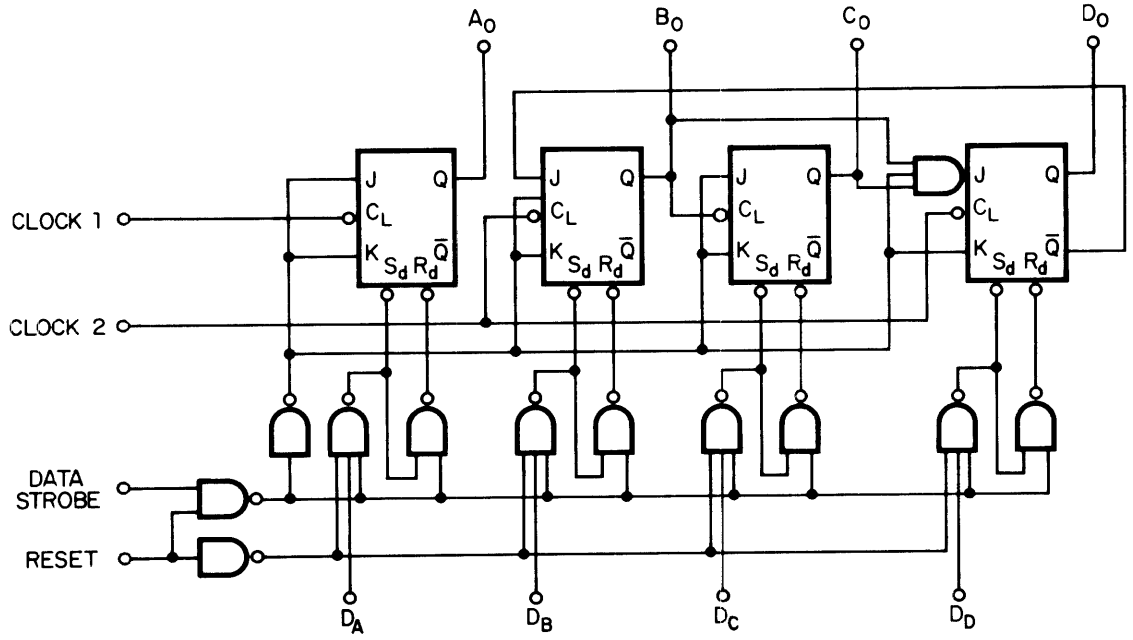


Figure 2-13a. The 8290 and 8292 BCD Decade Ripple Counters

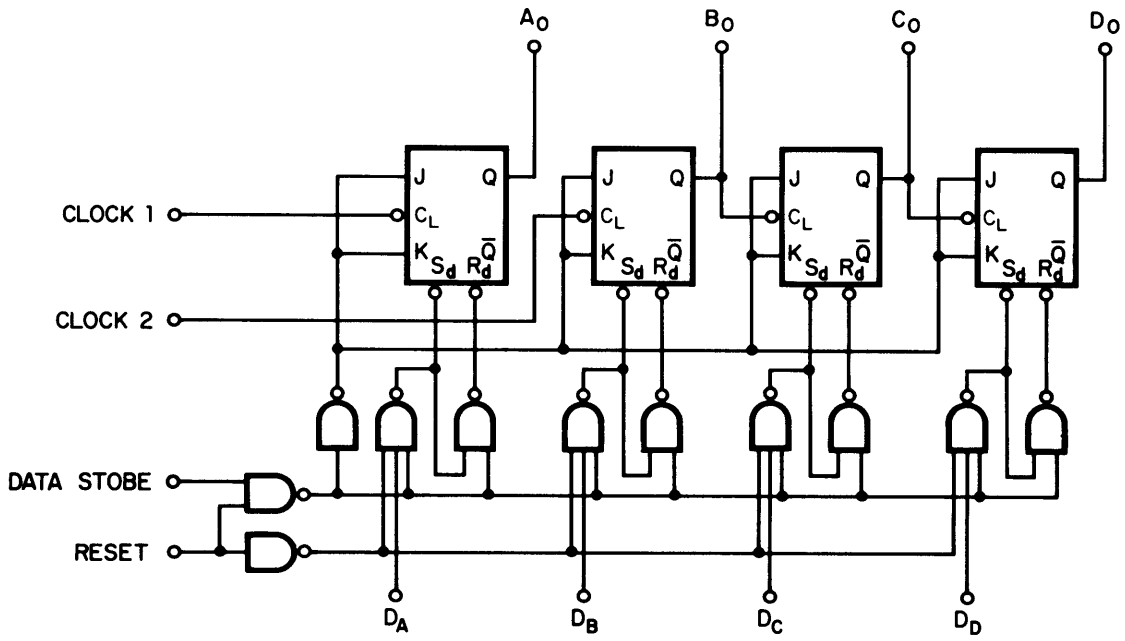
TRUTH TABLE
BCD DECADE MODE

CLOCK	A_O (1)	B_O (2)	C_O (4)	D_O (8)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0

TRUTH TABLE
BI-QUINARY MODE

CLOCK	B_O (1)	C_O (2)	D_O (4)	A_O (4)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	0	1
6	0	1	0	1
7	1	1	0	1
8	0	0	1	1
9	1	0	1	1
10	0	0	0	0

Figure 2-13b. The Logic Diagram for 8290 and 8292 BCD Decade Ripple Counters



TRUTH TABLE

CLOCK	A_O (1)	B_O (2)	C_O (4)	D_O (8)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1
16	0	0	0	0

Figure 2-14. The Logic Diagram for 8291 and 8293 4-Bit Binary Ripple Counters

Decoupling

The decoupling capacitor for the 8290 and 8291 should be 0.01 μF or more. The non-inductive capacitor should be mounted in close proximity to the counter package. Minimize lead inductance by keeping lead lengths to a minimum.

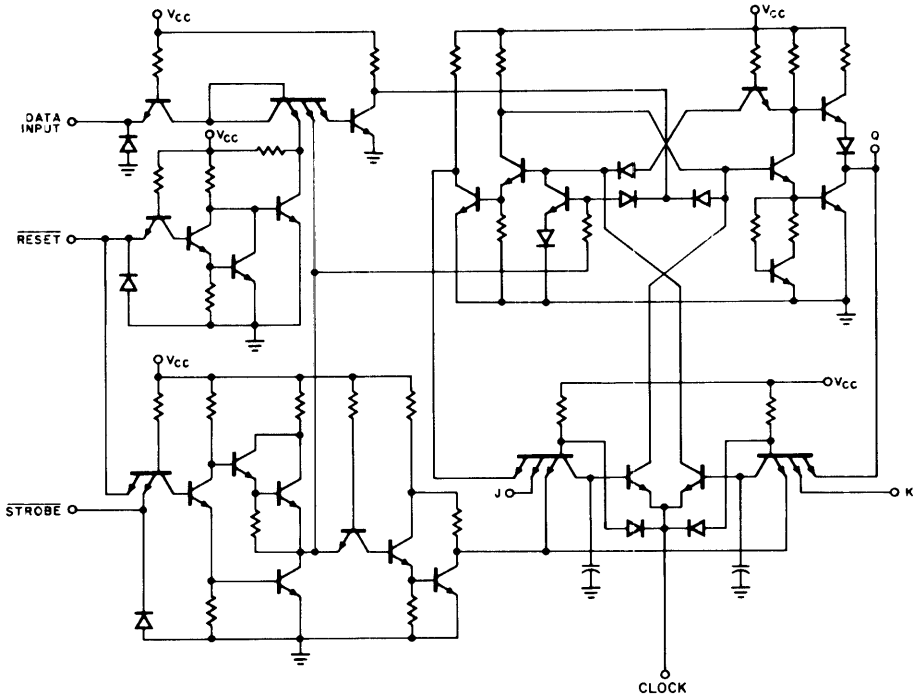


Figure 2-15a. 8288, 8290, and 8291 Basic Binary

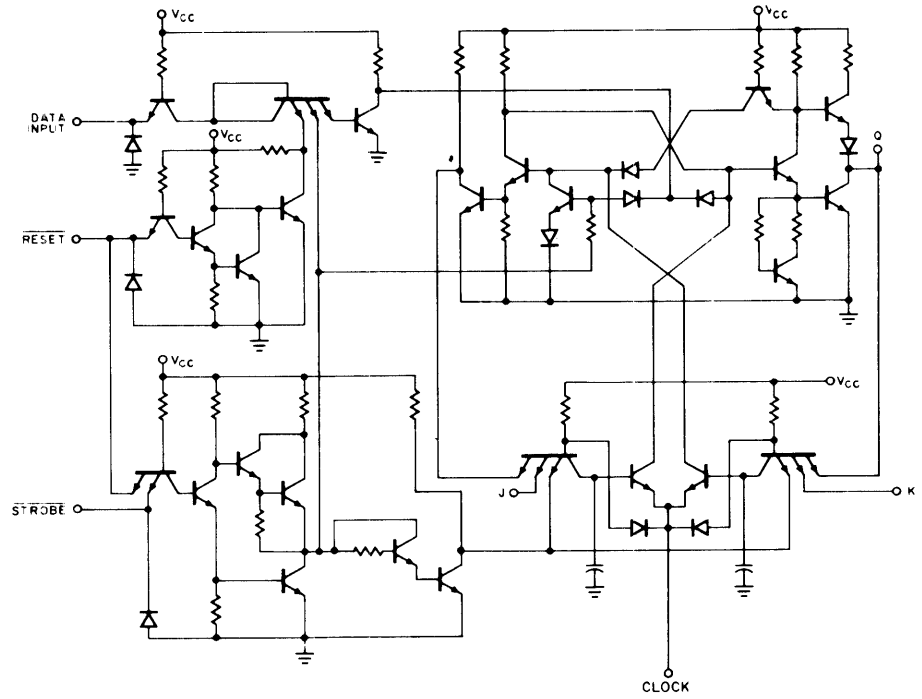


Figure 2-15b. 8292 and 8293 Basic Binary

Signal Processing/Clock Input Requirements

The 8290 and 8291 will operate reliably with clock pulse widths of 10ns or more. Clock pulse amplitude should be 2.6V or greater and the fall time should be limited to 75ns or less. The fall time requirement is independent of clock pulse width.

Asynchronous input ($\overline{\text{STROBE}}$, $\overline{\text{RESET}}$ and DATA preset) signals should maintain rise and fall times of less than 200ns as discussed in Section I.

Negative Excursions at the Clock Input

Negative ringing at the CLOCK input will not cause the 8290 or 8291 to malfunction. A diffused diode clamp limits negative excursions to about -1.0V and provides a low impedance current source which ensures that the isolation diodes will not become forward biased. Under these conditions the clocking transistors cannot turn on simultaneously.

Although negative ringing will not cause the counters to miscount, good layout techniques, as recommended in Section I, should be followed to keep the clock distribution system free from ringing.

Entering Parallel Data

The entry of any desired output code is achieved by placing that 4-bit code at the data inputs and strobing ($\overline{\text{STROBE}}$ = "0").

Because all clock capacitors are completely discharged on the activation of $\overline{\text{STROBE}}$, there are no transient conditions existing at the binary outputs. As a result, the complete parallel entry operation can be accomplished in a maximum of 25ns.

Parallel Entry of Undefined Codes

Output codes which are not contained in the normal 10-state output sequence may be parallel entered into the 8290. The binary representation of 10, 11, 12, 13, 14 and 15 are undefined for the decade counter. The counter will return to a normal count-up sequence within two clock pulses after the entry of an undefined code. The details are discussed in PARALLEL ENTRY OF UNDEFINED CODES for the 8280. The 8280 and 8290 react identically to the entry of undefined output codes.

Resetting the 8290 and 8291

Total reset may be accomplished in 30ns for the 8290 and 8291. As discussed, the activation of $\overline{\text{RESET}}$ ("0") dominates both CLOCK and $\overline{\text{STROBE}}$ while completely discharging the clocking capacitors, preventing transients at the output and the toggling of any binary.

Asynchronous Data Release Times

The 8290 and 8291 will accept a clocking transition typically 20ns following the entry of parallel data or the activation of $\overline{\text{RESET}}$. These parameters are defined as data strobe release time and reset release time and are illustrated in Figure 2-16.

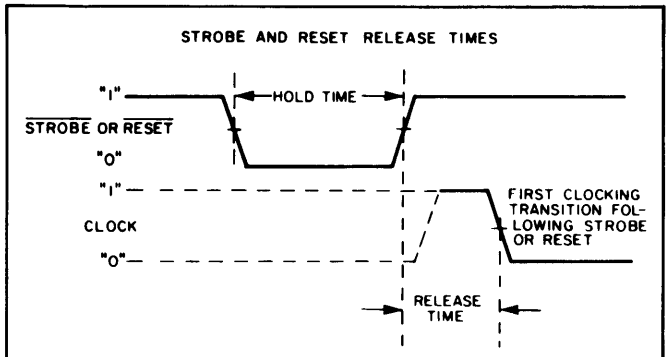


Figure 2-16. Strobe and Reset Release Times

Maximum Capacitive Loading

The outputs of the 8290 and 8291 are buffered (Figure 2-15a). Therefore, the only limitation to capacitive loading of these high-speed counters is the degradation of ripple propagation time and maintaining the required fall time of less than 75ns.

Description of Operation

Internally, the operation of the 8290 and 8291 is similar to the description of operation given for the 8280 and 8281. These high-speed counters were designed using a "75 MHz" binary for the A-bit, a "35 MHz" binary in the B position and "20 MHz" binaries for the C and D positions. Because an extremely high-speed binary is not required in the B-, C- and D-bit positions, overall power consumption is reduced using the lower power elements.

OPERATION OF THE LOW-POWER 8292 BCD DECADE RIPPLE COUNTER AND THE LOW-POWER 8293 4-BIT BINARY RIPPLE COUNTER

The 8292 is a 25mW variation of the 8290 BCD Decade Ripple Counter and is pin-for-pin interchangeable with both the 8290 and 8280. The 8293 is a low power variation of the 8291 4-Bit (16-State) Binary Ripple Counter and is pin-for-pin interchangeable with the 8281 as well as the 8291. Since a majority of counter requirements are at frequencies of less than 5 MHz, significant power saving can be realized by using the 8292 and 8293 for these requirements. Power consumption is typically 25mW at 5 MHz when operating from a 5.00V supply. Propagation delay from CLOCK to output is typically 35ns for each bit.

Decoupling

Although the 8292 and 8293 are low-power counters, they contain the same number of totem pole output structures as the 8280, 8281, 8290 and 8291. As a result, a minimum decoupling capacitance of 0.01 μF, non-inductive, is recommended. The capacitor should be mounted in accordance with the guidelines discussed in Section I.

Signal Processing/Input Clock Requirements

Minimum clock pulse amplitudes of 2.6V with pulse widths of 25ns are recommended for reliable toggling of the low power binaries. Fall times, independent of pulse width, should not exceed 75ns to achieve the energy transfer required to reliably activate the stored charge clock steering network. Output fall time tests are performed on other DCL devices to guarantee compatibility with this fall time requirement.

Negative Excursions at the Clock Input

A diffused diode clamp is incorporated at the CLOCK input of the 8292 and 8293 to ensure reliable operation in the presence of negative excursions at the clock line. Conservative design practices dictate, however, use of high-frequency layout techniques to minimize ringing within the system.

Entering Parallel Data

Presetting the 8292 and 8293 is performed by setting the desired output code at the respective data input terminals and activating $\overline{\text{STROBE}}$ ("0"). The data transfer is accomplished in parallel fashion with $\overline{\text{STROBE}}$ active for 30ns or more.

Parallel Entry of Undefined Codes

Should an undefined code, the binary equivalent of 10, 11, 12, 13, 14 or 15, be strobed into the 8292 10-state counter, the element will return to its normal count sequence within two clock pulses, and continue the up-count. The description of the count sequence following the entry of the undefined code is shown in Figures 2-10 and 2-11, for the logically equivalent 8280.

Resetting the 8292 and 8293

All bit positions may be forced to "0" by activating $\overline{\text{RESET}}$ with a "0" level. Both the 8292 and 8293 may be cleared to "0" by applying a reset signal of 35ns or more. The pulse width is measured at the 1.5V points of the falling and rising edge of the reset signal.

Maximum Capacitive Loading

The outputs of the 8292 and 8293 are buffered (Figure 2-15b). Therefore, the only limitation to capacitive loading of these high-speed counters is the degradation of ripple propagation time and maintaining the required fall time of less than 75ns.

Description of Operation

The 8292 and 8293 are logically identical to their respective high and medium speed counter parts. Internally, however, these counters are similar to the 8290 and 8291 with $\overline{\text{RESET}}$ dominating CLOCK and $\overline{\text{STROBE}}$ reducing reset holding time. $\overline{\text{STROBE}}$ also dominates CLOCK to ensure maximum parallel data entry rates.

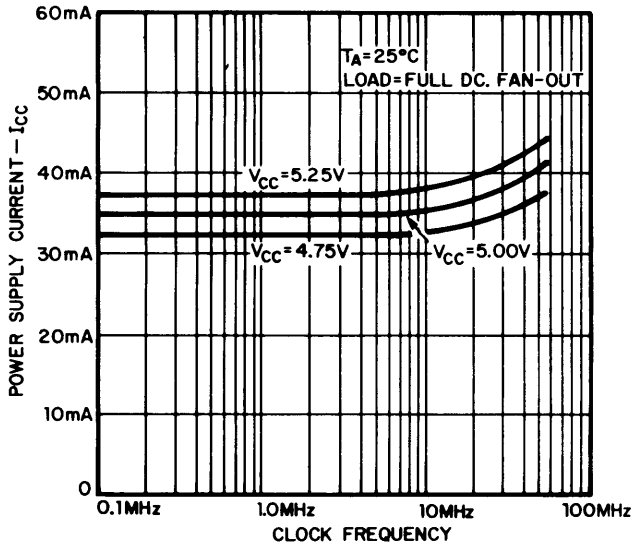
Asynchronous Data Release Times

The strobe release time and reset release time as defined in Figure 2-16 is 20ns. The 8292 and 8293 will accept the next activating clock pulse 20ns or more after an asynchronous pulse reaches the 1.5V level on its positive-going edge.

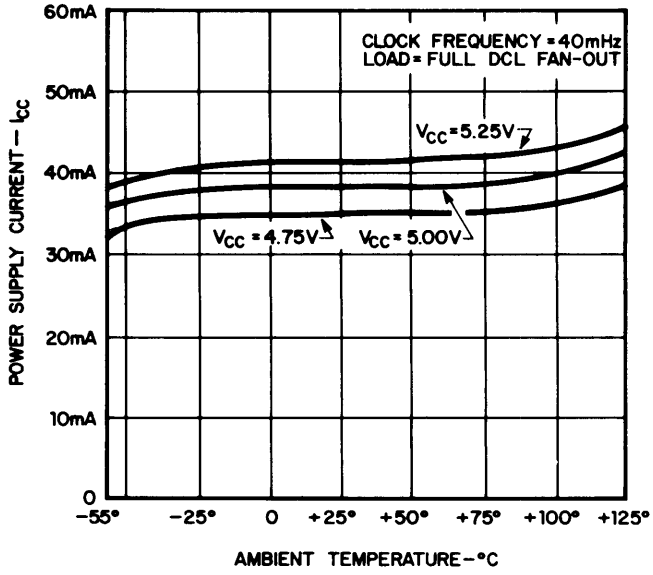
AC Characteristics of the 8290, 8291, 8292 and 8293

Shown in Curves 2-4 through 2-9 are the AC characteristics of the high-speed 8290 (8291) and low-power 8292 (8293) ripple counters. These curves show ONLY typical parameters and must not be construed as being guaranteed characteristics; however, assuming a possible deviation of up to ±25%; these curves demonstrate the rationale behind the guaranteed parameters. Each curve has two parts the (a) curve shows the 8290 and the (b) curve shows the 8292.

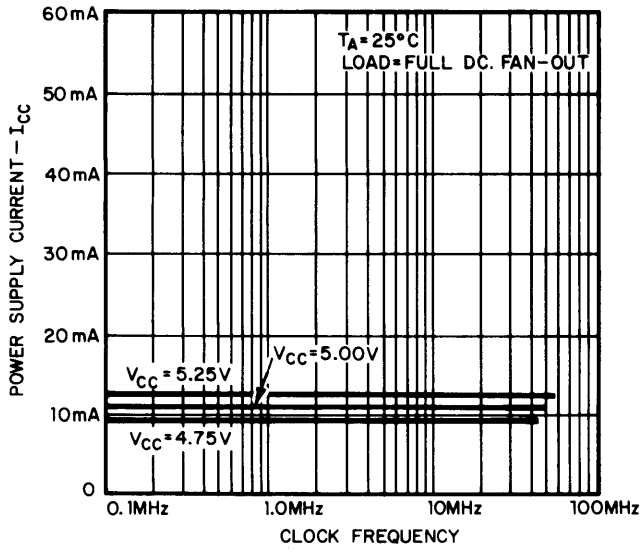
CURVE 2-4a. 8290



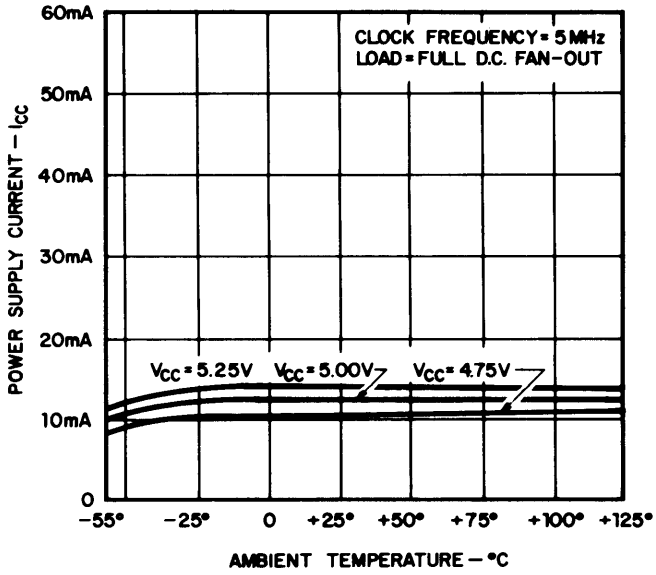
CURVE 2-5a. 8290



CURVE 2-4b. 8292



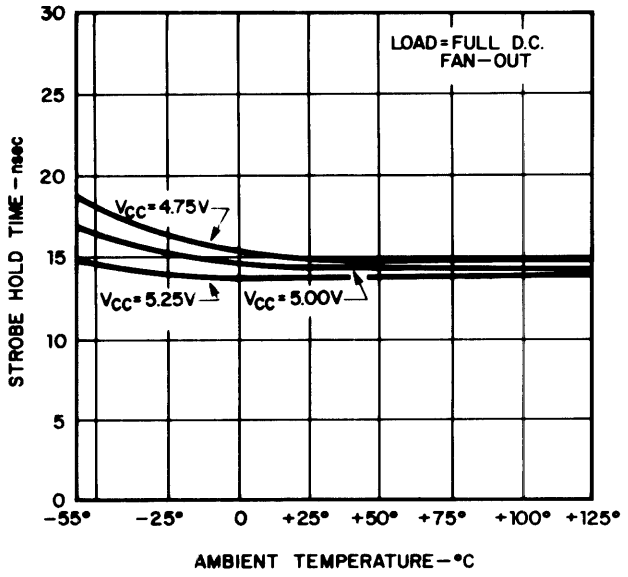
CURVE 2-5b. 8292



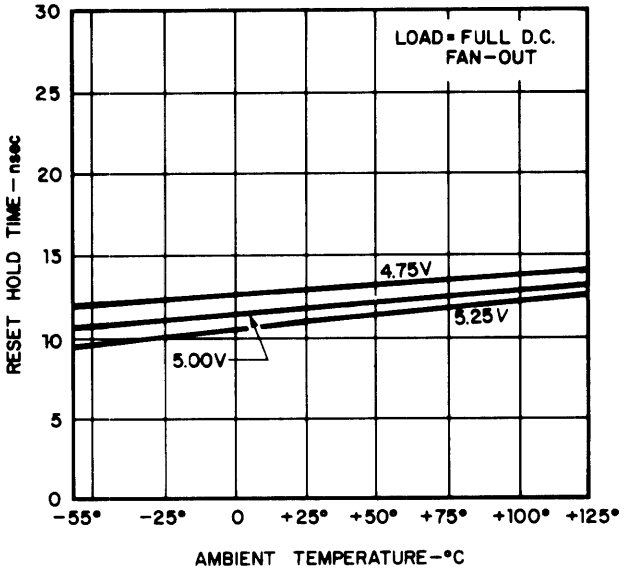
CURVE 2-4: The power supply current vs. clock frequency shown in these curves for three values of V_{CC} (V_{CC} = 5.00V ±5%). All testing was performed at an ambient temperature of 25°C (T_A = 25°C) and with all outputs fully loaded.

CURVE 2-5: These curves demonstrate the variation of power supply current vs. ambient temperature at the guaranteed operating frequency of these counters under full DC fan-out and at V_{CC} = 5.00V ±5%.

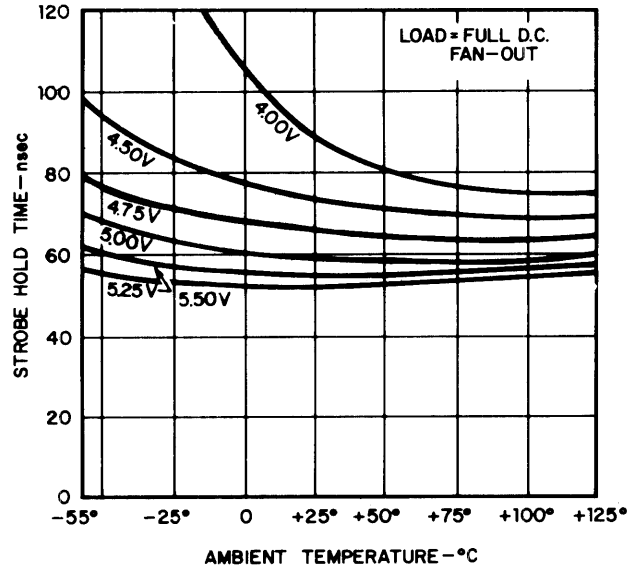
CURVE 2-6a. 8290



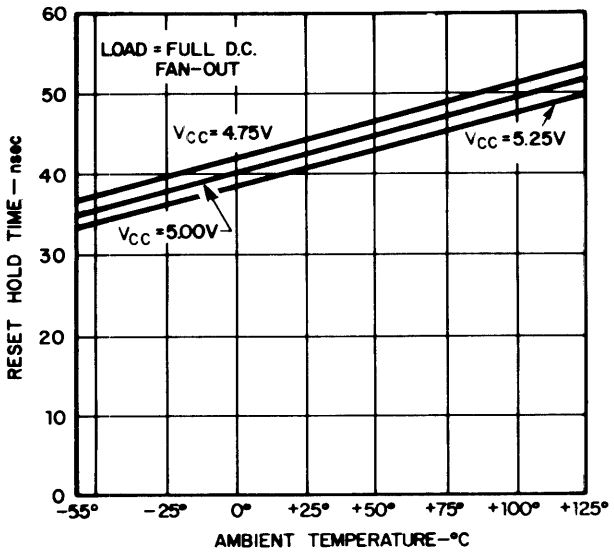
CURVE 2-7a. 8290



CURVE 2-6b. 8292



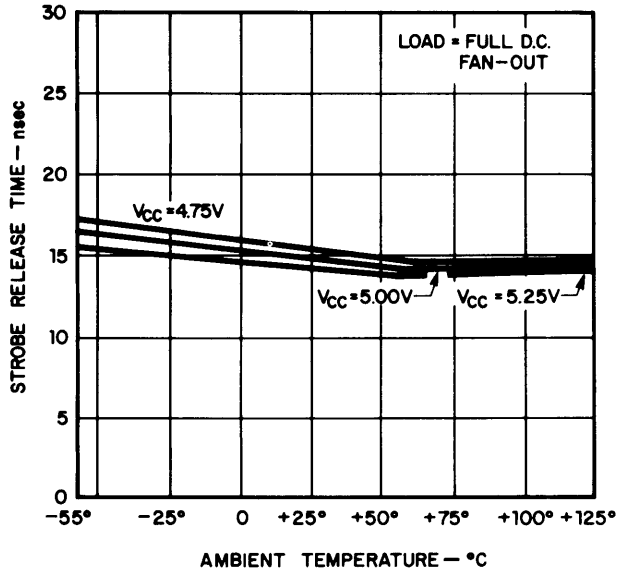
CURVE 2-7b. 8292



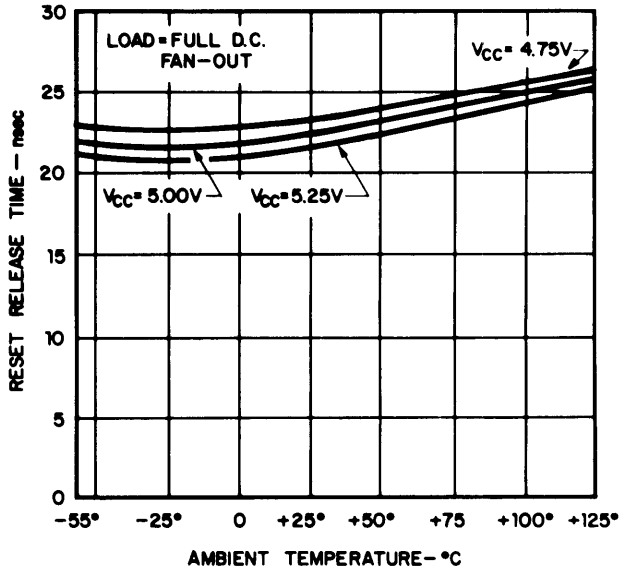
CURVE 2-6: The typical strobe hold time vs. ambient temperature shows the change with temperature of the minimum time the strobe input must be at a "0" level to guarantee that the information present at the parallel data inputs will be stored in each binary element. The strobe hold time was measured for V_{CC} = 5.00V ±5% with all outputs under full DC fan-out.

CURVE 2-7: The typical reset hold time vs. ambient temperature shows the change with temperature of the minimum time the reset input must be at a "0" level to guarantee that all outputs are "0". All tests were taken with full DC fan-outs and V_{CC} = 5.00V ±5%.

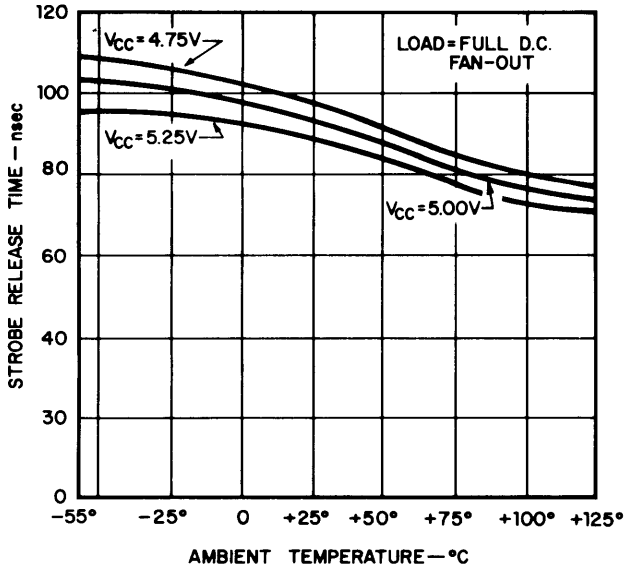
CURVE 2-8a. 8290



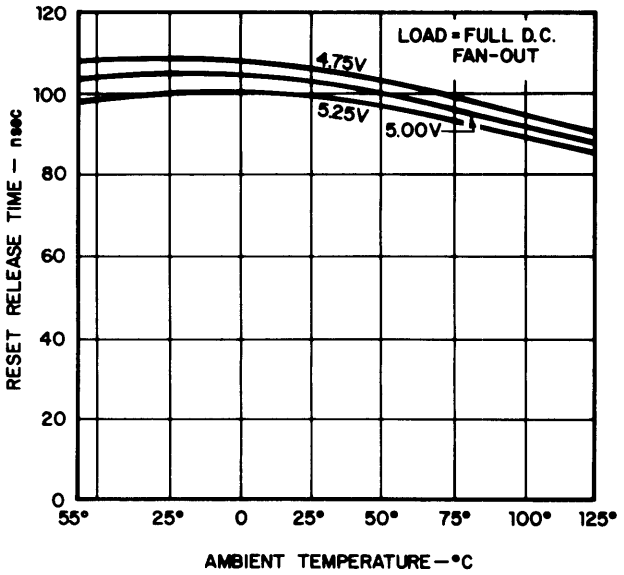
CURVE 2-9a. 8290



CURVE 2-8b. 8292



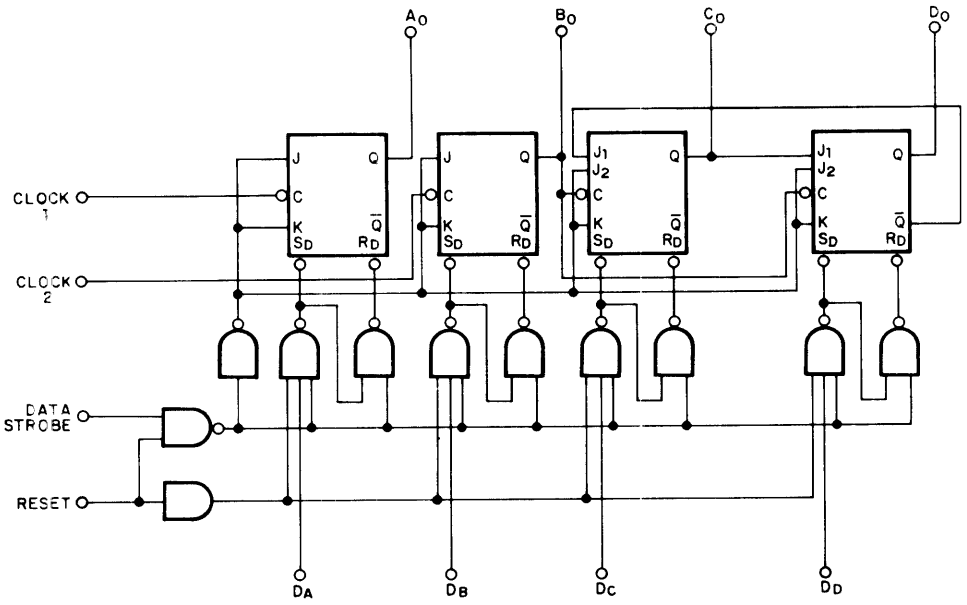
CURVE 2-9b. 8292



CURVE 2-8: The typical strobe release time vs. ambient temperature illustrates the variation with temperature of the minimum interval of time required before a clocking transition will be recognized by a counter after the strobe input has been disabled ("1").

CURVE 2-9: The typical reset release time vs. ambient temperature illustrates the variation with temperature of the minimum interval of time required before a clocking transition will be recognized by a counter after the reset has been disabled ("1").

These parameters are also characteristic of the 8291 and the 8293.



TRUTH TABLE

CLOCK	(1) A	(2) B	(4) C	(8) D	UNWEIGHTED B	C	D	A
0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0
2	0	1	0	0	0	1	0	0
3	1	1	0	0	1	1	0	0
4	0	0	1	0	0	0	1	0
5	1	0	1	0	1	0	1	0
6	0	1	1	0	0	0	0	1
7	1	1	1	0	1	0	0	1
8	0	0	0	1	0	1	0	1
9	1	0	0	1	1	1	0	1
10	0	1	0	1	0	0	1	1
11	1	1	0	1	1	0	1	1
12	0	0	0	0	0	0	0	0

Figure 2-17. The 8288 Logic Diagram

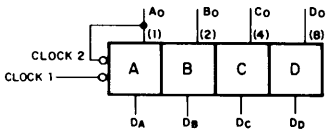
OPERATION OF THE 8288 12-STATE RIPPLE COUNTER

The 8288 is a modified ripple counter providing 12 distinct output states. The counter is intended primarily in applications requiring "real time" time base. The basic binary element is shown in Figure 2-15. As illustrated in Figure 2-17, the divide-by-twelve counter consists of a 2-state (divide-by-two) and a binary coded (4, 2, 1) 6-state (divide-by-six) counter. The 8288 will operate either as a 12-state binary weighted (8, 4, 2, 1) counter or as a 12-state non-weighted code counter with a square wave output. The truth table for both modes of operation are shown in Figure 2-17.

System Design Implementation

The 8288, like all asynchronous counters, traverses intermediate output codes during a single clocking cycle. Care should be taken when decoding to ensure that the counter has settled into the desired output state prior to decoding.

The technique described in Figure 2-5, for the 8280 and 8281, is an adequate solution. The intermediate states occurring during the normal 8-4-2-1 weighted count sequence are shown in Figure 2-18. Different intermediate states apply for the unweighted (square wave output) operating mode.



CLOCK PULSE	DESIRED DECIMAL OUTPUT	INTERMEDIATE DECIMAL EQUIVALENT	Binary Weighted Output Code A_O (1)	B_O (2)	C_O (4)	D_O (8)	NUMBER OF INTERMEDIATE STATES	APPROX DELAY TO DECODE DESIRED STATE
1	0		0	0	0	0	None	20ns
2	1		1	0	0	0		
		0	0	0	0	0	One	40ns
3	2		0	1	0	0	None	20ns
4	3		1	1	0	0		
		2	0	1	0	0	Two	60ns
		0	0	0	0	0		
5	4		0	0	1	0	None	20ns
6	5		1	0	1	0		
		4	0	0	1	0	One	40ns
7	6		0	1	1	0	None	20ns
8	7		1	1	1	0		
		6	0	1	1	0	Two	60ns
		4	0	0	1	0		
9	8		0	0	0	1	None	20ns
10	9		1	0	0	1		
		8	0	0	0	1	One	40ns
11	10		0	1	0	1	None	20ns
12	11		1	1	0	1		
		10	0	1	0	1	Two	60ns
		8	0	0	0	1		
13	0		0	0	0	0		

Figure 2-18. 8288 12-State Modified Ripple Counter Output Sequence (Binary Weighted Output Code)

Decoupling

The number of totem pole output structures within the 8288 requires the user to decouple the counter package from V_{CC} to GROUND with a 0.01μF ceramic disc capacitor or other non-inductive capacitor.

Signal Processing/Clock Input Requirements

The CLOCK 1 input of the 8288 will accept input frequencies in excess of 25 MHz. The clock pulse requirements are for 2.6V minimum amplitude with at least 25ns pulse width, measured at the 1.5V points. Independent of pulse width, the stored charge clocking mechanism requires fall times of less than 75ns from the minimum clock amplitude. Delay from the CLOCK input to the output of any binary is less than 25ns.

Negative Excursions at the Clock Input

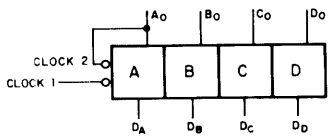
Like the other counters which incorporate the basic binary element shown in Figure 2-15, the 8288 will not miscount as a result of negative ringing at the CLOCK inputs. The CLOCK 1 and CLOCK 2 lines are clamped internally, with diffused diodes, to limit negative excursions to about -1.0V. This clamping action prevents the isolation diodes from turning on the clocking transistors.

Entering Parallel Data

The 8288 may be preset to any desired output state by presenting the desired 4-bit code at the data inputs and activating $\overline{\text{STROBE}}$ with a "0". The entry of the desired state will be accomplished when $\overline{\text{STROBE}}$ is active for 25ns or more.

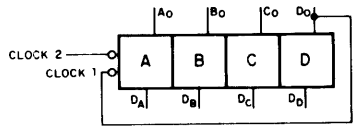
Parallel Entry of Undefined Codes

Output codes that are not in the normal count sequence of the 8288 may be entered by using the STROBE and data inputs. Should binary weighted 12, 13, 14 or 15 be entered into the 8288, the normal count-up sequence will be resumed within a maximum of four clocking transitions. The entry of undefined output codes is summarized in Figure 2-19 for the 12-state counter, operating in binary weighted output code. When any of the undefined codes is entered, the 8288 will continue to count up, in normal binary sequence, through 15, then return to 0. The reaction of 8288 to undefined parallel codes when operating in the unweighted square-wave output code configuration is shown in Figure 2-20.



UNDEFINED PRESET ENTERED	BINARY WEIGHTED OUTPUT CODE A_O (1)	B_O (2)	C_O (4)	D_O (8)	DECIMAL OUTPUT SEQUENCE	NUMBER OF CLOCK PULSES	LOGIC STATUS OF OUTPUT CODE
12	0	0	1	1	12	0	Undefined Preset
	1	0	1	1	13	1	Undefined Count
	0	1	1	1	14	2	Undefined Count
	1	1	1	1	15	3	Undefined Count
	0	0	0	0	0	4	Defined Count
13	1	0	1	1	13	0	Undefined Preset
	0	1	1	1	14	1	Undefined Count
	1	1	1	1	15	2	Undefined Count
	0	0	0	0	1	3	Defined Count
14	0	1	1	1	14	0	Undefined Preset
	1	1	1	1	15	1	Undefined Count
	0	0	0	0	0	2	Defined Count
15	1	1	1	1	15	0	Undefined Preset
	0	0	0	0	0	1	Defined Count

Figure 2-19. Parallel Entry of Undefined Codes for 8288 Operating as Binary 12-State Counter



UNDEFINED PRESET ENTERED	UNWEIGHTED OUTPUT CODE B_O	C_O	D_O	A_O	DECIMAL* OUTPUT SEQUENCE	NUMBER OF CLOCK PULSES	LOGIC STATUS OF OUTPUT CODE
"6"	0	1	1	0	(6)	0	Undefined Preset
	1	1	1	0	(7)	1	Undefined Count
	0	0	0	1	6	2	Defined Count
"7"	1	1	1	0	(7)	0	Undefined Preset
	0	0	0	1	6	1	Defined Count
"14"	0	1	1	1	(14)	0	Undefined Preset
	1	1	1	1	(15)	1	Undefined Count
	0	0	0	0	0	2	Defined Count
"15"	1	1	1	1	(15)	0	Undefined Preset
	0	0	0	0	0	1	Defined Count

Figure 2-20. Parallel Entry of Undefined Codes for the 8288 Operating with 12-State Unweighted Square Wave Output

Resetting the 8288

The basic binary element (Figure 2-15) of the 8288 prevents transient conditions at the Q output during reset mode. Reset of the counter is achieved by activating $\overline{\text{RESET}}$ with a "0" pulse displaying a pulse width (1.5V points) of 30ns.

Asynchronous Data Release Times

As defined in Figure 2-16, the strobe release time and reset time for the 8288 is 20ns. Either 12-state counter configuration will recognize the next clocking transition 20ns or more following the rise of a reset or strobe pulse to its 1.5V level.

Maximum Capacitive Loading

The 8288 has buffered outputs (Figure 2-15a). The only limitation to capacitive loading of these high-speed counters is the degradation of ripple propagation time and maintaining the required fall time of less than 75ns.

Description of Operation

When toggling normally with $\overline{\text{STROBE}}$ and $\overline{\text{RESET}}$ inactive ("1"), the 8288 is similar in operation to that of the 8280 and 8281. When $\overline{\text{STROBE}}$ or $\overline{\text{RESET}}$ are activated by "0", CLOCK is locked-out and the clocking capacitors are completely discharged, preventing the ripple of $\overline{\text{RESET}}$ or $\overline{\text{STROBE}}$ data from one bit to the next. Should the user activate $\overline{\text{RESET}}$ and $\overline{\text{STROBE}}$ simultaneously, reset will dominate and all outputs will go to "0".

OPERATION OF THE NON-PRESETTABLE 8282 BCD DECADE RIPPLE COUNTER* – NON-PRESETTABLE 8283 16-STATE BINARY RIPPLE COUNTER* – NON-PRESETTABLE 8289 12-STATE MODIFIED RIPPLE COUNTER*

The 8282 BCD Decade Ripple Counter is shown in Figure 2-21. Variations of the same basic die are used to produce the 8283 4-Bit Binary Ripple Counter (Figure 2-22) and the 8289 12-State Ripple Counter shown in Figure 2-23.

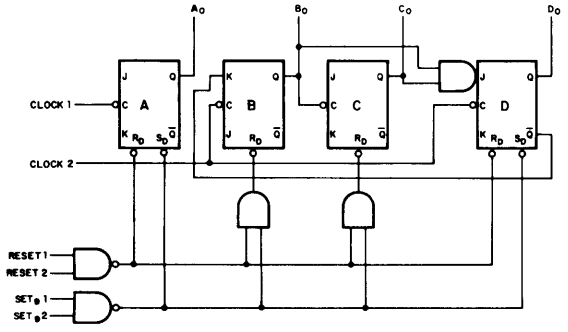


Figure 2-21. Logic Representation of 8282 BCD Decade Ripple Counter

*The 8282, 8283 and 8289 are functionally equivalent to the 7490, 7493 and 7492, respectively. However, the dual in-line package configuration is consistent with all 8200 MSI devices placing V_{CC} at Pin 14 and GROUND at Pin 7 to facilitate layout of the power and ground distribution system.

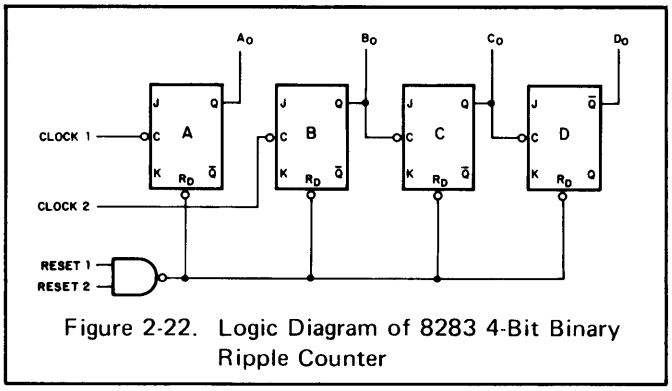


Figure 2-22. Logic Diagram of 8283 4-Bit Binary Ripple Counter

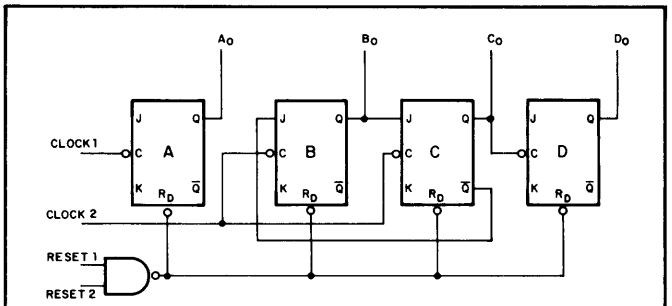


Figure 2-23. Logic Diagram of 8289 12-State Ripple Counter

Each of the counters contains four DC clocked master-slave J-K binaries which activate the negative-going edge of the clocking transition. The binaries are interconnected to provide the specified count sequence. Figure 2-24 is the schematic of the basic binary element along with the asynchronous gate entries. Although the gated RESET entry is available on all three counters, the gated SET, entry applies only to the 8282 decade counter. There are no provisions for presetting these counters to any binary number as discussed for previous counters under ENTERING PARALLEL DATA.

Intermediate codes traversed in the normal count sequence are the same for the 8282 as those described for the 8280 in Figure 2-4. The 8283 traverses the same intermediate codes as the 8281 (Figure 2-3).

Because the propagation delays from CLOCK to output for the non-presettable counters are about the same as for the 8280 and 8281, the "Delay Before Decoding Desired State" (Figures 2-3 and 2-4) is also the same.

The 8289 traverses the intermediate codes indicated in Figure 2-25, when operating as an unweighted 12-state counter with a square wave output. These are the same intermediate codes traversed by the 8288 when counting in the described mode.

Decoupling

Similar to the other ripple counters, there are four totem pole output structures contained in each of the three counters. Proper decoupling from V_{CC} to GROUND requires 0.01 μF of non-inductive capacitance. The ceramic disc capacitor recommended to achieve proper decoupling should be mounted in close proximity to the counter package.

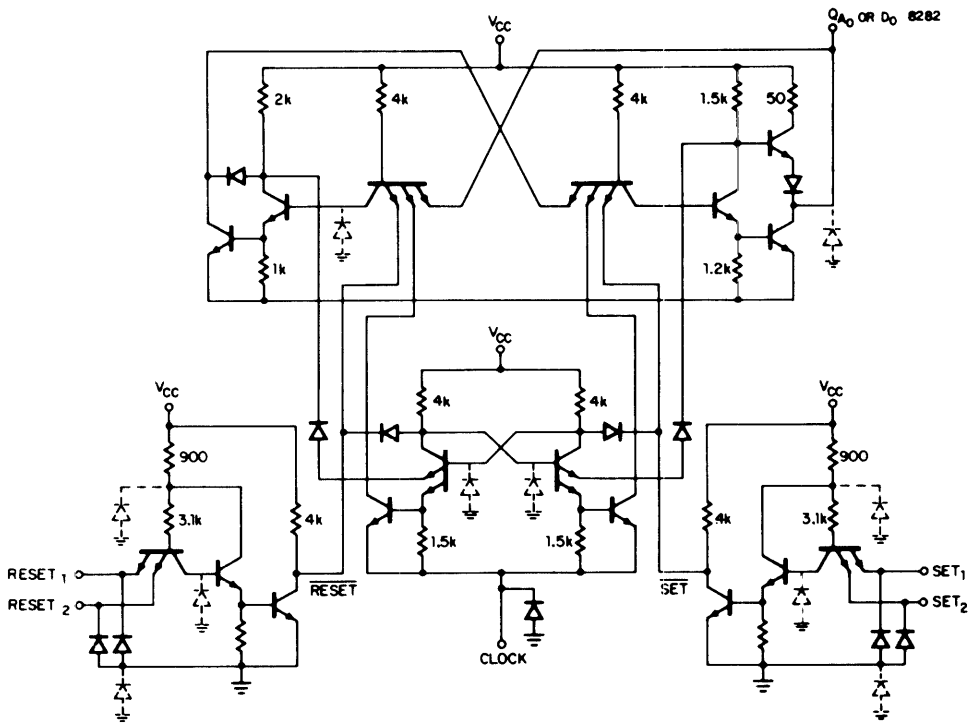
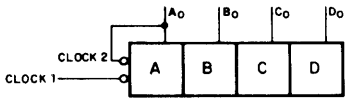


Figure 2-24. Basic Binary Element of the 8282, 8283 and 8289 Counters



CLOCK PULSE	DESIRED DECIMAL OUTPUT	INTERMEDIATE DECIMAL EQUIVALENT	WEIGHTED OUTPUT CODE				NUMBER OF INTERMEDIATE STATES	APPROX. DELAY TO DECODE DESIRED STATE
			A_0 (1)	B_0 (2)	C_0 (4)	D_0 (8)		
1	0		0	0	0	0	None	20ns
2	1		1	0	0	0		
		0	0	0	0	0	One	40ns
3	2		0	1	0	0	None	20ns
4	3		1	1	0	0		
		2	0	1	0	0	One	40ns
5	4		0	0	1	0	None	20ns
6	5		1	0	1	0		
		4	0	0	1	0	Two	60ns
		0	0	0	0	0		
7	6		0	0	0	1	None	20ns
8	7		1	0	0	1		
		6	0	0	0	1	One	40ns
9	8		0	1	0	1	None	20ns
10	9		1	1	0	1		
			0	1	0	1	One	40ns
11	10		0	0	1	1	None	20ns
12	11		1	0	1	1		
		10	0	0	1	1	Two	60ns
		6	0	0	0	1		
13	0		0	0	0	0		

Figure 2-25. Unweighted 12-State Ripple Counter Output Sequence

Leads on decoupling capacitors should be kept as short as possible. In most system layouts, it is most convenient to distribute the total required decoupling capacitance evenly around the printed circuit board.

Signal Processing/Clock Input Requirements

The 8282, 8283 and 8289 all incorporate DC clocked master-slave J-K binaries, theoretically removing any restriction on clock fall time. In practice, however, noise will be coupled onto all input and output lines within the system. For this reason, it is necessary to traverse the 200mV DC threshold uncertainty region in 15ns or less. To comply with this requirement there is a practical fall time restriction of 200ns, maximum, from the minimum clock pulse amplitude of 2.6V.

The guaranteed operating frequency of the CLOCK input is 10 MHz, requiring a minimum clock pulse width of 50ns. Typically, the 8282, 8283 and 8289 will operate reliably at frequencies above 25 MHz, with clock pulse widths of less than 20ns.

Negative Excursions at the Clock Input

Diffused diode clamps protect the CLOCK input when line reflections normally encountered in systems applications are present. The A-bit and B-bit can be made to malfunction with high energy negative excursions of -1.0V or more. Proper layout and termination techniques will ensure operational reliability. In particularly noisy environments, an external germanium diode may be used to clamp the CLOCK input at -0.3V.

Resetting the 8282, 8283 and 8289

Each of these counters provides a gated reset capability. All outputs will synchronously reset to "0" when RESET 1 and RESET 2 are simultaneously activated ("1") for 30ns. The activation of the reset function locks out the effect of further clocking transitions. Therefore, there is no need to gate out the CLOCK during asynchronous entry. The reset holding time for all three counters is 0ns, as illustrated in Figure 2-26.

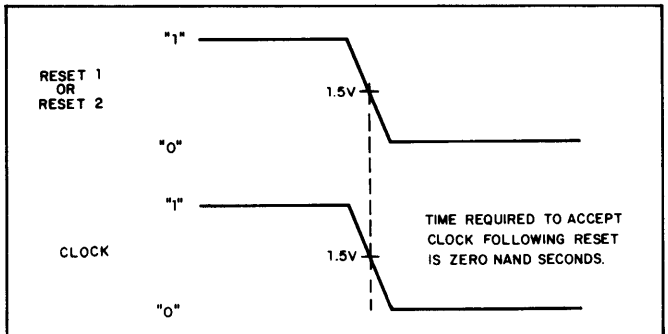


Figure 2-26. Reset Holding Time for 8282

Setting the 8282

A special provision is made on the 8282 decade counter so that it can be set to 9 (1 0 0 1) through the same type of asynchronous steering that is used for reset. When the SET_9 1 and SET_9 2 inputs are simultaneously active ("1"), the outputs of the 8282 will synchronously assume the states 1 0 0 1. A 30ns pulse width is sufficient to affect set to 9.

The internal set and reset points are ANDed into the direct reset connection of the B- and C-bit. Thus, when the external SET lines are activated, the A- and D-bits are set to "1" while the B- and C-bits are reset to "0". These internal connections are indicated in Figure 2-21.

Description of Operation/8282 Decade Ripple Counter

The 8282 Decade Ripple Counter consists of four master-slave J-K binaries and the internal interconnection and gating required to provide a 10-state BCD count sequence.

The A-bit is separate from the B-, C- and D-bit 5-state counter. When operating as a normal 10-state BCD counter, the CLOCK 1 line is driven by the data pulses to be counted, while CLOCK 2 is driven directly from the output of the A-bit. In normal counting or dividing modes, RESET 1 or RESET 2 and SET_9 1 or SET_9 2 are "0". The SET_9 and RESET inputs affect all four bits in the counter.

Like the 8280, the 8282 may be operated in the Bi-Quinary counting sequence. The output of the D-bit is connected to CLOCK 1 and the input frequency drives CLOCK 2. The resulting 5-state counter followed by a 2-state counter, produces a square wave output, occurring at one-tenth the CLOCK 2 frequency. Bi-Quinary configurations are particularly applicable to frequency synthesizer equipment. The 10-state coded output sequence is not a standard binary weighted code. The clocked mode turn-on and turn-off time is typically 20ns per binary. With the three levels of binary delay encountered in the 8282, 60ns delay should be allowed from the falling edge of the clock before decoding the outputs. The 8282 may be set to 9 (1 0 0 1), or reset to 0 (0 0 0 0) when "1" is applied to both inputs of the appropriate asynchronous entry gate shown in Figure 2-24. If both SET and RESET are applied simultaneously, the SET input will dominate as long as both remain active and the outputs will be set to 1 0 0 1. Should both asynchronous commands be removed simultaneously, the final output state will be arbitrary. A DC race condition exists internally under these circumstances. The multiple emitter transistor in the master latch (Figure 2-24) which turns on first, will determine the final output state of the counter.

8283 16-State 4-Bit Binary Ripple Counter

The 8283 consists of four DC clocked master-slave J-K binaries. The binaries in bit positions B, C and D are interconnected in classic ripple fashion to produce a 3-bit (8-

state) ripple counter. The A-bit is separated from the 8-state counter and may be used for a binary independently from the B-, C- and D-bits assuming the reset function of the A-bit coincides with the reset of the octal ripple counter.

When operating as a 4-bit binary ripple counter, the output of the A-bit is connected to CLOCK 2 and RESET 1 or RESET 2 is "0". In this configuration, the input pulses are applied to CLOCK 1. Divide-by-two, -four, -eight and -sixteen counters are available for decoding in this configuration, when the A, AB, ABC or ABCD outputs, respectively, are decoded.

Resetting all outputs to "0" is accomplished through the gated RESET input by simultaneously applying "1" to RESET 1 and RESET 2. In the event only one reset signal is required, RESET 1 and RESET 2 should be shorted together and driven from the same low impedance source. Disposing of the unused RESET input in this manner enhances speed with which reset is accomplished and provides optimum AC noise immunity at the unused input.

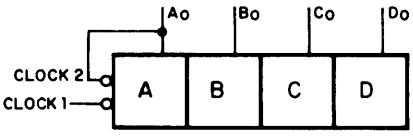
Typical propagation delay from the CLOCK input of each binary to the output of that binary is 20ns. Four levels of binary delay are encountered from CLOCK 1 input to D output. 80ns of delay should be allowed following the activation ("1" to "0" transition) of the CLOCK 1 input before the 4-bit output is decoded. The 80ns delay will ensure that an intermediate code (Figure 2-3) is not detected.

8289 12-State Unweighted Ripple Counter

The 8289 consists of four DC coupled, master-slave, J-K binaries with common reset function. The counter is organized with a 2-state counter, the A-bit separated from the B-, C- and D-bits. The B- and C-bits are interconnected in a 3-state counter which drives an additional 2-state counter, the D-bit. The 6-state counter (bits B, C and D) are not binary weighted as in the 8288. Additional decoding for numeric readout is required with the 8289. The 6-state counter consisting of the A-, B- and C-bits does provide a binary weighted output code.

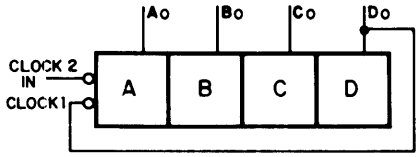
No other off-the-shelf MSI device is capable of the variety of direct counting and frequency dividing functions. A 2-state (divide-by-two), two separate 6-state (divide-by-six) and two separate 12-state (divide-by-twelve) configurations are available by choice of interconnection and/or decoding. The 12-state sequences are reviewed in Figure 2-27.

Reset of all output to "0" is accomplished by simultaneously applying "1" to RESET 1 and RESET 2 inputs. The outputs will change to "0" asynchronously. An unused gated RESET input may be tied to V_{CC} or tied to the driven RESET input. The latter disposition of the unused input is recommended. "1" level fan-out from the source of the reset signal will be doubled but the "0" level fan-out is not affected.



TRUTH TABLE

CLOCK	B_o	C_o	D_o	A_o
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	0	0	0	1
8	1	0	0	1
9	0	1	0	1
10	0	0	1	1
11	1	0	1	1
12	0	1	1	1
13	0	0	0	0



TRUTH TABLE

CLOCK	A_o	B_o	C_o	D_o
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	0	0	1
8	1	0	0	1
9	0	1	0	1
10	1	1	0	1
11	0	0	1	1
12	1	0	1	1
13	0	0	0	0

Figure 2-27. 12-State Truth Tables for 8289

Maximum Capacitive Loading

In the interest of power consumption, the outputs of the 8282, 8283 and 8289 have been left unbuffered. To ensure reliable latching of the slave binary of the individual bits, the capacitance load on any output should not exceed 100pF. Since the outputs are unbuffered, they should be physically isolated from high energy "1" to "0" voltage transients within the system. Improper isolation may cause any individual bit to latch in the wrong state.

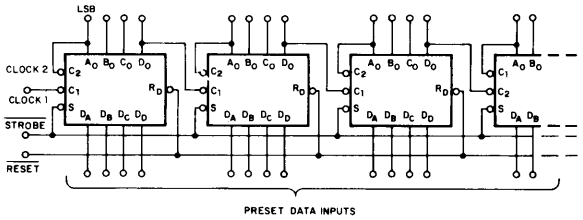


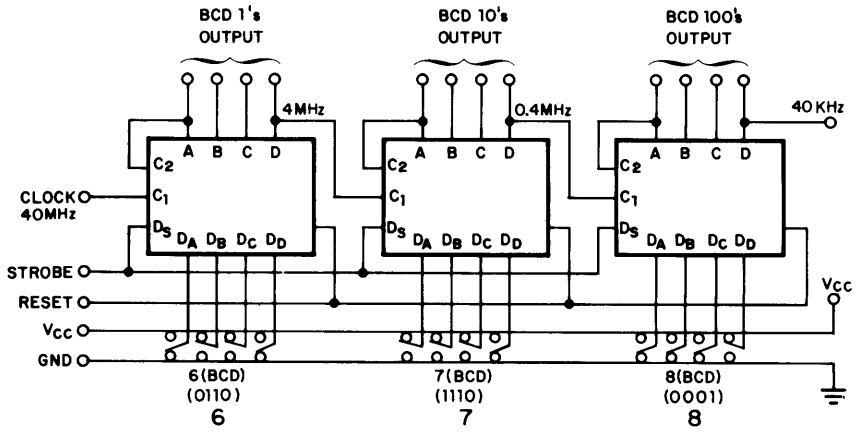
Figure 2-28. Cascading Presettable Asynchronous Counter

Ripple Counter Applications

Cascading Counters. Figure 2-28 illustrates how several 8280, 8281, 8288, 8290, 8291, 8292 and/or 8293 counters (Class I) may be cascaded in a ripple fashion to count or total any number of counts or events in any one or a combination of BCD decade, divide-by-twelve and/or 4-bit binary (hexadecimal) counting sequences.

The total number of counts before overflow occurs can be reduced by presetting the counter to some initial count. Class I counters are preset to the information present at the DATA inputs when a "0" is applied to the DATA STROBE (or STROBE) input. If a clocking signal is not present at the CLOCK 1 input after the STROBE ("0") is released (goes to a "1"), the preset information is stored. However, if a clocking signal ("1" to "0" transitions in less than 75ns) is then applied, the counter will eventually overflow to zero at a count equal to the total capacity of the counter minus the preset count.

An example of this function is illustrated in Figure 2-29. An 8290 40 MHz BCD Decade Counter and two 8292 5 MHz BCD Decade Counters are cascades producing a 40 MHz divide-by-1000 ripple counter. Notice that the high-speed 8290 was not required in the second and third decade positions due to the frequency division of ten in the first decade (8290). If the high-speed counters are unnecessary, significant power saving can be attained at frequencies below 5 MHz by using the low-power 8292 and 8293.



DEVICE TYPE	NUMBER OF OUTPUT STATES	GUARANTEED CLOCK INPUT FREQUENCY	POWER CONSUMPTION PER COUNTER	REQUIRED STROBE HOLD TIME	REQUIRED STROBE RELEASE TIME	REQUIRED RESET HOLD TIME	REQUIRED RESET RELEASE TIME
8280	10	20 MHz	125mW	250ns	0ns	1μs/counter	0ns
8281	16	20 MHz	125mW	250ns	0ns	750ns/counter	0ns
8288	12	25 MHz	125mW	25ns	20ns	30ns	20ns
8290	10	40 MHz	150mW	25ns	20ns	30ns	20ns
8291	16	40 MHz	150mW	25ns	20ns	30ns	20ns
8292	10	5 MHz	25mW	30ns	20ns	35ns	20ns
8293	16	5 MHz	25mW	30ns	20ns	35ns	20ns

Figure 2-29. Presetting Class I Counters

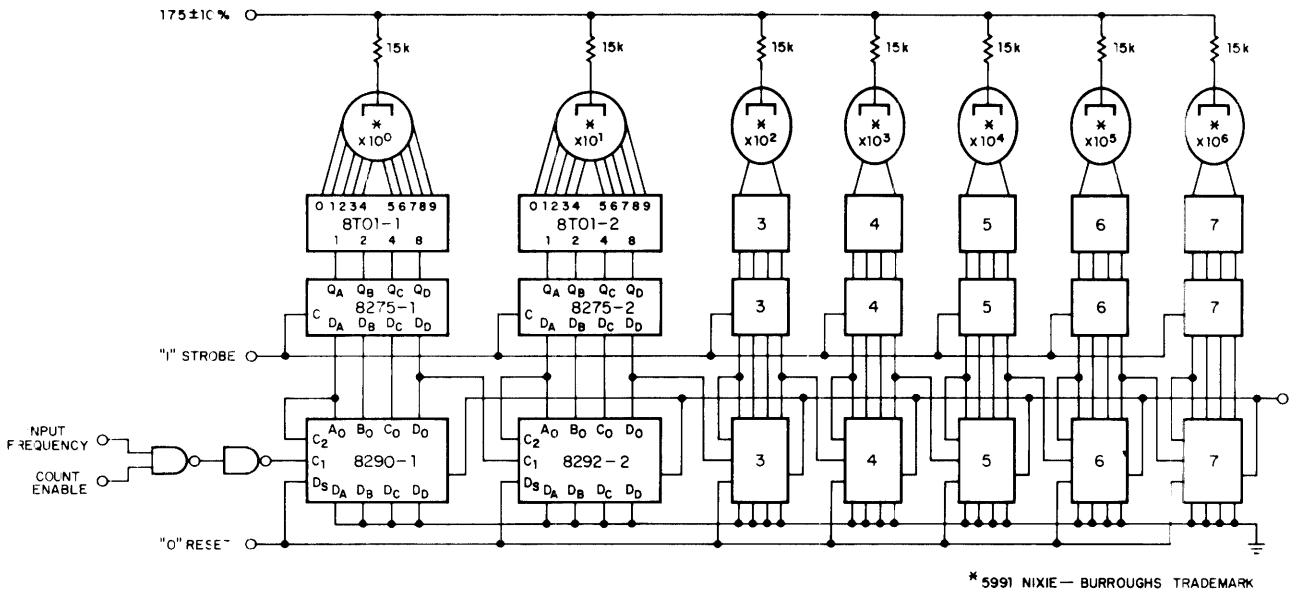
In the example (Figure 2-29), a preset count of 876 is strobed into the counter ($\overline{\text{STROBE}}$ = "0"). When the $\overline{\text{STROBE}}$ is released ("1"), the counter can count 876 events (clock transitions) before overflowing to zero.

Frequency Measurement

To measure frequency, the input frequency must be gated by a time standard. The total count after the timing interval is then strobed into storage/buffer register which could be any of the Class I counters or an 8275 Quad Latch. The counter can be reset and allowed to count again while the stored preceding count is being displayed, as shown in Figure 2-30. With the 8290 as the least significant decade, the maximum input frequency is guaranteed to be 40 MHz.

Any of the BCD decade counters may be used. Since the preset capability is not utilized in this application, the 8282 (a Class II BCD Decade Counter) can be interchanged with the Class I counters. To reset the 8282, both RESET inputs must go high ("1") and the SET inputs grounded ("0").

In all applications not requiring the presetting of an initial condition, the 8282 BCD Decade, 8283 Hexadecimal (4-bit binary) and/or 8289 Divide-by-Twelve (Class II) counters can replace the 8280, 8288, 8292 and/or 8293 (Class I) counters if the maximum frequency of 20 MHz for the Class II counters is not to be exceeded. However, to reset the Class II, a "1" level must be applied to both RESET inputs.



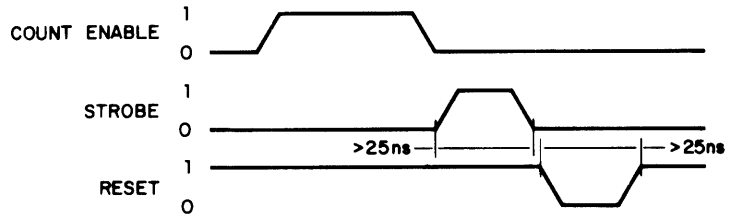
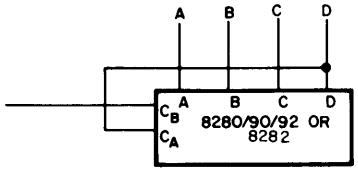


Figure 2-30. Frequency Counter

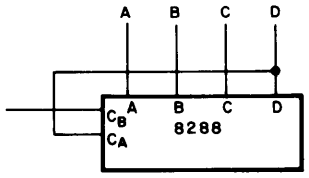
A Bi-Quinary counter for the 8280/8290/8292 or 8282 and a square wave divide-by-twelve counter for the 8288 are produced by connecting the D_O output to the A-bit CLOCK input and driving the B-bit CLOCK input with the input frequency. Figure 2-31 illustrates these connections. The 8289 already has a square wave output with the standard connection of the A_O output attached to the CLOCK input of the B-bit and the A-bit CLOCK input being driven. (See truth table in Figure 2-27.)



TRUTH TABLE

CLOCK	B	C	D	A	
0	0	0	0	0	÷ 5
1	1	0	0	0	
2	0	1	0	0	
3	1	1	0	0	
4	0	0	1	0	
5	0	0	0	1	÷ 5
6	1	0	0	1	
7	0	1	0	1	
8	1	1	0	1	
9	0	0	1	1	
10	0	0	0	0	

Figure 2-31a. Bi-Quinary Counter



TRUTH TABLE

CLOCK	B	C	D	A	
0	0	0	0	0	÷ 6
1	1	0	0	0	
2	0	1	0	0	
3	1	1	0	0	
4	0	0	1	0	
5	1	0	1	0	
6	0	0	0	1	÷ 6
7	1	0	0	1	
8	0	1	0	1	
9	1	1	0	1	
10	0	0	1	1	
11	1	0	1	1	
12	0	0	0	0	

BCD
÷ 6

Figure 2-31b. Square Wave Divide-By-Twelve Counter Using the 8288

Divide-By-N Configurations. A Variable Modulus Counter is one which can be made to count by or divide by any desired number. The VMC finds extensive use in precise frequency division applications such as digital clocks, sequential control operations and frequency synthesizers. The basic VMC circuit is shown in Figure 2-32. For the example illustrated a BCD decade counter (8280 or 8292) is cascaded with a hexadecimal (4-bit binary) counter (8281 or 8293) to produce a VMC of any modulus between 1 and 160 (10 x 16 counts). Larger moduli can be achieved by merely increasing the number of counting elements and the number of inputs on the expandable gates, W and X.

The VMC operation is attained by presetting an initial condition (N_C),

$$N_C = N_{MAX} - n$$

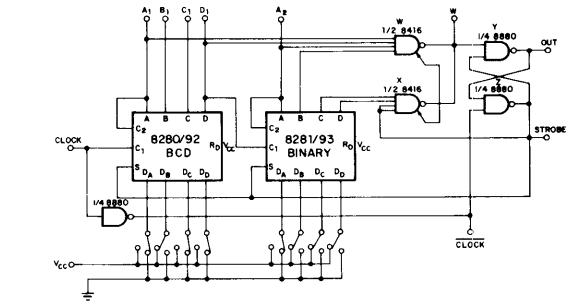
where: N_C is the preset or complement number.

$$N_C = 159 - 17 = 142$$

N_{MAX} is the maximum count the counter can attain before overflow.

n is the modulus or the frequency dividend number,

when the maximum count is detected. If the minimum



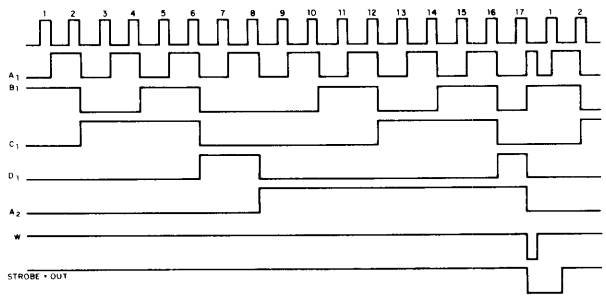


Figure 2-32. Variable Modulus Counter

count or zero were to be detected instead, the presetting of a modulus could not occur until the counter had completely rippled to zero (nearly 25ns per binary level). By detecting the maximum count, the counter will be preset when the least significant bit (LSB) goes high for the maximum count.

For example, in Figure 2-32, if a modulus of 17 is desired, the 159th count is detected when point W goes low ("0"). As seen in the timing diagram, point W falls after 17th clocking transition (falling edge). A "0" at W sets the Y/Z latch, and the $\overline{\text{STROBE}}$ line stays low for as long as CLOCK is low ($\overline{\text{CLOCK}}$ = "1") which presets the number $N_C = N_{MAX} - n$. The output frequency at gate Y (OUT), which is high while $\overline{\text{STROBE}}$ is low, is equal to the clock frequency divided by 17. Therefore, the output OUT period is equal to 17 x (CLOCK period):

$$f_{out} = f_{in/n} \text{ or } \tau_{out} = n \cdot \tau_{in}$$

The maximum frequency of operation for this configuration (Figure 2-32) is at least 4 MHz when 8280s and 8281s are used and greater than 5 MHz if the 8280/8281s are replaced with 8292/8293s. If 8290/8291s are used in Figure 2-32, the maximum VMC frequency will be in excess of 8 MHz.

25 MHz Variable Modulus Counter. Figure 2-33 illustrates a method of producing a guaranteed 25 MHz VMC. Gate 1 is used only as an inverter which clocks ("1" to "0" transition) the first decade on the rising edge ("0" to "1" transition) of the input CLOCK. The input CLOCK is NANDed with the D_O output and the output of Gate 5, which is "1" when all following decades are at their maximum count (or all inputs to Gate 6 are "1"). When D_O, Gate 5 and the input CLOCK are all "1"s, Gate 2's output goes to "0". The propagation delay from the eighth input CLOCK ("0" to "1" transition) to the D_O output going to a "1" is approximately 20ns. Therefore, if the CLOCK input pulse width is too long, the $\overline{D}_{S_1}$ line (output of Gate 2) will go to "0" on the eighth clock long enough to strobe the parallel data into the 8290. If the pulse is too short, $\overline{D}_{S_1}$ will not be "0" for a sufficient time to guarantee parallel entry even on the ninth clock. The curves in Figure 2-34 show the typical minimum and maximum pulse widths necessary to strobe this 25 MHz VMC for the following test conditions: outputs loaded only as shown in Figure 2-33; V_{CC} = 4.75V, 5.00V and 5.25V; ambient temperature (T_A) was varied from -55°C to +125°C; and the clock frequency was 25 MHz. The dashed line at 25ns illustrates the typical median pulse width with a tolerance of ±6ns (24%) at V_{CC} = 5.00V or ±5ns (25%) at V_{CC} = 4.75V over the full temperature range. From this data (Figure 2-34) one can easily ascertain that a clock pulse width of 25ns ±10% will guarantee proper operation. With V_{CC} = 5.25V and adjusting the clock pulse width as frequency was increased, a maximum frequency of 37 MHz was obtained with a clock pulse width of 16ns. However, this maximum frequency operation cannot be guaranteed due to normal process variations.

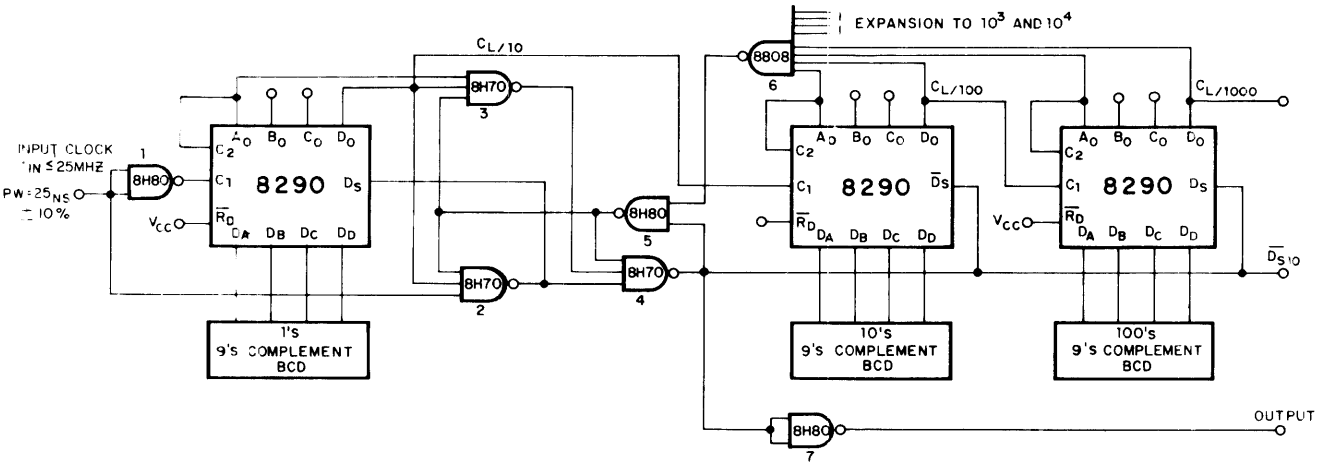


Figure 2-33. 25 MHz Variable Modulus Counter – Three Decades with Expansion

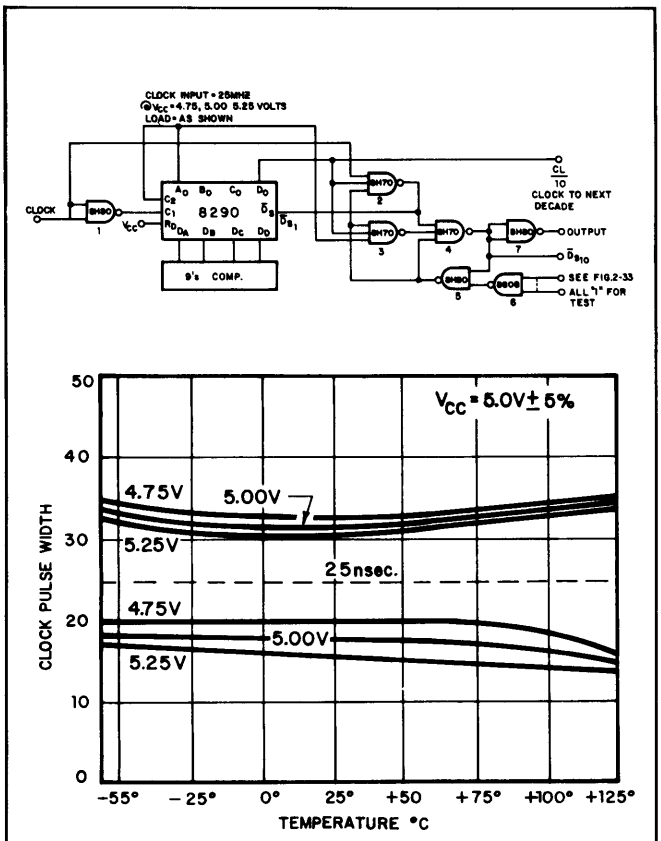


Figure 2-34. Minimum and Maximum Clock Pulse Width of a 25 MHz Anticipated Nine Variable Modulus Counter using the 8290

When all decades following the first decade are all 9 (maximum count), all inputs to Gate 6 are "1". The output of Gate 6 goes to "0", which sets the latch made up of Gates 4 and 5, since the outputs of Gates 2 and 3 are "1". The output of Gate 4 is the $\overline{\text{STROBE}}$ ($\bar{D}_{S_1}$) for all decades except the first. Gate 5 goes to a "1" enabling Gates 2 and 3. Nine clock pulses later, the output of Gate 2 goes to "0" strobing the 8290 and resetting the latch (Gates 4 and 5).

It is possible to produce a pulse at the count of 8 at the output of Gate 2 which will not strobe the 8290 but will reset the latch (Gates 4 and 5). This mode of operation will only cause problems for moduli less than 10 ($n \leqslant 10$), where upon a short pulse at 8 and a long pulse (25ns) at the count of 9 will appear at the output. Therefore, clock pulse of less than 25ns is recommended. Gate 3 is only used to inhibit the output when modulus of zero (n = 0) is applied. The output is taken from Gate 7. For moduli of 10 or greater ($N \geqslant 10$), the output will be high ("1") for 9 counts. For moduli less than 10 ($n \leqslant 10$), the output will be high for n−1 counts. For example, if n = 7, the output would be high for 6 counts and go low ("0") on the seventh count for the duration of the clock pulse. If a modulus of zero (n = 0) is applied, the output of Gate 5, A_0 and D_0 are all held at a "1" level, and the output of Gate 3 will go to "0". When Gate 3 is "0" the output (Gate 7) is "0" through Gate 4. If zero inhibit were not utilized, the moduli of zero and one (n = 0 and 1) would produce the same output since A_0 is not used to generate $\bar{D}_{S_1}$.

Again, the maximum count of a BCD decade counter is 9. Therefore, the 9's complement is the BCD equivalent of the number which is preset into a decade VMC to achieve a specified modulus. For example, a modulus of 27 in a two decade VMC requires a preset BCD number of 72: N_C = 99 - 27 = 72 (BCD).

Binary Variable Modulus Counter. The presettable binary counters (Class I – 8281, 8291, and 8293) when used in a VMC configuration must be preset with 1's complement information. That is, if a modulus of 11 is desired, the inverted binary equivalent or 1's complement number will preset the VMC for the proper modulus: the binary equivalent of 11 is 1 1 0 1 (LSB first); inverting 1 1 0 1 gives 0 0 1 0; if 0 0 1 0 is strobed into the VMC, eleven more counts will produce the maximum count of 1 1 1 1 (15), and 0 0 1 0 will be again preset into the VMC. See Figure 2-35.

Figure 2-35 shows a simple three phase generator which is self-correcting. The generator may be used with the VMC or any other clock source.

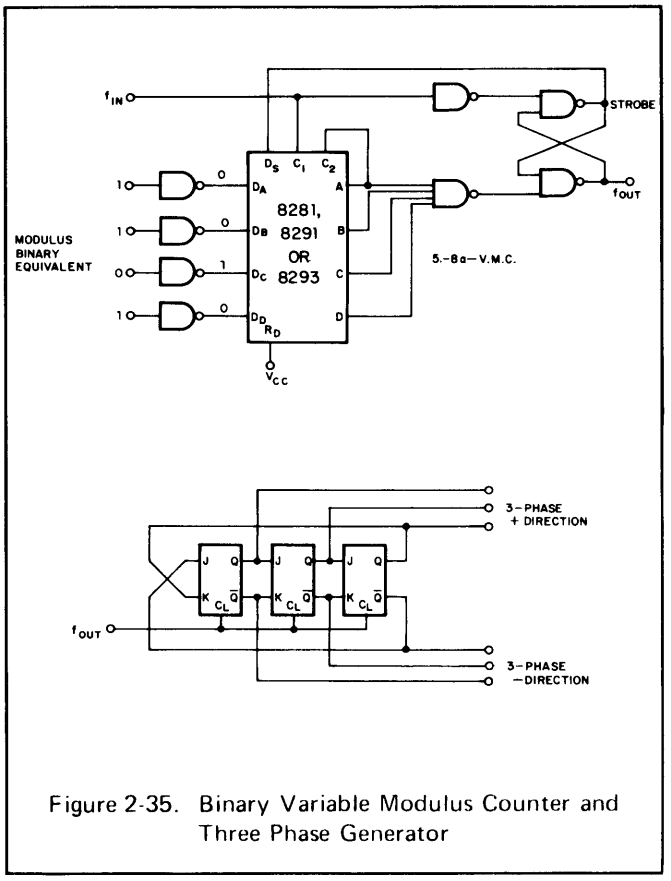


Figure 2-35. Binary Variable Modulus Counter and Three Phase Generator

Class II Modulus Counter. The 8282, 8283 and 8289 (Class II counters) do not have the preset capabilities of the Class I counters; therefore, other methods must be used to derive divide-by-N configurations. Figure 2-36 illustrates a series of wired modulus frequency dividers using Class II counters. Any modulus may be produced using the general methods shown in this figure. The moduli two, three, four, five, six, eight, ten, twelve and sixteen are directly available in one of the three Class II counters; however, these moduli may also be created, if desired. The moduli (2 through 15) will divide an input frequency of 20 MHz. Larger moduli are possible by extension of the methods shown in Figure 2-36.

A Synchronous Ripple Up Counter. The configuration shown in Figure 2-37 reduces the total ripple time to that of one MSI ripple counter while the entire count is operating at the maximum frequency of the first stage. The method used is similar to that used in the 8284 and 8285. The second, third, . . ., etc., stages anticipate the "Carry-Out" by the number of counts in the first stage (10, 12 or 16), This anticipated carry ripples from the second to the last stage with approximately 15ns per stage if 8H00 gates are used.

Digital Clock Design. The design of a digital clock is illus-

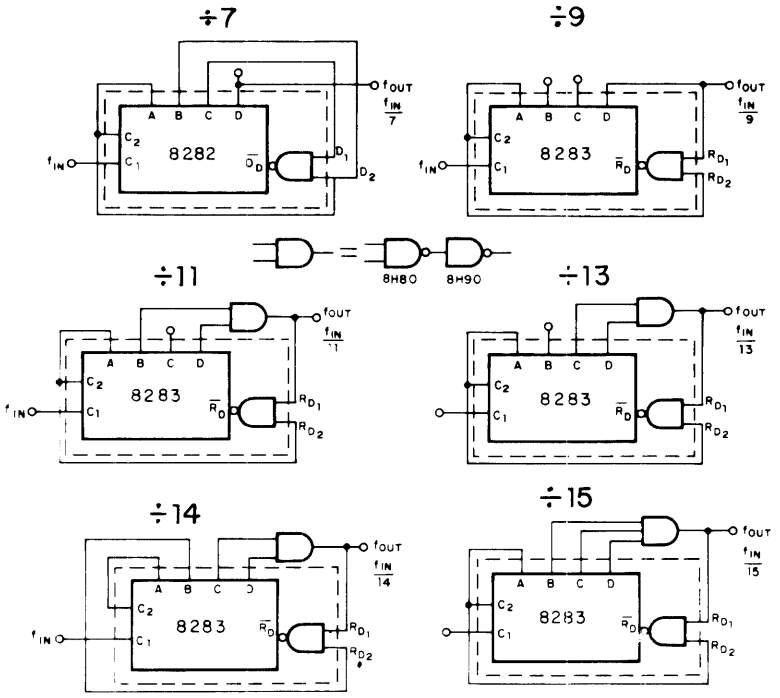


Figure 2-36. Wired Modulus Counters Moduli: 7, 9, 11, 13, 14 and 15

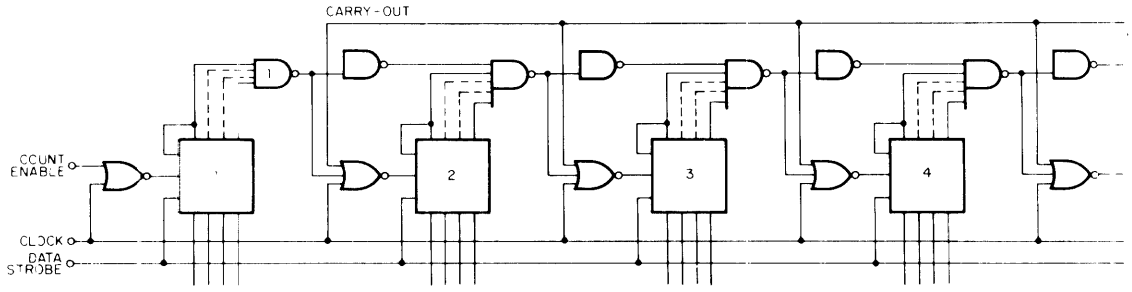


Figure 2-37. A Synchronous Ripple Up-Counter

trated in Figure 2-38. The advantages of having a BCD divide-by-six and a divide-by-two in the 8288 are utilized in this example. The second (8288-2) and third (8288-3) are used to detect AM/PM and tens of hours, respectively. Low power devices are used when possible. When the thirteenth hour is detected (13:00:00) the clock is preset to 1:00:00. Each time 12:00:00 is reached, the AM/PM flip-flop (A-bit of 8288-2) toggles from AM to PM or from PM to AM. The clock may be RESET to 00:00:00 and the TIME switch used as a START/STOP button for elapsed time applications. A 1 KHz oscillator is provided for setting the correct time into the digital clock.

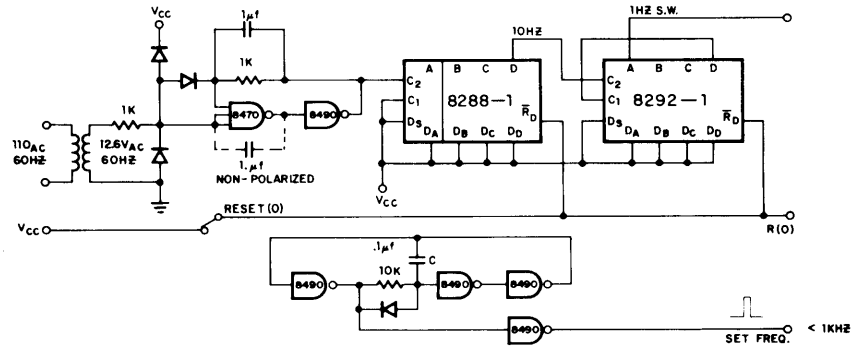


Figure 2-38a. A Digital Clock Design

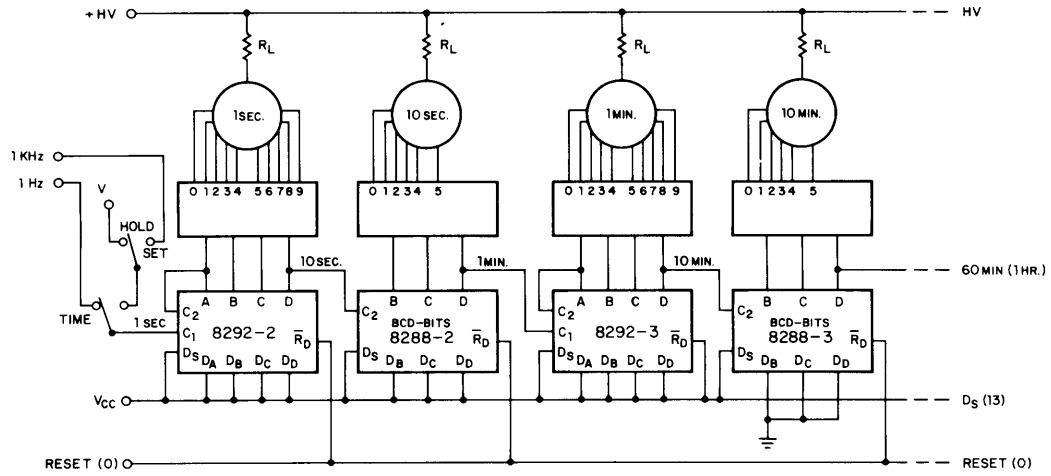


Figure 2-38b. A Digital Clock Design

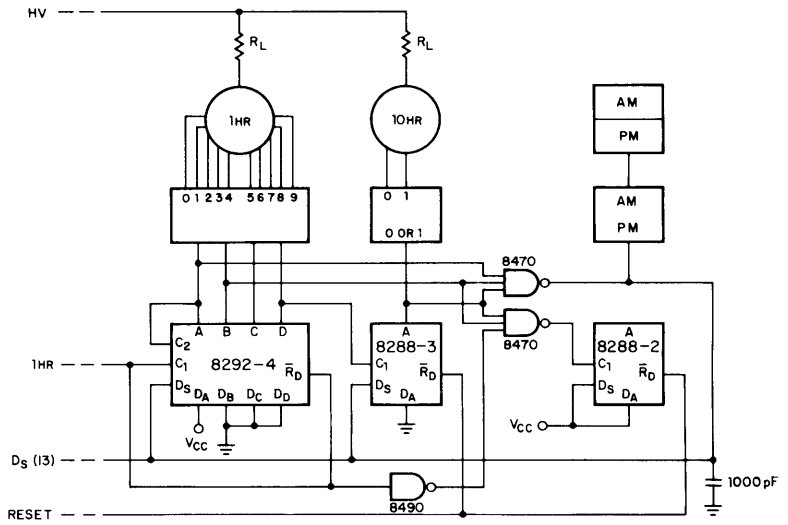


Figure 2-38c. A Digital Clock Design

SECTION III

MSI SYNCHRONOUS COUNTERS

The 8284 Hexadecimal (4-Bit Binary) Synchronous Up/Down Counter has sixteen unique 4-bit output codes which occur synchronously. The 8285 is a BCD Decade Synchronous Up/Down Counter and has ten unique binary-coded-decimal (8421) synchronous output states. The input/output functions of the 8284 and 8285 permit cascading of ten stages at the maximum operating frequency of 20 MHz. A detailed discussion of the operation and applications of these counters follows. The MSI design precautions in Section I should be reviewed.

OPERATION OF THE 8284 AND 8285

The 8284 and 8285 are synchronous up/down counters with reset to "0" and set to "15" (8284) or "9" (8285) asynchronous entry clock override (refer to Figure 3-1). Carry-out and propagation of data occur synchronously with the falling edge of the CLOCK input. The Q outputs of all four binaries are available, together with $\overline{Q}_4$ and CARRY-OUT. Both counters utilize four stored-charge binary of the design shown in Figure 3-2.

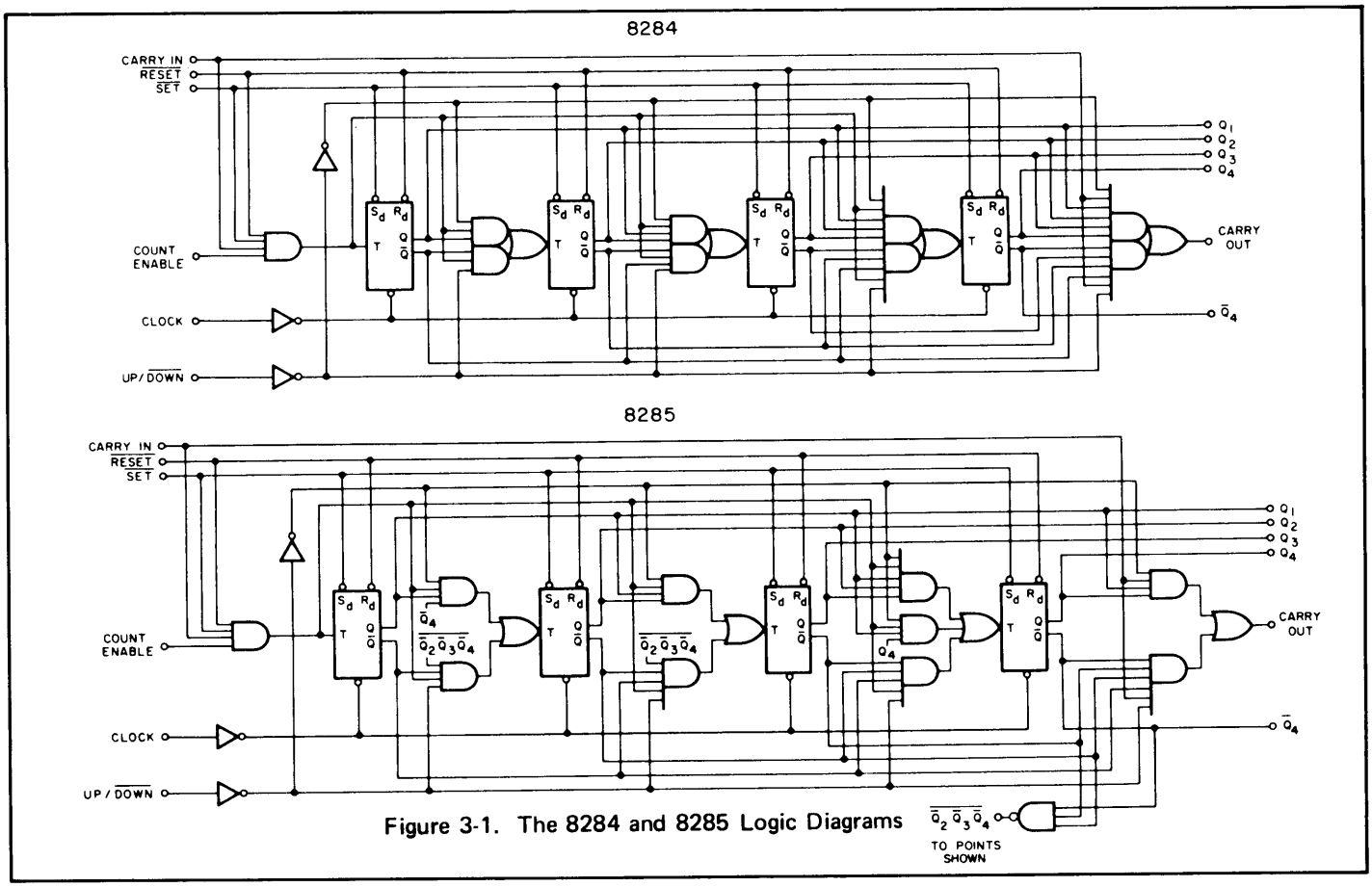


Figure 3-1. The 8284 and 8285 Logic Diagrams

Table 3-1. MODE OF OPERATION

	Set	Reset	Carry In	Count Enable	Up/Down	Function
A. Asynchronous						
	1	0	X	X	X	"0"
8284 Only	0	1	X	X	X	"15"
8285 Only	0	1	X	X	X	"9"
B. Synchronous						
	1	1	0	X	X	Hold *
	1	1	X	0	X	Hold *
	1	1	1	1	0	"Down" Count *
	1	1	1	1	1	"Up" Count *

*Function is synchronous with negative-going transition of the Clock pin.
X = don't care.

CARRY OUT $\quad \text{Carry Out}_{8284} = \text{Carry In}\,(Q_1 Q_2 Q_3 Q_4\ UP + \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{Q}_4\ \overline{UP})$

$\text{Carry Out}_{8285} = \text{Carry In}\,(Q_1 Q_4\ UP + \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{Q}_4\ \overline{UP})$

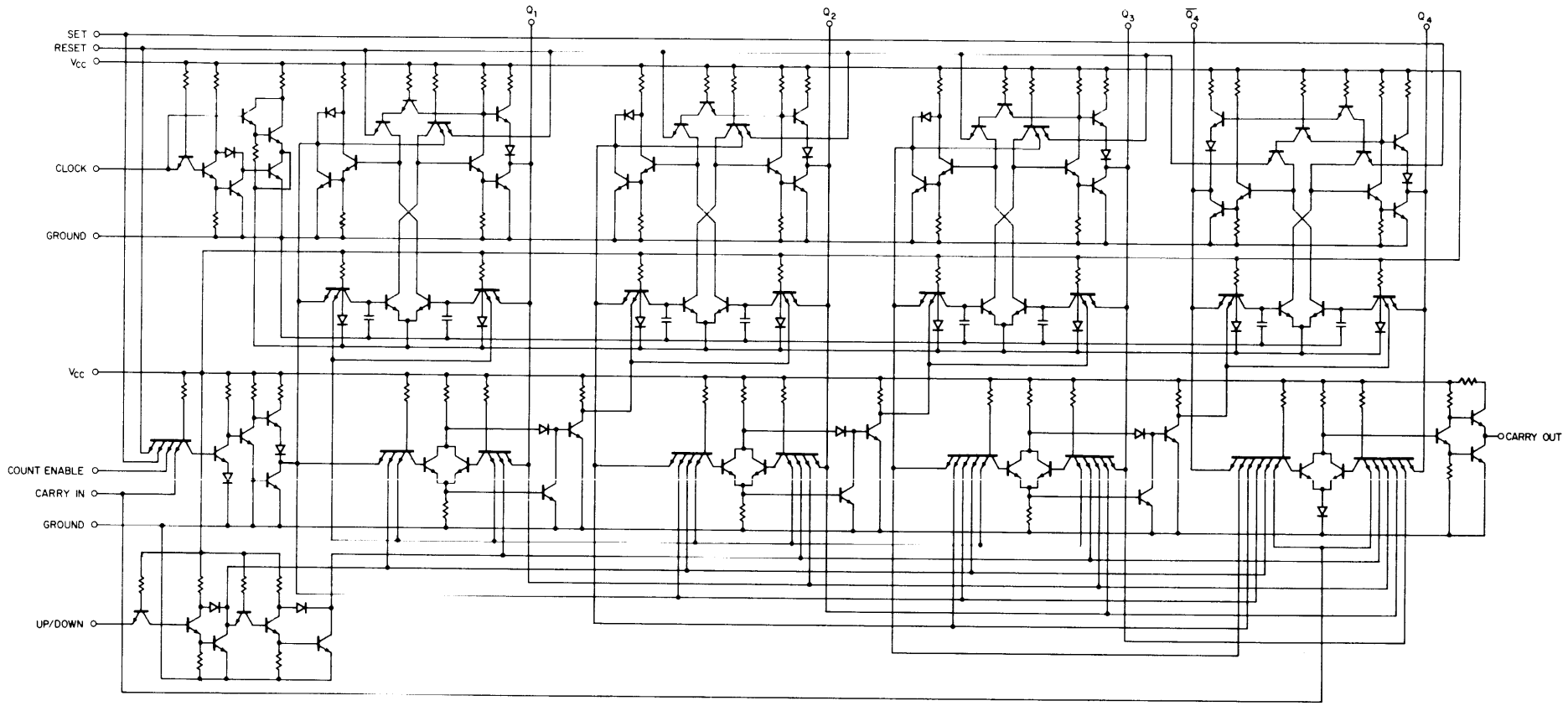


Figure 3-2. The 8284 and 8285 Binary Element

The COUNT-ENABLE input goes to an AND gate which is tied to the toggle ENABLE input of each binary element. This toggle enable AND gate also has the CARRY-IN, $\overline{SET}$, and $\overline{RESET}$ inputs connected to it. As shown in Figure 3-1, if one of these inputs is "0", the counter is disabled and will not count. The input/output function characteristics are described in Table 3-1.

The CARRY-IN input, besides being tied to the toggle enable AND gate, also enables the CARRY-OUT output. The COUNT-ENABLE input has no effect on the CARRY-OUT. Therefore, the carry term can propagate through the counter while counting is inhibited by the COUNT-ENABLE ("0"). This input/output configuration makes it possible to cascade up to eleven stages of 8284s or 8285s with completely synchronous operation at 20 MHz.

For the 8284 Hexadecimal Counter, a binary coded fifteen ($Q_1 = Q_2 = Q_3 = Q_4 =$ "1") in the count-up mode (UP/$\overline{DOWN}$ = "1" level) will generate a carry-out (C_O = "1" level) when CARRY-IN goes high. The 8285 BCD Decade Counter in the count-up mode generates carry-out for a binary coded nine ($Q_1 = Q_4 =$ "1"; $Q_2 = Q_3 =$ "0") when the CARRY-IN input goes to a "1" logic level. In the count-down mode (UP/$\overline{DOWN}$ = "0" level), both counters generate a carry-out when the CARRY-IN is a logic "1" level and a binary coded zero ($Q_1 = Q_2 = Q_3 = Q_4 =$ "0") is detected. The propagation delay from CARRY-IN going to a logic "1" level to CARRY-OUT going to a logic "1" level is typically 15ns. The propagation delay from CLOCK to CARRY-OUT is typically 30ns.*

The stored-charge clocking mechanism is buffered to reduce the clock line loading to a single TTL load. The rise and fall times should be less than 200ns into the internal clock buffer. This rise and fall time limitation will prevent possible oscillations due to poor V_{CC} to GROUND bypassing. With proper bypassing, fall times in excess of 1 μsec have been used to clock the 8284 and 8285 counters. The CLOCK input pulse width must be greater than 20ns at the 1.5V points of the rising and falling edges with an amplitude of 2.6V or greater.

The manner in which the first two 8284s or 8285s are connected is the key to cascading ten stages at the maximum guaranteed toggle rate of 20 MHz (Figure 3-3a). The least significant counter (1) has the COUNT-ENABLE and the CARRY-IN inputs tied together to optimize speed. These paralleled inputs are used to enable ("1" level) or inhibit ("0" level) the counter. The CARRY-OUT is connected to the COUNT-ENABLE inputs of all succeeding stages. The CARRY-IN input of the second stage (2) is tied to V_{CC} which generates an anticipated carry-in 16 counts (8284) or 10 counts (8285) before the COUNT-ENABLE is activated ("1" level) by the CARRY-OUT of the first stage (1).

The $\overline{SET}$ and $\overline{RESET}$ inputs provide complete clock lockout when activated ("0" level). $\overline{RESET}$ and $\overline{SET}$ are accomplished in typically 20ns.

The 2's complement is generated for all negative binary counts of the 8284. The 2's complement $^2(\bar{A})$ of a binary word is found in Table 3-2.

*All propagation delay measurements are taken at the 1.5V level.

Table 3-2. DEFINITION OF 2's COMPLEMENT

2's Complement of A $\quad ^2(\bar{A}) = {}^1(\bar{A}) + 2^\circ$ $\quad$ where: $\quad ^2(\bar{A})$ = 2's Complement of A; $^1(\bar{A})$ = 1's Complement of A

EXAMPLE:

$$^2(\overline{0\ 1\ 1\ 0}) = {}^1(\overline{0\ 1\ 1\ 0}) + 0\ 0\ 0\ 1 = 1\ 0\ 0\ 1 + 0\ 0\ 0\ 1 = 1\ 0\ 1\ 0$$

Count Sequence – UP/$\overline{DOWN}$ = "0"

0 0 1 1	+3
0 0 1 0	+2
0 0 0 1	+1
0 0 0 0	0
1 1 1 1	-1
1 1 1 0	-2
1 1 0 1	-3

The 1's complement of a word is found by inverting all bits: $^1(\overline{1\ 0\ 1\ 0}) = 0\ 1\ 0\ 1.$

System Implementation

Certain precautions must be taken to ensure optimum system performance of MSI circuit designs using TTL techniques.

High-frequency distribution techniques should be used for V_{CC} and GROUND. These techniques should include large ground planes to minimize DC offsets and provide an extremely low impedance path to reduce transient noise on the printed circuit boards. The V_{CC} power supply should be +5V ±5% with R-F (1 GHz) bypassing.

The current spike produced by the totem pole output structures during "0" to "1" switching transitions can cause MSI elements to malfunction if V_{CC} is not properly decoupled to GROUND. A ceramic disc capacitance of 2000pF or more for each totem pole structure should be connected between V_{CC} and GROUND in close proximity to the MSI device to provide proper bypassing. The six output and two internal totem pole structures of the 8284 and 8285 require a 0.02 μF ceramic disc capacitor V_{CC} bypass.

Electrically open inputs degrade the AC and DC noise immunity as well as the switching speed of an MSI circuit. All inputs must be connected to low impedance sources for optimum noise immunity and switching speed. Unused inputs should be tied to a driving source, V_{CC} or GROUND. Unused inputs may be tied directly to V_{CC} if power supply voltage never exceeds 6.0V; otherwise, the input should be tied to V_{CC} through a resistor (1KΩ). More than one unused input may be tied to V_{CC} through the same resistor.

For the 8284 and 8285, RESET and SET should be connected to V_{CC} when unused. COUNT-ENABLE when unused should be connected to the CARRY-IN input or to V_{CC}. The CARRY-IN input for a single counter or the first in a series of cascaded counters can be used to inhibit counting ("0" logic level) by a gate or, when unused, should be tied to V_{CC}.

All rise and fall times (10% to 90%) should be less than 200ns for a pulse amplitude of 2.6V or greater (not to exceed 6.0V).

If interconnections between devices are longer than 8 inches, precautions should be taken to minimize line reflections and ringing. All inputs to the 8284 and 8285 counters are protected with diffused diode clamps. These diodes will limit negative excursions to -1V or less.

Description of Operation

Cascading Counters. Their unique input and output functions make possible the cascading of up to ten 8284 Hexadecimal and 8285 BCD Decade Counters while operating at their guaranteed maximum frequency of 20 MHz. Being able to cascade ten stages permits the designer to count to 2^{40} or 1,099,511,627,776 counts for the 8284 and to 10^{10} or 10,000,000,000 counts for the 8285. These total counts can be achieved in both the up and down count modes with completely synchronous output code transitions at 20 MHz. Further cascading past the eleventh stage is possible, if necessary, but the carry-out of the first stage (C_{O_1}) would have to be buffered.

The following example is intended to clarify the interconnection scheme shown in Figure 3-3a. The example will show the cascading of ten 8285 BCD Decade Counters. The counters will be connected to take full advantage of the "anticipated-carry" capability to achieve 20 MHz synchronous up/down counter operation. This example will only show the count-up mode:

EXAMPLE: The first decade (1) has the CARRY-IN and COUNT-ENABLE inputs tied together. This input is used as the count-enable (C_e) for the entire 10-stage counter. The carry-in (C_i) to carry-out (C_O) propagation delay is typically 15ns (as shown in Figure 3-3b) and the typical propagation delay from the falling edge of the clock (C_L) to C_O is 30ns (as shown in Figure 3-3c for the ninth and tenth clocking transition).

The second decade (2) has the C_{i_2} tied to V_{CC}. The C_{O_2} is therefore always enabled. The C_{O_1} of the first decade which is connected to the C_e of the other nine decades enables the second decade to count one count for every ten counts in the first decade. C_{O_2} is allowed to ripple through all successive decades. The propagation delays are shown below:

For the:

9 9 9 9 9 9 9 9 8 9 to 9 9 9 9 9 9 9 9 9 0 transition

C_L to C_{O_2} = 30ns X 1 decade = 30 ns

C_{i_3} to C_{O_3} = 15ns X 8 decades = 120ns

-150ns -150ns

10 more counts in the first decade at 20 MHz = 500ns +500ns

+350ns

The 500ns between count-enables for the second through tenth decade allows three times the delay required for the carry term to propagate through nine decades. If the designer has a requirement for more than ten stages (either BCD decade or hexadecimal) of synchronous up/down counters, it is possible to buffer the C_O of the first stage and drive the C_e inputs of 24 stages at the maximum operating frequency of 20 MHz. A 25-stage hexadecimal counter is able to store

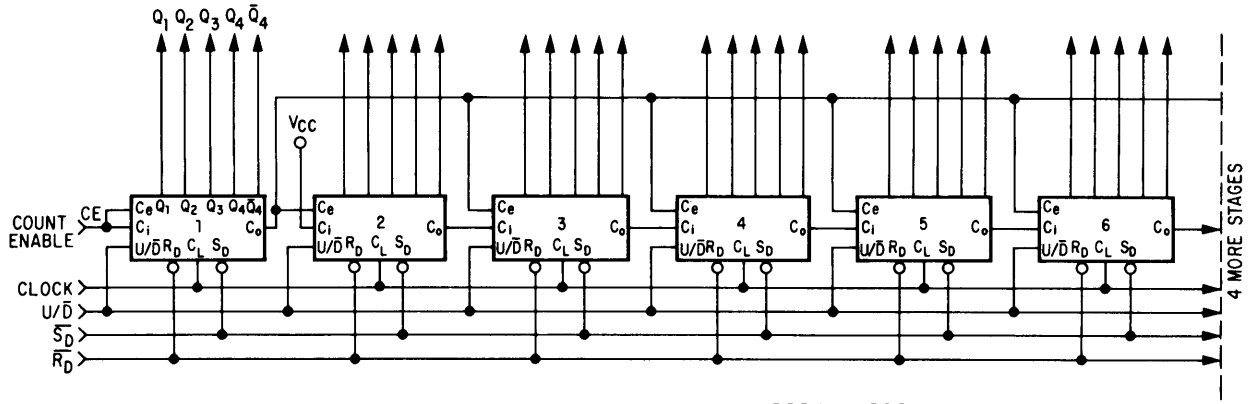


Figure 3-3a. Synchronous Cascading of the 8284 or 8285

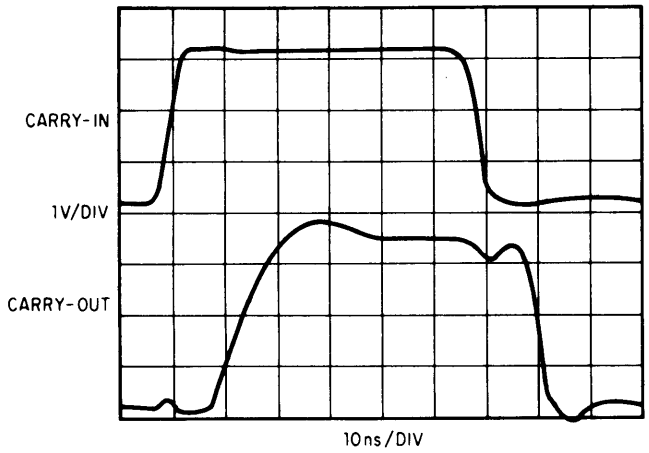


Figure 3-3b. Typical Propagation of CARRY-IN to CARRY-OUT

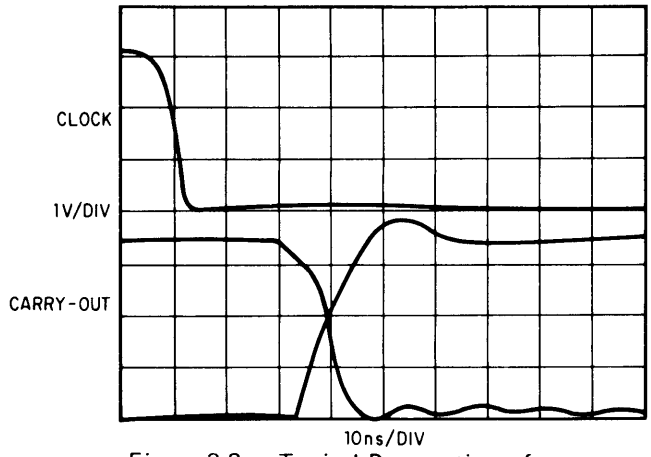


Figure 3-3c. Typical Propagation of CLOCK to CARRY-OUT

2^{100} counts. It would take approximately $2 \cdot 10^{15}$ years at 20 MHz to overflow this counter. A 10-stage hexadecimal will take over fifteen hours to overflow at 20 MHz. Therefore, few requirements ever exceed ten stages.

System Applications

1's Complement Generator. In the count-down mode, the 8284 (hexadecimal) generates the 2's complement (Table 3-2) of any negative count. The 2's complement permits addition of positive and negative binary numbers without code conversion of the negative number. However, if the 1's complement or the reciprocal of the positive binary number is desired, 2^0 (LSB) must be subtracted from the 2's complement number:

	-6 in 2's complement	= 1 0 1 0
	-2^0	-0 0 0 1
then:	-6 in 1's complement	= 1 0 0 1
where:	$2(\bar{A}) - 2^0$	$= 1(\bar{A})$

To generate the 1's complement automatically in the normal counting sequence of a system using 8284s require the addition of a single 8H70 (Triple 3-Input NAND Gate). As shown in Figure 3-4, the combined carry-out ($C_e \cdot C_i$) detects all zero crossings. The 1's complement has two states for zero, all 0s and all 1s. All outputs are set ($\overline{S}_D$ = "0") to "1"s when all "0"s are detected in the count-down (UP/DOWN = "0") mode. Conversely, all outputs are reset ($\overline{R}_D$ = "0") to "0"s when all 1s are detected in the count-up (UP/DOWN = "1") mode. An example of the generated "1"s complement counting sequence is shown in Table 3-3.

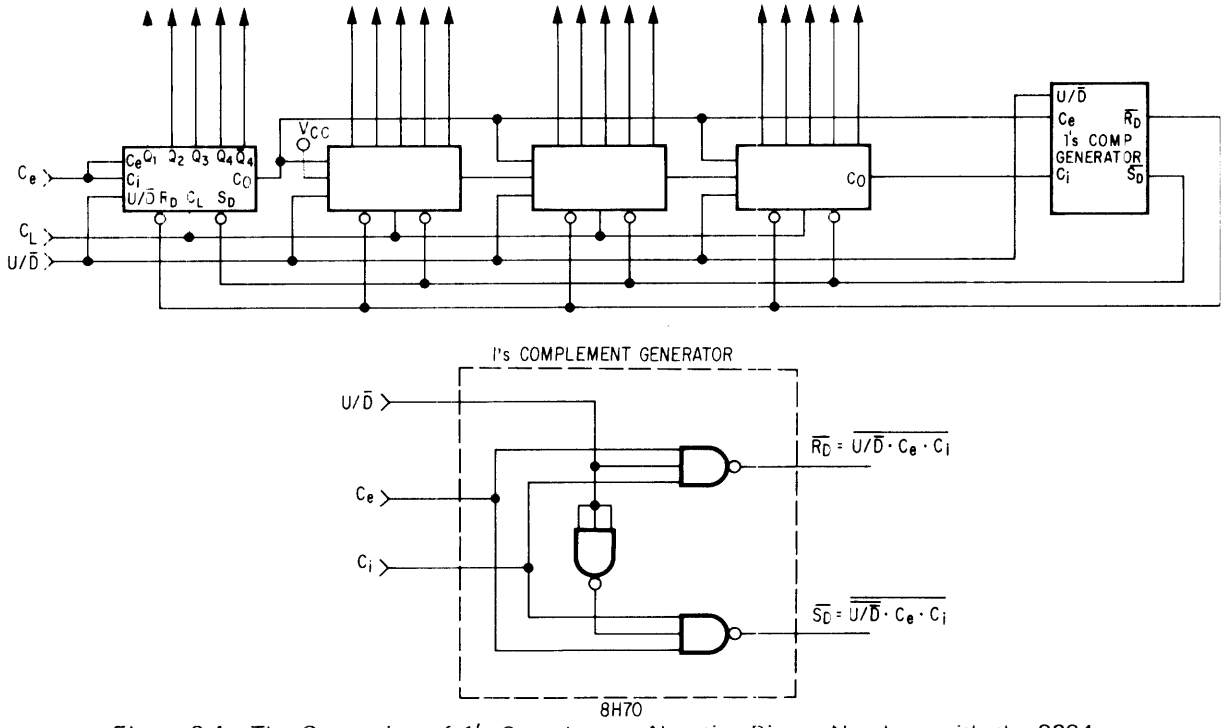


Figure 3-4. The Generation of 1's Complement Negative Binary Numbers with the 8284

Table 3-3. "1"s COMPLEMENT COUNTING SEQUENCE.

Clock	Decimal	Binary		$C_e \cdot C_i$	U/$\overline{D}$	S_D	R_D
0	+3	0 0 1 1		0	0	1	1
1	+2	0 0 1 0		0	0	1	1
2	+1	0 0 0 1		0	0	1	1
3	0	0 0 0 0		1	0	0	1
	0	1 1 1 1		0	0	1	1
4	-1	1 1 1 0		0	0	1	1
5	-2	1 1 0 1	1's Complement	0	0	1	1
6	-1	1 1 1 0		0	1	1	1
7	0	1 1 1 1		1	1	1	0
		0 0 0 0		0	1	1	1
8	+1	0 0 0 1		0	1	1	1

Magnitude and Sign Generator. The 1's and 2's complement representations of negative numbers are insufficient for some applications. When decoding the outputs of 8285s for numeric readouts, it is desirable to produce the absolute value of a number and its sign. A decoding system with these features eliminates any further decoding to display negative numbers. The magnitude and sign capability of the configuration shown in Figure 3-5 simplifies the decoding of negative numbers for both the 8284 and the 8285.

Circuit Description. As shown in Figure 3-5, Gates 1, 2, 3 and 4 form a D-type latch. The U/$\overline{D}$ input is transferred to point P (Gate 3) when the combined carry-out ($C_e \cdot C_i$) goes to a "1" level. The function generated at the output U/$\overline{D}$ is:

$$U/\overline{D}_O = S \cdot P + \overline{S} \cdot \overline{P}$$

where: P = "1" ($\overline{P}$ = "0") then N $\geqslant$ 0

P = "0" ($\overline{P}$ = "1") then N $\leqslant$ 0

N = Number of counts

S = "1", count positive

S = "0", count negative

The latch (P) is enabled when carry-in ($C_e \cdot C_i$) goes to "1" which occurs at all zero crossings.

Table 3-4 shows the count sequences generated for a single 8285 BCD Decade Counter with the magnitude and sign generator connected.

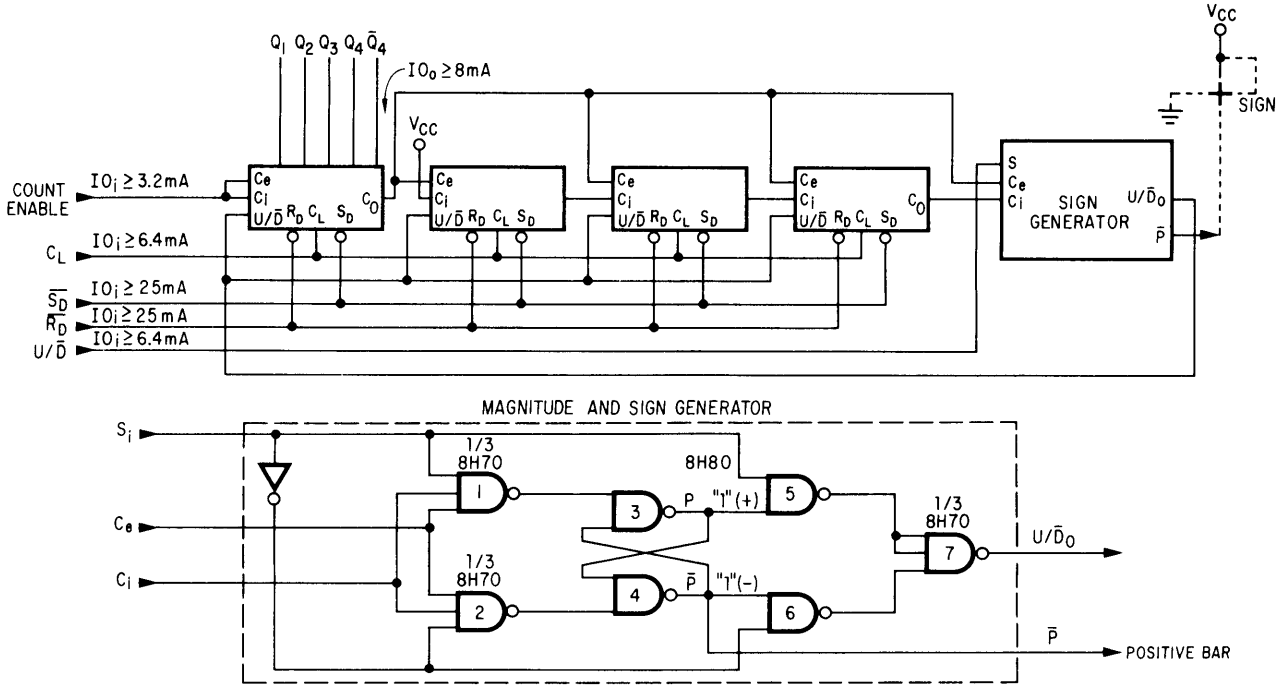


Figure 3-5. The Generation of Magnitude and Sign

Table 3-4. COUNT SEQUENCE USING THE MAGNITUDE AND SIGN GENERATOR

S*	Carry-Out $C_e \cdot C_i$	P	U/$\bar{D}$	N Clock	Binary	Decimal
0	0	1	0	0	0 0 1 1	+3
0	0	1	0	1	0 0 1 0	+2
0	0	1	0	2	0 0 0 1	+1
0	0	1	0	3	0 0 0 0	-0
0	1/0	0	1	4	0 0 0 1	-1
0	0	0	1	5	0 0 1 0	-2
0	0	0	1	6	0 0 1 1	-3
1	0	0	0	7	0 0 1 0	-2
1	0	0	0	8	0 0 0 1	-1
1	0	0	0	9	0 0 0 0	+0
1	1/0	1	1	10	0 0 0 1	+1
1	0	1	1	11	0 0 1 0	+2
0	0	1	0	12	0 0 0 1	+1
0	0	1	0	13	0 0 0 0	-0
0	1/0	0	1	14	0 0 0 1	-1

*S = "1" – Count Up S = "0" -- Count Down

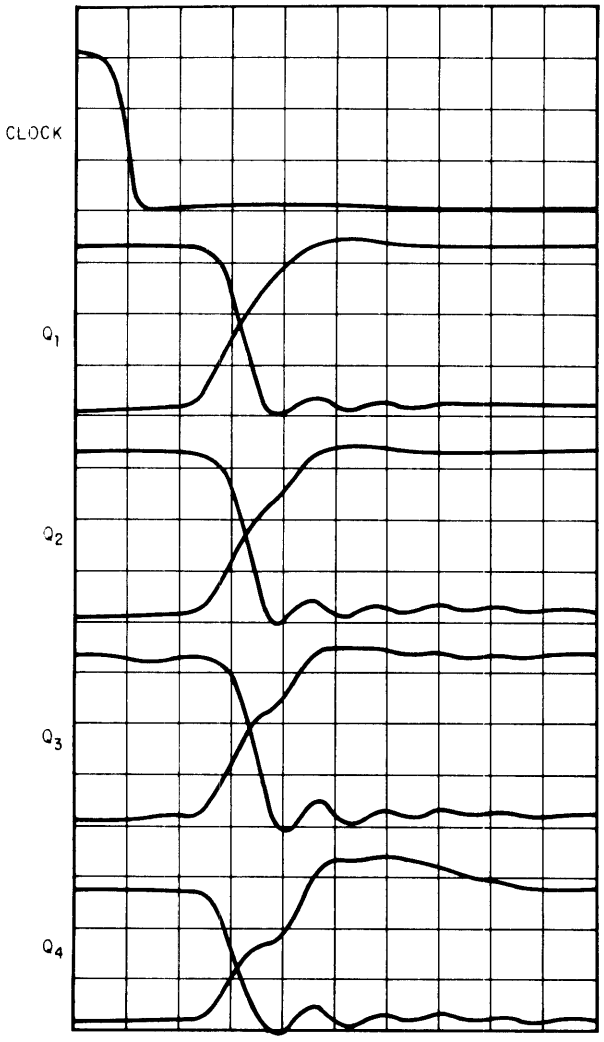


Figure 3-6. The Synchronous Output Changes of the 8284 and 8285

1-Out-Of-N Decoder. All the outputs of an 8284 and 8285 synchronous counter change simultaneously, eliminating the generation of false transition codes. Figure 3-6 shows the outputs of the 8284/8285 changing 22ns* after the falling edge of the input CLOCK.

A 1-in-16 decoder (4 lines to 16 lines) using an 8284 (Hexadecimal Counter) and two 8250s (Binary to Octal Decoders) is shown in Figure 3-7a. The necessity of having the $\bar{Q}_4$ output is apparent in this application. If $\bar{Q}_4$ was not available, an inverter would have to be connected to the Q_4 output to generate $\bar{Q}_4$ at some finite delay time after Q_4. This delay could cause possible decoding errors.

Figure 3-7b shows the use of an 8285 BCD Decade Counter in conjunction with an 8251 BCD to Decimal Decoder (Figure 3-7c).

The typical propagation delay for both counter decoder systems from CLOCK input to decoded output is 30ns.

Octave Frequency Multiplexer. The frequency multiplexer shown in Figure 3-8a uses two 8284s and one 8232 8-Input Digital Multiplexer (Figure 3-8b). This circuit permits any one of the eight outputs of the 8-bit synchronous binary counter (two 8284s) to be decoded. The decoded output frequency is determined by the inputs N_0, N_1, N_2 and Inhibit as shown in the truth table in Figure 3-8.

The propagation delay from the falling edge of the CLOCK to the outputs of the multiplexer (8232) is the same for all decoded frequencies. This propagation delay is typically 37ns for true output (f_O) and 30ns for the inverted output ($\bar{f}_O$).

Variable Modulus Counter. Figure 3-9 shows a variable modulus counter or programmable frequency divider using synchronous counters (8284s or 8285s) and 4-bit digital comparators (8242s). The 8242 (see truth table) has open-collector outputs. As shown in Figure 3-9 for four 8284s or 8385s, a "1" logic level is generated at point Z when the counter's outputs digitally compare with the input binary (8284) or BCD (8285) 16-bit word. The counter must be connected in the count-up (U/D = "1") mode. R_L was calculated for minimum propagation delay. The reset ("0") pulse will be greater than 40ns. The reset driver, such as 8H90 Inverter, must be able to sink at least 24mA ($IO_O \geqslant 24mA$).

*All propagation delay measurements are taken at the 1.5V level.

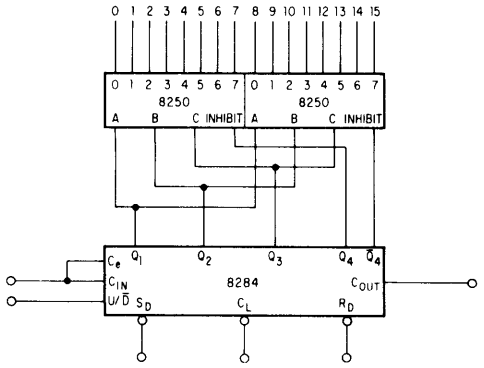


Figure 3-7a. 1-in-16 Counter/Decoder

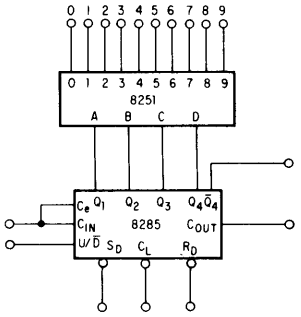


Figure 3-7b. 1-in-10 Counter/Decoder

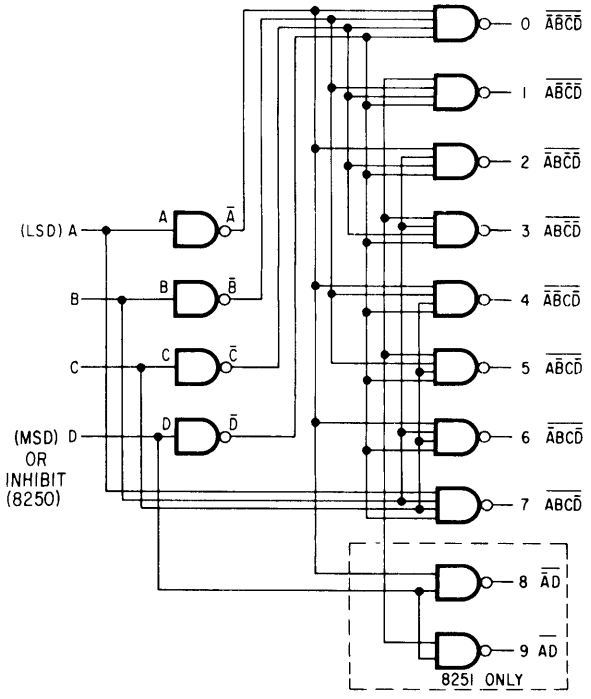


Figure 3-7c. The 8250/8251 Octal/Decade Decoder

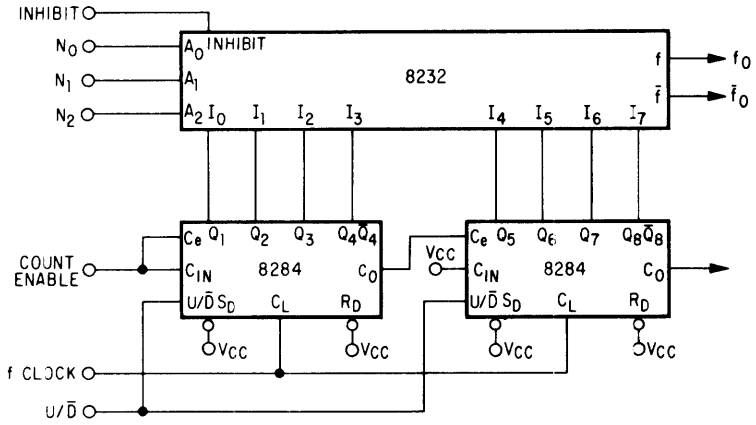
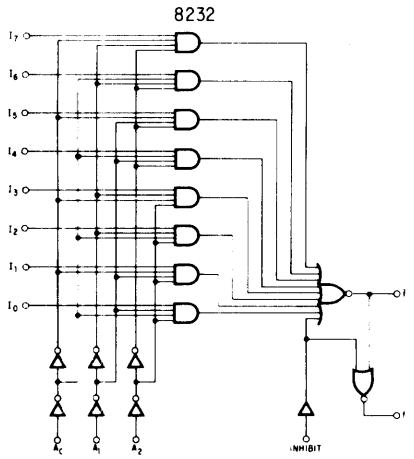


Figure 3-8a. Octave Frequence Multiplexer.



TRUTH TABLE

N_0	N_1	N_2	INHIBIT	f_0	$\bar{f}_0$	
0	0	0	0	Q_1	$\bar{Q}_1$	f/2
1	0	0	0	Q_2	$\bar{Q}_2$	f/4
0	1	0	0	Q_3	$\bar{Q}_3$	f/8
1	1	0	0	Q_4	$\bar{Q}_4$	f/16
0	0	1	0	Q_5	$\bar{Q}_5$	f/32
1	0	1	0	Q_6	$\bar{Q}_6$	f/64
0	1	1	0	Q_7	$\bar{Q}_7$	f/128
1	1	1	0	Q_8	$\bar{Q}_8$	f/256
X	X	X	1	0	0	

Figure 3-8b. The 8232 8-to-1 Line Multiplexer

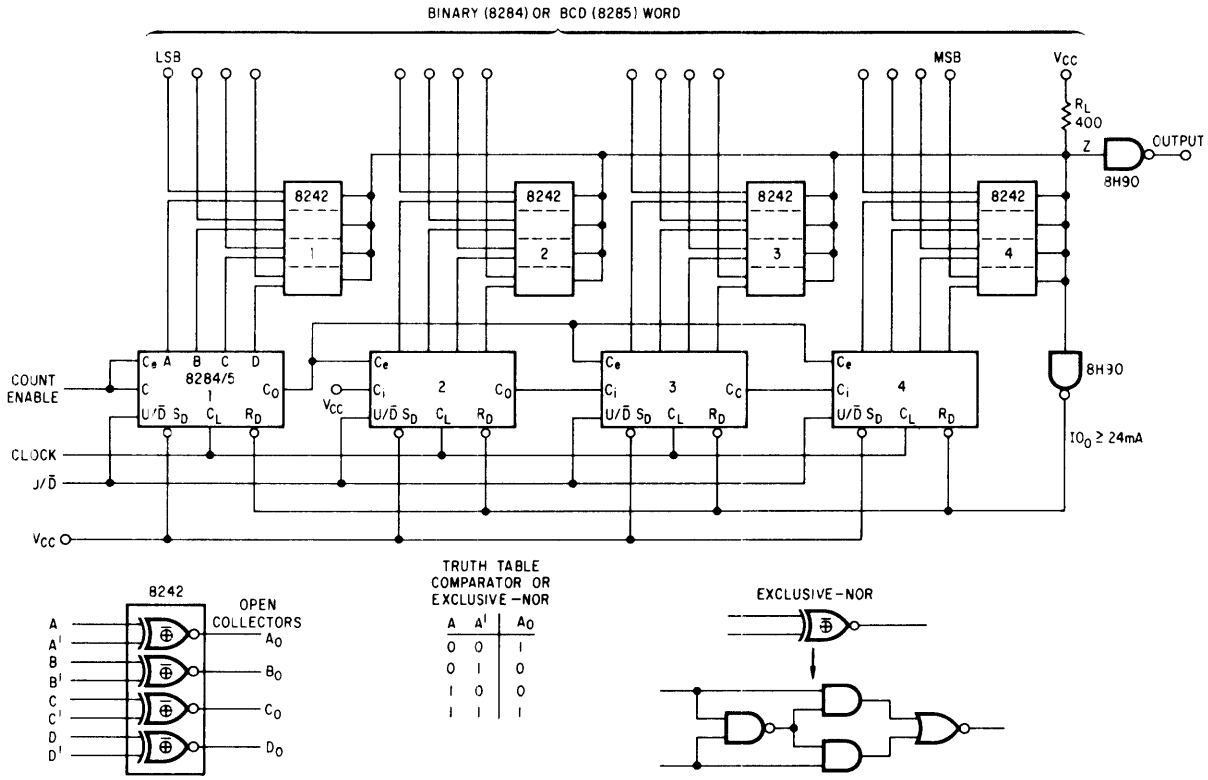


Figure 3-9. Variable Modulus Counter

SECTION IV

MSI SHIFT REGISTERS AND I/O BUFFER REGISTERS

A shift register can consist of an arbitrary number of binaries which are used primarily for temporary storage of digital data. There are four basic shift register classifications: (1) serial input to serial output, (2) serial input to parallel output, (3) parallel input to serial output, and (4) parallel input to parallel output, or buffer registers. Buffer registers may be divided into two categories: (a) clocked binary elements, and (b) strobed latch binary element. All the registers to be discussed are produced from D-type binary. The binary level ("1" or "0") present at the D or Data input appears at the true (Q) output upon activation of the CLOCK or STROBE.

The MSI shift and buffer registers to be discussed in this section will be: the 8270 and 8271, 4-Bit Universal Shift Register, the 8276 Serial Input to Serial Output 8-Bit Shift Register, the 8200, 8201, 8202 and 8203 10-Bit D-type Clocked Buffer Register, and the 8275 D-Type Strobe Quadruple Bistable Latch. Some specific applications are mentioned in the latter part of this section.

8270 AND 8271 4-BIT UNIVERSAL SHIFT REGISTER

Operation of the 8270 and 8271

The 8270/8271 is a 4-bit serial and parallel synchronous entry shift register with serial and parallel outputs. Figures 4-1a and 4-1b illustrate the logic diagram and circuit diagram, respectively. The buffered LOAD and SHIFT inputs control the four input AND-OR-INVERT gates of the 8270/8271 permitting either serial or parallel data to be synchronously entered on the falling edge of the Clock, as shown in Table 4-1. There are four modes of operation: (1) the 8270/8271 will store information, (2) parallel information will be synchronously entered, (3) and (4) serial data will be shifted to the right. It is impossible to cause a malfunction while changing modes of operation.

In addition to the 8270 features, the 8271 provides the not-true output for the fourth stage ($\bar{D}_O$) and a common asynchronous $\overline{\text{RESET}}$ input ($\bar{R}_D$). While $\overline{\text{RESET}}$ is activated, the CLOCK and control inputs are completely inhibited internally.

Table 4-1. THE EFFECT OF THE LOAD AND SHIFT INPUTS TO THE 8270/8271.

LOAD	SHIFT	OPERATING MODE
0	0	(1) Store (with clock running)
1	0	(2) Synchronous parallel load
0	1	(3) Shift right
1	1	(4) Shift right

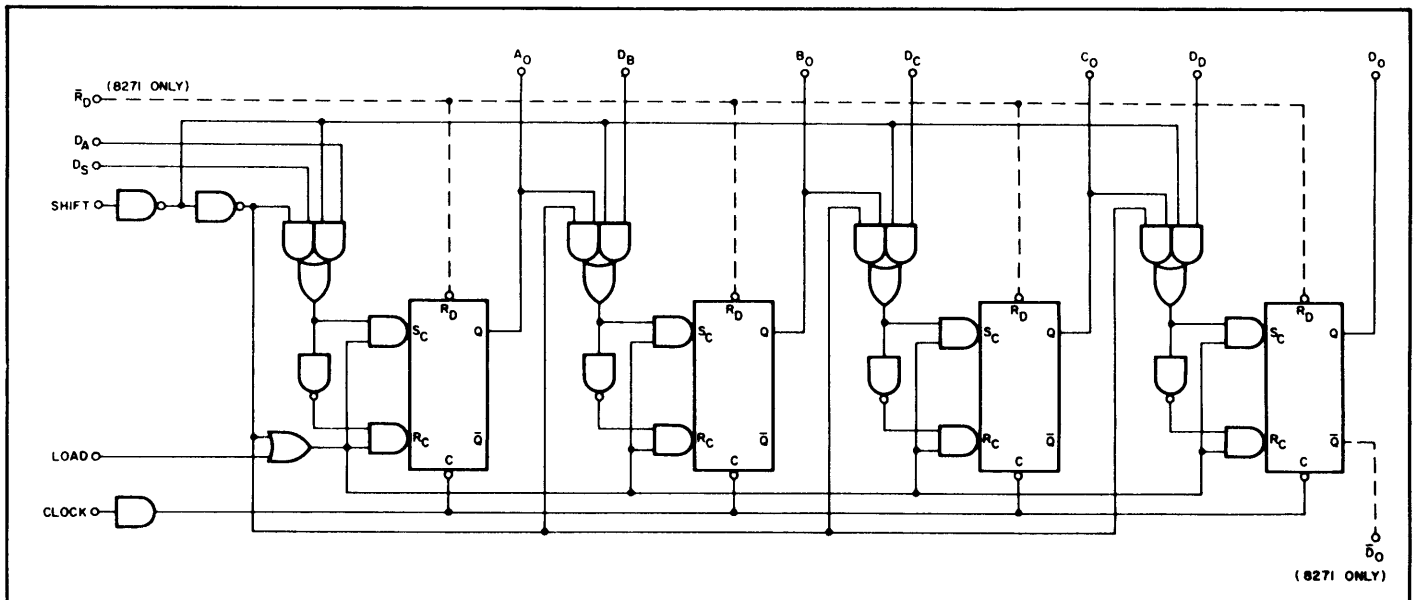


Figure 4-1a. The Logic Diagram of the 8270/8271

System Implementation

Many system malfunctions will be precluded by conservative or over-designed V_{CC} to GROUND bypassing (as mentioned in Section I). Each 8270/8271 should have at least 0.01μF of ceramic disc capacitance located as near to the package as possible from a practical standpoint. Don't try to cut costs by ignoring the recommended amount of power supply bypassing in a system designed with TTL gates, binaries and MSI arrays. The result could possibly be disastrous: a few pennies saved on capacitors could cost a company many thousands of dollars in future repairs and replacements.

The clock pulse should be greater than 20ns. The fall time should be less than 150ns. The 8270/8271 uses a stored-charge clocking mechanism internally which nominally requires a 75ns clock fall time. However, the clock buffer, having a gain of approximately 10, produces a clocking characteristic similar to a DC clocked device. Fall times in excess of 1μsec have been used with satisfactory results. Long clock fall times are not recommended due to noise problems and possible oscillations in the clock buffer. This buffer also reduces the CLOCK input DC load to less than 1.2mA.

The control inputs, LOAD and SHIFT, should be driven from a low impedance source in order to maintain good noise immunity. A low impedance source can be V_{CC}, GROUND or an 8000 series gate, or equivalent. If a single function such as shift right (Modes 3 and 4) is desired, the SHIFT input should be tied to V_{CC}, and the LOAD input can be connected to V_{CC} or GROUND (see Table 4-1). The $\overline{\text{RESET}}$ input ($\overline{R}_D$) of the 8271 should be tied to V_{CC} (when unused) or driven by a DTL/TTL gate. The data inputs (D_S, D_A, D_B, D_C and D_D) should also be tied to a low impedance when in use or when unused, may be left open. However, conservative design techniques dictate that all inputs to an MSI device must be connected to a low impedance source at all times. This precaution eliminates the possibility of having noise capacitively couple onto the highly complex MSI array through an open input terminal. The logic levels at the control inputs must be present typically 30ns before a clocking transition operates properly. The data inputs (D_S, D_A, D_B, D_C and D_D) should be present typically 15ns preceding the clock. These data inputs require 0ns hold time after the clock falls.

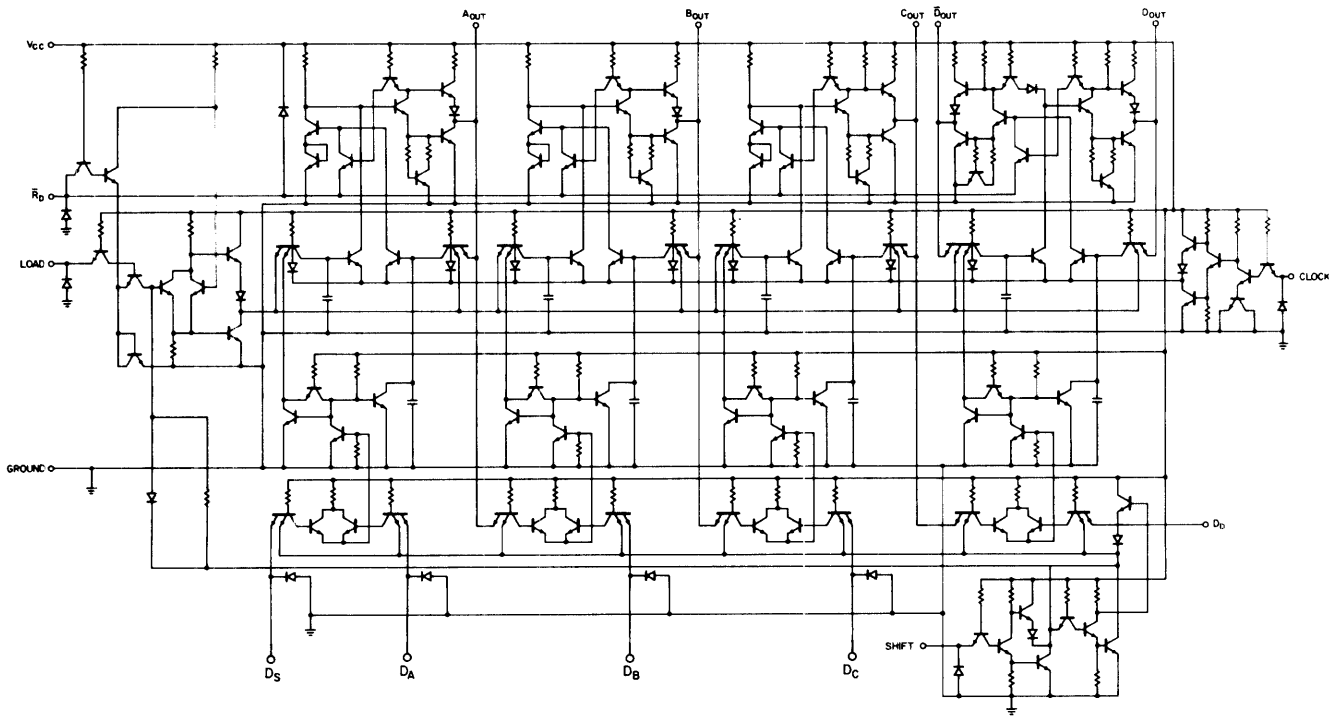


Figure 4-1b. The Circuit Diagram of the 8270/8271

Maximum Capacitive Loading

Since all four outputs are buffered, the maximum capacitive loading is limited only by output rise and fall time requirements. For large capacitive loads, the current spiking when turning off will be very long in duration, significantly increasing the average power consumption. Refer to Appendix II.

8276 8-BIT SHIFT REGISTER

Operation of the 8276

The 8276a is serial-input/serial-output 8-bit shift right shift register. The basic die contains eight R-S, master-slave binaries, input gating for both TRANSFER INHIBIT and serial DATA, and an inverting clock driver. Figure 4-2a shows the circuit diagram. The logic diagram is shown in Figure 4-2b.

The DATA INPUT and DATA ENABLE (inputs A and B) are redundant and may be interchanged (see Figure 4-2). An internal inverter provides the complement to the first R-S binary of the shift register. Each input (A, B, CP, and I_X) is fully buffered and appears as only one TTL input load.

The internal clock driver/inverter produces a single transfer or shift of data from one bit to the next on the positive-going or rising edge of the input clock pulse.

The TRANSFER INHIBIT input is buffered, as in the CLOCK input, with an inverting driver. A "1" or high level on the TRANSFER INHIBIT line prevents the transfer of data from the master to the slave sections.

The information presented at the A and B input gate 25ns before the clock input goes high will appear at the Q output eight "0" or "1" clock input transitions later. Although the set-up times are typically less than 10ns, the transfer rate or clock frequency is typically greater than 20 MHz.

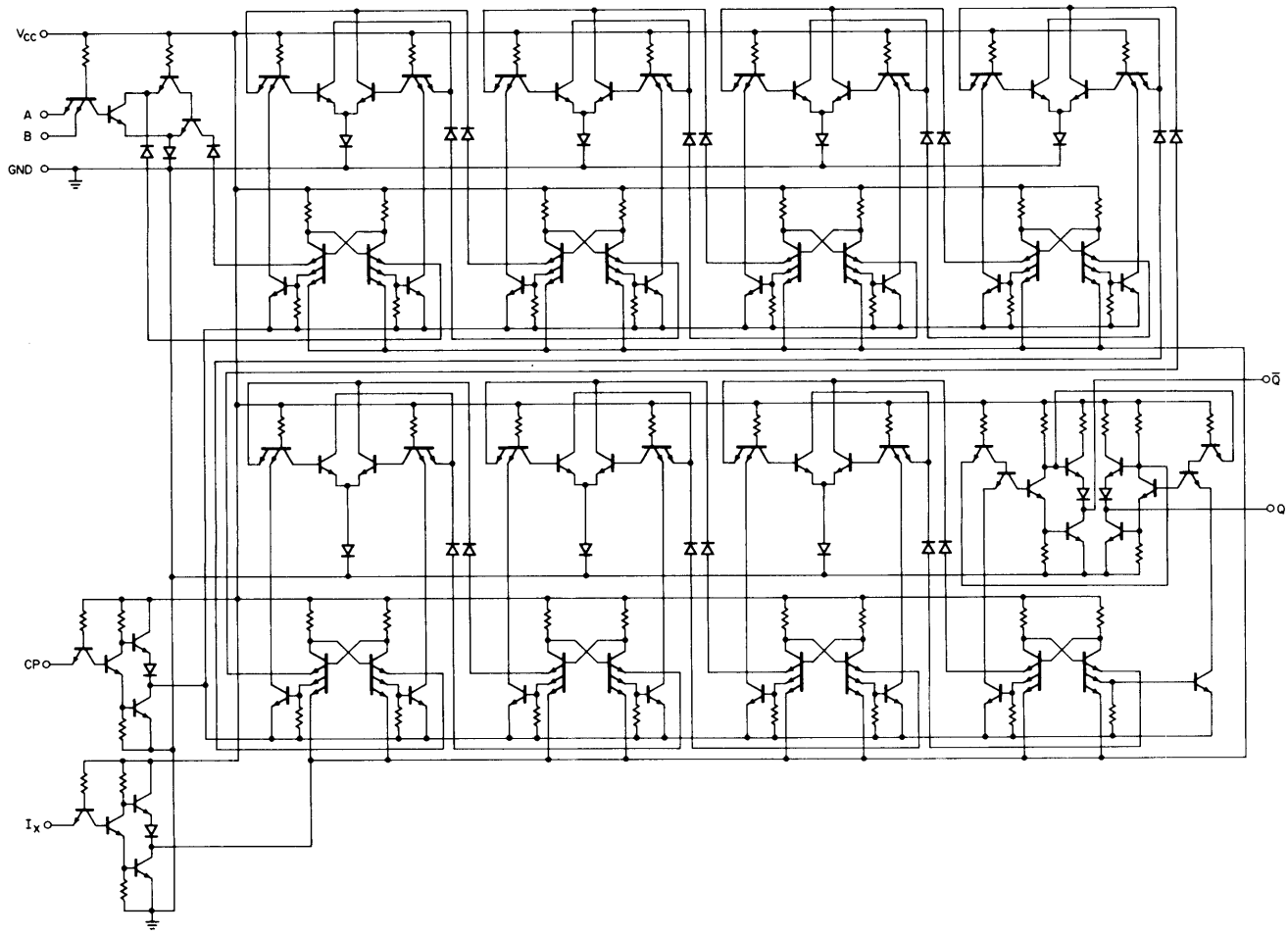


Figure 4-2a. 8276 Circuit Diagram

System Implementation

The clock driver/inverter is a classic TTL gate (as are the Q and $\overline{Q}$ output structures). As mentioned in Section I, due to positive feedback paths and current spike inherent to all medium and high speed TTL structures, the clock inverting buffer will oscillate if the clock input rise and fall times are too long. These oscillations on the rising and falling edge of the clock pulse will generate an indeterminate number of clocking transitions. If the clock input pulse has a rise and fall time of less than 200ns and an amplitude of greater than 2.6V, oscillation will not occur in the clock buffer. A classic symption of this problem is the appearance of the input data at the Q output after only one or two clock pulses.

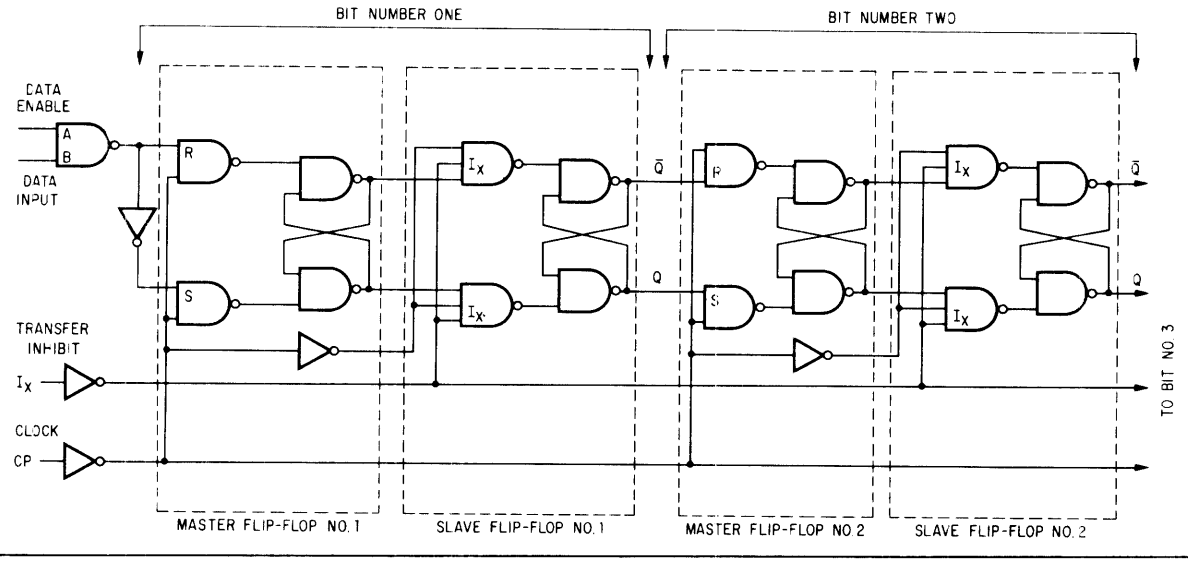
The V_{CC} to GROUND ceramic disc bypass capacitor should be greater than 0.01μF. The DATA ENABLE input should be connected to V_{CC} when not in use. If the TRANSFER INHIBIT is not being utilized, it must be ground. A floating or open TRANSFER INHIBIT input prevents the transfer of data.

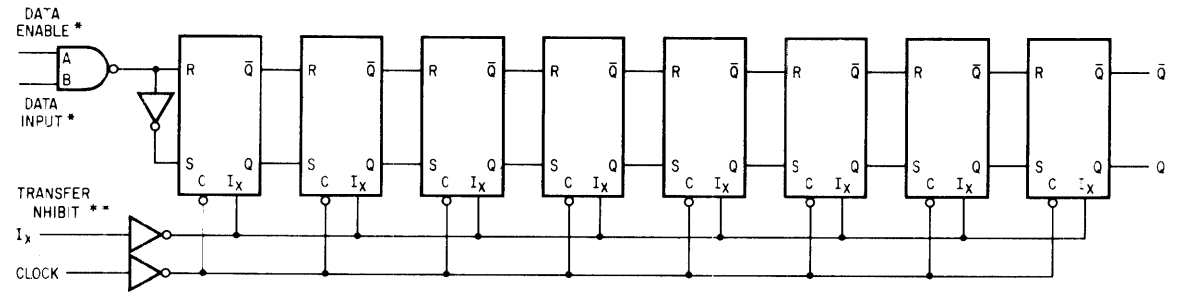
Maximum Capacitive Loading

The Q and $\overline{Q}$ outputs are buffered which eliminates a capacitive loading problem. The only consideration to output capacitance loading should be the desired rise and fall times.

AC CHARACTERISTICS OF THE 8276

CURVE 4-1 I_{CC} (Power Supply Current) vs. clock frequency is shown in this curve where: T_A = 25°C, V_{CC} = 5.00±10% under full DC fan-out.





* NOTE: THESE FUNCTIONS ARE INTERCHANGEABLE

** TRANSFER INHIBIT PREVENTS TRANSFER OF DATA FROM MASTER TO SLAVE

TRUTH TABLE

t_n A (Data Enable)	t_n B (Data Input)	t_n+8 Q
0	0	0
0	1	0
1	0	0
1	1	1

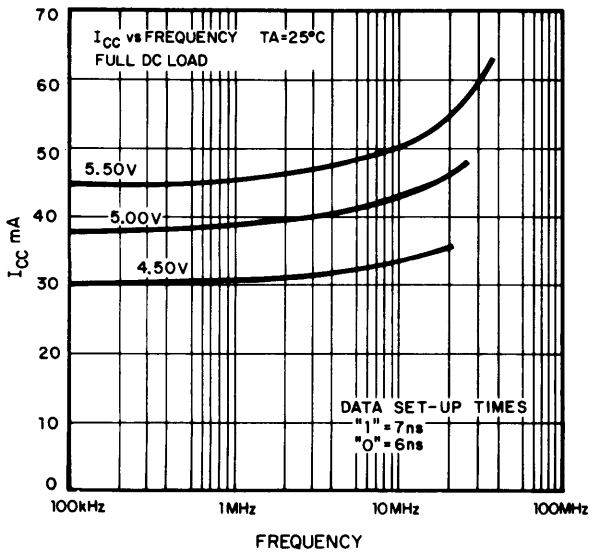
Notes:

t_n = Bit time before clock pulse.

t_n+8 = Bit time after 8 clock pulses.

Figure 4-2b. The Logic and Function Diagram of the 8276

Curve 4-1. I_{CC} vs. Frequency.



8200 DUAL 5-BIT BUFFER REGISTER (D-TYPE); 8201 DUAL 5-BIT BUFFER REGISTER ($\overline{D}$-TYPE); 8202 10-BIT BUFFER REGISTER (D-TYPE); 8203 10-BIT BUFFER REGISTER ($\overline{D}$-TYPE)

Four I/O buffer register, the 8200/8201/8202/8203, are fabricated from the same die with four metal variations. The D or $\overline{D}$ input and Q output are brought out from all ten binaries. All four combinations of dual 5-bit, single 10-bit, D-type and $\overline{D}$-type (D-complement) are made available. The dual 5-bit configurations have two CLOCK inputs and no reset. The single 10-bit configurations have a single CLOCK and a single $\overline{RESET}$ input driving all ten binaries.

Operations of the 8200/8201/8202/8203

The logic diagrams for the 8200/8201/8202/8203 are shown in Figure 4-3a, b, c and d, respectively. Figure 4-4 illustrates

DUAL 5-BIT BUFFER REGISTER

TRUTH TABLE

8200

D_n	Q_{n+1}
1	1
0	0

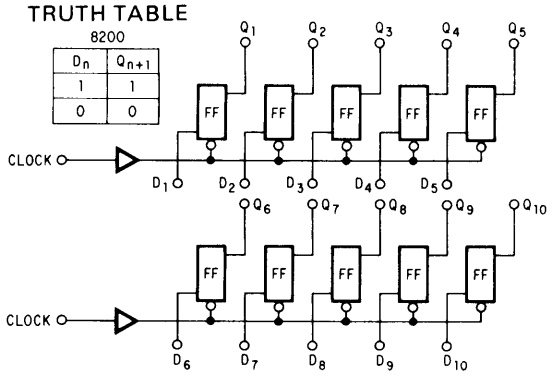


Figure 4-3a. 8200

DUAL 5-BIT BUFFER REGISTER— INVERTED INPUTS

TRUTH TABLE

8201

$\overline{D}_n$	Q_{n+1}
1	0
0	1

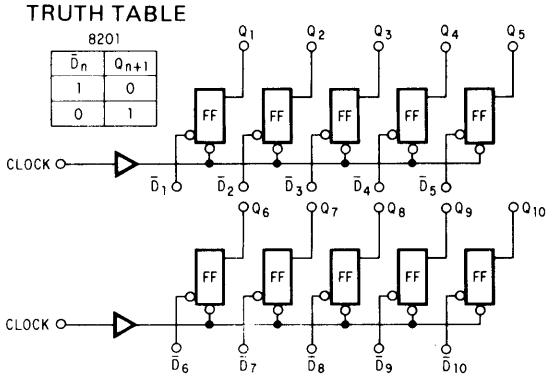
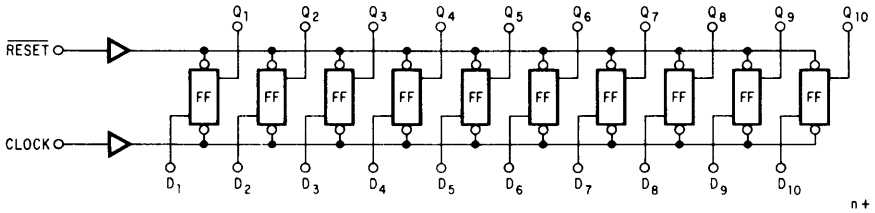


Figure 4-3b. 8201

10-BIT BUFFER REGISTER



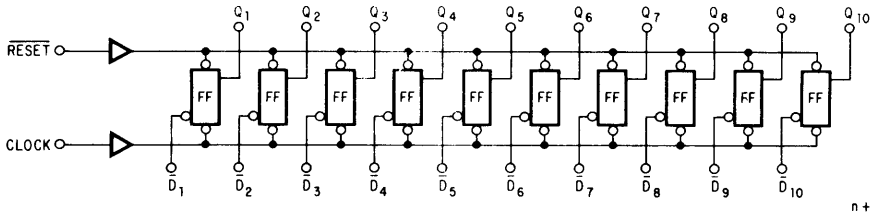
8202

D_n	$\overline{RESET}$	Q_{n+1}
1	1	1
0	1	0

$\overline{RESET} = 0 \Rightarrow Q = 0$
(OVERIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK

Figure 4-3c. 8202

10-BIT BUFFER REGISTER—INVERTED INPUTS



8203

$\overline{D}_n$	$\overline{RESET}$	Q_{n+1}
0	1	1
1	1	0

$\overline{RESET} = 0 \Rightarrow Q = 0$
(OVERIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK

Figure 4-3d. 8203

the composite circuit diagram of a single binary with clock and reset buffers. The binary is a DC couple master-slave type. The D and D-complement inputs may be interchanged depending upon the application without producing a propagation time-differential. This characteristic is made possible through the unique D/D-complement gating connection in conjunction with the master latch.

When the CLOCK input is "0", the output of clock buffer is "0" or less than 0.4V, and the D/D-complement inputs are locked out. This locking out of the data inputs occurs because the collectors of either the A or B transistors when turned on is held at about 1V (one $V_{CE(SAT)}$ and a diode drop). Thus, only when the clock goes high can the input (D or $\overline{D}$) control the master. The clock line, upon going low again, turns on either transistor C or D (depending on the state of the master latch) and locks out the D or $\overline{D}$ input. If C is turned on, the output (Q) goes to a "1" level. The output attains a "0" state when the D transistor is turned on.

System Implementation

The binaries of the 8200/8201/8202/8203 are DC-clocked master-slave elements which respond to the negative-going threshold of the input clock. The clock rise and fall times should be less than 200ns with an amplitude of 2.5V to prevent clock buffer oscillations. The minimum clock pulse width should be greater than 25ns.

The $\overline{RESET}$ ($\overline{R}_D$) input must be tied up to V_{CC} when not in use. The $\overline{R}_D$ can also be driven by a TTL gate, but must never be left floating. Both the clock and reset lines are only one (1.6mA) TTL "0" level load.

The propagation delays of the CLOCK input to Q output "1" and "0" levels and $\overline{RESET}$ ($\overline{R}_D$) to Q output "0" levels are typically less than 30ns. The maximum transfer rate is typically greater than 30 MHz. The D/$\overline{D}$ input set-up time is typically less than 10ns, and the input may be changed as the CLOCK falls (0ns hold time).

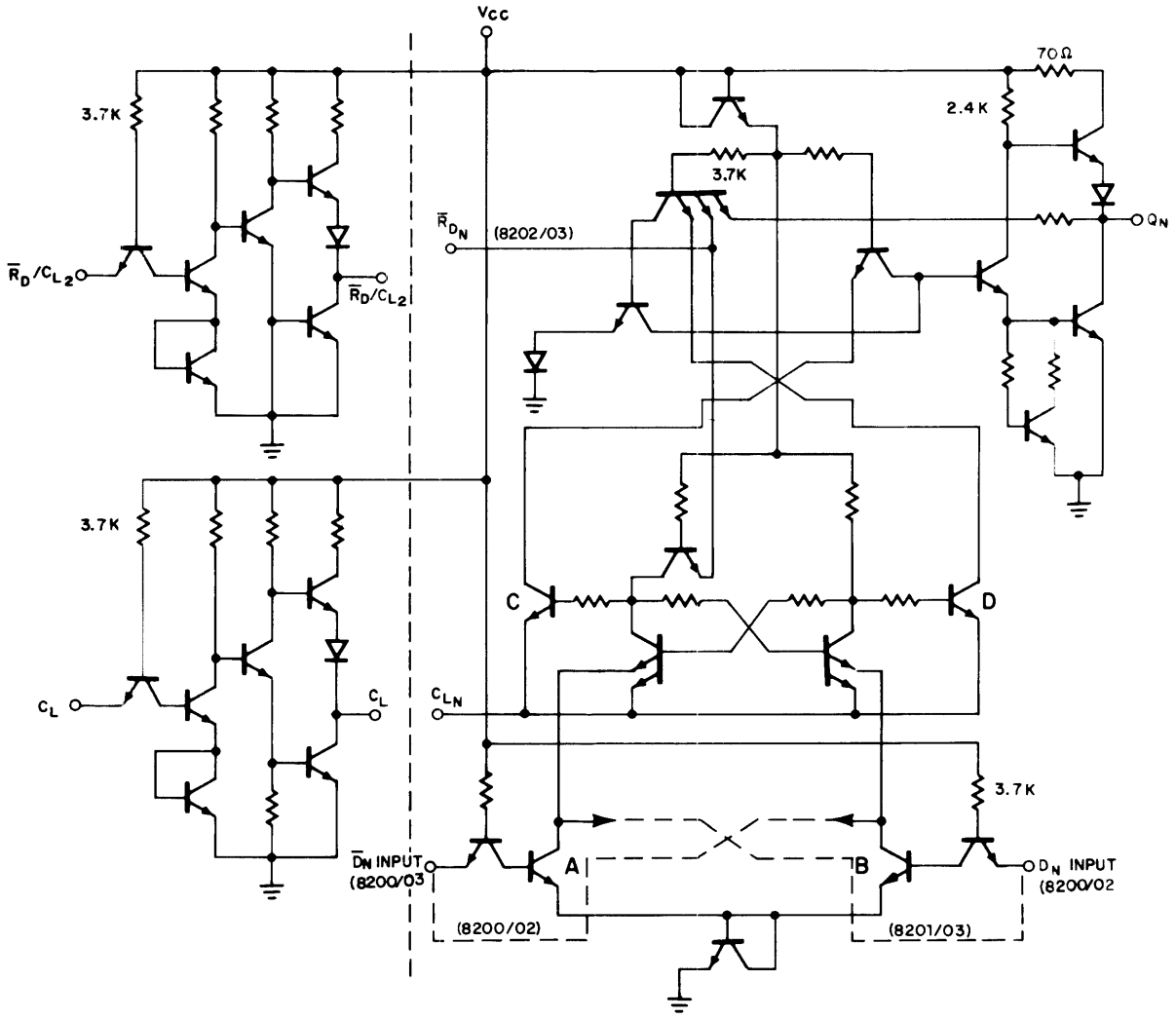


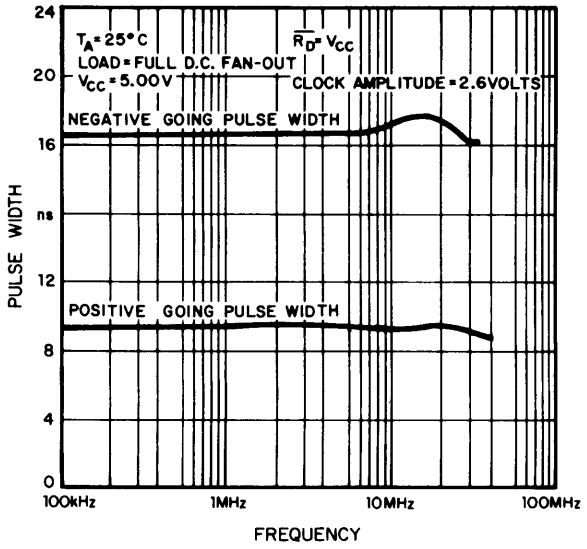
Figure 4-4. Composite Circuit Diagram of the 8200/8201/8202/8203

The power supply bypass should be in excess of 0.05μF of ceramic disc capacitance. Section I should be referenced for specific TTL system implementation techniques.

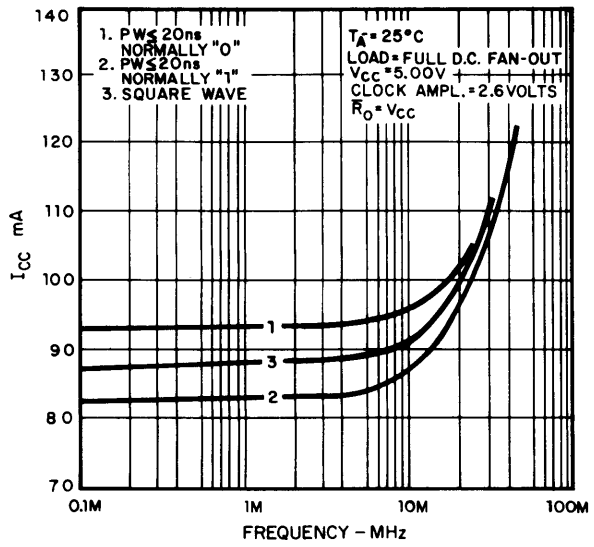
Maximum Capacitive Loading

Even though the slave latch is not buffered, high capacitive loading of the 8200/8201/8202/8203 outputs does not significantly alter the operation of the register. When the CLOCK is low, the output is effectively only a buffer for the master latch. The master is disconnected from the slave latch when the CLOCK is high ("1").

Curve 4-2. Minimum Pulse Width vs. Frequency for the 8202.



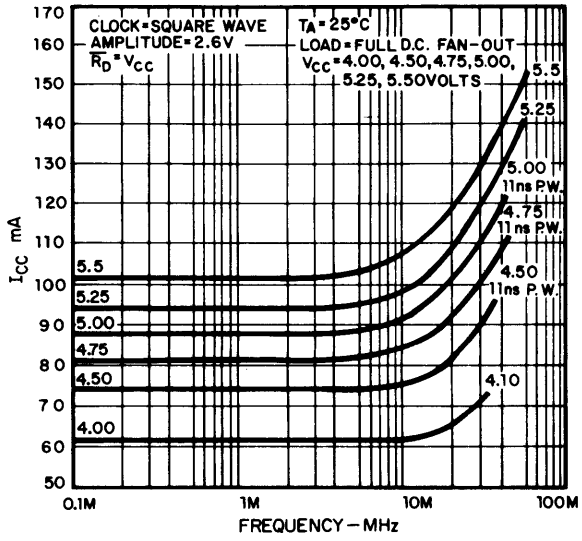
Curve 4-3. I_{CC} vs. Frequency for Negative- and Positive-Going Pulse for the 8202.



AC Characteristics of the 8200/8201/8202/8203

CURVE 4-2 and CURVE 4-3 Shows the typical clock pulse width vs. frequency for both positive- and negative-going clock pulses. Typically, a 17ns negative-going clock pulse width is required to clock the device as opposed to a 9ns positive-going clock pulse. By using a negative-going 20ns clock pulse (normally "1") as opposed to using a positive-going 20ns clock pulse (normally "0"), a typical power saving of 55mW may be realized as shown in Curve 4-3. The 50% duty cycle clock is also shown on this curve.

Curve 4-4. I_{CC} vs. Frequency for a Squarewave Clock for the 8202.



CURVE 4-4 Illustrates the typical I_{CC} vs. frequency for a squarewave CLOCK input, with all outputs fully loaded and an ambient temperature (T_A) of 25°C.

8275 QUADRUPLE BISTABLE LATCH

The 8275 is a quadruple gated latch. Each latch has the complementary outputs, Q and $\overline{Q}$, available. The Q output follows the D input while the STROBE or CLOCK input is high ("1") and retains the information which is present at the D input 20ns before the CLOCK goes low ("0"). Figure 4-5a shows the circuit diagram for the 8275. The equivalent logic diagram is illustrated in Figure 4-5b.

The strobe interval ("1") of 20ns will ensure that the information at the D input will be transferred and stored to the

outputs. Two CLOCK inputs are provided. Each CLOCK input is common to two latches. One CLOCK input appears as only two TTL input loads.

The V_{CC} to GROUND ceramic disc bypassing capacitor should be greater than 0.02μF because of the eight totem pole output structures of the 8275.

Maximum Capacitive Loading

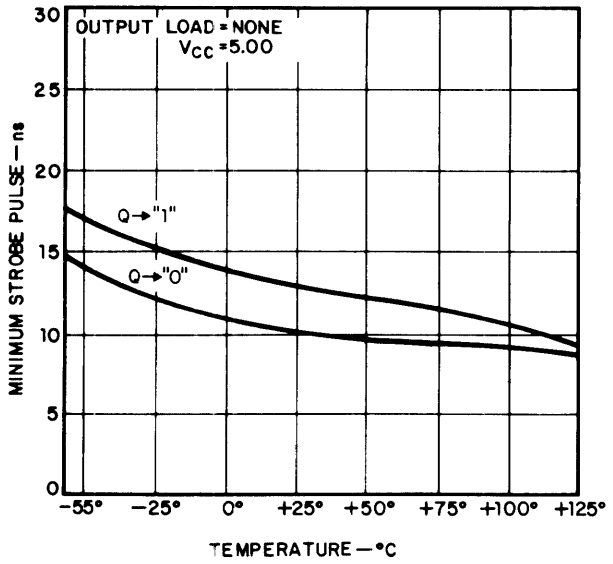
The unbuffered latch of the 8275 limits the amount of load capacitance to less than 300pF in very short strobe pulse applications. If the strobe is held high long enough for the device to latch, the only limitation to output capacitive loading is the desired rise and fall times.

AC Characteristics of the 8275

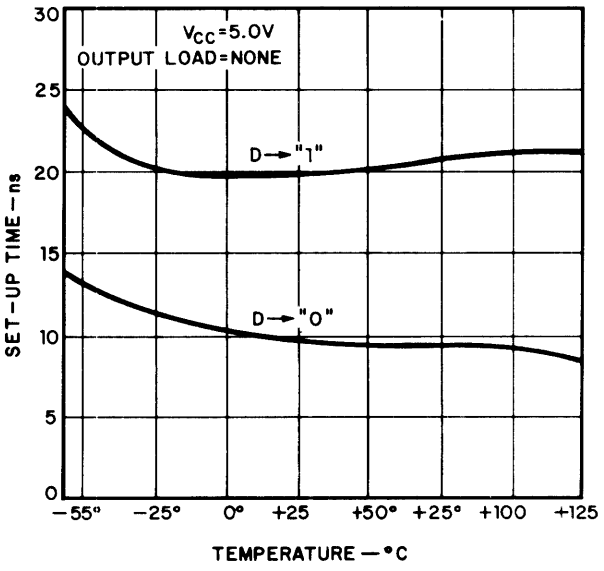
CURVE 4-5 Minimum strobe pulse vs. temperature (T_A) is the typical minimum strobe pulse width required to strobe a "1" (4-5a) or a "0" (4-5b) as a function of temperature.

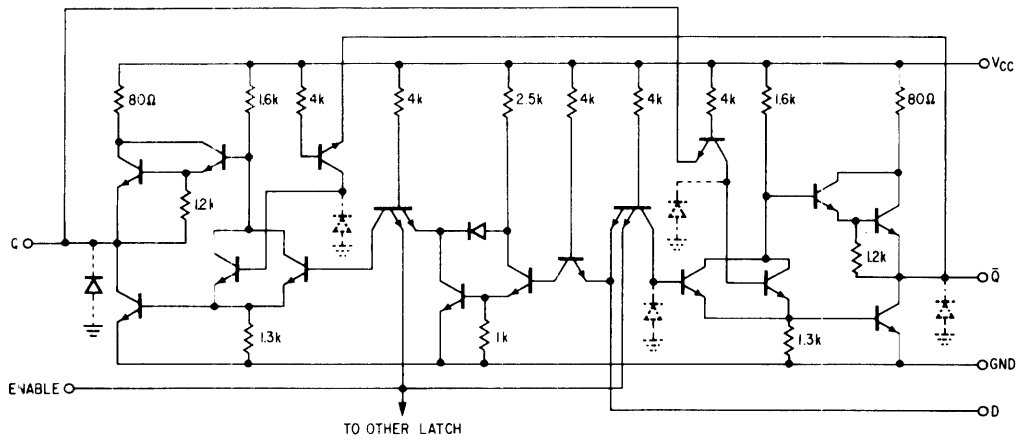
CURVE 4-6 D-input to strobe falling edge set-up time vs. temperature is the required time before the strobe falls that the D-input information must be present and stable as a function of ambient temperature and V_{CC} = 5.00V.

Curve 4-5



Curve 4-6





TRUTH TABLE (Each Latch)		
t_n	t_{n+1}	
D	Q	$\bar{Q}$
1	1	0
0	0	1

NOTES

1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

Figure 4-5a. Circuit Diagram for the 8275

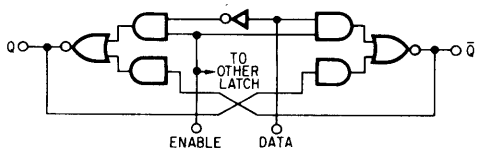


Figure 4-5b. Logic Diagram for the 8275

SHIFT REGISTER APPLICATIONS

Simple 8-Bit Right Shift Register

Let us assume first that the shift register flip-flops are reset to zero, applying a logic low to the $\bar{R}_D$ input. Now the first bit X_1, (X_1 = 1 or 0) using the series data input is shifted in the first flip-flop, A_{10}, by the first falling transition of the CLOCK signal. The second trigger pulse of the clock shifts the first bit X_1 to the second flip-flop B_{10}, and at the same time, the second bit X_2 is loaded in the first flip-flop A_{10}. To make it more clear, let us study an example with the series data (X_1, X_2, X_3, 0 0 0 . . . 0):

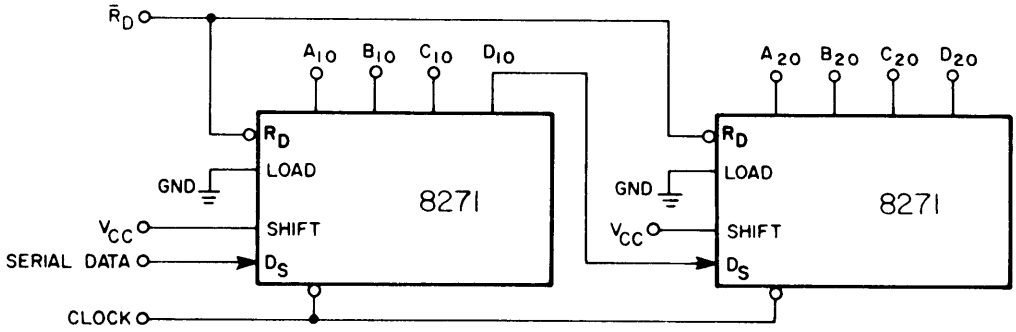


Figure 4-6. Simple 8-Bit Right Shift Register

CLOCK PULSE	STATE	SERIAL DATA (X_1 X_2 X_3 00...0)	FLIP-FLOP A_{10} B_{10} C_{10} D_{10} A_{20} B_{20} C_{20} D_{20}
		RESET	
→	0	X_1	0 0 0 0 0 0 0 0
→	1	X_2	X_1 0 0 0 0 0 0 0
	2	X_3	X_2 X_1 0 0 0 0 0 0
	3	0	X_3 X_2 X_1 0 0 0 0 0
	4	0	0 X_3 X_2 X_1 0 0 0 0
	5	0	0 0 X_3 X_2 X_1 0 0 0
	6	0	0 0 0 X_3 X_2 X_1 0 0
	7	0	0 0 0 0 X_3 X_2 X_1 0
	8	0	0 0 0 0 0 X_3 X_2 X_1
	9	0	0 0 0 0 0 0 X_3 X_2
	10	0	0 0 0 0 0 0 0 X_3
	11	0	0 0 0 0 0 0 0 0

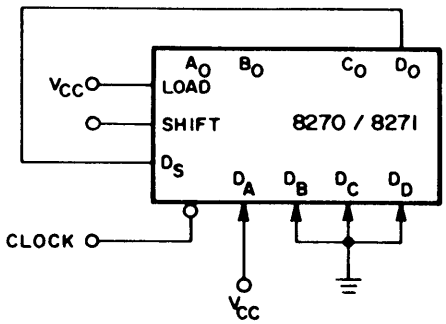
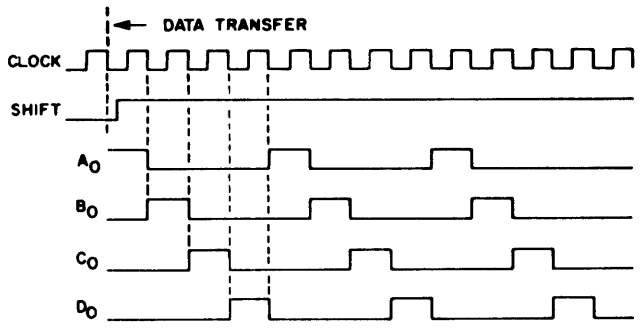


Figure 4-7. Ring Circuit

To demonstrate the parallel loading and serial shift operations, we intend to preload the shift register with the data (D_A, D_B, D_C, D_D) = (1, 0, 0, 0). Therefore, we apply a logic "1" to the pin D_A and a logic "0" to the pins D_B, D_C, D_D. A logic "0" at the control input SHIFT enables the falling clock signal to transfer the data (D_A, D_B, D_C, D_D) = (1, 0, 0, 0) to the shift register. To shift right now, the SHIFT input must stay on a logic "1" level permanently. The following diagram results:



A ring circuit is applied successfully if gating problems can be solved. A modified version of a ring circuit with self-correcting feature is shown below:

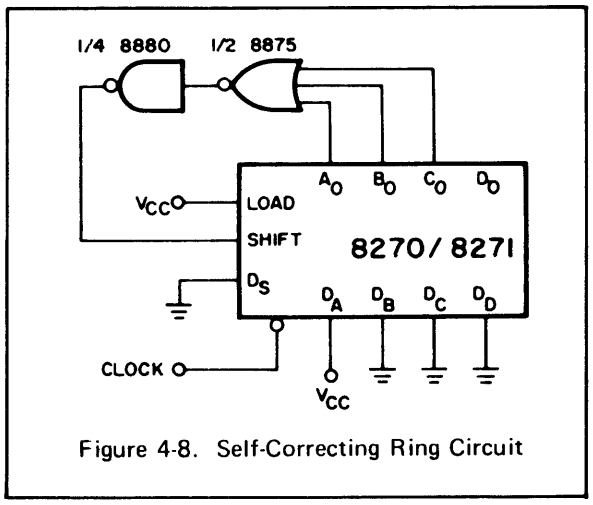


Figure 4-8. Self-Correcting Ring Circuit

We start with an arbitrary state (A, B, C, D) after maximum three shift pulses, we reach the state (0, 0, 0, A) and for this state, the SHIFT input is low. Thus, the word (1, 0, 0, 0) is preloaded by the next negative-going transition of the clock signal. The truth table for the ring circuit is given below:

1 0 0 0	preloaded data
0 1 0 0	
0 0 1 0	
0 0 0 1	feedback logic detects this state
1 0 0 0	preloaded data

Ring Counter

A ring counter built with an n-stage shift register counts through 2n states. For n = 4, the eight states are listed below:

STATE	A B C D	BCD	REMARK
1	1 1 1 1	15	FEEDBACK LOGIC DETECTS THIS STATE
2	0 1 1 1	7	PARALLEL LOADED DATA
3	0 0 1 1	3	
4	0 0 0 1	1	
5	0 0 0 0	0	
6	1 0 0 0	8	
7	1 1 0 0	12	
8	1 1 1 0	14	END OF PERIOD
1	1 1 1 1	15	

Note, another stable loop exists with the remaining unused states.

STATE	A B C D	BCD	REMARK
1	1 0 1 1	11	FEEDBACK LOGIC DETECTS THIS STATE
2	0 1 0 1	5	AND (0111) IS PRELOADED
3	0 0 1 0	2	
4	1 0 0 1	9	
5	0 1 0 0	4	
6	1 0 1 0	10	
7	1 1 0 1	13	
8	0 1 1 0	6	END OF PERIOD
1	1 0 1 1	11	

With an additional feedback loop, the ring counter will correct itself from stable loop conditions which exist in the unused states.

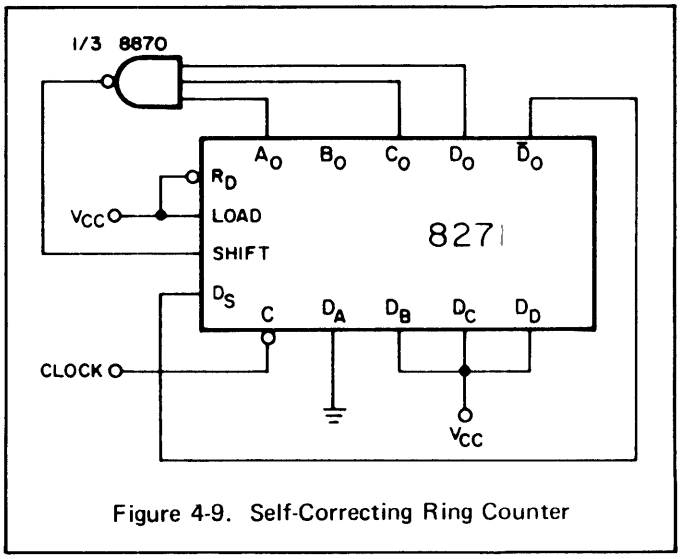


Figure 4-9. Self-Correcting Ring Counter

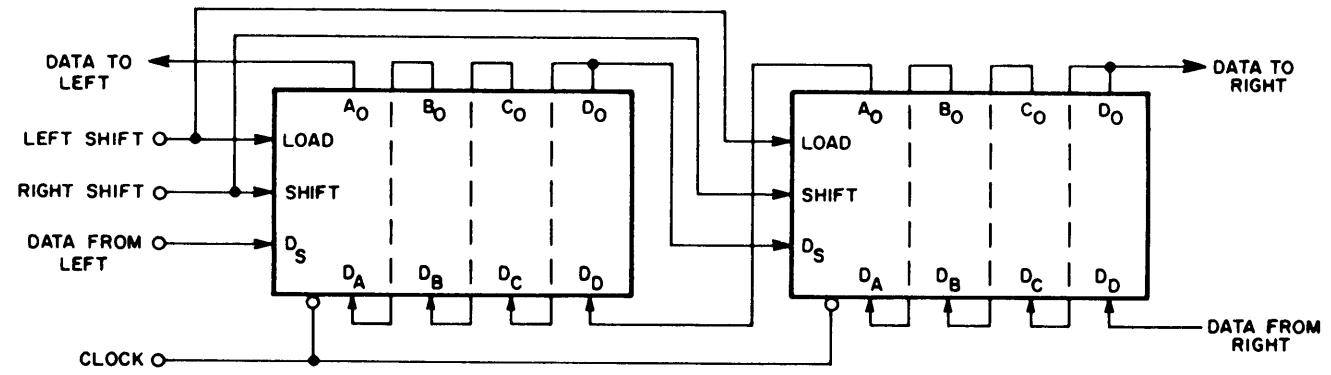


Figure 4-10. Left-Right Shift Registers (8270/8271)

The example shows an 8-bit serial entry, left-right shift application. Note, that a free-running clock can be applied.

LOAD	SHIFT	REMARK
0	0	Data Stored
0	1	Data Shifted Right
1	0	Data Shifted Left
1	1	Data Shifted Right

A left-right shift register with parallel entry is shown in the next example:

Variable 4-Bit Modulo N Counter ($2 \leqslant N \leqslant 15$)

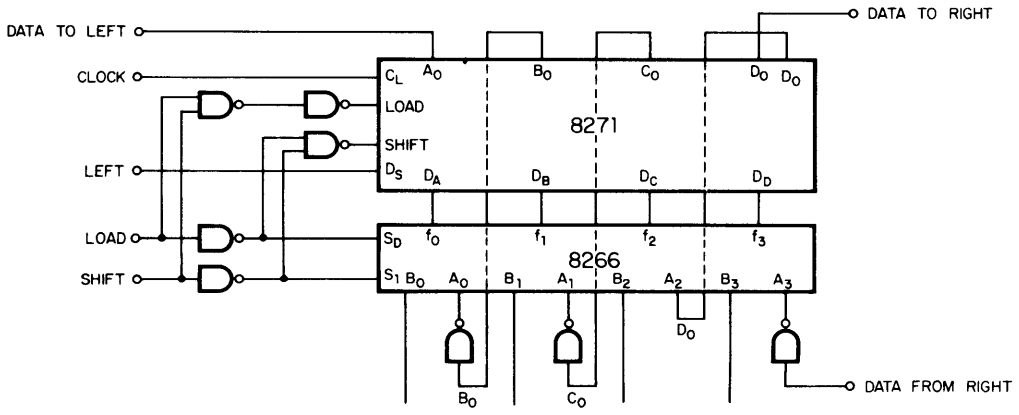
It is well-known that an n- stage binary shift register, when provided with suitably designed feedback paths, can count through 2^n-1 distinct states without any external input. For n = 4, there are two linear recurrences for a maximum period $p = 2^4-1 = 15$.

$$X_1 = A_O\bar{D}_O + \bar{A}_O D_O \qquad (\bar{X}_1 = \bar{A}_O\bar{D}_O + A_O D_O)$$

or

$$X_1 = C_O\bar{D}_O + \bar{C}_O D_O \qquad (\bar{X}_1 = \bar{C}_O\bar{D}_O + C_O D_O)$$

X_1: Generated bit, which is fed back to the first flip-flop.



LOAD	SHIFT	FUNCTION
0	0	Hold
0	1	Shift Left
1	0	Parallel Load
1	1	Shift Right

PACKAGE COUNT:
1 – 8271
1 – 8266
1 – 8H90
½ – 8H80

Figure 4-11. Shift-Right/Shift-Left/Parallel Entry Shift Register

As an example, we note the different states for the recurrence $\bar{X}_1 = \bar{C}_O\bar{D}_O + C_OD_O$, starting with $A_OB_OC_OD_O = (0\,1\,1\,1)$.

STATE	$\bar{X}_1 \equiv A_O\ B_O\ C_O\ D_O$	N
1	0 1 1 1	15
2	1 0 1 1	14
3	1 1 0 1	13
4	0 1 1 0	12
5	0 0 1 1	11
6	1 0 0 1	10
7	0 1 0 0	9
8	1 0 1 0	8
9	0 1 0 1	7
10	0 0 1 0	6
11	0 0 0 1	5
12	0 0 0 0	4
13	1 0 0 0	3
14	1 1 0 0	2
15	1 1 1 0	-
16≡1	0 1 1 1	

$\bar{C}_O\bar{D}_O + C_OD_O = 1 = \bar{X}_1$ FOR STATE 2

We note that only the state 1 1 1 1 is not generated. Starting with 1 1 1 1 and applying the rule $\bar{X}_1 = \bar{C}_O\bar{D}_O + C_OD_O$, the combination 1 1 1 1 will be generated once again. Therefore, it is obvious that the long period cannot include this state.

To implement a variable modulo N counter, we preload the shift register with the logic configuration $N = (A_OB_OC_OD_O)$ whenever the end of the period (1 1 1 0) is reached. (For N, see the truth table.)

The counter can be locked at the end of each period with the control input LOAD. Further, the counter has a self-correcting feature for all N, because every possible state leads back to the original period (truncated period for $2 \leqslant N \leqslant 14$). Note, that the special state (1 1 1 1) influences the shift input as well as the state (1 1 1 0).

Error-Correcting Code Generator

A 4-bit shift register with a feedback loop is preloaded with an arbitrary 4-bit number. The shift register feedback path is given by the equation

$$X_1 = A_O \oplus B_O \oplus D_O = Y \oplus D_O = Y\bar{D}_O + \bar{Y}D_O$$

and

$$Y = A_O \oplus B_O = A_O\bar{B}_O + \bar{A}_OB_O$$

The preloaded numbers are shifted seven times, generating the following output sequences.

	INPUT INFORMATION $A_O\ B_O\ C_O\ D_O$	OUTPUT CODEWORDS $b_1\ b_2\ b_3\ b_4\ b_5\ b_6\ b_7$
0	0 0 0 0	0 0 0 0 0 0 0
1	0 0 0 1	0 1 1 0 0 0 1
2	0 0 1 0	1 1 0 0 0 1 0
3	0 0 1 1	1 0 1 0 0 1 1
4	0 1 0 0	1 1 1 0 1 0 0
5	0 1 0 1	1 0 0 0 1 0 1
6	0 1 1 0	0 0 1 0 1 1 0
7	0 1 1 1	0 1 0 0 1 1 1
8	1 0 0 0	1 0 1 1 0 0 0
9	1 0 0 1	1 1 0 1 0 0 1
10	1 0 1 0	0 1 1 1 0 1 0
11	1 0 1 1	0 0 0 1 0 1 1
12	1 1 0 0	0 1 0 1 1 0 0
13	1 1 0 1	0 0 1 1 1 0 1
14	1 1 1 0	1 0 0 1 1 1 0
15	1 1 1 1	1 1 1 1 1 1 1

THE RELATIONS ARE

$b_1 = A_O \oplus B_O \oplus C_O$

$b_2 = B_O \oplus C_O \oplus D_O$

$b_3 = A_O \oplus B_O \oplus D_O$

$b_4 = A_O$

$b_5 = B_O$

$b_6 = C_O$

$b_7 = D_O$

The value of this procedure is that the set of sixteen codewords thus generated has the property that any two of them differ in at least three of their 7-bits. Further the additional bits $b_1b_2b_3$ enable to correct the code, if one but only one error occurs.

Additional gates 3/4 8880
1 8840

SHIFT = 0 preload the input information
SHIFT = 1 shift right

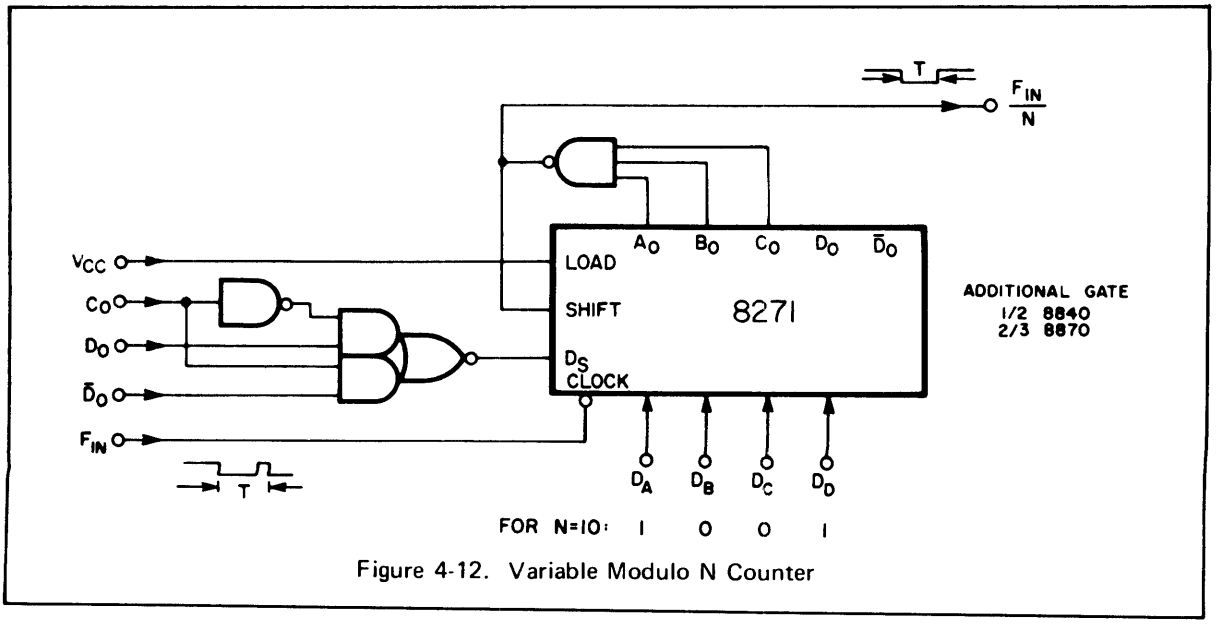


Figure 4-12. Variable Modulo N Counter

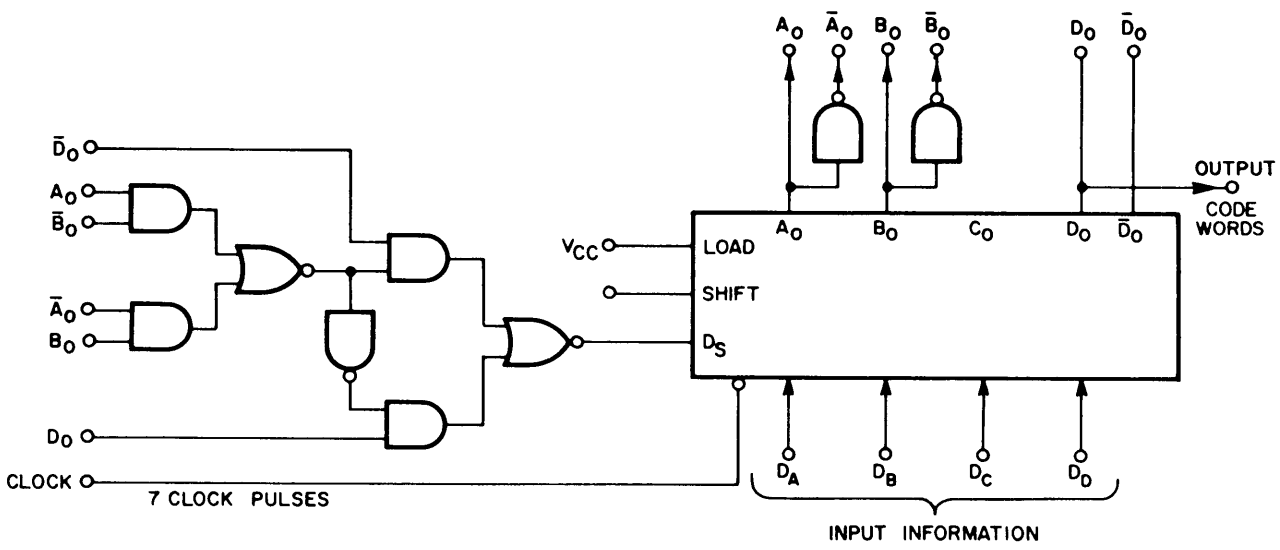


Figure 4-13. Self-Correcting Code Generator

To check and correct if necessary the received message, we form the sums

$$S_1, S_2, S_3$$

$$S_1 = b_2 + b_5 + b_6 + b_7$$

$$S_2 = b_1 + b_4 + b_5 + b_6$$

$$S_3 = b_3 + b_4 + b_5 + b_7$$

If each sum is even, no correction is necessary.

If, an an example, S_1 is odd, one of the bits b_2, b_5, b_6, b_7 is not correct. Assuming further the sum S_2 is also odd, only one of the bits b_5, b_6 being contained in S_1, as well as in S_2, can be incorrect. If the sum S_3 is even, the bit b_5 has the correct binary value implying b_6 is the erroneous bit. Assigning now the logic value Z = 1 if the corresponding sum is odd, and Z = 0 whenever the sum is even, we are able to construct a truth table for the erroneous bit.

Z_3	Z_2	Z_1	ERRONEOUS BIT	
0	0	1	b_2	
0	1	0	b_1	
1	0	0	b_3	
0	1	1	b_6	INFORMATION
1	0	1	b_7	
1	1	0	b_4	
1	1	1	b_5	

$$Z_1 = b_2 \oplus b_5 \oplus b_6 \oplus b_7$$

$$Z_2 = b_1 \oplus b_4 \oplus b_5 \oplus b_6$$

$$Z_3 = b_3 \oplus b_4 \oplus b_5 \oplus b_7$$

See reference [1], at the end of Appendix II.

PSEUDO-RANDOM SHIFT REGISTER SEQUENCES

Pseudo-Random Bit Sequences (PRBS) appear to be band-limited noise. However, since they are periodic, can be generated precisely and have reproducible pseudo-random noise spectra, PRBSs can provide significantly increased accuracy in time/distance measures and testing. By the use of a PRBS, JPL was able to achieve, to a high degree of accuracy, measurements of the distances from the Earth to Venus and the other planets through auto-correlation techniques.

Electronic equipment must function in an environment of random signal. The difficulty with random signals is that they are random and are very difficult to precisely generate repeatedly. Malfunctions of equipment in a random environment are nearly impossible to reproduce but can be very easily reproduced if a failure occurs during a pseudo-random sequence.

An example of a 15-state maximum length generator is shown in Figure 4-14. Table I of Appendix III shows the proper Exclusive-OR feedback for maximum length PRBS generates for n = 3 through n = 11 (where n is the number of bits in the shift register).

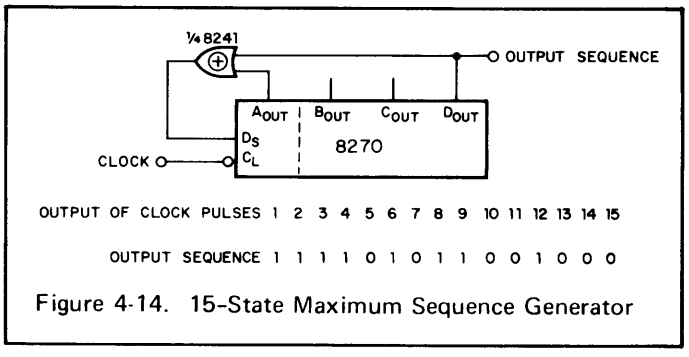
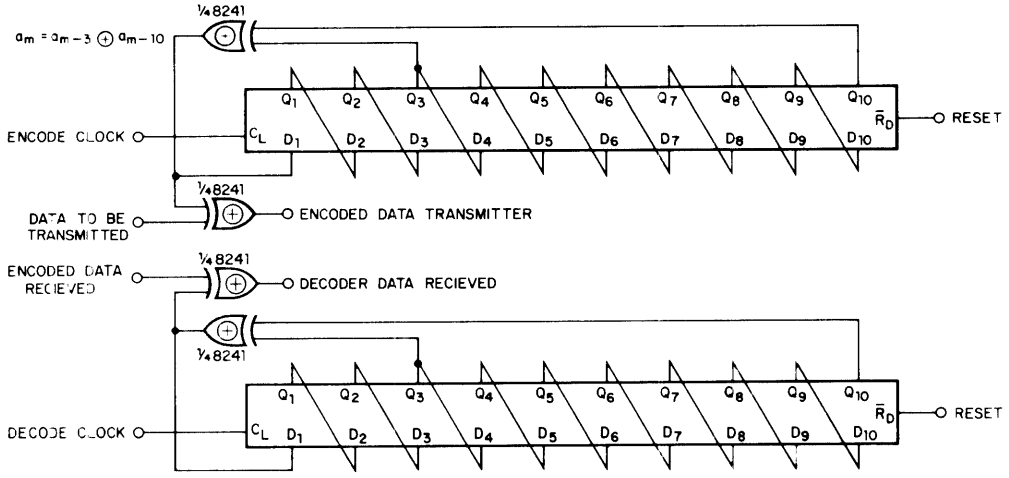


Figure 4-14. 15-State Maximum Sequence Generator

Figure 4-15 shows how a PRBS generator could be used to encode and decode data in a digital scrambling systems. In this as well as the preceding application there are 2^n-1 possible state. For systems (such as the ones shown) where Exclusive-ORs are used in the feedback loop and the true data both in and out of each binary is used, the only prohibited state occurs when all outputs are "0". A "0" into an Exclusive-OR gate gives a "0" perpetuating the all "0"s state. To prevent this condition, the outputs of Q_9 and Q_{10} could be inverted and all outputs (Q_1 through Q_9) could connect the OR gate tied to the RESET line. Then, when outputs Q_1 through Q_9 are "0", the shift register is reset, however, since Q_{10} is inverted, actually a "1" would be set into the tenth bit ($\overline{Q}_{10}$).



*The ENCODE CLOCK and DECODE CLOCK as well as the Pseudo-Random Sequence in both the Encoder and Decoder Shift Registers are synchronized. There are 2^n-1 or $2^{10}-1$ (1023) states which occur in a Pseudo-Random Binary Sequence.

Figure 4-15. Encoding/Decoding Digital Data

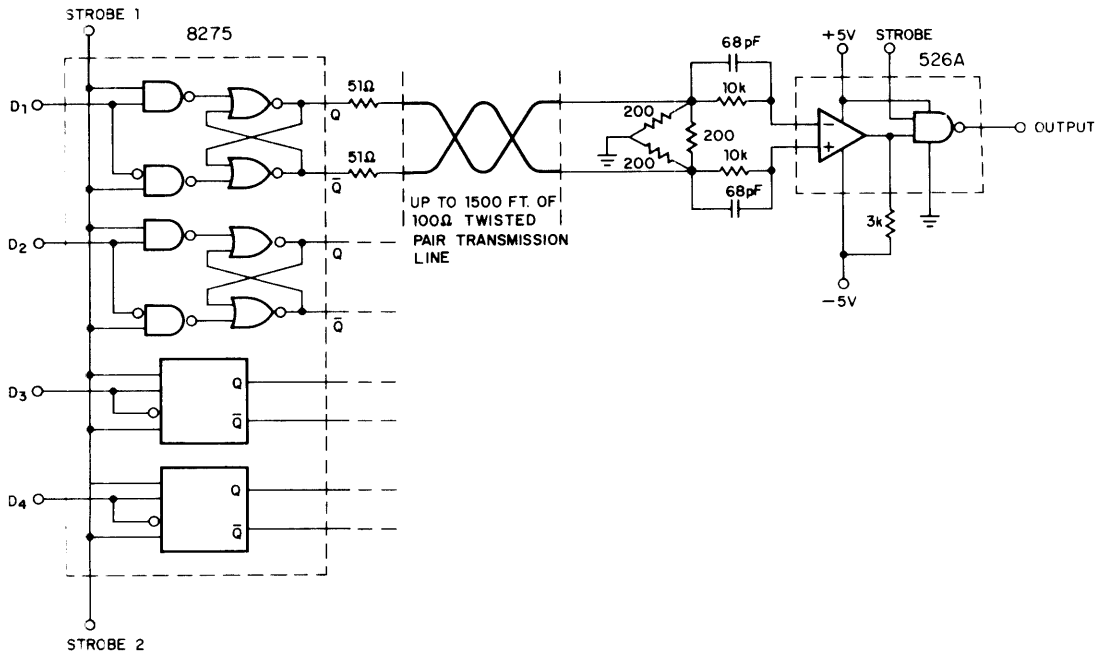


Figure 4-16. 20 MHz Quad Line Driver

APPENDIX I

CURRENT SPIKING

A TTL gate generates a current spike on the power supply bus (V_{CC}) during both switching transitions ("1" to "0" and "0" to "1"). During these switching transitions, both output transistors are conducting. The pull-down transistor of the totem pole structure has a finite constant current of 100mA for a typical 8800 gate. Figure A1-1 shows the "0" and "1" logic level output characteristic.

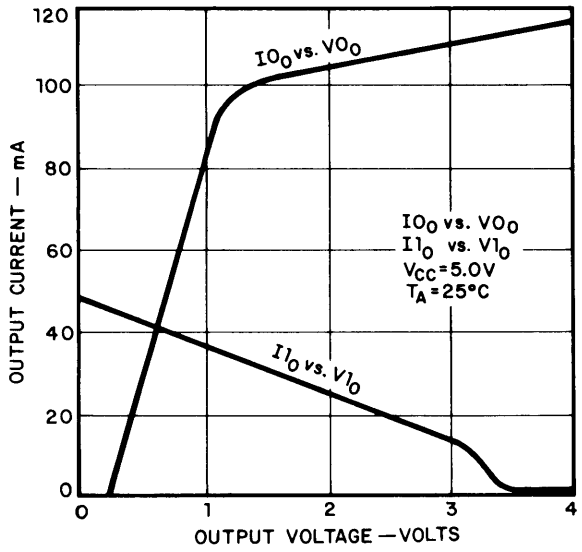


Figure A1-1. $I1_0$ vs. $V1_0$ and $I0_0$ vs. $V0_0$ for 8880

Figures A1-2 and A1-3 graphically illustrate the current spiking characteristics of an 8800 gate with a capacitive load.

As seen in Figure A1-2, during the negative-going transition, the capacitive load (C_L) current drives Q_1 into its constant current region. Since Q_1 cannot sink additional current, the current spike from V_{CC} through R_0 and Q_1 is minimized.

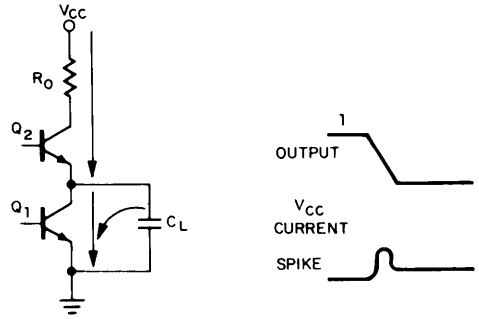


Figure A1-2. "1" to "0" Transition

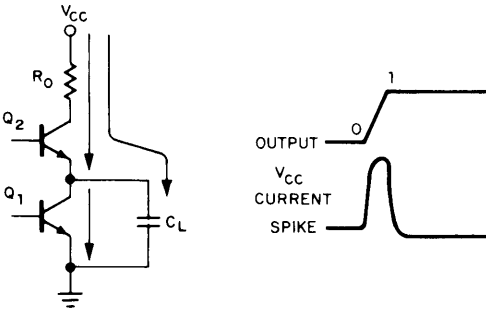


Figure A1-3. "0" to "1" Transition

The positive-going transition, Figure A1-3 generates a large V_{CC} current spike. As Q_1 begins to turn on, Q_2 is beginning to turn off and C_L initially appears to be a short to GROUND. This condition produces a V_{CC} current spike in excess of 40mA.

APPENDIX II

SHIFT REGISTER SEQUENCES

INTRODUCTION

A shift register is an arrangement of n flip-flops in a row and each flip-flop may have the binary value "0" or "1". Each flip-flop shifts its content to the next flip-flop when a clock pulse occurs. If no new "1" signals are introduced into the first flip-flop, after maximum of n-shift pulses, all flip-flops will have a logic zero output state. One way to keep the shift register active is to feedback the states of certain flip-flops into the first flip-flop.

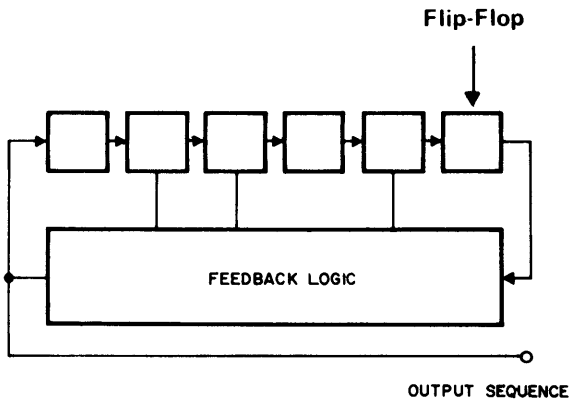


Figure A2-1. Feedback Shift Register

With suitably designed feedback paths, most useful binary sequences result. The purpose of this paper will be to present some interesting output sequences and their applications. The reader may find more literature in the references.

MAXIMUM LENGTH SEQUENCES

As we will show, every shift register with n flip-flops and a linear feedback logic has a period $p \leqslant 2^n-1$. Because each state of the shift register is completely determined by the previous one, a periodicity is established whenever a state is the same as some earlier state. Further, it is well-known that n flip-flops may represent a maximum of 2^n possible states. Now we introduce a linear recurrence for the feedback logic:

$$a_m = c_1\, a_{m-1} \oplus \ldots \oplus c_i\, a_{m-i} \oplus \ldots \oplus c_n\, a_{m-n} = S$$

$\oplus$ = Exclusive-OR

where:

a_m: new generated state, which is completely determined by the parity sum S.

$a_m = S = 1$ if S is odd, otherwise, $a_m = 0$

c_i = 1 when the state a_i of the particular flip-flop i is used in the feedback logic, otherwise $c_i = 0$.

If all n flip-flop outputs are zero, i.e., $a_{m-i} = 0$ for $1 \leqslant i \leqslant n$, then the linear recurrence always generates $a_m = 0$ and the periodicity is $p = 1$. Any sequence with $p > 1$ cannot include this state. Therefore, a non-trivial shift register sequence generator with a linear feedback logic has a period of $1 < p \leqslant 2^n-1$.

A maximum length linear sequence generator is a shift register with a suitably designed feedback which leads to a sequence with a period $p = 2^n-1$. The linear recurrences for maximum length sequences are tabulated in reference ([1]). Some examples are listed below. (n: number of flip-flops)

Table A2-1. MAXIMUM LENGTH SEQUENCES

n	LINEAR RECURRENCE	PERIOD
3	$a_m = a_{m-1} \oplus a_{m-3}$	7
4	$a_m = a_{m-1} \oplus a_{m-4}$	15
5	$a_m = a_{m-2} \oplus a_{m-5}$	31
6	$a_m = a_{m-1} \oplus a_{m-6}$	63
7	$a_m = a_{m-1} \oplus a_{m-7}$	127
8	$a_m = a_{m-1} \oplus a_{m-6} \oplus a_{m-7} \oplus a_{m-8}$	255
9	$a_m = a_{m-4} \oplus a_{m-9}$	511
10	$a_m = a_{m-3} \oplus a_{m-10}$	1,023
11	$a_m = a_{m-2} \oplus a_{m-11}$	2,047
12	$a_m = a_{m-2} \oplus a_{m-10} \oplus a_{m-11} \oplus a_{m-12}$	4,095
13	$a_m = a_{m-1} \oplus a_{m-11} \oplus a_{m-12} \oplus a_{m-13}$	8,191
14	$a_m = a_{m-2} \oplus a_{m-12} \oplus a_{m-13} \oplus a_{m-14}$	16,383
15	$a_m = a_{m-14} \oplus a_{m-15}$	32,767
16	$a_m = a_{m-11} \oplus a_{m-13} \oplus a_{m-14} \oplus a_{m-16}$	65,535
17	$a_m = a_{m-14} \oplus a_{m-17}$	131,071
18	$a_m = a_{m-11} \oplus a_{m-18}$	262,143
19	$a_m = a_{m-14} \oplus a_{m-17} \oplus a_{m-18} \oplus a_{m-19}$	524,287
20	$a_m = a_{m-17} \oplus a_{m-20}$	1,048,575

As an example, we will consider the sequence represented by:

$$a_m = a_{m-1} \oplus a_{m-4}$$

For the state a_0, which implies m = 0, we write:

$$a_0 = a_{-1} \oplus a_{-4}$$

Since all states except the all "0" are used, let's assume a starting state of:

$a_{-1} = a_{-2} = a_{-3} = 0$ and $a_{-4} = 1$

Table A2-2 shows the sequence for a 4-stage maximum length shift register.

Table A2-2. SEQUENCES FOR $(a_{m-1} \oplus a_{m-4})$

STATE m	a_m	a_{m-1}	a_{m-2}	a_{m-3}	a_{m-4}
0	1	0	0	0	1
1	1	1	0	0	0
2	1	1	1	0	0
3	1	1	1	1	0
4	0	1	1	1	1
5	1	0	1	1	1
6	0	1	0	1	1
7	1	0	1	0	1
8	1	1	0	1	0
9	0	1	1	0	1
10	0	0	1	1	0
11	1	0	0	1	1
12	0	1	0	0	1
13	0	0	1	0	0
14	0	0	0	1	0
15	1	0	0	0	1

To implement a maximum length sequence generator, we write:

$$a_0 = a_{-1} \oplus a_{-4}$$

To generate the sequence $S_A = (a_0, a_1, \ldots, a_{p-1})$, the data will be shifted by clock pulses. The initial state of the flip-flops may be arbitrary, the state (0, 0, 0,0) excluded.

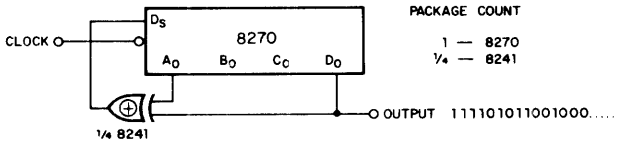


Figure A2-2. 15-State Maximum Length Sequence Generator

If the register starts in an all zero state, the feedback applies another zero to the serial input. Therefore, the same form of zero suppression must be used to keep the register out of the all zero state. Figure A2-3 shows a zero suppression that loads all "1"s whenever the all zero condition appears.

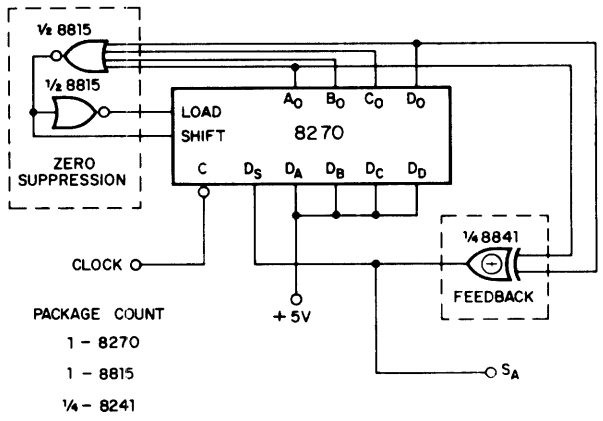


Figure A2-3. 15-State Maximum Length Sequence Generator with Zero Suppression

PSEUDO-RANDOM SEQUENCE GENERATORS

Now, we demonstrate an interesting feature of a maximum length generator; namely, a pseudo-random feature. For this purpose, we generate a longer sequence $S_A = (a_0, a_1, \ldots, a_m, \ldots, a_{p-1})$ with the recurrence:

$$a_m = (a_{m-1} \oplus a_{m-6})$$

and the period $p = 2^6-1 = 63$ with the conditions: $a_{-1} = \ldots = a_{-5} = 0$; $a_{-6} = 1$. The sequence S_A is listed below:

S_A = (1 1 1 1 1 1 0 1 0 1 0 1 1 0 0 1 1 0 1 1 1 1 0 1 1 0 1 0 0
1 0 0 1 1 1 0 0 0 1 0 1 1 1 1 0 0 1 0 1 0 0 0 1 1 0 0 0
0 1 0 0 0 0 0)

We form N = 63 different samples of 4-bits out of S_A: the first subset, starting with a_0: (1 1 1 1), (1 1 0 1), (0 1 0 1), . . . , the second subset, starting with a_1: (1 1 1 1), (1 0 1 0), (1 0 1 1),. . . the third subset, starting with a_2: (1 1 1 1), (0 1 0 1), (0 1 1 0), . . . and finally the fourth subset, starting with a_3: (1 1 1 0), (1 0 1 0), (1 1 0 0), . . . now an experimental frequency distribution of the number of 1s occurring in a sample of 4-bits is computed as follows:

$$p(i) = \frac{F(i)}{N} \qquad i = 0, 1, 2, 3, 4$$

where:

p(i): the statistical relative frequency of occurrence of i 1s in a sample of 4-bits.

N: the total number of samples of 4-bits

F(i): the number of occurrences of i 1s in a sample of 4-bits.

The result is listed in Table A2-3.

Table A2-3. OCCURRENCE OF "1"s.

i	F(i)	p(i)	b(i)
0	3	0.0476	0.0625
1	16	0.2540	0.2500
2	24	0.3810	0.3750
3	16	0.2540	0.2500
4	4	0.0635	0.0625

If the output of the generator were true-random noise, the probability of occurrence of "1"s in a sequence of 4-bits would be given by the binomial probability:

$$b(i) = \binom{4}{i}\left(\frac{1}{2}\right)^4 \qquad i = 0, 1, 2, 3, 4$$

which is also listed. To test the hypothesis that p(i) has a random feature, the experimental distribution is compared to a binomial distribution by using the chi-square function:

$$x^2 = \sum_{i=0}^{4} \frac{[F(i) - Nb(i)]^2}{Nb(i)} \quad \text{if } |F(i) - Nb(i)| < |[Nb(i)]^{2/3}|$$

Table A2-4. CHI-SQUARE FUNCTION PARAMETERS

i	F(i)	Nb(i)	d_i = F(i) - Nb(i)	$d_i^2/Nb(i)$
0	3	3.9375	-0.9375	0.2232
1	16	15.7500	+0.2500	0.0040
2	24	23.6250	+0.3750	0.0060
3	16	15.7500	+0.2500	0.0040
4	4	3.9375	+0.0625	0.0010
Sum	N = 63	63.0000	0.0000	x^2 = 0.2382

The maximum length sequence has a pseudo-random noise property. R. C. White[2] has investigated these features more in detail. He points out that a set of adjacent bits up to one shift register length (6-bits in our latest example) is, for practical purposes, a set of statistically independent variables. However, this is not true for larger sets. As the sample size increases beyond the shift register length, the approximation to the binomial distribution deteriorates. Thus, for applications with larger sample size, a corresponding larger shift register must be used.

Assuming representative 4-bit samples of a true-random sequence, 99 out of 100 tests, according to statistic tables, would result a value of:

$$x^2 \geqslant 0.297$$

Therefore, there is no evidence against the hypothesis that the experimental distribution is binomial for samples size of 4-bits.

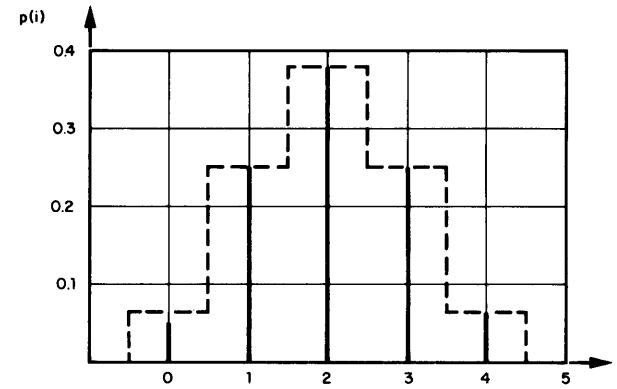


Figure A2-4. Distribution of 1's in 4-Bit Sample of a 6-Bit Pseudo-Random Sequence Generator

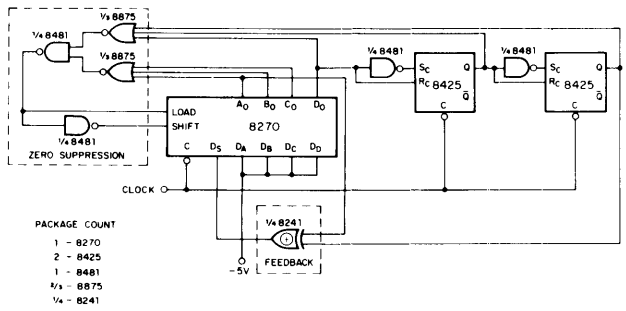


Figure A2-5. 6-Bit Pseudo-Random Sequence Generator with Zero Suppression

OUTPUT SEQUENCES WITH A KNOWN TIME PHASE

In many applications, it is useful to have an output with a known time phase relative to the normal output of the generator. As an example, we will consider the sequence represented by:

$$a_m = (a_{m-1} \oplus a_{m-3}) \quad \text{and } p = 7$$

We will generate the following relations

$$a_m = (a_{m-1} \oplus a_{m-3})$$

$$a_{m+1} = (a_m \oplus a_{m-2}) = (a_{m-1} \oplus a_{m-2} \oplus a_{m-3})$$

$$a_{m+2} = (a_{m+1} \oplus a_{m-1}) = (2a_{m-1} \oplus a_{m-2} \oplus a_{m+3}) = (a_{m-2} \oplus a_{m-3})$$

$$a_{m+3} = (a_{m+2} \oplus a_m) = (3a_{m-1} \oplus a_{m-2} \oplus 2a_{m-3}) = (a_{m-1} \oplus a_{m-2})$$

$$a_{m+4} = (a_{m+3} \oplus a_{m+1}) = (4a_{m-1} \oplus 2a_{m-2} \oplus 3a_{m-3}) = a_{m-3}$$

$$a_{m+5} = (a_{m+4} \oplus a_{m+2}) = (6a_{m-1} \oplus 3a_{m-2} \oplus 4a_{m-3}) = a_{m-2}$$

$a_{m+6} = (a_{m+5} \oplus a_{m+3}) = (9a_{m-1} \oplus 4a_{m-2} \oplus 6a_{m-3}) = a_{m-1}$

$a_{m+7} = (a_{m+6} \oplus a_{m+4}) = (13a_{m-1} \oplus 6a_{m-2} \oplus 9a_{m-3}) = (a_{m-1} \oplus a_{m-3})$

If we want a second output with a phase of three clock pulses, we will use:

$$a_m = (a_{m-1} \ominus a_{m-3})$$

as the feedback relation and

$$a_{m+3} = (a_{m-1} \oplus a_{m-2})$$

as the recurrence for the second output.

Table A2-5. EQUATION PARAMETERS.

STATE m	a_m	FLIP FLOP A	B	C	OUTPUT 1	OUTPUT 2
		a_{m-1}	a_{m-2}	a_{m-3}		
0	1	0	0	1	1	0
1	1	1	0	0	1	1
2	1	1	1	0	1	0
3	0	1	1	1	0	0
4	1	0	1	1	1	1
5	0	1	0	1	0	1
6	0	0	1	0	0	1
7	1	0	0	1	1	0

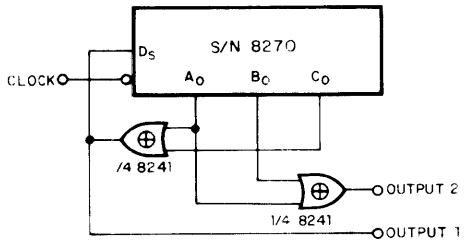


Figure A2-6. 7-State Maximum Length Sequence Generator with Second Output Leading First Output by 3 Counts

CODING AND DECODING OF A BINARY WORD

Using the pseudo-random feature of a long shift register sequence a binary word could be added, Modulo 2, to the output sequence, acting as the key. The decipherment consists of adding the same key, Modulo 2, to the encoded message using a second generator with the same synchronous sequence.

As an example, we will use the same sequence $S_A = (a_0, a_1, \ldots a_m, \ldots a_{p-1})$ $a_m = (a_{m-1} + a_{m-6})$ $(p = 63)$ as introduced earlier.

Table A2-6. ENCODING AND DECODING.

S_A	MESSAGE: M_1		ENCODED MESSAGE $C = (S_A + M_1)$ Mod 2		DECODED MESSAGE $M_2 = (C + S_A)$ Mod 2	
1	0		1		0	
1	1	4	0	11	1	4
1	0		1		0	
1	0		1		0	
1	0		1		0	
1	0	2	1	15	0	2
0	1		1		1	
1	0		1		0	
0	0		0		0	
1	0	1	1	4	0	1
0	0		0		0	
1	1		0		1	
0	0	8	0	1	0	8
0	0		0		0	
1	0		1		0	
0	0	3	0	8	0	3
1	1		0		1	
1	0		1		0	
0	1	5	1	14	1	5
1	0		1		0	
0	0		0		0	
1	0	0	1	4	0	0
0	0		0		0	
0	0		0		0	

The relations are:

$$M_2 = (C \oplus S_A) = C\bar{S}_A + \bar{C}S_A = C \oplus S_A$$

$$C = (S_A \oplus M_1) = S_A \oplus M_1$$

$$M_2 = C \oplus S_A = S_A \oplus M_1 \oplus S_A = (S_A \oplus S_A) \oplus M_1 = (S_A \bar{S}_A + \bar{S}_A S_A) \oplus M_1 = 0 \oplus M_1 = 0\bar{M}_1 + 1M_1 = M_1$$

Hence $M_2 = M_1$

where M_1: Transmitted, binary sequence

M_2: Received, binary sequence

For practical purpose a much longer shift register sequence would result to a more powerful encipherment.

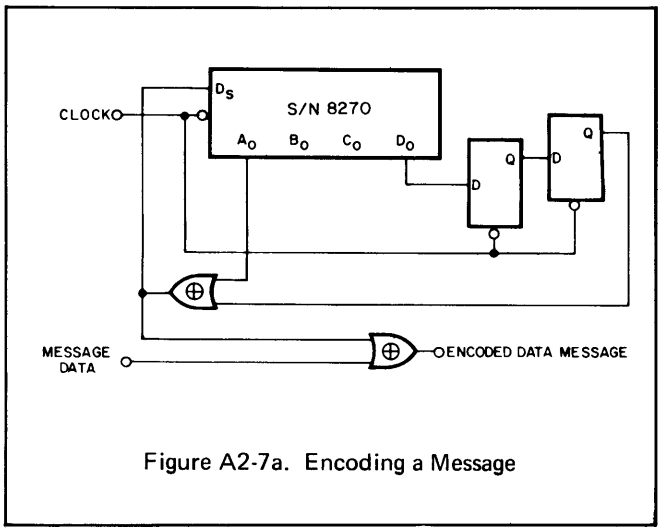


Figure A2-7a. Encoding a Message

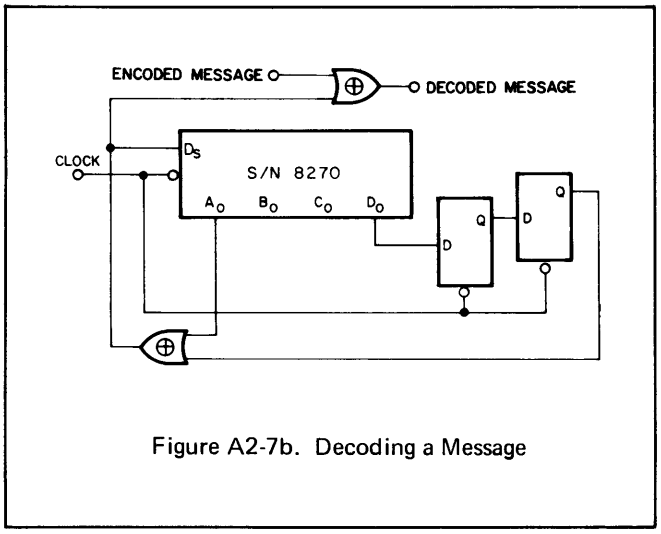


Figure A2-7b. Decoding a Message

Both sequence generators used in encoding and decoding must have the same sequence and they must also be in phase.

ERROR-CORRECTING CODE GENERATOR

A 4-bit shift register with a feedback loop is preloaded with an arbitrary 4-bit number. The shift register feedback path is given by the equation:

$$a_0 = (a_{-1} \oplus a_{-2} \oplus a_{-4}) =$$

$$a_{-1} \oplus a_{-2} \oplus a_{-4} = Y \oplus a_{-4} = Y\bar{a}_{-4} + \bar{Y}a_{-4}$$

$$\text{and } Y = a_{-1} \oplus a_{-2} = a_{-1}\,\bar{a}_{-2} + \bar{a}_{-1}\,a_{-2}$$

which is not a maximum length recurrence. The preloaded numbers are shifted seven times, generating the following output sequences:

Table A2-7. ERROR-CORRECTING CODE.

BCD NUMBER	INPUT INFORMATION A a_{-1}	B a_{-2}	C a_{-3}	D a_{-4}	OUTPUT CODEWORDS b_1	b_2	b_3	b_4	b_5	b_6	b_7
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	1	0	0	0	1
2	0	0	1	0	1	1	0	0	0	1	0
3	0	0	1	1	1	0	1	0	0	1	1
4	0	1	0	0	1	1	1	0	1	0	0
5	0	1	0	1	1	0	0	0	1	0	1
6	0	1	1	0	0	0	1	0	1	1	0
7	0	1	1	1	0	1	0	0	1	1	1
8	1	0	0	0	1	0	1	1	0	0	0
9	1	0	0	1	1	1	0	1	0	0	1
10	1	0	1	0	0	1	1	1	0	1	0
11	1	0	1	1	0	0	0	1	0	1	1
12	1	1	0	0	0	1	0	1	1	0	0
13	1	1	0	1	0	0	1	1	1	0	1
14	1	1	1	0	1	0	0	1	1	1	0
15	1	1	1	1	1	1	1	1	1	1	1

with the substitution $a_{-1} = A$; $a_{-2} = B$; $a_{-3} = C$; $a_{-4} = D$; the relations are:

$b_1 = A \oplus B \oplus C$ $\qquad$ $b_5 = B$

$b_2 = B \oplus C \oplus D$ $\qquad$ $b_6 = C$

$b_3 = A \oplus B \oplus D$ $\qquad$ $b_7 = D$

$b_4 = A$

The value of this procedure is that the set of 16 codewords thus generated has the property that any two of them differ in, at least, three of their seven bits. Further, the additional bits, b_1 b_2 b_3, enable one to correct the code, if one but only one error occurs.

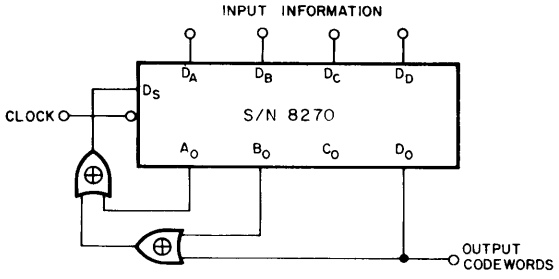


Figure A2-8. Error-Correcting Code Generator

To check and correct, if necessary, the received message, we for the terms Z_1, Z_2, Z_3:

$$Z_1 = b_2 \oplus b_5 \oplus b_6 \oplus b_7$$
$$Z_2 = b_1 \oplus b_4 \oplus b_5 \oplus b_6$$
$$Z_3 = b_3 \oplus b_4 \oplus b_5 \oplus b_7$$

If $Z_1 = Z_2 = Z_3 = 0$, no correction is necessary because the previous relations are still valid:

$$Z_1 = b_2 \oplus b_5 \oplus b_6 \oplus b_7 = (B \oplus C \oplus D) \oplus B \oplus C \oplus D = 0$$
$$Z_2 = b_1 \oplus b_4 \oplus b_5 \oplus b_6 = (A \oplus B \oplus C) \oplus A \oplus B \oplus C = 0$$
$$Z_3 = b_3 \oplus b_4 \oplus b_5 \oplus b_7 = (A \oplus B \oplus D) \oplus A \oplus B \oplus D = 0$$

If, however, as an example $Z_1 = 1$, one of the bits, b_2, b_5, b_6, b_7, is not correct. Assuming further $Z_2 = 1$, only one of the bits b_5, b_6, being contained in Z_1 as well as in Z_2, can be incorrect. If $Z_3 = 0$, b_5 has the correct binary value implying b_6 is the erroneous bit. Therefore, we are able to construct a truth table for the erroneous bit.

Z_3	Z_2	Z_1	Erroneous Bit	
0	0	0	–	
0	0	1	b_2	
0	1	0	b_1	
1	0	0	b_3	
0	1	1	b_6	
1	0	1	b_7	Information
1	1	0	b_4	
1	1	1	b_5	

If once the erroneous bit is detected, we are able to correct it by inverting the previous binary value.

VARIABLE COUNT SHIFT REGISTERS

Up to now we have discussed only maximum length sequence generators. If we detect the all "1"s condition and parallel enter a particular word, the length of the sequence can be shortened. Figure A2-9 shows an example of this using a 4-bit shift register.

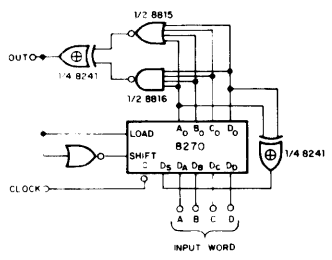


Figure A2-9. 2 to 15 Variable Frequency Divider

The sequence formed by a 4-bit register is 1 1 1 1 0 1 0 1 1 0 0 1 0 0 0. Table A2-8 shows the input code required for frequency divisions from 2 to 15.

Table A2-8. DIVISION AVAILABLE IN 4-BIT SHIFT REGISTER

INPUT CODE					INPUT CODE				
A	B	C	D	Division	A	B	C	D	Division
1	1	1	0	2	0	0	1	1	9
1	1	0	0	3	0	1	1	0	10
1	0	0	0	4	1	1	0	1	11
0	0	0	1	5	1	0	1	0	12
0	0	1	0	6	0	1	0	1	13
0	1	0	0	7	1	0	1	1	14
1	0	0	1	8	0	1	1	1	15

We see from Table A2-8 that four outputs must be fed back to form a maximum length sequence generator. Figure A2-10 shows two 8270s connected as a variable frequency divider from 2 to 255.

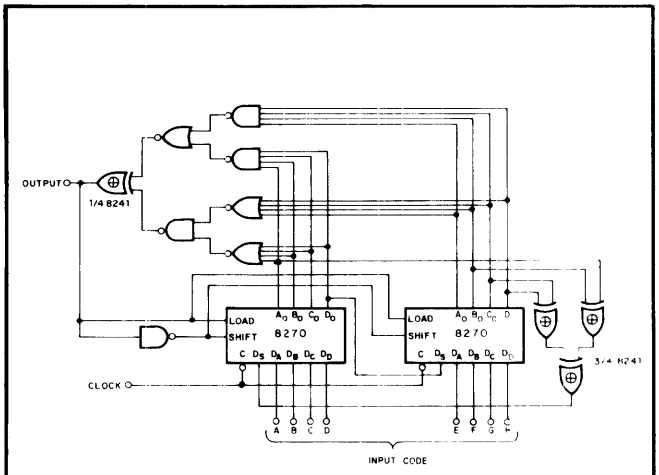


Figure A2-10. 2 to 255 Variable Frequency Divider

The required input code for a particular frequency division is shown in Table A2-9.

Table A2-9. 8-BIT SHIFT REGISTER FREQUENCY DIVIDER CODES

A	B	C	D	E	F	G	H	DIVISION	A	B	C	D	E	F	G	H	DIVISION
1	1	1	1	1	1	1	0	2	0	1	1	0	0	1	1	0	59
1	1	1	1	1	1	0	1	3	1	1	0	0	1	1	0	0	60
1	1	1	1	1	0	1	0	4	1	0	0	1	1	0	0	0	61
1	1	1	1	0	1	0	1	5	0	0	1	1	0	0	0	1	62
1	1	1	0	1	0	1	0	6	0	1	1	0	0	0	1	0	63
1	1	0	1	0	1	0	1	7	1	1	0	0	0	1	0	0	64
1	0	1	0	1	0	1	1	8	1	0	0	0	1	0	0	0	65
0	1	0	1	0	1	1	1	9	0	0	0	1	0	0	0	1	66
1	0	1	0	1	1	1	0	10	0	0	1	0	0	0	1	1	67
0	1	0	1	1	1	0	0	11	0	1	0	0	0	1	1	0	68
1	0	1	1	1	0	0	1	12	1	0	0	0	1	1	0	1	69
0	1	1	1	0	0	1	1	13	0	0	0	1	1	0	1	0	70
1	1	1	0	0	1	1	1	14	0	0	1	1	0	1	0	0	71
1	1	0	0	1	1	1	0	15	0	1	1	0	1	0	0	1	72
1	0	0	1	1	1	0	0	16	1	1	0	1	0	0	1	1	73
0	0	1	1	1	0	0	1	17	1	0	1	0	0	1	1	1	74
0	1	1	1	0	0	1	0	18	0	1	0	0	1	1	1	1	75
1	1	1	0	0	1	0	0	19	1	0	0	1	1	1	1	0	76
1	1	0	0	1	0	0	1	20	0	0	1	1	1	1	0	1	77
1	0	0	1	0	0	1	1	21	0	1	1	1	1	0	1	0	78
0	0	1	0	0	1	1	0	22	1	1	1	1	0	1	0	0	79
0	1	0	0	1	1	0	1	23	1	1	1	0	1	0	0	1	80
1	0	0	1	1	0	1	0	24	1	1	0	1	0	0	1	0	81
0	0	1	1	0	1	0	1	25	1	0	1	0	0	1	0	0	82
0	1	1	0	1	0	1	0	26	0	1	0	0	1	0	0	0	83
1	1	0	1	0	1	0	0	27	1	0	0	1	0	0	0	1	84
1	0	1	0	1	0	0	0	28	0	0	1	0	0	0	1	0	85
0	1	0	1	0	0	0	0	29	0	1	0	0	0	1	0	1	86
1	0	1	0	0	0	0	1	30	1	0	0	0	1	0	1	0	87
0	1	0	0	0	0	1	1	31	0	0	0	1	0	1	0	1	88
1	0	0	0	0	1	1	0	32	0	0	1	0	1	0	1	1	89
0	0	0	0	1	1	0	1	33	0	1	0	1	0	1	1	0	90
0	0	0	1	1	0	1	1	34	1	0	1	0	1	1	0	1	91
0	0	1	1	0	1	1	1	35	0	1	0	1	1	0	1	1	92
0	1	1	0	1	1	1	0	36	1	0	1	1	0	1	1	0	93
1	1	0	1	1	1	0	0	37	0	1	1	0	1	1	0	0	94
1	0	1	1	1	0	0	0	38	1	1	0	1	1	0	0	0	95
0	1	1	1	0	0	0	0	39	1	0	1	1	0	0	0	0	96
1	1	1	0	0	0	0	0	40	0	1	1	0	0	0	0	0	97
1	1	0	0	0	0	0	1	41	1	1	0	0	0	0	0	0	98
1	0	0	0	0	0	1	1	42	1	0	0	0	0	0	0	0	99
0	0	0	0	0	1	1	0	43	0	0	0	0	0	0	0	1	100
0	0	0	0	1	1	0	0	44	0	0	0	0	0	0	1	1	101
0	0	0	1	1	0	0	0	45	0	0	0	0	0	1	1	1	102
0	0	1	1	0	0	0	0	46	0	0	0	0	1	1	1	1	103
0	1	1	0	0	0	0	1	47	0	0	0	1	1	1	1	1	104
1	1	0	0	0	0	1	1	48	0	0	1	1	1	1	1	1	105
1	0	0	0	0	1	1	1	49	0	1	1	1	1	1	1	0	106
0	0	0	0	1	1	1	0	50	1	1	1	1	1	1	0	0	107
0	0	0	1	1	1	0	0	51	1	1	1	1	1	0	0	1	108
0	0	1	1	1	0	0	0	52	1	1	1	1	0	0	1	0	109
0	1	1	1	0	0	0	1	53	1	1	1	0	0	1	0	1	110
1	1	1	0	0	0	1	1	54	1	1	0	0	1	0	1	0	111
1	1	0	0	0	1	1	0	55	1	0	0	1	0	1	0	0	112
1	0	0	0	1	1	0	0	56	0	0	1	0	1	0	0	1	113
0	0	0	1	1	0	0	1	57	0	1	0	1	0	0	1	0	114
0	0	1	1	0	0	1	1	58	1	0	1	0	0	1	0	1	115

Table A2 9 8 BIT SHIFT REGISTER FREQUENCY DIVIDER CODES (Continued)

A	B	C	D	E	F	G	H	DIVISION	A	B	C	D	E	F	G	H	DIVISION
0	1	0	0	1	0	1	1	116	1	1	1	0	1	0	0	0	173
1	0	0	1	0	1	1	0	117	1	1	0	1	0	0	0	1	174
0	0	1	0	1	1	0	1	118	1	0	1	0	0	0	1	1	175
0	1	0	1	1	0	1	0	119	0	1	0	0	0	1	1	1	176
1	0	1	1	0	1	0	1	120	1	0	0	0	1	1	1	0	177
0	1	1	0	1	0	1	1	121	0	0	0	1	1	1	0	1	178
1	1	0	1	0	1	1	1	122	0	0	1	1	1	0	1	1	179
1	0	1	0	1	1	1	1	123	0	1	1	1	0	1	1	0	180
0	1	0	1	1	1	1	1	124	1	1	1	0	1	1	0	0	181
1	0	1	1	1	1	1	0	125	1	1	0	1	1	0	0	1	182
0	1	1	1	1	1	1	0	126	1	0	1	1	0	0	1	1	183
1	1	1	1	1	0	0	0	127	0	1	1	0	0	1	1	1	184
1	1	1	1	0	0	0	1	128	1	1	0	0	1	1	1	1	185
1	1	1	0	0	0	1	0	129	1	0	0	1	1	1	1	1	186
1	1	0	0	0	1	0	1	130	0	0	1	1	1	1	1	0	187
1	0	0	0	1	0	1	1	131	0	1	1	1	1	1	0	1	188
0	0	0	1	0	1	1	0	132	1	1	1	1	1	0	1	1	189
0	0	1	0	1	1	0	0	133	1	1	1	1	0	1	1	0	190
0	1	0	1	1	0	0	1	134	1	1	1	0	1	1	0	1	191
1	0	1	1	0	0	1	0	135	1	1	0	1	1	0	1	0	192
0	1	1	0	0	1	0	0	136	1	0	1	1	0	1	0	0	193
1	1	0	0	1	0	0	0	137	0	1	1	0	1	0	0	0	194
1	0	0	1	0	0	0	0	138	1	1	0	1	0	0	0	0	195
0	0	1	0	0	0	0	1	139	1	0	1	0	0	0	0	0	196
0	1	0	0	0	0	1	0	140	0	1	0	0	0	0	0	0	197
1	0	0	0	0	1	0	1	141	1	0	0	0	0	0	0	1	198
0	0	0	0	1	0	1	0	142	0	0	0	0	0	0	1	0	199
0	0	0	1	0	1	0	0	143	0	0	0	0	0	1	0	0	200
0	0	1	0	1	0	0	0	144	0	0	0	0	1	0	0	0	201
0	1	0	1	0	0	0	1	145	0	0	0	1	0	0	0	0	202
1	0	1	0	0	0	1	0	146	0	0	1	0	0	0	0	0	203
0	1	0	0	0	1	0	0	147	0	1	0	0	0	0	0	1	204
1	0	0	0	1	0	0	1	148	1	0	0	0	0	0	1	0	205
0	0	0	1	0	0	1	0	149	0	0	0	0	0	1	0	1	206
0	0	1	0	0	1	0	0	150	0	0	0	0	1	0	1	1	207
0	1	0	0	1	0	0	1	151	0	0	0	1	0	1	1	1	208
1	0	0	1	0	0	1	0	152	0	0	1	0	1	1	1	1	209
0	0	1	0	0	1	0	1	153	0	1	0	1	1	1	1	0	210
0	1	0	0	1	0	1	0	154	1	0	1	1	1	1	0	1	211
1	0	0	1	0	1	0	1	155	0	1	1	1	1	0	1	1	212
0	0	1	0	1	0	1	0	156	1	1	1	1	0	1	1	1	213
0	1	0	1	0	1	0	1	157	1	1	1	0	1	1	1	0	214
1	0	1	0	1	0	1	0	158	1	1	0	1	1	1	0	1	215
0	1	0	1	0	1	0	0	159	1	0	1	1	1	0	1	1	216
1	0	1	0	1	0	0	1	160	0	1	1	1	0	1	1	1	217
0	1	0	1	0	0	1	1	161	1	1	1	0	1	1	1	1	218
1	0	1	0	0	1	1	0	162	1	1	0	1	1	1	1	0	219
0	1	0	0	1	1	0	0	163	1	0	1	1	1	1	0	0	220
1	0	0	1	1	0	0	1	164	0	1	1	1	1	0	0	0	221
0	0	1	1	0	0	1	0	165	1	1	1	1	0	0	0	0	222
0	1	1	0	0	1	0	1	166	1	1	1	0	0	0	0	1	223
1	1	0	0	1	0	1	1	167	1	1	0	0	0	0	1	0	224
1	0	0	1	0	1	1	1	168	1	0	0	0	0	1	0	0	225
0	0	1	0	1	1	1	0	169	0	0	0	0	1	0	0	1	226
0	1	0	1	1	1	0	1	170	0	0	0	1	0	0	1	1	227
1	0	1	1	1	0	1	0	171	0	0	1	0	0	1	1	1	228
0	1	1	1	0	1	0	0	172	0	1	0	0	1	1	1	0	229

Table A2-9. 8-BIT SHIFT REGISTER FREQUENCY DIVIDER CODES (Continued)

A	B	C	D	E	F	G	H	DIVISION	A	B	C	D	E	F	G	H	DIVISION
1	0	0	1	1	1	0	1	230	0	1	1	1	1	0	0	1	243
0	0	1	1	1	0	1	0	231	1	1	1	1	0	0	1	1	244
0	1	1	1	0	1	0	1	232	1	1	1	0	0	1	1	0	245
1	1	1	0	1	0	1	1	233	1	1	0	0	1	1	0	1	246
1	1	0	1	0	1	1	0	234	1	0	0	1	1	0	1	1	247
1	0	1	0	1	1	0	0	235	0	0	1	1	0	1	1	0	248
0	1	0	1	1	0	0	0	236	0	1	1	0	1	1	0	1	249
1	0	1	1	0	0	0	1	237	1	1	0	1	1	0	1	1	250
0	1	1	0	0	0	1	1	238	1	0	1	1	0	1	1	1	251
1	1	0	0	0	1	1	1	239	0	1	1	0	1	1	1	1	252
1	0	0	0	1	1	1	1	240	1	1	0	1	1	1	1	1	253
0	0	0	1	1	1	1	0	241	1	0	1	1	1	1	1	1	254
0	0	1	1	1	1	0	0	242	0	1	1	1	1	1	1	1	255

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[1] Solomon W. Golomb, "Shift Register Sequences", Holden-Day, Inc. (San Francisco, Cambridge, London; 1967).

[2] R. C. White, Jr. "Experiments with Digital Computer Simulations of Pseudo-Random Noise Generators" IEEE Trans. on Electronic Computers (Short Notes) Vol. EC-16, pp. 355-357, June 1967.

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GLOSSARY

A

Abbreviations for Logic Forms:

CML:	Current – Mode – Logic
CTL:	Complementary – Transistor – Logic
DCL:	Designer's Choice Logic (SIGNETICS trademark)
DCTL:	Direct – Coupled – Transistor – Logic
DTL:	Diode – Transistor – Logic
ECL:	Emitter – Coupled – Logic
RCTL:	Resistor – Capacitor – Transistor – Logic
RTL:	Resistor – Transistor – Logic
TTL:	Transistor – Transistor – Logic
UTILOGIC:	Trademark for SIGNETICS-developed industrial logic form.

Access Time – Time required in a computer to move information from memory to the computing mechanism.

Accumulator – A register in an arithmetic unit for performance of arithmetical and logic functions such as addition and shifting.

Active Elements – Those components in a circuit which have gain or which direct current flow: diodes, transistors, SCR's, etc.

Adder – Switching circuits which combine binary bits to generate the sum and carry of these bits. Takes the bits from the two binary numbers to be added (ADDEND and AUGEND) plus the carry from the preceding less significant bit and generates the sum and the carry.

Address – Noun: a location, either name or number, where information is stored in a computer. Verb: to select or pick out the location or a stored information set for access.

Alphanumeric – A combination of alphabetic characters and digital numbers.

AND – A Boolean logic expression used to identify the logic operation wherein given two or more variables, all must be logical "1" for the result to be logical "1". The AND function is graphically represented by the dot (•) symbol. Example:

logic equation $A \cdot B \cdot C = D$

logic symbol

If A or B or C or all are ZERO, then D cannot be ONE (TRUE):

$\overline{A} + \overline{B} + \overline{C} = \overline{D}$

TRUTH TABLE

A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Anticipated Carry Adder – A parallel ADDER in which each stage is capable of looking back at all ADDEND and AUGEND bits of less significant stages and deciding whether the less significant bits provide a "0" or a "1" CARRY IN. Having determined the CARRY IN it combines it with its own ADDEND and AUGEND to give the SUM for that bit or stage. Also called FAST ADDER or look ahead CARRY ADDER.

Astable Multivibrator – An oscillator generally with complementary outputs; no trigger is necessary.

Asynchronous Inputs – Those terminals in a flip-flop which can affect the output state of the flip-flop independent of the CLOCK. Called SET, PRESET, RESET or DC SET and RESET, or CLEAR.

Asynchronous Operation – Generally an operation that is started by a completion signal from a previous operation. It then proceeds at the maximum speed of the circuits until finished and generates its own completion signal.

B

Bar – Used to symbolize the inverse, or complement, of a function. Example: Inversion of A is "$\overline{A}$", read "A bar" or "A not".

Binary Coded Decimal (BCD)– A binary numbering system for coding decimal numbers in groups of 4 bits. The binary value of these 4-bit groups ranges from 0000 to 1001 and codes the decimal digits "0" through 9. To count to 9 takes 4 bits; to count to 99 takes two groups of 4 bits; to count to 999 takes three groups of 4 bits. Examples:

Count Sequence for 8-4-2-1 BCD Code / 2-4-2-1 Code

	BCD Code	2-4-2-1 Code
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 0
3	0 0 1 1	0 0 1 1
4	0 1 0 0	1 0 1 0
5	0 1 0 1	1 0 1 1
6	0 1 1 0	1 1 0 0
7	0 1 1 1	1 1 0 1
8	1 0 0 0	1 1 1 0
9	1 0 0 1	1 1 1 1
0	0 0 0 0	0 0 0 0

Binary Logic – Digital logic elements which operate with two distinct states. The two states are variously called true and false, high and low, on and off, or "1" and "0". In computers they are represented by two different voltage levels. The level which is more positive (or less negative) than the other is called the high level, the other the low level. If the true ("1") level is the most positive voltage, such logic is referred to as positive true or positive logic.

Binary Number – Each digit of a binary number has only one of two possible states, which usually are called 0 and 1; each digit represents a number with the radix 2.

Example:

1 0 1 1 1 (binary)

$= 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$ (radix 2)

$= 16 + 0 + 4 + 2 + 1 = 23$

Bistable Element – Another name for flip-flop. A circuit in which the output has two stable states (output levels "0" or "1") and can be caused to go to either of these states by input signals, but remains in that state permanently after the input signals are removed. This differentiates the bistable element from a gate also having two output states but which requires the retention of the input signals to stay in a given state. The characteristic of two stable states also differentiates it from a monostable element which keeps returning to a specific state, and an astable element which keeps changing from one state to the other.

Bistable Multivibrator – A Flip-Flop, or Binary – A circuit with two stable states.

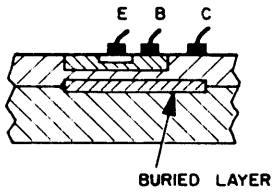
Bit – Binary Digit: The smallest part of information in a binary notation system. A bit is either a ONE or a ZERO.

Boolean Algebra – The mathematics of logic which uses alphabetic symbols to represent logical variables and "1" and "0" to represent states. There are three *basic* logic operations in this algebra: AND, OR and NOT. (Also see NAND, NOR, INVERT which are combinations of the three *basic* operations.)

Buffer – Usually an isolation stage between input and output of a digital circuit. Most of the Signetics flip-flops employ output buffering

- An intermediate storage device in a computer.
- Term sometimes used for a line driving element with high capacity loading capability and/or high fan-out.

Buried Layer – A layer of heavily doped material (high conductivity) under the collector region, generally applied to reduce the collector saturation resistance. This layer is diffused on the wafer before the epitaxial growth.



Buss (Line) – A common connection line for distribution of ground, power supply or signals.

Byte – An 8-bit grouping of bits. May contain two 4-bit characters or some other combinations of bit sub-grouping to facilitate information handling.

C

Carry – In the addition of two binary digits, a carry is generated when the sum exceeds the radix 2. Example:

0 plus 0 = 0
1 plus 0 = 1
0 plus 1 = 1
1 plus 1 = 0 with a carry of "1" to the next higher digit.

Character – A 4-bit decimal or 6-bit alpha-numeric code.

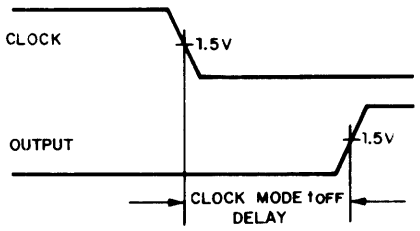
Chip (Die) – A single piece of silicon which has been cut from a slice by scribing and breaking. It can contain one or more circuits but is packaged as a unit.

Clear – Setting a number of memory elements or binaries to the ZERO state. Same as RESET.

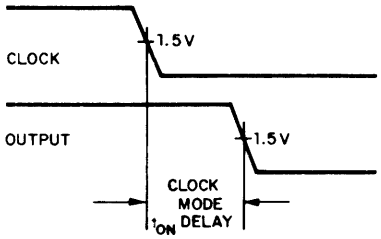
Clock – Basic timing device in a system, usually providing a continuous chain of timing pulses (clock pulses).

Clock Input – That terminal on a flip-flop whose condition or change of condition controls the admission of data into a flip-flop through the synchronous inputs and thereby controls the output state of the flip-flop. The clock signal performs two functions: (1) it permits data signals to enter the flip-flop; (2) after entry, it directs the flip-flop to change state accordingly. The J-K flip-flops permit data entry when the CLOCK goes to "1" and then causes the flip-flop to react to the data when the CLOCK goes to "0".

Clock Mode t_{off} Delay – The time interval between the 1.5V point of the clocking transition and the 1.5V point of the rising edge of the output of a toggle binary or counter.

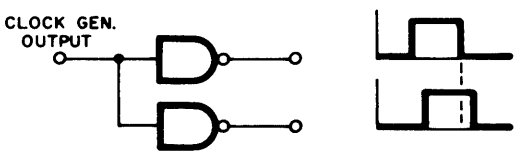


Clock Mode t_{on} Delay – The time interval between the 1.5V point of the clocking transition and the 1.5V point of the falling edge of the output of a toggle binary or counter.



Clock Mode Switching Test – This test is only pertinent to the capacitively coupled or stored charge binary elements and guarantees a maximum CLOCK input fall time for proper operation.

Clock Skew – A phase shift in a single clock distribution system. Can be introduced by different delays in clock driving elements and/or by distribution paths. Excessive skew will cause malfunction.



Clock Stagger – A term generally applied to the time separation between clock pulses in a multi-phase clock system. It may be applied to the voltage separation of the clock thresholds in a flip-flop such as the common DC-Clock Master-Slave devices.

CML (Current Mode Logic) – Logic in which transistors operate in the unsaturated mode as distinguished from most other logic types which operate in the saturation region. This logic has very fast switching speeds and low logic swings. Also called ECL or MECL.

Coder – A device for converting data from one notation system to another.

Collector Logic – See wired-AND.

Comparator – Digitally, an arrangement of gates that checks two signals or numbers for equality and usually indicates "equality", "less than", "greater than". The most common types indicate "equality" only. An analog comparator compares two input levels and indicates "less than" or "greater than".

Complement – The logical inversion of a Boolean function; see DeMorgan's theorem. Used to express negative numbers to facilitate subtraction.

Core Memory – Storage device consisting of ferromagnetic cores with provisions to enter data and to read data. A ferromagnetic core has two stable states which are used to store a binary digit.

Counter – A device capable of changing states in a specified sequence upon receiving appropriate input signals. The output of the counter indicates the number of pulses which have been applied. (See DIVIDER.) A counter is made from flip-flops and some gates. The output of all flip-flops are accessible to indicate the exact count at all times.

Counter, Binary – An interconnection of flip-flops having a single input so arranged to enable binary counting. Each time a pulse appears at the input, the counter changes state and tabulates the number of input pulses for readout in binary form. It has a 2^n possible counts where n is the number of flip-flops.

Counter, Ring – A special form of counter, sometimes called a Johnson or shift counter, which has very simple wiring and is fast. It forms a loop or circuits of interconnected flip-flops so arranged that only one is "0" and that, as input signals are received, the position of the "0" state moves in sequence from one flip-flop to another around the loop until they are all "0", then the first one goes to "1" and this moves in sequence from one flip-flop to another until all are "1". It has 2 x n possible counts where n is the number of flip-flops.

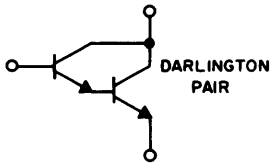
D

Data – Term used to denote facts, numbers, letters, symbols, binary bits presented as voltage levels in a computer. In a binary system, data can only be "0" or "1".

Data/Strobe t_{off} Delay – See Strobed Data t_{off} Delay.

Data/Strobe t_{on} Delay – See Strobed Data t_{on} Delay.

Darlington - Pair – Two transistors connected together according to figure below to obtain higher gain and higher input impedance.



Debugging – Act of checking system operation to identify malfunctions.

DeMorgan's Theorem – The theorem states that the inversion of a series of AND implications is equal to the same series of inverted OR implications, or the inversion of a series of OR implications is equal the same series of inverted AND implications.

$$\overline{A \cdot B \cdot D} = \bar{A} + \bar{B} + \bar{C} \qquad \overline{A + B + C} = \bar{A} \cdot \bar{B} \cdot \bar{C}$$

Decimal – A system of numerical representation which uses ten numerals 0, 1, 2, 3, . . . 9. Each numeral is called a digit. A numbering system to the radix 10.

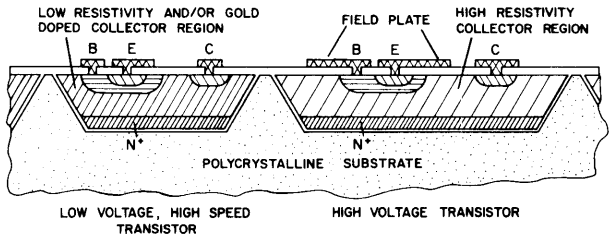
Delay – The slowing up of the propagation of a pulse either intentionally, such as to prevent inputs from changing while clock pulses are present, or unintentionally as caused by transistor rise and fall time pulse response effects.

Die (Dice) or Chip – Tiny silicon block containing one or more circuit components (such as transistors, diodes, resistors, capacitors). A die may contain several circuit functions (for example, quadruple gate).

Die Attach – Process of attaching by alloying the tiny silicon blocks to the mechanical support.

Die Sort – An electrical evaluation of the dice while in wafer form.

Dielectric Isolation – A process in which the individual components are separated through dielectric isolating layers (usually silicon dioxide).



Diffusion – A process used in the production of semiconductors which introduces minute amounts of impurities into a substrate material such as silicon or germanium and permits the impurity to spread into the substrate. The process is very dependent on temperature and time.

Digital Circuit – A circuit which operates in the manner of a switch, that is, it is either "on" or "off". More correctly should be called a binary circuit.

Discrete Circuits – Electronic circuits built of separate, individually manufactured, tested and assembled diodes, resistors, transistors, capacitors and other specific electronic components.

Divider (Frequency) – A counter which has a gating structure added which provides an output pulse after receiving a specified number of input pulses. The outputs of all flip-flops are not accessible.

Double Diffusion – See Isolation Diffusion.

Driver – An element which is coupled to the output stage of a circuit in order to increase its power or current handling capability or fan-out; for example, a clock driver is used to supply the current necessary for a clock line.

DTL (Diode-Transistor-Logic) – Logic employing diodes with transistors used only as inverting amplifiers.

E

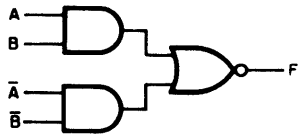
Enable – To permit an action or the acceptance or recognition of data by applying appropriate signals (generally a logic "1" in a positive logic) to the appropriate input. (See INHIBIT.)

Epitaxial Growth – A chemical reaction in which silicon is precipitated from a gaseous solution and grows in a very precise manner, that is, monocrystalline, upon the surface of a silicon wafer placed in the solution.

Excess Three Code – A self-complementing BCD code. Any 8-4-2-1 BCD code number might easily be transformed to an excess three number by adding a binary 3 (0011) to each number. If all zeros in a number are changed to ones and all ones to zeros, the nines complement of the number is obtained.

0	0	0	1	1	5	1	0	0	0
1	0	1	0	0	6	1	0	0	1
2	0	1	0	1	7	1	0	1	0
3	0	1	1	0	8	1	0	1	1
4	0	1	1	1	9	1	1	0	0

Exclusive-OR (A + B) – (1) The function, either one, but not both, or A not equal B. (2) A name frequently given to the AND-NOR circuit (for example, 8840) since they are ideally suited for forming the function.



$F = A\bar{B} + \bar{A}B$

Truth Table

A	B	F
0	0	0
1	0	1
0	1	1
1	1	0

Exclusive-NOR $\overline{(A + B)}$ – An inverted Exclusive-OR.

F

False – Statement for a ZERO in the Boolean algebra.

Fall Time – A measure of the time required for the output voltage of a circuit to change from a high voltage level to a low voltage level once a level change has started. Current could also be used as the reference, that is, from a high current to a low current level.

Fan-In – Total number of inputs of a particular gate or function.

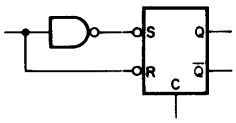
Fan-Out – The number of loads connected to the output of a gate or function.

Fast Adder – See Anticipated Carry and Adder.

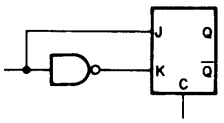
FEB (Functional Electronic Block) – Another name for a monolithic integrated circuit or thick film circuit.

Flip-Flop – A circuit with two and only two stable states.

D Flip-Flop – Delay binary, the output shows the input signal at the next clock pulse (one clock pulse delayed).



Derivation from RS

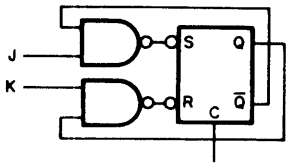


Derivation from J-K

Truth Table

D	Q_{n+1}
0	0
1	1

J-K Flip-Flop – Binary with synchronous set and reset inputs; all input combinations permitted. Note that first three entries for J-K and RS are the same.



Derivation from RS

Truth Table

J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

RS Flip-Flop – (See Latch.) Binary with set and reset inputs and the restriction that both inputs cannot be energized (0, for example, shown in truth table) simultaneously because the resultant state will be indeterminate.

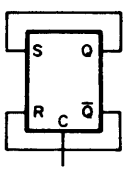
Q_{n+1} = Output state of the flip-flop one clock pulse (or one time increment) after the input combination appears.

Truth Table
SE125, SE424

S	R	Q_{n+1}
1	1	Q
0	1	1
1	0	0
0	0	?

"0" enables input

RST Flip-Flop – Binary with the feature of an RS and a T Flip-Flop.



RST Derivation from RS

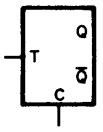
Truth Table

R^n	S^n	T^n	Q_{n+1}
0	0	0	Q^n
0	0	1	Q^n
0	1	0	1
1	0	0	0
0	1	1	?
1	0	1	?
1	1	0	?
1	1	1	?

? = indeterminate

RS/T Flip-Flop – An RS Flip-Flop which may be connected to operate in toggling mode. The SE124 and SE424 are of this type.

T Flip-Flop — Binary with a synchronous T-input; if T-input is high, flip-flop will toggle synchronously.



Truth Table

T^n	Q_{n+1}
0	Q^n
1	$\overline{Q}^n$

Full Adder — See Adder.

G

Gates (Decision Elements) — A circuit having two or more inputs and one output. The output depends upon the combination of logic signals at the input.

Gray Code — A binary code which is useful in input/output mechanisms (for example, shaft position encoders) because each number differs from the preceding one in one digit.

Example:	0000	0110
	0001	0100
	0011	0111
	0010	0101, etc.

H

Half-Adder — A switching circuit which combines binary bits to generate the SUM and the CARRY. It can only take in the two binary bits to be added and generate the SUM and CARRY (see Adder).

High — See Binary Logic.

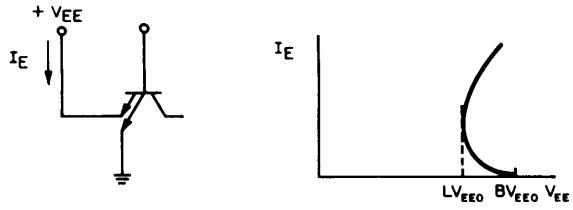
Holding Time — The period of time that the input states must remain after activation of the CLOCK input.

Hybrid — A mating of two or more technologies or techniques; for example: (1) A class of integrated circuits where two or more silicon chips are interconnected within the package. (2) A combination of the monolithic and thin film methods of manufacture.

I

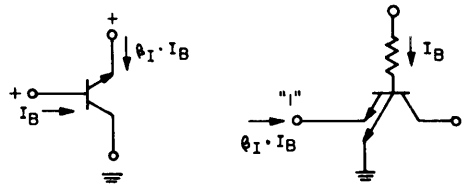
Inhibit — To prevent an action, acceptance of data by applying an appropriate signal to the appropriate input (generally a logic "0" in positive logic). (See Enable.)

Input Latch (LV_{EEO}) — Minimum voltage between two emitters (multiple emitter) after breakdown.



Integrated Circuit (EIA Definition) — "The physical realization of a number of electrical elements inseparably associated on or within a continuous body of semiconductor material to perform the functions of a circuit." (See definition for Slice and Chip.)

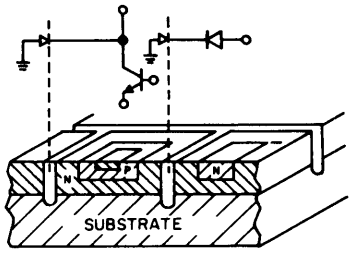
Inverse BETA — Resulting gain of a transistor when the emitter and collector loads are physically reversed in a circuit's operation.



Inverter — A device or circuit to complement a Boolean function (complement).

Buffer-Inverter AND Gate + Inverter

Isolation Diffusion — Technique to separate the individual components within the monolithic silicon n-structure. P-diffused isolation zones form the p-n junctions which act as reverse biased diodes.



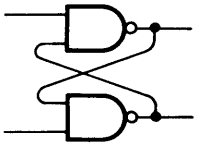
The transistors are double diffused; which means that the transistors are processed after the isolation diffusion by two diffusion steps.

Isolation Diode — p-n junctions, which surround all components, and act as biased diodes.

L

Latch — Usually a feedback loop in a symmetrical digital circuit (such as a flip-flop) for retaining a state.

A very simple RS flip-flop derived from two inverting gates:



Linear Circuit — A circuit whose output is an amplified version of its input, or whose output is a continuous predetermined variation of its input.

Logic Depth/Logic Levels – Generally the number of driven gates in a synchronous system between an output of a memory element binary and the enabling input of the next memory element binary. The maximum allowable logic depth is determined through the switching delays of the gates and the input/output delays of the memory element binaries.

Logic Diagram – A picture representation for the logical functions of AND, OR, NAND, NOR and NOT.

Logic Levels – One of two possible states, ZERO or ONE.

Definition: for positive logic: "UP" level = 1 TRUE
"DOWN" level = 0 FALSE
for negative logic: "DOWN" level = 1 TRUE
"UP" level = 0 FALSE

Logic Swing – The voltage difference between the two logic levels "1" and "0".

Low – See Binary Logic.

LSB (Least Significant Bit) – The lowest weighted digit of a binary number.

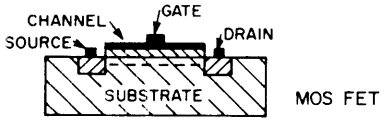
M

Master-Slave – A binary element containing two independent storage stages with a definite separation of the clock function to enter information to the master and to transfer it to the slave. For example, SU and LU320, SP620 and SE125J are master-slave flip-flops.

Monolithic – Elements or circuits formed within a single semiconductor substrate.

Monostable Multivibrator: One-Shot – A circuit with one stable state, and one quasi-stable state. When triggered, the monostable changes its state and falls back to the stable state after a certain time determined by its RC time constant.

MOS (Metal Oxide Semiconductor) – A field effect transistor whose gate is isolated from its channel through an oxide film. Also a capacitor formed by using similar techniques; semiconductor material forms one plate, metal (Al) the other plate, with oxide forming the dielectric.



MOS FET

Multiplex – Commutate: Sequentially connect a central unit or system to one of several channels.

MSB (Most Significant Bit) – The highest weighted digit of a binary number.

N

NAND – Logic implication that produces the inverted AND function.

$F = \overline{A \cdot B}$

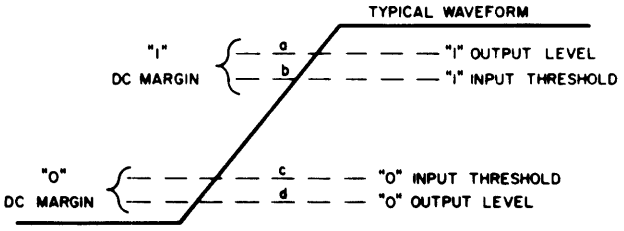
Truth Table

A	B	F
0	0	1
1	0	1
0	1	1
1	1	0

Negative Logic – Logic in which the more negative voltage represents the "1" state; the less negative voltage represents the "0" state. (See Binary Logic.)

Noise Immunity – A measure of the insensitivity of a logic circuit to triggering or reaction to spurious or undesirable electrical signals or noise, largely determined by the signal swing of the logic. Noise can be either of two directions, positive or negative. Noise immunity is high in both directions for SUHL.

Noise Margin (DCM) – The DC difference between the levels required at an input and available at an output. For example, in the figure below: "1" DCM = a - b
"0" DCM = c - d



NOR – Logic implication that produces the inverted OR function.

$F = \overline{A + B}$

Truth Table

A	B	F
0	0	1
1	0	0
0	1	0
1	1	0

NOT – A Boolean logic operation indicating negation, not "1". Actually an inverter. If input is "1" output is NOT "1" but "0". If the input is "0" output is NOT "0" but "1". Graphically represented by a bar over a Boolean symbol such as $\bar{A}$. $\bar{A}$ means "when A is not 1 . . ."

O

Octal Numbers – A system using numbers with the radix 8.

Offset – The change in input voltage required to produce a zero output voltage in a linear amplifier circuit. In digital circuits, it is the DC voltage on which a signal is impressed.

ONE ("1") – See Binary Logic.

One-Shot – See Monostable.

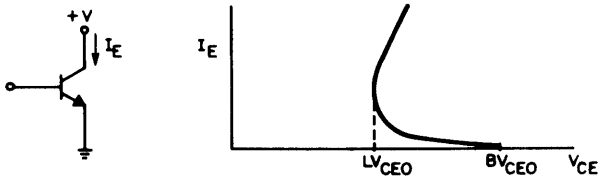
OR (Inclusive) – Logic implication that produces, at the output, a ONE if at least one input is ONE.

A + B = F

Truth Table

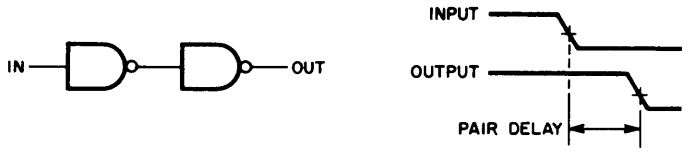
A	B	F
0	0	0
1	0	1
0	1	1
1	1	1

Output Latch (LV_{CEO}) – Minimum voltage after breakdown of collector-emitter.



P

Pair Delay — Propagation delay over two inverting stages.



Parallel — This refers to the technique for handling a binary data word which has more than one bit. All bits are acted upon simultaneously. It is like the line of a football team. Upon a signal, all line men act (see Serial).

Parallel Adder — A conventional technique for adding where the two multibit numbers are presented and added simultaneously (parallel). A ripple adder is still a parallel adder; the carry is rippled from the least significant to the most significant bit. Another type of parallel adder is the "Look Ahead", or "Anticipated Carry" adder. (See Ripple Adder and Fast Adder.)

Parallel Mode — The operation is performed for all binary digits simultaneously. For example, in a register, read-in and read-out occur simultaneously for all digits contained in the register. Usually parallel mode requires more equipment than series mode, but speeds up the operation.

Parallel Operation — The organization of data manipulation within computer circuitry where all the digits of a word are transmitted simultaneously on separate lines in order to speed up operation, as opposed to serial operation.

Parity Check — A simple kind of error-detecting scheme that requires an additional parity bit for each set of binary data. The binary set is always brought to an even (or odd) number of one digits with the parity bit before transfer operations and storage. The parity is tested after data transfers and storage read-outs to check for errors that may have occured during these operations.

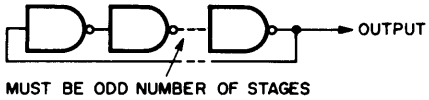
Passive Elements — Resistors, Inductors or capacitors, elements without gain.

Positive Logic — Logic in which the more positive voltage represents the "1" state; "1" = +3.45V, logic "0" = +0.45V. (See Binary Logic.)

Preset — An input like the SET input and which works in parallel with the SET.

Propagation Delay (t_{pd}) — Average propagation time per stage.

$$t_{pd} = \frac{1/\text{frequency}}{2 \times \text{no. stages}}$$



Propagation Time — The time necessary for a unit of binary information (high voltage or low) to be transmitted or passed from one physical point in a system or subsystem to another. For example, form input of a device to output.

Pull-Down Resistor — Generally a resistor connected to ground or a negative voltage; for example, from the base of a transistor to a negative voltage.

Pull-Up Resistor — Generally a resistor connected to the positive supply voltage. For example, from V_{CC} to the output collector (such as in SE180).

Pull-Up (Active) — A transistor replaces the pull-up resistor to effect low output impedance without high power consumption.

Q

Q Output — The reference output of a flip-flop. When this output is "1", the flip-flop is said to be in the "1" state; when it is "0", the output is said to be in the "0" state. (See State and Set.)

$\bar{Q}$ Output — The second output of a flip-flop. It is always opposite in logic level to the Q output.

R

Race — The condition that exists whenever a signal propagates through two or more memory elements during one clock period.

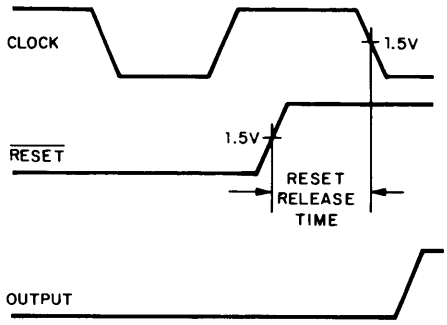
— A condition that occurs whenever changing the state of a system requires changing two or more state variables. If the final state is dependent upon which variable changes first, the condition is a critical race.

Register — A storage device for binary data generally used to store numbers for arithmetic operations or their result.

Reset — An input to a binary, counter or register which forces all binary elements to the zero logic state or the minimum binary state.

Reset Hold Time — The time required to completely reset a counter or register.

Reset Release Time — The interval of time required before a clocking transition will be recognized by a counter after the RESET input has been disabled.

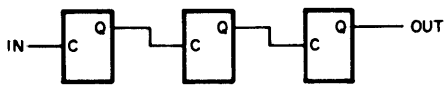


Ring Counter — A feedback shift register with only one stage in the ONE condition at any time. The shift register's output is fed back to the input to keep this single binary digit circulating. (See Twisted Ring Counter.)

Ripple — The transmission of data serially. It is a serial reaction analogous to a bucket brigade or a row of falling dominoes.

Ripple Adder — A binary adding system similar to the system most people use to add decimal numbers--that is, add the "units" column, get the carry, add it to the "10's" column, get the carry, add it to the "100's" column, and so on. Again, it is necessary to wait for the signal to propagate through all columns even though all columns are present at once (parallel). Note that the carry is rippled.

Ripple Counter – An asynchronously controlled counter; the clock is derived from an output of a previous stage.



Rise Time – A measure of the time required for the output voltage of a state from a low voltage level ("0") to a high voltage level ("1") once a level change has been started.

S

Scratch Pad Memory – Fast memory unit to store temporary data between operations in computers.

Serial – This refers to the technique for handling a binary data word which has more than one bit. The bits are acted upon one at a time. It is like a parade going by a review point.

Serial Mode – The operation is performed bit by bit, generally beginning with the least significant bit. Read-in and read-out occurs bit after bit by shifting the binary data through the register.

Serial Operation – The organization of data manipulation within computer circuitry where the digits of a word are transmitted one at a time along a single line. The serial mode of operation is slower than parallel operation, but utilizes less complex circuitry.

Set – An input to a binary, counter or register which forces all binaries to the maximum binary state.

Set-Up Time – The periods of time that logic levels must be presented at a binary's logic inputs before the CLOCK input may be activated.

Shift – The process of moving data from one place to another. Generally many bits are moved at once. Shifting is done synchronously and by command of the CLOCK. An 8-bit word can be shifted sequentially (serially)–that is, the 1st bit goes out, 2nd bit takes 1st bit's place, 3rd bit takes 2nd bit's place, and so on, in the manner of a bucket brigade. Generally referred to as shifting left or right. It takes 8 clock pulses to shift an 8-bit word or all bits of a word can be shifted simultaneously. This is called parallel load or parallel shift.

Shift Register – An arrangement of circuits, specifically flip-flops which is used to shift serially or in parallel. Binary words are generally parallel loaded and then held temporarily or serially shifted out.

Single-Rank Binary – A flip-flop which requires not more than one full clock pulse of a single clock system to transfer the logic from a synchronous input to the binary's output. Contains only one memory stage.

Sink Load – A load with a current flow out of its input. A sink load must be driven by a current sink.

Skewing – Refers to time delay or offset between any two signals in relation to each other.

Slewing Rate – Rate at which the output can be driven from limit to limit over the dynamic range.

Slice – A single wafer cut from a silicon ingot forming a thin substrate on which all active and passive elements for multiple integrated circuits have been fabricated utilizing semiconductor epitaxial growth, diffusion, passivation, masking, photo resist and metallization technologies. A completed slice generally contains hundreds of individual circuits. (See Chip.)

Source Load – A load with current flow into its input. A source load must be driven by a current source.

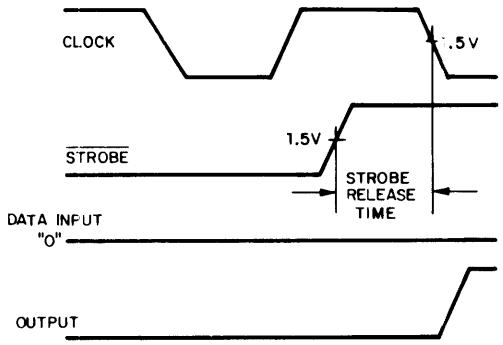
Standard Unit Load – Within each Signetics series, there is a standard load defined. Maximum fan-out is determined with this standard load or an equivalent circuit.

State – This refers to the condition of an input or output of a circuit as to whether it is a logic "1" or a logic "0". The state of a circuit (gate or flip-flop) refers to its output. The flip-flop is said to be in the "1" state when its Q output is "1". A gate is in the "1" state when its output is "1".

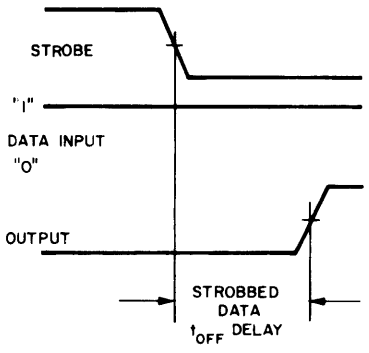
Strobe – An input to a counter or register which permits the entry of parallel data asynchronously.

Strobe Hold Time – The time required to completely strobe parallel data into a counter or register.

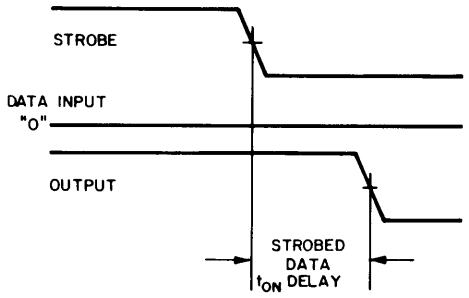
Strobe Release Time – The interval of time required before a clocking transition will be recognized by a counter after the STROBE input has been disabled.



Strobed Data t_{off} Delay – The time interval from the 1.5V point of the STROBE input falling edge to the 1.5V point of the output going high ("1") with a "1" on the asynchronous data input of a counter.



Strobed Data t_{on} Delay – The time interval from the 1.5V point of the STROBE input falling edge to the 1.5V point of the output going low ("0") with a "0" on the asynchronous data input.



Synchronous – Operation of a switching network by a clock pulse generator. All circuits in the network switch simultaneously. All actions take place synchronously with the clock.

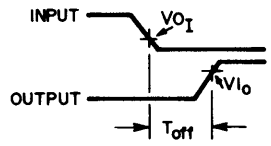
Synchronous Inputs – Those terminals on a flip-flop through which data can be entered but only upon command of the clock. These inputs do not have direct control of the output such as those of a gate but only when the clock permits and commands. Called J-K inputs of AC set and reset inputs.

Synchronous Operation – Operation controlled by a clock pulse.

T

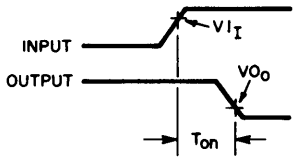
t_{hold} – (See Holding Time.)

t_{off} (turn off time) – Switching time delay of a driven digital element measured between input and output as specified voltage levels, usually the switching threshold voltages.



Inverting Element

t_{on} (turn on time) – Switching time delay of a driven digital element measured between input and output as specified voltage levels, usually the switching threshold voltages.



Inverting Element

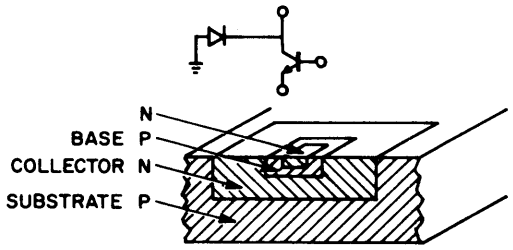
t_{pd} – (See Propagation Delay.)

Thick Film – A method of manufacturing integrated circuits by depositing thin layers of materials on an insulated substrate (often ceramic) to perform electrical functions; usually only passive elements are made this way.

Toggle – To switch between two states as in a flip-flop.

Trigger – A timing pulse used to initiate the transmission of logic signals through the appropriate circuit signal paths.

Triple Diffused – The transistors are fabricated within the monolithic substrate by three diffusion steps.



EXAMPLE: TRANSISTOR-DIODE

True – True condition, the statement for a ONE in the Boolean algebra.

Truth Table – A tabular list with all possible input logic combinations and the resulting output logic for all these combinations.

Example: $F = A \cdot \overline{B}$

Truth Table

A	B	F
0	0	0
1	0	1
0	1	0
1	1	0

Twisted Ring Counter – A feedback shift register with 2N states for N stages. The input to the first stage is the complement of the last stage.

U

Up-Down Counter (Reversible Counter) – Counter counting in ascending or descending order depending upon the logic at the up-down inputs.

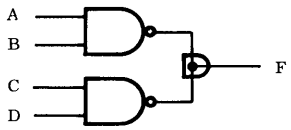
W

Wafer – Semiconductor slice of about 1¼-inch diameter, will generally produce several hundred dice.

Wired-AND/Dot AND Collector Logic – An AND function formed by wiring two or more outputs together. An AND will result from the connection of npn collectors as in conventional DTL or RTL logic. Equal to wired-OR if notation is negative logic (low level = 1).

Example:

$f = (\overline{AB}) \cdot (\overline{CD})$



Wired-OR/Dot OR – An OR function formed by wiring two or more outputs employing active pull-up and passive pull-down together. Frequently applied to wired-AND since its function, $f = \overline{AB} \cdot \overline{CD}$, can be written $f = \overline{AB + CD}$.

Word – A term for the largest grouping of bits, characters, or bytes.

Z

Zero ("0") – See Binary Logic.

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