Signetics

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8X305 Prototyping System Reference Manual

This document provides the information required to understand, set up and operate the 8X305 Prototyping System. It is recommended that the user become thoroughly familiar with the 8X305 MicroController and the high speed peripherals that support the device. For this purpose, the following documents are recommended:

- 8X305 Users Manual — comprehensive functional detail, interface characteristics, hardware and software design data, and systems information for the 8X305 MicroController.
- 8X300 Family Product Capabilities Manual — overview of the 8X300 Family of parts, including application information on the 8X305 MicroController and its support devices.
- MCCAP Manual — complete description of the powerful MicroController Cross-Assembler Program for the 8X300 and 8X305.
- Data Sheets — electrical and functional characteristics for each member of the 8X300 Family and related parts.
  - — 8X305 MicroController
  - — 8X310 Interrupt Control Coprocessor
  - — 8X320 Bus Interface Register Array
  - — 8X330 Floppy Disk Formatter/Controller
  - — 8X338 Local Area Network Controller
  - — 8X350 256 Byte Bipolar RAM
  - — 8X360 Memory Address Director
  - — 8X371 Latched 8-bit Bidirectional I/O Port
  - — 8X372/8X376 Addressable 8-bit Bidirectional I/O Port
  - — 8X374 Addressable 8-bit Bidirectional I/O Port with Parity
  - — 8X382 Addressable 4-IN/4-OUT I/O Port
  - — 8X60 FIFO RAM Controller

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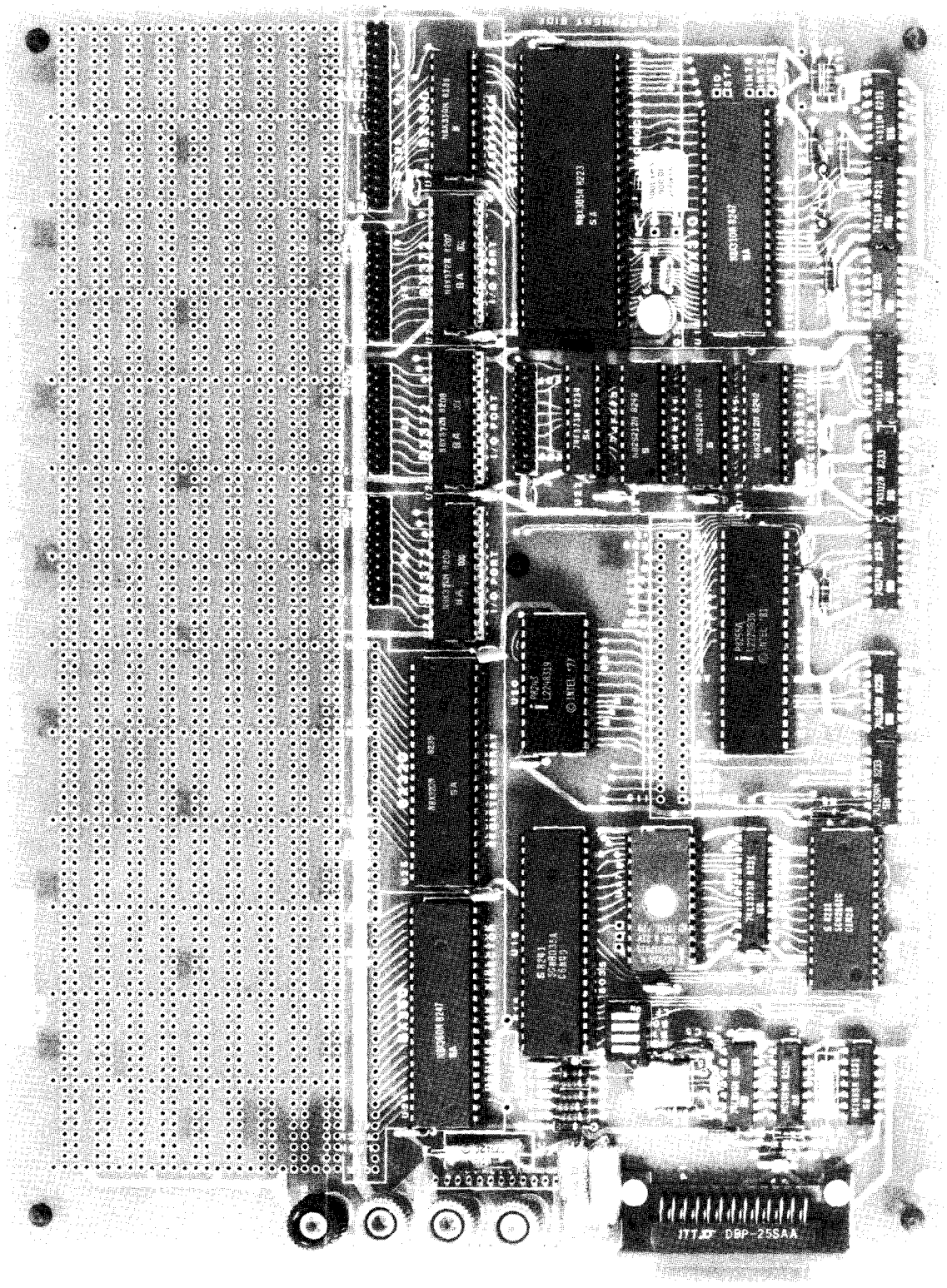


Figure 1-1. 8X305 Prototyping System

1.1 SYSTEM DESCRIPTION

The 8X305 Prototyping System is a powerful design support tool that aids the engineer in the evaluation, design, and prototyping of systems based on the Signetics 8X305 MicroController and its family of support devices. Its advanced features permit the development of both 8X305 firmware and application circuitry. The prototyping systems capabilities are adequate to serve as a complete development system for simple systems and provide a low-cost tool for evaluating portions of more complex designs.

1.2 ARCHITECTURAL OVERVIEW

As shown in Figure 1-1, the 8X305 Prototyping System consists of a single printed circuit board that includes an 8X305 MicroController and various 8X305 Family peripheral devices. The 8X305's microprogram resides in Writeable Control Storage (WCS). A Monitor Processor controls operation of the 8X305 by loading the WCS, activating the Run/ Step logic, and directly placing instructions onto the 8X305's Instruction bus. The Monitor Processor also controls the User Interface, which is through a standard RS-232 connector. The remainder of the board is occupied by power connections and a large wire-wrap area for prototyping of user-developed circuits. A complete discussion of the operation and interrelationship of these functions is contained in later chapters.

1.2.1 USER INTERFACE

The User Interface of the 8X305 Prototyping System is accomplished through a standard RS-232 connector. Data rates from 110 to 19,200 baud are switch selected by the user. The monitor program contained in the system controls all user communication, which is accomplished interactively through a straightforward and user-friendly syntax. While the operation of the system requires only a low-cost "dumb" terminal, it can be connected to a host computer to support more advanced developments. Commands are included to support up and down loading of programs in such applications.

1.2.2 MONITOR PROCESSOR AND RUN/STEP LOGIC

Operation of the system is controlled by the Monitor Processor, which is implemented using an 8035 Microprocessor. The Monitor Processor is responsible for the following functions:

- User interaction
- Loading Writeable Control Storage
- Loading and reading 8X305 registers and I/O devices
- Control of Run/Step logic

Programming for the Monitor Processor is supplied by Signetics and is contained in a PROM.

1.2.3 WRITEABLE CONTROL STORAGE

8X305 MicroController programs are executed from a Writeable Control Storage (WCS) that is contained on the board. The prototyping system is supplied with 256 words of instruction memory. An expansion module is available to support address space requirements of up to 4096 words. The WCS is sufficiently fast to permit full speed operation of the 8X305.

Writeable Control Storage words are 25 bits wide to support advanced microprogramming requirements. Sixteen of these bits contain actual 8X305 instructions. Eight of the remaining bits are used to support "Extended Microcode" designs as described in the 8X305 Users Manual. The 25th bit, transparent to the user, is set by the Monitor Processor to control breakpoints.

Since the three-bus architecture of the 8X305 does not permit the MicroController to modify its own program memory, the WCS is loaded by the Monitor Processor.

1.2.4 8X305 MICROCONTROLLER AND PERIPHERALS

An 8X305 MicroController and various 8X300 Family peripheral devices are included in the prototyping system.

The Instruction and Program Address busses of the 8X305 are connected to Writeable Control Storage (WCS) as well as an 8X310 Interrupt Control Coprocessor (ICC). The interrupt and status pins of the 8X310 are available to the user for use in prototyping real-time or other interrupt driven systems.

The 8X305's IV bus is connected to the following 8X300 Family peripheral devices:

(1) 8X320 Bus Interface Register Array
(1) 8X350 256 Byte Bipolar RAM
(1) 8X360 Memory Address Director
(3) 8X372 Addressable 8-bit Bidirectional I/O Ports

IV bus data and control signal connections are also available to the user to permit attachment of other devices or user developed logic. User interface connections to the 8X320, 8X360, and 8X372's are available adjacent to the wire-wrap area to permit prototyping of various 8X305 based designs.

2.1 POWER CONNECTIONS

CAUTION

Power connections must be properly made; otherwise, component damage will result.

Power connections to the Prototyping System are made through four binding posts located on the left hand edge of the board. These are labeled GROUND, +5, —12, and +12. Without options or user circuitry in the wire-wrap area, the current drawn from each power source is as follows:

+5 VDC — less than 2.5 amperes
+12 VDC — less than 20 milliamperes
—12 VDC — less than 20 milliamperes

Additional current must be supplied for any options or user circuitry added to the board. At the user's option, a DC-to-DC converter (converts +5 VDC to ±12 VDC) can be installed in the space allotted to the —12 VDC and +12 VDC binding posts. Refer to the parts list in Appendix B for the manufacturer and part number of the recommended device.

2.2 RS-232 INTERFACE

An RS-232 connector is provided in the lower left-hand corner of the system for interconnection to the user's CRT terminal, and is connected as shown in Table 2-1.

Table 2-1 RS-232 CONNECTOR

Pin No.	Signal	Description
1	GND	Ground
2	TXD	Transmit Data(in)
3	RXD	Receive Data(out)
4	RTS	Request to Send(in)
5	CTS	Clear to Send(out)
6	DSR	Data Set Ready(out)
7	GND	Ground
8	CAD	Carrier Detect(out)

RS-232 specifications call for data communications equipment (DCE), such as this system, to be connected to data terminal equipment (DTE), such as the user's CRT terminal. When connecting this system to another DCE, such as a host computer, be sure to interchange TXD (pin 2) with RXD (pin 3), and RTS (pin 4) with CTS (pin 5). This can be done on the cable or it can be accomplished logically by using a Null Modem. Due to the variety of interpretations of RS-232, some terminals may not immediately work with the Prototyping System. If difficulties are encountered, first reduce the connections to three signals: TXD, RXD, and GND. Then if necessary, interchange TXD and RXD signals.

2.3 BAUD RATE SELECTION

Any of the eight baud rates listed in Table 2-2 may be selected by proper setting of switches B2, B1 and B0 located near the RS-232 connector.

Table 2-2 BAUD RATES

B2	B1	B0	Baud Rate
0	0	0	19200
0	0	1	9600
0	1	0	4800
0	1	1	2400
1	0	0	1200
1	0	1	600
1	1	0	300
1	1	1	110

(0 = Switch off, 1 = Switch on)

For hard-copy printing terminals, an optional line-feed feature may be selected to avoid over-strike of characters after a backspace on error. This feature is selected by setting the LF switch located next to switch B0 to the ON position.

2.4 EXTERNAL OSCILLATOR CONNECTIONS

CAUTION

To prevent possible damage to the crystal, never apply an external oscillator signal to X1 or X2 input with crystal Y2 connected to the circuit.

The Prototyping System is supplied with a 10 MHz crystal; therefore it operates the 8X305 MicroController at its full rated speed of 200 nanoseconds per instruction. The crystal may be changed by the user to any frequency from 4 MHz to 10 MHz. Alternatively, an external oscillator may be connected to the X1 and X2 inputs of the 8X305, as described in the 8X305 Users Manual. The external oscillator may operate at any frequency between 0.2 MHz and 10 MHz. Note that the 8X305 is capable of running at frequencies lower than 0.2 MHz, but the Prototyping System's Monitor Processor expects the 8X305 to be finished executing an instruction within 10 microseconds, thereby imposing a lower limit of 0.2 MHz. Tie points for X1 and X2 are located next to crystal Y2 and the 8X305. Be sure to disconnect crystal Y2 before connecting the external oscillator inputs to X1 and X2.

2.5 INHIBIT JUMPER FOR 8X310 ROM DISABLE

The 8X310 Interrupt Control Coprocessor connects to the Instruction and Address buses of the 8X305. It accomplishes interrupt and subroutine control by disabling the control storage that contains the 8X305's microprogram and placing specific JMP instructions onto the instruction bus. To permit the Prototyping System to operate either with or without an 8X310 in the circuit, a jumper is incorporated into the ROM Disable (RD) circuitry.

When the 8X310 Interrupt Control Coprocessor is physically present in location U16, the ROM Disable Inhibit Jumper located at R14 next to the 8X310 must not be present so that the 8X310 can disable WCS and avoid bus contention problems. When the 8X310 is not present, this jumper must be connected to the board at location R14 to permanently enable the Writeable Control Store RAMs.

3.1 POWER UP AND DIAGNOSTICS

When power is applied to the Prototyping System, resident diagnostic programs are executed to test the Micro-Controller and Writeable Control Store (WCS). The following message is then printed:

8X305 PROTOTYPING SYSTEM

REV n

SYSTEM CHECK ON

*

where "n" equals the current revision level.

If the Prototyping System is functioning improperly, either "MEMORY ERROR" or "8X305 ERROR" messages will be printed. Then the "prompt" character (*) will be printed and the user may examine WCS memory or 8X305 functions to diagnose the problem.

3.2 MONITOR PROGRAM

With the printing of the "prompt" character (*), system control passes to the monitor program. The user may then enter any of the ten monitor commands:

I **INPUT 8X305 instructions into memory:**
Accepts a starting WCS memory address and then permits the entering of an 8X305 instruction in mnemonic form and an extension instruction in octal notation.

n **Register examine/change, where "n" = register number:**
Displays the register number and its contents and allows a new value to be substituted.

(R0 may be accessed by its alternate name AUX by entering "A" or, R10 may be accessed by its alternate name OVF by entering "0".)

G **GO execute user's 8X305 program:**
Accepts a starting memory address and executes at full speed until a breakpoint or keyboard entry is reached. Then the contents of the registers and the next executable instruction are displayed, and single stepping can proceed.

S **STEP, single step user's program:**
Accepts a starting memory address and displays the contents of the registers and the instruction at that memory address. The instruction is executed by hitting the space bar; and successive instructions by successively hitting the space bar.

M **MEMORY and breakpoint examine/change:**
Accepts a starting WCS memory address and then displays the contents of that location in mnemonic form and indicates a possible breakpoint by an exclamation point. A breakpoint at this location may be set by typing an exclamation point or cleared by typing a backspace. A new 8X305 instruction and extension instruction is then entered by typing an I, as with the INPUT command.

L **LB, left-bank examine/change:**
Accepts a bank address (or the currently enabled address, if a blank is entered) and displays the contents of that left-bank address (0-377 octal). A new value may be entered to substitute for the original content.

R **RB, right-bank examine/change:**
Operates the same as the LB command except action is upon the right-bank.

D **DUMP memory contents to terminal:**
Accepts a starting WCS memory address and an ending address, and then dumps the memory contents from the start address to the end address onto the RS-232 port in ASCII HEX QUOTE format as described in Section 3.6.

F **FILL memory contents from terminal:**
Accepts a starting WCS memory address and fills memory in ASCII HEX QUOTE format as described in Section 3.6.

X **XCODE, temporarily set extended microcode latch:**
Accepts a new extension code value to be temporarily set in the extended microcode latch for control of user circuitry. The content of the extended microcode section of WCS is not changed by this command.

Although the user need only enter a single letter command, the monitor will respond by typing the whole command name as indicated in capitals above.

Any of the commands may be aborted before completion by typing an ASCII "control-C" character. While entering any number (sequence of octal digits), corrections may be made by entering a backspace character and then entering the correct number.

3.3 COMMAND SYNTAX DIAGRAMS

System commands and monitor responses are defined in the syntax diagrams in Figure 3-1a, b and c.

3.4 SAMPLE USAGE

The sample program in Figure 3-3 is shown to give the user an idea of a typical session and includes most commands used by the Prototyping System. A short program is input to WCS via the terminal Keyboard that continually increments R6 of the 8X305 and writes each new (incremented) value to location 133 of the 8X350 on the Right-Bank of the IV Bus and to I/O Port 001 on the Left-Bank. Since extended microcode is not needed in this example, none was entered as indicated by "/000".

3.5 BREAKPOINTS

Breakpoints are designed to halt the 8X305 just prior to the execution of an instruction on which a breakpoint has been specified. If the GO command is issued to start at an address that has a breakpoint set, the system will not stop on that address immediately. If the 8X305 should access that address again then a breakpoint stop will occur.

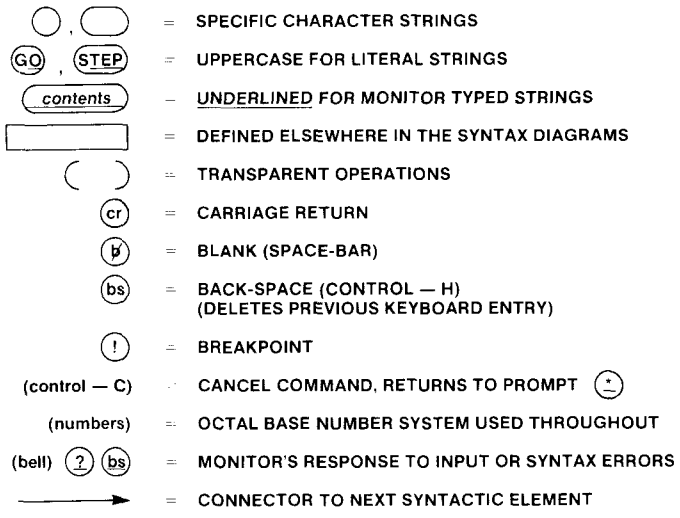


Figure 3-1a. Syntax Definitions

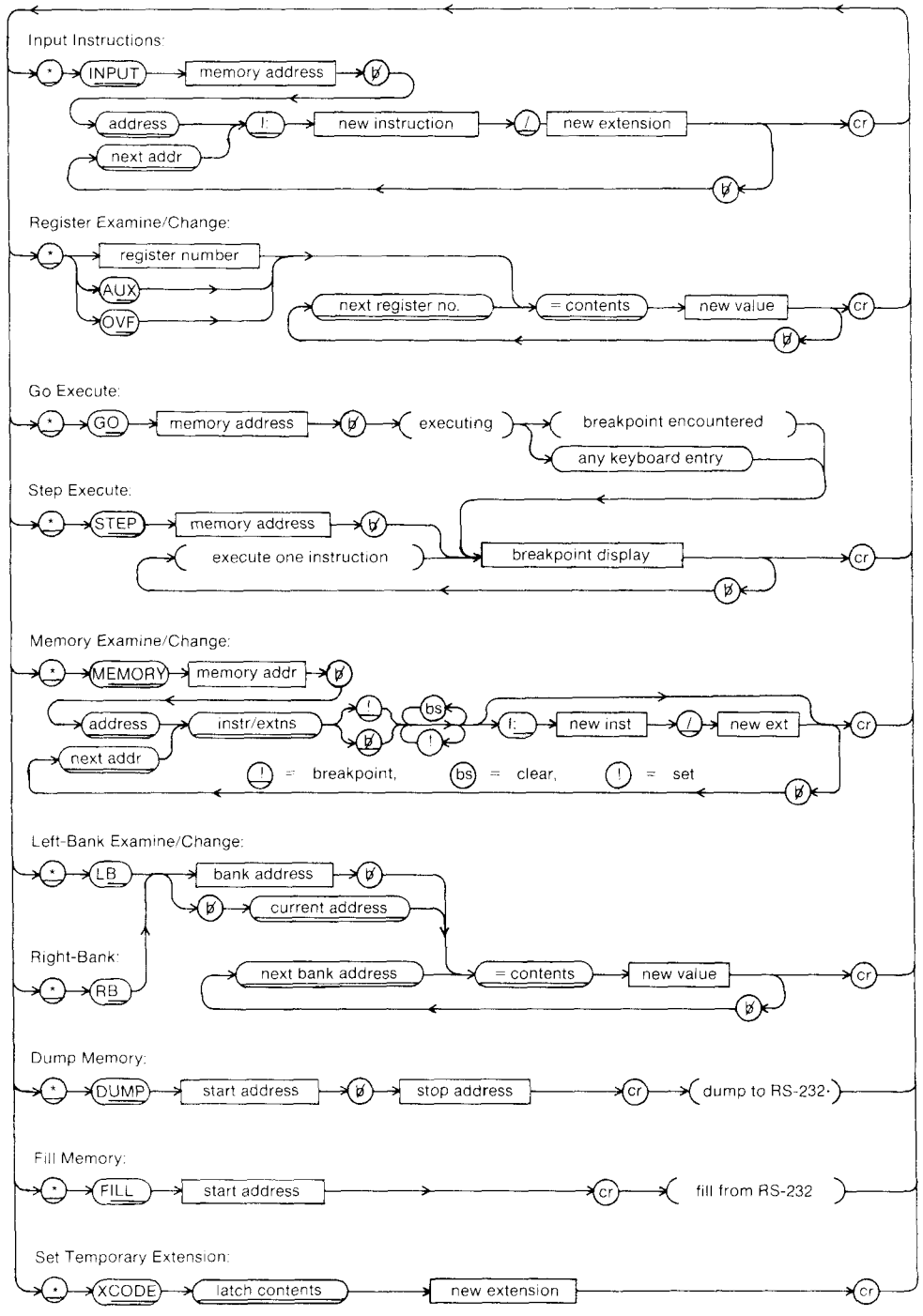
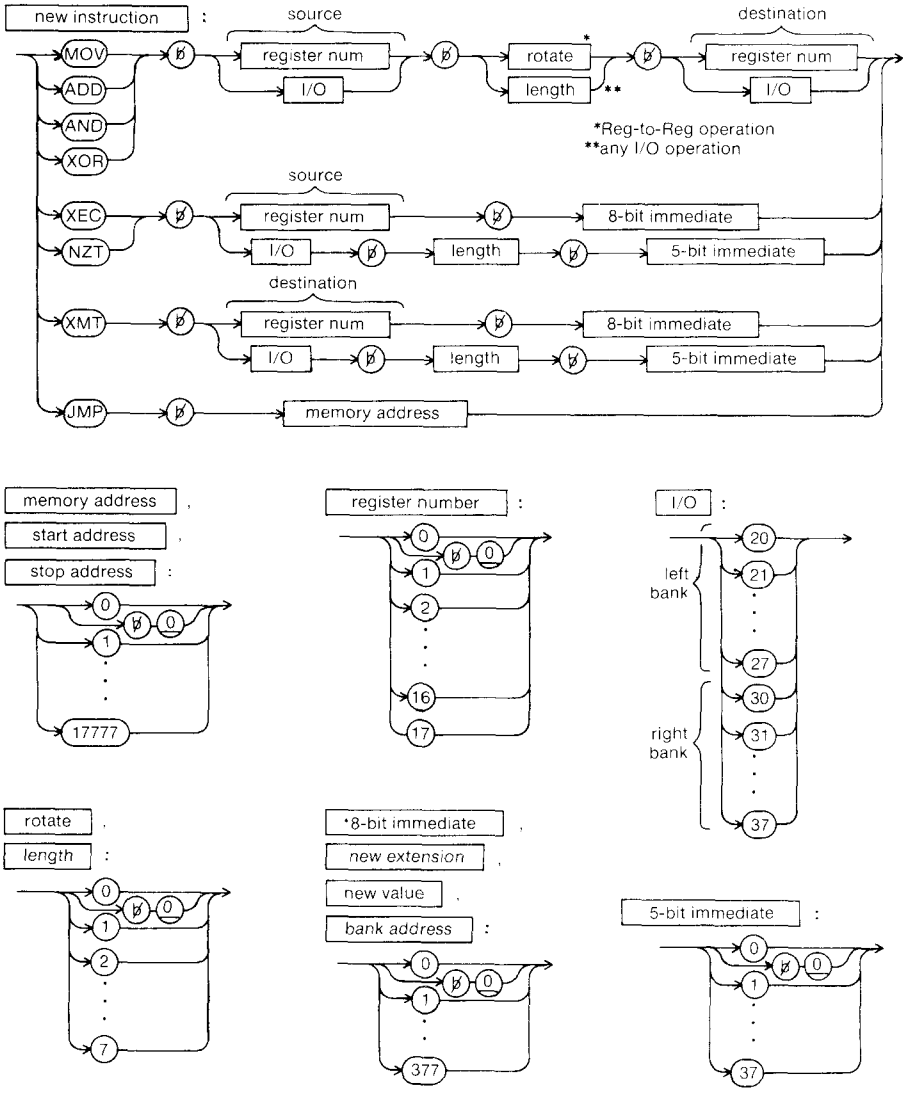


Figure 3-1b. Syntax Flow



note: — First two lines are column headers, printed each breakpoint or each 20 single steps.
— Third line is register contents.
— Fourth line is breakpoint: address — instruction/extension. This is the next instruction to be executed in single step.

Figure 3-1c. Syntax Flow

```
*
* DUMP 00000 00014
DUMPING HIGH BYTES ....
(STX)
00'C0'24'B9'C0'AC'68'74'01'10'70'11'F1'
(ETX)
DUMPING LOW BYTES ....
(STX)
00'00'08'BF'10'FF'FF'96'06'FF'7D'40'D7'
(ETX)
DUMPING EXT BYTES ....
(STX)
00'00'00'00'00'50'00'00'00'00'00'00'00'
(ETX)
*
*
```

Figure 3-2. Example of ASCII HEX QUOTE Format

3.6 ASCII HEX QUOTE FORMAT

Memory contents to and from the terminal during the DUMP and FILL commands are in an object code format commonly supported by PROM programming hardware known as "ASCII HEX QUOTE" format. Each block of eight-bit wide data is preceeded by an STX (ASCII Start of Text) character. Then each 8-bit byte is represented by 2 ASCII HEX characters (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F) followed by a single quote ('). As many bytes as necessary may be transmitted until an ETX (ASCII End of Text) character terminates the block. Three such blocks are transmitted for any specified memory range: high byte of 8X305 instruction, low byte of 8X305 instruction, and extended microcode byte. Figure 3-2 shows an example of ASCII HEX QUOTE format.

3.7 XEC (EXECUTE) INSTRUCTIONS

When stepping through a user program and an 8X305 XEC instruction is encountered, the system will display an "XR" after the next instruction to indicate an XEC range of address.

Note that stepping must start on or before an XEC instruction for the program flow to be correct. If while running a program, a breakpoint or stop occurs on an instruction that is the target of an XEC instruction, an "XR" will not be displayed and program flow will not be correct if single stepping is then begun.

It is valid to nest any number of XEC instructions. Single stepping will work properly provided that the user start on or before the first XEC instruction.

3.8 8X310 INTERRUPT CONTROL COPROCESSOR CONSIDERATIONS

Certain 8X305 "NOP" instructions have specific meanings to the 8X310 as indicated in the data sheet. When using an 8X310 in the system, the user must start running or stepping from an instruction that is not an 8X310 instruction. It is valid, however, to start running and encounter a breakpoint or stop on an 8X310 instruction and then continue single stepping the program.

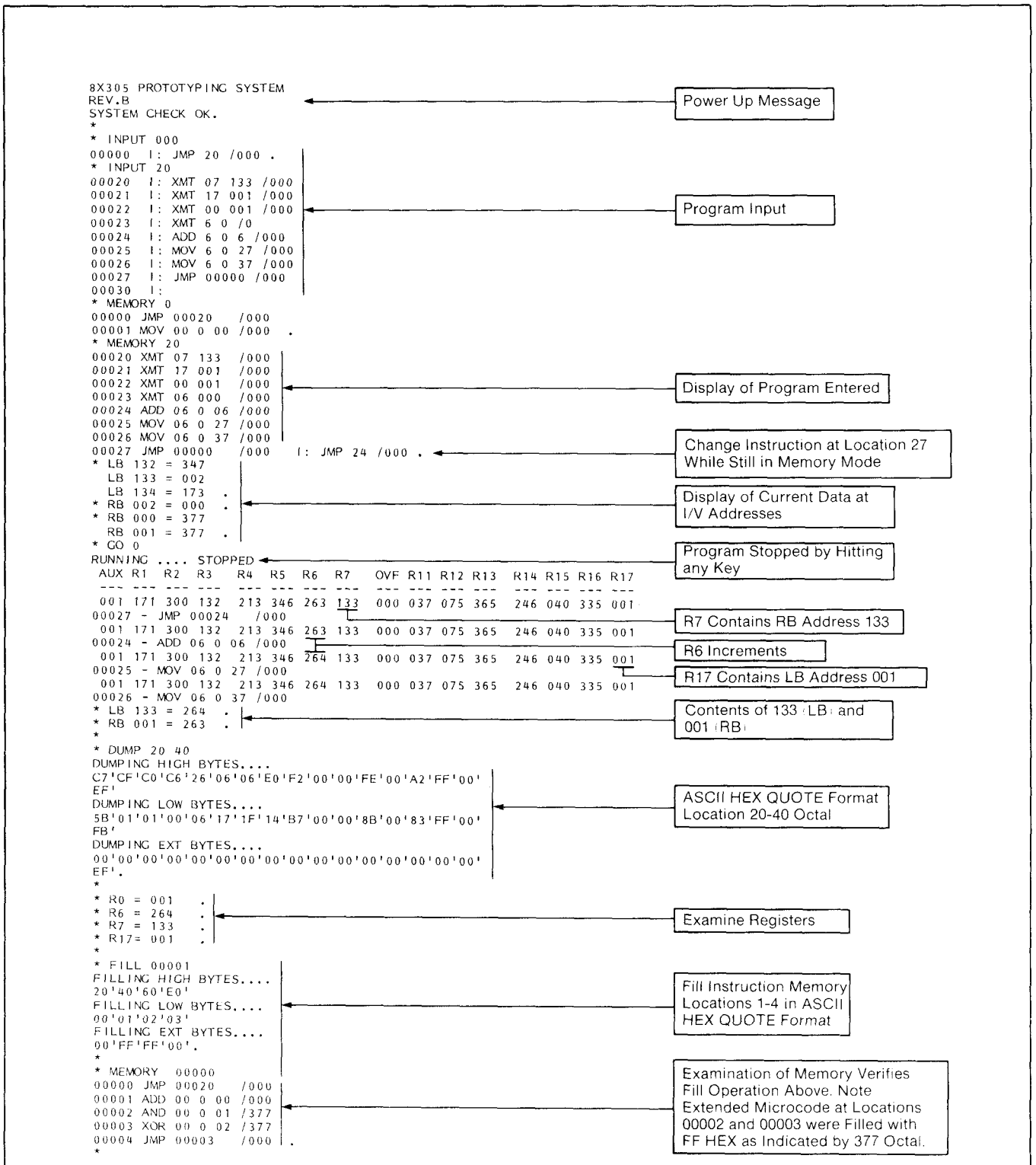


Figure 3-3. Sample Usage

4.1 WIRE-WRAP AREA

The wire-wrap area located at the top of the board provides 26 square inches for user prototyping. This space accommodates standard IC widths from 0.3 to 0.9 inches and also provides power and ground connections.

4.2 IV BUS CONNECTIONS

The IV bus is the major communications link between the 8X305 MicroController and its family of peripherals. The bus is logically partitioned into two banks, referred to as the Left-Bank and Right-Bank. In the Prototyping System the 8X350 Working Storage RAM is connected to the Left-Bank, and the 8X320 Register Array, 8X360 Memory Address Director, and 8X372 I/O Ports are connected to the Right-Bank. All IV bus signals are present at connector J2 as shown in Table 4-1.

Table 4-1 IV BUS CONNECTOR J2

Pin No.	Signal	Description
1	$\overline{IV0}$	BUS (MSB)
3	$\overline{IV1}$	BUS
5	$\overline{IV2}$	BUS
7	$\overline{IV3}$	BUS
9	$\overline{IV4}$	BUS
11	$\overline{IV5}$	BUS
13	$\overline{IV6}$	BUS
15	$\overline{IV7}$	BUS(LSB)
17	V_{CC}	+5 V
19	V_{CC}	+5 V
21	$\overline{HALT}$	Halt
23	$\overline{RESET}$	Reset
25	MCLK	Clock
27	$\overline{LB}$	Left-Bank
29	$\overline{RB}$	Right-Bank
31	SC	Select Control
33	WC	Write Control
(All even pins)	GND	Ground

4.3 I/O PORTS

These 8X372 I/O ports have been provided on the Right-Bank of the IV bus for latching of input or output data. The ports are programmed for addresses 000, 001 and 002 and all signals are available at connectors J4, J5 and J6 respectively. Signals on these connectors are described in Table 4-2. Note that I/O port compatibility allows the user to substitute an 8X376 or 8X382 for any one of the 8X372 I/O ports. (One 8X371 non-addressable I/O port may be substituted, but ONLY if all other components on that bank are removed.)

Table 4-2 I/O PORT CONNECTORS J4, J5 AND J6

Pin No.	Signal	Description
2	UD7	User Data (LSB)
4	UD6	User Data
6	UD5	User Data
8	UD4	User Data
10	UD3	User Data
12	UD2	User Data
14	UD1	User Data
16	UD0	User Data (MSB)
18	$\overline{UOC}$	Output Control
20	UIC	Input Control
(All odd pins)	GND	Ground

4.4 EXTENDED MICROCODE CAPABILITY

"Extended Microcode" is a technique commonly used in 8X305 MicroController based designs to optimize performance. It is implemented by designing program memory to be wider than the 16-bit instruction word required for the 8X305. The additional bits are referred to as the extension and can be used for fast I/O selection or other system control and status monitoring purposes.

The Prototyping System uses a 24-bit instruction word, thus providing facilities for 8 bits of extended microcode. These bits are accessible to the user at connector J3 as shown in Table 4-3.

Table 4-3 EXTENDED MICROCODE BITS AT CONNECTOR J3

Pin No.	Signal	Description
1		No Connection
3	ED0	Extended Microcode (MSB)
5	ED1	Extended Microcode
7	ED2	Extended Microcode
9	ED3	Extended Microcode
11	ED4	Extended Microcode
13	ED5	Extended Microcode
15	ED6	Extended Microcode
17	ED7	Extended Microcode (LSB)
19		No Connection
(All even pins)	GND	Ground

Table 4-4 8X320 SIGNAL CONNECTIONS

Signal	Description
B/$\overline{W}$	Byte/Word Control
A0	Primary Port Address (LSB)
A1	Primary Port Address
A2	Primary Port Address
A3	Primary Port Address (MSB)
$\overline{PIOE}$	Programmed I/O Enable
R/$\overline{W}$	Read/Write Control
WS	Write Strobe
$\overline{DMAE}$	Direct Mem. Access Enable
D7A	Primary Data Port (LSB)
D6A	Primary Data Port
D5A	Primary Data Port
D4A	Primary Data Port
D3A	Primary Data Port
D2A	Primary Data Port
D1A	Primary Data Port
D0A	Primary Data Port
D7B	Primary Data Port
D6B	Primary Data Port
D5B	Primary Data Port
D4B	Primary Data Port
D3B	Primary Data Port
D2B	Primary Data Port
D1B	Primary Data Port
D0B	Primary Data Port (MSB)

4.5 8X310 CONNECTIONS

The 8X310 is connected to the 8X305 MicroController and the Writeable Control Store RAM to provide interrupt and subroutine capability. Five additional signals are provided for user interface as described in the 8X310 data sheet. These signals are accessible at tie points just to the right of the 8X310 chip:

STF	Stack Full Status
ID	Interrupt Disable Control
INT0	Interrupt 0 Input
INT1	Interrupt 1 Input
INT2	Interrupt 2 Input

4.6 8X320 CONNECTIONS

An 8X320 Bus Interface Register Array has ben provided on the IV Bus as a Right-Bank I/O device for interfacing to the user's system. The primary data, status and command signals are accessible at tie points located between the 8X320 and the wire-wrap area. A list of these signals is provided in Table 4-4.

4.7 8X360 CONNECTIONS

The 8X360 Memory Address Director has been incorporated into the Prototyping System design to facilitate implementation of a DMA channel. It is connected to the IV Bus as a Right-Bank I/O device. Interconnection to the signals listed in Table 4-5 can be made at the tie points located between the 8X360 and the wire-wrap area.

In applications using extended microcode to enable I/O devices care must be taken to avoid IV Bus contention with 8X300 Family peripheral devices enabled through the more commonly used address — select cycle. Refer to the 8X305 Users Manual for more information on extended microcode operations.

4.8 MEMORY EXPANSION

The Prototyping System is provided with 256 24-bit words of Writeable Control Storage; 16 bits for 8X305 instructions and 8 bits for extended microcode. The depth of Control Storage can be increased by the connection of an expansion module to connector J1, as shown in Table 4-6. A 4096 word Writeable Control Storage Expansion Module is available from Signetics (Part Number 8X300KT2SK). A schematic for this expansion module is provided in Appendix D.

Table 4-5 8X360 SIGNAL CONNECTIONS

Signal	Description
CLK	Clock Input
TC	Terminal Count Status
LABN	Loop Abort Control
TSCL	Tri-state Control
A0	Address Output (LSB)
A1	Address Output
A2	Address Output
A3	Address Output
A4	Address Output
A5	Address Output
A6	Address Output
A7	Address Output
A8	Address Output
A9	Address Output
A10	Address Output
A11	Address Output
A12	Address Output
A13	Address Output
A14	Address Output
A15	Address Output (MSB)
RS0	Register Select (LSB)
RS1	Register Select
RS2	Register Select
RS3	Register Select (MSB)

Table 4-6 MEMORY EXPANSION CONNECTOR J1

Pin No.	Signal	Description	Pin No.	Signal	Description
1	RAMEN	Disables on-board RAM	2	I15	8X305 Instruction (LSB)
3	GND	Ground	4	I14	8X305 Instruction
5	GND	Ground	6	I13	8X305 Instruction
7	OD	Output Disable	8	I12	8X305 Instruction
9	BKPT	Breakpoint	10	I11	8X305 Instruction
11	$\overline{W}$	Write	12	I10	8X305 Instruction
13	—	No Connection	14	I9	8X305 Instruction
15	—	No Connection	16	I8	8X305 Instruction
17	—	No Connection	18	I7	8X305 Instruction
19	—	No Connection	20	I6	8X305 Instruction
21	CE1	Chip Enable	22	I5	8X305 Instruction
23	A0	8X305 Address (MSB)	24	I4	8X305 Instruction
25	A1	8X305 Address	26	I3	8X305 Instruction
27	A2	8X305 Address	28	I2	8X305 Instruction
29	A3	8X305 Address	30	I1	8X305 Instruction
31	A4	8X305 Address	32	I0	8X305 Instruction (MSB)
33	A5	8X305 Address	34	E7	Extended Microcode (LSB)
35	A6	8X305 Address	36	E6	Extended Microcode
37	A7	8X305 Address	38	E5	Extended Microcode
39	A8	8X305 Address	40	E4	Extended Microcode
41	A9	8X305 Address	42	E3	Extended Microcode
43	A10	8X305 Address	44	E2	Extended Microcode
45	A11	8X305 Address	46	E1	Extended Microcode
47	A12	8X305 Address (LSB)	48	E0	Extended Microcode (MSB)
49	V_{CC}	+5 V	50	V_{CC}	+5 V

As can be noted with the aid of the block diagram in Figure 5-1, the 8X305 prototyping system board contains circuits which may be categorized as follows:

1. Monitor Processor
2. 8X305 MicroController and Family
3. Writeable Control Store
4. Run/Step Logic

5.1 FUNCTIONS OF THE MONITOR PROCESSOR

The Monitor Processor, an 8035 microprocessor and peripherals, controls all the commands and operations described in Chapter 3. The Monitor Processor handles all communication with the terminal as well as reading and writing the 8X305's program storage, registers, and I/O port contents.

The 8X305 can execute instructions from Writeable Control Storage or an instruction that is latched into the 8243 by the Monitor Processor. Typically the instruction in the 8243 will store or read an 8X305's register contents, I/O Port contents, or set the address in the 8X305 Program Counter.

The 8243 is also used to read and write the contents of Writeable Control Store. Since the 8X305 does not have an address bus that can be three-stated and because a buffer would increase the memory access time, to read a specific memory location a JMP is "forced" upon the 8X305 by way of the 8243 to set the address lines.

The Monitor Processor reads the register contents of the 8X305 by forcing an XEC Rn, 000, where Rn is the desired register. This causes the register contents to be placed on the lower eight address lines of the 8X305 where it may be read by the Monitor Processor and sent out on the RS-232 interface. To store a value into the 8X305, the Monitor Processor will force a XMT Rn, XXX, where XXX is the desired register contents. (For R12 and R13, this will be accomplished by a XMT followed by a MOV.)

5.2 8X305 FAMILY

With the following two exceptions the 8X305 MicroController and its supporting peripherals connect to the prototyping system in a conventional manner:

1. Rather than a direct tie to the MCLK output of the 8X305, the MCLK input to the 8X310 Interrupt Control Coprocessor is gated. The gating circuits are required to implement correct single-step operation of the system.
2. The $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ inputs to the 8X305 are gated. Connected in this manner, the $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ signals will only affect the MicroController in the run mode. User circuits requiring either or both of these inputs should pick up the signals via the IV Bus connector J2.

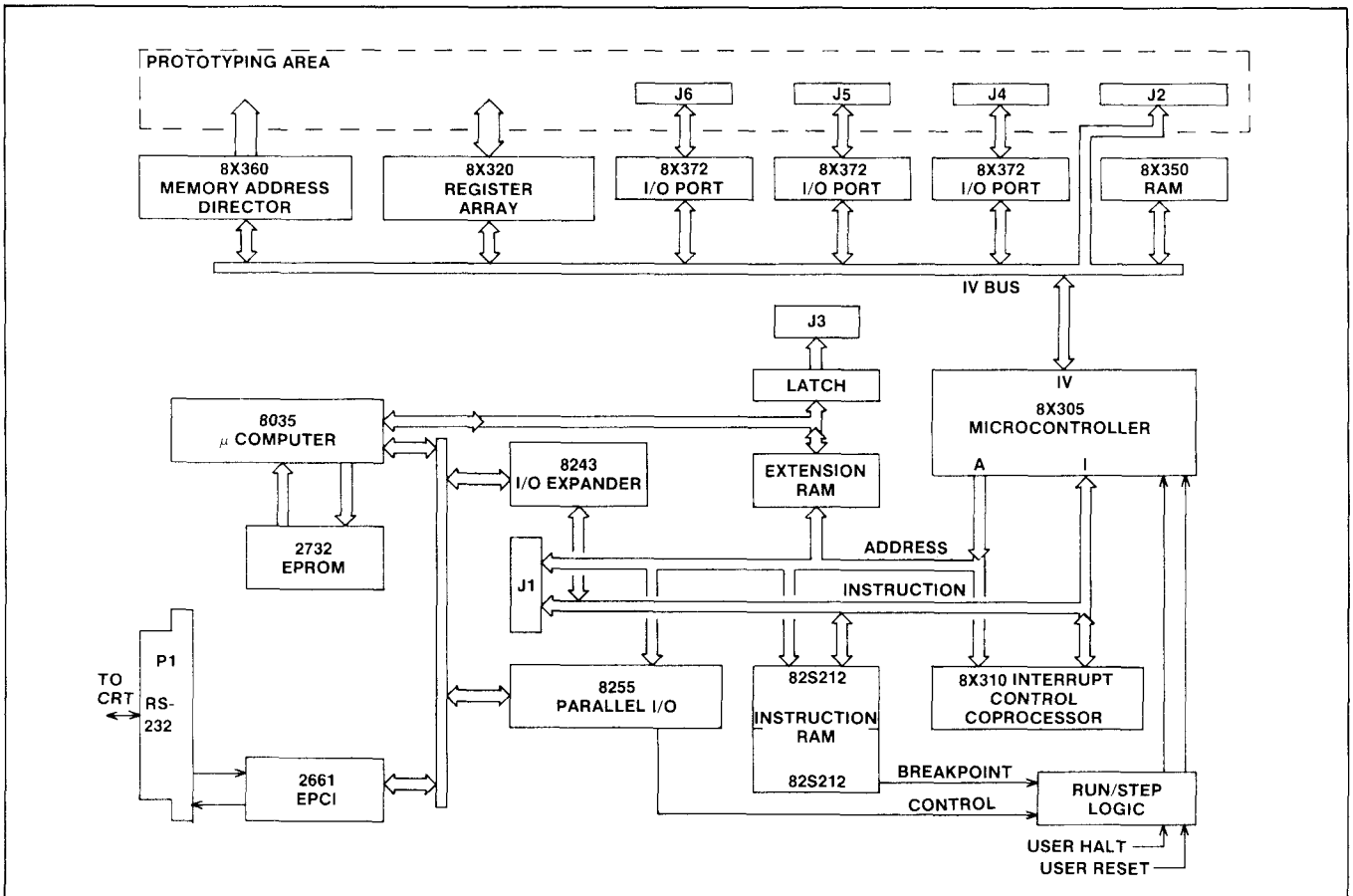


Figure 5-1. Detailed Block Diagram

5.3 WRITEABLE CONTROL STORAGE

Instead of the usual PROM or ROM instruction storage found in a typical 8X305 based system, a Writeable Control Store (WCS) has been implemented with high speed RAM to facilitate programming via the RS-232 terminal. The RAM memory provides 256 x 16 bits for 8X305 instruction storage, 256 x 8 bits for extended microcode, and 256 x 1 bit for breakpoints. If extended microcode is not desired the RAM chip at U21 may be removed and references to the extension will be removed from the display. Any one or all memory address locations may contain a breakpoint.

Note that no page decoding is provided on the board, so the 256 words of instructions will be repeated every 256 addresses throughout the entire 8K memory range of the 8X305.

The memory may be expanded up to the full 8K directly addressable by the 8X305. A 4K word Writeable Control Storage Expansion Module is available from Signetics (Part Number 8X300KT2SK). When the additional memory is installed in J1, the RAM enable (RAMEN) signal is grounded to disable the on-board 256-word memory, and the Monitor Processor is signaled to provide the correct write cycle at J1 for the added RAM. See Figure 5-2 for the differences:

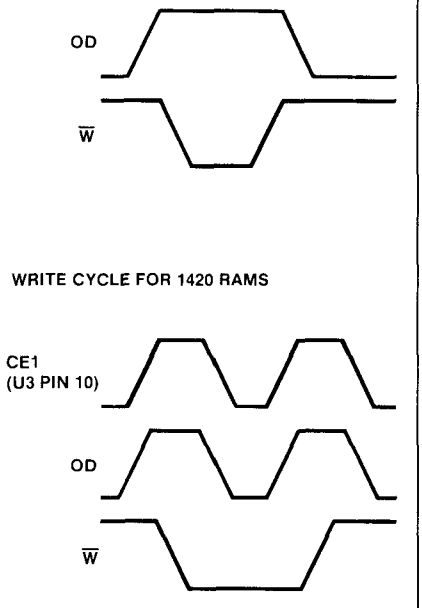


Figure 5-2. Write Cycle Variations

5.4 RUN STEP LOGIC

The Run-Step logic consists of components U5, U6, U7, U9 and U10 on the schematic in Appendix A. These circuits provide the control logic required to allow the 8X305 to execute instructions at full speed or in a single step mode of operation. This is easily accomplished since all instructions are executed within one machine cycle, the time from the falling edge of MCLK to the next falling edge of MCLK. The $\overline{\text{HALT}}$ input is sampled by the 8X305 sometime after the falling edge of MCLK. If it is low, the address lines of the MicroController are held stable; the current instruction is executed after the $\overline{\text{HALT}}$ input goes high (inactive). During the time that the $\overline{\text{HALT}}$ input is low (active), the MCLK output is unaffected. Inputs to the Run-Step logic are labeled RUN/$\overline{\text{WAIT}}$, STEP, BKPT and MCLK; the output is labeled $\overline{\text{HALT}}$ and connected directly to the $\overline{\text{HALT}}$ input of the 8X305 MicroController.

Two of the inputs, RUN/WAIT and STEP, are controlled by the Monitor Processor. The BKPT input connects to the extra bit in WCS that is used for breakpoints. The MCLK input comes directly from the MCLK output of the 8X305.

During single stepping the RUN/$\overline{\text{WAIT}}$ line is low and a pulse on the STEP line causes the 8X305 to execute only the current instruction. This is because the $\overline{\text{HALT}}$ line will go high for just one machine cycle. Entering the run mode the RUN/$\overline{\text{WAIT}}$ line is high and a pulse on the STEP line causes the 8X305 to begin executing instructions from the current address at full speed. The $\overline{\text{HALT}}$ input will go high and remain so until the RUN/$\overline{\text{WAIT}}$ line is brought low or until a breakpoint is encountered.

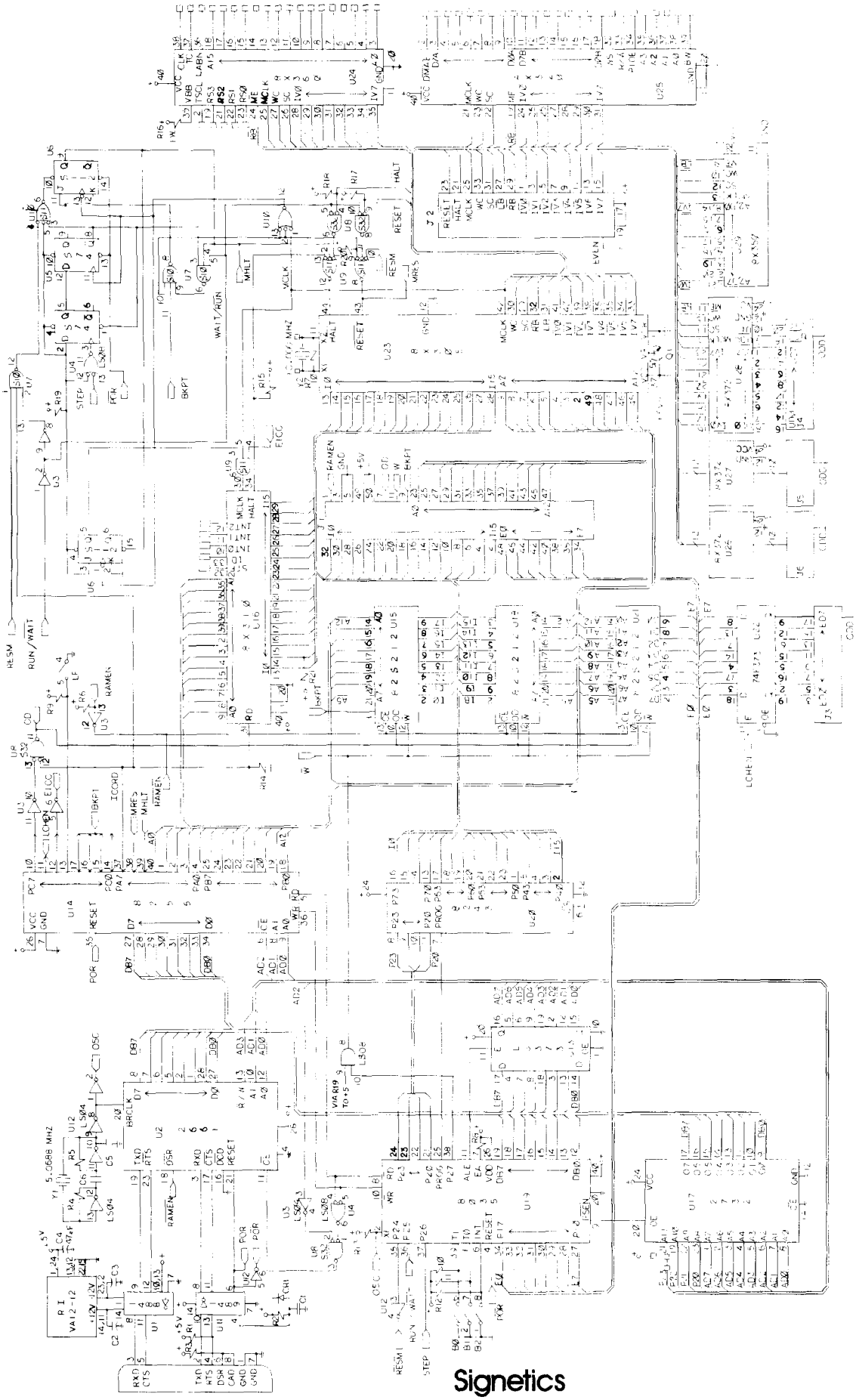
Appendices

A. 8X300KT1SK Prototyping System Schematic

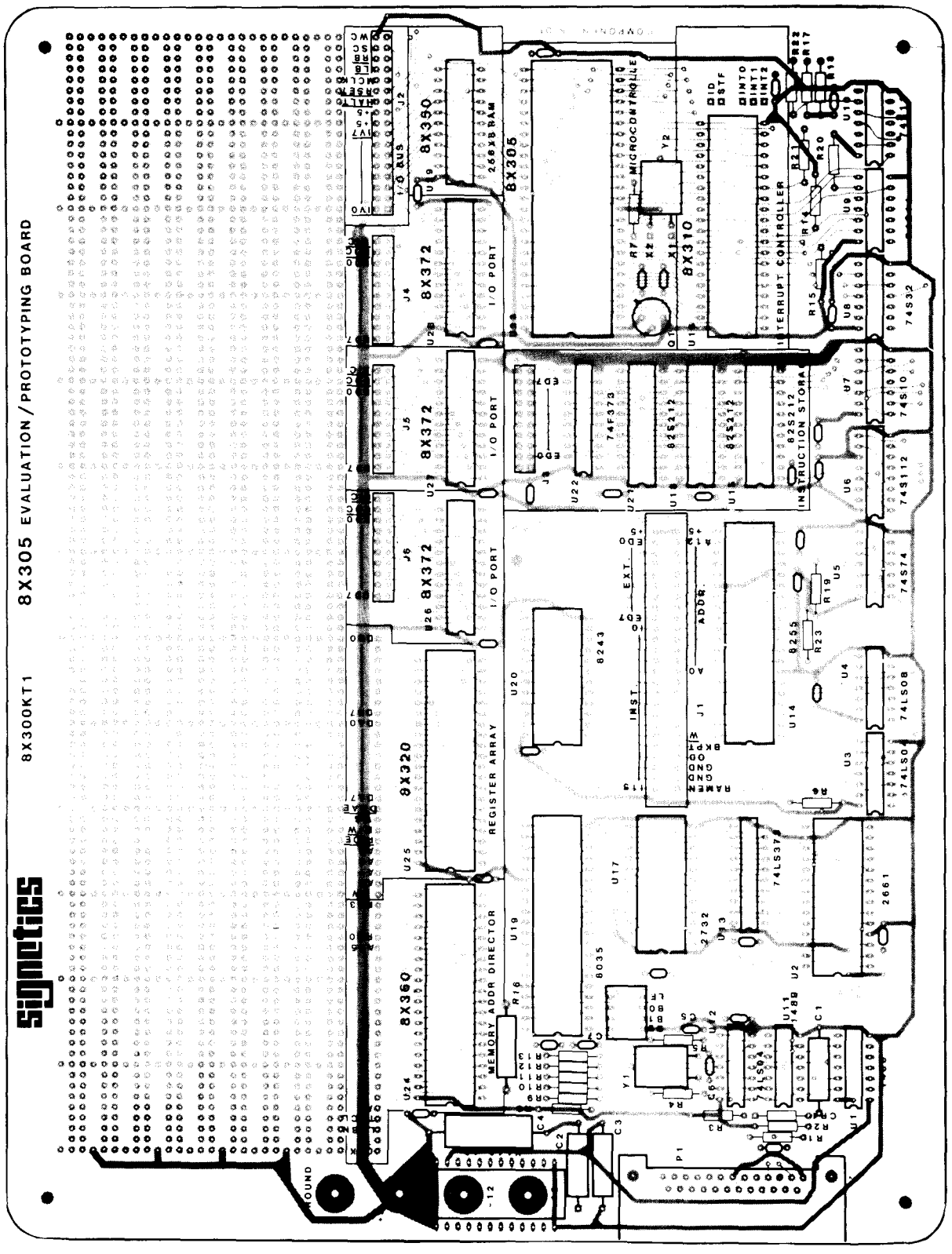
B. 8X300KT1SK PCB Layout and Parts Placement

C. Parts List

D. Memory Expansion Assembly Schematic



Appendix A. 8X300KT1SK Prototyping System Schematic



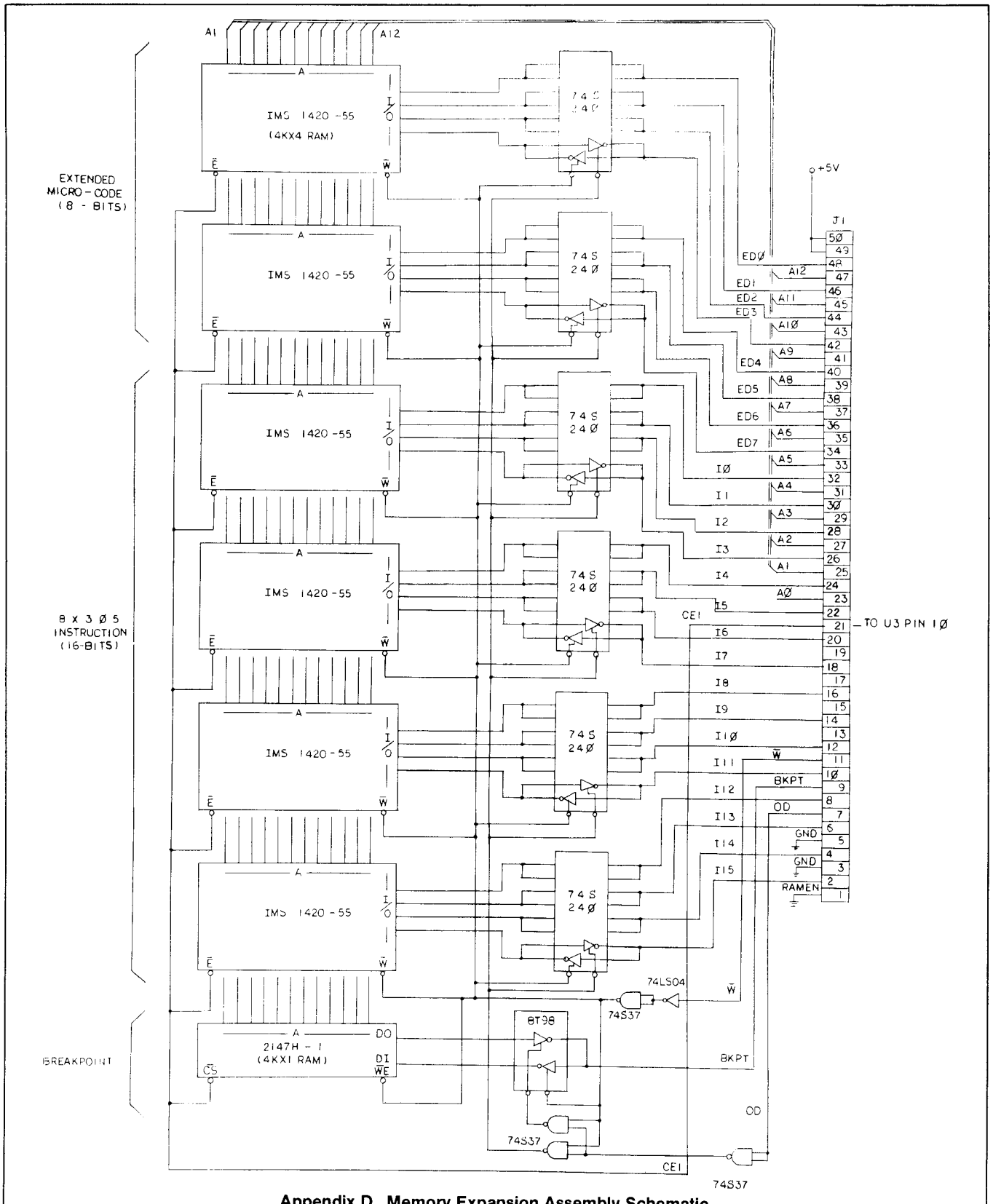
Appendix B. 8X300KT1SK PCB Layout and Parts Placement

Item No.	Manufacturer	Part Number	Description	Designator	Qty.
1	Signetics	MC1488N	Quad Line Driver	U1	1
2	Signetics	SCN2661CC1N28	EPCI	U2	1
3	Signetics	N74LS04N	Hex Inverter	U3, U12	2
4	Signetics	N74LS08N	Quad AND Gate	U4	1
5	Signetics	N74S74N	Dual D-Flip-Flop	U5	1
6	Signetics	N74S112N	Dual J-K Flip-Flop	U6	1
7	Signetics	N74S10N	Triple NAND Gate	U7	1
8	Signetics	N74S32N	Quad OR Gate	U8	1
9	Signetics	N74S11N	Triple AND Gate	U9, U10	2
10	Signetics	MC1489N	Quad Line Receiver	U11	1
11	Signetics	N74LS373N	Octal Latch	U13	1
12	Intel	P8255A	PPI	U14	1
13	Signetics	82S212N	256 x 9 RAM	U15, U18, U21	3
14	Signetics	N8X310N	Interrupt Control Coprocessor	U16	1
15	Intel	2732A-4	4096 x 8 EPROM	U17	1
16	Signetics	SCN8035AC6N40	8-Bit Microcomputer	U19	1
17	Intel	P8243	Input/Output Expander	U20	1
18	Signetics	N74F373N	Octal Latch	U22	1
19	Signetics	8X305I/N	MicroController	U23	1
20	Signetics	N8X360N	Memory Address Director	U24	1
21	Signetics	N8X320N	Register Array	U25	1
22	Signetics	N8X372-000N	I/O Port	U26	1
23	Signetics	N8X372-001N	I/O Port	U27	1
24	Signetics	N8X372-002N	I/O Port	U28	1
25	Signetics	N8X350N	256 x 8 RAM	U29	1
26	ITT CANNON	DBP-25SAA	RS-232 Connector	P1	1
27	TRW CINCH	252-25-30-360	Edge Connector, 50 Pin	J1	
28	Spectra-Strip	800-579	Header, 34 Pin	J2	1
29	Spectra-Strip	800-586	Header, 20 Pin	J3, J4, J5, J6	4

Appendix C. Parts List

Item No.	Manufacturer	Part Number	Description	Designator	Qty.
30	Reliability	VA12-12	DC-DC Converter		
31	Saronix	NMP051L	Crystal, 5.688 MHz	Y1	1
32	Saronix	NMP100L	Crystal, 10.000 MHz	Y2	1
33		2N5320	Transistor	Q1	1
34	ALCO	DSS-4	Switch, Mini-dip	B2, B1, B0, LF	1
35	Smith	230	Binding Post		4
36		1N914	Diode	CR1	1
37			CAP, 0.1 μF		28
38			CAP, 47 μF, 20 V	C2, C3, C4	3
39			CAP, 47 μF, 6 V	C1	1
40			CAP, 47 pF	C5	1
41			CAP, 0.1 μF	C6	1
42			RES., 1K, 1/4 W	R19	1
43			RES., 10K, 1/4 W	R1, R2, R3	3
44			RES., 390, 1/4 W	R4, R5	2
45			RES., 2.2K, 1/4 W	R6-R13, R15, R17, R18, R20, R21	13
46			RES., 18, 1 W	R16	1
47	H.H. Smith	2501	Bolt, Nylon 4 — 40 x 3/8"	P1	2
48	H.H. Smith	2554	HEX Nut, Nylon 4 — 40	P1	2
49	BURNDY	DILBQ50P-101	Socket, 50 Pin	U23	1
50	T.I.	C844002	Socket, 40 Pin	U14, U16, U19, U24, U25	5
51	T.I.	C842802	Socket, 0.6" 28 Pin	U2	1
52	T.I.	C842402	Socket, 0.6" 24 Pin	U17, U20	2
53	EMC	17424-01-445	Socket, 0.4" 24 Pin	U26, U27, U28	3
54	T.I.	C842202	Socket, 0.4" 22 Pin	U15, U18, U21, U29	4
55	T.I.	C842002	Socket, 0.3" 20 Pin	U22	1
56	Signetics	PCB-82001	P.C. Board		1
57	H.H. Smith	2450	Rubber Bumper		5

Appendix C. Parts List (continued)



Appendix D. Memory Expansion Assembly Schematic

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