XDS 901746A

SIGMA 5/7

TROUBLESHOOTING HANDBOOK

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Prepared by
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XEROX

FOREWORD

This handbook contains troubleshooting information for both the Sigma 5 and the Sigma 7 Computers. Troubleshooting information for the Sigma 5 was formerly issued under publication No. 65-50-xx while the Sigma 7 was issued under publication No. 65-70-xx. This handbook includes the information from both the Sigma 5 and Sigma 7 Handbooks and also contains information not previously covered in either handbook. The handbook is divided into three sections as follows:

Section I - Sigma 5 information
Section II - Sigma 7 information
Section III - Information common to both the Sigma 5 and Sigma 7.

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missing from original

Σ5 CABLING (TYPICAL)

E – ETCH SIDE
C – COMP. SIDE
B – BLANK TERMINATOR
T – 33Ω RES. TERM.
✳ – ABORT TERM
RC – RIBBON CABLE
TP – TWISTED PAIR CABLE

8201 Σ5 CPU
PWR. MON. 1 J5
PWR. MON. 2 J5
31N START, MFLO-7
12M MB0-13
25P MB14-27
18R MB28-31 L29-31
15R L15-28
15S MR, AH, AR, DR, PE

MEM. 1 / MEM. 2
2C, 8A, 8B, 8C, 6D, 8D, 6A, 6B, 4B, 2D, 4D, 2A, 2B, 4A, 4C, 6C
8251 8251

DUAL PORT EXP.
TP 8C 13C 19C 23C 27C
TP 6C 11C 17C 21C 25C

REG. EXT. UNIT 8216
9S RR16-23
13T RR24-31
13K RRO-7
15K RR8-15
28T CLÉCK

PT/P 7060
32D 30D 28D 26D ✳ 1C 3C 1D
READ J6 2A 4A PUNCH

INTEGRAL I⊙P
10L 8L 9F 9E

SIOP 8285
20D 18D 15D 11D 13D 11A 14E 21E 11E 9E 17E 19E 10F
BUS SHARED SIOP
4 BYTE CONT. 32A 30A 28A 26A
2 BYTE CONT. 32 30 28 26 ✳

CABLED AT TOP
(1) 2B 2D 10B 18B 26B
(2) 4B 4D 12B 20B 28B
(3) 6B 6D 14B 22B 30B
(4) 8B 6D 16B 24B 32B
8257

CABLE AT TOP
CFE-3 8291
32B 30B 28B 24B 26B
29E 27E 25E 30D → TO DIC INTERFA
28D → TO EXT. INT

MIOP 8271
10A 12A 14A 16A 18A 12C 14B 32A 14C 1D

KSR 7012 32B 30B 28B 5B KSR
C/P 7160 32D 30D 28D 26D 1D 5A
ASR 7020 32B 30B 28B 26B 1B 3B 12A 14A
C/R 7122 32F 30F 28F 26F 11E 16F 32A 25A

CL⊙CK CLOCKS
1E 32L 30T 32P 26T
FLOAT 8218 RC 32B 32D

(IOP PRIORITY)
IIOP 1st. MIOP 2nd SIOP 3 Rd.
7F 5F CNST. PR, RIO

DIO INTERFACE 8270
9M 22Q 26Q 29Q
DIO0-13 DIO14-27 DIO28-47 DIO32-54

COC 7611
26C 28C 30C 32C 13B 15B 17B 9B

EXT. INT. 8221
22R 31S 26S 27N
26J 28J 12J 19J 32J

PSC 7720
X 26B 28B 30B 32B
X Y OR 32A 30A 28A 26A
Y 24B 22B 20B 18B ✳ 4A 2A 3B
PERIPH. SW CONTROL BOX J1 J2 7721

NOTE – PERIPHERAL SWITCH CONTROLS WHICH IOP 'X' OR 'Y' THAT WILL HAVE CONTROL

MIOP-Y 8273
14B 32A 14C 1D

DIO ADAP. X or Y 7710
6A 4A 2A 18A 14A 10A 16A 12A 8A

CPU-Y 8270
22Q 26Q 29Q

PCP
2R 4R 17L 17M 18P 18Q 13A 15A
J1 J3 J5 J6 J8 J10 J13 J15

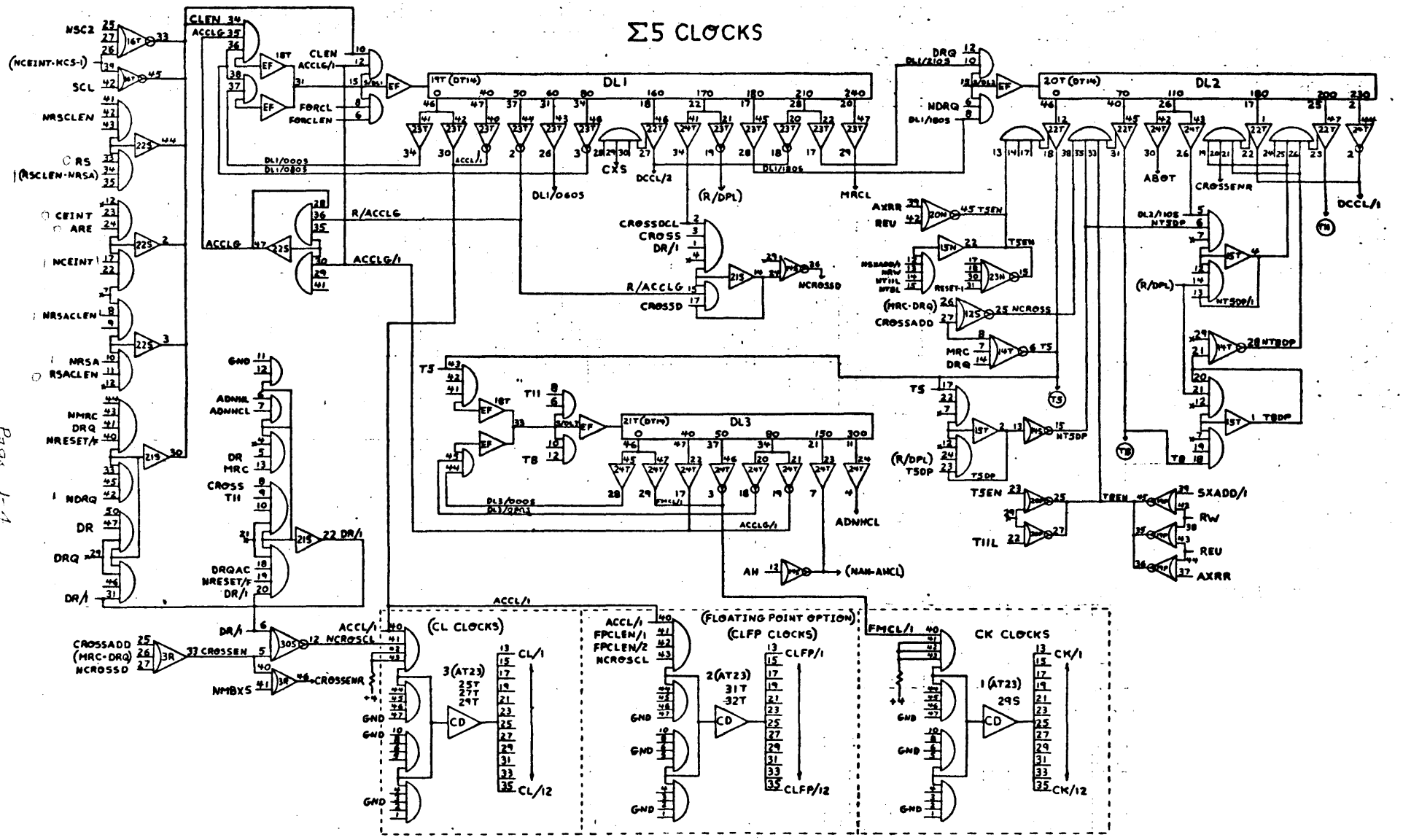
L/P 7440
32J 30J 28J 26J 2G P105 21E P106

MAG. TAPE
32Y 30Y 28Y 26Y 32W 32V 11V 28Z 26Z 32Z 25W 5S 11S 13S 19S 22S 30S 32S

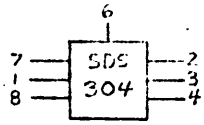
M/T SLAVE
5S 11S 13S 19S 22S 30S 32S

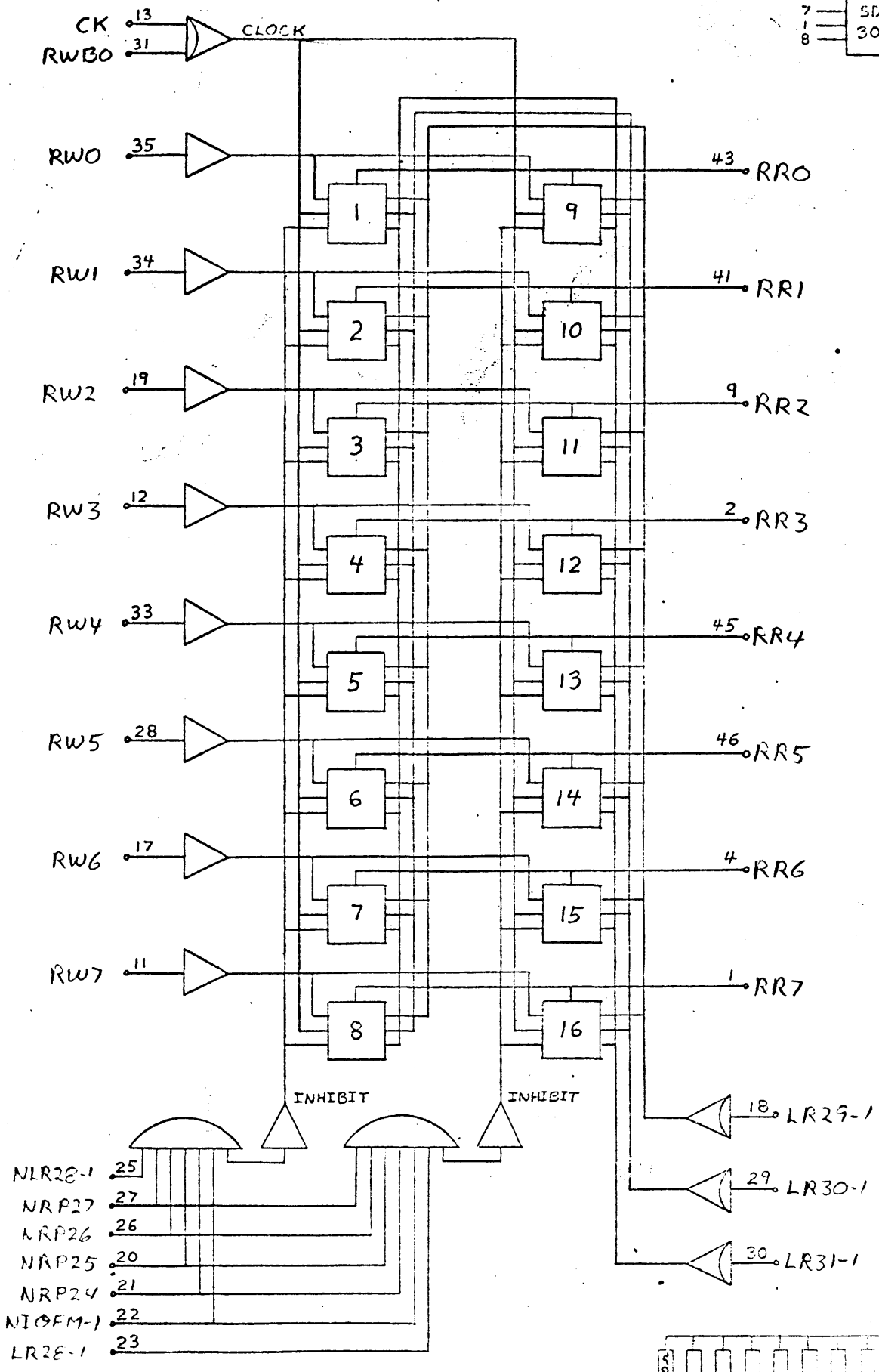
RAD 720X
32C 30C 28C 26C ✳ 30A 32A 18A 28A

RAD SLAVE 720X
28A 18A


Σ5 CLOCKS
NSC2
(NCEINT·NCS-1)
SCL
NRSCLEN
RS
(RSCLEN·NRSA)
CEINT
ARE
NCEINT
NRSACLEN
NRSA
RSACLEN
NMRC
DRQ
NRESET/F
NDRQ
DR
DRQ
DR/1
CLEN
ACCLG
ACCLG/1
FORCL
FORCLEN
DL1
DL1/0005
DL1/0805
DL1/0605
CXS
DCCL/2
(R/DPL)
MRCL
R/ACCLG
CROSSDCL
CROSS DR/1
CROSSD
NCROSSD
DRQ
NDRQ
DL1/1805
DL2
ABOT
CROSSENR
DCCL/1
AXRR
REU
T5EN
(MRC·DRQ)
CROSSADD
MRC DRQ
T5
T11
T8
DL3
ADNHCL
(NAH-ANCL)
DL2/1105
NT5DP
NT500/1
28 NT5DP
1 T5DP
(R/DPL) T5DP
T11L
SXADD/1
RW
REU
AXRR
GND
ADNHL
ADNHCL
DR MRC
CROSS T11
DRQAC NRESET/F DR/1
22 DR/1
CROSSADD (MRC·DRQ) NCROSSD
37 CROSSEN
NMBXS
+CROSSENR
NCROSCL
(CL CLOCKS)
3(AT23) 25T 27T 29T
CD
CL/1
CL/12
(FLOATING POINT OPTION)
(CLFP CLOCKS)
FPCLEN/1
FPCLEN/2
2(AT23) 31T 32T
CLFP/1
CLFP/12
FMCL/1
CK CLOCKS
1(AT23) 29S
CK/1
CK/12

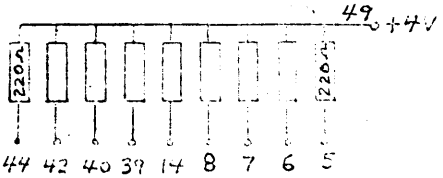
FT25 REGISTER (9K)





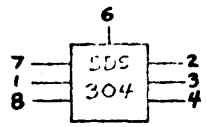
Σ5 REGISTER

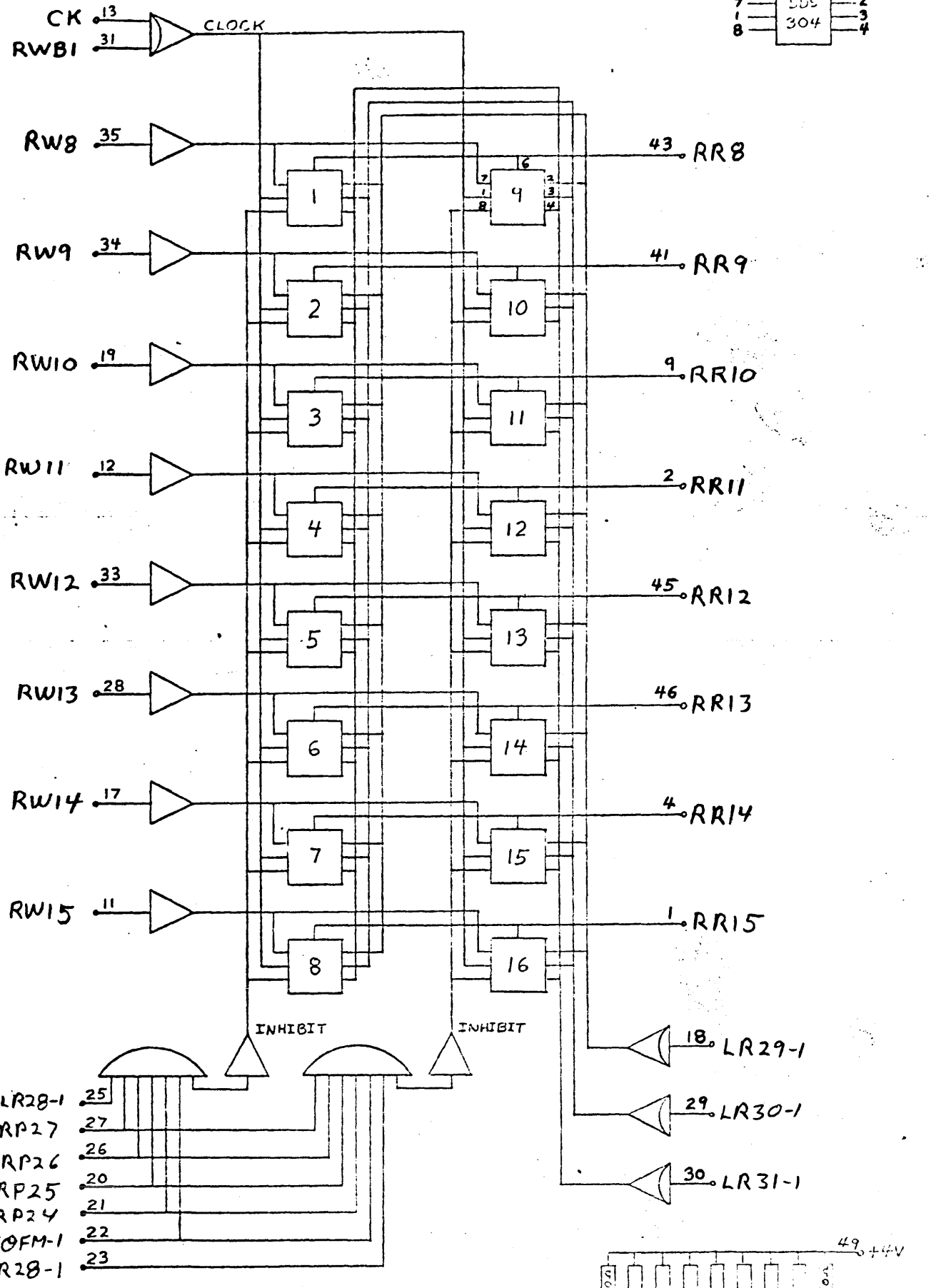
(9K) BITS 0-7

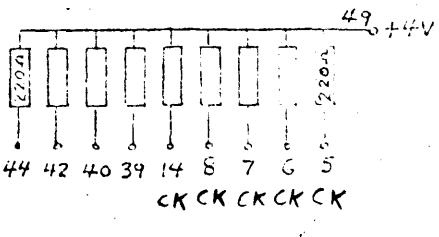


FT25

REGISTER (19K)



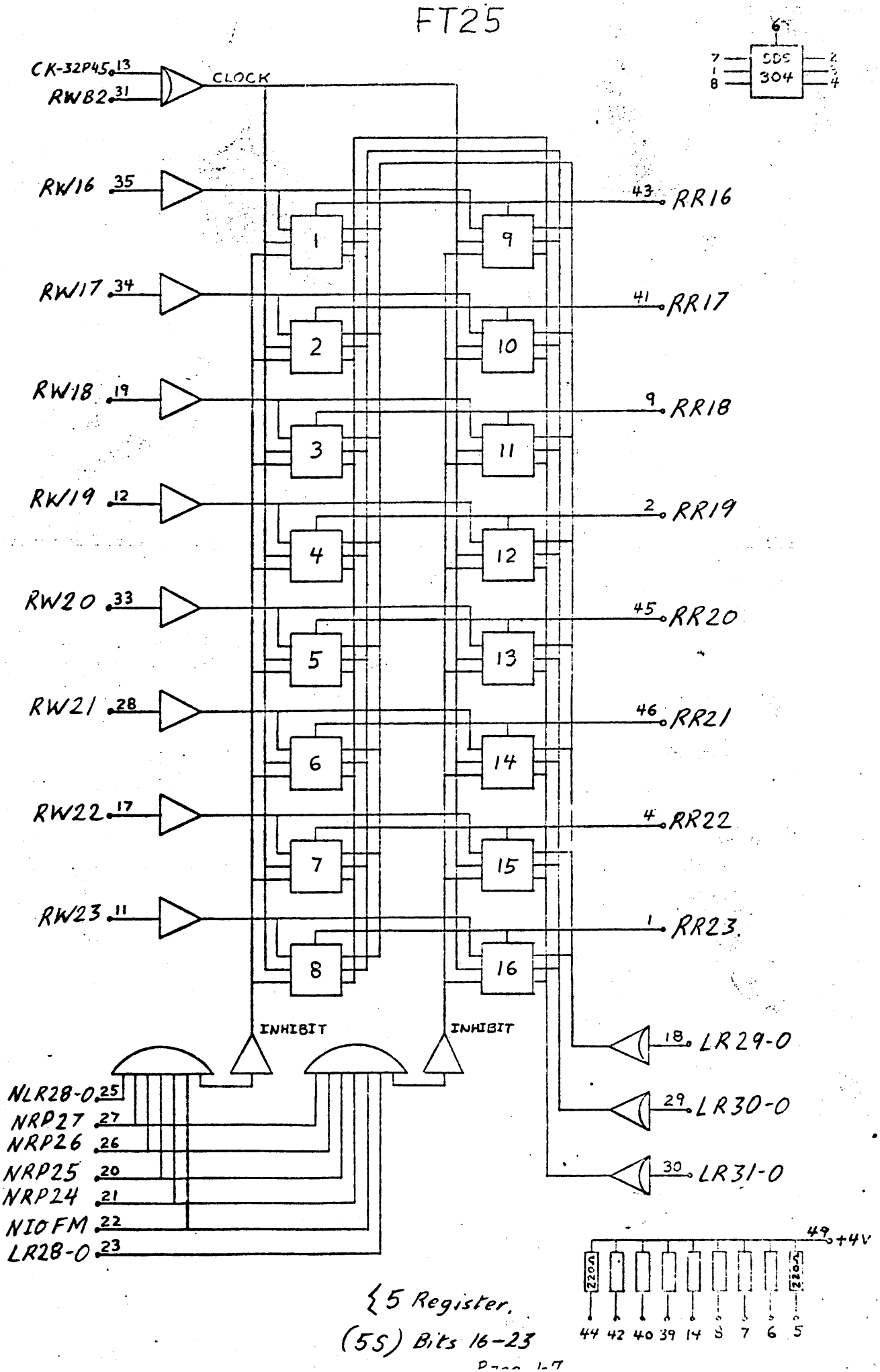




Σ5 REGISTER

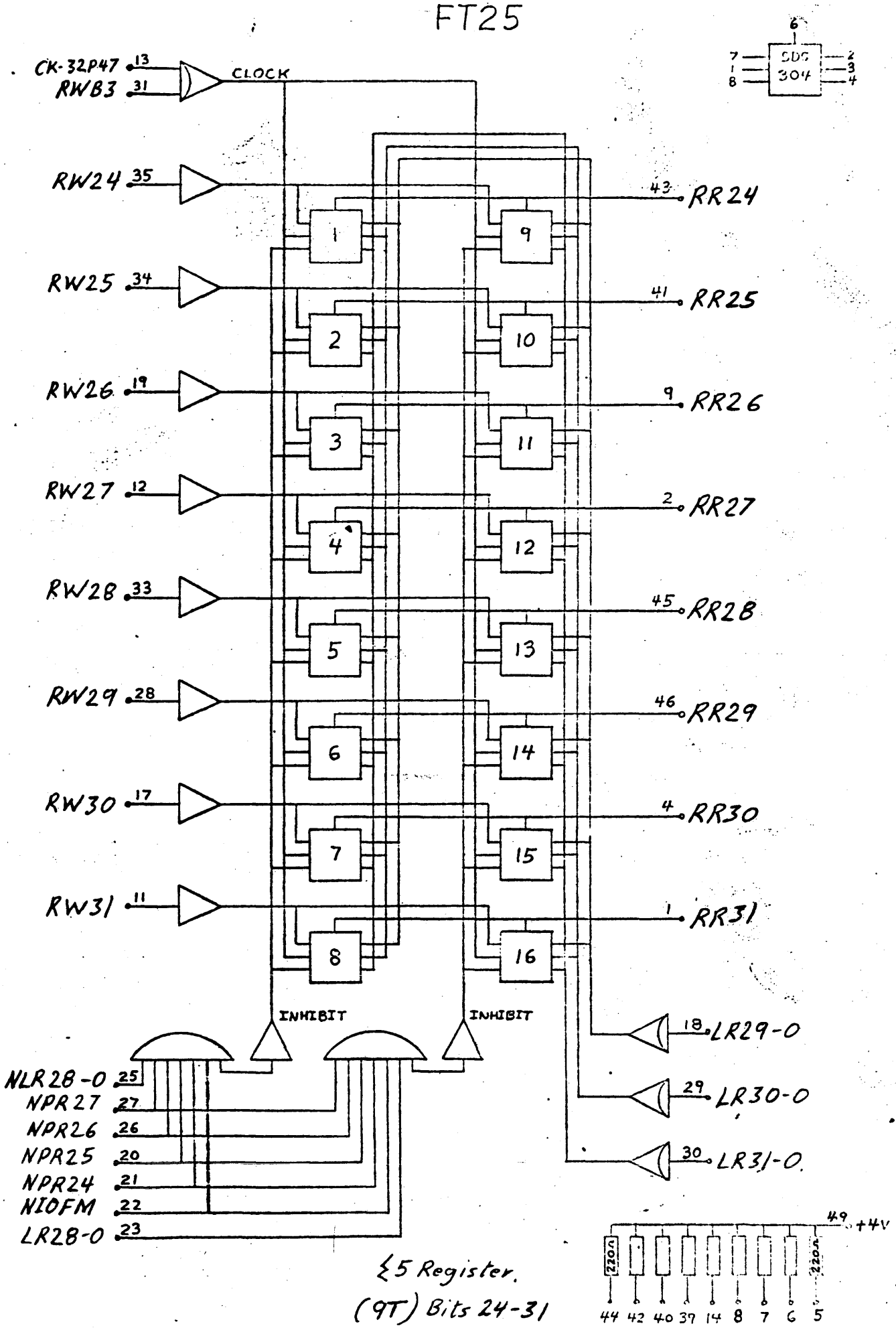
(19K) BITS 8-15

FT25



{5 Register.
(55) Bits 16-23

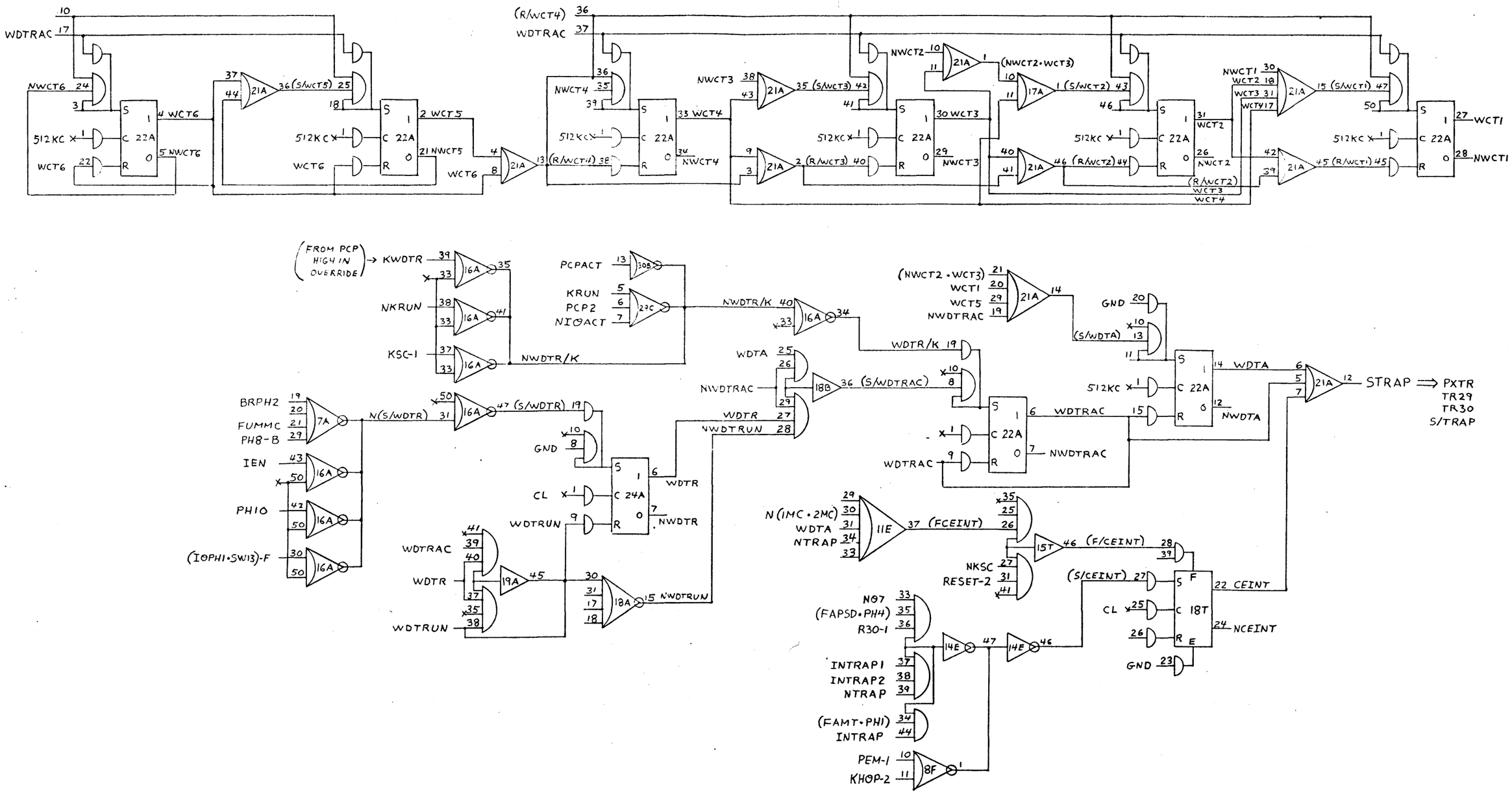
FT25



{5 Register.
(9T) Bits 24-31

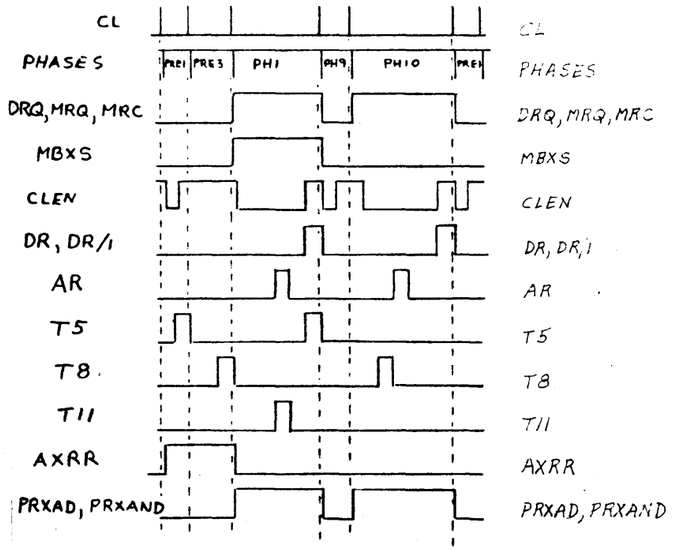
Σ5 WATCHDOG TIMER TRAP (46)

6/1/68
TO 'G' REV.
Cochrane

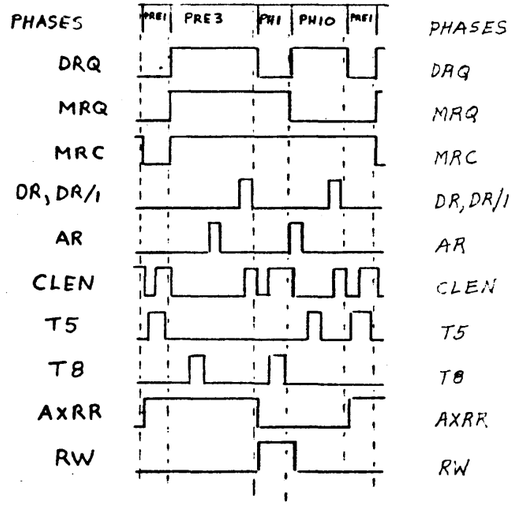


Σ5 TIMING STW & LW

STW
35C0 0100 & HOLD SW ON



LW
32C0 0100 & HOLD SW ON



SIGMA 5 FAMILY TERMS

FABYTE	08B47
FACAL	08A36
FACOMP	10B12
FACOMP/1	08B17
FACOMP/L	08B45
FADIV	07A36
FADIVH	04B18
FADW	08B46
FADW/1	08A35
FAFL	03A10
FAHW	08B36
FAILL	04B45
FAILL/1	30C10
FAIM	08B44
FAIO	07A02
FAIO/1	04B47
FALCF	11A10
FALCFP	09A01
FALOAD	11A28
FALOAD/A	08A02
FALOAD/C	04B25
FAMDS	04B15
FAMDST	30D13
FAMT	03B06
FAMUL	07A35
FAMULNH	04B11
FANIMP	11B46
FAPRIV	08A13
FAPSD	08B10
FARWD	03B35
FAS10	08B18
FASLL	08B35
FASEL	09A13
FASH	07A01
FAST-1	07A45
FAST/A-1	05044
FAST/C	07A46
FAST/L	03B25
FAST/M	10B45
FST/S	03B26
FASTORE	08B06
FASTORE/1	10B01
FASTORE/3	08A15
FASUB	07A34
FAW	07A34
FAWORDW	09A02
FUAIO	03B45
FUANLZ	03B05
FUAWM	03B47
FUBAL	03B46
FUBCR	12C01
FUBCS	03B44
FUBDR	12C45
FUBIR	12035
FUEXU	09B45
FUINT	03B36
FULAD	08A01
FULAWORDW	14F34
FULRP	04B44
FUMH	04B10
FUMI	17A36
FUMMC	03B41
FUMSP	08B11
FUMTHOVER	26N19
FUMTSIGN	18B47
FUPLM	08A46
FUPSW	03B28
FUPLW	03B27
FUS	04B05
FUSE	04B17
FUSEF/1	32E18
FUSIO	28F19
FUWAIT	08A45
FUXW	03B19

SIGMA 5 PHASE LOCATIONS

PCP PHASES

PCP 1	29A02
PCP 2	28A27
PCP 3	28A31
PCP 4	28A30
PCP 5	29A14
PCP 6	28A33

PRE PHASES

PRE 1	31A07
PRE 2	31A27
PRE 3	32A07
PRE 4	31A31

EXECUTION PHASES

PH 1	31A30
PH 2	31A33
PH3	31A02
PH 4	31A04
PH 5	32A27
PH 6	32A31
PH 7	32A30
PH 8	32A33
PH 9	32A02
PH10	32A04

A REGISTER (FF)

	A	NA	Set/A	Reset/A	Extra Set gates	Extra Reset gates
0	3L33	3L40	3L36	3L30	2L-5L	5L
1	3L25	3L26	3L31	3L24	2L-5L	
2	3L19	3L21	3L20	3L17	2L-51	
3	3L05	3L22	3L12	3L03	2L-51	
4	4L33	4L40	4L36	4L30	2L-5L	
5	4L25	4L26	4L31	4L24	2L-5L	
6	4L19	4L21	4L20	4L17	2L-5L	
7	4L05	4L22	4L12	4L03	2L-5L	
8	3M23	3M25	3M12	3M02	2M	
9	3M19	3M21	3M28	3M02	2M	
10	3M31	3M29	3M27	3M02	2M	
11	3M27	3M22	3M35	3M02	2M	
12	4M23	4M25	4M12	4M02	2M	
13	4M19	4M21	4M28	4M02	2M	
14	4M31	4M29	4M37	4M02	2M	
15	4M27	4M22	4M35	4M02	2M	
16	14P23	14P25	14P12	14P02	16P	
17	14P19	14P21	14P28	14P02	16P	
18	14P31	14P29	14P37	14P02	16P	
19	14P27	14P22	14P35	14P02	16P	
20	15P23	15P25	15P12	15P02	16P	
21	15P19	15P21	15P28	15P02	16P	
22	15P31	15P29	15P37	15P02	16P	
23	15P27	15P22	15P35	15P02	16P	
24	14Q23	14Q25	14Q12	14Q02	16Q	
25	14Q19	14Q21	14Q28	14Q02	16Q	
26	14Q31	14Q29	14Q37	14Q02	16Q	
27	14Q27	14Q22	14Q35	14Q02	11Q-16Q	
28	15Q23	15Q25	15Q12	15Q02	13Q-16Q	
29	15Q19	15Q21	15Q28	15Q02	13Q-16Q	
30	15Q31	15Q29	15Q37	15Q02	13Q-16Q	
31	15Q27	15Q22	15Q35	15Q02	13Q-16Q	

ADDER (PR)

	PR
0	25L02
1	25L01
2	26L02
3	26L01
4	27L02
5	27L01
6	28L02
7	28L01
8	25M02
9	25M01
10	26M02
11	26M01
12	27M02
13	27M01
14	28M02
15	28M01
16	2P02
17	2P01
18	3P02
19	3P01
20	4P02
21	4P01
22	5P02
23	5P01
24	2Q02
25	2Q01
26	3Q02
27	3Q01
28	4Q02
29	4Q01
30	5Q02
31	5Q01

ADDER (G)

	G
0	25L06
1	25L04
2	26L06
3	26L04
4	27L06
5	27L04
6	28L06
7	28L04
8	25M06
9	25M04
10	26M06
11	26M04
12	27M06
13	27M04
14	28M06
15	28M04
16	2P06
17	2P04
18	3P06
19	3P04
20	4P06
21	4P04
22	5P06
23	5P04
24	2Q06
25	2Q04
26	3Q06
27	3Q04
28	4Q06
29	4Q04
30	5Q06
31	5Q04

ADDER (K)

	K
0	29K26
1	29K27
2	29K25
3	15N26
4	29K19
5	29K18
6	29K20
7	15N27
8	30K26
9	30K27
10	30K25
11	15N25
12	30K19
13	30K18
14	30K20
15	15N17
16	17N26
17	17N27
18	17N25
19	15N19
20	17N19
21	17N18
22	17N20
23	15N18
24	16N26
25	16N27
26	16N25
27	15N20
28	16N19
29	16N18
30	16N20
31	8P12

B REGISTER (FF)

	B	NB	Set/B	Reset/B	Extra Set terms
0	22L27	22L28	22L50	22L45	21L
1	22L31	22L26	22L46	22L44	21L
2	22L30	22L29	22L41	22L40	21L
3	22L33	22L34	22L39	22L38	21L
4	23L27	23L28	23L50	23L45	21L
5	23L31	23L26	23L46	23L44	21L
6	23L30	23L29	23L41	23L40	21L
7	23L33	23L34	23L39	23L38	21L
8	20M27	20M28	20M50	20M45	19M
9	20M31	20M26	20M46	20M44	19M
10	20M30	20M29	20M41	20M40	19M
11	20M33	20M34	20M39	20M38	19M
12	21M27	21M28	21M50	21M45	19M
13	21M31	21M36	21M46	21M44	19M
14	21M30	21M29	21M41	21M40	19M
15	21M04	21M05	21M03	21M22	19M
16	7P27	7P28	7P50	7P45	9P
17	7P31	7P26	7P46	7P44	9P
18	7P30	7P29	7P41	7P40	9P
19	7P33	7P34	7P39	7P38	9P
20	8P27	8P28	8P50	8P45	9P
21	8P31	8P26	8P46	8P44	9P
22	8P30	8P29	8P41	8P40	9P
23	8P33	8P34	8P39	8P38	9P
24	7Q27	7Q28	7Q50	7Q45	9Q
25	7Q31	7Q26	7Q46	7Q44	9Q
26	7Q30	7Q29	7Q41	7Q40	9Q
27	7Q33	7Q34	7Q39	7Q38	9Q
28	7Q02	7Q21	7Q18	7Q23	9Q
29	7Q04	7Q05	7Q03	7Q22	9Q
30	8Q02	8Q21	8Q18	8Q23	9Q
31	8Q04	8Q05	8Q03	8Q22	9Q

C REGISTER (FB)

	C
0	25L15
1	25L05
2	26L15
3	26L05
4	27L15
5	27L05
6	28L15
7	28L05
8	25M15
9	25M05
10	26M15
11	26M05
12	27M15
13	27M05
14	28M15
15	28M05
16	2P15
17	2P05
18	3P15
19	3P05
20	4P15
21	4P05
22	5P15
23	5P05
24	2Q15
25	2Q05
26	3Q15
27	3Q05
28	4Q15
29	4Q05
30	5Q15
31	5Q05

D REGISTER (FFS)

	D	ND	Set/D	Reset/D
0	25L23	$	$	25L07
1	25L28	$	$	25L07
2	26L23	$	$	26L07
3	26L28	$	$	26L07
4	27L23	$	$	27L07
5	27L28	$	$	27L07
6	28L23	$	$	28L07
7	28L28	$	$	28L07
8	25M23	$	$	25M07
9	25M28	$	$	25M07
10	26M23	$	$	26M07
11	26M28	$	$	26M07
12	27M23	$	$	27M07
13	27M28	$	$	27M07
14	28M23	$	$	28M07
15	28M28	$	$	28M07
16	2P23	$	$	2P07
17	2P28	$	$	2P07
18	3P23	$	$	3P07
19	3P28	$	$	3P07
20	4P23	$	$	4P07
21	4P28	$	$	4P07
22	5P23	$	$	5P07
23	5P28	$	$	5P07
24	2Q23	$	$	2Q07
25	2Q28	$	$	2Q07
26	3Q23	$	$	3Q07
27	3Q28	$	$	3Q07
28	4Q23	$	$	4Q07
29	4Q28	$	$	4Q07
30	5Q23	$	$	5Q07
31	5Q28	$	$	5Q07

DATA AND ADDRESS SWITCHES

	KS		KSP
0	17L01	15	17M44
1	17L02	16	2R01
2	17L03	17	2R02
3	17L04	18	2R07
4	17L07	19	2R08
5	17L08	20	2R44
6	17L09	21	2R43
7	17L42	22	2R40
8	17M01	23	2R09
9	17M02	24	4R01
10	17M03	25	4R02
11	17M04	26	4R07
12	17M07	27	4R08
13	17M08	28	4R44
14	17M09	29	4R09
15	17M42	30	4R40
16	18P01	31	4R43
17	18P02		
18	18P03		
19	18P04		
20	18P07		
21	18P08		
22	18P09		
23	18P42		
24	18Q01		
25	18Q02		
26	18Q03		
27	18Q04		
28	18Q07		
29	18Q08		
30	18Q09		
31	18Q42		

LR LINES (B)

LR28-0	26P14
LR29-0	16N24
LR30-0	15N24
LR31	26P30

MB LINES (BCR)

	BCR/MB
0	12M04
1	12M06
2	12M08
3	12M10
4	12M13
5	12M18
6	12M20
7	12M22
8	12M27
9	12M34
10	12M36
11	12M38
12	12M40
13	27M01
14	25P04
15	25P06
16	25P08
17	25P10
18	25P13
19	25P18
20	25P20
21	25P22
22	25P27
23	25P34
24	25P36
25	25P38
26	25P40
27	25P42
28	18R04
29	18R06
30	18R08
31	18R10

O REGISTER (FF)

	O	NO	S/O	R/O
1	22L04	22L05	22L03	22L22
2	22L02	22L21	22L18	22L23
3	22L06	22L07	$	22L09
4	23L02	23L21	23L18	23L23
5	23L04	23L05	23L03	23L22
6	23L14	23L12	23L11	23L15
7	23L06	23L07	$	23L09

P REGISTER (FF)

	P	NP	Set/P	Reset/P	Extra Set Terms
15	12R33	12R40	12R36	12R30	
16	12R25	12R26	12R31	12R24	
17	12R19	12R21	12R20	12R17	
18	12R05	12R22	12R12	12R03	
19	13R33	13R40	13R36	13R30	
20	13R25	13R26	13R31	13R24	
21	13R19	13R21	13R20	13R17	
22	13R05	13R22	13R12	13R03	
23	14R25	14R26	14R31	14R24	
24	14R19	14R21	14R20	14R17	
25	14R05	14R22	14R12	14R03	17S
26	16R33	16R40	16R36	16R30	
27	16R25	16R26	16R31	16R24	
28	16R19	16R21	16R20	16R17	
29	16R05	16R	16R12	16R03	17S
30	17R33	17R40	17R36	17R30	
31	17R25	17R26	17R31	17R24	
32	17R19	17R21	17R20	17R17	17S
33	17R05	17R22	17R12	17R03	17S

R REGISTER (FF)

	R	NR	Set/R	Reset/R
28	23M33	23M40	23M36	
29	23M25	23M26	23M31	23M24
30	23M19	23M21	23M20	23M17
31	23M05	23M22	23M12	23M03

FAST MEMORY

	RR		RW
0	5K43	0	13L17
1	5K41	1	13L05
2	5K09	2	13L19
3	5K02	3	13L18
4	5K45	4	13L28
5	5K46	5	13L27
6	5K04	6	13L25
7	5K01	7	13L26
8	16K43	8	13L34
9	16K41	9	13L35
10	16K09	10	13L41
11	16K02	11	13L36
12	16K45	12	13L47
13	16K46	13	13L46
14	16K04	14	13L44
15	16K01	15	13L45
16	1S43	16	10S17
17	1S41	17	10S05
18	1S09	18	10S19
19	1S02	19	10S18
20	1S45	20	10S28
21	1S46	21	10S27
22	1S04	22	10S25
23	1S01	23	10S26
24	1T43	24	10S34
25	1T41	25	10S35
26	1T09	26	10S41
27	1T02	27	10S36
28	1T45	28	10S47
29	1T46	29	10S46
30	1T04	30	10S44
31	1T01	31	10S45

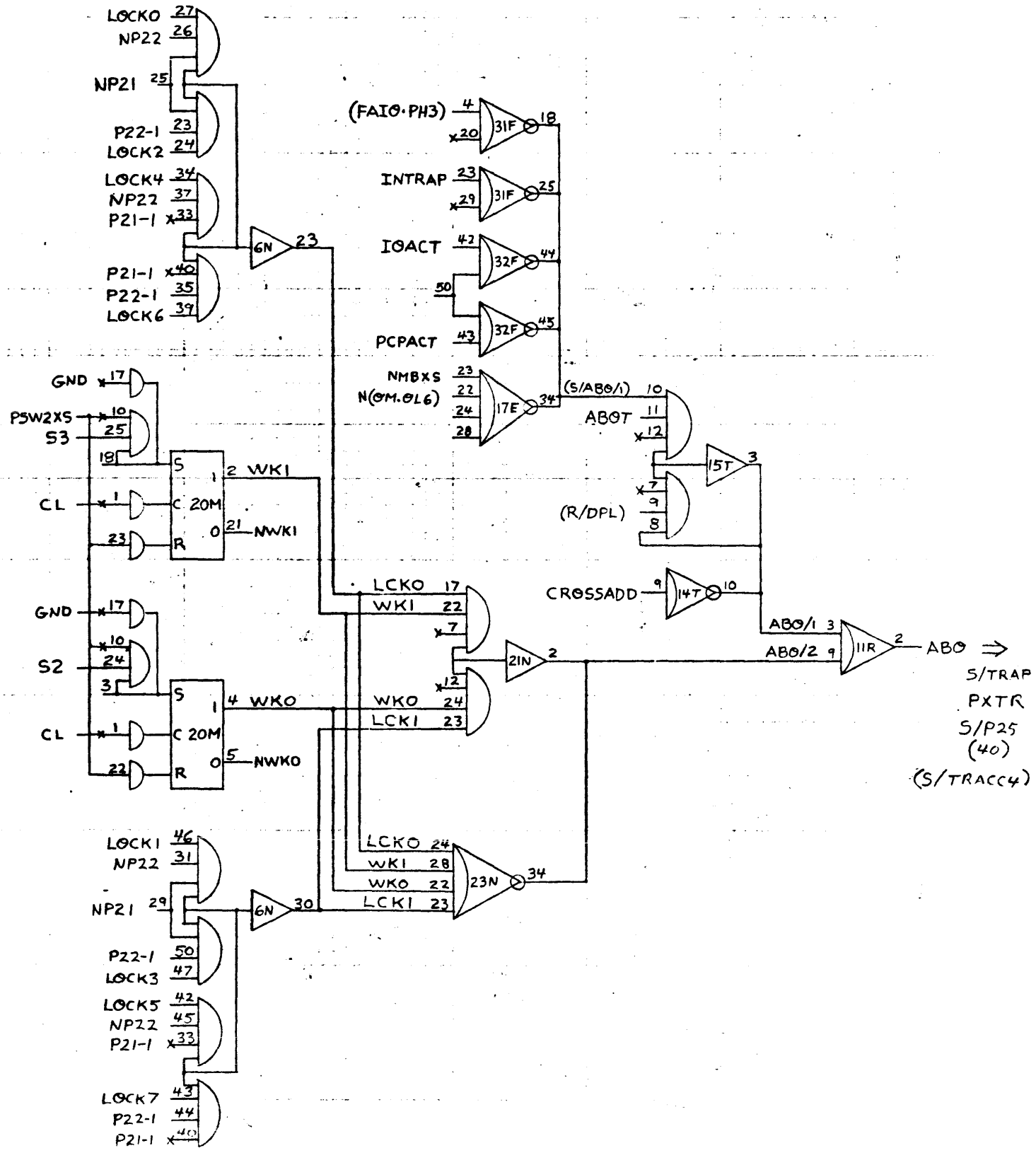
SUM BUSS

	S	Extra Gates
0	25L19	30L
1	25L17	
2	26L19	
3	26L17	
4	27L19	
5	27L17	
6	28L19	
7	28L17	
8	25M19	
9	25M17	
10	26M19	
11	26M17	
12	27M19	
13	27M17	
14	28M19	
15	28M17	
16	02P19	
17	2P17	
18	3P19	
19	3P17	
20	4P19	
21	5P17	
22	5P19	
23	5P17	1Q
24	02Q19	
25	2Q17	
26	3Q19	
27	3Q17	
28	4Q19	
29	4Q17	
30	5Q19	
31	5Q17	8N

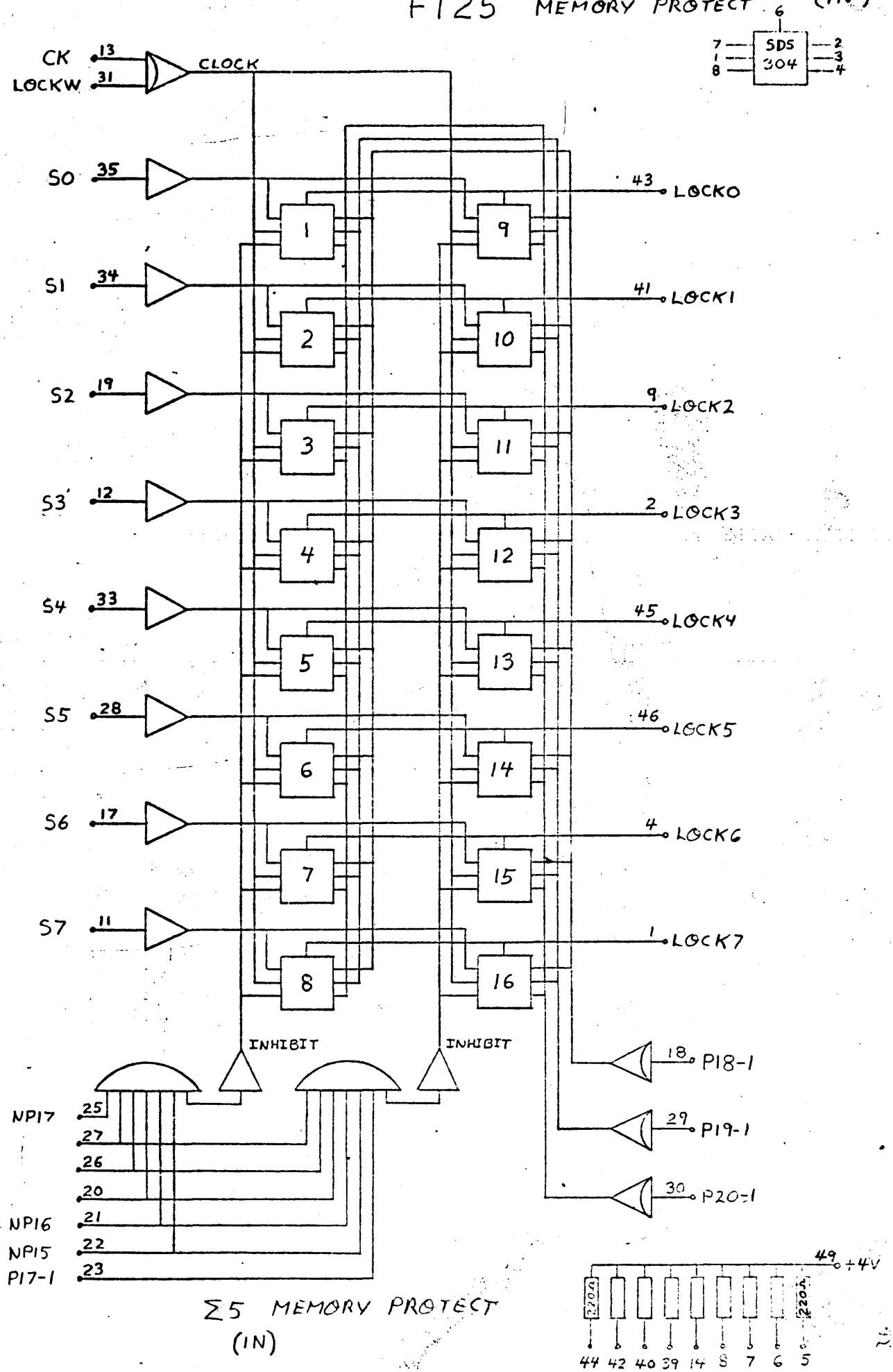
12/30/70
2/22/68
Cochrane

Σ5

MEMORY PROTET VIOLATION
(TRAP TO 40)

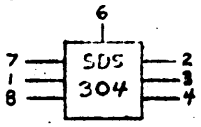


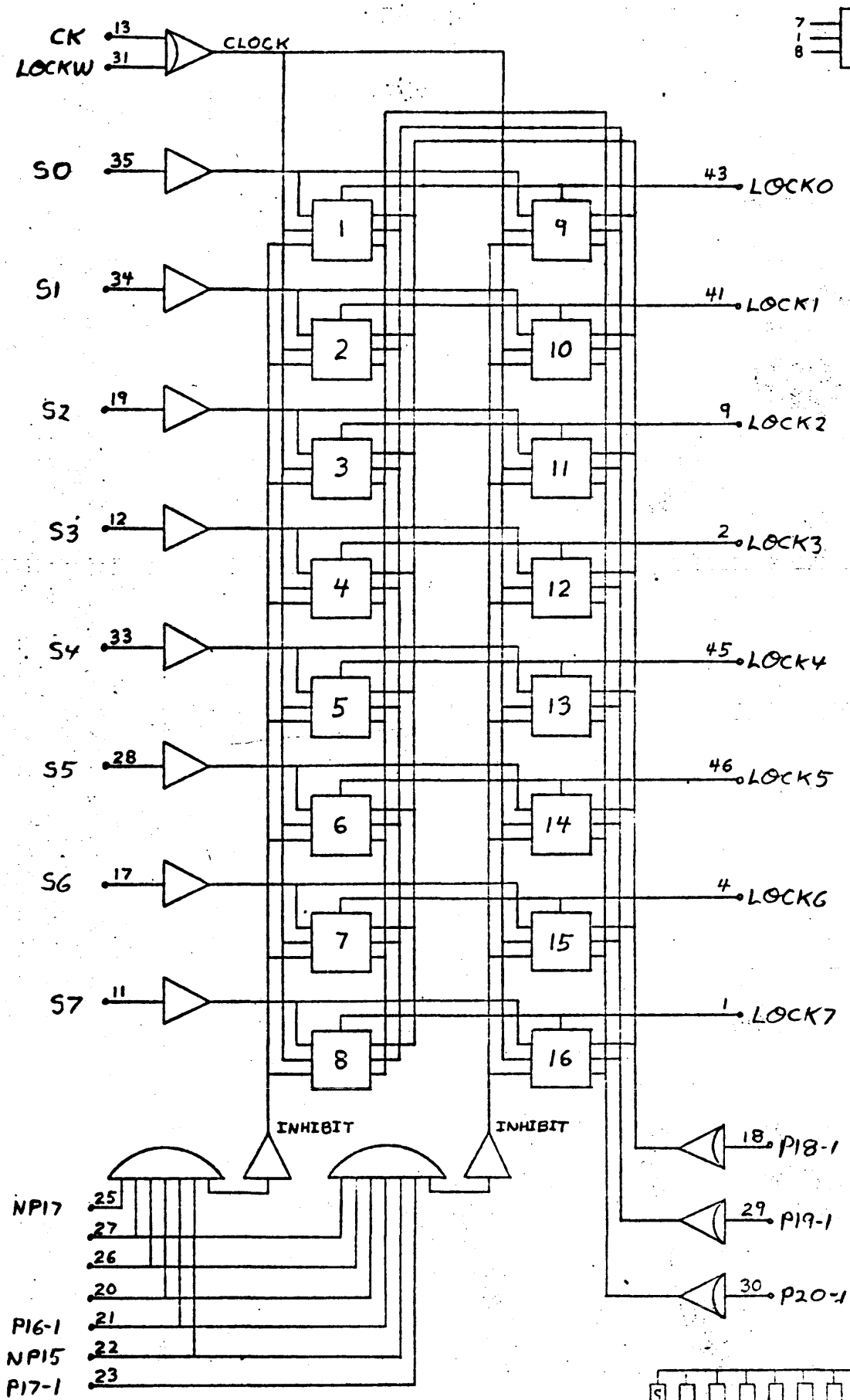
FT25 MEMORY PROTECT (IN)

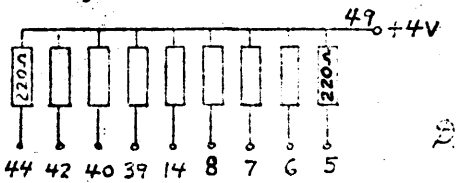


Σ5 MEMORY PROTECT
(IN)

FT25 MEMORY PROTECT (2N)

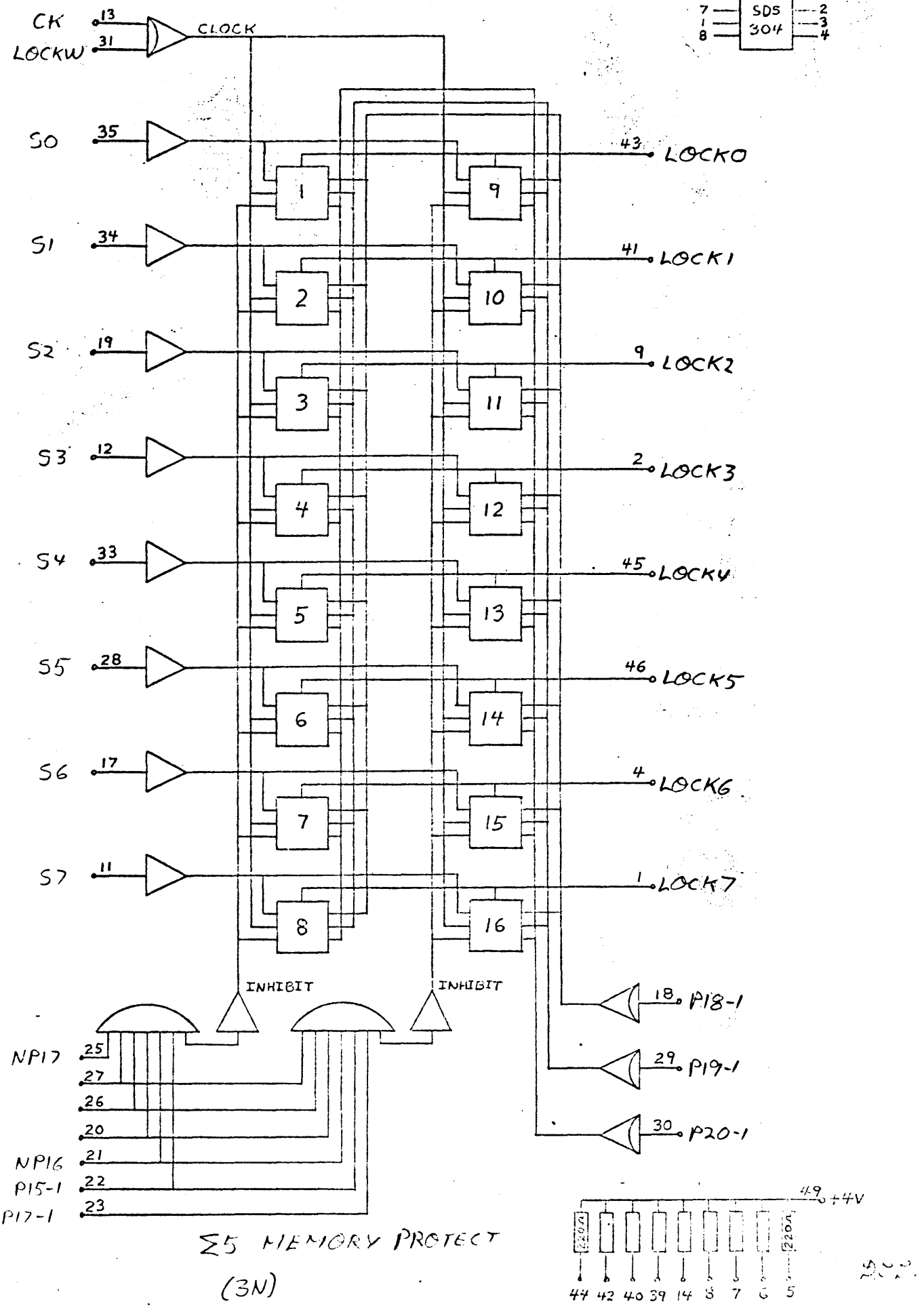






Σ5 MEMORY PROTECT (2N)

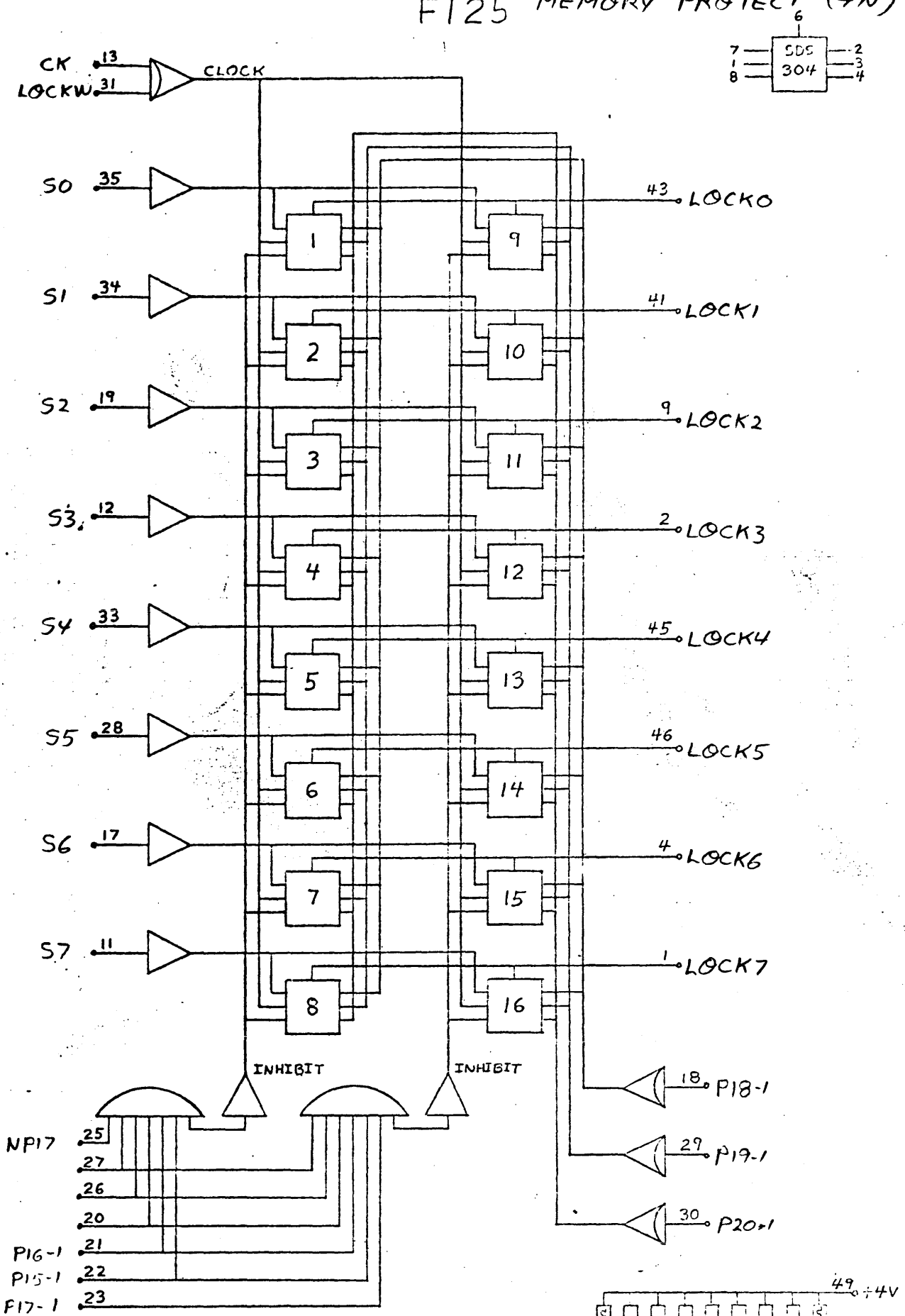
FT25 MEMORY PROTECT (3N)



Σ5 MEMORY PROTECT

(3N)

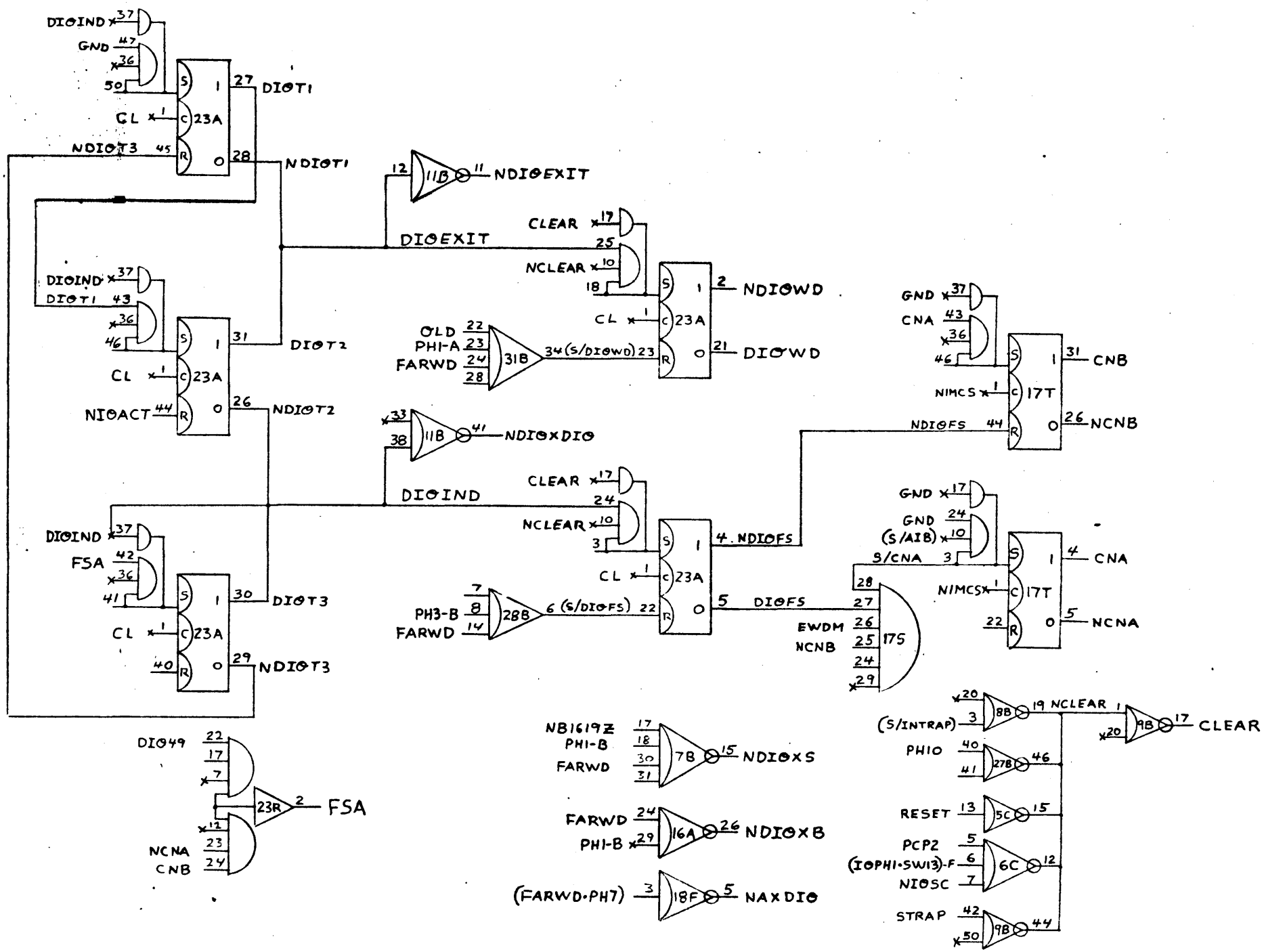
FT25 MEMORY PROTECT (4N)

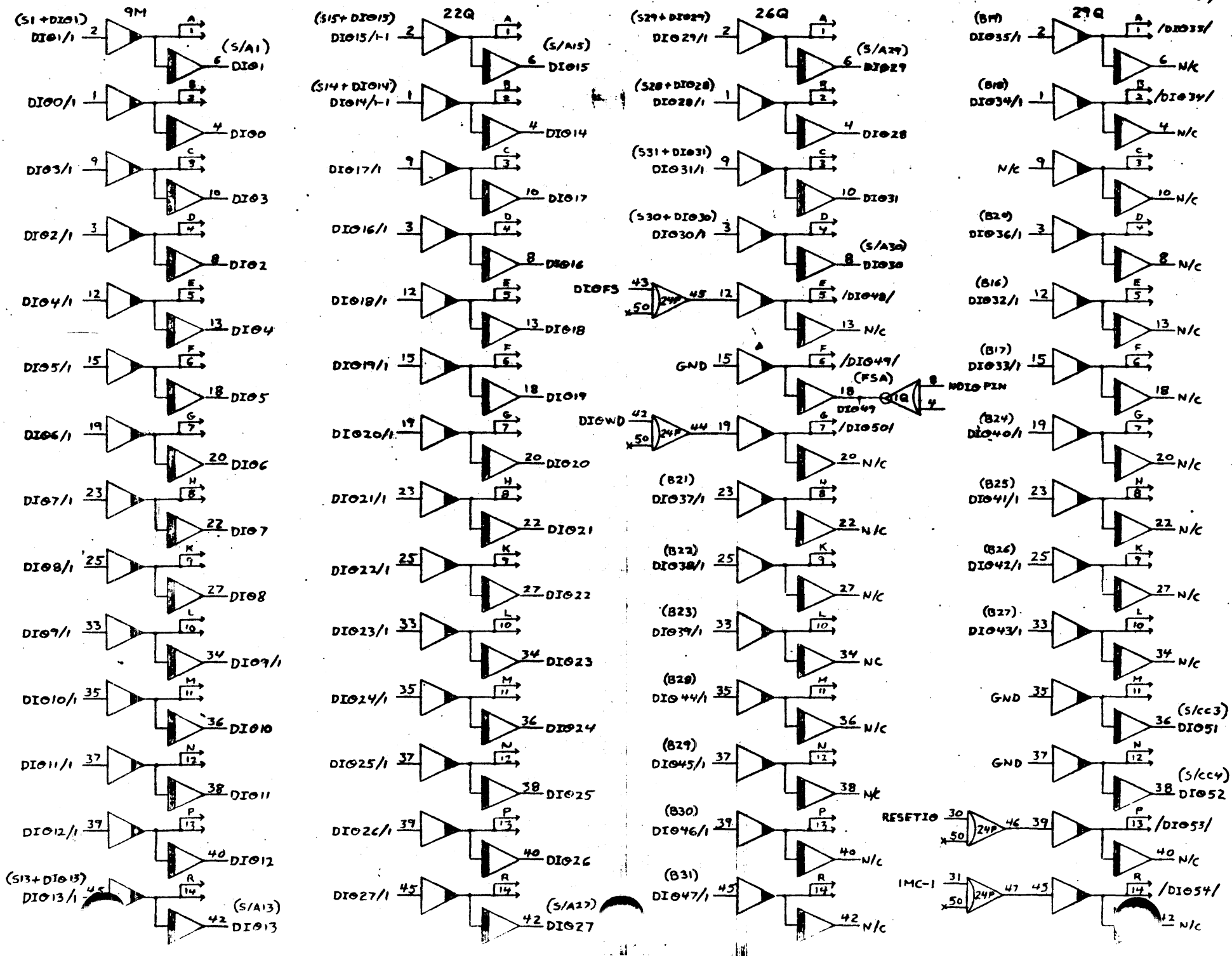


Σ5 MEMORY PROTECT (4N)

Σ5 DIO LOGIC

4/69
Cochrane




1/23/69
9M
(S1 + DIØ1)
DIØ1/1
(S/A1)
DIØ1
DIØØ/1
DIØØ
DIØ3/1
DIØ3
DIØ2/1
DIØ2
DIØ4/1
DIØ4
DIØ5/1
DIØ5
DIØ6/1
DIØ6
DIØ7/1
DIØ7
DIØ8/1
DIØ8
DIØ9/1
DIØ9/1
DIØ10/1
DIØ10
DIØ11/1
DIØ11
DIØ12/1
DIØ12
(S13 + DIØ13)
DIØ13/1
(S/A13)
DIØ13
22Q
(S15 + DIØ15)
DIØ15/1
(S/A15)
DIØ15
(S14 + DIØ14)
DIØ14/1
DIØ14
DIØ17/1
DIØ17
DIØ16/1
DIØ16
DIØ18/1
DIØ18
DIØ19/1
DIØ19
DIØ20/1
DIØ20
DIØ21/1
DIØ21
DIØ22/1
DIØ22
DIØ23/1
DIØ23
DIØ24/1
DIØ24
DIØ25/1
DIØ25
DIØ26/1
DIØ26
DIØ27/1
(S/A27)
DIØ27
26Q
(S29 + DIØ29)
DIØ29/1
(S/A29)
DIØ29
(S28 + DIØ28)
DIØ28/1
DIØ28
(S31 + DIØ31)
DIØ31/1
DIØ31
(S30 + DIØ30)
DIØ30/1
(S/A30)
DIØ30
DIOFS
24P
/DIØ48/
N/c
GND
/DIØ49/
(FSA)
NDIO PIN
DIØ49
DIOWD
24P
/DIØ50/
N/c
(B21)
DIØ37/1
N/c
(B22)
DIØ38/1
N/c
(B23)
DIØ39/1
NC
(B28)
DIØ44/1
N/c
(B29)
DIØ45/1
N/c
(B30)
DIØ46/1
N/c
(B31)
DIØ47/1
N/c
29Q
(BM)
DIØ35/1
/DIØ35/
N/c
(B18)
DIØ34/1
/DIØ34/
N/c
N/c
N/c
(B20)
DIØ36/1
N/c
(B16)
DIØ32/1
N/c
(B17)
DIØ33/1
N/c
(B24)
DIØ40/1
N/c
(B25)
DIØ41/1
N/c
(B26)
DIØ42/1
N/c
(B27)
DIØ43/1
N/c
GND
(S/cc3)
DIØ51
GND
(S/cc4)
DIØ52
RESETIO
24P
/DIØ53/
N/c
IMC-1
24P
/DIØ54/
N/c

Σ5 FLOAT OPTION 8218

COCHRANE

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	XT 10	IT 17	BT 16		IT 25	BT 11		IT 25		IT 25		IT 16	XT 10	BT 10	BT 10	LT 20	LT 20	BT 18	BT 11	IT 16		IT 26	GT 11	FT 22	XT 10		ST 14						A
B	ZT 26 32 L	FT 22	IT 16	IT 16	BT 16	BT 16				IT 16			IT 16	XT 10	FT 26	FT 26	FT 26	FT 26	XT 10	IT 16		LT 42	LT 42	LT 42	LT 18	LT 42	LT 42	LT 42	LT 42	LT 18	LT 42	LT 42	B
C	XT 10	FT 41	FT 22	FT 41	GT 12	FT 41	FT 22	FT 41		GT 12	BT 10	FT 22	FT 41	GT 12	FT 41	FT 41	FT 22	IT 16	GT 12	GT 11	FT 18	FT 22	FT 18	GT 12	FT 18	FT 18	FT 22	XT 10	GT 12	FT 22	GT 12	FT 22	C
D	ZT 23 30 T	LT 42	LT 42	LT 18		LT 42	LT 42	LT 42	LT 42	LT 18	LT 42	LT 42	XT 10	LT 18	LT 42	LT 42	LT 18	LT 42	LT 42	LT 42	XT 10	LT 42	LT 18	LT 42	LT 42	LT 42	LT 42	LT 18	XT 10	LT 18	LT 42	LT 42	D
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

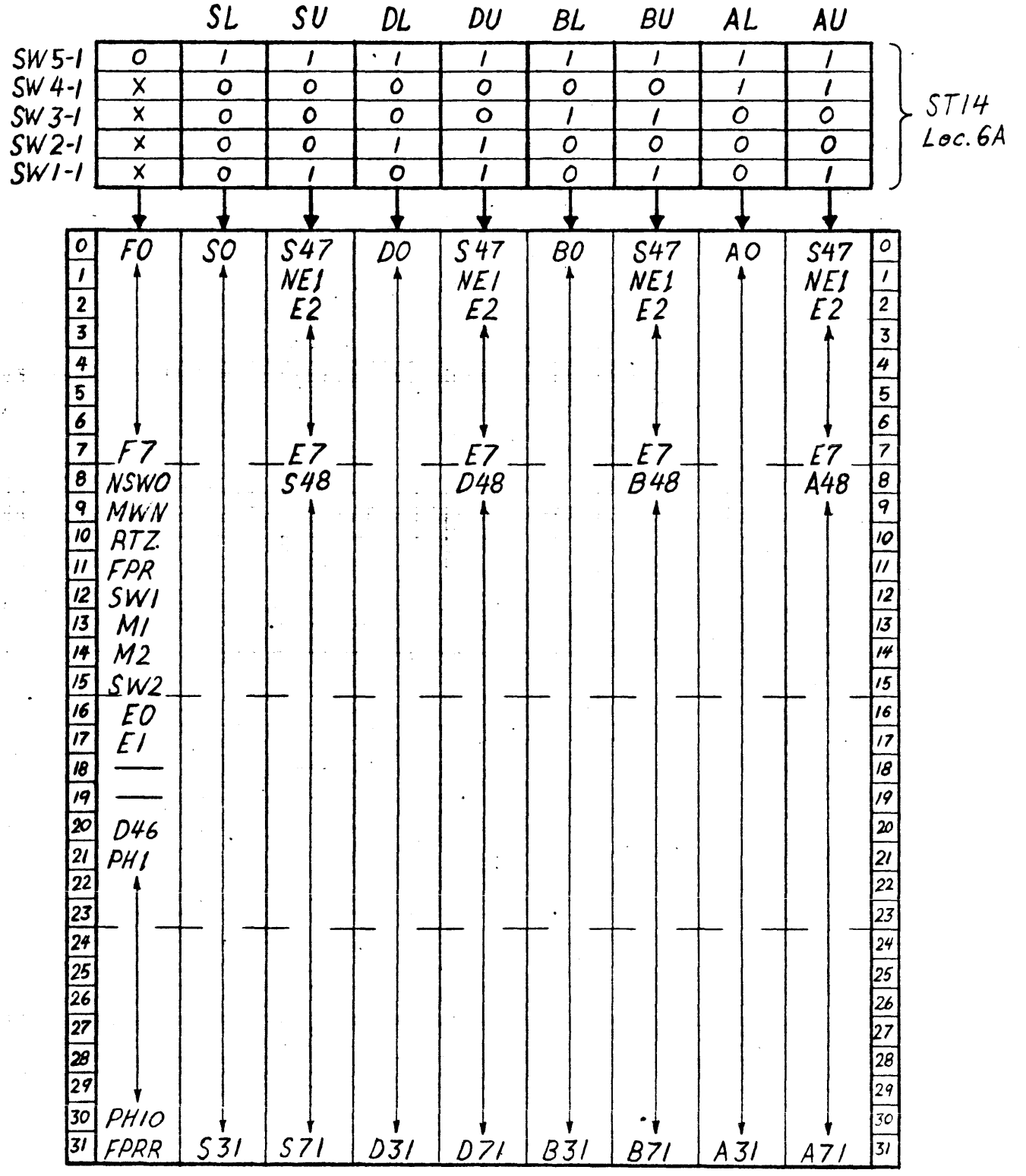
CLOCK WIRES

32D04 –TO– 09A01
06 —— 05B09
08 —— 31B01
10 —— 03C01
17 —— 06C01
19 —— 08C01
21 —— 11C01
24 —— 17C01
33 —— 25C01
36 —— 27C01
43 —— 18D09
32D47 –TO– 31D09

PHASE TEST POINTS

PH1 – 03C06
PH2 – 21C06
PH3 – 26C06
PH4 – 31B27
PH5 – 09A21
PH6 – 09A05
PH7 – 09A12
PH8 – 09A07
PH9 – 30C06
PH10 – 31B06

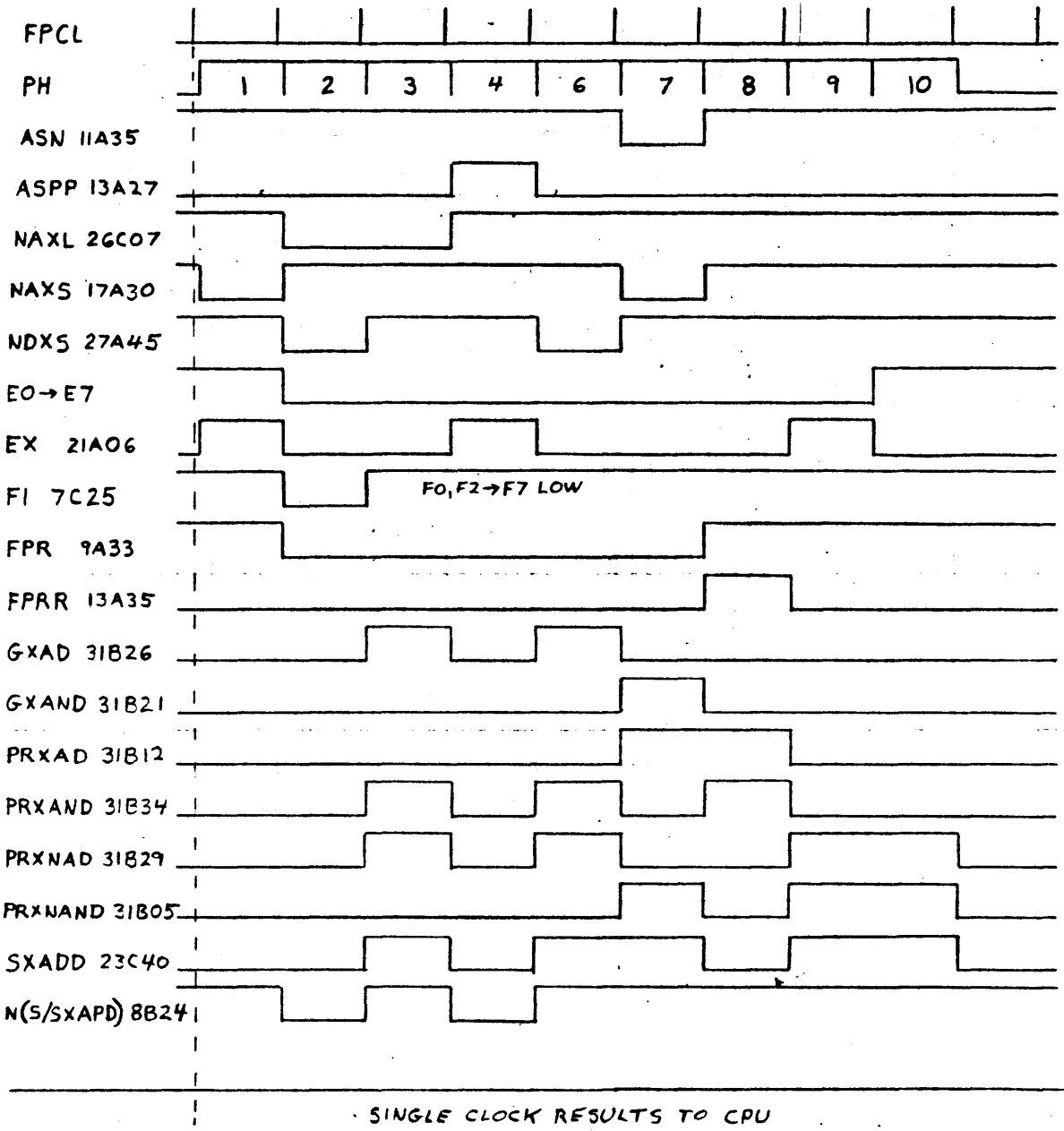
§5 FLOAT SWITCH DISPLAY.



Note: To display FLOAT registers on PCP panel with ST14 switch module, the Register Selection Switch must be on EXT.

EXU. LOC. 140 EXU. LOC. 14

Σ5 FLOAT BOX DIAG. 32C (ID FAL) NEW 5/7 DIAG. 408 (ID FAL)



SINGLE CLOCK RESULTS TO CPU

	SU	SL	40 AU 71	AD AL AS1	DU	DL
PH4 31B27	40000000	00000000	C0AAAAAA	AAAAAAAA	C0AAAAAA	BF800000
PH6 9A05	C0555555	55555554	"	"	"	AAAAAAAA
PH7 9A12	40AAAAAA	AAAAAAAC	40000000	00000000	C0555555	55555554
PH8 9A07	"	"	40AAAAAA	AAAAAAAC	"	"
PH9 30C06	C0555555	55555554	"	"	"	"
PH10 31B06	BF555555	"	3FAAAAAA	"	BF555555	"

Float Add Long Example

SIGMA 5 FLOAT PHASES

FF		NFF		S/FF	R/FF	C/
PH1	3C06	NPH1	3C07	$	09	01
PH2	21C06	NPH2	21C07	$	09	01
PH3	21C06	NPH3	26C07	$	09	01
PH4	31B27	NPH4	31B28	50	45	01
NPH5	9A02	PH5	0A21	18	23	01
NPH6	9A04	PH6	9A05	03	22	01
NPH7	9A14	PH7	9A12	11	15	01
NPH8	9A06	PH8	9A07	$	09	01
PH9	30C06	NPH9	30C07	$	09	01
PH10	31B06	NPH10	31B07	$	09	01

A-REGISTER (FLOAT)

FF		NFF	S/	R/	C/
A0	11C31	26	46	44	01
1	11C30	29	41	40	01
2	11C33	34	39	38	01
3	11C27	28	50	45	01
4	16C30	29	41	40	01
5	16C31	26	46	44	01
6	16C27	28	50	45	01
7	16C33	34	39	38	01
8	16C02	21	18	23	01
9	16C04	05	03	22	01
10	16C14	12	11	15	01
11	21C33	34	39	38	01
12	21C30	29	41	40	01
13	21C31	26	46	44	01
14	21C27	28	30	45	01
15	21C04	05	03	22	01
16	21C02	21	18	23	01
17	21C14	12	11	15	01
18	26C14	12	11	15	01
19	26C33	34	39	38	01
20	26C30	29	41	40	01
21	26C31	26	46	44	01
22	26C27	28	50	45	01
23	26C04	05	03	22	01
24	26C02	21	18	23	01
25	30C14	12	11	15	01
26	30C04	05	03	22	01
27	30C02	21	18	23	01
28	30C30	29	41	40	01
29	30C31	26	46	44	01
30	30C27	28	50	45	01
A31	30C33	34	39	38	01
A47	1C06	07	$	09	01
48	1C02	21	18	23	01
49	1C04	05	03	22	01
50	1C14	12	11	15	01
51	1C33	34	39	38	01
52	1C30	29	41	40	01
53	1C31	26	46	44	01
54	1C27	28	50	45	01
55	3C04	05	03	22	01
56	3C33	34	39	38	01
57	3C02	21	18	23	01
58	3C14	12	11	15	01
59	3C30	29	41	40	01
60	3C31	26	46	44	01
61	3C27	28	50	45	01
62	6C27	28	50	45	01
63	6C04	05	03	22	01
64	6C33	34	39	38	01
65	6C02	21	18	23	01
66	6C14	12	11	15	01
67	6C30	29	41	40	01
68	6C31	26	46	44	01
69	11C04	05	03	22	01
70	11C02	21	18	23	01
A71	11C14	12	11	15	01

ADDER PR (FLOAT)

PR0	8D01
1	8D02
2	9D01
3	9D02
4	11D01
5	11D02
6	13D01
7	13D02
8	14D01
9	14D02
10	15D01
11	15D02
12	17D01
13	17D02
14	18D01
15	18D02
16	21D01
17	21D02
18	22D01
19	22D02
20	24D01
21	24D02
22	25D01
23	25D02
24	26D01
25	26D02
26	27D01
27	27D02
28	30D01
29	30D02
30	31D01
PR31	31D02
PR46	11B01
47	11B02
48	10B01
49	10B02
50	9B01
51	9B02
52	7B01
53	7B02
54	6B01
55	6B02
56	5B01
57	5B02
58	4B01
59	4B02
60	2B01
61	2B02
62	1B01
63	1B02
64	1D01
65	1D02
66	2D01
67	2D02
68	6D01
69	6D02
70	7D01
71	7D02

G0	8D04
1	8D06
2	9D04
3	9D06
4	11D04
5	11D06
6	13D04
7	13D06
8	14D04
9	14D06
10	15D04
11	15D06
12	17D04
13	17D06
14	18D04
15	18D06
16	21D04
17	21D06
18	22D04
19	22D06
20	24D04
21	24D06
22	25D09
23	25D06
24	26D04
25	26D06
26	27D04
27	27D06
28	30D04
29	30D06
30	31D04
G31	31D06
G46	11B04
G47	11B06
48	10B04
49	10B06
50	9B04
51	9B06
52	7B04
53	7B06
54	6B04
55	6B06
56	5B04
57	5B06
58	4B04
59	4B06
60	2B04
61	2B06
62	1B04
63	1B06
64	1D04
65	1D06
66	2D04
67	2D06
68	6D04
69	6D06
70	7D04
71	7D06

K0	10D26
1	10D27
2	10D25
3	9D26
4	10D19
5	10D18
6	10D20
7	19D27
8	16D26
9	16D27
10	16D25
11	19D25
12	16D19
13	16D18
14	16D20
15	19D17
16	23D26
17	23D27
18	23D25
19	19D19
20	23D19
21	23D18
22	23D20
23	19D18
24	29D26
25	29D27
26	29D25
27	19D20
28	29D19
29	29D18
30	29D20
K31	27B27
K46	5D28
47	5D26
48	8B26
49	8B27
50	8B25
51	5D27
52	8B19
53	8B18
54	8B20
55	5D25
56	3B26
57	3B27
58	3B25
59	5D19
60	3B19
61	3B18
62	3B20
63	5D18
64	3D26
65	3D27
66	3D25
67	5D20
68	3D19
69	3D18
70	3D20
71	10D22

B-REGISTER (FLOAT)

FF		NFF	S/	R/	C/
B0	17C41	43	$	42	01
1	17C37	39	$	42	01
2	17C33	35	$	42	01
3	17C29	31	$	42	01
4	17C03	05	$	09	01
5	17C07	15	$	09	01
6	17C17	19	$	09	01
7	17C21	27	$	09	01
8	16C06	07	$	09	01
9	31C03	05	$	09	01
10	31C07	15	$	09	01
11	31C17	19	$	09	01
12	31C21	27	$	09	01
13	29C03	05	$	09	01
14	29C07	15	$	09	01
15	29C17	19	$	09	01
16	29C21	27	$	09	01
17	27C03	05	$	09	01
18	27C07	15	$	09	01
19	27C17	19	$	09	01
20	27C21	27	$	09	01
21	25C03	05	$	09	01
22	25C07	15	$	09	01
23	25C17	19	$	09	01
24	25C21	27	$	09	01
25	20C03	05	$	09	01
26	20C07	15	$	09	01
27	20C17	19	$	09	01
28	20C21	27	$	09	01
29	18C03	05	$	09	01
30	18C07	15	$	09	01
31	18C17	19	$	09	01
B48	31C41	43	$	42	01
49	31C37	39	$	42	01
50	31C33	35	$	42	01
51	31C29	31	$	42	01
52	29C41	43	$	42	01
53	29C37	39	$	42	01
54	29C35	35	$	42	01
55	29C29	31	$	42	01
56	27C41	43	$	42	01
57	27C37	39	$	42	01
58	23C33	35	$	42	01
59	27C29	31	$	42	01
60	25C41	43	$	42	01
61	25C37	39	$	42	01
62	25C33	35	$	42	01
63	25C29	31	$	42	01
64	20C41	43	$	42	01
65	20C37	39	$	42	01
66	20C33	35	$	42	01
67	20C29	31	$	42	01
68	18C41	43	$	42	01
69	18C37	39	$	42	01
70	18C33	35	$	42	01
71	18C29	31	$	42	01

C GATES (FLOAT)

C0	8D05
1	8D15
2	9D05
3	9D15
4	11D05
5	11D15
6	13D05
7	13D15
8	14D05
9	14D15
10	15D05
11	15D15
12	17D05
13	17D15
14	18D05
15	18D15
16	a1D05
17	21D15
18	22D05
19	22D15
20	24D05
21	24D15
22	25D05
23	25D15
24	26D05
25	26D15
26	27D05
27	27D15
28	30D05
29	30D15
30	31D05
31	31D15
C46	11B05
47	11B15
48	10B05
49	10B15
50	9B05
51	9B15
52	7B05
53	7B15
54	6B05
55	6B15
56	5B05
57	5B15
58	4B05
59	4B15
60	2B05
61	2B15
62	1B05
63	1B15
64	1D05
65	1D15
66	2D05
67	2D15
68	6D05
69	6D15
70	7D05
71	7D15

D-REGISTER (FLOAT)

FF		NFF	S/	R/	C/
D0	8D28	$	$	07	09
1	8D23	$	$	07	09
2	9D28	$	$	07	09
3	9D23	$	$	07	09
4	11D28	$	$	07	09
5	11D23	$	$	07	09
6	13D28	$	$	07	09
7	13D23	$	$	07	09
8	14D28	$	$	07	09
9	14D23	$	$	07	09
10	15D28	$	$	07	09
11	15D23	$	$	07	09
12	17D28	$	$	07	09
13	17D23	$	$	07	09
14	18D28	$	$	07	09
15	18D23	$	$	07	09
16	21D28	$	$	07	09
17	21D23	$	$	07	09
18	22D28	$	$	07	09
19	22D23	$	$	07	09
20	24D28	$	$	07	09
21	24D23	$	$	07	09
22	25D28	$	$	07	09
23	25D23	$	$	07	09
24	26D28	$	$	07	09
25	26D23	$	$	07	09
26	27D28	$	$	07	09
27	27D23	$	$	07	09
28	30D28	$	$	07	09
29	30D23	$	$	07	09
30	31D28	$	$	07	09
31	31D23	$	$	07	09
D46	11B28	$	$	07	09
D47	11B23	$	$	07	09
48	10B28	$	$	07	09
49	10B25	$	$	07	09
50	9B28	$	$	07	09
51	9B23	$	$	07	09
52	7B28	$	$	07	09
53	7B35	$	$	07	09
54	6B28	$	$	07	09
55	6B23	$	$	07	09
56	5B28	$	$	07	09
57	%b23	$	$	07	09
58	4B28	$	$	07	09
59	4B23	$	$	07	09
60	2B28	$	$	07	09
61	2B23	$	$	07	09
62	1B28	$	$	07	09
63	1B23	$	$	07	09
64	1D28	$	$	07	09
65	1D23	$	$	07	09
66	2D28	$	$	07	09
67	2D23	$	$	07	09
68	6D28	$	$	07	09
69	6D23	$	$	07	09
70	7D28	$	$	07	09
71	7D23	$	$	07	09

E-REGISTER (FLOAT)

	FF	NFF	S/	R/	C/
E0	8C33	40	36	30	01
E1	8C25	26	31	24	01
E2	8C19	21	20	17	01
E3	8C05	22	12	03	01
E4	10C33	40	36	30	01
E5	10C25	26	31	24	01
E6	10C19	21	20	17	01
E7	10C05	22	12	03	01

F-REGISTER (FLOAT)

FF		NFF	S/	R/	C/
F0	TC33	40	36	30	01
F1	TC25	26	31	24	01
F2	7C19	21	20	17	01
F3	7C05	22	12	03	01
F4	12C33	40	36	30	01
F5	12C25	26	31	24	01
F6	12C19	21	20	17	01
F7	12C05	22	12	03	01

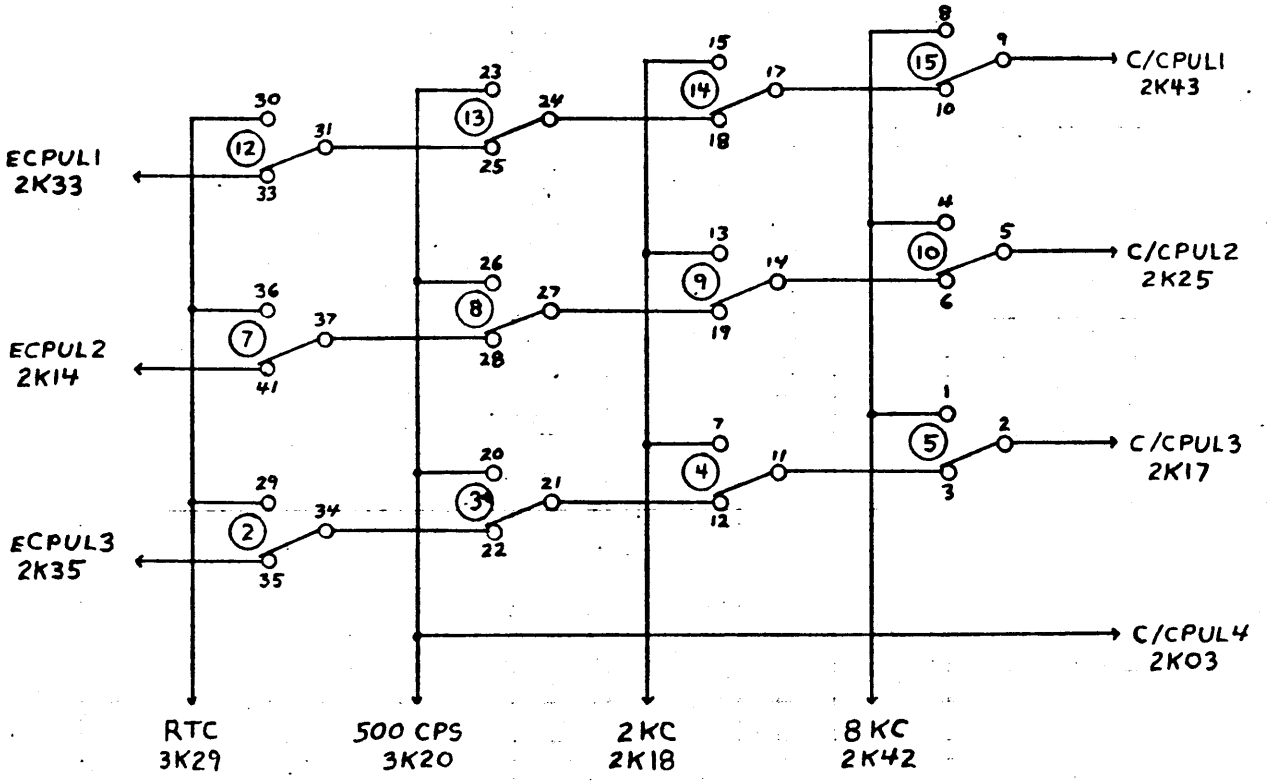
FP GATES (FLOAT)

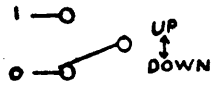
FP0	15B37
1	15B33
2	15B34
3	15B35
4	15B18
5	15B13
6	15B14
7	15B15
8	16B37
9	16B33
10	16B34
11	16B35
12	16B18
13	16B13
14	16B14
15	16B15
16	17B37
17	17B33
18	17B34
19	17B35
20	17B18
21	17B13
22	17B14
23	17B15
24	18B37
25	18B33
26	18B34
27	18B35
28	18B18
29	18B13
30	18B14
FP31	18B15

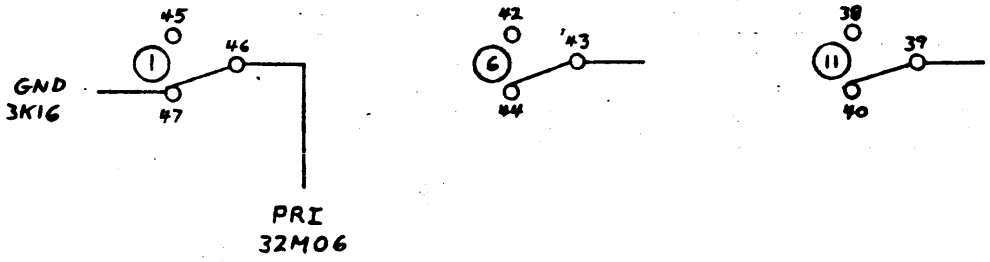
S0	8D17
1	8D19
2	9D17
3	9D19
4	11D17
5	11D19
6	13D17
7	13D19
8	14D17
9	14D19
10	15D17
11	15D19
12	17D17
13	17D19
14	18D17
15	18D19
16	21D17
17	21D19
18	22D17
19	22D19
20	24D17
21	24D19
22	25D17
23	25D19
24	26D17
25	26D19
26	27D17
27	27D19
28	30D17
29	30D19
30	31D17
S31	31D19
S46	11B17
47	11B19
48	10B17
49	10B19
50	9B17
51	9B19
52	7B17
53	7B19
54	6B17
55	6B19
56	5B17
57	5B19
58	4B17
59	4B19
60	2B17
61	2B19
62	1B17
63	1B19
64	1D17
65	1D19
66	2D17
67	2D19
68	6D17
69	6D19
70	7D17
S71	7D19

Σ5

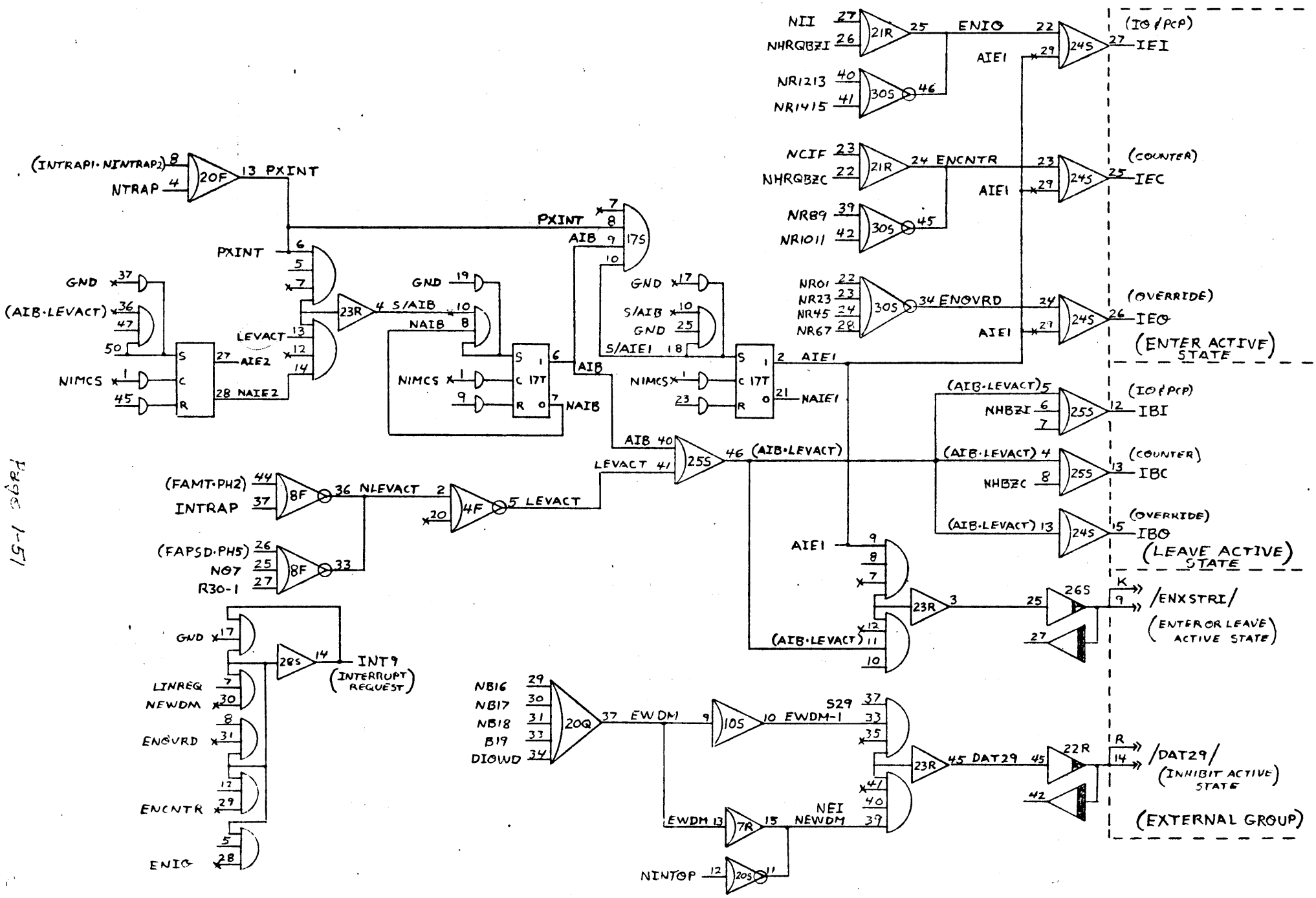
SW. REAL TIME CLOCK MODULE ST14 (3K)







Σ5 CPU INTERRUPT SERVICE LOGIC



CPU INTERRUPT SERVICE LOGIC

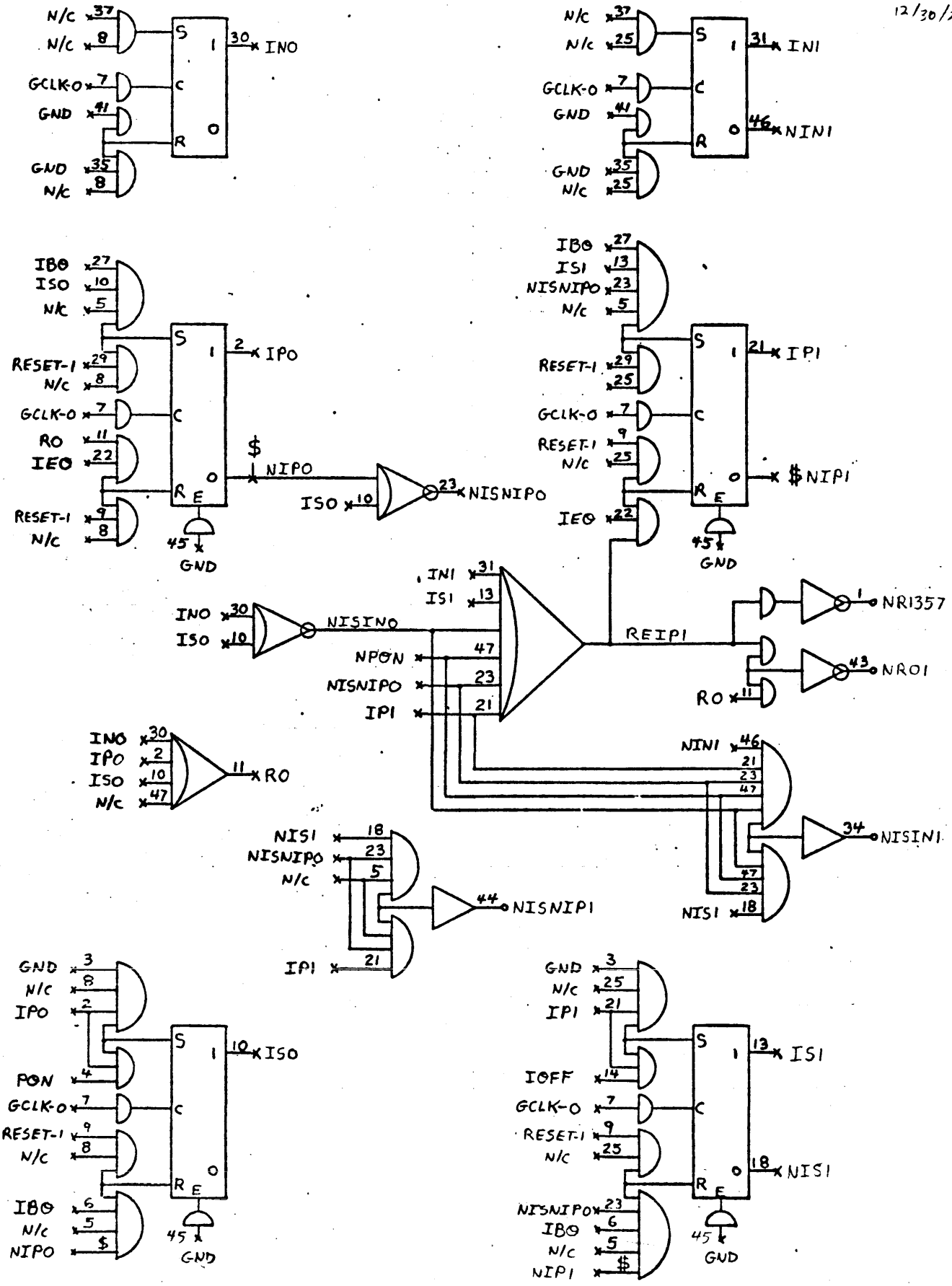
LTI6 INTERRUPT

≤5 (25R.)

POWER FAIL SAFE

OVERRIDE GROUP

12/30/70



POWER ON [50]

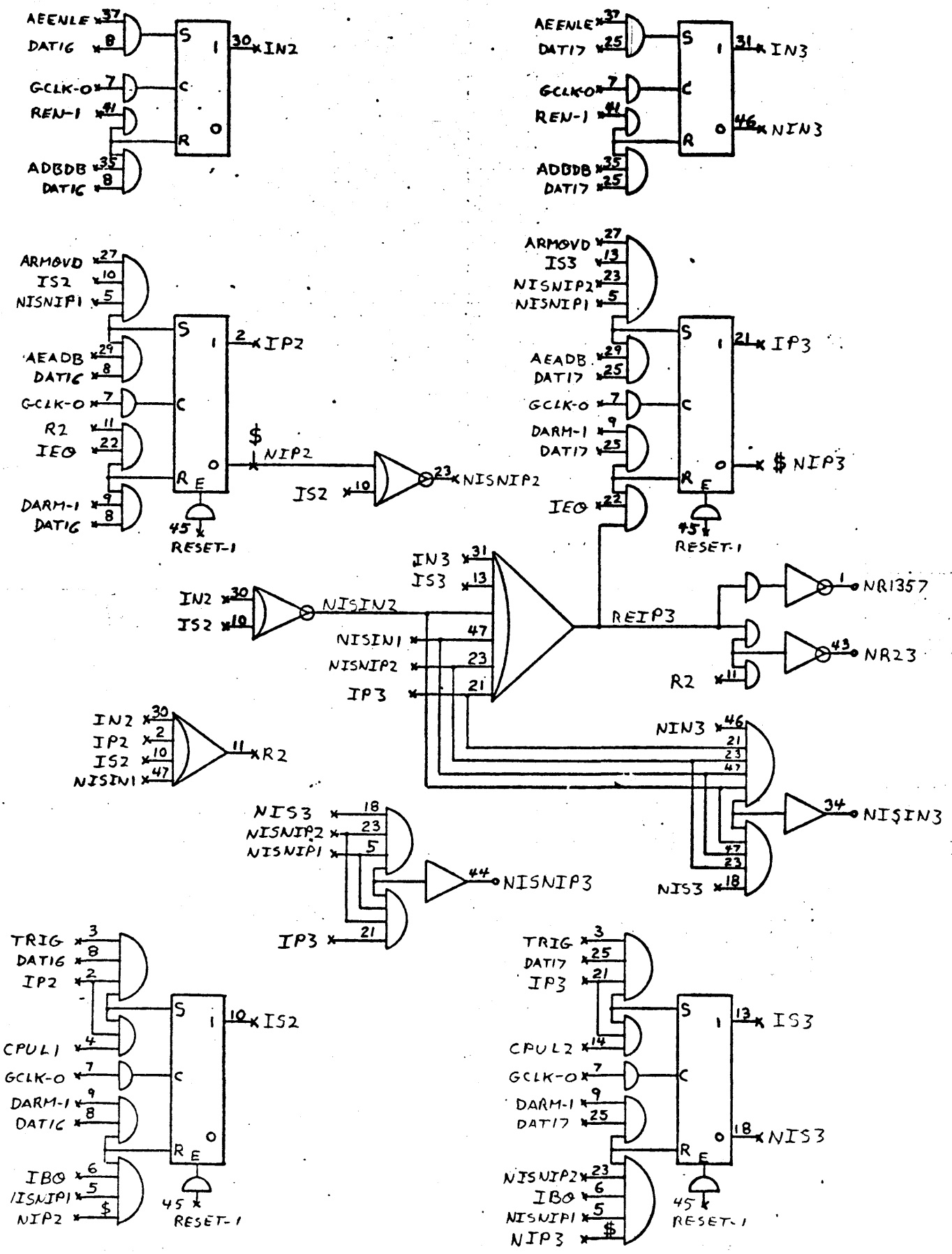
≤5 (25R)

POWER OFF [51]

LTI6 INTERRUPT ≤5(2GR)

OVERRIDE GROUP

Cochrane



COUNTER #1

[52]

≤5 (2GR)

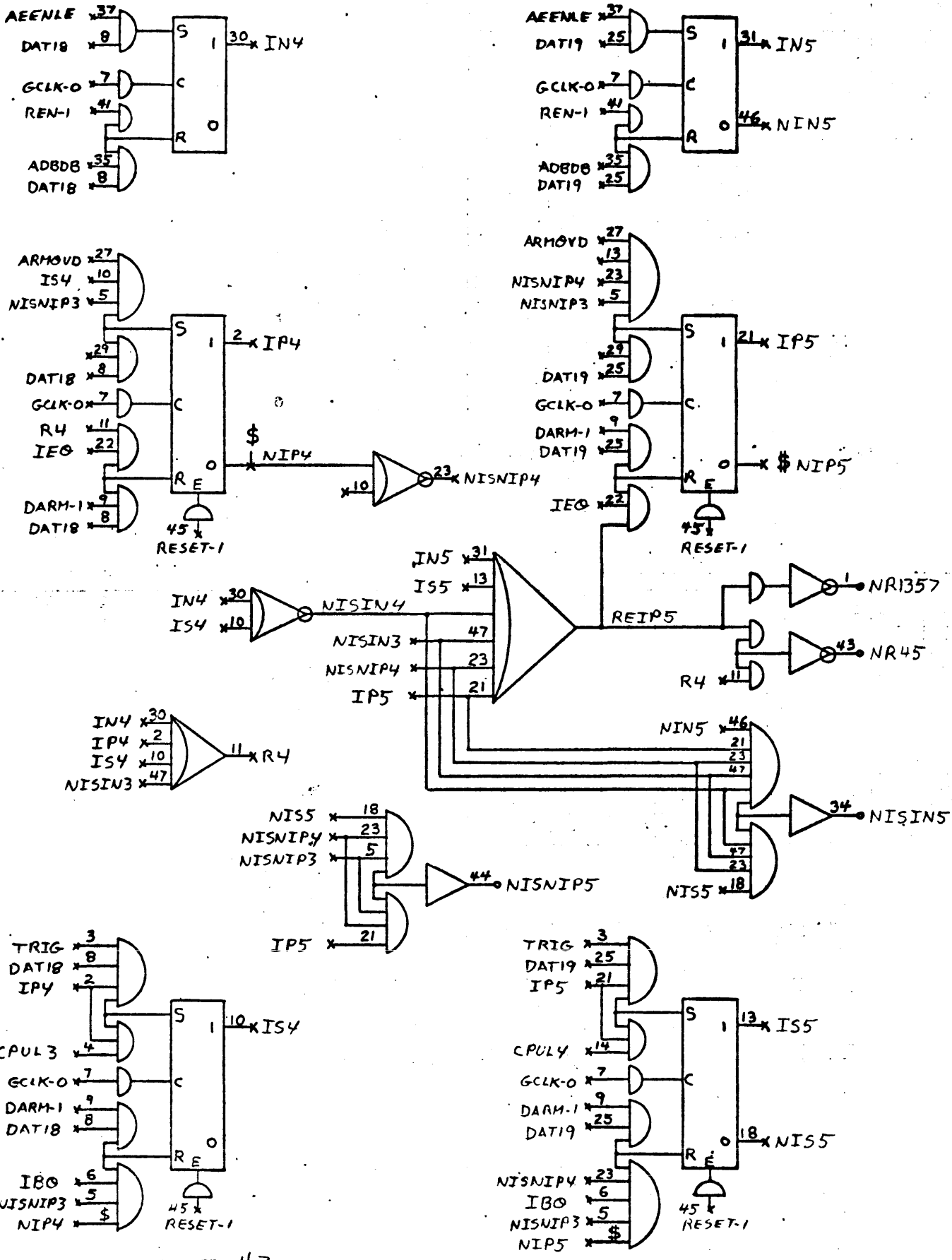
OPTIONAL

COUNTER #2

[53]

LTI6 INTERRUPT Σ5 (27R)

OVERRIDE GROUP



COUNTER #3 [54]

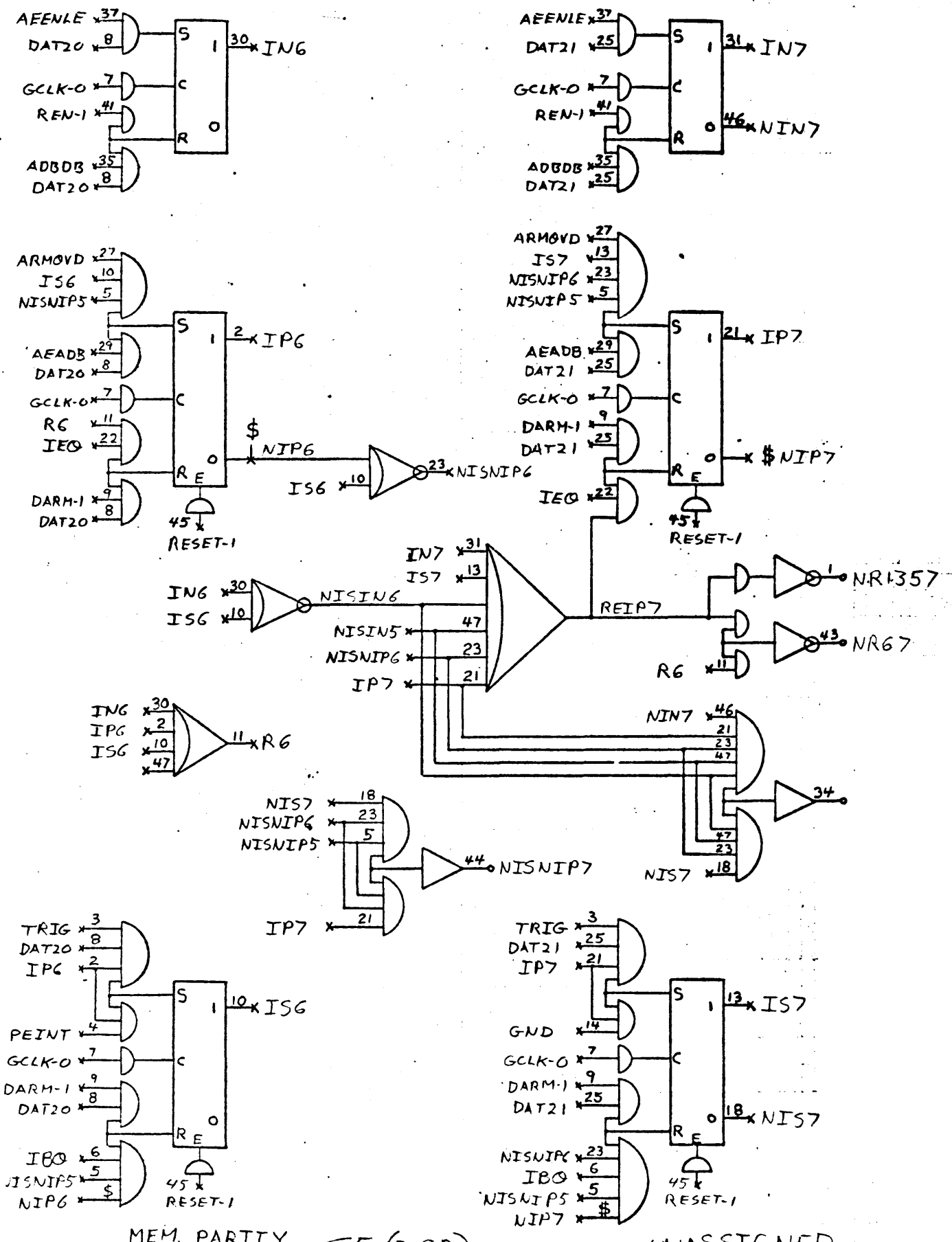
Σ5 (27R)

COUNTER #4 [55]

LTI6 INTERRUPT

Σ5 (28R)

OVERRIDE GROUP



MEM. PARITY

[56]

Σ5 (28R)

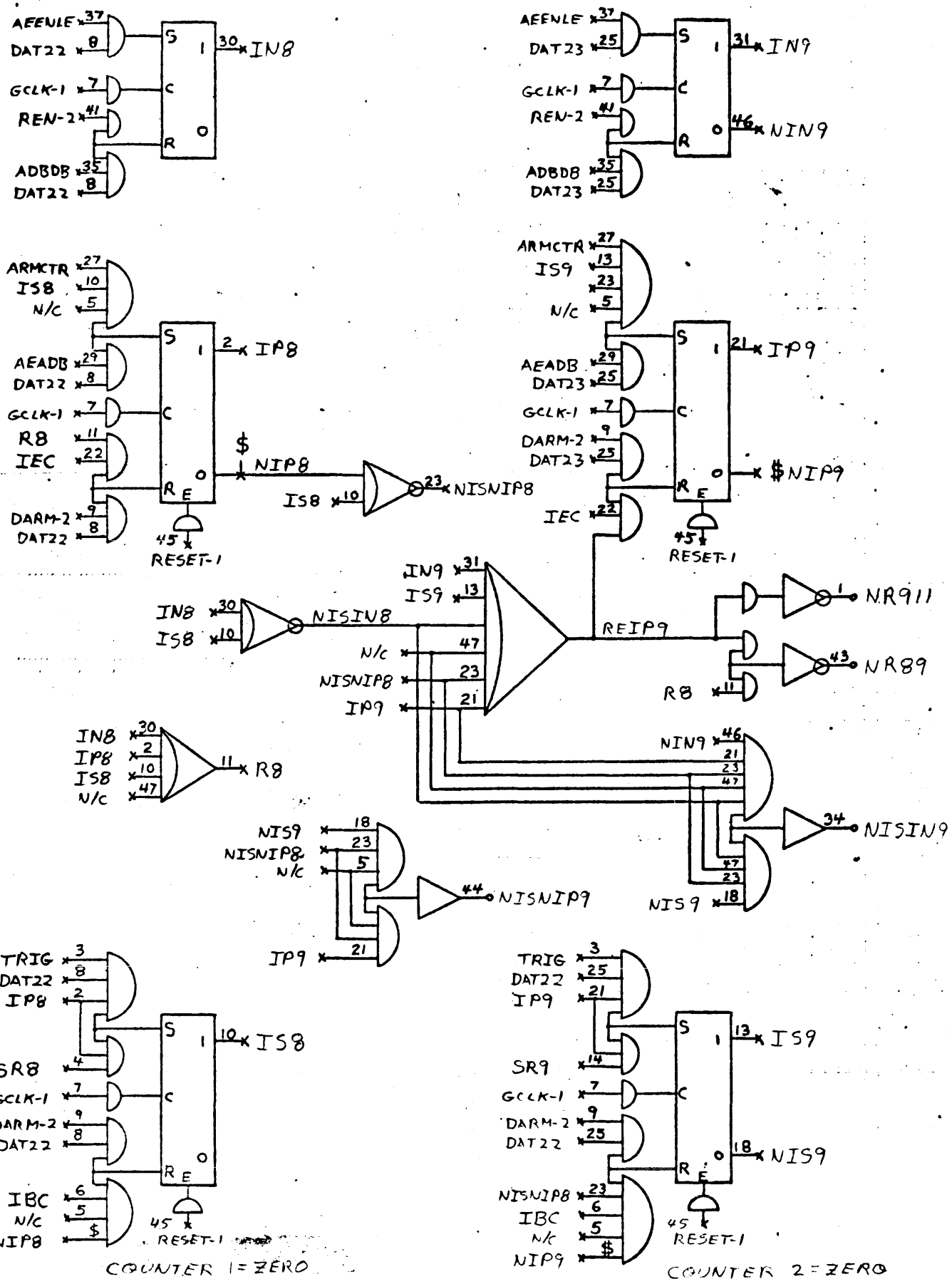
UNASSIGNED

[57]

LTI6 INTERRUPT ≤5 (29K)

COUNTER GROUP

Cochrane



COUNTER 1=ZERO

COUNTER 2=ZERO

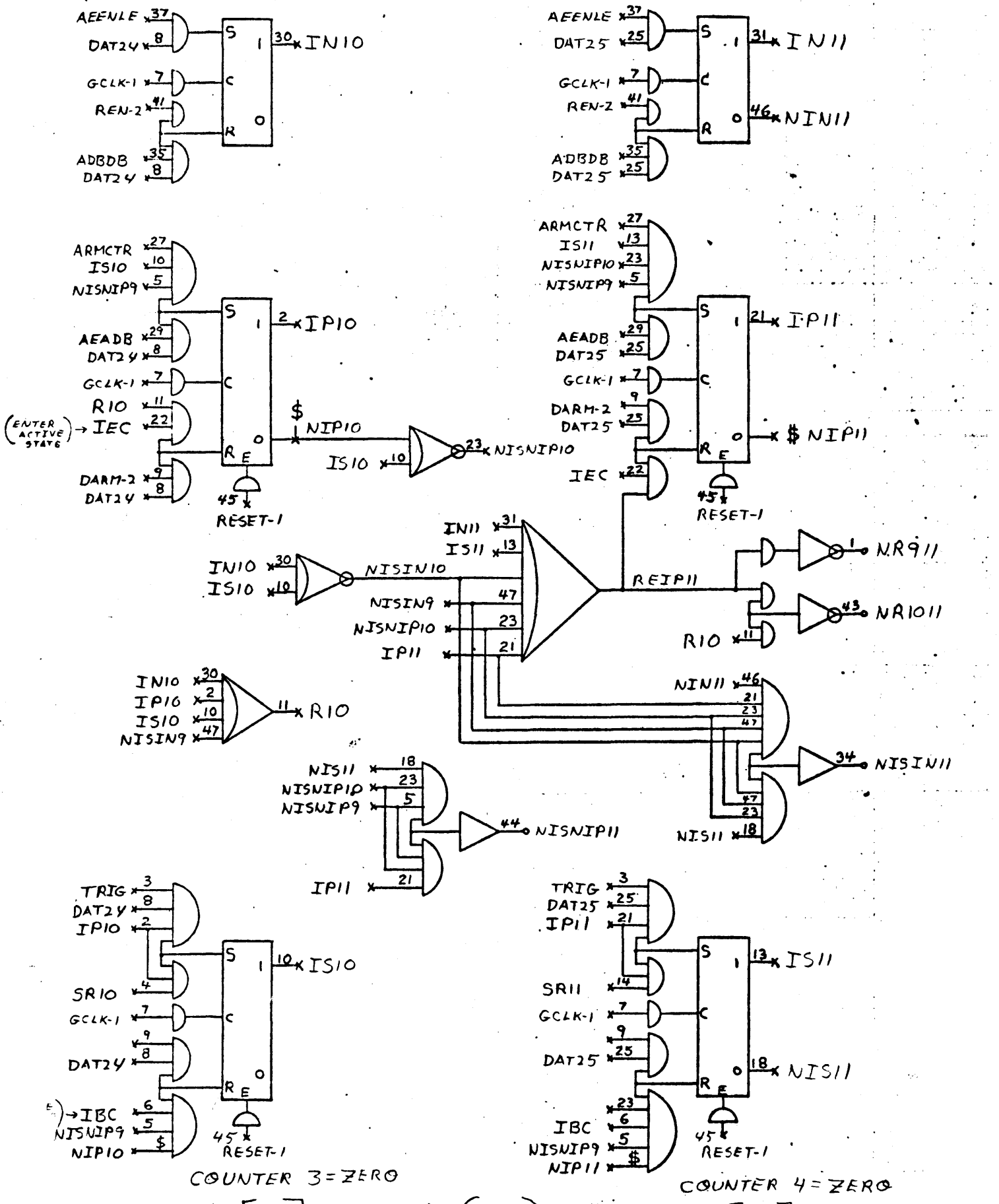
[58] ≤5 (29K) [59]

OPTIONAL

LTI6 INTERRUPT Σ5 (30R)

(COUNTER GROUP)

Cochrane



COUNTER 3 = ZERO

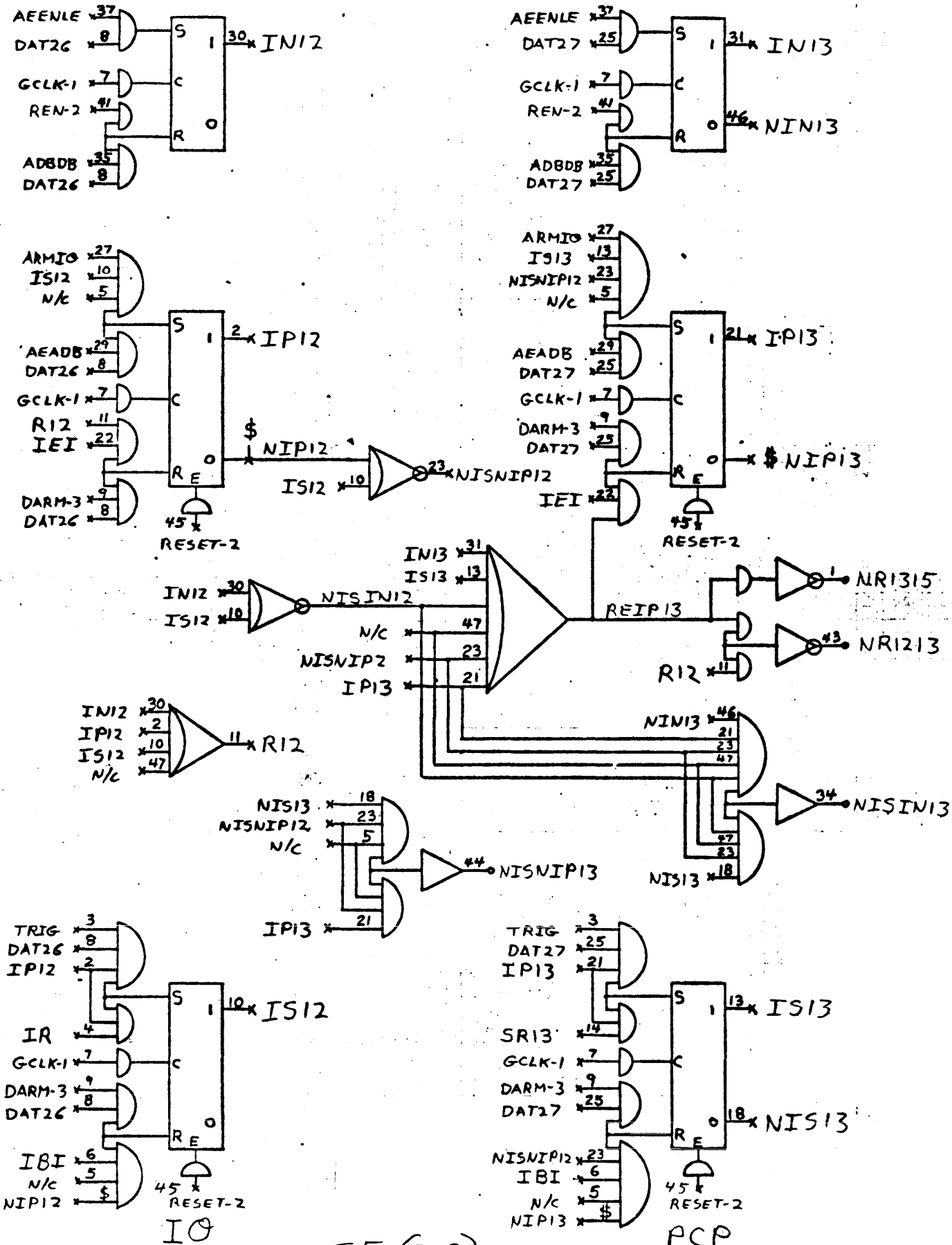
COUNTER 4 = ZERO

[5A] Σ5 (30R) [5B]

LTI6 INTERRUPT ≤5 (31R)

INPUT/OUTPUT GROUP

Cochrane



IO

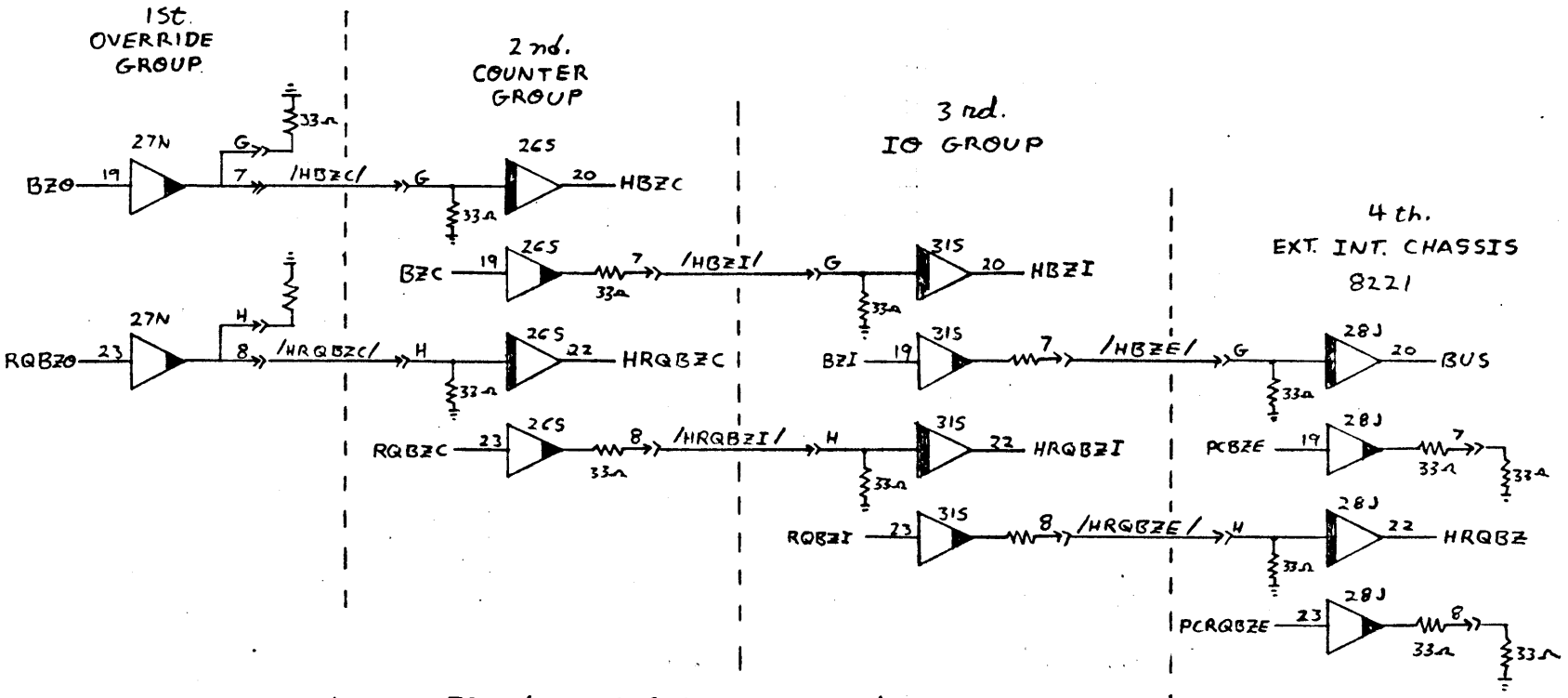
[5C]

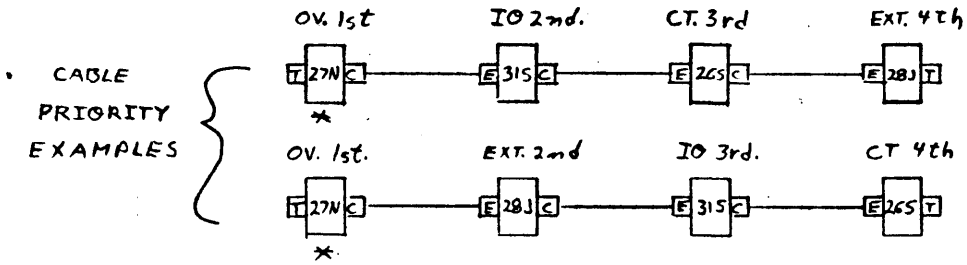
≤5 (31R)

PCP

[5D]

INTERRUPT PRIORITY CHAIN Σ5

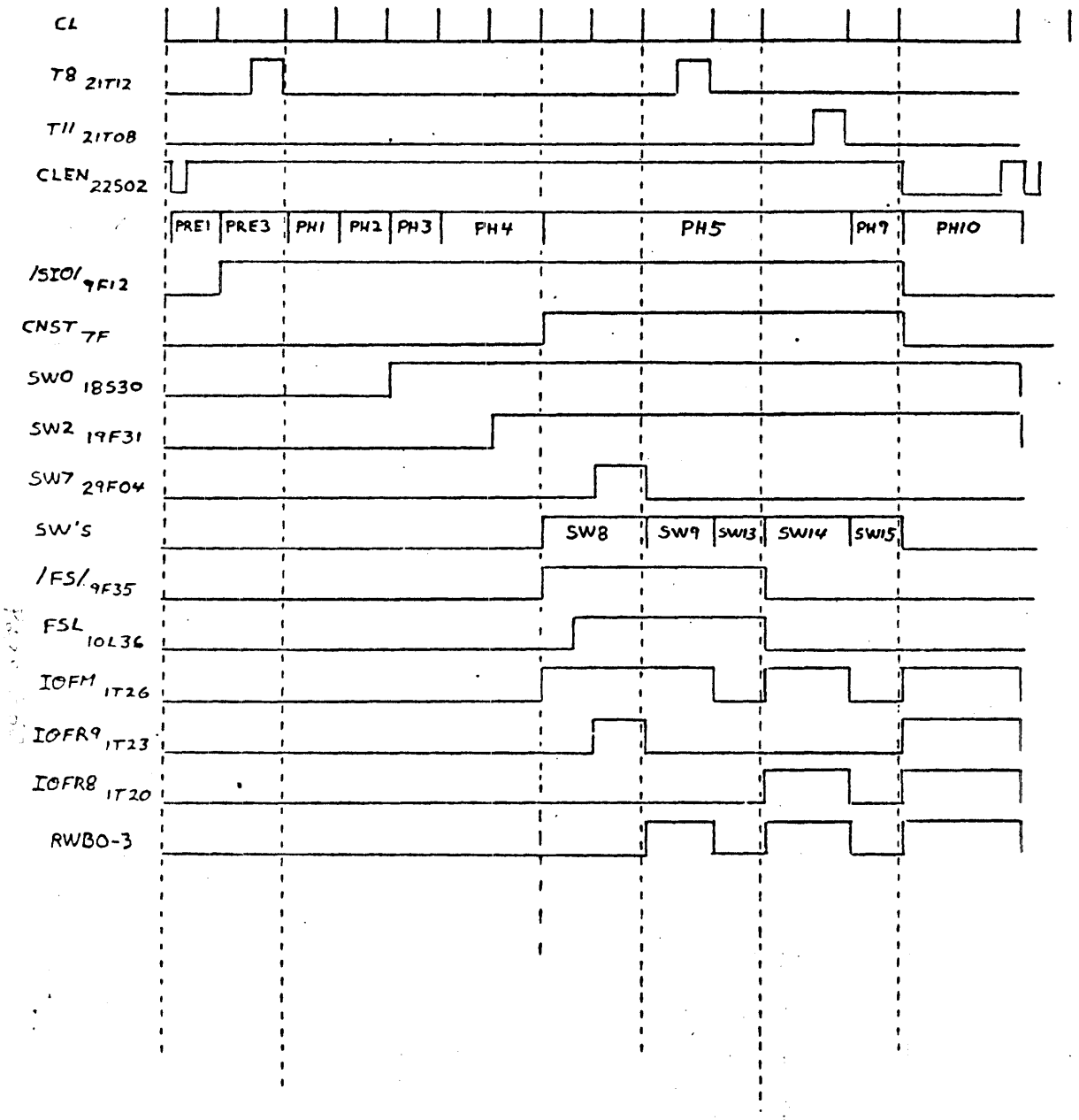




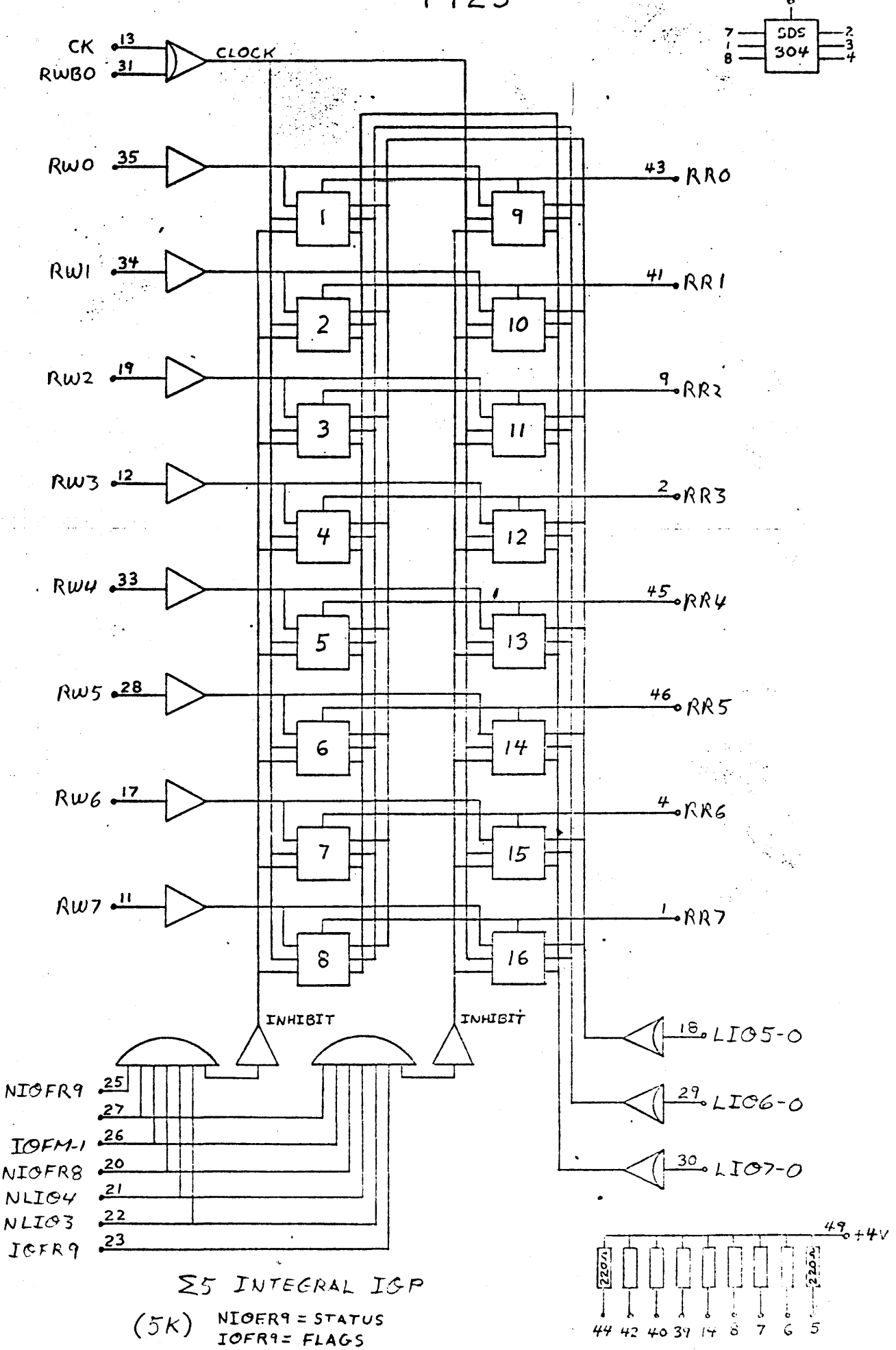
* NOTE
OVERRIDE GROUP
ALWAYS FIRST PRIORITY

Cochran

Σ5 IIOP SIO TIMING



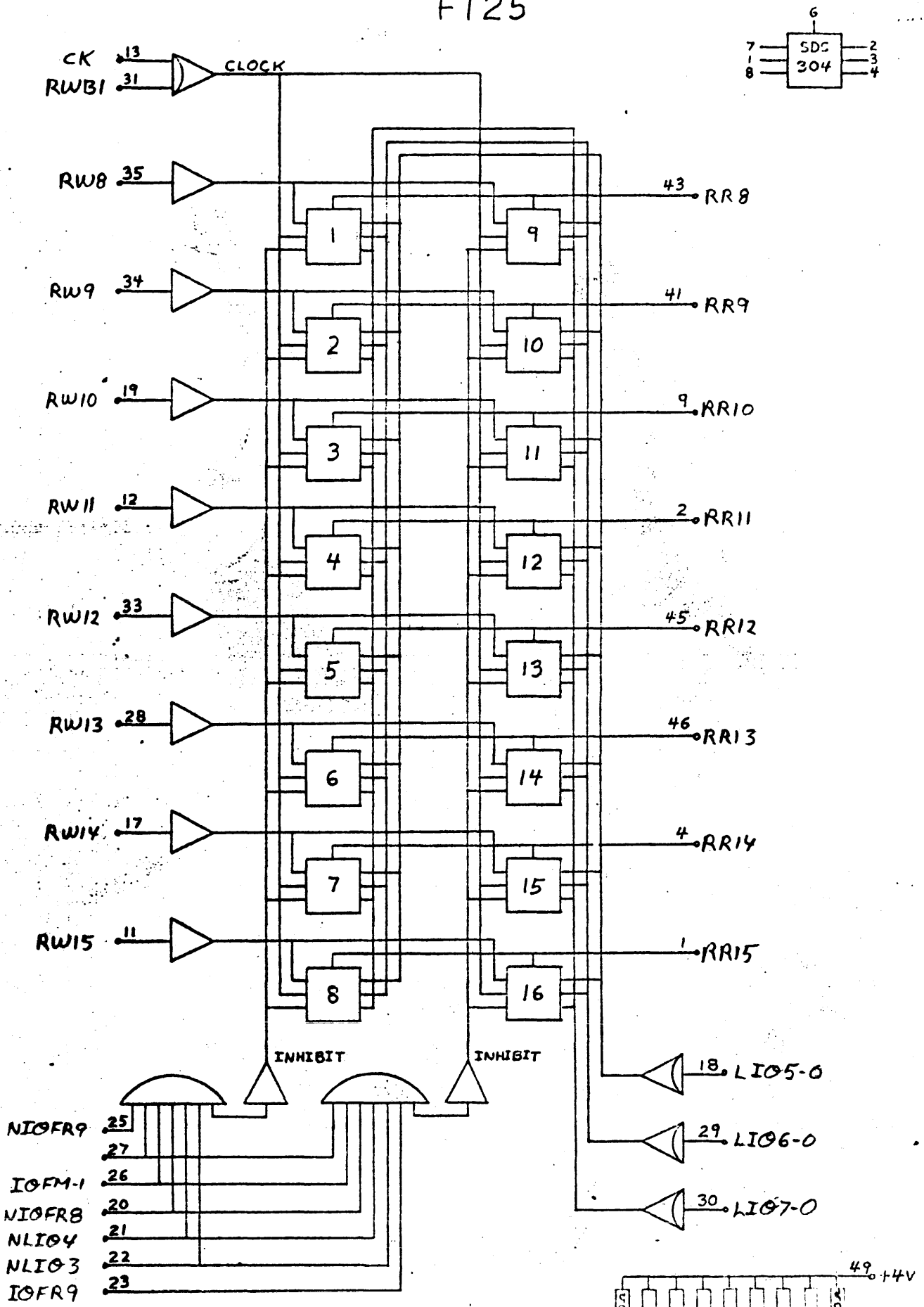
FT25 INTEGRAL IOP (5K)



Σ5 INTEGRAL IOP

(5K) NIOFR9 = STATUS
IOFR9 = FLAGS

FT25 INTEGRAL IOP 23K



Σ5 INTEGRAL IOP

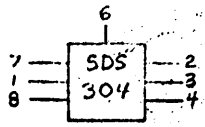
(23K)

NIOFR9 = STATUS

IOFR9 = LSB BYTE ADDR BIT RR8/RR9 → P32 & P33

FT25

INTEGRAL IOP (15)



CK 13
RWB2 31
CLOCK

RW16 35
RW17 34
RW18 19
RW19 12
RW20 33
RW21 28
RW22 17
RW23 11

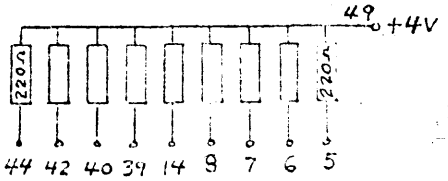
1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16

43 RR16
41 RR17
9 RR18
2 RR19
45 RR20
46 RR21
4 RR22
1 RR23

INHIBIT
INHIBIT

18 LIO5-1
29 LIO6-1
30 LIO7-1

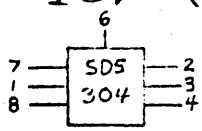
NIOFR7-1 25
27
IOFM 26
NIOFR8-1 20
NLIO4-1 21
NLIO3-1 22
IOFR9-1 23

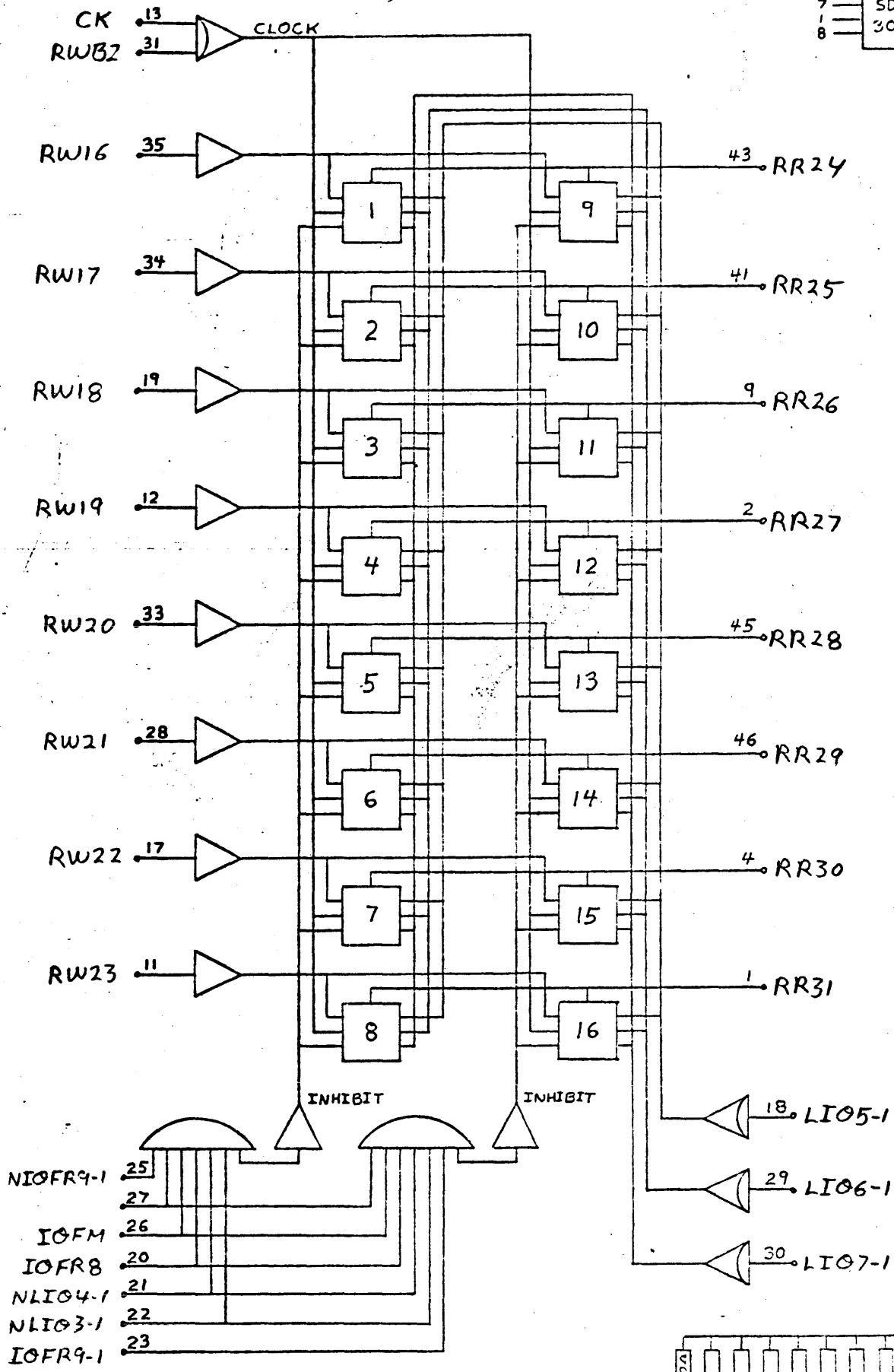


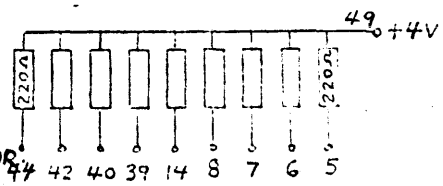
Σ5 INTEGRAL IOP

(15) NIOFR9 = BYTE ADDRESS
IOFR9 = BYTE COUNT

FT25 INTEGRAL IOP (IT)



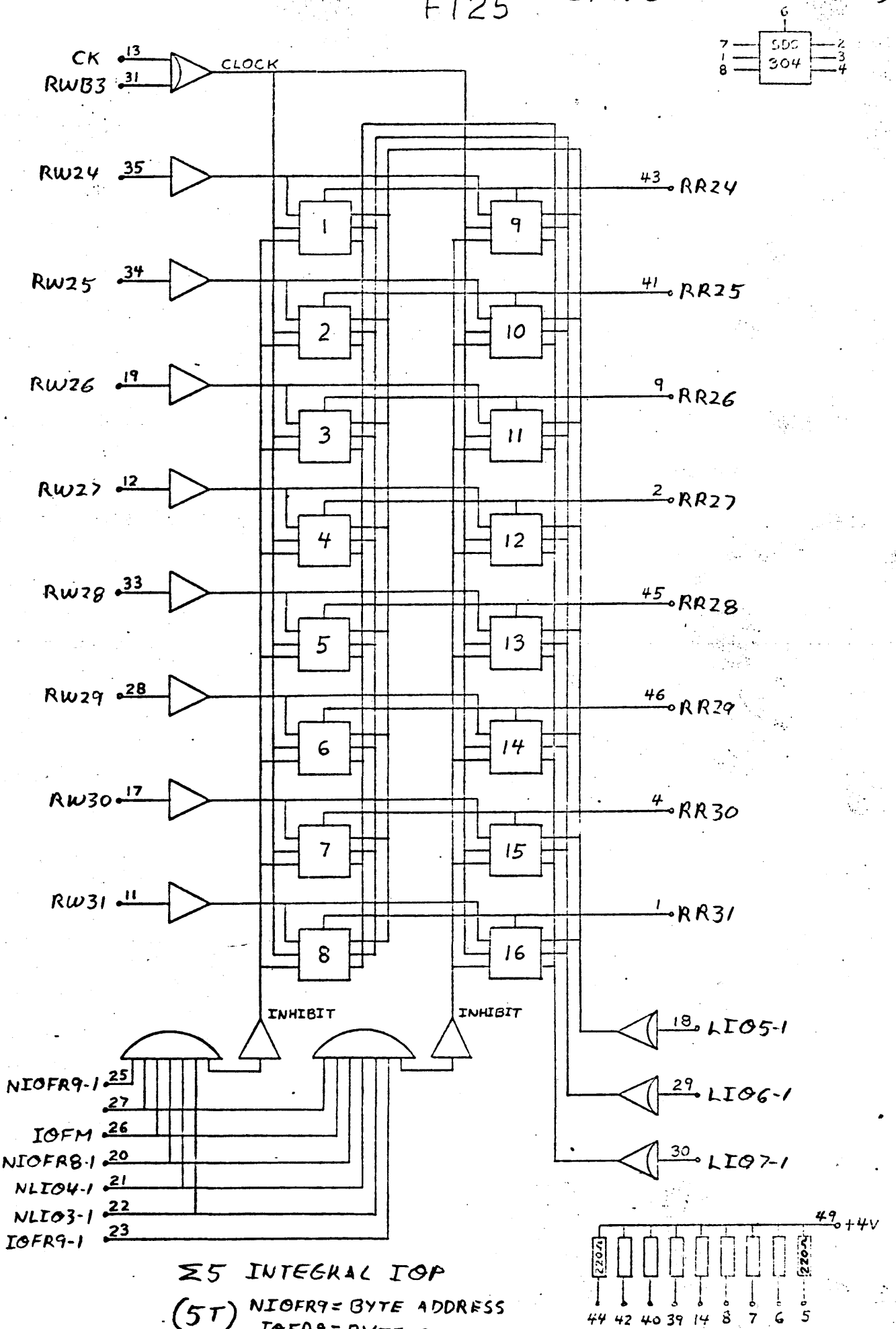




Σ5 INTEGRAL IOP

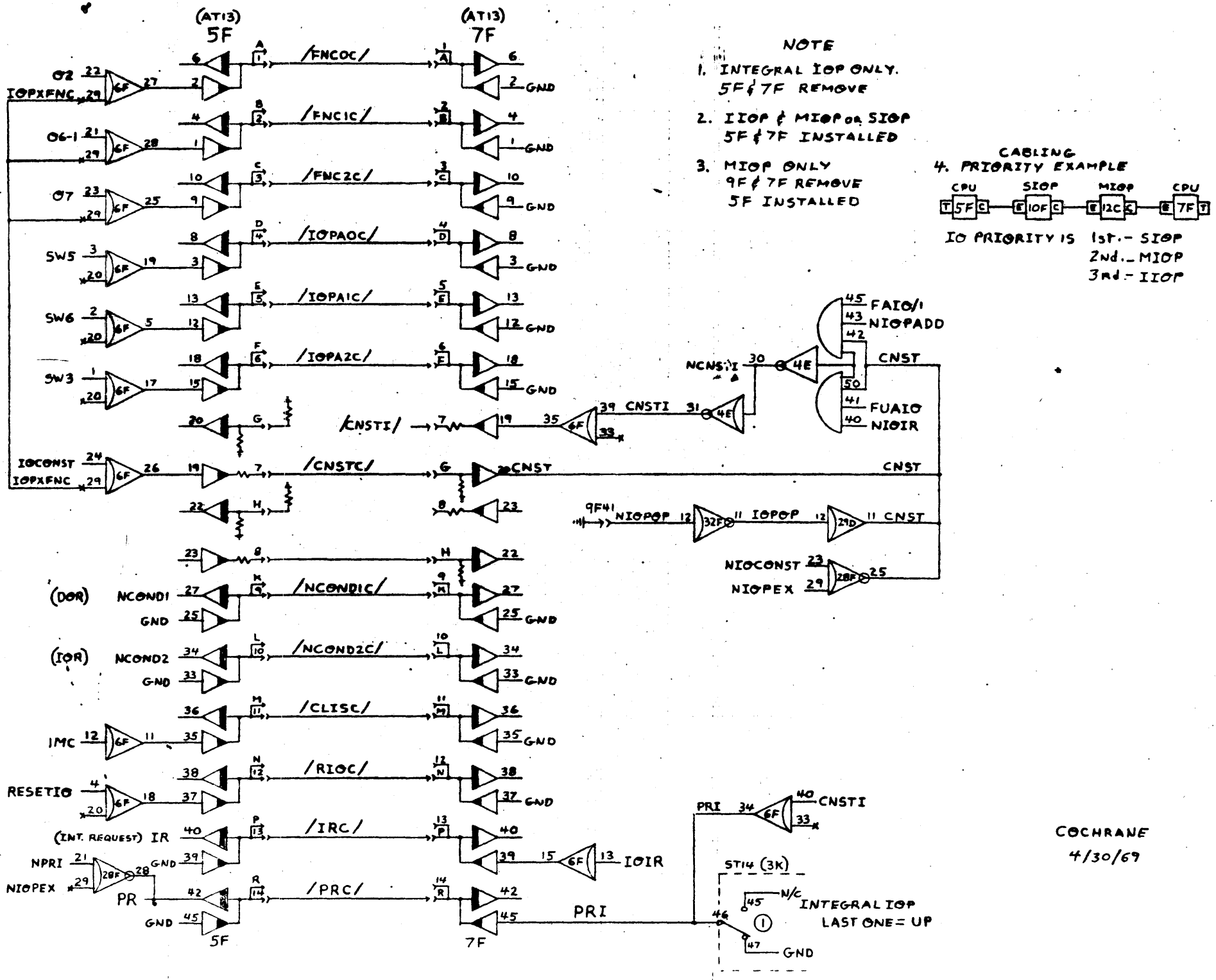
IOFR8·NIOFR9 = MS BYTE COMMAND DBW ADDR
IOFR8·IOFR9 = LS " " " "

FT25 INTEGRAL IOP (5T)



Σ5 INTEGRAL IOP

(5T) NIOFR9 = BYTE ADDRESS
IOFR9 = BYTE COUNT



NOTE

1. INTEGRAL IOP ONLY.
   5F & 7F REMOVE
2. IIOP & MIOP OR SIOP
   5F & 7F INSTALLED
3. MIOP ONLY
   9F & 7F REMOVE
   5F INSTALLED

CABLING

4. PRIORITY EXAMPLE

IO PRIORITY IS 1st.- SIOP
2nd.- MIOP
3rd.- IIOP

COCHRANE
4/30/69

FRI Σ7

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	BT 18	IT 16	BT 16	GT 11	GT 11	FT 22	FT 22	XT 10	FT 22	GT 11	GT 11	GT 11	FT 22	FT 22	FT 22	GT 11	LT 14	LT 14	IT 16	IT 16	IT 26	LT 20	IT 20	XT 10	LT 14	LT 20	IT 24	IT 20	IT 25	IT 25	BT 16	32 K	A
B	32 H	31 H	IT 16	IT 26	LT 14	LT 14	LT 14	XT 10	LT 14	BT 10	BT 11	LT 14	BT 10	IT 26	BT 11	AT 21	IT 25	ET 23	LT 21	IT 16	LT 13	IT F	IT F	XT 10	IT F	IT 25	BT 16	IT 11	XT 10	XT 10	32 U	32 L	B
C	32 G		IT 16	IT 26		LT 21	BT 18	BT 11	LT 14	XT 10	LT 14	IT 20		IT 20	BT 10		XT 10	IT 20		IT 26	IT 20		IT 26	XT 10		IT 26	LT 20		IT 20		LT 14	LT 14	C
D			IT 16	IT 20		IT 20	IT 20	IT 26	LT 20	XT 10	LT 21	IT D 16		LT D 20	AT D 11		BT 16	IT 20		XT 10	IT 20		XT 10	LT 14		IT 25	IT F 16		IT F 25		31 N	32 N	D
E	AT 21		IT 25	IT F 25	BT 11	BT 11	IT 16	XT 10	LT 20	LT 14	IT 26	FT 22	IT 16	BT 16	ET 23	XT 10	IT 16	LT 21	LT 13	LT 13	BT 17	BT 11	IT 25	XT 10	BT 11	IT 26	LT 13	FT 22	GT 11	FT 22	LT 13	31 U	E
F		IT 16	IT 26		IT 20	IT 20	LT 20	IT 25	LT 13		LT 13			LT 14	LT 14		LT 14	LT 14		BT 11	GT 10		FT 22	XT 10		FT 22	GT 11		IT 25	LT 20		32 Q	F
G	32 C		BT 11		BT 11	IT 16	BT 11	XT 10	IT 16		IT 20			IT 25	BT 11		IT 16	IT F 24		LT F 14	LT 21		LT 20	XT 10		IT 25	LT 20		IT 20	IT 16		LT 21	G
H	32 B	31 B	IT 25	LT 21	IT 16	LT 21	LT 21	LT 14	IT 25	BT 11	LT 20		IT 16	XT 10		IT 26	IT 20	LT 20	LT 20	IT F 20	IT 20	LT 20	IT 24	LT F 20	XT 10	IT 20	BT 11	BT 10	BT 16	30 S	31 S	32 S	H
J	BT 10	BT 16	BT 11	BT 11	BT 11	BT 11	BT 11	BT 11	BT 11	BT 10	BT 11	BT 11	BT 10	LT 14	XT 10	IT 16	IT 24	LT 20		IT 16	IT 20	IT 20	LT 20	IT 20	IT 20	XT 10	LT 20	IT 20	IT 20	BT 11	LT 21	32 T	J
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

F = FLOATING POINT 8418
D = DECIMAL ARITHMETIC 8419

FR2 Σ7

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
K	1A	30U	AT 11	IT 16	XT 10	IT 26	AT 21	IT 16	FT 22	FT 22	IT 16	IT 26	XT 10	FT 18	FT 18	FT 22	FT 22 F	FT 17 F	FT 17 F	FT 17 F	FT 17 F	LT 13	LT 18	LT 18 F	LT 18 F	IT 16 F	FT 17	FT 17 F	FT 22 F	XT 10	FT 17 F	FT 17 F	K
L	1B		IT 16	AT 11	BT 18	BT 16	XT 10	FT 18	GT 11	FT 18	FT 18	GT 11	FT 22	FT 17 F	FT 17 F	XT 10	FT 17	FT 17	GT 10	FT 17	FT 17	XT 10	FT 17 F	FT 17 F	BT 16	XT 10	LT 21	XT 10 AT11 RX	FT 25 R	FT 25 R	FT 25 R	FT 25 16-23	L
M	32R		LT 21	AT 21		BT 17			LT 17 F	LT 17 F		LT 17 F	LT 17 F	IT 16		BT 17	LT 17	LT 17		LT 17	LT 17		BT 17	LT 17 F	LT 17 F		LT 17 F	LT 17 F	XT 10	BT 18	BT 17	BT 17	M
N	1D	2D		AT 11		AT 11	BT 16		BT 17 D	XT 10		IT 26	XT 10	IT 16		AT 21	IT 16	LT 21		LT 18 F	XT 10		LT 18	LT 18	FT 22		GT 11	GT 10	FT 17	FT 17	FT 17	FT 17	N
P	ZT 23		AT 11	BT 16	AT 21	IT 16	XT 10	BT 16	LT 21	LT 20	BT 16	LT 13	LT 21	AT 11	XT 10	DT 16	FT 17	GT 11	FT 17	GT 11	GT 10	FT 17	GT 10	FT 17	FT 22	XT 10	LT 17	LT 17	LT 17	LT 17	IT 16	XT 10	P
Q	1F		AT 11	IT 16		AT 11	IT 17	LT 17	IT 17		LT 13	BT 17	XT 10	BT 17		BT 17	IT 16	FT 18		BT 16	IT 16		XT 10	FT 22	FT 22		BT 16	AT 11 RX	FT 25 R	FT 25 R	FT 25 R	FT 25 24-31	Q
R	32M		XT 10	AT 21		LT 17 F	LT 17 F	LT 17 F	LT 17 F		FT 17	FT 17	GT 11	LT 17		LT 17	LT 17	LT 17		XT 10	IT 16		BT 16	LT 17	LT 17		LT 17	LT 17	FT 17	FT 17	GT 11	FT 22	R
S	1H	2H	3H	IT 16	BT 18	XT 10	AT 21	FT 17	FT 17	AT 11	BT 16	AT 11	FT 17	FT 17	GT 11	FT 22	FT 22	FT 18	FT 18	BT 16	XT 10	BT 16	IT 16	IT 16	BT 16	FT 22	FT 17	FT 17	GT 11	FT 17	FT 17	XT 10	S
T	1J	BT 18	FT 22 F	IT 16 F	XT 10	FT 17 F	FT 17 F	FT 17 F	FT 17 F	FT 17 F	FT 17 F	IT 26	LT 18 F	AT 11 RX	FT 25 R	FT 25 R	FT 25 R	FT 25 8-15	IT 26	BT 18	IT 16	IT 26	LT 18	LT 18	XT 10	BT 17	IT 25	AT 11 RX	FT 25 R	FT 25 R	FT 25 R	FT 25 0-7	T
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

F = FLOATING POINT 8418 D = DECIMAL UNIT 8419

F GISTER EXTENSION 8416

R GISTER EXTENSION INTERFACE

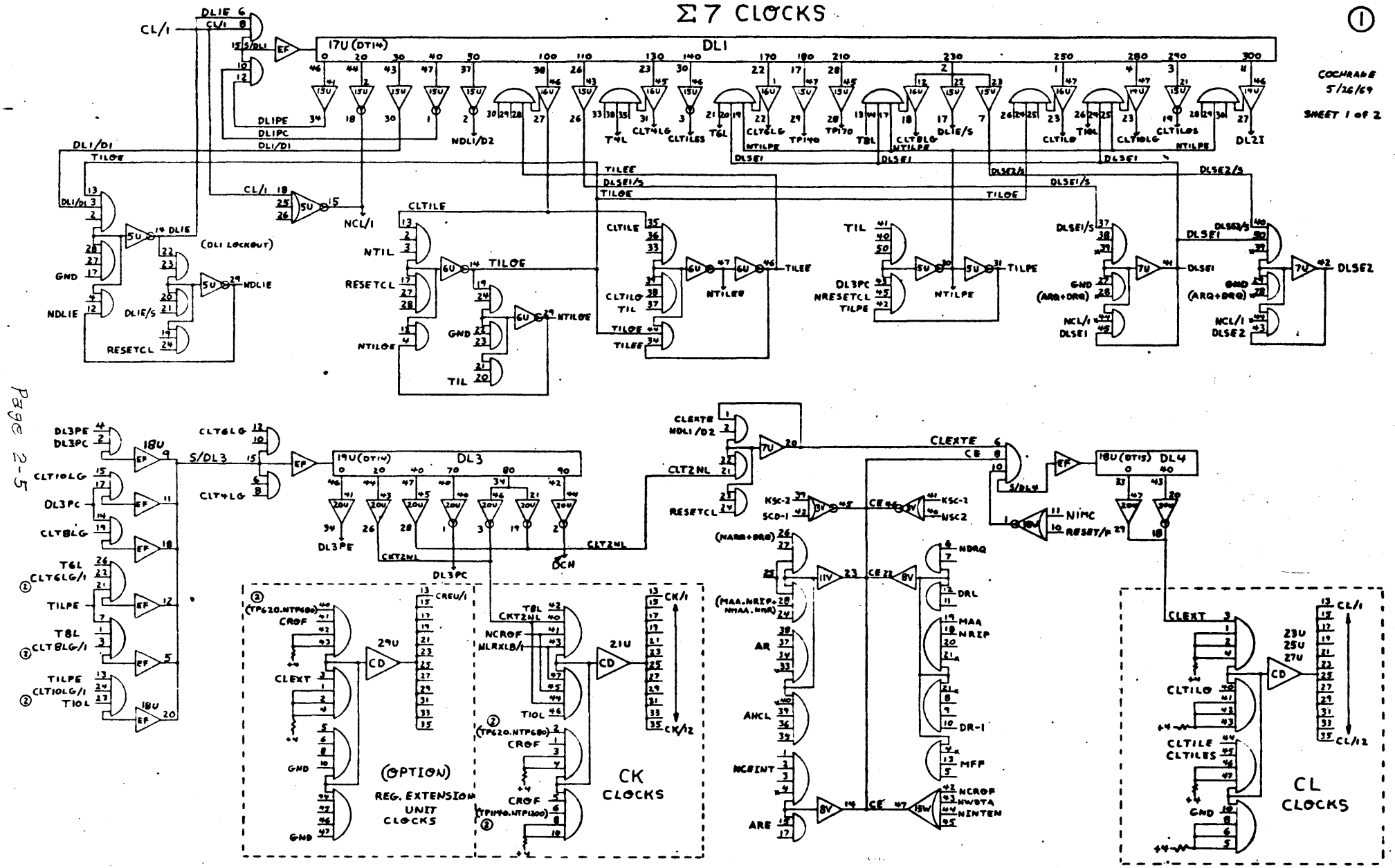
R3 Σ7

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
U	RC 2 B	RC 1 E	RC 31 K	AT 23 RX	ZT 23 RX	AT 23	ZT 23	AT 23	ZT 23	AT 23	ZT 23	AT 23	HT 15	DT 14	DT 15	DT 14	HT 16	HT 15	HT 16	HT 15	DT 14	HT 16	LT 29	XT 10	FT 22	BT 17	LT 14	LT 14	DT 16	XT 10			U
V	AT 10 Q 27		AT 11 J 26 FR3	LT 13	BT 16	AT 13	BT 16	FT 26	AT 12 K 30	IT 16	IT 16	IT 24	IT 24	BT 11	FT 22	BT 17	XT 10	BT 11	AT 11	DT 14	HT 15	LT 21	IT 25	BT 11	LT 21	LT 13	LT 13	IT 16	LT 21	IT 25	LT 21	XT 10	V
W	AT 11 P 30	BT 17	ST 29		AT 13	BT 17	AT 12	XT 10	ST 14	LT 16 SPARE INT.	LT 16 IO PCP	LT 16 RTC 3&4 = 2	LT 16 RTC 1&2 = 2/C	BT 16	IT 25	LT 16 MEM. PAR.	LT 16 RTC 3&4	LT 16 RTC 1&2/C	LT 16 PFS /P	LT 13	FT 28	FT 28	IT 25	IT 25	BT 11	IT 25	XT 10	CT 16	IT 25			1W	W
Y	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 M	FT 25 XT19 M	BT 10	AT 12	BT 16	XT 10	FT 25 M	FT 25 M	FT 25 M	FT 25 XT19 M	FT 25 MP	FT 25 MP	FT 25 MP	FT 25 MP	IT 24 MP	IT 24 MP	IT 16	1Y	Y
J	AT 11	(PRIORITY INTERRUPT CHASSIS 8421)	LT 26		AT 13		AT 11		BT 17	BT 16	IT 25	BT 17		AT 11		LT 16 14-15	LT 16 12-13	LT 16 10-11	LT 16 8-9		AT 11		LT 16 6-7	LT 16 4-5	LT 16 2-3	LT 16 0-1	IT 25	BT 18	XT 10			ST 14	J
A	AT 11	FT 27	LT 13	IT 25	LT 12	IT 16	FT 27	FT 26	FT 26	FT 26	FT 26	FT 26	XT 10 (MULTIPLEXING IOP 8471)		AT 11	IT 16	AT 11	BT 11	AT 11	BT 11	AT 12	IT 25	AT 11	IT 25	LT 13	XT 10	FT 24	FT 24	IT 25		FT 24	FT 24	A
B	XT 16	FT 23	FT 23	FT 23	BT 11	FT 23	FT 23	XT 10	FT 24	FT 24	FT 27	FT 27	IT 16	IT 25	BT 11	IT 16	IT 25	BT 11	AT 10		FT 24	FT 24	BT 11	AT 24	FT 27	FT 27	LT 21	BT 11	XT 10	LT 21	BT 11		B
C	32C	31C	FT 24	FT 24	FT 24	FT 24	FT 24	FT 24	FT 24	FT 24		BT 11	LT 13	IT 25	IT 25	IT 25	IT 25	XT 10	AT 12	LT 26	AT 13	IT 25	FT 24	9C	XT 10		FT 24	FT 24	LT 21	LT 13	IT 16	IT 25	C
D	32D	31D	FT 25 18-20 I	FT 25 8-F I	FT 25 10-17 I	FT 25 0-7 BA	FT 25 18-20 I	FT 25 8-F I	FT 25 10-17 I	FT 25 0-7 BA	FT 25 18-20 I	FT 25 8-F I	FT 25 10-17 I	FT 25 0-7 BC	FT 25 18-20 I	FT 25 8-F I	FT 25 10-17 I	FT 25 0-7 BC	FT 25 18-20 I	FT 25 8-F I	FT 25 10-17 I	FT 25 0-7 OF	XT 10	9D	HT 15	DT 11	HT 15	DT 11				AT 11	D
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

M = MAP 8415 XT19 CL. TERM. AND MAP
MP = MEM. PROTECT 8414
I = IO CHANNEL EXTENSION 8472
C = COUNTER INTERRUPT
P = PWR FAIL SAFE 8413
RX = REGISTER EXTENTION INTERFACE UNIT
RC = RIBBON CABLE

PAGE 2-3A

Σ7 CLOCKS

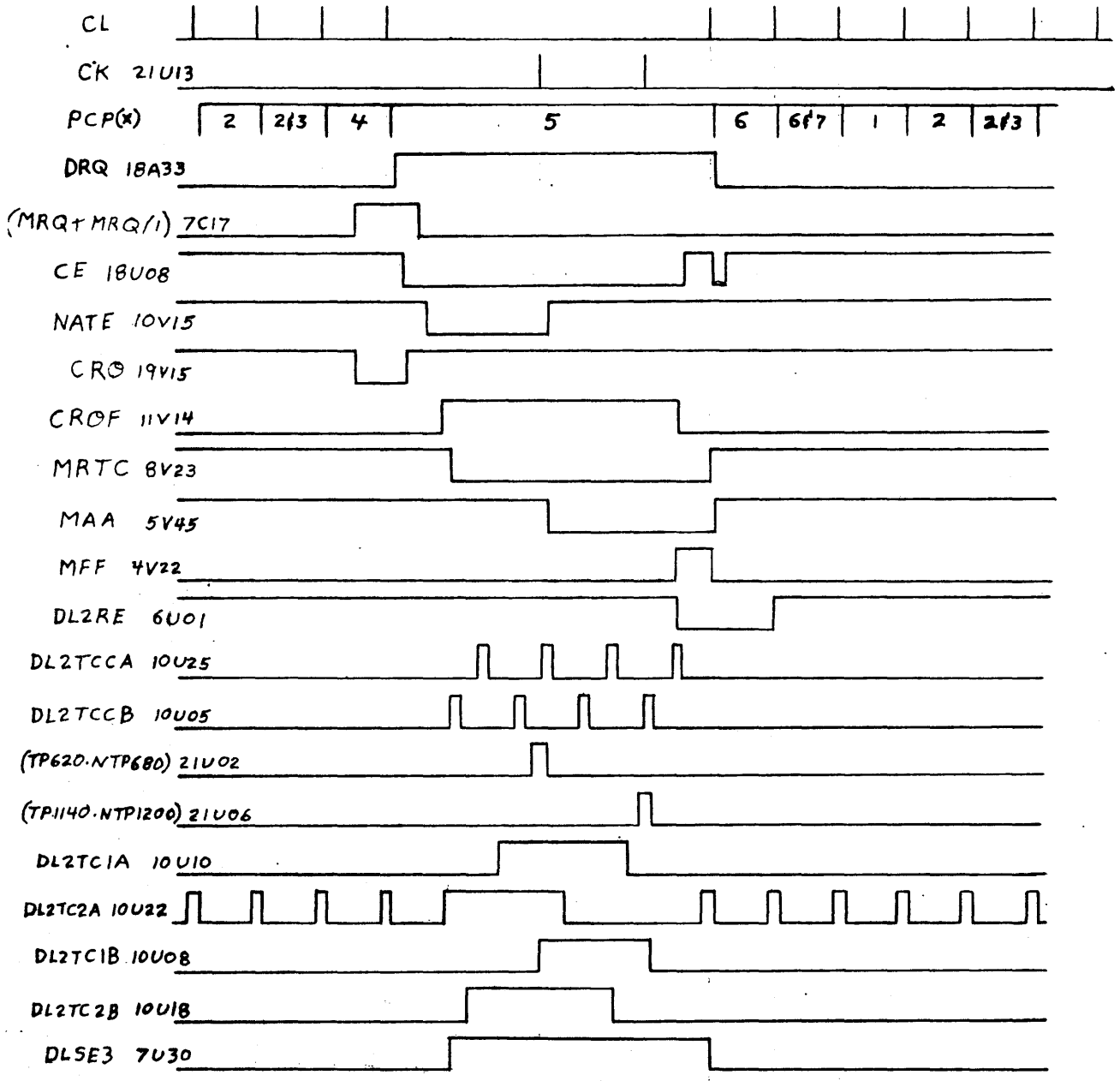


COCHRANE
5/26/69

SHEET 1 of 2

Page 2-5

Σ7 CK GENERATION FOR FAST MEMORY



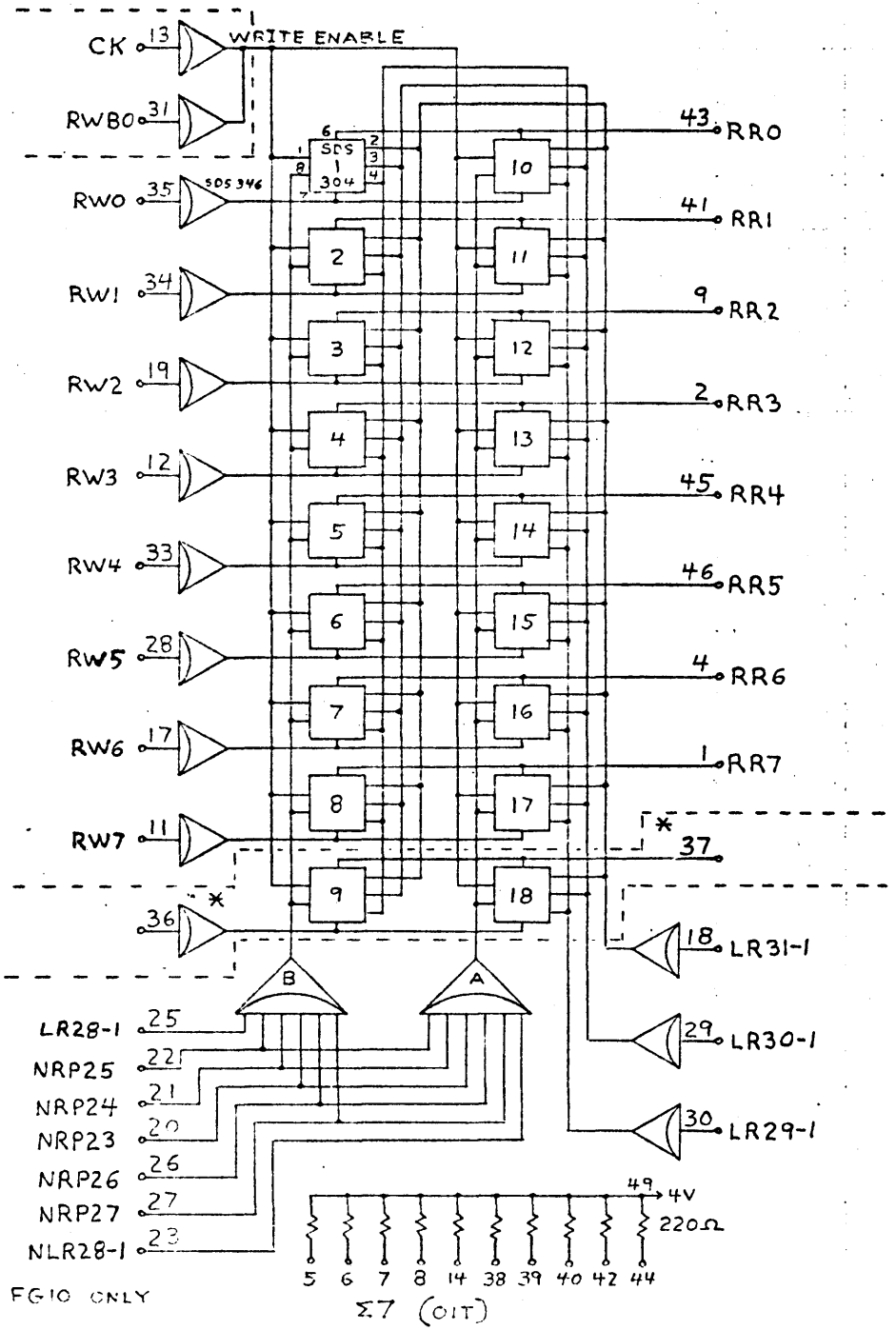
T6L-HIGH
MBB, MCC, MDD, MEE - LOW
MRQ/1 - LOW

S/HALT 20A50 GND
Q = 25
SEL. ADD. SW'S = ZERO

STORE SEL. ADD. SW. DOWN

Σ7 REGISTER (01T)

FG10/FT25

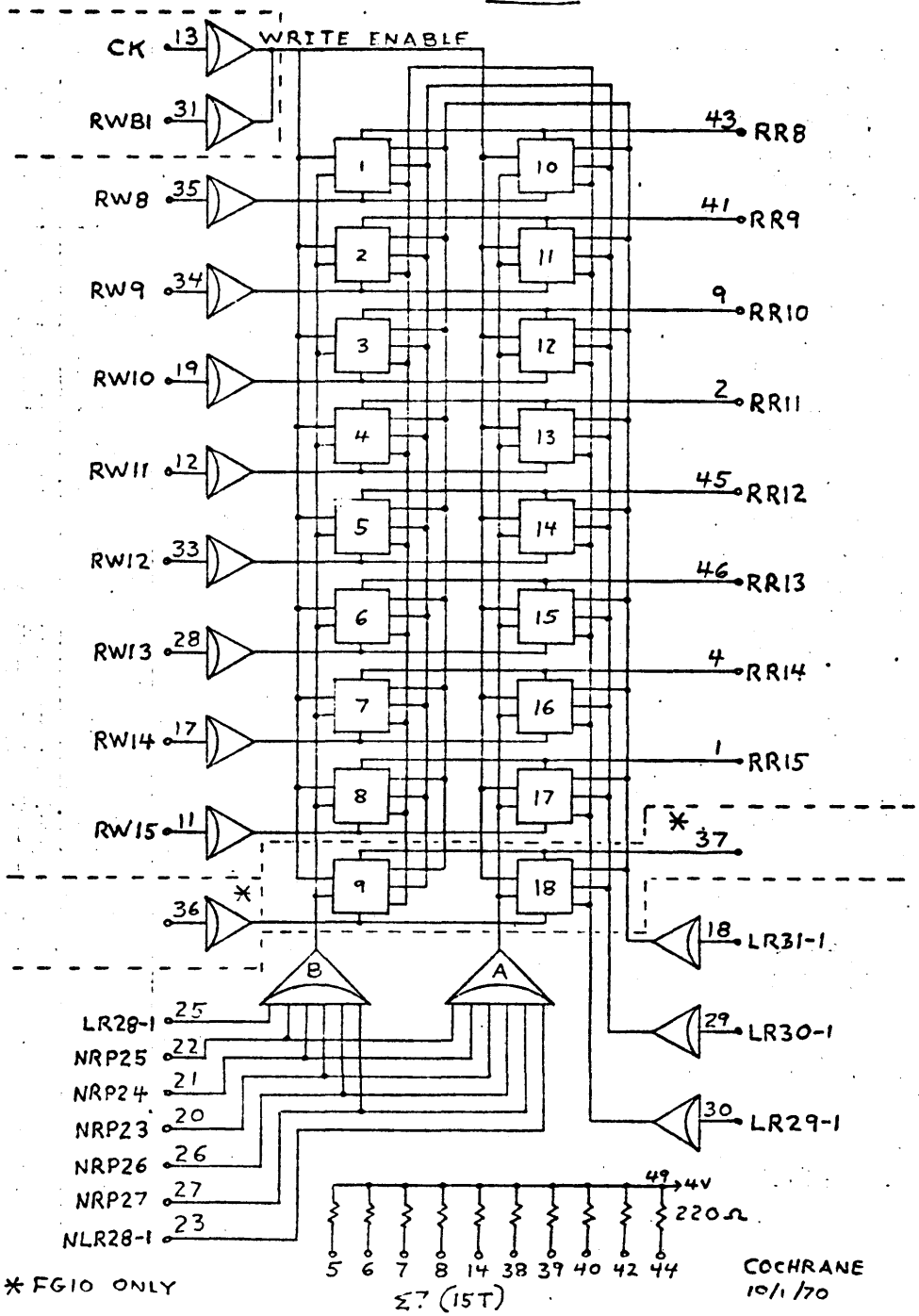


* FG10 ONLY

Σ7 (01T)

Σ7 REGISTER (15T)

FG10/FT25

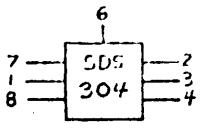


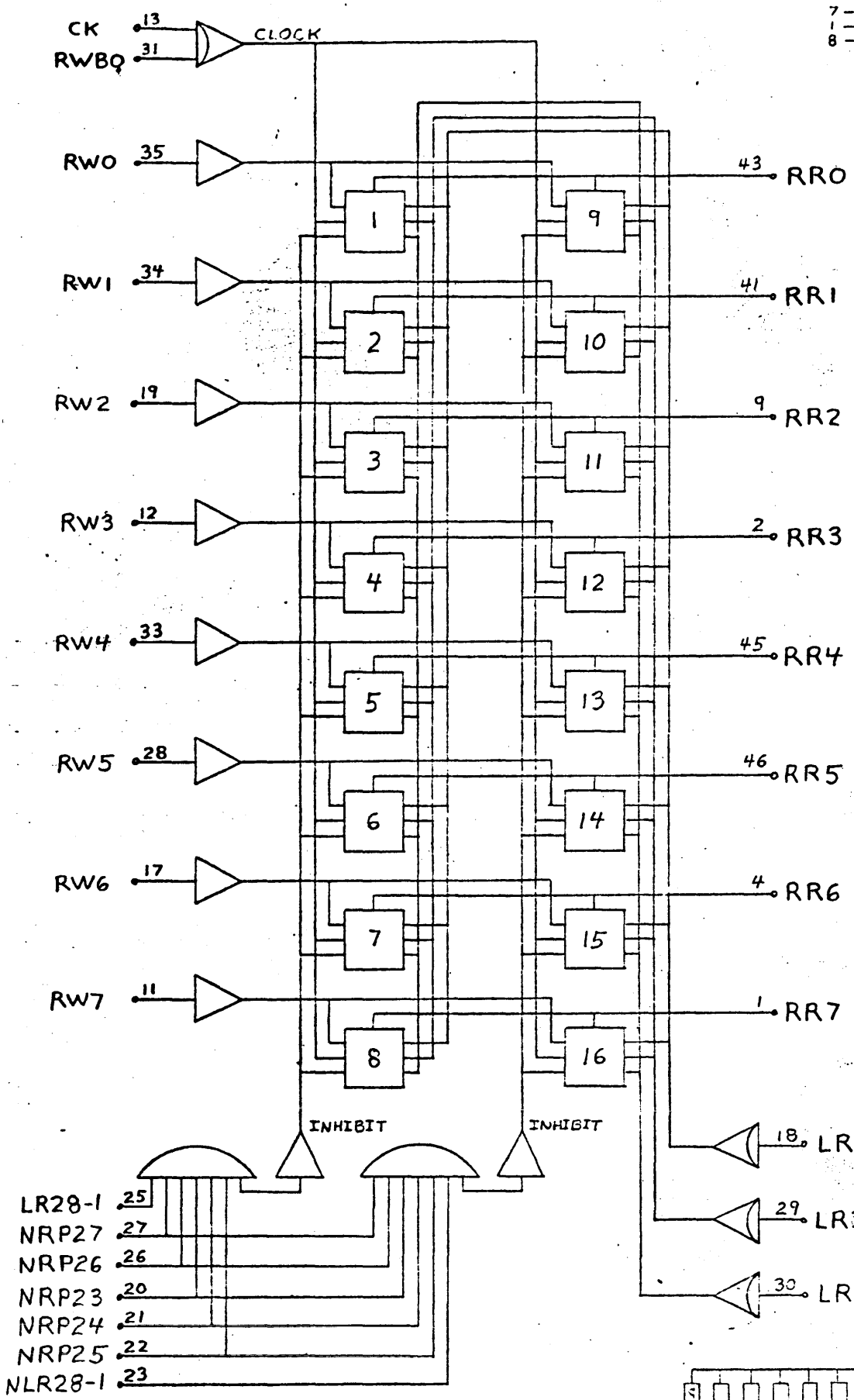
* FG10 ONLY

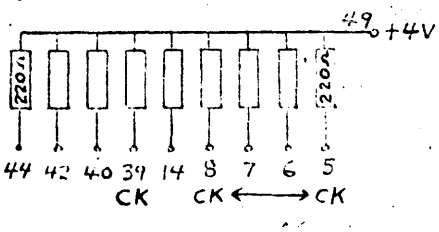
Σ7 (15T)

COCHRANE
10/1/70

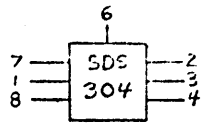
FT25







Σ7
REGISTER (OIT RR0-RR7)



CK 13
RWB1 31
CLOCK

RW8 35
RW9 34
RW10 19
RW11 12
RW12 33
RW13 28
RW14 17
RW15 11

1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16

43 RR8
41 RR9
9 RR10
2 RR11
45 RR12
46 RR13
4 RR14
1 RR15

INHIBIT
INHIBIT

18 LR31-1
29 LR30-1
30 LR29-1

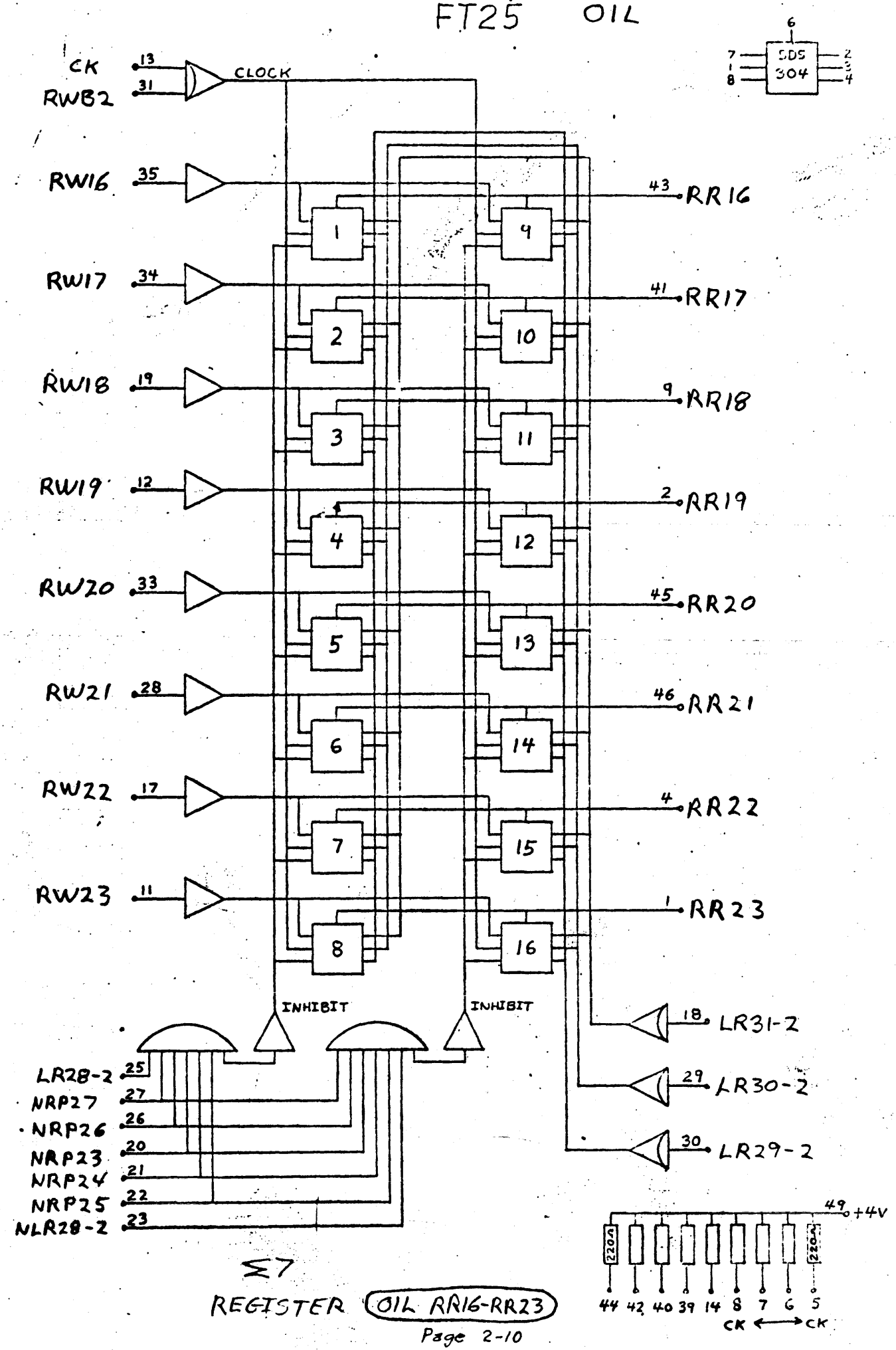
LR28-1 25
NRP27 27
NRP26 26
NRP23 20
NRP24 21
NRP25 22
NLR28-1 23

49 +4V
220Ω 220Ω
44 42 40 39 14 8 7 6 5
CK ⟷ CK

Σ7

REGISTER (15T RR0-RR15)

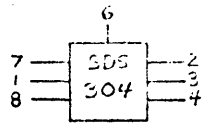
FT25 OIL



Σ7

REGISTER (OIL RR16-RR23)

FT25 01Q



CK 13
RWB3 31
CLOCK

RW24 35
RW25 34
RW26 19
RW27 12
RW28 33
RW29 28
RW30 17
RW31 11

1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16

43 RR24
41 RR25
9 RR26
2 RR27
45 RR28
46 RR29
4 RR30
1 RR31

INHIBIT
INHIBIT

18 LR31-1
29 LR30-1
30 LR27-1

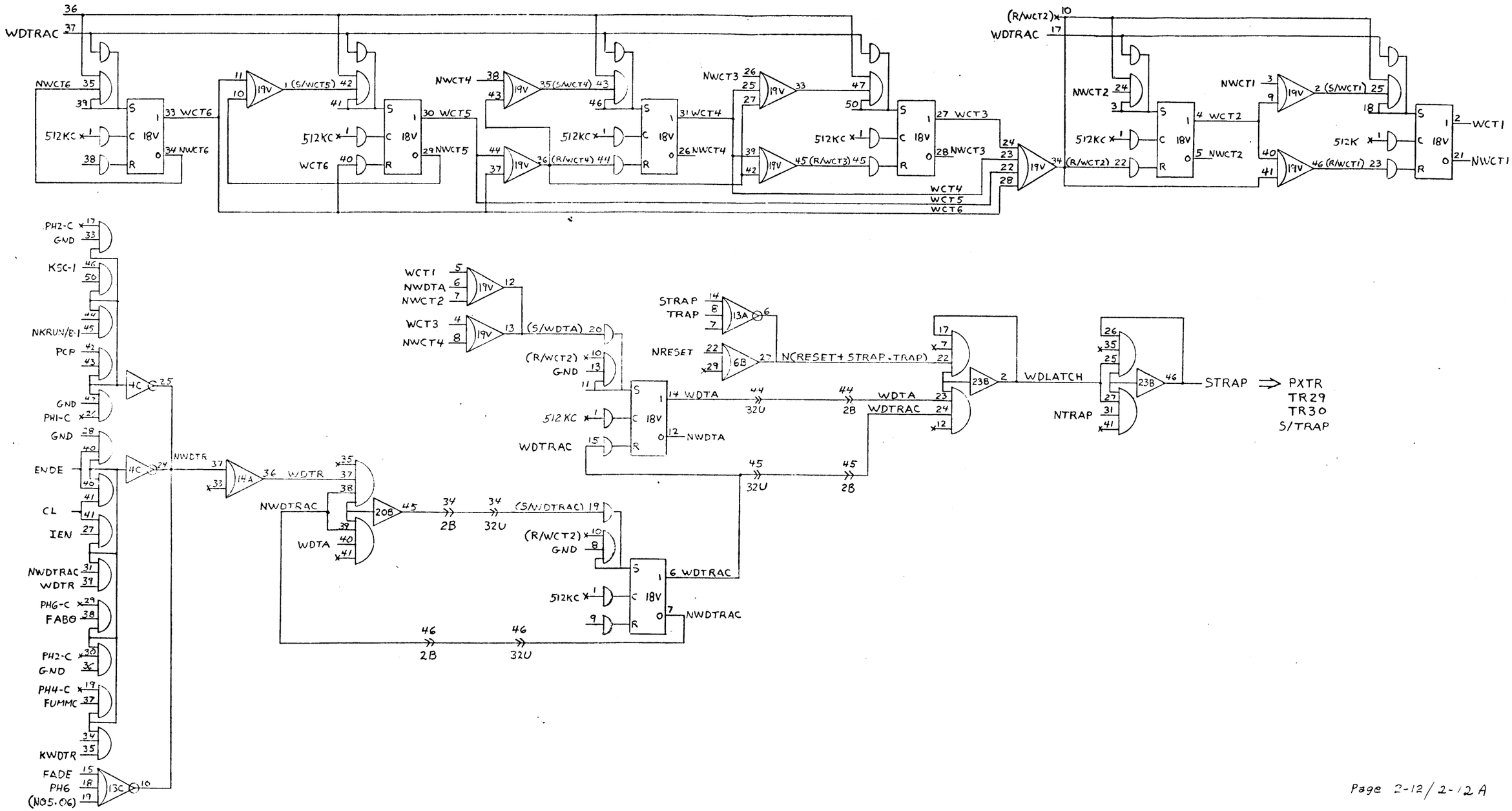
LR28-1 25
NRP27 27
NRP26 26
NRP23 20
NRP24 21
NRP25 22
NLR28-1 23

49 +4V
220Ω
220Ω
44 42 40 39 14 8 7 6 5
CK ⟷ CK

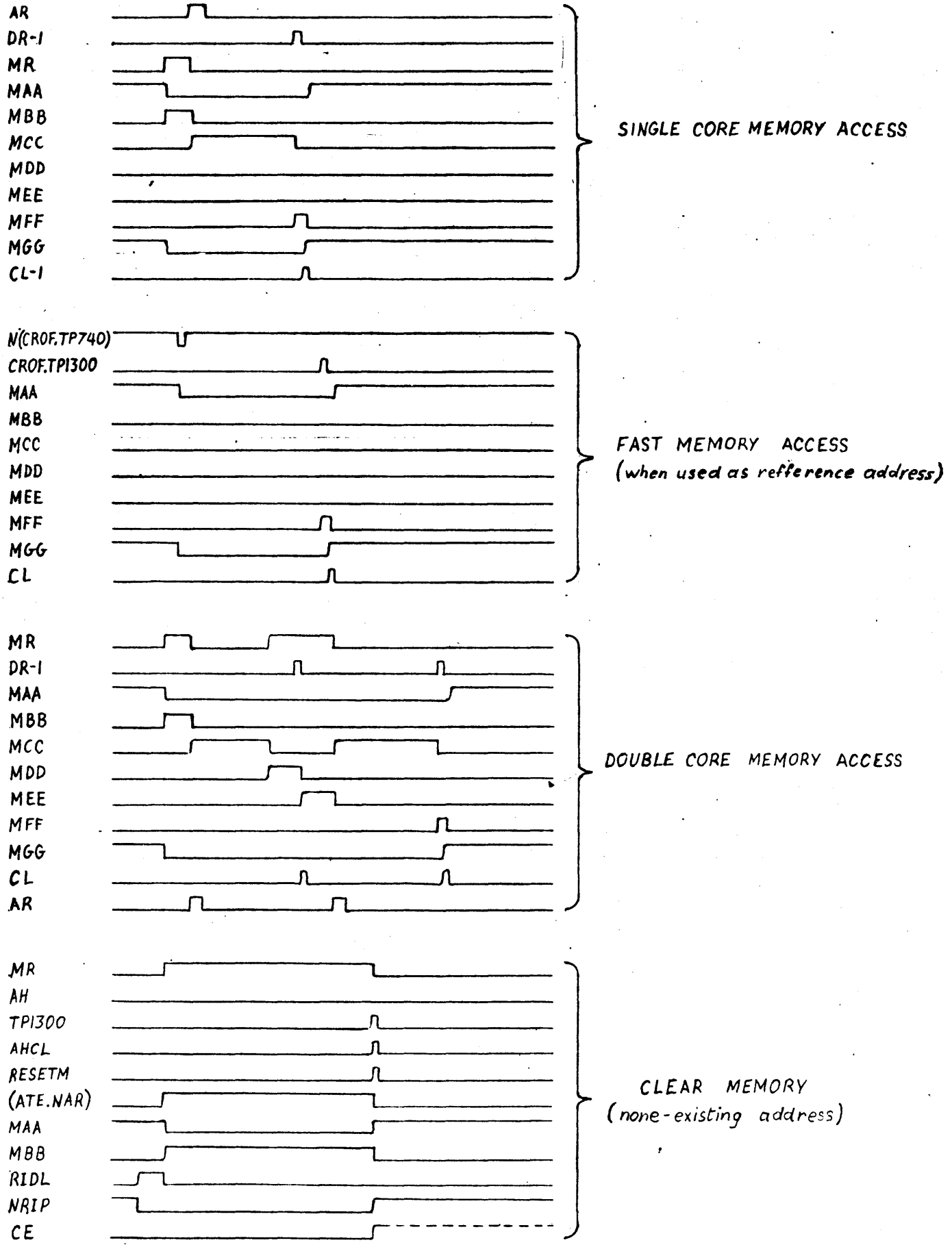
Σ7
REGISTET (01Q RR24-RR31)

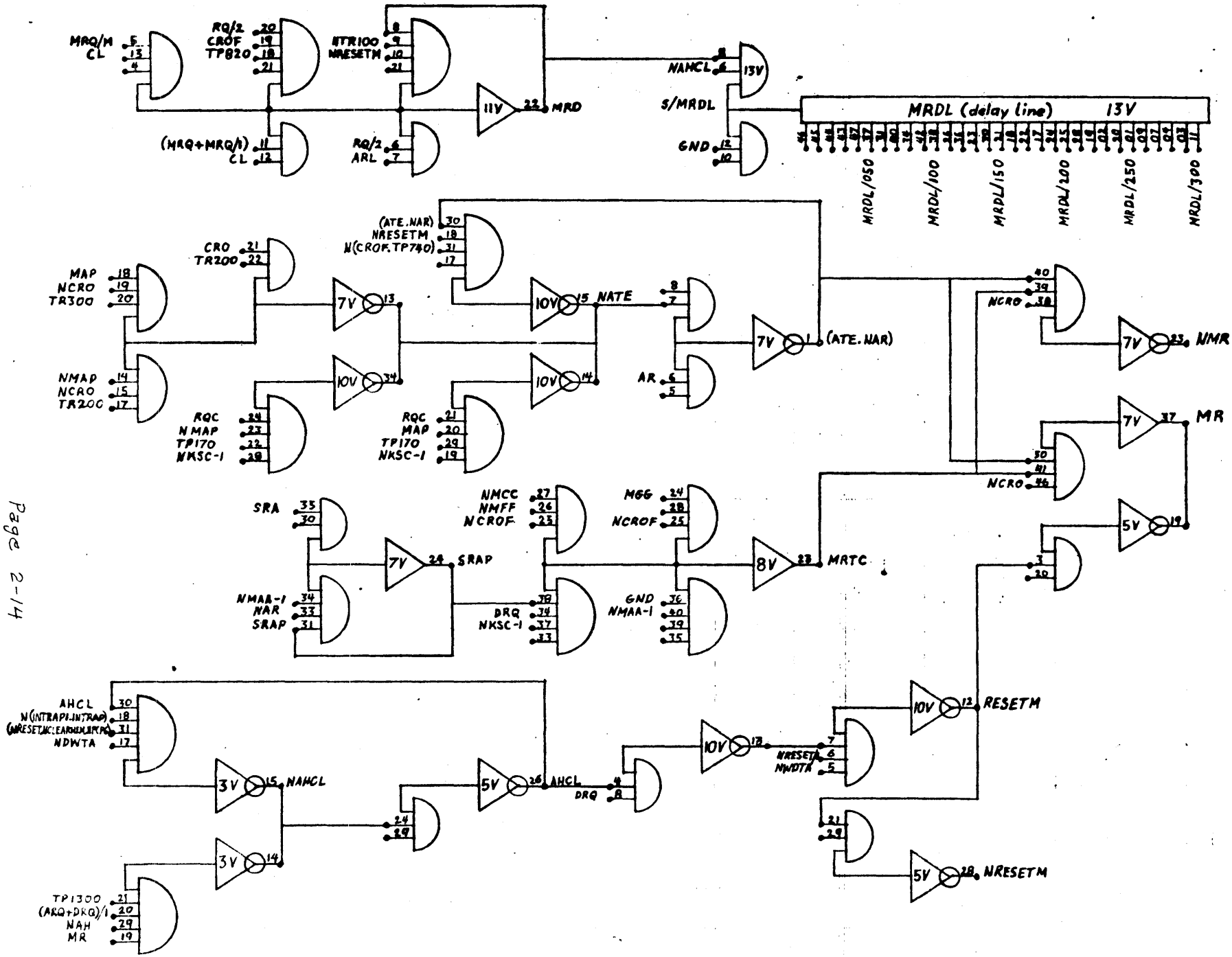
Σ7 WATCHDOG TIMER TRAP (46)

1/26/68
COCHRANE

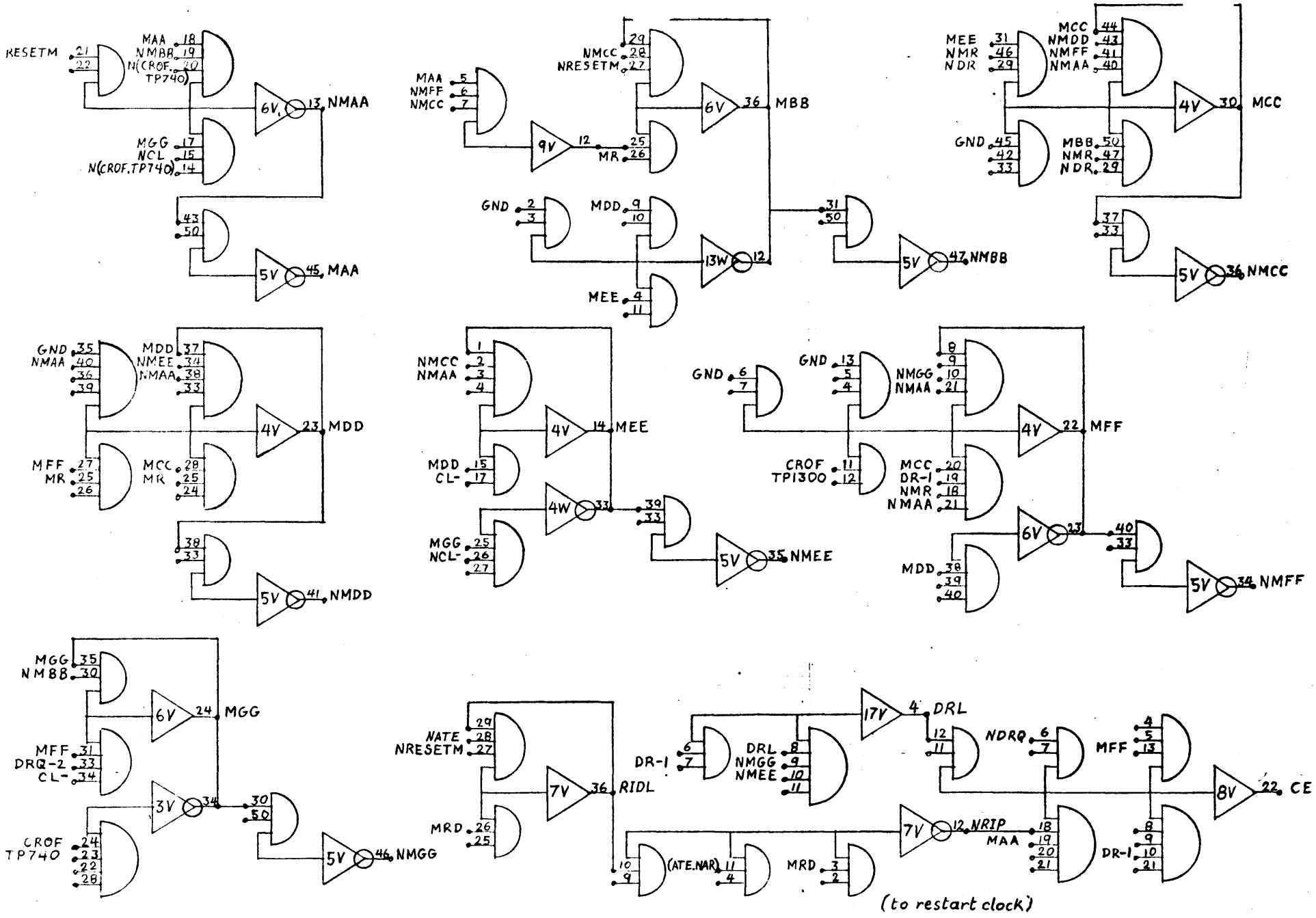


§7 MEMORY CYCLE CONTROL





§7 MEMORY REQUEST



MEMORY CYCLE CONTROL

FAMILY TERMS

SIGNAL NAME	TEST POINT
FABC	31J47
FABO	24J45
FABO/1	24J02
FABO/2	24J46
FABOA	24J35
FABOA/1	30H02
FABOA/2	22J01
FABOX	23J47
FABR	30Q15
NFA BRANCH	25H01
FABS	28H44
FABSA	28H25
FACAL	22J02
FACV	22J13
FADE	32J04
FADIO	30H13
FADIV	20J45
FADIVH	6H36
FADIVW	3J33
FADW	32J45
FAFL	25J13
FAFLM	25J46
FAFLMD	25J02
FAFLAS	25J35
FAFRR	27Q17
FAFRR/1	24H35
FAILL	28H15
FAIM	27J01
FAIO	25H31
FAIO/1	22J35
FAMDSF	16Q27
FAMDSE/D	20J03
FAMDSF/M	24H36
FAMUL	19J46
FAMULH	25J46
FAMULI	26J01
FAMULNH	26J35
FAMULW	
FANIMP	26H23
FAPRIV	27J13
FAPSD	26J02
FARWD	28H05
FASH	23H13
FASHFL	23H46
FASHFX	23H02
FATR	28H47
FATRA	28H27
FATR5	24J13
FAS1	30J35
FAS2	32J03
FAS3	31J28
FAS4	
FAS5	
FAS6	32J46
FAS7	23J02
FAS8	23J01
FAS9	27H30
FAS10	32J01
FAS11	27H14
FAS12	27H22
FAS13	27J35
FAS14	23J03
FAS15	23J44
FAS16	23J45
FAS17	23J04
FAS18	25H46
FAS19	30J46
FAS21	20J04
FAS22	29H14
FAS23	29H30
FAS24	29H22
FAS25	
FAS26	21J13
FAST/1	26H30
FAST	27J02
FASTA	24J01
FATR	28H47
FAW	29H23
FUANLZ	31J41
FUBAL	31J46
FUCS	31J36
FUCVS	21J36
FUEBS	20H11
FUEBSA	28H28
FUEBS8	31J18
FUEBS9	31J19
FUEBS14	31J05
FUEXU	31J45
FULAD	31J25
FULCD	31J27
FULD	31J01
FULS	31J35
FULRP	27J46
FUMMC	31J44
FUMTH	21J02
FUSID	31J26
FUSTH	21J46
FUSTS	31J34
FUWAIT	21J35
FAFLD	25J45
FUAD	28G46
FUAND	
FUAWM	28G45

Register	FF	NFF	S/FF	R/FF	C/FF	FF/L
PCP1	20A31	26	46	44	1	17B
2	20A30	29	41	40	1	
3	20A33	34	39	38	1	
4	20A02	21	18	23	1	
5	20A04	5	3	22	1	
6	20A14	12	11	15	1	
7	20A06	7	$	9	1	
PRE1	07F27	28	50	.	1	17B
2	07F31	26	46	.	1	
3	07F30	29	41	.	1	
4	07F33	34	39	.	1	
PH1	27A27	28	50	.	1	17B
2	27A31	26	46	.	1	17B
3	27A30	29	41	.	1	
4	27A33	34	39	.	1	17B
5	27A02	21	18	.	1	
6	27A04	5	3	.	1	
7	27A14	12	11	.	1	
8	27A06	7	$	.	1	17B
9	26A27	28	50	.	1	
10	26A31	26	46	.	1	
11	26A30	29	41	.	1	
12	26A06	7	$	.	1	
13	26A02	21	18	.	1	
14	26A04	5	3	.	1	
15	26A14	12	11	.	1	
PHA	26A33	34	39	38	1	

A- REGISTER

REGISTER	FF	NFF	S/FF	R/FF	C/FF
A0	05S23	25	12	2	1
1	05S19	21	28		1
2	05S31	29	37		1
3	05S27	22	35		1
4	06S23	25	12		1
5	06S19	21	28		1
6	06S31	29	37		1
7	06S27	22	35		1
8	19S23	25	12		1
9	19S19	21	28		1
10	19S31	29	37		1
11	19S27	22	35		1
12	20S23	25	12		1
13	20S19	21	28		1
14	20S31	29	37		1
15	12L23	22	35		1
16	12L23	25	12		1
17	12L31	21	28		1
18	12L31	29	37		1
19	12L27	22	35		1
20	13L23	25	12		1
21	13L19	21	28		1
A22	13L31	22	37		1
23	13L27	22	35		1
24	3N23	25	12		1
25	3N19	21	28	2	1
26	3N31	29	37		
27	3N27	22	35		
28	4N23	25	12		
29	4N19	21	28		
30	4N31	29	37		
31	4N27	22	35		
47	8N4	5	3		
48	22T23	25	12		
49	22T19	21	28		
50	22T31	29	37		
51	22T27	22	35		
52	23T23	25	12		
53	23T19	21	28		
54	23T31	29	37		
55	23T27	22	35		
56	12K23	25	12		
57	12K19	21	28		
58	12K31	29	37		
59	12K27	22	35		
A60	13K23	25	12		
61	13K19	21	28		
62	13K31	29	37		
63	13K27	22	35		
64	9L23	25	12		
65	9L19	21	28		
66	9L31	29	37		
67	9L27	22	35		
68	10L23	25	12		
69	10L19	21	28		
70	10L31	29	37		
71	10L27	22	35		

Signal	Test Point
PR0	5R17
PR1	5R31
PR2	6R17
PR3	6R31
PR4	8R17
PR5	8R31
PR6	9R17
PR7	9R31
PR8	15R17
PR9	15R31
PR10	16R17
PR11	16R31
PR12	17R17
PR13	17R31
PR14	19R17
PR15	19R31
PR16	12M17
PR17	12M31
PR18	13M17
PR19	13M31
PR20	15M17
PR21	15M31
PR22	16M17
PR23	16M31
PR24	3P17
PR25	3P31
PR26	4P17
PR27	4P31
PR28	5P17

Signal	Test Point
PR29	5P31
PR30	6P17
PR31	6P31
PR32	19Q31
PR47	25Q31
PR48	24R17
PR49	24R31
PR50	25R17
PR51	25R31
PR52	26R17
PR53	26R31
PR54	27R17
PR55	27R31
PR56	20M17
PR57	20M31
PR58	21M17
PR59	21M31
PR60	23M17
PR61	23M31
PR62	24M17
PR63	24M31
PR64	5M17
PR65	5M31
PR66	6M17
PR67	6M31
PR68	8M17
PR69	8M31
PR70	9M17
PR71	9M31

Signal	Test Point
G0	5R19
G1	5R29
G2	6R19
G3	6R29
G4	8R19
G5	8R29
G6	9R19
G7	9R29
G8	15R19
G9	15R29
G10	16R19
G11	16R29
G12	17R19
G13	17R29
G14	19R19
G15	19R29
G16	12M19
G17	12M29
G18	13M19
G19	13M29
G20	15M19
G21	15M29

Signal	Test Point
G22	16M19
G23	16M29
G24	3P19
G25	3P29
G26	4P19
G27	4P29
G28	5P19
G29	5P29
G30	6P19
G31	6P29
G47	25Q29
G48	24R19
G49	24R29
G50	25R19
G51	25R29
G52	26R19
G53	26R29
G54	27R19
G55	27R29
G56	20M19
G57	20M29
G58	21M19

Signal	Test Point
G59	21M29
G60	23M19
G61	23M29
G62	24M19
G63	24M29
G64	5M19
G65	5M29
G66	6M19
G67	6M29
G68	8M19
G69	8M29
G70	9M19
G71	9M29

ADDER (K)

Signal	Test Point	Signal	Test Point	Signal	Test Point
K0	9T26	K21	10K18	K57	9K27
K1	19T27	K22	10K20	K58	9K25
K2	9T25	K23	9N18	K59	13N19
K3	9N26	K24	10N26	K60	9K19
K4	9T19	K25	10N27	K61	9K18
K5	9T18	K26	10N25	K62	9K20
K6	9T20	K27	9N20	K63	13N18
K7	9N27	K28	10N19	K64	8K26
K8	10T26	K29	10N18	K65	8K27
K9	10T27	K30	10N20	K66	8K25
K10	10T25	K31	9N24	K67	13N20
K11	9N25	K47	13N26	K68	8K19
K12	10T19	K48	20T26	K69	8K18
K13	10T18	K49	20T27	K70	8K20
K14	10T20	K50	20T25		
K15	9N17	K51	13N27		
K16	10K26	K52	20T19		
K17	10K27	K53	20T18		
K18	10K25	K54	20T20		
K19	9N19	K55	13N25		
K20	10K19	K56	9K26		

B-REGISTER

REGISTER	FF	NFF	S/FF	R/FF	C/FF
B0	2S23	25	12	2	1
B1	2S19	21	28		
B2	2S31	29	37		
B3	2S27	22	35		
B4	3S23	25	12		
B5	3S19	21	28		
B6	3S31	29	37		
B7	3S27	22	35		
B8	24S23	25	12		
B9	24S19	21	28		
B10	24S31	29	37		
B11	24S27	22	35		
B12	25S23	25	12		
B13	25S19	21	28		
B14	25S31	29	37		
B15	25S27	22	35		
B16	15L23	25	12		
B17	15L19	21	28		
B18	15L31	29	37		
B19	15L27	22	35		
B20	16L23	25	12		
B21	16L19	21	28		
B22	16L31	29	37		
B23	16L37	22	35		
B24	1N23	25	12		
B25	1N19	21	28		
B26	1N31	29	37		
B27	1N27	22	35		
B28	2N23	25	12		
B29	2N19	21	28		
B30	2N31	29	37		
B31	2N27	22	35		
B47	8N14	12	11	15	
B48	24T23	25	12	2	
B49	24T19	21	28		
B50	24T31	29	37		
B51	24T27	22	35		
B52	25T23	25	12		
B53	25T19	21	28		
B54	25T31	29	37		
B55	25T27	22	35		
B56	14K23	25	12		
B57	14K19	21	28		
B58	14K31	29	37	2	1
B59	14K27	22	35		
B60	15K23	25	12		
B61	15K19	21	28		
B62	15K31	29	37		
B63	15K27	22	35		
B64	1K23	25	12		
B65	1K19	21	28		
B66	1K31	29	37		
B67	1K27	22	35		
B68	2K23	25	12		
B69	2K19	21	28		
B70	2K31	29	37		
B71	2K27	22	35		

C-REGISTER

REGISTER	FF	NFF
	C	NC
CO	5R18	5R10
1	5R28	36
2	6R18	10
3	6R28	36
4	8R18	10
5	8R28	36
6	9R18	10
7	9R28	36
8	15R18	10
9	15R28	36
10	16R18	10
11	16R28	36
12	17R18	10
13	17R28	36
14	19R18	10
15	19R28	36
16	12M18	10
17	12M28	36
18	13M18	10
19	13M28	36
20	15M18	10
21	15M28	36
22	16M18	10
23	16M28	36
24	3P18	10
25	3P28	36
26	4P18	10
C27	4P28	36
28	5P18	10
29	5P28	36
30	6P18	10
31	6P28	36

CS-REGISTER

REGISTER	FF	N/FF	S/FF	R/FF
CS0	7S27	28	50	
1	7S31	26	46	
2	7S30	29	41	40
3	7S33	34	39	38
4	7S02	21	18	23
5	7S04	5	3	22
6	7S06	7	$	9
7	7814	12	11	15
8	1R27	28	50	45
9	1R31	26	46	44
10	1R30	29	41	40
11	1R33	34	39	38
12	1R02	21	18	23
13	1R04	5	3	22
14	1R06	7	$	9
15	1R14	12	11	15
16	17K27	28	50	45
17	17K31	26	46	44
18	17K30	29	41	40
19	17K33	34	39	38
20	17K02	21	18	23
21	17K04	5	3	22
22	17K14	12	11	15
23	17K06	7	$	9
24	9Q27	28	50	45
25	9Q31	26	46	44
26	9Q30	29	41	40
27	9Q33	34	39	38
28	9Q02	21	18	23
CS29	9Q04	5	3	22
30	9A06	7	$	9
31	9Q14	12	11	15
32	8P02	21	18	23
47	8P06	7	$	9
48	30T27	28	50	45
49	30T31	26	46	44
50	30T30	29	41	40
51	30T33	34	39	38
52	30T02	21	18	23
53	30T04	5	3	22
54	30T14	12	11	15
55	30T06	7	$	9
56	15K27	28	50	45
57	16K31	26	46	44
58	16K30	29	41	40
59	16K33	34	39	38
60	16K02	21	18	23
61	16K04	5	3	22
62	16K14	12	11	15
63	16K06	7	$	9
64	4K27	28	50	45
65	4K31	26	46	44
66	4K30	29	41	40
67	4K33	34	39	38
68	4K02	21	18	23
69	4K04	5	3	22
70	4K14	12	11	15
71	4K06	7	$	9

D-REGISTER

REGISTER	FF	NFF	S/FF	R/FF	C/FF
D0	3R23	25	12	2	1
D1	3R19	21	28		
D2	3R31	29	37		
D3	3R27	22	35		
D4	4R23	25	12		
D5	4R19	21	28		
D6	4R31	29	37		
D7	4R27	22	35		
D8	21R23	25	12		
D9	21R19	21	28		
D10	21R31	29	37		
D11	21R27	22	35		
D12	22R23	25	12		
D13	22R19	21	28		
D14	22R31	29	37		
D15	22R27	22	35		
D16	14P23	25	12		
D17	14P19	21	28		
D18	14P31	29	37		
D19	14P27	22	35		
D20	16P23	25	12		
D21	16P19	21	28		
D22	16P31	29	37	2	1
D23	16P27	22	35		
D24	9P23	25	12		
D25	9P19	21	28		
D26	9P31	29	37		
D27	9P27	22	35		
D28	11P23	25	12		
D29	11P19	21	28		
D30	11P31	29	37		
D31	11P27	22	35		
D47	8P31	26	46	44	
D48	26T23	25	12	2	
D49	26T19	21	28		
D50	26T31	29	37		
D51	26T27	22	35		
D52	22T23	25	12		
D53	27T19	21	28		
D54	27T31	29	37		
D55	27T27	22	35		
D56	18L23	25	12		
D57	18L19	21	28		
D58	18L31	29	37		
D59	18L27	22	35		
D60	19L23	25	12		
D61	19L19	21	28		
D62	19L31	29	37		
D63	19L27	22	35		
D64	5K23	25	12		
D65	5K19	21	28		
D66	5K31	29	37		
D67	5K27	22	35		
D68	6K23	25	12		
D69	6K19	21	28		
D70	6K31	22	35		
D71	6K27	22	35		

E-REGISTER

REGISTER	FF	NFF	S/FF	R/FF	C/FF
E0	14S33	40	36	30	1
E1	14S25	26	31	24	
E2	14S19	21	20	17	
E3	14S05	22	12	3	
E4	15S33	40	36	30	
E5	15S25	26	31	24	
E6	15S19	21	20	17	
E7	15S05	22	12	3	

KNC DATA SWITCH

SIGNAL	TEST POINT
KNC0	29R1
KNC1	29R07
KNC2	29R23
KNC3	29R24
KNC4	29R47
KNC5	29R42
KNC6	29R09
KNC7	29R40
KNC8	29R08
KNC9	29R43
KNC10	29R46
KNC11	29R45
KNC12	28P01
KNC13	28P07
KNC14	28P03
KNC15	28P44
KNC16	28P04
KNC17	28P02
KNC18	29P02
KNC19	29R04
KNC20	32L33
KNC21	32L34
KNC22	32L35
KNC23	32L36
KNC24	28P09
KNC25	28P40
KNC26	28P42
KNC27	28P47
KNC28	28P08
KNC29	28P45
KNC30	28P46
KNC31	28P43

KS DATA SWITCH

SIGNAL	TEST POINT
KS0	26S1
KS1	26S01
KS2	26S03
KS3	26S04
KS4	26S07
KS5	26S08
KS6	26S09
KS7	26S40
KS8	26S42
KS9	26S43
KS10	26S44
KS11	26S45
KS12	26S46
KS13	26S47
KS14	26S46
KS15	32L29
KS16	17N40
KS17	17N46
KS18	17N47
KS19	26K43
KS20	26K45
KS21	26K46
KS22	29M02
KS23	29M04
KS24	17N01
KS25	17N02
KS26	17N03
KS27	17N04
KS28	17N07
KS29	17N08
KS30	32L30
KS31	32L31

KSP ADDRESS SELECT SWITCH

SIGNAL	TEST POINT
KSP15	26K01
KSP16	26K03
KSP17	26K07
KSP18	26K09
KSP19	26K40
KSP20	26K42
KSP21	26K44
KSP22	26K47
KSP23	29M01
KSP24	29M03
KSP25	29M07
KSP26	29M09
KSP27	29M40
KSP28	29M42
KSP29	29M44
KSP30	29M47
KSP31	17N44

KUA UNIT ADDRESS [illegible]

SIGNAL	TEST POINT
KUA21	29M08
KUA22	29M43
KUA23	29M45
KUA24	29M46
KUA25	17M09
KUA26	26K02
KUA27	17N42
KUA28	17N43
KUA29	17N45
KUA30	26K04
KUA31	26K08

Register	FF	NFF	S/FF	R/FF	C/FF
O1	8Q02	21	18	23	1
2	8Q27	28	50	45	1
3	8Q31	26	46	44	1
4	8Q30	29	41	40	1
5	8Q04	5	3	22	1
6	8Q33	34	39	38	1
7	8Q06	7	$	9	1

P-REGISTER

Register	FF	NFF	S/FF	R/FF	C/FF
P15	18K33	40	36	30	1
16	18K25	26	31	24	1
17	18K19	21	20	17	1
18	18K05	22	12	3	1
19	19K33	40	36	30	1
20	19K25	26	31	24	1
21	19K19	21	20	17	1
22	19K05	22	12	3	1
23	22L25	26	31	24	1
24	22L19	21	20	17	1
25	22L05	22	12	3	1
26	23L33	40	36	30	1
27	23L25	26	31	24	1
28	23L19	21	20	17	1
29	23L05	22	12	3	1
30	25L33	40	36	30	1
31	25L25	26	31	24	1
32	25L19	21	20	17	1
33	25L05	22	12	3	1

Q-Register Test Point List

Register	FF	NFF	S/FF	R/FF	C/FF	FF/L
Q15	23K27	28	50	45	1	26K
16	23K31	26	46	44	1	26K
17	23K30	29	41	40	1	26K
18	23K33	34	39	38	1	26K
19	23K2	21	18	23	1	26K
20	23K4	5	3	2	1	26K
21	23K14	12	11	15	1	26K
22	23K6	7	$	9	1	26K
23	24K27	28	50	45	1	26K
24	24K31	26	46	44	1	26K
25	24K30	29	41	40	1	26K
26	24K2	21	18	23	1	26K
27	24K6	7	$	9	1	26K
28	24K33	34	39	38	1	26K
29	24K4	5	3	2	1	29M
30	24K14	12	11	15	1	
31	20L27	28	50	45	1	

FAST MEMORY

REG.	RR	RW	HSM	HSM	HSM	HSM
0	5T2	8S36	1T43	2T43	3T43	4T43
1	5T22	8S41	1T41	2T41	3T41	4T41
2	5T27	8S36	1T09	2T09	3T09	4T09
3	5T34	8S34	1T02	2T02	3T02	4T02
4	5T36	8S45	1T45	2T45	3T45	4T45
5	5T38	8S44	1T46	2T46	3T46	4T46
6	5T40	8S46	1T04	2T04	3T04	4T04
7	5T42	8S47	1T01	2T01	3T01	4T01
8	19T20	22S19	15T43	16T43	17T43	18T43
9	19T22	22S18	15T41	16T41	17T41	18T41
10	19T27	22S05	15T09	16T09	17T09	18T09
11	19T34	22S17	15T02	16T02	17T02	18T02
12	19T36	22S28	15T45	16T45	17T45	18T45
13	19T38	22S27	15T46	16T46	17T46	18T46
14	19T40	22S25	15T04	16T04	17T04	18T04
15	19T42	22S26	15T01	16T01	17T01	18T01
16	5L20	8L19	1L43	2L43	3L43	4L43
17	5L22	8L18	1L41	2L41	3L41	4L41
18	5L27	8L05	1L09	2L09	3L09	4L09
19	5L34	8L17	1L02	2L02	3L02	4L02
20	5L36	8L28	1L45	2L45	3L45	4L45
21	5L38	8L27	1L46	2L46	3L46	4L46
22	5L40	8L25	1L04	2L04	3L04	4L04
23	5L42	8L26	1L01	2L01	3L01	4L01
24	5Q20	6Q19	1Q43	2Q43	3Q43	4Q43
25	5Q22	6Q18	1Q41	2Q41	3Q41	4Q41
26	5Q27	6Q05	1Q09	2Q09	3Q09	4Q09
27	5Q34	6Q17	1Q02	2Q02	3Q02	4Q02
28	5Q36	6Q28	1Q45	2Q45	3Q45	4Q45
29	5Q38	6Q27	1Q46	2Q46	3Q46	4Q46
30	5Q40	6Q25	1Q04	2Q04	3Q04	4Q04
31	5Q42	6Q26	1Q01	2Q01	3Q01	4Q01

S-BUS

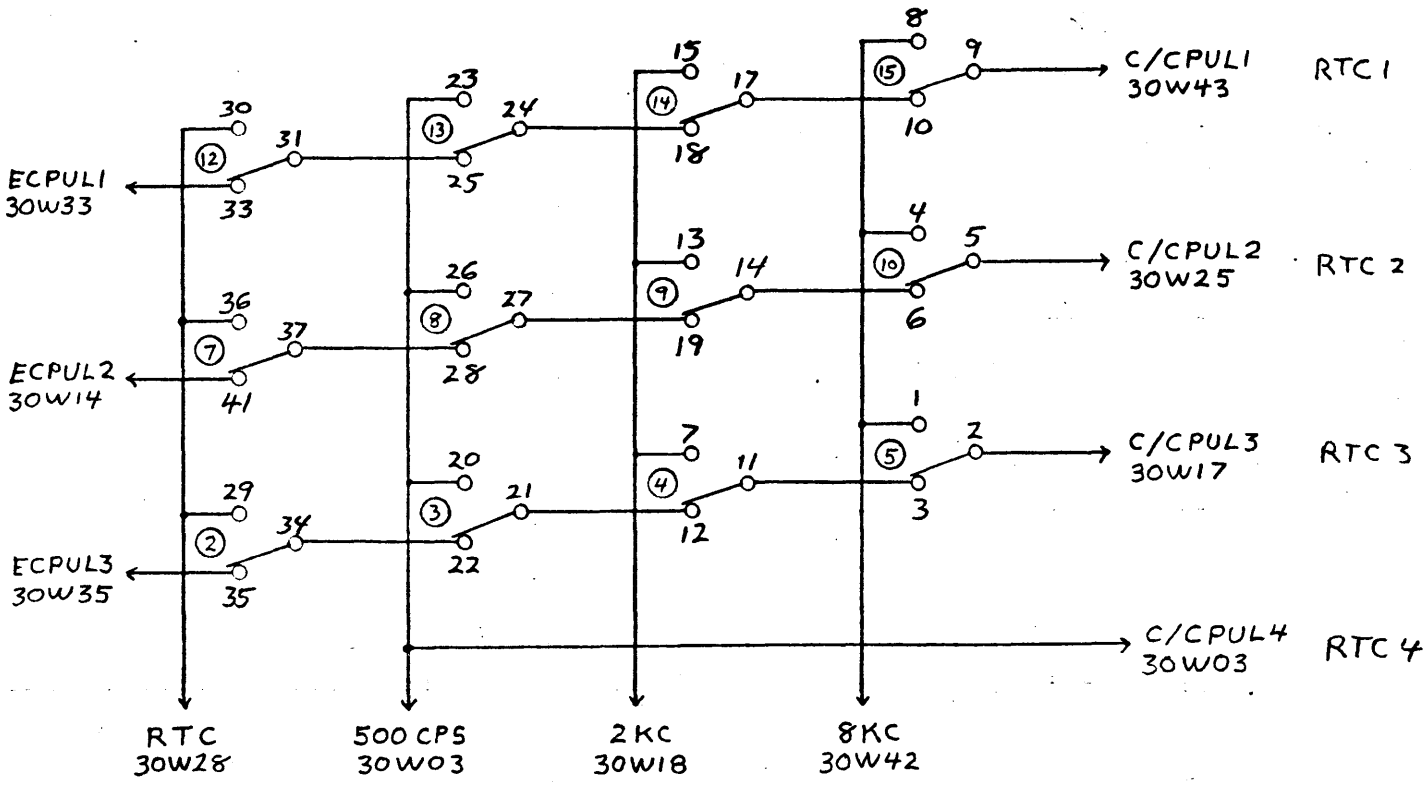
NAME	S
S0	5R15
1	5R33
2	6R15
3	6R33
4	8R15
5	8R33
6	9R15
7	9R33
8	15R15
9	15R33
10	16R15
11	16R33
12	17R15
13	17R33
14	19R15
15	19R33
16	12M15
17	12M33
18	13M15
19	13M33
20	15M15
21	15M33
22	16M15
23	16M33
24	3P15
25	3P33
26	4P15
27	4P33
28	5P15
29	5P33
30	6P15
31	6P33
47	25Q33
48	24R15
49	24R33
50	25R15
51	25R33
52	26R15
53	26R33
54	27R15
55	27R33
56	20M15
57	20M33
58	21M15
59	21M33
60	23M15
61	23M33
62	24M15
63	24M33
64	5M15
65	5M33
66	6M15
67	6M33
68	8M15
69	8M33
70	9M15
71	9M33

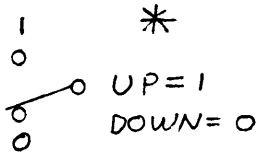
TRANSFER TERMS

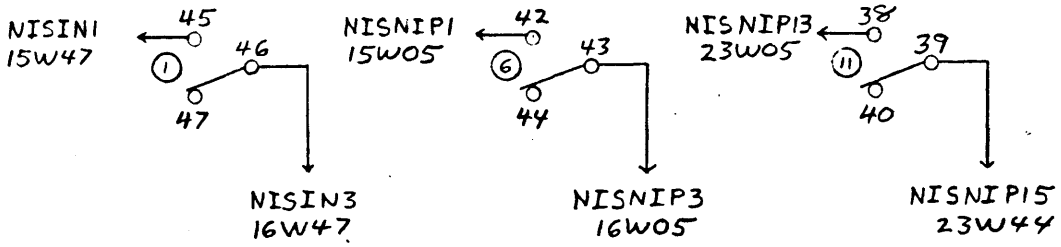
INTERREGISTER

FUNCTION	NAME	FRAME 1	NAME	FRAME 2
0 → A			NAX	31T35
E → A	NAXE	4J25		
PRR → A	NAXPRR	6J30		
R → A			AXR	16N18
RR → A			AXRR	10S25
S → A			AXS	22K26
0's → B			BXB	12T44
S → B			BXS	9S25
0's → CS			CSX1	29S06
0's → D			NDX	28S09
C → D			DXC	14T07
K → D			DXK	12T15
S → E	EXS	2J22		
S → MB	MBXS	2J23		
0's → O			OX	21N09
C → O			OXC	16Q06
S → PSW1	PSW1XS	22F24		
D → PSW2	PSW2XD	5H45		
1's → P	NPX/1	6A02		
2 → P	NPX/2	3A45		
20 → P			PX20	13A28
K → P			PXK	29K35
Q → P			RRWXS	22S10
S → P			PXS/1	29K45
P → Q			QXP-2	25K47
A → S			SXA	12Q26
ADD → S	NSXADD	19G15		
B → S			SXB	29S10
D → S			SXD	29T41
P → S			SXP	25K26
PR → S			SXPR	21T35

D. COCHRANE

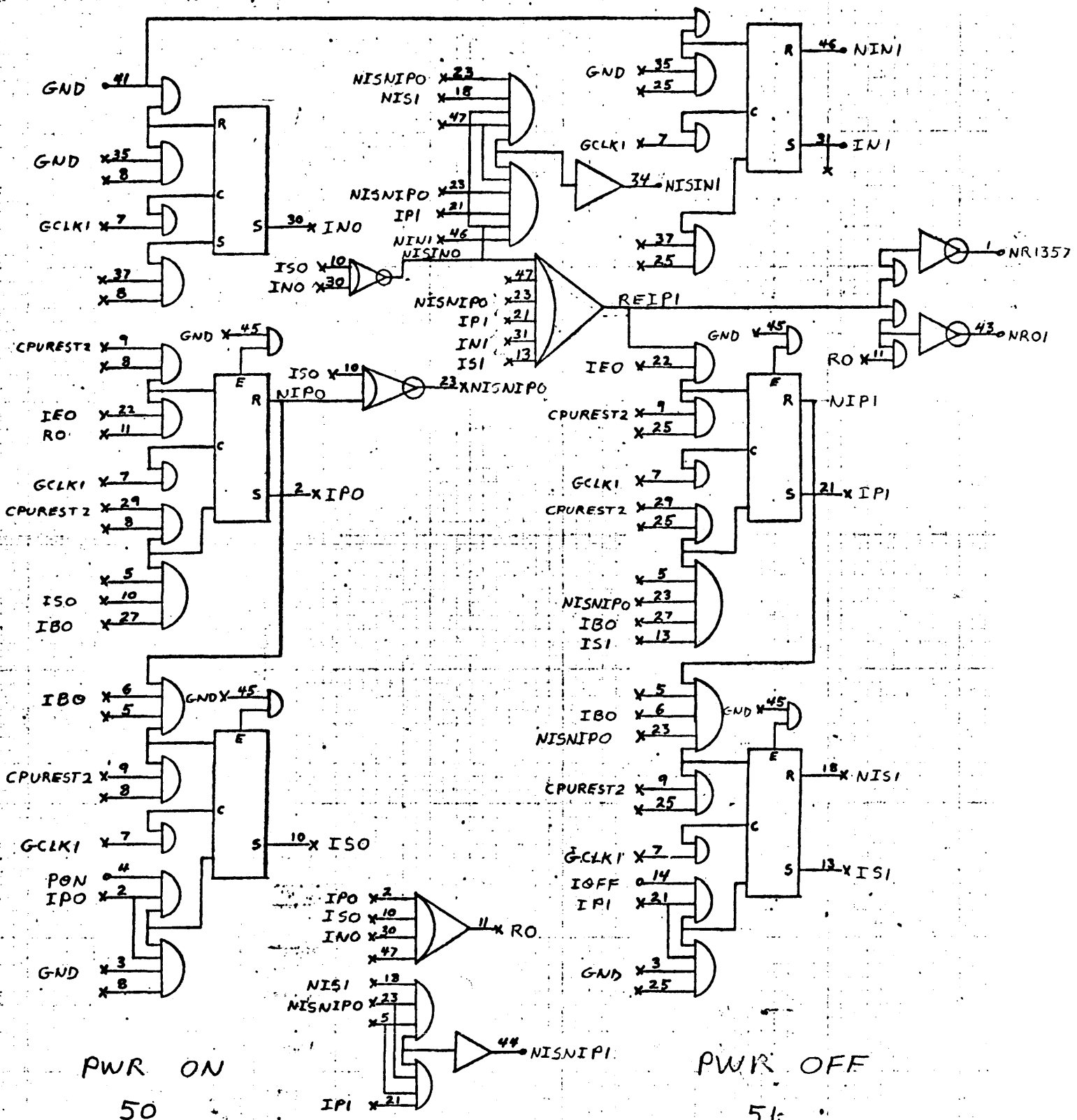






REAL TIME CLOCK MODULE (24W) ST14

Σ7



PWR ON

50

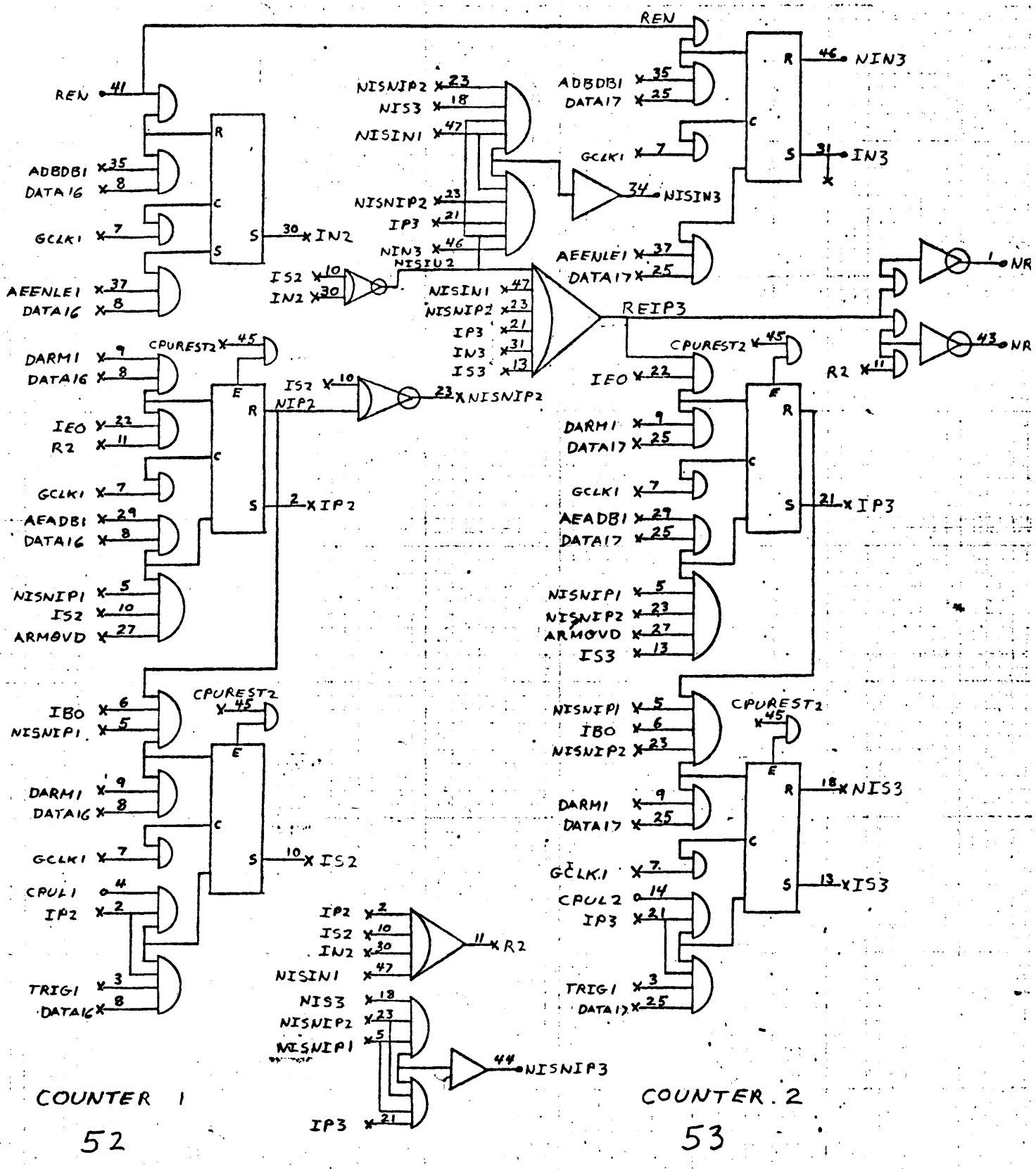
PWR OFF

51

PRIORITY INTERRUPT LT16

14W (OPTIONAL)

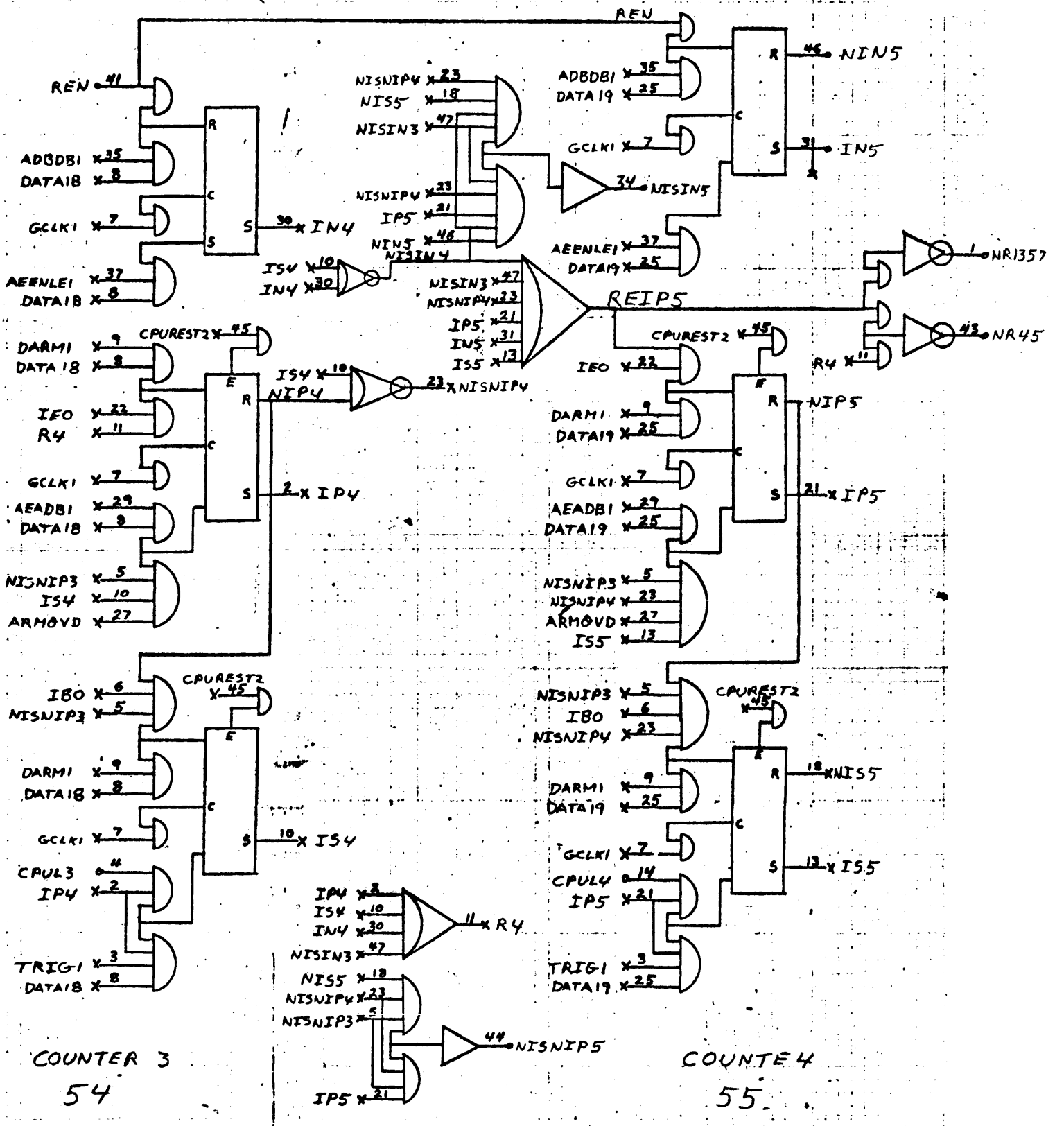
Σ7



PRIORITY INTERRUPT LT16

15W (OPTIONAL)

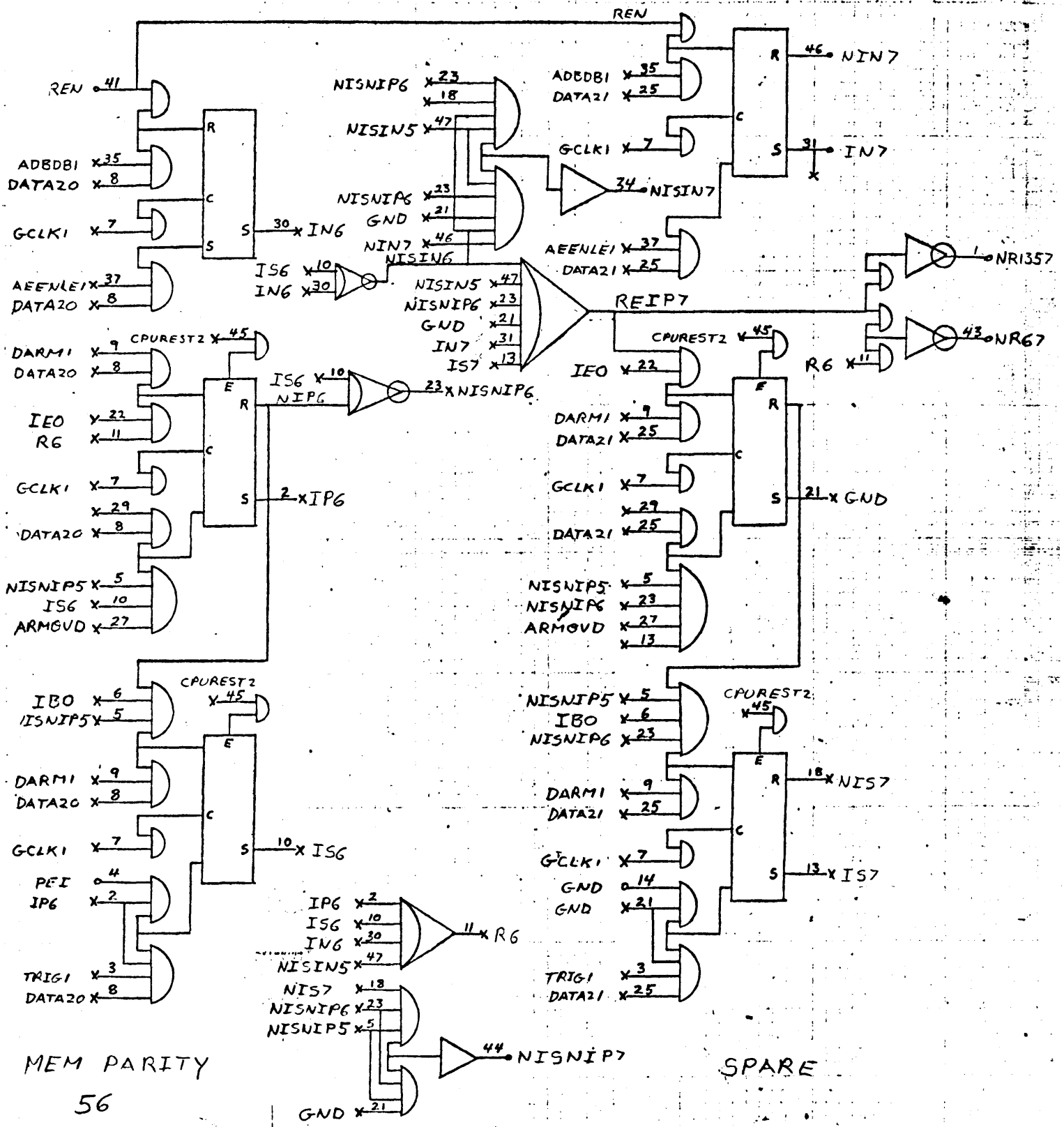
Σ7



PRIORITY INTERRUPT LTIG

16W

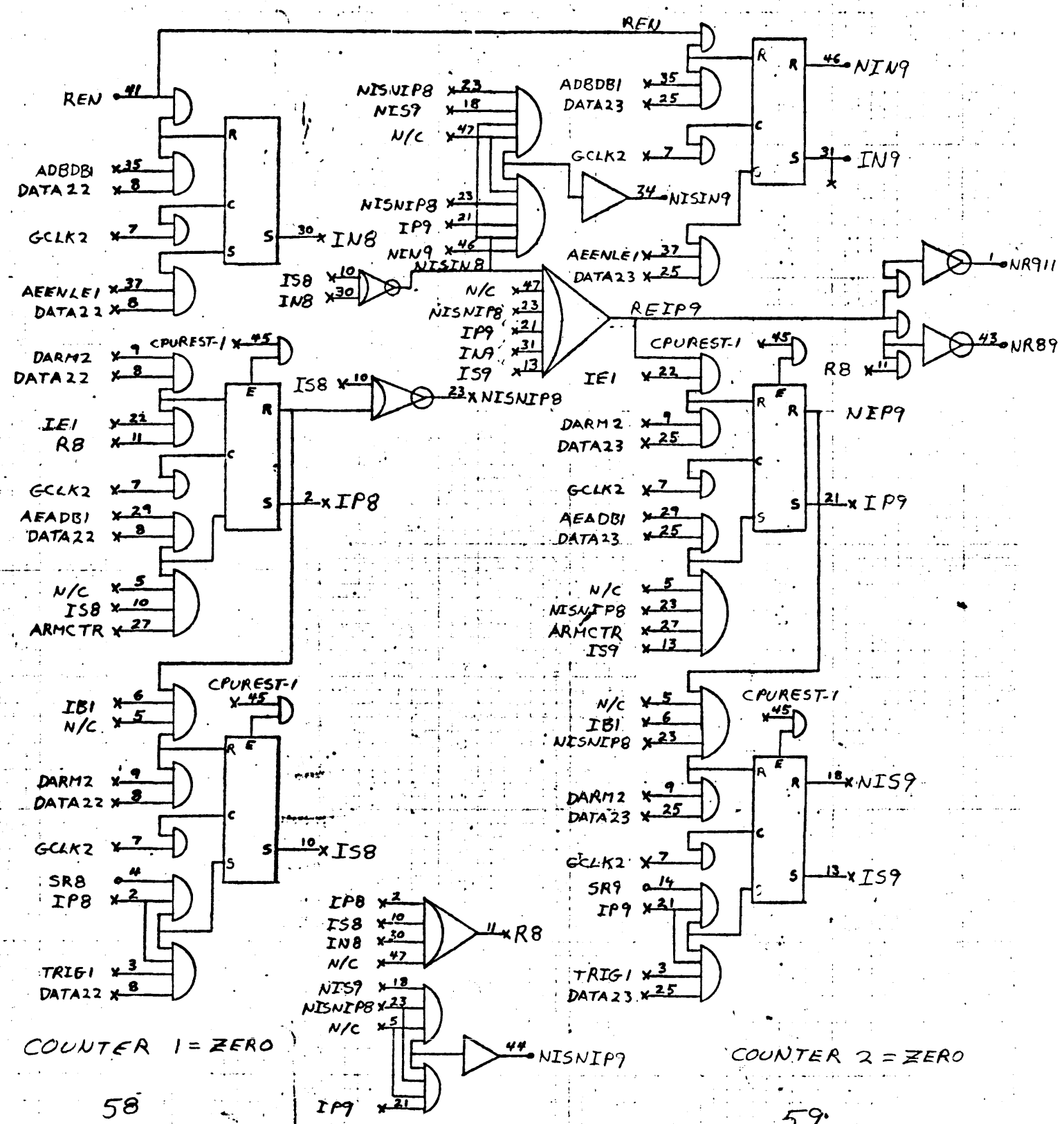
Σ7



PRIORITY INTERRUPT LTIG

17W

Σ7



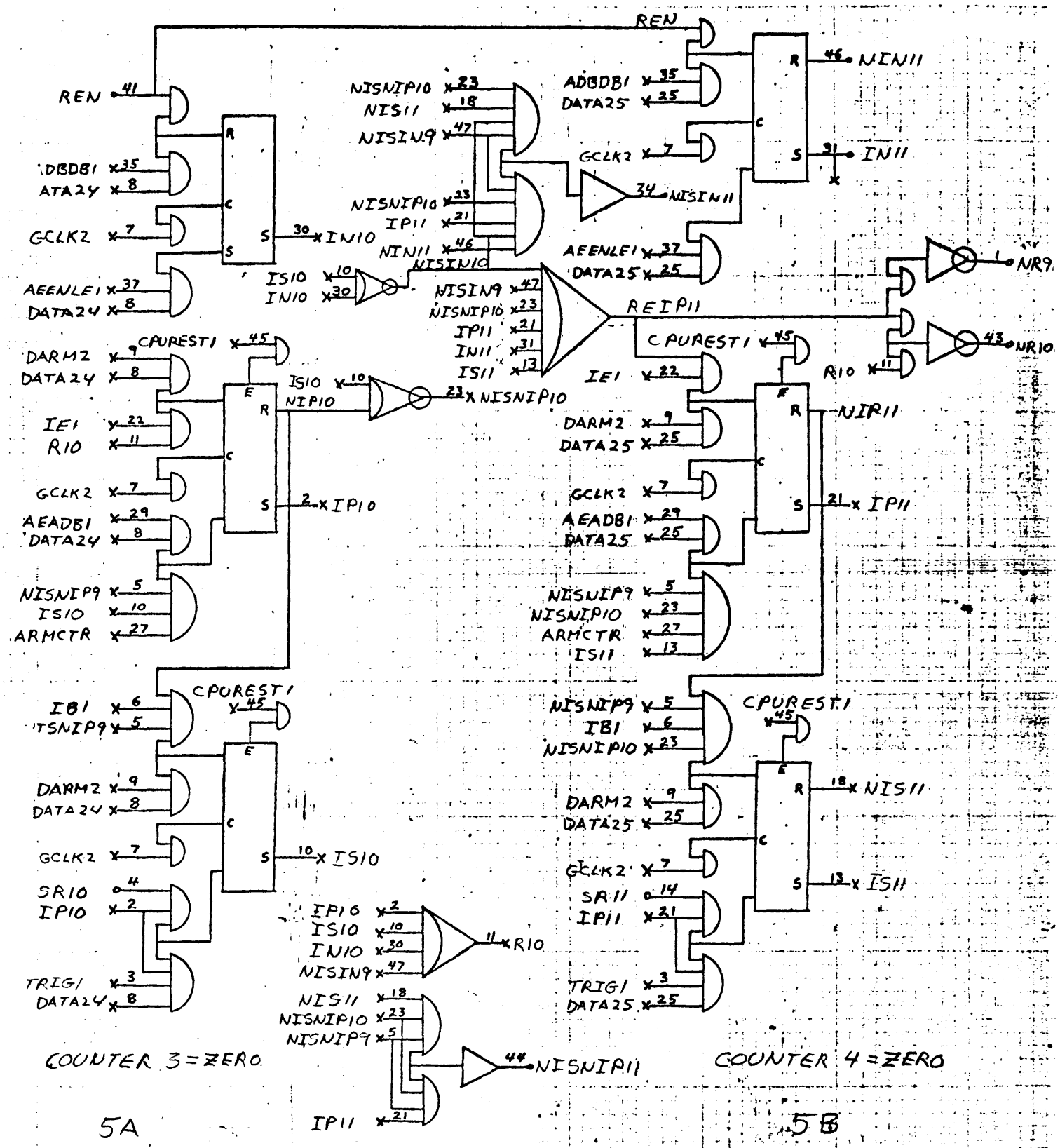
58

59

PRIORITY INTERRUPT LT16

20W

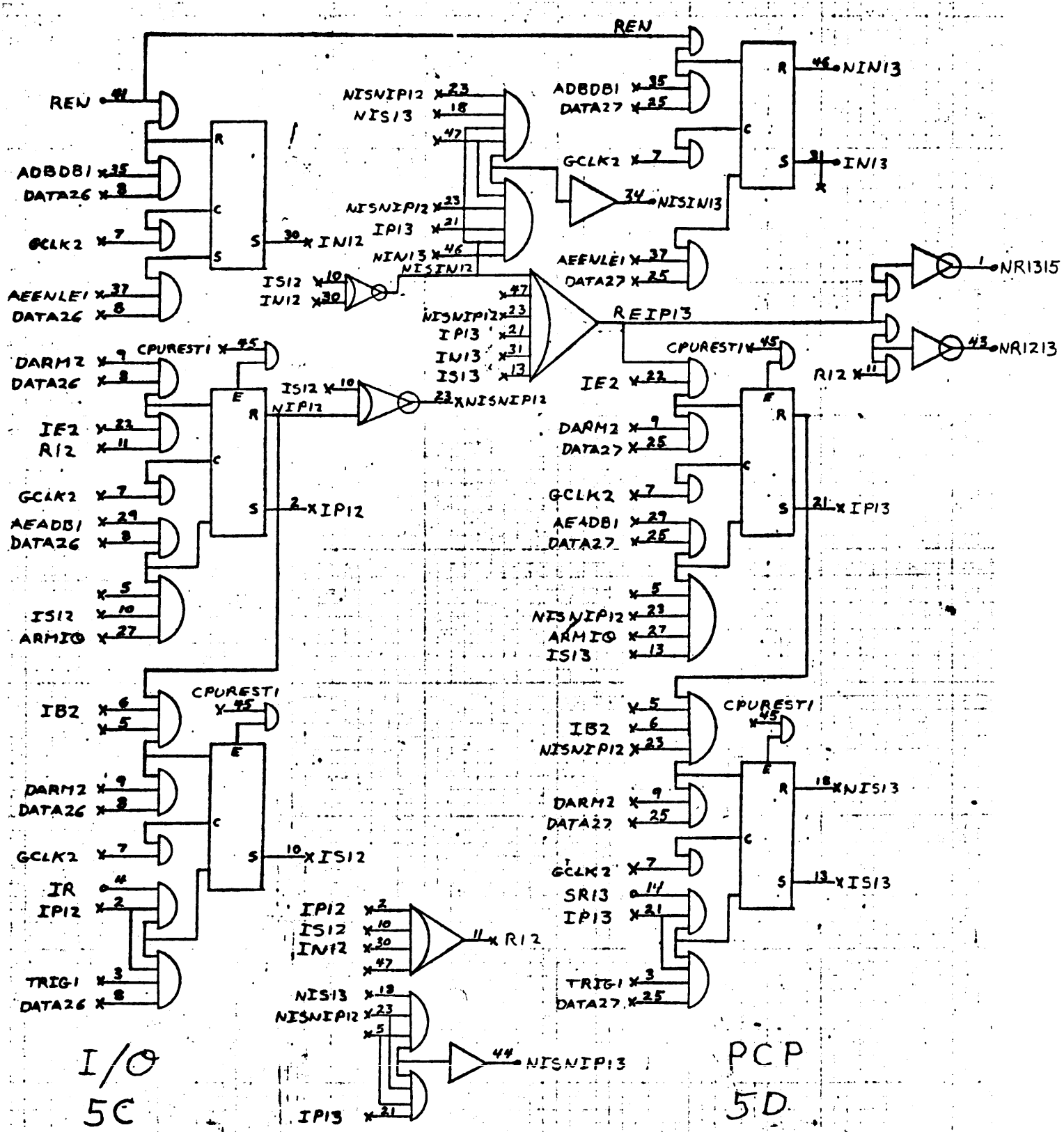
Σ7



PRIORITY INTERRUPT LT16

21W

Σ7



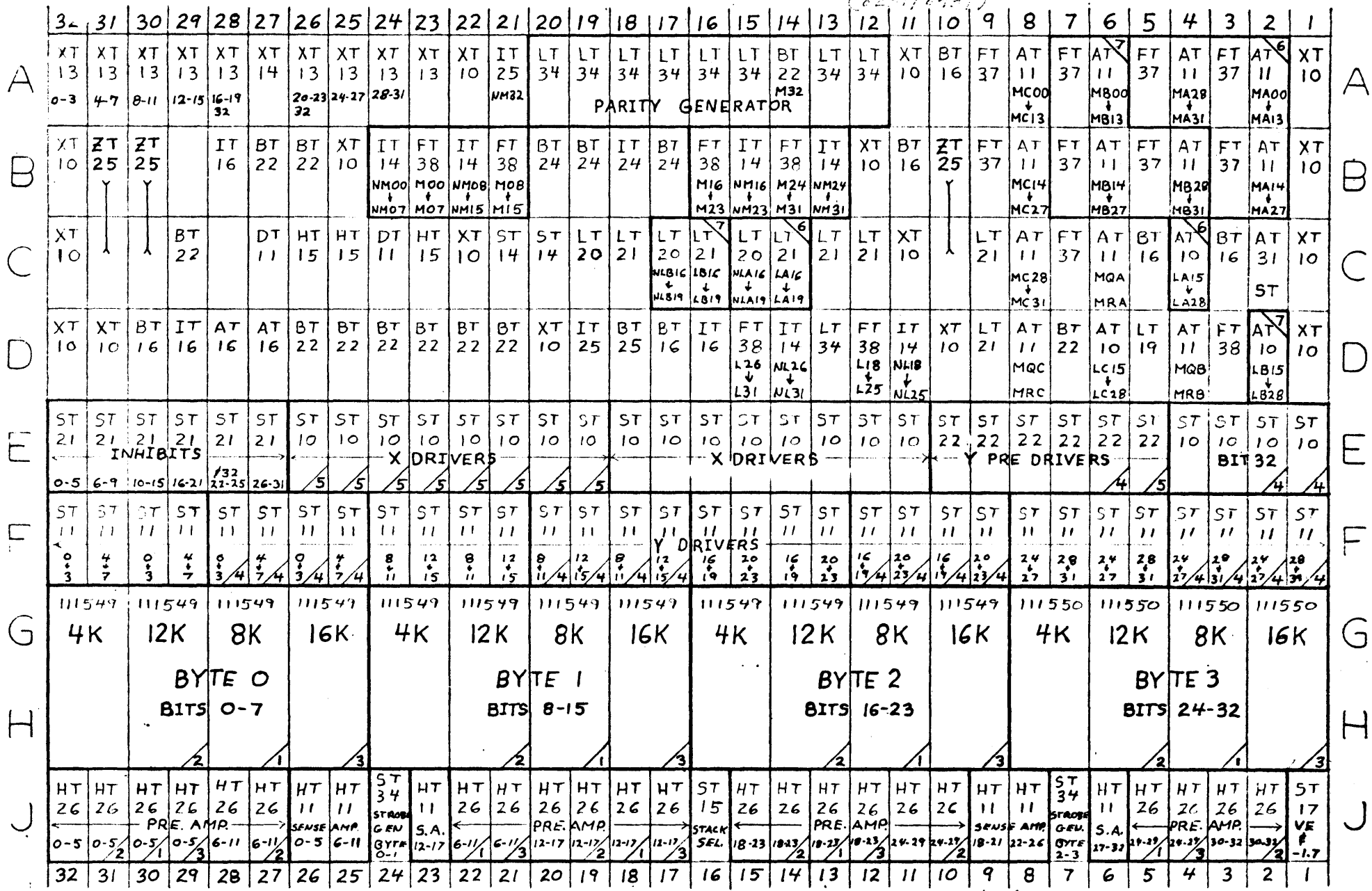
PRIORITY INTERRUPT LT16

22W

Σ7

Σ 5/7 MEMORY 8251

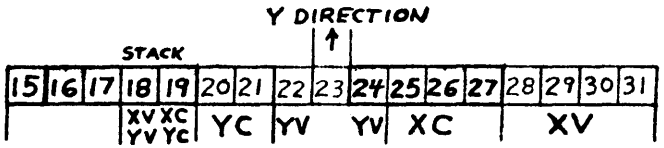
(8251/7/15)



1= 8K	6= 2-3 PORT EXP. } OPTION
2= 12K	7= 1-2 PORT EXP. } 8456
3=16K	
4=OVER 4K	
5=OVER 8K	

VM = 1/2 VD PIN 21 ST11's
* VD = 21.5 PIN 51 F'ROW
VC = 24.00 27A45
VT = 0.35 TOP POT 7/24J15
VS = 3.00 BOTTOM POT 7/24J24
VE = 1 VOLT LESS THAN -8 1J38
-1.7V = 1J18

* Final VD setting should be mid-point of the Schmoo

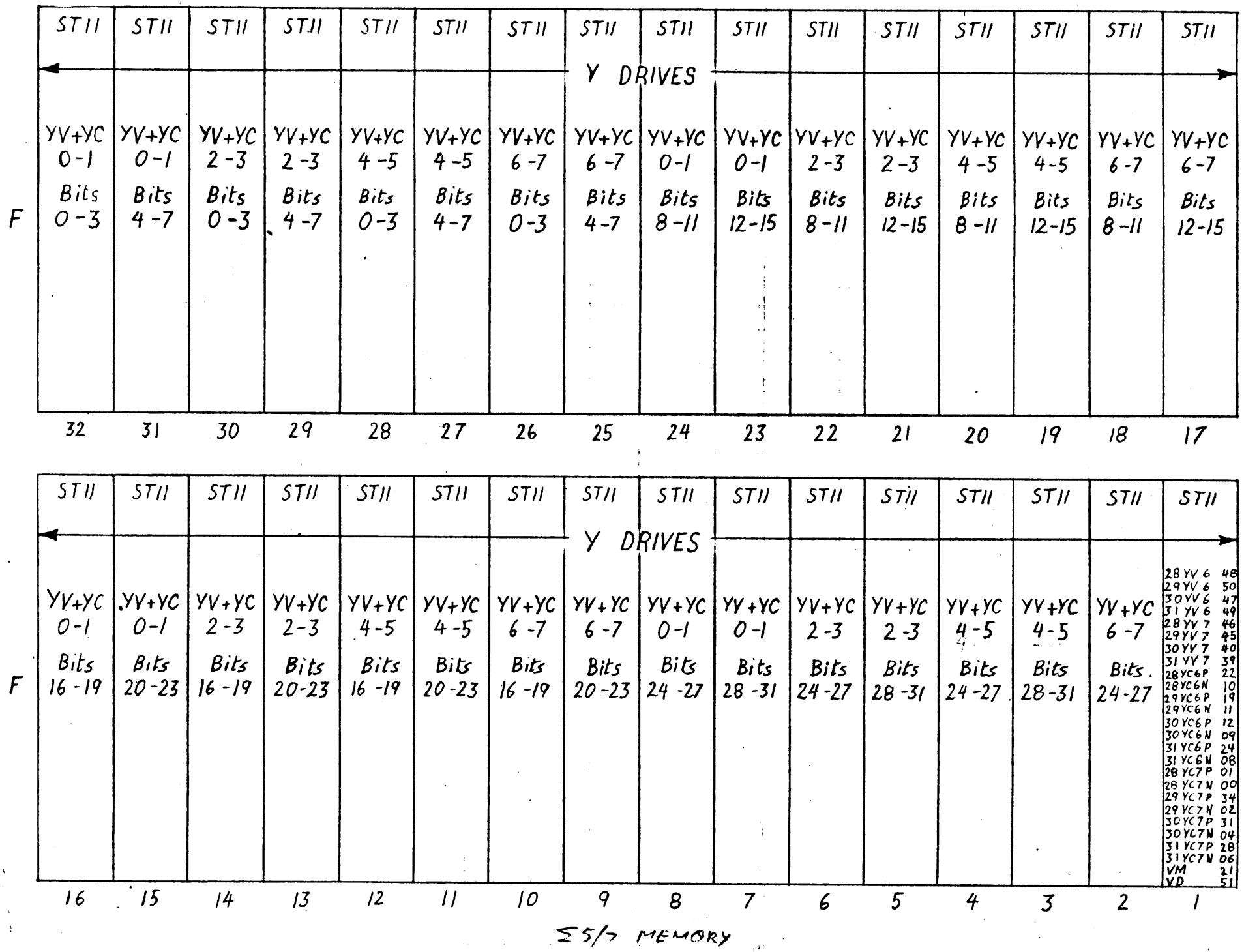


COCHRANE

ST21	ST21	ST21	ST21	ST21	ST21	ST10	ST10	ST10	ST10	ST10	ST10	ST10	ST10	ST10	ST10
← INHIBITS →						← X DRIVES →									
BITS 0-5	BITS 6-9	BITS 10-15	BITS 16-21	BITS 22-25,32	BITS 26-31	XV 30-31	XV 28-29	XV 26-27	XV 24-25	XV 22-23	XV 20-21	XV 18-19	XV 16-17	XV 14-15 XC 14-15	XV 12-13 XC 12-13
E															
0 YPIP 50	6 YPIP 50	10 YPIP 50	16 YPIP 50	22 YPIP 50	26 YPIP 50										
0 YNIN 26	6 YNIN 12	10 YNIN 26	16 YNIN 26	22 YNIN 12	26 YNIN 26										
1 YPIP 46	7 YPIP 46	11 YPIP 46	17 YPIP 46	23 YPIP 46	27 YPIP 46										
1 YNIN 23	7 YNIN 13	11 YNIN 23	17 YNIN 23	23 YNIN 13	27 YNIN 23										
2 YPIP 37	8 YPIP 37	12 YPIP 37	18 YPIP 37	24 YPIP 37	28 YPIP 37										
2 YNIN 12	8 YNIN 11	12 YNIN 12	18 YNIN 12	24 YNIN 11	28 YNIN 12										
3 YPIP 36	9 YPIP 36	13 YPIP 36	19 YPIP 36	25 YPIP 36	29 YPIP 36										
3 YNIN 13	9 YNIN 01	13 YNIN 13	19 YNIN 13	25 YNIN 01	29 YNIN 13										
4 YPIP 34		14 YPIP 34	20 YPIP 34	32 YPIP 34	30 YPIP 34										
4 YNIN 11		14 YNIN 11	20 YNYN 11	32 YNIN 23	30 YNIN 11										
5 YPIP 28		15 YPIP 28	21 YPIP 28		31 YPIP 28										
5 YNIN 01		15 YNIN 01	21 YNIN 01		31 YNIN 01										
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17

ST10	ST10	ST10	ST10	ST10	ST10	ST22	ST22	ST22	ST22	ST22	ST22	ST10	ST10	ST10	ST10
← X DRIVES →						← PREDRIVES →						← BIT 32 Y DRIVES →			
XV 10-11 XC 10-11	XV 8-9 XC 8-9	XV 6-7 XC 6-7	XV 4-5 XC 4-5	XV 2-3 XC 2-3	0 XV 0 48 1 XV 0 50 2 XV 0 47 3 XV 0 49 0 XV 1 46 ! XV 1 45 2 XV 1 40 3 XV 1 39 0 XC 0 P 22 0 XC 0 N 10 1 XC 0 P 19 1 XC 0 N 11 2 XC 0 P 12 2 XC 0 N 09 3 XC 0 P 24 3 XC 0 N 08 0 XC 1 P 01 0 XC 1 N 00 1 XC 1 P 34 1 XC 1 N 02 2 XC 1 P 31 2 XC 1 N 04 3 XC 1 P 28 3 XC 1 N 06 VM 21 VD 51	XPVK 0 50 XPVK 1 46 XPVK 2 37 XPVK 3 36 XNVK 0 34 XNVK 1 28 XNVK 2 14 XNVK 3 18 XNCD 0 12 XNCD 1 13 XNCD 2 11 XNCD 3 01	XPCK 0 50 XPCK 1 46 XPCK 2 37 XPCK 3 36 XNCK 0 34 XNCK 1 28 XNCK 2 14 XNCK 3 18 XPCD 0 12 XPCD 1 13 XPCD 2 11 XPCD 3 01	YPC 0 50 YPC 1 46 YPC 2 37 YPC 3 36 YNC 0 34 YNC 1 28 YNC 2 14 YNC 3 18 XNVD 0 12 XNVD 1 13 XNVD 2 11 XNVD 3 01	YPV 0 50 YPV 1 46 YPV 2 37 YPV 3 36 YNV 0 34 YNV 1 28 YNV 2 14 YNV 3 18 XPVD 0 12 XPVD 1 13 XPVD 2 11 XPVD 3 01	YPC 4 50 YPC 5 46 YPC 6 37 YPC 7 36 YNC 4 34 YNC 5 28 YNC 6 14 YNC 7 18 XNVD 4 12 XNVD 5 13 XNVD 6 11 XNVD 7 01	YPV 4 50 YPV 5 46 YPV 6 37 YPV 7 36 YNV 4 34 YNV 5 28 YNV 6 14 YNV 7 18 XPVD 4 12 XPVD 5 13 XPVD 6 11 XPVD 7 01	YV 0-1 YC 2-3	YV 2-3 YC 2-3	YV 4-5 YC 4-5	32 YV 6 48 32 YV 7 46 32 YC 6 P 22 32 YC 6 N 10 32 YC 7 P 10 32 YC 7 N 00 YM 21 YD 51
E															
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

≡ 5 MEMORY


ST11
Y DRIVES
YV+YC 0-1 Bits 0-3
YV+YC 0-1 Bits 4-7
YV+YC 2-3 Bits 0-3
YV+YC 2-3 Bits 4-7
YV+YC 4-5 Bits 0-3
YV+YC 4-5 Bits 4-7
YV+YC 6-7 Bits 0-3
YV+YC 6-7 Bits 4-7
YV+YC 0-1 Bits 8-11
YV+YC 0-1 Bits 12-15
YV+YC 2-3 Bits 8-11
YV+YC 2-3 Bits 12-15
YV+YC 4-5 Bits 8-11
YV+YC 4-5 Bits 12-15
YV+YC 6-7 Bits 8-11
YV+YC 6-7 Bits 12-15
F
32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17
ST11
Y DRIVES
YV+YC 0-1 Bits 16-19
YV+YC 0-1 Bits 20-23
YV+YC 2-3 Bits 16-19
YV+YC 2-3 Bits 20-23
YV+YC 4-5 Bits 16-19
YV+YC 4-5 Bits 20-23
YV+YC 6-7 Bits 16-19
YV+YC 6-7 Bits 20-23
YV+YC 0-1 Bits 24-27
YV+YC 0-1 Bits 28-31
YV+YC 2-3 Bits 24-27
YV+YC 2-3 Bits 28-31
YV+YC 4-5 Bits 24-27
YV+YC 4-5 Bits 28-31
YV+YC 6-7 Bits 24-27
F
28 YV 6 48
29 YV 6 50
30 YV 6 47
31 YV 6 49
28 YV 7 46
29 YV 7 45
30 YV 7 40
31 YV 7 39
28 YC6P 22
28 YC6N 10
29 YC6P 19
29 YC6N 11
30 YC6P 12
30 YC6N 09
31 YC6P 24
31 YC6N 08
28 YC7P 01
28 YC7N 00
29 YC7P 34
29 YC7N 02
30 YC7P 31
30 YC7N 04
31 YC7P 28
31 YC7N 06
VM 21
VD 51
16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
SS/7 MEMORY

HT26	HT26	HT26	HT26	HT26	HT26	HT11	HT11	ST34	HT11	HT26	HT26	HT26	HT26	HT26	HT26
4K BITS 0-5	12K BITS 0-5	8K BITS 0-5	16K BITS 0-5	4K BITS 6-11	12K BITS 6-11	BITS 0-5	BITS 6-10	STROBES 0-1	BITS 12-17	8K BITS 6-11	16K BITS 6-11	4K BITS 12-17	12K BITS 12-17	8K BITS 12-17	16K BITS 12-17
J	OUTPUT PINS	INPUT PINS				OUTPUT PINS	OUTPUT PINS	OUTPUT PINS	OUTPUT PINS						
	SPA00P 37	4SL00P 09	2SL04P 21			MD00 40	MD06 42	SAST0 29	MD12 38						
	SPA00N 36	4SL00N 08	2SL04N 20			TURN000 43	TURN006 43	SAST1 18	TURN012 39						
	SPA01P 35	5SL00P 11	3SL04P 13			MD01 38	MD07 38	VS 24	MD13 34						
	SPA01N 34	5SL00N 10	3SL04N 12			TURN001 39	TURN007 39	VT 15	TURN013 33						
	SPA02P 41	4SL01P 25	2SL05P 07			MD02 34	MD08 12		MD14 12						
	SPA02N 40	4SL01N 24	2SL05N 06			TURN002 33	TURN008 14	INPUT PINS	TURN014 14						
	SPA03P 39	5SL01P 23	3SL05P 15			MD03 12	MD09 08	NTSSTB 17	MD15 08						
	SPA03N 38	5SL01N 22	3SL05N 14			TURN003 14	TURN009 06	NTSSTB 31	TURN015 06						
	SPA04P 43	4SL02P 03	PASL2 29			MD04 08	MD10 04		MD16 04						
	SPA04N 42	4SL02N 02	PASL3 30			TURN004 06	TURN010 01		TURN016 01						
	SPA05P 45	5SL02P 05	PASL2 33			MD05 04	MD11 34		MD17 40						
	SPA05N 44	5SL02N 04	PASL3 31			TURN005 01	TURN011 33		TURN017 43						
	VE 28	4SL03P 19				-1.7V 02	-1.7V 02		-1.7V 02						
		4SL03N 18				VC 30	VC 30		VC 30						
		5SL03P 27													
		5SL03N 26													
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17

ST15	HT26	HT26	HT26	HT26	HT26	HT26	HT11	HT11	ST34	HT11	HT26	HT26	HT26	HT26	ST17
PASL 0-7	4K BITS 18-23	12K BITS 18-23	8K BITS 18-23	16K BITS 18-23	4K BITS 24-29	12K BITS 24-29	BITS 18-21	BITS 22-26	STROBES 2-3	BITS 27-32	8K BITS 24-29	16K BITS 24-29	4-8K BITS 30-32	12-16K BITS 30-32	-1.7V VE
J	OUTPUT PINS						OUTPUT PINS	OUTPUT PINS	OUTPUT PINS	OUTPUT PINS					OUTPUT PINS
	PASL0 28						MD18 34	MD22 40	SAST2 29	MD27 40					-1.7V 18
	PASL1 30						TURN018 33	TURN022 43	SAST3 18	TURN027 43					Ve 38
	PASL2 26						MD19 12	MD23 38	VS 24	MD28 38					
	PASL3 24						TURN019 14	TURN023 39	VT 15	TURN028 39					INPUT PINS
	PASL4 20						MD20 08	MD24 12		MD29 34					VC 01
	PASL5 18						TURN020 06	TURN024 14	INPUT PINS	TURN029 33					VD 20
	PASL6 22						MD21 09	MD25 08	NTSSTB 17	MD30 12					
	PASL7 03						TURN021 01	TURN025 06	NTSSTB 31	TURN030 14					
							-1.7V 02	MD26 04		MD31 08					
							VC 30	TURN026 01		TURN031 06					
								-1.7V 02		MD32					
								VC 30		TURN032					
										-1.7V 02					
										VC 30					
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

55/7 MEMORY

Bit Location

TURNOVER = Strobe + Core turnover

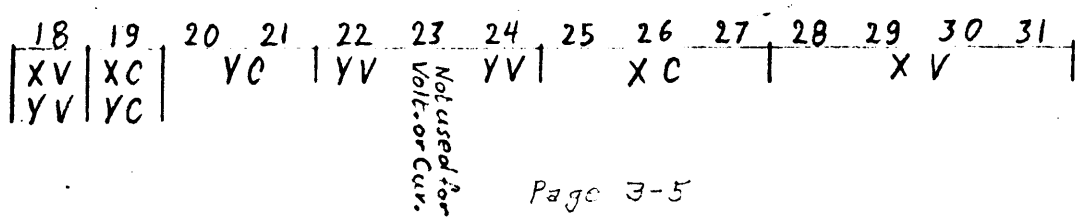
To look at core turnover only ground: 31D17

Strobe Loc.

SAST 0	24 J 29
SAST 1	24 J 18
SAST 2	07 J 29
SAST 3	07 J 18

BIT #	TURNOVER	SENSE AMP OUTPUT		M Reg.	BIT #
0	26 J 43	26 J 40	23 B 45	23 B 37	0
1	26 J 39	26 J 38	23 B 26	23 B 33	1
2	26 J 33	26 J 34	23 B 41	23 B 34	2
3	26 J 14	26 J 12	23 B 42	23 B 35	3
4	26 J 06	26 J 08	23 B 19	23 B 18	4
5	26 J 01	26 J 04	23 B 04	23 B 13	5
6	25 J 43	25 J 40	23 B 07	23 B 14	6
7	25 J 39	25 J 38	23 B 06	23 B 15	7
8	25 J 14	25 J 12	21 B 45	21 B 37	8
9	25 J 06	25 J 08	21 B 26	21 B 33	9
10	25 J 01	25 J 04	21 B 41	21 B 34	10
11	25 J 33	25 J 34	21 B 42	21 B 35	11
12	23 J 39	23 J 38	21 B 19	21 B 18	12
13	23 J 33	23 J 34	21 B 04	21 B 13	13
14	23 J 14	23 J 12	21 B 07	21 B 14	14
15	23 J 06	23 J 08	21 B 06	21 B 15	15
16	23 J 01	23 J 04	16 B 45	16 B 37	16
17	23 J 43	23 J 40	16 B 26	16 B 33	17
18	09 J 33	09 J 34	16 B 41	16 B 34	18
19	09 J 14	09 J 12	16 B 42	16 B 35	19
20	09 J 06	09 J 08	16 B 19	16 B 18	20
21	09 J 01	09 J 04	16 B 04	16 B 13	21
22	08 J 43	08 J 40	16 B 07	16 B 14	22
23	08 J 39	08 J 38	16 B 06	16 B 15	23
24	08 J 14	08 J 12	14 B 45	14 B 37	24
25	08 J 06	08 J 08	14 B 26	14 B 33	25
26	08 J 01	08 J 04	14 B 41	14 B 34	26
27	06 J 43	06 J 40	14 B 42	14 B 35	27
28	06 J 39	06 J 38	14 B 19	14 B 18	28
29	06 J 33	06 J 34	14 B 04	14 B 13	29
30	06 J 14	06 J 12	14 B 07	14 B 14	30
31	06 J 06	06 J 08	14 B 06	14 B 15	31
32	06 J 01	06 J 04	14 A 13	14 A 07	32

L Decode



ST14 (20C)

MQC	5	10	15	0
MQB	4	9	14	
MQA	3	8	13	
AHAEXP	2	7	12	
AHBEXP	1	6 PORT 'B'	11 PORT 'A'	50

ST14 (21C)

5	10	15	0
4	9	14	
3	8 M. FAULT	13	
2	7 MARGIN	12	
1 M. SIZE	6 INTERLEAVE	11 PORT 'C'	50

RULES FOR SETTING UP STARTING ADDRESS

1. MUST BE NO GAPS
2. STARTING ADDRESS MUST BE WHOLE MULTIPLE OF MEMORY SIZE
3. 12K MEMORY SIZE START AT MULTIPLES OF 16K (0, 16, 32, 48 ETC.)

0-16K-1 | 24-28K-1 | 16-24K-1 | 28-32K-1 → OK

16K	4K	8K	4K

20-28K-1 → NOT OK

STARTING ADD.	L15 SW6 / SW11	L16 7 / 12	L17 8 / 13	L18 9 / 14	L19 10 / 15	20C PORT B / (20C PORT A)(21C PORT C)
OK	0	0	0	0	0	
4K	0	0	0	0	1	
8K	0	0	0	1	0	
12K	0	0	0	1	1	4K INCREMENTS
16K	0	0	1	0	0	
20K	0	0	1	0	1	
24K	0	0	1	1	0	
28K	0	0	1	1	1	
32K | 48K	0 ↕ 0	1 ↕ 1	0 ↕ 1	0 ↕ 0	0 ↕ 0	
64K	1	0	0	0	0	
80K	1	0	1	0	0	16K INCREMENTS
96K	1	1	0	0	0	
112K	1	1	1	0	0	
128K	1	1	1	1	1	

*NOTE ENDING ADDRESS DETERMINED BY MEMORY SIZE SWITCHS

21C

MEM SIZE	SW1	SW2
4K	0	0
8K	0	1
12K	1	0
16K	1	1

INTERLEAVING SWITCHS

1. SET SAME VALUE ALL DOORS
2. TOTAL MEM. SIZE MUST BE EQUAL TO 8K, 16K, 32K OR 64K

21C

TOTAL M. SIZE	SW6	SW5	SW4	SW3
8K	0	0	0	1
16K	0	0	1	0
32K	0	1	0	0
64K	1	0	0	0

MEMORY FAULT LIGHTS

21C

LITE	SW8	SW9	SW10
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

MEMORY TIMING MARGINS

21C

SW7	SPEED	
0	SLOW	(DOWN)
1	FAST	(UP)

Σ 5/7 MEMORY SWITCHS

PORT EXPANDER CABLING (TYPICAL)

STARTING ADD. SW's

1st PORT EXPANDER

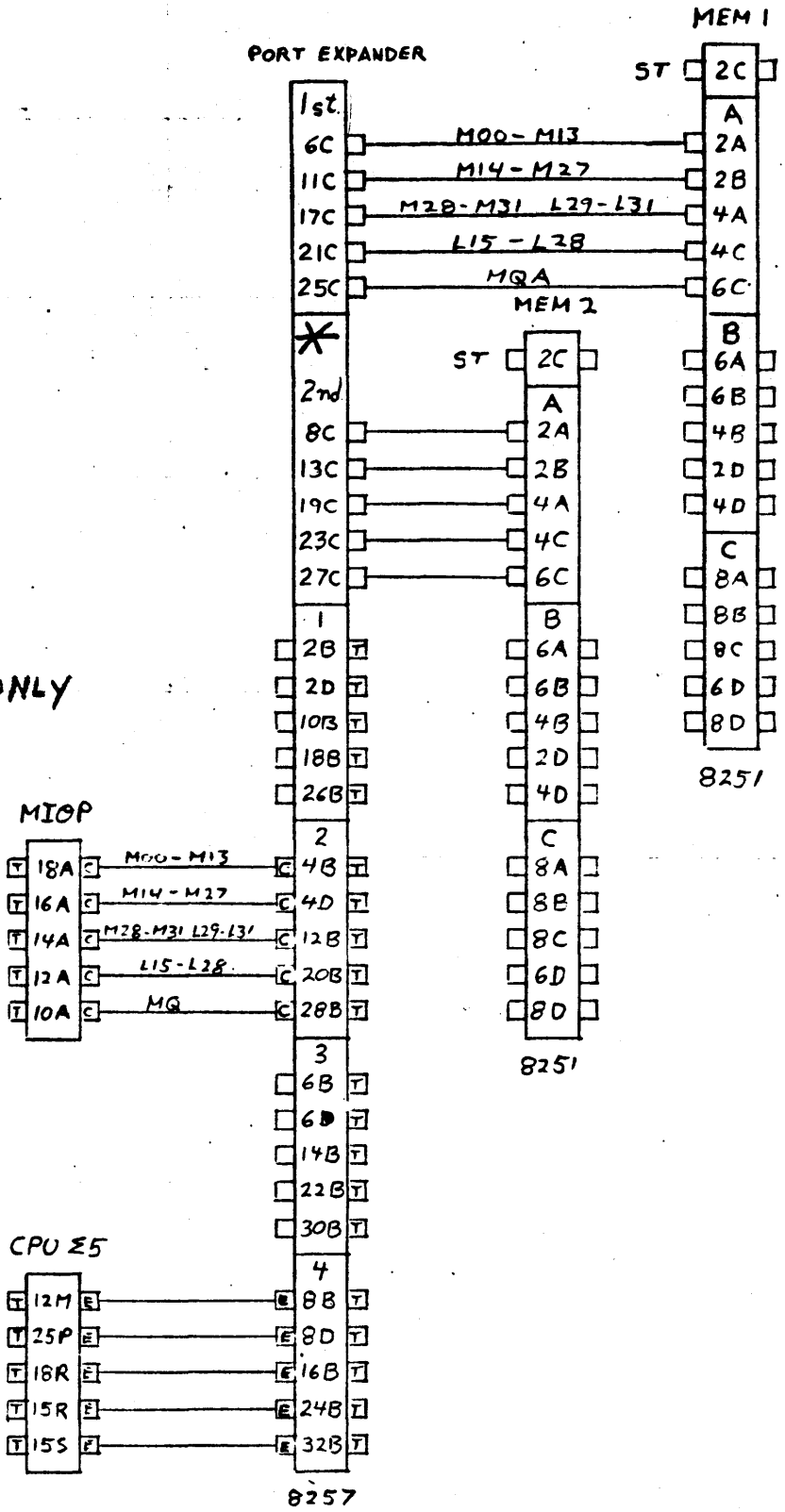
PORT	L15	L16	L17	L18	L19	
1	1	2	3	4	5	24D
2	6	7	8	9	10	
3	1	2	3	4	5	25D
4	6	7	8	9	10	

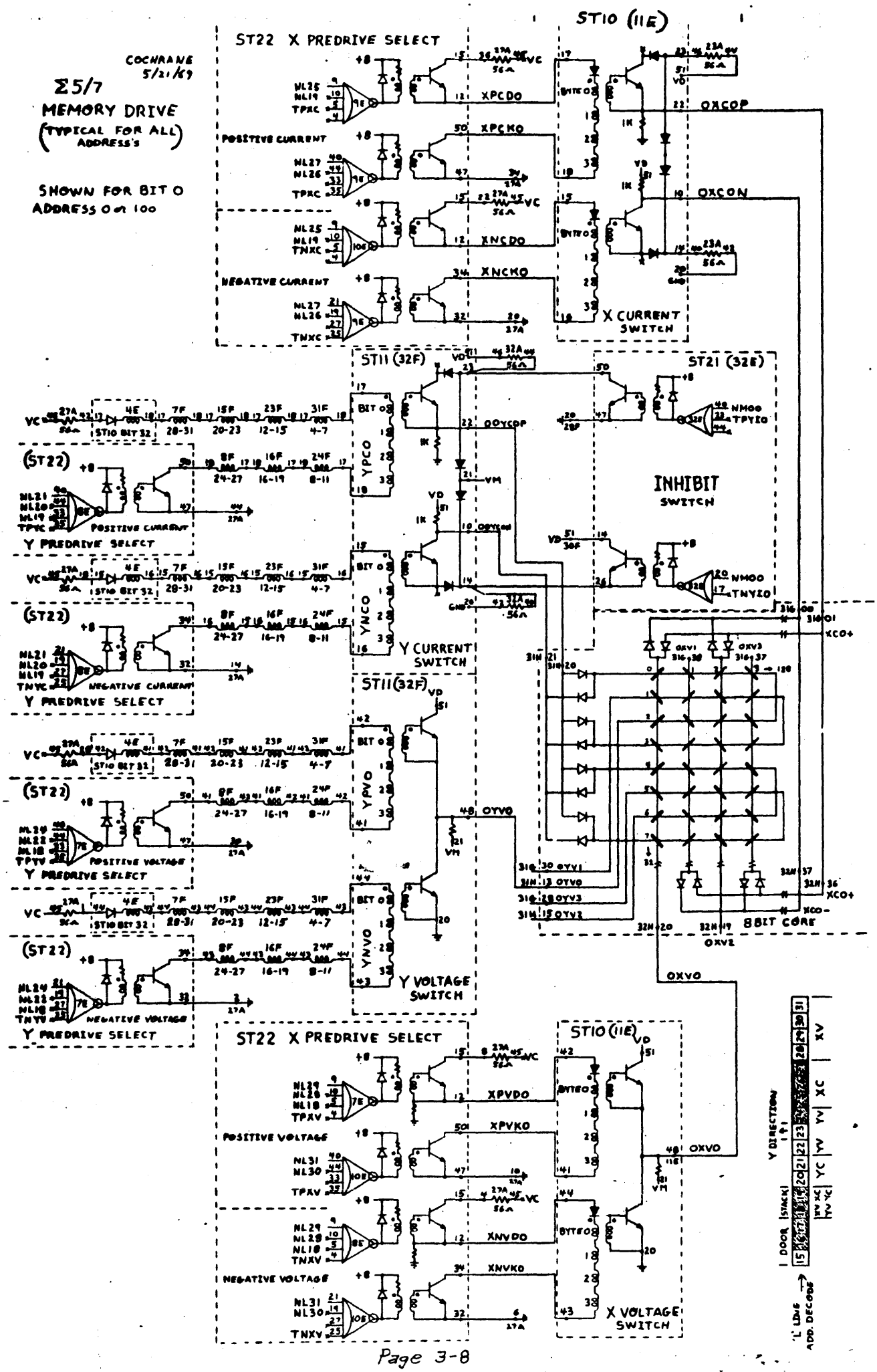
2d PORT EXPANDER

*

PORT	L15	L16	L17	L18	L19	
1	1	2	3	4	5	21E
2	6	7	8	9	10	
3	1	2	3	4	5	22E
4	6	7	8	9	10	

* DUAL EXPANDER ONLY



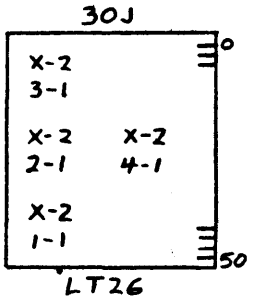

COCHRANE 5/21/69
Σ5/7 MEMORY DRIVE (TYPICAL FOR ALL ADDRESS'S)
SHOWN FOR BIT O ADDRESS O OR 100
ST22 X PREDRIVE SELECT
ST10 (11E)
POSITIVE CURRENT
NEGATIVE CURRENT
XPCDO
XPCKO
XNCDO
XNCKO
OXCOP
OXCON
X CURRENT SWITCH
ST11 (32F)
ST21 (32E)
INHIBIT SWITCH
YPCO
YNCO
Y CURRENT SWITCH
Y PREDRIVE SELECT
POSITIVE VOLTAGE
NEGATIVE VOLTAGE
YPVO
YNVO
Y VOLTAGE SWITCH
OYVO
OXVO
8 BIT CORE
XPVDO
XPVKO
XNVDO
XNVKO
X VOLTAGE SWITCH
Y DIRECTION
1 DOOR STACK
'L' LOAD ADD. DECODE
Page 3-8

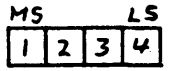
PRIORITY INTERRUPT CHASSIS
MODEL 8421

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AT 11		LT 26		AT 13		AT 11		BT 17	BT 16	IT 25	BT 17		AT 11		LT 16 /1	LT 16 /1	LT 16 /1	LT 16 /1		AT 11		LT 16 /1	LT 16 /1	LT 16 /1	LT 16 /1	IT 25	BT 18	XT 10	FT 10		ST 14

1 = OPTIONAL NO. OF LEVELS 8422
2 LEVELS PER LTI6

LOGIC EQUATION 124470-001
WIRE LIST 124472-001
PIN INDEX 124472-925





0 1 0 1 = GROUP 5

X = SW's NOT USED

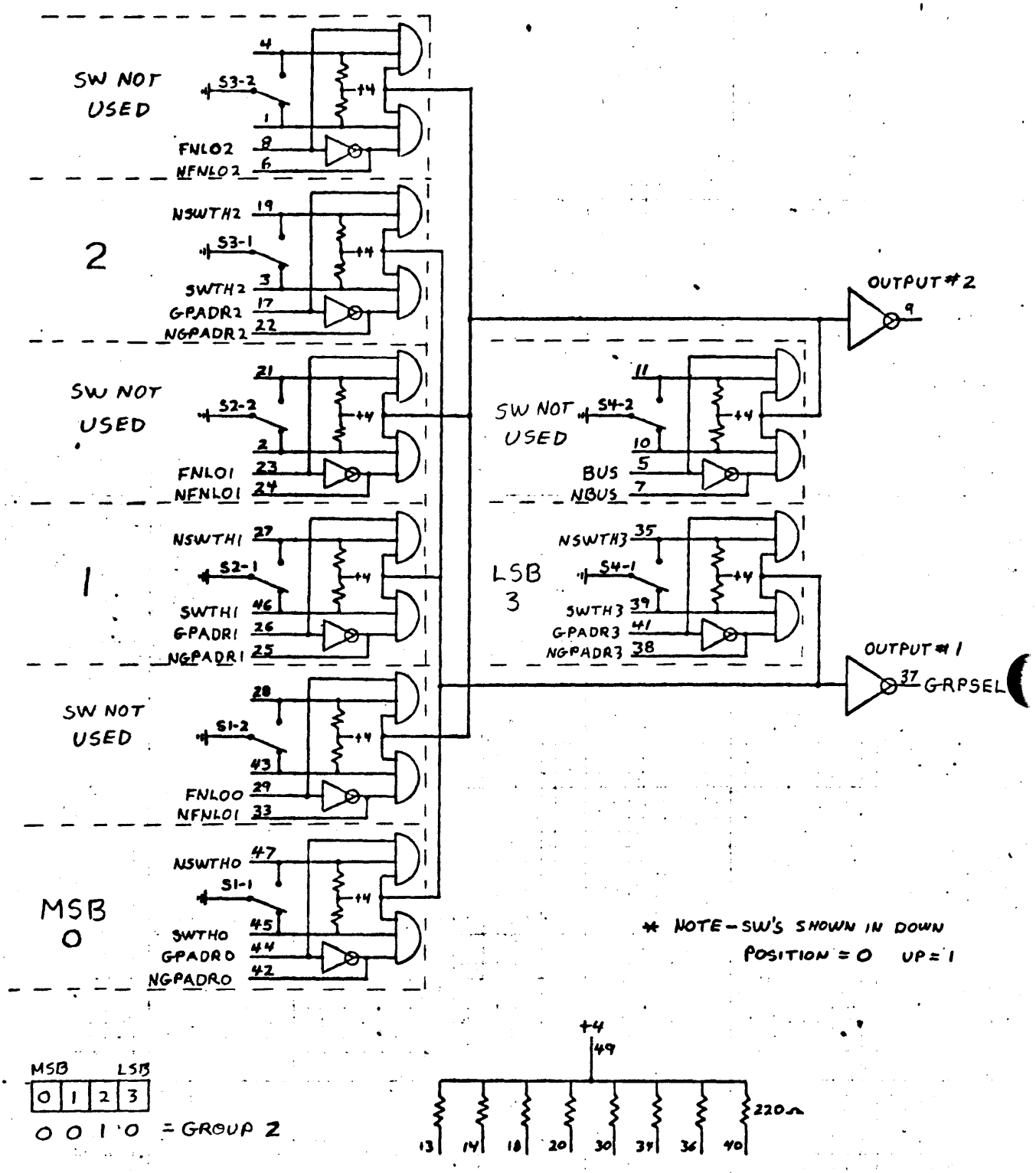
LTIC	LEVEL	ST14 IJ
7J	X0	NONE
	X1	
8J	X2	SW1
	X3	SW2
9J	X4	SW3
	X5	SW4
10J	X6	SW5
	X7	SW6
14J	X8	SW7
	X9	SW8
15J	XA	SW9
	XB	SW10
16J	XC	SW11
	XD	SW12
17J	XE	NONE
	XF	SW13

SW's TO 1 = UP POSITION FOR EACH LTI6

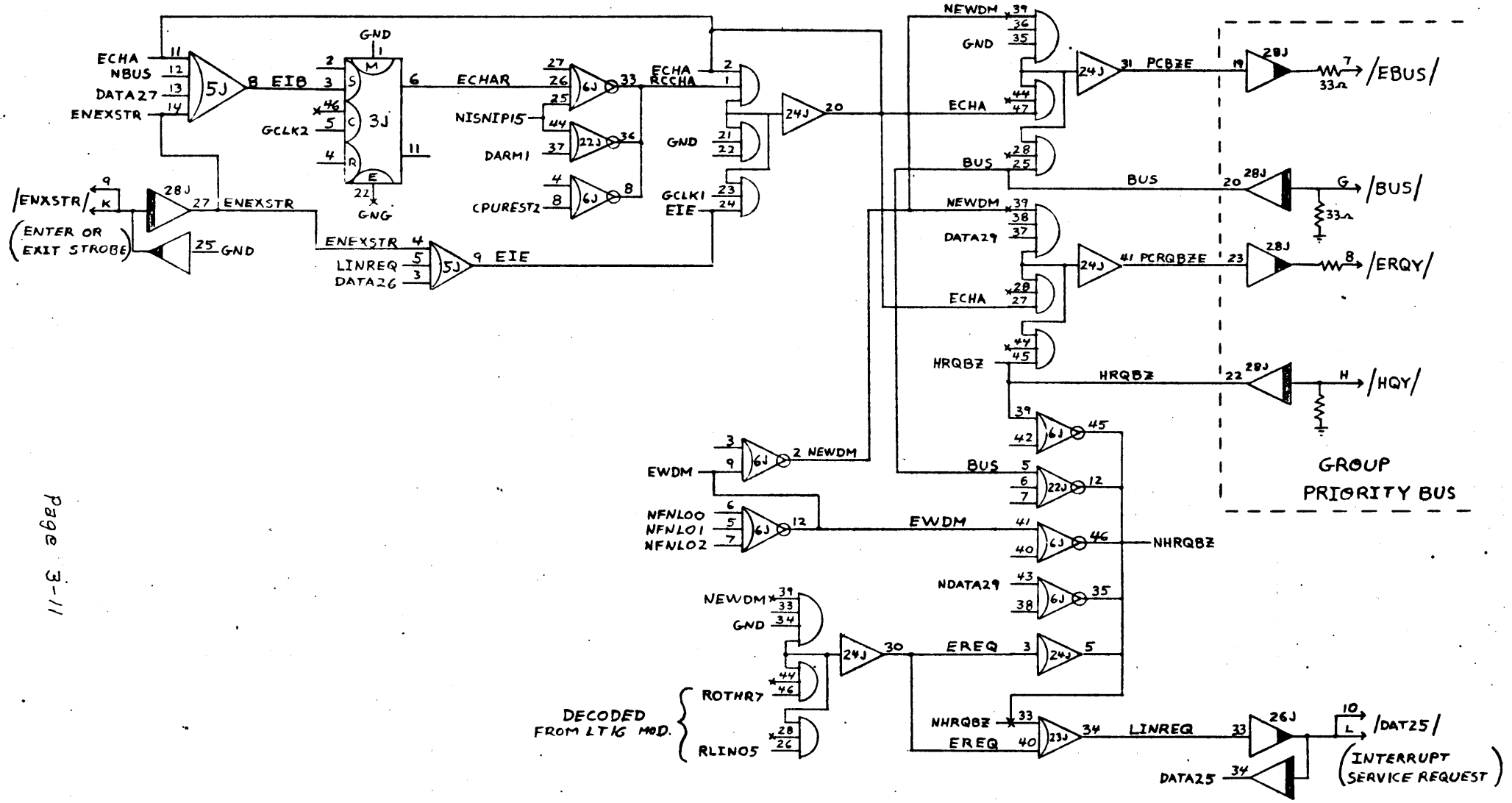
LT26 SWITCH MODULE

COCHRANE

30J EXT. PRI. INT.



EXT. INTERRUPT LT26 (30J)
SWITCH SETTING



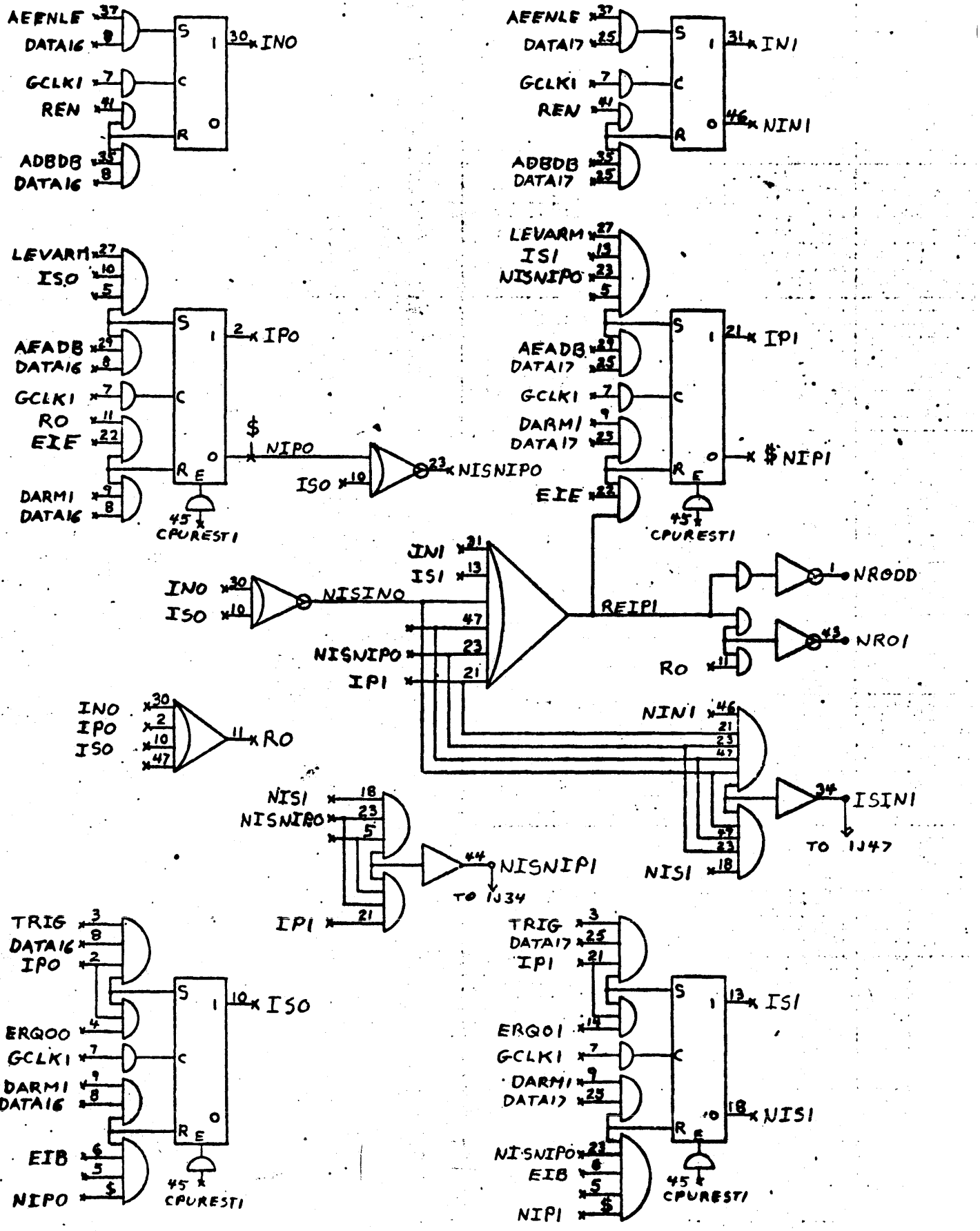
'H' REV.

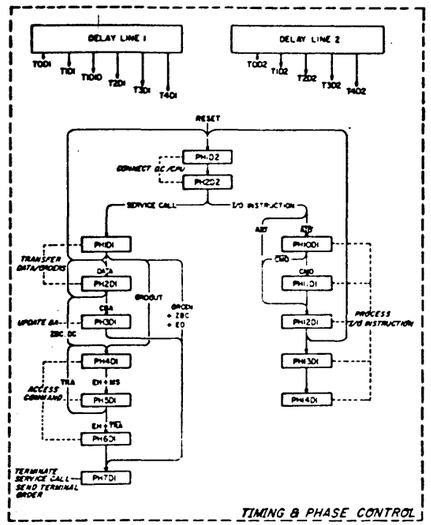
EXTERNAL INTERRUPT CHASSIS 8021

SERVICE & PRIORITY LOGIC

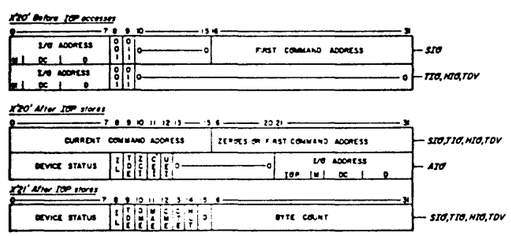
LTI6 INTERRUPT

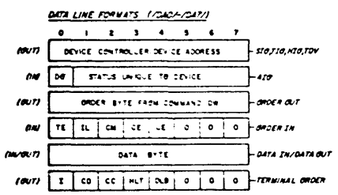
(7J) EXT. PRI. INT. CHASSIS Σ 5/7 f 2

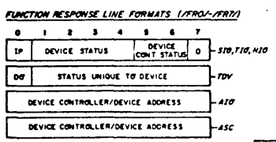


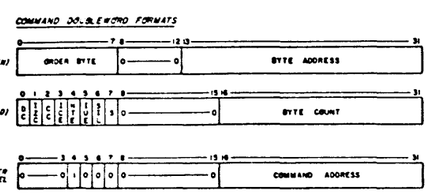


TIMING & PHASE CONTROL





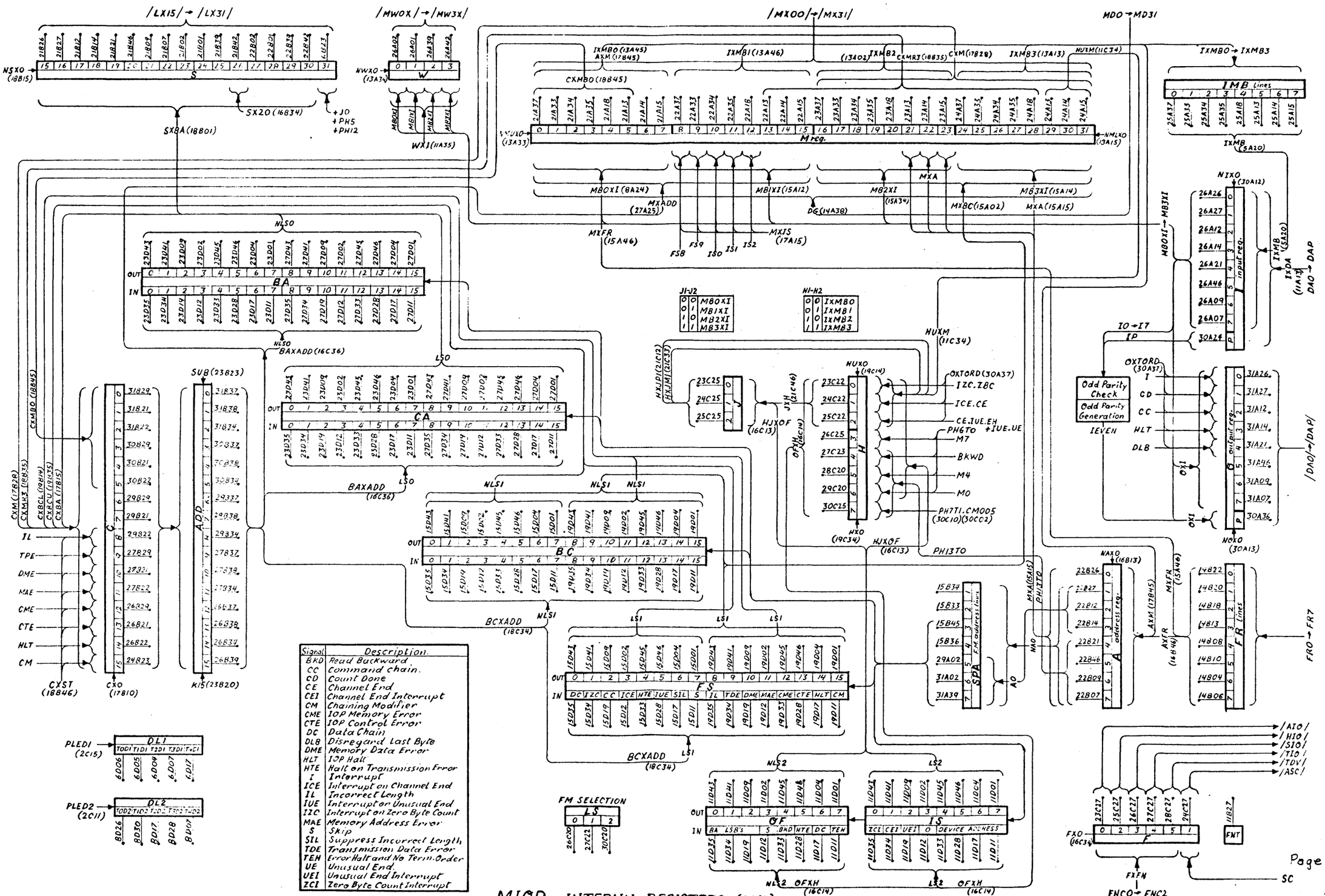




BKD	Read backward
CC	Command chaining.
CD	Count Done
CE	Channel end
CEI	Channel end interrupt.
CM	Chaining modifier.
CME	IOP memory error.
CTE	IOP control error
DC	Data chaining
DLB	Disregard last byte
DME	Memory data error
DO	Data overrun
HLT	IOP Halt
HTE	Hall on transmission error
I	Interrupt
ICE	Interrupt at channel end
IL	Incorrect length
IP	Interrupt pending
IUE	Interrupt on unusual end
IZC	Interrupt at zero byte count
MAE	Memory address error
S	Skip
SIL	Suppress Incorrect length
TDE	Transmission data error
TE	Transmission error
TEH	Remember EH
UE	Unusual end
UEI	Unusual end interrupt
ZCI	Zero byte count interrupt.

(8Bit) SIGMA MULTIPLEXOR IOP FUNCTIONAL DIAGRAM

MT-CH-MIOP-3



Signal	Description
BKD	Read Backward.
CC	Command Chain.
CD	Count Done
CE	Channel End
CEI	Channel End Interrupt
CM	Chaining Modifier
CME	IOP Memory Error
CTE	IOP Control Error
DC	Data Chain
DLB	Disregard Last Byte
DME	Memory Data Error
HLT	IOP Halt
HTE	Halt on Transmission Error
I	Interrupt
ICE	Interrupt on Channel End
IL	Incorrect Length
IUE	Interrupt on Unusual End
IZC	Interrupt on Zero Byte Count
MAE	Memory Address Error
S	Skip
SIL	Suppress Incorrect Length
TDE	Transmission Data Error
TEH	Error Halt and No Term. Order
UE	Unusual End.
UEI	Unusual End Interrupt
ZCI	Zero Byte Count Interrupt

MIOP INTERNAL REGISTERS. (8bit)

Note: Every PH#D1/2 (phase term) is reset at T3 time of its delay line.
Every PH#PD1/2 (phase term) is set at T3 time of its delay line and reset at T0 time of its delay line.
Leaving PH2PD2 and PH7PD1 or PH14PD1 high untill the next operation.

CPU

SIO PHASE SEQUENCE (8 bit MIOP)

CNST(12C20)
ICPA0(12C08)
ICPA1(12C19)
ICPA2(12C18)
ENCO(12C09)
ENC1(12C04)
ENC2(12C10)

PH1D2 (4C22) : Determine and initiate next operation.
PLED2(2C11) = ME (17A19) = IOP address recognition.
TOD2 : FNT (11B27) (8D26) CPU function
T2D2 : F3 (26C27) = /SIO/ (8D17)
T4D2 : PH2D2 (5C25) (8D07)

/SIO/(14C12)

PH2D2 (5C25) : Access location 20.
PLED2(2C11) = FIN (11B23) = End of previous operation.
/MQX/(10A01)
TOD2 : SX20 (16B34) (8D26) set Sreg. to location 20
T1D2 : LS0 (26C20) (8D30) LS1 (27C22) LS2 (30C20) CC1 (23B26) CC2 (24B26) MS (2A22) = MQ
T3D2 : IXMB (5A20) (8D28) MO→M7 to IMBO→IMB7 IMBO→IMB7 to Ireg. PH10D1 (7B01)

/FS/(14C35)
/DA0/(32A23)
/DA1/(32A19)
/DA2/(32A15)
/DA3/(32A12)
/DA4/(32A03)
/DA5/(32A07)
/DA6/(32A01)
/DA7/(32A02)
DALines
D.C. ADDRESS

PH10D1 (7B01): [M8] Set up and store 1rst return status word.
[NM8] Set up 2nd return status word.
POK(10A27)
PLED1(2C15) = MDR1 parity OK sets MDR1
/MQX/(10AD1)
T0D1 : 0XI (5A23) (6D06) AXM (17B45) M0→M7 to Areg. M8 sets CMD (24B20) M9 sets TPE (5C20) WX1 (11A35) set W0→W3 for write.
T2D1 : FS (14C35). [CMD]: CXBA (17B15) CA reg. to Creg. [NCMD]: CXM (17B28) M16→M31 to Creg.
T4D1 : MXADD (27A25) (6D17) Creg. -1 to M0→M15 [CMD]: MS (2A22) PH11D1 (7B09) [NCMD]: NLS1 (27C20) PH12D1 (7B39)
AVO(1D08) resets FS
AVO(1D08)

CMD
NCMD

PH11D1 (7B09): Cont. to process accessed word and set up 2nd status word.
PLED1(2C15) = PH11D1
T2D1 : CXM (17B28) (6D04) M16→M31 to Creg.
T4D1 : NLS1 (27C20) (6D17) PH12D1 (7B39)

PH12D1 (7B39) : Set up 2nd return status word.
PLED1(2C15) = (NFS + FSL)(NMS + MDR1) (11B22) (14B36) (2A20)
FSL (14B36)
DOR(32A38)
IOR(14B34)
DR (10A10)
NCC1=/NCOND1/(12C25)
NCC2=/NCOND2/(12C33)
/PR/(12C45)
T0D1 : S31 (6B23) (6D06) NF1N (11B25) WX1 (11A35) set W0→W3 for write NK15 (23B22)
T1D1 : MXFR (15A46) (6D05) FR lines to M0→M7 [FS]: DOR resets CC1 (23B26) IOR resets CC2 (24B26) SX20 (16B34) set S 26 (21B42) MXBC (15A02) BCreg. to M16→M31 F3 sets OUT (30C27) OUT remembers SIO
T2D1 : NFS (11B22) (6D04) [NCC1-NCC2]: BAXADD (16C36) Creg. to CA reg.
T3D1 : NFNT (11B26) (6D07) LS1 (27C22) [NTPE]: PR (12C45)
T4D1 : NF3 (26C26) (6D17) PH1D2 (4C22) PH13D1 (7B07)
FR0(14B22)
FR1(14B20)
FR2(14B18)
FR3(14B13)
FR4(14B08)
FR5(14B10)
FR6(14B04)
FR7(14B06)
FRlines
STATUS

Allow next operation to start.

PH13D1 (7B07) : [TPE] Set up and store 2nd status word
/MQX/(10A01)
PLED1(2C15) = PH13D1
T0D1 : CXBCL (19B14) (6D06) FS8→FS14 to C8→C14 A4→A7 to H4→H7 H0→H3 remains low
T2D1 : MXADD (27A25) (6D04) Creg. to M0→M15 [TPE.OUT] : MS (2A22) [NCC1.NCC2.OUT]: OFXH (18C14) IS0→IS3 is cleared Dev. Addr. to IS4→IS7
T4D1 : NLS2 (30C22) (6D17) CX0 (17B10) clear Creg. HX0 (19C39) clear Hreg. PH14D1 (7B42)

PH14D1 (7842): [NCC1.NCC2.OUT] for successfull SIO, clear status.
AR (10A08)
/PR/(12C45)
PLED1(2C15) = PH14D1
T1D1 : [NCC1.NCC2.OUT]: BCXADD (18C34) (6D05) clear FSreg. OFXH (18C14) clear OFreg.
T2D1 : FIN (11B23) (6D04)
AR = PR (12C45)

MEMORY

Location 20 before IOP storage

0 ← 7	8	9							16 → 31
Device Address	0	0	0	0	0	0	0	0	Command Doubleword Address
	1	1							

8 true = 2 words of status
9 true = 1 word of status

Location 20 after 1rst. Status word is stored.

0 ← 15	16 → 31
Previous Command Doubleword Address	Command Doubleword Address

Location 21 after 2nd. Status word is stored.

0 ← 7	8	9	10	11	12	13	14	15	16 → 31
IP Device Status 0	IL	TDE	DME	MAE	CME	CTE	HLT	0	Remaining Previous Byte Count.

CME = IOP memory error
CTE = IOP control error
DME = Memory data error
HLT = IOP halt
IL = Incorrect length
IP = Interrupt pending
MAE = Memory address error
TDE = Transmission data error

D Revision

Note: Every PH#D1/2 (phaseterm) is reset at T3 time of its delay line.
Every PH#PD1/2 (phase term) is set at T1 time of its delay line and reset at T0 time of its delay line.
Leaving PH2PD2 and PH7PD1 or PH14PD1 high until the next operation.

TIO, TDV, HIO. PHASE SEQUENCE. (8 bit MIOP)

CPU

CNST (12C20)
IOPA0 (12C08)
IOPA1 (12C13)
IOPA2 (12C18)
ENC0 (12C06)
ENC1 (12C04)
ENC2 (12C10)

PHID2 (4C22) : Determine and initiate next operation.
PLED2 (2C11) = ME (17A19) = IOP address recognition.
TOD2 : FNT (11B27) (8D26) CPU function
T2D2 : F4 (27C27) = /TIO/ (8D17) F5 (28C27) = /TDV/ F2 (25C27) = /HIO/
T4D2 : PH2D2 (5C25) (8D07)

OR /TIO/ (14C19)
OR /TDV/ (14C23)
OR /HIO/ (14C15)

PH2D2 (5C25): Access location 20.
PLED2 (2C11) = FIN (11B23) = End of previous operation.
TOD2 : SX20 (16B34) (8D26) set Sreg. to location 20
T1D2 : LS0 (26C20) (8D30) LS1 (27C22) LS2 (30C20) CC1 (23B26) CC2 (24B26) MS (2A22) = MQ
T3D2 : IXMB (5A20) (8D28) M0 → M7 to IM80 → IM87 IM80 → IM87 to Ireg. PH10D1 (7B01)

/MQX/ (10A01)

POK (10A27)
/MQX/ (10A01)

PH10D1 (7B01) : [M8] Set up and store 1rst. return status word.
[NM8] Set up 2nd return status word.
PLED1 (2C15) = MDR1 parity OK sets MDR1
TOD1 : CXI (5A23) (6D06) AXM (17B45) M0 → M7 to Areg. M8 sets CMD (24B20) M9 sets TPE (5C20) WX1 (11A35) set W0 → W3 for write
T2D1 : FS (14C35) (6D04) [CMD] : CXBA (17B15) CAreg. to Creg. [NCMD] : CXBCL (19B14) FS8 → FS14 to C8 → C14
T4D1 : MXADD (27A25) (6D17) Creg. − 1 to M0 → M15 [CMD] : MS (2A22) PH11D1 (7B09) [NCMD] : NLS1 (27C20) PH12D1 (7B39)
AV0 resets FS

/FS/ (14C35)
/DA0 (32A23)
/DA1 (32A19)
/DA2 (32A15)
/DA3 (32A12)
/DA4 (32A03)
/DA5 (32A09)
/DA6 (32A01)
/DA7 (32A02)
DA lines
D.C. ADDRESS
AV0 (1D08)

PH11D1 (7B09) : Set up 2nd status word.
PLED1 (2C15) = PH11D1
T2D1 : CXBCL (19B14) (6D04) FS8 → FS14 to C8 → C14
T4D1 : NLS1 (27C20) (6D17) PH12D1 (7B39)

DR (10A1C)
/MQX/ (10A01)
AR (10A08)
/PR/ (12C45)

PH12D1 (7B39) : [TPE] Set up and store 2nd status word
PLED1 (2C15) = (NFS + FSL) (NMS + MDR1) (11B22) (14B36) (2A20)
TOD1 : S31 (6B23) (6D06) NFIN (11B25) WX1 (11B35) set W0 → W3 for write
T1D1 : MXFR (15A46) (6D05) FR lines to M0 → M7 [FS] : DOR resets CC1 (23B26) IOR resets CC2 (24B26) SX20 (16B34) set S26 (21B42) MXBC (15A02) BCreg. to M16 → M31 MXADD (27A25) Creg. to M0 → M15 [TPE] : MS (2A22)
T2D1 : NFS (11B22) (6D04)
T3D1 : NFNT (11B26) (6D07) NLS1 (27C22) [NTPE] : PR (12C45)
T4D1 : PH1D2 (4C22) (6D17) PH13D1 (7B07)
AR = PR (12C45)

FSL (14B36)
DOR (32A38
IOR (14B34)
FR lines
FR0 (14B22)
FR1 (14B20)
FR2 (14B18)
FR3 (14B13)
FR4 (14B08)
FR5 (14B10)
FR6 (14B04)
FR7 (14B06)
STATUS

Allow next operation to start.

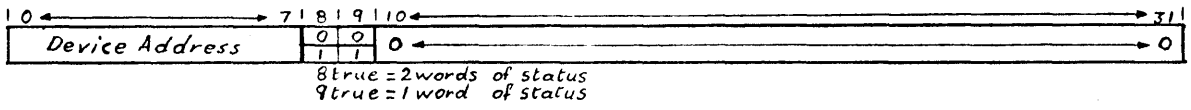
PH13D1 (7B07 : Used primarily for SIO and AIO.
PLED1 (2C15) = PH13D1
T4D1 : PH14D1 (7B42)

PH14D1 (7842): Termination.
PLED1 (2C15) = PH14D1
T2D1 : FIN (11B23)

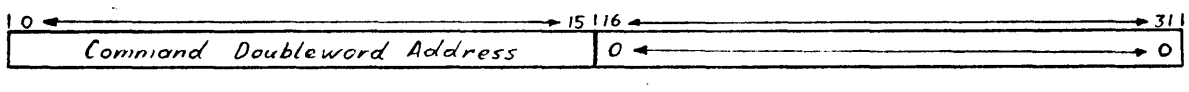
MEMORY

DEVICE CONTROLLER

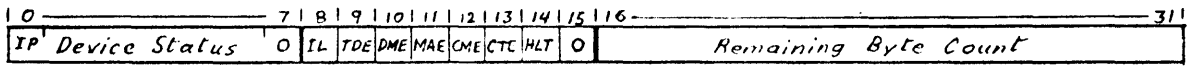
Location 20 before IOP storage.



Location 20 after 1rst. Status word is stored.



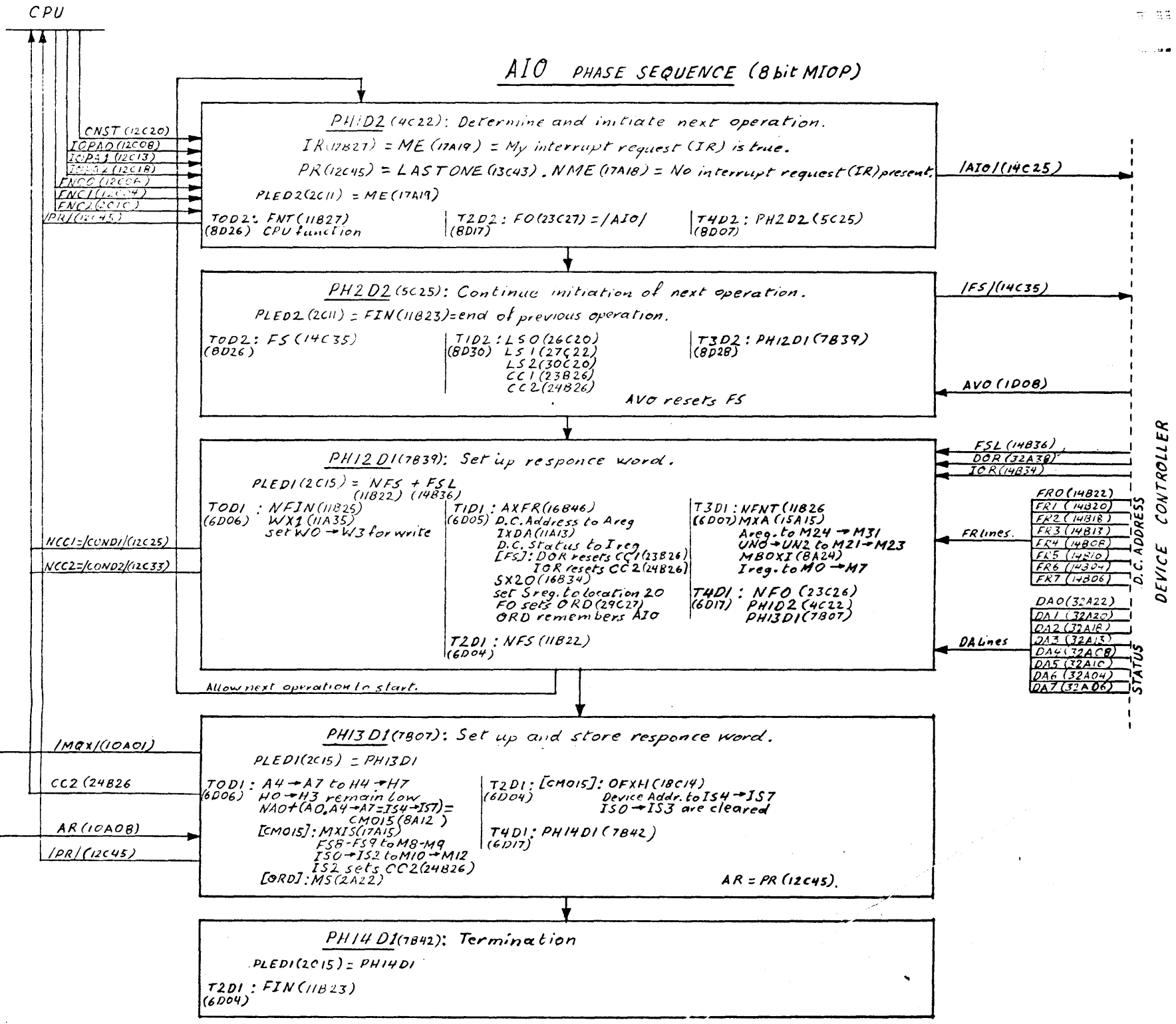
Location 21 after 2nd Status word is stored.



CME = IOP memory error
CTE = IOP control error
DME = Memory data error
HLT = IOP halt
IL = Incorrect length
IP = Interrupt pending
MAE = Memory address error
TDE = Transmission data error.

D Revision.

Note: Every PH#D1/2 (Phase term) is reset at T3 time of its delay line.
Every PH#PD1/2 (Phase term) is set at T1 time of its delay line, and is reset at T0 time of its delay line.
Leaving PH2PD2 and PH7PD1 or PH#PD1 high until the next operation.



Location 20 after response is stored

0 ← 7	8	9	10	11	12	13 ← 20	21 ← 23	24	25 ← 27	28 ← 31
D0 Device Status	IL	TDE	ZCI	CEI	UEI	0 ← 0	IOP#	M	D.C.	D.
							I.O. ADDRESS			

CEI = Channel end interrupt
D0 = Data overrun
IL = Incorrect length
TDE = Transmission data error.
UEI = Unusual end interrupt
ZCI = Zero byte count interrupt.

D. = M=0/Device Cont.#, M=1/Unit #
D.C. = Multiunit device cont. #
M. = 1/Multiunit device, 0/single unit device.

D Revision

Note: Every PH#D1/2 (phase term) is reset at T3 time of its delay line.
Every PH#PD1/2 (phase term) is set at T1 time of its delay line, and reset at T0 time of its delay line.
Leaving PH2PD2 and PH7PD1 or PH14PD1 true untill the next operation.

ORDER OUT PHASE SEQENCE (8bit MIOP)
(DOR.IOR)

PH1D2 (4C22) : Determine next operation and start service connection.

PLED2 (2C11) = SC (32A40)

T2D2 : F1 (24C27) = /ASC/ (8D17)

T4D2 : FS (14C35) (8D07) PH2D2 (5C25)

AV0 resets FS and F1

SC (32A40)
/ASC/ (14C33)
/FS/ (14C35)
AV0 (100B)

PH2D2 (5C25): Complete service connection.

PLED2 (2C11) := FIN (F1. FSL + NF1. NFSL) (11B23) (24C27) (14B36) (24C26)

T1D2 : AXFR (16B46) (8D30) Device address to Arg.
NCMD (24B22)
NTRA1 (28C25)

T2D2 : NFS (11B22) (8D17) K15 (23B20)

T4D2 : [F1]: PH1D1 (7B02) (8D07) [NF1]: PH1D2 (4C22)

FSL (14B36)
FR0 (14B22)
FR1 (14B20)
FR2 (14A18)
FR3 (14A13)
FR4 (14A0A)
FR5 (14A10)
FR6 (14B04)
FR7 (14B06)
FR lines

AV0 = NF1

PH1D1 (7B02): Determine type of service call and commence service cycle.

PLED1 (2C15) = RS (14B27)

T1D1 : DOR sets ORD (29C27) (6D05) IOR sets OUT (30C27)
ORDOUT (10B36)
NF1 (24C26)
EDI sets ED (32A33)

T2D1 : NFIN (11B25) (6D04) PH1D2 (4C22)
TORD (4C30)
NES (12B22)
LS0 (26C20)

T4D1 : PH4D1 (7B12) (6D17)

RS (14B27)
DOR (32A38)
IOR (14B34)
EDI (32A34)
/NES/
/ED/ (32A33)

Allow next operation to start.

PH4D1 (7B12): Access 1rst. word of command pair.

PLED1 (2C15) = NMS (2A20)

T0D1 : CXBA (17B15) (6D06) CA reg. to Creg.
SXBA (29C25)
CA reg. to Sreg.
WX0
clear W0 → W3 for read.
NSUB (23B25)

T1D1 : 1rst. time through PH4D1 (6D05) NFS15 sets MS (2A22)
FS15 = Chaining modifier
2nd. time through PH4D1
CMD sets MS (2A22)

T2D1 : BAXADD (16C36) (6D04) Creg+1 to CA reg.

T3D1 : IXMB (5C20) (6D07) M0 → M7 to IMB0 → IMB7
IMB0 → IMB7 to Ireg.
CMD (24B20)

T4D1 : NLS1 (27C20) (6D17) NLS2 (30C22)
[EH+MS]: NK15 (23B22)
PH5D1 (7B14)
[NEH.NMS]: PH4D1 (7B12)

/MQX/ (10A01)

Chaining modifier

PH5D1 (7B14) : Process 1rst word and access 2nd word of command pair.

PLED1 (2C15) = NMS + MDR1 (POK sets MDR1) (2A20)

T0D1 : [ORD]: 0XI (5A23) (6D06) Order to Oreg.
if order = 08_{16} = TRA (15A01)
S31 (6B23)
[TRA]: CXM (17B28)
M16 → M31 to Creg.
[NTRA]: NLS0 (26C22)
CXMR3 (18H33)
M13 → M28 to Creg.
HUXM (21C34)
M29 → M31 to 110 → H2
[TRA.TRA1]: EH (6A23)

T1D1 : [NEH.NTRA]: MS (2A22) (6D05)

T2D1 : [TRA]: BAXADD (16C36) (6D04) Command Addr. to CAreg.
[NTRA]: BAXADD (16C36) Byte addr. to BAreg.
[ORD (NTRA+EH)]: RSA (14C03)

T4D1 : TRA1 (28C23) (6D17) [NEH.TRA]: K15 (23B20)
PH4D1 (7B12)
[EH+NTRA]: PH6D1 (7B21)

POK (10A27)
/MQX/ (10A01)
/DA0/ (32A23)
/DA1/ (32A19)
/DA2/ (32A15)
/DA3/ (32A12)
/DA4/ (32A03)
/DA5/ (32A09)
/DA6/ (32A01)
/DA7/ (32A02)
DA lines if ORD.
/RSA/ (14C03) if ORD

Transfer in channel.

PH6D1 (7B21) : Process 2nd. word of command pair.

PLED1 (2C15) = NMS + MDR1 (2A20)

T0D1 : CXM (17B28) (6D06) M16 → M31 to C reg
M7 sets H3 (26C25)
Read reverse sets H4 (27C23)
M4 sets H5 (28C20)
M0 sets H6 (29C20)

T2D1 : BCXADD (18C34) (6D04) Bytecount to BC reg.
0FXH (18C14)
Hreg. to 0Freg.

T4D1 : LS1 (27C22) (6D17) LS2 (30C20)
PH7D1 (7B46)

POK (10A27)

PH7D1 (7B46): Termination

PLED1 (2C15) = RS (14B27)

T1D1 : CXBCL (19B14) (6D05) FS8 → FS14 to C8 → C14
ES (12B20)
[MAE]: C11 (27B21)
[MPE]: C12 (26B29)
[EH.NMAE.NMPE]: C13 (26B21)

T1D1 : [EH]: C14 (26B22) Cont. 03 (31A14)
04 (31A21)
CXBCU (19B35)
FS0 → FS7 to C0 → C7
[NEH]: CXMB0 (18B45)
M0 → M7 to C0 → C7

T3D1 : BCXADD (18C34) (6D07) Creg. to FS reg.
RSA (14C03)

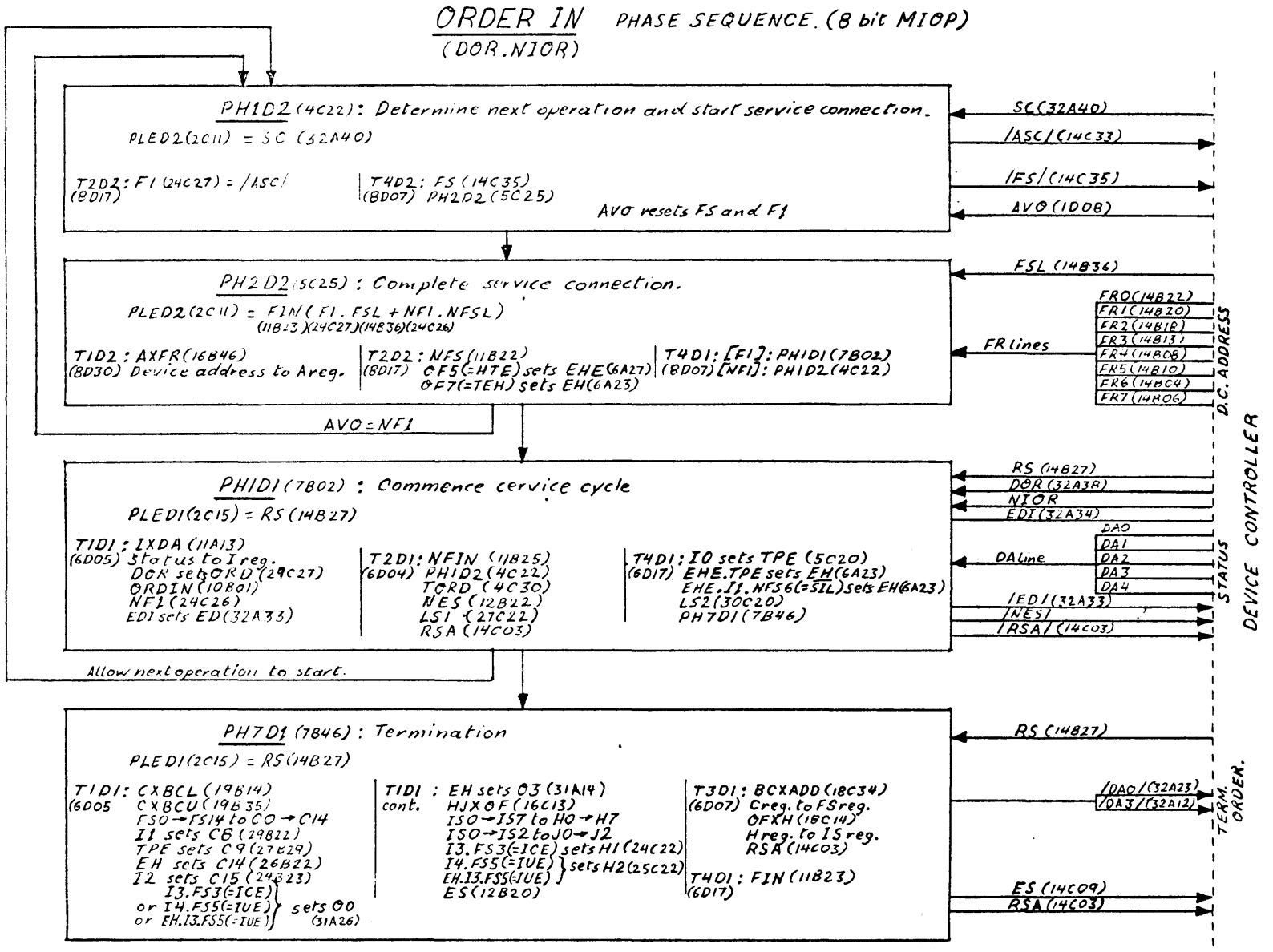
T4D1 : FIN (11B23) (6D17)

RS (14B27)
DA lines /DA3/ (32A12) /DA4/ (32A03)
/ES/ (14C09)
/RSA/ (14C03)

MEMORY
DEVICE CONTROLLER
ORDER
TERM. ORDER

D Revision

Note : Every PH#D1/2 (phase term) is reset at T3 time of its delay line.
Every PH#PD1/2 (phase term) is set at T1 time of its delay line, and reset at T0 time of its delay line.
Leaving PH2PD2 and PH7PD1 or PH14PD1 true untill the next operation.



Status in Ireg.

I0 = TE = Transmission error
I1 = IL = Incorrect length
I2 = CM = Chaining modifier
I3 = CE = Channel end
I4 = UE = Unusual end

Terminal order in Oreg.

00 = I = Interrupt
03 = HLT = IOP error halt.

NOTE: Every PH#D1/2 (phase term) is reset at T3 time of its delay line.
Every PH#PD1/2 (phase term) is set at T1 time of its delay line and reset at T0 time of its delay line.
Leaving PH2PD2 and PH7PD1 or PH3 PD1 true until the next operation.

DATA OUT (NDOR.IOR) PHASE SEQUENCE (8 bit MIOP)

PH1D2 (4C22): Determine next operation and start service connection.

PLED2 (2C11) = SC (32A40)

T2D2: F1 (24C27) = /ASC/ (8D17)

T4D2: FS (14C35) (8D07) PH2D2 (5C25)

AV0 resets FS and F1

SC (32A40)
/ASC/ (14C33)
/FS/ (14C35)
AV0 (1D0E)

PH2D2 (5C25): Complete service connection.

PLED2 (2C11) = FIN (F1 . FSL + NF1 . NFSL)
(11B13)(24C27)(14B36)(24C26)

T1D2: AXFR (16B46) (8D30) Device address to A reg.
NCMD (24B22)
NTRA1 (28C25)
NLS0 (26C22)
NLS1 (27C20)
NLS2 (30C22)
FP (12B23)

T2D2: NFS (11B22) (8D17) K15 (23B20)
SUB (23B23)

T3D2: HJXOF (16C13) (8D28) OF reg. to H reg
0F0 → 0F2 to J0 → J2
0F7 sets EH (6A23)

T4D2: [F1]: PH1D1 (7B02) (8D07) [NF1]: PH1D2 (4C22)

FSL (14B36)
FRlines
FR0 (14B22)
FR1 (14B20)
FR2 (14B18)
FR3 (14B13)
FR4 (14B08)
FR5 (14B10)
FR6 (14B04)
FR7 (14B06)
D.C. ADDRESS

AV0 = NF1

F1

PH1D1 (7B02): Determine type of service call and commence service cycle.

PLED1 (2C15) = RS (14B27)

T0D1: SXBA (29C25) (6D06) BA reg. to S15 → S30
WX0
clear W0 → W3 for read.

T1D1: IOR sets CUT (30C27) (6D05) EDI sets ED (6A20)
NF1 (24C26)
J0 sets S31 (6B23)

T2D1: NFIN (11B25) (6D04) PH1D2 (4C22)
MS (2A22)

T3D1: IXMB (5A20) (6D07) IMB0 → IMB7 to I reg.

T4D1: PH2D1 (7B26) (6D17)

NH1.NH2 = IXMB0 (13A45)
NH1.H2 = IXMB1 (13A46)
H1.NH2 = IXMB2 (13A02)
H1.H2 = IXMB3 (13A13)
selected M reg. byte to IMB0 → IMB7

RS (14B27)
NDOR
IOR (14B34)
EDI (32A34)
/MQX/ (10A01)
MEMORY

Allow next operation to start.

PH2D1 (7B26): Data output phase.

PLED1 (2C15) = +FP (12B23) . MDR1 ← 1rst time through PH2D1,
+NFP (12B25) . RS (14B27) ← next times through PH2D1.

T0D1: CXI (5A23) (6D06) Word boundry (J1, J2) = CM030
CM030 sets ED (6A20)
(8A01) sets ES (12B20)
sets TRA1 (28C23)
CXBCL (19B14)
CXBCU (19B35)
BC reg. to C reg.

T1D1: EDI sets ED (6A20) (6D05) HXJP1 (21C12)
3 LSB of byte addr. +1 to H0-H3
H0.TRA1 = CBA (18C13)
CBA = Update byte address

T2D1: BCXADD (18C34) (6D04) Creg. -1 to BC reg.
If byte count = 0 set ZBC
OFXH (18C14) (4C23)
[EH+ZBC]: ED (6A20)
NES (12B22)
TORD (4C30)
[ED.NEH.NZBC]: ES (12B20)
[TRA1+NED+FP]: RSA (14C03)

T3D1: NFP (12B25) (6D07) IXMB (5A20)
IMB0 → IMB7 to I reg.
ZBC sets LS0 (26C20)

T4D1: JXH (21C46) (6D17) H0 → H3 to J0 → J3
RSA (14C03)
ED sets LS1 (27C22)
TORD sets LS2 (30C20)
NED sets PH2D1 (7B26)
CBA.NZBC sets PH3D1 (7B27)
ZBC.H6 sets PH4D1 (7B12)
(ZBC+ED) NCBA.NH6 sets PH7D1 (7B46)

RS (14B27)
EDI (32A34)
/DA0/ (32A23)
/DA1/ (32A19)
/DA2/ (32A15)
/DA3/ (32A12)
DAlines
/DA4/ (32A07)
/DA5/ (32A09)
/DA6/ (32A01)
/DA7/ (32A03)
/DAP/ (32A25)
DATA
/ED/ (32A33)
/ES/ (14C09)
/RSA/ (14C03)
DEVICE CONTROLLER

PDK (10A27)

ZBC + ED

NED

H6. ZBC = DATA CHAINING

CBA

PH3D1 (7B27): Update byte address.

PLED1 (2C15) = PH3D1

T0D1: NSUB (23B25) (6D06) CXBA (17B15)
BA reg. to C reg.

T1D1: No error sets FP (12B23) (6D05)

T2D1: BAXADD (16C36) (6D04) Creg. +1 to BA reg.
FP sets FIN (11B23)

T4D1: NFP sets PH7D1 (7B46) (6D17)

ERROR

PH4D1 (7B14)
PH5D1 (7B12)
PH6D1 (7B21)
} Same as in Order Out except ORD is low.

PH7D1 (7B46): Termination.

PLED1 (2C15) = RS + MRD1 (14B27)

T0D1: NK15 (23B22) (6D06) CMD = Data chained

T1D1: CXBCL (19B14) (6D05) FS8 → FS14 to C8 → C14
[NCMD+EH]: CXACU (19B35)
FS0 → FS7 to C0 → C7
[CMD.NEH]: CXMB0 (18B45)
M0 → M7 to C0 → C7
[MPE]: C10 (27B21)
[MAE]: C11 (27B22)
[CMD.MPE]: C12 (26B29)
[CMD.EH.NMAE.NMPE]: C13 (26B21)
[EH]: C14 (26B22)

T1D1 cont.: TORD [ZBC.BC1(=IZC)]: 00 (31A26)
[ZBC.NBC0(=DC)]: 01 (31A27)
[BC2(=CC)]: 02 (31A12)
[EH]: 03 (31A14)
[NCMD.EH.OUT]: 04 (31A21)
HJXOF (16C13)
IS0 → IS7 to H reg.
[ZBC.BC1(=IZC)]: H0 (23C22)
NTORD: HJXOF (16C13)
0F0 → 0F6 to H0 → H6
[EH]: H7 (30C25)
[NMPE.NMAE.NTPE]: FIN (11B23)
ES (12B20)

T3D1: BCXADD (18C34) (6D07) Creg to FS reg.
RSA (14C03)

T4D1: FIN (11B23) (6D17)

RS (14B27)
DAlines
/DA0/ (32A23)
/DA1/ (32A19)
/DA2/ (32A15)
/DA3/ (32A12)
/DA4/ (32A03)
TERM. ORDER
/ES/ (14C09)
/RSA/ (14C03)

D Revision

NOTE : Every PH#DI/2 (phase term) is reset at T3 time of its delay line.
Every PH#PDI/2 (phase term) is set at T1 time of its delay line and reset at T0 time of its delay line.
Leaving PH2PD2 and PH7PD1 or PH3PD1 true until the next operation.

DATA IN PHASE SEQUENCE (8 bit MIOP)

(NDOR.NIOR)

PHID2 (4C22) : Determine next operation and start service connection.

PLED1(2C11) = SC (32A40)

T2D2 : FI (24C27) = /ASC/ (8D17)

T4D2 : FS (14C35) (8D07) PH2D2 (5C25)

AVO resets FS and FI

SC (32A40)
/ASC/ (14C33)
/FS/ (14C35)
AVO (1DCE)

PH2D2 (5C25) : Complete service connection.

PLED2 (2C11) = FIN (FI . FSL + NFI . NFSL)
(11B23)(24C27)(14B36)(24C26)

TID2 : AXFR (16B46) (8D30) Device address to Areg.
NCMD (24B22)
NTRAI (28C25)
NLS0 (26C22)
NLS1 (27C20)
NLS2 (30C22)
FP (12B23)

T2D2 : NFS (11B22) (8D17) K15 (23B20)
SUB (23B23)

T3D2 : HJX0F (16C13) (8D28) OFreg. to Hreg.
0F0 → 0F2 to J0 → J2
0F7 sets EH (6A23)

T4D2 : [FI] : PHIDI (7B02)
(8D07) [NFI] : PH1D2 (4C22)

FSL (14B36)
FR lines
FR0 (14B21)
FR1 (14B06)
FR2 (14B18)
FR3 (14B12)
FR4 (14B08)
FR5 (14B10)
FR6 (14B04)
FR7 (14B06)
D.C. ADDRESS.

AVO = NFI

FI

PHIDI (7B02) : Determine type of service call and commence service cycle.

PLED1(2C15) = RS (14B27)

TOD1 : SXBA (29C25) (6D06) BA reg. to S15 → S30
CXBCL (19B14)
CXBCU (19B35)
BCreg. to Creg.
Word boundry sets ES (12B20)
sets ED (6A20)
sets TRAI (28C23)
WX0
clear W0 → W3

TID1 : IXDA (11A13) (6D05) EDI sets ED (6A20)
J0 sets S31 (6B23)
NFI (24C26)
[NH4 (forward)] : HXJP1 (21C12)
3LSB of byte address + 1
[H4 (reverse)] : HXJM1 (21C33)
3LSB of byte address − 1

T2D1 : NFIN (11B25) (6D04) PHID2 (4C22)
BCXADD (18C34)
Creg − 1 to BCreg.
If BCreg = 0 = ZBS (28B34)
[ZBS+EH] : ED (6A20)
NES (12B22)
TORD (4C30)
[NZBS.NEH.ED] : ES (12B20)
[NED+TRAI] : RSA (14C03)
[(ED+EH+ZBS).NH3] : MS (2A22)
H3 = SKip command.
OFXH (18C14)
NJ1.NJ2 = MB0XI (8A24)
NJ1 . J2 = MB1XI (15A12)
J1 . NJ2 = MB2XI (15A34)
J1 . J2 = MB3XI (15A14)
Ireg. to selcted M byte.
MB0XI sets W0, MB1XI sets W1, etc.

T3D1 : NFP (12B25) (6D07) ZBC sets LS0 (26C20)

T4D1 : JXH (21C46) (6D17) H0 → H3 to J0 → J3
RSA (14C03)
IEVEN sets TPE (5C20)
EHE.TPE sets EH (6A23)
ED sets LS1 (27C22)
TORD sets LS2 (30C20)
NED sets PH2D1 (7B26)
NZBC.CBA sets PH3D1 (7B27)
[+NH4.NH0.TRAI + H4.H0.TRAI] : CBA (18C13)
ZBC.H6 sets PH4D1 (7B12)
H6 = data chaining.
ZBC.NH6+ED.NCBA set PH7D1 (7B46)

RS (14B27)
NDOR
NIOR
EDI (32A34)
DAO (32A22)
DA1 (32A20)
DA2 (32A18)
DA3 (32A13)
DA4 (32A08)
DA5 (32A10)
DA6 (32A04)
DA7 (32A06)
DAP (32A27)
DA lines
DATA
/ED/ (32A33)
/ES/ (14C09)
/RSA/ (14C03)

/MQX/ (10AC1)
DR (10A1C)
MEMORY

Allow next operation to start.
H6.ZBC = DATA CHAINING.
ZBC.NH6+ED
CBA = UPDATE BYTE ADDRESS.
NED

PH2DI (7B26) : Data input phase.

PLED1(2C15) = RS (14B27)

TOD1 : CXBCL (19B14) (6D06 CXBCU (19B35)
BCreg. to Creg.
word boundry sets ED (6A20)
sets ES (12B20)
sets TRAI (28C23)

TID1 : IXDA (11A13) (6D05) EDI sets ED (6A20)
[NH4 (Forward)] : HXJP1 (21C12)
3LSB of byte address + 1
[H4 (reverse)] : HXJM1 (21C33)
3LSB of byte address − 1

T2D1 : BCXADD (18C34) (6D04) Creg − 1 to BCreg.
If BCreg = 0 = ZBS (28B34)
[ZBS+EH] : ED (6A20
NES (12B22)
TORD (4C30)
[NZBS.NEH.ED] : ES (12B20)
[NED+TRAI] : RSA (14C03)
[(ED+EH+ZBS).NH3] : MS (2A22)
H3 = Skip command
OFXH (18C14)
NJ1.NJ2 = MB0XI (8A24)
NJ1 . J2 = MB1XI (15A12)
J1 . NJ2 = MB2XI (15A34)
J1 . J2 = MB3XI (15A14)
MB0XI sets W0
MB3XI sets W3

T3D1 : ZBC sets LS0 (26C20) (6D07)
T4D1 : JXH (21C46) (6D17) H0 → H2 to J0 → J2
RSA (14C03)
IEVEN sets TPE (5C20)
EHE.TPE sets EH (6A23)
ED sets LS1 (27C22)
TORD sets LS2 (30C20)
NED sets PH2D1 (7B26)
NZBC.CBA sets PH3D1 (7B27)
[+NH4.NH0.TRAI + H4.H0.TRAI] : CBA (18C13)
ZBC.H6 sets PH4D1 (7B12)
H6 = Data chaining
ZBC.NH6+ED.NCBA sets PH7D1 (7B46)

RS (14B27)
EDI (32A34)
DAO (32A22)
DA1 (32A20)
DA2 (32A18)
DA3 (32A13)
DA4 (32A08)
DA5 (32A10)
DA6 (32AC4)
DA7 (32A06)
DAP (32A27)
DA lines
DATA
/ED/ (32A33)
/ES/ (14C09)
/RSA/ (14C03)

/MQX/ (10AD1)
DR (10A10)

NED
H6.ZBC = DATA CHAINING.
ZBC.NH6+ED
CBA = UPDATE BYTE ADDRESS

PH3DI (7B27) : Update byte address.

PLED1(2C15) = PH3DI

TOD1 : NSUB (23B25) (6D06) CXBA (17B15)
BAreg. to Creg.

TID1 : No errors set FP (12B23) (6D05)

T2D1 : BAXADD (16C36) (6D04 Creg. + 1 to BAreg.
FP sets FIN (11B23)

T4D1 : NFP sets PH7D1 (7D46) (6D17)

ERROR

PH4DI (7B12)
PH5DI (7B14)
PH6DI (7B21)
} Same as for Order Out except DOR is low.

PH7DI (7B46) : Termination

PLED1 (2C15) = RS + MDR1 (14B27)

TOD1 : NK15 (23B22) (6D06)
CMD = Data chained

TID1 : CXBCL (19B14) (6D05) FSB → FS14 to CB → C14
[NCMD+EH] : CXBCU (19B35)
FSO → FS7 to C0 → C7
[CMD.NEH] : CXMB0 (16B45)
M0 → M7 to C0 → C7
[MPE] : C10 (27B21)
[MAE] : C11 (27B22)
[CMD.MPE] : C12 (26B29)
[CMD.EH.NMAE.NMPE] : C13 (26B21)
[EH] : C14 (26B22)

TID1 cont. : TORD [ZBC.BC1(=IZC)] : 00 (31A26)
[ZBC.NBC0(=IC)] : 01 (31A27)
[BC2(=CC)] : 02 (31A12)
[EH] : 03 (31A14)
[NCMD.EH.OUT] : 04 (31A21).
HJXOF (16C13)
IS0 → IS7 to Hreg.
[ZBC.BC1(=IZC)] : A0 (23C22)
NTORD : HJXOF (16C13)
0F0 → 0F6 to H0 → H6
[EH] : H7 (30C25)
[NMPE.NMAE.NTPE] : FIN (11B23)
ES (12B20)

T3D1 : BCXADD (18C34) (6D07) Creg. to FS reg.
RSA (14C03)

T4D1 : FIN (11B23) (6D17)

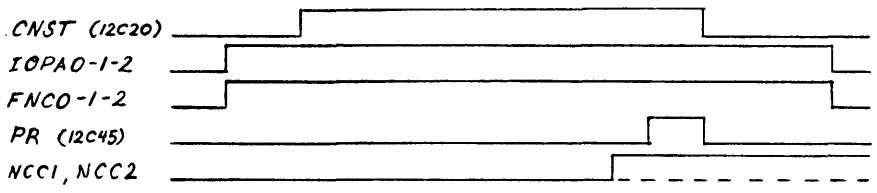
RS (14B27)
DA lines
/DA0/ (32A23)
/DA1/ (32A19)
/DA2/ (32A15)
/DA3/ (32A12)
/DA4/ (32AC3)
TEAM. ORDER
/ES/ (14C09)
/RSA/ (14C03)

DEVICE CONTROLLER

D Revision

MIOP Interface (8 bit MIOP)

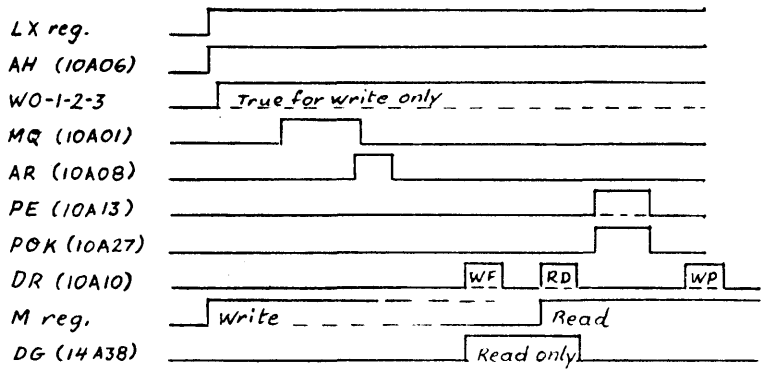
CPU / MIOP



IOPA0 (12C08) FNC0 (12C06)
IOPA1 (12C13) FNC1 (12C04)
IOPA2 (12C18) FNC2 (12C10)

NCC1 (23B26)
NCC2 (24B26)

MEMORY / MIOP



W0	W1	W2	W3
14A23	14A25	14A33	14A35

LX register.

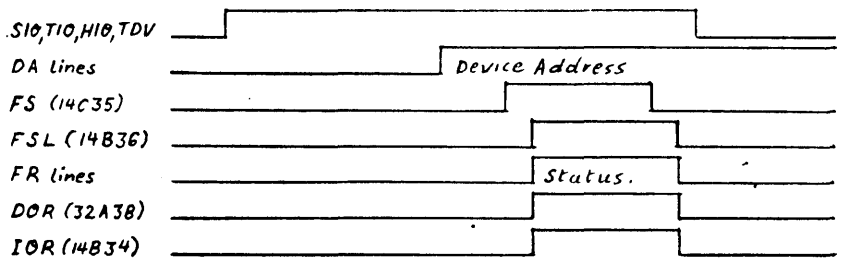
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
12A01	12A02	12A03	12A09	12A12	12A15	12A19	12A23	12A25	12A33	12A35	12A37	12A39	12A45	14A12	14A15	14A19

MX register.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
21A37	21A33	21A34	21A35	21A18	21A13	21A14	21A15	22A37	22A33	22A34	22A35	22A18	22A13	22A14	22A15	23A37	23A33	23A34	23A35	23A18	23A13	23A14	23A15	24A37	24A33	24A34	24A35	24A18	24A13	24A14	24A15

DEVICE CONTROLLER / MIOP

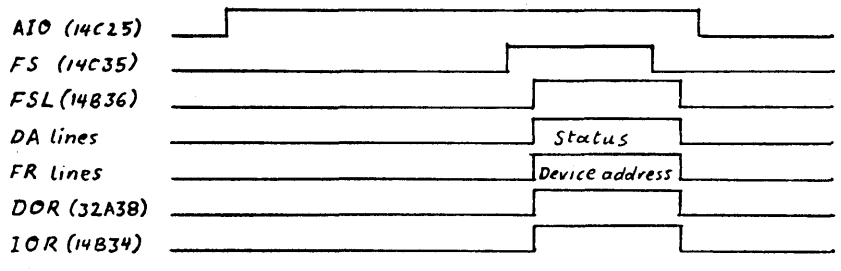
SIO, TIO, HIO, TDV



SIO (14C12)
TIO (14C19)
HIO (14C15)
TDV (14C23)
AIO (14C25)

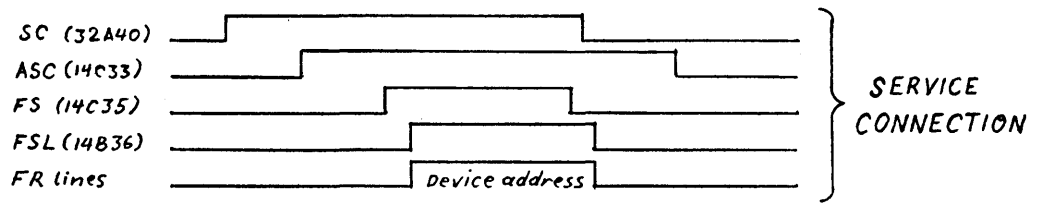
FR0 (14B22)
FR1 (14B20)
FR2 (14B18)
FR3 (14B13)
FR4 (14B08)
FR5 (14B10)
FR6 (14B04)
FR7 (14B06)

AIO



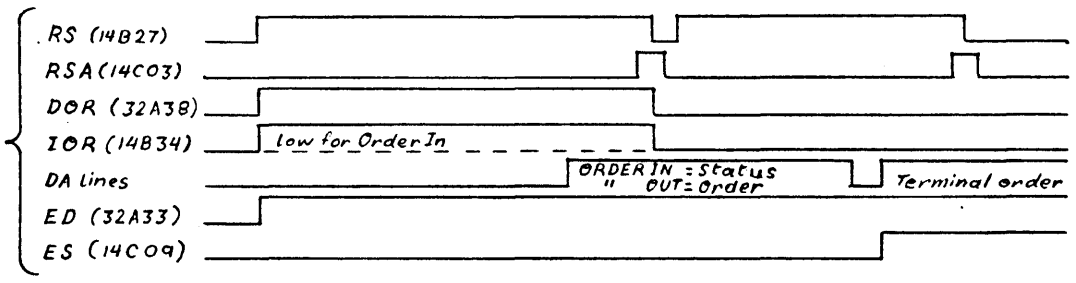
/DA0/ (32A23) DA0 (32A22)
/DA1/ (32A19) DA1 (32A20)
/DA2/ (32A15) DA2 (32A18)
/DA3/ (32A12) DA3 (32A13)
/DA4/ (32A03) DA4 (32A08)
/DA5/ (32A09) DA5 (32A10)
/DA6/ (32A01) DA6 (32A04)
/DA7/ (32A02) DA7 (32A06)
/DAP/ (32A25) DAP (32A27)

SERVICE CYCLE



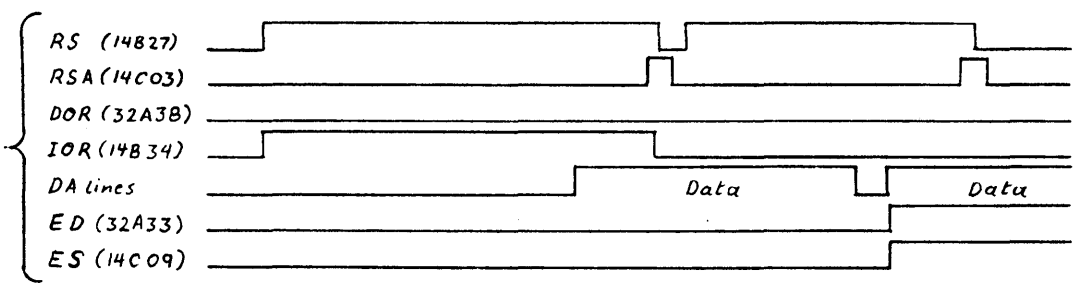
ORDER OUT + ORDER IN

Note: Order Out/In always has a terminal order.



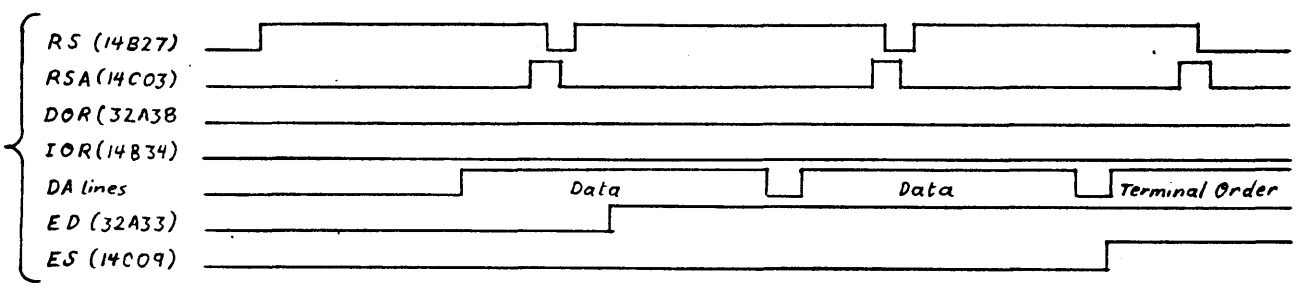
DATA OUT

Output 2 bytes



DATA IN

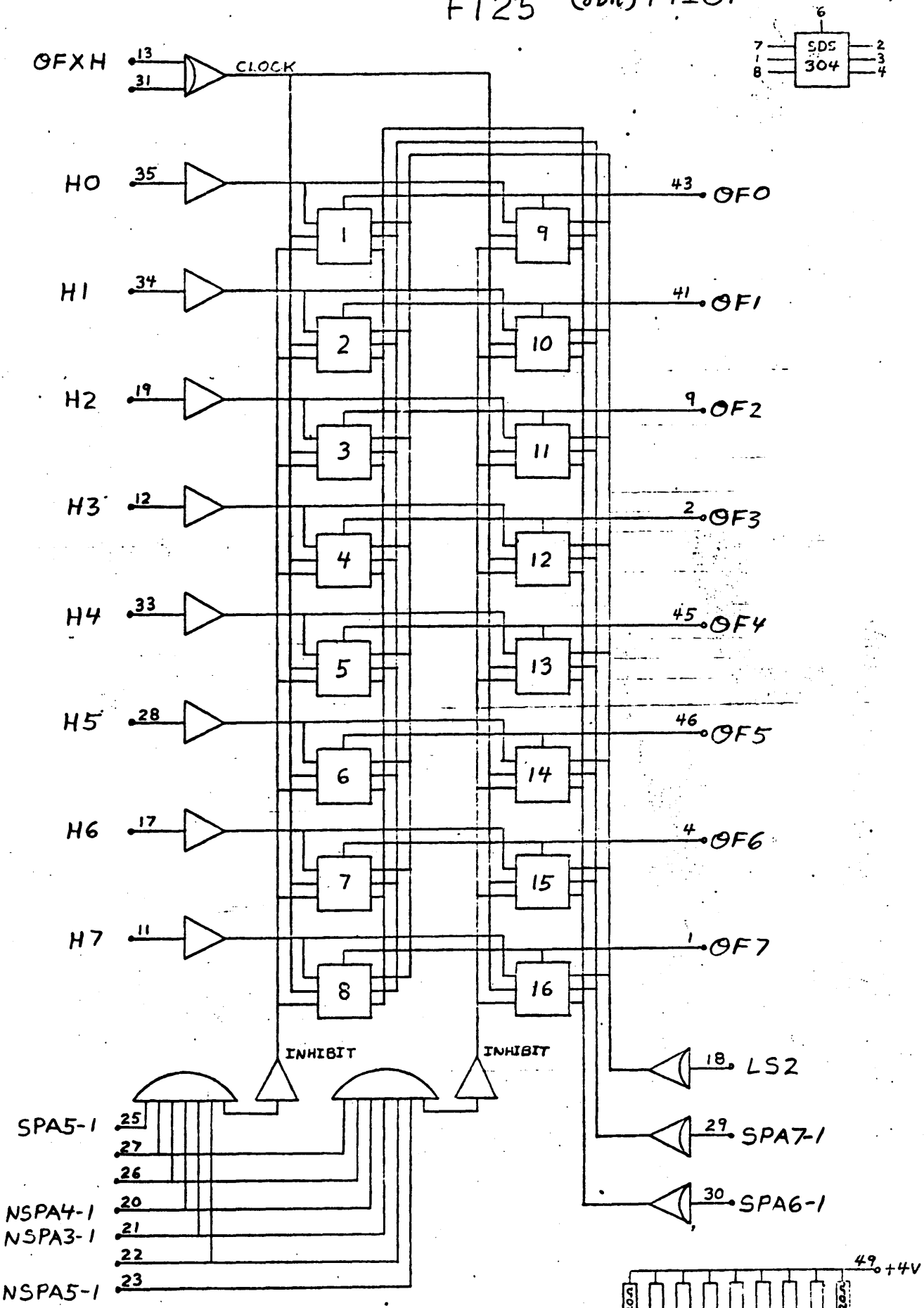
2nd data byte reaches zero byte count (ZBC)



Note: Terminal Orders (ED.NES) are requested on errors, zero byte count, order in and order out.

D Revision.

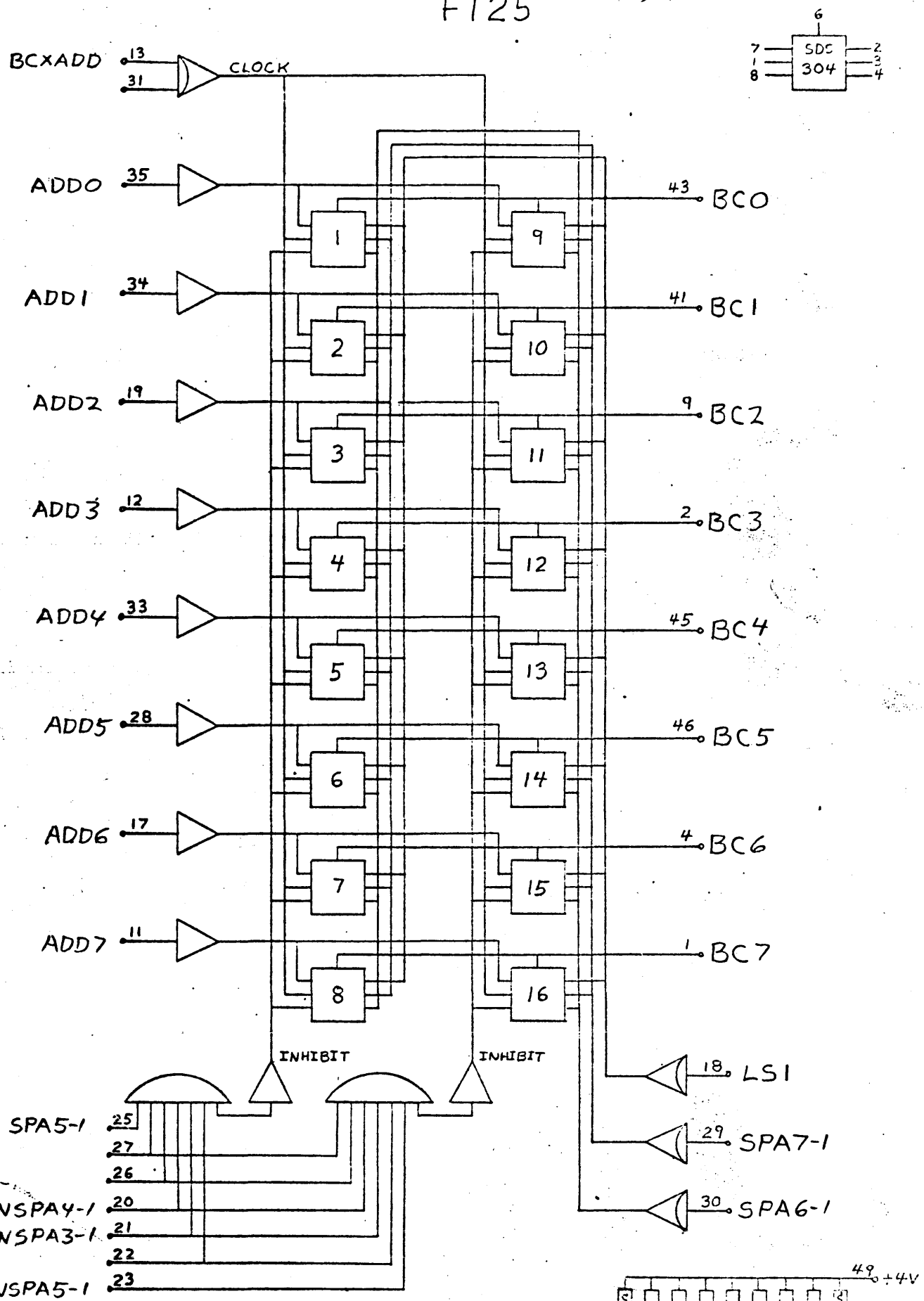
FT25 (8bit) MIOP



MIOP
Σ 5/7
11D

LS2 = INTERRUPT STATUS
NLS2 = LSB of Byte Address
f some flags

FT25 (8bit) MIOP 15D

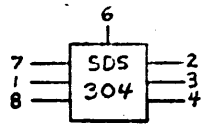


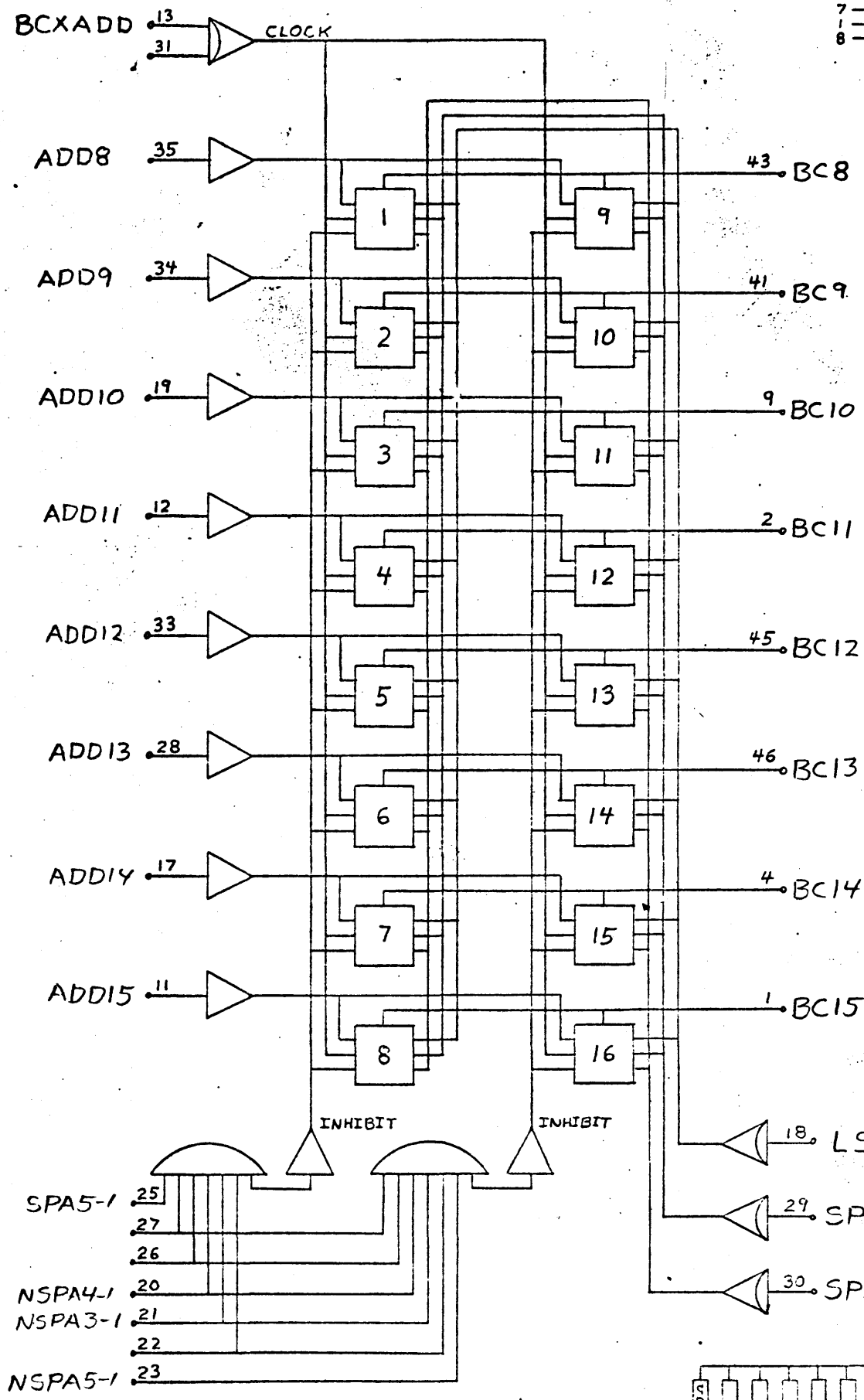
MIOP
Σ5/7
15D

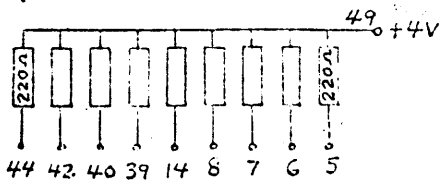
LS1 = FLAGS & STATUS

NLS1 = BYTE COUNT

FT25 (8bit) MIOP 19D





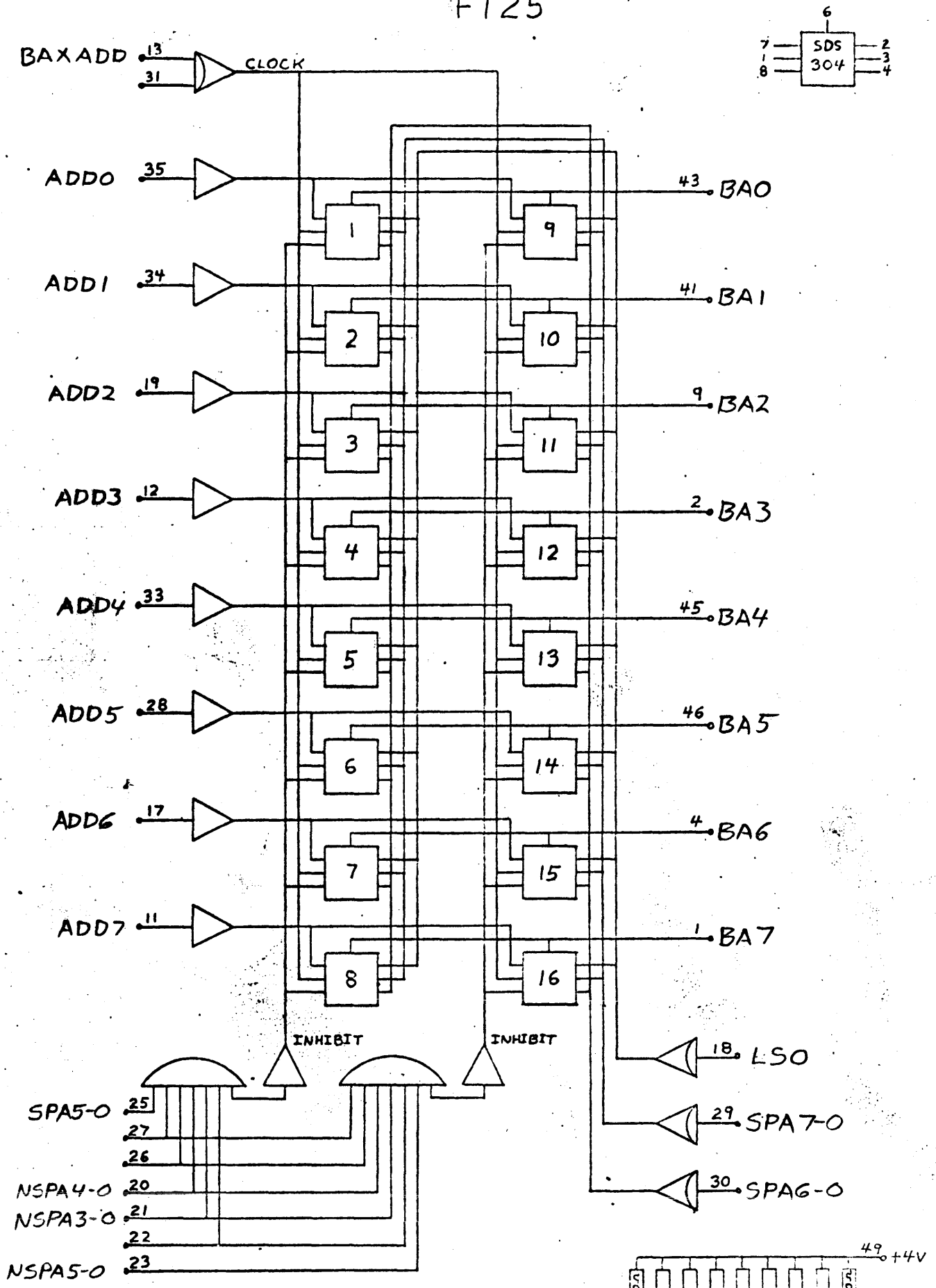


MIOP
2 5/7
19D

LSI = FLAGS & STATUS

NLSI = BYTE COUNT

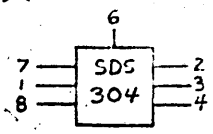
FT25 (8bit) MIOP 23D

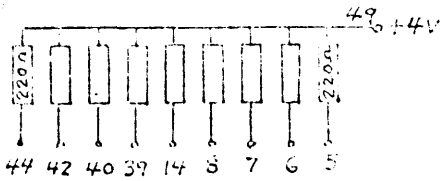


MIOP
Σ5/7
23D

LSO = COMMAND ADDRESS
NLSO = BYTE ADDRESS

FT25 (8bit) MIOP 27D



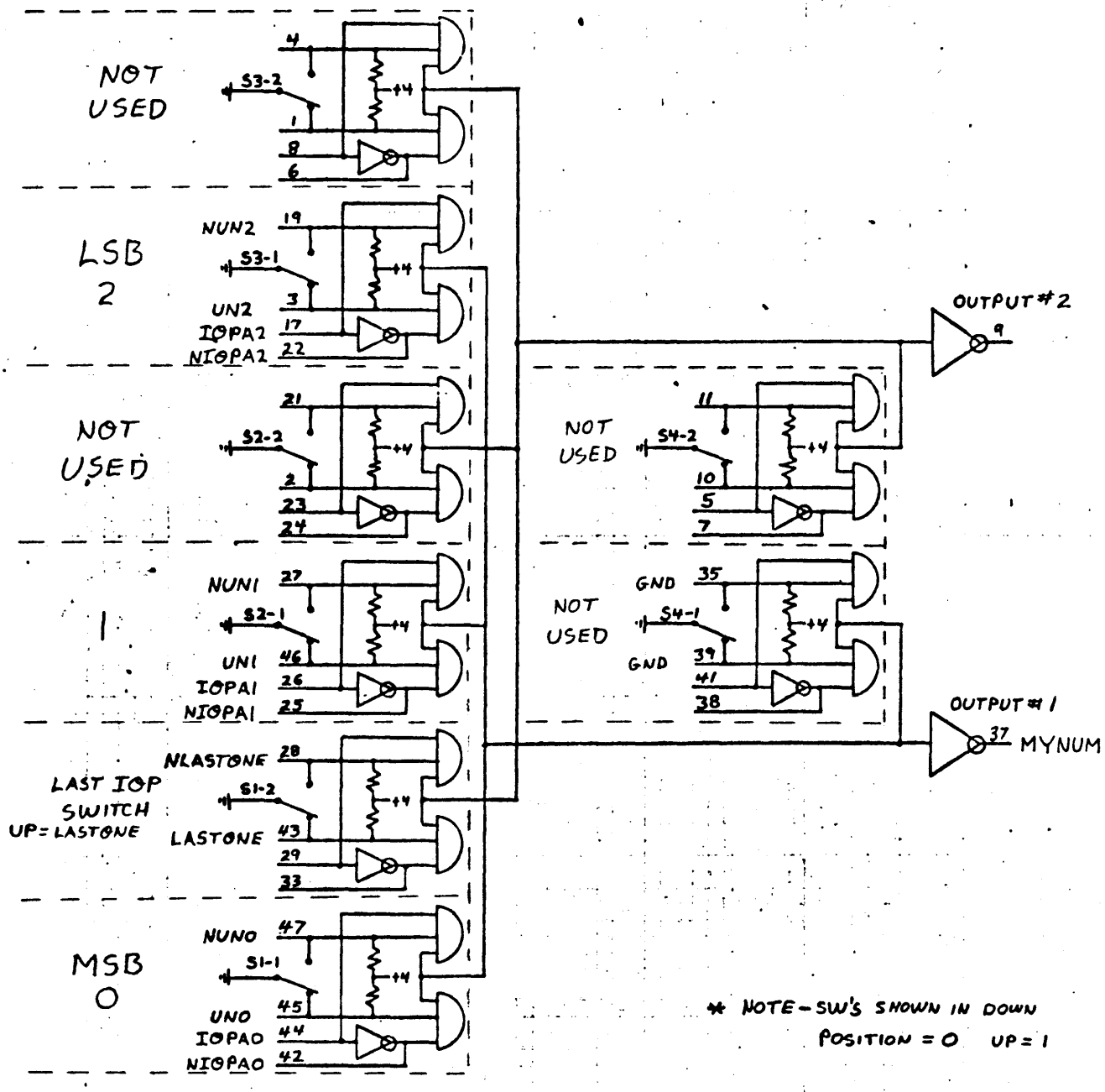


MIOP
≤ 5/7
27D

LSO = COMMAND ADDRESS
NLSO = BYTE COUNT

LT26 SWITCH MODULE (8bit) MIOP (13C)

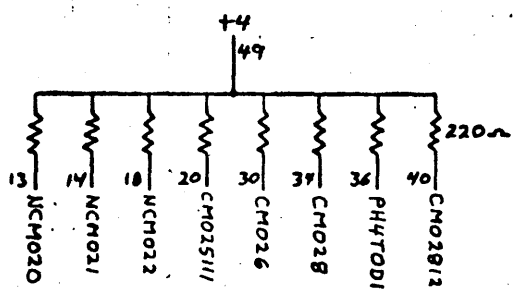
COCHRANE



* NOTE - SW'S SHOWN IN DOWN POSITION = 0 UP = 1

MSB		LSB
0	1	2

0 0 1 = 2nd. IOP



MIOP LT26 (13C)
SWITCH SETTING

BASIC (32 BIT) MIOP SEQUENCE OF EVENTS

SIO (START INPUT/OUTPUT)

1. CPU stores
   - Device Controller Address (M00 → M07)
   - Command Doubleword Address (M16 → M31)
   - Number of status words to be returned (M08, M09)

   in loc. 20.

2. CPU sends
   - IOP number (IOPA0:R → IOPA2:R)
   - Command to be executed (FNC0:R → FNC2:R)
   - and the Control Strobe (CNST:R)

   to the MIOP.

3. CPU waits for proceed (PR:R) from MIOP.

4. MIOP accesses loc. 20 (see 1.).

5. MIOP sends
   - Device Controller Address (M00 → M07)
   - Command (FNDSIO:D)
   - Function Strobe (FS:D)

   to Device Controller.

6. Device Controller responds with FSL:R and holds Device Controller status on FR Lines (FR0:R → FR7:R).

7. MIOP's 1st status word
   - send the old Command Doubleword Address from CA register to location 20.

8. MIOP stores new Command Doubleword Address in CA register.

9. MIOP's 2nd status word
   - Status off FR Lines (FR0:R → FR7:R)
   - Operational status from FS reg. (FS08 → 14)
   - Remaining byte count from BC reg.

   is stored in location 21.

10. MIOP clears FS and OF reg. with successful SIO possible. NCC1.NCC2

11. MIOP sends proceed to CPU.

12. CPU takes status from locations 20 and/or 21 and stores it in its designated registers.

    NOTE: If no status is asked for, none is sent.

Service call for Order Out from Device Controller that received the SIO.

ORDER OUT

1. MIOP
   - Connects for service with Device Controller
   - Receives Request Strobe (RS:D)
   - and determines Order Out Service Call (DOR:R,IOR:R)

ORDER OUT (CONT'D.)

2. MIOP accesses 1st word of Command Doubleword with Command Doubleword Address in CA reg. (Order and Start Byte Address) or (Transfer In Channel and Command Doubleword Address).

3. MIOP
   - if not Transfer In Channel:
     - sends order to Device Controller
     - stores Byte Address (M13 - 28) in BA reg.
     - and (M29 - 31) the 3 LSB. in OF reg. (OFF0 → OF02).
   - if Transfer In Channel:
     - stores new Command Doubleword Address (M16 - 31) in CA reg.
     - and goes back to step 2.

4. MIOP
   - accesses 2nd word of Command Doubleword (Flags and Byte Count)
   - stores Byte Count in BC reg.
   - stores Flags in FS reg. (FS00 → FS07)
   - sets up OF reg. (OF03 - OF06) with Flags and a read reverse order.

5. MIOP
   - sends Terminal Order to Device Controller
   - updates operational status and
   - disconnects service from Device Controller with End Service (ES:D).

Service Call for Data Out from Device Controller assuming the order sent during Order Out was an output order.

DATA OUT

1. MIOP
   - connects for service with Device Controller
   - receives Request Strobe (RS:D) and
   - determines Data Out Service Call from (NDOR:R.IOR:R)

2. MIOP with Byte Address received during Order Out access output data from Memory.

3. MIOP
   - 1 Byte interface:
     - sends 1 Byte at a time to Device Controller for every Request Strobe (RS:R).
   - 4 Byte interface:
     - sends 1 word at a time to Device Controller.

4. MIOP terminates data transfer (ED:D) if:
   - all data of accessed word has been transferred or
   - Device Controller sends End Data (ED:R) to MIOP or
   - Byte Count reaches zero (ZBC)

DATA OUT (CONT'D.)

5. For each Byte transferred:
   - 1 Byte interface: the Byte Count (BC reg.) is decremented by 1; the Byte Address is incremented by 1.
   - 4 Byte interface: the Byte Count (BC reg.) is decremented by 4; the Byte Address is incremented by 4.
6. MIOP sends Terminal Order to Device Controller and updates status if:
   - an error (EH) was encountered
   - Zero Byte Count (ZBC) not Data Chaining was reached.
7. MIOP disconnects service from Device Controller (ES:D).

NOTE: With Zero Byte Count (ZBC) and Data Chaining (OF06), the MIOP goes back to the Order Out but does not send the order of the next Command Doubleword to the Device Controller.

DATA OUT

Order Out (2)

Not Zero Byte Count and no error
Wait for next Data Out Service Call

Zero Byte Count and Data Chaining
go to step 2 of Order Out

Service Call for Order In from Device Controller. After a Terminal Order for Count Done or an error was encountered.

ORDER IN

1. MIOP connects for service with Device Controller; receives Request Strobe (RS:R) and determines Order In Service Call (DOR:R.NIOR:R).
2. MIOP accepts order from Device Controller.
3. MIOP updates its status (FS and IS reg.).
4. MIOP sends Terminal Order (TORD) to Device Controller.
5. MIOP disconnects service from Device Controller (ES:D).

Order Out

NOTE: If Command Chaining (02:D) was sent to the Device Controller during the Terminal Order, the Device Controller should come back with a Service Call for Order Out. If not, another SIO must be issued by the CPU for any further operation.

Command Chaining

DATA IN

1. Data In is equal to Data Out except that data is received by MIOP.

TIO (TEST INPUT/OUTPUT)

1. TIO is the same as SIO except for steps 7 and 11 and no Order Out Service Call is sent in response.

TDV (TEST DEVICE)

1. TDV is the same as TIO except that the status off FR Lines is unique to Device.

HIO (HALT DEVICE)

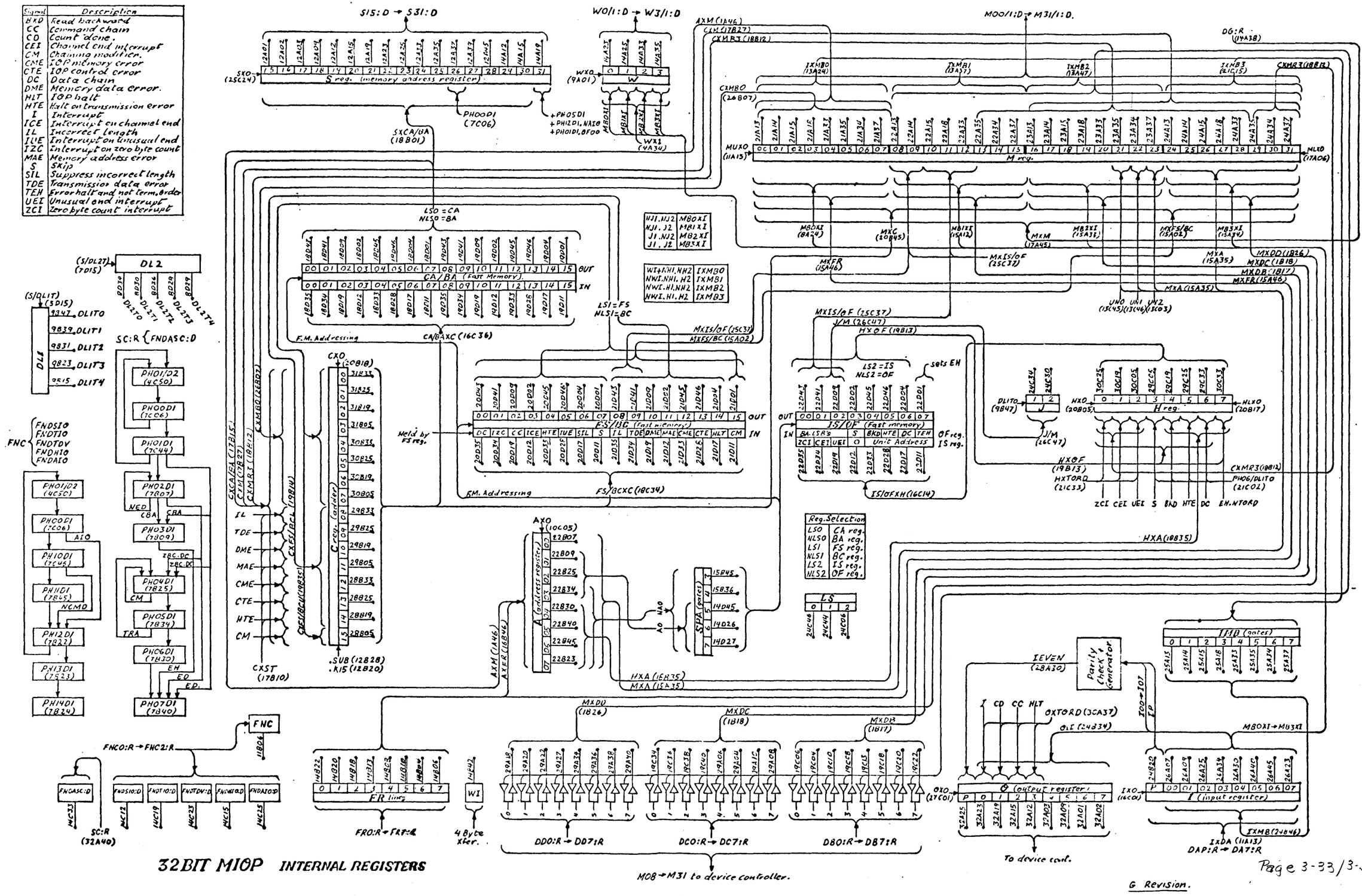
1. HIO is the same as TIO except the Device must stop all operations.

AIO (ACKNOWLEDGE INPUT/OUTPUT INTERRUPT)

1. CPU sends
   - command to be executed (FNCO:D - FNC2:D) to MIOP.
   - Control Strobe (CNST:R)
2. CPU waits for Proceed (PR:D).
3. MIOP sends
   - AIO Command (FNDAIO:D) to Device Controller.
   - Function Strobe (FS:D)
4. Device Controller responds with:
   - FSL:R
   - its address on FR Lines
   - status unique to Device on data lines
5. MIOP takes
   - Device Address off FR Lines (FRD:R → FR7:R)
   - its own address off its switches (UNO → UN2)
   - status unique to Device off Data Lines
   - interrupt status from IS register (ISO0 → ISO2)
   - operational status from FS reg. (FSO8 - FSO9)

   and store it into loc. 20
6. MIOP sends Proceed to CPU.
7. CPU takes the status from location 20 and stores it in its designated register.

Symbol	Description
BKD	Read backward
CC	Command chain
CO	Count done.
CEI	Channel end interrupt
CM	Chaining modifier.
CME	IOP memory error
CTE	IOP control error
DC	Data chain
DME	Memory data error.
HLT	IOP halt
HTE	Halt on transmission error
I	Interrupt
ICE	Interrupt on channel end
IL	Incorrect length
IUE	Interrupt on unusual end
IZC	Interrupt on zero byte count
MAE	Memory address error
S	Skip
SIL	Suppress incorrect length
TDE	Transmission data error
TEH	Error halt and not term. Brdcst
UEI	Unusual end interrupt
ZCI	Zero byte count interrupt



SIO (32 Bit MIOP)

CPU

CNST:R (12C20)
IOPA0:R (12C08)
IOPA1:R (12C13)
IOPA2:R (12C1R)
FNC0:R (12C06)
FNC1:R (12C04)
FNC2:R (12C10)
PR:D (12C45)

PH101/D2 (4C50) : Initiate next operation

PR:D = LASTONE.NME (13C43) (17A18)
(S/DL2T) (7D15) = ME (10C20) = IOP address recognition

DL2T0: FNC (11B06) (8D34) CPU function
DL2T2: FNDSIO:D (14C12) (6D26)
DL2T4: PH00D1 (7C06) (8D29)

FNDSIO:D (14C12)

PH100D1 (7C06) : Access location 20

(S/DLIT) (5D15) = FIN (12836) = End of previous operation.

DLIT0: S26:D (12A37) (9847) sets Sreg. to location 20
HX0 (20B05) } Clears H reg.
HLX0 (20B17) }
DLIT1: WX0 (9A01) (9839) Clears W0→W3 for read
MS (1AC4) = Memory request
CC1 (4C04)
CC2 (4C20)
LS0 (24C46)
LS2 (24C06)
DLIT2: AXM (1A46) (9831) for device address to Areg.
SUB (12B28)
K15 (12B20)
DLIT3: IXMB (24B46) (9823) IXMB0 (13A24) } M00→07 to Ireg
DLIT4: PH10D1 (7C46) (9815)

MQ:D (10A01)

PH110D1 (7C46) : Initiate status return and store 1rst status word.

(S/DLIT) (5D15) = MDR (1A30) set with POK:R = Memory cycle completed.

DLIT0: [M08] = CMD (24B06) (9847) CXCA/BA (17B15) CAreg. to Creg.
[NM08] = CXM (17B27) M16→M31 to Creg.
[M09] = TPE (12B06) 0XI (24B34) Device address to 0 reg.
WX1 (4A34) sets W0→W3 for write
DLIT2: FS:D (14C35) (9831) Creg.-) to Creg.
DLIT4: MXC (20B44) (9815) for CA-1 to M00→M15
[CMD] = PH11D1 (7B45) MS (1A04)
[NCMD] = PH12D1 (7B22) NLS1 (24C42)

AV0:R resets FS:D

FS:D (14C35)
00:D (32A23)
01:D (32A19)
02:D (32A15)
03:D (32A12)
04:D (32A08)
05:D (32A09)
06:D (32A01)
07:D (32A02)
A.C. ADDRESS

AV0:R (1D08)

POK:R (10A27)
MQ:D (10A01)

CMD
NCMD

PH111D1 (7B45)

(S/DLIT) (5D15) = PH11D1 (7B45)

DLIT0: CXM (17B27) (9847) M16→M31 to Creg.
DLIT4: PH12D1 (7B22) (9815) NLS1 (24C42)

NCMD

PH12D1 (7B22) = Prepare 2nd word of status.

(S/DLIT) (5D15) = (NFS+FSL).(NMS+MDR) (3C36) (4A36)

DLIT0: S31:D (14A19) (9847) to store in location 21
NFIN (12B34)
NK15 (12B22)
DLIT1: MXFR (15A46) (9839) FR lines to M00→M07
MXFS/BC (15A02)
BC reg. to M16→M31
[DOR:R] = NCC1 (4C02) D.C. address recognition
[IOR:R] = NCC2 (4C22) D.C. not busy
[FNDSIO:D] = OUT (12B44) OUT remembers SIO
DLIT2: [NCC1.NCC2] = CA/BAXC (16C36) (9831) Creg. to CA reg.
NFS:D (11B42)
DLIT3: NFNC (11B08) (9823) LS1 (24C44)
[NTPE] = PR:D (20B15) Proceed to CPU
DLIT4: NFNDSIO:D (7C36) (9815) PH01/D2 (4C50)
PH13D1 (7B23)

FSL:R (14B36)
DOR:R (32A38)
IOR:R (14B34)
FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B18)
FR3:R (14B13)
FR4:R (14B08)
FR5:R (14B10)
FR6:R (14B04)
FR7:R (14B06)
STATUS

DR:R (10A10)
NCC1=NCOND1:D (18B46)
NCC2=NCOND2:D (28B12)
PR:D (12C45)

Allow next operation to start

PH113D1 (7B23) = Store 2nd status word.

(S/DLIT) (5D15) = PH13D1 (7B23)

DLIT0: CXFS/BCL (19B14) (9847) FS8→FS14 to C8→C14
HXA (18B35)
A04→A07 to H4→H7
H0→H3 is cleared
DLIT2: [NCC1.NCC2] = IS/0FXH (16C14) (9831) Hreg. to IS reg
[TPE] = MS (1A04)
MXC (20B44)
operation status to M08→M14
DLIT4: NLS2 (24C08) (9815) PH14D1 (7B24)

MQ:D (10A01)

AR:R (10A08)
PR:D (12C45)

PH14D1 (7B24) = Clear OF and FS reg. and terminate

(S/DLIT) (5D15) = PH14D1 (7B24)

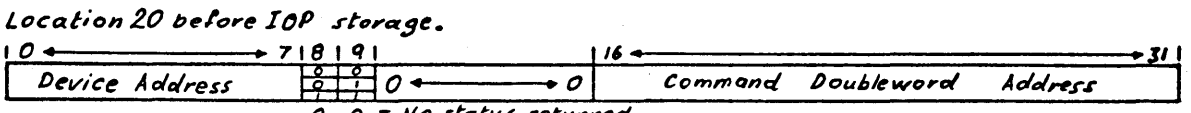
DLIT0: HX0 (20B05) } Clears H reg.
(9847) HLX0 (20B17) }
CX0 (20B18) Clears C reg.
DLIT1: [NCC1.NCC2] = IS/0FXH (16C14) (9839) Clears OF reg.
FS/BCXC (18B34) Clears FS reg.
DLIT3: FIN (12B36) (9823)

AR:R sets PR:D (12C45)

MEMORY

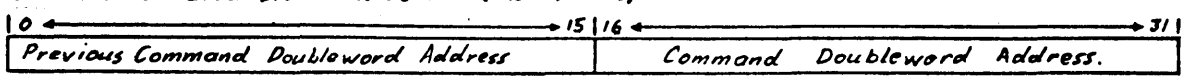
DEVICE CONTROLLER

Location 20 before IOP storage.

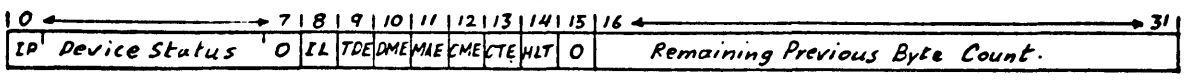


0 0 = No status returned
0 1 = 1 word of status returned.
1 1 = 2 words of status returned.

Location 20 after 1rst Status word is stored,



Location 21 after 2nd Status word is stored.



CME = IOP Memory Error.
CTE = IOP Control Error
DME = Memory Data Error
HLT = IOP Halt
IL = Incorrect Length
IP = Interrupt Pending
MAE = Memory Address Error
TDE = Transmission Data Error.

Note: Every PH# DI/D2 term is reset at T3 of its delay line.
Every PH# PDI/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

G Revision.

TIO, TDV, HIO (32 Bit MIOP)

CPU

CNST:R (12C20)
IOPA0:R (12C08)
IOPA1:R (12C13)
IOPA2:R (12C18)
ENC0:R (12C06)
ENC1:R (12C04)
ENC2:R (12C10)
PR:D (12C45)

PH01/D2 (4C50) = Initiate next operation

PR:D = LASTONE . NM2 (13C43) (17A18)
(S/DL2T) (7D15) = ME (10C20) = IOP address recognition.

DL2T0: FNC (11B06) (8D34) CPU function

DL2T2: for TIO FNDTIO:D (14C19) (8D26) for TDV FNDTDV:D (14C23) for HIO FNDHIO:D (14C15)

DL2T4: PH00D1 (7C06) • (8D29)

or FNDTIO:D (14C19)
or FNDTDV:D (14C23)
or FNDHIO:D (14C15)

MR:D (10A01)

PH100D1 (7CC6): Access location 20

(S/DL1T) (5D15) = FIN (12B36) = End of previous operation

DL1T0: S26:D (12A37) (9B47) Sets S reg. to location 20 HXC (20B05) } clears Hreg. HLX0 (20B17) }

DL1T1: WX0 (9A01) (9B39) Clear W0 → W3 for read
MS (1A04) = Memory request
CC1 (4C04)
CC2 (4C20)
LS0 (24C46)
LS1 (24C44)
LS2 (24C06)

DL1T2: AXM (1A46) (9B31) for device address to Areg.
SUBC (12B26)
K15 (12B20)

DL1T3: IXMB (24B46) (9B23) IXMB0 (13A24) } for M00 → 07 to I reg.

DL1T4: PH10D1 (7C46) (9B15)

POK:R (10A27)
MQ:D (10A01)

PH10D1 (7C46) = Initiate status return and store 1st status word.

(S/DL1T) (5D15) = MDR (1A30) set with POK:R = Memory cycle completed.

DL1T0: [M0B] = CMD (24BC6) (9B47) CXCA/BA (17B15) CA reg to C reg.
[NM0B] = CXFS/BCL (19B14) FSB → FS14 to Creg.
[M09] = TPE (12B06)
0XI (24B34) Device Address to B reg.
WX1 (4A34) sets W0 → W3 for write

DL1T2: FS:D (14C35) (9B31) Creg − 1 to Creg

DL1T4: MXC (20B44) (9B15) for CA−1 to M00 → M15
[CMD] = PH11D1 (7B45)
MS (1A04)
[NCMD] = PH12D1 (7B22)
NLS1 (24C42)

AV0:R resets FS:D

FS:D (14C35)

00:D (32A23)
01:D (32A19)
02:D (32A15)
03:D (32A12)
04:D (32A03)
05:D (32A09)
06:D (32A01)
07:D (32A02)

D.C. Address

AV0:R (1D08)

CMD
NCMD

PH11D1 (7B45)

(S/DL1T) (5D15) = PH11D1 (7B45)

DL1T0: CXFS/BCL (19B14) (9B47) FSB → FS14 to Creg.

DL1T4: PH12D1 (7B22) (9B15 NLS1 (24C42)

NCMD

DR:R (10A10)

PH12D1 (7B22) = Prepare and store 2nd status word.

(S/DL1T) (5D15) = (NFS + FSL) . (NMS + MDR)
(3C36) (4A36)

DL1T0: S31:D (14A19) (9B47) to store in location 21 NFIN (12B34)

DL1T1: MXFR (15A46) (9B39) FR lines to M00 → M07
MXFS/BC (15A02)
BC reg. to M16 → M31
[DOR:R] = NCC1 (4C02) D.C. Address recognition
[IOR:R] = NCC2 (4C22) D.C. not busy
MXC (20B44) operational status to M08 → M15
[TPE] = MS (1A04)

DL1T2: [NCC1.NCC2] = CA/BAXC (16C36) (9B31) Creg. to CA reg.
NFS:D (11B42)

DL1T3: NFNC (11B08) (9B23) [NTPE] = PR:D (20B15) Proceed to CPU.

DL1T4: if TIO = NFNDTIO:D (9B15) if TDV = NFNDTDV:D if HIO = NFNDHIO:D PH01D2 (4C50) PH13D1 (7B23)

FSL:R (14B36)
DOR:R (32A38)
IOR:R (14B34)

FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B18)
FR3:R (14B13)
FR4:R (14BC8)
FR5:R (14B10)
FR6:R (14BC4)
FR7:R (14BC6)

Status

PR:D (12C45)
MQ:D (10A01)
NCC1=NCOND1:D (1B46)
NCC2=NCOND2:D (2B12)

Allow next operation to start.

PH13D1 (7B23)

(S/DL1T) (5D15) = PH13D1 (7B23)

AR:R sets PR:D (12C45)

DL1T4: PH14D1 (7B24) (9B15).

PR:D (12C45)
AR:R (10A08)

PH14D1 (7B24) = Terminate

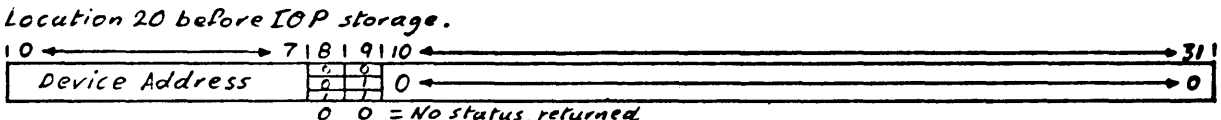
(S/DL1T) (5D15) = PH14D1 (7B24)

DL1T3: FIN (12B36) (9B23)

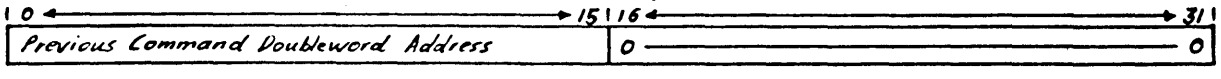
Memory

Device Controller

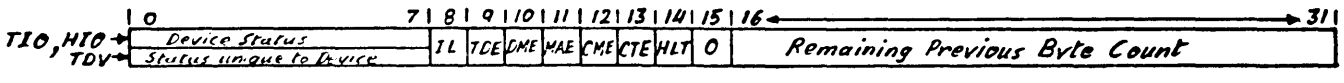
Location 20 before IOP storage.



Location 20 after 1rst Status word is stored.



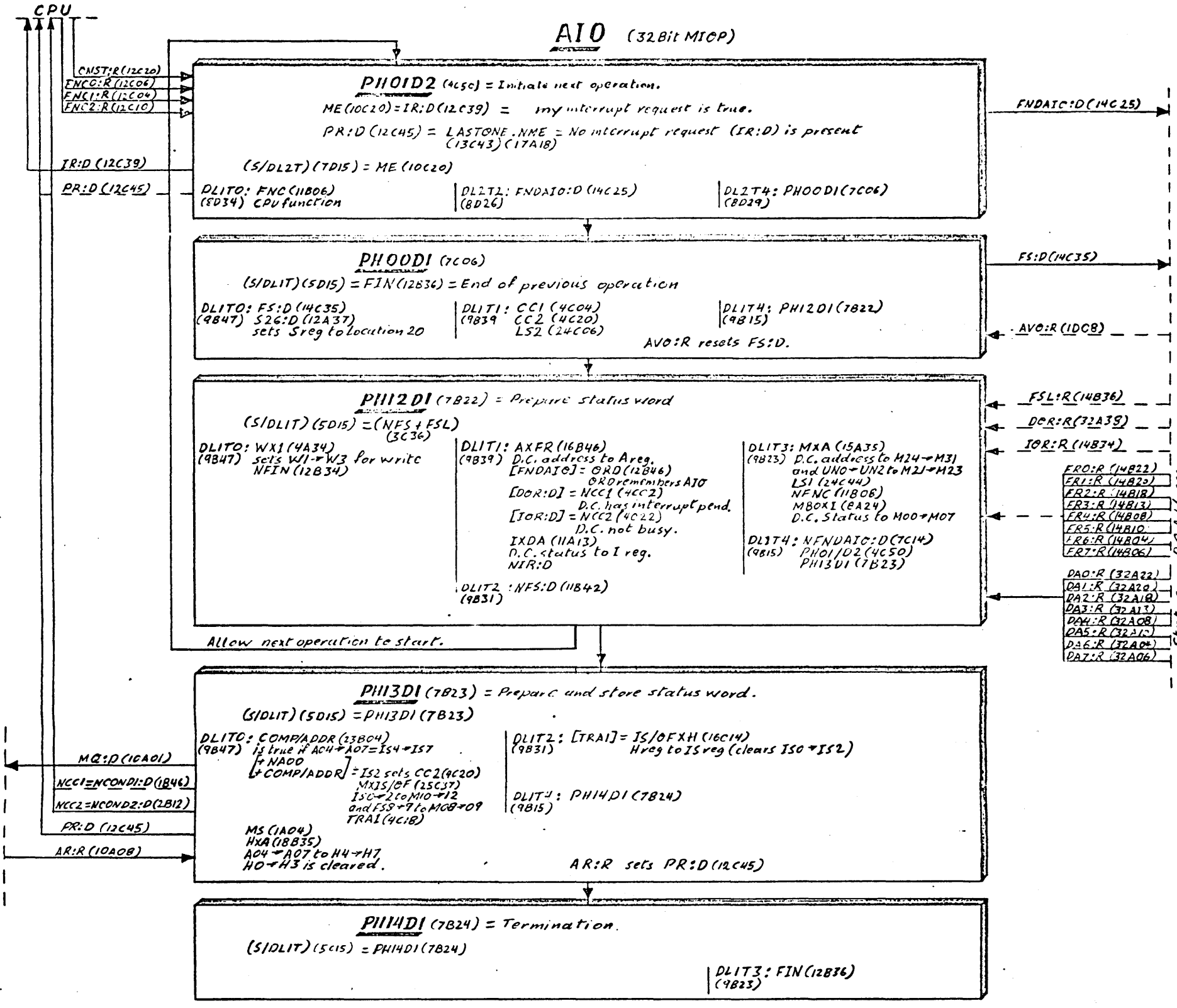
Location 21 after 2nd Status word is stored.



CME = IOP memory error.
CTE = IOP control error
DME = Memory data error
HLT = IOP halt
IL = Incorrect length
MAE = Memory address error
TDE = Transmission data error

Note: Every PH#D1/D2 term is reset at T3 time of its delay line.
Every PH#PD1/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

G Revision



Location 20 after responce is stored.

0 ← 7	8	9	10	11	12	13 ← 20	21 ← 23	24	25 ← 27	28 ← 31
Status unique to device	IL	TDE	ZCI	CEI	UEI	0 ← 0	IOP#	M	D.C.	D.
							I.O. Address			

CEI = Channel end interrupt
IL = Incorrect length
TDE = Transmission data error
UEI = Unusual end interrupt.
ZCI = Zero byte count interrupt

D. = if 'M.'=0 then D.= device controller number. if 'M.'=1 then D.= unit number.
D.C. = multiunit device controller number.
M. = if 0 means single unit device. if 1 means multiunit device.

Note: Every PH#D1/D2 term is reset at T3 time of its delay line. Every PH#P01/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

ORDER OUT (32 Bit MIOP)

PH01/D2 (4C50) = Initiate next operation.
(S/DL2T) (7D15) = SC:R (32A40).

DL2T2: FNDASC:D (14C33) (8D26)

DL2T4: FS:D (14C35) (8D29) PH00D1 (7C06)

SC:R (32A40)
FNDASC:D (14C33)
FS:D (14C35)

PH00D1 (7C06) = Service connect
(S/DLIT) (5D15) = FIN • (NASC + FSL) (12B36) (17B33)

DLIT1: AXFR (16B46) (9B39) NCMD (24B08)

DLIT2: NFS:D (11B42) (9B31) K15 (12B20)

DLIT4: [NFNDASC:D] = PH01/D2 (4C50) (9B15) [FNDASC:D] = PH01D1 (7C44)

AV0:R erases FNDASC:D

AV0:R (1D08)
FSL:R (14B36)
FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B16)
FR3:R (14B13)
FR4:R (14B08)
FR5:R (14B10)
FR6:R (14C04)
FR7:R (14B06)
D.C. Address

NFNDASC:D

FNDASC:D

PH01D1 (7C44) = Determine type of service call.
(S/DLIT) (5D15) = RS:R (14B27)

DLIT0: NFIN (12B34) (9B47)

DLIT1: DOR:R marks ORD (12B46) (9B39) IOR:R marks OUT (12B44) ORDOUT (10B36) NFNDASC:D (7C22) [ED:R] = ED:D (32A33)

DLIT2: TORD (24B04) (9B31) NES:D (11B28) LSO (24C46)

DLIT4: PH01/D2 (4C50) (9B15) PH04D1 (7B25)

RS:R (14B27)
DOR:R (32A38)
IOR:R (14B34)
ED:R (32A34)
NES:D (11B28)
ED:D (32A33)

Allow next operation to start.

TRA

ORDOUT

NMS.PH04D1

PH04D1 (7B25) = Access 1st word of command pair.
(S/DLIT) (5D15) = NMS (1A02)

DLIT0: SXCA/BA (18B01) (9B47) CA reg to Sreg, CXCA/BA (17B15) CA reg. to Creg. NSUB (12B30) HXO (20BC5) } Clears H reg. HLXO (20B17) [NCMD] = NTRA1 (4C14) MPE sets FP (12B18)

DLIT1: 1st time through (NFES1S.NEH) sets MS (9B39) 2nd time through (CMD) sets MS FSIS1S chaining modifier bit. WXO (9A01) clears WC→W3 for read.

DLIT2: Creg+1 to Creg. (9B31)

DLIT3: [MS+NEH] = CA/BAXC (16C36) (9B25) Creg to CA reg. IXMB (24B46) } gates H00→H07 IXMBO (13A24) } to I reg. CMD (24B06)

DLIT4: [NMS.NEH] = PH04D1 (7B25) (9B15) [MS+EH] - PH05D1 (7B34) [MS] = NK15 (12B22) NLS1 (24C42) NLS2 (24C08)

MQ:D (10A01)

MS

NMS

PH05D1 (7B34) = Access 2nd word of command pair
(S/DLIT) (5D15) = MDR (1A30) set with POK:R = Memory Cycle Completed.

DLIT0: [ORD] = 8XI (24B34) (9B47) $31:D (14A19) if order = 08 = TRA (15A15) [TRA] = CXM (17B27) M16→M31 to Creg [NTRA] = NLSO (24C50) CXMR3 (18B13) M13→M28 to Creg. M29→31 to H0→H2 [TRA.TRA3] = EH (24B44)

DLIT1: [NTRA.NEH] = MS (1A04) (9B39)

DLIT2: [(NTRA+EH).ORD] = RSA:D (9B31) [NEH] = CA/BAXC (16C36)

DLIT4: TRA1 (4C18) (9B15) [TRA] = K15 (12B20) [TRA.NEH] = PH04D1 (7B25) [NTRA+EH] = PH06D1 (7B30)

POK:R (10A27)
MQ:D (10A01)
00:D (32A23)
01:D (32A19)
02:D (32A15)
03:D (32A12)
04:D (32A03)
05:D (32C09)
06:D (32A01)
07:D (32A02)
Order
RSA:D (14C03)

TRA

PH06D1 (7B30) = Processes 2nd word.
(S/DLIT) (5D15) = (NMS + MDR) (4A36)

DLIT0: CXM (17B27) (9B47) M16→M31 to C reg. M07 (=skip) sets H3 (29C05) Read reverse sets H4 (29C19) MC4 (=HTE) sets H5 (29C25) MC0 (=UC) sets H6 (29C33)

DLIT2: [NEH] = FS/BCXC (18C34) (9B31) Creg to BC reg. IS/OFXH (16C14) H log. to OF reg. [N1+N2+NC00T12] = IER:D (14C45)

DLIT4: LS1 (24C44) (9B15) PH07D1 (7B40)

POK:R (10A27)
IER:D (14C45)

PH07D1 (7B40) = Termination.
(S/DLIT) (5D15) = RS:R (14B27)

DLIT1: ES:D (14C09) (9B39) EH set 03:D (32A12)

DLIT2: [NEH] = CXMBO (26B07) (9B31) M00→M07 to C00→C07 CXFS/BCL (19B14) FS08→FS14 to C08→C14 MAE sets C11 (29B05) MPE sets C12 (28B33) (EH.NMAE.NMPE) sets C13 (28B25) EH sets C14 (28B19)

DLIT3: FS/BCXC (18C34) (9B23) Creg to FS reg.

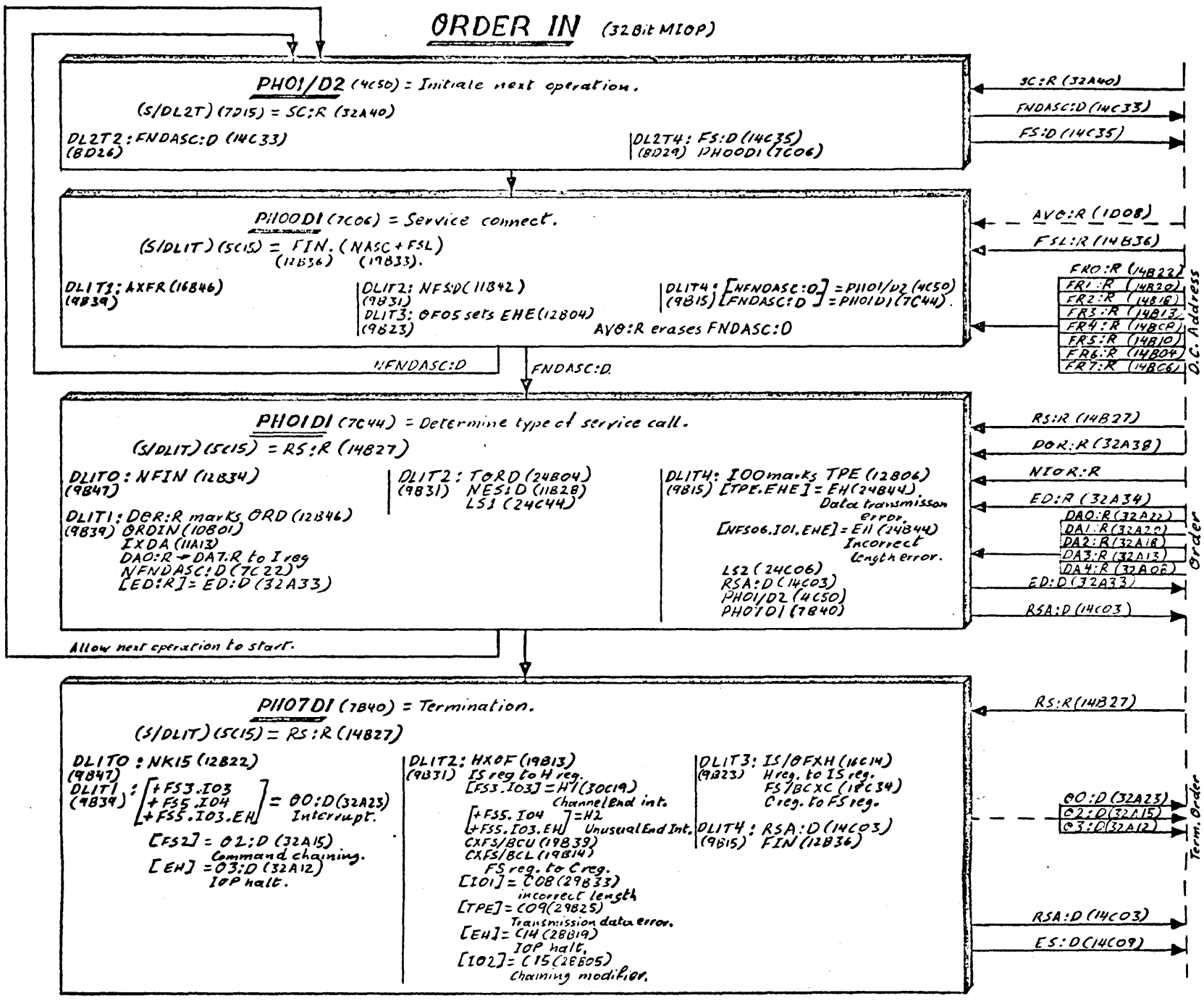
DLIT4: RSA:D (14C03) (9B15) FIN (12B36).

RS:R (14B27)
03:D (32A12)
ES:D (14C09)
RSA:D (14C03)
Device Controller.

Memory

Note: Every PH#D1/D2 is reset at T3 time of its delay line.
Every PH#PD1/D2 is set at T1 time of its delay line and reset at T0 time of its delay line.

G Revision



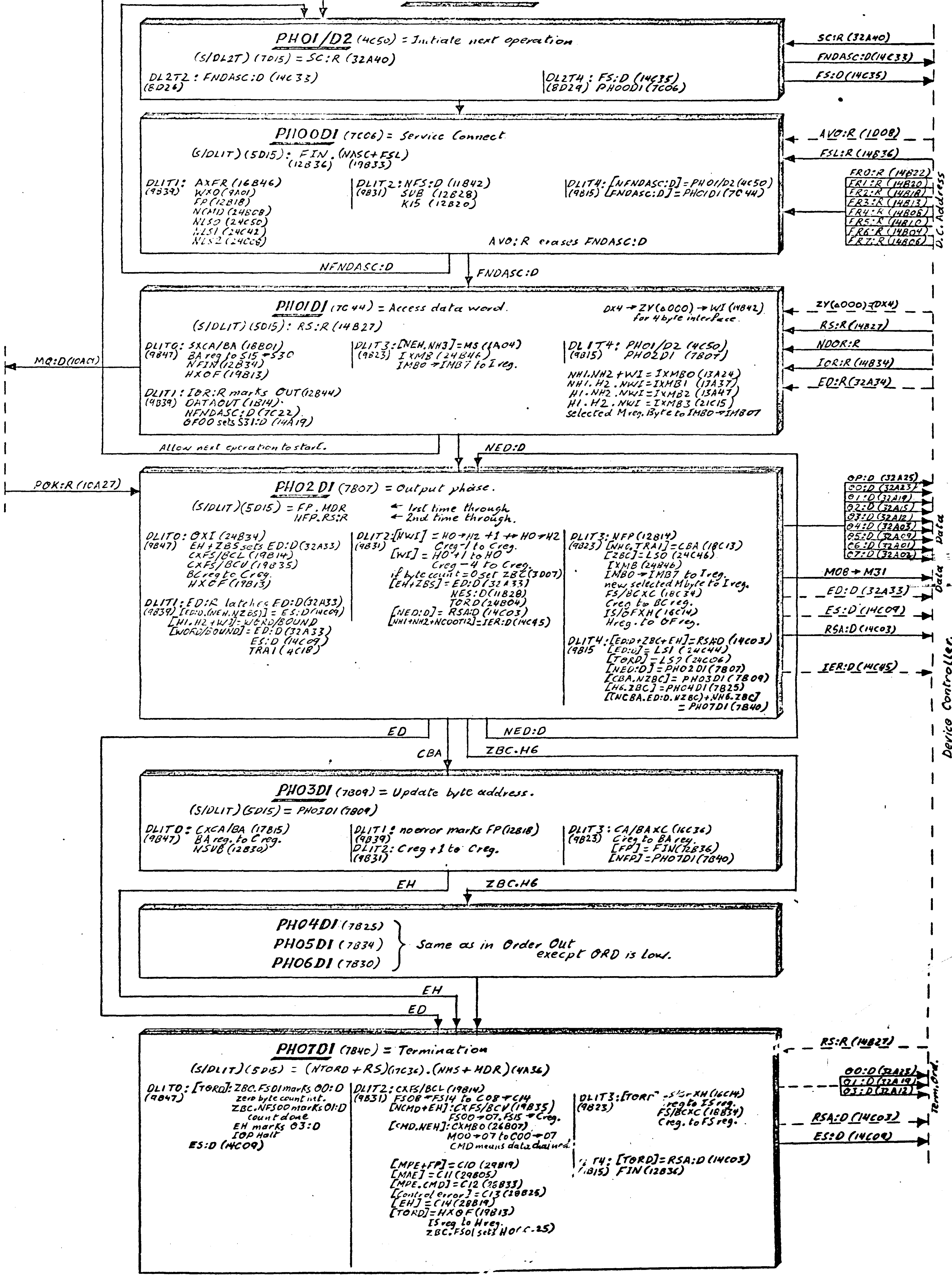
Note: Every PH#D1/D2 is reset at T3 time of its delay line.
Every PH#D1/D2 is set at T1 time of its delay line and reset at T0 time of its delay line.

ORDER

DA0:R = Transmission error
DA1:R = Incorrect length
DA2:R = Chaining modifier
DA3:R = Channel end.
DA4:R = Unusual end.

G Revision

DATA OUT (32 Bit MIOP)



Note: Every PH#D1/D2 term is reset at T3 time of its delay line.
Every PH#PD1/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

DATA IN (32 Bit MIOP)

PH01/D2 (4C50) = Initiate next operation

(S/DLIT)(7D15) = SC:R (32A40)

DL2T2 : FNDASC:D(14C33) (8D26)

DL2T4: FS:D (14C35) (8D29) PH00D1 (7C06)

SC:R (32A40)
FS:D (14C35)
FNDASC:D (14C33)

PH00D1 (7C06) = Service connect.

(S/DLIT) (5D15) = FIN . (NASC+FSL) (12B36) (14B33)

DLIT1: AXFR (16B46) (9B39) WX0 (9A01) FP (12B18) NCMD (24B08) NLSC (24C50) NLS1 (24C42) NLS2 (24C08)

DLIT2: NFS:D(11B42) (9B31) SUB (12B28) KIS (12B20)

DLIT3: CF07 marks EH (24C44) (4B23) CF05 marks EHE (12B14)

DLIT4 : [NFNDASC:D] = PH01 D2 (4C50) (9B15) [FNDASC:D] = PH01 D1 (7C44)

AV0:R erases FNDASC:D

AV0:R (1D08)
FSL:R (14B36)
FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B18)
FR3:R (14B13)
FR4:R (14B08)
FR5:R (14B15)
FR6:R (14B04)
FR7:R (14B06)
B.C. Address

NFNDASC:D

FNDASC:D

PH01D1 (7C44) = Input phase

(S/DLIT)(5D15) = RS:R (14B27)

DX4 → ZY(a000) → WI (14B42) for 4 byte interface

DLIT0: SXCA/BA (18B01) (9B47) BA reg to S15 → S30 HXOF (17B13) 8F00 marks S31:D (14A19) erase J1 and J2 CXFS/BCL (19B14) CXFS/BCU (19B35) BC reg. to Creg. NFIN (12B34)

DLIT1 : (J/M) (26C47) (9B39) 8F01 → 02 to J1 → 2 IXDA (11A13) [+WI, +NH4.H1.H2, +H4.NH1.NH2] = WORD/BOUND [WORD/BOUND] = ED:D (32A33) ES:D (14C09) TRA1 (4C18) ED:R marks ED:D (32A33) NFNDASC:D (7C22) DATAIN (1B15)

DLIT2: [NWI] = if NH4 then HO → 2+1 to HO → 2 if H4 then HO → 2-1 to HO → 2 Creg - 1 to Creg. for Ireg. to selected M byte NJ1.NJ2 = MB0XI (8A24) NJ1.J2 = MB1XI (15A12) J1.NJ2 = MB2XI (15A33) J1.J2 = MB3XI (15A34) MB0XI marks W0 MB1XI marks W1 ect. [WI] = HO → 2±4 to HO → 2 Creg. - 4 to Creg. WX1 (4A34) sets W0 → W3 MXDB (1B17) MXDC (1B18) MXDD (1B26) byte count = 0 set ZBC (3D07) [EH+ZBS] = ED:D (32A33) NES:D (11B28) TORD (24B04) [NEH.NZBS.ED:D] = ES:D (14C09) [NED.NZBS.NEH] = RSA:D (14C03) [NH1+NH2+NCOOT12] = IER:D (14C45)

DLIT3: IS/0FXH (16C14) (9B23) Hreg to 0F reg. FS/BCXC (18C34) Creg to BC reg. NFP (12B14) [+TRA1.NH0.NH4, +TRA1.H0.H4] = CBA (18C13) [(ED+ZBC-EH).NH3] = MS (1AC4) [ZBC] = LS0 (24C46)

DLIT4: IFEVEN marks TPE (12B06) (9B15) [TPE.EHE] = EH (24B44) [ED:D] = LS1 (24C44) [TORD] = LS2 (24CC6) [ED+EH+ZBC] = RSA:D (14C03) PH01/D2 (4C50) [NED:D] = PH02 D1 (7B07) [CBA.NZBC] = PH03 D1 (7B09) [ZBC.H6] = PH04 D1 (7B25) [NCBA.ED:D.NZBC+NH6.ZBC] = PH07 D1 (7B40)

ZY(a000) = (DX4)
RS:R (14B27)
NDOR:R
NIOR:R
ED:R (32A34)
DACR → DA7R
DB0:R → DB7:R
DC0:R → DC7:R
DD0:R → DD7:R
IER:D (14C45)
RSA:D (14C03)
ED:D (32A33)
ES:D (14CC9)
Data
Device Controller.

MQ:D (10A01)

Allow next operation to start.

ZBC.H6

ED:D

CBA

NED:D

NED:D

PH02D1 (7B07) = Input phase

(S/DLIT)(5D15) = RS:R (14B27)

DLIT0: erase J1 and J2 (9B47) HXOF (19B13) CXFS/BCL (19B14) CXFS/BCU (19B35) BC reg. to Creg.

DLIT1 : (J/M) = 26C47 (9B39) 8F01 → 8F02 to J1 → J2 IXDA (11A13) [+NH4.H1.H2, +H4.NH1.NH2] = WORD/BOUND [WORD/BOUND] = ED:D (32A33) ES:D (14C09) TRA1 (4C18)

DLIT2: if NH4 then HO → H2+1 to HO → H2 (9B31) if H4 then HO → H2-1 to HO → H2 Creg. -1 to Creg. for Ireg. to selected M byte. NJ1.NJ2 = MB0XI (18A24) NJ1.J2 = MB1XI (15A12) J1.NJ2 = MB2XI (15A33) J1.J2 = MB3XI (15A34) MB0XI marks W0 MB1XI marks W1 ect. byte count = 0 set ZBC (3D07) [EH+ZBS] = ED:D (32A33) NES:D (11B26) TORD (24B04) [NEH.ZBS.ED:D] = ES:D (14C09) [NED:D.NZBS.NEH] = RSA:D (14C03) [NH1+NH2+NCOOT12] = IER:D (14C45)

DLIT3: IS/0FXH (16C14) (9B23) Hreg. to 0F reg. FS/BCXC (18C34) Creg. to BC reg. NFP (12B14) [+TRA1.NH0.NH4, +TRA1.H0.H4] = CBA (18C13) [(ED+ZBC+EH).NH3] = MS (1AC4) [ZBC] = LS0 (24C46)

DLIT4: [IEVEN.PC:R] = TPE (12B06) (9B15) [TPE.EHE] = EH (24B44) [ED:D] = LS1 (24C44) [TORD] = LS2 (24CC6) [ED+EH+ZBC] = RSA:D (14C03) [NED:D] = PH02 D1 (7B07) [CBA.NZBC] = PH03 D1 (7B09) [ZBC.H6] = PH04 D1 (7B25) [NCBA.ED:D.NZBC+NH6.ZBC] = PH07 D1 (7B40)

RS:R (14B27)
ED:R (32A34)
DAP:R (32A27)
DA0:R (32A22)
DA1:R (32A20)
DA2:R (32A18)
DA3:R (32A13)
DA4:R (32AC8)
DA5:R (32A10)
DA6:R (32AC4)
DA7:R (32AC6)
PC:R (32A36)
IER:D (14C45)
RSA:D (14C03)
ED:D (32A33)
ES:D (14C09)
Data

MQ:D (10A01)

Memory.

CBA

CBA

PH03D1 (7B09) = Update byte address

(S/DLIT)(5D15) = PH03D1 (7B09)

DLIT0: CXCA/BA (17B15) (9B47) BA reg. to C reg. NSUB (12B30)

DLIT2: Creg+1 to Creg (9B31)

DLIT3: CA/BAXC (16C36) (9B23) Creg to BA reg

DLIT4: PH07D1 (7B40) (9B15)

ZBC.H6

PH04D1, PH05D1, PH06D1 (7B25) (7B34) (7B30) = Same as in Order Out except ORD is low.

DR:R (10A10)

PH07D1 (7B40) = Termination.

(S/DLIT)(5D15) = (NTORD+RS)(17C36).(NMS+MDR)(4A36)

DLIT0: [TORD]: ZBC.FSD1 marks 00:D zero byte count int. ZBC.NFS00 marks 01:D count done FS2 marks 02:D command chain. EH marks 03:D [OP halt] ES:D (14C09) (9B47)

DLIT2: CXFS/BCL (19BM) (9B31) FS08 → FS14 to C08 → C14 [NCMD+EH] = CXFS/BCU (19B35) FS00 → 07, FS15 to Creg. [CMD.NEH] = CXMB0 (26B07) M00 → M07 to C00 → 07 CMD = data chained. [TPE] = C9 (29B25) [MPE] = C10 (29B19) [MAE] = C11 (29B05) [MPE.CMD] = C12 (28B33) [EH] = C14 (28B19) [TORD] = HXOF (19B13) IS reg to H reg. ZBC.FS01 sets H0 (30C25) [NTORD] = HXOF (19B13) 0F reg. to H reg. EH sets H7 (30C33)

DLIT3: [TORD] = IS/0FXH (16C14) (9B23) H reg. to IS reg. [NTORD error] = IS/0FXH (16C14) H reg. to 0F reg. [+TORD +error] = FS/BCXC (18B34) Creg. to FS reg.

DLIT4: FIN (12B36) (9B15) [TORD] = RSA:D (14C03)

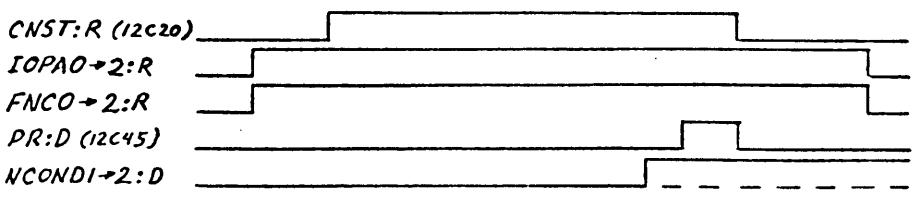
RS:R (14B27)
00:D (32A23)
01:D (32A19)
03:D (32A12)
RSA:D (14C03)
ES:D (14C09)
Data

Note: Every PH#D1/D2 term is reset at T3 time of its delay line.
Every PH#PD1/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

6 Revision.

MIOP Interfaces (32Bit)

CPU / MIOP



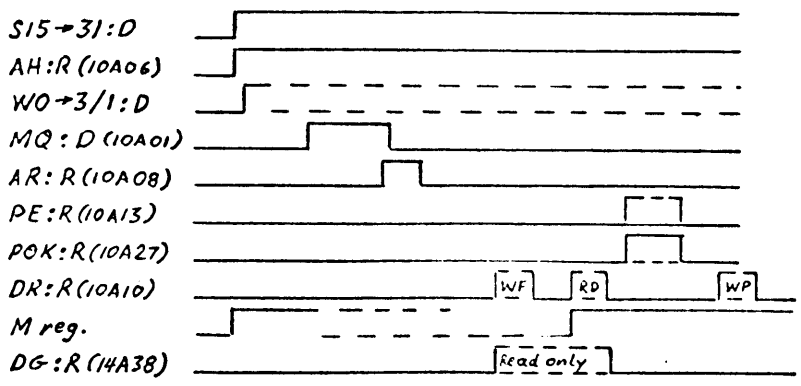
IOPA0:R (12C08)
IOPA1:R (12C13)
IOPA2:R (12C18)

FNC0:R (12C06)
FNC1:R (12C04)
FNC2:R (12C10)

NCOND1:D (12C25)
NCOND2:D (12C33)

W0/1:D (14A23)
W1/1:D (14A25)
W2/1:D (14A33)
W3/1:D (14A35)

MEMORY / MIOP



S reg. (memory address register)

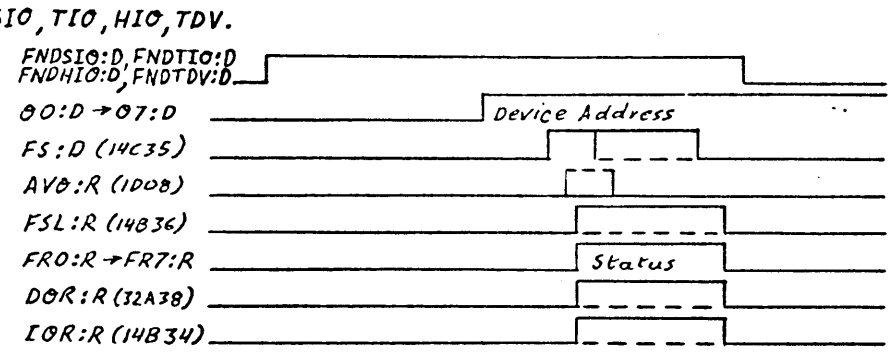
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
12A01	12A02	12A03	12A09	12A12	12A15	12A19	12A23	12A25	12A33	12A35	12A37	12A39	12A45	14A12	14A15	14A19

M register.

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
21A15	21A14	21A15	21A16	21A35	21A35	21A34	21A37	22A15	22A14	22A15	22A16	22A33	22A35	22A34	22A37	23A13	23A14	23A15	23A18	23A33	23A35	23A34	23A37	24A13	24A14	24A15	24A18	24A33	24A35	24A34	24A37

DEVICE CONTROLLER / MIOP

SIO, TIO, HIO, TDV.

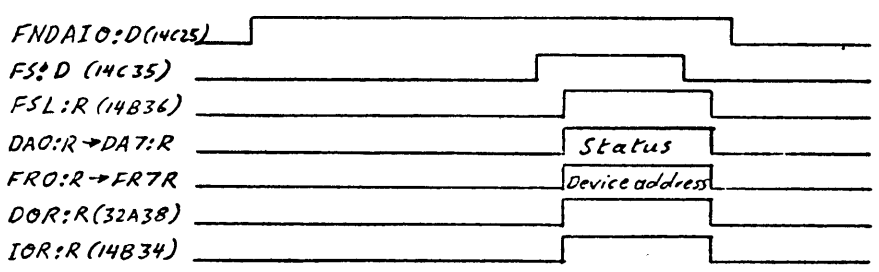


FNDSIO:D (14C12)
FNDTIO:D (14C19)
FNDTDV:D (14C23)
FNDHIO:D (14C15)
FNDAIO:D (14C25)

DATA

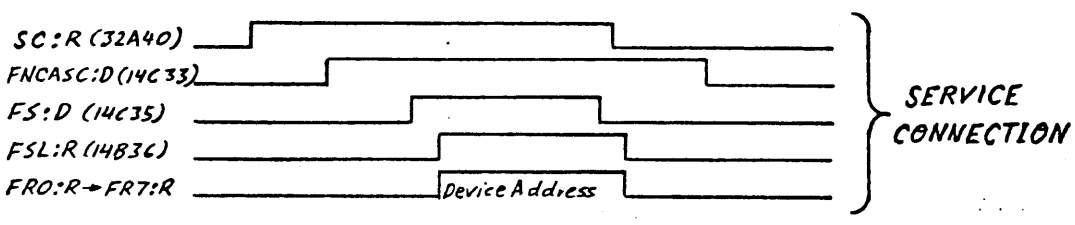
OUT		IN	
OP:D	32A25	DAP:R	32A27
00:D	32A23	DA0:R	32A22
01:D	32A19	DA1:R	32A20
02:D	32A15	DA2:R	32A18
03:D	32A12	DA3:R	32A13
04:D	32A03	DA4:R	32A08
05:D	32A09	DA5:R	32A10
06:D	32A01	DA6:R	32A04
07:D	32A02	DA7:R	32A06
M08	19C02	DB0:R	19C06
M09	19C01	DB1:R	19C04
M10	19C09	DB2:R	19C10
M11	M/C03	DB3:R	19CCE
M12	19C12	DB4:R	19C13
M13	19C15	DB5:R	19C18
M14	19C19	DB6:R	19C20
M15	19C23	DB7:R	19C22
M16	19C33	DC0:R	19C34
M17	19C35	DC1:R	19C36
M18	19C37	DC2:R	19C38
M19	19C39	DC3:R	19C40
M20	29A02	DC4:R	29A06
M21	29A01	DC5:R	29AC4
M22	29AC9	DC6:R	29A10
M23	29A03	DC7:R	29AC8
M24	29A15	DD0:R	29A18
M25	29A19	DD1:R	29A20
M26	29A23	DD2:R	29A22
M27	29A25	DD3:R	29A27
M28	29A33	DD4:R	29A34
M29	29A35	DD5:R	29A36
M30	29A37	DD6:R	29A38
M31	29A39	DD7:R	29A40

AIO



FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B18)
FR3:R (14B13)
FR4:R (14B08)
FR5:R (14B10)
FR6:R (14B04)
FR7:R (14B06).

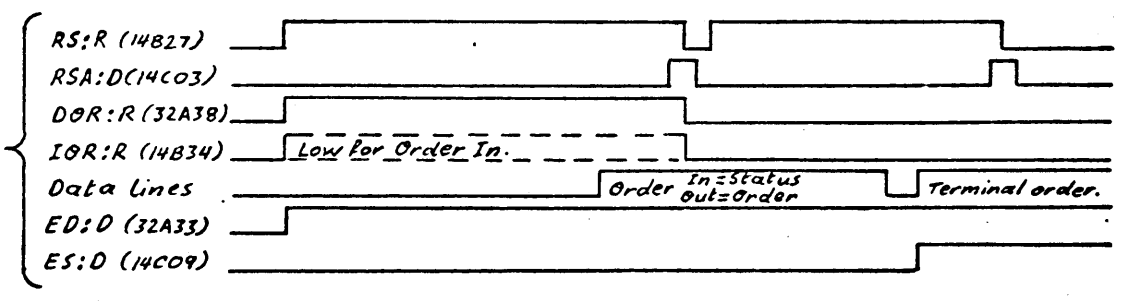
SERVICE CYCLE



SERVICE CONNECTION

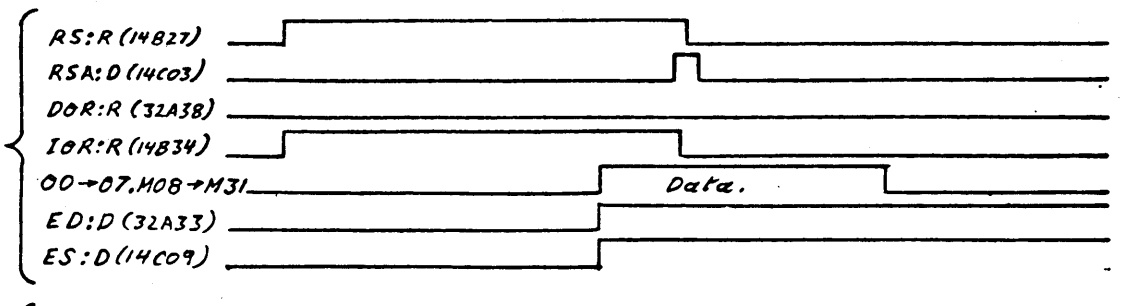
ORDER OUT + ORDER IN

Note: Order In and Out always has a terminal order.



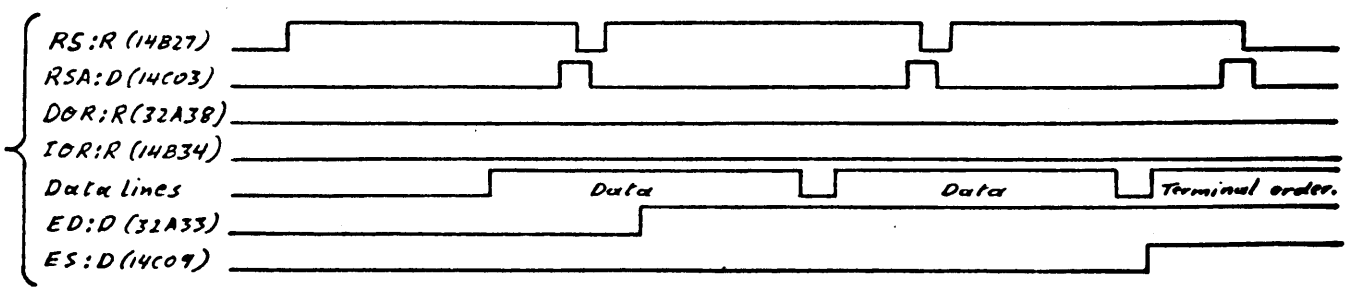
DATA OUT

Using 4byte interface



DATA IN

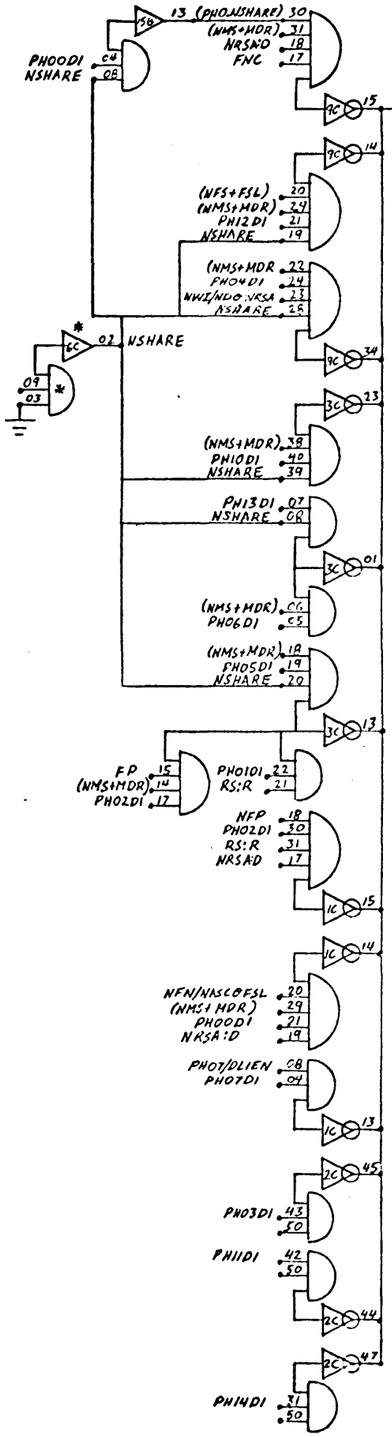
Using 1byte interface 2nd data byte reaches zero byte count (ZBC)

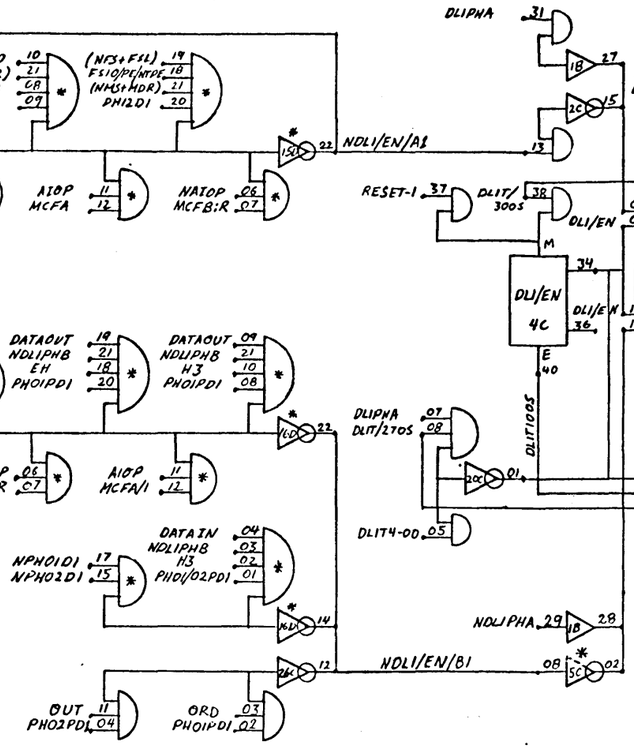


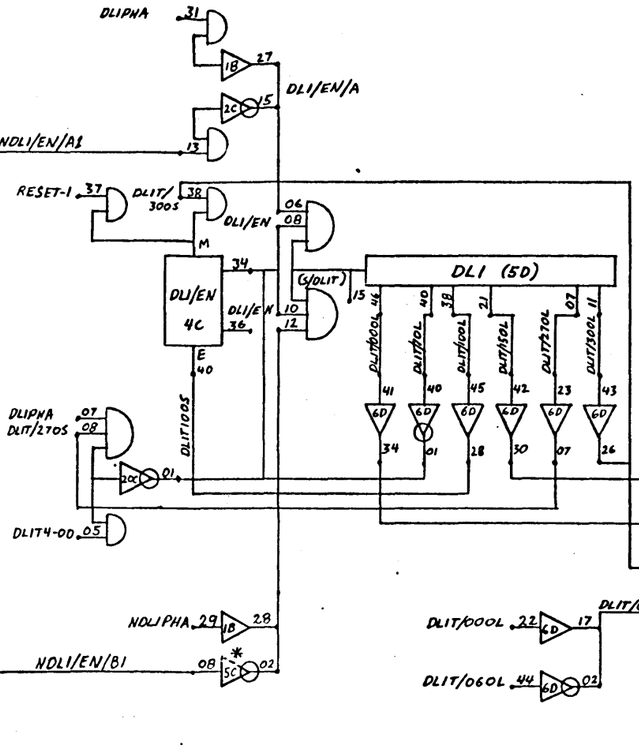
G Revision.

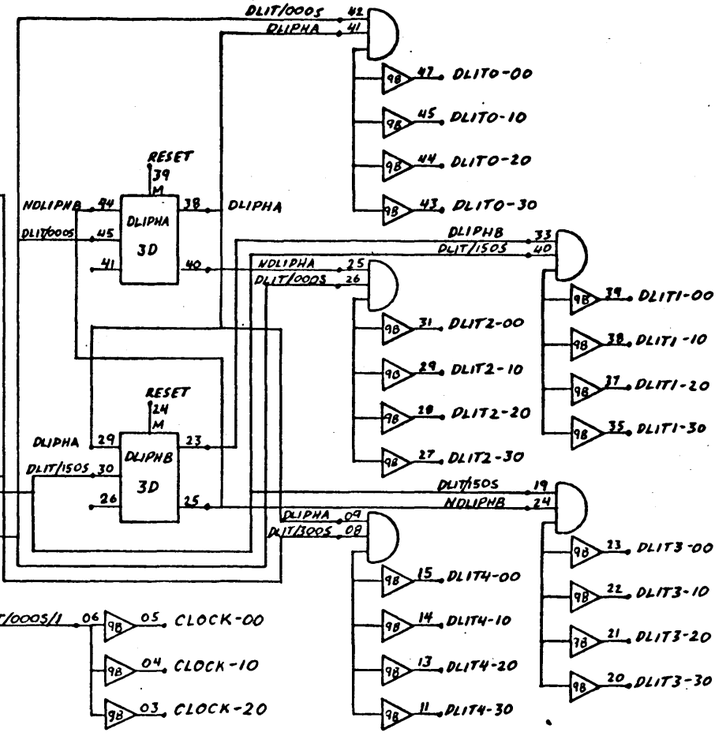
32Bit MIOP CLOCKS

* For bus sharing option only.

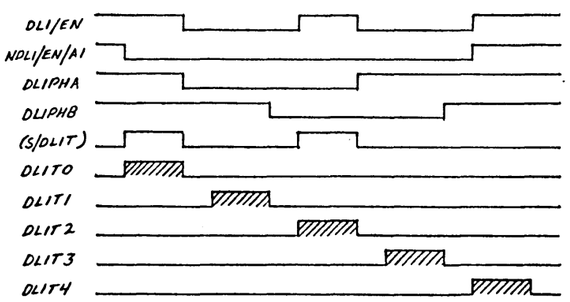


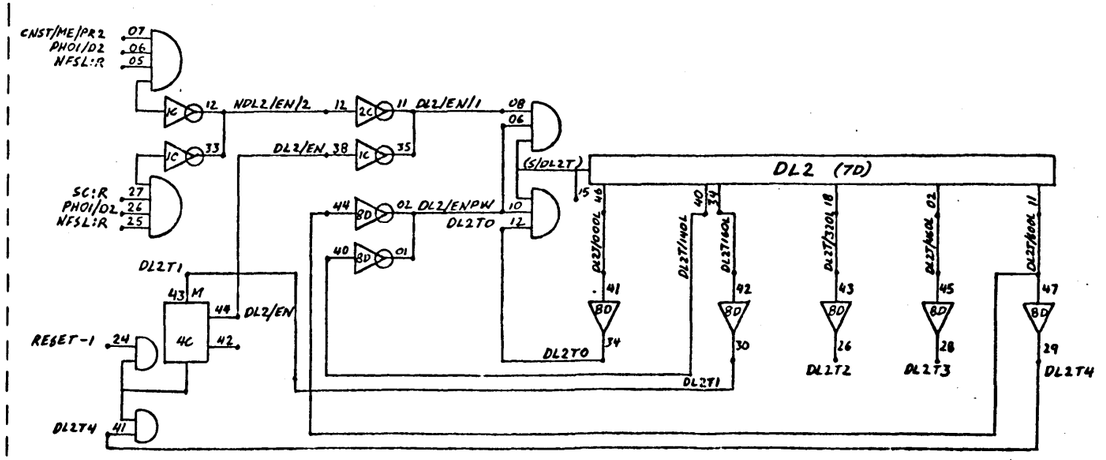






Normal DL1 delay line cycle

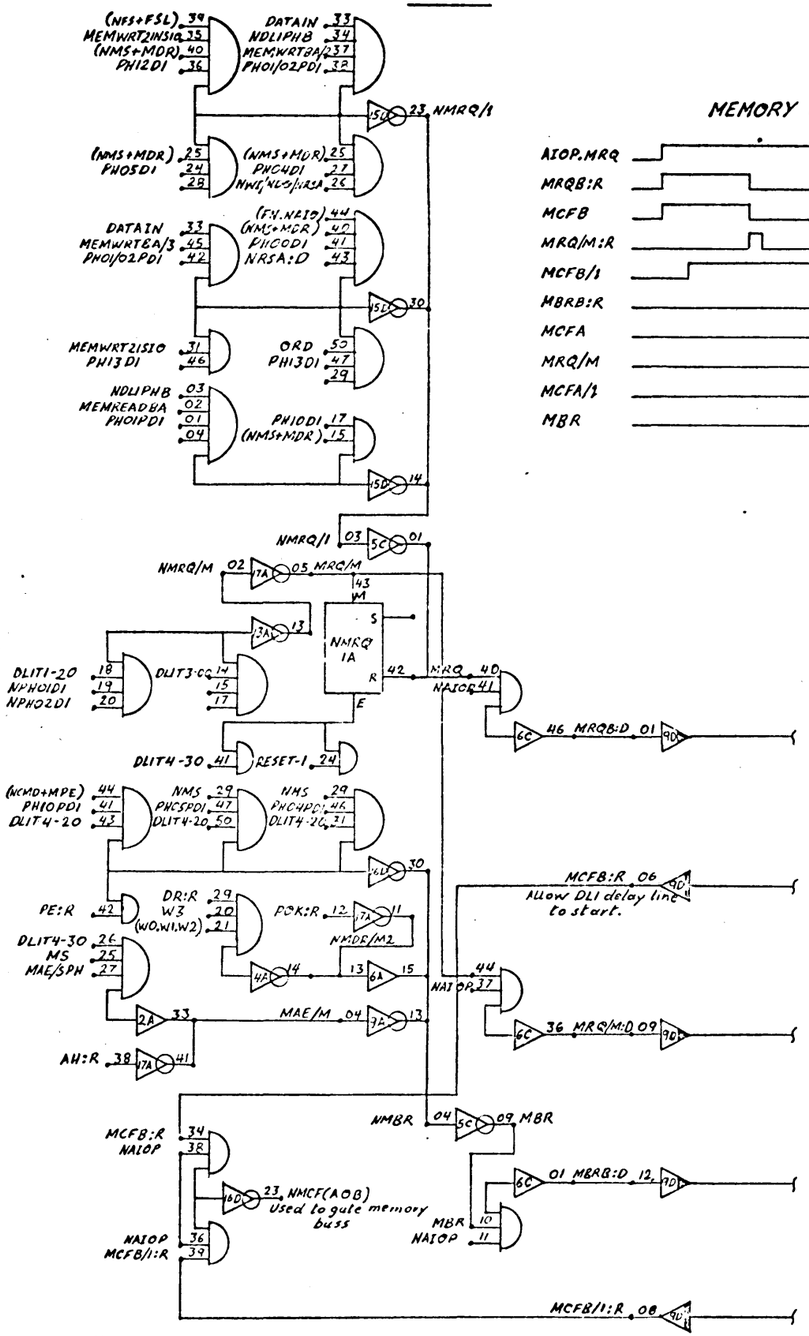




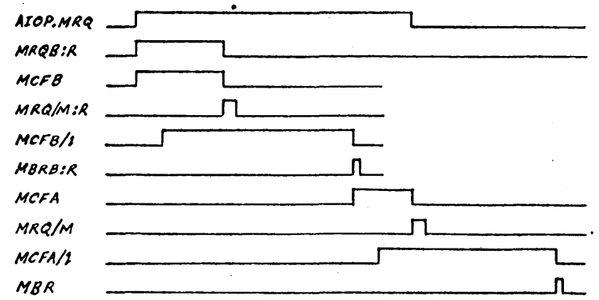
6 Revision

32BIT MIOP BUSS SHARING OPTION

NAIOP



MEMORY CONTROL TIMING



AIOP

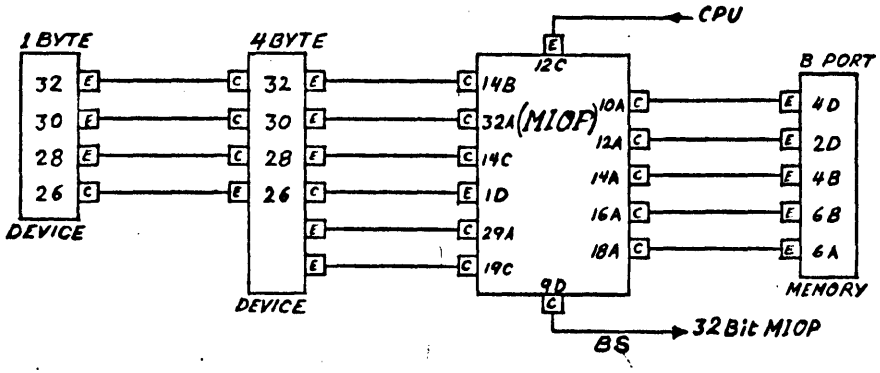
6 Revision

32 Bit MIOP (MODULE CHART)

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	AT11	FT65	LT13	AT11 (4B)	LT12	FT27	FT65	FT63	FT63	FT63	FT63	FT63	XT10	FT27	AT11	IT16	AT11	BT11	AT70	LT13	AT61	IT11	AT11	IT11	LT13	XT10	BT16	BT16	IT11		BT11	FT66
B	XT10	FT18	FT18	FT18	FT18	FT27	BT18	XT10	FT66	BT10	FT65	FT67	IT16	IT11	BT11	IT16	IT11	BT11	AT10		FT66	FT66	BT11	AT24	FT67	FT65	LT21	BT11	XT10	LT20	BT11	BT15
C	FT26	FT26	FT18	FT18	XT10	IT11	LT13	LT13	FT66	IT11		BT11	LT13	AT11 (4B)	IT11	IT11	IT11	XT10	AT12	LT26	AT13	IT11	BT17	IT11	XT10	FT66	BT25 (BS)	IT15 (BS)	FT66	LT13	IT16	IT11
D	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	XT10	LT20 (BS)	LT20 (BS)	IT16			LT13	XT10	AT11 (BS)	HT15	DT11	HT15	DT14	DT14 (ABS)	FT10	FT66 (ABS)	AT11
	2	2	2	2	2	1	1	1	1	1																						

IOP#	S1-1	S2-1	S3-1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

FOR: LASTONE → S1-2 UP
FOURBYTE → S2-2 UP
AIOP → S3-2 UP



1 : 8 Additional Channels. Channel 8 → 15

2 : 8 Additional Channels Channel 16 → 23

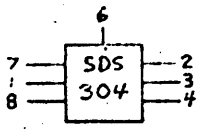
4B : 4 Byte Option.

BS : Memory Buss Sharing Option.

ABS : Buss Sharing Option In AIOP Only.

FT25 (18D)

32-BIT MIOP
8273/8473



(CA) - LSO = COMMAND ADDRESS

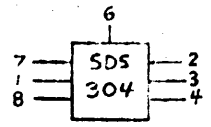
(BA) - NLSO = BYTE ADDRESS

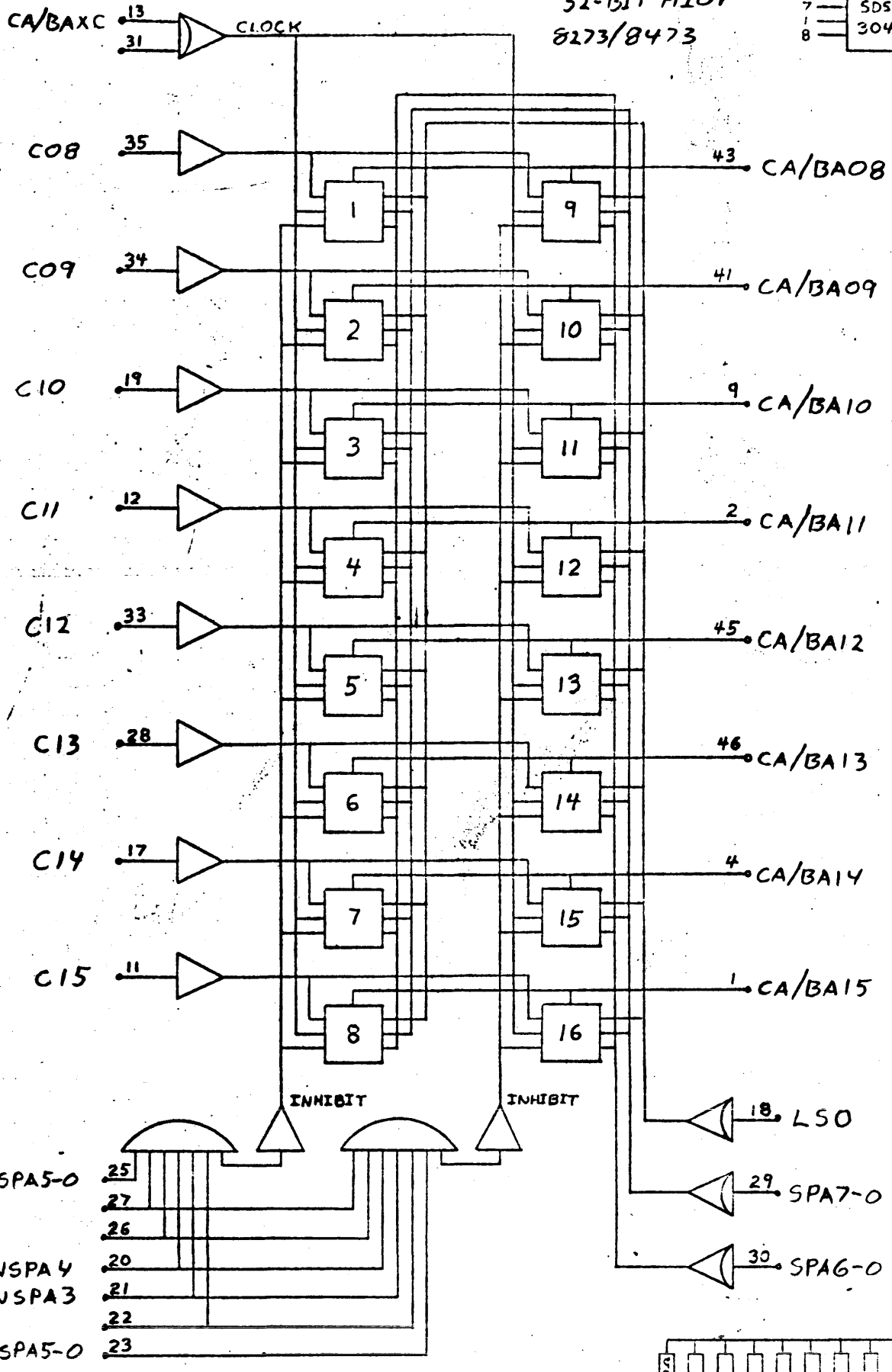
Σ5/7 32-BIT MIOP

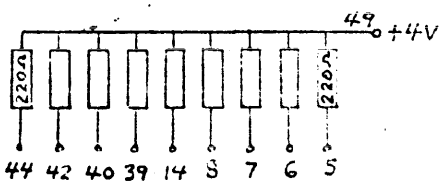
(18D)

FT25 (19D)

32-BIT MIOP
8273/8473







(CA)- LSO=COMMAND ADDRESS

(BA)-NLSO=BYTE ADDRESS

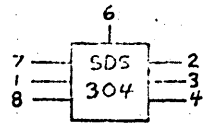
Σ5/7 32-BIT MIOP

(19D)

FT25 (20D)

32 BIT MIOP

8273/8473



FS/BCXC 13 31 CLOCK

CO0 35 — 1 9 — 43 FS/BCO0 — DC: FS = DATA CHAINING; BC = MSB BYTE CT.

CO1 34 — 2 10 — 41 FS/BCO1 — IZC: FS = INT. ZERO BC

CO2 19 — 3 11 — 9 FS/BCO2 — CC: FS = COMM. CHAINING

CO3 12 — 4 12 — 2 FS/BCO3 — ICE: FS = INT. CHAN. END

CO4 33 — 5 13 — 45 FS/BCO4 — HTE: FS = HALT TRANS. ERR.

CO5 28 — 6 14 — 46 FS/BCO5 — IUE: FS = INT. UNUSUAL END

CO6 17 — 7 15 — 4 FS/BCO6 — SIL: FS = SUPPRESS INCORRECT LENGTH

CO7 11 — 8 16 — 1 FS/BCO7 — FS = SKIP

INHIBIT INHIBIT

18 LS1

29 SPA7-0

30 SPA6-0

SPA5-0 25 27 26

NSPA4 20

NSPA3 21

22

NSPA5-0 23

49 +4V

220Ω

44 42 40 39 14 8 7 6 5

(FS) - LS1 = FLAGS & STATUS

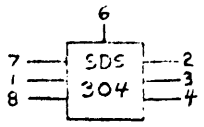
(BC) - NLS1 = BYTE COUNT

Σ5/7 32-BIT MIOP

FT25 (21D)

32-BIT MIOP

8273/8473



Σ5/7 32-BIT MIOP

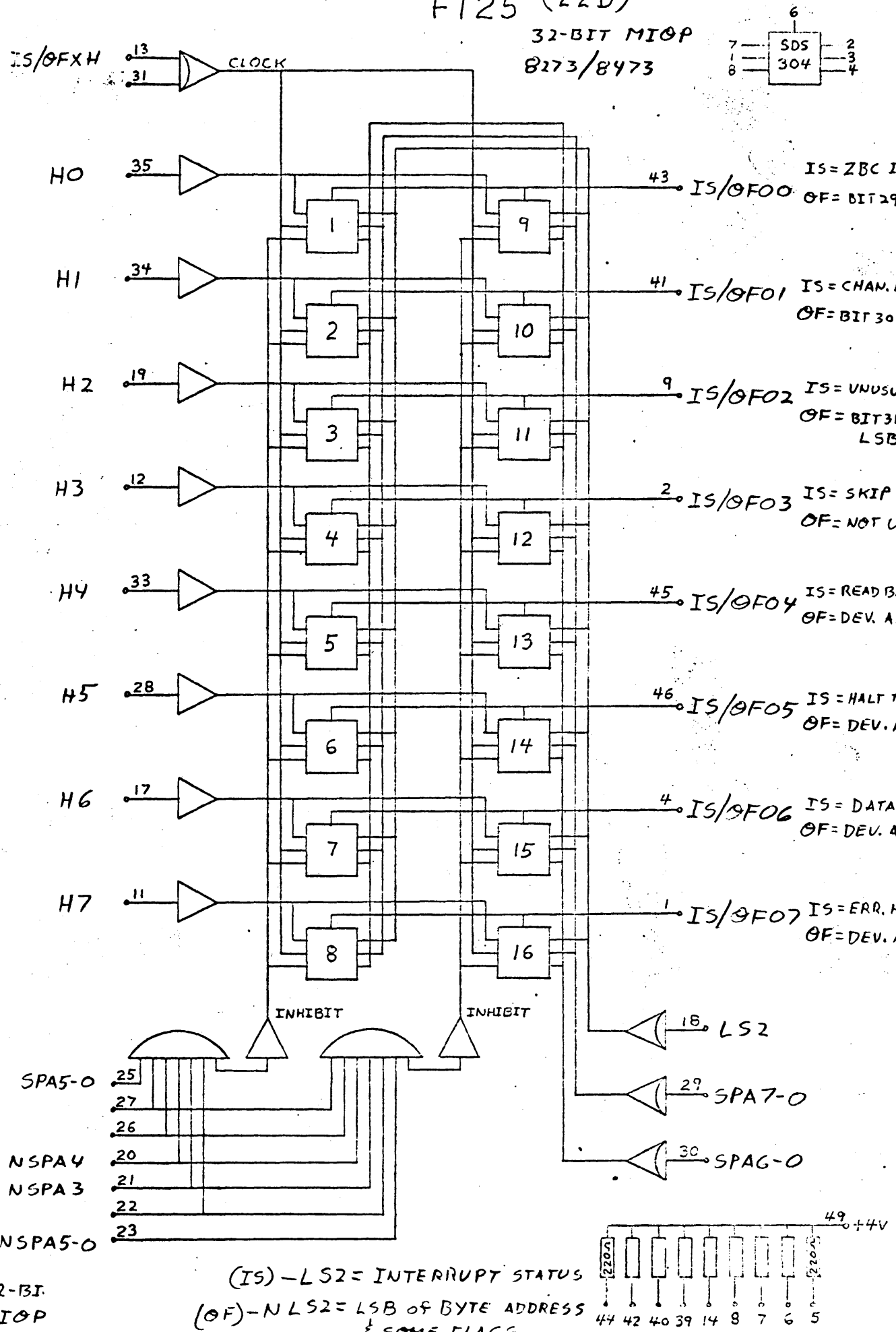
(FS)- LS1=FLAGS & STATUS

(BC)-NLS1= BYTE COUNT

(21D)

FT25 (22D)

32-BIT MIOP
8273/8473



32-BIT MIOP

(IS) – LS2 = INTERRUPT STATUS

(OF) – NLS2 = LSB of BYTE ADDRESS & SOME FLAGS

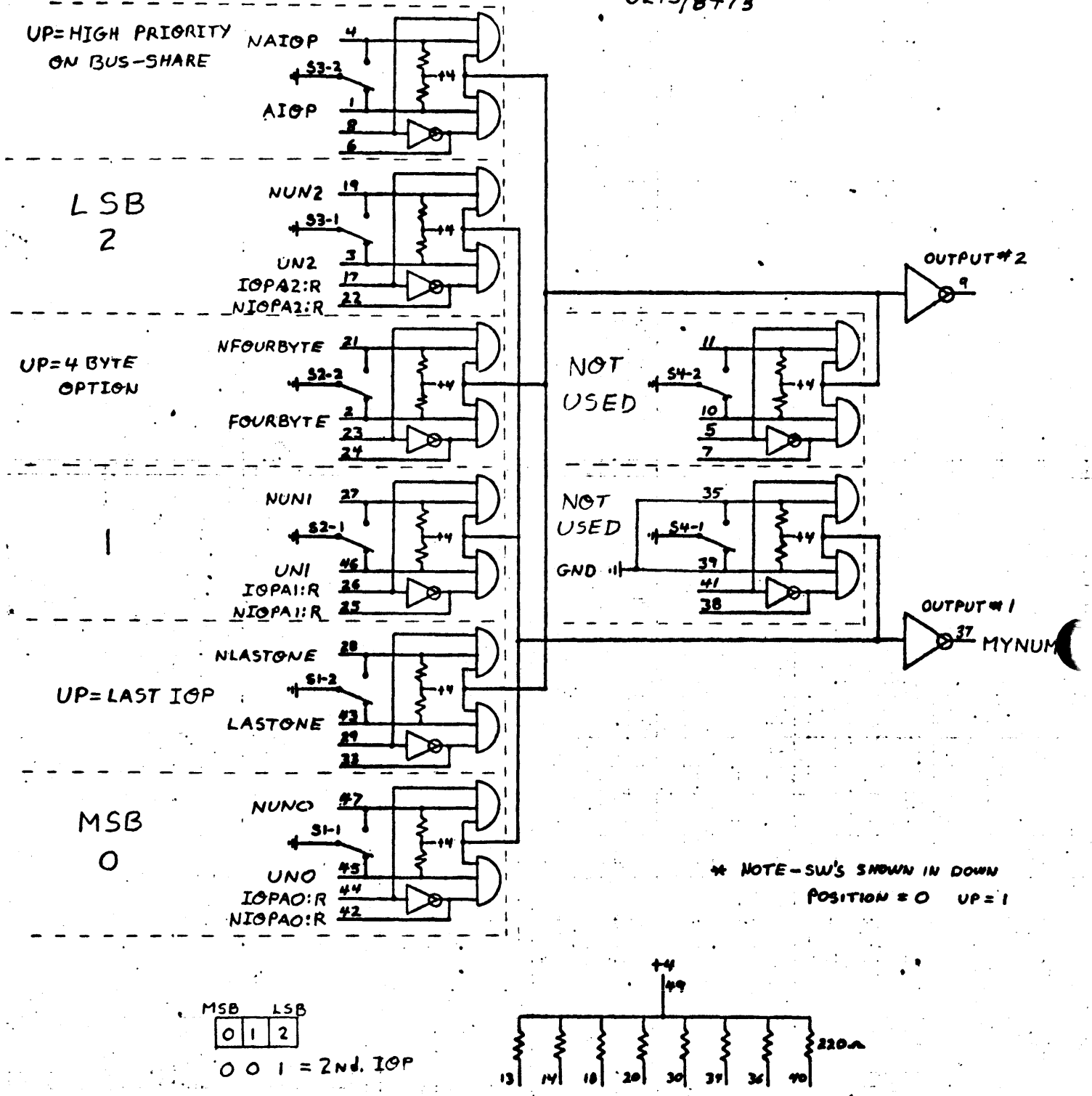
(22D)

LT26 SWITCH MODULE

COCHRANE

32-BIT MIOP (13C)

8273/8473

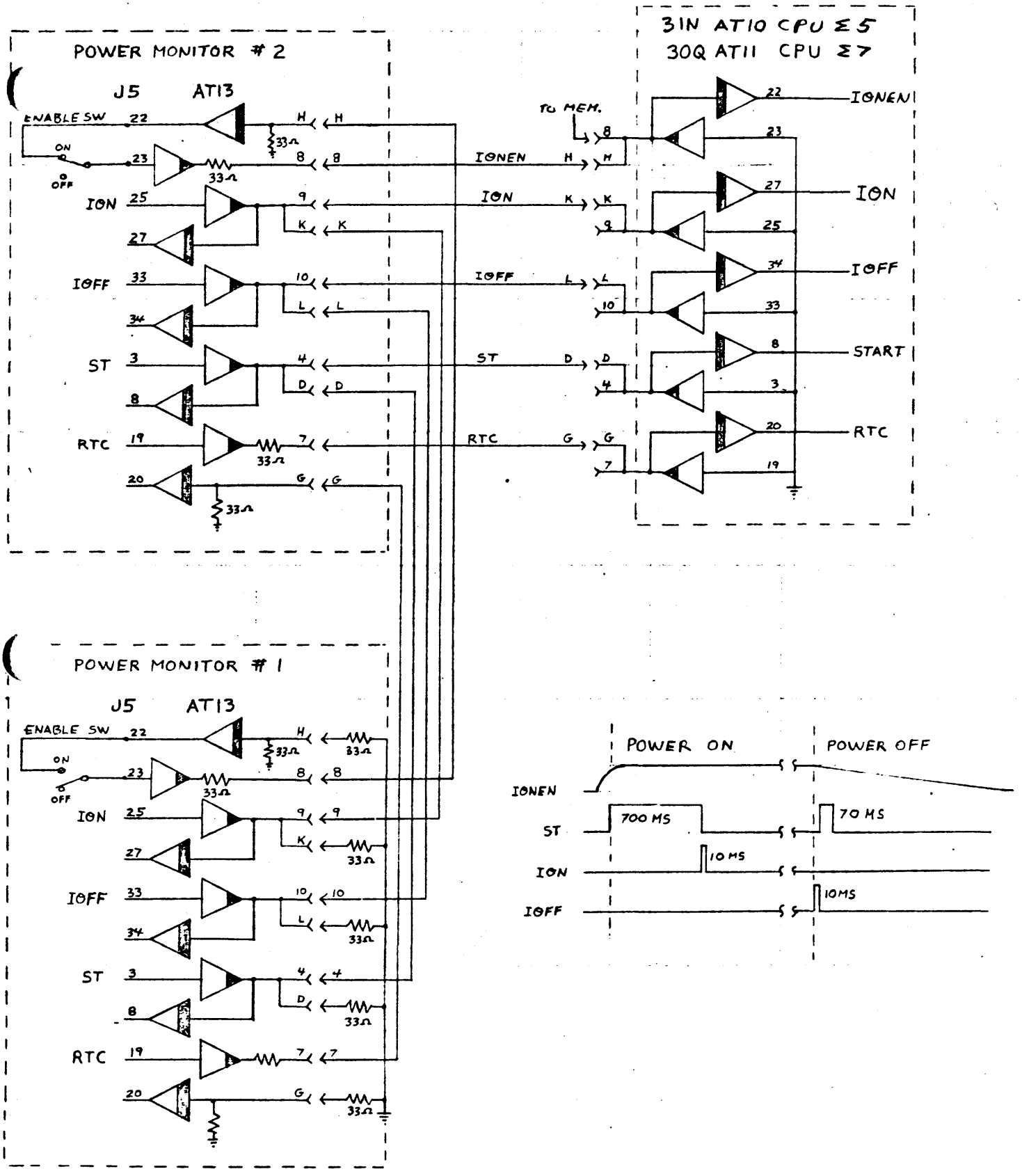


(13C)

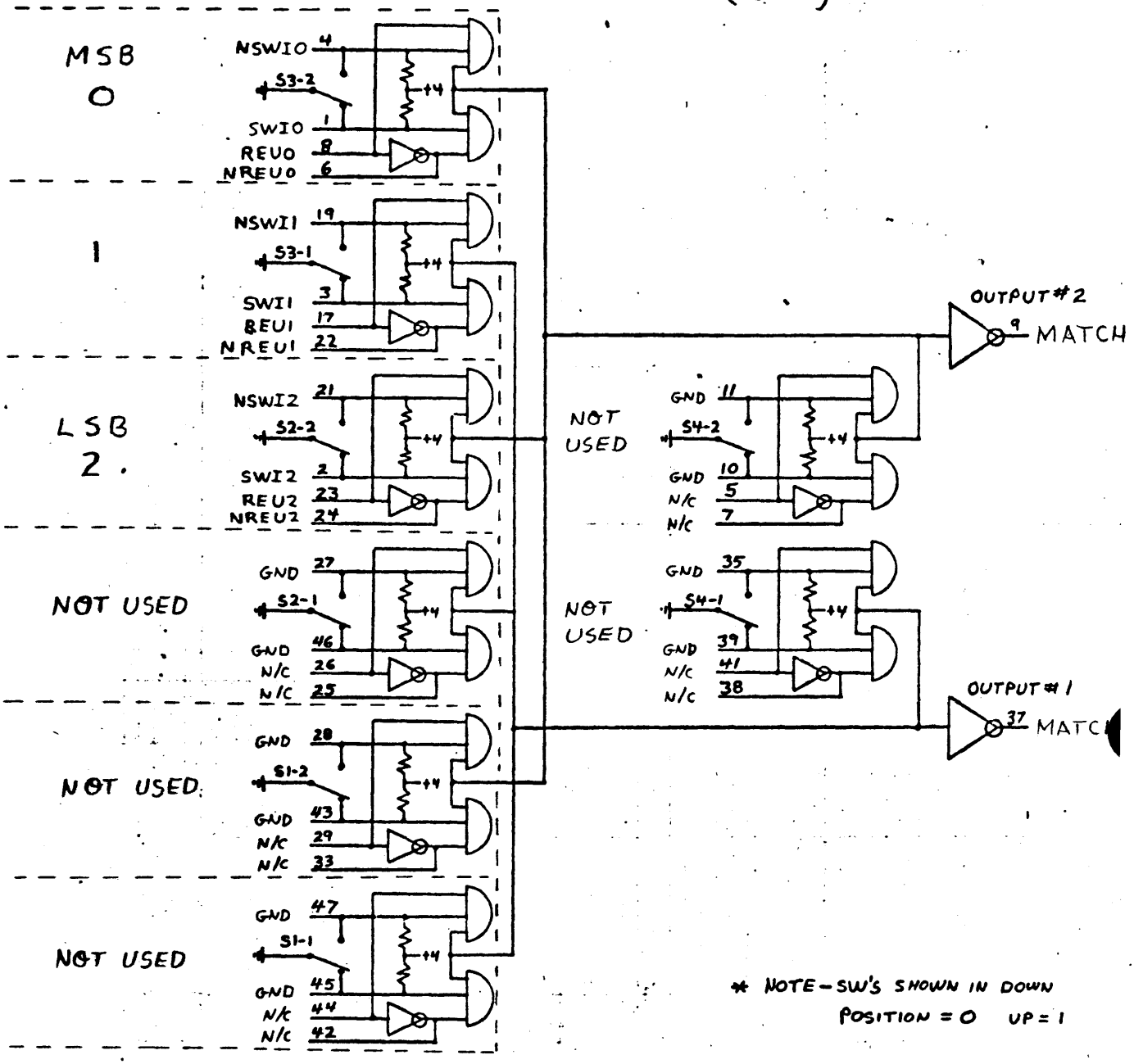
32-BIT MIOP

D. COCHRANE

POWER MONITOR INTERFACE Σ7/5



LT26 SWITCH MODULE
Σ5/7 REGISTER EXTENSION UNIT
(32A)



* NOTE - SW'S SHOWN IN DOWN POSITION = 0 UP = 1

Σ5/7 REGISTER EXTENSION UNIT
(32A)

Σ5/7 CFE WITH 1 MA SECTION (=2 MA UNITS)

'69 CHRANE

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	ZT 23	AT 23	XT 10	AT 23	ZT 23	AT 23	ZT 23	AT 23	ZT 23	AT 23	ZT 23	AT 23	ZT 23	AT 23	AT 23	ZT 23	AT 23	DT 14	HT 15	DT 14	HT 15	DT 14	LT 29	LT 29	LT 29	FT 22	GT 11	FT 22	XT 10	LT 26			A
B	AT 11 M00 ↓ M13		AT 11 M14 ↓ M27	BT 16	AT 11 M28 ↓ M31	BT 16	AT 11 NREQ	XT 10	AT 12 L15 ↓ L28	FT 22	FT 22		IT 14	IT 14	FT 12	FT 12	FT 12		FT 12	IT 16	LT 13		LT 21	BT 16	FT 26	FT 26	FT 22		FT 22	BT 16			B
C	ZT 46 31A/1	ZT 46 /2	FT 22	FT 22	PET	PET	XT 10	FT 41	LT 17	LT 17	FT 41		LT 18	FT 41	LT 17	LT 17	FT 41		FT 39	FT 39	FT 39		FT 26	IT 16	FT 26	BT 16	BT 16		FT 18	FT 18	FT 18	XT 10	C
D	ZT 23	IT 16	AT 11	FT 22	AT 11	LT 13	FT 41	LT 17	LT 17	FT 41	XT 10	LT 18	FT 41	LT 17	LT 17	FT 41	BT 10	IT 16	BT 16	LT 18	XT 10	GT 11	FT 22	FT 18	LT 18	IT 25	FT 26	LT 18	IT 25	FT 26	XT 10	BT 11	D
E			BT 11	AT 11	IT 14	AT 10	BT 16	AT 11	FT 22	XT 10	FT 22	FT 22	IT 16	BT 11		BT 16	IT 16	LT 13	BT 10	XT 10	LT 13	IT 25	IT 25	BT 11	IT 16	IT 25		IT 16	LT 13	XT 10	FT 22	FT 18	E
A			ZT 23		FT 41	LT 17	FT 17	FT 41	LT 17	XT 10		LT 17	FT 41	LT 18	FT 17	LT 17	FT 41	FT 17	LT 17	XT 10	LT 17	FT 41	FT 17	LT 17	FT 41	LT 18	XT 10	LT 17	FT 41	FT 17	LT 17	FT 41	A
B					FT 41	FT 41	BT 16			IT 16	BT 16	BT 16	BT 16	XT 10	IT 16	FT 41	BT 16	FT 41	FT 41	LT 18	XT 10	BT 16	FT 41								XT 10		B
C	ZT 46 32A/1		XT 10		FT 41	LT 17	FT 17	FT 41	LT 17	XT 10		LT 17	FT 41	LT 18	FT 17	LT 17	FT 41	FT 17	LT 17	XT 10	LT 17	FT 41	FT 17	LT 17	FT 41	LT 18	XT 10	LT 17	FT 41	FT 17	LT 17	FT 41	C

1= TO 1ST MULT/ADD FRAME MA2 THRU MA4

2= TO 2nd MULT/ADD FRAME MA5 THRU MA7

Σ 5/7 SIOP (without MS) 8285/8485

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	DT 14	HT 15	BT 22	FT 24	IT 26	LT 13	XT 10	BT 10	XT 10	AT 24	FT 37	IT 13	BT 16	FT 38	FT 38	FT 38	FT 38	AT 16 1,2	BT 10 1	LT 20 1	IT 16 1	AT 11 1	IT 25	LT 21		XT 10	LT 13	LT 13	FT 37	BT 18	BT 15	IT 18	A
B	AT 16	IT 25	IT 24	BT 22	IT 25	LT 21	FT 26	BT 16	IT 16	FT 39	FT 39	FT 27	FT 39	FT 26	FT 39	XT 10	LT 13	IT 16	IT 15	IT 11	IT 11	IT 11	BT 18	FT 37	XT 10	XT 10	IT 15	FT 37	IT 16	FT 37	LT 13	IT 25	B
C	FT 18	FT 18	LT 13	FT 27	XT 10		IT 15	IT 25	BT 25	XT 10		BT 10	BT 25	IT 16	IT 25		BT 10	BT 10	LT 21	BT 15		BT 18	IT 18	LT 13	XT 10		LT 29	DT 14	HT 15	BT 16		BT 22	C
D	BT 11	FT 18	FT 18	FT 18	FT 18		FT 38	FT 38	FT 38	FT 38		FT 38	AT 11	FT 38	AT 11		FT 38	AT 11	FT 38	AT 11		AT 12	FT 37	FT 37	LT 21		XT 10	DT 11	HT 15	BT 15		BT 22	D
E	GT 11	FT 18	FT 18	BT 11	FT 18	FT 18	FT 18	FT 18	FT 18	XT 10	FT 38	AT 11	FT 37	AT 11	FT 37	AT 11	BT 16	XT 10	AT 10	BT 18	BT 25	AT 12	LT 21	AT 11	LT 21	XT 10		FT 24	FT 37	LT 20	BT 10	LT 21	E
F			BT 22	BT 16	XT 10	BT 11	BT 15	FT 18	FT 18	GT 11	BT 22	BT 10	FT 22	BT 24	IT 16	LT 65	IT 15	IT 25	BT 18	IT 16	IT 25	BT 16	AT 13	LT 64	LT 26	XT 10	IT 16	IT 25					F
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

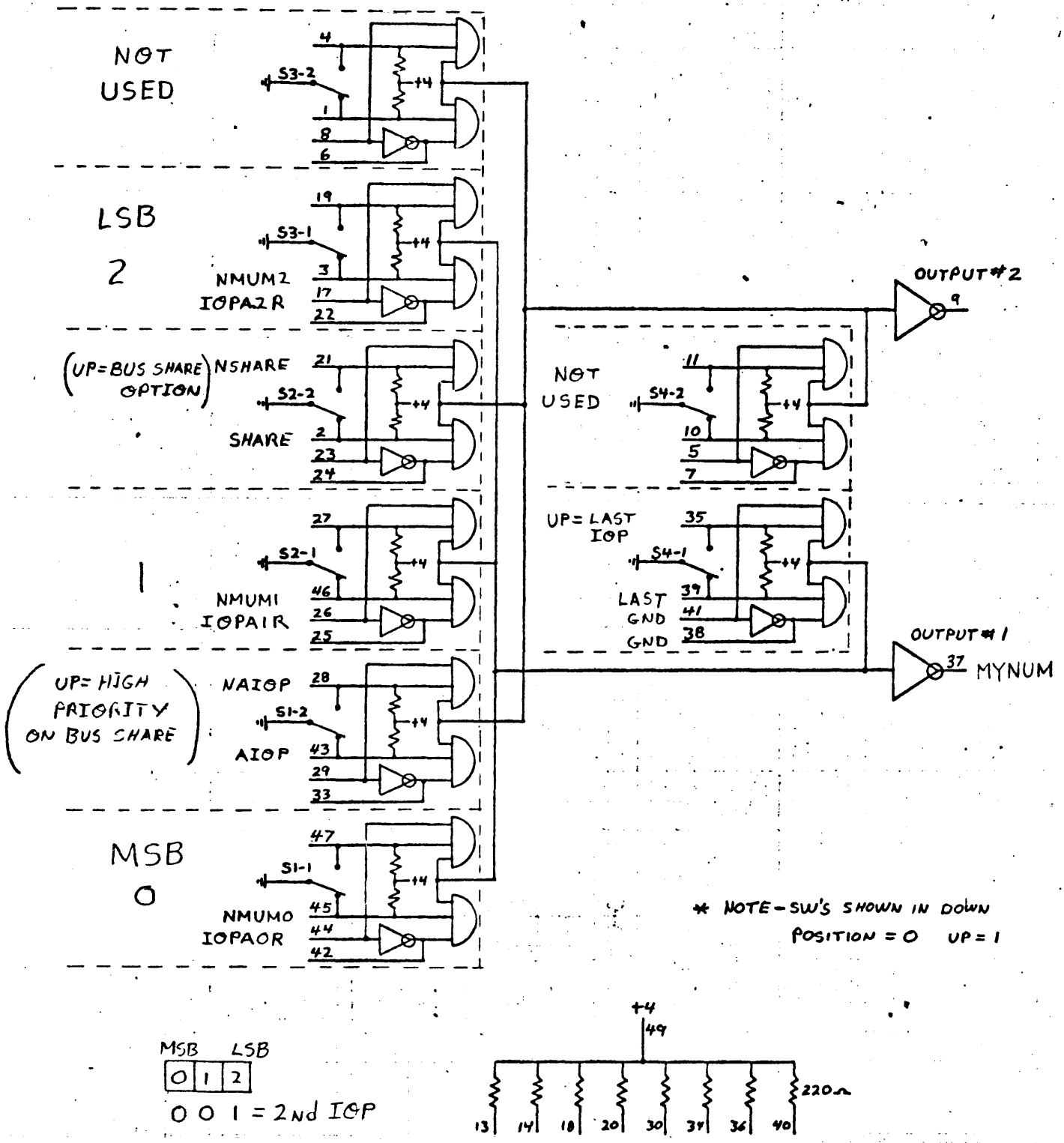
1 = BUSS SHARING OPTION

2 = ATIG USED IN 1st. SIOP ONLY

4/30/69

LT26 SWITCH MODULE (8F) SIOP

COCHRANE



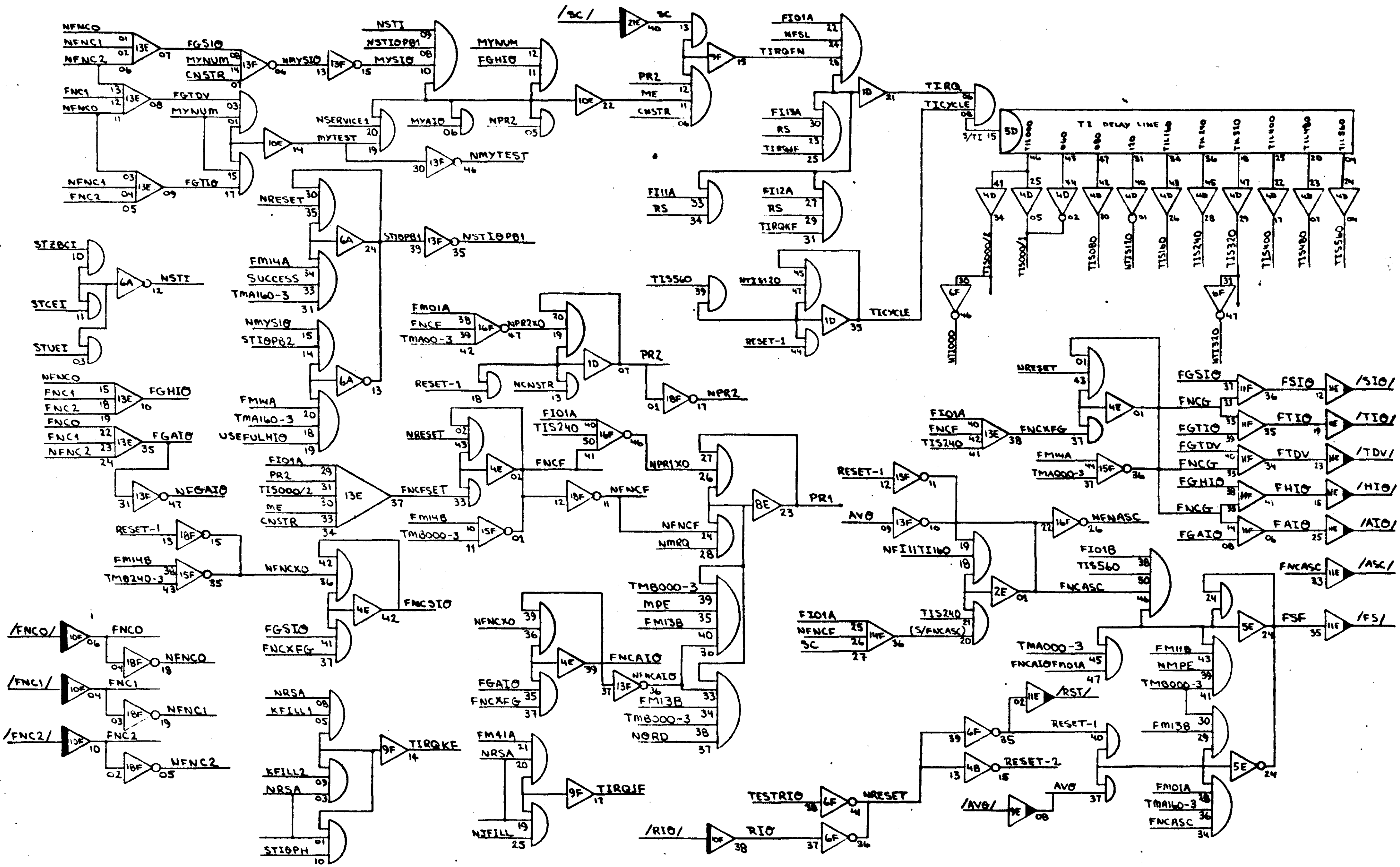
(8F) SIOP

SIOP LOGIC TERM INDEX

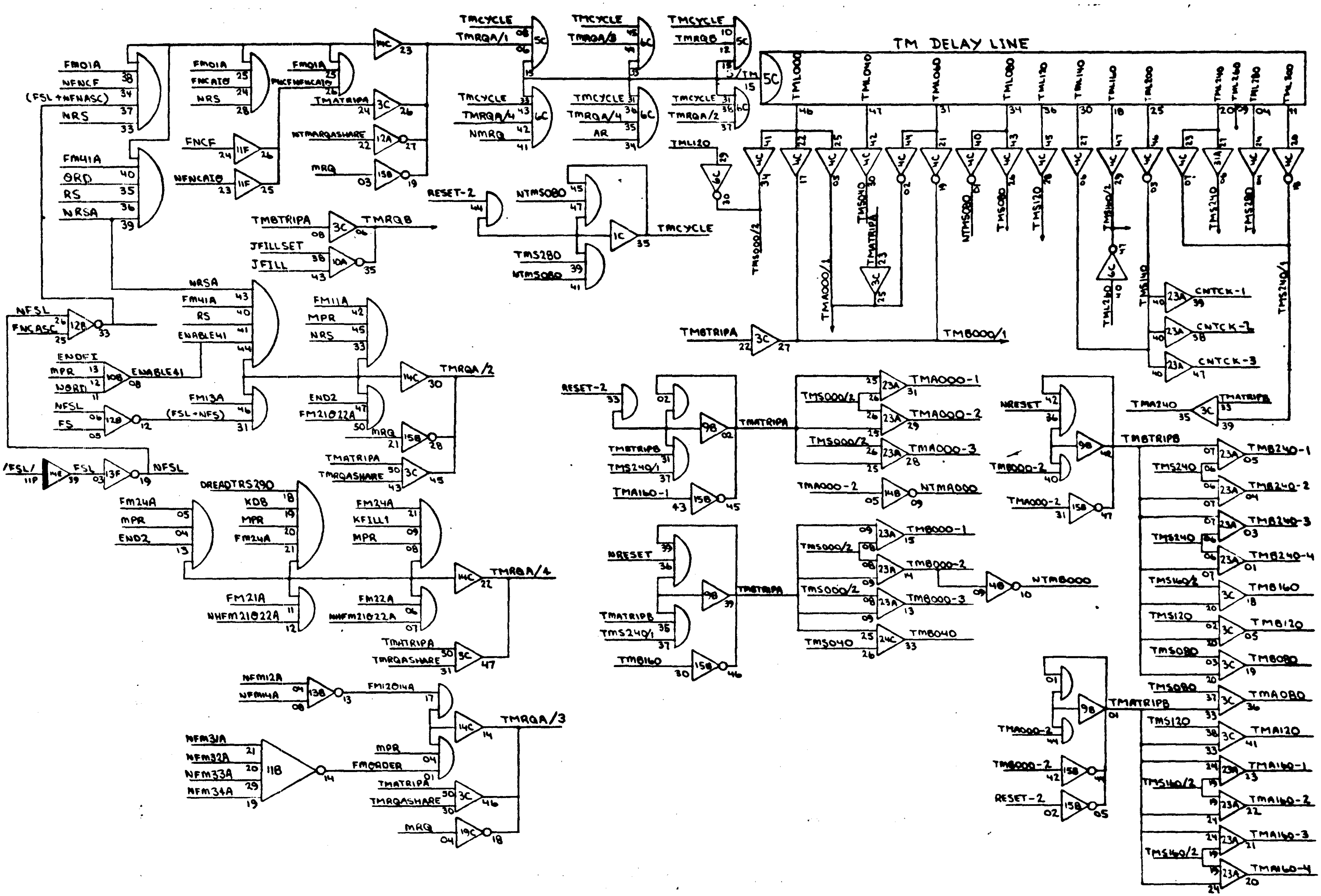
* BUSS SHARE

SIOP LOGIC TERM INDEX(Cont)

* BUSS SHARE



SIOP REV L
Eric Salomas
②



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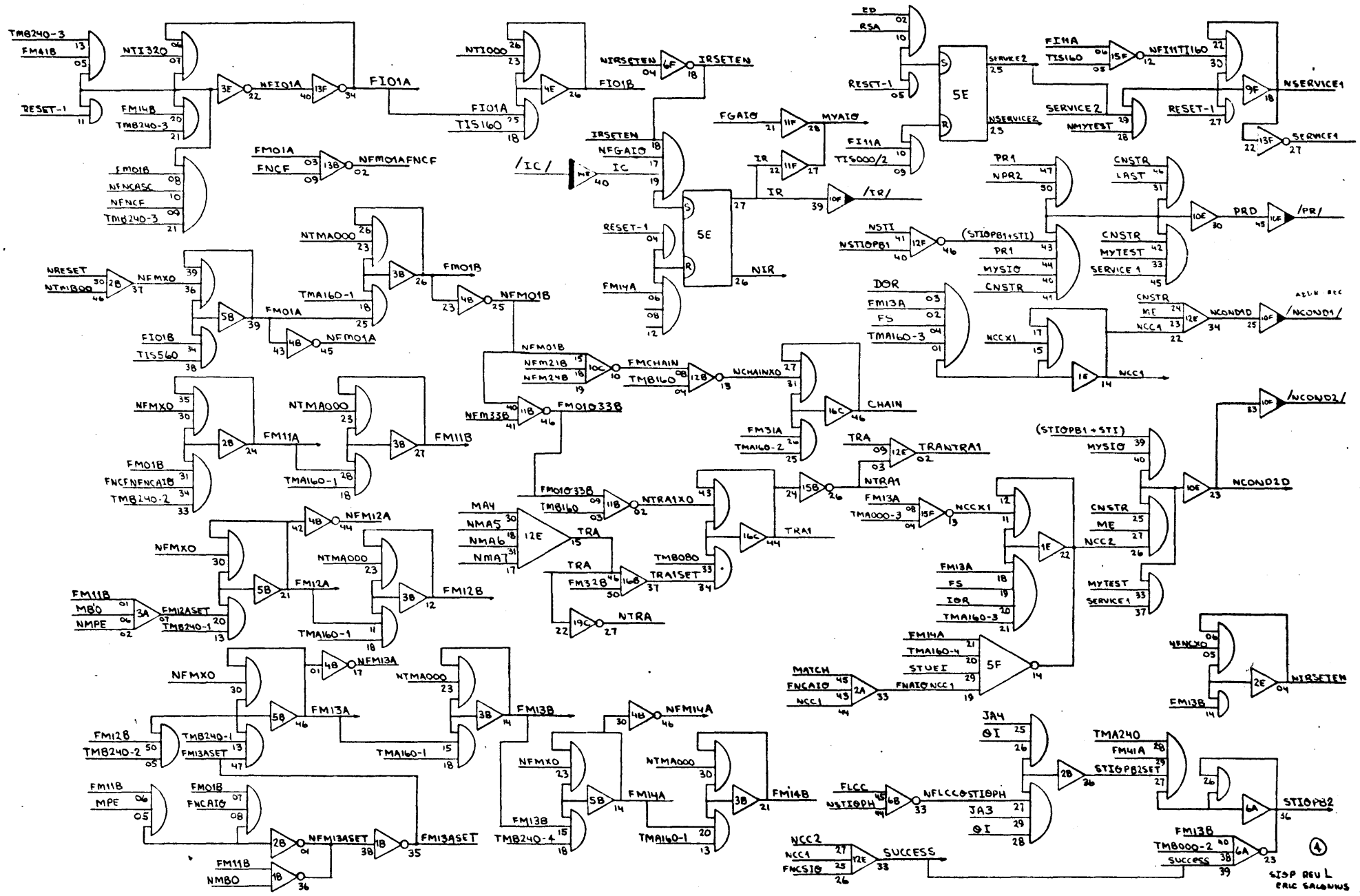
S10P REV L
(3)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RESET-1
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FM14B
TMB240-3
3E
NFIO1A
13F
FIO1A
NTI000
FIO1A
TIS160
4E
FIO1B
NIRSETEN
6F
IRSETEN
FM01A
FNCF
13B
NFM01AFNCF
FM01B
NFNCASC
NFNCF
TMB240-3
/IC/
IC
IRSETEN
NFGAIO
FGAIO
11F
MYAIO
IR
11F
IR
10F
/IR/
RESET-1
FM14A
5E
NIR
ED
RSA
RESET-1
5E
SERVICE2
NSERVICE2
FI11A
TIS000/2
FI11A
TIS160
15F
NFI11TI160
9F
NSERVICE1
SERVICE2
NMYTEST
RESET-1
13F
SERVICE1
PR1
NPR2
CNSTR
LAST
10E
PRD
10F
/PR/
NSTI
NSTIOPB1
12F
(STIOPB1+STI)
PR1
MYSIO
CNSTR
CNSTR
MYTEST
SERVICE1
DOR
FM13A
FS
TMA160-3
NCCX1
16
NCC1
CNSTR
ME
NCC1
12F
NCOND1D
10F
/NCOND1/
NRESET
NTMI800
2B
NFMXO
NTMA000
3B
FM01B
TMA160-1
5B
FM01A
4B
NFM01A
FIO1B
TIS560
NFM01B
NFM21B
NFM24B
10C
FMCHAIN
TMB160
12B
NCHAINXO
FM01033B
NFM33B
11B
16C
CHAIN
FM31A
TMA160-2
NFMXO
NTMA000
2B
FM11A
3B
FM11B
TMA160-1
FM01B
FNCFNFNCAIB
TMB240-2
TRA
12E
TRANTRA1
NTRA1
15B
NCCX1
(STIOPB1+STI)
MYSIO
10E
NCOND2D
/NCOND2/
FM01033B
TMB160
11B
NTRA1XO
MA4
NMA5
NMA6
NMA7
12E
TRA
TRA
TRA1SET
TMB080
16C
TRA1
TRA
FM32B
16B
NTRA
CNSTR
ME
NCC2
MYTEST
SERVICE1
NFM12A
4B
NFMXO
NTMA000
FM11B
MBO
NMPE
3A
FM12ASET
TMB240-1
5B
FM12A
3B
FM12B
TMA160-1
FM13A
FS
IOR
TMA160-3
1E
NFMXO
FM14A
TMA160-4
5F
STUEI
MATCH
FNCAIO
NCC1
2A
FNAIONCC1
NFMXO
FM13B
2E
NIRSETEN
NFM13A
4B
NTMA000
3B
FM13B
NFMXO
5B
FM13A
FM12B
TMB240-2
TMB240-1
FM13ASET
TMA160-1
NFM14A
4B
NFMXO
NTMA000
FM13B
TMB240-4
5B
FM14A
TMA160-1
3B
FM14B
JA4
OI
JA3
OI
TMA240
FM41A
STIOPB2SET
FLCC
NSTIOPH
6B
NFLCCOSTIOPH
NCC2
NCC1
FNCSIO
12E
SUCCESS
FM11B
MPE
FM01B
FNCAIO
2B
NFM13ASET
1B
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FM11B
NMBO
1B
STIOPB2
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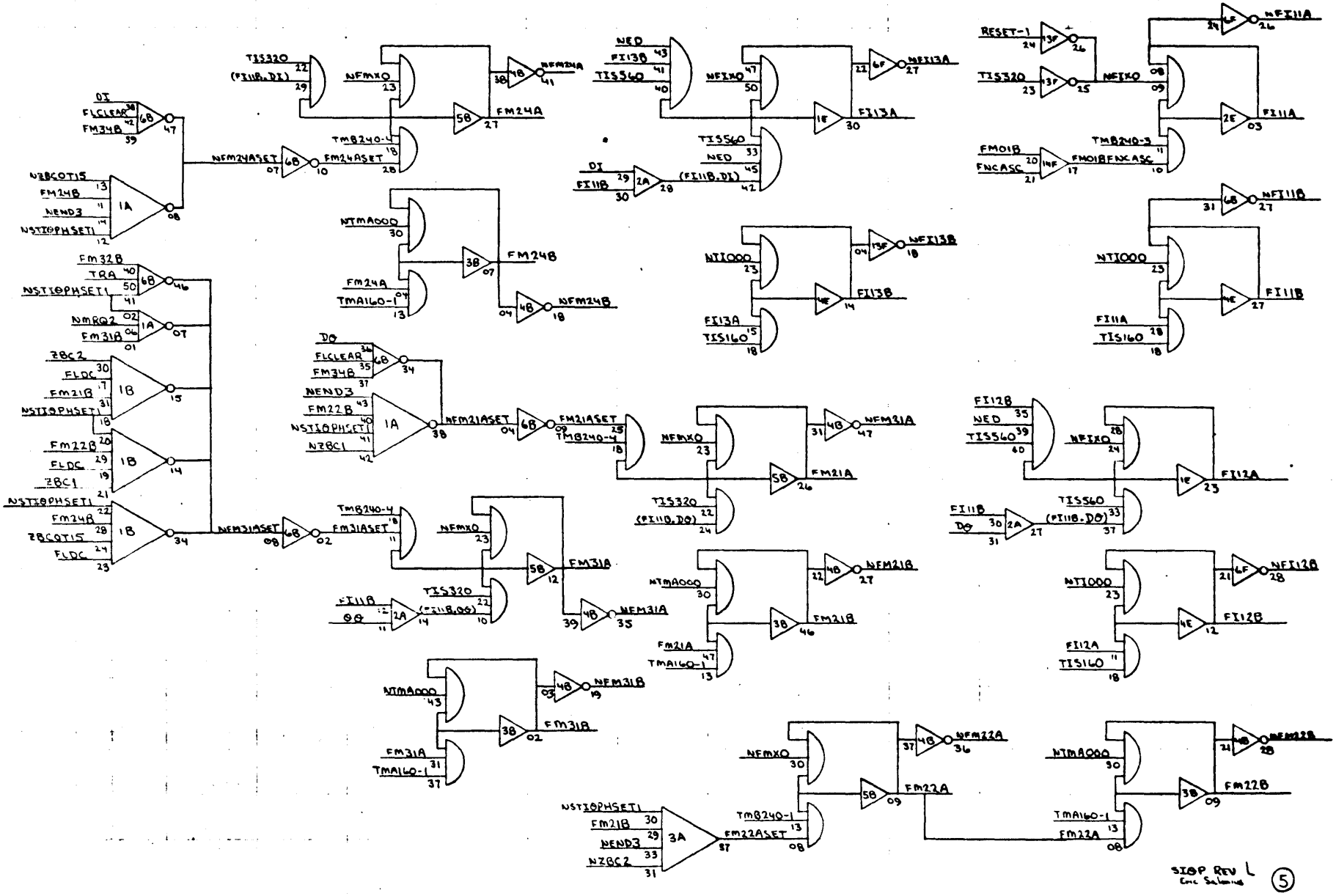
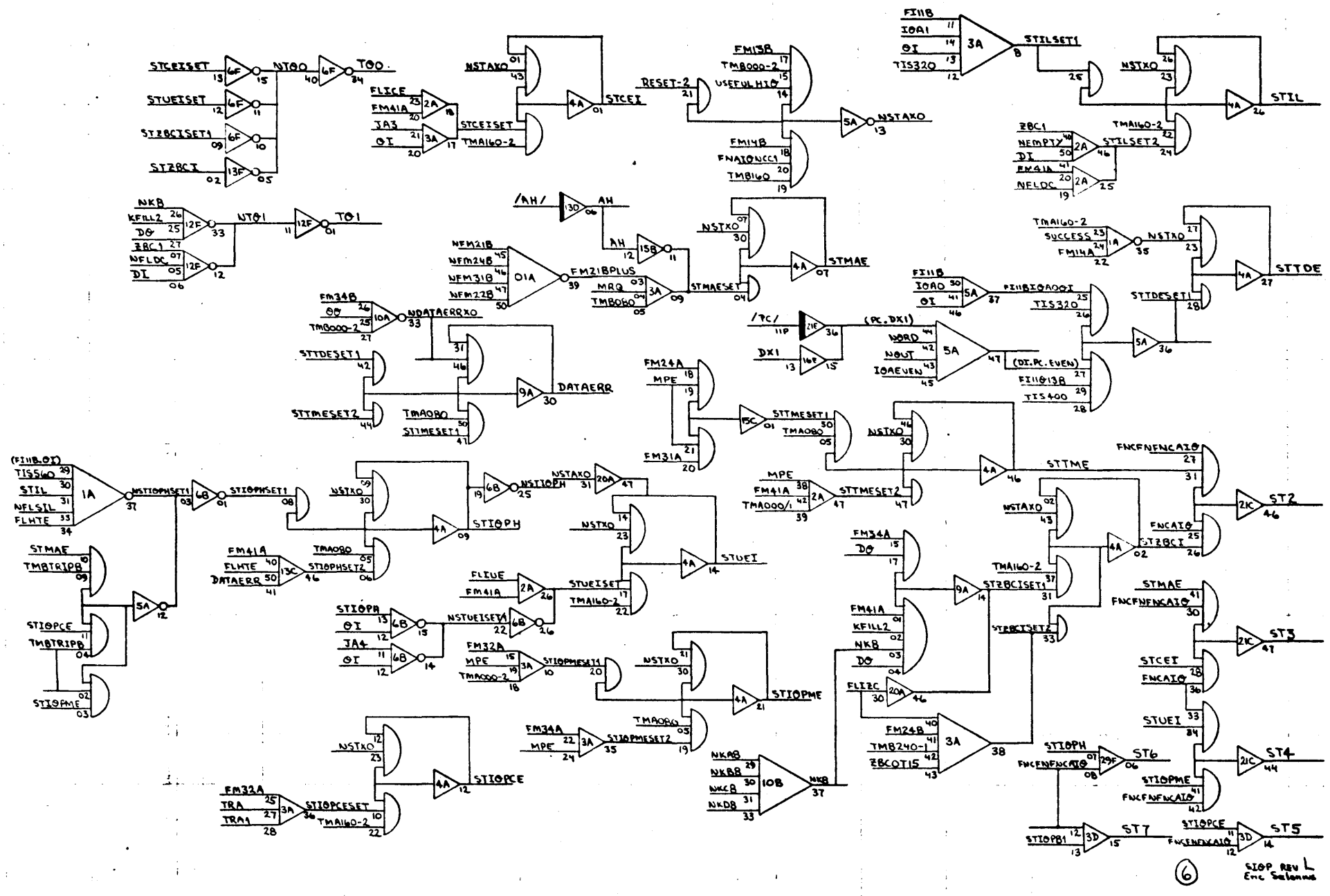
TMB000-2
6A
SUCCESS
4
SISP REV L
ERIC SALOMUS



SIOP Rev L
Eric Salmins

⑤



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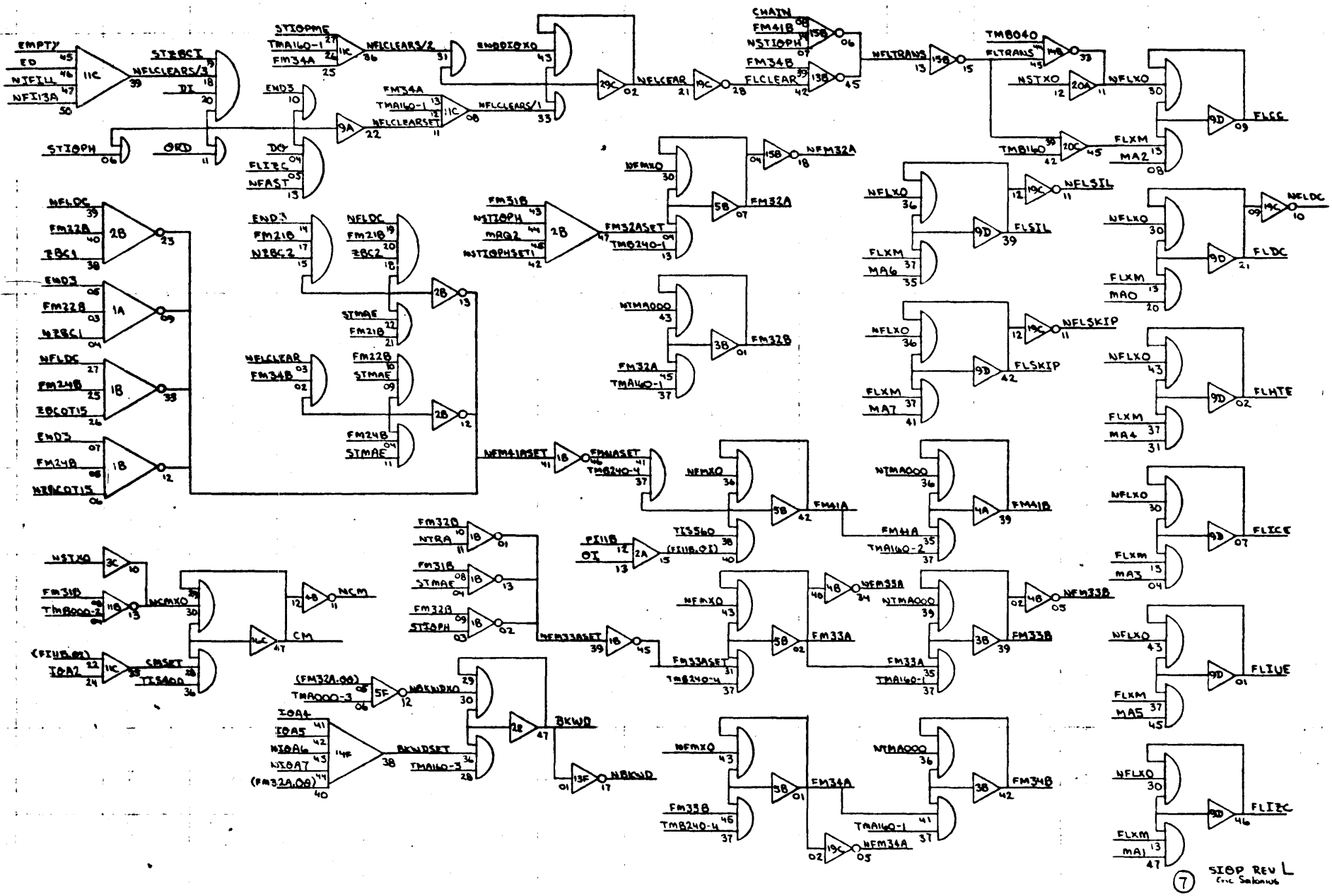
SIOP REV L
Eric Solomon


EMPTY
ED
NJFILL
NFI13A
STRBCI
NFLCLEARS/3
DI
STIOPH
ORD
DCY
FLIIC
NFAST
END3
NFLCLEARS/2
STIOPME
TMA140-1
FM34A
NFLCLEAR
NFLCLEARSET
NFLCLEARS/1
ENDDIOXO
FM34A
TMA140-1
CHAIN
FM41B
NSTIOPH
FM34B
FLCLEAR
NFLTRANS
TMB040
FLTRANS
NSTXO
NFLXO
FLCC
FLXM
MA2
TMB140
NFLDC
FM22A
FM21B
FM24B
FM22B
NFM32A
NFMXO
FM32A
FM31B
NSTIOPH
MAQ2
NSTIOPHSET1
FM32ASET
TMB240-1
NFLSIL
FLSIL
MA6
NFLDC
FLDC
MAO
NTMA000
FM32B
FM32A
TMA140-1
NFLSKIP
FLSKIP
MA7
NFLXO
FLHTE
MA4
NFM41ASET
FM41ASET
TMB240-4
FM41A
FM41B
TMA140-2
NTMA000
FLICE
MA3
FM32B
NTRA
FM31B
STMAE
FM33BSET
FI11B
OI
TI3540
(FI11B,OI)
NFM33A
FM33A
FM33ASET
NFM33B
FM33B
NSTXO
FM31B
TMB000-2
NCMXO
CM
(FI11B,OI)
IOA2
CMSET
TI3540
(FM32A,00)
TMA000-3
NBKWDXO
IOA4
IOA5
NIOA6
NIOA7
(FM32A,00)
BKWDSET
TMA140-3
BKWD
NBKWD
FLIUE
MA5
NFMXO
FM34A
FM33B
TMB240-4
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NTMA000
FM34B
FLITC
MA1
SIOP REV L
Eric Salonius
7
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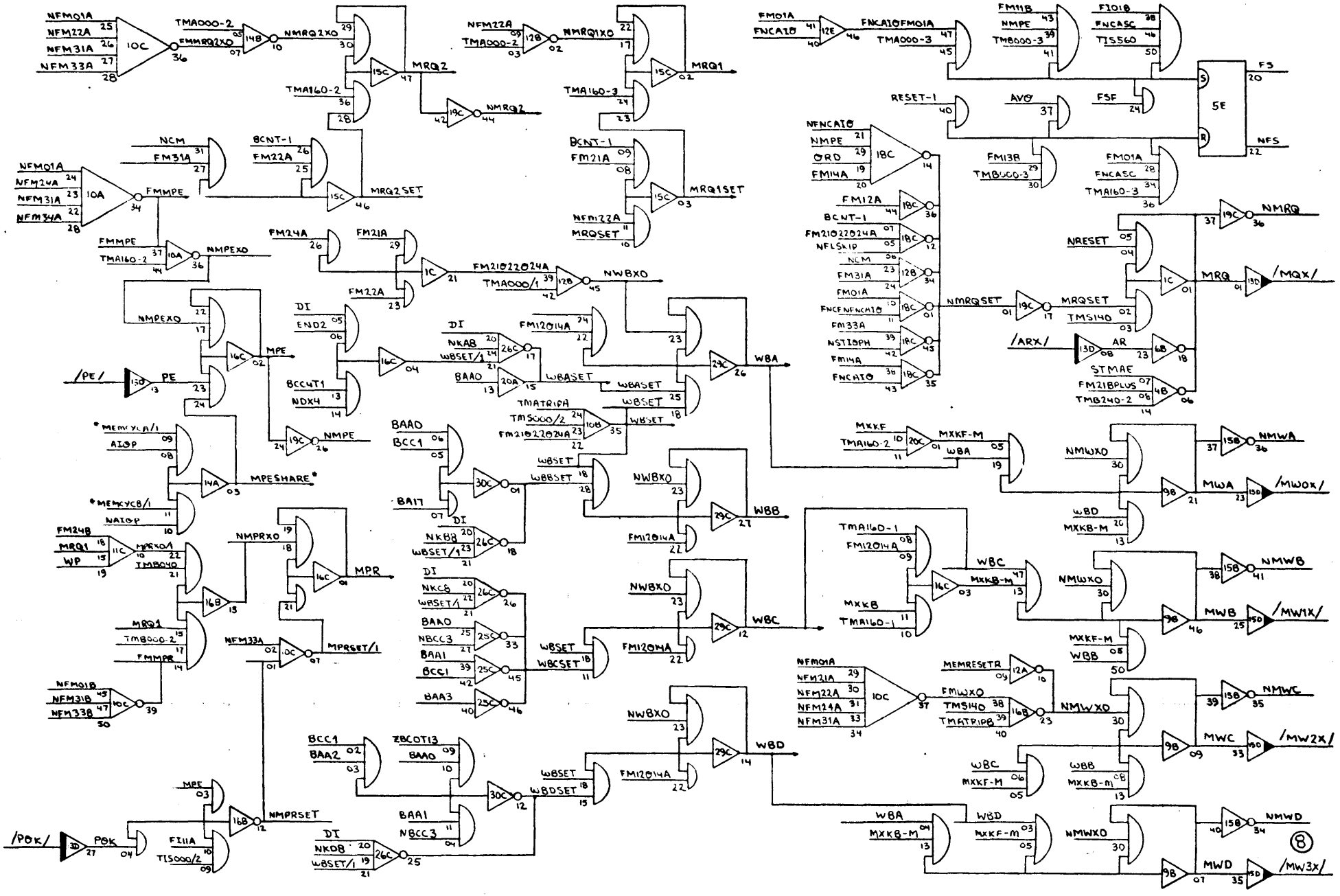
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NFM31A
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TMA000-2
EMMRQ2XO
14B
NMRQ2XO
MRQ2
15C
TMA160-2
19C
NMRQ2
NFM22A
TMA000-2
12B
NMRQ1XO
MRQ1
TMA160-3
FM01A
FNCA10
12E
FNCA10FM01A
TMA000-3
FM11B
NMPE
TMB000-3
F101B
FNCASC
TIS560
5E
FS
NFS
RESET-1
AV0
FSF
NCM
FM31A
BCNT-1
FM22A
MRQ2SET
FM01A
NFM24A
NFM31A
NFM34A
10A
FMMPE
NMPEXO
TMA160-2
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FM21A
1C
FM210220224A
TMA000/1
12B
NWBXO
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BCNT-1
FM21A
MRQ1SET
NFENCA10
NMPE
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18C
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FM210220224A
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FM31A
FM01A
FNCENFNCM10
FM33A
NSTI0PH
FM14A
FNCA10
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MRQSET
TMS140
FM13B
TMB000-3
FM01A
FNCASC
TMA160-3
NMRQ
NRESET
MRQ
/MQX/
/ARX/
AR
STMAE
FM21BPLUS
TMB240-2
NMPEXO
DI
END2
BCC4T1
NDX4
16C
MPE
/PE/
15D
PE
NMPE
DI
NKA8
WBSET/1
BAA0
20A
WBASET
FM12014A
WBASET
TMATRIPA
TMS000/2
FM210220224A
10B
WBSET
WBA
29C
MXKF
TMA160-2
20C
MXKF-M
WBA
NMWXO
NMWA
MWA
/MWOX/
WBD
MXKB-M
MEMCYCA/1
AIOP
14A
MPESHARE
MEMCYCB/1
NAIOP
BAA0
BCC1
30C
BAI7
NKB8
WBSET/1
26C
WBSET
WBBSET
NWBXO
WBB
FM12014A
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WBC
MXKB-M
16C
MXKB
TMA160-1
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MWB
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MXKF-M
WBB
FM24B
MRQ1
WP
11C
MPRXOA
TMB0040
NMPRXO
16C
MPR
NKC8
WBSET/1
BAA0
NBCC3
BAA1
BCC1
BAA3
25C
WBSET
WBCSET
NWBXO
FM12014A
WBC
NFM01A
NFM31A
NFM22A
NFM14A
NFM31A
10C
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12A
FMWXO
TMS140
TMATRIPB
16B
NMWXO
NMWC
MWC
/MW2X/
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MXKF-M
WBB
MXKB-M
MRQ1
TMB000-2
FMMPR
MPRSET/1
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10C
NFM01B
NFM31B
NFM33B
10C
MPE
16B
NMPRSET
/POK/
30
POK
FI11A
TIS000/2
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BAA2
ZBCOT13
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BAA1
NBCC3
30C
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WBDSET
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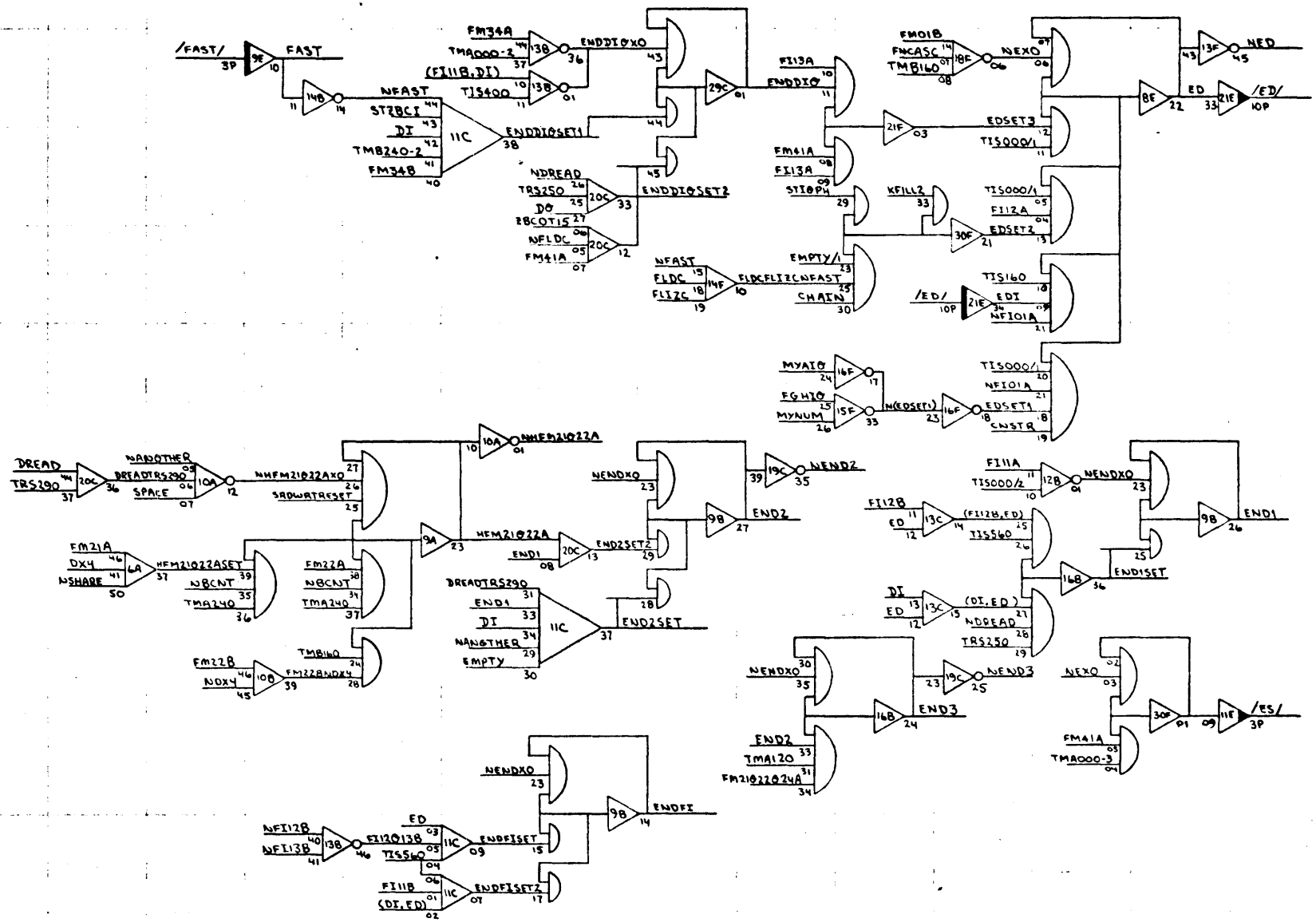
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3P
9E
FAST
14B
NFAST
ST2BCI
DI
TMB240-2
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11C
ENDDIOSET1
38
FM34A
TMA000-2
13B
ENDDIOXO
36
(FI11B,DI)
TIS400
43
29C
01
FI13A
ENDDIO
FM01B
FNCASC
TMB160
18F
NEXO
NED
13F
45
8E
ED
21E
/ED/
10P
21F
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TIS000/1
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TRS250
20C
33
DO
EBCOTI5
NFLDC
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FM41A
STIOP4
KFILL2
30F
EDSET2
TIS000/1
FI12A
EMPTY/1
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FLDC
FLIZC
14F
FLDCFLI2CNFAST
CHAIN
TIS160
EDI
NFI01A
MYAIO
16F
FGHIO
MYNUM
15F
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EDSET1
CNSTR
TIS000/1
NFI01A
DREAD
TRS290
WANOTHER
DREADTRS290
SPACE
10A
NWFM21022AXO
SRDWRTRESET
10A
NWFM21022A
NENDXO
END2
19C
WEND2
FM21A
DX4
WSHARE
5A
WFM21022ASET
WBCNT
TMA240
FM22A
WBCNT
TMA240
HFM21022A
END1
END2SET2
END2SET
DREADTRS290
END1
DI
WANOTHER
EMPTY
11C
FM22B
NDX4
10B
FM22BNDX4
TMB160
FI11A
TIS000/2
12B
NENDXO
END1
FI12B
ED
13C
(FI12B,ED)
TIS560
16B
END1SET
DI
ED
13C
(DI,ED)
NDREAD
TRS250
NENDXO
19C
WEND3
END3
END2
TMA120
FM21022024A
NEXO
FM41A
TMA000-3
30F
11E
/ES/
3P
NENDXO
98
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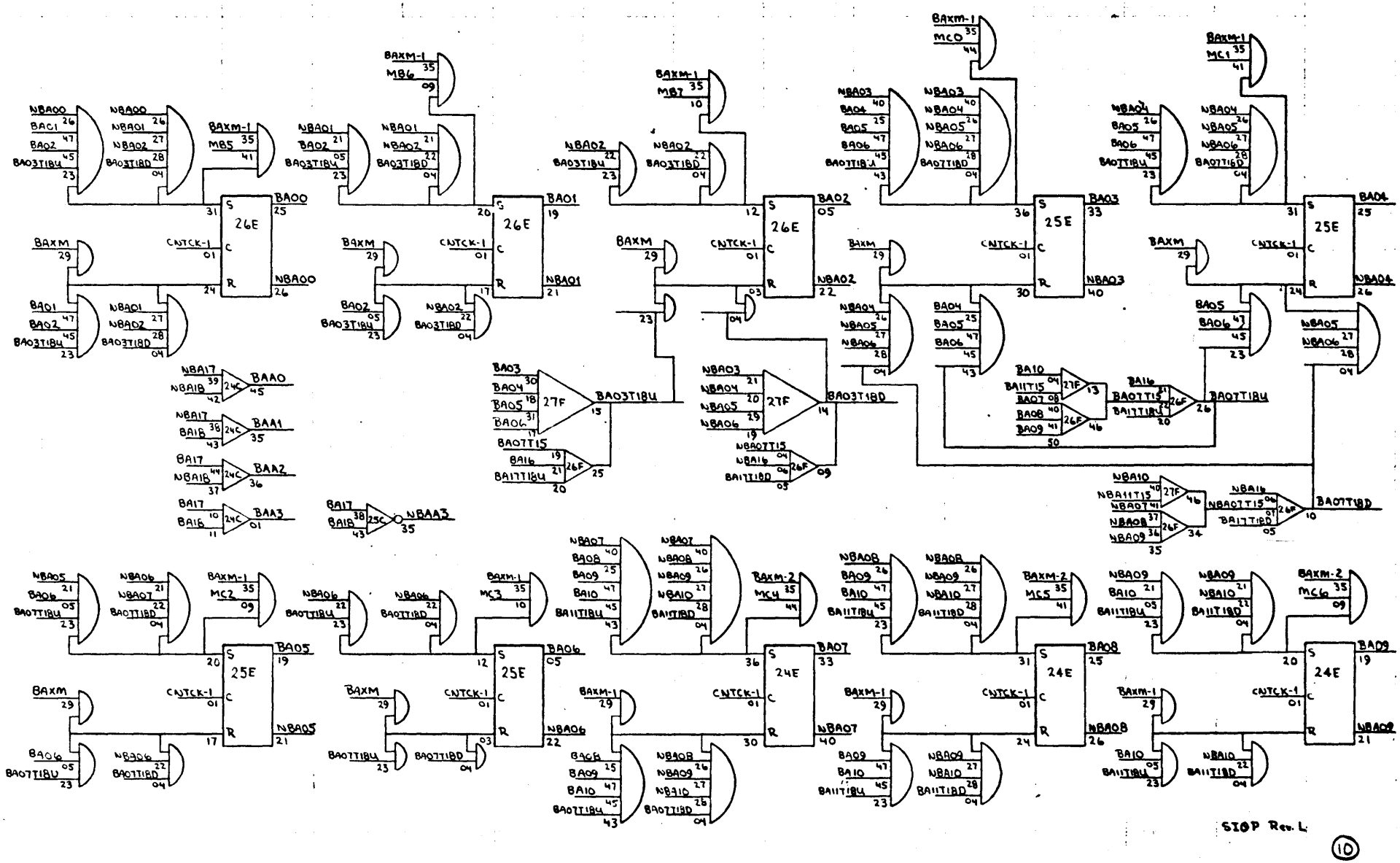
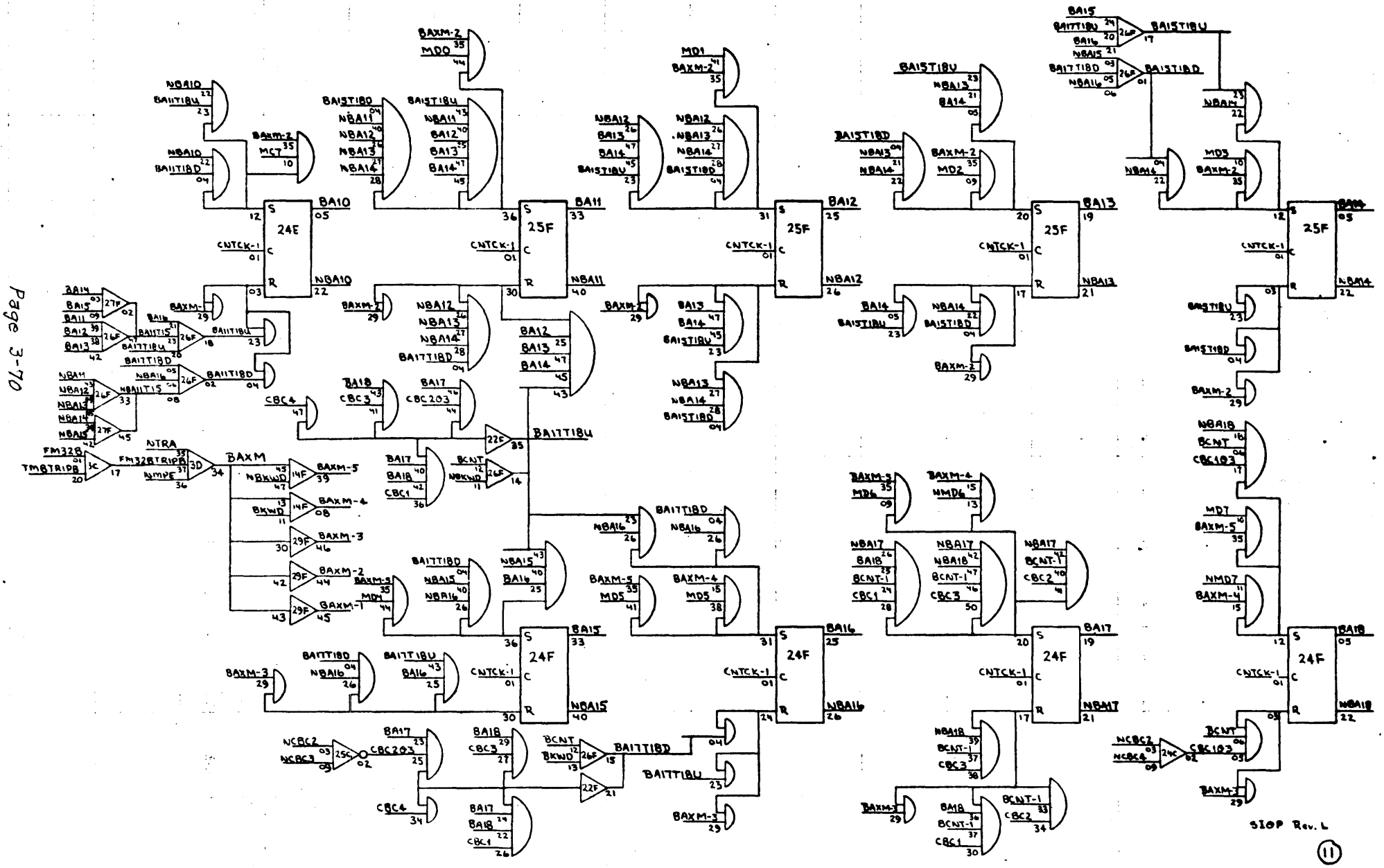
ENDFISET2


26E
25E
24E
27F
25C
26F
24C
CNTCK-1
BAXM
BAXM-1
BAXM-2
SIOP Rev. L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25F
24F
BA10
BA11
BA12
BA13
BA14
BA15
BA16
BA17
BA18
NBA10
NBA11
NBA12
NBA13
NBA14
NBA15
NBA16
NBA17
NBA18
CNTCK-1
BAXM
BAXM-2
BAXM-3
BAXM-4
BAXM-5
BA11T18U
BA11T18D
BA17T18U
BA17T18D
BA15T18U
BA15T18D
NTRA
BCNT
MD1
MD2
MD5
MD6
MD7
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NCBC2
NCBC3
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CBC4
CBC103
CBC203
SIOP Rev. L
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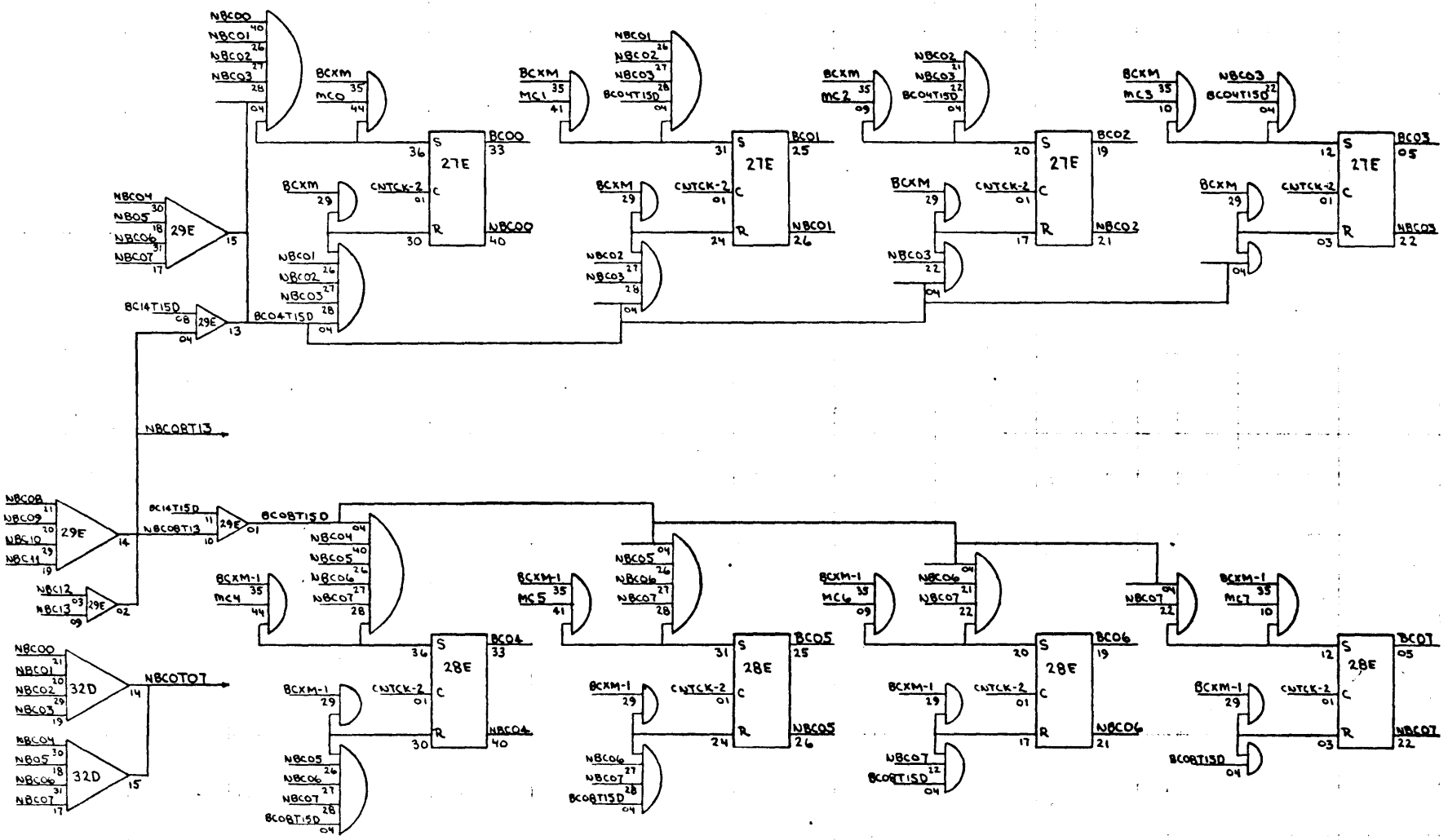
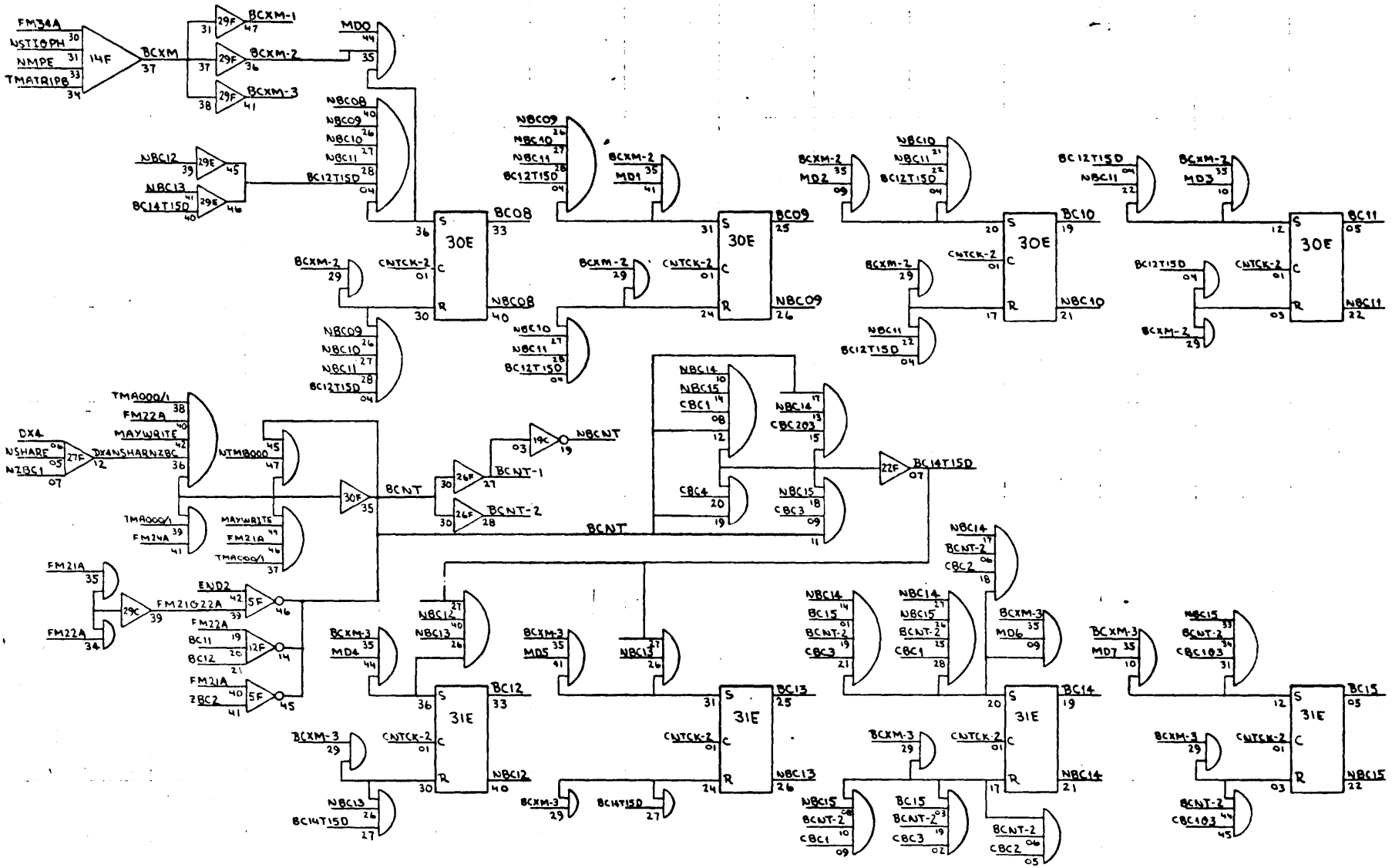
Page 3-70



S10P Rev. L

Eric Schwarz



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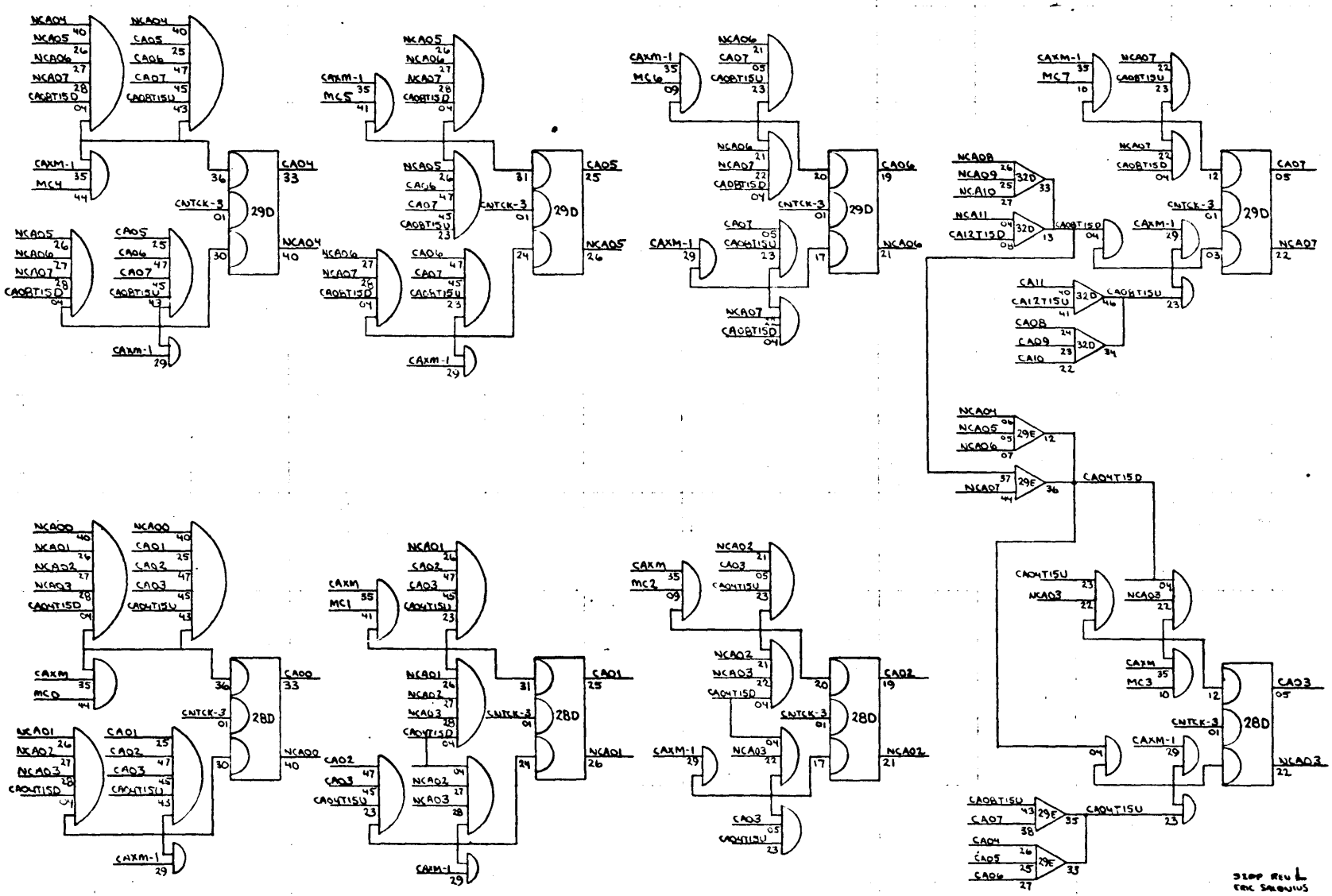
SIOP Rev L
Eric Salowus

(13)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NCA07
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CA05
CA06
CA07
CA0RTISU
CAXM-1
MC4
MC5
MC6
MC7
CNTCK-3
29D
CA04
33
NCA04
40
CA05
25
NCA05
26
CA06
19
NCA06
21
CA07
05
NCA07
22
CA0B
NCA09
NCA10
NCA11
CA12TISD
CA12TISU
32D
CA0HTISD
CA0HTISU
CA11
CA09
CA10
29E
NCA00
NCA01
NCA02
NCA03
CA00
CA01
CA02
CA03
CAXM
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MC1
MC2
MC3
28D
NCA00
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25
NCA02
19
NCA03
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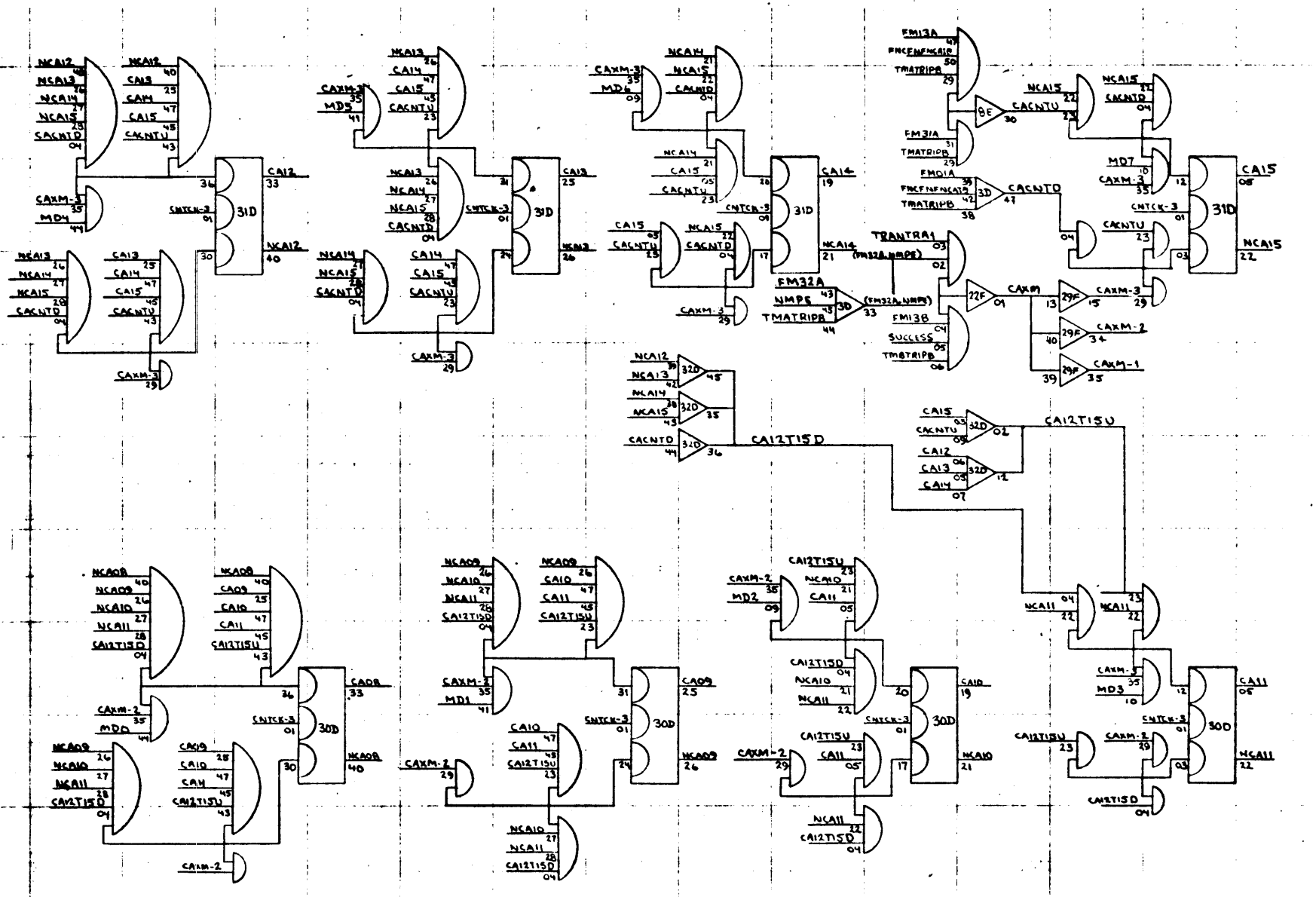
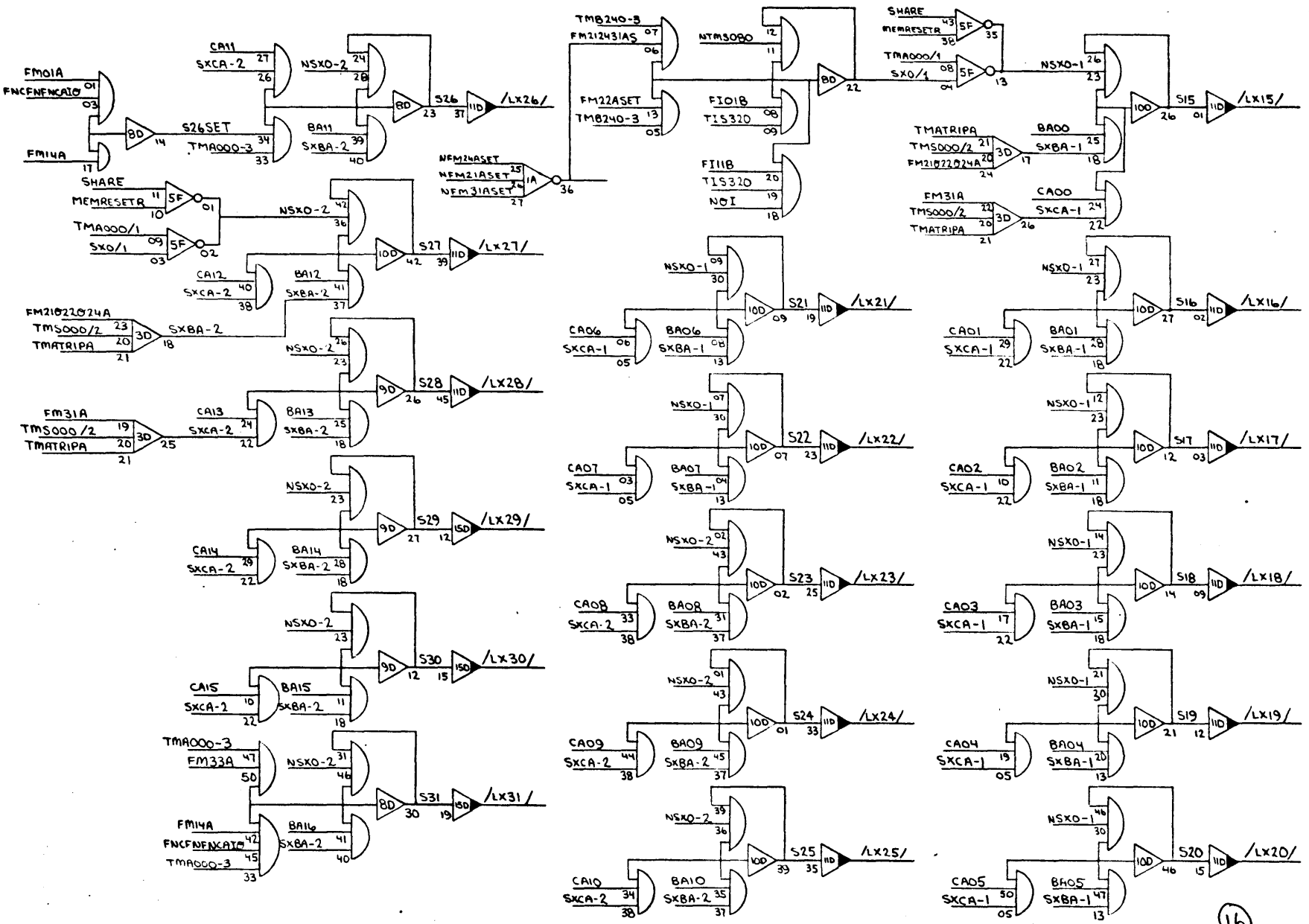


STOP REV L
ERIC SALONIUS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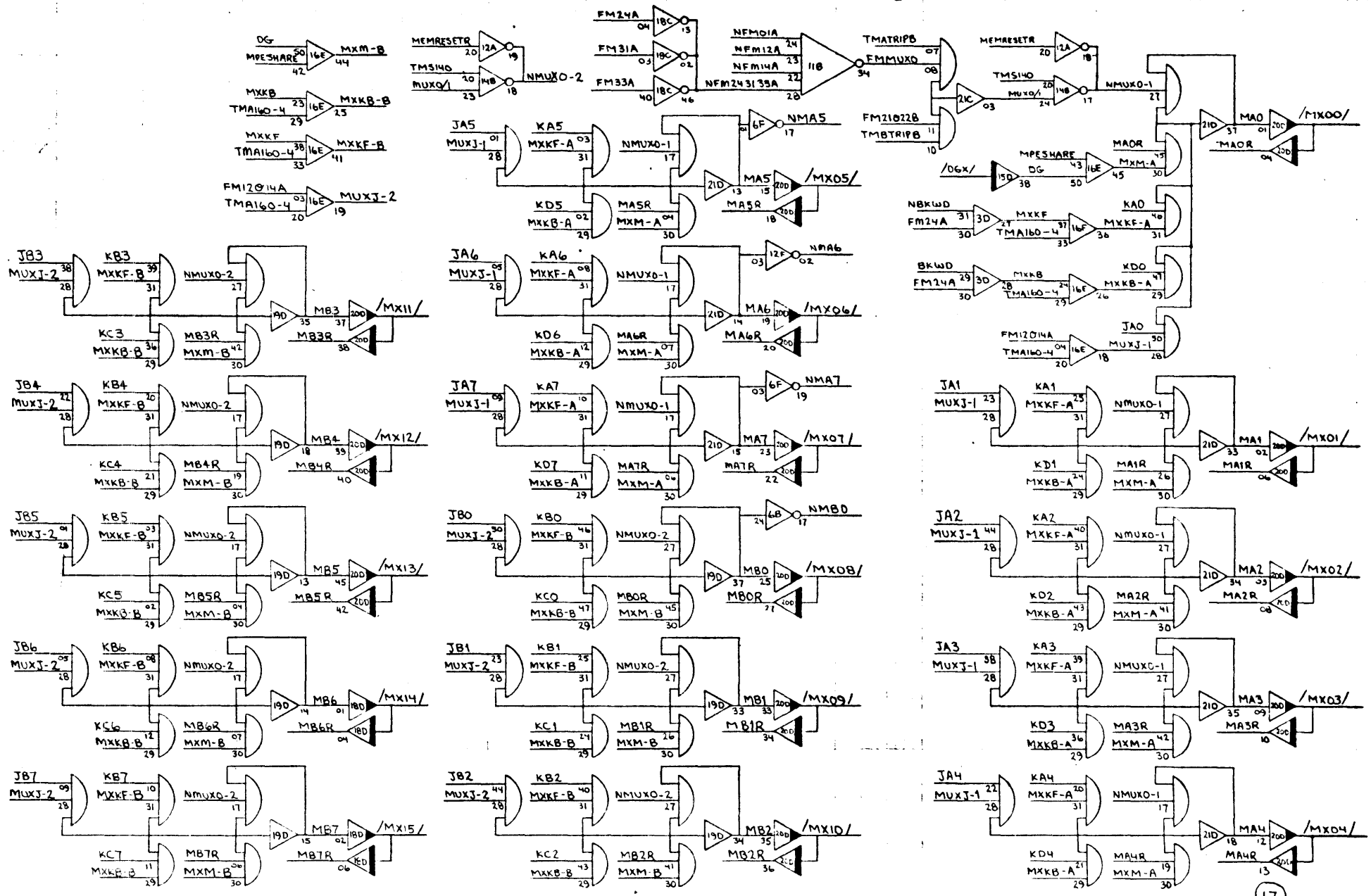
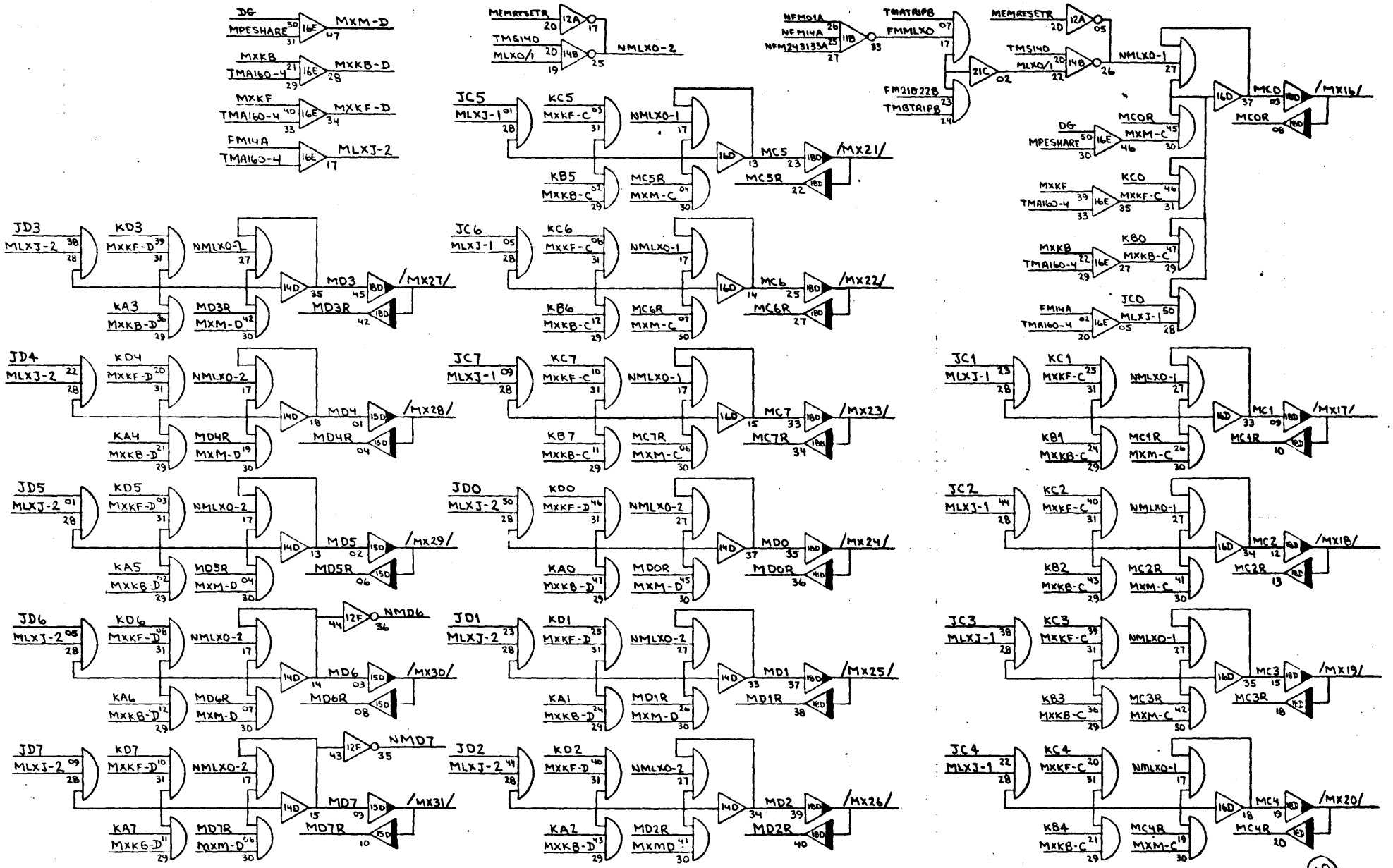
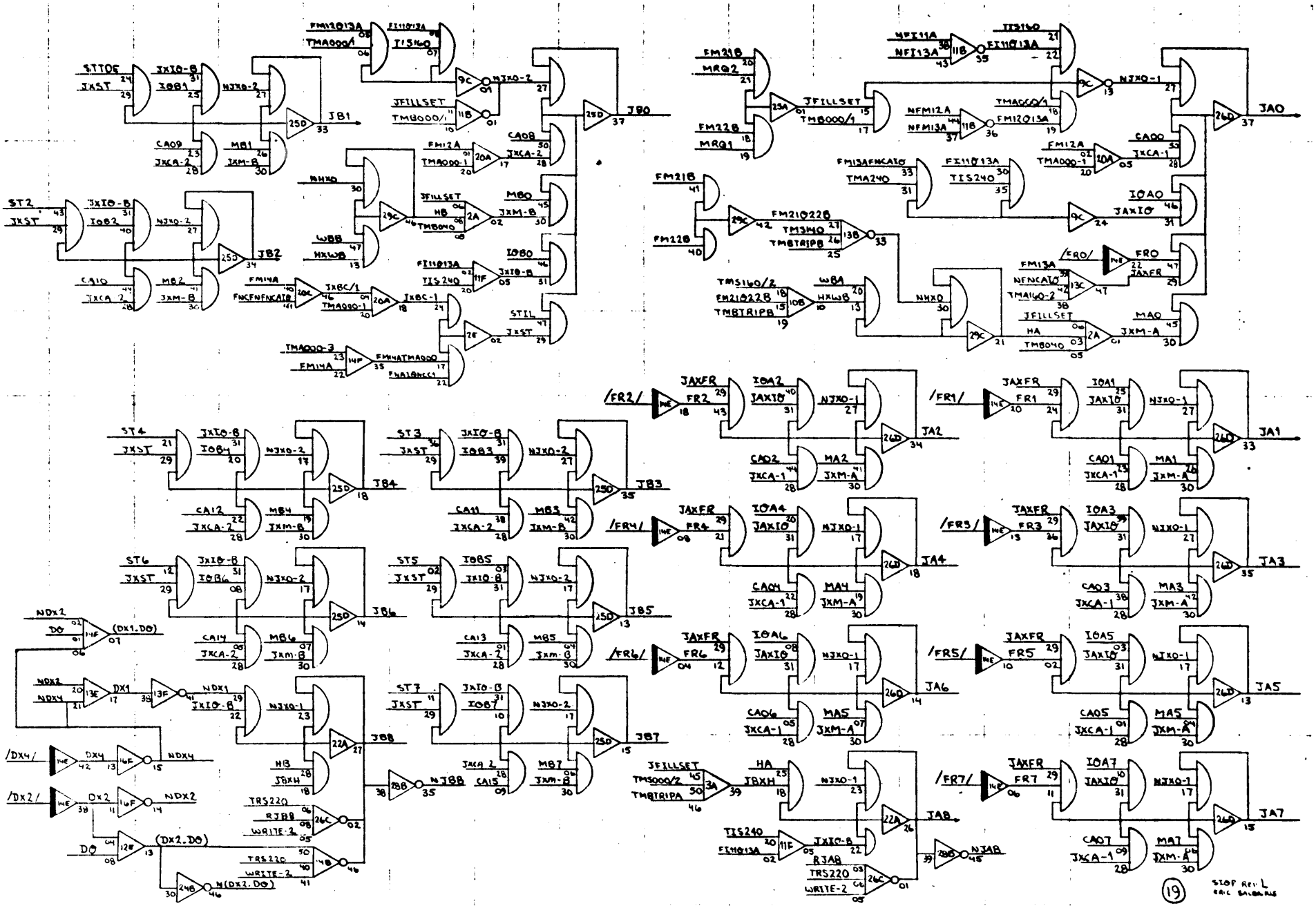
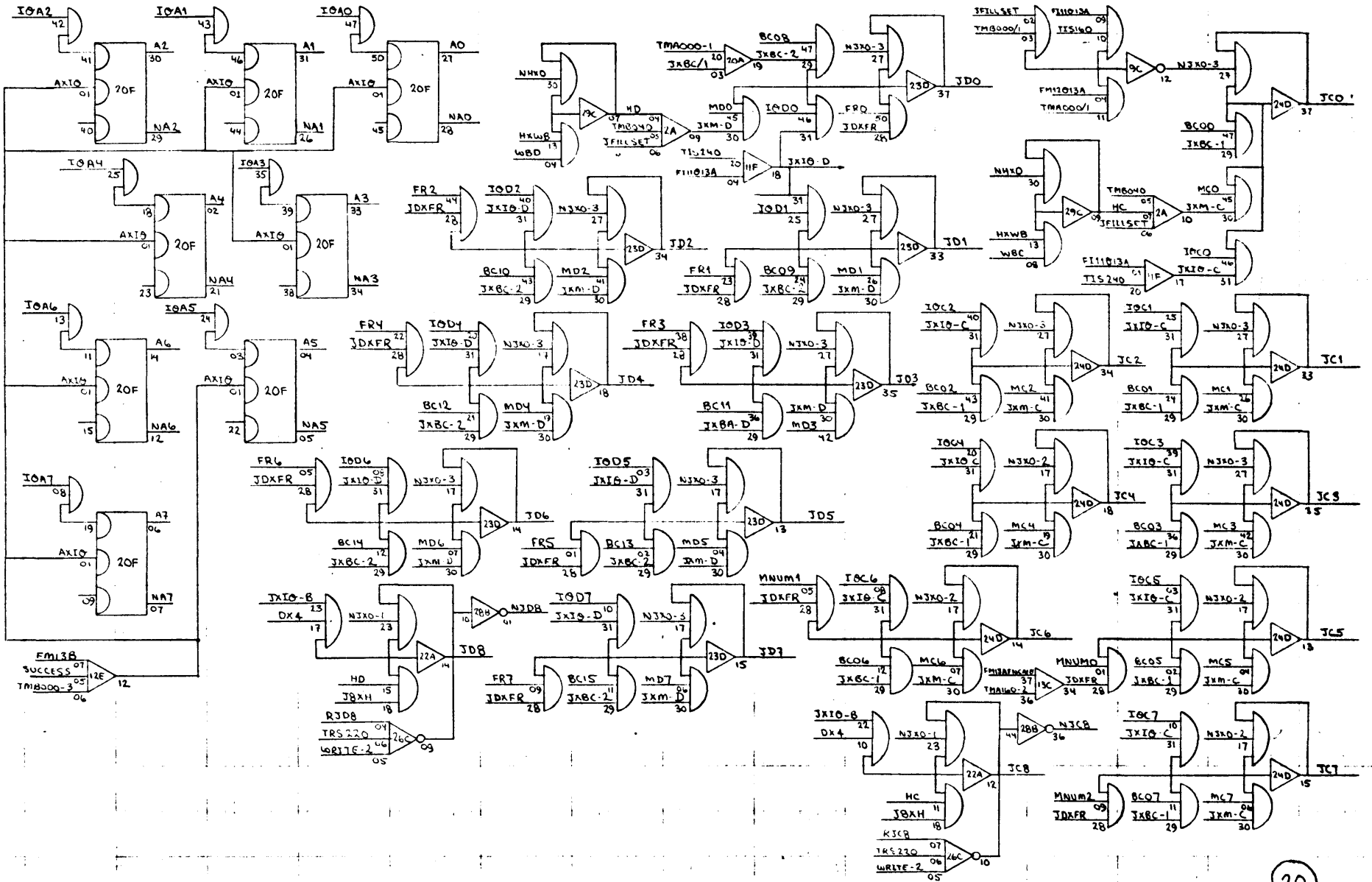
CA11
SXCA-2
NSXO-2
S26SET
TMA000-3
BA11
SXBA-2
S26
/LX26/
FM14A
SHARE
MEMRESETR
TMA000/1
SXO/1
S27
/LX27/
CA12
BA12
FM21B22B24A
TMS000/2
TMATRIPA
SXBA-2
S28
/LX28/
FM31A
CA13
BA13
S29
/LX29/
CA14
BA14
S30
/LX30/
CA15
BA15
TMA000-3
FM33A
S31
/LX31/
FM14A
FNCFNFNCAT0
BA16
TMB240-3
FM21243IAS
FM22ASET
TMB240-3
NFM24ASET
NFM21ASET
NFM31ASET
NTMS080
FI01B
TIS320
FI11B
TIS320
NOI
SHARE
MEMRESETR
TMA000/1
SXO/1
NSXO-1
TMATRIPA
TMS000/2
FM21B22B24A
BA00
SXBA-1
FM31A
TMS000/2
TMATRIPA
CA00
SXCA-1
S21
/LX21/
CA06
BA06
S22
/LX22/
CA07
BA07
S23
/LX23/
CA08
BA08
S24
/LX24/
CA09
BA09
S25
/LX25/
CA10
BA10
S15
/LX15/
S16
/LX16/
CA01
BA01
S17
/LX17/
CA02
BA02
S18
/LX18/
CA03
BA03
S19
/LX19/
CA04
BA04
S20
/LX20/
CA05
BA05


DG
MPESHARE
MXM-B
MXKB
MXKB-B
MXKF
MXKF-B
FM12014A
MUXJ-2
MEMRESETR
TMS140
NMUX0-2
FM24A
FM31A
FM33A
NFM01A
NFM12A
NFM14A
NFM24313 39A
TMATRIPB
FMMUX0
FM21B22B
TMBTRIPB
NMUX0-1
MA0
/MX00/
MA0R
/DGX/
NBKWD
KA0
KD0
JA0
MUXJ-1
JB3
KB3
KC3
MB3
MB3R
/MX11/
JA6
KA6
KD6
NMA6
MA6
MA6R
/MX06/
JB4
KB4
KC4
MB4
MB4R
/MX12/
JA7
KA7
KD7
NMA7
MA7
MA7R
/MX07/
JA1
KA1
KD1
MA1
MA1R
/MX01/
JB5
KB5
KC5
MB5
MB5R
/MX13/
JB0
KB0
KC0
NMB0
MB0
MB0R
/MX08/
JA2
KA2
KD2
MA2
MA2R
/MX02/
JB6
KB6
KC6
MB6
MB6R
/MX14/
JB1
KB1
KC1
MB1
MB1R
/MX09/
JA3
KA3
KD3
MA3
MA3R
/MX03/
JB7
KB7
KC7
MB7
MB7R
/MX15/
JB2
KB2
KC2
MB2
MB2R
/MX10/
JA4
KA4
KD4
MA4
MA4R
/MX04/


DG
MPESHARE
MXM-D
MXKB
TMA160-4
MXKB-D
MXKF
TMA160-4
MXKF-D
FM14A
TMA160-4
MLXJ-2
MEMRESETR
TMS140
MLXO/1
NMLXO-2
NFM01A
NFM14A
NFM2431334
TMATRIPB
FMMLXO
FM21822B
TMBTRIPB
MEMRESETR
TMS140
MLXO/1
NMLXO-1
DG
MPESHARE
MXM-C
MXKF
TMA160-4
MXKF-C
MXKB
TMA160-4
MXKB-C
FM14A
TMA160-4
MLXJ-1
JC5
MLXJ-1
KC5
MXKF-C
KB5
MXKB-C
MC5
MC5R
MXM-C
/MX21/
JD3
MLXJ-2
KD3
MXKF-D
KA3
MXKB-D
NMLXO-2
MD3
MD3R
MXM-D
/MX27/
JC6
MLXJ-1
KC6
MXKF-C
KB6
MXKB-C
NMLXO-1
MC6
MC6R
MXM-C
/MX22/
JD4
MLXJ-2
KD4
MXKF-D
KA4
MXKB-D
NMLXO-2
MD4
MD4R
MXM-D
/MX28/
JC7
MLXJ-1
KC7
MXKF-C
KB7
MXKB-C
NMLXO-1
MC7
MC7R
MXM-C
/MX23/
JC1
MLXJ-1
KC1
MXKF-C
KB1
MXKB-C
NMLXO-1
MC1
MC1R
MXM-C
/MX17/
JD5
MLXJ-2
KD5
MXKF-D
KA5
MXKB-D
NMLXO-2
MD5
MD5R
MXM-D
/MX29/
JD0
MLXJ-2
KD0
MXKF-D
KA0
MXKB-D
NMLXO-2
MD0
MD0R
MXM-D
/MX24/
JC2
MLXJ-1
KC2
MXKF-C
KB2
MXKB-C
NMLXO-1
MC2
MC2R
MXM-C
/MX18/
JD6
MLXJ-2
KD6
MXKF-D
KA6
MXKB-D
NMLXO-2
NMD6
MD6
MD6R
MXM-D
/MX30/
JD1
MLXJ-2
KD1
MXKF-D
KA1
MXKB-D
NMLXO-2
MD1
MD1R
MXM-D
/MX25/
JC3
MLXJ-1
KC3
MXKF-C
KB3
MXKB-C
NMLXO-1
MC3
MC3R
MXM-C
/MX19/
JD7
MLXJ-2
KD7
MXKF-D
KA7
MXKB-D
NMLXO-2
NMD7
MD7
MD7R
MXM-D
/MX31/
JD2
MLXJ-2
KD2
MXKF-D
KA2
MXKB-D
NMLXO-2
MD2
MD2R
MXMD
/MX26/
JC4
MLXJ-1
KC4
MXKF-C
KB4
MXKB-C
NMLXO-1
MC4
MC4R
MXM-C
/MX20/



STOP Rev L
ERIC BALDWIN



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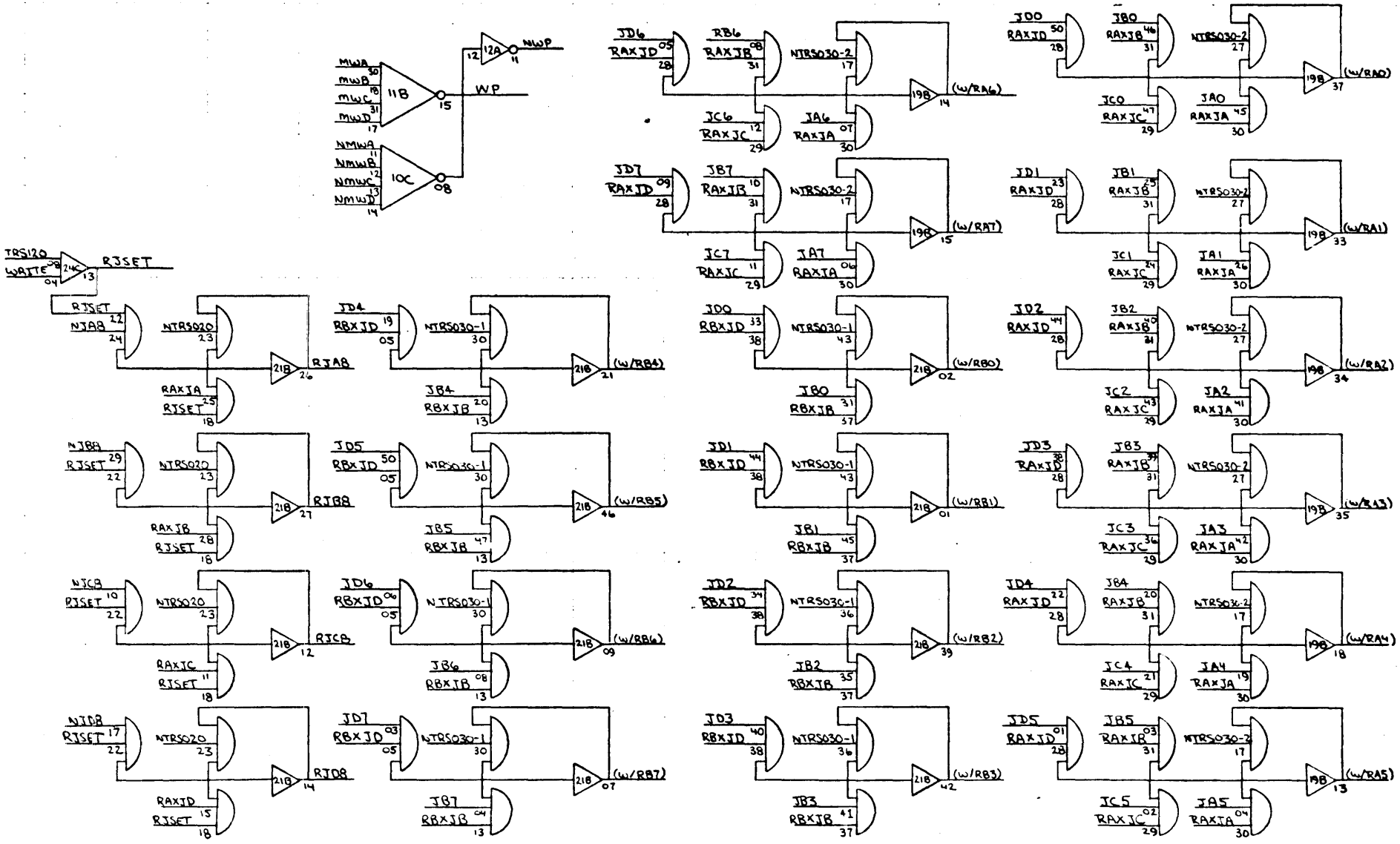
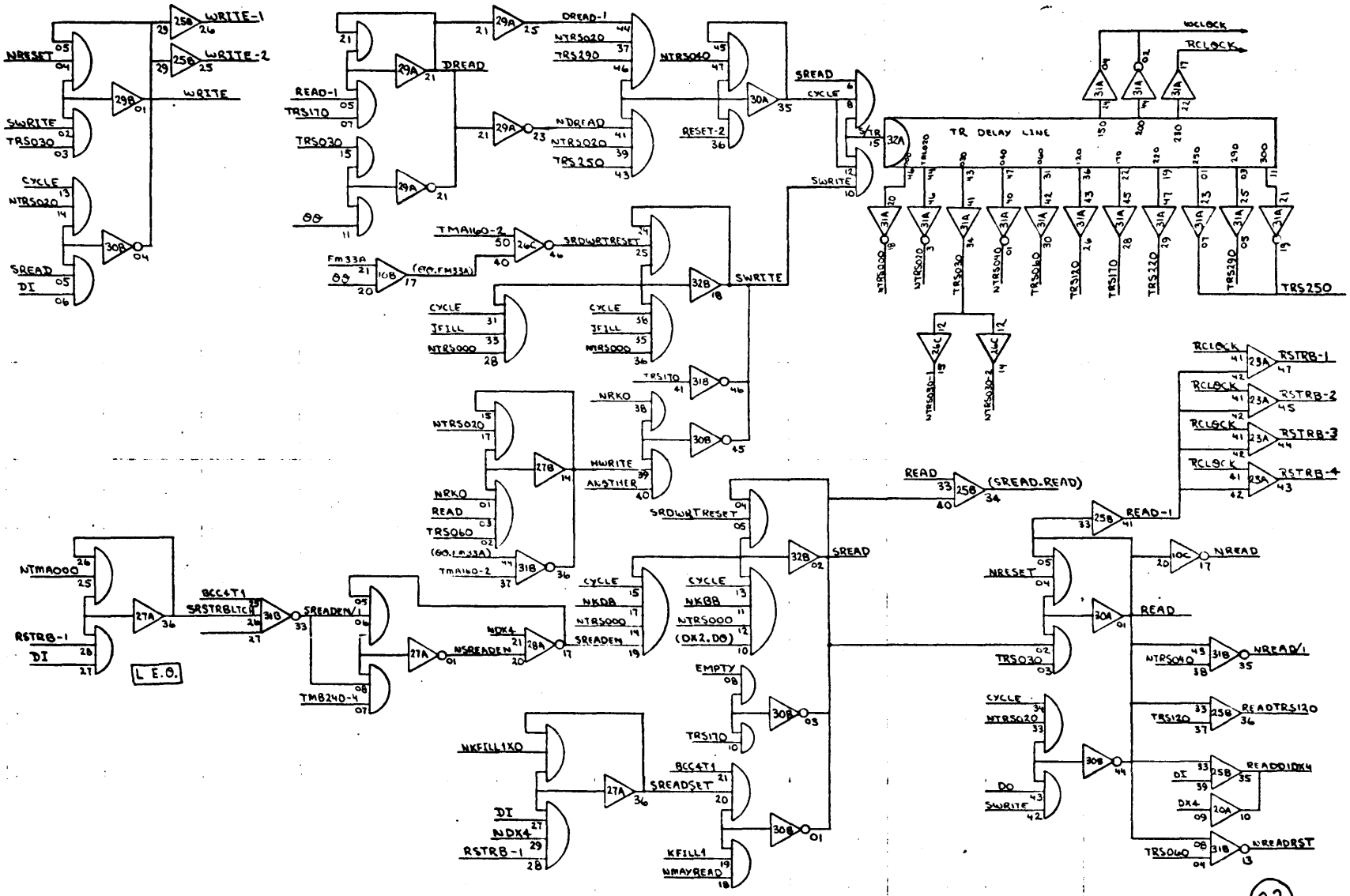
STOP REG L
ERIC SALONIUS



SIOP REV L
Eric Sakaue



SIOP REV L
Eric Salomon

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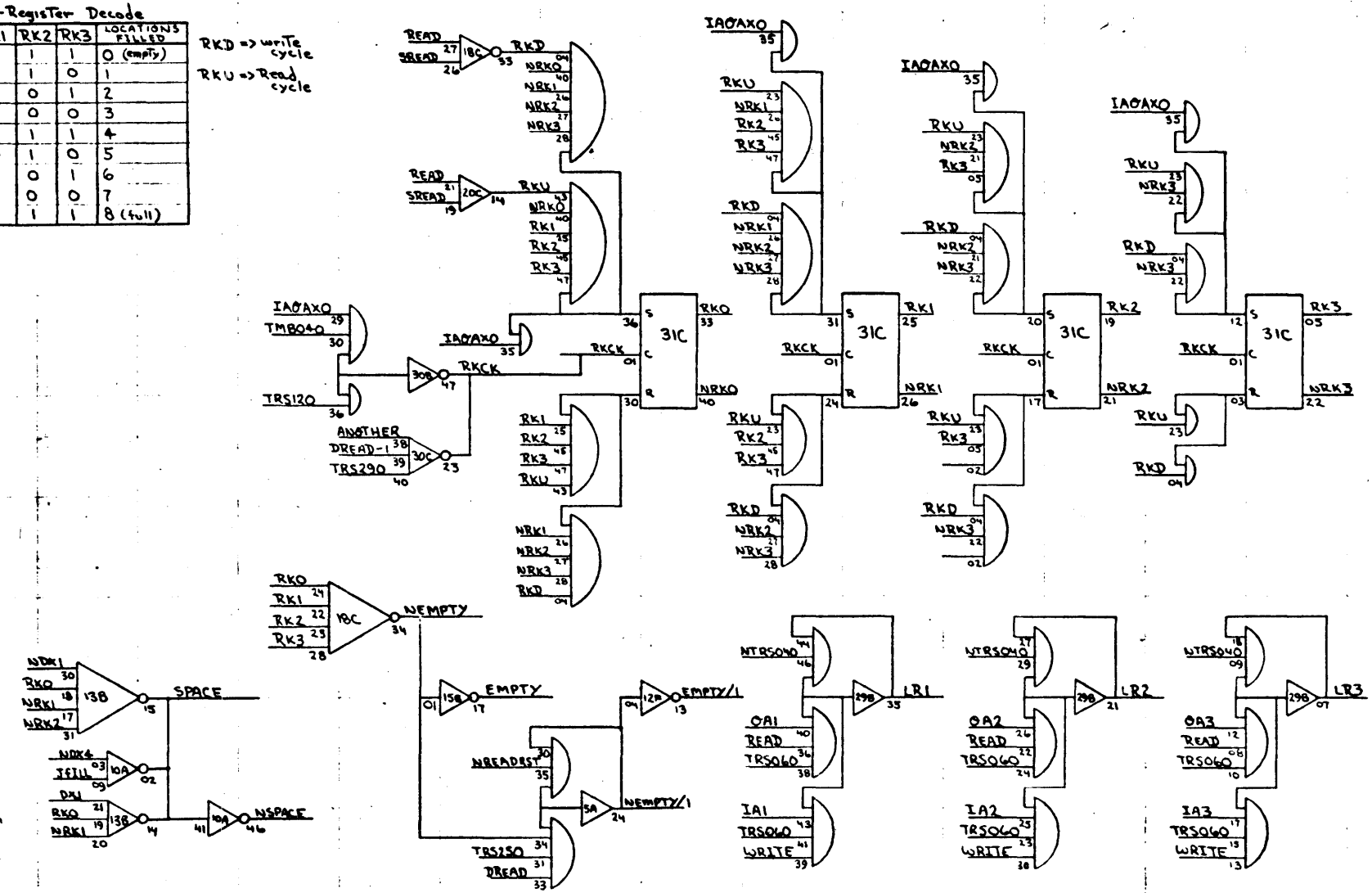
RK-Register Decode

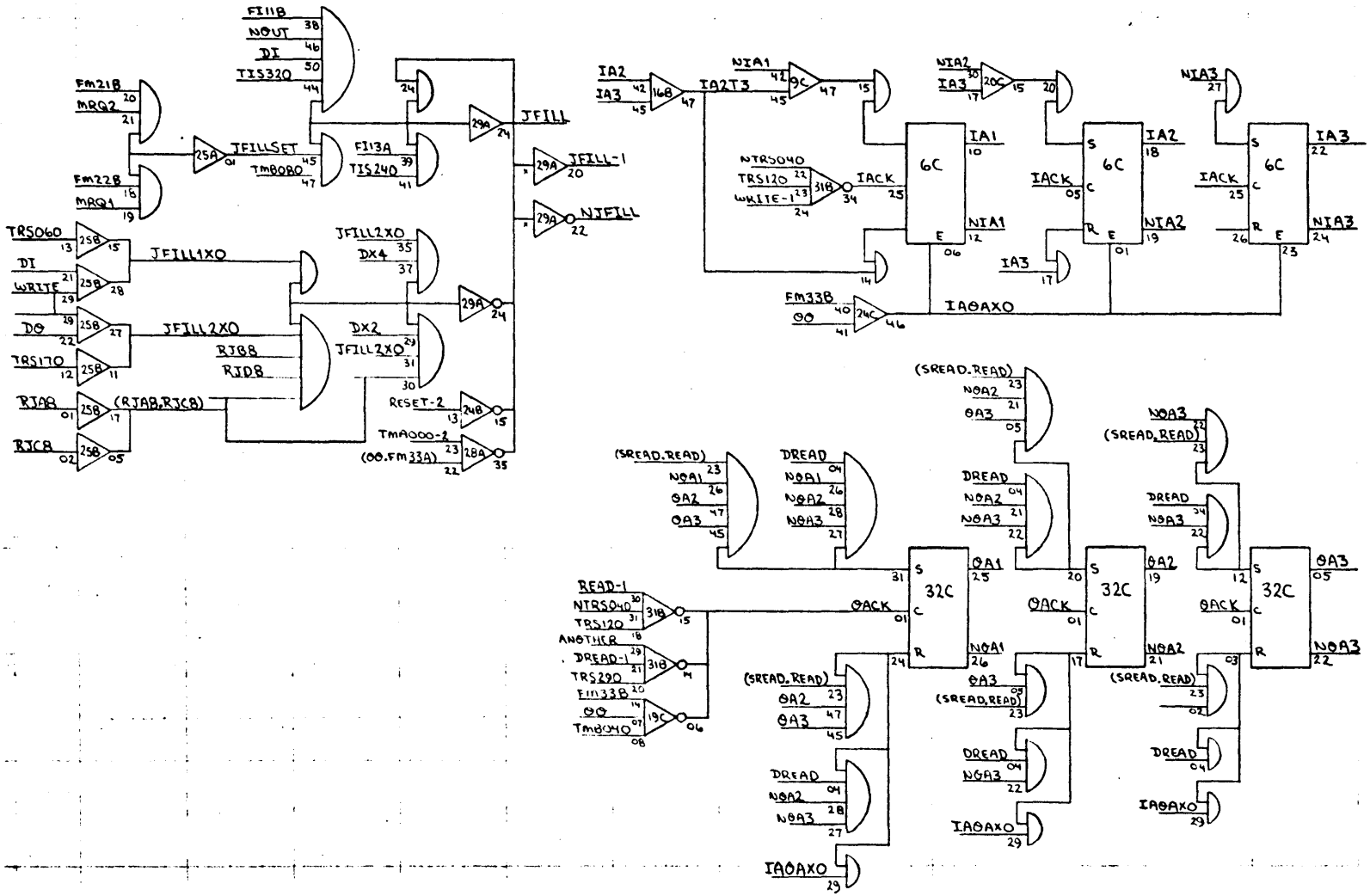
RK0	RK1	RK2	RK3	LOCATIONS FILLED
1	1	1	1	0 (empty)
1	1	1	0	1
1	1	0	1	2
1	1	0	0	3
1	0	1	1	4
1	0	1	0	5
1	0	0	1	6
1	0	0	0	7
0	1	1	1	8 (full)

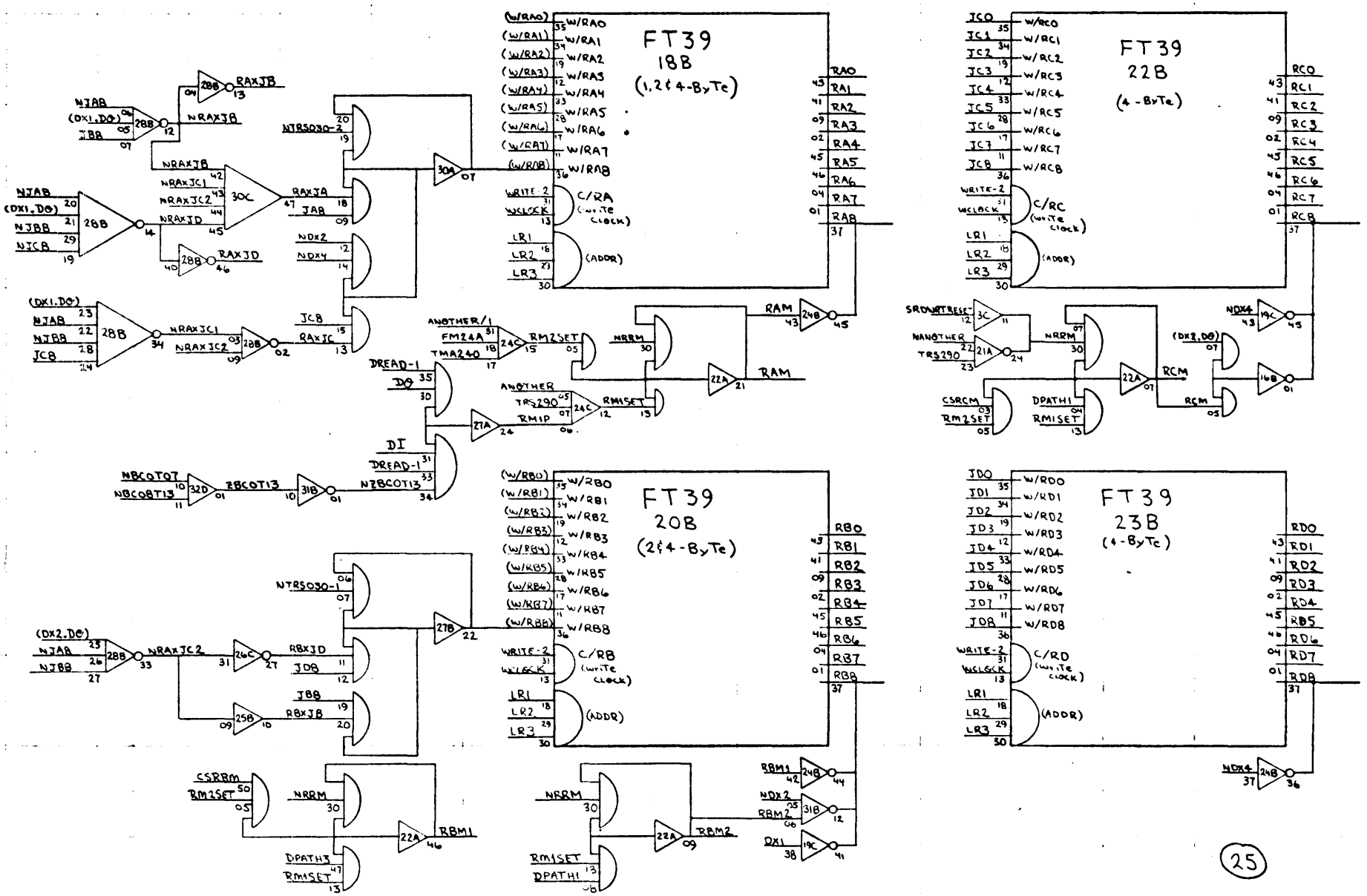
RKD => write cycle

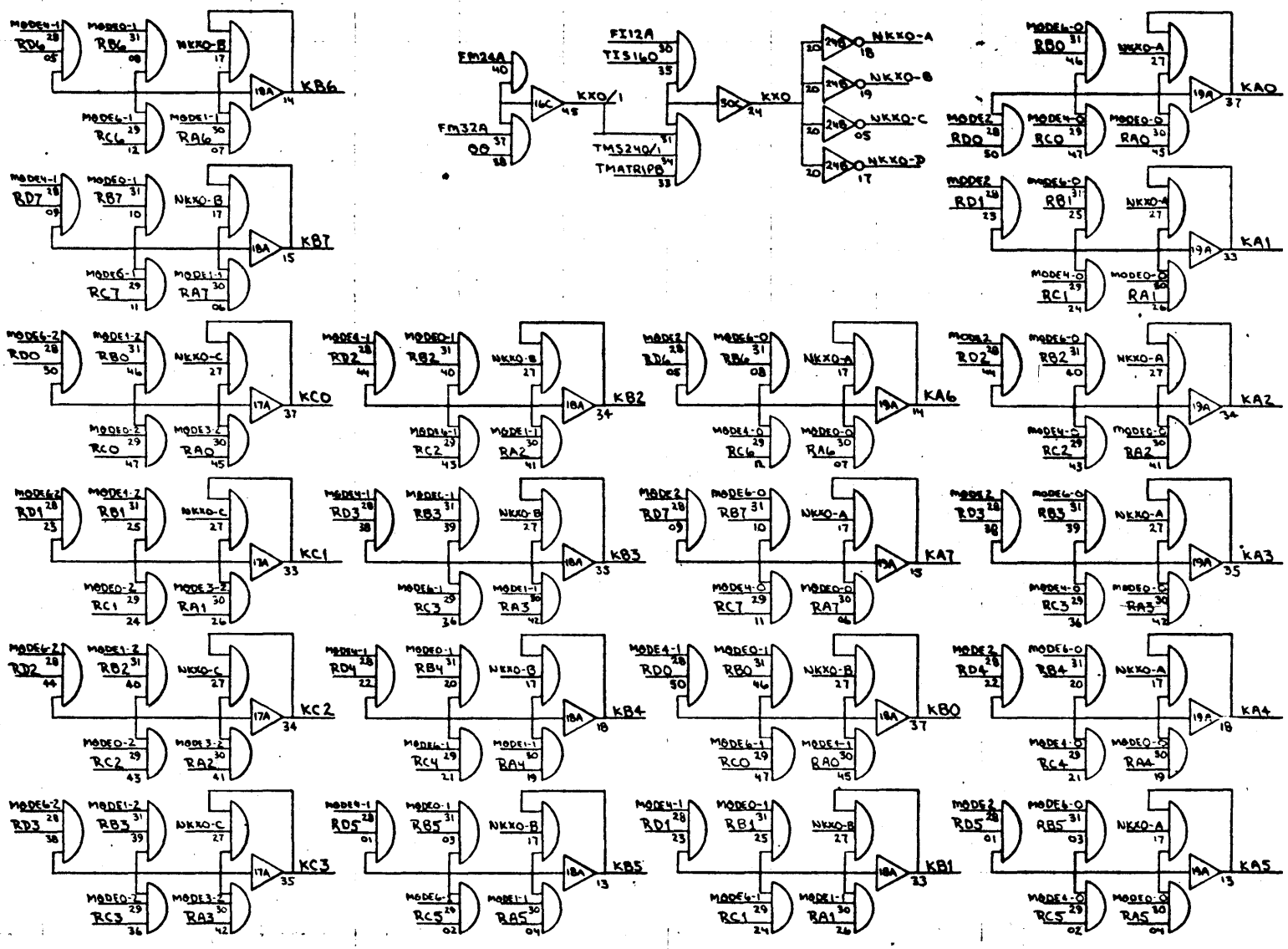
RKU => Read cycle



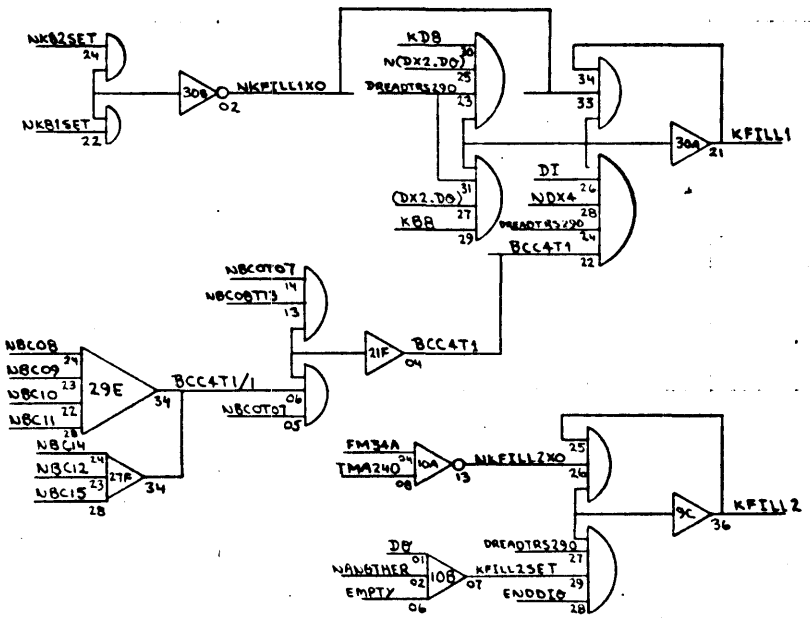
SIOP Rev L
Eric Salomon

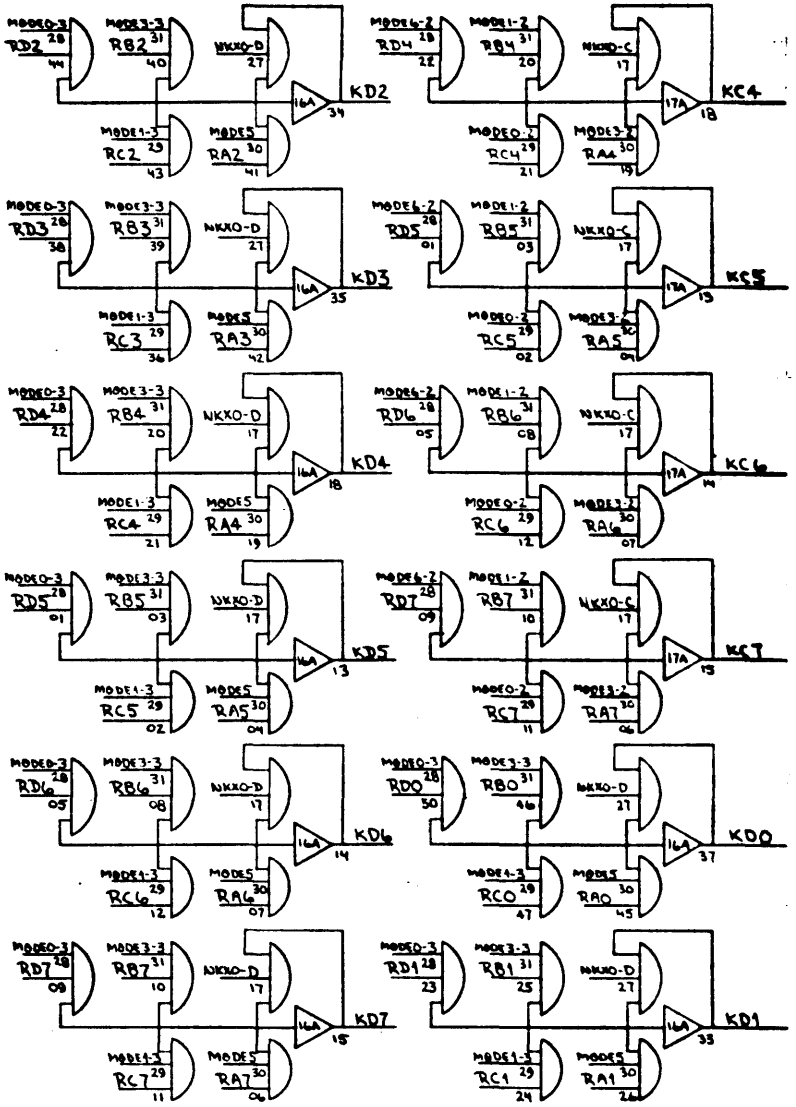

FI11B
NOUT
DI
TIS330
Fm21B
MRQ2
Fm22B
MRQ1
JFILLSET
TM8080
FI13A
TIS240
JFILL
JFILL-1
NJFILL
TRS060
DI
WRITE
DO
TRS170
RJAB
RJCB
(RJAB.RJCB)
JFILL1XO
JFILL2XO
RJDB
DX4
DX2
RESET-2
TMA000-2
(00.FM33A)
IA2
IA3
IA2T3
NIA1
NIA2
NIA3
NTRS040
TRS120
WRITE-1
IACK
IA1
IA2
IA3
IAØAXO
FM33B
(SREAD.READ)
NØA1
NØA2
NØA3
ØA1
ØA2
ØA3
DREAD
ØACK
READ-1
NTRS040
TRS120
ANOTHER
DREAD-1
TRS290
FM33B
00
TM8040
6C
32C


FT39
18B
(1,2 & 4-ByTe)
FT39
22B
(4-ByTe)
FT39
20B
(2 & 4-ByTe)
FT39
23B
(4-ByTe)
C/RA
C/RC
C/RB
C/RD
(ADDR)
(write clock)
RAM
RCM
RBM1
RBM2
NRRM
RAXJB
RAXJA
RAXJC
RAXJD
RBXJD
RBXJB
RBXJC
NTRS030-2
NTRS030-1
DREAD-1
DI
DO
ANOTHER/1
ANOTHER
FM24A
TMA240
TRS290
RM2SET
RMISET
RM1P
CSRRM
CSRCM
DPATH1
DPATH3
SROWTRESET
NANOTHER
NDX2
NDX4
DX1
NJAB
NJBB
NJCB
JAB
JBB
JCB
JDB



SIOP Rev L.
Eric Salomus





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Eric Schwinn

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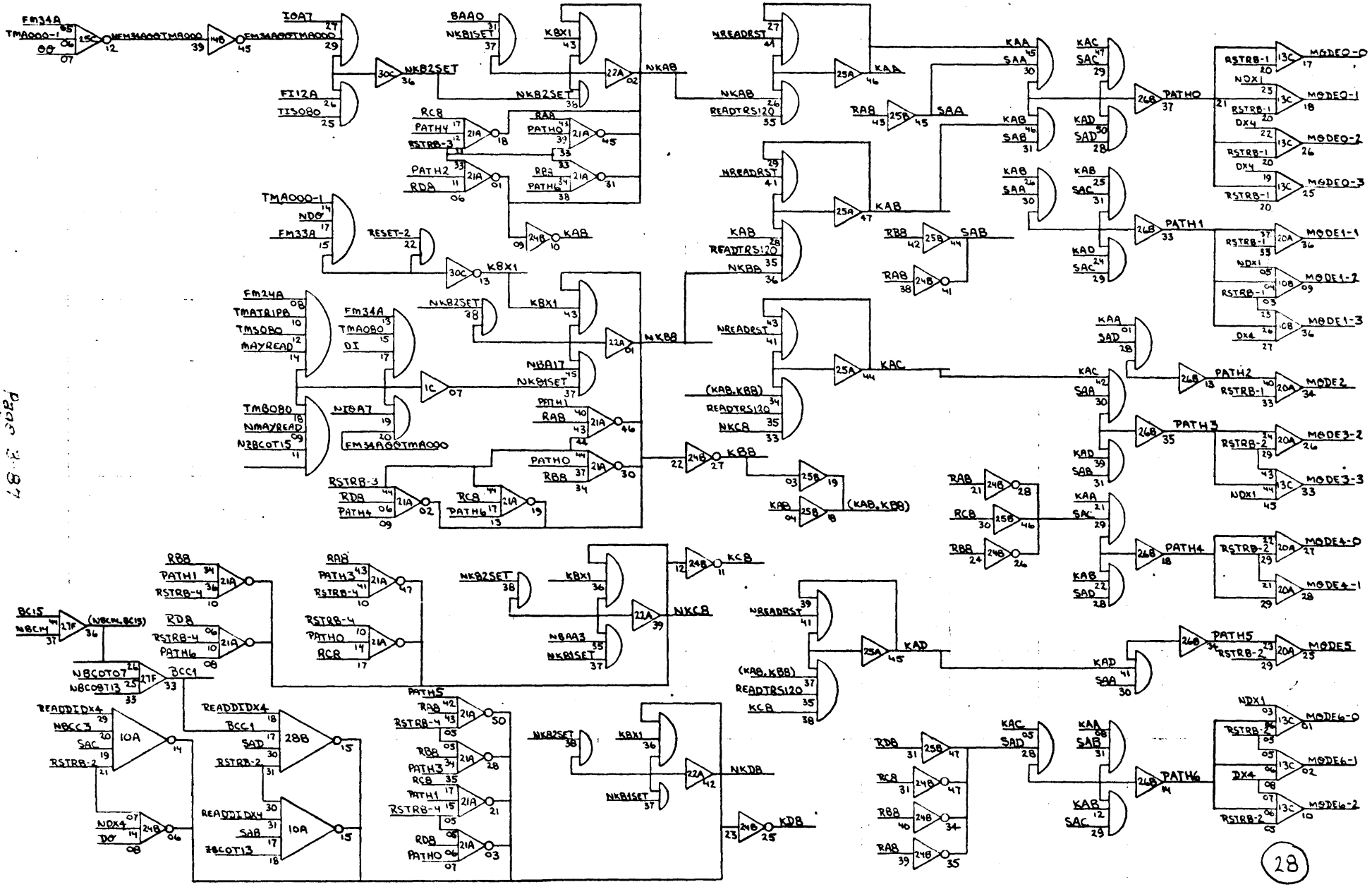
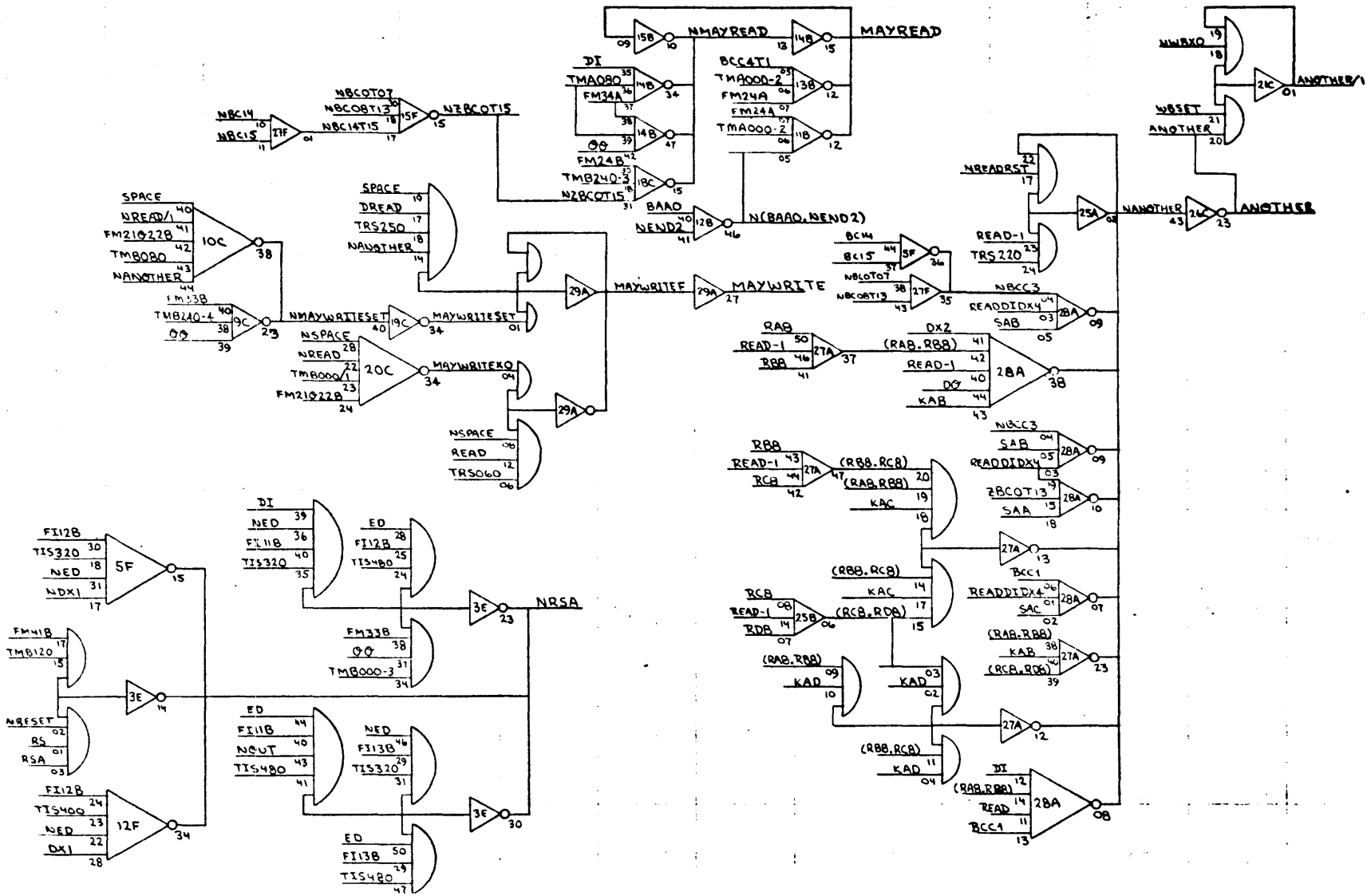
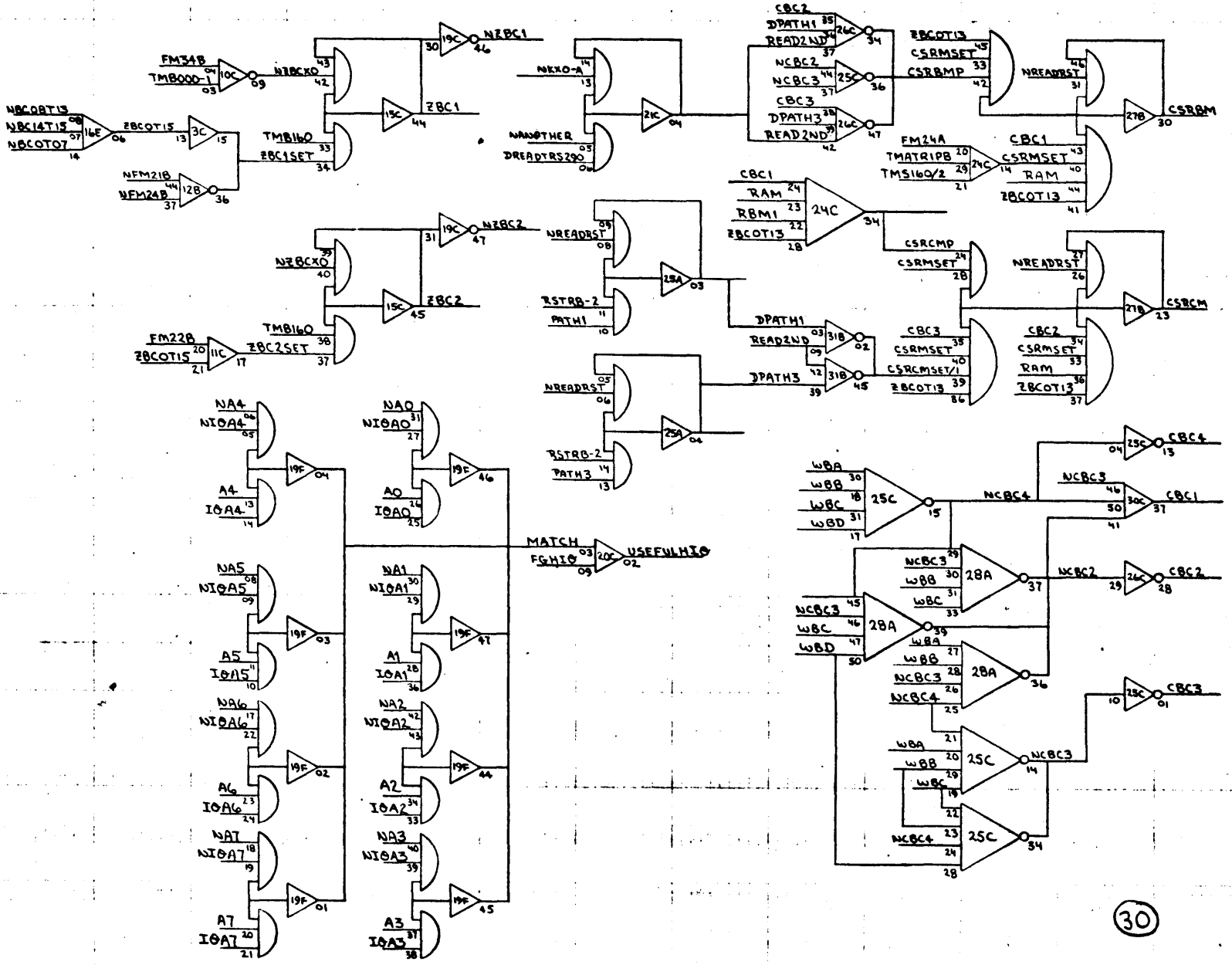
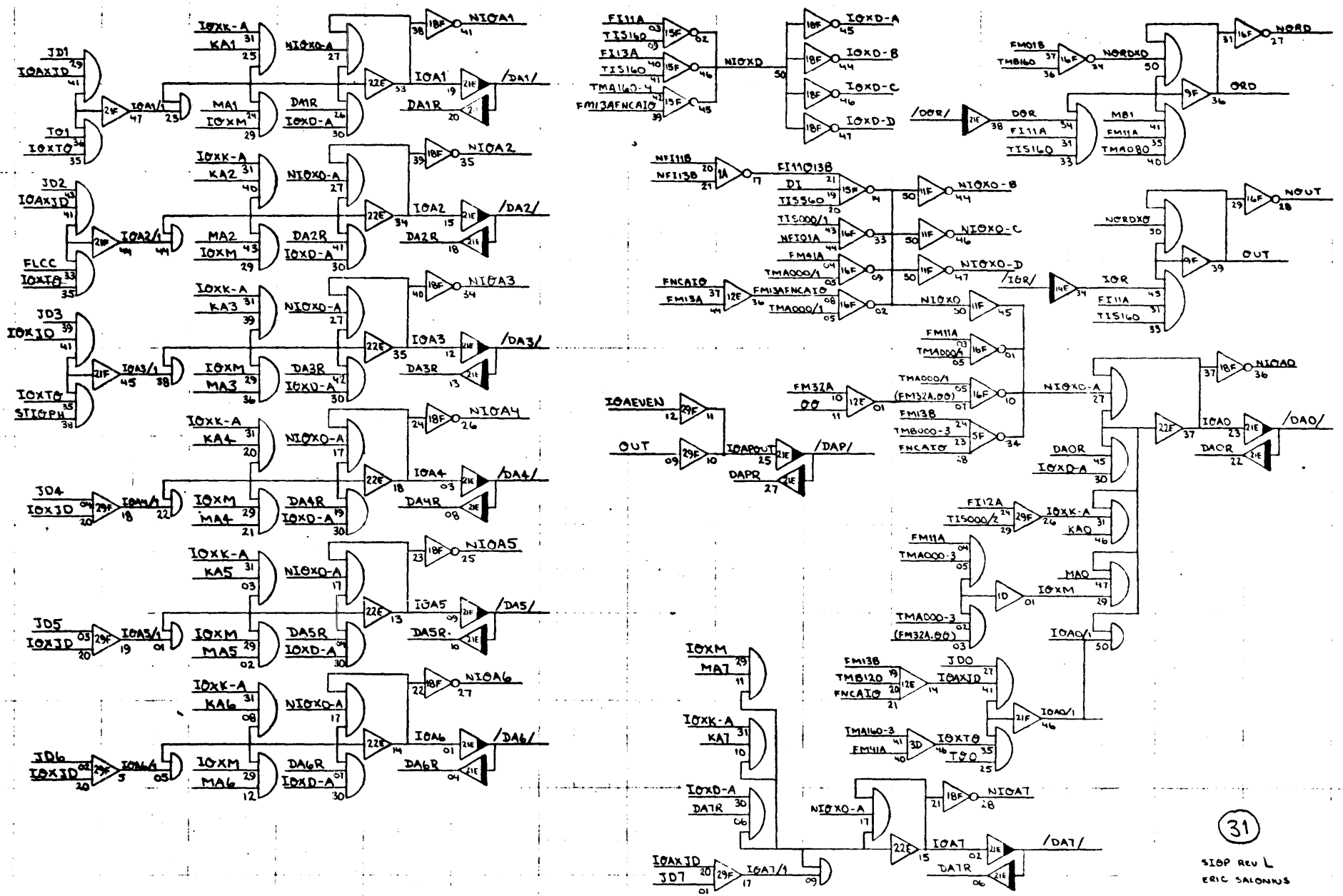

FM34A
TMA000-1
NFM34A00TMA000
FM34A00TMA000
IOA7
FI12A
TI5080
NKB2SET
BAA0
NKB1SET
KBX1
NKAB
NREADRST
READTRS120
KAA
SAA
KAC
SAC
KAB
SAB
KAD
SAD
PATH0
PATH1
PATH2
PATH3
PATH4
PATH5
PATH6
MODE0-0
MODE0-1
MODE0-2
MODE0-3
MODE1-1
MODE1-2
MODE1-3
MODE2
MODE3-2
MODE3-3
MODE4-0
MODE4-1
MODE5
MODE6-0
MODE6-1
MODE6-2
RCB
PATH4
RSTRB-3
RAB
PATH0
PATH2
RDA
PATH6
RBA
TMA000-1
NDO
FM33A
RESET-2
K8X1
FM24A
TMATRIPA
TM5080
MAYREAD
FM34A
TMA080
DI
NBA17
NKB1SET
PATH1
TM8080
NMAYREAD
N2BCOT15
FM34A00TMA000
RSTRB-3
RDA
PATH4
RCB
PATH6
PATH0
RBA
NKAB
KAB
(KAB.KB8)
KB8
KAA
SAA
KAC
SAC
KAB
SAB
KAD
SAD
PATH0
PATH1
PATH2
PATH3
PATH4
PATH5
PATH6
RSTRB-1
RSTRB-2
NDX1
DX4
MODE0-0
MODE0-1
MODE0-2
MODE0-3
MODE1-1
MODE1-2
MODE1-3
MODE2
MODE3-2
MODE3-3
MODE4-0
MODE4-1
MODE5
MODE6-0
MODE6-1
MODE6-2
RAB
PATH1
RSTRB-4
RDA
PATH6
RAB
PATH3
RSTRB-4
RSTRB-4
PATH0
RCB
NKB2SET
KBX1
NKCB
NBAA3
NKB1SET
KCB
BC15
NBCM
(NBCM.BC15)
NBCOTOT
NBCOBT13
BCC1
READDIDX4
NBCC3
SAC
RSTRB-2
10A
NDX4
DO
READDIDX4
BCC1
SAD
RSTRB-2
288
READDIDX4
SAB
Z8COT13
10A
PATH5
RAB
RSTRB-4
RDB
PATH3
RCB
PATH1
RSTRB-4
RDB
PATH0
NKB2SET
KBX1
NKDB
NKB1SET
KDB
NREADRST
READTRS120
(KAB.KB8)
KCB
KAD
RDB
RCB
RBB
RAB
KAC
KAA
KAB
KAD
PATH6
NDX1
DX4
RSTRB-1
RSTRB-2
MODE6-0
MODE6-1
MODE6-2


NMAYREAD
MAYREAD
NBCOTOT
NBCOBT13
NBC14T15
N2BCOT15
NBC14
NBC15
DI
TMA080
FM34A
FM24B
TMB240-3
BCC4T1
TMA000-2
FM24A
TMA000-2
BAA0
NEND2
N(BAA0.NEND2)
SPACE
NREAD/1
FM21@22B
TMB080
NANOTHER
FM33B
TMB240-4
NMAYWRITESET
MAYWRITESET
DREAD
TRS250
NSPACE
NREAD
TMB000-1
FM21@22B
MAYWRITEXO
MAYWRITEF
MAYWRITE
NSPACE
READ
TRS060
RAB
READ-1
RBB
(RAB.RBB)
DX2
KAB
BCC4
BC15
NBCOTOT
NBCOBT13
NBCC3
READDIDX4
SAB
NREADRST
TRS220
NWBXO
WBSET
ANOTHER
ANOTHER/1
RBB
READ-1
RCB
(RBB.RCB)
(RAB.RBB)
KAC
RCB
READ-1
RDB
(RCB.RDB)
(RBB.RCB)
KAD
(RAB.RBB)
KAD
(RBB.RCB)
KAD
ZBCOT13
SAA
BCC1
READDIDX4
SAC
(RAB.RBB)
KAB
(RCB.RDB)
DI
(RAB.RBB)
READ
BCC1
FI12B
TIS320
NED
NDX1
FM41B
TMB120
NRESET
RS
RSA
FI12B
TIS400
NED
DX1
DI
NED
FI11B
TIS320
ED
FI12B
TIS480
FM33B
TMB000-3
ED
FI11B
NOUT
TIS480
NED
FI13B
TIS320
ED
FI13B
TIS480
NRSA


FM34B
TMB000-1
10C
NZBCX0
19C
NZBC1
ZBC1
15C
TMB160
ZBC1SET
NBC08T13
NBC14T15
NBC07T7
16E
ZBC0T15
3C
NFM21B
NFM24B
12B
NEXO-A
NANOTHER
DREADTRS290
21C
CBC2
DPATH1
READ2ND
26C
NCBC2
NCBC3
25C
CBC3
DPATH3
READ2ND
24C
ZBC0T13
CSRMSET
CSRBMP
NREADRST
27B
CSRBM
FM24A
TMATRIPB
TMS160/2
24C
CBC1
CSRMSET
RAM
ZBC0T13
NZBC2
NZBCX0
ZBC2
TMB160
ZBC2SET
FM22B
ZBC0T15
11C
NREADRST
RSTRB-2
PATH1
25A
CBC1
RAM
RBM1
ZBC0T13
24C
CSRCMP
CSRMSET
DPATH1
READ2ND
31B
DPATH3
CSRCMSET/1
ZBC0T13
CBC3
CSRMSET
CBC2
CSRMSET
RAM
ZBC0T13
CSRCM
NREADRST
RSTRB-2
PATH3
NA4
NIOA4
A4
IOA4
NA5
NIOA5
A5
IOA5
NA6
NIOA6
A6
IOA6
NA7
NIOA7
A7
IOA7
NA0
NIOA0
A0
IOA0
NA1
NIOA1
A1
IOA1
NA2
NIOA2
A2
IOA2
NA3
NIOA3
A3
IOA3
19F
MATCH
FGHIO
20C
USEFULHIO
W8A
W8B
W8C
W8D
25C
NCBC4
CBC4
NCBC3
CBC1
28A
NCBC2
CBC2
CBC3
(30)



SIOP Rev L
ERIC SALONUS

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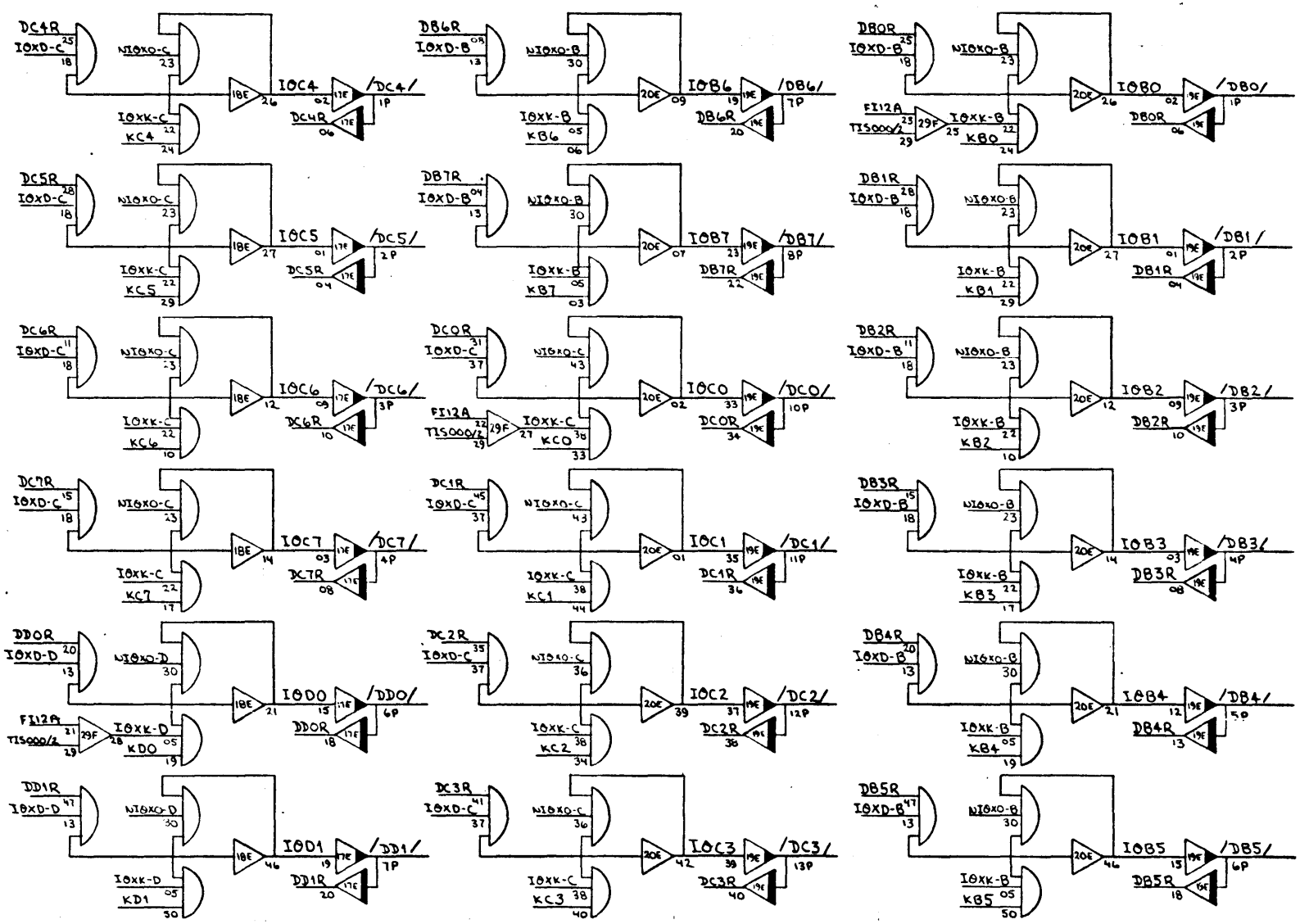
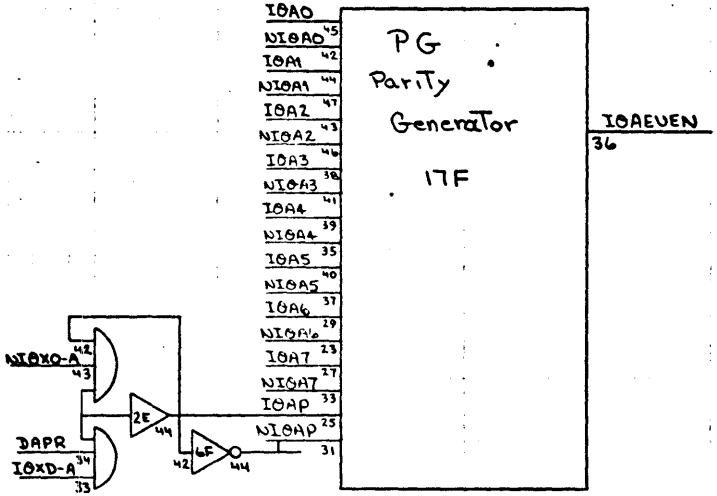
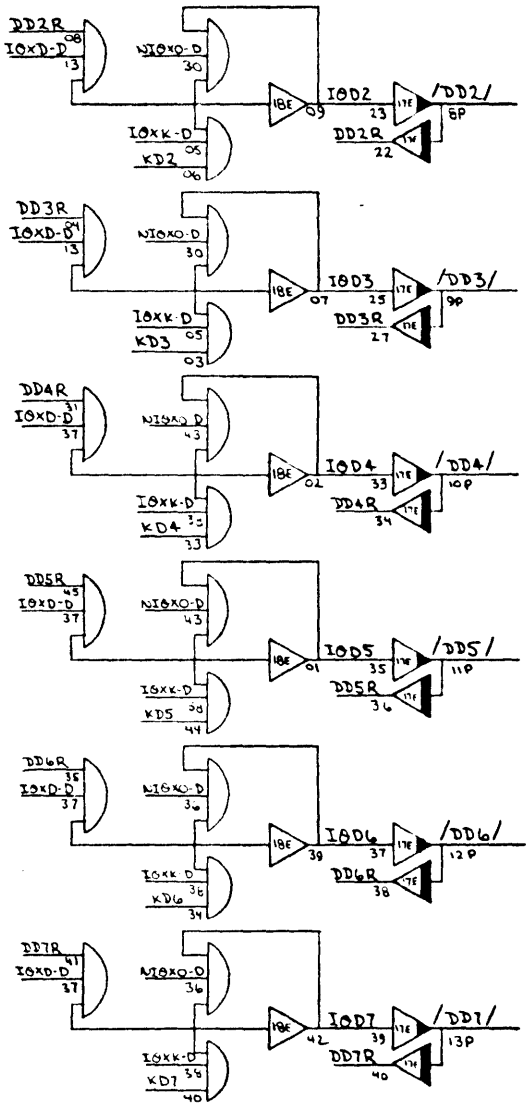


SIOP Rev L
Eric Salamus


IØA0
NIØA0
IØA1
NIØA1
IØA2
NIØA2
IØA3
NIØA3
IØA4
NIØA4
IØA5
NIØA5
IØA6
NIØA6
IØA7
NIØA7
IØAP
NIØAP
PG
Parity
Generator
17F
IØAEVEN
36
NIØXO-A
DAPR
IØXD-A
2E
6F


DD2R
IØXD-D
NIØXO-D
IØXK-D
KD2
18E
IØD2
/DD2/
DD2R
DD3R
IØD3
/DD3/
KD3
DD4R
IØD4
/DD4/
KD4
DD5R
IØD5
/DD5/
KD5
DD6R
IØD6
/DD6/
KD6
DD7R
IØD7
/DD1/
KD7

Signal	Description
BKD	Read backward
CC	Command chain
CD	Count done.
CEI	Channel end interrupt
CM	Chaining modifier.
CME	IOP memory error
CTE	IOP control error
DC	Data chain
DME	Memory data error.
HLT	IOP halt
HTE	Halt on transmission error
I	Interrupt
ICE	Interrupt on channel end
IL	Incorrect length
IUE	Interrupt on unusual end
IZC	Interrupt on zero byte count
MAE	Memory address error
S	Skip
SIL	Suppress incorrect length
TDE	Transmission data error
TEH	Error halt and not term. order
UEI	Unusual end interrupt
ZCI	Zero byte count interrupt

S15:D → S31:D

W0/1:D → W3/1:D

M00/1:D → M31/1:D.

DG:R (14A38)

SXO (25C24)

S reg. (memory address register)

PH00DI (7C06)

+PH05DI +PH12DI, NA16 +PH01DI, BF00

WXO (9A01)

W

WX1 (4A34)

SXCA/BA (18B01)

CXMBO (26B07)

IXMB0 (13A28) IXMB1 (13A37) IXMB2 (13A47) IXMB3 (21C15)

CXMR3 (18B12)

MUXO (11A15)

M reg.

MLXO (17A06)

LS0 = CA
NLS0 = BA

CA/BA (Fast Memory).

F.M. Addressing

CA/BAXC (16C36)

LS1 = FS
NLS1 = BC

FS/BC (Fast memory)

FS/BCXC (18C34)

F.M. Addressing

WJ1, NJ2	MB0XI
WJ1, J2	MB1XI
J1, NJ2	MB2XI
J1, J2	MB3XI

WI+NHI, NH2	IXMB0
NWI, NHI, H2	IXMB1
NWI, HI, NH2	IXMB2
NWI, HI, H2	IXMB3

MB0XI (8A24) MXC (20B45) MB1XI (15A12) MXM (17A45) MB2XI (15A33) MXXS/BC (15A02) MB3XI (15A14)

MXFR (15A46) MXIS/0F (25C37) MXA (15A35) MXDD (1826) MXDC (1818) MXDB (1817) MXFF (15A46)

UNO, UNI, UN2 (8C45), (8C46), 8C03)

MXIS/0F (25C37)
J/M (26C47)
HX0F (19B13)

LS2 = IS
NLS2 = 0F

sets EH

IS/0F (Fast memory)

IS/0FXH (16C14)

DLITO (9847) J (24C34, 24C30) J/M (26C47)

HX0 (20B05) H reg. HLX0 (20B17)

HX0F (19B13)
HXTORD (21C33)

CXMR3 (18B12)
PH06/DLITO (21C02)

ZCI CEI UEI S BKD HTE DC EH. NTORD

HXA (18B35)

(S/DL27) (7D15) DL2

DL2T0 DL2T1 DL2T2 DL2T3 DL2T4

(S/DLIT) (5D15) DLI

9847 DLIT0
9839 DLIT1
9831 DLIT2
9823 DLIT3
9815 DLIT4

SC:R { FNDASC:D

FNC { FNDSIO FNDTIO FNDTDV FNDHIO FNDAIO

PH01/D2 (4C50)
PH00DI (7C06)
PH01DI (7C44)
PH03DI (7809)
PH10DI (7C46)
PH11DI (7845)
PH12DI (7822)
PH13DI (7823)
PH14DI (7824)
PH02DI (7807)
PH04DI (7825)
PH05DI (7834)
PH06DI (7830)
PH07DI (7840)

NCMD AIO WED CBA TRA EM EO EP ZBC.DC

CXCA/CA (18B15) CXMBC (26B07) CXMR3 (18B12) CXSF/BCL (19B14)

IL TCE DME MAE CME CTE HTE CM

CXST (17B10)

CXO (20B18)

C reg. (adder)

.SUB (12B28) .K15 (12B20)

Held by FS reg.

AXO (10C05).

A (address register)

SPA (gates)

AXM (1A46) AXER (16B46)

HXA (16B35) MXA (15A35)

Reg. Selection	
LS0	CA reg.
NLS0	BA reg.
LS1	FS reg.
NLS1	BC reg.
LS2	IS reg.
NLS2	0F reg.

LS

IMB (gates)

IEVEN (28A30)

Parity Check + Generator

IDO→IO7 EP

I CD CC HLT 0XTORD (30A37)

0XE (24B34)

MB0XI → MB3XI

FNC

FNCO:R → FNC2:R

FNCASC:D (14C35) SC:R (32A40)

FNDSIO:D (14C12) FNDTIO:D (14C19) FNDTDV:D (14C23) FNDHIO:D (14C15) FNDAIO:D (14C25)

FR lines

FR0:R → FR7:R

WI

4 Byte Xfer.

MXDD (1826) MXDC (1818) MXDB (1817)

DD0:R → DD7:R DC0:R → DC7:R DB0:R → DB7:R

M08 → M31 to device controller.

0XO (27C01) G (output register)

To device cont.

IXO (18C04) I (input register)

IXDA (11A13) DAP:R → DA7:R

IXMB (24B46)

MIOP/MS Interface

32C DIS00 DIS01 DIS02 DIS03 DIS04 DIS05 DIS06 DIS07 DIS08 DIS09 DIS10 DIS11 DIS12 DIS13 DIS14 DIS15 32C

MIOP with MS INTERNAL REGISTERS

D Revision.

MIOP/MS MODULE LOCATION CHART

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	AT11	FT65	LT13	AT11	LT12	FT27	FT65	FT63	FT63	FT63	FT63	FT63	XT10	FT27	AT11	IT16	AT11	BT11	AT70	LT13	AT61	IT11	AT11	IT11	LT13	XT10	BT16	BT16	IT11	FT26	BT11	FT66
				4B																												
B	XT10	FT18	FT18	FT18	FT18	FT27	BT18	XT10	FT66	BT10	FT65	FT67	IT16	IT11	BT11	IT16	LT11	BT11	AT10	FT26	FT66	FT66	BT11	AT24	FT67	FT65	LT21	BT11	XT10	LT20	BT11	BT15
C		FT26	FT18	FT18	XT10	IT11	LT13	LT13	FT66	IT11	FT26	BT11	LT13	AT11	IT11	IT11	IT11	XT10	AT12	XT10	AT13	IT11	BT17	IT11	LT26	FT66	BT25	IT15	FT66	LT13	IT16	IT11
														4B													BS	BS				
D	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	FT25	XT10	LT20	LT20	IT16	FT66	IT27	LT13	XT10	AT11	HT15	DT11	HT15	DT14	DT14	FT10	FT66	AT11
	2	2	2	2	2	1	1	1	1	1							BS	BS						BS				ABS		ABS		
	MIOP																															

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A		AT56	DT26	AT60	LT89	AT57	LT90	AT83		LT94	LT95	LT26	BT16	AT60	LT71	AT60	FT67	AT11	FT63	AT11	FT63	AT11	FT63	FT63	IT31	BT12	BT31	BT31	BT10	FT66	FT66	FT43
		MS																														

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MIOP Address (LT26 Loc.8C)

S1-1 = Bit 21 → IOPA 0
S2-1 = Bit 22 → IOPA 1
S3-1 = Bit 23 → IOPA 2

LASTONE = S1-2 UP
FOURBYTE = S2-2 UP
AIOP = S3-2 UP

MS Address (LT26 Loc.21A)

S1-1 = Bit 26 → A10
S2-1 = Bit 25 → A09
S3-1 = Bit 24 → A08
S4-1 = Bit 23 → A07
S1-2 = Bit 22 → A06
S2-2 = Bit 21 → A05
S3-2 = Bit 20 → A04
S4-2 = Bit 19 → A03

MS off/on line (LT44 Loc.23A)

S1 Up = on line
S1 Down = off line

Note:

MS Test Mode is not used

S1 Loc.22A must be up.

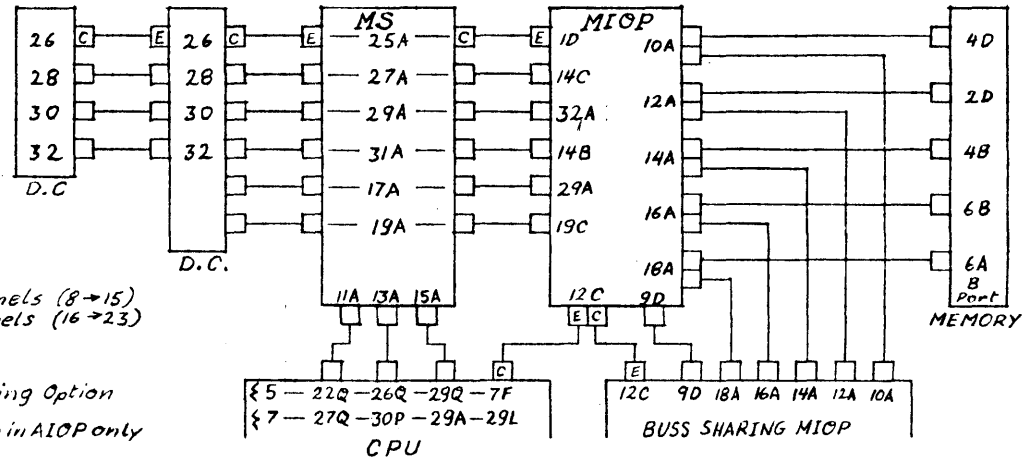
Options

1 = 8 additional channels (8 → 15)
2 = 8 additional channels (16 → 23)

4B = 4 Byte Option

BS = Memory Buss Sharing Option

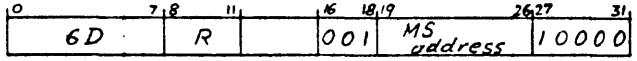
ABS = Buss Sharing Option in AIOP only



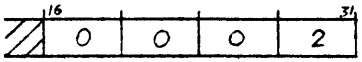
32C

Single Phasing The MIOP.

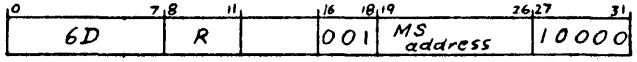
Set MIOP to Single Phase Mode



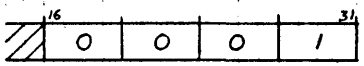
where R=



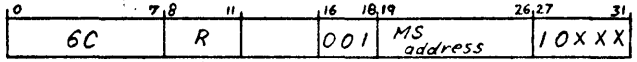
Step to next Phase



where R=



Read MIOP signals



Group 1→7

Group 1

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
PH01/D2	PH01/PD2	PH0CD1	PH0CPD1	PH10D1	PH10PD1	PH11D1	PH11PD1	PH12D1	PH12PD1	PH13D1	PH13PD1	PH14D1	PH14PD1	PR1	PR2

Group 2

PH00D1	PH00PD1	PH01D1	PH01PD1	PH02 D2	PH02PD1	PH03D1	PH03PD1	PH04D1	PH04PD1	PH05D1	PH05PD1	PH06D1	PH06PD1	PH07D1	PH07PD1

Group 3

MAE	MAR	MDR	MPE	MRQ	MS	PRCH	TPE	EH	EHE	DL3CYCLE	AIOP	MCFA	MCFA/1	MCFB	MCFB/1

Group 4

ORD	OUT	WI	FIN	FP	TORD	TRA1	ZBC	FS:D	FSL:R	RS:R	RSA:D	LASTONE	AVO:R		

Group 5

A00	A01	A02	A03	A04	A05	A06	A07	LS0	LS1	LS2	K15	SUB	UNO	UN1	UN2

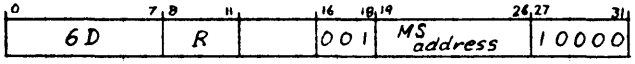
Group 6

H0	H1	H2	H3	H4	H5	H6	H7	CC1	CC2	CMD	IER:D	IR:D	FNC	J1	J2

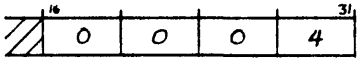
Group 7

C00	C01	C02	C03	C04	C05	C06	C07	C08	C09	C10	C11	C12	C13	C14	C15

Return MIOP to normal mode



where R =



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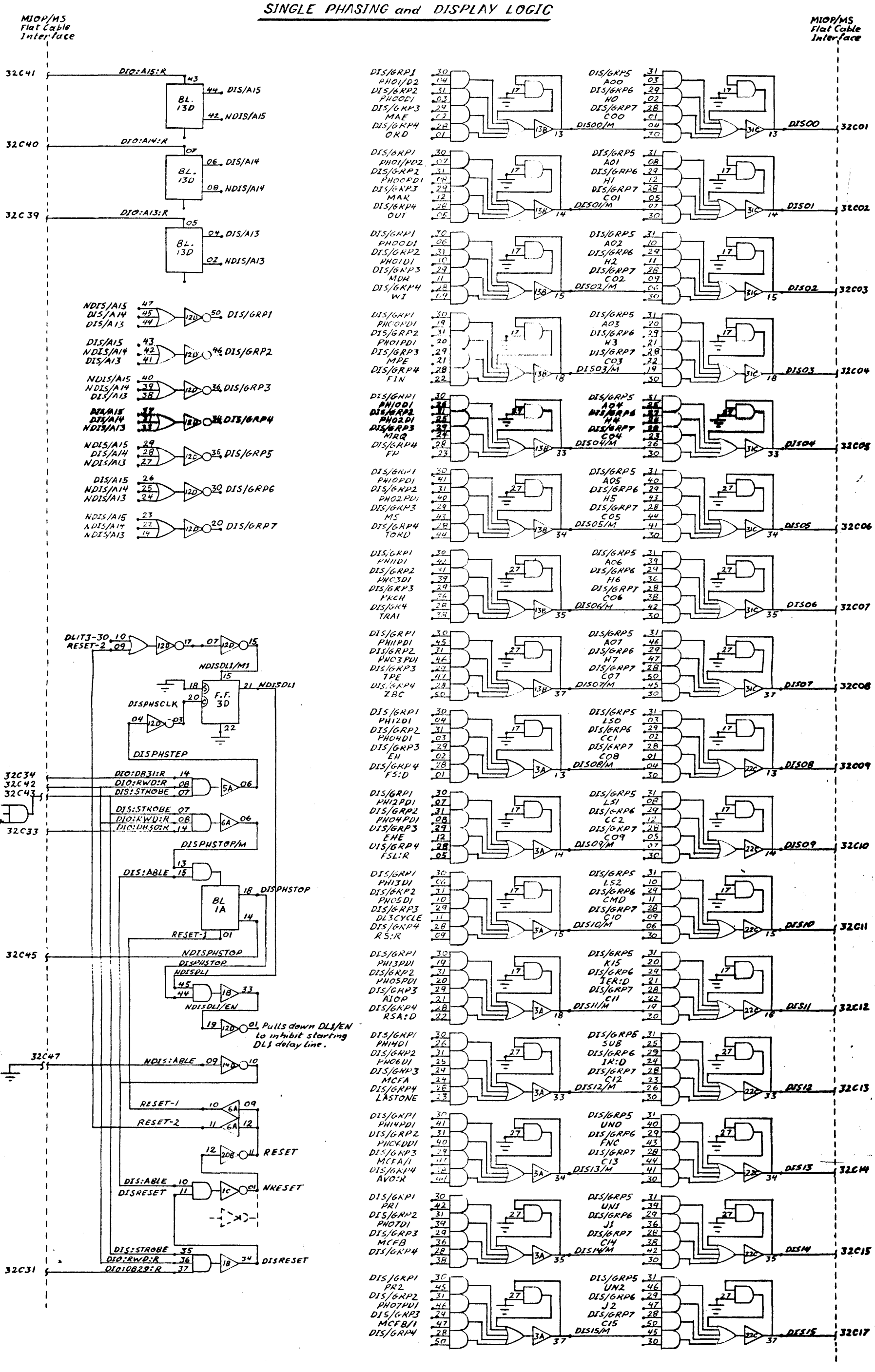
MIOP with MS

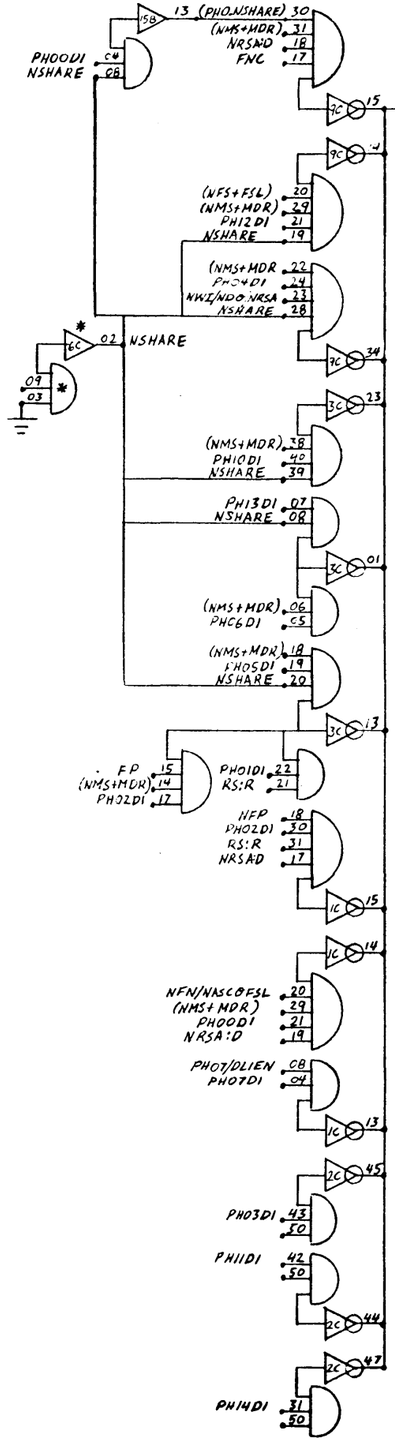
SINGLE PHASING and DISPLAY LOGIC

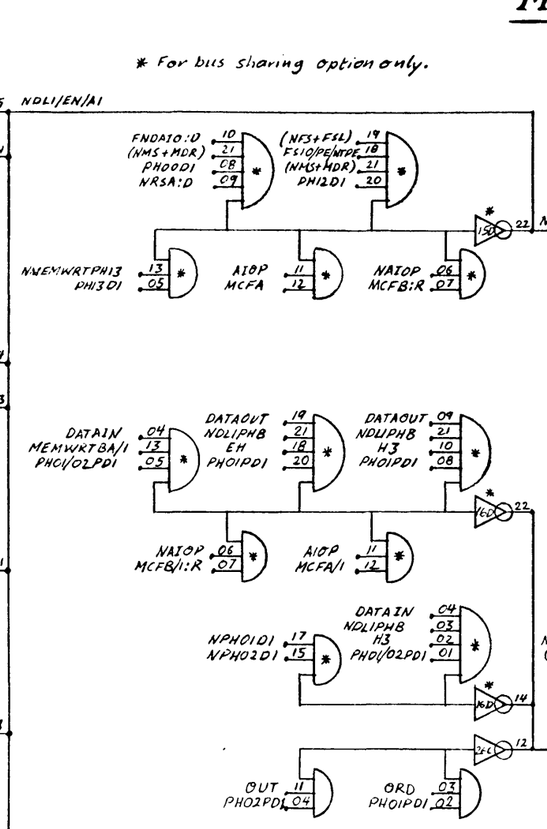


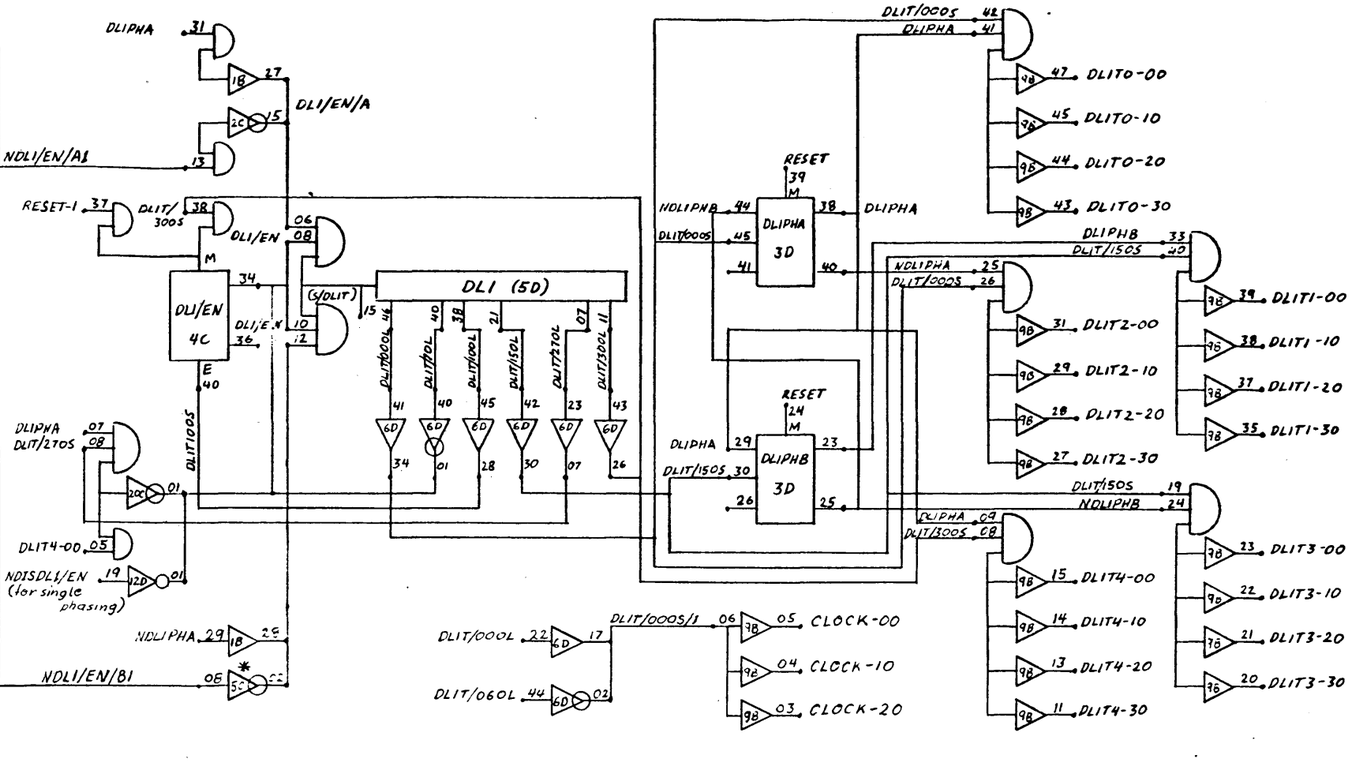
D Revision

MIOP CLOCKS (with MS)

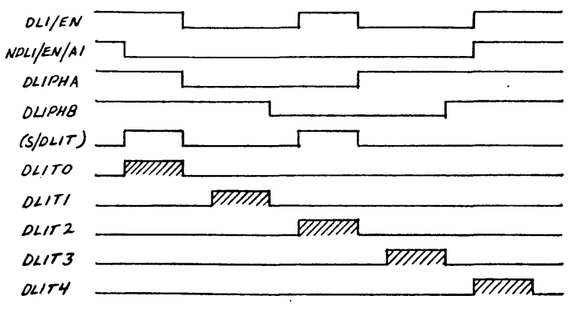
* For bus sharing option only.

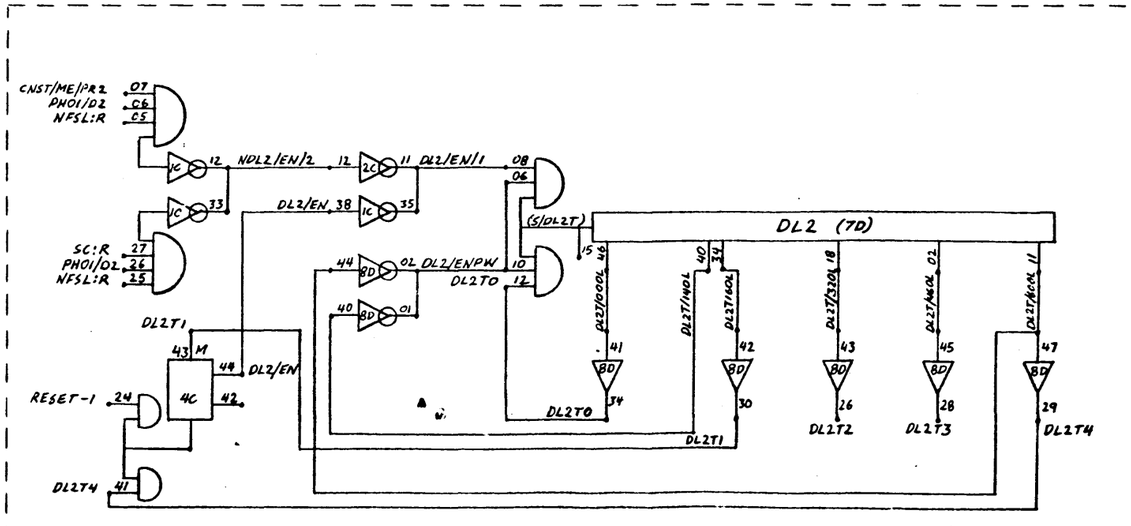






Normal DLI delay line cycle





D Revision

SIO (MIOP with MS)

CPU

CNST:R (12C20)
IOPA0:R (12C08)
IOPA1:R (12C13)
IOPA2:R (12C18)
ENC0:R (12C06)
ENC1:R (12C04)
ENC2:R (12C10)
PR:D (12C45)

PH101/D2 (4C50) : Initiate next operation

PR:D = LASTONE.NME (8C43) (17A18)
(S/DL2T) (7D15) = ME (10C20) = IOP address recognition

DL2T0: FNC (11B06) (8D34) CPU function
DL2T2: FNDSIO:D (14C12) (8D26)
DL2T4: PH00D1 (7C06) (8D29)

FNDSIO:D (14C12)

PH00D1 (7C06) : Access location 20

(S/DLIT) (5D15) = FIN (12B36) = End of previous operation.

DLIT0: S26:D (12A37) (9847) sets Sreg. to location 20
HX0 (20B05) } Clears H reg.
HLX0 (20B17) }
DLIT1: WX0 (9A01) (9839) Clears W0→W3 for read
MS (1A04) = Memory request
CC1 (4C04)
CC2 (4C10)
LS0 (24C46)
LS2 (24C06)
DLIT2: AXM (1A46) (9831) for device address to Arcg.
SUB (12B28)
K15 (12B20)
DLIT3: IXMB (24B46) (9823) IXMBO (13A24) } M00→07 to Ireg
DLIT4: PH10D1 (7C46) (9815)

MQ:D (10A01)

P0K:R (10A27)

PH110D1 (7C46) : Initiate status return and store 1rst status word.

(S/DLIT) (5D15) = MDR (1A30) set with P0K:R = Memory cycle completed.

DLIT0: [M08] = CMD (24B06) (9847) CXCA/BA (17B15) CAreg. to Creg.
[NM08] = CXM (17B27) M16→M31 to Creg.
[M09] = TPE (12B06) 0XI (24B34) Device address to 0 reg.
WX1 (4A34) sets W0→W3 for write
DLIT2: FS:D (14C35) (9831) Creg. -1 to Creg.
DLIT4: MXC (20B44) (9815) for CA-1 to M00→M15
[CMD] = PH11D1 (7B45) MS (1A04)
[NCMD] = PH12D1 (7B22) NLS1 (24C42)

AV0:R resets FS:D

MQ:D (10A01)

FS:D (14C35)

00:D (32A23)
01:D (32A19)
02:D (32A15)
03:D (32A12)
04:D (32A03)
05:D (32A09)
06:D (32A01)
07:D (32A02)
D.C. ADDRESS

AV0:R (1D08)

CMD
NCMD

PH11D1 (7B45)

(S/DLIT) (5D15) = PH11D1 (7B45)

DLIT0: CXM (17B27) (9847) M16→M31 to Creg.
DLIT4: PH12D1 (7B22) (9815) NLS1 (24C42)

NCMD

DR:R (10A10)

PH12D1 (7B22) = Prepare 2nd word of status.

(S/DLIT) (5D15) = (NFS + FSL).(NMS + MDR) (3C36) (4A36)

DLIT0: S31:D (14A19) (9847) to store in location 21
NFIN (12B34)
NK15 (12B22)
DLIT1: MXFR (15A46) (9839) FR lines to M00→M07
MXFS/BC (15A02)
BC reg. to M16→M31
[DOR:R] = NCC1 (4C02) D.C. address recognition
[IOR:R] = NCC2 (4C22) D.C. not busy
[FNDSIO:D] = OUT (12B44) OUT remembers SIO
DLIT2: [NCC1.NCC2] = CA/BAXC (16C36) (9831) Creg. to CA reg.
NFS:D (11B42)
DLIT3: NFNC (11B08) (9823) LS1 (24C44)
[NTPE] = PR:D (20B15) Proceed to CPU
DLIT4: NFNDSIO:D (7C36) (9815) PH01/D2 (4C50)
PH13D1 (7B23)

FSL:R (14B36)
DOR:R (32A38)
IOR:R (14B34)

FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B18)
FR3:R (14B13)
FR4:R (14B08)
FR5:R (14B10)
FR6:R (14B04)
FR7:R (14B06)
STATUS

NCC1=NCOND1:D (1B46)
NCC2=NCOND2:D (2B12)
PR:D (12C45)

Allow next operation to start

PH13D1 (7B23) = Store 2nd status word.

(S/DLIT) (5D15) = PH13D1 (7B23)

DLIT0: CXFS/BCL (19B14) (9847) FS8→FS14 to C8→C14
HXA (18B35)
A04→A07 to H4→H7
H0→H3 is cleared
DLIT2: [NCC1.NCC2] = IS/0FXH (16C14) (9831) Hreg. to IS reg
[TPE] = MS (1A04)
MXC (20B44) operation status to M08→M14
DLIT4: NLS2 (24C08) (9815) PH14D1 (7B24)

MQ:D (10A01)

AR:R (10A08)

PH14D1 (7B24) = Clear 0F and FS reg. and terminate

(S/DLIT) (5D15) = PH14D1 (7B24)

DLIT0: HX0 (20B05) } Clears H reg.
(9847) HLX0 (20B17) }
CX0 (20B18) Clears C reg.
DLIT1: [NCC1.NCC2] = IS/0FXH (16C14) (9839) Clears 0F reg.
FS/BCXC (18B34) Clears FS reg.
DLIT3: FIN (12B36) (9823)

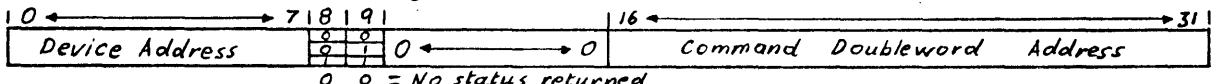
AR:R sets PR:D (12C45)

PR:D (12C45)

MEMORY

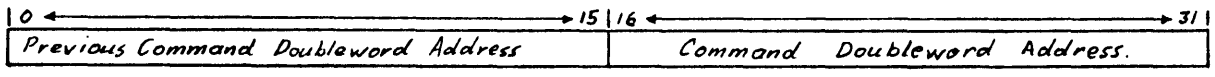
DEVICE CONTROLLER

Location 20 before IOP storage.

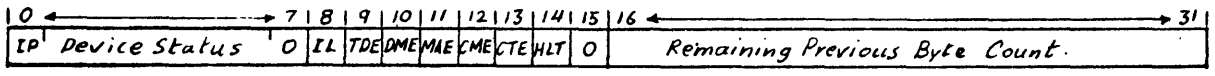


0 0 = No status returned.
0 1 = 1 word of status returned.
1 1 = 2 words of status returned.

Location 20 after 1rst Status word is stored.



Location 21 after 2nd Status word is stored.



CME = IOP Memory Error.
CTE = IOP Control Error
DME = Memory Data Error
HLT = IOP Halt
IL = Incorrect Length
IP = Interrupt Pending
MAE = Memory Address Error
TDE = Transmission Data Error.

Note: Every PH# DI/D2 term is reset at T3 of its delay line.
Every PH# PDI/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

D Revision.

TIO, TDV, HIO (MIOP with MS)

CPU

CNST:R (12C20)
IOPA0:R (12C08)
IOPA1:R (12C13)
IOPA2:R (12C18)
ENC0:R (12C06)
ENC1:R (12C04)
ENC2:R (12C10)
PR:D (12C45)

PH01/D2 (4C50) = Initiate next operation

PR:D = LASTONE.NM2 (8C43) (17A18)
(S/DL2T) (7D15) = ME (10C20) = IOP address recognition.

DL2T0: FNC (11B06) (8D34) CPU function

DL2T2: for TIO FNDTIO:D (14C19) (8D26) for TDV FNDTDV:D (14C23) for HIO FNDHIO:D (14C15)

DL2T4: PH00D1 (7C06) (8D29)

or FNDTIO:D (14C19)
or FNDTDV:D (14C23)
or FNDHIO:D (14C15)

PH100D1 (7CC6): Access location 20

(S/DL1T) (5D15) = FIN (12B36) = End of previous operation

DL1T0: S26:D (12A??) (9B47) Sets S reg. to Location 20
HX0 (20B05) } clears H reg.
HLX0 (20B17) }

DL1T1: WX0 (9A01) (9B39) Clear W0 → W3 for read
MS (1A04) = Memory request
CC1 (4C04)
CC2 (4C20)
LS0 (24C46)
LS1 (24C44)
LS2 (24C06)

DL1T2: AXM (1A46) (9B31) for device address to Areg.
SUB (12B26)
K15 (12B20)

DL1T3: IXMB (24B46) (9B23) IXMB0 (13A24) } for M00 → 07 to I reg.

DL1T4: PH10D1 (7C46) (9B15)

MQ:D (10A01)

PH10D1 (7C46) = Initiate status return and store 1rst status word.

POK:R (10A27)
MQ:D (10A01)

(S/DL1T) (5D15) = MDR (1A30) set with POK:R = Memory cycle completed.

DL1T0: [M0B] = CMD (24B06) (9B47) CXCA/BA (17B15) CA reg to C reg.
[NM0B] = CXFS/BCL (19B14) FS8 → FS14 to C reg.
[M09] = TPE (12B06)
0XI (24B34) Device Address to 0 reg.
WX1 (4A34) sets W0 → W3 for write

DL1T2: FS:D (14C35) (9B31) C reg - 1 to C reg

DL1T4: MXC (20B44) (9B15) for CA-1 to M00 → M15
[CMD] = PH11D1 (7B45) MS (1A04)
[NCMD] = PH12D1 (7B22) NLS1 (24C42)

AV0:R resets FS:D

FS:D (14C35)
00:D (32A23)
01:D (32A19)
02:D (32A15)
03:D (32A12)
04:D (32A03)
05:D (32A09)
06:D (32A01)
07:D (32A02)
D.C. Address

AV0:R (1D08)

CMD
NCMD

PH11D1 (7B45)

(S/DL1T) (5D15) = PH11D1 (7B45)

DL1T0: CXFS/BCL (19B14) (9B47) FS8 → FS14 to C reg.

DL1T4: PH12D1 (7B22) (9B15 NLS1 (24C42)

NCMD

PH12D1 (7B22) = Prepare and store 2nd status word.

DR:R (10A10)
PR:D (12C45)
MQ:D (10A01)
NCC1=NCOND1:D (1B46)
NCC2=NCOND2:D (2B12)

(S/DL1T) (5D15) = (NFS + FSL) . (NMS + MDR) (3C36) (4A36)

DL1T0: S31:D (14A19) (9B47) to store in location 21
NFIN (12B34)

DL1T1: MXFR (15A46) (9B39) FR lines to M00 → M07
MXFS/BC (15A02)
BC reg. to M16 → M31
[DOR:R] = NCC1 (4C02) D.C. Address recognition
[IOR:R] = NCC2 (4C22) D.C. not busy
MXC (20B44) operational status to M08 → M15
[TPE] = MS (1A04)

DL1T2: [NCC1.NCC2] = CA/BAXC (16C36) (9B31) C reg. to CA reg.
NFS:D (11B42)

DL1T3: NFNC (11B06) (9B23) [NTPE] = PR:D (20B15) Proceed to CPU.

DL1T4: if TIO = NFNDTIO:D (9B15) if TDV = NFNDTDV:D if HIO = NFNDHIO:D PH01/D2 (4C50) PH13D1 (7B23)

FSL:R (14B36)
DOR:R (32A38)
IOR:R (14B34)
ER0:R (14B22)
ER1:R (14B20)
ER2:R (14C18)
ER3:R (14B13)
ER4:R (14B08)
ER5:R (14B1C)
ER6:R (14BC4)
ER7:R (14B06)
Status

Allow next operation to start.

PH13D1 (7B23)

PR:D (12C45)
AR:R (10A08)

(S/DL1T) (5D15) = PH13D1 (7B23)

AR:R sets PR:D (12C45)

DL1T4: PH14D1 (7B24) (9B15)

PH14D1 (7B24) = Terminate

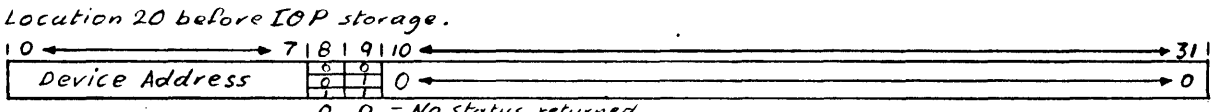
(S/DL1T) (5D15) = PH14D1 (7B24)

DL1T3: FIN (12B36) (9B23)

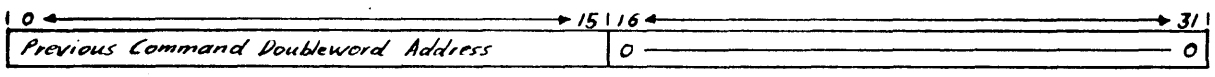
Memory

Device Controller

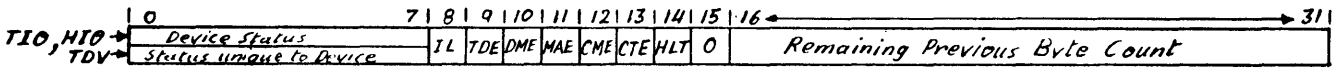
Location 20 before IOP storage.



Location 20 after 1rst Status word is stored.



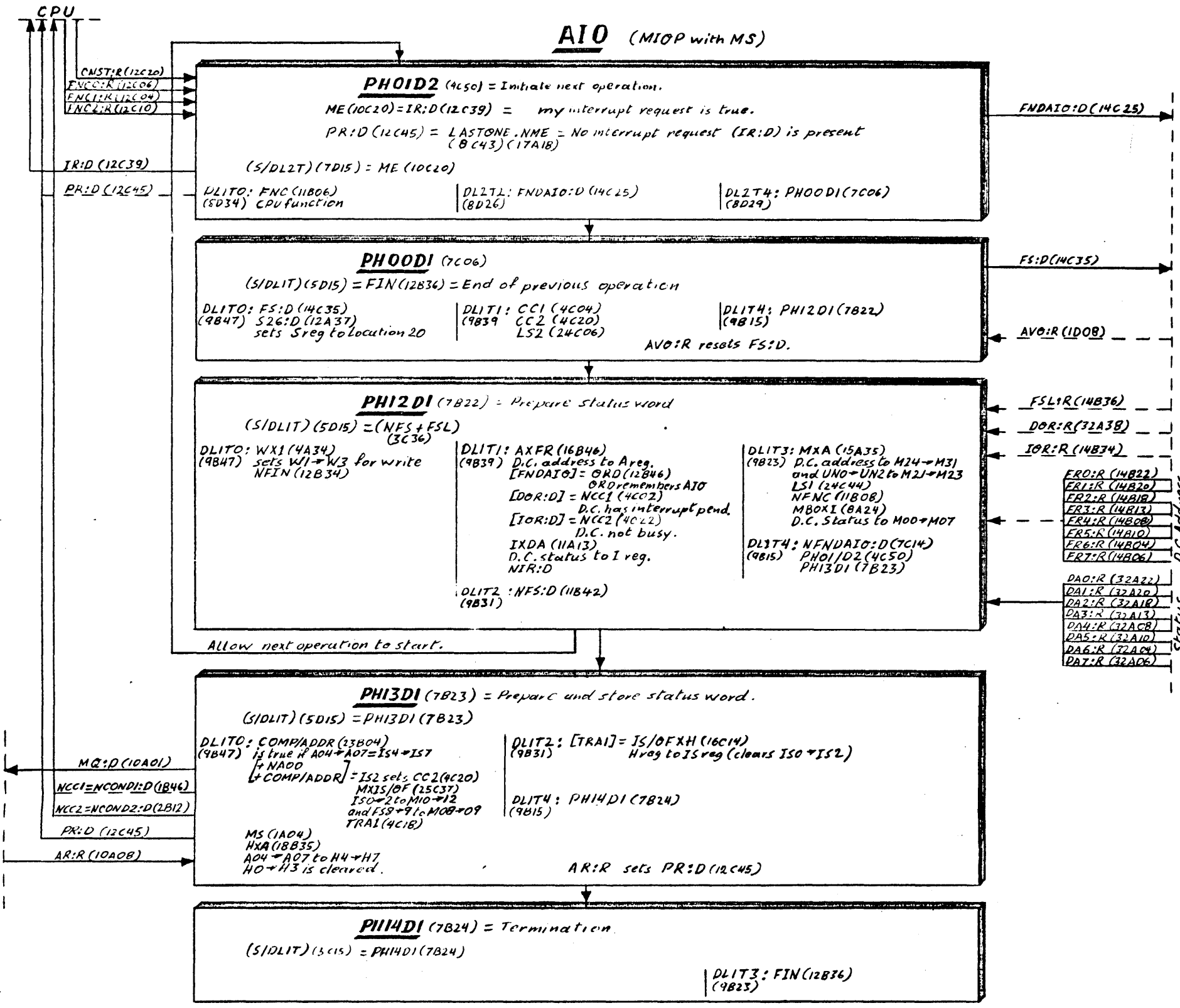
Location 21 after 2nd Status word is stored.



CME = IOP memory error.
CTE = IOP control error
DME = Memory data error
HLT = IOP halt
IL = Incorrect length
MAE = Memory address error
TDE = Transmission data error

Note: Every PH#DI/D2 term is reset at T3 time of its delay line
Every PH#DDI/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

D Revision



Location 20 after responce is stored.

0 ← 7	8	9	10	11	12	13 ← 20	21 ← 23	24	25 ← 27	28 ← 31
Status unique to device	IL	TDE	ZCI	CEI	UEI	0 ← 0	IOP #	M	D.C.	D.
							I.O. Address			

CEI = Channel end interrupt
IL = Incorrect length
TDE = Transmission data error
UEI = Unusual end interrupt.
ZCI = Zero byte count interrupt

D. = if 'M.'=0 then D.= device controller number.
if 'M.'=1 then D.= unit number.
D.C. = multiunit device controller number.
M. = if 0 means single unit device.
if 1 means multiunit device.

Note: Every PH#D1/D2 term is reset at T3 time of its delay line.
Every PH#D1/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

D Revision

ORDER OUT (MIOP with MS)

PH01/D2 (4C50) = Initiate next operation

(S/DL2T) (7D15) = SC:R (32A40).

DL2T2: FNDASC:D (14C33) (8D26)

DL2T4: FS:D (14C35) (8D29) PH00D1 (7C06)

SC:R (32A40)
FNDASC:D (14C33)
ES:D (14C35)

PH00D1 (7C06) = Service connect

(S/DLIT) (5D15) = FIN • (NASC + FSL)
(12B36) (9B33)

DLIT1: AXFR (16B46) (9B39) NCMD (24B08)

DLIT2: NFS:D (11B42) (9B31) K15 (12B20)

DLIT4: [NFNDASC:D] = PH01/D2 (4C50) (9B15) [FNDASC:D] = PH01D1 (7C44)

AV0:R erases FNDASC:D

AV0:R (1D08)
FSL:R (14B36)
FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B18)
FR3:R (14B13)
FR4:R (14B08)
FR5:R (14B10)
FR6:R (14B04)
FR7:R (14B06)
D.C. Address

NFENDASC:D

FNDASC:D

PH01D1 (7C44) = Determine type of service call.

(S/DLIT) (5D15) = RS:R (14B27)

DLIT0: NFIN (12B34) (9B47)

DLIT1: DOR:R marks ORD (12B46) (9B39) IOR:R marks OUT (12B44)
ORDOUT (10B36)
NFENDASC:D (7C22)
[ED:R] = ED:D (32A33)

DLIT2: TORD (24B04) (9B31) NES:D (11B28) LSO (24C46)

DLIT4: PH01/D2 (4C50) (9B15) PH04D1 (7B25)

RS:R (14B27)
DOR:R (32A38)
IOR:R (14B34)
ED:R (32A34)
NES:D (11B28)
ED:D (32A33)

Allow next operation to start.

TRA

ORDOUT

NMS.PH04D1

PH04D1 (7B25) = Access 1st word of command pair

(S/DLIT) (5D15) = NMS (1A02)

DLIT0: SXCA/BA (16B01) (9B47) CA reg to Sreg.
CXCA/BA (17B15)
CA reg. to C reg.
NSUB (12B30)
HX0 (20B05) } clears H reg.
HLX0 (20B17)
[NCMD] = NTRA1 (4C14)
MPE sets FP (12B18)

DLIT1: 1st time through (NFS1S.NEH) sets MS (9B39) 2nd time through (CMD) sets MS
FS1S1S chaining modifier bit.
WX0 (9A01)
clears W0→W3 for read.

DLIT2: Creg.+1 to C reg. (9B31)

DLIT3: [MS+NEH] = CA/BAXC (16C36) (9B25)
C reg to CA reg.
IXMB (24B46) } gates M00→M07
IXMB0 (13A24) } to I reg.
CMD (24B06)

DLIT4: [NMS.NEH] = PH04D1 (7B25) (9B15) [MS+EHJ - PH05D1 (7B34)
[MS] = NK15 (12B22)
NLS1 (24C42)
NLS2 (24C08)

MQ:D (10A01)

MS

NMS

POK:R (10A27)

PH05D1 (7B34) = Access 2nd word of command pair

(S/DLIT) (5D15) = MDR (1A30) set with POK:R = Memory Cycle Completed

DLIT0: [ORD] = 8XI (24B34) (9B47) $31:D (14A19)
if order = 08 = TRA (15A15)
[TRA] = CXM (17B27)
M16→M31 to C reg
[NTRA] = NLS0 (24C50)
CXMR3 (18B13)
M13→M28 to C reg.
M29→31 to H0→H2
[TRA.TRA3] = EH (24B44)

DLIT1: [NTRA.NEH] = MS (1A04) (9B39)
DLIT2: [NTRA+EH] = ORD: READ (9B31) [NEH] = CA/BAXB (16C36)

DLIT4: TRA1 (4C18) (9B15) [TRA] = K15 (12B20)
[TRA.NEH] = PH04D1 (7B25)
[NTRA+EH] = PH06D1 (7B30)

00:D (32A23)
01:D (32A19)
02:D (32A15)
03:D (32A12)
04:D (32A03)
05:D (32A09)
06:D (32A01)
07:D (32A02)
Order

RSA:D (14C03)

TRA

POK:R (10A27)

PH06D1 (7B30) = Process 2nd word.

(S/DLIT) (5D15) = (NMS + MDR) (4A36)

DLIT0: CXM (17B27) (9B47) M16→M31 to C reg.
M07 (=skip) sets H3 (29C05)
Read reverse sets H4 (29C19)
M04 (=HTE) sets H5 (29C25)
M00 (=DC) sets H6 (29C33)

DLIT2: [NEH] = FS/BCXC (18C34) (9B31) C reg to BC reg.
IS/OFXH (16C14)
H reg. to OF reg.
[W1+H2+NCOOT12] = IER:D (14C45)

DLIT4: LS1 (24C44) (9B15) PH07D1 (7B40)

IER:D (14C45)

PH07D1 (7B40) = Termination.

(S/DLIT) (5D15) = RS:R (14B27)

DLIT1: ES:D (14C09) (9B39) EH set 03:D (32A12)

DLIT2: [NEH] = CXMBO (26B07) (9B31) M00→M07 to C00→C07
CXFS/BCL (19B14)
FS0B→FS14 to C0B→C14
MAE sets C11 (29B05)
MPE sets C12 (28B33)
(EH.NMAE.NMPE) sets C13 (28B25)
EH sets C14 (28B19)

DLIT3: FS/BCXC (18C34) (9B23) C reg to FS reg.

DLIT4: RSA:D (14C03) (9B15) FIN (12B36).

RS:R (14B27)
03:D (32A12)
ES:D (14C09)
RSA:D (14C03)
Term. Order

Memory

Device Controller.

Note: Every PH#D1/D2 is reset at T3 time of its delay line.
Every PH#PD1/D2 is set at T1 time of its delay line and reset at T0 time of its delay line.

D Revision

ORDER IN (MIOP with MS)

PH01/D2 (4C50) = Initiate next operation.

(S/DL2T) (7D15) = SC:R (32A40)

DL2T2: FNDASC:D (14C33) (BD26)

DL2T4: FS:D (14C35) (BD29) PH00D1 (7C06)

3C:R (32A40)
FNDASC:D (14C33)
FS:D (14C35)

PH00D1 (7C06) = Service connect.

(S/DL1T) (5C15) = FIN. (NASC + FSL) (12B36) (19B33).

DL1T1: AXFR (16846) (9B39)

DL1T2: NFS:D (11B42) (9B31)
DL1T3: 0F05 sets EHE (12B04) (9B23)

DL1T4: [NFNDASC:0] = PH01/D2 (4C50) (9B15) [FNDASC:D] = PH01D1 (7C44).

AV8:R erases FNDASC:0

AV8:R (1D08)
FSL:R (14B36)
FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B18)
FR3:R (14B17)
FR4:R (14B0A)
FR5:R (14A1C)
FR6:R (14B04)
FR7:R (14B06)
D.C. Address

NFNDASC:D

FNDASC:D

PH01D1 (7C44) = Determine type of service call.

(S/DL1T) (5C15) = RS:R (14B27)

DL1T0: NFIN (12B34) (9B47)

DL1T1: D8R:R marks ORD (12B46) (9B34) ORDIN (10B01)
IXDA (11A13)
DA0:R → DA7.R to I reg
NFNDASC:D (7C22)
[ED:R] = ED:D (32A33)

DL1T2: T0RD (24B04) (9B31) NES:D (11B28)
LS1 (24C44)

DL1T4: 100 marks TPE (12B06) (9B15) [TPE.EHE] = EH (24B44) Data transmisson error.
[NFS06.I01.EHE] = E11 (24B44) Incorrect length error.
LS2 (24C06)
RSA:D (14C03)
PH01/D2 (4C50)
PH07D1 (7B40)

RS:R (14B27)
D0R:R (32A38)
NI0R:R
ED:R (32A34)
DA0:R (32A22)
DA1:R (32A20)
DA2:R (32A18)
DA3:R (32A13)
DA4:R (32A0B)
ED:D (32A33)
RSA:D (14C03)
Order
Device Controller

Allow next operation to start.

PH07D1 (7B40) = Termination.

(S/DL1T) (5C15) = RS:R (14B27)

DL1T0: NK15 (12B22) (9B47)

DL1T1: (9B39) [+FS3.I03 +FS5.I04 +FS5.I03.EH] = 00:D (32A23) Interrupt.
[FS2] = 02:D (32A15) Command chaining.
[EH] = 03:D (32A12) IOP halt.

DL1T2: HX0F (19B13) (9B31) IS reg to H reg.
[FS3.I03] = H1 (30C19) Channel End int.
[+FS5.I04 +FS5.I03.EH] = H2 Unusual End Int.
CXFS/BCU (19B39)
CXFS/BCL (19B14)
FS reg. to C reg.
[I01] = C08 (29B33) incorrect length
[TPE] = C09 (29B25) Transmission data error.
[EH] = C14 (28B19) IOP halt.
[I02] = C15 (28B05) Chaining modifier.

DL1T3: IS/8FXH (16C14) (9B23) H reg. to IS reg.
FS/BCXC (18C34) C reg. to FS reg.

DL1T4: RSA:D (14C03) (9B15) FIN (12B36)

RS:R (14B27)
00:D (32A23)
02:D (32A15)
03:D (32A12)
Term. Order
RSA:D (14C03)
ES:D (14C09)

Note: Every PH#D1/D2 is reset at T3 time of its delay line.
Every PH#D1/D2 is set at T1 time of its delay line and reset at T0 time of its delay line.

ORDER

DA0:R = Transmission error
DA1:R = Incorrect length
DA2:R = Chaining modifier
DA3:R = Channel end
DA4:R = Unusual end.

DATA OUT (MIOP with MS)

PH01/D2 (4C50) = Initiate next operation

(S/DL2T) (7D15) = SC:R (32A40)

DL2T2 (8D26): FNDASC:D (14C33)

DL2T4 (8D29): FS:D (14C35) PH00D1 (7C06)

SC:R (32A40)
FNDASC:D (14C33)
FS:D (14C35)

PH00D1 (7C06) = Service Connect

(S/DLIT) (5D15): FIN. (NASC+FSL) (12B36) (19B33)

DLIT1 (9B39): AXFR (16B46) WX0 (9A01) FP (12B18) N(MI) (24B08) NLS0 (24C50) NLS1 (24C42) NLS2 (24C08)

DLIT2 (9B31): NFS:D (11B42) SUB (12B28) K15 (12B20)

DLIT4 (9B15): [NFNDASC:D] = PH01/D2 (4C50) [FNDASC:D] = PH01D1 (7C44)

AV0:R erases FNDASC:D

AV0:R (1D08)
FSL:R (14B36)
FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B1B)
FR3:R (14B13)
FR4:R (14B08)
FR5:R (14B10)
FR6:R (14MC4)
FR7:R (14B06)
D.C. Address

NFNDASC:D

FNDASC:D

PH01D1 (7C44) = Access data word

(S/DLIT) (5D15): RS:R (14B27)

DX4 → ZY(a000) → WI (14B42) for 4 byte interface

DLIT0 (9B47): SXCA/BA (18B01) BA reg to S15 → S3C NFIN (12B34) HX0F (19B13)

DLIT1 (9B39): IOR:R marks OUT (12B44) DATAOUT (1B14) NFNDASC:D (7C22) 0F00 sets S31:D (14A19)

DLIT3 (9B23): [NEW.NH3] = MS (1A04) IXMB (24B46) IMB0 → IMB7 to I reg.

DLIT4 (9B15): PH01/D2 (4C50) PH02D1 (7B07)

NH1.NH2 + WI = IXMB0 (13A24)
NH1.H2.NWI = IXMB1 (13A37)
H1.NH2.NWI = IXMB2 (13A47)
H1.H2.NWI = IXMB3 (21C15)
selected M reg. Byte to IMB0 → IMB07

ZY(a000) = DX4)
RS:R (14B27)
NDOR:R
IOR:R (14B34)
ED:R (32A34)

MQ:D (10A01)

Allow next operation to start.

NED:D

POK:R (10A27)

PH02D1 (7B07) = Output phase.

(S/DLIT) (5D15) = FP.MDR ← 1st time through
NFP.RS:R ← 2nd time through

DLIT0 (9B47): OXI (24B34) EH + ZBS sets ED:D (32A33) CXFS/BCL (19B14) CXFS/BCU (19B35) BC reg to Creg HX0F (19B13)

DLIT1 (9B39): ED:R latches ED:D (32A33) [ED:D.(NEW.NZBS)] = ES:D (14C09) [H1.H2+WI] = WORD/BOUND [WORD/BOUND] = ED:D (32A33) ES:D (14C09) TRA1 (4C18)

DLIT2 (9B31): [NWI] = H0 → H2 +1 → H0 → H2 Creg-1 to Creg. [WI] = H0+1 to H0 Creg-4 to Creg. if byte count = 0 set ZBC (3D07) [EH+ZBS] = ED:D (32A33) NES:D (11B28) TORD (24B04) [NED:D] = RSA:D (14C03) [NH1+NH2+NC00T12] = IER:D (14C45)

DLIT3 (9B23): NFP (12B14) [NH6.TRA1] = CBA (18C13) [=BC] = LS0 (24C46) IXMB (24B46) IMB0 → IMB7 to I reg. new selected M byte to I reg. FS/BCXC (18C34) Creg to BC reg. IS/0FXH (16C14) H reg. to 0F reg.

DLIT4 (9B15): [ED:D+ZBC+EH] = RSA:D (14C03) [ED:D] = LS1 (24C44) [TORD] = LS7 (24C06) [NED:D] = PH02D1 (7B07) [CBA.NZBC] = PH03D1 (7B09) [H6.ZBC] = PH04D1 (7B25) [(NCBA.ED:D.NZBC)+NH6.ZBC] = PH07D1 (7B40)

OP:D (32A25)
00:D (32A23)
01:D (32A19)
02:D (32A15)
03:D (32A12)
04:D (32A08)
05:D (32A09)
06:D (32A01)
07:D (32A02)
Data
M08 → M31
ED:D (32A33)
ES:D (14C09)
RSA:D (14C03)
IER:D (14C45)
Data
Device Controller.

ED
NED:D
CBA
ZBC.H6

PH03D1 (7B09) = Update byte address.

(S/DLIT) (5D15) = PH03D1 (7B09)

DLIT0 (9B47): CXCA/BA (17B15) BA reg. to C reg. NSUB (12B30)

DLIT1 (9B39): no error marks FP (12B18)

DLIT2 (9B31): Creg + 1 to Creg.

DLIT3 (9B23): CA/BAXC (16C36) Creg to BA reg. [FP] = FIN (12B36) [NFP] = PH07D1 (7B40)

EH
ZBC.H6

PH04D1 (7B25)
PH05D1 (7B34)
PH06D1 (7B30)
} Same as in Order Out except ORD is low.

EH
ED

PH07D1 (7B40) = Termination

(S/DLIT) (5D15) = (NTORD + RS) (17C36). (NMS + MDR) (4A36)

DLIT0 (9B47): [TORD]: ZBC.FSD1 marks 00:D zero byte count int. ZBC.NFS00 marks 01:D count done EH marks 03:D IOP Halt ES:D (14C09)

DLIT2 (9B31): CXFS/BCL (19B14) FS08 → FS14 to C08 → C14 [NCMD+EH]: CXFS/BCV (19B35) FS00 → 07. FS15 → Creg. [CMD.NEH]: CXMB0 (26B07) M00 → 07 to C00 → 07 CMD means data chained

[MPE+FP] = C10 (29B19)
[MAE] = C11 (29B05)
[MPE.CMD] = C12 (28B33)
[Control error] = C13 (28B26)
[EH] = C14 (28B19)
[TORD] = HX0F (19B13) IS reg to H reg 7BC.FS01 sets H0 (30C25)

DLIT3 (9B23): [TORD] = IS/0FXH (16C14) H reg to IS reg. FS/BCXC (18B34) Creg. to FS reg.

DLIT4 (9B15): [TORD] = RSA:D (14C03) FIN (12B36)

RS:R (14B27)
00:D (32A23)
01:D (32A19)
03:D (32A12)
Term. Ord.
RSA:D (14C03)
ES:D (14C09)

Note: Every PH#D1/D2 term is reset at T3 time of its delay line.
Every PH#D1/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

D Revision

DATA IN (MIOP with MS)

PH01/D2 (4C50) = Initiate next operation

(S/DL2T)(7D15) = SC:R (32A40)

DL2T2 : FNDASC:D (14C33) (BD26)

DL2T4: FS:D (14C35) (BD29) PH00D1 (7C06)

SC:R (32A40)
FS:D (14C35)
FNDASC:D (14C33)

PH00D1 (7C06) = Service connect.

(S/DL1T)(5D15) = FIN.(NASC+FSL) (12B36) (19B33)

DL1T1: AXFR (16B46) (9B39) WX0 (9A01) FP (12B18) NCMD (24B08) NLS0 (24C50) NLS1 (24C42) NLS2 (24C08)

DL1T2: NFS:D (11B42) (9B31) SUB (12B28) K15 (12B20)

DL1T3: OF07 marks EH (24B44) (9B23) OF05 marks EHE (12B04)

DL1T4: [NFNDASC:D] = PH01/D2 (4C50) (9B15) [FNDASC:D] = PH01D1 (7C44)

AV0:R erases FNDASC:D

AV0:R (1D08)
FSL:R (14B36)
FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B18)
FR3:R (14B13)
FR4:R (14B08)
FR5:R (14B10)
FR6:R (14B04)
FR7:R (14B06)

B.C. Address

NFNDASC:D

FNDASC:D

PH01D1 (7C44) = Input phase

(S/DL1T)(5D15) = RS:R (14B27)

DX4 → ZY(a000) → WI (14B42) for 4 byte interface

DL1T0: SXCA/BA (18B01) (9B47) BA reg to S15 → S30 HX0F (19B13) 0F00 marks S31:D (14A19) erase J1 and J2 CXFS/BCL (19B14) CXFS/BCU (19B35) BC reg. to Creg. NFIN (12B34)

DL1T1: (J/M) (26C47) (9B39) 0F01 → 02 to J1 → 2 IXDA (11A13) [+WI, +NH4.W1.H2, +H4.NH1.NH2] = WORD/BOUND [WORD/BOUND] = ED:D (32A33) ES:D (14C09) TRA1 (4C18) ED:R marks ED:D (32A33) NFNDASC:D (7C22) DATAIN (1B15)

DL1T2: [NWI] = if NH4 then H0 → 2+1 to H0 → 2 if H4 then H0 → 2-1 to H0 → 2 Creg-1 to Creg. for Ireg. to selected M byte NJ1.NJ2 = MB0XI (8A24) NJ1.J2 = MB1XI (15A12) J1.NJ2 = MB2XI (15A33) J1.J2 = MB3XI (15A34) MB0XI marks W0 MB1XI marks W1 ect. [WI] = H0 → 2+4 to H0 → 2 Creg.-4 to Creg. WX3 (4A34) sets W0 → W3 MXDB (1B17) MXDC (1B18) MXDD (1B26) byte count: 0 set ZBC (3D07) [EH+ZBS] = ED:D (32A33) NES:D (11B28) TORD (24B04) [NEH.NZBS.ED:D] = ES:D (14C09) [NED.NZBS.NEH] = RSA:D (14C03) [NH1+NH2+NC00T12] = IER:D (14C45)

DL1T3: IS/0FXH (16C14) (9B23) Hreg to 0F reg. FS/BCXC (18C34) Creg to BC reg. NFP (12B14) [+TRA1.NH0.NH4, +TRA1.H0.H4] = CBA (18C13) [(ED+ZBC+EH).NH3] = MS (1A04) [ZBC] = LS0 (24C46)

DL1T4: IEVEN marks TPE (12B06) (9B15) [TPE.EHE] = EH (24B44) [ED:D] = LS1 (24C44) [TORD] = LS2 (24C06) [ED+EH+ZBC] = RSA:D (14C03) PH01/D2 (4C50) [NED:D] = PH02D1 (7B07) [CBA.NZBC] = PH03D1 (7B09) [ZBC.H6] = PH04D1 (7B25) [NCBA.ED:D.NZBC+NH6.ZBC] = PH07D1 (7B40)

ZY(a000) = (DX4)
RS:R (14B27)
NDOR:R
N10R:R
ED:R (32A34)
DA0:R → DA7:R
DB0:R → DB7:R
DC0:R → DC7:R
DD0:R → DD7:R

Data

IER:D (14C45)
RSA:D (14C03)
ED:D (32A33)
ES:D (14C09)

Device Controller.

MQ:D (10A01)

Allow next operation to start.

ZBC.H6

ED:D

CBA

NED:D

NED:D

PH02D1 (7B07) = Input phase

(S/DL1T)(5D15) = RS:R (14B27)

DL1T0: erase J1 and J2 (9B47) HX0F (19B13) CXFS/BCL (19B14) CXFS/BCU (19B35) BC reg. to Creg.

DL1T1: (J/M) = 26C47 (9B39) 0F01 → 0F02 to J1 → J2 IXDA (11A13) [+NH4.W1.H2, +H4.NH1.NH2] = WORD/BOUND [WORD/BOUND] = ED:D (32A33) ES:D (14C09) TRA1 (4C18)

DL1T2: if NH4 then H0 → H2+1 to H0 → H2 (9B31) if H4 then H0 → H2-1 to H0 → H2 Creg.-1 to Creg. for Ireg. to selected M byte. NJ1.NJ2 = MB0XI (18A24) NJ1.J2 = MB1XI (15A12) J1.NJ2 = MB2XI (15A33) J1.J2 = MB3XI (15A34) MB0XI marks W0 MB1X1 marks W1 ect. byte count = 0 set ZBC (3D07) [EH+ZBS] = ED:D (32A33) NES:D (11B28) TORD (24B04) [NEH.ZBS.ED:D] = ES:D (14C09) [NED.NZBS.NEH] = RSA:D (14C03) [NH1+NH2+NC00T12] = IER:D (14C45)

DL1T3: IS/0FXH (16C14) (9B23) Hreg. to 0F reg. FS/BCXC (18C34) Creg. to BC reg. NFP (12B14) [+TRA1.NH0.NH4, +TRA1.H0.H4] = CBA (18C13) [(ED+ZBC+EH).NH3] = MS (1A04) [ZBC] = LS0 (24C46)

DL1T4: [IEVEN.PC:R] = TPE (12B06) (9B15) [TPE.EHE] = EH (24B44) [ED:D] = LS1 (24C44) [TORD] = LS2 (24C06) [ED+EH+ZBC] = RSA:D (14C03) [NED:D] = PH02D1 (7B07) [CBA.NZBC] = PH03D1 (7B09) [ZBC.H6] = PH04D1 (7B25) [NCBA.ED:D.NZBC+.NH6.ZBC] = PH07D1 (7B40)

RS:R (14B27)
ED:R (32A34)
DA0:R (32A22)
DA1:R (32A20)
DA2:R (32A18)
DA3:R (32A13)
DA4:R (32A08)
DA5:R (32A10)
DA6:R (32A04)
DA7:R (32A06)

Data

PC:R (32A36)
IER:D (14C45)
RSA:D (14C03)
ED:D (32A33)
ES:D (14C09)

Memory.

MQ:D (10A01)

CBA

CBA

PH03D1 (7B09) = Update byte address

(S/DL1T)(5D15) = PH03D1 (7B09)

DL1T0: CXCA/BA (17B15) (9B47) BA reg. to C reg. NSUB (12B30)

DL1T2: Creg+1 to Creg (9B31)

DL1T3: CA/BAXC (16C36) (9B23) Creg to BA reg

DL1T4: PH07D1 (7B40) (9B15)

ZBC.H6

PH04D1, PH05D1, PH06D1 (7B25) (7B34) (7B30) = Same as in Order Out except ORD is low.

PH07D1 (7B40) = Termination.

(S/DL1T)(5D15) = (NTORD+RS)(17C36).(NMS+MDR)(4A36)

DL1T0: [TORD]: ZBC.FS01 marks 00:D zero byte count int. ZBC.NFS00 marks 01:D count done FS2 marks 02:D command chain. EH marks 03:D IOP halt (9B47) ES:D (14C09)

DL1T2: CXFS/BCL (19B14) (9B31) FS08 → FS14 to C08 → C14 [NCMD+EH] = CXFS/BCU (19B35) FS00 → 07, FS15 to Creg. [CMD.NEH] = CXMB0 (26B07) M00 → M07 to C00 → 07 CMD = data chained. [TPE] = C9 (29B25) [MPE] = C10 (29B19) [MAE] = C11 (29B05) [MPE.CMD] = C12 (28B33) [=H] = C14 (28B19) [TORD] = HX0F (19B13) IS reg to H reg. ZBC.FS0 sets H0 (30C25) [NTORD] = HX0F (19B13) 0F reg. to H reg. EH sets H7 (30C33)

DL1T3: [TORD] = IS/0FXH (16C14) (9B23) H reg. to IS reg [NTORD] error = IS/0FXH (16C14) H reg. to 0F reg [+TORD] +error = FS/BCXC (18B34) C reg. to FS reg.

DL1T4: FIN (12B36) (9B15) [TORD] = RSA:D (14C03)

DR:R (10A10)

RS:R (14B27)

00:D (32A23)
01:D (32A19)
03:D (32A12)

Term. Ord.

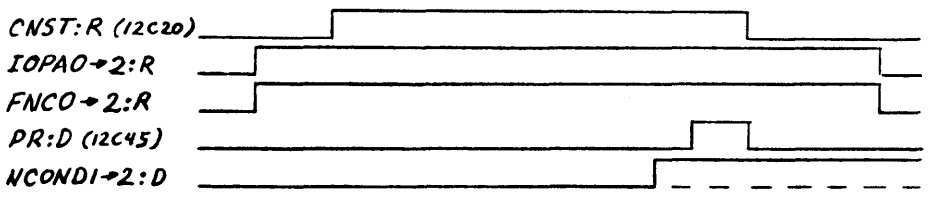
RSA:D (14C03)
ES:D (14C09)

Note: Every PH#D1/D2 term is reset at T3 time of its delay line.
Every PH#PD1/D2 term is set at T1 time of its delay line and reset at T0 time of its delay line.

D Revision.

MIOP Interfaces (with MS)

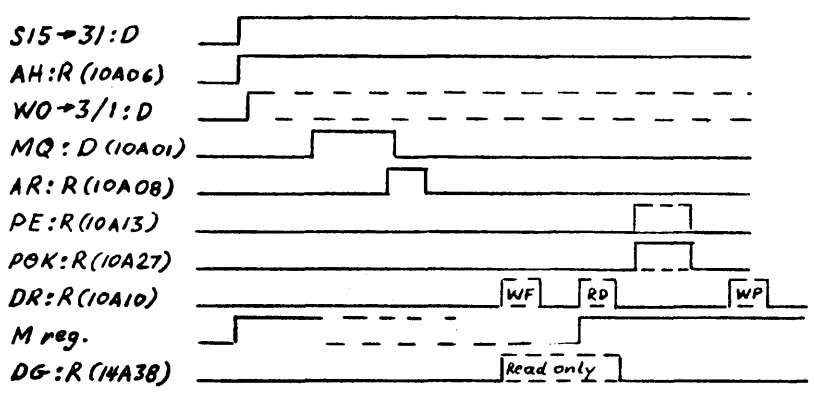
CPU / MIOP



IOPA0:R (12C08) FNC0:R (12C06)
IOPA1:R (12C13) FNC1:R (12C04)
IOPA2:R (12C18) FNC2:R (12C10)

NCOND1:D (12C25) W0/1:D (14A23)
NCOND2:D (12C33) W1/1:D (14A25)
W2/1:D (14A33)
W3/1:D (14A35)

MEMORY / MIOP



S reg. (memory address register)

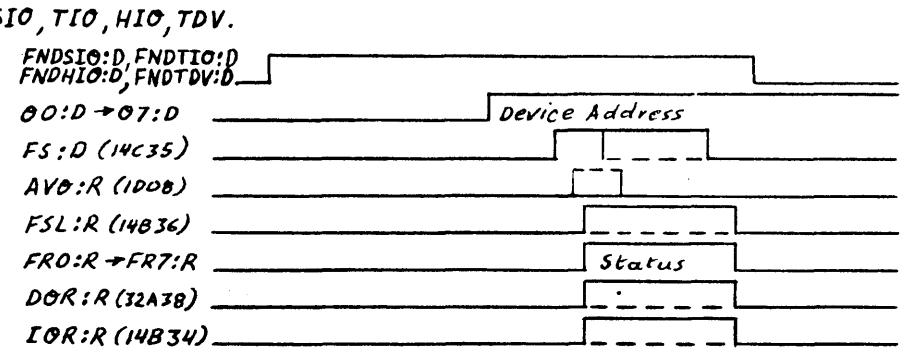
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
12A01	12A02	12A03	12A09	12A12	12A15	12A19	12A23	12A25	12A33	12A35	12A37	12A39	12A45	14A12	14A15	14A19

M register.

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
21A15	21A14	21A15	21A18	21A33	21A35	21A34	21A37	22A15	22A14	22A15	22A18	22A33	22A35	22A34	22A37	23A13	23A14	23A15	23A18	23A33	23A35	23A34	23A37	24A13	24A14	24A15	24A18	24A33	24A35	24A34	24A37

DEVICE CONTROLLER / MIOP

SIO, TIO, HIO, TDV.

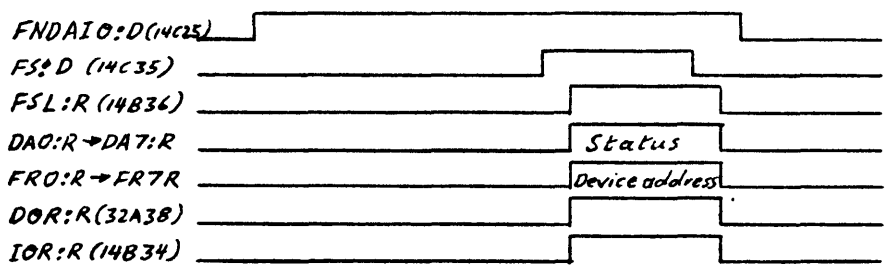


FNDSIO:D (14C12)
FNDTIO:D (14C19)
FNDTDV:D (14C23)
FNDHIO:D (14C15)
FNDAIO:D (14C25)

DATA

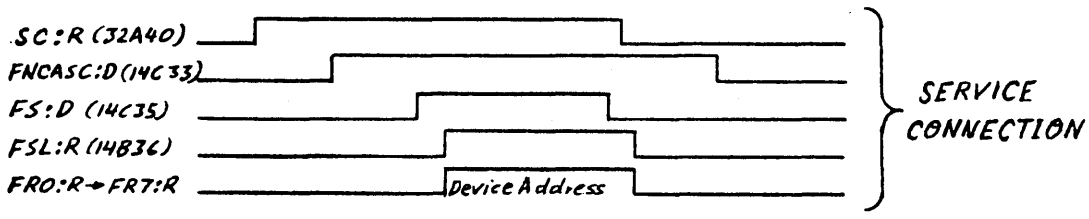
OUT		IN	
OP:D	32A25	DAP:R	32A27
00:D	32A23	DA0:R	32A22
01:D	32A19	DA1:R	32A20
02:D	32A15	DA2:R	32A18
03:D	32A12	DA3:R	32A13
04:D	32A03	DA4:R	32A08
05:D	32A09	DA5:R	32A10
06:D	32A01	DA6:R	32A04
07:D	32A02	DA7:R	32A06
M08	19C02	DB0:R	19C06
M09	19C01	DB1:R	19C09
M10	19C04	DB2:R	19C10
M11	19C03	DB3:R	19C08
M12	19C12	DB4:R	19C13
M13	19C15	DB5:R	19C18
M14	19C19	DB6:R	19C20
M15	19C23	DB7:R	19C22
M16	19C33	DC0:R	19C34
M17	19C35	DC1:R	19C36
M18	19C37	DC2:R	19C38
M19	19C39	DC3:R	19C40
M20	29A02	DC4:R	29A06
M21	29A01	DC5:R	29A04
M22	29A09	DC6:R	29A10
M23	29A03	DC7:R	29A08
M24	29A15	DD0:R	29A18
M25	29A19	DD1:R	29A20
M26	29A23	DD2:R	29A22
M27	29A25	DD3:R	29A27
M28	29A33	DD4:R	29A34
M29	29A35	DD5:R	29A36
M30	29A37	DD6:R	29A38
M31	29A39	DD7:R	29A40

AIO



FR0:R (14B22)
FR1:R (14B20)
FR2:R (14B18)
FR3:R (14B13)
FR4:R (14B08)
FR5:R (14B10)
FR6:R (14B04)
FR7:R (14B06).

SERVICE CYCLE

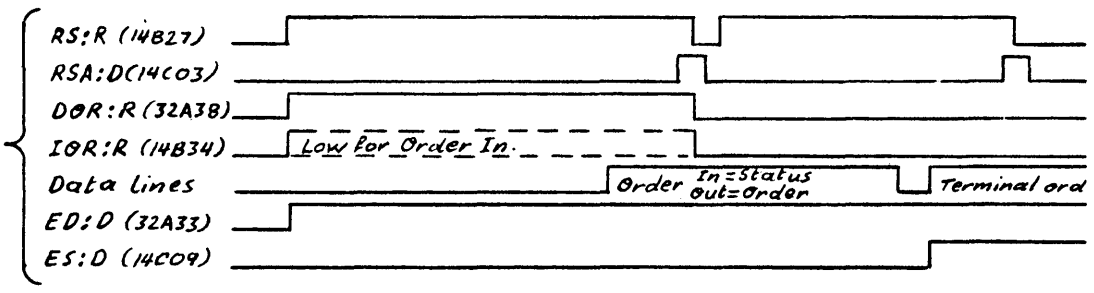


MIOP/MS

DIS00	32C01
DIS01	32C02
DIS02	32C03
DIS03	32C04
DIS04	32C05
DIS05	32C06
DIS06	32C07
DIS07	32C08
DIS08	32C09
DIS09	32C10
DIS10	32C11
DIS11	32C12
DIS12	32C13
DIS13	32C14
DIS14	32C15
DIS15	32C17
DIO:DB29:R	32C31
DIO:DB30:R	32C33
DIO:DB31:R	32C34
DIO:AI3:R	32C39
DIO:AI4:R	32C40
DIO:AI5:R	32C41
DIO:RWD:R	32C42
DIS:STROBE	32C43
NDISPWSTOP	32C45
NDIS:ABLE	32C47

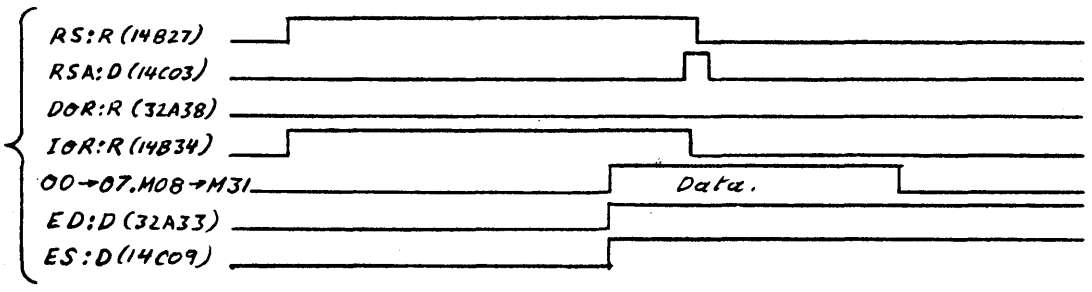
ORDER OUT + ORDER IN

Note: Order In and Out always has a terminal order.



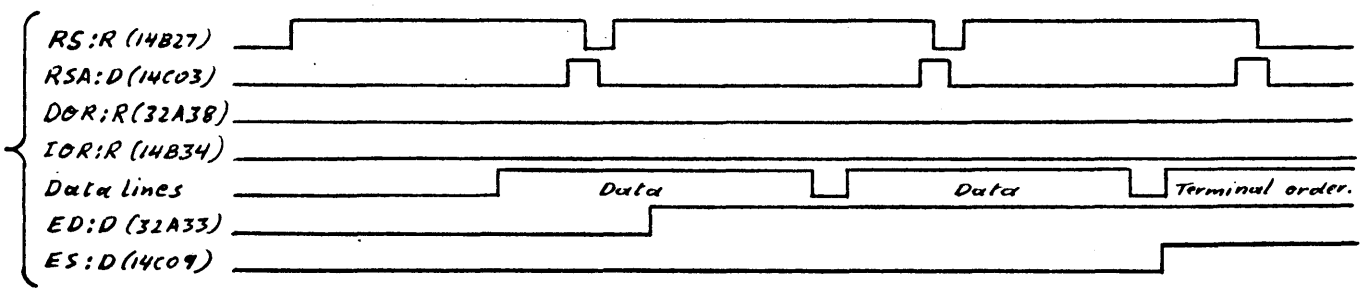
DATA OUT

Using 4byte interface



DATA IN

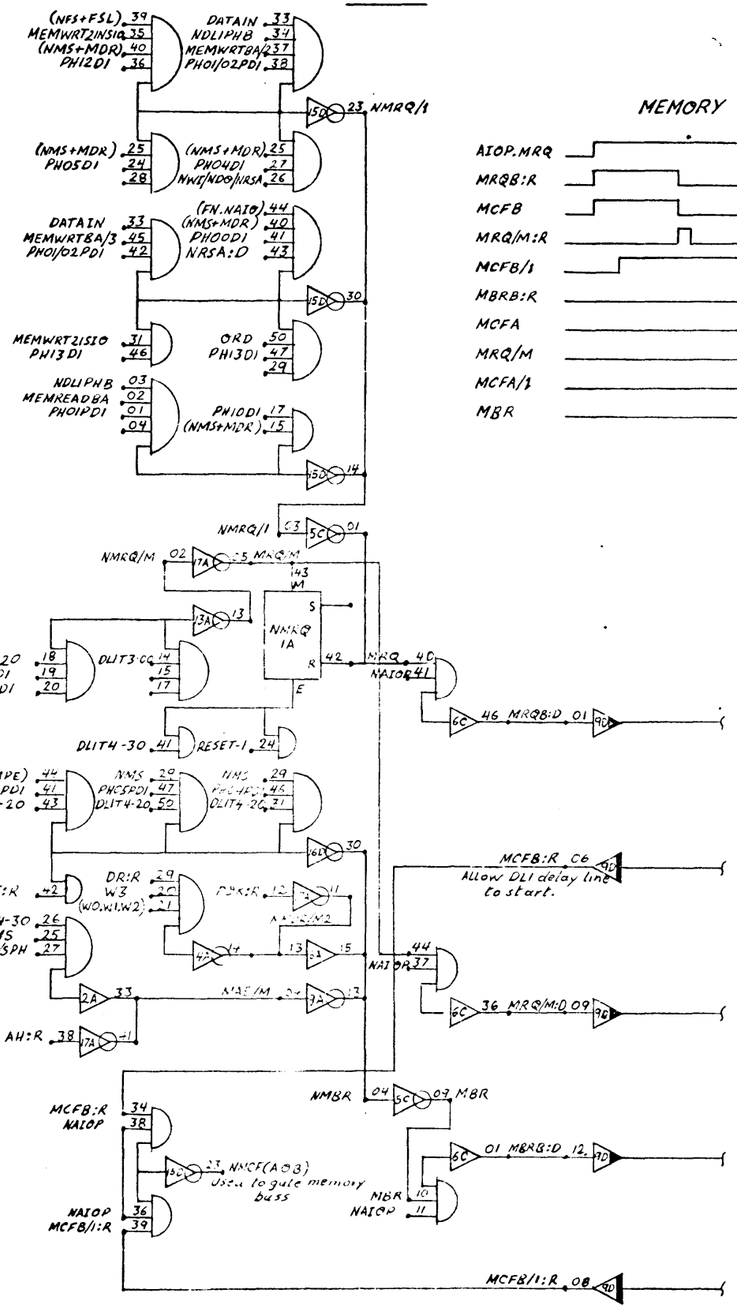
Using 1byte interface 2nd data byte reaches zero byte count (ZBC)



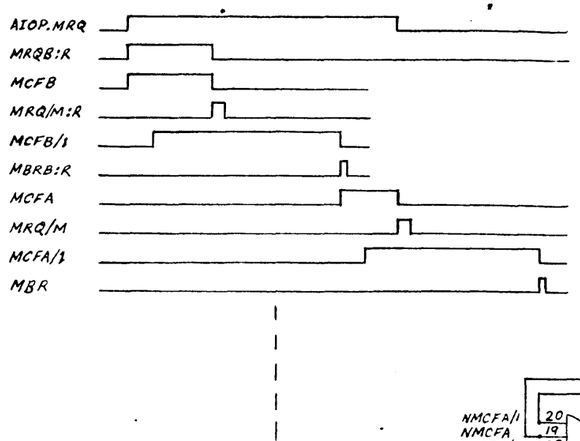
D Revision.

MIOP with MS – BUSS SHARING OPTION

NAIOP



MEMORY CONTROL TIMING



AIOP

D Revision

Page 7-135/5-136A

DECIMAL UNIT

PHASE CHARTS

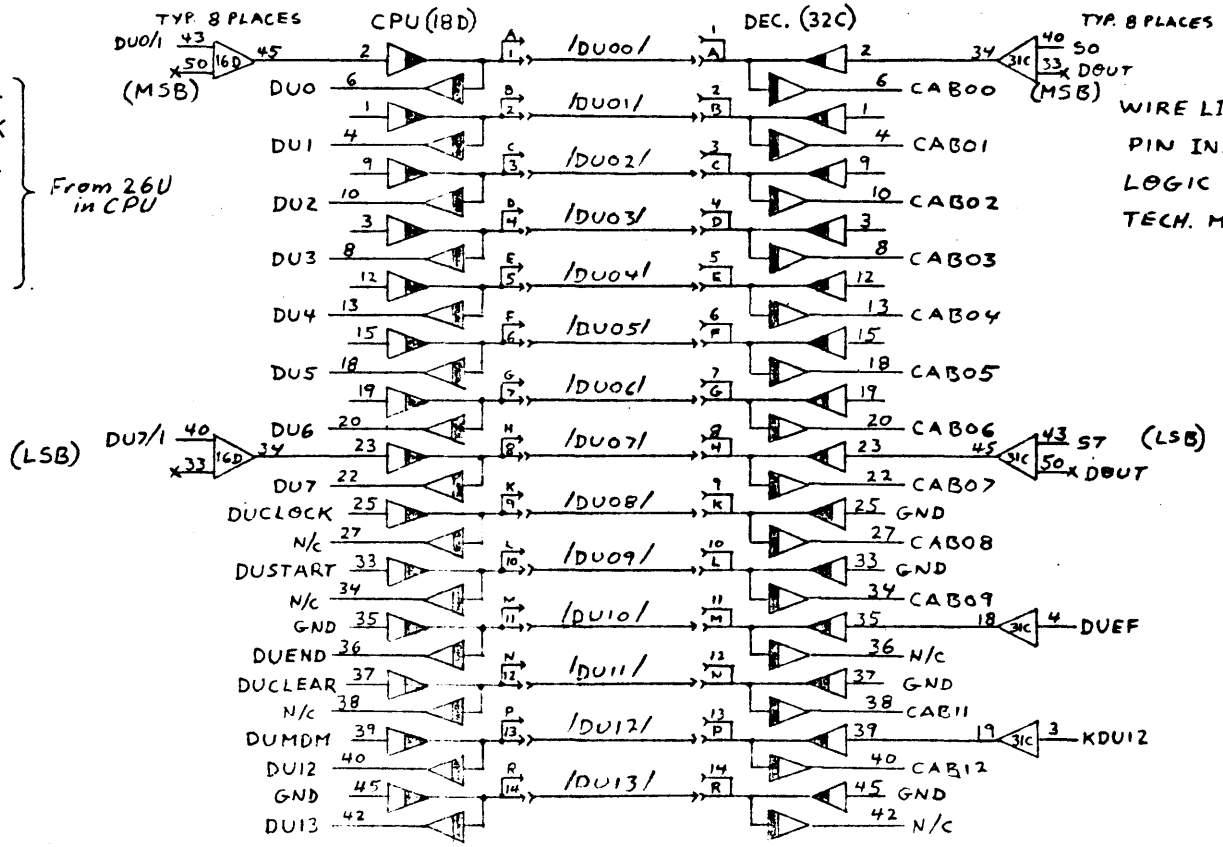
COCHRANE 10/30/6?

DECIMAL UNIT MOD. 8419

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	LT 21	BT 11	GT 11	FT 22	GT 11	LT 21	LT 21	FT 18	XT 10	LT 21	FT 18	BT 18	LT 21	BT 10	LT 21	LT 21	LT 21	FT 25 DA0 ↓ DA7	FT 25 DB0 ↓ DB7	FT 25 ED0 ↓ ED7	BT 10	IT 16	FT 18	LT 21	XT 10	GT 11	FT 22	GT 11	GT 11	LT 21	BT 18	IT 25	A
B	ZT 23 CL's CK	LT 21	LT 21	LT 21	FT 18	XT 10	LT 21	IT 16	BT 11	BT 10	FT 26	FT 17	FT 17	LT 21	LT 21	LT 21	IT 15	LT 21	BT 18	FT 17	FT 17	BT 18	BT 10	FT 22	GT 11	LT 21	XT 10	BT 11	BT 11	LT 21	IT 16	LT 21	B
C	AT 11	BT 16	LT 12	LT 12	LT 12	LT 12	LT 18	XT 10	BT 10	IT 16	LT 12	LT 12	LT 18	LT 21	LT 21	LT 20	LT 12	LT 21	BT 11	FT 22	GT 11	FT 22	BT 11	IT 16	IT 25								C
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

CLOCKS COAX

32B01 →	25A01	CL	From 26U in CPU
32B03 →	13A13	CK	
32E07 →	8A01	CL	
32B10 →	21B01	CL	
32B14 →	12B01	CL	
32B18 →	13C01	CL	



WIRE LIST 124822-001
PIN INDEX 124822-903
LOGIC EQU 124821-001
TECH. MAN. 901587A

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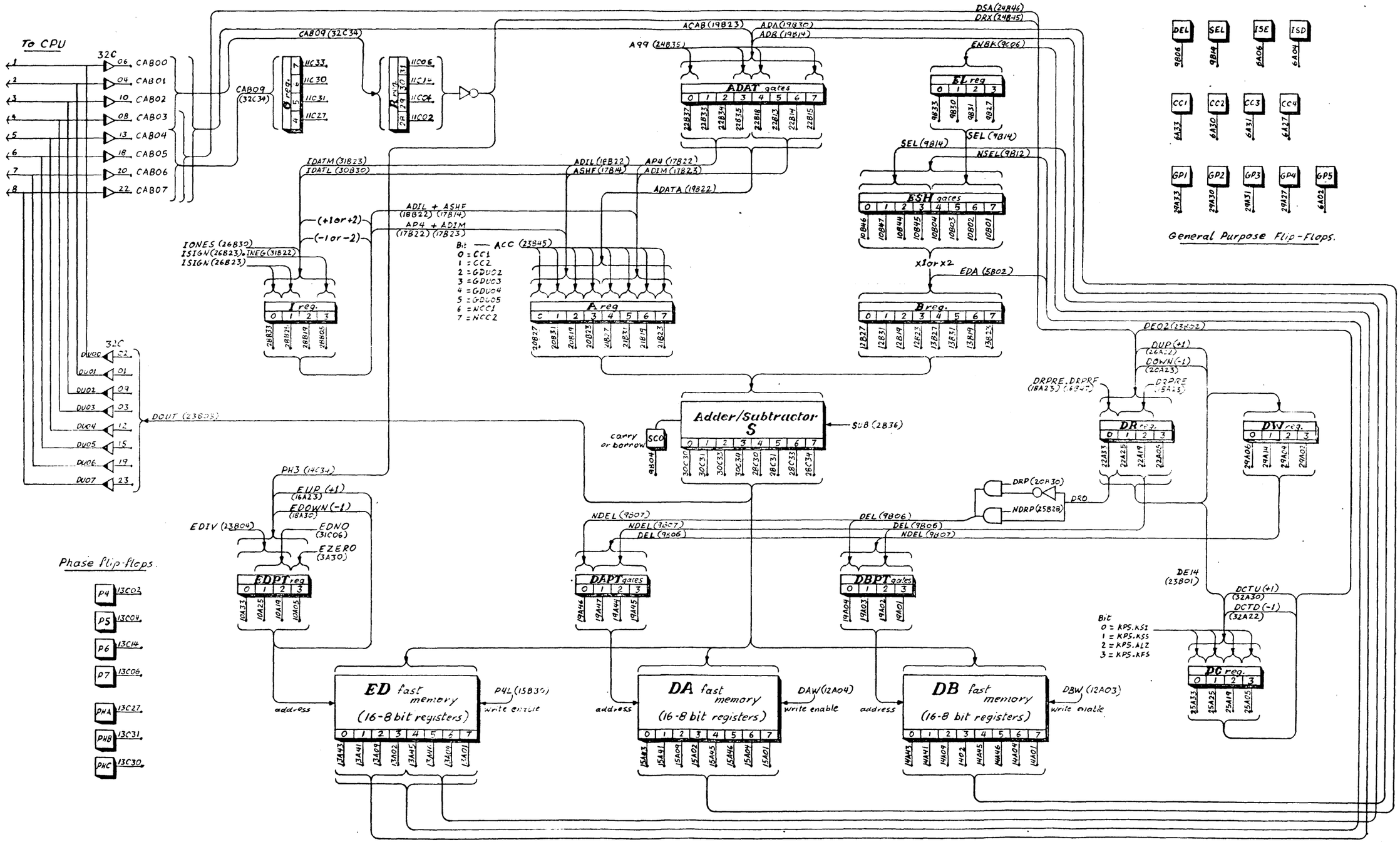
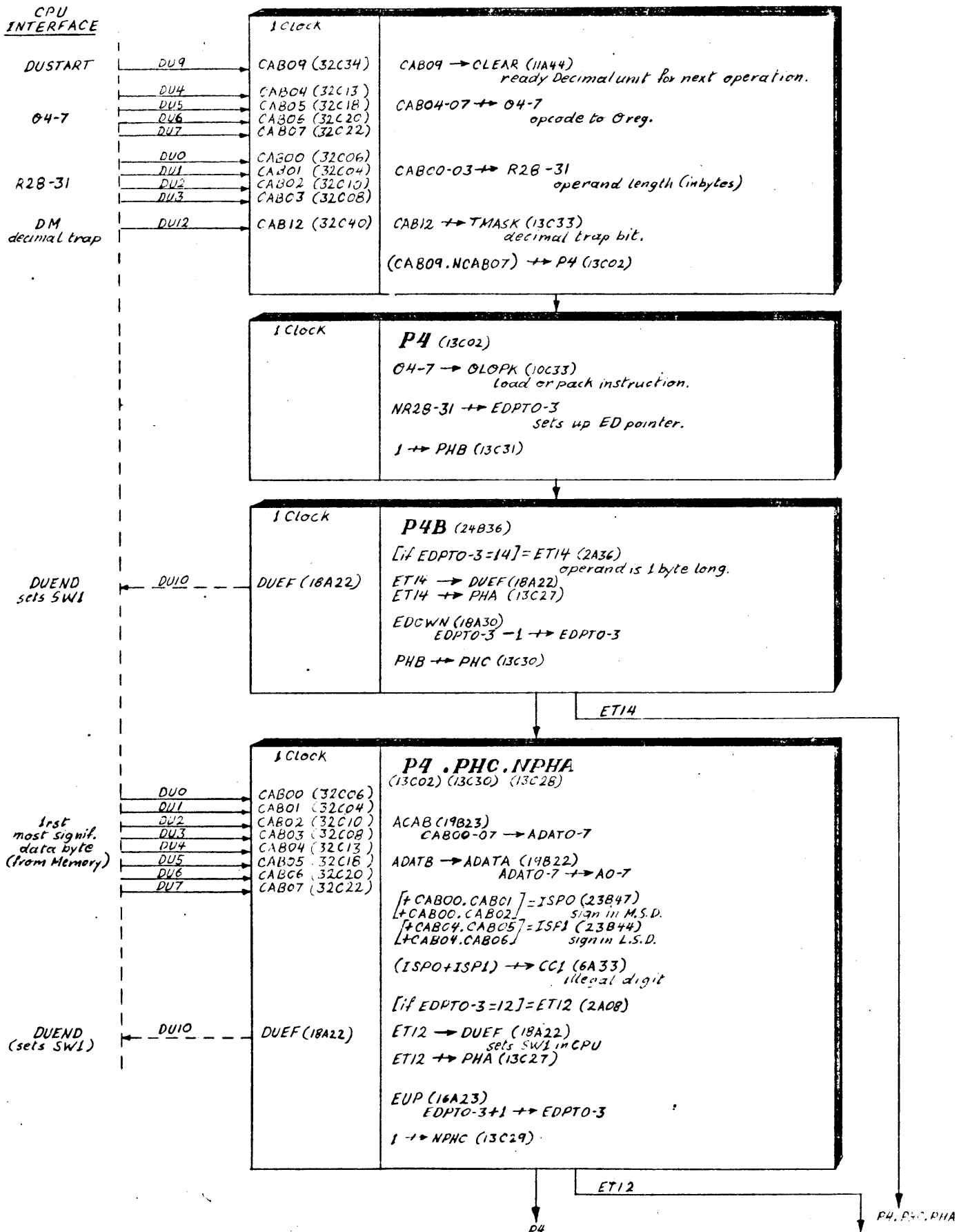
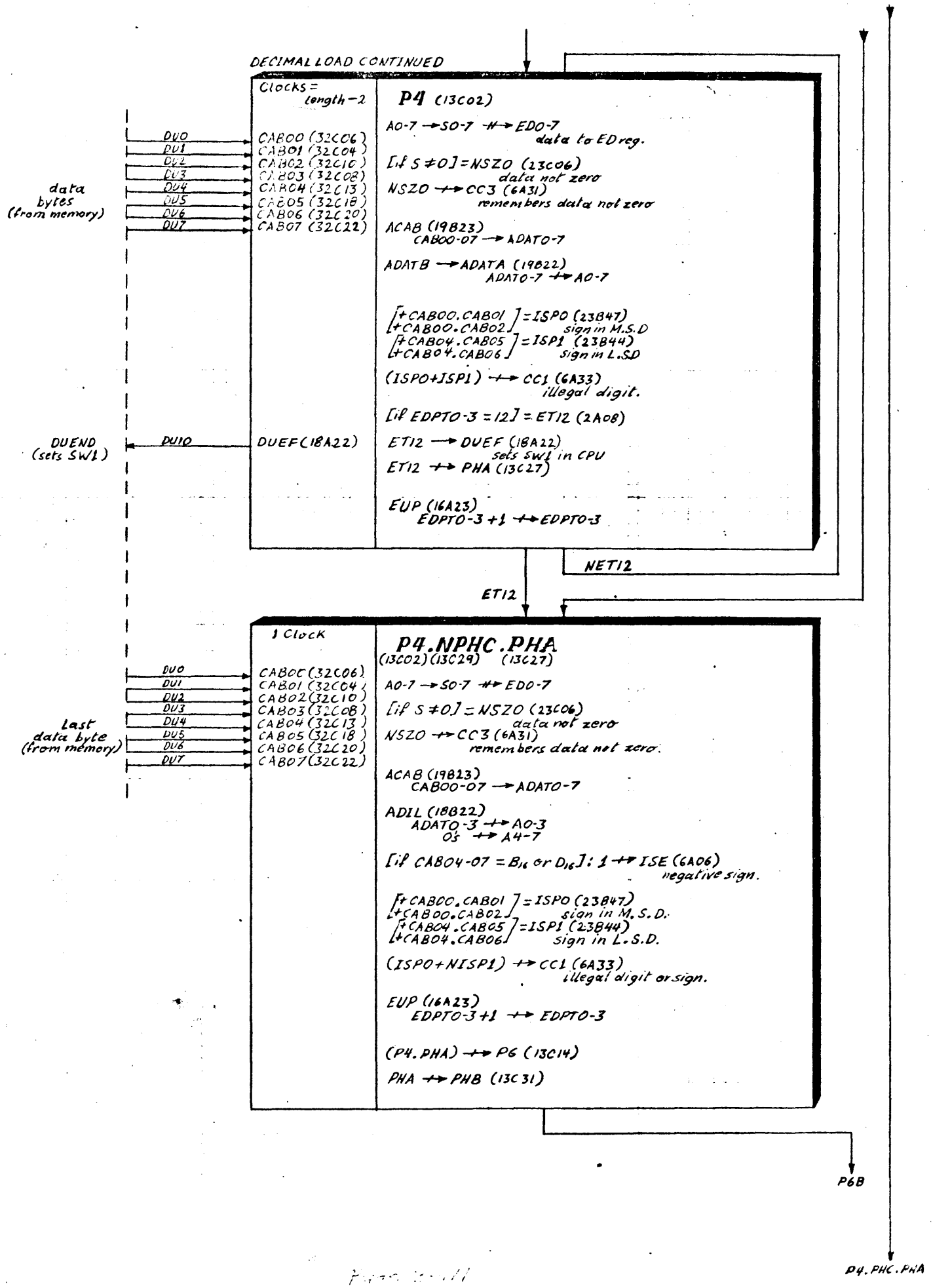
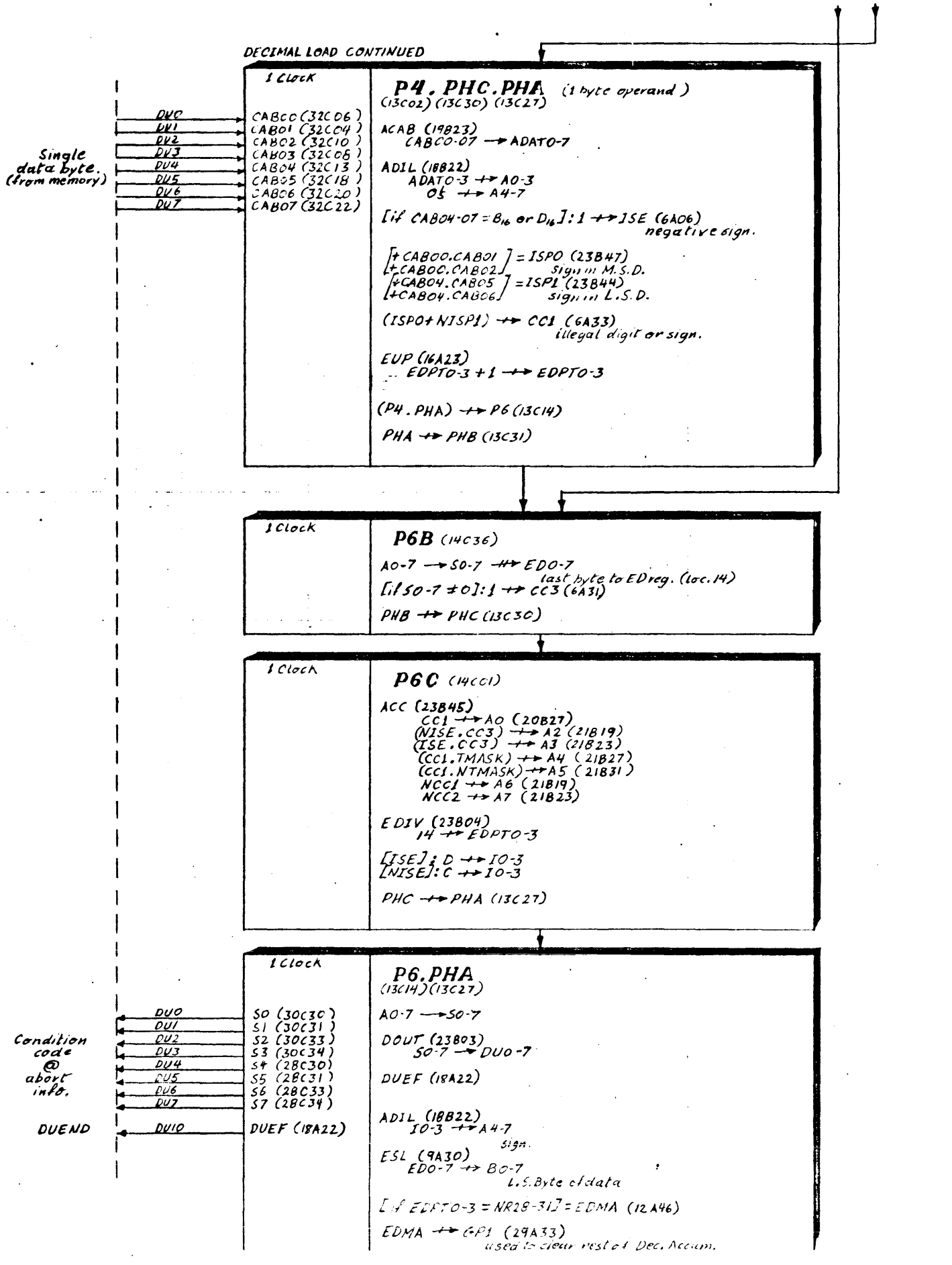
DECIMAL UNIT REGISTERS



DECIMAL LOAD (7E)




DECIMAL LOAD CONTINUED
Clocks = length − 2
P4 (13C02)
A0-7 → S0-7 ↔ ED0-7
data to ED reg.
[if S ≠ 0] = NSZ0 (23C06)
data not zero
NSZ0 ↔ CC3 (6A31)
remembers data not zero
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATB → ADATA (19B22)
ADAT0-7 ↔ A0-7
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47)
sign in M.S.D
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44)
sign in L.S.D
(ISP0+ISP1) ↔ CC1 (6A33)
illegal digit.
[if EDPT0-3 = 12] = ET12 (2A08)
ET12 → DUEF (18A22)
sets SW1 in CPU
ET12 ↔ PHA (13C27)
EUP (16A23)
EDPT0-3 +1 ↔ EDPT0-3
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
data bytes (from memory)
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
DUEND (sets SW1)
DU10
DUEF (18A22)
NET12
ET12
1 Clock
P4.NPHC.PHA
(13C02) (13C29) (13C27)
A0-7 → S0-7 ↔ ED0-7
[if S ≠ 0] = NSZ0 (23C06)
data not zero
NSZ0 ↔ CC3 (6A31)
remembers data not zero.
ACAB (19B23)
CAB00-07 → ADAT0-7
ADIL (18B22)
ADAT0-3 ↔ A0-3
0s ↔ A4-7
[if CAB04-07 = B16 or D16]: 1 ↔ ISE (6A06)
negative sign.
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47)
sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44)
sign in L.S.D.
(ISP0+NISP1) ↔ CC1 (6A33)
illegal digit or sign.
EUP (16A23)
EDPT0-3 +1 ↔ EDPT0-3
(P4.PHA) ↔ P6 (13C14)
PHA ↔ PHB (13C31)
Last data byte (from memory)
P6B
P4.PHC.PHA


DECIMAL LOAD CONTINUED
1 Clock
P4. PHC. PHA (1 byte operand)
(13C02) (13C30) (13C27)
Single data byte. (from memory)
DU0 CAB00 (32C06)
DU1 CAB01 (32C04)
DU2 CAB02 (32C10)
DU3 CAB03 (32C08)
DU4 CAB04 (32C13)
DU5 CAB05 (32C18)
DU6 CAB06 (32C20)
DU7 CAB07 (32C22)
ACAB (19B23)
CAB00-07 → ADAT0-7
ADIL (18B22)
ADAT0-3 → A0-3
05 → A4-7
[if CAB04-07 = B16 or D16]: 1 → ISE (6A06)
negative sign.
[+CAB00.CAB01] = ISP0 (23B47)
[+CAB00.CAB02] sign in M.S.D.
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB06] sign in L.S.D.
(ISP0+NISP1) → CC1 (6A33)
illegal digit or sign.
EUP (16A23)
EDPT0-3 + 1 → EDPT0-3
(P4. PHA) → P6 (13C14)
PHA → PHB (13C31)
1 Clock
P6B (14C36)
A0-7 → S0-7 → EDO-7
last byte to EDreg. (loc. 14)
[if S0-7 ≠ 0]: 1 → CC3 (6A31)
PHB → PHC (13C30)
1 Clock
P6C (14CC1)
ACC (23B45)
CC1 → A0 (20B27)
(NISE.CC3) → A2 (21B19)
(ISE.CC3) → A3 (21B23)
(CC1.TMASK) → A4 (21B27)
(CC1.NTMASK) → A5 (21B31)
NCC1 → A6 (21B19)
NCC2 → A7 (21B23)
EDIV (23B04)
14 → EDPT0-3
[ISE]: D → I0-3
[NISE]: C → I0-3
PHC → PHA (13C27)
1 Clock
P6. PHA
(13C14)(13C27)
Condition code @ abort info.
DU0 S0 (30C30)
DU1 S1 (30C31)
DU2 S2 (30C33)
DU3 S3 (30C34)
DU4 S4 (28C30)
DU5 S5 (28C31)
DU6 S6 (28C33)
DU7 S7 (28C34)
DUEND DU10 DUEF (18A22)
A0-7 → S0-7
DOUT (23B03)
S0-7 → DU0-7
DUEF (18A22)
ADIL (18B22)
I0-3 → A4-7
sign.
ESL (9A30)
EDO-7 → B0-7
L.S.Byte of data
[if EDPT0-3 = NR28-31] = EDMA (12A46)
EDMA → GP1 (29A33)
used to clear rest of Dec. Accum.

DECIMAL LOAD CONTINUED

EDOWN (18A30)
EDPTO-3 −1 →→ EDPTO-3

(P6. PHA) →→ P7 (13C06)

PHA →→ PHB (13C31)

1 Clock

P7. PHB
(13C06) (13C31)

	DU0	S0 (30C30)
	DU1	S1 (30C31)
	DU2	S2 (30C33)
	DU3	S3 (30C34)
1rst least signif. data byte to R15	DU4	S4 (28C30)
	DU5	S5 (28C31)
	DU6	S6 (28C33)
	DU7	S7 (28C33)

B0-3 → S0-3
A4-7 → S4-7

DOUT (23B03)
S0-7 → DU0-7

[NGP1] = ESL (9A30)
EDO-7 →→ BO-7

[GP1]: 0's →→ BO-7
to clear Dec. Accum.

[if EDPTO-3 = NR28-31] = EDMA (12A46)

EDMA →→ GP1 (29A33)
used to clear rest of Dec. Accum.

EDOWN (18A30)
EDPTO-3 −1 →→ EDPTO-3

14 Clocks

P7 (13C06)

	DU0	S0 (30C30)
	DU1	S1 (30C31)
	DU2	S2 (30C33)
Data or 0's to CPU fast memory.	DU3	S3 (30C34)
	DU4	S4 (28C30)
	DU5	S5 (28C31)
	DU6	S6 (28C33)
	DU7	S7 (28C34)

BO-7 → SO-7

DOUT (23B03)
SO-7 → DU0-7

[NGP1] = ESL (9A30)
EDO-7 →→ BO-7

[GP1]: 0's →→ BO-7
to clear Dec. Accum.

[if EDPTO-3 = NR28-31] = EDMA (12A46)

EDMA →→ GP1 (29A33)
used to clear rest of Dec. Accum.

[if EDPTO-3 = 15] = ET15 (2A37)
M.S.Byte in EDreg.

ET15 →→ PHA (13C27)

ET15

NET15

1 Clock

P7. PHA
(13C06) (13C27)

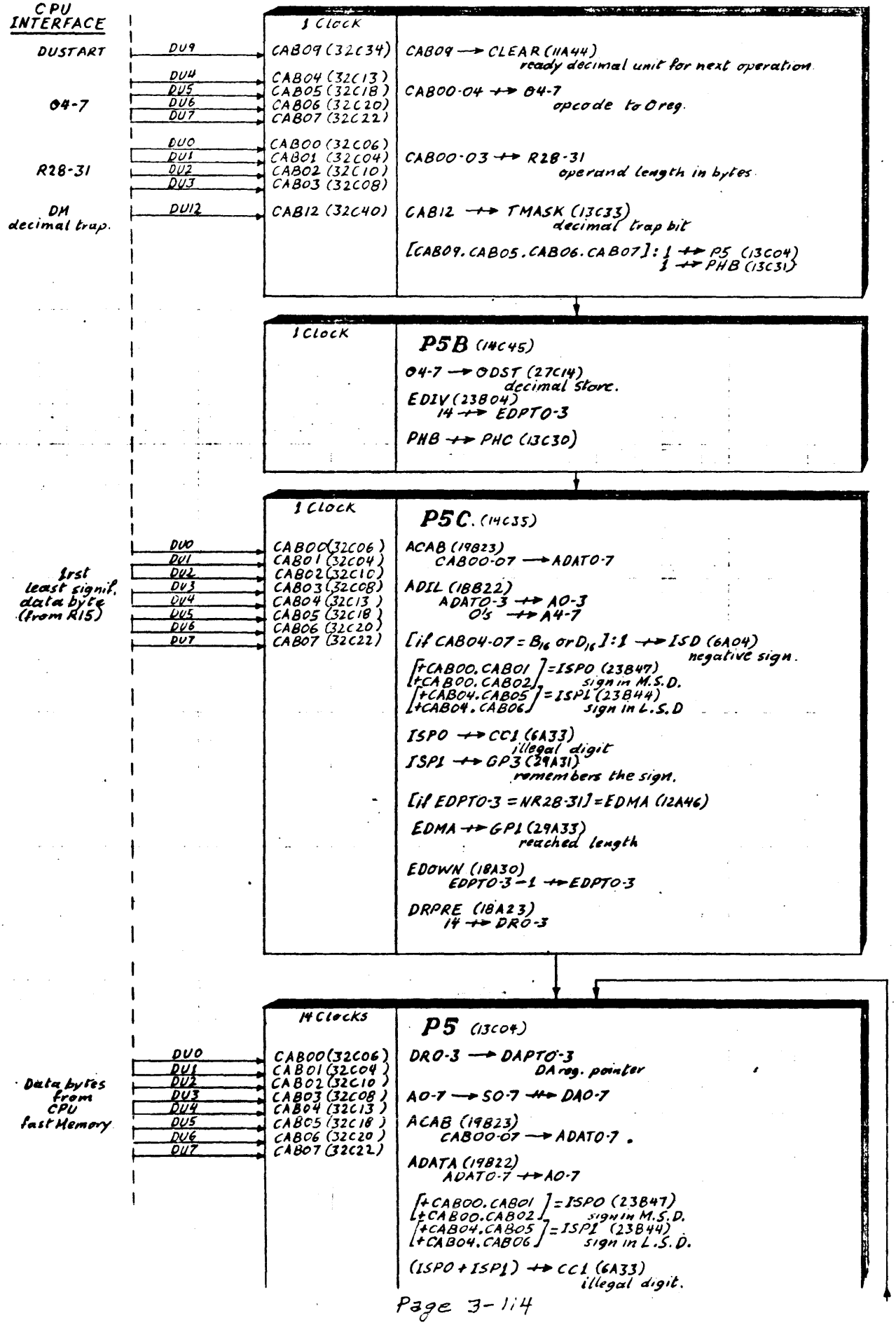
	DU0	S0 (30C30)
	DU1	S1 (30C31)
	DU2	S2 (30C33)
Last data-byte to CPU fast memory	DU3	S3 (30C34)
	DU4	S4 (28C30)
	DU5	S5 (28C31)
	DU6	S6 (28C33)
	DU7	S7 (28C34)
DUEND (sets SW1)	DI0	DUEF (18A22)

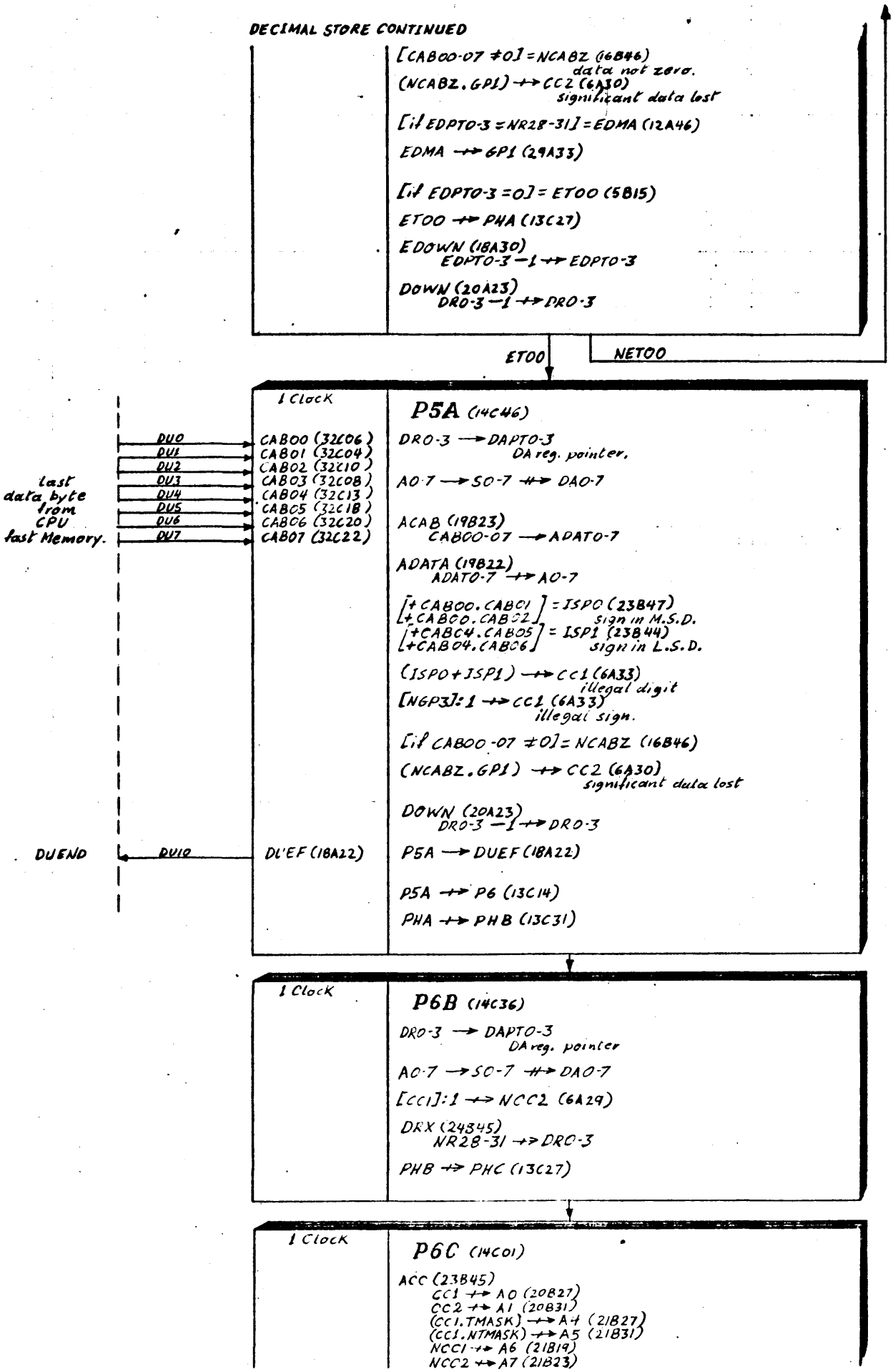
BO-7 → SO-7

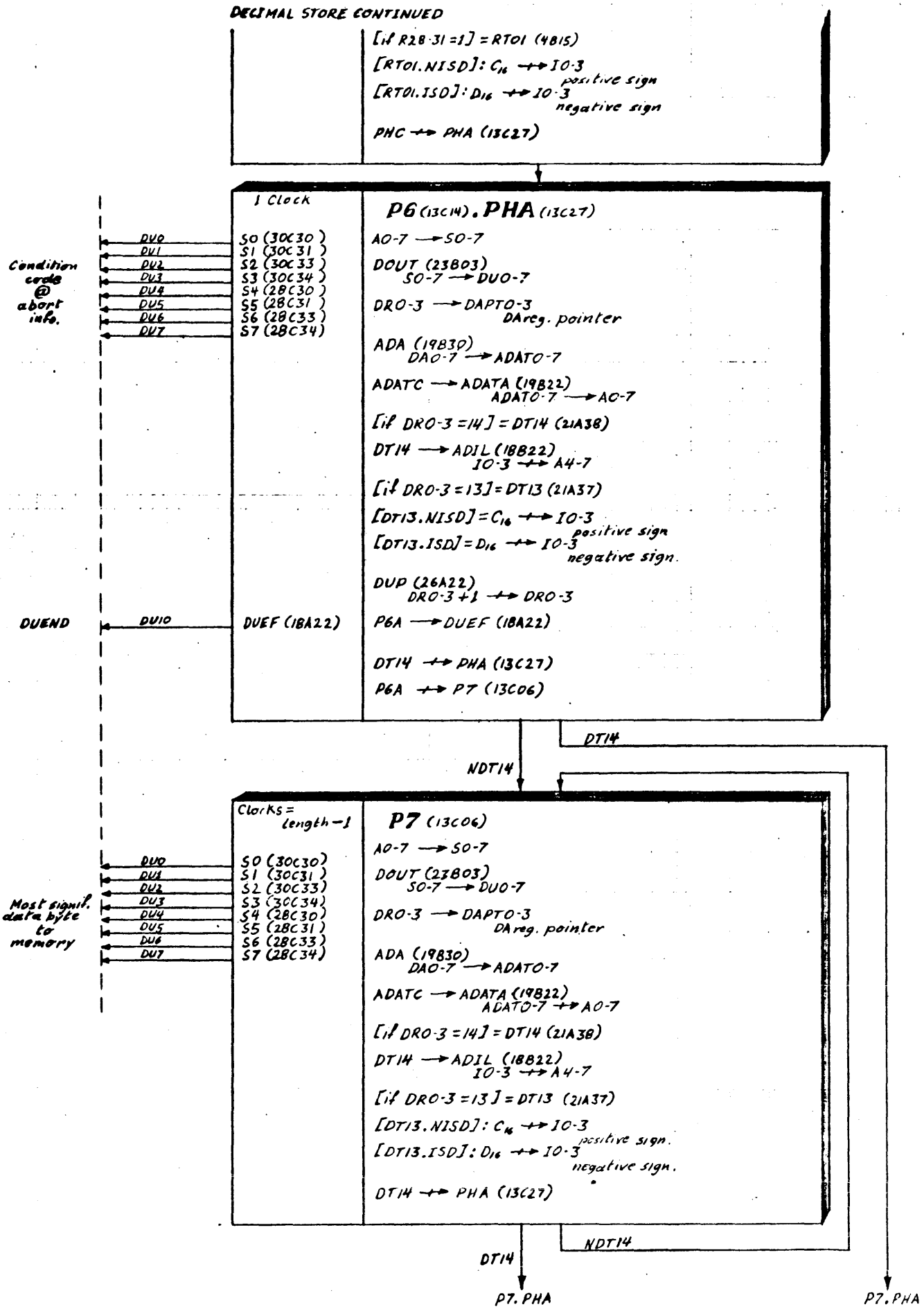
DOUT (23B03)
SO-7 → DU0-7
last byte to CPU

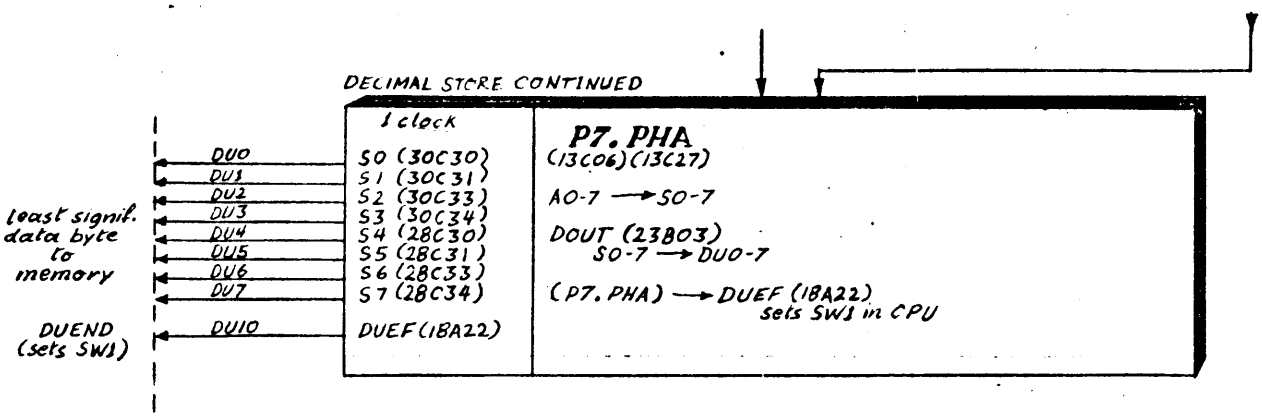
DUEF (18A22)
sets SW1 in CPU

DECIMAL STORE (7F)

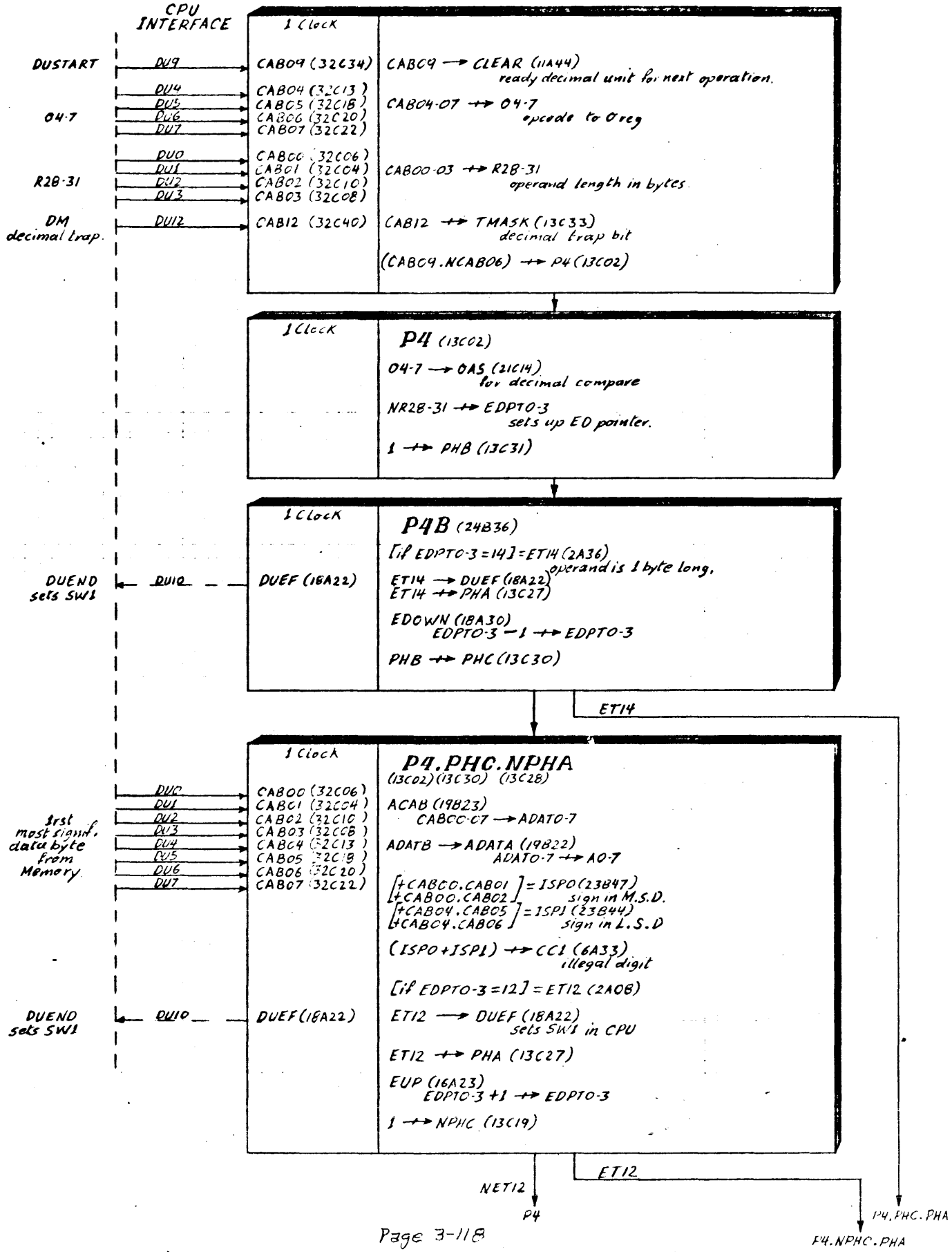


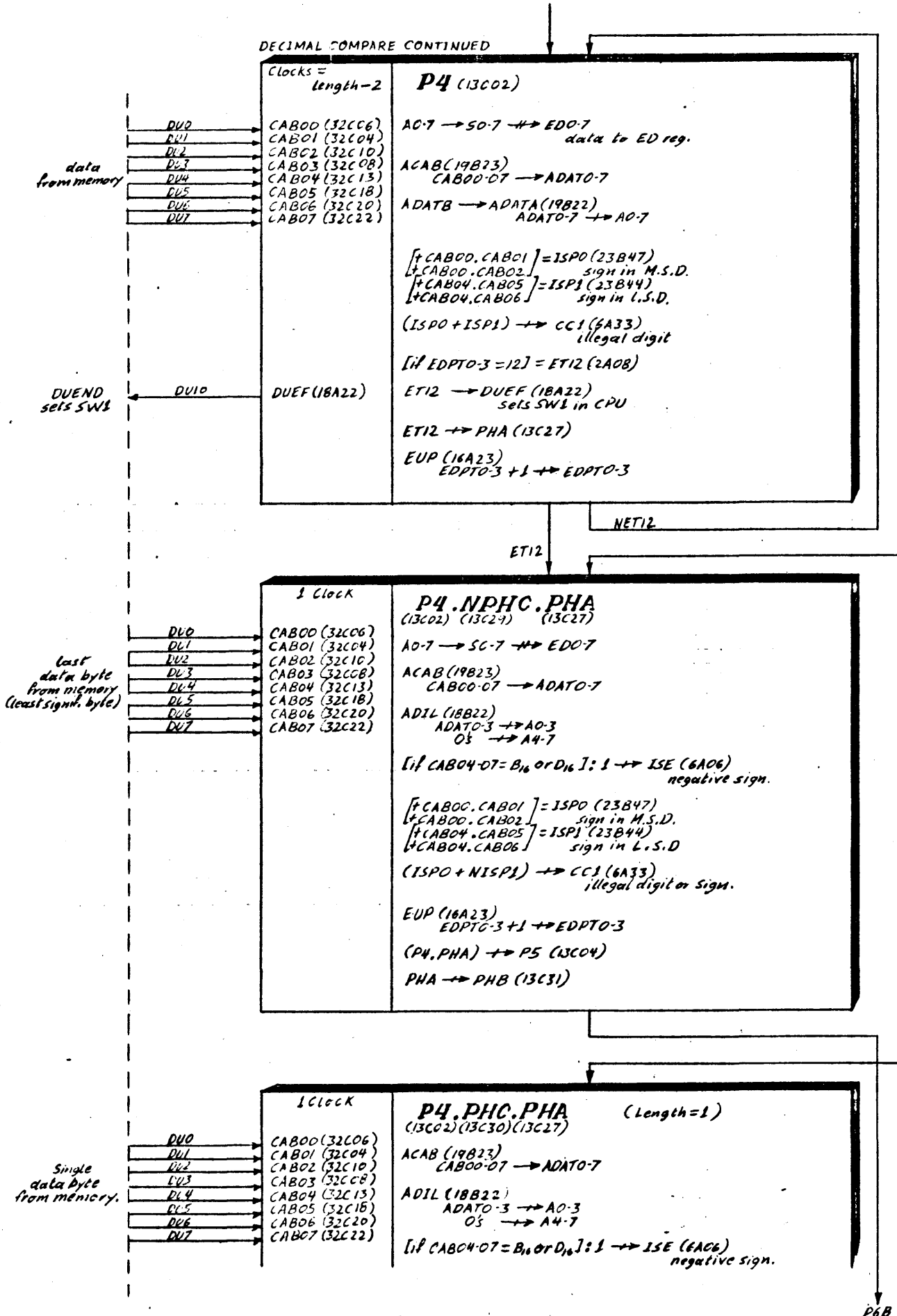

DECIMAL STORE CONTINUED
[CAB00-07 ≠0] = NCABZ (16B46)
data not zero.
(NCABZ.GP1) → CC2 (6A30)
significant data lost
[if EDPT0-3 = NR28-31] = EDMA (12A46)
EDMA → GP1 (29A33)
[if EDPT0-3 = 0] = ET00 (5B15)
ET00 → PHA (13C27)
EDOWN (18A30)
EDPT0-3 − 1 → EDPT0-3
DOWN (20A23)
DR0-3 − 1 → DR0-3
ET00
NET00
1 Clock
P5A (14C46)
DR0-3 → DAPT0-3
DA reg. pointer.
A0-7 → S0-7 → DA0-7
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 → A0-7
[+CAB00.CAB01] = ISP0 (23B47)
[+CAB00.CAB02] sign in M.S.D.
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB06] sign in L.S.D.
(ISP0+ISP1) → CC1 (6A33)
illegal digit
[NGP3]:1 → CC1 (6A33)
illegal sign.
[if CAB00-07 ≠0] = NCABZ (16B46)
(NCABZ.GP1) → CC2 (6A30)
significant data lost
DOWN (20A23)
DR0-3 − 1 → DR0-3
P5A → DUEF (18A22)
P5A → P6 (13C14)
PHA → PHB (13C31)
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
last data byte from CPU fast Memory.
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
DUEND
DU10
DUEF (18A22)
1 Clock
P6B (14C36)
DR0-3 → DAPT0-3
DA reg. pointer
A0-7 → S0-7 → DA0-7
[CC1]:1 → NCC2 (6A29)
DRX (24B45)
NR28-31 → DR0-3
PHB → PHC (13C27)
1 Clock
P6C (14C01)
ACC (23B45)
CC1 → A0 (20B27)
CC2 → A1 (20B31)
(CC1.TMASK) → A4 (21B27)
(CC1.NTMASK) → A5 (21B31)
NCC1 → A6 (21B19)
NCC2 → A7 (21B23)


DECIMAL STORE CONTINUED
[if R28-31=1] = RT01 (4B15)
[RT01.NISD]: C16 → IO-3
[RT01.ISD]: D16 → IO-3
positive sign
negative sign
PHC → PHA (13C27)
1 Clock
P6 (13C14). PHA (13C27)
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
DRO-3 → DAPTO-3
DAreg. pointer
ADA (19B30)
DAO-7 → ADATO-7
ADATC → ADATA (19B22)
ADATO-7 → AO-7
[if DRO-3=14] = DT14 (21A38)
DT14 → ADIL (18B22)
IO-3 → A4-7
[if DRO-3=13] = DT13 (21A37)
[DT13.NISD] = C16 → IO-3
[DT13.ISD] = D16 → IO-3
positive sign
negative sign.
DUP (26A22)
DRO-3+1 → DRO-3
P6A → DUEF (18A22)
DT14 → PHA (13C27)
P6A → P7 (13C06)
Condition code @ abort info.
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
S0 (30C30)
S1 (30C31)
S2 (30C33)
S3 (30C34)
S4 (28C30)
S5 (28C31)
S6 (28C33)
S7 (28C34)
DUEND
DU10
DUEF (18A22)
DT14
NDT14
Clocks = length-1
P7 (13C06)
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
DRO-3 → DAPTO-3
DAreg. pointer
ADA (19B30)
DAO-7 → ADATO-7
ADATC → ADATA (19B22)
ADATO-7 → AO-7
[if DRO-3=14] = DT14 (21A38)
DT14 → ADIL (18B22)
IO-3 → A4-7
[if DRO-3=13] = DT13 (21A37)
[DT13.NISD]: C16 → IO-3
[DT13.ISD]: D16 → IO-3
positive sign.
negative sign.
DT14 → PHA (13C27)
Most signif. data byte to memory
NDT14
DT14
P7.PHA
P7.PHA


DECIMAL STORE CONTINUED
1 clock
P7. PHA
(13C06)(13C27)
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
(P7. PHA) → DUEF (18A22)
sets SW1 in CPU
DUO
DU1
DU2
DU3
DU4
DU5
DU6
DU7
DU10
least signif. data byte to memory
DUEND (sets SW1)
S0 (30C30)
S1 (30C31)
S2 (30C33)
S3 (30C34)
S4 (28C30)
S5 (28C31)
S6 (28C33)
S7 (28C34)
DUEF (18A22)

DECIMAL COMPARE (7D)




DECIMAL COMPARE CONTINUED
Clocks = length-2
P4 (13C02)
DU0 CAB00 (32CC6)
DU1 CAB01 (32C04)
DU2 CAB02 (32C10)
DU3 CAB03 (32C08)
DU4 CAB04 (32C13)
DU5 CAB05 (32C18)
DU6 CAB06 (32C20)
DU7 CAB07 (32C22)
data from memory
A0-7 → S0-7 → EDO-7
data to ED reg.
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATB → ADATA (19B22)
ADAT0-7 → A0-7
[+CAB00.CAB01] = ISP0 (23B47)
[+CAB00.CAB02] sign in M.S.D.
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB06] sign in L.S.D.
(ISP0 + ISP1) → CC1 (6A33)
illegal digit
[if EDPT0-3 = 12] = ET12 (2A08)
DUEND sets SW1
DU10
DUEF (18A22)
ET12 → DUEF (18A22)
sets SW1 in CPU
ET12 → PHA (13C27)
EUP (16A23)
EDPT0-3 + 1 → EDPT0-3
NET12
ET12
1 Clock
P4.NPHC.PHA
(13C02) (13C29) (13C27)
DU0 CAB00 (32CC6)
DU1 CAB01 (32C04)
DU2 CAB02 (32C10)
DU3 CAB03 (32CC8)
DU4 CAB04 (32C13)
DU5 CAB05 (32C18)
DU6 CAB06 (32C20)
DU7 CAB07 (32C22)
last data byte from memory (least signif. byte)
A0-7 → SC-7 → EDO-7
ACAB (19B23)
CAB00-07 → ADAT0-7
ADIL (18B22)
ADAT0-3 → A0-3
05 → A4-7
[if CAB04-07 = B16 or D16]: 1 → ISE (6A06)
negative sign.
[+CAB00.CAB01] = ISP0 (23B47)
[+CAB00.CAB02] sign in M.S.D.
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB06] sign in L.S.D
(ISP0 + NISP1) → CC1 (6A33)
illegal digit or sign.
EUP (16A23)
EDPT0-3 + 1 → EDPT0-3
(P4.PHA) → P5 (13C04)
PHA → PHB (13C31)
1 Clock
P4.PHC.PHA (Length = 1)
(13C02) (13C30) (13C27)
DU0 CAB00 (32CC6)
DU1 CAB01 (32C04)
DU2 CAB02 (32C10)
DU3 CAB03 (32CC8)
DU4 CAB04 (32C13)
DU5 CAB05 (32C18)
DU6 CAB06 (32C20)
DU7 CAB07 (32C22)
Single data byte from memory.
ACAB (19B23)
CAB00-07 → ADAT0-7
ADIL (18B22)
ADAT0-3 → A0-3
05 → A4-7
[if CAB04-07 = B16 or D16]: 1 → ISE (6A06)
negative sign.
P6B

DECIMAL COMPARE CONTINUED

[+CABCC.CAB01] = ISP0 (23B47) sing in M.S.D.
[+CAB00.CAB02]
[+CAB04.CAB05] = ISP1 (23B44) sign in L.S.D.
[+CAB04.CAB06]

(ISP0 + NISP1) → CC1 (6A33) illegal digit or sign.

EUP (16A23)
EDPT0-3 + 1 → EDPT0-3

(P4.PHA) → P5 (13C04)

PHA → PHB (13C31)

1 Clock

P5B (14C45)

A0-7 → S0-7 → ED0-7 last data byte to ED reg. (Loc. M)

EDIV (23B04)
14 → EDPT0-3

PHB → PHC (13C30)

1 Clock

P5C (14C35)

1rst least signif. data byte from R15

DU0	CAB00 (32C06)
DU1	CAB01 (32C04)
DU2	CAB02 (32C10)
DU3	CAB03 (32C08)
DU4	CAB04 (32C13)
DU5	CAB05 (32C18)
DU6	CAB06 (32C20)
DU7	CAB07 (32C22)

ACAB (19B23)
CAB00-07 → ADAT0-7

ADIL (18B22)
ADAT0-3 → A0-3
0's → A4-7

[if CAB04-07 = B_{16} or D_{16}] : 1 → ISD (6A04) negative sign.

[+CAB00.CAB01] = ISP0 (23B47) sign in M.S.D.
[+CAB00.CAB02]
[+CAB04.CAB05] = ISP1 (23B44) sign in L.S.D.
[+CAB04.CAB06]

ISP0 → CC1 (6A33) illegal digit
ISP1 → GP3 (29A31) remembers the sign.

ED0-7 → ESH0-7

ESL (9A30)
ESH0-7 → B0-7

[if EDPT0-3 = NR2B-31] = EDMA (12AM6)

EDMA → GP1 (29A33) end of operand

EDOWN (18A30)
EDPT0-3 − 1 → EDPT0-3

DRPRE (18A23)
14 → DR0-3 to address DA reg.

14 Clocks

P5 (13C04)

[if ISE ≠ ISD] = NSUB (17C23)
A0-7 + B0-7 → S0-7

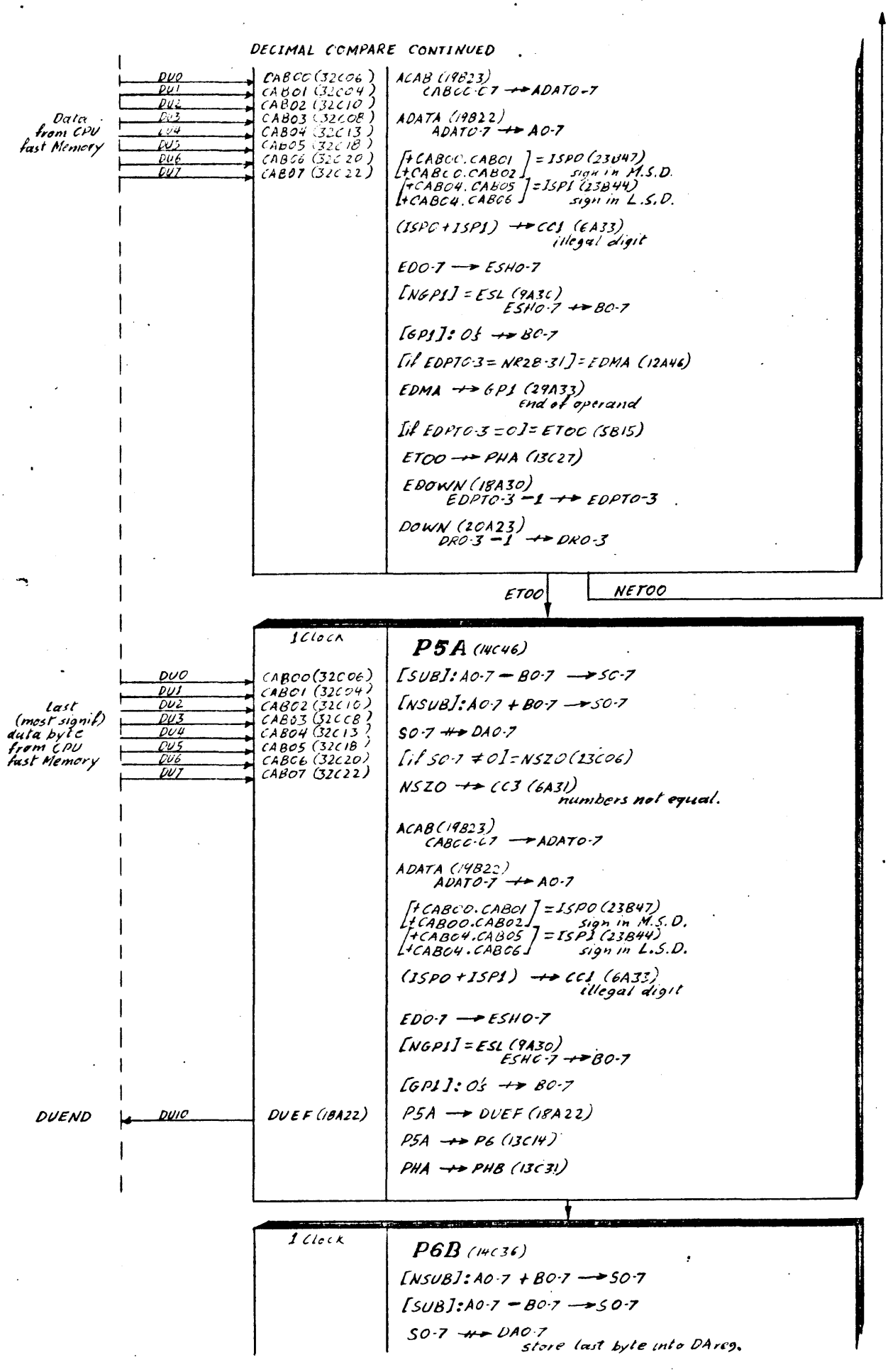
[if ISE = ISD] = SUB (23C45)
A0-7 − B0-7 → S0-7

SUB → GP5 (6A02) remembers subtract

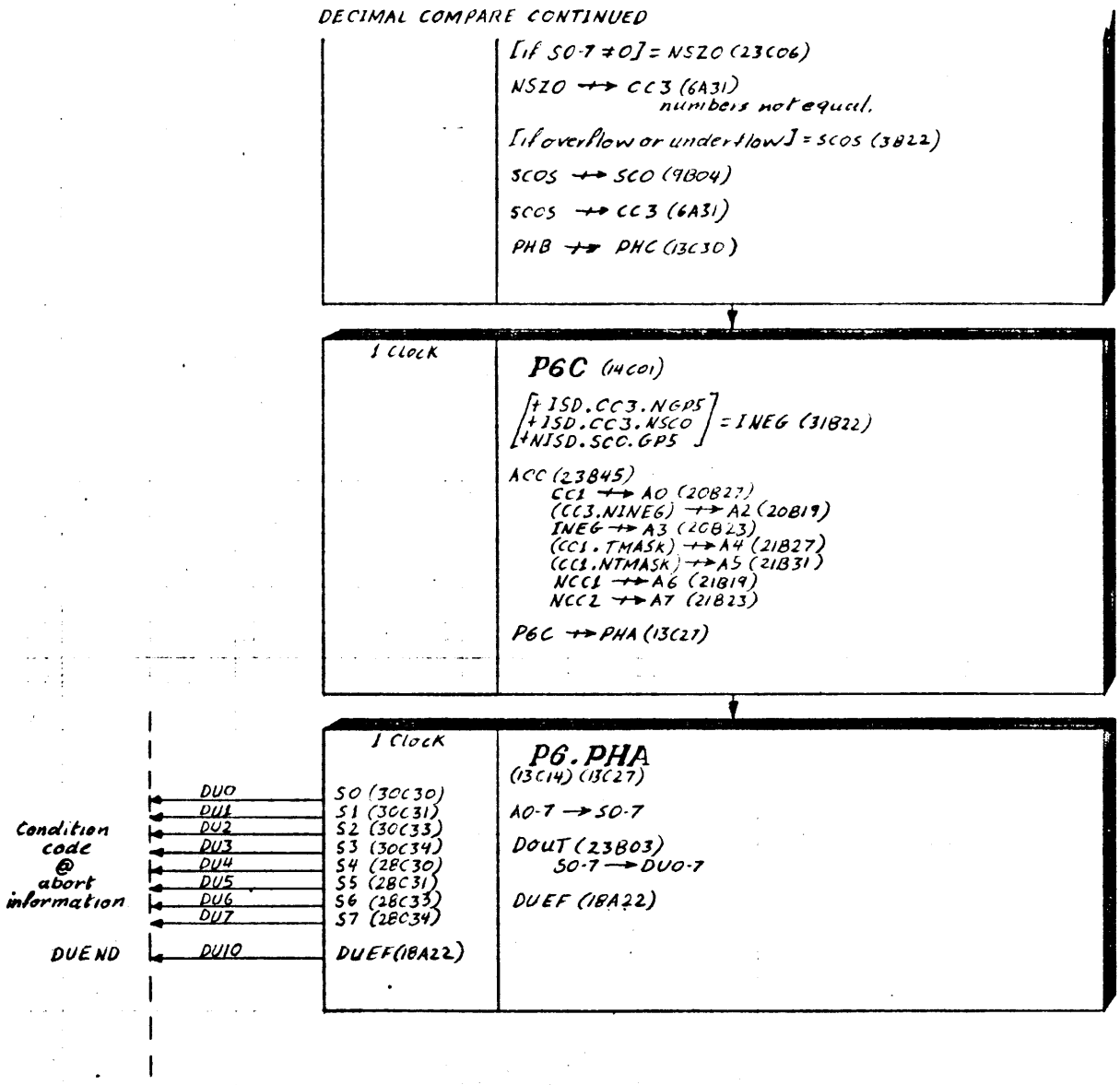
S0-7 → DA0-7 result to DA reg.

[if S ≠ 0] = NSZ0 (23C06)

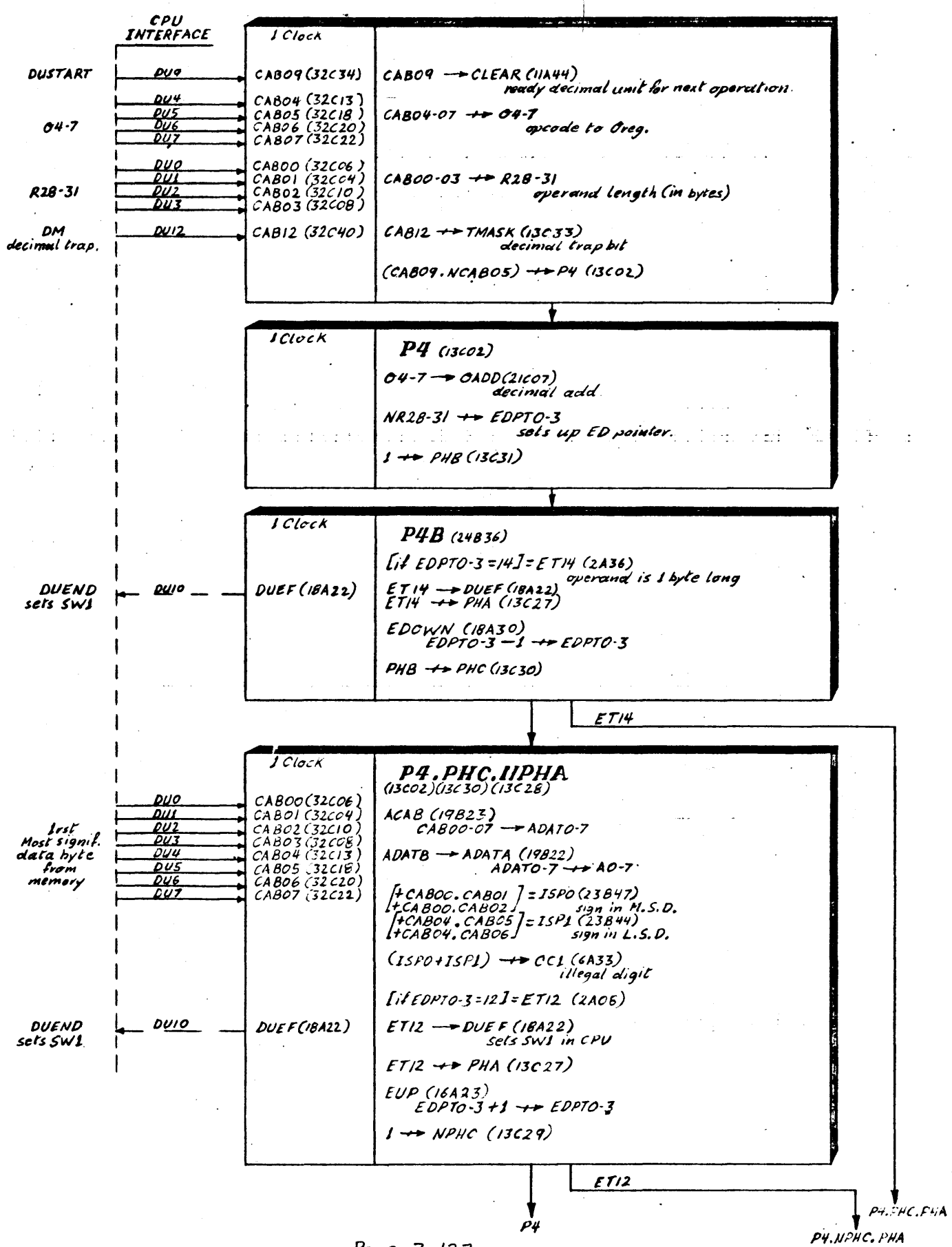
NSZ0 → CC3 (6A31) numbers not equal.


DECIMAL COMPARE CONTINUED
Data from CPU fast Memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
ACAB (19B23)
CABCC·C7 → ADAT0-7
ADATA (19B22)
ADAT0·7 → A0-7
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47) sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44) sign in L.S.D.
(ISP0 + ISP1) → CC1 (6A33) illegal digit
ED0·7 → ESH0-7
[NGP1] = ESL (9A30) ESH0·7 → B0-7
[GP1]: 0's → B0-7
[if EDPT0-3 = NR2B-31] = EDMA (12A46)
EDMA → GP1 (29A33) end of operand
[if EDPT0-3 = 0] = ETOO (5B15)
ETOO → PHA (13C27)
EDOWN (18A30) EDPT0·3 − 1 → EDPT0-3
DOWN (20A23) DR0·3 − 1 → DR0-3
ETOO
NETOO
1 Clock
P5A (14C46)
[SUB]: A0-7 − B0-7 → SC-7
[NSUB]: A0-7 + B0-7 → S0-7
S0-7 → DA0-7
[if S0-7 ≠ 0] = NSZ0 (23C06)
NSZ0 → CC3 (6A31) numbers not equal.
ACAB (19B23) CABCC·C7 → ADAT0-7
ADATA (19B22) ADAT0-7 → A0-7
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47) sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44) sign in L.S.D.
(ISP0 + ISP1) → CC1 (6A33) illegal digit
ED0·7 → ESH0-7
[NGP1] = ESL (9A30) ESH0·7 → B0-7
[GP1]: 0's → B0-7
P5A → DUEF (18A22)
P5A → P6 (13C14)
PHA → PHB (13C31)
last (most signif) data byte from CPU fast Memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
DUEND
DU10
DUEF (18A22)
1 Clock
P6B (14C36)
[NSUB]: A0-7 + B0-7 → S0-7
[SUB]: A0-7 − B0-7 → S0-7
S0-7 → DA0-7 store last byte into DA reg.

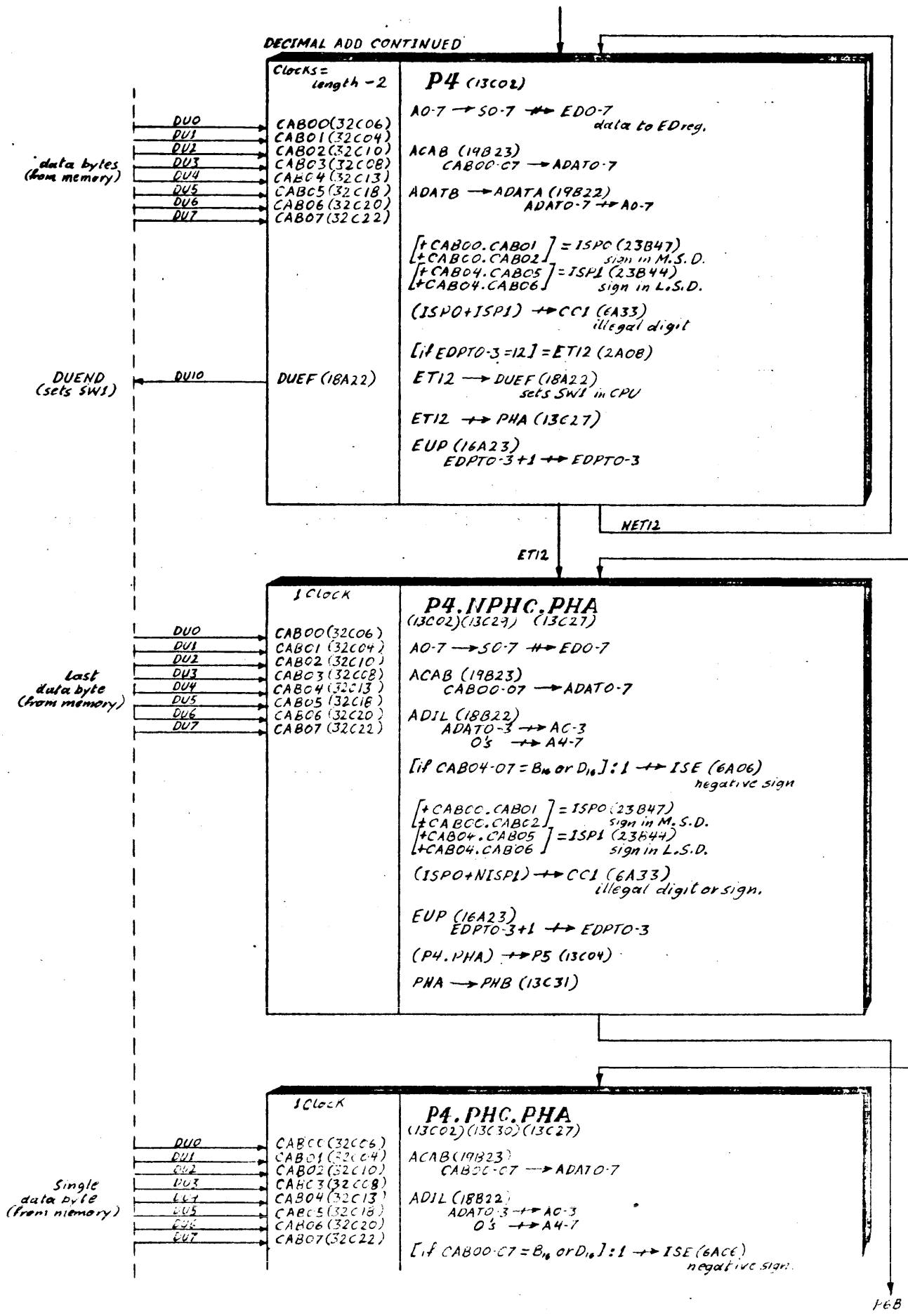
DECIMAL COMPARE CONTINUED



DECIMAL ADD (79)



DECIMAL ADD CONTINUED



DECIMAL ADD CONTINUED

[+CAB00.CAB01] = ISP0 (23B47)
[+CAB00.CAB02] sign in M.S.D.
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB06] sign in L.S.D.

(ISP0 + NISP1) →→ CC1 (6A33)
illegal sign or digit

EUP (16A23)
EDPTO-3 + 1 →→ EDPTO-3

(P4.PHA) →→ P5 (13C04)

PHA →→ PHB (13C31)

1 Clock

P5B (14C45)

A0-7 → S0-7 →→ ED0-7
last data byte to ED reg. (loc. 14)

EDIV (23B04)
14 →→ EDPTO-3
to address ED reg.

PHB →→ PHC (13C30)

1 Clock

P5C (14C35)

DV0 CAB00 (32C06)
DV1 CAB01 (32C04)
DV2 CAB02 (32C10)
DV3 CAB03 (32C0E)
DV4 CAB04 (32C13)
DV5 CAB05 (32C18)
DV6 CAB06 (32C20)
DV7 CAB07 (32C22)

1rst least signif data byte from R15

ACAB (19B23)
CAB00-07 → ADAT0-7

ADIL (18B22)
ADAT0-3 →→ A0-3
0s →→ A4-7

[if CAB04-07 = B_{16} or D_{16}]: 1 →→ ISD (6A04)
negative sign

[+CAB00.CAB01] = ISP0 (23B47)
[+CAB00.CAB02] sign in M.S.D
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB05] sign in L.S.D

ISP0 →→ CC1 (6A33)
illegal digit
ISP1 →→ GP3 (29A31)
remembers the sign.

ED0-7 → ESH0-7

ESL (9A30)
ESH0-7 →→ B0-7

[if EDPTO-3 = NR28-31] = EDMA (12A46)

EDMA →→ GP1 (29A33)
end of operand.

EDOWN (18A30)
EDPTO-3 − 1 → EDPTO-3

DRPRE (18A23)
14 →→ DR0-3
to address DA reg.

14 Clocks

P5 (13C04)

[if ISE = ISD] = NSUB (17C23)
A0-7 + B0-7 → S0-7

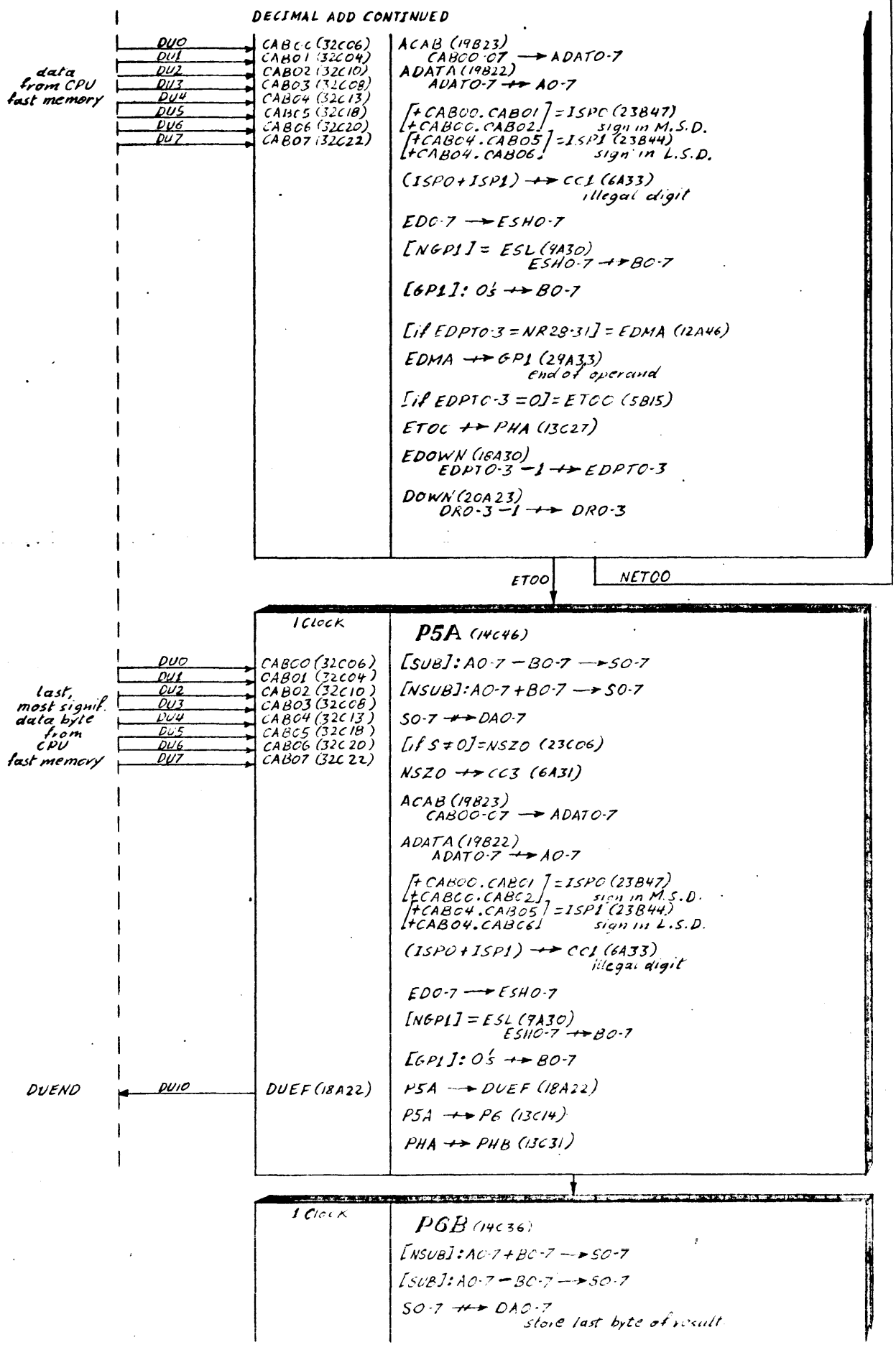
[if ISE ≠ ISD] = SUB (23C45)
A0-7 − B0-7 → S0-7

SUB →→ GP5 (6A02)
remembers subtract.

S0-7 →→ DA0-7
result to DA reg.

[if S ≠ 0] = NSZ0 (23C06)

NSZ0 →→ CC3 (6A31)
result not zero.


DECIMAL ADD CONTINUED
data from CPU fast memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 ↠ A0-7
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47) sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44) sign in L.S.D.
(ISP0+ISP1) ↠ CC1 (6A33) illegal digit
ED0-7 → ESH0-7
[NGP1] = ESL (9A30) ESH0-7 ↠ B0-7
[GP1]: 0's ↠ B0-7
[if EDPT0-3 = NR28-31] = EDMA (12A46)
EDMA ↠ GP1 (29A33) end of operand
[if EDPT0-3 = 0] = ETOO (5B15)
ETOO ↠ PHA (13C27)
EDOWN (18A30)
EDPT0-3 −1 ↠ EDPT0-3
DOWN (20A23)
DR0-3 −1 ↠ DR0-3
ETOO
NETOO
1 Clock
P5A (14C46)
last, most signif. data byte from CPU fast memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
[SUB]: A0-7 − B0-7 → S0-7
[NSUB]: A0-7 + B0-7 → S0-7
S0-7 ↠ DA0-7
[if S ≠ 0] = NSZ0 (23C06)
NSZ0 ↠ CC3 (6A31)
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 ↠ A0-7
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47) sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44) sign in L.S.D.
(ISP0+ISP1) ↠ CC1 (6A33) illegal digit
ED0-7 → ESH0-7
[NGP1] = ESL (9A30) ESH0-7 ↠ B0-7
[GP1]: 0's ↠ B0-7
DUEND
DU10
DUEF (18A22)
P5A → DUEF (18A22)
P5A ↠ P6 (13C14)
PHA ↠ PHB (13C31)
1 Clock
P6B (14C36)
[NSUB]: A0-7 + B0-7 → S0-7
[SUB]: A0-7 − B0-7 → S0-7
S0-7 ↠ DA0-7 store last byte of result

DECIMAL ADD CONTINUED

[if S0-7 ≠ 0] = NSZO (23C06)

NSZO → CC3 (6A31)
result not zero

[if overflow or underflow] = SCOS (3B22)

SCOS → SCO (9B04)
remembers overflow or underflow

SCOS → GP2 (29A30)
for complementing result if SUB

(NSUB.SCOS) → CC2 (6A30)
overflow.

PHB → PHC (13C30)

1 Clock

P6C (14C01)

ACC (23B45)
CC1 → A0 (20B27)
CC2 → A1 (20B31)
(CC3.NINEG) → A2 (20B19)
INEG → A3 (20B23)
(CC1.TMASK) → A4 (21B27)
(CC1.NTMASK) → A5 (21B31)
NCC1 → A6 (21B19)
NCC2 → A7 (21B23)

[+ISE.ISD.CC3 / +NSCO.ISD.CC3 / +GP5.SCO.NISD] = INEG (31B22)

[NINEG]: C_{16} → IO-3

[INEG]: D_{16} → IO-3

DRPRE (18A23)
14 → DRO-3

EDIV (23B04)
14 → EDPTO-3

P6C → PHA (13C27)

1 Clock

P6.PHA
(13C14) (13C27)

A0-7 → S0-7

DOUT (23B03)
S0-7 → DUO-7

DUEF (18A22)
sets SW1 in CPU

ADIL (18B22)
IO-3 → A4-7
sign.

EDA (5B02)
DA0-7 → B0-7

DOWN (20A23)
DRO-3 − 1 → DRO-3

EDOWN (18A30)
EDPTO-3 − 1 → EDPTO-3

P6A → P7 (13C06)

Condition code & abort info.

DU0	S0 (30C30)
DU1	S1 (30C31)
DU2	S2 (30C33)
DU3	S3 (30C34)
DU4	S4 (28C30)
DU5	S5 (28C31)
DU6	S6 (28C33)
DU7	S7 (29C34)

14 Clocks

P7 (13C06)

[GP2] = SUB (2B36)
A0-7 − B0-7 → S0-7

[NGP2] = NSUB (17C23)
A0-7 + B0-7 → S0-7

DOUT (23B03)
S0-7 → DUO-7

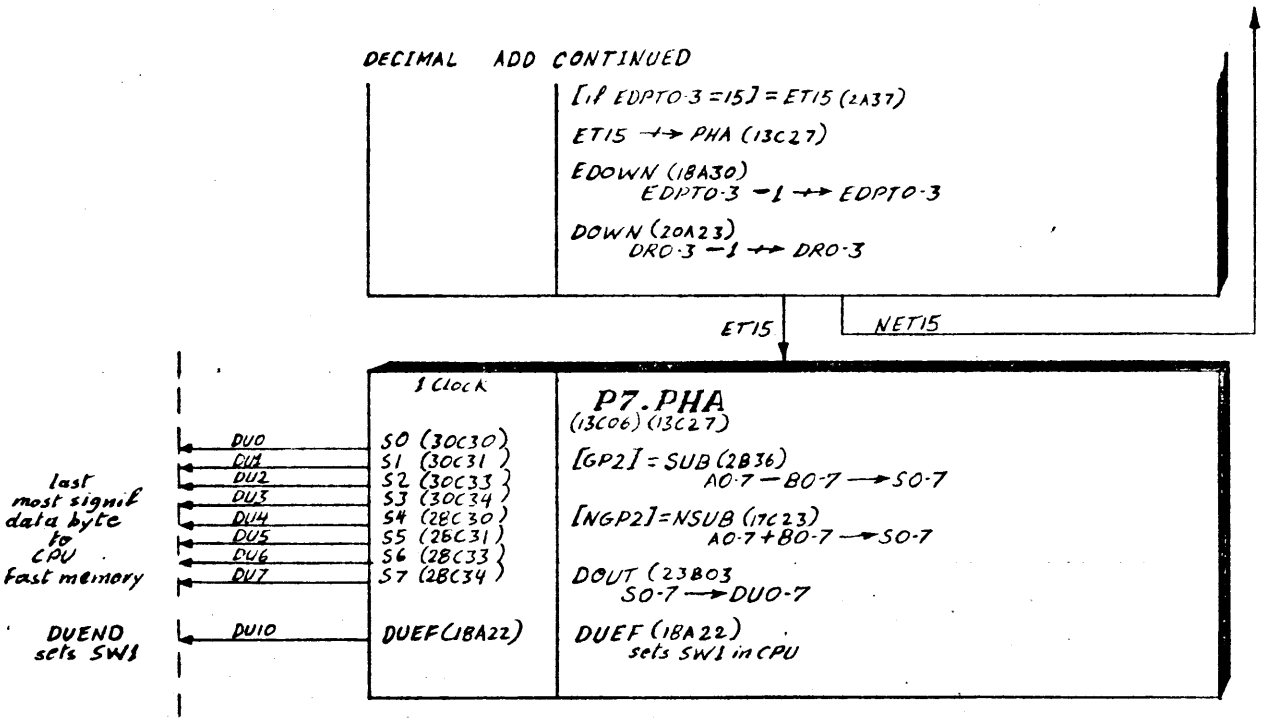
EDA (5B02)
DA0-3 → B0-7

0's → A0-7

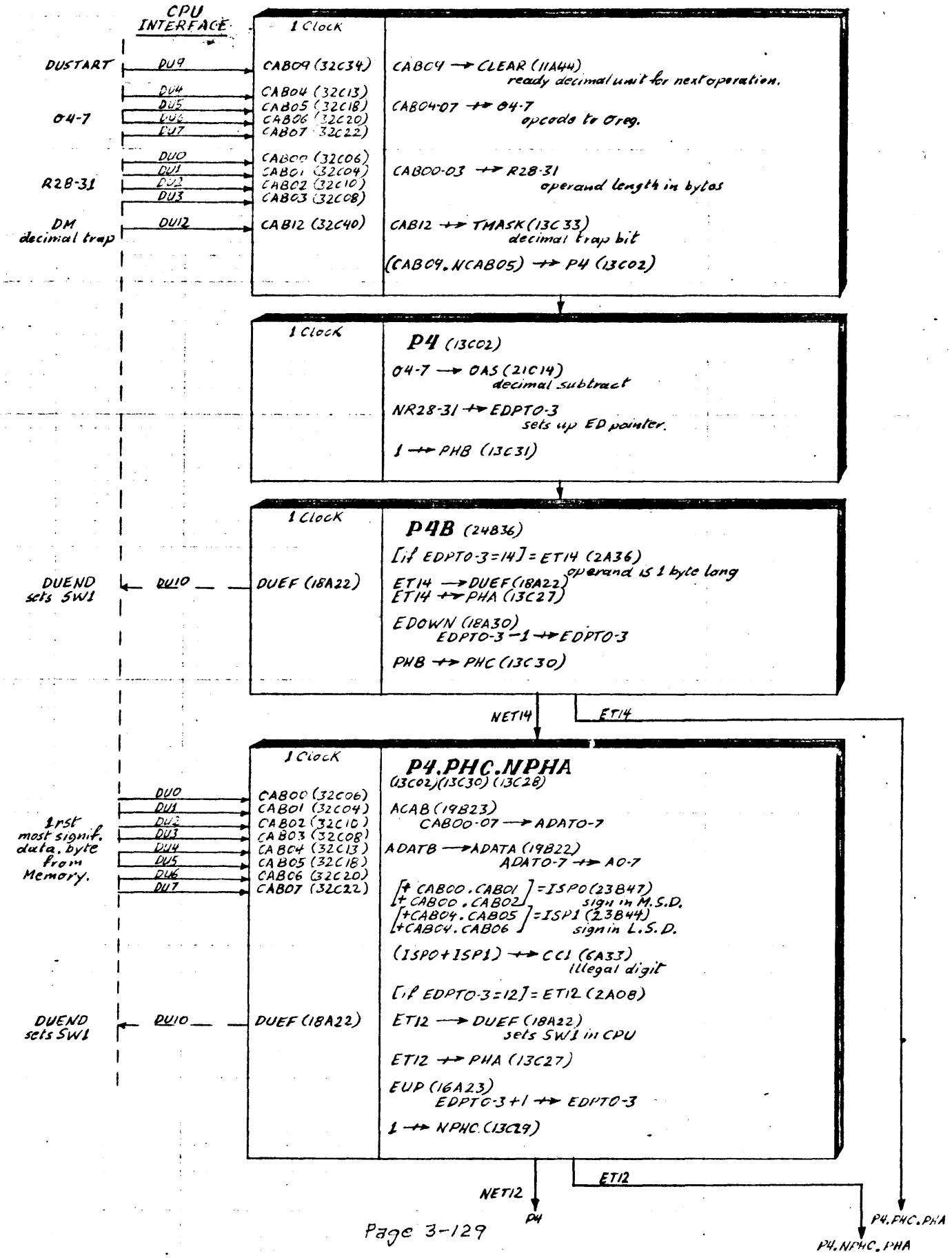
Result back to CPU starting with least signif. byte.

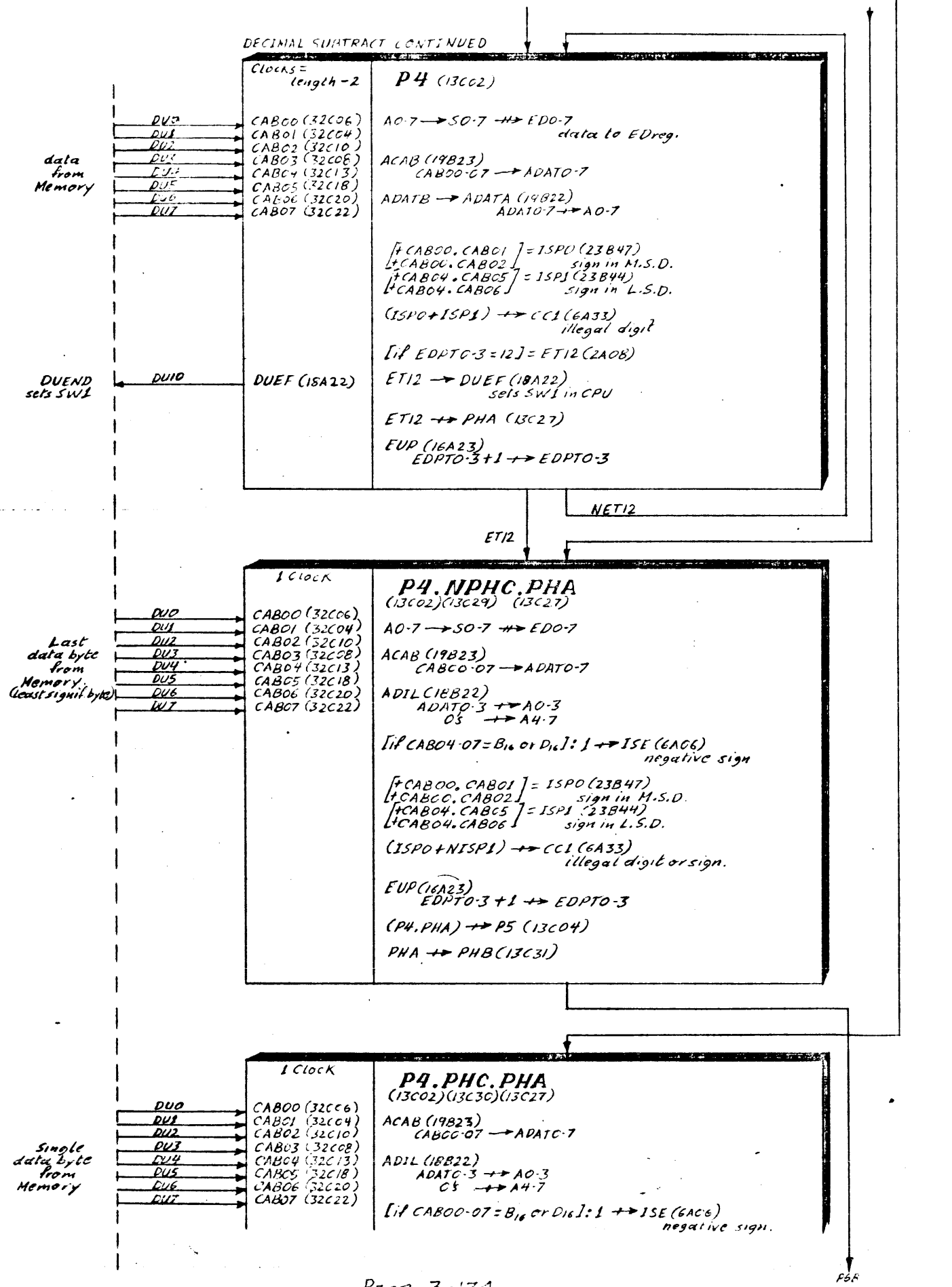
DU0	S0 (30C30)
DU1	S1 (30C31)
DU2	S2 (30C33)
DU3	S3 (30C34)
DU4	S4 (28C30)
DU5	S5 (28C31)
DU6	S6 (28C33)
DU7	S7 (29C34)

DECIMAL ADD CONTINUED



DECIMAL SUBTRACT (78)




DECIMAL SUBTRACT CONTINUED
Clocks = length - 2
P4 (13C02)
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
data from Memory
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
A0-7 → S0-7 → EDO-7
data to EDreg.
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATB → ADATA (19B22)
ADAT0-7 → A0-7
[↑CAB00. CAB01] = ISP0 (23B47)
[↑CAB00. CAB02] sign in M.S.D.
[↑CAB04. CAB05] = ISP1 (23B44)
[↑CAB04. CAB06] sign in L.S.D.
(ISP0+ISP1) → CC1 (6A33)
illegal digit
[if EDPT0-3 = 12] = ET12 (2A08)
DUEND sets SW1
DU10
DUEF (18A22)
ET12 → DUEF (18A22)
sets SW1 in CPU
ET12 → PHA (13C27)
EUP (16A23)
EDPT0-3 + 1 → EDPT0-3
NET12
ET12
1 Clock
P4.NPHC.PHA
(13C02)(13C29) (13C27)
Last data byte from Memory (least signif byte)
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
A0-7 → S0-7 → EDO-7
ACAB (19B23)
CAB00-07 → ADAT0-7
ADIL (18B22)
ADAT0-3 → A0-3
0s → A4-7
[if CAB04-07 = B16 or D16]: 1 → ISE (6A06)
negative sign
[↑CAB00. CAB01] = ISP0 (23B47)
[↑CAB00. CAB02] sign in M.S.D.
[↑CAB04. CAB05] = ISP1 (23B44)
[↑CAB04. CAB06] sign in L.S.D.
(ISP0+NISP1) → CC1 (6A33)
illegal digit or sign.
EUP (16A23)
EDPT0-3 + 1 → EDPT0-3
(P4.PHA) → P5 (13C04)
PHA → PHB (13C31)
1 Clock
P4.PHC.PHA
(13C02)(13C30)(13C27)
Single data byte from Memory
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
ACAB (19B23)
CAB00-07 → ADAT0-7
ADIL (18B22)
ADAT0-3 → A0-3
0s → A4-7
[if CAB00-07 = B16 or D16]: 1 → ISE (6AC6)
negative sign.
P6A

DECIMAL SUBTRACT CONTINUED

[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47) sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44) sign in L.S.D.

(ISP0+NISP1) →→ CC1 (6A33) illegal digit or sign.

EUP (16A23)
EDPTO-3 +1 →→ EDPTO-3

(P4, PHA) →→ P5 (13C04)

PHA →→ PHB (13C31)

1 Clock

P5B (14C45)

A0-7 → S0-7 →→ ED0-7 last data byte to ED reg. (Loc. 14)

EDIV (23B04)
14 →→ EDPTO-3

PHB →→ PHC (13C30)

1 Clock

P5C (14C35)

1rst least signif. data byte from R15

DU0	CAB00 (32C06)
DU1	CAB01 (32C04)
DU2	CAB02 (32C10)
DU3	CAB03 (32C08)
DU4	CAB04 (32C13)
DU5	CAB05 (32C18)
DU6	CAB06 (32C20)
DU7	CAB07 (32C22)

ACAB (19B23)
CAB00-07 → ADAT0-7

ADIL (18B22)
ADAT0-3 →→ A0-3
0's →→ A4-7

[if CAB04-07 = B_{16} or D_{16}]: 1 →→ ISD (6A04) negative sign.

[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47) sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44) sign in L.S.D.

ISP0 →→ CC1 (6A33) illegal digit
ISP1 →→ GP3 (29A31) remembers the sign.

ED0-7 → ESH0-7

ESL (9A30)
ESH0-7 →→ B0-7

[if EDPTO-3 = NR28-31] = EDMA (12A46)

EDMA →→ GP1 (29A33) end of operand

EDOWN (18A30)
EDPTO-3 −1 →→ EDPTO-3

DRPRE (18A23)
14 →→ DR0-3 to address DA reg

14 Clocks

P5 (13C04)

[if ISE ≠ ISD] = NSUB (17C23) A0-7 + B0-7 → S0-7

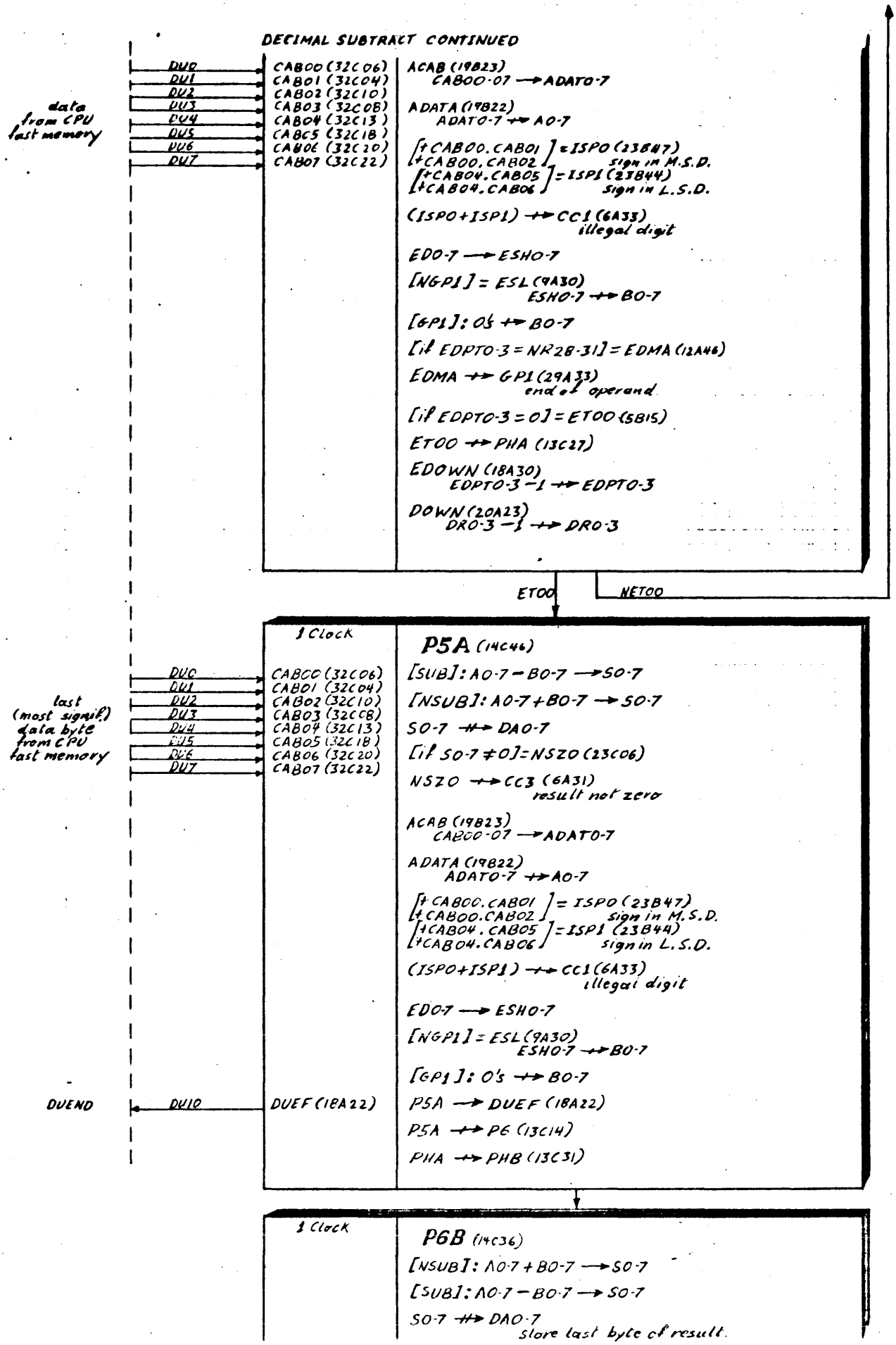
[if ISE = ISD] = SUB (23C45) A0-7 − B0-7 → S0-7

SUB →→ GP5 (6A02) remembers subtract.

S0-7 →→ DA0-7 result to DA reg.

[if S ≠ 0] = NSZ0 (23C06)

NSZ0 →→ CC3 (6A31) result not zero.


DECIMAL SUBTRACT CONTINUED
data from CPU last memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 ↔ A0-7
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47) sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44) sign in L.S.D.
(ISP0+ISP1) ↔ CC1 (6A33) illegal digit
ED0-7 → ESH0-7
[NGP1] = ESL (9A30) ESH0-7 ↔ B0-7
[GP1]: 0's ↔ B0-7
[if EDPT0-3 = NR28-31] = EDMA (12A46)
EDMA ↔ GP1 (29A33) end of operand
[if EDPT0-3 = 0] = ET00 (5B15)
ET00 ↔ PHA (13C27)
EDOWN (18A30) EDPT0-3 −1 ↔ EDPT0-3
DOWN (20A23) DR0-3 −1 ↔ DR0-3
ET00
NET00
1 Clock
P5A (14C46)
last (most signif.) data byte from CPU last memory
[SUB]: A0-7 − B0-7 → S0-7
[NSUB]: A0-7 + B0-7 → S0-7
S0-7 ↔ DA0-7
[if S0-7 ≠ 0] = NSZ0 (23C06)
NSZ0 ↔ CC3 (6A31) result not zero
ACAB (19B23) CAB00-07 → ADAT0-7
ADATA (19B22) ADAT0-7 ↔ A0-7
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47) sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44) sign in L.S.D.
(ISP0+ISP1) ↔ CC1 (6A33) illegal digit
ED0-7 → ESH0-7
[NGP1] = ESL (9A30) ESH0-7 ↔ B0-7
[GP1]: 0's ↔ B0-7
DUEND
DU10
DUEF (18A22)
P5A → DUEF (18A22)
P5A ↔ P6 (13C14)
PHA ↔ PHB (13C31)
1 Clock
P6B (14C36)
[NSUB]: A0-7 + B0-7 → S0-7
[SUB]: A0-7 − B0-7 → S0-7
S0-7 ↔ DA0-7 store last byte of result.

DEDIMAL SUBTRACT CONTINUED

[if SO-7 ≠ 0] = NSZO (23C06)

NSZO →→ CC3 (6A31)
result not zero

[if overflow or underflow] = SCOS (3B22)

SCOS →→ SCO (9B04)
remembers overflow or underflow

SCOS →→ GP2 (29A30)
for complementing result if SUB

(NSUB . SCOS) →→ CC2 (6A39)
overflow

PHB →→ PHC (13C30)

1 Clock

P6C (14C01)

$$\begin{bmatrix} +ISD.CC3.NGP5 \\ +ISD.CC3.NSCO \\ +NISD.SCO.GP5 \end{bmatrix} = INEG\ (31B22)$$

ACC (23B45)
- CC1 →→ A0 (20B27)
- CC2 →→ A1 (20B31)
- (CC3.NINEG) →→ A2 (20B19)
- INEG →→ A3 (20B23)
- (CC1.TMASK) →→ A4 (21B27)
- (CC1.NTMASK) →→ A5 (21B31)
- NCC1 →→ A6 (21B19)
- NCC2 →→ A7 (21B23)

[NINEG]: C_{16} →→ IO-3

[INEG]: D_{16} →→ IO-3

DRPRE (18A23)
14 →→ DRO-3

EDIV (23B04)
14 →→ EDPTO-3

P6C →→ PHA (13C27)

1 Clock

P6 (13C14) . **PHA** (13C27)

AO-7 → SO-7

DOUT (23B03)
SO-7 → DUO-7

DUEF (18A22)
sets SW1 in CPU

ADIL (18B22)
IO-3 →→ A4-7
0's → A0-3
sign to Areg.

EDA (5B02)
DAO-7 →→ BO-7

DOWN (20A23)
DRO-3 − 1 →→ DRO-3

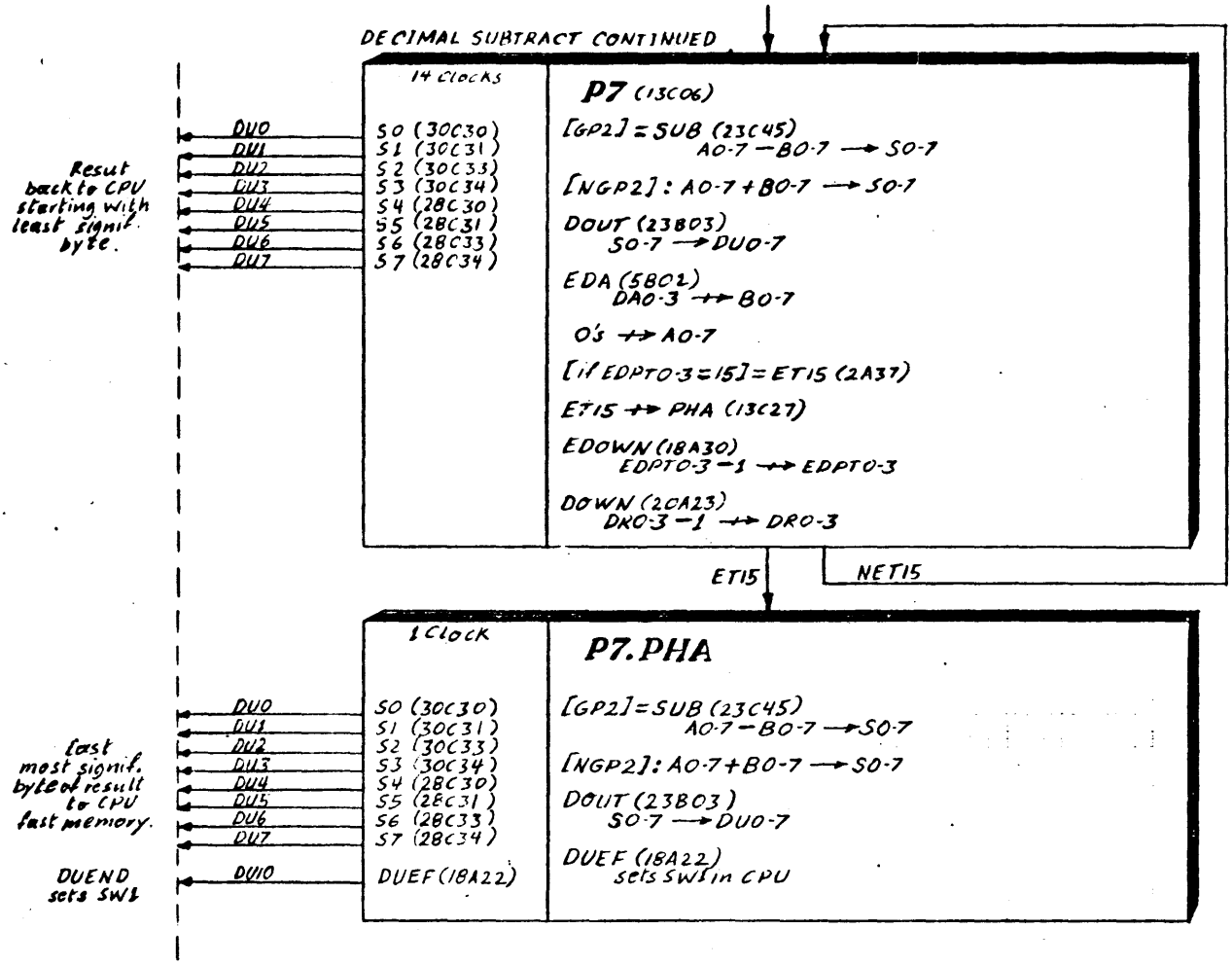
EDOWN (15A30)
EDPTO-3 − 1 →→ EDPTO-3

P6A →→ P7 (13C06)

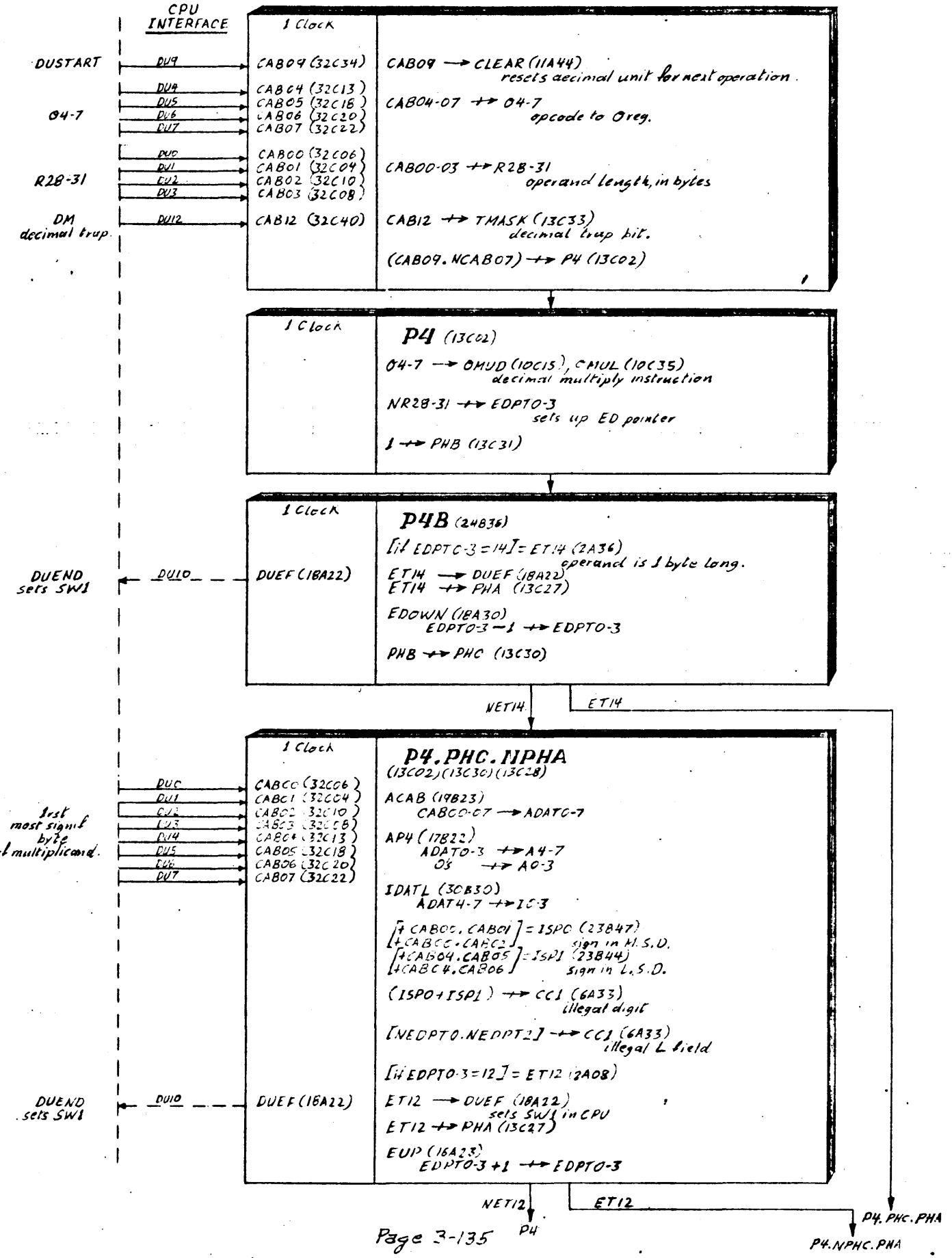
P7

Condition code @ abort information

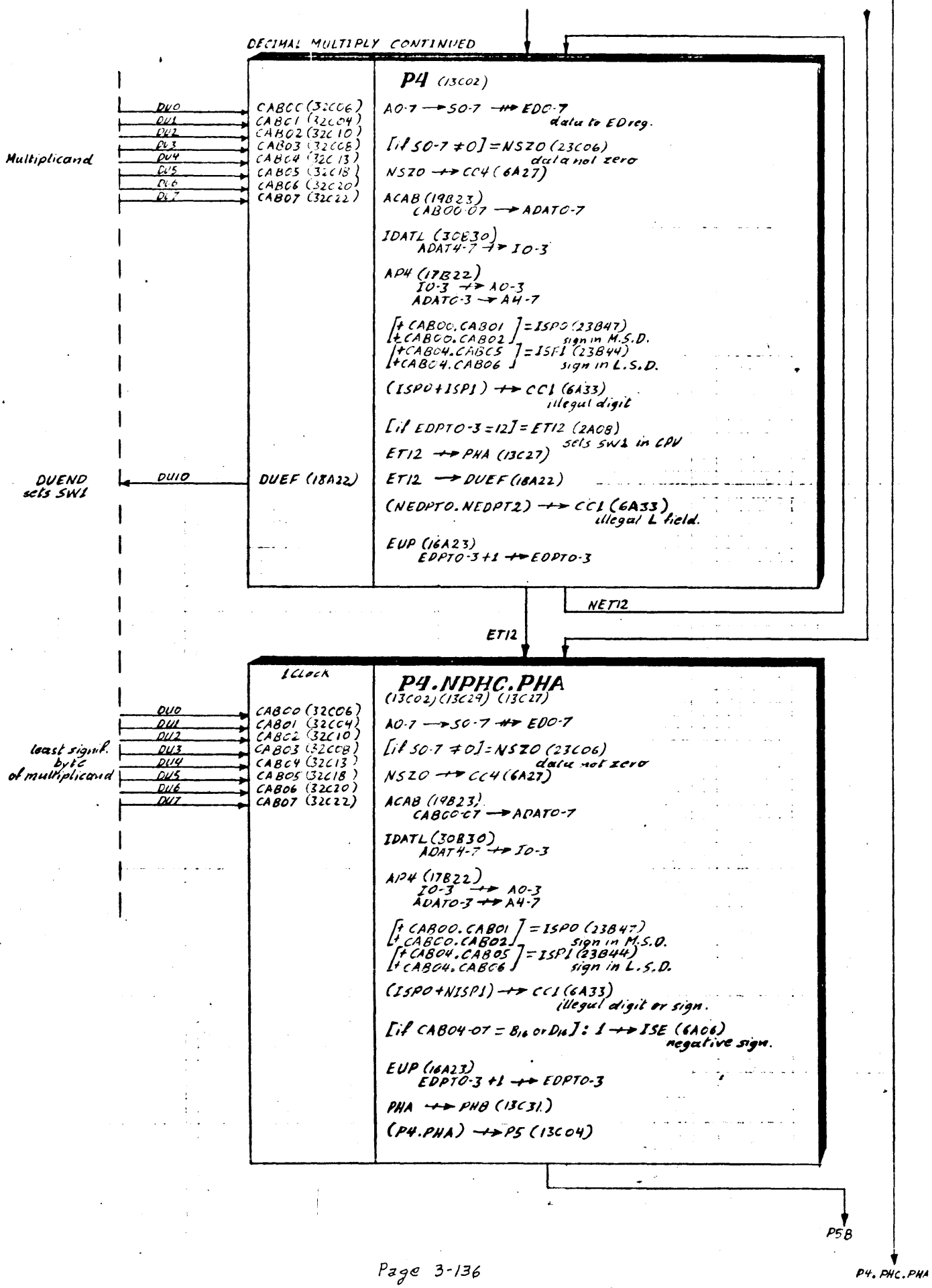
DU0	SC (30C30)	
DU1	S1 (30C31)	
DU2	S2 (30C33)	
DU3	S3 (30C34)	
DU4	S4 (28C30)	
DU5	S5 (28C31)	
DU6	S6 (28C33)	
DU7	S7 (28C34)	


DECIMAL SUBTRACT CONTINUED
14 clocks
P7 (13C06)
[GP2] = SUB (23C45)
A0-7 − B0-7 → S0-7
[NGP2]: A0-7 + B0-7 → S0-7
DOUT (23B03)
S0-7 → DU0-7
EDA (5B02)
DA0-3 → B0-7
0's → A0-7
[if EDPT0-3 = 15] = ET15 (2A37)
ET15 → PHA (13C27)
EDOWN (18A30)
EDPT0-3 − 1 → EDPT0-3
DOWN (20A23)
DR0-3 − 1 → DR0-3
ET15
NET15
1 Clock
P7.PHA
[GP2] = SUB (23C45)
A0-7 − B0-7 → S0-7
[NGP2]: A0-7 + B0-7 → S0-7
DOUT (23B03)
S0-7 → DU0-7
DUEF (18A22)
sets SW1 in CPU
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
DU10
S0 (30C30)
S1 (30C31)
S2 (30C33)
S3 (30C34)
S4 (28C30)
S5 (28C31)
S6 (28C33)
S7 (28C34)
DUEF (18A22)
Result back to CPU starting with least signif. byte.
last most signif. byte of result to CPU fast memory.
DUEND sets SW1

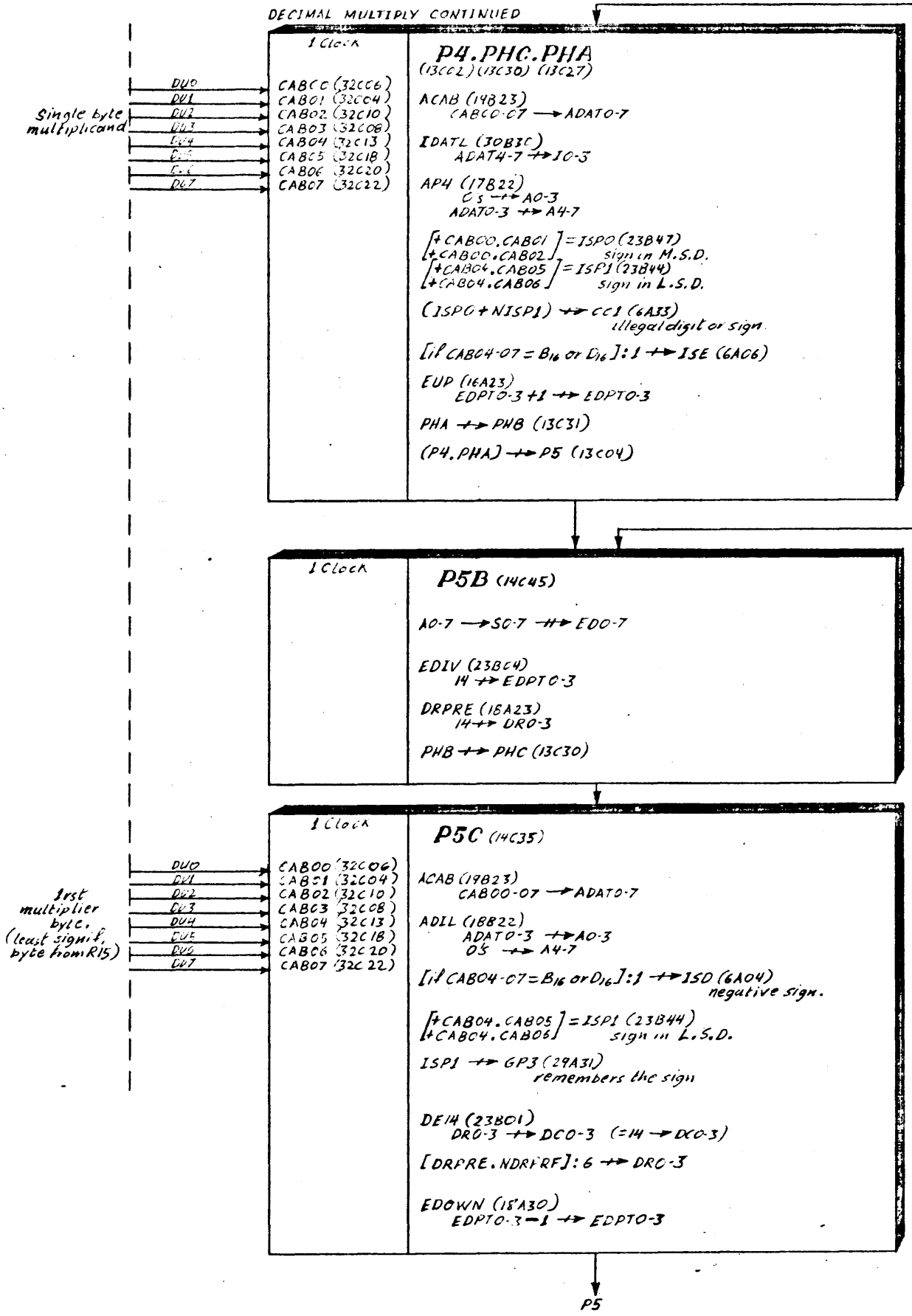
DECIMAL MULTIPLY (78)

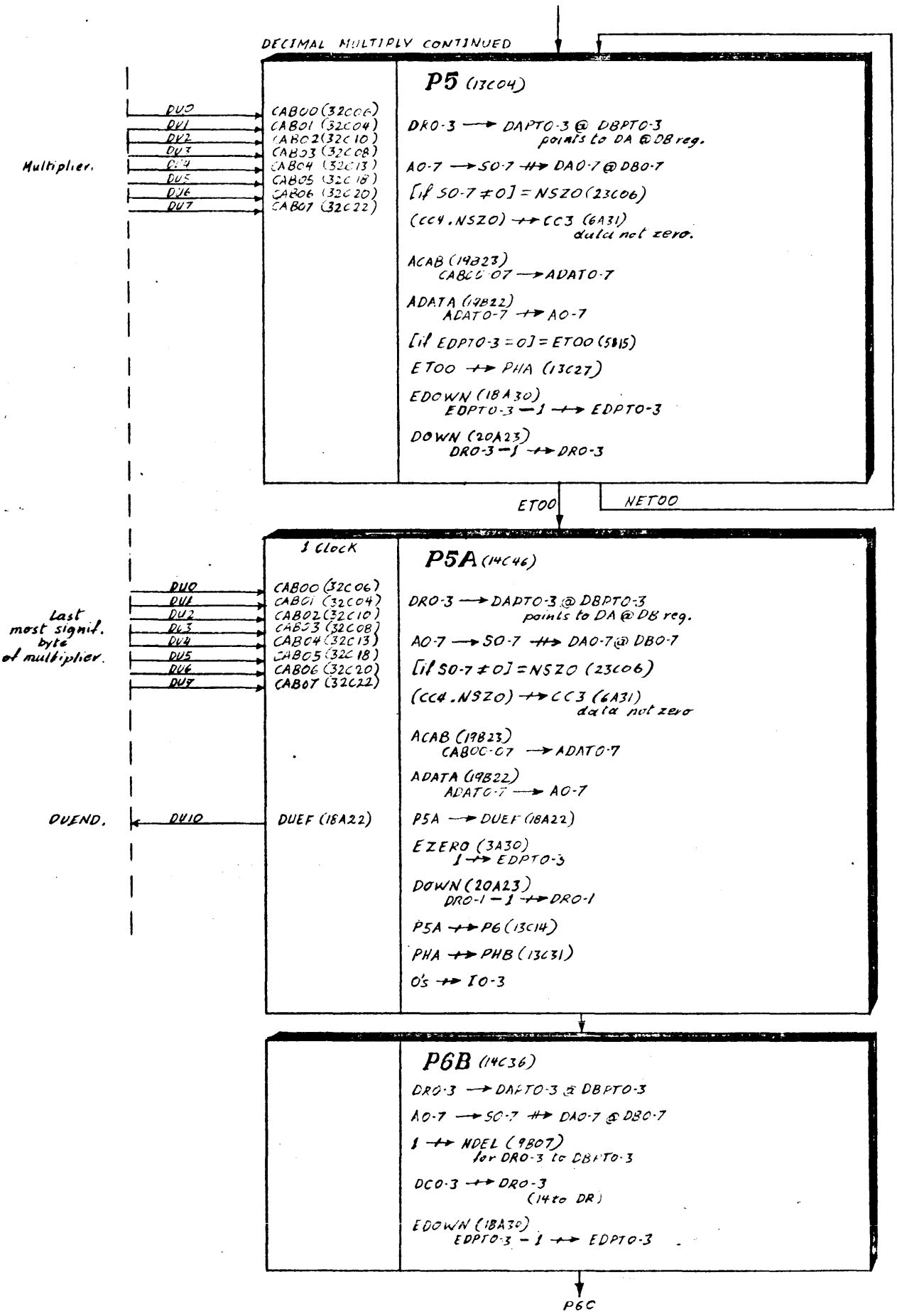


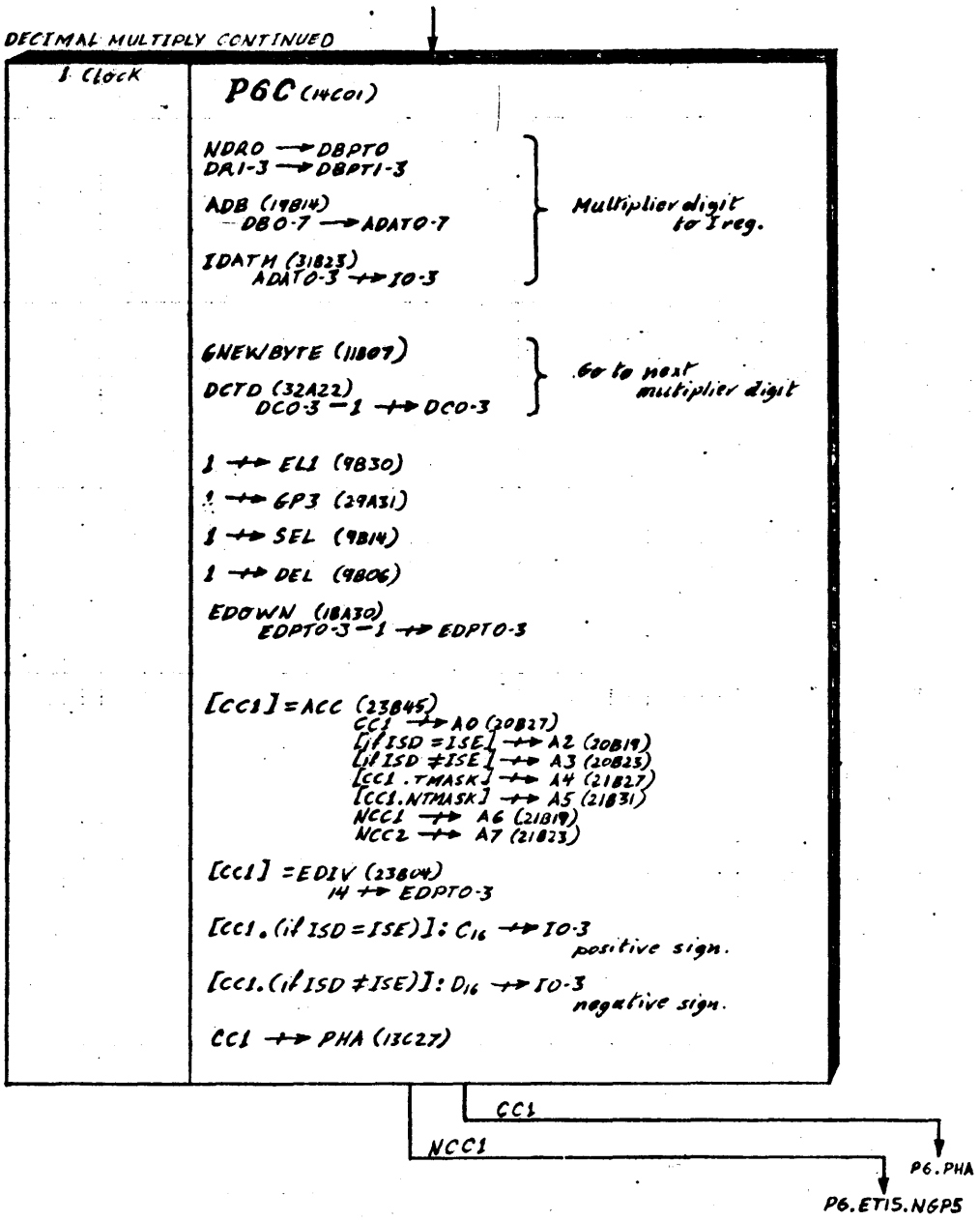
DECIMAL MULTIPLY CONTINUED



DECIMAL MULTIPLY CONTINUED




DECIMAL MULTIPLY CONTINUED
P5 (13C04)
DR0-3 → DAPT0-3 @ DBPT0-3
points to DA @ DB reg.
A0-7 → S0-7 ↔ DA0-7 @ DB0-7
[if S0-7 ≠ 0] = NSZ0 (23C06)
(CC4.NSZ0) ↔ CC3 (6A31)
data not zero.
ACAB (19B23)
CAB0-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 ↔ A0-7
[if EDPT0-3 = 0] = ET00 (5B15)
ET00 ↔ PHA (13C27)
EDOWN (18A30)
EDPT0-3 − 1 ↔ EDPT0-3
DOWN (20A23)
DR0-3 − 1 ↔ DR0-3
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
Multiplier.
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
ET00
NET00
1 Clock
P5A (14C46)
DR0-3 → DAPT0-3 @ DBPT0-3
points to DA @ DB reg.
A0-7 → S0-7 ↔ DA0-7 @ DB0-7
[if S0-7 ≠ 0] = NSZ0 (23C06)
(CC4.NSZ0) ↔ CC3 (6A31)
data not zero
ACAB (19B23)
CAB0-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 → A0-7
P5A → DUEF (18A22)
EZERO (3A30)
1 ↔ EDPT0-3
DOWN (20A23)
DR0-1 − 1 ↔ DR0-1
P5A ↔ P6 (13C14)
PHA ↔ PHB (13C31)
0's ↔ I0-3
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
Last most signif. byte of multiplier.
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
DUEND.
DU10
DUEF (18A22)
P6B (14C36)
DR0-3 → DAPT0-3 @ DBPT0-3
A0-7 → S0-7 ↔ DA0-7 @ DB0-7
1 ↔ NDEL (9B07)
for DR0-3 to DBPT0-3
DC0-3 ↔ DR0-3
(14 to DR)
EDOWN (18A30)
EDPT0-3 − 1 ↔ EDPT0-3
P6C


DECIMAL MULTIPLY CONTINUED
1 Clock
P6C (14C01)
NDRO → DBPTO
DR1-3 → DBPT1-3
ADB (19B14)
DB0-7 → ADAT0-7
IDATM (31B23)
ADAT0-3 → IO-3
Multiplier digit to I reg.
GNEWBYTE (11B07)
DCTD (32A22)
DCO-3 − 1 → DCO-3
Go to next multiplier digit
1 → EL1 (9B30)
1 → GP3 (29A31)
1 → SEL (9B14)
1 → DEL (9B06)
EDOWN (18A30)
EDPTO-3 − 1 → EDPTO-3
[CC1] = ACC (23B45)
CC1 → A0 (20B27)
[if ISD = ISE] → A2 (20B19)
[if ISD ≠ ISE] → A3 (20B23)
[CC1 . TMASK] → A4 (21B27)
[CC1.NTMASK] → A5 (21B31)
NCC1 → A6 (21B19)
NCC2 → A7 (21B23)
[CC1] = EDIV (23B04)
14 → EDPTO-3
[CC1 . (if ISD = ISE)] : C16 → IO-3
positive sign.
[CC1. (if ISD ≠ ISE)] : D16 → IO-3
negative sign.
CC1 → PHA (13C27)
CC1
NCC1
P6.PHA
P6.ET15.NGP5

from P6C

from P6C

DECIMAL MULTIPLY CONTINUED

P6.ET01
(13C14) (5B14)

[DEL]: DWO-3 → DBPTO-3 (DB reg. pointer.)
S0-7 ↛ DBO-7
[NDEL]: DWO-3 → DAPTO-3 (DA reg. pointer.)
S0-7 ↛ DAO-7
} Store last byte of product

[if I:0] = IZERO (15B14)
[IZERO]: DEL → NDEL (9B07)
or
NDEL → DEL (9B06)
} If previous multiplier digit was zero, invert DEL

DCO-3 → DRO-3
for adding multiplicand to proper partial product digit and for accessing proper multiplier digit.

[if IO-3 = 1]: IO-3 − 1 → IO-3
[if IO-3 = 2 or 3 or 4 or 5]: IO-3 − 2 → IO-3
[if IO-3 = 6 or 7 or 8]: IO-3 + 2 → IO-3
[if IO-3 = 9]: IO-3 + 1 → IO-3
} If Ireg is not 0 or 10 increment or decrement Ireg.

EDOWN (18A30)
EDPTO-3 − 1 → EDPTO-3
gives us ET00

P6.ET00
(13C14) (5B15)

[DEL]: NDRO → DAPTO
DR1-3 → DAPT1-3 (address multiplier in DAreg.)
ADA (19B30)
DAO-7 → ADATO-7
[NDEL]: NDRO → DBPTO
DR1-3 → DBPT1-3 (address multiplier in DBreg.)
ADB (19B14)
DBO-7 → ADATO-7
[if IO-3 = 0 or 10] = IZERO (15B14)
[IZERO.SEL] = IDATL (30B30)
ADAT4-7 → IO-3
[IZERO.NSEL] = IDATM (31B23)
ADATO-3 → IO-3
} Multiplier digit to Ireg if IZERO

[IZERO.NSEL] = GNEWBYTE (11B07)
[GNEWBYTE] = DCTO (32A22)
DCO-3 − 1 → DCO-3
} Go to next multiplier byte.

GNEWBYTE → EL1 (9B30)
remembers GNEWBYTE

[if IO-3 = 10]: 1 → GP2 (29A30)
rememembers previous subtraction.

IZERO → GP3 (29A31)
remembers IZERO

[IZERO]: SEL → NSEL (9B12) or NSEL → SEL (9B14)
} Invert SEL

DEL → NDEL (9B07)
NDEL → DEL (9B06)
} Invert DEL

P6.ET15.NGP5

P6.PHA

P6.ET01

from P6C

from P6C

DECIMAL MULTIPLY CONTINUED

[SEL] = DUP (26A22)
DRO-3+1 →→ DRO-3

EDOWN (18A30)
EDPTO-3 −1 →→ EDPTO-3

(NDRO.NDR3) → ELAST (31A46)
last iteration.

14 →→ DRO-3

[ELAST.NSEL] = ACC (23B45)
[(ISD=ISE).CC3] →→ A2 (20A19)
[(ISD≠ISE).CC3] →→ A3 (20A25)
NCC1 →→ A6 (21B19)
NCC2 →→ A7 (21B23).

[ELAST.NSEL] = EDIV (23B04)
14 →→ EDPTO-3

[ELAST.NSEL.(if ISD=ISE)]: C_{16} →→ IO-3
positive sign.

[ELAST.NSEL.(if ISD≠ISE]: D_{16} →→ IO-3
negative sign.

(ELAST.NSEL) →→ PHA (13C27).

} Supersedes previous logic

ELAST.NSEL

P6.ET15.NGP5
(13C14) (2A37) (6A21)

GP3 →→ GP5 (6A02)
remembers IZERO

(GP3.EL1) →→ EL1 (9B30)
remembers GNEWBYTE

[GP2]: IO-3+1 →→ IO-3
increment multiplier digit (multiplicand X10)
if previous multiplier digit was =>6 and
multiplicand was subtracted.

DRO-3 →→ DWO-3

[NGP3] = EDOWN (18A30)
EDPTO-3 −1 →→ EDPTO-3

GP3

NGP3

P6.ET15.GP5
(13C14) (2A37) (6A02)

GP5 → GM15/5 (18C14)

[if IO-3=0] = ITOO (4B34)
new multiplier digit is zero

[GM15/5.ITOO] = EZERO (3A30)
1 → EDPTO-3

[NEZERO] = EDOWN (18A30)
EDPTO-3 −1 →→ EDPTO-3

[NEL1] = DOWN (20A23)
DRO-3 −1 →→ DRO-3

0's →→ ELO-3

DRO-3 →→ DWO-3

EZERO

P6

P6

P6.PHA

from P6

P6.ETO1

DECIMAL MULTIPLY CONTINUED

P6 (13C14)

[DEL]: DRO-3 → DAPTO-3
DA reg. pointer
ADA (19B30)
DAO-7 → ADATO-7

[NDEL]: DRO-3 → DBPTO-3
DB reg. pointer.

ADB (19B14)
DBO-7 → ADATO-7

ADATA (19B22)
ADATO-7 ↠ AO-7

} Partial product to Areg.

EDO-3 ↠ ELO-3

[SEL]: ED4-7 → ESHO-3
ELO-3 → ESH4-7

[NSEL]: EDO-7 → ESHO-7

[if IO-3 = 2-8]: ESHO-7 X2 ↠ BO-7

[if IO-3 = 1 or 9]: ESHO-7 ↠ BO-7

} Multiplicand to Breg.

[if IO-3 = <5] = NSUB (17C23)
AO-7 + BO-7 → SO-7

[if IO-3 => 6] = SUB (2B36)
AO-7 − BO-7 → SO-7

} Add or subtract A and B.

[DEL]: DWO-3 → DBPTO-3
DB reg. pointer

SO-7 ↠ DBO-7

[NDEL]: DWO-3 → DAPTO-3
DA reg. pointer

SO-7 ↠ DAO-7

} Store result.

[if EDPTO-3 = NR2B-31] = EDMA (12A46)

EDMA → EZERO (3A30)
1 ↠ EDPTO-3

[NEZERO] = EDOWN (18A30)
EDPTO-3 − 1 ↠ EDPTO-3

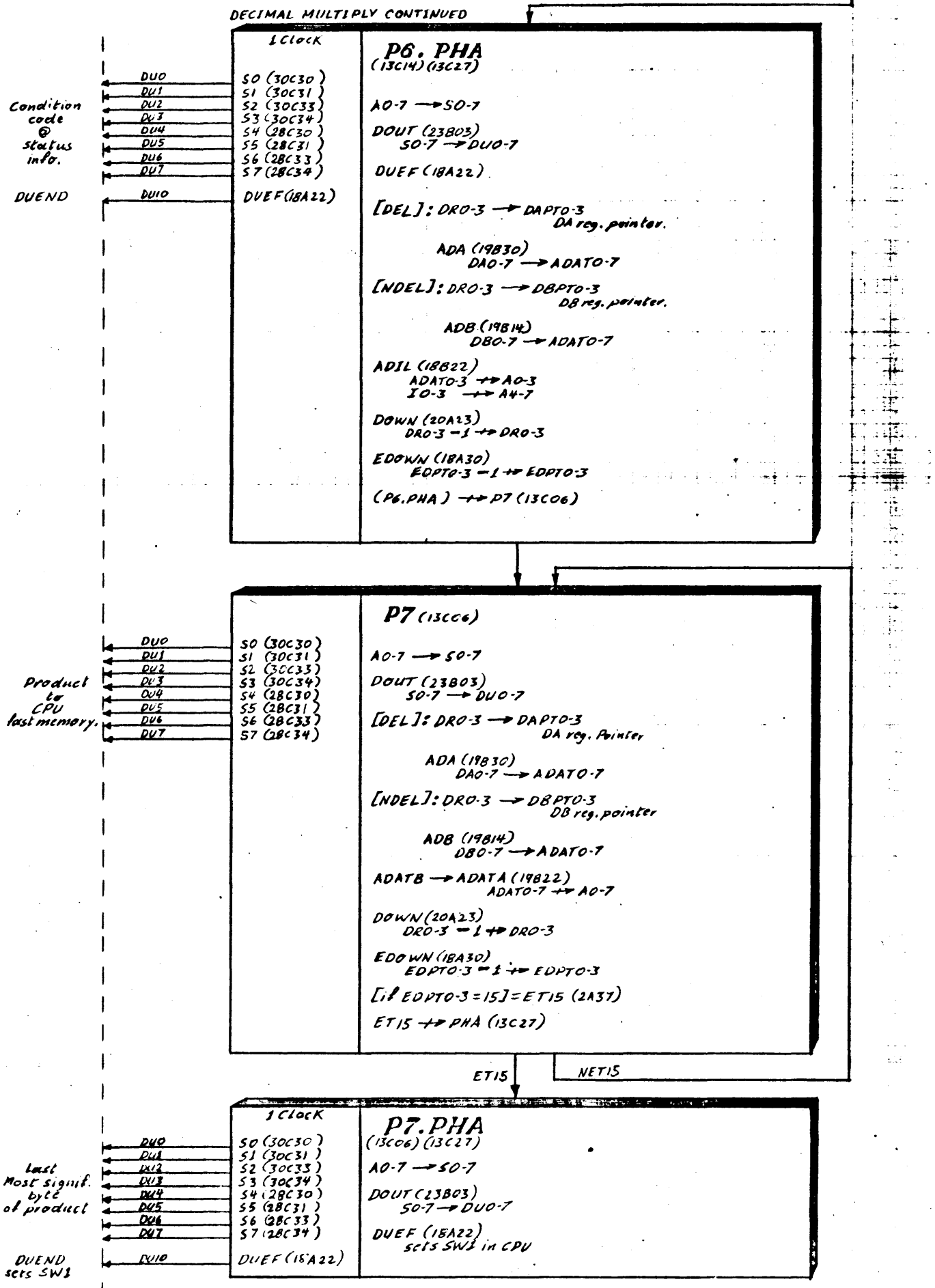
DOWN (20A23)
DRO-3 − 1 ↠ DRO-3

DRO-3 ↠ DWO-3

NEZERO

EZERO

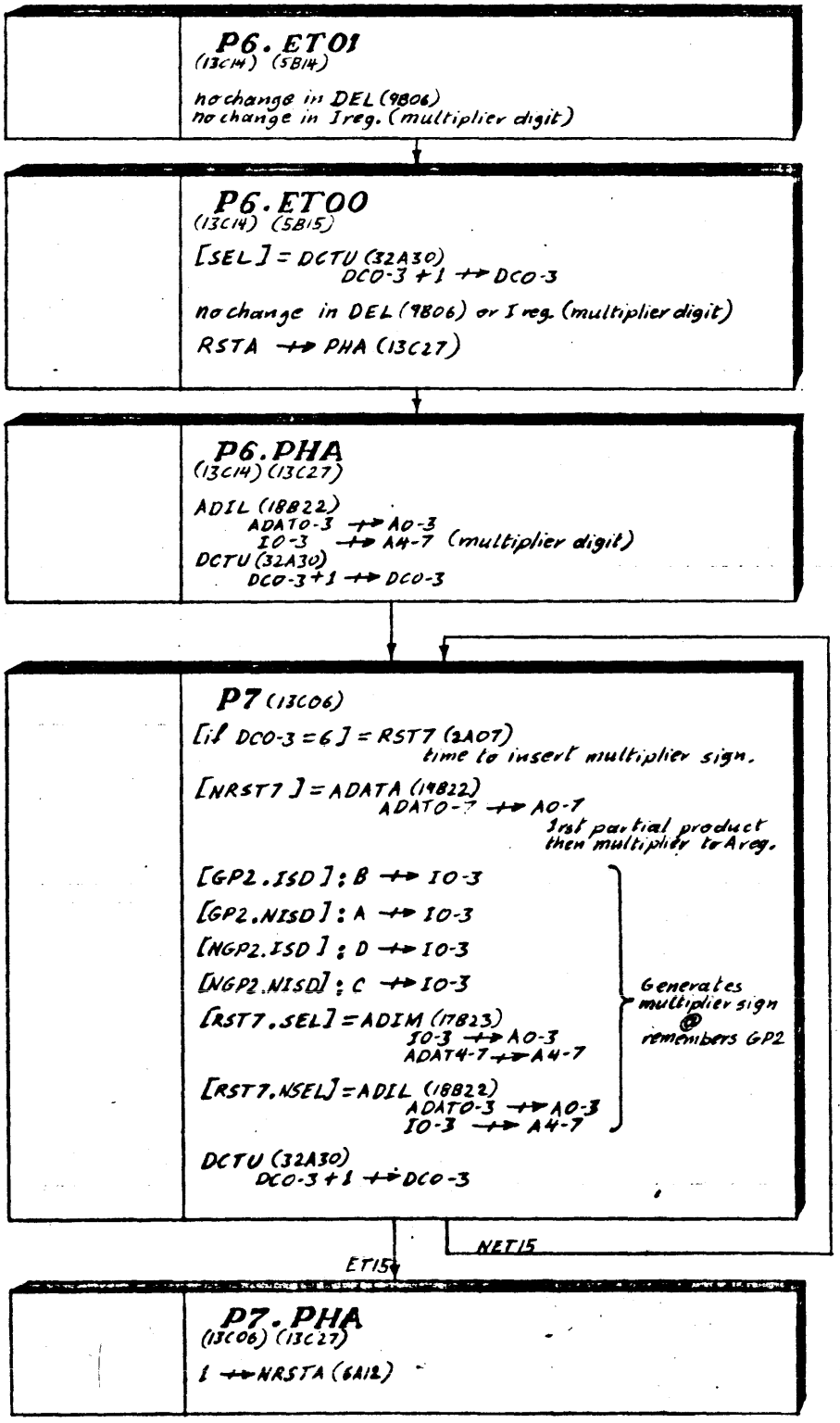
P6.1HA


DECIMAL MULTIPLY CONTINUED
1 Clock
P6. PHA
(13C14) (13C27)
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
Condition code & status info.
S0 (30C30)
S1 (30C31)
S2 (30C33)
S3 (30C34)
S4 (28C30)
S5 (28C31)
S6 (28C33)
S7 (28C34)
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
DUEF (18A22)
DUEND
DU10
DUEF (18A22)
[DEL]: DRO-3 → DAPTO-3
DA reg. pointer.
ADA (19B30)
DAO-7 → ADATO-7
[NDEL]: DRO-3 → DBPTO-3
DB reg. pointer.
ADB (19B14)
DBO-7 → ADATO-7
ADIL (18B22)
ADATO-3 ↔ AO-3
IO-3 ↔ A4-7
DOWN (20A23)
DRO-3 - 1 ↔ DRO-3
EDOWN (18A30)
EDPTO-3 - 1 ↔ EDPTO-3
(P6.PHA) ↔ P7 (13C06)
P7 (13C06)
Product to CPU fast memory.
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
[DEL]: DRO-3 → DAPTO-3
DA reg. Pointer
ADA (19B30)
DAO-7 → ADATO-7
[NDEL]: DRO-3 → DBPTO-3
DB reg. pointer
ADB (19B14)
DBO-7 → ADATO-7
ADATB → ADATA (19B22)
ADATO-7 ↔ AO-7
DOWN (20A23)
DRO-3 - 1 ↔ DRO-3
EDOWN (18A30)
EDPTO-3 - 1 ↔ EDPTO-3
[if EDPTO-3 = 15] = ET15 (2A37)
ET15 ↔ PHA (13C27)
ET15
NET15
1 Clock
P7. PHA
(13C06) (13C27)
Last Most signif. byte of product
DUEND sets SW1
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
DUEF (18A22)
sets SW1 in CPU

DECIMAL MULTIPLY INTERRUPTED

(differences only)

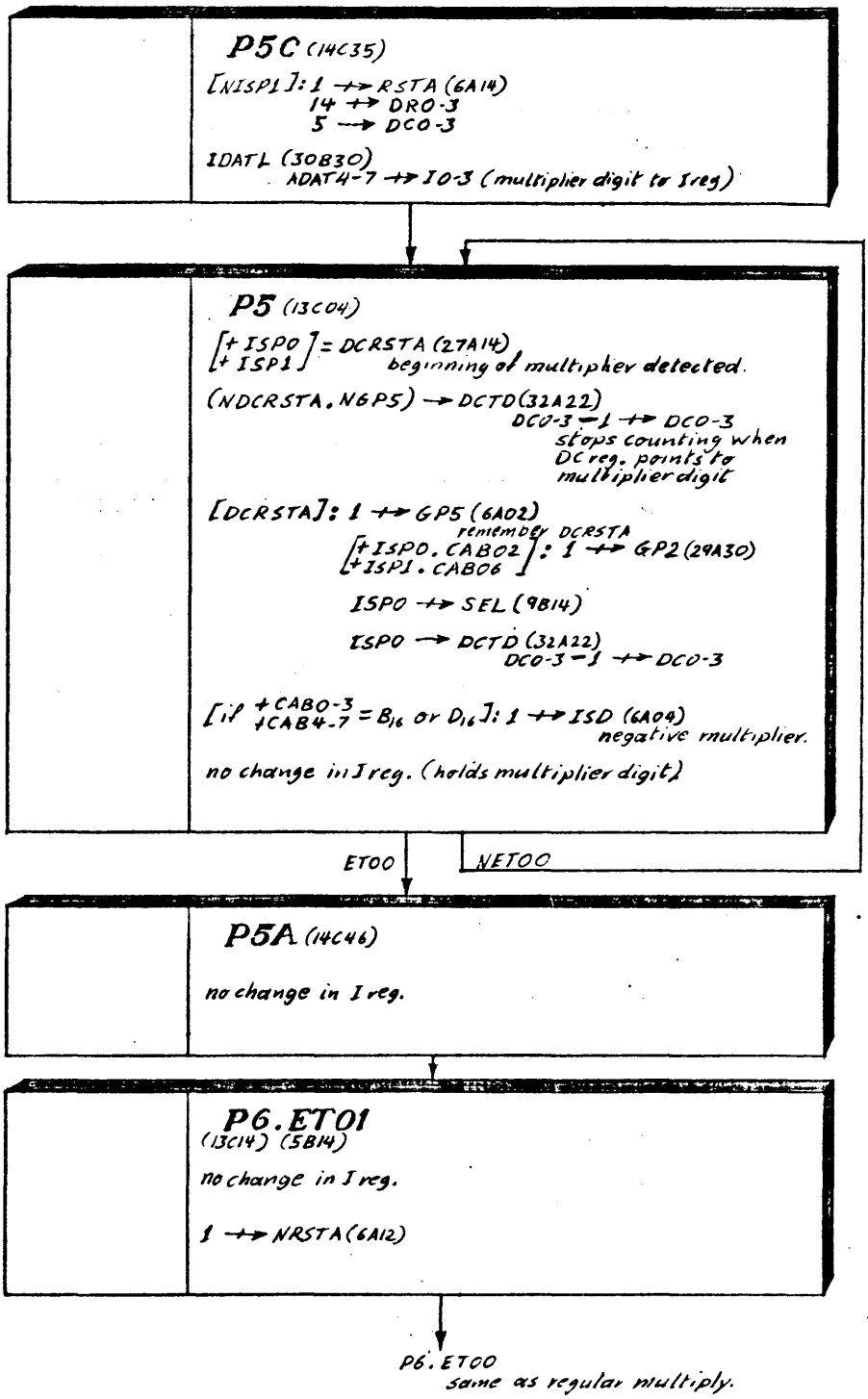
INT (in CPU) → DU12 → CAB12 (32C40)
(CAB12.P6.ET00) → RSTA (6A14)
wait for next ET01



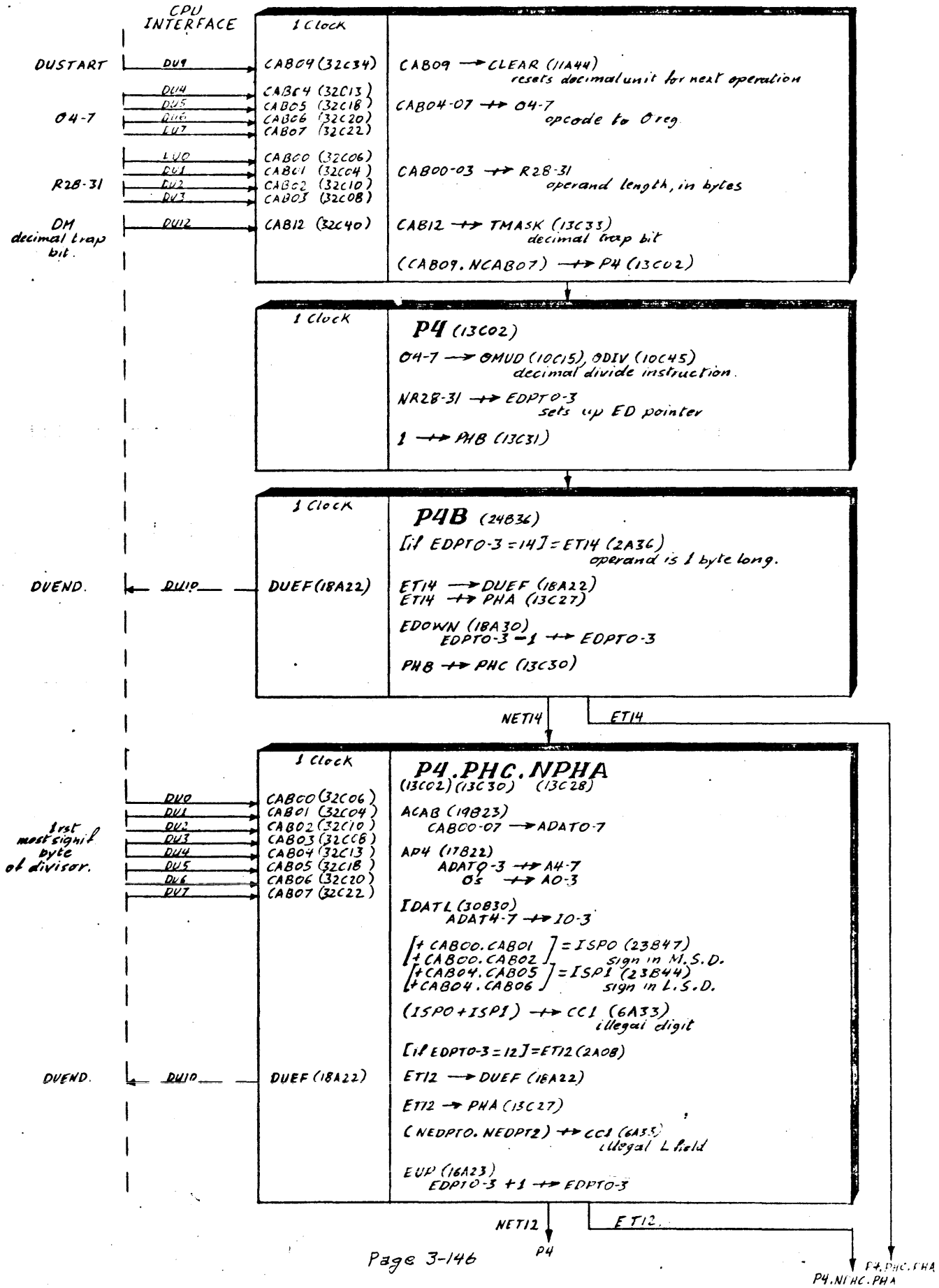
MULTIPLY REENTRY AFTER INTERRUPT

(differences only)

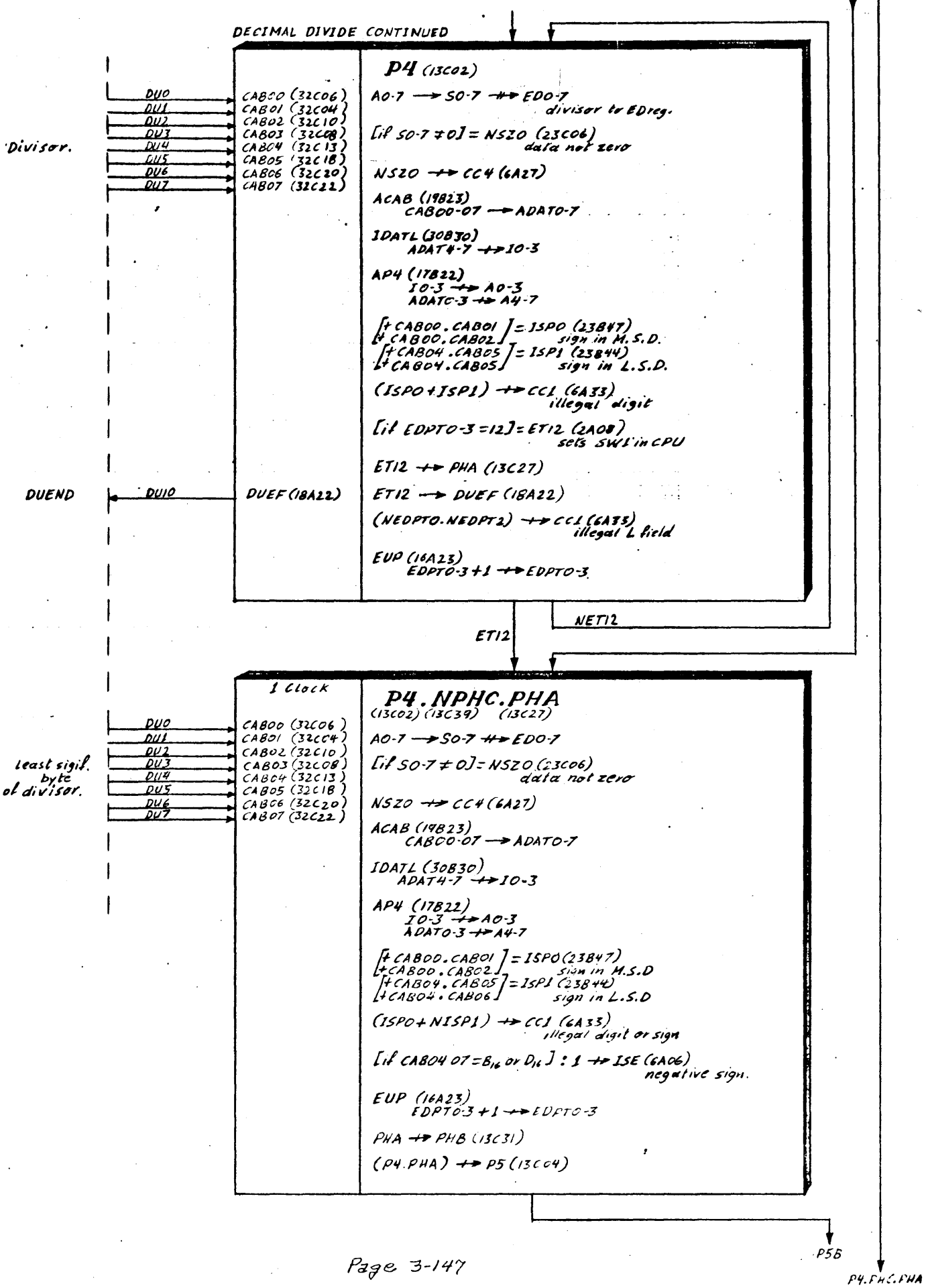
Same as regular multiply untill P5C



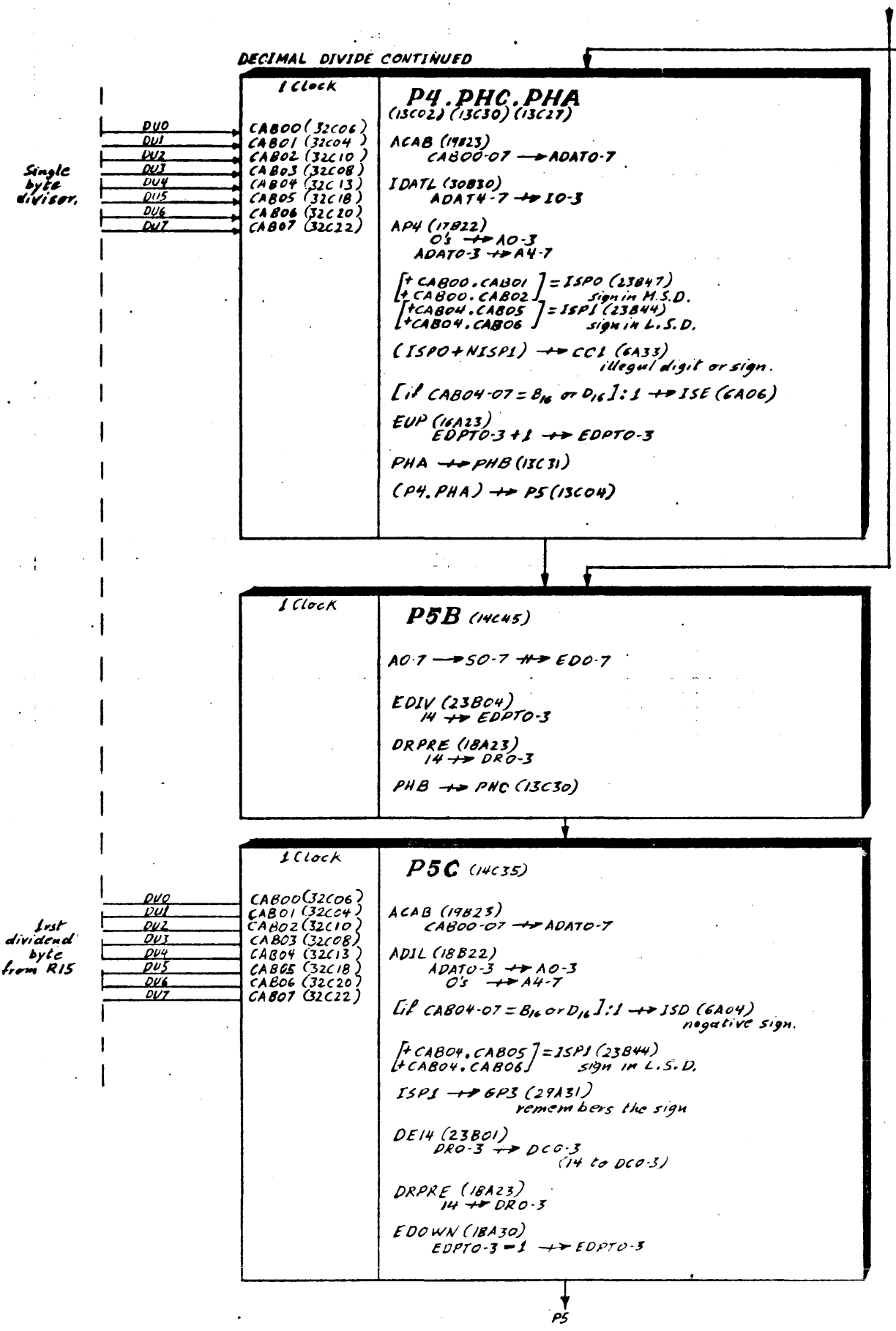
DECIMAL DIVIDE (7A)

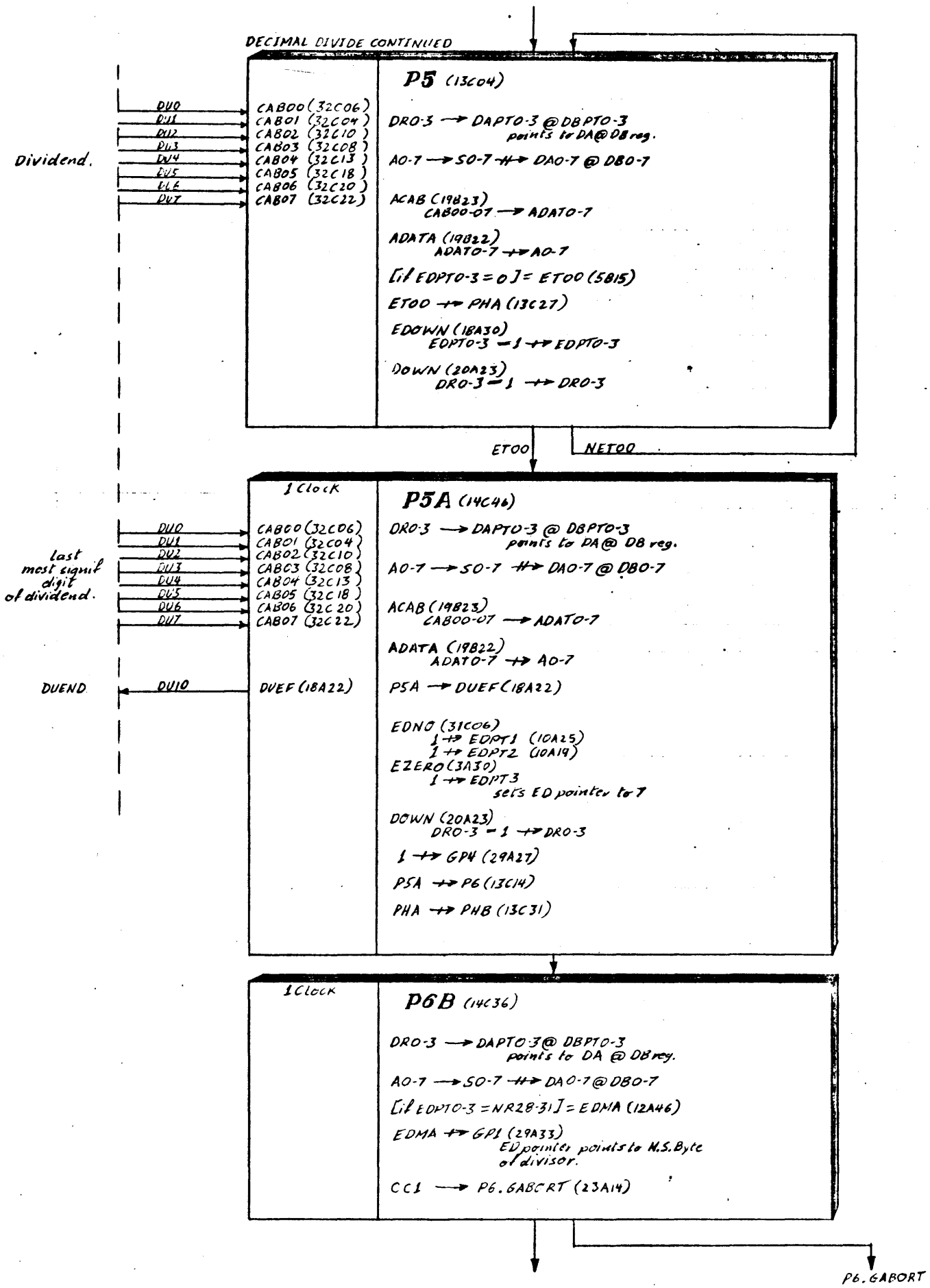


DECIMAL DIVIDE CONTINUED



DECIMAL DIVIDE CONTINUED




DECIMAL DIVIDE CONTINUED
P5 (13C04)
DR0-3 → DAPT0-3 @ DBPT0-3
points to DA@DB reg.
A0-7 → S0-7 ⇉ DA0-7 @ DB0-7
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 ⇉ A0-7
[if EDPT0-3 = 0] = ET00 (5B15)
ET00 ⇉ PHA (13C27)
EDOWN (18A30)
EDPT0-3 − 1 ⇉ EDPT0-3
DOWN (20A23)
DR0-3 − 1 ⇉ DR0-3
DV0
DV1
DV2
DV3
DV4
DV5
DV6
DV7
Dividend.
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
ET00
NET00
1 Clock
P5A (14C46)
DR0-3 → DAPT0-3 @ DBPT0-3
points to DA@ DB reg.
A0-7 → S0-7 ⇉ DA0-7 @ DB0-7
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 ⇉ A0-7
PSA → DUEF (18A22)
EDNO (31C06)
1 ⇉ EDPT1 (10A25)
1 ⇉ EDPT2 (10A19)
EZERO (3A30)
1 ⇉ EDPT3
sets ED pointer to 7
DOWN (20A23)
DR0-3 − 1 ⇉ DR0-3
1 ⇉ GP4 (29A27)
PSA ⇉ P6 (13C14)
PHA ⇉ PHB (13C31)
last most signif digit of dividend.
DV0
DV1
DV2
DV3
DV4
DV5
DV6
DV7
DUEND
DV10
DUEF (18A22)
1 Clock
P6B (14C36)
DR0-3 → DAPT0-3 @ DBPT0-3
points to DA @ DB reg.
A0-7 → S0-7 ⇉ DA0-7 @ DB0-7
[if EDPT0-3 = NR28-31] = EDMA (12A46)
EDMA ⇉ GP1 (29A33)
ED pointer points to M.S. Byte of divisor.
CC1 → P6.GABORT (23A14)
P6.GABORT

DECIMAL DIVIDE CONTINUED

P6.GP4 (13C14) (29A27) Normalization

[(B0-7 ≠ 0).GP1.NGP3] = BSIGF (11B37)
first none zero byte in divisor

[BSIGF]: 1 → GP3 (29A31)
stops ED pointer until none zero dividend byte is detected.

[BSIGF] = EDOWN (18A30)
EDPTO-3 − 1 → EDPTO-3
go back to none zero divisor byte.
DOWN (20A23)
DRO-3 − 1 → DRO-3
back up DRO-3 same as ED pointer.

} None zero byte in divisor

[(A0-7 ≠ 0).NGP2] = ASIGF (24B14)
first none zero byte in dividend

[ASIGF]: 1 → GP2 (29A30)
allows the count down of DRO-3 and EDPTO-3 with GP3 set.

} None zero byte in dividend

[+ASIGF.NBSIGF.(A0-3 ≠ 3)] = EUP (16A23)
[+ASIGF.NBSIGF.(B0-3 = 0)] EDPTO-3 + 1 → EDPTO-3

[+ASIGF.(A0-3 = 0).(B0-3 ≠ 0)]: 1 → SEL (9B14)
[+ASIGF.(A0-3 ≠ 0).(B0-3 = 0)]
shifts divisor 1 digit left

} Align M.S.D of divisor with M.S.D of dividend

ED0-7 → B0-7
divisor to B reg.

ADA (19B30)
DA0-7 → ADATO-7

ADATA (19B22)
ADATO-7 → A0-7
dividend to A reg.

[if EDPTO-3 = NR28-31] = EDMA (12A46)

EDMA → GP1 (29A33)
ED pointer now looking at divisor.

[GP2.NGP3]: 1 → CC2 (6A30)
overflow, abort the operation.

[+(DRO-3 = 15).GP3
[+(EDPTO-3 = 15).GP2] = GP4R (27A30)
normalization finished.

[GP4R]: 1 → NGP4 (29A28)
1 → NGP3 (29A26)
1 → NGP2 (29A29)
EZERO (3A30)
1 → EDPTO-3

[NBSIGF.NGP3] = EUP (16A23)
EDPTO-3 + 1 → EDPTO-3

[NGP4R.GP2.GP3] = EUP (16A23)
EDPTO-3 + 1 → EDPTO-3

[NGP4R]: DRO-3 → DCO-3
keeps track of difference between divisor and dividend for proper subtraction.

[NASIGF.NBSIGF] = DUP (26A22)
DRO-3 + 1 → DRO-3

GP4.NCC2

S/C22

EZERO

P6.GABORT

DECIMAL DIVIDE CONTINUED

P6.ET01
(13C14) (5814)

P6 → SUB (2B36)

A0-7 − B0-7 → S0-7

[DEL]: DW0-3 → DBPT0-3
S0-7 → DB0-7

[NDEL]: DW0-3 → DAPT0-3
S0-7 → DA0-7

} store last byte of new dividend.

DC0-3 ↔ DR0-3

EDOWN (18A30)
EDPT0-3 − 1 ↔ EDPT0-3
go to ET00

P6.ET00
(13C14) (5815)

I3. ↔ GP3 (29A31)
remembers to store quotient digit.

[NI3.NI0.NSC0S]: I0-3 + 2 ↔ I0-3
[I0.NI3.NSC0S]: I0-3 + 1 ↔ I0-3
[SC0S]: I0-3 − 1 ↔ I0-3

} Update quotient digit held in I reg..

(NSC0S.DEL) ↔ NDEL (9B07)
(NSC0S.NDEL) ↔ DEL (9B06)

} Invert DEL

[NSC0S. (I ≠ 0). (DC0-3 = 6)]: 1 ↔ CC2 (6A30)
overflow

EDOWN (18A30)
EDPT0-3 − 1 ↔ EDPT0-3

CC2

P6.ET15
(13C14) (2A37)

[I0-3 ≠ 0]: 1 → CC3 (6A31)
quotient not zero,

[GP3]: 1 ↔ GP2 (29A30)
remembers to store quotient digit

NDR0 → DAPT0 + DBPT0
DRI-3 → DAPTI-3 + DBPTI-3

[ADA]: DA0-7 → ADAT0-7
[ADB]: DB0-7 → ADA0-7

[GP3.NSEL]: ADIL (1EB22)
I0-3 ↔ A4-7

[GP3.SEL]: ADIM (17B23)
I0-3 ↔ A0-3
ADAT4-7 ↔ A4-7

} Put quotient digits in A reg.

[GP3.NSEL]: DCTU (32A30)
DC0-3 + 1 ↔ DC0-3

(GP3.SEL) ↔ NSEL (9812)
(GP3.NSEL) ↔ SEL (98M)

[GP3]: 0's ↔ I0-3

[NGP3] = EDOWN (18A30)
EDPT0-3 − 1 ↔ EDPT0-3

NGP3

P6.ET15.GP2

P6.GABORT

P6.ET01

DECIMAL DIVIDE CONTINUED

P6.ET15.GP2
(13C14) (2A37) (27A30)

DCOM (23A22)
NDRO → DAPTO @ DBPTO
DRI-3 → DAPTI-3 @ DBPTI-3
A0-7 → S0-7 → DAO-7 @ DB0-7
} Store quotient byte in both DA and DB reg.

[GP2]: 2 → IO-3

[SEL.NDT14] = DUP (26A22)
DRO-3 + 1 → DRO-3

[NDT14] = EDOWN (18A30)
EDPTO-3 − 1 → EDPTO-3

[if DRO-3 = 14] = DT14 (21A38)
[DT14] = ACC (23B45) go to ET14
[CC3.(ISD=ISE)] → A2
[CC3.(ISD≠ISE)] → A3
NCC1 → A6
NCC2 → A7

[ISD=ISE]: C_{16} → IO-3
positive sign.

[ISD≠ISE]: D_{16} → IO-3
negative sign.

} END of divide iterations.

EDIV (23B04)
14 → EDPTO-3

DRPRE (18A23)
14 → DRO-3

[DT14]: 1 → PHA (13C27)

DT14

P6.ET14
(13C14) (2A36)

[DEL]: DRO-3 → DAPTO-3
ADA
DAO-7 → ADATO-7

[NDEL]: DRO-3 → DBPTO-3
ADB
DBO-7 → ADATO-7

ADATA (19B22)
ADATO-7 → AO-7

} Dividend to Areg.

EDO-3 → ELO-3

[NSEL]: EDO-7 → ESHO-7

[SEL]: EDH-7 → ESHO-3
ELO-3 → ESH4-7

[NI3]: ESHO-7 X2 → BO-7

[I3]: ESHO-7 → BO-7

} Divisor to Breg.

[if EDPTO-3 = NR28-31] = EDMA (12A46)

[EDMA] = EZERO (3A30)
1 → EUPTO-3

[NEDMA] = EDOWN (16A30)
EDPTO-3 − 1 → EDPTO-3

DRO-3 → DW/O-3

DOWN (20A23)
DRO-3 − 1 → DRO-3

P6

P6.PHA

P6.GABORT

P6.ETOI

P6.PHA

P6.GABORT

DECIMAL DIVIDE CONTINUED

P6 (13C14)

P6 → SUB (2B36)

A0-7 − B0-7 → S0-7

[DEL]: DW0-3 → DBPT0-3
S0-7 ↛ DB0-7

[NDEL]: DW0-3 → DAPT0-3
S0-7 ↛ DA0-7

[DEL]: DR0-3 → DAPT0-3
ADA (19B30)
DA0-7 → ADAT0-7

[NDEL]: DR0-3 → DBPT0-3
ADB (19B14)
DB0-7 → ADAT0-7

ED0-3 ↛ EL0-3

[NSEL]: ED0-7 → ESH0-7

[SEL]: ED4-7 → ESH0-3
EL0-3 → ESH4-7

[NI3]: ESH0-7x2 ↛ B0-7

[I3]: ESH0-7 ↛ B0-7

[if EDPT0-3 = NR28-31] = EDMA (12A46)

[EDMA] = EZERO (3A30)
1 ↛ EDPT0-3

[NEZERO] = EDOWN (18A30)
EDPT0-3 − 1 ↛ EDPT0-3

DR0-3 ↛ DW0-3

DOWN (20A23)
DR0-3 − 1 ↛ DR0-3

NEZERO

EZERO

P6.GABORT
(13C14) (23A14)

ACC (23B45)
CC1 ↛ A0 (20B27)
CC2 ↛ A1 (20B31)
[CC3.(ISD=ISE) ↛ A2 (20B19)
[CC3.(ISD≠ISE) ↛ A3 (20B23)
(CC1.TMASK) ↛ A4 (21B27)
(CC1.NTMASK) ↛ A5 (21B31)
NCC1 ↛ A6 (21B19)
NCC2 ↛ A7 (21B23)

[ISD=ISE]: C_{16} ↛ I0-3
positive sign.

[ISD≠ISE]: D_{16} ↛ I0-3
negative sign.

EDIV (23B04)
14 ↛ EDPT0-3

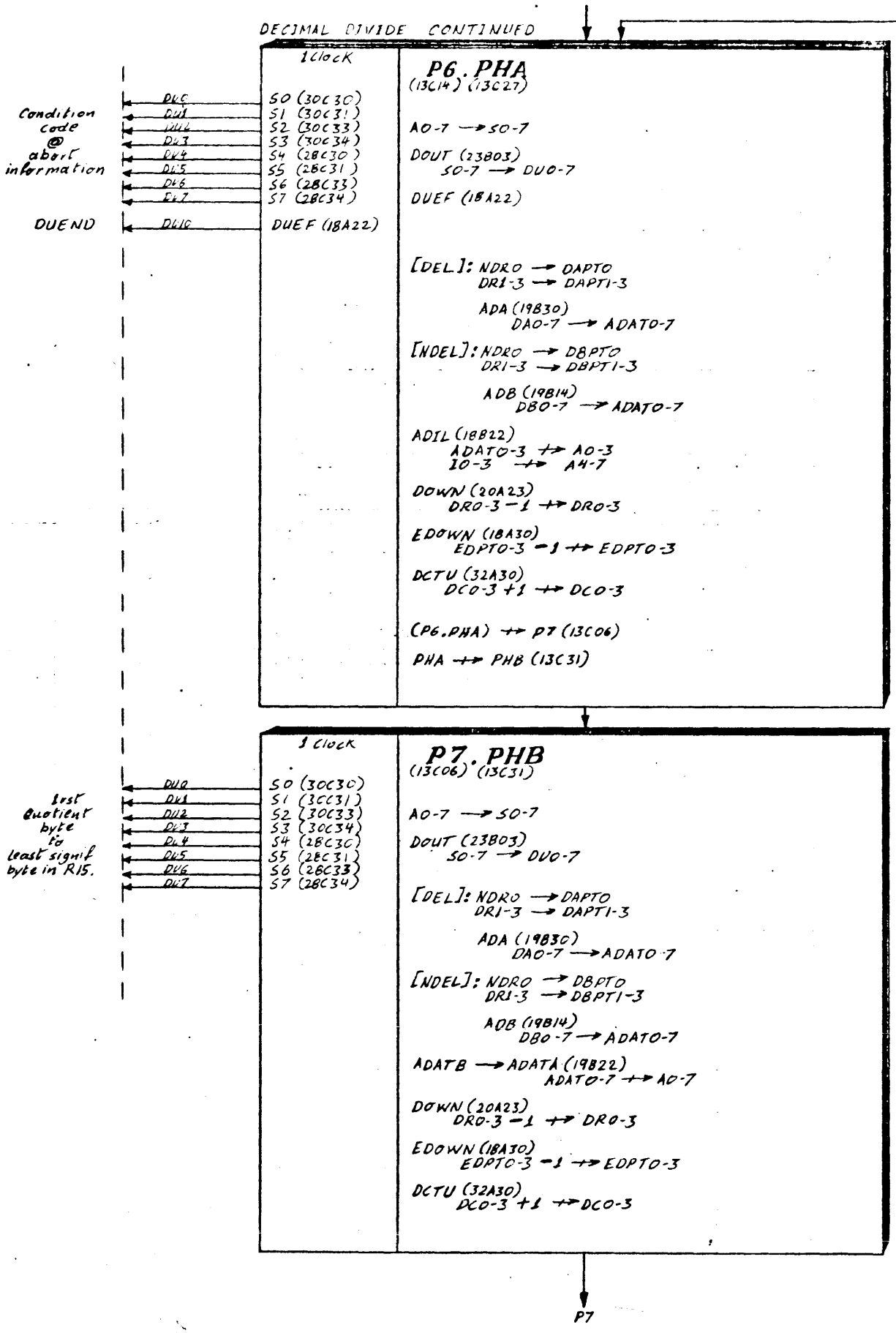
DRPRE (18A23)
14 ↛ DR0-3

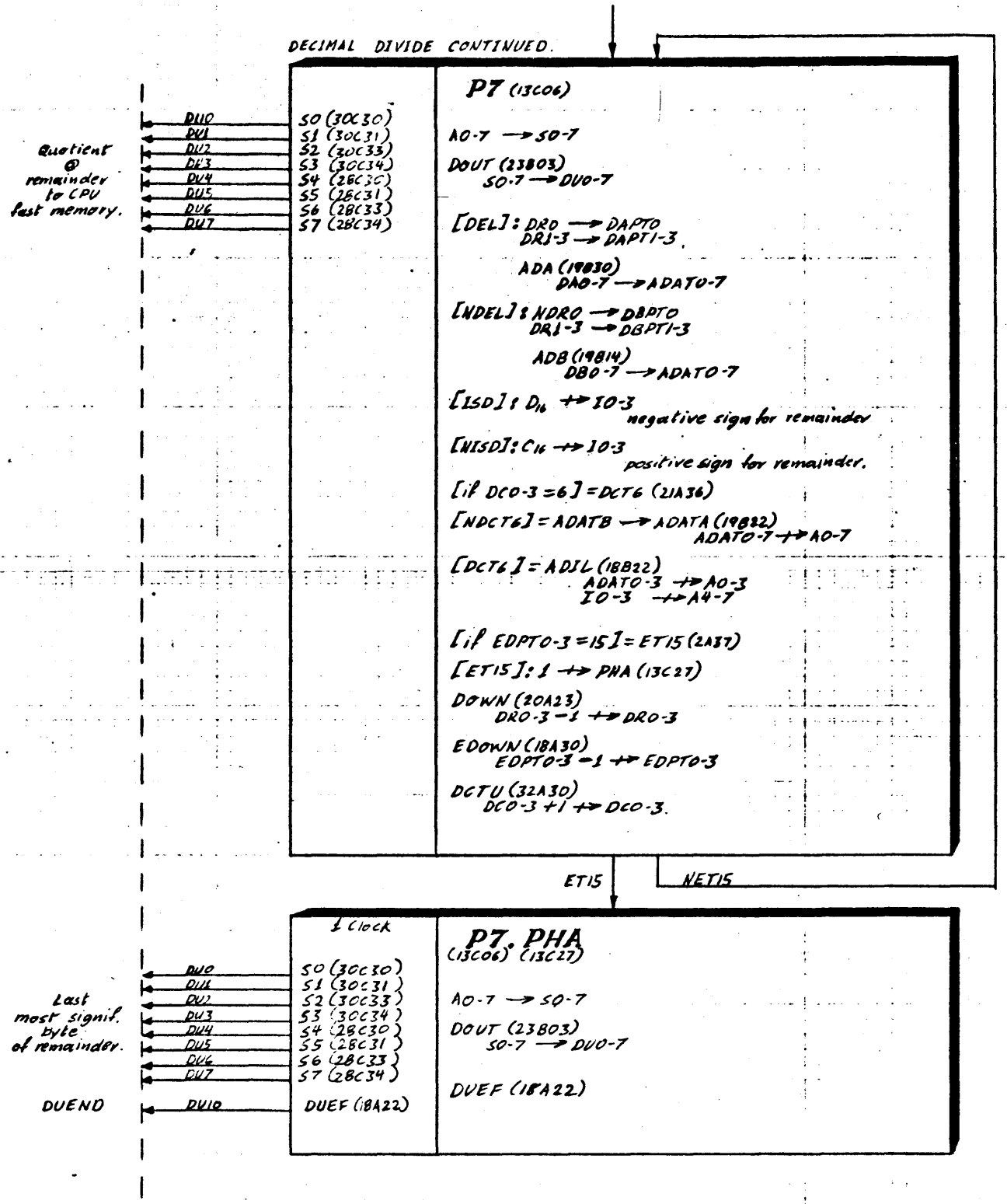
1 ↛ PHA (13C27)

P6.PHA

P6.PHA

DECIMAL DIVIDE CONTINUED




DECIMAL DIVIDE CONTINUED.
P7 (13C06)
Quotient @ remainder to CPU fast memory.
DU0 S0 (30C30)
DU1 S1 (30C31)
DU2 S2 (30C33)
DU3 S3 (30C34)
DU4 S4 (28C30)
DU5 S5 (28C31)
DU6 S6 (28C33)
DU7 S7 (28C34)
A0-7 → S0-7
DOUT (23B03)
S0-7 → DU0-7
[DEL]: DR0 → DAPT0
DR1-3 → DAPT1-3
ADA (19B30)
DA0-7 → ADAT0-7
[NDEL]: NDR0 → DBPT0
DR1-3 → DBPT1-3
ADB (19B14)
DB0-7 → ADAT0-7
[ISD]: D16 ↠ I0-3
negative sign for remainder
[NISD]: C16 ↠ I0-3
positive sign for remainder.
[if DC0-3 = 6] = DCT6 (21A36)
[NDCT6] = ADATB → ADATA (19B32)
ADAT0-7 ↠ A0-7
[DCT6] = ADJL (18B22)
ADAT0-3 ↠ A0-3
I0-3 ↠ A4-7
[if EDPT0-3 = 15] = ET15 (21A37)
[ET15]: 1 ↠ PHA (13C27)
DOWN (20A23)
DR0-3 − 1 ↠ DR0-3
EDOWN (18A30)
EDPT0-3 − 1 ↠ EDPT0-3
DCTU (32A30)
DC0-3 + 1 ↠ DC0-3.
ET15
NET15
1 Clock
P7. PHA
(13C06) (13C27)
Last most signif. byte of remainder.
DU0 S0 (30C30)
DU1 S1 (30C31)
DU2 S2 (30C33)
DU3 S3 (30C34)
DU4 S4 (28C30)
DU5 S5 (28C31)
DU6 S6 (28C33)
DU7 S7 (28C34)
A0-7 → S0-7
DOUT (23B03)
S0-7 → DU0-7
DUEND
DU10 DUEF (18A22)
DUEF (18A22)

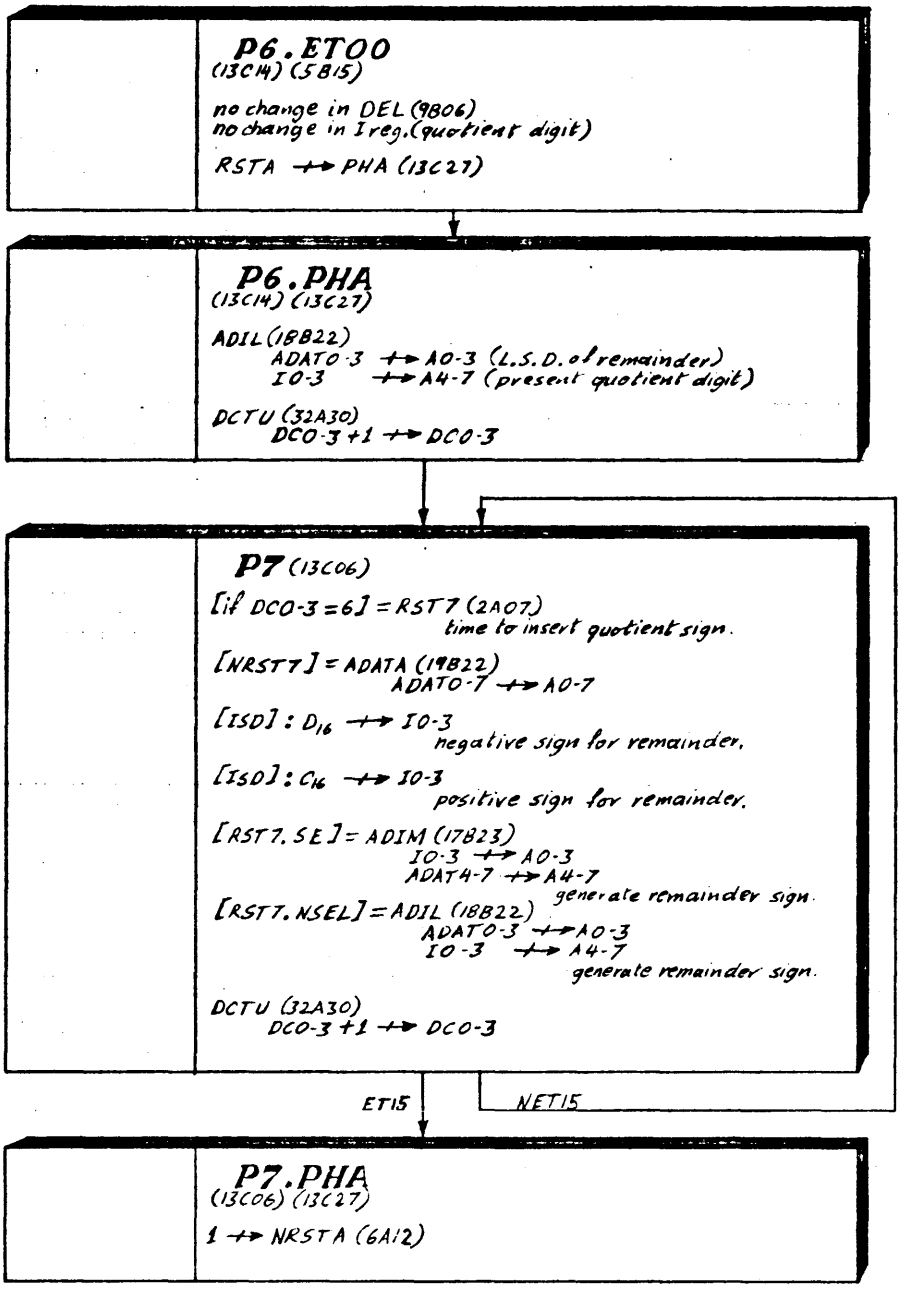
DECIMAL DIVIDE INTERRUPTED

(differences only)

INT (in CPU) → DU12 → CAB12 (32C40)

(CAB12.P6.ETOO) ↔ RSTA (6A14)

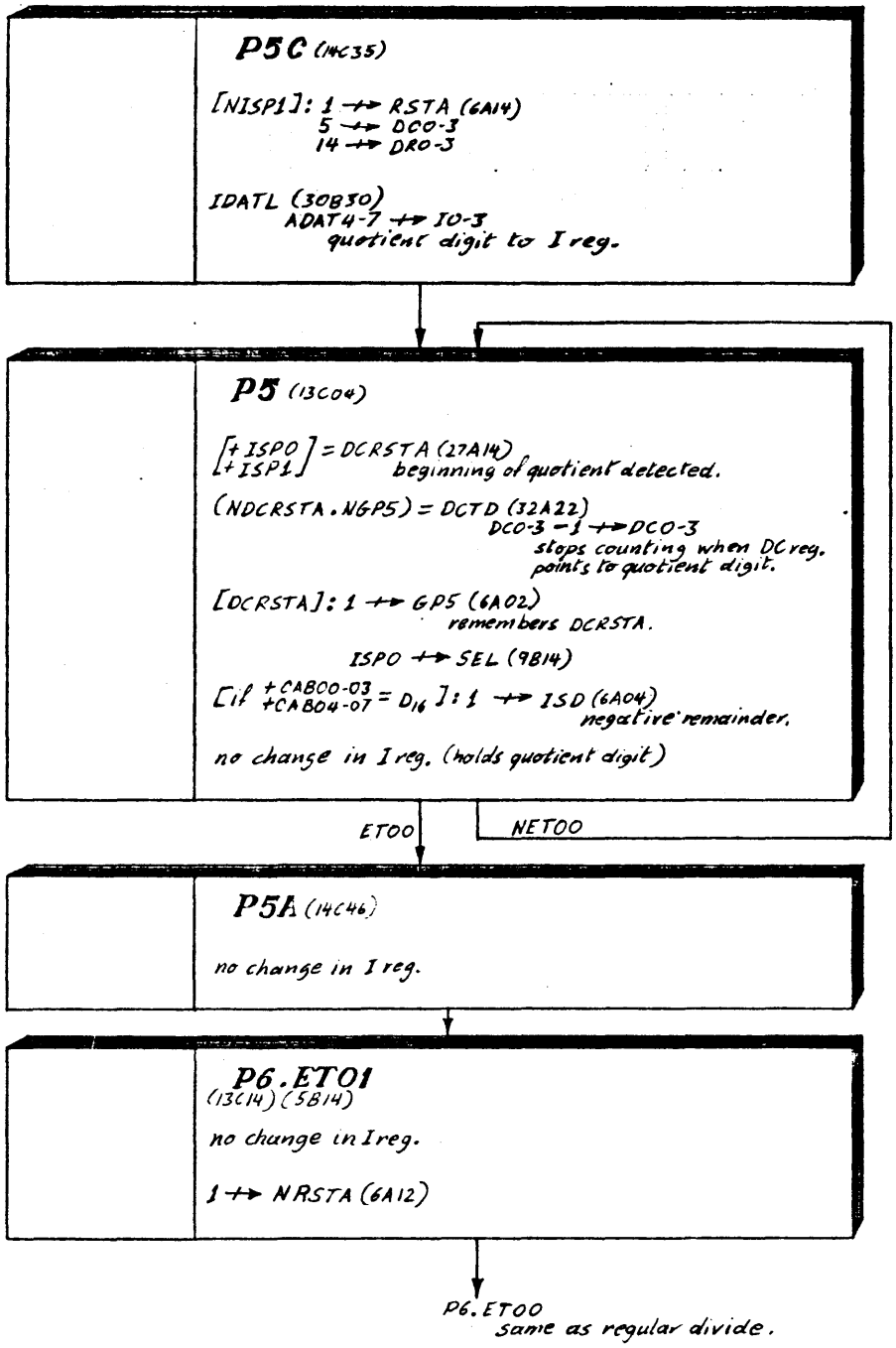
wait for next ETOO



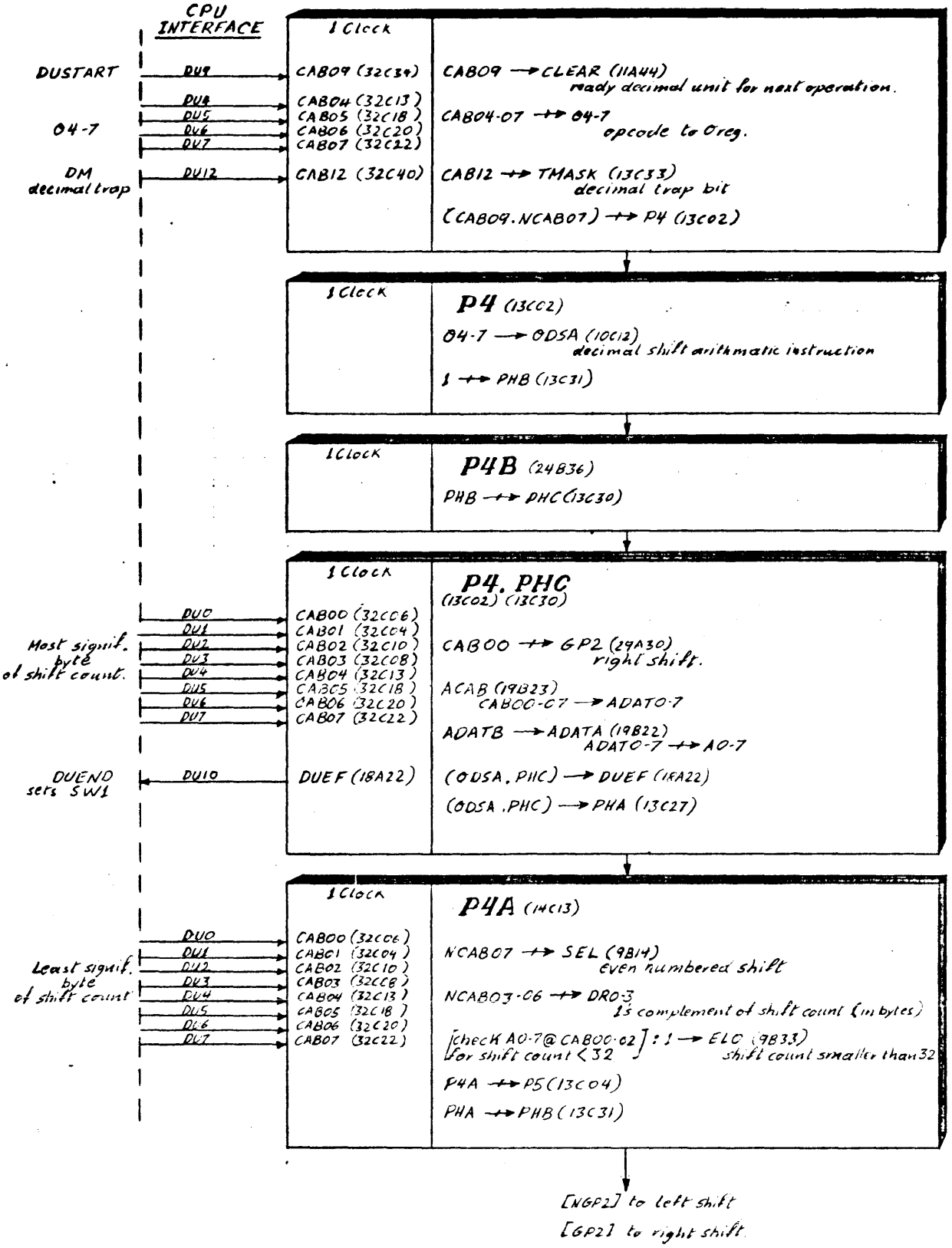
DIVIDE REENTRY AFTER INTERRUPT

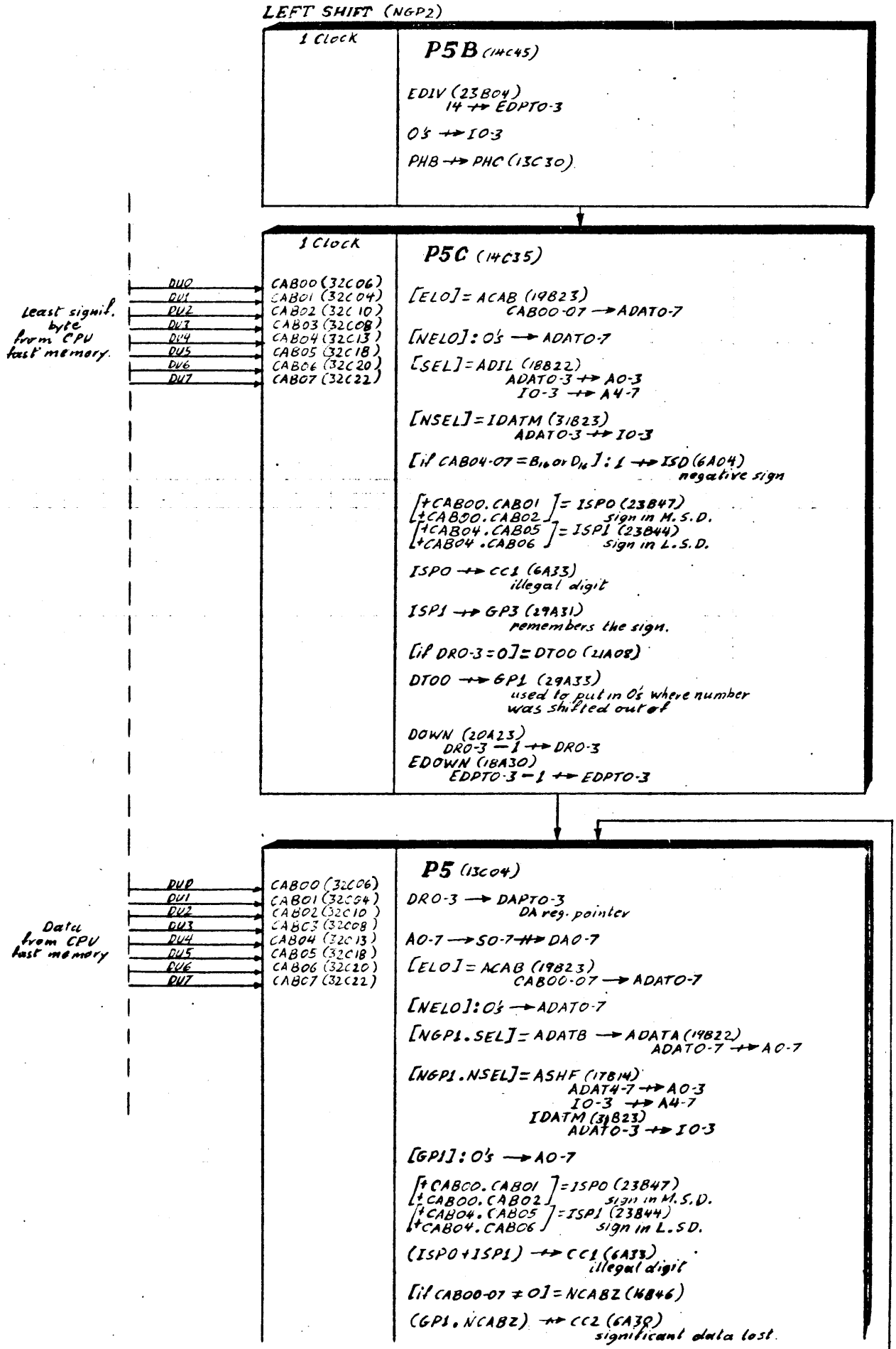
(differences only)

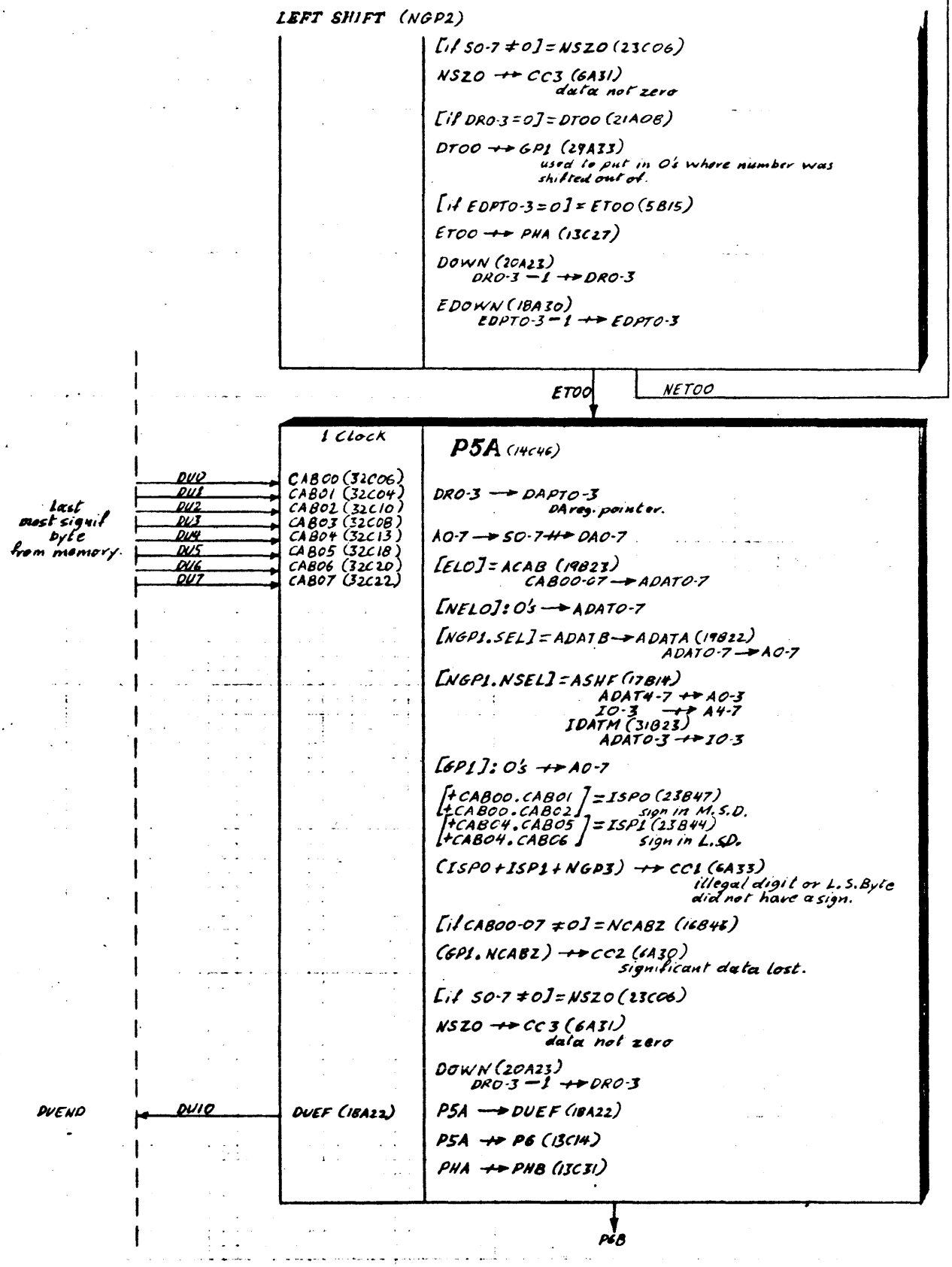
Same as regular divide untill P5C

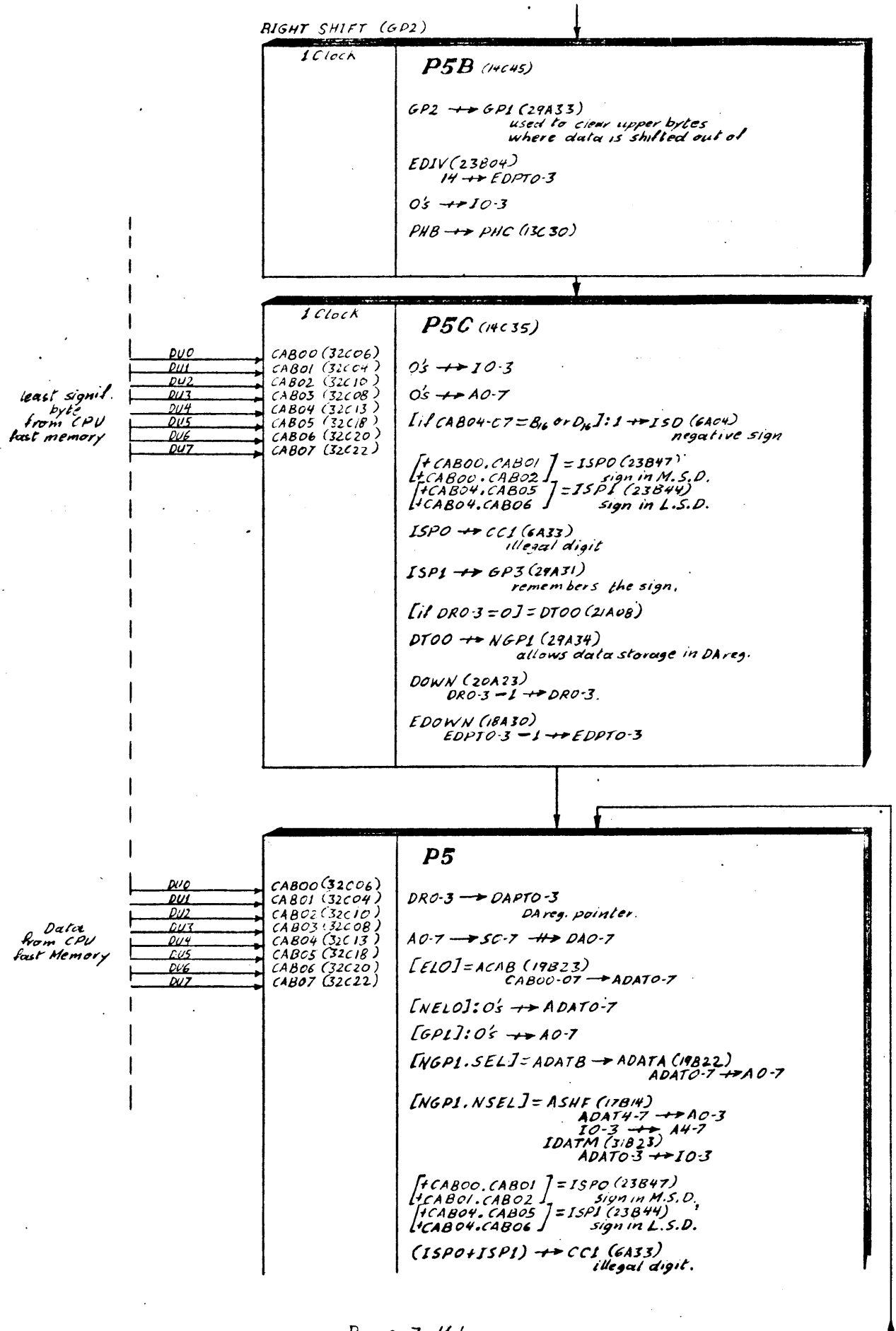


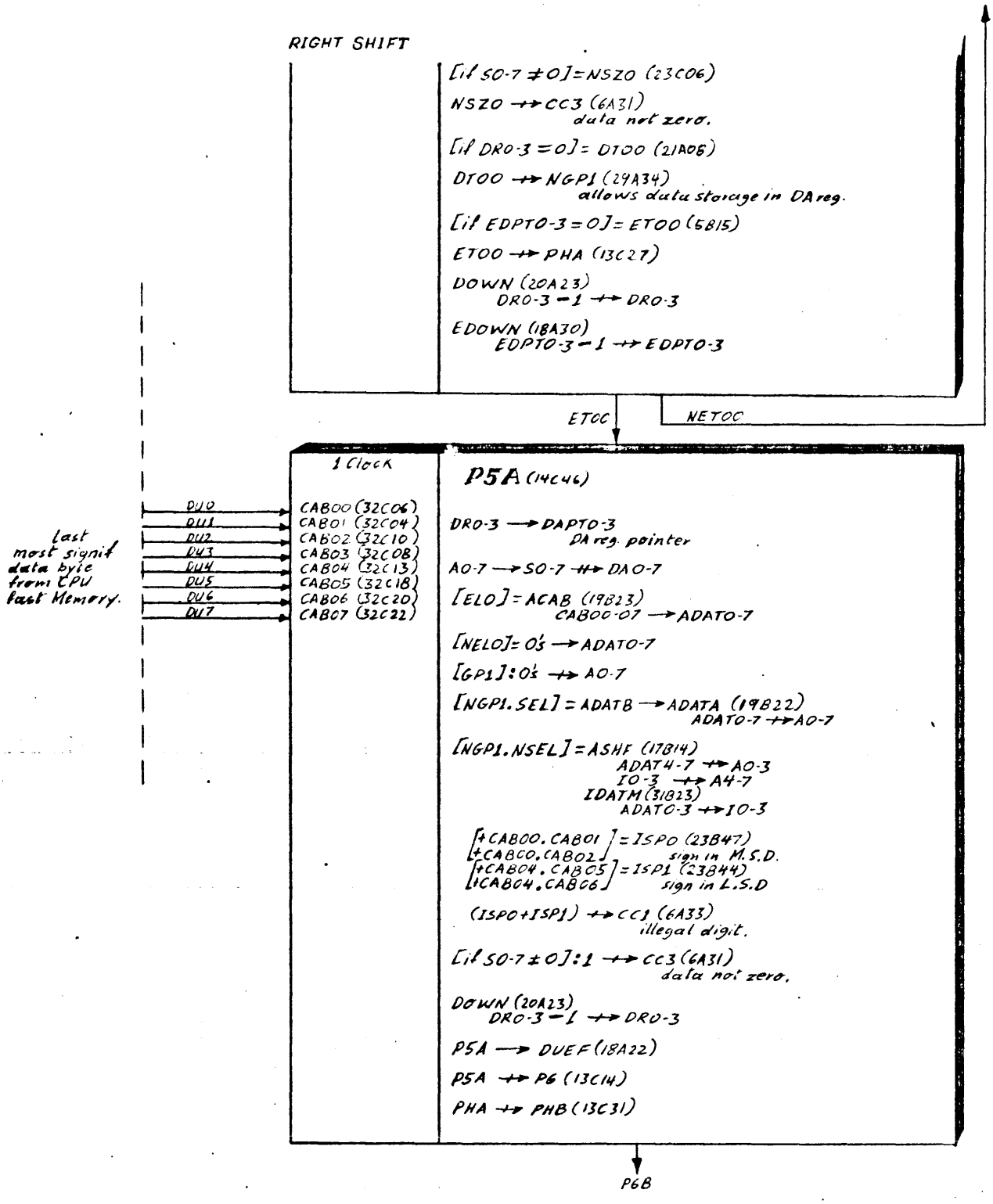
DECIMAL SHIFT ARITHMETIC (7C)




LEFT SHIFT (NGP2)
1 Clock
P5B (14C45)
EDIV (23B04)
14 → EDPTO-3
0's → IO-3
PHB → PHC (13C30)
1 Clock
P5C (14C35)
least signif. byte from CPU fast memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
[ELO] = ACAB (19B23)
CAB00-07 → ADAT0-7
[NELO]: 0's → ADAT0-7
[SEL] = ADIL (18B22)
ADAT0-3 → A0-3
IO-3 → A4-7
[NSEL] = IDATM (31B23)
ADAT0-3 → IO-3
[if CAB04-07 = B16 or D16]: 1 → ISD (6A04)
negative sign
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47)
sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44)
sign in L.S.D.
ISP0 → CC1 (6A33)
illegal digit
ISP1 → GP3 (29A31)
remembers the sign.
[if DR0-3 = 0] = DT00 (21A08)
DT00 → GP1 (29A33)
used to put in 0's where number was shifted out of
DOWN (20A23)
DR0-3 − 1 → DR0-3
EDOWN (18A30)
EDPT0-3 − 1 → EDPT0-3
Data from CPU fast memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
P5 (13C04)
DR0-3 → DAPT0-3
DA reg. pointer
A0-7 → S0-7 → DA0-7
[ELO] = ACAB (19B23)
CAB00-07 → ADAT0-7
[NELO]: 0's → ADAT0-7
[NGP1.SEL] = ADATB → ADATA (19B22)
ADAT0-7 → A0-7
[NGP1.NSEL] = ASHF (17B14)
ADAT4-7 → A0-3
IO-3 → A4-7
IDATM (31B23)
ADAT0-3 → IO-3
[GP1]: 0's → A0-7
[+CAB00.CAB01 / +CAB00.CAB02] = ISP0 (23B47)
sign in M.S.D.
[+CAB04.CAB05 / +CAB04.CAB06] = ISP1 (23B44)
sign in L.S.D.
(ISP0 + ISP1) → CC1 (6A33)
illegal digit
[if CAB00-07 ≠ 0] = NCAB2 (16B46)
(GP1. NCAB2) → CC2 (6A30)
significant data lost.


LEFT SHIFT (NGP2)
[if SO-7 ≠ 0] = NSZO (23C06)
NSZO → CC3 (6A31)
data not zero
[if DRO-3 = 0] = DTOO (21A08)
DTOO → GP1 (29A33)
used to put in 0's where number was shifted out of.
[if EDPTO-3 = 0] = ETOO (5B15)
ETOO → PHA (13C27)
DOWN (20A23)
DRO-3 − 1 → DRO-3
EDOWN (1BA30)
EDPTO-3 − 1 → EDPTO-3
ETOO
NETOO
1 Clock
P5A (14C46)
last most signif byte from memory.
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
DRO-3 → DAPTO-3
DA reg. pointer.
AO-7 → SO-7 → DAO-7
[ELO] = ACAB (19B23)
CAB00-07 → ADATO-7
[NELO]: 0's → ADATO-7
[NGP1.SEL] = ADA1B → ADATA (19B22)
ADATO-7 → AO-7
[NGP1.NSEL] = ASHF (17B14)
ADAT4-7 → AO-3
IO-3 → A4-7
IDATM (31B23)
ADATO-3 → IO-3
[GP1]: 0's → AO-7
[+CAB00.CAB01] = ISP0 (23B47)
[+CAB00.CAB02] sign in M.S.D.
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB06] sign in L.S.D.
(ISP0 + ISP1 + NGP3) → CC1 (6A33)
illegal digit or L.S.Byte did not have a sign.
[if CAB00-07 ≠ 0] = NCAB2 (16B46)
(GP1.NCAB2) → CC2 (6A30)
significant data lost.
[if SO-7 ≠ 0] = NSZO (23C06)
NSZO → CC3 (6A31)
data not zero
DOWN (20A23)
DRO-3 − 1 → DRO-3
DUEND
DU10
DUEF (1BA22)
P5A → DUEF (1BA22)
P5A → P6 (13C14)
PHA → PHB (13C31)
P6B


RIGHT SHIFT (GP2)
1 Clock
P5B (14C45)
GP2 → GP1 (29A33)
used to clear upper bytes where data is shifted out of
EDIV (23B04)
14 → EDPT0-3
0's → IO-3
PHB → PHC (13C30)
1 Clock
P5C (14C35)
least signif. byte from CPU fast memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
0's → IO-3
0's → A0-7
[if CAB04-C7 = B16 or D16]: 1 → ISO (6A04)
negative sign
[↑CAB00.CAB01 ↑CAB00.CAB02] = ISP0 (23B47)
sign in M.S.D.
[↑CAB04.CAB05 ↑CAB04.CAB06] = ISP1 (23B44)
sign in L.S.D.
ISP0 → CC1 (6A33)
illegal digit
ISP1 → GP3 (29A31)
remembers the sign.
[if DR0-3 = 0] = DT00 (21A08)
DT00 → NGP1 (29A34)
allows data storage in DA reg.
DOWN (20A23)
DR0-3 − 1 → DR0-3.
EDOWN (18A30)
EDPT0-3 − 1 → EDPT0-3
P5
Data from CPU fast Memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
DR0-3 → DAPT0-3
DA reg. pointer.
A0-7 → SC-7 ↔ DA0-7
[ELO] = ACAB (19B23)
CAB00-07 → ADAT0-7
[NELO]: 0's → ADAT0-7
[GP1]: 0's → A0-7
[NGP1.SEL] = ADATB → ADATA (19B22)
ADAT0-7 → A0-7
[NGP1.NSEL] = ASHF (17B14)
ADAT4-7 → A0-3
IO-3 → A4-7
IDATM (31B23)
ADAT0-3 → IO-3
[↑CAB00.CAB01 ↑CAB01.CAB02] = ISP0 (23B47)
sign in M.S.D.
[↑CAB04.CAB05 ↑CAB04.CAB06] = ISP1 (23B44)
sign in L.S.D.
(ISP0+ISP1) → CC1 (6A33)
illegal digit.


RIGHT SHIFT
[if SO-7 ≠ 0] = NSZO (23C06)
NSZO →→ CC3 (6A31)
data not zero.
[if DRO-3 = 0] = DTOO (21A06)
DTOO →→ NGP1 (29A34)
allows data storage in DA reg.
[if EDPTO-3 = 0] = ETOO (5B15)
ETOO →→ PHA (13C27)
DOWN (20A23)
DRO-3 − 1 →→ DRO-3
EDOWN (18A30)
EDPTO-3 − 1 →→ EDPTO-3
ETOC
NETOC
1 Clock
P5A (14C46)
last most signif data byte from CPU last Memory.
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
DRO-3 → DAPTO-3
DA reg. pointer
AO-7 → SO-7 →→ DAO-7
[ELO] = ACAB (19B23)
CAB00-07 → ADATO-7
[NELO] = 0's → ADATO-7
[GP1] : 0's →→ AO-7
[NGP1.SEL] = ADATB → ADATA (19B22)
ADATO-7 →→ AO-7
[NGP1.NSEL] = ASHF (17B14)
ADAT4-7 →→ AO-3
IO-3 →→ A4-7
IDATM (31B23)
ADATO-3 →→ IO-3
[+CAB00.CAB01] = ISPO (23B47)
[+CAB00.CAB02] sign in M.S.D.
[+CAB04.CAB05] = ISP1 (23B44)
[ICAB04.CAB06] sign in L.S.D
(ISPO+ISP1) →→ CC1 (6A33)
illegal digit.
[if SO-7 ≠ 0] : 1 →→ CC3 (6A31)
data not zero.
DOWN (20A23)
DRO-3 − 1 →→ DRO-3
P5A → DUEF (18A22)
P5A →→ P6 (13C14)
PHA →→ PHB (13C31)
P6B

DECIMAL SHIFT CONTINUED

1 Clock

P6B (14C36)

DRO-3 → ADPTO-3
DA reg. pointer.

AO-7 → SO-7 ↔ DAO-7

[if SO-7 ≠ 0] = NSZO (23C06)

NSZO ↔ CC3 (6A31)
data not zero

Right shift only: [if IO-3 ≠ 0] = NIZERO (25B46)
(GP2.NIZERO) ↔ CC3 (6A31)
data not zero.
IO-3 ↔ A4-7

CC1 ↔ NCC2 (6A29)

DOWN (20A23)
DRO-3 − 1 ↔ DRO-3

PHB ↔ PHC (13C30)

1 Clock

P6C (14C01)

Right shift only: [GP2]: DRO-3 → ADPTO-3
DA reg. pointer.
AO-7 → SO-7 ↔ DAO-7

ACC (23845)
CC1 ↔ AO (20B27)
CC2 ↔ A1 (20B31)
(CC3.NISD) ↔ A2 (20B19)
(CC3.ISD) ↔ A3 (20B23)
(CC1.TMASK) ↔ A4 (21B27)
(CC1.NTMASK) ↔ A5 (21B31)
NCC1 ↔ A6 (21B19)
NCC2 ↔ A7 (21B23)

[NISD]: C_{16} ↔ IO-3

[ISD]: D_{16} ↔ IO-3

DRPRE (18A23)
14 ↔ DRO-3

EDIV (23B04)
14 ↔ EDPTO-3

P6C → PHA (13C27)

1 Clock

P6. PHA
(13C14) (13C27)

AO-7 → SO-7

DOUT (23B03)
SO-7 → DUO-7

DUEF (18A22)

ADIL (18B22)
IO-3 ↔ A4-7
sign.

ADA (19B30)
DAC-7 → ADATO-7

ADATC → ADATA (19B22)
ADATO-3 ↔ AO-3

DOWN (20A23)
DRO-3 − 1 ↔ DRO-3

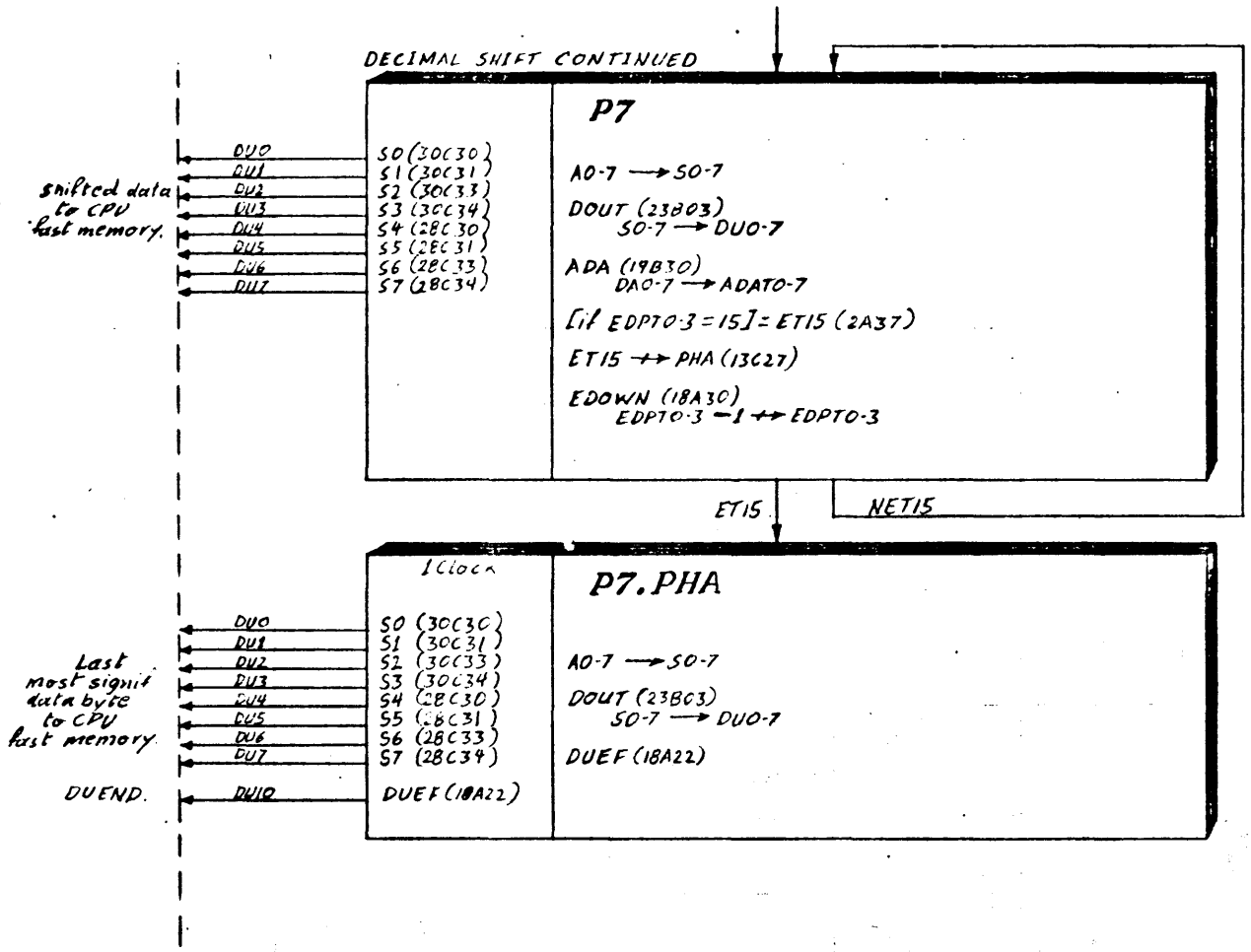
EDOWN (18A30)
EDPTO-3 − 1 ↔ EDPTO-3

(P6.PHA) ↔ P7 (13C06)

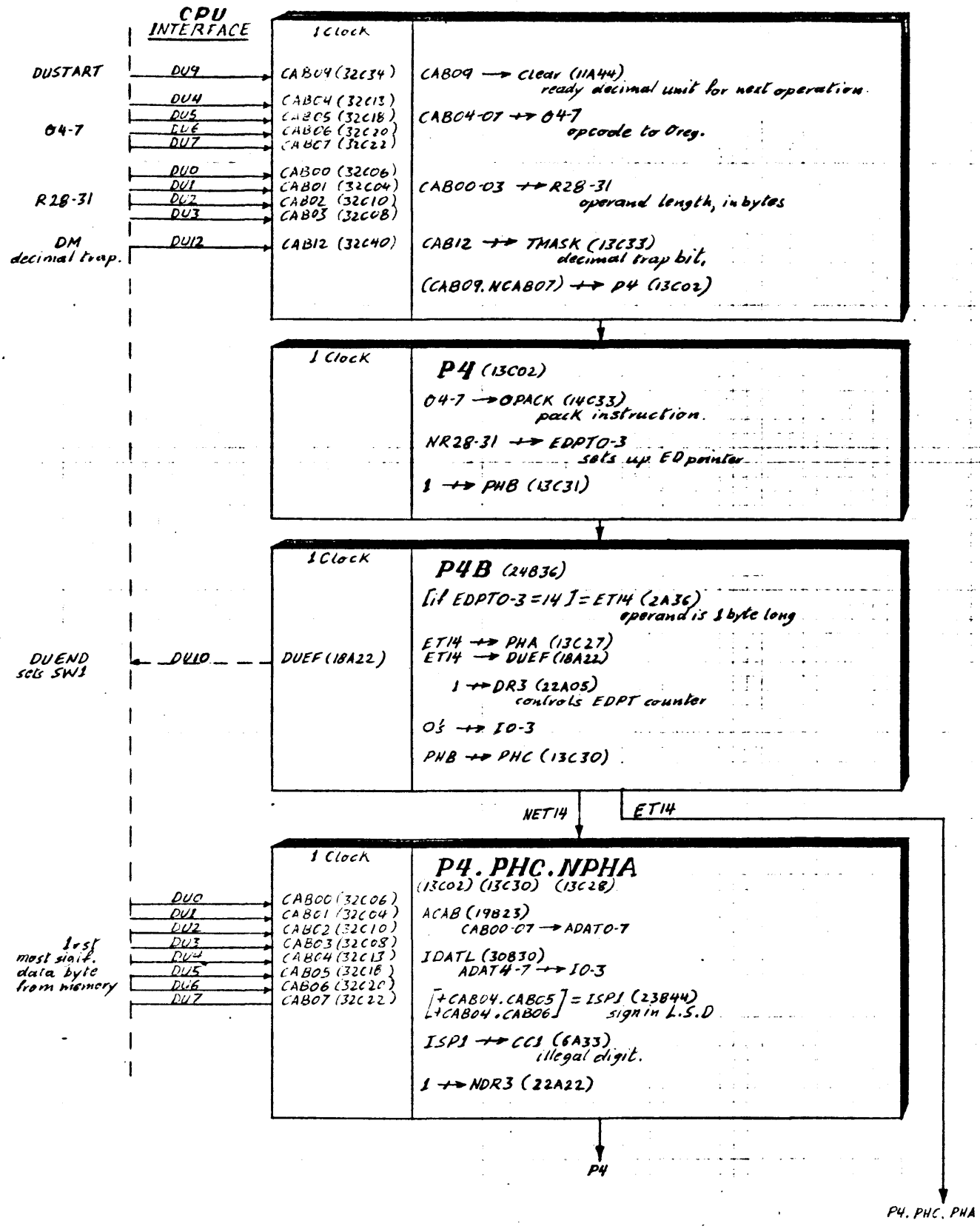
Condition code & abort info.

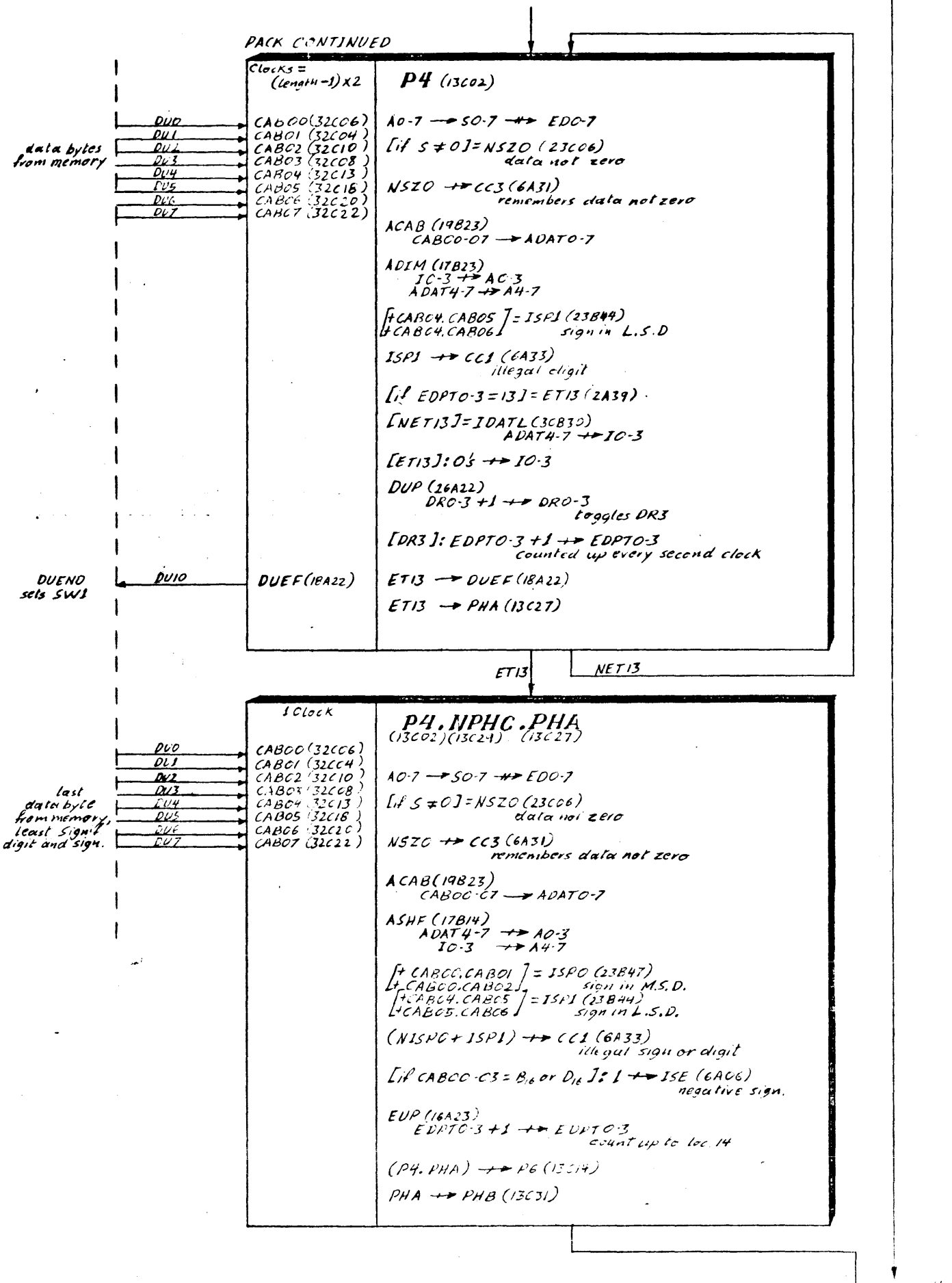
DUO ← SO (30C30)
DU1 ← S1 (30C31)
DU2 ← S2 (30C33)
DU3 ← S3 (30C34)
DU4 ← S4 (28C30)
DU5 ← S5 (28C31)
DU6 ← S6 (28C33)
DU7 ← S7 (28C34)

DUEND — DU10 ← DUEF (18A22)


DECIMAL SHIFT CONTINUED
P7
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
ADA (19B30)
DAO-7 → ADATO-7
[if EDPTO-3 = 15] = ET15 (2A37)
ET15 → PHA (13C27)
EDOWN (18A30)
EDPTO-3 −1 → EDPTO-3
ET15
NET15
1 Clock
P7.PHA
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
DUEF (18A22)
shifted data to CPU fast memory.
DUO
DU1
DU2
DU3
DU4
DU5
DU6
DU7
SO (30C30)
S1 (30C31)
S2 (30C33)
S3 (30C34)
S4 (28C30)
S5 (28C31)
S6 (28C33)
S7 (28C34)
Last most signif data byte to CPU fast memory.
DUEND.
DU10
DUEF (18A22)

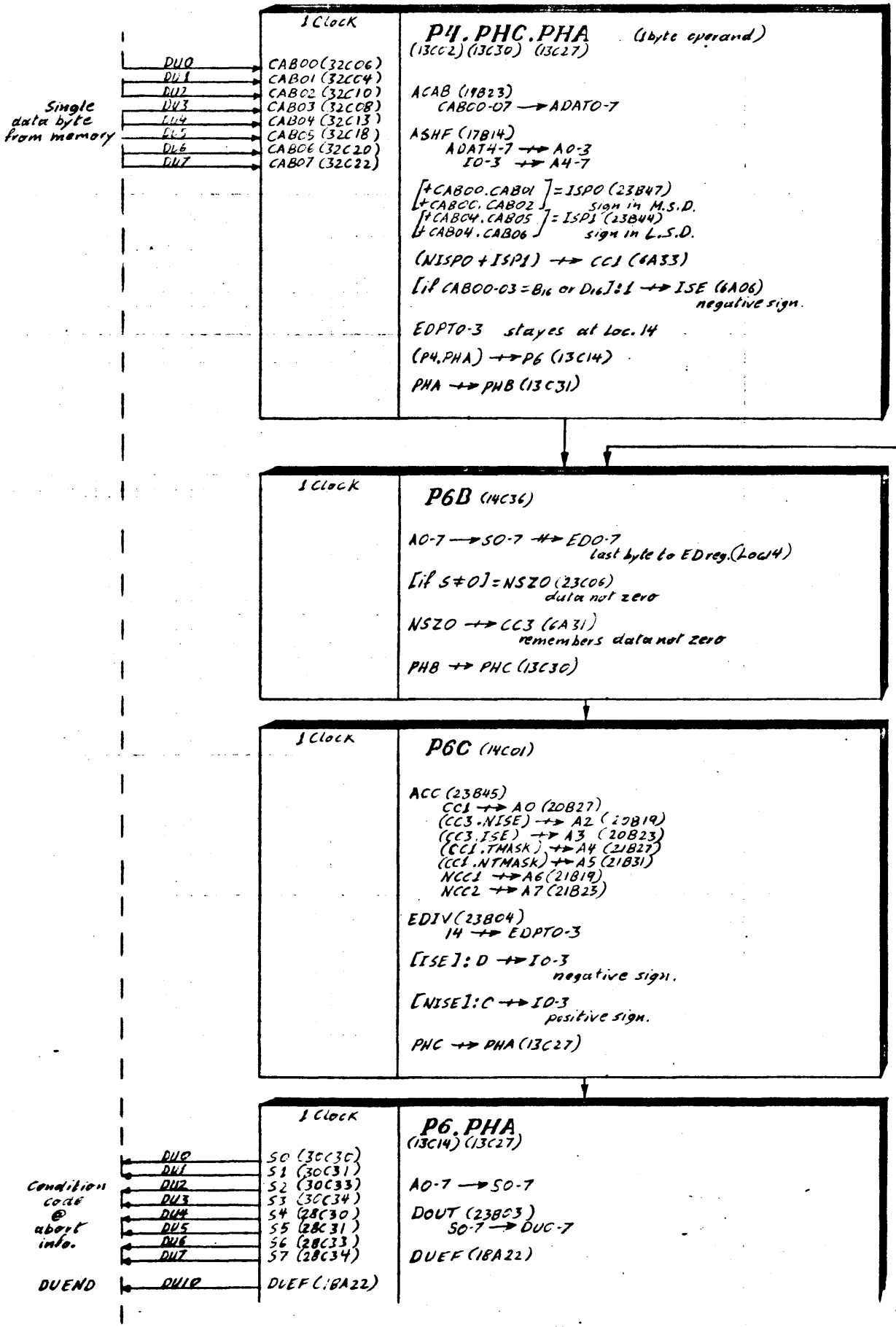
PACK DECIMAL DIGITS (76)





P4.PHC.PHA
TO P

PACK CONTINUED



PACK CONTINUED

ADIL (18B22)
B0-3 → A4-7
sign to Areg.

ESL (9A30)
EDO-7 → BO-7
L.S. byte of data.

[if EDPTO-3 = R2B-31] = EDMA (12A46)

EDMA → GP1 (29A33)
used to clear rest of decimal accumulator.

EDOWN (18A30)
EDPTO-3 − 1 → EDPTO-3

(P6.PHA) → P7 (13C06)

PHA → PHB (13C31)

1 clock

P7. PHB
(13C06) (13C31)

DUO	SO (30C30)	BO-3 → SO-3
DU1	S1 (30C31)	A4-7 → S4-7
DU2	S2 (30C33)	
DU3	S3 (30C34)	DOUT (23B03)
DU4	S4 (28C30)	SO-7 → DUO-7
DU5	S5 (28C31)	
DU6	S6 (28C33)	[NGP1] = ESL (9A30)
DU7	S7 (28C34)	EDO-7 → BO-7

1rst least sigif data byte to R15.

[GP1]: 0's → BO-7
to clear rest of decimal accumulator.

[if EDPTO-3 = NR2B-31] = EDMA (12A42)

EMMA → GP1 (29A33)
used to clear rest of decimal accumulator.

EDOWN (18A30)
EDPTO-3 − 1 → EDPTO-3

14 clocks

P7 (13C06)

DUO	SO (30C30)	BO-7 → SO-7
DU1	S1 (30C31)	
DU2	S2 (30C33)	DOUT (23B03)
DU3	S3 (30C34)	SO-7 → DUO-7
DU4	S4 (28C30)	
DU5	S5 (28C31)	[NGP1] = ESL (9A30)
DU6	S6 (28C33)	EDO-7 → BO-7
DU7	S7 (28C34)	

DATA or 0's to CPU fast Memory

[GP1]: 0's → BO-7
to clear decimal accumulator.

[if EDPTO-3 = NR2B-31] = EDMA (12A46)

EDMA → GP1 (29A33)
used to clear rest of decimal accumulator.

[if EDPTO-3 = 15] = ET15 (2A37)
M.S. byte in ED reg.

ET15 → PHA (13C27)

ET15

NET15

1 Clock

P7. PHA
(13C06) (13C27)

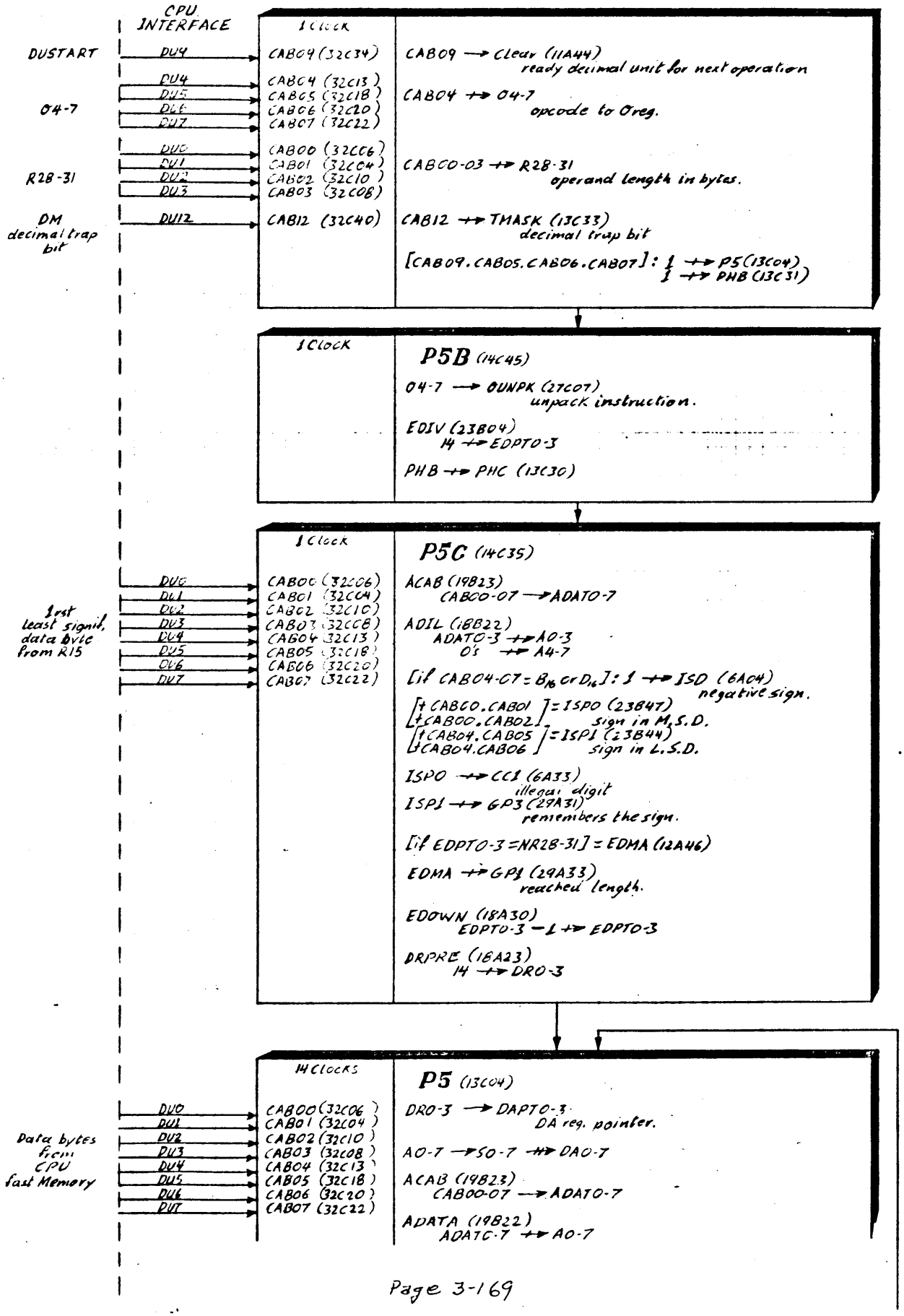
DUO	SO (30C30)	BO-7 → SO-7
DU1	S1 (30C31)	
DU2	S2 (30C33)	DOUT (23B03)
DU3	S3 (30C34)	SO-7 → DUO-7.
DU4	S4 (28C30)	last byte to CPU
DU5	S5 (28C31)	
DU6	S6 (28C33)	DUEF (18A22)
DU7	S7 (28C34)	sets SW1 in CPU

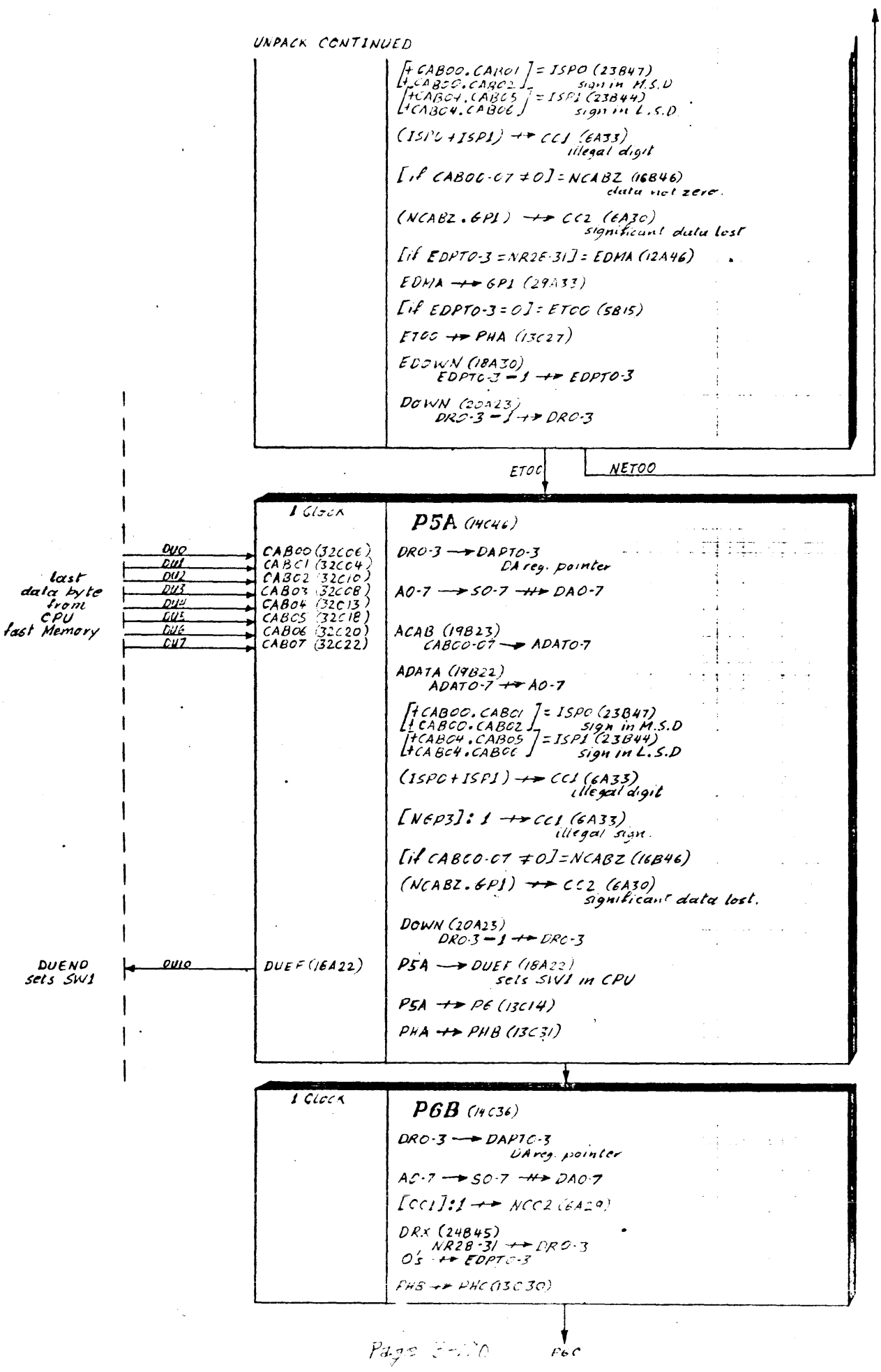
last data or 0's to CPU fast memory

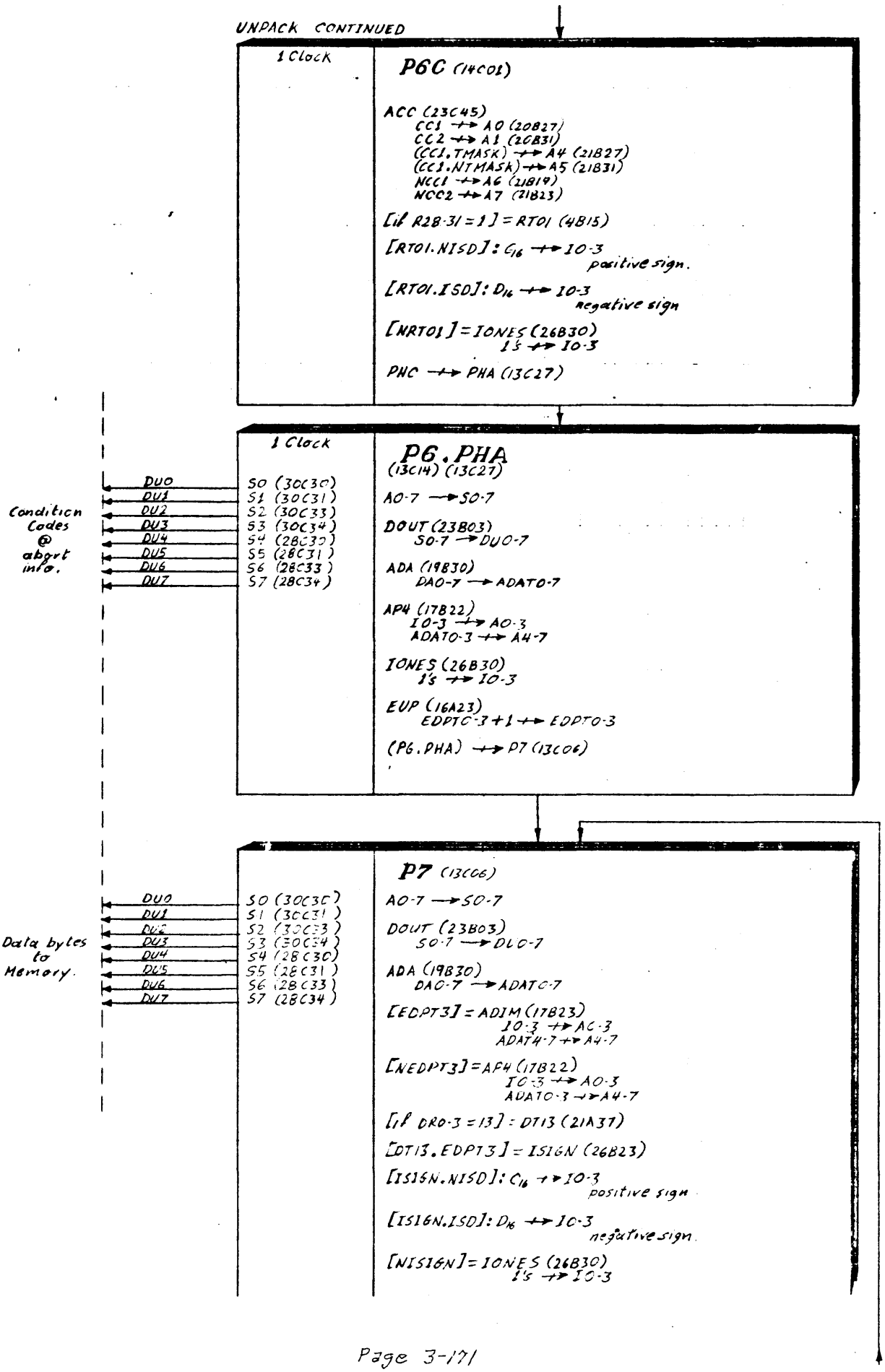
DUEND sets SW1

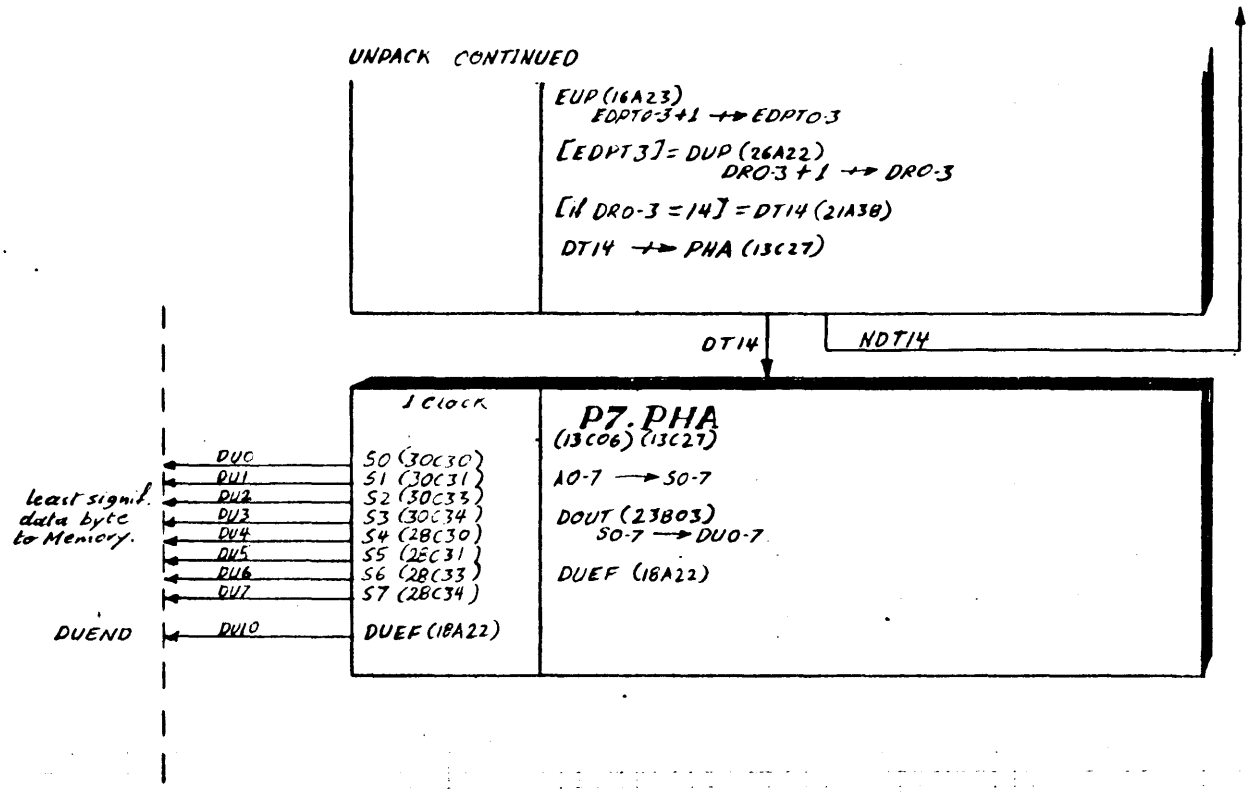
DIO — DUEF (18A22)

UNPACK DECIMAL DIGITS (77)

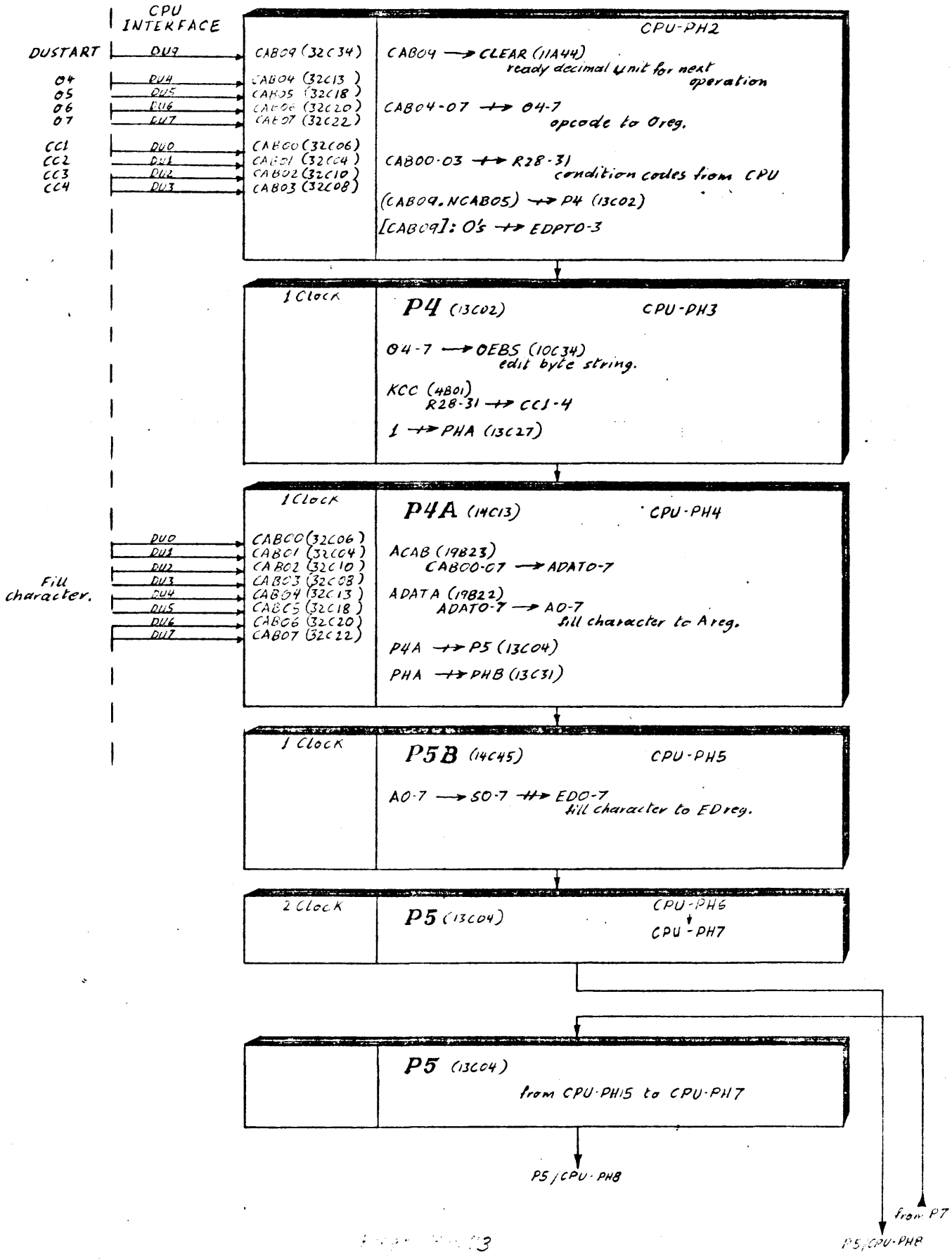


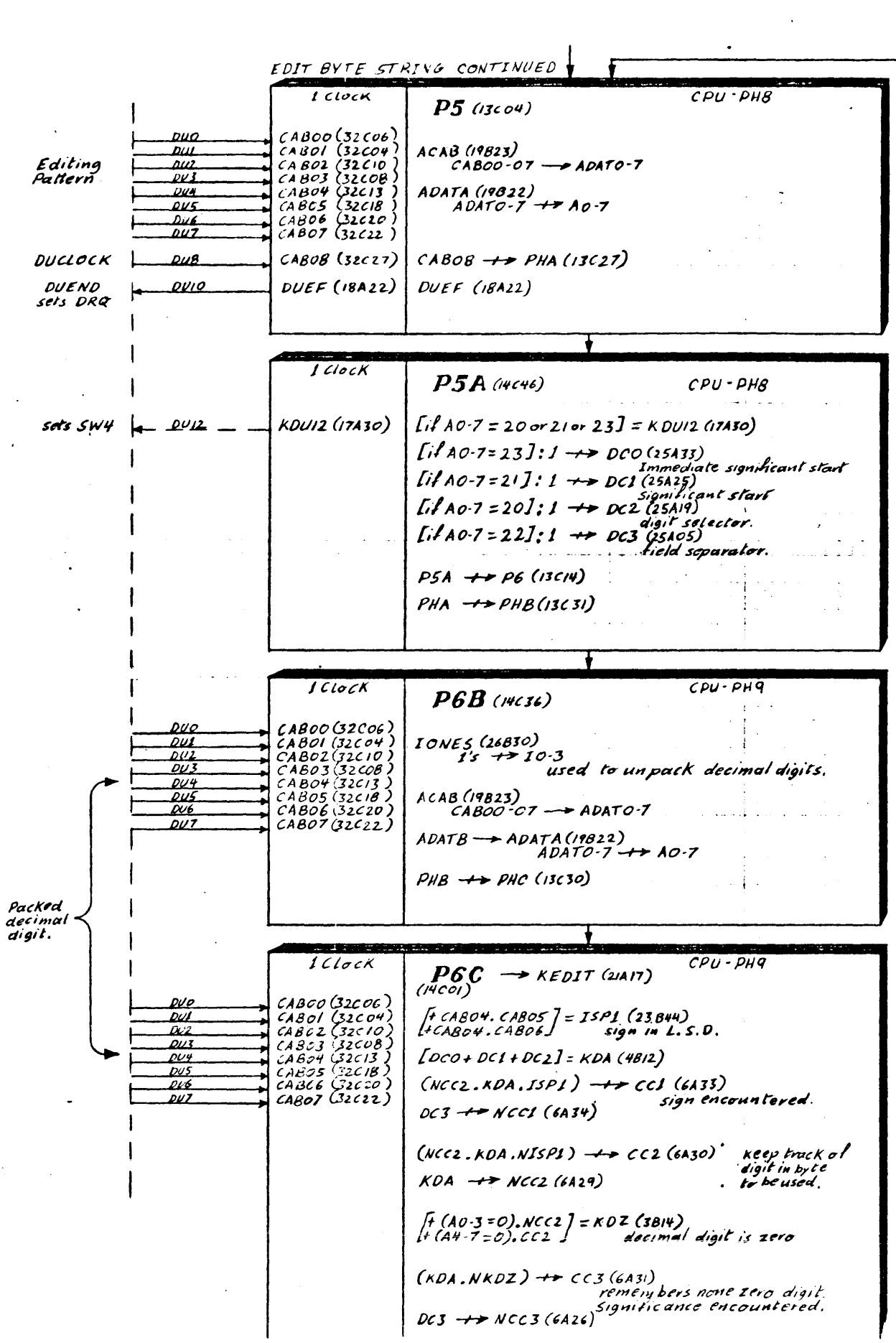

UNPACK CONTINUED
[+CAB00.CAB01] = ISP0 (23B47)
[+CAB00.CAB02] sign in M.S.D
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB06] sign in L.S.D
(ISP0 + ISP1) → CC1 (6A33)
illegal digit
[if CAB00-07 ≠ 0] = NCABZ (16B46)
data not zero.
(NCABZ.6P1) → CC2 (6A30)
significant data lost
[if EDPT0-3 = NR2E-31] = EDMA (12A46)
EDMA → GP1 (29A33)
[if EDPT0-3 = 0] = ETOO (5B15)
ETOO → PHA (13C27)
EDOWN (18A30)
EDPT0-3 − 1 → EDPT0-3
DOWN (20A23)
DR0-3 − 1 → DR0-3
ETOO
NETOO
1 Clock
P5A (14C46)
DR0-3 → DAPT0-3
DA reg. pointer
A0-7 → S0-7 → DA0-7
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 → A0-7
[+CAB00.CAB01] = ISP0 (23B47)
[+CAB00.CAB02] sign in M.S.D
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB06] sign in L.S.D
(ISP0 + ISP1) → CC1 (6A33)
illegal digit
[NGP3]: 1 → CC1 (6A33)
illegal sign.
[if CAB00-07 ≠ 0] = NCABZ (16B46)
(NCABZ.6P1) → CC2 (6A30)
significant data lost.
DOWN (20A23)
DR0-3 − 1 → DR0-3
P5A → DUEF (18A22)
sets SW1 in CPU
P5A → PE (13C14)
PHA → PHB (13C31)
last data byte from CPU fast Memory
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
DUEND sets SW1
DU10
DUEF (16A22)
1 Clock
P6B (14C36)
DR0-3 → DAPT0-3
DA reg. pointer
A0-7 → S0-7 → DA0-7
[CC1]: 1 → NCC2 (6A29)
DRX (24B45)
NR28-31 → DR0-3
0's → EDPT0-3
PHB → PHC (13C30)
P6C


UNPACK CONTINUED
1 Clock
P6C (14C01)
ACC (23C45)
CC1 → A0 (20B27)
CC2 → A1 (20B31)
(CC1.TMASK) → A4 (21B27)
(CC1.NTMASK) → A5 (21B31)
NCC1 → A6 (21B19)
NCC2 → A7 (21B23)
[if R28-31 = 1] = RT01 (4B15)
[RT01.NISD]: C16 → IO-3
positive sign.
[RT01.ISD]: D16 → IO-3
negative sign
[NRT01] = IONES (26B30)
1's → IO-3
PHC → PHA (13C27)
1 Clock
P6.PHA
(13C14) (13C27)
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
ADA (19B30)
DAO-7 → ADATO-7
APH (17B22)
IO-3 → AO-3
ADATO-3 → A4-7
IONES (26B30)
1's → IO-3
EUP (16A23)
EDPTO-3 + 1 → EDPTO-3
(P6.PHA) → P7 (13C06)
Condition Codes @ abort info.
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
S0 (30C30)
S1 (30C31)
S2 (30C33)
S3 (30C34)
S4 (28C30)
S5 (28C31)
S6 (28C33)
S7 (28C34)
P7 (13C06)
AO-7 → SO-7
DOUT (23B03)
SO-7 → DUO-7
ADA (19B30)
DAO-7 → ADATO-7
[EDPT3] = ADIM (17B23)
IO-3 → AC-3
ADAT4-7 → A4-7
[NEDPT3] = APH (17B22)
IO-3 → AO-3
ADATO-3 → A4-7
[if DRO-3 = 13] = DT13 (21A37)
[DT13.EDPT3] = ISIGN (26B23)
[ISIGN.NISD]: C16 → IO-3
positive sign
[ISIGN.ISD]: D16 → IO-3
negative sign.
[NISIGN] = IONES (26B30)
1's → IO-3
Data bytes to Memory.
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
S0 (30C30)
S1 (30C31)
S2 (30C33)
S3 (30C34)
S4 (28C30)
S5 (28C31)
S6 (28C33)
S7 (28C34)

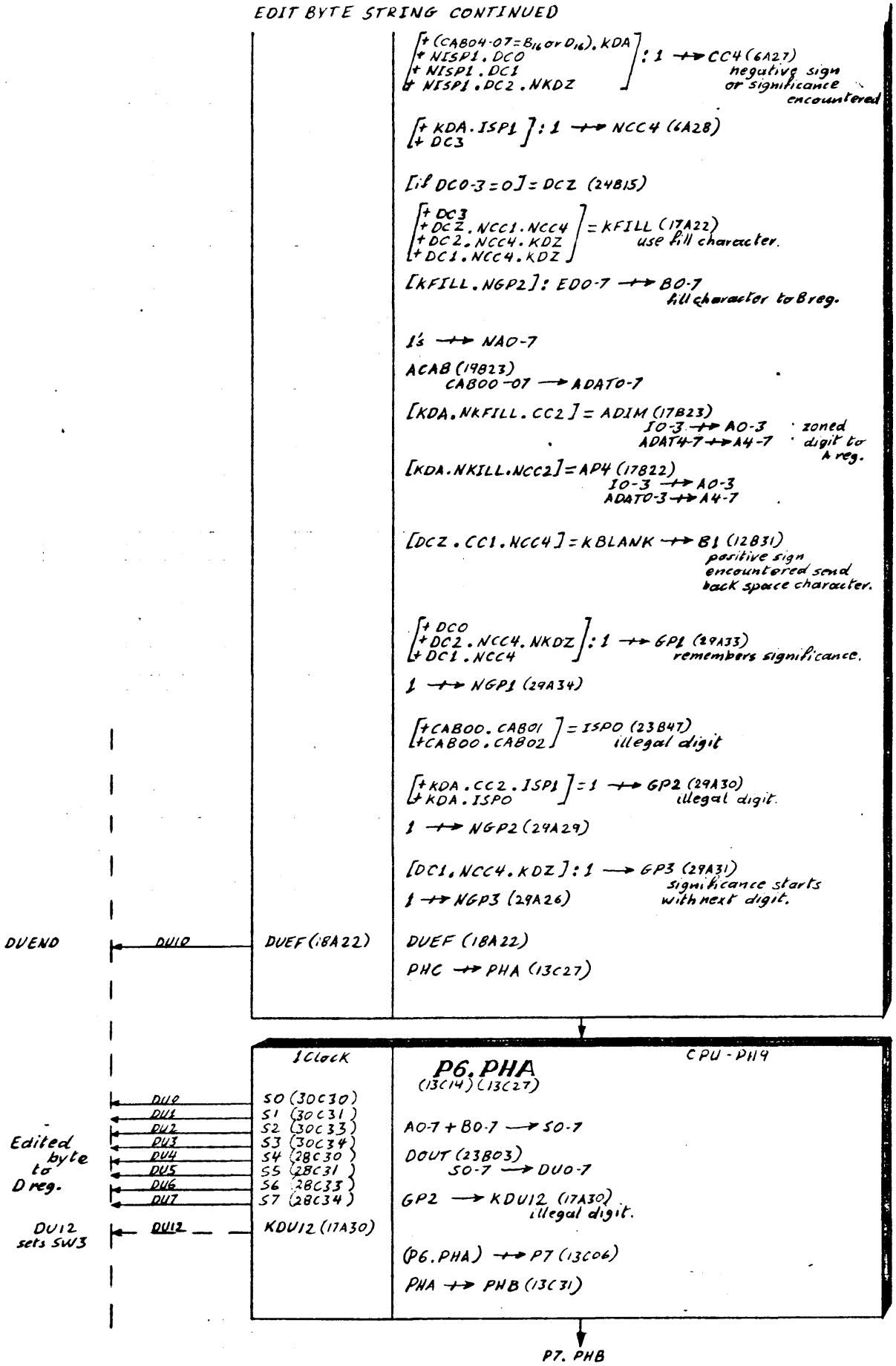

UNPACK CONTINUED
EUP (16A23)
EDPTO-3+1 → EDPTO-3
[EDPT3] = DUP (26A22)
DRO-3 + 1 → DRO-3
[If DRO-3 = 14] = DT14 (21A38)
DT14 → PHA (13C27)
DT14
NDT14
1 CLOCK
P7. PHA
(13C06) (13C27)
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
least signif. data byte to Memory.
S0 (30C30)
S1 (30C31)
S2 (30C33)
S3 (30C34)
S4 (28C30)
S5 (28C31)
S6 (28C33)
S7 (28C34)
A0-7 → S0-7
DOUT (23B03)
S0-7 → DU0-7
DUEF (18A22)
DUEND
DU10
DUEF (18A22)

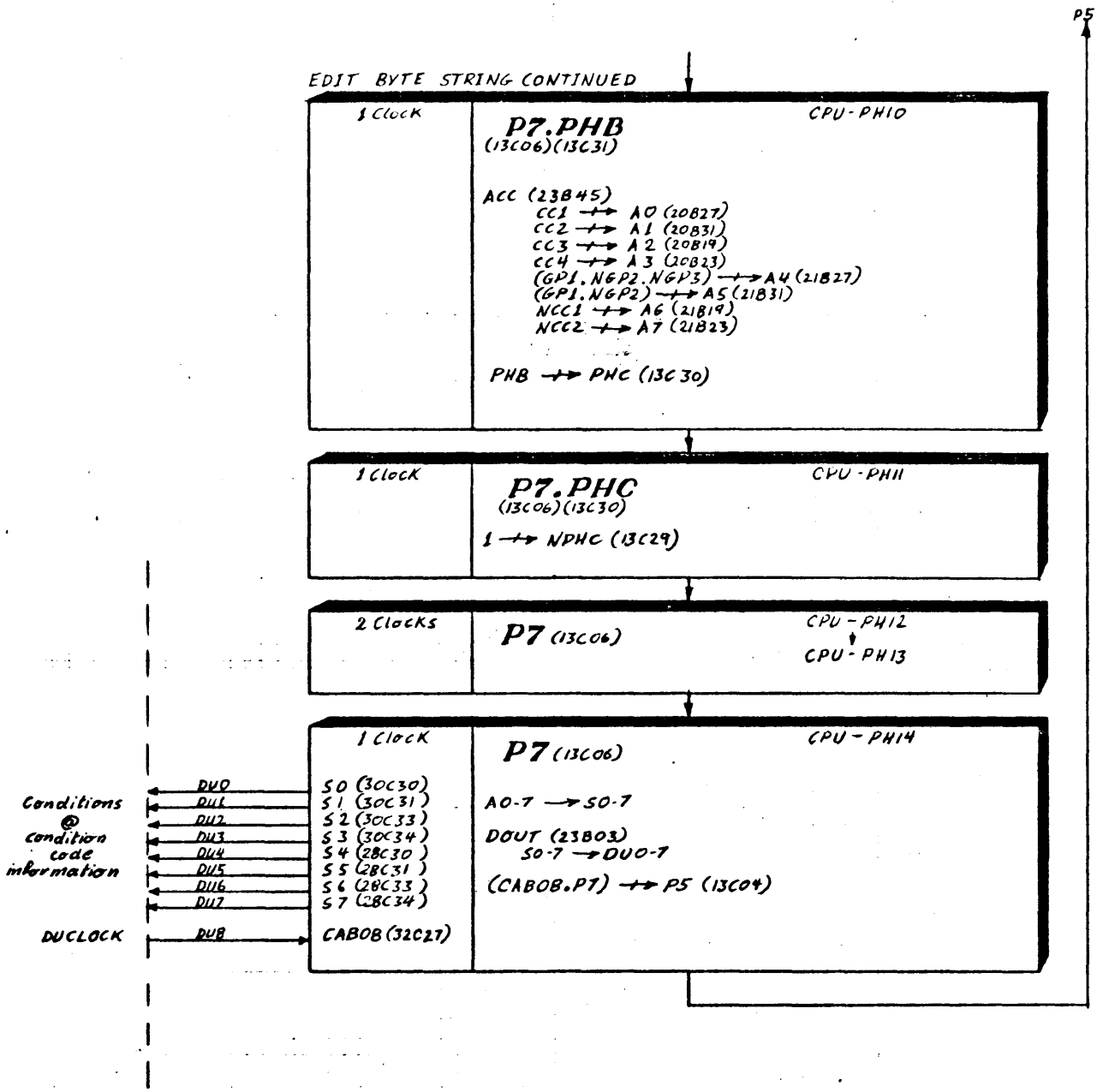
EDIT BYTE STRING (63)




EDIT BYTE STRING CONTINUED
1 clock
CPU - PH8
P5 (13C04)
Editing Pattern
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
CAB00 (32C06)
CAB01 (32C04)
CAB02 (32C10)
CAB03 (32C08)
CAB04 (32C13)
CAB05 (32C18)
CAB06 (32C20)
CAB07 (32C22)
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATA (19B22)
ADAT0-7 ↔ A0-7
DUCLOCK
DU8
CAB08 (32C27)
CAB08 ↔ PHA (13C27)
DUEND sets DRQ
DU10
DUEF (18A22)
DUEF (18A22)
1 clock
P5A (14C46)
CPU - PH8
sets SW4
DU12
KDU12 (17A30)
[if A0-7 = 20 or 21 or 23] = KDU12 (17A30)
[if A0-7 = 23]: 1 ↔ DC0 (25A33)
Immediate significant start
[if A0-7 = 21]: 1 ↔ DC1 (25A25)
significant start
[if A0-7 = 20]: 1 ↔ DC2 (25A19)
digit selector.
[if A0-7 = 22]: 1 ↔ DC3 (25A05)
field separator.
P5A ↔ P6 (13C14)
PHA ↔ PHB (13C31)
1 Clock
CPU - PH9
P6B (14C36)
Packed decimal digit.
IONES (26B30)
1's ↔ I0-3
used to unpack decimal digits.
ACAB (19B23)
CAB00-07 → ADAT0-7
ADATB → ADATA (19B22)
ADAT0-7 ↔ A0-7
PHB ↔ PHC (13C30)
1 Clock
CPU - PH9
P6C → KEDIT (21A17)
(14C01)
[+CAB04.CAB05] = ISP1 (23B44)
[+CAB04.CAB06]
sign in L.S.D.
[DC0 + DC1 + DC2] = KDA (4B12)
(NCC2.KDA.ISP1) ↔ CC1 (6A33)
sign encountered.
DC3 ↔ NCC1 (6A34)
(NCC2.KDA.NISP1) ↔ CC2 (6A30)
keep track of digit in byte to be used.
KDA ↔ NCC2 (6A29)
[+(A0-3=0).NCC2] = KDZ (3B14)
[+(A4-7=0).CC2]
decimal digit is zero
(KDA.NKDZ) ↔ CC3 (6A31)
remembers none zero digit
Significance encountered.
DC3 ↔ NCC3 (6A26)

EDIT BYTE STRING CONTINUED




P5
EDIT BYTE STRING CONTINUED
1 Clock
CPU-PH10
P7.PHB
(13C06)(13C31)
ACC (23B45)
CC1 → A0 (20B27)
CC2 → A1 (20B31)
CC3 → A2 (20B19)
CC4 → A3 (20B23)
(GP1.NGP2.NGP3) → A4 (21B27)
(GP1.NGP2) → A5 (21B31)
NCC1 → A6 (21B19)
NCC2 → A7 (21B23)
PHB → PHC (13C30)
1 Clock
CPU-PH11
P7.PHC
(13C06)(13C30)
1 → NPHC (13C29)
2 Clocks
P7 (13C06)
CPU-PH12
CPU-PH13
1 Clock
CPU-PH14
P7 (13C06)
A0-7 → S0-7
DOUT (23B03)
S0-7 → DU0-7
(CA80B.P7) → P5 (13C04)
Conditions @ condition code information
DU0
DU1
DU2
DU3
DU4
DU5
DU6
DU7
DUCLOCK
DU8
S0 (30C30)
S1 (30C31)
S2 (30C33)
S3 (30C34)
S4 (28C30)
S5 (28C31)
S6 (28C33)
S7 (28C34)
CA80B (32C27)

MODULE CATION CHART (SIOP)

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	DT14	HT15	BT22	FT24	IT26	LT13	XT10	BT10	XT10	AT24	FT37	IT13	BT16	FT38	FT38	FT38	FT38	AT16 ABS	BT10 BS	LT20 BS	IT16 BS	AT11 BS	IT25	LT21	XT10	XT10	LT13	LT13	FT37	BT18	FT15	IT15
B	AT16	IT25	IT24	BT22	IT25	LT21	FT26	BT16	IT16	FT39	FT39	FT27	FT39	FT26	FT39	XT10	LT13	IT16	IT15	IT11	IT11	IT11	BT18	FT37	XT10	XT10	IT15	FT37	IT16	FT37	LT13	IT21
C	FT18	FT18	LT13	FT27	XT10		IT15	IT25	BT25	XT10	FT26	BT10	BT25	IT16	IT25	FT26	BT10	BT10	LT21	BT15	FT26	BT18	IT18	LT13	XT10		LT29	DT14	HT15	BT16		BT23
D	BT11	FT15	FT18	FT18	FT18		FT38	FT38	FT38	FT38	FT26	FT38	AT11	FT38	AT11	FT26	FT38	AT11	FT38	AT11	FT26	AT12	FT37	FT37	LT21	BT22	XT10	DT11	HT15	BT15	AT25	BT23
E	GT11	FT18	FT18	BT11	FT12	FT18	FT18	FT18	FT18	XT10	FT38	AT11	FT37	AT11	FT37	AT11	BT16	XT10	AT10	BT18	BT25	AT12	LT21	AT11	LT21	XT10		FT24	FT37	LT20	BT10	LT2
F		BT18	BT22	BT16	XT10	BT11	BT15	FT18	FT18	GT11	BT22	BT10	FT22	BT24	IT16	LT65	IT15	IT25	BT18	IT16	IT25	BT16	AT13	LT64	LT26	XT10	IT16	IT25	IT11	FT66		

SIOP

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A		AT56	DT26	AT60	LT89	AT57	LT90	AT83		LT94	LT95	LT26	BT16	AT60	LT71	AT60	FT82	AT11	FT79	AT11	FT79	AT11	FT79	FT79	IT31	BT12	BT31	BT31	BT10	FT66	FT66	FT43

MS

SIOP SWITCHES (LT26 Loc. 8F)

ADDRESS

S1-1 = Bit 21 = IOPA0
S2-1 = Bit 22 = IOPA1
S3-1 = Bit 23 = IOPA2

AIOP = S1-2 up

Buss Shared = S2-2 up

LASTONE = S4-1 up.

MS SWITCHES

ADDRESS (LT26 Loc. 21A)

S1-1 = Bit 26 → A10
S2-1 = Bit 25 → A09
S3-1 = Bit 24 → A08
S4-1 = Bit 23 → A07
S1-2 = Bit 22 → A06
S2-2 = Bit 21 → A05
S3-2 = Bit 20 → A04
S4-2 = Bit 19 → A03

ON/OFF LINE (LT94 Loc. 23A)

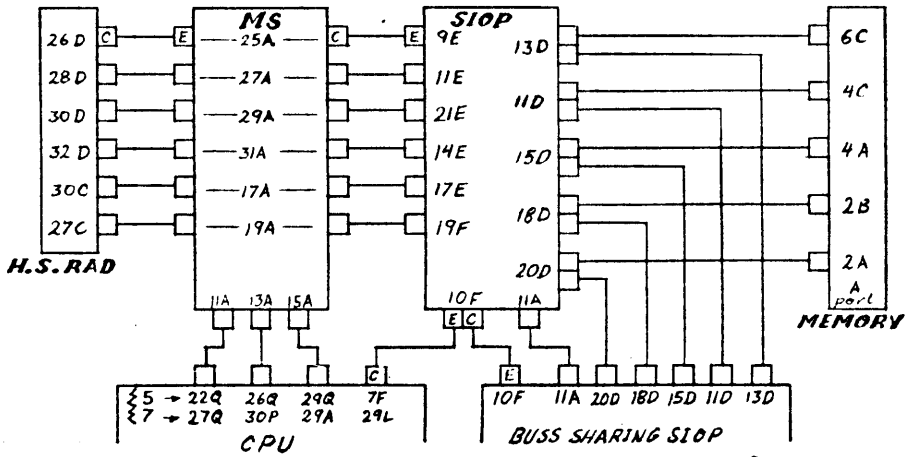
S1 up = On Line
S1 down = Off Line

Note: S1 Loc. 22A must be up.

OPTION

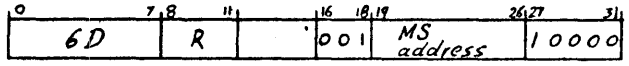
BS = Buss Sharing.

ABS = Buss Sharing AIOP only.

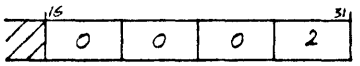


Single Phasing The SIOP

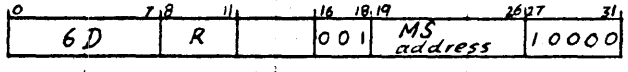
Set SIOP to single phase mode



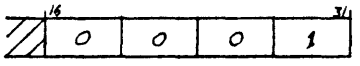
where R =



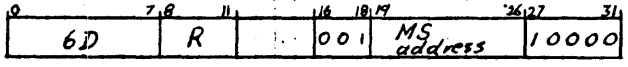
Run TI delay line once



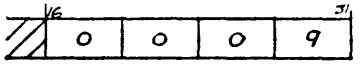
where R =



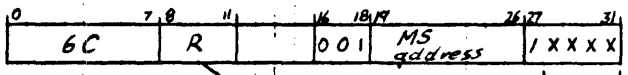
Run TM delay line twice (1 TM phase)



Where R =



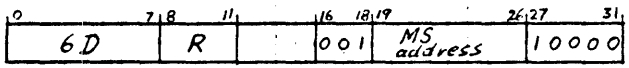
Read SIOP signals



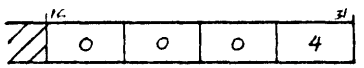
Group $I_{16} \rightarrow A_{16}$

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Group 1	FIO1A	FIO1B	FM01A	FM01B	FM11A	FM11B	FM12A	FM12B	FM13A	FM13B	FM14A	FM14B	LAST	MATCH	ZBC1	ZBC2
Group 2	FI11A	FI11B	FI12A	FI12B	FI13A	FI13B	FM21A	FM21B	FM22A	FM22B	FM24A	FM24B	ENDFI	NSERVICE1	CRD	CUT
Group 3	FM31A	FM31B	FM32A	FM32B	FM33A	FM33B	FM34A	FM34B	FM41A	FM41B	MWA	MWB	MWC	MWD		S31
Group 4	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30
Group 5	BC00	BC01	BC02	BC03	BC04	BC05	BC06	BC07	BC08	BC09	BC10	BC11	BC12	BC13	BC14	BC15
Group 6	CNSTR	PRI	FS	FSL	AVO	RS	RSA	SC	IC	IR	FNCF	MPE	MPR	MRQ	MRQ1	MRQ2
Group 7	STIL	STIDE	STTME	STMAE	STIOPME	STIOPCE	STIOPH	STIOPB1	STCE1	STLCI	STZBCI	END1	END2	END3	ENDDIO	FLCLEAR
Group 8	RK0	RK1	RK2	RK3	IA1	IA2	IA3	OA1	OA2	OA3	LR1	LR2	LR3	SWRITE	SREAD	DREAD
Group 9	RAB	RBB	RCB	RDB	KAA	KAB	KAC	KAD	SAA	SAB	SAC	SAD	KAB	KBB	KCB	KDB
Group A	WBA	WBB	WBC	WBD	JAB	JBB	JCB	JDB	ANOTHER			AIOP	PRQA	PRQB	MEMCYCA/1	MEMCYCB/1
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

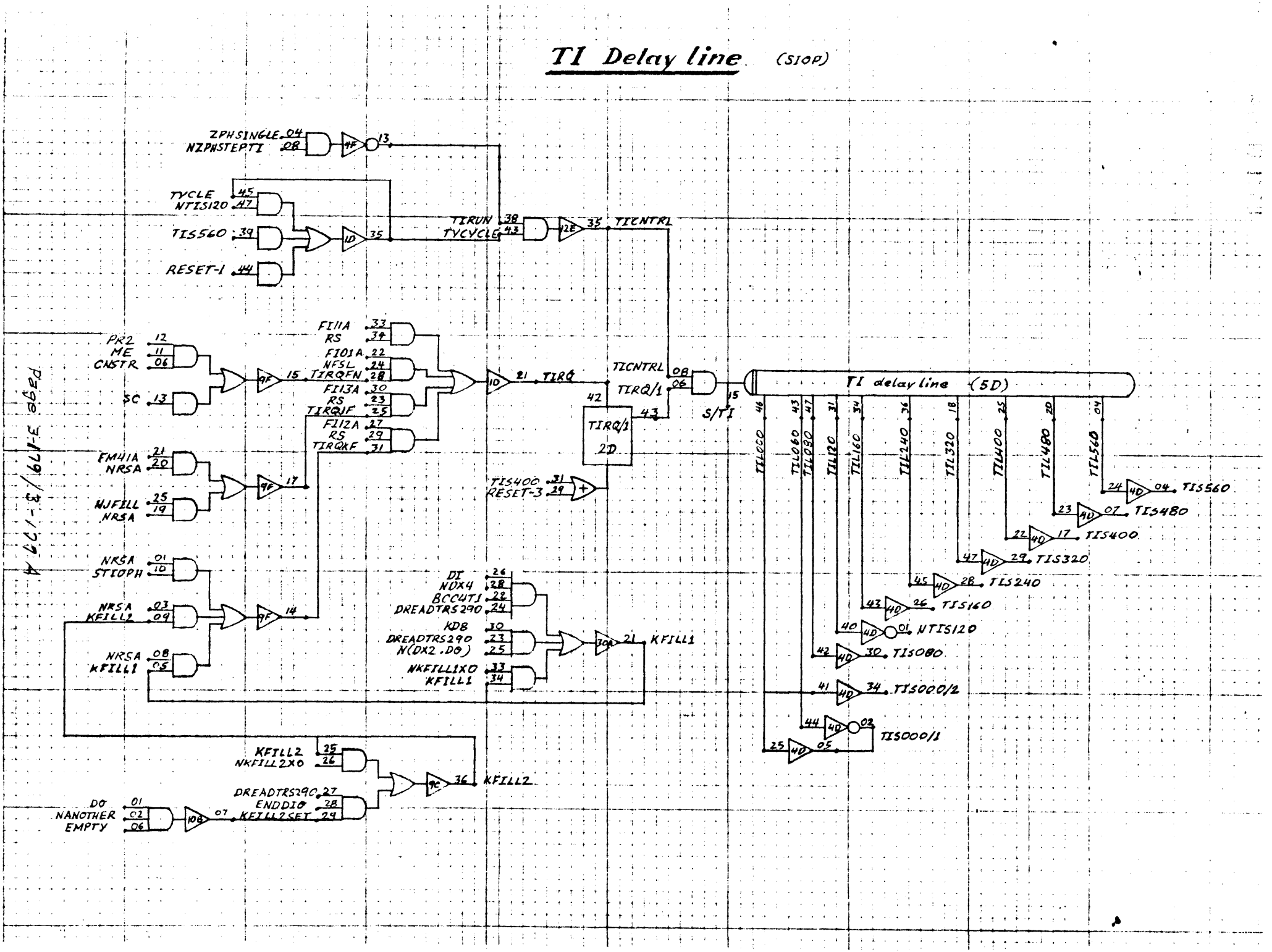
Return SIOP to normal mode (RESET)



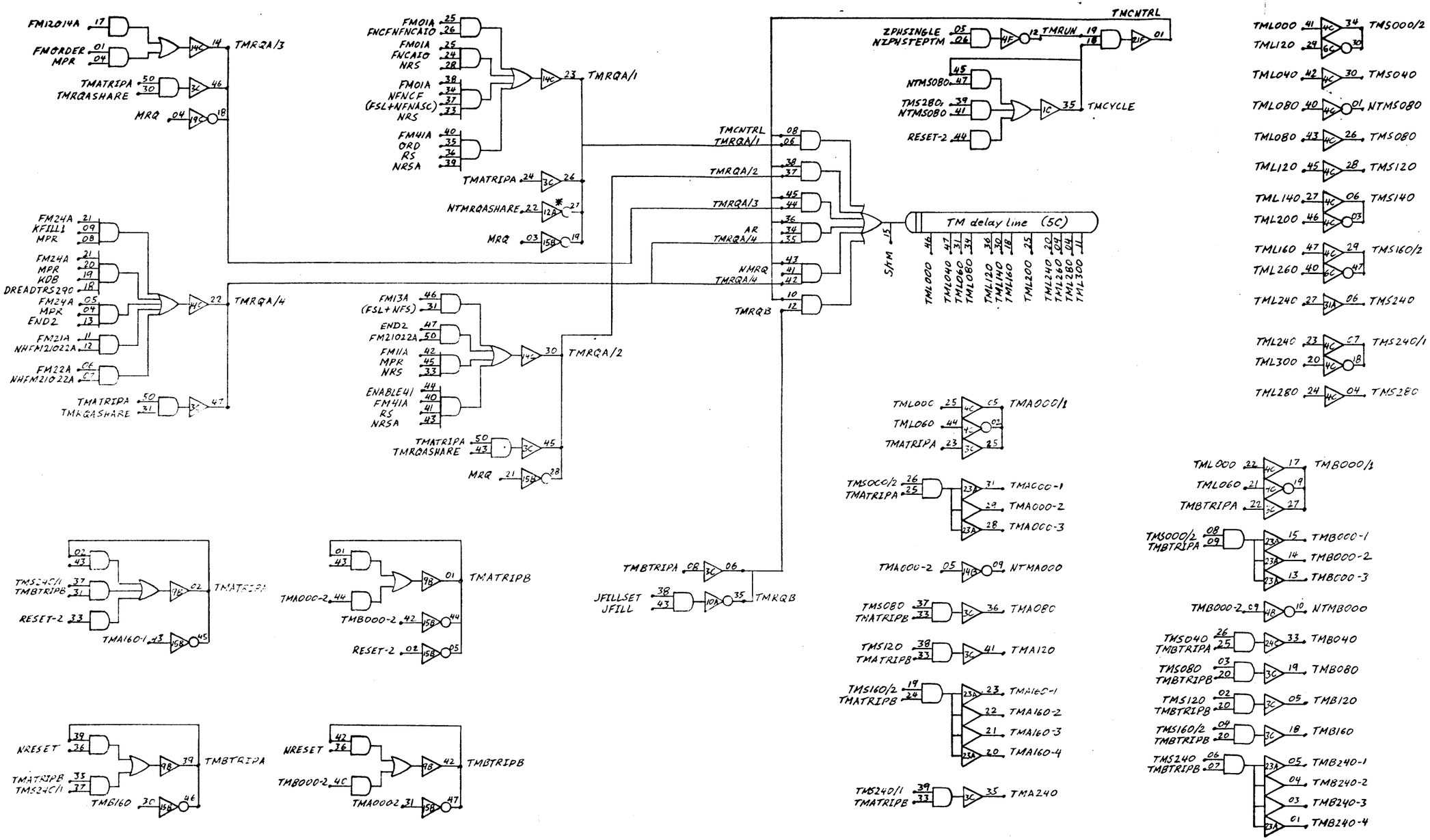
where R =



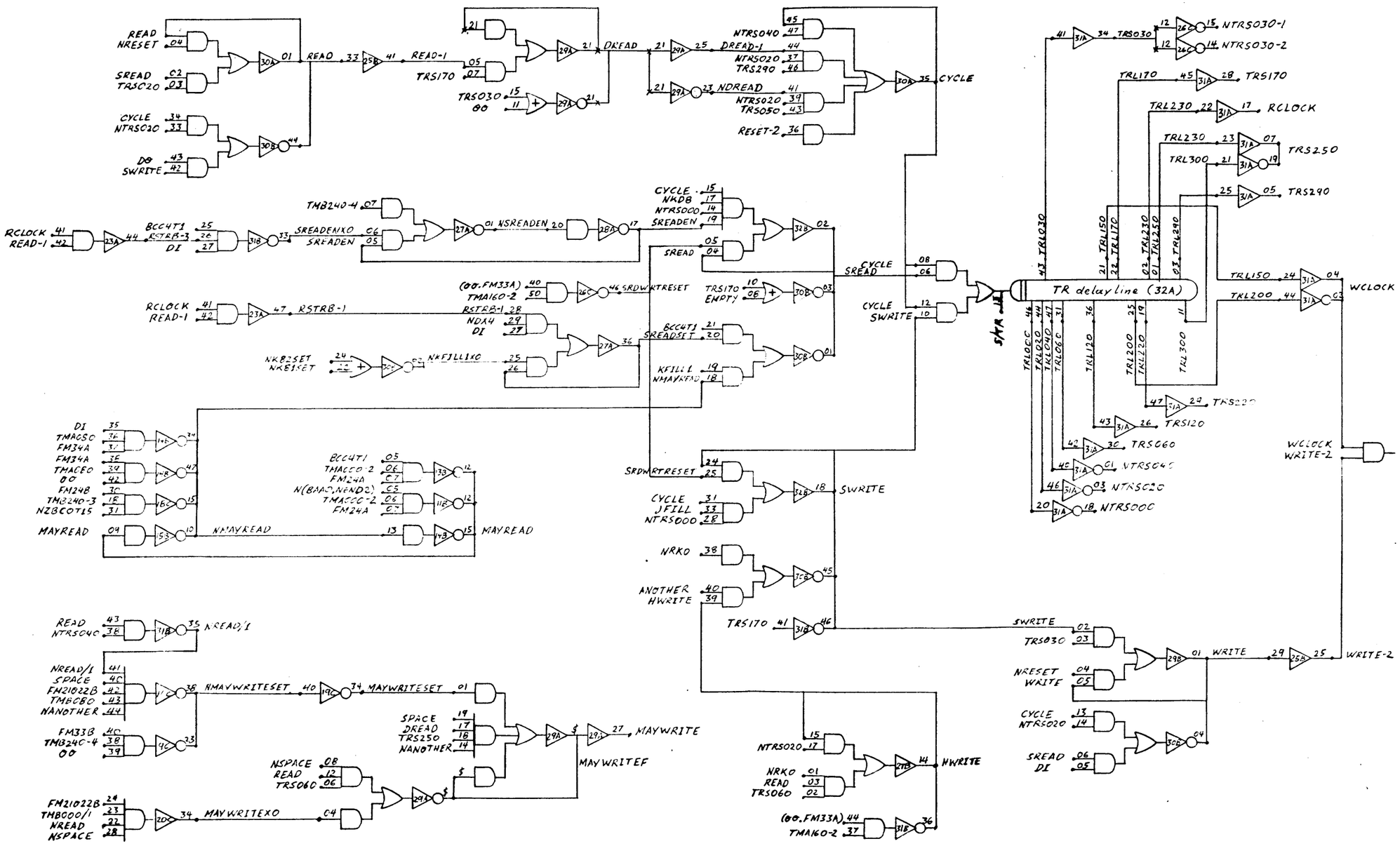
TI Delay line (SIOP)



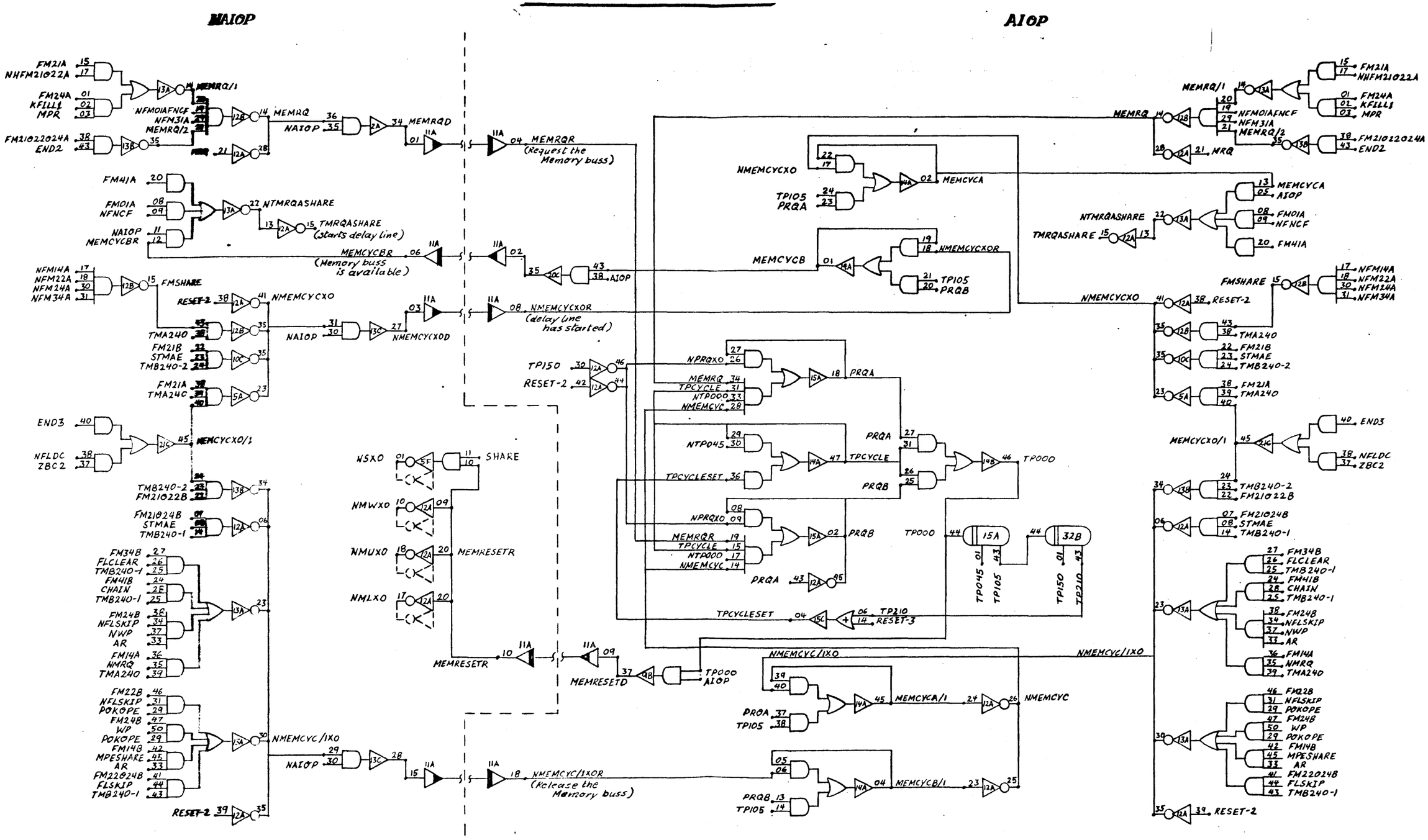
TM Delay Line (SIOP)



Fast Memory (TR) Delay Line. (S10P)



BUSS SHARING OPTION (SIOP)



D.C. Interface

RS(1HE27)
ES (1HE09)
IOA0(3HE23)
IOA1(3HE19)
IOA3&6(3HE18)
RSA (1HE03)

FM41A (5B42)

S/TM = RS (1HE27)
(5C15)

TMA000/1: MIXO (16F02)
(4C02) drops to clear IOreg.
[MPE]:STTME (4A16)
transmission memory error.
DATAERR (9A30)
[LBCOT15.FLIZC]=STIBCI (4E02)

TMA000-3: ES (1HE09)
(2JA28)

TMA080: [DATAERR.FLHTE]=STIOPH (4A09)
(3C36)

TMA160: FMHIB (4A39)
(2JA22) [STIBCI]=IOAC (3HE23)
Interrupt
[LBCOT15]=IOA1 (2HE19)
count done
[STIOPH]=IOA3 (3HE18)
IOP halt.

TMA240-3: FIOIA (3F34)
(2JA03)

TMB040: [CHAIN.NSTIOPH]=NFLXO (14B33)
(2HC33) drops to clear flags.

TMB120: RSA (1HE03)
(3C05)

TMB160: [CHAIN.NSTIOPH]=FLXN (20C45)
(3C18)

MA0 → FLDC (9021)
MA1 → FLIZC (9044)
MA2 → FLCC (9008)
MA3 → FLICE (9007)
MA4 → FLHTE (9002)
MA5 → FLILE (9001)
MA6 → FLSIL (9039)
MA7 → FLSKIP (9042)

Data Out DX4 continued.

FM41A

Display Control Logic (SIOP)

32F41 ZDIO:A15:R
32F40 ZDIO:A14:R
32F39 ZDIO:A13:R
32F38 ZDIO:A12:R

10 41F 01 NZDIO:A15:R
37 41F 36 NZDIO:A14:R
43 41F 35 NZDIO:A13:R
39 41F 45 NZDIO:A12:R

ZDIO:A15:R 41
NZDIO:A14R 42
NZDIO:A13R 43
NZDIO:A12:R 44
→ 31F 38 ZGP1

NZDIO:A15:R 47
ZDIO:A14:R 46
NZDIO:A13:R 50
NZDIO:A12:R 45
→ 31F 39 ZGP2

ZDIO:A15R 22
ZDIO:A14:R 23
NZDIO:A13R 24
→ 31F 35 ZGP3

NZDIO:A15:R 19
NZDIO:A14:R 18
ZDIO:A13:R 15
→ 31F 10 ZGP4

ZDIO:A15:R 05
NZDIO:A14:R 04
ZDIO:A13:R 03
→ 31F 09 ZGP5

NZDIO:A15R 01
ZDIO:A14R 02
ZDIO:A13R 06
→ 31F 07 ZGP6

ZDIO:A15R 05
ZDIO:A14:R 04
ZDIO:A13:R 03
→ 14F 09 ZGP7

NZDIO:A15:R 12
NZDIO:A14:R 13
NZDIO:A13R 14
→ 31F 08 ZGP8

ZDIO:A15R 25
NZDIO:A14:R 26
NZDIO:A13:R 27
ZDIO:A12:R 28
→ 31F 36 ZGP9

NZDIO:A15R 33
ZDIO:A14:R 31
NZDIO:A13:R 30
ZDIO:A12:R 29
→ 31F 37 ZGPA

RESET-2 21 → 3G 28 RESET-3

NRESET 13 → 4B 15

32F31 ZDIODB29:R 17
ZDIO:RWD:R 18
ZDIS:STROBE 11
ZDIS:ABLE 30
→ 4F 15 NRESET

NZDIS:ABLE 03 → 4F 02 ZDIS:ABLE

32F47

AIIR FSR Addr. Recog. 32F43

ZDIS:STROBE 08 10
TIS240 12
TM8080 13
→ 3G 07 ZDL/EN
40 → 4F 46 NZDL/EN

32F42

NZDL/EN 25
ZDIS:STROBE 26
ZDIO:RWD:R 28
ZDIO:DB31:R 27
→ 3E 36 ZPHSTEP

32F34

ZDIS:STROBE 50
ZDIO:RWD:R 48
ZDIO:DB30:R 46
→ 3E 39 ZPHSINGLE/M

32F33

21 → 4F 14 NZDIO:DB28:R

32F30 ZDIODB28:R

ZPHSTEP 29
NZDIO:DB28:R 27
→ 3F 30 PHSTEPTI
28 NPHSTEPTI

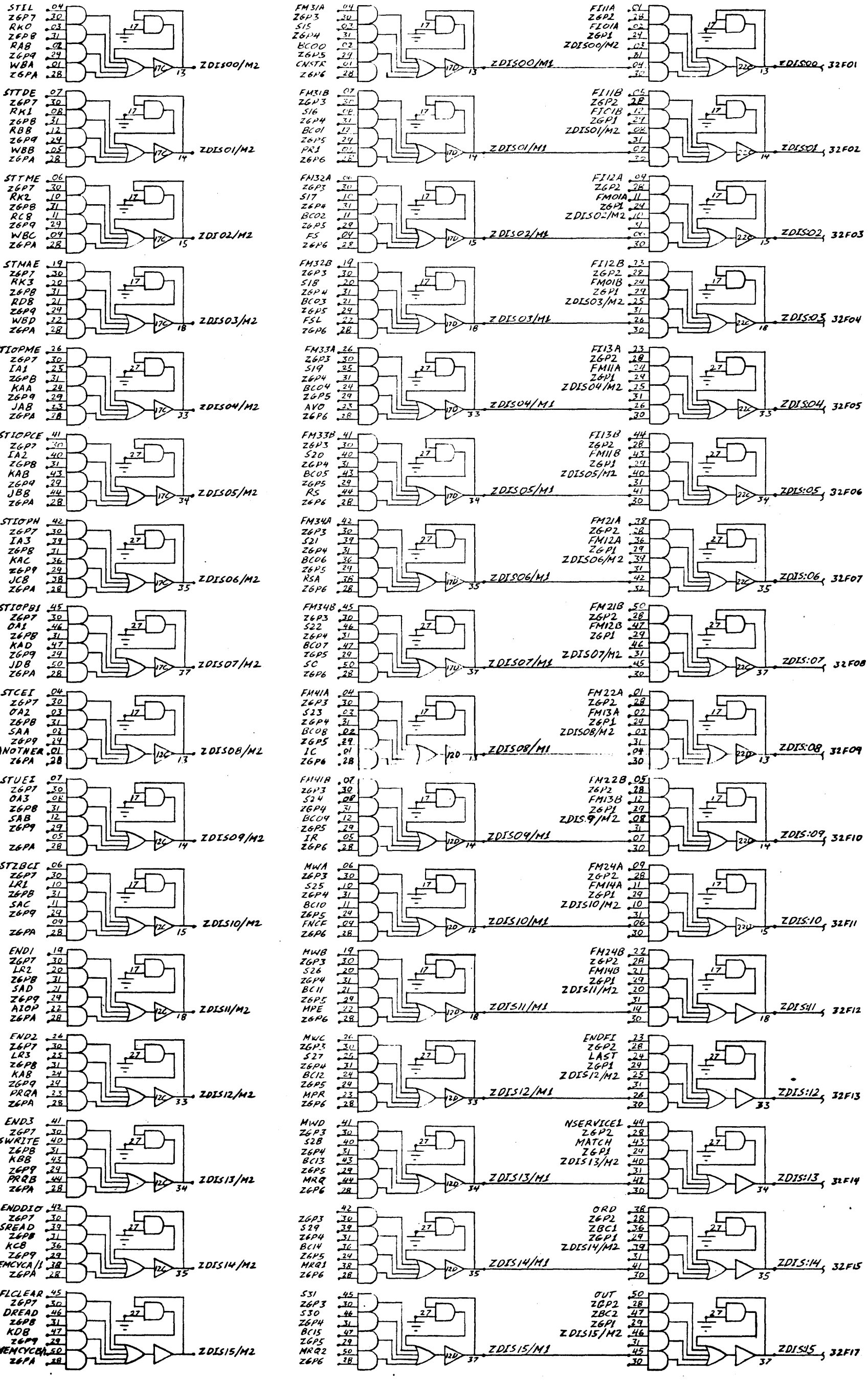
RESET-3 01
TIS240 26
→ + 08 04 → 4F 13 TIRUN

NRESET 40 39
ZDIS:ABLE 37
ZPHSINGLE/M 38
→ 2E 45 ZPHSINGLE

ZPHSTEP 38
ZDIO:DB28:R 39
→ 3F 34 NZPHSTEPTM

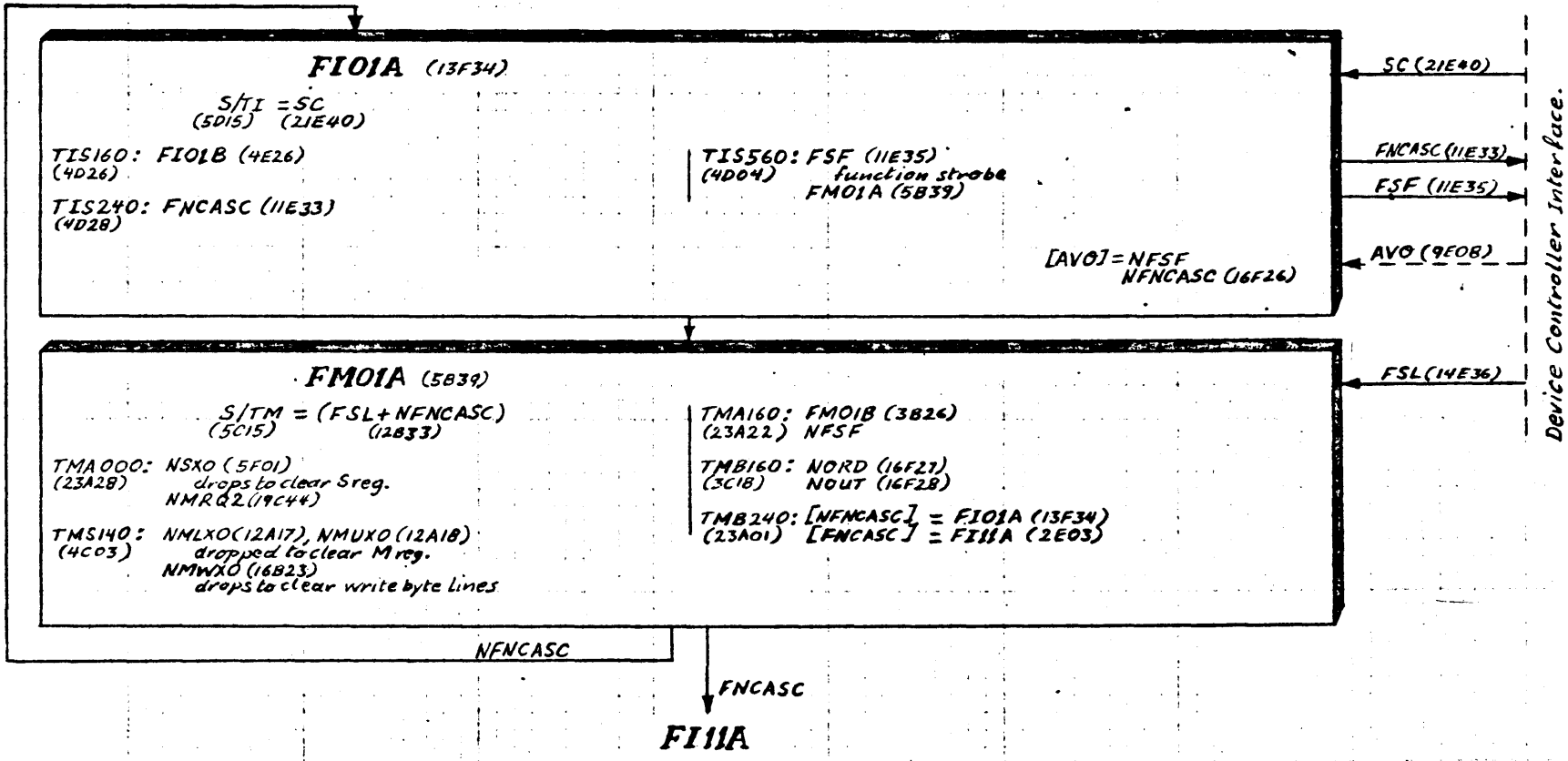
RESET-3 01
TM8080 40
→ + 05 06 → 4F 12 TMRUN

Display Logic (SIOP)

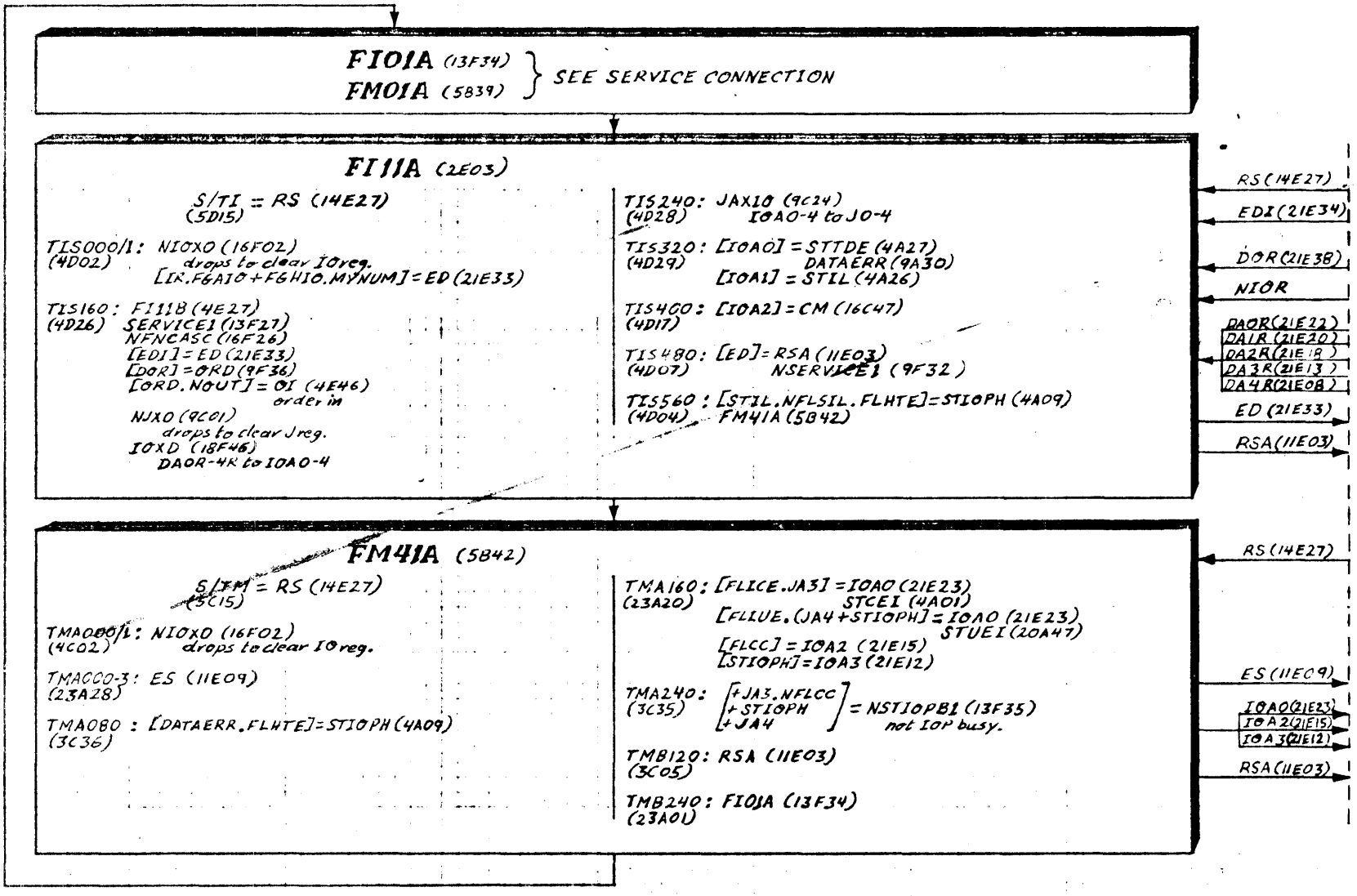


SERVICE CALL

Service Connection (SIOP)



ORDER IN (SIOP)



Order:

DAOR = data transmition error
DA1R = incorrect length
DA2R = chaining modifier bit
DA3R = channel end
DA4R = unusual end

Terminal Order:

IOAO = interrupt
IOA2 = command chain
IOA3 = IOP error

ORDER OUT (SIOP)

FI01A (13F34)
FM01A (5B39)
} SEE SERVICE CONNECTION

FI11A (2E03)

S/TI = RS (14E27) (5D15)

TIS000 : [IR.FGAIO+FGHIO.MYNUM] = ED (21E33) (4D02) MPR (16C01)

TIS160 : FI11B (4E27) (4D26) NFNCASC (16F26) [DOR] = ORD (9F36) [IOR] = OUT (9F39) [ORD.OUT] = 00 (4E21) [EDI] = ED (21E33) SERVICE1 (13F27)

TIS320 : FM31A (15B12) (4D29)

RS (14E27)
IOR (14E34)
DOR (21E38)
EDI (21E34)
ED (21E33)

FM31A (5B12)

S/TM = MPR (16C01) (5C15)

Get and dispose of 1rst. Word

TMA000/1 : NSXO (5F01) (4C02) drops to clear Sreg.

TMA000 : SXCA (3D26) (23A28) CAreg. to Sreg.

MRQ (13D01) ←

TMS140 : NMLXO (12A17), NMUXO (12A18) (4C03) dropped to clear Mreg.
NMWXO (16B23) drops write byte lines for read
[NCM] = MRQ (13D01) memory request.
CAreg. +1

POK (13D27) →
DG (15D38) →
PE (13D13) →
[POK] = MPR (16C01)
[DG] = MXM (16E46)
[PE] = MPE (16C02)

TMA160 : FM31B (3B02) (23A20) CHAIN (16C46) [NCM] = MRQ2 (15C47) NMPE

TMB000-2 : NCM (4B11) (23A14)

TMB080 : [MRQ.NAH] = STMAE (4A07) (3C19) STIOPH (4A09)

TMB240 : [NSTMAE.NMRQ2] = FM31A (5B12) (23A01) [NSTMAE.MRQ2] = FM32A (5B07) [STMAE] = FM33A (5B02)

Chaining Modifier was true

Memory address error.

FM32A (5B07)

Transfer in channel.

S/TM = MPR (16C01) (5C15)

TMA000/1 : NIOXO-A (16F01) (4C02) drops to clear IOreg [MA4.NMA5.NMA6.NMA7] = TRA (12E15) transfer in channel.

TMA000 : IOXM (3D01) (23A28) Order to IOA0-7 [MPE] = STIOPME (4A21)

TMS140 : [TRA.NMPE] = CAXM (22F01) (4C03) MC0-7@MD0-7 to CA reg.

TMA160 : FM32B (3B01) (23A20) [TRA.TRA1] = STIOPCE (4A12) control error.
[if IOA4-7 = C_{16}] = BKWD (2E47) read backwards.

TMB000 : [STIOPME+STIOPCE] = STIOPH (4A09) (23A14)

TMB080 : [TRA] = TRA1 (16C44) (3C19) remembers TRA

TMS140 : [NBKWD] = BAXM (3D34) (4C03) MB5-7@MC0-7@MD0-7 to BA00-18
[BKWD] = BAXM (3D34) MB5-7@MC0-7@MD0-5 to BA00-16, NMD6 to BA17, NMD7 to BA18

TMB240 : [TRA.NSTIOPH] = FM31A (5B12) (23A01) [NTRA+STIOPH] = FM33A (5B02)

ICA0 (21E23)
ICA1 (21E19)
ICA2 (21E15)
ICA3 (21F12)
ICA4 (21E03)
ICA5 (21E09)
ICA6 (21E01)
ICAT (21E02)

Transfer in channel.

Get and dispose of 2nd. Word

FM33A (5B02)

S/TM = FM33A (5B02) (5C15)

TMA000-3 : S31 (8D30) (23A28) for odd loc. access

MRQ (13D01) ←

TMS140 : NMLXO (12A7), NMUXO (12A18) (4C03) dropped to clear Mreg.
[NSTIOPH] = MRQ (13D01) memory request

POK (13D27) →
DG (15D38) →
PE (13D13) →
[POK] = MPR (16C01)
[DG] = MXM (16E46)
[PE] = MPE (16C02)

TMA160 : FM33B (3B39) (23A20) IABAXO (24C46) set IA reg. to 0's set OA reg. to 0's set RK reg. to 1's

TMB000-3 : RSA (11E03) (23A13) [RSA.ED] = NSERVICE1 (9F18)

TMB240-4 : FM34A (5B01) (23A01)

RSA (11E03)

FM34A (5B01)

S/TM = MPR (16C01) (5C15)

TMA000-2 : FLCLEAR (19C18) (23A29)

TMA080 : [MPE] = STIOPME (4A21) (3C36)

TMS140 : [NSTIOPH] = BCXM (14F37) (4C03) MC0-7@MD0-7 to BC reg.

TMA160 : FM34B (3B42) (23A20) [+ORD +STIOPH +DO.NFAST.FLIZC +DI.ED.FLIZC NMPE] = NFLCLEAR (29C02)

TMB040 : [FLCLEAR] = NFLX0 (14B33) (24C33) drops to clear flags.

TMB160 : [FLCLEAR] = FLXM (20C45) (3C18)
MA0 → FLDC (9D21)
MA1 → FLIZC (9D46)
MA2 → FLCC (9D09)
MA3 → FLICE (9D07)
MA4 → FLHTE (9D02)
MA5 → FLIUE (9D01)
MA6 → FLSIL (9D39)
MA7 → FLSKIP (9D42)

TMB240 : [DO.FLCLEAR] = FM21A (5B26) (23A01) [DI.FLCLEAR] = FM24A (5B27) [NFLCLEAR] = FM41A (5B42)

FM41A (5B42)

S/TM = RS (14E27) (5C15)

TMA000/1 : NIOXO (16F02) (4C02) drops to clear IOreg.

TMA000-3 : ES (11E09) (23A28)

TMA160 : FM41B (4A39) (23A20) [STIOPH] = IOA3 (21E12)

TMB040 : [NSTIOPH] = NFLXO (14B33) (24C33) drops to clear flags

TMB120 : RSA (11E03) (3C05)

TMB160 : [NSTIOPH] = FLXM (20C45) (3C18)
MA0 → FLDC (9D21)
MA1 → FLIZC (9D46)
MA2 → FLCC (9D09)
MA3 → FLICE (9D07)
MA4 → FLHTE (9D02)
MA5 → FLIUE (9D01)
MA6 → FLSIL (9D39)
MA7 → FLSKIP (9D42)

TMB240 : FI01A (13F34) (23A01)

RS (14E27)
ES (11E09)
IOA3 (21E12)
RSA (11E03)

Memory Interface

Device Controller Interface.

Data In DX1 (S10P)

Preset during Order Out
- SREADEN (28A17)
- MAYREAD (14B15)
- IA reg. to all 0's
- 0A reg. to all 0's
- RK reg. to all 1's
- EMPTY (15B17)
- SPACE (10A02)
- [NBA17.NBA18] = NKAB.NKBB.NKCB.NKDB
- [NBA17.BA18] = KAB.NKBB.NACB.NKDB
- [BA17.NBA18] = KAB.KBB.NACB.NKDB
- [BA17.BA18] = KA5.KBB.KCB, NKDB

FI01A (13F34)
FM01A (5B34)
} SEE SERVICE CONNECTION

FI11A (2E03)

Data flow

S/TI = RS (14E27) (5D15)

TIS000/1: [IR.FGA10+FGH10.MYNUM1=ED (21E33) (4D02) NICXC (16F02) drops to clear IO reg.

TIS160: FI11B (4127) (4D26) SERVICE1 (13F27) inhibits TIC's and TDV's
NFNCASC (16F26)
[EDI]=ED (21E33)
[NORD.NOUT]=DI (4E07) data in.
NJXO (9C01) drops to clear Jreg.
IOXD (18F45) DAOR-7R to IOA0-7

TIS240: JAX10 (9C24), JX10 (11F05) (4D28) IOA0-7 to JA0-7
JAB (26C01)

TIS320: FM24A (5B27) (4D24) JFILL (24B15) Jreg is filled.
[NED]: RSA (11E03)

TIS400: [PC.IOAEVEN]=STTDE (4A27) (4D17) DATAERR (9A30)

TIS460: [ED]=RSA (11E03) (4D07) [ED.RSA]=NSERVICE1 (9F16)

TIS560: NIOXO (16F02) (4D04) drops to clear IO reg.
[NED]=FI13A (1E30)

RS (14E27)
NDOR
NIOR
EDI (21E34)
ED (21E33)
PC (16E15)
DAOR (21E22)
DA1R (21E20)
DA2R (21E16)
DA3R (21E13)
DA4R (21E05)
DASR (21E10)
DACR (21E04)
DA7R (21E06)
DAPR (21E27)
RSA (11E03)

Device Controller Interface

WRITE into Fast Memory.

[WA8] = RAXJA (30C47) JA0-8 to W/RO-8

SWRITE = JFILL . RKO (32B18) (24B15) (31C33)

S/TR = SWRITE . CYCLE (32A15) (32B18) (30A35)

TRS030: WRITE (25B26) (31A34)

TRS060: IA reg. to LR reg. (31A30) NJFILL (29A22)

TRS120: NEMPTY (18C34) (31A26) IA reg. +1
RK reg. −1
NJA8 (28B45)

TRL150: W/RA0-8 to RA0-8 (32A21)

TRS250: [ED] = END1 (9B26) (31A07) remembers ED

READ from Fast Memory.

[NKA8.NKB8.NKC8.NKD8]

SREAD = .SREADEN.NKD8.NEMPTY (32B02) .N(KFILL1.NMAYREAD)

S/TR = .SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: CA reg. to LR reg. (31A30) [RA8] = SAA (25B45)

TRS120: [NKA8] = KAA (25A46) (31A26) [SAA.KAA] = PATH0 (26B37)
CA reg +1
RK reg +1

TRL230: [PATH0] = MODE0 (13C17) (32A02) RA0-7 to KA0-7
[BCC4T1] = NSREADEN
[PATH0.RA8] = KA8 (24B10)

TRS290: [BCC4T1] = KFILL1 (30A21) (31A05) [EMPTY.END1] = END2 (9B27)

[NBCC4T1.NEMPTY]

[KA8.NKB8.NKC8.NKD8]

SREAD = .SREADEN.NKD8.NEMPTY (32B02) .N(KFILL1.NMAYREAD)

S/TR = .SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: CA reg. to LR reg. (31A30) [RA8] = SAA (25B45)

TRS120: [KA8.NKB8] = KA8 (25A47) (31A26) [SAA.KA8] = PATH1 (26B33)
CA reg +1
RK reg +1

TRL230: [PATH1] = MODE1 (10B09) (32A02) RA0-7 to KB0-7
[BCC4T1] = NSREADEN (27A01)
[PATH1.RA8] = KB8 (24B27)

TRS290: [BCC4T1] = KFILL1 (30A21) (31A05) [EMPTY.END1] = END2 (9B27)

[NBCC4T1.NEMPTY]

[KA8.KB8.NKC8.NKD8]

SREAD = .SREADEN.NKD8.NEMPTY (32B02) .N(KFILL1.NMAYREAD)

S/TR = SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: CA reg. to LR reg. (31A30) [RA8] = SAA (25B45)

TRS120: [KA8.KB8.NKC8] = KAC (25A44) (31A26) [SAA.KAC] = PATH3 (26B35)
CA reg +1
RK reg +1

TRL230: [PATH3] = MODE3 (13C33) (32A02) RA0-7 to KC0-7
[BCC4T1] = NSREADEN (27A01)
[PATH3.RA8] = KC8 (24B11)

TRS290: [BCC4T1] = KFILL1 (30A21) (31A05) [EMPTY.END1] = END2 (9B27)

[NBCC4T1.NEMPTY]

[KA8.KB8.KC8.NKD8]

SREAD = SREADEN.NKD8.NEMPTY (32B02).N(KFILL1.NMAYREAD)

S/TR = .SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: CA reg to LR reg. (31A30) [RA8] = SAA (25B45)

TRS120: [KA8.KB8.KC8] = KAD (25A45) (21A26) [SAA.KAD] = PATH5 (26B34)
CA reg. +1
RK reg. +1

TRL230: [PATH5] = MODE5 (20A25) (32A02) RA0-7 to KD0-7
[BCC4T1] = NSREADEN (27A01)
[PATH5.RA8] = KD8 (24B25)

TRS290: [KD8] = KFILL1 (30A21) (31A05) [EMPTY.END1] = END2 (9B27)

NZBC2.NEND2.NSTMAE

FM24A (5B27)

S/TM = NMRQ.(KFILL1+END2) (5C15)

TMA000/1: NWBXO (12B45) (4C02) drops to clear WBA-D
NSXO (5F01) drops to clear Sreg.

TMA000: SXBA (3D18) (23A28) BA reg to Sreg.
WBSET (10B35) sets up WBA-D
[NBA17.NBA18.KA8] = WBA (29C26)
[+NBA17.BA18.KBB, +NBA17.NBA18.NBCC1.KBB] = WBB (29C27)
[+BA17.NBA18.KCB, +NBA17.BA18.NBCC1.KCB, +NBA7.NBA18.NBCC1.NBCC2.KCB] = WBC (29C12)
[+BA17.BA18.KDB, +BA17.NBA18.NBCC1.KDB, +NBA17.BA18.NBCC1.NBCC2.KDB, +NBA17.NBA18.NBCC1.NBCC2.NBCC3.KDB] = WBD (29C14)
[+BCC4T1+END2, +BA17+BA18] = NMAYREAD (14B34)

TMA080: [MAYREAD.NBA17.NBA18] = NKA8, NKB8, NKCB, NKD8 (3C36)
[MAYREAD.NBA17.BA18] = KA8, NKB8, NKCB, NKD8
[MAYREAD.BA17.NBA18] = KA8, KB8, NKCB, NKD8
[MAYREAD.BA17.BA18] = KA8, KB8, KCB, NKD8

TMS140: NMLXO (12A17), NMUXO (12A18) (4C03) dropped to clear Mreg.
[NFLSKIP] = MRQ (13D01)
[NBKWD] = BAreg. + # of bytes to be stored
[BKWD] = BA17-18 + # of bytes to be stored.
BA0-16 −1 if BA17-18 are incremented above a count of 3
BC reg. − # of bytes to be stored.

TMA160: FN24B (3B07) (23A20) [NBKWD] = MXKF (16E34) Kreg. to Mreg. WBA-D to MWA-D
[BKWD] = MXKB (16E28) KA0-7 to MD0-7, WBA to MWD
KB0-7 to MC0-7, WBB to MWC
KC0-7 to MB0-7, WBC to MWB
KD0-7 to MA0-7, WBD to MWA

TMS240/1: NKXO (24B05) drops to clear Kreg. (4C07)

TMB080: [MRQ.NAH] = STMAE (4A07), STIOPH (4A09)
[NZBCOT15] = NKFILL
[NMAYREAD.NBA17.NBA18] = NKA8, NKB8, NKC8, NKD8
[NMAYREAD.NBA17.BA18] = KA8, NKB8, NKC8, NKD8
[NMAYREAD.BA17.NBA18] = KA8, KB8, NKC8, NKD8
[NMAYREAD.BA17.BA18] = KA8, KB8, KC8, NKD8

TMB160: [ZBCOT15] = ZBC1 (15C44) zero byte count. (3C18)

TMB240: SREADEN (28A17) (23A01) [NZBCOT15] = MAYREAD (14B15)
[ZBCOT15] = STZBC1 (4A02)
[NZBCOT15.NEND2.NSTMAE] = FM24A (5B27)
[ZBCOT15.FLDC.NSTMAE] = FM31A (5B12)
[END2+ZBCOT15.NFLDC+STMAE] = FM41A (5B42)

MRQ (13D01)

AR (13D08)

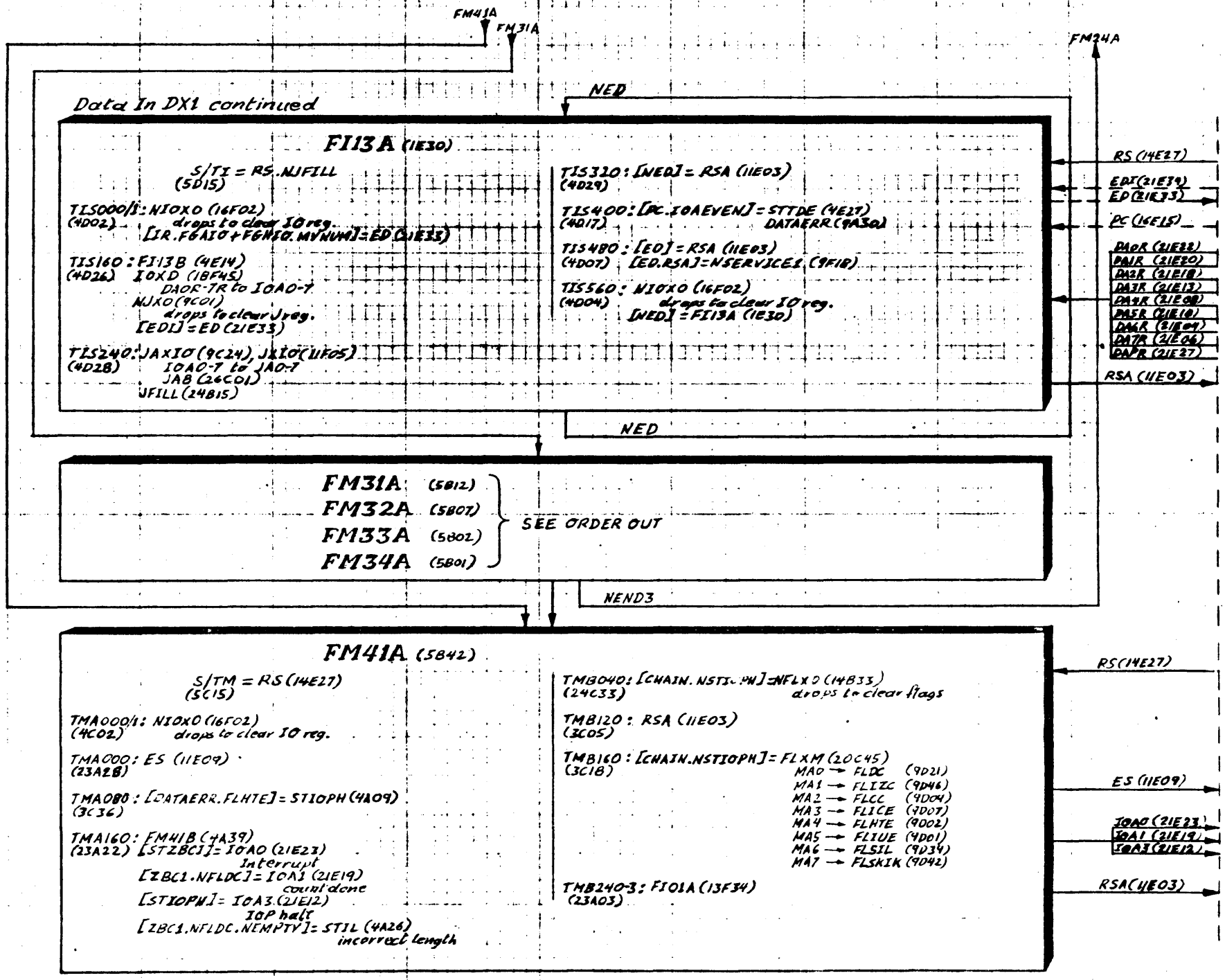
[AR] = NMRQ (19C36)

Memory Interface Page 3-184/3-188A

FI13A

FM41A

FM31A


FM41A
FM31A
FM24A
NED
Data In DX1 continued
FI13A (1E30)
S/TI = RS.NJFILL (5D15)
TIS000/1: NIOXO (16F02) (4D02) drops to clear IO reg. [IR.FGAIO+FGNIO.MYNUM]=ED (21E33)
TIS160: FI13B (4E14) (4D26) IOXD (18F45) DAOR-7R to IOAO-7 NJXO (9C01) drops to clear Jreg. [EDI]=ED (21E33)
TIS240: JAXIO (9C24), JXIO (11F05) (4D28) IOAO-7 to JAO-7 JAB (26C01) JFILL (24B15)
TIS320: [NED]=RSA (11E03) (4D29)
TIS400: [PC.IOAEVEN]=STTDE (4E27) (4D17) DATAERR (9A30)
TIS480: [ED]=RSA (11E03) (4D07) [ED.RSA]=NSERVICES (9F18)
TIS560: NIOXO (16F02) (4D04) drops to clear IO reg. [NED]=FI13A (1E30)
RS (14E27)
EDI (21E34)
ED (21E33)
PC (16E15)
DAOR (21E22)
DA1R (21E20)
DA2R (21E18)
DA3R (21E13)
DA4R (21E08)
DA5R (21E10)
DA6R (21E09)
DA7R (21E06)
DAPR (21E27)
RSA (11E03)
NED
FM31A (5B12)
FM32A (5B07)
FM33A (5B02)
FM34A (5B01)
SEE ORDER OUT
NEND3
FM41A (5B42)
S/TM = RS (14E27) (5C15)
TMA000/1: NIOXO (16F02) (4C02) drops to clear IO reg.
TMA000: ES (11E09) (23A28)
TMA080: [DATAERR.FLHTE]=STIOPH (4A09) (3C36)
TMA160: FM41B (4A39) (23A22) [STZBC]=IOA0 (21E23) Interrupt [ZBC1.NFLDC]=IOA1 (21E19) count done [STIOPH]=IOA3 (21E12) IOP halt [ZBC1.NFLDC.NEMPTY]=STIL (4A26) incorrect length
TMB040: [CHAIN.NSTIOPH]=NFLXO (14B33) (24C33) drops to clear flags
TMB120: RSA (11E03) (3C05)
TMB160: [CHAIN.NSTIOPH]=FLXM (20C45) (3C18)
MA0 → FLDC (9D21)
MA1 → FLIZC (9D46)
MA2 → FLCC (9D04)
MA3 → FLICE (9D07)
MA4 → FLHTE (9D02)
MA5 → FLIUE (9D01)
MA6 → FLSIL (9D34)
MA7 → FLSKIK (9D42)
TMB240-3: FIO1A (13F34) (23A03)
RS (14E27)
ES (11E09)
IOA0 (21E23)
IOA1 (21E19)
IOA3 (21E12)
RSA (11E03)
Device Controller Interface

Data In DX4 (S1OP)

Preset during Order Out
- SNEADEN (3BA17)
- NEAVREAD (1BA18)
- IAreg. to all Cs
- OAreg. to all Os
- RKreg to all 1s
- EMPTY (15B17)
- SPACE (10AC2)
- [NBA17.NBA16] = NKA8.NKB8.NKC8.NKD8
- [NBA17.BA18] = KA8.NKB8.NKC8.NKD8
- [BA17.NBA18] = KA8.KB8.NKC8.NKD8
- [BA17.BA18] = KA8.KB8.KC8.NKD8

FI01A (13F34)
FM01A (5B39)
} SEE SERVICE CONNECTION

FI11A (2E03)

1rst Data flow

S/TI = RS (14E27) (5D15)

TIS000/1: [IR.FGA10+FGH10.MYNUM] = ED (21E33) (4D02)
NIOXO (16F02) drops to clear IOreg.

TIS160: FI11B (4E27) (4D26)
SERVICE1 (13F27) inhibits TIOs and TDVs
NFNCASC (16F26)
[EDI] = ED (21E33)
[NORD.NOUT] = DI (4E07) data in
NJXO (9C01) drops to clear Jreg.
IOXD (18F45) Data lines to IOreg

TIS240: JAX10 (9C24), JXO (11F05) (4D28)
IOreg to Jreg.
JA$ (26C01)
JB$ (26C02)
JC$ (26C10)
JD$ (26C04)

TIS320: FM24A (5B27) (4D29)
JFILL (24B15) Jreg. is filled
[NED] = RSA (11E03)

TIS480: [ED] = RSA (11E03) (4D07)
[ED.RSA] = NSERVICE1 (9F18)

TIS560: NIOXO (16F02) (4D04)
drops to clear IOreg.
[NED] = FI13A (1E30)

RS (14E27)
EDI (21E34)
ED (21E33)
DAOR-DA7R
DBOR-DB7R
DCOR-DC7R
DDOR-DD7R
RSA (11EC3)

Device Controller Interface

WRITE into Fast Memory.

JA0-8 to W/RA0-8
JB0-8 to W/RB0-8

SWRITE = JFILL.RKO (32B18) (24B15) (31C33)

S/TR = SWRITE.CYCLE (32A15) (32B18) (30A35)

TRS030: WRITE (25B26) (31A34)

TRS060: IAreg.to LRreg. (31A30) NJFILL (29A22)

TRS120: NEMPTY (18C34) (31A26)
IAreg+1
RKreg -1

TRL150: W/RA0-8 to RA0-8
W/RB0-8 to RB0-8
JC0-8 to RC0-8
JD0-8 to RD0-8
(32A21)

TRS250: [ED] = END1 (9B26) (31A07)
remembers ED

1rst READ from Fast Memory

[NKA8.NKB8.NKC8.NKD8]

SREAD = .NKD8.NEMPTY.SREADEN (32B02) .N(KFILL1.NMAYREAD)

S/TR = SREAD.CYCLE (5D15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: OAreg.to LRreg. (31A30) [RA8] = SAA (25B45)

TRS120: [NKA8] = KAA (25A46) (31A26)
[SAA.KAA] = PATH0 (26B37)
OAreg.+1
RKreg.+1

TRL230: [PATH0] = MODE0 (13C17) (32A02)
RA0-7 to KA0-7
RB0-7 to KB0-7
RC0-7 to KC0-7
RD0-7 to KD0-7
KA8 (24B10)
KB8 (24B27)
KC8 (24B11)
KD8 (24B25)
[BCC4T1] = NSREADEN (27A01)

TRS290: [KD8] = KFILL1 (30A21) (31A05)
[EMPTY.END1] = END2 (9B27)

[KA8.NKB8.NKC8.NKD8]

SREAD = .NKD8.NEMPTY.SREADEN (32B02) .N(KFILL1.NMAYREAD)

S/TR = SREAD.CYCLE (5D15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: OAreg.to LRreg. (31A30) [RA8] = SAA (25B45)

TRS120: [KA8.NKB8] = KA8 (25A47) (31A26)
[SAA.KA8] = PATH1 (26B33)
OAreg.+1
RKreg.+1
[KA8.RD8] = ANOTHER (26C33)

TRL230: [PATH1] = MODE1 (10B04) (32A02)
RA0-7 to KB0-7
RB0-7 to KC0-7
RC0-7 to KD0-7
KB8 (24B27), KC8 (24B11), KD8 (24B25)
[BCC4T1] = NSREADEN (27A01)

TRS290: [KD8] = KFILL1 (30A21) (31A05)
[ANOTHER] = OAreg -1
RKreg -1
[ANOTHER.PATH1] = RAM (22A21)
grounds RA8
RBM2 (22A09)
grounds RB8
RCM (22A07)
grounds RC8

[KA8.KB8.NKC8.NKD8]

SREAD = .NKD8.NEMPTY.SREADEN (32B02) .N(KFILL1.NMAYREAD)

S/TR = SREAD.CYCLE (5D15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: OAreg.to LRreg. (31A30) [RA8] = SAA (25B45)

TRS120: [KA8.KB8.NKC8] = KAC (25A44) (31A26)
[SAA.KAC] = PATH3 (26B35)
OAreg.+1
RKreg+1
[KAC.RC8] = ANOTHER (26C33)

TRL230: [PATH3] = MODE3 (13C33) (32A02)
RA0-7 to KC0-7
RB0-7 to KD0-7
KC8 (24B11), KD8 (24B25)
[BCC4T1] = NSREADEN (27A01)

TRS290: [KD8] = KFILL1 (30A21) (31A05)
[ANOTHER] = OAreg.-1
RKreg.-1
[ANOTHER.PATH3] = RAM (22A21)
grounds RA8
RBM1 (22A16)
grounds RC8

[KA8.KB8.KC8.NKD8]

SREAD = .NK8.NEMPTY.SREADEN (32B02) .N(KFILL1.NMAYREAD)

S/TR = SREAD.CYCLE (5D15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: OAreg.to LRreg. (31A30) [RA8] = SAA (25B45)

TRS120: [KA8.KB8.KC8] = KAD (25A45) (31A26)
[SAA.KAD] = PATH5 (26B34)
OAreg+1
RKreg+1
[KAD.RB8] = ANOTHER (26C33)

TRL230: [PATH5] = MODE5 (20A25) (32A02)
RA0-7 to KD0-7
KD8 (24B25)
[BCC4T1] = NSREADEN (27A01)

TRS290: [KD8] = KFILL1 (30A21) (31A05)
[ANOTHER] = OAreg.-1
RKreg.-1
RAM (22A21)
grounds RA8

FM24A (5B27)

S/TM = NMRQ.(KFILL1+END2) (5C15)

TMA000/1: NWBXO (12B45) (4C02)
drops to clear WBA-D
NSXO (5F01)
drops to clear Sreg.

TMA000: SXBA (3D18) (23A28)
BAreg to Sreg.
WBSET (10B35)
[NBA17.NBA18.KA8] = WBA (29C26)
[+NBA17.BA18.KB8, +NBA17.NBA18.NBCC1.KB8] = WBB (29C27)
[+BA17.NBA18.KC8, +NBA17.BA18.NBCC1.KC8, +NBA17.NBA18.NBCC1.NBCC2.KC8] = WBC (29C12)
[+BA17.BA18.KD8, +BA17.NBA18.NBCC1.KD8, +NBA17.BA18.NBCC1.NBCC2.KD8, +NBA17.NBA18.NBCC1.NBCC2.NBCC3.KD8] = WBD (29C14)
[BCC4T1+END2+BA17+BA18] = NMAYREAD (14B34)

TMA080: [MAYREAD] = NKA8 (21A01) (3C36)
NKB8 (22A01)
NKC8 (21A04)
NKD8 (21A03)

[AR] = NMRQ (19C36)

IMS140: NMLXO (12A17), NMUXO (12A18) (4C03)
dropped to clear Mreg.
[NFLSKIP] = MRQ (13D01)
BAreg.+ # of bytes to be stored
BCreg.- " of bytes to be stored

TMA160: FM24B (3B07) (23A20)
MXKF (16E34)
Kreg to Mreg.
WBA-D to MWA-D

TMS240/1: NKXO (24B05) (4C07)
drops to clear Kreg.

TMB080: [MRQ.NAH] = STMAE (4A07), STIOPH (4A09) (3C19)
[NZBCOT15] = NKFILL
[NMAYREAD.NBA17.NBA18] = NKA8, NKB8, NKC8, NKD8
[NMAYREAD.NBA17.BA18] = KA8, KB8, NKC8, NKD8
[NMAYREAD.BA17.NBA18] = KA8, KB8, KC8, NKD8
[NMAYREAD.BA17.NBA18] = KA8, KB8, KC8, NKD8

TMB160: [ZBCOT15] = ZBC1 (15C44) (3C18)
Zero byte count.

TMB240: [NZBCOT15] = MAYREAD (14B15) (23A01)
[ZBCOT15] = STZBC1 (4AC2)
[NZBCOT15.NEND2.NSTMAE] = FM24A (5B27)
[ZBCOT15.FLDC.NSTMAE] = FM31A (5B12)
[END2+ZBCOT15.NFLDC+STMAE] = FM41A (5B42)
SREADEN (28A17)

MRQ (13D01)
AR (13D08)

Memory Interface Page 3-190/3-190A

FI13A
FM41A
FM31A
KFILL1

FI13A

FM41A FM51A

KFILL1 FM24A

Data In DX4 continued.

FI13A (1E30)

2nd to n's Data Flow

S/TI = RS.NJFILL

TIS000/1: NIOXO (16F02) (4D02)
drops to clear IO reg.
[IR.FGAIC+IGHIC.MYNUM]= ED (21E33)

TIS160: FI13B (4E14) (4D26)
IOXD (15F45)
Data lines to IO reg.
NJXO (9C01)
drops to clear J reg.
[EDI] = ED (21E33)

TIS240: JAXIC (9C14), JXIC (11F05) (4D28)
IC reg to J reg.
JA8 (26C01), JB8 (26C02)
JC8 (26C10), JD8 (26C09)
JFILL (24B15)

TIS320: [NED] = RSA (11E03) (4D29)

TIS400: [ED] = RSA (11E03) (4D07)
[ED.RSA] = NSERVICE] (9F18)

TIS560: NIOXO (16F02) (4D04)
drops to clear IO reg.
[NEL] = FI13A (1E30)

RS (14E27)
EDI (21E34)
ED (21E33)
DA0R-DA7R
DB0R-DB7R
DC0R-DC7R
DD0R-DD7R
RSA (11E03)

Device Controller Interface

WRITE into Fast Memory

JA0-8 to W/RA0-8
JB0-8 to W/RB0-8

SWRITE = JFILL. (32B18) (24B15)

S/TR = SWRITE.CYCLE (32A15) (32B18) (30A35)

TRS030: WRITE (25B26) (31A34)

TRS060: IA reg to LR reg. (31A30) NJFILL (29A22)

TR120: IA reg + 1 (31A26) RK reg - 1
NEMPTY (18C34)

TRL150: W/RA0-8 to RA0-8 (32A21)
W/RB0-8 to RB0-8
JC0-8 to RC0-8
JD0-8 to RD0-8

TRS250: [ED] = END1 (9B26) (31A07)
remembers ED

READ from Fast Memory 2nd through n's time

[RAB] = SAA (25B45)

SREAD = .NKDB.NEMPTY.SREADEN .N(KFILL1.NMAYREAD) (32B02)

S/TR = SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: OA reg to LR reg. (31A30)

TRS120: [NKAB] = KAA (25A46) (31A26)
[SAA.KAA] = PATH0 (26B37)
OA reg + 1
RK reg + 1

TRL230: [PATH0] = MODE0 (13C17) (32A02)
RA0-7 to KA0-7
RB0-7 to KB0-7
RC0-7 to KC0-7
RD0-7 to KD0-7
KAB (24B10)
KBB (24B27)
KCB (24B11)
KDB (24B25)

TRS240: KFILL1 (30A21) (31A05)

[NRAB.NRBB.NRCB.RDA] = SAD (25B47)

SREAD = .NKDB.NEMPTY.SREADEN .N(KFILL1.NMAYREAD) (32B02)

S/TR = SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: OA reg. to LR reg. (31A30)

TRS120: [NKAB] = KAA (25A46) (31A26)
[SAD.KAA] = PATH2 (26B13)
OA reg + 1
RK reg + 1

TRS220: NANOTHER (25A02) (31A29)

TRL230: [PATH2] = MODE2 (20A34) (32A02)
RD0-7 to KA0-7
[KDB] = KAB (24B10)
[BCC1] = KDB (24B25)

TRS240: [NANOTHER] = NRAM (31A05)
NRBM2
NRCM
[EMPTY.END1] = END2 (9B27)

[KDB] = KFILL1 (30A21)

[NKDB.NEMPTY.SREADEN] = SREAD (32B02)

S/TR = SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: OA reg to LR reg. (31A30) [RAB] = SAA (25B45)

TRS120: [KAB.NKBB] = KAB (25A47) (31A26)
[SAA.KAB] = PATH3 (26B33)
OA reg + 1
RK reg + 1
[KAB.KDB] = ANOTHER (26C33)

TRL230: [PATH1] = MODE1 (10B09) (32A02)
RA0-7 to KB0-7
RB0-7 to KC0-7
RC0-7 to KD0-7
KBB (24B27), KCB (24B11), KDB (24B25)

TRS290: [KDB] = KFILL1 (30A21) (31A05)
[ANOTHER] = OA reg - 1
RK reg - 1
[ANOTHER.PATH1] = RAM (22A21)
grounds RAB
RBM2 (22A09)
grounds RBB
RCM (22A07)
grounds RCB

[NRAB, NRBB, RC8] = SAC (25B46)

SREAD = .NKDB.NEMPTY.SREADEN .N(KFILL1.NMAYREAD) (32B02)

S/TR = SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: CA reg. to LR reg. (31A30)

TRS120: [NKAB] = KAA (25A46) (31A26)
[SAC.KAA] = PATH4 (26B16)
OA reg + 1
RK reg + 1

TRS220: NANOTHER (25A02) (31A29)

TRL230: [PATH4] = MODE4 (20A28) (32A02)
RC0-7 to KA0-7
RD0-7 to KB0-7
[KBB] = KAB (24B10)
[KDB] = KBB (24B27)
[BCC1+BCC2] = KDB (24B25)

TRS290: [NANOTHER] = NRAM (31A05)
NRBM1
[EMPTY.END1] = END2 (9B27)

[KDB] = KFILL1 (30A21)

[NKDB.NEMPTY.SREADEN] = SREAD (32B02)

S/TR = SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: CA reg to LR reg. (31A30) [RAB] = SAA (25B45)

TRS120: [KAB.KBB.NKCB] = KAC (25A44) (31A26)
[SAA.KAC] = PATH3 (26B35)
OA reg + 1
KK reg + 1
[KAC.RCB] = ANOTHER (26C33)

TRL230: [PATH3] = MODE3 (13C33) (32A02)
RA0-7 to KC0-7
RB0-7 to KD0-7
KCB (24B11), KDB (24B25)

TRS290: [KDB] = KFILL1 (30A21) (31AC5)
[ANOTHER] = OA reg - 1
RK reg - 1
[ANOTHER.PATH3] = RAM (22A21)
grounds KAB
RBM1
grounds KBB

[NRAB.RBB] = SAB (25B44)

SREAD = .NKDB.NEMPTY.SREADEN .N(KFILL1.NMAYREAD) (32B02)

S/TR = SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: OA reg to LR reg. (31A30)

TRS120: [NKAB] = KAA (25A46) (31A26)
[SAB.KAA] = PATH6 (26B14)
OA reg + 1
RK reg + 1

TRS220: NANOTHER (25A02) (31A29)

TRL230: [PATH6] = MODE6 (13C01) (32A02)
RB0-7 to KA0-7
RC0-7 to KB0-7
RD0-7 to KC0-7
[KBB] = KAB (24B10)
[KCB] = KBB (24B27)
[KDB] = KCB (24B11)
[BCC1+BCC2+BCC3] = KDB (24B25)

TRS290: [NANOTHER] = NRAM (31A05)

[KDB] = KFILL1 (30A21)

[NKDB.NEMPTY.SREADEN] = SREAD (32B02)

S/TR = SREAD.CYCLE (32A15) (32B02) (30A35)

TRS030: READ (30A01) (31A34)

TRS060: OA reg to LR reg. (31A30) [RAB] = SAA (25B45)

TRS120: [KAB.KBB.KCB] = KAD (25A45) (31A26)
[SAA.KAD] = PATH5 (26B34)
OA reg + 1
RK reg + 1
[KAD.RBB] = ANOTHER (26C33)

TRL230: [PATH5] = MODE5 (20A25) (32A02)
RA0-7 to KD0-7
KDB (24B25)

TRS290: [KDB] = KFILL1 (30A21) (31A05)
[ANOTHER] = OA reg - 1
RK reg - 1
RAM (22A21)
grounds RAB

To FM24A

FM31A (5B12)
FM32A (5B07)
FM33A (5B02)
FM34A (5B01)
} SEE ORDER OUT

FM41A

FM41A

Data In DX4 continued

FM41A (5B42)

S/TM = RS (14E27)
(5C15)

TMA000/1 : NIOXO (16F02)
(4C02) ..... drops to clear IO reg.

TMA000 : ES (11E09)
(23A28)

TMA160 : FM41B (4A39)
(23A22) [STZBC1] = IOAO (21E23)
interrupt
[ZBC1.NFLDC] = IOA1 (21E19)
count done
[STIOPH] = IA03 (21E12)
IOP halt
[ZBC1.NFLDC.NEMPTY] = STIL (4A26)
incorrect length

TMB040: [CHAIN.NSTIOPH] = NFLXO (14B33)
(24C33)

TMB120 : RSA (11E03)
(3C05)

TMB160 : [CHAIN.NSTIOPH] = FLXM (20C45)
(3C18)

MA0 →	FLDC	(9D21)
MA1 →	FLIZC	(9D46)
MA2 →	FLCC	(9D09)
MA3 →	FLICE	(9D07)
MA4 →	FLHTE	(9D02)
MA5 →	FLIVE	(9D01)
MA6 →	FLSIL	(9D39)
MA7 →	FLSKIP	(9D42)

TMB240-3: FIOIA (13F34)
(23A03)

RS (14E27)
ES (11E09)
IOA0 (21E23)
IOA1 (21E19)
IOA3 (21E12)
RSA (11E03)

Device Controller Interface

Page 3-192

Data Out. DX1 (SIOP)

FI01A (13F34)
FM01A (5B39) } SEE SERVICE CONNECTION

FI11A (2E03)

S/TI = RS (14E27)
(5D15)

TIS000: [IR.FGAIO + FGHIO.MYNUM] = ED (21E33)
(4D02) NEND1
NEND2 } remember ED
NEND3

TIS160: FI11B (4E27)
(4D26) NFNCASC (16F26)
[EDI] = ED (21E33)
[IOIR] = OUT (9F39)
[OUT.NOKD] = DO (14E09)
data out.
SERVICE1 (13F27)

TIS320: FM21A (5B26)
(4D29)

TIS560: FI12A (1E23)
(4D04)

RS (14E27)
NDOR
IOR (14E34)
EDI (21E34)
ED (21E33)

Device Controller Interface.

NZBC1 + data chained

FM21A (5B26)

Preset during Order Out { NHFM21022A (10A01)
MAYWRITF (29A27)
NJFILL (29A22)
IA reg. to all 0's
0A reg. to all C's
RK reg. to all 1's
EMPTY (15B17)
SPACE (10A02)

S/TM = NHFM21022A.NMRQ + END2
(15C15) (10A01) (19C36) (9B27)

Data from Memory to IO reg.

TMA000/1: NWBXO (12B45)
(4C02) drops to clear WBA-D
NSXO (5F01)
drops to clear S reg.
[NEND2] = BCNT (30F35)
allows memory access

TMA000: SXBA (3D18)
(23A28) BA reg. to S reg.
WBSET (10B35)
set up WBA-D
[NBA17.NBA18] = WBA (29C26)
[+NBA17.BA18
+NBA17.NBA18.NBCC1] = WBB (29C27)
[+BA17.NBA18
+NBA17.BA18.NBCC1
+NBA17.NBA18.NBCC1.NBCC2] = WBC (29C12)
[+BA17.BA18
+NBA17.NBA18.NBCC1
+NBA17.BA18.NBCC1.NBCC2
+NBA17.NBA18.NBCC1.NBCC2.NBCC3] = WBD (29C14)
NMRQ1

TMA120: [END2] = END3 (16B24)
(3C41) remembers ED

[AR] = NMRQ (19C36)
[DG] = MXM (16E46)
[PE] = MPE (16C02)

MRQ (13D01)
AR (13D08)
DG (13D38)
PE (13D13)

Memory Interface.

TMS140: NMWXO (12A10)
(4C03) drops to clear MWA-D for read
[BCNT.NFLSKIP] = MRQ (13D01)
memory request
[BCNT] = BA reg. + # of bytes used from Mreg
BC reg. - # of bytes used from Mreg.

TMA160: FM21B (3B46)
(23A20) [BCNT] = MRQ1 (15C02)
remembers memory request

TMB000: NBCNT (19C19)
(23A14)

TMB080: [MRQ.NAH] = STMAE (4A07)
(3C19) ST10PH (4A09)

TMS140: NMLXO (12A17), NMUXO (12A18)
(4C03) dropped to clear Mreg.
NHXO (13B33)
drops to clear HA-D

TMB160: HXWB (10B10)
(3C18) WBA-D to HA-D
[if BC reg = 0] = ZBC1 (15C44)
zero byte count

TMB240: [NEND3.NSTMAE] = FM22A (5B09)
(23A01) [STMAE + END3] = FM41A (5B42)

STMAE + END3

FM22A (5B09)

S/TM = NMRQ
(5C15) (19C36)

TMA160: FM22B (3B09)
(23A20) [MRQ1] = JFILLSET (25A01)
to set up Jreg.

TMB000: [JFILLSET] = NJXO (9C01)
(23A14) drops to clear J reg.
JBXH (3A39)
HA-D to JA8-DB

TMB040: [JFILLSET.HA] = JXM-A (2A01)
(24C33) MA0-7 to JA0-7
[JFILLSET.HB] = JXM-B (2A02)
MB0-7 to JB0-7
[JFILLSET.HC] = JXM-C (2A10)
MC0-7 to JC0-7
[JFILLSET.HD] = JXM-D (2A09)
MD0-7 to JD0-7

TMB080: [JFILLSET] = JFILL (24B15)
(3C19) J reg is filled.

TMB160; HFM21022A (9A23)
(3C18) [END1] = END2 (9B27)
remembers ED.

TMB240: [NZBC1] = FM21A (5B26)
(23A01) [ZBC1.FLDC] = FM31A (5B12)
[ZBC1.NFLDC] = FM41A (5B42)

ZBC1.NFLDC

ZBC1.FLDC

NZBC1

WRITE into Fast Memory.

SWRITE = JFILL.RKO
(32B18) (24B15) (31C33)

S/TR = SWRITE.CYCLE
(32A15) (32B18) (30A35)

[JA8]
RAXJA (30C47)
JA0-8 to W/RA0-8

TRS030: WRITE (25B26)
(31A34)

TRS060: IA reg. to LA reg.
(31A30)

TRS120: IA reg +1
(31A26) RK reg. -1
RJA8 (21B26)
drops JA8

TRL150: W/RA0-0 to RA0-8
(32A21)

[NJA8.JB8]
RAXJB (28B13)
JB0-8 to W/RA0-8

TRS030: WRITE (25B26)
(31A34)

TRS060: IA reg. to LA reg.
(31A30)

TRS120: IA reg +1
(31A26) RK reg. -1
RJB8 (21B27)
drops JB8

TRL150: W/RA0-8 to RA0-8
(32A21)

[NJA8.NJB8.JC8]
RAXJC (28B02)
JC0-8 to W/RA0-8

TRS030: WRITE (25B26)
(31A34)

TRS060: IA reg to LA reg.
(31A30)

TRS120: IA reg. +1
(31A26) RK reg. -1
RJC8 (21B12)
drops JC8

TRL150: W/RA0-8 to RA0-8
(32A21)

[NJA8.NJB8.NJC8.JD8]
RAXJD (28B46)
JD0-8 to W/RA0-8

TRS030: WRITE (25B26)
(31A34)

TRS060: IA reg. to LA reg.
(31A30)

TRS120: IA reg. +1
(31A26) RK reg. -1
RJD8 (21B14)
drops JD8

TRL150: W/R0-8 to RA0-8
(32A21)

[JB8] [JC8] [JD8] [NJDB]
[NJB8] [NJC8] [NJD8]

NJFILL (29A22)

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FI12A
FM41A
FM31A

READ from FAM.

data chained.

FM31A
FM41A
FI12A
Data Flow
FM21A

Data Out DX1 continued.

READ from Fast Memory

[00+FI12A.TIS080] = NKAB (22A02)
NKBB (22A01)
NKCB (22A39)
NKDB (22A42)

SREAD = NKDB.NEMPTY
(32B02) (22A42) (18C34)

S/TR = SREAD.CYCLE
(32A15) (32B02) (30A35)

TRS030 : READ (30A01)
(31A34)

TRS060 : OAreg to LR reg.
(31A30) SAA (25B45)

TRS120 : KAA (25A46)
(31A26) [SAA.KAA] = PATHO (26B37)
OAreq+1
RKreq+1
[NJFILL + (RK count > 11))] = SPACE (10A02)

TRL230 : [PATHO] = MODEO (13C17)
(32A02) RA0-7 to KA0-7
KDB (24B25)

TRS290 : [KDB] = KFILL1 (30A21)
(31A05) [SPACE] = NHFM21022A (10A01)

FI12A (1E23)

S/TI = RS (KFILL1+ZBCOT15.EMPTY+STIOPH)
(5D15)

TIS000/1: NIOXO (16F02)
(4D02) drops to clear IO reg.
[+STIOPH
+(IR.FGAIO + FGHIO.MYNUM)
+ZBCOT15.FLDC.NFAST.EMPTY
+ZBCOT15.NFLDC.EMPTY.FM41A] = EDO (21E33)

TIS000/2: IOXK (29F28)
(4D34) KA0-7 to IOA0-7

TIS080: NKFILL1 (30A21)
(4D30) NKAB (22A02)
NKBB (22A01)
NKCB (22A39)
NKDB (22A42)
starts Fast Memory read cycle.

TIS160 : FI12B (4E12)
(4D26) KXO (30C24)
clears K reg.
[EDI] = ED (21E33)

TIS400 : [NED] = RSA (11E03)
(4D17)

TIS480: [ED] = RSA (11E03)
(4D07) [ED.RSA] = NSERVICE1 (13F27)

TIS560 : [ED] = END1 (9B26)
(4D04) [NSPACE.END1] = END2 (9B27)
[NED] = FI12A (1E23)

RS (14E27)
EDI (21E34)
ED (21E33)
IOA0 (21E23)
IOA1 (21E19)
IOA2 (21E15)
IOA3 (21E12)
IOA4 (21E03)
IOA5 (21E09)
IOA6 (21E01)
IOA7 (21E02)
IOAPOUT (21E25)
RSA (11E03)

NED
NKDB

ZBC1.FLDC

FM31A (5B12)
FM32A (5B07)
FM33A (5B02)
FM34A (5B01)
} SEE ORDER OUT

ZBC1.NFLDC
NEND3.NSTIOPH.N (FLIZC.NFAST)

FM41A (5B42)

S/TM = RS
(5C15) (14E27)

TMA000/1: NIOXO (16F02)
(4C02) drops to clear IO reg.
[MPE]: STTME (4A46)
transmission memory error.
DATAERR (9A30)
[ZBCOT15.FLIZC] = STZBCI (4E02)

TMA000-3: ES (11E09)
(23A28)

TMA080 : [DATAERR.FLHTE] = STIOPH (4A09)
(3C36)

TMA160 : FM41B (4A39)
(23A22) [STZBCI] = IOA0 (21E23)
Interrupt
[ZBCOT15] = IOA1 (21E19)
Count done
[STIOPH] = IOA3 (21E12)
IOP halt

TMB040: [CHAIN.NSTIOPH] = NFLXO (1MB33)
(24C33) drops to clear flags

TMB120: RSA (11E03)
(3C05)

TMB160 : [CHAIN.NSTIOPH] = FLXM (20C45)
(3C18) MA0 → FLDC (9D21)
MA1 → FLIZC (9D46)
MA2 → FLCC (9D09)
MA3 → FLICE (9D07)
MA4 → FLHTE (9D02)
MA5 → FLIVE (9D01)
MA6 → FLSIL (9D39)
MA7 → FLSKIP (9D42)

TMB240-3 = FI01A (13F34)
(23A03)

RS (14E27)
ES (11E09)
IOA0 (21E23)
IOA3 (21E12)
RSA (11E03)

Device Controller Interface

Data Out DX4 (SIOP)

FI01A (13F34)
FM01A (5B39) } SEE SERVICE CONNECTION

FM11A (2E03)

S/TI = RS (14E27)
(5D15)

TIS000: [IR.FGAIO+FGHIO.MVNUM] = ED (21E33)
(4D02) NEND1
NEND2 } remember ED
NEND3

TIS160: FI11B (4E27)
(4D26) NFNCASC (16F26)
[EDI] = ED (21E33)
[IOR] = OUT (9F39)
[OUT.NORD] = DO (4EC9)
data out
SERVICE1 (13F27)

TIS320: FM21A (5B26)
(4D39)

TIS560: FI12A (1E23)
(4D04)

RS (14E27)
NDOR
IOR (14E34)
EDI (21E34)
ED (21E33)
D.C. Interface

NEND3.NZBC1.NSTMAE

FM21A (5B26)

Preset during Order Out
- NHFM21022A (10A01)
- MAYWRITE (29A27)
- NJFILL (29A22)
- IA reg. to all 0's
- OA reg. to all 0's
- RK reg. to all 1's
- EMPTY (15B17)
- SPACE (10A02)

S/TM = NHFM21022A.NMRQ + END2
(5C15) (10A01) (19C36) (9B27)

One way of Data Flow

TMA000/1: NWBX0 (12B45)
(4C02) drops to clear WBA-D
NSX0 (5F01)
drops to clear Sreg.
[NZBC2.NEND2.MAYWRITE] = BCNT (30F35)
allows memory access

TMA000: SXBA (3D18)
(23A28) BA reg. to Sreg.
WBSET (10B35)
sets up WBA-D
[NBA17.NBA18] = WBA (29C26)
[+NBA17.BA18 / +NBA17.NBA18.NBCC1] = WBB (29C27)
[+BA17.NBA18 / +NBA17.BA18.NBCC1 / +NBA17.NBA18.NBCC1.NBCC2] = WBC (29C12)
[+BA17.BA18 / +BA17.NBA18.NBCC1 / +NBA17.BA18.NBCC1.NBCC2 / +NBA17.NBA18.NBCC1.NBCC2.NBCC3] = WBD (29C14)
NMRQ1

TMA120: [END2] = END3 (16B24)
(3C41) remembers ED

TMS140: NMWX0 (12A10)
(4C03) drops to clear MWA-D for read
[BCNT.NFLSKIP] = MRQ (13D01)
memory request
[BCNT] = BA reg. + # of bytes used from Mreg.
BC reg. − # of bytes used from Mreg.

MRQ (13D01)

TMA160: FM21B (3B46)
(23A20) [BCNT] = MRQ1 (15C02)
remembers MRQ
[MRQ2] = JFILLSET (25A01)
to set up Jreg.

TMA240: [NBNCT.NSHARE] = HFM21022A (9A23)
(3C35) [HFM21022A.END1] = END2 (9B27)
remembers ED

TMB000: [JFILLSET] = NJX0 (9C01)
(23A14) drops to clear Jreg.
JBXH (3A39)
HA-D to JA8-D8
[NSPACE] = NMAYWRITE
NBCNT (19C19)

TMB040: [JFILLSET.HA] = JXM-A (2A01)
(24C33) MA0-7 to JA0-7
[JFILLSET.HB] = JXM-B (2A02)
MB0-7 to JB0-7
[JFILLSET.HC] = JXM-C (2A10)
MC0-7 to JC0-7
[JFILLSET.HD] = JXM-D (2AC9)
MD0-7 to JD0-7

TMB080: [MRQ.NAH] = STMAE (4A07)
(3C19) STIOPH (4A09)
[JFILLSET] = JFILL (24B15)
Jreg is filled

TMS140: NMLX0 (12A17), NMUX0 (12A18)
(4C03) dropped to clear Mreg.
NHX0 (13B33)
drops to clear HA-D

TMB160: HXWB (10B10)
(3C18) WBA-D to HA-D
[if BC reg = 0] = ZBC1 (15C44)
zero byte count.

TMB240: [NEND3.NZBC2.NSTMAE] = FM22A (5B09)
(23A01) [NSTMAE.ZBC2.FLDC] = FM31A (5B12)
[STMAE+END3+ZBC2.NFLDC] = FM41A (5B42)

Another way of Data Flow

AR (13D08)
DG (15D38)
PE (13D13)

[AR] = NMRQ (19C36)
[DG] = MXM (16E46)
[PE] = MPE (16C02)

ZBC2.FLDC

ZBC2.NFLDC + END3 + STMAE

FM22A (5B09)

S/TM = NHFM21022A.NMRQ + END2
(5C15) (10A01) (19C36) (9B27)

TMA000/1: NWBX0 (12B45)
(4C02) drops to clear WBA-D
NSX0 (5F01)
drops to clear Sreg.
[MAYWRITE.NZBC1.NSHARE] = BCNT (30F35)
allows memory access

TMA000: SXBA (3D18)
(23A28) BA reg. to Sreg.
WBSET (10B35)
sets up WBA-D
[NBA17.NBA18] = WBA (29C26)
[+NBA17.BA18 / +NBA17.NBA18.NBCC1] = WBB (29C27)
[+BA17.NBA18 / +NBA17.BA18.NBCC1 / +NBA17.NBA18.NBCC2] = WBC (29C12)
[+BA17.BA18 / +BA17.NBA18.NBCC1 / +NBA17.BA18.NBCC1.NBCC2 / +NBA17.NBA18.NBCC1.NBCC2.NBCC3] = WBD (29C14)
NMRQ2 (19C44)

TMA120: [END2] = END3 (16B24)
(3C41) remembers ED

TMS140: NMWX0 (12A10)
(4C03) drops to clear MWA-D for read
[BCNT.NFLSKIP] = MRQ (13D01)
memory request
[BCNT] = BA reg. + # of bytes used from Mreg.
BC reg. − # of bytes used from Mreg.

MRQ (13D01)

TMA160: FM22B (3B09)
(23A20) [MRQ1] = JFILLSET (25A01)
to set up Jreg.
[BCNT] = MRQ2 (15C47)
remembers MRQ

TMA240: [NBCNT] = HFM21022A (9A23)
(3C35) [HFM21022A.END1] = END2 (9B27)
remembers ED

TMB000: [JFILLSET] = NJX0 (9C01)
(23A14) drops to clear Jreg.
JBXH (3A39)
HA-D to JA8-D8
[NSPACE] = NMAYWRITE
NBCNT (19C19)

TMB040: [JFILLSET.HA] = JXM-A (2A01)
(24C33) MA0-7 to JA0-7
[JFILLSET.HB] = JXM-B (2A02)
MB0-7 to JB0-7
[JFILLSET.HC] = JXM-C (2A10)
MC0-7 to JC0-7
[JFILLSET.HD] = JXM-D (2A09)
MD0-7 to JD0-7

TMB080: [MRQ.NAH] = STMAE (4A07)
(3C19) STIOPH (4A09)
[JFILLSET] = JFILL (24B15)
Jreg. is filled

TMS140: NMLX0 (12A17), NMUX0 (12A18)
(4C03) dropped to clear Mreg.
NHX0 (13B33)
drops to clear HA-D

TMB160: HXWB (10B10)
(3C18) WBA-D to HA-D
[if BC reg = 0] = ZBC2 (15C45)
zero byte count.

TMB240: [NEND3.NZBC1.NSTMAE] = FM21A (5B26)
(23A01) [NSTMAE.ZBC1.FLDC] = FM31A (5B12)
[STMAE+END3+ZBC1.NFLDC] = FM41A (5B42)

MRQ (13D01)

AR
DG
PE

[AR] = NMRQ (19C36)
[DG] = MXM (16E46)
[PE] = MPE (16E02)

ZBC1.FLDC

ZBC1.NFLDC + END3 + STMAE

FI02A

Memory Interface

FM41A
FM31A
FI12A

Data Out DX4 continued.

Data flow.

FM21A

WRITE into Fast Memory

SWRITE = JFILL . RKO
(32B18) (24B15) (31C33)

S/TR = SWRITE . CYCLE
(32A15) (32B18) (30A35)

JA0-8 to W/RA0-8
JB0-8 to W/RB0-8

TRS030: WRITE (25B26)
(31A34) NJFILL (29A22)

TRS060: IA reg. to LR reg.
(31A30)

TRS120: IA reg. +1
(31A26) RK reg. -1

TRL150: [JA8] = W/RA0-8 to RA0-8
(32A21) [JB8] = W/RB0-8 to RB0-8
[JC8] = JC0-8 to RC0-8
[JD8] = JD0-8 to RD0-8

TRS170: NJFILL (29A22)
(31A26)

NKDB

READ from Fast Memory.

[00+ FI12A.TIS080] = NKAA (22A02)
NKAB (22A01)
NKCA (22A39)
NKDA (22A42)

SREAD = NKDB . NEMPTY
(32B02) (22A42) (15C34)

S/TR = SREAD . CYCLE
(32A15) (32B02) (30A35)

TRS030: READ (30A01)
(31A34)

TRS060: OA reg. to LR reg.
(31A30) [NSPACE] = NMAYWRITE

[RAB] = SAA (25B45)

TRS120: [NKAB] = KAA (25A46)
(31A26) [KAA.SAA] = PATH0 (26B37)
OA reg. +1
RK reg. +1
[RK count > 9] = SPACE (10A02)

TRL230: [PATH0] = MODE0 (13C17)
(32A02) RA0-7 to KA0-7
RB0-7 to KB0-7
RC0-7 to KC0-7
RD0-7 to KD0-7
[RAB] = KAB (24B10)
[RBB] = KBB (24B27)
[RCB] = KCB (24B11)
[RDB] = KDB (24B25)

TRS250: [SPACE] = MAYWRITE
(31A07) (29A27)

TRS290: [SPACE] = NHFM21022A (10A01)
(31A05) [KDB] = KFILL1 (30A21)

[NRAB.RBB] = SAB (25B44)

TRS120: [NKAB] = KAA (25A46)
(31A26) [KAA.SAB] = PATH6 (26B14)
CA reg. +1
RK reg. +1
[RK count > 9] = SPACE (10A02)

TRS220: NANOTHER (25A02)
(31A29)

TRL230: [PATH6] = MODE6 (13C01)
(32A02) RB0-7 to KA0-7
RC0-7 to KB0-7
RD0-7 to KC0-7
[RBB] = KAB (24B10)
[RCB] = KBB (24B27)
[RDB] = KCB (24B11)

TRS250: [SPACE] = MAYWRITE
(31A07) (29A27)

TRS290: NRAM
(31A05) [SPACE] = NHFM21022A (10A01)

[NKDB.NEMPTY] = SREAD (32B02)
[SREAD.CYCLE] = S/TR (32A15)

TRS030: READ (30A01)
(31A34)

TRS060: OA reg. to LR reg.
(31A30) [RAB] = SAA (25B45)

TRS120: [KAB.KBB.KCB] = KAD (25A45)
(31A26) [KAD.SAA] = PATH5 (26B34)
CA reg +1
RK reg -1
[KAD.KBB] = ANOTHER (26C33)

TRL230: [PATH5] = MODE5 (20A25)
(32A02) RA0-7 to KD0-7
[RAB.PATH5] = KDB (24B25)

TRS290: [ANOTHER] = RAM (22A21)
(31A05) pulls down RAB
OA reg -1
RK reg -1
[KDB] = KFILL1 (30A21)

[NRAB.NRBB.RCB] = SAC (25B46)

TRS120: [NKAB] = KAA (25A46)
(31A26) [KAA.SAC] = PATH4 (26B18)
CA reg. +1
RK reg +1
[RK count > 9] = SPACE (10A02)

TRS220: NANOTHER (25A02)
(31A29)

TRL230: [PATH4] = MODE4 (20A28)
(32A02) RC0-7 to KA0-7
RD0-7 to KB0-7
[RCB] = KAB (24B10)
[RDB] = KBB (24B27)

TRS250: [SPACE] = MAYWRITE
(31A07) (29A27)

TRS290: NRAM
(31A05) NRBM1
[SPACE] = NHFM21022A (10A01)

[NKDB.NEMPTY] = SREAD (32B02)
[SREAD.CYCLE] = S/TR (32A15)

TRS030: READ (30A01)
(31A34)

TRS060: CA reg to LR reg.
(31A30) [RAB] = SAA (25B45)

TRS120: [KAB.KBB.NKCB] = KAC (25A44)
(31A26) [KAC.SAA] = PATH3 (26B35)
OA reg +1
RK reg +1
[KAC.RCB] = ANOTHER (26C33)

TRL230: [PATH3] = MODE3 (13C33)
(32A02) RA0-7 to KC0-7
RB0-7 to KD0-7
[RBB.PATH3] = KDB (24B25)

TRS290: [ANOTHER.PATH3] = RAM (22A21)
(31A05) pulls down RAB
RBM1 (22A46)
pulls down RBB
[ANOTHER] = OA reg. -1
RK reg. -1
[KDB] = KFILL1 (30A21)

[NRAB.NRBB.NRCB.RDB] = SAD (25B47)

TRS120: [NKAB] = KAA (25A46)
(31A26) [KAA.SAD] = PATH2 (26B13)
OA reg. +1
RK reg +1
[RK count > 9] = SPACE (10A02)

TRS220: NANOTHER (25A02)
(31A29)

TRL230: [PATH2] = MODE2 (20A34)
(32A02) RD0-7 to KA0-7
[RDB] = KAB (24B10)

TRS250: [SPACE] = MAYWRITE
(31A07)

TRS290: NRAM
(31A05) NRBM2
NRCM
[SPACE] = NHFM21022A (10A01)

[NKDB.NEMPTY] = SREAD (32B02)
[SREAD.CYCLE] = S/TR (32A15)

TRS030: READ (30A01)
(31A34)

TRS060: CA reg to LR reg.
(31A30) [RAB] = SAA (25B45)

TRS120: [KAB.NKBB] = KAB (25A47)
(31A26) [KAB.SAA] = PATH1 (26B33)
OA reg +1
RK reg +1
[KAB.RDB] = ANOTHER (26C33)

TRL230: [PATH1] = MODE1 (10B09)
(32A02) RA0-7 to KB0-7
RB0-7 to KC0-7
RC0-7 to KD0-7
[RCB] = KDB (24B25)

TRS290: [ANOTHER.PATH1] = RAM (22A21)
(31A05) pulls down RAB
RBM2 (22A09)
pulls down RBB
RCM (22A07)
pulls down RCB
[ANOTHER] = OA reg -1
RK reg -1
[KDB] = KFILL1 (30A21)

FI12A (1E23)

S/TI = RS (KFILL1 + ZBCOT15.EMPTY + STIOPH)
(5D15)

TIS000/1: NIOXO (16F02)
(4D02) drops to clear IO reg.
+ STIOPH
+ (IR.FGAIO + FGNIO.MYNUM)
+ ZBCOT15.FLDC.NFAST.EMPTY
+ ZBCOT15.NFLDC.FM41A.EMPTY
= ED (21E33)

TIS000/2: IOXK (29F28)
(4D34) Kreg to IO reg.

TIS080: NKFILL1 (30A21)
(4D30) NKAA (22A02)
NKAB (22A01)
NKCA (22A39)
NKDA (22A42)
starts Fast Memory read cycle

TIS160: FI12B (4E12)
(4D26) KXO (30C24)
clears Kreg.
[EDI] = ED (21E33)

TIS320: [NED] = RSA (11E03)
(4D29)

TIS480: [EO] = RSA (11E03)
(4D07) [ED.RSA] = NSERVICE1 (13F27)

TIS560: [EO] = END1 (9B26)
(4D04) [NSPACE.END1] = END2 (9B27)
[NED] = FI12A (1E23)

RS (4E22)
EDI (21E39)
ED (21E33)
IO reg.
RSA (11E03)

D.C. Interface.

NED

NKDB

ZBCOT15.FLDC

FM31A (5B12)
FM32A (5B07)
FM33A (5B02)
FM34A (5B01)
} SEE ORDER OUT

FLIZC.NFAST + END3 + STIOPH

NEND3.NSTIOPH.N(FLIZC.NFAST)

FM41A

FM4

Data Out **DX4** continued.

FM41A (5B42)

S/TM = RS (14E27)
(5C15)

TMA000/1: NIOXO (16F02)
(4C02) drops to clear IO reg.
[MPE]: STTME (4A46)
transmission memory error.
DATAERR (9A30)
[IBCOT15.FLIZC] = STIBCI (4E02)

TMA000-3: ES (11E09)
(23A28)

TMA080: [DATAERR.FLHTE] = STIOPH (4A09)
(3C36)

TMA160: FM41B (4A34)
(23A22) [STIBCI] = IOA0 (21E23)
Interrupt.
[IBCOT15] = IOA1 (21E19)
count done
[STIOPH] = IOA3 (21E12)
IOP halt

TMB040: [CHAIN.NSTIOPH] = NFLXO (14B33)
(24C33) drops to clear flags.

TMB120: RSA (11E03)
(3C05)

TMB160: [CHAIN.NSTIOPH] = FLXM (20C45)
(3C18)
MA0 → FLDC (9D21)
MA1 → FLIZC (9D46)
MA2 → FLCC (9D09)
MA3 → FLICE (9D07)
MA4 → FLHTE (9DC2)
MA5 → FLIUE (9D01)
MA6 → FLSIL (9D39)
MA7 → FLSKIP (9D42)

TMB240-3: FIO1A (13F34)
(23A03)

RS (14E27)
ES (11E09)
IOA0 (21E23)
IOA1 (21E19)
IOA3 (21E12)
RSA (11E03)
D.C. Interface

SIO (SIOP)

CPU Interface

CNSTR(10F20)
IOPA0R(10F08)
IOPA1R(10F13)
IOPA2R(10F18)
FNC0 (10F06)
FNC1 (10F09)
FNC2 (10F10)
PRD (10F45)

FI01A (13F34)

PRD = + STIOPB1. (SIOP is busy)
(10F45) + STI (Interrupt pending)
+ CNSTD.LAST (no address recognition)

S/TI = ME = (MYSIO.NSTIOPB1.NSTI)
(5D15) (10F22)

TIS000/2: FNCF (4E02)
(4D34) CPU function

TIS160 : FI01B (4E26)
(4D26)

TIS240 : FNCSIO (4E42)
(4D28) FSIO (11F36)

TIS560 : FM01A (5B39)
(4D04)

FSIO (11E12)

Access and use contents of Location 20

FM01A (5B39)

S/TM = FNCSIO
(5C15) (4E42)

TMA000/1: NSX0 (5F02)
(4C02) drops to clear S reg.

TMA000-3: S26 (8D23)
(23A28) set address to loc. 20

[AR] = NMRQ (19C36)
[DG] = MXM (16E46)
[POK] = MPR (16C01)
[PE] = MPE (16C02) → MPR (16C01)

TMS140: NMWX0 (16B23)
(4C03) drops to clear write byte lines
NMLX0 (12A05), NMUX0 (12A18)
dropped to clear Mreg.
MRQ (13D01)
Memory request
CACNTD (3D47)
CA reg. -1

TMA160: FM01B (3B26)
(23A20)

TMB240-2: FM11A (2B24)
(23A04)

MRQ (13D01)
AR (13D08)
DG (15D38)
POK (13D27)
PE (13D13)

Get and Store Even Status Word

FM11A (2B24)

S/TM = MPR
(5C15) (16C01)

TMA000/1: NIOX0-A (16F01)
(4C02) drops to clear IOA0-7

TMA000-3: IOXM (1D01)
(23A28) DC. address MA0-7 to IOA0-7

TMA080 : [MB1] = ORD (9E36)
(3C36) odd word status desired

TMA160-1: FM11B (3B27)
(23A23)

TMB000-3: [NMPE] = FSF (11E35)
(23A13) function strobe

TMB240-1: [MB0, NMPE] = FM12A (5B21)
(23A05) [NMB0+MPE] = FM13A (5B46)

[AV0] = NFS

IOA0 (22E37)
IOA1 (22E33)
IOA2 (22E34)
IOA3 (22E35)
IOA4 (22E18)
IOA5 (22E13)
IOA6 (22E14)
IOA7 (22E15)

FSF (11E35)
AV0 (9E08)
NFSF

MB0
NMB0 + MPE

FM12A (5B21)

S/TM = FM12A
(5C15) (5B21)

TMA000/1: NJX0 (9C01)
(4C02) drops to clear J reg.
WBA (29C26), WBB (29C27)
WBC (29C12), WBD (29C14)
for setting memory write byte lines

TMA000-1: JXCA (20A05)
(23A31) CA reg. to JA0-7 and JB0-7

[AR] = NMRQ (19C36)

TMS140 : NMUX0 (12A16)
(4C03) drops to clear MA0-7 and MB0-7
MRQ (13D01)
Memory request

TMA160 : MXKB-M (16C03)
(23A20) WBA-D to MWA-D
for memory write.
MUXJ (16E18)
JA0-7 and JB0-7 to MA0-7 and MB0-7
FM12B (3B12)

TMB240-2: FM13A (5B46)
(23A04)

MRQ (13D01)
AR (13D08)

Get and Store Odd Status Word

FM13A (5B46)

S/TM = NMRQ (FSL+NFS)
(5C15) (19C36) (12B12)

TMA000/1: NJX0 (9C01)
(4C02) drops to clear J reg.

TMA000-3: NCCX1 (15F13)
(23A28) drops to set CC1 CC2

TMS140 : CACNTU (8E30)
(4C03) CA reg. +1

[NCC1] = NCOND1D (10F25)
[NCC2] = NCOND2D (10F33)

TMA160 : FM13B (3B14)
(23A20) [DOR] = NCC1 (1E14)
[IOR] = NCC2 (1E22)
[NCC1.NCC2] = SUCCESS (12E33)
successful SIO
JAXFR (13C47)
FR0-7 to JA0-7

TMB000-3: NFSF
(23A13) [SUCCESS] = AXIO (12E12)
clock for IOA0-7 to A0-7
[WORD+MPE] = PRD (10F45)

TMS140 : [SUCCESS] = CAXM (22F01)
(4C03) MC0-7 and MD0-7 to CA reg.

TMB240-4 : FM14A (5B14)
(23A01)

FSL (14E36)
DOR (21E38)
IOR (14E34)
FR0 (14E22)
FR1 (14E20)
FR2 (14E18)
FR3 (14E13)
FR4 (14E08)
FR5 (14E10)
FR6 (14E04)
FR7 (14E06)

PRD (10F45)
NCOND1D (10F25)
NCOND2D (10F33)

FM14A (5B14)

S/TM = FM14A
(5C15) (5B14)

TMA000: S26 (8D23) S31 (8D30)
(23A28) set address to Loc. 21
JXST (2F02)
operational status to JB0-7
JXBC (20A16)
BC reg. to JC0-7 and JD0-7
WBA (29C26), WBB (29C27)
WBC (29C12), WBD (29C14)
for setting memory write byte lines

TMS140 : NMLX0 (12A05), NMUX0 (12A18)
(4C03) dropped to clear Mreg.
[ORD.NMPE] = MRQ (13D01)
memory request

[AR] = NMRQ (19C36)
[NMRQ] = PRD (10F45)

TMA160 : FM14B (3B21)
(23A20) MXKB-M (16C03)
WBA-D to MWA-D
for memory write
MLXJ (16F17), MUXJ (16E18)
Jreg. to Mreg.
[SUCCESS] = NSTX0 (1A35)
drops to clear status
NFLX0 (1W33)
drops to clear flags
STIOPB1 (6A24)
SIOP busy.

TMB000-3 : NFNCF (18F11)
(23A13)

TMB240-3: NFNCSIO
NFSIO
FI11A (13F34)

Clear Flags@Status

MRQ (13D01)
AR (13D08)
PRD (10F45)

NOTE: The TM delay line is started twice for every FM phase

Location 20 stored by CPU.

0–7	8	9	10–15	16–31
Device Address	0	0	0	Command Doubleword Address
	0	1		
	1	1		

0 0 = no status desired
0 1 = 1 word status desired
1 1 = 2 words status desired.

Location 20 stored by SIOP

0–15	16–31
Previous Command Doubleword Address	Present Command Doubleword Address.

Location 21 stored by SIOP

0–7	8–15	16–31
Device Status	Operational Status	Remaining Byte Count

Operational Status.

Bit
8 = STIL = Incorrect length
9 = STTDE = Transmission data error
10 = STTME = Transmission memory error.
11 = STMAE = Memory address error.
12 = STIOPME = IOP memory error.
13 = STIOPCE = IOP control error
14 = STIOPH = IOP halt
15 = STIOPBL = IOP busy.

Memory Interface.

Device Controller Interface

1989-3-1984

TIO, TDV (SIOP)

CPU Interface

CNSTR (10F20)
IOPAOR (10F08)
IOPA1R (10F13)
IOPA2R (10F18)
FNC0 (10F06)
FNC1 (10F04)
FNC2 (10F10)
PRD (10F45)

FIO1A (13F34)

PRD = +SERVICE1.MYTEST (10F45) + CNSTD.LAST (service call in progress) (no address recognition)

S/TI = ME = (MYTEST.NSERVICE1) (SDIS) (10F22)

TIS000: FNCF (4E02) (4D34) CPU function.

TIS160: FIO1B (4E26) (4D26)

TIS240: [NFNC0.NFNC1.FNC2] = FTIO (11E19) [NFNC0.FNC1.NFNC2] = FTDV (11E23) (4D28)

TIS160: FMO1A (5B39) (4D04)

FTIO (11E19) + FTDV (11E23)

Access and use contents of location 20

FMO1A (5B39)

S/TM = FNCF (4E02) (5C15)

TMA000/1: NSX0 (5F02) (4C02) drops to clear Sreg.

TMA000-3: S26 (8D23) (23A28) sets address to loc. 20

TMS140: NMWX0 (16B23) (4C03) drops to clear write byte lines NMLX0 (12A17), NMUX0 (12A18) dropped to clear Mreg. MRQ (13D01) memory request CACNTU (3D47) CA reg-1

TMA160: FMO1B (3B26) (23A20)

TMB240-2: FM11A (2B24) (23A04)

MRQ (13D01)
AR (13D08)
DG (15D38)
POK (13D27)
PE (13D13)

[AR] = NMRQ (19C36)
[DG] = MXM (16E46)
[POK] = MPR (16C01)
[PE] = MPE (16C02) → MPR (16C01)

Get and Store Even Status Word.

IOA0 (21E23)
IOA1 (21E19)
IOA2 (21E15)
IOA3 (21E12)
IOA4 (21E03)
IOA5 (21E09)
IOA6 (21E01)
IOA7 (21E02)

FM11A (2B24)

S/TM = MPR (16C01) (5C15)

TMA000/1: NIOX0-A (16F01) (4C02) drops to clear IOA0-7

TMA000-3: IOXM (1D01) (23A28) D.C. address, MA0-7 to IOA0-7

TMA080: [MB1] = ORD (9E36) (3C36) odd status word desired

TMA160-1: FM11B (3B27) (23A23)

TMB000-3: [NMPE] = FSF (11E35) (23A13) function strobe

TMB240-1: [MB0.NMPE] = FM12A (5B21) (23A05) [NMB0+MPE] = FM13A (5B46)

[AV0] = NFSF

FSF (11E35)
AV0 (9E08)
NFSF

MB0
NMB0

FM12A (5B21)

S/TM = FM12A (5B21) (5C15)

TMA000/1: NJX0 (9C01) (4C02) drops to clear Jreg. WBA (29C26), WBB (29C27) WBC (29C12), WBD (29C14) for setting memory write byte lines.

TMA000-1: JXCA (20A05) (23A31) CA reg to JA0-7 @ JB0-7

[AR] = NMRQ (19C36)

TMS140: NMUX0 (12A18) (4C03) drops to clear MA0-7 @ MB0-7 MRQ (13D01) memory request.

TMA160: MXKB-M (16C03) (23A20) WBA-D to MWA-D for memory write MUXJ (16E18) JA0-7 @ JB0-7 to MA0-7 @ MB0-7 FM12B (3B12)

TMB240-2: FM13A (5B46) (23A04)

MRQ (13D01)
AR (13D08)

Get and Store Odd Status Word.

FM13A (5B46)

S/TM = NMRQ. (FSL+NFS) (5C15) (19C36) (12B12)

TMA000/1: NJX0 (9C01) (4C02) Drops to clear Jreg.

TMA000-3: NCCX1 (15F13) (23A28) Drops to set CC1, CC2

TMS140: CACNTU (8E30) (4C03) CA reg.+1

[NCC1] = NCOND1D (10F25)
[NCC2] = NCOND2D (10F33)

TMA160: FM13B (3B14) (23A20) [DOR] = NCC1 (1E14) [IOR] = NCC2 (1E22) JAXFR (13C47) FR0-7 to JA0-7

TMB000-3: NFSF (23A13) drop function strobe [NORD+MPE] = PRD (10F45)

TMB240-4: FM14A (5B14) (23A01)

PRD (10F45)
NCOND1D (10F25)
NCOND2D (10F33)

FSL (14E36)
DOR (21E38)
IOR (14E34)

FRC (14E22)
FR1 (14E20)
FR2 (14E18)
FR3 (14E13)
FR4 (14E08)
FR5 (14E10)
FR6 (14E04)
FR7 (14E06)

FM14A

S/TM = FM14A (5C15) (5B14)

TMA000: S26 (8D23), S31 (8D30) (23A28) sets address to loc 21 JXST (2E02) Status to JB0-7 JXBC (20A18) BC reg. to JC0-7 and JD0-7 WBA (29C26), WBB (29C27) WBC (29C12), WBD (29C14) for setting memory write byte lines

[AR] = NMRQ (19C36)
[NMRQ] = PRD (10F45)

TMS140: NMLX0 (12A05), NMUX0 (12A18) (4C03) Dropped to clear Mreg. [ORD.NMPE] = MRQ (13D01) Memory request

TMA160: FM14B (3B21) (23A20) MXKB-M (16C03) WBA-D to MWA-D for memory write. MLXJ (16E17), MUXJ (16E18) Jreg. to Mreg.

TMB000-3: NFNCF (18F11) (23A13) NFTIO NFTDV

TMB240-3: FIO1A (13F34) (23A03)

MRQ (13D01)
AR (13D08)

Memory Interface

Device Controller Interface

NOTE: The TM delay line is started twice for every FM phase.

Location 20 stored by CPU

0 ... 7	8	9	10 ... 31
Device Status	0	0	0 ... 0
	0	1	
	1	1	

0 0 = no status desired.
0 1 = 1 word status desired
1 1 = 2 words status desired.

Location 20 stored by SIOP

0 ... 15	16 ... 31
Previous Command Doubleword Address	0 ... 0

Location 21 stored by SIOP

0 ... 7	8 ... 15	16 ... 31
TIO/Device Status TDV/Status Unique to device	Operational Status	Remaining Byte Count.

Operational Status.

Bit
8 = STIL = Incorrect length
9 = STTDE = Transmission data error.
10 = STTME = Transmission memory error
11 = STMAE = Memory address error
12 = STIOPME = IOP memory error
13 = STIOPCE = IOP control error.
14 = STIOPH = IOP halt
15 = STIOPBI = IOP busy

HIO (SIOP)

CPU Interface

FIO1A (13F34)

PRD = CNSTD.LAST (10E30)
FGHIO = NFNCO, FNC1, FNC2
[FGHIO.MYNUM] = ED (21E33)
ME (10F22)

S/TI = ME (10F22) (5D15)

TIS000/2: FNCF (4E02) (4D34) CPU function.

TIS160: FIO1B (4E26) (4D26)

TIS240: FHIO (11F41) (4D28)

TIS560: FM01A (5B39) (4D04)

CNSTR (10F20)
IOPA0R (10F08)
IOPA1R (10F13)
IOPA2R (10F18)
FNC0 (10F06)
FNC1 (10F04)
FNC2 (10F10)
PRD (10FH5)

FHIO (11E15)

FM01A (5B39)

Access and dispose of Location 20

S/TM = FNCF (4E02) (5C15)

TMA000/1: NSX0 (5F02) (4C02) drops to clear Sreg.

TMA000-3: S26 (8D23) (23A28) sets address to loc. 20

[AR] = NMRQ (14C36)
[DG] = MXM (16E46)
[POK] = MPR (16C01)
[PE] = MPE (16C02) → MPR (16C01)

TMS140: NMWX0 (16B23) (4C03) drops to clear write byte lines
NMLX0 (12A17), NMUX0 (12A18) dropped to clear Mreg.
MRQ (13D01) memory request
CACNTD (3D47) CAreg -1

TMA160: FM01B (3B26) (23A20)

TMB240-2: FM11A (2B24) (23A04)

MRQ (13D01)
AR (13D08)
DG (15D30)
POK (13D27)
PE (13D13)

Get and Store Even Status Word

FM11A (2B24)

S/TM = MPR (5C15) (16C01)

TMA000/1: NIOX0-A (16F01) (4C02) drops to clear IOA0-7

TMA000-3: IOXM (1D01) (23A28) D.C. address, MA0-7 to IOA0-7
[if IOA0-7 = A0-7] = MATCH (19F46)
[MATCH.FGHIO] = USEFULHIO (20C02)

TMA080: [MB1] = ORD (4E36) (3C36) odd status word desired.

TMA160-1: FM11B (3B27) (23A23)

TMB000-3: [NMPE] = FSF (11E35) (23A13) function strobe

TMB240-1: [MB0.NMPE] = FM12A (5B21) (23A05) [NMB0 + MPE] = FM13A (5B46)

[AV0] = NFSF

IOA0 (21E23)
IOA1 (21E19)
IOA2 (21E15)
IOA3 (21E12)
IOA4 (21E03)
IOA5 (21EC9)
IOA6 (21E01)
IOA7 (21EQ2)

FSF (11E35)
AV0 (9E08)
NFSF

FM12A (5B21)

S/TM = FM12A (5B21) (5C15)

TMA000/1: NJX0 (9C01) (4C02) drops to clear Jreg.
WBA (29C26), WBB (29C27)
WBC (29C12), WBD (29C14)
for setting memory write byte lines

TMA000-1: JXCA (20A05) (23A31) CAreg. to JA0-7 @ JB0-7

[AR] = NMRQ (19C36)

TMS140: NMUX0 (12A18) (4C03) drops to clear MA0-7 @ MB0-7
MRQ (13D01) memory request

TMA160: MXKB-M (16C03) (23A20) WBA-D to MWA-D for memory write
MUXJ (16E18) JA0-7 @ JB0-7 to MA0-7 @ MB0-7
FM12B (3B12)

TMB240-2: FM13A (5B46) (23A04)

MRQ (13D01)
AR (13D08)

Get and Store Odd Status Word

FM13A (5B46)

S/TM = NMRQ.(FSL + NFS) (5C15) (19C36) (12B12)

TMA000/1: NJX0 (9C01) (4C02) drops to clear Jreg.

TMA000-3: NCCX1 (15F13) (23A28) drops to set CC1 @ CC2

TMS140: CACNTU (8E30) (4C03) CAreg. +1

[NCC1] = NCOND1D (10F25)
[NCC2] = NCOND2D (10F33)

TMA160: FM13B (3B14) (23A20) [DOR] = NCC1 (1E14)
[IOR] = NCC2 (1E22)
JAXFR (13C47) FR0-7 to JA0-7

TMB000: NFSF (23A15) [NORD + MPE] = PRD (10F45)
[USEFULHIO] = NSTAX0 (5A13) drops to clear interrupt status
NSTZBCI
NSTCEI
NSTUEI

TMB240-4: FM14A (5B14) (23A01)

PRD (10F45)
NCOND1D (10F25)
NCOND2D (10F33)

FSL (14E36)
DOR (21E38)
IOR (14E34)

FR0 (14E22)
FR1 (14E20)
FR2 (14E18)
FR3 (14E13)
FR4 (14E08)
FR5 (14E10)
FR6 (14E09)
FR7 (14E06)

FM14A (5B14)

S/TM = FM14A (5C15) (5B14)

TMA000: S26 (8D23), S31 (8D3) (23A28) sets address to loc. 21
JXST (2E02) status to JR0-7
JXBC (20A18) Breg. to JC0-7 (8) JD0-7
WBA (29C26), WBB (29C27)
WBC (29C12), WBD (29C14)
for setting memory write byte lines.
NIR (5E26)

[AA] = NMRQ (19C36)
[NMRQ] = PRD (10F45)

TMS140: NMLX0 (12A17), NMUX0 (12A18) (4C03) dropped to clear Mreg.
[ORD.NMPE] = MRQ (13D01) memory request.

TMA160: FM14B (3B21) (23A20) MXKB-M (16C03)
WBA-D to MWA-D for memory write.
MUXJ (16E18), MUXK (15E15) Jreg. to Mreg.
[USEFULHIO] = NSTIOPB1 (13F35)

TMB000-3: NFNCF (18F11) (23A13) NFHIO

TMB240-3: FIO1A (13F34) (23A03)

MRQ (13D01)
AR (13D08)
PRD (10F45)

Memory Interface.

Device Controller Interface.

Note: The TM delay line is started twice for every FM phase.

Location 20 stored by CPU

0 ... 7	8	9	10 ... 31
Device Status	0	0	0 ... 0
	0	1	
	1	1	

0 0 = no status desired
0 1 = 1 word status desired.
1 1 = 2 words status desired.

Location 20 stored by SIOP

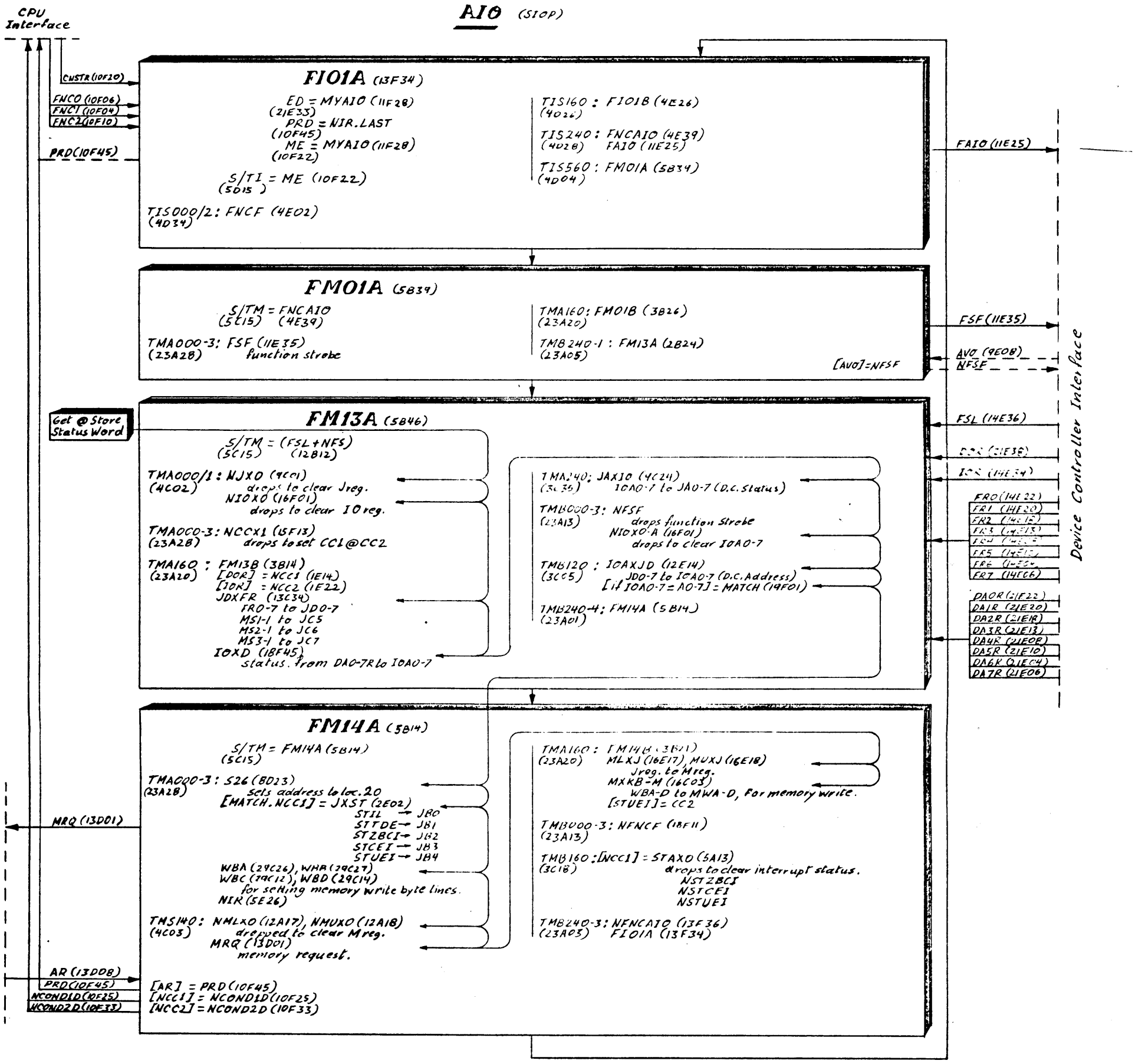
0 ... 15	16 ... 31
Previous Command Doubleword Address	0 ... 0

Location 21 stored by SIOP

0 ... 7	8 ... 15	16 ... 31
Device Status	Operational Status	Remaining Byte Count.

Operational Status:
Bit
8 = STIL
9 = STTDE
10 = STTME
11 = STTMAE
12 = STIOPME
13 = STIOPCE
14 = STIOPH
15 = STIOPB1

Page 3-200/3-200A



Location 20 stored by SIOP.

0 ← 7	8 9	10 ← 12	13 ← 20	21 ← 23	24 ← 31
Status Unique to device	Oper. Status	Interrupt Status	0 ← 0	SIOP Number	Device Controller Address

Operational Status

Bit 8 = STIL : Incorrect length
9 = STTDE : Transmission data error

Interrupt Status

Bit 10 = STZBCI = zero byte count interrupt
11 = STCEI = channel end interrupt
12 = STUEI = unusual end interrupt.

MEMORY

8265/8465

Σ5/7 or 6 MATRIX 1 & 2

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	ZT 46	ZT 46	ZT 46	FT 79	FT 79	FT 83	XT 10	AT 60 L29 ↓ L31		AT 60 M15 ↓ M27	FT 83	BT 36	AT 60 L29 ↓ L31 3	BT 36	AT 60 M15 ↓ M27 3	XT 10	IT 16	AT 60 M15 ↓ M27 2	BT 36	AT 60 L29 ↓ L31 2	BT 36	FT 83	AT 60 M15 ↓ M27		AT 60 L29 ↓ L31	XT 10	FT 83 M32B	FT 79 M16B ↓ M33B	FT 79 M00B ↓ M07B	ZT 46 TO BANK 'B' 30A	ZT 46 31A	ZT 46 32A	A
	TO BANK 'A' 30A	31A	32A	M00A ↓ M07A	M16A ↓ M23A	M32A																											
B	FT 79	FT 79	FT 79	FT 79	FT 79	FT 82	AT 60 MQ		AT 60 M00 ↓ M13 4		BT 15	AT 60 MQ 3	BT 36	AT 60 M00 ↓ M13 3	BT 36	BT 36	BT 36	BT 36	AT 60 M00 ↓ M13 2	BT 36	AT 60 MQ 2	BT 16	IT 16	AT 60 M00 ↓ M13		AT 60 MQ 1	FT 82	FT 79 M24B ↓ M31B	FT 79 M00B ↓ M15B	FT 79 ← L REG. B →	FT 79	FT 79	B
	← L REG. A →			M08A ↓ M15A	M24A ↓ M31A																												
C	ZT 45 XT10	ST 49 1A	XT10	ST 49 1B	LT 106 P4: AHA	AT 10 L15 ↓ L28 4	LT 106 P4: AHB	AT 75 PORT SEL. MATRIX A	AT 75 PORT SEL. MATRIX B	LT 106 P3: AHA	AT 10 L15 ↓ L28 3	LT 106 P3: AHB	ST 49 2A		ST 49 2B			ST 49 3A	FT 66 AH	ST 49 3B	LT 106 P2: AHA	AT 10 L15 ↓ L28 2	LT 106 P2: AHB	AT 75 PORT SEL. MATRIX A	AT 75 B	LT 106 P1: AHA	AT 10 L15 ↓ L28 1	LT 106 P1: AHB	ST 49 4A	ZT 45 XT10	ST 49 4B	XT10	C
																																S1	
D		ZT 46 TO BANK 'A' 31B	ZT 46 32B	FT 79	FT 79	FT 83	XT 10	AT 60		AT 60	FT 83	BT 36	AT 60 7	BT 36	AT 60 7	XT 10	IT 16	AT 60 6	BT 36	AT 60 6	BT 36	FT 83	AT 60		AT 60	XT 10 *	FT 83 *	FT 79 *	FT 79 *	*	ZT 46 * TO BANK 'B' 31B	ZT 46 * 32B	S2
E	FT 79	FT 79	FT 79	FT 79	FT 79	FT 82	AT 60		AT 60 8		BT 15	AT 60 7	BT 36	AT 60 7	BT 36	BT 36	BT 36	BT 36	AT 60 6	BT 36	AT 60 6	BT 16	IT 16	AT 60		AT 60 5	FT 82	FT 79 *	FT 79 *	FT 79 *	FT 79 *	FT 79 *	A
L	XT 10	ST 49 3A	XT 10	ST 49 5B	LT 106 9	AT 10 8	LT 106 9	AT 75	AT 75 *	LT 106 9	AT 10 7	LT 106 9	ST 49 6A		ST 49 6B			ST 49 7A	FT 66	ST 49 7B	LT 106 9	AT 10 6	LT 106 9	AT 75	AT 75 *	LT 106 9	AT 10 5	LT 106 * 9	ST 49 8A	XT 10 *	ST 49 8B	XT 10 *	B
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	C

Page 3-202

1-8 = PORT INTERFACE CABLES

* = REMOVE IF NO 'B' BANK S1 OR S2

1A-8A = STARTING ADD. SW's 'A' BANK

1B-8B = STARTING ADD. SW's 'B' BANK

9 = REMOVE IF RESPECTIVE PORT NOT IMP. ALSO APPLIES TO S1 MATRIX

ST49

64K	L15	STARTING ADDRESS's
32K	L16	
16K	L17	
8K	L18	
	INHP	PORT DISABLE
	BUSS PARITY	PORT CAN SEND OR RECEIVE M32
	CPU BUSS	ENABLES MF FROM DRIVER TO PE BUSS

SHEET 1 of 2

10/20/70

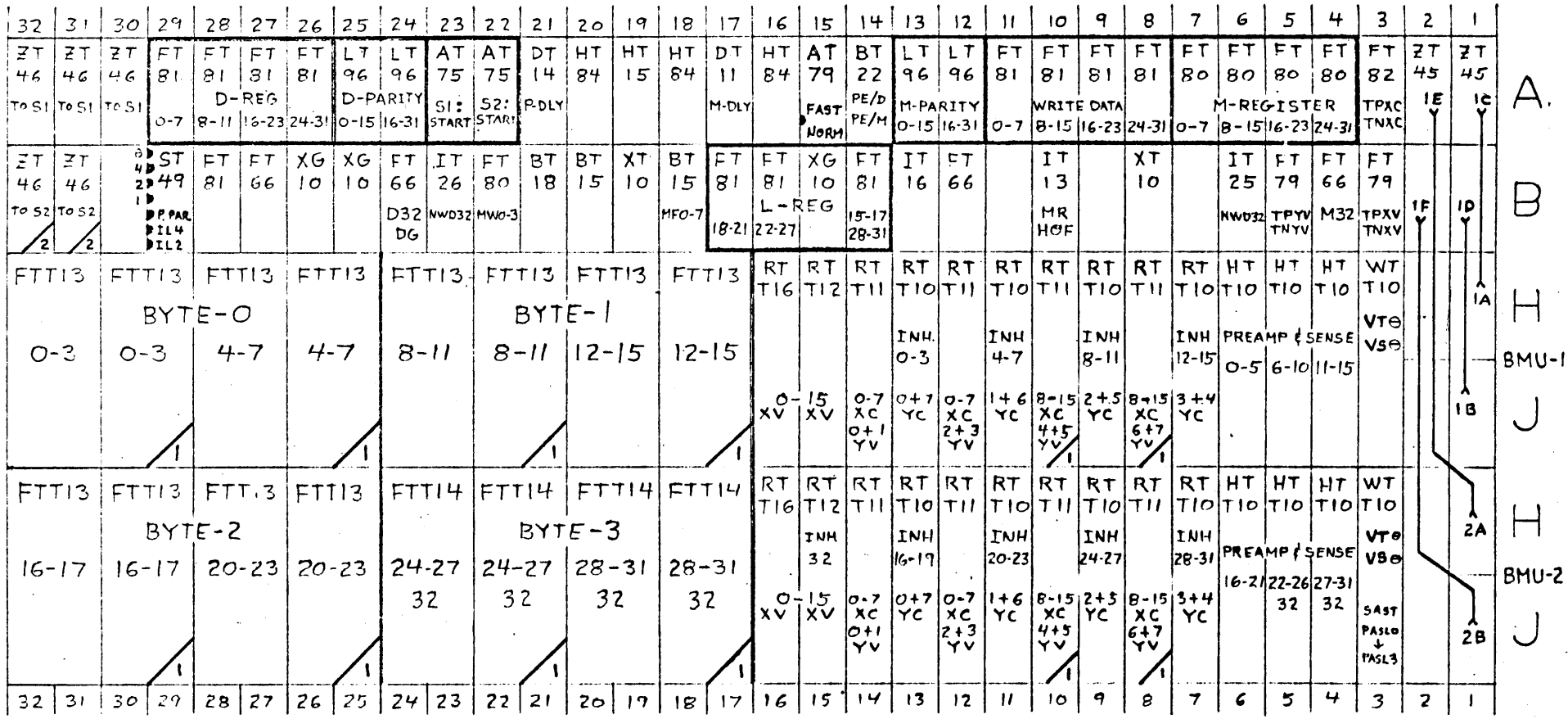
COCHRANE

MEMORY

8265/8465.

Σ5/7 OR 6 DRIVER & BMU's BANK 'A' OR 'B'

GND 10B38 TO CHANGE TO Σ6 TIMING



1 = 8 TO 16K OPTION

2 = S2 MATRIX OPTION

INTERLEAVE & DOOR SELECT IS DECODED IN MATRIX

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
	DOOR SEL.		XC YV	YC		YC		YV		YV		XC			XV			PREDRIVE DECODE
	S IN BMU																	
	L IN DRIVER																	

VD - 3H01 ≅ 21.5 V

VC - 3H45 = 24 V

VM - 3H46 ≅ VD/2 V

VT - 3H14 = .35 V

VS - 3H11 ≅ 4 V

VE - 3H18 = 14.4 ± .3 V

SAST - 3H22

ADJ. SAST BY VS POT, EACH BMU.

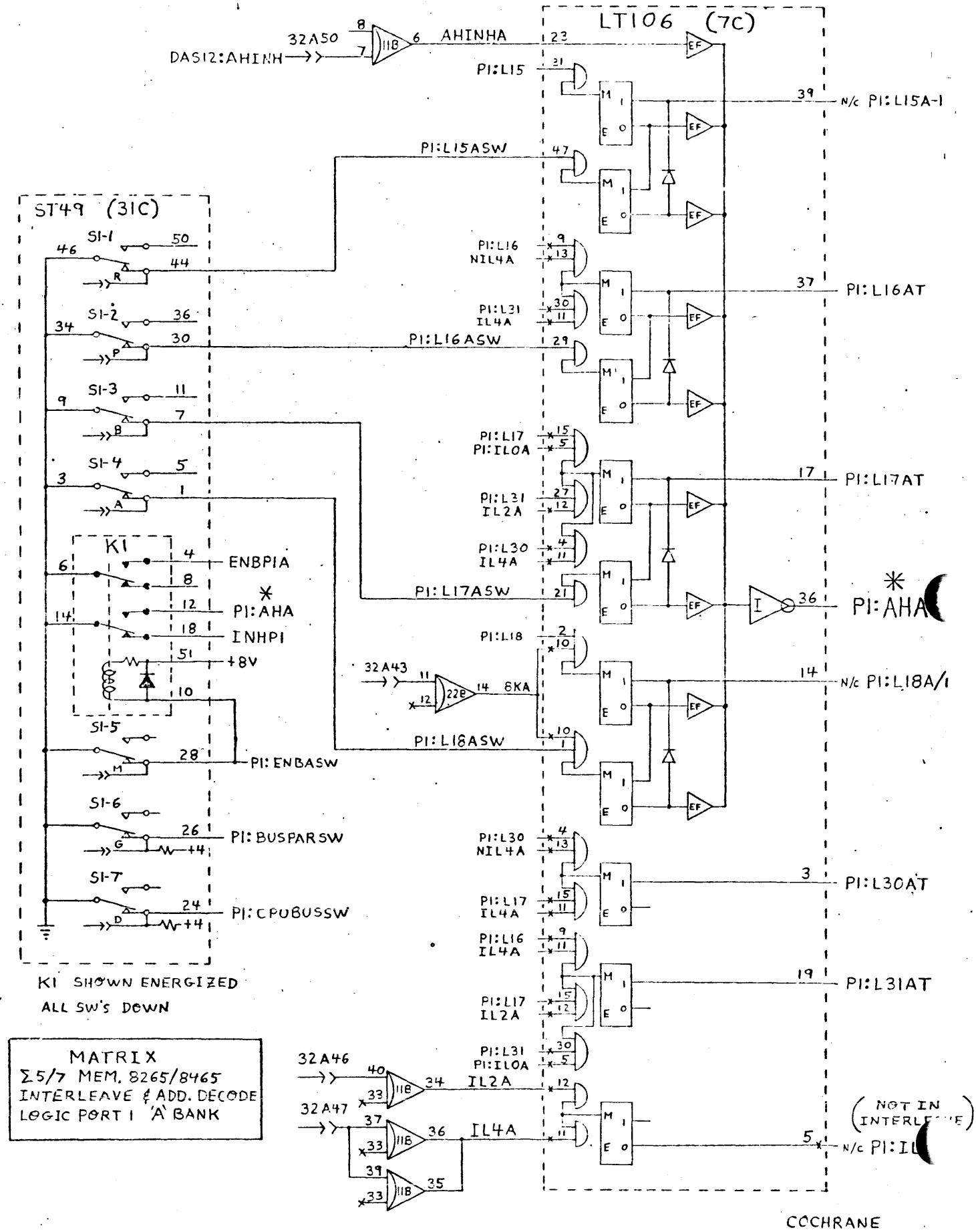
(KNEE OF FALL OF SAST 140 NSEC. FROM RISE OF TPXC 1J30 OR TNXC 1J31 DEPENDING ON ADD's. FOR READ HALF CYCLE)

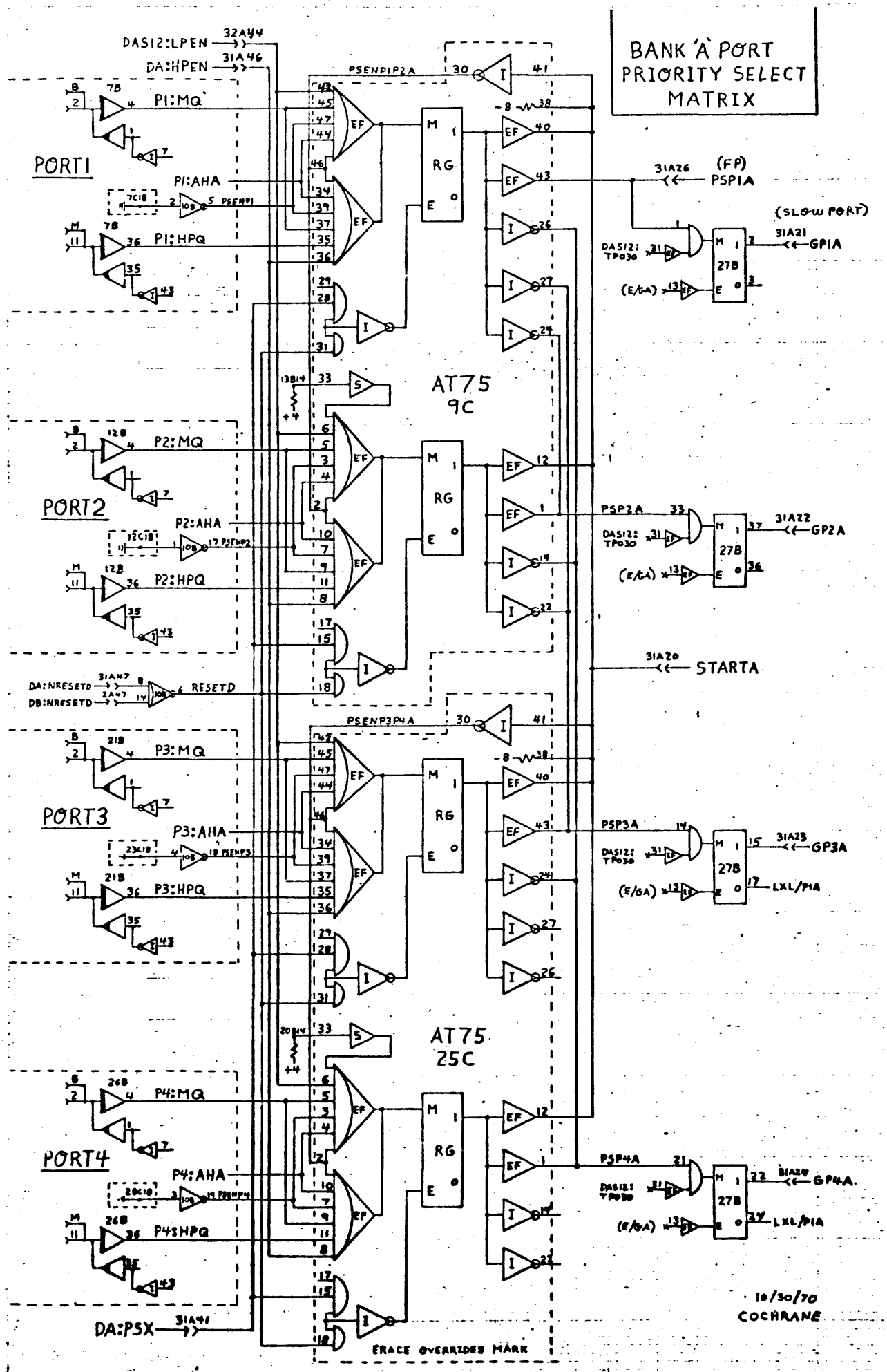
* - TPYI = 1,2,4,7 TNYI = 0,3,5,6
TPYC = 1,3,4,6 TNYC = 0,2,5,7
TPXC = 1,3,4,6 TNXC = 0,2,5,7
} DURING WHC

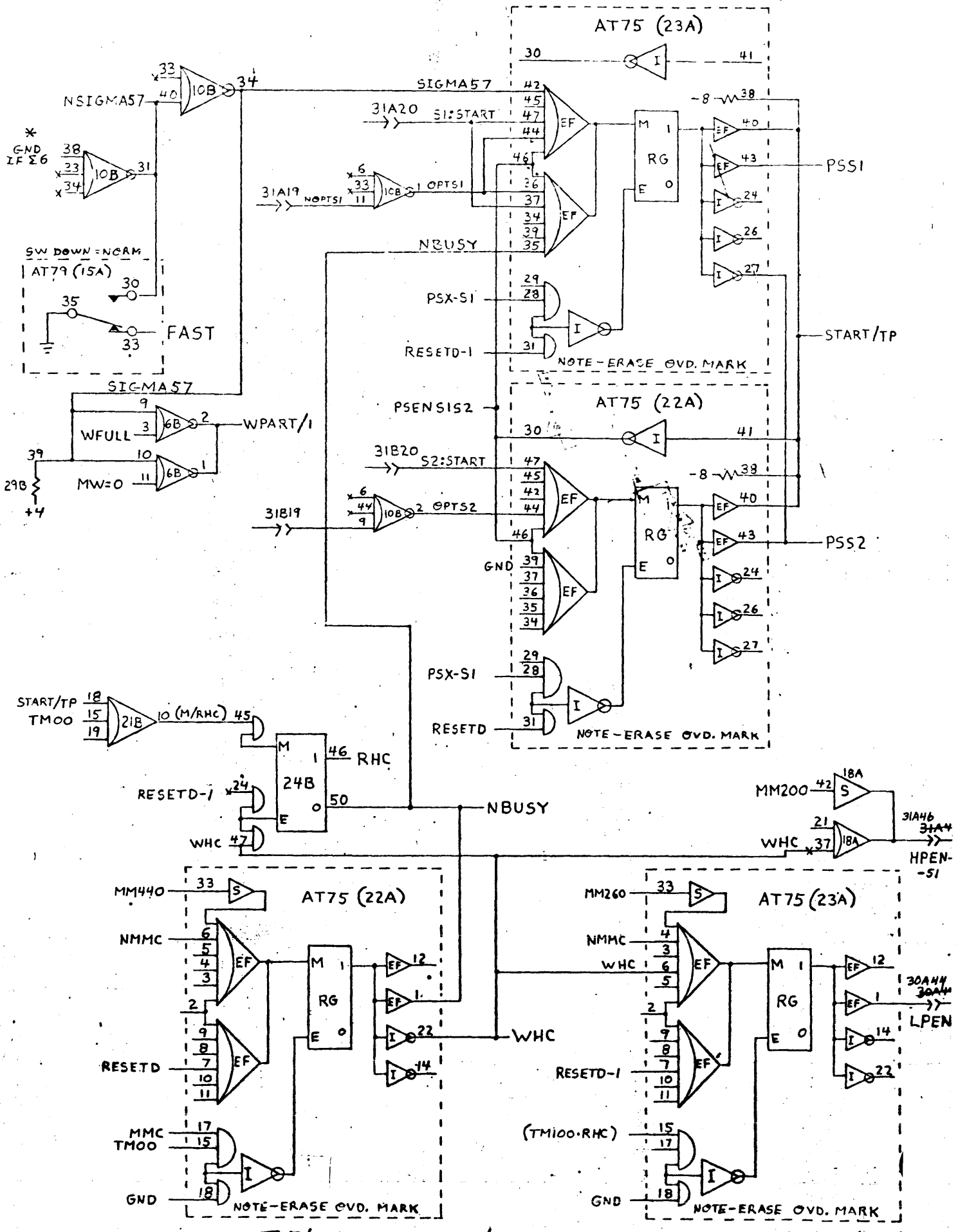
REFER TO DWR. # 153726 FOR A MORE DETAIL OF BMU

SHEET 2 of 2

10-16-70
COCHRANE


LT106 (7C)
ST49 (31C)
32A50
DAS12:AHINH
AHINHA
PI:L15
PI:L15ASW
PI:L16 NIL4A
PI:L31 IL4A
PI:L16ASW
PI:L17 PI:IL0A
PI:L31 IL2A
PI:L30 IL4A
PI:L17ASW
PI:L18
32A43
8KA
PI:L18ASW
PI:L30 NIL4A
PI:L17 IL4A
PI:L16 IL4A
PI:L17 IL2A
PI:L31 PI:IL0A
32A46
IL2A
32A47
IL4A
SI-1
SI-2
SI-3
SI-4
SI-5
SI-6
SI-7
K1
ENBPIA
PI:AHA
INHPI
+8V
PI:ENBASW
PI:BUSPARSW
PI:CPUBUSSW
K1 SHOWN ENERGIZED
ALL SW's DOWN
MATRIX
Σ5/7 MEM. 8265/8465
INTERLEAVE & ADD. DECODE
LOGIC PORT 1 'A' BANK
N/c PI:L15A-1
PI:L16AT
PI:L17AT
PI:AHA
N/c PI:L18A/1
PI:L30AT
PI:L31AT
(NOT IN INTERLEAVE)
N/c PI:IL
COCHRANE
1/5/71


BANK 'A' PORT PRIORITY SELECT MATRIX
DAS12:LPEN
DA:HPEN
PORT1
P1:MQ
P1:AHA
P1:HPQ
PORT2
P2:MQ
P2:AHA
P2:HPQ
PORT3
P3:MQ
P3:AHA
P3:HPQ
PORT4
P4:MQ
P4:AHA
P4:HPQ
DA:NRESETD
DB:NRESETD
RESETD
DA:PSX
PSENP1P2A
PSENP3P4A
AT75 9C
AT75 25C
RG
EF
PSP1A
PSP2A
PSP3A
PSP4A
STARTA
GP1A
GP2A
GP3A
GP4A
LXL/PIA
(FP)
(SLOW PORT)
DAS12: TP030
(E/GA)
ERACE OVERRIDES MARK
10/30/70
COCHRANE



Σ5/7 MEM. 8265/8465

DRIVER 'A' OR 'B'

11/27/70

COCHRANE

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