XDS 901586A
$5.75

TECHNICAL MANUAL

SIGMA 5 AND 7 CORE MEMORY

MODEL 8251/8451

February 1970

Prepared by
Field Engineering Publications

Xerox Data Systems 701 South Aviation Blvd., El Segundo, California 90245 (213) 772-4511, 679-4511

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LIST OF RELATED PUBLICATIONS

The following publications contain information not included in this manual but necessary for a complete understanding of the Core Memory Model 8251/8451 Assembly No. 132546 when used with related XDS equipment.

Publication Title	Publication No.
XDS Sigma 5 Computer, Reference Manual	900959
XDS Sigma 7 Computer, Reference Manual	900950
XDS Sigma Computer Systems Interface Design Manual	900973
Model 8251/8451 Core Memory, Engineering Support Manual	902308
Sigma 7 and 5 Memory (≥8K) Test (MEDIC 75), Diagnostic Program Manual (Program No. 704067)	900825
Sigma 5/7 Memory Interleaving Test (MIT), Diagnostic Program Manual (Program No. 704121)	901071
Power Supply Model PT16, Technical Manual	901080
Power Supply Model PT17, Technical Manual	901079

SECTION I

GENERAL DESCRIPTION

1-1 INTRODUCTION

This manual contains information pertaining to the operation and maintenance of the Core Memory Model 8251/8451, Assembly No. 132546 used in Sigma 5 and 7 computers. The core memory and the Sigma 5 and 7 computers are manufactured by Xerox Data Systems Inc., El Segundo, California. This manual contains four sections: Section I describes the physical and functional characteristics of the memory as a unit; section II describes the memory switches and how to set them for starting addresses, interleave size, bank size, bank number, port expander and simulated memory request; section III covers the theory of operation including all internal functions of a memory bank and port expanders; and section IV provides maintenance information and sequence charts. A list of replaceable parts and an illustrated parts breakdown are shown in appendix A.

Other technical manuals describing the equipment associated with core memory are referred to in the List of Related Publications provided in the front matter of this manual.

The memory for the Sigma 5 and 7 computers is referred to throughout this manual as the Sigma 5 and 7 memory, core memory, or memory. The memory provides magnetic core storage with high speed input/output capabilities and can accommodate Sigma 5 and 7 central processing units (CPU), multiplexing I/O processors (MIOP), selector I/O processors (SIOP), or special devices with compatible interfaces for direct to memory access.

1-2 PHYSICAL DESCRIPTION

In Sigma 5 and 7 computers, memory is contained in one to four cabinets, depending on total memory size for the given system. A memory cabinet may contain one or two independent units of memory, each mounted in a frame as indicated in figure 1-1. Each of frames 1 or 2 in the figure contain all of the core diode modules, electronics, control logic, and power supplies to operate independently as a memory unit. Frames 1 and 2 in a cabinet are hinged on one edge so that they can be swung open for easy access to their printed wiring modules. If either frame 1 or frame 2 has expanded ports, frame 3 is included in the cabinet to contain the port expanders. Frame 3 is not hinged and requires rear access to the cabinet when it is installed.

In everyday usage, several names have evolved for the memory contained in a frame. All are synonymous with frame. Some of these names are bank, block, rack, module, and door of memory. For this manual, the word bank has been chosen to describe the memory in one frame and is used hereafter. Figure 1-2 shows a typical memory bank. Some of the essential parts are called out. A module location chart relating the printed circuit modules to their respective functions is shown in figure 1-3.

1-3 STORAGE CAPACITY

A bank may have a word capacity of 4K (K = 1024), 8K, 12K, or 16K depending on the number of core diode modules it contains. A 4K bank contains four core diode modules (one stack). The bank shown in figure 1-2 has the maximum capacity of 16 core diode modules (four stacks). Storage capacity expansion requires additional printed circuit modules. Note 1 of figure 1-3 indicates the required module complement for any given expansion from the basic 4K memory. (All modules not related to note 1 comprise the basic 4K memory.)

The basic memory and the expansions are listed in table 1-1. The first four items in the table relate to memory size and expansions; the last four items relate to memory ports and port expansion.

Chassis G and H of figure 1-3 show that one core diode module provides storage for one byte (eight bits) of 4K words. One stack of core diode modules (four modules) provides storage for all four bytes (32 bits plus one parity bit) of 4K words. Note that the core diode modules in byte 3 are different from those in the other three bytes according to the part number. The core diode modules in byte 3 have nine bit planes instead of eight (one extra bit plane to store the parity bit).

1-4 MEMORY INTERCONNECTIONS

Memory banks are connected to the CPU or IOP and to other banks by memory buses, which consist of five cables terminated at the bank by module AT10 cable receivers or module AT11 cable driver-receivers, depending on the bus function. The buses connect the banks in successive memory cabinets in a trunk-tail manner. Figure 1-4 shows a block diagram of a maximum configuration for memory cabinet No. 1 with two memory banks and maximum port expansion. The buses connect to a bank at a port. A port is the interface between a bank and a bus. Physically, a port contains sufficient logic to perform three major functions: input/output address recognition, and interleaving. These functions are discussed in detail in section III; interleaving is also discussed in section II.

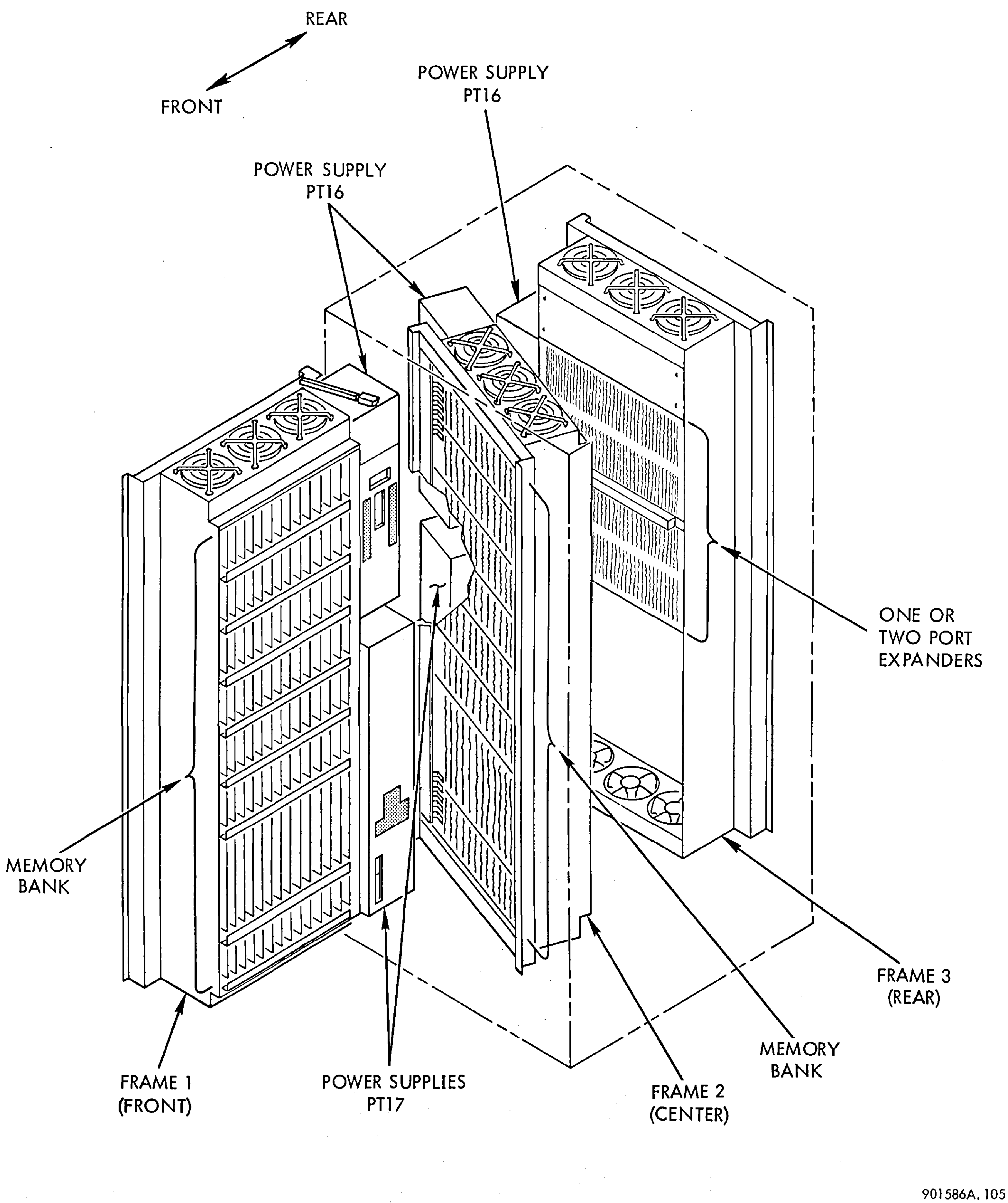

Figure 1-1. Memory Cabinet (Typical)

We have C only

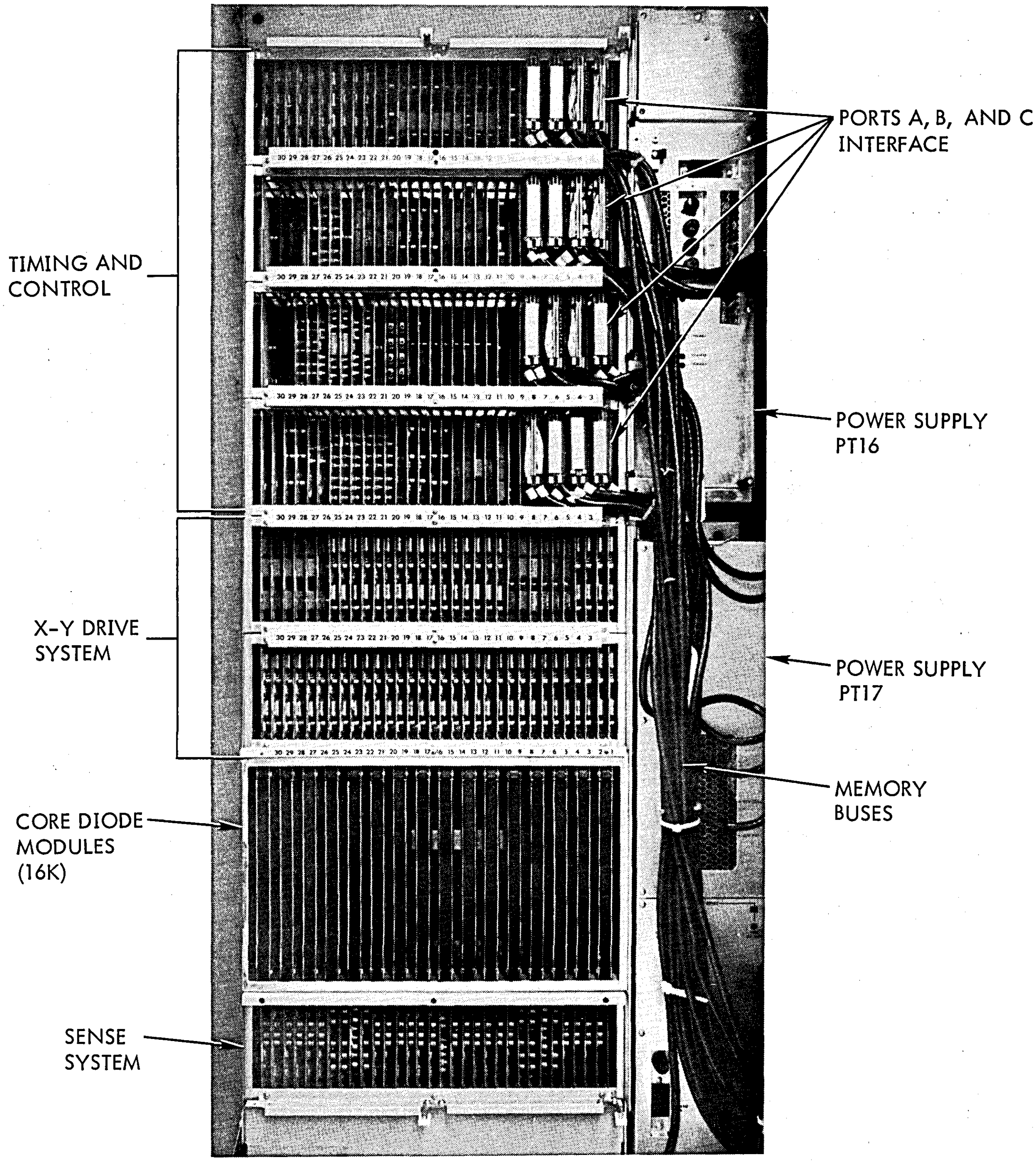

Figure 1-2. Memory Bank (Typical)

Checked Sept 10, 1975 [initials] · Dots → empty slots

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
A	XT 13 0-3	XT 13 4-7	XT 13 8-11	XT 13 12 15	XT 13 16-19 32	XT 14	XT 13 20-23 32	XT 13 24-27	XT 13 28-31	XT 13	XT 10	IT 25 NM32	LT 34	LT 34	LT 34 PARITY GENERATOR	LT 34
B	XT 10	ZT 25	ZT 25		IT 16	BT 22	BT 22	XT 10	IT 14 NM00 ↓ NM07	FT 38 M00 ↓ M07	IT 14 NM08 ↓ NM15	FT 38 M08 ↓ M15	BT 24	BT 24	IT 24	BT 24
C	XT 10			BT 22		DT 11	HT 15	HT 15	DT 11	HT 15	XT 10	ST 14	ST 14	LT 20	LT 21	LT 20 NLB16 ↓ NLB19
D	XT 10	XT 10	BT 16	IT 16	AT 16	AT 16	BT 22	BT 22	BT 22	BT 22	BT 22	BT 22	XT 10	IT 25	BT 25	BT 16
E	ST 21 BIT 0-5	ST 21 BIT 6-9	ST 21 INHIBITS BIT 10-15	ST 21 BIT 16-21	ST 21 BIT 22-25 32	ST 21 BIT 26-31	ST 10 ← X-DRIVERS /5	ST 10 /5	ST 10 /5	ST 10 /5	ST 10 /5	ST 10 /5	ST 10 /5	ST 10 → /5	ST 10 ← X-DRIVERS	ST 10
F	ST 11 ← Y-DRIVERS 0 ↓ 3	ST 11 4 ↓ 7	ST 11 0 ↓ 3	ST 11 → 4 ↓ 7	ST 11 ← Y-DRIVERS 0 ↓ 3 /4	ST 11 4 ↓ 7 /4	ST 11 0 ↓ 3 /4	ST 11 → 4 ↓ 7 /4	ST 11 ← Y-DRIVERS 8 ↓ 11	ST 11 12 ↓ 15	ST 11 8 ↓ 11	ST 11 → 12 ↓ 15	ST 11 ← Y-DRIVERS 8 ↓ 11 /4	ST 11 12 ↓ 15 /4	ST 11 8 ↓ 11 /4	ST 11 → 12 ↓ 15 /4
G-H	111549 4K		111549 12K BYTE 0 BITS 0-7 /2		111549 8K /1		111549 16K /3		111549 4K		111549 12K BYTE 1 BITS 8-15 /2		111549 8K /1		111549 16K /3	
J	HT 26 0-5	HT 26 0-5 /2	HT 26 PREAMPL 0-5 /1	HT 26 0-5 /3	HT 26 6-11	HT 26 6-11 /2	HT 11 SENSE AMPL 0-5	HT 11 6-10	ST 34 STROBE GEN BYTE 0-1	HT 11 S.A. 12-17	HT 26 6-11 /1	HT 26 6-11 /3	HT 26 PREAMPL 12-17	HT 26 12-17 /2	HT 26 12-17 /1	HT 26 12-17 /3
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	LT 34	LT 34	BT 22 M32	LT 34	LT 34	XT 10	BT 16	FT 37	AT 11 MC00 ↓ MC13	FT 37	/7 AT 11 MB00 ↓ MB13	FT 37	AT 11 MA28 ↓ MA31	FT 37	/6 AT 11 MA00 ↓ MA13	XT 10
B	FT 38 M16 ↓ M23	IT 14 NM16 ↓ NM23	FT 38 M24 ↓ M31	IT 14 NM24 ↓ NM31	XT 10	BT 16	ZT 25	FT 37	AT 11 MC14 ↓ MC27	FT 37	AT 11 MB14 ↓ MB27	FT 37	AT 11 MB28 ↓ MB31	FT 37	AT 11 MA14 ↓ MA27	XT 10
C	LT 21 LB16 ↓ LB19	LT 20 NLA16 ↓ NLA19	LT 21 LA16 ↓ LA19	LT 21	LT 21	XT 10		LT 21	AT 11 MC28 ↓ MC31	FT 37	AT 11 MOA MRA	BT 16	/6 AT 10 LA15 ↓ LA28	BT 16	AT 31 ST	XT 10
D	IT 16	FT 38	IT 14	LT 34	FT 38	IT 14	XT 10	LT 21	AT 11 MQC MRC	BT 22	AT 10 LC15 ↓ LC28	LT 19	AT 11 MQB MRB	FT 38	/7 AT 10 LB15 ↓ LB28	XT 10
E	ST 10	ST 10 X-DRIVERS	ST 10	ST 10	ST 10	ST 10 →	ST 22 ← X-AND Y-PREDRIVERS	ST 22	ST 22	ST 22	ST 22 /4	ST 22 → /5	ST 10	ST 10 BIT 32	ST 10 /4	ST 10 /4
F	ST 11 ← Y-DRIVERS 16 ↓ 19	ST 11 20 ↓ 23	ST 11 16 | 19	ST 11 → 20 | 23	ST 11 ← Y-DRIVERS 16 | 19 /4	ST 11 20 | 23 /4	ST 11 16 | 19 /4	ST 11 → 20 | 23 /4	ST 11 ← Y-DRIVERS 24 | 27	ST 11 28 | 31	ST 11 24 | 27	ST 11 → 28 | 31	ST 11 ← Y-DRIVERS 24 | 27 /4	ST 11 28 | 31 /4	ST 11 24 | 27 /4	ST 11 → 28 | 31 /4
G-H	111549 4K		111549 12K BYTE 2 BITS 16-23 /2		111549 8K /1		111549 16K /3		111550 4K		111550 12K BYTE 3 BITS 24-32 /2		111550 8K /1		111550 16K /3	
J	ST 15 STACK SELECT	HT 26 18-23	HT 26 18-23 /2	HT 26 PREAMPL 18-23 /1	HT 26 18-23 /3	HT 26 24-29	HT 26 24-29 /2	HT 11 SENSE AMPL 18-21	HT 11 22-26	ST 34 STROBE GEN BYTE 2-3	HT 11 S.A. 27-32	HT 26 24-29 /1	HT 26 PREAMPL 24-29 /3	HT 26 30-32	HT 26 30-32 /2	ST 17 Ve AND 1-7V
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

NOTES: 1. MEMORY EXPANSIONS

/1 = 8K
/2 = 12K
/3 = 16K
/4 = OVER 4K
/5 = OVER 8K
/6 = PORT A
/7 = PORT B

2. VOLTAGE POINTS & ADJUSTMENTS

VM = 1/2 VD (PIN 21 ON ST11'S)
VD ≈ +2215 VDC (ADJUST COARSE/FINE POTS ON PT17)
VC = +24.00 (ADJUST VC ON PT17)
VT = 0.33 ± .02 TOP POT PIN 15 (MODULE 1-24J) (MODULE 3-7J)
VS = 3.00 BOT POT PIN 24 (MODULE 1-24J) (MODULE 3-7J)
VE ≈ 1 VOLT LESS THAN -8 (MEASURE BETWEEN -8V AND 01J38)
-1.7 = PIN 1J18

Figure 1-3. Memory Bank, Module Locations

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Table 1-1. Sigma 5 and 7 Memory Models and Options

MODEL NUMBER		ASSEMBLY NUMBER	DESCRIPTION	PREREQUISITES		MAXIMUM NUMBER
Sigma 5	Sigma 7			Sigma 5	Sigma 7	
8251	8451	132546	4K memory, single access (port C); Model 8451 has two-way access (ports B and C)	8201	8401	8
8252	8452	117638	4K-8K memory expansion	8251	8451	8
8252	8452	117639	8K-12K memory expansion	8252	8452	8
8252	8452	117640	12K-16K memory expansion	8252	8452	8
8255		129463	Two-way access (port B)	8251		8
8256	8456	129463	Three-way access (port A)	8255	8451	8
8257	8457	130625	Port expander F (first); six-way access, one memory	8256	8456	4
8257	8457	130626	Port expander S (second); six-way access, one memory-two memory	8257(F)	8457(F)	4

Port C is standard with every bank and is the port to which the controlling CPU is usually connected. Facilities for port B and port A are provided. These ports are optional (port B is standard on Model 8451) and are added to a bank, in that order, to expand port facilities. Each port provides access to the bank from one source, either a CPU or an IOP. Since only one port can be accessed at any time, the bank contains port priority logic to control port selection. Port A has the highest priority, port B has the next highest, and port C has the lowest.

1-5 Port Expanders F and S

Port facilities can be expanded further by connecting a port expander to either port B or port A but not to both. (See figure 1-4.) A port expander provides connections for four sources and results in a net total of six access channels (maximum) per bank. Port expander F (first) is the first expander added to a memory cabinet and serves bank number 1, located in the center frame of the cabinet. Port expander S (second) is added to port expander F to serve bank number 2, located in the front frame of the cabinet. Port expanders F and S share some of the same printed circuit modules. Therefore, the combination of both expanders has only a slightly larger physical configuration than port expander F alone. The port expanders are mounted in frame 3 (fixed) of the memory cabinet in chassis B, C, D and E. The space for chassis A is used for cables. Chassis F, G, H and J are blank. Figure 1-5 shows the module locations of port expanders F and S. As indicated in the figure, port expander F is mounted in chassis B, C, and D. If port expander S is included, chassis E is used and additional modules are inserted in chassis B and C. The notes at the bottom of figure 1-5 describe the various configurations of port expanders F and S.

The ports in a port expander are numbered 1 through 4 and have a fixed priority in descending numerical order. That is, port number 1 has the highest priority and port number 4 has the lowest. If the port expander is connected to port A, then its four ports have a higher priority than port B; if connected to port B, they have a lower priority than port A.

1-6 PORT EXPANDER TO SOURCE CONNECTIONS

All signal transmission between the port expander and the sources is conducted by AT10 cable receiver modules and AT11 cable driver-receiver modules. The cables are conventional 33-ohm coaxial cables with etch/component connectors. All 33-ohm cables enter frame 3 of the memory cabinet through chassis A and fan downward into the port expander. For this reason, the cable connectors on the AT10 and AT11 cable modules are connected to the modules in an upside-down position. The resulting signal transposition is accommodated by the backpanel wiring in the port expander. If all four ports are used, there are twenty 33-ohm cables for the port expander entering the memory cabinet and twenty 33-ohm cables leaving the cabinet. Since port expander F and port expander S share the same AT10 and AT11 modules, cables connecting both port expanders are connected to only one module. The module locations for the AT10 and AT11 circuit boards and the ports which they serve are noted in chassis B and D of figure 1-5.

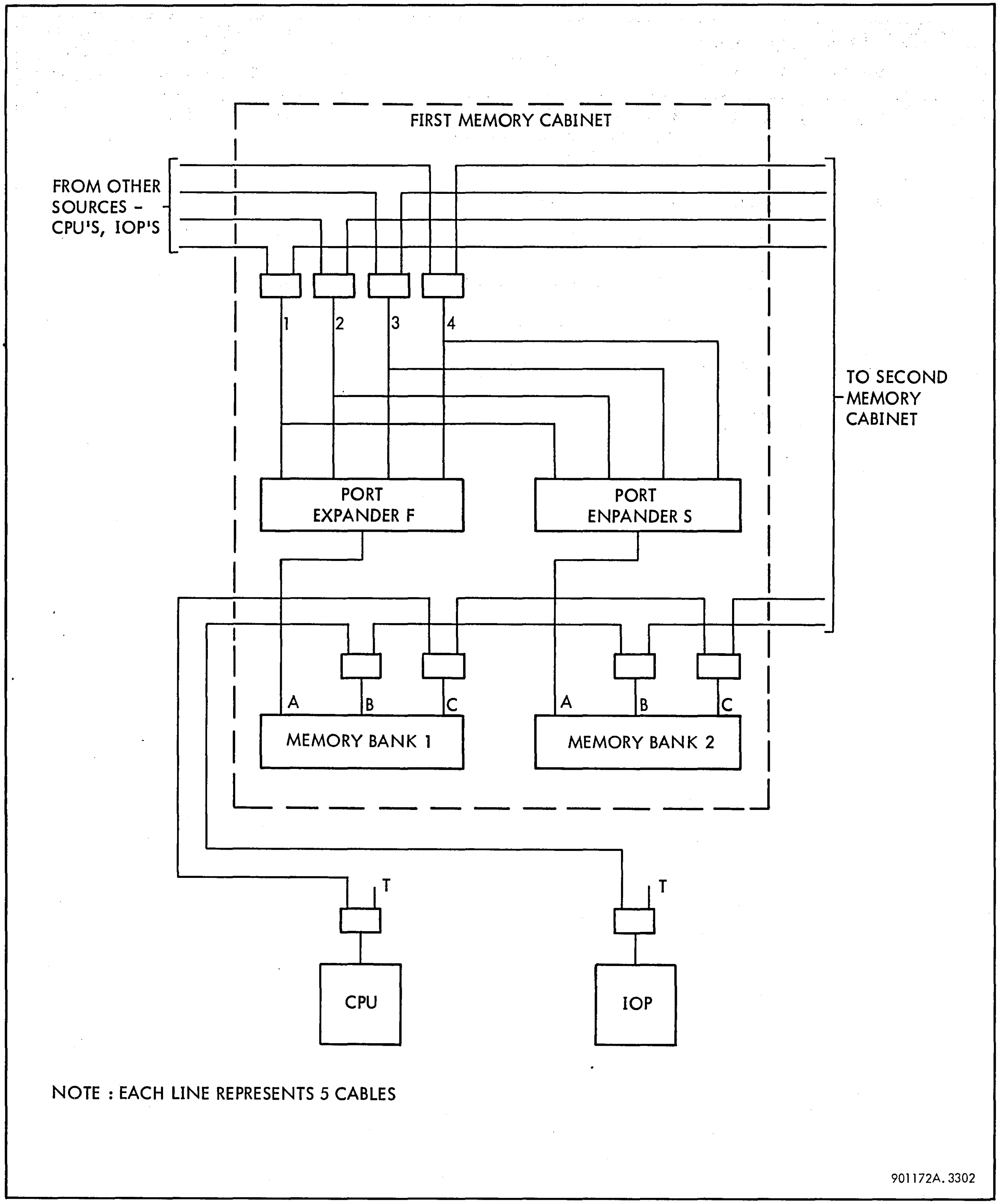

Figure 1-4. Memory Cabinet, Maximum Configuration

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
B	AT 11 PORT 4	BT 22	AT 11 PORT 3	FT 37	AT 11 PORT 2	FT 37	AT 11 PORT 1	XT 10 ③	AT 10 PORT 4	XT 10	AT 10 PORT 3	FT 38	AT 10 PORT 2	FT 38	AT 10 PORT 1	IT 16
C	XT 10	FT 26	BT 22	BT 24	IT 16	ZT 38	BT 22	ZT 38	FT 38	ZT 38	FT 38	ZT 38	FT 38	ZT 38	FT 38	ZT 38
D	- -	ZT 35 ①	AT 16	AT 16	IT 16	BT 15	IT 15	ST 14	ST 14	XT 10	LT 20	LT 21	LT 20	LT 21	LT 20	LT 21
E	- -	ZT 45 ②	BT 24	BT 22	XT 10	IT 15	AT 16	AT 16	IT 16	BT 15	ST 14	ST 14	XT 10	LT 20	LT 21	LT 20

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
B	AT 11 PORT 4	IT 16	AT 11 PORT 3	FT 37	AT 11 PORT 2	FT 37	AT 11 PORT 1	FT 37	AT 11 PORT 4	FT 37	AT 11 PORT 3	FT 37	AT 11 PORT 2	FT 37	AT 11 PORT 1	FT 37
C	FT 38	FT 38	FT 38	ZT 38	FT 38	ZT 38	FT 38	FT 38	ZT 38	FT 38	ZT 38	FT 38	XT 10	XT 10	XT 10 ③	XT 10
D	LT 20	LT 21	ZT 35 ①	XT 10	XT 10	IT 16	IT 16	FT 37	AT 11 PORT 4	FT 37	AT 11 PORT 3	FT 37	AT 11 PORT 2	FT 37	AT 11 PORT 1	FT 37
E	LT 21	LT 20	ZT 45 ②	LT 21	LT 20	LT 21	XT 10	- -	- -	- -	- -	- -	- -	- -	- -	- -

NOTES : MODULES HEAVILY OUTLINED ARE FOR PORT EXPANDER S ONLY.
SPECIAL CONFIGURATIONS ARE DEFINED BY THE FOLLOWING :

① ZT35 MODULE USED IN SIGMA 5 ONLY. FOR PORT EXPANDER F (WITHOUT S) IN SIGMA 7, XT10 MODULE IS USED. FOR PORT EXPANDER F AND S COMBINED IN SIGMA 7, ZT45 MODULE IS USED. XT10 MODULES REMOVED, WHEN ADDING PORT EXPANDER S TO F, ARE INSERTED IN POSITIONS B25 AND C2. SEE NOTE 3

② SIGMA 7 ONLY, BLANK FOR SIGMA 5

③ IN SIGMA 7, XT10 MODULES ARE INSERTED FROM POSITIONS D14 AND D31 WHEN ADDING PORT EXPANDER S TO F

Figure 1-5. Sigma 5 and 7 Memory Port Expanders F and S, Module Locations

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1-7 PORT EXPANDER TO MEMORY INTERCONNECTIONS

Each port expander and memory bank is interconnected by five 120-ohm twisted-pair cables. These are special cables, permanently attached to a ZT38 circuit board at each end. The cables are electrically symmetrical with respect to their ends. The ZT38 boards plug into the bank in module locations normally occupied by AT10 or AT11 circuit boards. Each conductor pair of the 120-ohm cables consists of two unidirectional conductors, each terminated in 220-ohms at its load end. The conductor pair represents a bidirectional conductor in a 33-ohm cable. The module locations for the cable interconnections between a port expander and either port A or port B of a memory bank are listed in table 1-2.

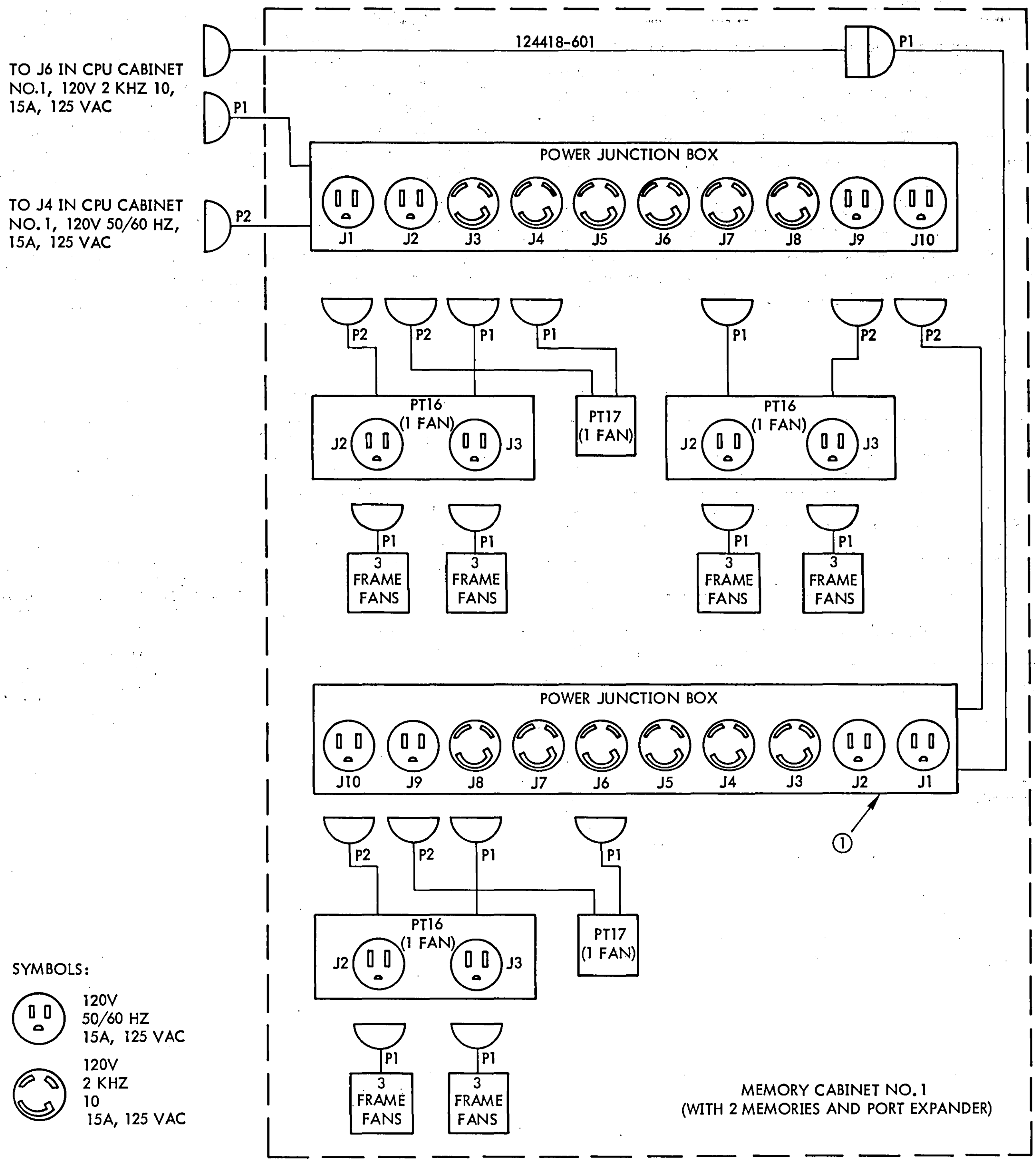
1-8 POWER DISTRIBUTION

Primary power to the memory cabinet is 120V, 50/60 Hz, and 120V, 2 kHz, obtained from a PT15 power supply. (See figure 1-6.) The power is usually obtained from a PT15 power supply mounted in CPU cabinet No. 1 or an accessory cabinet in the system. All cooling fans, including those in the PT16 and PT17 power supplies, are driven by the 120V, 50/60 Hz power. The 120V, 2 kHz power provides the primary input to the power supplies. For particulars on the PT16 and PT17 power supplies, refer to their respective technical manuals referenced in the List of Related Publications.

A memory cabinet may have one or two junction boxes (J-boxes) depending on hardware requirements. One J-box is sufficient for two banks of memory, but if the cabinet also contains a port expander, a second J-box is required.

Table 1-2. Port Expander to Memory, Cable Interconnections

	PORT		CABLE PLUG MODULE LOCATIONS				
From	Port Expander F		6C	11C	17C	21C	25C
To	Bank 1	Port A	2A	2B	4A	4C	6C
		Port B	6A	6B	4B	2D	4D
From	Port Expander S		8C	13C	19C	23C	27C
To	Bank 2	Port A	2A	2B	4A	4C	6C
		Port B	6A	6B	4B	2D	4D



NOTES: ① SECOND J-BOX REQUIRED ONLY WHEN A PORT EXPANDER FRAME IS USED. CONNECTIONS MAY BE MADE TO J-BOX(E) IN ADJACENT MEMORY CABINET IF LOAD ALLOWS

2. REFERENCE XDS DWG: 139273-5D

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Figure 1-6. Memory Cabinet Main Power Distribution

SECTION II
OPERATION

2-1 INTRODUCTION

A memory bank operates according to the address and the control information presented by the source that is requesting service. There are no manual operating controls in the memory, but every bank has two ST14 switch modules, each containing fifteen toggle switches. (See figure 2-1.) These modules are located in slots 20C and 21C and their switches form part of the bank logic. If the bank has a six-way access port expander, two similar switch modules are located in positions 24D and 25D of port expander F and in positions 21E and 22E of port expander S. (See figure 2-2.) These switches in the port expander are for starting address only and do not affect the other switches in the bank.

In general, the bank switches are set up according to the physical properties of the memory. Their configuration determines the memory's operating characteristics. Once the switches are set, they should not be changed unless it is necessary to change the interleave characteristics, to alter the bank configuration, or to perform certain troubleshooting procedures. The switches are not only set up according to the physical properties of the memory, but if interleaving is to be in effect, their configuration must also satisfy the interleaving requirements.

2-2 INTERLEAVING

Interleaving is a method of reducing the average memory access time when accessing sequential addresses. Each successive address in the given sequence is directed to a different memory bank. For example, if two banks are interleaved, they are accessed alternately. In this way, the next access may start before the memory cycle of the currently-accessed bank is finished. This method is especially useful with high speed devices that accomplish data block transfers in a single operation. Also, with interleaving, one device cannot monopolize a single bank. Not all banks in a system must be interleaved; one group may be interleaved apart from the remaining banks in the system, or groups of banks may be interleaved independently of other groups.

Interleaving requires the memory switches to be set up so that:

a. The assigned addresses form a continuous address field (no gaps or overlaps between banks)

b. The starting address of each bank is a multiple of the bank size

c. The total interleaved group is 8K, 16K, 32K, or 64K on its own boundary

d. An interleaved group contains no more than eight banks

A group of eight banks is interleaved in two groups of four. That is, the first four banks are accessed until completed; then the second four banks are accessed. When four banks only are interleaved, all four are accessed as a group until completed. The logical way in which an address is transformed, modified, and manipulated for interleaving is discussed in paragraph 3-9. It is recommended that paragraph 3-9 be understood before setting up the switches for interleaving.

2-3 MEMORY SWITCH SETUP

The memory switches are logically connected to:

a. Set the bank's starting address at all ports

b. Identify the bank size

c. Set the interleave group size

d. Identify the bank number for the processor control panel (PCP) MEMORY FAULT indicators

e. Condition port A or B for a port expander

f. Simulate a memory request

2-4 STARTING ADDRESS SWITCHES

Switches S15 through S19 are provided for each port. The switches for any port in the bank are set to reflect the five most significant bits of the starting address, which is the first address location in the bank. These bits uniquely identify the bank from other banks in the system. For normal applications, the starting address switch configuration is identical for all ports in the bank.

The memory configuration and the application of the system determines how the starting address switches should be set. Figure 2-1 identifies the starting address switches and table 2-1 shows the desired configuration for each. Table 2-1 holds true, with or without interleaving. Note that the possible starting address is a multiple of the bank size, as indicated by an X in the Bank Sizes column of table 2-1.

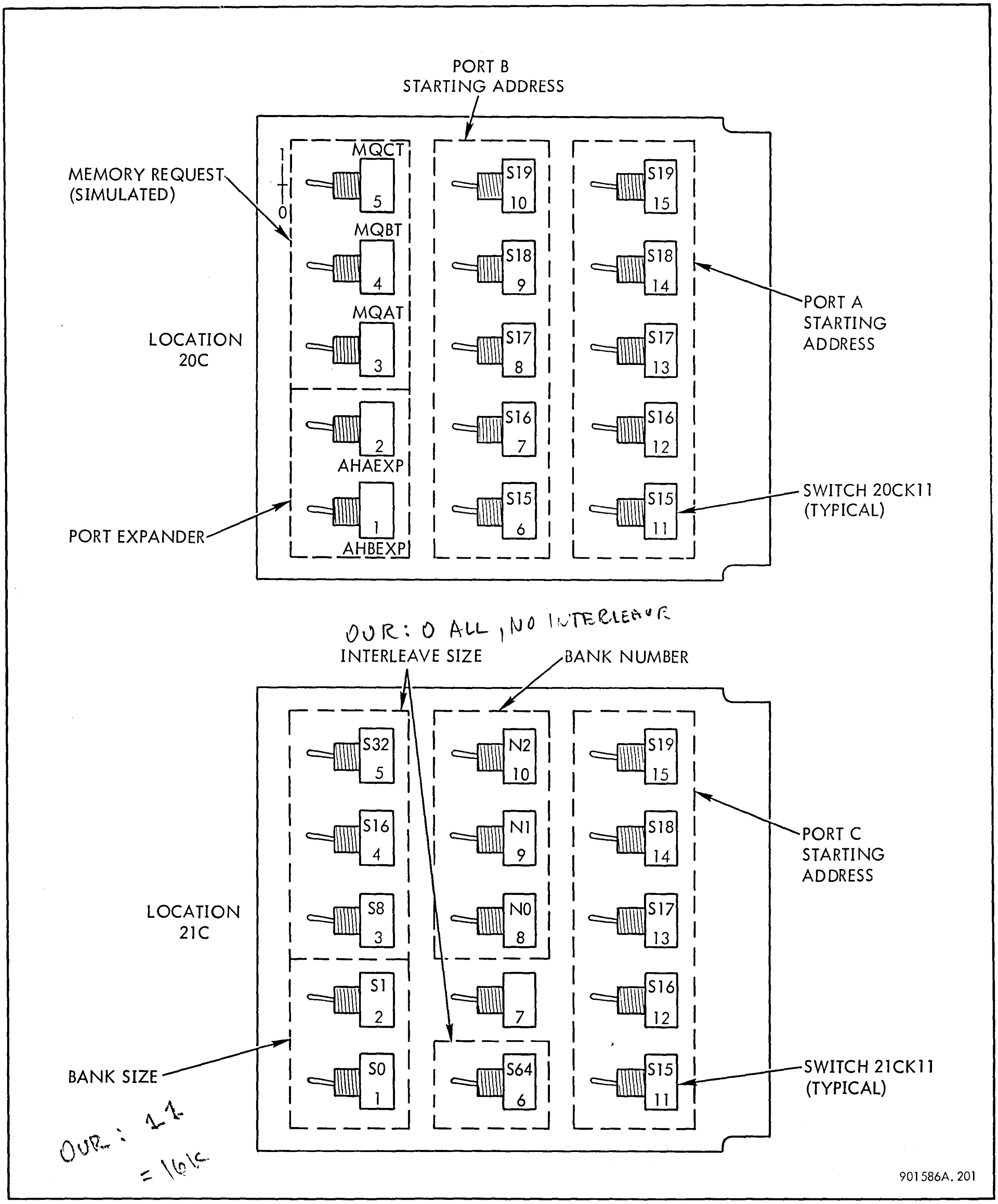

Figure 2-1. ST14 Memory Bank Switches Module

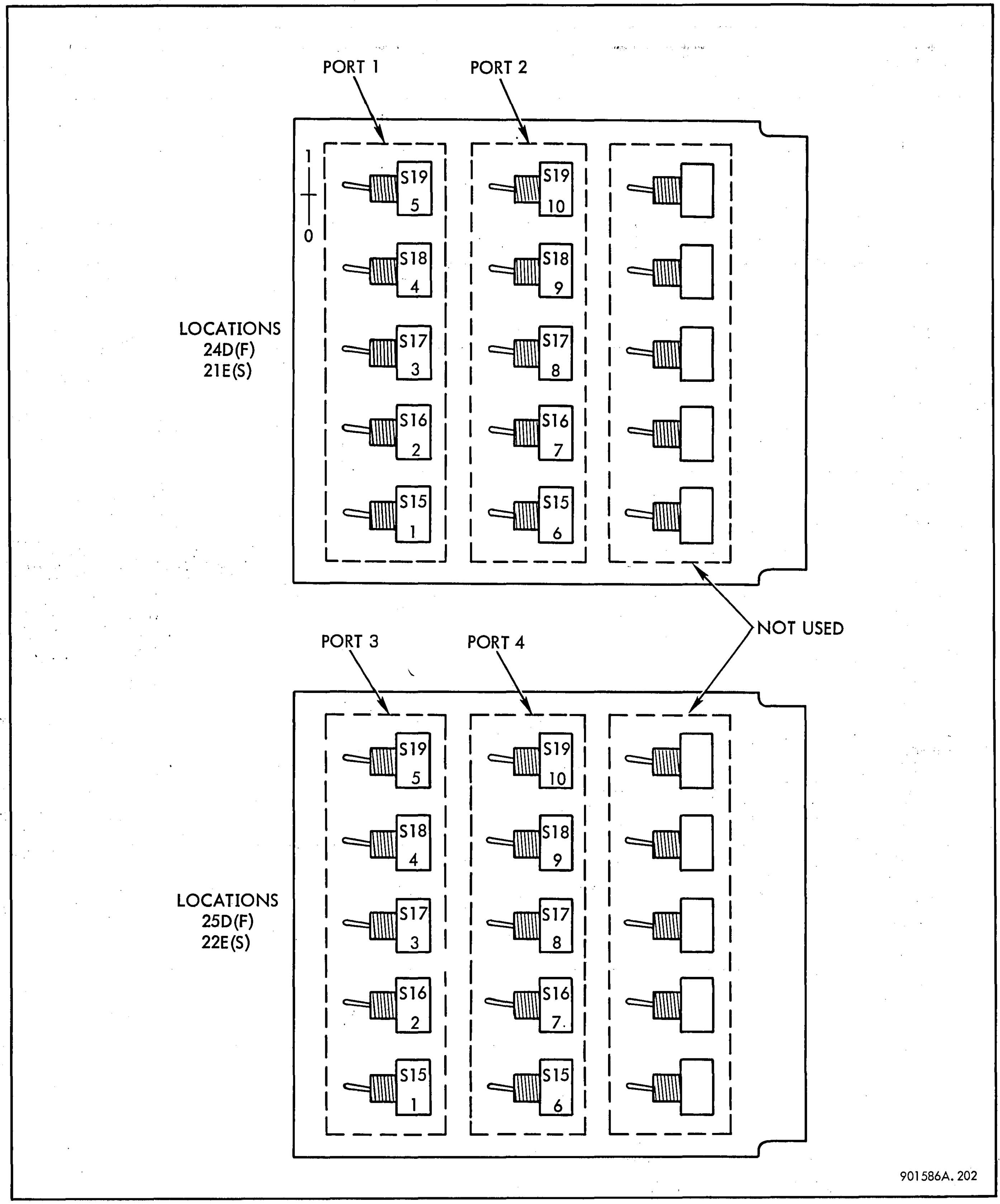

Figure 2-2. ST14 Port Expander Starting Address Switches Module

Table 2-1. Starting Address Switch Selection

POSSIBLE STARTING ADDRESSES	BANK SIZES*			STARTING ADDRESS SWITCH SETTINGS				
	4K	8K	16K	S15	S16	S17	S18	S19
0	x	x	x	0	0	0	0	0
4K	x			0	0	0	0	1
8K	x	x		0	0	0	1	0
12K	x			0	0	0	1	1
16K	x	x	x	0	0	1	0	0
20K	x			0	0	1	0	1
24K	x	x		0	0	1	1	0
28K	x			0	0	1	1	1
32K	x	x	x	0	1	0	0	0
36K	x			0	1	0	0	1
40K	x	x		0	1	0	1	0
44K	x			0	1	0	1	1
48K	x	x	x	0	1	1	0	0
52K	x			0	1	1	0	1
56K	x	x		0	1	1	1	0
60K	x			0	1	1	1	1
64K	x	x	x	1	0	0	0	0
68K	x			1	0	0	0	1
72K	x	x		1	0	0	1	0
76K	x			1	0	0	1	1
80K	x	x	x	1	0	1	0	0
84K	x			1	0	1	0	1
88K	x	x		1	0	1	1	0
92K	x			1	0	1	1	1
96K	x	x	x	1	1	0	0	0
100K	x			1	1	0	0	1
104K	x	x		1	1	0	1	0
108K	x			1	1	0	1	1
112K	x	x	x	1	1	1	0	0
116K	x			1	1	1	0	1
120K	x	x		1	1	1	1	0
124K	x			1	1	1	1	1

*The starting address for a 12K bank must be a multiple of 16K

A 12K bank is a special case since it must have a starting address that is a multiple of 16K, must be followed by a 4K bank, and, regardless of where it is located in a series, cannot be interleaved.

If either port A or port B is fed by a port expander, the starting address switches for ports 1, 2, 3, and 4 in the port expander are set to the bank starting address using figure 2-2 and table 2-1 for reference. In this case, the port A or port B port expander switch in bank location 20C is set to 1 and the starting address switches in bank location 20C for the corresponding port are bypassed. (See paragraph 2-8.)

2-5 BANK SIZE SWITCHES

Two switches, S0 and S1 (location 21C), are set to the binary configuration of the bank size. The switches and their settings are as follows:

Bank Size	S0	S1
4K	0	0
8K	0	1
12K	1	0
16K	1	1

2-6 INTERLEAVE GROUP SIZE SWITCHES

Switches S8, S16, S32, and S64 (location 21C) designate the total interleaved group memory size and correspond to 8K, 16K, 32K and 64K respectively. Only one of the switches can be true at any time. For example, switch S32 is set to interleave four 8K banks or two 16K banks. Switch S16 is set to interleave two 8K banks or four 4K banks. One requirement for interleaving is that the interleave size occur on its own boundary. That is, for an interleave size of 16K the starting address of the first bank in the interleaved group must be 0, 16K, 32K, ..., 112K.

2-7 BANK NUMBER SWITCHES

Switches N0, N1, and N2 (location 21C) are provided in each bank to identify the bank number in binary notation to the PCP. These switches are not involved in addressing; rather, they function with the parity error signal to energize the MEMORY FAULT lights on the PCP. Thus, the bank in which a parity error occurs is immediately identified by observing the fault lights. Switches N0, N1, and N2 for each bank are set as follows:

Bank Number	N0	N1	N2
1	0	0	0
2	0	0	1
3	0	1	0
⋮	⋮	⋮	⋮
8	1	1	1

2-8 PORT EXPANDER SWITCHES

Each bank has two port expander switches in location 20C, one for port A and one for port B. If a port expander is connected to either one of these ports, its corresponding port expander switch is set to 1; otherwise, the switch is left in the zero position. These switches are associated with address here signals AHAEXP and AHBEXP, respectively. When the port expander switch is in the one position, the address here signal from the port expander is connected to the respective port, and the address recognition logic in the respective port is bypassed.

2-9 MEMORY REQUEST SWITCHES

Three switches are provided in location 20C for maintenance personnel to apply a simulated memory request signal on ports C, B, or A. When set, these switches produce simulated memory request signals MQCT, MQBT or MQAT, at the respective port. During normal operation, these switches must be left in the zero position.

SECTION III
PRINCIPLES OF OPERATION

3-1 INTRODUCTION

The functions of a memory bank are described in detail in this section. First the memory input/output signals are described, then the internal functions are covered. Figure 3-1 is a functional block diagram of a Sigma 5 and 7 memory bank. All of the main functions described in this section are shown in some form on the diagram. The diagram serves as an overall reference for this section and is often referred to in the text.

In general, the address interface is shown on the left in the diagram, and the data and control line interface is shown on the right. Also note that, for most interface signals, the last letter in the signal name designates the port (C, B, or A) to which the signal is interfaced. Exceptions are the start signal /ST/, override signals /ORAB/, /ORAC/, /ORBC/, memory fault light signals /MFL0/-/MFL7/ and address signals /LX15/-/LX31/. The address signals have a general designator (X) until they enter the port, then the signals take the designator of the port. The letter X, similar to its use in the address signals, may also be used throughout the text in this section as a general designator for a letter or a numeral in a signal name.

Figure 3-1 does not show the functions of the port expander. These port expanders are covered in paragraphs 3-35 through 3-40.

3-2 FUNCTIONAL OVERVIEW (See Figure 3-1)

A memory bank becomes active when an address at one of its ports is recognized as being within the bank's assigned range. Since memory addressing and interleaving are discussed in detail in paragraphs 3-8 and 3-9, they are not described here. When the address is recognized, it is latched into the address register, L, where the address configuration selects X- and Y-predrive switches in the X-Y current/voltage predrive matrices. The X- and Y-predrive switches turn on X- and Y-drivers that send current through the core matrix to effect core switching. In figure 3-1, the core matrix is represented by a single core with its sense line fed to the sense preamplifier (PA). Pulses (data) resulting from the switched cores are amplified by PA and the sense amplifier (SA). The output of the sense amplifier is fed through a memory discriminator (MD). The memory mode of operation determines what occurs in the signal flow after this point.

3-3 MODES OF OPERATION

The memory has three modes of operation: read-restore, full clear-write, and partial clear-write. In the read-restore mode, the data from the discriminators takes two paths: it is loaded into data register M and it is gated out (by data gates DGXX) to the requesting source. The data in the M-register is ultimately restored to (written into) the cores to preserve it. (Data restoration is not shown in figure 3-1.) In the full clear-write mode, data is read from the cores but is not used. The M-register is loaded with a new word from the source, and the new word is written into the cores in a way resembling the restore portion of the read-restore mode. In a partial write mode, one, two, or three bytes from the cores are loaded into the M-register and the remaining byte (or bytes) are not used but are replaced by new bytes from the source. The revised word is then written into the cores in a way similar to the restore portion of the read-restore mode.

Note that, regardless of the mode of operation, a complete memory cycle involves both a read and a write activity. The timing of these activities is controlled by a read and a write delay line. Each delay line provides a 600-ns delay, and together they provide the timing for one memory cycle. However, the delay lines overlap in time so that the length of a memory cycle depends on the mode of operation. Mode control is a function of the write-byte flip-flops (or byte presence indicators) MW0 through MW3, as indicated in the upper right-hand portion of figure 3-1.

3-4 CORE SELECTION

During core selection, current flows through the cores in one direction for reading and through the same cores in the opposite direction for writing. Current direction is controlled by eight timing signals (TPXC, TNXC, . . .). These signals are timed by pulses from the read and write delay lines and gate to the X- and Y-drivers. For example, TPXC (time for positive X-current) and TNXV (time for negative X-voltage) enable the X-path between an X-positive current switch (XPCS) and an X-negative voltage switch (XNVS). Likewise, signals TNYC (time for negative Y-current) and TPYV (time for positive Y-voltage) enable a Y-path between a Y-negative current switch (YNCS) and a Y-positive voltage switch (YPVS). The selected X- and Y-paths are energized at the same time, and the cores at their intersections are the cores affected. Core selection is explained in detail in paragraphs 3-11 through 3-16. Writing into the cores also involves Y-inhibit drivers. These drivers inhibit current in the Y-lines where zeros are to be written. Inhibiting is explained in paragraph 3-17. A read cycle causes all selected cores to assume a binary zero state; a write cycle causes all selected cores to assume a binary one state unless inhibited.

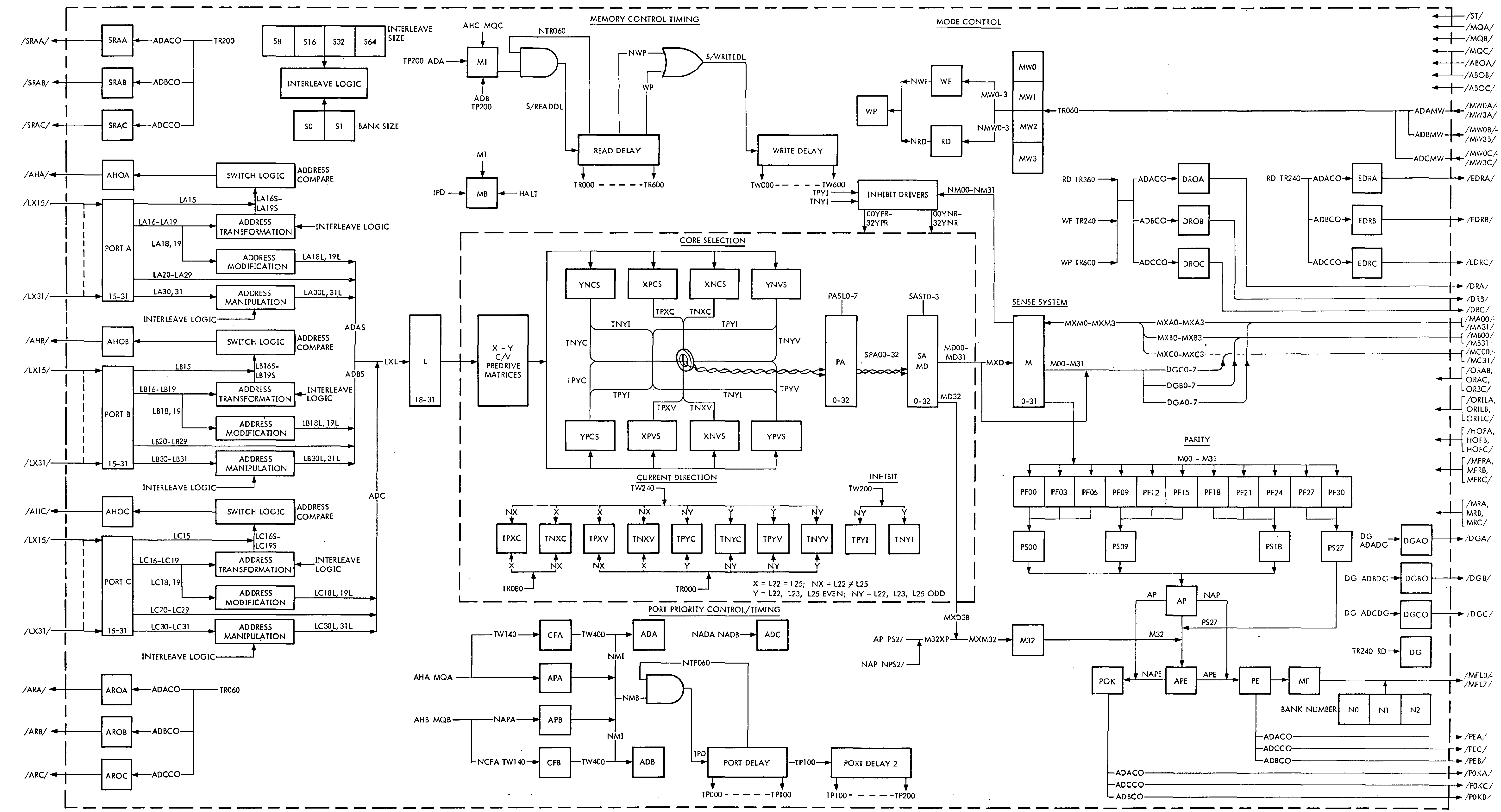

Figure 3-1. Memory Bank, Functional Block Diagram

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3-5 PARITY

Odd parity is checked whenever a word is read out of the cores and loaded into the M-register. The results of the parity check cause either the parity OK (POK) or the parity error (PE) signal to be sent to the source. Also, during the full clear-write mode or partial write mode, a parity bit is generated and loaded into bit M32 if the new word to be written into the cores does not contain an odd number of ones. Details on parity checking and generation are provided in paragraph 3-30.

3-6 PORT PRIORITY

For banks with more than one port, access to the bank is determined by the port priority timing and control logic. The process involves two delay lines and provides a port access decision signal that determines which port shall have access if two or more ports have recognized an address at the same time. Port C is not directly involved in the port priority decision since it always gets access if neither port A nor port B is busy. See paragraph 3-31 for details on the port priority logic.

3-7 MEMORY INPUT/OUTPUT SIGNALS

The following descriptions identify the input/output signals interfaced with a memory bank, as shown in figure 3-1. In general, the signals are listed in order of occurrence during a memory cycle.

a. /LX15/-/LX31/ address lines. Carry the address from the source to a port. Signals LX15 through LX19 are the five most significant bits and are used by the port logic for comparison with the starting address switches.

b. /AHA/, /AHB/, /AHC/, address here. Generated by the port when the address is recognized as being located within its respective bank. Address here serves two functions. It is output to the source to indicate that the address was valid. It also serves internally in the bank where it is gated with its corresponding memory request signal to perform the following:

1. AHA and AHB initiate a port priority decision for port A or port B, respectively, which ultimately leads to a memory cycle.

2. AHC initiates a memory cycle immediately. Port C requires no port priority decision.

c. /MQA/, /MQB/, /MQC/, memory request. Generated by the source to request a memory access. MQA and MQB are gated with AHA and AHB, respectively, in the bank to initiate a port priority decision, and MQC is gated with AHC to start a memory cycle immediately. (See address here, paragraph 3-76.)

d. /ORBC/, /ORAC/, /ORAB/, port override. One of these signals may be supplied by the source to each respective port. Signal ORBC is supplied to port A, ORAC to port B, and ORAB to port C. Each signal has the capability to override the other two ports by grounding their memory request signal, MQ(X).

e. /ORILA/, /ORILB/, /ORILC/, override interleave. Derived from the PCP when the INTERLEAVE SELECT switch is in the DIAGNOSTIC position. ORIL(X) allows the memory banks to be addressed without interleaving so that diagnostic tests may be run.

f. /ST/, start. Received by the bank from the power monitor. During a power-on sequence, ST is true until the dc power supplies have stabilized (approximately 300 ms); then ST goes false, indicating a ready condition for the bank. A memory cycle can only begin if ST is false. During a power-off sequence, ST again goes true to inhibit the X- and Y-predrivers and to reset control flip-flops, to prevent cycling of core memory during marginal power conditions which could cause errors.

g. /MW0A/-/MW3A/, /MW0B/-/MW3B/, /MW0C/-/MW3C/, write byte lines. Carry signals from the source to indicate which of the four bytes are to be written into memory for a partial write operation. If all four of the lines are true, the entire word is to be written, indicating a full clear-write operation. If all four lines are false, a read-restore operation occurs.

h. /ARA/, /ARB/, /ARC/, address release. Generated by the bank 60 ns after a memory cycle begins. Address release allows the source to drop its address lines, memory request, and write byte lines signal.

i. /ABOA/, /ABOB/, /ABOC/, abort. Generated by the source to override a write operation as specified by the write byte configuration. To be effective, ABO(X) must occur within 100 ns after the memory cycle begins and must remain high until the data release signal.

j. /SRAA/, /SRAB/, /SRAC/, second request allowed. Provided by the currently active memory bank. SRA(X) can be used by the source to initiate the next memory request. A new memory cycle may be started in another memory bank before the currently-active bank has completed its cycle.

k. /MA00/-/MA31/, /MB00/-/MB31/, /MC00/-/MC31/, data input/output lines. Provide 32 input/output data paths between a memory bank and a source.

l. /DGA/, /DGB/, /DGC/, data gate. Generated by the memory bank during the read mode to gate data into the receiving register of the source.

m. /DRA/, /DRB/, /DRC/, data release. Generated by the memory bank during a read and a write mode after a data transfer has occurred. During the read mode, the source may use DR(X) to gate the data from the receiving register to another register. During a write mode, DR(X) indicates to the source that the data has been received by memory and the data lines may be dropped.

n. /EDRA/, /EDRB/, /EDRC/, early data release. Generated by the bank during a read mode. EDR(X) can be used by the source to clear its receiving register.

o. /POKA/, /POKB/, /POKC/, parity okay. Generated by the bank during a read or partial write mode. POK(X) indicates to the source that the parity check on the word accessed showed an odd number of ones.

p. /PEA/, /PEB/, /PEC/, parity error. Generated by the bank during a read-restore or a partial write operation if a parity check detects an even number of ones in the word accessed.

q. /HOFA/, /HOFB/, /HOFC/, halt on fault. Signal derived from PARITY ERROR MODE switch on the PCP in the HALT position, causes memory bank to remain busy at the end of the cycle in which a parity error occurred. A new memory cycle cannot begin until the condition is cleared.

r. /MFL0/-/MFL7/, memory fault light. Signal derived from the bank number switches and a parity error, and sent to the MEMORY FAULT lamps on the PCP to indicate the bank number in which a parity error occurred.

s. /MFRPA/, /MFRPB/, /MFRPC/, memory fault reset parity. Reset signal from the source to clear a parity error by resetting the memory fault latch, MF.

t. /MRA/, /MRB/, /MRC/, memory reset. Reset signal from the source generated when the SYSTEM RESET/ CLEAR switch on the PCP is pressed.

3-8 MEMORY ADDRESSING

A memory bank is addressed by a configuration of address lines /LX15/ through /LX31/. Any configuration of the lines represents some address. Since a memory bank may have up to six ports (by a port expander), the bank is constantly being addressed by one or as many as six sources. When an address configuration matches the starting address switch setup in a port, the address is successfully decoded and the port generates the address here signal, AH(X). Address here is sent back to the source to indicate that the address has been recognized. If the source is not already generating a memory request signal, MQ(X), the source raises its /MQ(X)/ line upon receiving /AH(X)/. The two signals are then gated in the bank. If the port which recognized the address was port C, then AHC and MQC together initiate a memory cycle by setting the memory initiate signal, MI. At the same time, the address is latched into the L-register where it is decoded by the X- and Y-predrive matrices for core selection.

If the address was recognized by either port A or port B, signals AHA and MQA or AHB and MQB, respectively, initiate a port priority decision. This involves the port delay lines, numbers 1 and 2, and the associated logic. Ultimately, the port priority decision leads to the start of a memory cycle after port B or port A has gained access.

3-9 ADDRESS TRANSFORMATION, MODIFICATION AND MANIPULATION

If any one of the interleave size switches is set at the time the address enters the port logic, the interleave condition is true and four of the five most significant bits (16-19) go through a transformation before being decoded by the starting address switches (see figure 3-2). The same transformation occurs at every port (thus at every bank) to which the address is applied. The port whose address switch setup matches the transformed address configuration is the port which is activated. As a result of the transformation, a given bank is never activated twice in succession in a given address sequence. The transformation involves one or two bits of bits 16 through 19 being exchanged with one or both bits 30 and 31 of the address field. Bit 15 of the address is not involved in the transformation but is compared directly with its corresponding starting address switch, S15. Also note that bits LC20 through LC29 are not transformed but are applied directly to the L-register latches. Table 3-1 shows the address transformations resulting from the port C logic. Similar transformations occur for ports A and B. Note that the bits exchanged depend on the bank size and the interleave size (as established by the bank size and interleave size switches). Note also that address bits 15 through 17 are only used for address comparison and recognition. Bits 18 through 31 eventually go to the L-register latches for core selection.

The logic also provides zeros in one or both of bits LC18S and LC19S for banks greater than 4K because the highest starting address that could occur in an 8K bank is defined by the four most significant bits. The highest starting address that could occur in a 12K or a 16K bank is defined by the three most significant bits.

Address modification and manipulation involve bits Lx18L, Lx19L, and Lx30L, Lx31L, respectively. These bits represent the two least significant and the two most significant bits that are latched into the L-register. Modification and manipulation are independent of each other.

Modification refers to inserting zeros into one or both bits 18 and 19 for bank sizes of 4K and 8K. Modification compensates for the varying address field required to address a different size bank. For example, any location in a 4K bank can be addressed by bits 20 through 31 of the address field. Thus, zeros are inserted in both bits 18 and 19. In a similar way, bit 18 becomes a zero for an 8K bank because any location in that bank can be addressed by bits 19 through 31. Address modification occurs whether or not interleaving is effected.

Address manipulation is the result of exchanging bits during address transformation for interleaving. One or both bits 30 and 31 are altered depending on the bit for which each was exchanged.

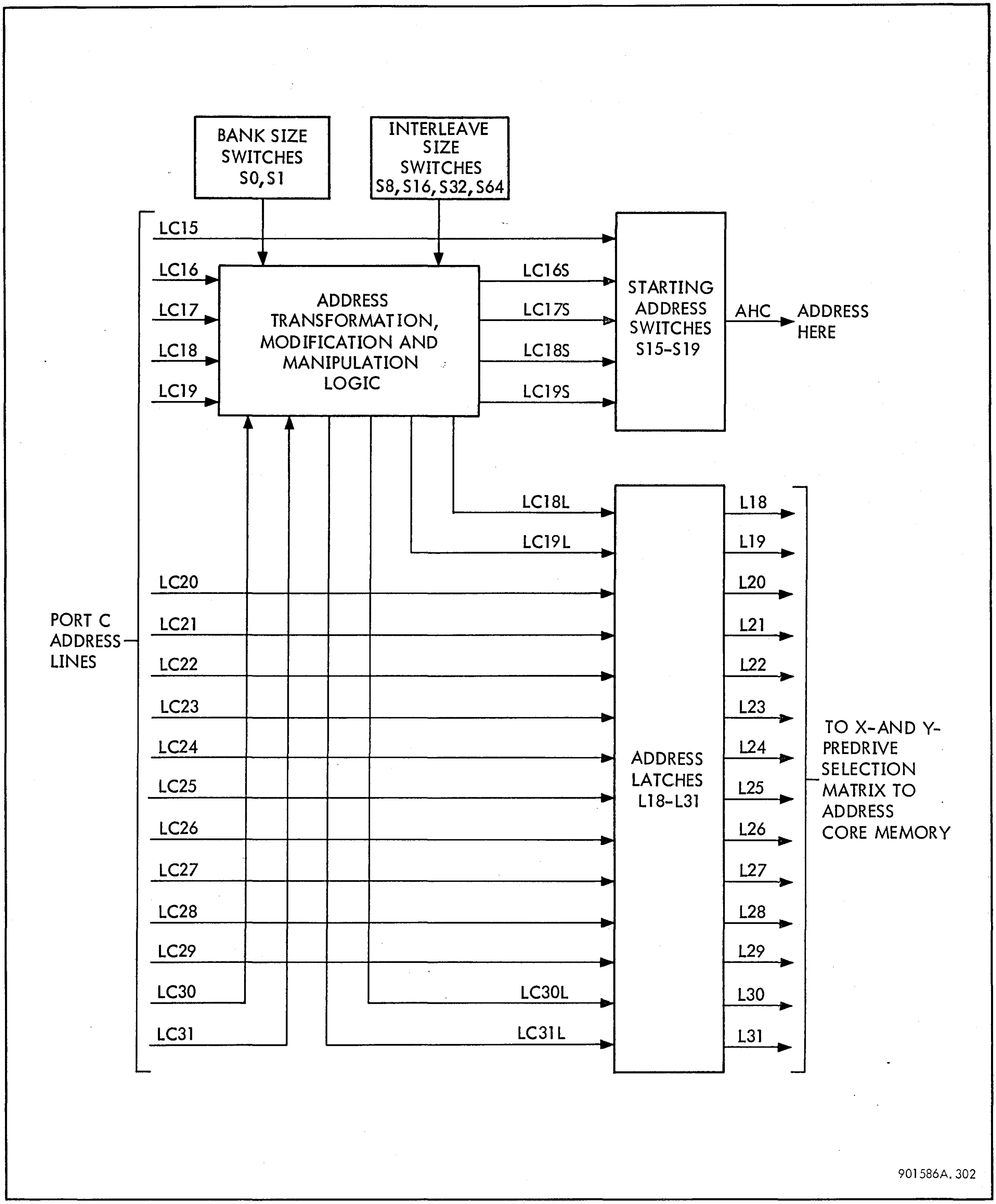


Figure 3-2. Address Transformation for Interleaving (Port C), Simplified Diagram

Table 3-1. Address Transformation, Modification, and Manipulation

TOTAL INTERLEAVE SIZE	BANK SIZE	ADDRESS INPUTS, PORT C*								
		Transformed Starting Address Bits					Modified Address Bits		Manipulated Address Bits	
		LC15	LC16S	LC17S	LC18S	LC19S	LC18L	LC19L	LC30L	LC31L
No Interleave	4K	LC15	LC16	LC17	LC18	LC19	0	0	LC30	LC31
	8K	LC15	LC16	LC17	LC18	0	0	LC19	LC30	LC31
	12K/16K	LC15	LC16	LC17	0	0	LC18	LC19	LC30	LC31
8K	4K	LC15	LC16	LC17	LC18	LC31	0	0	LC30	LC19
16K	4K	LC15	LC16	LC17	LC31	LC30	0	0	LC19	LC18
	8K	LC15	LC16	LC17	LC31	0	0	LC19	LC19	LC18
32K	4K	LC15	LC16	LC31	LC30	LC19	0	0	LC18	LC17
	8K	LC15	LC16	LC31	LC30	0	0	LC19	LC18	LC17
	16K	LC15	LC16	LC31	0	0	LC18	LC19	LC18	LC17
64K	8K	LC15	LC31	LC30	LC18	0	0	LC19	LC17	LC16
	16K	LC15	LC31	LC30	0	0	LC18	LC19	LC17	LC16

*Port C addressing is used here as an example. Addressing for ports A and B is similar

Figure 3-3 is an example of a memory configuration containing four banks with banks 2 and 3 interleaved. Table 3-2 shows the configuration of memory switches which are involved in addressing and which correspond to the memory bank configuration relative to bank size, address locations, and interleave size. Table 3-3 contains the interleave transformations which occur in an address sequence beginning with 16,000 (the starting address of the first bank in the interleaved group). For 16K interleave size and an 8K bank size, bits LC18 and LC19 are exchanged with bits LC31 and LC30, respectively (refer to table 3-1). Bit LC19S, however, becomes zero despite the exchange and the only bit affected relative to the starting address is bit LC18S.

Note that, as the sequence progresses, the banks that are activated by the interleaved address alternate between banks 2 and 3. This is because the bit configurations of LC15 through LC19S are alternately changed to reflect the starting address switch setup for banks 2 and 3 as shown in the upper part of the diagram. This is an example of modulo 2 interleaving because there are two transformations per interleave cycle. Modulo 4 interleaving occurs when there are four banks or eight banks of the same size in the interleave group. With eight banks in the group, the first four are accessed until exhausted, then the last four are accessed. Another significant point is that first the even numbered locations of each bank are addressed, then the odd numbered locations are addressed.

In figure 3-3, the access sequence occurs as follows: 0,2, 4,. . .24K-2,1,3,5. . .32K-1.

3-10 L-REGISTER (ADDRESS)

Figure 3-4 shows the L-register latches and the port C logic for interleaving and address recognition. Latch L20 is a typical latch and is shown in figure 3-4. Only the port C latch is shown. Note that the OR gate in the circuit is common to the latches for ports A and B. These are designated by signal name only; their gates are not shown. The term LXL0B and similar terms containing LXL are control signals used to latch and clear the L-register. Terms LXC0B, LXA0B, and LXB0B depend on their corresponding port, whose address has been recognized and whose access decision signal is high. L-register control is explained in paragraph 3-33. Latches similar to L20 are shown for L18 through L31. The interleave logic is also shown applied to the starting address switches. These paths form the address recognition logic and lead to the address here signal. Terms X8, X16, X32, and X64 in the interleave logic are derived from the interleave size switches, while terms S0 and S1 are set by the bank size switches. The results of this interleave logic are summarized in table 3-1.

The address here circuit for ports A and B is slightly different from that of port C. The inset in figure 3-4 shows this. Each of ports A and B have a port expander switch in series with the starting address switches.

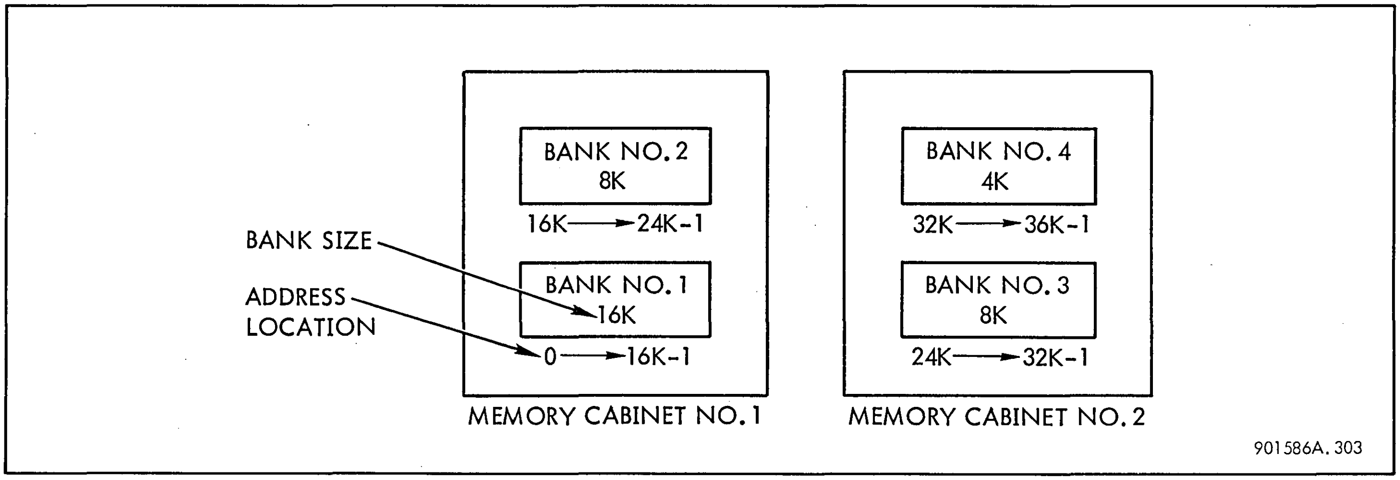


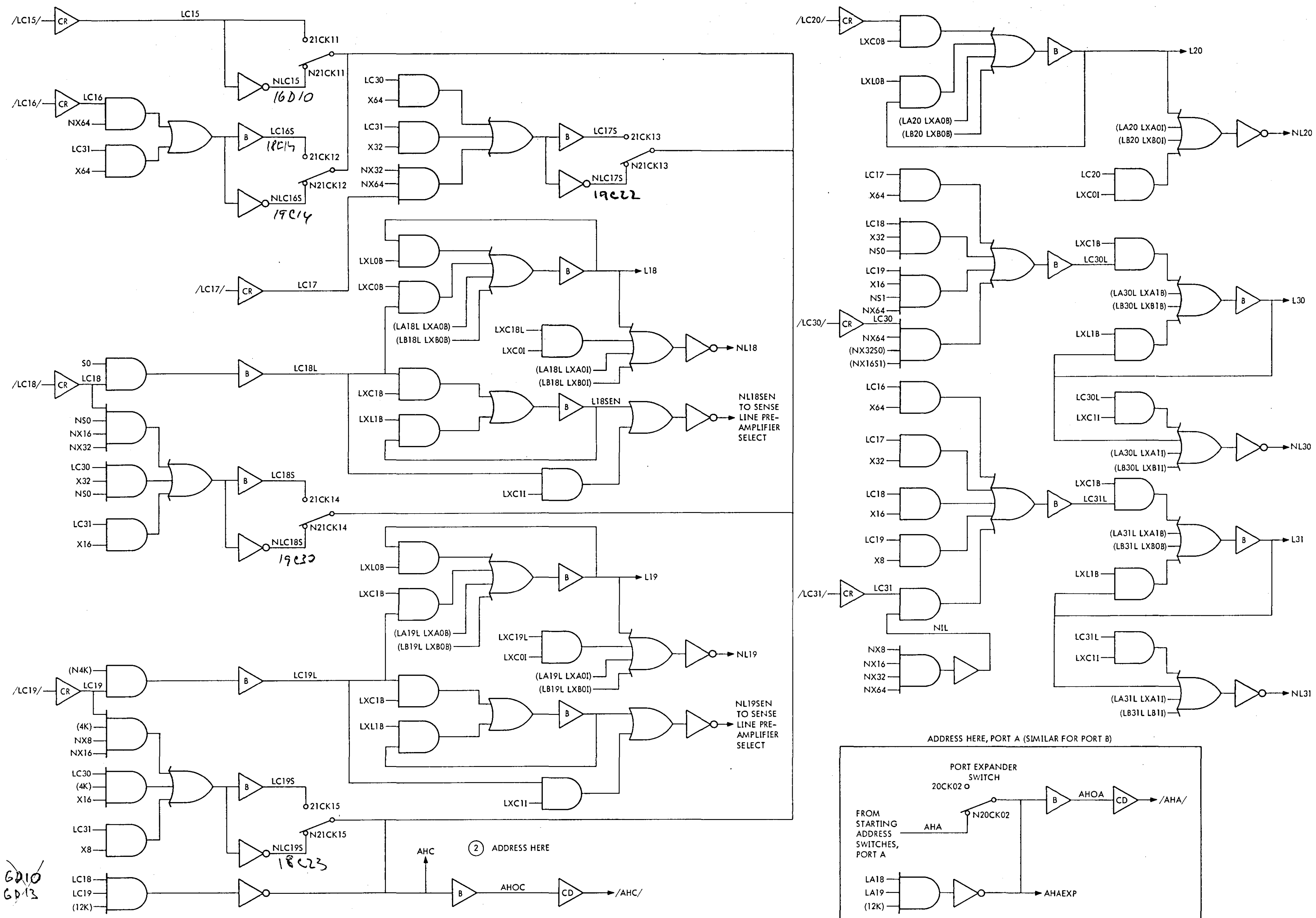
Figure 3-3. Example of a Four-Bank Memory with Banks 2 and 3 Interleaved

Table 3-2. Memory Switches for Addressing

BANK NUMBER	BANK SIZE SWITCHES		STARTING ADDRESS SWITCHES					INTERLEAVE SIZE SWITCHES			
	S0	S1	S15	S16	S17	S18	S19	S8	S16	S32	S64
1	1	1	0	0	0	0	0	0	0	0	0
2	0	1	0	0	1	0	0	0	1	0	0
3	0	1	0	0	1	1	0	0	1	0	0
4	0	0	0	1	0	0	0	0	0	0	0

Table 3-3. Interleave Transformation

ADDRESS LINE SEQUENCE	ADDRESS FIELD, PORT C								BANK NUMBER	BANK LOCATION
	(64K) LC15	(32K) LC16S	(16K) LC17S	(8K) LC18S	(4K) LC19S	. . .	(2) LC30L	(1) LC31L		
16,000	0	0	1	0	0	. . .	0	0		
Interleaved Address	0	0	1	0	0	. . .	0	0	2	0
16,001	0	0	1	0	0	. . .	0	1		
Interleaved Address	0	0	1	1	0	. . .	0	0	3	0
16,002	0	0	1	0	0	. . .	1	0		
Interleaved Address	0	0	1	0	0	. . .	1	0	2	2
16,003	0	0	1	0	0	. . .	1	1		
Interleaved Address	0	0	1	1	0	. . .	1	0	3	2



NOTES: 1. CIRCUITS L21 THROUGH L29 ARE SIMILAR TO L20
2 ADDRESS HERE, PORTS A AND B

Figure 3-4. L-Register Latches with Port C Interleave and Address Recognition Logic

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This switch provides a path to the port expander address here line if the port contains an expander. In that case, the address here signal (AHA or AHB) is taken from the port expander and the starting address switches shown in figure 3-4 are not in the circuit.

The two latch circuits shown in figure 3-4 provide addressing signals to the sense preamplifiers. These latches provide signals NL18SEN and NL19SEN which supply jumpered signals L18J and L19J, respectively. Terms L18J and L19J and L23J are used to select the proper preamplifier (via PASL0-PASL7) during core readout. See paragraphs 3-22 through 3-25 for a detailed description.

3-11 CORE SELECTION

Specific address bits in the L-register enable a pair of X-predrive switches and a pair of Y-predrive switches in the X- and Y-predrive matrices. The X- and Y-predrive switches are coupled to respective X- and Y-drive switches which provide current through the X- and Y-drive lines threaded through the cores. When each pair of X- and Y-predrive switches conduct, the corresponding X- and Y-drive switches are turned on and send current onto the respective drive lines through the core matrix. The cores at the X- and Y-intersections are the affected cores.

It is necessary to understand the drive switch operation before discussing the predrive arrangements. Therefore, in paragraph 3-12 a discussion of drive switch operation, similar for both X and Y, precedes the discussion of the X- and Y-predrive/drive matrix arrangements.

3-12 X- AND Y-DRIVE SYSTEM

To read or write a word, four X-current drivers (switches) and four X-voltage drivers (one current-voltage driver combination for each byte) are turned on simultaneously. At the same time, 33 Y-current drivers and 33 Y-voltage drivers (one current-voltage driver combination for each bit) are turned on simultaneously. Note that the X-drivers are byte oriented and the Y-drivers are bit oriented. A current-voltage driver combination consists of either a positive current switch and a negative voltage switch or a negative current switch and a positive voltage switch. One positive-negative combination of each pair is coupled through diodes to each drive line in the core matrix. (See figure 3-5.) If the first combination is selected to read a word from the cores (that is, on the first half memory cycle), then the second combination connected to the line is selected to write the word (or new word) back into the cores on the second half memory cycle. In figure 3-5, X-drivers are used to illustrate this explanation but the Y-drivers operate in a similar manner.

To pass a positive current through the drive wire, the positive current switch and negative voltage switch are turned on through transformer coupling with the corresponding X-predrive circuit. See figure 3-5. The current flows from the Vd (+22V) supply (figure 3-5, point Ⓓ) through the 53-ohm resistor and the positive current switch, through the diode (point Ⓐ) and drive wire, and through the negative voltage switch to ground.

To pass a negative current through the drive wire, the negative current switch and positive voltage switch are turned on. Current flows from the Vd (+22V) supply (figure 3-5, point Ⓔ), through the positive voltage switch and drive wire, through the diode (point Ⓑ), through the negative voltage switch and the 53-ohm resistor to ground. Voltage Vm (+11V) is not generated externally; rather, it is the result of thirty-seven 53-ohm divider chains (four X and 33 Y) passing current continuously through the VM clamp diodes. As indicated in the figure, each driver module contains coupling capacitors for Vm (+11V). The Vm (+11V) voltage is nominally +11V.

In the quiescent state, the 1 kilohm resistors connected to point Ⓒ in figure 3-5 bias all drive wires to the value of Vm (+11V). The 1 kilohm resistors connected to the current switches reverse-bias all of the diodes so that drive current is not lost into other lines as charging current. The Vm (+11V) clamp diodes prevent the voltage at the current switches (developed across the inductance of the drive line during the rise of current) from exceeding Vm (+11V). Thus, the decode diodes do not become forward biased.

All of the current and voltage switches are XDS 226 transistors coupled to the predrive matrices by transformers, each of which has a primary winding of one turn and a secondary winding of four turns. The magnetizing current is built up in the transformer during the time that the transistor is conducting and serves to turn off the transistor when the base drive is removed.

To provide heat dissipation, the 53-ohm resistors shown in figure 3-5 are located in the top chassis of the cabinet beneath the cooling fans. Connection to the resistors is made through a twisted pair of wires that minimizes the inductance of the drive loop.

3-13 X-PREDRIVE MATRIX

Each memory bank has four X-predrive matrices, one matrix for each type of X-drive switch as follows:

a. X-negative current predrive matrix

b. X-positive current predrive matrix

c. X-negative voltage predrive matrix

d. X-positive voltage predrive matrix

Figure 3-6 shows a simplified diagram of the X-negative current predrive matrix. This matrix is a four by four arrangement of current drive switches (that is, XNCD0, . . .) and current drivers (XNCK0, . . .). Each predrive circuit contains four transformers which couple the predrive circuit to four X-drivers (0XCON, 1XCON, . . .).

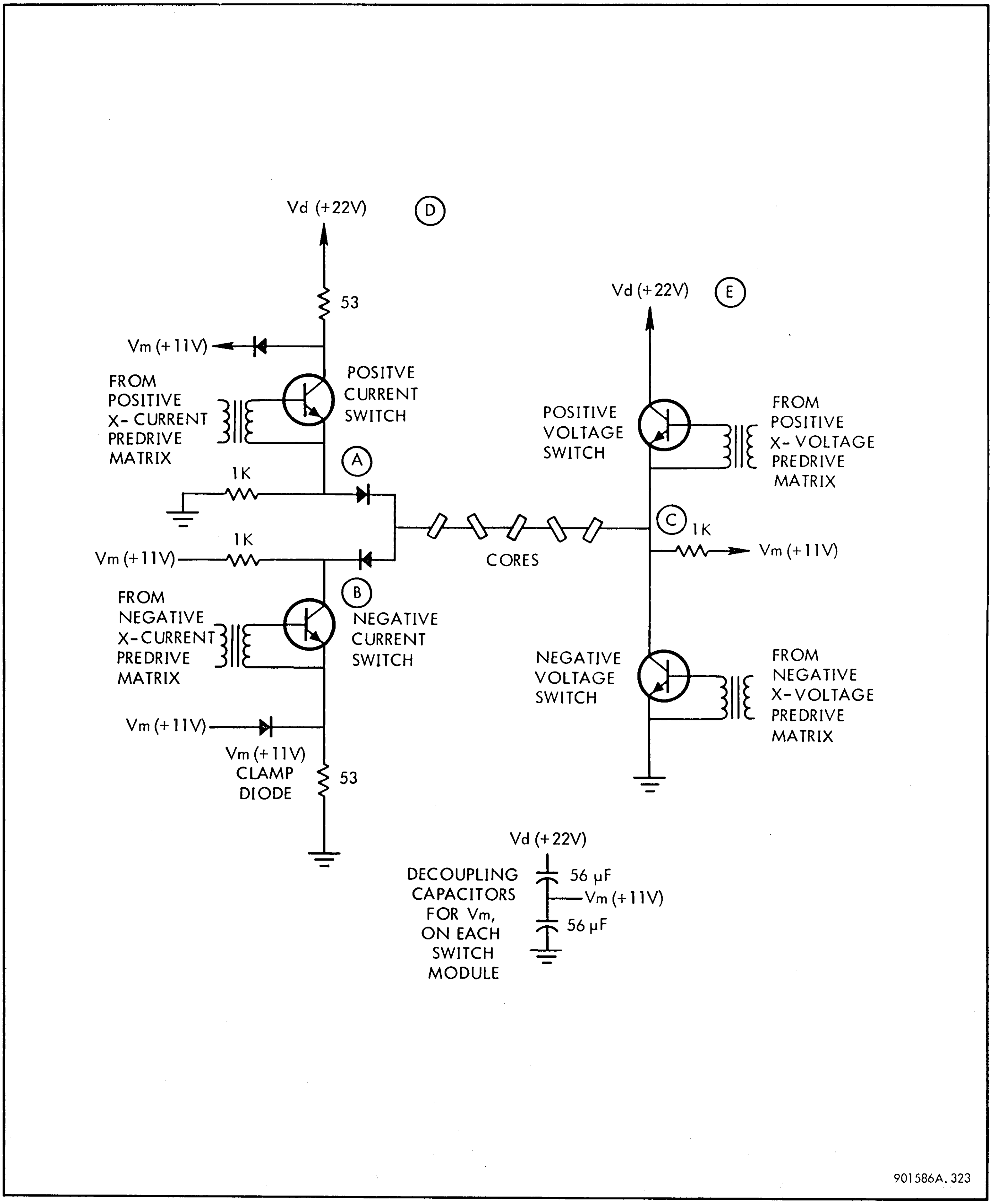


Figure 3-5. Memory Core Drive System, Simplified Schematic Diagram

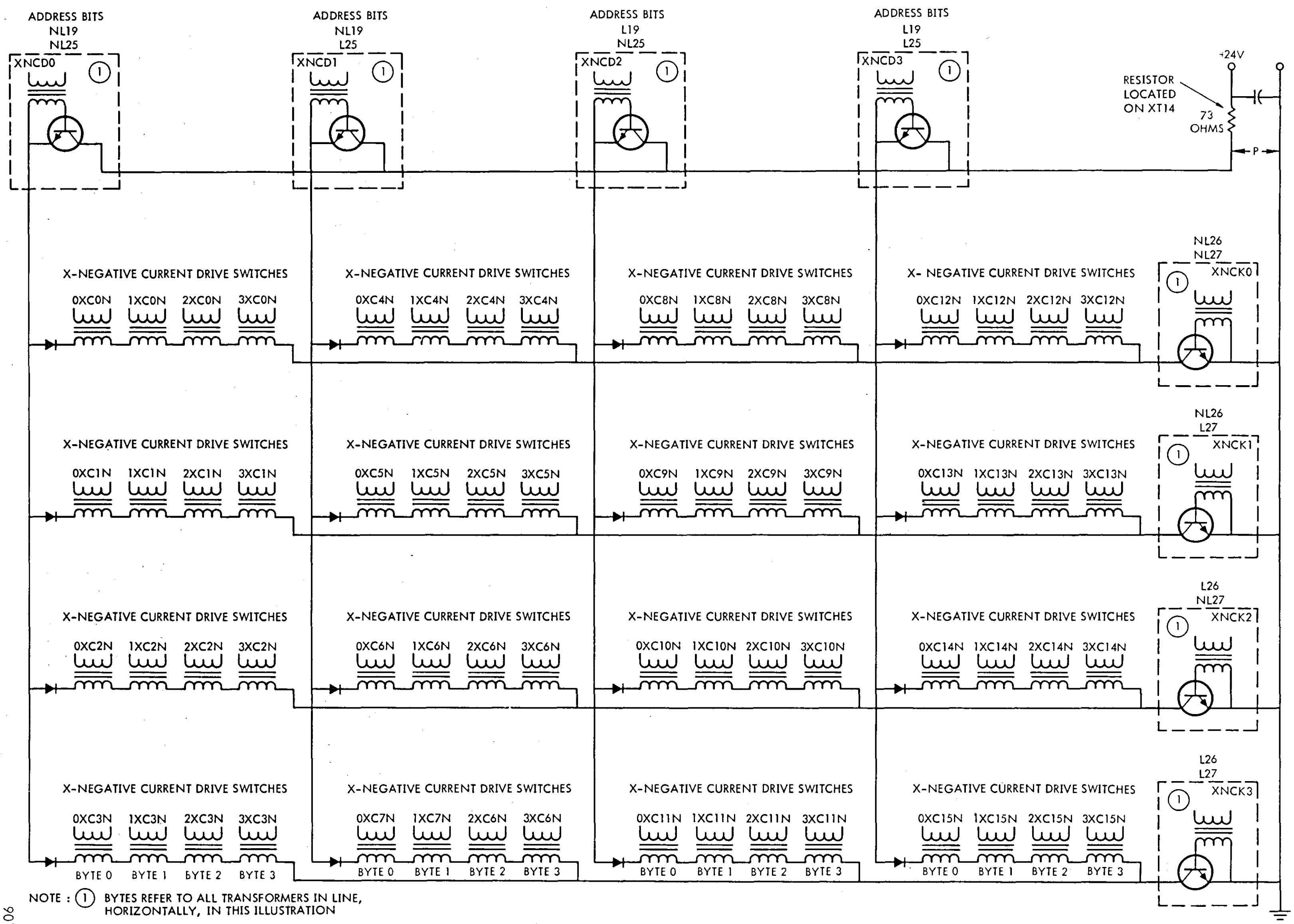
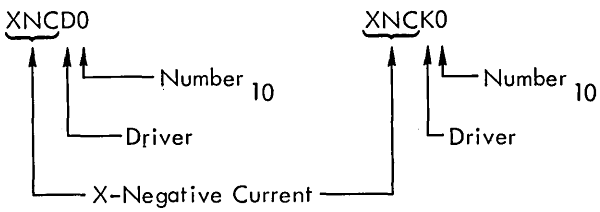


Figure 3-6. X-Negative Current Predrive Matrix, Simplified Schematic Diagram

Only the transformers are shown in figure 3-6; the drivers are omitted. A predrive switch can be easily identified in the logic equations and other documentation since all use a similar syntax as shown in the following example.



As indicated in figure 3-6, address bits L19, L25, L26, and L27 select the predrive current drivers. One other input to the predrive switches is a timing signal not shown in the figure. This timing signal, time for negative X-current (TNXC), is applied to each predrive switch. Since all combinations of the given address bits are applied to the predrive switches, one current driver pair is always addressed. When TNXC is true, the addressed current driver pair is turned on and the respective driver transformers in the circuit are energized. Thus, the four X-drivers coupled by the transformers are turned on. However, this only represents one-half of the drive circuit. For this example, a pair of switches in the positive voltage predrive matrix would also be turned on by timing signal TPXV. The four respective X-positive voltage drivers connected at the other end of the selected drive lines (opposite the negative current drivers) would be energized, and the drive circuit would be complete. The complete circuit is described in paragraph 3-14.

Figure 3-6 correlates with figures 3-7 through 3-10. These charts show all of the predrivers, and the drivers which they control, in a 16K bank. Module locations and pin numbers for each predrive and drive switch output are also shown in the charts. An X-driver can easily be identified by its symbol as indicated in figures 3-7 or 3-8. This is self-explanatory except for the term bus which has not been introduced. Bus, in this case, refers to all of the X-lines connected to a driver through diodes. Since there are 16 negative current drivers there are 16 negative current buses. Likewise, there are 16 positive current buses. However, a 16K bank contains 32 positive voltage drivers and 32 negative voltage drivers, as shown in figures 3-9 and 3-10. Again, the number of voltage buses matches the number of voltage drivers.

Figures 3-7 and 3-8 also contain a diagram relating X-current direction to address bits L22 and L25 for reading and writing. Reading is performed during the first portion of every memory cycle and writing is performed during the last portion. Therefore, the current in a selected drive line is reversed once during every memory cycle. Current direction is a function of the timing signals, and the timing signals for X-drive are a function of address bits L22 and L25. The diagrams in figures 3-7 and 3-8 show the X-current direction between drivers for all conditions. Conventional current flow (positive to negative) is assumed.

Note that both current predrive matrices and both voltage predrive matrices are addressed identically. If bits L22 and L25 are not alike for any given address (figure 3-8), timing signals TPXC and TNXV go true during the read portion of the cycle and the positive current predrive matrix and negative voltage predrive matrix are selected. Current flows from the XPCS driver to the XNVS driver. Current is reversed during the write portion of the cycle (from an XNCS driver to an XPVS driver) because timing signals TNXC and TPXV go true.

3-14 X-DRIVE

Figure 3-11 shows one X-drive configuration to drive current in one direction through selected lines in the core matrix. In this configuration, the drive circuits consist of a negative current switch and a positive voltage switch arrangement for one stack of core diode modules. The drivers (ST10 modules) are turned on by their respective X-predrive switches (ST22 modules). The predrive switches, selected by the address bits on their input gates, are turned on when the timing signal (TNXC for current and TPXV for voltage) goes true. The four driver switches in each of the predrive circuits are turned on.

In this example, the current flows through the cores as follows: From voltage supply Vd (+22V) in the positive voltage drive switches, through the active transistor switch, up through the core diode module, through the diode, down through the transistor in the negative current drive switch, through the diode and resistor to ground. On the ST10 module containing the voltage drive switches, note that each circuit has two transistor switches. The upper switch, active in this example, is the X-positive voltage drive switch. The lower switch is the negative voltage switch connected to the drive line.

To drive current in the opposite direction through the line, current from the positive current drive switch connected to the line at point Ⓐ in figure 3-11 is driven down through the core-diode module and through the negative voltage switch to ground. The positive current switches connected to the line at point Ⓐ in this example are 0XCOP, 1XCOP, 2XCOP, and 3XCOP, respectively.

3-15 Y-PREDRIVE-DRIVE ARRANGEMENT

Each 16K bank has 32 Y-predrive switch arrangements as follows:

a. Eight Y-positive current predrive switches

b. Eight Y-negative current predrive switches

c. Eight Y-positive voltage predrive switches

d. Eight Y-negative voltage predrive switches

Since the Y-drive system is bit oriented, 33 positive and 33 negative Y-switches (and four X-drive switches) are turned on simultaneously to access one word.

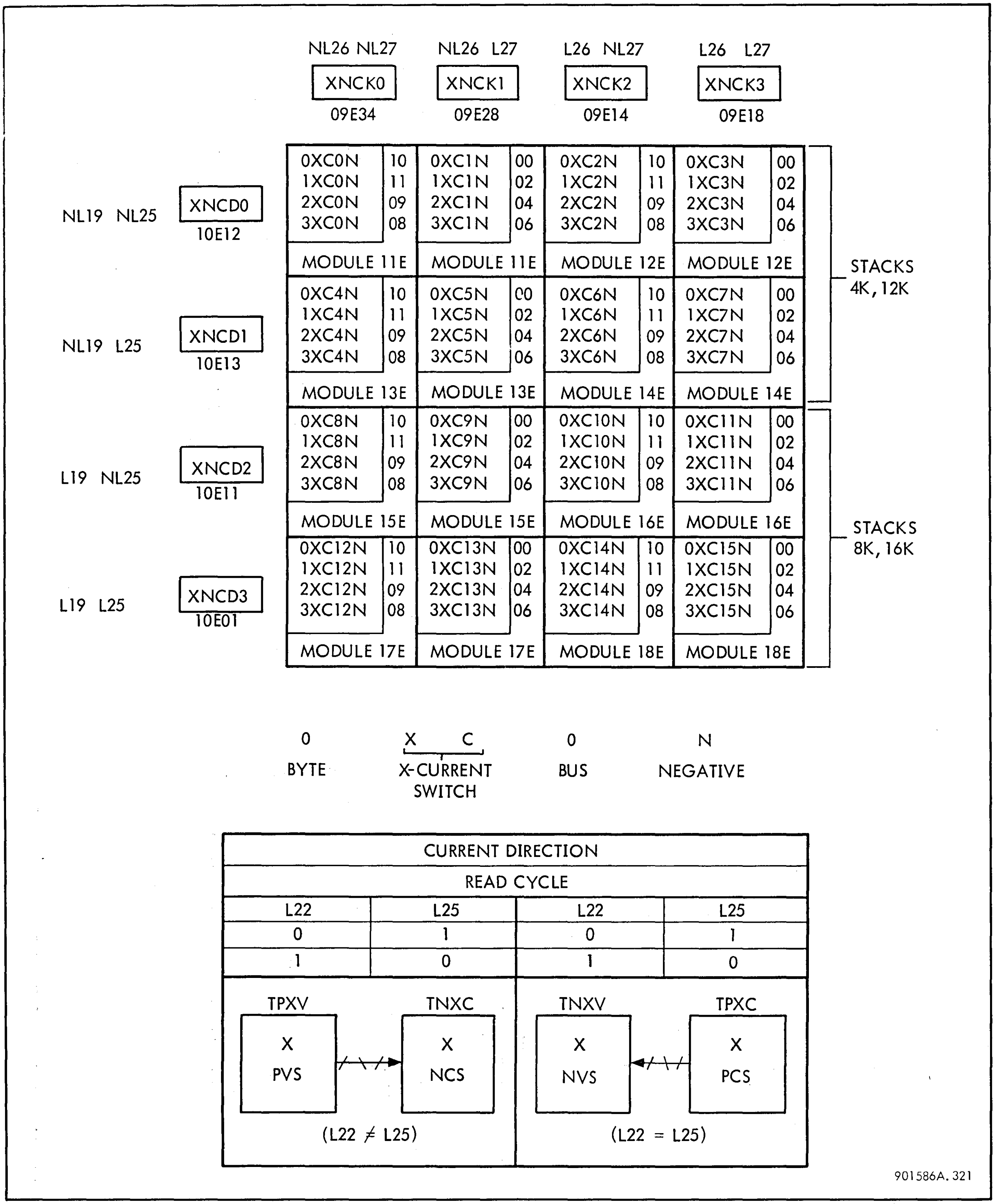


Figure 3-7. X-Negative Current Predrive Matrix

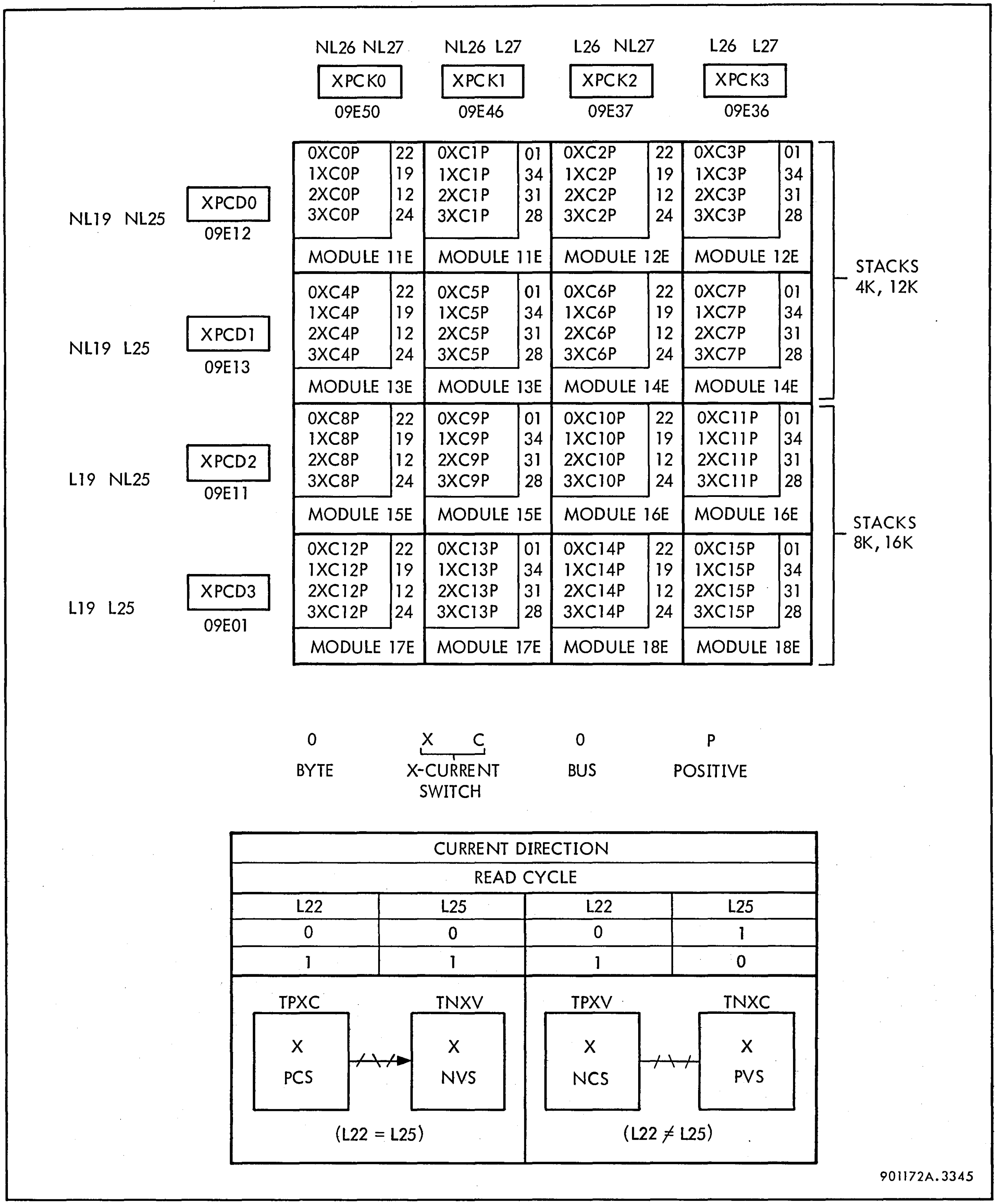


Figure 3-8. X-Positive Current Predrive Matrix

		NL18 NL28 NL29 XPVD0 07E12	NL18 NL28 L29 XPVD1 07E13	NL18 L28 NL29 XPVD2 07E11	NL18 L28 L29 XPVD3 07E01	L18 NL28 NL29 XPVD4 05E12	L18 NL28 L29 XPVD5 05E13	L18 L28 NL29 XPVD6 05E11	L18 L28 L29 XPVD7 05E01
NL30 NL31	XPVK0 10E50	0XV0 48 1XV0 50 2XV0 47 3XV0 49 MODULE 11E	0XV4 48 1XV4 50 2XV4 47 3XV4 49 MODULE 13E	0XV8 48 1XV8 50 2XV8 47 3XV8 49 MODULE 15E	0XV12 48 1XV12 50 2XV12 47 3XV12 49 MODULE 17E	0XV16 48 1XV16 50 2XV16 47 3XV16 49 MODULE 19E	0XV20 48 1XV20 50 2XV20 47 3XV20 49 MODULE 21E	0XV24 48 1XV24 50 2XV24 47 3XV24 49 MODULE 23E	0XV28 48 1XV28 50 2XV28 47 3XV28 49 MODULE 25E
NL30 L31	XPVK1 10E46	0XV1 46 1XV1 45 2XV1 40 3XV1 39 MODULE 11E	0XV5 46 1XV5 45 2XV5 40 3XV5 39 MODULE 13E	0XV9 46 1XV9 45 2XV9 40 3XV9 39 MODULE 15E	0XV13 46 1XV13 45 2XV13 40 3XV13 39 MODULE 17E	0XV17 46 1XV17 45 2XV17 40 3XV17 39 MODULE 19E	0XV21 46 1XV21 45 2XV21 40 3XV21 39 MODULE 21E	0XV25 46 1XV25 45 2XV25 40 3XV25 39 MODULE 23E	0XV29 46 1XV29 45 2XV29 40 3XV29 39 MODULE 25E
L30 NL31	XPVK2 10E37	0XV2 48 1XV2 50 2XV2 47 3XV2 49 MODULE 12E	0XV6 48 1XV6 50 2XV6 47 3XV6 49 MODULE 14E	0XV10 48 1XV10 50 2XV10 47 3XV10 49 MODULE 16E	0XV14 48 1XV14 50 2XV14 47 3XV14 49 MODULE 18E	0XV18 48 1XV18 50 2XV18 47 3XV18 49 MODULE 20E	0XV22 48 1XV22 50 2XV22 47 3XV22 49 MODULE 22E	0XV26 48 1XV26 50 2XV26 47 3XV26 49 MODULE 24E	0XV30 48 1XV30 50 2XV30 47 3XV30 49 MODULE 26E
L30 L31	XPVK3 10E36	0XV3 46 1XV3 45 2XV3 40 3XV3 39 MODULE 12E	0XV7 46 1XV7 45 2XV7 40 3XV7 39 MODULE 14E	0XV11 46 1XV11 45 2XV11 40 3XV11 39 MODULE 16E	0XV15 46 1XV15 45 2XV15 40 3XV15 39 MODULE 18E	0XV19 46 1XV19 45 2XV19 40 3XV19 39 MODULE 20E	0XV23 46 1XV23 45 2XV23 40 3XV23 39 MODULE 22E	0XV27 46 1XV27 45 2XV27 40 3XV27 39 MODULE 24E	0XV31 46 1XV31 45 2XV31 40 3XV31 39 MODULE 26E

STACKS 4K,8K (XPVD0–XPVD3) STACKS 12K,16K (XPVD4–XPVD7)

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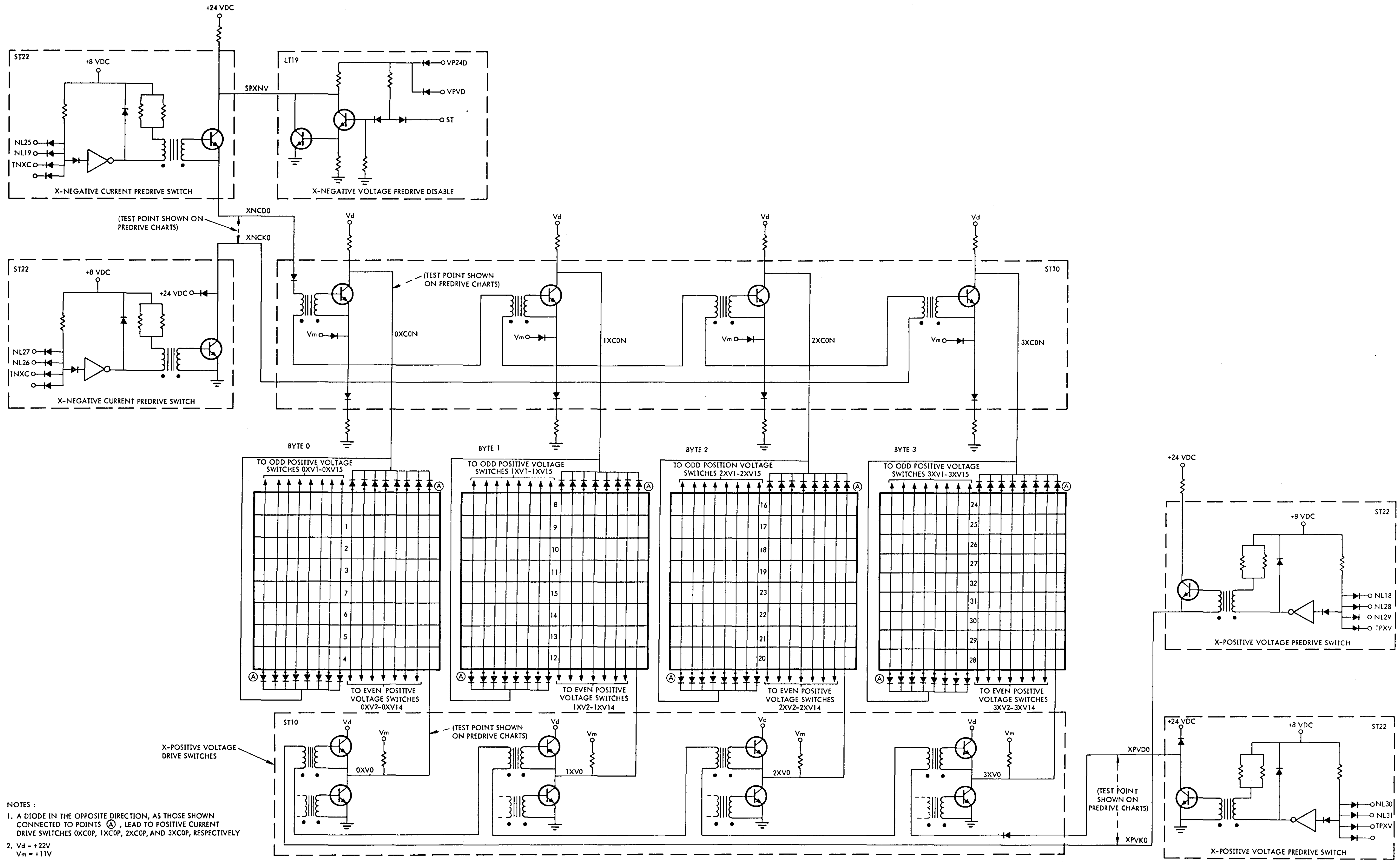
Figure 3-9. X-Positive Voltage Predrive Matrix

		NL18 NL28 NL29 XNVD0 08E12	NL18 NL28 L29 XNVD1 08E13	NL18 L28 NL29 XNVD2 08E11	NL18 L28 L29 XNVD3 08E01	L18 NL28 NL29 XNVD4 06E12	L18 NL28 L29 XNVD5 06E13	L18 L28 NL29 XNVD6 06E11	L18 L28 L29 XNVD7 06E01
NL30 NL31	XNVK0 10E34	0XV0 48 1XV0 50 2XV0 47 3XV0 49 MODULE 11E	0XV4 48 1XV4 50 2XV4 47 3XV4 49 MODULE 13E	0XV8 48 1XV8 50 2XV8 47 3XV8 49 MODULE 15E	0XV12 48 1XV12 50 2XV12 47 3XV12 49 MODULE 17E	0XV16 48 1XV16 50 2XV16 47 3XV16 49 MODULE 19E	0XV20 48 1XV20 50 2XV20 47 3XV20 49 MODULE 21E	0XV24 48 1XV24 50 2XV24 47 3XV24 49 MODULE 23E	0XV28 48 1XV28 50 2XV28 47 3XV28 49 MODULE 25E
NL30 L31	XNVK1 10E28	0XV1 46 1XV1 45 2XV1 40 3XV1 39 MODULE 11E	0XV5 46 1XV5 45 2XV5 40 3XV5 39 MODULE 13E	0XV9 46 1XV9 45 2XV9 40 3XV9 39 MODULE 15E	0XV13 46 1XV13 45 2XV13 40 3XV13 39 MODULE 17E	0XV17 46 1XV17 45 2XV17 40 3XV17 39 MODULE 19E	0XV21 46 1XV21 45 2XV21 40 3XV21 39 MODULE 21E	0XV25 46 1XV25 45 2XV25 40 3XV25 39 MODULE 23E	0XV29 46 1XV29 45 2XV29 40 3XV29 39 MODULE 25E
L30 NL31	XNVK2 10E14	0XV2 48 1XV2 50 2XV2 47 3XV2 49 MODULE 12E	0XV6 48 1XV6 50 2XV6 47 3XV6 49 MODULE 14E	0XV10 48 1XV10 50 2XV10 47 3XV10 49 MODULE 16E	0XV14 48 1XV14 50 2XV14 47 3XV14 49 MODULE 18E	0XV18 48 1XV18 50 2XV18 47 3XV18 49 MODULE 20E	0XV22 48 1XV22 50 2XV22 47 3XV22 49 MODULE 22E	0XV26 48 1XV26 50 2XV26 47 3XV26 49 MODULE 24E	0XV30 48 1XV30 50 2XV30 47 3XV30 49 MODULE 26E
L30 L31	XNVK3 10E18	0XV3 46 1XV3 45 2XV3 40 3XV3 39 MODULE 12E	0XV7 46 1XV7 45 2XV7 40 3XV7 39 MODULE 14E	0XV11 46 1XV11 45 2XV11 40 3XV11 39 MODULE 16E	0XV15 46 1XV15 45 2XV15 40 3XV15 39 MODULE 18E	0XV19 46 1XV19 45 2XV19 40 3XV19 39 MODULE 20E	0XV23 46 1XV23 45 2XV23 40 3XV23 39 MODULE 22E	0XV27 46 1XV27 45 2XV27 40 3XV27 39 MODULE 24E	0XV31 46 1XV31 45 2XV31 40 3XV31 39 MODULE 26E

STACKS 4K, 8K (XNVD0–XNVD3) STACKS 12,16K (XNVD4–XNVD7)

901172A. 3348

Figure 3-10. X-Negative Voltage Predrive Matrix



NOTES :

1. A DIODE IN THE OPPOSITE DIRECTION, AS THOSE SHOWN CONNECTED TO POINTS (A), LEAD TO POSITIVE CURRENT DRIVE SWITCHES 0XC0P, 1XC0P, 2XC0P, AND 3XC0P, RESPECTIVELY
2. Vd = +22V
   Vm = +11V

Figure 3-11. X-Current Predrive-Drive Schematic Diagram

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Figure 3-12 is a simplified diagram of the Y-positive current predrive-drive arrangement. Other Y-predrive and drive switches are arranged in a similar way. The Y-drivers are coupled in groups of four (on ST11 modules) to predrive transformers connected in series. Thus, 33 Y-drive switches are turned on by one predrive current. Note that when the predrive transistor conducts, current flows from the +24V supply through the 32-ohm resistor and diode, through the transformer primary windings, and down through the predrive transistor switch to ground. Three address bits and a timing signal (TPYC in this example) turn on the predrive switch. The predrive switch is a power transistor which drives approximately 300 mA into the series string of 33 drive switch primaries.

Figures 3-13, 3-14, and 3-15 are charts showing the Y-predrive-drive arrangement for all Y-drivers in a 16K bank. Note that the Y-positive current predrive switches and Y-negative current predrive switches are addressed by the same address bits. This is also true for the Y-positive voltage and Y-negative voltage predrive switches. Like the X-predrive arrangement, the addressed predrive switches are turned on when the respective timing signal goes true. As indicated in figures 3-13 and 3-14, the Y-timing signals are a function of address bits L22, L23 and L25. The diagrams at the bottom of these figures indicate the current direction for all possible conditions.

3-16 Y-DRIVE

Figure 3-16 shows one Y-drive arrangement to access a set of Y-drive lines during a read or a write portion of a memory cycle. In this configuration, the drive circuits consist of 33 Y-positive current switches and 33 Y-negative voltage switches. By tracing the line from driver 00YC0P, it is seen that current flows from the Vd (+22V) supply through positive current driver 00YC0P, through a loop in bit 0 of byte 0 core diode module, down through Y-negative voltage switch 00YV0 to ground. Similar to the X-drivers, the other switch shown at 00YV0 is the positive voltage switch connected to the line. Current is reversed in the same Y-line during the alternate portion of the memory cycle. At this time, current flows from Vd (+22V) at 00YV0, up through the drive loop in bit 0 of byte 0 and goes to ground through a negative current switch not shown on this diagram. In this example, the negative current switch would be numbered 00YC0N and would be coupled to the line through a diode in the opposite direction from the diodes shown in the diagram. All of the other Y-drivers operate in a similar manner.

3-17 Y-INHIBIT

As a result of reading data during the read portion of a memory cycle, all of the selected cores are set to zero. Cores which have been zero remain zero, and those which have contained ones are switched to zero. Therefore, when writing data into the cores during the write portion of the memory cycle, it is only necessary to write ones in those cores which are to contain ones, that is, those cores which correspond to ones in the M-register.

To write a zero (or not write a one) in a particular bit, the Y-current is inhibited for that bit. This is accomplished by the Y-inhibit drivers. Figure 3-17 is a simplified schematic diagram of a typical Y-inhibit circuit, connected across a set of Y-drive switches. The inhibit circuit, an ST21 module, is internally identical to an ST22 predrive circuit. The M-register data bit containing a zero is inverted and gated to the inhibit driver with timing signal TPYI (time for positive Y-inhibit) or TNYI (time for negative Y-inhibit). Whenever an inhibit driver conducts, Y-current is short-circuited to ground through the inhibit driver.

3-18 CORE DIODE MODULE

A core diode module is made of two glass epoxy circuit boards on which a magnetic core array, decode diodes, and temperature sensing diodes are mounted. The circuit boards are hinged together to form a complete core diode module. Connections to the drive and sense electronics are made through 208 printed circuit contacts at the edge of the boards. Figure 3-18 shows a photograph of a core diode module lying open to expose the magnetic core array and the printed circuit wiring for the diodes. The 128 X-wires can be seen jumpered across the hinge. Individual magnetic cores in the array are too small to be seen in the photograph. As shown in figure 3-19, the module is folded when it is inserted in the chassis in the memory bank. The core diode module is completely symmetrical. That is, when folded, the module is operable whichever way it is inserted in the chassis. One-half of the decode diodes and one temperature sensing diode can be seen in this view.

3-19 MAGNETIC CORE ARRAY

The magnetic core array consists of eight bit planes or nine bit planes depending on the type of module. Figure 3-20 is a diagram of a module having nine bit planes. Each bit plane has 4096 cores and represents one bit (for example, bit 0) of 4096 words. A module containing eight bit planes (an eight-bit module) has 32,768 ferrite cores and 512 decode diodes. A nine-bit module has 36,864 ferrite cores and 544 decode diodes. The eight-bit modules are used for bytes 0, 1, and 2. The nine-bit modules are used for byte 3; the extra bit stores the parity bit. All core-diode modules have two temperature-sensing diodes.

The magnetic core array is arranged for coincident current operation with three wires linking each core, an X-drive wire, a Y-drive wire, and a sense wire. There is no inhibit wire. Figure 3-21 is a simplified diagram of the core array for bit plane 0. Not all of the cores are shown and only two X-wires and one Y-line are indicated. The drawing indicates the relation between the wires linking the cores and the wire paths through the cores. In a complete module the X-drive wires originate on one end of the circuit boards, cross over at the hinge, and terminate on the other board. Two diodes on one end of each X-wire are used to decode the line during operation. One of the diodes couples the wire to a positive current driver; the other diode couples the wire to a negative current driver.

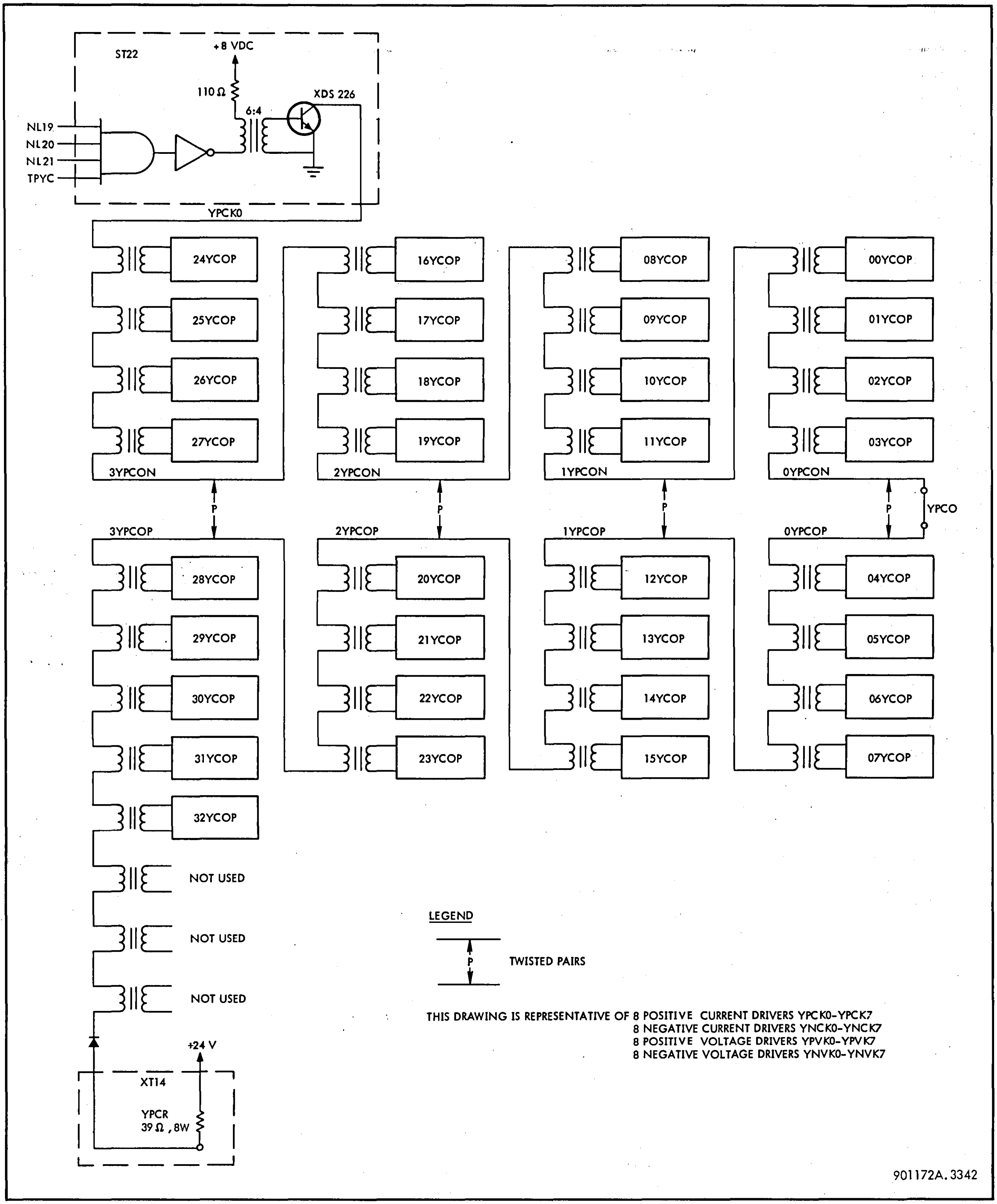

Figure 3-12. Y-Positive Current Predrive-Drive Coupling, Simplified Schematic Diagram

NL19
NL20
NL21
YPCK0

0YPC0N	0YPC0P	1YPC0N	1YPC0P	2YPC0N	2YPC0P	3YPC0N	3YPC0P	
00YC0P 22	04YC0P 22	08YC0P 22	12YC0P 22	16YC0P 22	20YC0P 22	24YC0P 22	28YC0P 22	32YC0P 22
01YC0P 19	05YC0P 19	09YC0P 19	13YC0P 19	17YC0P 19	21YC0P 19	25YC0P 19	29YC0P 19	NOT USED
02YC0P 12	06YC0P 12	10YC0P 12	14YC0P 12	18YC0P 12	22YC0P 12	26YC0P 12	30YC0P 12	NOT USED
03YC0P 24	07YC0P 24	11YC0P 24	15YC0P 24	19YC0P 24	23YC0P 24	27YC0P 24	31YC0P 24	NOT USED
MODULE 32F	MODULE 31F	MODULE 24F	MODULE 23F	MODULE 16F	MODULE 15F	MODULE 08F	MODULE 07F	MODULE 04E

NL19
NL20
L21
YPCK1

0YPC1N	0YPC1P	1YPC1N	1YPC1P	2YPC1N	2YPC1P	3YPC1N	3YPC1P	
00YC1P 01	04YC1P 01	08YC1P 01	12YC1P 01	16YC1P 01	20YC1P 01	24YC1P 01	28YC1P 01	32YC1P 01
01YC1P 34	05YC1P 34	09YC1P 34	13YC1P 34	17YC1P 34	21YC1P 34	25YC1P 34	29YC1P 34	NOT USED
02YC1P 31	06YC1P 31	10YC1P 31	14YC1P 31	18YC1P 31	22YC1P 31	26YC1P 31	30YC1P 31	NOT USED
03YC1P 28	07YC1P 28	11YC1P 28	15YC1P 28	19YC1P 28	23YC1P 28	27YC1P 28	31YC1P 28	NOT USED
MODULE 32F	MODULE 31F	MODULE 24F	MODULE 23F	MODULE 16F	MODULE 15F	MODULE 08F	MODULE 07F	MODULE 04E

NL19
L20
NL21
YPCK2

0YPC2N	0YPC2P	1YPC2N	1YPC2P	2YPC2N	2YPC2P	3YPC2N	3YPC2P	
00YC2P 22	04YC2P 22	08YC2P 22	12YC2P 22	16YC2P 22	20YC2P 22	24YC2P 22	28YC2P 22	32YC2P 22
01YC2P 19	05YC2P 19	09YC2P 19	13YC2P 19	17YC2P 19	21YC2P 19	25YC2P 19	29YC2P 19	NOT USED
02YC2P 12	06YC2P 12	10YC2P 12	14YC2P 12	18YC2P 12	22YC2P 12	26YC2P 12	30YC2P 12	NOT USED
03YC2P 24	07YC2P 24	11YC2P 24	15YC2P 24	19YC2P 24	23YC2P 24	27YC2P 24	31YC2P 24	NOT USED
MODULE 30F	MODULE 29F	MODULE 22F	MODULE 21F	MODULE 14F	MODULE 13F	MODULE 06F	MODULE 05F	MODULE 03E

NL19
L20
L21
YPCK3

0YPC3N	0YPC3P	1YPC3N	1YPC3P	2YPC3N	2YPC3P	3YPC3N	3YPC3P	
00YC3P 01	04YC3P 01	08YC3P 01	12YC3P 01	16YC3P 01	20YC3P 01	24YC3P 01	28YC3P 01	32YC3P 01
01YC3P 34	05YC3P 34	09YC3P 34	13YC3P 34	17YC3P 34	21YC3P 34	25YC3P 34	29YC3P 34	NOT USED
02YC3P 31	06YC3P 31	10YC3P 31	14YC3P 31	18YC3P 31	22YC3P 31	26YC3P 31	30YC3P 31	NOT USED
03YC3P 28	07YC3P 28	11YC3P 28	15YC3P 28	19YC3P 28	23YC3P 28	27YC3P 28	31YC3P 28	NOT USED
MODULE 30F	MODULE 29F	MODULE 22F	MODULE 21F	MODULE 14F	MODULE 13F	MODULE 06F	MODULE 05F	MODULE 03E

L19
NL20
NL21
YPCK4

0YPC4N	0YPC4P	1YPC4N	1YPC4P	2YPC4N	2YPC4P	3YPC4N	3YPC4P	
00YC4P 22	04YC4P 22	08YC4P 22	12YC4P 22	16YC4P 22	20YC4P 22	24YC4P 22	28YC4P 22	32YC4P 22
01YC4P 19	05YC4P 19	09YC4P 19	13YC4P 19	17YC4P 19	21YC4P 19	25YC4P 19	29YC4P 19	NOT USED
02YC4P 12	06YC4P 12	10YC4P 12	14YC4P 12	18YC4P 12	22YC4P 12	26YC4P 12	30YC4P 12	NOT USED
03YC4P 24	07YC4P 24	11YC4P 24	15YC4P 24	19YC4P 24	23YC4P 24	27YC4P 24	31YC4P 24	NOT USED
MODULE 28F	MODULE 27F	MODULE 20F	MODULE 19F	MODULE 12F	MODULE 11F	MODULE 04F	MODULE 03F	MODULE 02E

L19
NL20
L21
YPCK5

0YPC5N	0YPC5P	1YPC5N	1YPC5P	2YPC5N	2YPC5P	3YPC5N	3YPC5P	
00YC5P 01	04YC5P 01	08YC5P 01	12YC5P 01	16YC5P 01	20YC5P 01	24YC5P 01	28YC5P 01	32YC5P 01
01YC5P 34	05YC5P 34	09YC5P 34	13YC5P 34	17YC5P 34	21YC5P 34	25YC5P 34	29YC5P 34	NOT USED
02YC5P 31	06YC5P 31	10YC5P 31	14YC5P 31	18YC5P 31	22YC5P 31	26YC5P 31	30YC5P 31	NOT USED
03YC5P 28	07YC5P 28	11YC5P 28	15YC5P 28	19YC5P 28	23YC5P 28	27YC5P 28	31YC5P 28	NOT USED
MODULE 28F	MODULE 27F	MODULE 20F	MODULE 19F	MODULE 12F	MODULE 11F	MODULE 04F	MODULE 03F	MODULE 02E

L19
L20
NL21
YPCK6

0YPC6N	0YPC6P	1YPC6N	1YPC6P	2YPC6N	2YPC6P	3YPC6N	3YPC6P	
00YC6P 22	04YC6P 22	08YC6P 22	12YC6P 22	16YC6P 22	20YC6P 22	24YC6P 22	28YC6P 22	32YC6P 22
01YC6P 19	05YC6P 19	09YC6P 19	13YC6P 19	17YC6P 19	21YC6P 19	25YC6P 19	29YC6P 19	NOT USED
02YC6P 12	06YC6P 12	10YC6P 12	14YC6P 12	18YC6P 12	22YC6P 12	26YC6P 12	30YC6P 12	NOT USED
03YC6P 24	07YC6P 24	11YC6P 24	15YC6P 24	19YC6P 24	23YC6P 24	27YC6P 24	31YC6P 24	NOT USED
MODULE 26F	MODULE 25F	MODULE 18F	MODULE 17F	MODULE 10F	MODULE 09F	MODULE 02F	MODULE 01F	MODULE 01E

L19
L20
L21
YPCK7

0YPC7N	0YPC7P	1YPC7N	1YPC7P	2YPC7N	2YPC7P	3YPC7N	3YPC7P	
00YC7P 01	04YC7P 01	08YC7P 01	12YC7P 01	16YC7P 01	20YC7P 01	24YC7P 01	28YC7P 01	32YC7P 01
01YC7P 34	05YC7P 34	09YC7P 34	13YC7P 34	17YC7P 34	21YC7P 34	25YC7P 34	29YC7P 34	NOT USED
02YC7P 31	06YC7P 31	10YC7P 31	14YC7P 31	18YC7P 31	22YC7P 31	26YC7P 31	30YC7P 31	NOT USED
03YC7P 28	07YC7P 28	11YC7P 28	15YC7P 28	19YC7P 28	23YC7P 28	27YC7P 28	31YC7P 28	NOT USED
MODULE 26F	MODULE 25F	MODULE 18F	MODULE 17F	MODULE 10F	MODULE 09F	MODULE 02F	MODULE 01F	MODULE 01E

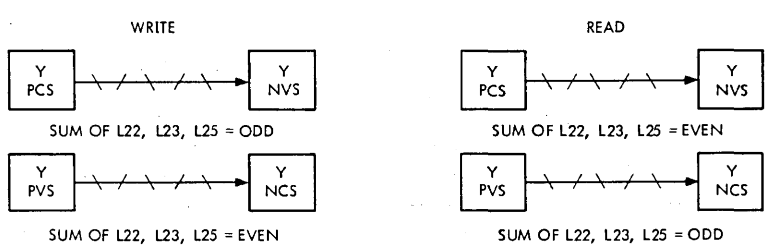

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Figure 3-13. Y-Positive Current Predrive-Drive Coupling System

	0YNC0N		0YNC0P		1YNC0N		1YNC0P		2YNC0N		2YNC0P		3YNC0N		3YNC0P			
NL19	00YC0N	10	04YC0N	10	08YC0N	10	12YC0N	10	16YC0N	10	20YC0N	10	24YC0N	10	28YC0N	10	32YC0N	10
NL20	01YC0N	11	05YC0N	11	09YC0N	11	13YC0N	11	17YC0N	11	21YC0N	11	25YC0N	11	29YC0N	11	NOT USED	
NL21	02YC0N	09	06YC0N	09	10YC0N	09	14YC0N	09	18YC0N	09	22YC0N	09	26YC0N	09	30YC0N	09	NOT USED	
YNCK0	03YC0N	08	07YC0N	08	11YC0N	08	15YC0N	08	19YC0N	08	23YC0N	08	27YC0N	08	31YC0N	08	NOT USED	
	MODULE 32F		MODULE 31F		MODULE 24F		MODULE 23F		MODULE 16F		MODULE 15F		MODULE 08F		MODULE 07F		MODULE 04E	

	0YNC1N		0YNC1P		1YNC1N		1YNC1P		2YNC1N		2YNC1P		3YNC1N		3YNC1P			
NL19	00YC1N	00	04YC1N	00	08YC1N	00	12YC1N	00	16YC1N	00	20YC1N	00	24YC1N	00	28YC1N	00	32YC1N	00
NL20	01YC1N	02	05YC1N	02	09YC1N	02	13YC1N	02	17YC1N	02	21YC1N	02	25YC1N	02	29YC1N	02	NOT USED	
L21	02YC1N	04	06YC1N	04	10YC1N	04	14YC1N	04	18YC1N	04	22YC1N	04	26YC1N	04	30YC1N	04	NOT USED	
YNCK1	03YC1N	06	07YC1N	06	11YC1N	06	15YC1N	06	19YC1N	06	23YC1N	06	27YC1N	06	31YC1N	06	NOT USED	
	MODULE 32F		MODULE 31F		MODULE 24F		MODULE 23F		MODULE 16F		MODULE 15F		MODULE 08F		MODULE 07F		MODULE 04E	

	0YNC2N		0YNC2P		1YNC2N		1YNC2P		2YNC2N		2YNC2P		3YNC2N		3YNC2P			
NL19	00YC2N	10	04YC2N	10	08YC2N	10	12YC2N	10	16YC2N	10	20YC2N	10	24YC2N	10	28YC2N	10	32YC2N	10
L20	01YC2N	11	05YC2N	11	09YC2N	11	13YC2N	11	17YC2N	11	21YC2N	11	25YC2N	11	29YC2N	11	NOT USED	
NL21	02YC2N	09	06YC2N	09	10YC2N	09	14YC2N	09	18YC2N	09	22YC2N	09	26YC2N	09	30YC2N	09	NOT USED	
YNCK2	03YC2N	08	07YC2N	08	11YC2N	08	15YC2N	08	19YC2N	08	23YC2N	08	27YC2N	08	31YC2N	08	NOT USED	
	MODULE 30F		MODULE 29F		MODULE 22F		MODULE 21F		MODULE 14F		MODULE 13F		MODULE 06F		MODULE 05F		MODULE 03E	

	0YNC3N		0YNC3P		1YNC3N		1YNC3P		2YNC3N		2YNC3P		3YNC3N		3YNC3P			
NL19	00YC3N	00	04YC3N	00	08YC3N	00	12YC3N	00	16YC3N	00	20YC3N	00	24YC3N	00	28YC3N	00	32YC3N	00
L20	01YC3N	02	05YC3N	02	09YC3N	02	13YC3N	02	17YC3N	02	21YC3N	02	25YC3N	02	29YC3N	02	NOT USED	
L21	02YC3N	04	06YC3N	04	10YC3N	04	14YC3N	04	18YC3N	04	22YC3N	04	26YC3N	04	30YC3N	04	NOT USED	
YNCK3	03YC3N	06	07YC3N	06	11YC3N	06	15YC3N	06	19YC3N	06	23YC3N	06	27YC3N	06	31YC3N	06	NOT USED	
	MODULE 30F		MODULE 29F		MODULE 22F		MODULE 21F		MODULE 14F		MODULE 13F		MODULE 06F		MODULE 05F		MODULE 03E	

	0YNC4N		0YNC4P		1YNC4N		1YNC4P		2YNC4N		2YNC4P		3YNC4N		3YNC4P			
L19	00YC4N	10	04YC4N	10	08YC4N	10	12YC4N	10	16YC4N	10	20YC4N	10	24YC4N	10	28YC4N	10	32YC4N	10
NL20	01YC4N	11	05YC4N	11	09YC4N	11	13YC4N	11	17YC4N	11	21YC4N	11	25YC4N	11	29YC4N	11	NOT USED	
NL21	02YC4N	09	06YC4N	09	10YC4N	09	14YC4N	09	18YC4N	09	22YC4N	09	26YC4N	09	30YC4N	09	NOT USED	
YNCK4	03YC4N	08	07YC4N	08	11YC4N	08	15YC4N	08	19YC4N	08	23YC4N	08	27YC4N	08	31YC4N	08	NOT USED	
	MODULE 28F		MODULE 27F		MODULE 20F		MODULE 19F		MODULE 12F		MODULE 11F		MODULE 04F		MODULE 03F		MODULE 02E	

	0YNC5N		0YNC5P		1YNC5N		1YNC5P		2YNC5N		2YNC5P		3YNC5N		3YNC5P			
L19	00YC5N	00	04YC5N	00	08YC5N	00	12YC5N	00	16YC5N	00	20YC5N	00	24YC5N	00	28YC5N	00	32YC5N	00
NL20	01YC5N	02	05YC5N	02	09YC5N	02	13YC5N	02	17YC5N	02	21YC5N	02	25YC5N	02	29YC5N	02	NOT USED	
L21	02YC5N	04	06YC5N	04	10YC5N	04	14YC5N	04	18YC5N	04	22YC5N	04	26YC5N	04	30YC5N	04	NOT USED	
YNCK5	03YC5N	06	07YC5N	06	11YC5N	06	15YC5N	06	19YC5N	06	23YC5N	06	27YC5N	06	31YC5N	06	NOT USED	
	MODULE 28F		MODULE 27F		MODULE 20F		MODULE 19F		MODULE 12F		MODULE 11F		MODULE 04F		MODULE 03F		MODULE 02E	

	0YNC6N		0YNC6P		1YNC6N		1YNC6P		2YNC6N		2YNC6P		3YNC6N		3YNC6P			
L19	00YC6N	10	04YC6N	10	08YC6N	10	12YC6N	10	16YC6N	10	20YC6N	10	24YC6N	10	28YC6N	10	32YC6N	10
L20	01YC6N	11	05YC6N	11	09YC6N	11	13YC6N	11	17YC6N	11	21YC6N	11	25YC6N	11	29YC6N	11	NOT USED	
NL21	02YC6N	09	06YC6N	09	10YC6N	09	14YC6N	09	18YC6N	09	22YC6N	09	26YC6N	09	30YC6N	09	NOT USED	
YNCK6	03YC6N	08	07YC6N	08	11YC6N	08	15YC6N	08	19YC6N	08	23YC6N	08	27YC6N	08	31YC6N	08	NOT USED	
	MODULE 26F		MODULE 25F		MODULE 18F		MODULE 17F		MODULE 10F		MODULE 09F		MODULE 02F		MODULE 01F		MODULE 01E	

	0YNC7N		0YNC7P		1YNC7N		1YNC7P		2YNC7N		2YNC7P		3YNC7N		3YNC7P			
L19	00YC7N	00	04YC7N	00	08YC7N	00	12YC7N	00	16YC7N	00	20YC7N	00	24YC7N	00	28YC7N	00	32YC7N	00
L20	01YC7N	02	05YC7N	02	09YC7N	02	13YC7N	02	17YC7N	02	21YC7N	02	25YC7N	02	29YC7N	02	NOT USED	
L21	02YC7N	04	06YC7N	04	10YC7N	04	14YC7N	04	18YC7N	04	22YC7N	04	26YC7N	04	30YC7N	04	NOT USED	
YNCK7	03YC7N	06	07YC7N	06	11YC7N	06	.5YC7N	06	19YC7N	06	23YC7N	06	27YC7N	06	31YC7N	06	NOT USED	
	MODULE 26F		MODULE 25F		MODULE 18F		MODULE 17F		MODULE 10F		MODULE 09F		MODULE 02F		MODULE 01F		MODULE 01E	

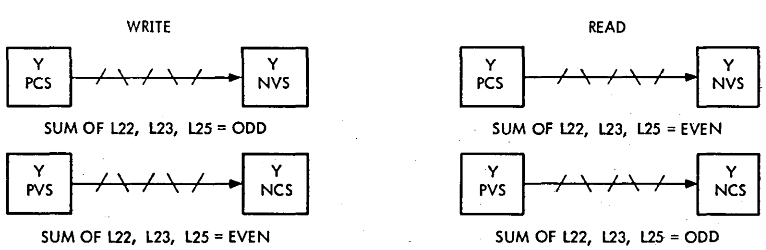

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Figure 3-14. Y-Negative Current Predrive-Drive Coupling System

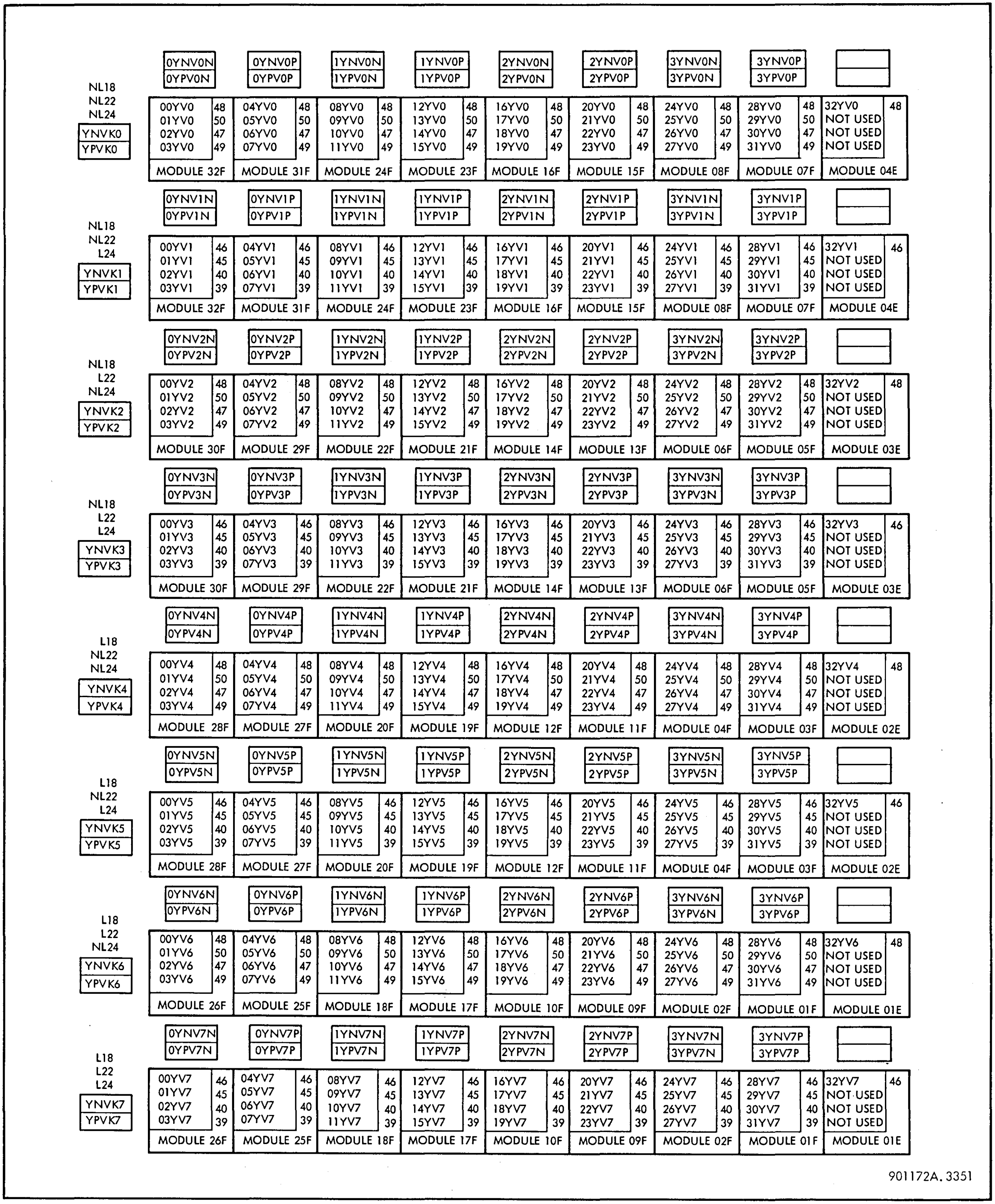

Figure 3-15. Y-Positive/Negative Voltage Predrive-Drive Coupling System

NOTE: Vd = +22V
Vm = +11V

Figure 3-16. Y-Current Predrive-Drive, Schematic Diagram

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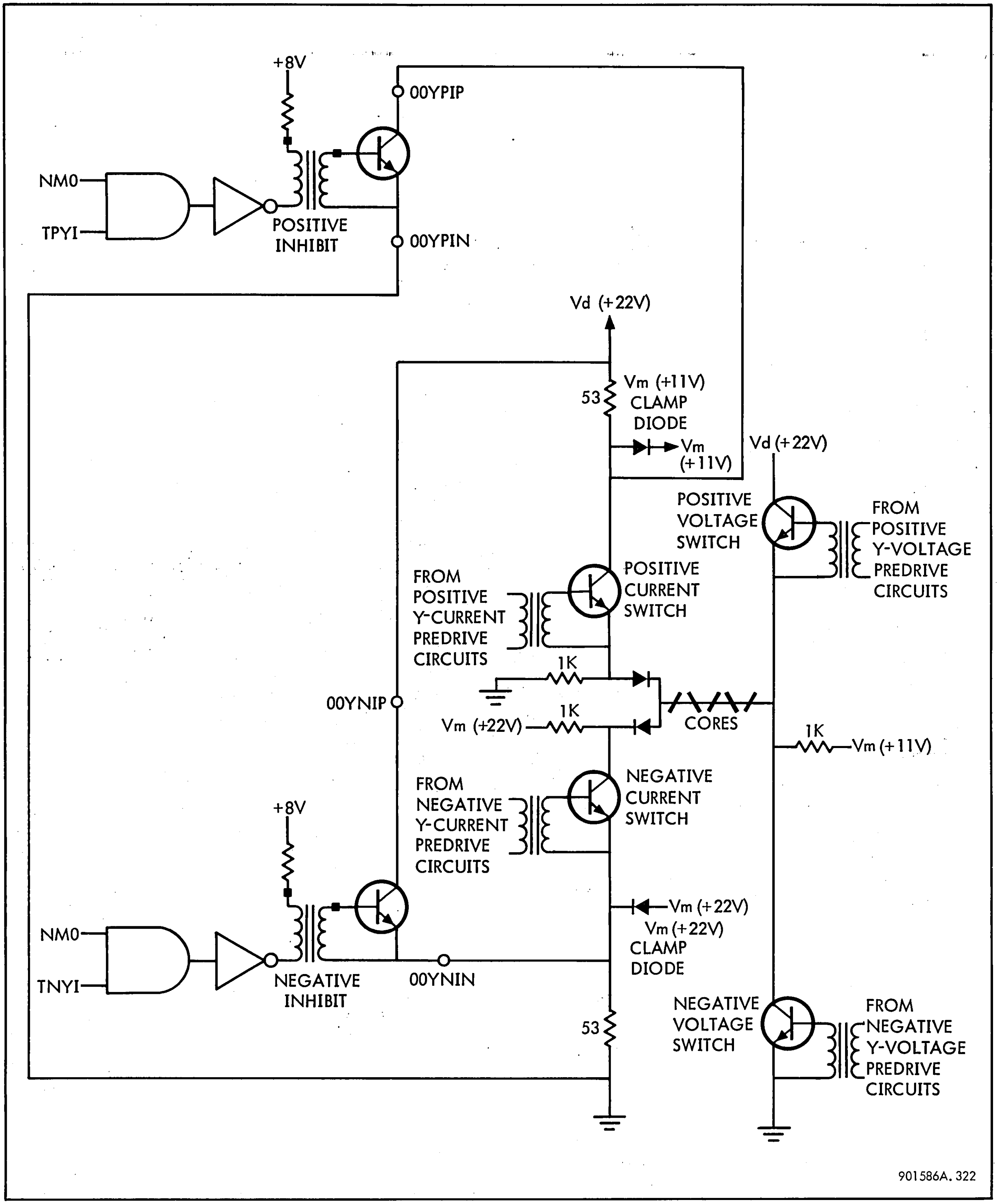

Figure 3-17. Y-Current Inhibit Circuits, Simplified Diagram

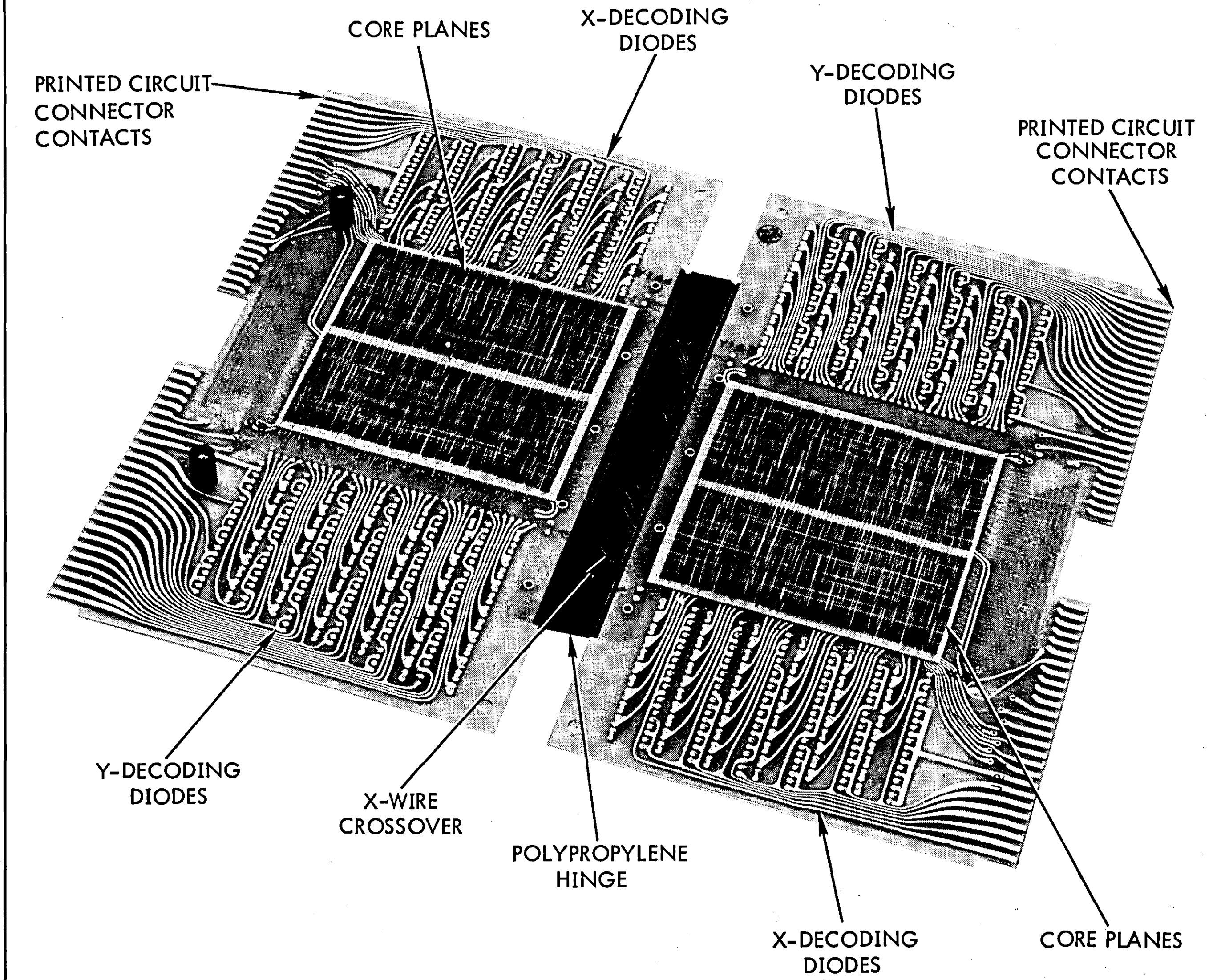

Figure 3-18. Core Diode Module, Nine-Bit (Open)

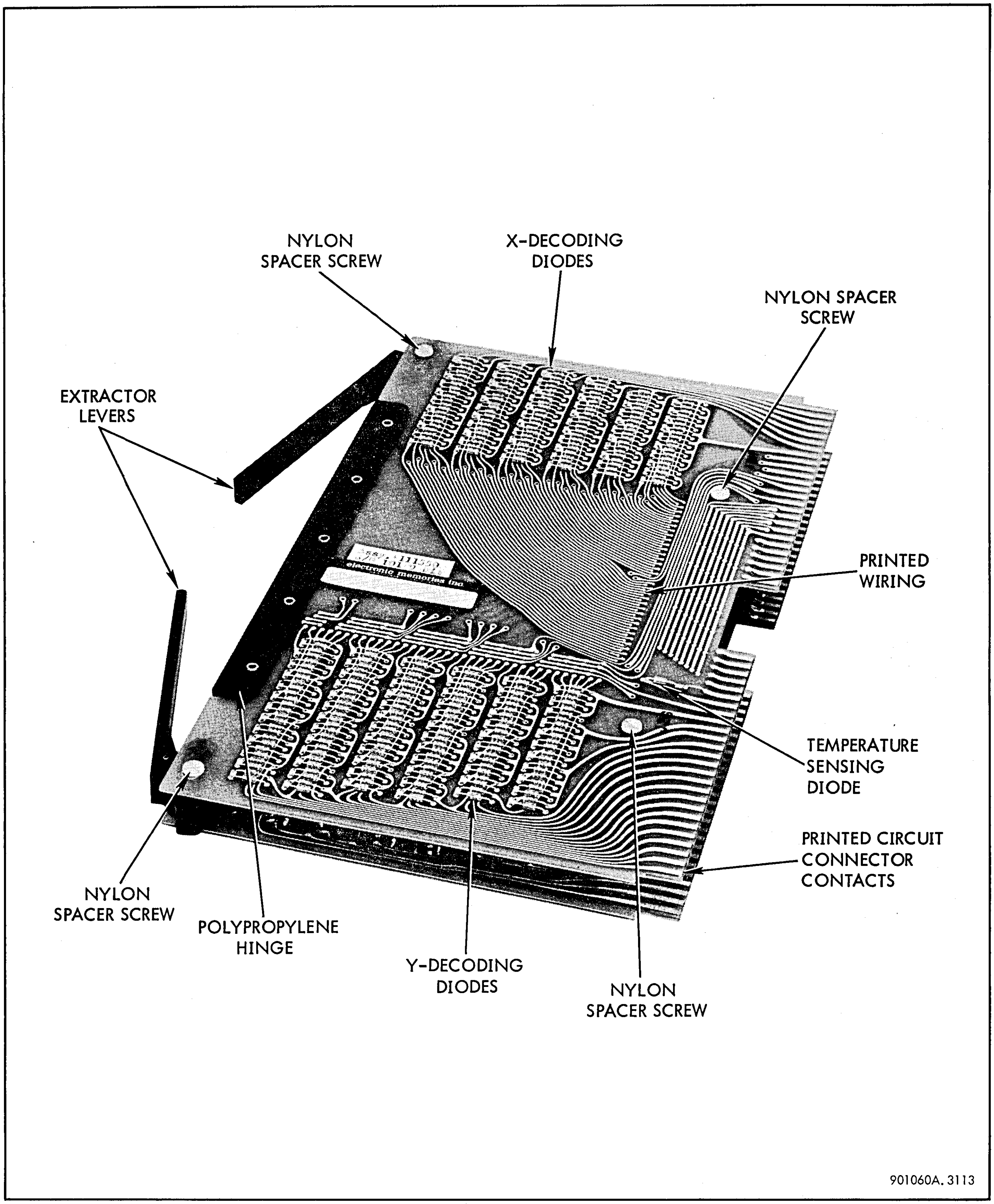

Figure 3-19. Core Diode Module As Inserted (Closed)

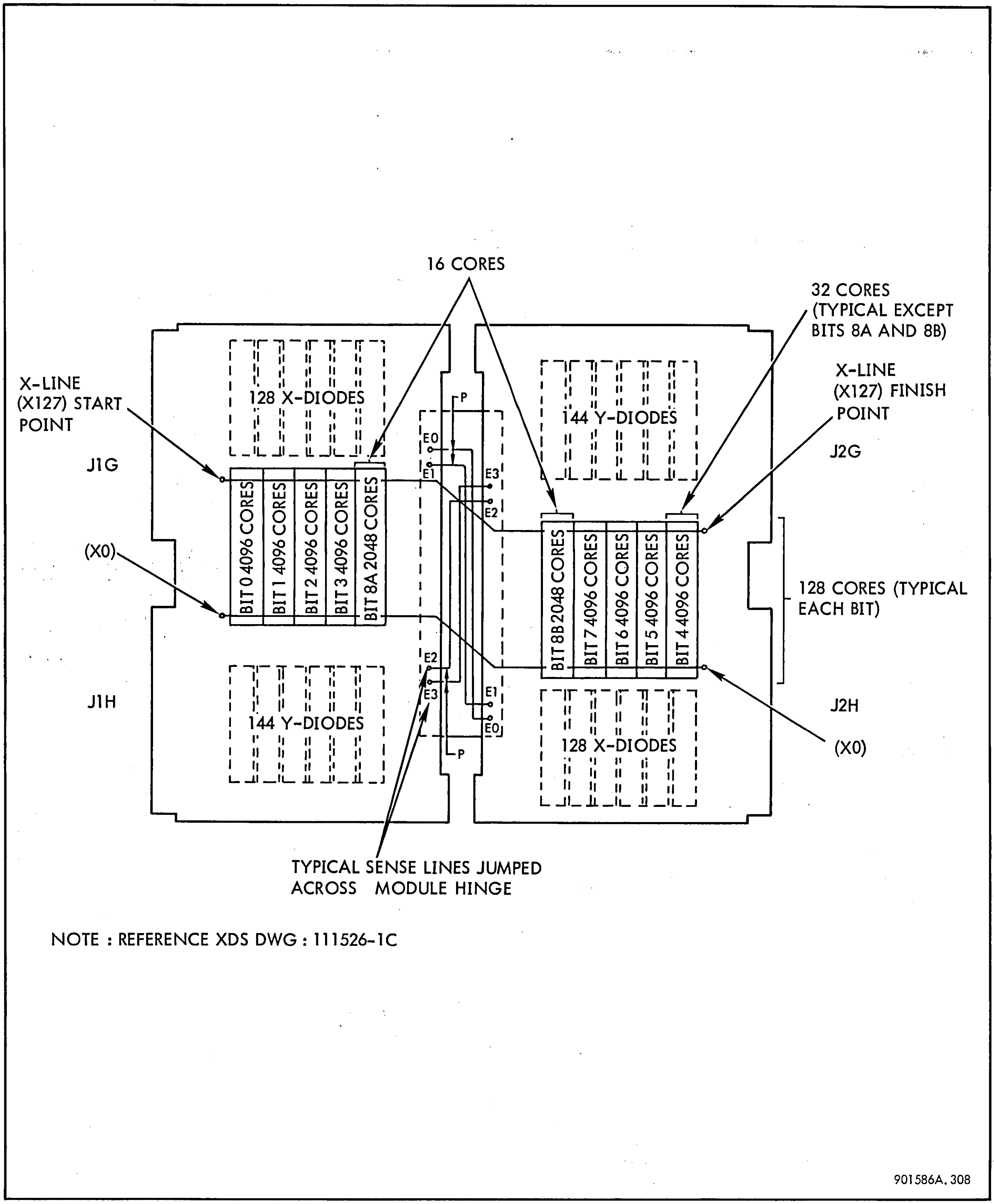

Figure 3-20. Core Diode Module, Bit Planes, X-Wire Crossover

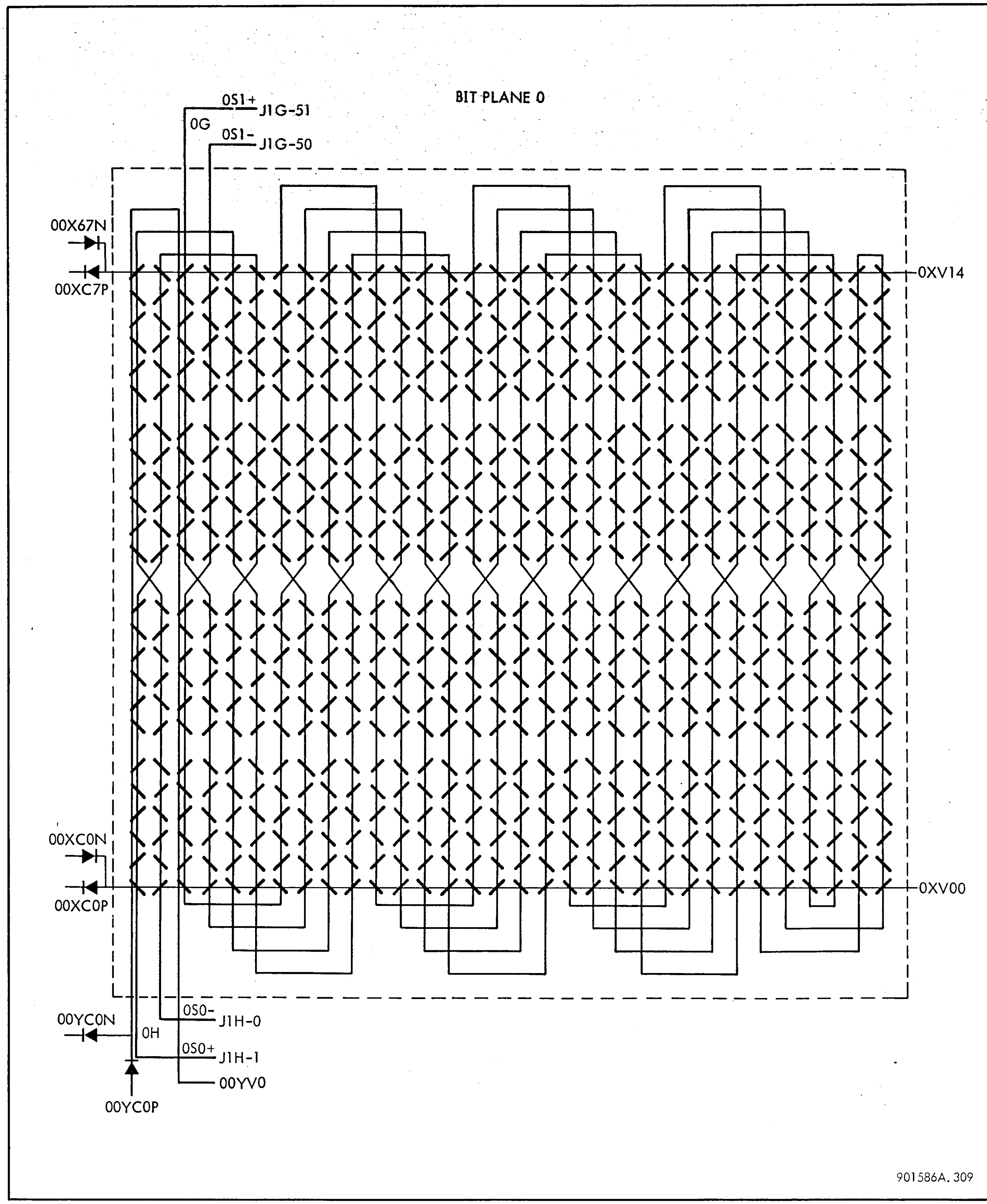

Figure 3-21. Bit 0 Sense Winding, Simplified Schematic Diagram

Sixteen X-wires with diodes share the same positive and negative current drivers. These 16 wires form one X-bus. There are eight X-buses on one module. Therefore, with respect to the bit planes, the X-buses and bit planes form an 8 by 8 (or an 8 by 9) matrix.

Each bit plane has 32 Y-drive lines. The Y-lines for each bit form pairs such that Y-line 0 is in series with Y-line 2, Y-line 1 is in series with Y-line 3, and so forth throughout the bit plane. Each Y-line can be described as being interlaced through the X-lines (see figure 3-21). The Y-lines linking two cores on the same X-line provide coincident-anticoincident operation. That is, while a core is selected through coincident current, there is a corresponding core on the mated Y-line which has anticoincident current. Only the core with coincident current is affected. The Y-lines are decoded by two diodes at one end, but, unlike the X-lines, only four double Y-lines share the same current driver during operation. The opposite end of the Y-line terminates in a complementary voltage driver. Each bit plane is independent with respect to the Y-lines, that is, there is no connection between Y-lines of one bit plane and Y-lines of another bit plane.

There are two sense lines that link the cores in a bit plane. As shown in figure 3-21, each sense line links half of the cores. Note that the sense lines cross each other in the center of the bit plane. This method reduces undesirable delta noise inherent in core memories.

3-20 CORE SWITCHING

During operation, approximately 350 mA of current flows through the selected X-wire to affect a specific core, and approximately an equal amount of current flows through the selected Y-wire. The amount of current through either the X- or the Y-wire is half the amount of current required to switch a core. When the currents through the X-wire and through the Y-wires at the core junction are additive, reduction causes the core to assume a state of polarity assigned a binary zero. If the currents at the core junction are subtractive, the two currents cancel, and the state of the core is unaffected. In considering the half-currents only, each core is subjected to one of four possible conditions:

a. X- and Y-half-currents are additive in a direction to cause the core to switch from a one to a zero.

b. X- and Y-half-currents are additive in a direction to cause the core to switch from a zero to a one.

c. X- and Y-half-currents are subtractive, and each half-current cancels the effects of the other. The core is not affected.

d. Half-current flows through either the X- or the Y-wire or no current flows through either wire. The core is not affected.

To switch a core, the two half-currents must enter the core from the same side; otherwise, they cancel each other. Figure 3-22 illustrates core switching. Assumed current flow is from positive to negative.

3-21 TEMPERATURE SENSING

Two diodes on every core-diode module are used in a temperature sensing network. The network controls the output of the memory power supply drive current to compensate for temperature variations. Because less current is required to switch a core at higher temperatures, the temperature sensing network raises or lowers the drive current inversely as temperature varies.

3-22 SENSE SYSTEM

Figure 3-23 shows a portion of the sense system in the core memory. Since there are two sense loops for every bit plane, there are 66 sense loops for every stack of core-diode modules. Figure 3-23 shows the relationship between the sense loops, the sense preamplifiers (PA), the sense amplifiers (SA), and discriminators (D). The sense system is identical for each bit of a word. All of the sense preamplifiers for a given bit on all of the stacks feed the same sense amplifier. Note that each preamplifier is selected by address bits so that only one preamplifier is enabled for any memory access. The sense preamplifier is enabled by signal PASL(X) when it is false. No output can occur from the sense preamplifier until the output of PASL(X) is at -8V. By selecting the proper preamplifier with PASL(X), all of the delta noise caused by a current buildup in the drive lines is not passed on to the preamplifier. The sense amplifier with strobe signal SAST(X) operates in a similar manner. The discriminators isolate the M-register from the sense amplifier output.

The waveshapes shown in figure 3-23 should be used only for reference. These waveshapes may not necessarily be duplicated in a given system because of different cable lengths, scope characteristics, and other factors.

3-23 HT26 SENSE PREAMPLIFIER MODULE

Figure 3-24 is a schematic diagram of the sense preamplifiers fed by the bit 0 sense loops of stack 0. The sense preamplifier is a differential pair transistor, Q1, with input through the common mode transformer, T . This transformer, known as a "Balon" transformer, rejects common mode noise. Emitter current for Q1 is derived from current source, Q2, and from the 1 kilohm precision resistor.Voltage Ve controls the gain of the preamplifier by changing the emitter current, and thus, the emitter resistance of Q1. Voltage Ve is supplied by the ST17 module and is temperature controlled to provide gain compensation for the preamplifier. Transistors Q1 and Q2 are mounted in the same housing and have matched Vbe characteristics. Preamplifier selection signal, PASLO, when at -8V, allows emitter current in Q2, which turns on Q1. This produces differential outputs SPA00P and SPA00N which are applied to the sense amplifier as described in paragraph 3-24 which follows.

3-24 HT11 SENSE AMPLIFIER AND DISCRIMINATOR MODULE

Figure 3-25 is a simplified schematic diagram of the sense amplifier and discriminator. Transistors Q3, Q4, and Q5 form the sense amplifier and transistors Q6, Q7, and Q8 make up the discriminator.

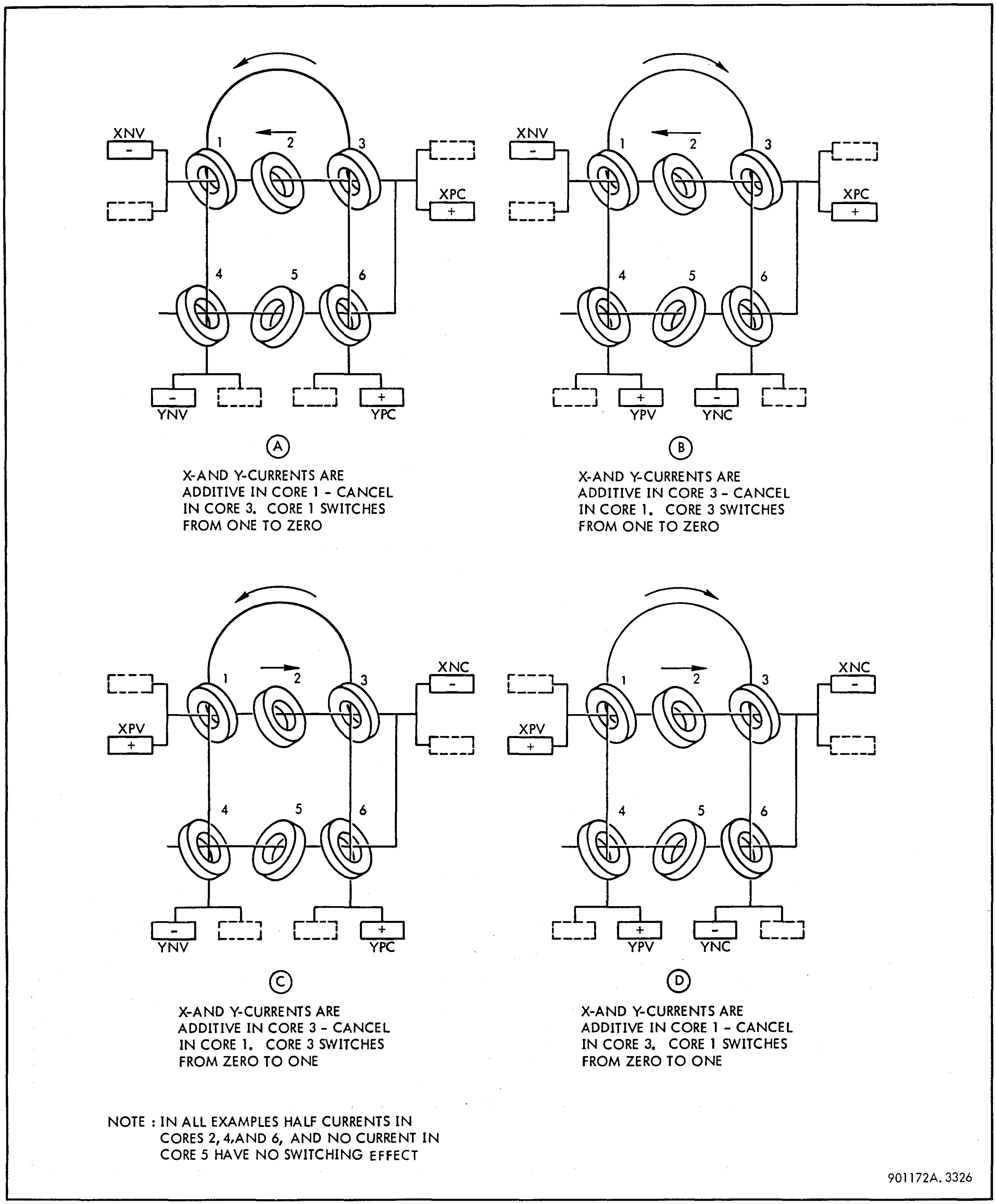

Figure 3-22. Basic Core Switching

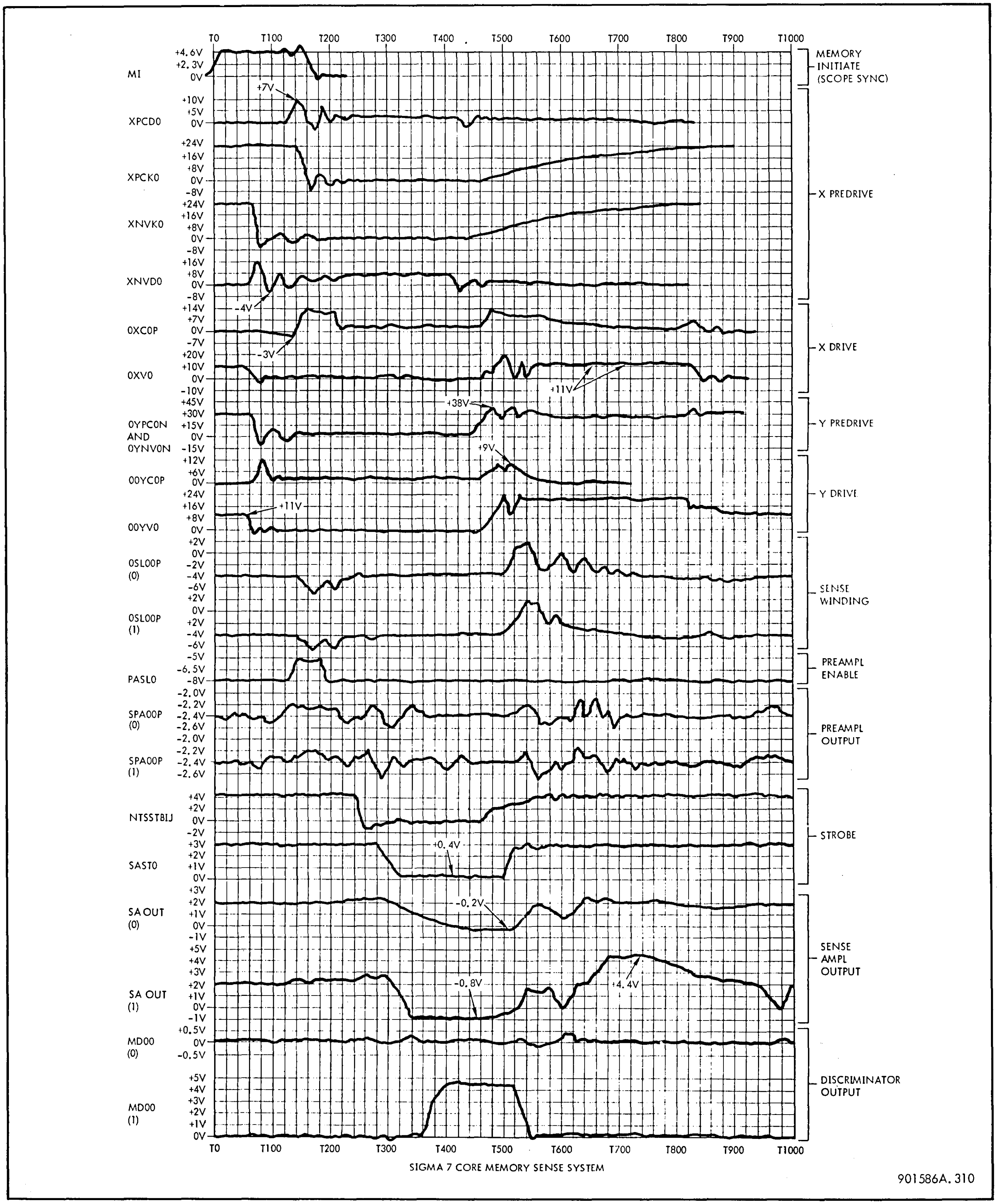

Figure 3-23. Sigma 5 and 7 Core Memory Sense System, Simplified Schematic and Timing Diagram

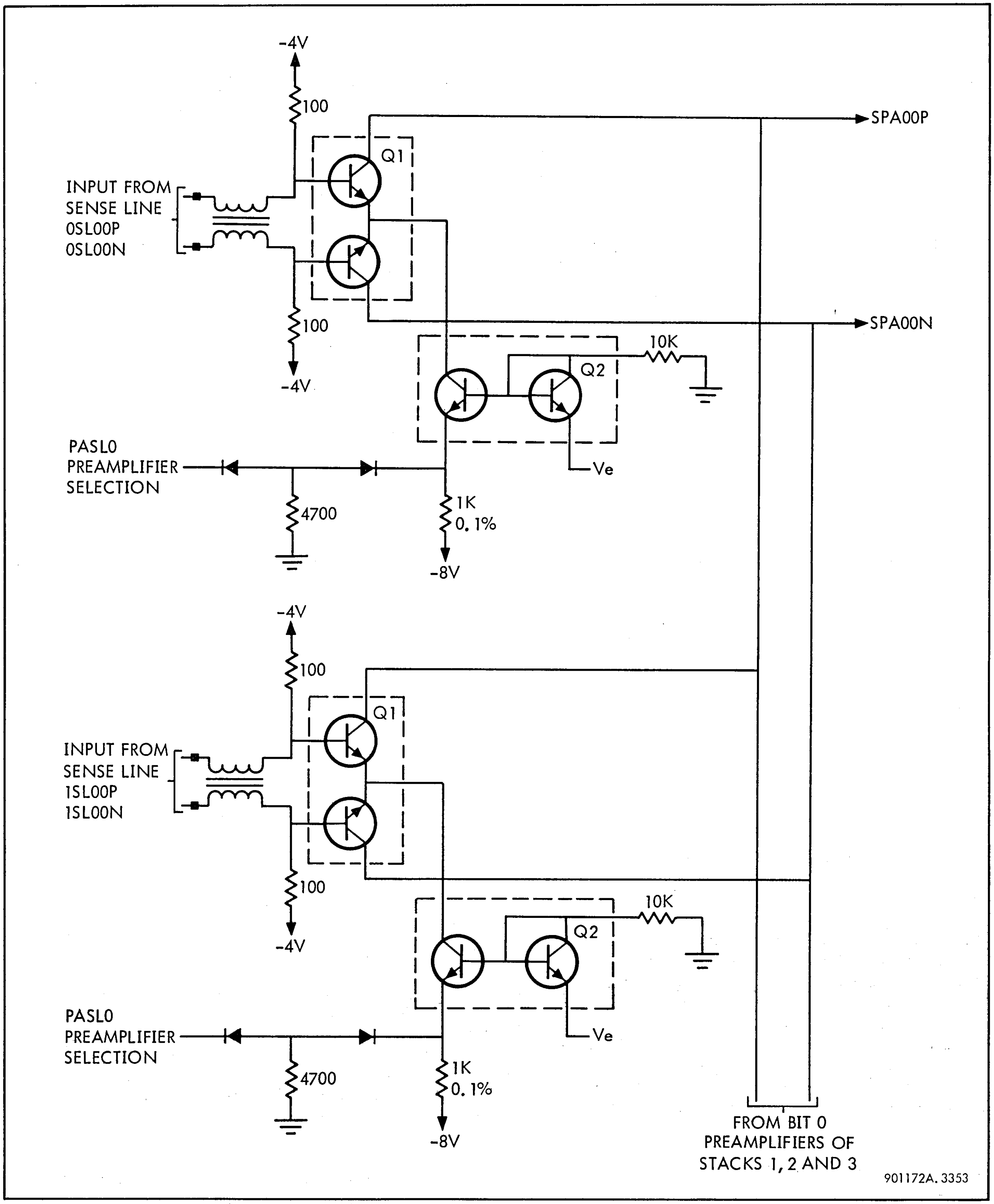

Figure 3-24. HT26 Sense Preamplifier, Bit 0, Stack 0, Simplified Schematic Diagram

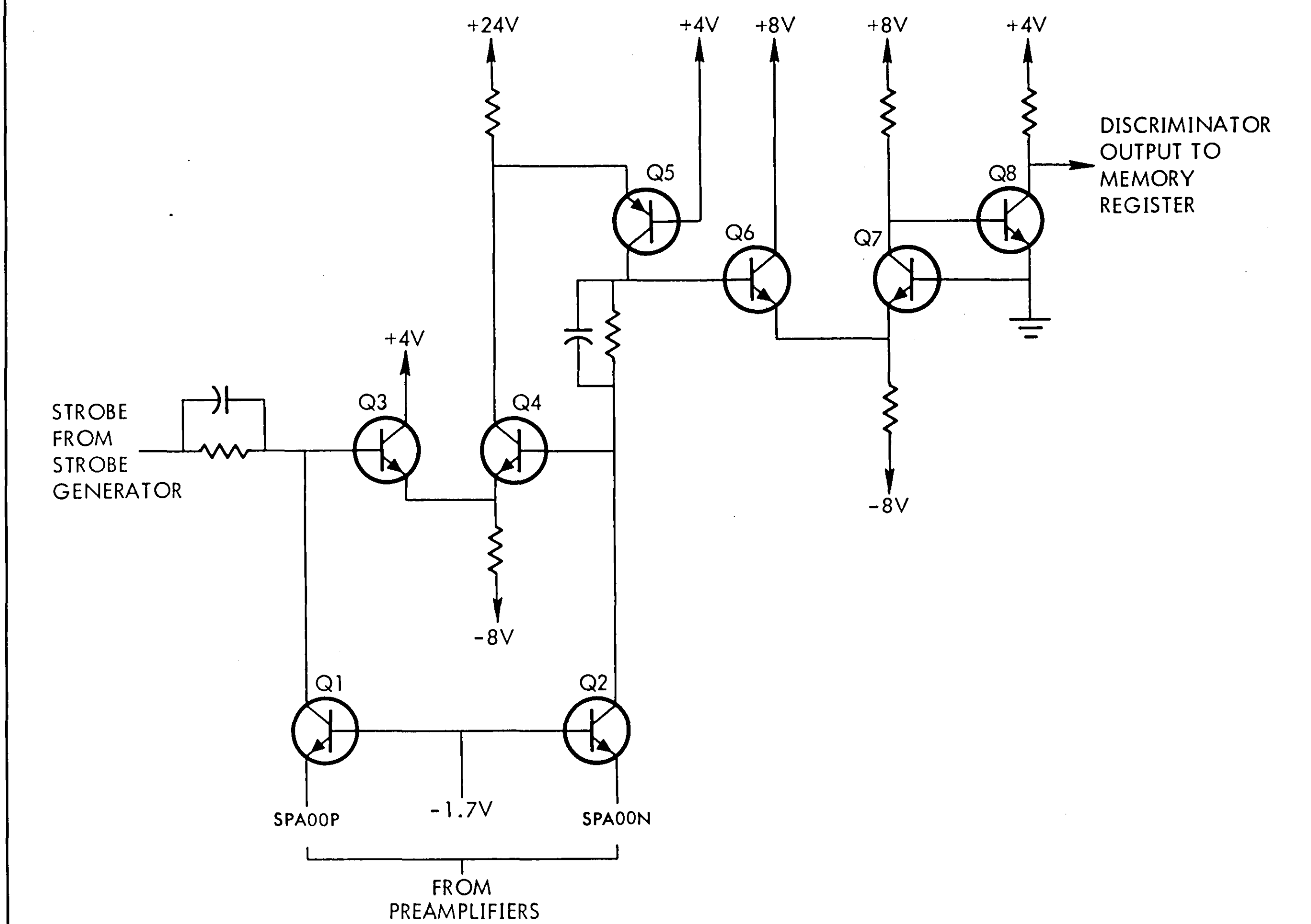

Figure 3-25. Sense Amplifier/Discriminator, Simplified Schematic Diagram

Transistors Q1 and Q2 are buffer amplifiers with bases biased at -1.7V that provide a low impedance input for the preamplifier outputs. Feedback occurs through the resistance-capacitance network between Q5 and Q4.

With no differential input, the circuit acts as a unity gain amplifier for the strobe signal. The strobe signal (SAST0-SAST3) varies approximately between +3V (Vs) and +0.7V (Vt). In operation, the core output (about 26 mV) causes the output of the sense amplifier to swing down through 0V to about -0.5V. The discriminator responds to such a signal because it discriminates about ground. With neither a strobe signal nor a core output, the sense amplifier does not fall to ground and no discriminator output is produced.

3-25 SENSE SYSTEM CHARTS

Figure 3-26 provides a summary of signals with module and pin locations for each data bit in a 16K Sigma 5 and 7 sense system. These charts are especially useful in locating sense system signals during troubleshooting.

3-26 TIMING AND CONTROL

Basic timing in each memory bank is controlled by two 600-ns delay lines. One of the delay lines controls the read half of a memory cycle, the other delay line controls the write half of a cycle. Figure 3-27 shows a simplified diagram of the read and write delay lines and initiating logic. Each delay line has taps at every 20-ns interval. Buffer and inverter delay sensors pick off the delay line pulse at strategic times. The outputs of the buffers and inverters are distributed to the memory control logic to provide the basic memory timing.

All memory cycles start when signal S/READDL goes true and initiates the read delay line. At TR060 time, signal NTR060 goes false and disables signal S/READDL.

DATA BIT	SIZE	C/D MODULE	SENSE LINE NAME	SENSE LINE PIN	PREAMPLIFIER NAME	PREAMPLIFIER INPUT	PREAMPLIFIER OUTPUT	SENSE AMPLIFIER INPUT	SENSE AMPLIFIER OUTPUT	DISCRIM. OUTPUT
0	4K	31H	0SL00P	01	SPA00P	32J09	32J37	26J45	26J43	26J40
			0SL00N	00	SPA00N	32J08	32J36	(SPA00P)		(MD00)
		31G	1SL00P	51	SPA00P	32J11	32J37	25J44		
			1SL00N	50	SPA00N	32J10	32J36	(SPA00N)		
	8K	27H	2SL00P	01	SPA00P	30J09	30J37			
			2SL00N	00	SPA00N	30J08	30J36	STROBE		
		27G	3SL00P	51	SPA00P	30J11	30J37	INPUT		
			3SL00N	50	SPA00N	30J10	30J36	25J29		
	12K	29H	4SL00P	01	SPA00P	31J09	31J37	(SASTO)		
			4SL00N	00	SPA00N	31J08	31J36			
		29G	5SL00P	51	SPA00P	31J11	31J37			
			5SL00N	50	SPA00N	31J10	31J36			
	16K	25H	6SL00P	01	SPA00P	29J09	29J37			
			6SL00N	00	SPA00N	29J08	29J36			
		25G	7SL00P	51	SPA00P	29J11	29J37			
			7SL00N	50	SPA00N	29J10	29J36			
1	4K	31H	0SL01P	03	SPA01P	32J25	32J35	26J47	26J39	26J38
			0SL01N	02	SPA01N	32J24	32J34	(SPA01P)		(MD01)
		31G	1SL01P	49	SPA01P	32J23	32J35	26J46		
			1SL01N	48	SPA01N	32J22	32J34	(SPA01N)		
	8K	27H	2SL01P	03	SPA01P	30J25	30J35			
			2SL01N	02	SPA01N	30J24	30J34	STROBE		
		27G	3SL01P	49	SPA01P	30J23	30J35	INPUT		
			3SL01N	48	SPA01N	30J22	30J34	26J29		
	12K	29H	4SL01P	03	SPA01P	31J25	31J35	(SASTO)		
			4SL01N	02	SPA01N	31J24	31J34			
		29G	5SL01P	49	SPA01P	31J23	31J35			
			5SL01N	48	SPA01N	31J22	31J34			
	16K	25H	6SL01P	03	SPA01P	29J25	29J35			
			6SL01N	02	SPA01N	29J24	29J34			
		25G	7SL01P	49	SPA01P	29J23	29J35			
			7SL01N	48	SPA01N	29J22	29J34			
2	4K	31H	0SL02P	05	SPA02P	32J03	32J41	26J27	26J33	26J34
			0SL02N	04	SPA02N	32J02	32J40	(SPA02P)		(MD02)
		31G	1SL02P	47	SPA02P	32J05	32J41	26J28		
			1SL02N	46	SPA02N	32J04	32J40	(SPA02N)		
	8K	27H	2SL02P	05	SPA02P	32J03	30J41			
			2SL02N	04	SPA02N	30J02	30J40	STROBE		
		27G	3SL02P	47	SPA02P	30J05	30J41	INPUT		
			3SL02N	46	SPA02N	30J04	30J40	26J29		
	12K	29H	4SL02P	05	SPA02P	31J03	31J41	(SASTO)		
			4SL02N	04	SPA02N	31J02	31J40			
		29G	5SL02P	47	SPA02P	31J05	31J41			
			5SL02N	46	SPA02N	31J04	31J40			
	16K	25H	6SL02P	05	SPA02P	29J03	29J41			
			6SL02N	04	SPA02N	29J02	29J40			
		25G	7SL02P	47	SPA02P	29J05	29J41			
			7SL02N	46	SPA02N	29J04	29J40			
3	4K	31H	0SL03P	07	SPA03P	32J19	32J39	26J22	26J14	26J12
			0SL03N	06	SPA03N	32J18	32J38	(SPA03P)		(MD03)
		31G	1SL03P	45	SPA03P	32J27	32J39	26J21		
			1SL03N	44	SPA03N	32J26	32J38	(SPA03N)		
	8K	27H	2SL03P	07	SPA03P	30J19	30J39			
			2SL03N	06	SPA03N	30J18	30J38			
		27G	3SL03P	45	SPA03P	30J27	30J39	STROBE		
			3SL03N	44	SPA03N	30J26	30J38	INPUT		
	12K	29H	4SL03P	07	SPA03P	31J19	31J39	26J20		
			4SL03N	06	SPA03N	31J18	31J38	(SASTO)		
		29G	5SL03P	45	SPA03P	31J27	31J39			
			5SL03N	44	SPA03N	31J26	31J38			
	16K	25H	6SL03P	07	SPA03P	29J19	29J39			
			6SL03N	06	SPA03N	29J18	29J38			
		25G	7SL03P	45	SPA03P	29J27	29J39			
			7SL03N	44	SPA03N	29J26	29J38			

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Figure 3-26. Core Memory Sense System Charts (Sheet 1 of 9)

DATA BIT	SIZE	C/D MODULE	SENSE LINE NAME	SENSE LINE PIN	PREAMPLIFIER NAME	PREAMPLIFIER INPUT	PREAMPLIFIER OUTPUT	SENSE AMPLIFIER INPUT	SENSE AMPLIFIER OUTPUT	DISCRIM. OUTPUT
4	4K		0SL04P	51	SPA04P	32J21	32J43	26J23	26J06	26J08
		32G	0SL04N	50	SPA04N	32J20	32J42	(SPA04P)		(MD04)
			1SL04P	01	SPA04P	32J13	32J43	25J24		
		32H	1SL04N	00	SPA04N	32J12	32J42	(SPA04N)		
	8K		2SL04P	51	SPA04P	30J21	30J43			
		28G	2SL04N	50	SPA04N	30J20	30J42	STROBE		
			3SL04P	01	SPA04P	30J13	30J43	INPUT		
		28H	3SL04N	00	SPA04N	30J12	20J42	26J20		
	12K		4SL04P	51	SPA04P	31J21	31J43	(SASTO)		
		30G	4SL04N	50	SPA04N	31J20	31J42			
			5SL04P	01	SPA04P	31J13	31J43			
		30H	5SL04N	00	SPA04N	31J12	31J42			
	16K		6SL04P	51	SPA04P	29J21	29J43			
		26G	6SL04N	50	SPA04N	29J20	29J42			
			7SL04P	01	SPA04P	29J13	29J43			
		26H	7SL04N	00	SPA04N	29J12	29J42			
5	4K		0SL05P	49	SPA05P	32J07	32J45	26J25	26J01	26J04
		32G	0SL05N	48	SPA05N	32J06	32J44	(SPA05P)		(MD05)
			1SL05P	03	SPA05P	32J15	32J45	26J26		
		32H	1SL05N	02	SPA05N	32J14	32J44	(SPA05N)		
	8K		2SL05P	49	SPA05P	30J07	30J45			
		28G	2SL05N	48	SPA05N	30J06	30J44	STROBE		
			3SL05P	03	SPA05P	30J15	30J45	INPUT		
		28H	3SL05N	02	SPA05N	30J14	30J44	26J20		
	12K		4SL05P	49	SPA05P	31J07	31J45	(SASTO)		
		30G	4SL05N	48	SPA05N	31J06	31J44			
			5SL05P	03	SPA05P	31J15	31J45			
		30H	5SL05N	02	SPA05N	31J14	31J44			
	16K		6SL05P	49	SPA05P	29J07	29J45			
		26G	6SL05N	48	SPA05N	29J06	29J44			
			7SL05P	03	SPA05P	29J15	29J45			
		26H	7SL05N	02	SPA05N	29J14	29J44			
6	4K		0SL06P	47	SPA06P	28J09	28J37	25J45	25J43	25J40
		32G	0SL05N	46	SPA06N	28J08	28J36	(SPA06P)		(MD06)
			1SL06P	05	SPA06P	28J11	28J37	25J44		
		32H	1SL06N	04	SPA06N	28J10	28J36	(SPA06N)		
	8K		2SL06P	47	SPA06P	22J09	22J37			
		28G	2SL06N	46	SPA06N	22J08	22J36	STROBE		
			3SL06P	05	SPA06P	22J11	22J37	INPUT		
		28H	3SL06N	04	SPA06N	22J10	22J36	25J29		
	12K		4SL06P	47	SPA06P	27J09	27J37	(SASTO)		
		30G	4SL06N	46	SPA06N	27J08	27J36			
			5SL06P	05	SPA06P	27J11	27J37			
		30H	5SL06N	04	SPA06N	27J10	27J36			
	16K		6SL06P	47	SPA06P	21J09	21J37			
		26G	6SL06N	46	SPA06N	21J08	21J36			
			7SL06P	05	SPA06P	21J11	21J37			
		26H	8SL06N	04	SPA06N	21J10	21J36			
7	4K		0SL07P	45	SPA07P	28J25	28J35	25J47	25J39	25J38
		32G	0SL07N	44	SPA07N	28J24	28J34	(SPA07P)		(MD07)
			1SL07P	07	SPA07P	28J23	28J35	25J46		
		32H	1SL07N	06	SPA07N	28J22	28J34	(SPA07N)		
	8K		2SL07P	45	SPA07P	22J25	22J35			
		28G	2SL07N	44	SPA07N	22J24	22J34	STROBE		
			3SL07P	07	SPA07P	22J23	22J35	INPUT		
		28H	3SL07N	06	SPA07N	22J22	22J34	25J29		
	12K		4SL07P	45	SPA07P	27J25	27J35	(SASTO)		
		30G	4SL07N	44	SPA07N	27J24	27J34			
			5SL07P	07	SPA07P	27J23	27J35			
		30H	5SL07N	06	SPA07N	27J22	27J34			
	16K		6SL07P	45	SPA07P	21J25	21J35			
		26G	6SL07N	44	SPA07N	21J24	21J34			
			7SL07P	07	SPA07P	21J23	21J35			
		26H	7SL07N	06	SPA07N	21J22	21J34			

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Figure 3-26. Core Memory Sense System Charts (Sheet 2 of 9)

DATA BIT	SIZE	C/D MODULE	SENSE LINE		PREAMPLIFIER			SENSE AMPLIFIER		DISCRIM.
			NAME	PIN	NAME	INPUT	OUTPUT	INPUT	OUTPUT	OUTPUT
	4K		0SL08P	01	SPA08P	28J03	28J41	25J22	25J14	25J12
		23H	0SL08N	00	SPA08N	28J02	28J40	(SPA08P)		(MD08)
			1SL08P	51	SPA08P	28J05	28J41	25J21		
		23G	1SL08N	50	SPA08N	28J04	28J40	(SPA08N)		
	8K		2SL08P	01	SPA08P	22J03	22J41			
		19H	2SL08N	00	SPA08N	22J02	22J41	STROBE		
			3SL08P	51	SPA08P	22J05	22J41	INPUT		
8		19G	3SL08N	50	SPA08N	22J04	22J40	25J20		
	12K		4SL08P	01	SPA08P	27J03	27J41	(SAST1)		
		21H	4SL08N	00	SPA08N	27J02	27J40			
			5SL08P	51	SPA08P	27J05	27J41			
		21G	5SL08N	50	SPA08N	27J04	27J40			
	16K		5SL08P	01	SPA08P	21J03	21J41			
		17H	6SL08N	00	SPA08N	21J02	21J40			
			7SL08P	51	SPA08P	21J05	21J41			
		17G	7SL08N	50	SPA08N	21J04	21J40			
	4K		0SL09P	03	SPA09P	28J19	28J39	25J23	25J06	25J08
		23H	0SL09N	02	SPA09N	28J18	28J38	(SPA09P)		(MD09)
			1SL09P	49	SPA09P	28J27	28J39	25J24		
		23G	1SL09N	48	SPA09N	28J26	28J38	(SPA09N)		
	8K		2SL09P	03	SPA09P	22J19	22J39			
		19H	2SL09N	20	SPA09N	22J18	22J38	STROBE		
			3SL09P	49	SPA09P	22J27	22J39	INPUT		
9		19G	3SL09N	48	SPA09N	22J26	22J38	25J20		
	12K		4SL09P	03	SPA09P	27J19	27J39	(SAST1)		
		21H	4SL09N	02	SPA09N	27J18	27J38			
			5SL09P	49	SPA09P	27J27	27J39			
		21G	5SL09N	48	SPA09N	27J26	27J38			
	16K		6SL09P	03	SPA09P	21J19	21J39			
		17H	6SL09N	02	SPA09N	21J18	21J38			
			7SL09P	49	SPA09P	21J27	21J39			
		17G	7SL09N	48	SPA09N	21J26	21J38			
	4K		0SL10P	05	SPA10P	28J21	28J43	25J25	25J01	25J04
		23H	0SL10N	04	SPA10N	28J20	28J42	(SPA10P)		(MD10)
			1SL10P	47	SPA10P	28J13	28J43	25J26		
		23G	1SL10N	46	SPA10N	28J12	28J42	(SPA10N)		
	8K		2SL10P	05	SPA10P	22J21	22J43			
		19H	2SL10N	04	SPA10N	22J20	22J42	STROBE		
			3SL10P	47	SPA10P	22J13	22J43	INPUT		
		19G	3SL10N	46	SPA10N	22J12	22J42	25J20		
10	12K		4SL10P	05	SPA10P	27J21	27J43	(SAST1)		
		21H	4SL10N	04	SPA10N	27J20	27J42			
			5SL10P	47	SPA10P	27J13	27J43			
		21G	5SL10N	46	SPA10N	27J12	27J42			
	16K		6SL10P	05	SPA10P	21J21	21J43			
		17H	6SL10N	04	SPA10N	21J20	21J42			
			7SL10P	47	SPA10P	21J13	21J43			
		17G	7SL10N	46	SPA10N	21J12	21J42			
	4K		0SL11P	07	SPA11P	28J07	28J45	25J27	25J33	25J34
		23H	0SL11N	06	SPA11N	28J06	28J44	(SPA11P)		(MD11)
			1SL11P	45	SPA11P	28J15	28J45	25J28		
		23G	1SL11N	44	SPA11N	28J14	28J44	(SPA11N)		
	8K		2SL11P	07	SPA11P	22J07	22J45			
		19H	2SL11N	06	SPA11N	22J06	22J44			
			3SL11P	45	SPA11P	22J15	22J45	STROBE		
11		19G	3SL11N	44	SPA11N	22J14	22J44	INPUT		
	12K		4SL11P	07	SPA11P	27J07	27J45	25J28		
		21H	4SL11N	05	SPA11N	28J06	27J44	(SAST0)		
			5SL11P	45	SPA11P	27J15	27J45			
		21G	5SL11N	44	SPA11N	27J14	27J44			
	16K		5SL11P	07	SPA11P	21J07	21J45			
		17H	6SL11N	06	SPA11N	21J06	21J44			
			7SL11P	45	SPA11P	21J15	21J45			
		17G	8LS11N	44	SPA11N	21J14	21J44			

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Figure 3-26. Core Memory Sense System Charts (Sheet 3 of 9)

DATA BIT	SIZE	C/D MODULE	SENSE LINE NAME	SENSE LINE PIN	PREAMPLIFIER NAME	PREAMPLIFIER INPUT	PREAMPLIFIER OUTPUT	SENSE AMPLIFIER INPUT	SENSE AMPLIFIER OUTPUT	DISCRIM. OUTPUT
12	4K	24G	0SL12P	51	SPA12P	20J09	20J37	23J47	23J39	23J38
			0SL12N	50	SPA12N	20J08	20J36	(SPA12P)		(MD12)
		24H	1SL12P	01	SPA12P	20J11	20J37	23J46		
			1SL12N	00	SPA12N	20J10	20J36	(SPA12N)		
	8K	20G	2SL12P	41	SPA12P	18J09	18J37			
			2SL12N	50	SPA12N	18J08	18J36	STROBE		
		20H	3SL12P	01	SPA12P	18J11	18J37	INPUT		
			3SL12N	00	SPA12N	18J10	18J36	23J29		
	12K	22G	4SL12P	51	SPA12P	19J09	19J37	(SAST1)		
			4SL12N	50	SPA12N	19J08	19J36			
		22H	5SL12P	01	SPA12P	19J11	19J37			
			5SL12N	00	SPA12N	19J10	19J36			
	16K	18G	6SL12P	51	SPA12P	17J09	19J37			
			6SL12N	50	SPA12N	17J08	17J36			
		18H	7SL12P	01	SPA12P	17J11	17J37			
			7SL12N	00	SPA12N	17J10	17J36			
13	4K	24G	0SL13P	49	SPA13P	20J25	20J35	23J27	23J33	23J34
			0SL13N	48	SPA13N	20J24	20J34	(SPA13P)		(MD13)
		24H	1SL13P	03	SPA13P	20J23	20J35	23J28		
			1SL13N	02	SPA13N	20J22	20J34	(SPA13N)		
	8K	20G	2SL13P	49	SPA13P	18J25	18J35	STROBE		
			2SL13N	48	SPA13N	18J24	18J34	INPUT		
		20H	3SL13P	03	SPA13P	18J23	18J35	23J29		
			3SL13N	02	SPA13N	18J22	18J34	(SAST1)		
	12K	22G	4SL13P	49	SPA13P	19J25	19J35			
			4SL13N	48	SPA13N	19J24	19J34			
		22H	5SL13P	03	SPA13P	19J23	19J35			
			5SL13N	02	SPA13N	19J22	19J34			
	16K	18G	6SL13P	49	SPA13P	17J25	17J35			
			6SL13N	48	SPA13N	17J24	17J34			
		18H	7SL13P	03	SPA13P	17J23	17J35			
			7SL13N	02	SPA13N	17J22	17J34			
14	4K	24G	0SL14P	47	SPA14P	20J03	20J41	23J22	23J14	23J12
			0SL14N	46	SPA14N	20J02	20J40	(SPA14P)		(MD14)
		24H	1SL14P	05	SPA14P	20J05	20J41	23J21		
			1SL14N	04	SPA14N	20J04	20J40	(SPA14N)		
	8K	20G	2SL14P	47	SPA14P	18J03	18J41			
			2SL14N	46	SPA14N	18J02	18J40	STROBE		
		20H	3SL14P	05	SPA14P	18J05	18J41	INPUT		
			3SL14N	04	SPA14N	18J04	18J40	23J20		
	12K	22G	4SL14P	47	SPA14P	19J03	19J41	(SAST1)		
			4SL14N	46	SPA14N	19J02	19J40			
		22H	5SL14P	05	SPA14P	19J05	19J41			
			5SL14N	04	SPA14N	19J04	19J40			
	16K	18G	6SL14P	47	SPA14P	17J03	17J41			
			6SL14N	46	SPA14N	17J02	17J40			
		18H	7SL14P	05	SPA14P	17J05	17J41			
			7SL14N	04	SPA14N	17J04	17J40			
15	4K	24G	0SL15P	45	SPA15P	20J19	20J39	23J23	23J06	23J08
			0SL15N	44	SPA15N	20J18	20J35	(SPA15P)		(MD15)
		24H	1SL15P	07	SPA15P	20J27	20J39	28J24		
			1SL15N	06	SPA15N	20J26	20J38	(SPA15N)		
	8K	20G	2SL15P	45	SPA15P	18J19	18J39			
			2SL15N	55	SPA15N	18J18	18J38	STROBE		
		20H	3SL15P	07	SPA15P	18J27	18J39	INPUT		
			3SL15N	06	SPA15N	18J26	18J38	23J20		
	12K	22G	4SL15P	45	SPA15P	19J19	19J39	(SAST1)		
			4SL15N	44	SPA15N	19J18	19J38			
		22H	5SL15P	07	SPA15P	19J27	19J39			
			5SL15N	06	SPA15N	19J26	19J38			
	16K	18G	6SL15P	45	SPA15P	17J19	17J39			
			6SL15N	44	SPA15N	17J18	17J38			
		18H	7SL15P	07	SPA15P	17J27	17J39			
			7SL15N	06	SPA15N	17J28	17J38			

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Figure 3-26. Core Memory Sense System Charts (Sheet 4 of 9)

DATA BIT	SIZE	C/D MODULE	SENSE LINE		PREAMPLIFIER			SENSE AMPLIFIER		DISCRIM.
			NAME	PIN	NAME	INPUT	OUTPUT	INPUT	OUTPUT	OUTPUT
			0SL16P	01	SPA16P	20J21	20J43	23J25	23J01	23J04
	4K	15H	0SL16N	00	SPA16N	20J20	20J42	(SPA16P)		(MD16)
			1SL16P	51	SPA16P	20J13	20J43	23J26		
		15G	1SL16N	50	SPA16N	20J12	20J42	(SPA16N)		
			2SL16P	01	SPA16P	18J21	18J43			
	8K	11H	2SL16N	00	SPA16N	18J20	18J42	STROBE		
			3SL16P	51	SPA16P	18J13	18J43	INPUT		
		11G	3SL16N	50	SPA16N	18J12	18J42	23J20		
16			4SL16P	01	SPA16P	19J21	19J43	(SAST1)		
	12K	13H	4SL16N	00	SPA16N	19J20	19J42			
			5SL16P	51	SPA16P	19J13	19J43			
		13G	5SL16N	50	SPA16N	19J12	19J42			
			6SL16P	01	SPA16P	17J21	17J43			
	16K	09H	6SL16N	00	SPA16N	17J20	17J42			
			7SL16P	51	SPA16P	17J13	17J43			
		09G	7SL16N	50	SPA16N	17J12	17J42			
			0SL17P	03	SPA17P	20J07	20J45	23J45	23J43	23J40
	4K	15H	0SL17N	02	SPA17N	20J06	20J44	(SPA17P)		(MD17)
			1SL17P	49	SPA17P	20J15	20J45	23J44		
		15G	1SL17N	48	SPA17N	20J14	20J44	(SPA17N)		
			2SL17P	03	SPA17P	18J07	18J45			
	8K	11H	2SL17N	02	SPA17N	18J06	18J44	STROBE		
			3SL17P	49	SPA17P	18J15	18J45	INPUT		
		11G	3SL17N	48	SPA17N	18J14	18J44	23J29		
17			4SL17P	03	SPA17P	19J07	19J45	(SAST1)		
	12K	13H	4SL17N	02	SPA18N	19J06	19J44			
			5SL17P	49	SPA17P	19J15	19J45			
		13G	5SL17N	48	SPA17N	19J14	19J44			
			6SL17P	03	SPA17P	17J07	17J45			
	16K	09H	6SL17N	02	SPA17N	17J06	17J44			
			7SL17P	49	SPA17P	17J14	17J45			
		09G	7SL17N	48	SPA17N	17J14	17J44			
			0SL18P	05	SPA18P	15J09	15J37	09J27	09J33	09J34
	4K	15H	0SL18N	04	SPA18N	15J08	15J36	(SPA18P)		(MD18)
			1SL18P	47	SPA18P	15J11	15J37	09J28		
		15G	1SL18N	46	SPA18N	15J10	15J36	(SPA18N)		
			2SL18P	05	SPA18P	13J09	13J37			
	8K	11H	2SL18N	04	SPA18N	13J08	13J36			
			3SL18P	47	SPA18P	13J11	13J37	STROBE		
		11G	3SL18N	46	SPA18N	13J10	13J36	INPUT		
18			4SL18P	05	SPA18P	14J09	14J37	09J29		
	12K	13H	4SL18N	04	SPA18N	14J08	14J36	(SAST2)		
			5SL18P	47	SPA18P	14J11	14J37			
		13G	5SL18N	46	SPA18N	14J10	14J36			
			6SL18P	05	SPA18P	12J09	12J37			
	16K	09H	6SL18N	04	SPA18N	12J08	12J36			
			7SL18P	47	SPA18P	12J11	12J37			
		09G	7SL18N	46	SPA18N	12J10	12J36			
			0SL19P	07	SPA19P	15J25	15J35	09J22	09J14	09J12
	4K	15H	0SL19N	06	SPA19N	15J24	15J34	(SPA19P)		(MD19)
			1SL19P	45	SPA19P	15J23	15J35	09J21		
		15G	1SL19N	44	SPA19N	15J22	15J34			
			2SL19P	07	SPA19P	13J25	13J35	STROBE		
	8K	11H	2SL19N	06	SPA19N	13J24	13J34	INPUT		
			3SL19P	45	SPA19P	13J23	13J35	09J20		
		11G	3SL19N	44	SPA19N	13J22	13J34	(SAST2)		
19			4SL19P	07	SPA19P	14J25	14J35			
	12K	13H	4SL19N	06	SPA19N	14J24	14J34			
			5SL19P	45	SPA19P	14J23	14J35			
		13G	5SL19N	44	SPA19N	14J22	14J34			
			6SL19P	07	SPA19P	12J25	12J35			
	16K	09H	6SL19N	06	SPA19N	12J24	12J34			
			7SL19P	45	SPA19P	12J23	12J35			
		09G	7SL19N	44	SPA19N	12J22	12J34			

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Figure 3-26. Core Memory Sense System Charts (Sheet 5 of 9)

DATA BIT	SIZE	C/D MODULE	SENSE LINE NAME	SENSE LINE PIN	PREAMPLIFIER NAME	PREAMPLIFIER INPUT	PREAMPLIFIER OUTPUT	SENSE AMPLIFIER INPUT	SENSE AMPLIFIER OUTPUT	DISCRIM. OUTPUT
			0SL20P	51	SPA20P	15J03	15J41	09J23	09J06	09J08
	4K	16G	0SL20N	50	SPA20N	15J02	15J40	(SPA20P)		(MD20)
			1SL20P	01	SPA20P	15J05	15J41	09J24		
		16H	1SL20N	00	SPA20N	15J04	15J40	(SPA20N)		
			2SL20P	51	SPA20P	13J03	13J41			
	8K	12G	2SL20N	50	SPA20N	13J02	13J40			
			3SL20P	01	SPA20P	13J05	13J41	STROBE		
		12H	3SL20N	00	SPA20N	13J04	13J40	INPUT		
20			4SL20P	51	SPA20P	14J03	14J41	09J20		
	12K	14G	4SL20N	50	SPA20N	14J02	14J40	(SAST2)		
			5SL20P	01	SPA20P	14J05	14J41			
		14H	5SL20N	00	SPA20N	14J04	14J40			
			6SL20P	51	SPA20P	12J03	12J41			
	16K	10G	5SL20N	50	SPA20N	12J02	12J40			
			7SL20P	01	SPA20P	12J05	12J41			
		10H	7SL20N	00	SPA20N	12J04	12J40			
			0SL21P	49	SPA21P	15J19	15J39	09J25	09J01	09J04
	4K	16G	0SL21N	48	SPA21N	15J18	15J38	(SPA21P)		(MD21)
			1SL21P	03	SPA21P	15J27	15J39	09J26		
		16H	1SL21N	02	SPA21N	15J26	15J38	(SPA21N)		
			2SL21P	49	SPA21P	13J19	13J39			
	8K	12G	2SL21N	48	SPA21N	13J18	13J38	STROBE		
			3SL21P	03	SPA21P	13J27	13J39	INPUT		
21		12H	3SL21N	02	SPA21N	13J26	13J38	09J20		
			4SL21P	49	SPA21P	14J19	14J39	(SAST2)		
	12K	14G	4SL21N	48	SPA21N	14J18	14J38			
			5SL21P	03	SPA21P	14J27	14J39			
		14H	5SL21N	02	SPA21N	14J26	14J38			
			6SL21P	49	SPA21P	12J19	12J39			
	16K	10G	6SL21N	48	SPA21N	12J18	12J38			
			7SL21P	03	SPA21P	12J26	12J39			
		10H	7SL21N	02	SPA21N	12J26	12J38			
			0SL22P	47	SPA22P	15J21	15J43	08J45	08J43	08J40
	4K	16G	0SL22N	46	SPA22N	15J20	15J42	(SPA22P)		(MD22)
			1SL22P	05	SPA22P	15J13	15J43	08J44		
		16H	1SL22N	04	SPA22N	15J12	15J42	(SPA22N)		
			2SL22P	47	SPA22P	13J21	13J43			
	8K	12G	2SL22N	46	SPA22N	13J20	13J42			
			3SL22P	05	SPA22P	13J13	13J43	STROBE		
		12H	3SL22N	04	SPA22N	13J12	13J42	INPUT		
22			4SL22P	47	SPA22P	14J21	14J43	08J29		
	12K	14G	4SL22N	46	SPA22N	14J20	14J42	(SAST2)		
			5SL22P	05	SPA22P	14J13	14J43			
		14H	5SL22N	04	SPA22N	14J12	14J42			
			6SL22P	47	SPA22P	12J21	12J43			
	16K	10G	6SL22N	46	SPA22N	12J20	12J42			
			7SL22P	05	SPA22P	12J13	12J43			
		10H	7SL22N	04	SPA22N	12J12	12J42			
			0SL23P	45	SPA23P	15J07	15J45	08J46	08J39	08J38
	4K	16G	0SL23N	44	SPA23N	15J06	15J44	(SPA23P)		(MD23)
			1SL23P	07	SPA23P	15J15	15J45	08J46		
		16H	1SL23N	06	SPA23N	15J14	15J44	(SPA23N)		
			2SL23P	45	SPA23P	13J07	13J45			
	8K	12G	2SL23N	44	SPA23N	13J06	13J44	STROBE		
			3SL23P	07	SPA23P	13J15	13J45	INPUT		
23		12H	3SL23N	06	SPA23N	13J14	13J44	08J29		
			4SL23P	45	SPA23P	14J07	14J45	(SAST2)		
	12K	14G	4SL23N	44	SPA23N	14J06	14J44			
			5SL23P	07	SPA23P	14J15	14J45			
		14H	5SL23N	06	SPA23N	14J14	14J44			
			6SL23P	45	SPA23P	12J07	12J45			
	16K	10G	6SL23N	44	SPA23N	12J06	12J44			
			7SL23P	07	SPA23P	12J15	12J45			
		10H	7SL23N	06	SPA23N	12J14	12J44			

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Figure 3-26. Core Memory Sense System Charts (Sheet 6 of 9)

DATA BIT	SIZE	C/D MODULE	SENSE LINE NAME	SENSE LINE PIN	PREAMPLIFIER NAME	PREAMPLIFIER INPUT	PREAMPLIFIER OUTPUT	SENSE AMPLIFIER INPUT	SENSE AMPLIFIER OUTPUT	DISCRIM. OUTPUT
24	4K		0SL24P	01	SPA24P	11J09	11J37	08J22	08J14	08J12
		07H	0SL24N	00	SPA24N	11J08	11J36	(SPA24P)		(MD24)
			1SL24P	51	SPA24P	11J11	11J37	08J21		
		07G	1SL24N	50	SPA24N	11J10	11J36	(SPA24N)		
	8K		2SL24P	01	SPA24P	05J09	05J37			
		03H	2SL24N	00	SPA24N	05J08	05J36	STROBE		
			3SL24P	51	SPA24P	05J11	05J37	INPUT		
		03G	3SL24N	50	SPA24N	05J10	05J36	08J20		
	12K		4SL24P	01	SPA24P	10J09	10J37	(SAST3)		
		05H	4SL24N	00	SPA24N	10J08	10J36			
			5SL24P	51	SPA24P	10J11	10J37			
		05G	5SL24N	50	SPA24N	10J10	10J36			
	16K		6SL24P	01	SPA24P	04J09	04J37			
		01H	6SL24N	00	SPA24N	04J08	04J36			
			7SL24P	51	SPA24P	04J11	04J37			
		01G	7SL24N	50	SPA24N	04J10	04J36			
25	4K		0SL25P	03	SPA25P	11J25	11J35	08J23	08J06	08J08
		07H	0SL25N	02	SPA25N	11J24	11J34	(SPA25P)		(MD25)
			1SL25P	49	SPA25P	11J23	11J35	08J24		
		07G	1SL25N	48	SPA25N	11J22	11J34	(SPA25N)		
	8K		2SL25P	03	SPA25P	05J25	05J35			
		03H	2SL25N	02	SPA25N	05J24	05J34	STROBE		
			3SL25P	49	SPA25P	05J23	05J35	INPUT		
		03G	3SL25N	48	SPA25N	05J22	05J34	08J20		
	12K		4SL25P	03	SPA25P	10J25	10J35	(SAST3)		
		05H	4SL25N	02	SPA25N	10J24	10J34			
			5SL25P	49	SPA25P	10J23	10J35			
		05G	5SL25N	48	SPA25N	10J22	10J34			
	16K		6SL25P	03	SPA25P	04J25	04J35			
		01H	5SL25N	02	SPA25N	04J24	04J34			
			7SL25P	49	SPA25P	04J23	04J35			
		01G	7SL25N	48	SPA25N	04J22	04J34			
26	4K		0SL26P	05	SPA26P	11J03	11J41	08J25	08J01	08J04
		07H	0SL26N	04	SPA26N	11J02	11J40	(SPA26P)		(MD26)
			1SL26P	47	SPA26P	11J05	11J41	08J26		
		07G	1SL26N	46	SPA26N	11J04	11J40	(SPA26N)		
	8K		2SL26P	05	SPA26P	05J03	05J41			
		03H	2SL26N	04	SPA26N	05J02	05J40	STROBE		
			3SL26P	47	SPA26P	05J04	05J41	INPUT		
		03G	3SL26N	46	SPA26N	05J04	05J40	08J20		
	12K		4SL26P	05	SPA26P	10J03	10J41	(SAST3)		
		05H	4SL26N	04	SPA26N	10J02	10J40			
			5SL26P	47	SPA26P	10J05	10J41			
		05G	5SL26N	46	SPA26N	10J04	10J40			
	16K		6SL26P	05	SPA26P	04J03	04J41			
		01H	6SL26N	04	SPA26N	04J02	04J40			
			7SL26P	47	SPA26P	04J05	04J41			
		01G	4SL26N	46	SPA26N	04J04	04J40			
27	4K		0SL27P	07	SPA27P	11J19	11J39	06J45	06J43	06J40
		07H	0SL27N	06	SPA27N	11J18	11J38	(SPA27P)		(MD27)
			1SL27P	45	SPA27P	11J27	11J39	06J44		
		07G	1SL27N	44	SPA27N	11J26	11J38	(SPA27N)		
	8K		2SL27P	07	SPA27P	05J19	05J39			
		03H	2SL27N	06	SPA27N	05J18	05J38	STROBE		
			3SL27P	45	SPA27P	05J27	05J39	INPUT		
		03G	3SL27N	44	SPA27N	05J26	05J38	06J29		
	12K		4SL27P	07	SPA27P	10J19	10J39	(SAST3)		
		05H	4SL27N	06	SPA27N	10J18	10J38			
			5SL27P	45	SPA27P	10J27	10J39			
		05G	5SL27N	44	SPA27N	10J26	10J38			
	16K		5SL27P	07	SPA27P	04J19	04J39			
		01H	6SL27N	05	SPA27N	04J18	04J38			
			7SL27P	45	SPA27P	04J27	04J39			
		01G	7SL27N	44	SPA27N	04J26	04J38			

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Figure 3-26. Core Memory Sense System Charts (Sheet 7 of 9)

DATA BIT	SIZE	C/D MODULE	SENSE LINE NAME	SENSE LINE PIN	PREAMPLIFIER NAME	PREAMPLIFIER INPUT	PREAMPLIFIER OUTPUT	SENSE AMPLIFIER INPUT	SENSE AMPLIFIER OUTPUT	DISCRIM. OUTPUT
			0SL28P	51	SPA28P	11J21	11J43	06J47	06J39	06J38
	4K	08G	0SL28N	50	SPA28N	11J20	11J42	(SPA28P)		(MD28)
			1SL28P	01	SPA28P	11J13	11J43	06J46		
		08H	1SL28N	00	SPA28N	11J12	11J42	(SPA28N)		
			2SL28P	51	SPA28P	05J21	05J43			
	8K	04G	2SL28N	50	SPA28N	05J20	05J42			
			3SL28P	01	SPA28P	05J13	05J43	STROBE		
		04H	3SL28N	00	SPA28N	05J12	05J42	INPUT		
28			4SL28P	51	SPA28P	10J21	10J43	06J29		
	12K	06G	4SL28N	50	SPA28N	10J20	10J42	(SAST3)		
			5SL28P	01	SPA28P	10J13	10J43			
		06H	5SL28N	00	SPA28N	10J12	10J42			
			6SL28P	51	SPA28P	04J21	04J43			
	16K	02G	6SL28N	50	SPA28N	04J20	04J42			
			7SL28P	01	SPA28P	04J13	04J43			
		02H	7SL28N	00	SPA28N	04J12	04J42			
			0SL29P	49	SPA29P	11J07	11J45	06J27	06J33	06J34
	4K	08G	0SL29N	48	SPA29N	11J06	11J44	(SPA29P)		(MD29)
			1SL29P	03	SPA29P	11J15	11J45	06J28		
		08H	1SL29N	02	SPA29N	11J14	11J44	(SPA29N)		
			2SL29P	49	SPA29P	05J07	05J45			
	8K	04G	2SL29N	48	SPA29N	05J06	05J44	STROBE		
			3SL29P	03	SPA29P	05J15	05J45	INPUT		
		04H	3SL29N	02	SPA29N	05J14	05J44	06J29		
29			4SL29P	49	SPA29P	10J07	10J45	(SAST3)		
	12K	06G	4SL29N	48	SPA29N	10J06	10J44			
			5SL29P	03	SPA29P	10J15	10J45			
		06H	5SL29N	02	SPA29N	10J14	10J44			
			6SL29P	49	SPA29P	04J07	04J45			
	16K	02G	6SL29N	48	SPA29N	04J06	04J44			
			7SL29P	03	SPA29P	04J15	04J45			
		02H	7SL29N	02	SPA29N	04J14	04J44			
			0SL30P	47	SPA30P	03J09	03J37	06J22	06J14	06J12
	4K	08G	0SL30N	46	SPA30N	03J08	03J36	(SPA30P)		(MD30)
			1SL30P	05	SPA30P	03J11	03J37	06J21		
		08H	1SL30N	04	SPA30N	03J10	03J36			
			2SL30P	47	SPA30P	03J19	03J39			
	8K	04G	2SL30N	46	SPA30N	03J18	03J38	STROBE		
			3SL30P	05	SPA30P	03J27	03J39	INPUT		
		04H	3SL30N	04	SPA30N	03J26	03J38	06J20		
30			4SL30P	47	SPA30P	02J09	02J37	(SAST3)		
	12K	06G	4SL30N	46	SPA30N	02J08	02J36			
			5SL30P	05	SPA30P	02J11	02J37			
		06H	5SL30N	04	SPA30N	02J10	02J36			
			6SL30P	47	SPA30P	02J19	02J39			
	16K	02G	6SL30N	46	SPA30N	02J18	02J38			
			7SL30P	05	SPA30P	02J27	02J39			
		02H	7SL30N	04	SPA30N	02J26	02J38			

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Figure 3-26. Core Memory Sense System Charts (Sheet 8 of 9)

DATA BIT	SIZE	C/D MODULE	SENSE LINE NAME	SENSE LINE PIN	PREAMPLIFIER NAME	PREAMPLIFIER INPUT	PREAMPLIFIER OUTPUT	SENSE AMPLIFIER INPUT	SENSE AMPLIFIER OUTPUT	DISCRIM. OUTPUT
31	4K	08G	0SL31P	45	SPA31P	03J25	03J35	06J23	06J06	06J08
			0SL31N	44	SPA31N	03J24	03J34	(SPA31P)		(MD31)
		08H	1SL31P	07	SPA31P	03J23	03J35	06J24		
			1SL31N	06	SPA31N	03J22	03J34	(SPA31N)		
	8K	04G	2SL31P	45	SPA31P	03J21	03J43			
			2SL31N	44	SPA31N	03J20	03J42	STROBE		
		04H	3SL31P	07	SPA31P	03J13	03J43	INPUT		
			3SL31N	06	SPA31N	03J12	03J42	06J20		
	12K	06G	4SL31P	45	SPA31P	02J25	02J35	(SAST3)		
			4SL31N	44	SPA31N	02J24	02J34			
		06H	5SL31P	07	SPA31P	02J23	02J35			
			5SL31N	06	SPA31N	02J22	02J34			
	16K	02G	6SL31P	45	SPA31P	02J21	02J43			
			6SL31N	44	SPA31N	02J20	02J42			
		02H	7SL31P	07	SPA31N	02J13	02J43			
			7SL31N	06	SPA31P	02J12	02J42			
32 (Parity)	4K	07H	0SL32P	09	SPA32P	03J03	03J41	06J25	06J01	06J04
			0SL32N	08	SPA32N	03J02	03J40	(SPA32P)		(MD32)
		07G	1SL32P	43	SPA32P	03J05	03J41	06J26		
			1SL32N	42	SPA32N	03J04	03J40	(SPA32N)		
	8K	03H	2SL32P	09	SPA32P	03J07	03J45			
			2SL32N	08	SPA32N	03J06	03J44			
		03G	3SL32P	43	SPA32P	03J15	03J45	STROBE		
			3SL32N	42	SPA32N	03J14	03J44	INPUT		
	12K	05H	4SL32P	09	SPA32P	02J03	02J41	06J20		
			4SL32N	08	SPA32N	02J02	02J40	(SAST3)		
		05G	5SL32P	43	SPA32P	02J05	02J41			
			5SL32N	42	SPA32N	02J04	02J40			
	16K	01H	5SL32P	09	SPA32P	02J07	02J45			
			6SL32N	08	SPA32N	02J06	02J44			
		01G	7SL32P	43	SPA32P	02J15	02J45			
			7SL32N	42	SPA32N	02J14	02J44			

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Figure 3-26. Core Memory Sense System Charts (Sheet 9 of 9)

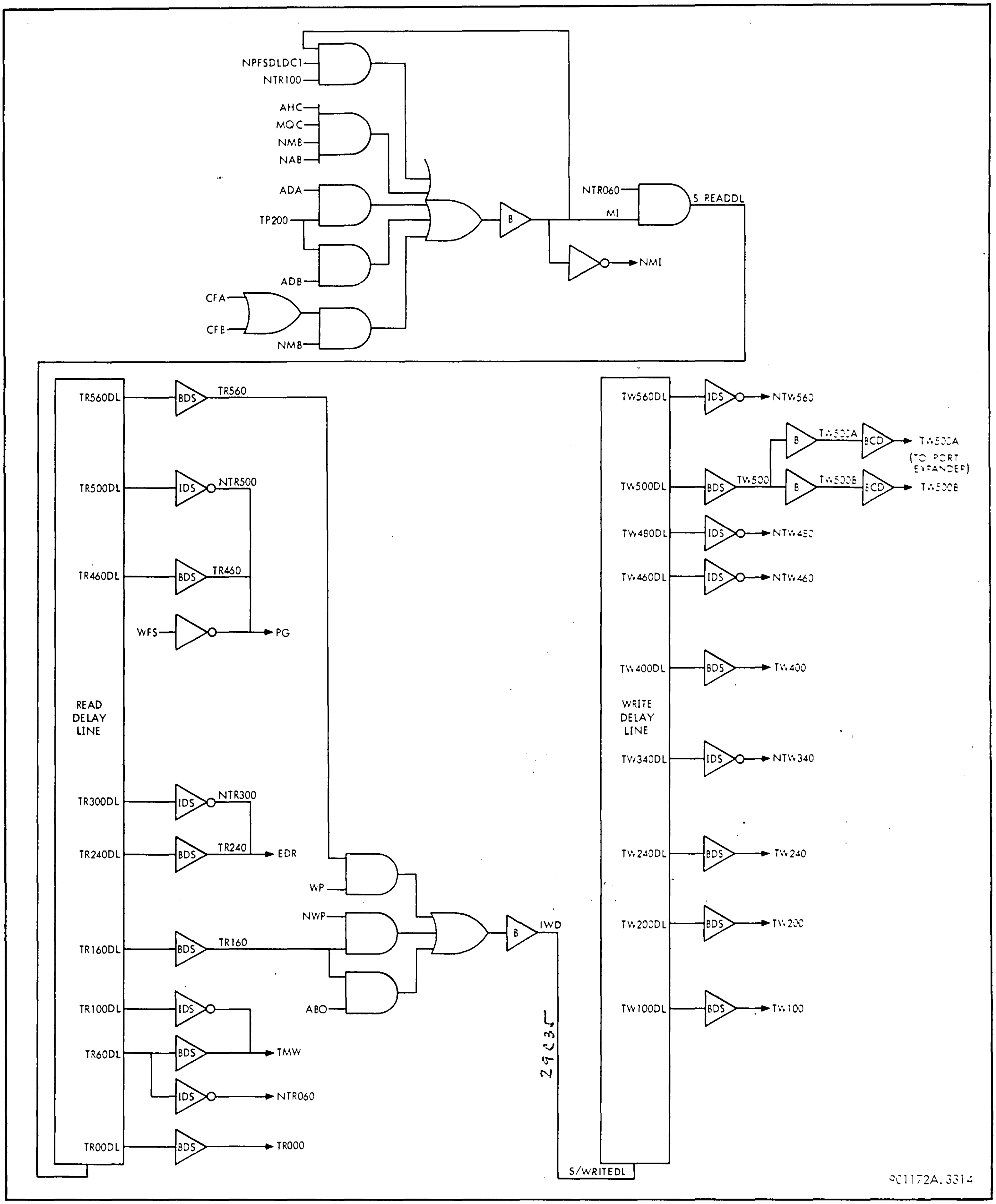


Figure 3-27. Read and Write Delay Lines, Simplified Logic Diagram

This produces a 60-ns pulse on the line. The write delay line is initiated at TR160 for a full write operation (NWP true) or at TR560 for a partial write (WP true). The partial write mode requires a longer time between the read half-cycle and the write half-cycle. In this mode, parity is checked after the read half-cycle and new parity is generated before the write half-cycle is initiated. In the full write mode, parity checking is omitted after the read half-cycle. Timing for different modes and ports is discussed in paragraph 3-27.

In figure 3-27 note that signal S/READDL, which initiates a memory cycle, is the result of the memory initiate signal, MI. This signal is latched for 100 ns after it goes true (it is disabled by TR100). As indicated in the figure, any one of four AND gates can bring up MI as follows:

a. If port C has recognized the address (AHC), if the source has sent a memory request (MQC), if the memory bank is not busy (NMB) with another memory cycle, and if neither port A nor port B has been given access

b. If port A has been given the access decision (ADA) and if the port priority delay line has run out (TP200)

c. If port B has been given the access decision (ADB) and if the port priority delay line has run out (TP200)

d. If a cycle has just been completed (NMB) and if either port A or port B has had a memory request before TW320 time of that cycle (CFA or CFB, respectively). This is the result of an early access decision, explained in detail in paragraph 3-31.

3-27 MEMORY CYCLE TIMING

Timing for read-restore, full clear-write or partial write cycles using port C is shown in figures 3-28, 3-29, and 3-30, respectively. These diagrams contain ideal waveforms reflecting the logic equations and are not intended to show actual times since delays due to differences in cable lengths and other variables are omitted. The logic used to generate these diagrams is listed in the sets of sequence charts contained in section IV. The charts may be compared to the timing diagrams for a detailed analysis of each memory cycle type.

Since a read and a write operation occur in every cycle, the timing diagrams are similar with only a few exceptions.

The write delay line is initiated to restore the entire word to the cores after new parity is generated. In the partial write cycle, the write delay line is not started until TR560 instead of TR160. This allows time to modify the word in the M-register. Before TR560, a word is read into the M-register from the cores and parity is checked. Signal MXM at TR480 goes false to clear out the unwanted byte or bytes according to the write-byte configuration. Then MXC (or MXB or MXA) transfers a new byte (or bytes) into the M-register from the active port.

3-28 MODE CONTROL

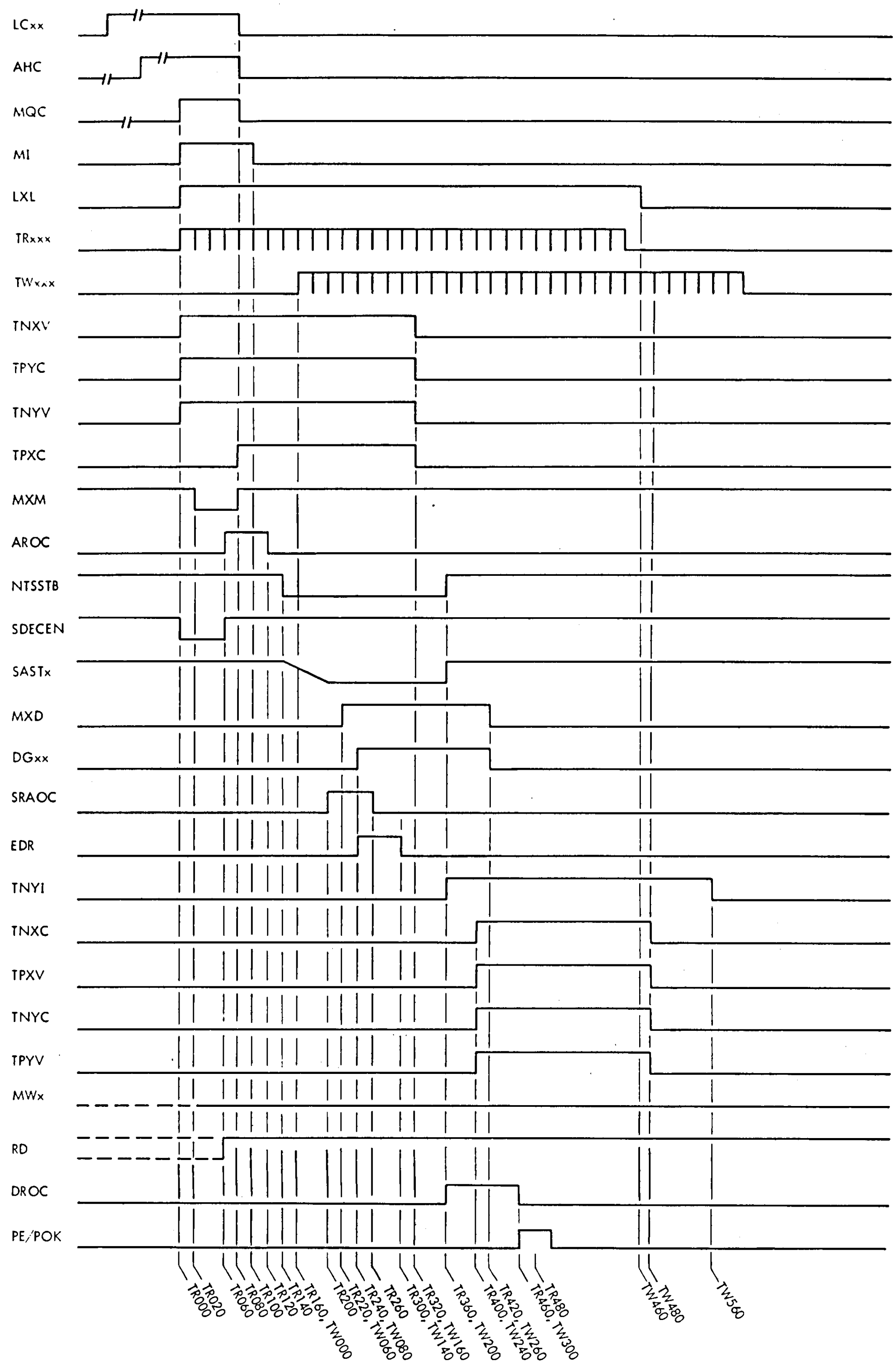
The three modes of operation, read-restore, full clear-write, and partial write, are controlled by the write byte latches set by the write byte lines of the accessed port. The write byte configuration determines the mode of operation. Figure 3-31 is a simplified logic diagram showing the write byte and mode control logic. The write byte lines of each port are fed to the write byte latches, together with the corresponding port access decision signal (for example ADCMW, . . .) and a timing signal from the read delay line, TMW. The latch outputs, MW0 through MW3 are decoded by the mode control logic. The chart in the figure shows the result of the decode. Any configuration of the byte indicators other than all false (read) or all true (write) results in the partial write mode. However, this is not true if an operation is aborted. An abort signal is generated by the CPU if an instruction attempts to write into a protected area of memory. A true abort signal on the port that has access causes mode signals write full and write partial (WF and WP) to be grounded if the abort signal occurs within 100 ns after the read delay line is initiated. This also clears the write byte latches MW0 through MW3, making them all zero. With the byte latches all zero, the mode is changed from a write mode to a read mode thus preserving the protected area of memory. If a partial write mode is aborted, the write delay line is initiated at TR160 instead of TR560 time.

3-29 M-REGISTER CONTROL

The logic diagram for the most significant bit of the M-register, M00, is shown in figure 3-32. This is typical of all M-register bits M00 through M31. Parity bit M32 is a special case and is discussed in paragraph 3-30. The left side of the diagram shows the input gating to latch M00 with data from a port (MA00, MB00, MC00). The gating to latch M00 from the sense line discriminator (MD00) is also shown. Data from the sense line discriminators is also applied to the gates shown on the right side of the diagram. Through this gating, with signal DG(XX), the condition of M00 or the discriminator output is gated onto the output lines to the source. The status of M00 is restored to the cores through the gates shown on the lower right side of the diagram. The data is output to the Y-inhibit circuits.

3-30 PARITY CHECKING AND GENERATION

The Sigma 5 and 7 memory employs odd parity; that is, if any word stored in memory contains an even number of ones, bit M32 contains a one, or if any word in memory contains an odd number of ones, bit M32 contains a zero. Parity is checked when a word enters the M-register from the cores during either a read-restore or partial write operation. Four levels of parity generators are used to test the word for an odd or an even number of ones. Figure 3-33 shows the four parity scheme levels. A fifth logic level reflects the status of each parity check. If the parity check is satisfactory, signal POK goes true; if a parity error exists, PE goes true. The parity circuitry shown in figure 3-33 is used for both checking and generating odd parity.



NOTE: SOURCE MAY USE ADDRESS RELEASE TO DROP MQC AND ADDRESS LINES

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Figure 3-28. Read-Restore, Port C, Timing Diagram

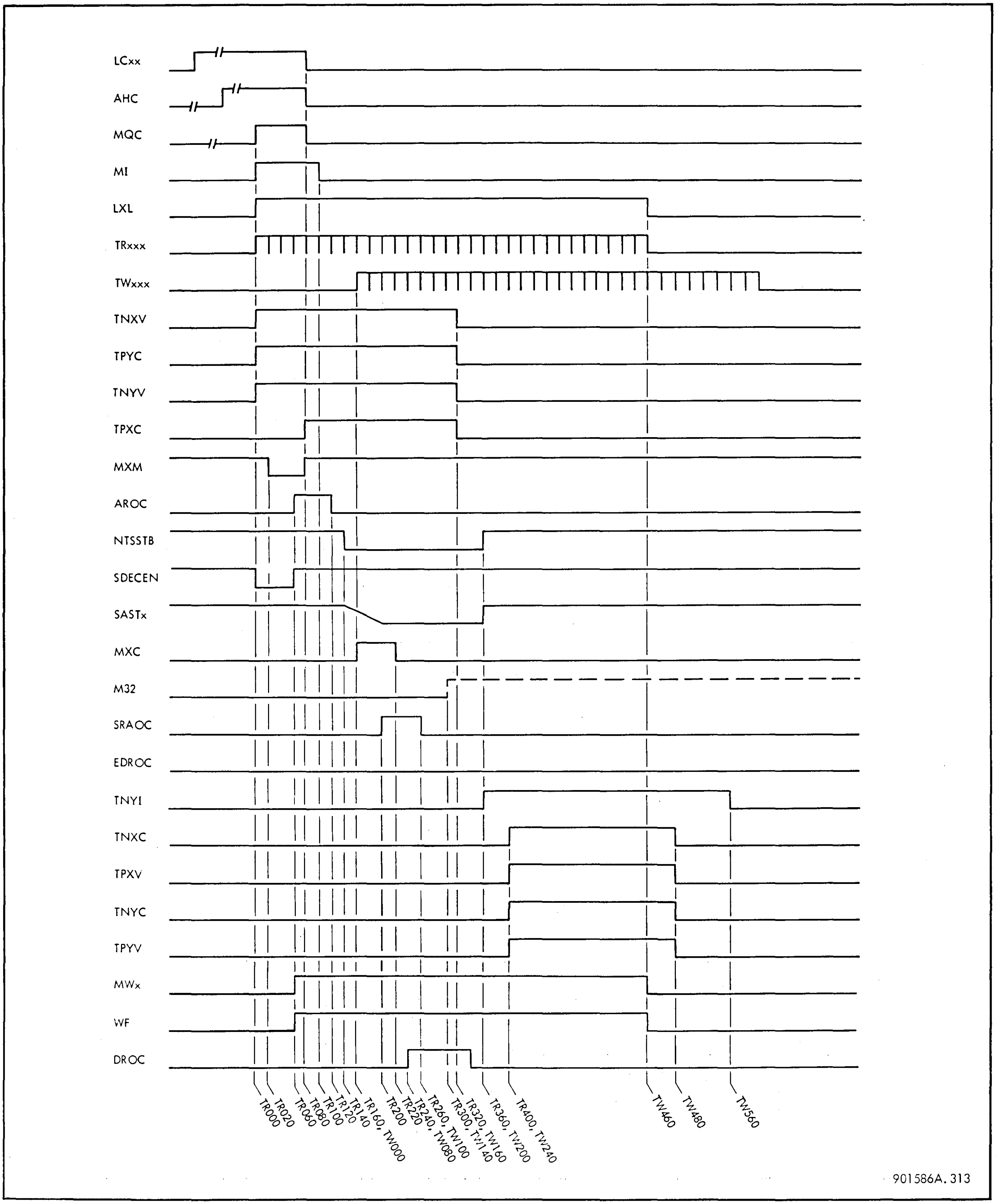

Figure 3-29. Full Clear-Write, Port C, Timing Diagram

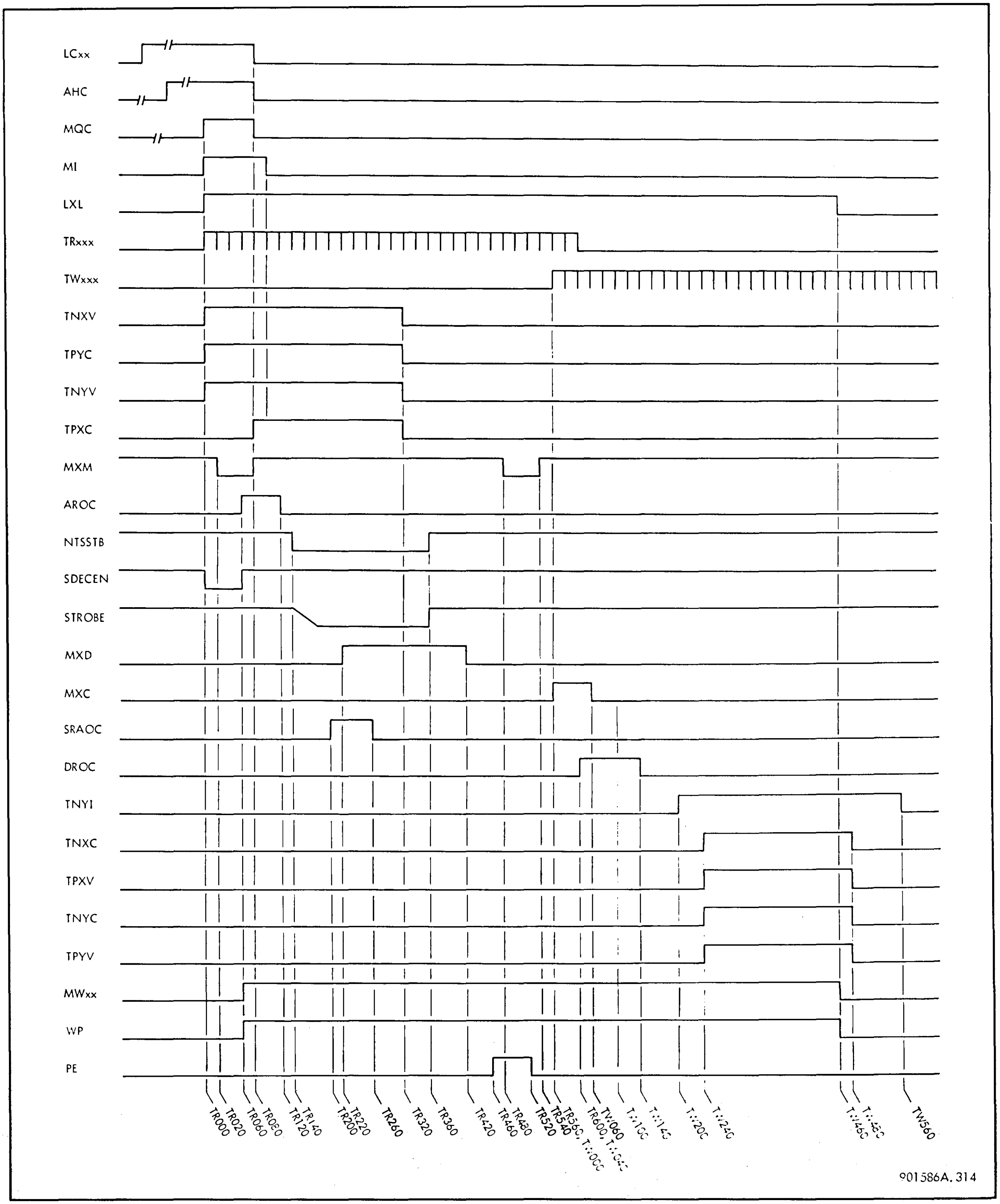

Figure 3-30. Partial Write, Port C, Timing Diagram

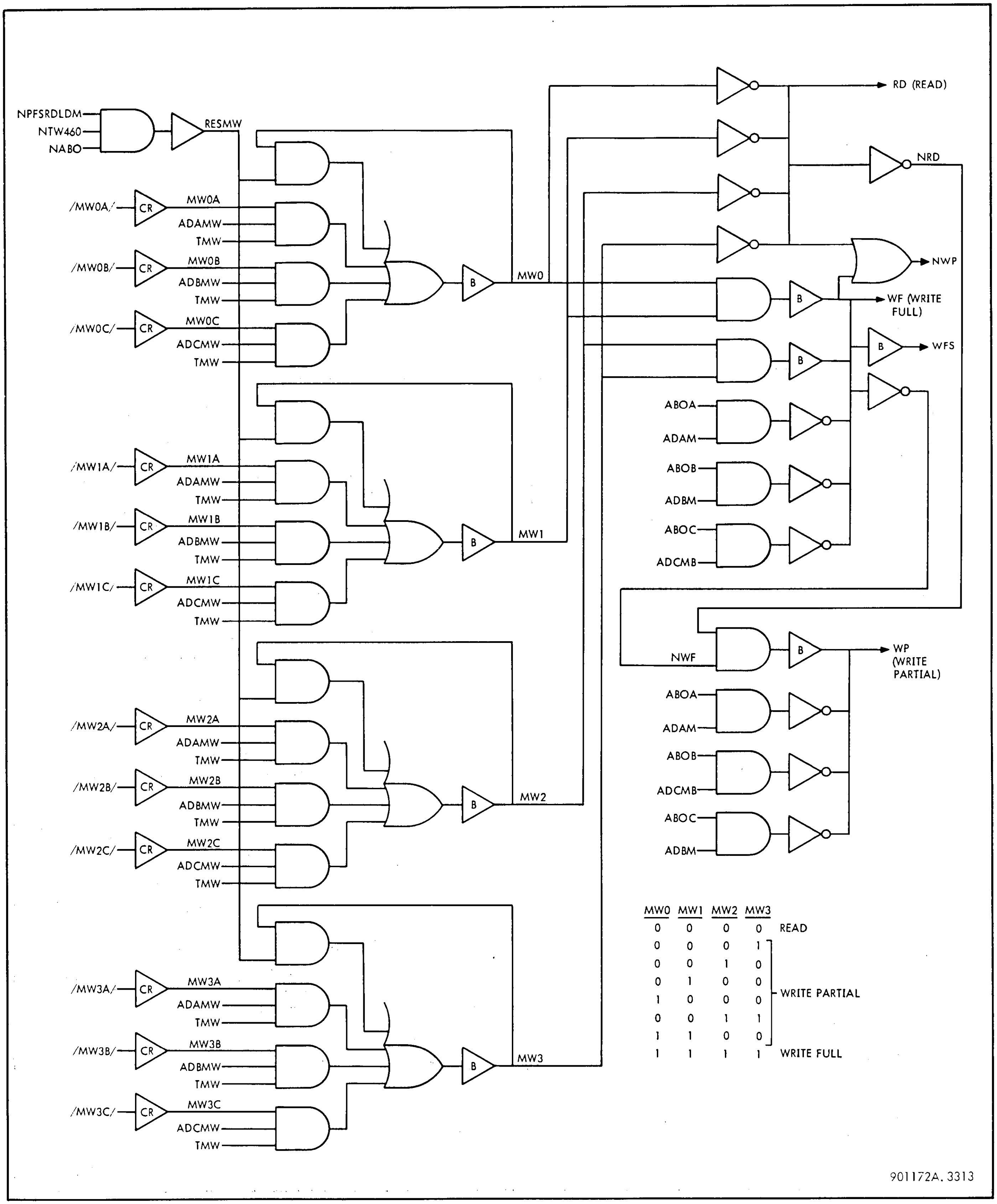

Figure 3-31. Write Byte and Mode Control, Simplified Logic Diagram

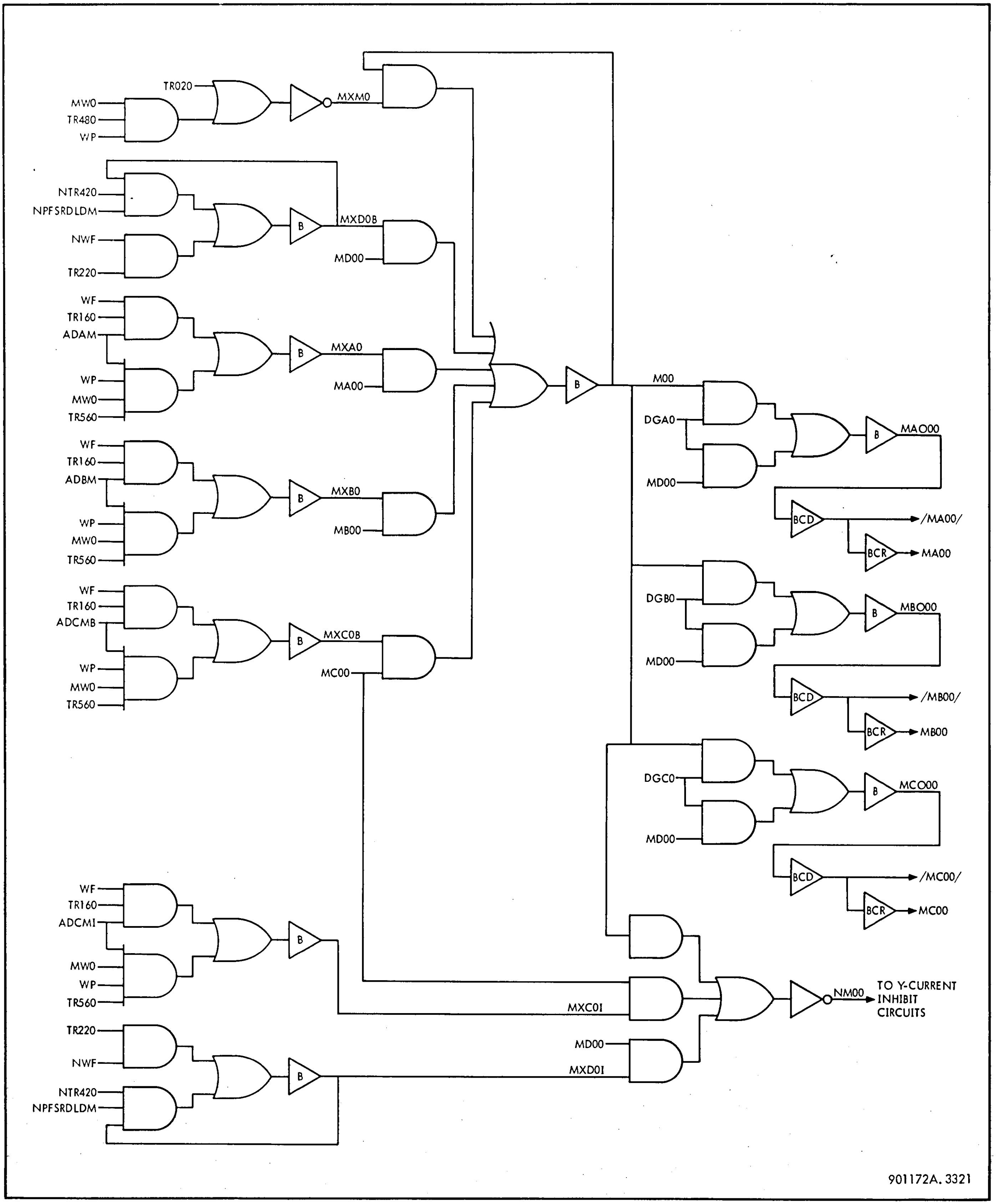

Figure 3-32. M-Register (M00, Typical of M00-M31), Simplified Logic Diagram

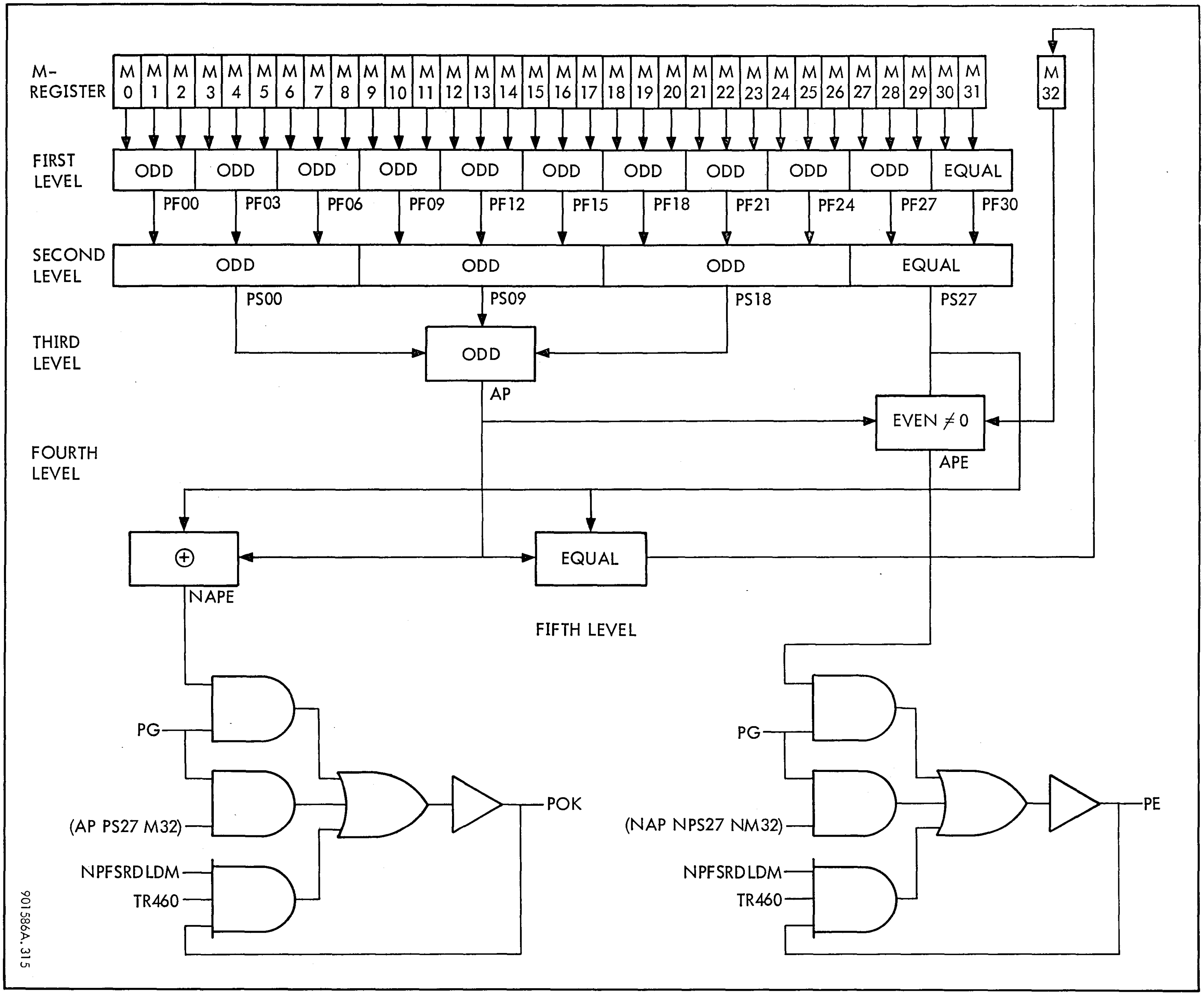

Figure 3-33. Parity Network, Simplified Logic Diagram

Signal NAPE (not a parity error) is true when either PS27 or AP is true and when the other is false. In the case when both PS27 and AP are both true or both false (or equal), a signal is generated to set M32. Then when parity gate PG is true, POK is generated.

To determine a parity error, PS27, AP and M32 are tested. Signal APE goes true if their sum is even but is not zero. Signal PE is generated when signal PG occurs. Signals PS27, AP, and M32 are also gated with PG to handle the case when they are all zeros or all ones. If all zeros, PE is generated; if all ones, POK is generated.

3-31 PORT PRIORITY AND TIMING

The time interval between the receipt of a memory request at a port and the occurrence of TO is called the selection interval. The time between TO and the end of a memory cycle is the active interval. The selection interval is widely variable depending on which port is requesting service, the current state of the memory, the mode operation, and current and subsequent requests at other ports. Figure 3-34 shows read-restore timing for access through either port A or port B. The normal selection shown in the figure is 200 ns and is the result of two port delay lines each 100 ns long. (See figure 3-35.) A priority decision for the next cycle is called an early access decision when it is successfully gained before TW320 time of the current cycle. This involves port A and port B only. Port C cannot gain access while either port A or port B has access. As shown in figure 3-34, a memory request on port B (MQB) before TW320 of the cycle where port A has access (MQA) allows port B to gain an early access decision. However, this occurs only because port A does not have another memory request. If another request is present on port A, the early access decision would go to port A. Thus, port A would access for another cycle.

Figure 3-36 shows the logic involved in a priority decision and figure 3-37 shows the port priority timing. Network A in figure 3-36 determines the early access decision, if one occurs. Signal CFA (cycle for A) or CFB (cycle for B) is generated in that case. If an early access decision is not possible (for example, after TW320), network B is enabled. The outputs of both network B and network A are applied to network C which produces the access decision signals. Note that if neither port A nor port B has been given access (ADA and ADB, respectively), signal ADC is true and port C gains access if a memory request is present.

The address release logic in figure 3-36 shows how the access decision signals are used to generate the address release signal at TR60 of the memory cycle.

3-32 PORT OVERRIDE

Port access priority can be overriden by a port override signal from the source. The logic diagram in figure 3-38 shows how a given override signal grounds any memory requests on the other two ports designated by the override signal. The remaining port can then gain access when the current cycle is completed. Note that a port override signal

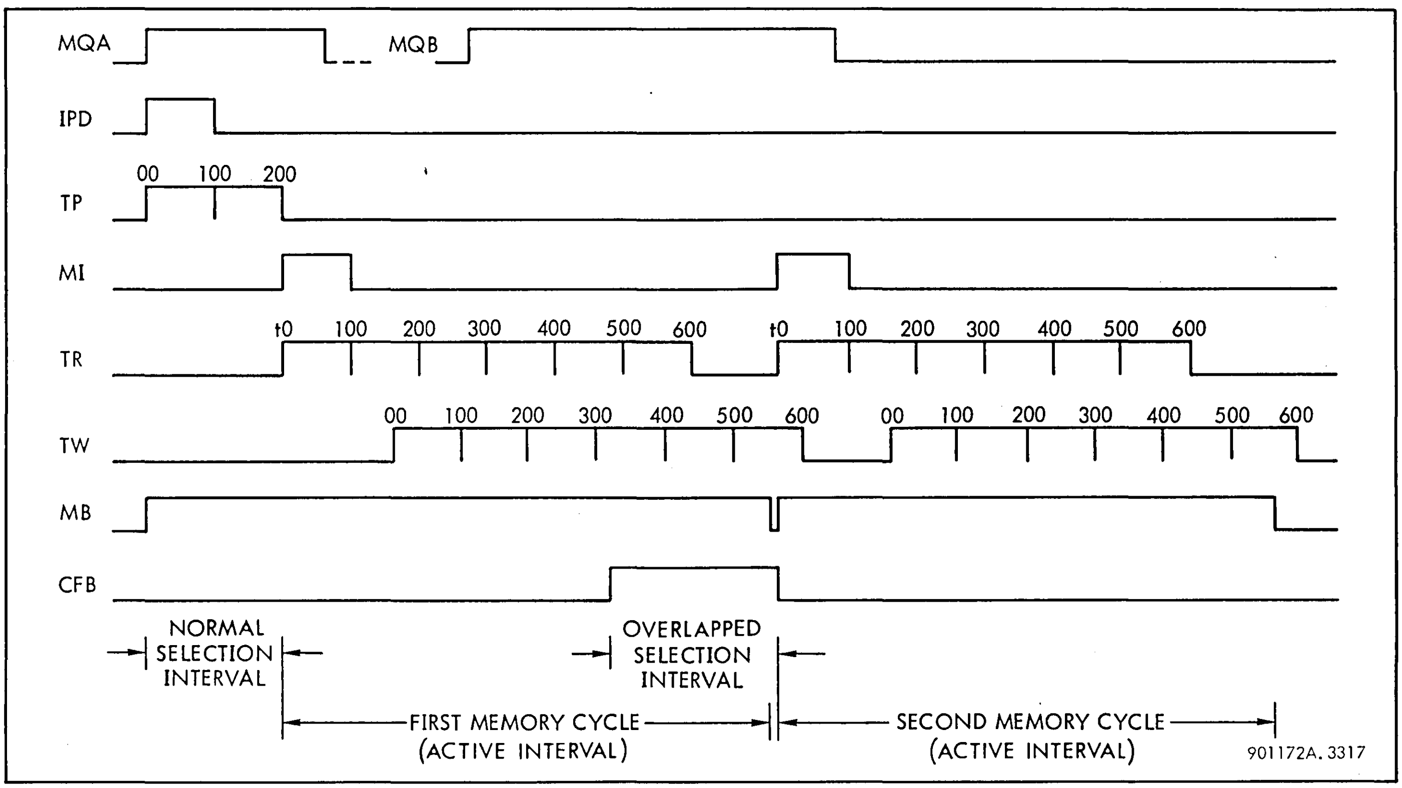

Figure 3-34. Read-Restore Timing for Port A or B

does not interrupt a priority decision if one is in progress. Signal NAB (not A and not B) cannot go true until both APA and APB are false. If all override signals are true, no requests are allowed to go true.

3-33 L-REGISTER CONTROL

Control of the L-register for receiving an address involves signals derived from the access decision signals. Figure 3-39 shows the logic and timing involved. The control timing diagram in the figure shows how the L-register is cleared at TW460 of each cycle (LXL and LXL0B) and is again enabled at the beginning of the next cycle. Signal LG and either signal ADAS, ADBS or ADC are true depending on which port has access for the next cycle. The address is latched into the L-register by the time TR060 arrives in the current cycle, so at that time, signal LG goes false.

3-34 MEMORY BUSY AND MEMORY RESET

The memory busy logic is shown in figure 3-40. Signal MB goes true when a memory cycle is initiated (MI), a port delay is initiated (IPD), or a HALT signal occurs. Either a memory reset (MR) or a combination of a memory fault reset (MFR) or parity error (PE) with a halt on fault (HOF) generates a HALT signal. Signal MB true indicates that the memory is engaged and that no new memory requests can be processed. The 2-3 μs delay line in the figure allows sufficient time for the current cycle to be completed before disabling MB.

The memory reset logic is shown in figure 3-41. The memory is held reset while power is being applied or removed from the system, by signal ST, and also when manual reset signal MRA, MRB or MRC is generated. With MR(X) true, signal HALT is generated and, by setting MB, inhibits any new memory requests from being processed. After an average delay of 2 μs to allow time for the current cycle to be completed, signal MRD goes true, generating PFSRDLD. This signal drops all of the reset signals shown in figure 3-41. Thus all of the indicated latches are cleared. The memory fault latch, MF, shown in the figure is also cleared. Signal MF is generated by a parity error and is then gated with the bank number switches to control the memory fault indicators on the PCP. Latch MF can be cleared by the system reset signal or by the memory fault reset signal, MFR, shown in figure 3-41.

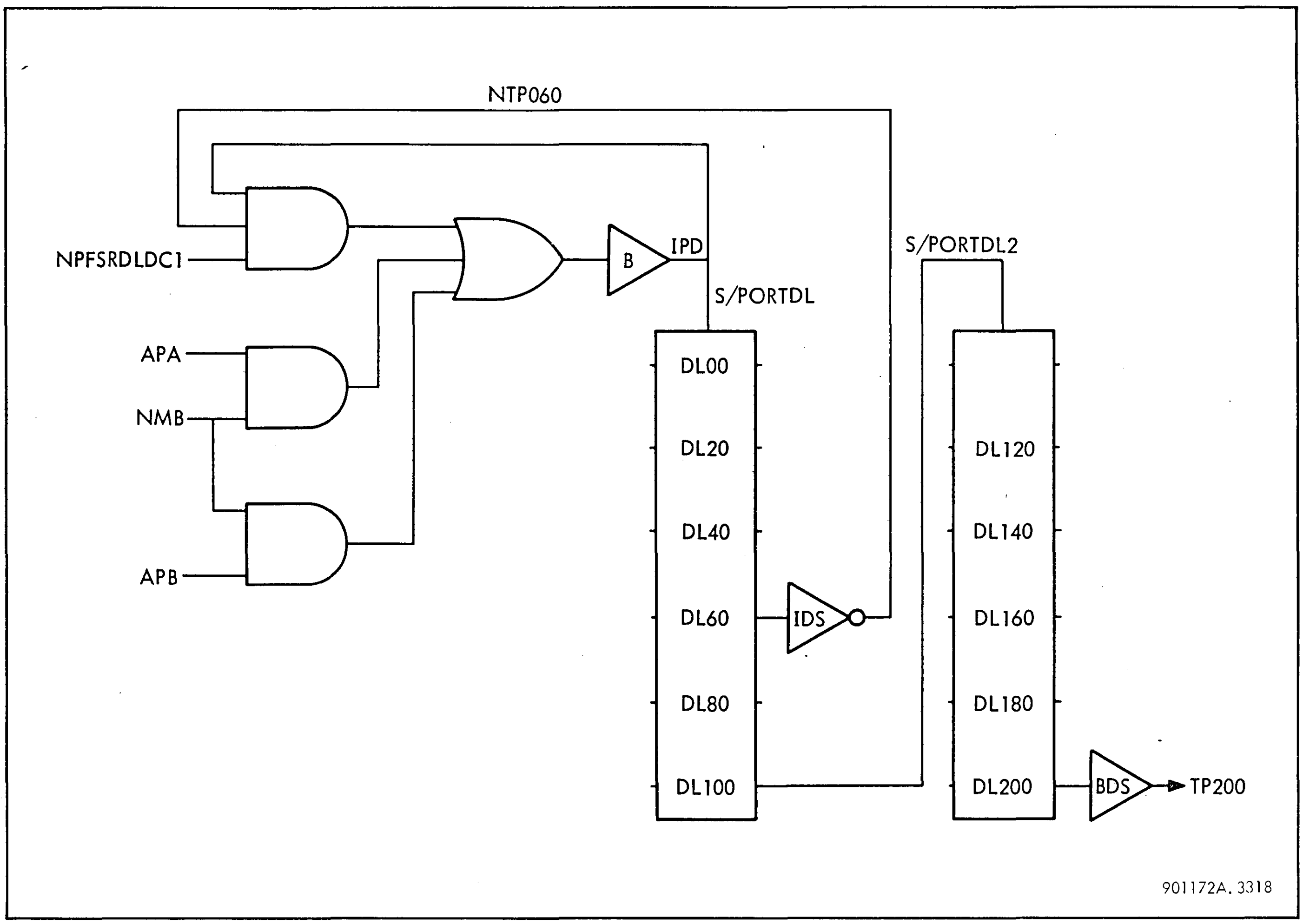

Figure 3-35. Ports A and B Delay Line, Simplified Logic Diagram

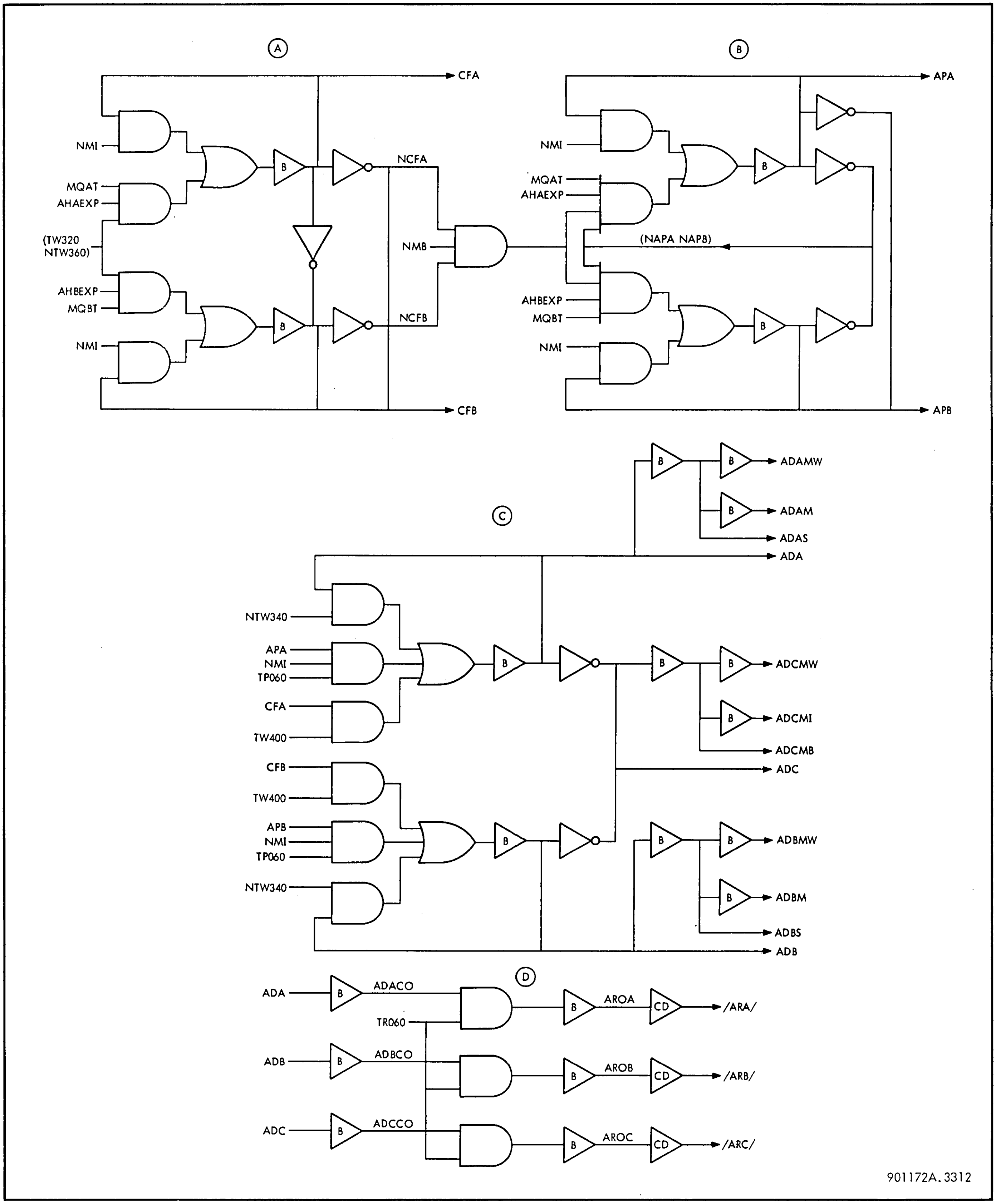

Figure 3-36. Port Priority and Address Release, Simplified Logic Diagram

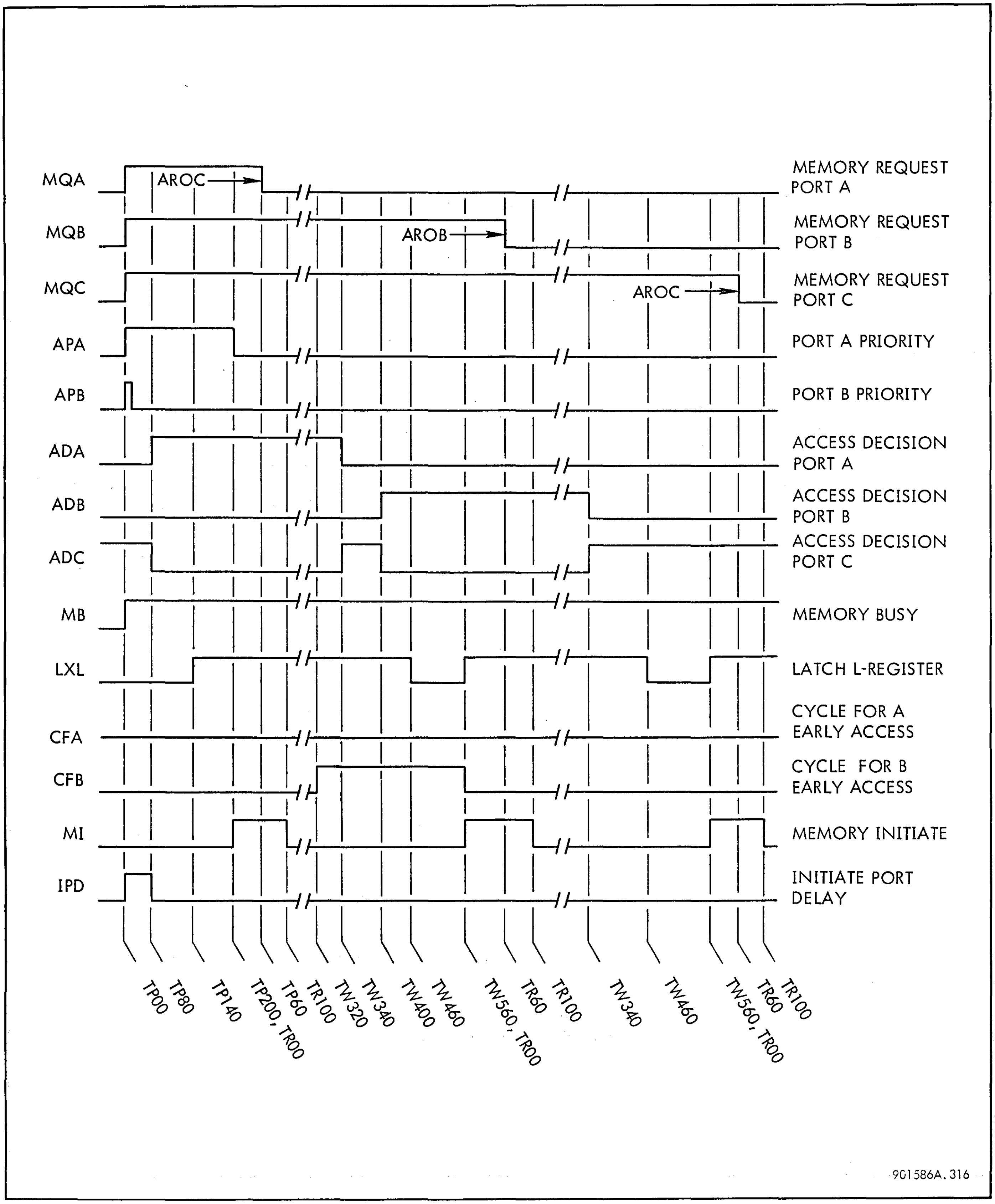

Figure 3-37. Port Priority Timing Diagram

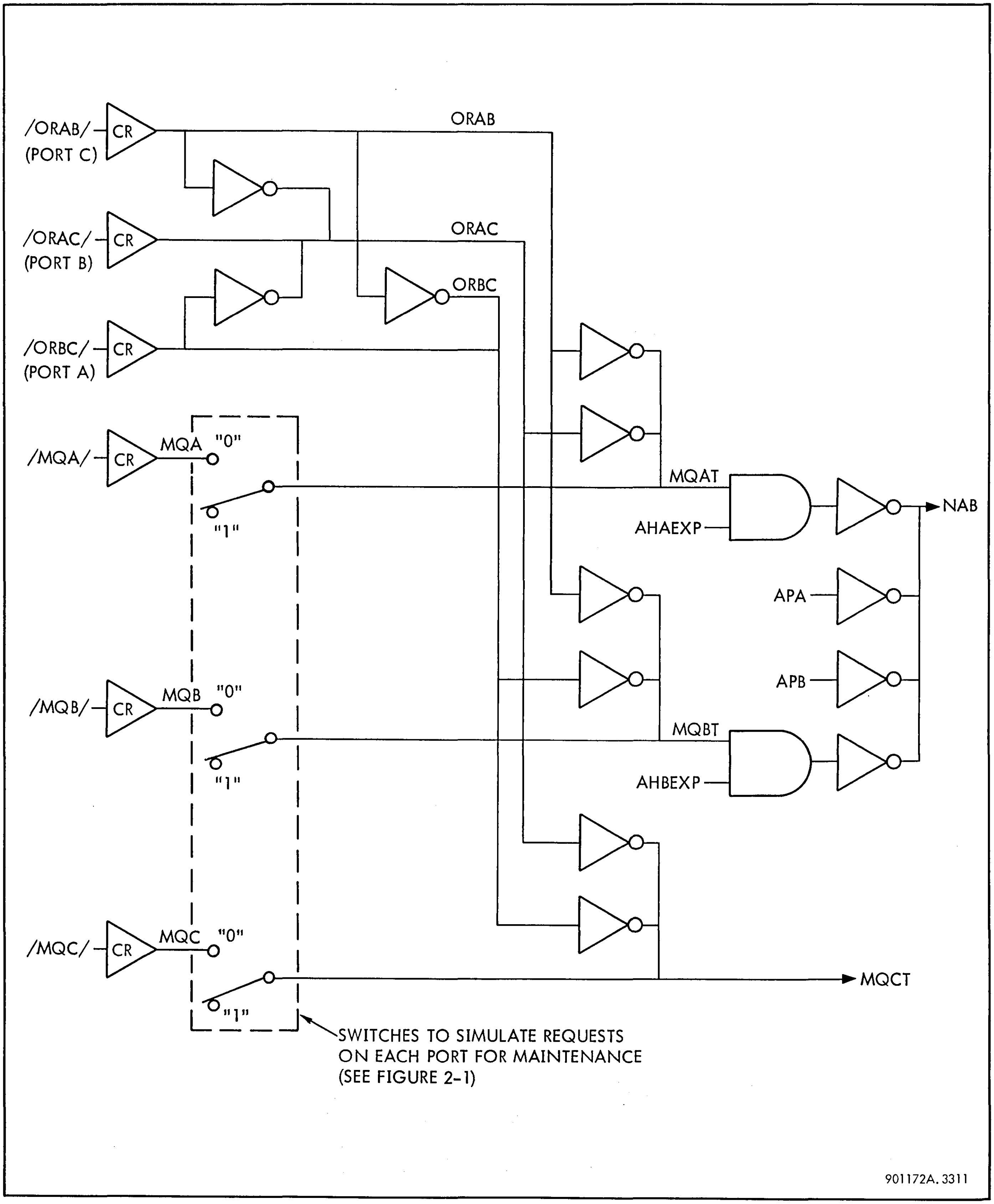

Figure 3-38. Memory Request and Port Override, Simplified Logic Diagram

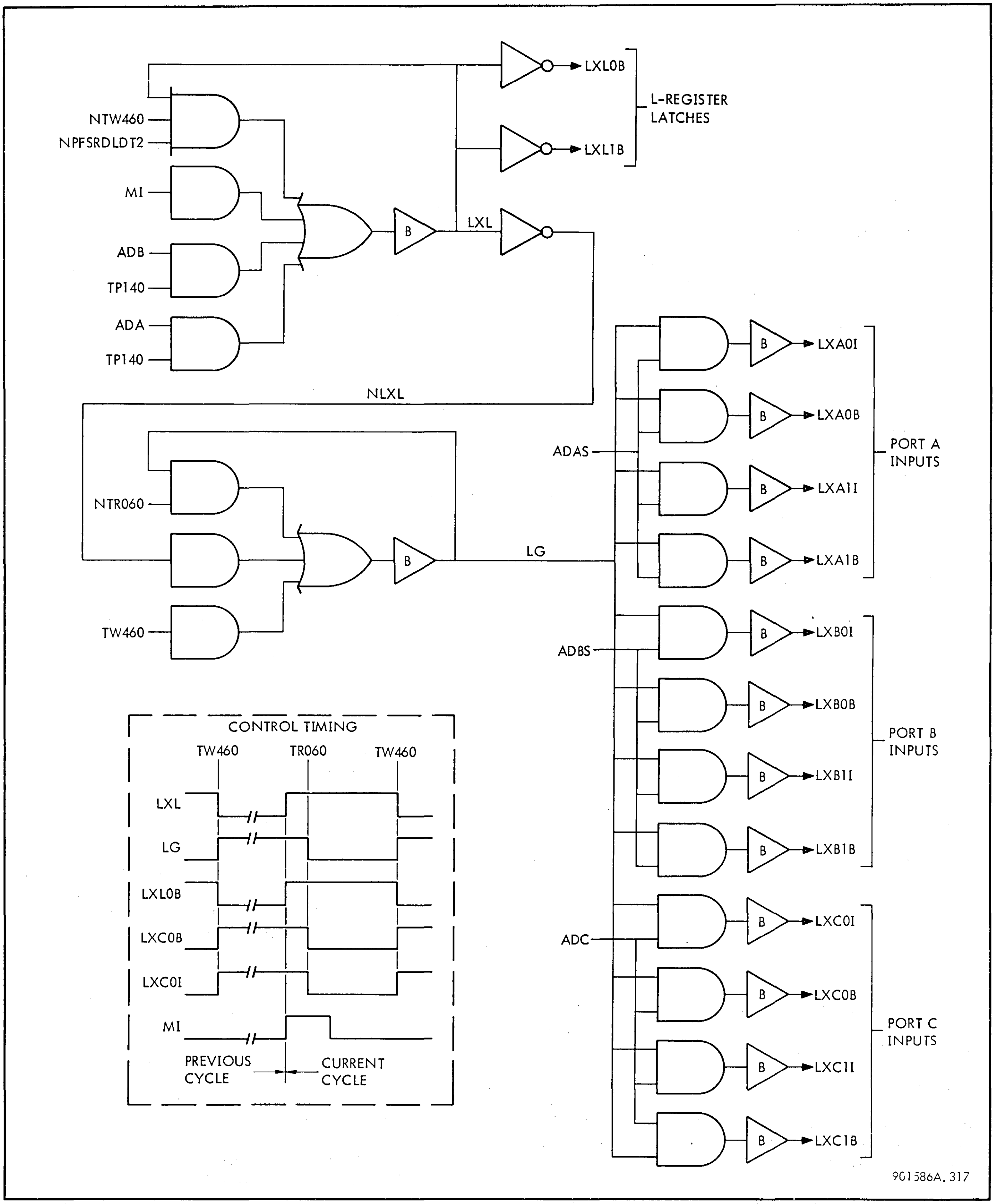

Figure 3-39. L-Register Control, Simplified Logic Diagram

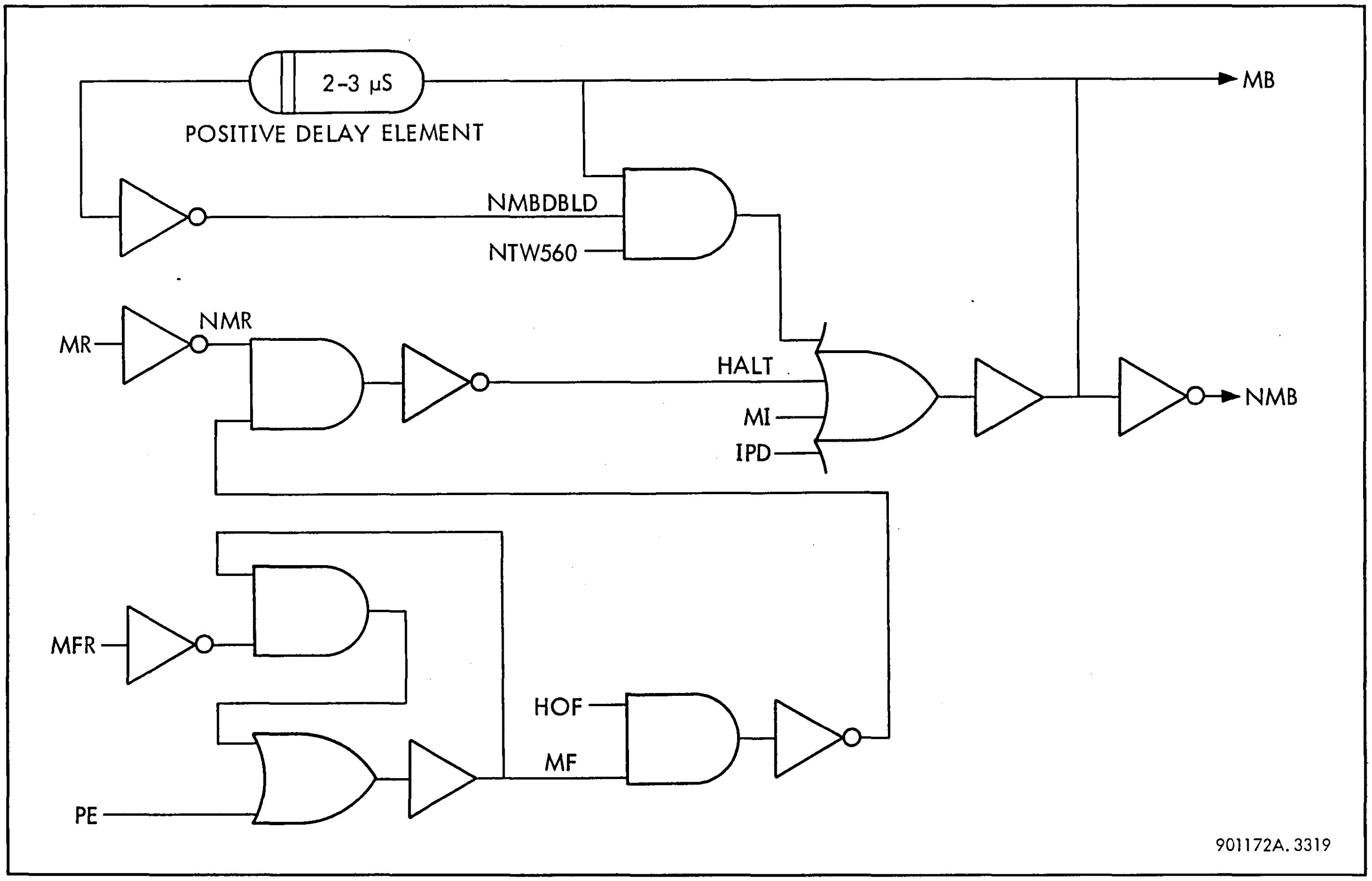

Figure 3-40. Memory Busy (MB), Simplified Logic Diagram

3-35 PORT EXPANDERS F AND S

Port expanders F and S both provide the same functions as either port A or port B in a memory bank. These functions are interleaving, address recognition, and input/output. Each port in a port expander has its own set of starting address switches (see figure 2-2), but no other switches in the bank are duplicated in the port expander. Therefore, to perform interleaving and address recognition, seven interleave transformation signals are brought over from the port in the bank to which the port expander is connected. Several other timing and control signals are taken from the corresponding port in the bank to accomplish the port functions. All of these signals are defined in paragraph 3-36, which follows. Since interleaving and address recognition are discussed in paragraphs 3-8 and 3-9, the subjects are not included in this description except to explain signal functions in the port expanders.

3-36 SIGNAL FLOW

Signal flow between each port in a port expander and the source to which the expander is connected is exactly the same as that between a memory port and its source.

Table 3-4 lists the cables and pin assignments for signals between the source and a port in a port expander. Table 3-5 lists the cables and pin assignments for signals between the port expander and either port A or port B. In addition to the 14 pins (table 3-4) equivalent to the 14 pins of the 33-ohm cables (table 3-5), seven pins in cable 4 and four pins in cable 5 are used by the ZT38 modules to transmit signals from the memory port to the port expander. These special signals are described as follows:

a. Interleave transformation signals. These include interleave size (signals NR08, NR16, NR32, and NR64), bank size (signals S0, S1), and 12K suppression [signal (12K)]. All are determined by the bank switches.

b. START. Signal START is generated in memory and is conveyed to the port expander when one of the following conditions exists:

1. The memory is not busy (NMB).

2. The port expander has gained an early access decision (CFA or CFB).

3. The current memory cycle is nearly complete (TW500), and, if the port expander is on port A, port B has not gained an early access decision or if the expander is on port B, there is no memory request on port A.

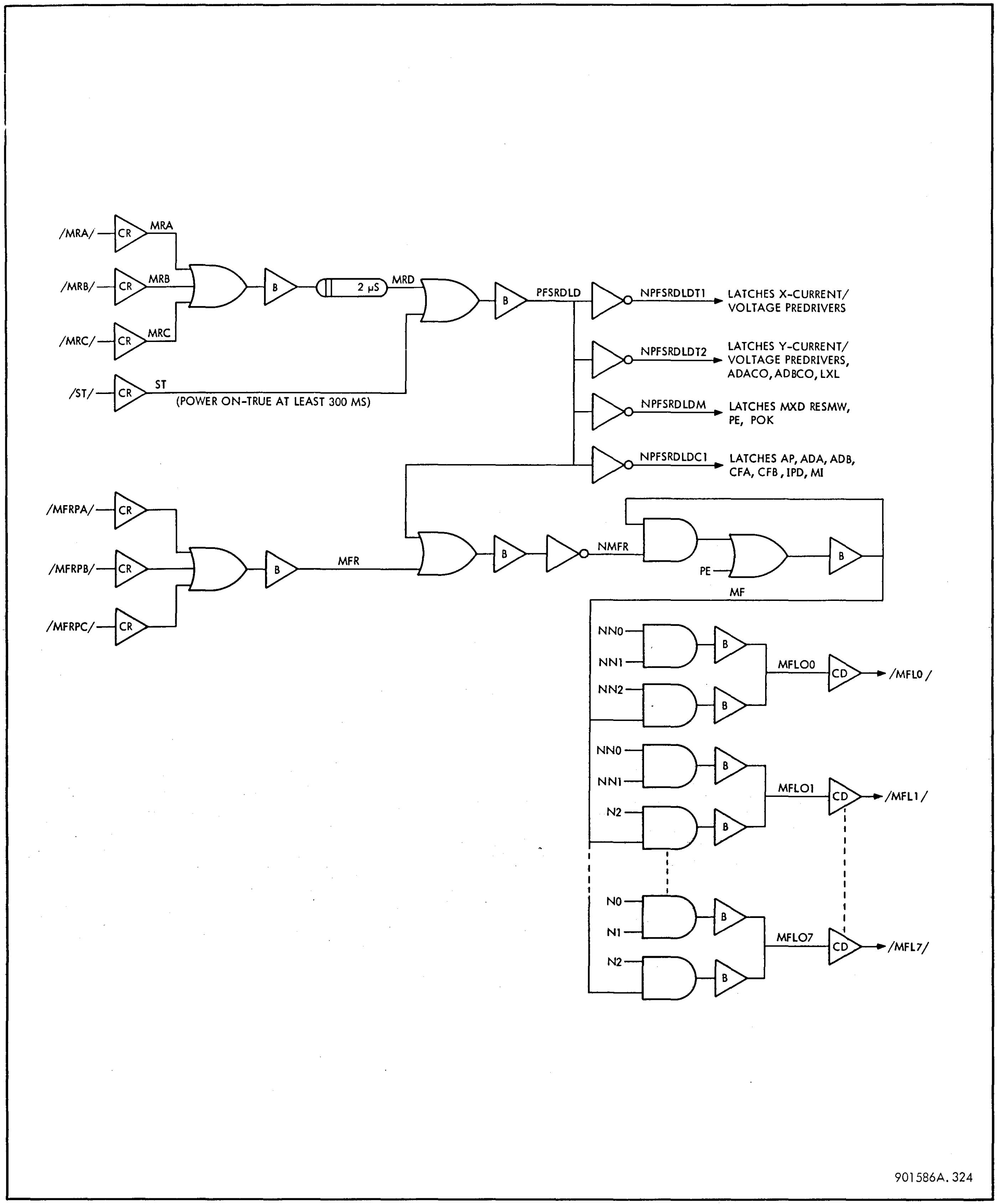

Figure 3-41. Memory Reset and Memory Fault, Simplified Logic Diagram

c. TW500. Derived from the 500-ns tap on the write delay line in memory. TW500 may be used in memory to generate START and is conveyed to the port expander to end data transmissions.

d. TO. Generated by memory at the beginning of a memory cycle. TO is conveyed to the port expander to generate address release and is used for phase control.

e. NPFSRD. In the port expander, this signal becomes NFRES and functions as a power monitor and reset signal to clear flip-flops.

Two signals not transmitted between the port expander and memory are L15, because it is only used in address recognition and not core selection, and AH, because each port in the expander generates its own address here signal to the source when an address is recognized.

3-37 PORT EXPANDER I/O FUNCTIONS

The port expander I/O functions are common to both port expander F and port expander S. Figure 3-42 shows a block diagram of the I/O functions for port 1 of port expander F. The remaining ports are connected in a similar way. The signals shown in the figure are defined in table 3-8. The standard signals shown are the address, data and control signals which are normally transferred between the source and a memory port.

3-38 Priority Logic

The priority logic selects one of the four ports for memory access. The port selection process begins when signal FPD is generated. FPD goes true when the START signal is received from the memory bank. This occurs only if there is coincidence of a memory request and an address here signal on at least one port. Figure 3-43 shows how signal FPD

Table 3-4. Port Expander to Source, Pin Assignments

Pin	Cable 1 AT11	Cable 2 AT11	Cable 3 AT11	Cable 4 AT10	Cable 5 AT11
02	M00 ←→	M14 ←→	M28 ←→	L15 →	MQ →
01	M01 ←→	M15 ←→	M29 ←→	L16 →	AH ←
04	M02 ←→	M16 ←→	M30 ←→	L17 →	AR ←
03	M03 ←→	M17 ←→	M31 →	L18 →	DR ←
05	M04 ←→	M18 ←→	L29 →	L19 →	PE ←
06	M05 ←→	M19 ←→	L30 →	L20 →	SRA →
07	M06 ←→	M20 ←→	L31 →	L21 →	
08	M07 ←→	M21 ←→	MW0 →	L22 →	ABO →
09	M08 ←→	M22 ←→	MW1 →	L23 →	POK ←
10	M09 ←→	M23 ←→	MW2 →	L24 →	MR →
11	M10 ←→	M24 ←→	MW3 →	L25 →	OR →
12	M11 ←→	M25 ←→	DG ←	L26 →	ORIL →
13	M12 ←→	M26 ←→	EDR ←	L27 →	HOF →
14	M13 ←→	M27 ←→		L28 →	MFR →

Legend

→ Inputs to port

← Outputs

←→ Two-way signal flow

serves the selection function. FPD enables the A-buffers (F1A through F4A) and also causes a narrow gating pulse, FPDG, to be generated. One or more ports may have both a memory request and an address here signal. For those ports, the corresponding A-buffers are set and latched. When FPDG goes false after 20 ns, any further access is blocked. At this point, the higher priority buffers turn off the lower priority buffers through the inverter network shown in the figure. Only the highest priority of the A-buffers which were initially set remains on. This is the selected port.

3-39 Gating

Gating is accomplished in the port expander in phase A and phase B. The function of phase A is to gate the address; the function of phase B is to gate the data. Phase A begins with a port selection decision and ends with address release, AR. Signal AR is the first signal released by memory after a memory cycle is in process. Phase B begins with TO from the memory and ends with TW500. Signal TW500 is derived from the 500-ns tap of the write delay line near the end of a memory cycle. Phase A and phase B overlap as shown in figure 3-44, which summarizes the port expander control. This overlap occurs between TO, the beginning of a memory cycle, and AR (60 ns later).

Phase A gates are driven directly from the access decision buffers through an intermediate level of buffering. They stay on during the entire selection phase of the memory and turn off with AR.

Table 3-5. Pin Assignments for Memory/Port Expander Cables

Pin	Cable 1 ZT38	Cable 2 ZT38	Cable 3 ZT38	Cable 4 ZT38	Cable 5 ZT38
02	M00 ←→	M14 ←→	M28 ←→		MQ →
01	M01 ←→	M15 ←→	M29 ←→	L16 →	
04	M02 ←→	M16 ←→	M30 ←→	L17 →	AR ←
03	M03 ←→	M17 ←→	M31 ←→	L18 →	DR ←
05	M04 ←→	M18 ←→	L29 →	L19 →	PE ←
06	M05 ←→	M19 ←→	L30 →	L20 →	SRA ←
07	M06 ←→	M20 ←→	L31 →	L21 →	
08	M07 ←→	M21 ←→	MW0 →	L22 →	ABO →
09	M08 ←→	M22 ←→	MW1 →	L23 →	POK ←
10	M09 ←→	M23 ←→	MW2 →	L24 →	MR →
11	M10 ←→	M24 ←→	MW3 →	L25 →	OR →
12	M11 ←→	M25 ←→	DG ←	L26 →	ORIL →
13	M12 ←→	M26 ←→	EDR ←	L27 →	HOF →
14	M13 ←→	M27 ←→		L28 →	MFR →
15				NR08 ←	START ←
16				NR16 ←	TW500 ←
17				NR32 ←	TO ←
18				NR64 ←	NPFSRD ←
19				NS1 ←	
20				NS0 ←	
21				(12K) ←	

Legend:

→ To memory

← From memory

←→ Two-way signal flow

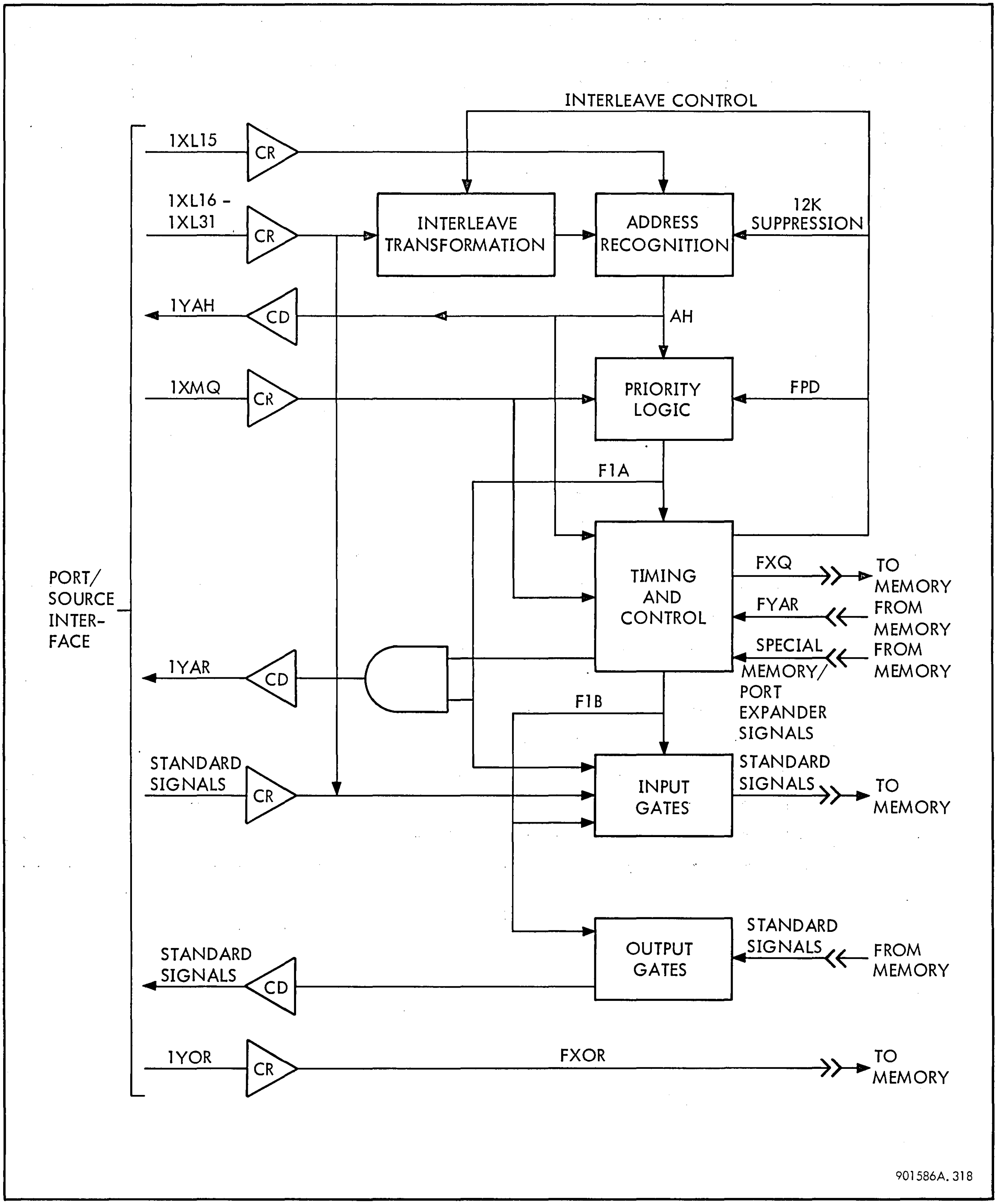

Figure 3-42. Input/Output Functions, Port Expander F, Port 1

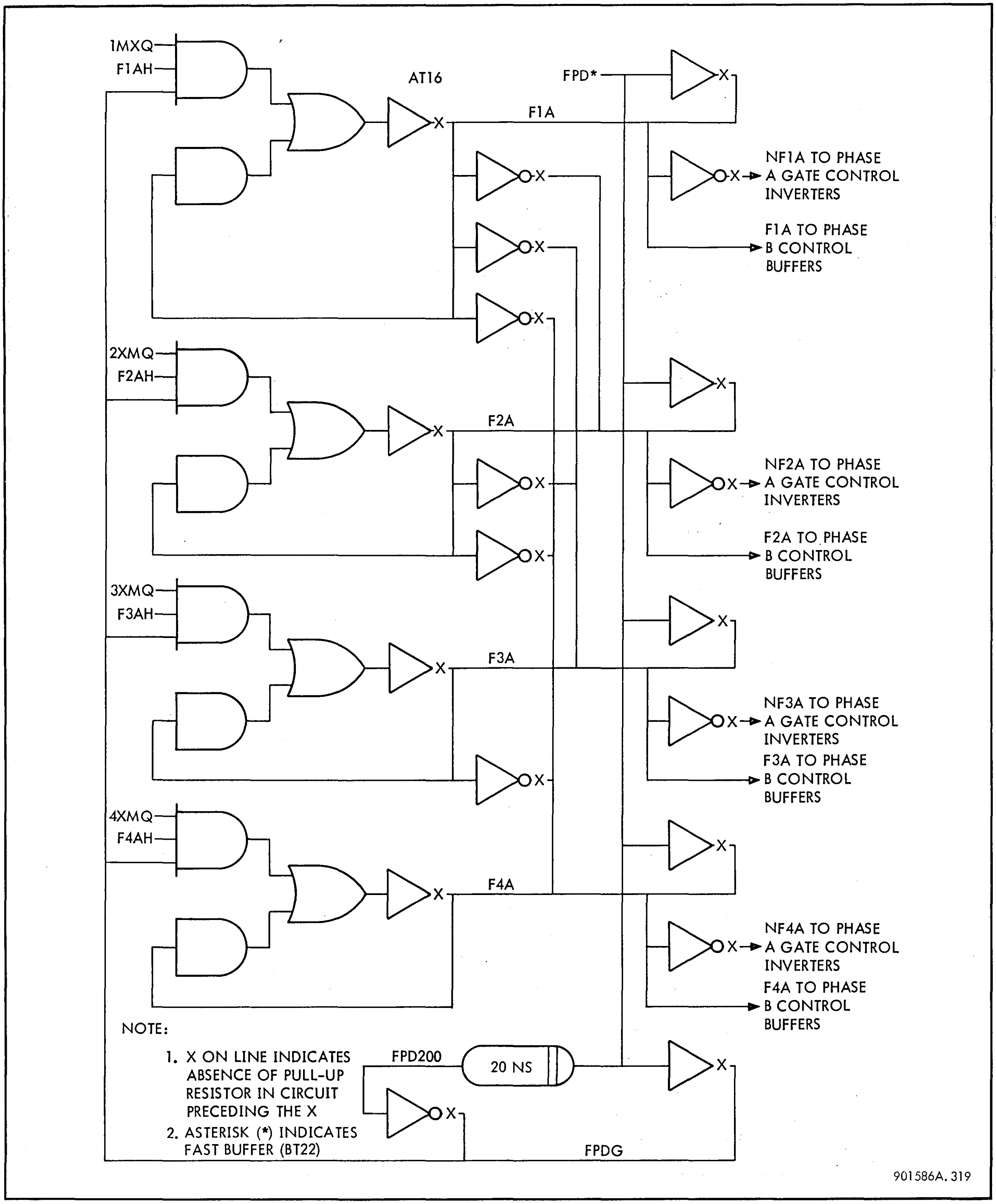

Figure 3-43. Priority and Port Selection, Simplified Logic Diagram

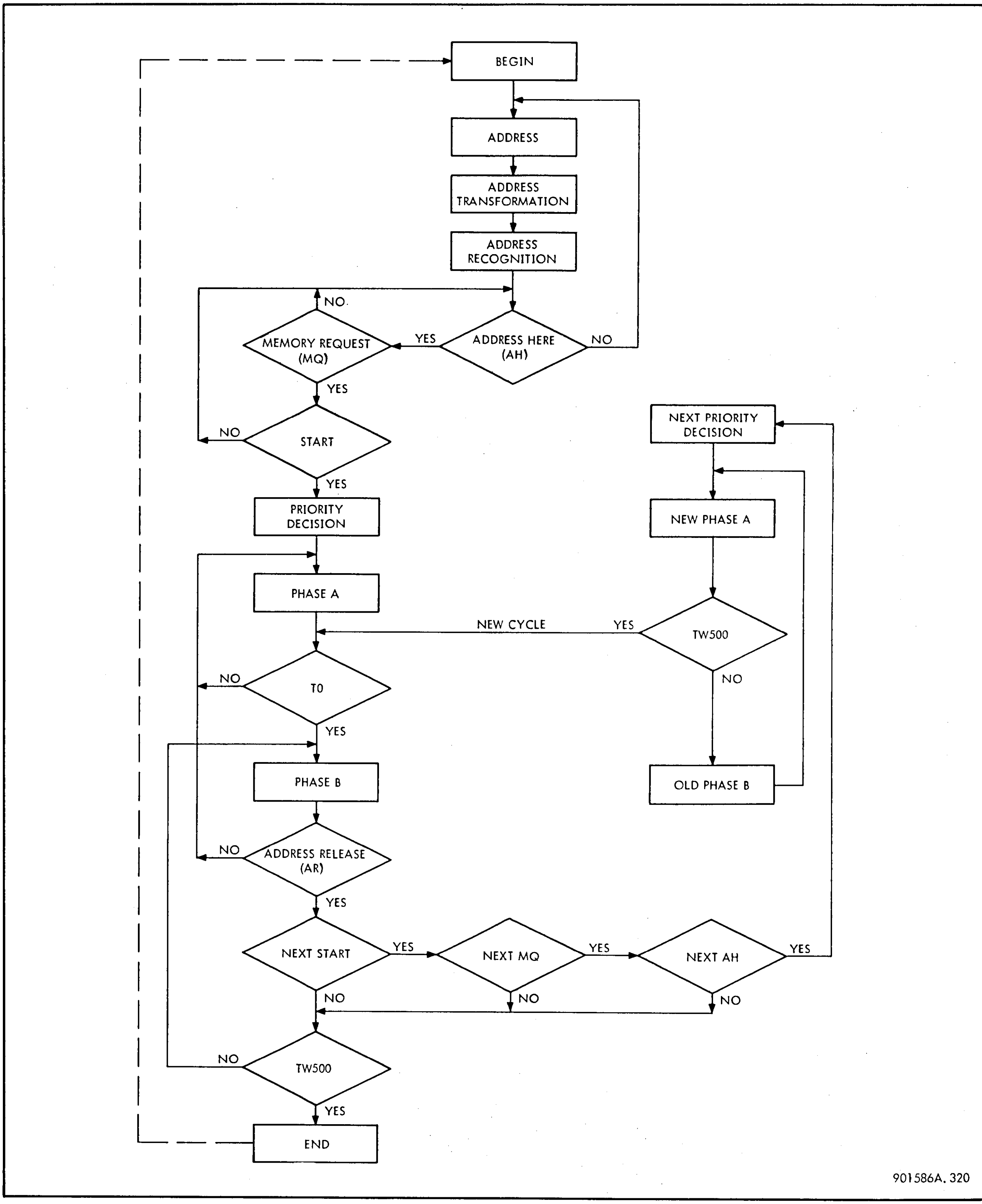

Figure 3-44. Port Expander Control, Flow Chart

In addition to the address signals, the write byte signals (MW0-MW3), abort (ABO), and address release (AR) are gated by phase A gates. The remainder of the inputs and outputs are gated by phase B, except the special signals from the memory detailed in paragraph 3-36 which are not gated by either phase.

If another request is present when phase A ends or if the same source sends a second request within 360 ns after AR, the port expander attempts to gain access through an early decision. If successful, phase A of the second request starts in the middle of phase B of the first request.

3-40 PORT EXPANDER SIGNAL NAMES

Signal names of the port expander are based on the memory signal names with prefixes added to identify a signal uniquely. The prefix of the name may consist of the first one or two characters; the base has an arbitrary length and, in general, is comparable to the memory signal of the same name. For example, a signal in port expander F has F for a prefix. The same signal may have a second prefix of X if the signal is input to the memory, or of Y, if the signal is output from memory. Some signals may have a suffix such as -1, -2, and so forth. These suffixes indicate equivalent signals which have been amplified by more than one buffer to increase fanout. N, used at the beginning of a signal, means inverse and is not part of the prefix. Table 3-6 lists the prefixes and table 3-7 lists the bases.

3-41 GLOSSARY OF INTERNAL MEMORY SIGNALS

The glossary of memory signals is listed in table 3-8. Only the internal signals of the memory are defined since the interface (input/output) signals are defined in paragraph 3-7.

Table 3-6. Port Expander Signal Prefixes

First Character	Definition	Second Character	Definition
1, 2, 3, 4	Port signals	1, 2, 3, 4	Port signals
		X	Input from memory
F	First port expander		
		Y	Output from memory
S	Second port expander		
		G	Ground
Z	Nonlogical signals (ground, voltage, and so on)	V	Voltage

Note

The second character is part of the base if it is not listed above

Table 3-7. Port Expander Signal Bases

Base	Definition	Base	Definition
(12K)	12K memory size	PD	Priority decision
(4K)	4K memory size	PD100D	PD delayed 100 ns
500	500 ns tap of write delay line in memory	PD20D	PD delayed 20 ns
		PE	Parity error
A	Phase A gate control	PEX	Port expander(s) is connected (as in SPEX)
ABO	Abort		
AH	Address here	PFSRD	Derived from PFSRDLD, power fail-safe and reset delayed
AR	Address release		
B	Phase B gate control	POK	Parity okay
		Q	Q signal (MQ AH)
B01	Module location B01 (as in ZGB01)		
		RES	Reset, derived from PFSRDLD
DG	Data gate		
		R08	8K interleave size
DR	Data release		
		S0	Bank size switch S0
EDR	Early data release		
		SRA	Second request allowed
L15	Address bit 15		
M00	Data bit 0	START	Start signal from memory
MQ	Memory request		
		T0	Time zero, derived from tap zero of read delay line
MW0	Write byte signal for byte 0		
		T15	Transformed address bit 15
N8	Negative 8 volts (as in ZNV8)		
		T16X31	Bit 31 into bit position 16 exchange control
OR	Override	TW500	Same as 500

Table 3-8. Glossary of Internal Memory Signals

Signal	Definition
00YNIP-32YNIP	Y-negative inhibit driver signals generated by the true condition of TNYI and the reset output of the respective M-register flip-flops
00YPIP-32YPIP	Y-positive inhibit driver signals generated by the true condition of TPYI and the reset output of the respective M-register flip-flops
3YNC0N-3YNC7N	Y-negative current predrive elements which decode bits L19, L20, and L21 of the address register
3YNV0N-3YNV7N	Y-negative voltage predrive elements which decode bits L18, L22, and L24 of the address register
3YPC0N-3YPC7N	Y-positive current predrive elements which decode bits L19, L20, and L21 of the address register
3YPV0N-3YPV7N	Y-positive voltage predrive elements which decode bits L18, L22, and L24 of the address register
(4K)	Signal is true when the memory size switches are in the configuration NS0 NS1. Signal is used in address and interleave logic
(12K)	Signal is true when the memory size switches are in the configuration S0 NS1. Signal is used in the address here and interleave logic
ABOA, ABOB, ABOC	Abort signals from the CPU to ports A, B, and C. Signals are used to override a write operation to prevent changing the contents of a protected memory location
ADA, ADB, ADC	Access decision signals used to indicate which port has priority for the current memory cycle
ADACO, ADBCO, ADCCO	Intermediate port logic signals used to gate various timing signals to the CPU and IOP
ADADG	Port A data gate enable signal
ADAM, ADBM, ADCMB, ADCMI	Signals derived from port priority logic and used to enable M-register transfer terms
ADAMW, ADBMW, ADCMW	Signals derived from port priority logic and used to enable byte presence indicators
ADAS, ADBS	Signals derived from port priority logic and used to enable L-register transfer terms
ADBDG	Port B data gate enable signal
ADCDG	Port C data gate enable signal
AHA, AHB, AHC	Address here signals as they appear in the internal memory logic. Signals are true when the requested address compares with the setting of the starting address switches for that particular memory bank (bits 15-19)
AP	Almost parity. Third level parity signal, true if bits M00 through M26 contain an odd number of ones

(Continued)

Table 3-8. Glossary of Internal Memory Signals (Cont.)

Signal	Definition
APA	Port A priority signal, which is true when AHA and MQA have been received and memory is not busy. Signal is used to trigger the port delay line causing IPD to go true
APB	Port B priority signal, which is true when AHB and MQB have been received and memory is not busy. Same function as APA
APE	Almost parity error. Fourth level parity signal, true if M00 through M32 contain even number of ones indicating that error has occurred
CFA, CFB	Port priority control signals for ports A and B. True when respective port has gained an early access decision
DG	Data gate enable signal used to enable data output gates for ports A, B, and C during a read-restore mode
DGA0-DGA7	Port A data output gates. Signals gate output of M-register onto data lines for port A during a read-restore mode
DGB0-DGB7	Port B data output gates. Same function as DGA0-DGA7
DGC0-DGC7	Port C data output gates. Same function as DGA0-DGA7
HALT	A signal generated whenever the following conditions exist: Either the power fail-safe and reset (PFSR) are true or halt on fault (HOF) and memory fault (MF), AND-gated, are both true. The HALT signal is used to cause memory busy (MB) to stay true and to ignore any further memory requests
HOF	Halt on fault signal generated by the CPU when parity error mode switch on PCP is in HALT position
IPD	Initiate port delay signal used to trigger the port delay lines for access decision when port A and port B have memory requests
L18-L31	L-register outputs, used for X and Y core drive selection. Bits 15-17 do not go into the L-register. Instead, they are used for address recognition to select one of eight possible memory banks
L18SEN, L19SEN	Duplicate logic of L18 and L19 used to drive the preamplifier selection signals PASL0-PASL7 where they appear as L18J and L19J
LA15-LA31	Port A address signals as they appear at the input to port A after the port A cable receivers. LA20-LA29 are direct inputs to the L-register
LA16S-LA19S	Port A memory selection signals. After interleave transformation by LA30 and LA31, they are compared with starting address switch logic
LA18L-LA19L	L-register inputs after address modification
LA30L, LA31L	L-register inputs after address manipulation
LB15-LB31	Port B address signals. Same function as LA15-LA31
LB16S-LB19S	Port B memory selection signals. Same function as LA16S-LA19S

(Continued)

Table 3-8. Glossary of Internal Memory Signals (Cont.)

Signal	Definition
LB18L, LB19L	Port B special address signals. Same function as LA18L and LA19L
LB30L, LB31L	Port B memory selection signals. Same function as LA30L and LA31L
LC15-LC31	Port C address signals. Same function as LA15-LA31
LC16S-LC19S	Port C memory selection signals. Same function as LA16S-LA19S
LC18L, LC19L	Port C special address signals. Same function as LA18L and LA19L
LC30L, LC31L	Port C memory selection signals. Same function as LA30L and LA31L
LXA --	Port A transfer signals for address lines into the L-register
LXB --	Port B transfer signals for address lines into the L-register
LXC --	Port C transfer signals for address lines into the L-register
LXL	Source of clear and latch signals for the L-register
LXL --	L-register latch signals generated by LXL
M00-M31	M-register flip-flops. The flip-flops accept data inputs from ports A, B, and C or from core memory discriminator outputs. Each complete memory bank (4, 8, 12, or 16K) has its own M-register
M32	Parity flip-flop. Flip-flop M32 is set during a read-restore or partial write operation if the word from memory contains an even number of ones. Flip-flop M32 is set during a partial or full write if the data to be strobed into core memory has an even number of ones
M32XP	Parity flip-flop transfer signal used to set flip-flop M32 during parity generation (partial or full write)
MA00-MA31	Port A data lines. Inputs to the M-register
MB	Memory busy signal which is true during the time that memory is in the process of satisfying a memory request. The MB signal is also kept true during a memory halt condition to prevent any new memory requests from being honored
MB00-MB31	Port B data lines. Inputs to the M-register
MC00-MC31	Port C data lines. Inputs to the M-register
MD00P-MD31P	Sense amplifier-discriminator outputs from core memory. Inputs to the M-register
MD32P	Sense amplifier-discriminator output from parity bit in core memory. Input to parity flip-flop
MF	Memory fault signal used to gate MFL00-MFL07 memory fault signals
MFR	Memory fault reset signal which is generated by the CPU and is used to reset MF

(Continued)

Table 3-8. Glossary of Internal Memory Signals (Cont.)

Signal	Definition
MI	Memory initiate signal used to begin a memory cycle when both the address here and memory request signals are true
MQA, MQB, MQC	Memory request signals from external units as they appear in the memory logic
MR	Memory reset signal from the CPU (where it appears as MRS) which resets control elements in core memory. Do not confuse this signal with the MR signaled by the CPU as a memory request
MW0-MW3	Byte presence indicator flip-flops used to determine which memory operation is to take place. If all flip-flops are reset, a read-restore operation occurs. If all flip-flops are set, a full write operation occurs. If neither of these conditions exist, a partial write operation occurs
MW0A-MW3A	Write-byte signals to port A from an external unit. Used to set the byte presence indicator flip-flops
MW0B-MW3B	Write-byte signals to port B from an external unit. Used to set the byte presence indicator flip-flops
MW0C-MW3C	Write-byte signals to port C from an external unit. Used to set the byte presence indicator flip-flops
MXA0-MXA3	Port A transfer signals between the M-register set input and the port A data lines
MXB0-MXB3	Port B transfer signals between the M-register set input and the port B data lines
MXC0B-MXC3B	Port C transfer signals between the M-register set input and the port C data lines
MXC0I-MXC3I	Port C transfer signals between the M-register reset input and the port C data lines
MXD0B-MXD3B	Core memory discriminator transfer signals between the M-register set input and the discriminator outputs
MXD0I-MXD3I	Core memory discriminator transfer signals between the M-register reset input and the discriminator outputs
MXM0-MXM3	M-register clear and latch signals
MXM32	Parity flip-flop clear and latch signal
N0, N1, N2	Memory number switches used to control the MEMORY FAULT lamps on the processor control panel
NIL	Interleave logic. True if interleaving is not established
NTSSTB	Not time for sense strobe signal. When false, this signal causes the strobe signals, SAST0-SAST3, to go false and to strobe the preamplifier outputs into the sense amplifiers
ORIL	Override interleave signal. Generated by the processor control panel and used to disable interleaving

(Continued)

Table 3-8. Glossary of Internal Memory Signals (Cont.)

Signal	Definition
ORSP	Override slow port signal. Generated by the CPU to cause port C to have the highest priority. Locks out ports A and B even though the CPU may not have a memory request pending
PASL0-PASL7	Sense preamplifier selection signals which enable the proper preamplifiers by decoding address bits L18, L19, and L23
PE	Parity error signal which is true if a parity error is detected during a read-restore or a partial write operation. The signal is also called a fifth level parity signal
PF00-PF30	Parity first level gates
PFSR	Power fail-safe and reset signal which can go true as a result of receiving MR from the CPU, or ST from the power fail-safe circuits. Signal is used to reset MF
POK	Parity okay flip-flop. Used to signal external unit that parity check was satisfactory on word just received from memory
PORTDL	Port delay line triggered by IPD, which generates TP000 through TP100 in 20-ns steps. Signal is generated whenever port A or B receives a memory request, unless CFA or CFB is active
PORTDL2	Port delay line triggered by TP100, which generates TP120 through TP200 in 20-ns steps
PS00-PS27	Parity second level gates
RD	Read signal generated whenever all four byte lines are false
READDL	Read delay line which is triggered by MI to generate TR000 through TR600 in 20-ns steps. Signal is used to control read portion of a memory cycle
RESMW	Latch signal for byte presence indicator flip-flops, MW0-MW3
S0, S1	Memory size switches used to establish size of memory module
S8	Interleave switch, true for 8K
S16	Interleave switch, true for 16K
S32	Interleave switch, true for 32K
S64	Interleave switch, true for 64K
SAST0-SAST3	Sense amplifier strobe signals
SPA00P-SPA07P SPA00N-SPA07N	Sense preamplifier outputs for byte 0
SPA08P-SPA15P SPA08N-SPA15N	Sense preamplifier outputs for byte 1
SPA16P-SPA23P SPA16N-SPA23N	Sense preamplifier outputs for byte 2

(Continued)

Table 3-8. Glossary of Internal Memory Signals (Cont.)

Signal	Definition
SPA24P-SPA32P SPA24N-SPA32N	Sense preamplifier outputs for byte 3
ST	Start signal generated by the power-on circuit, which is true for at least 300 ms. True also during power-off
TNXC	Time for negative X-current. Signal is true during the read portion of a memory cycle if L22 ≠ L25. Signal is true during the write portion of a memory cycle if L22 = L25. Signal is used to enable selected X-negative voltage predrive switches
TNXV	Time for negative X-voltage. Signal is true during the read portion of a memory cycle if L22 = L25. Signal is true during the write portion of a memory cycle if L22 ≠ L25. Signal is used to enable selected X-negative voltage predrive switches
TNYC	Time for negative Y-current. Signal is true during the read portion of a memory cycle if the sum of L22, L23, and L25 is odd. Signal is true during the write portion of a memory cycle if the sum is even. Signal is used to enable selected Y-negative current predrive switches
TNYI	Time for negative Y-inhibit. Signal is true during the write portion of a memory cycle if the sum of L22, L23, and L25 is even. Signal is used to short-circuit those Y-current switches where a zero is to be generated in core memory
TNY10-TNY13	Amplified versions of TNYI; byte-oriented
TNYV	Time for negative Y-voltage. Signal is true during the read portion of a memory cycle if the sum of L22, L23, and L25 is even. Signal is true during the write portion of a memory cycle if the sum is odd
TP000-TP100	Output signals from PORTDL delay line. Used to control priority decision logic
TP120-TP200	Output signals from PORTDL2 delay line. Used to control priority decision logic
TPXC	Time for positive X-current. Signal is true during the read portion of a memory cycle if L22 = L25. Signal is true during the write portion of a memory cycle if L22 ≠ L25
TPXV	Time for positive X-voltage. Signal is true during the read portion of a memory cycle if L22 ≠ L25. Signal is true during the write portion of a memory cycle if L22 = L25
TPYC	Time for positive Y-current. Signal is true during the read portion of a memory cycle if the sum of L22, L23, and L25 is even. Signal is true during the write portion of a memory cycle if the sum is odd
TPYI	Time for positive Y-inhibit. Signal is true during the write portion of a memory cycle if the sum of L22, L23, and L25 is odd
TPY10-TPY13	Amplified version of TPYI; byte-oriented

(Continued)

Table 3-8. Glossary of Internal Memory Signals (Cont.)

Signal	Definition
TPYV	Time for positive Y-voltage. Signal is true during the read portion of a memory cycle if the sum of L22, L23, and L25 is odd. Signal is true during the write portion of a memory cycle if the sum is even
TR000-TR600	Output signals from READDL delay line. Used to control read portion of a memory cycle
TW000-TW580	Output signals from WRITEDL delay line. Used to control write portion of a memory cycle
WF	Write full signal which is true whenever all the byte presence indicator flip-flops are set
WP	Write partial signal, which is true whenever some (but not all) of the byte presence indicator flip-flops are set
WRITEDL	Write delay line which is triggered by TR160 during a read-restore or a full write operation and by TR560 during a write partial operation. Signal is used to control the write portion of a memory cycle
X, NX	Current direction control signals for the X selection. X is true when L22 = L25. NX is true when L22 ≠ L25
X8	Interleave logic: interleave size is 8K
X161, X162	Interleave logic: interleave size is 16K
X32	Interleave logic: interleave size is 32K
X641, X642	Interleave logic: interleave size is 64K
XNCD0-XNCD3	X-negative current predrive elements which decode L19 and L25
XNCK0-XNCK3	X-negative current predrive elements which decode L26 and L27. XNCD0-XNCD3 and NXCK0-NXCK3 form a matrix for the X-negative current predrive system
XNVD0-XNVD7	X-negative voltage predrive elements which decode L18, L28 and L29
XNVK0-XNVK3	X-negative voltage predrive elements which decode L30 and L31. XNVD0-XNVD7 and XNVK0-NXVK3 form a matrix for the X-negative voltage predrive system
XPCD0-XPCD3	X-positive current predrive elements which decode L19 and L25
XPCK0-XPCK3	X-positive current predrive elements which decode L26 and L27. XPCD0-XPCD3 and XPCK0-XPCK3 form a matrix for the X-positive current predrive system
XPVD0-XPVD7	X-positive voltage predrive elements which decode L18, L28, and L29
XPVK0-XPVK3	X-positive voltage predrive elements which decode L30 and L31. XPVD0-XPVD7 and XPVK0-XPVK3 form a matrix for the X-positive voltage predrive system
Y, NY	Current direction control signals for the Y selection. Y is true if the sum of L22, L23, and L25 is even. NY is true if the sum is odd

SECTION IV
MAINTENANCE

4-1 INTRODUCTION

This section provides information for preventive and corrective maintenance. Refer to ESM publication No. 902308 for automated equations, pin lists, and other engineering documentation and to appendix A for a parts list of all applicable parts.

4-2 PREVENTIVE MAINTENANCE

Preventive maintenance of the Sigma 5 or 7 memory consists of visual inspection, cleaning, and running diagnostic programs. Because there are no mechanical components, lubrication and mechanical adjustments are not required.

4-3 VISUAL INSPECTION

The interior of cabinets must be free of wire cuttings, dust, and other foreign matter. No clip leads or push-on jumpers should be connected to any back panel pins. All cables should be dressed with cable clamps. All chassis and frames must be properly bolted down and all hardware in place.

4-4 CLEANING

External and internal surfaces of the memory cabinet must be kept clean and free of dust. Tops of cabinets must be cleared of all materials so that fan assemblies are able to expel the air for proper cooling.

The air filters (XDS part No. 117427) should be checked periodically for cleanliness. They should be washed with warm water and detergent.

4-5 DIAGNOSTIC TESTING

The two diagnostic programs which apply to Sigma 5 and 7 memories are the Sigma 5 and 7 Memory Diagnostic (MEDIC 75) and the Sigma 5 and 7 Memory Interleaving Test (MIT). They are discussed in paragraphs 4-6 and 4-7, respectively.

4-6 SIGMA 5 AND 7 MEMORY DIAGNOSTIC (MEDIC 75)

This diagnostic program consists of an executive routine and 14 individual memory tests which are designed to perform 14 discrete tests. Error type-outs and several operator-controlled options are available for test selection, address range selection, data checking discrimination and looping on individual tests. This program cannot be used for memories smaller than 8K.

Document	Description
XDS publication No. 900825	Diagnostic program manual, with listing
Program No. 704067-83	Diagnostic program on absolute binary paper tape
Program No. 704067-84	Diagnostic program on absolute binary cards

4-7 SIGMA 5 AND 7 MEMORY INTERLEAVING TEST (MIT)

This diagnostic program verifies the successful operation of memory interleaving in two discrete sections. The first section is a memory addressing test. The second section attempts to access between interleaved memories at the fastest programmable rate. MIT is meant to supplement MEDIC 75 and is not a substitute. MIT should not be run unless MEDIC 75 is successful.

Document	Description
XDS publication No. 901071	Diagnostic program manual, with listing
Program No. 704121-83	Diagnostic program on absolute binary paper tape
Program No. 704121-84	Diagnostic program on absolute binary cards

Diagnostic testing should be performed with normal, +10 percent, and -10 percent PT16 power supply voltage margins.

4-8 CORRECTIVE MAINTENANCE

The following corrective maintenance procedures have been found useful. The order in which they appear does not imply a sequence to be followed in troubleshooting.

4-9 PORT AND CONTROL TIMING LOGIC VERIFICATION

The following verification procedures are useful in determining if the port priority and control logic is functioning satisfactorily.

Perform a read or load word operation. Using positive scope sync, monitor TR000 (23C30) with probe A and use probe B to check the points listed below. See figure 2-1 for switch locations. Timing measurements are made at the 50 percent amplitude points of the waveshapes.

LXL (21D35). LXL should reset to ground at TW500 or approximately 700 ns after TR000.

LG (07D07). LG, with reference to TR000, should go to ground in approximately 50 ns and to +4V in 700 ns.

MB (25D07). MB should reset at TW560 or approximately 800 ns after TR000.

CFA (29C07), CFB (29C21)

a. Set switches 1 (AHBEXP), 2 (AHAEXP), and 3 (MQAT) on module 20C to 1. CFA should set to +4V at TW320 or 500 ns after TR000 and reset to ground at TR000.

b. On module 20C, set switch 3 (MWAT) to 0 and switch 4 (MWBT) to 1. CFB should set to +4V at TW320 or 500 ns after TR000 and reset to ground at TR000.

CFA + CFB (24D01). This signal should be equal to CFB. After setting switch 3 (MWAT) on module 20C to 1, the signal should be equal to CFA.

ADA (26D07), ADB (26D21).

a. ADA should reset to ground at TW360 or 565 ns after TR000.

b. On module 20C set switch 3 (MQAT) to 0. ADB should reset to ground at TW360, or 565 ns after TR000. Reset switches 1, 2, 3, and 4 on module 20C to 0.

TW000 (23C29), TW600DL. TW000 should be 80 ns wide minimum. TW600DL (27C11) should go from -4V to +2V minimum and should be 80 ns wide at the 50 percent level.

ADCCO (07D01). During port C access, ADCCO should go to +4V 60 ns after TR000 and should reset to ground at the trailing edge of MB or 850 ns after TR000.

SDECEN (29D06). This signal is transmitted on twisted wire. It should go to ground 20 ns before TR000 and to +4V 60 ns after TR000.

MI (28D2). Turn off PT17 power supply. Monitor MI and remove module 20C. Memory should cycle at a rate of approximately 850 ns. Press the SYSTEM RESET switch several times. The memory cycle time should remain the same. Replace module 20C. Turn on PT17 power supply.

PG (25C30). PG should be a positive going pulse, 60 ns wide and should occur 500 ns after TR000.

DG-1 (26B01), DG-2 (27B01). DG-1 and DG-2 should go positive 250 ns after TR000 and should go negative 480 ns after TR000.

TR500-1 (25C17), TR500-2 (25C05). Both pulses should be 100-ns wide and should occur 520 ns after TR000.

MXM32 (18B04).

a. Perform a write or store word operation. MXM32 should be two negative going pulses 100 ns wide. The first pulse occurs 30 ns after TR000 and the second pulse occurs 250 ns after TR000.

b. Perform a partial write or a store byte operation. MXM32 should be two negative going pulses 100 ns wide. The first occurs 30 ns after TR000 and the second occurs 600 ns after TR000.

4-10 SIGMA 5 AND 7 MEMORY CATASTROPHIC FAILURE DIAGNOSTIC

This diagnostic tests for single component failures occurring in the sense, drive and predrive systems. Open diodes in core diode modules are also diagnosed. Diagnosis is to the module level. For certain failures, it is possible only to isolate the failure to two modules. Module failures diagnosed include:

a. Y-predrivers (ST22)

b. Y-drivers (ST11)

c. X-predrivers (ST22)

d. X-drivers (ST10)

e. Sense preamplifier (HT26)

f. Sense amplifiers/discriminators (HT11)

g. Preamplifier select terms (ST15)

h. Inhibit drivers (ST21)

i. Core diode modules (111549, 111550)

j. L-register and control terms

k. M-register and control terms

l. Miscellaneous control terms

4-11 Procedures and Methods Used for Fault Isolation

The procedures consist of five diagnostic routines:

a. Ones Discrimination (DATA)

b. Zeros Discrimination (DATA)

c. Addressing

d. Ones Discrimination (PARITY)

e. Zeros Discrimination (PARITY)

The tests are run in sequence until a failure occurs. The failures are then analyzed and the problems are diagnosed. Each of the five diagnostic programs resides in the general registers. Failures confined to the parity bit are neither detected nor diagnosed. If these five tests run successfully or if failures are confined to the parity bit, then they may be diagnosed using the Sigma 5 and 7 Memory ($\geq$8K) Test (MEDIC 75), XDS publication No. 900825. All programs have been written to test a 16K bank. If a smaller bank is to be tested, the upper address limit must be changed in routines 1 and 2. Routines 3, 4, and 5 require several changes to be used in smaller banks.

4-12 GENERATION OF ADMASK (EXAMPLE). Consider a hypothetical memory having 16 locations. Addresses are expressed in binary. Each address followed by an X is a failing address. Shown below is a step-by-step description of the use of ONAC and ZACC. Registers ONAC and ZACC are not altered unless an error is detected. When an error is detected, the current address is logically AND-gated with ONAC and inclusive OR-gated with ZACC to create a value called ADMASK. The ADMASK value is a key used to locate a particular fault isolation table.

	Current Address	ONAC	ZACC	Failure	Last Failing Address
Initial Setting	0000	1111	0000		0000
0	0000	1111	0000		0000
1	0001	0001	0001	X	0001
2	0010	0001	0001		0001
3	0011	0001	0011	X	0011
4	0100	0001	0011		0011
5	0101	0001	0011		0011
6	0110	0001	0011		0011
7	0111	0001	0011		0011
8	1000	0001	0011		0011
9	1001	0001	1011	X	1001
10	1010	0001	1011		1001
11	1011	0001	1011	X	1011
12	1100	0001	1011		1011
13	1101	0001	1011		1011
14	1110	0001	1011		1011
15	1111	0001	1011		1011
Bit No.	0123				

Every one bit in ADMASK indicates an address bit which remains constant for all failures. Hence the bit is important in diagnosing the failure. In this example, a failure occurs any time address bit 1 is zero and address bit 3 is one. As a result, bit 1 and bit 3 of ADMASK are ones.

$$\text{ADMASK} = \text{ONAC} + \overline{\text{ZACC}} \quad \text{Composition of ADMASK}$$

$$\left.\begin{aligned} \text{ONAC} &= 0001 \\ \text{ZACC} &= 1011 \\ \overline{\text{ZACC}} &= 0100 \end{aligned}\right\} \text{Generation of ADMASK}$$

$$\text{ADMASK} = 0101$$

4-13 DESCRIPTION OF FAULT ISOLATION ROUTINES. The following tests are run to aid in fault isolation:

a. Routine 1 - ONES DISCRIMINATION (DATA)

1. Load the following program into the general registers. If loading is by means of a self-loading binary card, verify the contents of the general registers before running the program. Many memory errors do not result in parity errors.

Note

All addresses and contents are in hexadecimal.

	Location	Contents	Mnemonic	Description
	0	B5F0000E	STW, R15	Try one address
	1	B1F0000E	CW, R15	
	2	68300007	BCR, 3	Gather failure address data
	3	4BD0000E	AND, R13	
	4	49C0000E	OR, R12	
	5	32B0000E	LW, R11	
	6	20A00001	AI, R10	
	7	20E00001	AI, R14	Update address
	8	21E04000	CI, R14	Check for upper limit
	9	69300000	BCS, 3	Try again if not upper limit
10	A	2E000000	WAIT	Failure count in HW1
11	B	00000000	DATA	Last failing address
12	C	00000000	DATA	ZACC (zero-bit accumulator)
13	D	00003FFF	DATA	ONAC (one-bit accumulator)
14	E	00000010	DATA	Current address. Initial value is lower limit
15	F	FFFFFFFF	DATA	Pattern

2. Clear PSW1 and PSW2.

3. Display instruction address.

4. Place the COMPUTE switch in RUN.

5. When the computer comes to a WAIT, the display register contains the content of X'B', the last failing address. If the last failing address is zero, then no failures have been detected. If no failures have been detected, proceed with routine 2.

6. Read and record the following:

a. The content of X'A' (failure count)

b. The content of X'B' (last failing address)

c. The content of X'C' (ZACC)

d. The content of X'D' (ONAC)

e. The content of the location whose address is contained in X'B'.

7. Take the one's complement of the contents of X'C'. Gate the result in an inclusive OR operation with the content of X'D'. Take bits 18-31 of the result; express as a four digit hexadecimal number. Call the result ADMASK.

$$\text{ADMASK} = \text{ONAC} + \overline{\text{ZACC}}$$

8. Look at the contents of the last failing address (obtained in step 6e) to determine the category of the failures.

Description	Category
All bits dropped	1
One byte dropped	2
One half-byte dropped	3
One bit dropped	4

9. Use the combination of ADMASK and the category number in table 4-1 to select the applicable paragraph. Go to the paragraph selected to diagnose the failure.

Table 4-1. Fault Diagnosis, Ones Discrimination

ADMASK	CATEGORY			
	1	2	3	4
0000	par. 4-25	par. 4-24	par. 4-20	par. 4-21
0003	par. 4-15			
0030	par. 4-15			
1040	par. 4-15			

Table 4-1. Fault Diagnosis, Ones Discrimination (Cont.)

ADMASK	CATEGORY			
	1	2	3	4
1070		par. 4-16		
1C00	par. 4-17			par. 4-18
200C	par. 4-15			
200F		par. 4-16		
2280	par. 4-17			par. 4-18
307F		par. 4-22		
3100	*			par. 4-19
3E80				par. 4-23

*Replace preamplifier module 16J

In the event no paragraph is applicable, suspect a multiple or other unusual failure.

b. Routine 2 – ZEROS DISCRIMINATION (DATA)

1. Load the following program into the general registers. If loading is by means of the self loading binary card, verify the content of the general registers before the program is run.

Note

All addresses and contents are in hexadecimal.

Location	Contents	Mnemonics	Description
0	B5F0000E	STW, R15	Try one address
1	B1F0000E	CW, R15	
2	68300007	BCR, 3	
3	4BD0000E	AND, R13	
4	49C0000E	OR, R12	Gather failure address data
5	32B0000E	LW, R11	
6	20A00001	AI, R10	
7	20E00001	AI, R14	Update address
8	21E04000	CI, R14	Check for upper limit
9	69300000	BCS, 3	Try again if not upper limit
A	2E000000	WAIT	Failure count in HW1
B	00000000	DATA	Last failing address
C	00000000	DATA	ZACC (zero-bit accumulator)

Location	Contents	Mnemonics	Description
D	00003FFF	DATA	ONAC (one-bit accumulator)
E	00000010	DATA	Current address. Initial value is lower limit
F	00000000	DATA	Pattern

2. Clear PSW1 and PSW2.

3. Display instruction address.

4. Place the COMPUTE switch in RUN.

5. When the computer comes to a WAIT, the display register contains the contents of X'B', the last failing address. If the last failing address is zero, then no failures have been detected. If no failures have been detected, proceed with routine 3.

6. Read and record the following:

a) The content of X'A' (failure count)

b) The content of X'B' (last failing address)

c) The content of X'C' (ZACC)

d) The content of X'D' (ONAC)

e) The content of the location whose address is contained in X'B'

f) The content of X'10'

g) The content of X'100'

7. Take the one's complement of the content of X'C'. Logically OR-gate the result with the content of X'D'. Take bits 18-31 of the result; express this as a four digit hexadecimal number. Call this number ADMASK.

$$\text{ADMASK} = \text{ONAC} + \overline{\text{ZACC}}$$

8. Look at the content of the last failing address (obtained in step 6e) to determine the category of the failures.

Description	Category
Pick one bit	1
Pick one byte	2
Pick all bits	3

9. Use the data obtained to select a paragraph from table 4-2. Go to the paragraph selected to further diagnose the failure.

Table 4-2. Fault Diagnosis, Zeros Discrimination

ADMASK		CATEGORY
0000	3100	
par. 4-21	par. 4-19	1
par. 4-24		2
par. 4-28	*	3
par. 4-26		1
†		2
par. 4-27		3

*Replace preamplifier select module 16J

†Replace module 30D

In the event that no applicable paragraph is found, suspect a multiple or unusual failure.

c. Routine 3 - ADDRESSING

1. Load the following program into general registers.

Note

All addresses and contents are in hexadecimal

Location	Contents	Mnemonics	Description
0	00000000	DATA	ZACC (zero-bit accumulator)
1	00003FFF	DATA	ONAC (one-bit accumulator)
2	00000000	DATA	Last failing address
3	FFFFC010	DATA	Index
4	35364000	STW, R3	
5	65300004	BIR, R3	
6	223FC010	LI, R3	
7	31364000	CW, R3	
8	6830000C	BCR, 3	
9	32200003	LW, RS	
A	49000003	OR, R0	
B	4B100003	AND, R1	
C	65300007	BIR, R3	

Location	Contents	Menmonics	Description
D	2E000000	WAIT	
E	00000000		Not used
F	00000000		

2. Clear PSW2, set PSW1 to X'00000004'.

3. Place the COMPUTE switch in RUN.

4. When the computer halts, display the contents of location 2.

5. If R2 = 0, no failures were detected, go to routine 4.

6. Take the one's complement of the content of R0. Logically OR-gate this with the contents of R1. Take bits 18-31 of the result and express the bits as a four digit hexadecimal number. Call this number ADMASK.

7. Load one of the following instructions into register 0.

Bank Size	Instruction
4K	32100FFF
8K	32101FFF
12K	32102FFF
16K	32103FFF

8. Clear PSW1, PSW2.

9. Display instruction address.

10. Turn on the hold switch.

11. Place the COMPUTE switch in RUN.

12. Look up ADMASK in table 4-3 to find the signals to scope.

d. Routine 4 - ONES DISCRIMINATION (PARITY)

1. Load the following program into the general registers. It may not be possible to load from binary cards since the IOP aborts an operation if a parity error is detected.

Note

All addresses and contents are in hexadecimal.

Location	Contents	Mnemonics	Description
0	00000000	DATA	ZACC (zero-bit accumulator)
1	00003FFF	DATA	ONAC (one-bit accumulator)
2	00000000	DATA	Last failing address
3	FFFFC010	DATA	Index
4	35F64000	STW, R15	Try one location
5	31F64000	CW, R15	
6	6CE00010	RD, R14	
7	21E00000	CI, R14	
8	6830000C	BCR, 3	
9	4B100003	AND, R1	Gather failure data
A	49000003	OR, R0	
B	32200003	LW, R2	
C	65300004	BIR, R3	Next location
D	2E000000	WAIT	
E	00000000	DATA	Parity check register
F	00000000	DATA	Pattern. Causes parity bit to be a one

2. Clear PSW1, PSW2.

3. Set the instruction address to X'00004'.

4. Display the instruction address.

5. Place the COMPUTE switch in RUN.

6. When the computer comes to a WAIT, display the content of register 2. If R2 = 0 go to routine 5.

7. Read and record the following:

a) The content of register 0 (ZACC).

b) The content of register 1 (ONAC).

c) The content of register 2 (last failing address).

8. Take the one's complement of the content of register 0. Logically OR-gate this result with the content of register 1. Take bits 18-31 of the result and express as a four digit hexadecimal number. Call this number ADMASK.

$$ADMASK = ONAC + \overline{ZACC}$$

9. Look up ADMASK in the following table to select a paragraph. Go to the paragraph selected to diagnose the failure.

Note

Parity bit number 32, byte number 3.

ADMASK	Paragraph
0000	4-21
1C00	4-18

Table 4-3. L-Register Signals

ADMASK	Suspect Signals (Assuming Port C)	Transfer and Latch Signals
0000	LXL(21D35), LG(07D07), NLXL(16D17), LXL0B(17D41), LXL1B(17D34), LXC0B(17D05), LXC1B(17D19)	
0001	L31(15D15), LC31L(18C22), LC31(08C20)	
0002	L30(15D14), LC30L(13C22), LC30(08C18)	LXL1B
0004	L29(15D13), LC29(08C13)	LXC1B
0008	L28(15D18), LC28(06D42)	
0010	L27(15D35), LC27(06D40)	
0020	L26(15D34), LC26(06D38)	
0040	L25(12D15), LC25(06D36)	LCL0B
0080	L24(12D14), LC24(06D34)	LXC0B
0100	L23(12D13), LC23(06D27)	
0200	L22(12D18), LC22(06D22)	
0400	L21(12D35), LC21(06D20)	
0800	L20(12D34), LC20(06D18)	
1000	L19(12D33), LC19(06D13), LC19L(18D45)	
2000	L18(12D37), LC18(06D10), LC18L(18D13)	

ADMASK	Paragraph
2280	4-18
3100	4-19
3E80	4-23

e. Routine 5 - ZEROS DISCRIMINATION (PARITY)

1. Load the following program into the general registers.

Note

All addresses and contents are in hexadecimal.

Location	Contents	Mnemonics	Description
0	00000000	DATA	ZACC (zero-bit accumulator)
1	00003FFF	DATA	ONAC (one-bit accumulator)
2	00000000	DATA	Last failing address
3	FFFFC010	DATA	Index
4	35F64000	STW,R15	Try one location
5	31F64000	CW,R15	
6	6CE00010	RD,R14	
7	21E00000	CI,R14	Try one location
8	6830000C	BCR,3	
9	4B100003	AND,R1	Gather failure data
A	49000003	OR,R0	
B	32200003	LW,R2	
C	65300004	BIR,R3	Next location
D	2E000000	WAIT	
E	00000000	DATA	Parity check register
F	00000001	DATA	Pattern. Causes parity bit to be zero

2. Clear PSW1, PSW2.

3. Set the instruction address to X'0004'.

4. Display the instruction address.

5. Place the COMPUTE switch in RUN.

6. When the computer comes to a WAIT, display the content of register 2. If R2 = 0, no errors have been detected and a more sophisticated diagnostic may be used.

7. Read and record the following:

a) The content of register 0 (ZACC).

b) The content of register 1 (ONAC).

c) The content of register 2 (Last failing address).

8. Take the one's complement of the content of register 0. Logically OR-gate this result with the content of register 1. Take bits 18-31 of the result and express as a four digit hexadecimal number. Call this number ADMASK.

9. Press SYSTEM RESET.

10. Set the select address switches to X'10'.

11. Display select address.

12. Read and record the state of the memory fault indicators.

13. Press SYSTEM RESET.

14. Set the select address switches to X'100'.

15. Display select address.

16. Read and record the state of the memory fault indicators.

17. If one and only one of these display operations resulted in a memory fault, go to paragraph 4-26.

18. Use the following to select a paragraph for failure diagnosis. Go to the paragraph selected.

ADMASK	Paragraph
0000	4-21
3100	4-19

4-14 Fault Isolation Tables and Data

Paragraphs 4-15 through 4-30 and the accompanying tables are directly related to the diagnostic routine described in paragraph 4-13. Refer to paragraph 4-13 for instructions in their use.

4-15 X-PREDRIVE MODULES.

ADMASK	Module
0030	9E
1040	9E, 10E
0003	10E
200C	If last failing address = 0000-1FFF ⟹ 7E, 8E Else ⟹ 5E, 6E

4-16 X-DRIVE.

a. AND-gate ADMASK with the last failing address.

b. Look the result up in table 4-4:

Table 4-4. Fault Isolation, X-Drive Modules

ADMASK · LASTFAIL		MODULE
0000 0001	0000 0010	11E
0002 0003	0020 0030	12E
0004 0005	0040 0050	13E
0006 0007	0060 0070	14E
0008 0009	1000 1010	15E
000A 000B	1020 1030	16E
000C 000D	1040 1050	17E
000E 000F	1060 1070	18E
2000 2001		19E
2002 2003		20E
2004 2005		21E
2006 2007		22E
2008 2009		23E
200A 200B		24E
200C 200D		25E
200E 200F		26E

4-17 Y-PREDRIVE.

a. AND-gate ADMASK with the last failing address. Express the result as a four digit hexadecimal number.

b. Look up the result in the following table.

If ADMASK equals 2280

ADMASK . LASTFAIL	Module Number
0000	7E
0080	
0200	
0280	
2000	5E
2080	
2200	
2280	

If ADMASK equals 1C00

ADMASK . LASTFAIL	Module Number
0000	8E
0400	
0800	
0C00	
1000	6E
1400	
1800	
1C00	

4-18 Y-DRIVE.

a. Determine the number of the failing bit. Divide it by 4 discarding the remainder. This is the half-byte number.

b. AND-gate ADMASK with the last failing address. Look up the result in table 4-5.

Table 4-5. Group Numbers for Y-Drive Modules

ADMASK .	LASTFAIL	Category Number
0000	0000	1
0080	0400	1
0200	0800	2
0280	0C00	2
2000	1000	3
2080	1400	3
2200	1800	4
2280	1C00	4

c. Use the group number and the half-byte number to determine the module number from table 4-6.

Table 4-6. Fault Isolation, Y-Drive Modules

CATEGORY NUMBER	HALF-BYTE NUMBER								
	0	1	2	3	4	5	6	7	8
1	32F	31F	24F	23F	16F	15F	08F	07F	04E
2	30F	29F	22F	21F	14F	13F	06F	05F	03E
3	28F	27F	20F	19F	12F	11F	04F	03F	02E
4	26F	25F	18F	17F	10F	09F	02F	01F	01E

4-19 SENSE PREAMPLIFIER.

a. Determine the bit number of the failing bit. Divide the bit number by 6 and discard any remainder.

b. AND-gate ADMASK with the last failing address. Express the result as a four digit hexadecimal number.

c. Use these two results to determine the module number from table 4-7.

Table 4-7. Fault Isolation, Sense Preamplifier Modules

ADMASK • LASTFAIL	BIT NUMBER 6					
	0	1	2	3	4	5
0000 0100	32J	28J	20J	15J	11J	03J
1000 1100	30J	22J	18J	13J	05J	03J
2000 2100	31J	27J	19J	14J	10J	02J
3000 3100	29J	21J	17J	12J	04J	02J

4-20 DATA GATE TERMS.

Failing Bits	Module
0 - 3	10A
4 - 7	
8 - 11	
12 - 15	
16 - 19	11B
20 - 23	
24 - 27	
28 - 31	

4-21 ADDRESS INDEPENDENT - SINGLE BIT.

a. Load the following program into the general registers.

Location	Contents	Mnemonic
0	35300FFF	STW, R3
1	32400FFF	LW, R4
2	68000000	BCR, 0
3	FFFFFFFF	DATA

b. With the program running, scope to isolate the trouble. Test point information is contained in table 4-8.

Table 4-8. Fault Isolation, Sense System (Single Bit)

BIT	MXX M-Register	MCXX Port C In	MCOXX Port C Out	MDXX Discriminator	NMXX M-Register
0	23B37	08A04	09A26	26J40	24B37
1	23B33	08A06	09A27	26J38	24B38
2	23B34	08A08	09A12	26J34	24B36
3	23B35	08A10	09A14	26J12	24B35
4	23B18	08A13	09A21	26J08	24B14
5	23B13	08A18	09A46	26J04	24B17
6	23B14	08A20	09A09	25J40	25B15
7	23B15	08A22	09A07	25J38	24B12
8	21B37	08A27	09A02	25J12	22B37
9	21B33	08A34	09A01	25J08	22B38
10	21B34	08A36	09A39	25J04	22B36
11	21B35	08A38	09A42	25J34	22B35
12	21B18	08A40	09B26	23J38	22B14
13	21B13	08A42	09B27	23J34	22B17
14	21B14	08B04	09B12	23J12	22B15
15	21B15	08B06	09B14	23J08	22B12
16	16B37	08B08	09B21	23J04	15B37
17	16B33	08B10	09B46	23J40	15B38
18	16B34	08B13	09B09	09J34	15B36
19	16B35	08B18	09B07	09J12	15B35
20	16B18	08B20	09B02	09J08	15B14
21	16B13	08B22	09B01	09J04	15B17
22	16B14	08B27	09B39	08J40	15B15
23	16B15	08B34	09B42	08J38	15B12
24	14B37	08B36	07C26	08J12	13B37
25	14B33	08B38	07C27	08J08	13B38
26	14B34	08B40	07C12	08J04	13B36
27	14B35	08B42	07C14	06J40	13B37
28	14B18	08C04	07C26	06J38	13B14
29	14B13	08C06	07C46	06J34	13B17
30	14B14	08C08	07C09	06J12	13B15
31	14B15	08C10	07C07	06J08	13B12
32	14A07	---	---	06J04	21A12

4-22 CORE DIODE MODULE. The open X-line diode:

a. Determines the number of the failing byte.

b. Uses the byte number and the last failing address to locate the module number in table 4-9.

Table 4-9. Fault Isolation, Core Diode Module, X-Line

LAST FAILING ADDRESS	BYTE NUMBER 0	1	2	3
0XXX	32G	24G	16G	08G
1XXX	28G	20G	12G	04G
2XXX	30G	22G	14G	06G
3XXX	26G	18G	10G	02G

4-23 CORE DIODE MODULE. The open Y-line diode:

a. Determines the byte number within which the failing bit is located.

b. Uses the byte number and the last failing address to locate the module number in table 4-10.

Table 4-10. Fault Isolation, Core Diode Module, Y-Line

LAST FAILING ADDRESS	BYTE NUMBER 0	1	2	3
0XXX	32G	24G	16G	08G
1XXX	28G	20G	12G	04G
2XXX	30G	22G	14G	06G
3XXX	26G	18G	10G	02G

4-24 ADDRESS INDEPENDENT BYTE.

a. Load the following program into the general registers:

Location	Contents	Mnemonic
0	35300FFF	STW, R3
1	32400FFF	LW, R4
2	68000000	BCR, 0
3	FFFFFFFF	

b. With this program running, scope to isolate the fault. Use table 4-11 for test point information.

Table 4-11. Fault Isolation, Sense System (Byte)

Byte	MXMx	MXCxB	MXDxB	MWx	MWxC	SASTx
0	18B46	20B04	19B46	26B35	08C22	24J29
1	18B47	20B02	19B44	26B21	08C27	24J18
2	18B44	17B04	19B04	27B21	08C34	07J29
3	18B45	17B02	19B02	27B21	08C36	07J18

4-25 ADDRESS INDEPENDENT - ALL BITS.

a. Replace 13D if X'A' shows a count of approximately one-half the number of locations tested. Otherwise, proceed to step 2b.

b. Load the following program into the general registers.

Location	Contents	Mnemonic
0	3530DFFF	STW
1	32400FFF	LW
2	68000000	
3	FFFFFFFF	

c. With this program running, scope the following points to isolate the failure.

TPXC	(22D35)
TNXC	(23D35)
TPYC	(24D35)
TNYC	(25D35)
TR220	(33C07)
TR020-1	(23C34)
DG-2	(26B01)
TPXV	(22D21)
TNXV	(23D21)
TPYV	(24D21)
TNYV	(25D21)
ADCMB	(15A14)
ADCDG	(11B10)
NTSSTB	(21D21)

4-26 INHIBIT.

Failing Bit	Module Number
0 - 5	32E
6 - 9	31E
10 - 15	30E
16 - 21	29E
22 - 25, 32	28E
26 - 31	27E

4-27 INHIBIT ENABLES - WORD ORIENTED.

a. If X'10' = FFFFFFFF, replace module 26D.

b. If X'100' = FFFFFFFF, replace module 25D.

4-28 ADDRESS INDEPENDENT - PICK ALL BITS.

a. Load the following program into the general registers.

Location	Contents	Mnemonic
0	35300FFF	STW, R3
1	32400FFF	LW, R4
2	68000000	BCR, 0
3	FFFFFFFF	

b. With this program running, scope the following points to isolate the problem:

1. TR020-1 (23C34) should be changing. If constantly low, replace module 23C.

2. NTSSTB (21D21) should be low for 200 ns.

4-29 PT17 POWER SUPPLY ADJUSTMENT

The PT17 Memory Power Supply Vc and Vd (+22V) outputs should be adjusted whenever a memory bank or size option is installed. Whenever a module is replaced in chassis E through J (magnetics) of a memory frame, the procedures in paragraphs 4-21 and 4-22 should be followed.

Marginal operation of the PT17 can result in intermittent failures which can cause hours of troubleshooting within the frame. If failures are of this nature, the PT17 should be adjusted before troubleshooting.

4-30 Special Tools and Test Equipment Required

The following special tools and test equipment are required to adjust the PT17 power supply:

a. Dc voltmeter, Digitek 211 or equivalent, with 1.8 kHz adapter, XDS part No. 158991

b. Ac voltmeter, Simpson 260 or equivalent

c. Thermometer, XDS part No. 153273

d. Compound, XDS part No. 129766

4-31 General

The PT17 is a series-regulated dc power supply that supplies Vd (+22V) voltage of 18 to 25V at 20A, and Vc voltage of 24V at 2A. The Vd (+22V) voltage is designed to track the temperature of the memory core. This circuit is called Vcr tracking. It causes Vd (+22V) track at a rate of -100 mV per degree centigrade. There is also an input from the memory core temperature protection circuit that shuts down the supply with a +4V signal if the memory overheats, (for example, in case of fan failure). The supply has coarse and fine margin adjust dials to change the output voltage from 18 to 25V. The supply has a current limit protection circuit as well as an overvoltage circuit. The regulation is ±1 percent for all conditions. It also has a thermostat switch that turns off the circuit breaker if the heatsink is overheated from a fan failure.

The PT17 Vd (+22V) output must be aligned in the system since the Vd (+22V) voltage and associated adjustments are a function of the temperature sensing diodes in the memory which it powers. All adjustments except Vd (+22V) output are normally preset at the factory. They require adjustment only if they are disturbed or if a PT17 module (WT14 or WT15) is replaced. Before proceeding with the PT17 alignment, check the output of the PT15 for 120 Vac ±3.0 percent using the 1.8 kHz adapter, and the PT16 logic supplies associated with memory for nominal voltages ±0.5 percent with margin switch at normal.

Unless otherwise specified, the computer is ON and in the IDLE mode, and the memory is at operating temperature. See figure 4-1 for the location of all adjustments. Perform all adjustments in the sequence given.

4-32 Vc Adjustment

Adjust J1R25 (Vc) for +24V ±1% at Vc output terminal TB1-2 (marked 25V, 2A).

4-33 Overvoltage (O/V) Adjustment

CAUTION

Care should be taken at all times to prevent Vd (+22V) from exceeding +30V, as this causes damage to the equipment.

a. Monitor Vd (+22V) output voltage at terminal TB1-3 (marked 25V, 20A).

b. Slowly adjust J2R6 (Vcr null) so Vd increases to +28V, or the circuit breaker trips on the PT17. The circuit breaker should trip between +27V and +28V. If the circuit breaker does not trip, proceed to step c. If it does trip within this range, proceed to the Vd adjustment procedure, paragraph 4-21.

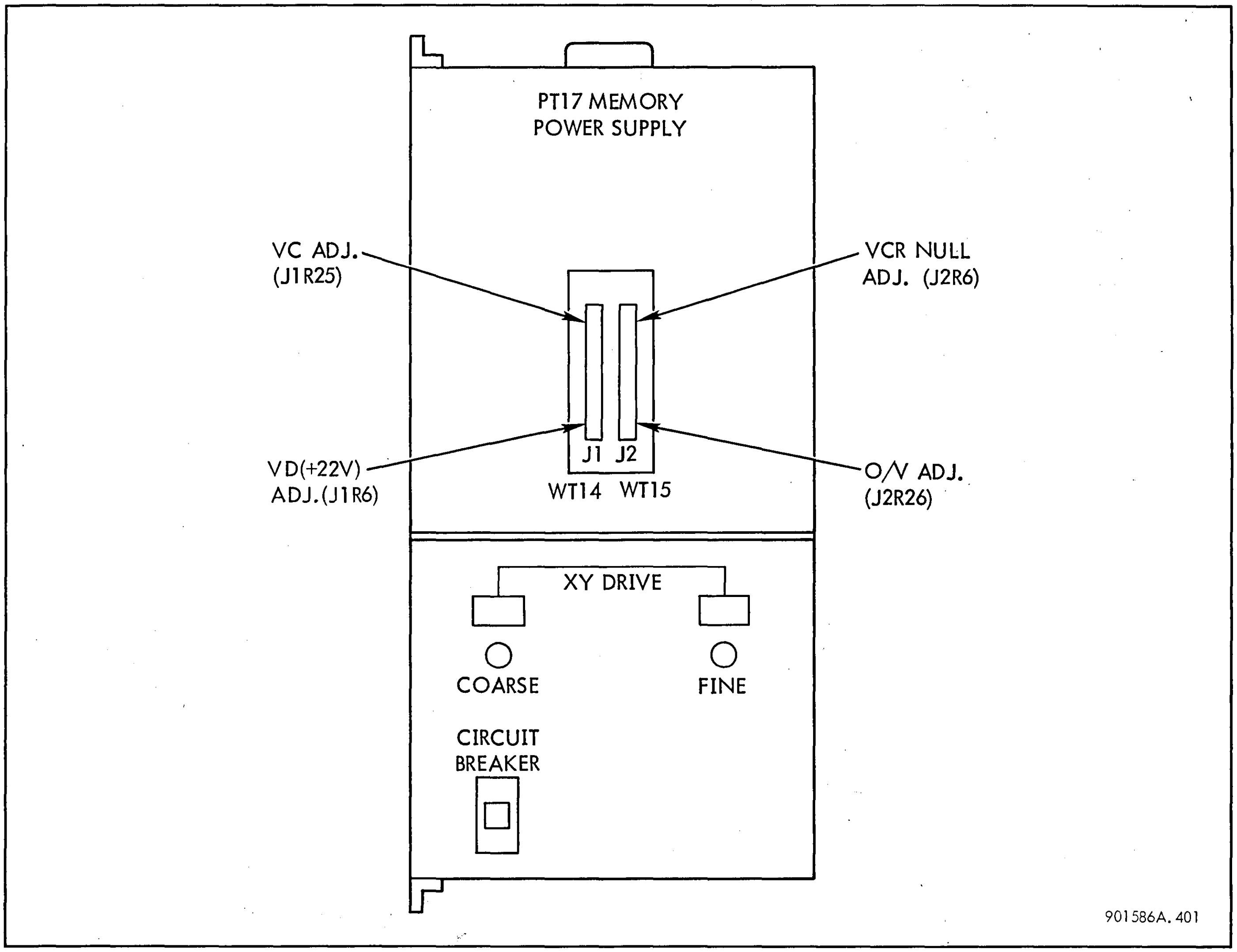

Figure 4-1. PT17 Power Supply Adjustment Locations

c. Adjust J2R6 (Vcr null) so that Vd reads +27.5V at TB1-3.

d. Slowly adjust J2R26 (O/V) counter-clockwise until the circuit breaker trips. This is the proper O/V setting.

e. Verify that the overvoltage is set properly by turning J2R6 (Vcr null) a few turns clockwise, and reset the circuit breaker to ON. While observing Vd (+22V) slowly increase Vd (X22V) by turning J2R6 (Vcr null) counterclockwise until the circuit breaker trips. Vd (+22V) should be between +27V and +28V at this time.

4-34 Vd (+22V) Adjustment

a. Turn PT17 circuit breaker to OFF.

b. Remove the top front cover of the PT17.

c. Remove the WT15 module from location J2.

d. Turn PT17 circuit breaker to ON.

e. Set COARSE and FINE dials to position 9.

f. Adjust J1R6 (Vd) so that Vd (+22V) output (TB1-3) is +25V.

g. Set PT17 circuit breaker to OFF.

h. Replace WT15 module in J2.

i. Set PT17 circuit breaker to ON.

4-35 Vcr Null Adjustment (SCHMOO)

a. Set COARSE and FINE dials to position 5.

b. Adjust J2R6 (Vcr null) so that Vd (TB1-3) reads +21.5V.

c. Load MEDIC 75 diagnostic, and allow it to run only in the frame being adjusted. While performing the following Vd (+22V) adjustments, observe the PCP display for stopping of the program or a parity error indication.

d. Slowly adjust the Vd (+22V) voltage in the positive direction by turning J2R6 (Vcr null) clockwise, and observing both the Vd (+22V) output (TB1-3) and the PCP display. It may be necessary to turn J2R6 fully counterclockwise, increment the COARSE and FINE dials towards position 9 and then turn J2R6 clockwise again. When the PCP indicates that MEDIC 75 no longer runs or when a parity error occurs, reduce Vd (+22V) slightly until MEDIC again runs without error. Record the Vd output (Vd max).

e. Return the COARSE and FINE dials to position 5.

f. Slowly adjust the Vd (+22V) voltage in the negative direction by turning J2R6 (Vcr null) counterclockwise and observe both the Vd (+22V) output (TB1-3) and the PCP display. It may be necessary to turn J2R6 fully clockwise and to decrement the COARSE and FINE dials towards position 1, and then turn J2R6 counterclockwise again. When the PCP indicates that MEDIC 75 no longer runs, or a parity error occurs, increase Vd (+22V) slightly until MEDIC again runs without error. Record the Vd (+22V) output (Vd min).

Note

For an acceptable adjustment, the Vd (+22V) minimum and maximum settings must be related to memory ambient temperature and must be outside the limits shown in figure 4-2 for existing ambient memory temperature. The ambient memory temperature is obtained by measuring the air temperature just under the bottom fans, using a thermometer XDS part No. 153273. Add the readings for each row and divide by the number of readings taken.

g. Set COARSE and FINE dials to position 5.

h. Adjust J2R6 (Vcr null) so that Vd (+22V) output (TB1-3) is equal to the following:

$$\text{Final Vd output} = \frac{\text{Vd max} + \text{Vd min}}{2}$$

i. Reseal adjustment pots J1R6 and J2R26 with compound XDS part No. 129766. Cover half the screw head.

j. Replace top front cover on PT17.

4-36 Overtemperature Check

With the PT17 on, remove the XT14 module in location 27A. This simulates an overtemperature condition in memory and should cause the circuit breaker to trip. If it does not, the overvoltage adjustment should be rechecked. If that does not solve the problem, the WT15 (J2) in the PT17 may be defective.

4-37 Phase Sequence Charts

The following phase sequence charts (tables 4-12, 4-13, and 4-14) are included to assist in troubleshooting.

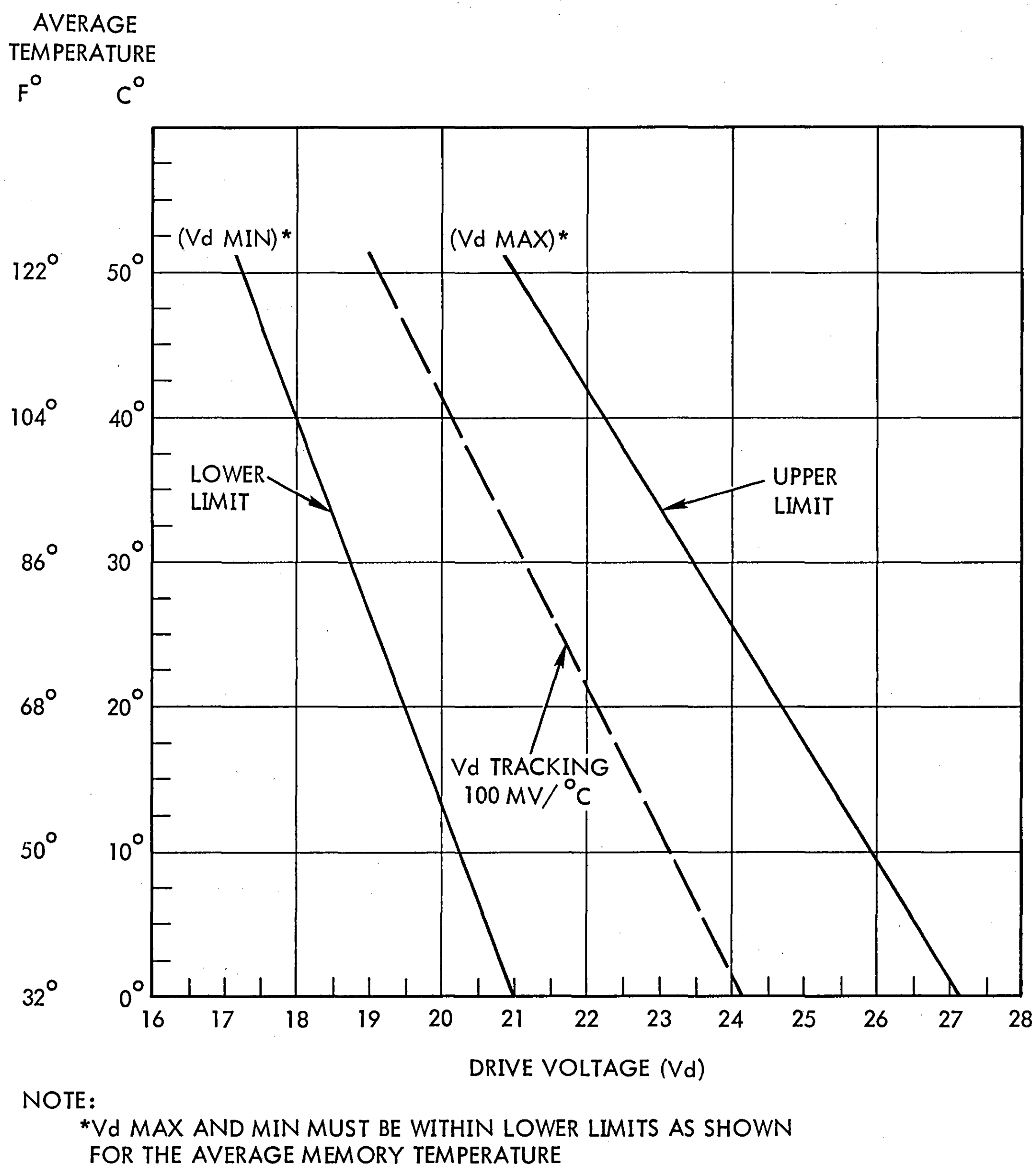

Figure 4-2. Minimum Vd Limits

Table 4-12. Read-Restore Mode, Port C, Phase Sequence

Phase	Function Performed	Signals Involved		Comments
	Selection interval			
	Address port C	LC15-LC31	= /LC15/-/LC31/	Address lines connected to port C
	Address recognition	AHC	= (21CK11 LC15 + N21CK11 NLC15 + 21CK12 LC16S + N21CK12 NLC16S + . . . + N21CK15 NLC19S) (NLC18 NLC19 12K)	Address here, port C. Five most significant address bits match port C starting address switches
TR000	Begin active interval	MQC	= /MQC/	Memory request received from source
		MQCT	= NORAC NORAB (MQC N20CK05 + 20CK05)	Simulated memory request switch off or on and no port override
	Start read delay line	S/READDL	= MI NTR060	
		MI	= MI NTR100 NPFSRDLDC1 + AHC MQCT NMB NAB + . . .	Memory initiate latch
	Latch address into L-register	L18	= L18 LXL0B + LC18L LXC0B + . . .	
		L19	= L19 LXL0B + LC19L LXC0B + . . .	
		L20	= L20 LXL0B + LC20 LXC0B + . . .	
		⋮	⋮	
		L29	= L29 LXL1B + LC29 LXC1B + . . .	
		L30	= L30 LXL1B + LC30L LXC1B + . . .	
		L31	= L31 LXL1B + LC31L LXC1B	
		LXL0B	= LXL	L-register latching terms
		LXL1B	= LXL	
		LXC0B	= ADC LG	
		LXC1B	= ADC LG	
		LXL	= LXL NTW460 NPFSRDLDT2 + MI	

(Continued)

Table 4-12. Read-Restore Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved			Comments
TR000 (Cont.)	Select and turn on X-voltage predrivers and drivers	TNXV	=	TNXV NTR320 NTW480 NPFSRDLDT1 + X TR000 + ...	Time for negative X-voltage. For drivers, see figure 3-10
		TPXV	=	TPXV NTR320 NTW480 NPSRDLDT1 + NX TR000 +...	Time for positive X-voltage. For drivers, see figure 3-9
		X	=	L22 L25 + NL22 NL25	X-current direction control (L22 = L25)
		NX	=	L22 NL25 + NL22 L25	X-current direction control (L22 ≠ L25)
	Select and turn on Y-current and voltage predrivers and drivers	TPYC	=	TPYC NTR30 NTW480 NPFSRDLDT2 + Y TR000 + ...	Time for positive Y-current. For drivers, see figure 3-13
		TNYV	=	TNYV NTR320 NTW480 NPFSRDLDT2 + Y TR000 + ...	Time for negative Y-voltage. For drivers, see figure 3-15
		TNYC	=	TNYC NTR320 NTW480 NPFSRDLDT2 + NY TR000 + ...	Time for negative Y-current. For drivers, see figure 3-14
		TPYV	=	TPYV NTR320 NTW480 NPFSRDLDT2 + NY TR000 + ...	Time for positive Y-voltage. For drivers, see figure 3-15
		Y	=	NL22 NL23 NL25 + L22 L23 L25 + L22 NL23 L25 + NL22 L23 L25	Y-current direction control. (Sum L22, L23, L25 = even)
		NY	=	L22 L23 L25 + NL22 NL23 L25 + NL22 L23 NL25 + L22 NL23 NL25	Y-current direction control. (Sum L22, L23, L25 = odd)
	Clear sense preamplifiers	PASL0	=	SDECEN ...	See TR060 time below for sense line selection
		⋮		⋮	
		PASL7	=	SDECEN ...	
		SDECEN	=	NTR000 + ...	
TR020	Clear M-register latches	M00	=	M00 MXM0 + ...	Clear byte 0
		⋮		⋮	
		M07	=	M07 MXM0 + ...	
		M08	=	M08 MXM1 + ...	Clear byte 1
		⋮		⋮	
		M15	=	M15 MXM1 + ...	

(Continued)

Table 4-12. Read-Restore Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TR020 (Cont.)		M16 = M16 MXM2 + ...	Clear byte 2
		⋮	
		M23 = M23 MXM2 + ...	
		M24 = M24 MXM3 + ...	Clear byte 3
		⋮	
		M31 = M31 MXM3 + ...	
		M32 = M32 MXM32 + ...	Clear Parity
		MXM(0), (1), (2), (3) = NTR020 + ...	
		MXM32 = NTR20 + ...	
TR060	Address release	AROC = ADCCO TR060	Source may use address release to drop LC15-LC31, and MQC
		ADCCO = ADC	
	Unlatch read delay line start	S/READDL = MI NTR060 ...	
	Enable sense line preamplifiers	PASL0 = NL18 NL19 NL23 SDECEN	Selects active sense line
		PASL1 = NL18 NL19 L23 SDECEN	
		PASL2 = NL18 L19 NL23 SDECEN	
		PASL3 = NL18 L19 L23 SDECEN	
		PASL4 = L18 NL19 NL23 SDECEN	
		PASL5 = L18 NL19 L23 SDECEN	
		PASL6 = L18 L19 NL23 SDECEN	
		PASL7 = L18 L19 L23 SDECEN	
		SDECEN = TR060 + ...	
	Enable read	RD = NMW0 NMW1 NMW2 NMW3	All byte indicators are false for read
		MW0 = MW0 RESMW + MW0C ADCMW TMW-1 + ...	Write byte 0
		MW1 = MW1 RESMW + MW1C ADCMW TMW-1 + ...	Write byte 1
		MW2 = MW2 RESMW + MW2C ADCMW TMW-2 + ...	Write byte 2
		MW3 = MW3 RESMW + MW3C ADCMW TMW-2 + ...	Write byte 3

(Continued)

Table 4-12. Read-Restore Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TR060 (Cont.)		ADCMW = ADC + . . .	Access decision, port C
		TMW-1 = TR060 NTR100	
		TMW-2 = TR060 NTR100	
		MW0C = /MW0C/	Memory write byte lines
		MW1C = /MW1C/	
		MW2C = /MW2C/	
		MW3C = /MW3C/	
TR080	Select and turn on X-current pre-drivers and drivers	TPXC = TPXC NTR320 NTW480 NPFSRDLDT1 + X TR080 + . . .	Time for positive X-current. For drivers, see figure 3-8
		TNXC = TNXC NTR320 NTW480 NPFSRDL0T1 + X TR080 + . . .	Time for negative X-current. For drivers, see figure 3-7
TR100	Unlatch memory initiate	MI = MI NTR100 . . .	
TR140	Enable sense amplifier strobe	SAST(0), (1), (2), (3) = NTSSTB	Sense strobe goes false, allowing sense amplifier to respond to core read-out
		NTSSTB = NTSSTB NTR140 + TR360 + PFSRDLD	
TR160 TW000	Start write delay line	S/WRITEDL = IWD	
		IWD = TR160 NWP	Initiate write delay
		NWP = RD + WF	
TR200 TW040	Enable second request, port C	SRA0C = A0CCO TR200 + . . .	Allows source to begin second memory request for read only
TR220 TW060	Read data into M-register	M00 = MD00 MXD0B + . . .	One's into M-register. Byte 0
		⋮	
		M07 = MD07 MXD0B + . . .	
		M08 = MD08 MXD1B + . . .	Byte 1
		⋮	
		M15 = MD15 MXD1B + . . .	
		M16 = MD16 MXD2B + . . .	Byte 2
		⋮	
		M23 = MD23 MXD2B + . . .	

(Continued)

Table 4-12. Read-Restore Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TR220 TW060 (Cont.)		M24 = MD24 MXD3B + . . .	Byte 3
		⋮ ⋮	
		M31 = MD31 MXD3B + . . .	
		MXD0B = MXD0B NTR420 NPFSRDLDM + TR220 NWF	Transfer terms
		MXD1B = MXD1B NTR420 NPFSRDLDM + TR220 NWF	
		MXD2B = MXD2B NTR420 NPFSRDLDM + TR220 NWF	
		MXD3B = MXD3B NTR420 NPFSRDLDM + TR220 NWF	
		NM00 = NMD00 MXD0I + . . .	Zeros into M-register. Byte 0
		⋮ ⋮	
		NM07 = NMD07 MXD0I + . . .	
		NM08 = NMD08 MXD1I + . . .	Byte 1
		⋮ ⋮	
		NM15 = NMD15 MXD1I + . . .	
		NM16 = NMD16 MXD2I + . . .	Byte 2
		⋮ ⋮	
		NM23 = NMD23 MXD2I + . . .	
		NM24 = NMD24 MXD3I + . . .	Byte 3
		⋮ ⋮	
		NM31 = NMD31 MXD3I + . . .	
		MXD0I = MXD0I NTR420 NPFSRDLDM + TR220 NWF	Transfer terms
		MXD1I = MXD1I NTR420 NPFSRDLDM + TR220 NWF	
		MXD2I = MXD2I NTR420 NPFSRDLDM + TR220 NWF	
		MXD3I = MXD3I NTR420 NPFSRDLDM + TR220 NWF	

(Continued)

Table 4-12. Read-Restore Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved		Comments
TR240 TW080	Gate data onto port C data lines	/MC00/	= MCO00	The read data from the sense amplifier takes two paths; one path leads into the M-register (see TR220), the other path bypasses M-register and goes directly to the port output drivers (MCO00-MCO31), where it is gated onto the data lines by data gates DGC0-DGC7
		⋮	⋮	
		/MC31/	= MCO31	
		MCO00	= MD00 DGC0 + M00 DGC0	
		⋮	⋮	
		MCO31	= MD31 DGC7 + M31 DGC7	
		DGC0	= ADCDG DG2	
		⋮	⋮	
		DGC7	= ADCDG DG2	
		ADCDG	= ADC	
		DG2	= DG2 NTR420 NPFSRDLDM + RD TR240	
	Early data release	EDR	= TR240 NTR300	Notifies source that data is on data lines
TR320 TW160	Turn off X- and Y-currents and voltage	TNXV, TPXV, TPYC, TNYV, TNYC, TPYV		See TR000 for latch terms
		TPXC, TNXC		See TR080 for latch terms
TR360 TW200	Disable sense amplifiers	SAST(0), (1), (2), (3)	= NTSSTB	
		NTSSTB	= TR360 + . . .	Strobe input
	Latch Y-inhibit	TNYI	= TNYI NTW560 NPFSRDLDT2 + Y TW200	Inhibits Y-current to write zeros in the cores
	Data release	DROC	= ADCCO TR360 RD + . . .	Last chance for source to accept data. Prepare to drop data lines
TR400 TW240	Turn on X- and Y-current and voltage drivers	TPXC	= TPXC NTR320 NTW480 NPFSRDLDT1 + NX TW240 + . . .	Restores data to cores from M-register
		TNXC	= TNXC NTR320 NTW480 NPFSRDLDT1 + X TW240 + . . .	Same address bits select X- and Y-drivers so that X- and Y-currents are reversed in direction from that in TR000 during the read portion of the cycle
		TNXV	= TNXV NTR320 NTW480 NPFSRDLDT1 + NX TW240	
		TPXV	= TPXV NTR320 NTW480 NPFSRDLDT1 + X TW240	

(Continued)

Table 4-12. Read-Restore Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TR400 TW240 (Cont.)		TPYC = TPYC NTR320 NTW480 NPFSRDLDT2 + NY TW240	
		TNYC = TNYC NTR320 NTW480 NPFSRDLDT2 + Y TW240	
		TPYV = TPYV NTR320 NTW480 NPFSRDLDT2 + Y TW240	
		TNYV = TNYV NTR320 NTW480 NPFSRDLDT2 + NY TW240	
		X = L22 L25 + NL22 NL25	X-current direction control. L22 = L25
		NX = L22 NL25 + NL22 L25	L22 ≠ L25
			Y-current direction control
		Y = NL22 NL23 NL25 + L22 L23 NL25 + L22 NL23 L25 + NL22 L23 L25	Sum L22, L23, L25 even
		NY = L22 L23 L25 + NL22 NL23 L25 + NL22 L23 NL25 + L22 NL23 NL25	Sum L22, L23, L25 odd
TR420 TW260	Unlatch MXD(X)B and MXD(X)I	MXD(X)B = MXD(X)B NTR420 ...	See TR220 for latch terms
		MXD(X)I = MXD(X)I NTR420...	
	Unlatch data gate DG(X)(X)	DGC(X) = ADCDG DG2	See TR240 for latch terms
		DG2 = DG2 NTR420 ...	
TR460 TW300	Output parity	POKOC = POK ADCC0	Parity OK
		POO = POK TR460 NPFSRDLDM + AP P527 M32 PG + NAPE PG	
		PG = TR460 NTR500 NWFS	
		PEOC = PE ADCC0	Parity error
		PE = PE TR460 NPFSRDLDM + NAP NP527 NM32 PG + APE PG	
TW460	Unlatch L-register	LXL = LXL NTW460 ...	See TR000 for latch terms

(Continued)

Table 4-12. Read-Restore Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TW480	Turn off X and Y-currents	TPXC, TNXC, TNXV, TPXV, TPYC, TYNC, TPYV, TNYV	See TR400, TW240 for latch terms
TW560	Disable Y-inhibit	TNYI = TNYI NTW560 . . .	See TR360, TW200 for latch terms
	End read-restore mode		

Table 4-13. Full Clear-Write Mode, Port C, Phase Sequence

Phase	Function Performed	Signals Involved	Comments
	Selection interval		
	Address port C	LC15-LC31 = /LC15/-/LC31/	Address lines to port C
	Address recognition	AHC = (21CK11 LC15 + N21CK11 NLC15 + 21CK12 LC16 + N21CK12 NLC16 + . . . + N21CK15 NLC195) (NLC18 NLC19 12K)	Address here, port C, five most significant address bits match port C starting address switches
TR000	Begin active interval Start read delay line Latch address into L-register Select and turn an X- and Y-voltage, and Y-current predrivers and drivers Clear sense preamplifiers	Same as read-restore mode	See TR000, read-restore mode
TR020	Clear M-register latches	Same as read-restore mode	See TR020, read-restore mode
TR060	Address release. Unlatch read delay line start		
	Enable sense line preamplifiers	Same as read-restore mode	See TR060, read-restore mode
	Enable write full	WF = MW0 MW1 MW2 MW3 N(ADCMB ABOC) + . . .	All byte indicators true for clear-full write
		MW0 = MW0 RESMW + MW0C ADCMW TMW-1 + . . .	Write byte 0
		MW1 = MW1 RESMW + MW1C ADCMW TMW-1 + . . .	Write byte 1
		MW2 = MW2 RESMW + MW2C ADCMW TMW-2 + . . .	Write byte 2
		MW3 = MW3 RESMW + MW3C ADCMW TMW-2 + . . .	Write byte 3
		ADCMW = ADC + . . .	Access decision, port C
		TMW-1 = TR060 NTR100	
		TMW-2 = TR060 NTR100	
		MW0C = /MW0C/	Memory write-byte lines
		MW1C = /MW1C/	
		MW2C = /MW2C/	
		MW3C = /MW3C/	

(Continued)

Table 4-13. Full Clear-Write Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TR080	Select and turn on X-current pre-drivers and drivers	Same as read-restore mode	See TR080, read-restore mode
TR100	Unlatch memory initiate	MI = MI NTR100	
TR140	Enable sense amplifier strobe	SAST(0), (1), (2), (3) = NTSSTB NTSSTB = NTSSTB NTR140 + TR360 + PFSRDLD	Sense strobe goes false, allowing sense amplifier to respond to core read-out. However, core data does not enter M-register because MXD0B at TR220 is inhibited.
TR160 TW000	Start write delay line	S/WRITEDL = IWD IWD = TR160 NWP NWP = RD + WF	Initiate write delay
	Latch port data into M-register	M00 = MC00 MXC0B + ... ⋮ M07 = MC07 MXC0B + ...	Ones into M-register. Byte 0
		M08 = MC08 MXC1B + ... ⋮ M15 = MC15 MXC1B + ...	Byte 1
		M16 = MC16 MXC2B + ... ⋮ M23 = MC23 MXC2B + ...	Byte 2
		M24 = MC24 MXC3B + ... ⋮ M31 = MC31 MXC3B + ...	Byte 3
		MXC0B = ADCMB WF TR160 ⋮ MXC3B = ADCMB WF TR160	Transfer terms
		NM00 = NMC00 MXC0I + ... ⋮ NM07 = NMC07 MXC0I + ...	Zeros into M-register. Byte 0

(Continued)

Table 4-13. Full Clear-Write Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TR160 TW000 (Cont.)		NM08 = NMC08 MXC1I + . . . ⋮ ⋮ NM15 = NMC15 MXC1I + . . .	Byte 1
		NM16 = NMC16 MXC2I + . . . ⋮ ⋮ NM23 = NMC23 MXC2I + . . .	Byte 2
		NM24 = NMC24 MXC3I + . . . ⋮ ⋮ NM31 = NMC31 MXC3I + . . .	Byte 3
		MXC0I = ADCMI WF TR160 ADCMI = ADC	
TR200 TW040	Enable second request, port C	SRAOC = ADCCO TR200 + . . .	
TR240 TW080	Data release, port C	DROC = ADCCO WFS TR240 + . . . WFS = WF	Source may drop its data lines
TR300 TW140	Parity into M32	M32 = AP P527 M32XP + NAP NP527 M32XP + . . . M32XP = WFS TR300 + . . .	
TR320 TW160	Turn off X- and Y-currents and voltage	TNXV, TPXV, TPYC, TNYC, TPYV	See read-restore mode TR000 for latch terms
		TPXC, TNXC	See read-restore mode TR080 for latch terms
TR360 TW200	Disable sense amplifiers	SAST(0), (1), (2), (3) = NTSSTB	
		NTSSTB = TR360 + . . .	Strobe input
	Latch Y-inhibit	TNYI = TNYI NTW560 NPFSRDLDT2 + Y TW200	Inhibits Y-current to write zeros into the cores
TR400 TW240	Turn on X- and Y-current and voltage drivers	Same as read-restore mode	Writes data from M-register into cores. See read-restore mode, TR400, TW240

(Continued)

Table 4-13. Full Clear-Write Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TW460	Unlatch write byte indicators	MW(0), (1), (2), (3) = MW0 RESMW + . . .	
		RESMW = NTW460 . . .	
	Disable write full	WF = MW0 MW1 MW2 MW3 . . .	
	Unlatch L-register	LXL = LXL NTW460 . . .	
TW480	Turn off X- and Y-currents	TPXC, TNXC, TNXV, TPXV, TPYC, TNYC, TPYV, TNYV	See read-restore mode TR400, TW240 for latch terms
TW560	Turn off Y-inhibit	TNYI = TNYI NTW560 . . .	
	End full clear-write mode		

Table 4-14. Partial Write Mode, Port C, Phase Sequence

Phase	Function Performed	Signals Involved	Comments
	Selection interval Address port C Address here, port C	 LC15-LC31 = /LC15-LC31/ AHC = ?	 Address lines to port C Address here, port C, five most significant address bits match port C starting address switches
TR000	Begin active interval Start read delay line Latch address into L-register Select and turn on X- and Y-voltage and Y-current predrivers and drivers Clear sense preamplifiers	Same as read-restore mode	See TR000, read-restore mode
TR020	Clear M-register latches	Same as read-restore mode	See TR020, read-restore mode
TR060	Address Release Unlatch read delay line start Enable sense line preamplifiers Enable write partial	 Same as read-restore mode WP = NRD NWF N(ADCMB ABOC) + . . . ADCMB = ADC ABOC = /ABOC/	 See TR060, read-restore mode Access decision, port C Abort. Change from write to read
TR080	Select and turn on X-current pre-drivers and drivers	Same as read-restore mode	See read-restore mode TR080
TR100	Unlatch memory initiate	MI = MI NTR100	
TR140	Enable sense amplifier strobe	Same as read-restore mode	See read-restore mode, TR140
TR200	Enable second request, port C	SRAOC = ADCCO TR200 + . . .	Allows source to begin second request for read only
TR220	Read data into M-register	Same as read-restore mode	See read-restore mode, TR220
TR320	Turn off X- and Y-currents and voltages	TNXV, TPXV, TPYC, TNYV, TNYC, TPYV TPXC, TNXC	See read-restore mode TR000 for latch terms See read-restore mode, TR080 for latch terms

(Continued)

Table 4-14. Partial Write Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved		Comments
TR360	Disable sense amplifiers	SAST(0), (1), (2), (3)	= NTSSTB	
		NTSSTB	= TR360 + . . .	Strobe input
TR420	Unlatch M-register transfer terms MXD(X)B and MXD(X)I	MXD(X)B	= MXD(X)B NTR420 . . .	See read-res.ore mode TR220 for complete latch terms
		MXD(X)I	= MXD(X)I NTR420 . . .	
TR460	Output parity	Same as read-restore mode		See read-restore mode, TR460
TR480	Clear M-register latches if respective byte indicator is false	M00	= M00 MXM0 + . . .	Byte 0
		⋮	⋮	
		M07	= M07 MXM0 + . . .	
		M08	= M08 MXM1 + . . .	Byte 1
		⋮	⋮	
		M15	= M15 MXM1 + . . .	
		M16	= M16 MXM2 + . . .	Byte 2
		⋮	⋮	
		M23	= M23 MXM2 + . . .	
		M24	= M24 MXM3 + . . .	Byte 3
		⋮	⋮	
		M31	= M31 MXM3 + . . .	
		NMXM0	= MW0 TR480 WP + . . .	
		NMXM1	= MW1 TR480 WP + . . .	
		NMXM2	= MW2 TR480 WP + . . .	
		NMXM3	= MW3 TR480 WP + . . .	
TR560 TW000	Start write delay line	S/WRITEDL	= IWD	
		IWD	= TR560 WP + . . .	Initiate write delay
	Latch port data into M-register if respective byte indicator is true	M00	= MC00 MXC0B + . . .	Ones into M-register. Byte 0
		⋮	⋮	
		M07	= MC07 MXC0B + . . .	
		M08	= MC08 MXC1B + . . .	Byte 1
		⋮	⋮	
		M15	= MC15 MXC1B + . . .	

(Continued)

Table 4-14. Partial Write Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TR560 TW000 (Cont.)		M16 = MC16 MXC2B + ...	Byte 2
		⋮ ⋮	
		M23 = MC23 MXC2B + ...	
		M24 = MC24 MXC3B + ...	Byte 3
		⋮ ⋮	
		M31 = MC31 MXC3B + ...	
		MXC0B = ADCMB MW0 WP TR560 +...	
		MXC1B = ADCMB MW1 WP TR560 +...	Transfer terms
		MXC2B = ADCMB MW2 WP TR560 +...	
		MXC3B = ADCMB MW3 WP TR560 + ...	
		NM00 = NMC00 MXC0I + ...	Zeros into M-register. Byte 1
		⋮ ⋮	
		NM07 = NMC07 MXC0I + ...	
		NM08 = NMC08 MXC1I + ...	Byte 2
		⋮ ⋮	
		NM15 = NMC15 MXC1I + ...	
		NM16 = NMC16 MXC2I + ...	Byte 3
		⋮ ⋮	
		NM23 = NMC23 MXC2I + ...	
		NM24 = NMC24 MXC3I + ...	Byte 4
		⋮ ⋮	
		NM31 = NMC31 MXC3I + ...	
		MXC0I = ADCMI MW0 WP TR560 +...	Transfer terms
		MXC1I = ADCMI MW1 WP TR560 +...	
		MXC2I = ADCMI MW2 WP TR560 +...	
		MXC3I = ADCMI MW3 WP TR560 +...	
TR600 TW040	Data release on port C	DROC = WP ADCCO TR600 + ...	Allows source to drop data lines

(Continued)

Table 4-14. Partial Write Mode, Port C, Phase Sequence (Cont.)

Phase	Function Performed	Signals Involved	Comments
TW100	Parity into M32	M32 = AP P527 M32XP + NAP NP527 M32XP + ... M32XP = WP TW100 + ...	
TW200	Latch Y-inhibit	TNYI = TNYI NTW560 NPFSRDLDT2 + Y TW200	Inhibits Y-current to write zeros
TW240	Turn on X- and Y-current and voltage drivers	Same as read-restore mode	See read-restore mode TW240. Restores new word from M-register into cores
TW460	Reset memory write byte indicators Disable write partial Unlatch L-register	MW0 = MW0 RESMW + ... MW1 = MW1 RESMW + ... MW2 = MW2 RESMW + ... MW3 = MW3 RESMW + ... RESMW = NPFSRDLDT NTW460 NAB0 WP = NRD NWF N(ADCMB ABOC) + ... RD = NMW0 NMW1 NMW2 NMW3 LXL = LXL NTW460 ...	 See read-restore mode TR000 for latch terms
TW480	Turn off X- and Y-currents	TPXC, TNXC, TNXV, TPXV, TPYC, TNYC TPYV, TNYV	See read-restore mode TR400, TW240 for latch terms
TW560	Disable Y-inhibit End partial write mode	TNYI = TNYI NTW560 ...	

APPENDIX A
ILLUSTRATED PARTS BREAKDOWN

A-1 GROUP ASSEMBLY PARTS LIST

The Group Assembly Parts List is a breakdown of all systems, assemblies, and subassemblies which can be disassembled, reassembled, or replaced and which are contained in the end article. The Group Assembly Parts List consists of columnar listings of parts related to illustrations. Parts are listed in order of disassembly sequence, except in cases where sequence of disassembly cannot be maintained. Attaching parts are listed below the related assembly or subassemblies. Items which are purchased in bulk form (for example, wire and insulating material) are not listed.

Each parts list table is arranged in seven columns as follows:

a. The figure number of the part listed and the index number corresponding to the illustration reference

b. The XDS manufacturer's part number for the part

c. The vendor's part number for the part (if available)

d. A brief description of the part

e. The manufacturer's code for the part

f. The quantity of the part used per assembly

g. Usable on code column indicating that when a letter is used in the code column, the use of the coded part is restricted to the model identified by the code letter. (Where no letter symbol appears in this column, the part is used on all models of this configuration.)

How to use the Illustrated Parts Breakdown

To obtain information about a part, the following steps should be taken:

a. Refer to the applicable assembly breakdown

b. Compare the part with the illustration until part is located

c. Note the index number

d. Locate the index number in the corresponding Group Assembly Parts List

e. Find the part number and name of part opposite the index number listed

A-2 NUMERICAL INDEX

This index is a listing of the items contained in the Group Assembly Parts List. The numerical order of the index (table A-14) is determined by the XDS part number.

Illustrated Parts Breakdown Contents

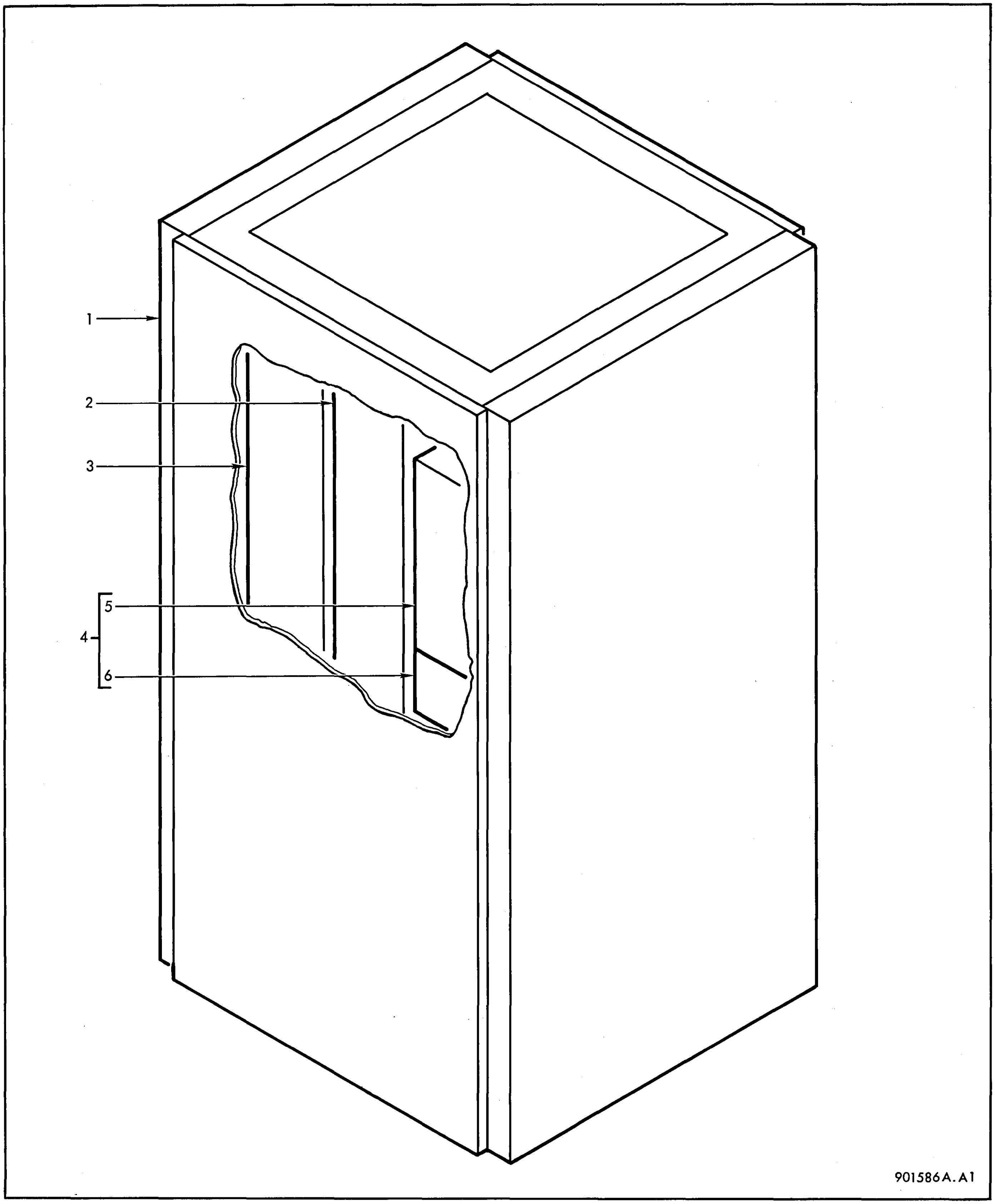

Figure A-1. Basic 4K X 33 Bit Assembly (Port C)

Table A-1. Basic 4K X 33 Bit Assembly (Port C)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-1-			Basic Memory Assy Sigma 5 and 7	XDS		
1-	132546Y*		Basic 4K X 33 Bit Assy (Port C)		1	8251/ 8451
-1	131416		. Basic Cabinet Assy		1	
-	139203		. Hardware Kit/Basic Cabinet (Ref Instl Dwg 127409)		1	
-	131410		. Side Panel Assy		2	
-	131419		. Door, Rear or Front		2	
-2	117500Y[†]		. Memory Frame Assy (See Fig. A-2) (Center Frame - Frame 2)		2	
-	139205		. Hardware Kit/Center Frame (Ref Instl Dwg 127409)		1	
-3	117500Y**		. Memory Frame Assy (Same as Fig. A-2) (Front Frame-Frame 1)		1	Option
-	139204		. Hardware Kit/Front Frame (Ref Instl Dwg 127409)		1	
-4	136978F[††]		. Fixed Accessory Frame Assy (See Fig. A-9)		1	Option
-	139515		. Hardware Kit/Fixed Frame (Ref Instl Dwg 127409)		1	
-5	130625J[††]		. Memory Port Expansion F Assy (See Fig. A-10)		1	Option
-6	130626H[††]		. Memory Port Expansion S Assy (See Fig. A-11)		1	Option
			*Port C is standard with the Sigma 5 and is included in the 4K basic assembly. Post B (Fig. A-7) is standard with the Sigma 7			
			[†]The first 16K memory block is located in the center frame			
			**The second 16K memory block (expansion to 32K) is located in the front frame			
			[††]Expansion kit F or expansion kit S, if required, is installed in the fixed accessory frame			

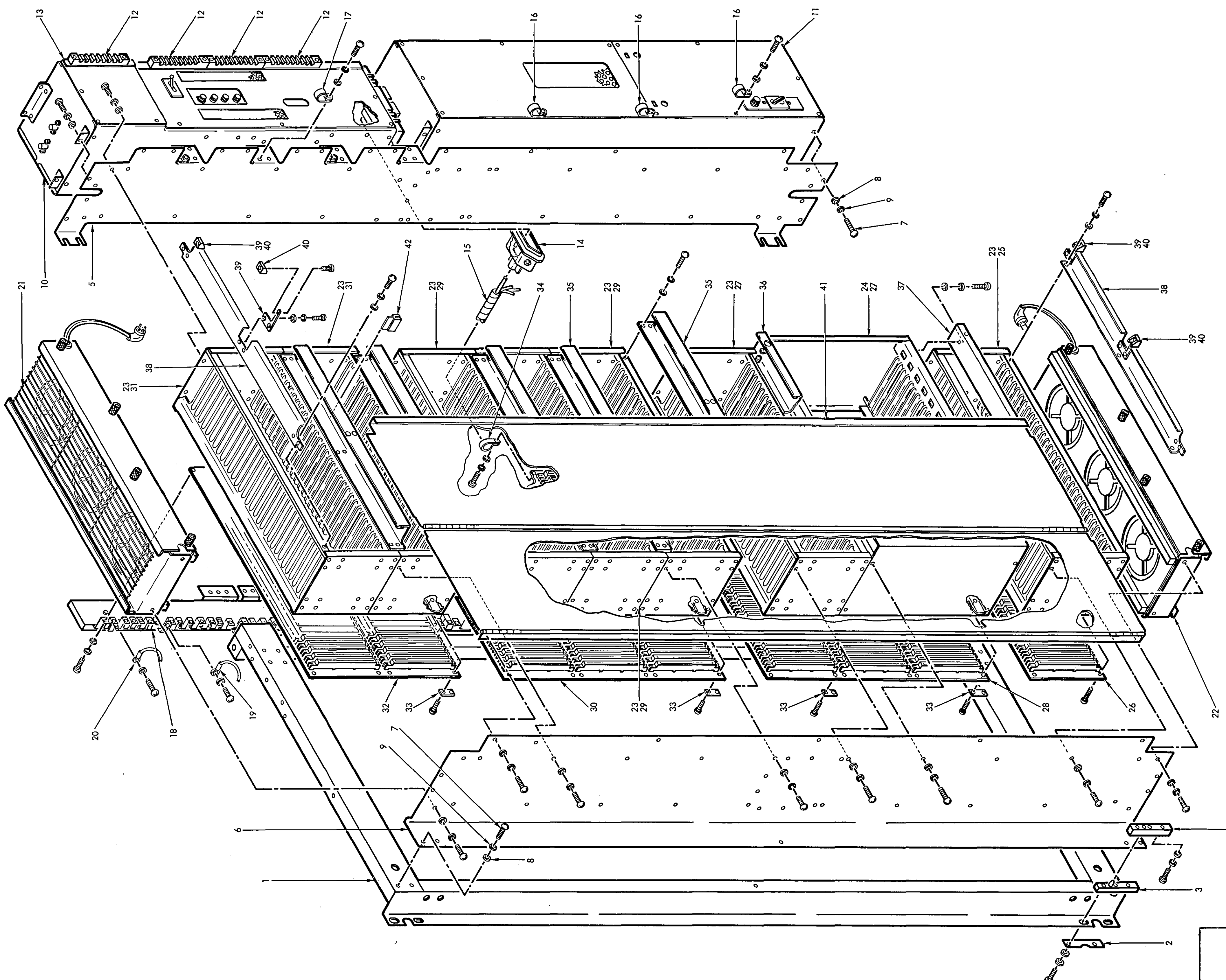

Figure A-2. Memory Frame Assembly

901586A. A2

Table A-2. Memory Frame Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-2-	117500Y		. Memory Frame Assy			8251/ 8451
-1	117319		. . Frame, Swing		1	
-2	145314		. . Cover, Shear Pin Mtg		2	
-3	139592		. . Block, Shear Pin Mtg		2	
-4	139593		. . Block, Swing Frame Stop		2	
			(Attaching Parts)			
	100012-507		. . Screw, Pan Hd Phil		8	
	100018-500		. . Washer, Flat		8	
	100024-500		. . Washer, Lock Int Tooth		8	
			- - - * - - -			
-5	124484-001		. . Bracket, Chassis Mtg		1	
			(Attaching Parts)			
	101441-001		. . Screw, Cap Hex Hd		4	
	100018-500		. . Washer, Flat		4	
	100008-500		. . Nut, Hex Mach		4	
			- - - * - - -			
-6	124742-001		. . Angle, Chassis Mtg		1	
			(Attaching Parts)			
	100012-508		. . Screw, Pan Hd Phil		5	
	100018-500		. . Washer, Flat		5	
	100024-500		. . Washer, Lock Int Tooth		5	
			- - - * - - -			
-7	100012-506		. . Screw, Pan Hd Phil		13	
-8	100018-500		. . Washer, Flat		13	
-9	100024-500		. . Washer, Lock Int Tooth		13	
-10	117264T		. . Power Supply Assy (PT16)		1	

(Continued)

Table A-2. Memory Frame Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-2-						
-11	117265X		. . Power Supply Assy (PT17)		1	
			(Attaching Parts)			
	100012-508		. . Screw, Pan Hd Phil		8	
	100018-500		. . Washer, Flat		8	
	100024-500		. . Washer, Lock Int Tooth		8	
			- - - * - - -			
-12	134447		. . Block, Cable Clamping		4	
			(Attaching Parts)			
	100012-312		. . Screw, Pan Hd Phil		8	
	100018-300		. . Washer, Flat		8	
	100024-300		. . Washer, Lock Int Tooth		8	
			- - - * - - -			
-13	134472		. . Nut, Bar		1	
			(Attaching Parts)			
	100039-306		. . Screw, Flat Hd Phil		5	
			- - - * - - -			
-14	110871		. . Connector Male, 14 Contacts (P1)		1	
-15	101625-001		. . Tubing, Spiral		A/R	
-15	100274-003		. . Tubing, Teflon		A/R	
-15	126827		. . Wire, Solid Twisted Pair		A/R	
-16	100657-009		. . Clamp, Cable Nylon		3	
-17	100657-003		. . Clamp, Cable Nylon		3	
			(Attaching Parts)			
	100012-405		. . Screw, Pan Hd Phil		6	
	100018-400		. . Washer, Flat		6	
	100024-400		. . Washer, Lock Int Tooth		6	
			- - - * - - -			

(Continued)

Table A-2. Memory Frame Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-2-						
-18	133955		. . Busbar Assy		1	
			(Attaching Parts)			
	100008-300		. . Nut, Hex Mach		56	
	100024-300		. . Washer, Lock Int Tooth		56	
			---*---			
-19	131891-001		. . Cable Assy, Busbar Pick-up		8	
-20	131891-005		. . Cable Assy, Busbar Pick-up		1	
			(Attaching Parts)			
	100008-200		. . Nut, Hex Mach		9	
	100024-200		. . Washer, Lock Int Tooth		9	
			---*---			
-21	123943K		. . Top Fan Assy		1	
			(Attaching Parts)			
	100012-306		. . Screw, Pan Hd Phil		8	
	100018-300		. . Washer, Flat		8	
	100024-300		. . Washer, Lock Int Tooth		8	
			---*---			
-22	117320U		. . Bottom Fan Assy		1	
			(Attaching Parts)			
	100012-306		. . Screw, Pan Hd Phil		8	
	100018-200		. . Washer, Flat		8	
	100024-200		. . Washer, Lock Int Tooth		8	
			---*---			
-23	116231		. . Chassis, 32 Module		7	

(Continued)

Table A-2. Memory Frame Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-2-						
-24	116444		. . Chassis, 32 Module Memory (See Fig. A-3 for Module Locations)		1	
			(Attaching Parts)			
	100012-406		. . Screw, Pan Hd Phil		32	
	100018-400		. . Washer, Flat		16	
	100024-400		. . Washer, Lock Int Tooth		32	
			- - - * - - -			
-25	117510M		. . Sense Electronics Assy		1	
-26	126502		. . . Backwiring Board Assy (Sense)		1	
-27	117520N		. . Magnetics and Drive Assy		1	
-28	126829		. . . Backwiring Board Assy (Memory)		1	
			(Attaching Parts)			
	148832-514		. . Screw, Hex Thread Forming		REF	
	100018-300		. . Washer, Flat		22	
	100024-300		. . Washer, Lock Int Tooth		22	
			- - - * - - -			
-29	117530M		. . Logic and Drive Assy		1	
-30	126830		. . . Backwiring Board Assy		1	
-31	126834P		. . Resistor and Logic Assy		1	
-32	124760		. . . Backwiring Board Assy		1	
-33	117644		. . Strap, Jumper Ground		36	
-34	100657-001		. . Clamp, Cable Nylon		1	
			(Attaching Parts)			
	148832-514		. . Screw, Hex Thread Forming		166	
			- - - * - - -			
-35	116522		. . Channel, Cable Routing		5	
-36	123940-001		. . Channel, Cable Routing		1	

(Continued)

Table A-2. Memory Frame Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-2-						
-37	123940-002		. . Channel, Cable Routing		1	
			(Attaching Parts)			
	100012-203		. . Screw, Pan Hd Phil		36	
	100018-200		. . Washer, Flat		36	
	100024-200		. . Washer, Lock Int Tooth		36	
			--- * ---			
-38	134170-001		. . Bracket, Door Latch Mtg		2	
			(Attaching Parts)			
	100012-206		. . Screw, Pan Hd Phil		6	
	100018-200		. . Washer, Flat		6	
	100024-200		. . Washer, Lock Int Tooth		6	
-39	134171		. . Spring, Door Latch		4	
			(Attaching Parts)			
	100012-306		. . Screw, Pan Hd Phil		8	
	100018-300		. . Washer, Flat		8	
	100024-300		. . Washer, Lock Int Tooth		8	
			--- * ---			
-40	129554		. . Trigger, Door Latch		4	
			(Attaching Parts)			
	100012-103		. . Screw, Pan Hd Phil		4	
			--- * ---			
-41	134169		. . Door, Chassis		1	
			(Attaching Parts)			
	100012-205		. . Screw, Pan Hd Phil		6	
	100018-200		. . Washer, Flat		6	
	100024-200		. . Washer, Lock Int Tooth		6	
			--- * ---			
-42	149850		. . Retainer (See Dwg 132546X)		6	
-	154377-001		. . Clamp, Strap Type		A/R	

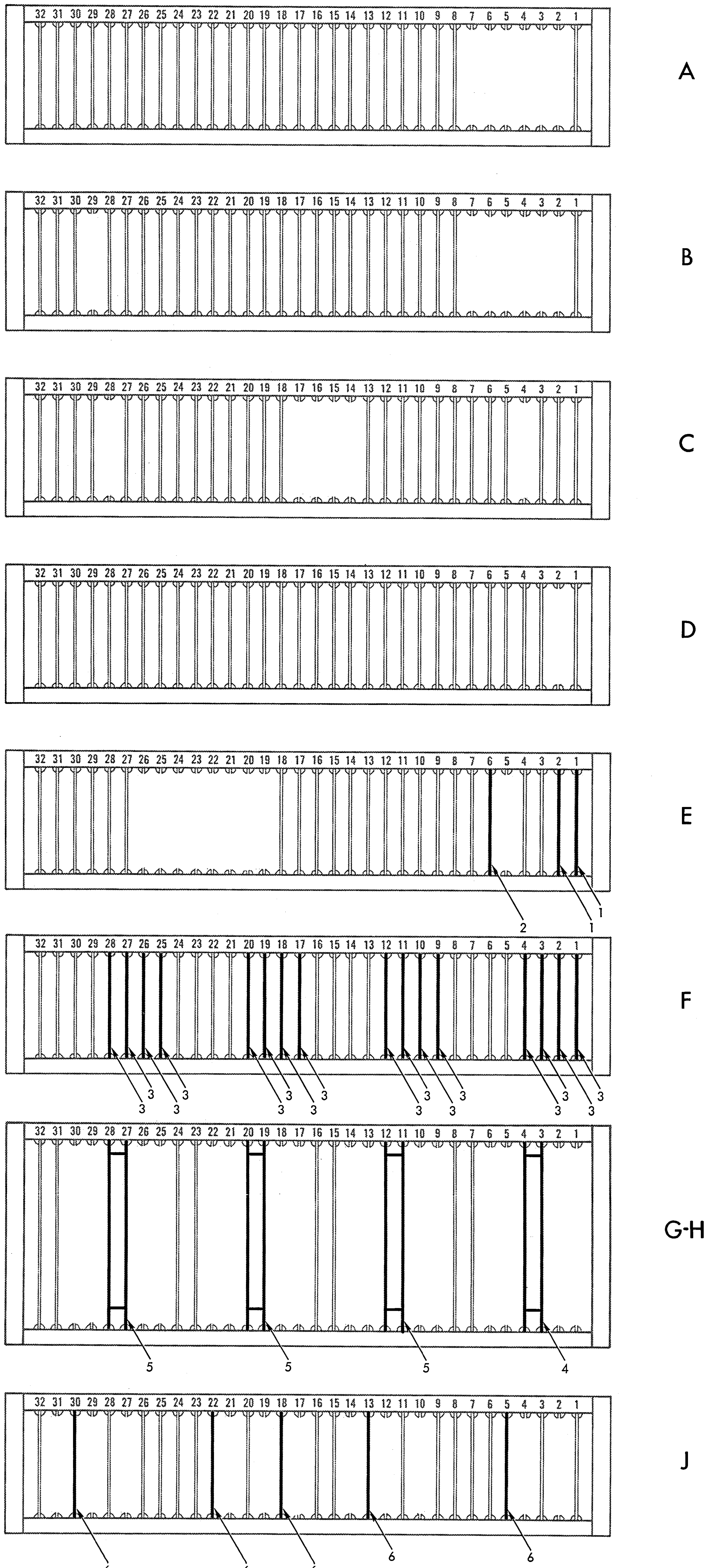

Figure A-4. 4K to 8K Memory Expansion Kit

901586A.A4

Table A-3. Module Locations, Basic 4K X 33 Bit Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-3-			Basic 4K X 33 Bit Assy (Sigma 5/7) (Module Locations)			8251/ 8451
-1	116257		. Module Assy, XT10 Term Module		16	
-2	123019		. Module Assy, AT11 Cable Dr/Rec		6	
-3	130942		. Module Assy, FT37 Buffered Latch No.2		3	
-4	125262		. Module Assy, BT16 Gated Buffer		6	
-5	130958		. Module Assy, LT34 Parity Generator		9	
-6	127393		. Module Assy, BT22 Fast Buffer		11	
-7	128190		. Module Assy, IT25 NAND Gate		2	
-8	127791		. Module Assy, XT13 Module C		9	
-9	127793		. Module Assy, XT14 Module D		1	
-10	126617		. Module Assy, IT14 Gated Inverter		6	
-11	130952		. Module Assy, FT38 Buffered Latch No.3		7	
-12	130967		. Module Assy, BT24 Buffered AND/OR Gate		3	
-13	128188		. Module Assy, IT24, NAND/NOR Gate		1	
-14	125264		. Module Assy, IT16, Gated Inverter		3	
-15	133053		. Module Assy, AT31 Cable Dr/Rec		1	
-16	126615		. Module Assy, LT21 Logic Element W/Buff		5	
-17	124717		. Module Assy, LT20 Logic Element W/Inv		1	
-18	123008		. Module Assy, ST14 Toggle Switch Module		2	
-19	126963		. Module Assy, DT11 Delay Line		2	
-20	127391		. Module Assy, HT15 Delay Line Sensor		3	
-21	123915		. Module Assy, LT19 Logic Element		1	
-22	123018		. Module Assy, AT10 Cable Receiver		1	
-23	130447		. Module Assy, BT25 BAND Gate		1	
-24	126611		. Module Assy, AT16 Rejection Gate		2	
-25	123005		. Module Assy, ST10 Memory Switch A		10	
-26	132159		. Module Assy, ST22 Memory Driver		4	

(Continued)

Table A-3. Module Locations, Basic 4K X 33 Bit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-3-						
-27	132153		. Module Assy, ST21 Inhibit Driver		6	
-28	123006		. Module Assy, ST11 Memory Switch B		16	
-29	111550		. Core Diode Module Assy (9 Bit)		1	
-30	111549		. Core Diode Module Assy (8 Bit)		3	
-31	131292		. Module Assy, ST17 Voltage Regulator		1	
-32	131633		. Module Assy, HT26 Memory Pre-Amplifier		6	
-33	123010		. Module Assy, HT11 Memory Sense Amplifier		6	
-34	130902		. Module Assy, ST34 Strobe Generator		2	
-35	123012		. Module Assy, ST15 Memory Pre-Amp Selector		1	
-36	137481-171		. Interframe Ribbon Cable Assy (Loc 10B to 10C, 30B to 30C, 31B to 31C) preassigned locations in the center frame are reserved for modules for the following optional features:		3	
	117638*		. 4K to 8K Memory Expan Kit (See Fig. A-4)		A/R	8252/ 8452
	117639*		. 8K to 12K Memory Expan Kit (See Fig. A-5)		A/R	8252/ 8452
	117640*		. 12K to 16K Memory Expan Kit (See Fig. A-6)		A/R	8252/ 8452
	129463†		. Port Expan Assy 1x2 (Port B) (See Fig. A-7)		A/R	8255/ 8455
	128125		. Port Expan Assy 2x3 (Port A) (See Fig. A-8)		A/R	8256/ 8456
			*Each 4K increment consists of modules inserted in the basic 4K memory, to a maximum of 16K			
			†Port B is standard with Sigma 7			

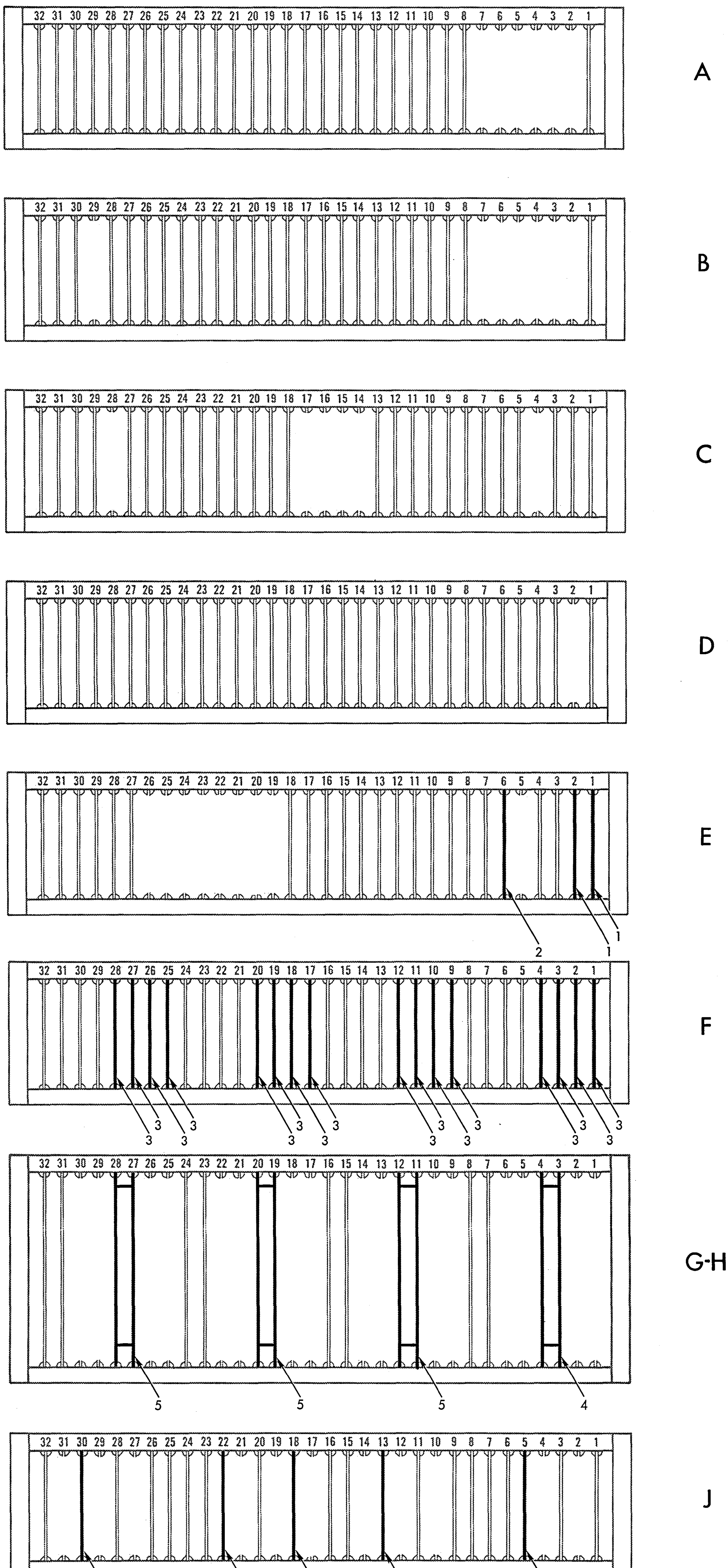

Figure A-4. 4K to 8K Memory Expansion Kit

901586A. A4

Table A-4. 4K to 8K Memory Expansion Kit

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-4-	117638B		4K to 8K Memory Expansion Kit		1	8252/ 8452
-1	123005		. Module Assy, ST10 Memory Switch A		2	
-2	132159		. Module Assy, ST22 Memory Driver		1	
-3	123006		. Module Assy, ST11 Memory Switch B		16	
-4	111550		. Core Diode Module Assy (9-Bit)		1	
-5	111549		. Core Diode Module Assy (8-Bit)		3	
-6	131633		. Module Assy, HT26 Memory Pre-Amp			
-	132546		Prerequisite: Basic 4K X 33 Bit Assy		1	8251/ 8451

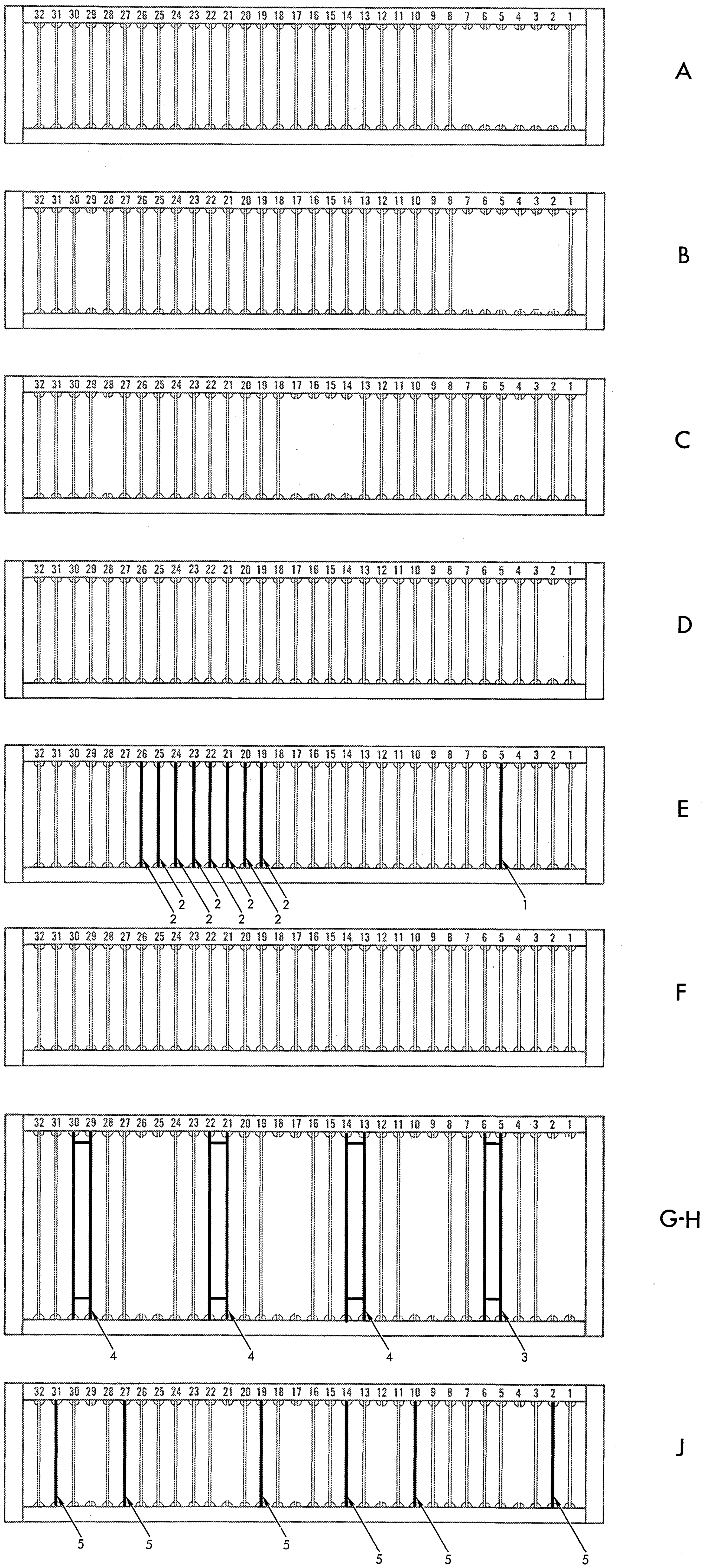

Figure A-5. 8K to 12K Memory Expansion Kit

901586A.A5

Table A-5. 8K to 12K Memory Expansion Kit

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-5-	117639B		8K to 12K Memory Expansion Kit		1	8252/ 8452
-1	132159		. Module Assy, ST22 Memory Driver		1	
-2	123005		. Module Assy, ST10 Memory Switch A		8	
-3	111550		. Core Diode Module Assy (9-Bit)		1	
-4	111549		. Core Diode Module Assy (8-Bit)		3	
-5	131633		. Module Assy, HT26 Memory Pre-Amp		6	
			Prerequisite:			
-	117638B		4K to 8K Memory Expansion Kit		1	8252/ 8452

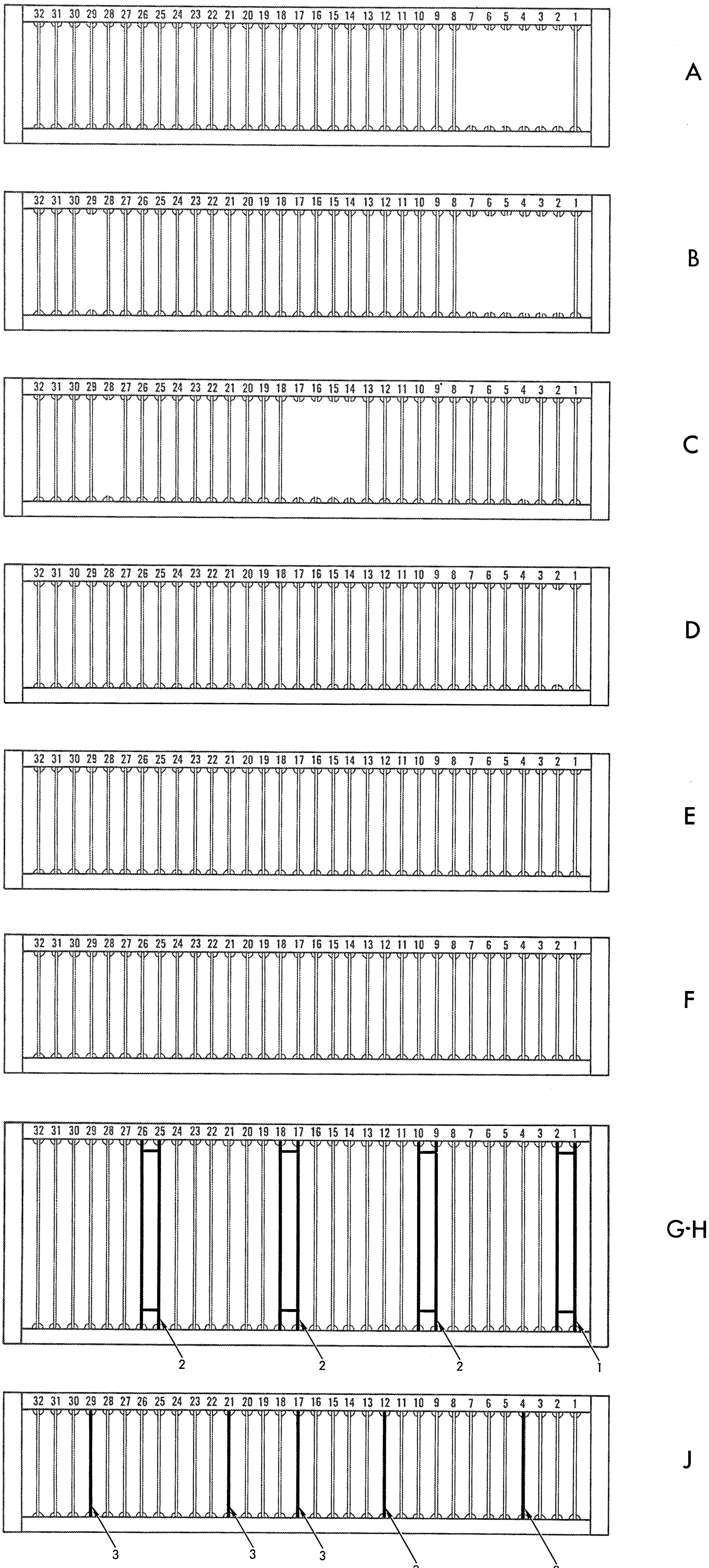

Figure A-6. 12K to 16K Memory Expansion Kit

901586A.A6

Table A-6. 12K to 16K Memory Expansion Kit

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-6-	117640		12K to 16K Memory Expansion Kit		1	8252/ 8452
-1	111550		. Core Diode Module Assy (9-Bit)		1	
-2	111549		. Core Diode Module Assy (8-Bit)		3	
-3	131633		. Module Assy, HT26 Memory Pre-Amp		5	
			Prerequisite:			
-	117638B		4K to 8K Memory Expansion Kit		1	8252/ 8452
-	117639B		8K to 12K Memory Expansion Kit		1	8252/ 8452

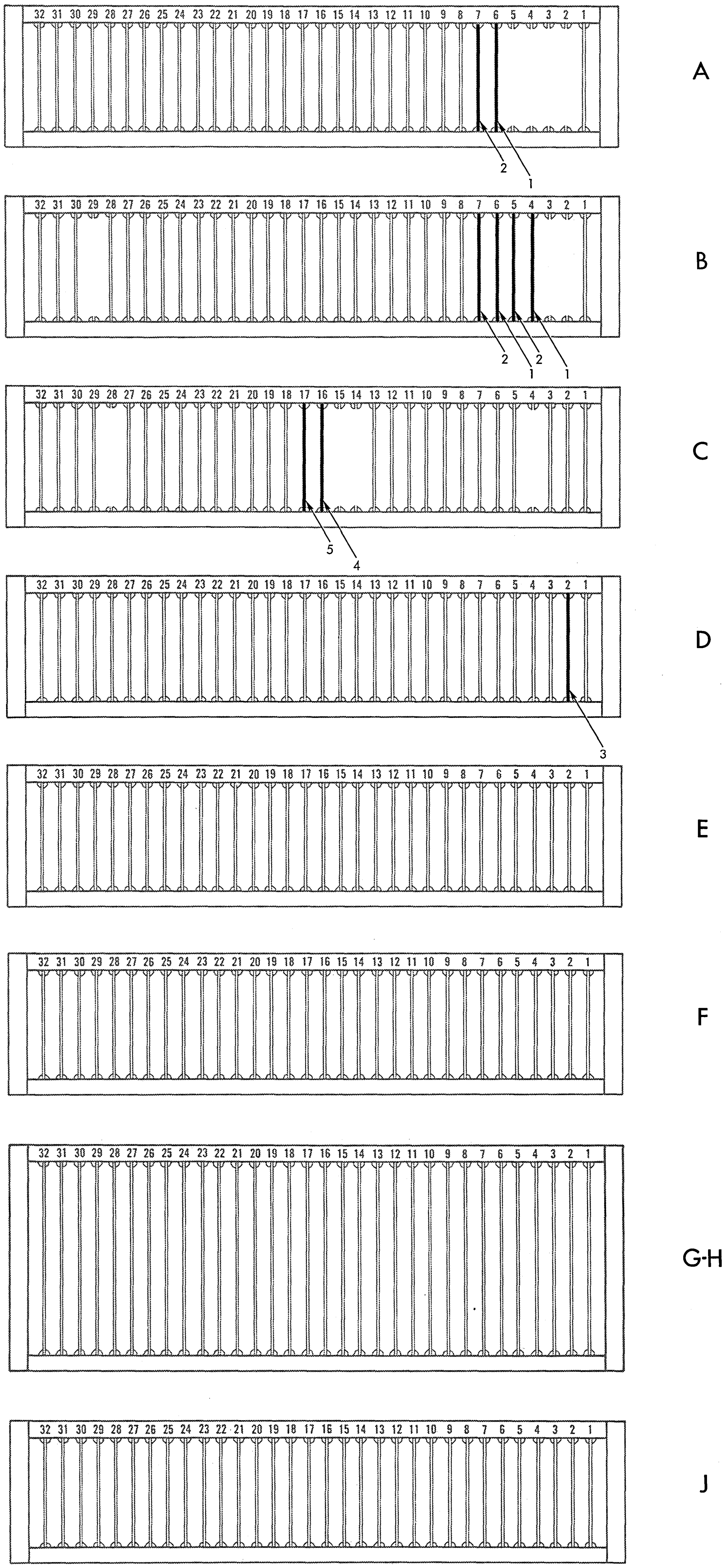

Figure A-7. Port Expansion Assembly, 1x2 (Port B)

901586A.A7

Table A-7. Port Expansion Assembly, 1 X 2 (Port B)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-7-	129463C*		. Port Expansion Assy, 1x2 (Port B)		1	8255/ 8455
-1	123019		. . Module Assy, AT11 Cable Dr/Rec Loc 2A, 4A, 2B		3	
-2	130942		. . Module Assy, FT37 Buffered Latch No.2A Loc 3A, 5A, 3B		3	
-3	126615		. . Module Assy, LT21 Logic Element W/Buff Loc 16C		1	
-4	124717		. . Module Assy, LT20 Logic Element W/Inv Loc 17C		1	
-5	123018		. . Module Assy, AT10 Cable Receiver Loc 2D		1	
			*Port B is standard with the Sigma 7			

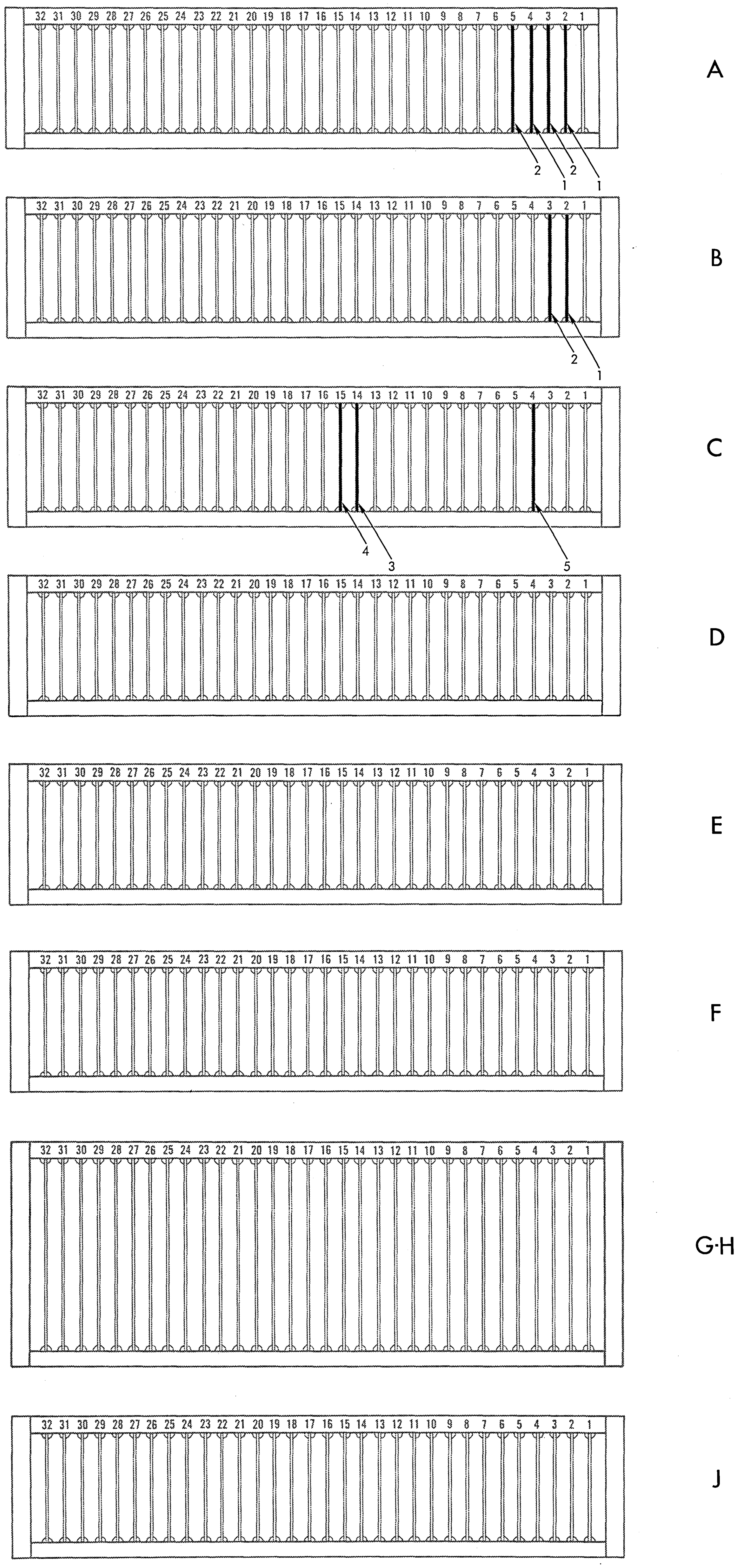

Figure A-8. Port Expansion Assembly, 2x3 (Port A)

901586A.A8

Table A-8. Port Expansion Assembly, 2 X 3 (Port A)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-8-	128125C		. Port Expansion Assy, 2x3 (Port A)		1	8256/ 8456
-1	123019		. . Module Assy, AT11 Cable Dr/Rec Loc 6A, 4B, 6B		3	
-2	130942		. . Module Assy, FT37 Buffered Latch No.2A Loc 7A, 5B, 7B		3	
-3	123018		. . Module Assy, AT10 Cable Receiver Loc 4C		1	
-4	126615		. . Module Assy, LT21 Logic Element Loc 14C		1	
-5	124717		. . Module Assy, LT20 Logic Element Loc 15C		1	

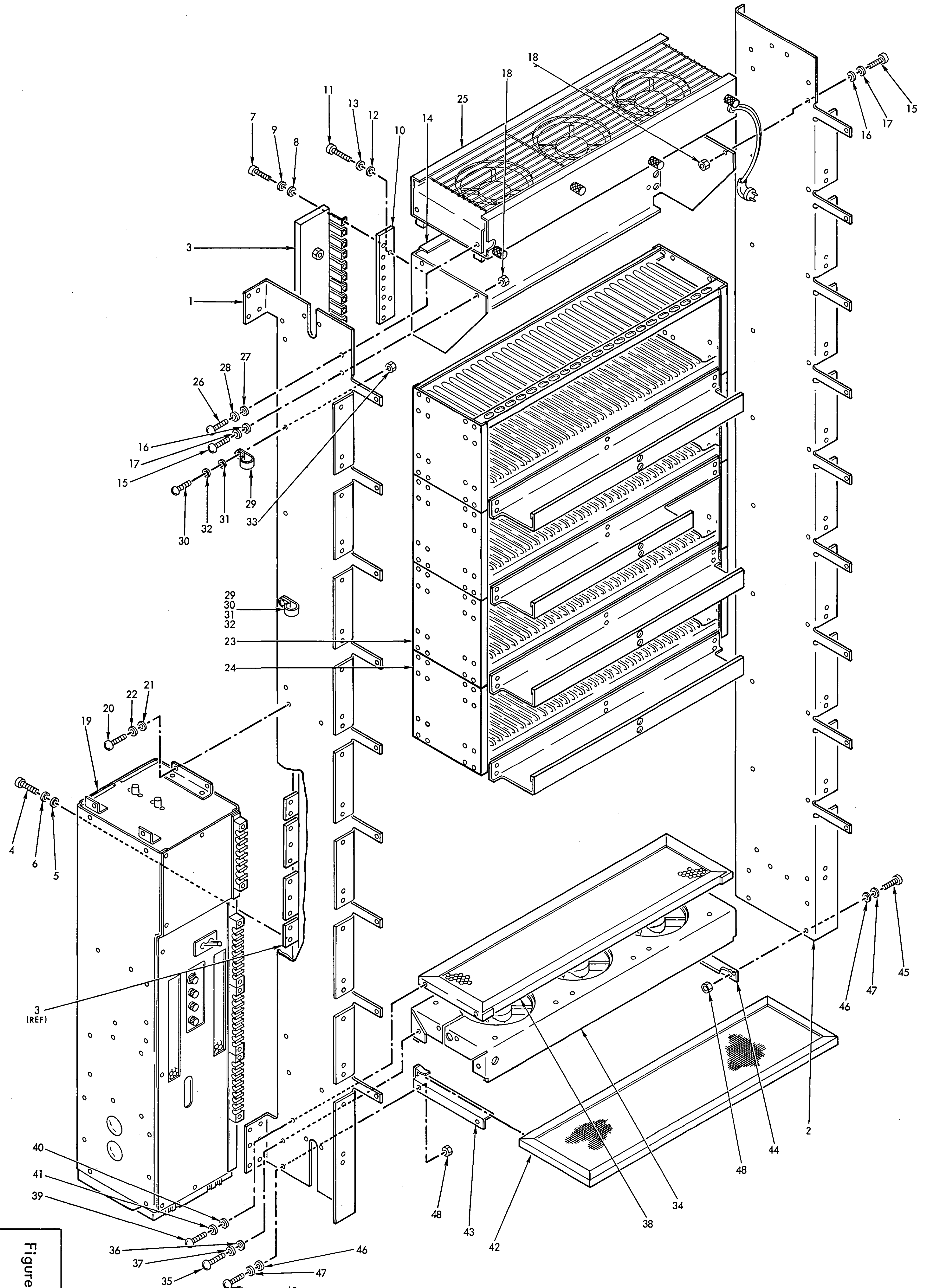

Figure A-9. Fixed, Accessory Frame Assembly

901586A.A9

Table A-9. Fixed, Accessory Frame Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-9-	136978F		. Fixed, Accessory Frame Assy		1	8257/ 8457
-1	136979		. . Bracket, Chassis Mtg LH		1	
-2	136980		. . Bracket, Chassis Mtg RH		1	
-3	134196		. . Busbar Port Expander Assy		1	
			(Attaching Parts)			
-4	100012-500		. . Screw, Pan Hd Phil		10	
-5	100018-500		. . Washer, Flat		10	
-6	100024-500		. . Washer, Lock Int Tooth		10	
			- - - * - - -			
-7	100012-306		. . Screw, Pan Hd Phil		8	
-8	100018-300		. . Washer, Flat		8	
-9	100024-300		. . Washer, Lock Int Tooth		8	
-10	129693		. . Strip, Insulating		1	
			(Attaching Parts)			
-11	100012-306		. . Screw, Pan Hd Phil		2	
-12	100018-300		. . Washer, Flat		2	
-13	100024-300		. . Washer, Lock Int Tooth		2	
			- - - * - - -			
-14	129694		. . Panel, Blank Board Simulator		1	
			(Attaching Parts)			
-15	100012-410		. . Screw, Pan Hd Phil		4	
-16	100018-400		. . Washer, Flat		4	
-17	100024-400		. . Washer, Lock Int Tooth		4	
-18	100008-400		. . Nut, Hex Mach		4	
			- - - * - - -			

(Continued)

Table A-9. Fixed, Accessory Frame Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-9-						
-19	117264S		. . Power Supply Assy (PT16)		1	
			(Attaching Parts)			
-20	100012-505		. . Screw, Pan Hd Phil		4	
-21	100018-500		. . Washer, Flat		4	
-22	100024-500		. . Washer, Lock Int Tooth		4	
			- - - * - - -			
-23	130625J		. Memory Port Expansion F Assy (See Fig.A-10)		REF	
-24	130626H		. Memory Port Expansion S Assy (See Fig.A-11)		REF	
-25	123943K		. . Top Fan Assy		1	
			(Attaching Parts)			
-26	100012-306		. . Screw, Pan Hd Phil		8	
-27	100018-300		. . Washer, Flat		8	
-28	100024-300		. . Washer, Lock Int Tooth		8	
			- - - * - - -			
-29	100657-004		. . Clamp, Cable Nylon		2	
			(Attaching Parts)			
-30	100012-408		. . Screw, Pan Hd Phil		2	
-31	100018-400		. . Washer, Flat		2	
-32	100024-400		. . Washer, Lock Int Tooth		2	
-33	100008-400		. . Nut, Hex Mach		2	
			- - - * - - -			
-34	134861		. . Auxiliary Fan Assy		1	
			(Attaching Parts)			
-35	100012-206		. . Screw, Pan Hd Phil		8	
-36	100018-200		. . Washer, Flat		8	
-37	100024-200		. . Washer, Lock Int Tooth		8	
			- - - * - - -			

(Continued)

Table A-9. Fixed, Accessory Frame Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-9-						
-38	134239		. . Cover, Fan-Channel Mtg		1	
			(Attaching Parts)			
-39	100012-408		. . Screw, Pan Hd Phil		4	
-40	100018-400		. . Washer, Flat		4	
-41	100024-400		. . Washer, Lock Int Tooth		4	
			---*---			
-42	117427		. . Filter, Air Panel		1	
-43	134826-001		. . Bracket, Filter LH		1	
-44	134826-002		. . Bracket, Filter RH		1	
			(Attaching Parts)			
-45	100012-306		. . Screw, Pan Hd Phil		4	
-46	100018-400		. . Washer, Flat		4	
-47	100024-300		. . Washer, Lock Int Tooth		4	
-48	100008-300		. . Nut, Hex Mach		4	
			---*---			
-	154377-001		. . Clamp, Strap Type		A/R	

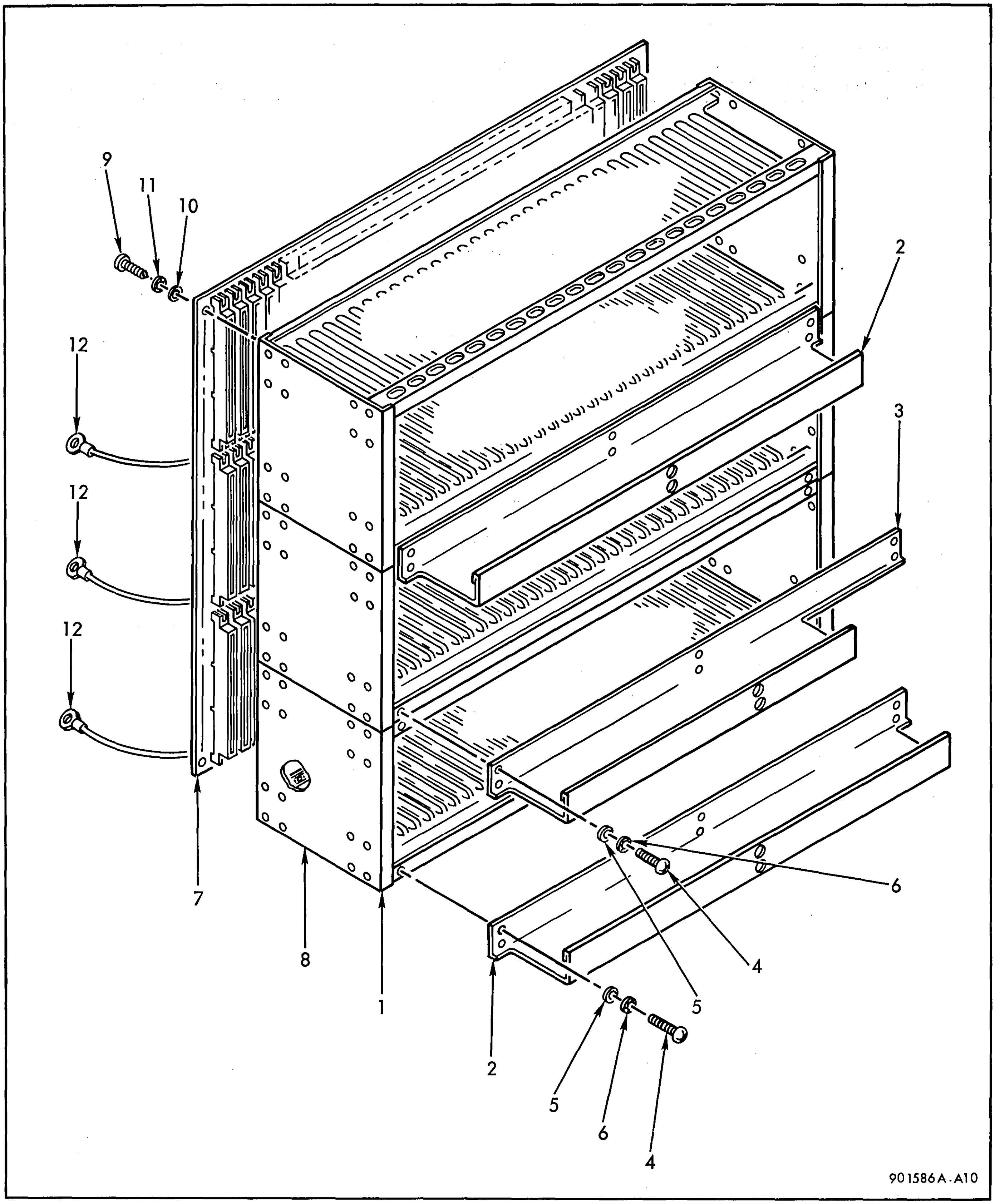

Figure A-10. Memory Port Expander F Assembly

Table A-10. Memory Port Expander F Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-10-	130625J		Memory Port Expansion F Assy		REF	8257/ 8457
A-10-	136992C		. Memory Port Expander F Assy		1	
-1	116231		. . Chassis, 32 Module (See Fig. A-12 for Module locations)		3	
-2	132197		. . Channel, Cable Routing		2	
-3	136132		. . Channel, Cable Routing		1	
			(Attaching Parts)			
-4	100012-203		. . Screw, Pan Hd		15	
-5	100018-200		. . Washer, Flat		15	
-6	100024-200		. . Washer, Lock Int Tooth		15	
			- - - * - - -			
-7	133623		. . Port Expander F Assy		1	
-7	124725		. . . Backwiring Board Assy (3 High)		1	
-8	129567-001		. . Nut, Strip Speed		6	
			(Attaching Parts)			
-9	114538-213		. . Screw, Sheet Metal		54	
-10	100018-300		. . Washer, Flat		54	
-11	100024-300		. . Washer, Lock Int Tooth		54	
			- - - * - - -			
-12	131891-001		. . Cable Assy, Busbar Pick-Up		3	

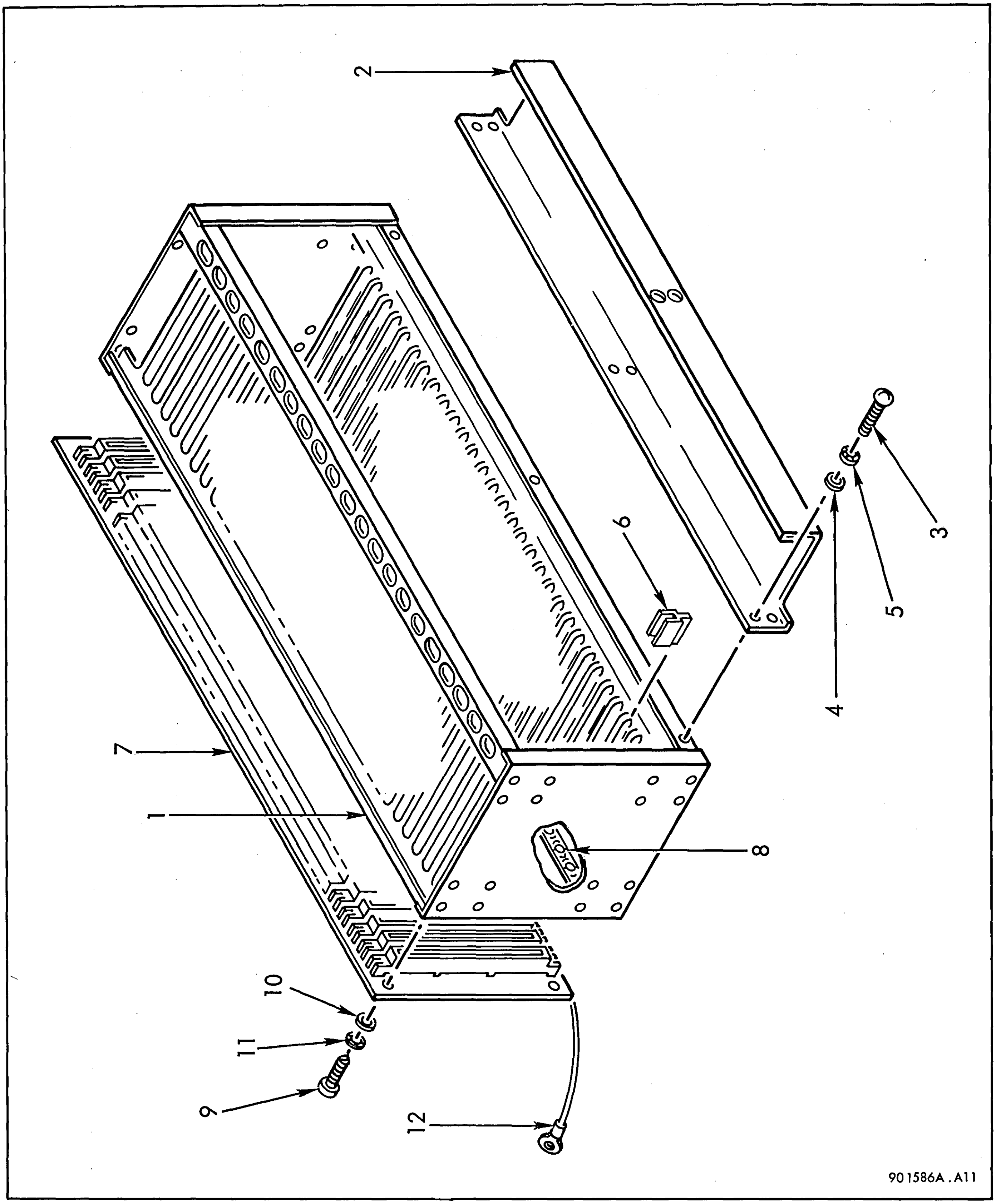

Figure A-11. Memory Port Expander S Assembly

Table A-11. Memory Port Expander S Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-11-	130626H		Memory Port Expansion S Assy		REF	8257/ 8457
A-11-	133651E		. Memory Port Expander S Assy		1	
-1	116231		. . Chassis, 32 Module (See Fig. A-13 for Module Locations)		1	
-2	132197		. . Channel, Cable Routing		1	
			(Attaching Parts)			
-3	100012-203		. . Screw, Pan Hd		3	
-4	100018-200		. . Washer, Flat		3	
-5	100024-200		. . Washer, Lock Int Tooth		3	
			- - - * - - -			
-6	149850		. . Retainer (See Dwg 130626H)		4	
-7	133645		. . Port Expander S Assy		1	
-7	126502		. . . Backwiring Board Assy (1 High)		1	
-8	129567		. . Nut, Strip Speed		2	
			(Attaching Parts)			
-9	114538-214		. . Screw, Sheet Metal		18	
-10	100018-300		. . Washer, Flat		18	
-11	100024-300		. . Washer, Lock Int Tooth		18	
			- - - * - - -			
-12	131891-001		. . Cable Assy, Busbar Pick-Up		1	

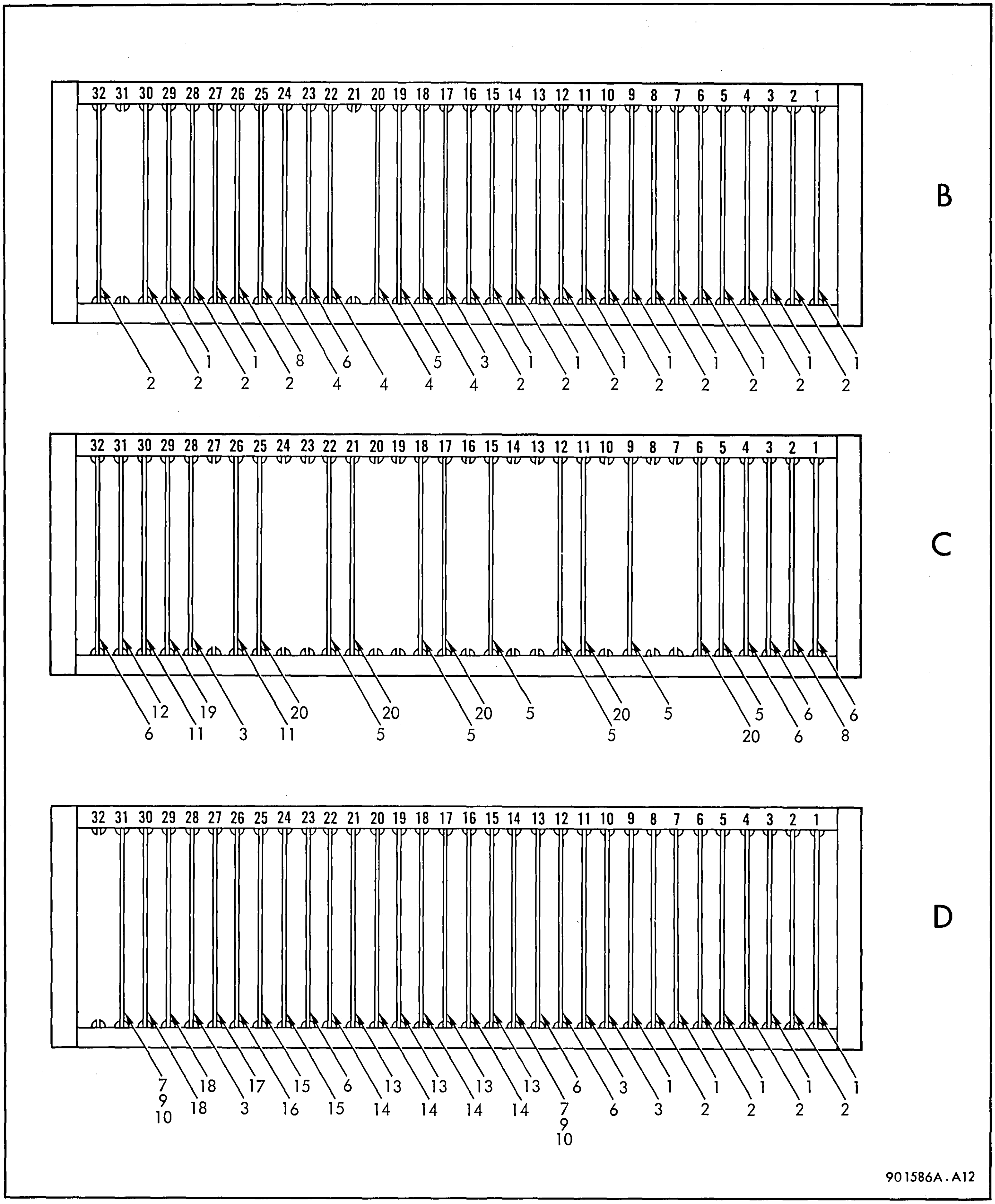

Figure A-12. Module Locations, Memory Port Expander F Assembly

Table A-12. Module Locations, Memory Port Expander F Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-12-			Memory Port Expander F Assy (Module Locations)			8257/ 8457
-1	130942		. Module Assy, FT37 Buffered Latch No. 2A		14	
-2	123019		. Module Assy, AT11 Cable Dr/Rec		16	
-3	125264		. Module Assy, IT16 Gated Inverter		6	
-4	123018		. Module Assy, AT10 Cable Receiver		4	
-5	130952		. Module Assy, FT38 Buffered Latch No. 3		7	
-6	116257		. Module Assy, XT10 Terminator Module		6	
-7	116257		. Module Assy, XT10 Term Module Loc 14D 31D (For Port Expander F-Without S-in Sigma 7)		2	8457
-8	116257		. Module Assy, XT10 Term Module Loc 25C C2 (When Adding Port Expander S to F in Sigma 7 Modules, XT10 Are Removed from Loc 14D 31D and Are Inserted in Loc 25B C2)		2	8457
-9	133212-171		. Module Assy, ZT45 Ribbon Cable		2	8457
-9	137481-171		. Interframe, Ribbon Cable Assy Loc 14D 31D (For Port Expander F and S combined in Sigma 7)		REF	
-10	132277		. Module Assy, ZT35 Ribbon Cable Loc 14D 31D (Used in Sigma 5 only)		2	8257
-11	127393		. Module Assy, BT22 Fast Buffer		2	
-12	126856		. Module Assy, FT26 Buff Latch No. 3		1	
-13	126615		. Module Assy, LT21 Logic Element W/Buffer		4	
-14	124717		. Module Assy, LT20 Logic Element W/Inverter		4	
-15	123008		. Module Assy, ST14 Address Selector		2	
-16	117375		. Module Assy, IT15 Gated Inverter		1	
-17	117389		. Module Assy, BT15 Gated Buffer		1	
-18	126611		. Module Assy, AT16 Rejection Gate		2	
-19	130967		. Module Assy, BT24 Buffered AND/OR Gate		1	

(Continued)

Table A-12. Module Locations, Memory Port Expander F Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
			Port Expander F to Memory Cable Interconnections:			
-20	133763-201		. Cable Plug Module Assy (P252-P253)		2	
-20	133763-301		. Cable Plug Module Assy (P252-P253)		2	
-20	133763-401		. Cable Plug Module Assy (P252-P253)		1	
-20	133625		. . Printed Wiring Board Assy, Twisted Pair Cable (ZT38) (Loc 6C 11C 17C 21C 25C)		10	

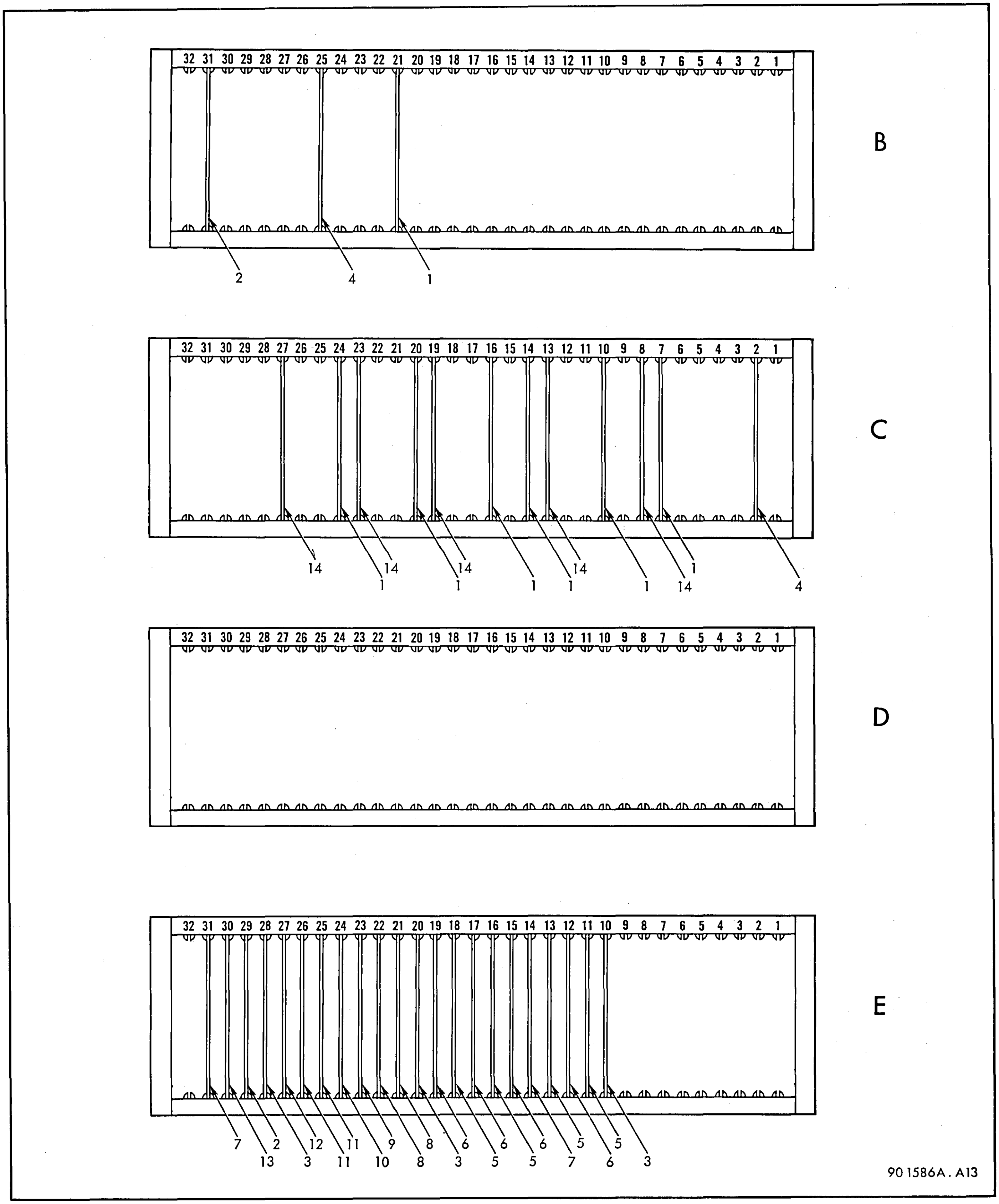

Figure A-13. Module Locations, Memory Port Expander S Assembly

Table A-13. Module Locations, Memory Port Expander S Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
A-13-			Memory Port Expander S Assy (Module Locations)			8257/ 8457
-1	130952		. Module Assy, FT38 Buff Latch No.3 (Loc 21B 7C 10C 14C 16C 20C 24C)		7	
-2	127393		. Module Assy, BT22 Fast Buffer (Loc 31B 29E)		2	
-3	116257		. Module Assy, XT10 Term Module		3	
-4	116257		. Module Assy, XT10 Term Module (Loc 25B 2C) (When Port Expander S Is Added to F in Sigma 7, Two XT10 Modules Are Removed from Loc 14D 31D and Are Inserted into Loc 25B 2C)		REF	8457
-5	126615		. Module Assy, LT21 Logic Element W/Buffer		4	
-6	124717		. Module Assy, LT20 Logic Element W/Inverter		4	
-7	137481-171		. Interframe Ribbon Cable Assy		2	8457
-7	133212-171		. Module Assy, ZT45 Ribbon Cable (Loc 14E 31E) (Used in Sigma 7 only, Blank for Sigma 5)		REF	
-8	123008		. Module Assy, ST14 Address Selector		2	
-9	117389		. Module Assy, BT15 Gated Buffer		1	
-10	125264		. Module Assy, IT16 Gated Inverter		1	
-11	126611		. Module Assy, AT16 Rejection Gate		2	
-12	117375		. Module Assy, IT15 Gated Buffer		1	
-13	130967		. Module Assy, BT24 Buffered AND/OR Gate		1	
			Port Expander S to Memory Cable Interconnections:			
-14	133763-001		. Cable Plug Module Assy (P252-P253)		3	
-14	133763-651		. Cable Plug Module Assy (P252-P253)		2	
-14	133625		. Printed Wiring Board Assy, Twisted Pair Cable (ZT38) (Loc 8C 13C 19C 23C 27C)		2	

Table A-14. Numerical Index

Fig. & Index No.	XDS Part Number	Description
A-14-	100008-200	Nut, Hex Mach
9-48	100008-300	Nut, Hex Mach
9-18	100008-400	Nut, Hex Mach
9-33	100008-400	Nut, Hex Mach
	100008-500	Nut, Hex Mach
	1000012-103	Screw, Pan Hd Phil
10-4	1000012-203	Screw, Pan Hd Phil
11-3	100012-203	Screw, Pan Hd Phil
	100012-205	Screw, Pan Hd Phil
9-7	100012-306	Screw, Pan Hd Phil
9-26	100012-306	Screw, Pan Hd Phil
9-26	100012-306	Screw, Pan Hd Phil
9-45	100012-306	Screw, Pan Hd Phil
	100012-312	Screw, Pan Hd Phil
	100012-405	Screw, Pan Hd Phil
	100012-406	Screw, Pan Hd Phil
9-30	100012-408	Screw, Pan Hd Phil
9-39	100012-408	Screw, Pan Hd Phil
9-15	100012-410	Screw, Pan Hd Phil
9-4	100012-500	Screw, Pan Hd Phil
9-20	100012-505	Screw, Pan Hd Phil
2-7	100012-506	Screw, Pan Hd Phil
	100012-507	Screw, Pan Hd Phil
	100012-508	Screw, Pan Hd Phil
9-36	100018-200	Washer, Flat
10-5	100018-200	Washer, Flat
11-4	100018-200	Washer, Flat

Fig. & Index No.	XDS Part Number	Description
9-8	100018-300	Washer, Flat
9-27	100018-300	Washer, Flat
10-10	100018-300	Washer, Flat
11-10	100018-300	Washer, Flat
9-16	100018-400	Washer, Flat
9-31	100018-400	Washer, Flat
9-40	100018-400	Washer, Flat
9-46	100018-400	Washer, Flat
2-8	100018-500	Washer, Flat
9-5	100018-500	Washer, Flat
9-21	100018-500	Washer, Flat
9-37	100024-200	Washer, Lock Int Tooth
10-6	100024-200	Washer, Lock Int Tooth
11-5	100024-200	Washer, Lock Int Tooth
9-28	100024-300	Washer, Lock Int Tooth
9-47	100024-300	Washer, Lock Int Tooth
10-11	100024-300	Washer, Lock Int Tooth
11-11	100024-300	Washer, Lock Int Tooth
9-6	100024-400	Washer, Lock Int Tooth
9-17	100024-400	Washer, Lock Int Tooth
9-32	100024-400	Washer, Lock Int Tooth
9-41	100024-400	Washer, Lock Int Tooth
2-9	100024-500	Washer, Lock Int Tooth
9-6	100024-500	Washer, Lock Int Tooth
9-22	100024-500	Washer, Lock Int Tooth
	100039-306	Screw, Flat Hd Phil
2-15	100274-003	Tubing, Teflon

(Continued)

Table A-14. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
A-14-		
2-34	100657-001	Clamp, Cable Nylon
2-17	100657-003	Clamp, Cable Nylon
9-29	100657-004	Clamp, Cable Nylon
2-16	100657-009	Clamp, Cable Nylon
2-	101441-001	Screw, Cap Hex Hd
2-15	101625-001	Tubing, Spiral
2-14	110871	Connector, Male 14 Contacts (P1)
3-30	111549	Core Diode Module Assy (8-Bit)
4-5	111549	Core Diode Module Assy (8-Bit)
5-4	111549	Core Diode Module Assy (8-Bit)
6-2	111549	Core Diode Module Assy (8-Bit)
3-29	111550	Core Diode Module Assy (9-Bit)
4-4	111550	Core Diode Module Assy (9-Bit)
5-3	111550	Core Diode Module Assy (9-Bit)
6-1	111550	Core Diode Module Assy (9-Bit)
10-9	114538-213	Screw, Sheet Metal
11-9	114538-214	Screw, Sheet Metal
2-23	116231	Chassis, 32 Module
10-1	116231	Chassis, 32 Module
11-1	116231	Chassis, 32 Module
3-1	116257	Module Assy, XT10 Term Module
12-6	116257	Module Assy, XT10 Term Module
12-7	116257	Module Assy, XT10 Term Module
12-8	116257	Module Assy, XT10 Term Module
13-3	116257	Module Assy, XT10 Term Module
13-4	116257	Module Assy, XT10 Term Module
2-24	116444	Chassis, 32 Module Memory
2-35	116522	Channel, Cable Routing
9-19	117264T	Power Supply Assy (PT16)
2-10	117264T	Power Supply Assy (PT16)
2-11	117265X	Power Supply Assy (PT17)
2-1	117319	Frame, Swing
2-22	117320U	Bottom Fan Assy
12-16	117375	Module Assy, IT15 Gated Inverter
13-12	117375	Module Assy, IT15 Gated Inverter
12-17	117389	Module Assy, BT15 Gated Buffer
13-9	117389	Module Assy, BT15 Gated Buffer
9-42	117427	Filter, Air Panel
1-2	117500Y	Memory Frame Assy
1-3	117500Y	Memory Frame Assy
2-	117500Y	Memory Frame Assy
2-25	117510M	Sense Electronics Assy
2-27	117520N	Magnetics & Drive Assy

(Continued)

Table A-14. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
A-14-		
2-29	117530M	Logic & Drive Assy
3-	117638B	4K to 8K Expan Kit
4-	117638B	4K to 8K Expan Kit
5-	117638B	4K to 8K Expan Kit
6-	117638B	4K to 8K Expan Kit
3-	117639B	8K to 12K Expan Kit
5-	117639B	8K to 12K Expan Kit
6-	117639B	8K to 12K Expan Kit
3-	117640C	12K to 16K Expan Kit
6-	117640C	12K to 16K Expan Kit
2-33	117644	Strap, Jumper Ground
3-25	123005	Module Assy, ST10 Memory Switch A
4-1	123005	Module Assy, ST10 Memory Switch A
5-2	123005	Module Assy, ST10 Memory Switch A
3-28	123006	Module Assy, ST11 Memory Switch B
4-3	123006	Module Assy, ST11 Memory Switch B
3-18	123008	Module Assy, ST14 Toggle Switch Module
12-15	123008	Module Assy, ST14 Toggle Switch Module
13-8	123008	Module Assy, ST14 Toggle Switch Module
3-33	123010	Module Assy, HT11 Memory Sense Amp
3-35	123012	Module Assy, ST15 Memory Pre-Amp Select

Fig. & Index No.	XDS Part Number	Description
3-22	123018	Module Assy, AT10 Cable Receiver
7-3	123018	Module Assy, AT10 Cable Receiver
8-5	123018	Module Assy, AT10 Cable Receiver
12-4	123018	Module Assy, AT10 Cable Receiver
3-2	123019	Module Assy, XT10 Term Module
7-1	123019	Module Assy, XT10 Term Module
8-1	123019	Module Assy, XT10 Term Module
12-2	123019	Module Assy, XT10 Term Module
3-21	123915	Module Assy, LT19 Logic Element
2-36	123940-001	Channel, Cable Routing
2-37	123940-002	Channel, Cable Routing
2-21	123943K	Top Fan Assy
9-25	123943K	Top Fan Assy
2-5	124484-001	Bracket, Chassis Mtg
3-17	124717	Module Assy, LT20 Logic Element W/Inv
7-5	124717	Module Assy, LT20 Logic Element W/Inv
8-4	124717	Module Assy, LT20 Logic Element W/Inv
13-6	124717	Module Assy, LT20 Logic Element W/Inv
10-7	124725	Backwiring Board Assy
2-6	124742-001	Angle Chassis Mtg
2-32	124760	Backwiring Board Assy

(Continued)

Table A-14. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
A-14-		
3-4	125262	Module Assy, BT16 Gated Buffer
3-14	125264	Module Assy, IT16 Gated Inverter
12-3	125264	Module Assy, IT16 Gated Inverter
13-10	125264	Module Assy, IT16 Gated Inverter
2-26	126502	Backwiring Board Assy (1 High)
11-7	126502	Backwiring Board Assy (1 High)
3-24	126611	Module Assy, AT16 Rejection Gate
12-18	126611	Module Assy, AT16 Rejection Gate
3-16	126615	Module Assy, LT21 Logic Element W/Buff
7-4	126615	Module Assy, LT21 Logic Element W/Buff
8-3	126615	Module Assy, LT21 Logic Element W/Buff
12-13	126615	Module Assy, LT21 Logic Element W/Buff
13-5	126615	Module Assy, LT21 Logic Element W/Buff
3-10	126617	Module Assy, IT14 Gated Inverter
2-15	126827	Wire, Solid Twisted Pair
2-28	126829	Backwiring Board Assy (Memory)
2-30	126830	Backwiring Board Assy
2-31	126834P	Resistor & Logic Assy

Fig. & Index No.	XDS Part Number	Description
12-13	126856	Module Assy, FT26 Buffered Latch No 3
3-19	126963	Module Assy, DT11 Delay Line
3-20	127391	Module Assy, HT15 Delay Line Sensor
3-6	127393	Module Assy, BT22 Fast Buffer
12-11	127393	Module Assy, BT22 Fast Buffer
13-2	127393	Module Assy, BT22 Fast Buffer
1-	127409	Instl Dwg (Ref Only)
3-8	127791	Module Assy, XT13 Module C
3-9	127793	Module Assy, XT14 Module D
8-	128125C	Port Expan Assy, 2x3 (Port A)
3-13	128188	Module Assy, IT24 NAND/NOR Gate
3-7	128190	Module Assy, IT25 NAND Gate
7-	129463C	Port Expan Assy, 1x2 (Port B)
2-40	129554	Trigger Door Latch
11-8	129567	Nut Strip, Speed
10-8	129567-001	Nut Strip, Speed
9-10	129693	Strip, Insulating
9-14	129694	Panel, Blankboard Simulator
1-5	130625J	Memory Port Expan F Assy
9-23	130625J	Memory Port Expan F Assy

(Continued)

Table A-14. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
A-14-		
1-6	130626H	Memory Port Expan S Assy
9-24	130626H	Memory Port Expan S Assy
3-34	130902	Module Assy, ST34 Strobe Generator
3-3	130942	Module Assy, FT37 Buffered Latch No. 2
7-2	130942	Module Assy, FT37 Buffered Latch No. 2
8-2	130942	Module Assy, FT37 Buffered Latch No. 2
12-1	130942	Module Assy, FT37 Buffered Latch No. 2
3-23	130947	Module Assy, BT25 BAND Gate
3-11	130952	Module Assy, FT38 Buffered Latch No. 3
12-5	130952	Module Assy, FT38 Buffered Latch No. 3
13-1	130952	Module Assy, FT38 Buffered Latch No. 3
3-5	130958	Module Assy, LT34 Parity Generator
3-12	130967	Module Assy, BT24 Buffered AND/OR Gate
12-19	130967	Module Assy, BT24 Buffered AND/OR Gate
13-13	130967	Module Assy, BT24 Buffered AND/OR Gate
3-31	131292	Module Assy, ST17 Voltage Regulator
1-	131410	Side Panel Assy
1-	131416	Basic Cabinet Assy
1-	131419	Door, Rear or Front
3-32	131633	Module Assy, HT26 Memory Pre-Amp
5-5	131633	Module Assy, HT26 Memory Pre-Amp
6-3	131633	Module Assy, HT26 Memory Pre-Amp
2-19	131891-001	Cable Assy, Busbar Pick-Up
10-12	131891-001	Cable Assy, Busbar Pick-Up
2-20	131891-005	Cable Assy, Busbar Pick-Up
11-12	131891-005	Cable Assy, Busbar Pick-Up
3-27	132153	Module Assy, ST21 Inhibit Driver
3-26	132159	Module Assy, ST22 Memory Driver
4-2	132159	Module Assy, ST22 Memory Driver
5-1	132159	Module Assy, ST22 Memory Driver
10-2	132197	Channel, Cable Routing
11-2	132197	Channel, Cable Routing
12-10	132277	Module Assy, ZT35 Ribbon Cable
1-	132546Y	Basic 4Kx33 Bit Assy (Port C)
4-	132546Y	Basic 4Kx33 Bit Assy (Port C)
3-15	133053	Module Assy, AT31 Cable Dr/Rec
12-9	133212-171	Module Assy, ZT45 Ribbon Cable
13-7	133212-171	Module Assy, ZT45 Ribbon Cable
10-7	133623	Port Expander F Assy

(Continued)

Table A-14. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
A-14-		
13-14	133625	Printed Wiring Board, Cable Twisted Pair
12-20	133625	Printed Wiring Board, Cable Twisted Pair
11-7	133645	Port Expander S Assy
11-	133651E	Memory Port Expan S Assy
13-14	133763-001	Cable Plug Module Assy (P252-P253)
12-20	133763-201	Cable Plug Module Assy (P252-P253)
12-20	133763-301	Cable Plug Module Assy (P252-P253)
12-20	133764-401	Cable Plug Module Assy (P252-P253)
13-14	133763-651	Cable Plug Module Assy (P252-P253)
2-18	133955	Busbar Assy
2-41	134169	Door, Chassis
2-38	134170-001	Bracket, Door Match Mtg
2-39	134171	Spring, Door Latch
9-3	134196	Busbar Port Expand Assy
9-38	134239	Cover, Fan-Channel Mtg
2-12	134447	Block, Cable Clamping
2-13	134472	Nut, Bar
9-43	134826-001	Bracket, Filter LH
9-44	134826-002	Bracket, Filter RH
9-34	134861	Auxiliary Fan Assy
10-3	136132	Channel, Cable Routing
1-4	136978F	Fixed, Accessory Frame Assy
9-	136978F	Fixed, Accessory Frame Assy
9-1	136979	Bracket, Chassis Mtg LH
9-2	136980	Bracket, Chassis Mtg RH
10-	136992C	Memory Port Expan F Assy
3-36	137481-171	Interframe Ribbon Cable Assy
12-9	137481-171	Interframe Ribbon Cable Assy
13-7	137481-171	Interframe Ribbon Cable Assy
1-	139203	Hardware Kit/Basic Cabinet
1-	139204	Hardware Kit/Front Frame
1-	139205	Hardware Kit/Center Frame
1-	139515	Hardware Kit/Fixed Frame
2-3	139592	Block, Shear Pin Mtg
2-4	139593	Block, Spring Frame Stop
2-2	145314	Cover, Shear Pin Mtg
2-	148832-514	Screw, Hex Thread Forming
2-42	149850	Retainer (See Dwg 132546X)
11-6	149850	Retainer (See Dwg 130626H)
2-	154377-001	Clamp, Strap Type

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