APPLICATION	
NEXT ASSY	USED ON
Final	General Use

REVISIONS			
LTR	DESCRIPTION RN 7-278	DATE	APPROVED
-	REL FOR PROD	23 JAN 81	[illegible]

DEPT. 1-2825-C

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REVISION STATUS OF SHEETS																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
REVISION	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
XX DECIMAL ± XXX DECIMAL ±
ANGLES ± SURFACE QUALITY √ MAX
INTERPRET DWG PER 815002

PRODUCTION

CHANGE BY ECO ONLY

MFG [illegible] 1-22-81

CONT NO.

DRFTG: DR [illegible] DATE 7/19/80
APPD [illegible] 22JAN81
CHK

ENGRG: DEV [illegible] 7/19/80
E/M [illegible] 1/22/81
PROJ [illegible] 1/22/81

SANDERS ASSOCIATES, INC NASHUA, NEW HAMPSHIRE

INTERFACE CONTROL DOCUMENT
SEL HSD-9132/GRAPHIC 7
32-BIT PARALLEL INTERFACE

SIZE	CODE IDENT NO.	DWG NO.
A	94117	5977334

SCALE — SHEET 1 OF 22

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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TABLE OF CONTENTS

SIZE	CODE IDENT NO.	DWG NO.
A	94117	5977334

SCALE		REV	SHEET 2 OF
—		-	

1.0 INTRODUCTION

1.1 GENERAL

This Interface Control Document describes the interface signals, protocol and cabling which are utilized as the 32-bit communications link between the Systems Engineering Labs (SEL) Series--32 computer and the Sanders Associates, Inc., (S/A) Graphic 7 Display System.

All changes or modifications to this ICD will be by change control procedures currently in effect for the Graphic 7 line.

This document is limited to defining interface characteristics; i.e., physical, functional and electrical. Details concerning operation of the individual I/O equipments are not included as part of the ICD.

1.2 SCOPE

This ICD is comprised of two major sections--hardware and software interface characteristics. The hardware interface section defines the various interface signals, timing and cabling. The software section specifies the interface protocol.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

2.0 REFERENCE DOCUMENTS

2.1 SANDERS ASSOCIATES, INC., DOCUMENTS

1. Logic Diagram, S/A Parallel Interface, SEL-HSD9132/Graphic-7, Drawing Number 1088752

2. GCP+ Programmer's Reference Manual, H-77-0348

3. Software Test Requirement Specification, 1088693

2.2 SEL DOCUMENTS

1. Systems Engineering Labs, Inc., Technical Manual, High-Speed Data Interface, Model 9132/9136, Publication No. 303-329132-000, dated April, 1979.

3.0 HARDWARE INTERFACE CHARACTERISTICS

3.1 GENERAL

1. All references to input or output in the ICD are made with reference to the host computer; that is, input is input to the host computer from the Graphic 7 and output is always output from the host computer to the Graphic 7.

2. All communication between the host computer and the Graphic 7 is in parallel mode.

3.2 INTERFACE SIGNAL DEFINITION

The following is a list of the signals and their definitions which will provide the interface communications between the SEL/HSD-9132 and the Graphic 7 parallel interface board.

1. Bidirectional Data Bus (DATØØ-31)

   This 32-bit bidirectional bus carries data, command, status and address information.

2. Input Data Ready (IDR)

   This signal is generated by the Graphic 7 interface and indicates that the input data is stable. This signal remains true until the Input Acknowledge signal is returned by the HSD-9132.

3. Input Acknowledge (IA)

   This signal, generated by the HSD-9132, is used to acknowledge the receipt of the input data. This signal remains true until the IDR signal goes false.

4. Output Data Ready (ODR)

   This signal is generated by the HSD-9132, in conjunction with output data information. This signal remains true until the Output Acknowledge signal is returned by the Graphic 7 interface.

5. Output Acknowledge (OA)

   This signal is generated by the Graphic 7 interface and is used to acknowledge the receipt of the output data. This signal remains true until the ODR signal goes false.

6. External Function (EA)

This signal is generated by the HSD-9132; and, when true, indicates that the associated host computer (SEL-32/55) has placed a command (e.g., Initialize, request status or input/output) onto the data lines.

7. External Function Acknowledge (EFA)

This signal is generated by the Graphic 7 interface and is used to acknowledge the receipt of the EF signal. The EFA signal remains true until the EF signal goes false.

8. Device Present (DP)

This signal is a level which is generated by the Graphic 7 interface. This signal remains true after the Graphic 7 power is turned on.

9. Input Status Ready (ISR)

This signal is generated by the Graphic 7 interface and, when true, indicates that the Graphic 7 system has data which should be read by the host computer. That is, the host computer should initiate an Input command sequence. It should be noted that the host (SEL) computer must first issue a "Device Status Request" command in order for the Graphic 7 interface to generate the ISR signal. The ISR signal remains true until the receipt of either the ISA signal or the IOR signal.

10. Input Status Acknowledge (ISA)

This signal is generated by the HSD 9132 and is used to acknowledge the receipt of the ISR signal. The ISA signal remains true until the ISR signal goes false.

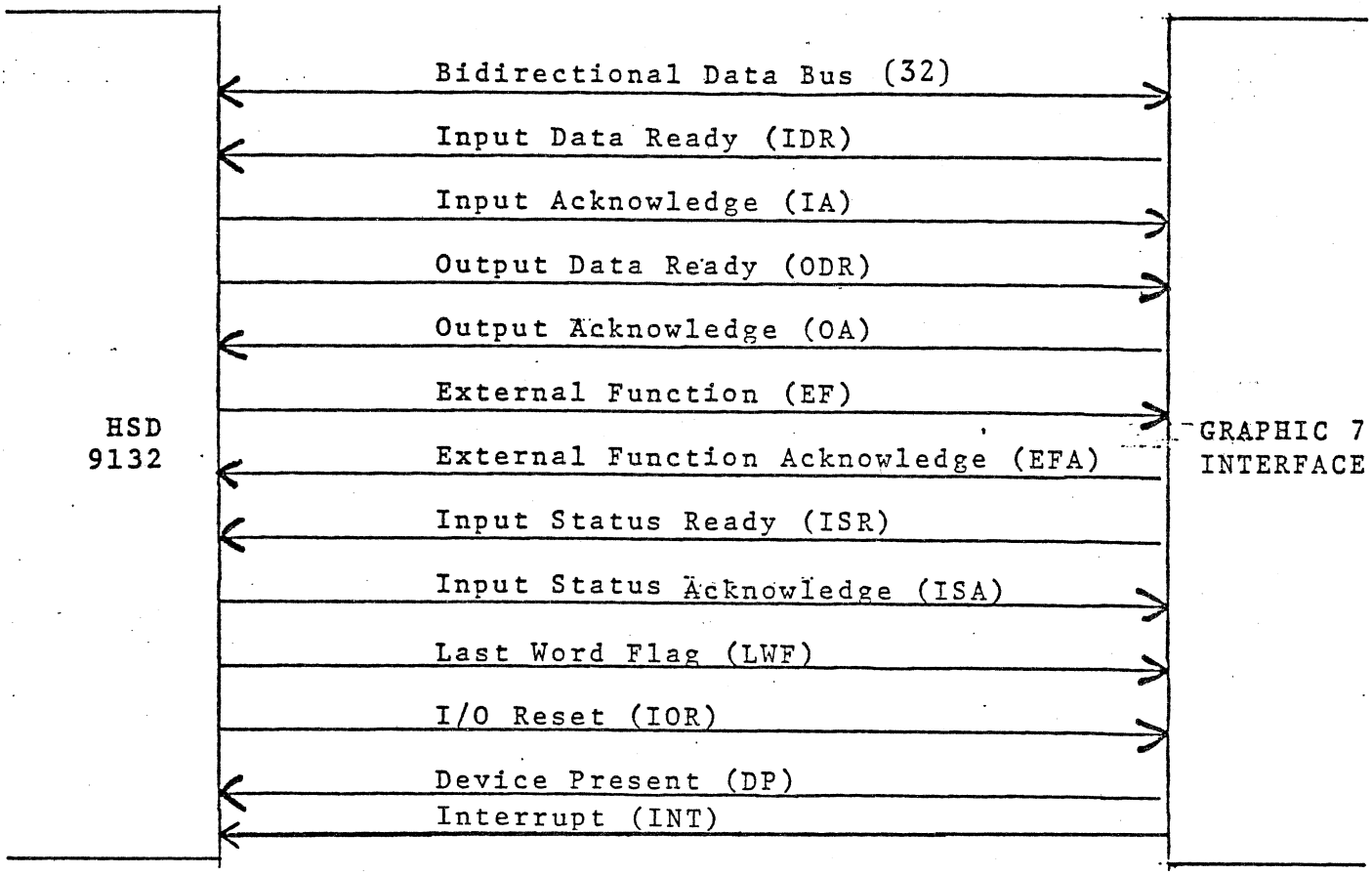
11. Last Word Flag (LWF)

This signal accompanies the last ODR signal in the output mode or the last IA signal in the input mode. This is a flag from the HSD 9132 to the Graphic 7 interface signifying End-of-Block.

I/O Reset (IOR)

is signal is generated by the HSD9132 and is used by the
phic 7 interface to reset a previously received "Device
us Request" command.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



HSD-9132/GRAPHIC 7

INTERFACE SIGNALS

FIGURE I

SIZE	CODE IDENT NO.	DWG NO.	
A	94117	5977334	
SCALE —		REV -	SHEET 7 OF

13. Interrupt (INT)

This signal (250 - 400 ns pulse) is generated by the Graphic 7 whenever it has input data to send. The HSD3192 has the option of using this or the ISR signal to determine if the Graphic 7 has input data to send.

3.3 INTERFACE OPERATION

3.3.1 Initialization

1. Host places a low logic level on the DATØ8 data line and, if set up to address a particular Graphic 7 parallel interface, will place the proper address (determined by four switches on the Graphic 7 parallel interface board) on the Data bus lines, DAT 12 - 15.

2. Host places a low logic level on the External Function (EF) line.

3. If the Graphic 7 Parallel Interface is set up to respond to a certain address (this is an option), it will read the address on data lines DAT 12 - 15. If it is being addressed, it will continue with Step 4. If it is not being addressed, it will do nothing. If it is not set to respond to a particular address, it will proceed directly from step 2 to step 4.

4. The Graphic 7 Parallel Interface detects the low logic level on the DATØ8 and the EF lines, executes the initialization sequence and puts a low logic level on the External Function Acknowledge (EFA) line.

5. The host detects the reset EFA line and places a high logic level on the EF line.

6. The Graphic 7 parallel interface detects the high EF line and places a high logic level on the EFA line.

3.3.2 Input Transfer Setup

3.3.2.1 Interrupt

1. The Graphic 7 parallel interface sends a low going 250 - 400 nanosecond pulse on the Interrupt (INT) line.

2. The host parallel interface detects the pulse on the INT line.

3.3.2.2 Status Poll

If the Interrupt line is not being used by the host interface, the following will be used to set up for an input transfer:

1. Host places a low logic level on the DATØ2 line; and if set up to, will place an address on the DAT12 - 15 lines. The host will then place a low logic level on the EF line.

2. If the Graphic 7 is set up to respond to an address on the DAT12 - 15 lines, it will read the address; and if it is the proper address, it will proceed to Step 3. If the address is not the proper address, the Graphic 7 parallel interface will do nothing in response. If the Graphic 7 is not set up to respond to an address on the DAT12 - 15 lines, it will proceed directly from step 1 to step 3.

3. The Graphic 7 parallel interface detects the low DATØ2 and EF lines and places a low logic level on the EFA line.

4. The host detects the low EFA line and places a high on the EF line.

5. The Graphic 7 detects the high EF line and places a high logic level on the EFA line. If the Graphic 7 is ready to send an input transfer, it will place a low logic level on the Input Status Ready (ISR) line. If it is not ready, it will wait until it is ready to send an input transfer, then place a low logic level on the ISR line.

6. The host detects the low ISR line and places a low logic level on the Input Status Acknowledge (ISA) line.

7. The Graphic 7 detects the low ISA line and places a high on the ISR line.

8. The host detects the high ISR line and places a high on the ISA line.

3.3.3 Input Transfers

In response to the interrupt pulse or the ISR signal, the host parallel interface will initiate the input transfer sequence. The following steps describe this sequence.

1. The host places a low logic level on the DATØØ line; and if set up to, will place an address on the DAT12 - 15 lines. The host will then place a low logic level on the EF line.

2. If the Graphic 7 is set up to respond to an address on the DAT12 - 15 lines, it will read the address; and if it is the proper address, it will proceed to step 3. If it is not the proper address, the Graphic 7 parallel interface will proceed no further. If the parallel interface is not set up to respond to the address, it will proceed directly from step 1 to step 3.

3. The Graphic 7 parallel interface detects the low DATØØ and EF lines and places a low logic level on the EFA line.

4. The host detects the low EFA line and places a high logic level on the EF line.

5. The Graphic 7 detects the high EF line and places a high logic level on the EFA line.

6. The Graphic 7 places the data word to be sent on the Data Bus DATØØ - DAT 31 and places a low logic level on the Input Data Ready (IDR) line.

7. The host detects the low IDR line, receives the input data and places a low logic level on the Input Acknowledge (IA) line.

8. The Graphic 7 detects the low IA line and places a high logic level on the IDR line.

9. The host detects the high IDR line and places a high logic level on the IA line.

10. Steps 6 through 9 are executed for every word in the transfer; and on the host word, the host will place a low logic level on the Last Word Flag (LWF) line in step 7 when it lowers the IA line and will set the LWF line again when it sets the IA line in step 9.

3.3.4 Output Transfers

Whenever the host is ready to transfer output data to the Graphic 7, it will initiate the following sequence:

1. The host will place a high logic level on the DATØØ line; and if it is set up to, will place an address on the DAT12 - 15 lines. The host will then place a low logic level on the EF line.

2. If the Graphic 7 is set up to respond to an address on the DAT12-15 lines, it will read the address. If it is the proper address, it will proceed to step 3. If it is not the proper address, the Graphic 7 parallel interface will proceed no further. If the Graphic 7 parallel interface is not set up to respond to the address on DAT12-15, it will proceed directly from step 1 to step 3.

3. The Graphic 7 parallel interface detects the low EF line and the high DATØØ line and places a low logic level on the EFA line.

4. The host detects the low EFA line and places a high logic level on the EF line.

5. The Graphic 7 detects the high EF line and places a high logic level on the EFA line.

6. The host parallel interface places a 32-bit data word on the DATØØ-DAT31 data bus lines and places a low logic level on the Output Data Ready (ODR) line.

7. The Graphic 7 Parallel Interface detects the low ODR line, receives the 32-bit data word from the DATØØ-DAT31 lines and places a low logic level on the Output Acknowledge (OA) line.

8. The host detects the low OA line and places a high logic level on the ODR line.

9. The Graphic 7 detects the high ODR line and places a high logic level on the OA line.

10. Steps 6 through 9 are repeated for each word of the transfer. On the last word of the transfer, the host will place a low logic level on the LWF line at the same time that it lowers the ODR line in step 6 and sets the LWF line at the same time that it sets the ODR line in step 8.

3.4 ELECTRICAL CHARACTERISTICS

3.4.1 Signal Levels

At the interface, a logic ONE is defined as being between zero volts and +1.5 volts; and a logic ZERO is defined as being +3.2 volts and +5.0 volts.

These seemingly pseudo TTL levels exist because of the driver-receiver circuit (SN75138, open-collector quad bus transceivers).

The Graphic 7 Parallel Interface board utilizes 0.01 microfarad capacitors, for high frequency decoupling purposes.

3.4.2 Interface Connectors

1. The SEL-HSD9132 end of the interface cable assembly A utilizes two (2) connectors of the following types:

   AMP Mod-4, Body: 2-86177-1 Contacts: 86016-1

   These two (2) connectors are referred to as "P1" and "P2" in Figure 2.

2. The Graphic 7 end of the interface cable assembly A utilizes two (2) connectors of the following type:

   Berg: 65043-012

   This is referred to as "P4" and "P5" in Figure 2.

3. Cable assemblies B and C are connectors of the following type:

   3M: 3425-6050

3.4.3 Interface Cabling

1. Cable assembly A uses:

   Belden number 9525
   (25) twisted pairs, No. 28 AWG
   Outer shield and vinyl cover, 70 feet

2. Cable assemblies B and C use:

   Scotchflex number 3365/50
   50 wire ribbon cable, 1.5 feet

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

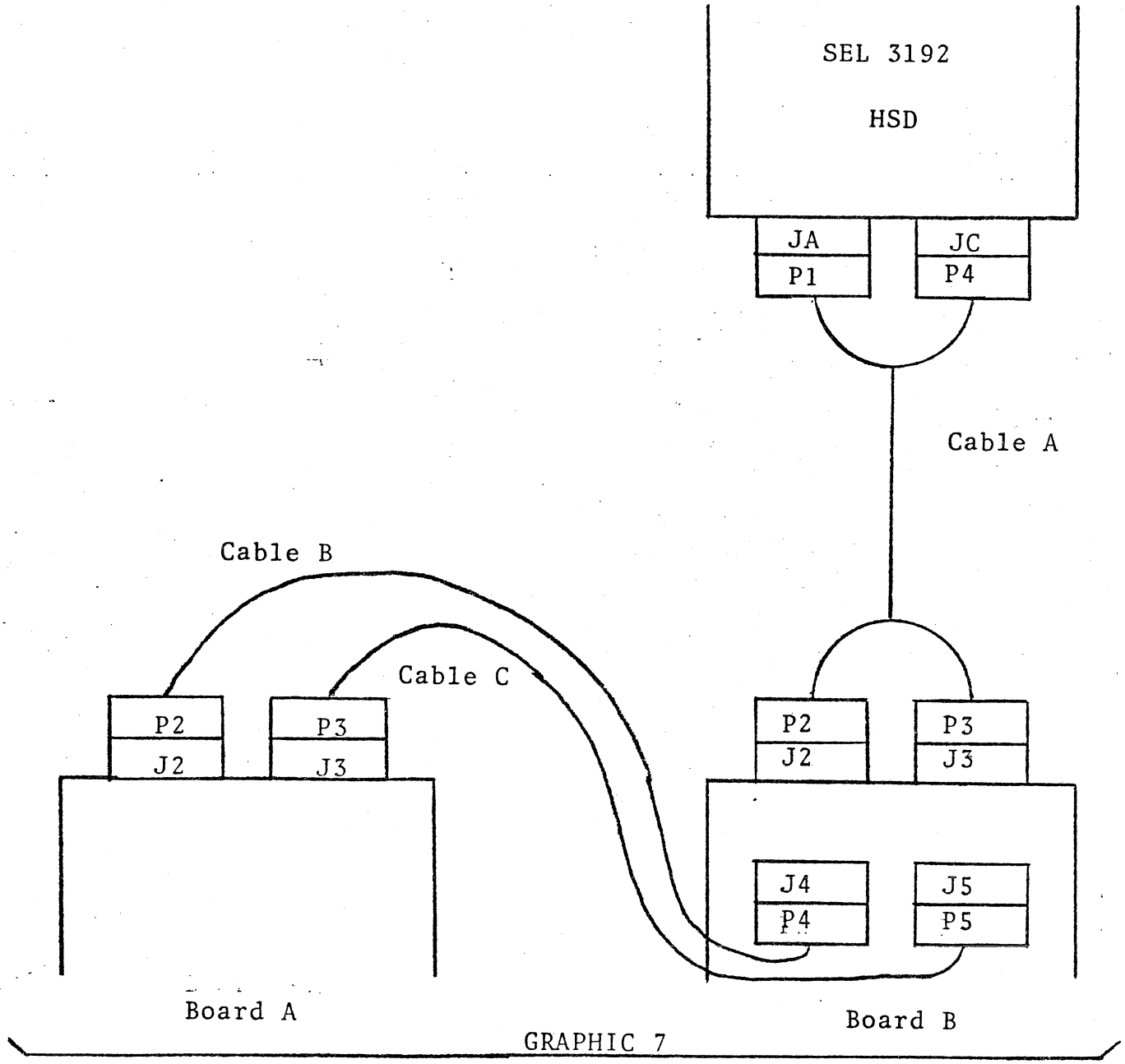


FIGURE 2

Configuration: SEL 9132 - Graphic 7 32-Bit Parallel Interface

SIZE	CODE IDENT NO.	DWG NO.	
A	94117	5977334	
SCALE —		REV -	SHEET 13 OF

4.0 SOFTWARE CHARACTERISTICS

All communications between the host computer and the Graphic 7 can be handled by GCP+ (Graphics Control Program) or by down-loaded user-generated software. Transmissions in either direction are referenced to as messages. Each message begins with a command header that contains two ASCII characters to define the message type. The header is then followed by as many 16-bit words as are required to transmit the associated data. No translation of the data words is necessary, and no end of message indicator is required.

GCP+ supports nineteen different types of messages across the interface that are divided into two groups--fundamental and additional messages.

However, as noted above, additional messages forming the user's own communications software can be written and used as per the interface protocol described herein.

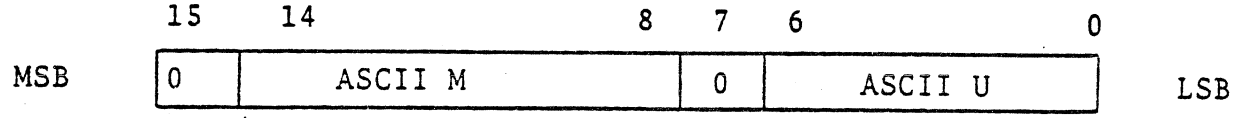
4.1 GCP+ FUNDAMENTAL MESSAGES

These messages which represent a nucleus of Graphic 7 functions allow the user to achieve an interactive graphic capability. These messages provide a means to display a graphic image and allow (1) the image to be rapidly transformed and (2) system identification of particular items within the image in response to operator actions.

The format for these messages is as shown by the example below.

Each message consists of a command word followed by a number of argument words. The 16-bit command word is always formed from two 7-bit ASCII letters.

Example: Command Word: MU



The argument words contain either auxiliary data for the command word or display data.

4.2 GCP+ ADDITIONAL MESSAGES

Additional GCP Graphic 7 messages give the user detailed control and access to all of the display terminal registers and parameters. These messages are available, ready for use, in the basic Graphic 7 terminal controller. See Table 4-1.

The additional message format is as per Section 4.1. Additional detail concerning all standard Host/Graphic 7 messages may be found in the Programmer's Reference Manual. This manual also contains information for linking user code with the standard version of GCP+.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TABLE 1

HOST/GRAPHIC 7 MESSAGE SUMMARY

Fundamental Messages

Host-to-Graphic 7		Graphic 7-to-Host	
Initialize	(IZ)	Keyboard	(KY)
Memory Update	(MU)	Lightpen	(PN)
Start Picture	(SP)	Function Key	(RK)
Halt Picture	(HP)		

Additional Messages

Host-to-Graphic 7		Graphic 7-to-Host	
Continue Picture	(KP)	Keyboard #2	(KT)*
Selective Update	(SU)	Lightpen #2	(PT)*
Give Image	(GI)	Return Image	(RI)
Give Register	(GR)	Return Register	(RR)
Selective Interrupt Control	(IK)	Scratchpad Ready	(XR)(XT)*
Light Function Keys	(LK)(LT)*	Return PED	(RP)(RW)*
Initialize PED ①	(IP)(IT)*	Lightpen Switch	(SW)(ST)*
Give PED	(GP)(GT)*	Display Halt Interrupt	(HI)
Initialize Scratchpad	(ZR)(ZT)*	Display X-Y Overflow	(XI)
Transfer Control	(TK)	Error Condition	(XX)
		Variable Length Block	(VL)
		Function Key #2	(RL)*

① PED - Positional Entry Device (i.e., Trackball, forcestick)

SIZE	CODE IDENT NO.	DWG NO.
A	94117	5977334
SCALE —		REV - SHEET 6 OF

5.0 TEST REQUIREMENTS

5.1 ACCEPTANCE TESTING

Acceptance testing of the SEL 9132 HSD Graphic 7 Parallel Interface shall be as per the following document:

Software Test Requirement Specification, Host Computer Interface to Graphic 7 — 1088693

APPENDIX A

Parallel Interface Register Descriptions

A-1 General

Tables A-1 and A-2 list register and interrupt trap addresses in the Parallel Interface. Tables A-3 through A-7 list and describe the significance of individual bits in the Parallel Interface registers.

TABLE A-1

Parallel Interface Register Addresses

Register	Address
Word Count (WCR)	172410
Memory Address (MAR)	172412
Status (STR)	172414
Data (IDR and ODR)	172416

TABLE A-2

Parallel Interface Interrupt Trap Addresses

	Address
Input	120
Output	124
Attention	130

TABLE A-3

WORD COUNT REGISTER BIT DESCRIPTIONS

Bit #	Name	Description
00-15	Word Count	Program read/write, cleared by bus reset. To initiate a DMA mode, the program writes the two's complement of the number of words to be transferred between memory and the Host. Each time the Interface completes a DMA word transfer, the word count is incremented by +1. The Interface continues the DMA mode until the word count = 0 and then sets DMA Complete (status register, bit 04) and generates an interrupt.

TABLE A-4

MEMORY ADDRESS REGISTER BIT DESCRIPTIONS

Bit #	Name	Description
00-15	Memory Address	Program read/write, cleared by bus reset. Before entering a DMA mode, the program writes the starting memory byte address of the transfer. After each word is transferred, during the DMA mode, the Interface increments the address by +2 bytes.

TABLE A-5

STATUS REGISTER BIT DESCRIPTIONS (Cont)

Bit #	Name	Description
06	Output Interrupt Enable	Program read/write, cleared by bus reset. This bit when set allows the Interface to generate an interrupt to indicate either a data ready or an output DMA complete.
07	Output Control	Program read only. This bit reflects the state of the Output Control signal from the Host and is raised to indicate that output data is available.
08	Count ≠ Ø BEG END	Program read only, cleared by bus reset. This bit when set indicates that the word count register contains a non-zero value.
09, 10	Attention #1, #2	Program Read Only. If attention bit #1 is high, the word being transferred is the first word in the transfer. If attention bit 2 is high, the word being transferred is the last word of the transfer.
11	Attention Interrupt Enable	Program read/write, cleared by bus reset. This bit when set allows the interface to generate an Attention (optional) interrupt if either Attention #1 (bit 09) or Attention #2 (bit 10) goes high.
12	Spare Input #2	Program read/write, cleared by bus reset. This bit is directly presented to the Host and can be programmed as required.

TABLE A-5

STATUS REGISTER BIT DESCRIPTIONS (Cont)

Bit #	Name	Description
13	Input Word Request	Program read/write (set only), cleared by bus reset. If a single word input transfer is desired, the program loads the input data register and then sets this bit to indicate to the Host that data is available. Either a data taken interrupt or sensing Input Ready (bit 15) indicates that the single transfer is complete. During an input DMA mode, the Interface reads data from memory, loads the input data register and then sets this bit. This bit is cleared whenever a new data ready pulse (NDRY) occurs. (Note: The Interface generates an NDRY pulse, for the Host, whenever Input Control, from the Host, goes high.
14	Input Interrupt Enable	Program read/write, cleared by bus reset. This bit, when set, allows the Interface to generate an interrupt to indicate either a data taken or an input DMA complete.
15	Input Not Ready	Program read only. This bit is reset if both the Input Word Request (bit 13) and the Input Control signal, from the Host, are clear. When set, this bit indicates that an input data transfer is in process.

TABLE A-6
OUTPUT DATA REGISTER BIT DESCRIPTIONS

Bit #	Name	Description
00-15	Output Data	Program Read only. These bits reflect the state of the data lines from the Host. The program reads these bits either when a Data Ready interrupt occurs or after sensing output control (status bit 07). During output DMA, the Interface loads this data into memory. Note: The Interface will accept either high true or low true output data from the Host.

TABLE A-7
INPUT DATA REGISTER BIT DESCRIPTIONS

Bit #	Name	Description
00-15	Input Data	Program write only, cleared by bus reset. These bits are directly presented to the Host. (Note: The Interface will provide either high true or low true data to the Host.) During an input DMA, the Interface loads this register with memory data. During single data transfers, the program loads this data prior to raising Input Word Request (status bit 13).