H-80-0055

Graphic7™

COMPUTER GRAPHICS DISPLAY SYSTEM

MODELS 7709/7710 TERMINAL CONTROLLER MAINTENANCE MANUAL

Information Products Division
Federal Systems Group
SANDERS
DANIEL WEBSTER HIGHWAY, SOUTH—NASHUA, NEW HAMPSHIRE 03061

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RECORD OF CHANGES

CHANGE NO.	DATE	TITLE OR BRIEF DESCRIPTION	ENTERED BY
1	SEPT 81	Corrects Errors	

SAFETY PRECAUTIONS

The following are general safety precautions not related to any specific procedure and therefore do not appear elsewhere in this manual. These are recommended precautions that must be understood and applied during installation or maintenance of the terminal controller.

AVOID LIVE CIRCUITS

Observe all safety regulations at all times. Do not replace components in the terminal controller power panel assembly with power applied.

RESUSCITATION

When working with or near high voltages, be familiar with modern resuscitation methods.

WARNING

Primary power (100 Vac to 240 Vac) is present at the power panel assembly. Line voltage of 115 Vac is present at the power supply.

Always turn off terminal controller and pull power plug before removing any cabinet- or chassis-mounted component.

TERMINAL CONTROLLER PROTECTION

Circuit card assemblies in the terminal controller can be damaged by transient surges.

CAUTION

Always turn off terminal controller before removing or installing any circuit card.

Always turn down brightness of display indicator before removing or installing any circuit card in terminal controller.

SPECIAL HANDLING FOR MOS DEVICES

MOS devices are subject to damage caused by static charges. Assemblies that contain MOS devices are the D/A converters and character generator. When not installed in the card cage, these assemblies should be stored in black Velostat bags with the MOS warning statement printed on the outside of the bag.

CAUTION

Always handle these cards only by the card extractors or by the edges of the connector. Avoid touching the card components or the printed circuit.

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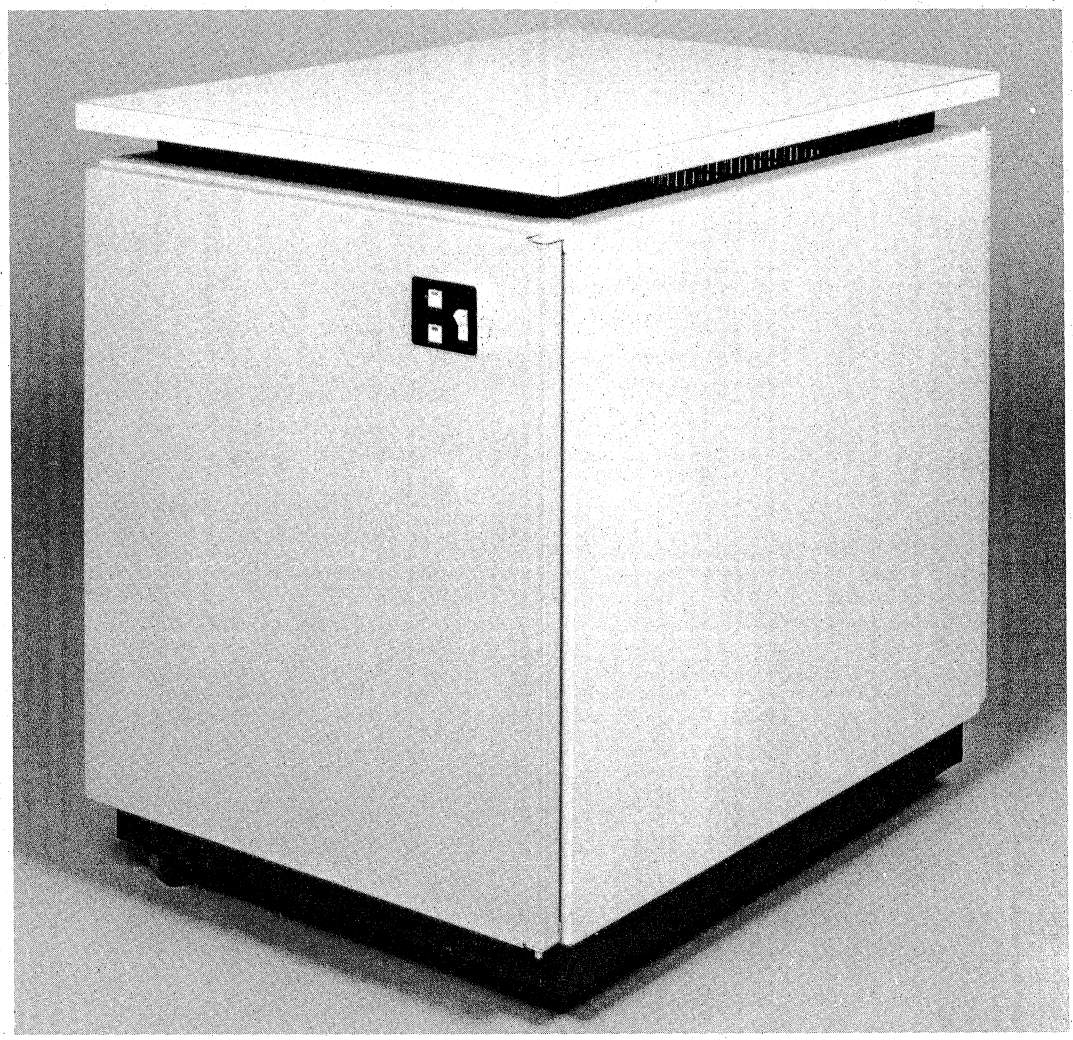

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Figure 1-1. GRAPHIC 7 Terminal Controller

SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

The GRAPHIC 7® system is an intelligent interactive graphic display system that is compatible with most computers. System output is a display image on a CRT indicator.

The GRAPHIC 7 terminal controller (figure 1-1) is a fundamental component of the GRAPHIC 7 system (figure 1-2).

The terminal controller is that component of the GRAPHIC 7 system that receives instructions from the host computer and converts those instructions to X, Y, Z drive signals that produce graphic displays on up to four display indicators. The displays may consist of combinations of lines (vectors), conics, alphanumerics, and special symbols. Displays may have a wide variety of formats: tabular, maps, diagrams, or pictorial. The terminal controller determines the form of the display, the position of the data, its intensity, size, orientation, and color.

When suitable options are provided, the terminal controller can impart motion to displayed data in two or three dimensions.

The terminal controller is controlled either by a host computer or by the terminal operator. The computer may be located near the terminal controller or remote from it; in the latter case, modems may be required for communication.

Major assemblies of the terminal controller include two microprocessors, read-only memory, random access read/write memory, vector and character generators, and an output channel.

Various ancillary devices such as tape readers, position entry devices, alpha-numeric/function keyboards, PHOTOPEN®, and hardcopy units are available as options.

1.2 PHYSICAL DESCRIPTION

The terminal controller comprises a card cage containing 17 circuit card slots, a power supply, and two blower fans (figure 1-3). A control panel covers the front of the unit; a protective cover is mounted on the back.

The terminal controller is mounted either in a standard 19-inch equipment rack or in an optional cabinet (figure 1-4). In either case, the control panel is removed for access into the terminal controller.

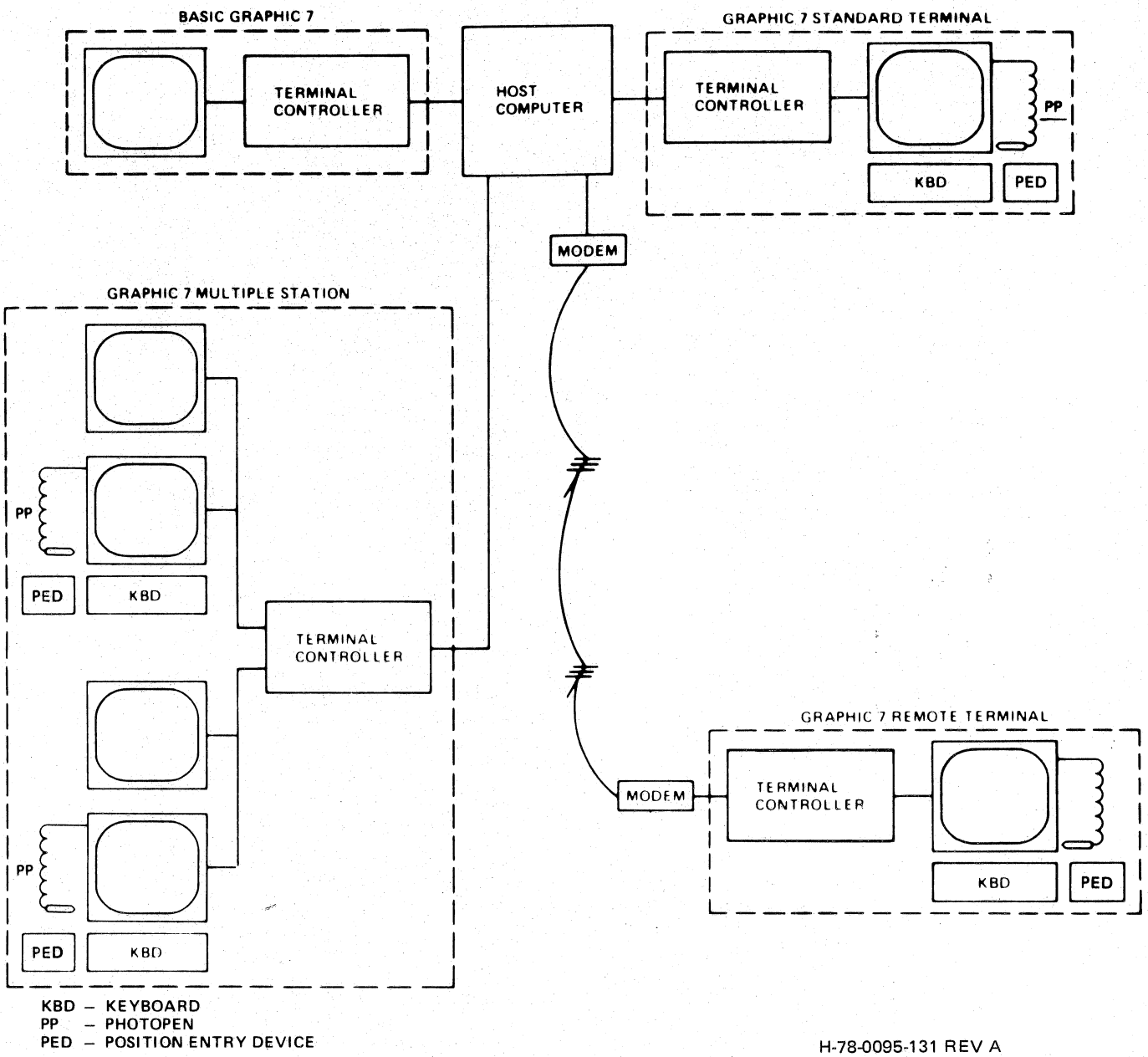

Figure 1-2. Typical GRAPHIC 7 System Configurations

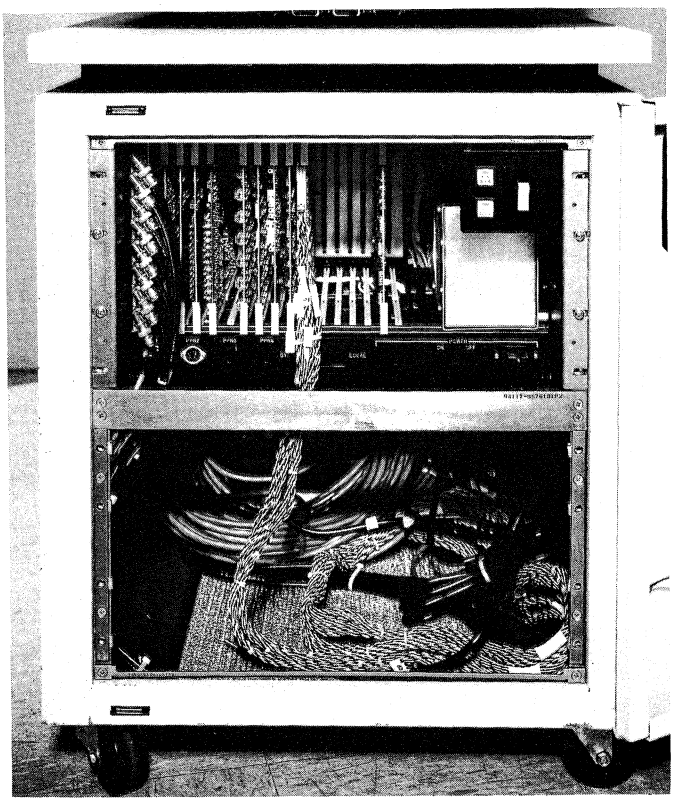

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Figure 1-3. Terminal Controller Interior

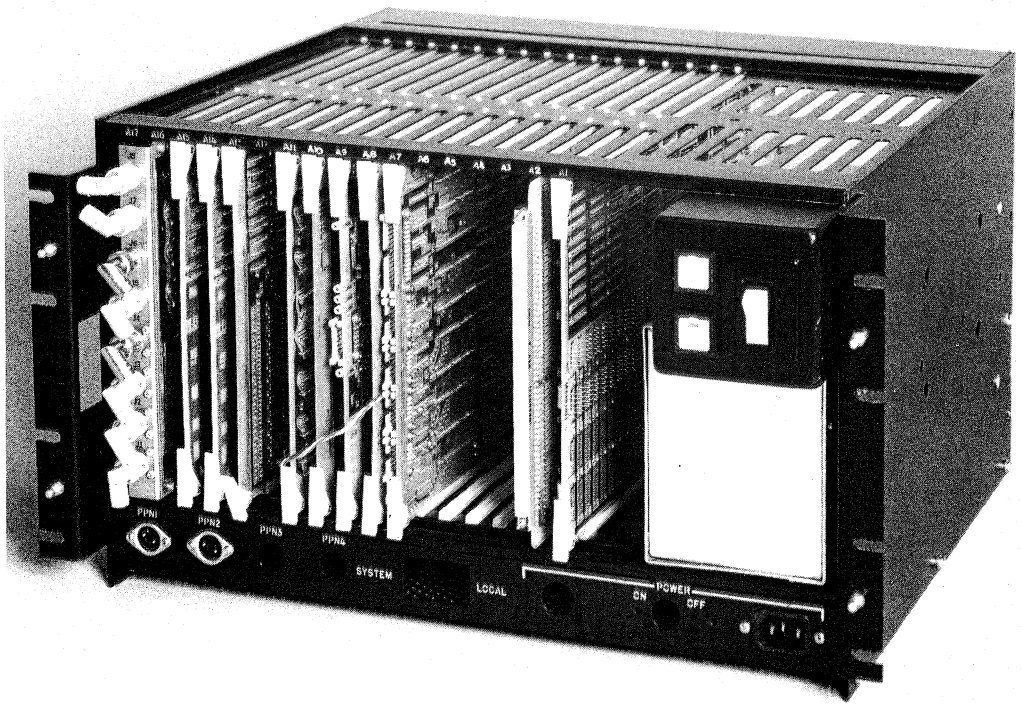

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Figure 1-4. Card Cage

As shown in figure 1-3, the circuit cards are inserted into the card cage from the front of the terminal controller, and plug into a wire-wrapped backplane. The blower fans, located beneath the card cage and power supply, draw air from the bottom of the unit and discharge the air through the top.

The basic terminal controller contains nine standard circuit cards. Optional cards are inserted as required. Most applications use both the multiport serial interface and the parallel interface cards. Other cards are available to expand the read/write memory or provide special display functions.

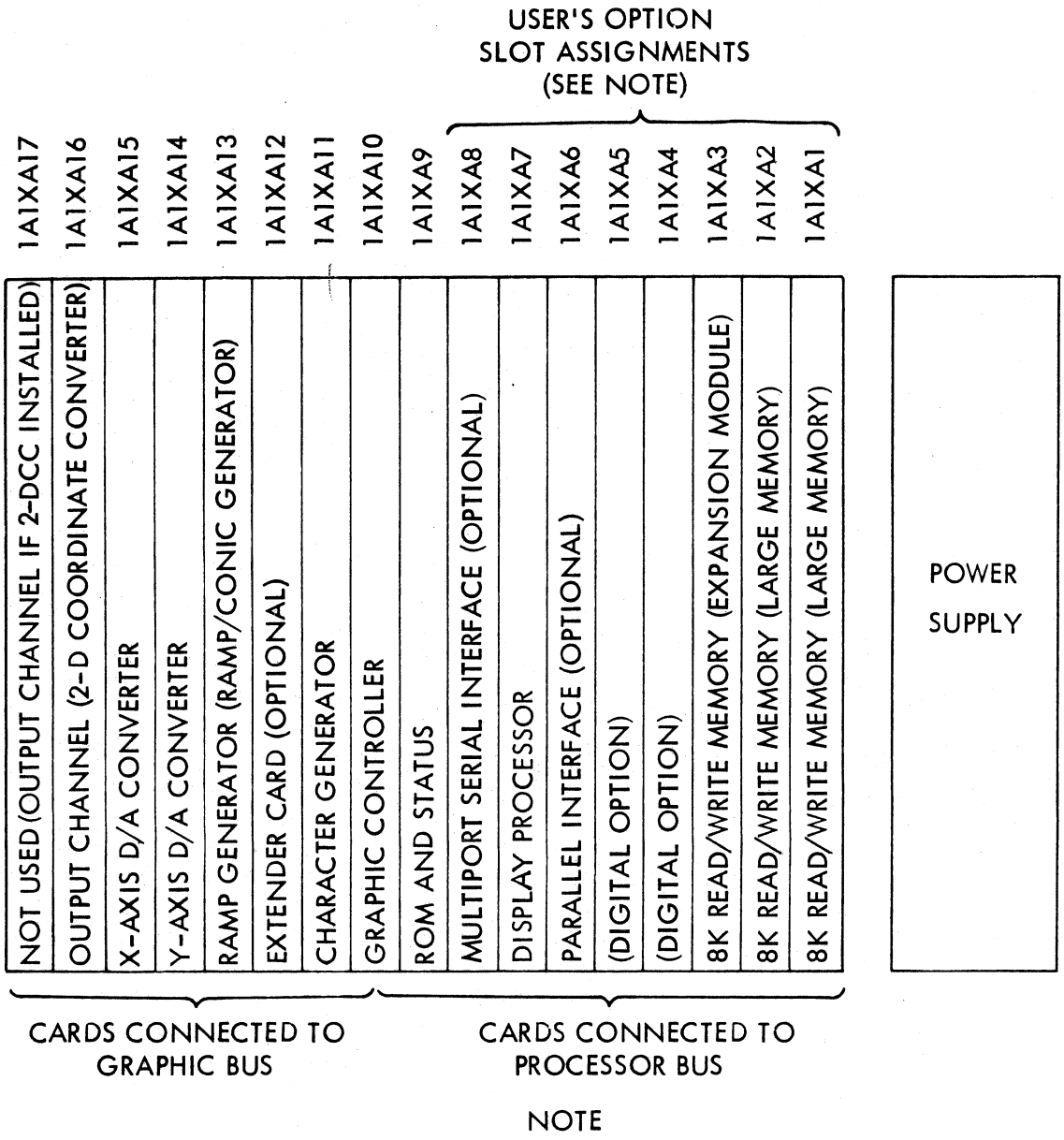
Figure 1-5 shows the circuit card order assumed for this manual. The figure indicates the normal locations for a full complement of circuit cards, including the optional interface cards and read/write memory expansion cards. The figure also shows the optional circuit card extender located in the normally unused 1A1XA12 position.

Table 1-1 lists the physical characteristics of the terminal controller and circuit cards.

Table 1-1. Physical Characteristics

TERMINAL CONTROLLER	
Height	10.5 inches (26.8 cm)
Width	19.0 inches (48.2 cm) including mounting flanges
Depth	16.0 inches (40.6 cm)
Weight	55 pounds (25 kg) including circuit cards
CIRCUIT CARDS	
Height	12-3/8 inches (31.4 cm)
Width	7-3/4 inches (19.7 cm)

The terminal controller can operate with 100V - 120V or 220V - 240V ac input power. An input power control panel (located in the lower front of the equipment cabinet) contains a fuse, a power receptacle, and a removable configuration plug. The configuration plug must be wired for the proper voltages.



NOTE

The backplane wiring for the card cage is identical for card slots 1A1XA1 through 1A1XA8, making the designated card placement for those slots arbitrary. Except for the read/write memory cards, the cards in these eight slots can be interchanged to reassign processor bus control priorities as desired, with the bus control priority grant function being passed in card slot sequence from the highest-priority slot (1A1XA1) toward the lowest-priority card (graphic controller 1A1XA10). Relocatable cards must be placed in adjacent slots (1A1XA8, 1A1XA7, 1A1XA6, etc., in that order); leaving any one of these slots vacant would break the priority chain, which could result in unit malfunction. The read/write memory cards are passive circuits that are accessed by the processor bus but do not seize bus control; their grant outputs never go false. Accordingly, read/write memory cards should be placed in available position (usually spaced for better heat dissipation) toward the highest-priority slot.

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Figure 1-5. Terminal Controller Card Locations

1.3 FUNCTIONAL DESCRIPTION

The terminal controller circuit cards comprise two interconnected groups (see figure 1-6):

Group 1	Group 2
Display processor	Graphic controller (common to both groups)
Read/write memory	Character generator
Read-only memory	Ramp generator (or ramp/conic generator option)
Graphic controller (common to both groups)	Y-axis D/A converter
Multiport serial interface (optional)	X-axis D/A converter
Parallel interface (optional)	Output channel
Expansion module (optional)	2D coordinate converter (optional)
Floating point converter (optional)	
2D/3D coordinate converter (optional)	

Group 1 cards are interconnected by a common processor bus containing data, address, and control lines. This group is controlled by the microprocessor on the display processor card. Group 1 cards handle communications with the host computer and direct the operations of group 2 cards.

Group 2 cards are interconnected by a common graphic bus containing data and control lines. This group is controlled by the microprocessor on the graphic controller card, and directs the development of images on the display indicators and associated hard copy unit.

The following paragraphs summarize the functions of the group 1 and group 2 cards.

1.3.1 GROUP 1 CIRCUIT CARDS

1.3.1.1 Display Processor. The display processor card is a general purpose digital computer that runs the GCP+ and acts as master control for all devices connected to the processor bus. It contains eight high-speed general purpose registers that can be used as accumulators, pointers, index registers, or auto-indexing pointers in auto-increment and auto-decrement modes. Functions performed by the display processor include system initialization, interface handling, local data editing, and local generation of simple display images.

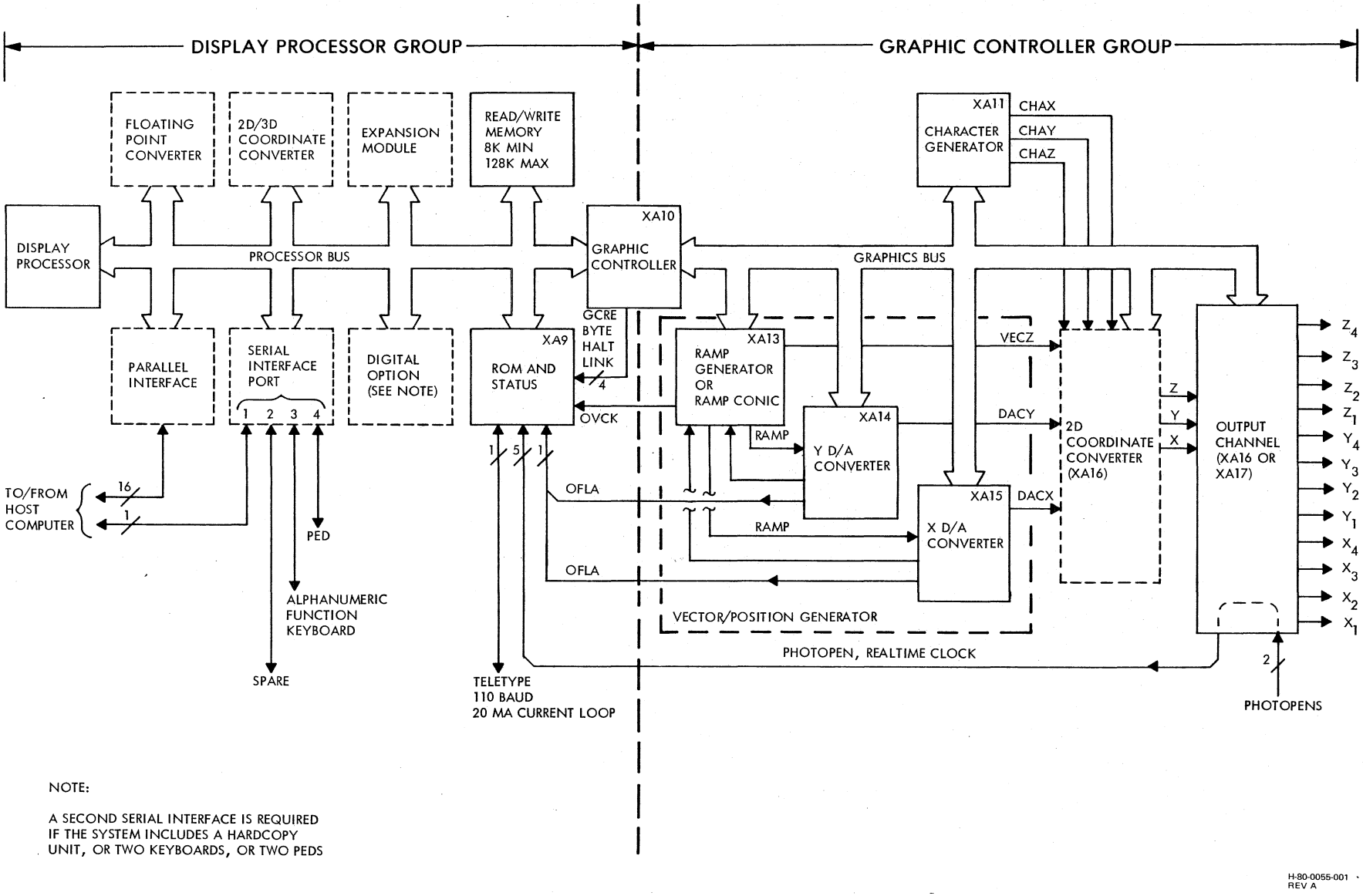


Figure 1-6. Terminal Controller Block Diagram

Instructions used for the display processor emulate the instruction set for the PDP-11® series of minicomputers manufactured by Digital Equipment Corporation (DEC®). They are fetched either from the GCP+ in read-only memory or from the read/write memory.

1.3.1.2 ROM and Status Logic. The ROM and status logic card contains the read-only memory in which the GCP+ used to control the display processor is stored (refer to figure 1-7). Also contained on the card are display status and interrupt logic circuits plus a serial interface port to which the teletypewriter may be connected for diagnostic purposes.

The standard read-only memory provided on the ROM and status logic card contains the GCP+ program. The GCP+ is approximately 6.6K words (16 bits). Like read/write memory, read-only memory may be accessed to retrieve either 16-bit words or individual 8-bit bytes.

1.3.1.3 Read/Write Memory. The basic configuration of a GRAPHIC 7 terminal controller includes one card of random access read/write memory capable of storing 8192 16-bit words. Two additional cards may be added to provide a total of 24,576 words of read/write memory. Locations in the read/write memory are assigned addresses 000000_8 through 137777_8 and are accessed by means of a 16-bit address on the processor bus. The 16-bit address can be used to access the location of a word (16 bits) or of an individual byte (8 bits) as required. Refer to figure 1-7 for a GRAPHIC 7 system memory map.

NOTE

User refresh programs will not execute in RAM memory in the 24K to 32K area (140000-177777). This area is reserved for Sanders' display processor option software. The option software is loaded from the expansion module or is down-loaded from the host.

A large read/write memory is available as an optional replacement for the 8K memory. Each large memory card is capable of storing $65,536_{10}$ (64K) sixteen bit words or 128K separately addressable 8-bit bytes. A maximum of two large memory cards can be installed in a GRAPHIC-7 system for a total of 128K 16-bit words of memory. (The large read/write memory card is also available in 16K and 32K word sizes.)

The large read/write memory cards (options) cannot be used with the basic 8K memory cards. The large read/write memory cards are described in Sanders' "Models 7702-7704 Large Read/Write Memory Technical Manual" (see Appendix C).

1.3.1.4 Expansion Module. Additional memory option features are stored in EPROMs on the expansion module card. The terminal controller can accommodate two such cards. Each expansion module may contain up to 32 EPROMs, providing a maximum (per card) of 32K 16-bit words of non-volatile memory storage.

Each group of two EPROMs represents a 2048 x 16-bit option group. This is the smallest grouping in which options are supplied.

®PDP and DEC are registered trademarks of Digital Equipment Corporation

NOTE

Addresses listed are byte addresses. Each 16-bit word occupies two byte addresses. The last digit in the address is always even when the system is in WORD MODE, but may be odd when the system is in BYTE MODE. Memory address counters throughout the system increment by 2 in WORD MODE.

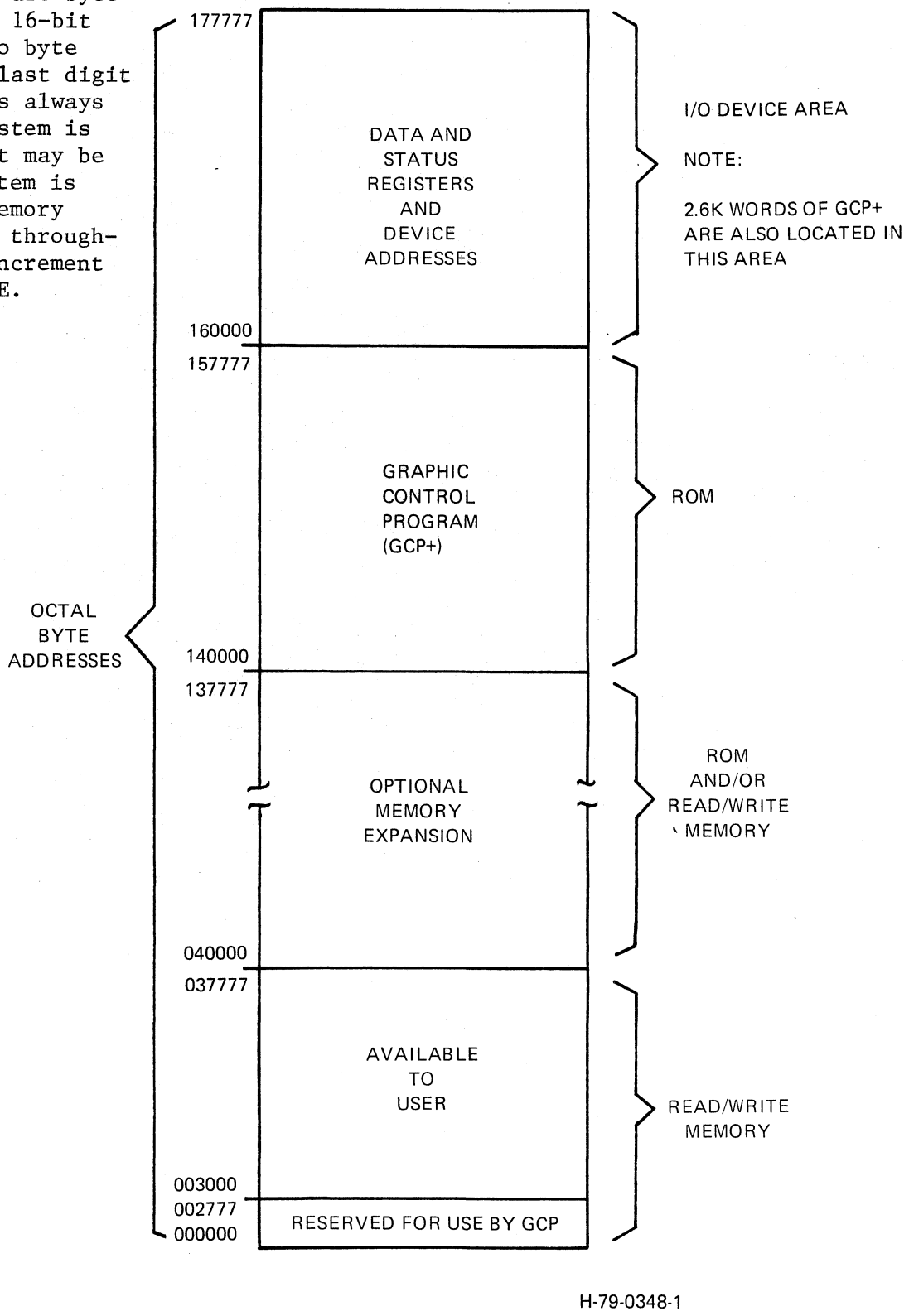


Figure 1-7. GRAPHIC 7 System Memory Map

The expansion module is described in Sanders' "Model 7750 Expansion Module Technical Manual." Individual options are described in their respective user's manuals. See Appendix C.

1.3.1.5 Multiport Serial Interface. The multiport serial interface card contains four serial interface ports that operate in a serial asynchronous mode using RS-232C or TTL voltage levels with standard transmission rates up to 9600 baud. In addition, the first port can be operated as a full RS-232C asynchronous interface at transmission rates greater than 9600 baud. For GCP+ applications, the maximum transmission rate supported is 9600 baud. Normally, the host computer is connected to the first port, which is compatible with the standard communication and terminal interfaces supplied by most computer manufacturers. The remaining three ports on the card are used for peripheral devices.

Two multiport serial interface cards may be installed in a terminal controller to handle additional peripheral devices if required. Normal device assignments for each port are listed in Section 4.

1.3.1.6 Parallel Interface. The parallel interface card is an option intended for installations where the GRAPHIC 7 is located in proximity to the host computer. It allows high-speed host/GRAPHIC 7 communications with handshaking and can be operated in a DMA mode. If a parallel interface card is installed in the terminal controller, GCP+ assumes that it is connected to the host computer. Therefore, if serial communication with the host computer is desired, a parallel interface card cannot be connected to the processor bus.

NOTE

Normally, if a parallel interface port is used, a single parallel interface card (for the host computer) is installed in the terminal controller. For special applications, however, up to four parallel interface cards may be installed.

1.3.1.7 Graphic Controller. The graphic controller card is a microcontroller that controls generation of the image on the display indicator. Instructions used by the graphic controller are fetched via the processor bus from either the read/write or the read-only memory. The complete series of sequential instructions that defines any particular display image is referred to as a refresh file. These instructions are described in Sanders' "Graphic Control Program Enhanced (GCP+) Programmer's Reference Manual." See Appendix C.

The graphic controller may be considered as a device on the processor bus of the terminal controller. It contains its own set of registers that maintain instruction addresses, control fetch operations, and perform any branching that may be specified by non-graphic instructions. It also calculates relative data when required, loads data into appropriate registers, and initiates execution of refresh file instructions.

Status bits of the graphic controller are maintained by circuits on the ROM and status logic card (paragraph 1.3.1.2). These bits plus the graphic controller registers are accessible to the display processor (paragraph 1.3.1.1) which maintains control over the entire terminal controller.

1.3.1.8 2-D/3-D Coordinate Converter. The Model 5753 2-D/3-D coordinate converter converts a Sanders graphic display into a three dimensional display capable of independent dynamic manipulation of objects in apparent space. Among the functions provided by the Model 5753 are translation, scaling, rotation, windowing, independent display coordinate mapping, perspective, and zooming with perspective.

The perspective feature is especially useful for realistic viewing of an object. Utilizing perspective, the location of the viewer is defined relative to the image space, and all lines and objects within the image space are then viewed at the proper perspective for that location. The view may be completely orthographic if the viewer does not wish to use the perspective feature.

Objects can be defined within a 64K (X), 64K (Y), by 32K (Z) image space and presented on a 1K by 1K screen or any portion thereof. Translations can be made within the limits of the image space and scaling range is 64 to 1. Rotation can be provided about any axis.

3-D windowing, in conjunction with independent screen coordinate mapping, allows the presentation of any data within a software definable X, Y, Z image space to be presented on the full screen or any portion of the screen. Zooming is accommodated by scaling and changing the user's apparent perspective viewpoint.

Alphanumeric data can be moved about the screen with vector defined data without scaling and rotation.

The 5753 provides for both homogeneous and non-homogeneous matrix operation. Also, transformations of 2-D images can be accomplished including translation, rotation, scaling, and windowing.

Refer to Sanders' "2-D/3-D Coordinate Converter User's Manual" (see Appendix C) for programming instructions.

1.3.1.9 Floating-Point Converter. The model 5744 floating-point converter option transforms incoming floating point binary numbers into displayable numbers. The displayable numbers may be in any of sixteen formats selected by the host. The bi-directional converter also converts the displayed numbers into floating-point binary for transmission back to the host.

The floating-point converter saves host computer time and storage resources by performing these conversions within the graphic terminal. It allows data to be transmitted to and from the host in its most compact form and frees the host programmer from the conversion programming task.

The floating-point converter can perform more than 500 conversions per second, which allows it to be used in high data-rate applications resulting in significant off-loading of the host computer. Application and programming are described in Sanders' "Model 5744 Floating Point Converter User's Manual" (see Appendix C).

1.3.2 GROUP 2 CIRCUIT CARDS

1.3.2.1 Vector/Position Generator. The vector/position generator comprises three separate circuit cards on the graphic bus: a ramp generator and two digital-to-analog (D/A) converter cards. These cards operate together to produce CRT beam-positioning voltages as defined by digital X- and Y-coordinate instructions. They

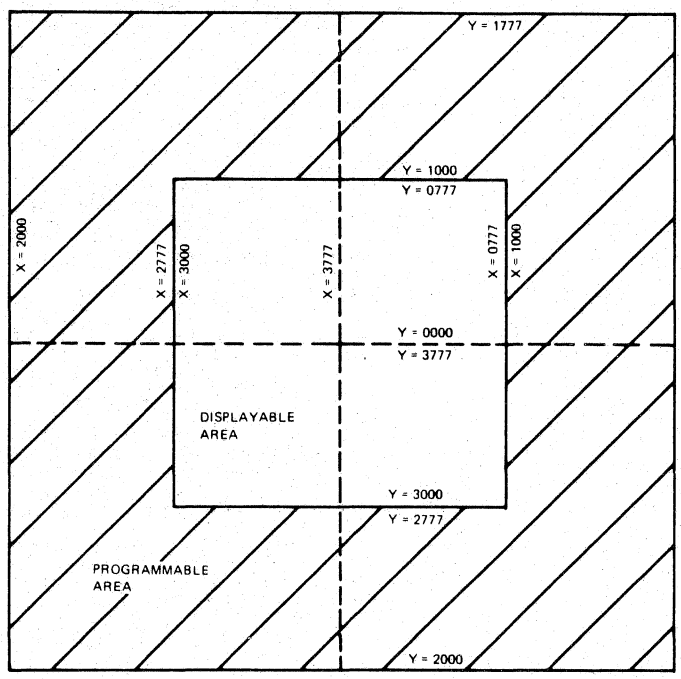
also generate unblanking signals to enable vectors to be drawn on the associated display indicators.

One D/A converter is used to address X coordinates on the face of the display indicator CRT while the second is used to address Y coordinates. Each D/A converter can address 2048 coordinates of which 1024 fall within the displayable area. The CRT beam is automatically blanked whenever it is moved to a coordinate that lies outside the displayable area. Refer to figure 1-8.

Beam positioning and vector drawing instructions may specify either absolute or relative data. Absolute data specifies the locations of particular coordinates whereas relative data specifies locations in terms of the distance moved from the previous location.

1.3.2.2 Character Generator. The character generator card contains read-only memories that store information for drawing characters in accordance with instructions received on the graphic bus from the graphic controller. The basic set of characters supplied with the character generator read-only memories is a standard set of 96 ASCII characters. When the ASCII code corresponding to the desired character is applied to the read-only memories, the character is drawn at the position determined by the vector/position generator.

As determined by instructions from the graphic controller, characters of four different sizes can be generated or characters can be made to blink. Characters may also be rotated 90 degrees counterclockwise to accommodate vertical writing requirements.



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NOTE

Coordinate designations are in octal format.

Figure 1-8. CRT Programmable vs. Displayable Areas

Space is provided on the character generator card for additional read-only memories so that characters in addition to the basic set of 96 can be generated. Read-only memories for six groups of 16 characters can be added to provide a total of up to 192 standard and special characters that can be produced by the character generator.

1.3.2.3 Ramp/Conic Generator. The ramp/conic generator is an optional card that may be connected to the graphic bus. It generates X-, Y-, and Z-axis waveforms that enable ellipses, or 90-degree segments thereof to be drawn on the display indicator. Ellipses may be centered at any addressable location on or off the CRT screen and are oriented so that their major and minor axes lie in parallel with the X and Y areas of the display indicator. The lengths of the axes are determined by instructions that specify semimajor and semiminor axis lengths for each ellipse. Semimajor and semiminor axis lengths are independently programmable from zero to half-screen.

Program control also permits any combination of 90-degree segments of an ellipse to be displayed. These segments are defined by the ellipse axes.

1.3.2.4 Output Channel. The output channel card contains four Z-axis output channels. Thus, up to four display indicators and/or hard copy units can be driven by one output channel card. Program control permits the four Z-axis outputs to be blanked and unblanked selectively so that the same or different images can be sent to each of the output devices as required.

Intensity control circuits and a blink oscillator are also located on the output channel card. Three bits under program control permit eight different intensity levels to be selected for the Z-axis outputs. A single bit enables or disables the blink oscillator.

When a four-color display indicator is used, the Z-axis output channels also carry the color select commands.

Additional functions performed by the output channel card include providing timing signals to the graphic controller and processing signals from PHOTOPENs. In normal system installations, each of the output devices connected to an output channel card can be located up to 50 cable-feet away with no degradation in performance.

1.3.2.5 2-D Coordinate Converter. A 2-D coordinate converter card is available as an option for the GRAPHIC 7. This option permits components of a displayed image to be rotated and/or translated on the CRT screen as determined by software instructions. Refer to Sanders' "Model 5752 2-D Coordinate Converter Technical Manual" (see Appendix C).

1.4 OPTIONAL EQUIPMENT

The following paragraphs describe the GRAPHIC 7 display indicator, input device, and output device options.

1.4.1 DISPLAY INDICATORS. Up to four display indicators (monochrome or 4-color) can be connected to one GRAPHIC 7 terminal controller.

The GRAPHIC 7 display indicator is a self-contained unit, available in the following configurations:

- Monochrome, 21-inch rectangular CRT, desk top, horizontal or vertical orientation
- Monochrome, 21-inch rectangular CRT, rack mount, horizontal or vertical orientation
- Monochrome, 23-inch round CRT, desk top or rack mount
- Four color, 21-inch rectangular CRT, desk top, horizontal or vertical orientation
- Four color, 21-inch rectangular CRT, rack mount, horizontal or vertical orientation
- Four color, 23-inch round CRT, desk top or rack mount.

The CRTs are available in a variety of phosphors. Refer to Appendix C for a list of display indicator technical manuals.

The rectangular CRT provides a standard 12- by 12-inch display area, which can be modified to a 12- by 16-inch display area. The display area of the round CRT has a 20-inch diameter.

Locations on the CRT screen are specified in terms of a matrix containing 2048 coordinates in the X dimension and 2048 coordinates in the Y dimensions. Two's complement notation is used to designate the coordinates with location 0, 0 being defined as the center of the CRT screen. Of the 2048 by 2048 addressable locations, the displayable area comprises the field of 1024 by 1024 coordinates centered about the middle of the CRT screen. Refer to figure 1-8.

1.4.2 INPUT DEVICES. Optional data input devices for the GRAPHIC 7 give the operator two-way interaction with the display and processing system. Input devices available include two types of keyboards, a PHOTOPEN, a trackball, a forcestick, and a data tablet. The GCP+ in firmware can support up to two keyboards, two PHOTOPENS, and two position entry devices (trackball, forcestick, or data tablet). In addition to the foregoing, a teletypewriter or paper tape reader can be connected to the GRAPHIC 7 for the input of maintenance data.

1.4.2.1 Keyboards. Standard keyboards available for the GRAPHIC 7 are the Model 5783 and Model 5784 keyboards. The keyboards contain a main block of alphanumeric keys plus a matrix and a row of function keys.

The Model 5783 keyboard offers an alphanumeric block of 58 keys. These keys generate standard seven-bit ASCII codes with an eighth (MSB) bit always set to 1. The alphabetic keys generate both upper and lower case codes. A four-by-four matrix of function keys is located to the right of the alphanumeric block and a row of 16 function keys is located immediately above the alphanumeric block. Each function key generates a single eight-bit octal code from 000 to 037.

An added feature of the Model 5784 keyboard is that each function key contains a LED that can be lighted or turned off as required under program control. The Model 5784 also has provisions for additional keys to the basic board. These keys are for future expansion and are located on both sides of the space bar.

The keyboards operate at a rate of 9600 baud and interface to the terminal controller via ports on the multiport serial interface card.

1.4.2.2 PHOTOPEN. The PHOTOPEN is a small hand-held device that detects light from data displayed on the CRT of a display indicator. Detected light is converted into an electrical impulse to identify the specific data at which the PHOTOPEN is pointed. The excellent resolving capability of the PHOTOPEN enables individual characters and even displayed points of light to be distinguished.

A switch in the PHOTOPEN is actuated when the PHOTOPEN is pressed against the CRT screen. Actuation of this switch causes the data sensed by the PHOTOPEN to be processed as determined by program control. GCP+ provided with the GRAPHIC 7 can support up to two PHOTOPENs.

1.4.2.3 Trackball, Forcestick, and Data Tablet. The trackball, forcestick, and data tablet are referred to as PEDs (position entry devices). These devices are used as determined by program control to move a cursor and/or data displayed on the CRT screen. Movement initiated by the trackball is proportional to the speed and direction in which the trackball is rolled. Movement initiated by the forcestick is proportional to the direction and force with which the forcestick is deflected. Movement initiated by a data tablet is proportional to the speed and direction in which the data tablet pen is moved along the data tablet surface. PEDs are connected to the system via ports on the multiport serial interface card(s) in the terminal controller.

1.4.2.4 Maintenance Data Input Devices. The teletypewriter and/or a paper tape reader can be connected to the GRAPHIC 7 to input data for maintenance purposes. The teletypewriter is normally connected to a port on the ROM and status card in the terminal controller while the paper tape reader is connected to one of the ports on a multiport serial interface card. The teletypewriter serves basically as a trouble-shooting aid. The paper tape reader is used to load special user or diagnostic programs into the GRAPHIC 7.

1.4.3 OUTPUT DEVICES. The standard output device for the GRAPHIC 7 is the CRT display indicator described in paragraph 1.4.1. A hard copy unit is available as an optional output device. Using the same signals that go to a standard display indicator, the hard copy unit can produce a duplicate on paper of any static image displayed on the CRT of the display indicator. Operation of the hard copy unit is controlled manually or by program control.

A hard copy multiplex switch is available as an optional device. The multiplex switch is capable of interfacing up to four GRAPHIC 7 units to a single hard copy unit. The multiplex switch generates copies on a first come, first served basis and requires no additional interfacing.

1.5 POWER AND ENVIRONMENTAL REQUIREMENTS

The terminal controller requires 250W of single-phase primary power. The power source must be within six cable-feet of the terminal controller.

The terminal controller fits a 10.5-inch vertical space in a standard 19-inch equipment rack, either directly or on slides. The controller can also be supplied as a stand-alone cabinet unit.

The operating environment temperature range is +15°C (59°F) through +40°C (104°F). The relative humidity should not exceed 90%.

1.6 PERFORMANCE SPECIFICATIONS

Table 1-2 lists the performance specifications for the overall terminal controller and its assemblies where applicable.

1.7 EQUIPMENT SUPPLIED

Table 1-3 lists the assemblies that comprise the terminal controller, including standard and optional items.

1.8 EQUIPMENT IDENTIFICATION

The part number of the terminal controller is a function of its card complement and thus varies from installation to installation. The Sanders identification plate at the rear of the terminal controller carries the part number, voltage rating, current rating, and UL, CSA, and VDE identification.

The part number of the card cage is 5976112G1.

Nomenclatures and part numbers for the circuit cards are etched on the component side of the cards. Serial numbers are stenciled next to part numbers.

All correspondence and documentation concerning the terminal controller or its assemblies should include full identification data.

1.9 RELATED PUBLICATIONS

This manual is one in a set of manuals available to support the GRAPHIC 7 system and its peripheral equipment. Other manuals in the set are listed in Appendix C.

1.10 TEST EQUIPMENT REQUIRED

The following equipment (or equivalent) is recommended for maintenance of the terminal controller:

Oscilloscope	Tektronix type 547 with type 1A1 preamplifier
Digital voltmeter	Fluke model 8000A
Multimeter	Triplett model 630
Card extender	Sanders part no. 1086794

Table 1-2. GRAPHIC 7 Terminal Controller Specifications

GENERAL	
Power source	100-120 Vac or 200-220 Vac 48-63 Hz
Power	250 Watts
Temperature, storage	0° to 50°C
Temperature, operating	15° to 40°C
Relative humidity	10 to 90%
Dimensions:	
Height	10.5 Inches
Width	19.0 Inches
Depth	16.0 Inches
Weight	55 Pounds

DISPLAY PROCESSOR	
General purpose microprocessor	Yes
Word length	16 bits
Byte mode	8 bits
Instructions	400 plus
Registers	8
Software stacks	Yes
Automatic priority interrupt	Yes
Memory	16 bits
ROM	8192 words
RAM	8192 words
RAM expansion to	131,072 words (less ROM)

INTERFACE OPTIONS (DIGITAL)	
Parallel	16 bits
Serial	RS-232C

VECTOR/POSITION GENERATOR	
Addressabe locations	2048 x 2048
Viewing area	1024 x 1024

VECTOR/POSITION GENERATOR (Cont)	
Line texture	4
Programmable speeds	2
Adaptive timing	Yes

CHARACTER GENERATOR	
Type	Cursive stroke
Character set (std)	96 ASCII
User defined (opt)	Up to 96
Aspect ratio	3:2 (normal)
Rotation	90° CCW
Character sizes	4
Tabular characters	Auto text spacing
High speed	2.4 µs (typical)
	3.0 µs (with tab)
Programmable speeds	2
Adaptive timing	Yes

OUTPUT CHANNEL	
Total displays	4
X channels	2
Y channels	2
Z channels	4
X, Y channels	-5V to +5V
Z channels (video)	0 to 1.5V
Z channels (color)	-1.5V pulses
Terminations (X and Y)	75Ω
Brightness levels	8
Blinking (adjustable)	0.5 to 5.0 Hz
PHOTOPEN intensifier	Yes

Table 1-3. Basic Components of the Model 7709 Terminal Controller

PART NUMBER	NOMENCLATURE	REQUIRED QUANTITY (BASIC)	OPTIONAL QUANTITY (MAXIMUM)
5976112	Card cage assembly	1	-
1088682	ROM and status card	1	-
5976251	Multiport serial interface card (option)	-	2
1089845	Graphic controller card	1	-
1086762	Read/write memory card (8K)	1**	3**
	Output channel card	1***	-
1086775	D/A converter card	2	-
1086779	Display processor card	1	-
1086783	Character generator card	1	-
1086798	Ramp generator card	1*	-
	Parallel interface card (option)	-	4
1086855	Extender card (option)	-	1
1086939	Ramp/conic generator card (option)	1*	1*
1086943	2-D coordinate converter card (option)	-	1
1089881	3-D coordinate converter card (option)	-	1
1089724	Large read/write memory (option)	-	2**
1088670	Floating point converter card (option)	-	1
5977053	Expansion module (option)	-	2

*The ramp generator card and the ramp/conic generator card are interchangeable. The system must have one or the other but cannot have both.

**The large read/write memory would replace the 8K read/write memory in any system needing more than 24K of RAM memory. (Possible configurations include: 32K, 48K, 64K, 80K, 96K, 128K.)

***Part number for monochrome is 1086771; for color, 5977409.

SECTION 2

OPERATION

2.1 GENERAL

This section contains information for operating the GRAPHIC 7 terminal controller. Topics discussed include: controls and indicators, turn-on procedure, and operation in the SYSTEM and LOCAL modes.

2.2 CONTROLS AND INDICATORS

Table 2-1 lists the terminal controller controls and indicators, their locations and functions. Figure 2-1 shows their location on the equipment. Circuit connections for the controls and indicators are shown on the applicable terminal controller diagrams in the Terminal Controller Diagrams Manual (H-78-0096).

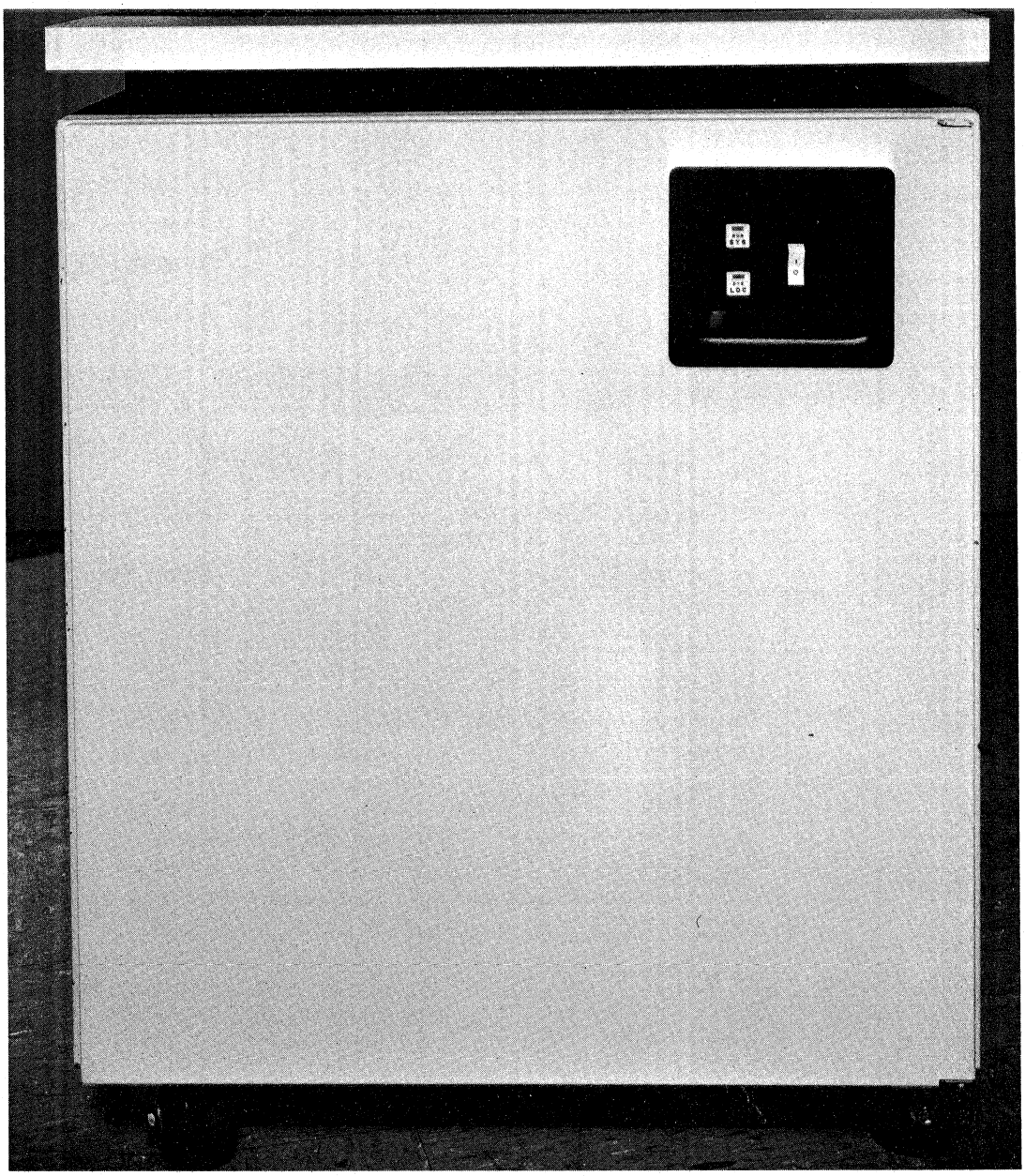
Table 2-1. Terminal Controller Controls and Indicators

NOMENCLATURE	LOCATION	FUNCTION
POWER ON/OFF circuit breaker	Top right of control panel	Energizes/deenergizes terminal controller
RUN/SYS pushbutton	Top right of control panel	Initiates SYSTEM mode (host computer control)
RUN/SYS lamp	In RUN/SYS pushbutton	Indicates display processor card operating
DIS/LOC pushbutton	Top right of control panel	Initiates LOCAL mode (GCP+/ operator commands)
DIS/LOC lamp	In DIS/LOC pushbutton	Indicates graphic controller card operating

2.3 TURN-ON PROCEDURE

NOTE

Refer to Section 5 for maintenance information if (a) RUN/SYS lamp does not light following power turn-on; (b) host computer subsequently reports terminal controller defective; or (c) terminal controller operation is suspect for any reason.



80-346-015

Figure 2-1. Terminal Controller Controls and Indicators

To turn the terminal controller on, press the 1 side of the POWER ON/OFF circuit breaker. This action lights the RUN/SYS lamp and applies power to the circuit cards.

Delay timers in the circuit cards allow initial power surges to settle, then initialize the terminal controller in the SYSTEM mode. All peripheral devices are reset, and the GCP+ performs automatic diagnostic tests to verify operation of the basic terminal controller functions.

If the terminal controller is connected to a host computer that is already operating, the controller automatically transmits a performance status report to the computer. If the host computer is not operating, the computer can receive this status report only by initializing the terminal controller as part of its own turn-on procedure. In either case, the host computer's response to the status report is a function of the host computer application software.

2.4 OPERATING PROCEDURES

The terminal controller has two types of operation:

1. Normal Operation: regular controller functions performed in the SYSTEM or LOCAL mode.

2. Checkout: operator test of controller operation.

2.4.1 NORMAL OPERATING PROCEDURES. After normal turn-on, the terminal controller is in the SYSTEM mode; i.e., under host computer control. Pressing the DIS/LOC pushbutton places the terminal controller in LOCAL mode, under GCP+ control and operator commands. The terminal controller remains in LOCAL mode until it is placed in SYSTEM mode again as described in paragraph 2.4.1.1.

2.4.1.1 SYSTEM Mode Operation. This mode is established when one of the following occurs:

1. When primary ac power is applied to the terminal controller.

2. When you press the RUN/SYS pushbutton.

3. When the terminal controller is in LOCAL mode and you type S on the keyboard.

4. When the terminal controller is in LOCAL mode and you type 157760G RETURN on the keyboard.

5. When an initialize signal comes from the host computer via the parallel interface or the multiport serial interface.

6. When the terminal controller is in the teletypewriter emulation mode (see paragraph 2.4.2.5) and you press function key F13 on the keyboard or the host computer sends octal code 035 (ASCII control character GS Group Separator).

If the terminal controller is already in SYSTEM mode, it can be initialized again by either of the following:

1. A discrete initialize signal from the host computer via the parallel interface or the multiport serial interface.

2. An IZ (initialize) message from the host computer.

Initialization in the SYSTEM mode automatically causes the built-in diagnostic routines to be performed and the results sent in an error status message to the host computer. The diagnostic routines include GO/NO-GO checks of the graphic controller, display processor, read/write memory, 2-D/3-D coordinate converter (if installed), and either the parallel interface or the multiport serial interface (whichever is the device used for communications with the host computer). The error status message also includes a checksum of GCP+ stored in read-only memory.

In the SYSTEM mode, responses to all operator actions are determined by the application program of the host computer. Control is exercised and data is transferred by means of messages sent between the host computer and the terminal controller. A complete description of available messages is presented in the Sanders publications listed in Appendix C.

The host computer application program accesses all display registers and parameters for organization of display images. The initialization sequence enables the associated keyboards so you can enter commands without special action by the host computer.

The GCP+ handles all internal display interrupts and operator inputs, including PHOTOPEN strike and switch signals. The GCP+ performs all housekeeping required for these events, and sends the host computer a message containing all information needed for operational decisions. However, the host computer can preset the terminal controller to transmit only specified signals under specified conditions.

The GCP+ processes trackball, forcestick, or data tablet inputs without host computer intervention. The GCP+ detects all PED (position entry device) inputs and either transmits them to the host computer, or uses them to update the position of a predefined PED identifier symbol on the display. GCP+ processing of PED symbols is controlled by the host computer application program.

GCP+ also inserts alphanumeric data from the keyboard into the refresh pattern; you can enter and edit a message without host computer intervention. You complete your entry by pressing the RETURN key, and GCP+ informs the computer that a new message is ready. The application program indicates how alphanumeric inputs are handled by issuing special commands.

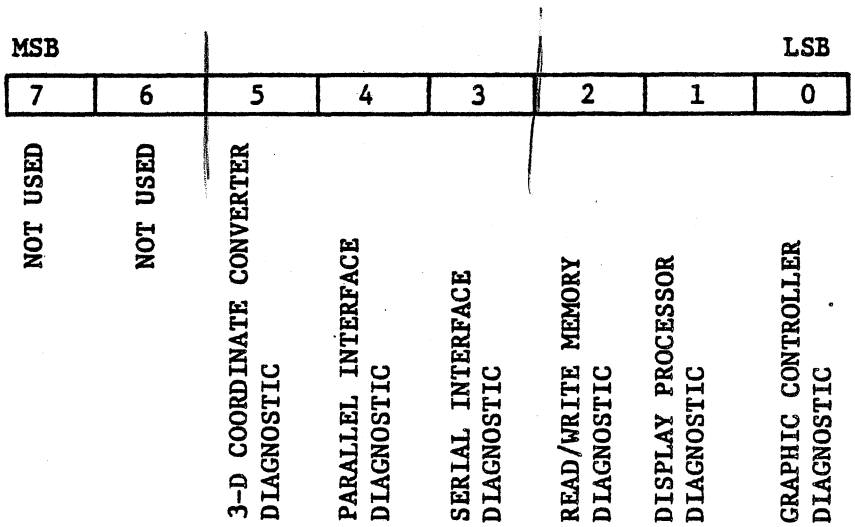
2.4.1.2 LOCAL Mode Operation. After primary power has been applied to the terminal controller, you can initialize the terminal controller in LOCAL mode by pressing the DIS/LOC pushbutton. When you press this pushbutton, the verification test pattern appears on each of the associated display indicators, the terminal controller performs its built-in diagnostic routines, and local mode commands can be executed.

NOTE

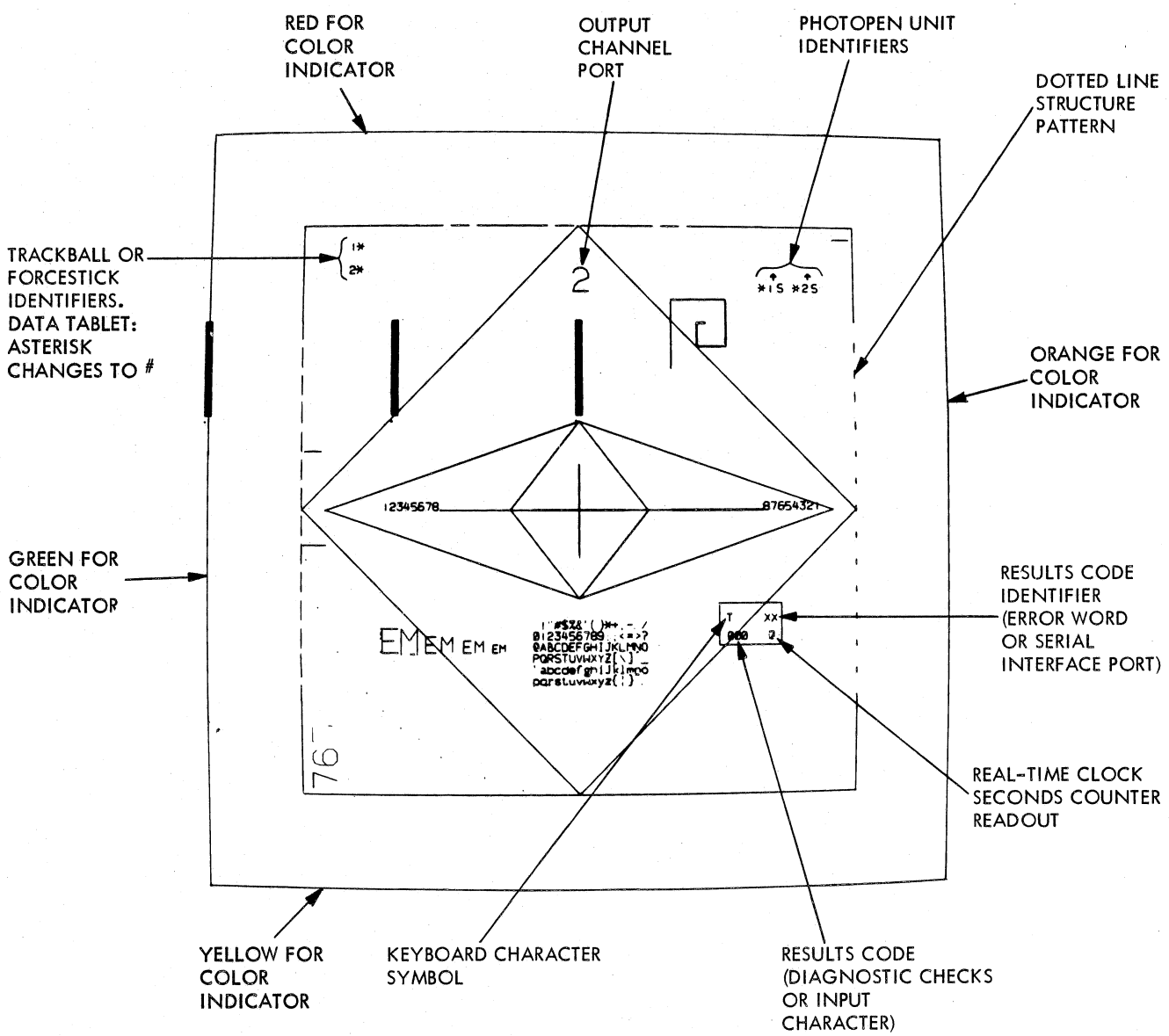
When you press the DIS/LOC pushbutton, the built-in diagnostic exercises the complete memory system. For systems containing more than 32K of memory, it may take several seconds before the terminal verification pattern appears. As part of the memory diagnostic, the memory configuration installed in the terminal controller is saved and can be examined if desired. Address 736 contains the RAM configuration word; address 750 contains the ROM configuration word.

2.4.1.3 Verification Test Pattern and Diagnostics. Figure 2-2 shows the verification test pattern that is displayed on each display indicator when the terminal controller is initialized in the LOCAL mode. The pattern remains displayed until terminated by the proper command or until 45 minutes have elapsed since that last performed operation that affected the pattern.

When the system is first initialized in the LOCAL mode, 'XX' appears in the small box in the lower right portion of the pattern. The 'XX' indicates that the code appearing in the same box contains the results of the built-in diagnostic routines that were automatically performed. The diagnostic code is a three-digit octal representation of an eight bit binary code that indicates the results of each diagnostic routine. Bits in the binary code are assigned as follows:



When a diagnostic routine detects a malfunction, the corresponding bit in the error code is set to a 1; if no malfunction is detected, the bit is set to a 0. The octal code displayed in the verification test pattern then tells you the results of all the diagnostic tests. For example, 000 indicates all tests passed, 002 indicates the display processor diagnostic test failed, 030 indicates the serial and the parallel interface diagnostic tests failed, and 077 indicates that all diagnostic tests failed.

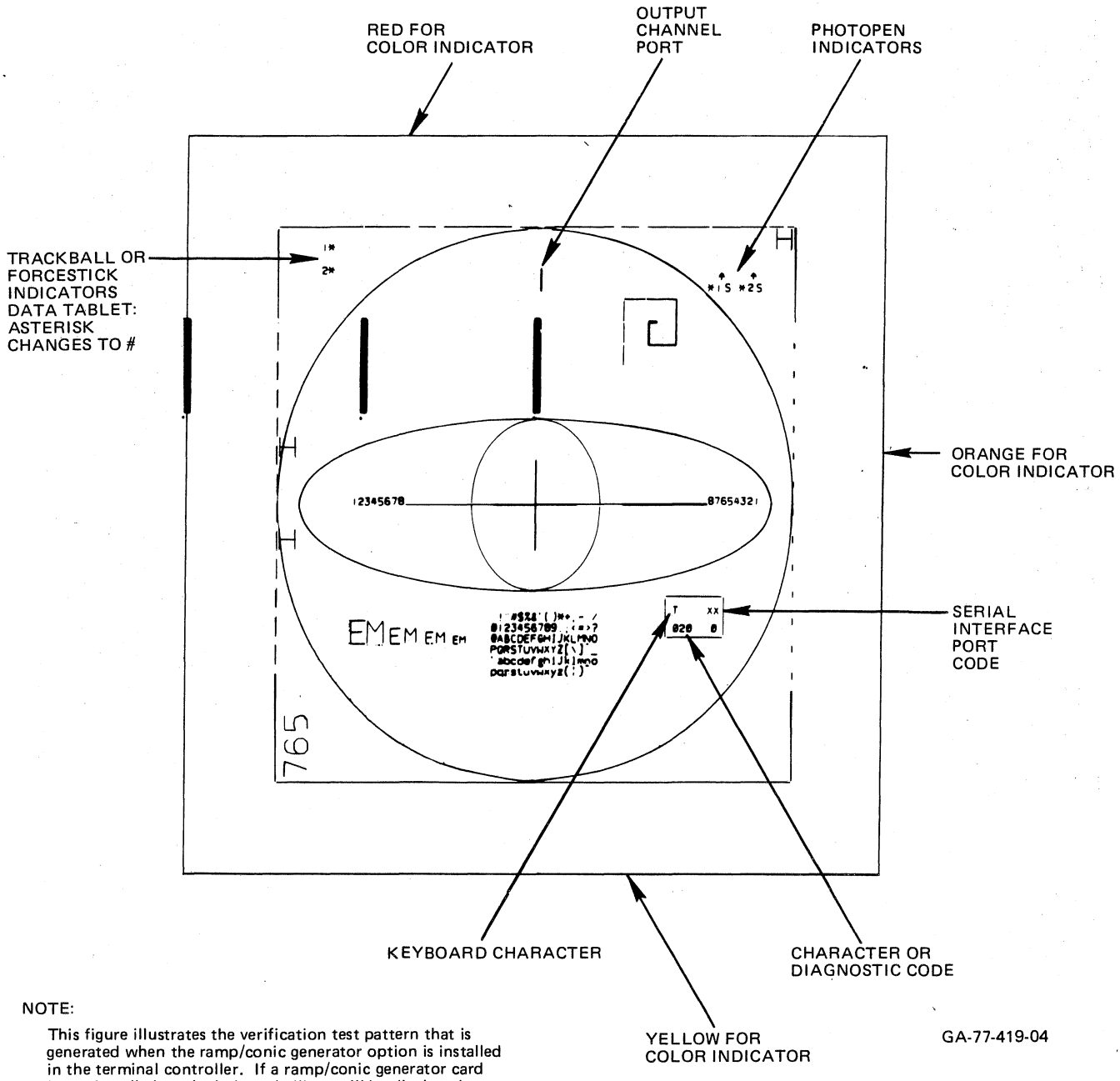


NOTE:

This figure illustrates the verification test pattern that is generated when the standard ramp generator card is installed in the terminal controller. If an optional ramp/conic generator card is substituted, the three innermost diamonds will be displayed as a circle and two elipses.

H-78-0095-041 REV A

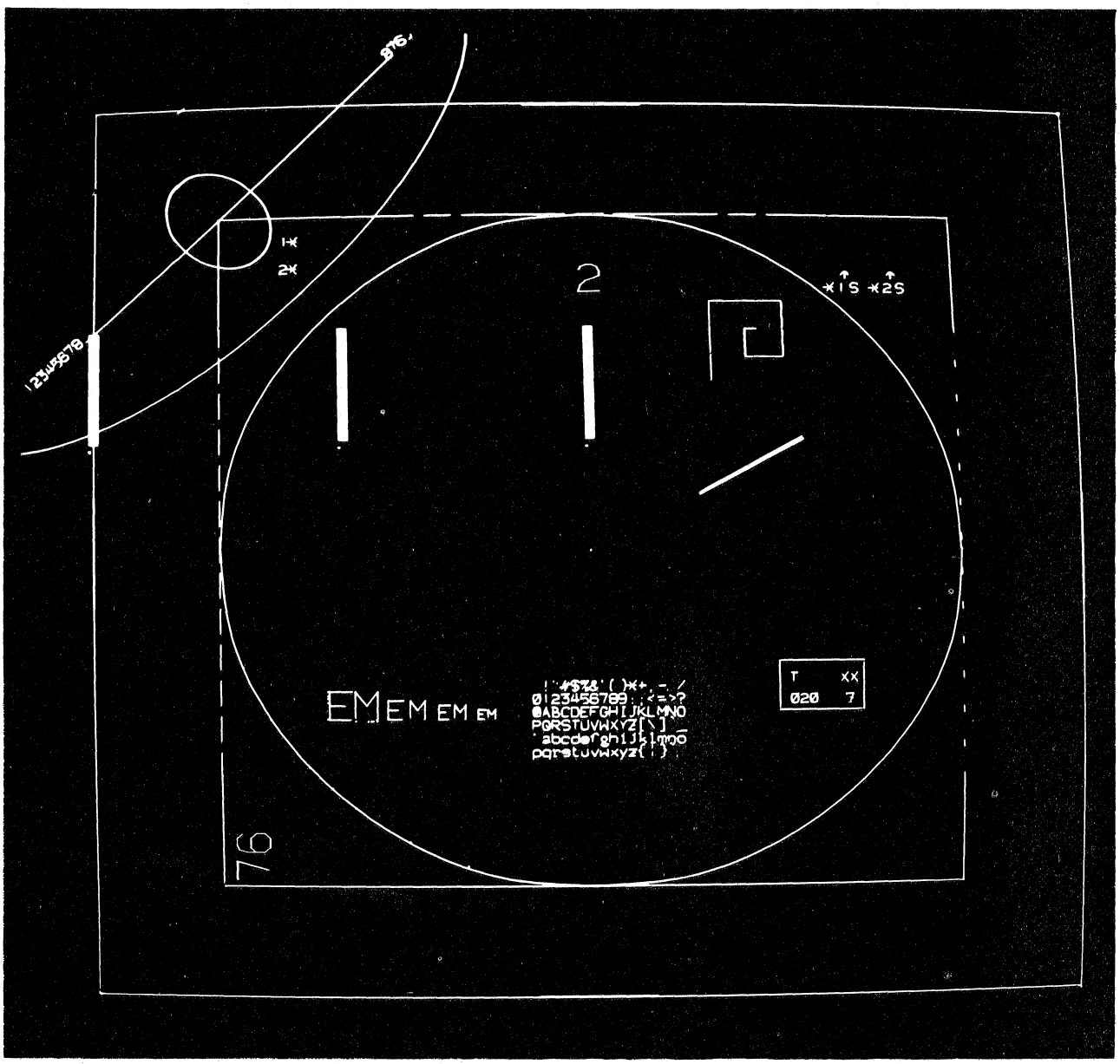
Figure 2-2. Verification Test Pattern (Sheet 1 of 3)



NOTE:

This figure illustrates the verification test pattern that is generated when the ramp/conic generator option is installed in the terminal controller. If a ramp/conic generator card is not installed, each circle and ellipse will be displayed as four straight lines. If a 2-D coordinate converter card is installed in the terminal controller, all information contained within the ellipse will be rotated, translated and displayed at the top left of the display.

Figure 2-2. Verification Test Pattern (Sheet 2 of 3)



NOTE

This figure shows the verification test pattern with ramp/conic generator and 2D coordinate converter installed.

Neg. No. 78-202-2

Figure 2-3. Verification Test Pattern (Sheet 3 of 3)

An additional routine performed whenever the GRAPHIC 7 is initialized in the local mode is a checksum calculation based on all GCP+ stored in read only memory. You can examine the result, which is deposited in memory 5ØØ (octal), as described in paragraph 2.4.2.1.

As soon as the terminal controller receives any input via a serial interface port, the "XX" in the small box is replaced by a code that indicates the port to which the input device is connected. Codes associated with each serial interface port are shown in table 2-2.

When the serial interface port designation is displayed in the small box, the three digit octal code in the box indicates the code last transmitted to the terminal controller. Also, if the code represents a displayable character, the character appears in the upper left corner of the box. If the code does not represent a displayable character, the upper left corner of the box is blank. In systems using SI (shift-in) and SO (shift-out) codes to identify characters in an extended set, the SI character is displayed over the left hand digit of the code and the SO character is displayed over the right hand digit.

The test results box also contains a single-digit real-time clock counter readout in the lower right corner. This counter increments from 0 through 7 continuously at a 1-Hz rate to confirm operation of the real-time clock timing function.

The numeral in the upper center of the verification test pattern indicates the port on the output channel card to which the Z axis of the display indicator is connected. Connectors J5 through J8 on the output channel card correspond to indicators 1 through 4, respectively.

Table 2-2. Serial Interface Port Codes

CODE	SERIAL INTERFACE PORT	DEVICE	ASSOCIATED CONNECTOR
F1	3	Keyboard (with function keys)	J5 on multiport serial interface card no. 1
F2	7	Keyboard (with function keys)	J5 on multiport serial interface card no. 2
TT	TTY	Teletypewriter	J2 on ROM and status card
S1, S5	1 or 5	Any	J2 or J3 on multiport serial interface card no. 1 or no. 2
HC	5	Hardcopy	J3 on multiport serial interface card no. 2.

NOTE

No indicator code is provided for ports 4 or 8. These ports are normally used for PEDs which have separate indicators on the test pattern.

Trackball (or forcestick) indicators appear in the upper left corner of the verification test pattern. The "1*" indicator is associated with the device normally connected to serial interface port 4 (J6 on multiport serial interface card no. 1) while the "2*" is associated with the device normally connected to serial interface port 8 (J6 on multiport serial interface card no. 2). These indicators are always displayed on the test pattern regardless of whether or not a trackball or forcestick is connected to the system. If a trackball or forcestick is connected to port 4 or 8, it can be manipulated to move its associated indicator about the screen of the CRT as desired. (See paragraph 2.4.1.5 for data tablet.)

PHOTOPEN indicators are displayed in the upper right corner of the verification test pattern. The "*1S" with an arrow is associated with a PHOTOPEN connected to the PPN1 connector on the front of the terminal controller. The "*2S" with an arrow is associated with a PHOTOPEN connected to the PPN2 connector. Like the trackball/ forcestick indicators, the PHOTOPEN indicators appear on the verification test pattern whether or not PHOTOPENs are connected to the system.

If a PHOTOPEN is connected to the system, its associated indicator responds as light from various data items is sensed by the PHOTOPEN. Whenever an item of data is sensed, the sensed point is intensified and the indicator moves so that the arrow points to the location at which the data item ends. Alphanumeric data is normally stored with two characters per data item. Therefore, the arrow always points to the end of the second character in a pair. If the PHOTOPEN is also pointed at the character, an asterisk is added to the indicator. When the PHOTOPEN is pointed at the first character in a pair or at a non-character data item, the asterisk is removed from the indicator.

The "S" in each indicator provides an indication of PHOTOPEN switch operation. When you actuate the switch by pressing the PHOTOPEN against the CRT screen, the "S" is removed from the indicator. Pressing the switch a second time causes the "S" to reappear with the indicator.

NOTE

The complete character set is displayed at the bottom center of the terminal verification pattern. In this area all characters are insensitive to PHOTOPEN strikes.

2.4.1.4 Hardcopy Generation. You can make a hardcopy of the terminal verification pattern by pressing function key FØ on the keyboard. When you press this key, an HC appears in the serial interface port code. The HC indicates that a hardcopy request has been initiated. Successful generation of a hardcopy is indicated by the display of the characters S5 in the serial interface port code and the number 000 in the character or diagnostic code section of the terminal verification pattern. If the hardcopy request is unsuccessful, the characters HC remain displayed in the serial interface port code.

If a hardcopy multiplex switch is connected to the terminal controller, successful generation of a hardcopy is indicated as previously described. If the hardcopy request is unsuccessful, the characters S5 are displayed in the serial interface port code and the numbers 377 are displayed in the character or diagnostic code section of the terminal verification pattern. The 377 code indicates the hardcopy unit is either off-line or busy.

NOTE

The generation of hardcopies takes approximately 10 seconds. To generate hardcopies remotely with function key FØ requires that a serial cable be connected between port 5 (multiport serial interface No. 2) and the hardcopy. The X, Y, Z cables must also be connected between the output channel card and the hardcopy unit or hardcopy multiplexer unit.

2.4.1.5 Data Tablet Testing. You can test the data tablet by pressing function key F1. This causes the 1* and 2* trackball/forcestick indicators to change to 1# and 2#. The 1# and 2# symbols indicate that all messages received via ports 4 and 8 are in data tablet format. (Data tablet messages consist of 10 characters messages, whereas the trackball and forcestick generate 2-character messages.) When you press the data tablet pen switch and move the pen along the active area of the data table surface, the appropriate cursor symbol (1# or 2#) moves at a rate proportional to the movement of the pen. The 1# symbol is associated with the data tablet connected to port 4 and the 2# symbol is associated with the data tablet connected to port 8.

NOTE

Successively pressing function key F1 causes the terminal verification pattern to switch from processing data tablet messages to trackball/forcestick messages and vice versa.

2.4.2 LOCAL MODE COMMANDS. After the GRAPHIC 7 has been initialized in the LOCAL mode and the verification test pattern is no longer required, you can terminate the pattern by pressing the RETURN key on the keyboard. The pattern then disappears and the letters "BØ M" are displayed in the center of the CRT screen as an indication that the system is in the LOCAL MONITOR mode. At this point, you can perform any of several operations that let you monitor or debug a program, transfer control, or communicate with the host computer.

NOTE

Commands are executed when you press the RETURN key on the keyboard.

The following paragraphs discuss commands that can be executed when the system is in the LOCAL MONITOR mode. Table 2-3 is a summary of the commands.

Table 2-3. Local Mode Command Summary

KEYBOARD ENTRY	OPERATION
RETURN	Executes LOCAL mode command or returns system to LOCAL MONITOR level.
nnnnnn/	Displays contents of memory address nnnnnn (octal).
/	Increments memory address counter by two and displays address contents.
^ or ↑	Decrements memory address counter by two and displays address contents.
Bn	Select different memory bank. (BØ 0-32K; B1 32-64K; B2 64-96K; B3 96-128K; and B4 16-32K RAM).
S	Transfers GRAPHIC 7 to SYSTEM mode operation.
T RETURN	Transfers to the verification test pattern.
L RETURN	Loads memory from paper tape reader.
nnnnL RETURN	Loads selected option from expansion module
U RETURN	Unload all options.
O RETURN	Display status of all options loaded.
Q	Decrements contents of display processor Q register by two and displays result. Used with diagnostics to indicate address at which display processor halted.
nnnnnnD RETURN	Directs graphic controller to display refresh file beginning at address nnnnnn (octal).
nnnnnnG RETURN	Transfers control of display processor to program beginning at memory address nnnnnn (octal).
Y RETURN	Calls teletypewriter emulation program. After entering emulation program, function key FØ clears CRT screen. Function key F1 selects full or half duplex operation; receipt of octal code 035 from the host computer or pressing function key F13 transfers GRAPHIC 7 to SYSTEM operating mode.
RUB OUT	Deletes last octal entry from keyboard.

2.4.2.1 Memory Commands. You can display the content of a memory location by typing the octal address (typing of leading zeros is not required) followed by a slash (/). As soon as you type the slash, the content of the memory location is displayed immediately to the right of the address. You can examine successive memory locations by simply pressing the slash key. Each time you press the slash key, the memory address is incremented by two and its content displayed immediately to the right of the slash.

After you have used the slash key to examine the content of a memory location, you can use the up arrow (↑ or ∧) key in a similar manner to examine preceding memory locations. Each time you press the up arrow key, the memory address is decremented by two and its content displayed immediately to the right of the slash.

You can change the content of a memory location after you have examined it by typing the new data (typing of leading zeros is not required) before pressing the slash or up arrow key. The new data is displayed to the right of the old data and is automatically substituted when the slash or up arrow key is pressed.

You can examine or change memory locations in other banks via the bank (B) select command. Typing BØ, B1, B2, B3, or B4 changes the memory bank selection to bank Ø, bank 1, bank 2, bank 3, or bank 4 respectively. Below is a table representing the associated virtual and physical addresses for each bank.

Bank Number	Virtual Address	Physical Address	Pages
0*	000000-177777	000000-177777	00-07
1	000000-177777	200000-377777	10-17
2	000000-177777	400000-577777	20-27
3	000000-177777	600000-777777	30-37
4*	100000-177777	100000-177777	04-07

NOTE

*Addresses in the range of 100000-177777 (pages 4, 5, 6, and 7) for bank Ø correspond to ROM and I/O device registers. Addresses in the range of 100000-177777 for bank 4 correspond to RAM.

You can return to the monitor level by pressing the RETURN key. When you press this key, any specified memory content change is completed and the system returns to monitor level as indicated by letters "BO M" displayed at the center of the CRT screen.

2.4.2.2 Displaying a Refresh File. When the system is in the local monitor mode, you can display the contents of a refresh file by typing the starting address of the file (in octal notation) followed by a "D" and then pressing the RETURN key. This command instructs the graphic controller to display the entire refresh file that begins at the specified address. Display of the refresh file continues until you press RETURN key again, at which time the system returns to the local monitor level. This command is subject to the bank argument presently displayed.

2.4.2.3 Transfer of Program Control. You can transfer program control from local monitor level to any desired address location in bank Ø by typing the address location in octal notation followed by a "G" and then pressing the RETURN key. The display processor then executes instructions beginning with the instruction at the specified address. Any further operations depend on the program in which control is transferred.

2.4.2.4 Transfer to System Mode. To transfer to the system mode of operation from monitor, level, type "S". This command has the same effect as pressing the RUN/SYS pushbutton on the terminal controller. After transferring to the system mode, operation in the local mode can be reestablished only by a message from the host computer or by pressing the DIS/LOC pushbutton on the terminal controller.

2.4.2.5 Teletypewriter Emulation. For purposes of communicating with a host computer, the GRAPHIC 7 can be made to emulate the functions of a teletypewriter. In this mode, the keyboard operates like the keyboard of a teletypewriter and the display indicator serves as the printout device. Scrolling of data on the display indicator is handled on a half-page basis. That is, when the CRT screen is full, the top half of the data is deleted from the display and the bottom half of the data moves up to take its place.

If a parallel interface card is installed in the terminal controller, the graphic control program assumes that communications with the host computer are to be handled over the parallel interface. In this case, teletypewriter emulation signals are transmitted in parallel using only the low order byte (bits 0-7) of the 16-bit interface. If a parallel interface card is not installed, a standard 8-bit serial interface via serial interface port 1 is assumed. In either case, bit 7 is always equal to zero.

You enter the emulation program from the monitor level by typing the letter "Y" followed by RETURN. Full-duplex or half-duplex emulation may then be selected by pressing function key F1 which changes the selection each time it is pressed. The type of emulation selected is indicated by the "TTY F" (full duplex) or "TTY H" (half duplex) that is displayed at the top of the CRT screen at all times during emulation. You can switch between full and half duplex operation at any time during emulation by pressing function key F1. Pressing function key FØ during teletypewriter emulation clears the CRT screen.

Exit from the teletypewriter emulation program occurs when octal code 035 (ASCII control character GS Group Separator) is received from the host computer. This code, which can also be generated by pressing function key F13, immediately causes the GRAPHIC 7 to transfer to the SYSTEM mode of operation. Return to the LOCAL MONITOR level can be achieved only by a command from the host computer or by pressing the DIS/LOC pushbutton on the terminal controller.

2.4.2.6 Additional Local Mode Commands. Additional commands that you can use when the GRAPHIC 7 is in the LOCAL mode at the monitor level are the L, U, O, T, Q, and RUB OUT commands. The L command enables the memory to be loaded from a paper tape reader connected to the terminal controller. After the tape has been placed in the reader, loading is initiated by typing the letter "L" followed by RETURN.

NOTE

A paper tape reader may be connected to multiport serial interface card ports 1, 2, or 3 or to the serial interface port on the ROM and status logic card.

You also use the L command to load in options from the expansion module. The option command format is as follows:

nnnnL RETURN

where nnnn is the option number. Valid option numbers are in the ranges of 1 to 3777 and 4001 to 7777.

NOTE

The optional expansion module can store a variety of option types.

The U command is used to unload all options. Typing "U" followed by RETURN unloads all options.

The O command is used to detect the presence and status of all loaded options. Typing O followed by RETURN causes the display of the first option loaded. Successively pressing the RETURN key causes the display of all other options loaded. The option status is displayed in the following format.

nnnn ss

where nnnn is the option number and ss is the option status

The option status code is as follows:

00 Detected but unloaded
01 Unloaded, checksum error (local)
11 Unloaded, checksum error (system)
02 Unloaded, checksum OK, hardware not present (local)
12 Unloaded, checksum OK, hardware not present (system)
03 Unloaded, checksum OK, self-test = no go (local)
13 Unloaded, checksum OK, self-test = no go (system)
04 Loaded, checksum OK, self-test = go (local)
14 Loaded, checksum OK, self-test = go (system)

You use the T command to recall the verification test pattern when the system is at the local monitor level. This command is executed by typing the letter "T" followed by RETURN. The effect is the same as pressing the DIS/LOC pushbutton on the terminal controller. Pressing RETURN a second time causes the system to return to the monitor level.

The Q command is a special command used for diagnostic and debugging purposes. Whenever a HALT instruction is executed by the display processor, the content of the program counter is stored in the Q register of the display processor. After you have reinitialized the system by pressing the DIS/LOC pushbutton on the terminal controller, you can use the Q command to display the address at which the display processor halted. The Q command is executed by typing the letter "Q". This causes the content of the Q register to be decremented by two and the result displayed to indicate the address of the HALT instruction. Note that the Q command always decrements the content of the Q register by two and displays the result. The result, however, is only meaningful immediately following initialization in the LOCAL mode after a HALT instruction has been executed. After using a Q command, pressing RETURN returns the system to the local monitor level.

The RUB OUT command provides a means of correcting erroneous entries from the keyboard. At any time before a command is executed, pressing RUB OUT causes the last keystroke entry to be deleted. An additional entry is deleted each time the RUB OUT key is pressed.

2.4.3 STANDARD TRANSFER TABLE. ROM addresses 157700 through 157770 (octal) constitute a standard transfer table for certain routines of the graphic control program (GCP+). Information identifying the version of GCP+ installed in the ROM is also contained in these addresses. When the GRAPHIC 7 is operating in the LOCAL mode, you can examine the contents of locations containing information by typing the address of the location followed by a slash. To transfer to one of the GCP+ routines, the G command should be used as described in paragraph 2.4.2.3. Table 2-4 lists the addresses in the standard transfer table and identifies the information or routine associated with each.

NOTE

When the GRAPHIC 7 is operating in the SYSTEM mode, transfer to one of the GCP+ routines can be accomplished by using a host-to-GRAPHIC 7 TK message. Refer to H-79-0348 for details.

2.4.4 OPERATOR PERFORMANCE CHECKS. If you suspect a malfunction in the terminal controller or any of its peripherals (or if the host computer reports the terminal controller to be defective), you can perform the following procedure to verify basic system operation. If you do not get the described results, refer to Section 5.

1. Press the DIS/LOC pushbutton to initialize LOCAL mode. Confirm that the verification test pattern (figure 2-2) is present on the display indicator.

2. Confirm that the test results box shows a 000 value (code for all tests passed), with the "XX" error word code displayed in the upper right corner of the box.

3. Confirm that the seconds counter at the lower right corner of the test results box runs continuously through an 8-count cycle (0-7).

4. Confirm that the letter "T" appears in the upper left corner of the test results box.

Table 2-4. Standard Transfer Table

ADDRESS (OCTAL)	INFORMATION OR ROUTINE	REMARKS
157700	GCP+ date (year and month)	High order byte indicates month in octal form. Low order byte indicates last two digits of year in octal form (e.g., 003115 indicates June 1977).
157702	GCP+ date (day)	Day of month is indicated in octal form.
157704	GCP+ release number	Release number is indicated in octal form.
157706	Number of GCP+ field changes	Number of field changes is indicated by the number of bits set to 1 (e.g., 000007 indicates three field changes).
157710	ZERO	Maintenance routine. Graphic controller sets X and Y positions at zero (center of CRT screen) and then halts. Used for voltmeter adjustment of vector/position generator output voltages.
157720	PLUS	Maintenance routine. Graphic controller sets X and Y positions at maximum on-screen positions (upper and right corner) and then halts. Used for voltmeter adjustment of vector/ position generator output voltages.
157730	MINUS	Maintenance routine. Graphic controller sets X and Y positions at minimum on-screen positions (lower left corner) and then halts. Used for voltmeter adjustment of vector/position generator output voltages.
157740	LOADER	Enables a file to be loaded into read/ write memory from various input devices.
157750	DEBUG MODE	Enables local mode commands to be executed.
157760	SYSTEM MODE	Enables system mode.
157770	TEST PATTERN	Transfers to verification test pattern.

5. Press one or more alphanumeric keys on the keyboard. Confirm that:

   a. The alphanumeric symbol replaces the letter "T" in the upper left corner of the test results box.

   b. The applicable ASCII value in octal format replaces the test results value below that symbol.

   c. The appropriate source code (table 2-2) replaces the "XX" code.

6. Confirm that a full library of alphanumeric and special symbols is displayed at the lower center of the verification test pattern.

7. Confirm that four different sized sets of "EM" letter pairs are displayed in the lower left quadrant of the verification test pattern.

8. Confirm that the line structure of the overall test pattern conforms with the pattern shown in figure 2-2 with respect to the following:

   a. The corners of the displayed squares are clearly defined right angles, with uniform intensity through the points of congruence in all four corners.

   b. The central portions of the sides of the inner square represent different line structure patterns: solid (bottom), dotted (right), dashed (left), and centerline (top).

   c. The short vector segments that make up the broken pattern in the middle of the upper right quadrant have fairly uniform intensity.

   d. The 1/8-, 1/4-, and 1/2-screen position bars in the upper left quadrant each contain nine parallel lines, with no observable offset at the tops or bottoms of these lines.

9. Confirm that the number of the output channel port associated with a specific display indicator appears in the upper center of the pattern, continuously blinking on and off.

10. Confirm that the trackball/forcestick/data tablet identifier symbols are initially presented in the upper left corner of the pattern, with the applicable symbol moving as appropriate for any PED displacement inputs.

11. Confirm that the PHOTOPEN identifier signals are initially presented in the upper right corner of the test pattern with the applicable symbol moving as appropriate for any strike inputs, and responding appropriate ("S" character disappearing or reappearing) each time you press the PHOTOPEN switch.

12. In the case of a four-color display, confirm that the proper colors are displayed as shown in figure 2-2.

2.5 TURN-OFF PROCEDURE

To turn off the terminal controller, press the O side of the POWER ON/OFF circuit breaker.

SECTION 3

THEORY OF OPERATION

3.1 GENERAL

This section contains the theory of operation for the terminal controller functional circuits. Topics presented are the terminal controller signal/bus structure, and block-diagram level discussions of each standard circuit card assembly. Unique circuit card options are covered in separate manuals (see Appendix C).

The signals used in the terminal controller and the mnemonic conventions for these signals are presented in Appendix A of this volume.

3.2 SIGNAL/BUS STRUCTURE

Terminal controller inputs are provided as digital signals from a host computer or peripheral equipment. Except for PHOTOPEN inputs, all inputs are applied to the terminal controller circuits via edge-mounted connectors on the front of one or more interface cards located in the terminal controller card cage.

Terminal controller outputs are applied either as digital signals through the same edge mounted connectors or as analog signals to the associated CRT display indicators (or hard copy unit) through BNC connectors on the front of the output channel card. All interconnections among the various circuit card assemblies are accomplished through backplane wiring (see backplane wiring diagram in H-78-0096). For convenience, backplaning connections common to groups of cards are called buses. The three main terminal controller buses are: the processor bus, graphic bus, and power bus.

3.2.1 PROCESSOR BUS. The processor has comprises backplane wiring connections common to the display processor circuit card and all circuit cards that interface with the display processor to perform the digital analysis that creates display files. These cards (the processor subsystem) are located in card cage slots 1A1XA1 through 1A1XA10. The ROM and status card and the graphic controller card both have discrete-line backplane connections to circuit cards in the graphic subsystem and therefore occupy specific locations: 1A1XA9 and 1A1XA10, respectively. All other processor subsystem cards interface through the common processor bus connections, and can occupy any card cage slot depending on the interrupt/bus control priority. Table 3-1 lists the standard cards in their preferred priority arrangement.

Table 3-2 lists the processor bus signals and identifies their basic functions. For convenience, these signals are discussed as three separate buses: the 18-line processor address bus (AD00-B through AD17-B), the 16-line processor data bus (DA00-B through DA15-B), and the 25-line processor control bus.

Table 3-1. Processor Subsystem Cards, Preferred Priority Arrangement

CARD CAGE SLOT	CIRCUIT CARD ASSEMBLY	
1A1XA1	8K Read/Write Memory No. 1	May be replaced by one or two optional large (16K/32K/64K) read/write memory cards and expansion module.
1A1XA2	8K Read/Write Memory No. 2 (Optional)	
1A1XA3	8K Read/Write Memory No. 3 (Optional)	
1A1XA4	Digital Option	
1A1XA5	Digital Option	
1A1XA6	Parallel Interface (Optional)	Any system usually has one or both of these interface cards--and may have more than one of either of them.
1A1XA7	Multiport Serial Interface (Optional)	
1A1XA8	Display Processor	
1A1XA9	ROM and Status	
1A1XA10	Graphic Controller	

Table 3-2. Processor Bus Signals

CARD PIN	MNEMONIC	SIGNAL NAME	FUNCTION WHEN ACTIVE
		PROCESSOR ADDRESS BUS	
57 thru 74	ADnn-B	Address bus bits (AD00-B thru AD17-B)	Selects circuit in which an operation is to be performed
		PROCESSOR DATA BUS	
13 thru 28	DAnn-B	Data bus bits (DA00-B thru DA15-B)	Carries 16-bit data or control code to or from circuit that was addressed
		PROCESSOR CONTROL BUS	
4, 5, 6*	INLn-B	Interrupt levels 5, 6, 7	Three priority levels for interrupt selection; set by jumpers on each card

*All listed signals are common to all processor subsystem card slots 1A1XA1 through 1A1XA10, except that asterisked signals do not connect to graphic controller 1A1XA10. The asterisked signals pertain mostly to program interrupt handshaking signals. Graphic controller 1A1A10 does not interrupt the processor program directly. Certain of its operations can interrupt the program through status connections to ROM and status card 1A1A9.

Table 3-2. Processor Bus Signals (Cont)

CARD PIN	MNEMONIC	SIGNAL NAME	FUNCTION WHEN ACTIVE
7*	IREQ-D	Interrupt request pulse	Produced by display processor at end of each instruction cycle to let any card that is ready to interrupt the program activate its INLn-B output
8*	IENA-D	Interrupt enable	Produced by display processor in response to INLn-B signal to let the requesting card generate an interrupt
9*	IADV-B	Interrupt address valid	Produced by interrupting card to let display processor read interrupt trap address; response to IENA-D
10, 11, 12, 3*	DEV-nB	Device code levels 0, 1, 2, 3 (BCD)	Identifies (by unique BCD code) the card that has control of the bus
31	CLOK-F	10 MHz clock	Master clock for GRAPHIC 7 system
33	BUSB-B	Bus busy	Indicates that bus is under control of some processor subsystem card
36	GRAI+B	Grant input	Lets receiving card gain control of bus (comes as GRAO+B from higher priority card)
35*	GRAO+B	Grant output	Lets lower priority card gain control of bus (goes to that card as GRAI+B)
37	WRIT-B	Write/read control	Activated by card that controls the bus. Low indicates that controlling card is writing to addressed card. High indicates that controlling card is reading from addressed card
38	ADRV-B	Address valid	Indicates ADnn-B address lines are stable; enables address decoder and related logic on addressed card

Table 3-2. Processor Bus Signals (Cont)

CARD PIN	MNEMONIC	SIGNAL NAME	FUNCTION WHEN ACTIVE
39	MEMA-B	Memory acknowledge	Indicates that addressed card has accepted data or has placed data on DAnn-B lines
40*	BYTE-B	Byte/word control	Allows high order byte to be carried on low order byte lines of data bus
41	REST-B	Reset	Resets all circuit card assemblies
42*	BTOM-M	Bus timeout	Indicates that requested data transfer was not completed within normal instruction interval
43*	SYST-B	System mode	Initiates SYSTEM mode
44*	LOCA-B	Local mode	Initiates LOCAL mode
45	TORN-O	Turn-on	Power-up initialize command; activates REST-B sequence
47*	DPRN-D	Display processor run	Lights lamp in SYS/RUN pushbutton
50*	50DB-F	50 kilobaud clock	50 kilobaud I/O clock pulsetrain

3.2.2 GRAPHIC BUS. The graphic bus comprises backplane wiring connections common to the graphic controller card and all circuit cards that interface with the graphic controller card to develop analog signal levels that control the image presented on the display indicator or hard copy unit. These graphic subsystem cards are located in card cage slots 1A1XA10 through 1A1XA17. All card cage slots in this subsystem are dedicated, facilitating the numerous discrete line interconnections between these cards, except that the output channel card can occupy either slot 1A1XA16 or, if the optional 2-D coordinate converter card is in slot 1A1XA16, slot 1A1XA17. Table 3-3 lists the standard graphic subsystem cards.

Functionally, the term "graphic bus" pertains to the graphic controller outputs to other graphic subsystem circuit cards. This bus includes a 12-bit DBnn-G data bus that carries coded data or setup-control codes to those cards, and a variety of timing signals that determine which cards/circuits receive the DBnn-G data. Except for the 12 DBnn-G lines (pins 1 through 12, respectively), these signals either do not connect to all cards on the bus or connect at different pins. Pin connections and identifications for the graphic bus signals are presented in Appendix A.

Table 3-3. Standard Graphic Subsystem Cards

CARD CAGE SLOT	CIRCUIT CARD ASSEMBLY	
1A1XA10	Graphic controller	
1A1XA11	Character generator	
1A1XA12	Extender card (optional)	
1A1XA13	Ramp generator (or optional ramp/conic generator)	
1A1XA14	(Y-axis) D/A converter	Identical cards
1A1XA15	(X-axis) D/A converter	
1A1XA16	Output channel (or optional 2-D coordinate converter)	
1A1XA17	Not used (or output channel, if 2-D coordinate converter is installed in slot 1A1XA16)	

3.2.3 POWER BUS. The power bus comprises backplane wiring connections that carry operating power to all card cage slots. Power is distributed through redundant pins to facilitate current flow to and from each card. Table 3-4 lists the common power bus connections.

Table 3-4. Power Bus (Common to All Cards)

CARD CAGE PINS	BUS MNEMONIC	SIGNAL/NAME/FUNCTION
1*, 2* 29, 30 53, 54	DRET-	Digital ground return (common circuit ground connections on all cards as return for circuits receiving P05V+ power.)
55, 56	P05V+	Positive 5 volts DC
77, 78 97, 98	ARET-	Analog ground return (common circuit ground for circuits receiving N15V- and/or P15V+ power.)
93, 94	N15V-	Negative 15 volts DC
95, 96	P15V+	Positive 15 volts DC

*These redundant DRET- connections apply only to slots 1A1XA1 through 1A1XA9 in the processor subsystem.

3.3 PROCESSOR BUS CONTROL AND TIMING

To perform a program operation, a circuit card seizes control of the processor bus either to obtain data from that bus or to pass data via that bus to some other circuit card. This process involves a handshaking sequence controlled by a grant-signal connection, running as a series string through all cards in the processor subsystem (slots 1A1XA1 through 1A1XA10). This connection configuration means that the GRAO+B (grant output) signal at pin 35 of any slot is connected as the GRAI+B (grant input) signal at pin 36 of the next-higher numbered slot. This connection configuration continues along the card cage from slot 1A1XA1 (highest priority) to slot 1A1XA10 (lowest priority).

A card obtains bus control only when its GRAI+B input is active (high logic level). This normal condition is established by a pullup resistor on the GRAI+B input line of each card, holding that input active unless it is forced low by a preceding higher-priority card that has requested bus control. A card requests bus control by deactivating its GRAO+B output, thereby disabling the GRAI+B input of the next card in sequence which, in turn, lowers the GRAO+B output from that card. The priority string thus begins with the first non-memory card installed in the card cage and continues through graphic controller card 1A1A10 (which has lowest priority).

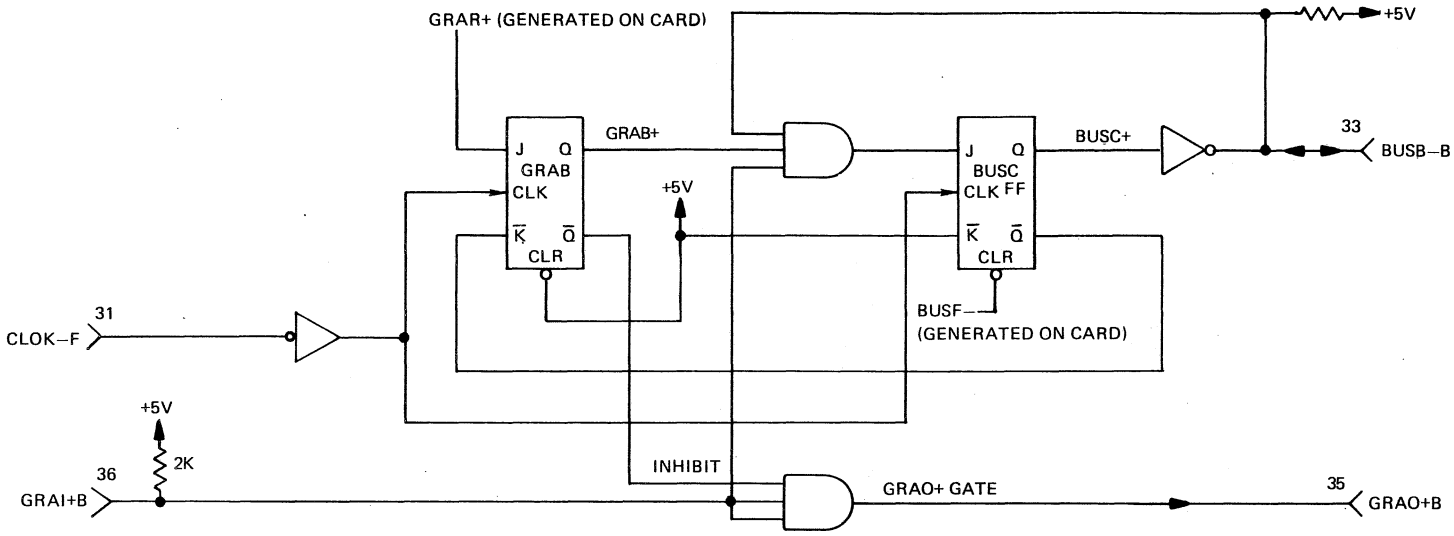
The priority-grant configuration permits user discretion in assigning priorities to the processor bus circuit cards, since the cards in slots 1A1XA1 through 1A1XA8 can be switched around at will. Read/write memory cards are not affected by the priority structure; their GRAI+B input is connected through to their GRAO+B output to maintain priority continuity.

The unused (spare) processor subsystem card slots allow the addition of optional bus-compatible circuit cards. If such cards are not used, the standard cards (excluding the read/write memory cards) must be moved up to maintain the priority string (i.e., no empty card slots between controlling cards).

If a particular configuration requires a vacant slot between cards that can gain control of the bus, then the GRAI+B and GRAO+B pins of the vacant slot must be jumpered at the back plane. See Section 4 for details.

3.3.1 BUS CONTROL LOGIC. Figure 3-1 is a simplified logic diagram of a typical bus-grant circuit which allows any processor bus circuit card to request and gain control of the bus unless inhibited by a higher-priority card. A bus-grant circuit similar to the one shown in figure 3-1 is contained on all processor subsystem cards except the read/write memory cards (which have through-line connections). The exact circuit configuration may differ slightly on individual cards, but the functions illustrated are valid in all cases.

When a function circuit on any card is set up to gain processor bus control, that circuit generates an internal GRAR+ (grant request) signal which is loaded into the GRAB buffer flip-flop by the next 10-MHz CLOK-F pulse. The resultant GRAB $\overline{Q}$ output inhibits the GRAO+ gate, deactivating the GRAO+B output, which serves as the GRAI+B input to the next card on the bus. That low GRAI+B input then inhibits the corresponding GRAO+ gate on that next card, deactivating its GRAO+B output to the next card in sequence, and so on.



NOTES: 1.

SIGNAL	FUNCTION (TRUE STATE)
GRAR+ (GRANT REQUEST);	INITIATES BUS REQUEST.
GRAB+ (GRANT REQUEST BUFFER)	SYNCHRONIZES BUS REQUEST.
BUSC+ (BUS CONTROL)	LATCHED GRAB+ ENABLED BY TRUE GRAI.
BUS–B (BUS BUSY)	DISABLES BUS CONTROL UNTIL USAGE IS COMPLETED (HERE OR EXTERNAL).
BUSF– (BUS FINISHED)	TERMINATES BUS CONTROL
GRAI+ (GRANT INPUT)	BUS CONTROL ENABLE FROM HIGHER PRIORITY MODULE.
GRAO+ (GRANT OUTPUT)	BUS CONTROL ENABLE TO LOWER PRIORITY MODULE

2. ALL SIGNALS INTERNAL EXCEPT GRAI+B, GRAO+B, BUSB–B, CLOK–F. BUSB–B IS BIDIRECTIONAL INTERNAL, SOMETIMES EXTERNAL; CLOK–F IS INTERNAL ON ROM AND STATUS CARD.

H-78-0095-135A

Figure 3-1. Bus Grant Circuit, Simplified Diagram

If the GRAI+B input to the card requesting bus control is high and the BUSB-B (bus busy) line currently is not active, GRAI+ gates the GRAB+ flag signal to the BUSC flip-flop, which loads that signal on the next CLOK-F pulse. The resulting BUSC+ output is inverted to activate the BUSB-B control line, informing all other cards that the processor bus is currently under control. At the same time, the BUSC Q output is applied as the $\overline{K}$ input of the GRAB flip-flop, resetting that flip-flop on the next CLOK-F pulse (third pulse after GRAB+ is generated). This event removes the inhibit from the GRAO+ output gate, reestablishing GRAO+B output as a high logic level. BUSB-B remains active, however, until the BUSC flip-flop is cleared by a low BUSF- (bus finished) signal. BUSF- is generated internally in the card's function circuit when bus control can be relinquished (i.e., after completion of a read or write cycle).

3.3.2 BUS CONTROL TIMING. Figure 3-2 shows the timing of a typical bus control sequence. In this diagram, signals generated by the display processor are suffixed D, while signals generated by the graphic controller are suffixed G.

In figure 3-2, the display processor and the graphic controller simultaneously attempt to gain bus control. Thus, GRAR+D and GRAR+G go high simultaneously, setting the GRAB flip-flops on the two cards. The cross-hatching of the two GRAR+ signals in figure 3-2 designates the periods in which they can be active with respect to the CLOK-F pulse train during the particular bus sequence.

Because of its higher priority location on the bus, the display processor gains bus control first. When the display processor's GRAB flip-flop is set, the resultant low GRAO+B output from that card applies a low GRAI+B to the graphic controller card, thereby inhibiting the conditioning gate for the BUSC flip-flop on that card and preventing that flip-flop from activating the BUSB-B output. The grant ripple timing shown in the GRAO+/GRAI+ signals represents an allowance for gate delays along the bus.

After the GRAB flip-flop on the display processor card is set, the BUSC flip-flop on that card is set by the next CLOK-F pulse, and the BUSB-B output goes low. Internally, the BUSC- signal gates the address of the processor subsystem card that is to be accessed onto the ADnn-B processor address bus.

The display processor then generates a low ADRV-B (address valid) output. The delay between activation of BUSB-B and activation of ADRV-B is approximately 100 nanoseconds (i.e., ADRV-B is produced by the same CLOK-F pulse that clears the GRAB flip-flop). ADRV-B initiates operation within the addressed device (read/write memory, ROM and status, interface, or the graphic controller).

The addressed device responds by generating a low MEMA-B* (memory acknowledge) signal. The period between activation of ADRV-B and activation of MEMA-B is a function of the addressed device card and can range from a few hundred nanoseconds to seven microseconds. In a READ operation, MEMA-B indicates that the addressed device has placed valid data on the DAnn-B processor data bus. In a WRITE operation, MEMA-B indicates that the addressed device has taken data from the DAnn-B bus. Activation of MEMA-B terminates ADRV-B, whose active period is a function of the addressed device circuit. Following activation of MEMA-B (and, in the case of a read operation, following acceptance of data from the bus), the display processor generates an internal BUSF- (bus finished) signal. This signal clears the BUSC flip-flop in the display processor, terminating BUSB-B and relinquishing bus control.

*MEMA-B (memory acknowledge) is a general response/acknowledge signal, generated by any addressable device/register on the bus. It is not limited to memory accesses.

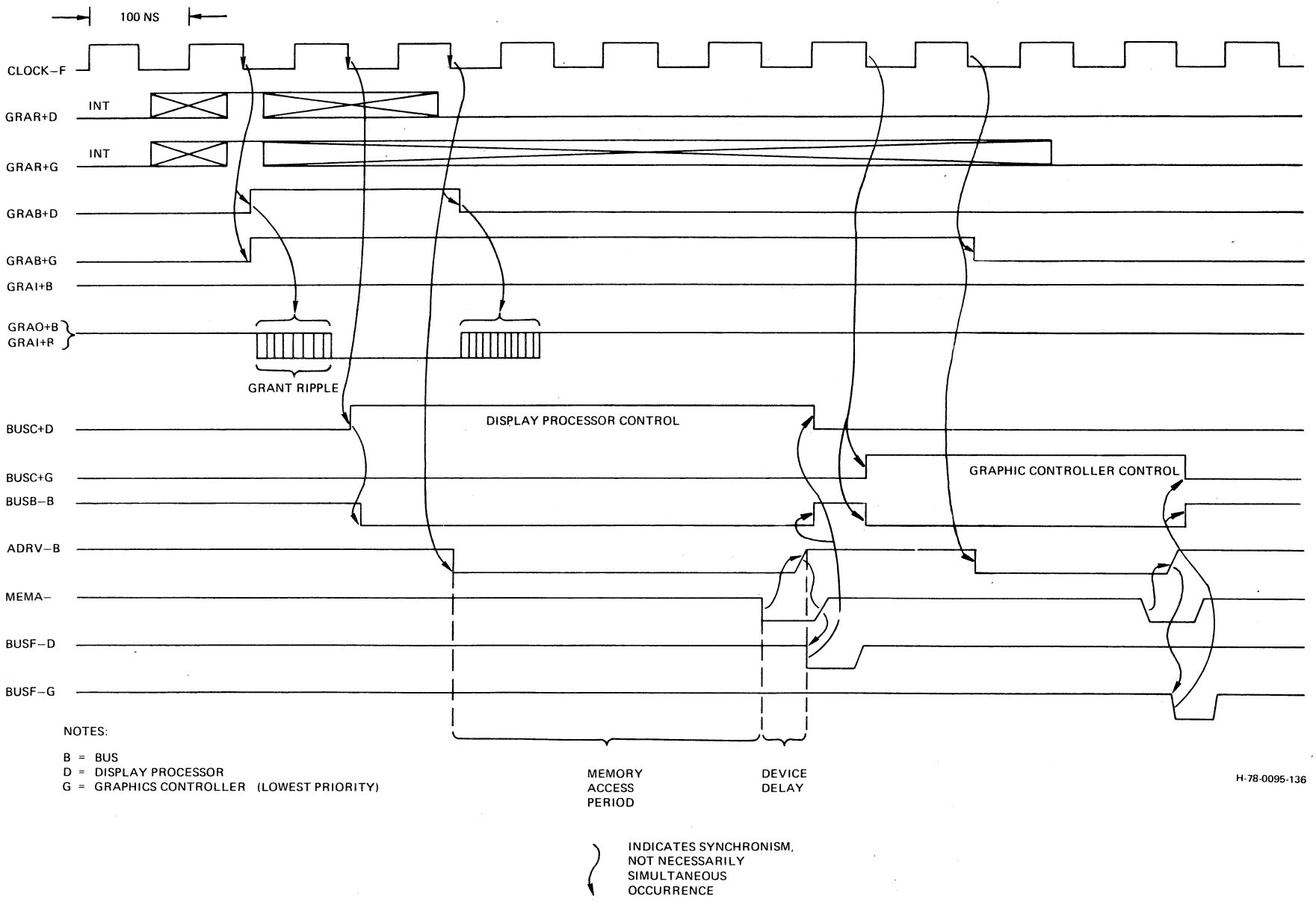


Figure 3-2. Processor Bus Timing

When the display processor's GRAB flip-flop clears, the GRAI+ input to the graphic controller goes high, but the active BUSB-B signal continues to inhibit the conditioning gate for the BUSC flip-flop in the graphic controller card (see figure 3-1). If the GRAR+G signal is still active (or has become active again), deactivation of the BUSB-B signal at the end of the display processor's control cycle permits the BUSC flip-flop to be set by the next CLOK-F pulse (see figure 3-2). This condition initiates a graphic controller sequence, letting the following CLOK-F pulse set the BUSC flip-flop in the graphic controller to reactivate the BUSB-B signal. These conditions remain in effect until the graphic controller completes its function and activates its BUSF-G signal to clear its BUSC flip-flop, releasing the BUSB-B processor control line once more.

3.3.3 INTERRUPT LOGIC. Figure 3-3 is a simplified diagram of the interrupt logic contained on all processor subsystem cards that can interrupt the program. The interrupt logic on different cards varies in detail, but the functions shown are common. The interrupt logic operates in conjunction with the bus grant circuit. The associated bus grant circuit is repeated in figure 3-3 to show its control of interrupts. A simplified timing diagram is also included to show approximate time relationships.

A card set up to interrupt the program first generates an initial, high-level interrupt request signal or flag. This flag is the conditioning input to the INTERRUPT flip-flop. Except for a sync-link condition, all interrupts are program-maskable, and the mask must be enabled before the interrupt flag can be generated.

At the end of every instruction cycle, the display processor activates the IREQ-D (interrupt request) control line to sample all interrupt logic circuits to determine their interrupt request status. On any card which has an active interrupt-request flag, IREQ-D both sets of the applicable INTERRUPT flip-flop and gates the resultant INLn-B (interrupt level) signal pulse from the card. In figure 3-3, the INTERRUPT flip-flop activates INL7-B, the highest of three jumper-selectable priority levels.

The display processor senses all INLn-B signals simultaneously. If the display processor's program status word (PSW) determines that the interrupt being requested is of a higher priority than the current program operation, the PSW enables an interrupt sequence by (a) forcing the highest activated priority INLn-B lines low (if more than one went active) and (b) activating the IENA-D (interrupt enable) control line to enable the GRAB flip-flop on the card. These conditions (INTERRUPT flip-flop set, INLn-B reactivated, and a low-going IENA-D signal) enable the INTERRUPT gate, activating the GRAR+ flag to the GRAB flip-flop. This flip-flop is set by the next CLOK-F pulse, and its GRAB $\overline{Q}$ output disables the GRAO+ gate to deactivate the GRAO+B output from that card, thus disabling all following lower-priority cards.

If the processor bus is not busy (BUSB-B is high), the conditioning gate is enabled for the BUSC flip-flop on that card, which is set by the next CLOK-F pulse. This, in turn, activates the BUSB-B control line to all other cards on the processor bus, while the low $\overline{Q}$ BUSC flip-flop output enables trap address drivers on the card. These drivers then place the applicable trap address (usually a ROM output accessed by the same signal conditions that caused the original interrupt-request flag) on the DAnn-B data bus for transfer to the display processor as a program branching command. Setting the BUSC flip-flop also clears the INTERRUPT flip-flop and initiates an interrupt complete condition within the interrupt request circuit, deactivating the interrupt-request flag. When the following CLOK-F pulse appears (approximately 100

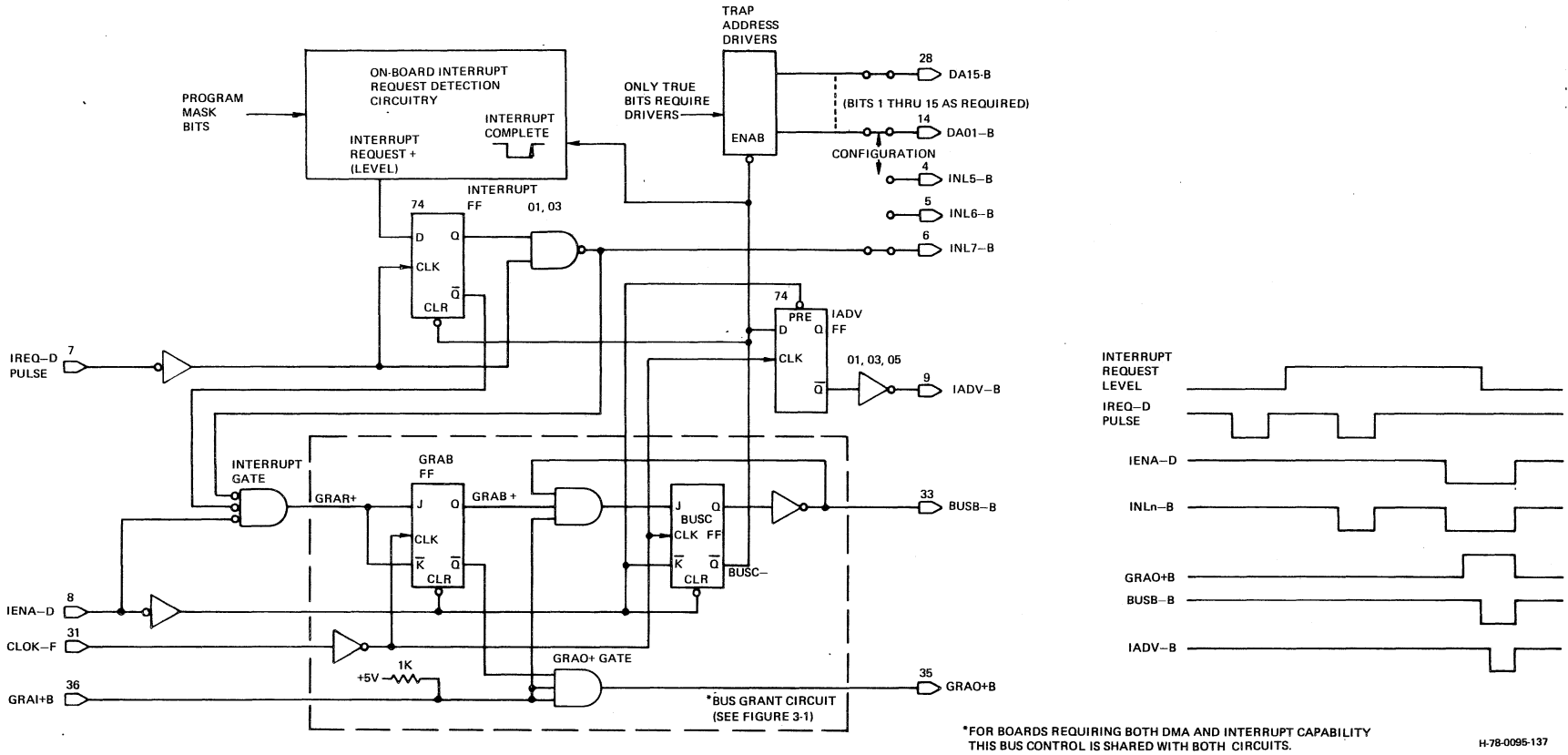


Figure 3-3. Interrupt Logic and Timing

nanoseconds after BUSB-B goes active), the low $\overline{Q}$ BUSC flip-flop output is loaded into the IADV flip-flop, sending a low IADV-B (interrupt address valid) signal to the display processor as a command to read the trap address. After accepting the trap address, the display processor deactivates IENA-D, clearing the GRAB and BUSC flip-flops to terminate the interrupt cycle on the applicable circuit card.

The display processor then handles the interrupt.

3.4 READ/WRITE MEMORY

NOTE

If your system contains large read/write memory cards, skip this paragraph and refer instead to Sanders' H-78-0408.

The terminal controller may contain up to three read/write memory cards, each capable of storing up to 8,192 separately addressable 16-bit words, or up to 16,384 separately addressable 8-bit bytes.

All read/write memory cards are identical and can operate in any card cage slot from XA1 through XA7. The preferred location is at the lower end of the card cage. Each card contains a manually set address selector switch that establishes the value of its address.

The read/write memory cards connect to the processor bus. They are controlled by signals from that bus, but they do not take control of the bus.

Any circuit card connected to the processor bus can write data into a specific memory location by:

1. Seizing control of the bus.

2. Placing the desired address on the ADnn-B lines and the desired data on the DAnn-B lines.

3. Grounding the WRIT-B (write command) and ADRV-B (address valid) control lines.

The same circuit cards can read out stored data onto the DAnn-B lines by the same procedure, except that WRIT-B remains high.

When the memory card is not responding to read or write instructions, it continuously refreshes itself.

3.4.1 MAJOR CIRCUITS. Figure 3-4 is simplified block diagram of the read/write memory card. The following paragraphs describe the functions of each major circuit.

Memory Card Address Select. This circuit compares the binary value of bits AD14-B through AD17-B with the settings of the manual switch to determine if the card is being addressed. The manual switch lets each read/write memory card be set for 40,000 octal byte locations, as shown in table 3-5.

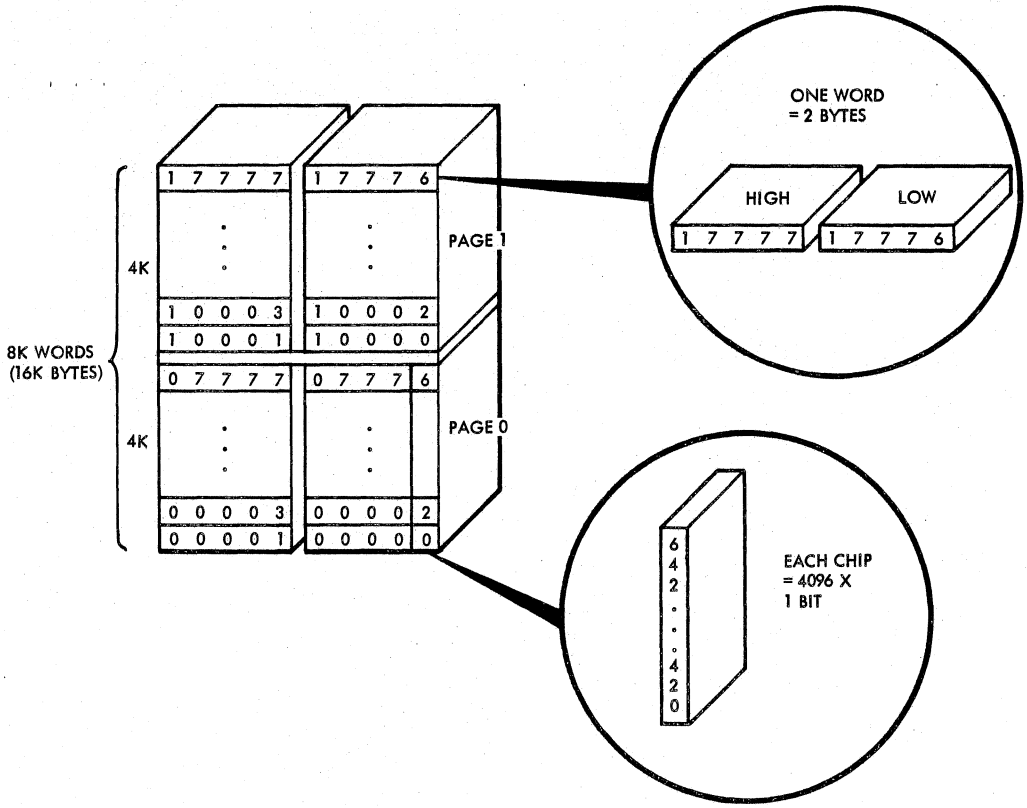


Figure 3-4. Memory Organization

Table 3-5. Read/Write Memory Card Addressing

AD17-B	AD16-B	AD15-B	AD14-B	ADDRESS SELECTION
High	High	High	High	First 40,000 locations (000000_8 thru 037777_8), identified as memory card no. 1
High	High	High	Low	Second 40,000 locations (040000_8 thru 077777_8), identified as memory card no. 2
High	High	Low	High	Third 40,000 locations (100000_8 thru 137777_8), identified as memory card no. 3

Memory Cycle Control and Bus Time-Out Logic. This circuit responds to processor bus control signals or to the refresh oscillator clock train. It performs the following functions:

1. It directs the address multiplexer to select the proper address (address bus bits or the output of the refresh counter).

2. It directs the data bus transceiver to accept memory write data from the data bus lines, or to place memory read data on the data bus lines.

3. It generates the memory page select and strobe signals.

4. It generates the MEMA-B (memory acknowledge) to indicate the completion of a memory read or write cycle.

5. It generates the BTOM-M (bus timeout) signal if the read or write cycle could not be completed.

Refresh Oscillator. This circuit generates a 123.33 kHz OSC+ clock train.

Refresh Counter. This circuit produces a constantly stepping 6-bit refresh address word that goes to the address multiplexer, and a 66.667 kHz timing signal that goes to the memory cycle control and bus time-out logic.

Address Multiplexer. This circuit determines which 6-bit address is applied to each storage cell in both read/write memory pages. This circuit selects either an address from the AD01-B through AD12-B lines, or the output of the refresh counter.

Random Access Memory. This circuit accepts and stores data bits from the processor bus data lines during a write operation, or reads the stored data out onto the data lines during a read operation. When not engaged in reading or writing, the memory is continuously refreshed by the stepping address from the refresh counter and strobes from the memory cycle control and bus timeout logic.

The memory consists of two pages. Each page contains 16 storage devices (chips). Each chip is a 4096 x 1-bit device; thus each page can store 4096 16-bit words, and the entire memory card stores 8192 16-bit words. See figure 3-4.

Bit AD13-B is the page select bit. A high bit AD13-B selects page 0, a low bit AD13-B selects page 1.

When BYTE-B is low, the memory is in byte mode. Bit AD00-B is the byte select bit. A low bit AD00-B selects the low order byte, a high bit AD00-B selects the high order byte. When BYTE-B is high, the memory is in word mode.

Byte Swap Logic. This circuit comprises two circuits: input byte swap and output byte swap.

When the memory is in byte mode, these circuits make possible the following alternatives:

1. Write a high order data byte into a high order memory location.

2. Write a low order data byte into a high order memory location.

3. Read a low order byte from memory onto the low order data bus lines.

4. Read a high order byte from memory onto the low order data bus lines.

When the memory is in word mode, high order data bytes are always written into or read from high order memory locations, and low order data bytes are always written into or read from low order memory locations.

Data Bus Transceiver. This circuit provides 3-state connections between the processor bus data lines and the read/write memory card circuits. The three states are high, low, and high impedance (essentially open).

The transceiver passes data bits DAnn-B to the memory as Dnn at all times. When so directed by the OUTL- and OUTH- signals from the memory cycle control logic, the transceiver passes the Onn memory output data to the processor data bus lines. When the OUTL- and OUTH- signals are high, the connections from Onn to the DAnn-B lines are a high impedance load.

Voltage Regulation Circuits. These circuits process the standard +5V and ±15V input to produce regulated +5V, +12V, and -5V (the latter two voltages required by the MOS memory devices).

3.4.2 OPERATION. The read/write memory performs three operations:

1. A write cycle to store data in memory.

2. A read cycle to fetch data from memory.

3. A refresh cycle to preserve the stored data.

The memory cycle control circuit responds to the ADRV-B signal (following completion of any refresh cycle already in process, by:

1. Inhibiting the refresh timing logic.

2. Enabling the bus time-out logic.

3. Activating one or both of two write commands to the memory devices. If BYTE-B is high (word mode), the circuit activates both WRIL- (which connects to the memory devices that receive data inputs D00 through D07) and

WRIH- (which goes to memory devices receiving data inputs D08 through D15). If BYTE-B is low (byte mode), the circuit activates only one of these, as determined by the state of AD00-B.

The memory cycle control circuit places a ground on one of two RASn+ (row address select) outputs to the memory devices. If page select bit AD13-B is high, RAS0+ goes low, enabling the first 4K x 16-bit memory page. If AD13-B is low, RAS1+ goes low, enabling the second 4K x 16-bit memory page. In either case, the setup logic inside the selected memory devices automatically refreshes the addressed row of 64 storage cells.

After a brief delay to allow completion of the setup/refresh operation, the memory cycle control logic grounds the ROWT+ output to the address multiplexer. The address multiplexer then passes bits AD01-B through AD06-B to the memory devices. After another short delay to let the new address bits settle, the memory cycle control logic produces low CAS0- and CAS1- (column address select) outputs. The memory devices accept the new 6-bit An word as the column address of a specific storage cell in the previously addressed row. This means that the applicable cell in whichever page received the low RASn+ signal stores the current value of the Dnn bit, passed to it by the data bus transceiver and the input byte swap circuit.

The memory cycle control logic then terminates the column and row address commands, leaving the stored value in place. At the same time it places a ground on the MEMA-B (memory acknowledge) line. This informs the device that has control of the bus that the read/write memory has stored the given data, and the bus can now be released. The controlling device terminates the ADRV-B signal. The trailing edge of ADRV-B terminates MEMA-B, clears the bus time-out logic, and releases the memory cycle control circuit for another operation (read, write, or refresh).

Read Cycle Operation. The read cycle operates with the same handshaking logic and timing as the write cycle, except that the WRIT-B line remains high. As a result, both WRIL- and WRIH- write commands from the memory cycle control logic are inhibited.

The bus controller first places the address on the ADnn-B lines, then grounds ADRV-B to confirm that the address is valid. The memory cycle control logic grounds the applicable RASn+ row select command with ROWT+ high. This action selects:

1. Bits AD07-B through AD12-B as the An address.

2. One of 64 rows of memory cells in each device. This selection refreshes the stored value in each cell in that row.

ROWT+ is then grounded, switching the address multiplexer to pass bits AD01-B through AD06-B, and the CASn- column select lines are grounded to select the one cell common for both selections for readout.

If BYTE-B is high (word mode), the memory cycle control logic produces low OUTL- and OUTH- signals. The eight high order bits pass from the memory devices through the data transceivers to the high order data lines. The eight low order bits pass from the memory device through the output byte swap circuit and the data transceiver to the low order data lines.

If BYTE-B is low (byte mode), the memory cycle control logic produces only the low OUTL- signal, enabling the low order half of the data transceiver. The state of AD00-B determines which memory byte passes through the output byte swap circuit to the data transceiver: a high AD00-B selects the low order byte, a low AD00-B selects the high order byte.

The memory cycle control logic gives these signals time to stabilize on the processor bus, then grounds the MEMA-B line. The card in control of the bus responds by loading the DAnn-B word into its own data register, then terminates the ADRV-B signal, clears the MEMA-B and OUTL-/OUTH- signals, and released the memory cycle control logic for its next operation (read, write, or refresh).

Initialization. Each read/write memory card is initialized when the output channel card produces a low-going TORN-0 pulse at power-on. This input clears the basic timing logic in the memory cycle control circuit, establishing a starting setup for the memory refresh function. Nothing exists in memory to be refreshed until the information is written in.

Write Cycle Operation. When a circuit card seizes control of the processor bus to write data into the read/write memory, the seizure follows a specific sequence: the 18-bit memory address is placed on the ADnn-B lines; the 16-bit data word is placed on the DAnn-B lines (or an 8-bit byte is placed on the eight least-significant DAnn-B lines and the BYTE-B line is grounded), the WRIT-B (write command) lines is grounded, and then the ADRV-B (address valid) line is grounded.

The DAnn-B data bits pass through the data bus transceivers on all read/write memory cards as the Dnn bits, applied to both memory pages on each card. If the BYTE-B signal is high, the full 16-bit Dnn word connects to the memory devices. If BYTE-B is low, the AD00-B signal controls the input byte swap circuit. If AD00-B is low, only the low order byte is taken, and it goes to the high order memory location. If AD00-B is high, the high order byte is taken, and it goes to the high order memory location.

At the same time, the four most-significant address lines are decoded by the memory card address select circuit. Only one memory card discovers a match between the address code and its own switch settings. That card's address select circuit enables its memory cycle control circuit. The corresponding circuits on other read/write memory cards are inhibited.

When the memory cycle control circuit is enabled, its initially high REFB- (refresh B) and ROWT+ (row time) signals cause the address multiplexer to select address lines AD07-B through AD12-B as the 6-bit address applied to all memory devices. This address selects one of 64 rows of storage cells in each memory chip.

Finally the arrival of the low ADRV-B signal triggers the memory cycle control and bus time-out logic on the addressed card, initiating a single memory cycle sequence. The other memory cards remain inhibited.

Refresh Cycle Operation. The refresh cycle is an independent timing function on each read/write memory card, operating continuously without external control. While any read/write memory card is undergoing either a write or read operation, the refresh logic is inhibited until the operation is complete. The refresh operation is timed by the free-running refresh oscillator. The OSC+ clock produces a 7-bit binary address from the refresh counter circuit, with LSB signal REFC+ applied to the memory cycle control logic and the other six bits applied to the address multiplexer.

Each time REFC+ goes high (i.e., every other OSC+ clock pulse), its high-going edge interrogates the current status of the memory cycle control logic. If no read or write cycle is in process, the memory cycle control logic goes into a refresh cycle. If a read or write cycle is in process, the refresh cycle is delayed until that output/input cycle is done. The memory cycle control logic then (a) grounds the REFB- signal, which internally triggers the timing sequence and prevents that logic from responding to any ADRV-B signal until the refresh cycle is done, and (b) sets the address multiplexer for refresh address selections.

The address multiplexer then selects the other six bits of the refresh counter output as the An address to the memory storage devices. This address remains in effect while the memory cycle control circuit grounds both RAS0+ and RAS1+ row-select commands and both CAS0- and CAS1 column-select commands. This arrangement means that all storage cells in the An-designated row are refreshed. Since no memory write or output enable command gets activated, no Dnn values are stored and no Onn values are produced.

The refresh cycle ends by clearing the RASn+, CASn-, and REFB- signals, thus releasing the memory cycle control logic for regular read/write operation. If no such cycle is requested by the processor bus at that time, conditions remain static while the refresh oscillator increments the refresh counter again. When REFC+ again goes high, the memory cycle control circuit repeats this same timing sequence, this time refreshing the rows of storage cells addressed by the next higher An value. This cycle operation repeats through all 64 steps of the refresh counter, refreshing all storage cells in each memory device within a total period of less than two milliseconds. The refresh counter then returns to zero value and starts through the same 64-step incrementation sequence again, repeating the same sequence indefinitely as long as the system remains powered.

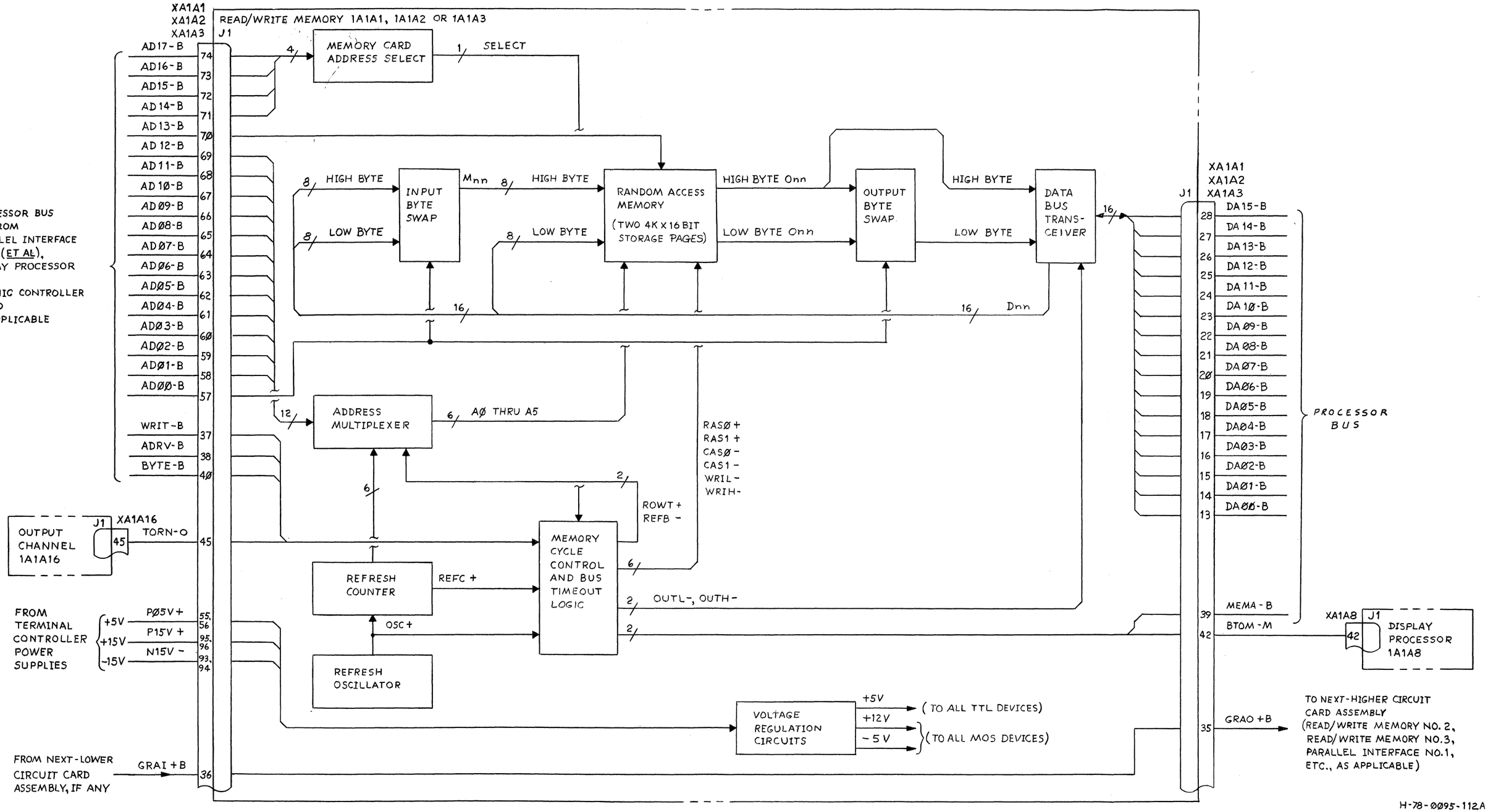


Figure 3-5. Read/Write Memory Card, Block Diagram

3.5 PARALLEL INTERFACE

NOTE

If your GRAPHIC 7 system contains a parallel interface that has its own technical manual, skip this paragraph and refer to that manual instead.

The parallel interface allows input/output communications betweeen the GRAPHIC 7 system and the host computer. The interface card is designed for easy modification during assembly to accommodate different host computers and applications. For example, host/interface communications pass through buffer gates that can be jumpered to produce the positive logic (active high) conditions used on the parallel interface card. If the host computer uses negative logic (active low) signals, the buffer gates are inverters. If the host computer uses positive logic (active high) signals, the buffer gates do not invert.

Other special requirements are acccommodated by convenient jumper selections between lug terminals on the parallel interface card. These jumper selections include: subordinate addressing, word/byte mode selection, interrupt priority, or other special conditions as required. Refer to Section 4 for instructions.

The basic functions of the parallel interface card are:

1. To pass a system initialization command from the host computer to the GRAPHIC 7 system.

2. To generate a GCP+ interrupt when the host computer announces that it has output data for the GRAPHIC 7 system.

3. To accept output data from the host and pass it to the appropriate destination in the GRAPHIC 7 system: the display processor for single-word transfers, the read/write memory for multiword transfers.

4. To accept data from the display processor or read/write memory and pass it to the host computer.

5. To generate a GCP+ interrupt after the host computer accepts a GRAPHIC 7 input (either single word or multiword).

6. To perform internal housekeeping activities, and monitor and report status.

3.5.1 SIGNAL CONNECTIONS. The parallel interface card connects through J1 to all the display processor buses, including the 16-bit DAnn-B data bus, the 18-bit ADnn-B address bus, and all bus control and interrupt lines (see paragraph 3.2.1).

The parallel interface connects to the host computer through a 2-way cable attached to edge-mounted connectors J2 and J3.

Connector J2 receives a 16-bit parallel output data word, OD00±* through OD15±, plus a variety of handshaking signals concerned with host computer output data transfers.** This connector also receives an INIT± host computer output, representing a system reset command. Tables B-1 and B-2 (Appendix B) list the J2 input and output signals and define their functions.

Connector J3 passes a 16-bit parallel input data word, ID00± through ID15±, plus a variety of handshaking signals concerned with host computer input data transfers. Tables B-3 and B-4 in Appendix B identify the J3 input and output signals and define their functions.

3.5.2 PARALLEL INTERFACE INTERNAL BUSES. The parallel interface contains two internal buses: the 16-bit IOnn+ input/output data bus, and the 16-bit STnn+ status bus.

The IOnn+ bus carries the following signals:

1. ODnn± data words from the host computer. These signals go either to the DAnn-B processor data bus or to storage registers on the parallel interface card.

2. DAnn-B data words from the processor bus. These signals go to storage registers on the parallel interface card, including the host input data register which, in turn, places the data on the IDnn± bus for transmission to the host computer.

3. Data stored in various registers on the parallel interface card. These signals go either to the DAnn-B processor bus for distribution to other GRAPHIC 7 circuits, or to the host input register on the parallel interface card for transmission to the host computer on the IDnn± bus.

The 16-bit STnn+ status bus carries various control and monitoring signals. Certain STnn+ bus bits represent GCP+ commands that establish the correct logic setup for specific operations. Other bits represent monitoring signals that direct the GCP+ to sequence from one program function to another.

3.5.3 MAJOR CIRCUITS (See figure 3-7)

Reset and Timing. An active REST-B input from the display processor is converted to REST+ and REST- signals to establish initial conditions throughout the parallel interface card. Similarly, the CLOK-F clock train from the ROM and status logic card is converted to a CLOK+ pulse train for use within the parallel interface.

*Those input/output signals ending with ± can be true in either state, depending on the type of computer used. The parallel interface card gets wired so that all logic true outputs from the host computer are received as high logic levels, and all logic true inputs to the host computer are logic highs up to the point where they enter the input buffer gates.

**Unless otherwise specified, the terms input and output are referenced to the host computer.

Data Multiplexer/Storage. This circuit selects the source for the data on the 16-bit IOnn+ bus. It enables the proper register to store the resultant data; it also causes the associated buffer gates to pass that data when appropriate. The data multiplexer controls operation of the buffer gates, passing ODnn± output data from the host computer to the IOnn+ bus. The data multiplexer also controls the gating circuits to and from the DAnn-B processor data bus.

The storage registers include:

1. Host input data register. This register receives inputs from the IOnn+ bus; its output goes to the IDnn± bus as an input to the host computer.

2. Memory address register. This register receives inputs from the IOnn+ bus; its output goes to the ADnn-B processor address bus and represents a specific memory address for a read or write operation.

3. Word count register. This register receives inputs from the IOnn+ bus; its output is a WC≠0 signal that stays active as long as there remains data to be transferred during a DMA (direct memory access) sequence. An LED on the card lights when this register is empty (WC+0) and goes out when this register contains any word count value (WC≠0).

4. Status register. This register receives inputs from the IOnn+ bus and from other circuits. The hardware that makes up this register consists of elements that are actually contained in other circuits. The status register outputs can be read on the IOnn+ bus.

Instruction Decoder. This circuit receives as inputs the AD01-B and AD02-B signals from the processor address bus, and the WRIT+ and ADRV+ signals from the processor control bus. Its outputs are read and write commands that go to different registers in the data multiplexer/storage circuit. A write command tells the addressed register to accept data from the IOnn+ bus. A read command tells the addressed register to place its contents on the IOnn+ bus.

Sequence Decoder. This circuit controls the sequence of input/output transfers between the parallel interface and the host computer.

The sequence decoder is a state counter. It increments from one count to another when it detects different control signals. Each count represents a specific state in the input/output transfer sequence, and is accompanied either by command signals that operate on another circuit, or inhibit signals that prevent further actions until the action in process is completed.

The counting sequence varies, depending on whether the specified operation is an input transfer or an output transfer, and whether the operation is a single-word transfer or part of a DMA sequence. LED indicators DS1 through DS4, mounted on the parallel interface card, give a continuous readout of the count. Figure 3-6 shows the indicator convention.

Figure 3-8 shows different counter sequences for each type of input/output transfer, including single word transfers and DMA transfers. Each state of the sequence decoder is represented by a large circle. The small circles give the count value.

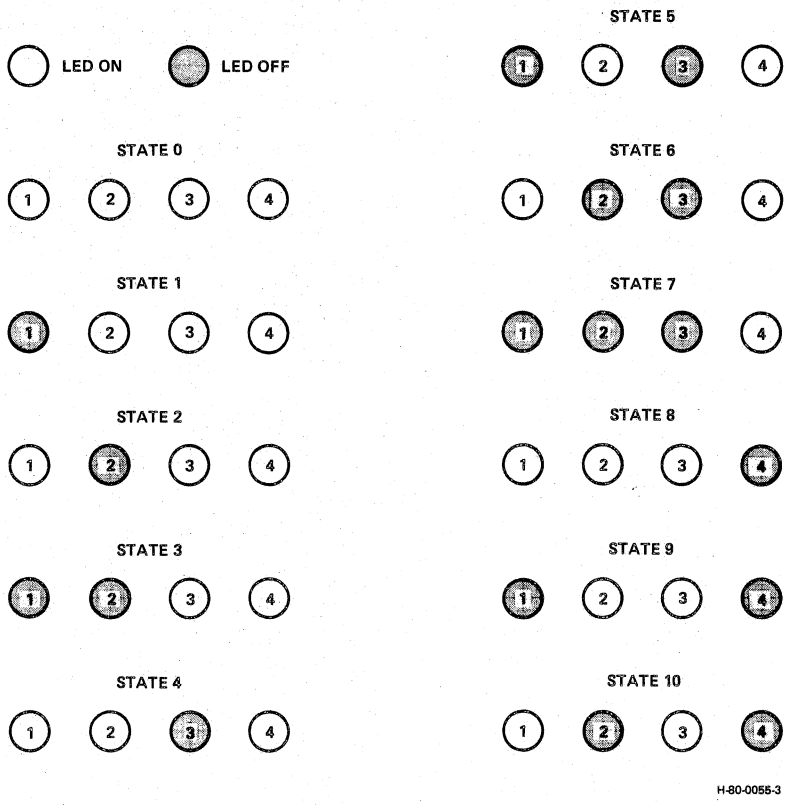


Figure 3-6. Parallel Interface LED Indications

Interrupt and Processor Bus Control. This circuit controls the transfer of data between the parallel interface card and the GRAPHIC 7 processor bus. To perform this function, the circuit monitors the STnn+ status bits and the control lines of the processor bus. Its outputs are timing and enabling signals that:

1. Transfer data to another GRAPHIC 7 card by seizing control of the bus, place the device address and the data on the bus, activate ADRV-B, and wait for the MEMA-B response from the receiving device.

2. Receive data from another GRAPHIC 7 card, steer the data to the appropriate storage register, and generate the MEMA-B response.

The interrupt circuit is triggered by signals from the sequence decoder when single-word input or output transfers are processed, or at the end of a DMA transfer. This circuit interrupts the GCP+ and sends a trap address to the display processor. The trap address indicates the type of interrupt condition detected by the sequence decoder, and branches the GCP+ to the applicable firmware subroutine. Table 3-6 lists the parallel interface interrupt trap addresses.

Table 3-6. Parallel Interface Interrupt Trap Addresses

	TRAP ADDRESS			
INTERRUPT	1ST CARD	2ND CARD	3RD CARD	4TH CARD
Input	120	400	420	440
Output	124	404	424	444
Attention	130	410	430	450

Handshaking Logic. This circuit sends discrete signals to the host computer for handshaking control of all I/O transfers between the parallel interface and the host computer. The circuit consists of an input section and an output section.

1. The output section responds to an active OCTL± signal from the host computer. After the parallel interface has stored the data from the computer, the handshaking logic sends both an OWR± signal and an ODR± signal. The OWR± signal remains active until the host computer terminates its OCTL± output. The output handshaking logic also includes an OMR± signal (a replica of status bit ST00) that can be programmed for unique applications.

2. The input section sends an IWR± signal to the host computer after valid input data have been placed on the IDnn± interface bus. When the host computer responds by sending its ICTL± signal, the input section terminates IWR± and sends an NDRY± pulse. The input handshaking logic also includes an IMR± signal (a replica of status bit ST12) that can be programmed for unique applications.

Initialize Buffer Gates. These circuits convert INIT± signals from the host computer into low SYST-B signals that go to the display processor to initiate a terminal controller system reset sequence.

3.5.4 OPERATION. The parallel interface performs the following types of operation:

1. Receive single-word output from host computer.

2. Receive DMA transfer from host computer.

3. Send single-word input to host computer.

4. Send DMA transfer to host computer.

In performing these operations, the parallel interface also communications with the display processor and the read/write memory; it generates GCP+ interrupts and status signals.

The following paragraphs describe initialization and operation in each of the various modes.

3.5.4.1 Initialization. There are two initialization signals: INIT± from the host computer and REST-B from the display processor.

An active INIT± signal from the host computer enters the parallel interface at J2-47, passes through two or three inverters (depending on the jumper connection at E94) and leaves the parallel interface at J1-43 as a low STST-B that goes to the display processor. The display processor responds by making REST-B low.

A low REST-B signal from the display processor enters the parallel interface at J1-41 and performs the following actions:

1. Clears the interrupt and bus control circuits.

2. Clears the data multiplexer storage registers; memory address and word count go to zero.

3. Clears the sequence decoder; the parallel interface card goes to State 0.

4. Clears the handshaking logic.

In this condition the parallel interface is ready to receive commands and data from either the GCP+ (over the processor bus) or the host computer (over the interface bus).

3.5.4.2 Status Setup. In its cleared state, the parallel interface is unable to report anything to the GCP+. Early in the GCP+ setup sequence for I/O processing, therefore, the GCP+ writes a new status word. This word establishes interrupt enable conditions and any other desired applications (e.g., extended memory address, programmed handshaking requests, etc.). Table 3-8 lists each status bit and its function.

To load the status word into the parallel interface, the GCP+ places that word on the data bus (DA00-B through DA15-B)*, then places the address for the parallel interface status register on the address bus (AD00-B through AD17-B). See table 3-7.

*Status bits 04, 07, 08, 09, 10 and 15 are read-only bits, not loaded by GCP+. They get generated by the parallel interface.

Table 3-7. Parallel Interface Register Addresses

REGISTER	ADDRESS			
	1ST CARD	2ND CARD	3RD CARD	4TH CARD
Word count	172410	172430	172450	172470
Memory address	172412	172432	172452	172472
Status	172414	172434	172454	172474
Data	172416	172436	172456	172476

The display processor then generates the low BUSB-B, WRIT-B, and ADRV-B signals. These conditions make the instruction decoder in the parallel interface send a WSTA- (write status) command to the data multiplexer/storage logic. The status registers accept and store the bits of the DAnn-B data word, placing them on the status bus to other parallel interface circuits. These status bits remain in effect until the next status update instruction arrives. The parallel interface generates a low MEMA-B to indicate it has recognized its card address.

Table 3-8. Parallel Interface Status Register Bit Description

BIT	IDENTIFICATION	DESCRIPTION
00	OMR+ (output message request) (spare bit #1) (TEST1-OUT)	Program read/write, cleared by processor bus reset. This bit can be programmed as required and presents an OMR± signal to the host computer. When J2/J3 test strap is connected, this signal triggers the NDRY single-shot.
01	MAR16 (memory address register bit 16)	Program read/write, cleared by processor bus reset. This bit is used in conjunction with standard memory address register outputs (MARnn) to expand DMA addressing capability to 64K words (128K bytes).
02	MAR17 (memory address register bit 17)	Program read/write, cleared by processor bus reset. This bit is used in conjunction with standard memory address register outputs (MARnn) to expand DMA addressing capability to 128K words (256K bytes).
03	MODE+ (DMA I/O mode)	Program read/write, cleared by processor bus reset. When set (bit = 1), indicates input operation (word transfers from GRAPHIC 7 to the host computer). When cleared (bit = 0), indicates output operation (word transfers from host computer to GRAPHIC 7). The GCP+ writes this bit before a DMA sequence after decoding message header instructions, and leaves it unchanged until the DMA sequence is completed.

Table 3-8. Parallel Interface Status Register Bit Description (Cont)

BIT	IDENTIFICATION	DESCRIPTION
04	DMAC+ (DMA complete)	Program read-only, cleared by processor bus reset or by start of DMA sequence. Normally set condition (bit = 1) is cleared when sequence decoder activates status bit 08 (word count ≠ 0) and remains cleared until the write-status clock signal triggered by end of DMA sequence finds status bit 08 returned to normal inactive state (word count = 0). Also receives set command with activation of input interrupt request (IINT-) from sequence decoder (effective only if status bit 08 is low and sequence decoder is not at State 0).
05	OWR+ (output word received)	Program read/write (set only), cleared by processor reset. The sequence decoder sets this bit to acknowledge receipt of host-output data announced by an active OCTL± (output control) handshaking signal from host computer before each output-word transfer. When set, the OWR+ bit sets up the I/O transfer timing logic for output-transfer operation and triggers a 150-nanosecond ODR± (output data received) pulse to the host computer. This bit is cleared when status register bit 07 is deactivated by termination of OCTL± in response to either OWR± signal or associated ODR± pulse.
06	EOUT+ (enable output interrupt)	Program read/write, cleared by processor bus reset. This bit can be programmed as required to enable (set) or mask (reset) output interrupts initiated by host computer announcement of output data. When set (bit = 1), this bit enables generation of GCP+ output interrupt when the sequence decoder is stepped to State 9 by an initial OCTL± handshaking signal from the host computer or following completion of a DMA output-transfer sequence.
07	SYOC+ (synchronized output control)	Program read-only, cleared by processor bus reset. This bit is set following detection of an active OCTL± (output control) output from the host computer, and remains set until that OCTL± signal is deactivated. While set (bit = 1), SYOC+ establishes output-transfer setup conditions and releases OWR-generation and certain interrupt

Table 3-8. Parallel Interface Status Register Bit Description (Cont)

BIT	IDENTIFICATION	DESCRIPTION
07 (Cont)		generation functions; when reset (bit = 0), SYOC+ clears OWR+ signal (bit 05) and same interrupt functions.
08	WC≠0 (word count ≠ zero)	Program read-only, cleared by processor bus reset. This bit reflects the sign bit of the word count register and is set whenever that register is loaded with any two's complement value designating an absolute number of DMA-block words remaining to be transferred. It is cleared when the word count register is incremented to zero value, indicating that all DMA block words have been transferred.
09	ATN1+ (attention #1)	Program read-only. ATN1+ reflects the state of a host computer signal called ATN1±, and allows the host computer to provide any applicable handshaking condition or timing signal. For some host computers, ATN1+ is associated with a host-initiated interrupt triggered on circuits added to the standard parallel interface.
10	ATN2+ (attention #2)	Program read-only. ATN2+ reflects the state of a host computer signal called ATN2±, and allows the host computer to provide any applicable handshaking condition or timing signal. For some host computers, ATN2+ is associated with a host-initiated interrupt triggered on circuits added to the standard parallel interface.
11	Spare attention interrupt enable	Program read/write, cleared by processor bus reset. Spare can be programmed as required. Not used for the standard interface card, this bit is normally reserved as an enabling bit for any attention-interrupt circuit that might be added as a circuit modification for a specific host computer.
12	IMR+ (input message request) (spare bit #2) (TEST2-OUT)	Program read/write, cleared by processor bus reset. This bit can be programmed as required and presents an IMR± signal to the host computer. When J2/J3 test strap is connected, this signal enables/inhibits reset of OWR flip-flop.

Table 3-8. Parallel Interface Status Register Bit Description (Cont)

BIT	IDENTIFICATION	DESCRIPTION
13	IWR+ (input word request)	Program read/write, cleared by processor bus reset. For single-word input transfers, the GCP+ loads the input data word into the host input data register, then sets this IWR+ bit to announce data availability. For DMA input transfers, the parallel interface bus control logic initiates a memory transfer of DAnn-B data to the IDnn± interface bus, then sets this IWR+ bit. In either case, the sequence decoder clears this IWR bit when the host computer activates its ICTL± handshaking signal to confirm data receipt.
14	EINP+ (enable input interrupt)	Program read/write, cleared by processor bus reset. EINP+ can be programmed to enable (set) or mask (reset) GCP+ input interrupts initiated by host computer command for input data. When set (bit = 1), EINP+ enables generation of a GCP+ input interrupt when the sequence decoder is stepped to State 7 by activating the ICTL± handshaking signal from the host computer for each single-word input transfer, or following the final input transfer of a DMA input-transfer sequence.
15	INR+ (input busy)	Program read-only, cleared by processor bus reset. When high, INR+ indicates a transfer of GRAPHIC 7 data to the host computer is in process. The bit goes active when status bit 13 (IWR+) is set, indicating that DAnn-B data have been loaded into the host input data register and are available on the IDnn± interface bus. The INR+ stays active until the host computer terminates the ICTL± handshaking signal to announce receipt of the data word.

3.5.4.3 Single Word Output Transfers. Output transfers are either single word transfers (comprising commands to the GCP+) or multi-word transfers (comprising complex instructions or data).

Table 3-9 shows the sequence of events for single-word output transfers; refer also to figures 3-8 and 3-9.

Table 3-9. Single-Word Output Transfer Sequence

HOST COMPUTER	PARALLEL INTERFACE	DISPLAY PROCESSOR
Places 16 bits of data on ODnn± interface data bus, activates OCTL± line.	Change from State 0 to State 9, primes interrupt circuit.	Sends regular IREQ-D pulse.
	On receipt of IREQ-D, sends INLx-B to display processor (if status bit ST06 was previously set). Changes from State 9 to State 10.	Receives INLx-B, generates IENA-D.
	Seizes processor bus, sends INLx-B, sends trap address 000124_8, sends IADV-B.	Reads trap address, terminates IENA-D
	Releases bus.	Stores the address of the next instruction it was going to execute. Branches to output interrupt handling subroutine. Sends data read instruction to parallel interface.
	Passes ODnn± data to DAnn-B processor bus.	Reads data. Sends new status word to parallel interface with bit ST05 set.
	Sends OWR± and ODR± to host computer.	
Terminates ODnn± and OCTL±.	Terminates OWR±, changes from State 10 to State 0.	

At this point the host computer could initiate another output transfer, using the same procedure.

NOTE

If the GCP+ leaves parallel interface status bit ST06 high, each new word initiates a new GCP+ interrupt sequence, as described in table 3-9. For some applications, however, GCP+ deactivates status bit ST06 and simply monitors the state of status bit ST07 to determine when the next OCTL± condition occurs. The GCP+ then performs the same sequence.

3.5.4.4 DMA Output Transfers. In the case of a multi-word transfer, the first word is a message header, describing the function of the message. The second word normally contains the GCP+ memory address argument for the message string. The third word is the word count, specifying the number of words in the remainder of the output message.

Table 3-10 shows the sequence of events; refer also to figure 3-8.

Table 3-10. DMA Output Transfer Sequence

HOST COMPUTER	PARALLEL INTERFACE	DISPLAY PROCESSOR
Sends OCTL± and first word as in table 3-9.	Passes first word to display processor as in table 3-9.	Reads header of output message, makes DMA decision. Responds as in table 3-9.
Sends OCTL± and second word as in table 3-9.	Passes second word to display processor as in table 3-9.	Tells parallel interface to store the data in its memory address register.
	Stores address in its memory address register.	Responds to host computer as in table 3-9.
Sends OCTL± and third word as in table 3-9.	Passes third word to display processor as in table 3-9.	Tells parallel interface to store the data in its word count register.
	Stores two's complement value of word count in its word count register. WC≠0 goes high, status bit ST08 goes high.	
	NOTE This completes the setup for DMA operation.	
Sends OCTL± and next data word.	Bypasses interrupt loop. Changes from State 0 or State 10 to State 1. Status bit ST04 goes low. Seizes control of processor bus.	
	Changes from State 1 to State 2. Places contents of memory address register on ADnn-B bus; connects ODnn± to DAnn-B bus. Initiates low ADRV-B on processor control bus.	

Table 3-10. DMA Output Transfer Sequence (Cont)

HOST COMPUTER	PARALLEL INTERFACE	DISPLAY PROCESSOR
	Changes from State 2 to State 3. Status bit ST05 goes high, activating OWR± and ODR± handshaking signals to host computer.	
	Increments memory address register by two, increments word count register by one, and changes from State 3 to State 10.	
Deactivates OCTL±	Status bit ST07 goes low, OWR± terminates. Changes from State 10 to State 0.	
	NOTE	
	This sequence repeats until the host comaputer has sent the number of words specified in the set-up instructions. When the parallel interface word count register returns to zero, status bit ST04 goes high, initiating another interrupt to the display processor.	
	Sends INLx-B, sends trap address 000124_8, sends IADV-B to display processor.	Reads trap address, terminates IENA-D.
	Releases processor bus.	Recognizes that DMA sequence is complete, resumes normal operation.

3.5.4.5 Single Word Input Transfer. Input transfers are either single word transfers or multi-word transfers.

Table 3-11 shows the sequence of events for single-word input transfers; refer also to figures 3-8 and 3-10.

Table 3-11. Single-Word Input Transfer Sequence

DISPLAY PROCESSOR	PARALLEL INTERFACE	HOST COMPUTER
Places data word on DAnn-B lines, sends write data instruction.	Stores DAnn-B word in input data register, connected to IDnn± interface bus.	
Places new status word on DAnn-B bus; bits ST03 and and ST13 high. Sends write status instruction.	Loads status word into status register. Sends IWR± handshaking signal to computer. Status bit ST15 goes high. Parallel interface remains in State 0.	Sends ICTL± when ready to accept input data.
	Changes from State 0 to State 5. Sends NDRY± pulse (150 ns) to computer, clearing IWR±. Changes from State 5 to State 6.	Reads IDnn±, deactivates ICTL±.
	When ICTL± is deactivated, status bit ST15 goes low, parallel interface changes from State 6 to State 7. If status bit ST14 is high, sends interrupt to display processor, then changes to State 0. Interrupt trap address is 000120_8.	
Reads trap address. Executes parallel interface read status. If status bit ST15 is low, sequence is complete.		

At this point the display processor could initiate another input transfer, using the same procedure.

3.5.4.6 DMA Input Transfers. In the case of a multi-word transfer, the first word is a message header, the second word is the source address, and the third word is the word count.

Table 3-12 shows the sequence of events; refer also to figure 3-8.

Table 3-12. DMA Input Transfer Sequence

DISPLAY PROCESSOR	PARALLEL INTERFACE	HOST COMPUTER
Sends first word as in table 3-11.	Passes first word to host computer as in table 3-11.	Reads first word as in table 3-11.
Sends second word as in table 3-11.	Passes second word to host computer as in table 3-11.	Reads second word as in table 3-11.
Sends third word as in table 3-11.	Passes third word to host computer as in table 3-11.	Reads third word as in table 3-11.
Places read/write memory start address on DAnn-B lines; executes write address instruction. If address bits AD16 and AD17 are required, loads these into status register as status bits ST01, ST02 with a separate write status instruction.	Loads start address into its memory address register (and status register if needed).	
Places two's complement of remaining word count on DAnn-B lines; executes write word instruction.	Loads word count value into word count register. WC≠0 goes high.	
Places new status word on DAnn-B lines; executes write status instruction. Status bit ST03 is high.	Changes from State 0 to State 1. Bypasses interrupt loop. Seizes control of processor bus.	
	Changes from State 1 to State 2. Places contents of memory address register on ADnn-B lines. Connects DAnn-B response from memory to IDnn± lines. When memory sends MEMA-B, parallel interface sends IWR± to host computer.	
	Changes from State 2 to State 3, increments memory address register by two, increments word count register by one. Changes from State 3 to State 4, waiting for host computer to respond to IWR±.	Activates ICTL± handshaking line.

Table 3-12. DMA Input Transfer Sequence (Cont)

DISPLAY PROCESSOR	PARALLEL INTERFACE	HOST COMPUTER
	Changes from State 4 to State 5. Sends 150-ns NDRY± pulse to host computer, terminates IWR±. Changes from State 5 to State 6.	Terminates ICTL±.
	If WC≠0, goes back to State 1.	
	If WC=0, changes from State 6 to State 7. Sends input interrupt to GCP+, returns to State 0.	

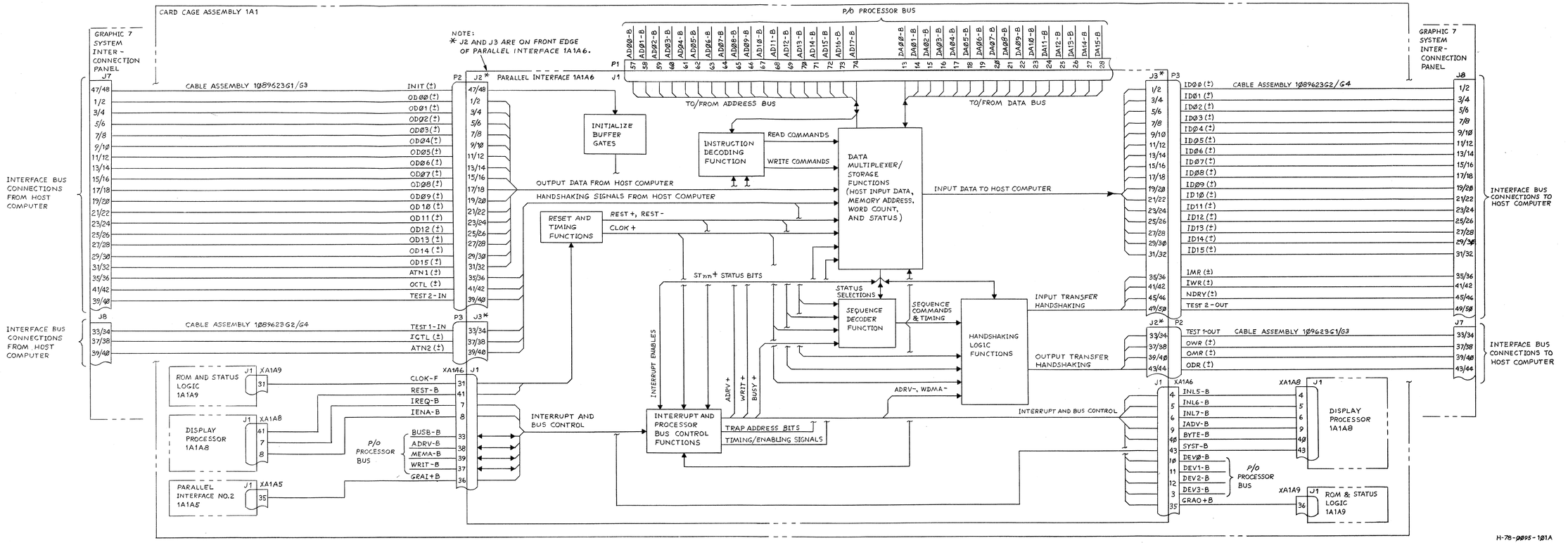


Figure 3-7. Parallel Interface Block Diagram

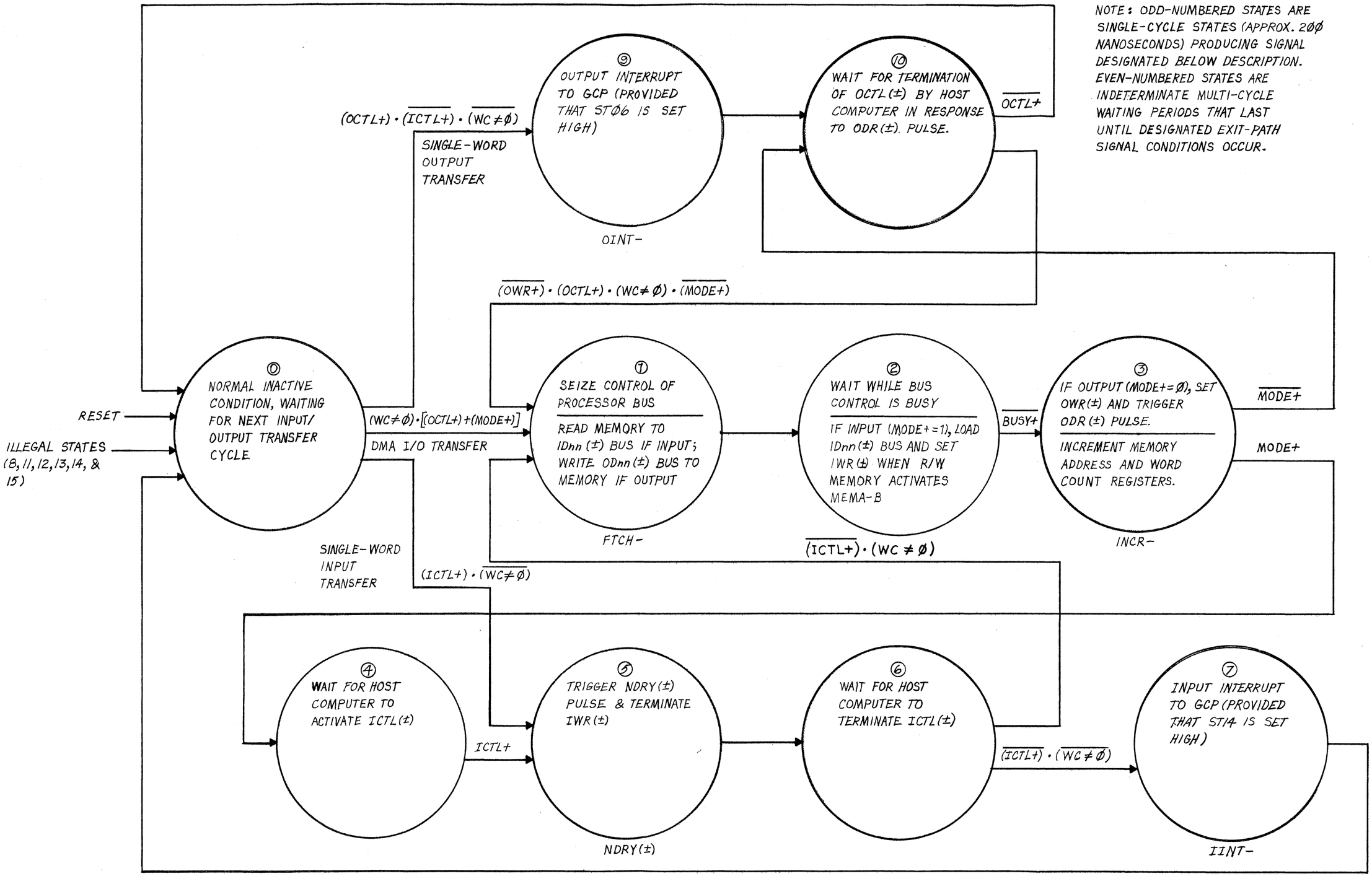


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Figure 3-8. Parallel Interface State Diagram

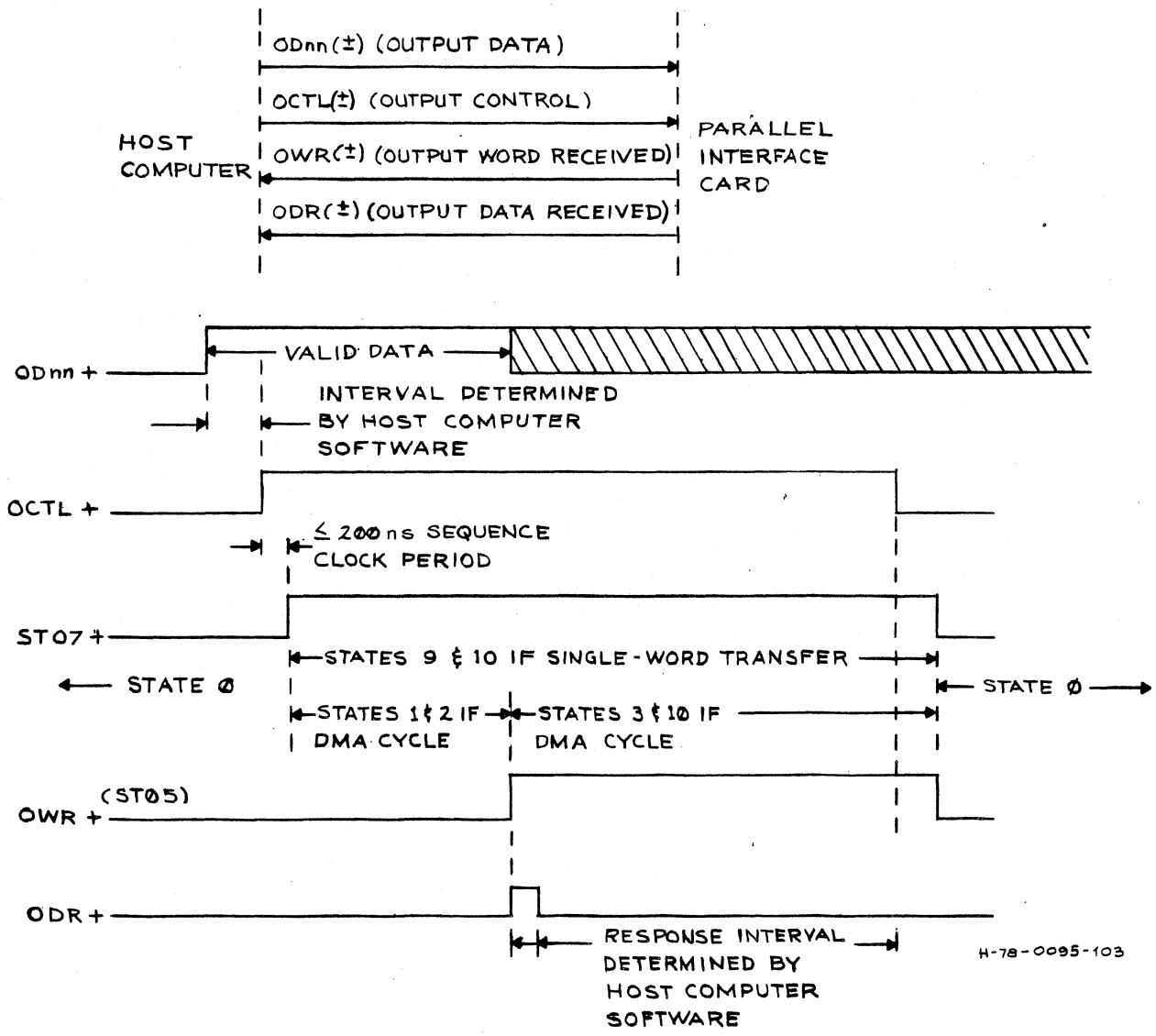

Figure 3-9. Parallel Interface Output Transfer, Timing Diagram

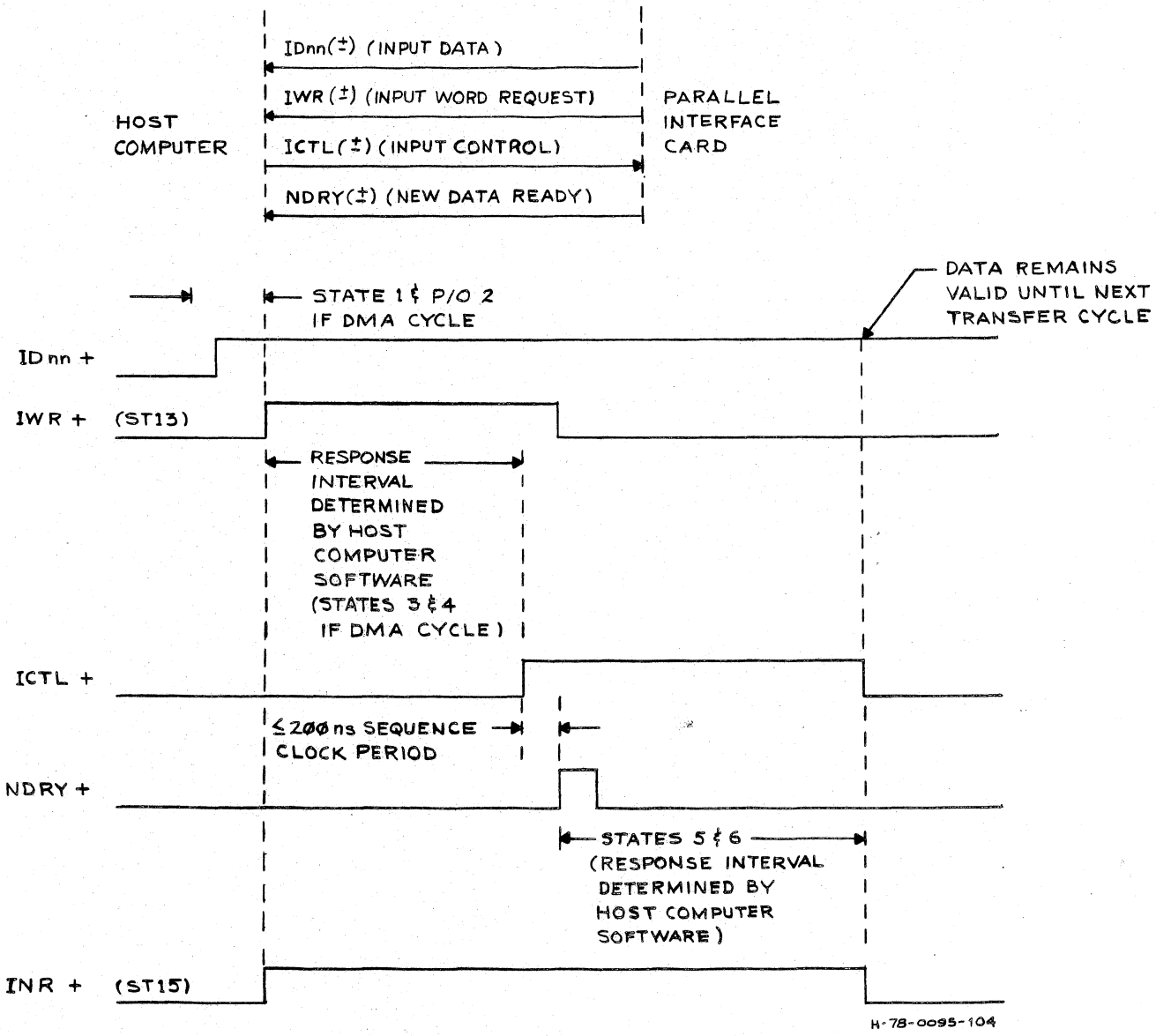

Figure 3-10. Parallel Interface Input Transfer, Timing Diagram

3.6 MULTIPORT SERIAL INTERFACE

NOTE

This paragraph describes serial interface part number 5976251. An older model, part number 1086750, is still widely used. The model described here has the following features not found on the older model:

- DIP switches for setting port address codes, baud rate, data ready, and for identifying a second serial interface card. In part number 1086750, these settings were made by jumper connections.
- A break decoder and a loopback decoder, which eliminate the requirement for external test connectors during test and troubleshooting.
- Use of a single UART for the port 1 channel. The older model used separate P/SAR and P/SAT devices for the port 1 channel.

If your terminal controller contains serial interface part number 1086750, refer to the following Sanders documents for information, drawings, and parts lists:

- H-78-0095, Terminal Controller Maintenance Manual, Volume I, Operation and Maintenance
- H-78-0096, Terminal Controller Maintenance Manual, Volume II, Diagrams and Parts Lists

The multiport serial interface is an optional circuit card that provides four separate interface channels for communications between the terminal controller (which uses parallel data) and up to four peripheral equipments that use serial data. Such equipment might be a host computer, communications modem, high speed tape reader, alphanumeric and function keyboards, or position entry devices (trackball/forcestick/data tablet).

Additional external devices can be accommodated by installing additional multiport serial interface cards. The terminal controller can handle two such cards.

Each communication channel is called a "port", which refers both to a connector on the front edge of the card and to the associated channel circuitry. Each port handles input transfers from the connected peripheral equipment to the terminal controller, and output transfers from the terminal controller to the external equipment.

The ports are designated 1 through 4 (1 through 8 in a two-card system). The port 1 circuitry can handle simple asynchronous I/O transfers and full RS-232-C communications. Ports 2, 3, and 4 handle only simple asynchronous I/O transfers. See figure 3-12.

Each port contains a universal asynchronous receiver/transmitter (UART). The port 1 channel connects to two edge-mounted connectors: J2 and J3. Connector J2, a 26-pin connector, handles all RS-232-C data and handshaking control lines needed for synchronous or asynchronous operation, in full-duplex or half-duplex modes. Connector J3, a 10-pin connector, handles asynchronous serial data transfers. Connector J3 supplies operating power (±15V, +5V and ground return), three discrete signal lines (serial input, serial output, and reader-enable confirmation), and shielded return lines for the three discrete signals. (The shields are connected together.) The I/O lines on J3 have a standard configuration for RS-232-C, but can be reconfigured for TTL logic levels.

Ports 2, 3, and 4 connect to the same type of 10-pin I/O connector as J3. The connectors for ports 2, 3, and 4 are J4, J5, and J6 respectively. The I/O lines for ports 2, 3, and 4 have a standard configuration for RS-232-C but can be reconfigured for TTL logic levels.

Each UART (see figure 3-11) contains:

1. A receiver shift register, which accepts serial character data inputs on a discrete line from the external equipment and produces various condition signals.

2. A receive buffer register, which holds the received character data until an associated control circuit requests parallel format readout.

3. A transmit buffer register, which accepts parallel character data output from the terminal controller processor bus and produces a busy/empty signal.

4. A transmitter shift register, which can be commanded to accept the data stored in the transmit buffer register and shift it out serially on a discrete line to the external equipment.

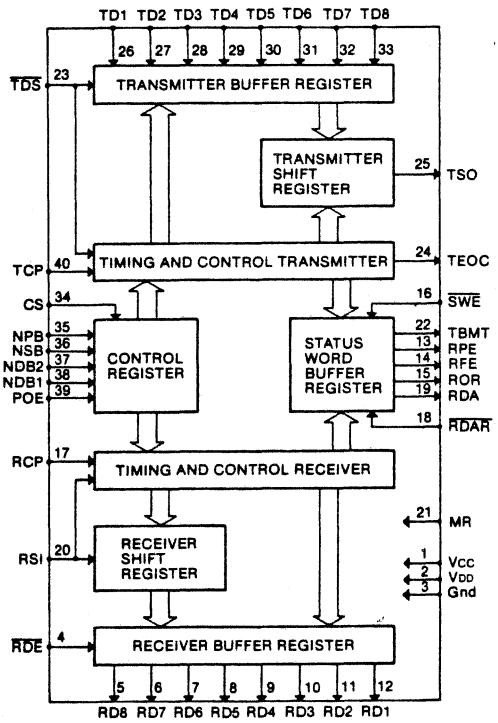

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Figure 3-11. UART Functional Block Diagram

3.6.1 MAJOR CIRCUITS

Address Decoder. This circuit recognizes when the serial interface is being addressed by another card in the terminal controller. Address bits AD06-B through AD17-B make up the card address code: $1765XX_8$.*

If the terminal controller contains two serial interface cards, both have the same card address. Individual channels are defined by bits AD03-B through AD05-B.

Bits AD03-B through AD05-B select channels 1 through 4 (if one card is used) or channels 1 through 8 (if two cards are used).

Bits AD01-B and AD02-B select one of the four UART register functions for the addressed channel.

Table 3-13 lists the 32 addresses shared by serial interface cards 1 and 2. Table 3-13 also contains the following information.

1. The register mnemonics.

*When the expand switch (U19-S8) is closed, the card address becomes $1766XX_8$. GCP+ at present does not support this address.

Table 3-13. Multiport Serial Interface Devices

CARD	PORT	OCTAL ADDRESS	REGISTER MNEMONIC	VECTOR TRAP ADDRESS RECEIVE	VECTOR TRAP ADDRESS TRANSMIT	ASSOCIATED EXTERNAL DEVICE	CARD CONNECTOR
Multiport Serial Interface Card 1	1	176500 176502 176504 176506	RSR1 RDB1, PCR1 TSR1 TDB1	300	304	Communicator 1 (RS-232-C 1, asynchronous)	J2 or J3
	2	176510 176512 176514 176516	RSR2 RDB2 TSR2 TDB2	310	314	Spare Keyboard 2	J4
	3	176520 176522 176524 176526	RSR3 RDB3 TSR3 TDB3	320	324	Keyboard 1	J5
	4	176530 176532 176534 176536	RSR4 RDB4 TSR4 TDB4	330	334	PED 1 (trackball, forcestick, or data tablet)	J6
Multiport Serial Interface Card 2	5	176540 176542 176544 176546	RSR5 RDB5, PCR5 TSR5 TDB5	340	344	Communicator 2, hardcopy unit	J2 or J3
	6	176550 176552 176554 176556	RSR6 RDB6 TSR6 TDB6	350	354	Spare	J4
	7	176560 176562 176564 176566	RSR7 RDB7 TSR7 TDB7	360	364	Keyboard 2	J5
	8	176570 176572 176574 176576	RSR8 RDB8 TSR8 TDB8	370	374	PED 2 (trackball, forcestick, or data tablet)	J6

2. The vector trap addresses sent to the display processor when the serial interface generates an interrupt.

3. The type of external equipment that may be connected by each interface port. The GCP+ always assumes that this is the type of equipment that is connected to a given port.

NOTE

The device address switches on the serial interface card let you change the port identification on a card. For example, you could connect two keyboards and a hardcopy unit to a single serial interface by identifying the channels as ports 3, 5, and 7. See Section 4 for instructions.

Device Switches. Switches U19 and U39, consisting of eight SPST switches each, perform the following functions:

1. They configure the serial interface ports to accommodate specific peripheral devices.

2. U19-S8, when closed, changes the card address from 1765XX to 1766XX.

3. U39-S7, when open, forces the DTRY+ function at connector J2.

Table 3-14 lists the device assignments for each port. When setting up these assignments, do not use the same switch settings for more than one port; only the lowest numbered port will respond to the device. If two serial interface cards are used, ports 5 through 8 are programmed in the same manner as ports 1 through 4. Do not duplicate any card #1 switch settings on card #2; if there is a duplication, neither port will work.

Table 3-14. Serial Interface Port Device Assignments

DEVICE	PORT 1 (U19) S1	S2	S3	PORT 2 (U19) S4	S5	S6	PORT 3 (U39) S1	S2	S3	PORT 4 (U39) S4	S5	S6
Communicator (RS-232-C)	On*	On*	On*	-	-	-	-	-	-	-	-	-
Keyboard #1	On	Off	On	On	Off	On	On*	Off*	On*	On	Off	On
PED #1	On	Off	Off	On	Off	Off	On	Off	Off	On*	Off*	Off*
Hardcopy	Off	On	On	Off	On	On	Off	On	On	Off	On	On
Keyboard #2	Off	Off	On	Off	Off	On	Off	Off	On	Off	Off	On
PED #2	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off
Spare #1	On	On	Off	On*	On*	Off*	On	On	Off	On	On	Off
Spare #2	Off	On	Off	Off	On	Off	Off	On	Off	Off	On	Off

*These are the nominal switch settings. Unless otherwise specified by the customer, switches are set to these positions at the factory.

Read/Write Decoder. This circuit responds to the selected address code and the states of the WRIT+ and ADRV+ signals to generate specific command signals at specific times. These command signals control the actions of other circuits throughout the serial interface card.

Mask Register. This circuit responds to the selected address code and the state of input data bit ID06+. When this bit is high, the mask register puts a high on one of eight lines that go to both the priority encoder and the status register.

This circuit lets the programmer determine which conditions will and will not cause interrupts to be generated.

Status Register. This circuit receives the eight lines from the mask register, plus the TRYX+ and DRYX+ signals from each of the four UARTs. The register is addressed by three bits from the address decoder and strobed by RIOR- from the read/write decoder. The output of the status register consists of four bits (OD04+ through OD07+) which, after inversion, go back to the display processor card on the terminal controller data bus. (Bits OD04+ and OD05+ are low.) The bits tell the display processor the current status of the serial interface.

Interrupt Status Register. This circuit receives the eight lines from the mask register and is clocked by any of the DRYX+ or TRYX+ signals from the four UARTs. The eight outputs from this register go to the priority encoder.

Priority Encoder. This circuit decodes the eight lines from the interrupt status register. If one of the mask register bits is active, the priority encoder sets the FLAG+ lines to the bus control circuit, generating an interrupt.

The 3-line coded output of the priority encoder is latched by the GRAB+ signal and passed to the reset decoder and the trap address encoder.

Bus Control Circuit. The bus control circuit operates as described in paragraph 3.3.

Reset Decoder. This circuit decodes the latched output of the priority encoder to reset the interrupt status register.

Trap Address Encoder. This trap address encoder is a multiplexer. The switched inputs are twelve DSXX+ signals from the device switches, which identify the type of device connected to each port of the serial interface. Two outputs from latch U58 select three bits as the output of the trap address encoder. The BUSC- signal strobes the trap address encoder, making those three bits available as output bits OD03+, OD04+ and OD05+.

In addition, bits OD00+ and OD01+ are low, and a third output from latch U58 passes as bit OD02+. After inversion, these bits go back to the display processor on the terminal controller data bus.

Baud Rate Generator and UARTs. Baud rate generator U79 is a clock generator with a fundamental frequency of 5.0688 MHz. The nominal output frequency (fT) is 153.6 kHz, corresponding to a baud rate of 9600.

The fT signal goes to the UARTs for ports 2, 3, and 4. The fT baud rate can be changed by changing the jumpers at the T-terminals of the baud rate generator. Refer to Section 4 for details.

The fR output of the baud rate generator goes to the UART for port 1. The nominal frequency for this terminal is also 153.6 kHz, corresponding to a baud rate of 9600. The fR baud rate can be changed by changing the settings of switches S4 through S7 on chip U80. Refer to Section 4 for details.

Each UART performs all the receiving and transmitting functions associated with asynchronous data communications. External connections give control over duplex mode, baud rate, data word length, parity mode, and the number of stop bits. The following paragraphs describe its operation.

The clock frequency is always 16 times the baud rate.

a. Transmitting. The UART is reset at power turn-on. Under these conditions, TBMT (transmitter buffer empty) and TSO (transmitter serial output) are both high.

When TBMT is high, the data bits may be set. The bits ID00+ through ID07 are applied to the UART's TR-terminals and strobed in by the WDBX- pulse at the TDS terminal. At this time TBMT goes low, indicating that the data bits buffer register is full and unable to accept additional data.

If the transmitter shift register is still sending previously loaded data, TBMT remains low. If the transmitter shift register is empty, or when it is through sending the previous character, the data in buffer register is loaded immediately into the transmitter shift register and data transmission starts. TSO (transmitter serial output) goes low and TBMT goes high.

If new data is loaded into the transmitter buffer register at this time, TBMT goes low again and stays low until the present transmission is completed.

Data transmission proceeds in this manner: start bit, data bits, parity bit (if selected), and the stop bit(s). If TBMT is low, transmission of the next character begins immediately. If TBMT is high, the transmitter is completely at rest.

b. Receiving. The UART is reset at power turn-on. Under these conditions, RDA (receiver data available) is low.

Data reception starts when the serial input line (RSI) goes low. The first bit received is a start bit, and must remain low for at least one-half a bit time. After the start bit has been received and verified, data transmission proceeds in this manner: data bits received, parity bit received (if selected), and stop bit(s) received.

If the transmitted parity bit does not agree with the received parity bit, the RPE (received parity error) line is set high. If no parity mode is selected, RPE is held low.

After a full character has been received, RDA goes high. At this time a low RDBX- signal at the UART's RDE terminal enables the outputs at the RR-terminals. The received data (OD00+ through OD07+), after inversion, goes onto the terminal controller data bus.

If a character is transferred into the receiver buffer register before the previous character was read, the ROR (receiver overrun) output goes high.

A low RDYX- pulse must be applied to the UART's $\overline{\text{RDAR}}$ (receiver data available reset) terminal to clear RDA.

c. Options. Switches S1 through S3 of chip U80 give you the option to select certain features with respect to the port 1 UART only.

When switch S1 is open, no parity bit is sent on transmission; the stop bit follows the last data bit. No parity bit is expected during receiving; the stop bit(s) must follow immediately after the last data bit. The RPE signal is held low. The NDB1 (number of data bits per character) line is held high, and in conjunction with the high NDB2 line selects 8 bits per character.

When switch S1 is closed, the parity circuit is enabled for odd or even parity, depending on the setting of switch S2, and the number of bits per character is 7.

When switch S1 is closed, on open switch S2 selects even parity; closing switch S2 selects odd parity.

Switch S3 selects the number of stop bits. Opening switch S3 selects two stop bits; closing switch S3 selects one stop bit.

Status Multiplexer. The status multiplexer detects any parity error condition or receiver overrun condition in the UARTs and reports such an error by a 3-bit code when addressed.

Readers Enable Register. These flip-flops are preset by the SREX- signals from the read/write decoder and produce the RENX- signals that allow an automatic external device (such as a tape reader) to advance to its next cycle. The circuit is cleared by the start bit when the external device sends a word.

Break and Loopback Decoders and Multiplexer. These circuits are used during tests of the serial interface card. When the break decoder is turned on, it causes a continuous SPACE on the data line, simulating the BREAK key of a teletypewriter.

When loopback decoder is turned on, its output signal LDXX+ causes the gate in the UART RSI lines to accept the data that was sent on the UART TSO lines. This feature makes it unnecessary to use external test plugs when making loopback tests.

The multiplexer, when addressed, reports the status of these devices in the form of four bits, OD00+ through OD03+.

Receiver Status Register. This circuit is involved only when transmitting to a device connected to the port 1 J2 connector. When programmed by two IDXX+ instruction bits, it activates the DTRY+ (data ready) and/or RQTS+ (request to send) lines, and reports its status in the form of three bits, OD01+ through OD03+.

3.6.2 OPERATION

3.6.2.1 Definitions of Bits. In general, communications between the display processor and the serial interface takes place in the form of "register words". Before the serial interface can pass data from an external device to the terminal controller data bus, the display processor must have prepared the serial interface to receive such data. Similarly, before the serial interface can pass data from the data bus to an external device, the display processor must have prepared the serial interface to transmit such data.

In addition, the display processor can read the status of the serial interface at any time by sending an appropriate read instruction; the serial interface responds in the form of a register word that contains the desired information.

a. Transmitting. Before the serial interface can pass data from the data bus to an external device, the display processor must prepare the serial interface to transmit such data.

The display processor sends a TSRn (transmit status register) word to one of the addresses listed in table 3-13. To do this, the display processor places the appropriate instruction on the data bus, places the appropriate address on the address bus, then activates the address valid signal ADRV- and the write command WRIT-.

The following intructions are possible:

Data bit 00, when active, enables the break decoder, causing the affected channel to send a continuous SPACE on the data line, simulating the BREAK key of a teletypewriter.

Data bit 02, when active, enables the loopback decoder, bypassing the external device and connecting the UART output of the affected port to the UART input.

Data bit 06, when active, allows an interrupt to be generated when the UART sends a word to the external device and is ready to accept another word.

After the serial interface has been set up to transmit, the display processor sends the data to be transmitted in the form of a TDBn (transmit data buffer) word, to the appropriate address (see table 3-13). To do this, the display processor places the appropriate data on the data bus, places the address on the address bus, then activates the address valid signal ADRV- and the write command WRIT-.

Data bits 00 through 07 contain the information to be passed to the external device.

b. Receiving. Before the serial interface can pass data from an external device to the data bus, the display processor must prepare the serial interface to pass such data.

This display processor sends a RSRn (receive status register) word to one of the addresses listed in table 3-13. To do this, the display processor places the appropriate instruction on the data bus, places the appropriate address on the address bus, then activates the address valid signal ADRV- and the write command WRIT-.

The following instructions are possible:

Data bit 00, when active, causes the SREX- signal to be generated, which places a ground on the RENX- pin of the addressed port. This ground is automatically cleared when the external device sends a start bit to the serial interface.

Data bit 01, when active, sets the DTRY+ (data terminal ready) line of the port 1 26-pin connector. It applies to port 1 only.

Data bit 02, when active, sets the RQTS+ (request to send) line of the port 1 26-pin connector. It applies to port 1 only.

Data bit 06, when active, allows an interrupt to be generated when the UART receives a word from the external device, and is waiting for that word to be read by the display processor.

After the serial interface has been set up to receive, the external device sends its data word. If the interrupt circuit was primed during set-up, the serial interface sends an interrupt to the display processor. The display processor then sends a RDBn (receive data buffer) command. To do this, the display processor places the appropriate address on the address bus, and activates the address valid signal ADRV-, leaving WRIT- high.

The serial interface responds by sending a 16-bit message, as follows:

Data bits 00 through 07 contain the word received from the external device.

Data bit 12, if active, indicates a parity error in the received data. This bit applies only to communications received through connector J2 of port 1.

Data bit 14, if active, indicates an overrun error (a new word was received from the external device before the display processor read the preceding word).

Data bit 15 becomes active if either data bit 12 or data bit 14 is active.

c. Reading Status. The display processor can read the conditions of the transmit function by sending a TSRn message to one of the addresses listed in table 3-13 with the WRIT- line held high. The serial interface responds by sending the status of bits 00, 02, and 06 as they were set up. In addition, bit 07, if active, indicates that the transmit data buffer in the addressed UART is empty and ready to accept another word.

The display processor can read the conditions of the receive function by sending a RSRn message to one of the addresses listed in table 3-13 with the WRIT- line held high. The serial interface responds by sending the status of bits 01, 02, and 06 as they were set up. In addition:

Bit 07, if active, indicates that the UART has a word in its receive data buffer, waiting to be read.

Bit 09, if active, indicates that the external device has set its DATA SET READY line.

Bit 12, if active, indicates that the external device has set its CARRIER line.

Bit 13, if active, indicates that the external device has set its CLEAR TO SEND line.

Bit 14, if active, indicates that the external device has set its RING INDICATOR line.

NOTE

Bits 09, 12, 13, and 14 apply to connector J2 of port 1 only.

3.6.2.2 Typical Receive Sequence. The serial interface waits in an idle condition until the external device sends a serial word. The UART stores the received word in its receive data buffer and activates its RDA terminal. The DRYX+ signal goes to the interrupt status register and the status register. If the interrupt circuit had been set up, the serial interface generates an interrupt to the display processor, at the same time sending the vector trap address for the device that causes the interrupt.

If the interrupt circuit is not set up, the display processor detects the data ready condition the next time it reads status and discovers bit 07 active.

Either way, the display processor sends a RDBn command. The serial interface responds by sending the data, accompanied by the MEMA-B signal to indicate that the data is stable on the bus. After the display processor reads the data, it terminates ADRV- and the serial interface terminates MEMA-B.

3.6.2.3 Typical Transmit Sequence. The GCP+ initiates output transfers by placing the 8-bit character data code on the low order byte lines of the data bus, activates the WRIT-B line, places the serial interface address on the address bus, and activates the ADRV-B line.

The character data goes to all four UARTs. The address decoder decodes the port selection code and sends a WDBX- (write data bit) command to the one appropriate UART; this command goes to the UART TDS terminal. The UART responds by sending the output message (one start bit, eight data bits, and one or two stop bits) to the external device; the TBMT (transmitter buffer empty) signal goes low when the data is strobed into the UART and goes high when the character has been sent to the external device.

If interrupt enable bit 06 has been previously set, the serial interface sends an interrupt back to the GCP+ when TBMT goes high. This interrupt reports completion of the transfer and readiness to transmit another character. The interrupt response sequence produces an appropriate trap vector address, which causes the program to branch to the appropriate data handling subroutine for the selected port.

If the interrupt is disabled (bit 06 cleared), the display processor can read the transmit status word directly to determine if the transmitter ready bit (bit 07) has been set.

3.6.2.4 Modem Operation. Modem operation is only through connector J2 of port 1. Modem operation is generally used for long-distance transfers (via telephone line or rf links). For asynchronous operation, the message code structure is the same as for local asynchronous transfers: a start bit, up to eight data bits, and one or two stop bits.

Modem operation protocol requires that:

a. The external device send an active DSRY+ (data set ready) signal to the serial interface.

b. The GCP+ set bit 01 of the RSR1 status instruction, to keep the DTRY+ (data terminal ready) signal to the external device high.

The serial interface is always ready to receive data from the external device. However, transfers from the GCP+ to the external device require that the serial interface send an active RQTS+ (request to send) signal and wait for a CLTS+ (clear to send) reply from the external device.

The external device sends a high CARR+ (data carrier detect) signal to the serial interface as long as detection circuits in the external device find no fault with the quality of the data from the serial interface.

The external device produces a RING+ signal that is available to the display processor as status bit 14.

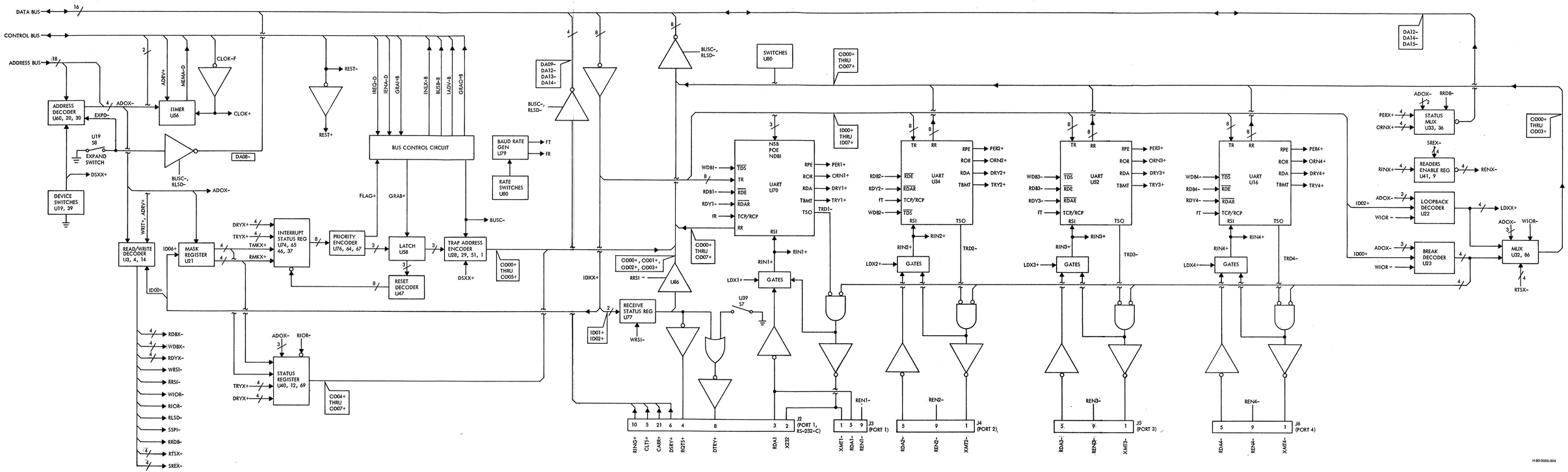

Figure 3-12. Serial Interface, Block Diagram

3.7 DISPLAY PROCESSOR

The display processor (figures 3-13 and 3-14) comprises six logic circuits: input/output, instruction, control, central processing, interrupt, and timing/ miscellaneous. These circuits, which together to emulate a PDP-11 type minicomputer (figure 3-15) are described in the following paragraphs.

Input/Output (I/O) Logic. The I/O logic is the primary interface between the display processor and other circuit cards connected to the processor bus. Input information (data or instruction) for the display processor is applied to the I/O logic on the data lines (DAnn-B) of the processor bus. The I/O logic routes the information to the instruction logic or central processing logic, as appropriate. Similarly, information from the display processor (data or address) intended for other circuit cards is routed from the central processing logic, through the I/O logic, to the processor bus. If it is data, the output information is placed on the processor bus data lines; if it is an address, the information is placed on the processor bus address lines (ADnn-B).

Instruction Logic. This circuit accepts instruction information from the I/O logic, then decodes the data to determine (a) the processor registers to be used and (b) the starting address of the microroutine that will execute the instruction. As required, the decoding operation is modified by decode control inputs from the control logic and by condition code data from the central processing logic. The resulting register selection data goes to the central processing logic while starting address data goes to the control logic.

Control Logic. This circuit determines the specific microinstruction, or series thereof, necessary to execute the macro-instruction decoded by the instruction logic. This is accomplished via a microcontrol program located in a read-only memory (ROM). Execution of an instruction is initiated by application of an address from the instruction logic to identify the proper starting location in the microcontrol program ROM. A counter then causes sequential microcontrol ROM locations to be accessed as necessary to generate the required microinstructions. Simultaneously, decode control signals required for instruction execution are generated and sent to the instruction logic.

The control logic also accepts microcontrol ROM starting locations from the interrupt logic so that microjumps to an interrupt-handling microroutine can be performed. When microroutine execution is required, the control logic sends an enable signal to the interrupt logic which responds by returning the microroutine starting location (microjump address) to the control logic.

Control Processing Logic. This circuit, which contains a 16-bit microcontroller, performs the actual data processing. In response to (a) microinstructions from the control logic, and (b) register select signals from the instruction logic, the microcontroller operates on input data received from the I/O logic and generates output data or an address that is applied to the I/O logic. The central processing logic also generates: (a) condition code signals that are sent to the instruction logic and (b) interrupt priority signals that control interrupt logic operations. As a maintenance aid, the central processing logic generates a DPRN-B (display processor run) signal to indicate that the display processor is operating. This signal lights indicator DS1 on the display processor card and the RUN indicator on the terminal controller front panel.

Interrupt Logic. This circuit monitors: (a) three levels of interrupts (INL5-B through INL7-B) from other circuit cards connected to the processor bus, (b) BTOM-M (bus timeout) signals from the read/write memories, and (c) LOCA-B (local mode) and SYST-B (system mode) commands from interface cards and pushbutton switches. Response to these interrupts is determined by interrupt priority signals from the central processing logic. When an interrupt of higher priority than the display processor is received and the control logic generates a microjump enable signal, the interrupt logic sends a microjump address to the control logic. This microjump address specifies the starting location in the microcontrol ROM of the required interrupt handling microroutine.

Timing and Miscellaneous Logic. This circuit controls the timing and coordination of all display processor functions, monitors status signals on the processor bus, applies status and control signals to the processor bus, and controls initialization of all terminal controller circuit cards.

Timing signals are derived from the CLOK-F (master clock) input from the ROM and status logic card. Normally, this is a 10-MHz signal generated by a ROM and status card circuit, but an optional external clock signal may be used.

Processor bus status signals monitored by the timing and control logic include IADV-B (interrupt address valid), MEMA-B (memory acknowledge), and GRAI+B (grant input). This signals synchronize display processor operations with those of other circuit cards, and indicate when processor bus control has been seized by another card.

When processor-bus control is seized by the display processor, the timing and miscellaneous logic applies bus status and control signals to the bus. These signals include ADRV-B (address valid), WRIT-B (write), BUSB-B (bus-busy), BYTE-B, IENA-D (interrupt enable), IREQ-D (interrupt request); DEVn-B (device code), and GRAO+B (grant output) signals.

Initialization of all terminal controller circuit cards occurs each time primary power is applied to the controller. Applying primary power causes the output channel card to send a TORN-O (turn on) pulse to the timing and miscellaneous logic which then initializes the other display processor circuits and applies a REST-B (reset) pulse to the processor bus to initialize all other terminal controller cards.

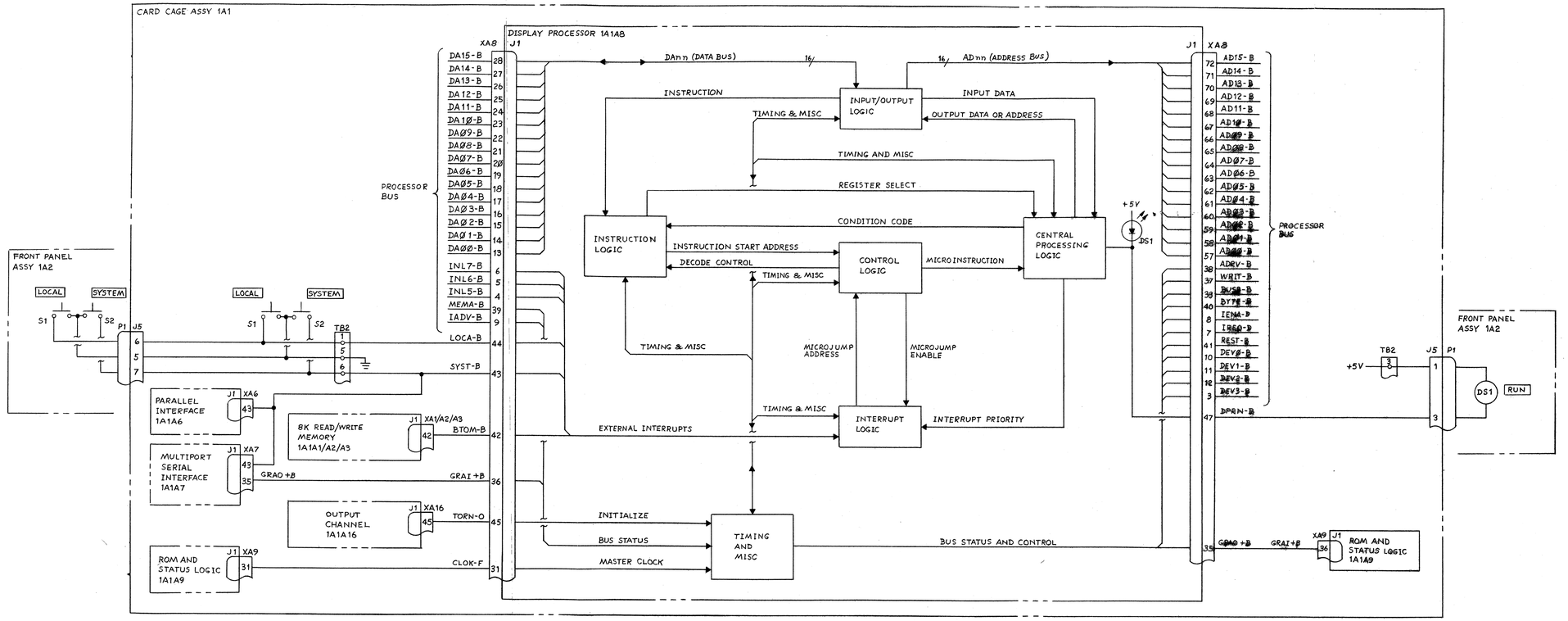

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Figure 3-13. Display Processor, Block Diagram

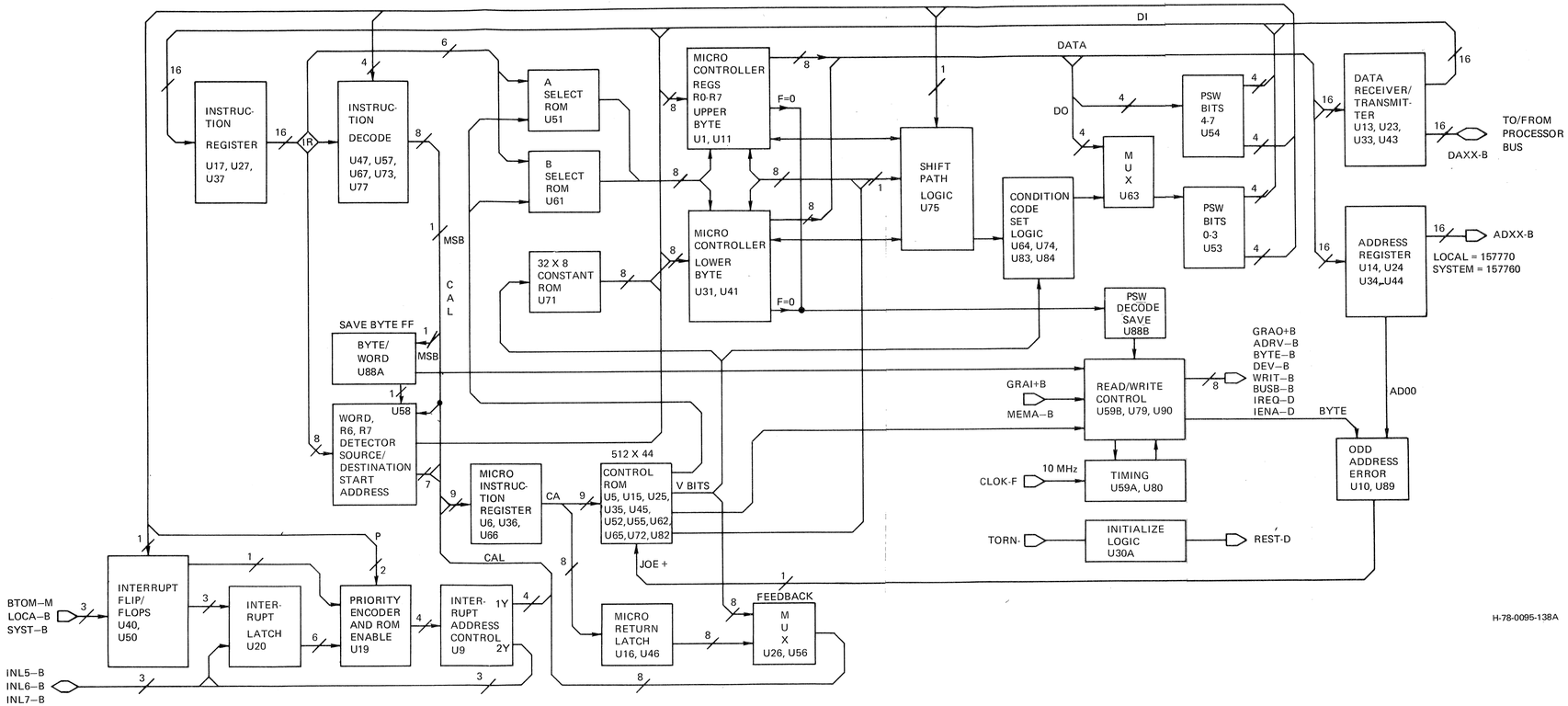


Figure 3-14. Display Processor, Functional Block Diagram

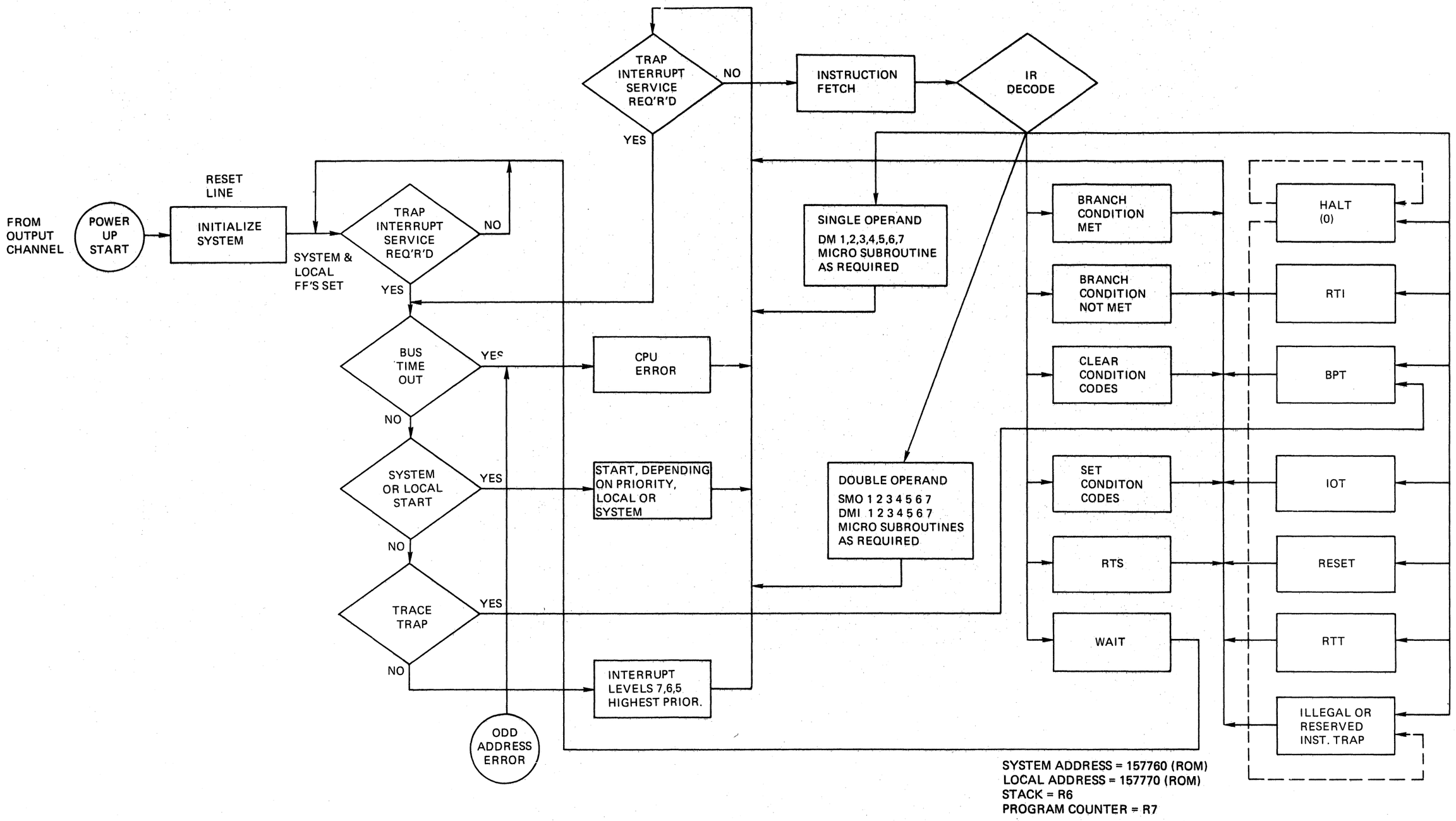


Figure 3-15. Display Processor, Flow Diagram

3.8 ROM AND STATUS CARD

NOTE

This paragraph describes two ROM and status cards. Part number 1086746 contains a 4K ROM and is used with the GCP operating program. Part number 1088683 contains 8K of ROM and is used with the GCP+ operating program. There are no other significant differences between the two cards.

The ROM and status card (figures 3-16 and 3-17) contain the ROM-stored macro-control programs used by graphic controller, display processor and option card microprocessors. These programs include GCP or GCP+ and other special-option firmware, as applicable. The circuit card is available in a number of "G" configuration (determined by the nature of the ROM programs).

The ROM and status card also contains a serial I/O communication circuit that interfaces to external equipment through connector J2. This circuit communicates with a teletypewriter to facilitate diagnostic communications. However, the design is adaptable to a variety of asynchronous-mode, serial-transfer equipments.

The ROM and status card also contains interrupt/monitor status circuits that receive various signals from the graphic controller, D/A converters, ramp or ramp/conic generator, and PHOTOPEN from the output channel card. These circuits inform the display processor of the status of the signals, with some critical inputs causing program interrupts for immediate processing.

Major circuits of the ROM and status card are as follows:

DAnn-/IDnn+ Buffer/Inverter Input Gates. These gates pass the low-order byte on DAnn-B processor data bus to the 8-bit IDnn+ input data bus. This permanently enabled connection provides GCP+ access to a universal asynchronous receiver/transmitter (UART) device for serial output transfers to: (a) teletypewriter or other external equipment, (b) an I/O status register to enable/inhibit the UART's I/O communication interrupts, and (c) a display mask register to enable/inhibit other interrupt signals applied to the ROM and status card by other circuits.

ENRM. This circuit enables ROM control logic which:

1. Enables an applicable 2K bank of ROM storage devices (RR00- through RR03, respectively).

2. Enables the ROM output as a 16-bit data word to the processor bus data lines.

3. Enables the ROM high byte output to the low order processor bus data lines.

4. Enables the ROM low byte output to the low order processor bus data lines.

5. Generates a 300 ns delay for memory acknowledge.

ENRG. This circuit enables register control logic which controls:

1. Mask register read/write

2. Sense buffer read

EIOR. This circuit enables serial I/O control logic which selects addressed registers with read/write functions.

The address decoder logic includes a jumper selection to match the size of the ROM. The standard GCP storage requirement is four kilowords located in the memory area from system addresses 140000_8 through 157776_8 (see figure 1-7). GCP+ requires 6.6 kilowords in the memory area between 140000_8 and 177777_8.

ROM Circuit. This circuit stores macrocontrol programs used by the display processor, graphic controller, and optional card microprocessors. The full ROM storage circuit comprises four separately addressed rows of 4-bit preprogrammed storage devices, with the four devices in each row producing a full 16-bit output word for each address within its address range.

The address decoder controls ROM row selection by activating only one row-read enabling signal (RR00- through RR03-) at a time. The address decoder also provides 8-bit byte selection by enabling or inhibiting the storage devices pertaining to the low-order byte data. If the LSEL- (low select) control signal is active, the low-order bits are enabled; if that signal is inactive, only the high-order bits are enabled.

Three different addressing capabilities can be established on the 8K ROM cards. Table 3-15 lists the addressing configurations for the 4K ROM card while table 3-16 lists the different relationships for three 8K ROM cards. In all cases, the corresponding read/write memory addresses must be either deleted (by not using memory card 3 in a system using memory cards) or inhibited (by manual switch settings on large 32K/64K memory cards).

Byte Select Multiplexer. This circuit passes high-order byte outputs from the program ROM to the low-order lines on the output-data bus when enabled by a low HSEL- (high select) command from the address decoder. This condition occurs when the BYTE-B (processor bus byte mode control) signals and byte selector address bit AD00-B both are low.

High-Order Byte ODnn+/DAnn- Data Output Gates. These gates, when enabled by a low HBYT- command from the address decoder, pass high order 8-bit byte from the program ROM to the high order lines of the processor data bus. When enabled by a low RRDB- (read reader data buffer) signal from the serial I/O register decoder, they pass the activity state of an OERR- (overflow error from receiver register) outout from the UART to processor bus data lines DA15-B from DA14-B.

Table 3-15. Program Address/Hardware Relationships For Different PN 1086746 4K ROM Configurations

ROM CONFIGURATION	PROGRAM ADDRESS (OCTAL)	ACTIVATED ROW READ SIGNAL	ONnn+ OUTPUT DATA BITS AND/OR DAnn-B PROCESSOR BUS DATA BITS			
			15-12	11-08	07-04	03-00
	140000 through 143777 (24K through 25K-1)	RR02-	U26	U25	U24	U23
I	144000 through 147777 (25K through 26K-1)	RR00-	U6	U5	U4	U3
(E31-E32 Jumper)	150000 through 153777 (26K through 27K-1)	RR03-	U36	U35	U34	U33
	154000 through 157777 (27K through 28K-1)	RR01-	U16	U15	U14	U13
	120000 through 123777 (20K through 21K-1)	RR02-	U26	U25	U24	U23
II	124000 through 127777 (21K through 22K-1)	RR00-	U6	U5	U4	U3
(E30-E32 Jumper)	130000 through 133777 (22K through 23K-1)	RR03-	U36	U35	U34	U33
	134000 through 137777 (23K through 24K-1)	RR01-	U16	U15	U14	U13

Low-Order Byte Data Output Gates. These gates, when enabled, pass the eight LSBs of the ODnn+ lines to the corresponding low order DAnn- data lines on the processor bus. This transfer includes any of the following:

1. Eight LSBs of any ROM word (word or byte addressed).
2. Eight MSBs of any ROM word (byte addressed only).
3. An 8-bit parallel data word from the UART as an input transfer from peripheral serial communication equipment.
4. Status bits from the serial I/O UART status register for an input or output transfer.
5. An 8-bit parallel word from the program loaded display mask register.
6. A 4-bit parallel word from the display sense buffer.
7. An 8-bit parallel word from the trap vector address encoder that defines a trap vector which contains a start address of the appropriate interrupt handling subroutine for any of the nine interrupt conditions.

Table 3-16. Program Address/Hardware Relationships For Different PN 1088682 8K ROM Configurations

ROM CONFIGURATION	PROGRAM ADDRESS (OCTAL)	ACTIVATED ROW READ SIGNAL	ODnn+ OUTPUT DATA BITS AND/OR DAnn-B PROCESSOR BUS DATA BITS			
			15-12	11-08	07-04	03-00
I	140000 through 147777 (24K through 26K-1)	RR02-	U26	U25	U24	U23
(E31-E32 Jumper)	150000 through 157777 (26K through 28K-1)	RR03-	U36	U35	U34	U33
	120000 through 127777 (20K through 22K-1)	RR00-	U6	U5	U4	U3
II	130000 through 137777 (22K through 24K-1)	RR01-	U16	U15	U14	U13
(E30-E32 Jumper)	140000 through 147777 (24K through 26K-1)	RR02-	U26	U25	U24	U23
	150000 through 157777 (26K through 28K-1)	RR03-	U36	U35	U34	U33
	100000 through 177777 (16K through 18K-1)	RR02-	U26	U25	U24	U23
III	110000 through 117777 (18K through 20K-1)	RR03-	U36	U35	U34	U33
	120000 through 127777 (20K through 22K-1)	RR00-	U6	U5	U4	U3
(E44-E32 Jumper)	130000 through 137777 (22K through 24K-1)	RR01-	U16	U15	U14	U13

Register Control Logic. This circuit decodes the processor bus address lines together with ENRG- from the address decoder to:

1. Display mask register - read/write.
2. Display sense buffer - read.
3. Generate EIOR - enables the serial I/O control logic.
4. Generate 600 ns delay for memory acknowledge.

Serial I/O Control Logic. This circuit decodes the processor bus address lines, together with EIOR- from the register control logic, to establish full communication with the UART. The data includes:

1. Reader status register - read/write.

2. Reader data buffer - read.

3. Transmitter status register - read/write.

4. Transmitter data register - write.

Display Mask Register. This circuit stores eight bit of program-selected data to enable/disable the corresponding inputs to an interrupt storage register. The display mask register is accessed by a 177662_8 address, which activates either a WMSK- (write mask) signal from the register control logic if the WRIT-B processor bus line is low, or an RMSK- (read mask) output if the WRIT-B line is high. The WMSK- signal loads the IDnn+ data word into the display mask register, enabling or disabling the program interrupt conditions. Activation of the RMSK- signal reads out the last stored value of these mask signals for status analysis. Table 3-17 lists the mask bits and their effects.

Table 3-17. Display Mask Register Bits

DAnn-B BIT	ASSOCIATED INTERRUPT CONDITION/SIGNIFICANCE
00	Not used.
01	Graphic controller refresh file program halted.
02	X-axis or Y-axis display vector overflow detection.
03	Real time clock (60-Hz interrogation rate).
04	PHOTOPEN unit 1 strike detection.
05	PHOTOPEN unit 1 switch actuation.
06	PHOTOPEN unit 2 strike detection.
07	PHOTOPEN unit 2 switch actuation.

Sense/ODnn+ Buffer Gates. The circuits, when enabled by a low RSEN- (read sense) signal from the TTY command decoder as the result of a read command addressed to location 177660_8, pass (a) PPS1 and PPS2 (PHOTOPEN units 1 and 2 switch signals), (b) graphic controller signal GCRE-G (request enable) and (c) BYTE-G (character byte) status signals as a 4-bit data word to the DAnn-B processor bus (see table 3-18).

Table 3-18. DAnn-B Processor Bus Data Word

DAnn-B BIT	SOURCE	SENSE CONDITION WHEN SET TO LOGIC "1"
04	GCRE-G	Graphic controller display refresh sequence halted.
05	BYTE-G*	Second character of text pair currently is addressed by graphic controller refresh program.
06	PPS1-	Switch in PHOTOPEN unit 1 is actuated.
07	PPS2-	Switch in PHOTOPEN unit 2 is actuated.

*Activating the BYTE-G signal does not generate a program interrupt sequence; each of the other three sense bits interrupts the GCP+ when enabled by the mask register bits.

Interrupt Status Register. Depending on (a) enable/disable status of the mask signals produced by display mask and (b) I/O status registers, this register confirms or ignores activation of nine different input interrupt signals (see table 3-19).

Table 3-19. Interrupt Status Register Input Signals

SIGNAL	ACTIVATION CONDITION/SIGNIFICANCE
HALT-G	Graphic controller display refresh sequence halted.
OVCK-E	With OFLW-A, indicates a vector overflow condition in either the X or Y D/A converter.
DRDY-	Data ready condition in UART receive buffer register (input word to be read).
TBRE-	Transmitter buffer register empty condition in UART (ready to accept next output transfer character from processor data bus).
PPD1-0	PHOTOPEN unit 1 strike confirmation from output channel card.
PPD2-0	PHOTOPEN unit 2 strike confirmation from output channel card.
RTCK-0	Real time clock pulse signal from output channel card.
PPS1-	PHOTOPEN unit 1 switch actuation.
PPS2-	PHOTOPEN unit 2 switch actuation.

Sync Storage Register. This circuit, when enabled by a low STAT+ command from the interrupt/processor bus control logic, stores the current logic state of eight mask enabled status bits from the interrupt status register. One status bit is common to both PPSn- PHOTOPEN unit switch signals.

Priority Encoder. If the LINK+ output from interrupt/processor bus control logic is low, the priority encoder activates a 3-bit code giving the octal identification of the highest valued input from the sync storage register (see table 3-20). The priority encoder ignores lower priority inputs occurring simultaneously with, or after, activation of any higher priority input; but responds to any following higher priority input. When an input is active, the priority encoder produces a FLAG- output to the interrupt/processor bus control logic, maintaining this steady state output as long as the associated sync storage register input remains active.

Table 3-20. Priority Encoder Trap Address Values

	PRIORITY ENCODER VALUE (OCTAL)	MEMORY TRAP ADDRESS (OCTAL)	INTERRUPT HANDLING SUBROUTINE
	0	140	Execution of halt refresh instruction by graphic controller
	1	144	X-axis/Y-axis position data overflow (offscreen)
	2	060	Received serial data ready for input
LINK+ inactive	3	064	Output serial data transmitted (ready for next character load)
	4	150	PHOTOPEN unit 1 strike
	5	154	PHOTOPEN unit 2 strike
	6	100	Real time clock pulse
	7	160	PHOTOPEN units 1 or 2 switch on
LINK+ active	X	170	Sync link execution

Interrupt Trap Vector Address Encoder. If the LINK+ output from the interrupt control logic is low, this encoder circuit responds to coded inputs from the priority encoder by producing an 8-bit output word specifying the trap address of the subroutine that handles the interrupt condition that triggered an active FLAG- signal (see table 3-20). When the LINK+ signal is high, the trap vector address encoder produces SYNC LINK address 1708, regardless of the priority encoder output state. In all cases, the trap address is placed on the ODnn+ output data bus for transfer (via the low order byte ODnn+/DAnn- data output gates) to the DAnn-B processor data bus.

Interrupt Register Reset Decoder. This circuit responds to coded inputs from the priority encoder by clearing the storage cell in the interrupt status register associated with the input signal that triggered an active FLAG- output from the priority encoder.

Interrupt Control Logic. This circuit initiates an interrupt-processing sequence in response to activation of (a) nonmaskable LINK-G link interrupt commands from the graphic controller or (b) unmasked FLAG- interrupt signals from the priority encoder. In either case, the sequence begins with activation of the IREQ-D interrupt request signal from the display processor at the end of the instruction cycle during which the FLAG- input or the LINK-G input goes active.

If the FLAG- input is the trigger signal, activation of IREQ-D places an active low on the INL5-B interrupt priority line.* If the LINK-G input is the trigger signal, the IREQ-D input produces an active low logic level on the INL7-B interrupt-priority line.* The circuit then waits until the display processor card responds to INLn-B with an active low IENA-D interrupt enable. If the interrupt cycle was triggered by FLAG-, STAT+ is activated and halts transfer of interrupt signals from the sync storage register to the priority encoder. This means that the priority encoder cannot change state until the announced interrupt condition is processed, ensuring that the established trap address output from the interrupt trap vector address encoder remains valid. If the interrupt cycle was triggered by LINK-G, however, LINK+ is activated to (a) inhibit the priority encoder, and (b) condition the interrupt trap vector address encoder to produce the 170_8 trap address associated with sync link operation.

When the ROM and status card receives an active GRAI+B input, the interrupt control logic deactivates its GRAO+B output to inhibit the graphic controller card from seizing control of the processor bus. Simultaneously, the interrupt control logic activates BUSC-, BUSB-B, and DEV1-B. Internally, BUSC- enables the interrupt trap vector address encoder (transferring the selected trap address code onto the ODnn+ output data bus) and enables the low order byte ODnn+/DAnn- data output gates to pass that trap address code to the DAnn-B processor data bus. Simultaneously, if the interrupt condition is a FLAG-triggered sequence, the interrupt control logic activates an interrupt reset signal to keep (a) the sync storage register inhibited, and (b) cause the interrupt reset decoder to produce a 1-of-8 output code that clears the interrupt status register storage cell that created the FLAG- signal.

Externally, BUSB-B prevents other processor bus circuit cards from seizing control of the bus during the remainder of the interrupt-handling sequence. DEV1-B is not part of the standard system, but may perform active functions with certain optional circuit cards. If, for example, the system includes a large read/write memory card, the active DEV1-B signal informs that memory card that the bus controller for the coming operation is the ROM and status card, thereby inhibiting the memory-mapping circuits normally used when the display processor is in control.

One CLOK+ pulse period later, the interrupt control logic activates a low IADV-B signal that directs the display processor to examine the valid interrupt trap address word now on the DAnn-B processor bus data lines. The same CLOK+ pulse then deactivates BUSB-B and DEV1-B, in turn deactivating the ODnn+/DAnn- enabling logic, releasing the sync storage buffer, and terminating the enabling condition of the interrupt reset decoder.

*The designated FLAG- and LINK-G priorities are the standard jumper selections. Actually, either IREQ-D loaded interrupt condition can be jumpered to the INL5-B, INL6-B, or INL7-B lines in any desired combination.

The subsequent termination of the IENA-D input allows the control logic to return to its normal quiescent state, deactivating STAT+ or LINK+, as applicable. If this cycle was triggered by FLAG-, termination of STAT+ and IRST- reenables the sync storage register. If any lower priority interrupt signals were loaded into the interrupt status register during the completed sequence, this same sequence is repeated to handle that lower-priority interrupt condition.

If the cycle was triggered by LINK-G, termination of LINK+ reenables the priority encoder and the interrupt trap address encoder to respond to any interim or subsequent interrupt inputs.

PHOTOPEN Delay Enable Logic. This circuit generates a PPDE-F (PHOTOPEN delay enable) level to the graphic controller card whenever the PHOTOPEN logic is enabled on the output channel card by the display parameter register. This condition causes the graphic controller to go into a 900-nanosecond wait routine at the end of all displayable refresh commands (a) in anticipation of a PHOTOPEN strike at the very end of a vector/character, and (b) to allow for the delay while PHOTOPEN and associated interrupt logic circuits generate PPDT-F (PHOTOPEN strike detect). If PPDT-F occurs before the 900-nanosecond wait, the graphic controller halts refresh before fetching the next command. PPDT-F is derived from the interrupt status register to indicate PHOTOPEN 1 or 2 strike, or X, Y overflow condition.

Memory Acknowledge Generator. This circuit places an active low on the MEMA-B processor bus control line after completion of an instruction operation setup. For ROM readouts, this condition occurs within 300 nanoseconds (i.e., three 10-MHz CLOK-F pulsetrain periods) after activation of the RDRM- (read ROM) enabling signal to the ODnn+/DAnn- output enabling logic. For serial I/O data transfers through the UART or write/read registers, this condition is delayed an additional 300 nanoseconds by routing the applicable outputs from the register control logic to the timing delay circuit.

Universal Asynchronous Receiver/Transmitter (UART). This device services a full duplex serial communication channel through connector J2. The UART accepts serial data from a teletypewriter (or other serial communication equipment) and converts it to an 8-bit parallel word on the ODnn+ output data bus for passage to the DAnn-B processor data bus. Conversely, the UART accepts 8-bit parallel data from the IDnn+ input data bus and transmits it in serial format to the external equipment.

The UART sends two transfer operation signals to the interrupt sense/status mask register. One signal is the low DRDY- (data ready) applied after the UART has placed a received word in its internal receive data buffer register. The other signal is the low TBRE- (transmit buffer register empty) that goes low after the last output word has been passed to the internal serial transmit circuit, and the UART is ready to accept a new word from the IDnn+ bus for transfer to the external equipment.

These outputs initiate program interrupt sequences, producing trap addresses to branch the program to the appropriate handling subroutine for the I/O transfers. Note that these interrupts can be masked by program control of the I/O status register, which monitors DRDY- and TBRE- signals for direct readout by the program when applicable.

I/O Status Register. This circuit stores (a) program-selected values of DA00-B and DA06-B data bits (written to address 177560_8) as external equipment reader enable/inhibit and receive interrupt enable/inhibit commands, and (b) the value of data bit DA06-B (written to address 177564_8) as a transmit interrupt enable/inhibit command. The I/O status register sends an RDEN- (reader enable) signal to the external equipment if DA00-B is loaded as a logic low at 177560_8; this signal is cleared when the external equipment sends a serial input word to the UART. The stored DA06-B values are reproduced as RMSK+ (receive mask) and TMSK+ (transmit mask) signals, respectively. These signals are applied to the interrupt status register as conditioning signals for the storage cells receiving DRDY- and TBRE- interrupt signals from the UART. Consequently, the stored value of the two mask bits determines whether the GCP+ is interrupted when either UART readiness signal becomes activated.

Under program control, the I/O status register passes output data bits OD04+ through OD07+ to the DAnn-B processor data bus to identify the current I/O communication status. Two data values are possible: one when the program calls for a readout of receiver status (address 177560_8); the other, when the program calls for a readout of transmitter status (address 177564_8). In either case, bits 04 and 05 are always inactive. Bit 06 identifies the current value of the corresponding interrupt enable/inhibit bit (receive or transmit) in the I/O status register. Bit 07 identifies the current value of the corresponding transfer-operation output (DRDY- or TBRE-) from the UART. The display processor program can therefore be coded to inhibit I/O interrupts, but to maintain communication with the external I/O equipment by reading out the monitor circuits as part of a service loop in the program sequence. Tables 3-21 through 3-24 summarize the programming capabilities for I/O communication through the serial-interface connector J2.

Input Conditioning Logic and Gating. This circuit passes the serial RDAT+ (received data) signal from the external equipment to the UART. The conditioning logic incorporates jumper options for adapting the UART's receiver input line to teletypewriter outputs (the standard 20 mA current loop selection), TTL logic levels, or RS-232C logic levels.

Output Conditioning Logic and Gating. This circuit passes the UART's serial transmitter output signal to the external equipment. The conditioning logic incorporates jumper options to adapt the UART's output to the standard teletypewriter 20 mA current loop, RS-232C communication signals, or TTL logic level.

Baud Rate Generator. This circuit supplies common receive mode and transmit mode clock train signals to the UART, using the selected countdown of a free running crystal controlled oscillator. The standard setting is a rate of 110 baud. Other jumper-selected rates for user equipments cover common industry I/O rate choices; i.e., 300, 1200, 1800, 2400, 4800, or 9600 baud. Note that the UART clock input lines can be jumped to a 50-kiloword output from the independent system clock circuit.

Table 3-21. TTY Receive Status Register (Address 177560_8) Bit Descriptions

DAnn-B BIT	NAME	FUNCTION DESCRIPTION
00	Reader enable	Program read/write, cleared by system reset. When set, this bit establishes an active low RDEN- reader enable signal on pin 9 of I/O connector 1A1A9J2 to advance the associated external equipment to the next transfer cycle (if applicable). This bit is cleared when a serial data START bit is received from the external equipment, and must be rewritten as part of the data read sequence for each character.
06	Receiver interrupt enable	Program read/write, cleared by system reset. When set (the normal condition), this bit allows a program interrupt to be generated whenever the DRDY- (data ready) signal from the UART goes active.
07	Receiver ready	Program read only, cleared by system reset. This bit is set when the UART device accepts a character code from the external equipment and stores that data in its receive data buffer. The bit is cleared when the program reads the receive data buffer. If bit 06 has been set, setting this bit generates a program interrupt.

Table 3-22. TTY Transmit Status Register (Address 177564_8) Bit Descriptions

DAnn-B BIT	NAME	FUNCTION DESCRIPTION
06	Transmitter interrupt enable	Program read/write, cleared by system reset. When set (the normal condition), this bit allows a program interrupt to be generated whenever the UART activates its TBRE- output following transfer of the last loaded character into its internal shift register for transmission to the external equipment.
07	Transmitter ready	Program read only, set by system reset. This bit is cleared when the program writes new data into the UART, then is reset after the UART transfers that parallel data to its serial output shift register, presenting the first bit to the external equipment (meaning the UART is ready to accept another character from the program).

Table 3-23. TTY Receive Data Buffer (Address 177562_8) Bit Descriptions

DAnn-B BIT	NAME	FUNCTION DESCRIPTION
00 through 07	Received data	Program read only. These bits contain the latest received serial character data stored by the UART as input from the TTY (or other J2-connected external equipment). If the applicable character code length is less than eight data bits, the unused high order bits are inactive (logic 0).
14	Overrun error	Program read only, cleared by system reset. This bit is set when the UART detects a data-overrun condition (i.e., receipt of a new character code from the external equipment before the GCP+ has read out the last character). This bit is updated each time a new character code is received from the external equipment.
15	Error	Program read only, cleared by system reset. This bit is set when the UART overrun error flag (bit 14) is set. This bit is cleared when the overrun error bit is cleared.

Table 3-24. TTY Transmit Data Buffer (Address 177566_8) Bit Descriptions

DAnn-B BIT	NAME	FUNCTION DESCRIPTION
00 through 07	Transmit data	Program write only. These bits are the character data codes loaded into the UART's transmit data buffer by the program for transfer to the J2-connected external equipment.

System Clock. This circuit generates the 10 MHz (CLOK-F) system clock frequency used by all processor bus circuit cards as the basic timing signal for system operations. The free running clock circuit generates CLOK-F (also available on the ROM and status card as CLOK+/CLOK-) by dividing the output of a 20 MHz crystal oscillator. The system clock circuit also produces a 50KB-F output available for use by other processor bus cards.

Voltage Filters. These devices are inductive pi-network that filters that smooth and isolate the +15V, -15V, and +5V lines to the external communications equipment.

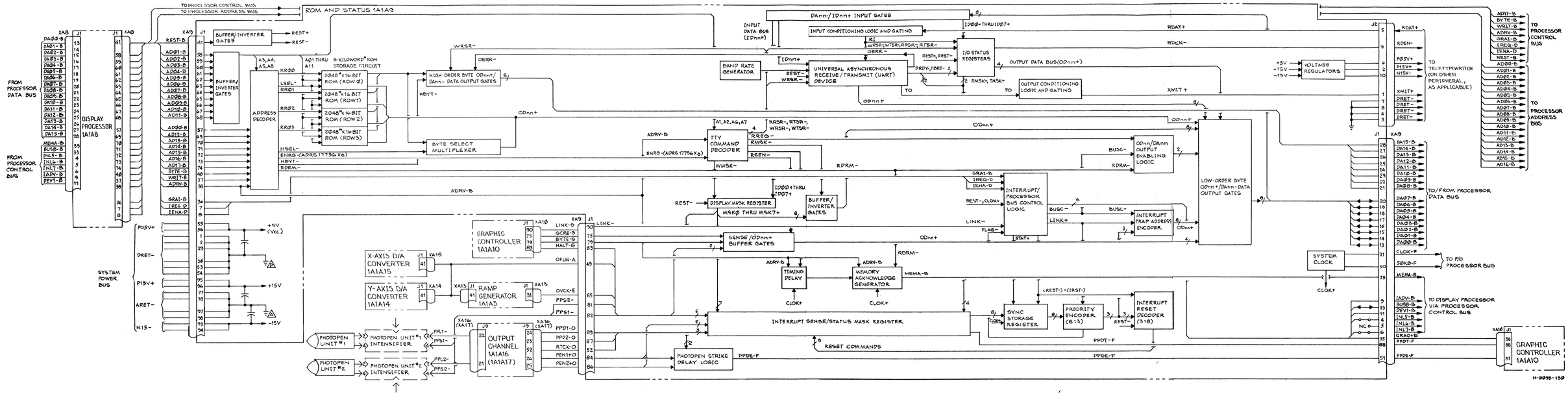


Figure 3-16. ROM and Status Card, Block Diagram

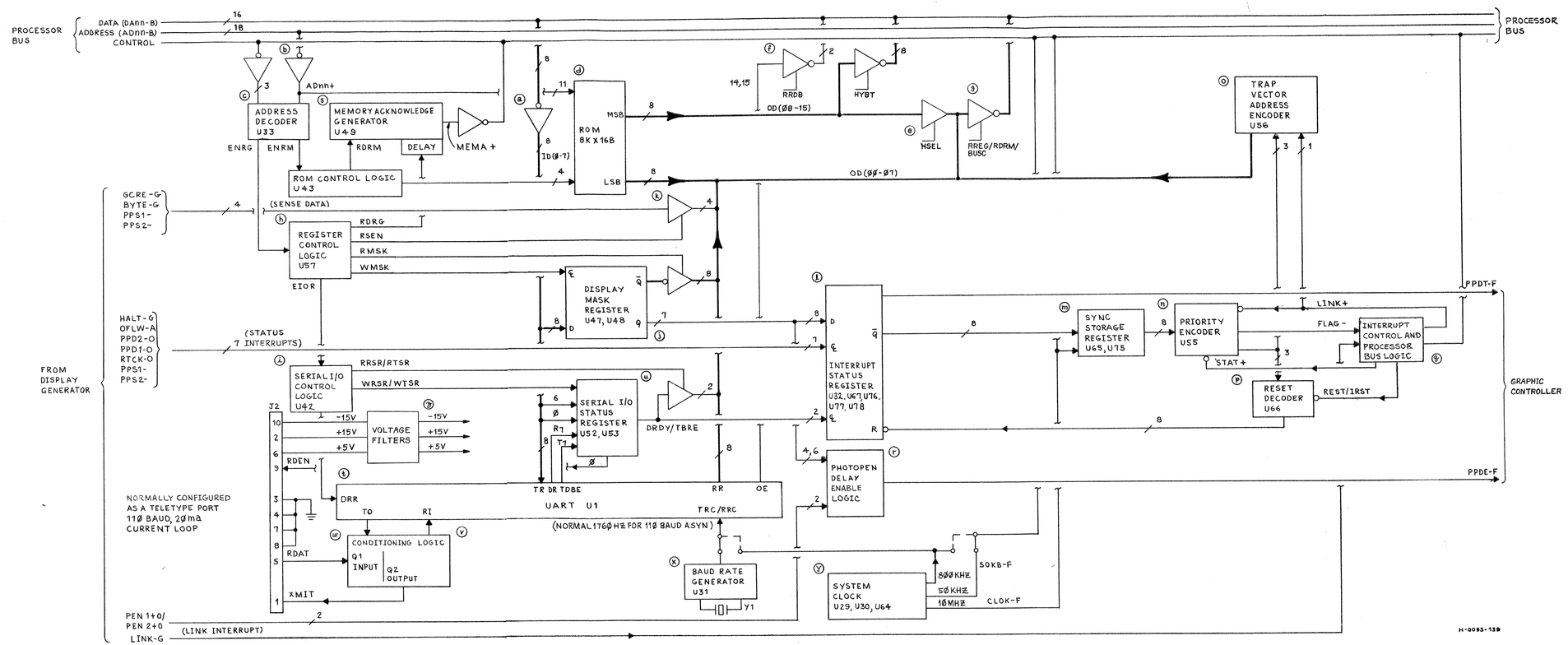


Figure 3-17. ROM and Status Card, Functional Block Diagram

3.9 GRAPHIC CONTROLLER

The primary functions of the graphic controller are to retrieve the display instructions from refresh memory; extract, reformat, calculate, and distribute the data contained in these instructions; and initiate the actions required by the instructions. The instruction set is described in the programmer's reference manuals listed in Appendix C.

The graphic controller maintains the instruction address, controls instruction memory fetches, and performs any branching specified by control (non-graphic) instructions.

The graphic controller also initiates the operations required to execute the draws and moves specified by the graphic instructions. Each graphic instruction consists of an operation code, which specifies the action required, and the data which is to be distributed. The graphic instructions require the distribution (loading) of the data into a data register located in the graphic controller, the vector/position generator, the character generator, the output channel, or the optional conics generator. A move instruction requires the additional step of moving the beam, blanked, to the position indicated by the data. A draw instruction is a move instruction with the beam unblanked.

The graphic controller (figure 3-18) contains logic circuits that can be grouped into six functional areas: input/output logic, instruction logic, control logic, central processing logic, function decode logic, and timing and miscellaneous logic. These circuits operate together to (a) process display instructions contained in refresh files and (b) control the image-generating circuits on other circuit cards. These circuits are described in the following paragraphs.

3.9.1 MAJOR CIRCUITS

Input/Output Logic. This circuit handles all information sent to or from the graphic controller via data bus lines (DAnn-B) or address bus lines (ADnn-B) on the processor bus. The I/O logic contains three registers and a read-only memory (ROM) for this purpose.

Input information handled by the I/O logic comprises (a) graphic controller input data and instructions received via the data bus lines and (b) register addresses received via the address bus lines. Input data and instructions are loaded into an instruction register and applied to the instruction logic. Register addresses go to a ROM which decodes the addresses and sends signals to the control logic to initiate a read/write operation as required.

Output information handled by the I/O logic comprises (a) data applied to the processor bus data bus lines and (b) refresh file addresses applied to the processor bus address lines. Both types of output information come to the I/O logic from the central processing logic. Data passed via the I/O logic are graphic controller register data generated in response to a display processor register read command. These data are applied to the data bus lines via an output data register in the I/O logic. The output addresses placed on the address bus lines are memory locations containing the refresh file (display instructions) to be processed by the graphic controller. These addresses are generated by the central processing logic and applied to the address bus lines via a display program counter register in the I/O logic.

Instruction Logic. This circuit accepts instruction information from the instruction register in the I/O logic and decodes the information to initiate the required action. The OP code portion of each instruction is decoded to determine the starting location of the microroutine that executes the instruction. The starting location is applied to the control logic. If the decoded instruction contains data, the data are separated from the instruction and sent to the central processing logic.

Control Logic. This circuit determines the microroutines required to execute each graphic controller instruction. This is accomplished via a control program in the 512-by-40-bit ROM contained in the control logic. The starting location of each microroutine is selected by input signals from the instruction logic. A control logic counter then sequences through the remaining ROM addresses of the microroutine.

Microroutines are also used to execute register read/write operations in response to display processor commands. When a register read/write operation is required, the register address is decoded by a ROM in the I/O logic which determines the microroutine to be used. The starting location of the microroutine is then applied to the control logic to initiate execution of the microroutine. A control logic counter then sequences through the remaining addresses of the microroutine.

As each ROM control program address is accessed during execution of a microroutine, the control ROM generates a set of 40 output signals, consisting of microinstructions, display function select signals, and function control signals (see table 3-25). Microinstructions go to the central processing logic; the display function select signals go to the function decode logic; and function control signals go to the ramp generator, character generator, and output channel to control their display functions.

The control logic also receives external control signals: NULL-C (null) from the character generator, PPDE-F (PHOTOPEN delay enable) from the ROM and status logic, and TOGL-E (toggle) from the ramp generator. NULL-C prevents a text increment operation from being performed when a null character is drawn by the character generator; PPDE-F enables a microroutine branch condition for PHOTOPEN operations; and TOGL-E permits the state of the ramp generator toggle flip-flop to be sensed and retained as necessary to accommodate special system operating conditions (e.g., using the display indicator to display both graphics and radar images).

As a maintenance aid, nine LEDs (DS1 through DS9), indicate the states of the ROM address input at all times.

Central Processing Logic. This circuit, which contains a 16-bit microcontroller, processes data within the graphic controller. The processing microinstructions are applied to the central processing logic from the control logic. Data to be processed comes from the instruction logic.

Central processing logic outputs include addresses and data. Addresses go to the I/O logic DPC register to select graphic controller instructions from the refresh file. Data are applied to the processor bus or the graphic bus by the applicable microroutine as required. When a register read operation is performed, data are generated by the central processing logic and sent to the processor bus data bus lines (DAnn-B) via the output data register in the I/O logic. When a display instruction is executed, the resulting data are placed directly on the graphic bus lines (DBnn-G) by the central processing logic.

Table 3-25. Graphic Controller Control ROM Bit Assignments

BIT	MNEMONIC	DESCRIPTION
0	I_0	Microcontroller microinstruction code.
1	I_1	
2	I_2	
3	I_3	
4	I_4	
5	I_5	
6	I_6	
7	I_7	
8	A_0	Microcontroller A address bit 0; shift data override; absolute branch address bit 0.
9	A_1	Microcontroller A address bit 1; branch address bit 1.
10	A_2	Microcontroller A address bit 2; branch address bit 2.
11	A_3	Microcontroller A address bit 3; branch address bit 3.
12	B_0	Microcontroller B address bit 0; function decoder bit 0.
13	B_1	Microcontroller B address bit 1; function decoder bit 1.
14	B_2	Microcontroller B address bit 2; function decoder bit 2.
15	B_3	Microcontroller B address bit 3; function decoder bit 3.
16	C_N	Microcontroller carry input.
17	MBEN-	Memory busy enable (causes wait if memory is busy).
18	FGEN-	Function generator enable (enables function decoder).
19	SREL-	Short relative sign extension; branch address bit 4.
20	TINC-	Text increment sign extension; branch address bit 5.
21	RELA-	Relative sign extension; branch address bit 6.
22	LBYT-	Left byte select, branch address bit 7.
23	POST-	Position sign extension; branch address bit 8.
24	FTCH-	Fetch (initiates memory fetch).

Table 3-25. Graphic Controller Control ROM Bit Assignments (Cont)

BIT	MNEMONIC	DESCRIPTION
25	WRIT-	Write (low = write, high = read; FTCH- bit must be low).
26	DAVL-	Data available (loads output data register for I/O transfers).
27	SLDP-	Select display parameter register (for display processor read display parameter register).
28	NEXT-	Next instruction (low true in last step of each instruction; loads address counter with start address of next instruction).
29	GCRE-	Graphic controller request enable (low when graphic controller halted).
30	FBEN-	Function generator busy enable (causes wait if a function generator is busy).
31	RAEN-	Radar branch test (radar capability expansion bit).
32	VPS1+	Vector position start 1 (vector position information bit to ramp generator).
33	VPS2+	Vector position start 2 (vector position information bit to ramp generator).
34	ROEN-	Rotate énable (causes Y axis incrementing for rotated characters).
35	NLEN-	Null enable (disables tab moves if NULL- from character generator is low true).
36	VPST-	Vector position start (start instruction to ramp generator).
37	BRT0+	Branch test bit 0.
38	BRT1+	Branch test bit 1.
39	BRT2+	Branch test bit 2.

NOTE: Branch conditions established by BRT0 through BRT2 as follows:

BRT2+	BRT1+	BRT0+	BRANCH CONDITION
L	L	L	Absolute (unconditional)
L	L	H	TOGL flip-flop (conditional branch)
L	H	L	Not used
L	H	H	PHOTOPEN enabled (conditional branch)
H	L	L	Zero detect (conditional branch)
H	L	H	Indirect bit (conditional branch)
H	H	L	Radar request (conditional branch)
H	H	H	Branch inhibit

Timing and Miscellaneous Logic. This circuit provides timing signals to coordinate the operation of all graphic controller circuits. The timing signals are derived from the CLOK-F (master clock) input from the ROM and status logic. CLOK-F is normally a 10-MHz signal generated by the ROM and status logic, but an optional external clock signal may be used.

The timing and miscellaneous logic accepts control inputs from other terminal controller cards. These input signals include: REST-B (bus reset) from the display processor; PPDT-F (PHOTOPEN detect interrupt) from the ROM and status logic; SYNC-O (frame sync) from the output channel, and FBSY- (function busy) from any of several cards connected to the graphic bus. Each signal modifies the timing and miscellaneous logic outputs as required to coordinate graphic controller operations with the operations performed by other cards. Auxiliary inputs are also provided to accommodate systems configured to operate with various external equipments.

A third timing and miscellaneous logic function is to monitor and generate processor bus status signals; i.e., BUSB-B (bus busy), WRIT-B (write), ADRV-B (address valid), MEMA-B (memory acknowledge), and GRAI+ (grant input). Except for GRAI+, each signal can be either an output (when the graphic controller controls the bus) or an input (when another device controls the bus). GRAI+ is an input signal only, and is generated by the ROM and status logic to indicate that the graphic controller may control the bus (high GRAI+) or that another device controls the bus (low GRAI+). Note that, in a standard terminal controller configuration, the graphic controller position gives it the lowest priority with regard to being able to assume processor bus control.

Two additional signals generated by the timing and miscellaneous logic are BYTE-G (byte) and GCRE- (graphic controller request enable), which are sent to the ROM and status logic. The BYTE-G signal goes low to indicate a byte operation is being performed by the graphic controller; and is high to indicate a word operation is being performed. GCRE- indicates when the graphic controller is running (GCRE- high) or when the graphic controller is halted (GCRE- low). As a maintenance aid, the complement of GCRE- (GCRE+G) is monitored by LED indicators DS10 (marked RUN) on the graphic controller card and DS2 (marked DISPLAY) on the terminal controller front panel assembly. These indicators light when the graphic controller is running and go out when the graphic controller is halted.

Function Decode Logic. This circuit decodes function select signals generated by the control ROM in the control logic (function select signals correspond to the microcontroller B address signals listed in table 3-26). The resulting function control signals are then distributed as required to circuit cards to produce the display image. Specific signals generated by the function decode logic and their destinations are shown in figure 3-18.

Table 3-26. Graphic Controller Microcontroller Register Addresses and Function Control Signal Selection Codes

B ADDRESS BIT				MICROCONTROLLER REGISTER	FUNCTION CONTROL SIGNAL
B_3	B_2	B_1	B_0		
0	0	0	0	DR0	HALT-
0	0	0	1	DR1	LDIR-
0	0	1	0	DR2	FRDY-
0	0	1	1	DR3	DRDY-
0	1	0	0	DW0	LINK-
0	1	0	1	DW1	VPIZ-
0	1	1	0	DSP	WAIT-
0	1	1	1	DPC	LDMA-
1	0	0	0	DTI	STRT-
1	0	0	1	DPR	STDP-
1	0	1	0	DZR	STDZ-
1	0	1	1	DCR	STDC-
1	1	0	0	DYR	STDY-
1	1	0	1	DXR	STDX-
1	1	1	0	KYR	STKY-
1	1	1	1	KXR	STKX-

NOTE: Function control signals are generated only when the FGEN- (control ROM bit 18) signal is low true.

3.9.2 OPERATION. When refreshing, the graphic controller requests and gains control of the graphic bus. The display program counter contains the address of the next instruction in the refresh memory. The next instruction can be loaded into the instruction register as soon as the previous instruction data has been used. This enables fetching and loading the next instruction while the function generator is busy. This process of fetching and executing instructions continues until a wait control bus command occurs. The next frame sync pulse restarts the refresh process.

The execution of an instruction is as follows: The nine operation code bits in the instruction are used by the refresh instruction decoder to point to the starting address for each microinstruction routine in the control ROM. At the start of the execution, this starting address is loaded into the ROM address counter. The address counter is normally incremented by the sequence control and sequences through the steps required for the instruction. The address counter is loaded instead if conditional or absolute branching is microprogrammed so as to repeat a sequence or to jump to a different sequence. The address counter is normally incremented every 300 ns, but the cycle time can be delayed if the micro step enables it by gating off the clock with a wait-if-busy condition. The last word of a refresh instruction has a "next instruction" bit which forces the address counter to be loaded with the starting address of the next instruction sequence.

The execution of certain instructions requires sign extending or byte swapping. The appropriate micro steps of the instruction contain ROM bits which control the byte and sign extend multiplexer so that the current data is entered into the microcontroller. All micro steps for a given instruction are executed sequentially unless one of the following conditions occur when enabled: branch absolute, branch if indirect, branch if zero, branch if PHOTOPEN enabled, and branch if radar request. The eight LSBs of the branch address, which are programmed in the control ROM, go to the address counter when enabled through the address multiplexer. The address counter MSB remains unchanged after conditional branching, while absolute branching sets the MSB. Absolute branching, therefore, can only be done to the upper 256 locations of the 512 x 40-bit control ROM.

The functions "rotate" and "null" are performed external to the microcontroller. An enabled "rotate" status forces the LSB of the microcontroller B register select to true so that the DY register is modified by the text increment instead of the DX register. The "null" indication, from the character generator, disables the text increment function. The microcontroller instruction is modified so that the text increment data is not added to the X (or Y) position register. The vector start, to the vector position generator, is also disabled.

If the graphic controller is stopped while executing a graphic instruction, the address counter resets when the current instruction is completed. The address multiplexer is disabled so that the stop, rather than the next starting, address is loaded into the address counter.

The graphic controller can be stopped by a function command from the display processor, by a halt or link refresh command, or by a PHOTOPEN strike. While at the stop address, the graphic controller enables and waits for a read or write register command or a continue function command from the display processor. The control instruction decoder is enabled and, through the address multiplexer, points to the starting of the appropriate micro routine.

The address decoder provides four address bits and the read/write line to the control instruction decoder. The control instruction decoder (as well as the refresh instruction decoder) provides the eight LSBs to the address multiplexer. The MSB is zero so that all I/O and refresh instructions start in the lower 256 locations of the control ROM. An absolute branch to the upper half allows the entire ROM to be used for instruction microprogramming.

The display processor reading a graphic register causes a return to the stop address when the read is completed. If a function command continues or a write display program counter is performed, the graphic controller resumes executing refresh instructions. (NOTE: The graphic registers are all contained in the micro-controller which provides the read register data.)

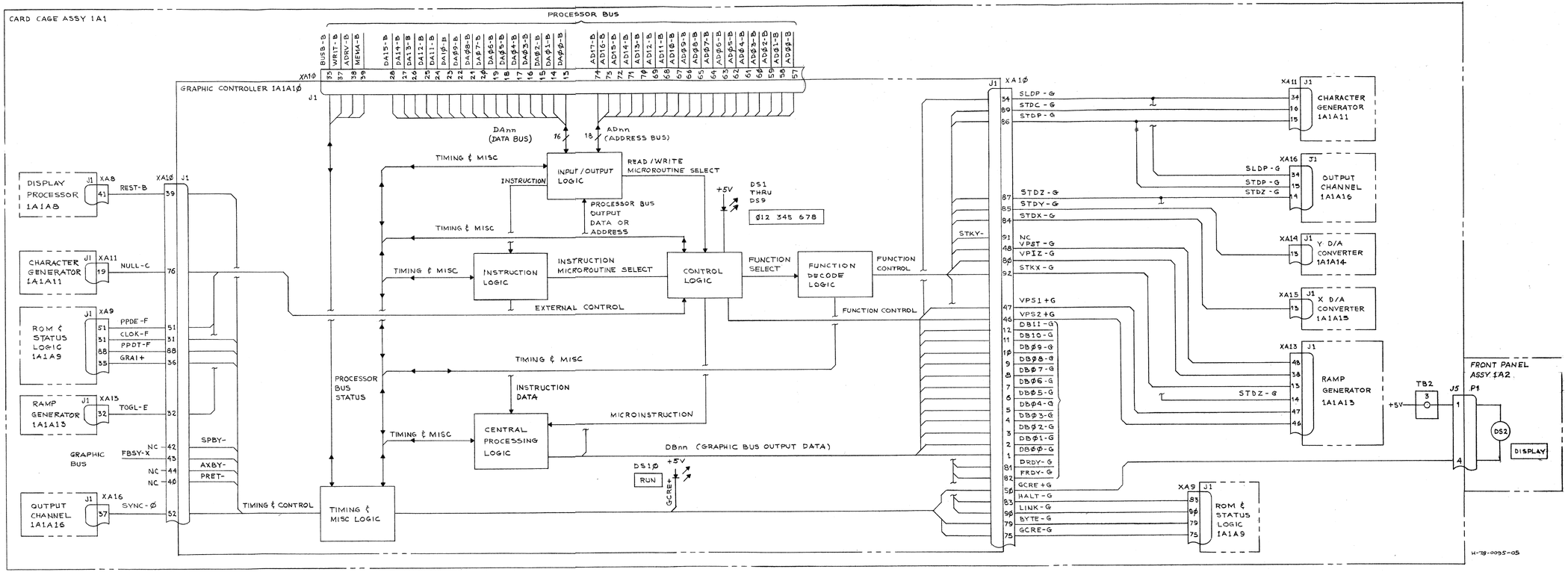
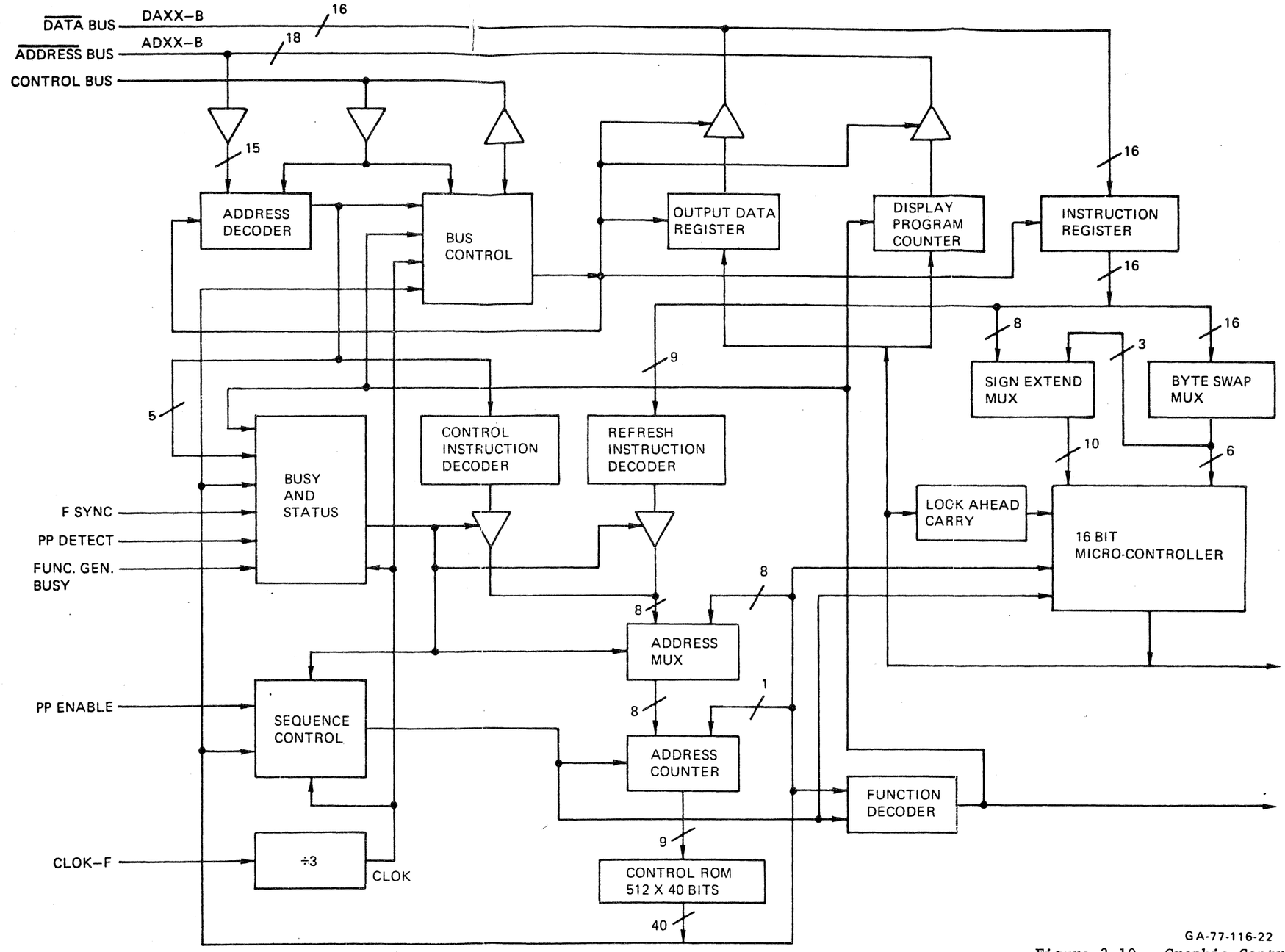


Figure 3-18. Graphic Controller Block Diagram



GA-77-116-22

Figure 3-19. Graphic Controller Functional Block Diagram

3.10 CHARACTER GENERATOR

The character generator (figure 3-21) controls the production of alphanumeric text characters and other symbols on the display indicator screen. The process involves two separate stages for each character: in stage one, the graphic controller sets up the ramp generator and the two D/A converters so that the output channel moves the blanked CRT beam to the desired character position. In stage two, the character generator is set up to convert an ASCII or EBCDIC character code into X-, Y-, and Z-axis analog outputs in accordance with the character size, orientation, and speed specifications from the most recent LDDP instruction.

The three analog outputs comprise sequences of very short stroke vectors that describe the form of the desired character. The number of vectors can range from zero (the space character) to 22 (the @ character). Two analog outputs (CHAX-C and CHAY-C) represent the X- and Y-axis deflection information that defines the stroke vector. The third output (CHAZ+C) represents the Z-axis intensity signal, containing unblank information for each stroke vector.

3.10.1 MAJOR CIRCUITS.

Display Character Register. This circuit is an 8-bit storage register that accepts and stores ASCII or EBCDIC character code data (bits DB00-G through DB07-G) when clocked by an active STDC-G (set display character register) signal from the graphic controller.

ROM Address Selection Logic. This circuit consists of three logic elements:

1. The mode control detects shift-in and shift-out codes to select either the normal character set or special symbols.

2. The column decoder selects ASCII or EBCDIC character columns in the ROM character table.

3. The up/down counter sequences through the ROM character table.

ROM Character Table. This circuit comprises a group of ROMs that store displacement data (direction, length, and repeat) and blank/unblank data for each stroke of specific display characters. The information is stored in the form of 8-bit word sequences. The character table is so arranged that successive pairs of character codes are defined by successive memory sections.

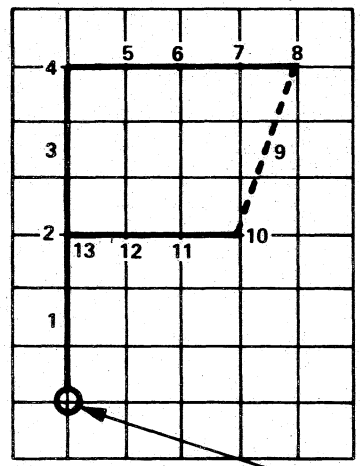
Each memory section contains up to 32 8-bit words (see figure 3-20). The normal character table circuit produces 96 characters in 48 memory sections. Six pairs of 256 word by 4-bit ROMs cover the standard ASCII character set.

In each character code, only as many 8-bit words are used as are needed to produce the given character. Unused word spaces are left blank. The last 8-bit word in each character code is an end-of-character signal that deactivates the character busy control circuit and resets the character generator circuits.

STROKE #	1 2	3 4	5 6	7 8	9 10	11 12	13											17	16	15	14	12 13	11	10	9	8	6 7	5	3 4	1 2	STROKE #
WORD #	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	WORD #
X0	0	0	1	1	0	0	0	1											1	1	1	1	1	0	0	0	0	0	0	0	1	1	X0 (SIGN)*
X1	0	0	1	1	0	1	1	0											0	0	1	1	0	0	0	1	1	1	0	0	1	1	X1 (FULL)
X2	0	0	0	0	1	0	0	0											0	1	1	0	1	0	1	0	0	0	0	1	0	0	X2 (HALF)
Y0	1	1	0	0	0	0	0	0											0	0	0	1	1	1	1	1	0	0	0	0	0	1	Y0 (SIGN)*
Y1	1	1	0	0	1	0	0	0											0	1	0	0	1	1	1	0	0	1	1	0	0	1	Y1 (FULL)
Y2	1	1	0	0	1	0	0	0											0	0	0	1	1	0	1	1	0	0	0	0	0	1	Y2 (HALF)
UNBLANK	1	1	1	1	0	1	1	0											0	1	1	1	1	1	1	1	1	1	1	0	1	0	UNBLANK
SKIP	1	1	1	1	1	1	0	0											0	0	0	0	0	1	0	0	0	0	1	0	1	1	SKIP

HORIZ. (X0 (SIGN)*, X1 (FULL), X2 (HALF))

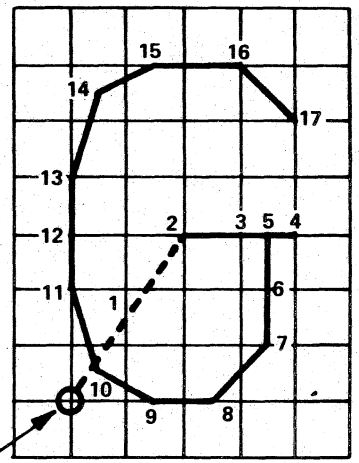
VERT. (Y0 (SIGN)*, Y1 (FULL), Y2 (HALF))



*SIGN SIGNIFICANCE:

X0 = 1 = RIGHT
= 0 = LEFT OR ZERO

Y0 = 1 = UP
= 0 = DOWN OR ZERO



INITIAL BEAM POSITION

H-78-0095-110

Figure 3-20. Character Generators for Typical Character Table

As an option, the character generator card may contain up to 32 additional special symbols. When installed, these symbols are contained in additional ROMs (two additional ROMs for up to 16 symbols, four additional ROMs for up to 32 symbols). When installed, these symbols are invoked by the SHIFT signal.

Extended character sets (up to 96 special symbols) may be had by substituting 512 word by 4-bit ROMs for the standard devices. The maximum capacity of the character generator is 192 characters (96 standard characters and 96 special symbols).

Buffer Register. This circuit is a 9-bit register that converts the position output code from the ROM character table into control bits for the analog X- and Y-axis drive generators. This register, driven by CLK2, also latches the blank/unblank commands from the ROM character table and generates the CHAZ+C signal that goes to the output channel card.

X-MUX and Y-MUX. This circuit controls the character orientation. Normally the character appears right-reading; the XP (X positive) signals drive the X D/A converter and the YP signals drive the Y D/A converter. When the ROTA signal is active, however, the character appears rotated 90° counterclockwise. The XN (X negative) signals drive the Y D/A converter and the YN signals drive the X D/A converter.

D/A Converters and Drive Amplifiers. These circuits respond to signals from the X and Y multiplexers and produce the X- and Y-axis drive outputs (CHAX-C and CHAY-C) that go to the output channel card.

Character Busy Control. This circuit determines when a display character is being generated and keeps the function busy signal active until the character has been completed.

Display Parameter Register. This 4-bit storage register accepts and stores display parameter information as defined by the last LDDP instruction. This register stores character size data (bits DB00-G and DB01-G) and a rotate selection (bit DB02-G) when bit DB03-G (change enable) gates an STDP-G (set display parameters register) signal from the graphic controller. The register stores the speed selection bits (DB09-G) when bit DB10-G (change enable) gates an STDP-G signal from the graphic controller.

When so directed by an SLDP-G signal from the graphic controller, this register reads out its currently stored values back onto the graphic data bus. Bits DB00-G, DB01-G, DB02-G, and DB09-G are read back as stored; DB03-G and DB10-G are read back as logic highs.

Size Decoder. This circuit converts the size data code stored in the display parameter register into clock divider signals that go to the stroke timing logic.

Character Generator Master Clock. This circuit consists of a 13.35 MHz oscillator (period of 75 nanoseconds) and a divide-by-16 circuit. The circuit is enabled by the function busy signal. If the slow speed command (display parameter bit 09) is inactive, the CLK1 pulse occurs every 75 nanoseconds. If the slow speed command is active, the CLK1 pulse occurs every 1200 nanoseconds.

Stroke Timing Logic. This timing circuit converts the CLK1 pulse train into a CLK2 pulse train as a function of character size and the SKIP- command from the ROM character table. The CLK2 pulse train determines the rate at which the address logic sequences the ROM character table from one stroke command to the next.

For larger character sizes, the stroke timing logic makes the CLK2 period longer, letting the CRT beam move further before the next stroke occurs.

When the character table includes an active SKIP- signal, the stroke timing logic suppresses the next CLK2 output pulse, thereby doubling the CRT beam movement for the selected stroke.

3.10.2 OPERATION. Operation of the character generator starts when the graphic controller loads the display parameter and display character data. The character generator responds to those inputs and produces the required X-, Y-, and Z-axis drive signals to make the output channel trace the desired character on the CRT screen.

Loading the Display Parameter Data. In response to a LOOP refresh instruction, the graphic controller sends a control word to the character generator. The bits of the control word set up the display parameter register (in conjunction with the STDP-G clock signal). Once set, these parameters remain in effect until the graphic controller sends another setup word. Table 3-27 describes the bits in the setup word.

The speed command switches the divide-by-16 counter into or out of the stroke timing logic circuit. The size code causes the stroke timing logic to modify the CLK2 clock train that addresses the ROM character table. The rotation command causes the X- and Y-axis drive generators to interchange functions, translating X-axis strokes into Y-axis drive signals, and Y-axis strokes into X-axis drive signals.

Character Generation. The graphic controller, in response to a TEXT or CHAR refresh command, places the code for the desired character (either ASCII or EBCDIC) on the graphic data bus, then sends a low STDC-G pulse to clock the data bits into the display character register.

The STDC-G pulse also activates the character busy control circuit, setting the FBSY-X (function busy) signal low to enable the CLK1 oscillator. The first CLK1 pulse causes CHEN+ (character enable) to go high, which enables the character busy control circuit and the up/down counter. The function busy signal also disables a reset function from the master clock circuit, thus turning on the X- and Y-axis drive generators, buffer register, and address select logic.

If the character code from the graphic controller defines a control character (including the SHIFT IN and SHIFT OUT commands that precede special or standard character strings), the register circuit produces a NULL-C output. The NULL-C output terminates the function busy signal, returning all character generator circuits to their initial conditions (except that the display parameters register remains loaded). Further, the NULL-C signal prevents the graphic controller from directing the ramp generator to increment the CRT beam to the next character location.

Table 3-27. Display Parameter Setup Data Codes

DB03-G	DB02-G	DB01-G	DB00-G	ORIENTATION/SIZE SELECTION
H	X	X	X	No effect (STDP-G is suppressed).
L	H	X	X	Normal horizontal orientation, reading left to right across display.
L	L	X	X	90° counterclockwise rotation, reading bottom to top.
L	X	H	H	X1 character size (smallest) (1/3 the adusted size).
L	X	H	L	X1.5 character size (1/2 the adjusted size).
L	X	L	H	X2 character size (2/3 the adjusted size).
L	X	L	L	X3 character size (the adjusted size).
	DB10-G	DB09-G		WRITING SPEED SELECTION
	H	X		No effect (STDP-G is ignored).
	L	H		Normal text-writing speed (one stroke every 150 nanoseconds, plus any size delay).
	L	L		Slow text-writing speed (one stroke every 2.4 microseconds, plus any size delay).

If the character code from the graphic controller defines any other character (alphanumeric, punctuation mark, or special symbol), the CHEN+ output from the master clock circuit lets the stroke timing logic count CLK1 pulses to produce the CLK2 pulse train as follows:

1. For an X1.0 size selection, every second CLK1 pulse (150 nanosecond period).

2. For an X1.5 size, every third CLK1 pulse (225 nanosecond period).

3. For an X2.0 size, every fourth CLK1 pulse (300 nanosecond period).

4. For an X3.0 size, every sixth CLK1 pulse (450 nanosecond period).

The resulting CLK2 pulse train then clocks the up/down counter and the buffer register, produces the stroke sequences for the character. If a specific word in the ROM character table includes an active SKIP bit, the SKIP- line goes low to the stroke timing logic. Each time the SKIP- line goes low, the stroke timing logic skips one CLK2 pulse (effectively doubling the period of the preceding CLK2 pulse and doubling the length of the vector).

Development of Analog Drive Signals. The control word from the buffer register turns on or turns off up to four current limiter switches in each drive generator circuit, thus controlling:

1. How much current is available to charge or discharge a common integrating capacitor.

2. How fast the integrating capacitor charges or discharges.

Each of four current limiter switches in each drive generator corresponds to a specific polarity (positive or negative) and rate (full or half) of charge, which corresponds to the direction and length of each vector. The two length values can be added, providing three displacement lengths in the selected direction: half unit, full unit, or 1-1/2 units, where "unit" is a relative measure defined by the relationship between the adjusted output voltage and the charge time.

The resultant change in charge/discharge output voltage through the CLK2 internal represents a CRT beam direction command for the associated display axis. The duration of the command is doubled when SKIP- is low. The collection of such vector commands, in combination with the blank/unblank commands, causes the output channel card to trace the character on the CRT screen.

Figure 3-20 shows both the 32 by 8-bit matrix stored in the ROM character table for the letter-pair F-G, and the resulting construction of those two letters. Note that the up/down counter counts up for the F character (whose ASCII code ends in logic 0), and counts down for the letter G (whose ASCII code ends in logic 1).

The letter F is defined in 13 strokes, as follows:

1. Strokes 1 through 4 draw the vertical leg.

2. Strokes 5 through 8 draw the top horizontal.

3. Strokes 9 and 10 are blanked move to the start of the lower horizontal.

4. Strokes 11 through 13 draw the lower horizontal.

The letter G is defined in 17 strokes, as follows:

1. Strokes 1 and 2 are a blanked move to the center of the character area.

2. Strokes 3 and 4 draw the horizontal crossbar.

3. Stroke 5 is a blanked move.

4. Strokes 6 through 17 are vectors at various angles to complete the letter.

All characters are drawn from an initial point at the lower left-hand corner of the character area. The beam is brought to this point by the last move instruction processed by the ramp generator card.

Note also that the last word of each character code in the ROM character table is 10000000_2. This word is the end-of-character signal.

End-of-Character Sequence. When the end-of-character signal appears, the following events occur:

1. The function busy condition becomes inactive.

2. The CHEN+ signal goes low.

3. The master clock circuit generates a reset signal. The reset signal clears the address select logic, buffer register, and both drive generators. The CRT beam moves (blanked) to its initial position for that character.

4. If additional characters are to be produced, the graphic controller directs the ramp generator to move the CRT beam to the initial position for the next character, (spacing determined by the LDTI refresh command) then loads the character code for the next character into the display character register and sends a low STDC-G clocking signal. If any display parameter is to change, the graphic controller makes the parameter change assignment before loading the display character register.

Stroke Time. Table 3-28 gives stroke times in nanoseconds for different character sizes.

Table 3-28. Stroke Times Vs. Character Size

RELATIVE CHARACTER SIZE	HEIGHT (INCHES)	STROKE TIME (NS)
1.0	0.125	150
1.5	0.1875	225
2.0	0.25	300
3.0	0.375	450

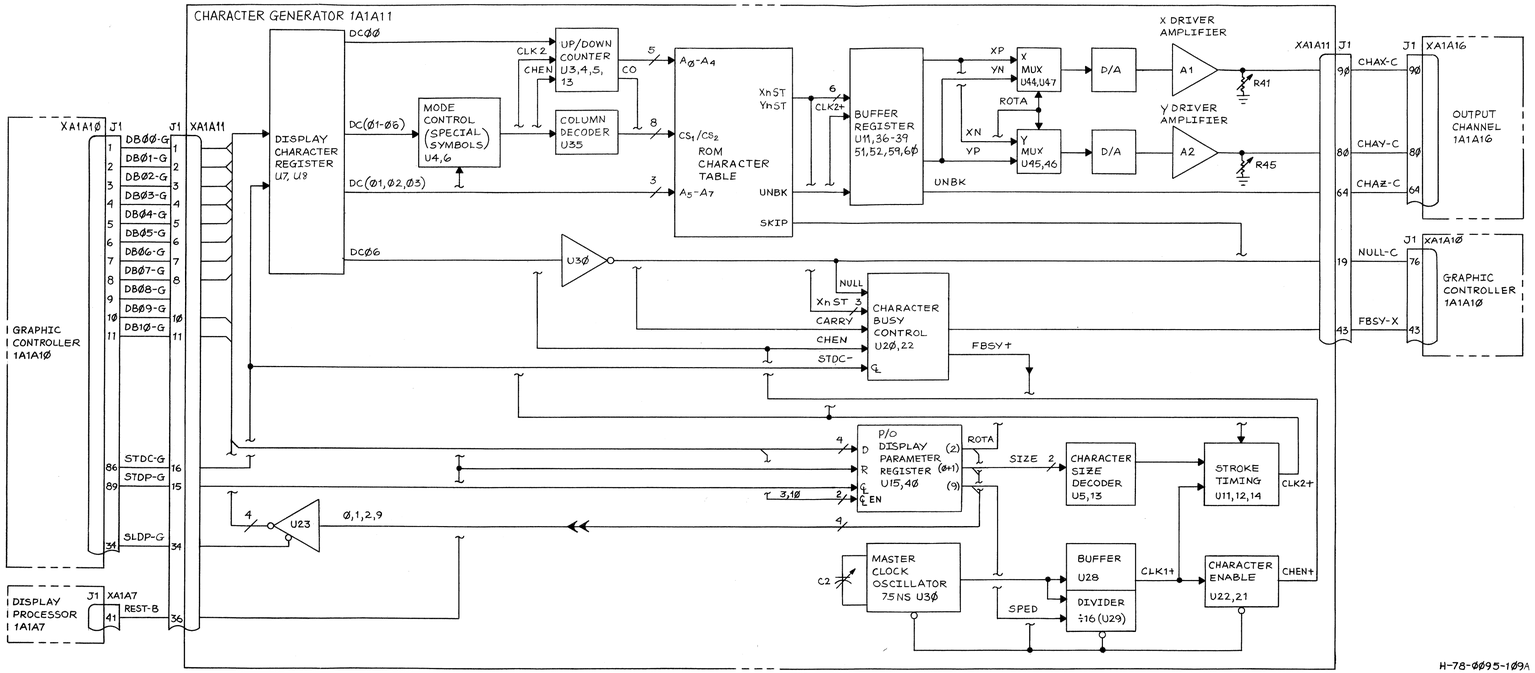


Figure 3-21. Character Generator Card, Block Diagram

3.11 RAMP GENERATOR

NOTE

If your system contains a ramp/conic generator, skip this paragraph and refer instead to H-78-0060.

The ramp generator, in conjunction with the two D/A converters, forms the vector/position generator (figure 3-23). Together these three cards convert beam position instructions and line structure instructions from the graphic controller into analog signals that go to the output channel card to control CRT beam movement and unblanking.

In a typical move or draw operation, the following sequence occurs:

1. The graphic controller loads the ramp generator with LINE STRUCTURE and SPEED SELECT bits and DISPLAY FUNCTION commands.

2. The graphic controller loads the X D/A converter with the X-axis coordinate of the end position of the move or draw (NEW POSITION DATA and DISPLAY FUNCTION COMMANDS).

3. The graphic controller loads the Y D/A converter with the Y-axis coordinate of the end position of the move or draw (NEW POSITION DATA and DISPLAY FUNCTION COMMANDS).

4. The X and Y D/A converters calculate the differences between their old position values and the new position values and pass this information to the ramp generator (X-AXIS DISPLACEMENT DATA and Y-AXIS DISPLACEMENT DATA).

5. The ramp generator uses the information supplied by the X and Y D/A converters to calculate the proper time duration for its ramp output signals (RMPX+E, RMPY+E). These signals go to the X and Y D/A converters at the same time.

6. The X and Y D/A converters send X and Y axis analog drive signals (DACX-A, DACY-A) to the output channel. These drive signals are a function of the amount of displacement in each axis and the duration of the ramp. At the same time, the ramp generator is supplying Z-AXIS DRIVE signals to the output channel.

The overall result is a picture on the CRT screen that has the proper relative intensity, given the length of the draw and any special Z-axis instructions.

The resulting line patterns may extend to any addressable XY coordinate point, on the CRT screen. Length in each axis is independently programmable from zero to twice the width of the display screen. The CRT beam deflection follows a straight line path because the ramp signal is linear.

The ramp generator has two modes of operation, depending on the type of move or draw instruction being performed:

1. Constant velocity mode, used for vectors or moves greater than 1/32 full screen displacement. The ramp excursion time is proportional to the length of the vector or move. There are two constant velocity modes:

   a. Constant vector velocity of a nominal 3.3 microseconds per inch. Full screen vector draw for a 12-inch display is about 40 microseconds.

   b. Constant move velocity of a nominal 2.1 microseconds per inch. Full screen move for a 12-inch display is about 25 microseconds.

2. Constant time mode, used for vectors less than 1/32 full screen displacement. Ramp excursion time is fixed at 1.25 microseconds and the Z-axis drive signal is attenuated in proportion to vector length.

In addition, there is a slow speed function (16 times slower), controlled by the LDDP refresh command.

3.11.1 MAJOR CIRCUITS. See figure 3-24.

Vector Length Calculator. This circuit receives as input the LX signals from the X D/A converter and the LY signals from the Y D/A converter. The LX and LY signals represent the spatial distance in each coordinate between the present beam position and the position defined by the new data words from the graphic controller.

This circuit then calculates two values: $(Y + X/2)$ and $(X + Y/2)$ and selects the larger of the two values as the basis for generating its RV outputs.

The rationale for these calculations is as follows:

1. Each move or draw requires the beam to travel along the hypotenuse of a right triangle. The sides of the triangle corresponds to the ΔX and ΔY values of the move.

2. The approximation $R = L + S/2$ (L = long side, S = short side) differs from the exact solution $R = \sqrt{L^2 + S^2}$ by only a small amount. The effect is a difference in brightness on the screen; the average human eye cannot detect this small difference in brightness.

Mode Control Logic. This circuit decodes two mode select signals from the graphic controller to generate the proper enabling conditions for other ramp generator circuits. The mode control logic also monitors the overflow signals from the X and Y D/A converters, and the six most significant Y-axis position bits.

The outputs of the mode control logic reflect the following decisions:

1. Whether the ramp generation logic produces a vector draw ramp or a position move ramp (VROM is low for vector draw, high for position move, text, point plot, or character).

2. Whether the ramp is to be produced at fast speed or at normal speed.

3. Whether the function busy signal should go active.

4. Whether the Z-axis control logic circuit should be enabled.

Table 3-29 relates the mode control logic outputs to various input conditions.

Charge Rate Calculator Logic. This circuit receives as input the RV outputs of the vector length calculator and the VROM output of the mode control logic. The output of this circuit is a 12-bit command (I0- through I11-) that goes to the ramp generator to establish the value of charging current. The 12-bit commands are the outputs of sets of ROMs; selection and address of the appropriate ROM is a function of the RV and VROM inputs.

Toggle Flip-Flop. Flip-flop U17B is cleared by an initialization signal (VPIZ-G) from the graphic controller. Thereafter it changes state in response to vector position state signals from the graphic controller. The state of this flip-flop determines the polarity of the ramp timing signal developed by the ramp generator circuit.

Ramp Generator Logic. This circuit responds to each change of state of the toggle flip-flop. It generates a linear RAMP output signal that rises if the TOGGLE signal is high and falls if the TOGGLE signal is low. The limits of the RAMP signal are +5V and 0V; it always reaches its limits.

RAMP is a timing signal. Its duration depends on these factors:

1. The state of the $\overline{\text{FAST}}$ signal from the mode control logic. (The RAMP signal is short for blanked position moves and point plots, longer for vectors).

2. The state of the $\overline{\text{VROM}}$ signal from the mode control logic.

3. The length of the vector to be drawn.

Current Limiters. The current limiters hold the ramp limits to precisely +5V and 0V and keep the slope linear to within 20 millivolts.

The current limiters circuit also produces a 2-bit timing code (ACLP- and BCLP-) that goes to the Z-axis control logic and the operation timing logic. One or the other of these two signals goes low when the RAMP signal reaches either of its limits. Both signals are high while the RAMP signal is changing.

The reference voltage regulator produces a +5V output and a 0V output that serve as the reference for the ramp generator circuit and for the D/A converter cards.

Line Structure Control Logic. The line structure control logic decodes data bits DB03-G and DB04-G from the graphic controller to produce the proper line type during a vector draw. The line types are: solid, dotted, dashed, and centerline. Circuit output is enabled by a low BUSY signal from the operation timing logic. The circuit output is the UNBLANKING ENABLE signal that goes to the Z-axis control logic. Table 3-30 shows the line structures as a function of input instruction bits.

Table 3-29. Mode Control Logic Input/Output Relationships

MODE CONTROL LOGIC INPUT CONDITIONS											OUTPUT RESULTS		
PROGRAMMING INSTRUCTIONS	OFLW-A	VPS2+G	VPS1+G	LY10+					LY05	$\overline{\text{FAST}}$	LINE VECTOR UNBLANKING LOGIC	$\overline{\text{VROM}}$	FBSY-X
Any	Low	X	X	X	X	X	X	X	X	High	Inhibited	Low	Enabled
MVXA MVXR MVYA MVYR MVSR LDKX	High	Low	Low	X	X	X	X	X	X	High	Inhibited	High	Enabled
DRXA DRXR DRYA DRYR DRSR DRKY	High	Low	High	X	X	X	X	X	X	High	Enabled	Low	Enabled
TEXT	High	High	Low	X	X	X	X	X	X	Low	Inhibited	High	Enabled
PPLR CHAR	High	High	High	0	0	0	0	0	0	Low	Inhibited	High	Inhibited[1]
LDXA LDXR	High	High	High	0	0	0	0	0	0	Low	Inhibited	High	Inhibited[1]
LDDZ LDDP LDTI	High	High	High	Y	Y	Y	Y	Y	Y[2]	High	Inhibited	High	Enabled

[1] FBSY-X generation circuit is reenabled if program calls for slow-speed output.

[2] YYYYYY stands for any binary value other than zero.

Table 3-30. Line Structure Select Bits

DB04-G	DB03-G	RESULT (EFFECTIVE WITH ACTIVE STDZ-G PULSE)
L	L	Centerline pattern: Two bits low, separated by three high bits on one side and eleven high bits (accumulatively) on the other.
L	H	Dashed pattern: Three out of every four bits high.
H	L	Dotted pattern: One out of every four bits high.
H	H	Solid pattern: Serial output of register held steadily high.

Line Vector Speed Control Logic. This circuit decodes data bits DB09-G and DB10-G from the graphic controller to select the proper line structure speed. Normal speed is obtained by using the output of the oscillator directly; the slow speed needed to operate the hardcopy unit is obtained by dividing the oscillator output by 16. Table 3-31 shows the speeds as a function of input instruction bits.

Table 3-31. Line Vector Speed Select Bits

DB10-G	DB09-G	RESULT (EFFECTIVE WITH ACTIVE STDP-G PULSE)
L	H	Regular speed selection, matching line pattern requirements to vector length.
L	L	Slow speed selection (1/16th that of regular selection, with RAMP generation circuit slowed correspondingly).

Z-Axis Control Logic. This circuit produces the VECZ+E signal that controls the presence and intensity of the display vector. Inputs to this circuit include the VPS1+G and VPS2+G signals (which identify load, move, draw, text, or point plot activity) and the ACLP-, BCLP- signals from the current limiters circuit (which identify the interval during which the vector is to be drawn). When the vector is a short vector (less than 1/32 full screen), an output from the short vector intensity control circuit attenuates the VECZ+E signal to ensure a consistent display intensity. When the vector is to be any type other than a solid line, an input from the line structure control logic turns the VECZ+E output on and off as necessary to produce the requested line structure.

Short Vector Intensity Control. This circuit determines when a short vector is called for, and sends an appropriate correction signal (based on vector length) to the Z-axis control logic.

Operation Timing Logic. This circuit monitors the timing functions throughout the ramp generator card. While an operation is in process, this circuit sends an FBSY-X (function busy) signal to the graphic controller. At the end of the ramp operation, this circuit sends the VPNL+E signal to both the X and Y D/A converters. In the D/A converters, this signal clears out old data, to prepare them for a new set of instructions from the graphic controller.

Overflow Circuit. When either D/A converter is loaded with an instruction that calls for a vector draw to some point outside the programmable area of the display, that D/A converter generates an overflow signal (OVFW-A). The overflow circuit in the ramp generator card generates a clock signal (OVCK-E) while the RAMP signal is changing its level. This clock signal goes to the ROM and status card to clock the OVFW-A signal into the ROM and status card's program interrupt register.

3.11.2 OPERATION

3.11.2.1 Setup. The input signals that set up the ramp generator are the following:

1. Timing signals VPIZ-G, STDZ-G, and STDP-G from the graphic controller.

2. Data bits DB03-G, DB04-G, DB09-G, and DB10-G from the graphic controller.

3. LXnn+A and LYnn+A (11 bits each) from the D/A converters.

4. OFLW-A from the two D/A converters (a common input).

The following paragraphs describe the sequence in which these signals occur, and what happens thereafter.

1. Data Bits. The graphic controller loads the line structure data bits (DB03-G, DB04-G), and clocks them in with the STDZ-G signal. The line structure decoding network sets up the 16-bit shift register with the appropriate line type.

   The graphic controller then loads the speed information data bits (DB09-G, DB10-G), and clocks them in with the STDP-G signal. Speed flip-flop U6C primes the clock select gates and the FBSY gate.

   The ramp generator is now set up and prepared for operation.

2. LXnn+A and LYnn+A. The graphic controller loads the D/A converters before it loads the ramp generator; hence these signals are available to the ramp generator before anything else happens.

   Bits LY05+ through LY10+ go to the mode control logic. If these six bits are all low, the Y-axis deflection is less than 1/32 of the full screen, and the fast move condition may apply. If any of these bits is high, the Y-axis deflection is more than 1/32 of the full screen. If the subsequent instruction is a draw, the fast move condition does not apply. (If the subsequent instruction is a move, the fast move condition can apply.)

   All the LX and LY bits go to the vector length calculator, which produces its RV outputs. These RV outputs go to the charge rate calculator, which generates the ROM addresses for a position move or a vector draw. The RV outputs also go to the short vector intensity control.

3. OFLW-A. The OFLW-A signal arrives from the D/A converters at the same time as the LX and LY signals. OFLW-A goes to the mode control logic. If OFLW-A is low (or goes low later when the ramp is being produced), it inhibits generation of the ramp and blanks the beam.

4. VPIZ-G. The graphic controller sends this active low pulse to clear the toggle flip-flop.

3.11.2.2 Operation. The graphic controller then sends the VPS1+G, VPS2+G, and VPST-G signals.

VPS1+G and VPS2+G go to the mode select decoder, the Z-axis control logic, and the operation timing logic. VPST-G goes to the toggle flip-flop.

The mode select decoder generates the appropriate output signals for the type of operation being performed. The $\overline{\text{VROM}}$ signal selects the proper ROM (vector or position move); the ROM establishes the charge rate of the constant current generator. In the case of a short vector, $\overline{\text{VROM}}$ inverted enables the short vector intensity control circuit, which in turn affects the VECZ+E output of the Z-axis control logic.

The FBSY INHIBIT signal, if active, is gated with the output of the speed flip-flop and goes to the operation timing logic to prevent the FBSY-X signal.

The $\overline{\text{FAST}}$ signal, if active, causes the ramp generator to ignore the inputs from the ROMs and produce its ramp in the shortest possible time.

The DRAW signal, when active, goes to the Z-axis control logic where it contributes to generation of the LINE ENABLE signal.

When the VPST-G signal goes to the toggle flip-flop, that device changes state with the following results:

1. The constant current generator produces the RAMP signal, sloping either upward or downward (depending on the last state of the toggle flip-flop). The slope is determined by the outputs of the ROMs or by the FAST signal. See figure 3-22.

2. The operation timing logic produces a BUSY signal that turns on the line structure control logic.

3. The FBSY-X signal goes to the graphic controller.

4. The TOGL-E signal goes to the graphic controller and the two D/A converters.

The operation timing logic turns on the oscillator in the line vector speed control logic, which in turn clocks the 16-bit shift register in the line structure control logic. The output of the shift register (the UNBLANKING ENABLE signal) goes to gate U15C in the Z-axis control logic.

The RAMP signal (limited and buffered) goes to the D/A converters as RMPX+E and RMPY+E. At the same time the ramp generator card sends the reference voltages REFP+E and REFN-E to the D/A converters.

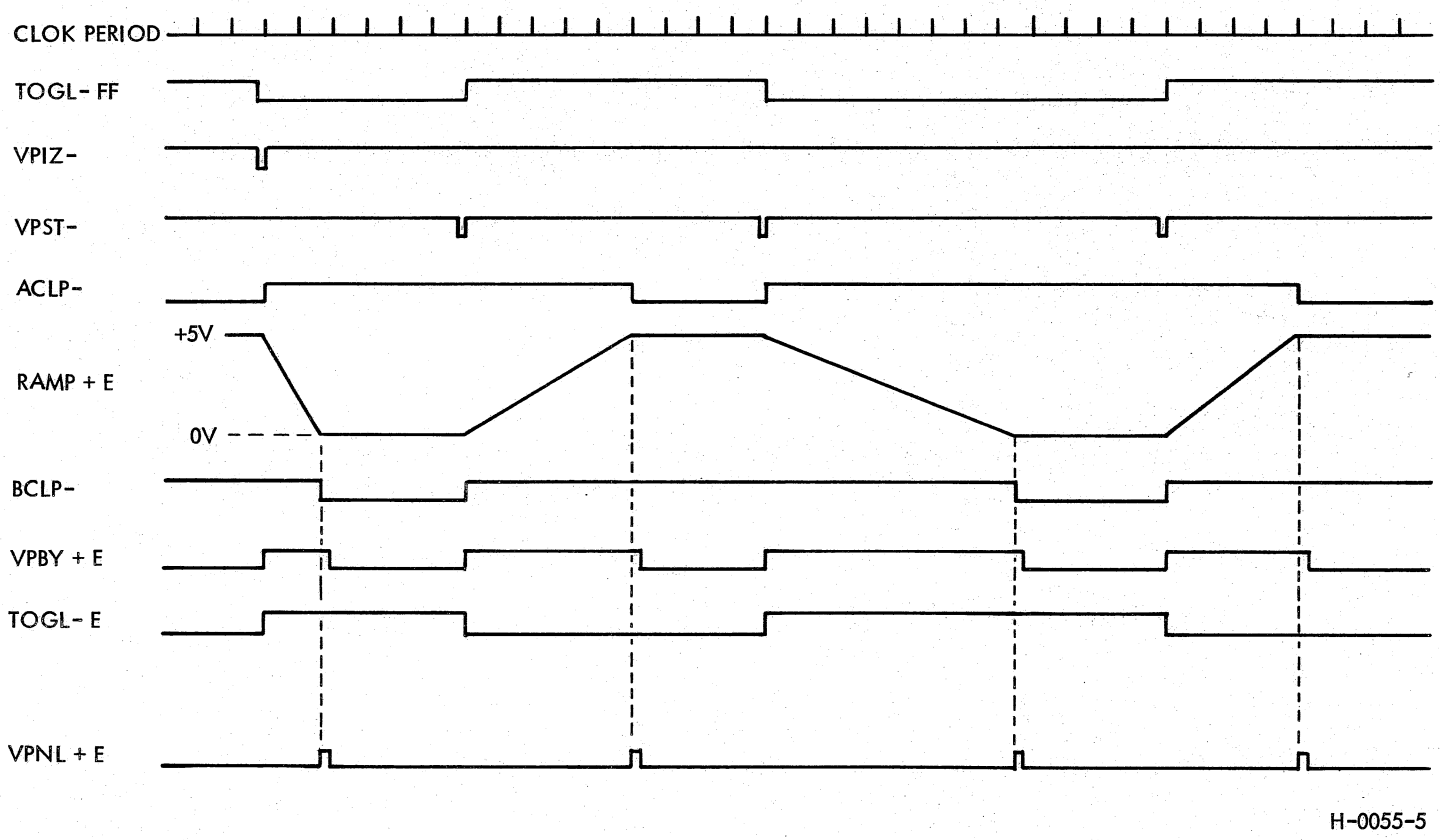


Figure 3-22. Ramp Generator Timing

Each time the RAMP signal reaches one of its limits, the ramp generator card sends the OVCK-E pulse to the ROM and status card. The high and low limit detectors also control the line vector unblanking logic, so that the VECZ+E signal (which goes to the output channel) carries the unblanking information (line structure or point plot). The 40 nanosecond delay line in the Z-axis control logic delays the application of the Z-axis information to compensate for delays in the ramp circuit, so that the Z-axis information arrives at the output channel card at the same time as the beam deflection information.

While the ramp is being generated, the signal VPBY+E (which goes to both D/A converters) is high; when the ramp is complete, VPBY+E goes low and the signal VPNL+E goes high.

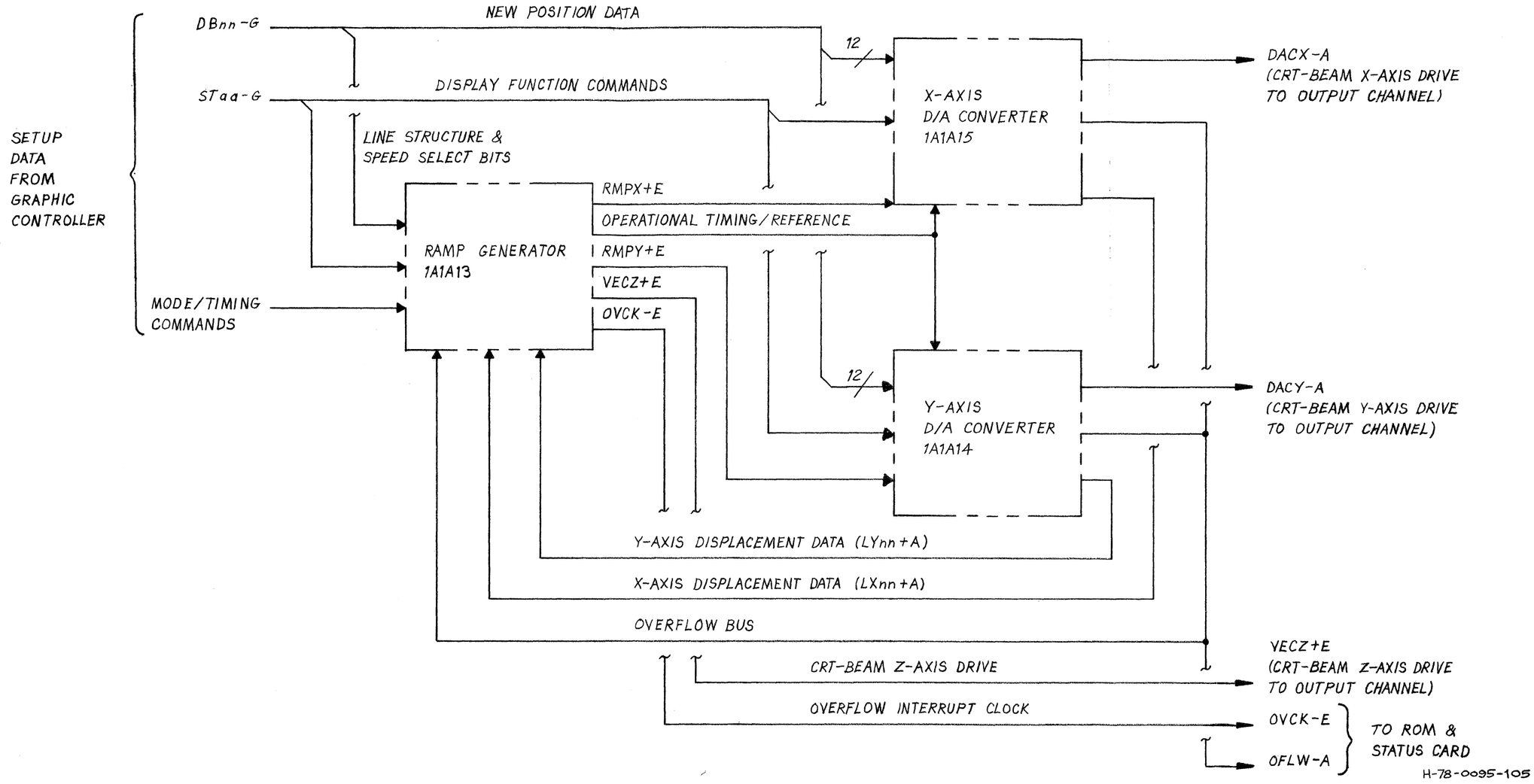


Figure 3-23. Vector/Position Generator, Block Diagram (Sheet 1 of 2)

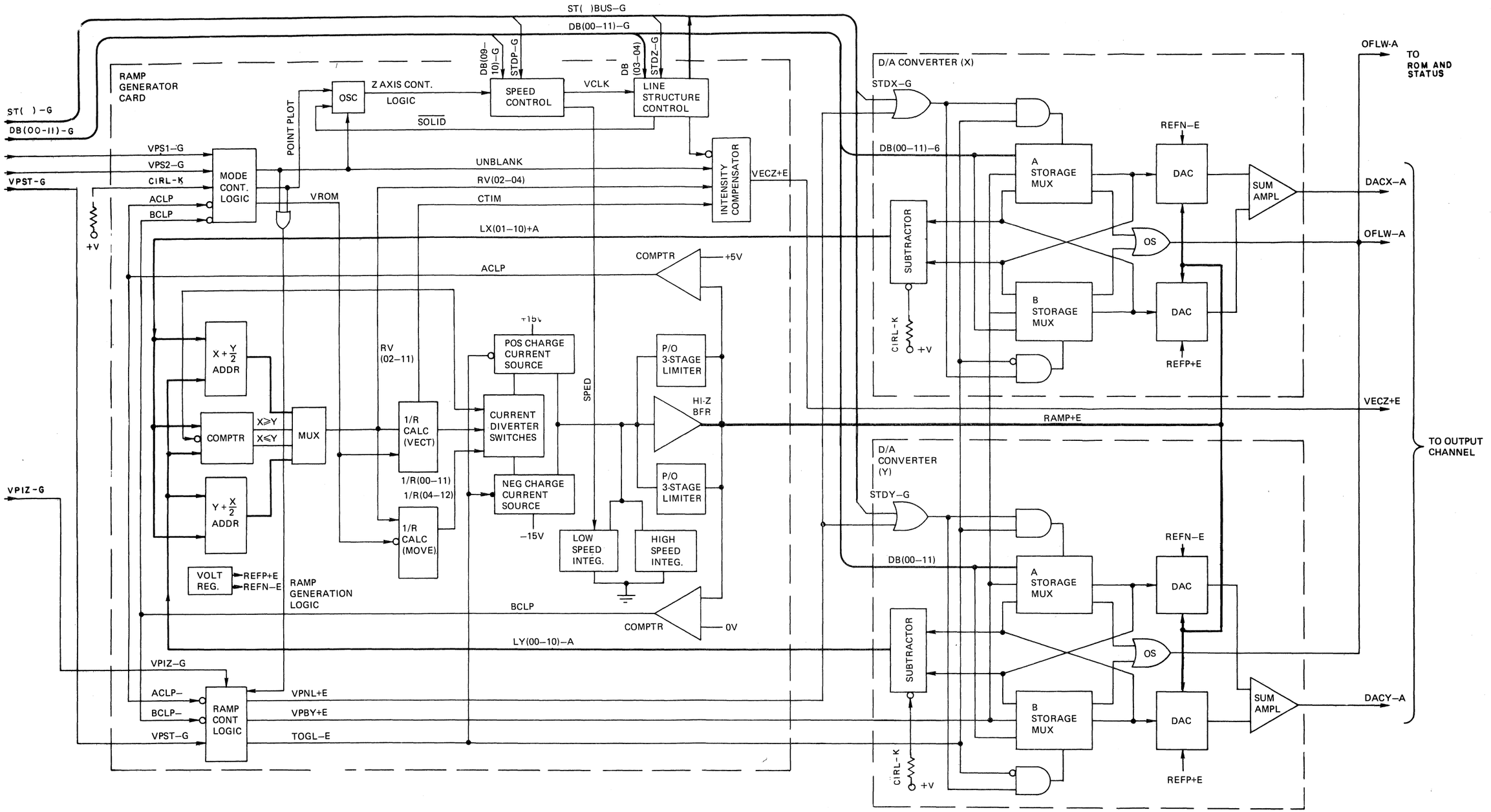


Figure 3-23. Vector/Position Generator, Block Diagram (Sheet 2 of 2)

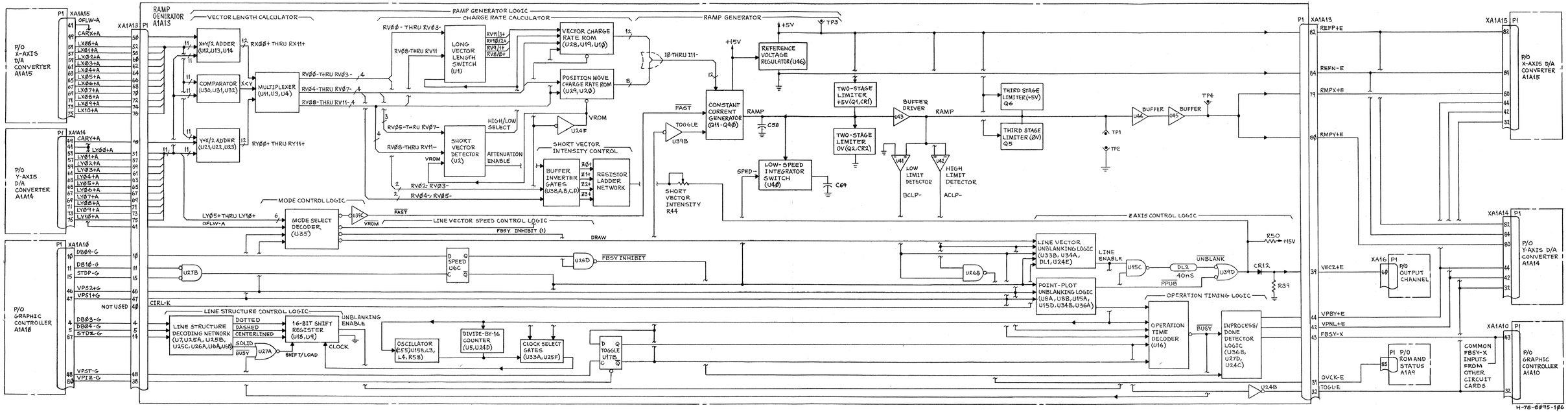


Figure 3-24. Ramp Generator Card, Block Diagram

3.12 D/A CONVERTERS

The terminal controller contains two identical D/A converters (figure 3-27). One controls X-axis deflection of the CRT beam; the other controls Y-axis deflection.

Overall operation of the D/A converter is as follows:

1. Initially the D/A converter has an old position coordinate stored in one of its two position registers.

2. The graphic controller sends new position data, which gets stored in the D/A converter's other position register.

3. The D/A converter subtracts the data in its B-position register from the data in its A-position register and sends the difference information to the ramp generator.

4. The ramp generator develops its RAMP signal on the basis of the information supplied by the two D/A converters and sends the RAMP signal back as RMPX+E, RMPY+E.

5. Each D/A converter generates its drive voltage (DACX-A or DACY-A) and sends this voltage to the output channel.

If the new position data from the graphic controller will drive the CRT beam beyond the programmable display area, the D/A converter generates an overflow signal that goes to the ROM and status card.

3.12.1 MAJOR CIRCUITS. Clock Generator. This decoding circuit reproduces either of two timing signals on either of two output lines, depending on the level of the TOGL-E input from the ramp generator, as follows:

TOGL-E high	A low-going STDX-G or STDY-G produces a low-going STAR- pulse	A high-going VPNL+E produces a low-going STBR- pulse.
TOGL-E low	A low-going STDX-G or STDY-G produces a low-going STBR- pulse	A high-going VPNL+E produces a low-going STAR- pulse

The STAR- and STBR- pulses are clocking inputs to the A-position and B-position registers.

A-Position Register. The A-position register is a 12-bit register that is clocked by the STAR- pulse. If VPBY+E is low, the register stores the DBnn-G control word from the graphic controller. If VPBY+E is high, the register stores the BRnn- data previously stored in the B-position register.

B-Position Register. The B-position register is a 12-bit register that is clocked by the STBR- pulse. If VPBY+E is low, the register stores the DBnn-G control word from the graphic controller. If VPBY+E is high, the register stores the ARnn- data previously stored in the A-position register.

Position Inverters. The A-position inverter inverts the ARnn- outputs from the A-position register into a 12-bit ARnn+ control word. The B-position inverter inverts the BRnn- outputs from the B-position register into a 12-bit BRnn+ control word.

Subtracter. The subtracter is a full-adder logic circuit. It subtracts the BRnn- word from the ARnn+ word, producing a 13-bit differential value (12 bits plus carry).

Carry Detector. This circuit produces the complement of the carry output from the subtracter. The CARX+A and CARY+A signals go to the ramp generator card. The carry detector logic also controls the true/complement multiplexer circuit.

True/Complement Multiplexer. This circuit accepts the 12 data bits produced by the subtracter. If the carry signal is high, it passes those bits unchanged. If the carry signal is low, the multiplexer inverts the 12 bits. Bits LX00+A through LX10+A (or LY00+A through LY10+A) go to the ramp generator with the associated carry signal as the LXnn+A or LYnn+A value of the vector component. The most significant bit (LX11+A, LY11+A) is not used.

A-Position D/A Converter. This D/A converter circuit produces an output voltage as a function of the ARnn control word when the RAMP+ input is more positive than the REFN-E ground reference input.

B-Position D/A Converter. This D/A converter circuit produces an output voltage as a function of the BRnn control word when the RAMP+ input is less positive than the REFP+E reference level input.

Summing Amplifier. This analog amplifier accepts outputs from the A-position and B-position D/A converters and produces an output (DACX-A or DACY-A) that represents the proportional difference between the two inputs.

3.12.2 OPERATION. The two D/A converters are set up by instructions and timing signals from the graphic controller. In a full set-up sequence, the graphic controller:

1. Loads the ramp generator with instruction data for the given vector: blanking/unblanking command, line structure information, speed selection. This information is contained in LDDP, LDDZ instructions.

2. Loads the X D/A converter with the X-coordinate value of the new position.

3. Loads the Y D/A converter with the Y-coordinate value of the new position.

4. Starts the ramp generator.

The ramp generator then produces its RAMP signal; as a result, the two D/A converters produce their drive signal outputs for the output channel card. At the same time the ramp generator is producing the Z-axis information for the output channel card.

If a new coordinate position is not different from the old position, the graphic controller does not load the new position into a D/A converter. If the vector is to be drawn truly horizontal or truly vertical, the graphic controller loads only one D/A converter. The data previously stored in the other D/A converter is still valid.

3.12.2.1 Set-Up A-Position Register. After initialization, the initial conditions of the ramp generator output are as follows:

1. RMPX+E (RMPY+E) is low (ground potential).

2. VPBY+E (vector position busy) is low.

3. VPNL+E (vector position null) is low.

4. TOGL-E (toggle) is high.

Under these conditions, the D/A converter can accept A-position register inputs from the graphic controller.

The following discussion describes what happens in the X-axis D/A converter. The same sequence is true for the Y-axis D/A converter, but the signal names are different.

The X D/A converter responds whenever the GCP+ instruction changes the X-axis deflection of the CRT beam. Such instructions include LDXA, LDXR, DRXA, DRXR, MVSR, DRSR, PPLR, or LDKX.

The low VPBY+E signal enables both position storage registers to receive new data inputs from the graphic data bus. The graphic controller places new X-position data (in two's complement form) on the DBnn-G lines and sets STDX-G (set X-position register) low. Because TOGL-E is high, the clock generator produces a low STAR- pulse that clocks the data into the A-position register. Data already in the B-position register remains unchanged.

3.12.2.2 Vector Length Calculation. The contents of the A-position is inverted and added to the contents of the B-position register. The result represents the difference between the old position value in the B-position register and the new position value in the A-position register. If the difference is positive, the subtracter carry output is high, and the differential output goes through the true/complement multiplexer unchanged. If the difference is negative, the subtracter carry is low, and the true/complement multiplexer inverts the subtracter output.

The carry detector also inverts the CARRY- signal, which becomes CARX+A. CARX+A is low if the multiplexer output is true data, high if the multiplexer output is complemented data.

The resulting 12-bit output word (CARX+A and LX00+A through LX10+A) represents the true difference in the X-axis distance between the old position in the B register and the new position in the A register. This output word goes to the ramp generator with a similar word from the Y D/A converter.

3.12.2.3 Beam Drive Signal Development. The RAMP signal from the ramp generator is applied to the X D/A converter as RMPX+E and to the Y D/A converter as RMPY+E. If your system contains the standard ramp generator, these signals are identical. Each D/A converter also receives the REFP+E and REFN-E reference voltages in common.

NOTE

If your system contains a ramp/conic generator card, the RMPX+E and RMPY+E signals are not always identical. They differ when the ramp conic generator is drawing curved lines.

The RAMP+ signal is applied to both D/A converter circuits. The A-position D/A converter is referenced to the ground level REFN-E input. This circuit receives as steering inputs both the ARnn- outputs from the A-position register and the ARnn+ outputs from the A-poistion inverters.

The B-position D/A converter is referenced to the positive REFP+E input. This circuit receives as steering inputs both the BRnn- outputs from the B-position register and the BRnn+ outputs from the B-position inverters.

After system initialization, the RAMP+ signal is at a logic low. This condition shuts off the A-position D/A converter (because RAMP+ = REFN-E). The low RAMP+ signal turns on the B-position D/A converter; the B-position D/A converter generates an output level controlled by the old position data.

Each D/A converter includes a ladder network with resistive steps that are switched in and out by the binary value of the word in the associated position register. In the post-initialization condition, the B-position control word is a random value established by power turn-on. This value activates the ladder paths that receive BRnn-/BRnn+ signals and deactivates those that do not. The resulting output represents an X-axis deflection of the CRT beam from the center of the display.

The outputs of the D/A converters pass through the summing amplifier, producing the DACX-A signal that goes to the output channel card. However, the CRT beam does not turn on during this post-initialization sequence because the ramp generator has not yet produced its axis drive signal VECZ+E.

3.12.2.4 Drive Output Signal on Up-Ramp. When the graphic controller sends a VPST-G (vector position start) signal to the ramp generator, the toggle flip-flop changes state and the RAMP signal starts to change. At the same time the TOGL-E input to the D/A converters and output channel cards goes low, and VPBY+E goes high.

As the RAMP+ signal becomes more positive, it turns on the A-position D/A converter and attenuates the output of the B-position D/A converter. Consequently, as the RAMP+ signal develops, the output of the A-position D/A converter rises until it reaches the value established by the ARnn signals, while the

output of the B-position D/A converter falls toward zero. These signals reach their limits when the RAMP+ signal reaches the REFP+E reference level.

The two D/A converter outputs change at different rates, as determined by the values stored in their position registers. The DACX-A output is therefore a changing value that moves the CRT beam during the ramp timing period from its initial position to the new position.

At the end of this change, the A-position D/A converter has complete control of the DACX-A output, and the B-position D/A converter is turned off by the high RMPX+E signal.

3.12.2.5 End-of-Ramp Update. When the RAMP+ signal reaches the REFP+E level, the ramp generator sends a high VPNL+E pulse to the D/A converter cards, keeping VPBY+E high until the VPNL+E pulse ends. This condition lets each position register accept as its input the output of the other position register. The next change-of-state of the TOGL-E signal produces a low STBR- pulse from the clock generator logic. STBR- clocks the output of the A-position register into the B-position register, leaving the content of the A-position register unchanged.

NOTE

The replacement of "old" B-position data by "new" A-position data occurs in both D/A converters at the same time, after the B-position D/A converter circuit is turned off. This arrangement simplifies the programming requirements for "on-axis" vectors, because the position does not now have to be respecified for the next operation unless it actually changes. If the next move or draw includes an on-axis displacement in either axis, the setup requires only one instruction, instead of two.

3.12.2.6 Set-Up B-Position Register. If the next move or draw instruction does require new X-axis setup data, the contents of the B-position register are replaced with the data for the latest instruction. The sequence begins as described in paragraph 3.12.2.1, with the graphic controller placing the data on the DBnn-G lines and activating the STDX-G timing pulse.

Because VPBY+E is low, both position registers are conditioned to accept new DBnn-G inputs. But as TOGL-E is still low, the clock generator responds to the STDX-G pulse by generating another STBR- pulse, which clocks the latest data into the B-position register. The contents of the A-position register now represents "old" data.

The subtracter logic now sends the ramp generator a new LXnn+A value, representing the difference between the start point in the A-position register and the end point in the B-position register.

3.12.2.7 Drive Output Signal on Down-Ramp. When the graphic controller turns on the ramp generator, TOGL-E goes high and the RAMP+ signal changes from its high level (equal to REFP+E) to a low level (equal to REFN-E). As the RAMP+ signal falls, it reduces the output of the A-position D/A converter and increases the output of the B-position D/A converter. Thus the DACX-A signal to the output channel changes during the RAMP+ period from the position value stored in the A-position register to the value stored in the B-position register. The CRT beam moves accordingly.

NOTE

If the program called for no change in X-axis, the graphic controller would not load any new X-position data. Both position registers would hold old position data. Then, during the RAMP+ period, the increasing B-position output would match the decreasing A-position output, and the DACX-A signal would remain constant at its appropriate value.

At the end of this second ramp sequence, the ramp generator produces a VPNL+E pulse while VPBY+E is still high. TOGL-E is now also high. Therefore the clock generator produces a STAR- pulse, which clocks the new end-point value from the B-position register into the A-position register, leaving the contents of the B-position register unchanged. The circuit is now ready for the next sequence.

Figure 3-25 shows the relative timing of the various signals that contribute to D/A converter operation.

Figure 3-26 shows a typical vector drawing sequence, including the blanked and unblanked maneuvers that might be required to generate a full-screen box pattern. The figure includes a list of GCP+ instructions (expressed in octal code) associated with each change in XY position, designating in each case the values that are to be loaded into the D/A converters.

3.12.2.8 Overflow Detector. The position registers receive a 12-bit DBnn-G word. Bits DB00-G through DB10-G represent the actual position data. Bit DB11-G is a sign bit.

The offscale overflow detector monitors the sign bit and MSB data values from each position register to determine if the corresponding position falls within the programmable area. For the 1023 programmable positions to the right of center (of which only 512 are displayable), both X-axis bits are low. The MSB data bit goes high when the X-axis displacement value goes outside the programmable area.

For the 1023 programmable positions to the left of center, both bits are high. The MSB data bit goes low when the X-axis displacement value goes outside the programmable area.

The Y-axis values operate in the same way.

The offscale overflow detector decodes these two possibilities for each of the two position registers. If an overflow occurs, the detector sends a low OFLW-A signal to the output channel, where it disables the Z-axis drive signal to blank the CRT beam.

The OFLW-A signal also goes to the ramp generator, where it:

1. blanks the VECZ+E Z-axis drive signal.

2. enables the function busy circuit.

The OFLW-A signal also goes to the ROM and status card, which sends a program interrupt to the GCP+, stating that the last loaded instruction drives the CRT beam to a point outside the displayable area.

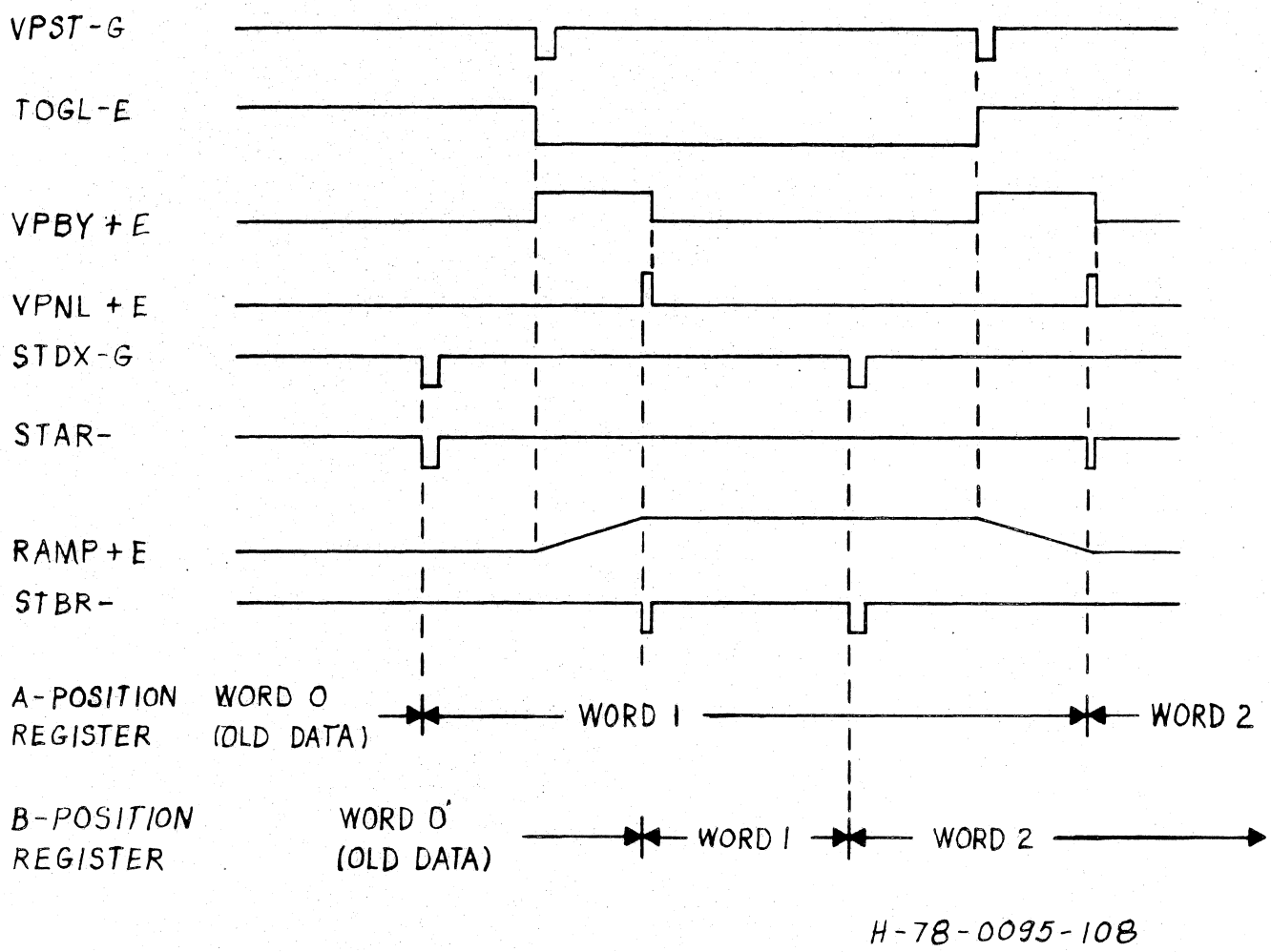


Figure 3-25. D/A Converter Timing Diagram

MOVE/ VECTOR SEQUENCE	PROGRAM INSTRUC- TION	LABEL	ASSEMBLY MNE- MONIC	COMMENT/MEANING
	013707	START	LDDZ <ALL,BLOFF,LINE,BR7>	
	016310		LDDP <FAST,F60,NOPP,NOROTATE,C50>	
	003000		IZPR	;INITIALIZE RAMP
	020000		LDXA,0	;RELOCATE DISPLAY BEAM
	060000		MVYA,0	; AT CENTER OF CRT SCREEN
	007000		WATE	;WAIT FOR FRAME SYNC
(1)	020777		LDXA +511	;LOAD +511 AS X-AXIS ADDRESS
	060777		MVYA +511	;LOAD +511 AS Y-AXIS ADDRESS, THEN MOVE BEAM
(2)	023000		LDXA -512	;LOAD -512 AS X-AXIS ADDRESS
	043000		DRYA -512	;LOAD -512 AS Y-AXIS ADDRESS, THEN DRAW VECTOR
(3)	050777		MVXA +511	;LOAD +511 AS X-AXIS ADDRESS, THEN MOVE BEAM
(4)	023000		LDXA -512	;LOAD -512 AS X-AXIS ADDRESS
	040777		DRYA +511	;LOAD +511 AS Y-AXIS ADDRESS, THEN DRAW VECTOR
(5)	050000		MVXA 0	;LOAD 0 AS X-AXIS ADDRESS, THEN MOVE BEAM
(6)	043000		DRYA -512	;LOAD -512 AS Y-AXIS ADDRESS, THEN DRAW VECTOR
(7)	020777		LDXA +511	;LOAD +511 AS X-AXIS ADDRESS
	060000		MVYA 0	;LOAD 0 AS Y-AXIS ADDRESS, THEN MOVE BEAM
(8)	033000		DRXA -512	;LOAD -512 AS X-AXIS ADDRESS, THEN DRAW VECTOR
(9)	063000		MVYA -512	;LOAD -512 AS Y-AXIS ADDRESS, THEN MOVE BEAM
(10)	030777		DRXA +511	;LOAD +511 AS X-AXIS ADDRESS, THEN DRAW VECTOR
(11)	040777		DRYA +511	;LOAD +511 AS Y-AXIS ADDRESS, THEN DRAW VECTOR
(12)	03300		DRXA -512	;LOAD -512 AS X-AXIS ADDRESS, THEN DRAW VECTOR
(13)	043000		DRYA -512	;LOAD -512 AS Y-AXIS ADDRESS, THEN DRAW VECTOR
(14)	023076		LDXA -450	;LOAD -450 AS X-AXIS ADDRESS
	063076		MVYA -450	;LOAD -450 AS Y-AXIS ADDRESS, THEN MOVE BEAM
(15)	045604		DRYR +900	;DRAW VECTOR 900 UNITS UP RELATIVE CURRENT POSITION
(16)	035604		DRXA +900	;DRAW VECTOR 900 UNITS TO RIGHT RELATIVE CURRENT POSITION
(17)	046174		DRYR -900	;DRAW VECTOR 900 UNITS DOWN RELATIVE CURRENT POSITION
(18)	036174		DRXR -900	;DRAW VECTOR 900 UNITS TO LEFT RELATIVE CURRENT POSITION
(19)	005704		JMPR START	;REPEAT SAME LOOP INDEFINITIELY

RESULTANT CRT PATTERN ON DISPLAY INDICATOR (FROM FRONT)

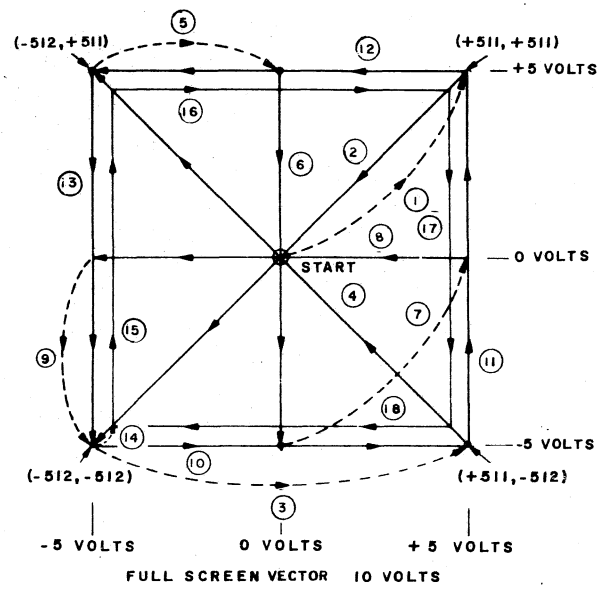


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Figure 3-26. Vector Position Generator Pattern Development

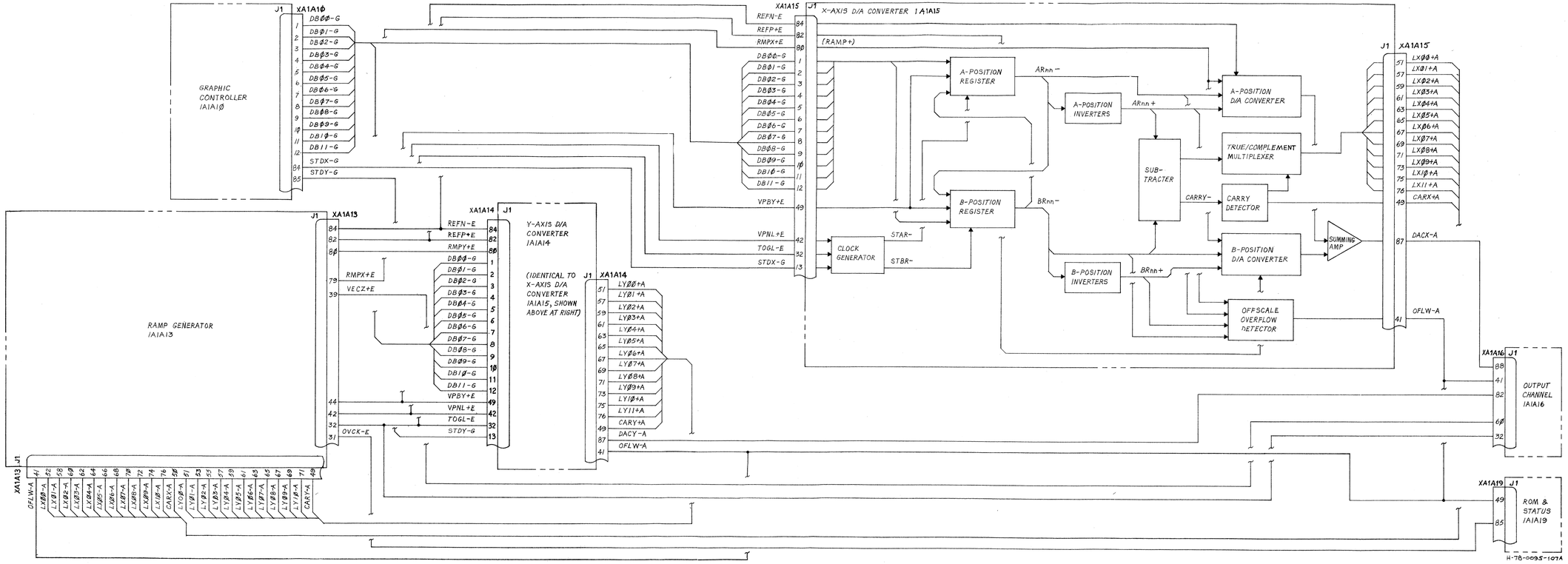


Figure 3-27. D/A Converter Card, Block Diagram

3.13 OUTPUT CHANNEL CARD

NOTE

This paragraph describes two output channel cards. Part number 1086771 is the standard output channel card, capable of driving up to four monochrome display indicators. Part number 5977409 is required for four-color display indicators; it is capable of driving up to four such display indicators. In the following discussions, those paragraphs that apply only to the output channel card for the four-color display indicators are indicated by the word (Color) at the beginning of the paragraph.

The output channel card develops the X, Y, and Z axis drive signals for up to four display indicators as functions of the drive signals developed by the vector position generator (the ramp generator and the two D/A converters) and the character generator. The output channel card processes these signals in such a way that the X and Y axis outputs go simultaneously to all the display indicators, but the Z axis signal is selectable for each display indicator. In this way each display indicator can present a different display.

The output channel also processes blink setup data for the Z axis signals, selects any one of eight levels of Z axis intensity, and automatically blanks the Z axis output if either the X or Y axis signal drives the beam outside the display area.

Other output channel functions include generating a power turn-on signal that lets the display processor initialize the terminal controller, developing a real-time clock signal for the ROM and status card, and producing a frame sync signal for the graphic controller. The output channel card also contains inhibit/enable circuits for a PHOTOPEN.

(Color) The output channel also recognizes color selection instructions and generates sequences of pulses, coded to select the colors to be displayed by each display indicator. The output channel card contains circuits that make the Z4 signal follow any of the other Z axis signals; this feature selects the data that goes to a hardcopy unit.

3.13.1 MAJOR CIRCUITS AND OPERATION. Refer to figures 3-28 and 3-29.

Program Registers. The standard output channel card contains two program registers that get loaded to establish the setup conditions for other circuits on the output channel card. The color output channel card contains three such registers.

When the graphic controller processes an LDDP instruction, certain bits on the DBnn-G graphic data bus get loaded into the output channel card's display parameter register. These bits enable separate channels in the PHOTOPEN support circuit and allow selection of a desired frame sync rate. (Other bits appearing on the DBnn-G graphic data bus at the same time go to the character generator.)

When the graphic controller processes an LDDZ instruction, certain bits on the DBnn-G graphic data bus get loaded into the output channel card's Z-axis

display register to enable blink mode, select the display intensity level, and determine which display indicator receives the Z-axis drive signal. (Other bits appearing on the DBnn-G graphic data bus at the same time go to the ramp generator line structure select logic.)

(Color) When the graphic controller processes an LDRI instruction that calls for a color selection, the eight color bits (DB00-G through DB07-G) and the four display select bits (DB08-G through DB11-G) get loaded into the output channel card's color select register and associated circuit.

XY Axis Analog Processing. The X and Y axis inputs from the respective D/A converters and the character generator are applied to summing amplifier circuits. (The summing networks have input connections for a third source of analog data; these growth-potential connections are not currently used.)

The amplifier outputs have sufficient power to drive up to four display indicators. Two sets of output connectors are provided to facilitate local and remote connections. Each summing amplifier circuit includes separate gain and offset controls for adjustment of full screen deflection and screen centering in both axes.

The output channel incudes an XY overdrive sensor common to both analog outputs. If either summing amplifier produces an excessive drive signal (one which drives the CRT beam outside the displayable area), this protection circuit produces an active blanking command for the Z-axis processing circuit.

Z-Axis Analog Processing. Z-axis inputs from the ramp generator and character generator are applied to a summing network. The resultant output is applied to a blanking/attenuation switching circuit controlled by the Z-axis display register and the blanking command from the XY overdrive sensor.

When an LDDZ instruction calls for a blinking function for any display vector or character string, the graphic controller drives DB05-G low and sends a low STDZ-G pulse that loads the blink command into the Z-axis display register. This condition enables a blink oscillator circuit that alternately enables and inhibits the Z-axis drive signal at a rate of approximately 4 Hz. The resultant output is applied to an intensity level selector circuit that is also controlled by the Z-axis display register. This selector circuit produces one of eight output levels, as determined by bits DB00-G, DB01-G, and DB02-G of the LDDZ instruction. When all three bits are high, the beam is at its lowest intensity; when all three bits are low, the beam is at its highest intensity.

The Z-axis drive signal is applied to a display select steering circuit, controlled by the Z-axis display register. This steering circuit consists of four enabling circuits, each of which receives the Z-axis drive signal. The Z-axis display register outputs enable one or more of these paths, as determined by bits DB06-G through DB10-G of the LDDZ instruction (bit DB10-G is the select enable bit). Consequently the Z-axis drive output from the blanking/attenuation switching circuit is distributed through this selection circuit only to the desired display indicators.

Frame Sync Generator. The frame sync generator includes a zero crossover detector and the associated sync selector circuit. The zero crossover detector develops two internal pulse trains. One train, RTCK-0 (real time clock), is a 60 Hz output to the ROM and status card that goes low momentarily every time the 60 Hz LINE+ signal switches from positive to negative (i.e., crosses the 0V line). The second 60 Hz pulse train also goes low momentarily every time the LINE+ signal switches from negative to positive. The two clock trains are then OR'ed to produce a 120 Hz pulse train, which goes low every time the LINE+ signal crosses the 0V line in either direction.

NOTE

When the power line is 50 Hz, the combined pulse train goes low 100 times per second.

The combined pulse train goes to a sync selector circuit that is controlled by a 2-bit code stored in the display parameter register. The 2-bit code sets up a programmable divider circuit that counts every second, third, or fourth clock pulse, thus selecting a 60 Hz, 40 Hz, or 30 Hz train as the SYNC-0 refresh rate output to the graphic controller (see table 3-32). (If the power line frequency is 50 Hz, the SYNC-0 rate is 50, 33.3, or 25 Hz.)

Table 3-32. Programmable Divider Bit Codes

DB08-G	DB09-G	RESULTING SELECTION
H	H	No change from previous selection
H	L	Every 2nd pulse
L	H	Every 3rd pulse
L	L	Every 4th pulse

The frame sync circuit can be disabled by applying a ground on the SL60+0 line.

Power Turn-On Sensor. This circuit consists of a single-shot that produces a low-going TORN-0 pulse following system power turn-on. TORN-0 goes to the display processor, and the display processor turns on the SYST-B (system reset) pulse. SYST-B then initializes all programmable circuits throughout the terminal controller.

TORN-0 can also be generated by applying a ground at the EXTR- input.

PHOTOPEN Support Circuit. This circuit supports two PHOTOPENS (optional): one associated with display indicators 1 and 2, the other associated with display indicators 3 and 4.

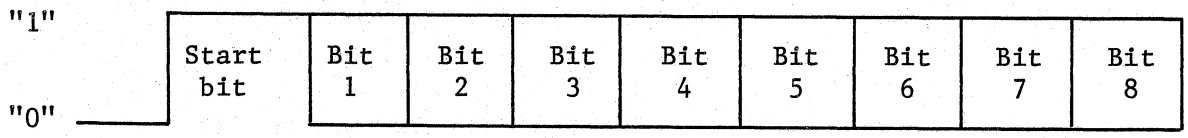
The PHOTOPEN support circuit stores the values of bits DB04-G (PHOTOPEN 1 enable) and DB05-G (PHOTOPEN 2 enable) of the LDDP (load display parameter register) instruction, provided that bit DB06-G (PHOTOPEN select change enable) is low. Bits DB04-G and DB05-G, when low, enable receipt of signals from the associated PHOTOPEN; when high, these bits inhibit such signals.

The enabling signals prime gates that also receive the outputs from the PHOTOPENS. Each such gate passes its PPLn- (PHOTOPEN light strike) signal from the driver circuit to an interrupt circuit on the ROM and status card as PPDn-0 (PHOTOPEN detect). The enabling signals are also applied as PENn+0 (PHOTOPEN strike enable) signals to the ROM and status card.

(This paragraph does not apply to the color card.) The PHOTOPEN support circuit also includes single-shots that are triggered by the PPLn- light strike signals. Triggering does not depend on the condition of the PHOTOPEN select enabling signal. When triggered, these single-shots send 250-nanosecond pulses to the display select steering logic to generate a maximum intensity Z-axis signal for the currently selected display indicator. One result is a bright spot on the display screen where the PHOTOPEN light strike occurs.

(This paragraph does not apply to the color card.) In those GRAPHIC 7 systems in which the strike illuminator function is contained in the PHOTOPEN intensifier/driver assembly mounted in the display indicator assembly, the single-shots should be disabled on the output channel card by removing jumper connections. See Section 4.

3.13.2 UNIQUE CIRCUITS OF COLOR OUTPUT CHANNEL CARD. Color Select. The color select circuit receives instruction data and sends a proper serial bit stream to the selected display indicator. The instruction data consists of eight color bits that get strobed into an 8-bit shift register, and four display select bits that get strobed into four display select flip-flops. The bits are shifted out of the shift register by a clock signal developed on the color output channel card; they go to the Z axis amplifier in the following form:



This arrangement lets the output channel select up to 256 colors. Each serial bit is 100 nanoseconds wide, and the whole transmission takes 900 nanoseconds. The shift register output is gated with the outputs of the display select flip-flops to enable or disable the input to the Z axis amplifiers.

For the four-color display, the instruction is set up to send:

1 pulse for red

2 pulses for orange

3 pulses for yellow

4 pulses for green

Each pulse is 100 nanoseconds long. Spacing between pulses is 100 nanoseconds.

At the start of execution, the output channel card's function busy signal FSBY-X goes low for approximately 250 microseconds to let the display indicators change color.

At turn on, one pulse is sent to each display indicator to initialize to the color red.

The color instruction has the following form:

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Word 1	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	Octal 6010
Word 2	X	X	X	X	Disp. select				Color select								

Display Select

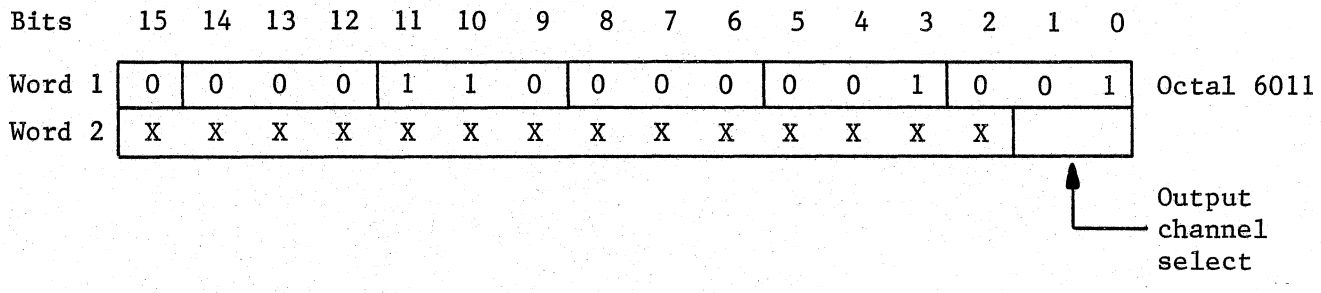
Bit 11	Change color for display #1
Bit 10	Change color for display #2
Bit 9	Change color for display #3
Bit 8	Change color for display #4

Color Select

Bits	7	6	5	4	3	2	1	0	Color
	0	0	0	0	0	0	0	0	Red
	0	0	0	0	0	0	1	0	Orange
	0	0	0	0	1	0	1	0	Yellow
	0	0	1	0	1	0	1	0	Green

Output Channel Select. When a terminal controller contains two output channel cards, this circuit is used to select or deselect one card. Both cards are selected at turn-on and remain selected until the proper instruction deselects one of them. When the terminal controller contains only one output channel card, the program need not select the output channel; it is selected at turn-on.

The circuit selects or deselects the output channel card by enabling or disabling the control lines (STDZ, SLDP, STDP, etc.) as they enter the card. The instruction has the following form:



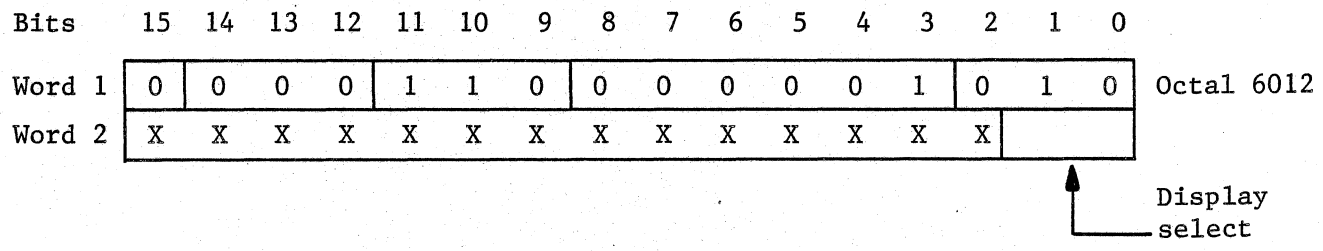
Output Channel Select

Bit 0	Select output channel 1
Bit 1	Select output channel 2

Hardcopy Display Select. This circuit lets the program select (by an LDRI instruction) the display to be reproduced by the hardcopy unit. The hardcopy unit, when used, connects to these connectors identified as channel 4 (i.e., the hardcopy unit replaces display indicator #4).

At turn-on, the circuit is set up so channel 4, to which the hardcopy is connected, copies itself. If a presentation is addressed to channel 4 (i.e., a previous LDDZ instruction selected display indicator #4), no additional instructions are required except an initiate hardcopy command.

To make the hardcopy unit copy one of the other three channels, the graphic controller sends an LDRI instruction having the following form:



Display Select

Bits 1	0	Display to be Copied
0	0	1
0	1	2
1	0	3
1	1	4

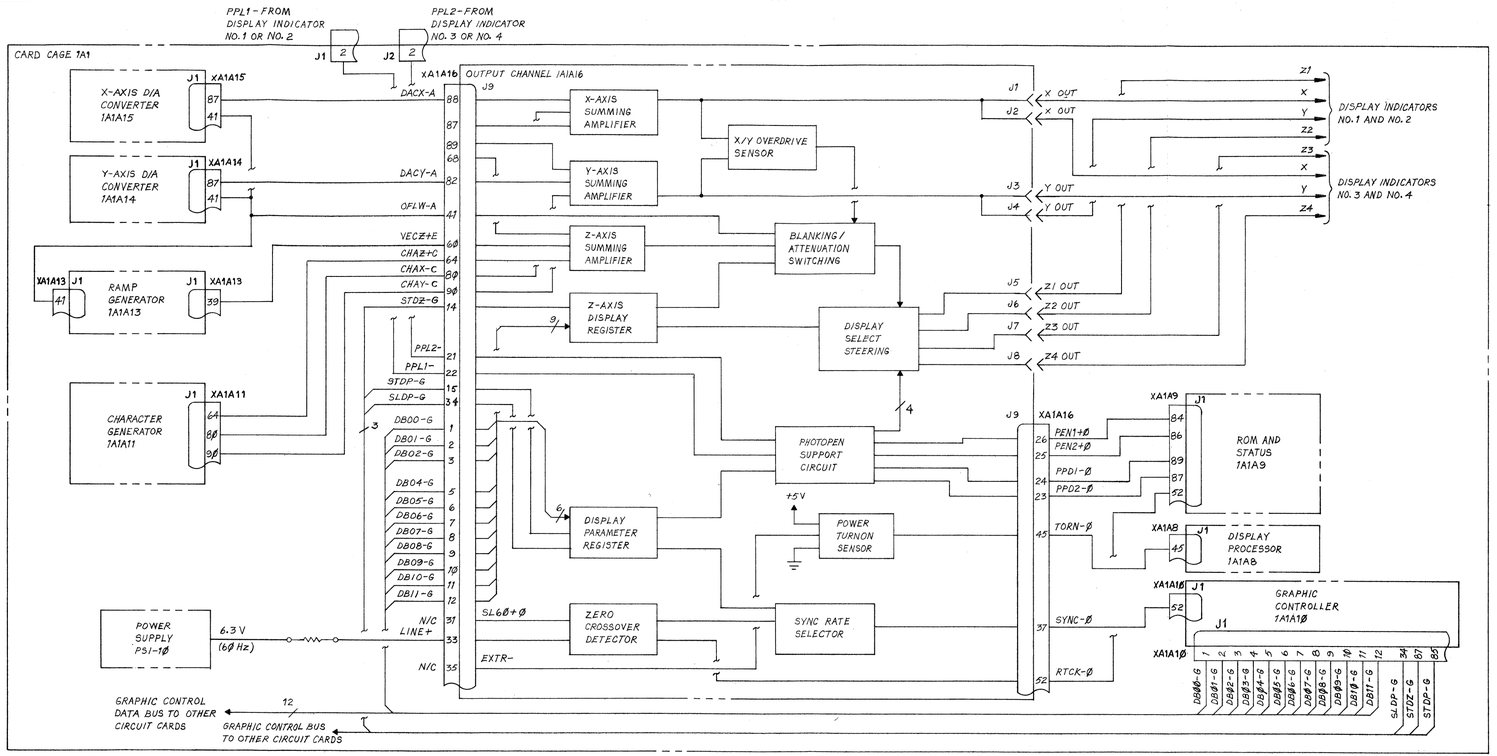


Figure 3-28. Output Channel Card P/N 1086771 Block Diagram

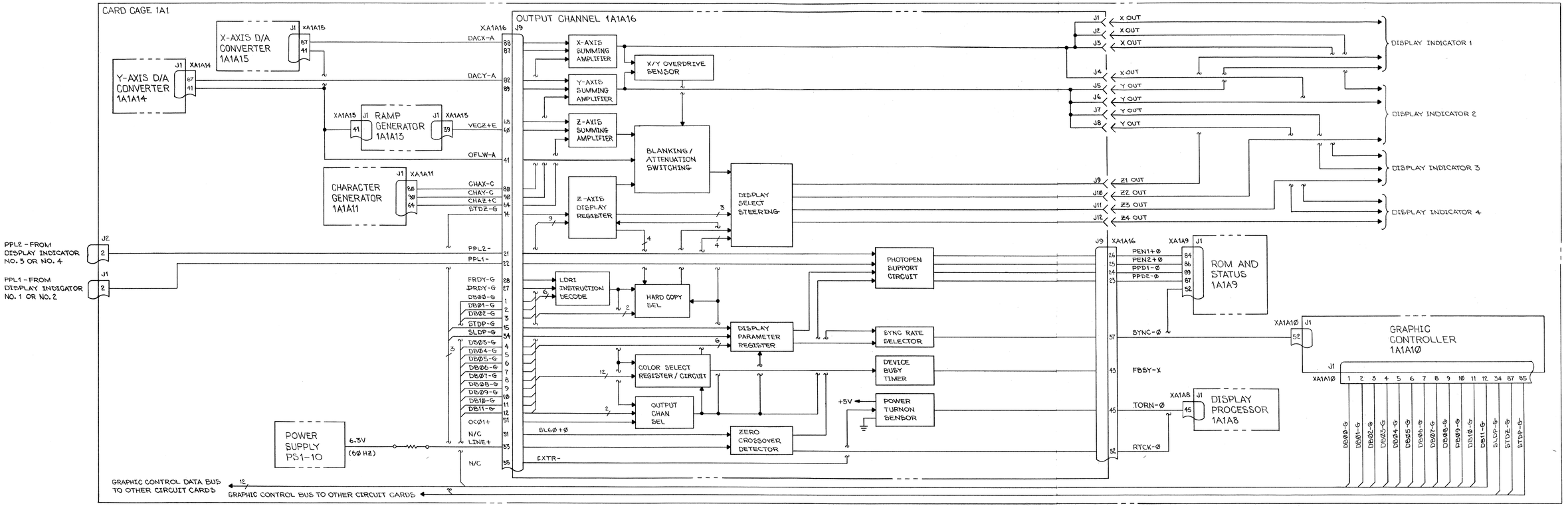


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Figure 3-29. Color Output Channel Card P/N 5977409 Block Diagram

SECTION 4

INSTALLATION

4.1 ENVIRONMENTAL CONSIDERATIONS

The terminal controller is designed to operate in an ambient temperature range of 15°C to 40°C (59°F to 104°F), and a relative humidity not exceeding 90%.

The terminal controller can be mounted in a 10.5-inch vertical space of a standard 19-inch equipment rack, either directly or on optional slide assemblies. The terminal controller can also be mounted in the equipment cabinet (Sanders part number 5976104), which also accommodates a system interconnect panel and a power panel assembly.

4.2 EQUIPMENT CABINET

The equipment cabinet is a four-wheeled, semi-portable equipment rack with the following approximate dimensions:

Height	Width	Depth
30 inches (76.2 cm)	23 inches (58.4 cm)	30 inches (76.2 cm)

When the equipment cabinet contains the terminal controller, system interconnect panel, and power panel assembly, they are arranged as follows:

The terminal controller is accessible from the front of the cabinet, and is installed in the upper half of the cabinet.

The power panel assembly is accessible from the front of the cabinet, and is installed in the lower half of the cabinet.

The system interconnect panel is accessible from the rear of the cabinet, and is installed in the lower half of the cabinet.

The cabinet has doors on both front and back. The front door is hinged on its right side, and is held shut by a magnetic latch. The front door has a cut-out to give access to the terminal controller controls and indicators. The rear door is hinged on its left side, and is held shut by a magnetic latch.

A cut-out in the bottom of the cabinet, below the system interconnect panel, is the entryway for power and signal cables.

4.3 POWER PANEL ASSEMBLY

The standard power panel assembly is Sanders part number 5976120. This power panel assembly is usable with prime power voltages of 100 Vac, 120 Vac, 220 Vac, and 240 Vac.

The power panel assembly contains a circuit breaker (CB1) in the prime power lines; a programmable power transformer; a line filter assembly; a 15-pin connector (J3) for voltage configuration; and a duplex 110 Vac power outlet (J1, J2).

The power cord is Belden type 17612 (length 6 feet, 7 inches, or 2 meters), from which the original power connector has been removed. The first step in installation is to connect an appropriate power connector to this power cord. The three lines in the power cord are color-coded as follows:

Light blue for the neutral line

Brown for the high line

Green/yellow for safety ground

The power cord is soldered to terminals on the line filter. The line filter suppresses transients that may appear on the primary power line. The output of the line filter goes to the circuit breaker.

The circuit breaker opens if the current at 115V exceeds 10A or if the current at 220V exceeds 5A.

The high line output of the circuit breaker goes to pin 1 of connector J3 (brown wire) and to pin 3 of connector J3 (light blue wire). The neutral line output of the circuit breaker goes to pin 2 of connector J3 (tan wire) and to pin 4 of connector J3 (dark blue wire).

The mating connector P3 contains jumper connections that set up the primary windings of the power transformer to match the input voltage. Connector P3 is wired as shown in table 4-1.

Table 4-1. Connector P3 Configurations

G-CONDITION	INPUT VOLTAGE	JUMPERS INSTALLED
G1	100 Vac	1 to 6; 3 to 7; 10 to 13 to 15; 11 to 12 to 14
G2	120 Vac	1 to 5 to 8; 3 to 7 to 9; 10 to 13 to 15; 11 to 12 to 14
G3	220 Vac	2 to 6; 4 to 9; 7 to 8; 10 to 13 to 15; 11 to 12 to 14
G4	240 Vac	2 to 5; 4 to 9; 7 to 8; 10 to 13 to 15; 11 to 12 to 14

Connections from J3 to the transformer primary winding are as follows:

From J3-5 to T1-C (white)

From J3-6 to T1-A (white)

From J3-7 to T1-E (white)

From J3-8 to T1-D (white)

From J3-9 to T1-F (white)

The output from the transformer secondary winding (110 Vac) goes back to connector J3 as follows:

From T1-1 to J3-10 (light blue)

From T1-2 to J3-11 (brown)

The 110 Vac lines go from connector J3 to the duplex output box as follows:

From J3-13 to J2-N (light blue)

From J3-12 to J2-L (brown)

The ground pin of the duplex output box is connected to the outlet box mounting stud.

4.3.1 ALTERNATIVE POWER PANEL ASSEMBLY. The alternative power panel assembly (Sanders part number 5976119) is usable if the prime power is 110 Vac. The alternative power panel contains a filter, a circuit breaker and a duplex outlet box. The power cord is Belden type 17612 (length 6 feet, 7 inches, or 2 meters) with the original power connector left on. Power flow is from the power connector to the filter, to the circuit breaker, and thence to the outlet box.

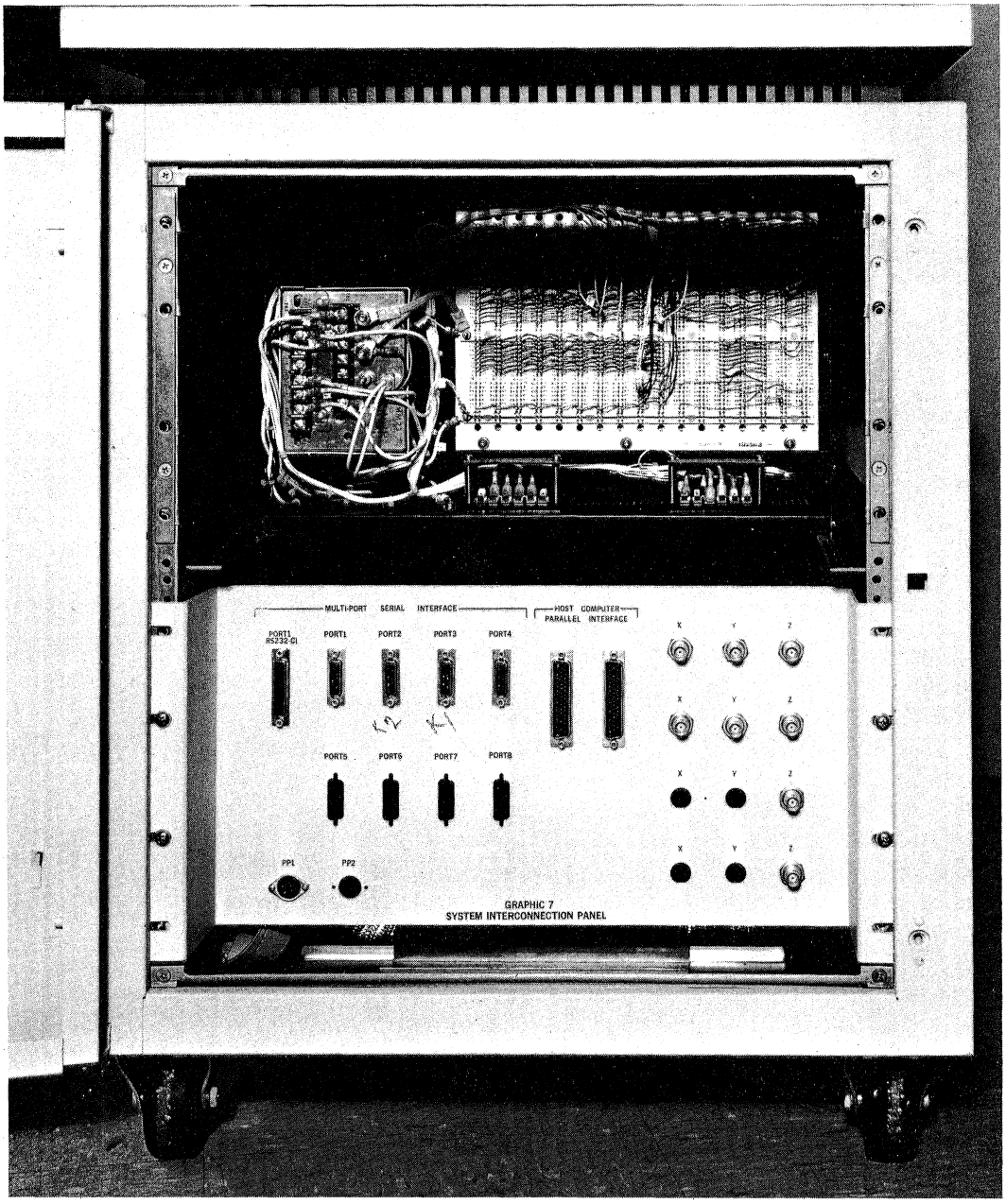
4.4 SYSTEM INTERCONNECT PANEL ASSEMBLY

The system interconnect panel (Sanders part number 5976105G1 or G2) provides a convenient means of connecting the terminal controller to the host computer, to the display indicators, and to other peripheral devices (keyboards, position entry devices, and PHOTOPENS).

The panel assembly consists of a panel with cutouts, and a number of cable assemblies with connectors; some of the connectors are secured to the panel at their respective cutouts. See figure 4-1.

The difference between the G1 and G2 configurations of the system interconnect panel is the number of X and Y connections. The G1 has two X connections and two Y connections. The G2 has four X connections and four Y connections.

Figure 4-2 shows the wiring between the terminal controller and the system interconnect panel and lists the part numbers of the cable assemblies. Note that figure 4-2 shows the back side of the interconnect panel assembly.



NEG 80-346-011

Figure 4-1. System Interconnect Panel

4.5 CONNECTIONS TO BE MADE AT INSTALLATION

4.5.1 TERMINAL CONTROLLER MOUNTED IN EQUIPMENT CABINET. If the terminal controller and equipment cabinet are ordered at the same time, the terminal controller is shipped from the factory installed in the equipment cabinet, and all connections between the terminal controller and the system interconnect panel are already made.

For other situations, refer to figure 4-2.

Connections between the system interconnect panel and other devices are a function of the individual installation. Refer to the top assembly drawing for your installation. In general:

1. Connections to the host computer are made by cables from J7 and J8 of the system interconnect panel to the appropriate point in the host computer. If the parallel interface is not Sanders model no. 5712 (part number 1086802), then the cables needed to connect between the system interconnect panel and the host computer may be supplied with the parallel interface. If the parallel interface is Sanders model no. 5712, then the interconnecting cables are the customer's responsibility.

2. If the GRAPHIC 7 system does not contain a parallel interface, and communications with the host computer are through the multiport serial interface, then the cable needed to connect between the system interconnect panel and the host computer is the customer's responsibility. The cable would normally be connected to the J2 connector on the system interconnect panel, but in some cases could be connected to J3.

3. If the GRAPHIC 7 system includes one alphanumeric keyboard, the keyboard shall connect to J5 on the system interconnect panel. However, if the associated display indicator contains an accessory panel, the keyboard may plug into that accessory panel, from whence another cable leads to J5 on the system interconnect panel.

4. If the GRAPHIC 7 system includes two alphanumeric keyboards and two serial interface cards, the second keyboard connects (either directly or through an accessory panel) to J12 on the system interconnect panel.

5. If the GRAPHIC 7 system includes two alphanumeric keyboards and only one serial interface card, the second keyboard connects (either directly or through an accessory panel) to J4 on the system interconnect panel; the serial interface card must be modified (as described in table 3-14) to make its port 2 appear to be port 7.

6. If the GRAPHIC 7 system includes one position entry device (trackball, forcestick, or data tablet), the PED shall connect to J6 on the system interconnect panel. However, if the associated display indicator contains an accessory panel, the PED may plug into that accessory panel, from whence another cable leads to J6 on the system interconnect panel.

7. If the GRAPHIC 7 system includes two PEDs and two serial interface cards, the second PED connects (either directly or through an accessory panel) to J13 on the system interconnect panel.

8. If the GRAPHIC 7 system includes two PEDs and only one serial interface card, the second PED connects (either directly or through an accessory panel) to J4 on the system interconnect panel; the serial interface card must be modified (as described in table 3-14) to make its port 2 appear to be port 8.

9. If the GRAPHIC 7 system includes one PHOTOPEN, it connects to J26 on the system interconnect panel. However, if the associated display indicator contains an accessory panel, the PHOTOPEN may plug into that accessory panel, from whence another cable leads to J26 on the system interconnect panel.

10. If the GRAPHIC 7 system includes two PHOTOPENs, the second one connects (either directly or through an accessory panel) to J27 on the system interconnect panel. In this case the customer must specify an additional cable, part number 5976150G1, to connect from the system interconnect panel to the PHOTOPEN 2 connector on the terminal controller.

NOTE

Refer to the technical manual for the associated display indicator for PHOTOPEN connections to the display indicator Z connector.

11. The X, Y, and Z connectors on the system interconnect panel are exact replicas of the X, Y and Z connectors on the output channel card. Refer to the technical manual for your display indicator for the method of making connections.

12. Connector J2 on the ROM and status card (usable with a teletypewriter, paper tape reader, keyboard, PED, or even the host computer) does not have a comparable connector on the system interconnect panel. Any connection must be made directly to the connector on the edge of the ROM and status card.

4.5.2 TERMINAL CONTROLLER WITHOUT EQUIPMENT CABINET. If the terminal controller is purchased without the equipment cabinet (as for rack mounting or installation in a display console), and if the system interconnect panel is not procured, then connections between the terminal controller, the host computer, and the peripheral devices must be made directly to connectors on the terminal controller.

If the GRAPHIC 7 system includes a parallel interface, the cables from the host computer go to connectors J2 and J3 on the edge of the parallel interface card. J2 accepts output data and control signals from the host computer. J3 carries input data and control signals to the host computer. Table 4-2 lists and identifies the pins in parallel interface connectors J2 and J3.

If the GRAPHIC 7 system does not include a parallel interface, the cable from the host computer goes to connectors J2 or J3 on the edge of the serial interface card, or (in some cases) to connector J2 on the ROM and status card. In addition,

peripheral devices (keyboard, PED) connect directly to the appropriate connector on the edge of the serial interface card. (Refer to table 3-14.) It is imperative that the serial interface card be configured to match each port to the type of device connected to it. Table 4-3 lists and identifies the pins in serial interface connectors J2 through J6.

The J2 connector on the ROM and status card is identical to connectors J3 through J6 of the serial interface.

Display indicators connect to the X, Y, and Z connectors on the edge of the output channel card. Refer to the technical manual for your display indicator for the method of making connections.

PHOTOPENs connect directly to PHOTOPEN connector J1 and J2 on the terminal controller card cage.

Table 4-2. Parallel Interface I/O Connectors, Pin Assignments

JACK/PIN	SIGNAL	JACK/PIN	SIGNAL	JACK/PIN	SIGNAL
J2-1	0D00(±)	J2-34	SPARE	J3-17	ID08(±)
J2-2	DRET-	J2-35	ATN1(±)	J3-18	DRET-
J2-3	0D01(±)	J2-36	DRET-	J3-19	ID09(±)
J2-4	DRET-	J2-37	OWR(±)	J3-20	DRET-
J2-5	0D02(±)	J2-38	DRET-	J3-21	ID10(±)
J2-6	DRET-	J2-39	OMR(±)	J3-22	DRET-
J2-7	0D03(±)	J2-40	DRET-	J3-23	ID11(±)
J2-8	DRET-	J2-41	OCTL(±)	J3-24	DRET-
J2-9	0D04(±)	J2-42	DRET-	J3-25	ID12(±)
J2-10	DRET-	J2-43	ODR(±)	J3-26	DRET-
J2-11	0D05(±)	J2-44	DRET-	J3-27	ID13(±)
J2-12	DRET-	J2-45	SPARE	J3-28	DRET-
J2-13	0D06(±)	J2-46	SPARE	J3-29	ID14(±)
J2-14	DRET-	J2-47	INIT	J3-30	DRET-
J2-15	0D07	J2-48	DRET-	J3-31	ID15(±)
J2-16	DRET-	J2-49	*IMR(±)	J3-32	DRET-
J2-17	0D08(±)	J2-50	SPARE	J3-33	*SPR1-
J2-18	DRET-			J3-34	SPARE
J2-19	0D09(±)	J3-1	ID00(±)	J3-35	IMR(±)
J2-20	DRET-	J3-2	DRET-	J3-36	DRET-
J2-21	0D10(±)	J3-3	ID01(±)	J3-37	ICTL(±)
J2-22	DRET-	J3-4	DRET-	J3-38	DRET-
J2-23	0D11(±)	J3-5	ID02(±)	J3-39	ATN2(±)
J2-24	DRET-	J3-6	DRET-	J3-40	DRET-
J2-25	0D12(±)	J3-7	ID03(±)	J3-41	IWR(±)
J2-26	DRET-	J3-8	DRET-	J3-42	DRET-
J2-27	0D13(±)	J3-9	ID04(±)	J3-43	SPARE
J2-28	DRET-	J3-10	DRET-	J3-44	DRET-
J2-29	0D14(±)	J3-11	ID05(±)	J3-45	NDRY(±)
J2-30	DRET-	J3-12	DRET-	J3-46	SPARE
J2-31	0D15(±)	J3-13	ID06(±)	J3-47	SPARE
J2-32	DRET-	J3-14	DRET-	J3-48	SPARE
J2-33	*SPR1-	J3-15	ID07(±)	J3-49	*SPR2-
		J3-16	DRET-	J3-50	SPARE

*Signals used only in test operation using input to output (J3 to J2) loop cable.

Table 4-3. Multiport Serial Interface I/O Connectors, Pin Assignments

JACK/PIN	SIGNAL	
J2-1	CGND	PORT 1
J2-2	SPARE	
J2-3	X232-	
J2-4	TSCK+	
J2-5	RDA1-	
J2-6	SPARE	
J2-7	RQTS+	
J2-8	RSCK+	
J2-9	CLTS+	
J2-10	SPARE	
J2-11	DSRY+	
J2-12	SPARE	
J2-13	SPARE	
J2-14	DGND	
J2-15	DTRY+	
J2-16	CARR+	
J2-17	SPARE	
J2-18	SPARE	
J2-19	RING+	
J2-20	SPARE	
J2-21	SPARE	
J2-22	SPARE	
J2-23	TXCO+	
J2-24	SPARE	
J2-25	SPARE	
J2-26	SPARE	
J3-1	XMT1-	PORT 1
J3-2	P15V+	
J3-3	DRET-	
J3-4	DRET-	
J3-5	RDA1-	
J3-6	P05V+	
J3-7	DRET-	
J3-8	DRET-	

JACK/PIN	SIGNAL	
J3-9	REN1-	PORT 1
J3-10	N15V	
J4-1	XMT2-	PORT 2
J4-2	P15V+	
J4-3	DRET-	
J4-4	DRET-	
J4-5	RDA2-	
J4-6	P05V+	
J4-7	DRET-	
J4-8	DRET-	
J4-9	REN2-	
J4-10	N15V-	
J5-1	XMT3	PORT 3
J5-2	P15V+	
J5-3	DRET-	
J5-4	DRET-	
J5-5	RDA3-	
J5-6	P05V+	
J5-7	DRET-	
J5-8	DRET-	
J5-9	REN3-	
J5-10	N15V-	
J6-1	XMT4-	PORT 4
J6-2	P15V+	
J6-3	DRET-	
J6-4	DRET-	
J6-5	RDA4-	
J6-6	P05V+	
J6-7	DRET-	
J6-8	DRET-	
J6-9	REN4-	
J610	N15V-	

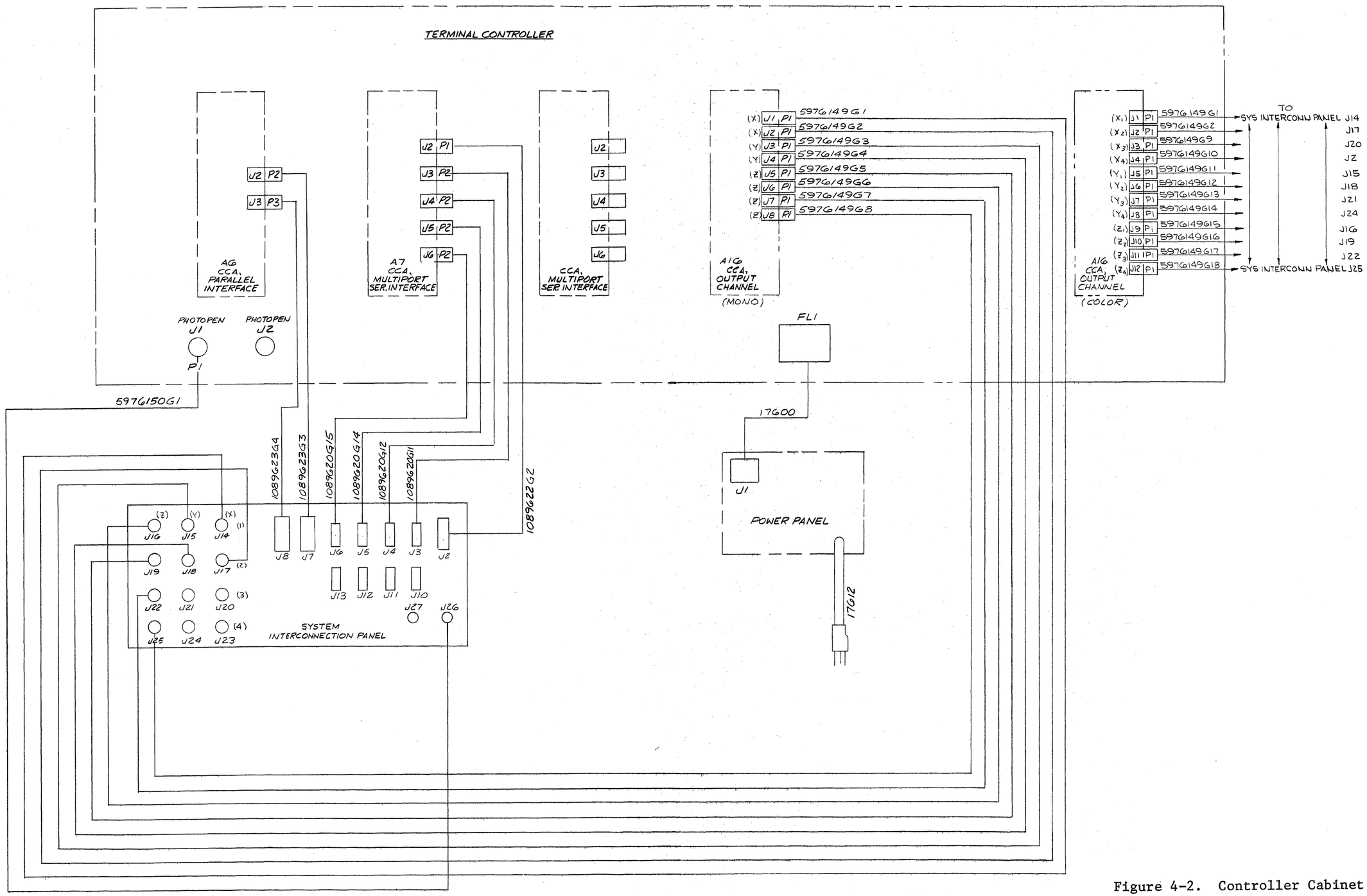


Figure 4-2. Controller Cabinet Interconnect Diagram

4.6 SWITCH AND JUMPER SELECTIONS

Some of the circuit cards in the terminal controller contain jumper terminals and/or switches to allow selection of operating characteristics that differ from those normally preselected at the factory.

4.6.1 DISPLAY PROCESSOR. Terminals E39 and E40 let the display processor recognize instruction 0 as a halt instruction or as an illegal instruction, as follows:

STATUS	JUMPER CONFIGURATION
Instruction 0 = halt	E39 to E40 jumpered (normal configuration)
Instruction 0 illegal	E39 and E40 open

4.6.2 8K READ/WRITE MEMORY CARD. Switch S1 on the 8K read/write memory card selects the range of addresses to which the card responds. Switch S1 has eight sections, of which only the first two are used.

In a single card system, set all positions of S1 to OFF.

In a two-card system:

a. On the first card, set all positions of S1 to OFF.

b. On the second card, set position 1 to ON, all other positions to OFF.

In a three-card system:

a. On the first card, set all positions of S1 to OFF.

b. On the second card, set position 1 to ON, all other positions to OFF.

c. On the third card, set position 2 to ON, all other positions to OFF.

4.6.3 8K ROM AND STATUS CARD. This card contains jumper terminals that allow reconfiguration of 15 different parameters, as described in table 4-4.

Table 4-4. ROM and Status Card Jumper Configurations

FEATURE	JUMPER CONFIGURATION
Sync link interrupt level	
Level 7	E1 to E4 (normal configuration)
Level 6	E2 to E4
Level 5	E3 to E4

Table 4-4. ROM and Status Card Jumper Configurations (Cont)

FEATURE	JUMPER CONFIGURATION
Display status interrupt level	
Level 5	E3 to E5 (normal configuration)
Level 6	E2 to E5
Level 7	E1 to E5
Transmit data select	
TTY, RS-232C, or 20 mA current loop	E7 to E8 (normal configuration)
TTL	E7 to E6
Receive data termination	
TTY	E35 to E36 (normal configuration)
TTL	E9 to E10; E35 to E36 open
20 mA current loop	E9 to E11; E35 to E36 open
RS-232C	No jumper at E35, E36, E9
Receive/transmit data	
TTY	E12 to E13 open (normal configuration)
TTL or RS-232C	E12 to E13
Word length select	
5 bits	E14 to E17 to E19
6 bits	E14 to E19
7 bits	E17 to E19
8 bits	E14 and E17 open (normal configuration)
Receive/transmit parity	
Checked and generated	E16 to E19
Disabled	E16 open (normal configuration)

Table 4-4. ROM and Status Card Jumper Configurations (Cont)

FEATURE	JUMPER CONFIGURATION
Parity select	
Odd	E18 to E19
Even	E18 open (normal configuration)
Number of stop bits	
2 stop bits	E15 to E19
1 stop bit	E15 open (normal configuration)
Receive/transmit frequency select	
110 baud	E20 to E22; E23 to E25 to E26 to E27 (normal configuration)
300 baud	E20 to E22; E24 to E26 to E27
1200 baud	E20 to E22; E26 to E27
2400 baud	E20 to E22; E23 to E25 to E27
4800 baud	E20 to E22; E23 to E24 to E27
9600 baud	E20 to E22; E23 to E27
50K baud	E20 to E21
System clock mode	
Internal clock	E28 to E29 (normal configuration)
External clock	E29 open
Address selection	
16K to 24K	E44 to E32
20K to 28K	E30 to E32
24K to 32K	E31 to E32
NOTE The 4K ROM and status card has only the following address selections:	
20K to 24K	E30 to E32
24K to 28K	E31 to E32

Table 4-4. ROM and Status Card Jumper Configurations (Cont)

FEATURE	JUMPER CONFIGURATION
Status logic enable	
Enabled	E33 to E34 (normal configuration)
Disabled	E33 open
Trap address memory locations	
0 - 8K	E37, E38, E39, E40 open (normal configuration)
8K - 16K	E39 to E40
16K - 24K	E37 to E38
24K - 32K	E37 to E38; E39 to E40
50K/800K baud select	
50 kHz	E42 to E43 (normal configuration)
800 kHz	E41 to E43

4.6.4 MULTIPORT SERIAL INTERFACE. This card contains both jumper terminals and DIP switches that allow reconfiguration of 14 different parameters, as described in table 4-5.

Table 4-5. Multiport Serial Interface Parameter Selections

FEATURE	CONFIGURATION
NOTE This table applies to serial interface part number 5976251. If your serial interface is part number 1086750, refer to H-78-0095.	
Device address select	
Standard address (1765XX)	U19-S8 OFF (normal configuration)
Expanded address (1766XX)	U19-S8 ON
Device assignments	
Refer to table 3-14.	

Table 4-5. Multiport Serial Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION			
Word length select	Port 2	Port 3	Port 4	
5 bits	E43 to E44, E45 to E46	E33 to E34, E35 to E36	E53 to E54, E55 to E56	
6 bits	E45 to E46	E35 to E36	E55 to E56	
7 bits	E43 to E44	E33 to E34	E53 to E54	
8 bits (normal configuration)	E44, E46 open	E34, E36 open	E54, E56 open	
Parity select	Port 2	Port 3	Port 4	
Parity enabled (normal configuration)	E49 to E50	E39 to E40	E59 to E60	
Parity disabled	E50 open	E40 open	E60 open	
Odd parity	E47 to E48	E37 to E38	E57 to E58	
Even parity	E48 open	E38 open	E58 open	
Stop bit select	Port 2	Port 3	Port 4	
1 stop bit (normal configuration)	E51 to E52	E41 to E42	E61 to E62	
2 stop bits	E52 open	E42 open	E62 open	
Transmit levels	Port 1	Port 2	Port 3	Port 4
RS-232 (normal configuration)	E9 to E10	E12 to E13	E30 to E31	E23 to E24
TTL	E10 to E11	E13 to E14	E31 to E32	E24 to E25
Receive levels	Port 1	Port 2	Port 3	Port 4
TTL	E5 to E6	E15 to E16	E19 to E20	E26 to E27
RS-232	E5 open	E15 open	E19 open	E26 open

Table 4-5. Multiport Serial Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
F_t baud rate (all ports, asynchronous)	
NOTE E63 to E64 and E65 to E66 are connected for all baud rates.	
9600 baud (normal configuration)	E68 to E67; E69, E71, E73 open
50 baud	E68 to E67 to E69 to E71 to E73
75 baud	E68 to E69 to E71 to E73
110 baud	E68 to E67 to E71 to E73
134.5 baud	E68 to E71 to E73
150 baud	E68 to E67 to E69 to E73
300 baud	E68 to E69 to E73
600 baud	E68 to E67 to E73
1200 baud	E68 to E73
1800 baud	E68 to E67 to E69 to E71
2000 baud	E68 to E69 to E71
2400 baud	E68 to E67 to E71
3600 baud	E68 to E71
4800 baud	E68 to E67 to E69
7200 baud	E68 to E69
19200 baud	E68 to E67

F_r baud rate (port 1 only)	U80-S4	U80-S5	U80-S6	U80-S7
50	On	On	On	On
75	Off	On	On	On
110	On	Off	On	On
134.5	Off	Off	On	On

Table 4-5. Multiport Serial Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION			
F_r baud rate (port 1 only) (Cont)	U80-S4	U80-S5	U80-S6	U80-S7
150	On	On	Off	On
300	Off	On	Off	On
600 (normal configuration)	On	Off	Off	On
1200	Off	Off	Off	On
1800	On	On	On	Off
2000	Off	On	On	Off
2400	On	Off	On	Off
3600	Off	Off	On	Off
4800	On	On	Off	Off
7200	Off	On	Off	Off
9600	On	Off	Off	Off
19200	Off	Off	Off	Off
Number of stop bits (port 1)				
1 stop bit	U80-S3 on			
2 stop bits	U80-S3 off			
Parity (port 1 only)				
Parity disabled	U80-S1 off			
Parity enabled	U80-S1 on			
Odd parity	U80-S2 on			
Even parity	U80-S2 off			

NOTE

If parity is disabled, there are eight data bits. If parity is enabled, there are seven data bits.

Table 4-5. Multiport Serial Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
Data terminal ready (port 1 only)	
Circuit forced on	U39-S7 off
Circuit under system control	U39-S7 on
Interrupt level select	
Level 5	E1 to E3
Level 6 (normal configuration)	E2 to E3
Level 7	E4 to E3

Figure 4-3 shows the normal switch positions for the standard port configuration. The + mark on the switch indicates the ON side. The dots in the figure indicate the side of the switch that is pushed down.

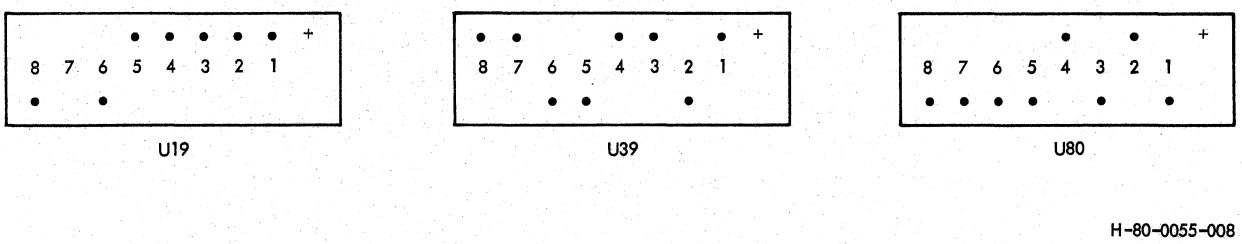


Figure 4-3. Serial Interface, Normal Switch Positions

4.6.5 PARALLEL INTERFACE. The parallel interface card contains 105 terminals that allow you to customize the card for special installations. Most of the terminals (E1 through E43 and E49 through E66) plus an 2.35 by 6.5 inch (6 by 16.5 cm) unused area are for use with additional integrated circuit elements, which can interface with devices that have unique signal definitions, signal polarities, handshaking requirements, and/or driver/receiver and line matching requirements.

The remaining terminals let you change certain operating parameters, as described in table 4-6.

Table 4-6. Parallel Interface Parameter Selections

FEATURE	CONFIGURATION
Register address select	
First card, address 17241X (normal configuration)	E96 to E99
Second card, address 17243X	E98 to E99

Table 4-6. Parallel Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
Register address select (Cont)	
Third card, address 17245X	E97 to E99
Fourth card, address 17247X	E95 to E99
Interrupt trap address select	
First card (normal configuration)	E87, E88 open; E47, E45 open
Second card	E87 to E88, E46 to E47; E45 open
Third card	E87 to E88, E44 to E45; E47 open
Fourth card	E87 to E88, E44 to E45, E46 to E47
Word vs byte mode	
Word mode (normal configuration)	E90 open
Byte mode	E89 to E90
Polarity of INIT signal from host	
Low (INIT-) produces SYST-B	E93 to E94
High (INIT+) produces SYST-B	E92 to E94
SYST-B inhibited	E91 to E94
Interrupt priority level	
Level 6 (normal configuration)	E83 to E85
Level 5	E84 to E85
Level 7	E86 to E85
Clock speed	
CLOK-F (10 MHz) (normal configuration)	E100 to E101
Clock rate divided (for long distance interface)	Open E100 to E101. Connect E100 to input of a suitable divider. Connect divider output to E101. (Divider may be added to the parallel interface card or located externally with connections made through unused backplane connections).

Table 4-6. Parallel Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
Output data enable ODEN- signal from host	
ODEN- enabled	E102 to E103
ODEN- disabled	E102, E103 open
Input data enable function	
Ground enable to input drivers	E104 to E105
Ground enable not required	E104, E105 open
Additional integrated circuit connections	
NOTE These connections allow additional integrated circuits to be added to the card.	
Connect attention interrupt enable to IC	E48
Accept interrupt requests from IC	E67
Connect resets to IC	E68
Connect fixed logic high to IC	E69
Connect +5V to IC	E70 through E78
Connect -15V to IC	E79
Connect ARET- to IC	E80
Connect +15V to IC	E81
Accept reset from IC	E82
Card device select	
Normal configuration is:	
DEV0-B high	E112, E113 open
DEV1-B low	E114 to E115

Table 4-6. Parallel Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
Card device select (Cont)	
DEV2-B high	E116, E117 open
DEV3-B active	E110 to E111
Device codes for second, third, and fourth cards can be created by connecting E112 to E113, E116 to E117, or both.	

4.6.6 GRAPHIC CONTROLLER. The graphic controller card contains four terminals to select the memory addressing capability, as follows:

MEMORY ADDRESS BITS	CONNECTIONS
16 bits	E1, E2, E3, E4 all open
17 bits	E2 to E4; E1 and E3 open
18 bits (normal configuration)	E1 to E3, E2 to E4

4.6.7 RAMP GENERATOR. The ramp generator contains seven terminals. Two of these terminals let you disable the FBSY-X (function busy) override function during fast beam moves. The other five let you change the ratio between slow speed and normal speed from 1/16 (its normal value) to 1/8, 1/4, or 1/2. These selections are described in table 4-7.

Table 4-7. Ramp Generator Parameter Selections

FEATURE	CONFIGURATION
Function busy override	
Enabled (normal configuration)	E5 to E6
Disabled	E5, E6 open
Slow speed/normal speed ratio	
1/16 (normal configuration)	E9 to E10
1/8	E9 to E7
1/4	E9 to E8
1/2	E9 to E11

4.6.8 CHARACTER GENERATOR. The character generator card contains 12 terminals that allow the card to respond either to ASCII character codes (the normal configuration) or EBCDIC character codes, as follows:

ASCII CODE JUMPERS	EBCDIC CODE JUMPERS
For 96-character card:	E2 to E3
E1 to E4, E2 to E3;	E4 to E5
E5 open	E6 to E7
For 192-character card:	E9 to E10
E1 to E2, E3 to E4;	E12 to E14
E5 open	E1, E8, E11, E13 open
For both cards:	
E7 to E8; E6 open	
E10 to E11; E9 open	
E12 to E13; E14 open	

SECTION 5

MAINTENANCE

5.1 GENERAL

This section contains the maintenance philosophy, test equipment required, troubleshooting instructions, adjustments, and repair information.

5.2 MAINTENANCE PHILOSOPHY

The maintenance philosophy for the terminal controller is to limit repairs to replacement of plug-in circuit cards and chassis-mounted components. This approach reduces system down-time if a failure occurs. Field repair of circuit cards is not recommended because of their complexity. Testing them requires special factory-level test equipment.

If you encounter a failure, try to isolate the failure to a specific circuit card, then replace that card and make any required adjustments. If the system resumes normal operation, the card that you took out is defective. Return that card to Sanders for repair. Send us also a description of the symptoms that led you to the failed card.

5.3 TEST EQUIPMENT REQUIRED

The following equipment (or equivalent) is recommended for maintenance of the terminal controller:

Oscilloscope	Tektronix type 547 with type 1A1 preamplifier
Digital voltmeter	Fluke model 8000A
Multimeter	Triplett model 630
Card extender	Sanders part no. 1086794

5.4 TROUBLESHOOTING INSTRUCTIONS

Follow the steps indicated in figure 5-1. Pay attention to the cautions on sheet 1 of the figure.

5.4.1 BUILT-IN DIAGNOSTICS. When the terminal controller is initialized in the SYSTEM mode, it executes a set of diagnostic routines that test the GO/NO GO status of certain circuit cards. If a NO GO is detected, the terminal controller sets a bit in the diagnostic error word, and an error message containing the error word is sent to the host computer. The message indicates the diagnostic routine that failed, but does not specifically state how the routine failed.

When you initialize the terminal controller in the LOCAL mode, it executes the same set of diagnostic routines, then executes the terminal verification pattern. The results of the diagnostic routines are displayed in the left field of the readout box as an octal number with the letter T above it (the letter T means that the 3-digit code is the result of the diagnostic routines).

If all tests pass, the 3-digit number is 000, assuming all cards are installed. If any card is not installed, the bit for that card is set, producing an error indication (see table I in figure 5-1).

If more than one test fails, and sequencing through the remaining tests does not stop, the readout is the sum of all the failed tests. For example, if the terminal controller does not contain a 3D coordinate converter, and both the memory and the display generator diagnostics fail, the readout is 045.

The following paragraphs describe the diagnostic routines.

Serial Interface Diagnostic. This test verifies initialization of the status registers.

Parallel Interface Diagnostic. This test verifies initialization of the handshaking circuits and status registers.

Display Processor Diagnostic. This test verifies execution of a branch instruction, an interrupt sequence, and single-word, double-word, and triple-word instructions from the instruction set.

Memory Diagnostic. This test verifies the ability to write and read at each memory location. (During this test, any data already contained in a memory location is temporarily stored in a general purpose register, then restored to its location.)

Display Generator Diagnostic. This test verifies that:

1. Each display register is initialized.

2. The graphic controller and function generators are in their proper states.

3. The display processor can start a refresh sequence.

4. The graphic controller can start, run, access memory, perform refresh functions, and stop.

3D Coordinate Converter Diagnostic. This test verifies the 3D coordinate converter's ability to write and execute a simple instruction.

5.4.2 TERMINAL VERIFICATION PATTERN. The terminal verification pattern can be used with up to two display indicators and a full complement of peripherals. The pattern verifies proper alignment of the various function generators and display indicators. Each area of the verification pattern has a specific function: either executing a system parameter or providing a visual indication for maintenance adjustments.

5.4.2.1 Vector/Position Generator Verification. The components of the terminal verification pattern that verify operation of the vector/position generator are:

1. The full screen box.

2. The 3/4 screen box.

3. D/A alignment bars.

4. The letter H in two places at the left edge of the 3/4 screen box.

Each letter H in two places is written as two characters, written at the same position under different internal conditions. If the ramp generator is properly adjusted, each letter H appears as a single character. If X-axis ghosting appears in either letter H, the ramp generator or ramp/conic generator requires adjustment.

The 3/4 screen box includes the four types of line structure: center line at the top, dotted line at the right, solid line on the bottom, and dashed line at the left. Incorrect line structure indicates a faulty ramp generator.

The D/A alignment bars consist of nine lines each and show the D/A adjustment for selection of 1/8, 1/4, and 1/2 screen positions. These bars are not PHOTOPEN sensitive. If there is any offset between the lines at the tops and bottoms of the bars, or if the lines are not parallel, D/A converter adjustment is required.

Observe the corners of the full-screen box, the 3/4-screen box, and the small box around the readout area. If there is any breakage at the corners of any box, the ramp generator requires adjustment.

5.4.2.2 Character Generator Verification. The character generator area of the test pattern displays the character generator repertoire, including alphanumerics and special symbols. In addition, the letters EM are displayed in four different sizes. Dots at the left side of the largest E and beneath the largest M verify the proper character height and width, depending on the screen size. If the E and M do not match the dots, character generator adjustment is required.

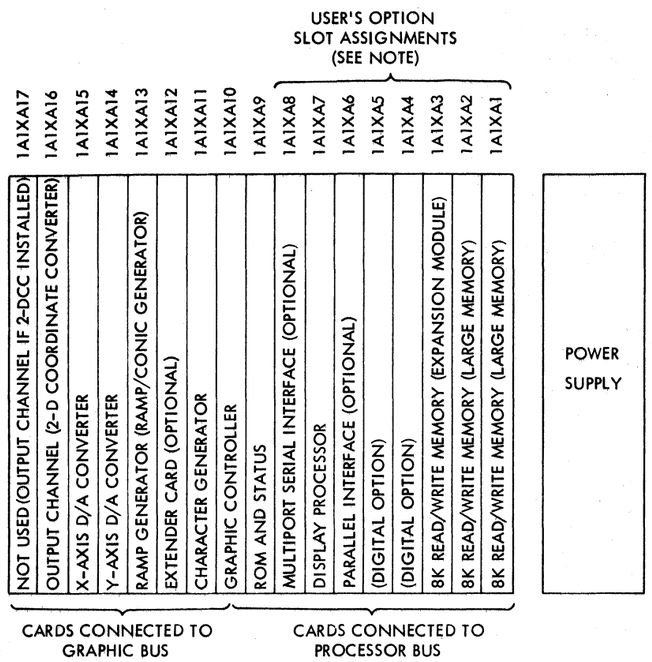
5.4.2.3 Character Rotate and Gray Level Verification. The large, rotated numerals at the lower left corner of the 3/4-screen box verify that the graphic controller can rotate characters and that the output channel can vary intensity level.

5.4.3 ADDITIONAL HINTS. The circuit cards that connect to the processor bus (cards in slots XA1 through XA8) can be installed in other arrangements than that shown in figure 5-1. However, the following rules must be followed:

1. All read/write memory cards should be installed in consecutive slots.

2. Those cards that can seize the processor bus should be installed in consecutive slots, to maintain the integrity of the grant bus. If there is a gap between such cards, you effectively get two grant buses in parallel, with subsequent interference when two cards want the bus at the same time. If it is necessary to separate such cards, you must

connect the grant out connection (pin 35) of the higher priority card (lower numbered slot) across the gap to the grant in connection (pin 36) of the next lower priority card (higher numbered slot). For this type of connection, use Sanders part number 47067, daisy-chain jumper.



NOTE

The backplane wiring for the card cage is identical for card slots 1A1XA1 through 1A1XA8, making the designated card placement for those slots arbitrary. Except for the read/write memory cards, the cards in these eight slots can be interchanged to reassign processor bus control priorities as desired, with the bus control priority grant function being passed in card slot sequence from the highest-priority slot (1A1XA1) toward the lowest-priority card (graphic controller 1A1XA10). Relocatable cards must be placed in adjacent slots (1A1XA8, 1A1XA7, 1A1XA6, etc., in that order); leaving any one of these slots vacant would break the priority chain, which could result in unit malfunction. The read/write memory cards are passive circuits that are accessed by the processor bus but do not seize bus control; their grant outputs never go false. Accordingly, read/write memory cards should be placed in available position (usually spaced for better heat dissipation) toward the highest-priority slot.

WARNING

TERMINAL CONTROLLER OPERATES ON 110 VAC POWER. ASSOCIATED POWER CONTROL PANEL MAY HAVE 220 TO 240 VAC INPUT.

CAUTION

ALWAYS TURN TERMINAL CONTROLLER OFF AND REDUCE DISPLAY INDICATOR BRIGHTNESS BEFORE REMOVING OR INSERTING CIRCUIT CARDS.

CHARACTER GENERATOR CARD AND D/A CONVERTER CARDS CONTAIN MOS DEVICES. WHEN NOT IN USE, STORE THESE CARDS IN STATIC-PROOF CONTAINERS.

NOTES

1. TECHNICAL MANUALS FOR DISPLAY INDICATORS:

MODELS	MANUAL NO.
730-733	H-79-0378
740-743	H-79-0394
750, 753	H-79-0386
760, 763	H-79-0395

2. TECHNICAL MANUAL FOR MODEL 5783/5784 KEYBOARDS: H-79-0363.

3. TECHNICAL MANUAL FOR MODEL 5781 PHOTOPEN: H-78-0042.

4. TECHNICAL MANUAL FOR MODEL 5786 TRACKBALL/5787 FORCESTICK: H-78-0044. FOR SIMPLE-2 DATA TABLET, SEE TALOS MANUAL 50114-1.

5. TECHNICAL MANUAL FOR MODEL 570 HARDCOPY UNIT: GA-77-045. TECHNICAL MANUAL FOR MODEL 0575 HARDCOPY MULTIPLEX SWITCH: H-78-0435. FOR SOFTWARE INSTRUCTIONS, SEE H-79-0348.

6. FOR SOFTWARE INSTRUCTIONS, SEE H-79-0350.

7. ALIGNMENT PROCEDURES:

CARD	PARAGRAPH
RAMP GENERATOR	5.5.1
D/A CONVERTERS	5.5.2
CHARACTER GENERATOR	5.5.3
MONOCHROME OUTPUT CHANNEL	5.5.4.1
COLOR OUTPUT CHANNEL	5.5.4.2

8. TECHNICAL MANUALS FOR POWER SUPPLIES:

   MODEL MM23-E0647/115 H-80-0087

   IF OTHER MODELS ARE USED, APPROPRIATE MANUALS WILL BE PROVIDED.

9. TECHNICAL MANUAL FOR 2D COORDINATE CONVERTER: H-78-0061.

H-80-0055-011A

Figure 5-1. Terminal Controller Troubleshooting Diagram, Sheet 1

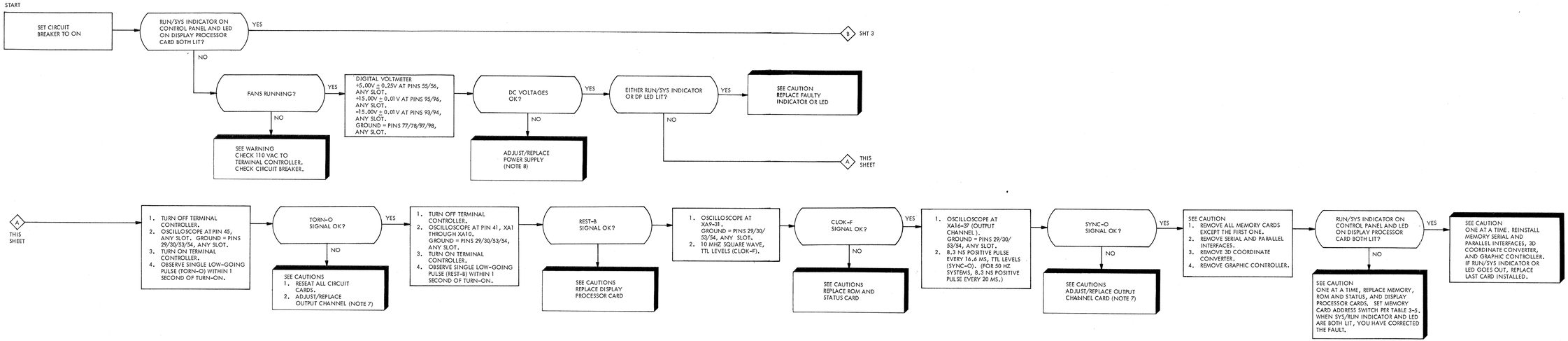
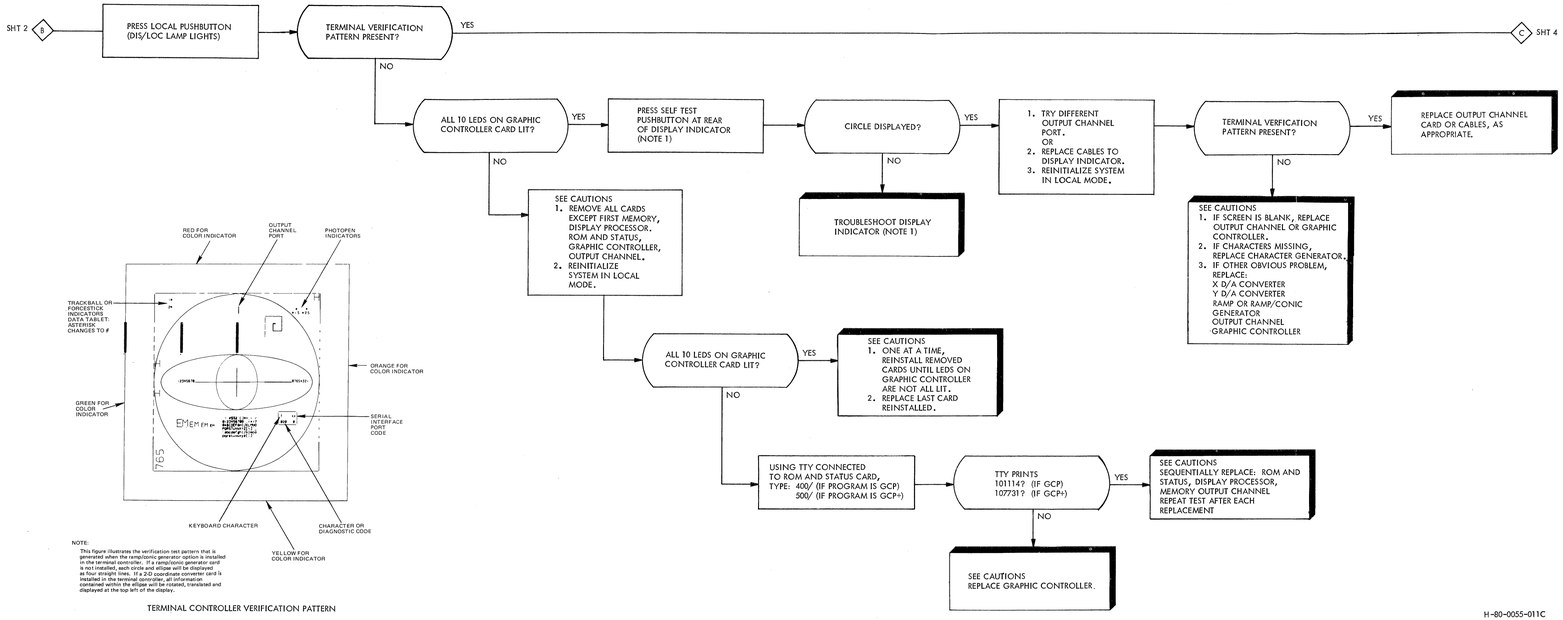


Figure 5-1. Terminal Controller Troubleshooting Diagram, Sheet 2



NOTE:
This figure illustrates the verification test pattern that is generated when the ramp/conic generator option is installed in the terminal controller. If the ramp/conic generator card is not installed, each circle and ellipse will be displayed as four straight lines. If a 2-D coordinate converter card is installed in the terminal controller, all information contained within the ellipse will be rotated, translated and displayed at the top left of the display.

TERMINAL CONTROLLER VERIFICATION PATTERN

Figure 5-1. Terminal Controller Troubleshooting Diagram, Sheet 3

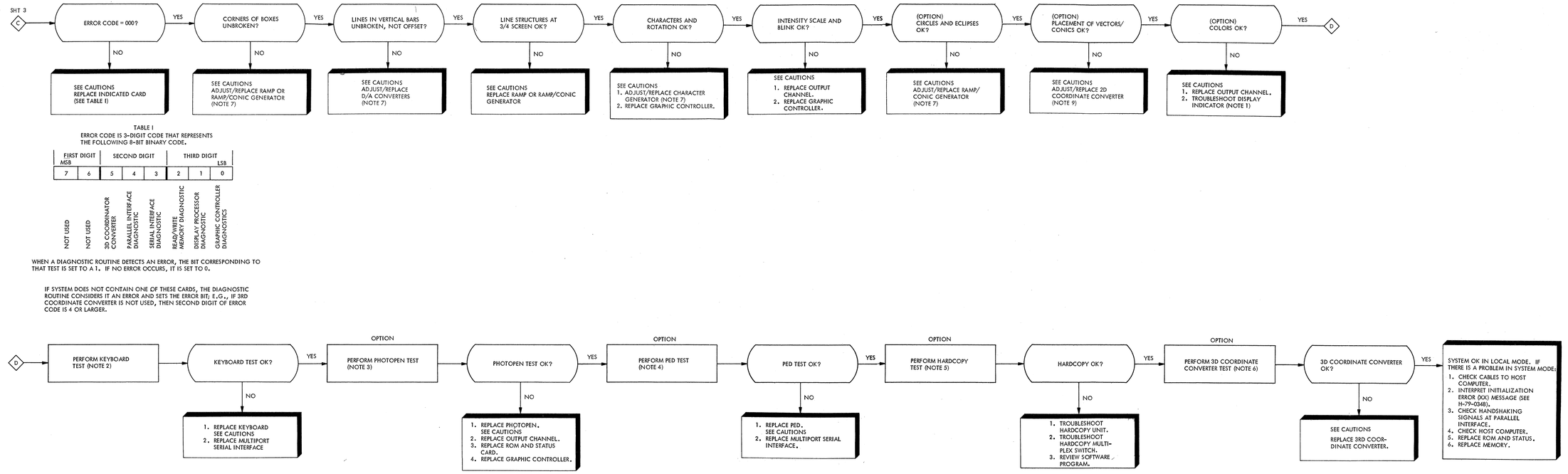


Figure 5-1. Terminal Controller Troubleshooting Diagram, Sheet 4

5.5 ADJUSTMENT PROCEDURES

The following circuit cards contain adjustment points:

1. Ramp generator
2. D/A converters
3. Output channel
4. Character generator

NOTES

The read/write memory card has four adjustment points. These are critical factory adjustments. Any attempt to adjust them in the field can result in equipment misalignment.

For power supply adjustments, refer to separate power supply manual.

The Sanders extender card (part no. 1086794) is required for making card adjustments. Distributed electrical characteristics of a card may be slightly different when the card is mounted on the card extender. You may have to make some slight compensation before the card is reinstalled in the card cage.

5.5.1 RAMP GENERATOR ADJUSTMENTS. The ramp generator has six adjustments (see figure 5-2). Adjust the ramp generator as follows.

Table 5-1. Ramp Generator Adjustments

SETUP	ADJUSTMENT POINT	PROPER INDICATION
SYSTEM mode. Digital voltmeter between TP3 (REFP+E) and TP2 (ground).	R113 (reference adjust)	+5.00V ± 0.01V
SYSTEM mode. Connect TP1 to TP2. Digital voltmeter between TP4 (RAMP+) and TP2.	R20 (baseline adjust)	0V. Disconnect TP1 from TP2 after adjustment.
LOCAL mode, verification test pattern displayed.	R11 (-ramp limit), R15 (+ramp limit)	Minimum ghosting of letter H (two places) at left side of verification test pattern.
Observe verification test pattern.	R28 (B-clamp), R29 (A-clamp)	Best corner closure without blooming in full and 3/4-screen boxes.
NOTE R11 and R15 also affect corner closure. Make best compromise between corner closure and minimum ghosting.		
Observe verification test pattern. Set display indicator brightness level for optimum display consistent with ambient light level.	R44 (short vector brightness adjust)	Short vectors in involute pattern at upper right corner of 3/4-screen box have same brightness as other vectors in display.
NOTE This adjustment is valid only for the particular brightness setting of the display indicator. At radically different brightness settings, short vectors may be too faint or too bright.		

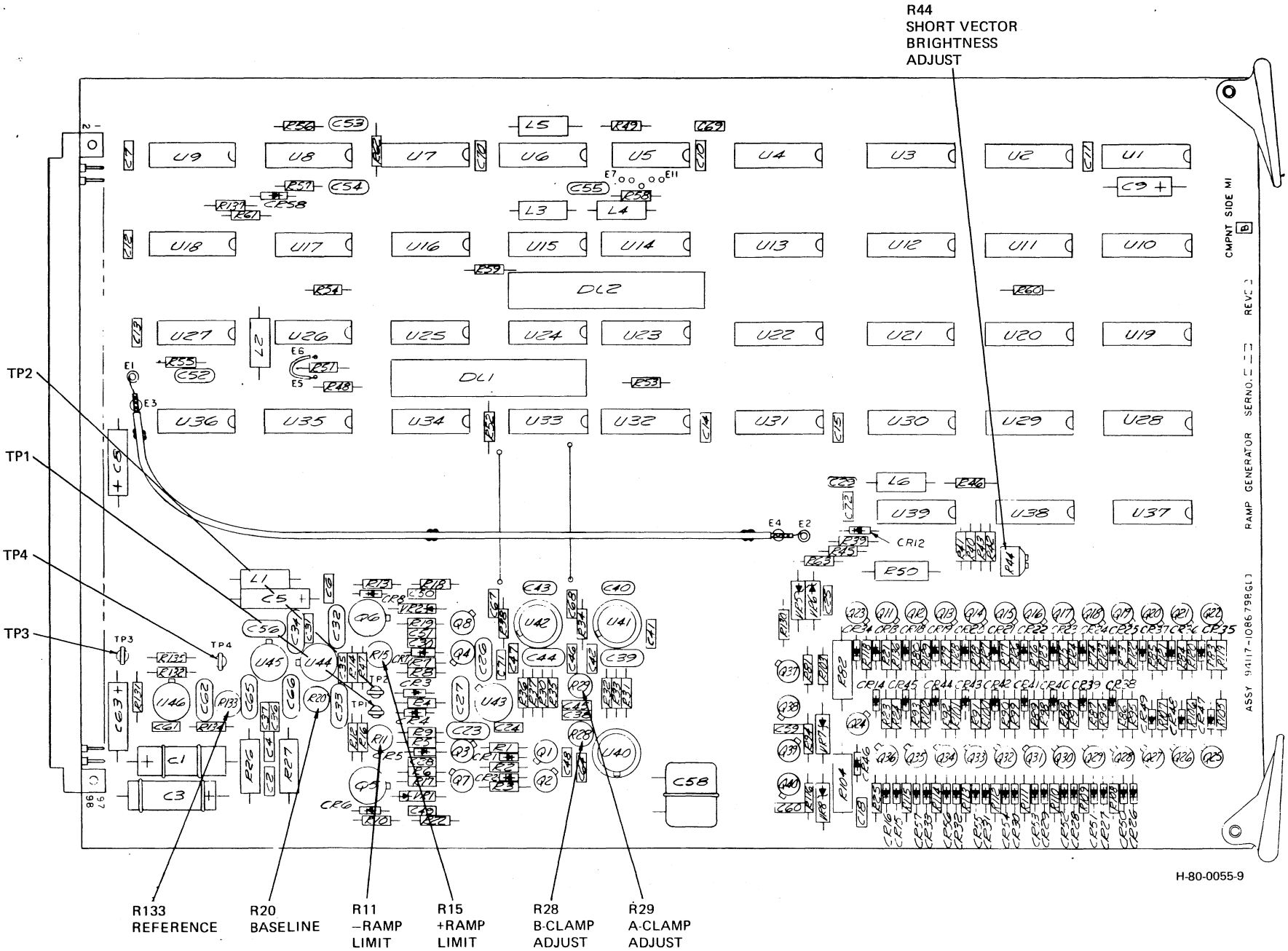


Figure 5-2. Ramp Generator Card Adjustments

5.5.2 D/A CONVERTER ADJUSTMENTS. Each D/A converter has seven potentiometers and may have one or two adjustable capacitors (see figure 5-3). Always adjust the X D/A converter first at slot XA15. Then swap the adjusted card with the card at XA14. Adjust the second D/A converter card while it is installed in the XA15 slot. After adjustment, remove the card extender and leave the second card in the XA15 slot.

Table 5-2. D/A Converter Adjustments

SETUP	ADJUSTMENT POINT	PROPER INDICATION
LOCAL mode, verification test pattern displayed. Observe middle group of 9 parallel lines.	R18 (balance)	Adjust for best alignment of upper and lower halves of middle group.
LOCAL mode, verification test pattern displayed. Observe middle group of 9 parallel lines.	R19 (2nd bar B register) R24 (2nd bar A register)	Adjust for best parallelism and spacing (no bright lines, no dark lines).
Observe left group of 9 parallel lines.	R20 (left bar B register) R23 (left bar A register)	Adjust for best parallelism and spacing (no bright lines, no dark lines).
Observe right group of 9 parallel lines.	R21 (right bar B register) R22 (right bar A register)	Adjust for best parallelism and spacing (no bright lines, no dark lines).
Observe middle group.	R18 (balance)	Retouch as necessary.
Observe involute pattern at upper right of 3/4 screen box.	C25 (high speed) C26 (high speed) if installed.	Adjust for straightest lines in short vectors.

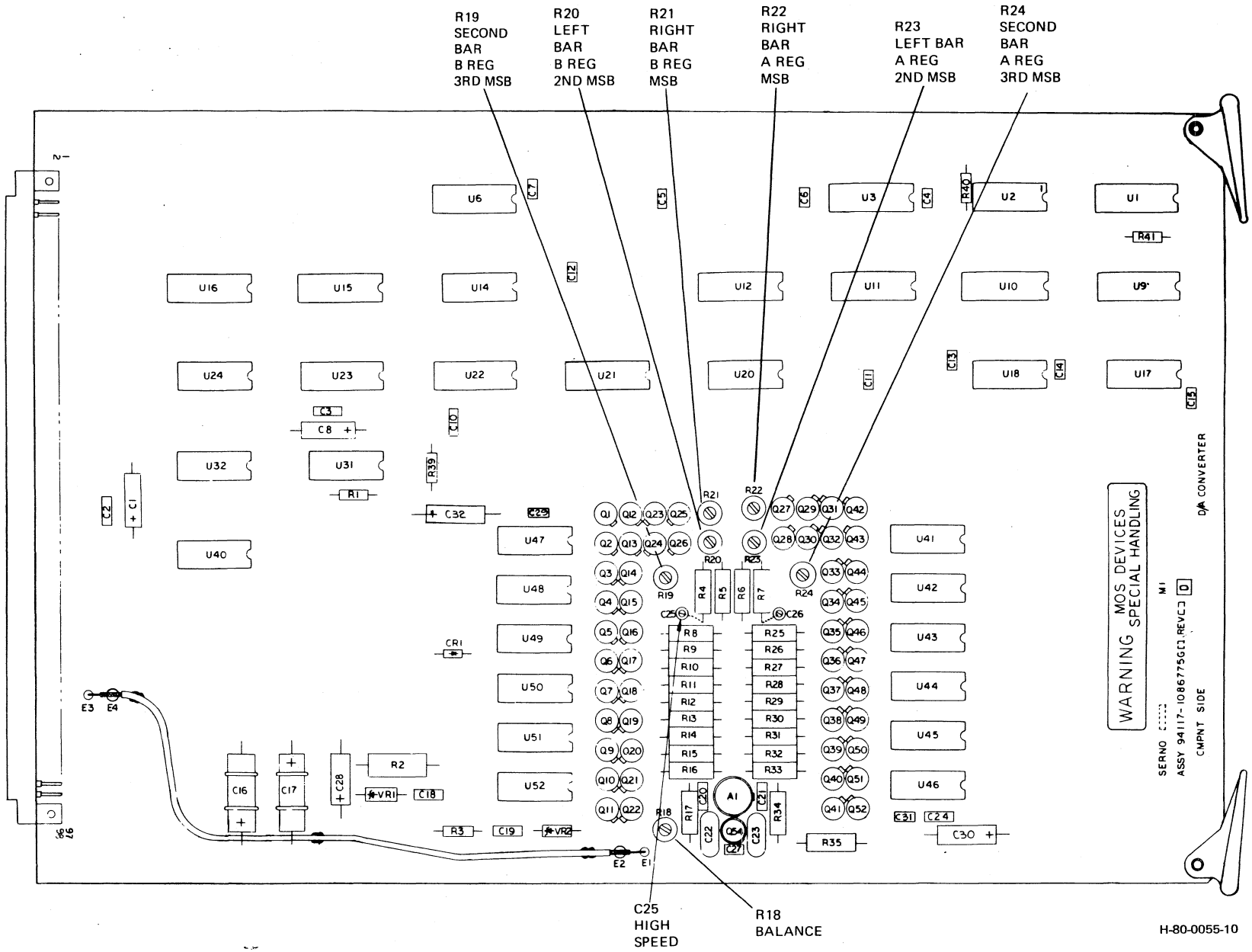


Figure 5-3. D/A Converter Card Adjustments

5.5.3 CHARACTER GENERATOR ADJUSTMENTS. The character generator has an oscillator rate adjustment capacitor and two character size adjustment potentiometers (see figure 5-5). Adjust character generator as follows.

Table 5-3. Character Generator Adjustments

SETUP	ADJUSTMENT POINT	PROPER INDICATION
LOCAL mode, verification test pattern displayed. Oscilloscope probe at U28-3 or U29-8 or U30-3. Ground at extender card pins 29/30/53/54.	C2 (oscillator rate)	Period = 75.0 nanoseconds
LOCAL mode, verification test pattern displayed. Observe characters E and M in lower left quadrant of 3/4-screen box. See figure 5-4.	R41 (X size), R45 (Y size)	Characters have 3:2 aspect ratio. Smallest character is 1/8 inch high, regardless of screen size. Other three characters have heights of 3/16, 1/4, and 3/8 inches. Adjust height of E and width of M to match dots as follows: Display indicator screen size (inches) — Dot No. (both axes) 20 — 1 16 — 2 14 — 3 12 — 4

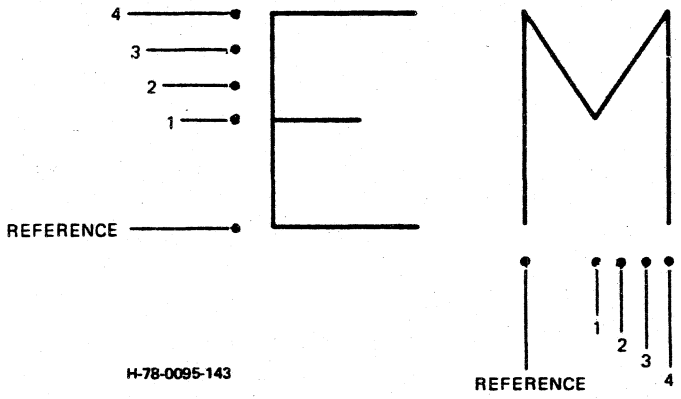


Figure 5-4. Terminal Verification Pattern, Character Height and Width Adjustment Gauges

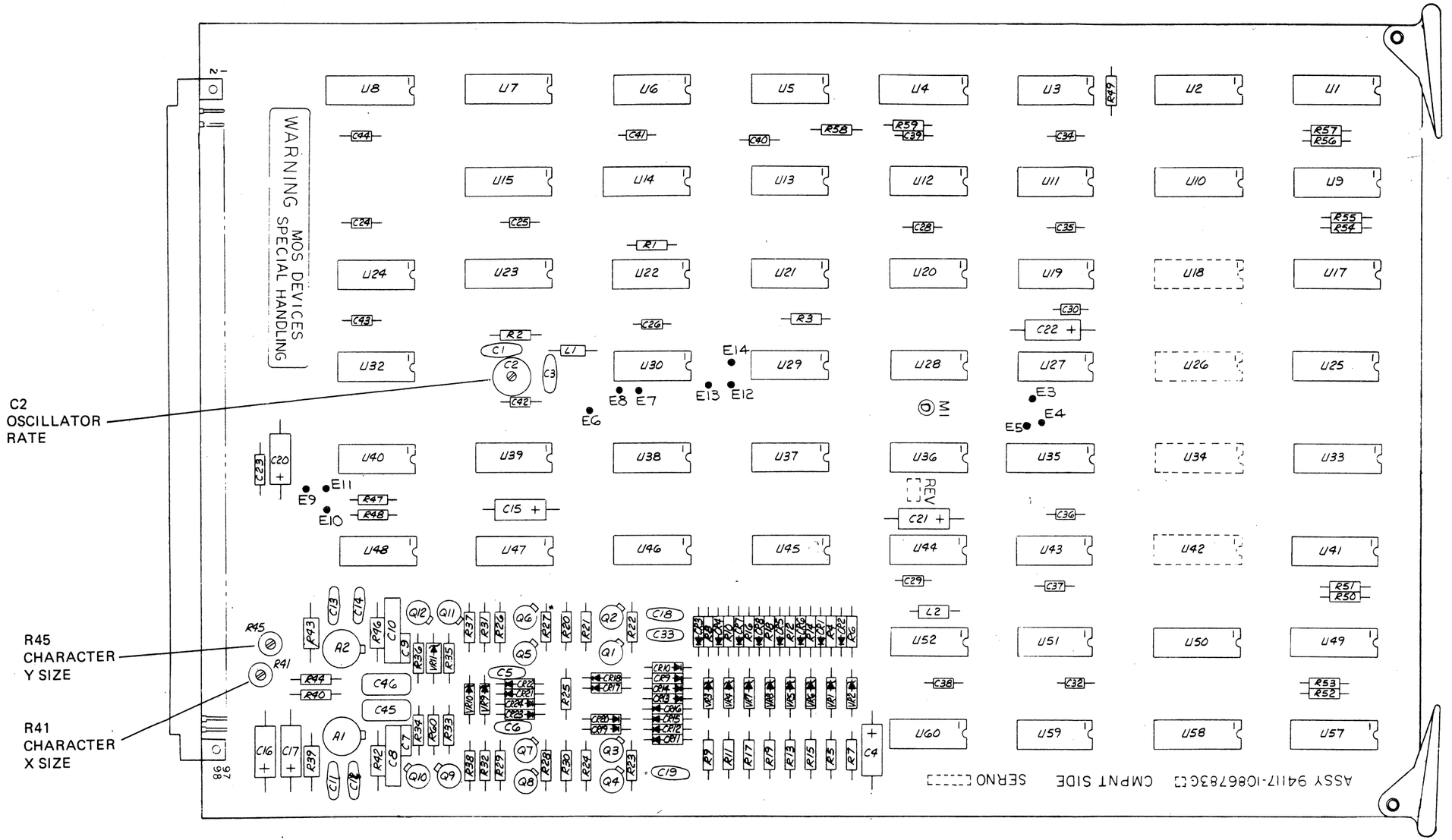


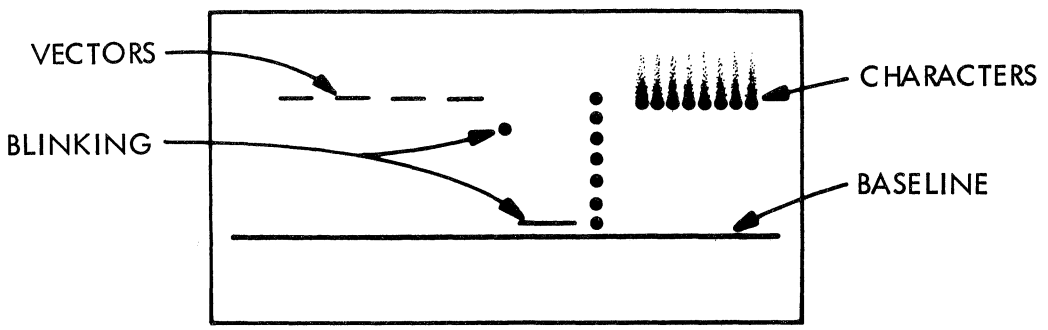
Figure 5-5. Character Generator Card Adjustments

5.5.4 OUTPUT CHANNEL ADJUSTMENTS

5.5.4.1 Monochrome Output Channel 1086771. The output channel contains eight adjustments for X, Y offset; X, Y, and Z gain; and blink rate (see figure 5-7). Adjust output channel as follows.

Table 5-4. Monochrome Output Channel Adjustments

SETUP	ADJUSTMENT POINT	PROPER INDICATION
LOCAL MONITOR mode (see paragraph 2.4.2). Type 157710G, press RETURN key. Digital voltmeter at E1 (display indicator connected to J1). Ground is pins 77/78/83/84/85/86/97/98 on card extender.	R44 (X offset)	0V ± 0.02V
Digital voltmeter at E5 (display indicator connected to J3).	R46 (Y offset)	0V ± 0.02V
Type 157720G, press RETURN key. Digital voltmeter at E1 (display indicator connected to J1).	R43 (X gain)	+4.95V ± 0.05V
Digital voltmeter at E5 (display indicator connected to J3).	R45 (Y gain)	Same as value for R43 adjustment, ± 0.001V
Type T, press RETURN key; verification test pattern displayed. Oscilloscope at E20 (display indicator connected to J5).	R118 (VECZ gain)	1.2V average for vectors; see figure 5-6.
	R117 (CHAZ gain)	1.1V average for characters; see figure 5-6.
Oscilloscope at U31-10.	R93 (blink rate)	Period = 250 milliseconds (4 Hz)
If auxiliary input is not used.	R116 (AUXZ gain)	Fully counterclockwise (minimum gain)



H-80-0055-12

Figure 5-6. Oscilloscope Display

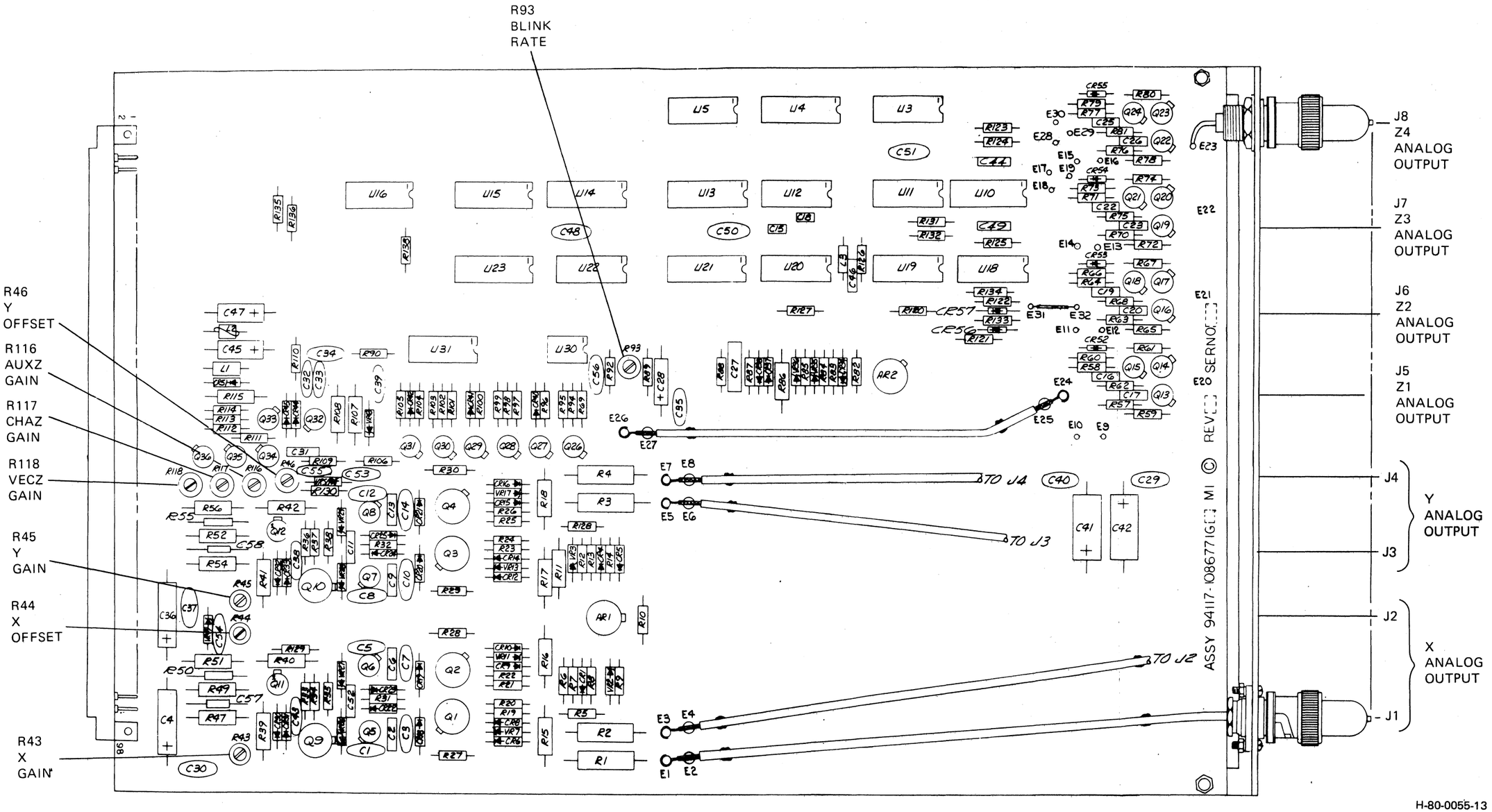


Figure 5-7. Monochrome Output Channel Adjustments

5.5.4.2 Color Output Channel 5977409. The color output channel contains nine adjustments for X and Y offset; X, Y, and Z gain; blink rate; and FBSY (function busy) pulse width. See figure 5-8. Adjust color output channel as follows.

Table 5-5. Color Output Channel Adjustments

SETUP	ADJUSTMENT POINT	PROPER INDICATION
LOCAL MONITOR mode (see paragraph 2.4.2). Type 157710G, press RETURN key. Digital voltmeter at E3 (display indicator connected to J1). Ground is pins 77/78/83/84/85/86/98/98 on card extender.	R7 (X offset)	0V ± 0.02V
Digital voltmeter at E7 (display indicator connected to J5).	R36 (Y offset)	0V ± 0.02V
Type 157720G, press RETURN key. Digital voltmeter at E3 (display indicator connected to J1).	R8 (X gain)	+4.95V ± 0.05V
Digital voltmeter at E7 (display indicator connected to J5).	R37 (Y gain)	Same as value for R8 adjustment, ± 0.001V
Type T, press RETURN key; verification test pattern displayed. Oscilloscope at E11 (display indicator connected to J9).	R70 (VECZ gain)	1.2V average for vectors; see figure 5-6.
	R71 (CHAZ gain)	1.1V average for characters; see figure 5-6.
Oscilloscope at U34-2.	R81 (blink rate)	Period = 250 milliseconds (4 Hz)
If auxiliary input is not used.	R72 (AUXZ gain)	Fully counterclockwise (minimum gain)
LOCAL MONITOR mode (see paragraph 2.4.2). From the keyboard, load the following routine starting at address 2000:		

Table 5-5. Color Output Channel Adjustments (Cont)

SETUP	ADJUSTMENT POINT	PROPER INDICATION
2000 6010 4000 6010 2002 6010 1012 6010 0452 1000 2000		
Oscilloscope at E11 (display indicator connected to J9).		Color switching signal is a single negative pulse approx -1.6V (-1.0V minimum).
Oscilloscope at E12 (display indicator connected to J10).		Color switching signal is two negative pulses approx -1.6V (-1.0V minimum).
Oscilloscope at E13 (display indicator connected to J11).		Color switching signal is three negative pulses approx -1.6V (-1.0V minimum).
Oscilloscope at E14 (display indicator connected to J12).		Color switching signal is four negative pulses approx -1.6V (-1.0V minimum).
From the keyboard, load the following routine starting at address 2500: 2500 7000 6010 4000 1000 2500		
Oscilloscope at E1 or E2.	R92 (FBSY pulse width)	Pulse width = 250 us minimum.
Type T, press RETURN key; verification test pattern displayed. Observe pattern.	R92 (FBSY pulse width)	No smearing of colors in full-screen box.

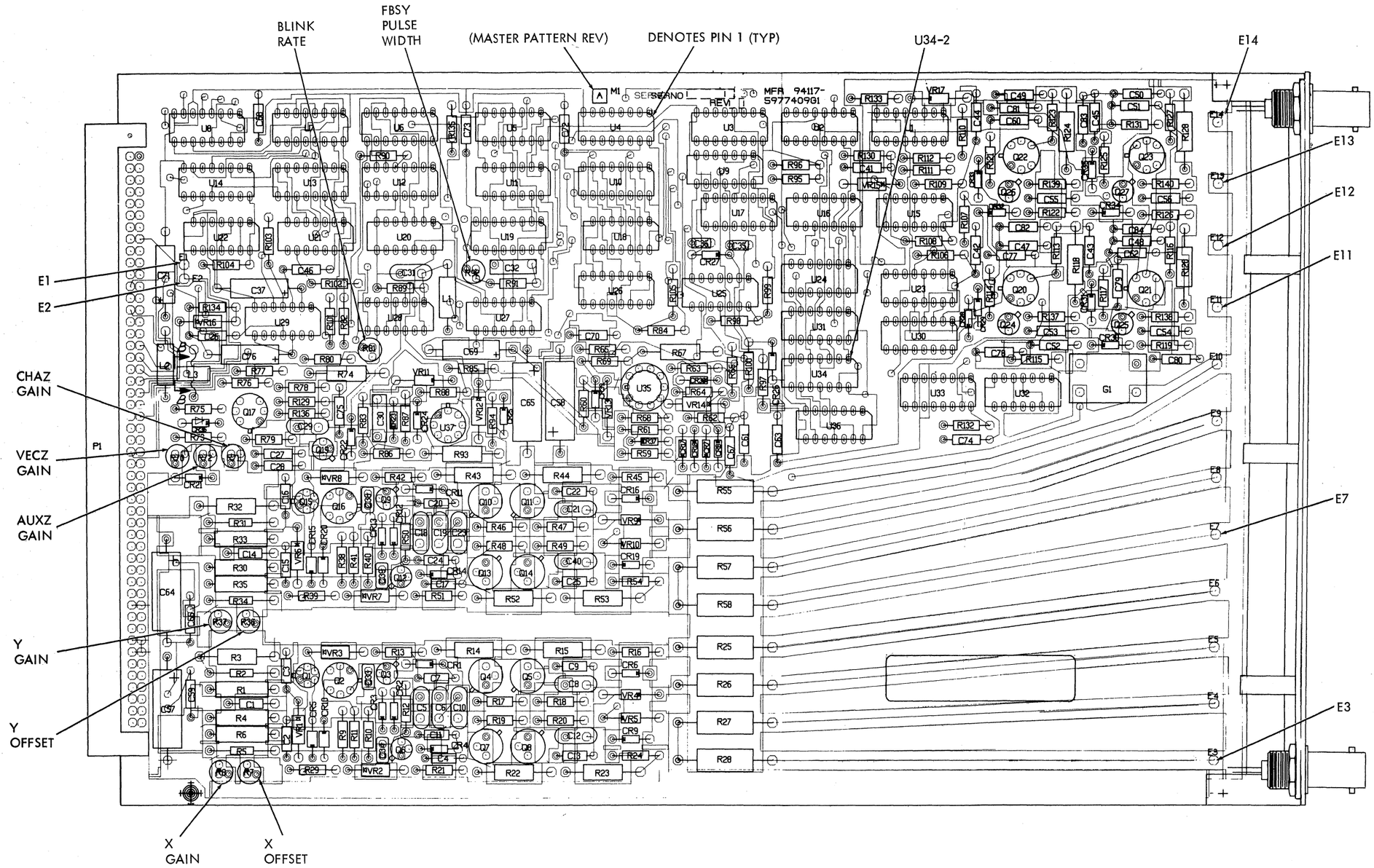


Figure 5-8. Color Output Channel Adjustments

5.6 REPAIR

Repair consists of replacing circuit cards or chassis-mounted electrical assemblies suspected of being faulty, based on the troubleshooting analysis (figure 5-1).

CAUTION

Always turn off terminal controller before removing or installing any circuit card. Always turn down brightness of display indicator before removing or installing any circuit card in terminal controller.

Always turn off terminal controller and pull power plug before removing any chassis-mounted component.

5.6.1 CIRCUIT CARD REPLACEMENT. To remove a circuit card assembly, grasp the two card extractor handles, exert outward pressure to disengage the card from its connector, and pull straight out of card cage.

Before installing a circuit card assembly, verify the part number of the card. Insert the card (component side to the left) into its slot in the card cage. Engage it with its connector by exerting firm inward pressure.

5.6.2 CHASSIS-MOUNTED COMPONENTS. Chassis-mounted assemblies are secured with standard mounting hardware, and can be removed and replaced using common hand tools.

Refer to the appropriate separate manual for maintenance of the terminal controller power supply.

5.6.3 SPECIAL HANDLING FOR MOS DEVICES. MOS devices are subject to damage caused by static charges. Assemblies that contain MOS devices are the D/A converters and character generator. When not installed in the card cage, these assemblies should be stored in black Velostat bags with the MOS warning statement printed on the outside of the bag.

CAUTION

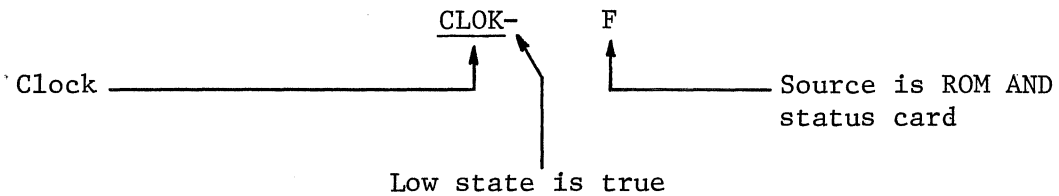
Always handle these cards only by the card extractors or by the connector. Avoid touching the card components or the printed circuit.

APPENDIX A

MNEMONICS

A-1. GENERAL.

This appendix contains definitions and descriptions of the signal mnemonics used in the terminal controller. The terminal controller signal mnemonics consist of six characters (figure A-1). The first four are an alphanumeric abbreviation of the signal name. The fifth character is a sign (+ or -) that indicates the true state (high or low) of the signal. The final character is an alphabetic code that identifies the source of the signal. Table A-1 lists the alphabetic codes that identify the sources.



NOTE

Signals with a "B" suffix are controller bus signals common to all bus modules. The source at any time is the module having bus control or being accessed during a terminal controller routine.

Figure A-1. Illustrative Signal Mnemonic

A-2. MNEMONICS DICTIONARY.

Table A-2 lists and defines all signal mnemonics in alphanumerical order.

Table A-1. Signal Source Codes

SOURCE CODE	SOURCE
A	Digital-to-analog converter (X or Y)*
B	Processor bus signal
C	Character generator
D	Display processor
E	Ramp generator or ramp conic generator
F	ROM and status
G	Graphic controller
I	Parallel interface
M	Read/write memory
O	Output channel
P	Radar sweep
S	Multiport Serial Interface
T	Coordinate converter
R	Return (twisted pair)
X	Multiple Source

*D/A converters are identical on a pin-for-pin basis. Destinations of signals differ as governed by backplane wiring.

Table A-2. Mnemonics Dictionary

MNEMONIC	DEFINITION
ADRV-B	Address Valid
AD00-B to AD17-B	Address bits 00 to 17
ANALOG Z1 to Z4 OUTPUTS	Output channel card Z-axis outputs (J5 to J8)
ARET-	Analog return
ATTN 1 (±) and ATTN 2 (±)	Parallel interface card (J2) attention bits from host computer
AUXX-	Auxiliary X input to output channel card (not wired in backplane)
AUXY-	Auxiliary Y input to output channel card (not wired in backplane)
AUXZ+	Auxiliary Z input to output channel card (not wired in backplane)
BLNK	Blank output from output channel card (not wired in backplane)
BTOM-M	Bus timeout
BUSB-B	Bus busy
BYTE-B	Byte (upper or lower word)
CARR+	Multiport card port 1 (J2) data carrier detect from modem
CARX+A	Carry X
CARY+A	Carry Y
CGND	Chassis ground
CHAX-C	Character generator X output
CHAY-C	Character generator Y output
CHAZ-C	Character generator Z output
CHEN+(C)	Character enable
CLOK-F	10 MHz master clock

Table A-2. Mnemonics Dictionary (Cont)

MNEMONIC	DEFINITION
CLTS+	Multiport card port 1 (J2 clear-to-send input from modem
DACX-A	D/A converter X output
DACY-A	D/A converter Y output
DA00-B to DA15-B	Controller bus data bits 00 to 15
DB00-G to DB11-G	Graphic bus data bits 00 to 11
DEV0-B to DEV2-B	Device code bits
DGND	Multiport card port 1 (J2) data ground
DPRN-D	Display processor run (LED signal)
DRDY-G	Data terminal ready
DRET-	Digital return
DSRY+	Multiport card port 1 (J2) data set ready input from modem
DTRY+	Multiport card port 1 (J2) data ready output
EXTR-O	External reset input to output channel card (not wired in backplane)
FBSY-X	Function busy
FRDY-G	Function ready
GCRE-G	Graphic controller request enable (true = graphic controller halted)
GRAI+B	Grant input (bus grant)
GRAO+B	Grant output (bus grant)
HALT-G	Halt
IADV-B	Interrupt address valid
ICTL(±)	Parallel interface card (J2) input control line to host computer
ID00(±) to ID15(±)	Parallel interface card (J3) input data bits to host computer

Table A-2. Mnemonics Dictionary (Cont)

MNEMONIC	DEFINITION
IENA-D	Interrupt enable
IMR(±)	Input message request from parallel interface card (J3) to host (spare input 2)
INL5-B to INL7-B	Interrupt levels 5 to 7
IREQ-D	Interrupt request pulse
LINE+	3V rms AC input to output channel card from chassis transformer
LINK-G	Link interrupt
LOCA-B	Local (operator control) mode enable
LX00+A to LX10+A	X move length bits 00 to 10
LY00+A to LY10+A	Y move length bits 00 to 10
MEMA-B	Memory acknowledge
NDRY(±)	New data ready, parallel interface card (J3) to host computer
NULL-C	Null
N15V-	-15V supply voltage
OCTL(±)	Parallel interface (J2) output control line from host computer
ODR(±)	Output data ready, parallel interface (J2) to host computer
ODXX+F	Output data bits from ROM and status card serial interface port
OD00(±) to OD15(±)	Parallel interface card (J2) output data bits from host computer
OFLW-A	Overflow
OMR(±)	Output message request parallel interface card J2 to host computer (spare input 1)
OVCK-E	Overflow interrupt clock
OWR(±)	Output word request, parallel interface card (J2) to host computer

Table A-2. Mnemonics Dictionary (Cont)

MNEMONIC	DEFINITION
PEN1+0	PHOTOPEN 1 strike enable
PEN2+0	PHOTOPEN 2 strike enable
PPDE-F	PHOTOPEN delay enable
PPDT-F	PHOTOPEN detect interrupt from ROM and status card
PDP1-0	PHOTOPEN 1 detect
PDP2-0	PHOTOPEN 2 detect
PPL1-	PHOTOPEN light 1 input to output channel card (not wired in backplane)
PPL2-	PHOTOPEN light 2 input to output channel card (not wired in backplane)
P05V+	+5V supply voltage
P15V+	+15V supply voltage
RAMP+E	Ramp generator card analog output
RDAT+	ROM and status card J2 I/O receive data control line input
RDAI	Multiport card port 1 (J2 or J3) receive input data
RDEN±	Receive data enable (ROM and status I/O connector J2)
REFN-E	Negative reference to D/A converters
REFP+E	Positive reference to D/A converters
REN1-	Multiport card port 1 (J3) reader enable
REN2-	Multiport card port 2 (J4) reader enable
REN3-	Multiport card port 3 (J5) reader enable
REN4-	Multiport card port 4 (J6) reader enable
REST-B	Bus reset

Table A-2. Mnemonics Dictionary (Cont)

MNEMONIC	DEFINITION
RING+	Multiport card port 1 (J2) ring indicator RS-232C from modem input (host initialize)
RQTS+	Multiport card port 1 (J2) request to send
RRTN1	Multiport card port 1 (J3) receive input data return
RSCK+	Multiport card port 1 (J2) receive clock
RTCK-O	Real-time clock (60 Hz)
SLDP-G	Select display parameter register
SL60+O	Select 60 Hz input (normally open, not wired in backplane)
STDC-G	Set character register
STDP-G	Set display parameter register
STDX-G	Set display X position register
STDY-G	Set display Y position register
STDZ-G	Set D display register
SYNC-O	Frame sync
SYST-B	System (host control) mode enable
TOGL-E	Toggle (ramp toggle between A and B registers)
TORN-O	Turn-on (power up initialize)
TSCK+	Multiport port 1 (J2) external transmit clock
TXCO+	Multiport card port 1 (J2) transmit clock output
VECZ+E	Ramp generator Z-Axis output
VPBY+E	Vector position busy
VPIZ-G	Vector position initialize
VPNL+E	Vector position null
VPST+G and VPST-G	Vector position start

Table A-2. Mnemonics Dictionary (Cont)

MNEMONIC	DEFINITION
VPS1 + G	Vector position select 1
VPS2 + G	Vector position select 2
WRIT-B	Write (memory write or read control)
XMIT+	ROM and status card J2 I/O serial transmit data output
XMIT1-	Multiport port 1 (J3) transmit output data
XRTN1	Multiport port 1 (J3) transmit output return
X232-	Multiport port 1 (J2) data RS-232C level transmit data signal
50KB-F	50 kilobaud (clock)

A-3. REGISTER AND BUS BIT MNEMONICS.

Register and bus mnemonics use the lowest numeric to designate the least significant bit (LSB) and highest numeric to designate the most significant bit (MSB). For example, in the terminal controller data bus:

DA00-B = LSB

DA15-B = MSB

A-4. POWER SUPPLY MNEMONICS.

Table A-3 lists the mnemonics used for power supply voltages and grounds. These are applied in common to all terminal controller cards on a pin-for-pin basis.

Table A-3. Power Supply Mnemonics

MNEMONIC	DESCRIPTION
P05V+	+5 Vdc
P15V+	+15 Vdc
N15V-	-15 Vdc
ARET-	Analog ground
DRET-	Digital ground
CGND	Chassis ground

A-5. CARD SLOT PIN SIGNALS.

Table A-4 lists the common controller bus signals at the pins of card slots XA1 to XA8. Tables A-5 through A-10 list the signals at the pins of card slots XA9, XA10, XA11, XA13, XA14, XA15, and XA16. Each card slot contains a unique circuit card. Card slot XA17 is an unwired spare slot available for expansion.

Table A-4. Card Slots XA1 to XA8, Common Controller Bus Signals

SIGNAL	PIN		SIGNAL
DRET-	2	1	DRET-
INL5-B	4	3	DEV3-B
INL7-B	6	5	INL6-B
IENA-D	8	7	IREQ-D
DEV0-B	10	9	IADV-B
DEV2-B	12	11	DEV1-B
DA01-B	14	13	DA00-B
DA03-B	16	15	DA02-B
DA05-B	18	17	DA04-B
DA07-B	20	19	DA06-B
DA09-B	22	21	DA08-B
DA11-B	24	23	DA10-B
DA13-B	26	25	DA12-B
DA15-B	28	27	DA14-B
DRET-	30	29	DRET-
	32	31	CLOK-F
	34	33	BUSB-B
GRAI+B*	36	35	GRAO+B*
ADRV-B	38	37	WRIT-B
BYTE-B	40	39	MEMA-B
BTOM-M	42	41	REST-B
LOCA-B	44	43	SYST-B
	46	45	TORN-O
	48	47	DPRN-D

*Note: All connections are pin-to-pin except GRAO+B (grant output) and GRAI+B (grant input). GRAO+B from XA1 is GRAI+B at XA2; GRAO+B from XA2 is GRAI+B at XA3; etc. The Grants assign highest bus priority to XA1 and lowest to XA10 (Graphic controller, listed separately).

Table A-4. Card Slots XA1 to XA8, Common Controller Bus Signals (Cont)

SIGNAL	PIN		SIGNAL
50KB-F	50	49	
	52	51	
DRET-	54	53	DRET-
P05V+	56	55	P05V+
AD01-B	58	57	AD00-B
AD03-B	60	59	AD02-B
AD05-B	62	61	AD04-B
AD07-B	64	63	AD06-B
AD09-B	66	65	AD08-B
AD11-B	68	67	AD10-B
AD13-B	70	69	AD12-B
AD15-B	72	71	AD14-B
AD17-B	74	73	AD16-E
	76	75	
ARET-	78	77	ARET-
	80	79	
	82	81	
	84	83	
	86	85	
	88	87	
	90	89	
CGND	92	91	CGND
N15V-	94	93	N15V-
P15V+	96	95	P15V+
ARET-	98	97	ARET-

Table A-5. ROM and Status Card Slot XA9 Signals

SIGNAL	PIN		SIGNAL
DRET-	2	1	DRET-
INL5-B	4	3	DEV3-B
INL7-B	6	5	INL6-B
IENA-D	8	7	IREQ-D
(DEV0-B)	10	9	IADV-B
(DEV2-B)	12	11	DEV1-B
DA01-B	14	13	DA00-B
DA03-B	16	15	DA02-B
DA05-B	18	17	DA04-B
DA07-B	20	19	DA06-B
DA09-B	22	21	DA08-B
DA11-B	24	23	DA10-B
DA13-B	26	25	DA12-B
DA15-B	28	27	DA14-B
DRET-	30	29	DRET-
	32	31	CLOK-F
	34	33	BUSB-B
GRAI+B	36	35	GRAO+B
ADRV-B	38	37	WRIT-B
BYTE-B	40	39	MEMA-B
(BOTM-M)	42	41	REST-B
(LOCA-B)	44	43	(SYST-B)
	46	45	(TORN-O)
	48	47	(DPRN-D)

( ) Signal present at backplane, not used by circuit.

Table A-5. ROM and Status Card Slot XA9 Signals (Cont)

SIGNAL	PIN		SIGNAL
50KB-F	50	49	OFLW-A
RTCK-O	52	51	PPDE-F
DRET-	54	53	DRET-
P05V+	56	55	P05V+
AD01-B	58	57	AD00-B
AD03-B	60	59	AD02-B
AD05-B	62	61	AD04-B
AD07-B	64	63	AD06-B
AD09-B	66	65	AD08-B
AD11-B	68	67	AD10-B
AD13-B	70	69	AD12-B
AD15-B	72	71	AD14-B
AD17-B	74	73	AD16-B
	76	75	GCRE-G
ARET-	78	77	ARET-
	80	79	BYTE-G
PPS1-	82	81	PPS2-
PEN1+O	84	83	HALT-G
PEN2+O	86	85	VPNL+E
PPDT-F	88	87	PPD2-O
LINK-G	90	89	PPD1-O
(CGND)	92	91	(CGND)
N15V-	94	93	N15V-
P15V+	96	95	P15V+
ARET-	98	97	ARET-

( ) Signal present at backplane, not used by circuit.

Table A-6. Graphic Controller Card Slot XA10 Signals

SIGNAL	PIN		SIGNAL
DB01-G	2	1	DB00-G
DB03-G	4	3	DB02-G
DB05-G	6	5	DB04-G
DB07-F	8	7	DB06-G
DB09-G	10	9	DB08-G
DB11-G	12	11	DB10-G
DA01-B	14	13	DA00-B
DA03-B	16	15	DA02-B
DA05-B	18	17	DA04-B
DA07-B	20	19	DA06-B
DA09-B	22	21	DA08-B
DA11-B	24	23	DA10-B
DA13-B	26	25	DA12-B
DA15-B	28	27	DA14-B
DRET-	30	29	DRET-
TOGL-E	32	31	CLOK-F
SLDP-G	34	33	BUSB-B
GRAI+B	36	35	
ADRV-B	38	37	WRIT-B
[PRET-]	40	39	MEMA-B
[SPBY-]	42	41	REST-B
[AXBY-]	44	43	FBSY-X
VPS2+G	46	45	(TORN-0)
VPST-G	48	47	VPS1+G

( ) Signal present at backplane, not used by circuit.
[ ] Provision for accepting input signal; not wired in backplane.

Table A-6. Graphic Controller Card Slot XA10 Signals (Cont)

SIGNAL	PIN		SIGNAL
GCRE+G	50	49	
SYNC-O	52	51	PPDE-F
DRET-	54	53	DRET-
P05V+	56	55	P05V+
AD01-B	58	57	AD00-B
AD03-B	60	59	AD02-B
AD05-B	62	61	AD04-B
AD07-B	64	63	AD06-B
AD09-B	66	65	AD08-B
AD11-B	68	67	AD10-B
AD13-B	70	69	AD12-B
AD15-B	72	71	AD14-B
AD17-B	74	73	AD16-B
NULL-C	76	75	CGRE-G
ARET-	78	77	ARET-
VPIZ-G	80	79	BYTE-G
FRDY-G	82	81	DRDY-G
STDX-G	84	83	HALT-G
STDC-G	86	85	STDY-G
PPDT-F	88	87	STDZ-G
LINK-G	90	89	STDP-G
[STKX-G]	92	91	[STKY-G]
N15V-	94	93	N15V-
P15V+	96	95	P15V+
ARET-	98	97	ARET-

[ ] Provision for accepting input signal; not wired in backplane.

Table A-7. Character Generator Card Slot XA11 Signals

SIGNAL	PIN		SIGNAL
DB01-G	2	1	DB00-G
DB03-G	4	3	DB02-G
DB05-G	6	5	DB04-G
(DB07-G)	8	7	DB06-G
DB09-G	10	9	(DB08-G)
(DB11-G)	12	11	DB10-G
(STDZ-G)	14	13	
STDC-G	16	15	STDP-G
	18	17	
	20	19	NULL-C
	22	21	
	24	23	
	26	25	
(FRDY-G)	28	27	(DRDY-G)
DRET-	30	29	DRET-
(TOGL-E)	32	31	
SLDP-G	34	33	
REST-B	36	35	
	38	37	
	40	39	
	42	41	(OFLW-A)
	44	43	FBSY-X
	46	45	TORN-O
	48	47	

( ) Signal present at backplane; not used by circuit.

Table A-7. Character Generator Card Slot XA11 Signals (Cont)

SIGNAL	PIN		SIGNAL
	50	49	
	52	51	
DRET-	54	53	DRET-
P05V+	56	55	P05V+
	58	57	
	60	59	
	62	61	
CHAZ+C	64	63	
	66	65	
	68	67	
	70	69	
	72	71	
	74	73	
	76	75	
ARET-	78	77	ARET-
CHAY-C	80	79	
	82	81	
	84	83	
	86	85	
	88	87	
CHAX-C	90	89	
	92	91	
N15V-	94	93	N15V-
P15V+	96	95	P15V+
ARET-	98	97	ARET-

Table A-8. Ramp Generator Card Slot XA13 Signals

SIGNAL	PIN		SIGNAL
(DB01-G)	2	1	(DB00-G)
DB03-G	4	3	(DB02-G)
(DB05-G)	6	5	DB04-G
(DB07-G)	8	7	(DB06-G)
DB09-G	10	9	(DB08-G)
DB11-G	12	11	DB10-G
STDZ-G	14	13	
	16	15	STDP-G
	18	17	
	20	19	
	22	21	
	24	23	
	26	25	
(FRDY-G)	28	27	(DRDY-G)
DRET-	30	29	DRET-
TOGL-E	32	31	
SLDP-G	34	33	
	36	35	
VPIZ-G	38	37	
CIRL-E	40	39	VECZ+E
VPNL+E	42	41	OFLW-A
VPBY+E	44	43	FBSY-X
VPS2+G	46	45	TORN-O
VPST-G	48	47	VPS1+G

( ) Signal present at backplane; not used by circuit.

Table A-8. Ramp Generator Card Slot XA13 Signals (Cont)

SIGNAL	PIN		SIGNAL
CARX+A	50	49	CARY+A
LX00+A	52	51	LY00+A
DRET-	54	53	DRET-
P05V+	56	55	P05V+
LX01+A	58	57	LY01+A
LX02+A	60	59	LY02+A
LX03+A	62	61	LY03+A
LX04+A	64	63	LY04+A
LX05+A	66	65	LY05+A
LX06+A	68	67	LY06+A
LX07+A	70	69	LY07+A
LX08+A	72	71	LY08+A
LX09+A	74	73	LY09+A
LX10+A	76	75	LY10+A
ARET-	78	77	ARET-
RAMP+E	80	79	RAMP+E
REFP+E	82	81	
REFN-E	84	83	
	86	85	
	88	87	
	90	89	
	92	91	
N15V-	94	93	N15V-
P15V+	96	95	P15V+
ARET-	98	97	ARET-

Table A-9. D/A Converters Card Slots XA14, XA15 Signals

SIGNAL	PIN		SIGNAL
DB01-G	2	1	DB00-G
DB03-G	4	3	DB02-G
DB05-G	6	5	DB04-G
DB07-G	8	7	DB06-G
DB09-G	10	9	DB08-G
DB11-G	12	11	DB10-G
(STDZ-G)	14	13	STDX-G, STDY-G
	16	15	(STDP-G)
	18	17	
	20	19	
	22	21	
	24	23	
	26	25	
(FRDY-G)	28	27	(DRDY-G)
DRET-	30	29	DRET-
TOGL-E	32	31	
(SLDP-G)	34	33	
	36	35	
	38	37	
CIRL-E	40	39	
VPNL+E	42	41	OFLW-A
VPBY+E	44	43	(FBSY-X)
	46	45	(TORN-O)
	48	47	

( ) Signal present at backplane; not used by circuit.

Table A-9. D/A Converters Card Slots XA14, XA15 Signals (Cont)

SIGNAL	PIN		SIGNAL
	50	49	CARX+A, CARY+A
	52	51	LX00+A, LY00+A
DRET-	54	53	DRET-
P05V+	56	55	P05V+
	58	57	LX01+A, LY01+A
	60	59	LX02+A, LY02+A
	62	61	LX03+A, LY03+A
	64	63	LX04+A, LY04+A
	66	65	LX05+A, LY05+A
	68	67	LX06+A, LY06+A
	70	69	LX07+A, LY07+A
	72	71	LX08+A, LY08+A
	74	73	LX09+A, LY09+A
[LX11+A, LY11+A]	76	75	LX10+A, LY10+A
ARET-	78	77	ARET-
RAMP+E	80	79	
REFP+E	82	81	
REFN-E	84	83	
	86	85	
	88	87	DACX-A, DACY-A
	90	89	
	92	91	
N15V-	94	93	N15V-
P15V+	96	95	P15V+
ARET-	98	97	ARET-

[ ] Signal output present on card; not wired in backplane.

Table A-10. Output Channel Card Slot XA16 Signals

SIGNAL	PIN		SIGNAL
DB01-G	2	1	DB00-G
DB03-G	4	3	DB02-G
DB05-G	6	5	DB04-G
DB07-G	8	7	DB06-G
DB09-G	10	9	DB08-G
DB11-G	12	11	DB10-G
STDZ-G	14	13	
	16	15	STDP-G
	18	17	
	20	19	
PPL1-	22	21	PPL2-
PPD1-O	24	23	PPD2-O
PEN1+O	26	25	PEN2+O
(FRDY-G)	28	27	(DRDY-G)
DRET-	30	29	DRET-
(TOGL-E)	32	31	[SL60+0]
SLDP-G	34	33	LINE+
	36	35	[EXTR-]
	38	37	SYNC-O
	40	39	[BLNK-O]
	42	41	(OFLW-A)
	44	43	(FBSY-X)
	46	45	TORN-O

( ) Signal present at backplane; not used by circuit.
[ ] Signal output present on card; not wired in backplane.

Table A-10. Output Channel Card Slot XA16 Signals (Cont)

SIGNAL	PIN		SIGNAL
	48	47	
	50	49	
RTCK-O	52	51	
DRET-	54	53	DRET-
P05V+	56	55	P05V+
	58	57	
VECZ+E	60	59	
	62	61	
CHAZ+C	64	63	
	66	65	
[AUXZ+]	68	67	
	70	69	
	72	71	
	74	73	
	76	75	
ARET-	78	77	ARET-
CHAY-C	80	79	[AUXY-]
DACY-A	82	81	
	84	83	
	86	85	
DACX-A	88	87	[AUXX-]
CHAX-C	90	89	
	92	91	

[ ] Signal output present on card; not wired in backplane.

Table A-10. Output Channel Card Slot XA16 Signals (Cont)

SIGNAL	PIN		SIGNAL
N15V-	94	93	N15V-
P15V+	96	95	P15V+
ARET-	98	97	ARET-

APPENDIX B

CONNECTIONS TO HOST COMPUTER

Tables B-1 through B-4 list the signals at the host-computer connectors of the parallel interface card.

Table B-1. Connector J2, Inputs to Host Computer

CARD PIN	SIGNAL NAME	DESCRIPTION
37	OWR(±) (output word received)	During single-word output transfer, goes active after display processor has read output data and sent new status word to parallel interface with bit ST05 set. During DMA output transfer, goes active when parallel interface advances from state 2 to state 3. In both cases, clears when host computer terminates OCTL±.
39	OMR(±) (output message request)	This is a spare signal, to which may be assigned any applicable timing or condition function. It goes active when the display processor writes active STØØ into the parallel interface status register. It goes inactive when the display processor writes inactive STØØ or on processor bus reset.
43	ODR(±) (output data received)	Goes active for approximately 150 nanoseconds after the parallel interface activates OWR(±).
33	TEST1-OUT	Does not ordinarily go to host computer. If test jumper cable is used, becomes TEST1-IN signal at J3-33. Signal is the complement of OMR(±).

Table B-2. Connector J2, Outputs from Host Computer

CARD PIN	SIGNAL NAME	DESCRIPTION
1 thru 32	ODnn(±) (output data bits ØØ thru 15; odd pins = signal, even pins = ground	16-bit output data word. Available to parallel interface when OCTL(±) is active. Must remain stable until parallel interface sends OWR(±) or ODR(±).

Table B-2. Connector J2, Outputs from Host Computer (Cont)

CARD PIN	SIGNAL NAME	DESCRIPTION
35	ATN1(±) (attention #1)	This is a spare signal and may be programmed as required for handshaking. Display processor reads the value of this signal as status bit STØ9.
41	OCTL(±) (output control)	Host computer sets this signal active after placing ODnn(±) on output data lines. Must remain stable until parallel interface sends OWR(±) or ODR(±).
47	INIT(±) (initialize)	Directs GRAPHIC 7 display processor to initialize all circuits, clearing all in-process activities and stored data. Display processor generates REST-B signal and sends 4-word XX message to host.
49	TEST2-IN	Does not ordinarily come from host computer. See TEST2-OUT from connector J3 (table B-3).

Table B-3. Connector J3, Inputs to Host Computer

CARD PIN	SIGNAL NAME	DESCRIPTION
1 thru 32	IDnn(±) (input data bits ØØ thru 15; odd pins = signal, even pins = ground	16-bit input data word. Available to host computer when IWR(±) is active. Remains stable until host computer sends ICTL(±).
35	IMR(±) (input message request)	This is a spare signal and may be assigned any timing or condition function. Goes active when display processor sets status bit ST12. Goes inactive when display processor resets ST12 or on processor bus reset.
41	IWR(±) (input word request)	During single word input transfer, goes high when display processor sets bit ST13 active (after placing IDnn(±) on input data lines). During DMA input transfer, goes active when parallel interface advances from state 2 to state 3. Terminates when host computer sends ICTL(±).
45	NDRY(±) (new data ready)	Goes active for approximately 150 nano-seconds after host computer activates ICTL(±).

Table B-3. Connector J3, Inputs to Host Computer (Cont)

CARD PIN	SIGNAL NAME	DESCRIPTION
49	TEST2-OUT	Does not ordinarily go to host computer. If test jumper cable is used, becomes TEST2-IN signal at J2-49. Signal is the complement of status bit ST12.

Table B-4. Connector J3, Outputs from Host Computer

CARD PIN	SIGNAL NAME	DESCRIPTION
33	TEST1-IN	See TEST1-OUT at J2-33 (table B-1). When this signal is low, the parallel interface cannot generate NDRY and cannot clear IWR(±).
37	ICTL(±) (input control)	Host computer sets this signal active to acknowledge receipt of IWR(±). Signal remains active until parallel interface terminates IWR(±) or sends NDRY(±).
39	ATN2(±) (attention #2)	This is a spare signal and may be programmed as required for handshaking. Display processor reads the value of this signal as status bit ST1Ø.

APPENDIX C

RELATED PUBLICATIONS

MANUAL NO.*	TITLE
	GRAPHIC 7 SYSTEM AND SOFTWARE MANUALS
GA-76-165	GRAPHIC 7 Technical Description
GA-77-274	GRAPHIC 7 Acceptance Test Procedure
GA-77-419	(GCP) Programmer's Reference Manual
GA-77-300	GCP Source Listings (Release 2)
H-78-0452	GCP Source Listings (Release 4)
H-79-0348	GCP+ Programmer's Reference Manual
H-79-0356	GCP+ Source Listings
H-78-0047	GSS-4 User's Manual
H-78-0111	GSS-4 Version 1.1 Program Listings
H-79-0347	Fortran Support Package User's Manual
H-78-0447	Multitask User's Manual
H-79-0267	Multitask Acceptance Test Procedure
H-79-0007	Monitor Software Version 1.0 User's Manual
	TERMINAL CONTROLLER MANUALS
H-80-0055	Model 7709 Terminal Controller Maintenance Manual
H-78-0096	Terminal Controller Maintenance Manual, Volume II, Diagrams and Parts Lists
H-80-0087	Terminal Controller Power Supply Model MM23-E0647/115
	TERMINAL CONTROLLER OPTIONS MANUALS
H-79-0357	GRAPHIC 7 Options Reference Manual
H-78-0060	Model 5843 Ramp/Conic Generator Technical Manual

* - This column lists the manual's basic number. Revisions are indicated on the cover of the manual by a letter following this basic number.

MANUAL NO.*	TITLE
H-78-0408	Models 7702-7704 Large Read/Write Memory Technical Manual
H-78-0061	Model 5752 2-D Coordinate Converter Technical Manual
H-79-0350	Model 5753 2-D/3-D Coordinate Converter User's Manual
H-79-0450	Model 7750 Expansion Module Technical Manual
H-79-0411	GET-2 Tektronix Emulator User's Manual
H-79-0412	GET-2 Tektronix Emulator Source Listing
	PARALLEL INTERFACE MANUALS
H-78-0115	Model 5716 Parallel Interface to SEL32; HSD-9132
H-78-0343	Model 5719 Parallel Interface to Data General NOVA and ECLIPSE
H-79-0353	Model 5721 Parallel Interface, NTDS Slow
H-79-0354	Model 5722 Parallel Interface to Honeywell 516 DMC
	DISPLAY INDICATOR MANUALS
H-79-0378	Models 730-733 Monochrome Display Indicators Technical Manual
H-79-0394	Models 740-743 Four-Color Display Indicators Technical Manual
H-79-0395	Models 760, 763 Four-Color Display Indicators Technical Manual
	KEYBOARD MANUAL
H-79-0363	Model 5783 Alphanumeric Function Keyboard/Model 5784 Lighted Alphanumeric Function Keyboard
	POSITION ENTRY DEVICES MANUALS
H-78-0044	Model 5786 Trackball/Model 5787 Forcestick Entry Devices Technical Manual
50114-1	SIMPLE-2 Data Tablet (Talos, Scottsdale, Arizona)
	PHOTOPEN MANUAL
H-78-0042	Model 5781 PHOTOPEN Unit Technical Manual
	HARDCOPY MANUALS
GA-77-045	Model 570 Hardcopy Unit Technical Manual
H-78-0435	Model 0575 Hardcopy Multiplex Switch Technical Manual

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