S-MOS
SYSTEMS
A Seiko Epson Affiliate

1996 Graphics Products Data Book

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1996 DATABOOK

GRAPHICS PRODUCTS

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GRAPHICS PRODUCTS

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*1. Omitted from the 1996 Graphics Data Book.

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GRAPHICS PRODUCTS

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PRODUCT SUMMARY TABLES

The following pages contain product summary tables for all the S-MOS Graphics Products in this Data Book.

■ VGA GRAPHICS CONTROLLERS FEATURES MATRIX

Part Number		SPC8104 FOA	SPC8106FOC	SPC8107FOE	SPC8108FOC	SPC8110F OA
Part Name		Low Voltage LCD VGA Controller	Mixed Voltage Color LCD VGA Controller	Low Voltage VGA LCD Controller	Low Power LCD VGA Controller	Local Bus LCD/CRT VGA Controller
Discontinued?		No	No	No	No	No
Replacement		—	—	—	—	—
CRT Support		No	w/ external RAMDAC	No	w/ external RAMDAC	Yes
Color LCD Support	8-bit single/dual	x	x			x
	16-bit single/dual	x	x			x
	9-bit TFT		x			x
	12-bit TFT					x
	18-bit TFT					x
	12-bit RGB		x			
Monochrome LCD Support	4-bit single panel	x	x	x	x	x
	8-bit single/dual panel	x	x	x	x	x
CPU Bus Interface	ISA-8bit	x	x	x		
	ISA-16bit	x	x		x	
	VL-32bit					x
	PCI 2.0					x
	486DX Local bus					x
Display Resolution		320x200 to 640x480	320x200 to 640x480	320x200 to 640x480	320x200 to 640x480	320x200 to 1024x768
On-chip Color Lookup Table		64x4	256x12	64x4	256x6	256x18
Maximum Color	CRT		256		256	256
	color LCD		256			256
Maximum Grade Shades		16	64	16	64	64
Programmable Grayscale	base			(25,50,25)		
Weightings	NTSC	(30,59,11)	(30,59,11)	(30,59,11)	(30,59,11)	(30,59,11)
	text	(0,100,0)	(0,100,0)	(0,100,0)	(0,100,0)	(0,100,0)
Frame Buffer Support		one 256kx16 DRAM	one 256kx16 DRAM	one 256kx16 DRAM	one 256kx16 DRAM	two 256Kx16 DRAM

(continued)

■ VGA GRAPHICS CONTROLLERS FEATURES MATRIX (continued)

Part Number		SPC8104 FOA	SPC8106FOC	SPC8107FOE	SPC8108FOC	SPC8110F OA
Frame Buffer Data Bus Width (bits)		16	16	16	16	32
Self Refresh DRAM Support		x	x	x	x	x
Selectable CAS/WE DRAM Configuration		x	x	x	x	x
Asymmetrical/Symmetrical DRAM Support		x	x	x	x	x
Simultaneous Display			w/ single panel LCD			Yes
Power Save Modes	H/W Activated (# of pins)	1	1	1	1	2
	S/W Activated	5	5	5	5	2
I/O Interface Voltage	5V		x		x	x
	3.3V		x	x		x
Core Voltage	5V	x	x		x	x
	3.3V	2.5 or 3.3	x	x		x
Sprite/Hardware Cursor (bits)			64x64x2		64x64x2	64x64x2
Hardware Vertical Centering		x	x	x	x	x
Hardware Vertical Expansion		x	x		x	x
Bit Block Transfer Engine (BitBLT)						x
Linear Addressing						x
Color Expansion						x
Display Pipeline		4-stage	4-stage	4-stage	4-stage	32-bit
Integrated PLL						2
MClk,max		28.322 MHz	28.322 MHz	28.322 MHz	28.322 MHz	40MHz
PClk,max		28.322 MHz	28.322 MHz	28.322 MHz	28.322 MHz	65MHz
Package		144-pin QFP	144-pin QFP	100-pin QFP	144-pin QFP	208-pin QFP
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■ GRAPHIC LCD CONTROLLERS

Part Number		SED1330	SED1335	SED1336	SED1341	SED1345	SED1351	SED1352
Discontinued?		No	No	No	No	No	No	No
Replacement		—	—	—	—	—	—	—
Internal CGROM		160 chars (5x7)	160 chars (5x7)	160 chars (5x7)				
CPU Interface (Bits)	68xx	8	8	8			8, 16	8, 16
	80xx	8	8	8			8, 16	8, 16
	MPU				4	4	8, 16	8, 16
	ISA							8, 16
	Digital RGB				1(R or G or B)	4 (R,G,B,I)		
Display Size		up to 640x256 dots at a duty of 1/256	up to 640x256 dots at a duty of 1/256	LCD: 640x200, TV: 256x200	adjusted by H/W 640x200 640x350 640x400 640x480 720x350 720x480	adjusted by S/W 640x200 640x350 640x400 640x480	max. duty of 1/1024 up to 1024x1024	1/1024 single mode, 1/2048 dual mode, 640x480, 320x200
Frame Buffer Support		64KB SRAM	64KB SRAM	64KB SRAM	40KB SRAM	40KB SRAM	64KB SRAM	128KB SRAM
Frame Buffer Data Bus Width (bits)		8	8	8	8	8	16	8/16
fclk,max (MHz)		10	10	10	11.2		12.5	22
fosc (MHz)		10	10	10	34	30	14.29	25
Supply voltage	5V	x	x	x	x	x	FOA	x
	3V		x	x		x	FLB	x
Gray shade levels	2	x	x	x	x			
	4						x	x
	8					x		
	16							x
Display Data Bus (bits)	4	x	x	x	x	x	x	x
	8				x	x	x	x

(continued)

■ GRAPHIC LCD CONTROLLERS (continued)

Part Number		SED1330	SED1335	SED1336	SED1341	SED1345	SED1351	SED1352
Control Register		3 layers, smooth scrolling, inverse video, text and graphic display	3 layers, smooth scrolling, inverse video, text and graphic display	LCD/TV support, 3 layers, smooth scrolling, inverse video, text and graphic display	Set by digital switches or MPU for panel size, panel timing, clock select	Set by ROM or MPU for panel size, panel timing, clock select	2 layers, data OR function, smooth scrolling, overlay, inverse video	
Panel Type	Passive	x	x	x	x	x	x	x
	TV			ntsc/pal				
Package	QFP	FBA (QFP5-60pin), FBB (QFP6-60pin)	F0A (QFP5-60pin), F0B (QFP6-60pin)	F0A (QFP6-60pin)	F0E (QFP5-80pin)	F0A (QFP5-80pin)	F0A (QFP5-100pin), FLB (QFP15-100pin)	F0A (QFP5-100pin)
Page Number		125	139	153	165	185	197	215

Notes: 1. Some packages of certain parts labeled with # are still under development.

■ LCD DRIVER-CONTROLLERS (12xx Series)

Part Number		SED 1200	SED 1210	SED 1230	SED 1231 T	SED 1232 E	SED 1233 X	SED 1234 T	SED 1235	SED 1278	SED 1280
Discontinued?		No	No	No	No	No	No	No	No	No	No
Replacement		—	—	—	—	—	—	—	—	—	—
Commons		16	16	30	23	16	16	30	16	16	16
Segments		50	40	65	65	65	80	62	62	40	40
Duty Cycle	1/3										
	1/4										
	1/7										
	1/8	x	x							x	x
	1/9										
	1/10										
	1/11									x	x
	1/16	x	x			x	x		x	x	x
	1/17										
	1/23				x						
	1/24										
	1/25										
	1/30			x				x			
	1/32										
	1/33										
	1/48										
	1/49										
	1/64										
	1/65										
LCD Voltage (V)		−3.5 to −5.5	−3.5 to −5.5	−4.5 to −12	−4.5 to −12	−4.5 to −12	−4.5 to −12	−4.5 to −12	−4.5 to −12	−3 to −5.5	−3 to −5.5
Supply Voltage	5V	x	x							x	x
	3V	x	x	x	x	x	x	x	x		
CPU Interface	MPU	x	x	x	x	x	x	x	x	x	
	68xx			x	x	x	x	x	x	x	
	80xx	x	x	x	x	x	x	x	x		

(continued)

■ LCD DRIVER-CONTROLLERS (12xx Series – continued)

Part Number			SED 1200	SED 1210	SED 1230	SED 1231 T	SED 1232 E	SED 1233 X	SED 1234 T	SED 1235	SED 1278	SED 1280
Display Data Bus (bits)		1			x	x	x	x	x	x		x
		4	x		x	x	x	x	x	x	x	
		8		x	x	x	x	x	x	x	x	
Fosc,max (KHz)			100	100	39	30	21	26			250	1000
CGROM Size (chars)			160	160	256	256	256	256			240	240
CGRAM size (chars)			4	4	4	4	4	4			8	8
Display Data RAM size			20 char	40 char	48 char	48 char	48 char	48 char	48 char	48 char	80 char	80 char
Companion Chips				1181							1181, 1681	1181, 1681
Integrated DC/DC Converter					x	x	x	x				
Static Icon					x	x	x	x				
Contrast Adjustment By Software					x	x	x	x				
Master/Slave Operation												
Panel Type		Passive	x	x	x	x	x	x			x	x
		MIM										
		TFT										
Package	Die	Al	D0A(JIS) D0B (ASCII)	D0A(JIS) D0B (ASCII)	D0A	D0A	D0A	D0A	D0A	D0A	D0A D0B D0C D0E D0G D0H	
		Au			D0B	D0B	D0B	D0B	D0B	D0B		
		COG										
		PadPitch (μm)	190	190	110	110	110	110				
	QFP	Thin	F1B									
		Thick	F0A (JIS) F0B (ASCII)	F0A (JIS) F0B (ASCII)							F0A F0B F0C F0E F0G F0H	F0A F0B F0C
		# of Pins	80	80							80	100
	TAB	2sided			TBB	TBB	TBB	TBB				
		4sided										
		LeadPitch (μm)										
Page Number			237	253	265	265	265	265	265	265	287	303

(continued)

■ LCD DRIVER-CONTROLLERS (15xx Series)

Part Number		SED 1500	SED 1501	SED 1502 T	SED 1503 E	SED 1507 X	SED 1510 T	SED 1520	SED 1521 &	SED 152A	SED 1522 G	SED 1526 R	SED 1527 A	SED 1528 P	SED 1530 H	SED 1531 I	SED 1532 C	SED 1540 S	SED 1560	SED 1561	SED 1562
Discontinued?		Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No
Replacement		No	No	No	No	No	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Commons		8	10	16	8	7	4	16	0	0	8	17	17	33	33	0	33	4	65/0	33	17
Segments		42	40	34	42	43	32	61	80	80	69	80	80	64	100	132	100	73	102/ 165	134	150
Duty Cycle	1/3																	x			
	1/4						x											x			
	1/7					x															
	1/8	x							x	x	x	x									
	1/9								x	x		x									
	1/10		x						x	x											
	1/11								x	x											
	1/16			x	x			x	x	x	x	x	x								x
	1/17								x	x		x	x								x
	1/23									x											
	1/24								x	x										x	
	1/25								x	x										x	
	1/30									x											
	1/32							x	x	x			x	x						x	
	1/33												x	x	x					x	
	1/48																		x		
	1/49																		x		
	1/64																		x		
	1/65															x	x		x		
LCD Voltage (V)		–3 to –10	–3 to –10	–3 to –10	–3 to –10	–3 to –10	–1.8 to –6	–3.5 to –13	–3.5 to –13	+3.5 to +13	–3.5 to –13	–4.5 to –16	–4.5 to –16	–4.5 to –16	–4.5 to –16	–4.5 to –16	–4.5 to –16	–3.5 to –11	–6 to –16	–5 to –16	–4.5 to –16
Supply Voltage	5V	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	3V	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
CPU Interface	MPU	x	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	x	x
	68xx							x	x	x	x	x	x	x	x	x	x	x	x	x	x
	80xx							x	x	x	x	x	x	x	x	x	x	x	x	x	x
Display Data Bus (bits)	1						x					x	x	x	x	x	x		x	x	x
	4	x	x	x	x	x															
	8	x	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	x	x
Fosc,max (KHz)		32	32	32	32	32	18	2,18	2,18	2	2,18	20	20	20	22	22	22	4,18	18	18	18

(continued)

■ LCD DRIVER-CONTROLLERS (15xx Series – continued)

Part Number			SED 1500	SED 1501	SED 1502	SED 1503	SED 1507	SED 1510	SED 1520	SED 1521	SED 152A	SED 1522	SED 1526	SED 1527	SED 1528	SED 1530	SED 1531	SED 1532	SED 1540	SED 1560	SED 1561	SED 1562
Display Data RAM size			672 bits	672 bits	672 bits	672 bits	672 bits	128 bits	2560 bits	2560 bits	2560 bits	2560 bits	2640 bits	2640 bits	2640 bits	8580 bits	8580 bits	8580 bits	2560 bits	10790 bits	10790 bits	10790 bits
Companion Chips									1520					1527			1635	1532		1630 /31	1630 /31	1630 /31
Integrated DC/DC Converter													2x, 3x	2x, 3x	2x, 3x	x	x	x		2x, 3x	2x, 3x	2x, 3x
Static Icon																x	x	x				
Contrast Adjustment By Software													x	x	x	x	x	x		x	x	x
Master/Slave Operation									x	slave only	slave only	x	x	x	x	x	x	x	x	x	x	x
Panel Type		Passive	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
		MIM																				
		TFT																				
Package	Die	Al						D0C	D0A DAA	D0A DAA	D0A #	D0A DAA	D*A	D*A	D*A	D*A	D*A	D*A	D0A			
		Au							D0B DAB	D0B DAB		D0B DAB	D*B	D*B	D*B	D*B	D*B	D*B	D0B			
		COG																				
		Pad Pitch (µm)							199	199		199	130	130	130	118	118	118	199	100	100	100
	QFP	Thin						F0C	F0C FAC	F0C FAC		F0C FAC										
		Thick	F0A	F0A	F0A	F0A	F0A	F0E (QFP 6-60)	F0A FAA	F0A FAA		F0A FAA	F0A	F0A	F0A				F0A			
		# of Pins	80	80	80	80	80	48	100	100		100	128	128	128				100			
	TAB	2sided							T0A TAA	T0A TAA		T0A TAA	T0A	T0A	T0A	T0A	T0A	T0A TBA		T0B	T0B	T0B
		4sided																		TQA	TQA	TQA
		Lead Pitch (µm)																				280
Page Number			307	307	307	307	307	315	329	329	341	343	353	353	353	369	369	369	389	395	395	395

■ HIGH-DUTY LCD SEGMENT DRIVERS

Part Number			SED 1180	SED 1181 xLA	SED 1181 F0A/ 5A	SED 1570	SED 1600	SED 1601	SED 1606	SED 1620	SED 1640	SED 1648	SED 1681	SED 1722	SED 1724	SED 1742	SED 1744	SED 1748	SED 1752	SED 1756	SED 1758	SED 1765	SED 1766	SED 1770	SED 1771
Discontinued?			Yes	Yes	Yes	No	Yes	Yes	No	Yes	No	No	Yes	No	No	No	No	No	No	No	No	No	No	No	No
Replacement			No	SED 168x	SED 168x	—	SED 1606	No	—	No	—	—	SED 168x	—	—	—	—	—	—	—	—	—	—	—	—
Resolution of segments			64	64	64	80	80	80	80	128	80	80	80	80	80	160	160	160	240	240	160	160	160	160	162
Duty Cycle			1/64 to 1/128	static to 1/32	1/64 to 1/128	1/64 to 1/200	1/100 to 1/300	1/100 to 1/300	1/100 to 1/300	1/64 to 1/200	1/100 to 1/300	1/100 to 1/300	1/8 to 1/32	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500
LCD Voltage (V)			–14 to –25	–3 to –12	–14 to –25	8 to 20	–12 to –28	–12 to –28	–8 to –28	–12 to –28	–8 to –28	–8 to –28	–3 to –12	14 to 40	14 to 40	14 to 40	14 to 40	8 to 42	8 to 42	14 to 42	14 to 42	14 to 40	14 to 40	5 to 17	5 to 17
Supply Voltage		5V	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
		3V		x		x			x		x	x				x	x	x	x	x	x				
Display Data Bus (Bits)	1			x	x								x												
	2																								
	3 (R,G,B)																							x	x
	4		x			x	x		x	x	x	x		x		x									
	8							x							x		x	x	x	x	x	x	x		
Xscl,max (Mhz)			6	0.6	6	6.6	6.5	6.5	10	4	7.5	7.5	1	12	12	12	12	16	18		18	12	12	10	10
Companion Chips			1190	1210/ 78	1191	1635	1610/ 30/31	1610/ 30/31	1630/ 35	1631/ 32	1635	1651	1278	1733	1733	1743	1743	1743	1743	1755	1743	1703	1703	1743	1743
Panel Type	Passive		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x		
	MIM																					x		x	x
	TFT																							x	x

(continued)

■ HIGH-DUTY LCD SEGMENT DRIVERS (continued)

Part Number			SED 1180	SED 1181 xLA	SED 1181 F0A/ 5A	SED 1570	SED 1600	SED 1601	SED 1606	SED 1620	SED 1640	SED 1648	SED 1681	SED 1722	SED 1724	SED 1742	SED 1744	SED 1748	SED 1752	SED 1756	SED 1758	SED 1765	SED 1766	SED 1770	SED 1771
Package	Die	Al	D0A	DLA	D0A	D0A	DAA	DAA	D0A			D0A	D0A	D0A	D0A							D0A	D0A	D0A	D0A
		Au				D0B	DAB		D0B		D0B					D1B	D1B	D0B			D0B	D0B	D0B		
		COG								D0A										D0A					
		Pad Pitch (µm)		190	190	170	153	180	153	125	105	178	160	160	160	108	108	82				134	134	120	120
	QFP	Thin	F0A		F0A																				
		Thick	F5A	FLA	F5A		FAA	FAA					F0A	F0A	F0A										
		# of Pins	80	80	80		100	100					100	100	100										
	TAB	2 side														T0A	T0A	T0A					T0A		
		Lead Pitch (µm)														180	180								
		Slim									T0A#								T0A		T0A T0B (flex)				
Page number			425	443	435	453	469	479	489	503	513	525	539	551	551	563	563	583	599	615	627	645	657	673	673

Notes:
1. Some packages of certain parts labeld with # are still under development.

■ HIGH-DUTY LCD COMMON DRIVERS

Part Number		SED 1190	SED 1191	SED 1610	SED 1630	SED 1631	SED 1632	SED 1633	SED 1634	SED 1635	SED 1651	SED 1733	SED 1741	SED 1743	SED 1753	SED 1755
Discontinued?		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No
Replacement		No	No	No	SED 167x	SED 167x	SED 167x	SED 167x	SED 167x	SED 167x	—	—	—	—	—	—
Resolution of commons		64	64	86	68	100	86	100	100	100	100	100	100	160	120	240
Duty Cycle		1/64 to 1/128	1/64 to 1/128	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/100 to 1/400	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500
LCD Voltage (V)		−14 to −25	−14 to −25	−12 to −28	−12 to −28	−12 to −28	−12 to −28	−12 to −28	−12 to −28	−8 to −28	−8 to −28	14 to 40	14 to 42	14 to 40	8 to 42	8 to 42
Supply Voltage	5V	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	3V				x			x	x	x	x		x	x	x	x
Data Bus (bits)	1	x	x	x	x	x	x	x	x	x	x	x	x	x		
	4															
Clock Frequency, max (MHz)		2.5	2.5	2.0	2.0	2.0	2.0	2.0 (5V), 1.0 (3V)	2.0 (5V), 1.0 (3V)	2.0 (5V), 1.0 (3V)	2.0 (5V), 1.0 (3V)	2.5	2.5 (5V), 1.25 (3V)	2.5 (5V), 1.25 (3V)		
Companion Chips		1180/ 81	1181	1600/ 01	1600/ 01	1600/ 01/20	1600	1600	1600	1570, 1600	1648	1722/ 24	1742/ 44	1742/ 44	1752/ 58	1756
Panel Type	Passive	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	MIM															
	TFT															

(continued)

■ HIGH-DUTY LCD COMMON DRIVERS (continued)

Part Number			SED 1190	SED 1191	SED 1610	SED 1630	SED 1631	SED 1632	SED 1633	SED 1634	SED 1635	SED 1651	SED 1733	SED 1741	SED 1743	SED 1753	SED 1755
Package	Die	Al	D0A	D0B		D0A	D0A	D0A	D1A	D1A	D1A	D0A	D0A				
		Au					D0B		D1B	D1B	D1B			D1B	D1B	D0B	
		COG															D0A
		Pad Pitch (μm)		190			149	240	149	149	149	153	170	108	108		
	TAB	2 Sided												T0A	T0A	T0A	
		Lead Pitch (μm)													180		
	QFP	Thin	F0A, F0B	F0B													
		Thick	F5A, F5B2	F5B	FAA	F0A							F0A				
		# of Pins	80	80	100	80							128				
Page number			705	713	721	727	733	741	747	759	771	783	795	805	819	835	849

Notes:
1. Some packages of certain parts labeled with # are still under development.

■ DC/DC CONVERTERS

Part Number	SCI7660	SCI7661	SCI7654
Part Name	CMOS DC/DC Converter	DC/DC Converter with voltage regulator and temperature compensation	DC/DC Converter with voltage regulator and temperature compensation
Discontinued?	No	No	No
Replacement	—	—	—
Maximum output voltage	−20V	−20V	−22V
Maximum output current	30 mA	20 mA	80/N mA
Voltage doubler	yes	yes	yes
Voltage tripler	no	yes	yes
Voltage quadrupler	no	no	yes
Input Voltage	−1.2 to −8.0V	−1.2 to −6.0V	−2.0 to −11.0V
Number of Output Voltage Levels	2	4	4
Conversion Efficiency	95%	95%	95%
Package	DIP-8pin(C0A) SOP4-8pin(M0A)	DIP-14pin(C0A) SOP5-14pin(M0A) SSOP2-16pin(MAA)	SSOP2-16pin (M0A) Al pad Die (D0A)
Page number	867	873	879

CUSTOMER TECHNICAL SUPPORT

S-MOS Systems provides Technical Support Services to their customers for all the graphics products. Please follow the technical support guidelines as listed below for the different graphics product families — VGA LCD Controllers, LCD Controllers, LCD Driver/Controllers, and LCD Drivers.

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North East and North Central
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1996 DATABOOK

GRAPHICS PRODUCTS

II. VGA GRAPHICS CONTROLLERS

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■ VGA GRAPHICS CONTROLLERS FEATURES MATRIX

Part Number		SPC8104 FOA	SPC8106FOC	SPC8107FOE	SPC8108FOC	SPC8110F OA
Part Name		Low Voltage LCD VGA Controller	Mixed Voltage Color LCD VGA Controller	Low Voltage VGA LCD Controller	Low Power LCD VGA Controller	Local Bus LCD/CRT VGA Controller
Discontinued?		No	No	No	No	No
Replacement		—	—	—	—	—
CRT Support		No	w/ external RAMDAC	No	w/ external RAMDAC	Yes
Color LCD Support	8-bit single/dual	x	x			x
	16-bit single/dual	x	x			x
	9-bit TFT		x			x
	12-bit TFT					x
	18-bit TFT					x
	12-bit RGB		x			
Monochrome LCD Support	4-bit single panel	x	x	x	x	x
	8-bit single/dual panel	x	x	x	x	x
CPU Bus Interface	ISA-8bit	x	x	x		
	ISA-16bit	x	x		x	
	VL-32bit					x
	PCI 2.0					x
	486DX Local bus					x
Display Resolution		320x200 to 640x480	320x200 to 640x480	320x200 to 640x480	320x200 to 640x480	320x200 to 1024x768
On-chip Color Lookup Table		64x4	256x12	64x4	256x6	256x18
Maximum Color	CRT		256		256	256
	color LCD		256			256
Maximum Grade Shades		16	64	16	64	64
Programmable Grayscale	base			(25,50,25)		
Weightings	NTSC	(30,59,11)	(30,59,11)	(30,59,11)	(30,59,11)	(30,59,11)
	text	(0,100,0)	(0,100,0)	(0,100,0)	(0,100,0)	(0,100,0)
Frame Buffer Support		one 256kx16 DRAM	one 256kx16 DRAM	one 256kx16 DRAM	one 256kx16 DRAM	two 256Kx16 DRAM

(continued)

■ VGA GRAPHICS CONTROLLERS FEATURES MATRIX (continued)

Part Number		SPC8104 FOA	SPC8106FOC	SPC8107FOE	SPC8108FOC	SPC8110F OA
Frame Buffer Data Bus Width (bits)		16	16	16	16	32
Self Refresh DRAM Support		x	x	x	x	x
Selectable CAS/WE DRAM Configuration		x	x	x	x	x
Asymmetrical/Symmetrical DRAM Support		x	x	x	x	x
Simultaneous Display			w/ single panel LCD			Yes
Power Save Modes	H/W Activated (# of pins)	1	1	1	1	2
	S/W Activated	5	5	5	5	2
I/O Interface Voltage	5V		x		x	x
	3.3V		x	x		x
Core Voltage	5V	x	x		x	x
	3.3V	2.5 or 3.3	x	x		x
Sprite/Hardware Cursor (bits)			64x64x2		64x64x2	64x64x2
Hardware Vertical Centering		x	x	x	x	x
Hardware Vertical Expansion		x	x		x	x
Bit Block Transfer Engine (BitBLT)						x
Linear Addressing						x
Color Expansion						x
Display Pipeline		4-stage	4-stage	4-stage	4-stage	32-bit
Integrated PLL						2
MClk,max		28.322 MHz	28.322 MHz	28.322 MHz	28.322 MHz	40MHz
PClk,max		28.322 MHz	28.322 MHz	28.322 MHz	28.322 MHz	65MHz
Package		144-pin QFP	144-pin QFP	100-pin QFP	144-pin QFP	208-pin QFP
Page Number		5	21	53	69	87

VGA LCD CONTROLLER

■ DESCRIPTION

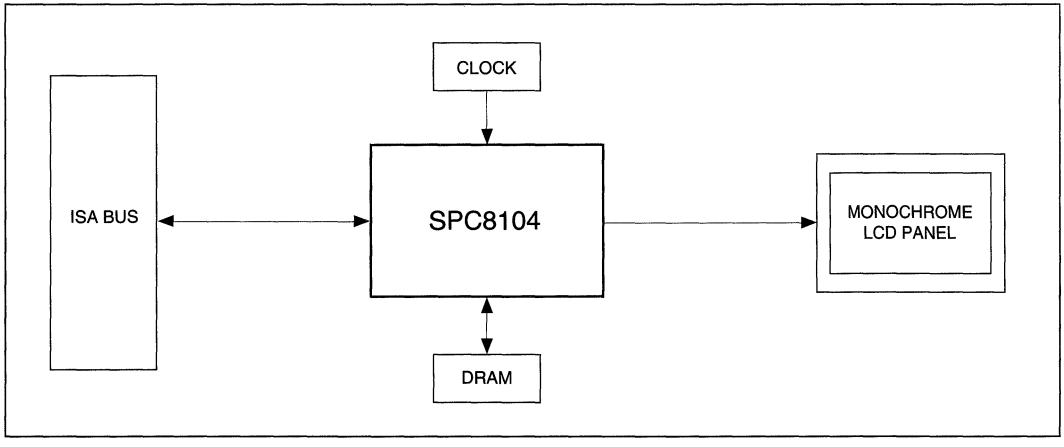
The SPC8104 is a low power, mixed 2.5/3.3 volt graphics controller based on VGA architecture and optimized for driving a 640x480 LCD panel display. VGA standard mode functionality (with the exception of mode 13h) is supported using standard IBM VGA parameters. A proprietary 64x4-bit gray scale lookup table is provided to allow re-mapping of the 16 possible gray shades displayed on an LCD panel.

The target markets for this device are small, cost sensitive mixed 2.5V/3.3V hand-held organizers, or other specialized consumer products where low cost, low power consumption, low component count, and the ability to run most VGA software on a 640x480 LCD panel display are the major design considerations. This chip is intended to operate mainly in planar graphics modes.

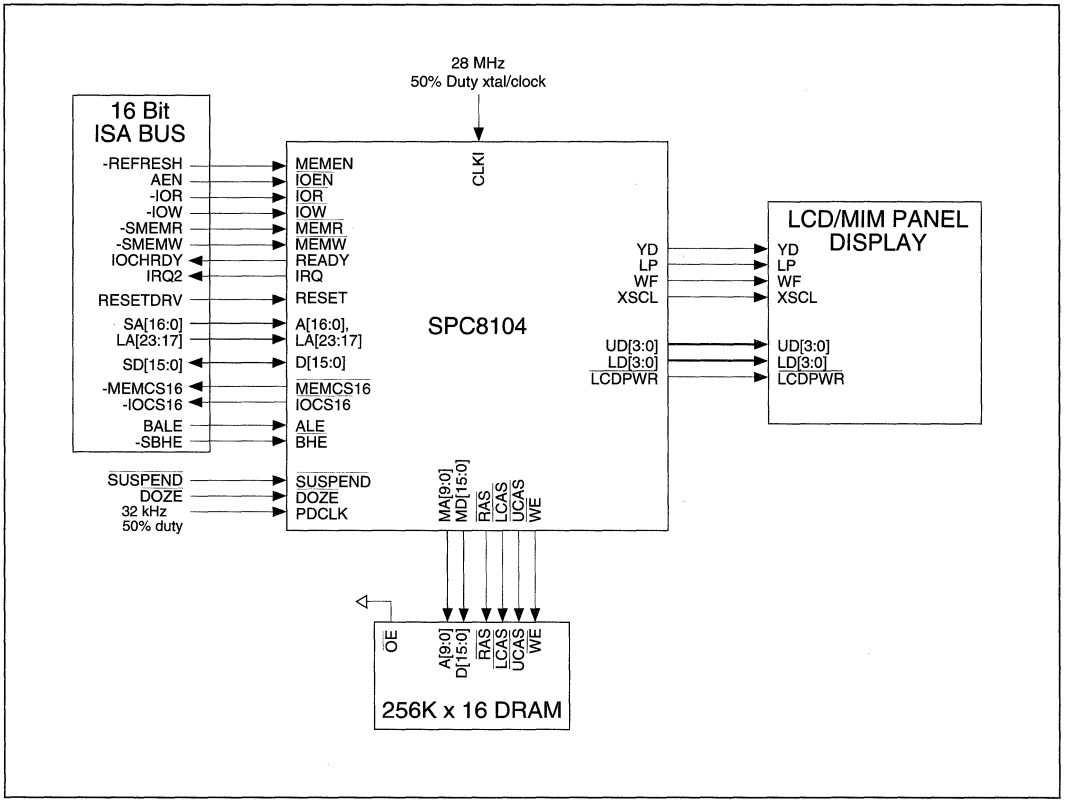
■ FEATURES

- Low power CMOS with 2.5V/3.3V core and 3.3V I/O
- 8/16-bit ISA CPU data bus interface
- Interfaces to a single 256 Kx16 DRAM
- Selectable 256 cycle/4 msec or 256 cycle/32 msec DRAM refresh rate, or low power self-refresh mode
- Three hardware or software initiated power-save modes
- Supports all standard VGA modes except mode 13h.
- Proprietary internal 64x4 gray scale lookup table
- Programmable hardware mapping of VGA palette-style writes to 16 level LCD gray scale values
- Vertical interrupt function on IRQ pin supported
- Optimized for 640x480 single and dual panel monochrome LCD displays
- Flexible support of LCD panels of various sizes
- Supports 0-255 vertical non-display periods
- Supports 640x480 4-bit monochrome MIM panels
- Power consumption of 60 mW in active mode and 0.6 mW in "Power Save" mode when operating at 24 MHz
- F0A - 128 pin QFP15 package

■ SYSTEM BLOCK DIAGRAM



■ INTERFACE OPTIONS



Note: Example implementation, actual may vary.

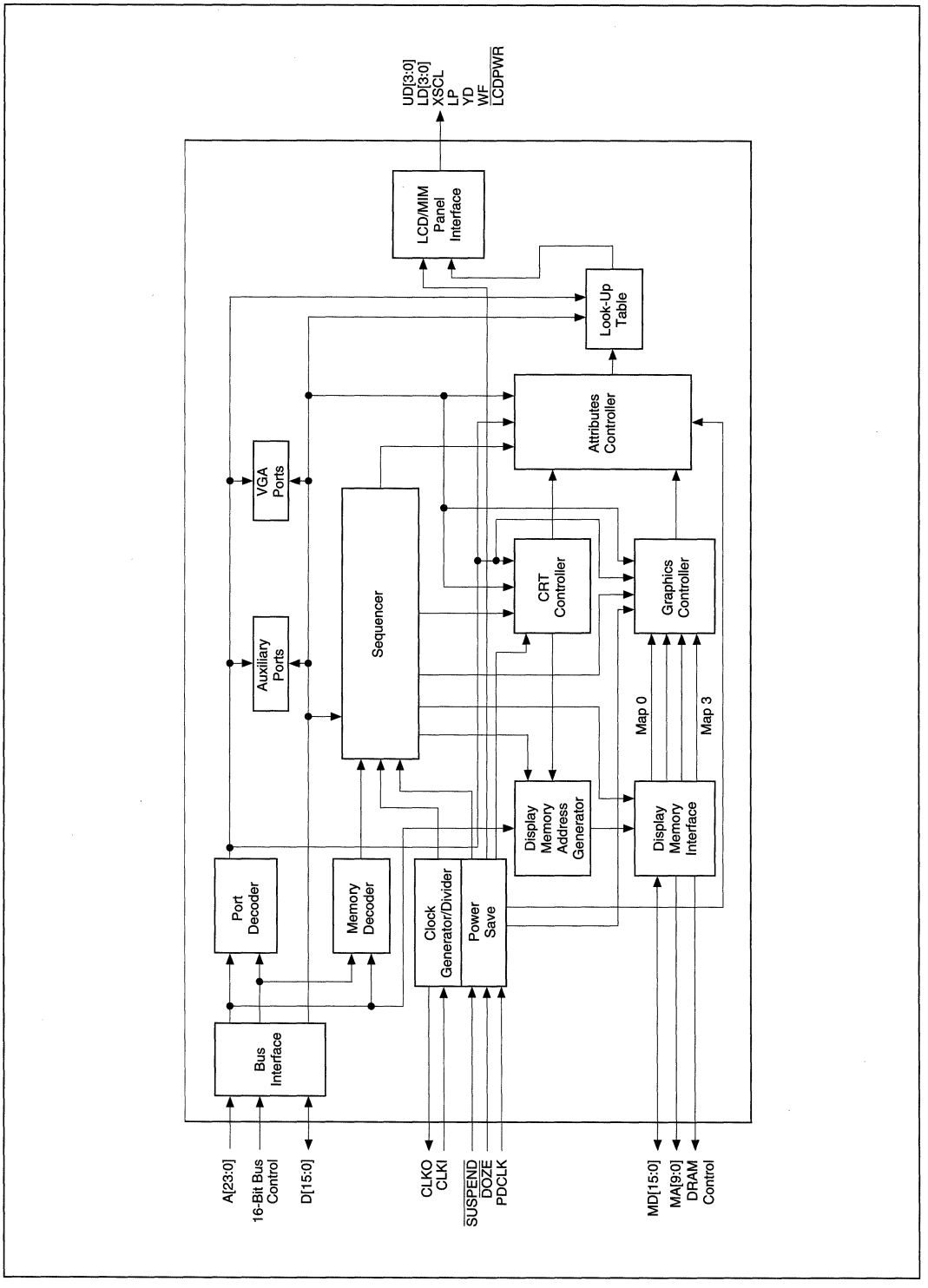
■ SUPPORTED RESOLUTIONS

Mode No.	Mode Type	Font	Characters	Resolution	Displayed Pixels	Gray Shades	Memory Segment
0	T	8 X 8	40 X 25	320 X 200	640 X 400	16	B800
0+	T	8 X 14	40 X 25	320 X 350	640 X 350	16	B800
0++	T	8 X 16	40 X 25	320 X400	640 X 400	16	B800
1	T	8 X 8	40 X 25	320 X 200	640 X 400	16	B800
1+	T	8 X 14	40 X 25	320 X 350	640 X 350	16	B800
1++	T	8 X 16	40 X 25	320 X 400	640 X 400	16	B800
2	T	8 X 8	80 X 25	640 X 200	640 X 400	16	B800
2+	T	8 X 14	80 X 25	640 X 350	640 X 350	16	B800
2++	T	8 X 16	80 X 25	640 X400	640 X 400	16	B800
3	T	8 X 8	80 X 25	640 X 200	640 X 400	16	B800
3+	T	8 X 14	80 X 25	640 X 350	640 X 350	16	B800
3++	T	8 X 16	80 X 25	640 X 400	640 X 400	16	B800
4	G	N/A	NA	320 X 200	640 X 400	4	B800
5	G	N/A	N/A	320 X 200	640 X 400	4	B800
6	G	N/A	N/A	640 X200	640 X 400	2	B800
7	T	8 X 14	80 X 25	640 X 350	640 X 350	2	B800
7+	T	8 X 16	80 X 25	640 X 400	640 X 400	2	B800
0D	G	N/A	N/A	320 X 200	640 X 400	16	A000
0E	G	N/A	N/A	640 X 200	640 X 400	16	A000
0F	G	N/A	N/A	640 X 350	640 X 350	2	A000
10	G	N/A	N/A	640 X350	640 X 350	16	A000
11	G	N/A	N/A	640 X 480	640 X 480	2	A000
12	G	N/A	N/A	640 X 480	640 X 480	16	A000

■ SUPPORTED LCD INTERFACES

8-Bit Interface				4-Bit Interface	
Dual Panel		Single Panel		Single panel	
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
1 to 640	241 to 480	1 to 640	1 to 480	1 to 640	1 to 480

■ BLOCK DIAGRAM



■ DC SPECIFICATIONS

● Absolute Maximum Ratings

Parameters	Codes	Rating	Units
Supply voltage	V_{DD}	V_{SS} –0.3 to +7.0	V
Input voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	V_{SS} –0.3 to V_{DD} +0.3	V
Operating temperature	T_{OPR}	0 to +70	°C
Storage temperature	T_{STG}	–65 ~ +150	°C
Soldering temperature/time	T_{SOL}	–260 for 10 sec max at lead	°C

● Recommended Operating Conditions

Parameter	Symbol	Condition	Range			Unit
			Min	Typ	Max	
Supply voltage	HV_{DD}	V_{SS} = 0V	3.0	3.3	3.6	V
Supply voltage	LV_{DD}	V_{SS} = 0V	2.25	2.5	3.6	V
Input voltage	V_{IN}	V_{SS}	V_{SS}	—	V_{DD}	V
Operating temperature	T_{OPR}		0	25	70	°C
Average power consumption	I_{OPR}			20		mA
Doze mode 1	IP_{D1}			10		mA
Doze mode 2	IP_{D2}		5	5		mA
Suspend	IP_{SUS}			0.2		mA

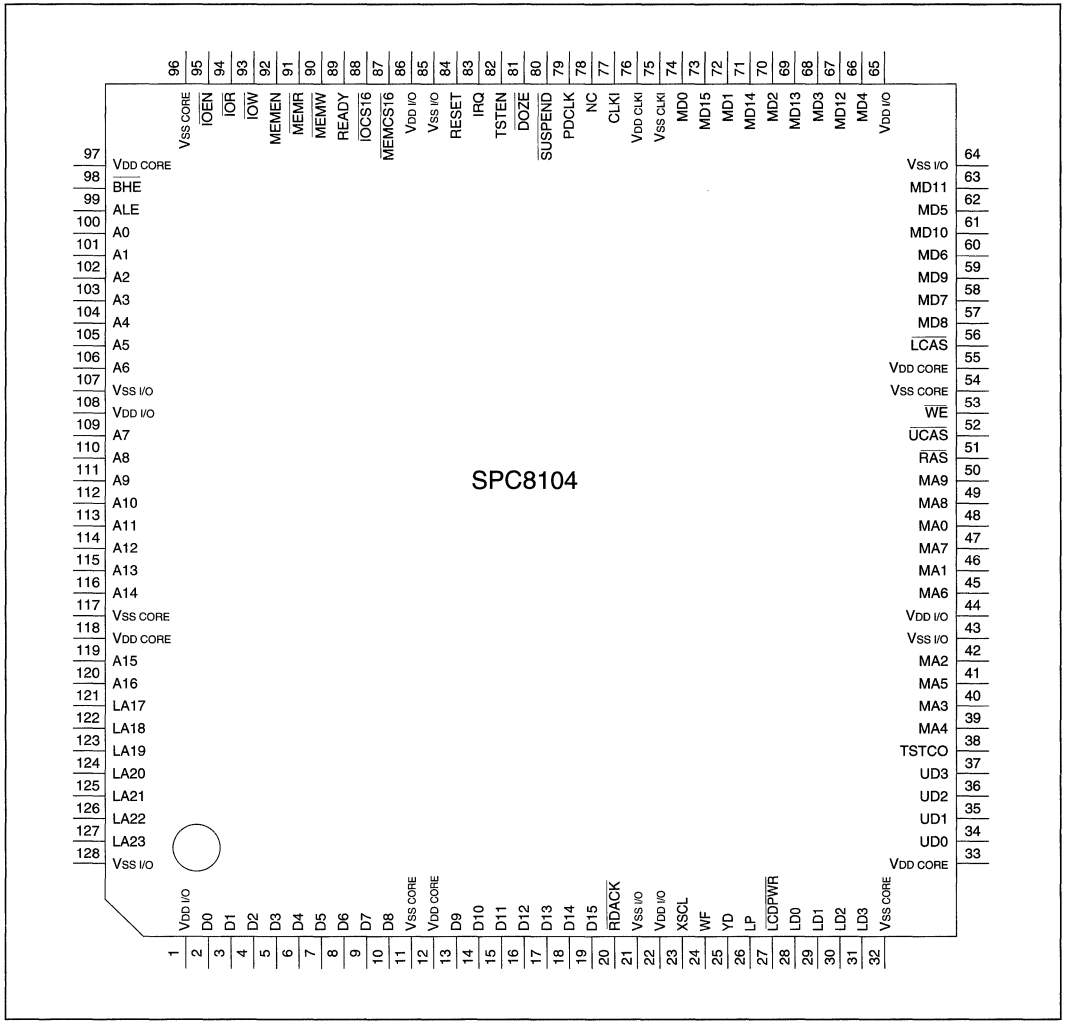
● Input Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low level input voltage	V_{IL}	V_{DD} =MIN			0.8	V
High level input voltage	V_{IH}	V_{DD} = MAX	2.0			V
Positive-going threshold (CMOS Schmitt inputs)	V_{T+}	V_{DD} = 3.3V			2.4	V
Negative-going threshold (CMOS Schmitt inputs)	V_{T-}	V_{DD} = 3.3V	0.6			V
Hysteresis voltage (CMOS Schmitt inputs)	V_H	V_{DD} = 3.3V	0.1			V
Input leakage current	I_{IZ}	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1		1	µA
Input pin capacitance	C_{IN}			8		pF
Pull up resistance	R_{PU}	V_{DD} = 3.3V		90		KΩ
Pull down resistance	R_{PD}	V_{DD} = 3.3V		90		KΩ

● Output Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low level output current	I_{OL1}	V_{OL} =V_{SS} +0.4V TSI, TSIU, CO1	3.0			mA
High level output current	I_{OH1}	V_{OH} = V_{DD} –0.4V TSI, TSIU, CO1	–3.0			mA
Low level output current	I_{OL2}	V_{OL} = V_{SS} +0.4V TS2, CO2	6.0		2.4	mA
High level output current	I_{OHI2}	V_{OH} = V_{DD} –0.4V TS2, CO2	–6.0			mA
Output leakage current	I_{OZ}	V_{OH} = V_{DD} or V_{OL} = V_{SS}	–1		1	μA
Output pin capacitance	C_{OUT}			8		pF

■ SPC8104 PIN OUTS



■ PIN DESCRIPTION

Key

A = Analog
I = Input
O = Output
I/O = Bi-directional
P = Power

CPU Interface

Pin Name	Type	Pin#	Description
A[O:16], LA[17:23]	I	100~106, 109~116 119~127	CPU bus unlatched address inputs. For an 8-bit CPU interface configuration, LA[20:23] are ignored and LA[17:19] should be connected to the latched CPU address SA[17:19]. In Suspend Mode, the address inputs are internally masked off.
D[0:15]	I/O	2~10, 13~19	16 bit ISA-Bus data bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
ALE	I	99	ISA Bus Address Latch Enable. ALE is ignored for an 8-bit CPU interface configuration. In Suspend Mode this input is disabled.
MEMEN	I	92	ISA Bus Memory Enable. This signal should be connected to the -REFRESH signal on the ISA bus. When this signal is low (e.g. during a system memory refresh cycle), memory address decoding is disabled.
IOR#	I	94	ISA Bus I/O Read Strobe. In Suspend Mode this input is disabled.
IOW#	I	93	ISA Bus I/O Write Strobe. In Suspend Mode this input is disabled.
MEMR#	I	91	ISA Bus Memory Read Strobe. In Suspend Mode this input is disabled.
MEMW#	I	90	ISA Bus Memory Write Strobe. In Suspend Mode this input is disabled.
IOEN#	I	95	ISA Bus I/O Enable. This input should be connected to the ISA bus AEN signal. When this signal is high, I/O address decoding is dis-abled. In Suspend Mode this input is disabled.
READY	O	89	ISA Bus READY signal. This output is driven low to force the CPU to insert wait states during memory cycles. READY is released to high-Z after a transfer is complete.
RESET	I	84	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state. During Suspend Mode the RESET input is ignored.
IRQ	O	83	ISA Bus Vertical Interrupt. When enabled, a Vertical Retrace Interrupt will cause this signal to be driven from a logic 0 state to a logic 1 (rising-edge triggered interrupt). Once set, this interrupt must be cleared by a bit in the CRTC registers. A control bit in the Auxiliary Registers allows this output to be optionally disabled (tri-stated).
MEMCS16#	O	87	ISA Bus Memory Chip Select 16. Address inputs LA[23:17] are decoded to drive this output low when a valid memory address (AXXXXh, BXXXXh) appears on the bus.
IOCS16#	O	88	ISA Bus Memory Chip Select 16. Address inputs LA[23:17] are decoded to drive this output low when a valid SPC 8104 I/O register address appears on the bus. Note that I/O addresses 3C6h-3C9h does not result in IOCS16# being driven low (i.e. internal LUT register reads and writes are 8 bit cycles).
BHE#	I	98	ISA Bus Byte High Enable. In Suspend Mode the this input is disabled.
RDACK#	O	20	Read Acknowledge. This pin goes low during valid I/O or memory reads to the chip.

Frame Buffer Memory Interface

Pin Name	Type	Pin#	Description
MA[0:9]	O	48,46,42, 40,39,41, 45,47,49, 50	Multiplexed row/column address bits for video display memory.
MD[0:4] MD[7:15]	I/O	74,72,70, 68,66,58, 57,59,61, 63,67,69, 71,73	Data bits for video display memory. The output drivers of these are placed into a high-impedance state when RESET is high. On the falling edge of RESET, the values on MD[3:0] are latched into a read-only Auxiliary Register and are available to be read as configuration inputs. Also, the values on MD[5:6] are used to configure other various hardware options - see "Summary of Configuration Options", for details. Note that there are internal pullup resistors on the inputs of these pins except MD[5:6].
MD[5:6]	I/O	62,60	
RAS#	O	51	DRAM Row Address Strobe.
LCAS# (LWE#)	O	56	DRAM Column Address Strobe for low byte (LCAS#), or Write Enable Strobe for low byte (LWE#), as determined by logic value on MD[6] during RESET (see pin mapping table).
UCAS# (CAS#)	O	52	DRAM Column Address Strobe for high byte (UCAS#), or single Column Address Strobe (CAS#), as determined by logic value on MD[6] during RESET (see pin mapping table).
WE# (UWE#)	O	53	DRAM Write Enable Strobe (WE#), or Write Enable Strobe for high byte (UWE#), as determined by logic value on MD[6] during RESET (see pin mapping table).

Clock Inputs

Pin Name	Type	Pin #	Description
CLKI	I	77	This is the clock source input and should be connected to an external oscillator.

Power Supply

Pin Name	Type	Pin #	Description
V_{DD} CORE	P	12, 33, 55, 97, 118	V_{DD} supply for core logic.
V_{DD} I/O	P	1, 22, 44, 65, 86, 108	V_{DD} supply for I/O pins.
V_{DD} CLKI	P	76	V_{DD} supply for CLKI pin.
V_{SS} CORE	P	11, 32, 54, 96, 117	V_{SS} supply for core logic.
V_{SS} I/O	P	21, 43, 64, 85, 107, 128	V_{SS} supply for I/O pins.
V_{SS} CLKI	P	75	V_{DD} supply for CLKI pin.

Test Function

Pin Name	Type	Pin #	Drv	Description
TSTCO	I	38	CD	This pin enables the chip's test mode for the core logic. This pin must always be unconnected or tied to ground.
TSTEN	I	82	CD	This pin enables the chip's test mode for the I/O cells. This pin must always be unconnected or tied to ground.

LCD Panel Interface

Pin Name	Type	Pin#	Description
YD	O	25	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD/MIM panel module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	O	26	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD/MIM panel module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O	23	Shift Clock for LCD panel data or Pixel Clock for MIM panel data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD/MIM panel module column drivers (X drivers) on each falling edge).
UD[0:3]	O	34~37	Upper panel display data for dual LCD panel mode. For single LCD panel mode, these bits are the most significant 4 bits of the 8 bit output data to the panel (PD[4:7]). For 4-bit single LCD panel mode, these bits are the 4 bits of output data to the panel. For 4-bit MIM panel mode, these bits are driven 0.
LD[0:3]	O	28~31	Lower panel display data for dual LCD panel mode. For 8-bit single LCD panel mode, these bits are the least significant 4 bits of the 8 bit output data to the panel (PD[0:3]). For 4-bit single LCD panels, these bits are driven 0. For 4-bit MIM panel mode, these are the 4 bits of output data to the panel.
LCDPWR#	O	27	LCD power control. In normal operation this signal is driven low to enable an external LCD power supply. This signal is driven high when the chip is put into any power save mode, or if the Sequencer is in a reset state. It can be used externally to turn off the panel supply voltage and backlight. After a RESET, this signal is held high until the CRTC is programmed and running.
WF	O	24	LCD Panel Backplane Bias Signal or MIM Panel Data Enable Signal. In LCD panel mode, the WF signal toggles once per vertical frame period. In MIM panel mode, this signal goes high whenever display data are valid.

Power Save Mode Control

Pin Name	Type	Pin#	Description
PDCLK	I	79	Power Down Clock. This input may be used to provide a low frequency clock for generating DRAM refresh in Suspend mode, as an optional alternative to using the pixel clock or MEMEN input as the DRAM refresh clock source. This clock input should be driven by a 32 kHz 50% duty cycle clock. The PDCLK input is used to directly generate the RAS and CAS pulses in Suspend mode.
SUSPEND#	I	80	A low level on this pin puts the chip into the hardware Suspend mode. The SUSPEND# signal overrides any sofrware initiated power save modes as well as the DOZE# input pin, and disables the CPU bus interface inputs. CPU Address and Data inputs are masked when this signal is low. When in Suspend Mode the UD[3:0], LD[3:0], XSCL, LP, YD and WF signals are driven into a low state (or optionally, a high impendance state) and the LCDPWR# signal is driven high.
DOZE#	I	81	A low level on this pin puts the chip in Doze mode. The function of the Doze mode is determined by the Doze Mode Select bits in AUX[03]. This pin is ignored if the SUSPEND# input pin is asserted.

Configuration Options

Pin Name	Value on this pin at falling edge of RESET is used to configure: (1/0)
MD [3:0]	Values latched into read-only AUX [0C] bits 7–4 for software use
MD [5]	LCD signals' state in Suspend mode: Low (1), or Hi–Z (0)
MD [6]	2 CAS, 1 WE type DRAM (1), or 1 CAS, 2 WE type DRAM (0)

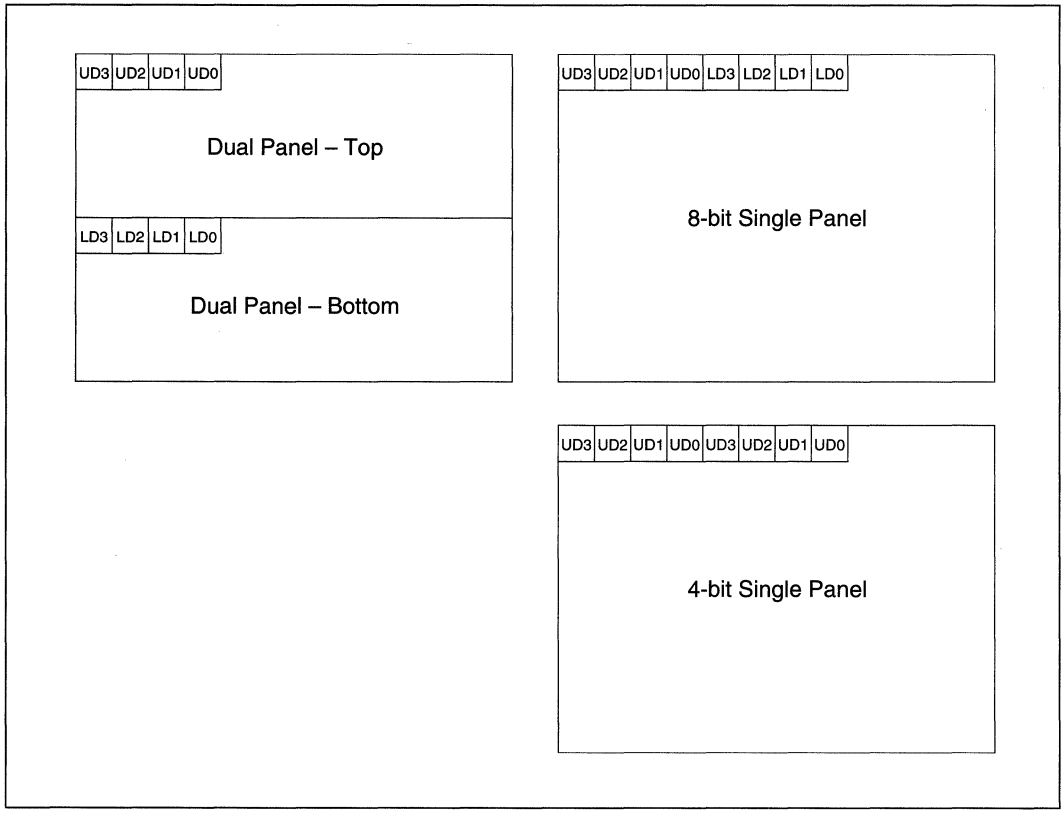
Multiple Function Pin Descriptions

Pin Name	Function	MD Line Status	Functional Description
LCAS#, LWE#	LCAS#	MD [6] = 1	DRAM column address strobe (low byte)
	LWE#	MD [6] = 0	DRAM write enable strobe
UCAS#, CAS#	UCAS#	MD [6] = 1	DRAM column address strobe (high byte)
	CAS#	MD [6] = 0	DRAM column address strobe
WE#, UWE#	WE#	MD [6] = 1	DRAM write strobe
	UWE#	MD [6] = 0	DRAM write strobe (high byte)

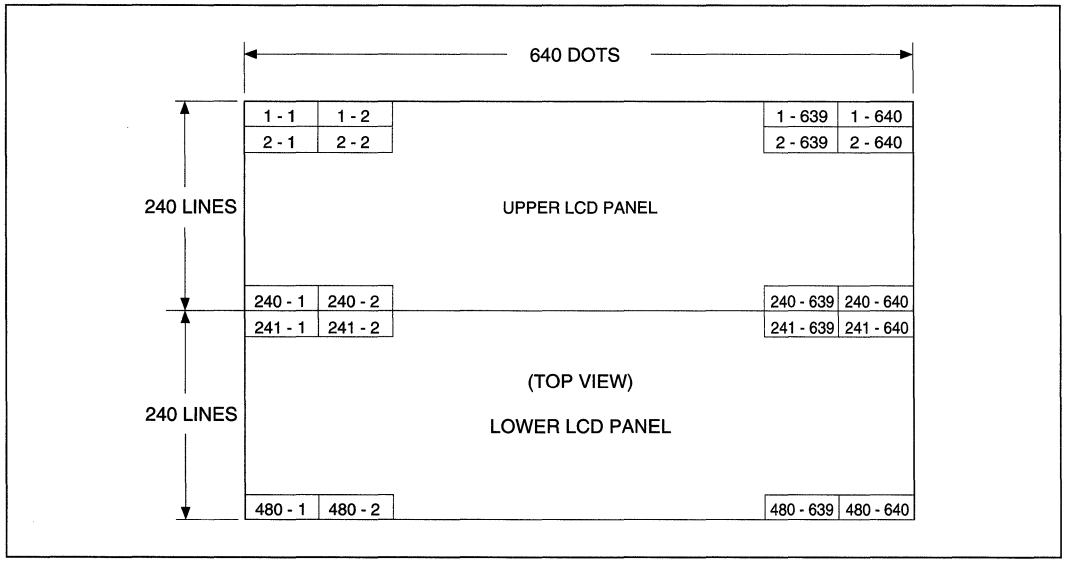
Mixed Voltage Configurations

Core V_{DD}	I/O V_{DD}	
	2.5 V	3.3 V
2.5 V	No	Yes
3.3 V	No	Yes

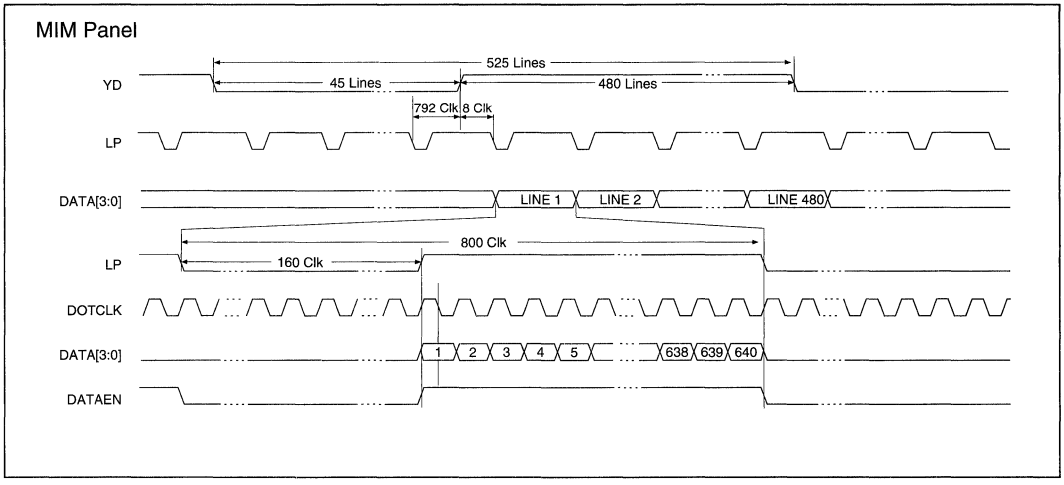
Illustrated below are the display data output which are output from the UD0 to UD3, LD0/UD4 to LD3/UD7 and the display on the panel:



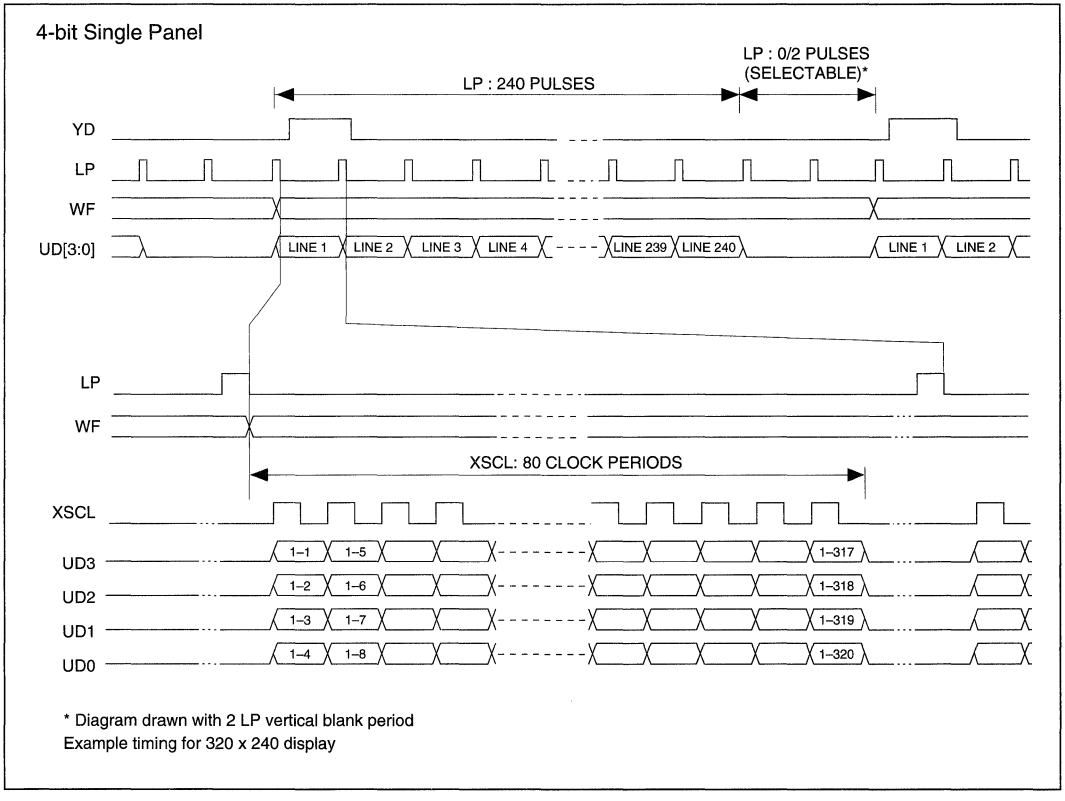
■ LCD Panel Pixels



■ MIM Panel Interface



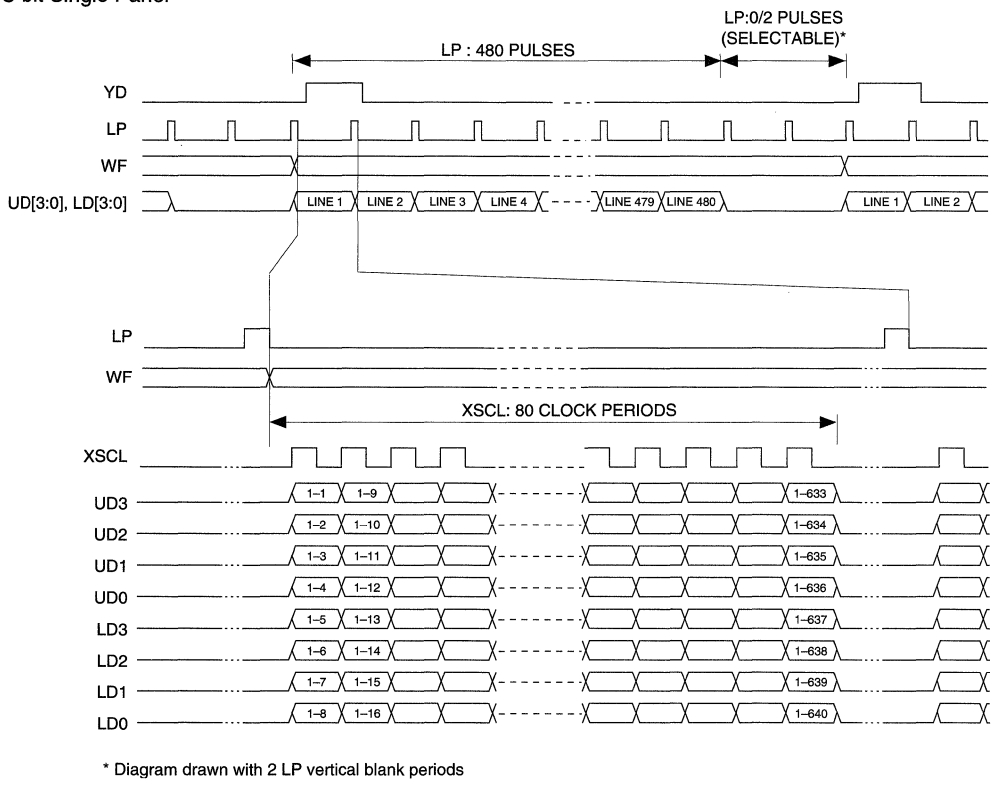
■ Monochrome Passive STN LCD Panel Interface



* Diagram drawn with 2 LP vertical blank period
Example timing for 320 x 240 display

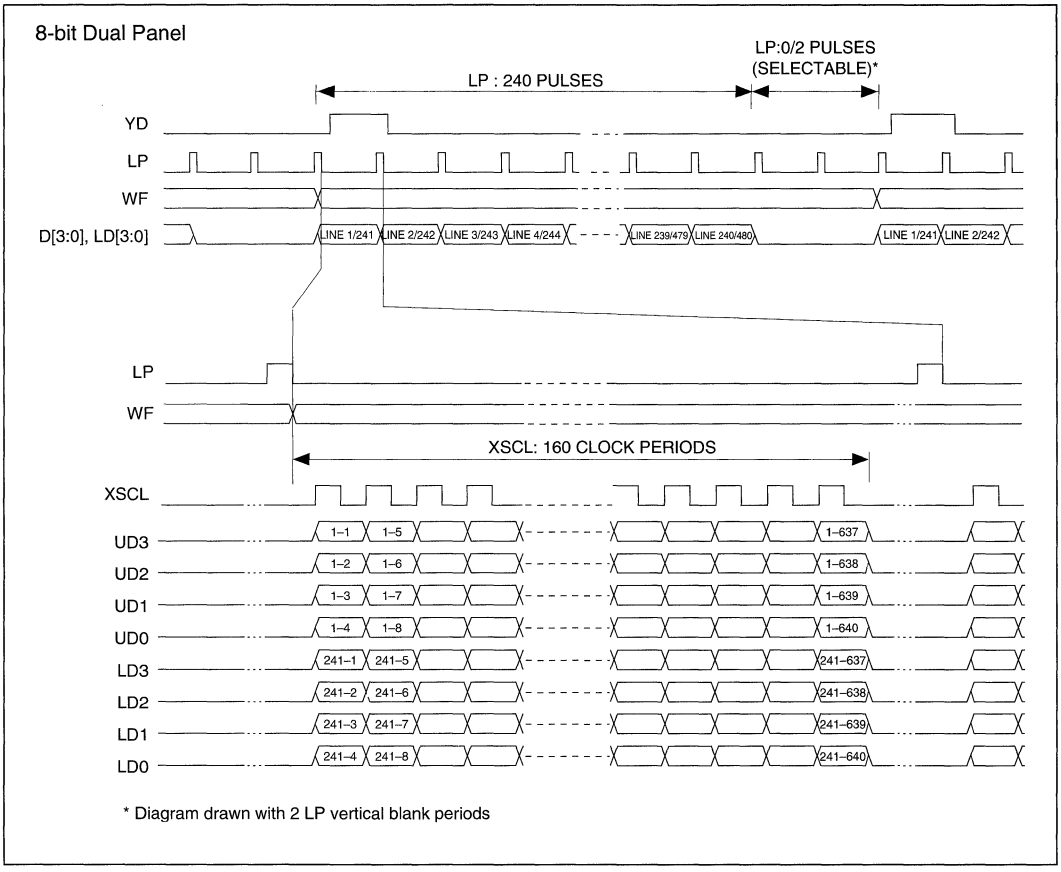
■ Monochrome Passive STN LCD Panel Interface

8-bit Single Panel



* Diagram drawn with 2 LP vertical blank periods

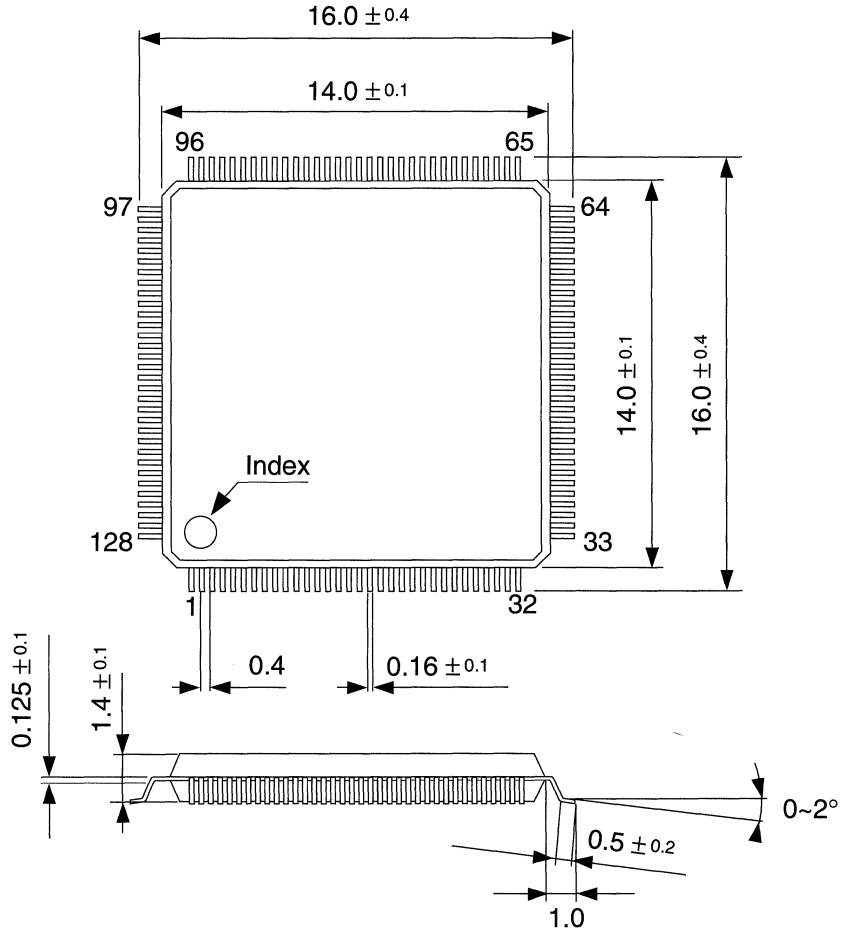
■ Monochrome Passive STN LCD Panel Interface



■ PACKAGE DIMENSIONS

QFP15-128 pin

Unit: mm



VGA LCD CONTROLLER

■ DESCRIPTION

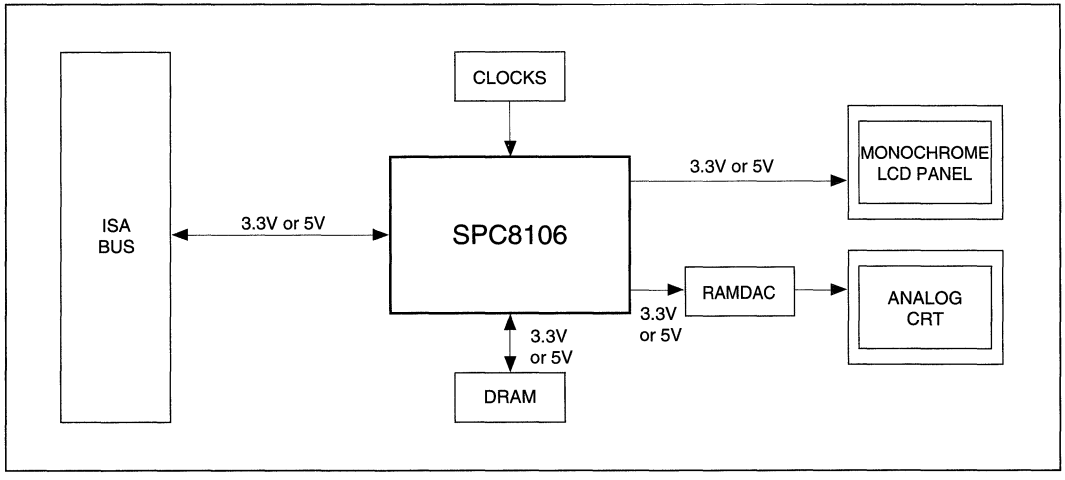
The SPC8106F0C is a versatile mixed voltage VGA graphics controller capable of driving liquid crystal displays, TFT displays and analog CRT monitors. The controller integrates all LCD interface, sequencing and color modulation logic into one small form factor 144 pin package. With the addition of an industry standard '477 compatible RAMDAC, the SPC8106F0C will also drive a VGA fixed frequency or multifrequency monitor.

The target products for this device are price and power sensitive 80x86 microprocessor based portable personal computer or other specialized LCD systems where 320 x 200 to 640 x 480 x 256 color LCD panel displays are the major design criteria.

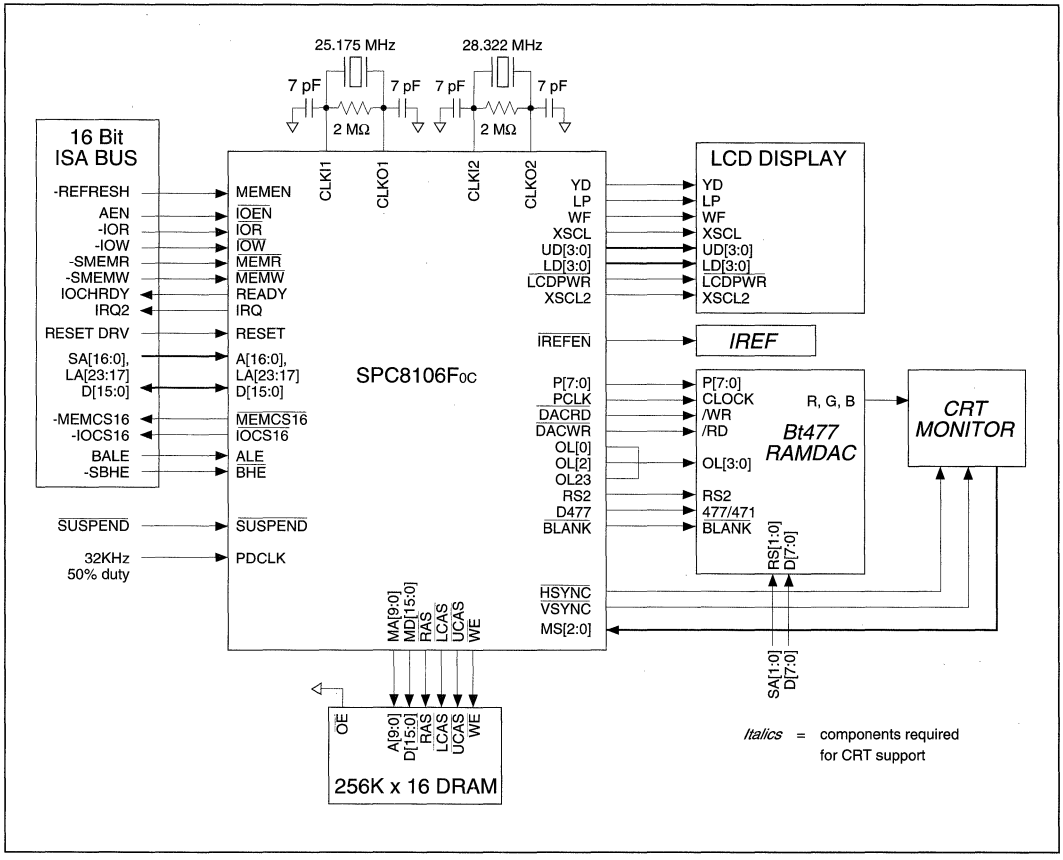
■ FEATURES

- Low-power CMOS technology
- Hardware VGA compatible
- 8- or 16-bit ISA support
- One 256K x 16 80ns DRAM (self refresh optional)
- 64 x 64 x 2-bit pixel hardware cursor
- Two-terminal crystal or external oscillator support
- Hardware or software power-down
- Video BIOS, software driver and utility support
- 144-pin QFP package
- 9- or 12-bit color TFT panel interface for 640 x 480
- Single panel or dual panel interface for sizes 320 x 200 to 640 x 480
- On-chip 256 x 12 look-up table
- 16 gray shades or 4096 colors by FRM
- 64 gray shades by FRM and dithering
- Two programmable gray-scale weightings: NTSC and Green-Only
- Vertical centering and expansion for LCDs
- Full CRT support with '477 compatible RAMDAC
- Pin Compatible with the SPC8108F0C
- Mixed voltage 3.3V/5V operation

■ SYSTEM BLOCK DIAGRAM



■ INTERFACE OPTIONS



Note: Example implementation, actual may vary.

■ SUPPORTED RESOLUTIONS

● LCD Display Modes

Mode No.	Mode Type	Font	Characters	Resolution	Displayed Pixels	Gray Shades	Colors	Memory Segment
0	Text	8 X 8	40 X 25	320 X 200	640 X 400	16	16	B800
0+	Text	8 X 14	40 X 25	320 X 350	640 X 350	16	16	B800
0++	Text	8 X 16	40 X 25	320 X 400	640 X 400	16	16	B800
1	Text	8 X 8	40 X 25	320 X 200	640 X 400	16	16	B800
1+	Text	8 X 14	40 X 25	320 X 350	640 X 350	16	16	B800
1++	Text	8 X 16	40 X 25	320 X 400	640 X 400	16	16	B800
2	Text	8 X 8	80 X 25	640 X 200	640 X 400	16	16	B800
2+	Text	8 X 14	80 X 25	640 X 350	640 X 350	16	16	B800
2++	Text	8 X 16	80 X 25	640 X 400	640 X 400	16	16	B800
3	Text	8 X 8	80 X 25	640 X 200	640 X 400	16	16	B800
3+	Text	8 X 14	80 X 25	640 X 350	640 X 350	16	16	B800
3++	Text	8 X 16	80 X 25	640 X 400	640 X 400	16	16	B800
4	Graphics	N/A	N/A	320 X 200	640 X 400	4	4	B800
5	Graphics	N/A	N/A	320 X 200	640 X 400	4	4	B800
6	Graphics	N/A	N/A	640 X200	640 X 400	2	2	B800
7	Text	8 X 14	80 X 25	640 X 350	640 X 350	2	2	B000
7+	Text	8 X 16	80 X 25	640 X 400	640 X 400	2	2	B000
0D	Graphics	N/A	N/A	320 X 200	640 X 400	16	16	A000
0E	Graphics	N/A	N/A	640 X 200	640 X 400	16	16	A000
0F	Graphics	N/A	N/A	640 X 350	640 X 350	2	2	A000
10	Graphics	N/A	N/A	640 X 350	640 X 350	16	16	A000
11	Graphics	N/A	N/A	640 X 480	640 X 480	2	2	A000
12	Graphics	N/A	N/A	640 X 480	640 X 480	16	16	A000
13	Graphics	N/A	N/A	320 X 200	640 X 400	64	256	A000
100	Graphics	N/A	N/A	640 x 400	640 x 400	64	256	A000
101	Graphics	N/A	N/A	640 x 480	640 x 480	64	256	A000
108	Text	8 x 8	80 x 60	640 X 480	640 X 480	16	16	B800

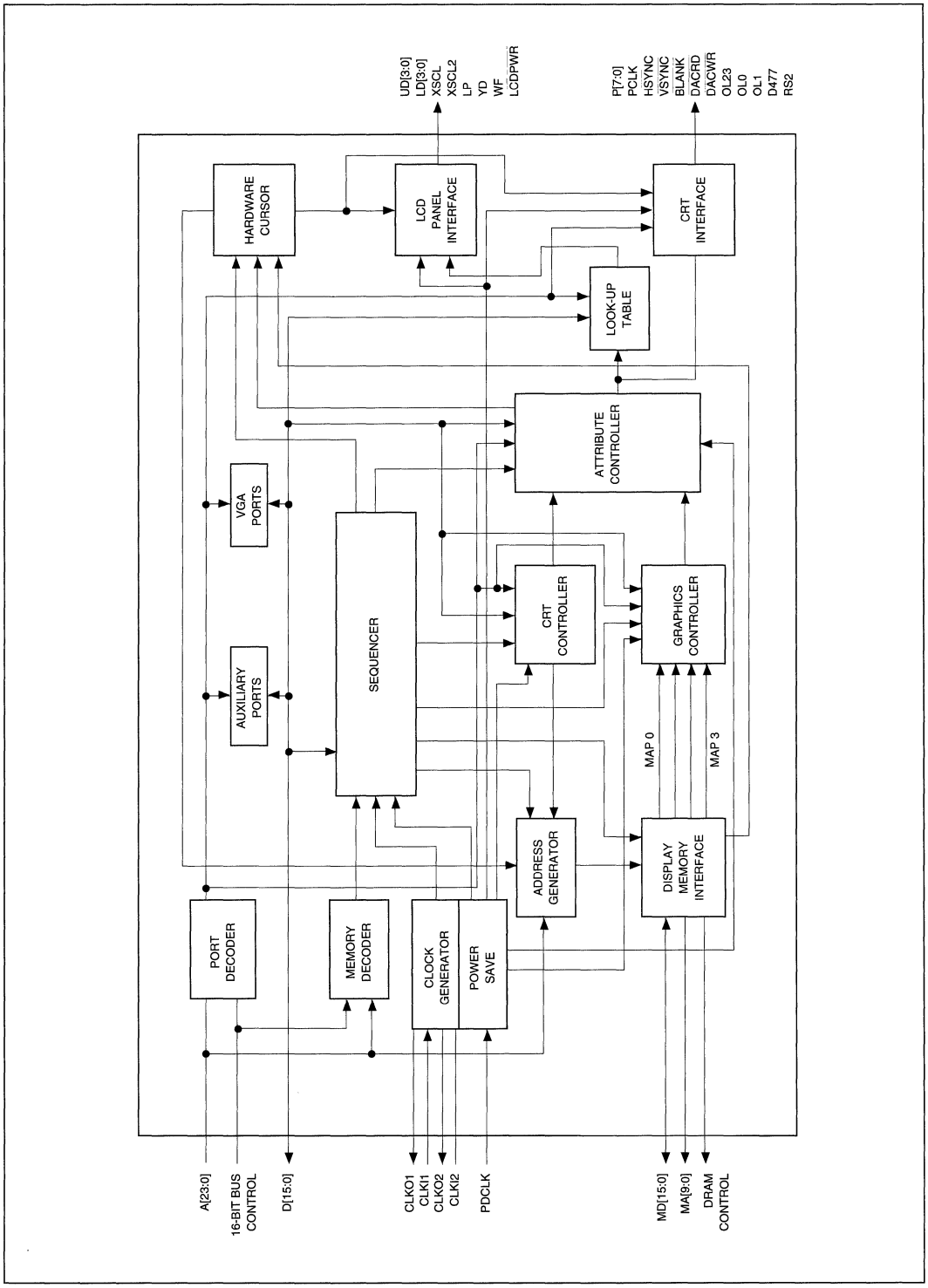
● CRT Display Modes

Mode No.	Mode Type	Font	Characters	Resolution	Displayed Pixels	Colors	Memory Segment
0	Text	8 X 8	40 X 25	320 X 200	640 X 400	16	B800
0+	Text	8 X 14	40 X 25	320 X 350	640 X 350	16	B800
0++	Text	8 X 16	40 X 25	320 X 400	720 X 400	16	B800
1	Text	8 X 8	40 X 25	320 X 200	640 X 400	16	B800
1+	Text	8 X 14	40 X 25	320 X 350	640 X 350	16	B800
1++	Text	8 X 16	40 X 25	320 X 400	720 X 400	16	B800
2	Text	8 X 8	80 X 25	640 X 200	640 X 400	16	B800
2+	Text	8 X 14	80 X 25	640 X 350	640 X 350	16	B800
2++	Text	8 X 16	80 X 25	720 X 400	640 X 400	16	B800
3	Text	8 X 8	80 X 25	640 X 200	640 X 400	16	B800
3+	Text	8 X 14	80 X 25	640 X 350	640 X 350	16	B800
3++	Text	8 X 16	80 X 25	720 X 400	640 X 400	16	B800
4	Graphics	N/A	N/A	320 X 200	640 X 400	4	B800
5	Graphics	N/A	N/A	320 X 200	640 X 400	4	B800
6	Graphics	N/A	N/A	640 X 200	640 X 400	2	B800
7	Text	8 X 14	80 X 25	640 X 350	640 X 350	2	B000
7+	Text	9 X 16	80 X 25	720 X 400	720 X 400	2	B000
0D	Graphics	N/A	N/A	320 X 200	640 X 400	16	A000
0E	Graphics	N/A	N/A	640 X 200	640 X 400	16	A000
0F	Graphics	N/A	N/A	640 X 350	640 X 350	2	A000
10	Graphics	N/A	N/A	640 X 350	640 X 350	16	A000
11	Graphics	N/A	N/A	640 X 480	640 X 480	2	A000
12	Graphics	N/A	N/A	640 X 480	640 X 480	16	A000
13	Graphics	N/A	N/A	320 X 200	640 X 400	256	A000
100	Graphics	N/A	N/A	640 x 400	640 x 400	256	A000
101	Graphics	N/A	N/A	640 x 480	640 x 480	256	A000
108	Text	8 x 8	80 x 60	640 X 480	640 X 480	16	B8s00

■ SUPPORTED LCD INTERFACES

8-Bit Interface				4-Bit Interface	
Dual Panel		Single Panel		Single Panel	
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
640	400 480	640	1 to 480	320 480 640	200 240 320 400 480

■ BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

The Sequencer

The Sequencer generates internal signals to synchronize the operation of the chip as well as the signals to control the timing of the display DRAM. The Sequencer also arbitrates between CPU and video display accesses to the DRAM. It contains registers that allows selection of character font set, control the structure of the video memory and allow write masking of the individual plane of memory.

CRT Controller

The CRT Controller generates the horizontal and vertical synchronization signals for the CRT, single panel or dual panel LCD display and character and/or pixel addresses for display data from DRAM.

CRT Interface

The CRT interface aligns CRT signals to the Pixel Clock and generates the I/O Control signals for CPU access to the RAMDAC.

Address Generator

The Address Generator takes the display and refresh addresses from the CRT Controller and converts them into RAS and CAS addresses for the display DRAM, and multiplexes these display accesses with CPU memory accesses.

Attributes Controller

The Attributes Controller takes in pixel and attribute information from the Graphics Controller and display DRAM and formats the data into pixel information which then passes through the lookup table. It also controls display character attributes such as blink, underline and horizontal pixel panning.

Graphics Controller

The Graphics Controller supplies display memory data to the Attributes Controller during display time and provides data translation between the CPU bus and the display memory during CPU read or write access cycles.

Display Memory Interface

The Display Memory Interface is a bridge by which the chip communicates with the DRAM. It contains buffers that are used to store recently fetched DRAM data.

Memory Decoder

The Memory Decoder monitors the CPU-bus activity and decodes cycles for the display DRAM. It supplies memory access control signals to the Sequencer.

Port Decoder

The Port Decoder decodes CPU-bus I/O cycles to provide enable and write strobes for the on-chip I/O registers.

Auxiliary Ports

The Auxiliary Ports are I/O registers used to control functions of the chip beyond the basic VGA register set. Registers are included for controlling the LCD interface circuits as well as the power save modes.

VGA Ports

The VGA Ports contain the Miscellaneous Output Status register and the Video Subsystem Enable register used in VGA mode.

Clock Generation

The Clock Generation contains oscillator support for external crystals.

Power Save

The Power Save block contains the logic to implement six software controlled and one hardware controlled power down modes.

Lookup Table

The Lookup Table consists of a memory array of 256 locations of 12 bits each and hardware to convert VGA palette writes to gray-scale values.

LCD Interface

The LCD Interface block converts the display video data from the Lookup Table into LCD display data. It also generates control signals necessary to drive single or dual-panel LCD panels. For monochrome LCD panels, the LCD interface block generates a maximum 64 gray shades through frame rate modulation and dithering techniques. For color LCD panels, the LCD interface block generates 256 simultaneous colors from a possible 4096 colors through frame rate modulation.

Hardware Cursor

The Hardware Cursor block generates a 4 gray shade or color cursor/sprite that can be overlaid on the LCD or CRT display. The cursor is 64 x 64 pixels or optionally expanded to 128 x 128 through pixel replication.

■ DC SPECIFICATIONS

● Absolute Maximum Ratings

Parameters	Symbol	Rating	Units
Supply voltage	V_{DD}	V_{SS} –0.3 to +7.0	V
Input voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	V_{SS} –0.3 to V_{DD} +0.3	V
Operating temperature	T_{OPR}	0 to +70	°C
Storage temperature	T_{STG}	–65 ~ +150	°C
Soldering temperature/time	T_{SOL}	–260 for 10 sec max at lead	°C

● Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Supply voltage	HV_{DD}	V_{SS} = 0V	4.5	5.0	5.5	V
Supply voltage	LV_{DD}	V_{SS} = 0V	3.0	3.3	3.6	V
Input voltage	V_{IN}	V_{SS}	V_{SS}	—	V_{DD}	V
Operating temperature	T_{OPR}		0	25	70	°C

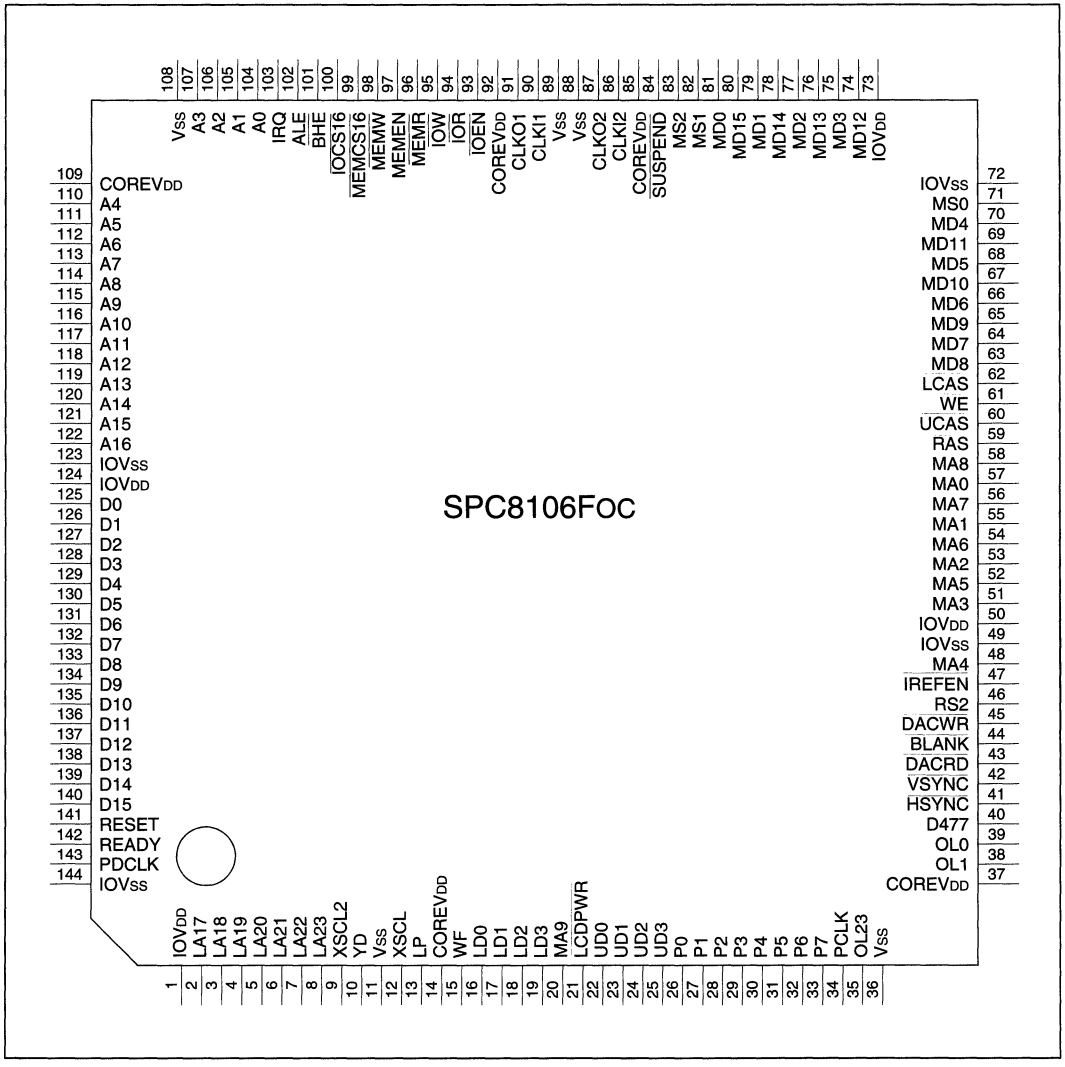
● Input Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low level input voltage (CMOS inputs)	V_{IL}	V_{DD} =MIN			1.0	V
High level input voltage (CMOS inputs)	V_{IH}	V_{DD} = MAX	3.5			V
Low level input voltage (TTL inputs)	V_{IL}	V_{DD} =MIN			0.8	V
High level input voltage (TTL inputs)	V_{IH}	V_{DD} = MAX	2.0			V
Positive-going threshold (CMOS Schmitt inputs)	V_{T+}	V_{DD} = 5.0V			4.0	V
Negative-going threshold (CMOS Schmitt inputs)	V_{T-}	V_{DD} = 5.0V	0.8			V
Hysteresis voltage (CMOS Schmitt inputs)	V_H	V_{DD} = 5.0V	0.3			V
Positive-going threshold (CMOS Schmitt inputs)	V_{T+}	V_{DD} =5.0V			3.0	V
Negative-going threshold (CMOS Schmitt inputs)	V_{T-}	V_{DD} =5.0V	0.6			V
Hysteresis voltage (CMOS Schmitt inputs)	V_H	V_{DD} = 5.0V	0.1			V
Input leakage current	I_{IZ}	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1		1	µA
Input pin capacitance	C_{IN}			8		pF
Pull up resistance	R_{PU2}	V_{DD} = 5.0V	50	100	200	KΩ
Pull up resistance	R_{PU3}	V_{DD} = 5.0V	100	200	400	KΩ
Pull down resistance	R_{PD}	V_{DD} = 5.0V	100	200	400	KΩ

● Output Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low level output current	I_{OL2}	$V_{OL} = V_{SS} + 0.4V$ TS2	6.0			mA
High level output current	I_{OH2}	$V_{OH} = V_{DD} - 0.4V$ TS2	–2.0			mA
Low level output current	I_{OL3}	$V_{OL} = V_{SS} + 0.4V$ TS3	12.0			mA
High level output current	I_{OH3}	$V_{OH} = V_{DD} - 0.4V$ TS3	–4.0			mA
Low level output current	I_{OL4}	$V_{OL} = V_{SS} + 0.4V$ TS4	24.0			mA
High level output current	I_{OH4}	$V_{OH} = V_{DD} - 0.4V$ TS4	–8.0			mA
Output leakage current	I_{OZ}	$V_{OH} = V_{DD}$ or $V_{OL} = V_{SS}$	–1		1	μA
Output pin capacitance	C_{OUT}			8		pF
Bidirectional pin capacitance	C_{BID}			10		pF

■ SPC8106 PIN OUT



■ PIN DESCRIPTION

Key

A	=	Analog
I	=	Input
O	=	Output
I/O	=	Bi-directional
P	=	Power

CPU Interface

Pin Name	Type	Pin#	Description
A[0:16}, LA[17:23]	I	104..107, 110..122, 2..4, 5..8	CPU bus address inputs. In Suspend Mode, the Address inputs are internally masked off. If the value on MD[5] at RESET = 1, then the ALE input pin is used to internally latch LA[19:17] and A[16:2], allowing these address bits to be driven by the processor address bus. If the value on MD[5] at RESET = 0, then standard ISA address timing is assumed, where pins A[0:16], LA[17:23] should be connected to the ISA bus signals SA[0:16], LA[17:23] respectively.
ALE	I	102	ISA Bus Address Latch Enable. In Suspend Mode the ALE input is disabled. If the value on MD[5] at RESET = 1, then the ALE input is used to internally latch LA[19:17] and A[16:2], allowing these address bits to be driven by the processor address bus. In this mode, the processor ADS# output should be connected to this pin. If the value on MD[5] at RESET = 0, then standard ISA address timing is assumed, and only the LA[19:17] inputs are internally latched.
D[0:15]	I/O	125..140	16 bit ISA-Bus data bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
MEMEN	I	97	ISA Bus Memory Enable. This signal should be connected to the REFRESH# signal on the ISA bus. When this signal is low (e.g. during a system memory refresh cycle), memory address decoding is disabled.
IOR#	I	94	ISA Bus I/O Read Strobe. In Suspend Mode the IOR# input is disabled.
IOW#	I	95	ISA Bus I/O Write Strobe. In Suspend Mode the IOW# input is disabled.
MEMR#	I	96	ISA Bus System Memory Read Strobe. In Suspend Mode the MEMR# input is disabled.
MEMW#	I	98	ISA Bus System Memory Write Strobe. In Suspend Mode the MEMW# input is disabled.
IOEN#	I	93	ISA Bus I/O Enable. This input should be connected to the ISA bus AEN signal. When this signal is high, I/O address decoding is disabled. In Suspend Mode the IOEN# input is disabled.
READY	O	142	ISA Bus READY signal. This output is driven low to force the CPU to insert wait states during memory cycles. READY is released to high-Z after a transfer is complete.
RESET	I	141	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state.
IRQ	O	103	ISA Bus Vertical Interrupt. When enabled, a Vertical Retrace Interrupt will cause this signal to be driven from a logic 0 state to a logic 1(rising-edge triggered interrupt). Once set, this interrupt must be cleared by a bit in the CRTC registers. A control bit in the Auxiliary Registers allows this output to be optionally disabled (tri-stated). This pin also is used for the output of the NAND tree in pin test mode.
MEMCS16#	O	99	ISA Bus Memory Chip Select 16. Address inputs LA[23:17] are decoded to drive this output low when a valid memory address (AXXXXh, BXXXXH) appears on the bus.
IOCS16#	O	100	ISA Bus I/O Chip Select 16. Address inputs A[15:0] and IOEN# are decoded to drive this output low when a valid SPC8106F0C I/O register address appears on the bus. Note that I/O addresses 3C6h-3C9h do not result in IOCS16# being driven low (i.e. RAMDAC and internal LUT register reads and writes are 8 bit cycles.
BHE#	I	101	ISA Bus Byte High Enable. In Suspend Mode the BHE# input is disabled.

Video Memory Interface

Pin Name	Type	Pin#	Description
MA[0:9]	O	57, 55, 53, 51, 48, 52, 54, 56, 58, 20	Multiplexed row/column address bits for video display memory.
MD[0:15]	I/O	81, 79 77, 75 70, 68 66, 64 63, 65 67, 69, 74, 76, 78, 80	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET is high, or when the Sequencer is in a reset state. On the falling edge of RESET, the values on MD[3:0] and MD[12:9] are latched into a read-only Auxiliary Register and are available to be read as configuration inputs. Also, the value on MD[8:4] and MD[15:13] are used to configure various hardware options. See "Summary of Configuration Options" for details.
RAS#	O	59	DRAM Row Address Strobe for single 256Kx16 DRAM.
LCAS# (LWE#)	O	62	Multiple Function: DRAM Column Address Strobe for low byte (LCAS#). For alternate function see "Multiple Function Pin Descriptions" on page 16.
UCAS# (CAS#)	O	60	Multiple Function: DRAM Column Address Strobe for high byte (UCAS#). For alternate function see "Multiple Function Pin Descriptions" on page 16.
WE# (UWE#)	O	61	Multiple Function: DRAM Write Enable Strobe (WE#). For alternate function see "Multiple Function Pin Descriptions" on page 16.

Clock Inputs

Pin Name	Type	Pin#	Description
CLKI1	I	90	This pin, along with CLKO1 is the 25.175 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO1	O	91	This pin, along with CLKI1 is the 25.175 MHz 2- terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.
CLKI2	I	86	This pin, along with CLKO2 is the 28.322 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO2	O	87	This pin, along with CLKI2 is the 28.322 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.

LCD Panel Interface

Pin Name	Type	Pin#	Description
YD	O	10	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	O	13	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O	12	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
XSCL2	O	9	This second shift clock is used together with XSCL in 8-bit single color panel mode to shift in alternate sets of display data. XSCL2 is also used alone as the shift clock in 8-bit dual color panel mode and 4-bit single color panel mode.
UD[0:3]	O	22..25	Upper panel display data for dual panel - dual drive mode. For 8-bit single panel-single drive mode, these bits are the most significant 4-bits of the 8-bit output data to the panel (data[7:4]). For 4-bit single panel mode, these bits are the 4 bits of data output to the panel. For 16-bit LCD modes, these outputs are the multiplexed upper panel data if MD[7] = 1 at RESET, or the lower nibble of the upper panel data if MD[7]=0 at RESET.
UD[4:7]	O	26..29	When MD[7]=0 at RESET, these pins are the upper nibble of the 16-bit LCD mode upper panel data.
LD[0:3]	O	16..19	Lower panel display data for dual panel-dual drive mode. For 8-bit single panel-single drive mode, these bits are the least significant 4 bits of the 8-bit output data to the panel (data[3:0]). For 4-bit single panel mode, these outputs are driven low. For 16-bit LCD modes, these outputs are the multiplexed lower panel data if MD[7]=1 at RESET, or the lower nibble of the lower panel data if MD[7]=0 at RESET.
LD[4:7]	O	30..33	When MD[7]=0 at RESET, these pins are the upper nibble of the 16-bit LCD mode lower panel data.
LCDPWR#	O	21	LCD power control. In normal operation this signal is driven low to enable an external LCD power supply. This signal is driven high when the chip is put into any power save mode, when Auxiliary Register 06 bit 0 is set to 1, or when the Sequencer is in a reset state. It can be used externally to turn off the panel supply voltage and backlight. After a RESET, this signal is held high until the CRTC is programmed and running.
WF	O	15	LCD Backplane Bias signal. This output toggles once every n LP periods, as programmed in Auxiliary Register [0D].

External CRT/RAMDAC Interface

Pin Name	Type	Pin#	Description
P[0:7]	O	26..33	When MD[7]=1 at RESET, these pins are the Pixel Data outputs. These 8 bits are connected to the pixel select inputs of the external RAMDAC.
PCLK	O	34	Pixel Clock. Pixel data is clocked out of the chip on the falling edge of PCLK.
BLANK#	O	44	Blank output. This output is clocked out on the falling edge of PCLK and is driven low during display blanking periods.
HSYNC#	O	41	Horizontal Sync. This output is clocked out on the falling edge of PCLK and is driven to indicate the horizontal retrace period. The polarity of this signal is determined by a control bit in register 3C2h.
VSYNC#	O	42	Vertical Sync. This output is clocked out on the falling edge of PCLK and is driven to indicate the vertical retrace period. The polarity of this signal is determined by a control bit in register 3C2h.
DACRD#	O	43	RAMDAC Read Stobe. This signal goes low when a valid read access to the VGA RAMDAC is decoded by the chip.
DACWR#	O	45	RAMDAC Write Stobe. This signal goes low when a valid write access to the VGA RAMDAC is decoded by the chip.
RS2	O	46	Register Select 2 output. This output should be connected to the RS2 input of the RAMDAC (Bt477 or equivalent). The logic level on this output may be set by setting Auxiliary Register [0B] bit 3. This signal is required to allow CPU access the control and overlay registers of the external RAMDAC.
OL[0:1]	I/O	39, 38	Multiple Function: Overlay Select outputs 1:0. When MD[13] =0 at RESET, these pins are outputs used to provide sprite/HW cursor function on the CRT display. In this case, these outputs should be connected to the OL[0:1] inputs of the RAMDAC (Bt477 or equivalent). They are used by the sprite circuitry to access the overlay registers in the RAMDAC. For alternate function see "Multiple Function Pin Descriptions" on page 16.
OL23	O	35	Overlay Select output 2/3. This output should be connected to both the OL2 and OL3 inputs of the RAMDAC (Bt477 or equivalent). This signal is used by the sprite circuitry to access the overlay registers in the RAMDAC.
D477	O	40	477 Control Signal. This output should be connected to the 477/471 input of the RAMDAC (Bt477 or equivalent). This signal is used to access the control register of the RAMDAC and to allow it to be powered down. The logic level on this output can be controlled by setting Auxiliary Register [0B] bit 4, and is also controlled by the power save logic.
IREFEN#	O	47	IREF Enable outout. This signal is used to control the external current reference source required by the RAMDAC, allowing powering down the analog circuitry when not required. When this signal is driven low, the external current reference should be enabled. When this signal is high, the external current reference should be shut off.
MS[2:0]	I/O	83, 82, 71	Monitor Sense inputs. These signals should be connected to the monitor sense lines from the CRT monitor cable. The status of these bits is readable in Auxiliary Register [08] bits 2:0, and is used by BIOS software to determine the presence and type of monitor connected. Optionally, the SENSE output of the RAMDAC may be connected to one of these inputs to allow the BIOS to read the SENSE signal and detect the monitor. MS[2:1] can be forced low by the DCC2 monitor support bits in Auxiliary Register [10] bits 1:0.

Power Save Mode Control

Pin Name	Type	Pin#	Description
SUSPEND#	I	84	A low level on this pin puts the chip into a hardware power down mode. The SUSPEND# signal overrides any software initiated power down modes, and disables the ISA-Bus interface inputs except RESET. Address and Data inputs are also masked when this signal is low. When in Suspend Mode the UD(3:0), LD(3:0), XSCL, XSCL2, LP, YD and WF signals are driven into a high impedance or low state (configurable) and the LCDPWR# signal is driven high.
PDCLK	I	143	Power Down Clock. This input may be used to provide a low frequency clock for generating refresh in Power Save Modes 4 and Suspend, as an optional alternative to using the pixel clock or sMEMEN input as the refresh clock source. This clock input should be driven by either a 32kHz 50% duty cycle clock source, or a 64kHz clock source with a high period as short as possible (but> minimum RAS low pulse width) to minimize DRAM current consumption during refresh. The PDCLK input is used to directly generate the RAS and CAS pulses during Power Save Mode 4 and Suspend.

Power Supply

Pin Name	Type	Pin#	Description
$COREV_{DD}$	P	14, 37, 85, 92, 109	V_{DD} supply for core logic.
IOV_{DD}	P	1, 50, 73, 124	V_{DD} supply for interface pins.
V_{SS}	P	11, 36, 88, 89, 108	V_{SS} supply for core logic.
IOV_{SS}	P	49, 72, 123, 144	V_{SS} supply for interface pins.

Pin Mapping for Various Display Modes

Pin Name	Display Mode		RGBI	12-bit RGB	TFT	
	CRT	LCD			9-bit	12-bit
YD	None	YD	VSYNC#	VSYNC#	VSYNC#	VSYNC#[a]
LP	None	LP	HSYNC#	HSYNC#	HSYNC#	HSYNC#[a]
WF	None	WF	None (forced 0)	None (forced 0)	DATAEN	DATAEN
XCSL	None	XCSL	PCLK	PCLK	PANCLK	PANCLK
XCSL2	None	XCSL2	None (forced 0)	R[3]	R[2]	R[3]
UD[3]	None	UD[3]	None (forced 0)	B[3]	B[2]	B[3]
UD[2]	None	UD[2]	None (forced 0)	B[2]	B[1]	B[2]
UD[1]	None	UD[1]	None (forced 0)	B[1]	B[0]	B[1]
UD[0]	None	UD[0]	None (forced 0)	R[2]	R[1]	R[2]
LD[3]	None	LD[3]	D[3]	G[3]	G[2]	G[3]
LD[2]	None	LD[2]	D[2]	G[2]	G[1]	G[2]
LD[1]	None	LD[1]	D[1]	G[1]	G[0]	G[1]
LD[0]	None	LD[0]	D[0]	R[1]	R[0]	R[1]
OL0	OL0	None	None	B[0]	None	B[0]
OL1	OL1	None	None	G[0]	None	G[0]
OL23	OL23	None	None	R[0]	None	R[0]

Mixed Voltage Configurations

Core V_{DD}	I/O V_{DD}	
	3.3	5.0
3.3V	OK	OK
5.0V	NO	OK

Summary of Configuration Options

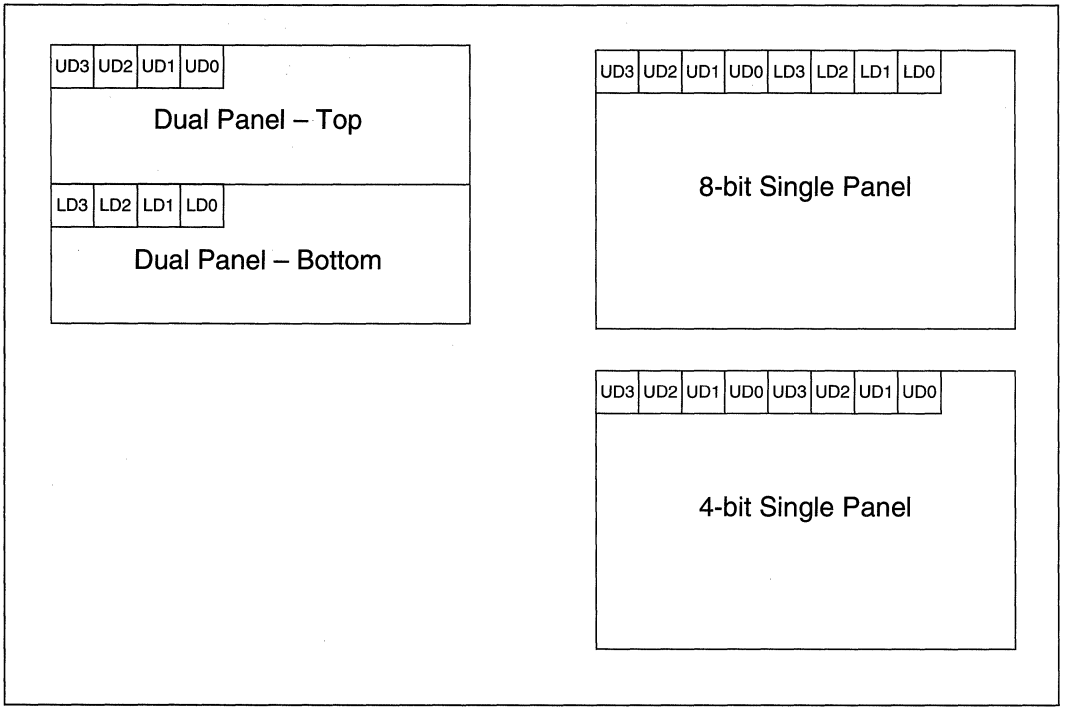
Pin Name	Value on this pin at falling edge of RESET is used to configure: (1/0)
MD [3:0]	Values latched into read-only Aux Reg [0C] bits 3:0 for software use
MD [4]	8-bit I/O interface (1) / 16-bit I/O interface (0)
MD [5]	A [19:2] latched internally by ALE (1) / standard ISA bus ALE – A [16:0] not latched (0)
MD [6]	2 CAS, 1 WE type DRAM (1) / 1 CAS, 2 WE type DRAM (0)
MD [7]	Support 16-bit panel with external logic (1) / support 16-bit panel directly (0)
MD [8]	5 V core operating voltage (1) / 3.3 V core operating voltage (0)
MD [12:9]	Values latched into read-only bits 7:4 of Aux Reg [0C] for software use
MD [13]	Pins 38, 39 used for ext. RC for 32 KHz PDCLK (1) / pins 38, 39 used for OL [1:0] (0)
MD [14]	Internal PDCLK doubling disable (1) / enable (0)
MD [15]	3C3h used as video enable port (1) / 46E8h and 102h used as video enable port (0)

These inputs have internal pullup resistors. Based on the value of the internal pull-ups, the external pull-down resistors if necessary, should be approximately 15K ohm. This value will provide the correct voltage levels on power-up without loading the DRAM Data lines (V_{DD} = 5.0V).

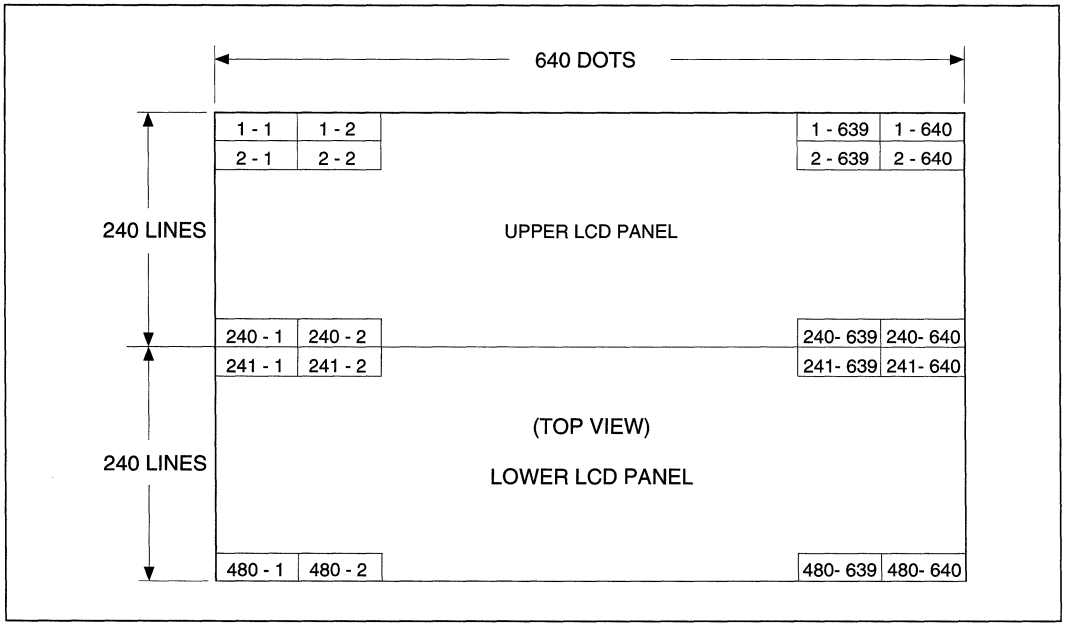
Multiple Function Pin Descriptions

Pin Name	Function	MD Line Status	Functional Description
LCAS#, LWE#	LCAS#	MD [6] = 1	DRAM column address strobe (low byte)
	LWE#	MD [6] = 0	DRAM write strobe (low byte)
UCAS#, CAS#	UCAS#	MD [6] = 1	DRAM column address strobe (high byte)
	CAS#	MD [6] = 0	DRAM column address strobe
WE#, UWE#	WE#	MD [6] = 1	DRAM write strobe
	UWE#	MD [6] = 0	DRAM write strobe (high byte)
OL0, P320	OL0	MD [13] = 0	Overlay bit 0 used for CRT HW Cursor/Sprite support
	P320	MD [13] = 1 MD [14] = 1	32 KHz clock outpur. Used with external RC when using external PDCLK support
OL1, P321	OL1	MD [13] = 0	Overlay bit 1 used for CRT HW Cursor/Sprite support
	P321	MD [13] = 1 MD [14] = 1	32 KHz clock outpur. Used with external RC when using external PDCLK support
P[0:3], UD [4:7]	P[0:3]	MD [7] = 1	Lower nibble of the CRT pixel data outputs
	UD [4:7]	MD [7] = 0	Upper nibble of the 16-bit LCD mode upper panel data
P[4:7], LD [4:7]	P[4:7]	MD [7] = 1	Upper nibble of the CRT pixel data outputs
	LD [4:7]	MD [7] = 0	Upper nibble of the 16-bit LCD mode lower panel data

Illustrated below are the display data output which are output from the UD0 to UD3, LD0/UD4 to LD3/UD7 and the display on the panel:

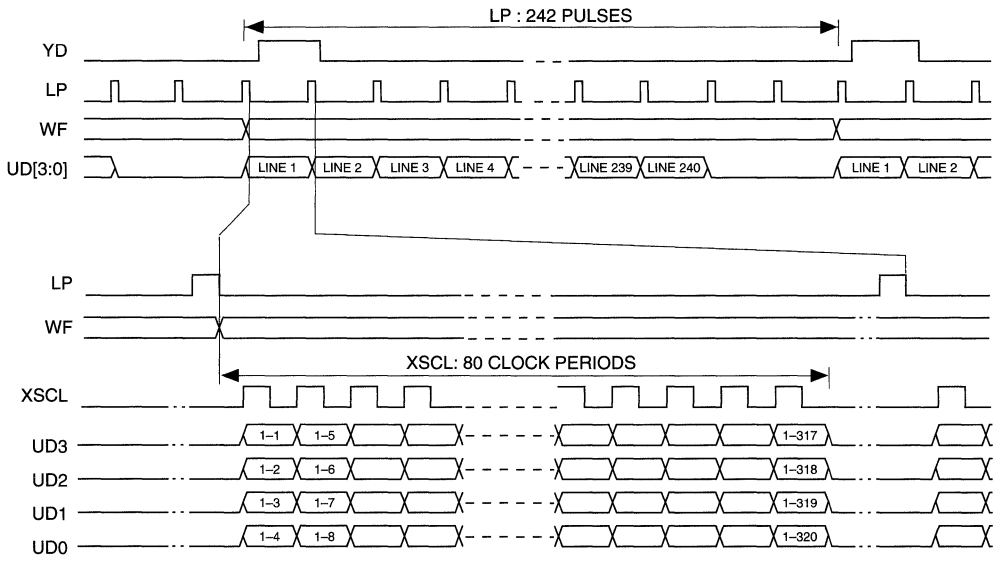


■ LCD Panel Pixels



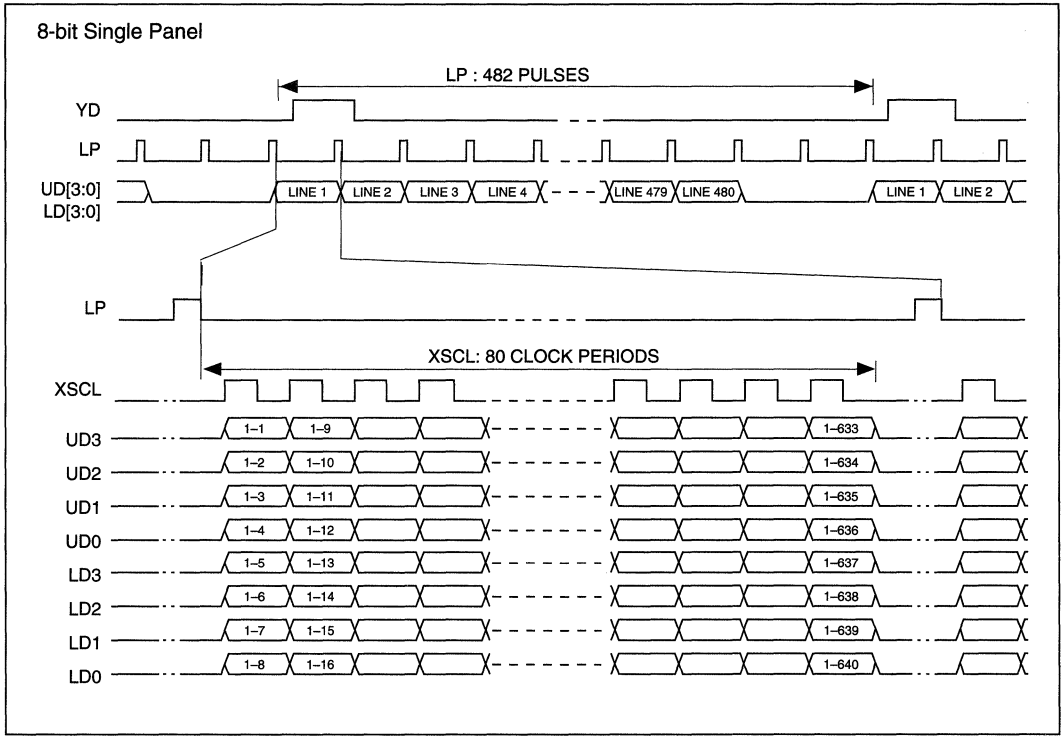
■ Monochrome Passive STN LCD Panel Interface

4-bit Single Panel

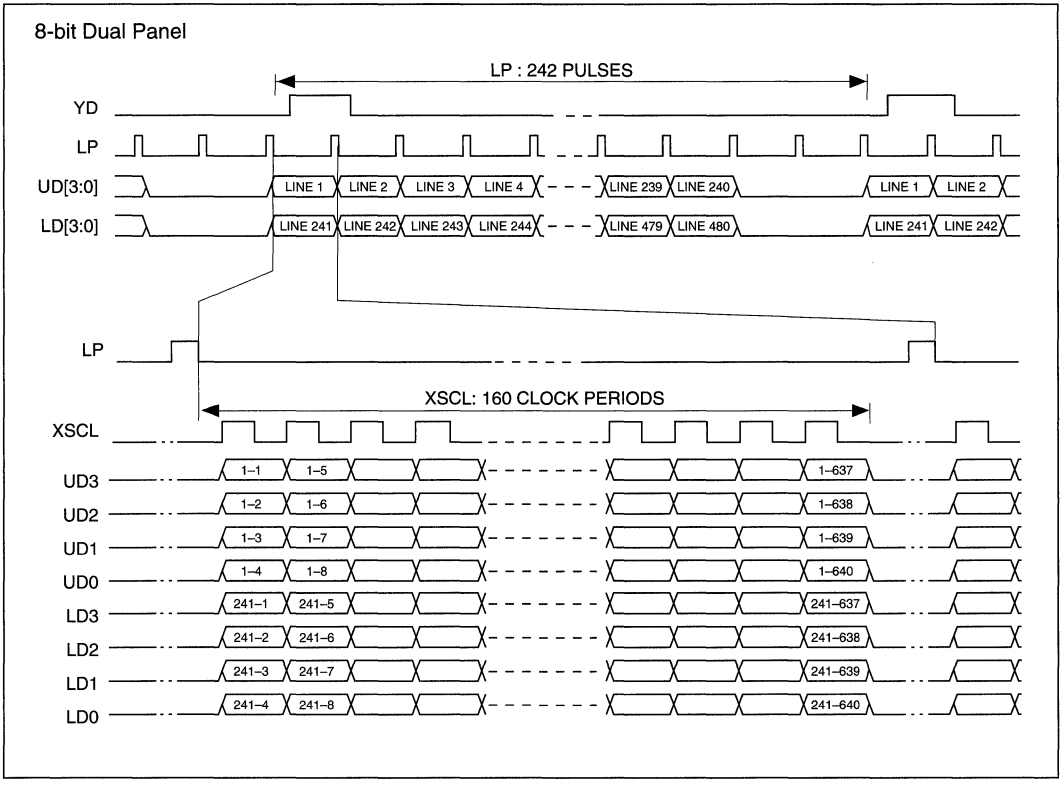


Example timing for 320 × 240 panel

■ Monochrome Passive STN LCD Panel Interface

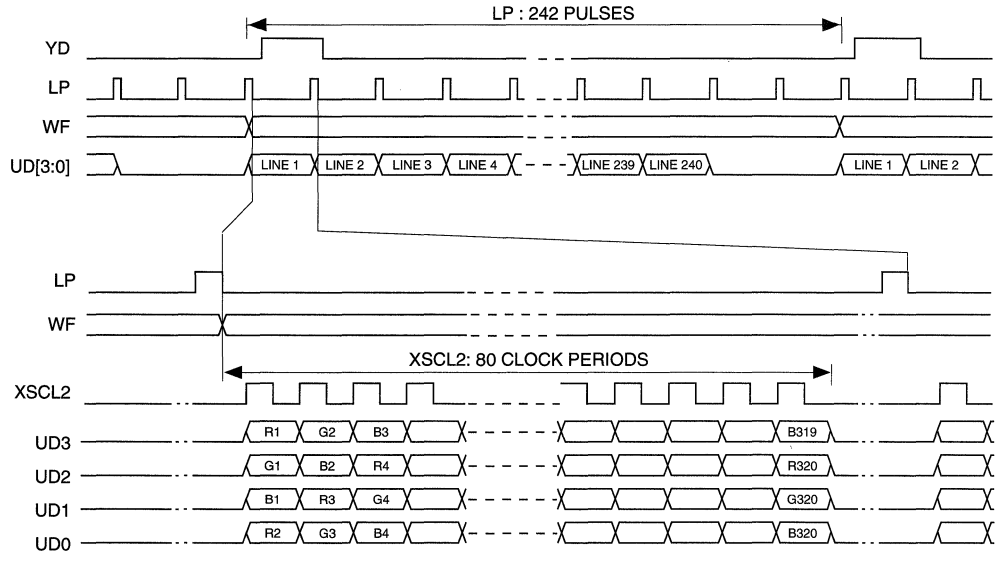


■ Monochrome Passive STN LCD Panel Interface



■ Color STN LCD Panel Interface

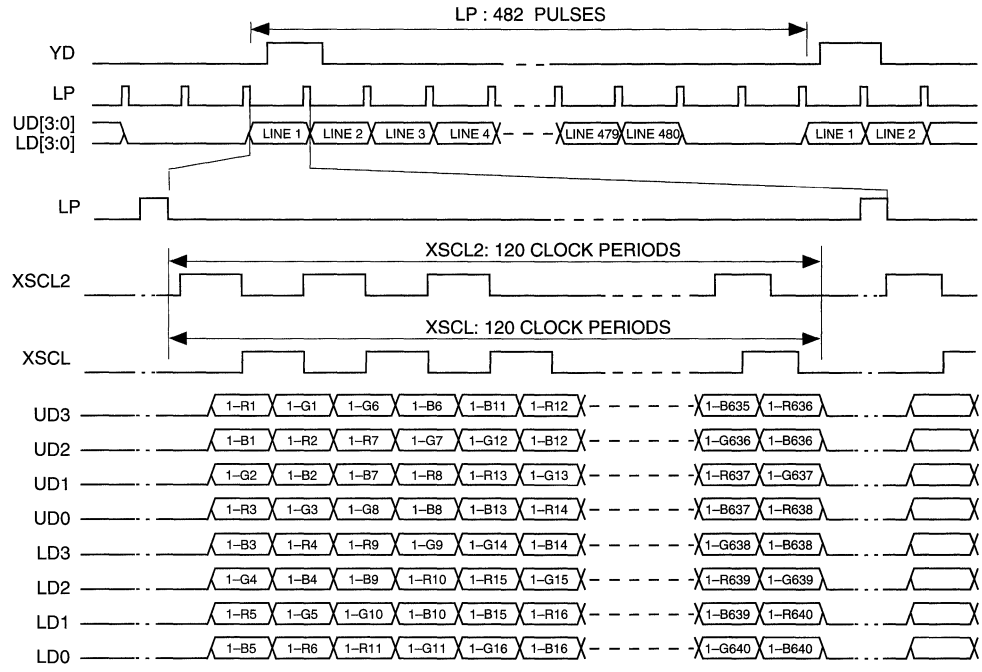
4-bit Single Panel



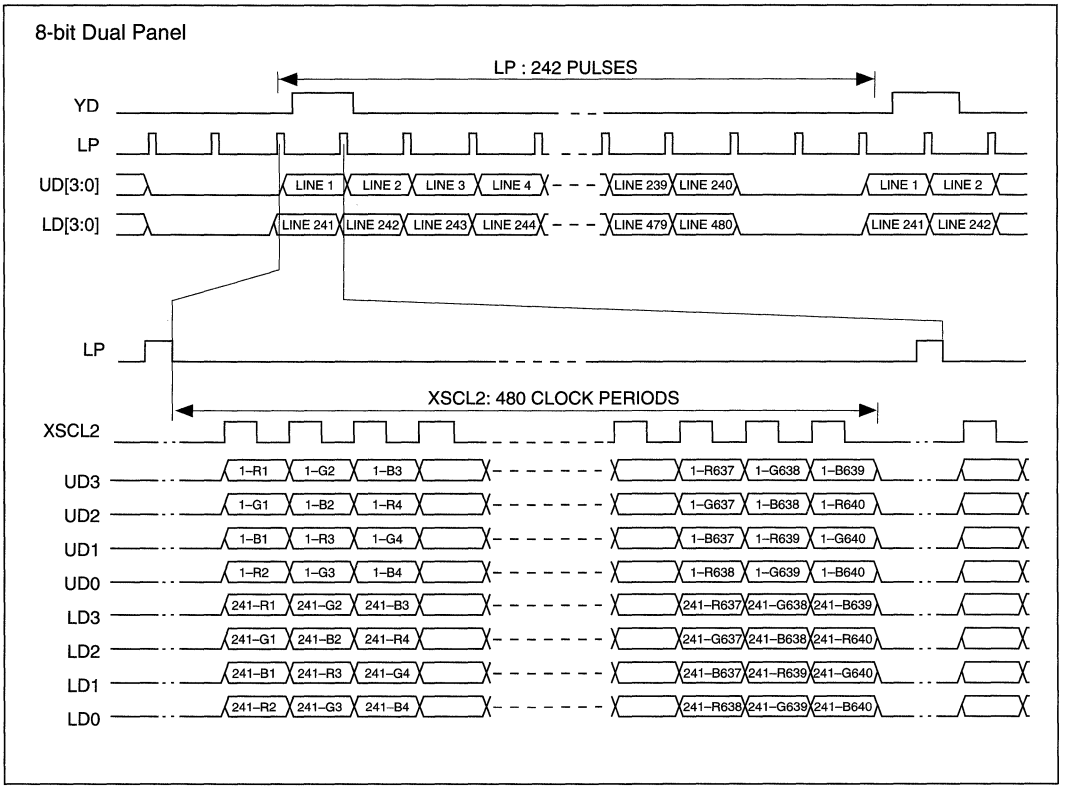
Example timing for 320 × 240 panel

■ Color STN LCD Panel Interface

8-bit Single Panel

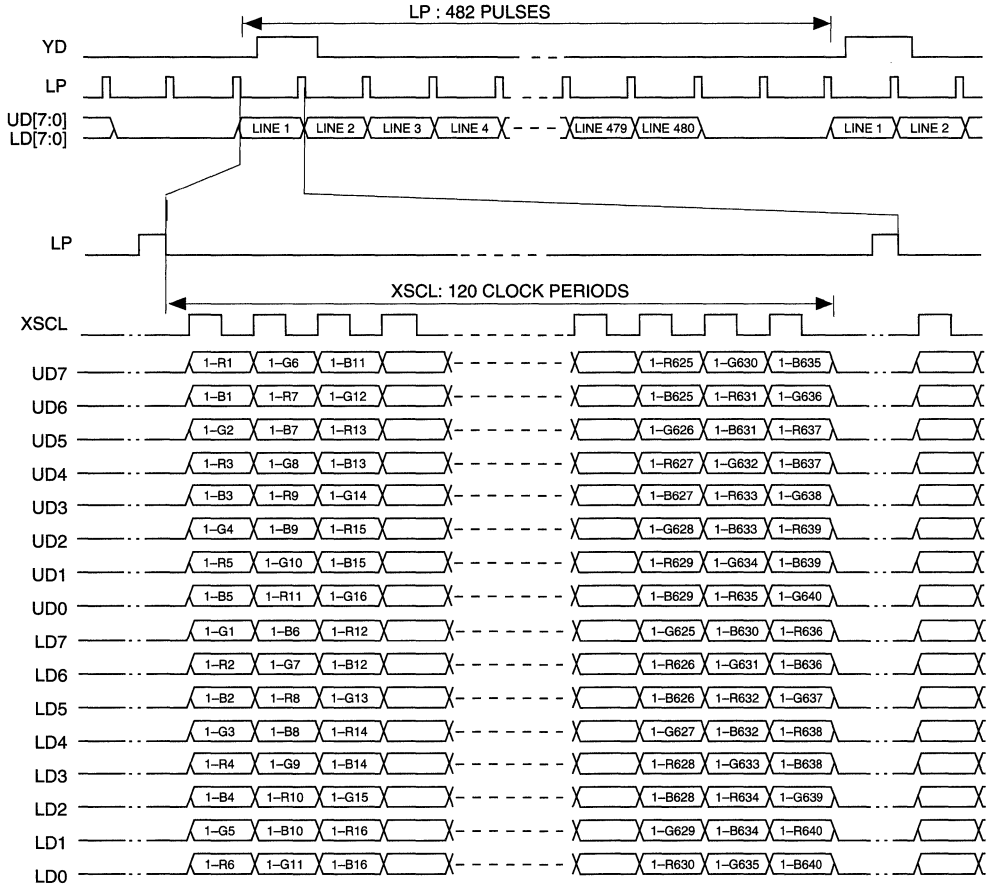


■ Color STN LCD Panel Interface



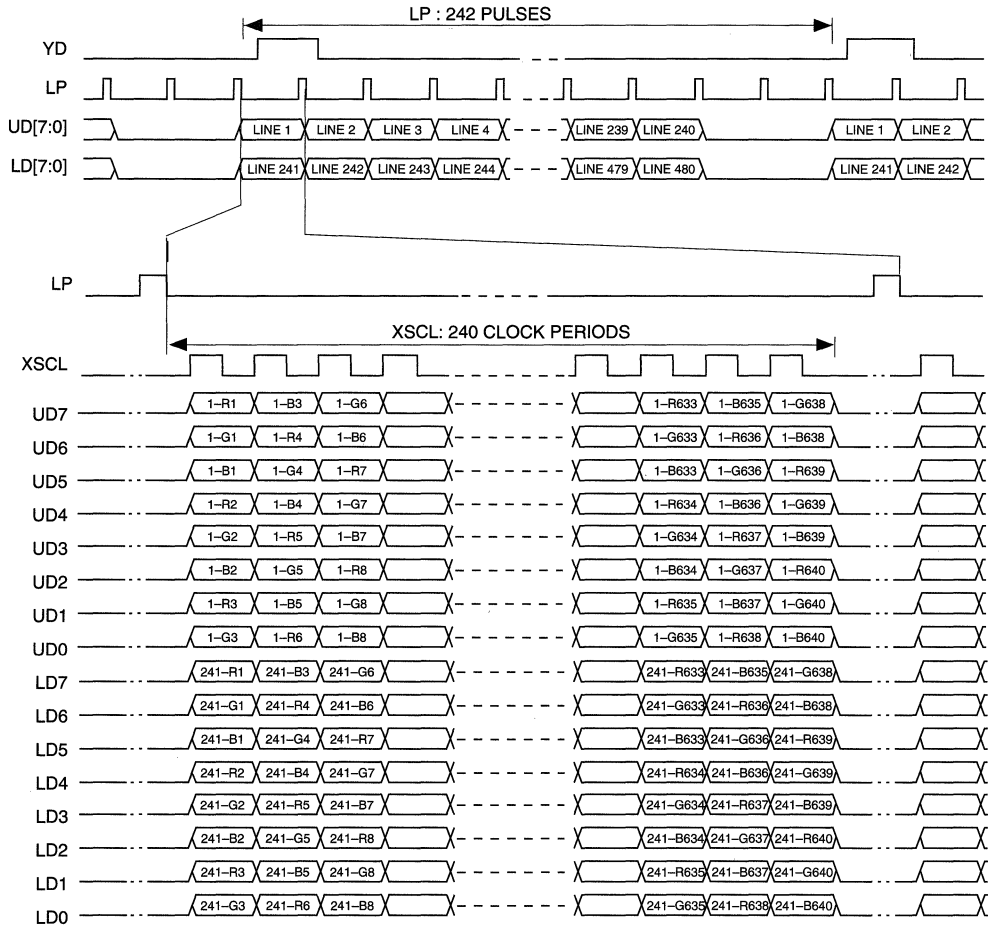
■ Color STN LCD Panel Interface

16-bit Single Panel



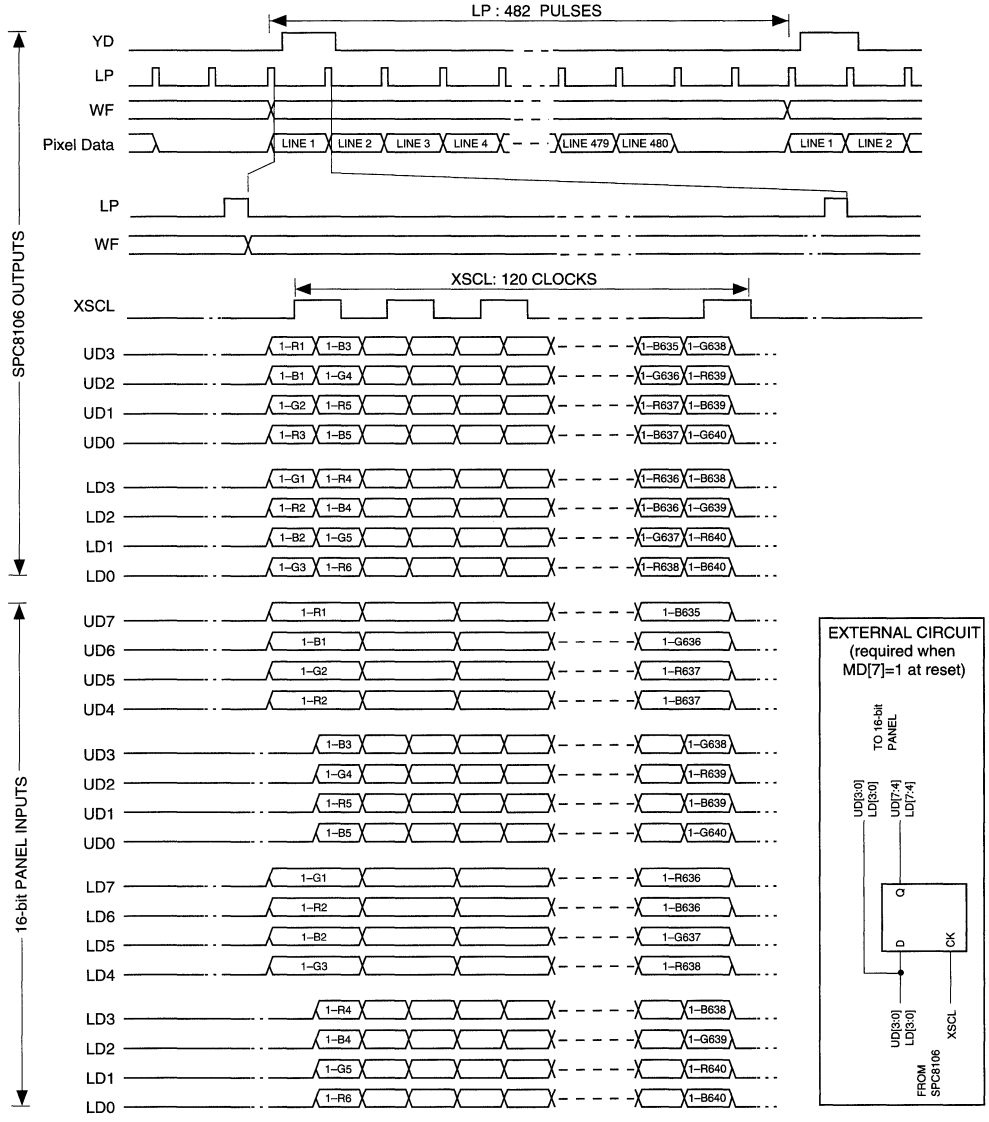
■ Color STN LCD Panel Interface

16-bit Dual Panel



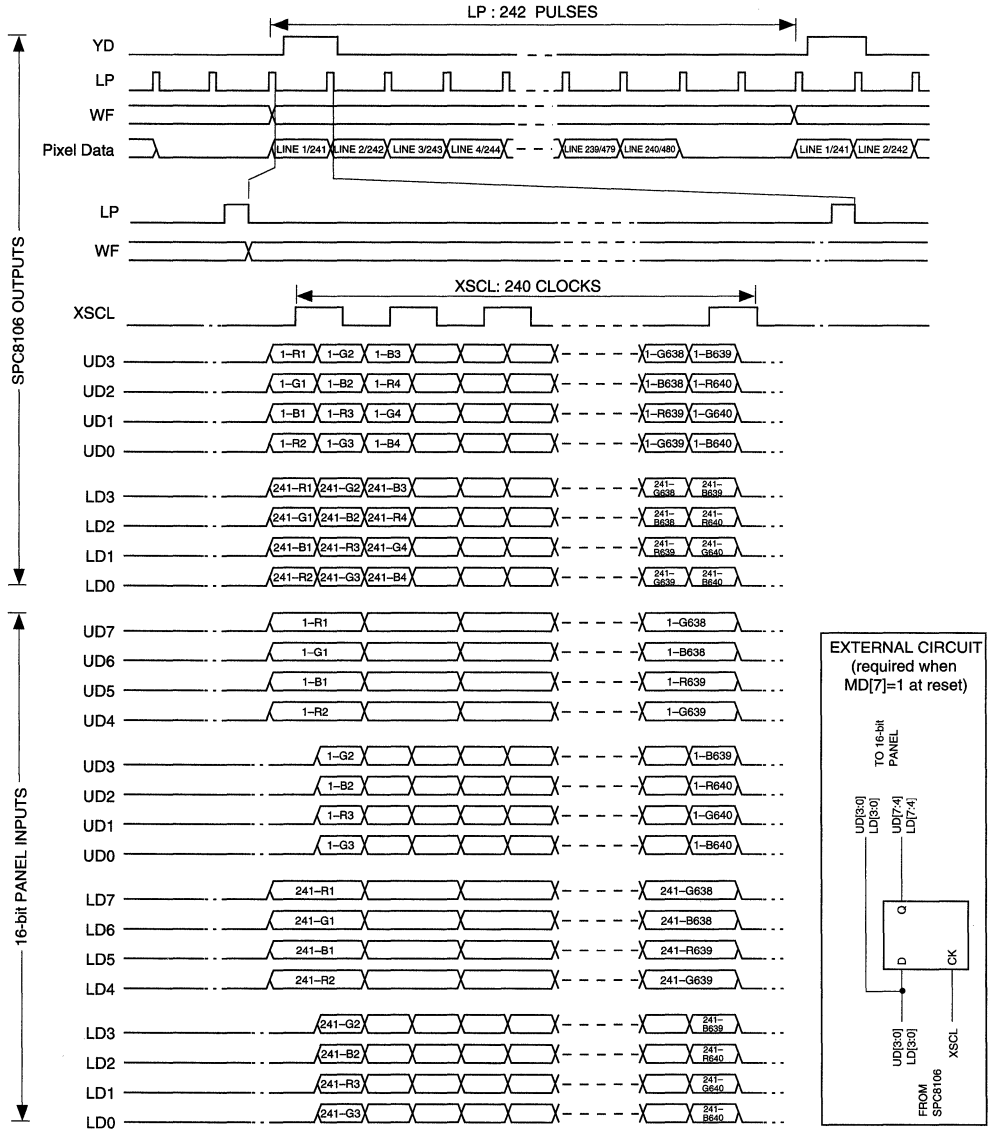
■ Color STN LCD Panel Interface

16-bit Single Panel with External Circuit



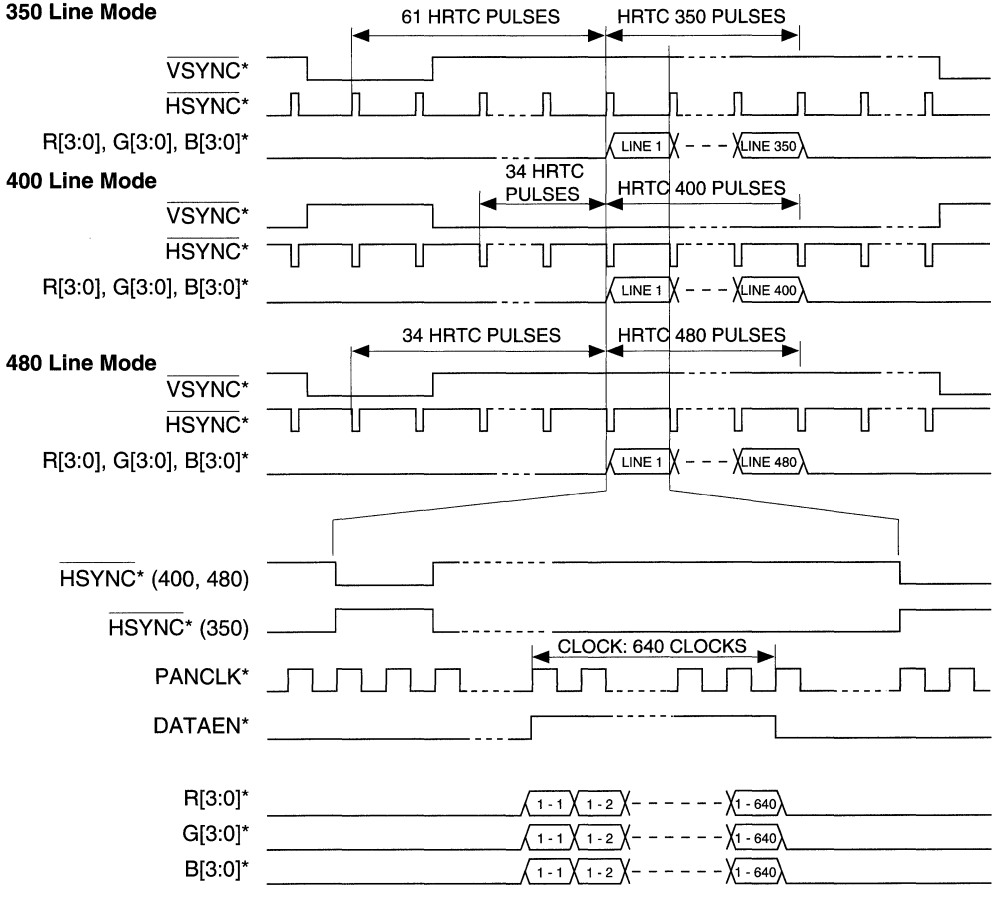
■ Color STN LCD Panel Interface

16-bit Dual Panel with External Circuit



■ Color TFT Panel Interface

Auxiliary Register [00] bit 5=1 and Auxiliary Register [0B] bit 1=1

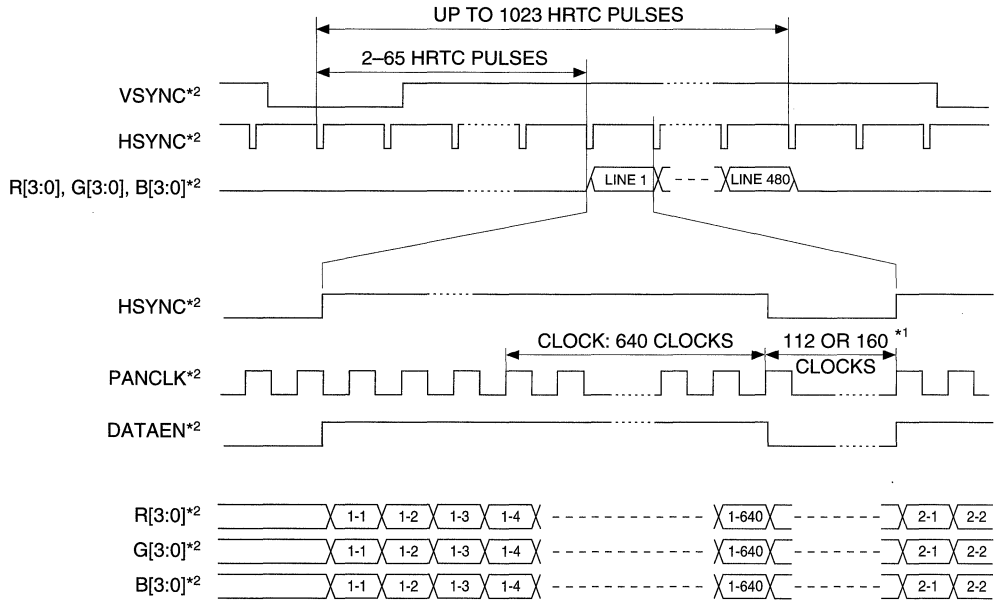


9-bit panels use data bits [2:0]

* Refer to "Pin Mapping for Various Display Modes" on page 15 for actual pin names

■ Color TFT Panel Interface

Auxiliary Register [00] bit 5=1 and Auxiliary Register [0B] bit 1=0



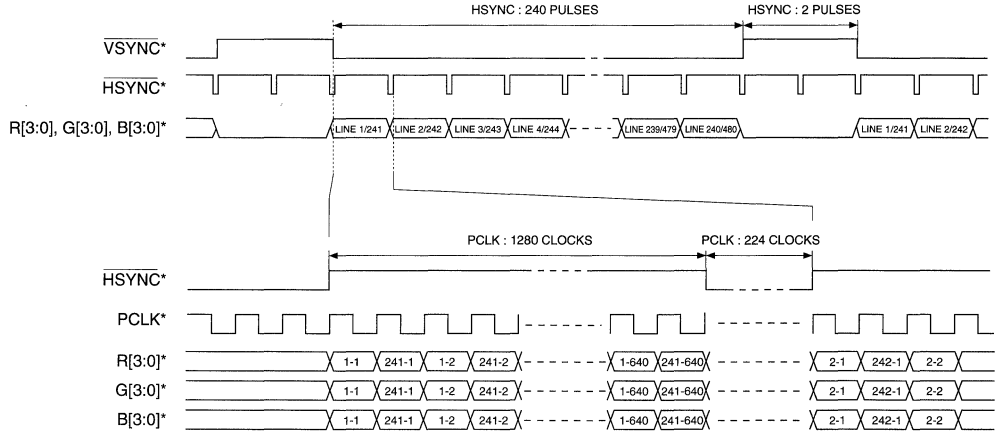
9-bit panels use data bits [2:0]

*1: This number is controlled by Auxiliary Register [06] bit 2

*2: Refer to "Pin Mapping for Various Display Modes" on page 15 for actual pin names

■ RGB Mode Panel Interface

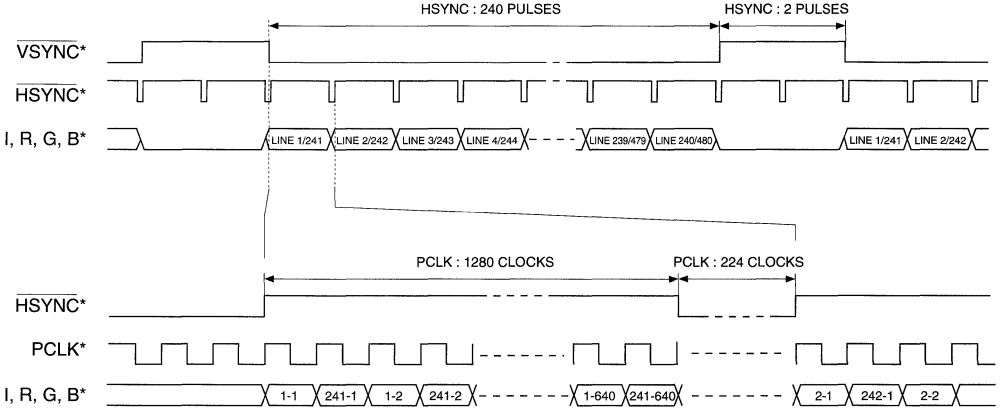
12-bit RGB Mode Panel



* Refer to "Pin Mapping for Various Display Modes" on Page 15 for actual pin names.

■ RGBI Mode Dual Panel Interface

RGBI Mode Dual Panel

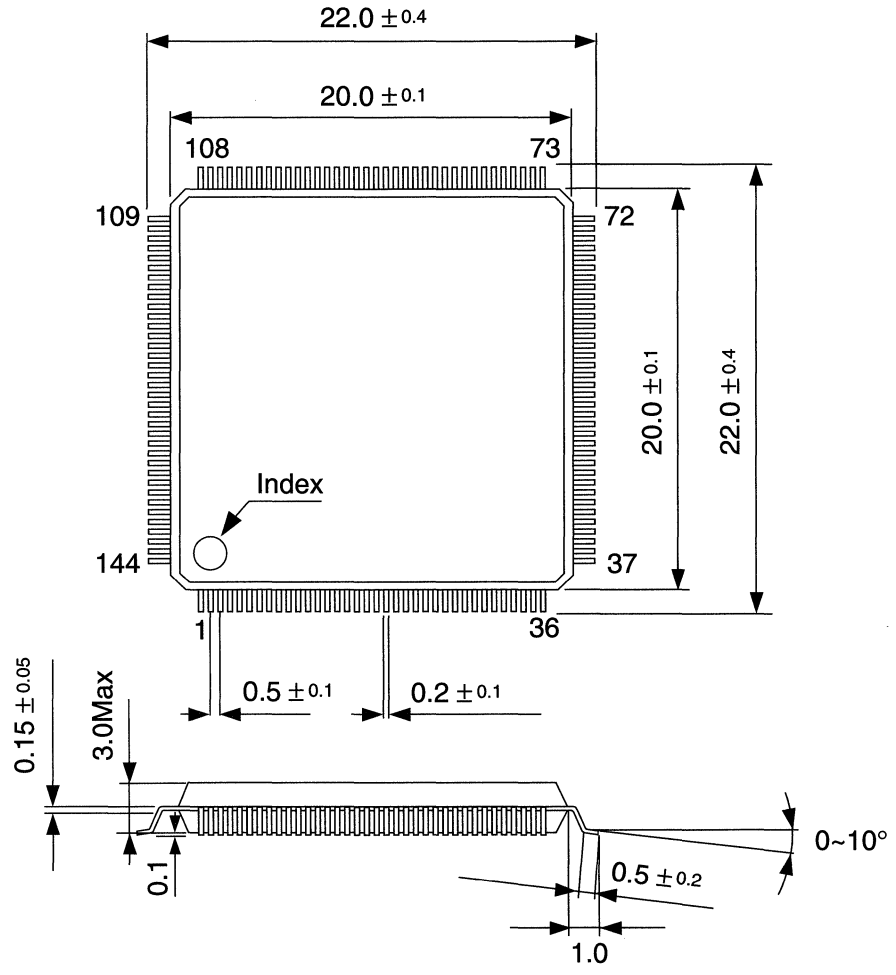


* Refer to "Pin Mapping for Various Display Modes" on Page 15 for actual pin names.

■ PACKAGE DIMENSIONS

QFP17-144 pin

Unit: mm



LOW VOLTAGE VGA LCD CONTROLLER

■ DESCRIPTION

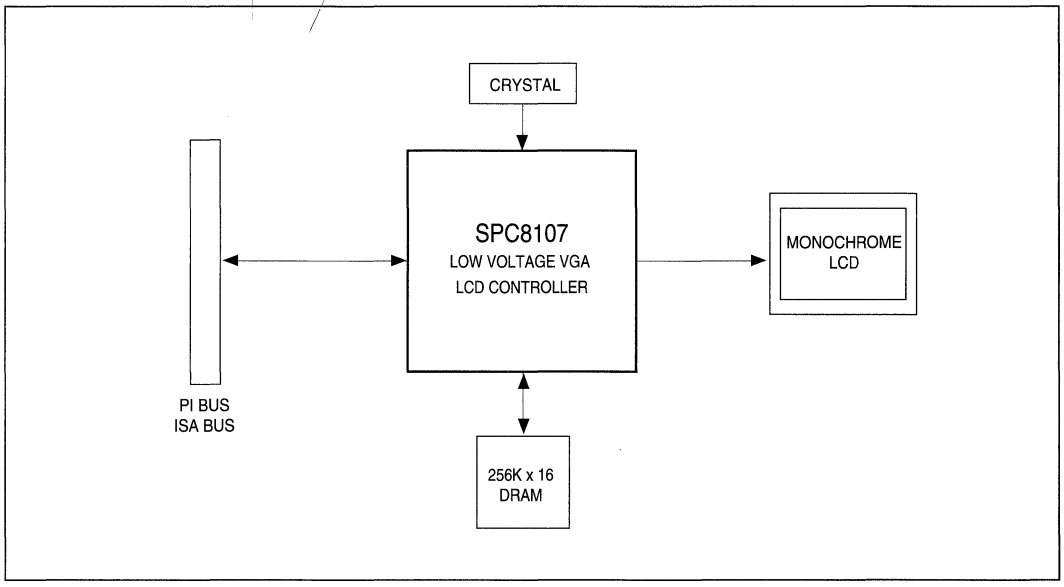
The SPC8107FOE is a single-chip, low-voltage LCD controller based on the VGA architecture and dedicated to driving a liquid crystal display. The fully VGA-compatible controller core, high-performance CPU interface and flexible 64 x 4-bit gray-scale lookup table are integrated into a very small footprint 100-pin QFP package.

The target markets for this device are low-cost and low-power sub-notebook and handheld products where low component count and a high performance 80 x 86 microprocessor interface are the major design considerations.

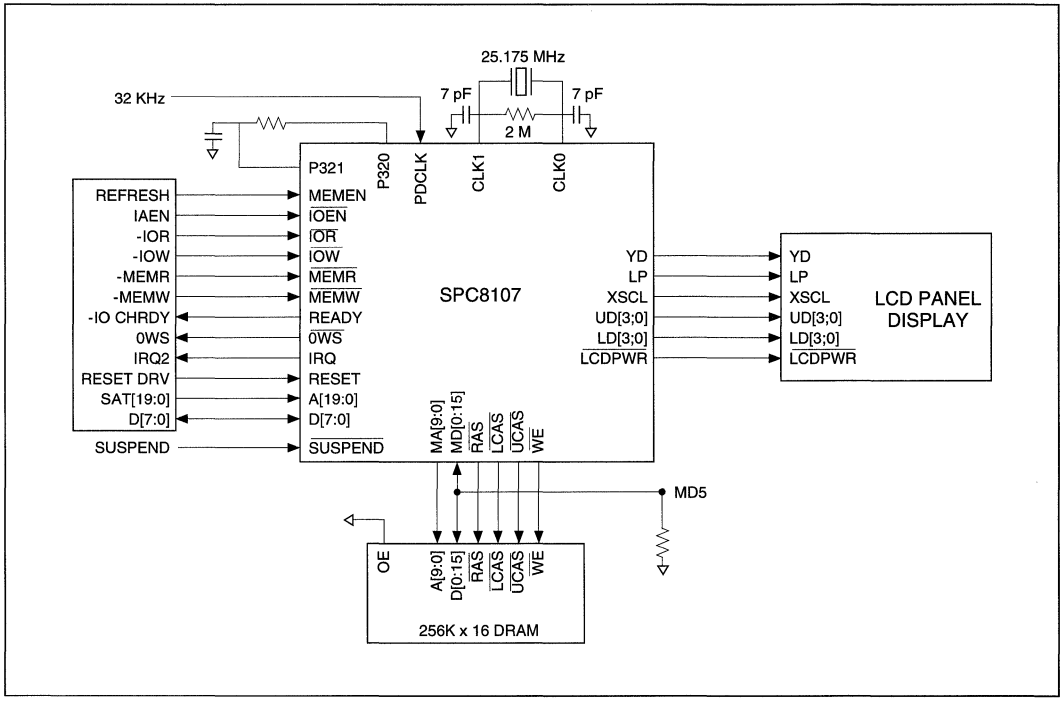
■ FEATURES

- Low-power CMOS technology
- Hardware VGA compatible
- High performance ISA & PI bus support
- One 256K x 16 self-refresh DRAM
- Four-stage display pipeline
- Video BIOS, software driver and utility support
- Single two-terminal crystal support
- Five power-down modes
- Package: QFP15-100 pin
- 3.3 volt core
- Monochrome LCD panel interface, for sizes 320 x 200 to 640 x 480
- On-chip 64 x 4 gray-scale look-up table
- 16 gray shades by frame rate modulation
- Three programmable gray-scale weightings (RGB), base (25, 50, 25), NTSC (30, 59, 11), and text (0, 100, 0)

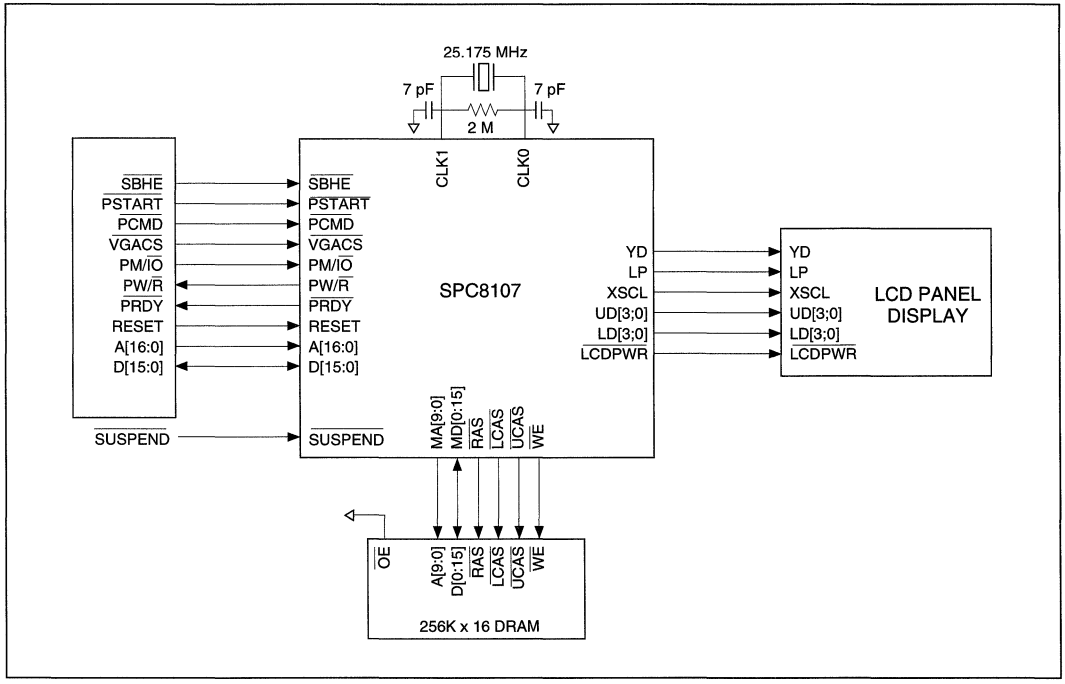
■ BLOCK DIAGRAM



■ ISA BUS SYSTEM BLOCK DIAGRAM



■ PI-BUS SYSTEM BLOCK DIAGRAM



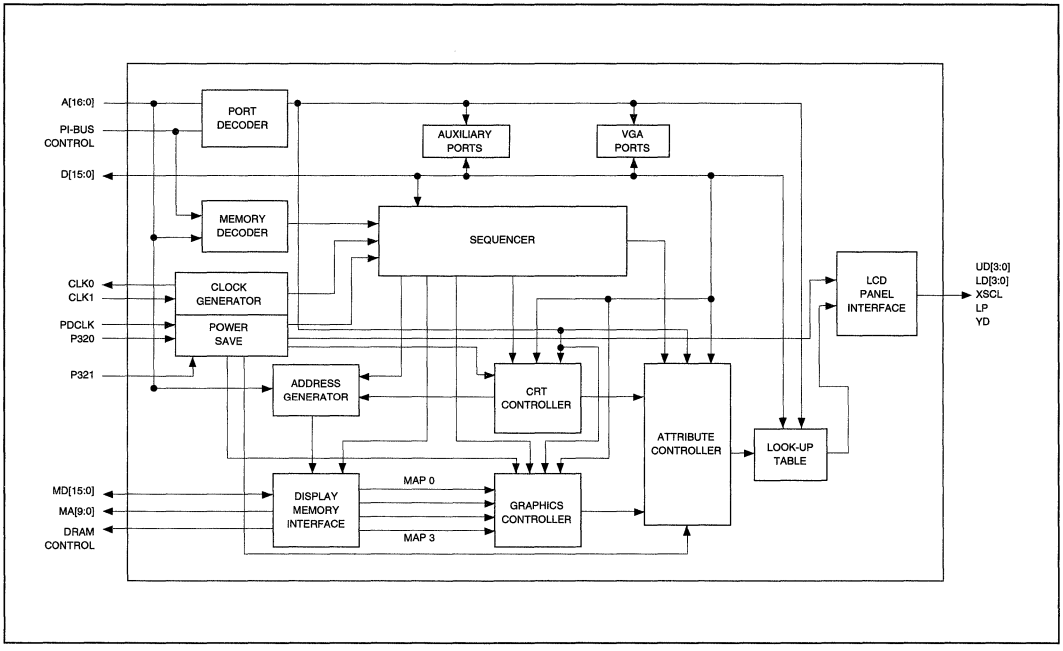
■ SPC8107 VIDEO MODES

Mode Number (Hex)	Horizontal Pixels Addressable	Vertical Pixels Addressable	Horizontal Pixels Displayed	Vertical Pixels Displayed	Monochrome LCD Display (Gray Shades)
0	320	200	320	200	16
0+	320	350	320	350	16
0++	360	400	320	400	16
1	320	200	320	200	16
1+	320	350	320	350	16
1++	360	400	320	400	16
2	640	200	640	200	16
2+	640	350	640	350	16
2++	720	400	640	400	16
3	640	200	640	200	16
3+	640	350	640	350	16
3++	720	400	640	400	16
4	320	200	320	200	4
5	320	200	320	200	4
6	640	200	640	200	2
7	720	350	640	350	2
7+	720	400	640	400	2
0D	320	200	320	200	16
0E	640	200	640	200	16
0F	640	350	640	350	2
10	640	350	640	350	16
11	640	480	640	480	2
12	640	480	640	480	16
13	320	200	640	400	16

■ SUPPORTED LCD PANELS

8-bit Interface				4-bit Interface	
Dual Panel		Single Panel		Single Panel	
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
640	400 480	640	400 480	320 480 640	200 240 320 400 480

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

The Sequencer

The Sequencer generates internal signals to synchronize the operation of the chip as well as the signals to control the timing of the display DRAM. The Sequencer also arbitrates between CPU and video display accesses to the DRAM. It contains registers that allow selection of character font set, control the structure of the video memory and allow write masking of the individual planes of memory.

CRT Controller

The CRT Controller generates the horizontal and vertical synchronization signals for the single panel or dual panel LCD display and character and/or pixel addresses for display data from DRAM.

Address Generator

The Address Generator takes the display and refresh addresses from the CRT Controller and converts them into RAS and CAS addresses for the display DRAM and multiplexes these display accesses with CPU memory accesses.

Attributes Controller

The Attributes Controller takes in pixel and attribute information from the Graphics Controller and display DRAM and formats the data into pixel information which then passes through the lookup table. It also controls display character attributes such as blink, underline and horizontal pixel panning.

Graphics Controller

The Graphics Controller supplies display memory data to the Attributes Controller during display time and provides data translation between the CPU bus and the display memory during CPU read or write access cycles.

Memory Decoder

The Memory Decoder monitors the CPU-bus activity and decodes cycles for the display DRAM. It supplies memory access control signals to the Sequencer.

Port Decoder

The Port Decoder decodes CPU-bus I/O cycles to provide enable and write strobes for the on-chip I/O registers.

Auxiliary Ports

The Auxiliary Ports are I/O registers used to control functions of the chip beyond the basic VGA register set. Registers are included for controlling the LCD interface circuits as well as the power save modes.

VGA Ports

The VGA Ports contain the Miscellaneous Output Status register and the Video Subsystem Enable register used in VGA mode.

Clock Generation

The Clock Generation contains oscillator support for an external crystal.

Power Save

The Power Save block contains the logic to implement one hardware- and five software-controlled power save modes.

Lookup Table

The Lookup Table consists of a memory array of 64 locations of 4 bits each and hardware to convert VGA palette writes to gray-scale values.

LCD Interface

The LCD Interface block converts the display video data from the Lookup Table into LCD display data. It also generates control signals necessary to drive single or dual-panel LCD panels. The LCD interface block generates 16 levels of gray shades through frame rate modulation techniques.

■ DC SPECIFICATIONS

● Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS}–0.3 to +7.0	V
V_{IN}	Input Voltage	V_{SS}–0.3 to V_{DD}+0.3	V
V_{OUT}	Output Voltage	V_{SS} to V_{DD}	V
T_{OPR}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–65 to +150	°C
T_{SOL}	Soldering Temperature/Time	260 for 10 sec max at lead	°C

● Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage	V_{SS} = 0V	3.0	3.3	3.6	V
V_{IN}	Input Voltage		V_{SS}	—	V_{DD}	V
I_{OPR}	Average Power Consumption (estimated)		—	30	—	mA
$IP_{D1,2}$	Power Save Mode 1, 2		—	20, 5	—	mA
$IP_{D3,4}$	Power Save Modes 3, 4 & SUSPEND		—	1	—	mA
IP_{D5}	Power Save Mode 5		—	25	—	mA

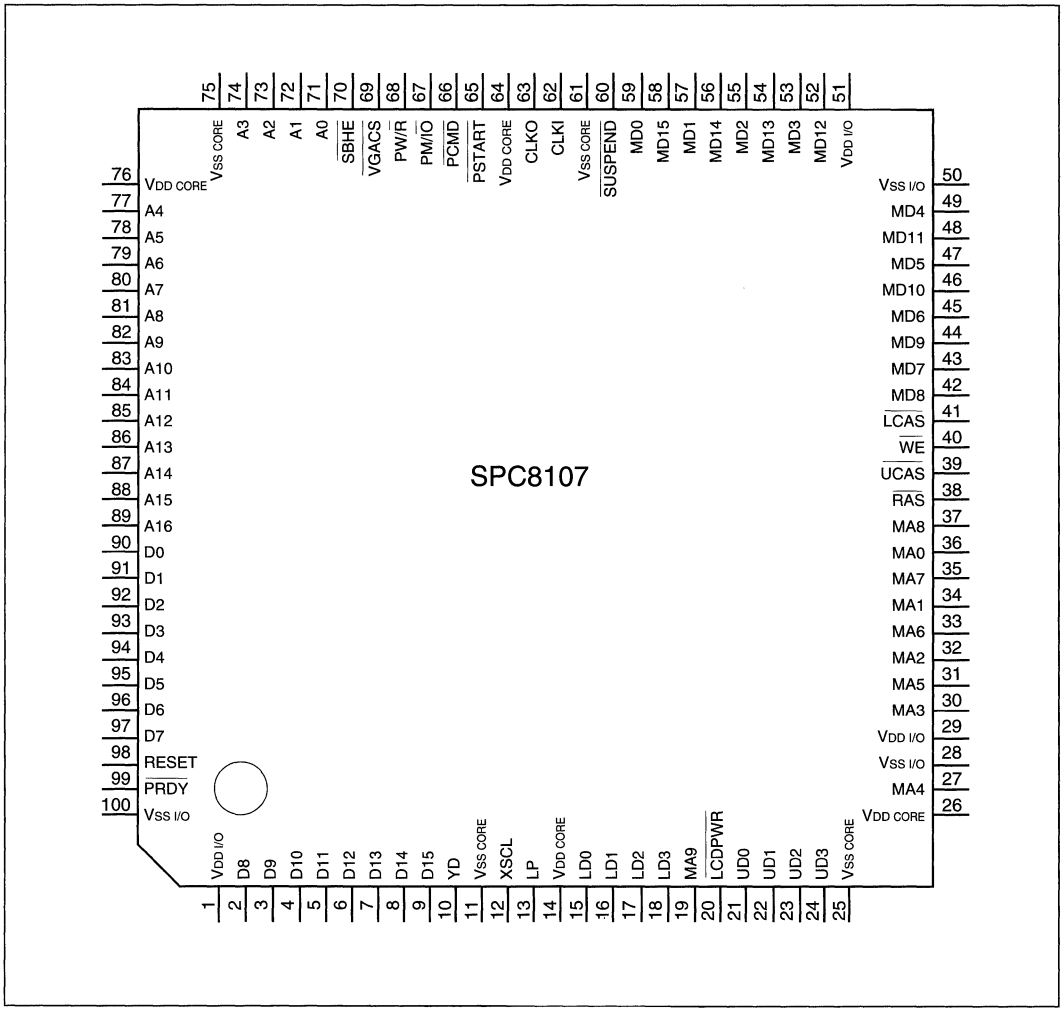
- **Input Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low-Level Input Voltage	V_{DD} = MIN	—	—	0.6	V
V_{IL}	Low-Level Input Voltage	V_{DD} = MIN	2.5	—	—	V
V_{T+}	Positive-going Threshold (CMOS Schmitt inputs)	V_{DD} =	—	—	—	V
V_{T-}	Negative-going Threshold (CMOS Schmitt inputs)	V_{DD} =	—	—	—	V
V_H	Hysteresis Voltage (CMOS Schmitt inputs)	V_{DD} =	—	—	—	V
I_{IZ}	Input Leakage Current	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1	—	1	µA
C_{IN}	Input Pin Capacitance		—	8	—	pF
R_{PU}	Pull Up Resistance	V_{DD} = 3.3 V	90	—	360	kΩ

- **Output Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OL}	Low-Level Output Current	V_{DD} = 3.0V	3.0	—	—	mA
I_{OH}	High-Level Output Current	TS6, TSU6, CO2	–1.0	—	—	mA
I_{OL}	Low-Level Output Current	V_{DD} = 3.0V	6.0	—	—	mA
I_{OH}	High-Level Output Current	TS6, TSU6, CO3	–2.0	—	—	mA
I_{OL}	Low-Level Output Current	V_{DD} = 3.0V	12.0	—	—	mA
I_{OH}	High-Level Output Current	TS4	–4.0	—	—	mA
I_{OZ}	Output Leakage Current	V_{DD} = 3.6V V_{OH} = V_{DD} or V_{OL} = V_{SS}	–1	—	—	µA
C_{OUT}	Output Pin Capacitance		—	8	—	pF

■ SPC8107 PIN OUTS



Note: Pin names on this diagram correspond to the default configuration (PI Bus, 2 CAS, 1 WE DRAM).

■ PIN DESCRIPTION

Key

C = CMOS level input
CS = CMOS level input with hysteresis
COx = CMOS level output, x denotes cell type
TSx = Tri-state CMOS level driver, x denotes cell type
TSUx = Tri-state CMOS level driver with 100 kΩ pull up resistor, x denotes cell type

● CPU Interface - PI-Bus

Note: to configure chip for PI-Bus operation, MD[5] must be held at logic 1 during RESET (there is an internal pull up for the MD[5] pin, so no pullup resistor is required).

Pin Name	Type	Pin #	Drv	Description (when MD [5] = 1 during RESET)
A[0:16]	I	71..74, 77..89	C	CPU bus address inputs. In Suspend Mode, the Address inputs are internally masked off.
D[0:15]	I/O	90..97, 2..9	C /CO3	16 bit PI-Bus data bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
/VGACS	I	69	C	PI-Bus VGA Chip Select. In Suspend Mode, the /VGACS input is disabled.
/PCMD	I	66	C	PI-Bus Command Strobe. In Suspend Mode the /PCMD input is disabled.
PM/IO	I	67	C	PI-Bus Memory or I/O Select. In Suspend Mode the PM/IO input is disabled.
PW/R	I	68	C	PI-Bus Write or Read Select. In Suspend Mode the PW/R input is disabled.
/SBHE	I	70	C	System Byte High Enable. In Suspend Mode the /SBHE input is disabled.
/PSTART	I	65	CS	PI-Bus Start Strobe. In Suspend Mode the /PSTART input is disabled.
/PRDY	O	99	TS3	PI-Bus Ready. This output is driven low to terminate a bus cycle.
RESET	I	98	CS	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state. During Suspend Mode the RESET input is ignored.

● Pin Mapping for ISA/PI Bus Interfaces

Pin No.	PI Bus Pin Name	ISA Bus Usage
71..74, 77..89	A[0:16]	A[0:16]
90..97	D[0:7]	D[0:7]
2..4	D[8:10]	A[17:19]
5	D[11]	IRQ
6	D[12]	/0WS
7..9	D[13:15]	PDCLK, P32O, P32I
65	/PSTART	/IOEN

Pin No.	PI Bus Pin Name	ISA Bus Usage
66	/PCMD	/IOR
67	PM/IO	/IOW
68	PW/R	/MEMR
69	/VGACS	MEMEN
70	/SBHE	/MEMW
99	/PRDY	READY

- **CPU Interface - ISA-Bus**

Note: to configure chip for ISA Bus operation, MD[5] must be held at logic 0 during RESET with an external pull-down resistor.

Pin Name	Type	Pin #	Drv	Description (when MD [5] = 1 during RESET)
A[0:19]	I	71..74, 77..89, 2..4	C	CPU bus address inputs. In Suspend Mode, the Address inputs are internally masked off.
D[0:7]	I/O	90..97	C /CO3	8 bit ISA-Bus data bus. These lines are driven by the chip only during read cycles and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
MEMEN	I	69	CS	ISA Bus Memory Enable. This signal should be connected to the /REFRESH signal on the ISA bus. When this signal is low (e.g. during a system memory refresh cycle), memory address decoding is disabled.
/IOR	I	66	C	ISA Bus I/O Read Strobe. In Suspend /IOR is disabled.
/IOW	I	67	C	ISA Bus I/O Write Strobe. In Suspend the /IOW is disabled.
/MEMR	I	68	C	ISA Bus Memory Read Strobe. In Suspend /MEMR is disabled.
/MEMW	I	70	C	ISA Bus Memory Write Strobe. In Suspend /MEMW is disabled.
/IOEN	I	65	CS	ISA Bus I/O Enable. This input should be connected to the ISA bus AEN signal. When this signal is high, I/O address decoding is disabled. In Suspend Mode, the /IOEN input is disabled.
READY	O	99	TS3	ISA Bus READY signal. This output is driven low to force the CPU to insert wait states during memory cycles. READY is released to high-Z after a transfer is complete.
RESET	I	98	CS	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state. During Suspend Mode the RESET input is ignored.
IRQ	O	5	TS3	ISA Bus Vertical Interrupt. When enabled, a Vertical Retrace Interrupt will cause this signal to be driven from a logic 0 state to a logic 1 (rising-edge triggered interrupt). Once set, this interrupt must be cleared by a bit in the CRTC registers. A control bit in the Auxiliary Registers allows this output to be optionally disabled (tri-stated).
/0WS	O	6	TS3	0 Wait State. This output is driven low when a valid I/O access is decoded. This will allow the CPU to complete the ISA bus I/O access with zero wait states. When inactive, this output will be tri-stated.

- **Video Memory Interface**

Pin Name	Type	Pin #	Drv	Description
MA[0:8]	O	36, 34, 32, 30, 27, 31, 33, 35, 37	CO3	Multiplexed row/column address bits for video display memory.
MA[9] (/RDACK, or WF)	O	19	CO3	Multiplexed row/column address bit 9 (MA[9]), or Read Acknowledge (/RDACK), or LCD Bias Signal WF, as determined by the logic value on MD[4] and MD[7] during RESET. When MD[7] is latched in as 0, this pin functions as the LCD Backplane Bias signal WF. When MD[7] is latched in as 1, then this pin's function is determined by MD[4] as follows: when MD[4] is latched in as 1, this pin is configured as address bit MA[9] which is only required for 256K x 16 DRAMs which are organized as 1024 x 256 x 16 (i.e. 10 row address bits, 8 column address bits). For other DRAMs, MA[9] is not required. When MD[4] is latched in as 0, this pin is configured as the /RDACK signal, which goes low during valid I/O or memory reads to the chip.
MD[0:15]	I/O	42-49, 52-59	C/ TSU3	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET is high, or when the Sequencer is in a reset state. On the falling edge of RESET, the values on MD[3:0] are latched into a read-only Auxiliary Register and are available to be read as configuration inputs. Other MD inputs are used to configure various hardware options. See Configuration Options below.
/RAS	O	38	CO6	DRAM Row Address Strobe.
/LCAS (/LWE)	O	41	CO6	DRAM Column Address Strobe for low byte (/LCAS) or Write Enable Strobe for low byte (/LWE), as determined by logic value on MD[6] during RESET (see pin mapping table).
/UCAS (/CAS)	O	39	CO6	DRAM Column Address Strobe for high byte (/UCAS) or single Column Address Strobe (/CAS) as determined by logic value on MD[6] during RESET.
/WE (/UWE)	O	40	CO6	DRAM Write Enable Strobe(/WE), or Write Enable Strobe for high byte (/UWE), as determined by logic value on MD[6] during RESET.

- **Miscellaneous**

Pin Name	Type	Pin #	Drv	Description
/SUSPEND	I	60	CS	A low level on this pin puts the chip into a hardware power save mode. The /SUSPEND signal overrides any software initiated power save modes, and disables the PI-Bus interface inputs. Address and Data inputs are also masked when this signal is low. When in Suspend Mode the UD(3:0), LD(3:0), XSCL, YD, LP and WF signals are driven into a high impedance state (optionally driven low) and the /LCDPWR signal is driven high.

- **Clock Inputs**

Pin Name	Type	Pin #	Drv	Description
CLKI	I	62	•	This pin, along with CLKO is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO	O	63	•	This pin, along with CLKI is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.
PDCLK	I	7	C	Power Down Clock. This input may be used in ISA bus configuration (MD[5] = 0 at RESET) to provide a low frequency clock for generating refresh in Power Save Mode 4 and Suspend, as an optional alternative to using the pixel clock or MEMEN input as the refresh clock source.
P32O	O	8	CO2	P32 Clock Output. This pin is used to support a 50% duty cycle 32 KHz PDCLK input (pin 7). This P32O output is a buffered version of the PDCLK input used to drive an external RC circuit. For a 64 KHz PDCLK input, this output should be left unconnected.
P32I	I	9	C	P32I Clock Input. This pin is used to support a 50% duty cycle 32 KHz PDCLK input (pin 7). This P32I input should be connected to an external RC circuit which generates 100-200 ns delay from P32O. Internally this will be used to generate a 64 KHz refresh clock with the appropriate low period. For a 64 KHz PDCLK input, this pin must be tied high.

- **Power Supply**

Pin Name	Type	Pin #	Description
VDD CORE	P	14, 26, 64, 76	VDD supply for core logic.
VDD I/O	P	1, 51, 29	VDD supply for I/O pins.
VSS CORE	P	11, 25, 61, 75	VSS supply for core logic.
VSS I/O	P	50, 100, 28	VSS supply for I/O pins.

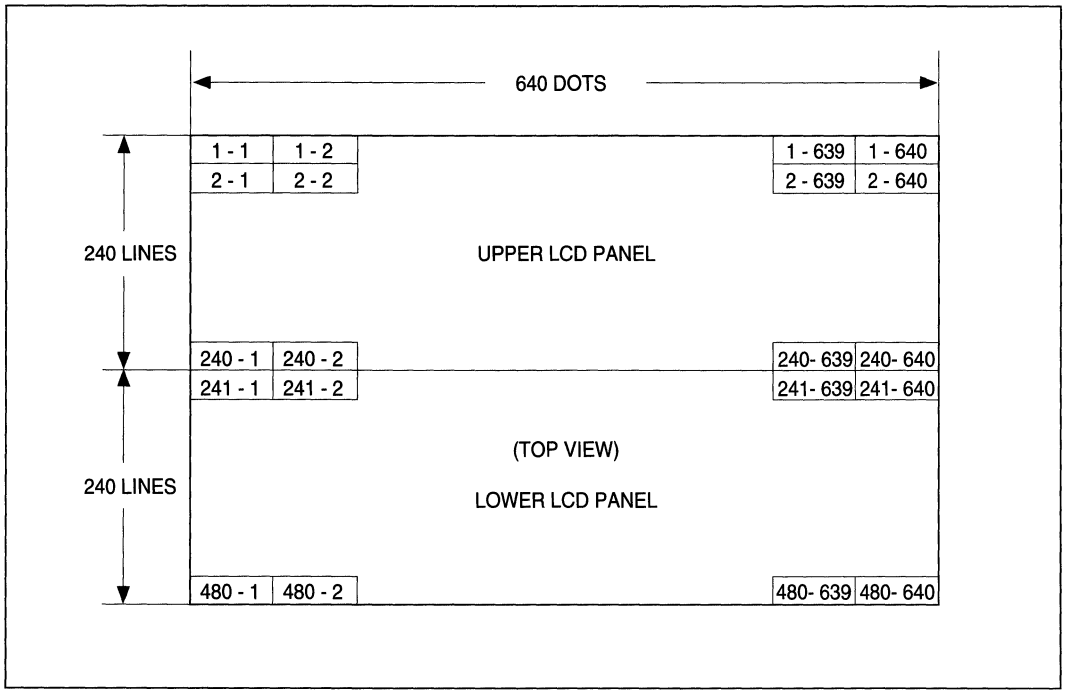
- **Configuration Options**

Pin Name	Values on this pin at falling edge of RESET is used to configure: (1/0)
MD[3:0]	Values stored in read-only Aux Reg [02] bits 7:4 for software use
MD[4]	Select the function of output pin 19 as MA[9] (1), or /RDACK (0) - see also MD[7]
MD[5]	PI-bus operation (1) /ISA bus operation (0)
MD[6]	2 CAS, 1 WE type DRAM (1) / 1 CAS, 2 WE type DRAM (0)
MD[7]	use MD[4] to configure pin 6 as MA9 or /RDACK (1) / pin 6 is WF output (0)
MD[8]	Reserved
MD[9]	Reserved

- **LCD Panel Interface**

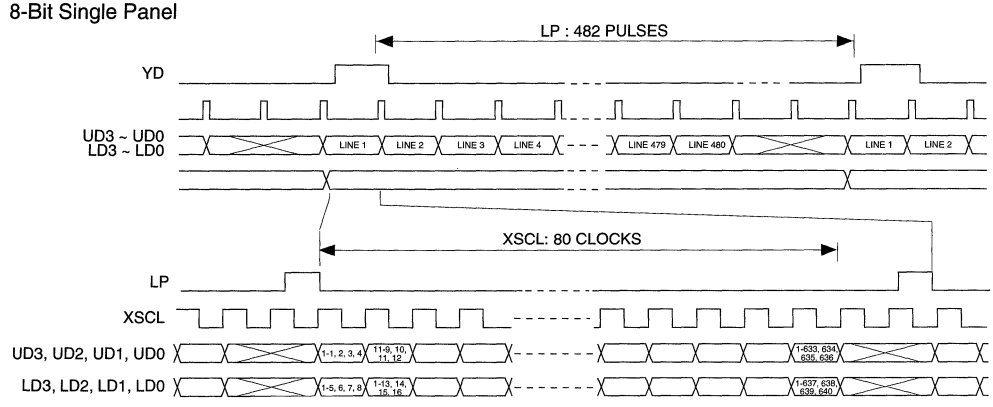
Pin Name	Type	Pin #	Drv	Description
YD	O	10	TS12	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of vertical frame.
LP	O	13	TS12	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O	12	TS12	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
UD[0:3]	O	21..24	TS12	Upper panel display data for dual panel mode. For single panel mode these bits are the most significant 4 bits of the 8 bit output data to the panel (PD[4:7]). For 4-bit single panel mode, these bits are the 4 bits of output data to the panel.
LD[0:3]	O	15..18	TS12	Lower panel data for dual panel mode. For 8-bit single panel mode, these bits are the least significant 4 bits of the 8-bit output data to the panel (PD[0:3]). For 4-bit single panels, these bits are driven 0.
/LCDPWR	O	20	CO3	LCD power control. In normal operation this signal is driven low to enable an external LCD power supply. This signal is driven high when the chip is put into any power save mode, or if the Sequencer is in a reset state. It can be used externally to turn off the panel supply voltage and backlight. After a RESET, this signal is held high until the CRTC is programmed and running.
WF (MA[9] or /RDACK)	O	19	CO3	LCD Backplane Bias Signal. This pin is shared with the MA9 and /RDACK functions. To use this pin as WF, the value on MD[7] at RESET must be 0. The WF signal toggles once per vertical frame.

■ LCD Panel Pixels

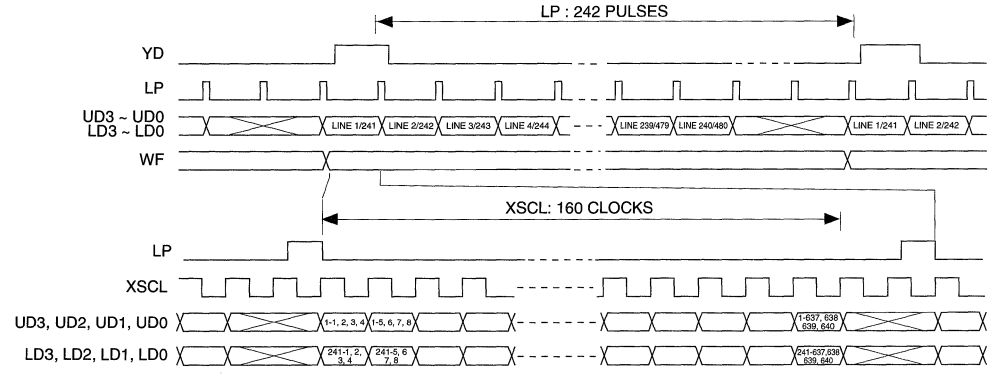


■ LCD Panel Interface

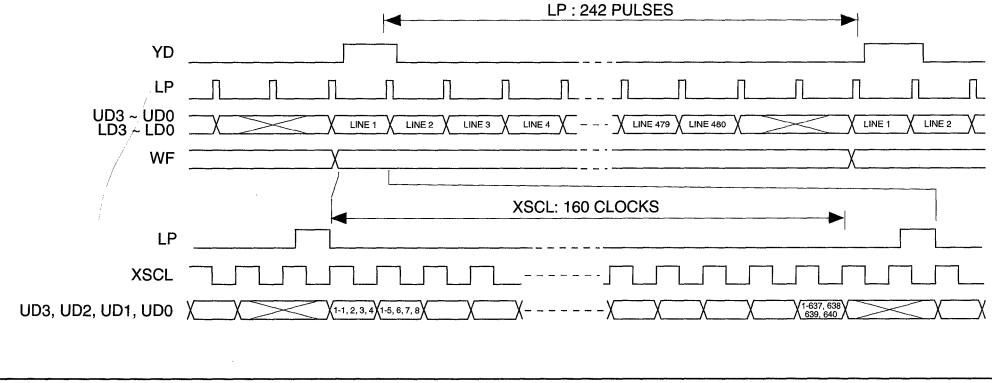
8-Bit Single Panel



8-Bit Dual Panel



4-Bit Single Panel



■ POWER SAVE MODES

One hardware-controlled and five software-controlled Power Save Modes are provided by the SPC8107.

Software Power Save Mode 1

- No video display accesses to display memory.
- Dedicated CPU accesses to display memory.
- Display memory refresh is maintained and is generated from CLKI input (nominally 25 MHz). Refresh rate can be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- I/O read/write of all registers is allowed.
- /LCDPWR signal forced high.

Options

- LCD output signals tri-stated or forced low.

Software Power Save Mode 2

Mode 2 has two states. Initially the chip enters State 1. If no display memory read or write is detected for about two horizontal lines (approx. 63.5 us), the chip enters State 2. If a display memory read or write is requested while in State 2, the chip returns to State 1 to service the display memory access within 3 - 7 Ts periods (CLKI input).

State 1

- Same as Power Save Mode 1

State 2

- No video display accesses to display memory.
- No CPU accesses to display memory.
- Sequencer is halted.
- Display memory refresh is maintained and is generated from CLKI input (nominally 25 MHz). Refresh rate can be selected: 64 kHz or 8 kHz, (for 256 cycle/4 msec, or 256 cycle/32 msec DRAM, respectively).
- I/O read/write of all registers is allowed.
- /LCDPWR signal forced high.

Options

- LCD output signals tri-stated or forced low.

Software Power Save Mode 3

- No video display accesses to display memory.
- No CPU accesses to display memory.
- Sequencer is halted.
- No display memory refresh.
- I/O read/write of all registers is allowed.
- /LCDPWR signal forced high.

Options

- I/O read/write to all registers except Auxiliary Registers can be disabled.
- Internal clock oscillator cell can be disabled if a 2-terminal crystal is used.
- LCD output signals tri-stated or forced low.

Software Power Save Mode 4

- No video display accesses to display memory.
- No CPU accesses to display memory.
- Sequencer is halted.
- Display memory refresh maintained.
- I/O read/write of all registers is allowed.
- /LCDPWR signal forced high.

Options

- Select MEMEN, PDCLK, or CLKI as refresh clock source (ISA only)
- I/O read/write to all registers except Auxiliary Registers can be disabled.
- Internal clock oscillator cell can be disabled, if a 2-terminal crystal is used.
- LCD output signals tri-stated or forced low.
- DRAM self-refresh mode can be used to maintain display memory contents.

Software Power Save Mode 5

- Video display remains active/visible.
- CPU accesses to display memory allowed.

Options

- Internal clock can be slowed by 20%.

Hardware Power Save Mode (Suspend Mode)

- No video display accesses to display memory.
- No CPU accesses to/from display memory.
- Sequencer is halted.
- Display memory refresh maintained.
- No I/O register or memory accesses allowed.
- /LCDPWR signal forced high.
- LCD output signals tri-stated or forced low.
- All CPU interface input signals are internally masked off. All CPU interface output signals are inactive.
- Internal clock oscillator cell will be disabled, if a 2-terminal crystal is used.

Options

- DRAM self-refresh mode can be used to maintain display memory contents.
- Select MEMEN, PDCLK, or CLKI as refresh clock source (ISA only).

LOW POWER LCD & CRT VGA CONTROLLER

■ DESCRIPTION

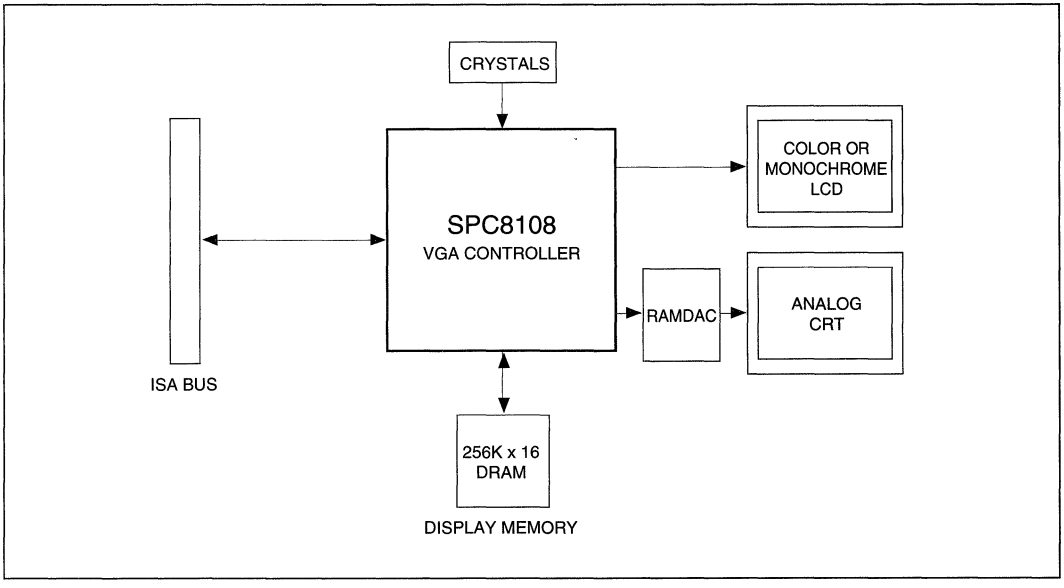
The SPC8108F0C is a versatile VGA graphics controller capable of driving liquid crystal displays and analog CRT monitors. The controller integrates all LCD interface, sequencing and gray shading logic into one small form factor 144 pin package. With the addition of an industry standard '477 type RAMDAC, the SPC8108F0C will also drive a VGA fixed frequency or multifrequency monitor.

The target products for this device are price and power sensitive 80x86 microprocessor based subnotebooks or other specialized LCD systems where a high quality 16 or 64 gray shade VGA image on a 320 x 200 to 640 x 480 LCD panel display are the major design criteria.

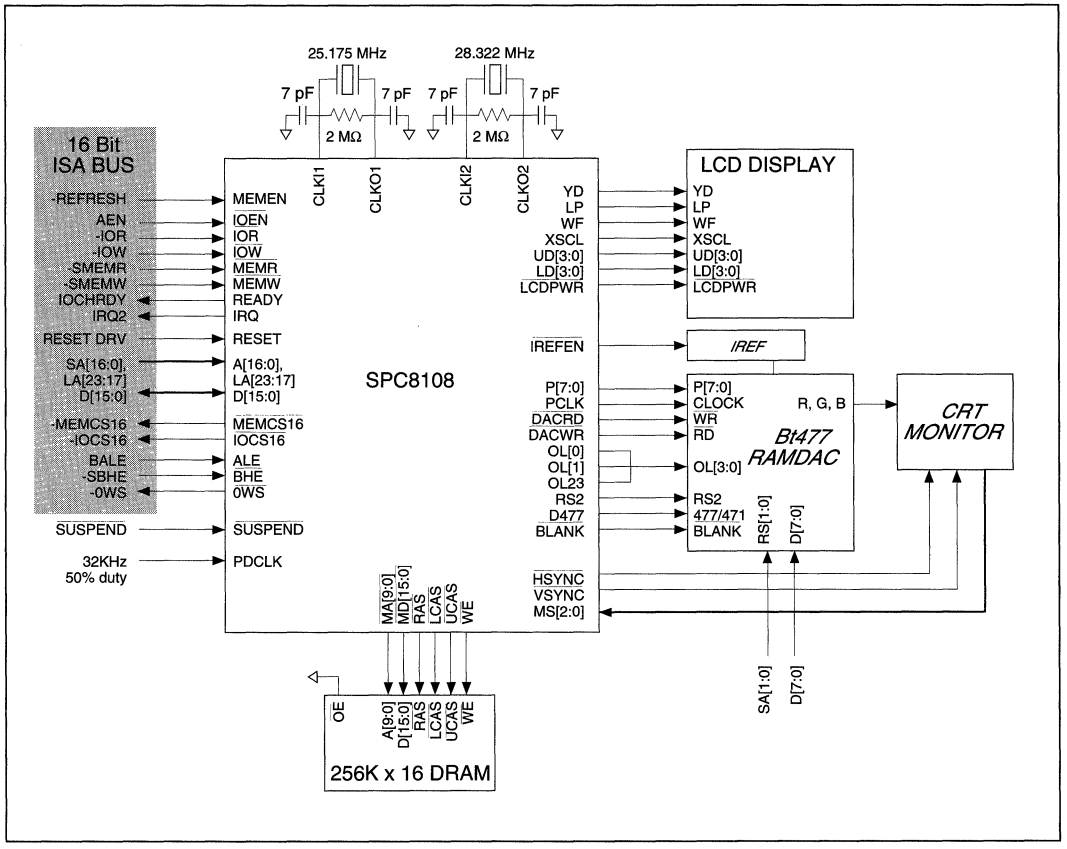
■ FEATURES

- Low-power CMOS technology
- Hardware VGA compatible
- High-performance 16-bit ISA support
- One 256K x 16 self-refresh DRAM
- Four-stage display pipeline
- 64 x 64 pixel hardware cursor
- Two-terminal crystals support
- Five power-down modes
- Video BIOS, software driver and utility support
- 5 volt operation
- QFP17-144 pin
- Monochrome LCD panel interface for sizes 320 x 200 to 640 x 480
- On-chip 256 x 6 grayscale look-up table
- 16 gray shades by frame rate modulation
- 64 gray shades by frame rate modulation and dithering
- Two programmable grayscale weightings (RGB), NTSC (30,59,11), and text (0,100,0)
- Vertical centering and expansion for LCDs
- Full CRT support with '477 RAMDAC

■ BLOCK DIAGRAM



■ ISA BUS SYSTEM BLOCK DIAGRAM



■ SPC8108 VIDEO MODES

Mode Number (Hex)	Horizontal Pixels Addressable	Vertical Pixels Addressable	Horizontal Pixels Displayed	Vertical Pixels Displayed	Monochrome LCD Display Gray Shades	CRT Colors
0	320	200	320	200/480	16	16
0+	320	350	320	350	16	16
0++	360/320	400	320	400/480	16	16
1	320	200	320	200/480	16	16
1+	320	350	320	350	16	16
1++	360/320	400	320	400/480	16	16
2	640	200	640	200/480	16	16
2+	640	350	640	350	16	16
2++	720/640	400	640	400/480	16	16
3	640	200	640	200/480	16	16
3+	640	350	640	350	16	16
3++	720/640	400	640	400/480	16	16
4	320	200	320	200/480	4	4
5	320	200	320	200/480	4	4
6	640	200	640	200/480	2	2
7	720/640	350	640	350	2	2
7+	720/640	400	640	400/480	2	2
0D	320	200	320	200/480	16	16
0E	640	200	640	200/480	16	16
0F	640	350	640	350	2	2
10	640	350	640	350	16	16
11	640	480	640	480	2	2
12	640	480	640	480	16	16
13	320	200	640	400/480	64	256

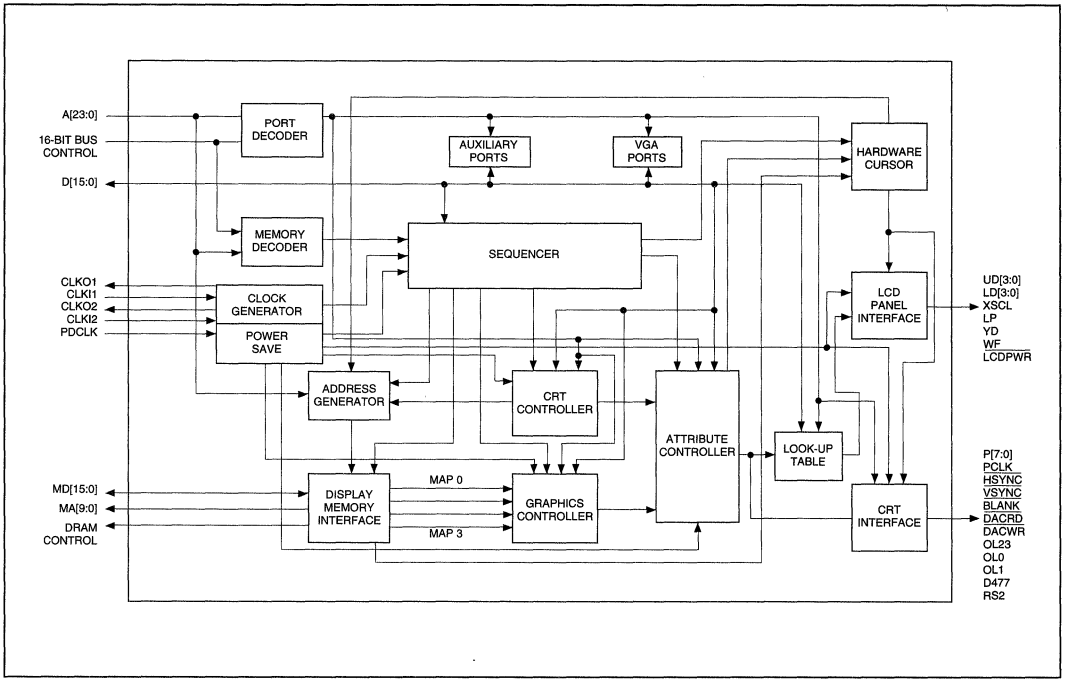
Notes: 400 line text and graphics modes can be stretched vertically to 480 lines as an option.

360 and 720 dot text modes are actually displayed as 320 and 640 dots on an LCD panel.

■ SUPPORTED STN LCD PANELS

8-bit Interface				4-bit Interface	
Dual Panel		Single Panel		Single Panel	
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
640	400 480	640	400 480	320 480 640	200 240 320 400 480

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

The Sequencer

The Sequencer generates internal signals to synchronize the operation of the chip as well as the signals to control the timing of the display DRAM. The Sequencer also arbitrates between CPU and video display accesses to the DRAM. It contains registers that allows selection of character font set, control the structure of the video memory and allow write masking of the individual plane of memory.

CRT Controller

The CRT Controller generates the horizontal and vertical synchronization signals for the CRT, single panel or dual panel LCD display and character and/or pixel addresses for display data from DRAM.

CRT Interface

The CRT interface aligns CRT signals to the Pixel Clock and generates the I/O Control signals for CPU access to the RAMDAC.

Address Generator

The Address Generator takes the display and refresh addresses from the CRT Controller and converts them into RAS and CAS addresses for the display DRAM, and multiplexes these display accesses with CPU memory accesses.

Attributes Controller

The Attributes Controller takes in pixel and attribute information from the Graphics Controller and display DRAM and formats the data into pixel information which then passes through the lookup table. It also controls display character attributes such as blink, underline and horizontal pixel panning.

Graphics Controller

The Graphics Controller supplies display memory data to the Attributes Controller during display time and provides data translation between the CPU bus and the display memory during CPU read or write access cycles.

Memory Decoder

The Memory Decoder monitors the CPU-bus activity and decodes cycles for the display DRAM. It supplies memory access control signals to the Sequencer.

Port Decoder

The Port Decoder decodes CPU-bus I/O cycles to provide enable and write strobes for the on-chip I/O registers.

Auxiliary Ports

The Auxiliary Ports are I/O registers used to control functions of the chip beyond the basic VGA register set. Registers are included for controlling the LCD interface circuits as well as the power save modes.

VGA Ports

The VGA Ports contain the Miscellaneous Output Status register and the Video Subsystem Enable register used in VGA mode.

Clock Generation

The Clock Generation contains oscillator support for external crystals.

Power Save

The Power Save block contains the logic to implement four software controlled and one hardware controlled power down modes.

Lookup Table

The Lookup Table consists of a memory array of 256 locations of 6 bits each and hardware to convert VGA palette writes to gray scale values.

LCD Interface

The LCD Interface block converts the display video data from the Lookup Table into LCD display data. It also generates control signals necessary to drive single or dual-panel LCD panels. The LCD interface block generates 16 levels of gray shades through frame rate modulation techniques and 64 levels of grey shades with additional dithering techniques.

Hardware Cursor

The Hardware Cursor block generates a 64 x 64 x 4 grey shade cursor or sprite that can be overlayed on the current displayed image.

■ DC SPECIFICATIONS

● Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS}–0.3 to +7.0	V
V_{IN}	Input Voltage	V_{SS}–0.3 to V_{DD}+0.3	V
V_{OUT}	Output Voltage	V_{SS} to V_{DD}	V
T_{OPR}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–65 to +150	°C
T_{SOL}	Soldering Temperature/Time	260 for 10 sec max at lead	°C

● Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage	V_{SS} = 0V	4.75	5.0	5.25	V
V_{IN}	Input Voltage		V_{SS}	—	V_{DD}	V
I_{OPR}	Average Power Consumption (estimated)		—	125	—	mA
I_{PD1}	Power Save Mode 1		—	75	—	mA
I_{PD2}	Power Save Mode 2		—	20	—	mA
$I_{PD3, 4}$	Power Save Modes 3, 4		—	1	—	mA
I_{PDSUS}	SUSPEND Mode		—	0.5	—	mA

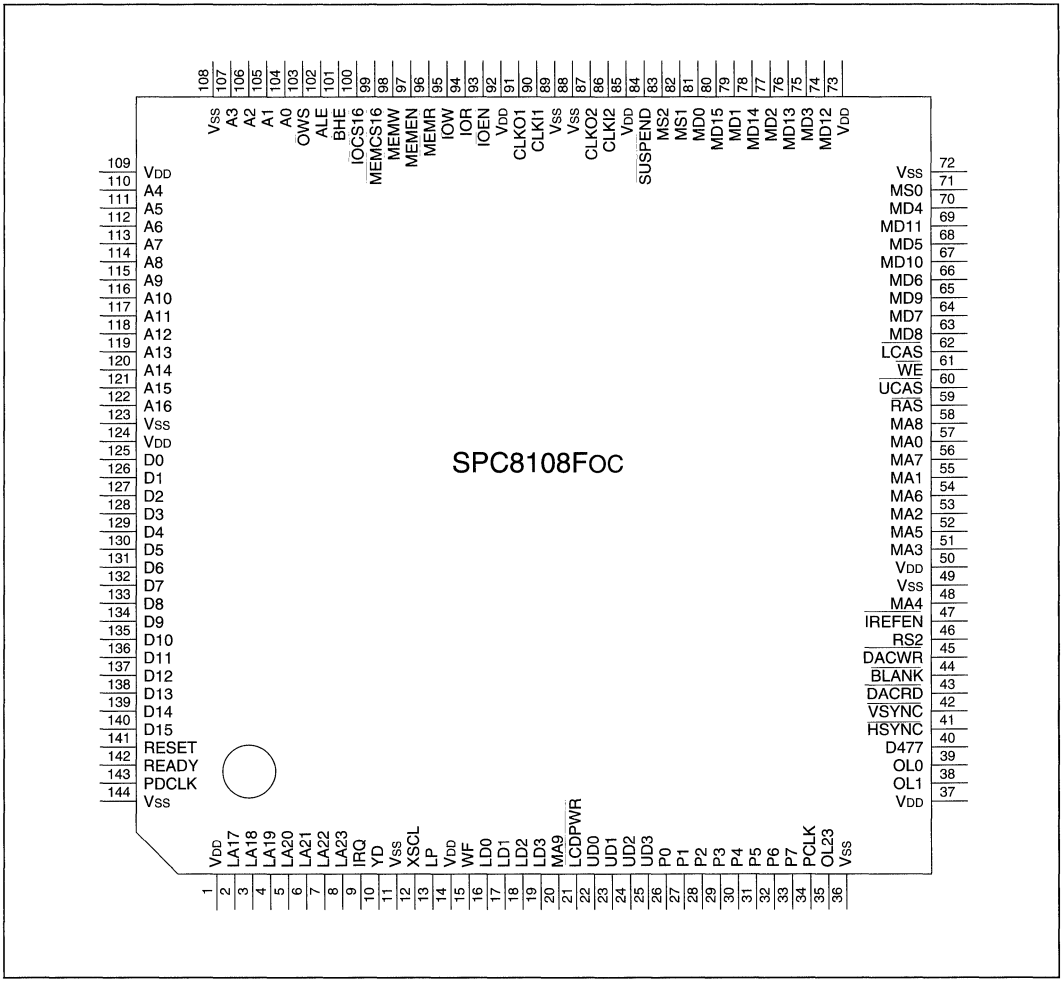
- **Input Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (CMOS Inputs)	V_{DD} = MIN	—	—	1.0	V
V_{IL}	Low Level Input Voltage (TTL Inputs)	V_{DD} = MIN	—	—	0.8	V
V_{IH}	High Level Input Voltage (CMOS Inputs)	V_{DD} = MAX	3.5	—	—	V
V_{IH}	High Level Input Voltage (TTL Inputs)	V_{DD} = MAX	2.0	—	—	V
V_{T+}	Positive-going Threshold (TTL Schmitt inputs)	V_{DD} = 5.0	—	—	3.0	V
V_{T-}	Negative-going Threshold (TTL Schmitt inputs)	V_{DD} = 5.0	0.6	—	—	V
V_H	Hysteresis Voltage (TTL Schmitt inputs)	V_{DD} = 5.0	0.1	—	—	V
I_{IZ}	Input Leakage Current	V_{DD}= MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1	—	1	µA
C_{IN}	Input Pin Capacitance		—	8	—	pF
R_{PU}	Pull Up Resistance	V_{DD} = 5.0 V	50	—	200	kW

- **Output Specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OL}	Low Level Output Current (TS2)	V_{OL} = V_{SS}+0.4V	6.0	—	—	mA
I_{OH}	High Level Output Current (TS2)	V_{OH} = V_{DD}–0.4V	–2.0	—	—	mA
I_O	Low Level Output Current (C03)	V_{OL} = V_{SS}+0.4V	12.0	—	—	mA
I_{OH}	High Level Output Current (C03)	V_{OH} = V_{DD}–0.4V	–4.0	—	—	mA
I_O	Low Level Output Current (TS4)	V_{OL} = V_{SS}+0.4V	24.0	—	—	mA
I_{OH}	High Level Output Current (TS4)	V_{OH} = V_{DD}-0.4V	–8.0	—	—	mA
I_{OZ}	Output Leakage Current	V_{OH} = V_{DD} or V_{OL} = V_{SS}	–1	—	1	µA
C_{OUT}	Output Pin Capacitance		—	6	—	pF
C_{BID}	Bidirectional Pin Capacitance		—	10	—	pF

■ SPC8108 PIN OUTS



■ PIN DESCRIPTION

Key

Key

C = CMOS level input
CS = CMOS level input with hysteresis
COx = CMOS level output, x denotes cell type
TSx = Tri-state CMOS level driver, x denotes cell type
TSUx = Tri-state CMOS level driver with 100 kΩ pull up resistor, x denotes cell type

● Video Memory Interface

Pin Name	Type	Pin #	Drv	Description
MA[0:9]	O	20, 48, 51, 52, 54, 55, 56, 57, 58	TS2 (* C)	Multiplexed row/column address bits for video display memory.
MD[0:15]	I/O	63, 64, 66, 67, 68, 69, 70, 74, 75, 76, 77, 78, 79, 80, 81	TTL/ TS2U2	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET is high, or when the Sequencer is in a reset state. On the falling edge of RESET, the values on MD[3:0] and MD[12:9] are latched into a read-only Auxiliary Register and are available to be read as configuration inputs. Also, the value on MD[8:4] and MD[14:13] are used to configure various hardware options. See section on configuration options for details.
/RAS	O	59	TS3 (*C)	DRAM Row Address Strobe for single 256Kx16 DRAM.
/LCAS (/LWE)	O	62	TS3 (*C)	DRAM Column Address Strobe for low byte (/LCAS). For alternate function see *Multiple Function Pin Descriptions.*
/UCAS (/CAS)	O O	60 61	TS3 (*C)	DRAM Column Address Strobe for high byte (/UCAS). For alternate function see Multiple Function Pin Descriptions. DRAM Write Enable Strobe (/WE).
/WE (/UWE)			TS3 (*C)	For alternate function see *Multiple Function Pin Descriptions.*

- **Clock Inputs**

Pin Name	Type	Pin #	Drv	Description
CLKI1	I	90	C	This pin, along with CLKO1 is the 25.175 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO1	O	91	•	This pin, along with CLKI1 is the 25.175 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.
CLKI2	I	86	C	This pin, along with CLKO2 is the 28.322 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO2	O	87	•	This pin, along with CLKI2 is the 28.322 MHz 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.

- **CPU Interface**

Pin Name	Type	Pin #	Drv	Description
A[0:16], LA[17:23]	I	2..8, 104..107, 110..122	TTL	CPU bus address inputs. In Suspend Mode, the Address inputs are internally masked off. If the value on MD[5] at RESET = 1, then the ALE input is used to internally latch LA[23:20] and A[19:2], allowing these address bits to be driven by the processor address bus. If the value on MD[5] at RESET = 0, then standard ISA address timing is assumed.
D[0:15]	I/O	125..140	TTL TS2	16 bit ISA-Bus data bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times. In Suspend Mode, these inputs are internally masked off.
MEMEN	I	97	TTLS	ISA Bus Memory Enable. This signal should be connected to the /REFRESH signal on the ISA bus. When this signal is low (e.g. during a system memory refresh cycle), memory address decoding is disabled.
/IOR	I	94	TTL	ISA Bus I/O Read Strobe. In Suspend Mode the /IOR input is disabled.
/IOW	I	95	TTL	ISA Bus I/O Write Strobe. In Suspend Mode the /IOW input is disabled.
/MEMR	I	96	TTL	ISA Bus System Memory Read Strobe. In Suspend Mode the /MEMR input is disabled.
/MEMW	I	98	TTL	ISA Bus System Memory Write Strobe. In Suspend Mode the /MEMW input is disabled.
/IOEN	I	93	TTLS	ISA Bus I/O Enable. This input should be connected to the ISA bus AEN signal. When this signal is high, I/O address decoding is disabled. In Suspend Mode, the /IOEN input is disabled.

(continued)

- **CPU Interface (continued)**

Pin Name	Type	Pin #	Drv	Description
READY	O	142	TS2	ISA Bus READY signal. This output is driven low to force the CPU to insert wait states during memory cycles. READY is released to high-Z after a transfer is complete.
RESET	I	141	TTLS	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state. During Suspend Mode the RESET input is ignored.
IRQ	O	9	TS2	ISA Bus Vertical Interrupt. When enabled, a Vertical Retrace Interrupt will cause this signal to be driven from a logic 0 state to a logic 1 (rising-edge triggered interrupt). Once set, this interrupt must be cleared by a bit in the CRTC registers. A control bit in the Auxiliary Registers allows this output to be optionally disabled (tri-stated)
/MEMCS16	O	99	TS4 (*C)	ISA BusMemory Chip Select 16.
/IOCS16	O	100	TS4 (*C)	ISA Bus I/O Chip Select 16
/BHE	I	101	TTL	ISA Bus Byte High Enable. In Suspend Mode the / BHE input is disabled.
ALE	I	102	TTL	ISA Bus Address Latch Enable. In Suspend Mode the ALE input is disabled. If the value on MD[5] at RESET = 1, then the ALE input is used to internally latch LA[23:17] and A[16:2], allowing these address bits to be driven by the processor address bus. If the value on MD[5] at RESET = 0, then standard ISA address timing is assumed.
/0WS	O	103	TS2	ISA Bus 0 Wait State. This signal will be driven low during I/O accesses to indicate 0 wait state cycles may be performed. When inactive, this output will be in the high-impedance state.

- **External CRT/RAMDAC Interface**

Pin Name	Type	Pin #	Drv	Description
P[0:7]	O	26..33	TS2	Pixel Data outputs. These 8 bits are connected to the pixel select inputs of the external RAMDAC.
PCLK	O	34	TS2	Pixel Clock. Pixel data is clocked out of the chip on the falling edge of PCLK.
/BLANK	O	44	TS2	Blank output. This output is driven low during display blanking periods.
/HSYNC	O	41	TS4	Horizontal Sync. This output is driven to indicate the horizontal retrace period. The polarity of this signal is determined by a control bit in register 3C2H.
/VSYNC	O	42	TS4	Vertical Sync. This output is driven to indicate the vertical retrace period. The polarity of this signal is determined by a control bit in register 3C2H.
/DACRD	O	43	TS2	RAMDAC Read Strobe. This signal goes low when a valid read access to the VGA RAMDAC is decoded by the chip.
/DACWR	O	45	TS2	RAMDAC Write Strobe. This signal goes low when a valid write access to the VGA RAMDAC is decoded by the chip.
RS2	O	46	TS2	Register Select 2 output. This output should be connected to the RS2 input of the RAMDAC (Bt477 or equivalent). The logic level on this output may be set by setting Auxiliary Reigister [0B] bit 3. This signal is required to allow CPU access the control and overlay registers of the external RAMDAC.
OL[0:1]	O	38, 39	TS2	Multiple Function Pin Function is determined by the value on MD[13] at RESET. When MD[13]=0 at RESET, these pins are outputs used to provide sprite/HW cursor function on the CRT display. In this case, these outputs should be connected to the OL[0:1] inputs of the RAMDAC (Bt477 or equivalent). They are used by the sprite circuitry to access the overlay registers in the RAMDAC. When MD[13] = 1 at RESET, the sprite/HW cursor function is unavailable on the CRT display. Refer to functional specification for alternate function.
OL23	O	35	TS2	Overlay Select output 2/3. This output should be connected to both the OL2 and OL3 inputs of the RAMDAC (Bt477 or equivalent). This signal is used by the sprite circuitry to access the overlay registers in the RAMDAC.
D477	O	40	TS2	477 Control Signal. This output should be connected to the 477/471 input of the RAMDAC (Bt477 or equivalent). This signal is used to access the control register of the RAMDAC and to allow it to be powered down. The logic level on this output can be controlled by setting Auxiliary Regiser [0B] bit 4, and is also controlled by the power save logic.

(continued)

- **External CRT/RAMDAC Interface (continued)**

Pin Name	Type	Pin #	Drv	Description
/IREFEN	O	47	TS2U3 (*C)	IREF Control output. This signal is used to control the external current reference source required by the RAMDAC, allowing powering down the analog circuitry when not required. When this signal is driven low, the external current reference should be enabled. When this signal is high, the external current reference should be shut off.
MS[2:0]	I	71, 82, 83	TTL	Monitor Sense inputs. There are internal pullups on each of these inputs. These signals should be connected to the monitor sense lines from the CRT monitor cable. The status of these bits is readable in Auxiliary register [08] bits 2:0, and is used by BIOS software to determine the presence and type of monitor connected. Optionally, the SENSE output of the RAMDAC may be connected to one of these inputs to allow the BIOS to read the SENSE signal and detect the monitor.

- **Power Save Mode Control**

Pin Name	Type	Pin #	Drv	Description
/SUSPEND	I	84	CS	A low level on this pin puts the chip into a hardware power down mode. The /SUSPEND signal overrides any software initiated power down modes, and disables the ISA-Bus interface inputs. Address and Data inputs are also masked when this signal is low. When in Suspend Mode the UD(3:0), LD(3:0), XSCL, and WF signals are driven into a high impedance or low state (configurable) and the /LCDPWR signal is driven high.
PDCLK	I	143	TTL	Power Down Clock. This input may be used to provide a low frequency clock for generating refresh in Power Save Modes 4 and Suspend, as an optional alternative to using the pixel clock or MEMEN input as the refresh clock source. This clock input should be driven by either a 64 kHz or 32 kHz clock source. If using a 32 kHz clock source, MD[14] must be set to 0 at reset. Refer to the SPC8108 Functional Specification for PDCLK support details. If the use of Power Save modes while driving a CRT monitor is required, then this PDCLK input must be driven by a 32 kHz clock, since this input is used to generate sync signals to the CRT when a Power Save Mode is enabled.

- **Power Supply**

Pin Name	Type	Pin #	Description
VDD	P	14,37,85,92,109	VDD supply for core logic.
VDD	P	1, 50, 73, 124	VDD supply for I/O pins.
VSS	P	11,36,88,89,108	VSS supply for core logic.
VSS	P	49, 72, 123, 144	VSS supply for I/O pins.

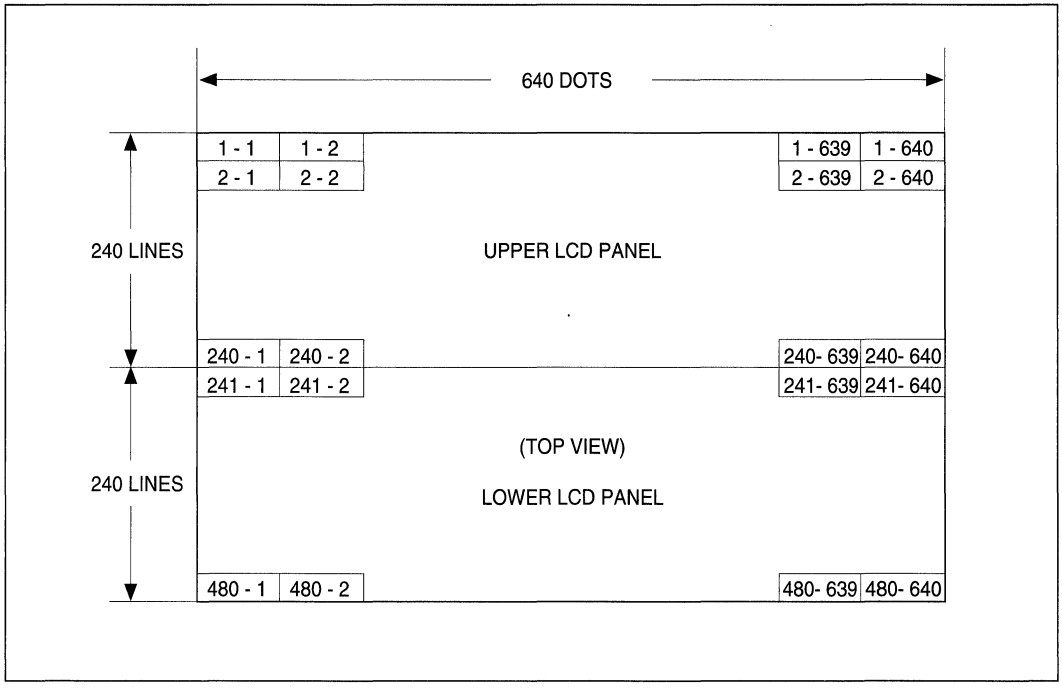
- **Configuration Options**

Pin Name	Value on this pin at falling edge of RESET is used to configure: (1/0)
MD[3:0]	Values latched into read-only Aux Reg[0C] bits 3:0 for software use
MD[4]	Reserved
MD[5]	A[19:2] latched internally by ALE (1) / standard ISA bus ALE - A[16:0] not latched (0) (this pin only has an effect if MD[4] = 1 at RESET)
MD[6]	2 CAS, 1 WE type DRAM (1) / 1 CAS, 2 WE type DRAM (0)
MD[7][8]	Reserved
MD[12:9]	Values latched into read-only bits 7:4 of Aux Reg[0C] for software use
MD[13]	Pins 38, 39 used for ext. RC for 32kHz PDCLK (1) / pins 38, 39 used for OL[1:0] (0)
MD[14]	Internal PDCLK disable (1) /enable (0)

- **LCD Panel Interface**

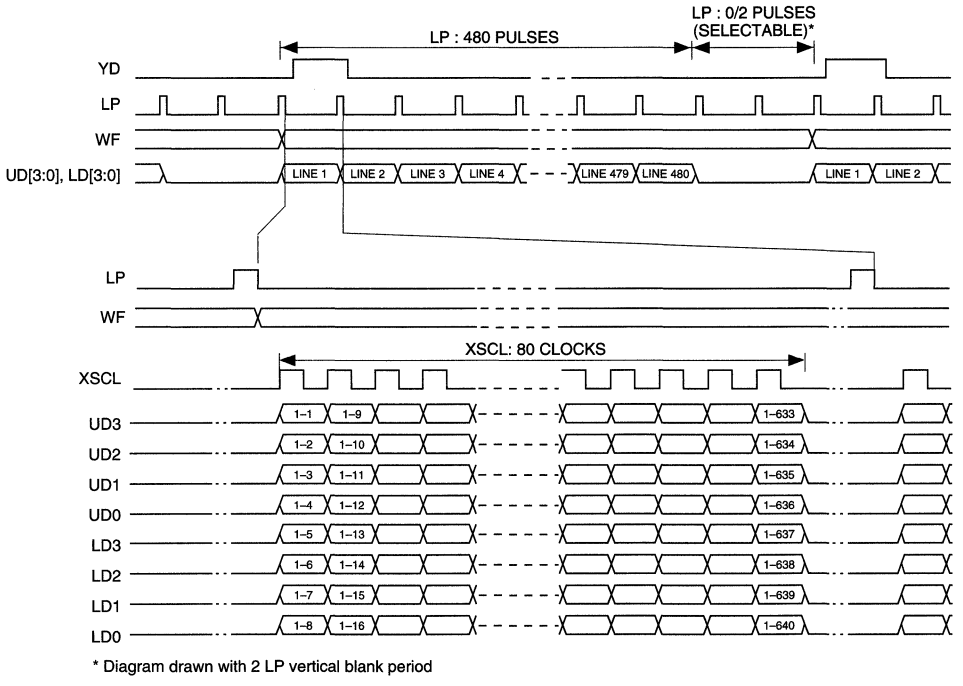
Pin Name	Type	Pin #	Drv	Description
YD	O	10	TS4	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	O	13	TS4	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O	12	TS4	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
UD[0:3]	O	22..25	TS4	Upper panel display data for dual panel - dual drive mode. For 8-bit single panel - single drive mode, these bits are the most significant 4 bits of the 8 bit output data to the panel (PD[4:7]). For 4 -bit single panel mode, these bits are the 4 bits of data output to the panel.
LD[0:3]	O	16..19	TS4	Lower panel display data for dual panel - dual drive mode. For 8-bit single panel - single drive mode, these bits are the least significant 4 bits of the 8 bit output data to the panel (PD[0:3]). For 4-bit single panel mode, these outputs are driven low.
/LCDPWR	O	21	TS2	LCD power control. In normal operation this signal is driven low to enable an external LCD power supply. This signal is driven high when the chip is put into any power save mode, or if the Sequencer is in a reset state. It can be used externally to turn off the panel supply voltage and backlight. After a RESET, this signal is held high until the CRTC is programmed and running.
WF	O	15	TS2	LCD Backplane Bias signal. This output can be programmed to toggle once per frame or once per 1-31 latch pulses (LP).

■ LCD Panel Pixels



■ LCD Panel Interface

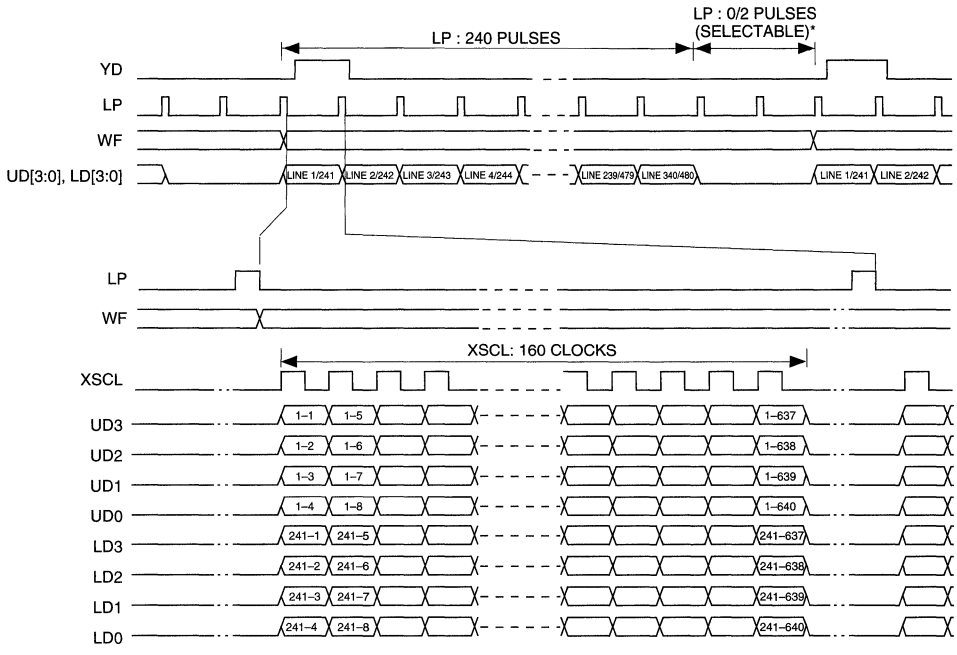
8-Bit Single Panel



* Diagram drawn with 2 LP vertical blank period

■ LCD Panel Interface

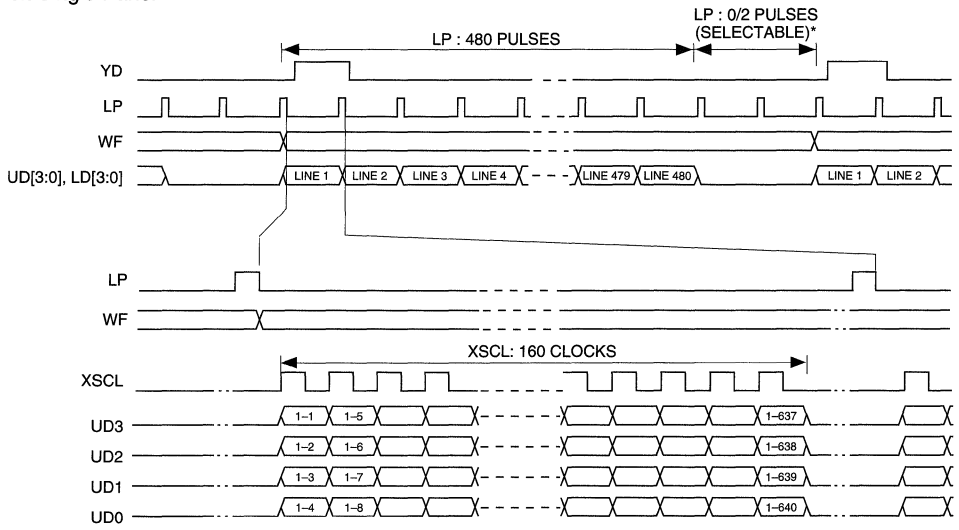
8-Bit Dual Panel



* Diagram drawn with 2 LP vertical blank period

■ LCD Panel Interface

4-bit Single Panel



* Diagram drawn with 2 LP vertical blank period
See Functional Specifications for variations in 4–bit timing.

LOCAL BUS LCD/CRT VGA CONTROLLER

■ DESCRIPTION

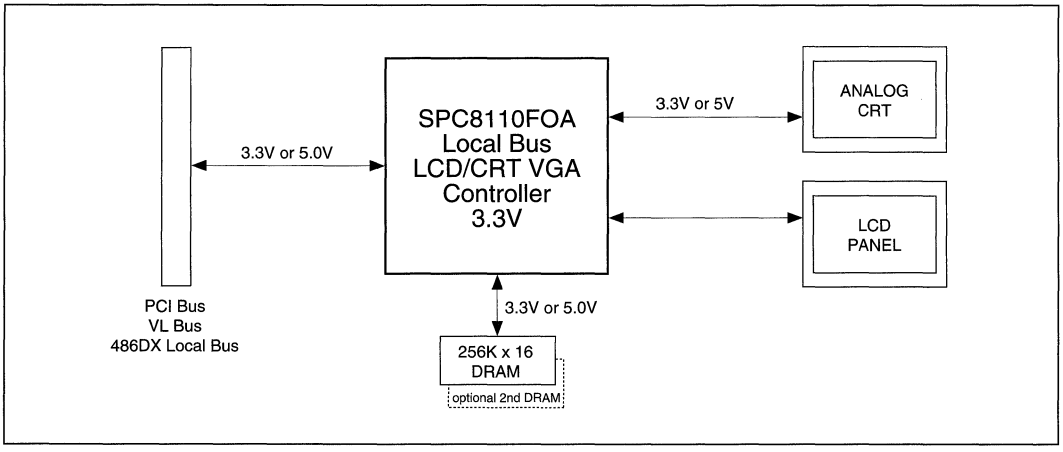
The SPC8110 is a single chip multi-function Low Voltage LCD & CRT VGA Controller with an integrated RAMDAC, PLL and a Liquid Crystal Display interface. With a built-in Hardware Cursor, a Bit Block Transfer Engine (BitBLT), and a CPU Local Bus Interface, the SPC8110 accelerates the display of Graphical User Interface software on Analog CRT Monitors and Single or Dual Panel Monochrome or Color LCD Displays.

Optimized for cost and power savings, the SPC8110 mixes 3.3 Volt 0.72 micron standard cell and gate array technology to achieve high density integration. Power consumption in 8-bit monochrome LCD modes is estimated to be 700 mW peak during extensive 32-bit 33 MHz Local Bus BitBLT operations, and 0.5 mW in standby with self-refresh DRAM.

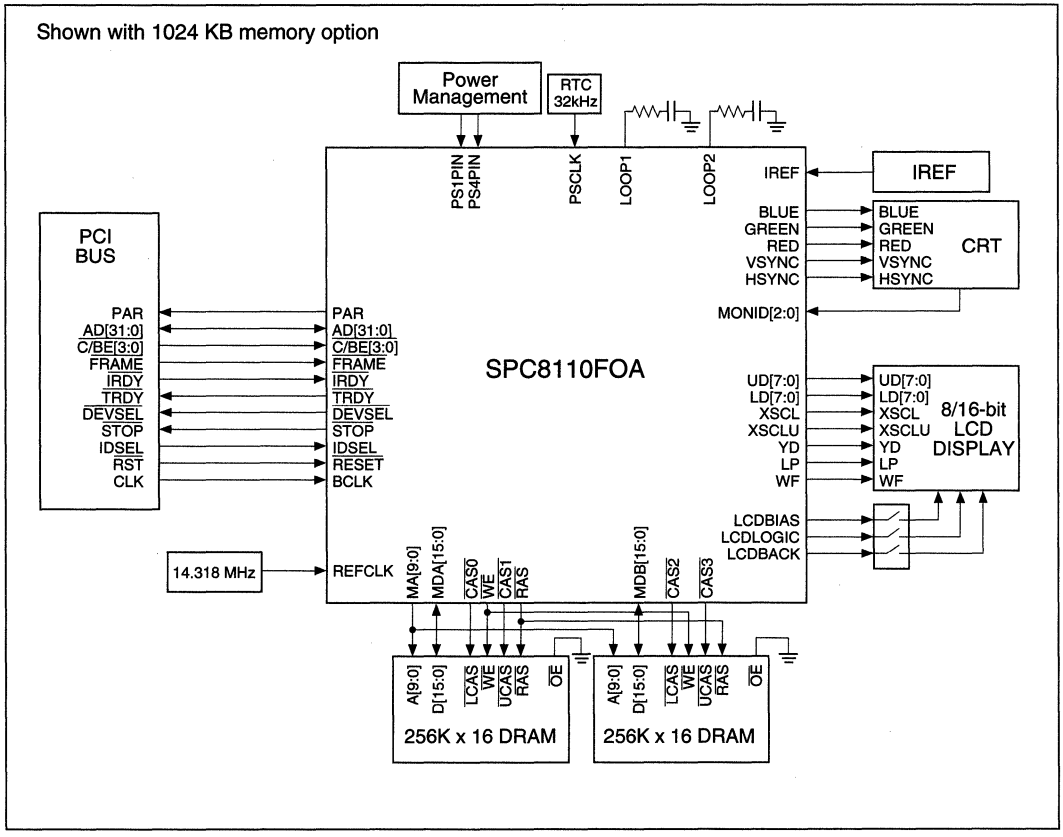
■ FEATURES

- Hardware VGA Compatible
- Mixed voltage 32-bit PCI, VL-Bus™ or 486DX local bus direct Interface
- 512KB or 1024KB display memory using one or two 256K x 16 self-refresh DRAM respectively (CAS or WE controlled; symmetrical or asymmetrical addressing)
- Hardware Bit Block Transfer Engine
- Hardware 64 x 64 pixel 2-bit Cursor
- Hardware Color Expansion
- 8 stage 32-bit Display Pipeline
- Linear Mode Addressing
- Internal PLL and Clock Generation
- Internal 256 x 18-bit RAMDAC
- Direct Analog CRT drive
- Mixed voltage multi-resolution LCD Panel Interface, Dual Panel-Dual Drive, Single Panel-Single Drive
- 16, 32 & 64 LCD Gray Shades by FRM and Dithering
- Up to 256K LCD Colors by Frame Rate Modulation (FRM) and Dithering
- Vertical Centering and Expansion
- Programmable Gray-scale Weighting and Contrast
- LCD Panel Power Sequencing
- Simultaneous LCD and Analog CRT display
- Extensive Hardware and Software activated Power Save Modes and Status Signals
- 208 pin QFP 28 x 28 mm Package
- 3.3 Volt Core Operating Voltage

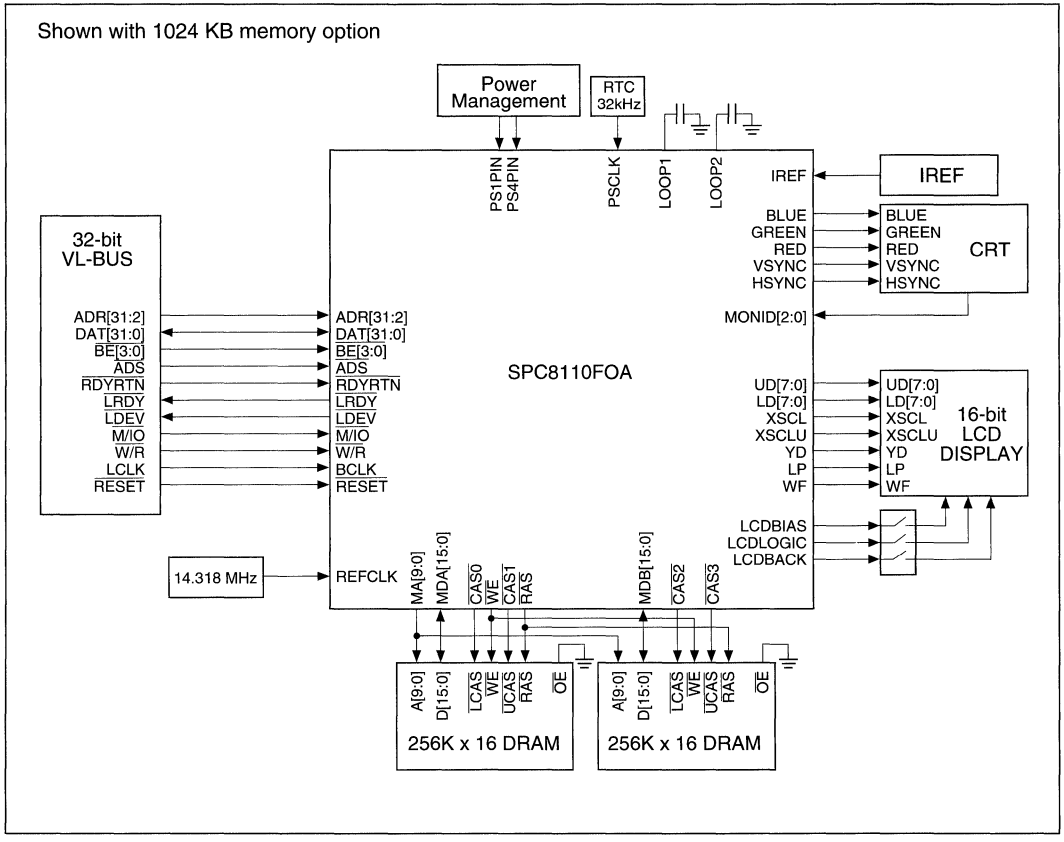
■ SYSTEM BLOCK DIAGRAM



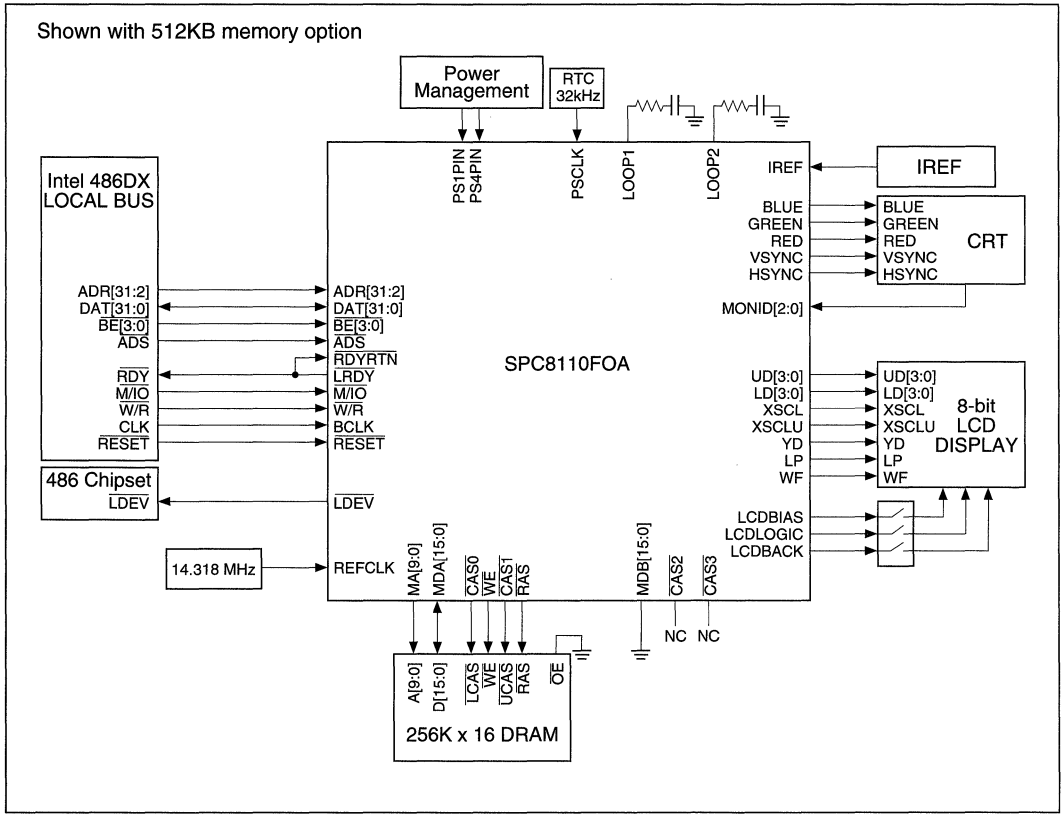
■ PCI BUS SYSTEM BLOCK DIAGRAM



■ VL-Bus SYSTEM BLOCK DIAGRAM



■ 486DX-33 LOCAL BUS SYSTEM BLOCK DIAGRAM



■ SPC8110 VIDEO MODES

Mode No. (Hex)	Pixels Addressable		Horiz. Pixels Displayed		Vertical Pixels Displayed	Font Size		No. of Shades			Frame Rate (Hz)		
	Horizontal (Chars.)	Vertical (Rows)	CRT	LCD		CRT	LCD	Mono LCD	Color LCD	CRT	CRT (Typical)	Single Panel LCD	Dual Panel LCD
0	(40)	(25)	320	320	200	8 X 8	8 X 8	16	16	16	70	79	78
0+	(40)	(25)	320	320	350	8 X 14	8 X 14	16	16	16	70	79	78
0++	(40)	(25)	360	320	400	9 X 16	8 X 16	16	16	16	70	79	78
1	(40)	(25)	320	320	200	8 X 8	8 X 8	16	16	16	70	79	78
1+	(40)	(25)	320	320	350	8 X 14	8 X 14	16	16	16	70	79	78
1++	(40)	(25)	360	320	400	9 X 16	8 X 16	16	16	16	70	79	78
2	(80)	(25)	640	640	200	8 X 8	8 X 8	16	16	16	70	79	78
2+	(80)	(25)	640	640	350	8 X 14	8 X 14	16	16	16	70	79	78
2++	(80)	(25)	720	640	400	9 X 16	8 X 16	16	16	16	70	79	78
3	(80)	(25)	640	640	200	8 X 8	8 X 8	16	16	16	70	79	78
3+	(80)	(25)	640	640	350	8 X 14	8 X 14	16	16	16	70	79	78
3++	(80)	(25)	720	640	400	9 X 16	8 X 16	16	16	16	70	79	78
4	320	200	320	320	200	N/A	N/A	4	4	4	70	79	78
5	320	200	320	320	200	N/A	N/A	4	4	4	70	79	78
6	640	200	640	640	200	N/A	N/A	2	2	2	70	79	78
7	(80)	(25)	640	640	350	8 X 14	8 X 14	2	2	2	70	79	78
7+	(80)	(25)	720	640	400	9 X 16	8 X 16	2	2	2	70	79	78
0D	320	200	320	320	200	N/A	N/A	16	16	16	70	79	78
0E	640	200	640	640	200	N/A	N/A	16	16	16	70	79	78
0F	640	350	640	640	350	N/A	N/A	2	2	2	70	79	78
10	640	350	640	640	350	N/A	N/A	16	16	16	70	79	78
11	640	480	640	640	480	N/A	N/A	2	2	2	60	79	78
12	640	480	640	640	480	N/A	N/A	16	16	16	60	79	78
13	320	200	320	320	200	N/A	N/A	64	256	256	70	79	78
6A	800	600	800	800	600	N/A	N/A	16	16	16	72	65	72
100	640	400	640	640	400	N/A	N/A	64	256	256	72	79	78
101	640	480	640	640	480	N/A	N/A	64	256	256	72	79	78
102	800	600	800	800	600	N/A	N/A	16	16	16	72	65	72
103	800	600	800	800	600	N/A	N/A	64	256	256	72	a65	72
104	1024	768	1024	1024	768	N/A	N/A	16	16	16	60	N/A	70
105	1024	768	1024	1024	768	N/A	N/A	64	N/A	256	N/A	60	70
108	(80)	(60)	640	640	480	8 X 8	8 X 8	16	16	16	60	79	78
109	(132)	(25)	1056	N/A	350	8 X 14	N/A	N/A	N/A	16	70	N/A	R
10A	(132)	(43)	1056	N/A	350	8 X 8	N/A	N/A	N/A	16	70	N/A	N
10B	(132)	(50)	1056	N/A	400	8 X 8	N/A	N/A	N/A	16	70	N/A	N
10C	(132)	(60)	1056	N/A	480	8 X 8	N/A	N/A	N/A	16	70	N/A	N

■ Display Resolution Support

The following three tables show the combinations of modes and display types supported by the SPC8110F0A with the maximum 40 MHz MClk.

Memory	Mode	640 x 480				
		CRT, TFT, Single STN Panel	Dual Mono STN Panel	Dual Color STN Panel	Simultaneous CRT & Dual Mono STN Panel	Simultaneous CRT & Dual Color STN Panel
512 K	0, 1	yes	yes	yes	yes	yes
512 K	2, 3, 7	yes	yes	yes	yes	[a]yes
512 K	fast ext	[b]yes	yes	yes	yes	[a]yes
512 K	4, 5	yes	yes	yes	yes	yes
512 K	planar	[c]yes	yes	yes	yes	yes
512 K	256	yes	yes	yes	[a]yes	[a]yes
1024 K	0, 1	yes	yes	yes	yes	yes
1024 K	2, 3, 7	yes	yes	yes	yes	[a]yes
1024 K	fast ext	[b]yes	yes	yes	yes	yes
1024 K	4, 5	yes	yes	yes	yes	yes
1024 K	planar	[c]yes	yes	yes	yes	yes
1024 K	256	yes	yes	yes	yes	yes

Notes: a. if half frame buffer is disabled.
b. fastext is Fast Text Mode
c. planar is 16 Color Planar Mode

Memory	Mode	800 x 600				
		CRT, TFT, Single STN Panel	Dual Mono STN Panel	Dual Color STN Panel	Simultaneous CRT & Dual Mono STN Panel	Simultaneous CRT & Dual Color STN Panel
512 K	0, 1	yes	yes	yes	—	—
512 K	2, 3, 7	—	yes	—	—	—
512 K	fast ext	[b]yes	yes	yes	—	—
512 K	4, 5	yes	yes	yes	—	—
512 K	planar	[c]yes	yes	yes	—	—
512 K	256	—	yes	—	—	—
1024 K	0, 1	yes	yes	yes	—	—
1024 K	2, 3, 7	—	yes	yes	—	—
1024 K	fast ext	[b]yes	yes	yes	—	—
1024 K	4, 5	yes	yes	yes	—	—
1024 K	planar	[c]yes	yes	yes	—	—
1024 K	256	yes	yes	yes	—	—

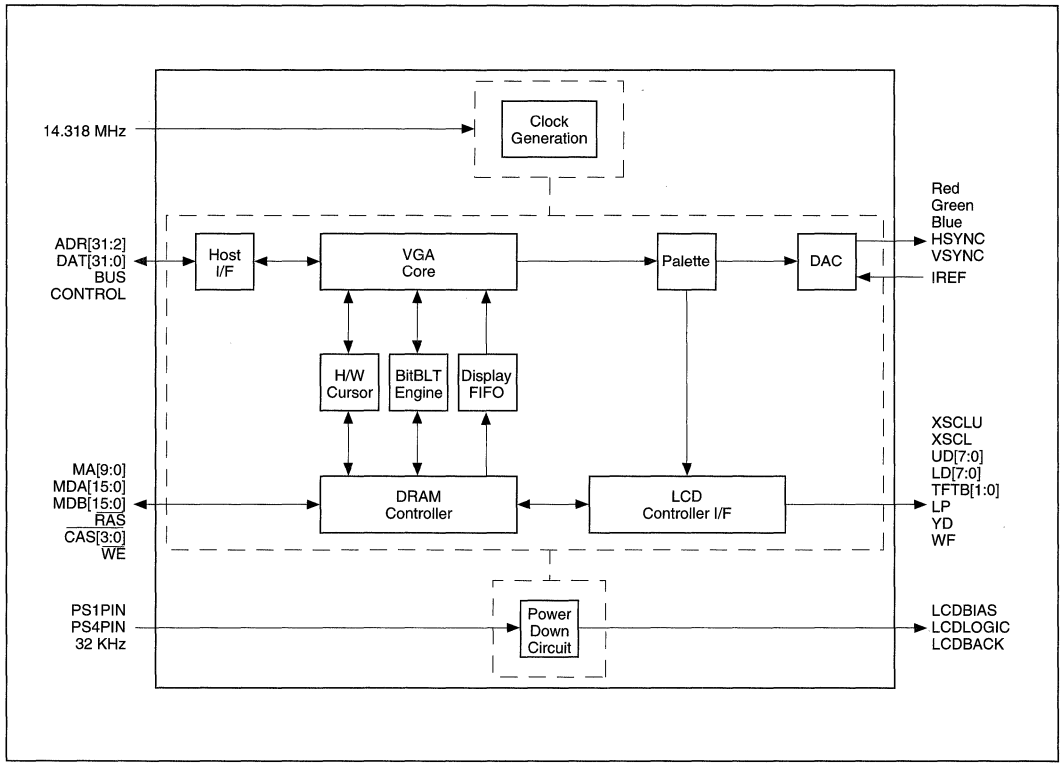
Notes: a. fastext is Fast Text Mode
b. planar is 16 Color Planar Mode

Memory	Mode	1024 x 768				
		CRT, TFT, Single STN Panel	Dual Mono STN Panel	Dual Color STN Panel	Simultaneous CRT & Dual Mono STN Panel	Simultaneous CRT & Dual Color STN Panel
512 K	0, 1	yes	yes	—	—	—
512 K	2, 3, 7	—	—	—	—	—
512 K	fast ext	—	yes	—	—	—
512 K	4, 5	yes	yes	yes	—	—
512 K	planar	cyes	yes	—	—	—
512 K	256	—	—	—	—	—
1024 K	0, 1	yes	yes	yes	—	—
1024 K	2, 3, 7	—	—	—	—	—
1024 K	fast ext	—	yes	—	—	—
1024 K	4, 5	yes	yes	yes	—	—
1024 K	planar	cyes	yes	yes	—	—
1024 K	256	yes	yes	—	—	—

Notes: a. fastext is Fast Text Mode

b. planar is 16 Color Planar Mode

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

Host Interface

The Host interface can be programmed to interface to any of the following three standards: 486DX local bus interface, VL-Bus interface, and PCI interface. It has a one-stage buffer for zero wait-state write operation.

Clock Generator

The clock generator contains two PLL's that are separately programmed to produce the memory and pixel clocks from a single clock source. The reference clock is typically 14.318 MHz.

VGA Core

The VGA Core contains the Sequencer, CRTC Controller, Graphics Controller, Attribute Controller, and the rest of the standard VGA circuitry.

Hardware Cursor

The Hardware Cursor block generates a 4 gray shade or color, 64 x 64 x 2-bit hardware cursor/sprite that can be overlaid on the displayed image.

Bit Block Transfer (BitBLT) Engine

The Bit Block Transfer Engine performs read, write, move BLTs, solid fills, destination inversions, and pattern fills. It performs all data alignment and masking at the BLT boundary. It also performs text expansion to accelerate the writing of monochrome images. It operates in both 4-bit planar mode and 8-bit linear (packed-pixel) mode.

Display FIFO

This is an 8 stage by 32-bit FIFO that is used to buffer the video data from display memory.

VGA Palette

This block implements the standard 256 x 18 VGA lookup table.

DAC

This block functions as a triple 6-bit 65 MHz DAC to drive the RGB outputs connected to the analog monitor.

LCD Interface

This block contains frame rate modulation and dithering circuitry for a maximum of 64 shades of gray in monochrome single and dual panel modes. In color LCD mode, it uses frame rate modulation to generate 4K colors, and additional dithering techniques for a full 256K colors.

Power Save Logic

This block implements all the power down features of the chip.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameters	Codes	Rating	Units
Supply voltage	V_{DD}	V_{SS}–0.3 to +7.0	V
Input voltage	V_{IN}	V_{SS}–0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	V_{SS}–0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	–65 ~ 150	°C
Soldering temperature/time	T_{SOL}	260 for 10 sec max at lead	°C

● Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Supply voltage	HV_{DD}	V_{SS} = 0V	4.5	5.0	5.5	V
Supply voltage	LV_{DD}	V_{SS} = 0V	3.0	3.3	3.6	V
Input voltage	V_{IN}	V_{SS}	V_{SS}	—	V_{DD}	V
Operating temperature	T_{OPR}		0	25	70	°C

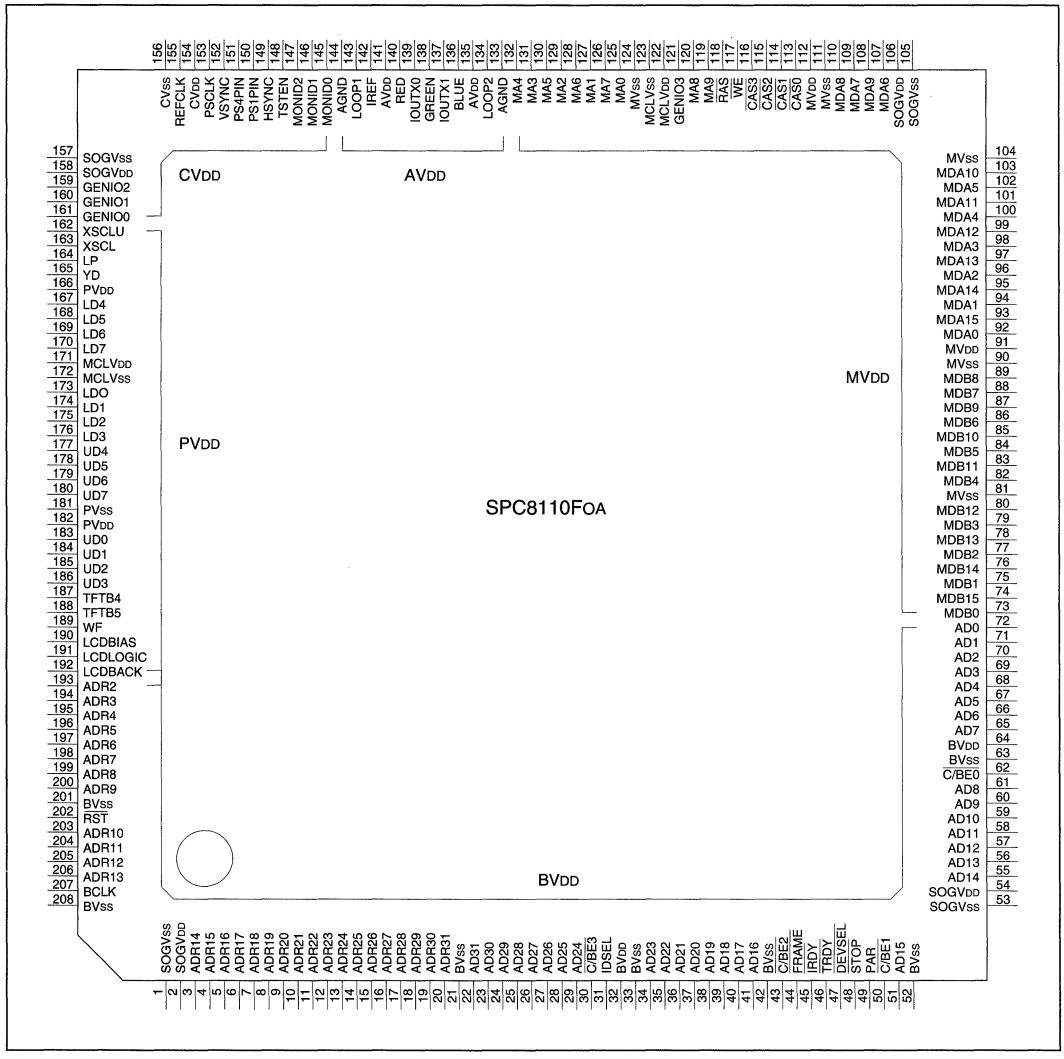
● Input Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low level input voltage	V_{IL}	V_{DD} =4.5 V/3.0 V			0.8	V
High level input voltage	V_{IH}	V_{DD} = 5.5 V/3.6 V	2.0			V
Pull down resistance	HR_{PD}	V_{DD} = 5.0V	25	50	100	KΩ
Pull down resistance	LR_{PD}	V_{DD} = 3.3V	45	90	180	KΩ
Positive-going threshold CMOS Schmitt Trigger	VT_+	V_{DD} = 5./3.3V			2.4	V
Negative-going threshold CMOS Schmitt Trigger	V_{T-}	V_{DD} = 5./3.3V	0.6			V
Hysteresis voltage CMOS Schmitt Trigger	HV_H	V_{DD} =5./3.3V	0.1			V
Clock pin capacitance	C_{IN}	BCLK,RESET#,REFCLK, MONID [2:0], TSTENPSIPIN, PS4PIN, PSCLK		4		pF
Input pin capacitance	C_{BID}	All pins not listed in C_{IN}		10		pF
Input leakage current	I_L	V_{DD} =MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1		1	µA

● Output Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low level output voltage Type 2 Type 3 Type 4	V_{OL}	V_{DD} = 5 /3.3 V I_{OL} = 6mA I_{OL} = 12mA I_{OL} = 24mA			V_{SS} + 0.3	V
High level input voltage Type 2 Type 3 Type 4	V_{0H}	V_{DD} = 5 /3.3 V I_{OH} = –2mA I_{OH} = –4mA I_{OH} = –8mA	V_{DD} – 0.3			V
Off-state leakage current	I_{OZ}	V_{DD} =MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1		1	µA

■ SPC8110 PIN OUT



Note: Pin names correspond to the PCI bus configuration.

Pin placement subject to change.

■ PIN DESCRIPTION

Key

A = Analog
I = Input
O = Output
I/O = Bi-directional
P = Power

● CPU Interface

PCI Bus

Pin Name	Type	Pin #	Description
AD [31:0]	I/O	22-29, 34-41 51, 55-61 65-72	PCI multiplexed address and data Bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times.
ADR [31:2	I	20-3, 206-203, 200-193	Unused VL-bus address inputs. These pins should be tied high in PCI mode.
C/BE [3:0]#	I	30, 43, 50, 62	PCI bus command and byte enables.
IDSEL	I	31	PCI bus initialization device select.
STOP#	I/O	48	PCI bus stop
FRAME#	I	44	PCI bus cycle frame
IRDY#	I	45	PCI bus initiator ready.
PAR	O	49	Parity. This line is driven by the chip onlyu during read cycles, and is in a hi-Z state at alll other times. It is always hi-Z and should be tied high in VL bus mode.
BCLK	I	207	PCI bus clock
TRDY#	I/O	46	PCI bus target ready
DEVSEL#	O	47	PCI bus device select
RST#	I	202	CPU reset. The active low reset signal from the CPU clears all internal registers and forces all signals to their inactive state. On the rising edge of the RESET# the MDA [0...15] bus is latched in for configuration.

Intel486/VL-Bus

Pin Name	Type	Pin #	Description
ADR [31:2]	I	20-3,206-203, 200-193	VL-bus address inputs. These pins should be tied high in PCI bus mode.
DAT [31:0]	I/O	22-29, 34-41, 51,55-61, 65-72	VL-bus Data inputs. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times
BE [3:0]#	I	30, 43, 50, 62	VL- bus byte enables.
W/R#	I	31	VL- bus write or read status
M/IO#	I	48	VL- memory or I/O status
ADS#	I	44	VL- bus address data strobe
RDYRTN#	I	45	VL- bus ready return
BCLK	I	207	VL- bus local CPU clock
LRDY#	O	46	VL- bus local ready
LDEV#	O	47	PCI bus local device
RST#	I	202	CPU reset. The active low reset signal from the CPU clears all internal registers and forces all signals to their inactive state. On the rising edge of the RESET# the MDA [0...15] bus is latched in for configuration.
PAR	O	49	Unused (Parity)s. This line is used in PCI mode only. It is hi-Z state at all times in VL mode and should be tied high

- **Video Memory Interface**

Pin Name	Type	Pin#	Description
MA[9:0]	O	119, 120, 126, 128, 130, 132, 131, 129, 127, 125	Multiplexed row/column address bits for video display memory.
MDA[15:0]	I/O	93, 95, 97, 99, 101, 103, 108, 110, 109, 107, 102, 100, 98, 96, 94, 92	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET# is low, or when MClkOFF is active. The inputs have internal pulldown resistors that have typical values of 50KΩ100KΩ at 5V/3.3V respectively.
MDB[15:0]	I/O	74, 76, 78, 80, 83, 85, 87, 89, 88 86, 84, 82 79, 77, 75, 73	Data bits for video display memory when 1024KB of memory is present The output drivers of these pins are placed into a high-impedance state when RESET# is low, or when MClkOFF is active. The inputs have internal pulldown resistors that have typical values of 50KΩ100KΩ at 5V/ 3.3Vrespectively. They should be left open-circuit when only 512KB of memory is attached.
RAS#	O	118	DRAM Row Address Strobe
CAS[0]# (CAS#)	O	113	DRAM Column Address Strobe for MDA[7:0], or Column Address Strobe for all bytes, as configured by AUX [03h] bit 7.
CAS[3:1]# (WE[3:1]#)	O	116-114	DRAM Column Address Strobes or Write Enable Strobes for {MDB[15:0], MDA[15:8]}, as configured by AUX[03h] bit 7. CAS[3:2]# (WE[3:2]#) are unused and should be left open-circuit when only512KB of memory is present.
WE# (WE[0]#)	O	117	DRAM Write Enable Strobe for all bytes or Write Enable Strobe for MDA[7:0], as configured by AUX[03h] bit 7.

- **Clock Inputs**

Pin Name	Type	Pin#	Description
REFCLK	I	155	This pin is the reference clock used by the internal PLLs to generate all the necessary clocks. This must be stable during full operation. REFCLK may shut down only after the chip is totally powered down. Input frequency is typically 14.318 MHz.
PSCLK	I	153	Power Save Clock. This input must be used to provide a low frequency clock for generating refresh. This clock must be approximately 32 kHz and 50% duty cycle.

- **CRT Interface**

Pin Name	Type	Pin#	Description
RED,A GREEN, BLUE	AO	140, 138, 136	Analog outputs from the Video DAC. Internal comparator for monitor sense is available on all three pins.
HSYNC	O	149	Horizontal Sync. This output is driven to indicate the horizontal retrace period. In CRT only mode, the polarity of this signal is controlled by register 3C2h, bit 6. In TFT or double scan mode this bit is active low to indicate 640 x 480 resolution. This pin is held low in LCD modes. sThis pin follows the DPMS standard during power down modes.
VSYNC	O	152	Vertical Sync. This output is driven to indicate the vertical retrace period. In CRT only mode, the polarity of this signal is controlled by register 3C3h bit 7. In TFT or double scan mode this bit is active low to indicate 640 x 480 resolution. This pin is held low in LCD modes. This pin follows the DPMS standard during power down modes.
IREFA	AI	142	Current reference input for the Video DAC.
MONID[2:0]	I	147-145	Monitor ID bits. Connected to the CRT to identify the monitor type.

- **LCD Panel Interface**

Pin Name	Type	Pin#	Description
YD	O	165	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	O	164	Latch Pulse ouput. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O	163	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
XSCLU	O	162	Second Shift Clock for some color LCD displays.
UD[7:0] LD[7:0]	I/O	180-177, 186-183, 170-167 176-173	Panel display data bus. The data format depends on the specific panel connected. These pins are driven low when the LCD interface is disabled (e.g. CRT only mode). For 8-bit panels, UD[7:4] and LD [7:4] are driven low.
TFTB[5:4]	O	188-187	TFT display data bus for the two lsb of the color blue. For non-TFT panels, these two pins are driven low.
LCDBIAS	O	190	LCD power control for the LCD bias circuitry. Active (On) polarity is defined by the state of MDA[3] on the rising edge of RESET#.
LCDBACK	O	192	LCD power control for the LCD back light. Active (On) polarity is defined by the state of MDA[1] on the rising edge of RESET#.
LCDLOGIC	O	191	LCD power control for the LCD logic circuitry. Active (On) polarity is defined by the state of MDA[2] on the rising edge of RESET#.
WF	O	189	LCD Backplane Bias signal. Output toggling frequency is programmable in an auxiliary register. For TFT panels, this pin outputs the display enable signals.

- **Miscellaneous**

Pin Name	Type	Pin#	Description
TSTEN	I	148	This pin, when high, sets the SPC8110F0A into either boundary pin SCAN or pin output drive test, depending on the state of PS1PIN. This input has an internal pull down resistor that has a typical value of 50K/100KΩ at 5 V/3.3 V respectively.
GENIO[3:0]	I/O	121, 159, 160, 161	Three General purpose I/O pins. Output state of each pin is programmable to control external devices.
LOOP1	I	143	Connects to Loop Filter Capacitor for PLL1
LOOP2	I	134	Connects to Loop Filter Capacitor for PLL2
IOUTX[1:0]	A	137, 139	Balanced current output for the DAC.

- **Power Save Mode Controls**

Pin Name	Type	Pin#	Description
PS1PIN	I	150	Pin used to initiate a power save mode 1. The polarity of this pin is programmable and has a default polarity of active low. This input has an internal pull down resistor that has a typical value of 50K/100K Ω at 5 V/3.3 V respectively. When TSTEN is active, the polarity of PS1PIN selects the test to be either boundary pin SCAN (PS1PIN = 1) or pin output drive test (PS1PIN = 0)
PS4PIN	I	151	Pin used to initiate a power save mode 4. The polarity of this pin is programmable and has a default polarity of active low. This input has an internal pull down resistor that has a typical value of 50K/100K Ω at 5 V/3.3 V respectively.

- **Power Supply**

Pin Name	Type	Pin #	Description
$SOGV_{DD}$	P	158, 106, 54, 2	V_{DD} supply for 3.3V core logic
MV_{DD}	P	112, 91	V_{DD} supply for memory pins
BV_{DD}	P	32, 64	V_{DD} supply for bus interface pins
CV_{DD}	P	154	V_{DD} supply for control interface pins
PV_{DD}	P	166, 182	V_{DD} supply for panel interface pins
AV_{DD}	P	135, 141	Analog power supply
$SOGV_{SS}$	P	157, 105, 53, 1	V_{SS} supply for 3.3 V core logic
MV_{SS}	P	111, 124, 104, 90, 81	V_{SS} supply for memory pins
BV_{SS}	P	201, 208, 21, 42, 52, 33, 63	V_{SS} supply for bus interface pins
CV_{SS}	P	156	V_{SS} supply for control interface pins
PV_{SS}	P	181	V_{SS} supply for panel interface pins
AGND	P	133, 144	Analog ground
$MCLV_{DD}$	P	122, 171	V_{DD} supply for
$MCLV_{SS}$	P	123, 172	V_{SS} supply for

■ Intel486/VL-Bus to PCI Bus Pin Mapping

VL-Bus Name	PCI Name	Pin No.
RESET#	RST#	202
RDYRTN#	IRDY#	45
ADR [31:2]	—	20-3, 206-203, 200-193
W/R#	IDSEL	31
LDEV#	DEVSEL#	47
DAT [31:0]	AD [31:0]	22-29, 34-41, 51, 55-61, 65-72

VL-Bus Name	PCI Name	Pin No.
BCLK	BCLK	207
—	PAR	49
M/IO#	STOP	48
ADS#	FRAME	44
LRDY#	TRDY#	46
BE [3:0]#	C/BE [3:0]	30, 43, 50, 62

■ MIXED VOLTAGE OPERATION

Mixed Voltage	$SOGV_{DD}$ $MCLV_{DD}$ AV_{DD}	BV_{DD}	CV_{DD}	PV_{DD}	MV_{DD}
Configuration 1	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Configuration 2					5.0 V
Configuration 3				5.0 V	3.3 V
Configuration 4					5.0 V
Configuration 5			5.0 V	3.3 V	3.3 V
Configuration 6					5.0 V
Configuration 7				5.0 V	3.3 V
Configuration 8					5.0 V
Configuration 9		5.0 V	3.3 V	3.3 V	3.3 V
Configuration 10					5.0 V
Configuration 11				5.0 V	3.3 V
Configuration 12					5.0 V
Configuration13			5.0 V	3.3 V	3.3 V
Configuration 14					5.0 V
Configuration 15				5.0 V	3.3 V
Configuration 16					5.0 V

■ Default Pin Mapping for the Various LCD and TFT Panel Options

(AUX[07] bit 2 = 0)

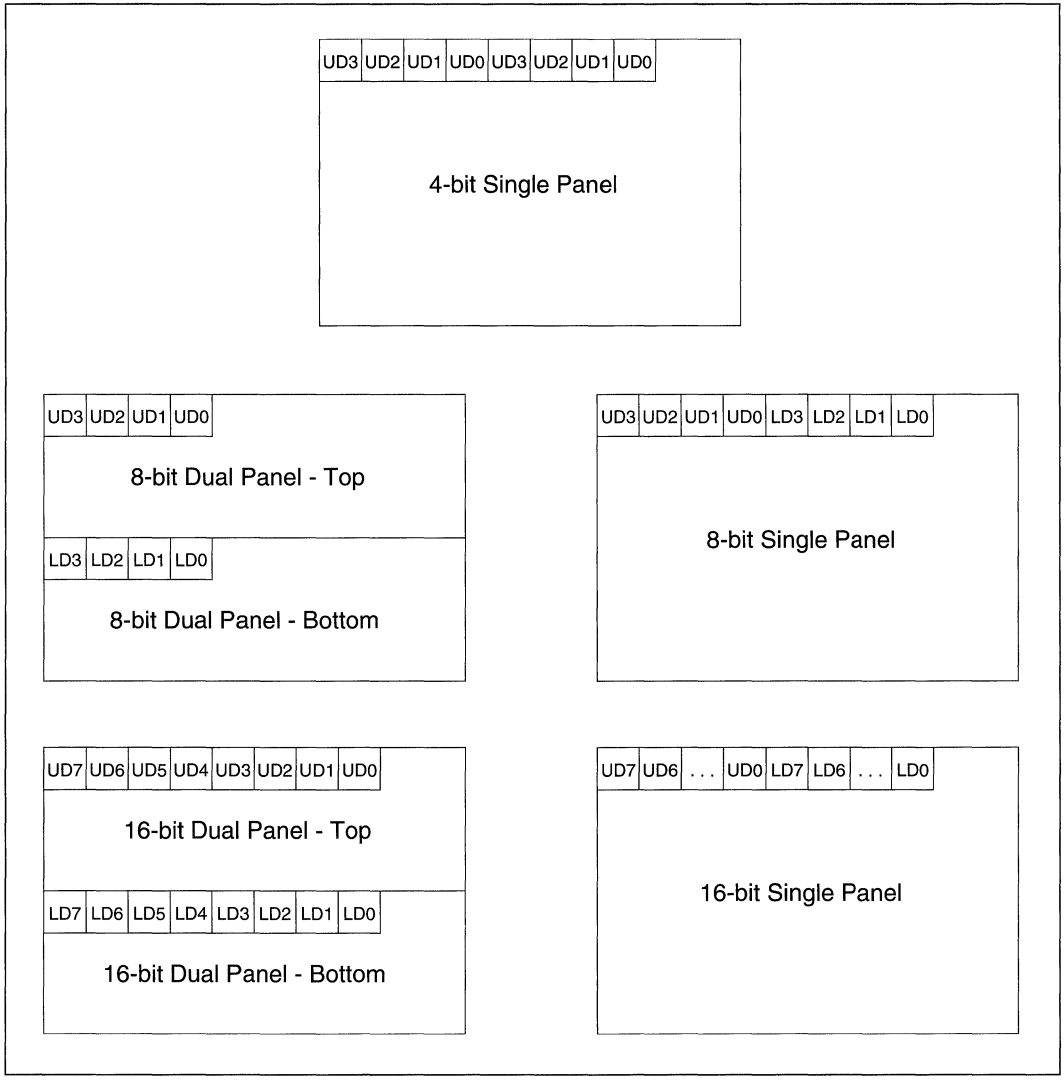
Pin Name	TFT			Color LCD				Mono LCD	
	18-Bit Color	12-Bit Color	9-Bit Color	16-Bit	8-Bit Half Panel	8-Bit	6-Bit	8-Bit	4-Bit
XSCLU	CLK	CLK	CLK			XSCLU			
XSCL				XSCL	XSCL	XSCL	XSCL	XSCL	XSCL
LP	HS	HS	HS	LP	LP	LP	LP	LP	LP
YD	VS	VS	VS	YD	YD	YD	YD	YD	YD
LD4	R0			LD4				UD0	UD0
LD5	R1			LD5				UD1	UD1
LD6	R2	R0		LD6				UD2	UD2
LD7	R3	R1	R0	LD7				UD3	UD3
LD0	R4	R2	R1	LD0		LD0	LB	LD0	
LD1	R5	R3	R2	LD1		LD1	LG	LD1	
LD2	G0			LD2		LD2	LR	LD2	
LD3	G1			LD3		LD3		LD3	
UD4	G2	G0		UD4	UD4				
UD5	G3	G1	G0	UD5	UD5				
UD6	G4	G2	G1	UD6	UD6				
UD7	G5	G3	G2	UD7	UD7				
UD0	B0			UD0	UD0	UD0	UB		
UD1	B1			UD1	UD1	UD1	UG		
UD2	B2	B0		UD2	UD2	UD2	UR		
UD3	B3	B1	B0	UD3	UD3	UD3			
TFTB4	B4	B2	B1						
TFTB5	B5	B3	B2						
WF	DE	DE	DE	WF	WF	WF	WF/DE	WF	WF
LCDBIAS				(DISP)	(DISP)	(DISP)	(DISP)	(DISP)	(DISP)

■ Alternate Pin Mapping for the Various LCD and TFT Panel Options

(AUX[07] bit 2 = 1)

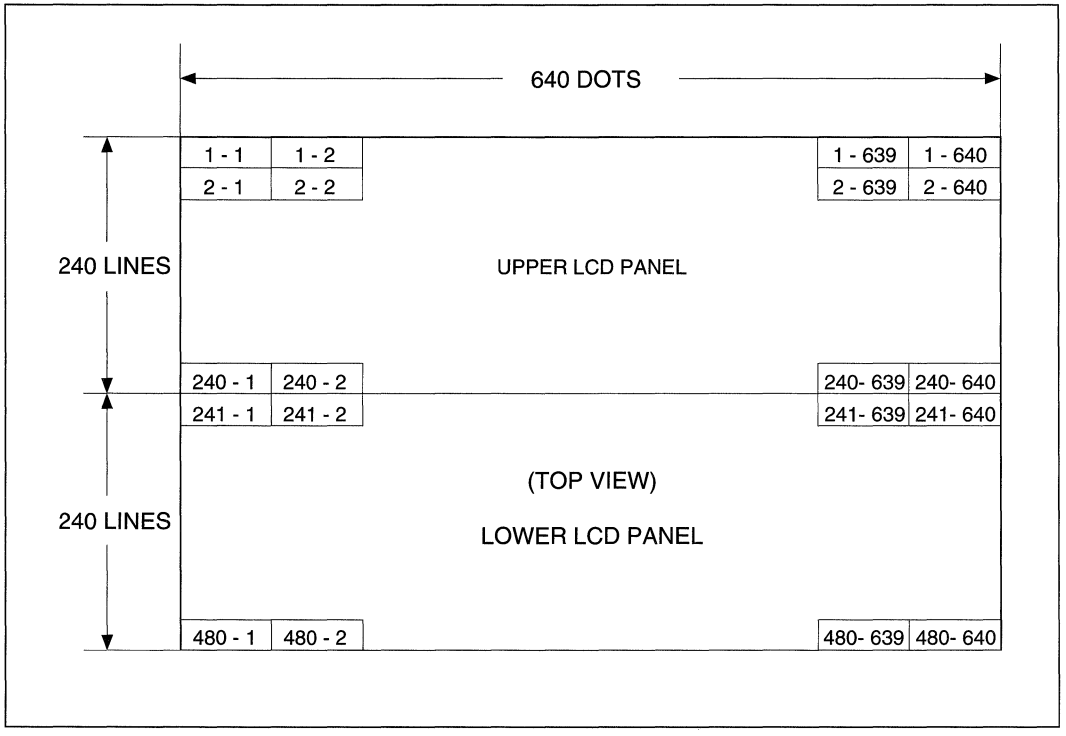
Pin Name	TFT			Color LCD		Mono LCD	
	18-Bit Color	12-Bit Color	9-Bit Color	16-Bit	8-Bit	8-Bit Single	4-Bit x 2 Dual
XSCLU	CLK	CLK	CLK		XSCLU		
XSCL				XSCL	XSCL	XSCL	XSCL
LP	HS	HS	HS	LP	LP	LP	LP
YD	VS	VS	VS	YD	YD	YD	YD
LD4	R0						
LD5	R1						
LD6	R2	R0		UD0	UD0		
LD7	R3	R1	R0	UD1	UD1	D6	UD2
LD0	R4	R2	R1	UD2	UD2	D7	UD3
LD1	R5	R3	R2	UD3	UD3		
LD2	G0			UD4			
LD3	G1			UD5			
UD4	G2	G0		LD4			
UD5	G3	G1	G0	LD5		D3	LD3
UD6	G4	G2	G1	LD6		D4	UD0
UD7	G5	G3	G2	LD7		D5	UD1
UD0	B0			UD6			
UD1	B1			UD7			
UD2	B2	B0		LD0	LD0		
UD3	B3	B1	B0	LD1	LD1	D0	LD0
TFTB4	B4	B2	B1	LD2	LD2	D1	LD1
TFTB5	B5	B3	B2	LD3	LD3	D2	LD2
WF	DE	DE	DE	WF	WF	WF	WF
LCDBIAS				(DISP)	(DISP)	(DISP)	(DISP)

Illustrated below is the display data output as displayed on the panel:



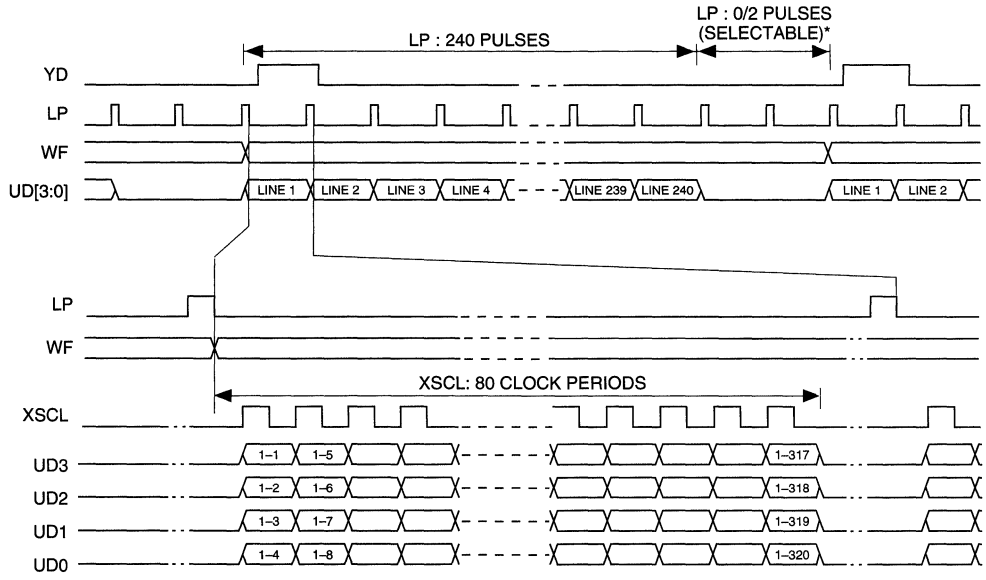
■ LCD Panel Pixels

The figure below shows the pixel layout for a 640x480 dual panel.



■ Monochrome Passive STN LCD Panel Interface

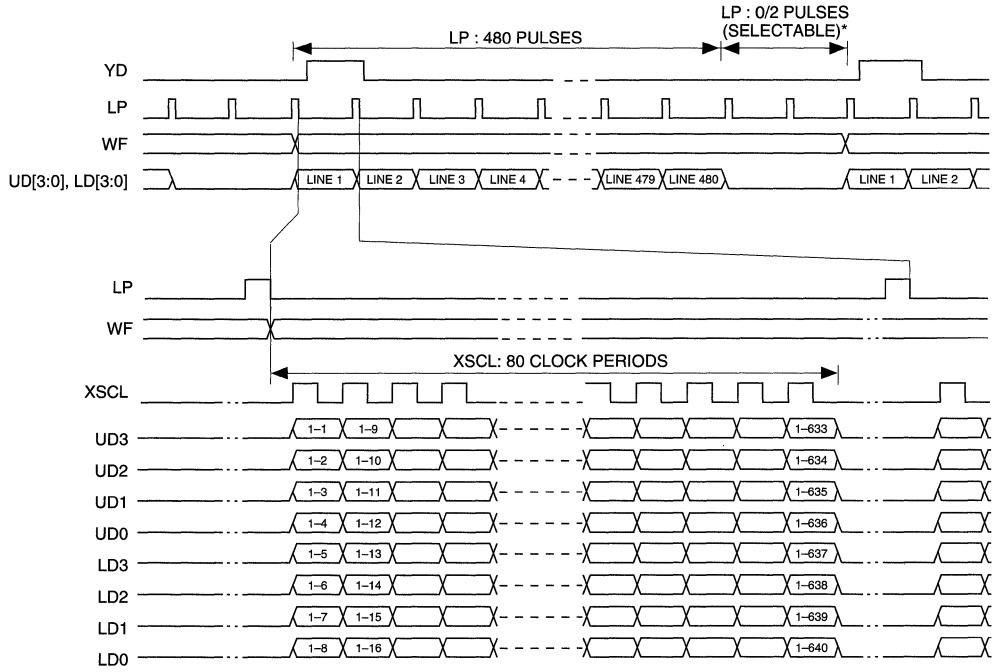
4-bit Single Panel



* Diagram drawn with 2 LP vertical blank period
Example timing for a 320 × 240 panel

■ Monochrome Passive STN LCD Panel Interface

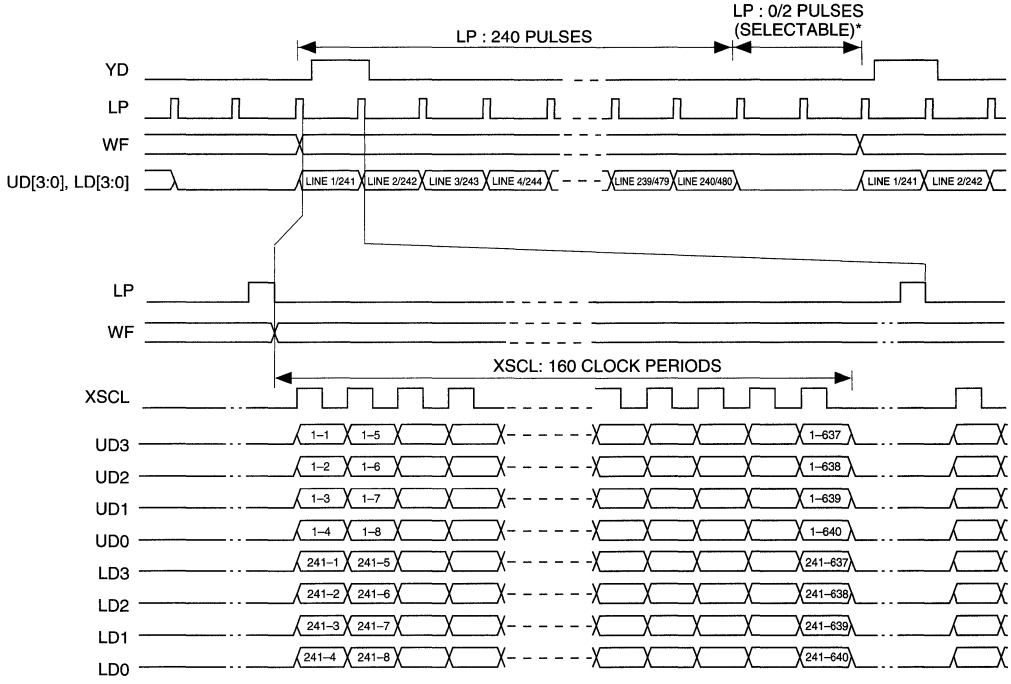
8-bit Single Panel



* Diagram drawn with 2 LP vertical blank period
Example timing for 640 × 480 panel

■ Monochrome Passive STN LCD Panel Interface

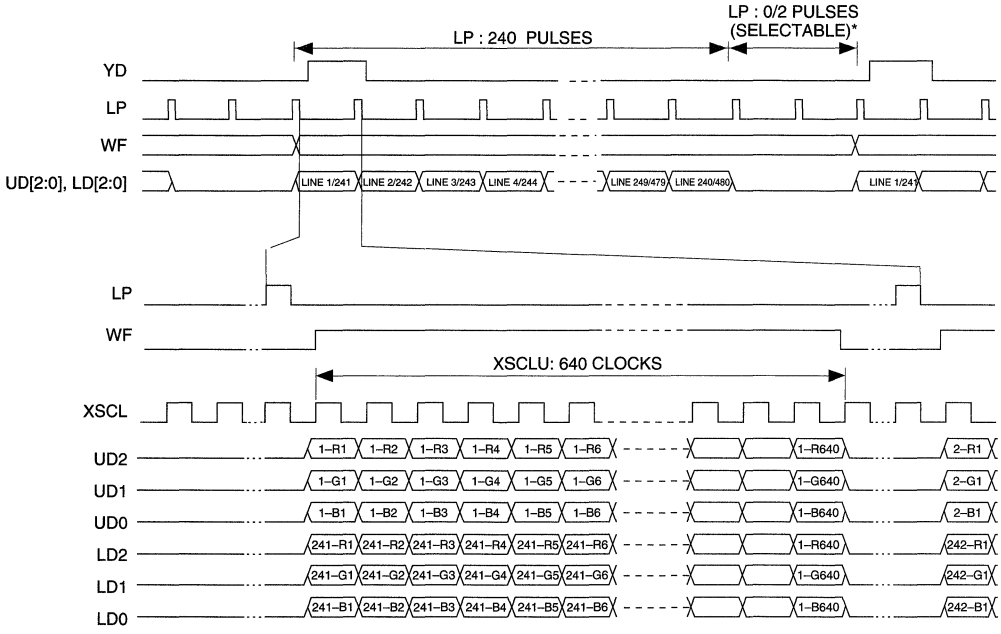
8-bit Dual Panel



* Diagram drawn with 2 LP vertical blank period
Example timing for 640 × 480 panel

■ Color Passive STN LCD Panel Interface

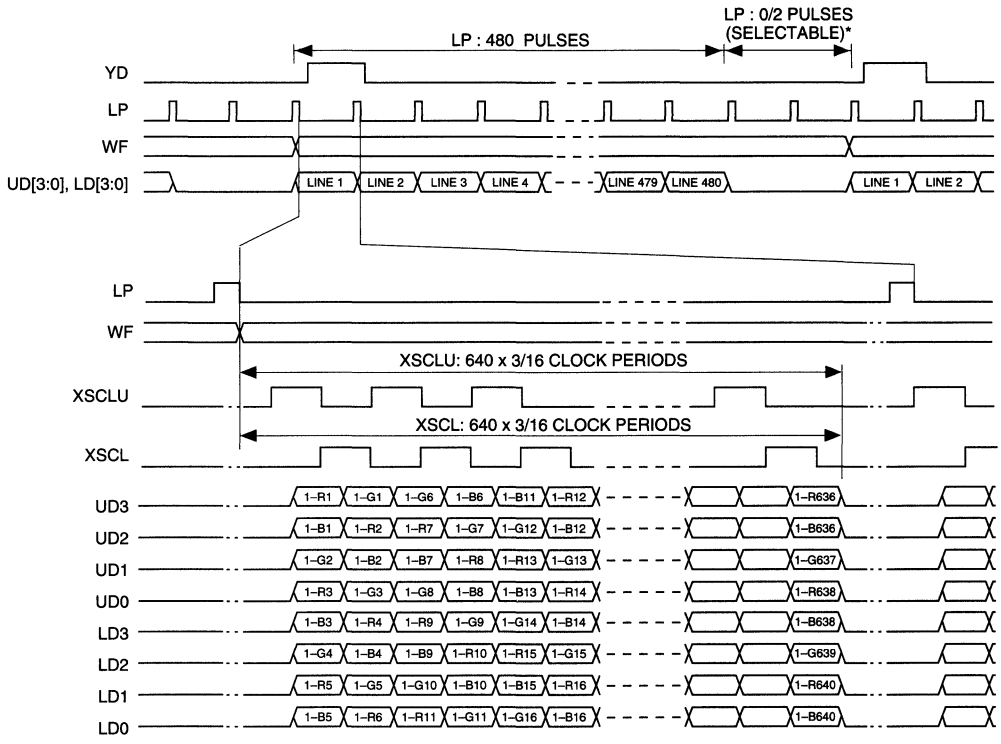
6-bit Dual Color Panel



* Diagram drawn with 2 LP vertical blank period
Example timing for 640 × 480 panel

■ Color Passive STN LCD Panel Interface

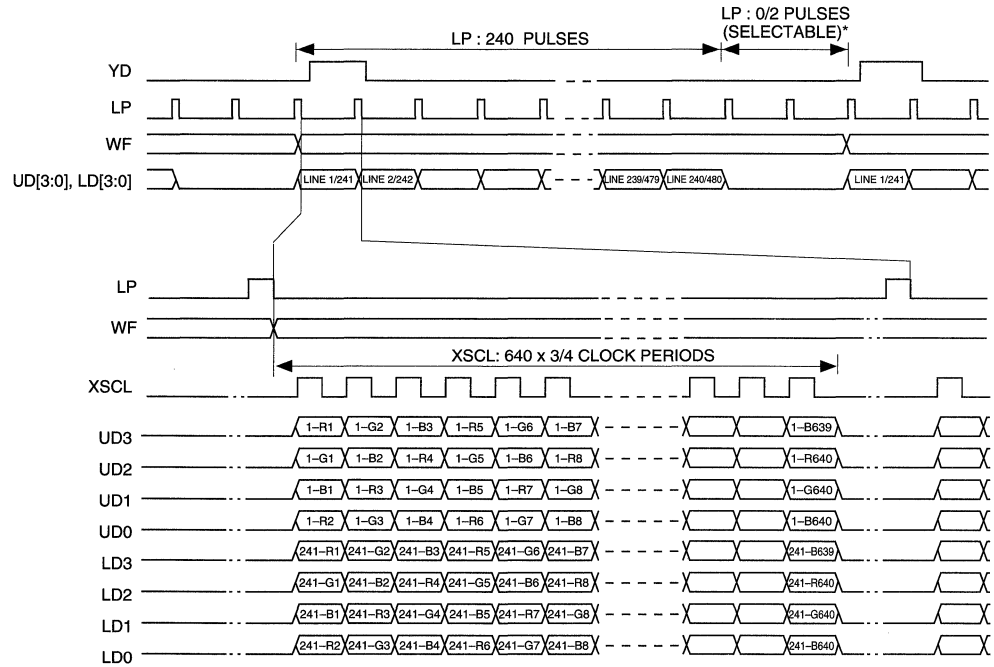
8-bit Single Color Panel



* Diagram drawn with 2 LP vertical blank period
Example timing for 640 × 480 panel

■ Color Passive STN LCD Panel Interface

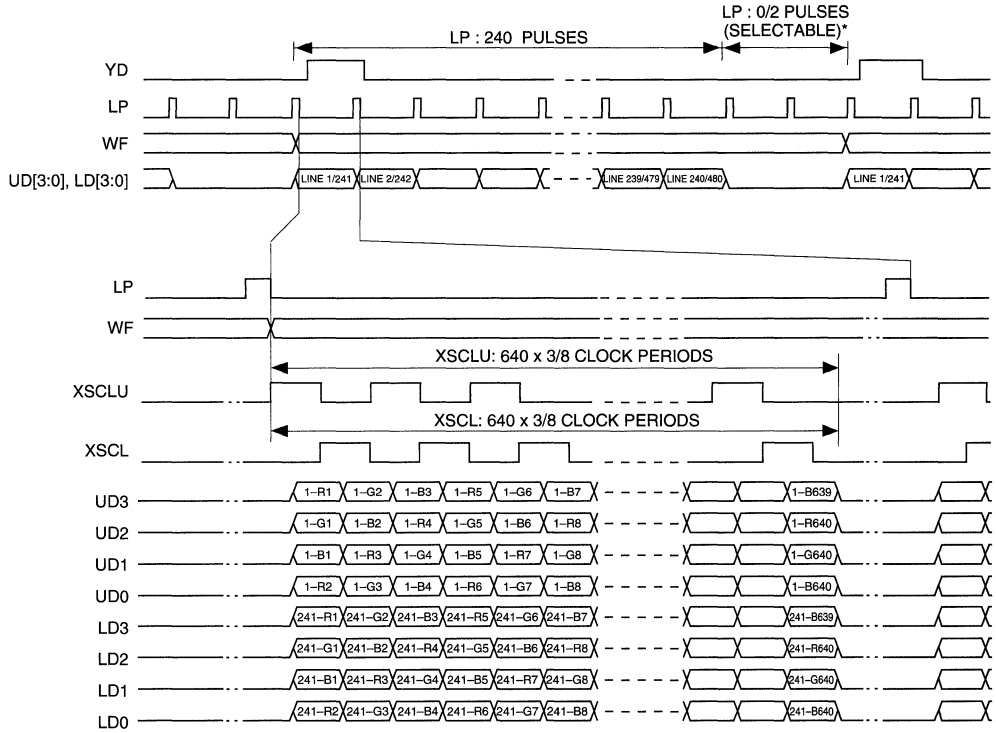
8-bit Dual Color Panel (One Shift Clock)



* Diagram drawn with 2 LP vertical blank period
Example timing for 640 × 480 panel

■ Color Passive STN LCD Panel Interface

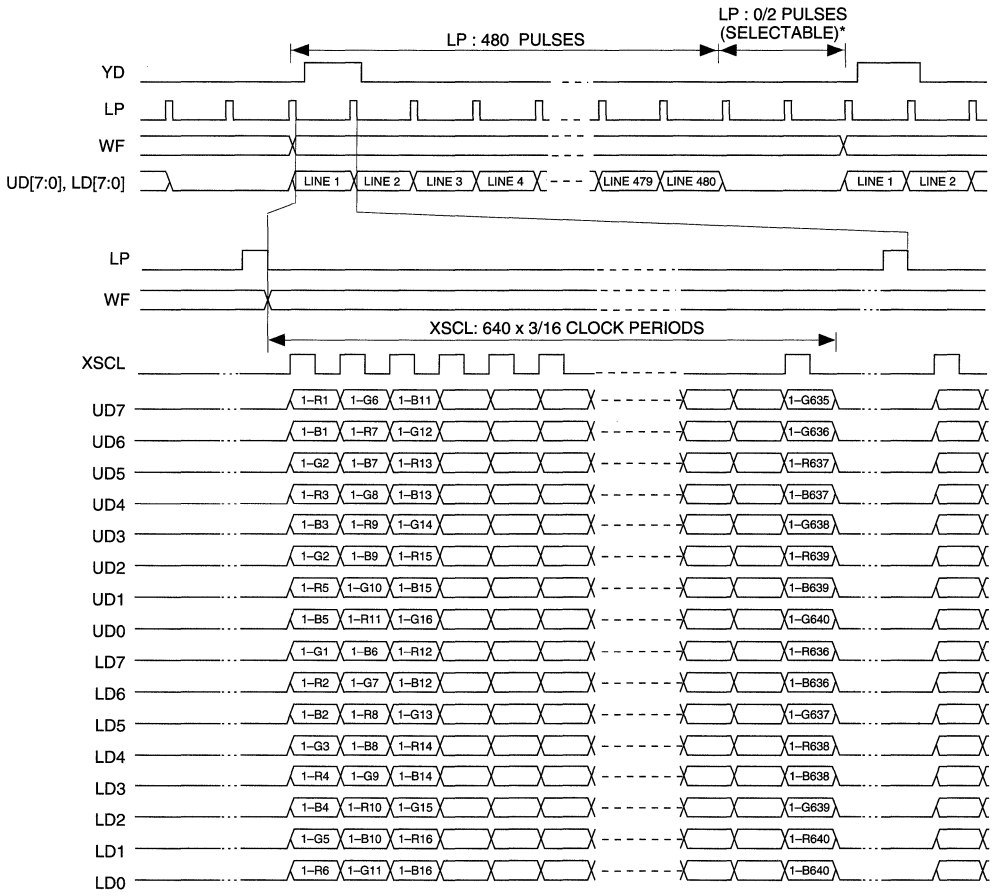
8-bit Dual Color Panel (Two Shift Clocks)



* Diagram drawn with 2 LP vertical blank period
Example timing for 640 × 480 panel

■ Color Passive STN LCD Panel Interface

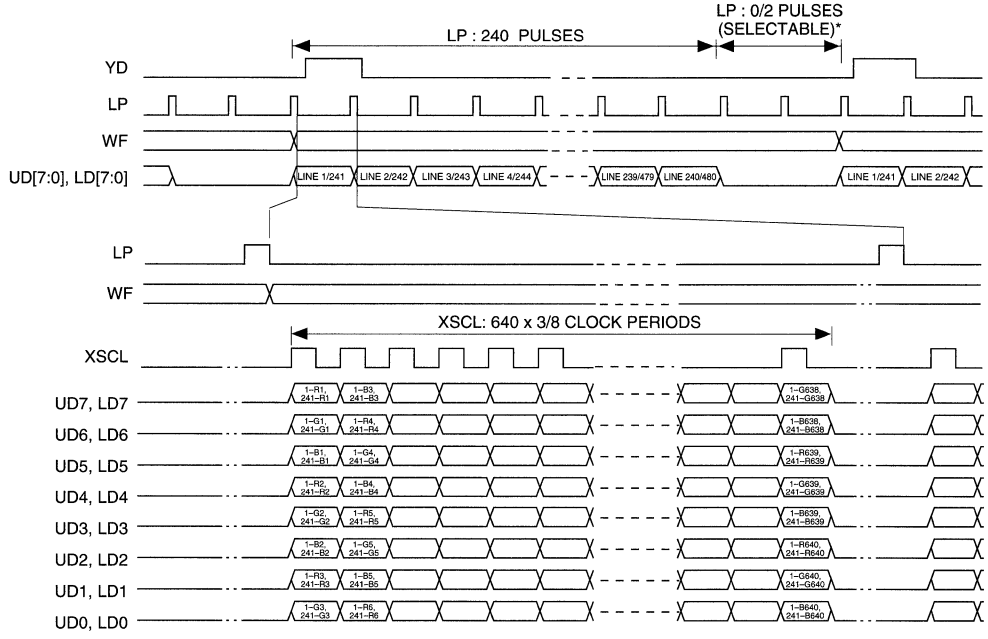
16-bit Single Color Panel



* Diagram drawn with 2 LP vertical blank period
Example timing for640 × 480 panel

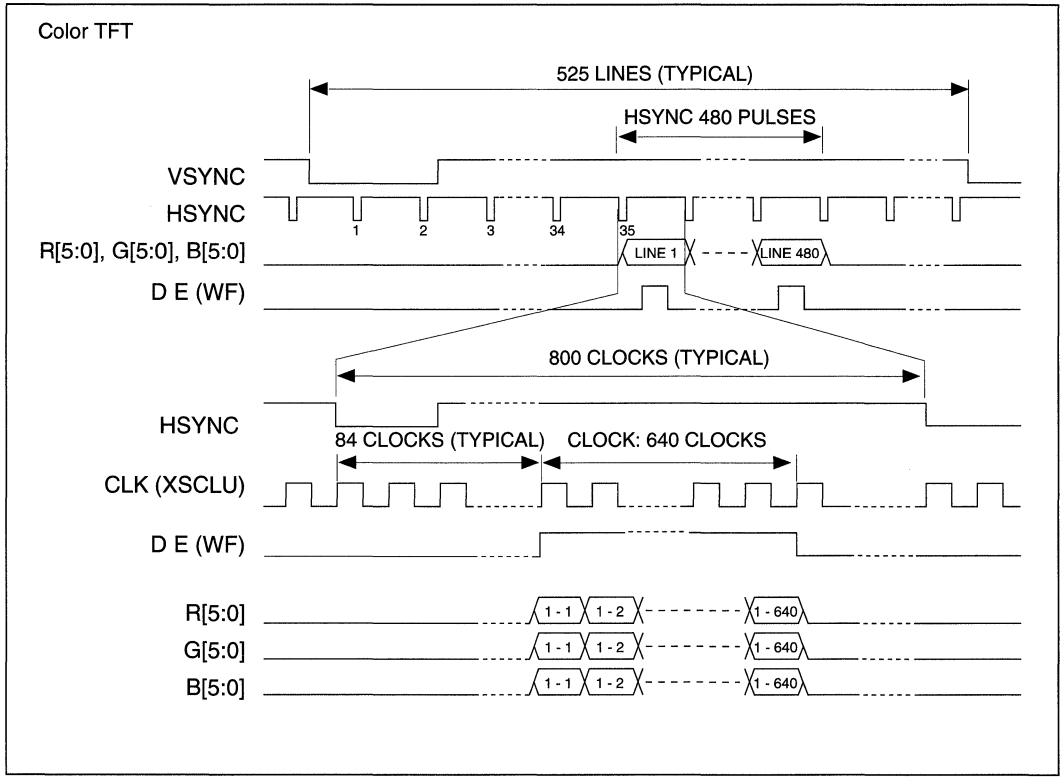
■ Color Passive STN LCD Panel Interface

16-bit Dual Color Panel

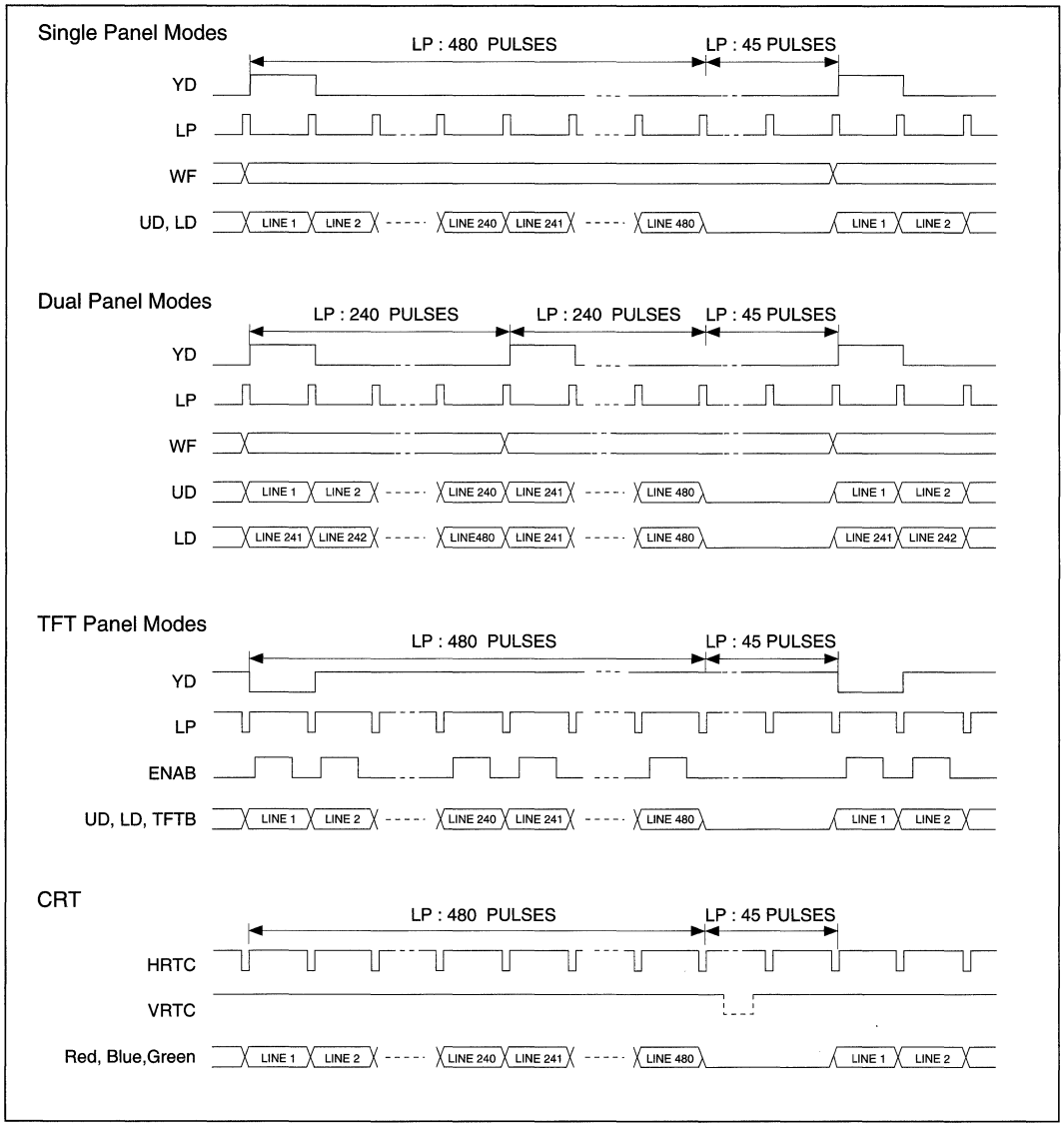


* Diagram drawn with 2 LP vertical blank period
Example timing for 640 × 480 panel

■ Active Matrix LCD Panel Interface



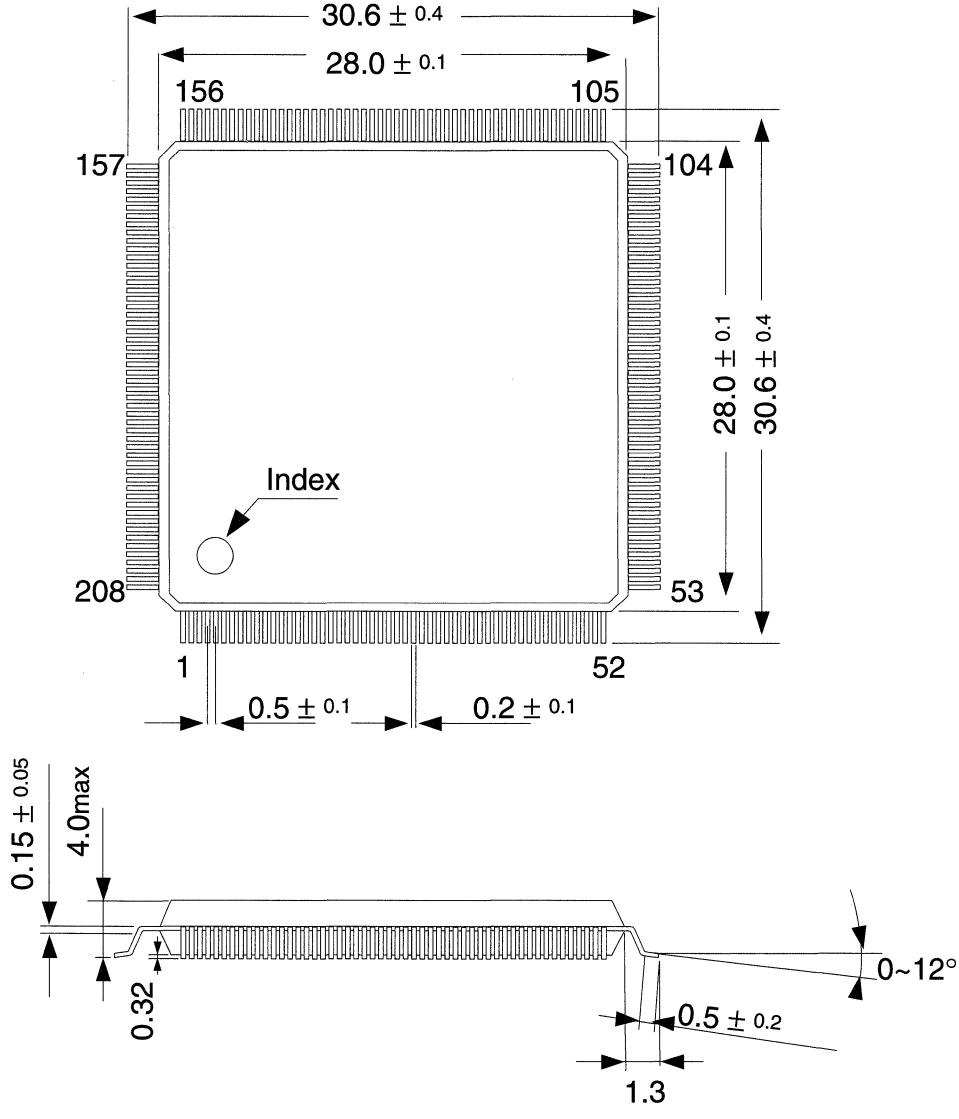
■ Simultaneous Display Interface



■ PACKAGE DIMENSIONS

QFP8-208 S1s

Unit: mm



1996 DATABOOK

GRAPHICS PRODUCTS

III. GRAPHIC LCD CONTROLLERS

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■ GRAPHIC LCD CONTROLLERS

Part Number		SED1330	SED1335	SED1336	SED1341	SED1345	SED1351	SED1352
Discontinued?		No	No	No	No	No	No	No
Replacement		—	—	—	—	—	—	—
Internal CGROM		160 chars (5x7)	160 chars (5x7)	160 chars (5x7)				
CPU Interface (Bits)	68xx	8	8	8			8, 16	8, 16
	80xx	8	8	8			8, 16	8, 16
	MPU				4	4	8, 16	8, 16
	ISA							8, 16
	Digital RGB				1(R or G or B)	4 (R,G,B,I)		
Display Size		up to 640x256 dots at a duty of 1/256	up to 640x256 dots at a duty of 1/256	LCD: 640x200, TV: 256x200	adjusted by H/W 640x200 640x350 640x400 640x480 720x350 720x480	adjusted by S/W 640x200 640x350 640x400 640x480	max. duty of 1/1024 up to 1024x1024	1/1024 single mode, 1/2048 dual mode, 640x480, 320x200
Frame Buffer Support		64KB SRAM	64KB SRAM	64KB SRAM	40KB SRAM	40KB SRAM	64KB SRAM	128KB SRAM
Frame Buffer Data Bus Width (bits)		8	8	8	8	8	16	8/16
fclk,max (MHz)		10	10	10	11.2		12.5	22
fosc (MHz)		10	10	10	34	30	14.29	25
Supply voltage	5V	x	x	x	x	x	FOA	x
	3V		x	x		x	FLB	x
Gray shade levels	2	x	x	x	x			
	4						x	x
	8					x		
	16							x
Display Data Bus (bits)	4	x	x	x	x	x	x	x
	8				x	x	x	x

(continued)

■ GRAPHIC LCD CONTROLLERS (continued)

Part Number		SED1330	SED1335	SED1336	SED1341	SED1345	SED1351	SED1352
Control Register		3 layers, smooth scrolling, inverse video, text and graphic display	3 layers, smooth scrolling, inverse video, text and graphic display	LCD/TV support, 3 layers, smooth scrolling, inverse video, text and graphic display	Set by digital switches or MPU for panel size, panel timing, clock select	Set by ROM or MPU for panel size, panel timing, clock select	2 layers, data OR function, smooth scrolling, overlay, inverse video	
Panel Type	Passive	x	x	x	x	x	x	x
	TV			ntsc/pal				
Package	QFP	FBA (QFP5-60pin), FBB (QFP6-60pin)	F0A (QFP5-60pin), F0B (QFP6-60pin)	F0A (QFP6-60pin)	F0E (QFP5-80pin)	F0A (QFP5-80pin)	F0A (QFP5-100pin), FLB (QFP15-100pin)	F0A (QFP5-100pin)
Page Number		125	139	153	165	185	197	215

Notes: 1. Some packages of certain parts labeled with # are still under development.

DISCONTINUED

SED1330

CMOS GRAPHIC LCD CONTROLLER

This part is replaced by SED1335. Some pin differences between SED1330 and SED1335 exist. Please check SED1335 data sheet. S-MOS Systems, Inc., will continue to support existing designs which use SED1330.

■ DESCRIPTION

The SED1330 is a CMOS low-power dot matrix liquid crystal graphic display controller. The device stores in external RAM display data sent by an 8-bit microcomputer, and generates all the signals required by the LCD drivers. The LSI incorporates an internal character generator ROM which supports user-defined characters (also an external CGROM can be supported).

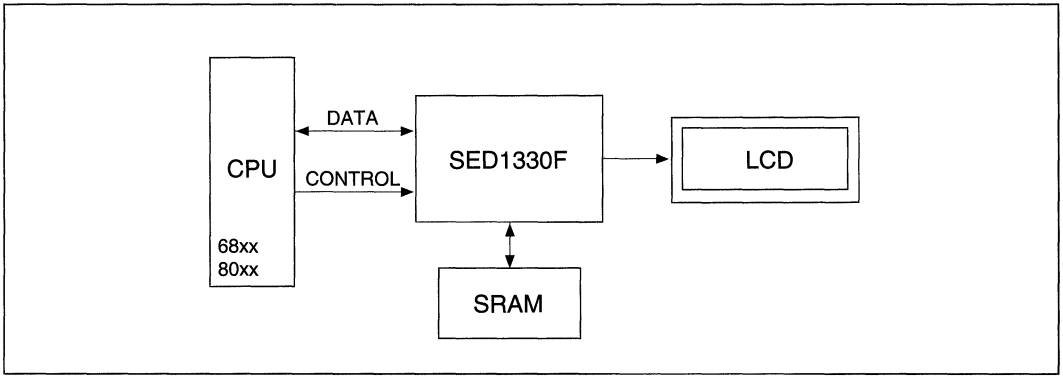
The SED1330 can be interfaced to high-speed microprocessors such as the Intel family or Motorola family. The controller supports a set of rich commands that will allow the user to create a layered display of characters and graphics.

Also, the controller functions as a pipeline buffer between the MPU and display memory so that low-cost, medium-speed SRAM can be used.

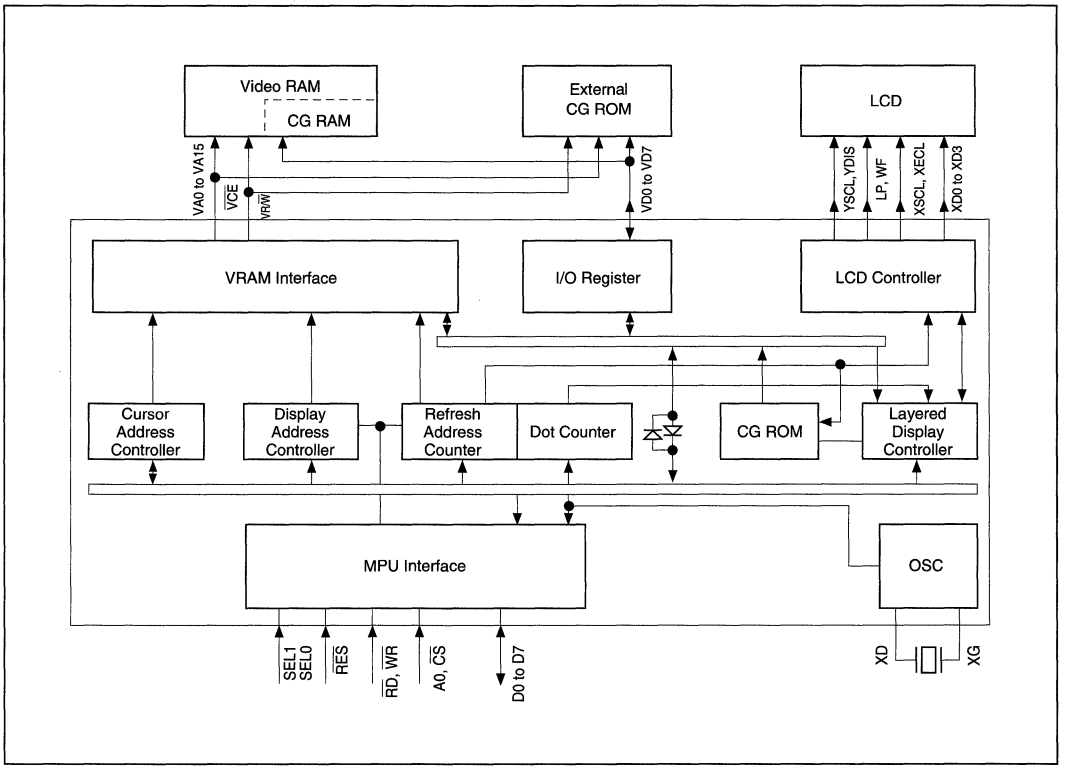
■ FEATURES

- CMOS low-power graphic and character display controller
- Selectable MPU interface is compatible with both the Intel family and the Motorola family
- Smooth scrolling support:
  Horizontal and vertical scroll
  Scrolling of selected areas of the display
- Multimode display:
  2 layers of overlapping character and graphics
  3 layers of overlapping graphics
- Selectable display synthesis:
  Inverse video
  Flashing display, cursor on/off/blink
  Under and bar cursor, block cursor
  Simple animation
- Programmable cursor
- Internal character generator ROM
- Supports external character generator ROM:
  8 × 8 or 8 × 16 pixel characters
  Allows mixing of ROM and RAM character sets
- Supports 64K bytes of memory:
  2 of 32K × 8 100ns SRAM
  or 8 of 8K × 8 100ns SRAM
- Display duty ..... 1/2 to 1/256
- Low power dissipation ..... 5mA (typical)
  0.05μA (typical), standby
- Logic power supply ..... 4.5 to 5.5V
- Package ..... Plastic QFP5-60 pin (FBA)
  Plastic QFP6-60 pin (FBB)

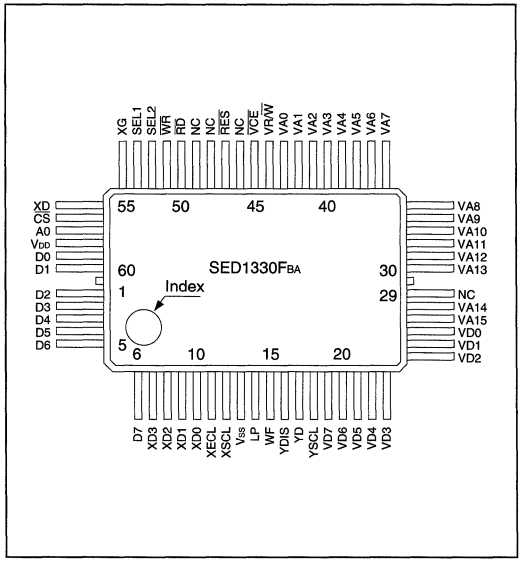
■ SYSTEM BLOCK DIAGRAM

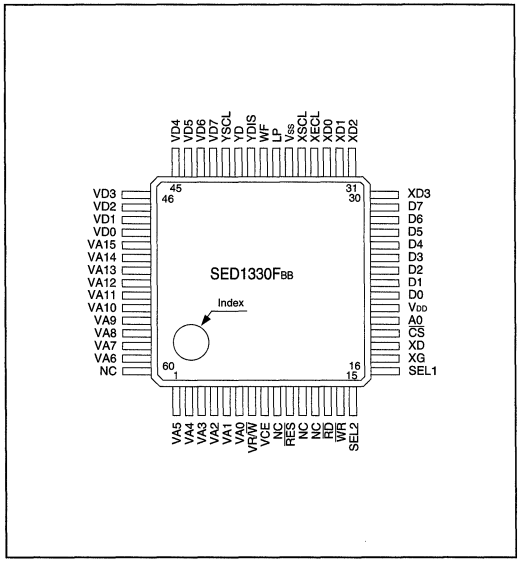


■ BLOCK DIAGRAM



■ PINOUT





■ PIN DESCRIPTIONS

Pin Name	Pin No.		I/O	Functions
	SED1330F$_{BA}$	SED1330F$_{BB}$		
XG	54	17	I	Oscillator terminal
XD	55	18	O	Oscillator terminal
V_{DD}	58	21	+5V	Power supply
V_{SS}	13	36	GND (0V)	Power supply
SEL1, 2	53 • 52	16 • 15	I	MPU interface format selection
D0 to D7	59 to 60 1 to 6	22 to 29	I/O	Data bus
A0	57	20	I	Data type selection
$\overline{RD}$	50	13	I	80 series Read strobe signal 68 series "E" clock
$\overline{WR}$	51	14	I	80 series Write strobe signal 68 series R/$\overline{W}$ signal
$\overline{CS}$	56	19	I	Chip select
$\overline{RES}$	47	10	I	Reset
VA0 to VA15	43 to 30 28 to 27	6 to 1 59 to 50	O	VRAM address bus
VD0 to VD7	26 to 19	49 to 42	I/O	VRAM data bus
VR/$\overline{W}$	44	7	O	VRAM R/$\overline{W}$ signal
$\overline{VCE}$	45	8	O	Memory control signal
XD0 to XD3	10 to 7	33 to 30	O	Dot data output bus to X driver
XSCL	12	35	O	Dot data shift clock for X driver
XECL	11	34	O	Chip enable shift clock for Y driver
LP	14	37	O	Dot data latch pulse
WF	15	38	O	Frame signal
YSCL	18	41	O	Scan data shift clock for Y driver
YD	17	40	O	Scan data output
YDIS	16	39	O	Power down signal when display OFF

NC: No Connection

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.3 to 7.0	V
Input voltage	V_I	–0.5 to V_{DD}+0.5	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–60 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

● DC ELECTRICAL CHARACTERISTICS

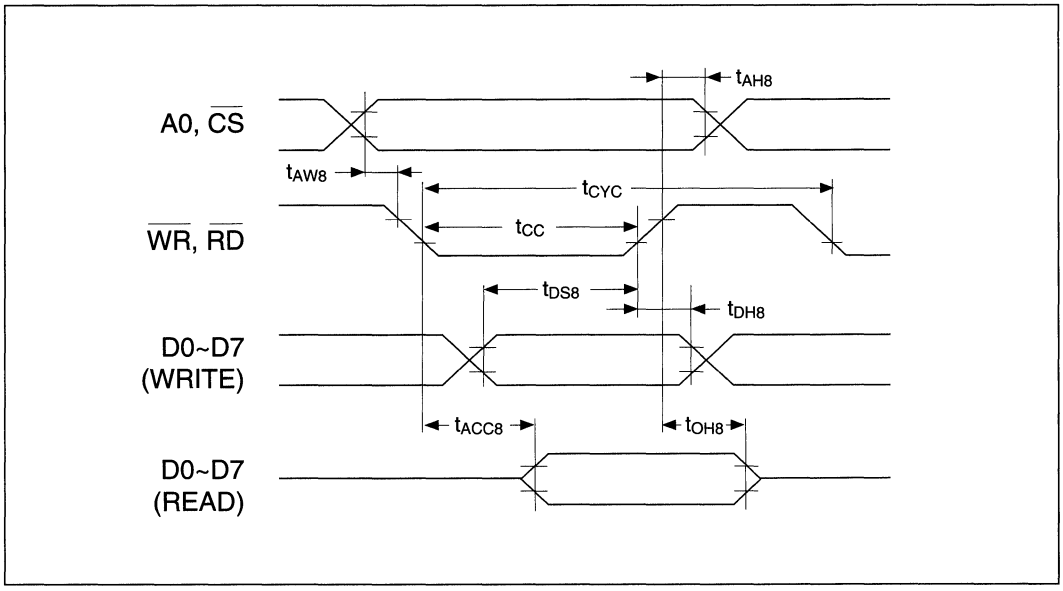
(V_{DD} = 5V±10%, V_{SS} = 0V, T_a = –20 to 75°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Operating voltage		V_{DD}		4.5	5.0	5.5	V
Register data retention voltage		V_{OH}		2.0	—	6.0	V
TTL	High level input voltage	V_{IHT}	D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$,	2.2	—	V_{DD}+0.3	V
	Low level input voltage	V_{ILT}	VD0 to VD7, I_{OH}= –5.0mA,	–0.3	—	0.8	V
	High level output voltage	V_{OHT}	I_{OL}=5.0mA, VR/$\overline{W}$, $\overline{VCE}$,	2.4	—	—	V
	Low level output voltage	V_{OLT}	$\overline{REF}$	—	—	0.4	V
CMOS	High level input voltage	V_{IHC}	I_{OH}=1.6mA, I_{OL}= –1.6mA,	0.8V_{DD}	—	—	V
	Low level input voltage	V_{ILC}	SEL1, 2, SYNC, YD, XD0 to	—	—	0.2V_{DD}	V
	High level output voltage	V_{OHC}	XD3, XSCL, XECL, LP, FR,	V_{DD}–0.4	—	—	V
	Low level output voltage	V_{OLC}	YSCL, YDIS, OSC1, OSC2	—	—	0.4	V
SCHMITT	Positive trigger threshold voltage	V_{T+}	$\overline{RES}$ *	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
	Negative trigger threshold voltage	V_{T-}		0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V
Input leakage current		I_{LI}	V_I=V_{DD} or V_{SS}	—	0.05	2.0	µA
Output leakage current		I_{LO}		—	0.10	5.0	µA
Average operating current		I_{DDA}	f_{OSC}=10MHz, No load (No external V-RAM) $\overline{XG}$=$\overline{CS}$=V_{DD}	—	8	12	mA
Standby current		I_{DDS}		—	0.05	20	µA
Oscillation frequency		f_{OSC}	AT X'tal	1.0	—	10.0	MHz
External clock frequency		f_{CLK}	XG, XD	—	—	10.0	MHz
Feed back resistance		R_f		0.5	1.0	5.0	MΩ

* $\overline{RES}$ input pulse should be longer than 1.0ms.

VL5 should be OFF when $\overline{RES}$ is "L".

- **AC CHARACTERISTICS**
  - **System Bus READ/WRITE Timing I (8080)**

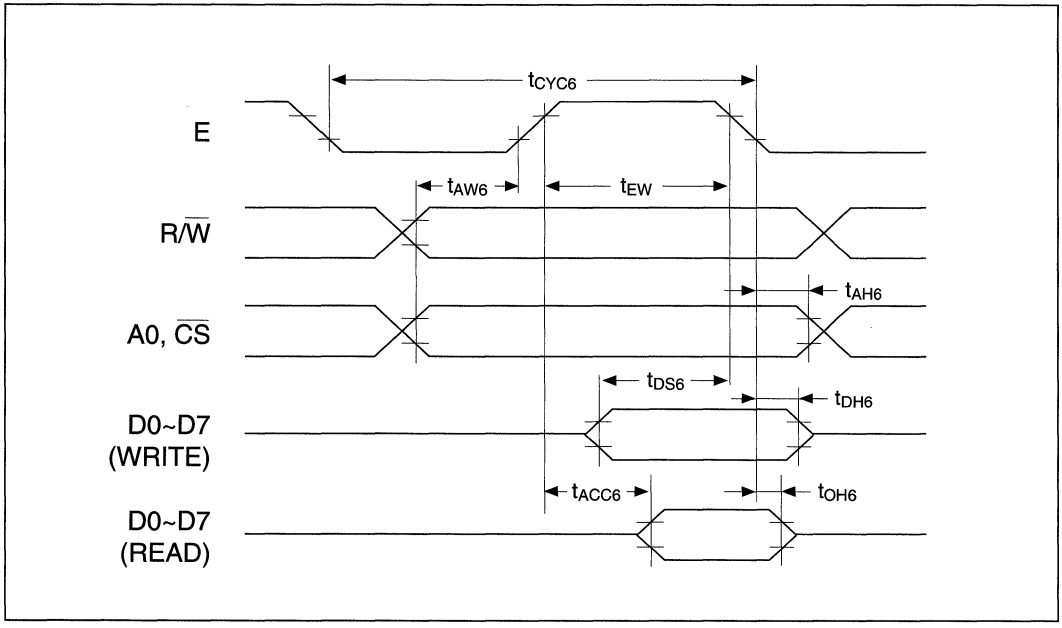


Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
A0, CS	Address hold time	tAH8	10	—	ns	CL = 100 pF + 1TTL
	Address setup time	tAW8	30	—	ns	
WR, RD	System cycle time	tCYC	*1	—	ns	
	Control pulse width	tCC	220	—	ns	
D0 to D7	Data setup time	tDS8	120	—	ns	
	Data hold time	tDH8	10	—	ns	
	RD access time	tACC8	—	120	ns	
	Output disable time	tOH8	10	50	ns	

*1. $t_{CYC} = 2t_c + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$ ..... Memory control/movement control commands.

$= 4t_C + t_{CC} + 30$ ..... All other commands.

○ **System Bus READ/WRITE Timing II (6800)**



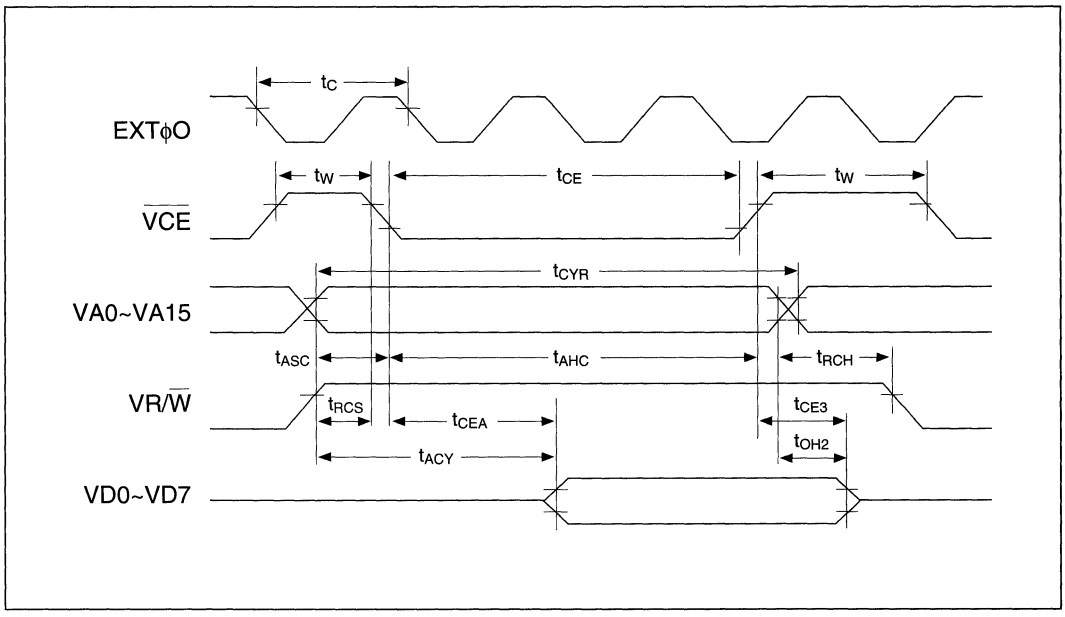
Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
A0, CS, R/W	System cycle time	tCYC6*1	*2	—	ns	CL = 100 pF + 1 TTL
	Address setup time	tAW6	30	—	ns	
	Address hold time	tAH6	10	—	ns	
D0 to D7	Data setup time	tDS6	120	—	ns	
	Data hold time	tDH6	10	—	ns	
	Output disable time	tOH6	10	50	ns	
	Access time	tACC6	—	120	ns	
E	Enable pulse width	tEW	220	—	ns	

*1. t_{CYC6} means a cycle of ($\overline{CS}$.E) not E alone.

*2. $t_{CYC6} = 2t_c + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$ ..... Memory control/movement control commands.

$= 4t_c + t_{EW} + 30$ ..... All other commands.

○ **Display Memory READ Timing**



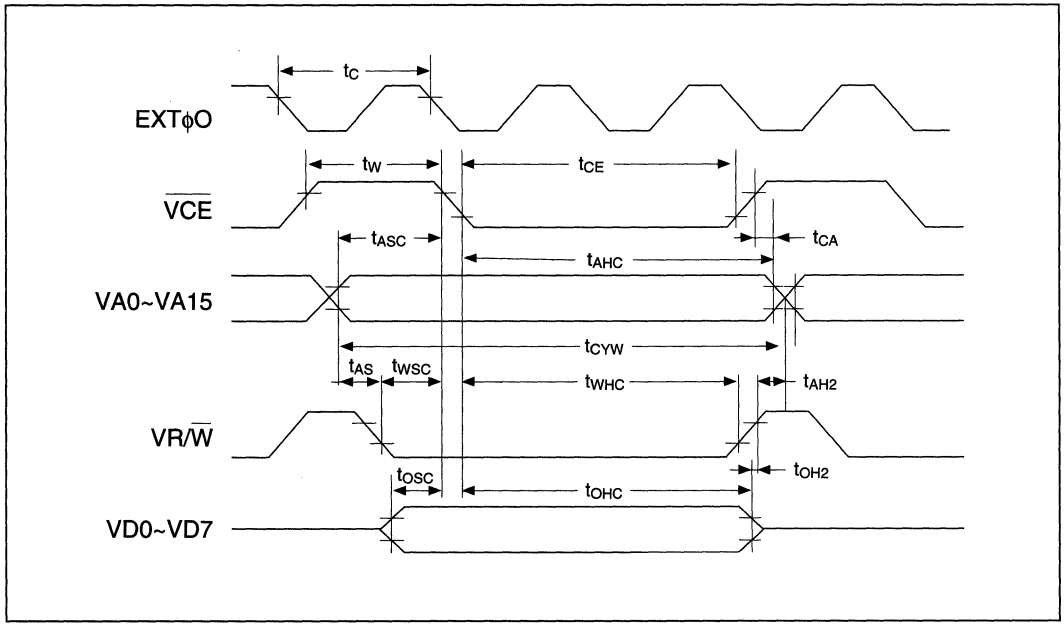
Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
EXT ϕ0	Clock cycle	tC	100	—	ns	CL = 100 pF + 1TTL
VCE	VCE high-level pulse width	tW	tC – 40	—	ns	
	VCE low-level pulse width	tCE	2tC – 40	—	ns	
VA0 to VA15	Read cycle time	tCYR	*1	—	ns	
	VCE address setup time (fall)	tASC	tC – 45	—	ns	
	VCE address hold time (fall)	tAHC	2tC – 40	—	ns	
VR/W	VCE read cycle setup time (fall)	tRCS	tC – 45	—	ns	
	VCE read cycle hold time (fall)	tRCH	tc/2 – 35	—	ns	
VD0 to VD7	Address access time	tACV	—	*2	ns	
	VCE access time	tCEA	—	*3	ns	
	Output data hold time	tOH2	0	—	ns	
	VCE data off time	tCE3	0	—	ns	

*1. tCYR = 3tC

*2. tACV = 3tC – 120

*3. tCEA = 2tC – 120

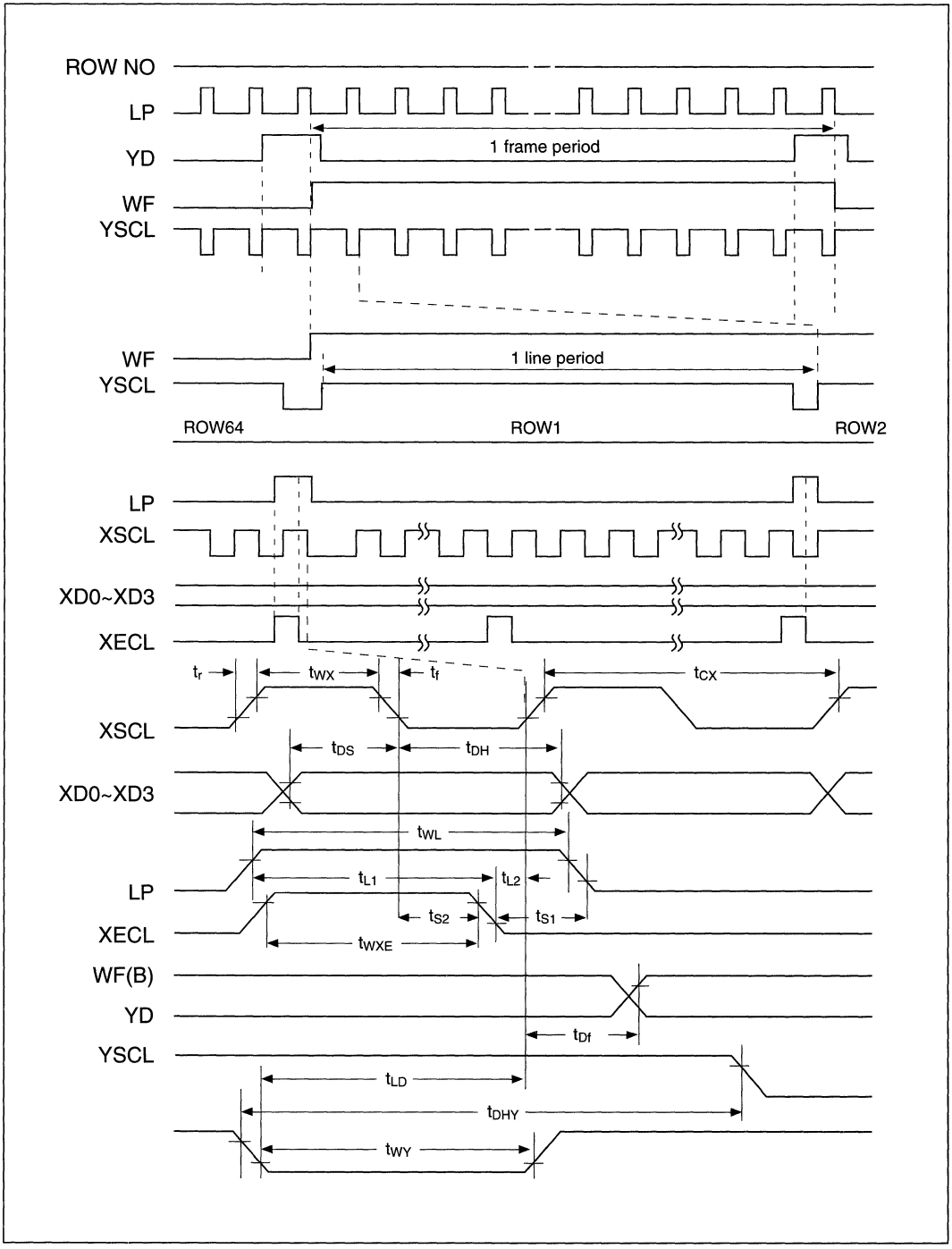
○ **Display Memory WRITE Timing**



Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
EXT φ0	Clock cycle	tC	100	—	ns	CL = 100 pF + 1TTL
VCE	VCE HIGH-level pulse width	tW	tC – 40	—	ns	
	VCE LOW-level pulse width	tCE	2tC – 40	—	ns	
VA0 to VA15	Write cycle time	tCYW	3tC	—	ns	
	VCE address hold time (fall)	tAHC	2tC – 40	—	ns	
	VCE address setup time (fall)	tASC	tC – 55	—	ns	
	VCE address hold time (rise)	tCA	5	—	ns	
	VR/W address setup time (fall)	tAS	0	—	ns	
	VR/W address hold time (rise)	tAH2	15	—	ns	
VR/W	VCE write setup time (fall)	tWSC	tC – 55	—	ns	
	VCE write hold time (fall)	tWHC	2tC – 40	—	ns	
VD0 to VD7	VCE data input setup time (fall)	tDSC	tWSC – 10	—	ns	
	VCE data input hold time (fall)	tDHC	2tC – 30	—	ns	
	VR/W data hold time (rise)	tDH2	10*	50	ns	

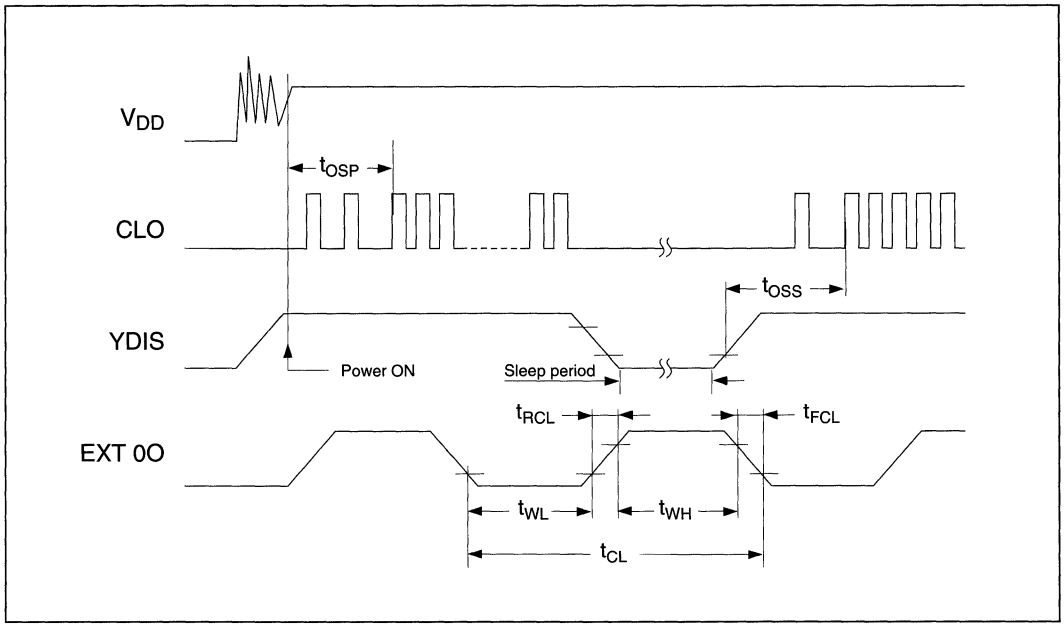
* Lines VD0 to VD7 are latched.

○ **LCD Control Timing**



Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
EXT ϕ0	Clock cycle	t_C	100	—	ns	V_{DD} = 5.0V ± 10% CL = 150F
	Rising time	t_r	—	35	ns	
	Falling time	t_f	—	35	ns	
XSCL	Shift clock cycle time	t_{CX}	4t_C	—	ns	
	XSCL clock pulse width	t_{WX}	t_{CX2} – 80	—	ns	
XD0 to XD3	X-data hold time	t_{DH}	t_{CX2} – 100	—	ns	
	X-data setup time	t_{DS}	t_{CX2} – 100	—	ns	
LP	Latch data setup time	t_{LS}	t_{CX2} – 100	—	ns	
	LP signal pulse width	t_{WL}	t_{CX4} – 80	—	ns	
XECL	XECL setup time	t_{L1}	t_{CX3} – 100	—	ns	
	XECL data hold time	t_{L2}	t_C – 30	—	ns	
	Enable setup time	t_{S1}	t_C – 30	—	ns	
	Enable delay time	t_{S1}	t_C – 30	—	ns	
	XECL clock pulse width	t_{WXE}	t_{CX3} – 80	—	ns	
WF	Time allowance of WF delay	t_{DF}	—	100	ns	
YSCL	LP delay time against YSCL	t_{LD}	t_{CX4} – 100	—	ns	
	YSCL clock pulse width	t_{WY}	t_{CX4} – 80	—	ns	
YD	Y-data hold time	t_{DHY}	t_{CX6} – 100	—	ns	

○ **Oscillator Timing**

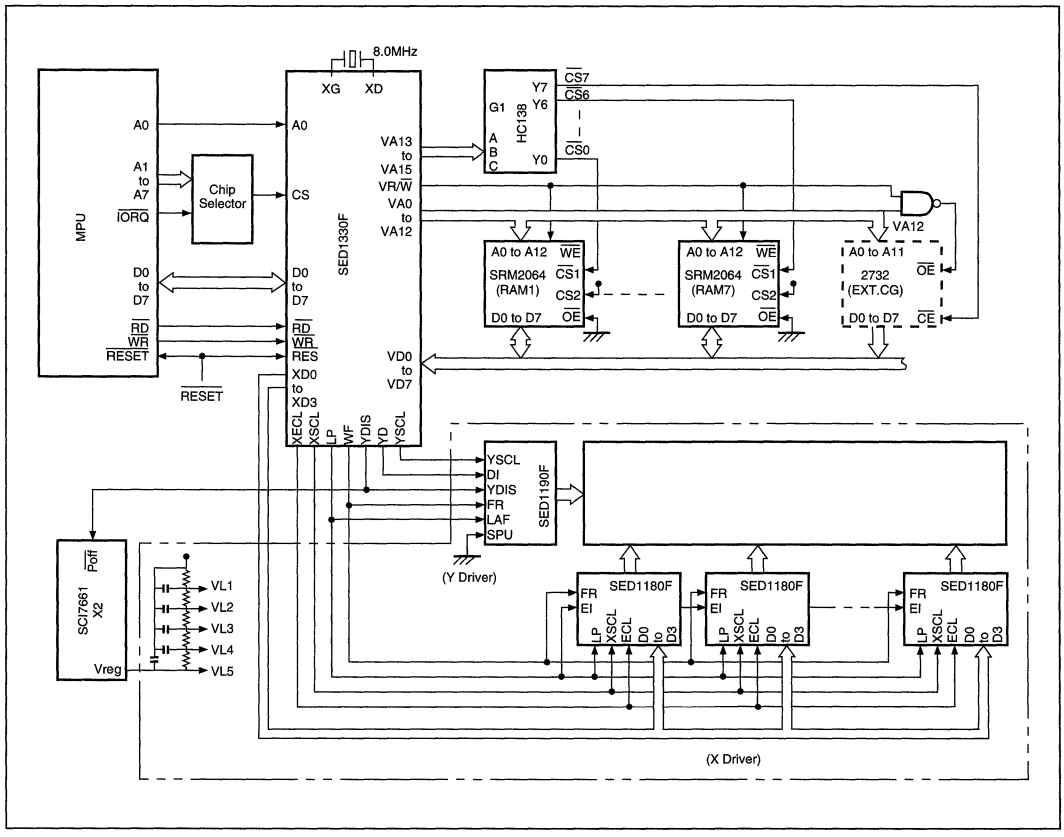


Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
CLO	Time to stable CLO output after power-ON	tOSP	—	3	ms	$\overline{RES}$ = H 20 pF
	Time to stable CLO after sleep OFF	tOSS	—	1	ms	
EXT ϕ0	External clock rise time	tRCL	—	15	ns	
	External clock fall time	tFCL	—	15	ns	
	External clock high-pulse width	tWH	*1	*2	ns	
	External clock low-pulse width	tWL	*1	*2	ns	
	External clock cycle	tCL	100	—	ns	

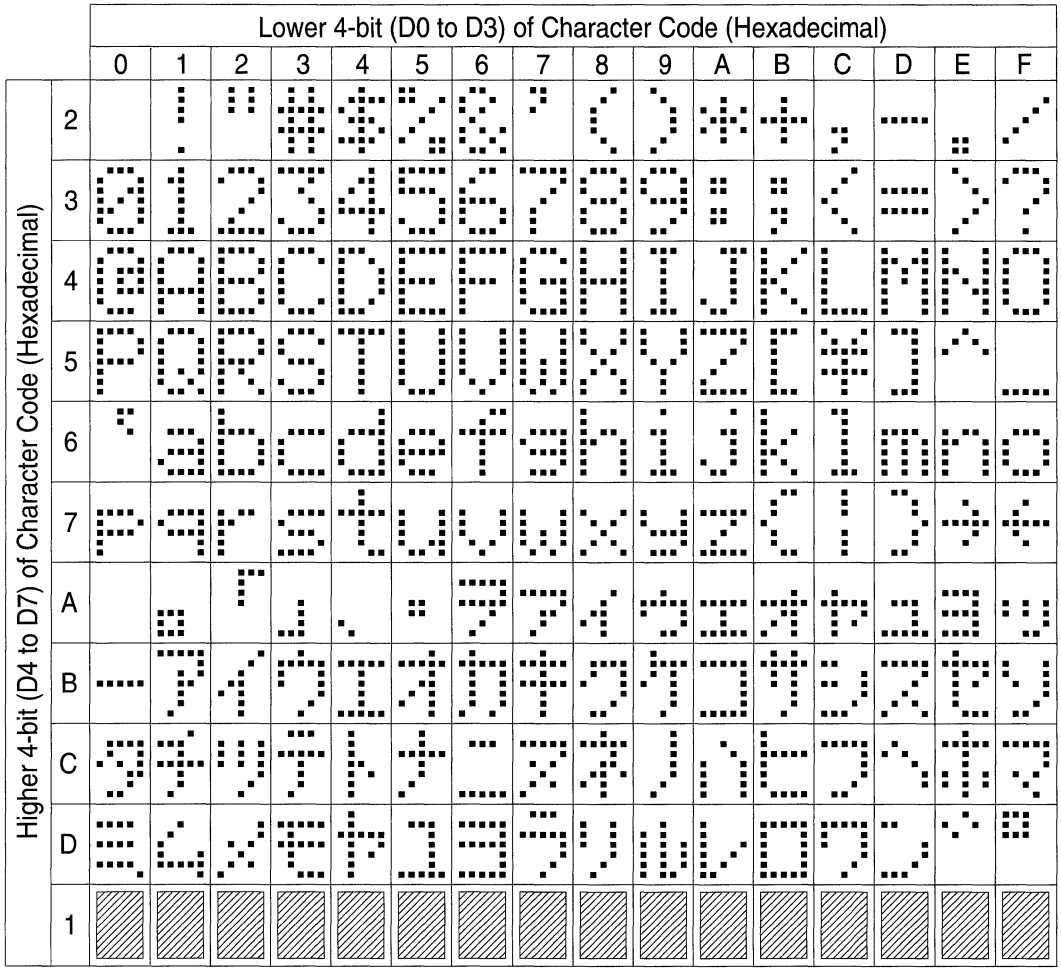
*1. (tc – tRCL – tFCL) × 475/1000 < tWH, tWL

*2. (tc – tRCL – tFCL) × 525/1000 > tWH, tWL

■ EXAMPLE OF APPLICATION



■ CHARACTER CODE TABLE (BUILT-IN CHARACTER GENERATOR)



Note: ▨ means all dots of 6 × 8 matrix are on.

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CMOS GRAPHIC LCD CONTROLLER

- **For Medium-Scale LCD**
- **Low Operating Voltage 2.7 to 5.0V**
- **On-Chip Character Generator ROM**

■ DESCRIPTION

The SED1335 is a CMOS low-power dot matrix liquid crystal graphic display controller. The device stores in external RAM display data sent by an 8-bit microcomputer, and generates all the signals required by the LCD drivers. The LSI incorporates an internal character generator ROM which supports user-defined characters (also an external CGROM can be supported).

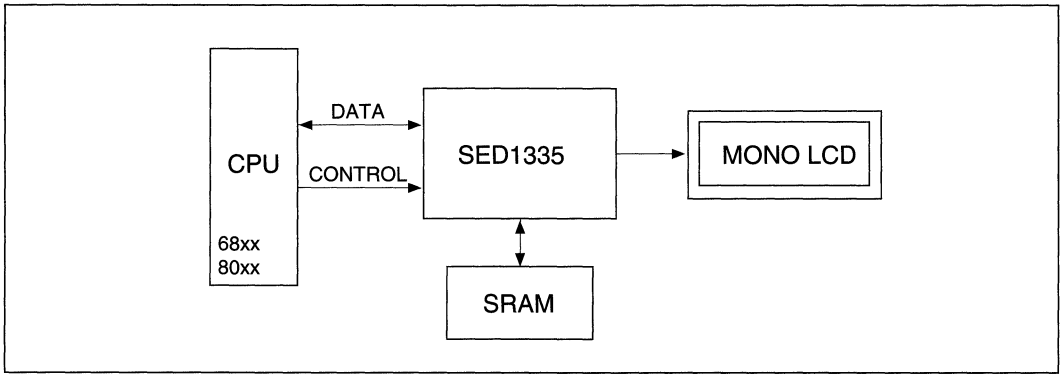
The SED1335 can be interfaced to high-speed microprocessors such as the Intel family or Motorola family. The controller supports a set of rich commands that will allow the user to create a layered display of characters and graphics.

Also, the controller functions as a pipeline buffer between the MPU and display memory so that low-cost, medium-speed SRAM can be used.

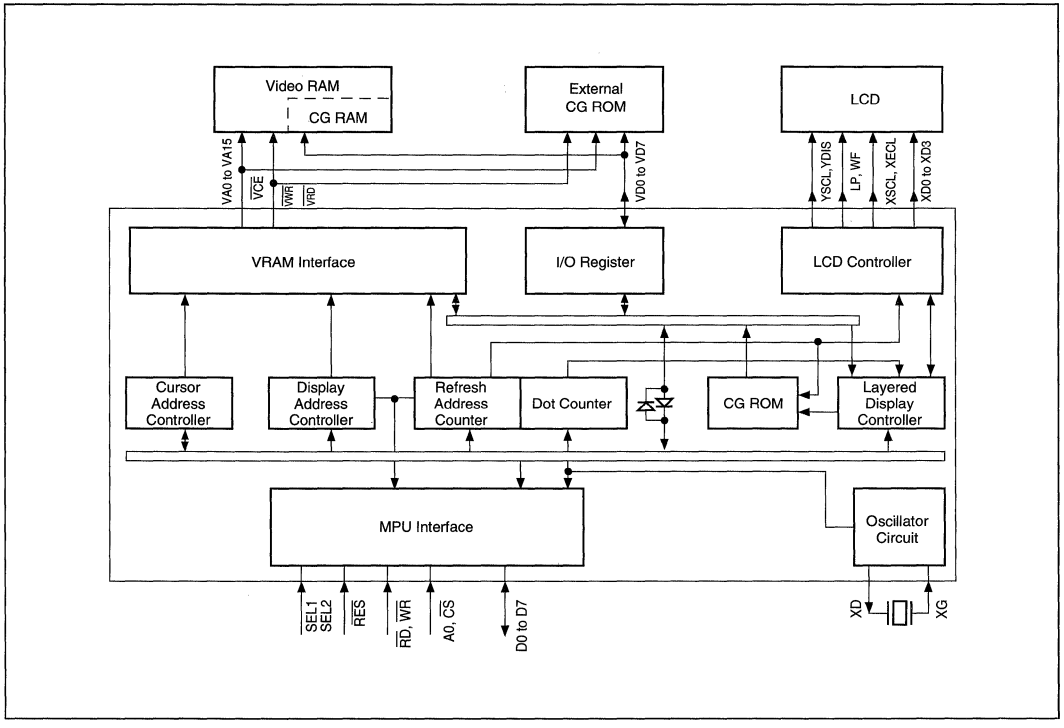
■ FEATURES

- CMOS low-power graphic and character display controller
- Selectable MPU interface is compatible with both the Intel family and the Motorola family
- Smooth scrolling support:
  Horizontal and vertical scroll
  Scrolling of selected areas of the display
- Multimode display:
  2 layers of overlapping characters and graphics
  3 layers of overlapping graphics
- Selectable display synthesis:
  Inverse video
  Flashing display, cursor on/off/blink
  Under and bar cursor, block cursor
  Simple animation
- Programmable cursor
- Internal character generator ROM
- Supports external character generator ROM:
  8 × 8 or 8 × 16 pixel characters
  Allowing mixing of ROM and RAM character sets
- Supports 64K bytes of memory:
  4K bytes of user-definable characters
  60K bytes of display memory
  in 2 of 32K × 8 100ns SRAM
  or in 8 of 8K × 8 100ns SRAM
- Display duty ..... 1/2 to 1/256
- Low power dissipation
  5mA (typical)
  0.05μA (typical), standby
- Logic power supply ..... 2.7 to 5.5V
- Package: ..... Plastic QFP5-60 pin (FOA)
  Plastic QFP6-60 pin (FOB)

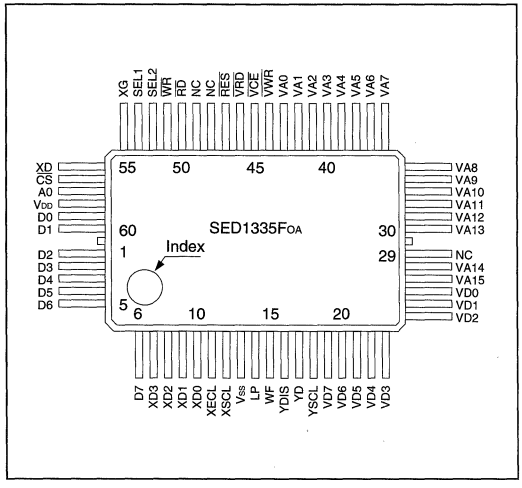
■ SYSTEM BLOCK DIAGRAM

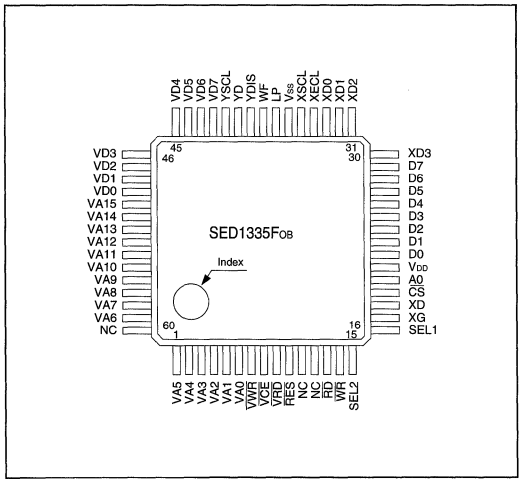


■ BLOCK DIAGRAM



■ PINOUT





■ PIN DESCRIPTION

Pin Name	Pin No.		I/O	Functions
	SED1335F0A	SED1335F0B		
XG	54	17	I	Oscillator terminal
XD	55	18	O	Oscillator terminal
V_{DD}	58	21	+5V	Power supply
V_{SS}	13	36	GND(0V)	Power supply
SEL1,2	53 • 52	16 • 15	I	MPU interface format selection
D0 to D7	59 to 60, 1 to 6	22 to 29	I/O	Data bus
A0	57	20	I	Data type selection
$\overline{RD}$	50	13	I	80 series Read strobe signal 68 series "E" clock
$\overline{WR}$	51	14	I	80 series Write strobe signal 68 series R/W signal
$\overline{CS}$	56	19	I	Chip select
$\overline{RES}$	47	10	I	Reset
VA15 to VA0	27 • 28, 30 to 43	1 to 6, 50 to 59	O	VRAM address bus
VD7 to VD0	19 to 26	42 to 49	I/O	VRAM data bus
$\overline{VWR}$	44	7	O	VRAM write signal
$\overline{VRD}$	46	9	O	VRAM read signal
$\overline{VCE}$	45	8	O	VRAM chip enable
XD3 to XD0	7 to 10	30 to 33	O	Dot data output bus to X driver
XSCL	12	35	O	Dot data shift clock for X driver
XECL	11	34	O	Chip enable shift clock for X driver
LP	14	37	O	Dot data latch pulse
WF	15	38	O	Frame signal
YSCL	18	41	O	Scan data shift clock for Y driver
YD	17	40	O	Scan data output
YDIS	16	39	O	Power down signal when display is OFF

NC: No Connection

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	−20 to 75	°C
Storage temperature	T_{stg}	−60 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

● DC Electrical Characteristics (1)

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_a = –20 to 75°C)

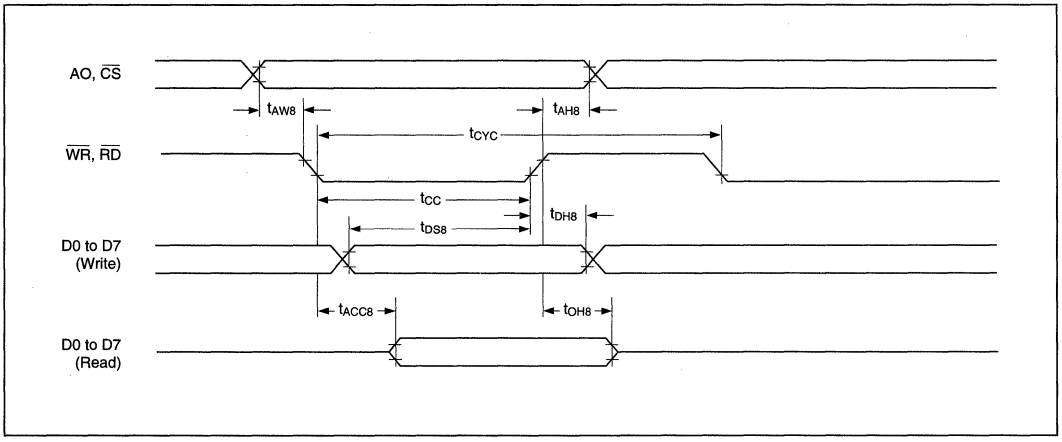
Parameter		Symbol	Condition	Min	Typ	Max	Unit	Terminal
Operating voltage		V_{DD}		4.5	5.0	5.5	V	V_{DD}
Register data retention voltage		V_{OH}		2.0	—	6.0	V	
TTL	High level input voltage	V_{IHT}		0.5xV_{DD}	—	V_{DD}	V	D0 to D7, A0, CS, RD, WR, VD0 to VD7, VA0 to VA15, VCE, VRD, VWR
	Low level input voltage	V_{ILT}		V_{SS}	—	0.2xV_{DD}	V	
	High level output voltage	V_{OHT}	I_{OH} = –5.0mA	2.4	—	—	V	
	Low level output voltage	V_{OLT}	I_{OL} = 5.0mA	—	—	V_{SS}+0.4	V	
CMOS	High level input voltage	V_{IHC}		0.8xV_{DD}	—	V_{DD}	V	SEL1, SEL2, YD, XD0 to XD3, XSCL, YDIS, LP, WF, CL0, XECL, YSCL
	Low level input voltage	V_{ILC}		V_{SS}	—	0.2xV_{DD}	V	
	High level output voltage	V_{OHC}	I_{OH} = –2.0mA	V_{DD}–0.4	—	—	V	
	Low level output voltage	V_{OLC}	I_{OL} = 2.0mA	—	—	V_{SS}+0.4	V	
SCHMITT	Positive trigger threshold voltage	V_{T+}		0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V	$\overline{RES}$
	Negative trigger threshold voltage	V_{T-}		0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V	
Input leakage current		I_{LI}	V_{IN} = V_{DD}/V_{SS}	—	0.05	2.0	µA	
Output leakage current		I_{LO}		—	0.10	5.0	µA	
Average operating current		I_{opr}	f_{osc} = 10MHz, No-load 256 × 200 dot	—	11	15	mA	V_{DD}
Standby current		I_Q	Sleep X_G, $\overline{CS}$, $\overline{RD}$ = V_{DD}	—	0.05	20	µA	V_{DD}
Oscillation frequency		f_{osc}	AT X'tal	1.0	—	10.0	MHz	XG, XD
External clock frequency		f_{CL}	Duty 47.5%	1.0	—	10.0	MHz	
Feed back resistance		R_f		0.5	1.0	3.0	MΩ	

● DC Electrical Characteristics (2)

(V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –20 to 75°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Terminal
Operating voltage		V_{DD}		2.7	3.5	4.5	V	V_{DD}
Register data retention voltage		V_{OH}		2.0	—	6.0	V	
TTL	High level input voltage	V_{IHT}		0.8xV_{DD}	—	V_{DD}	V	D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, $\overline{VCE}$, $\overline{VRD}$, $\overline{VWR}$
	Low level input voltage	V_{ILT}		V_{SS}	—	0.2xV_{DD}	V	
	High level output voltage	V_{OHT}	I_{OH} = –3.0mA	V_{DD}–0.4	—	—	V	
	Low level output voltage	V_{OLT}	I_{OL} = 3.0mA	—	—	V_{SS}+0.4	V	
CMOS	High level input voltage	V_{IHC}		0.8xV_{DD}	—	V_{DD}	V	SEL1, SEL2, YD, XD0 to XD3, XSCL, YDIS, LP, WF, CL0, XECL, YSCL
	Low level input voltage	V_{ILC}		V_{SS}	—	0.2xV_{DD}	V	
	High level output voltage	V_{OHC}	I_{OH} = –1.0mA	V_{DD}–0.4	—	—	V	
	Low level output voltage	V_{OLC}	I_{OL} = 1.0mA	—	—	V_{SS}+0.4	V	
SCHMITT	Positive trigger threshold voltage	V_{T+}		0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V	$\overline{RES}$
	Negative trigger threshold voltage	V_{T-}		0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V	
Input leakage current		I_{LI}	V_{IN} = V_{DD}/V_{SS}	—	0.05	2.0	µA	
Output leakage current		I_{LO}		—	0.10	5.0	µA	
Average operating current		I_{opr}	f_{osc} = 6.1MHz, No-load 256 × 200 dot	—	3.5 (V_{DD}=3.5V)	7.0	mA	V_{DD}
Standby current		I_Q	Sleep X_G, $\overline{CS}$, $\overline{RD}$ = V_{DD}	—	0.05	20	µA	V_{DD}
Oscillation frequency		f_{osc}	AT X'tal	1.0	—	8.0	MHz	XG, XD
External clock frequency		f_{CL}	Duty 47.5%	1.0	—	8.0	MHz	
Feed back resistance		R_f		0.7	—	4.0	MΩ	

- **Timing Diagrams**
  - **8080-Family Interface Timing**



T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100 pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
WR, $\overline{RD}$	t_{CYC}	System cycle time	See note	—	See note	—	ns	
	t_{CC}	Strobe pulsewidth	120	—	150	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	$\overline{RD}$ access time	—	50	—	80	ns	
	t_{OH8}	Output disable time	10	50	10	55	ns	

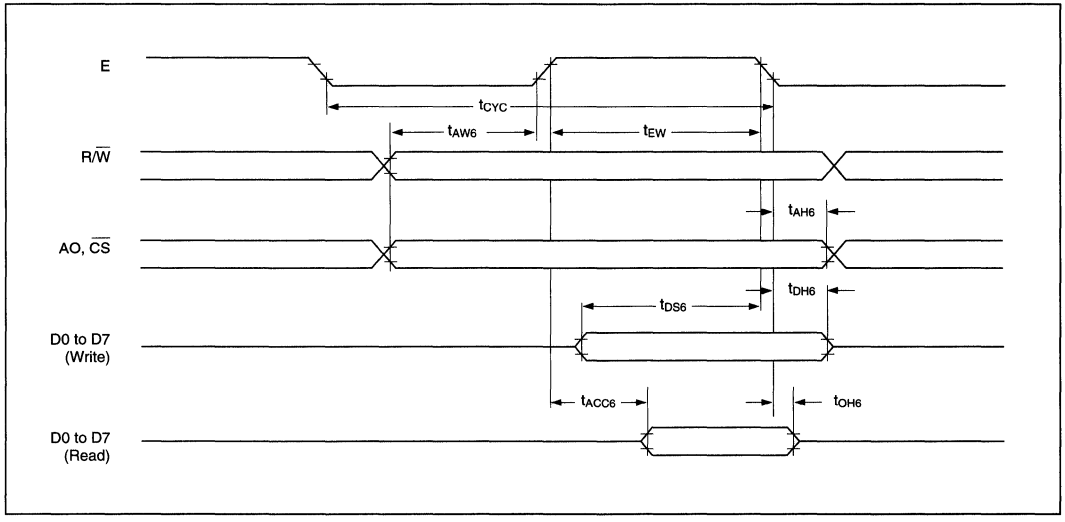
Note: For memory control and system control commands:

$t_{CYC8} = 2tc + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4tc + t_{CC} + 30$

○ 6800-Family Interface Timing



Note: tCYC6 indicates the interval during which $\overline{CS}$ is LOW and E is HIGH.

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$, R/$\overline{W}$	tCYC6	System cycle time	See note	—	See note	—	ns	CL = 100 pF
	tAW6	Address setup time	0	—	10	—	ns	
	tAH6	Address hold time	0	—	0	—	ns	
D0 to D7	tDS6	Data setup time	100	—	120	—	ns	
	tDH6	Data hold time	0	—	0	—	ns	
	tOH6	Output disable time	10	50	10	75	ns	
	tACC6	Access time	—	85	—	130	ns	
E	tEW	Enable pulsewidth	120	—	150	—	ns	

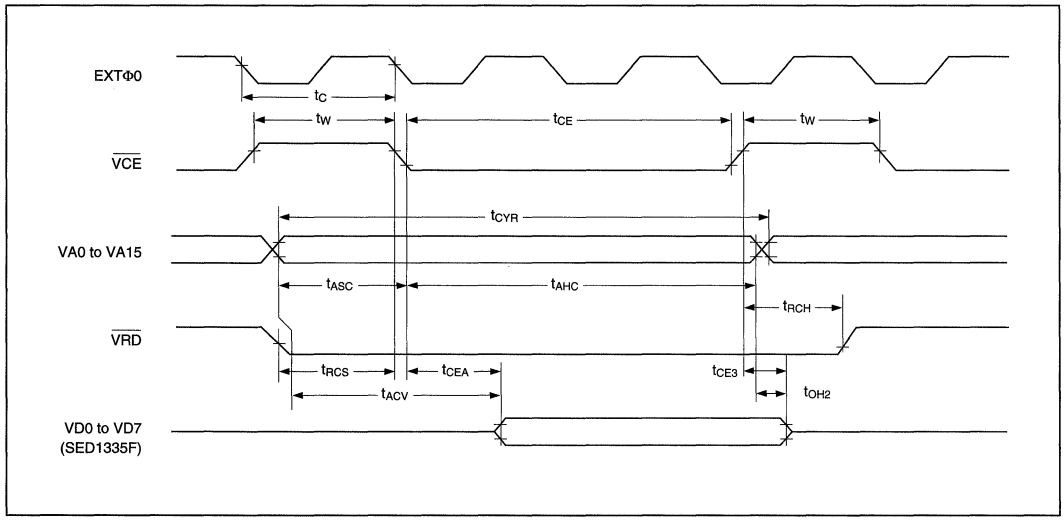
Note: For memory control and system control commands:

tCYC6 = 2tC + tEW + tCEA + 75 > tACV + 245

For all other commands:

tCYC6 = 4tC + tEW + 30

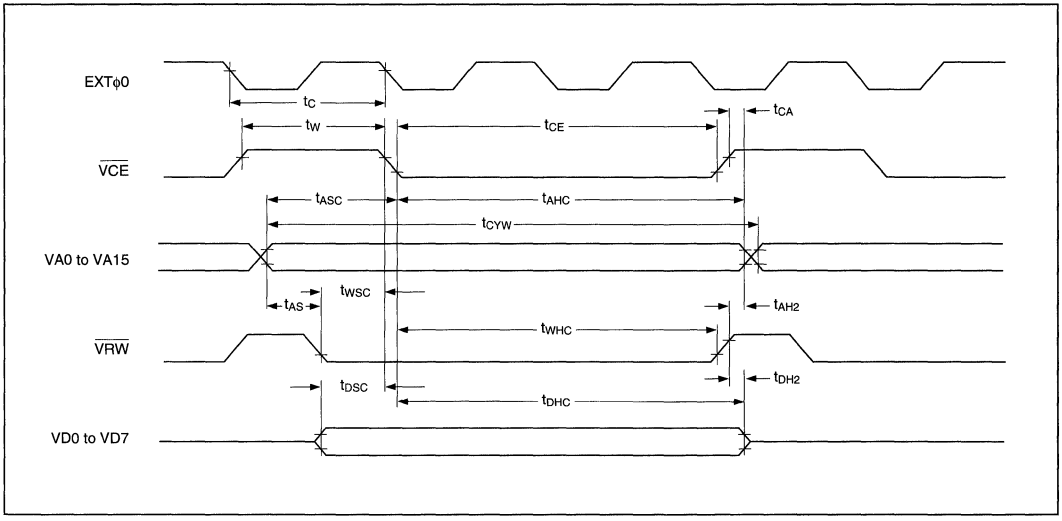
○ Display Memory Read Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	tW	$\overline{VCE}$ HIGH-level pulsewidth	tC – 50	—	tC – 50	—	ns	
	tCE	$\overline{VCE}$ LOW-level pulsewidth	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYR	Read cycle time	3tC	—	3tC	—	ns	
	tASC	Address setup time to falling edge of $\overline{VCE}$	tC – 70	—	tC – 100	—	ns	
	tAHC	Address hold time from falling edge of $\overline{VCE}$	2tC – 30	—	2tC – 40	—	ns	
$\overline{VRD}$	tRCS	Read cycle setup time to falling edge of $\overline{VCE}$	tC – 45	—	tC – 60	—	ns	
	tRCH	Read cycle hold time from rising edge of $\overline{VCE}$	0.5tC	—	0.5tC	—	ns	
VD0 to VD7	tACV	Address access time	—	3tC – 100	—	3tC – 115	ns	
	tCEA	$\overline{VCE}$ access time	—	2tC – 80	—	2tC – 90	ns	
	tOH2	Output data hold time	0	—	0	—	ns	
	tCE3	$\overline{VCE}$ to data off time	0	—	0	—	ns	

○ Display Memory Write Timing

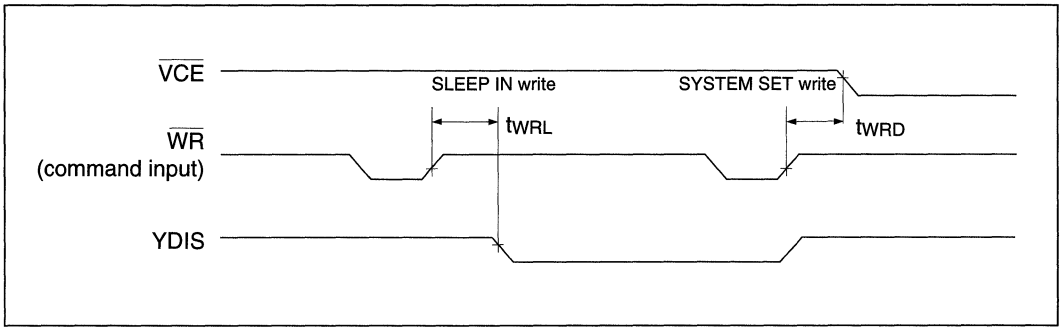


Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
VCE	tW	VCE HIGH-level pulse-width	tC – 50	—	tC – 50	—	ns	
	tCE	VCE LOW-level pulse-width	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYW	Write cycle time	3tC	—	3tC	—	ns	
	tAHC	Address hold time from falling edge of VCE	2tC – 30	—	2tC – 40	—	ns	
	tASC	Address setup time to falling edge of VCE	tC – 70	—	tC – 110	—	ns	
	tCA	Address hold time from rising edge of VCE	0	—	0	—	ns	
	tAS	Address setup time to falling edge of VWR	0	—	0	—	ns	
	tAH2	Address hold time from rising edge of VWR	10	—	10	—	ns	
VWR	tWSC	Write setup time to falling edge of VCE	tC – 80	—	tC – 115	—	ns	
	tWHC	Write hold time from falling edge of VCE	2tC – 20	—	2tC – 20	—	ns	
VD0 to VD7	tDSC	Data input setup time to falling edge of VCE	tC – 85	—	tC – 125	—	ns	
	tDHC	Data input hold time from falling edge of VCE	2tC – 30	—	2tC – 30	—	ns	
	tDH2	Data hold time from rising edge of VWR	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

○ SLEEP IN Command Timing



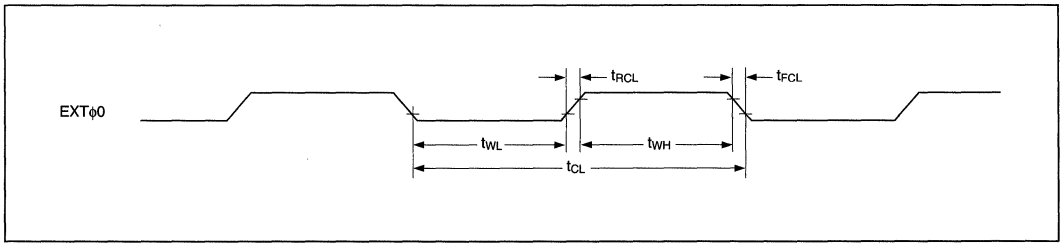
T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
WR	tWRD	VCE falling-edge delay time	*1	—	*1	—	ns	CL = 100 pF
	tWRL	YDIS falling-edge delay time	—	*2	—	*2	ns	

Notes:

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C \times [TC/R] \times [L/F] + 70$

● External Oscillator Signal Timing



T_a = –20 to 75°C

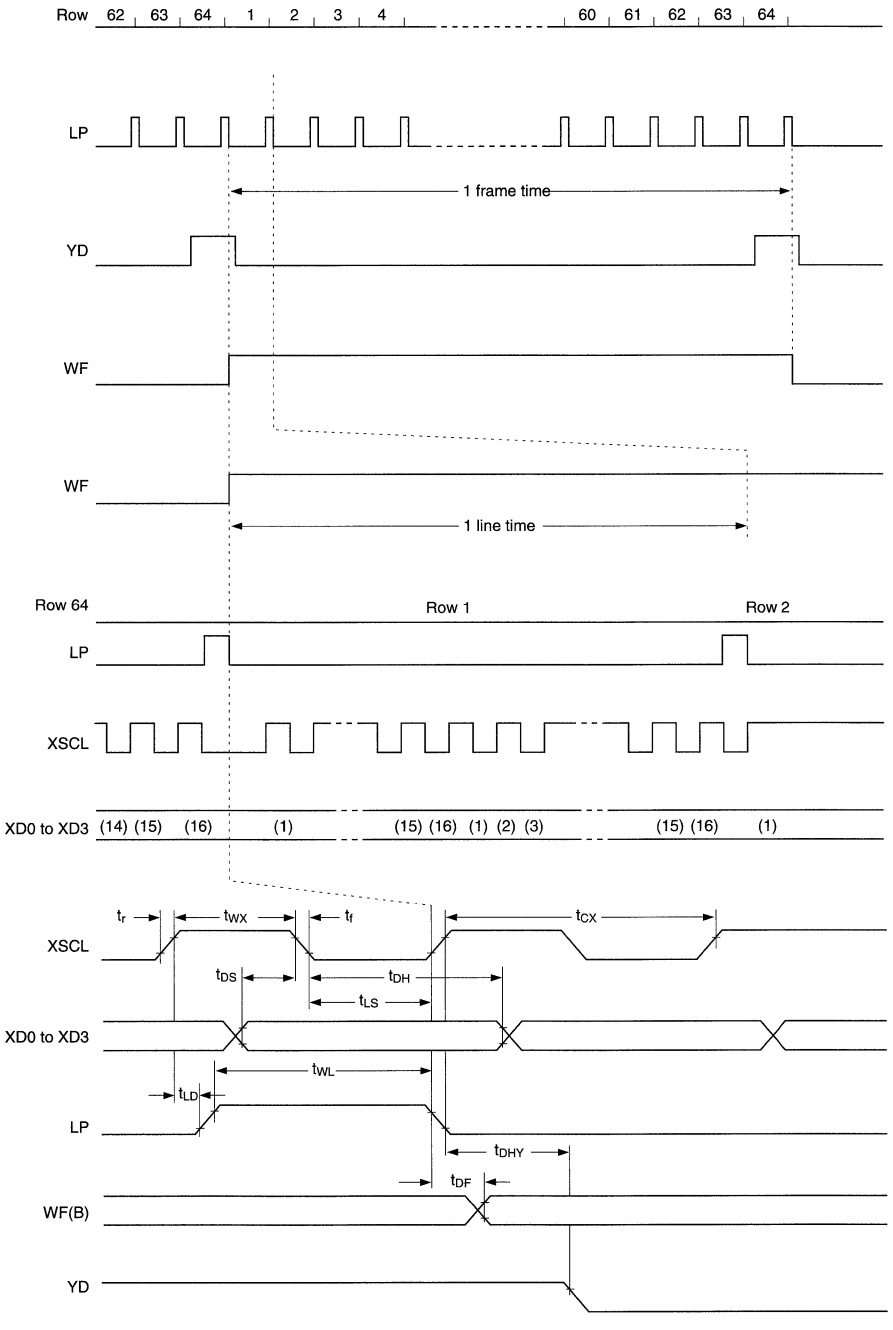
Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT φ0	tRCL	External clock rise time	—	15	—	15	ns	
	tFCL	External clock fall time	—	15	—	15	ns	
	tWH	External clock HIGH-level pulsewidth	*1	*2	*1	*2	ns	
	tWL	External clock LOW-level pulsewidth	*1	*2	*1	*2	ns	
	tC	External clock period	100	—	125	—	ns	

Notes:

1. $(t_C - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$
2. $(t_C - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

○ LCD Output Timing

The following characteristics are for a 1/64 duty cycle.

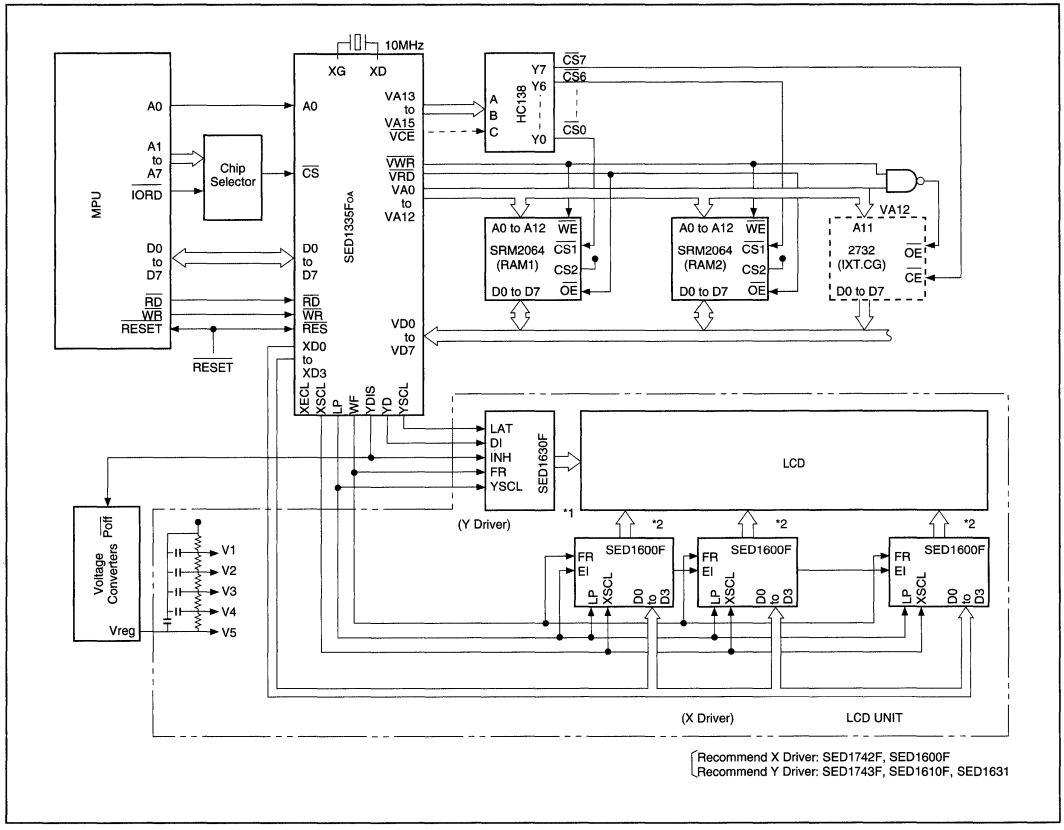


T_a = –20 to 75°C

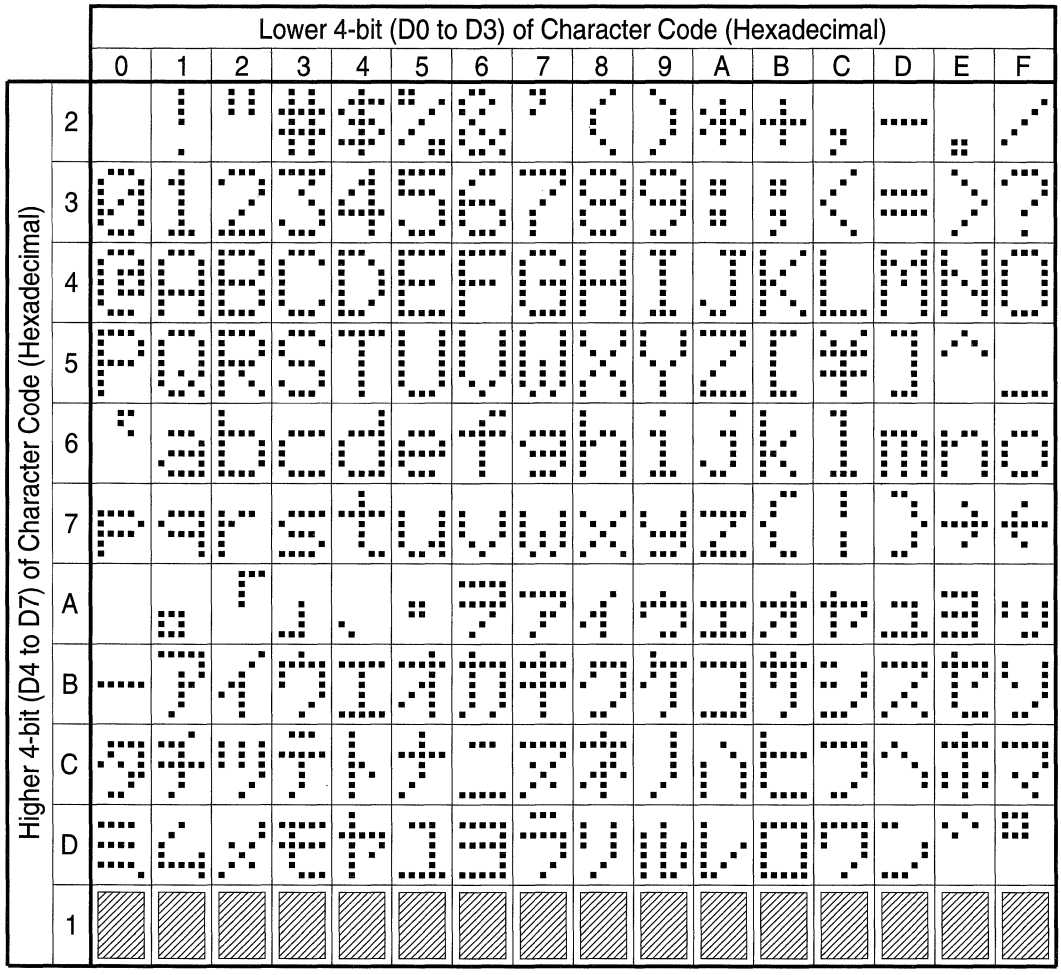
Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
	t_r	Rise time	—	30	—	40	ns	CL = 100pF
	t_f	Fall time	—	30	—	40	ns	
XSCL	t_{CX}	Shift clock cycle time	4tc	—	4tc	—	ns	
	t_{WX}	XSCL clock pulsewidth	2tc – 60	—	2tc – 60	—	ns	
XD0 to XD3	t_{DH}	X data hold time	2tc – 50	—	2tc – 50	—	ns	
	t_{DS}	X data setup time	2tc – 100	—	2tc – 105	—	ns	
LP	t_{LS}	Latch data setup time	2tc – 50	—	2tc – 50	—	ns	
	t_{WL}	LP pulsewidth	4tc – 80	—	4tc – 120	—	ns	
	t_{LD}	LP delay time from XSCL	0	—	0	—	ns	
WF	t_{DF}	Permitted WF delay	—	50	—	50	ns	
YD	t_{DHY}	Y data hold time	2tc – 20	—	2tc – 20	—	ns	

Note: The SED1335F reads display memory data from the address of the top left corner of the display screen, then scans horizontally until it reaches the address for the bottom right corner of the display screen. Therefore, each line of X-driver data is sent starting from the left side of the display line.

■ EXAMPLE OF APPLICATION



■ CHARACTER CODE TABLE (Built-in Character Generator)



CMOS GRAPHIC LCD/TV CONTROLLER

- **For Medium-Scale LCD**
- **Output to LCD-Screen**
- **Virtual Screen Display RAM**
- **Enhanced Control Function**
- **Simultaneous LCD & TV Display**

■ DESCRIPTION

The SED1336 is a CMOS low-power dot matrix liquid crystal graphic display controller with built-in TV support. The built-in TV support IC is capable of displaying characters and graphic images simultaneously on TV monitors and flat panels.

The SED1336 has a built-in TV control circuit that generates either NTSC or PAL system synchronous signals, memory. The device stores the display data in external SRAM that is sent by an 8-bit microcomputer, and generates all the control signals required by the LCD drivers.

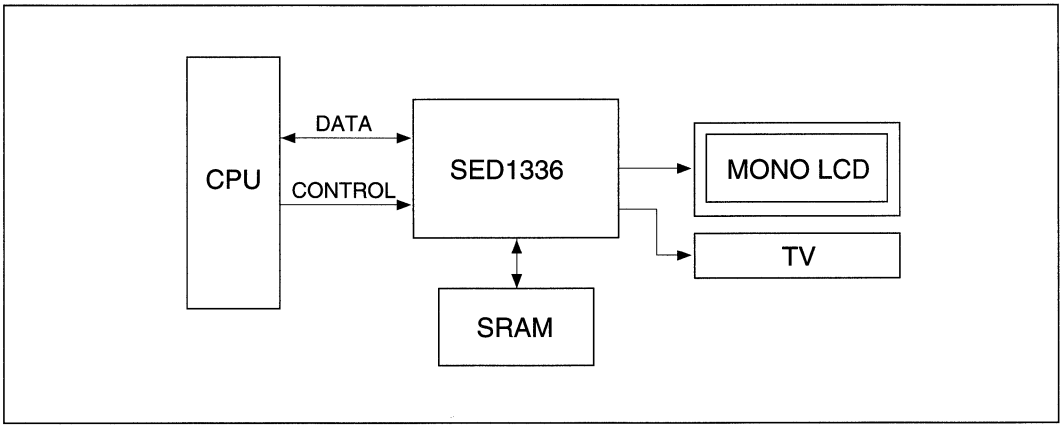
The controller incorporates an internal character generator ROM which supports user-defined characters. An external CG ROM can also be supported to provide additional characters.

The SED1336 can be interfaced to high-speed microprocessors such as the Intel 80xx family or the Motorola 68xx family. The controller supports a set of commands that allow the user to create a layered display of characters and graphics.

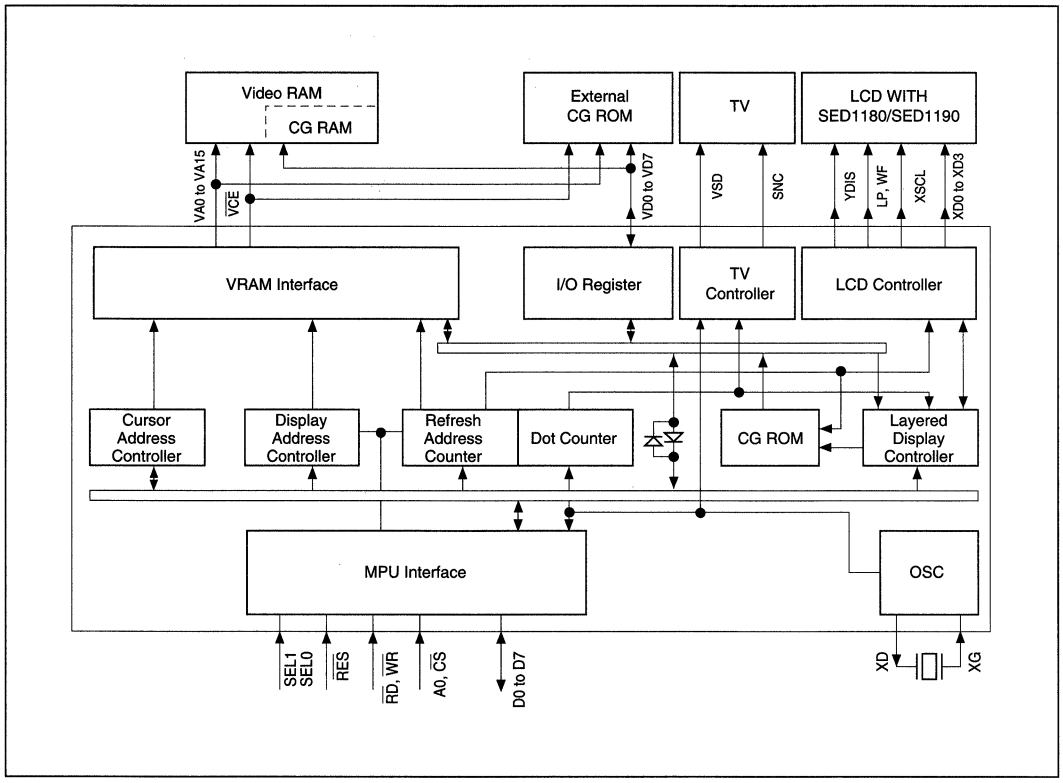
■ FEATURES

- Low-power CMOS fabrication
- Compatible with both Intel 80XX and Motorola 68XX high-speed MPU
- Display duty:
  LCD ..... 1/2 to 1/256 can be selected
  TV ..... 256 × 200 dots
- Internal and external character generator ROM
- Simultaneous LCD and TV operation
- Selectable display synthesis
- Programmable cursor movement
- Multimode display:
  2 layers of overlapping character and graphic
  3 layers of overlapping graphic
- Supports 64K bytes of memory
- Single power supply ..... 3.0V to 5.5V
- Package ..... Plastic QFP6-60 pin (FOA)

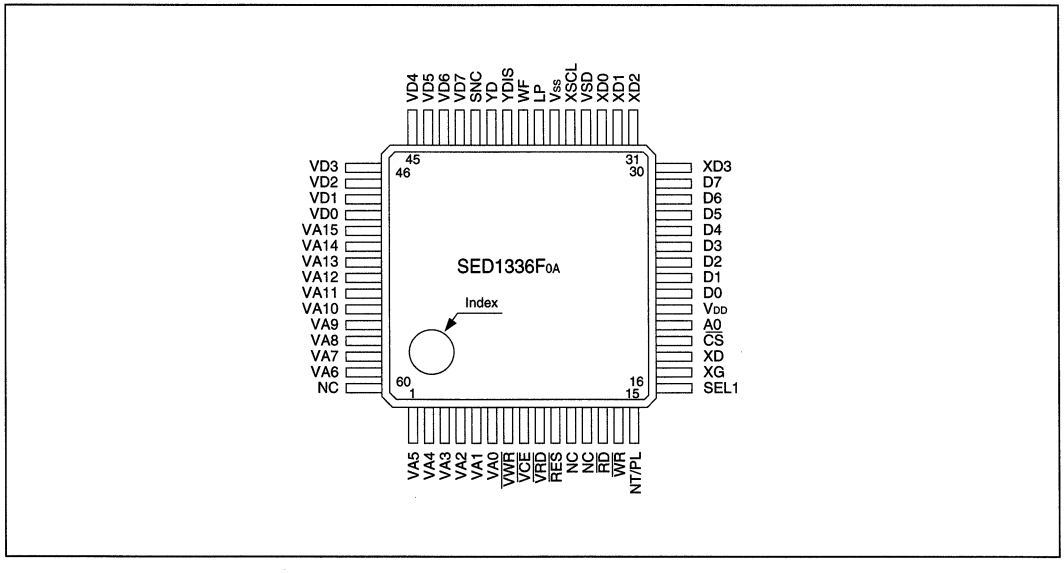
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN ASSIGNMENT DIAGRAM



■ PIN DESCRIPTION

Name	Number	Type	Description
VA0 to VA5 VA6 to VA15	6 to 1 59 to 50	Output	VRAM address bus
$\overline{VWR}$	7	Output	VRAM write signal
$\overline{VCE}$	8	Output	Memory control signal
$\overline{VRD}$	9	Output	VRAM read signal
$\overline{RES}$	10	Input	Reset
NC	11, 60	—	No connection
CLO	12	Output	Clock output
$\overline{RD}$	13	Input	8080-family: Read signal 6800-family: Enable clock (E)
$\overline{WR}$	14	Input	8080-family: Write signal 6800-family: R/$\overline{W}$ signal
NT/PL	15	Input	NTSC or PAL TV mode select
SEL1	16	Input	8080- or 6800-family interface select
OSC1	17	Input	Oscillator connection
OSC2	18	Output	Oscillator connection
$\overline{CS}$	19	Input	Chip select
A0	20	Input	Data type select
VDD	21	Supply	3.0 to 5.5V supply
D0 to D7	22 to 29	Input/output	Data bus
XD0 to XD3	30 to 33	Output	Data to LCD X-driver
VSD	34	Output	Video data
XSCL	35	Output	Data shift clock
VSS	36	Supply	Ground
LP	37	Output	Latch pulse
WF	38	Output	Frame signal
YDIS	39	Output	Power-down signal when display is blanked
YD	40	Output	Scan start pulse
SNC	41	Output	TV sync signal
VD0 to VD7	42 to 49	Input/output	VRAM data bus

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	300	mW
Operating temperature range	T_{opr}	–20 to 75	°C
Storage temperature range	T_{stg}	–65 to 150	°C
Soldering temperature (10 seconds). See note 1.	T_{solder}	260	°C

1. The humidity resistance of the flat package may be reduced if the package is immersed in solder. Use a soldering technique that does not heatstress the package.
2. If the power supply has a high impedance, a large voltage differential can occur between the input and supply voltages. Take appropriate care with the power supply and the layout of the supply lines.
3. All supply voltages are referenced to V_{SS} = 0V.

● DC Electrical Characteristics

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_a = –20 to 75°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Register data retention voltage	V_{HO}		2.0	—	6.0	V
Input leakage current	I_{LI}	V_I = V_{DD}. See note 6.	—	0.05	2.0	µA
Output leakage current	I_{LO}	V_I = V_{SS}. See note 6.	—	0.10	5.0	µA
Operating supply current	I_{opr}	See note 4.	—	11	15	mA
Quiescent supply current	I_Q	Sleep mode, V_{OSC1} = $V\overline{CS}$ = $V\overline{RD}$ = V_{DD}	—	0.05	20.0	µA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 7.	1.0	—	10.0	MHz
External clock frequency	f_{CL}		1.0	—	10.0	MHz
Oscillator feedback resistance	R_f		0.5	1.0	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	0.8V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHT}	I_{OH} = –5.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	I_{OL} = 5.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHC}	I_{OH} = –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	I_{OH} = 1.6 mA. See note 2.	—	—	V_{SS} + 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	I_{OL} = 6.0 mA. See note 5.	—	—	V_{SS} + 0.4	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
Falling-edge threshold voltage	V_{T-}	See note 3.	0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V

Notes:

1. D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, $\overline{VRD}$, $\overline{VWR}$ and $\overline{VCE}$ are TTL-level inputs.
2. SEL1 and NT/PL are CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS and CLO are CMOS-level outputs.
3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200 µs. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. fOSC = 10 MHz, no load (no display memory), internal character generator, 256 × 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
5. SNC and VSD are n-channel, open-drain outputs. The voltage on the outputs should not exceed V_{DD} as internal diodes connect the pins to V_{DD} (SED1336F only).
6. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
7. Because the oscillator circuit input bias current is in the order of µA, design the printed circuit board so as to reduce leakage currents.

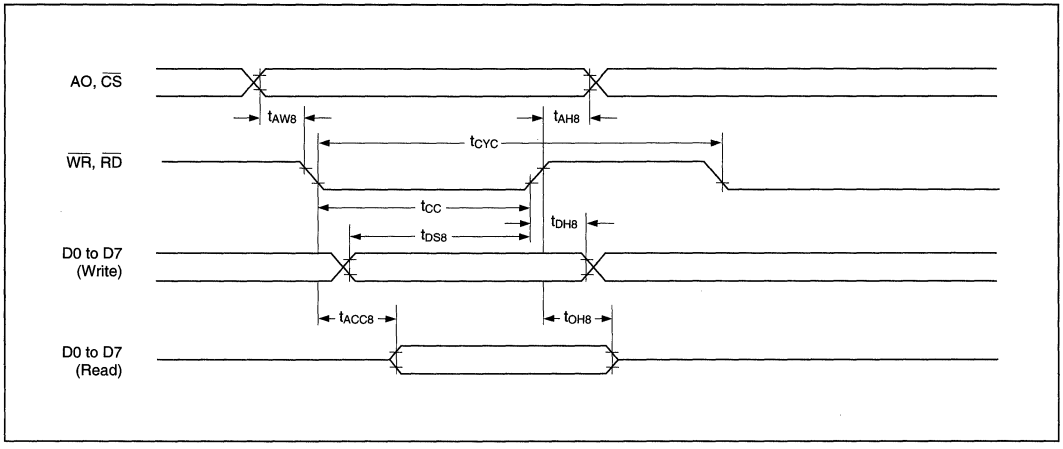
V_{DD} = 3.0 to 4.5V, V_{SS} = 0V, T_a = –20 to 75°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}	See note 8.	3.0	3.5	4.5	V
Register data retention voltage	V_{HO}		2.0	—	6.0	V
Input leakage current	I_{LI}	V_I = V_{DD}. See note 6.	—	0.05	2.0	µA
Output leakage current	I_{LO}	V_I = V_{SS}. See note 6.	—	0.10	5.0	µA
Operating supply current	I_{opr}	V_{DD} = 3.5V. See note 4. See note 4.	— —	3.5 —	— 7.0	mA
Quiescent supply current	I_Q	Sleep mode, V_{OSC1} = $V_{\overline{CS}}$ = $V_{\overline{RD}}$ = V_{DD}	—	0.05	20.0	µA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 7.	1.0	—	8.0	MHz
External clock frequency	f_{CL}		1.0	—	8.0	MHz
Oscillator feedback resistance	R_f		0.7	—	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	0.8V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHT}	I_{OH} = –3.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	I_{OL} = 3.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHC}	I_{OH} = –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	I_{OH} = 1.6 mA. See note 2.	—	—	V_{SS} + 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	I_{OL} = 6.0 mA. See note 5.	—	—	V_{SS} + 0.4	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
Falling edge threshold voltage	V_{T-}	See note 3.	0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V

Notes:

1. D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, $\overline{VRD}$, $\overline{VWR}$ and $\overline{VCE}$ are TTL-level inputs.
2. SEL1 and NT/PL are CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS and CLO are CMOS-level outputs.
3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200 µs. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. fOSC = 10 MHz, no load (no display memory), internal character generator, 256 × 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
5. SNC and VSD are n-channel, open-drain outputs. The voltage on the outputs should not exceed V_{DD} as internal diodes connect the pins to V_{DD}.
6. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
7. Because the oscillator circuit input bias current is in the order of µA, design the printed circuit board so as to reduce leakage currents.
8. V_{DD} = 2.7 to 4.5V (SED1335F)

- **Timing Diagrams**
  - **8080-Family Interface Timing**



T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
A0, CS	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100 pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
WR, RD	t_{CYC}	System cycle time	See note	—	See note	—	ns	
	t_{CC}	Strobe pulsewidth	120	—	140	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	RD access time	—	50	—	70	ns	
	t_{OH8}	Output disable time	10	50	10	50	ns	

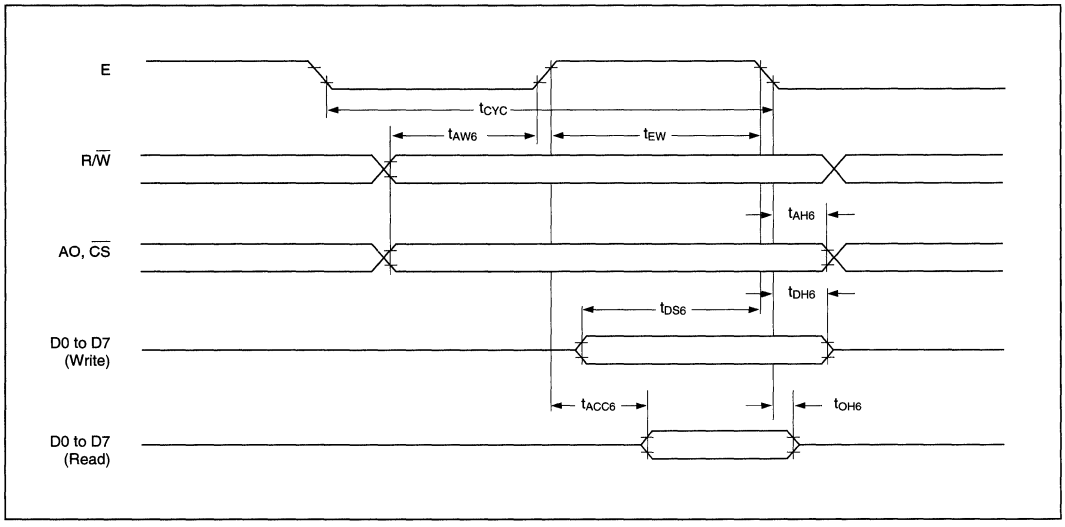
Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

○ 6800-Family Interface Timing



Note: tCYC6 indicates the interval during which $\overline{CS}$ is LOW and E is HIGH.

Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$, R/$\overline{W}$	tCYC6	System cycle time	See note	—	See note	—	ns	CL = 100 pF
	tAW6	Address setup time	0	—	10	—	ns	
	tAH6	Address hold time	0	—	0	—	ns	
D0 to D7	tDS6	Data setup time	100	—	120	—	ns	
	tDH6	Data hold time	0	—	0	—	ns	
	tOH6	Output disable time	10	50	10	70	ns	
	tACC6	Access time	—	85	—	120	ns	
E	tEW	Enable pulsewidth	120	—	140	—	ns	

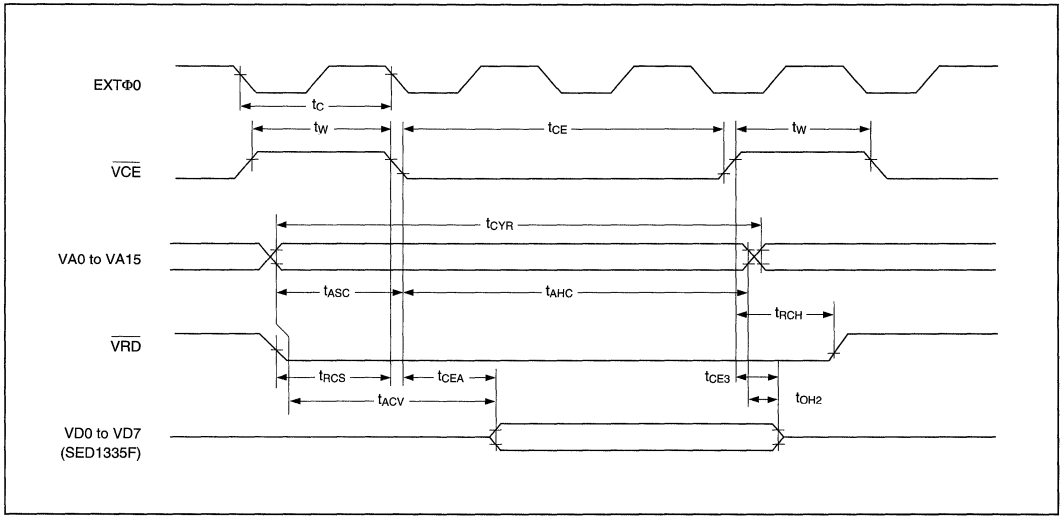
Note: For memory control and system control commands:

tCYC6 = 2tC + tEW + tCEA + 75 > tACV + 245

For all other commands:

tCYC6 = 4tC + tEW + 30

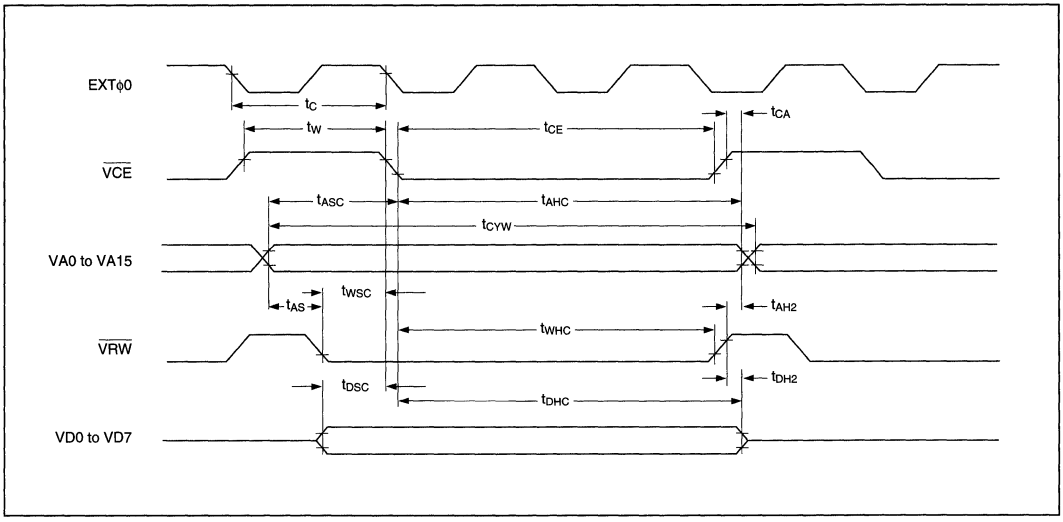
○ **Display Memory Read Timing**



T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
VCE	tW	VCE HIGH-level pulsewidth	tC – 50	—	tC – 50	—	ns	
	tCE	VCE LOW-level pulsewidth	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYR	Read cycle time	3tC	—	3tC	—	ns	
	tASC	Address setup time to falling edge of VCE	tC – 70	—	tC – 100	—	ns	
	tAHC	Address hold time from falling edge of VCE	2tC – 30	—	2tC – 40	—	ns	
VRD	tRCS	Read cycle setup time to falling edge of VCE	tC – 45	—	tC – 55	—	ns	
	tRCH	Read cycle hold time from rising edge of VCE	0.5tC	—	0.5tC	—	ns	
VD0 to VD7	tACV	Address access time	—	3tC – 100	—	3tC – 110	ns	
	tCEA	VCE access time	—	2tC – 80	—	2tC – 85	ns	
	tOH2	Output data hold time	0	—	0	—	ns	
	tCE3	VCE to data off time	0	—	0	—	ns	

○ Display Memory Write Timing

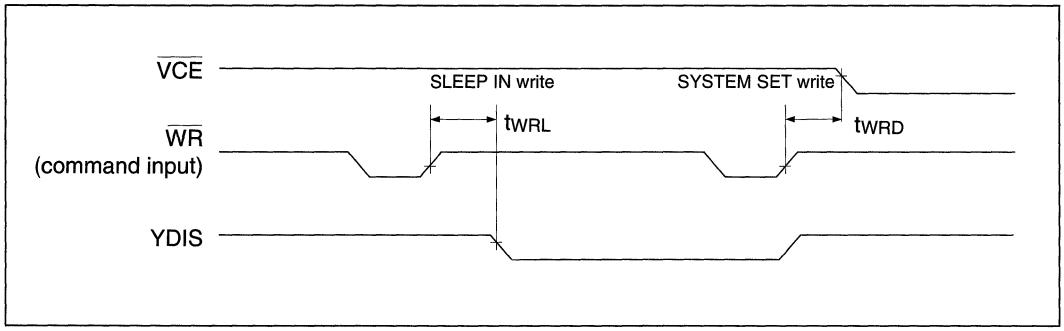


Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
VCE	tW	VCE HIGH-level pulse-width	tC – 50	—	tC – 50	—	ns	
	tCE	VCE LOW-level pulse-width	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYW	Write cycle time	3tC	—	3tC	—	ns	
	tAHC	Address hold time from falling edge of VCE	2tC – 30	—	2tC – 40	—	ns	
	tASC	Address setup time to falling edge of VCE	tC – 70	—	tC – 100	—	ns	
	tCA	Address hold time from rising edge of VCE	0	—	0	—	ns	
	tAS	Address setup time to falling edge of VWR	0	—	0	—	ns	
	tAH2	Address hold time from rising edge of VWR	10	—	10	—	ns	
VWR	tWSC	Write setup time to falling edge of VCE	tC – 80	—	tC – 110	—	ns	
	tWHC	Write hold time from falling edge of VCE	2tC – 20	—	2tC – 20	—	ns	
VD0 to VD7	tDSC	Data input setup time to falling edge of VCE	tC – 85	—	tC – 120	—	ns	
	tDHC	Data input hold time from falling edge of VCE	2tC – 30	—	2tC – 30	—	ns	
	tDH2	Data hold time from rising edge of VWR	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

○ SLEEP IN Command Timing

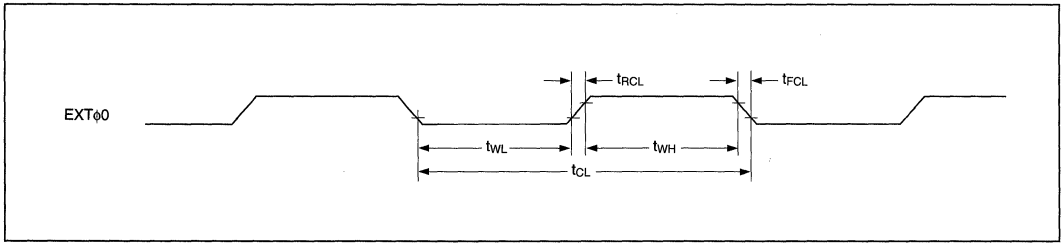


T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
$\overline{WR}$	t_{WRD}	$\overline{VCE}$ falling-edge delay time	*1	—	*1	—	ns	CL = 100 pF
	t_{WRL}	YDIS falling-edge delay time	—	*2	—	*2	ns	

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C \times [TC/R] \times [L/F] + 70$

○ External Oscillator Signal Timing



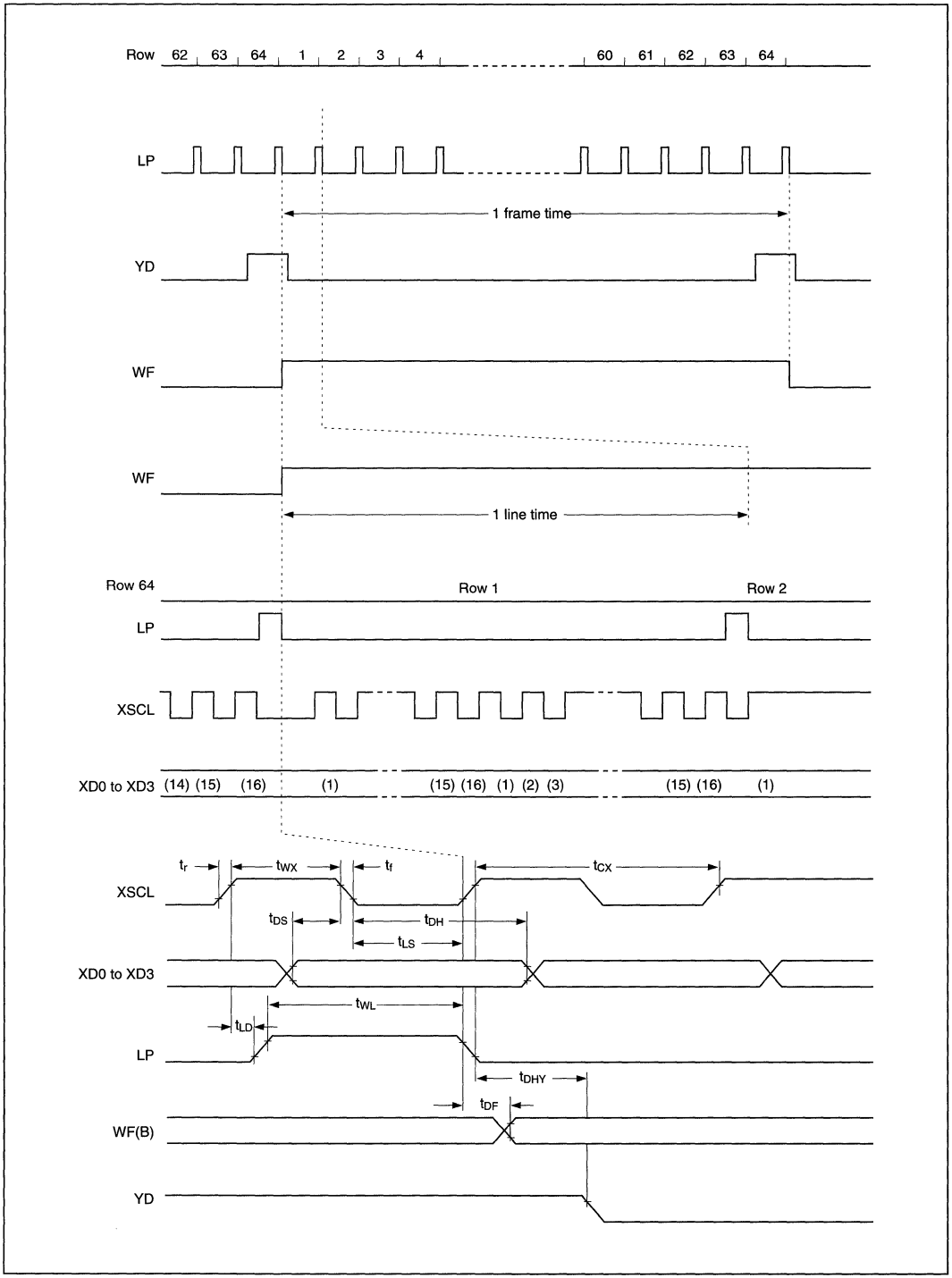
T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	t_{RCL}	External clock rise time	—	15	—	15	ns	
	t_{FCL}	External clock fall time	—	15	—	15	ns	
	t_{WH}	External clock HIGH-level pulsewidth	*1	*2	*1	*2	ns	
	t_{WL}	External clock LOW-level pulsewidth	*1	*2	*1	*2	ns	
	t_C	External clock period	100	—	125	—	ns	

1. $(t_C - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$
2. $(t_C - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

○ LCD Output Timing

The following characteristics are for a 1/64 duty cycle.



T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
	t_r	Rise time	—	30	—	35	ns	CL = 100 pF
	t_f	Fall time	—	30	—	35	ns	
XSCL	t_{CX}	Shift clock cycle time	4tc	—	4tc	—	ns	
	t_{WX}	XSCL clock pulsewidth	2tc – 60	—	2tc – 60	—	ns	
XD0 to XD3	t_{DH}	X data hold time	2tc – 50	—	2tc – 50	—	ns	
	t_{DS}	X data setup time	2tc – 100	—	2tc – 100	—	ns	
LP	t_{LS}	Latch data setup time	2tc – 50	—	2tc – 50	—	ns	
	t_{WL}	LP pulsewidth	4tc – 80	—	4tc – 100	—	ns	
	t_{LD}	LP delay time from XSCL	0	—	0	—	ns	
WF	t_{DF}	Permitted WF delay	—	50	—	50	ns	
YD	t_{DHY}	Y data hold time	2tc – 20	—	2tc – 20	—	ns	

Note: The SED1336F reads display memory data from the address of the top left corner of the display screen, then scans horizontally until it reaches the address for the bottom right corner of the display screen. Therefore, each line of X-driver data is sent starting from the left side of the display line.

CMOS VIDEO – LCD INTERFACE (VLI)

■ DESCRIPTION

The SED1341 is a VLI (video-LCD interface) for converting previously separated video signals, intended for a CRT display, into signals compatible with dot-matrix liquid-crystal displays (LCDs). When sync and data separators are added, composite video signals can also be processed. Using the SED1341, a compact LCD monitor can replace a monochrome CRT display without including additional software or hardware.

The frame-buffer memory controlled by the VLI accurately matches the high-frequency video signals to the low-frequency operation of the LCD unit. A screen alignment function for the adjustment of the display position makes it easy to implement an LCD module that is compatible with CRT display.

Individual selection of the video data screen and LCD panel sizes and a vertical double line display mode allow the SED1341 to interface LCDs with the video outputs of a variety of personal computers (PCs).

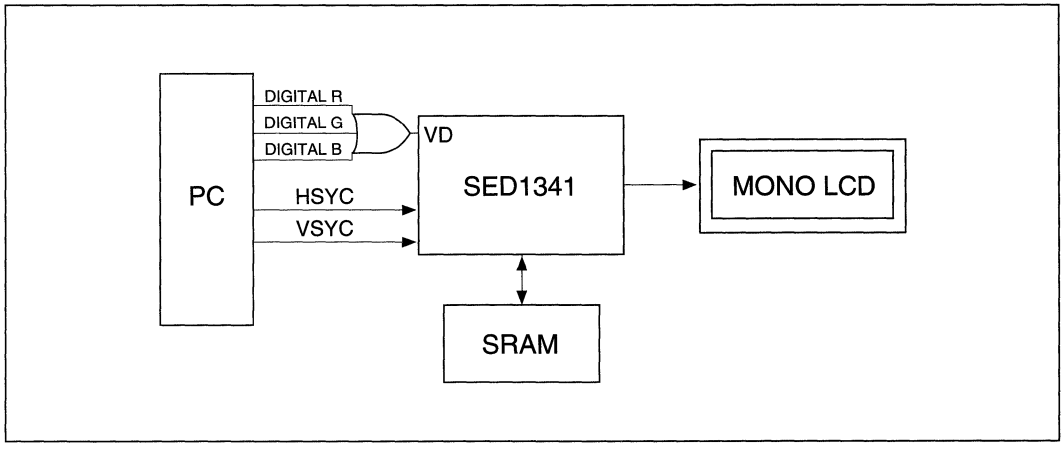
■ FEATURES

- Low-power CMOS technology
- TTL-compatible signal input
- Built-in PLL to generate dot clock
- Screen alignment adjustment via 4-bit bus or hardware
- Horizontal and vertical back porch register
- Internal oscillator to optimize the frame frequency to match the LCD timing
- Supports vertical flyback time
- Supports single panel and dual panel
- Supports 4-bit, 8-bit dual panel and 8-bit single panel
- Supports 40KB SRAM frame buffer
- Supports screen size from 640 × 200 to 720 × 400
- Duty cycle ..... 1/100 to 1/496
- Power-on clear function
- Single power supply ..... 5V ± 5%
- Package ..... QFP5-80 pin (FOE)

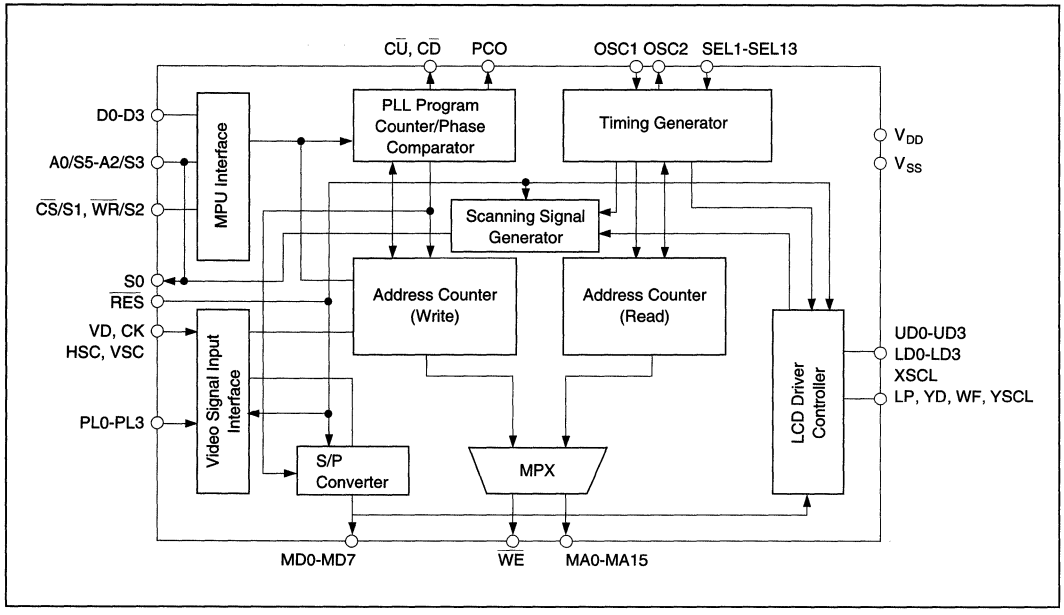
■ AVAILABLE MODELS

SED1341FOC and SED1341FOE. See the functional comparison table at the end of this data sheet.

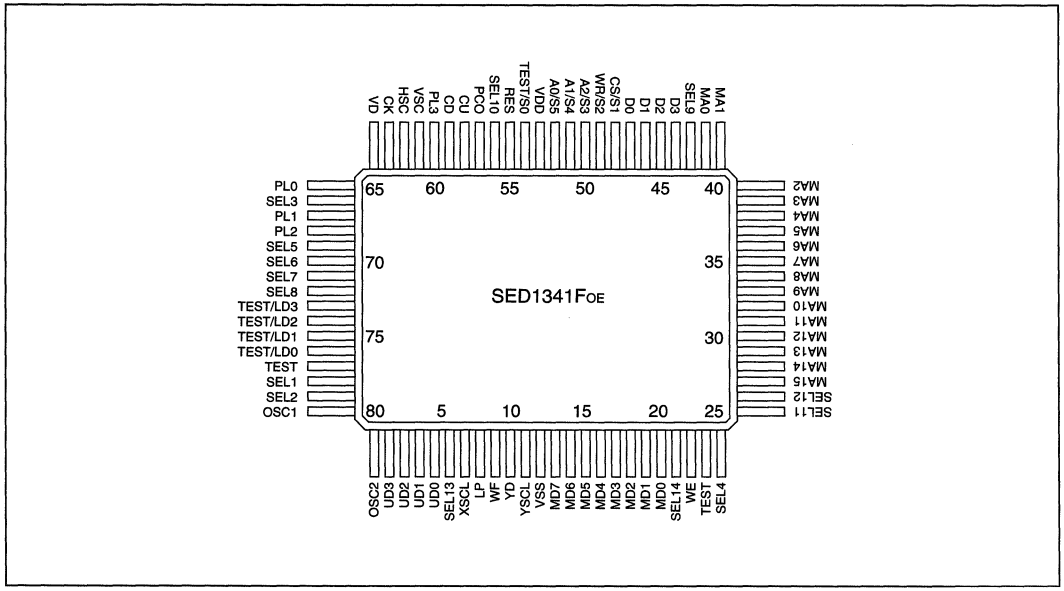
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ SED1341F0C/SED1341F0E Pin Comparison



■ PINOUT

Pin	
Number	Name
1	OSC2
2	UD3
3	UD2
4	UD1
5	UD0
6	SEL13
7	XSCL
8	LP
9	WF
10	YD
11	YSCL
12	Vss
13	MD7
14	MD6
15	MD5
16	MD4
17	MD3
18	MD2
19	MD1
20	MD0

Pin	
Number	Name
21	SEL14
22	$\overline{WE}$
23	TEST
24	SEL4
25	SEL11
26	SEL12
27	MA15
28	MA14
29	MA13
30	MA12
31	MA11
32	MA10
33	MA9
34	MA8
35	MA7
36	MA6
37	MA5
38	MA4
39	MA3
40	MA2

Pin	
Number	Name
41	MA1
42	MA0
43	SEL9
44	D3
45	D2
46	D1
47	D0
48	$\overline{CS}$/S1
49	$\overline{WR}$/S2
50	A2/S3
51	A1/S4
52	A0/S5
53	VDD
54	TEST/S0
55	$\overline{RES}$
56	SEL10
57	PCO
58	$\overline{CU}$
59	$\overline{CD}$
60	PL3

Pin	
Number	Name
61	VSC
62	HSC
63	CK
64	VD
65	PL0
66	SEL3
67	PL1
68	PL2
69	SEL5
70	SEL6
71	SEL7
72	SEL8
73	TEST/LD3
74	TEST/LD2
75	TEST/LD1
76	TEST/LD0
77	TEST
78	SEL1
79	SEL2
80	OSC1

Note: TEST pins must be left open as they are wired to individual IC chips inside the package.

■ PIN DESCRIPTION

Pin Name	Pin Number	Description	
V_{DD}	53	Supply voltage (+5V)	
V_{SS}	12	GND	
OSC1	80	Oscillator pin (input)	
OSC2	1	Oscillator pin (output)	
UD0 to UD3	5 to 2	X-driver data bus output (upper)	
TEST/LD0 to TEST/LD3	76 to 73	X-driver data bus output (lower)	
XSCL	7	X-driver shift clock output	
LP	8	Latch pulse output	
WF	9	AC waveform output for LCD	
YD	10	Row scanning start data output for Y-driver	
YSCL	11	Y-driver shift clock output	
VD	64	Video data input	
CK	63	Dot clock input	
HSC	62	Horizontal sync signal input	
VSC	61	Vertical sync signal input	
MA0 to MA15	42 to 27	Address bus output to frame buffer memory	
MD0 to MD7	20 to 13	Data bus I/O to frame buffer memory	
$\overline{WE}$	22	Write enable signal output	
D0 to D3	47 to 44	Data input for screen position input	
		SEL5 = LOW	SEL5 = HIGH
TEST/S0	54	TEST	Scan signal output for digital switch
A0/S5 to A2/S3	52 to 50	Address bus input	Scan signal output for digital switch
$\overline{CS}$/S1	48	Chip select input	Scan signal output for digital switch
$\overline{WR}$/S2	49	Write signal input	Scan signal output for digital switch
$\overline{RES}$	55	Reset signal input	
SEL1	78	LCD drive mode select input (single/dual)	
SEL2	79	LCD panel line number select input	
SEL3	66	LCD panel line number select input	
SEL4	24	LCD panel line length select input	
SEL5	69	Screen alignment method select input (SW/MPU) (disable/enable)	
SEL6	70	LCD panel vertical flyback time select input	
SEL7	71	Latch pulse output timing select input (edge/level)	
SEL8	72	X-driver interface data bus select input (4-bit, 4 × 2-bit, 8-bit)	
SEL9	43	LCD panel vertical flyback line number select input	
SEL10	56	Video data vertical line number select input	
SEL11	25	Video data vertical line number select input	
SEL12	26	Video data line length select input	
SEL13	6	Vertical doubleline display select input (enable/disable)	
SEL14	21	Horizontal back porch range select input (normal/high)	
PL0	65	Polarity select input for video signal VD	
PL1	67	Polarity select input for video signal HSC	
PL2	68	Polarity select input for video signal VSC	
PL3	60	Polarity select input for video signal CK	
PCO	57	Program counter output from PLL section	
$\overline{CU}$, $\overline{CD}$	58, 59	Phase comparator output from PLL section	

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.3 to 7.0	V
Input voltage	V_I	–0.3 to V_{DD}+0.3	V
Output voltage	V_D	–0.3 to V_{DD}+0.3	V
I/O voltage	$V_{I/O}$	–0.3 to V_{DD}+0.3	V
Output current	I_O	–10 to 10	mA
Power dissipation	P_D	250	mW
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

● RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Supply voltage	V_{SS}		—	0	—	V

● DC CHARACTERISTICS

(V_{DD} = 5V±5%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Oscillation Frequency	f_{OSC}	fck = 14.3MHz (640×200)	fck/3.6	4.5	fck/2.28	MHz
		fck = 16MHz (640×350)	fck/3.6	7	and	MHz
		fck = 21MHz (640×400)	fck/3.6	9	11.2	MHz
		fck = 24MHz (640×480)	fck=3.6	10		MHz
Average Operating Current Consumption	I_{opr}	fck = 32MHz f_{osc} = 12MHz	—	—	40	mA
High Level Input Voltage 1	V_{IH1}	*1	2.0	—	V_{DD}+0.3	V
Low Level Input Voltage 1	V_{IL1}		–0.3	—	0.8	V
High Level Input Voltage 2	V_{IH2}	*2	4.0	—	V_{DD}+0.3	V
Low Level Input Voltage 2	V_{IL2}		–0.3	—	0.8	V
High Level Input Voltage 3	V_{IH3}	*3	3.0	—	V_{DD}+0.3	V
Low Level Input Voltage 3	V_{IL3}		–0.3	—	0.6	V
High Level Output Voltage	V_{OH}	I_{OH} = –2mA *4	4.35	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 6mA *4	—	—	0.4	V
Input Current Leakage	I_{L1}	VI–0V to V_{DD}	–1	—	1	mA
I/O Current Leakage	$I_{LI/O}$	$V_{I/O}$ = 0V to V_{DD}	–1	—	1	mA

Notes:

*1. VD, CK, HSC, VSC, MD0 to MD7, A0 to A2, CS, WR, SEL9, SEL10

*2. PL0 to PL3, SEL1 to SEL8, SEL11 to SEL13, D0 to D3

*3. RES

*4. Except OSC2 Pin

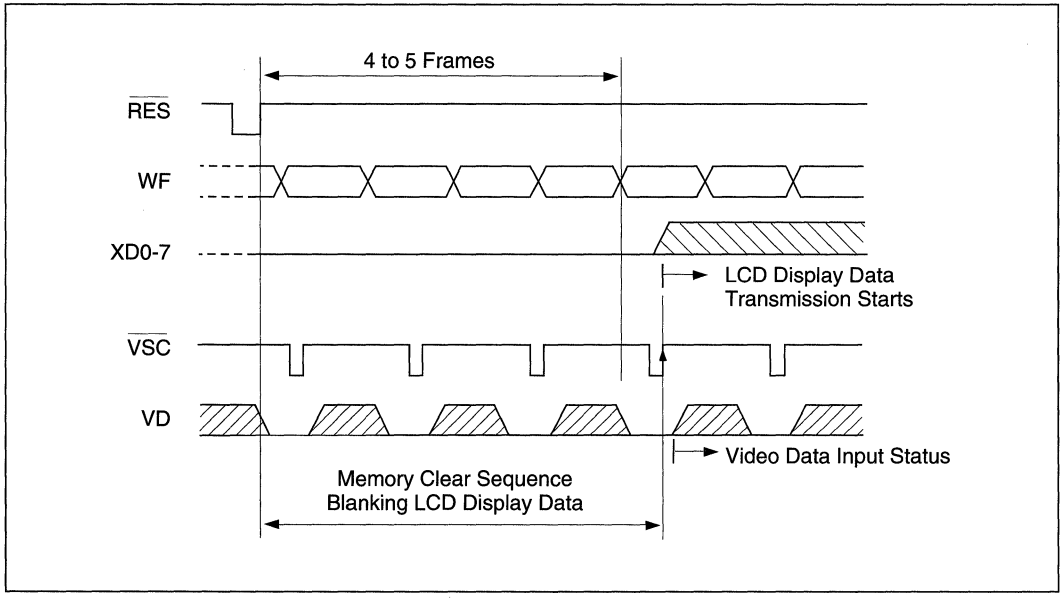
- **Power-On Clear Function**

VLI has an internal power-on clear function which prevents unusual display after power-on and random data display of buffer memory outside the display area.

The reset input makes the power-on clear function enable, and VLI performs as follows:

Clearing the frame buffer memory
Blanking the LCD display data

When the vertical sync signal, $\overline{VSC}$, is input after the four to five-frame time following the reset release, the power-on clear function is released, and ordinary display operation starts.



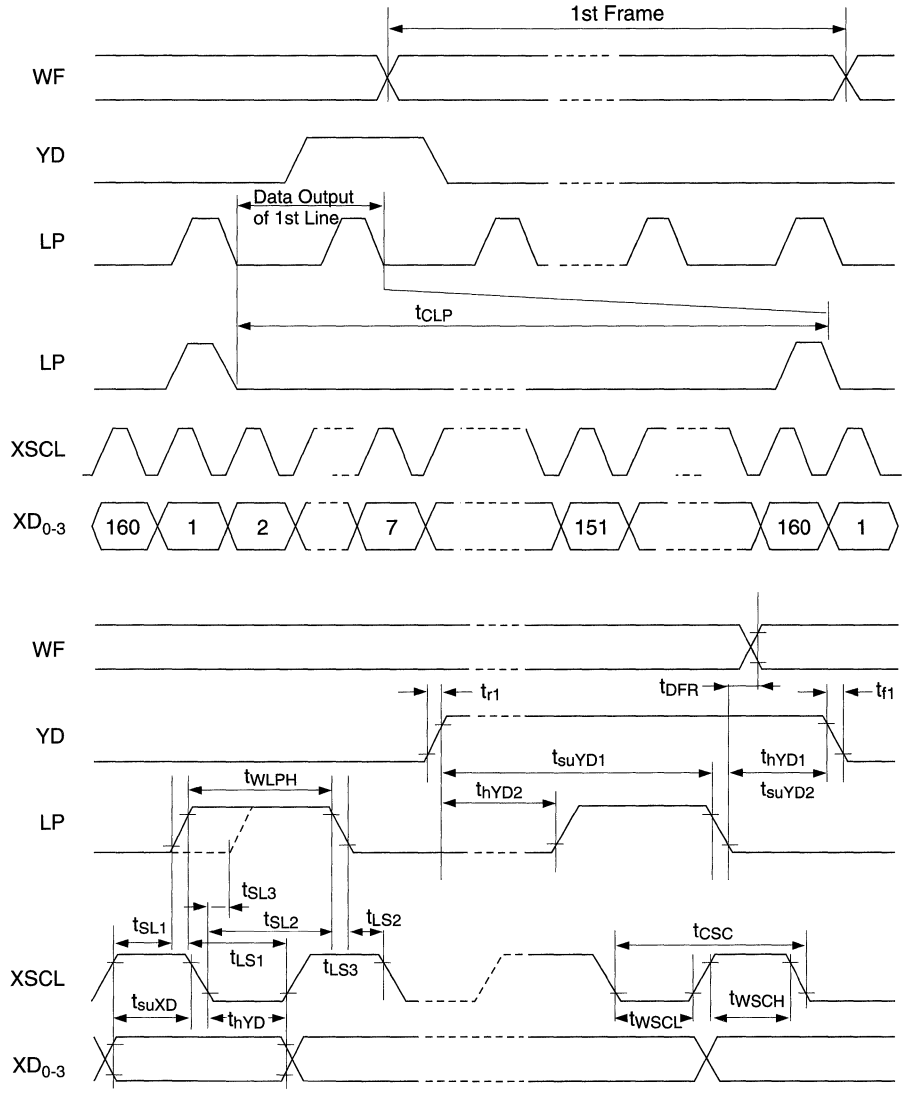
Power-on Waveforms

No video data, VD, is input during the memory clear sequence.

LCD-associated signals, such as shift clock, XSCL, and latch pulse LP are output during reset input.

● **AC CHARACTERISTICS**

○ **LCD Interface Timing Chart**



Note: "H" = $V_{DD} \times 0.8V$

"L" = $V_{DD} \times 0.2V$

Output Signal Reference Level

○ Oscillation, Output Rise Time, Output Fall Time

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Oscillation	t_{t1}		2.28•tcck and 89.2	—	3.6•tcck	ns
Output Rise Time	t_{tr1}	C=150pF	—	—	50	ns
Output Fall Time	t_{tf1}	C=150pF	—	—	50	ns

Note: t_{cck} is a cycle time of dot clock (t_{cck} = 1/fck)

○ X Driver

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition		Min*	Typ	Max	Unit
XSCL Cycle Time	t_{CSC}	SEL8 = "H"		2t1	—	—	ns
		SEL8 = "L"		4t1			
XSCL "H" Pulse Width	t_{WSCH}	SEL8 = "H"		t1–20	—	—	ns
		SEL8 = "L"		2t1–20			
XSCL "L" Pulse Width	t_{WSCL}	SEL8 = "H"		t1–20	—	—	ns
		SEL8 = "L"		2t1–20			
UD_{0-3}, $\overline{UD}_{0-3}$ Setup Time before XSCL	t_{SUXD}	SEL8 = "H"		t1–30	—	—	ns
		SEL8 = "L"		2t1–30			
UD_{0-3}, $\overline{UD}_{0-3}$ Setup Time after XSCL		SEL8 = "H"		t1–30	—	—	ns
		SEL8 = "L"		2t1–30			
XSCL to LP Time	t_{SL1}	SEL7 = "H"	SEL8 = "H"	0.5t1–30	—	—	ns
			SEL8 = "L"	t1–30			
XSCL to LP Time	t_{SL2}		SEL8 = "H"	t1–20	—	—	ns
			SEL8 = "L"	2t1–20			
LP to XSCL Time	t_{LS1}		SEL8 = "H"	1.5t1–50	—	—	ns
			SEL8 = "L"	3t1–50			
LP to XSCL Time	t_{LS2}		SEL8 = "H"	t1–20	—	—	ns
			SEL8 = "L"	2t1–20			
XSCL to LP Time	t_{SL3}	SEL7 = "L"	SEL8 = "H"	0.5t1–40	—	—	ns
			SEL8 = "L"	t1–40			
LP to XSCL Time	t_{LS3}		SEL8 = "H"	0.5t1–40	—	—	ns
			SEL8 = "L"	t1–40			
LP Cycle Time	t_{CLP}	SEL1 = "H"		320t1	—	—	ns
		SEL1 = "L"		640t1			
LP "H" Pulse Width	t_{WLPW}	SEL7 = "H"	SEL8 = "H"	1.5t1–50	—	—	ns
			SEL8 = "L"	3t1–50			
		SEL7 = "L"	SEL8 = "H"	t1–40	—	—	ns
			SEL8 = "L"	2t1–40			
WF Output Delay Time After LP1, LP2	t_{DFR}	—		—	—	100	ns

*t1 is an oscillation frequency of X'tal oscillation circuit (t1 = 1/f_{osc})

○ Y Driver

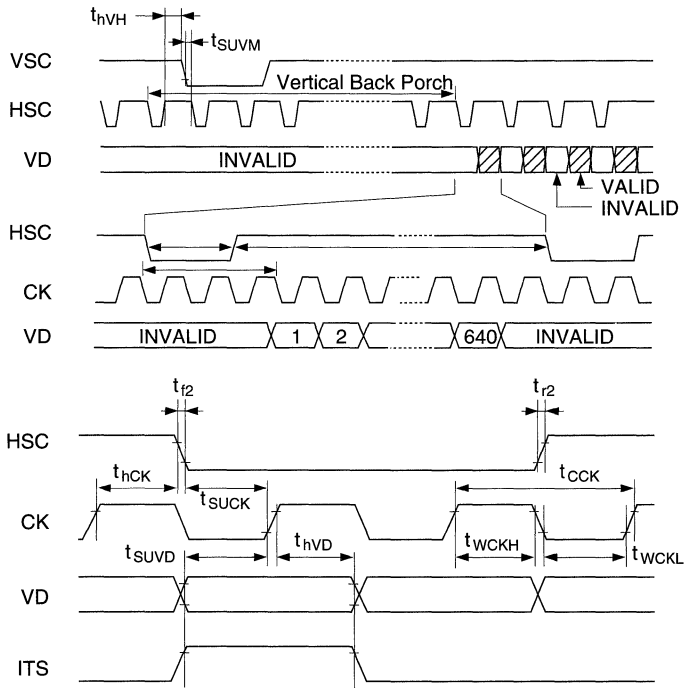
(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition			Min*	Typ	Max	Unit
YD Setup Time before LP, YSCL	t_{SUYD1}	SEL7 = "H"	SEL1 = "H"		142t1–100	—	—	ns
			SEL1 = "L"		302t1–100			
YD Hold Time after LP, YSCL	t_{hYD1}		SEL1 = "H"		18t1–100	—	—	ns
			SEL1 = "L"		18t1–10			
YD Setup Time before LP, YSCL	t_{SUYD2}	SEL7 = "L"	SEL1 = "H"	SEL8 = "H"	141.5t1–100	—	—	ns
				SEL8 = "L"	141t1–100			
			SEL1 = "L"	SEL8 = "H"	301.5t1–100			
				SEL8 = "L"	301t1–100			
YD Hold Time after LP, YSCL	t_{hYD2}		SEL1 = "H"	SEL8 = "H"	17.5t1–100	—	—	ns
				SEL8 = "L"	17t1–100			
			SEL1 = "L"	SEL8 = "H"	17.5t1–100			
				SEL8 = "L"	17t1–100			

*t1 is an oscillation frequency of X'tal oscillation circuit (t1 = 1/f_{osc})

○ Video Signal Interface

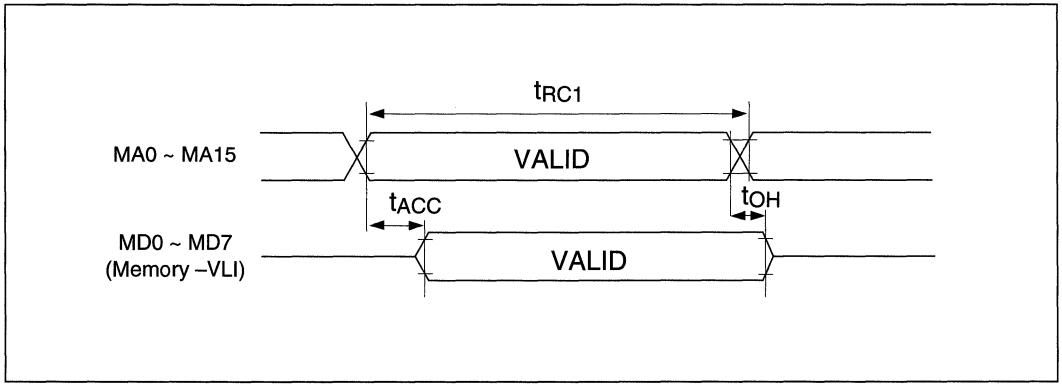
(When PL1 = "L", PL2 = "L", PL3 = "L")



(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CK Cycle Timer	t_{CCK}		29.4	—	—	ns
CK "H" Pulse Width	t_{WCKW}		12	—	—	ns
CK "L" Pulse Width	t_{WCKL}		12	—	—	ns
Input Rise Time	t_{r2}		—	—	5	ns
Input Fall Time	t_{f2}		—	—	5	ns
VD Setup Time Before CK	t_{SUVD}		16	—	—	ns
VD Hold Time After CK	t_{hVD}		2	—	—	ns
CK Setup Time Before HSC	t_{SUCK}		20	—	—	ns
CK Hold Time After HSC	t_{hCK}		0	—	—	ns
HSC Setup Time Before VSC	t_{SUVW}		80	—	—	ns
HSC Hold Time After VSC	t_{hUM}		0	—	—	ns

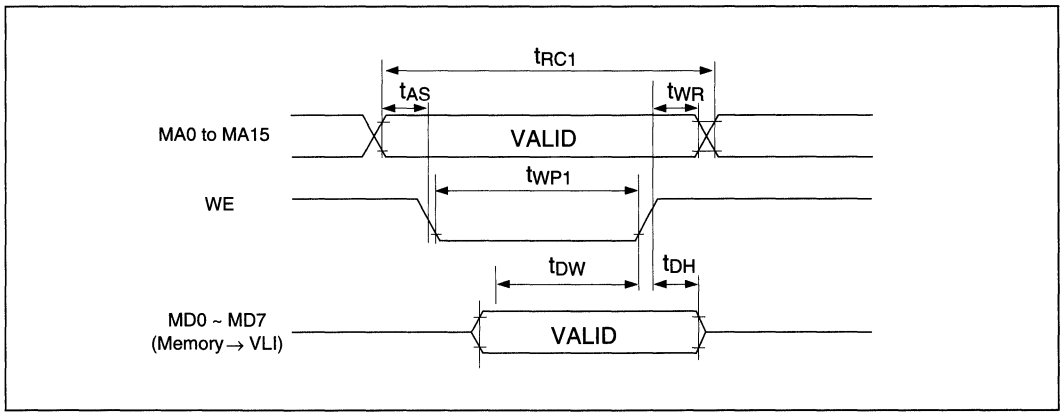
- **Memory Interface**
  - **Read Cycle**



(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Read Cycle Time	t_{RC1}		4t_{CCK}	—	—	ns
Address Access Time	t_{ACC}		—	—	4t_{CCK}–17	ns
Output Hold Time	t_{OH}		10	—	—	ns

○ **Write Cycle**



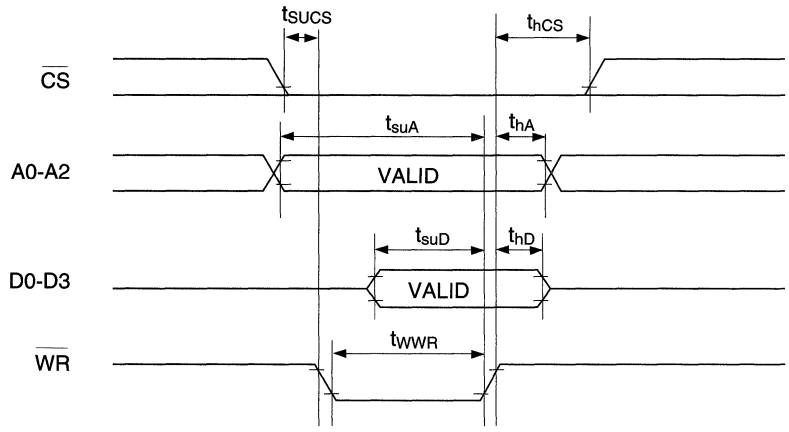
(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min*	Typ	Max	Unit
Write Cycle Time	t_{WC1}		4t_{CCK}	—	—	ns
Write Pulse Width	t_{WD1}		3t_{CCK}–13	—	—	ns
Address Setup Time	T_{AS}		0.5t_{CCK}–14	—	—	ns
Address Hold Time	t_{WR}		0.5t_{CCK}–14	—	—	ns
Data Setup Time	t_{DW}		3t_{CCK}–38	—	—	ns
Data Hold Time	t_{DH}		5	—	—	ns

Input, Output Signal Reference Level; "H" = 2.0V "L" = 0.8V

*t_{CCK} is a cycle time of Dot Clock (t_{CCK} = 1/f_{CK}).

- **Register Program**
  - **Write Method of MPU**

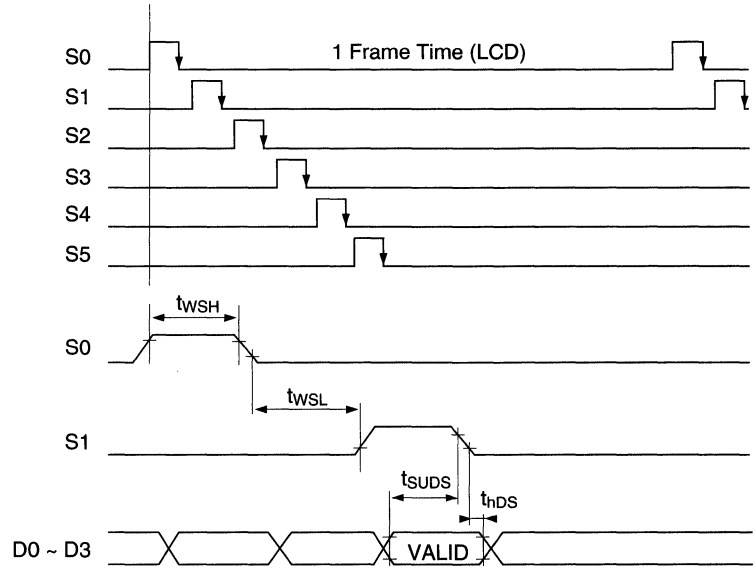


Input, Signal Reference Level; "H" = 2.0V "L" = 0.8V

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{CS}$ Setup Time	t_{SUCS}		10	—	—	ns
$\overline{CS}$ Hold Time	t_{hCS}		10	—	—	ns
A0–A2 Setup Time	t_{suA}		10	—	—	ns
A0–A2 Hold Time	t_{hA}		10	—	—	ns
D0–D3 Setup Time	t_{suD}		50	—	—	ns
D0–D3 Hold Time	t_{hD}		10	—	—	ns
Pulse Width	t_{WWR}		50	—	—	ns

● **Data Set Method By Digital Switch**



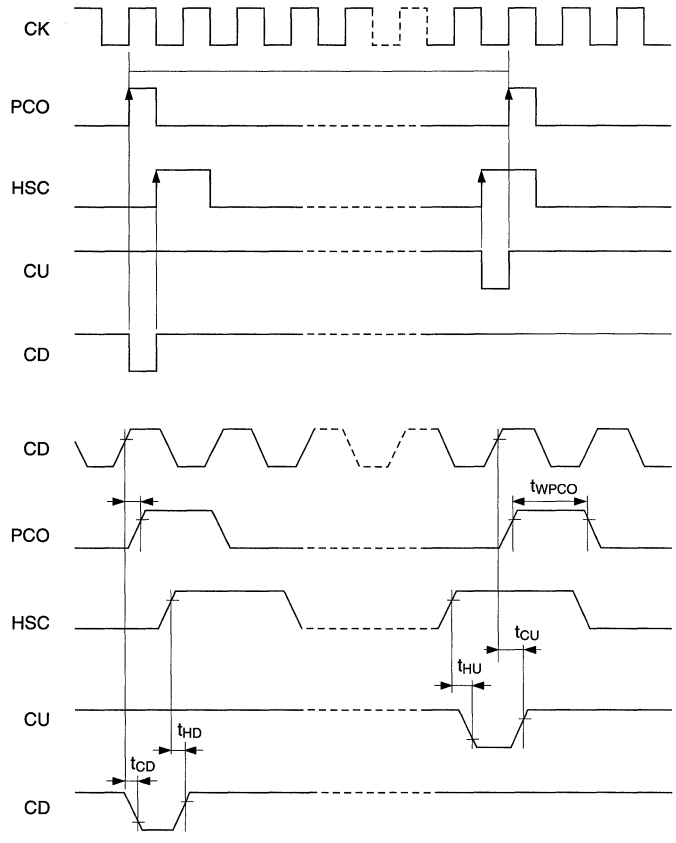
* Input Signal Reference Level; "H" = 2.0V "L" = 0.8V

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min*	Typ	Max	Unit
Scanning Signal "H" Pulse Width	t_{WSH}		8t1–150	—	—	ns
Scanning Signal "OFF" Width	t_{WSL}		8t1–150	—	—	ns
D0–D3 Setup Time	t_{SUDS}		100	—	—	ns
D0–D3 Hold Time	t_{hDS}		0	—	—	ns

*t1 is an oscillation frequency of X'tal oscillation circuit (t1 = 1/f_{osc})

● **PLL Interface**

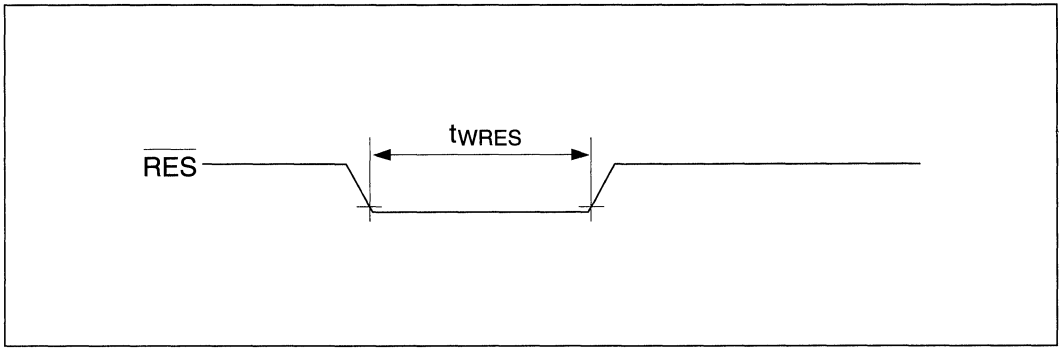


Input Signal Reference Level; "H" = 2.0V "L" = 0.8V

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{CU}$ "ON" Delay Time After HSC	t_{HU}	CL = 20pF	—	22	40	ns
$\overline{CU}$ "OFF" Delay Time After CK	t_{CU}	CL = 20pF	—	22	40	ns
$\overline{CU}$ "ON" Delay Time After CK	t_{CD}	CL = 20pF	—	22	40	ns
$\overline{CD}$ "OFF" Delay Time After HSC	t_{HD}	CL = 20pF	—	22	40	ns
PCO Delay Time After CK	t_{CPCD}	CL = 20pF	—	—	35	ns
PCO Pulse Width	t_{WPCO}	CL = 20pF	t_{CCK}–25	—	—	ns

● **Reset Input**

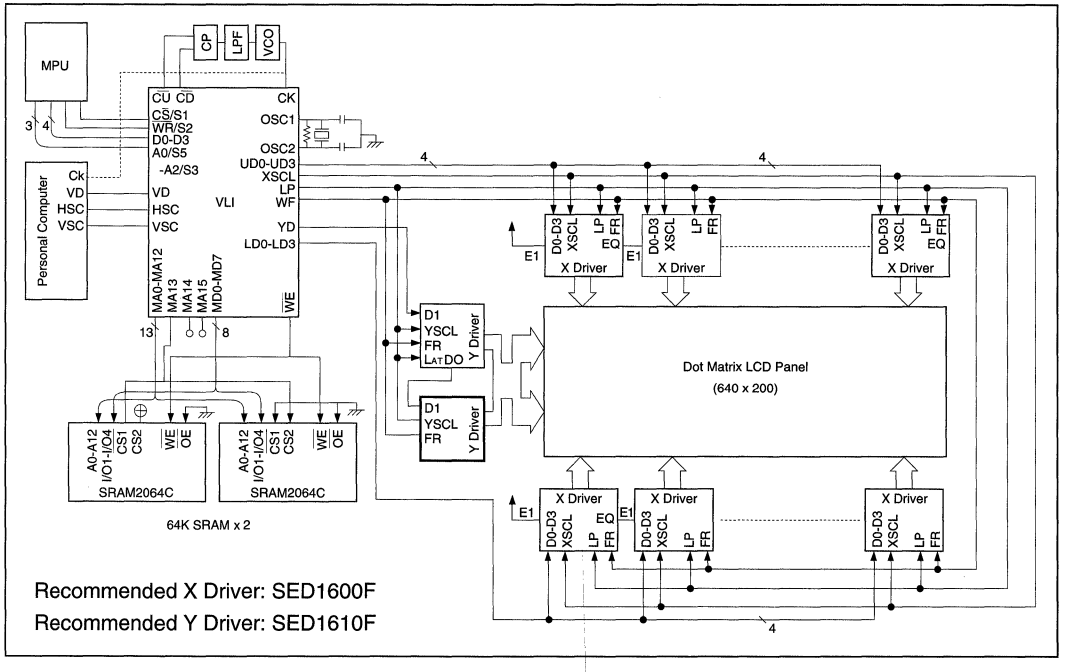


(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

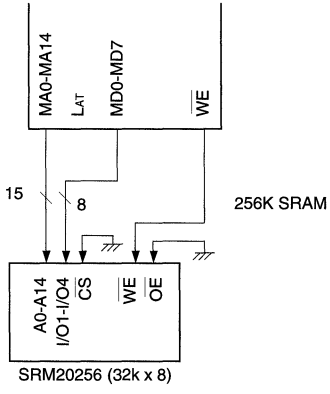
Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{RES}$ Pulse Width	tWRES		1.0	—	—	ns

Input Signal Reference Level; "H" = 2.0V "L" = 0.8V

■ EXAMPLE OF APPLICATION: 640 × 200 Dots, 4 bit 2-Bus, 2-Screen Operation

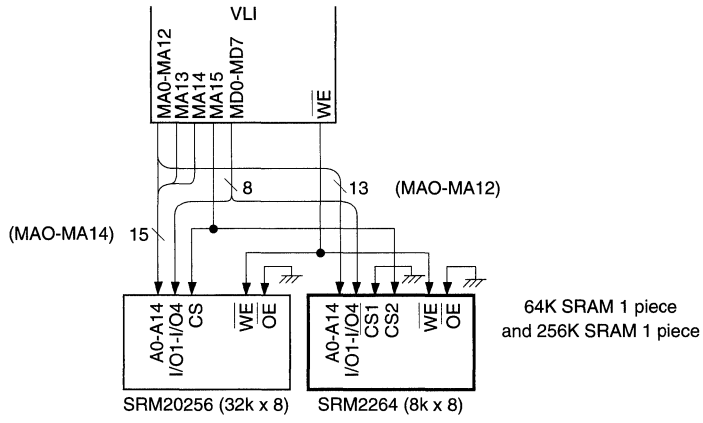


● 640 × 400 Dots/640 × 350 Dots Connecting to Memory



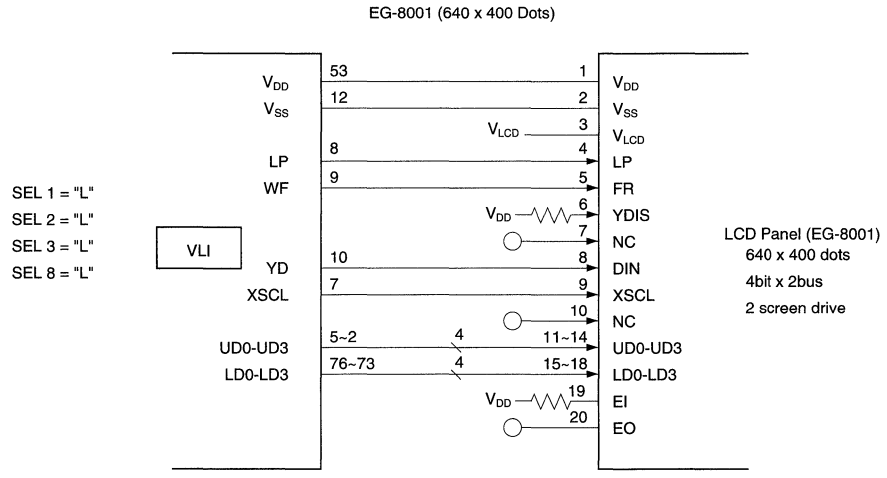
640 × 400 Dots/640 × 350 Dots Application Circuit

● 640 × 480 Dots Connecting to Memory



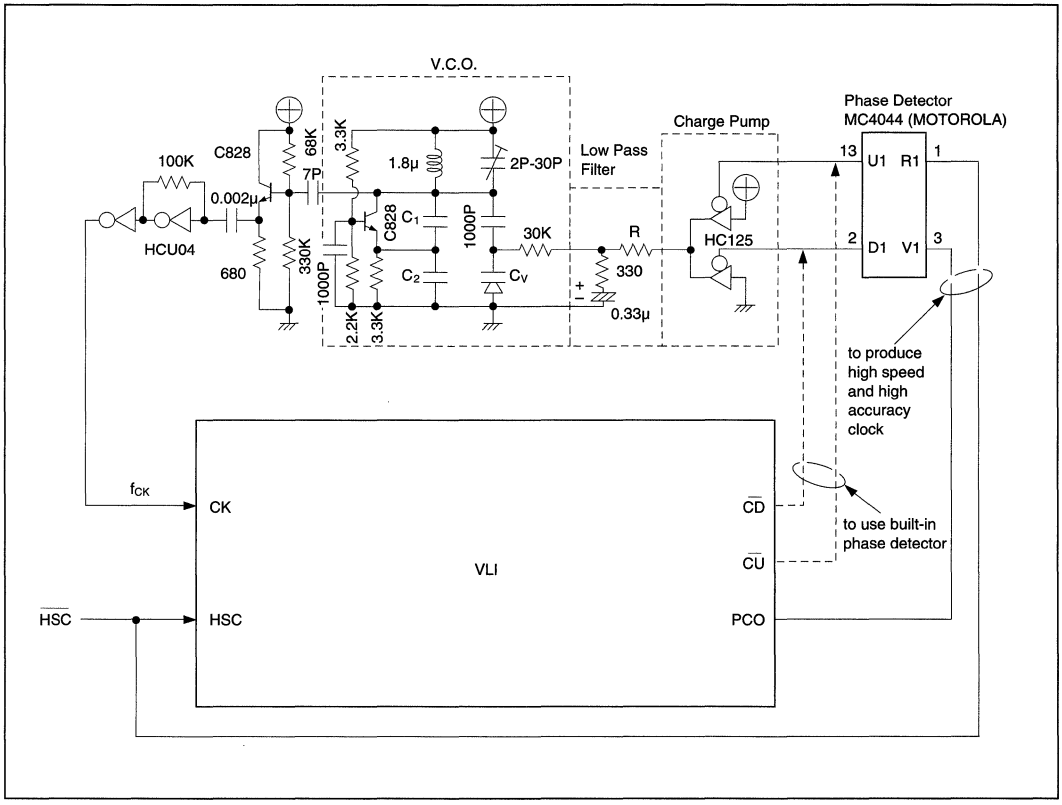
640 × 480 Application Circuit

● Example of LCD Module



LCD Interface Circuit

● Example of PLL Circuit



fCK	CU	C1	C2	R
14.3 MHz	1SV73(JRC)	22pF	30pF	330 Ω
21 MHz	1S2267 (Toshiba)	10pF	15pF	510 Ω

■ DIFFERENCES BETWEEN SED1341F0C and SED1341F0E

No.	Name	
	D1341F0C	D1341F0E
1	OSC2	OSC2
2	UD3	UD3
3	UD2	UD2
4	UD1	UD1
5	UD0	UD0
6	XECL	SEL13
7	XSCL	XSCL
8	LP1	LP
9	WF	WF
10	YD	YD
11	NU/LP2	YSCL
12	VSS	VSS
13	MD7	MD7
14	MD6	MD6
15	MD5	MD5
16	MD4	MD4
17	MD3	MD3
18	MD2	MD2
19	MD1	MD1
20	MD0	MD0
21	CAS	NU
22	WE	WE
23	NU	NU
24	SEL4	SEL4
25	RAS2	SEL11
26	RAS1	SEL12
27	MA14/MA15	MA15
28	MA14	MA14
29	MA13	MA13
30	MA12	MA12
31	MA11	MA11
32	MA10	MA10
33	MA9	MA9
34	MA8	MA8
35	MA7	MA7
36	MA6	MA6
37	MD5	MD5
38	MA4	MA4
39	MA3	MA3
40	MA2	MA2

No.	Name	
	D1341F0C	D1341F0E
41	MA1	MA1
42	MA0	MA0
43	NU/SEL9	SEL9
44	D3	D3
45	D2	D2
46	D1	D1
47	D0	D0
48	$\overline{CS}$/S1	$\overline{CS}$/S1
49	$\overline{WR}$/S2	$\overline{WR}$/S2
50	A2/S3	A2/S3
51	A1/S4	A1/S4
52	A0/S5	A0/S5
53	VDD	VDD
54	NU/S0	NU/S0
55	$\overline{RES}$	$\overline{RES}$
56	NU/ITS	SEL10
57	PCO	PCO
58	$\overline{CU}$	$\overline{CU}$
59	$\overline{CD}$	$\overline{CD}$
60	PL3	PL3
61	VSC	VSC
62	HSC	HSC
63	CK	CK
64	VD	VD
65	PL0	PL0
66	SEL3	SEL3
67	PL1	PL1
68	PL2	PL2
69	SEL5	SEL5
70	NU/SEL6	SEL6
71	NU/SEL7	SEL7
72	NU/SEL8	SEL8
73	NU/LD3	NU/LD3
74	NU/LD2	NU/LD2
75	NU/LD1	NU/LD1
76	NU/LD0	NU/LD0
77	$\overline{SEL}$	NU
78	SEL1	SEL1
79	SEL2	SEL2
80	OSC1	OSC1

NU = Not Used. NU terminals must be open since they are wired to individual IC chips in the package.

● Functional Comparison Table

Item	SED1341F0C	SED1341F0E
640 × 200	O	O
640 × 350	O	O
640 × 400	O	O
640 × 480	O	O
720 × 350	X	O
720 × 400	X	O
Automatic Centering Display	X	O
Automatic Horizontal Line Blanking	X	O
PLL Counter Dividing Ratio	1/706 to 1/961	1/514 to 1/1025
Frame Buffer Memory	SRAM/DRAM	SRAM
ITS (Half Tone) Display	O	X
XECL (X-Driver Enable Clock) (output)	O	X

O: Possible

X: Not Possible

CMOS VIDEO - LCD INTERFACE (VLI)

● **8 Levels of Gray Scale**

■ DESCRIPTION

The SED1345 is a video-LCD interface (VLI) developed for a dot matrix LCD display system. It converts separate video signals for CRT display into signals for LCD.

The SED1345 can use a conventional LCD driver to display data at eight gradation levels corresponding to digital video signal data I, R, G and B. The on-chip color pallet for gradation display allows setting of any gradation level for each of the 16 colors on the CRT display.

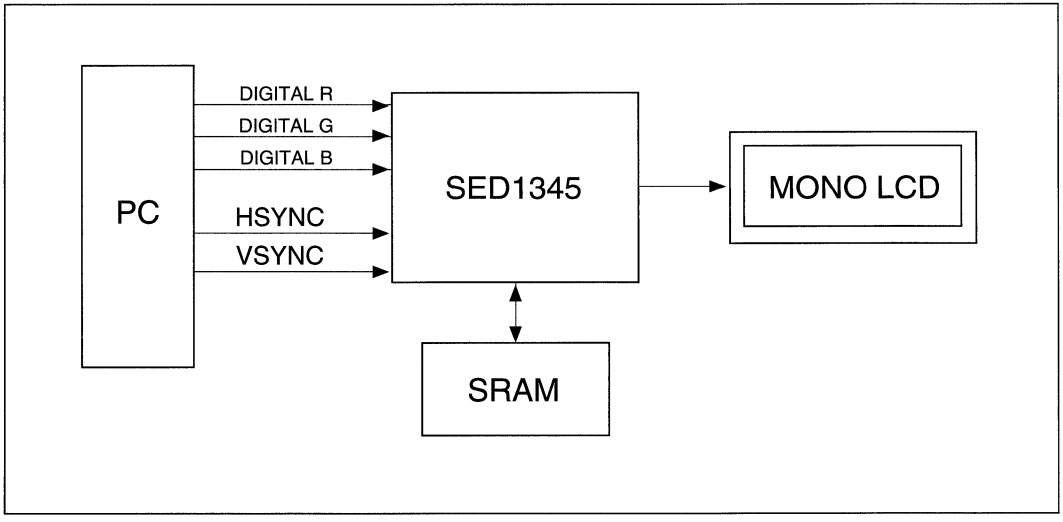
A 640 × 480 dot panel with eight gradation levels can be driven using only 256K bits of frame buffer memory. This leads to a significant reduction in system memory cost.

With the SED1345, the user can select not only a display size but a display area to configure a display panel of flexible size from 640 × 200 dots to 640 × 480 dots (maximum). These LCD display sizes are compatible with various display modes such as CGA® and EGA®.

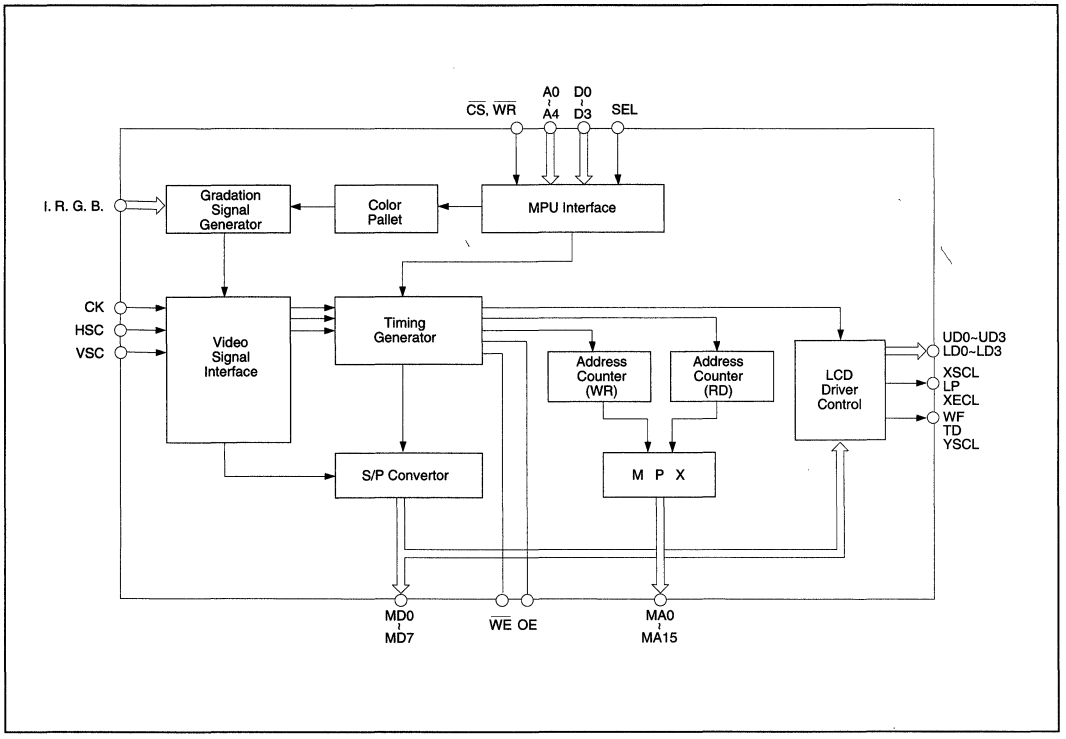
■ FEATURES

- Low-power CMOS technology
- TTL-compatible signal input
- LCD display size:
  Horizontal: ..... 640 dots
  Vertical: ..... 200, 350, 400, 480 lines
- Supports 8 levels of gray shade
- Supports single panel and dual panel
- LCD driver interface:4 bits bus and 4 bits × 2 bus
- Register programming by 4 bits
- Maximum dot clock: ..... 30 MHz
- Supports 40KB SRAM frame buffer
- Duty cycle: ..... 1/200 to 1/480
- Power-on clear function
- Single power supply: ..... 5V ± 5%
- Package: ..... QFP5-80 pin (FOA)

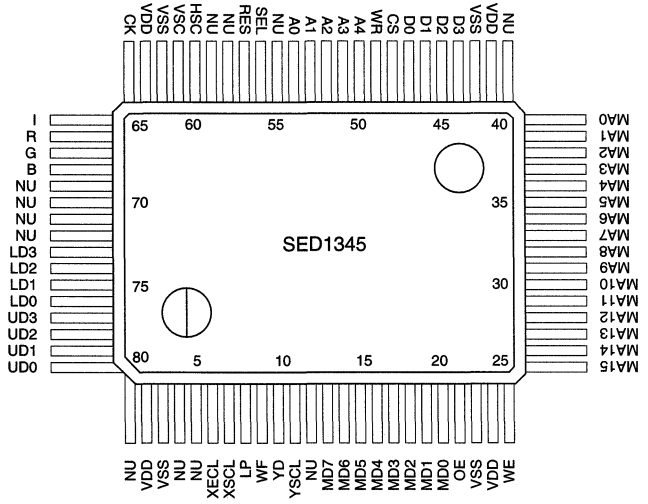
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN OUT



■ PIN OUT

No.	Name
1	NU
2	VDD
3	VSS
4	NU
5	NU
6	XECL
7	XSCL
8	LP
9	WF
10	YD
11	YSCL
12	NU
13	MD7
14	MD6
15	MD5
16	MD4
17	MD3
18	MD2
19	MD1
20	MD0

No.	Name
21	$\overline{OE}$
22	VSS
23	VDD
24	$\overline{WE}$
25	MA15
26	MA14
27	MA13
28	MA12
29	MA11
30	MA10
31	MA9
32	MA8
33	MA7
34	MA6
35	MA5
36	MA4
37	MA3
38	MA2
39	MA1
40	MA0

No.	Name
41	NU
42	VDD
43	VSS
44	D3
45	D2
46	D1
47	D0
48	$\overline{CS}$
49	$\overline{WR}$
50	A4
51	A3
52	A2
53	A1
54	A0
55	NU
56	SEL
57	$\overline{RES}$
58	NU
59	NU
60	HSC

No.	Name
61	VSC
62	VSS
63	VDD
64	CK
65	I
66	R
67	G
68	B
69	NU
70	NU
71	NU
72	NU
73	LD3
74	LD2
75	LD1
76	LD0
77	UD3
78	UD2
79	UD1
80	UD0

Note: NU = Pin is Not Used
The NU pin is wired to the IC chip inside the package, and must be held open.

■ PIN DESCRIPTION

Pin Name	Pin No.	Function
VDD	2, 23, 42, 63	+5V power
VSS	3, 22, 43, 62	GND
UD0 to UD3	80 to 77	Data bus output to X-driver
LD0 to LD3	76 to 73	Data bus output to X-driver
XSCL	7	Shift clock output to X-driver
LP	8	Latch pulse output
XECL	6	Enable shift clock output to X-driver
WF	9	LCD AC signal output
YD	10	Scanning start data output to Y-driver
YSCL	11	Shift clock output to Y-driver
I, R, G, B	65 to 68	Video data input
CK	64	Dot clock input
HSC	60	Horizontal sync signal input
VSC	61	Vertical sync signal input
MA0 to MA15	40 to 25	Address bus output to frame buffer memory
MD0 to MD7	20 to 13	Data bus input/output to frame buffer memory
$\overline{WE}$	24	Write enable signal output
$\overline{OE}$	21	Output enable signal output
D0 to D3	47 to 44	Data bus input for writing registers
A0 to A4	54 to 50	Address bus input/output for writing registers
$\overline{CS}$	48	Chip select signal input
$\overline{WR}$	49	Write signal input
SEL	56	Register write mode selection input (ROM/MPU)
$\overline{RES}$	57	Reset signal input

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Ratings	Unit
Supply Voltage	V_{DD}	Based on V_{SS}	–0.3 to 7.0	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	V
Output Voltage	V_D		–0.3 to V_{DD}+0.3	V
I/O Voltage	$V_{I/O}$		–0.3 to V_{DD}+0.3	V
Output Current/Pin	I_O		–10 to 10	mA
Power Dissipation	P_D		250	mW
Operating Temperature	T_{opr}		0 to 70	°C
Storage Temperature	T_{stg}		–65 to 150	°C
Soldering Temperature and Time	T_{sol}		260°C, 10s (at lead)	—

● Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		4.75	5.00	5.25	V

● DC Characteristics

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Average Operating Current Consumption	I_{opr}	fck=24MHz	—	—	40	mA
High Voltage Input Voltage 1	V_{IH1}	*1	2.0	—	V_{DD}+0.3	V
Low Level Input Voltage 1	V_{IL1}		–0.3	—	0.8	V
High Level Input Voltage 2	V_{IH2}	*2	4.0	—	V_{DD}+0.3	V
Low Level Input Voltage 2	V_{IL2}		–0.3	—	0.8	V
High Level Input Voltage 3	V_{IH3}	*3	3.0	—	V_{DD}+0.3	V
Low Level Input Voltage 3	V_{IL3}		–3.0	—	0.6	V
High Level Output Voltage	V_{OH}	I_{OH} = –2mA	4.35	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 6mA	—	—	0.4	V
Input Current Leakage	I_{LI}	VI = 0V to V_{DD}	–1	—	1	µA
I/O Current Leakage	$I_{LI/O}$	$V_{I/O}$ = 0V to V_{DD}	–1	—	1	µA

*1 Pad: I, R, G, B, CK, HSC, VSC, MD0 to MD7, A0 to A4, $\overline{CS}$, $\overline{WR}$

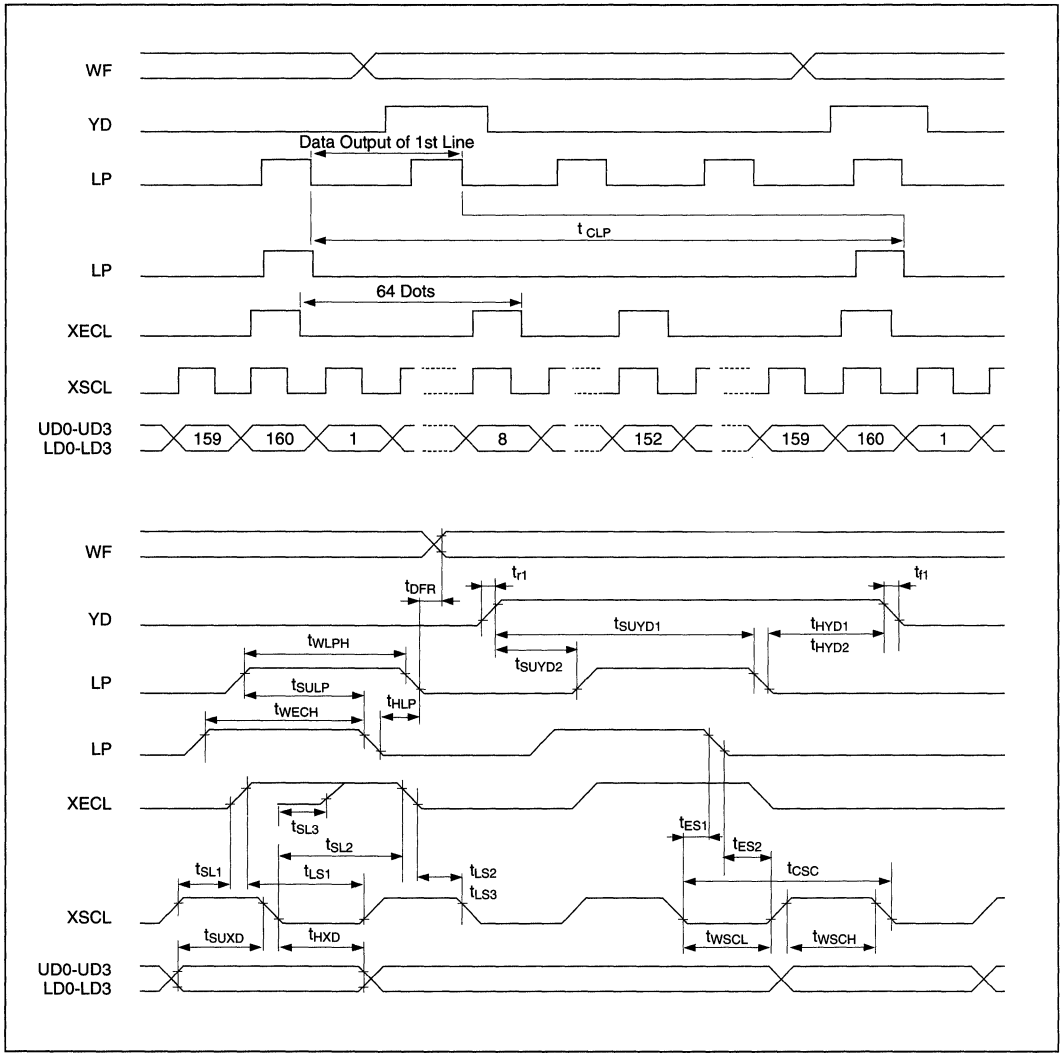
*2 Pad: D0 to D3, SEL

*3 Pad: $\overline{RES}$

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Rise Time	tri	CL = 150pF	—	—	50	ns
Output Fall Time	tfl	CL = 150pF	—	—	50	ns

- **AC CHARACTERISTICS**
  - **LCD Interface Timing Chart**



Output Signal Reference Level: "H" = $V_{DD} \times 0.8V$
"L" = $V_{DD} \times 0.2V$

○ **X Driver**

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
XSCL Cycle Time	t_{CSC}	S6 = "H"		2t1	—	—	ns
		S6 = "L"		4t1			
XSCL "H" Pulse Width	t_{WSCH}	S6 = "H"		t1–20	—	—	ns
		S6 = "L"		2t1–20			
XSCL "L" Pulse Width	t_{WSCL}	S6 = "H"		t1–20	—	—	ns
		S6 = "L"		2t1–20			
UD0–3, LD0–3 Setup Time before XSCL	t_{SUXD}	S6 = "H"		t1–30	—	—	ns
		S6 = "L"		2t1–30			
UD0–3, LD0–3 Hold Time after XSCL	t_{HXD}	S6 = "H"		21–30	—	—	ns
		S6 = "L"		2t1–30			
XSCL to LP Time	t_{SL1}	S5 = "H"	S6 = "H"	0.5t1–30	—	—	ns
			S6 = "L"	t1–30			
XSCL to LP Time	t_{SL2}		S6 = "H"	t1–20	—	—	ns
			S6 = "L"	2t1–20			
LP to XSCL Time	t_{LS1}		S6 = "H"	1.5t1–50	—	—	ns
			S6 = "L"	3t1–50			
LP to XSCL Time	t_{LS2}		S6 = "H"	t1–20	—	—	ns
			S6 = "L"	2t1–20			
XSCL to LP Time	t_{SL3}	S5 = "L"	S6 = "H"	0.5t1–40	—	—	ns
			S6 = "L"	t1–40			
LP to XSCL Time	t_{LS3}		S6 = "H"	0.5t1–40	—	—	ns
			S6 = "L"	t1–40			
LP Cycle Time	t_{CLP}	S0 = "H"		320t1	—	—	ns
		S0 = "L"		640t1			
LP, YSCL "H" Pulse Width	t_{WLPH}	S5 = "H"	S6 = "H"	1.5t1–50	—	—	ns
			S6 = "L"	3t1–50			
		S5 = "L"	S6 = "H"	t1–40	—	—	ns
			S6 = "L"	2t1–40			
LP Setup Time before XECL	t_{SULP}	S5 = "H", S6 = "H"		t1–50	—	—	ns
LP Hold Time after XECL	t_{HLP}	S5 = "H", S6 = "H"		0.5t1–40	—	—	ns
XSCL to XECL Time	t_{ES1}	S5 = "H", S6 = "H"		0.5t1–30	—	—	ns
XECL to XSCL Time	t_{ES2}	S5 = "H", S6 = "H"		0.5t1–40	—	—	ns
XECL "H" Pulse Width	t_{WECH}	S5 = "H", S6 = "H"		1.5t1–50	—	—	ns
WF Output Delay Time After LP, YSCL	t_{DFR}	S5 = "H", S6 = "H"		—	—	100	ns

t1 = 2t_{CCK} (t_{CCK} = dot clock cycle)

○ **Y Driver**

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition			Min*	Typ	Max	Unit
YD Setup Time before LP, YSCL	t_{SUYD1}	S5 = "H"	S0 = "H"		142t1–100	—	—	ns
			S0 = "L"		302t1–100			
YD Hold Time after LP, YSCL	t_{hYD1}	S5 = "H"	S0 = "H"		18t1–100	—	—	ns
			S0 = "L"		18t1–100			
YD Setup Time before LP, YSCL	t_{SUYD2}	S5 = "L"	S0 = "H"	S6 = "H"	141.5t1–100	—	—	ns
				S6 = "L"	141t1–100			
			S0 = "L"	S6 = "H"	301.5t1–100			
				S6 = "L"	301t1–100			
YD Hold Time after LP, YSCL	t_{HYD2}		S0 = "H"	S6 = "H"	17.5t1–100	—	—	ns
				S6 = "L"	17t1–100			
			S0 = "L"	S6 = "H"	17.5t1–100			
				S6 = "L"	17t1–100			

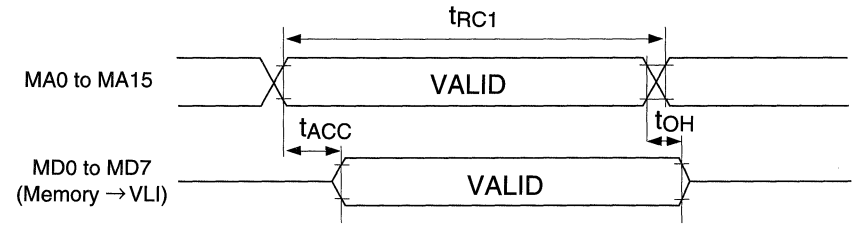
t1=2t_{CCK} (t_{CCK} = dot clock cycle)

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CK Cycle Time	t_{CCK}		33	—	—	ns
CK "H" Pulse Width	t_{WCKW}		12	—	—	ns
CK "L" Pulse Width	t_{WCKL}		12	—	—	ns
Input Rise Time	t_{r2}		—	—	5	ns
Input Fall Time	t_{f2}		—	—	5	ns
VD Setup Time Before CK	t_{SUVD}		16	—	—	ns
VD Hold Time After CK	t_{HVD}		2	—	—	ns
CK Setup Time Before HSC	t_{SUCK}		20	—	—	ns
CK Hold Time After HSC	t_{HCK}		0	—	—	ns
HSC Setup Time Before VSC	t_{SUVH}		80	—	—	ns
HSC Hold Time After VSC	t_{HVM}		0	—	—	ns
Active Pulse Width HSC	t_{WH1}		8t_{CCK}	—	—	ns
Non-Active Pulse Width HSC	t_{WH2}		64t_{CCK}	—	—	ns

● **Memory Interface**
○ **Read Cycle**

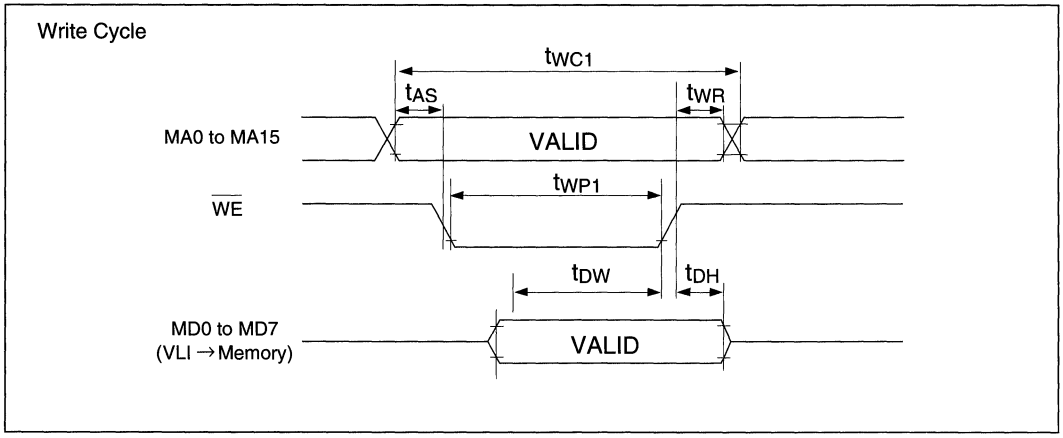
SRAM Read Cycle



(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Read Cycle Time	t_{RC1}		4t_{CCK}	—	—	ns
Address Access Time	t_{ACC}		—	—	4t_{CCK}–17	ns
Output Hold Time	t_{OH}		10	—	—	ns

○ **Write Cycle**



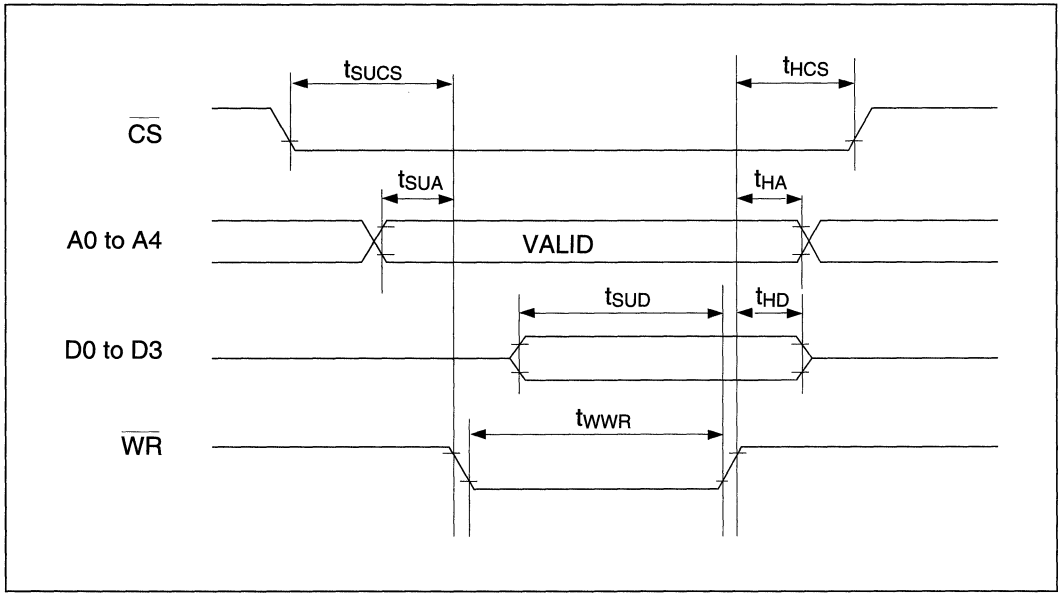
(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min*	Typ	Max	Unit
Write Cycle Time	t_{WC1}		4t_{CCK}	—	—	ns
Write Pulse Width	t_{WP1}		3t_{CCK}–13	—	—	ns
Address Setup Time	t_{AS}		0.5t_{CCK}–14	—	—	ns
Address Hold Time	t_{WR}		0.5t_{CCK}–14	—	—	ns
Data Setup Time	t_{DW}		3t_{CCK}–38	—	—	ns
Data Hold Time	t_{DH}		5	—	—	ns

Input/Output Signal Reference Level: "H" = 2.0V "L" = 0.8V

*t_{CCK} is the cycle time of dot clock (t_{CCK} = 1/f_{CK}).

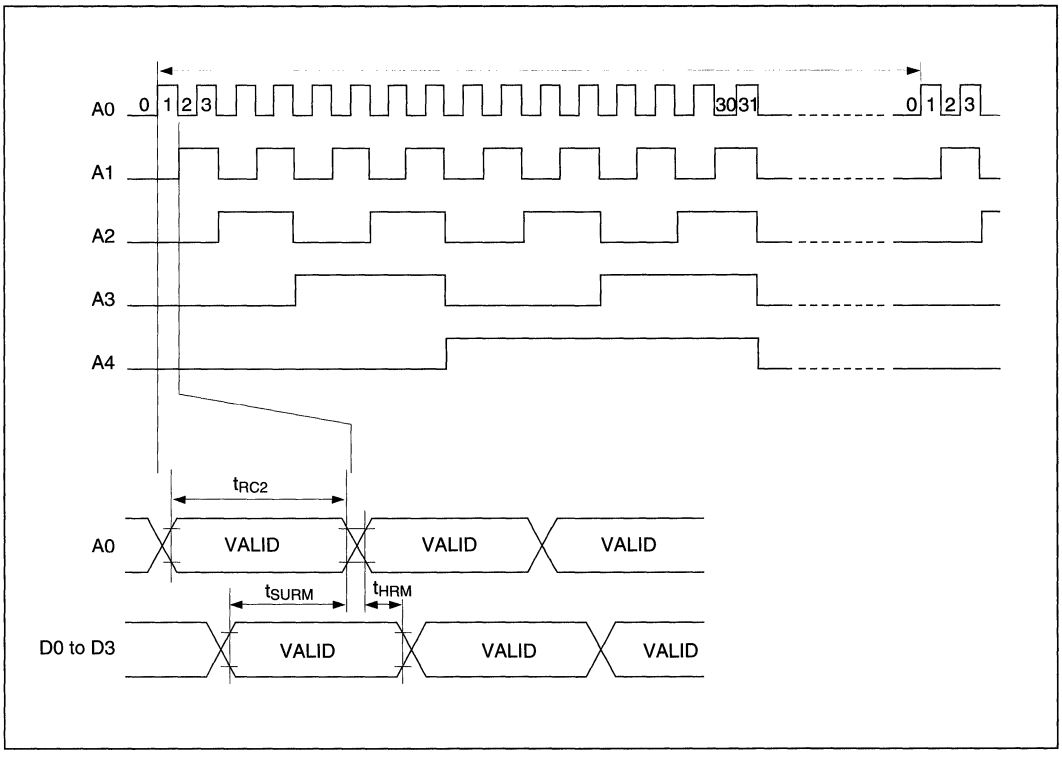
- **Register Program**
  - Write Data Using MPU



(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{CS}$ Setup Time	t_{SUCS}		50	—	—	ns
$\overline{CS}$ Hold Time	t_{HCSH}		50	—	—	ns
A0–A4 Setup Time	t_{SUA}		50	—	—	ns
A0–A4 Hold Time	t_{HA}		50	—	—	ns
D0–D3 Setup Time	t_{SUD}		100	—	—	ns
D0–D3 Hold Time	t_{HD}		50	—	—	ns
$\overline{WR}$ Pulse Width	t_{WWR}		50	—	—	ns

● **Write Data Using ROM**



Input/output signal level identification voltages:

"H" level – 2.0V

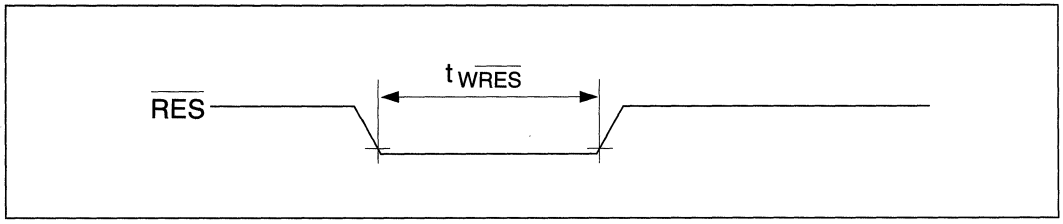
"L" level – 0.8V

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min*	Typ	Max	Unit
ROM Read Cycle Time	t_{RC2}		8t1–100	—	—	ns
D0 to D3 Setup Time	t_{SURM}		100	—	—	ns
D0 to D3 Hold Time	t_{HRM}		10	—	—	ns

* t1=2t_{CCK} (t_{CCK} is a cycle time of dot clock)

● Reset Input



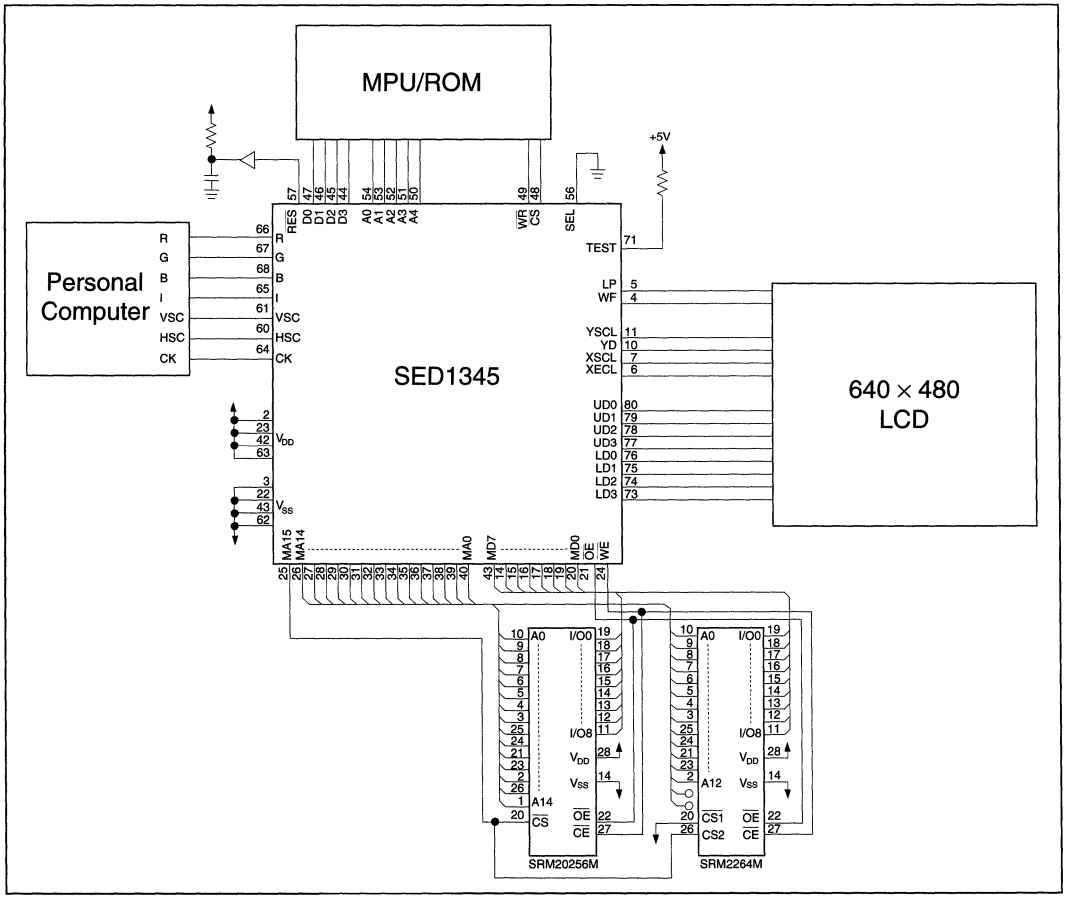
(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{RES}$ Pulse Width	$tw_{\overline{RES}}$		1.0	—	—	ns

Input signal reference level: "H" = 2.0V "L" = 0.8V

t_{CCK} is a cycle time of dot clock (t_{CCK} = 1/f_{CK})

● System Configuration



GRAPHICS LCD CONTROLLER

■ DESCRIPTION

The SED1351F is a graphics LCD controller capable of controlling medium to large resolution displays. It transfers data from MPU to external frame buffer RAM and converts this data to display signals for LCD drivers. The SED1351F can display images with 4 gray shades and support display duty cycle as high as 1/1024.

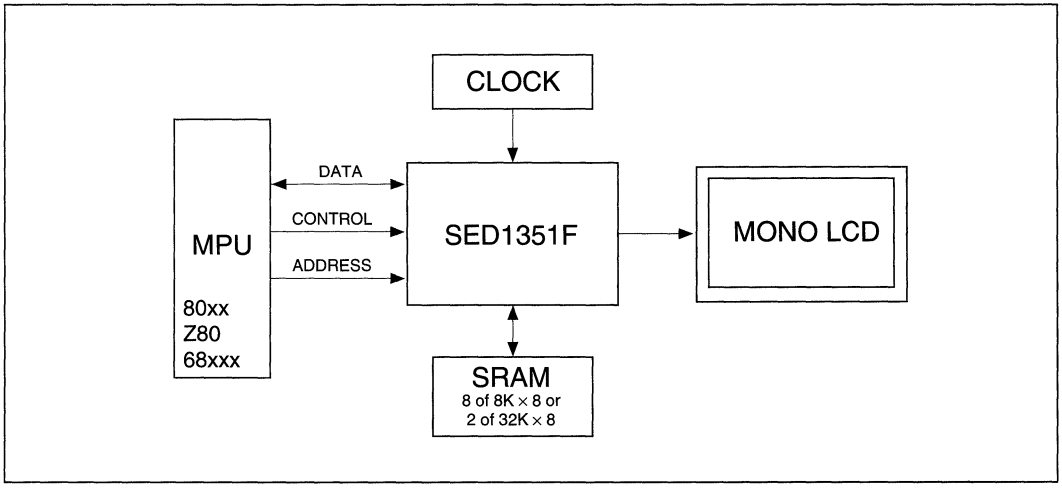
The SED1351F is designed to achieve high efficiency and data throughput to the LCD. It has a cycle steal mode which allows MPU to access frame buffer RAM without interfering with the display operation. The SED1351F can directly interface with up to eight 64K-bit SRAMs or two 256K-bit SRAMs.

The SED1351F can operate with either 5V or 3V power supply. The 5V version chip is the SED1351F0A and the 3V version chip is the SED1351FLB.

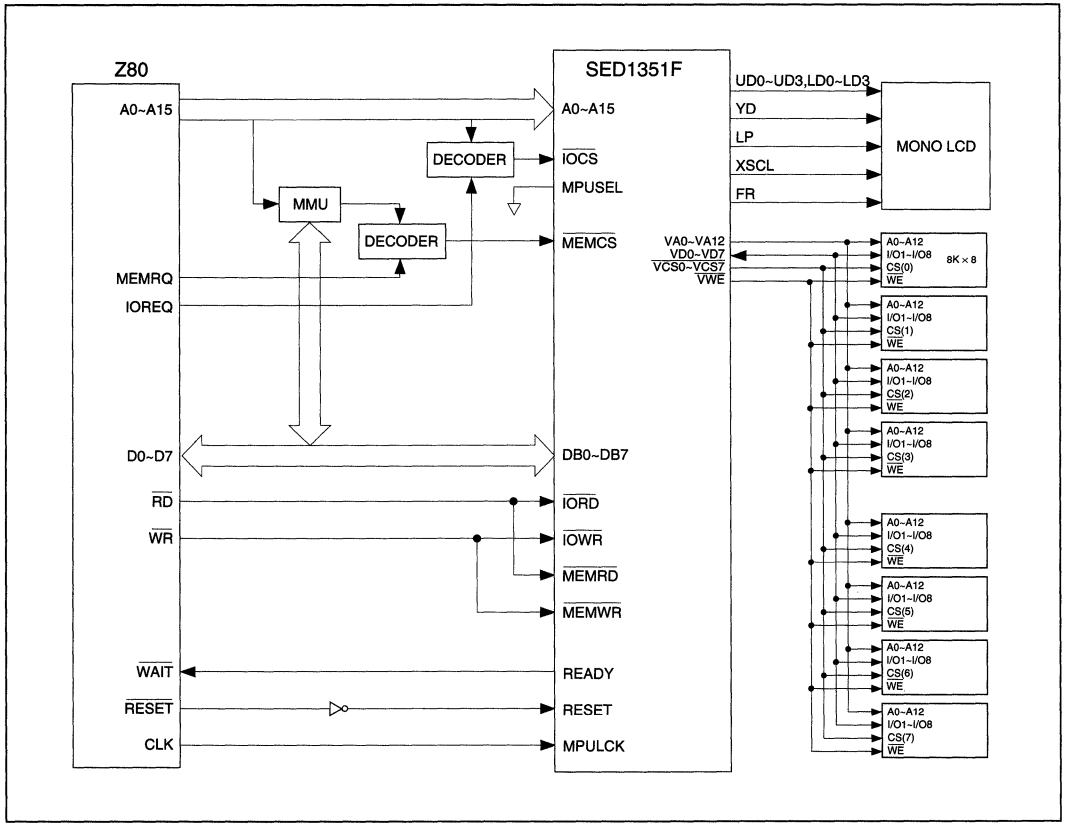
■ FEATURES

- Low-power CMOS technology
- 8-bit or 16-bit MPU data interface
- Direct interface with 80xx, Z80 and 68xxx MPU
- 4- or 8-bit panel data bus for single panel and 4-bit bus for dual panel
- Support logical OR of layers and panel division
- Smooth vertical scrolling
- Virtual screen display up to 1024
- Binary mode (on/off only) generates black & white images
- Gray mode (on/off and two gray steps) generates images with 4 gray shades
- Maximum number of rows
  Binary mode 2048
  Gray mode 1024
- Maximum number of rows:
  Single panel 1024
  Dual panel 2048
- Maximum display sizes when 64K-byte SRAMs are used:
  Binary mode ..... 2048 × 256 / 1024 × 512
  Gray mode ..... 1024 × 256 / 512 × 512
- Available models:
  $SED1351F_{0A}$ ..... 5V, QFP5-100 pin
  $SED1351F_{LB}$ ..... 3V,QFP15-100 pin

■ SYSTEM BLOCK DIAGRAM

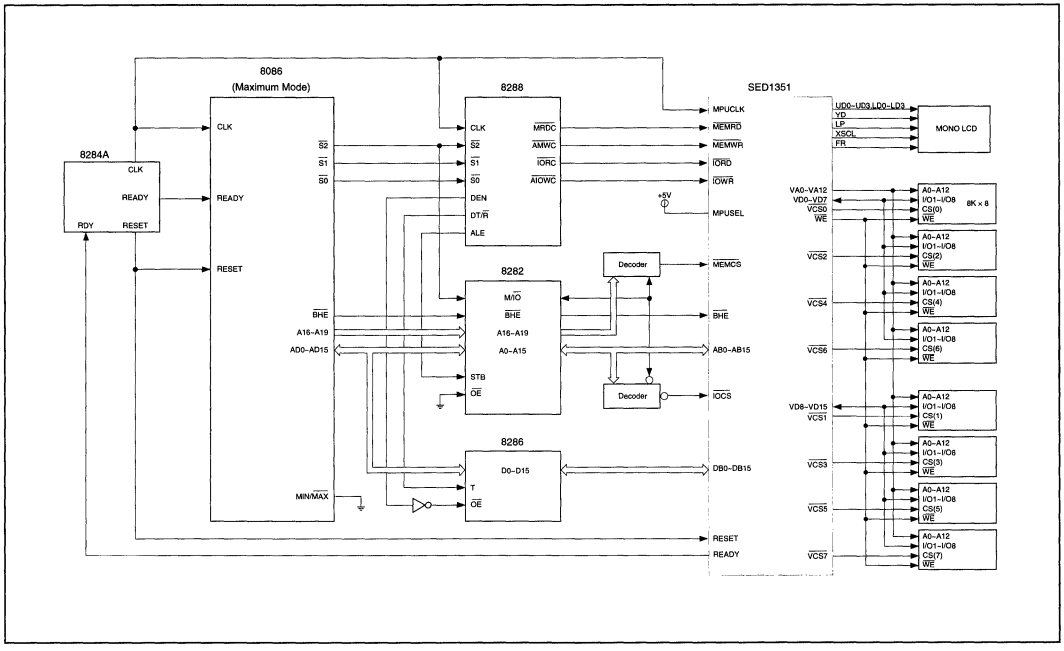


■ INTERFACE WITH 8-BIT MPU (Z-80) AND 64K-BIT SRAM (8 of 8K x 8)



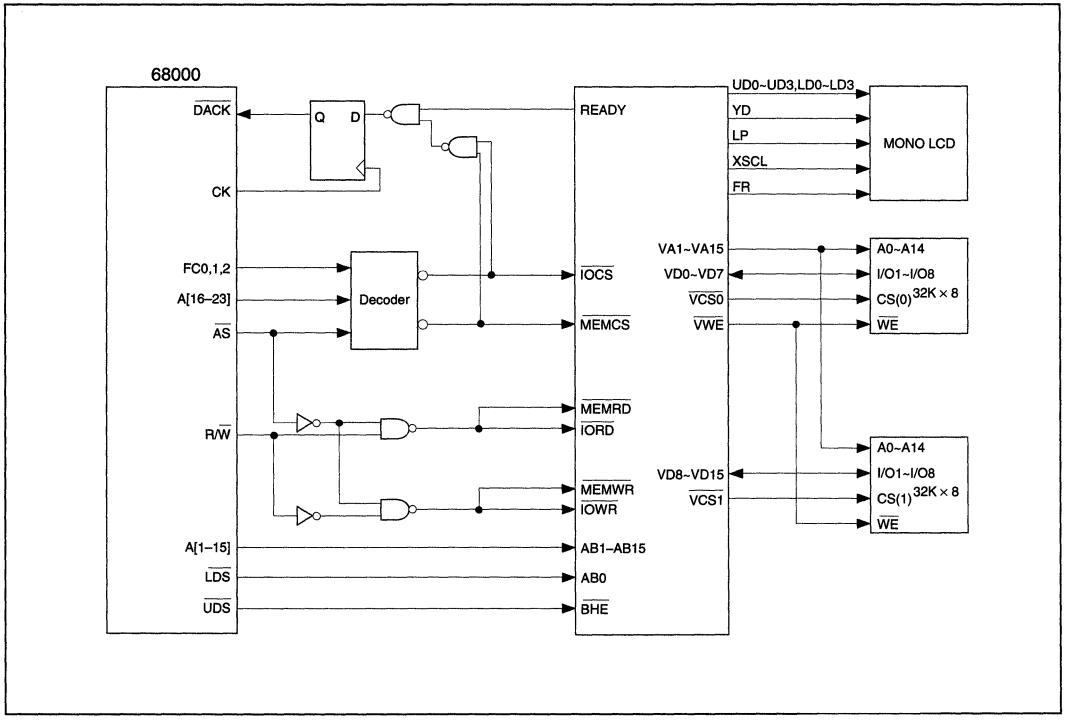
Note: Example implementation, actual may vary.

■ INTERFACE WITH 16-BIT MPU (8086) AND 64K-BIT SRAM (8 of 8K x 8)



Note: Example implementation, actual may vary.

■ INTERFACE WITH 16-BIT MPU (68000) AND 256K-BIT SRAM (2 of 32K x 8)

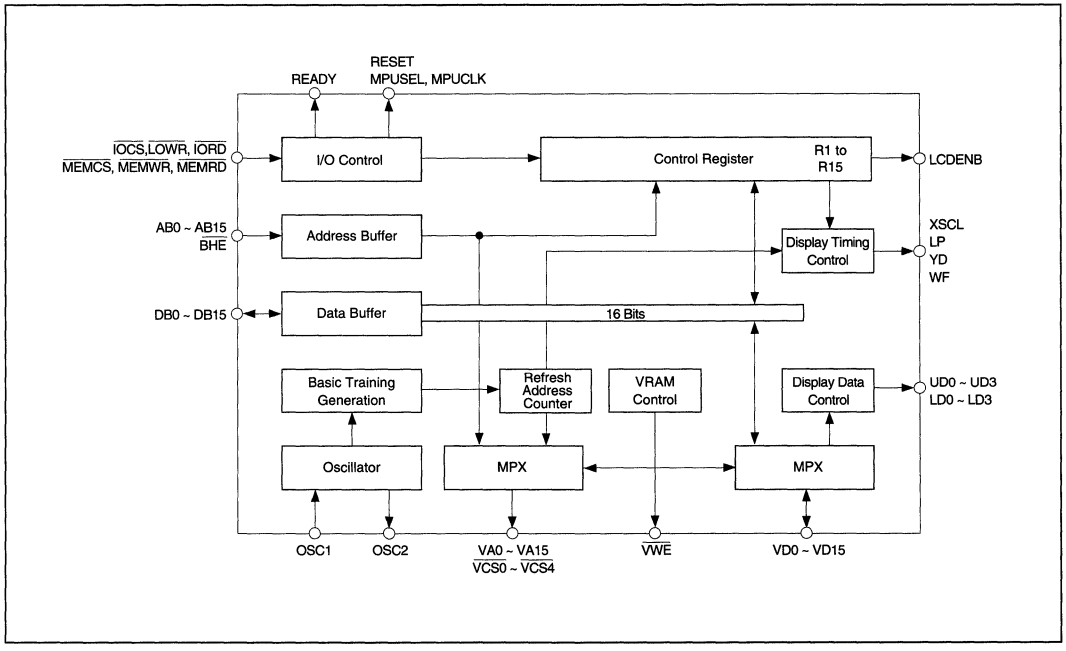


Note: Example implementation, actual may vary.

■ SUPPORTED RESOLUTIONS

Display RAM	Maximum Display Size				SRAM Type	CPU Interface	SRAM Interface
	Monochrome		4 Grayscale				
	X	Y	X	Y			
8K	256	256	256	128	1 of 8K × 8	8 bit	8 bit
16K	512	256	256	256	2 of 8K × 8	8 bit 16 bit	8 bit 16 bit
24K	512	384	384	256	3 of 8K × 8	8 bit	8 bit
32K	512	512	512	256	4 of 8K × 8	8 bit 16 bit	8 bit 16 bit
					1 of 32K × 8	8 bit	8 bit
48K	768	512	512	384	6 of 8K × 8	8 bit 16 bit	8 bit 16 bit
56K	896	512	512	448	7 of 8K × 8	8 bit	8 bit
64K	1024	512	512	512	8 of 8K × 8	8 bit 16 bit	8 bit 16 bit
					2 of 32K × 8	8 bit 16 bit	8 bit 16 bit

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS

● SED1351F0A

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	V_{SS}–0.3 to 7.0	V
Input voltage	V_I	V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage	V_O	V_{SS}–0.3 to V_{DD}+0.3	V
Output current/pin	I_O	±10	mA
Power dissipation	P_D	200	mW
Supply current	I_{DD}/I_{SS}	±40	mA
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

● Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_I		V_{SS}	—	V_{DD}	V
Operating temperature	T_{opr}		–20	—	75	°C

○ DC Characteristics (F0A)

(Ta = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static current	I_{DDS}	$V_{IN} = V_{DD}$, V_{DD} = Max, V_{SS}, $I_{OH} = I_{OL} = 0$	—	—	100	μA
Input leakage current (Type 1)	I_{LI}	V_{DD} = 5.5V, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	–10	—	10	μA
High level input voltage 1 (OSC1)	V_{IH1}	V_{DD} = 5.5V	3.5	—	—	V
Low level input voltage 1 (OSC1)	V_{IL1}	V_{DD} = 4.5V	—	—	1.0	V
High level input voltage 2 (Type 2)	V_{IH2}	V_{DD} = 5.5V	2.0	—	—	V
Low level input voltage 2 (Type 2)	V_{IL2}	V_{DD} = 4.5V	—	—	0.8	V
High level input voltage 3 (Type 3)	V_{T+}	V_{DD} = 5.5V	4.0	—	—	V
Low level input voltage 3 (Type 3)	V_{T-}	V_{DD} = 4.5V	—	—	0.8	V
Hysteresis voltage (Type 3)	V_H	V_{DD} = 5V	0.3	—	—	V
High level output voltage 1 (Type 4)	V_{OH1}	V_{DD} = 4.5V, I_{OH} = –2mA, I_{OL} = 6mA	V_{DD} – 0.4	—	—	V
Low level output voltage 1 (Type 4)	V_{OL1}		—	—	V_{SS} + 0.4	V
High level output voltage 2 (OSC2)	V_{OH2}	V_{DD} = 4.5V, I_{OH} = –50μA, I_{OL} = 50μA	V_{DD} – 0.4	—	—	V
Low level output voltage 2 (OSC2)	V_{OL2}		—	—	V_{SS} + 0.4	V

Note:

Type 1. $\overline{MEMCS}$, $\overline{MEMWR}$, $\overline{MEMRD}$, $\overline{IOCS}$, $\overline{IOWR}$, $\overline{IORD}$, MPUCLK, AB0 ~ AB15, $\overline{BHE}$, MPUSEL, RESET, OSC

Type 2. $\overline{MEMCS}$, $\overline{MEMWR}$, $\overline{MEMRD}$, $\overline{IOCS}$, $\overline{IOWR}$, $\overline{IORD}$, MPUCLK, AB0 ~ AB15, $\overline{BHE}$, DB0 ~ DB15, VD0 ~ VD15

Type 3. MPUSEL, RESET

Type 4. DB0 ~ DB15, READY, VA0 ~ VA15, $\overline{VCS0}$ ~ $\overline{VCS4}$, VD0 ~ VD15, $\overline{VWE}$, XSCL, LP, WF, YD, UD0 ~ UD3, LD0 ~ LD3, LCDENB

- **SED1351FLA**
- **Absolute Maximum Ratings**

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	V_{SS}–0.3 to 7.0	V
Input voltage	V_I	V_{SS}–0.3 to V_{DD}+0.5	V
Output voltage	V_O	V_{SS}–0.3 to V_{DD}+0.5	V
Output current/pin	I_O	±24	mA
Power dissipation	P_D	200	mW
Supply current	I_{DD}/I_{SS}	±40	mA
Storage temperature	T_{stg}	–65 to 150	°C

- **Recommended Operating Conditions**

(V_{SS} = 0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		2.7	—	3.6	V
Input voltage	V_I		V_{SS}	—	V_{DD}	V
Operating temperature	T_{opr}		–20	—	75	°C

○ DC Characteristics (FLB)

(Ta = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static current	I_{DDS}	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = MAX, $I_{OH} = I_{OL} = 0$	—	—	30	μA
Input leakage current (Type 1)	I_L	V_{DD} = MAX, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	–1	—	1	μA
High level input voltage 1 (OSC1)	V_{IH1}	V_{DD} = MAX	0.7V_{DD}	—	—	V
Low level input voltage 1 (OSC1)	V_{IL1}	V_{DD} = MIN	—	—	0.2V_{DD}	V
High level input voltage 2 (Type 2)	V_{IH2}	V_{DD} = MAX	0.7V_{DD}	—	—	V
Low level input voltage 2 (Type 2)	V_{IL2}	V_{DD} = MIN	—	—	0.2V_{DD}	V
High level input voltage 3 (Type 3)	V_{T+}	V_{DD} = MAX	0.8V_{DD}	—	—	V
Low level input voltage 3 (Type 3)	V_{T-}	V_{DD} = MIN	—	—	0.2V_{DD}	V
Hysteresis voltage (Type 3)	V_H	V_{DD} = TYP	0.3	—	—	V
High level output voltage 1 (Type 4)	V_{OH1}	V_{DD} = MIN, I_{OH} = –1.5mA, I_{OL} = 3mA	V_{DD} – 0.3	—	—	V
Low level output voltage 1 (Type 4)	V_{OL1}		—	—	V_{SS} + 0.3	V
High level output voltage 2 (OSC2)	V_{OH2}	V_{DD} = MIN, I_{OH} = –50μA, I_{OL} = 50μA	V_{DD} – 0.4	—	—	V
Low level output voltage 2 (OSC2)	V_{OL2}		—	—	V_{SS} + 0.4	V

Note:

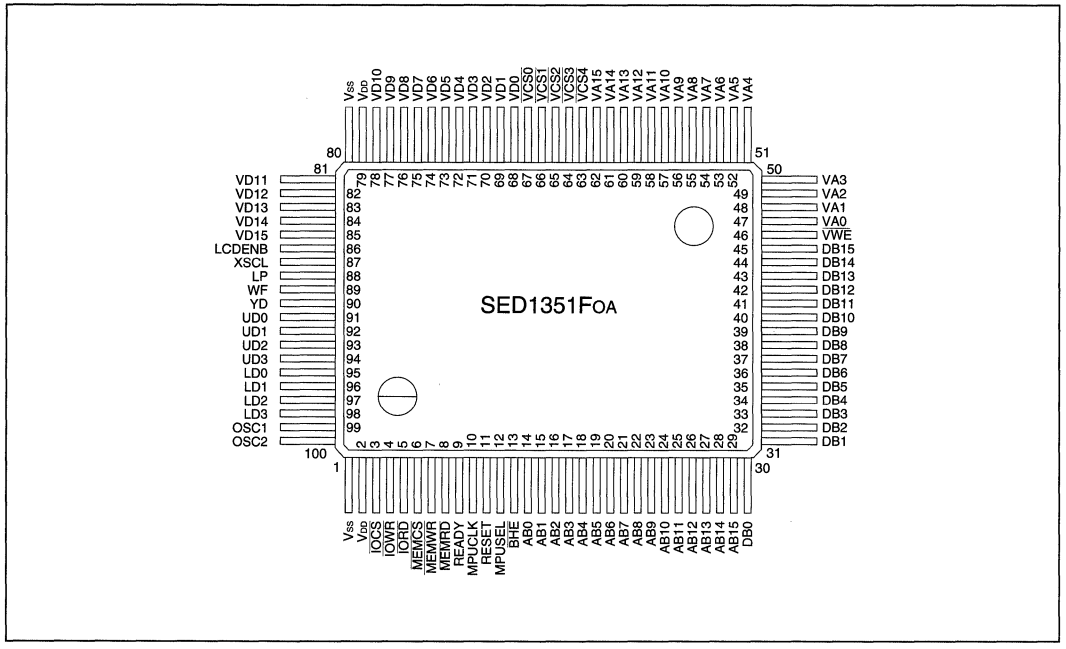
Type 1. $\overline{MEMCS}$, $\overline{MEMWR}$, $\overline{MEMRD}$, $\overline{IOCS}$, $\overline{IOWR}$, $\overline{IORD}$, MPUCLK, AB0 ~ AB15, $\overline{BHE}$, MPUSEL, RESET, OSC

Type 2. $\overline{MEMCS}$, $\overline{MEMWR}$, $\overline{MEMRD}$, $\overline{IOCS}$, $\overline{IOWR}$, $\overline{IORD}$, MPUCLK, AB0 ~ AB15, $\overline{BHE}$, DB0 ~ DB15, VD0 ~ VD15

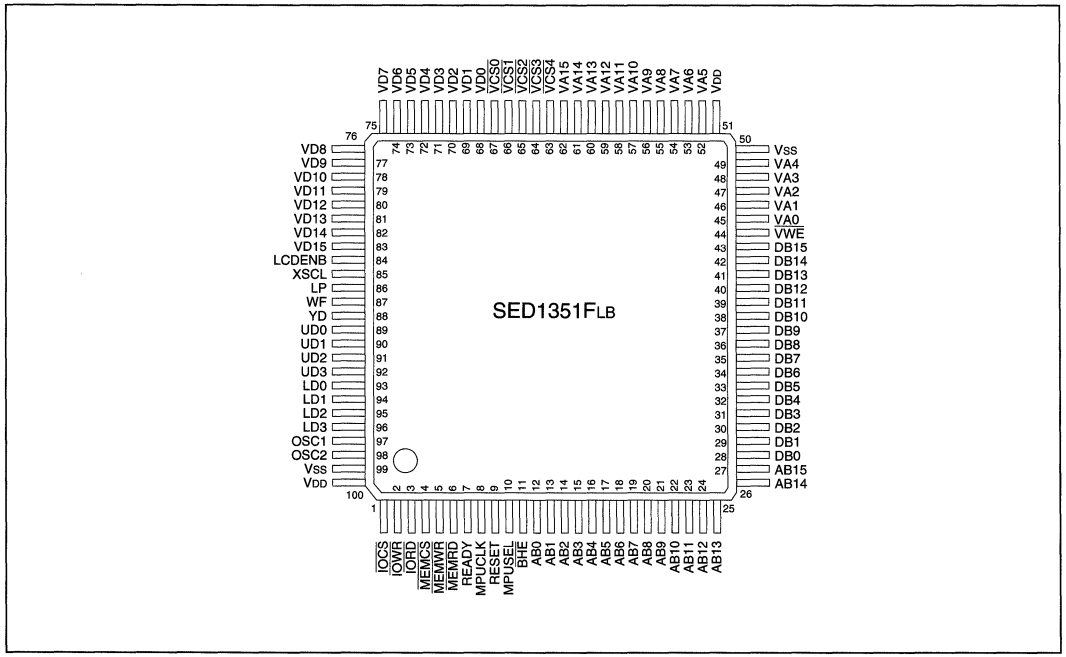
Type 3. MPUSEL, RESET

Type 4. DB0 ~ DB15, READY, VA0 ~ VA15, $\overline{VCS0}$ ~ $\overline{VCS4}$, VD0 ~ VD15, $\overline{VWE}$, XSCL, LP, WF, YD, UD0 ~ UD3, LD0 ~ LD3, LCDENB

■ PIN CONFIGURATION (F0A)



■ PIN CONFIGURATION (FLB)



■ PIN DESCRIPTION

1. System Connector Terminals (at MPU)

Pin Name	Type	FOA Pin No.	FLB Pin No.	Drv	Description
DB0 to DB15	I/O	30 to 45	28 to 43		These pins are interfaced with the MPU data bus. When using an 8-bit MPU, connect DB8 to DB15 to VDD.
AB0 to AB15	I	14 to 29	12 to 27		These pins are interfaced with the MPU address bus. If multiplexed address signals are used, connect them via latch circuits. A control register is selected by AB0 to AB3. Correspondence of the MPU address bus to the VRAM address bus is such that ABi = VAi (where i is a pin number).
$\overline{BHE}$	I	13	11		This signal is a bus high enable signal where a 16-bit MPU is used. It goes "L" (low) when an odd address is encountered. When using an 8-bit MPU configuration, connect the BHE pin to VDD.
$\overline{IOCS}$	I	3	1		This pin selects a control register contained in the SED1351. It is "L" active, and must be assigned to MPU I/O space.
$\overline{IOWR}$	I	4	2		This signal is used for writing data into a control register contained in the SED1351. It is "L" active, and must go "L" when it encounters an OUT instruction from the MPU.
$\overline{IORD}$	I	5	3		This signal is used for reading data from a control register contained in the SED1351. It is "L" active, and must go "L" when it encounters an IN instruction from the MPU.
$\overline{MEMCS}$	I	6	4		This signal is used for selecting VRAM. It is "L" active, and must be assigned to MPU memory space.
$\overline{MEMWR}$	I	7	5		This signal is used for writing data to the VRAM. It is "L" active, and must go "L" when it encounters a memory write instruction from the MPU.
$\overline{MEMRD}$	I	8	6		This signal is used for reading data from the VRAM. It is "L" active, and must go "L" when it encounters a memory read instruction from the MPU.
READY	O	9	7		This signal requests the MPU to wait. It goes "L" by the falling edge of IOCS or MEMCS. It goes "H" by the rising edge of MPUCLK after completion of the SED1351 internal processing. Since READY is not a tri-state pin, it needed not be pulled up and must be connected directly to the READY (WAIT) terminal of the MPU.
MPUCLK	I	10	8		This pin accepts an MPU clock. The MPU wait state is cleared by the rising edge of MPUCLK.
MPUSEL	I	12	10		This signal is connected to either VDD or VSS for selection of an MPU. MPUSEL = V_{SS} 8-bit MPU (e.g., Z80, V20, i8088) MPUSEL = V_{DD} 16-bit MPU (e.g., V30, i8086)
RESET	I	11	9		The MPU reset signal comes to this pin. It is "H" active, and initializes a control register.

Combinations of Control Pins

$\overline{IOCS}$	$\overline{IOWR}$	$\overline{IORD}$	$\overline{MEMCS}$	$\overline{MEMWR}$	$\overline{MEMRD}$	Operation
1	*	*	1	*	*	Invalid
0	0	1	1	1	1	Write to control register
0	1	0	1	1	1	Read from control register
1	1	1	0	0	1	Write to VRAM
1	1	1	0	1	0	Read from VRAM

Note: Any combination other than those listed above will cause a system error.

1 = "H" (high)
0 = "L" (low)
* = Don't care

2. VRAM Connector Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
VD0 to VD15	I/O	68 to 78, 81 to 85	68 to 83		These pins are interfaced with the VRAM data bus. For a 16-bit MPU configuration, VD0 to VD7 must be connected to even addresses, and VD8 to VD15 to odd addresses. For an 8-bit configuration, VD8 to VD15 must be connected to VDD.
VA0 to VA12	O	47 to 59	45 to 49, 52 to 59		These pins are interfaced with the VRAM address bus and chip select pins.
VA13/$\overline{VCS7}$ to VA15/VCS5	O	60 to 62	60 to 62		The SED1351 has chip select pins that can directly control eight 64K SRAMs (8K bytes each) or two 256K SRAMs (32K bytes) in the 64K VRAM space. See Technical Manual for details.
$\overline{VCS0}$ to $\overline{VCS4}$	O	67 to 63	67 to 63		
$\overline{VWE}$	O	46	44		This signal is used for writing data to the VRAM. It is "L" active, and must be connected to the WE pin of the VRAM.

3. Oscillator Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
OSC1	I	99	97		The OSC1 (input) and OSC2 (output) pins generate clocks for internal operation. They allow crystal oscillation and external clock input.
OSC2	O	100	98		

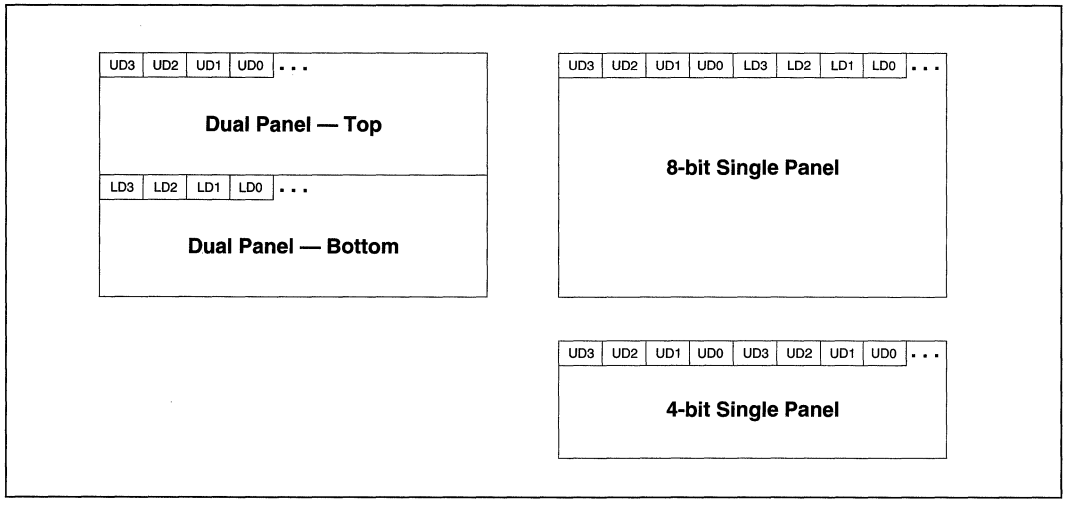
4. Power Terminals

Pin Name	Type	F0A Pin No.	FLB Pin No.	Drv	Description
V_{DD}	—	2, 79	51, 100		The power supply pins include two V_{DD}s and two V_{SS}s. Apply +5V or +3V to V_{DD} and 0V to V_{SS}. A capacitor (4.7 µF or more) must be connected near each pair of V_{DD}/V_{SS} pins.
V_{SS}	—	1, 80	50, 99		

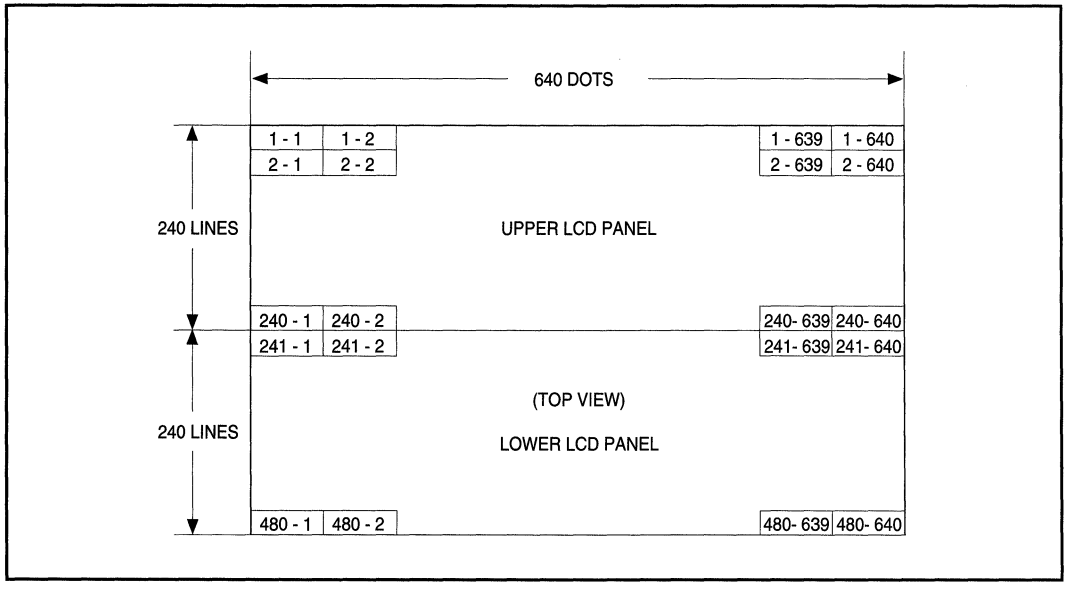
5. LCD Connector Terminals

Pin Name	Type	FOA Pin No.	FLB Pin No.	Drv	Description
UD0 to UD3	I/O	91 to 94	89 to 92		LCD display data. UD0 to UD3 are the upper panel display data in the signal panel or double panel drive panel mode. LD0/UD4 to LD3/UD7 are the lower panel display data in the double panel drive mode. UD0 to UD3, and LD0/UD4 to LD3/UD7 are used for 8-bit data transfer in the single panel drive mode.
LD0/UD4 to LD3/UD7	O	95 to 98	93 to 96		
XSCL	O	87	85		This single is a shift clock for display data transfer. Take the UD0 to UD3, LD0/UD4 to LD3/UD7 display data into LCDs by the falling edge of XSCL.
LP	O	88	86		This pin provides both a display data latch pulse and a scan signal transfer clock. Upon completion of transferring the LCD data on one line, display data can be latched or a scan signal transferred by the falling edge of LP.
WF	O	89	87		This pin provides a frame signal used for LCD AC driving.
YD	O	90	88		This pin provides a scanning line start pulse. The signal is "H" active. Allow the scanning line drive IC to take in YD by the falling edge of LP. The SED1351 has two lines of retracing; if two scanning line drive ICs are cascade-connected for the upper and lower panels in the double panel drive mode, two lines must be provided between the upper and lower scanning line drive outputs.
LCDENB	O	86	84		This pin provides the data which is set in bit 1 (D1) of the mode register (R1). LCDENB goes "L" when the system is reset; it can be effectively used for LCD power control.

Illustrated below are the display data which are output from the UD0 to UD3, LD0/UD4 to LD3/UD7 and the display on the panel:

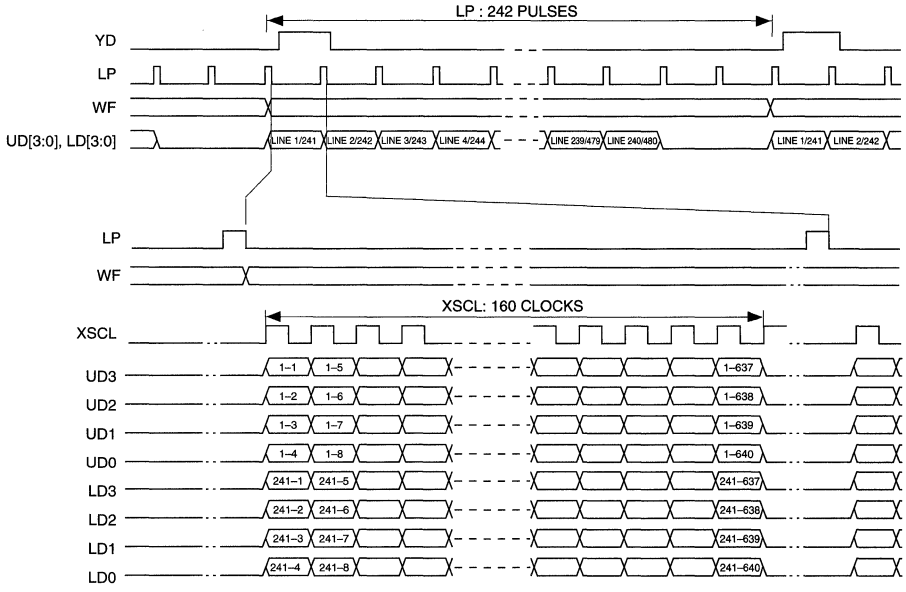


■ LCD PANEL PIXELS



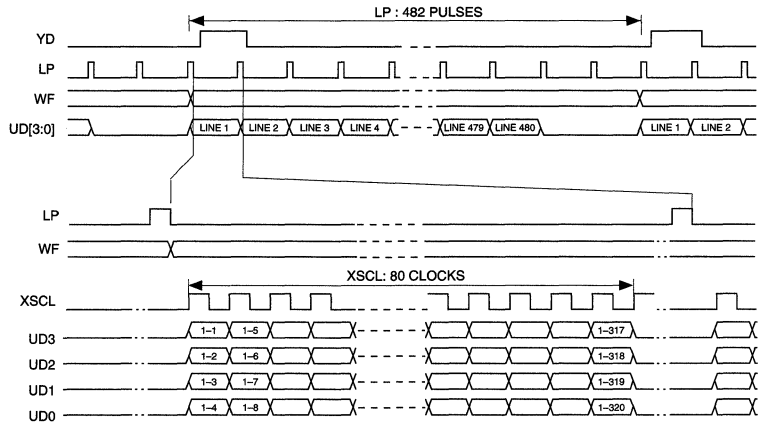
■ MONOCHROME LCD PANEL INTERFACE

8-Bit Dual Monochrome Panel (i.e. 640 × 480)

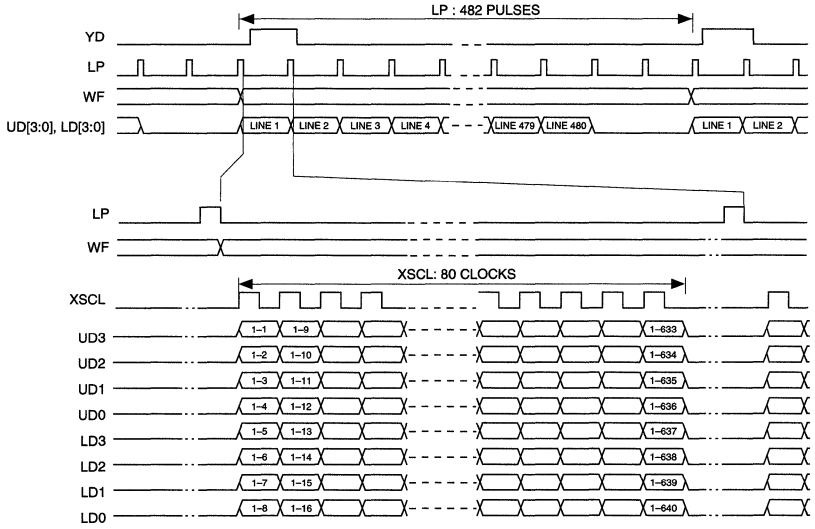


■ MONOCHROME LCD PANEL INTERFACE

4-Bit Single Monochrome Panel (i.e. 320 × 480)



8-Bit Single Monochrome Panel (i.e. 640 × 480)

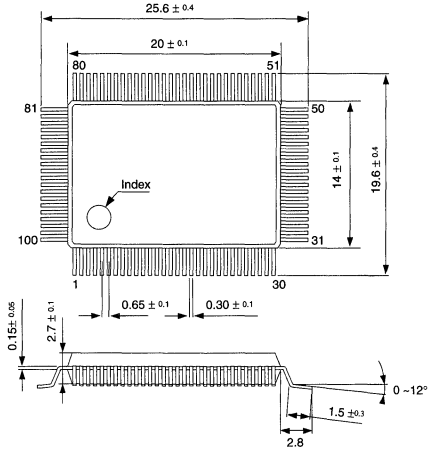


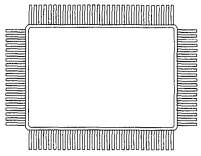
■ PACKAGE DIMENSIONS

● SED1351F0A

QFP5-100pin

Unit: mm



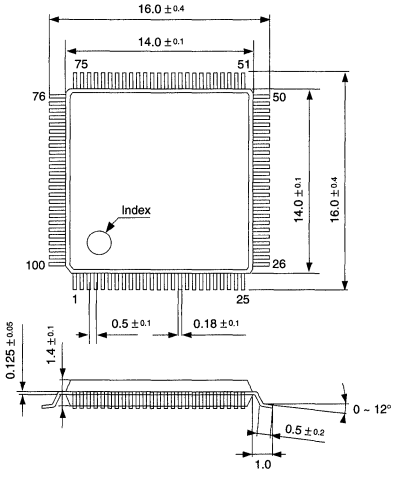


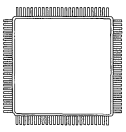
Actual Size

● SED1351FLB

QFP15-100pin

Unit: mm





Actual Size

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GRAPHICS LCD CONTROLLER

■ DESCRIPTION

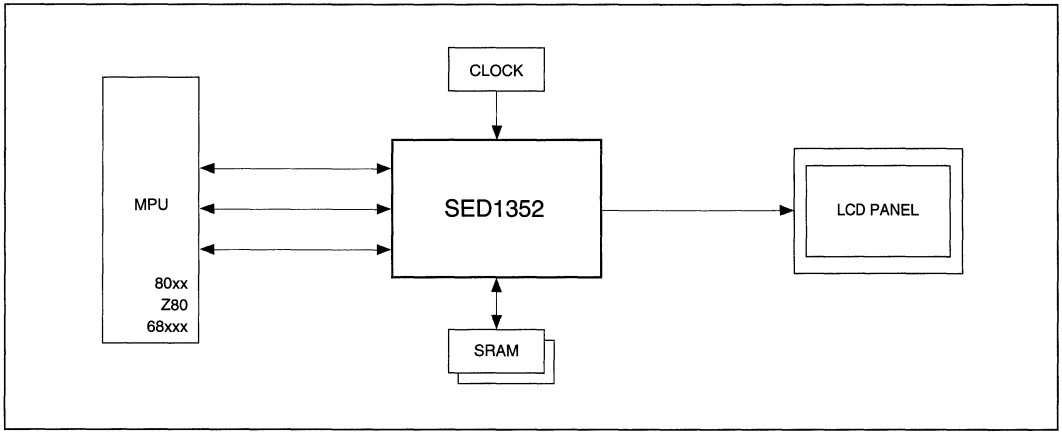
The SED1352 is a high duty cycle, graphic display LCD controller capable of displaying a maximum of 16 levels of gray shade on single and dual scan Liquid Crystal Displays. A 16x4 lookup table is provided to allow remapping of the 16 possible gray shades displayed on the LCD panel. The SED1352 can interface to MC68000 microprocessor, 8/16 bit ISA Bus, and 8/16 bit MPUs with READY (WAIT#) signal with minimum external "glue" logic. This chip can directly control up to 128 Kbytes of static SRAM.

Optimized for cost and power savings, the SED1352 can operate from 2.7 Volt to 5.5 Volt and from 5 Mhz to 25Mhz.

■ FEATURES

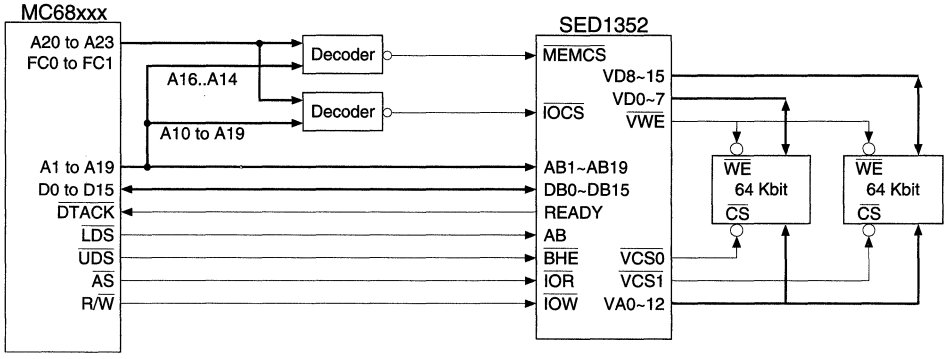
- 16-bit 16 Mhz MC68000 MPU interface
- 8/16-bit ISA data bus interface bus
- 8/16 bit MPU interface controlled by a READY (or WAIT#) signal
- Option to use built-in index register or direct-mapping to access one of fifteen internal registers
- 2-terminal crystal input for internal or external crystal oscillator
- 8/16 bit SRAM interface configurations
- Two software power-save modes
- Low power consumption
- Virtual display support
- Packed pixel mode support
- Display modes:
  - 2 bit/pixel, 4-level gray-scale display
  - 4 bit/pixel, 16-level gray-scale display
- Display memory interface:
  - One 1 Mbit SRAM(64Kx16)
  - One or two 32Kbyte SRAM(s)
  - One or two 8Kbyte SRAM(s)
  - One 8Kbyte and one 32Kbyte SRAM
- LCD panel configurations:
  - Single-panel, single-drive display
  - Dual-panel, dual-drive display
- Maximum number of vertical lines:
  - 1,024 lines (single-panel, single-drive display)
  - 2,048 lines (dual-panel, dual-drive display)
- Split screen display support at single-panel mode
- QFP5-100-S2 package

■ SYSTEM BLOCK DIAGRAM



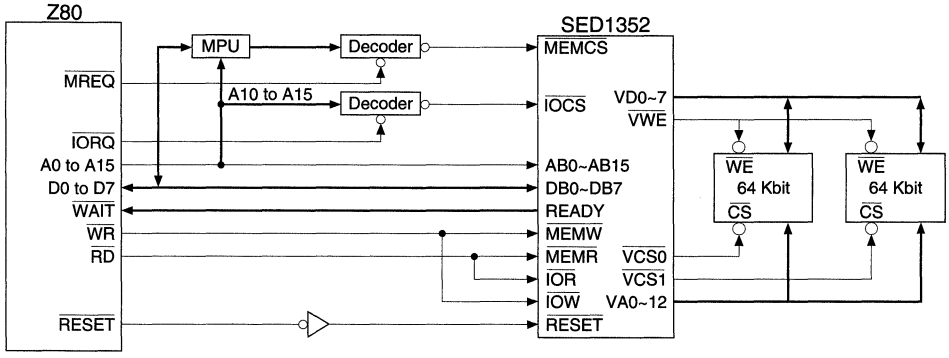
■ INTERFACE OPTIONS

Interface with 16-bit MC68xxx MPU and 16Kbytes SRAM (2 of 8K × 8)



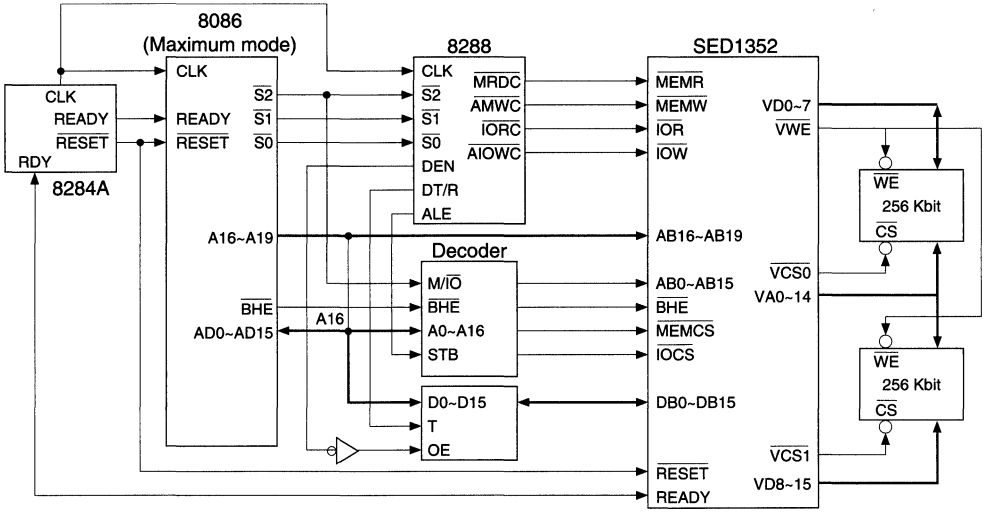
Note: Example implementation, actual may vary.

Interface with 8-bit Z80 MPU and 16Kbytes SRAM (2 of 8K × 8)



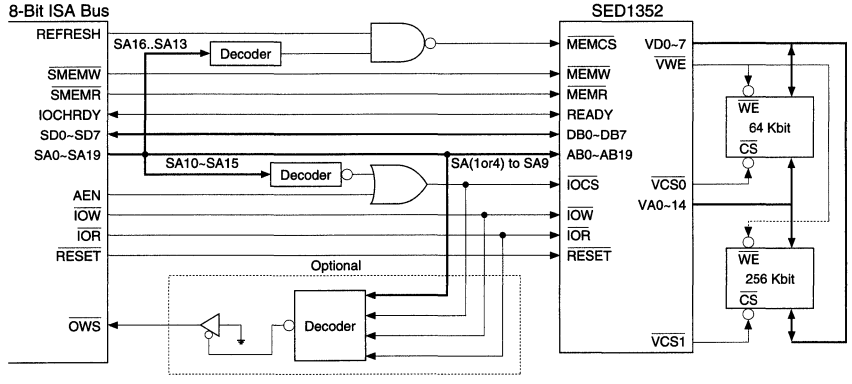
Note: Example implementation, actual may vary.

Interface with 16-bit 8086 MPU and 64Kbytes SRAM (2 of 32K × 8)



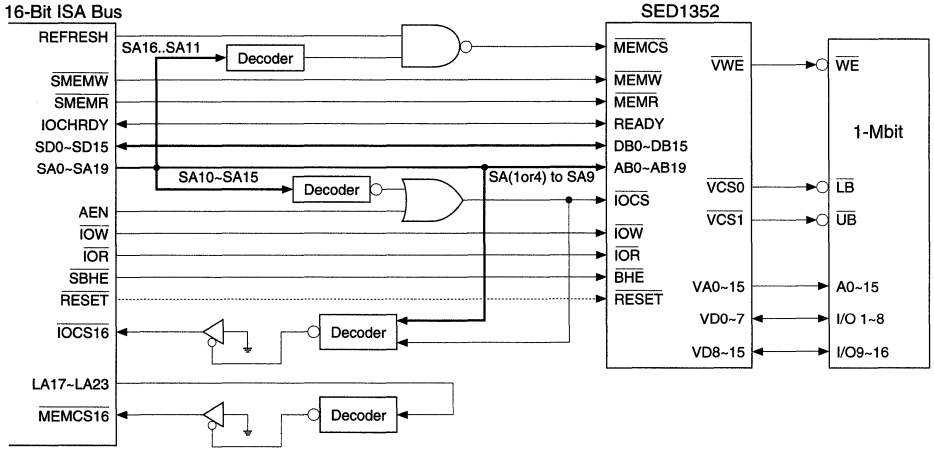
Note: Example implementation, actual may vary.

Interface with 8-bit ISA Bus and 40Kbytes SRAM (1 of 8K × 8 and 1 of 32K × 8)



Note: Example implementation, actual may vary.

Interface with 16-bit ISA Bus and 128Kbytes SRAM (1 of 128K × 8)

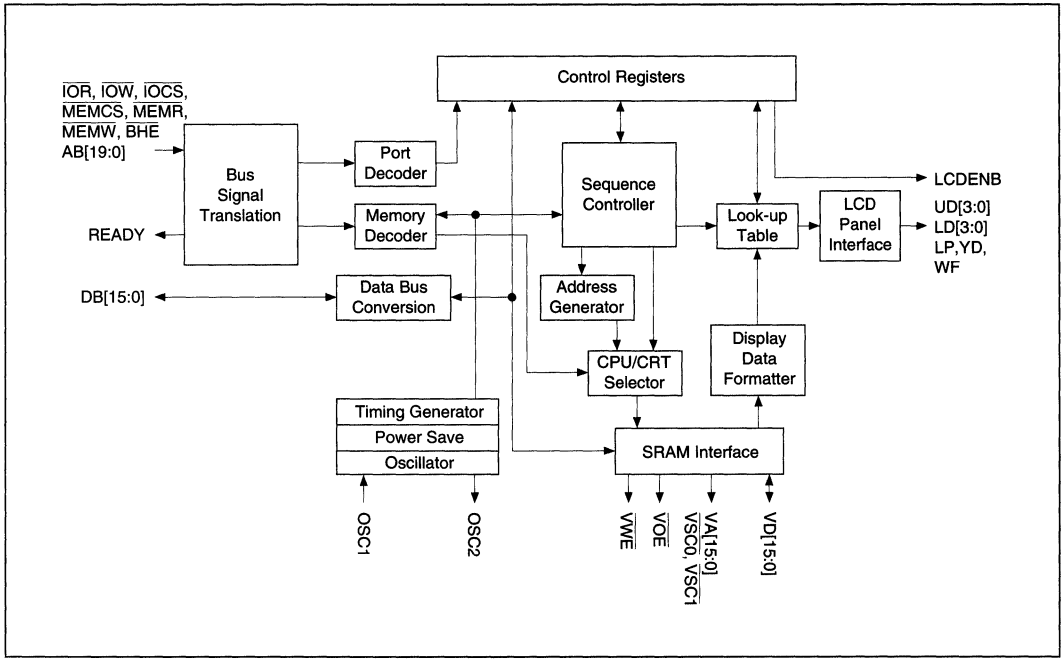


Note: Example implementation, actual may vary.

■ SUPPORTED RESOLUTIONS

Display RAM	Example Display Size		SRAM Type	CPU Interface	SRAM Interface
	4 Grays	16 Grays			
	x y	x y			
8 Kbyte	256 x 128	128 x 128	1 of 8Kx8	8-bit	8-bit
16 Kbyte	320 x 200	200 x 160	2 of 8Kx8	8-bit	8-bit/16-bit
				16-bit	16-bit
32 Kbyte	512 x 256	256 x 256	1 of 32Kx8	8-bit	8-bit
40 Kbyte	512 x 320	320 x 256	1 of 8Kx8 and 1 of 32Kx8	8-bit	8-bit
64 Kbyte	512 x 512	512 x 256	2 of 32Kx8	8-bit	8-bit/16-bit
				16-bit	16-bit
128 Kbyte	1024 x 512	512 x 512	1 of 64Kx16	16-bit	16-bit

■ BLOCK DIAGRAM



■ DC SPECIFICATIONS

● Absolute Maximum Ratings

Parameters	Symbol	Rating	Units
Supply voltage	V_{DD}	V_{SS} –0.3 to +6.5	V
Input voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	V_{SS} –0.3 to V_{DD} +0.3	V
Ambient temperature	T_A	–55 to 125	°C
Storage temperature	Tstg	–65 to 150	°C
Solder temperature/time	T_{SOL}	260 for 10 sec. max at lead	°C

● Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units
Supply voltage	$V_{DD\ (1)}$	V_{SS} = 0V	4.5	5.0	5.5	V
Supply voltage	$V_{DD\ (2)}$	V_{SS} = 0V	2.7	3.0	3.3	V
Input voltage	V_{IN}		V_{SS}	—	V_{DD}	V
Junction temperature	T_j		0	—	115	°C
Operating temperature	T_{OPR}		0	25	70	°C

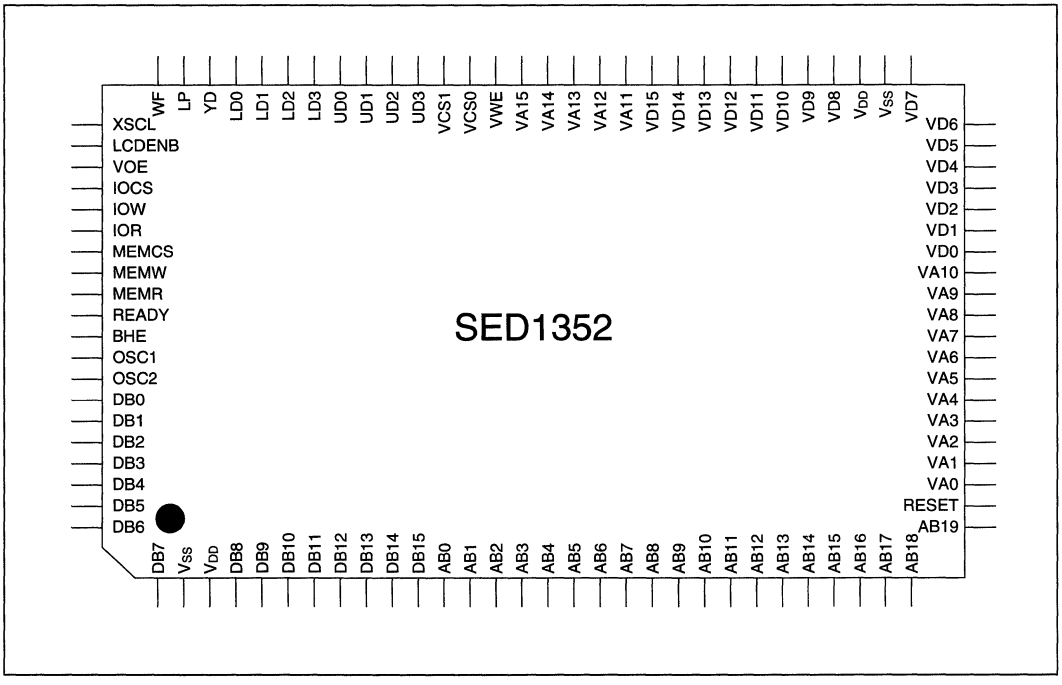
● Input Specifications

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units
Low level input voltage CMOS inputs TTL inputs	V_{IL}	V_{DD} = Min			1.0 0.8	V V
Low level input voltage CMOS inputs TTL inputs	V_{IH}	V_{DD} = Max	3.5 2.0			V V
Positive going threshold CMOS Schmitt inputs TTL Schmitt inputs	V_{T+}	V_{DD} = 5.0			4.0 2.4	V V
Negative going threshold CMOS Schmitt inputs TTL Schmitt inputs	V_{T-}	V_{DD} = 5.0	0.8 0.6			V V
Hysteresis voltage CMOS Schmitt inputs TTL Schmitt inputs	V_H	V_{DD} = 5.0	0.3 0.1			V V
Input leakage current	I_{IZ}	V_{DD} = MAX $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$	–1		1	µA
Input pin capacitance	C_{IN}			4		pF
Pull down resistance	HR_{PD}	V_{DD} = 5.0 V $V_I = V_{DD}$	50	100	180	KΩ
Pull down resistance	LR_{PD}	V_{DD} = 3.3 V $V_I = V_{DD}$	90	180	360	KΩ

● Output Specifications

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units
Low level output voltage Type 2 – TS2, CO2, TS2D1 Type 3 – TS3 Type 4 – TS4, OD4	V_{OL}	I_{OL} = 6 mA I_{OL} = 12 mA I_{OL} = 24 mA			V_{SS} + 0.4	V
High level output voltage Type 2 – TS2, CO2, TS2D1 Type 3 – TS3 Type 4 – TS4, OD4	V_{OH}	I_{OL} = –2 mA I_{OL} = –4 mA I_{OL} = –8 mA	V_{DD} – 0.4			V
Output leakage current	I_{OZ}	V_{DD} = MAX $V_{OH} = V_{DD}$ $V_{OL} = V_{SS}$	–1		1	µA
Output pin capacitance	C_{OUT}			6		pF
Bidirectional pin capacitance	C_{BID}			10		pF

■ SED1352 PIN OUTS



■ PIN DESCRIPTION

Key

A = Analog
I = Input
O = Output
I/O = Bi-directional
P = Power

Bus Interface

Pin Name	Type	Pin #	Description
DB0-DB15	I/O	94 - 100, 1, 4 - 11	These pins are connected to the system data bus. In 8-bit bus mode, DB8-DB15 must be tied to VDD.
AB0	I	12	In MC68000 MPU interface, this pin is connected to the Lower Data Strobe (LDS#) pin of MC68000. In other bus interfaces, this pin is connected to the system address bus.
AB1-AB19	I	13 - 31	These pins are connected to the system address bus.
BHE#	I	91	In MC68000 MPU interface, this pin is connected to the Upper Data Strobe (UDS#) pin of MC68000. In other bus interfaces, this pin is the Bus High Enable input for use with 16-bit system. In 8-bit bus mode, tie BHE# input to VDD.
IOCS#	I	84	Active low input to select one of fifteen internal registers.
IOW#	I	85	In MC68000 MPU interface, this pin is connected to the R/W# pin of MC68000. This input pin will define whether the data transfer is a read (active high) or write (active low) cycle. In other bus interfaces, this is the active low input to write data into an internal register.
IOR#	I	86	In MC68000 MPU interface, this pin is connected to the AS# pin of MC68000. This input pin will indicate a valid address is available on the address bus. In other bus interfaces, this is the active low input to read data from an internal register.
MEMCS#	I	87	Active low input to indicate the attempt to access the display memory.
MEMW#	I	88	Active low input to write data to the display memory.
MEMR#	I	89	Active low input to read data from the display memory.
READY	O	90	For MC68000 MPU interface, this pin is connected to the DTACK# pin of MC68000 and will be driven low whenever a data transfer is complete. In other bus interfaces, this output is driven low to force the system to insert wait states when needed. READY is released to high-Z after the transfer is completed.
RESET	I	32	Active high input to force all signals to their inactive states.

Display Memory Interface

Pin Name	Type	Pin #	Description
VD0-VD15	I/O	44-51, 54-61	These pins are connected to the display memory data bus. For 16-bit interface, VD0-VD7 are connected to the display memory data bus of even byte addresses and VD8-VD15 are connected to the display memory data bus of odd byte addresses. The output drivers of these pins are placed into a high-Z state when RESET is high. On the falling edge of RESET, the values of VD0-VD15, each with internal pull-down resistor, will be latched into the chip to configure various hardware options.
VA0-VA15	O	33-43, 62-66	These pins are connected to the display memory address bus.
VCS1#	O	69	Active low chip-select output to the second or odd byte address SRAM. See display memory interface section for details.
VCS0#	O	68	Active low chip-select output to the first or even byte address SRAM. See display memory interface section for details.
VWE#	O	67	Active low output used for writing data to the display memory. This pin is connected to the WE# input of the SRAMs.
VOE#	O	83	Active low output to enable reading of data from the display memory. This pin is connected to the OE# input of the SRAMs.

LCD Interface

Pin Name	Type	Pin#	Description
UD3-UD0	O	70 - 73	Upper panel display data for dual panel mode. For single panel mode, these bits are the most significant 4 bits of the 8 bits output data to the panel (PD[4:7]). For 4-bit signel panel mode, these bits are the 4 bits of output data to the panel.
LD3-LD0	O	74 - 77	Lower panel display data for dual panel mode. For 8-bit single panel mode, these bits are the least significant 4 bits of the 8 bits output data to the panel (PD[0:3]). For 4-bit signel panels, these bits are driven 0 (low state).
XSCL	O	81	Display data shift clock. Data is shifted into the LCD X-drivers on the falling edge of this signal.
LP	O	79	Display data latch clock. The falling edge of this signal is used to latch a row of display data in the LCD X-drivers and to turn on the row driver (Ydriver).
WF	O	80	LCD AC-drive signal output.
YD	O	78	Vertical scanning start pulse. A logic '1' on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row driver (Y driver) to indicate the start of the vertical frame.
LCDENB	O	82	LCD enable signal output. It can be used externally to turn off the panel supply voltage and backlight.

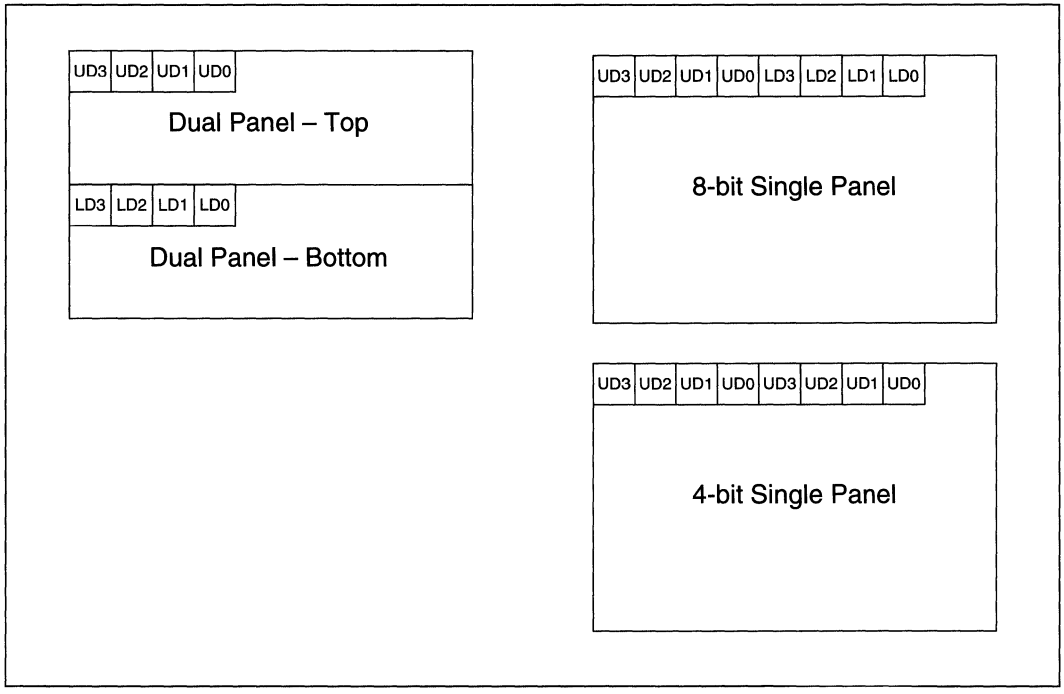
Clock Inputs

Pin Name	Type	Pin#	Description
OSC1	I	92	This pin, along with OSC2 is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
OSC2	O	93	This pin, along with OSC1 is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.

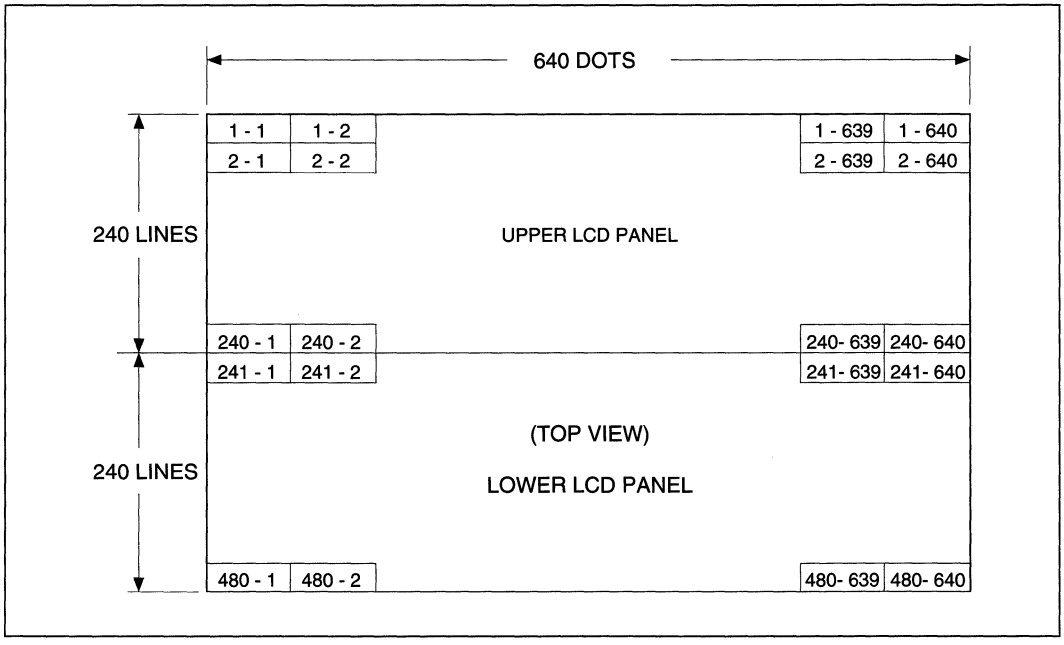
Power Supply

Pin Name	Type	Pin#	Description
V_{DD}	P	3, 53	Voltage supply.
V_{SS}	P	2, 52	Voltage ground.

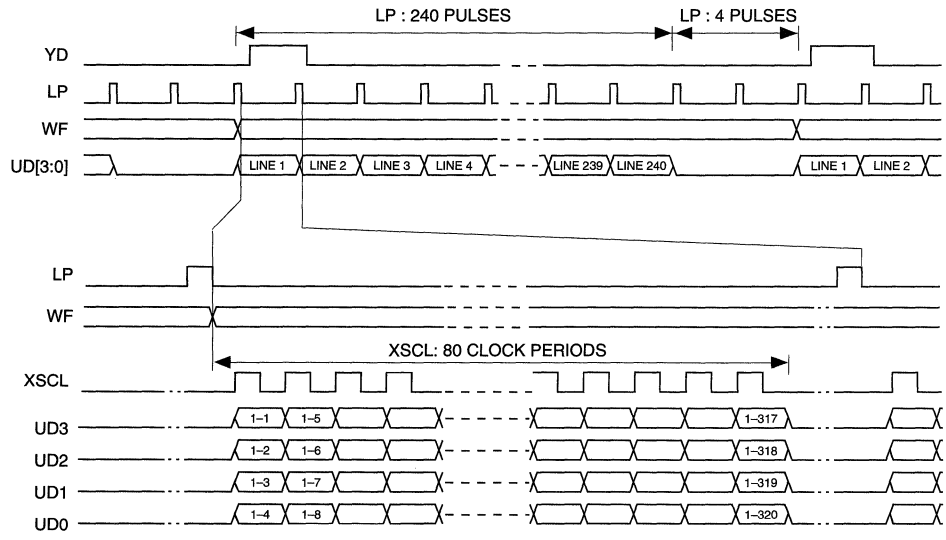
Illustrated below are the display data output which are output from the UD0 to UD3, LD0/UD4 to LD3/UD7 and the display on the panel:



■ LCD PANEL PIXELS

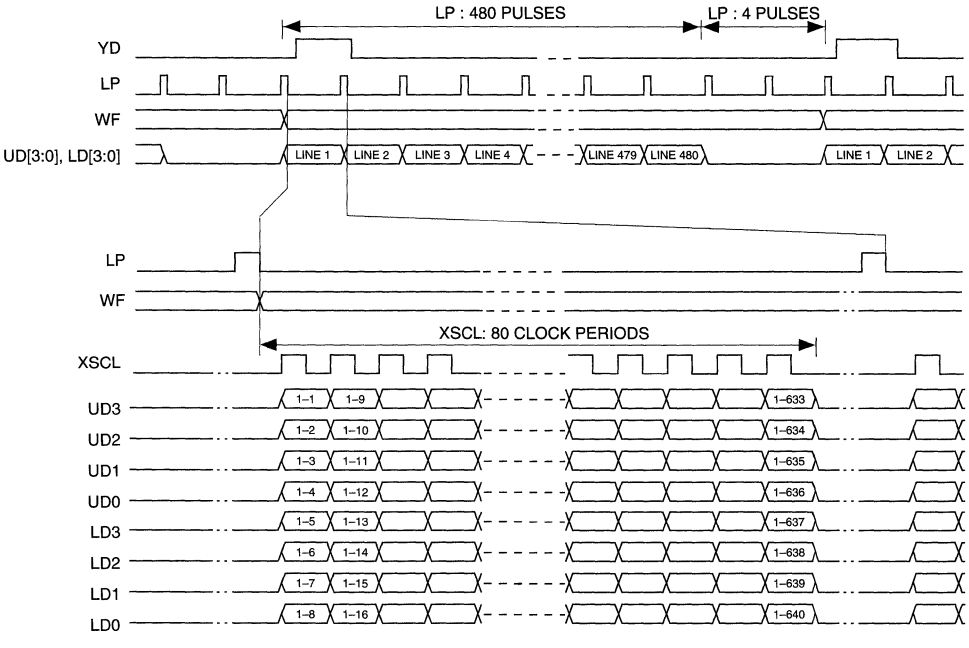


■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE



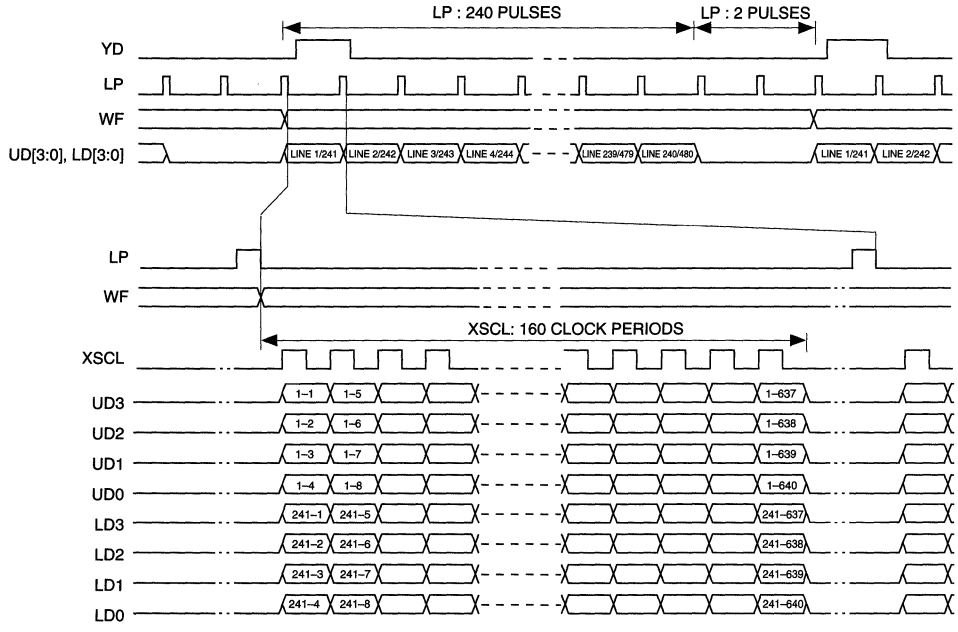
Example timing for 320 × 240 single panel

■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE



Example timing for 640 × 480 panel

■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE

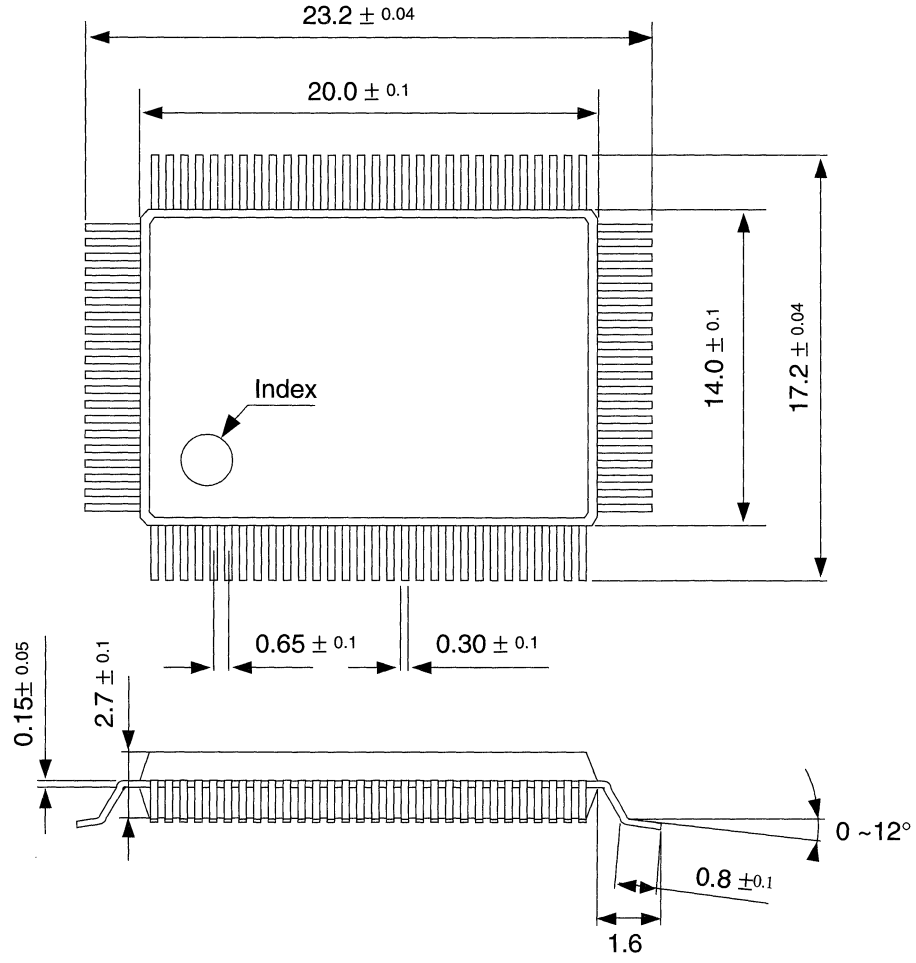


Example timing for 640 × 480 panel

■ PACKAGE DIMENSIONS

QFP5-100-S2 100 pin

Unit: mm



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1996 DATABOOK

GRAPHICS PRODUCTS

IV. LCD DRIVER-CONTROLLERS

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■ LCD DRIVER-CONTROLLERS (12xx Series)

Part Number		SED 1200	SED 1210	SED 1230	SED 1231 T	SED 1232 E	SED 1233 X	SED 1234 T	SED 1235	SED 1278	SED 1280
Discontinued?		No	No	No	No	No	No	No	No	No	No
Replacement		—	—	—	—	—	—	—	—	—	—
Commons		16	16	30	23	16	16	30	16	16	16
Segments		50	40	65	65	65	80	62	62	40	40
Duty Cycle	1/3										
	1/4										
	1/7										
	1/8	x	x							x	x
	1/9										
	1/10										
	1/11									x	x
	1/16	x	x			x	x		x	x	x
	1/17										
	1/23				x						
	1/24										
	1/25										
	1/30			x				x			
	1/32										
	1/33										
	1/48										
	1/49										
	1/64										
	1/65										
LCD Voltage (V)		−3.5 to −5.5	−3.5 to −5.5	−4.5 to −12	−4.5 to −12	−4.5 to −12	−4.5 to −12	−4.5 to −12	−4.5 to −12	−3 to −5.5	−3 to −5.5
Supply Voltage	5V	x	x							x	x
	3V	x	x	x	x	x	x	x	x		
CPU Interface	MPU	x	x	x	x	x	x	x	x	x	
	68xx			x	x	x	x	x	x	x	
	80xx	x	x	x	x	x	x	x	x		

(continued)

■ LCD DRIVER-CONTROLLERS (12xx Series – continued)

Part Number			SED 1200	SED 1210	SED 1230	SED 1231 T	SED 1232 E	SED 1233 X	SED 1234 T	SED 1235	SED 1278	SED 1280
Display Data Bus (bits)		1			x	x	x	x	x	x		x
		4	x		x	x	x	x	x	x	x	
		8		x	x	x	x	x	x	x	x	
Fosc,max (KHz)			100	100	39	30	21	26			250	1000
CGROM Size (chars)			160	160	256	256	256	256			240	240
CGRAM size (chars)			4	4	4	4	4	4			8	8
Display Data RAM size			20 char	40 char	48 char	48 char	48 char	48 char	48 char	48 char	80 char	80 char
Companion Chips				1181							1181, 1681	1181, 1681
Integrated DC/DC Converter					x	x	x	x				
Static Icon					x	x	x	x				
Contrast Adjustment By Software					x	x	x	x				
Master/Slave Operation												
Panel Type		Passive	x	x	x	x	x	x			x	x
		MIM										
		TFT										
Package	Die	Al	D0A(JIS) D0B (ASCII)	D0A(JIS) D0B (ASCII)	D0A	D0A	D0A	D0A	D0A	D0A	D0A D0B D0C D0E D0G D0H	
		Au			D0B	D0B	D0B	D0B	D0B	D0B		
		COG										
		PadPitch (μm)	190	190	110	110	110	110				
	QFP	Thin	F1B									
		Thick	F0A (JIS) F0B (ASCII)	F0A (JIS) F0B (ASCII)							F0A F0B F0C F0E F0G F0H	F0A F0B F0C
		# of Pins	80	80							80	100
	TAB	2sided			TBB	TBB	TBB	TBB				
		4sided										
		LeadPitch (μm)										
Page Number			237	253	265	265	265	265	265	265	287	303

(continued)

■ LCD DRIVER-CONTROLLERS (15xx Series)

Part Number		SED 1500	SED 1501	SED 1502	SED 1503	SED 1507	SED 1510	SED 1520	SED 1521	SED 152A	SED 1522	SED 1526	SED 1527	SED 1528	SED 1530	SED 1531	SED 1532	SED 1540	SED 1560	SED 1561	SED 1562
				T	E	X	T		&		G	R	A	P	H	I	C	S			
Discontinued?		Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No
Replacement		No	No	No	No	No	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Commons		8	10	16	8	7	4	16	0	0	8	17	17	33	33	0	33	4	65/0	33	17
Segments		42	40	34	42	43	32	61	80	80	69	80	80	64	100	132	100	73	102/ 165	134	150
Duty Cycle	1/3																	x			
	1/4						x											x			
	1/7					x															
	1/8	x							x	x	x	x									
	1/9								x	x		x									
	1/10		x						x	x											
	1/11								x	x											
	1/16			x	x			x	x	x	x	x	x								x
	1/17								x	x		x	x								x
	1/23									x											
	1/24								x	x										x	
	1/25								x	x										x	
	1/30									x											
	1/32							x	x	x			x	x						x	
	1/33												x	x	x					x	
	1/48																		x		
	1/49																		x		
	1/64																		x		
	1/65															x	x		x		
LCD Voltage (V)		–3 to –10	–3 to –10	–3 to –10	–3 to –10	–3 to –10	–1.8 to –6	–3.5 to –13	–3.5 to –13	+3.5 to +13	–3.5 to –13	–4.5 to –16	–4.5 to –16	–4.5 to –16	–4.5 to –16	–4.5 to –16	–4.5 to –16	–3.5 to –11	–6 to –16	–5 to –16	–4.5 to –16
Supply Voltage	5V	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	3V	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
CPU Interface	MPU	x	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	x	x
	68xx							x	x	x	x	x	x	x	x	x	x	x	x	x	x
	80xx							x	x	x	x	x	x	x	x	x	x	x	x	x	x
Display Data Bus (bits)	1						x					x	x	x	x	x	x		x	x	x
	4	x	x	x	x	x															
	8	x	x	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	x	x
Fosc,max (KHz)		32	32	32	32	32	18	2,18	2,18	2	2,18	20	20	20	22	22	22	4,18	18	18	18

(continued)

■ LCD DRIVER-CONTROLLERS (15xx Series – continued)

Part Number			SED 1500	SED 1501	SED 1502	SED 1503	SED 1507	SED 1510	SED 1520	SED 1521	SED 152A	SED 1522	SED 1526	SED 1527	SED 1528	SED 1530	SED 1531	SED 1532	SED 1540	SED 1560	SED 1561	SED 1562
Display Data RAM size			672 bits	672 bits	672 bits	672 bits	672 bits	128 bits	2560 bits	2560 bits	2560 bits	2560 bits	2640 bits	2640 bits	2640 bits	8580 bits	8580 bits	8580 bits	2560 bits	10790 bits	10790 bits	10790 bits
Companion Chips									1520					1527			1635	1532		1630 /31	1630 /31	1630 /31
Integrated DC/DC Converter													2x, 3x	2x, 3x	2x, 3x	x	x	x		2x, 3x	2x, 3x	2x, 3x
Static Icon																x	x	x				
Contrast Adjustment By Software													x	x	x	x	x	x		x	x	x
Master/Slave Operation									x	slave only	slave only	x	x	x	x	x	x	x	x	x	x	x
Panel Type		Passive	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
		MIM																				
		TFT																				
Package	Die	Al						D0C	D0A DAA	D0A DAA	D0A #	D0A DAA	D*A	D*A	D*A	D*A	D*A	D*A	D0A			
		Au							D0B DAB	D0B DAB		D0B DAB	D*B	D*B	D*B	D*B	D*B	D*B	D0B			
		COG																				
		Pad Pitch (µm)							199	199		199	130	130	130	118	118	118	199	100	100	100
	QFP	Thin						F0C	F0C FAC	F0C FAC		F0C FAC										
		Thick	F0A	F0A	F0A	F0A	F0A	F0E (QFP 6-60)	F0A FAA	F0A FAA		F0A FAA	F0A	F0A	F0A				F0A			
		# of Pins	80	80	80	80	80	48	100	100		100	128	128	128				100			
	TAB	2sided							T0A TAA	T0A TAA		T0A TAA	T0A	T0A	T0A	T0A	T0A	T0A TBA		T0B	T0B	T0B
		4sided																		TQA	TQA	TQA
		Lead Pitch (µm)																				280
Page Number			307	307	307	307	307	315	329	329	341	343	353	353	353	369	369	369	389	395	395	395

CMOS DOT MATRIX LCD CONTROLLER DRIVER

- **1/8 or 1/16 Duty Cycle Dot Matrix Drive**
- **20-Character Simultaneous Display**
- **Built-in Character Generator ROM and RAM**

■ DESCRIPTION

The SED1200 is a character LCD controller-driver, capable of driving display as large as 2 lines of 10 characters (5 × 8 pixels), with minimum external components.

The SED1200 has an internal CGROM consisting of 160 characters (5 × 7) plus the underline cursor, JIS, ASCII, and four user-programmable characters in RAM.

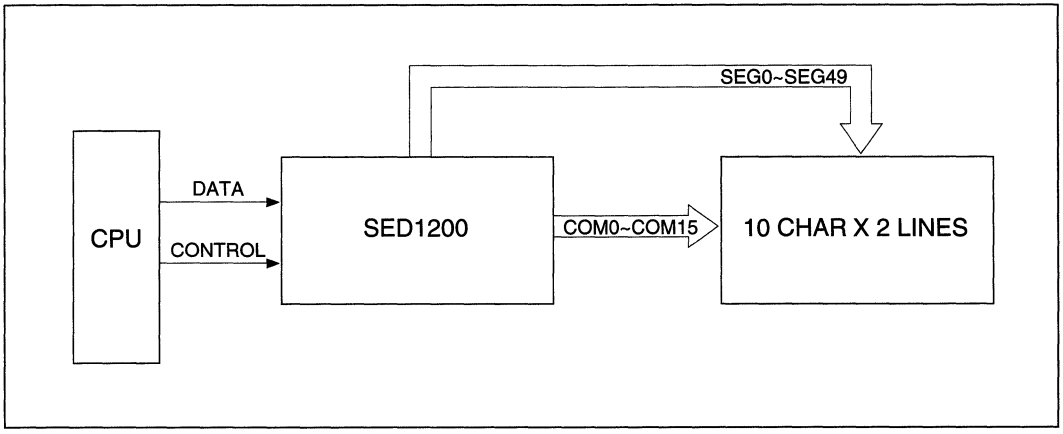
The SED1200 has 50 segment output and 16 common output built-in. Thus, one chip is capable of displaying up to 20 characters.

The device also contains the resistor array for the LCD power supply. The SED1200 is fabricated silicon gate CMOS technology process and features very low power dissipation. This makes the device suitable for hand-held and portable applications.

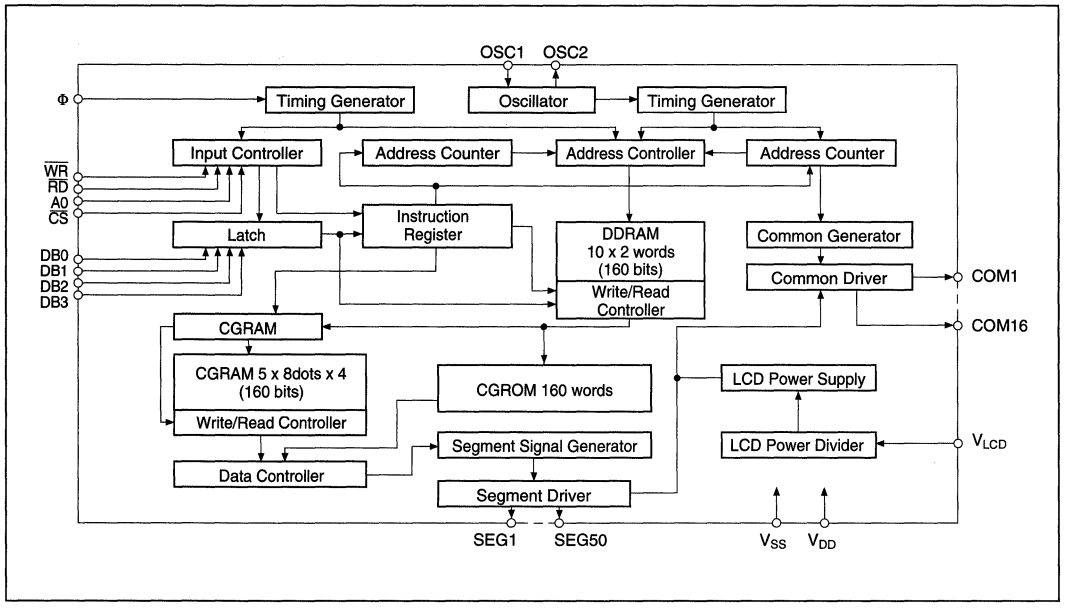
■ FEATURES

- Low-power CMOS technology
- 50 segment output
- 16 common output
- Duty: 1/8 or 1/16 (set by command)
- 4-bit CPU data interface, TTL compatible
- 13 display control commands
- CGROM: 160 characters
- CGRAM: 4 characters (5 × 8 dots)
- Display data RAM: 20 × 8 bits (20 characters)
- Built-in RC oscillator
- Built-in LCD driver voltage-divider network
- TTL compatible CPU interface
- Supply voltage: Logic: ..... 2.5V to 5.5V
  LCD: ..... 3.5V to 5.5V
- Package: ..... QFP1-80 pins (F_{0A}, F_{0B})
  QFP14-80 pins (F_{1B})
  Al pad (D_{0A}, D_{0B})

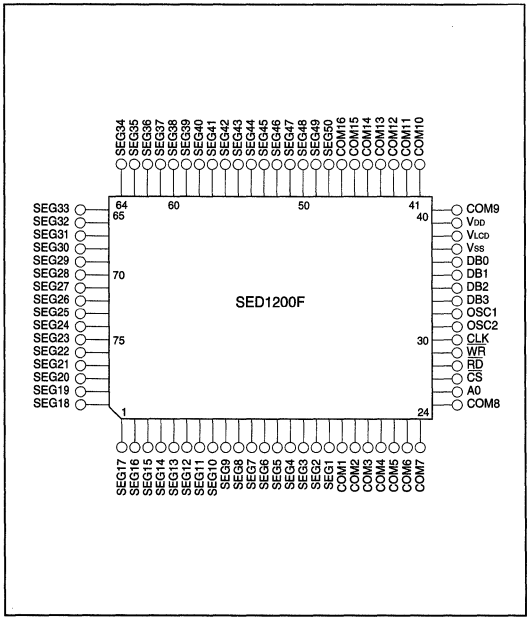
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTION

Pin No.	Pin Name	I/O	Functions
18 to 25 40 to 47	COM1 to COM16	O	LCD Common output
17 to 1 80 to 48	SEG1 to SEG50	O	LCD Segment output
27	$\overline{CS}$	I	Chip select input (active "Low")
28	$\overline{RD}$	I	Read enable input (active "Low")
29	$\overline{WR}$	I	Write enable input (active "Low" to "High")
26	A0	I	"High"; Set character code, "Low"; Command
36 to 33	DB0 to DB3	I, I/O	Data input (except DB3; Data input/output)
30	Φ	I	Clock for command
32, 31	OSC1, OSC2	—	Connect oscillation resistor*
39	VDD	—	Supply voltage (+5V) for logic
37	VSS	—	GND (0V)
38	VLCD	—	Supply voltage for LCD

* If an external clock is used, it should be connected to OSC1 and leave OSC2 open.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	−0.3 to +7.0	V
Supply voltage (2)	V_{LCD}	V_{DD}−7.0 to V_{DD}+0.3	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	−10 to +70	°C
Storage temperature	T_{stg}	−40 to +150	°C

● DC Electrical Characteristics — V_{DD} = 5V

V_{DD} = 5V, V_{SS} = 0V, T_a = −10 to +70°C

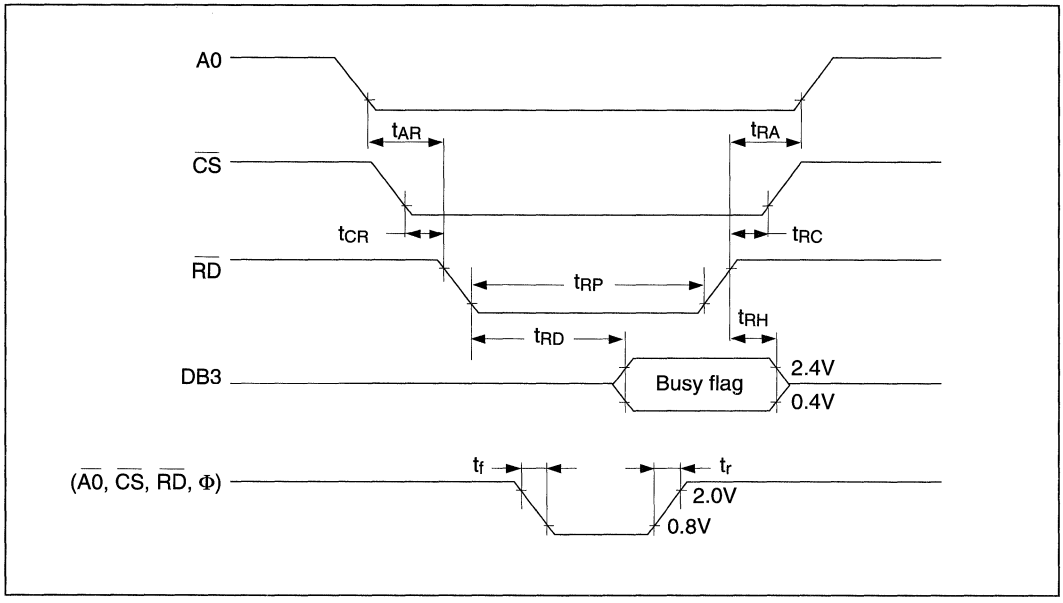
Parameter	Symbol	Conditions	Terminal	Min	Typ	Max	Unit
Logic supply voltage	V_{DD}		V_{DD}	4.5	5.0	5.5	V
Liquid crystal display supply voltage	V_{LCD}		V_{LCD}	V_{DD}−5.5	—	V_{DD}−3.5	V
Oscillator feedback resistor	R_f	V_{DD} = 5.0V, f_{OSC} = 100 kHz	OSC1, OSC2	240	310	380	kΩ
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 4.5 to 5.5V	OSC1, OSC2	—	100	300	kHz
Operating frequency (2)	Φ	V_{DD} = 4.5 to 5.5V	Φ	—	—	3.2	MHz
External clock duty		V_{DD} = 4.5 to 5.5V	OSC1, Φ	45	50	55	%
External clock rise time	t_r	V_{DD} = 4.5 to 5.5V	OSC1, Φ	—	—	50	ns
External clock fall time	t_f	V_{DD} = 4.5 to 5.5V	OSC1, Φ	—	—	50	ns
H-level input voltage (1)	V_{IH1}	V_{DD} = 4.5 to 5.5V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB3, Φ	2.0	—	V_{DD}	V
L-level input voltage (1)	V_{IL1}	V_{DD} = 4.5 to 5.5V		0	—	0.8	V
H-level input voltage (2)	V_{IH2}	V_{DD} = 4.5 to 5.5V	OSC1	0.8 V_{DD}	V_{DD}	V_{DD}	V
L-level input voltage (2)	V_{IL2}	V_{DD} = 4.5 to 5.5V		0	0	0.2 V_{DD}	V
H-level input leakage current	I_{LIH}	V_{DD} = 5.5V, V_{IH} = 5.5V	Φ, OSC1, DB0 to DB3	—	—	|−1.0|	μA
L-level input leakage current	I_{LIL}	V_{DD} = 5.5V, V_{IL} = 0V		—	—	1.0	μA
Input pull-up current	I_{IPU}	V_{DD} = 5.0V, V_{IL} = 0V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0	3.0	10	30	μA
H-level output current	I_{OH}	V_{DD} = 4.5 to 5.5V, V_{OH} = 2.4V	DB3	|−1.0|	—	—	mA
L-level output current	I_{OL}	V_{DD} = 5.5V, V_{OL} = 0.4V		1.6	—	—	mA
Common driver output current (1)	I_{OH}	V_{DD} level	V_{DD} = 4.5V, V_{LCD} = 1.0V, Voltage-divider resistor in low impedance state. 1/16 duty 0.5V voltage drop. Measured on one pin with other pins open circuit.	COM1 to COM16	|−20|	—	—	μA
Common driver output current (2)	I_{OL}	V_{LCD} level		COM1 to COM16	20	—	—	μA
Common driver output current (3)	I_{OL}	V_{L1} level		COM1 to COM16	|±8|	—	—	μA
Common driver output current (4)	I_{OL}	V_{L4} level		COM1 to COM16	|±8|	—	—	μA
Segment driver output current (1)	I_{OH}	V_{DD} level		SEG1 to SEG50	|−12|	—	—	μA
Segment driver output current (2)	I_{OL}	V_{LCD} level		SEG1 to SEG50	12	—	—	μA
Segment driver output current (3)	I_{OL}	V_{L2} level		SEG1 to SEG50	|±4|	—	—	μA
Segment driver output current (4)	I_{OL}	V_{L3} level		SEG1 to SEG50	|±4|	—	—	μA
Voltage-divider resistor (1)	R_{d1}	Normal conditions			30	130	300	kΩ
Voltage-divider resistor (2)	R_{d2}	Low impedance state			3.0	13	30	kΩ
Voltage-divider resistor low impedance duty	t_{Rd1}/t_{Rd2}	1/8 Duty 1/16 Duty		— —	11/400 11/200	— —	— —	
Command execution time	t_{comd}	From $\overline{WR}$ rising edge to the end of internal processing			—	—	16/Φ (MHz)	μs
Average operating current	I_{DD}	V_{DD} = 5.0V, V_{LCD} = 0V, f_{OSC} = 100kHz, Φ = 1MHz, $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = 5.0V, output open	V_{DD}	—	80	150	μA

● DC Electrical Characteristics — V_{DD} = 3V

V_{DD} = 3V, V_{SS} = 0V, T_a = −10 to +70°C

Parameter	Symbol	Conditions	Terminal	Min	Typ	Max	Unit
Logic supply voltage	V_{DD}		V_{DD}	2.5	3.5	4.5	V
Liquid crystal display supply voltage	V_{LCD}		V_{LCD}	V_{DD} −5.5	—	V_{DD} −3.5	V
Oscillator feedback resistor	R_f	V_{DD} = 3.0V, f_{OSC} = 100 kHz	OSC1, OSC2	2210	290	370	kΩ
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 2.5V	OSC1, OSC2	—	—	300	kHz
Operating frequency (2)	Φ	V_{DD} = 2.5V	Φ	—	—	1.0	MHz
External clock duty		V_{DD} = 2.5V	OSC1, Φ	—	50	—	%
External clock rise time	t_r	V_{DD} = 2.5V	OSC1, Φ	—	—	50	ns
External clock fall time	t_f	V_{DD} = 2.5V	OSC1, Φ	—	—	50	ns
H-level input voltage (1)	V_{IH1}	V_{DD} = 2.5V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB3, Φ	0.8 V_{DD}	—	V_{DD}	V
L-level input voltage (1)	V_{IL1}	V_{DD} = 2.5V		0	—	0.2V_{DD}	V
H-level input voltage (2)	V_{IH2}	V_{DD} = 2.5V	OSC1	0.8 V_{DD}	—	—	V
L-level input voltage (2)	V_{IL2}	V_{DD} = 2.5V		—	—	0.2 V_{DD}	V
H-level input leakage current	I_{LIH}	V_{DD} = 4.5V	Φ, OSC1, DB0 to DB3	—	—	|−1.0|	μA
L-level input leakage current	I_{LIL}	V_{DD} = 4.5V		—	—	1.0	μA
Input pull-up current	I_{IPU}	V_{DD} = 3.5V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0	1.0	4.0	15	μA
H-level output current	I_{OH}	V_{DD} = 2.5V, V_{OH} = 2.0V	DB3	200	—	—	mA
L-level output current	I_{OL}	V_{DD} = 2.5V, V_{OL} = 0.5V		200	—	—	mA
Common driver output current (1)	I_{OH}	V_{DD} level; V_{DD} − V_{LCD}= 3.5V Voltage-divider resistor in low impedance state. 1/16 duty 0.5V voltage drop Measured on one pin with other pins open circuit.	COM1 to COM16	|−20|	—	—	μA
Common driver output current (2)	I_{OL}	V_{LCD} level	COM1 to COM16	20	—	—	μA
Common driver output current (3)	I_{OL}	V_{L1} level	COM1 to COM16	|±8|	—	—	μA
Common driver output current (4)	I_{OL}	V_{L4} level	COM1 to COM16	|±8|	—	—	μA
Segment driver output current (1)	I_{OH}	V_{DD} level	SEG1 to SEG50	|−12|	—	—	μA
Segment driver output current (2)	I_{OL}	V_{LCD} level	SEG1 to SEG50	12	—	—	μA
Segment driver output current (3)	I_{OL}	V_{L2} level	SEG1 to SEG50	|±4|	—	—	μA
Segment driver output current (4)	I_{OL}	V_{L3} level	SEG1 to SEG50	|±4|	—	—	μA
Voltage-divider resistor (1)	R_{d1}	Normal conditions		—	130	—	kΩ
Voltage-divider resistor (2)	R_{d2}	Low impedance state		—	13	—	kΩ
Voltage-divider resistor low impedance duty	t_{Rd1}/t_{Rd2}	1/8 Duty	—	11/400	—	—	—
		1/16 Duty	—	11/200	—	—	
Command execution time	t_{comd}	From $\overline{WR}$ rise time to the end of internal processing		—	—	16/Φ (MHz)	μs
Average operating current	I_{DD}	V_{DD} − V_{SS} = 3.5V, V_{DD} − V_{LCD} = 1.5V, f_{OSC} = 100kHz, Φ = 500 kHz, $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = V_{DD}, output open	V_{DD}	—	60	150	μA

- **AC Electrical Characteristics**
  - **MPU Read Timing**



V_{DD} = 4.5 to 5.5V, T_a = –10 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Setup time for A0 → $\overline{RD}$	t_{AR}	—	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	—	0	—	—	ns
$\overline{RD}$ delay output time	t_{RD}	—	—	—	250	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	—	20	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	—	20	—	—	ns
Data hold time	t_{RH}	—	10	—	—	ns
Read pulsewidth	t_{RP}	—	350	—	—	ns
Input fall time	t_f	—	—	—	50	ns
Input rise time	t_r	—	—	—	50	ns

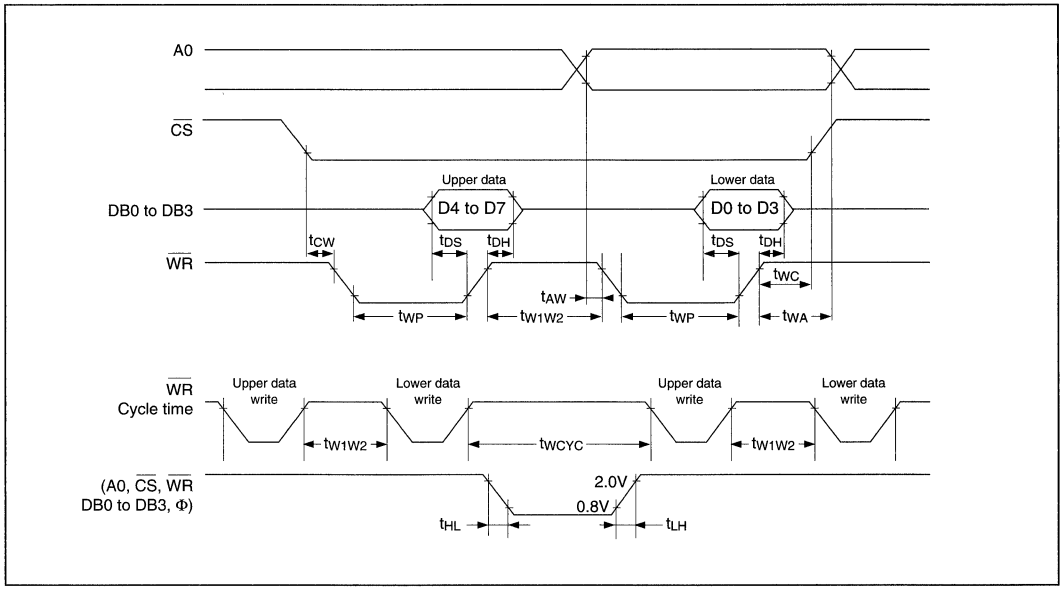
Note: Load on pin DB3 is C_L = 100 pF.

V_{DD} = 2.5 to 4.5V, T_a = –10 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Setup time for A0 → $\overline{RD}$	t_{AR}	—	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	—	0	—	—	ns
$\overline{RD}$ delay output time	t_{RD}	—	—	—	350	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	—	0	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	—	0	—	—	ns
Data hold time	t_{RH}	—	10	—	—	ns
Read pulsewidth	t_{RP}	—	400	—	—	ns
Input fall time	t_f	—	—	—	50	ns
Input rise time	t_r	—	—	—	50	ns

Note: Load on pin DB3 is C_L = 100 pF.

○ MPU Write Timing



V_{DD} = 5V, T_a = –10 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
A0 → $\overline{WR}$ setup time	t_{AW}	—	0	—	—	ns
$\overline{CS}$ → $\overline{WR}$ setup time	t_{CW}	—	0	—	—	ns
Data setup time	t_{DS}	—	120	—	—	ns
$\overline{WR}$ → A0 hold time	t_{WA}	—	20	—	—	ns
$\overline{WR}$ → $\overline{CS}$ hold time	t_{WC}	—	20	—	—	ns
Data hold time	t_{DH}	—	20	—	—	ns
Write pulsewidth	t_{WP}	—	200	—	—	ns
Upper write pulse rising edge to lower write pulse falling edge time	t_{W1W2}	—	200	—	—	ns
Lower write pulse rising edge to upper write pulse falling edge time	t_{WCYC}	—	16/Φ (MHz)	—	—	ns
Input fall time	t_f	—	—	—	50	ns
Input rise time	t_r	—	—	—	50	ns

V_{DD} = 3V, T_a = –10 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
A0 → $\overline{WR}$ setup time	t_{AW}	—	0	—	—	ns
$\overline{CS}$ → $\overline{WR}$ setup time	t_{CW}	—	0	—	—	ns
Data setup time	t_{DS}	—	120	—	—	ns
$\overline{WR}$ → A0 hold time	t_{WA}	—	0	—	—	ns
$\overline{WR}$ → $\overline{CS}$ hold time	t_{WC}	—	0	—	—	ns
Data hold time	t_{DH}	—	100	—	—	ns
Write pulsewidth	t_{WP}	—	200	—	—	ns
Upper write pulse rising edge to lower write pulse falling edge time	t_{W1W2}	—	200	—	—	ns
Lower write pulse rising edge to upper write pulse falling edge time	t_{WCYC}	—	16/Φ (MHz)	—	—	ns
Input fall time	t_f	—	—	—	50	ns
Input rise time	t_r	—	—	—	50	ns

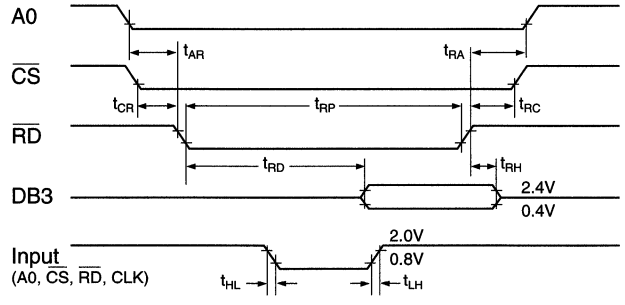
● AC Characteristics (Write cycle)

(V_{DD} = 5V±10%, V_{SS} = 0V, T_a = −10 to +70°C)

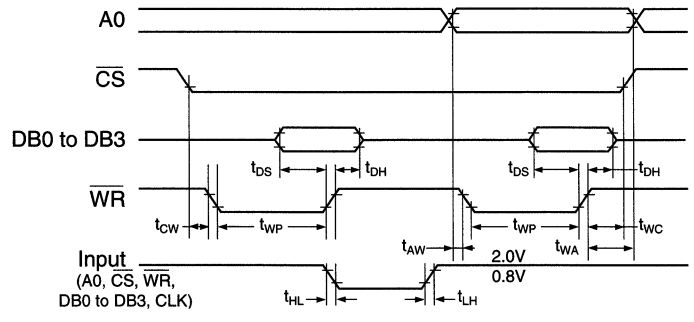
Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
A0 setup time to $\overline{WR}$	t_{AW}		0	—	—	ns
$\overline{CS}$ setup time to $\overline{WR}$	t_{CW}		0	—	—	ns
Data setup time	t_{DS}		120	—	—	ns
A0 hold time after $\overline{WR}$	t_{WA}		20	—	—	ns
$\overline{CS}$ hold time after $\overline{WR}$	t_{WC}		20	—	—	ns
Data hold time	t_{DH}		20	—	—	ns
Write pulse width	t_{WP}		200	—	—	ns
Input fall time	t_{HL}		—	—	50	ns
Input rise time	t_{LH}		—	—	50	ns

● Timing Chart

○ Read cycle



○ Write cycle



● DC Characteristics

○ V_{DD} = 5V

(V_{SS} = 0V, T_a = −10 to +70°C)

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Logic operating voltage	V_{DD}		4.5	5	5.5	V
LCD operating voltage	V_{LCD}		V_{DD}–5.5	—	V_{DD}–3.5	V
Resistor for oscillator	R_f	V_{DD}=5V, f_{OSC}=100kHz	240	310	380	kΩ
Input voltage ; High (1)	V_{IH1}	V_{DD}=4.5 to 5.5V *1	2.0	—	V_{DD}	V
Input voltage ; Low (1)	V_{IL1}	V_{DD}=4.5 to 5.5V *1	0	—	0.8	V
Input leakage current ; High	I_{LIH}	V_{DD}=5.5V, V_{IH}=5.5V *2	—	—	1.0	µA
Input leakage current ; Low	I_{LIL}	V_{DD}=5.5V, V_{IL}=0V *2	—	—	1.0	µA
Input voltage ; High (2)	V_{IH2}	V_{DD}=4.5 to 5.5V *3	0.8V_{DD}	V_{DD}	V_{DD}	V
Input voltage ; Low (2)	V_{IL2}	V_{DD}=4.5 to 5.5V *3	0	0	0.2V_{DD}	V
Output current ; High	I_{OH}	V_{DD}=5V, V_{OH}=2.4V *4	1.0	—	—	mA
Output current ; Low	I_{OL}	V_{DD}=5V, V_{OL}=0.4V *4	1.6	—	—	mA
Input pull up current	I_{IPU}	V_{IL}=0V, V_{DD}=5V *5	3	10	30	µA
Resistor as power divider	R_d		30	130	300	kΩ
Operating frequency (1)	f_{OSC}	V_{DD}=4.5 to 5.5V	—	100	300	kHz
Operating frequency (2)	CLK	V_{DD}=4.5 to 5.5V	—	—	3.2	MHz
Operating current	I_{DD}	V_{DD}=5V, V_{LCD}=0V *6 f_{OSC}=100KHz, CLK=1MHz	—	80	150	µA
Command execution time	t_{COMD}		—	—	16/CLK (MHz)	µs
Common output current (1)	$\|I_{OH}\ V_{DDC}\|$	V_{DD}=4.5V V_{LCD}=1.0V 1/16 duty drive Voltage drop by 0.5V When one terminal is measured, the others are open.	20	—	—	µA
Common output current (2)	$I_{OL}\ V_{LCDC}$		20	—	—	µA
Common output current (3)	$\|I_{OL}\ V_{L1C}\|$		8	—	—	µA
Common output current (4)	$\|I_{OL}\ V_{L4C}\|$		8	—	—	µA
Segment output current (1)	$\|I_{OL}\ V_{DDS}\|$		12	—	—	µA
Segment output current (2)	$I_{OL}\ V_{LCDS}$		12	—	—	µA
Segment output current (3)	$\|I_{OL}\ V_{L2S}\|$		4	—	—	µA
Segment output current (4)	$\|I_{OL}\ V_{L3S}\|$		4	—	—	µA

*1. Terminal: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, DB0 to DB3, CLK

*2. Terminal: CLK, OSC1, DB0 to DB3

*3. Terminal: OSC1 (for external clock)

*4. Terminal: DB3

*5. Terminal: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0

*6. $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = 5.0V, (open output terminals)

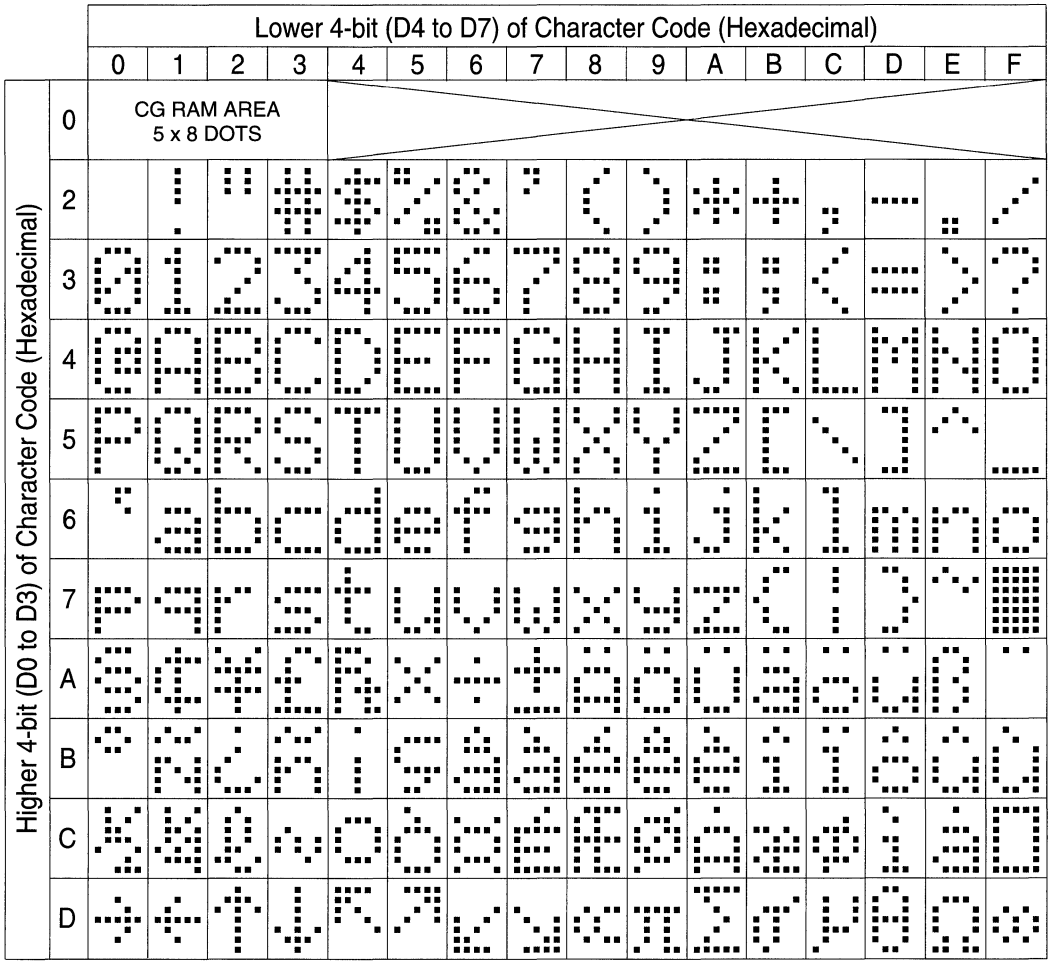
■ DISPLAY COMMAND

Command Name		$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A0	1st input DB3 (D7)	DB2 (D6)	DB1 (D5)	DB0 (D4)	2nd input DB3 (D3)	DB2 (D2)	DB1 (D1)	DB0 (D0)	Note
SET CURSOR DIRECTION		0	0	1	0	0	0	0	0	0	1	0	D/I	D0=1: Decrement D0=0: Increment
CURSOR ADDRESS –1/+1		0	0	1	0	0	0	0	0	0	1	1	–1/+1	D0=1: –1 D0=0: +1
CURSOR FONT SELECT		0	0	1	0	0	0	0	0	1	0	0	A/U	D0=1: All dots blinking D0=0: Under line
CURSOR BLINK ON/OFF		0	0	1	0	0	0	0	0	1	0	1	ON/OFF	D0=1: ON D0=0: OFF
DISPLAY ON/OFF		0	0	1	0	0	0	0	0	1	1	0	ON/OFF	D0=1: ON D0=0: OFF
CURSOR ON/OFF		0	0	1	0	0	0	0	0	1	1	1	ON/OFF	D0=1: ON D0=0: OFF
SYSTEM RESET		0	0	1	0	0	0	0	1	0	0	0	0	Except data RAM and CGRAM
LINE SELECT		0	0	1	0	0	0	0	1	0	0	1	2/1	D0=1: 2 line display (1/16 duty) D0=0: 1 line display (1/8 duty)
SET CURSOR ADDRESS	1st LINE	0	0	1	0	1	0	(N figure-1) B						
	2nd LINE	0	0	1	0	1	1	(N figure-1) B						
SET CHARACTER CODE		0	0	1	1	(CHARACTER CODE)								
BUSY FLAG CHECK		0	1	0	0	BF	*	*	*	BF	*	*	*	D7(D3)=1: Busy D7(D3)=0: Not Busy
SET CGRAM ADDRESS		0	0	1	0	0	0	1	0	(Set lower address)				
SET CGRAM DATA		0	0	1	0	0	1	0	(Set CGRAM data)					

* = High impedance

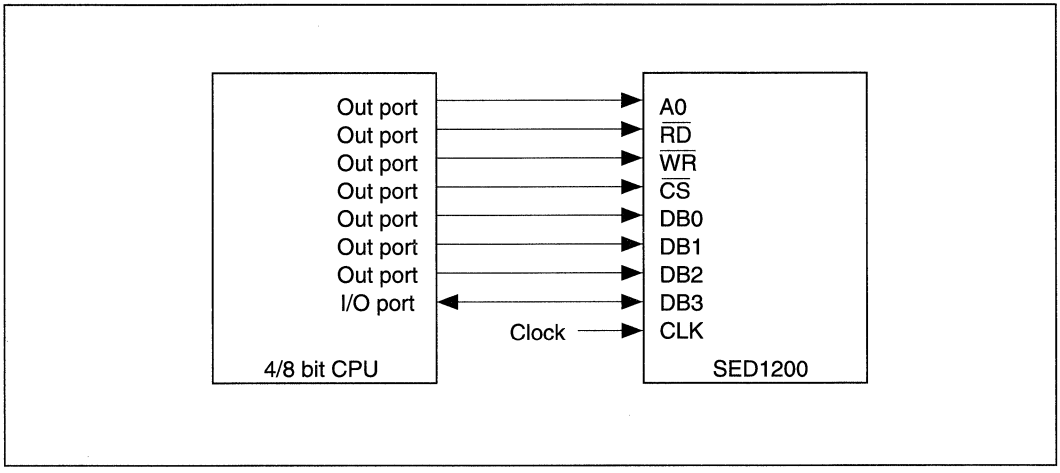
Note: Misoperation may be caused when any command other than that listed in the above table is inputted.

■ CHARACTER CODE MAP (SED1200F0B)



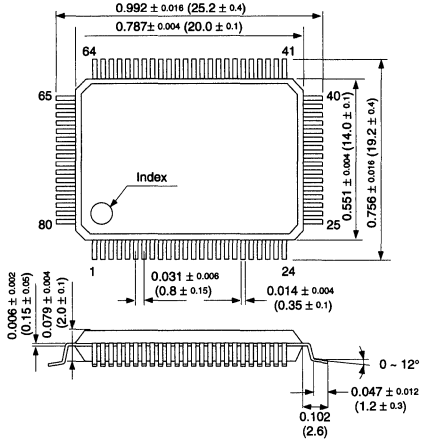
■ APPLICATION FOR CPU

The SED1200 can connect to the address bus or the data bus directly, as shown below.

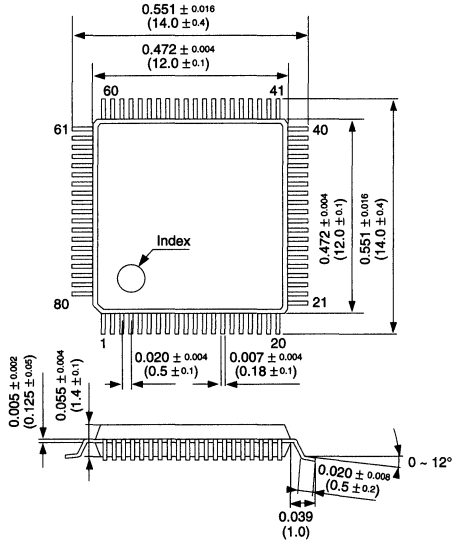


■ SED1200F PACKAGE DIMENSIONS

Plastic QFP1-80 pins
SED1200F0B



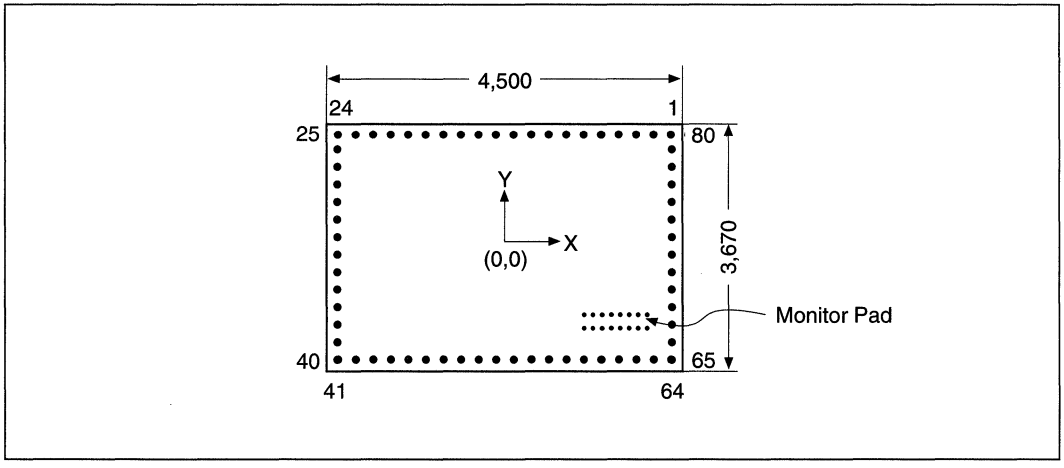
Plastic QFP14-80 pins
SED1200F1B



■ SED1200D PACKAGE DIMENSIONS

Chip size:	5.86 mm x 3.41 mm
Chip thickness:	0.40 mm x 0.03 mm
Pad size:	0.90 mm x 0.90 mm
Pad pitch:	0.19 mm

■ PAD LAYOUT



● PAD COORDINATES

unit: μm

Pad No.	Pad Name	X (μm)	Y (μm)
1	SEG17	2123	1552
2	SEG16	1932	1552
3	SEG15	1742	1552
4	SEG14	1551	1552
5	SEG13	1361	1552
6	SEG12	1170	1552
7	SEG11	980	1552
8	SEG10	789	1552
9	SEG9	599	1552
10	SEG8	408	1552
11	SEG7	218	1552
12	SEG6	27	1552
13	SEG5	–163	1552
14	SEG4	–354	1552
15	SEG3	–544	1552
16	SEG2	–735	1552
17	SEG1	–925	1552
18	COM1	–1116	1552
19	COM2	–1306	1552
20	COM3	–1497	1552
21	COM4	–1687	1552
22	COM5	–1878	1552
23	COM6	–2068	1552
24	COM7	–2259	1552
25	COM8	–2778	1429
26	A0	–2778	1238
27	$\overline{CS}$	–2778	1048
28	$\overline{RD}$	–2778	857
29	$\overline{WR}$	–2778	667
30	Φ	–2778	476
31	OSC2	–2778	286
32	OSC1	–2778	95
33	D3	–2778	–95
34	D2	–2778	–286
35	D1	–2778	–476
36	D0	–2778	–667
37	V_{SS}	–2778	–857
38	V_{LCD}	–2778	–1048
39	V_{DD}	–2778	–1238
40	COM9	–2778	–1429

Pad No.	Pad Name	X (μm)	Y (μm)
41	COM10	–2220	–1552
42	COM11	–2029	–1552
43	COM12	–1839	–1552
44	COM13	–1648	–1552
45	COM14	–1458	–1552
46	COM15	–1267	–1552
47	COM16	–1077	–1552
48	SEG50	–886	–1552
49	SEG49	–696	–1552
50	SEG48	–505	–1552
51	SEG47	–315	–1552
52	SEG46	–124	–1552
53	SEG45	66	–1552
54	SEG44	257	–1552
55	SEG43	447	–1552
56	SEG42	638	–1552
57	SEG41	828	–1552
58	SEG40	1019	–1552
59	SEG39	1209	–1552
60	SEG38	1400	–1552
61	SEG37	1590	–1552
62	SEG36	1781	–1552
63	SEG35	1971	–1552
64	SEG34	2162	–1552
65	SEG33	2777	–1385
66	SEG32	2777	–1195
67	SEG31	2777	–1004
68	SEG30	2777	–814
69	SEG29	2777	–623
70	SEG28	2777	–433
71	SEG27	2777	–242
72	SEG26	2777	–52
73	SEG25	2777	139
74	SEG24	2777	329
75	SEG23	2777	520
76	SEG22	2777	710
77	SEG21	2777	901
78	SEG20	2777	1091
79	SEG19	2777	1282
80	SEG18	2777	1472

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CMOS DOT MATRIX LCD CONTROLLER DRIVER

■ DESCRIPTION

The SED1210 is a character LCD controller-driver, capable of driving displays as large as 2 lines of 8 character (5 × 8 pixels), with minimum external components.

The SED1210 has an internal CGROM consisting of 160 characters (5 × 7) plus the underline cursor, JIS, ASCII, and four user-programmable characters in RAM.

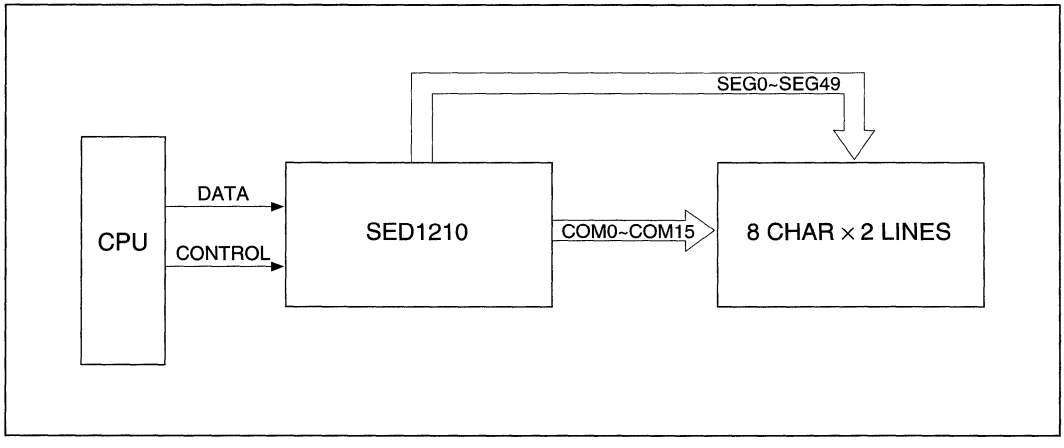
The SED1210 has 40 segment output and 16 common output built-in. Thus, one chip is capable of displaying up to 16 characters. The SED1210 can display one line of 40 characters using an SED1181FLA (64 bits) as an expansion segment driver.

The SED1210 is fabricated using a silicon gate CMOS technology process and features very low power dissipation. This makes the device suitable for handheld and portable applications.

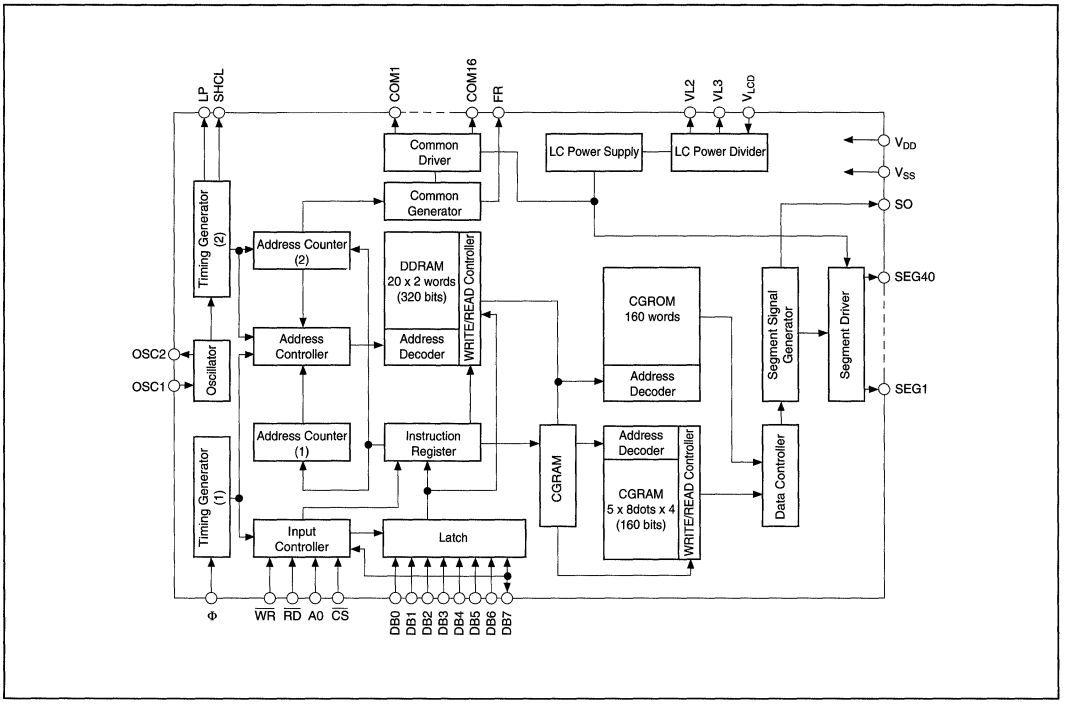
■ FEATURES

- Low-power CMOS technology
- 40 segment output
- 16 common output
- Duty: 1/8 or 1/16 (set by command)
- 8-bit CPU data interface, TTL compatible
- 13 display control commands
- CGROM: 160 characters
- CGRAM: 4 characters
- Display data RAM: 40 × 8 bits (40 characters)
- Built-in RC oscillator
- Built-in LCD driver voltage-divider network
- TTL compatible CPU interface
- Supply voltage ..... Logic: 2.5V to 5.5V
  LCD: 3.5V to 5.5V
- Package ..... QFP5-80 pins (FOB, FOA)
  Al pad (DOA)
  Au bump (DOB)

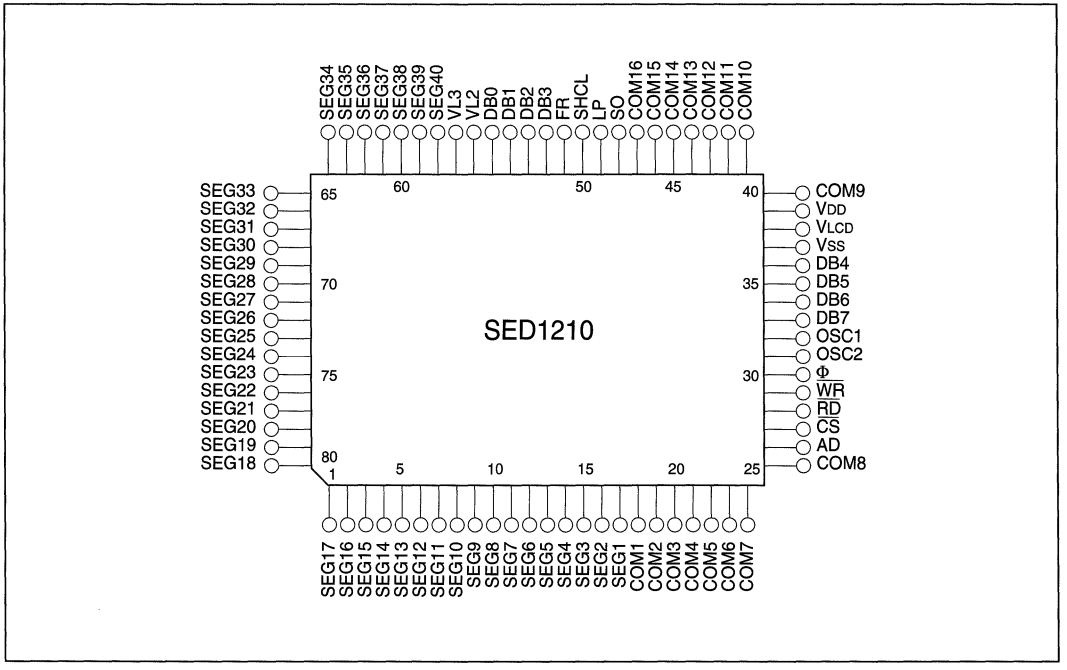
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTION

Pin Name	Functions	No. of Pin
COM1 to 16	LCD common output	16
SEG1 to 40	LCD segment output	40
$\overline{CS}$	Chip select input (active "Low")	1
$\overline{RD}$	Read enable input (active "Low")	1
$\overline{WR}$	Write enable input (active "Low" to "High")	1
A0	"High" ; Display data "Low" ; Command	1
DB0 to 7	Data input (except DB7 ; Data input/output)	8
Φ	Clock for command execution	1

Pin Name	Functions	No. of Pin
OSC1, OSC2	Connect oscillation resistor between OSC1 and OSC2. OSC1 also can be external clock input.	2
SO	Serial output for Segment driver	1
LP	Latch output for Segment driver	1
SHCL	Shift clock for Segment driver	1
FR	Frame output for Segment driver	1
VL2, VL3	Supply voltage for Segment driver	2
V_{DD}	Supply voltage (2.5V to 5.5V) for logic	1
V_{SS}	GND (0V)	1
V_{LCD}	Supply voltage for LCD $3.5V \leq V_{DD}-V_{LCD} \leq 5.5V$	1

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V, T_a = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to 7.0	V
Supply voltage (2)	V_{LCD}	V_{DD}–7.0 to V_{DD}+0.3	V
Input voltage	V_I	–0.3 to V_{DD}+0.3	V
Output voltage	V_O	–0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	–20 to 70	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C•10s (at lead)	—

■ DC CHARACTERISTICS

● V_{DD} = 5V

V_{SS} = 0V, T_a = –20 to +70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Pin
Liquid crystal display supply voltage	V_{LCD}		V_{DD} – 5.5	—	V_{DD} – 3.5	V	V_{LCD}
Oscillator feedback resistor	R_f	V_{DD} = 5.0V, f_{OSC} = 100kHz	240	310	380	kΩ	OSC1, OSC2
Oscillator frequency	f_{OSC}	V_{DD} = 5.0V, R_f = 300kΩ	—	100	—	kHz	OSC1, OSC2
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 4.5V	—	—	300	kHz	OSC1
Operating frequency (2)	Φ	V_{DD} = 4.5 to 5.5V	—	—	3.2	MHz	Φ
External clock duty		V_{DD} = 4.5 to 5.5V	45	50	55	%	OSC1, Φ
External clock rise time	t_r	V_{DD} = 4.5 to 5.5V	—	—	50	ns	OSC1, Φ
External clock fall time	t_f	V_{DD} = 4.5 to 5.5V	—	—	50	ns	OSC1, Φ
H-level input voltage (1)	V_{IH1}	V_{DD} = 4.5 to 5.5V	2.0	—	V_{DD}	V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB7, Φ, A0
L-level input voltage (1)	V_{IL1}	V_{DD} = 4.5 to 5.5V	0	—	0.8	V	
H-level input voltage (2)	V_{IH2}	V_{DD} = 4.5 to 5.5V	0.8 × V_{DD}	V_{DD}	V_{DD}	V	OSC1
L-level input voltage (2)	V_{IL2}	V_{DD} = 4.5 to 5.5V	0	0	0.2 × V_{DD}	V	OSC1
H-level input leakage current	I_{LIH}	V_{DD} = 5.5V, V_{IH} = 5.5V	—	—	|–1.0|	μA	Φ, OSC1, DB0 to DB7
L-level input leakage current	I_{LIL}	V_{DD} = 5.5V, V_{IL} = 0V	—	—	1.0	μA	Φ, OSC1, DB0 to DB7
Input pull-up current	I_{IPU}	V_{DD} = 5.0V, V_{IL} = 0V	3.0	10	30	μA	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0
H-level output current (1)	I_{OH1}	V_{DD} = 4.5 to 5.5V, V_{OH} = 2.4V	|–1.0|	—	—	mA	DB7
L-level output current (1)	I_{OL1}	V_{DD} = 4.5 to 5.5V, V_{OL} = 0.4V	1.6	—	—	mA	DB7
H-level output current (2)	I_{OH2}	V_{DD} = 4.5V, V_{OH} = 4.0V	200	—	—	μA	FR, LP
L-level output current (2)	I_{OL2}	V_{DD} = 4.5V, V_{OL} = 0.5V	200	—	—	μA	XSCL, SO
Common driver output current (1)	I_{OH}	V_{DD} level; V_{DD} – V_{LCD} = 3.5V. Dividing resistor in low impedance state. 1/16 duty. 0.5 voltage drop. Measured on one pin with other pins open circuit.	|–20|	—	—	μA	COM1 to COM 16
Common driver output current (2)	I_{OL}	V_{LCD} level	20	—	—	μA	
Common driver output current (3)	I_{OL}	V_{L1} level	|±8|	—	—	μA	
Common driver output current (4)	I_{OL}	V_{L4} level	|±8|	—	—	μA	
Segment driver output current (1)	I_{OH}	V_{DD} level	|–12|	—	—	μA	SEG1 to SEG40
Segment driver output current (2)	I_{OL}	V_{LCD} level	12	—	—	μA	
Segment driver output current (3)	I_{OL}	V_{L2} level	|±4|	—	—	μA	
Segment driver output current (4)	I_{OL}	V_{L3} level	|±4|	—	—	μA	
Driver current	I_{OH}	V_{DD} – V_{LCD} = 3.5V 0.5V voltage drop	—	2	—	μA	V_{L2}, V_{L3}
	I_{OL}		—	2	—	μA	
Voltage-divider resistor (1)	R_{d1}	Normal conditions	30	130	300	kΩ	
Voltage-divider resistor (2)	R_{d2}	Low impedance state	3.0	13	30	kΩ	
Voltage-divider resistor low impedance duty	t_{Rd1}/ t_{Rd2}	1/8 duty	—	11/400	—	—	
		1/16 duty	—	11/200	—	—	
Command execution time	t_{comd}	From $\overline{WR}$ rising edge to the end of internal processing	—	—	16/Φ	μs	
Average operating current	I_{DD}	V_{DD} = 5.0V, V_{LCD} = 0V, f_{OSC} = 100 kHz, Φ = 1 MHz, $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = 5.0V, output open	—	80	150	μA	V_{DD}

● **V_{DD} = 3V**

V_{SS} = 0V, T_a = –20 to +70°C

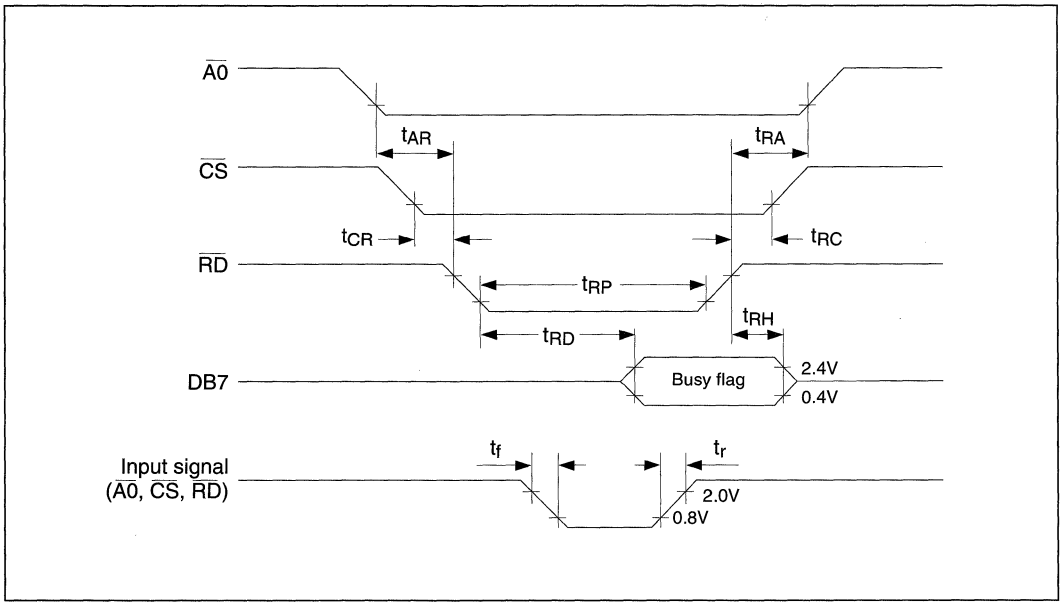
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Pin
Liquid crystal display supply voltage	V_{LCD}		3.5	—	5.5	V	V_{LCD}
Oscillator feedback resistor	R_f	V_{DD} = 3.0V, f_{OSC} = 100kHz	210	290	370	kΩ	OSC1, OSC2
Oscillator frequency	f_{OSC}	V_{DD} = 3.0V, R_f = 300kΩ	—	100	—	kHz	OSC1, OSC2
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 2.5V	—	—	300	kHz	OSC1
Operating frequency (2)	Φ	V_{DD} = 2.5 to 4.5V	—	—	1	MHz	Φ
External clock duty		V_{DD} = 2.5 to 4.5V	—	50	—	%	OSC1, Φ
External clock rise time	t_r	V_{DD} = 2.5 to 4.5V	—	—	50	ns	OSC1, Φ
External clock fall time	t_f	V_{DD} = 2.5 to 4.5V	—	—	50	ns	OSC1, Φ
H-level input voltage (1)	V_{IH1}	V_{DD} = 2.5 to 4.5V	0.8 × V_{DD}	—	—	V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB7, Φ, A0
L-level input voltage (1)	V_{IL1}	V_{DD} = 2.5 to 4.5V	—	—	0.2 × V_{DD}	V	
H-level input voltage (2)	V_{IH2}	V_{DD} = 2.5 to 4.5V	0.8 × V_{DD}	—	—	V	OSC1
L-level input voltage (2)	V_{IL2}	V_{DD} = 2.5 to 4.5V	—	—	0.2 × V_{DD}	V	OSC1
H-level input leakage current	I_{LIH}	V_{DD} = 4.5V	—	—	—	µA	Φ, OSC1, DB0 to DB7
L-level input leakage current	I_{LIL}	V_{DD} = 4.5V	—	—	—	µA	Φ, OSC1, DB0 to DB7
Input pull-up current	I_{IPU}	V_{DD} = 3.5V	—	—	—	µA	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0
H-level output current (1)	I_{OH1}	V_{DD} = 2.5V, V_{OH} = 2.0V	200	—	—	µA	DB7
L-level output current (1)	I_{OL1}	V_{DD} = 2.5V, V_{OL} = 0.5V	200	—	—	µA	DB7
H-level output current (2)	I_{OH2}	V_{DD} = 2.5V, V_{OH} = 2.0V	200	—	—	µA	FR, LP
L-level output current (2)	I_{OL2}	V_{DD} = 2.5V, V_{OL} = 0.5V	200	—	—	µA	XSCL, SO
Common driver output current (1)	I_{OH}	V_{DD} level	|–20|	—	—	µA	COM1 to COM16
Common driver output current (2)	I_{OL}	V_{LCD} level	20	—	—	µA	
Common driver output current (3)	I_{OL}	V_{L1} level	|±8|	—	—	µA	
Common driver output current (4)	I_{OL}	V_{L4} level	|±8|	—	—	µA	
Segment driver output current (1)	I_{OH}	V_{DD} level	|–12|	—	—	µA	SEG1 to SEG40
Segment driver output current (2)	I_{OL}	V_{LCD} level	12	—	—	µA	
Segment driver output current (3)	I_{OL}	V_{L2} level	|±4|	—	—	µA	
Segment driver output current (4)	I_{OL}	V_{L3} level	|±4|	—	—	µA	

Common driver / segment driver output current rows: V_{DD} – V_{LCD} = 3.5V. Dividing resistor in low impedance state. 1/16 duty. 0.5 voltage drop. Measured on one pin with other pins open circuit.

Driver current (1)	I_{OH}	V_{DD} – V_{LCD} = 3.5V 0.5V voltage drop	—	2	—	µA	V_{L2}, V_{L3}
Driver current (2)	I_{OL}		—	2	—	µA	
Voltage-divider resistor (1)	R_{d1}	Normal conditions	—	130	—	kΩ	
Voltage-divider resistor (2)	R_{d2}	Low impedance state	—	13	—	kΩ	
Voltage-divider resistor low impedance duty	t_{Rd1}/ t_{Rd2}	1/8 duty	—	11/400	—	—	
		1/16 duty	—	11/200	—	—	
Command execution time	t_{comd}	From $\overline{WR}$ rise time to the end of internal processing	—	—	16/Φ	µs	
Average operating current	I_{DD}	V_{DD} – V_{SS} = 3.5V, V_{DD} – V_{LCD} = 5V, Φ = 500kHz, $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ =A0 = V_{DD}, R_f = 300kΩ	—	60	—	µA	V_{DD}

■ AC CHARACTERISTICS

● MPU Read Timing



V_{DD} = 5V, T_a = –20 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Setup time for A0 → $\overline{RD}$	t_{AR}	—	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	—	0	—	—	ns
$\overline{RD}$ delay output time*	t_{RD}	—	—	—	200	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	—	20	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	—	20	—	—	ns
Data hold time	t_{RH}	—	10	—	—	ns
Read pulsewidth	t_{RP}	—	300	—	—	ns
Input fall time	t_f	—	—	—	50	ns
Input rise time	t_r	—	—	—	50	ns

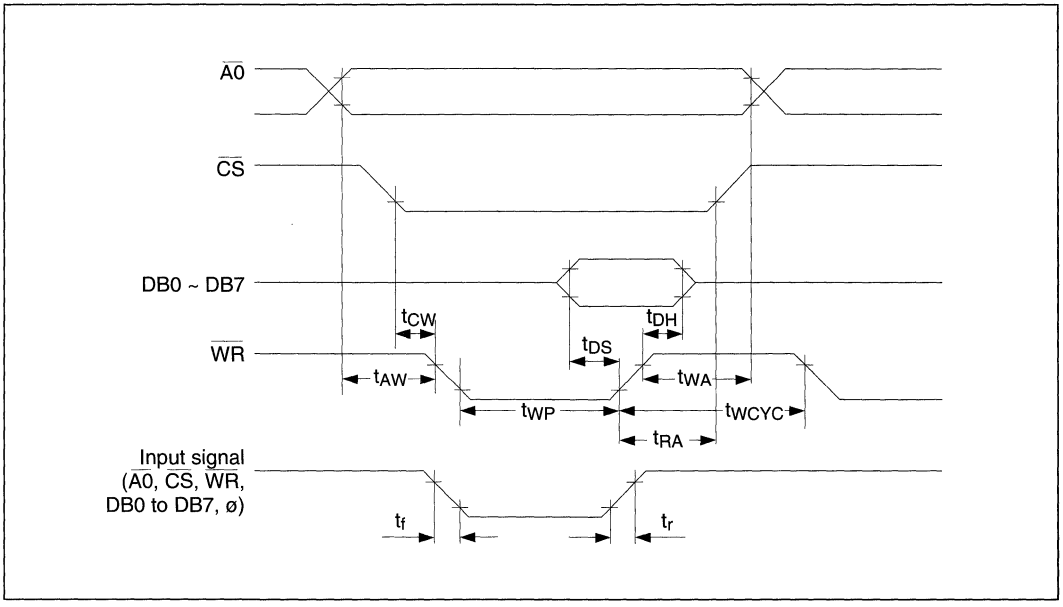
Note: Load on pin DB7 is C_L = 100 pF.

V_{DD} = 3V, T_a = –20 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Setup time for A0 → $\overline{RD}$	t_{AR}	—	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	—	0	—	—	ns
$\overline{RD}$ delay output time*	t_{RD}	—	—	—	350	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	—	0	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	—	0	—	—	ns
Data hold time	t_{RH}	—	10	—	—	ns
Read pulsewidth	t_{RP}	—	400	—	—	ns
Input fall time	t_f	—	—	—	50	ns
Input rise time	t_r	—	—	—	50	ns

Note: Load on pin DB7 is C_L = 100 pF.

● MPU Write Timing



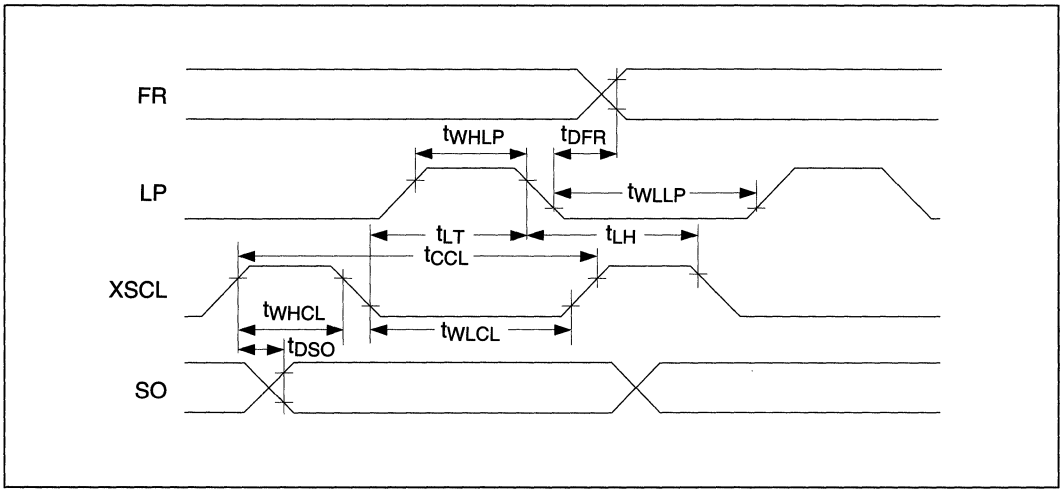
V_{DD} = 5V, T_a = –20 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
A0 → WR setup time	t_{AW}	—	0	—	—	ns
CS → WR setup time	t_{CW}	—	0	—	—	ns
Data setup time	t_{DS}	—	120	—	—	ns
WR → A0 hold time	t_{WA}	—	20	—	—	ns
WR → CS hold time	t_{WC}	—	20	—	—	ns
Data hold time	t_{DH}	—	20	—	—	ns
Write pulsewidth	t_{WP}	—	200	—	—	ns
Write cycle	t_{WCYC}	—	16/Φ	—	—	µs
Input fall time	t_f	—	—	—	50	ns
Input rise time	t_r	—	—	—	50	ns

V_{DD} = 3V, T_a = –20 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
A0 → WR setup time	t_{AW}	—	0	—	—	ns
CS → WR setup time	t_{CW}	—	0	—	—	ns
Data setup time	t_{DS}	—	120	—	—	ns
WR → A0 hold time	t_{WA}	—	0	—	—	ns
WR → CS hold time	t_{WC}	—	0	—	—	ns
Data hold time	t_{DH}	—	100	—	—	ns
Write pulsewidth	t_{WP}	—	200	—	—	ns
Write cycle	t_{WCYC}	—	16/Φ	—	—	µs
Input fall time	t_f	—	—	—	50	ns
Input rise time	t_r	—	—	—	50	ns

● X-Driver Control Timing



V_{DD} = 2.5 to 5.5V, T_a = –20 to 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Shift clock cycle	t_{CCL}	—	3.3	10	—	µs
Shift clock "H" pulsewidth	t_{WHCL}	—	1.0	—	—	µs
Shift clock "L" pulsewidth	t_{WLCL}	—	1.0	—	—	µs
Delay time for XSCL rise → SO output	t_{DSO}	—	—	—	1	µs
Latch pulse "H" pulsewidth	t_{WHLP}	—	1.0	—	—	µs
Latch pulse "L" pulsewidth	t_{WLLP}	—	300	—	—	ns
Latch time	t_{LT}	—	500	—	—	ns
Latch hold time	t_{LH}	—	500	—	—	ns
Delay time for frame signal	t_{DFR}	—	—	—	500	ns

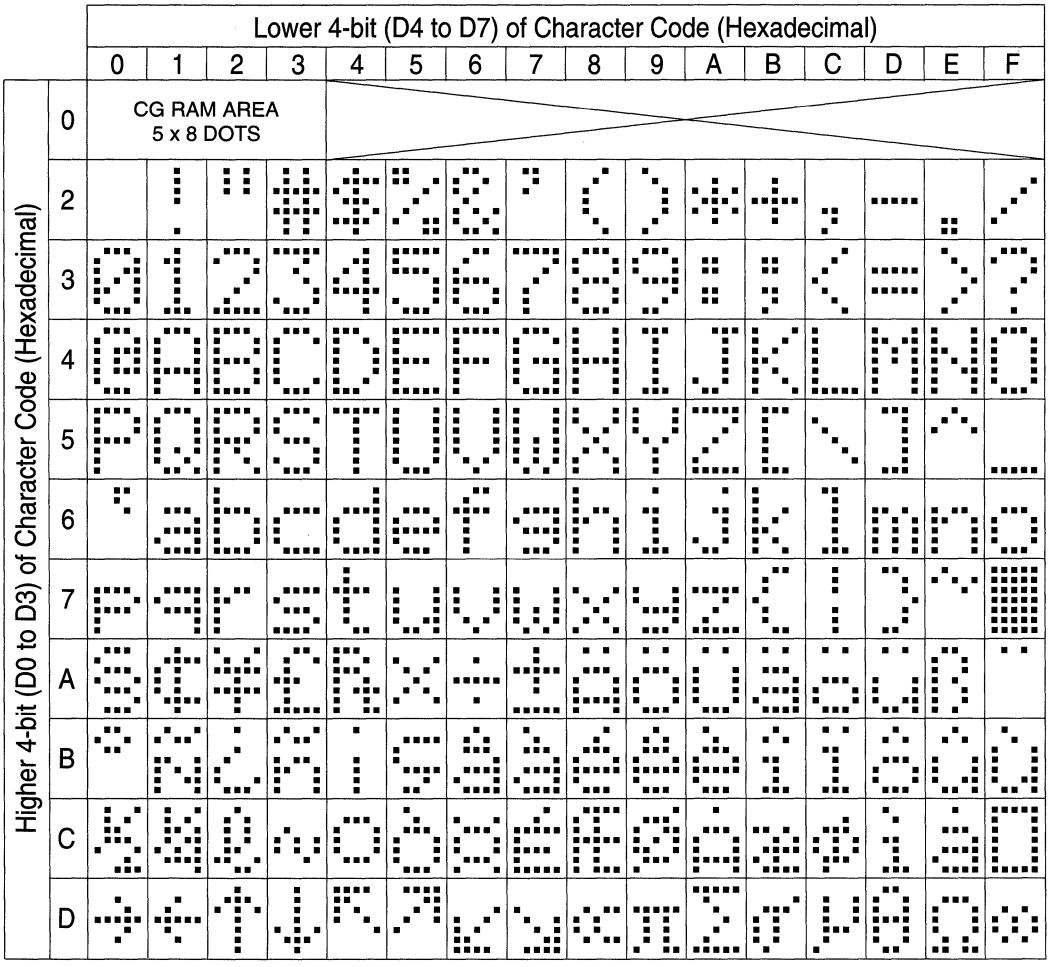
Note: Load capacitance C_L = 15 pF

■ DISPLAY COMMAND

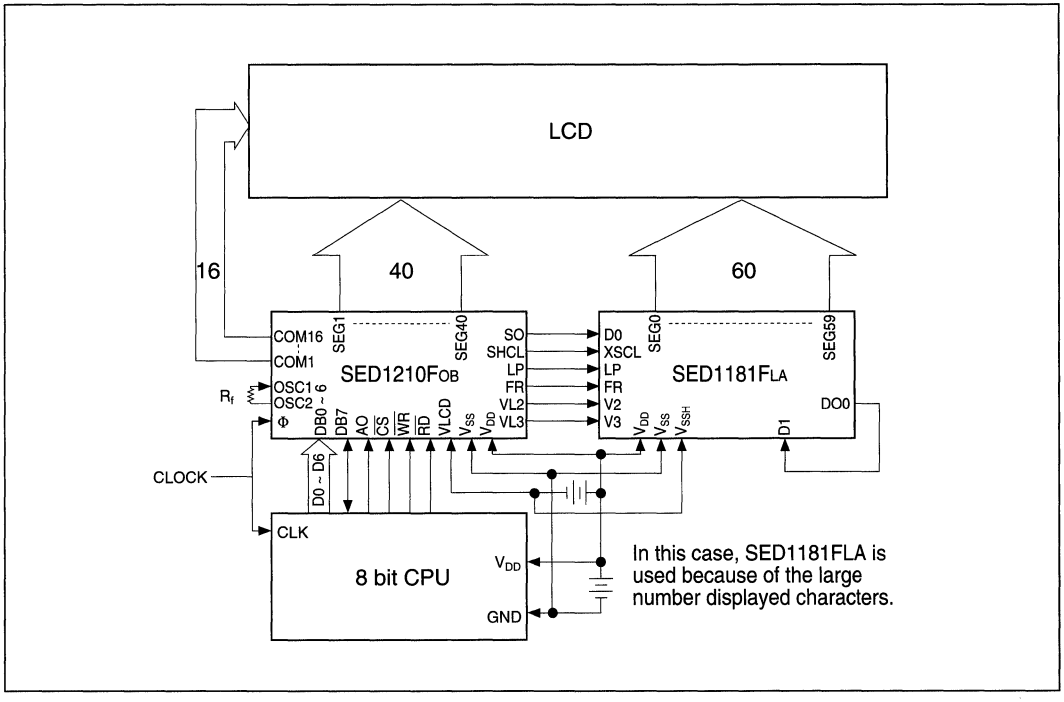
Command Name	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A0	D7	D6	D5	D4	D3	D2	D1	D0	Note
SET CURSOR DIRECTION	0	0	1	0	0	0	0	0	0	1	0	D/I	D0=1: Decrement D0=0: Increment
CURSOR ADDRESS –1/+1	0	0	1	0	0	0	0	0	0	1	1	–1/+1	D0=1: –1 D0=0: +1
CURSOR FONT SELECT	0	0	1	0	0	0	0	0	1	0	0	A/U	D0=1: All dots blinking D0=0: Under line
CURSOR BLINK ON/OFF	0	0	1	0	0	0	0	0	1	0	1	ON/OFF	D0=1: ON D0=0: OFF
DISPLAY ON/OFF	0	0	1	0	0	0	0	0	1	1	0	ON/OFF	
CURSOR ON/OFF	0	0	1	0	0	0	0	0	1	1	1	ON/OFF	
SYSTEM RESET	0	0	1	0	0	0	0	1	0	0	0	0	Except data RAM and CGRAM
DUTY SELECT	0	0	1	0	0	0	0	1	0	0	1	2/1	D0=1: 2 line display (1/16 duty) D0=0: 1 line display (1/8 duty)
SET CGRAM ADDRESS	0	0	1	0	0	0	1	0	A3	A2	A1	A0	UPPER ADDRESS IS FIXED TO 0H
SET CGRAM DATA	0	0	1	0	0	1	0	D4	D3	D2	D1	D0	
SET CURSOR ADDRESS	0	0	1	0	1	2nd/1st	A5	A4	A3	A2	A1	A0	D6=1: N figure for second line D6=0: N figure for first line
SET CHARACTER CODE	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
BUSY FLAG CHECK	0	1	0	0	BF	*	*	*	*	*	*	*	BF=0: Ready *: High impedance BF=1: Busy

Note: Misoperation may be caused when any command other than that listed in the above table is inputted.

■ CHARACTER CODE MAP (SED1210F0B)



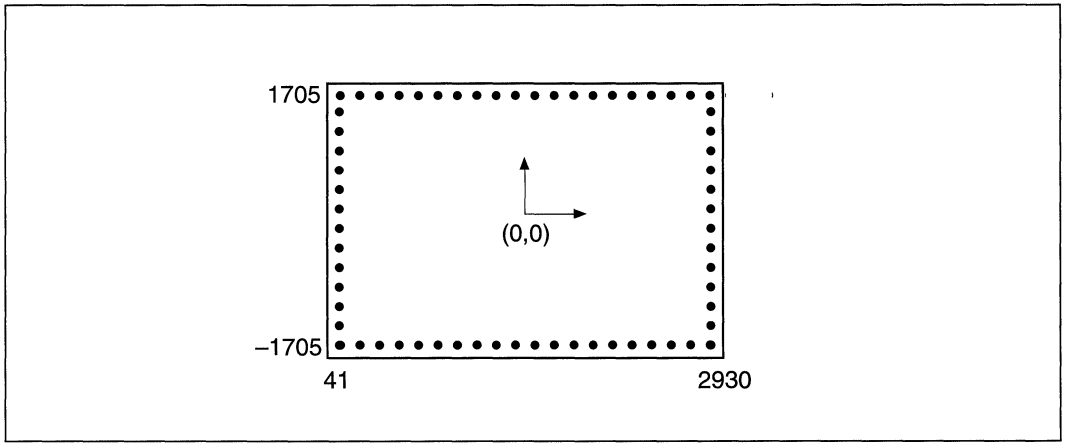
■ EXAMPLE OF APPLICATION (20 characters × 2 lines display)



SED1210FOB can be connected directly to the address bus or the data bus of a microprocessor, or to a peripheral interface unit.

■ DIE SPECIFICATION

● PAD LAYOUT



● DIE & PAD SPECIFICATIONS

Die Size:	5.86 mm x 3.41 mm
Die Thickness:	400 μm
Pad Size:	90 μm x 90 μm
Pad Pitch:	190 μm

● PAD COORDINATES

unit: μm

Pad No.	Pad Name	X	Y
1	SEG17	2123	1552
2	SEG16	1932	1552
3	SEG15	1742	1552
4	SEG14	1551	1552
5	SEG13	1361	1552
6	SEG12	1170	1552
7	SEG11	780	1552
8	SEG10	789	1552
9	SEG9	599	1552
10	SEG8	408	1552
11	SEG7	218	1552
12	SEG6	27	1552
13	SEG5	–163	1552
14	SEG4	–354	1552
15	SEG3	–544	1552
16	SEG2	–735	1552
17	SEG1	–925	1552
18	COM1	–1116	1552
19	COM2	–1306	1552
20	COM3	–1497	1552
21	COM4	–1687	1552
22	COM5	–1878	1552
23	COM6	–2068	1552
24	COM7	–2259	1552
25	COM8	–2778	1429
26	A0	–2778	1238
27	$\overline{CS}$	–2778	1048
28	$\overline{RD}$	–2778	857
29	$\overline{WR}$	–2778	667
30	Φ	–2778	476
31	OSC2	–2778	286
32	OSC1	–2778	95
33	DB7	–2778	–95
34	DB6	–2778	–286
35	DB5	–2778	–476
36	DB4	–2778	–667
37	V_{SS}	–2778	–857
38	V_{LCD}	–2778	–1048
39	V_{DD}	–2778	–1238
40	COM9	–2778	–1429

Pad No.	Pad Name	X	Y
41	COM10	–2220	–1552
42	COM11	–2029	–1552
43	COM12	–1839	–1552
44	COM13	–1648	–1552
45	COM14	–1458	–1552
46	COM15	–1267	–1552
47	COM16	–1077	–1552
48	SO	–886	–1552
49	LP	–696	–1552
50	SHCL	–505	–1552
51	FR	–315	–1552
52	DB3	–124	–1552
53	DB2	66	–1552
54	DB1	257	–1552
55	DB0	447	–1552
56	VL2	638	–1552
57	VL3	828	–1552
58	SEG40	1019	–1552
59	SEG39	1209	–1552
60	SEG38	1400	–1552
61	SEG37	1590	–1552
62	SEG36	1781	–1552
63	SEG35	1971	–1552
64	SEG34	2162	–1552
65	SEG33	2777	–1385
66	SEG32	2777	–1195
67	SEG31	2777	–1004
68	SEG30	2777	–814
69	SEG29	2777	–623
70	SEG28	2777	–433
71	SEG27	2777	–242
72	SEG26	2777	–52
73	SEG25	2777	139
74	SEG24	2777	329
75	SEG23	2777	520
76	SEG22	2777	710
77	SEG21	2777	901
78	SEG20	2777	1091
79	SEG19	2777	1282
80	SEG18	2777	1472

Note: The origin of coordination is the center of the die.

LCD DRIVER-CONTROLLER

■ DESCRIPTION

The SED1230 Series are intelligent CMOS LCD controller-drivers with the ability to display characters (5 × 7) and icons. The SED1230 Series communicates with a high-speed microprocessor such as the Intel 80XX or 68XX family through a serial or 4/8-bit parallel interface.

These devices incorporate an internal DC/DC converter to generate the negative voltage needed for the LCD contrast. The controller features software contrast adjustment by command setting.

The device has internal CGROM with the maximum capacity of 256 characters (5 × 7 dots). The user can store four different characters in the CGRAM area. The device has built-in display data RAM which is capable of displaying up to 48 characters.

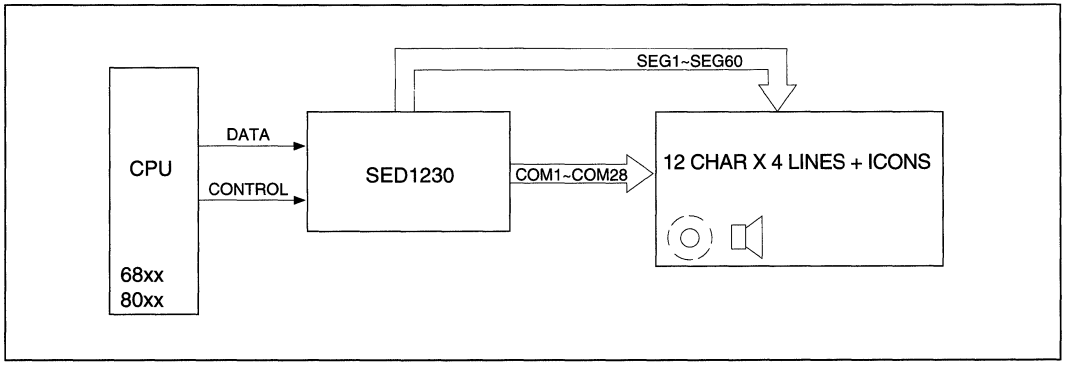
The SED1230 Series has a symbol register which can be set to generate the on-screen symbol display. The symbol capacity is 64 bits.

■ FEATURES

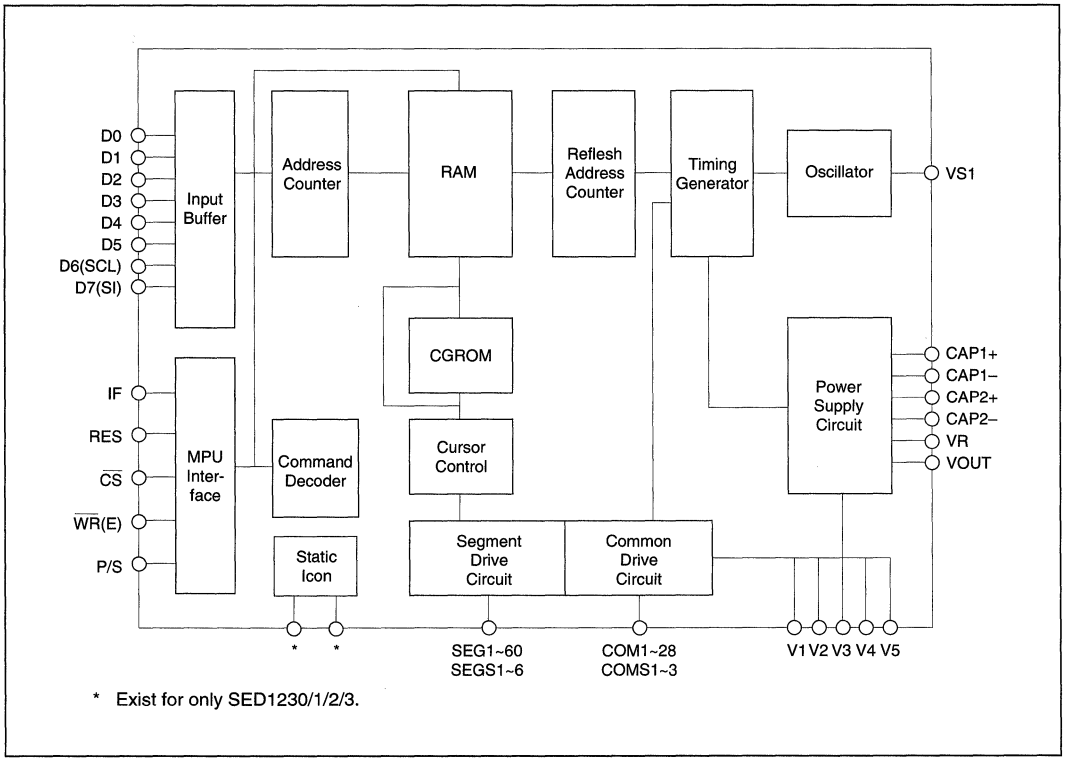
- Built-in display data RAM ..... 48 characters
- CGRAM ..... 4 characters
- CGROM ..... 256 characters (5 × 7) max.
- Symbol registers ..... 64 bits
- Static mode is supported
- Built-in CR oscillator circuit
- On-chip DC/DC converter for the LCD voltage
- Supports two power save modes
- Voltage regulator, low-power voltage follower
- –0.17%/°C temperature gradient
- Low power CMOS process
- 100 µA (operation)
- 16-level contrast adjustment by software
- 2.4 to 3.6V supply voltage
- –4.5 to –11V LCD voltage
- Package ..... Au bump (D_{OB}) TAB

Models	Duty Ratio	Display Character
SED1230	1/30	12 char × 4 lines + 1 Static Icon + 52 symbols
SED1231	1/23	12 char × 3 lines + 1 Static Icon + 52 symbols
SED1232	1/16	12 char × 2 lines + 1 Static Icon + 52 symbols
SED1233	1/16	16 char × 2 lines + 1 Static Icon + 64 symbols
SED1234	1/30	12 char × 4 lines + 48 symbols
SED1235	1/16	12 char × 2 lines + 48 symbols

■ SYSTEM BLOCK DIAGRAM

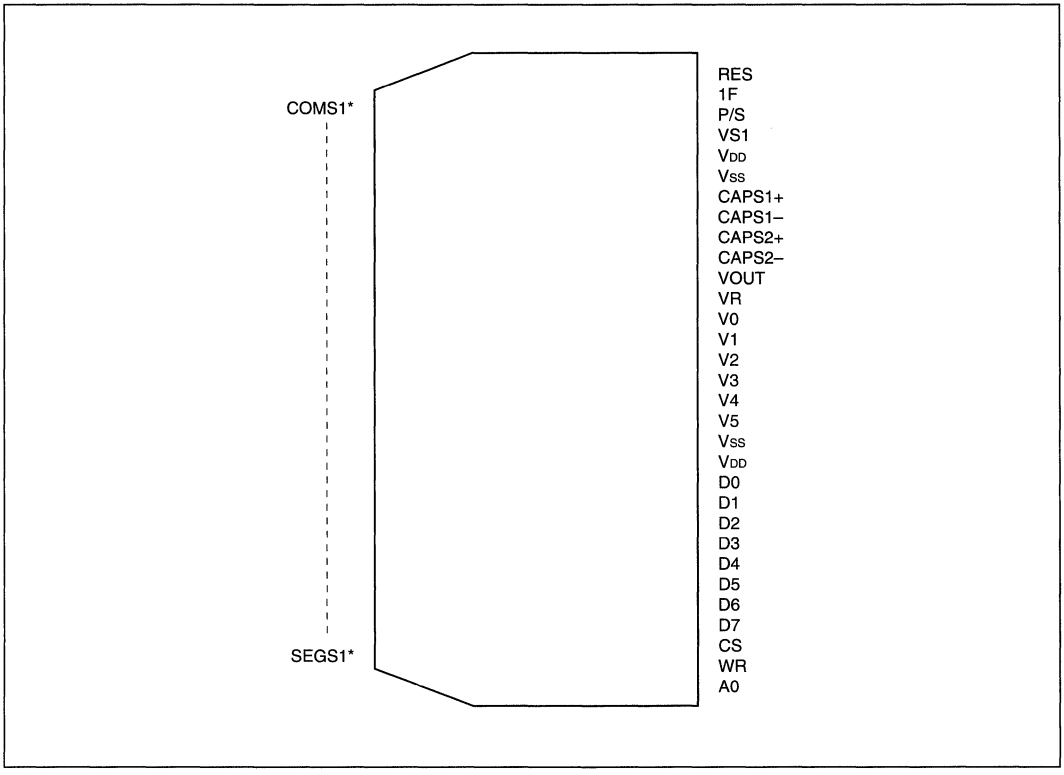


■ BLOCK DIAGRAM



* Exist for only SED1230/1/2/3.

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

● Power Supply

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>VDD</td><td>Power Supply</td><td>Common to MPU power supply pin VCC</td><td>2</td></tr>
<tr><td>VSS</td><td>Power Supply</td><td>Ground</td><td>2</td></tr>
<tr><td>V1, V2, V3, V4, V5</td><td>Power Supply</td><td>LCD driver supply voltages. The voltages determined bthe LCD cell is impedance converted by resistive divider or an operational amplifier. These voltages should be determined on a VDD-basis so as to satisfy the following relationship:
VDD ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5
When the internal power supply is ON, the following voltages are generated on-chip.
<table>
<tr><th></th><th>SED1232D**</th><th></th><th>SED1232D**</th></tr>
<tr><td>V1</td><td>1/5 V5</td><td>V3</td><td>3/5 V5</td></tr>
<tr><td>V2</td><td>2/5 V5</td><td>V4</td><td>4/5 V5</td></tr>
</table>
</td><td>5</td></tr>
<tr><td>VS1</td><td>O</td><td>Power supply and voltage output for crystal power circuit</td><td>1</td></tr>
</table>

● LCD Driver Supply

Pin Name	I/O	Description	No. of Pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connect	1
CAP1–	O	DC/DC voltage converter capacitor 1 negative connect	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connect	1
CAP2–	O	DC/DC voltage converter capacitor 2 negative connect	1
V_{OUT}	O	DC/DC voltage converter output. Capacitor must be connected between V_{OUT} and V_{SS} pad.	1
VR	I	Voltage adjustment pin. Applies voltage between V_{DD} and V5 using a resistive divider.	1

● Microprocessor Interface

Pin Name	I/O	Description	No. of Pins
D7 (SI), D6 (SCL), D5 to D0	I	Data input from the data bus of standard MPU (8-bit or 16-bit). D7 and D6 pins are used for serial data input and a serial clock input respectively when P/S = "L". P/S: "L" → D7 = SI, D6 = SCL, D5 – D0 = —, $\overline{CS}$ = $\overline{CS}$, A0 = A0 P/S: "H" → D7 = D7, D6 = D6, D5 – D0 = D5 – D0, $\overline{CS}$ = $\overline{CS}$, A0 = A0	8
A0	I	Control/display data flag input. This is connected to the LSB of the microprocessor address bus. When LOW, the data on D0 to D7 is command data. When HIGH, the data on D0 to D7 is display data.	1
RES	I	This pin is used to initialize the SED1230 and to select the MPU interface type. For a 68xx MPU interface, initialization occurs after a $\overline{RES}$ ↓ edge transition. For a 80xx MPU interface, initialization occurs after a $\overline{RES}$ ↑ edge transition. MPU interface type is selected by input level after the reset. "H" : 68xx MPU Interface "L" : 80xx MPU Interface	1
$\overline{CS}$	I	Chip select signal	1
$\overline{WR}$ (E)	I	<80xx MPU Connection> Active "L" This is a pin for connecting the $\overline{WR}$ signal of the 80xx MPU. The signal on the data bus is fetched when $\overline{WR}$ signal rises to "H". <68xx MPU Connection> Active "L" This is the enable clock of the 68xx MPU.	1
P/S	I	Parallel/serial data input select. P/S: "L" → Serial Clock = SCL (D6), Data = SI (D7), Chip Select = $\overline{CS}$, Data/Command = A0 P/S: "H" → Serial Clock = —, Data = D7 ~ D0, Chip Select = $\overline{CS}$, Data/Command = A0	
IF	I	Interface data long select pin. "H" : 8-bit parallel input "L" : 4-bit parallel input (When P/S = "L", connect this pin to V_{DD} or V_{SS}.)	

● **LCD Drive Output Signals**

○ **SED1230, SED1231, SED1232**

Pin Name	I/O	Description	No. of Pins
COM1 – COM28	O	Common Signal Output Pin (for character)	28*
COMS1 – COMS3	O	Common Signal Output Pin (static signal and symbol) COMS1 : Common output for static driver** COMS2, COMS3 : Common output for symbol display	3
SEG1 – SEG60	O	Segment Signal Output Pin (for character)	60
SEGS1 – SEGS6	O	Segment Signal Output Pin (static signal and symbol) SEGS1 : Segment output for static driver** SEGS2 – SEGS6 : Segment output for signal output	7

* For SED1230, 28 pins. For SED1232, 14 pins. For SED1231, 21 pins. ** Output in stand-by mode only.

○ **SED1233**

Pin Name	I/O	Description	No. of Pins
COM1 – COM14	O	Common Signal Output Pin (for character)	14
COMS1 – COMS3	O	Common Signal Output Pin (static signal and symbol) COMS1 : Common output for static driver** COMS2, COMS3 : Common output for symbol display	3
SEG1 – SEG80	O	Segment Signal Output Pin (for character)	80
SEGS1	O	Segment Signal Output Pin (for static driver) SEGS1 : Segment output for static driver**	1

** Output in stand-by mode only.

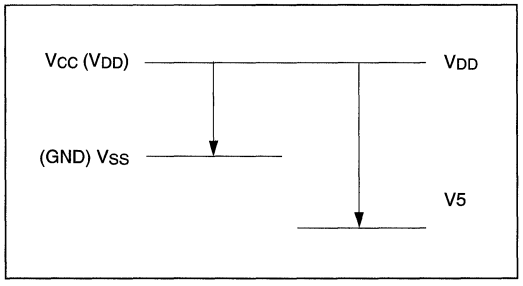
○ **SED1234, SED1235**

Pin Name	I/O	Description	No. of Pins
COM1 – COM28	O	Common signal output pin (for character)	28
COMS2 – COMS3	O	Common signal output pin (for symbol)	2
SEG1 – SEG60	O	Segment signal output pin (for character)	60
SEGS2, SEGS6	O	Segment signal output pin (for symbol)	2

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter		Symbol	Ratings	Unit
Supply voltage		V_{SS}	–5.0 to +0.3 –4.0 to +0.3	V
Driver supply voltage		V5	–16.0 to +0.3	V
Driver supply voltage		V1, V2, V3, V4	V5 to +0.3	V
Input voltage		V_{IN}	V_{SS} – 0.3 to +0.3	V
Output voltage		V0	V_{SS} – 0.3 to +0.3	V
Operating temperature		T_{OPR}	–30 to +85	°C
Storage temperature	TCP	T_{STR}	–55 to +100	°C
	Chip		–65 to +125	°C



Note:

1. The voltages shown are based on V_{DD} = 0V.
2. Always maintain the LCD driving voltage condition such that: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$.
3. If these devices are used over their absolute maximum rating, they may be permanently damaged. To avoid a malfunction or degraded reliability these devices must be operated within the boundries defined by the electrical characteristic conditions for general operation.

● DC Electrical Characteristics

(V_{SS} = –3.6 to –2.4V, T_a = –30 to 85°C, unless otherwise specified)

Parameter		Symbol	Conditions	Applicable Pin	Min	Typ	Max	Unit
Power Voltage 1	Recommended Operation	V_{SS}		V_{SS} *1	–3.6	–3.0	–2.4	V
	Operational				–5.5	–3.0	–2.0	V
Power Voltage 2	Recommended Operation	V5		V5	–11.0	—	–5.0	V
	Operational			*2	–11.0	—	–4.5	V
	Operational	V1, V2		V1, V2	0.6 × V5	—	V_{DD}	V
	Operational	V3, V4		V3, V4	V_{DD}	—	0.4 × V5	V
Hi-level input voltage		V_{IHC}		*3	0.2 × V_{SS}	—	V_{DD}	V
Low-level input voltage		V_{ILC}		*3	V_{SS}	—	0.8 × V_{SS}	V
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	*3	–1.0	—	1.0	µA
LCD drive ON resistance		R_{ON}	T_a = 25°C, ΔV = 0.1V, V5=7V	COM, SEG *4	—	20	40	kΩ
Static power consumption		I_{DD}	During display V5 = –7V	V_{DD} *5	—	—	100	µA
			Stand-by (Power OFF OSC ON)	V_{DD} *6	—	—	20	µA
			Sleep (Power OFF OSC ON)	V_{DD}	—	—	5	µA
			During access f_{CYC} = 200kHz	V_{DD} *7	—	—	500	µA
Input pin capacity		C_{IN}	T_a = 25°C f = 1MHz	*3	—	5.0	8.0	pF
Reset time		t_R		*8	1.0	—	—	µs
Reset "L" pulse width		t_{RW}		*9	10	—	—	µs
Built-in supply circuit	Input voltage	V_{SS}		*10	–3.6	—	–2.4	V
	Raised output voltage	V_{OUT}	Raising 2 times	V_{OUT}	–7.2	—	–4.0	V
			Raising 3 times		–10.8	—	–5.0	V
	Voltage follower circuit	V5①	Applies to SED1230		–11.0	—	–4.5	V
		V5②	Applies to SED1231		–11.0	—	–4.5	V
		V5③	Applies to SED1232		–11.0	—	–4.5	V
	Reference voltage	V_{REG}	T_a = 25°C		–3.5	–3.1	–2.7	V

*1. Correct operation is assured over the recommended operating voltage range. However, during MPU access excessive voltage variation may degrade operation.

*2. Operating voltage range applies when an external power supply is used.

*3. D0 to D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$, $\overline{WR}$(E), P/S, IF

*4. This resistance value applies when 0.1V is applied between output "SEGn", "SEGSn", "COMn", "COMSn", and each power supply pin (V1, V2, V3, V4). R_{ON} = 0.1V/ΔI.

*5. This applies when the character  is displayed and the built-in oscillator and the built-in power supply is used.

*6. This applies when the built-in oscillator circuit is used and power supply are not used in stand-by mode.

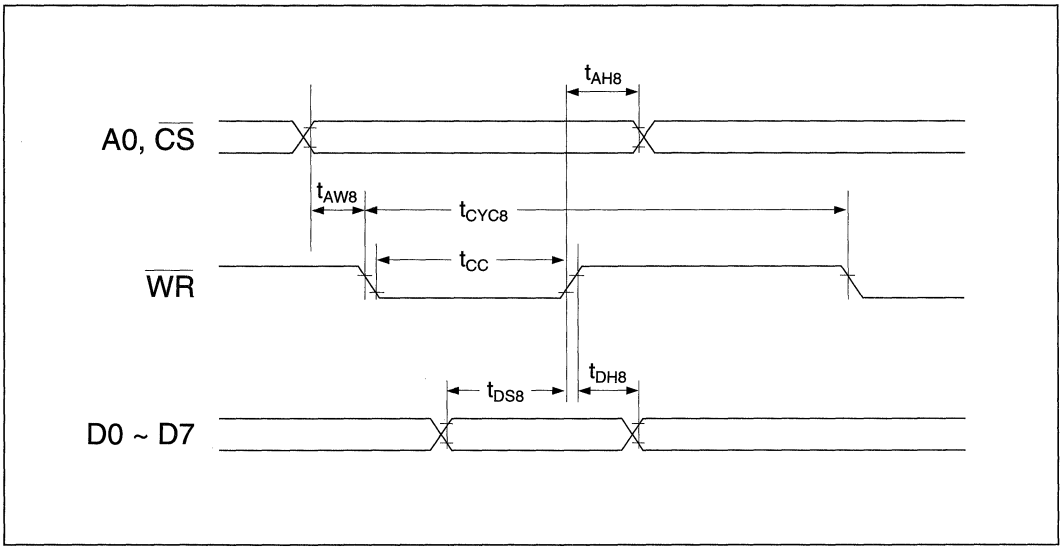
*7. This indicates power consumption during writing of vertical bar patterns at constant fCYC. The power consumption during access is nearly proportional to the access frequency (f_{CYC}). Only I_{DD}(1) applies when there is no access.

*8. t_r (reset time) indicates the interval between the rising edge of an $\overline{RES}$ signal and completion of the internal circuit reset. Therefore, the SED1230 Series does not start normal operation until after the lapse of tr.

*9. t_{rw} is the minimum pulse width of the $\overline{RES}$ signal. For reset to occur, $\overline{RES}$ must pulse to "L" for a time period greater than trw.

*10. Power supply V_{SS} on the primary side is used within the input voltage range if the voltage is doubled or tripled in the built-in power supply circuit.

- **AC Characteristics**
  - **System Bus: Write Characteristics 1 (8080-Series MPU)**



(VSS = –3.6 to –2.4V, Ta = –30 to 85°C)

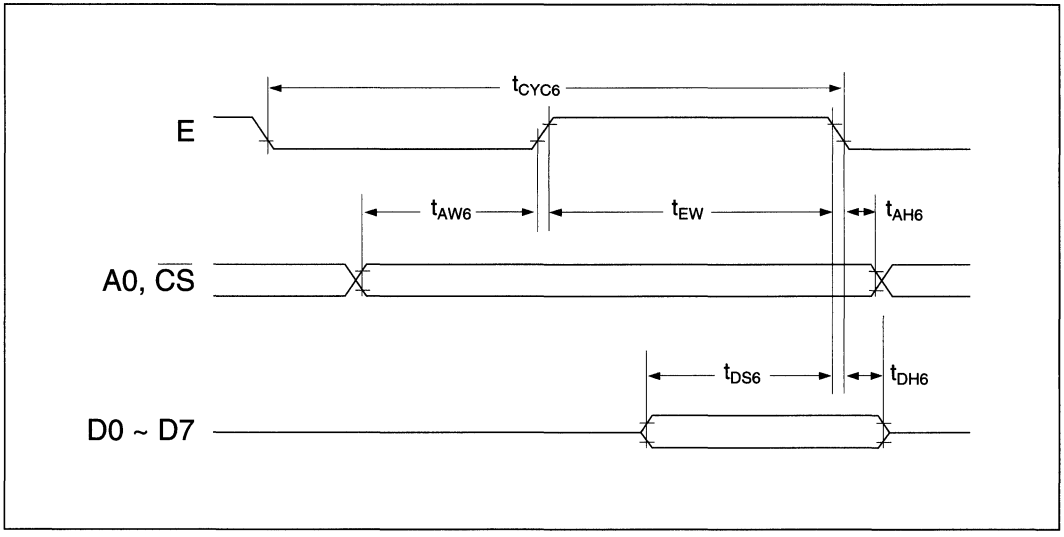
Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
Address hold time	t_{AH8} *3		A0, $\overline{CS}$	30	—	—	ns
Address setup time	t_{AW8} *3			30	—	—	ns
System cycle time	t_{CYC8}	V_{SS} = –2.7V	$\overline{WR}$	500	—	—	ns
		V_{SS} = –2.4V		650	—	—	ns
Control pulse width	t_{CC}	V_{SS} = –2.7V		100	—	—	ns
		V_{SS} = –2.4V		150	—	—	ns
Data setup time	t_{DS8}		D0 to D7	100	—	—	ns
Data hold time	t_{DH8}			50	—	—	ns

*1. The input signal rise time and fall time must both be 15ns or less.

*2. Timing is based on 20% and 80% of Vss.

*3. It is not necessary that A0 timing be the same as $\overline{CS}$.

○ **System Bus: Write Characteristics 2 (6800-Series MPU)**

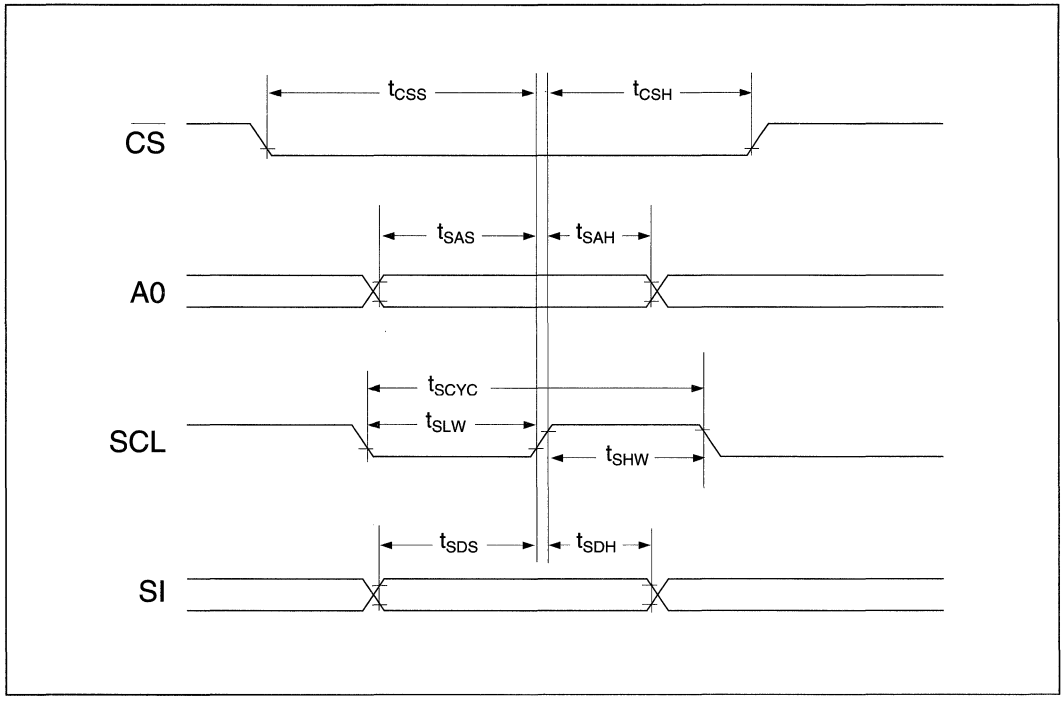


(V_{SS} = –3.6 to –2.4V, T_a = –30 to 85°C)

Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
System cycle time	t_{CYC6}		A0, $\overline{CS}$	500 @ V_{SS} = –2.7V 650 @ V_{SS} = –2.4V	—	—	ns
Address setup time	t_{AW6}			60	—	—	ns
Address hold time	t_{AH6}		D0 to D7	30	—	—	ns
Data setup time	t_{DS8}			100	—	—	ns
Data hold time	t_{DH8}			50	—	—	ns
Enable pulse width	t_{EW}		E	100 @ V_{SS} = –2.7V 150 @ V_{SS} = –2.4V	—	—	ns

*1. t_{CYC6} indicates E signal cycle when $\overline{CS}$ is active. t_{CYC6} must be ensured after $\overline{CS}$ becomes active.
*2. The input signal rise time and fall time must both be 15ns or less.
*3. Timing is based on 20% and 80% of V_{SS}.
*4. It is not necessary that A0 have the same timing as $\overline{CS}$.

○ **Serial Interface**



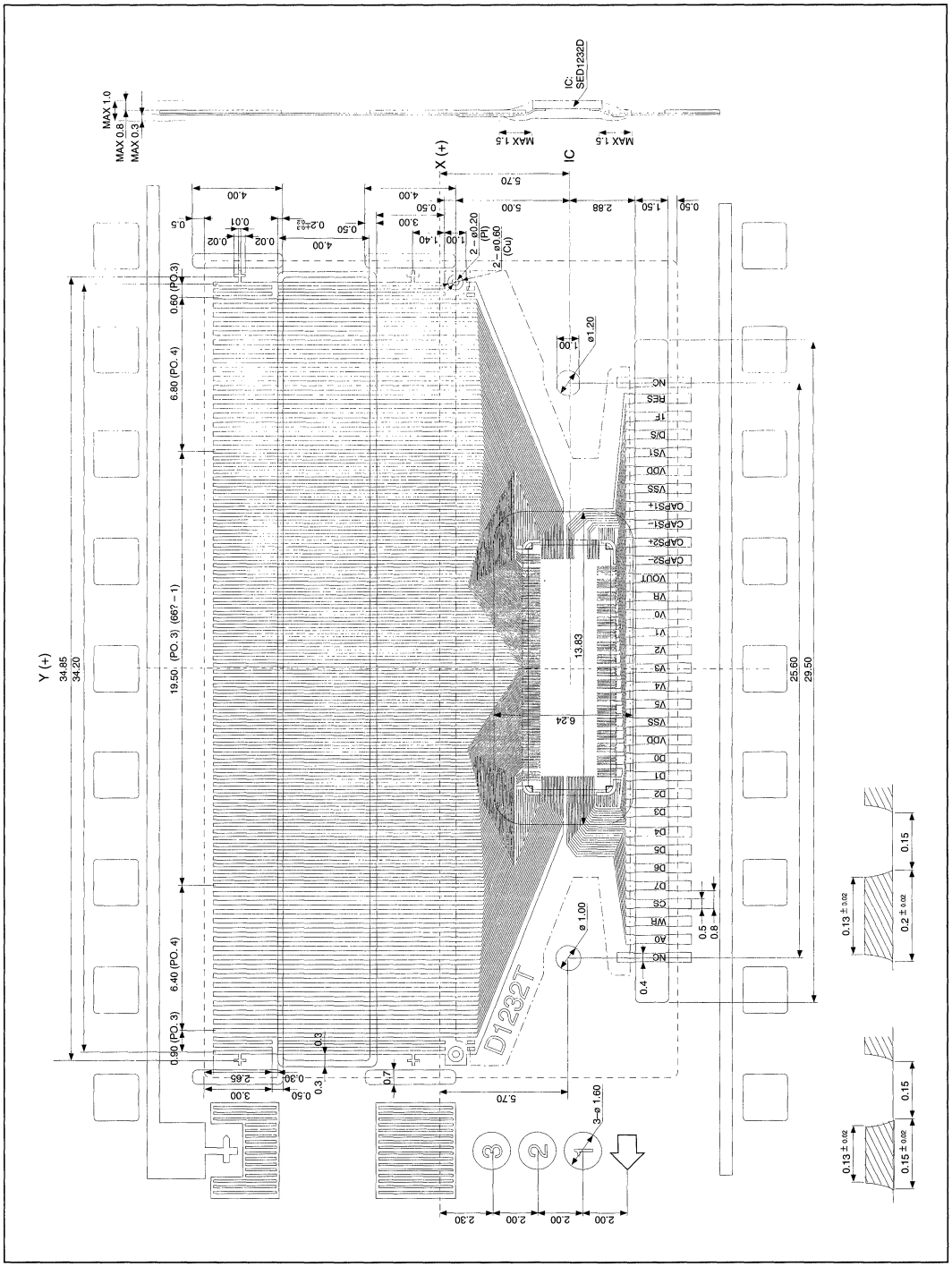
(VSS = –3.6 to –2.4V, Ta = –30 to 85°C)

Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
System clock cycle	tSCYS		SCL	1000	—	—	ns
SCL "H" pulse width	tSHW			300	—	—	ns
SCL "L" pulse width	tSLW			300	—	—	ns
Address setup time	tSAS		A0	50	—	—	ns
Address hold time	tSAH			300	—	—	ns
Data hold time	tSDS			50	—	—	ns
	tSDH			50	—	—	ns
CS-SCL time	tCSS		$\overline{CS}$	150	—	—	ns
	tCSH			700	—	—	ns

*1. The input signal rise time and fall time must both be 15ns or less.

*2. Timing is based on 20% and 80% of VSS.

■ PACKAGE DIMENSIONS



■ SED1230 SERIES COMMAND SUMMARY

Command	Code										Function
	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor home	0	0	0	0	0	1	*	*	*	*	Moves cursor to Home position.
(2) Static display control	0	0	0	0	1	0	*	*	SD1	SD0	Sets display mode of Symbol. (SD1, SD0) = (0, 0) (No display) (0, 1) (1~2Hz blink) (1, 0) (3~4Hz blink) (1, 1) (All display)
(3) Display ON/ OFF control	0	0	0	0	1	1	C	B	DC	D	Sets cursor ON/OFF (C), cursor blink ON/OFF (B), double cursor ON/OFF (DC), and display ON/OFF (D). C = 1 (cursor ON) = 0 (cursor OFF) B = 1 (blink ON) = 0 (blink OFF) DC = 1 (double cursor ON) = 0 (double cursor OFF) D = 1 (display ON) = 0 (display OFF)
(4) Power save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillator circuit ON/OFF (O). PS = 1 (power save ON) = 0 (power save OFF) O = 1 (oscillator circuit ON) = 0 (oscillator circuit OFF)
(5) Power supply control	0	0	0	1	0	1	0	VC	VF	P	Sets internal feedback register ON/OFF (VR), voltage regulator ON/OFF (VC), voltage converter ON/OFF (P), and voltage follower ON/OFF (VF). VR = 1 (voltage regulator ON) = 0 (voltage regulator OFF) VC = 1 (voltage regulator ON) = 0 (voltage regulator OFF) VF = 1 (voltage follower ON) = 0 (voltage follower OFF) P = 1 (voltage converter ON) = 0 (voltage converter OFF)
(6) System set	0	0	0	1	1	0	N2	N1	*	CG	Sets the CGRAM (CG) to USED/NOT USED and the number of display lines (N2, N1). CG = 1 (CGRAM USED) = 0 (CGRAM NOT USED) (N2, N1) = (0, 0) (2 lines) (0, 1) (3 lines) (1, 0) (4 lines)
(7) Electronic volume register	0	0	0	1	1	4	MSB			LSB	Sets the value of electronic contrast control register.
(8) RAM address set	0	0	1	ADDRESS							Sets the address of DDRAM, CGRAM or symbol register.
(9) RAM writing	1	0	DATA								Writes data to DDRAM, CGRAM or symbol register.

■ DIE SPECIFICATION

SED1230D** ..... 1/30 duty ..... 12 Characters × 4 Lines
SED1231D** ..... 1/23 duty ..... 12 Characters × 3 Lines
SED1232D** ..... 1/16 duty ..... 12 Characters × 2 Lines
SED1233D** ..... 1/16 duty ..... 16 Characters × 2 Lines
SED1234D** ..... 1/30 duty ..... 12 Characters × 4 Lines
SED1235D** ..... 1/16 duty ..... 12 Characters × 2 Lines

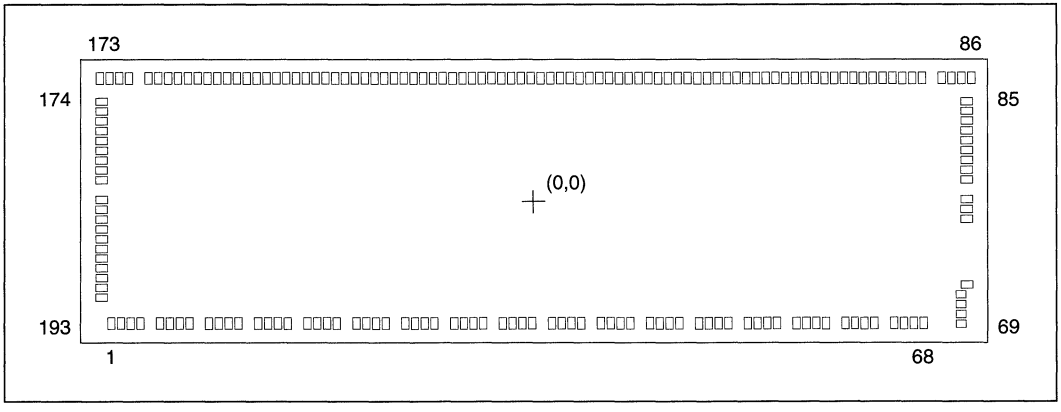
Chip Size : 10.23 × 3.11 mm
Pad Pitch : 110 μm (Min.) SED1230/1/2/3
126μm (Min.) SED1234/5
Chip Thickness : 625 ± 25 μm (SED123*D*A, SED123*D*B)
525 ± 25 μm (SED123*D*C, SED123*D*E)

1) Al Pad Spec. (SED123*D*A and SED123*D*C)

Pad Size : A 86 μm × 135 μm
B 135 μm × 86 μm

2) Au Bump Spec. (SED123*D*B and SED123*D*C) (for reference)

Bump Size : A 80 μm × 129 μm
B 129 μm × 80 μm
Bump Height : 22.5 μm ± 5.5 μm



■ SED1230D** PAD COORDINATES

Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	NC	–4793	–1371
2	NC	–4683	–1371
3	NC	–4572	–1371
4	NC	–4462	–1371
5	V_{DD}	–4242	–1371
6	V_{DD}	–4132	–1371
7	V_{DD}	–4021	–1371
8	V_{DD}	–3911	–1371
9	V_{SS}	–3691	–1371
10	V_{SS}	–3581	–1371
11	V_{SS}	–3470	–1371
12	V_{SS}	–3360	–1371
13	V5	–3140	–1371
14	V5	–3030	–1371
15	V5	–2919	–1371
16	V5	–2809	–1371
17	V4	–2589	–1371
18	V4	–2479	–1371
19	V4	–2368	–1371
20	V4	–2258	–1371
21	V3	–2021	–1371
22	V3	–1910	–1371
23	V3	–1800	–1371
24	V3	–1690	–1371
25	V2	–1453	–1371
26	V2	–1342	–1371
27	V2	–1232	–1371
28	V2	–1122	–1371
29	V1	–884	–1371
30	V1	–774	–1371
31	V1	–664	–1371
32	V1	–554	–1371
33	V0	–316	–1371
34	V0	–206	–1371
35	V0	–96	–1371
36	V0	14	–1371
37	VR	235	–1371
38	VR	345	–1371
39	VR	455	–1371
40	VR	565	–1371
41	V_{OUT}	803	–1371
42	V_{OUT}	913	–1371
43	V_{OUT}	1023	–1371
44	V_{OUT}	1133	–1371
45	CAP2–	1354	–1371
46	CAP2–	1464	–1371
47	CAP2–	1574	–1371
48	CAP2–	1684	–1371
49	CAP2+	1905	–1371
50	CAP2+	2015	–1371
51	CAP2+	2125	–1371
52	CAP2+	2235	–1371
53	CAP1–	2473	–1371
54	CAP1–	2583	–1371
55	CAP1–	2693	–1371
56	CAP1–	2803	–1371
57	CAP1+	3024	–1371
58	CAP1+	3134	–1371
59	CAP1+	3244	–1371
60	CAP1+	3354	–1371
61	V_{SS}	3592	–1371
62	V_{SS}	3702	–1371
63	V_{SS}	3812	–1371
64	V_{SS}	3923	–1371
65	V_{DD}	4143	–1371
66	V_{DD}	4253	–1371
67	V_{DD}	4363	–1371
68	V_{DD}	4474	–1371
69	NC	4883	–1343
70	NC	4883	–1233
71	NC	4883	–1123
72	NC	4883	–1013
73	VS1	4929	–902
74	P/S	4929	–186
75	IF	4929	–76
76	$\overline{RES}$	4929	34
77	COMS1	4929	255
78	COMS2	4929	365
79	COM1	4929	475
80	COM2	4929	585
81	COM3	4929	695
82	COM4	4929	806
83	COM5	4929	916
84	COM6	4929	1026
85	COM7	4929	1136
86	NC	4947	1382
87	NC	4836	1382
88	NC	4726	1382
89	NC	4616	1382
90	COM8	4347	1382
91	COM9	4237	1382
92	COM10	4127	1382
93	COM11	4017	1382
94	COM12	3906	1382
95	COM13	3796	1382
96	COM14	3686	1382
97	SEGS2	3576	1382
98	SEGS3	3466	1382
99	SEGS4	3355	1382
100	SEG1	3245	1382
101	SEG2	3135	1382
102	SEG3	3025	1382
103	SEG4	2915	1382
104	SEG5	2804	1382
105	SEG6	2694	1382
106	SEG7	2584	1382
107	SEG8	2474	1382
108	SEG9	2364	1382
109	SEG10	2253	1382
110	SEG11	2143	1382
111	SEG12	2033	1382
112	SEG13	1923	1382
113	SEG14	1813	1382
114	SEG15	1702	1382
115	SEG16	1592	1382
116	SEG17	1482	1382
117	SEG18	1372	1382
118	SEG19	1262	1382
119	SEG20	1151	1382
120	SEG21	1041	1382
121	SEG22	931	1382
122	SEG23	821	1382
123	SEG24	711	1382
124	SEG25	600	1382
125	SEG26	490	1382
126	SEG27	380	1382
127	SEG28	270	1382
128	SEG29	160	1382
129	SEG30	49	1382
130	SEG31	–61	1382
131	SEG32	–171	1382
132	SEG33	–281	1382
133	SEG34	–391	1382
134	SEG35	–502	1382
135	SEG36	–612	1382
136	SEG37	–722	1382
137	SEG38	–832	1382
138	SEG39	–942	1382
139	SEG40	–1053	1382
140	SEG41	–1163	1382
141	SEG42	–1273	1382
142	SEG43	–1383	1382
143	SEG44	–1493	1382
144	SEG45	–1504	1382
145	SEG46	–1714	1382
146	SEG47	–1824	1382
147	SEG48	–1934	1382
148	SEG49	–2044	1382
149	SEG50	–2155	1382
150	SEG51	–2265	1382
151	SEG52	–2375	1382
152	SEG53	–2485	1382
153	SEG54	–2595	1382
154	SEG55	–2706	1382
155	SEG56	–2816	1382
156	SEG57	–2926	1382
157	SEG58	–3036	1382
158	SEG59	–3146	1382
159	SEG60	–3257	1382
160	SEGS4	–3367	1382
161	SEGS5	–3477	1382
162	SEGS6	–3587	1382
163	COM28	–3697	1382
164	COM27	–3808	1382
165	COM26	–3918	1382
166	COM25	–4028	1382
167	COM24	–4138	1382
168	COM23	–4248	1382
169	COM22	–4359	1382
170	NC	–4627	1382
171	NC	–4738	1382
172	NC	–4848	1382
173	NC	–4958	1382
174	COM21	–4940	1136
175	COM20	–4940	1026
176	COM19	–4940	916
177	COM18	–4940	806
178	COM17	–4940	696
179	COM16	–4940	585
180	COM15	–4940	475
181	COMS3	–4940	365
182	SEGS1	–4940	255
183	A0	–4940	34
184	$\overline{WR}$	–4940	–76
185	$\overline{CS}$	–4940	–186
186	D7	–4940	–296
187	D6	–4940	–406
188	D5	–4940	–517
189	D4	–4940	–627
190	D3	–4940	–737
191	D2	–4940	–847
192	D1	–4940	–957
193	D0	–4940	–1068

■ SED1231D** PAD COORDINATES

Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	NC	−4793	−1371
2	NC	−4683	−1371
3	NC	−4572	−1371
4	NC	−4462	−1371
5	V_{DD}	−4242	−1371
6	V_{DD}	−4132	−1371
7	V_{DD}	−4021	−1371
8	V_{DD}	−3911	−1371
9	V_{SS}	−3691	−1371
10	V_{SS}	−3581	−1371
11	V_{SS}	−3470	−1371
12	V_{SS}	−3360	−1371
13	V5	−3140	−1371
14	V5	−3030	−1371
15	V5	−2919	−1371
16	V5	−2809	−1371
17	V4	−2589	−1371
18	V4	−2479	−1371
19	V4	−2368	−1371
20	V4	−2258	−1371
21	V3	−2021	−1371
22	V3	−1910	−1371
23	V3	−1800	−1371
24	V3	−1690	−1371
25	V2	−1453	−1371
26	V2	−1342	−1371
27	V2	−1232	−1371
28	V2	−1122	−1371
29	V1	−884	−1371
30	V1	−774	−1371
31	V1	−664	−1371
32	V1	−554	−1371
33	V0	−316	−1371
34	V0	−206	−1371
35	V0	−96	−1371
36	V0	14	−1371
37	VR	235	−1371
38	VR	345	−1371
39	VR	455	−1371
40	VR	565	−1371
41	VOUT	803	−1371
42	VOUT	913	−1371
43	VOUT	1023	−1371
44	VOUT	1133	−1371
45	CAP2−	1354	−1371
46	CAP2−	1464	−1371
47	CAP2−	1574	−1371
48	CAP2−	1684	−1371
49	CAP2+	1905	−1371
50	CAP2+	2015	−1371
51	CAP2+	2125	−1371
52	CAP2+	2235	−1371
53	CAP1−	2473	−1371
54	CAP1−	2583	−1371
55	CAP1−	2693	−1371
56	CAP1−	2803	−1371
57	CAP1+	3024	−1371
58	CAP1+	3134	−1371
59	CAP1+	3244	−1371
60	CAP1+	3354	−1371
61	V_{SS}	3592	−1371
62	V_{SS}	3702	−1371
63	V_{SS}	3812	−1371
64	V_{SS}	3923	−1371
65	V_{DD}	4143	−1371
66	V_{DD}	4253	−1371
67	V_{DD}	4363	−1371
68	V_{DD}	4474	−1371
69	NC	4883	−1343
70	NC	4883	−1233
71	NC	4883	−1123
72	NC	4883	−1013
73	VS1	4929	−902
74	P/S	4929	−186
75	IF	4929	−76
76	$\overline{RES}$	4929	34
77	COMS1	4929	255
78	COMS2	4929	365
79	COM1	4929	475
80	COM2	4929	585
81	COM3	4929	696
82	COM4	4929	806
83	COM5	4929	916
84	COM6	4929	1026
85	COM7	4929	1136
86	NC	4947	1382
87	NC	4836	1382
88	NC	4726	1382
89	NC	4616	1382
90	COM8	4347	1382
91	COM9	4237	1382
92	COM10	4127	1382
93	COM11	4017	1382
94	COM12	3906	1382
95	COM13	3796	1382
96	COM14	3686	1382
97	SEGS2	3576	1382
98	SEGS3	3466	1382
99	SEGS4	3355	1382
100	SEG1	3245	1382
101	SEG2	3135	1382
102	SEG3	3025	1382
103	SEG4	2915	1382
104	SEG5	2804	1382
105	SEG6	2694	1382
106	SEG7	2584	1382
107	SEG8	2474	1382
108	SEG9	2364	1382
109	SEG10	2253	1382
110	SEG11	2143	1382
111	SEG12	2033	1382
112	SEG13	1923	1382
113	SEG14	1813	1382
114	SEG15	1702	1382
115	SEG16	1592	1382
116	SEG17	1482	1382
117	SEG18	1372	1382
118	SEG19	1262	1382
119	SEG20	1151	1382
120	SEG21	1041	1382
121	SEG22	931	1382
122	SEG23	821	1382
123	SEG24	711	1382
124	SEG25	600	1382
125	SEG26	490	1382
126	SEG27	380	1382
127	SEG28	270	1382
128	SEG29	160	1382
129	SEG30	49	1382
130	SEG31	−61	1382
131	SEG32	−171	1382
132	SEG33	−281	1382
133	SEG34	−391	1382
134	SEG35	−502	1382
135	SEG36	−612	1382
136	SEG37	−722	1382
137	SEG38	−832	1382
138	SEG39	−942	1382
139	SEG40	−1053	1382
140	SEG41	−1163	1382
141	SEG42	−1273	1382
142	SEG43	−1383	1382
143	SEG44	−1493	1382
144	SEG45	−1504	1382
145	SEG46	−1714	1382
146	SEG47	−1824	1382
147	SEG48	−1934	1382
148	SEG49	−2044	1382
149	SEG50	−2155	1382
150	SEG51	−2265	1382
151	SEG52	−2375	1382
152	SEG53	−2485	1382
153	SEG54	−2595	1382
154	SEG55	−2706	1382
155	SEG56	−2816	1382
156	SEG57	−2926	1382
157	SEG58	−3036	1382
158	SEG59	−3146	1382
159	SEG60	−3257	1382
160	SEGS4	−3367	1382
161	SEGS5	−3477	1382
162	SEGS6	−3587	1382
163	NC	−3697	1382
164	NC	−3808	1382
165	NC	−3918	1382
166	NC	−4028	1382
167	NC	−4138	1382
168	NC	−4248	1382
169	NC	−4359	1382
170	NC	−4627	1382
171	NC	−4738	1382
172	NC	−4848	1382
173	NC	−4958	1382
174	COM21	−4940	1136
175	COM20	−4940	1026
176	COM19	−4940	916
177	COM18	−4940	806
178	COM17	−4940	696
179	COM16	−4940	585
180	COM15	−4940	475
181	COMS3	−4940	365
182	SEGS1	−4940	255
183	A0	−4940	34
184	$\overline{WR}$	−4940	−76
185	$\overline{CS}$	−4940	−186
186	D7	−4940	−296
187	D6	−4940	−406
188	D5	−4940	−517
189	D4	−4940	−627
190	D3	−4940	−737
191	D2	−4940	−847
192	D1	−4940	−957
193	D0	−4940	−1068

■ SED1232D** PAD COORDINATES

Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	NC	–4793	–1371
2	NC	–4683	–1371
3	NC	–4572	–1371
4	NC	–4462	–1371
5	V_{DD}	–4242	–1371
6	V_{DD}	–4132	–1371
7	V_{DD}	–4021	–1371
8	V_{DD}	–3911	–1371
9	V_{SS}	–3691	–1371
10	V_{SS}	–3581	–1371
11	V_{SS}	–3470	–1371
12	V_{SS}	–3360	–1371
13	V5	–3140	–1371
14	V5	–3030	–1371
15	V5	–2919	–1371
16	V5	–2809	–1371
17	V4	–2589	–1371
18	V4	–2479	–1371
19	V4	–2368	–1371
20	V4	–2258	–1371
21	V3	–2021	–1371
22	V3	–1910	–1371
23	V3	–1800	–1371
24	V3	–1690	–1371
25	V2	–1453	–1371
26	V2	–1342	–1371
27	V2	–1232	–1371
28	V2	–1122	–1371
29	V1	–884	–1371
30	V1	–774	–1371
31	V1	–664	–1371
32	V1	–554	–1371
33	V0	–316	–1371
34	V0	–206	–1371
35	V0	–96	–1371
36	V0	14	–1371
37	VR	235	–1371
38	VR	345	–1371
39	VR	455	–1371
40	VR	565	–1371
41	V_{OUT}	803	–1371
42	V_{OUT}	913	–1371
43	V_{OUT}	1023	–1371
44	V_{OUT}	1133	–1371
45	CAP2–	1354	–1371
46	CAP2–	1464	–1371
47	CAP2–	1574	–1371
48	CAP2–	1684	–1371
49	CAP2+	1905	–1371
50	CAP2+	2015	–1371
51	CAP2+	2125	–1371
52	CAP2+	2235	–1371
53	CAP1–	2473	–1371
54	CAP1–	2583	–1371
55	CAP1–	2693	–1371
56	CAP1–	2803	–1371
57	CAP1+	3024	–1371
58	CAP1+	3134	–1371
59	CAP1+	3244	–1371
60	CAP1+	3354	–1371
61	V_{SS}	3592	–1371
62	V_{SS}	3702	–1371
63	V_{SS}	3812	–1371
64	V_{SS}	3923	–1371
65	V_{DD}	4143	–1371
66	V_{DD}	4253	–1371
67	V_{DD}	4363	–1371
68	V_{DD}	4474	–1371
69	NC	4883	–1343
70	NC	4883	–1233
71	NC	4883	–1123
72	NC	4883	–1013
73	VS1	4929	–902
74	P/S	4929	–186
75	IF	4929	–76
76	$\overline{RES}$	4929	34
77	COMS1	4929	255
78	COMS2	4929	365
79	COM1	4929	475
80	COM2	4929	585
81	COM3	4929	696
82	COM4	4929	806
83	COM5	4929	916
84	COM6	4929	1026
85	COM7	4929	1136
86	NC	4947	1382
87	NC	4836	1382
88	NC	4726	1382
89	NC	4616	1382
90	COM8	4347	1382
91	COM9	4237	1382
92	COM10	4127	1382
93	COM11	4017	1382
94	COM12	3906	1382
95	COM13	3796	1382
96	COM14	3686	1382
97	SEGS2	3576	1382
98	SEGS3	3466	1382
99	SEGS4	3355	1382
100	SEG1	3245	1382
101	SEG2	3135	1382
102	SEG3	3025	1382
103	SEG4	2915	1382
104	SEG5	2804	1382
105	SEG6	2694	1382
106	SEG7	2584	1382
107	SEG8	2474	1382
108	SEG9	2364	1382
109	SEG10	2253	1382
110	SEG11	2143	1382
111	SEG12	2033	1382
112	SEG13	1923	1382
113	SEG14	1813	1382
114	SEG15	1702	1382
115	SEG16	1592	1382
116	SEG17	1482	1382
117	SEG18	1372	1382
118	SEG19	1262	1382
119	SEG20	1151	1382
120	SEG21	1041	1382
121	SEG22	931	1382
122	SEG23	821	1382
123	SEG24	711	1382
124	SEG25	600	1382
125	SEG26	490	1382
126	SEG27	380	1382
127	SEG28	270	1382
128	SEG29	160	1382
129	SEG30	49	1382
130	SEG31	–61	1382
131	SEG32	–171	1382
132	SEG33	–281	1382
133	SEG34	–391	1382
134	SEG35	–502	1382
135	SEG36	–612	1382
136	SEG37	–722	1382
137	SEG38	–832	1382
138	SEG39	–942	1382
139	SEG40	–1053	1382
140	SEG41	–1163	1382
141	SEG42	–1273	1382
142	SEG43	–1383	1382
143	SEG44	–1493	1382
144	SEG45	–1504	1382
145	SEG46	–1714	1382
146	SEG47	–1824	1382
147	SEG48	–1934	1382
148	SEG49	–2044	1382
149	SEG50	–2155	1382
150	SEG51	–2265	1382
151	SEG52	–2375	1382
152	SEG53	–2485	1382
153	SEG54	–2595	1382
154	SEG55	–2706	1382
155	SEG56	–2816	1382
156	SEG57	–2926	1382
157	SEG58	–3036	1382
158	SEG59	–3146	1382
159	SEG60	–3257	1382
160	SEGS4	–3367	1382
161	SEGS5	–3477	1382
162	SEGS6	–3587	1382
163	NC	–3967	1382
164	NC	–3808	1382
165	NC	–3918	1382
166	NC	–4028	1382
167	NC	–4138	1382
168	NC	–4248	1382
169	NC	–4359	1382
170	NC	–4627	1382
171	NC	–4738	1382
172	NC	–4848	1382
173	NC	–4958	1382
174	COM14	–4940	1136
175	COM13	–4940	1026
176	COM12	–4940	916
177	COM11	–4940	806
178	COM10	–4940	696
179	COM9	–4940	585
180	COM8	–4940	475
181	COMS3	–4940	365
182	SEGS1	–4940	255
183	A0	–4940	34
184	$\overline{WR}$	–4940	–76
185	$\overline{CS}$	–4940	–186
186	D7	–4940	–296
187	D6	–4940	–406
188	D5	–4940	–517
189	D4	–4940	–627
190	D3	–4940	–737
191	D2	–4940	–847
192	D1	–4940	–957
193	D0	–4940	–1068

■ SED1233D** PAD COORDINATES

Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	NC	–4793	–1371
2	NC	–4683	–1371
3	NC	–4572	–1371
4	NC	–4462	–1371
5	V_{DD}	–4242	–1371
6	V_{DD}	–4132	–1371
7	V_{DD}	–4021	–1371
8	V_{DD}	–3911	–1371
9	V_{SS}	–3691	–1371
10	V_{SS}	–3581	–1371
11	V_{SS}	–3470	–1371
12	V_{SS}	–3360	–1371
13	V5	–3140	–1371
14	V5	–3030	–1371
15	V5	–2919	–1371
16	V5	–2809	–1371
17	V4	–2589	–1371
18	V4	–2479	–1371
19	V4	–2368	–1371
20	V4	–2258	–1371
21	V3	–2021	–1371
22	V3	–1910	–1371
23	V3	–1800	–1371
24	V3	–1690	–1371
25	V2	–1453	–1371
26	V2	–1342	–1371
27	V2	–1232	–1371
28	V2	–1122	–1371
29	V1	–884	–1371
30	V1	–774	–1371
31	V1	–664	–1371
32	V1	–554	–1371
33	V0	–316	–1371
34	V0	–206	–1371
35	V0	–96	–1371
36	V0	14	–1371
37	VR	235	–1371
38	VR	345	–1371
39	VR	455	–1371
40	VR	565	–1371
41	VOUT	803	–1371
42	VOUT	913	–1371
43	VOUT	1023	–1371
44	VOUT	1133	–1371
45	CAP2–	1354	–1371
46	CAP2–	1464	–1371
47	CAP2–	1574	–1371
48	CAP2–	1684	–1371
49	CAP2+	1905	–1371
50	CAP2+	2015	–1371
51	CAP2+	2125	–1371
52	CAP2+	2235	–1371
53	CAP1–	2473	–1371
54	CAP1–	2583	–1371
55	CAP1–	2693	–1371
56	CAP1–	2803	–1371
57	CAP1+	3024	–1371
58	CAP1+	3134	–1371
59	CAP1+	3244	–1371
60	CAP1+	3354	–1371
61	V_{SS}	3592	–1371
62	V_{SS}	3702	–1371
63	V_{SS}	3812	–1371
64	V_{SS}	3923	–1371
65	V_{DD}	4143	–1371
66	V_{DD}	4253	–1371
67	V_{DD}	4363	–1371
68	V_{DD}	4474	–1371
69	NC	4883	–1343
70	NC	4883	–1233
71	NC	4883	–1123
72	NC	4883	–1013
73	VS1	4929	–902
74	P/S	4929	–186
75	IF	4929	–76
76	$\overline{RES}$	4929	34
77	COMS1	4929	255
78	COMS2	4929	365
79	COM1	4929	475
80	COM2	4929	585
81	COM3	4929	696
82	COM4	4929	806
83	COM5	4929	916
84	COM6	4929	1026
85	COM7	4929	1136
86	NC	4947	1382
87	NC	4836	1382
88	NC	4726	1382
89	NC	4616	1382
90	SEG1	4347	1382
91	SEG2	4237	1382
92	SEG3	4127	1382
93	SEG4	4017	1382
94	SEG5	3906	1382
95	SEG6	3796	1382
96	SEG7	3686	1382
97	SEG8	3576	1382
98	SEG9	3466	1382
99	SEG10	3355	1382
100	SEG11	3245	1382
101	SEG12	3135	1382
102	SEG13	3025	1382
103	SEG14	2915	1382
104	SEG15	2804	1382
105	SEG16	2694	1382
106	SEG17	2584	1382
107	SEG18	2474	1382
108	SEG19	2364	1382
109	SEG20	2253	1382
110	SEG21	2143	1382
111	SEG22	2033	1382
112	SEG23	1923	1382
113	SEG24	1813	1382
114	SEG25	1702	1382
115	SEG26	1592	1382
116	SEG27	1482	1382
117	SEG28	1372	1382
118	SEG29	1262	1382
119	SEG30	1151	1382
120	SEG31	1041	1382
121	SEG32	931	1382
122	SEG33	821	1382
123	SEG34	711	1382
124	SEG35	600	1382
125	SEG36	490	1382
126	SEG37	380	1382
127	SEG38	270	1382
128	SEG39	160	1382
129	SEG40	49	1382
130	SEG41	–61	1382
131	SEG42	–171	1382
132	SEG43	–281	1382
133	SEG44	–391	1382
134	SEG45	–502	1382
135	SEG46	–612	1382
136	SEG47	–722	1382
137	SEG48	–832	1382
138	SEG49	–942	1382
139	SEG50	–1053	1382
140	SEG51	–1163	1382
141	SEG52	–1273	1382
142	SEG53	–1383	1382
143	SEG54	–1493	1382
144	SEG55	–1504	1382
145	SEG56	–1714	1382
146	SEG57	–1824	1382
147	SEG58	–1934	1382
148	SEG59	–2044	1382
149	SEG60	–2155	1382
150	SEG61	–2265	1382
151	SEG62	–2375	1382
152	SEG63	–2485	1382
153	SEG64	–2595	1382
154	SEG65	–2706	1382
155	SEG66	–2816	1382
156	SEG67	–2926	1382
157	SEG68	–3036	1382
158	SEG69	–3146	1382
159	SEG70	–3257	1382
160	SEG71	–3367	1382
161	SEG72	–3477	1382
162	SEG73	–3587	1382
163	SEG74	–3967	1382
164	SEG75	–3808	1382
165	SEG76	–3918	1382
166	SEG77	–4028	1382
167	SEG78	–4138	1382
168	SEG79	–4248	1382
169	SEG80	–4359	1382
170	NC	–4627	1382
171	NC	–4738	1382
172	NC	–4848	1382
173	NC	–4958	1382
174	COM14	–4940	1136
175	COM13	–4940	1026
176	COM12	–4940	916
177	COM11	–4940	806
178	COM10	–4940	696
179	COM9	–4940	585
180	COM8	–4940	475
181	COMS3	–4940	365
182	SEGS1	–4940	255
183	A0	–4940	34
184	$\overline{WR}$	–4940	–76
185	$\overline{CS}$	–4940	–186
186	D7	–4940	–296
187	D6	–4940	–406
188	D5	–4940	–517
189	D4	–4940	–627
190	D3	–4940	–737
191	D2	–4940	–847
192	D1	–4940	–957
193	D0	–4940	–1068

■ SED1234D**

Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	VDD	–4077	–1371
2	VSS	–3526	–1371
3	V5	–2975	–1371
4	V4	–2424	–1371
5	V3	–1855	–1371
6	V2	–1287	–1371
7	V1	–719	–1371
8	V0	–151	–1371
9	VR	400	–1371
10	VOUT	968	–1371
11	CAP2–	1519	–1371
12	CAP2+	2070	–1371
13	CAP1–	2638	–1371
14	CAP1+	3189	–1371
15	VSS	3757	–1371
16	VDD	4308	–1371
17	(NC)	4883	–1343
18	(NC)	4883	–1233
19	(NC)	4883	–1123
20	(NC)	4883	–1013
21	VS1	4929	–903
22	P/S	4924	–184
23	IF	4924	–57
24	RES	4924	70
25	COMS2	4950	255
26	COM1	4950	382
27	COM2	4950	510
28	COM3	4950	637
29	COM4	4950	764
30	COM5	4950	891
31	COM6	4950	1019
32	COM7	4950	1146
33	COM8	4896	1406
34	COM9	4769	1406
35	COM10	4642	1406
36	COM11	4515	1406
37	COM12	4388	1406
38	COM13	4262	1406
39	COM14	4135	1406
40	SEGS2	4008	1406
41	SEG1	3881	1406
42	SEG2	3754	1406
43	SEG3	3627	1406
44	SEG4	3501	1406
45	SEG5	3374	1406
46	SEG6	3247	1406
47	SEG7	3120	1406
48	SEG8	2993	1406
49	SEG9	2866	1406
50	SEG10	2740	1406
51	SEG11	2613	1406
52	SEG12	2486	1406
53	SEG13	2359	1406
54	SEG14	2232	1406
55	SEG15	2106	1406
56	SEG16	1979	1406
57	SEG17	1852	1406
58	SEG18	1725	1406
59	SEG19	1598	1406
60	SEG20	1471	1406
61	SEG21	1345	1406
62	SEG22	1218	1406
63	SEG23	1091	1406
64	SEG24	964	1406
65	SEG25	837	1406
66	SEG26	710	1406
67	SEG27	584	1406
68	SEG28	457	1406
69	SEG29	330	1406
70	SEG30	203	1406
71	SEG31	76	1406
72	SEG32	–51	1406
73	SEG33	–177	1406
74	SEG34	–304	1406
75	SEG35	–431	1406
76	SEG36	–558	1406
77	SEG37	–685	1406
78	SEG38	–812	1406
79	SEG39	–938	1406
80	SEG40	–1065	1406
81	SEG41	–1192	1406
82	SEG42	–1319	1406
83	SEG43	–1446	1406
84	SEG44	–1572	1406
85	SEG45	–1699	1406
86	SEG46	–1826	1406
87	SEG47	–1953	1406
88	SEG48	–2080	1406
89	SEG49	–2207	1406
90	SEG50	–2333	1406
91	SEG51	–2460	1406
92	SEG52	–2587	1406
93	SEG53	–2714	1406
94	SEG54	–2841	1406
95	SEG55	–2968	1406
96	SEG56	–3094	1406
97	SEG57	–3221	1406
98	SEG58	–3348	1406
99	SEG59	–3475	1406
100	SEG60	–3602	1406
101	SEGS6	–3729	1406
102	COM28	–3855	1406
103	COM27	–3982	1406
104	COM26	–4109	1406
105	COM25	–4236	1406
106	COM24	–4363	1406
107	COM23	–4679	1405
108	COM22	–4806	1405
109	COM21	–4933	1405
110	COM20	–4964	1094
111	COM19	–4964	966
112	COM18	–4964	839
113	COM17	–4964	712
114	COM16	–4964	584
115	COM15	–4964	457
116	COMS3	–4964	330
117	A0	–4964	202
118	WR	–4964	75
119	CS	–4964	–52
120	D7	–4964	–180
121	D6	–4964	–307
122	D5	–4964	–434
123	D4	–4964	–562
124	D3	–4964	–689
125	D2	–4964	–816
126	D1	–4964	–943
127	D0	–4964	–1071

■ SED1235D**

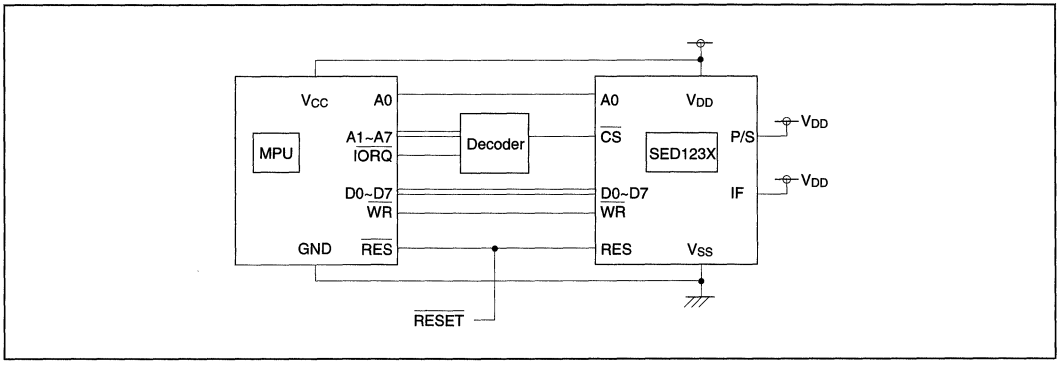
Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	VDD	–4077	–1371
2	VSS	–3526	–1371
3	V5	–2975	–1371
4	V4	–2424	–1371
5	V3	–1855	–1371
6	V2	–1287	–1371
7	V1	–719	–1371
8	V0	–151	–1371
9	VR	400	–1371
10	VOUT	968	–1371
11	CAP2–	1519	–1371
12	CAP2+	2070	–1371
13	CAP1–	2638	–1371
14	CAP1+	3189	–1371
15	VSS	3757	–1371
16	VDD	4308	–1371
17	(NC)	4883	–1343
18	(NC)	4883	–1233
19	(NC)	4883	–1123
20	(NC)	4883	–1013
21	VS1	4929	–903
22	P/S	4924	–184
23	IF	4924	–57
24	RES	4924	70
25	COMS2	4950	255
26	COM1	4950	382
27	COM2	4950	510
28	COM3	4950	637
29	COM4	4950	764
30	COM5	4950	891
31	COM6	4950	1019
32	COM7	4950	1146
33	COM8	4896	1406
34	COM9	4769	1406
35	COM10	4642	1406
36	COM11	4515	1406
37	COM12	4388	1406
38	COM13	4262	1406
39	COM14	4135	1406
40	SEGS2	4008	1406
41	SEG1	3881	1406
42	SEG2	3754	1406
43	SEG3	3627	1406
44	SEG4	3501	1406
45	SEG5	3374	1406
46	SEG6	3247	1406
47	SEG7	3120	1406
48	SEG8	2993	1406
49	SEG9	2866	1406
50	SEG10	2740	1406
51	SEG11	2613	1406
52	SEG12	2486	1406
53	SEG13	2359	1406
54	SEG14	2232	1406
55	SEG15	2106	1406
56	SEG16	1979	1406
57	SEG17	1852	1406
58	SEG18	1725	1406
59	SEG19	1598	1406
60	SEG20	1471	1406
61	SEG21	1345	1406
62	SEG22	1218	1406
63	SEG23	1091	1406
64	SEG24	964	1406
65	SEG25	837	1406
66	SEG26	710	1406
67	SEG27	584	1406
68	SEG28	457	1406
69	SEG29	330	1406
70	SEG30	203	1406
71	SEG31	76	1406
72	SEG32	–51	1406
73	SEG33	–177	1406
74	SEG34	–304	1406
75	SEG35	–431	1406
76	SEG36	–558	1406
77	SEG37	–685	1406
78	SEG38	–812	1406
79	SEG39	–938	1406
80	SEG40	–1065	1406
81	SEG41	–1192	1406
82	SEG42	–1319	1406
83	SEG43	–1446	1406
84	SEG44	–1572	1406
85	SEG45	–1699	1406
86	SEG46	–1826	1406
87	SEG47	–1953	1406
88	SEG48	–2080	1406
89	SEG49	–2207	1406
90	SEG50	–2333	1406
91	SEG51	–2460	1406
92	SEG52	–2587	1406
93	SEG53	–2714	1406
94	SEG54	–2841	1406
95	SEG55	–2968	1406
96	SEG56	–3094	1406
97	SEG57	–3221	1406
98	SEG58	–3348	1406
99	SEG59	–3475	1406
100	SEG60	–3602	1406
101	SEGS6	–3729	1406
102	COM28	–3855	1406
103	COM27	–3982	1406
104	COM26	–4109	1406
105	COM25	–4236	1406
106	COM24	–4363	1406
107	COM23	–4679	1405
108	COM22	–4806	1405
109	COM21	–4933	1405
110	COM20	–4964	1094
111	COM19	–4964	966
112	COM18	–4964	839
113	COM17	–4964	712
114	COM16	–4964	584
115	COM15	–4964	457
116	COMS3	–4964	330
117	A0	–4964	202
118	WR	–4964	75
119	CS	–4964	–52
120	D7	–4964	–180
121	D6	–4964	–307
122	D5	–4964	–434
123	D4	–4964	–562
124	D3	–4964	–689
125	D2	–4964	–816
126	D1	–4964	–943
127	D0	–4964	–1071

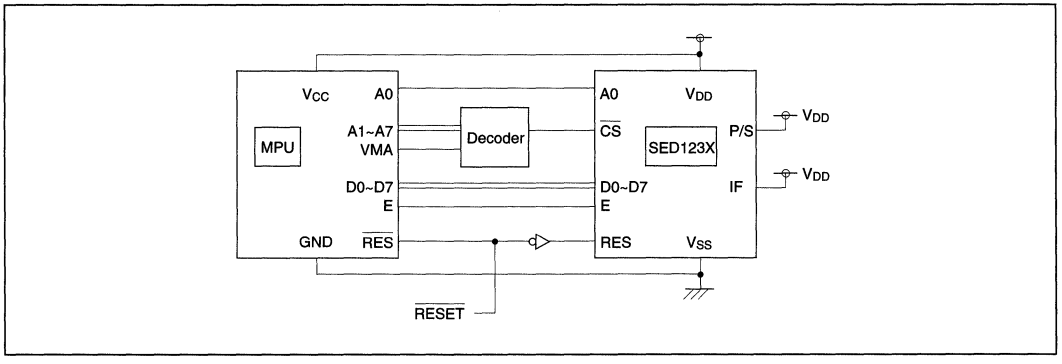
■ MICROPROCESSOR INTERFACE

The SED1230 Series interfaces to either 8080- or 6800- Series microprocessors. The number of connections to the microprocessor can be minimized by using a serial interface.

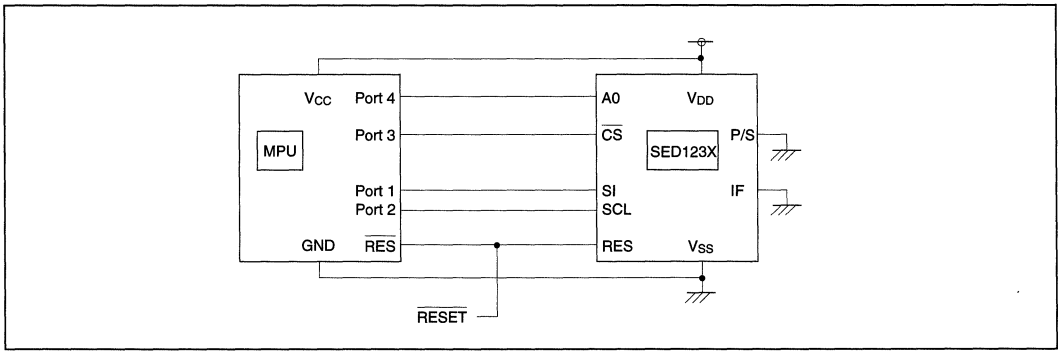
● 8080-Series Microprocessors



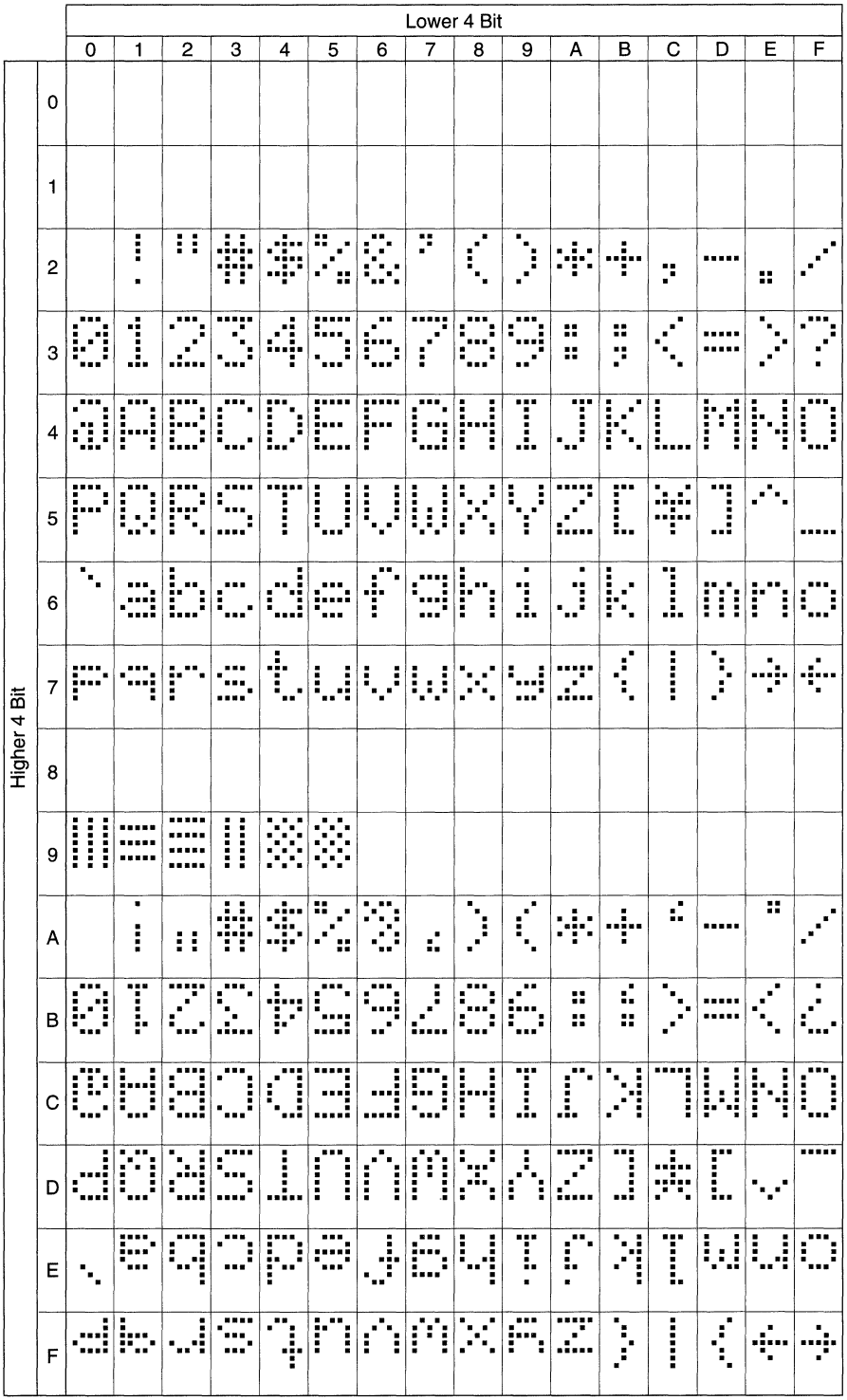
● 6800-Series microprocessors



● Serial Interface



■ CHARACTER CODES AND FONTS



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CMOS DOT MATRIX LCD CONTROLLER DRIVER

■ DESCRIPTION

The SED1278 is a character LCD controller-driver, capable of driving displays as large as 2 lines of 8 characters (5 × 8 pixels), with minimum external components.

The SED1278 has an internal CGROM consisting of 240 characters (5 × 7) plus the underline cursor, JIS, ASCII, and eight user-programmable characters in RAM.

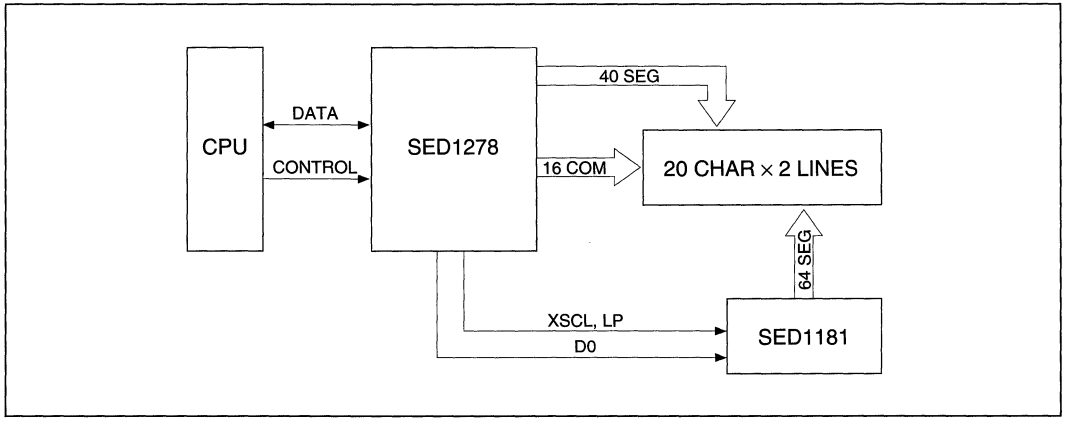
The SED1278 has 40 segment output and 16 common output built-in. Thus, one chip is capable of displaying up to 16 characters. The SED1278 can display one line of 48 characters using an SED1681F (80-bit output) as an expansion segment driver.

The SED1278 is fabricated using a silicon gate CMOS technology process and features very low power dissipation. This makes the device suitable for handheld and portable applications.

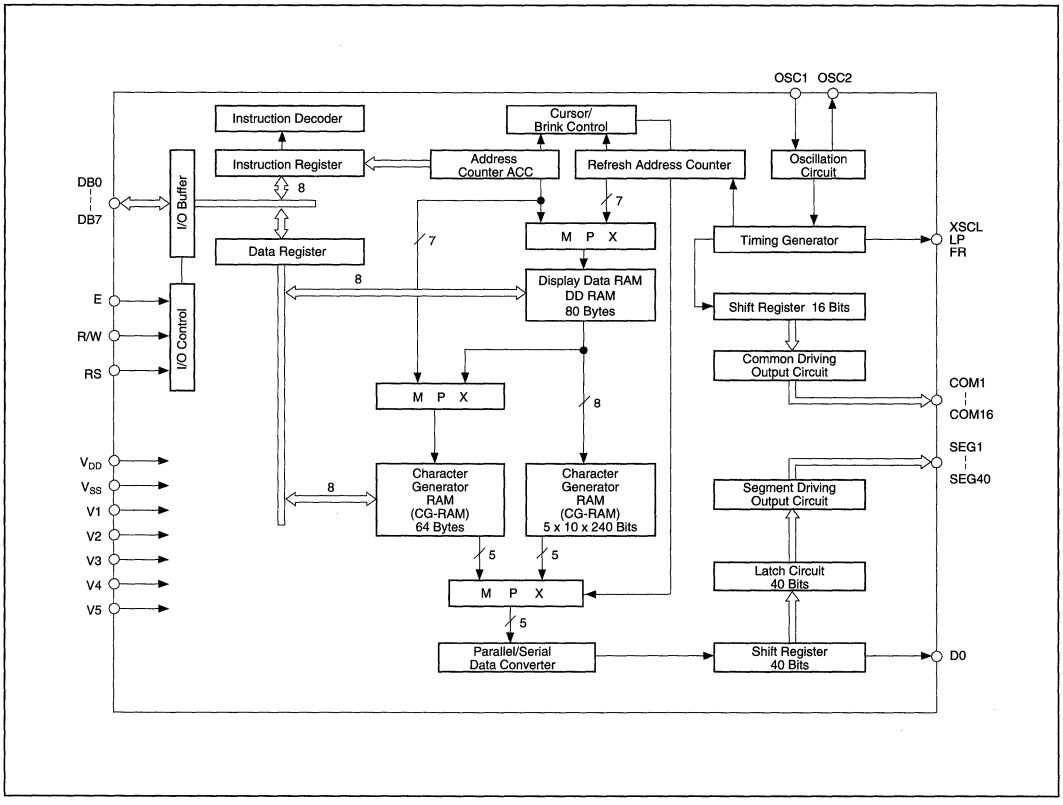
■ FEATURES

- Low-power CMOS technology
- 40 segment output
- 16 common output
- Duty: 1/8 or 1/16 (set by command)
- 4/8-bit CPU data interface, TTL compatible
- Two frame AC drive wave form
- CGROM: ..... 240 characters
- CGRAM: ..... 8 characters
- Display data RAM: ... 80 × 8 bits (80 characters)
- Recommended expansion segment driver:
  SED1181FLA (64 output)
  SED1681F (80 output)
- Built-in power on power-on reset
- Built-in RC oscillator
- Built-in LCD driver voltage-divider network
- TTL compatible CPU interface
- Supply voltage ..... Logic: 4.5V to 5.5V
  LCD: 3.5V to 5.5V
- Package:
  QFP5-80 pins (F_{0A}, F_{0B}, F_{0C}, F_{0D}, F_{0G}, F_{0H})
  Al pad (D_{0A}, D_{0B}, D_{0C}, D_{0D}, D_{0G}, D_{0H})

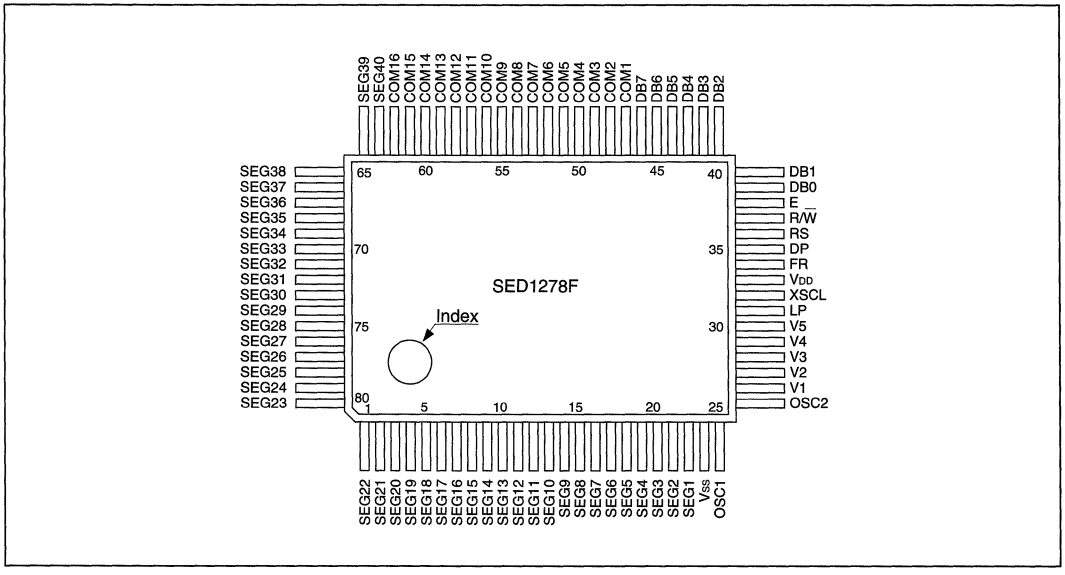
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Symbol	No. of signals	Functions	
RS	1	Register select signal	*1
R/$\overline{W}$	1	Read/write select signal	
E	1	Read/write execute signal	
DB0 to DB7	8	Data bus	
LP	1	Data latching pulse	
XSCL	1	Data transfer clock	
FR	1	LCD AC driving signal	
DO	1	Serial data	
COM1 to COM16	16	Common outputs COM9 to COM16 : non-select for 1/8 duty COM12 to COM16: non-select for 1/11 duty	
SEG1 to SEG40	40	Segment outputs	
V1 to V5	5	LCD driving power (V5≥Vss)	
V_{DD}	1	+5V	
Vss	1	0V (GND)	
OSC1 OSC2	2	Used to connect resistor (typ. 91KΩ) for oscillation; OSC1 is for external clock input.	

*1

RS	R/W	E	Operation
0	0		Instruction write cycle
0	1	1	Busy flag read cycle Address counter read cycle
1	0		DD RAM or CG RAM data write cycle
1	1	1	DD RAM or CG RAM data read cycle

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V, T_a = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to 7.0	V
Supply voltage (2)	V1 to V5	–0.3 to V_{DD}+0.3	V
Input voltage	V_I	–0.3 to V_{DD}+0.3	V
Output voltage	V_O	–0.3 to V_{DD}+0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C•10s (at lead)	—

Note: The following condition must always hold true: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

● DC Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
"H" level input voltage (1)	V_{IH1}		DB0~DB7	2.0	—	V_{DD}	V
"L" level input voltage (1)	V_{IL1}		RS, R/W, E	V_{SS}	—	0.8	V
"H" level input voltage (2)	V_{IH2}		OSC1	V_{DD}–1.0	—	V_{DD}	V
"L" level input voltage (2)	V_{IL2}			V_{SS}	—	1.0	V
"H" level output voltage (1)	V_{OH1}	I_{OH}=–0.205mA	DB0~DB7	2.4	—	—	V
"L" level output voltage (1)	V_{OL1}	I_{OL}=1.6mA		—	—	0.4	V
"H" level output voltage (2)	V_{OH2}	I_{OH}=–0.04mA	XSCL LP D0	0.9V_{DD}	—	—	V
"L" level output voltage (2)	V_{OL2}	I_{OL}=0.04mA		—	—	0.1V_{DD}	V
Driver-on resistor (COM)	R_{COM}	|V_{COM}–V_n|=0.5V	COM1~16	—	2	10	kΩ
Driver-on resistor (SEG)	R_{SEG}	|V_{SEG}–V_n|=0.5V	SEG1~40	—	2.5	10	kΩ
I/O leakage current	I_{IL}	V_I=0 to V_{DD}		—	—	1	µA
Pull-up MOS current	–I_P	V_{DD}=5V		50	125	250	µA
Supply current	I_{op}	Rf oscillation, from external clock V_{DD}=5V, f_{OSC}=f_{CP}=270kHz	V_{DD}	—	0.5	0.8	mA
External clock operation							
External clock operating frequency	f_{EXTCL}			125	250	350	kHz
External clock duty	Duty			45	50	55	%
External clock rise time	t_{rEXTCL}			—	—	0.2	µs
External clock fall time	t_{fEXTCL}			—	—	0.2	µs
Internal clock operation (Rf oscillation)							
Oscillation frequency	f_{OSC}	R_f=91kΩ±2%		190	270	350	kHz
Internal clock operation (Ceramic filter oscillation)							
Oscillation frequency	f_{OSC}	Ceramic filter		245	250	255	kHz
LCD driving voltage	V_{LCD}	V_{DD}–V5		3.0	—	V_{DD}	V

● AC Characteristics

○ Read cycle

(V_{DD} = 5.0V ± 10%, V_{SS} = 0V, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}		500	—	—	ns
Enable "H" level pulse width	t_{WEH}		220	—	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	—	25	ns
RS, R/$\overline{W}$ setup time	t_{AS}		40	—	—	ns
RS, R/$\overline{W}$ address hold time	t_{AH}		10	—	—	ns
Read data output delay	t_{RD}	C_L=100pF	—	—	120	ns
Read data hold time	t_{DHR}		20	—	—	ns

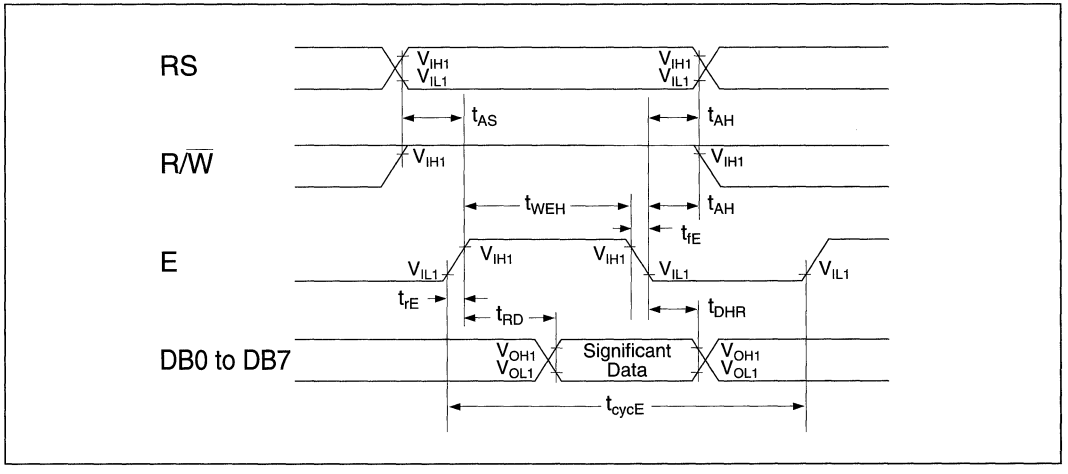
○ **Write cycle**

(V_{DD} = 5.0V±10%, V_{SS} = 0V, T_a = –20 to 75°C)

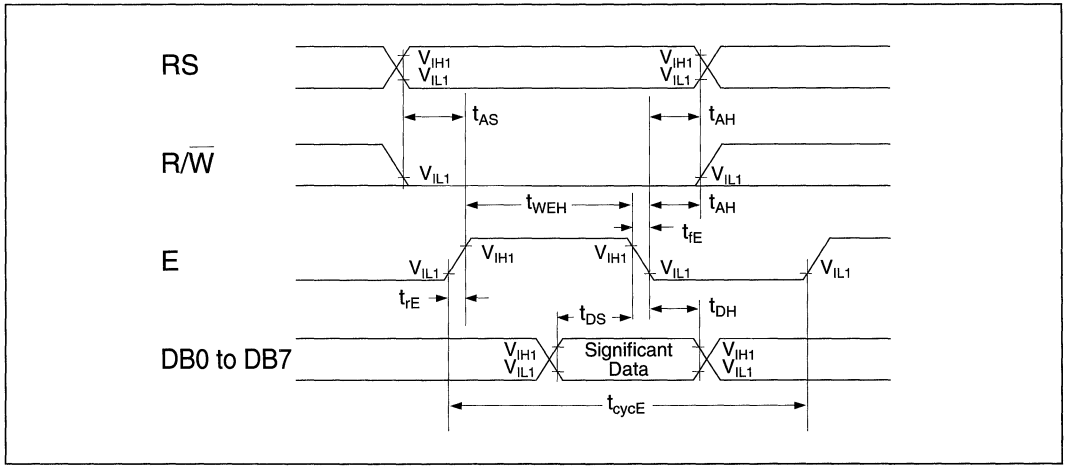
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}		500	—	—	ns
Enable "H" level pulse width	t_{WEH}		220	—	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	—	25	ns
RS, R/$\overline{W}$ setup time	t_{AS}		40	—	—	ns
RS, R/$\overline{W}$ address hold time	t_{AH}		10	—	—	ns
Data setup time	t_{DS}		60	—	—	ns
Write data hold time	t_{DH}		10	—	—	ns

● **Timing Chart**

○ **Read cycle**



○ **Write cycle**

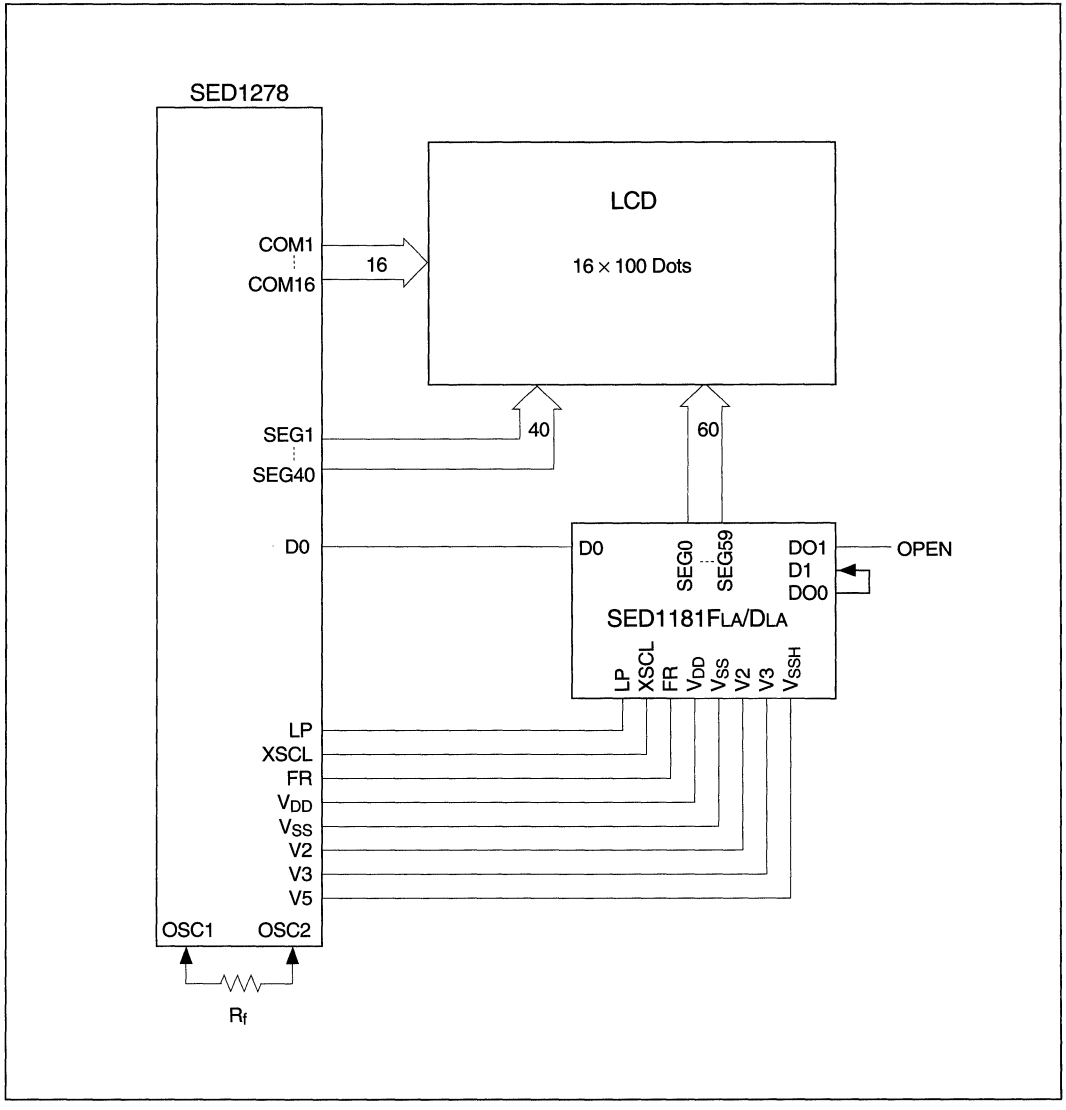


■ DISPLAY COMMAND

Parameter	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Note
CLEAR DISPLAY	0	0	0	0	0	0	0	0	0	1	
CURSOR HOME	0	0	0	0	0	0	0	0	1	*	
ENTRY MODE SET	0	0	0	0	0	0	0	1	I/D	S	DB1=1 : Increment, DB1=0 : Decrement DB0=1 : The display is shifted. DB0=0 : The display is not shifted.
DISPLAY ON/OFF	0	0	0	0	0	0	1	D	C	B	DB2=1 : Display on DB2=0 : Display off DB1=1 : Cursor on DB1=0 : Cursor off DB0=1 : Brinking on DB0=0 : Brinking off
CURSOR/DISPLAY SHIFT	0	0	0	0	0	1	S/C	R/L	*	*	DB3=1 : Shifts display one character DB2=1 : Right shift, DB2=0 : Left shift
SYSTEM SET	0	0	0	0	1	DL	N	F	*	*	DB4=1 : 8 bits, DB4=0 : 4 bits DB3=1 : 2 lines display (1/16 duty), DB3=0 : 1 line display (DB2=1 : 5x10 dots, 1/11 duty DB2=0 : 5x7dots, 1/8 duty)
SET CGRAM ADDRESS	0	0	0	1	ACG						The address length that can be set is 64 addresses.
SET DDRAM ADDRESS	0	0	1	ADD							The address length that can be set is 80 addresses.
READ BUSY FLAG/ ADDRESS COUNTER	0	1	BF	AC							DB7=1 : Busy (instruction not accepted) DB7=0 : Ready (instruction accepted)
WRITE DATA	1	0	Write Data								
READ DATA	1	1	Read Data								

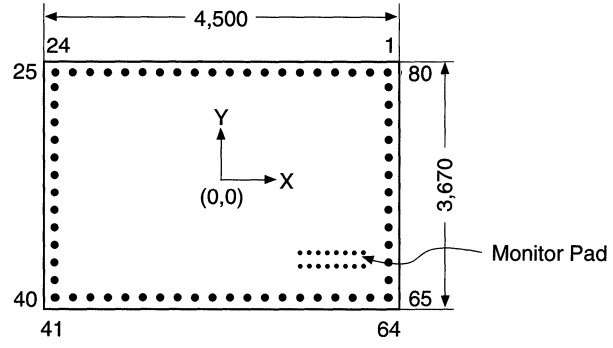
* Don't care

■ EXAMPLE OF APPLICATION (2 lines × 20 characters)



SED1278 is usually connected to 8-bit MPU via I/O ports.

■ PAD LAYOUT



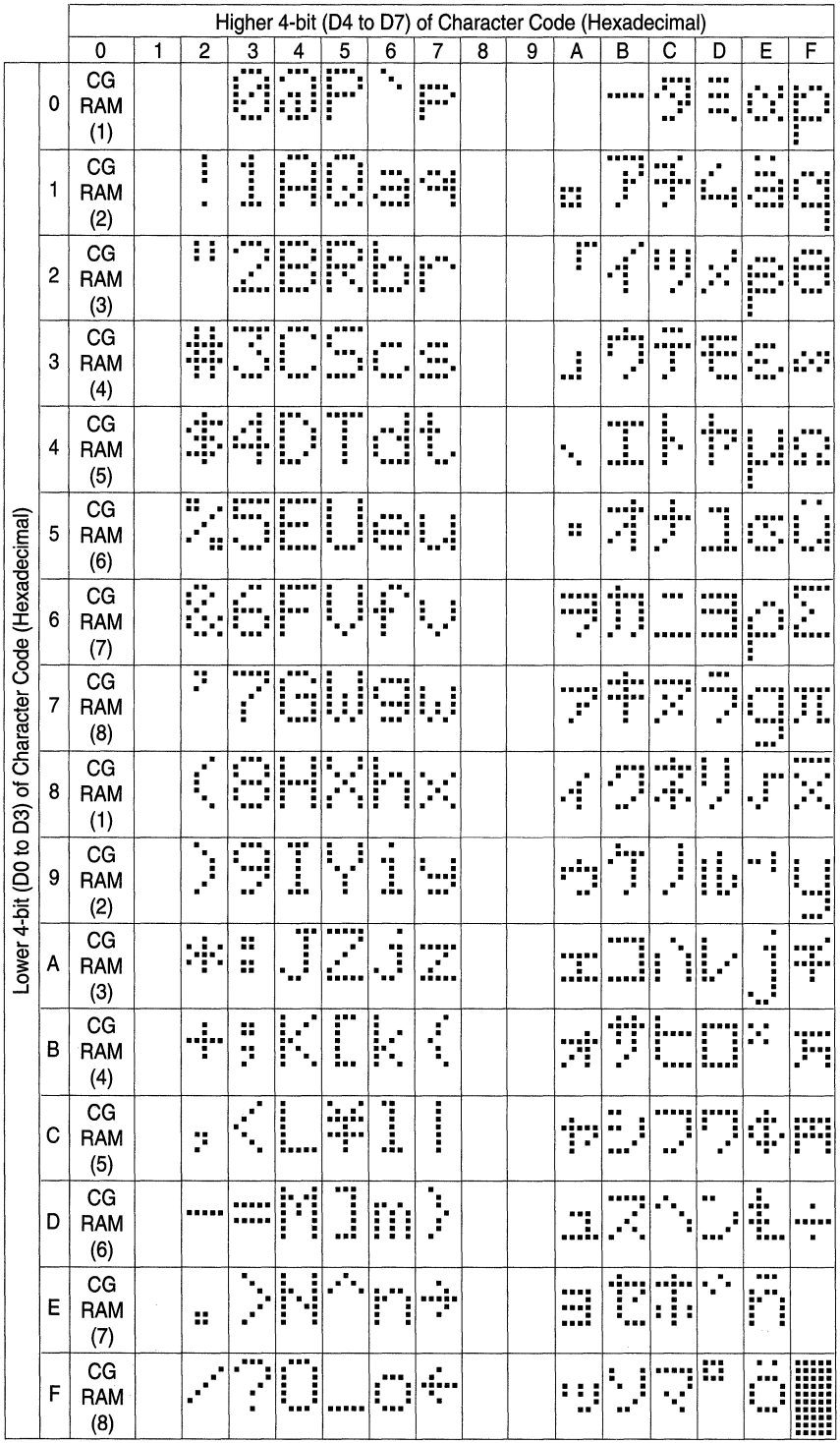
Pad size: 109 × 109

● PAD COORDINATES

Pad No.	Pad Name	X	Y
1	SEG22	2087	1671
2	SEG21	1905	1671
3	SEG20	1723	1671
4	SEG19	1541	1671
5	SEG18	1359	1671
6	SEG17	1177	1671
7	SEG16	995	1671
8	SEG15	814	1671
9	SEG14	633	1671
10	SEG13	452	1671
11	SEG12	272	1671
12	SEG11	91	1671
13	SEG10	–91	1671
14	SEG9	–272	1671
15	SEG8	–452	1671
16	SEG7	–633	1671
17	SEG6	–814	1671
18	SEG5	–995	1671
19	SEG4	–1177	1671
20	SEG3	–1359	1671
21	SEG2	–1541	1671
22	SEG1	–1723	1671
23	GND	–1905	1671
24	OSC1	–2087	1671
25	OSC2	–2087	1365
26	V1	–2087	1183
27	V2	–2087	1001
28	V3	–2087	819
29	V4	–2087	637
30	V5	–2087	455
31	LP	–2087	273
32	XSCL	–2087	91
33	VCC	–2087	–91
34	FR	–2087	–273
35	DO	–2087	–455
36	RS	–2087	–637
37	R/W	–2087	–819
38	E	–2087	–1001
39	DB0	–2087	–1183
40	DB1	–2087	–1365

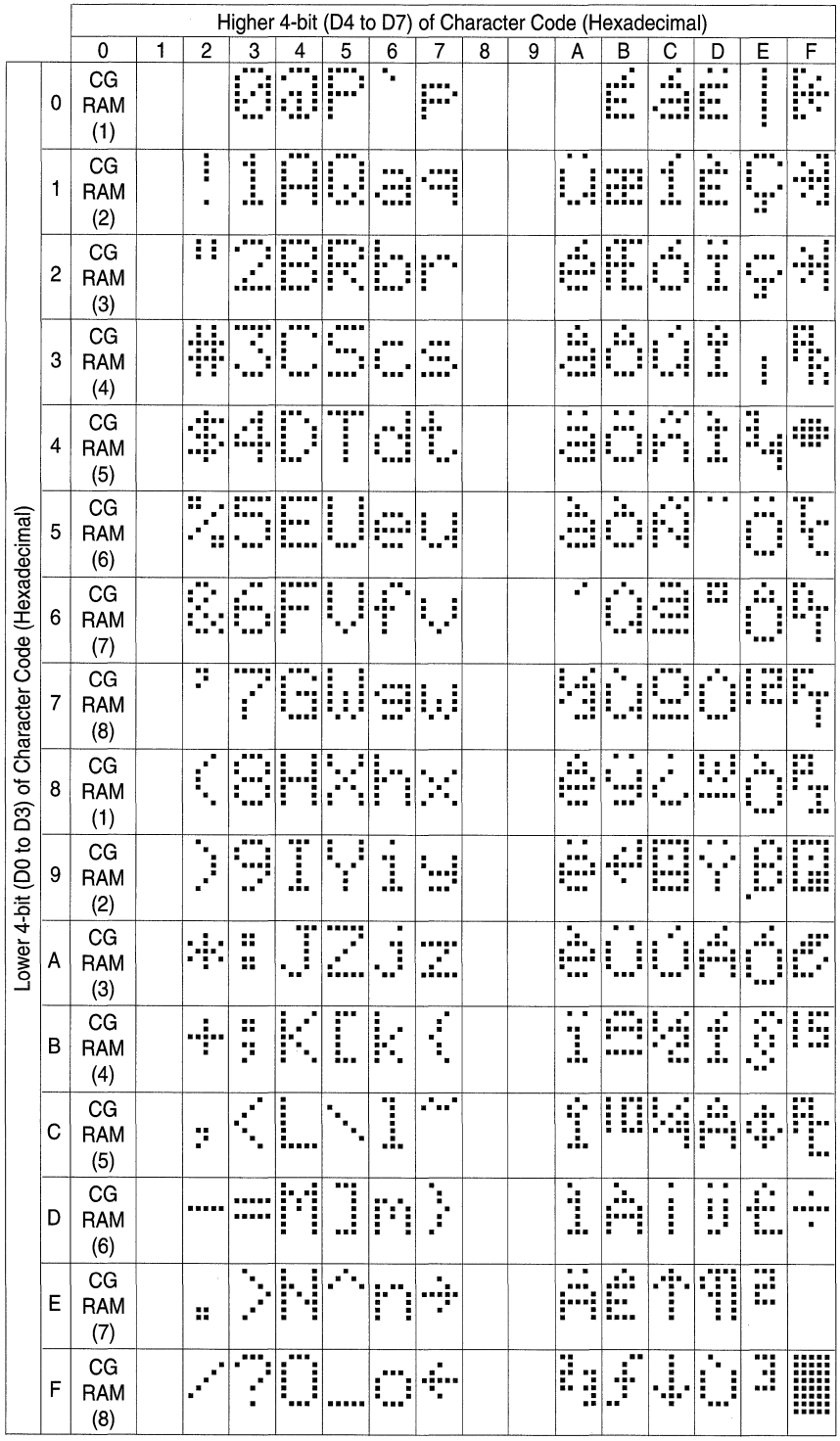
Pad No.	Pad Name	X	Y
41	DB2	–2087	–1671
42	DB3	–1905	–1671
43	DB4	–1723	–1671
44	DB5	–1541	–1671
45	DB6	–1359	–1671
46	DB7	–1177	–1671
47	COM1	–995	–1671
48	COM2	–814	–1671
49	COM3	–633	–1671
50	COM4	–452	–1671
51	COM5	–272	–1671
52	COM6	–91	–1671
53	COM7	91	–1671
54	COM8	272	–1671
55	COM9	452	–1671
56	COM10	633	–1671
57	COM11	814	–1671
58	COM12	995	–1671
59	COM13	1177	–1671
60	COM14	1359	–1671
61	COM15	1541	–1671
62	COM16	1723	–1671
63	SEG40	1905	–1671
64	SEG39	2087	–1671
65	SEG38	2087	–1365
66	SEG37	2087	–1183
67	SEG36	2087	–1001
68	SEG35	2087	–819
69	SEG34	2087	–637
70	SEG33	2087	–455
71	SEG32	2087	–273
72	SEG31	2087	–91
73	SEG30	2087	91
74	SEG29	2087	273
75	SEG28	2087	455
76	SEG27	2087	637
77	SEG26	2087	819
78	SEG25	2087	1001
79	SEG24	2087	1183
80	SEG23	2087	1365

■ SED1278F0A/D0A CHARACTER FONT

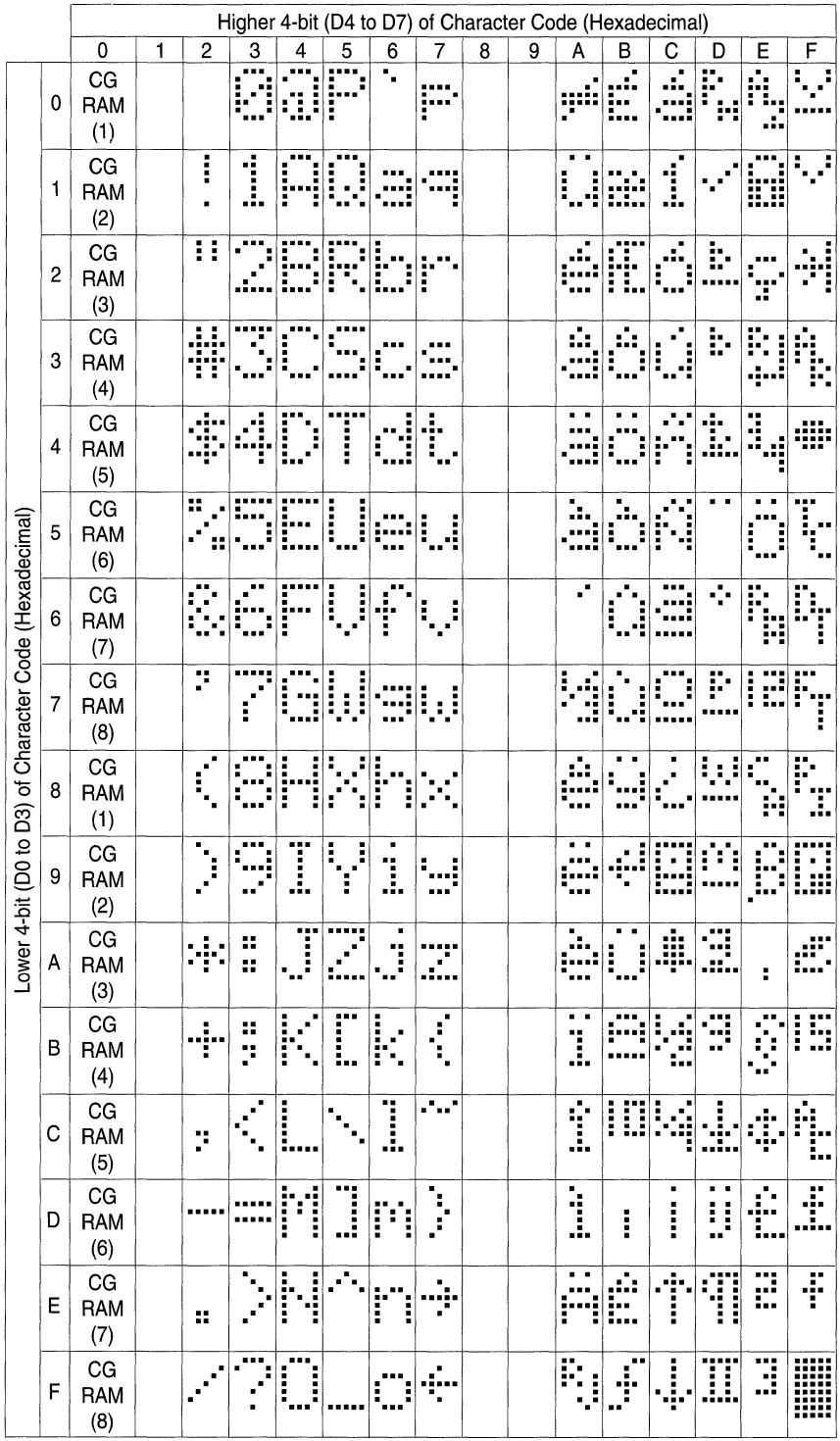


■ SED1278F0B/D0B CHARACTER FONT

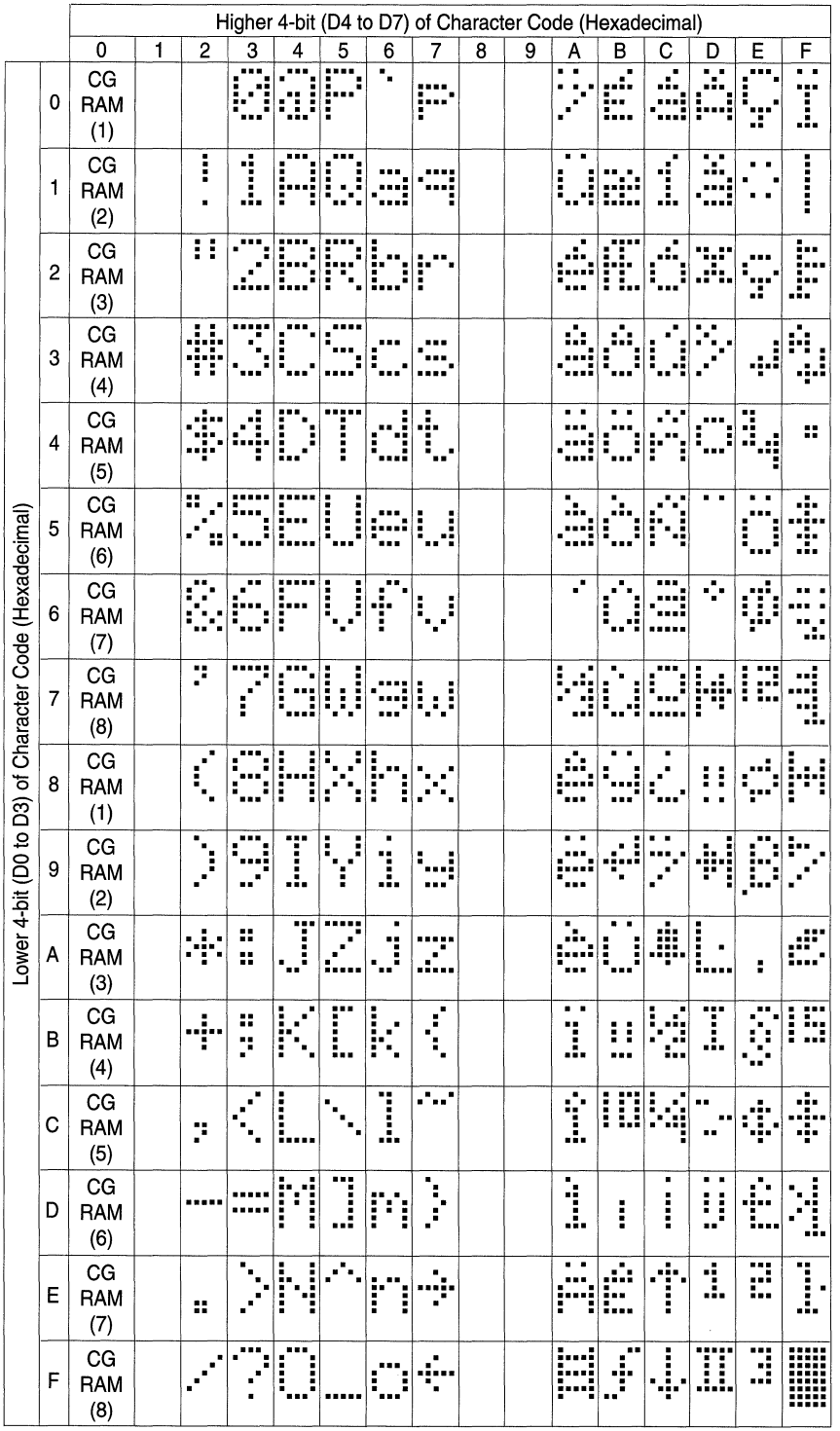
■ SED1278Foc/Doc CHARACTER FONT



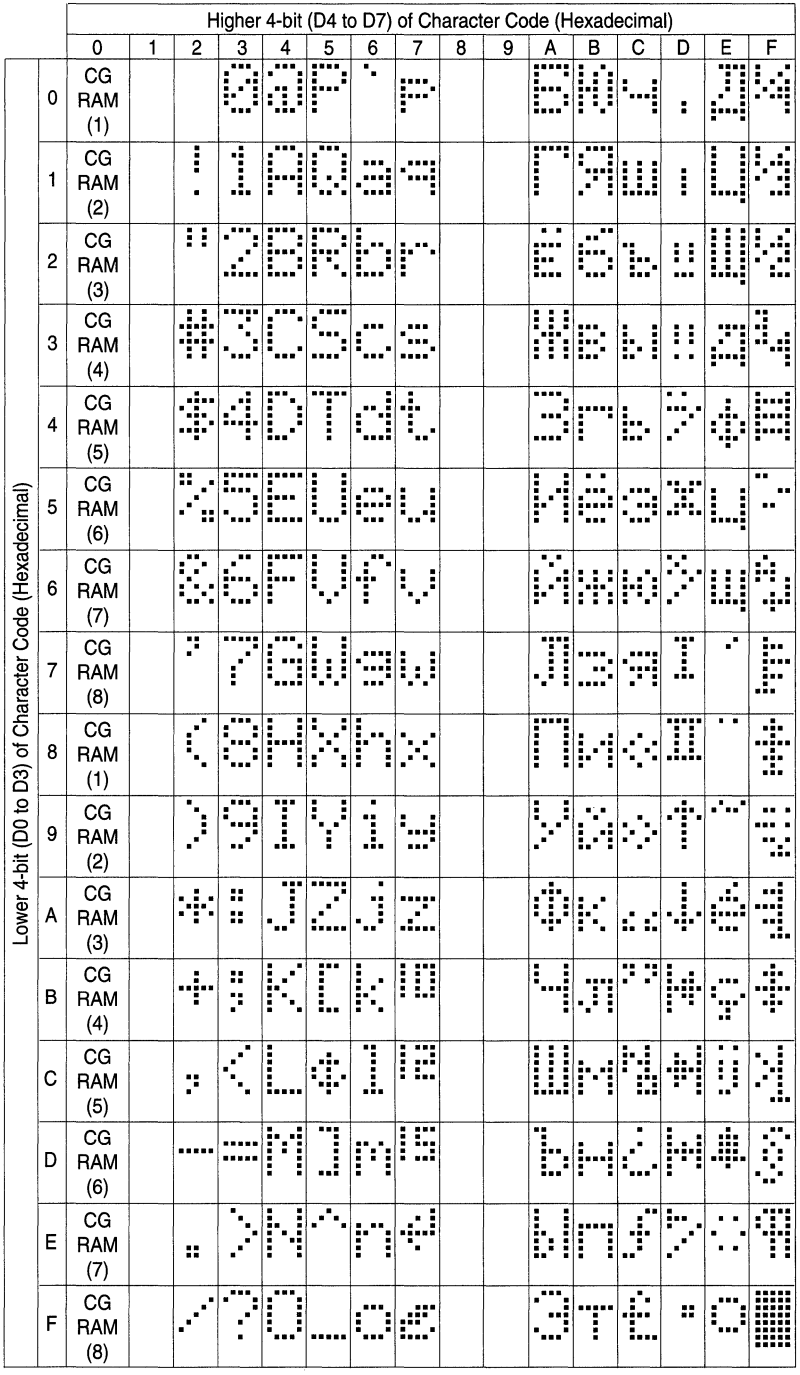
■ SED1278F0D/D0D CHARACTER FONT



■ SED1278F0G/D0G CHARACTER FONT



■ SED1278F0H/D0H CHARACTER FONT



* Character codes (00H-0FH) of SED1278F are assigned to the area of character generator RAM (CG RAM). The CG ROM of the SED1278F is masked; if you wish to have your own CG ROM, consult S-MOS Marketing Department for conversion of the masked ROM.

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CMOS DOT MATRIX LCD CONTROLLER DRIVER

■ DESCRIPTION

The SED1280 is a character LCD controller-driver, capable of driving displays as large as 2 lines of 8 characters (5 × 8 pixels), with minimum external components.

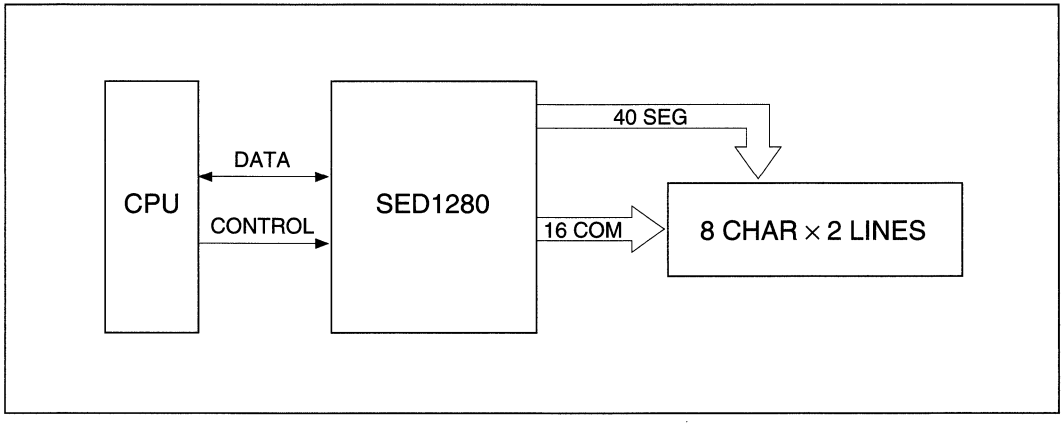
The SED1280 has an internal CGROM consisting of 240 characters (5 × 7) plus the underline cursor, JIS, ASCII, and eight user-programmable characters in RAM.

The SED1280 has 40 segment output and 16 common output built-in. Thus, one chip is capable of displaying up to 16 characters. The SED1280 can display one line of 48 characters using an SED1681F (80-bit output) as an expansions segment driver, since the driver is provided with the SED1278F core. Also, the LSI features serial data interface to interface to MPU, key matrix controller, LED controller and input/output ports. These features are suitable for applications such as facsimile machines.

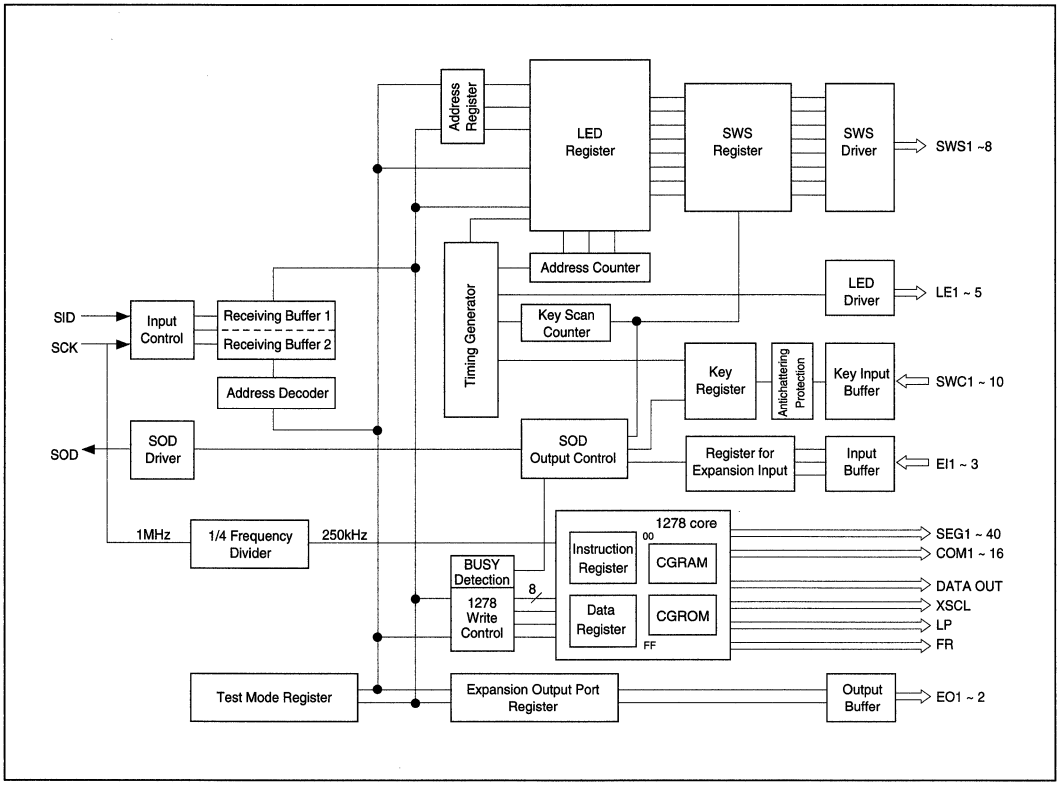
■ FEATURES

- Low-power CMOS technology
- 40 segment output
- 16 common output
- Duty ..... 1/8 or 1/16 (set by command)
- Serial data interface, TTL compatible
- Two-frame AC drive waveform
- CGROM ..... 240 characters
- CGRAM ..... 8 characters
- Display data RAM .... 80 × 8 bits (80 characters)
- Recommended expansion segment driver:
  SED1181 (64-bit output)
  SED1681 (80-bit output)
- Key matrix scan controller:
  Capable of controlling 8 × 10 keys
- LED controller:
  Capable of controlling 5 × 8 LEDs
- I/O ports ..... 3 input, 2 output
- Built-in RC oscillator
- Built-in LCD driver voltage-divider network
- TTL compatible CPU interface
- Supply voltage: .. Logic ..... 4.5V to 5.5V
  LCD ..... 3.5V to 5.5V
- Package: ..... QFP5-100 pins (F_{OA}, F_{OB}, F_{OC})
  Al pad (D_{OA}, D_{OB}, D_{OC})

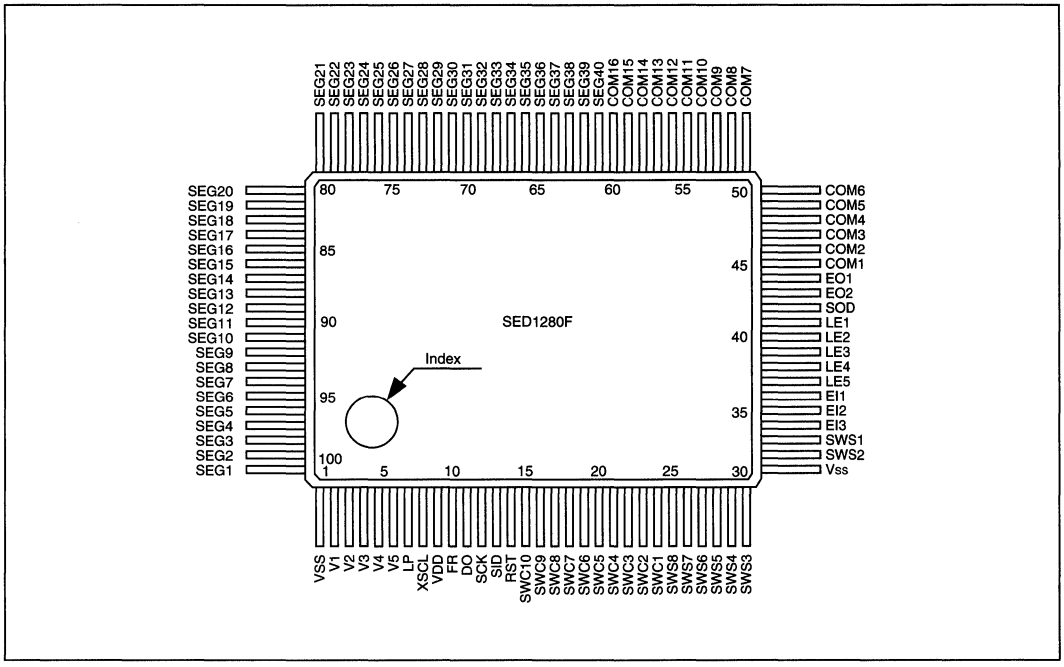
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT


SEG21 SEG22 SEG23 SEG24 SEG25 SEG26 SEG27 SEG28 SEG29 SEG30 SEG31 SEG32 SEG33 SEG34 SEG35 SEG36 SEG37 SEG38 SEG39 SEG40 COM16 COM15 COM14 COM13 COM12 COM11 COM10 COM9 COM8 COM7
SEG20 SEG19 SEG18 SEG17 SEG16 SEG15 SEG14 SEG13 SEG12 SEG11 SEG10 SEG9 SEG8 SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1
80 75 70 65 60 55 50
85
45
90
40
95
35
100 1 5 10 15 20 25 30
SED1280F
Index
COM6 COM5 COM4 COM3 COM2 COM1 EO1 EO2 SOD LE1 LE2 LE3 LE4 LE5 EI1 EI2 EI3 SWS1 SWS2 Vss
VSS V1 V2 V3 V4 V5 LP XSCL VDD FR DO SCK SID RST SWC10 SWC9 SWC8 SWC7 SWC6 SWC5 SWC4 SWC3 SWC2 SWC1 SWS8 SWS7 SWS6 SWS5 SWS4 SWS3

■ PIN DESCRIPTION

Pin Name	I/O	Pull-up resistance	Functions	Number of terminals
SID	I	None	Serial data input	1
SOD	O	—	Serial data output. (For use input status of expansion input port (EI) and key input port (SWC))	1
SCK	I	None	1 MHz system clock input. System clock synchronized serial data input/output, LCD display and key input control.	1
Segment driver signal output pin for expansion				
LP	O	—	Data latching pulse	1
XSCL	O	—	Data transfer clock	1
FR	O	—	LCD AC driving signal	1
D0	O	—	Serial data	1
LCD AC drive pin				
COM1 to COM16	O	—	Common output	16
SEG1 to SEG40	O	—	Segment output	40
V1 to V5	Power supply	—	LCD driving power	5
Key/LED control pin				
SWS1 to SWS8	O	—	Output port for commonly driving key and LED by time sharing	8
LE1 to LE5	O	—	LED driver	5
SWC1 to SWC10	I	Existing	Key input port	10
Expansion input port				
EI1 to EI3	I	—	Input port, 3 input port	3
Expansion output port				
EO1 to EO2	O	—	Output port, 2	2
RST	I	—	System reset	1
Power supply pin				
V_{DD}	Power supply	—	+5V	1
V_{SS}	Power supply	—	0V (GND)	2

DISCONTINUED

SED1500 Series

CMOS DOT MATRIX LCD CONTROLLER DRIVER

■ DESCRIPTION

The SED1500 Series is a dot matrix LCD driver CMOS LSI with the ability of alpha-numeric and graphic display. The device stores the parallel data that is sent from the microcomputer in a built-in data RAM and generates a liquid drive signal. The LSI can be connected directly to the 4-bit/8-bit microcomputer. The SED1500 Series is suitable to applications involving low speed, large capacity. The device consumes only a little current because it is operated by a low-frequency clock so that, by combining it with a CMOS microcomputer unit, a battery driven, long life system can be built at low cost.

■ FEATURES

- Low-power CMOS technology
- Direct CPU interface ..... 4/8 bits
- Duty cycle ..... 1/7 to 1/16 (mask option)
- Built-in display data RAM ..... 42 × 2 bytes
  Maximum ..... 672 dots
- On-chip CR oscillation circuit
- Master/slave operation is supported
- LCD voltage ..... –3 to –10V
- Single power supply ..... 3.0 to 6.0V
- Package ..... QFP1-80 pin (FOA)

■ SED1500 Series

The capacity of the SED1500 Series is varied as follows with a duty of LCD multiplex drive.

● **Common-single series**

Duty	Type	No. of COM output	No. of SEG output
1/7	SED1507F	7	42
1/8	SED1500F	8	42
1/10	SED1501F	10	40
1/11	*2	11	39
1/12	*2	12	38
1/13	*2	13	37
1/14	*2	14	36
1/15	*2	15	35
1/16	SED1502F	16	34

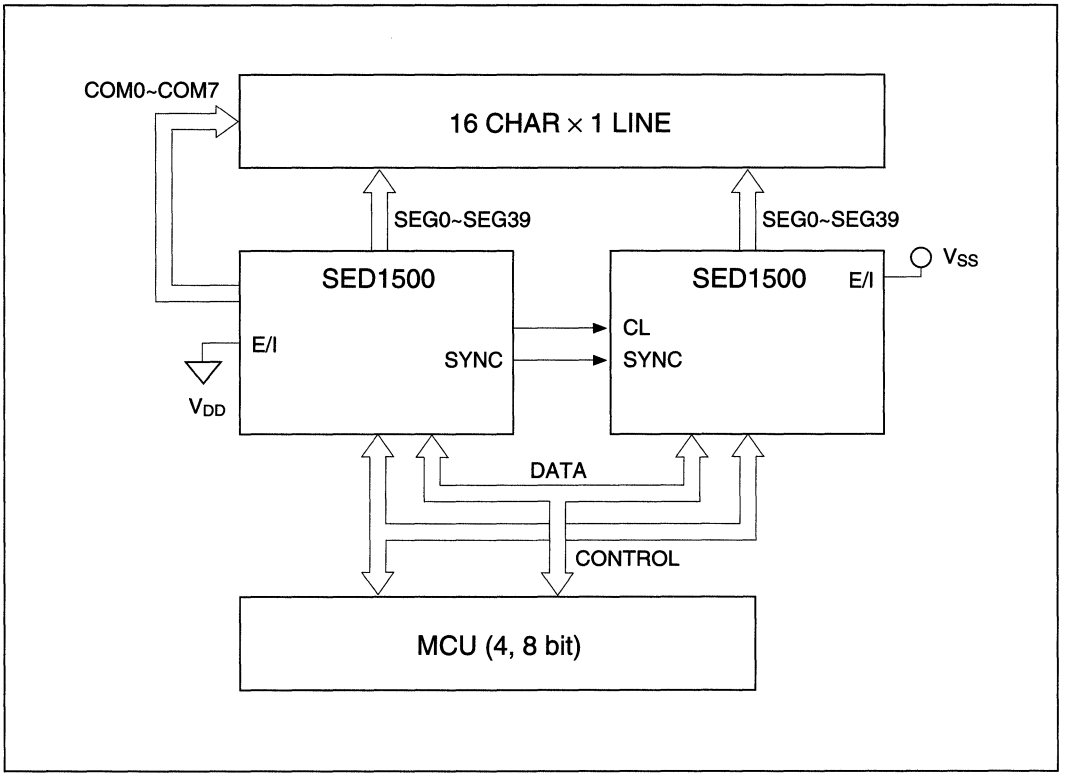
● **Common-multi series**

Duty	Type	No. of COM output	No. of SEG output
1/8	*2	4	42
1/9	*2	5	42
1/10	*2	5	42
1/11	*2	6	42
1/12	*2	6	42
1/13	*2	7	42
1/14	*2	7	42
1/15	*2	8	42
1/16	SED1503F	8	42

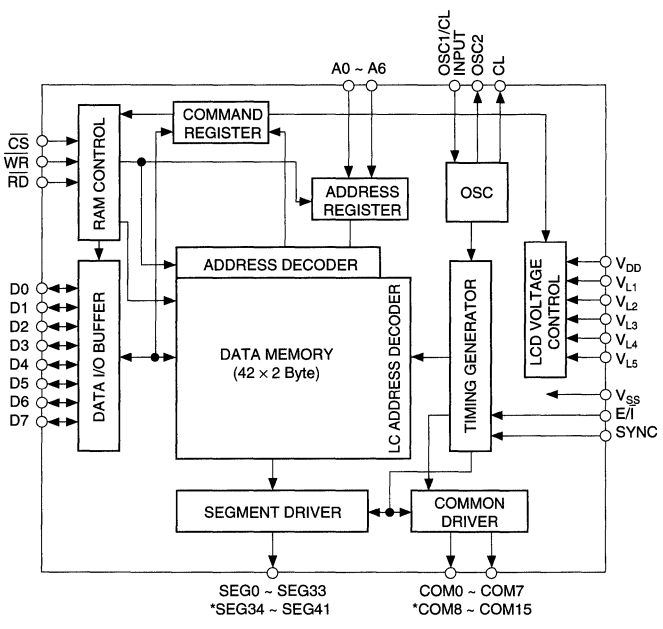
*1. The driver is open-ended by the cascade connection.

*2. Above-mentioned Duties are all available by the mask option. Please consult S-MOS marketing for availability.

■ SYSTEM BLOCK DIAGRAM

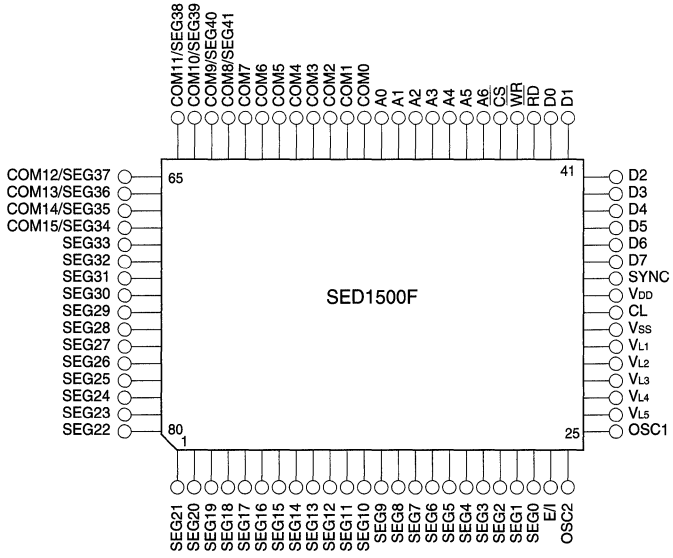


■ BLOCK DIAGRAM



* These terminals can be used as either SEG or COM terminals

■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A6	RAM Address
D0 to D7	Data Input/Output
$\overline{RD}$	Read Enable
$\overline{WR}$	Write Enable
OSC1, OSC2	Oscillation Circuit
$\overline{CS}$	Chip Select Input
CL	Clock Output
E/$\overline{I}$	Master/Slave Selection
SYNC	Slave Synchronous Input/Output

COM0 to COM15	LCD Common (Y) Drive Output
SEG0 to SEG41	LCD Segment (X) Drive Output
V_{L1} to V_{L5}	LCD Drive Power Supply
V_{DD}	Power Supply (+)
V_{SS}	Logic Power Supply (–)

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{SS}	–7.0 to 0.3	V
	V_{L1} to V_{L5}	–13.0 to 0.3	V
Input voltage	V_I	V_{SS}–0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–55 to 125	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

● DC Characteristics

(V_{DD} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Supply voltage	V_{SS}		–3.0	—	–5.5	V
Supply voltage	V_{L5}		–3.0	—	–10	V
Operating dissipation	I_{OP1}	V_{SS}=–5.5V $\overline{CS}$=H V_{L5}=–10.0V R_f=1.0MΩ	—	60	100	μA
Oscillation start voltage	V_{STA}	R_f=1.0MΩ	—	—	–2.0	V
Oscillation stop voltage	V_{STP}	R_f=1.0MΩ	—	—	–2.0	V
Read cycle time	$t_{c(RD)}$	V_{SS}=–5V V_{IH}=V_{OH}=–2.0V V_I=V_{OL}=V_{SS}+0.8V C_L=100pF+1TTL	1,000	—	—	ns
Write cycle time	$t_{c(WR)}$		1,000	—	—	ns
Access time	t_a		—	—	800	ns

● **Timing Characteristics**

○ **Read Operation**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Read cycle time	t_{RC}		1000	—	—	ns
Access time 1	t_{A1}	$V_{IH} = V_{OH} = V_{DD} - 2.0V$	—	—	800	ns
Read input → valid data output time	t_{RD}	$V_{IL} = V_{DL} = V_{SS} + 0.8V$	—	—	800	ns
Read input → data output time	t_{RX}	C_L = 100 pF + 1 TTL	—	—	150	ns
Output disable time	t_{OTD}		30	—	—	ns
Output hold time	t_{OHA}	V_{SS} = –5V ± 10%	20	—	—	ns
Address set pulse width	t_{AS}	T_a = –20 to +75°C	200	—	—	ns
Address hold time	t_{AH}		100	—	—	ns
Port setup time	t_{PS}		200	—	—	ns

○ **Write Operation**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Write recovery time	t_{WC}		1000	—	—	ns
Write time	t_W		800	—	—	ns
Port setup time	t_{PS}		200	—	—	ns
Address setup time	t_{AW}	$V_{IN} = V_{OH} = V_{DD} - 2.0V$	0	—	—	ns
Write recovery time	t_{WR}	$V_{IL} = V_{OL} = V_{SS} + 0.8V$	200	—	—	ns
Output disable time	t_{ODW}	C_L = 100 pF + 1 TTL	—	—	0	ns
Data setup time	t_{DS}	V_{SS} = –5V ± 10%	300	—	—	ns
Data hold time	t_{DH}	T_a = –20 to 75°C	100	—	—	ns
Address set pulse width	t_{AS}		200	—	—	ns
Address hold time	t_{AH}		100	—	—	ns

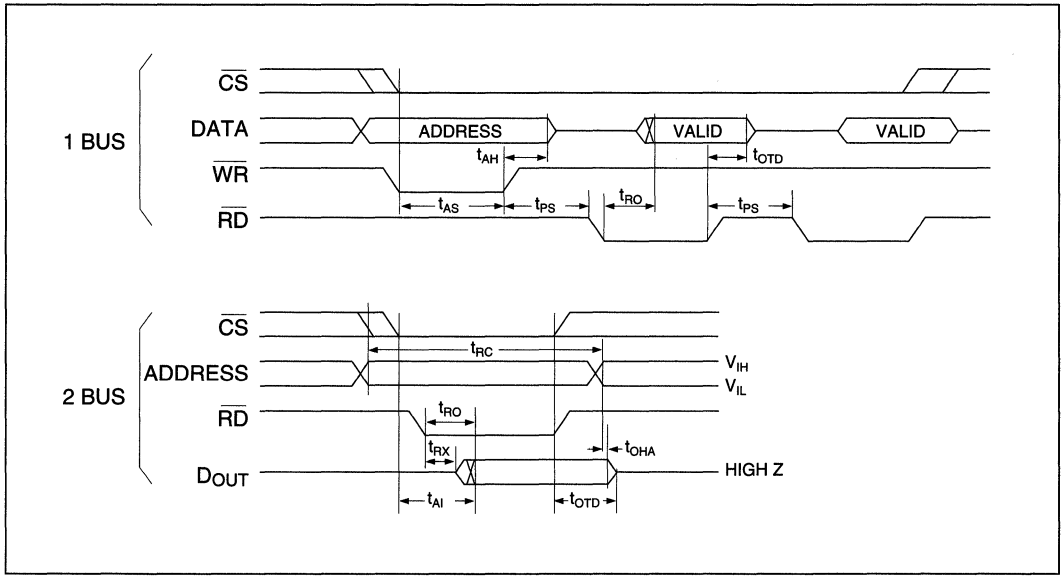
○ **Truth Table**

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0 to A_3	A_4 to A_6	D_{IN}		D_{OUT}		Mode
					D_0 to D_3	D_4 to D_7	D_0 to D_3	D_4 to D_7	
H	*	*	*	*	*	*	High impedance	High impedance	Standby
L	L	H	Stable	Stable**	High impedance	High impedance	Data output	Data output**	Read cycle
L	H	L	Stable	Stable**	Stable	Stable**	High impedance	High impedance	Write cycle

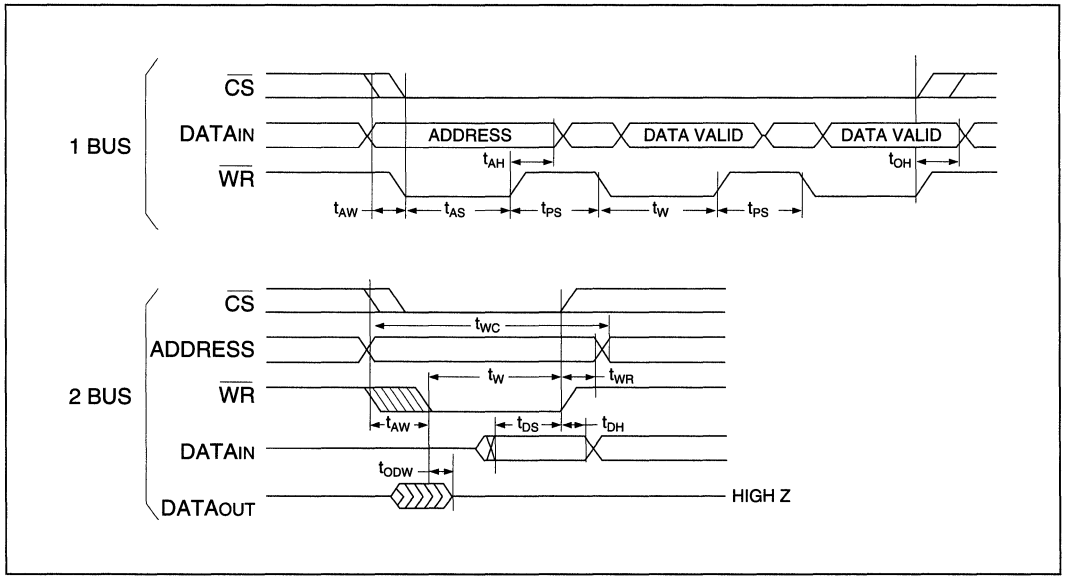
* "H" or "L"

** High impedance in 4-bit mode

- **Timing Diagrams**
  - **Read Operation**

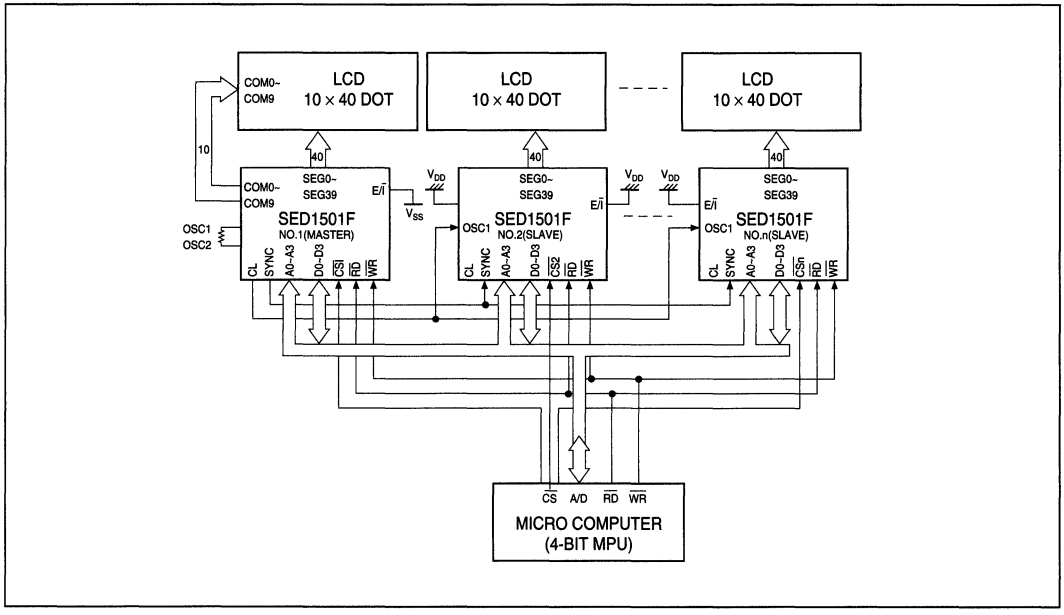


  - **Write Operation**

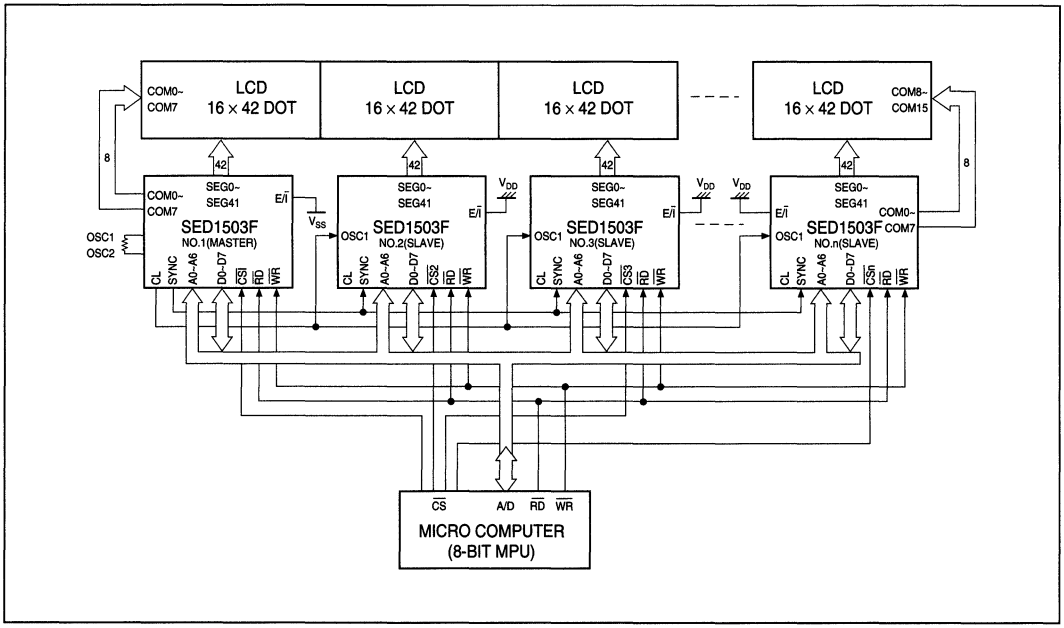


■ EXAMPLE OF APPLICATIONS (Interfacing the SED1500 Series to LCD and MPU)

● **Number of display dots = 10 × 40 × n**
n = 1–10 (in the case of SED1501F)
n = number of driver chips



● **Number of display dots = 16 × 42 × n**
n = 2–10 (in the case of SED1503F)
n = number of driver chips



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CMOS SEGMENT–TYPE LCD CONTROLLER DRIVER

- **Serial Data Interface**
- **Built-in Display data RAM**
- **4 COM Driver Output and 32 SEG Driver Output**

■ DESCRIPTION

The SED1510 is an intelligent CMOS LCD driver-controller for segment type liquid crystal display with the ability of alpha-numeric and graphic application. It can directly drive any static and multiplexed LCD containing up to 4 backplanes and 32 segments.

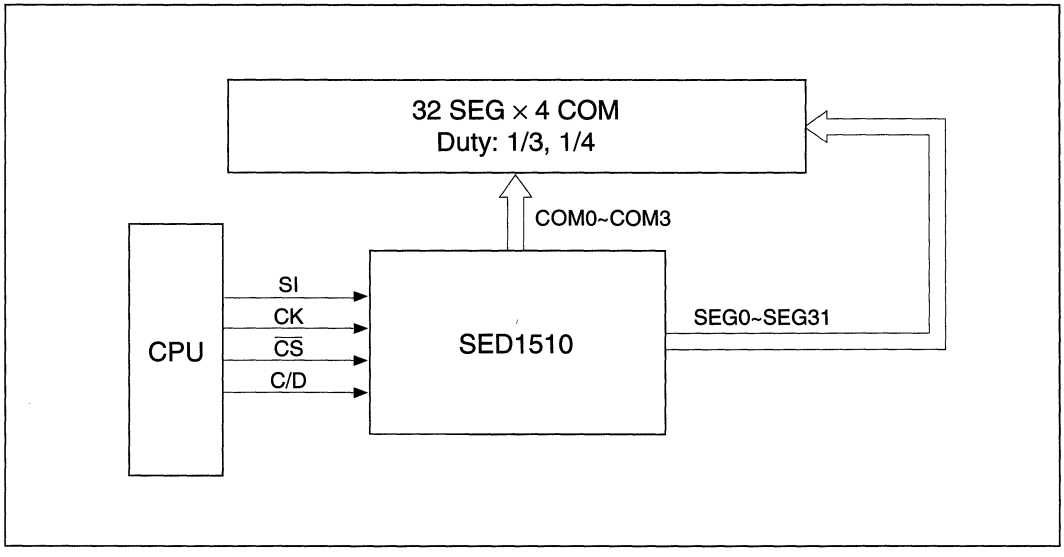
The SED1510 communicates with a host microprocessor through a serial interface. It stores the serial data that is sent from the microprocessor in the built-in data RAM and generates a liquid drive signal.

The SED1510 is manufactured with low power consumption CMOS process allowing use of single power supply between 0.9 and 6.0V.

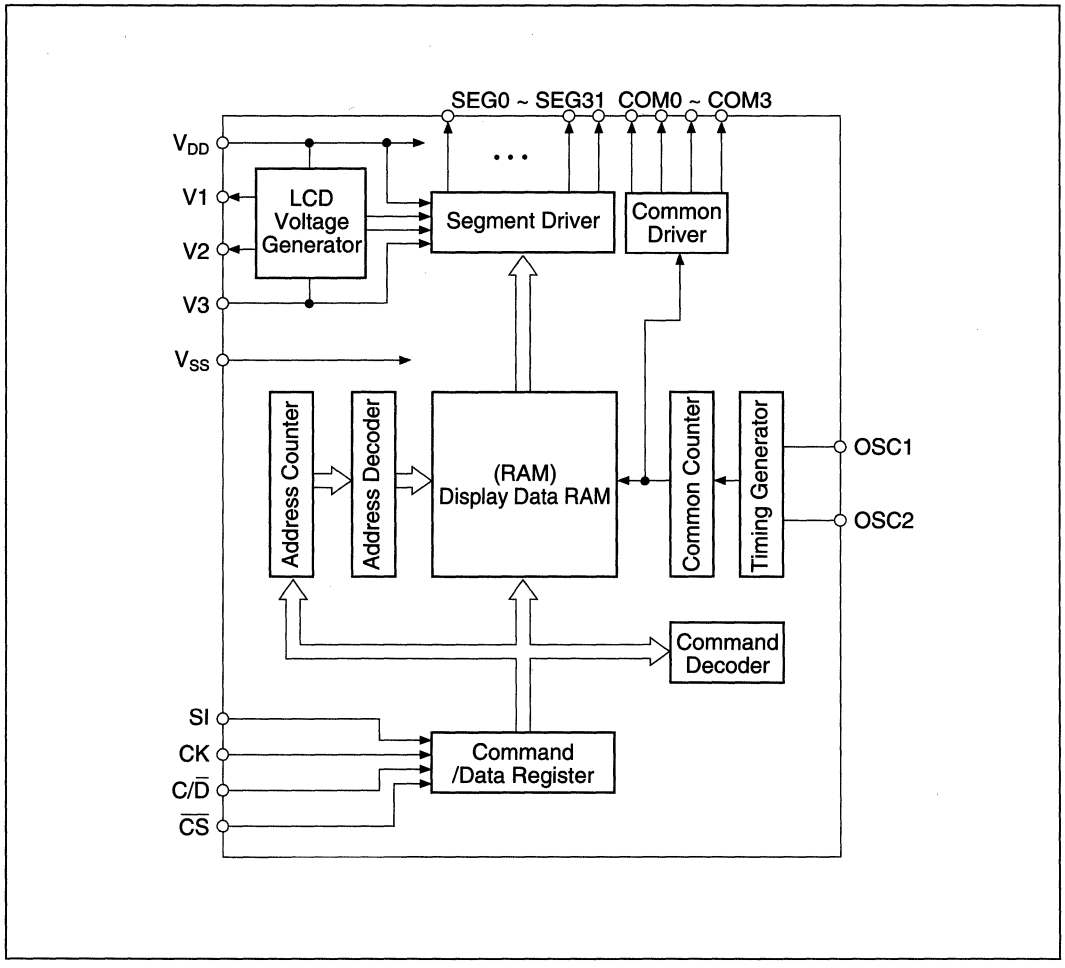
■ FEATURES

- Low-power CMOS technology
- High-speed serial data interface
- Built-in display data RAM (128 bits)
- Provides up to 4 backplanes and 32 segments
- Built-in LCD driver circuitry
- Duty cycle 1/4, 1/3
- Low power consumption .... 150 μW
- Supply voltage ..... 0.9 to 6.0V
- LCD voltage ..... 1.8 to 6.0V
- Package ..... 1510 ..... QFP-12 48-pin (FOC)
  QFP-6 60-pin (FOE)
  Al pad (DOC)

■ SYSTEM BLOCK DIAGRAM

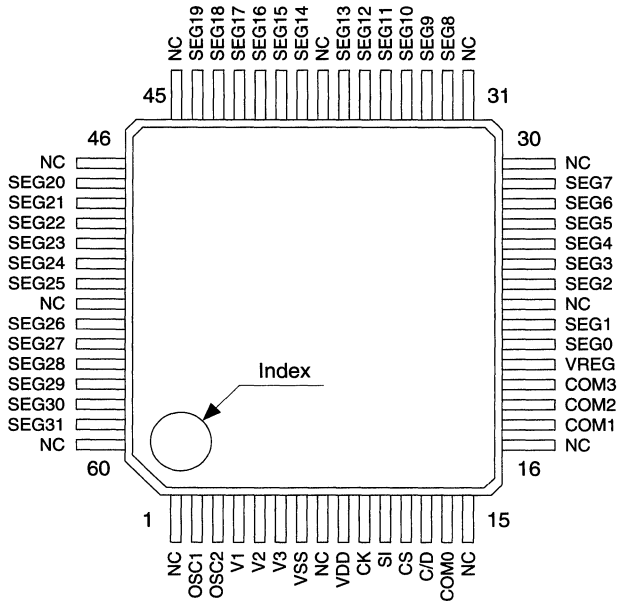


■ BLOCK DIAGRAM



■ PINOUT (SED1510F0C)

SED1510F0C

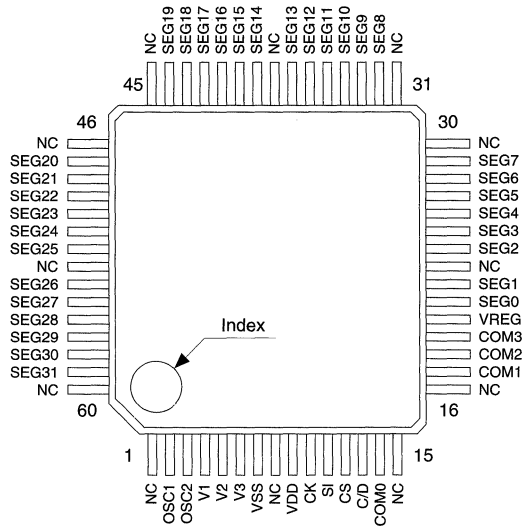


■ PIN DESCRIPTION

Number	Name	Description
1	OSC1	Oscillator feedback resistor connection or external clock input
2	OSC2	Oscillator feedback resistor connection
3	V1	LCD driver voltage monitoring outputs
4	V2	
5	V3	LCD driver supply voltage
6	V_{SS}	Negative supply
7	V_{DD}	Positive supply
8	CK	Serial data clock input
9	SI	Serial data input
10	$\overline{CS}$	Active-LOW chip select input
11	C/$\overline{D}$	Command/data select input
12 to 15	COM0 to COM3	LCD common driver outputs
16	VREG	Regulated voltage monitor output
17 to 48	SEG0 to SEG31	LCD segment driver outputs

■ PINOUT (SED1510F0E)

SED1510F0E



■ PIN DESCRIPTION

Pin No.	Pin Name
1	NC
2	OSC1
3	OSC2
4	V1
5	V2
6	V3
7	VSS
8	NC
9	VDD
10	CK
11	SI
12	CS
13	C/D
14	COM0
15	NC
16	NC
17	COM1
18	COM2
19	COM3
20	VREG

Pin No.	Pin Name
21	SEG0
22	SEG1
23	NC
24	SEG2
25	SEG3
26	SEG4
27	SEG5
28	SEG6
29	SEG7
30	NC
31	NC
32	SEG8
33	SEG9
34	SEG10
35	SEG11
36	SEG12
37	SEG13
38	NC
39	SEG14
40	SEG15

Pin No.	Pin Name
41	SEG16
42	SEG17
43	SEG18
44	SEG19
45	NC
46	NC
47	SEG20
48	SEG21
49	SEG22
50	SEG23
51	SEG24
52	SEG25
53	NC
54	SEG26
55	SEG27
56	SEG28
57	SEG29
58	SEG30
59	SEG31
60	NC

■ AC ELECTRICAL CHARACTERISTICS

V_{DD} = 0V, V_{SS} = –5.0 ± 0.5V, T_a = –20 to 75°C

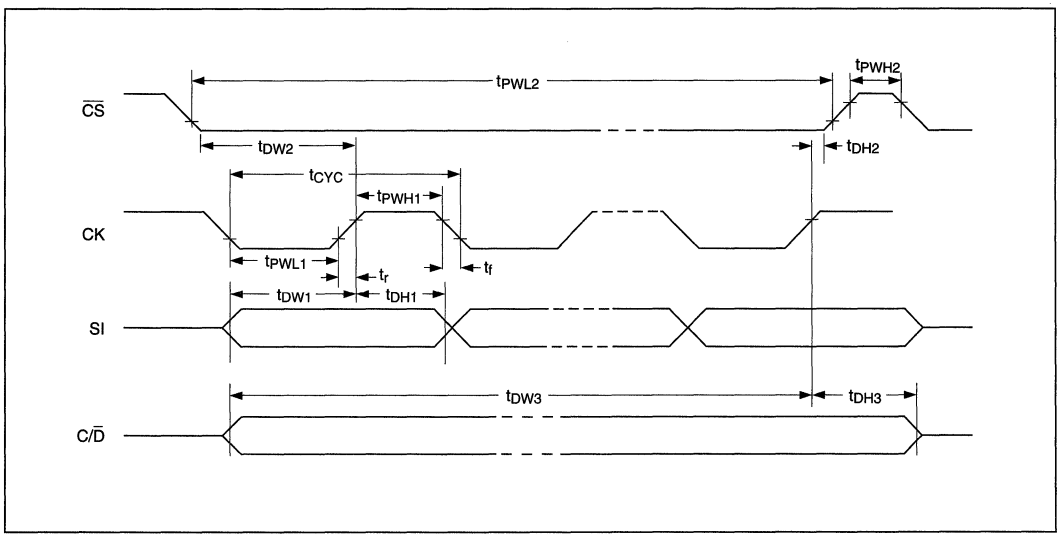
Parameter	Symbol	Condition	Min	Typ	Max	Unit
CK period	t_{CYC}	—	900	—	—	ns
CK LOW-level pulsewidth	t_{PWL1}	—	400	—	—	ns
CK HIGH-level pulsewidth	t_{PWH1}	—	400	—	—	ns
SI to CK setup time	t_{DW1}	—	100	—	—	ns
CK to SI hold time	t_{DH1}	—	200	—	—	ns
$\overline{CS}$ LOW-level pulsewidth	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	7200*1	—	—	ns
$\overline{CS}$ HIGH-level pulsewidth	t_{PWH2}	—	400	—	—	ns
$\overline{CS}$ to CK setup time	t_{DW2}	Referenced to the rising edge of the first CK cycle	100	—	—	ns
CK to $\overline{CS}$ hold time	t_{DH2}	Referenced to the rising edge of the eighth CK cycle	200	—	—	ns
C/$\overline{D}$ to CK setup time	t_{DW3}	Referenced to the rising edge of the eighth CK cycle	9	—	—	µs
CK to C/$\overline{D}$ hold time	t_{DH3}	Referenced to the rising edge of the eighth CK cycle	1	—	—	µs
Rise time	t_r	—	—	—	50	ns
Fall time	t_f	—	—	—	50	ns

*1. $t_{CYC} \times 8$

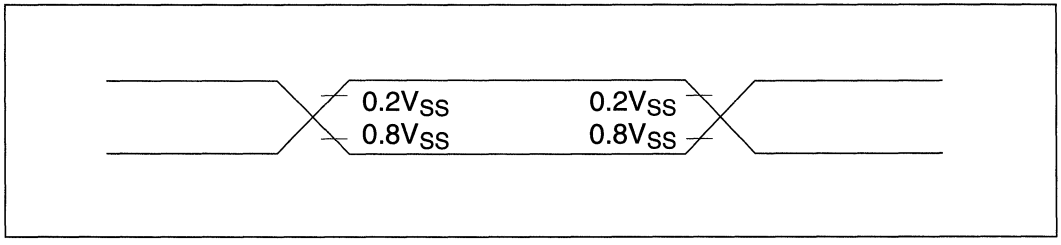
V_{DD} = 0V, V_{SS} = –6.0 to –1.5V, T_a = –20 to 75°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CK period	t_{CYC}	—	10	—	—	µs
CK LOW-level pulsewidth	t_{PWL1}	—	4.5	—	—	µs
CK HIGH-level pulsewidth	t_{PWH1}	—	4.5	—	—	µs
SI to CK setup time	t_{DW1}	—	1.2	—	—	µs
CK to SI hold time	t_{DH1}	—	2.3	—	—	µs
$\overline{CS}$ LOW-level pulsewidth	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	80*1	—	—	µs
$\overline{CS}$ HIGH-level pulsewidth	t_{PWH2}	—	4.5	—	—	µs
$\overline{CS}$ to CK setup time	t_{DW2}	Referenced to the rising edge of the first CK cycle	1.2	—	—	µs
CK to $\overline{CS}$ hold time	t_{DH2}	Referenced to the rising edge of the eighth CK cycle	2.3	—	—	µs
C/$\overline{D}$ to CK setup time	t_{DW3}	Referenced to the rising edge of the eighth CK cycle	100	—	—	µs
CK to C/$\overline{D}$ hold time	t_{DH3}	Referenced to the rising edge of the eighth CK cycle	11	—	—	µs
Rise time	t_r	—	—	—	50	ns
Fall time	t_f	—	—	—	50	ns

*1. $t_{CYC} \times 8$



● **Timing Measurement**

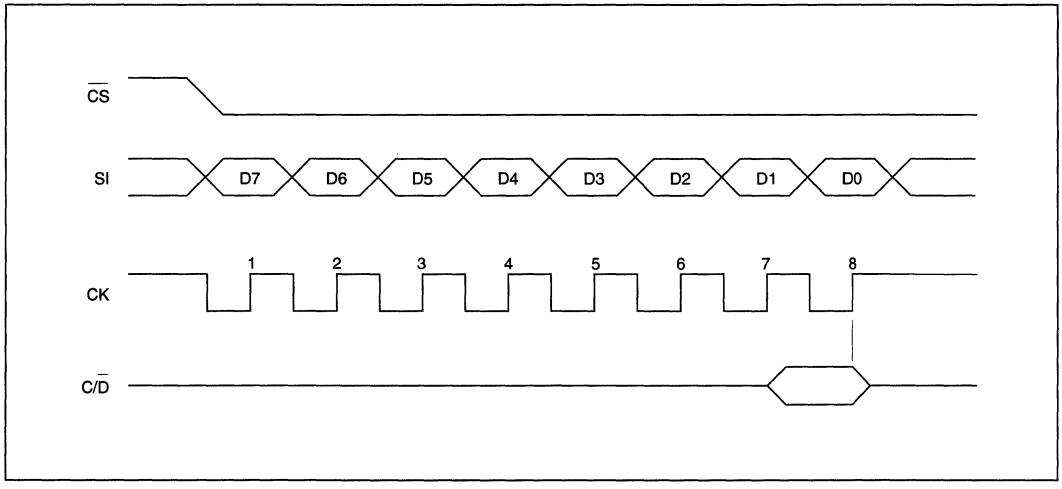


■ FUNCTIONAL DESCRIPTION

● Command/Data Register

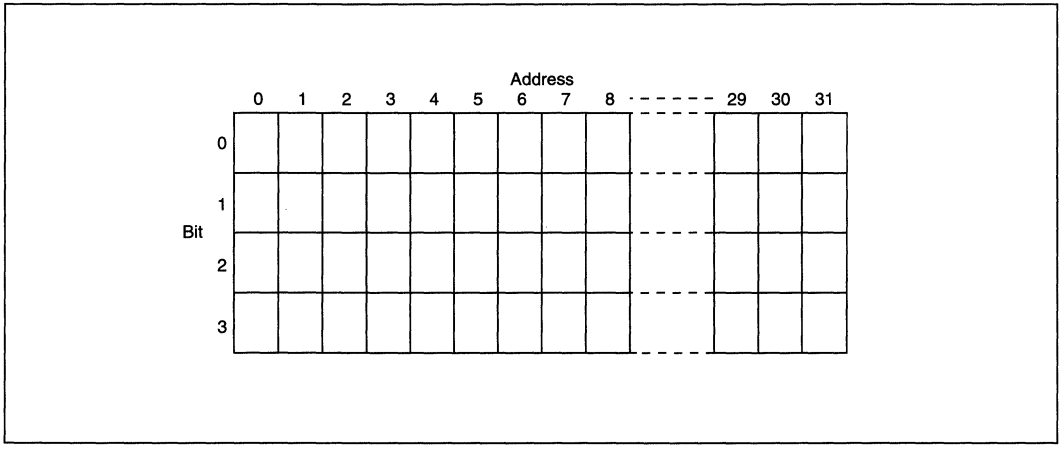
The command/data register comprises an 8-bit shift register and a 3-bit counter. The counter is reset and re-enabled on the falling edge of $\overline{CS}$. The CK counter is initialized when the built-in timing generator circuit (CR oscillating circuit) starts oscillating. The counter is incremented, and the serial input data is shifted into the register on the rising edge of CK. The data is input msb-first as shown in the following figure.

C/$\overline{D}$ is sampled, and the register data is latched into either the display data memory or the command decoder on every eighth rising edge of CK. C/$\overline{D}$ should be set HIGH when a command is input, and LOW, when display data is input.

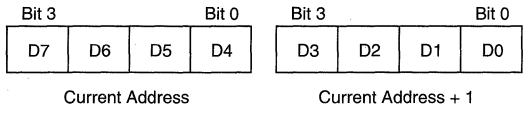


● Display Data Memory

The format of the 32 × 4-bit memory is shown in the following figure.



Each 8-bit display data byte loaded from the command/data register is stored in two consecutive addresses as shown in the following figure. The upper four bits are stored at the location specified by the address counter, and the lower four bits, at the next location. The address counter is automatically incremented by two.



A single 4-bit word can be written to memory using the Data Memory Write command as shown in the following figure. The lower four bits are stored at the location specified by the address counter. The address counter is automatically incremented by one.

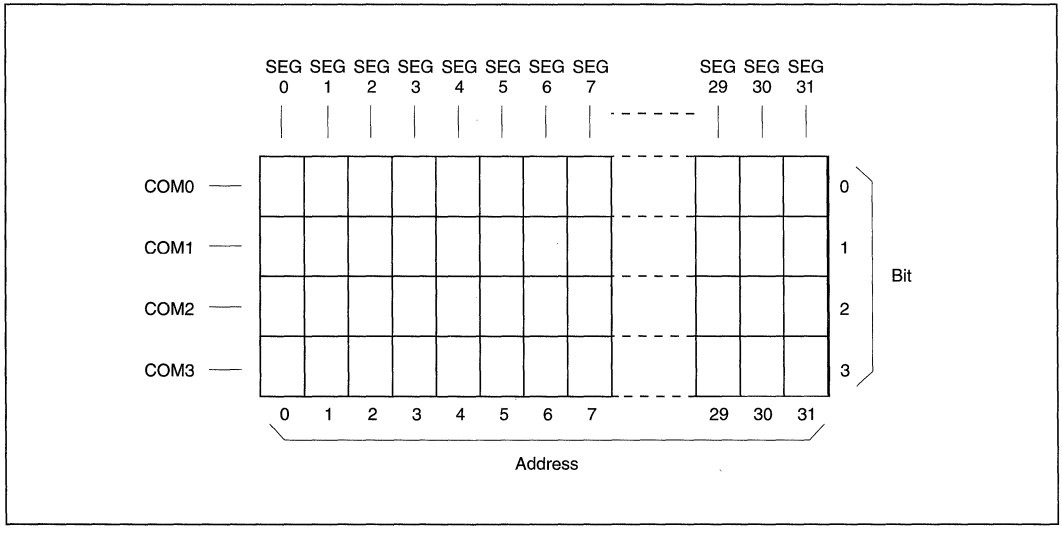
1	0	0	X	D3	D2	D1	D0

Note: x = don't care.

The display data memory address of the SED1511 is automatically incremented by 2 when 8-bit display data is stored.

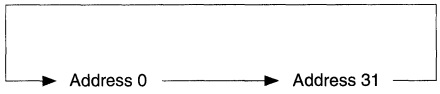
Address 0 is automatically set when the built-in timing generating circuit (CR oscillating circuit) starts oscillating after power on.

Display memory data is output on SEG0 to SEG31 in synchronization with the COM0 to COM3 output scan. The correspondence between memory location and display position is shown in the following figure. When the data is 0, the segment is OFF, and when 1, ON.



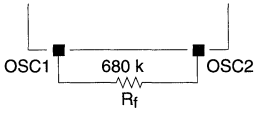
- **Address Counter**

The 5-bit address counter is used to address display data memory. It is set by the Address Set command, and automatically increments when data is stored in the memory. The counter automatically resets to 0 when it increments past 31 as shown in the following figure.

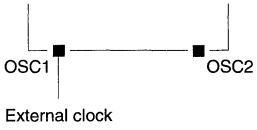


- **Timing Generator**

A low-power oscillator can be constructed using an external feedback resistor as shown in the following figure.



Alternatively, an 18 kHz external clock can be input on OSC1, and OSC2 left open, as shown in the following figure.



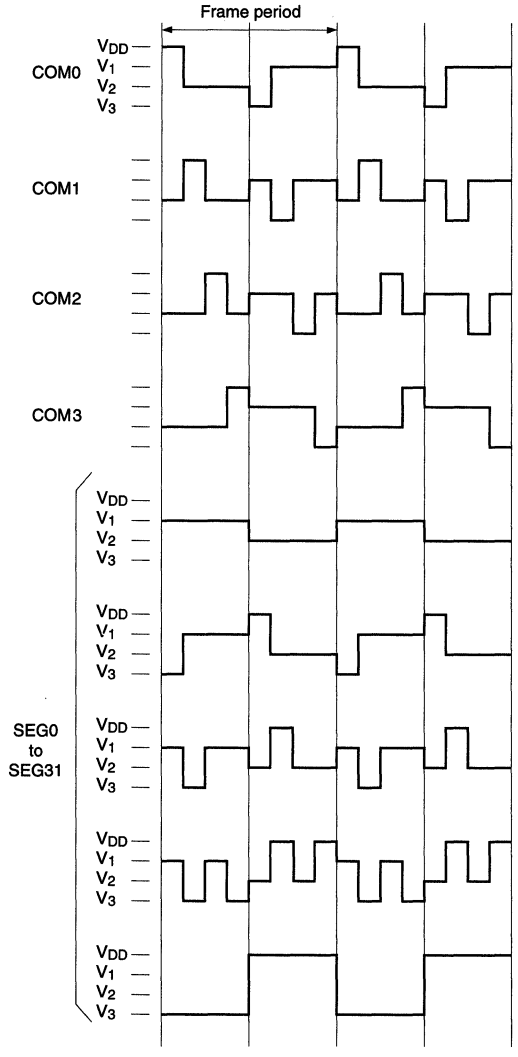
- **Common Counter**

The timing generator clock signal is frequency-divided by the common counter to generate both the common drive timing and the alternating frame timing.

- **Segment and Common Drivers**

The 32 segment drivers and the four common drivers are 4-level outputs that switch between V_{DD} and the V1, V2 and V3 LCD driver voltage levels.

The output states are determined by the display data values and the common counter as shown in the following figure. The outputs are used to drive a 1/3-bias, 1/4-duty LCD panel.



COM0	COM1	COM2	COM3	
0	0	0	0	All segments are OFF.
1	0	0	0	Segments connected to COM0 are ON.
0	1	0	0	Segments connected to COM1 are ON.
0	1	0	1	Segments connected to COM1 or COM3 are ON.
1	1	1	1	All segments are ON.

- **Commands**

The SED1510F0C samples C/D on every eighth rising edge of CK. If C/D is HIGH, the command/data register contents are latched into the command decoder. The command decoder executes the following six commands.

Address Set

Set the address counter to the value specified by D0 to D4.

0	0	0	D4	D3	D2	D1	D0

Display ON

Turn all LCD segments ON. The display memory data is not affected.

0	0	1	X	X	X	X	X

Note: x = don't care.

Display OFF

Turn all LCD segments OFF. The display memory data is not affected.

0	1	0	X	X	X	X	X

Note: x = don't care.

Display Start

Return to normal display mode. The display memory data is output to the display.

0	1	1	X	X	X	X	X

Note: x = don't care.

Memory Write

Store the data D0 to D3 at the location specified by the address counter. The address counter is automatically incremented by one. The other display memory locations are not affected.

1	0	0	X	D3	D2	D1	D0

Note: x = don't care.

Reset

Reset the SED1510F0C. The SED1510F0C then enters normal operating mode, and the display turns OFF.

1	1	0	X	X	X	X	X

Note: x = don't care.

■ APPLICATION NOTE

● Supply Voltages

In addition to V_{DD}, there are three LCD supply voltages: V1, V2 and V3. V3 is supplied externally, whereas V1 and V2 are generated internally. V1, V2 and V3 are given by the following equations:

$V1 = V_{DD} - 1/3\ V_{LCD}$

$V2 = V_{DD} - 2/3\ V_{LCD}$

$V3 = V_{DD} - V_{LCD}$

where V_{LCD} is the LCD drive voltage. The voltages must be such that $V_{DD} \geq V1 \geq V2 \geq V3$.

LCD supply voltage connections when the LCD drive supply is connected to Vss are shown in Figure 1, below, and the connections when the drive supply is independent of Vss, in Figure 2.

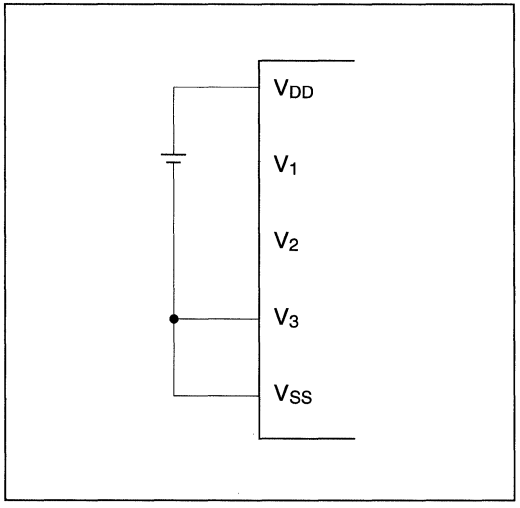


Figure 1. LCD drive supply connected to Vss

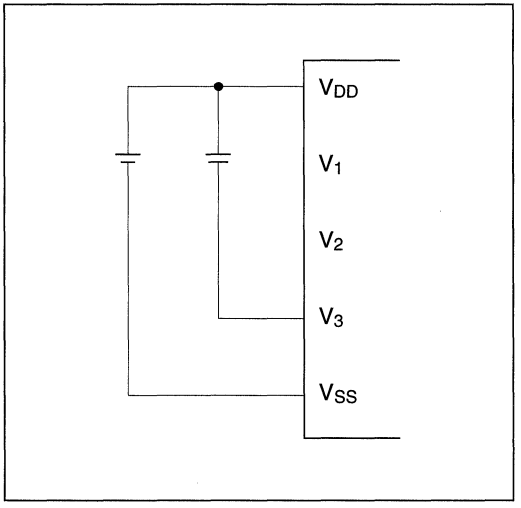
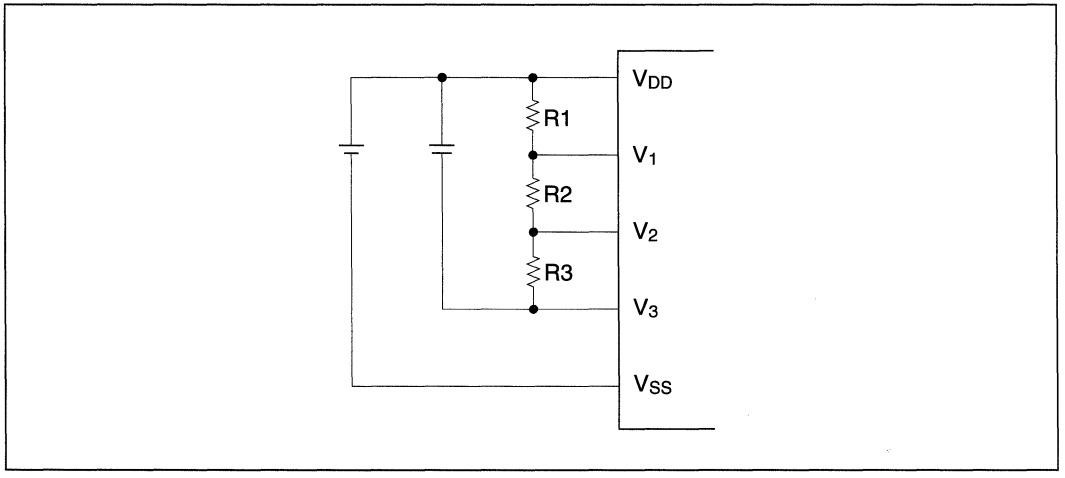
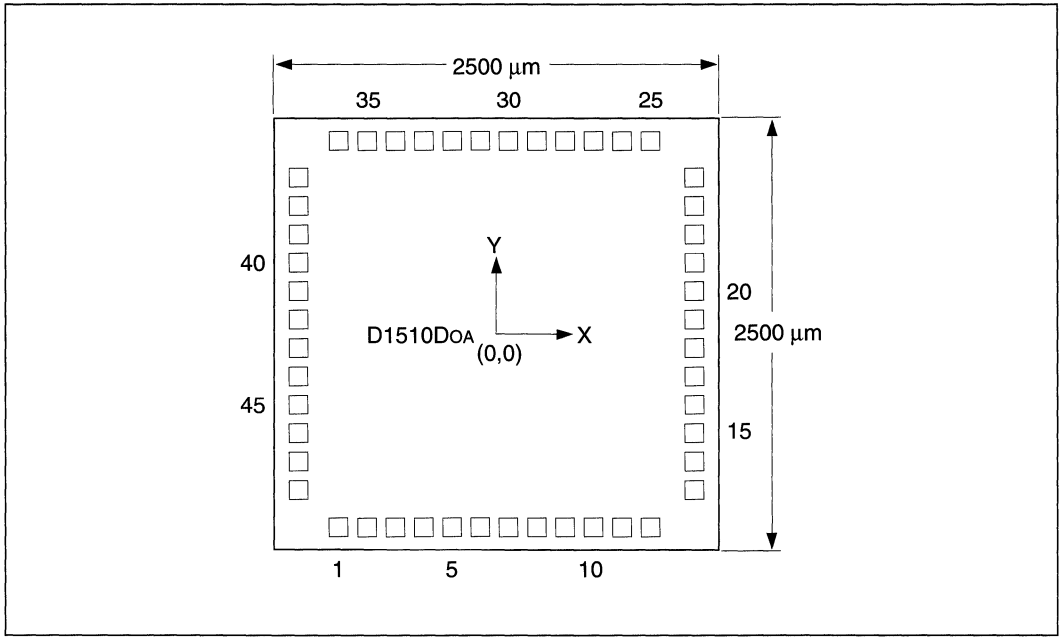


Figure 2. LCD drive supply not connected to Vss

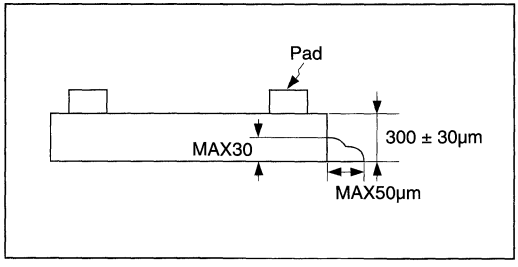
When there is a lot of distortion in the LCD drive waveforms, connect bleeder resistors as shown in the following figure.



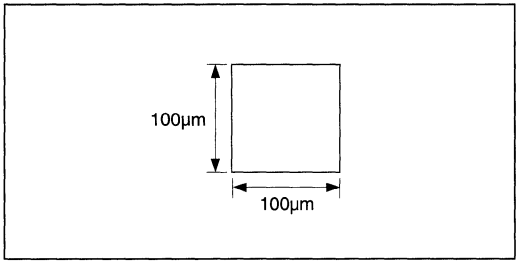
■ PAD LAYOUT AND COORDINATES (SED1510D0A)



● Sectional Dimensions



● Size of Pad Opening



● **Pad Coordinates**

unit: μm

Pad No.	Pad Name	X	Y
1	OSC1	–898	–1091
2	OSC2	–738	–1091
3	V1	–578	–1091
4	V2	–418	–1091
5	V3	–258	–1091
6	Vss	–98	–1091
7	VDD	63	–1091
8	CK	223	–1091
9	SI	383	–1091
10	NC	543	–1091
11	NC	703	–1091
12	COM0	863	–1091
13	COM1	1091	–898
14	COM2	1091	–738
15	COM3	1091	–578
16	VREG	1091	–418
17	SEG0	1091	–258
18	SEG1	1091	–98
19	SEG2	1091	63
20	SEG3	1091	224
21	SEG4	1091	383
22	SEG5	1091	543
23	SEG6	1091	703
24	SEG7	1091	863

Pad No.	Pad Name	X	Y
25	SEG8	898	1091
26	SEG9	738	1091
27	SEG10	578	1091
28	SEG11	418	1091
29	SEG12	258	1091
30	SEG13	98	1091
31	SEG14	–63	1091
32	SEG15	–223	1091
33	SEG16	–383	1091
34	SEG17	–543	1091
35	SEG18	–703	1091
36	SEG19	–863	1091
37	SEG20	–1091	898
38	SEG21	–1091	578
39	SEG22	–1091	578
40	SEG23	–1091	418
41	SEG24	–1091	258
42	SEG25	–1091	98
43	SEG26	–1091	–223
44	SEG27	–1091	–223
45	SEG28	–1091	–383
46	SEG29	–1091	–543
47	SEG30	–1091	–703
48	SEG31	–1091	–863

Note: The origin is the center of the chip. The chip size is 2,500 × 2,500.

■ DESCRIPTION

The SED1520 is a dot matrix LCD driver LSI intended for display of characters and graphics. The bit-addressable display data which is sent from a microcomputer is stored in a built-in display data RAM and generates the LCD drive signal.

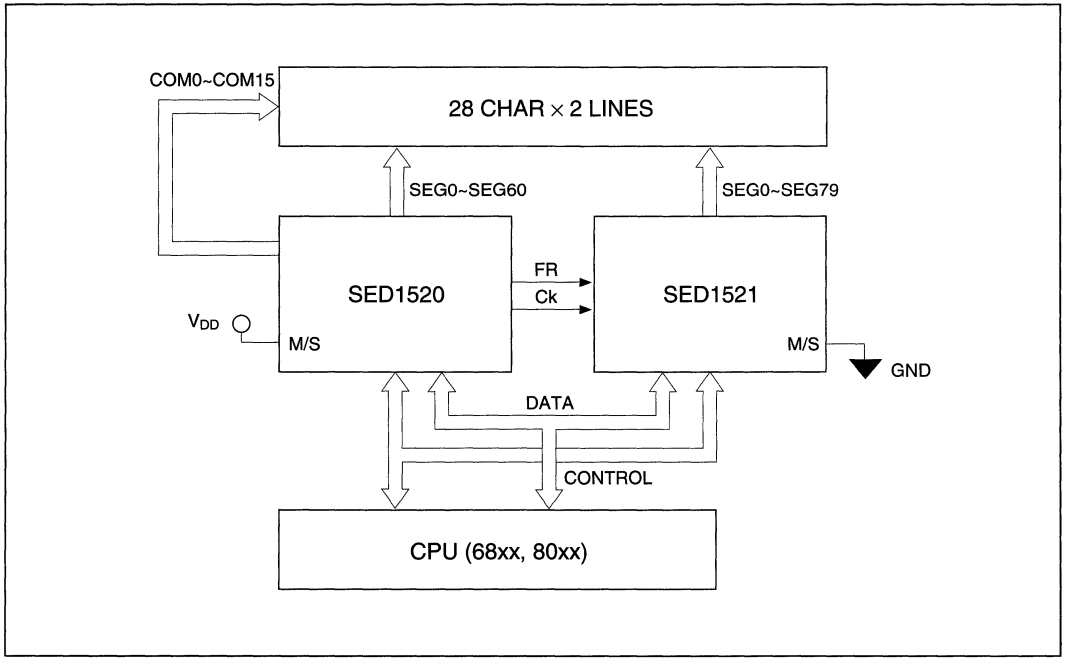
The SED1520 incorporates innovative circuit design strategies to assure very low current dissipation and a wide range of operating voltages. With these features, the SED1520 permits the user to implement high-performance handy systems operating from a miniature battery.

In order for the user to adaptively configure his system, the SED1520 family offers two application forms. One form allows an LCD display of 12 characters × 2 lines with an indicator with a single chip. The other is dedicated to driving a total of 80 segments, enabling a medium-size display to be achieved by using a minimum number of drivers.

■ FEATURES

- Low-power CMOS technology
- Fast CPU 8-bit data interface (80xx, 68xx)
- Segment output ..... 61 outputs
- Common output ..... 16 outputs
- Duty cycle ..... SED1520 ..... 1/16 to 1/32
  SED1521 ..... 1/8 to 1/32
- Built-in display data RAM ..... 2560 bits
- Rich display command setting
- On-chip CR oscillation circuit
- Recommended expansion segment driver: 80 bit
- Master/slave operation is supported
- Low power consumption 30μW
- LCD voltage ..... 3.5 to 13V
- Single power supply ..... 2.4 to 7.0V
- Package ..... QFP5-100 pin (F_{0A}, F_{AA})
  QFP15-100 pin (F_{0C}, F_{AC})
  Al pad (D_{0A}, D_{AA})
  Au bump (D_{0B}, D_{AB})
  TAB (T_{0A})

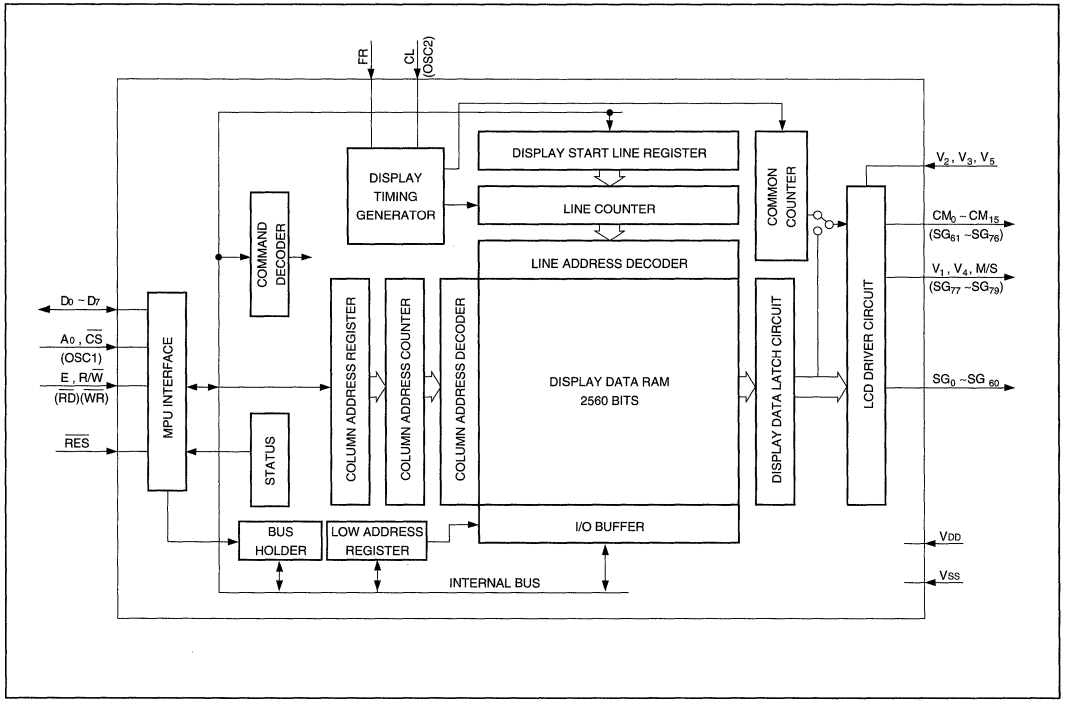
■ SYSTEM BLOCK DIAGRAM



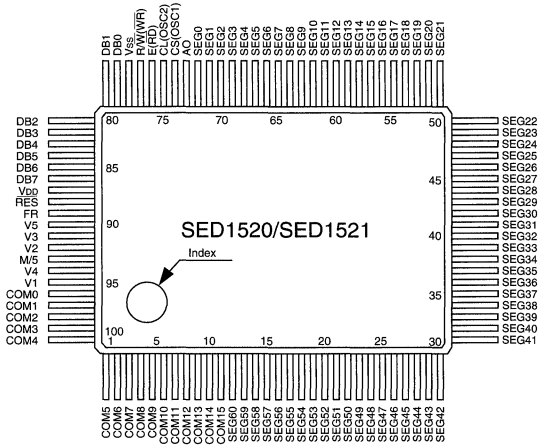
- SED1520 family specifications:

Product Name	Clock Frequency		Applicable Driver	No. of SEG Drivers	No. of COM Drivers
	On Chip	External			
SED1520F0A	18kHz	18kHz	SED1520F0A, SED1521F0A	61	16
SED1521F0A	—	18kHz		80	0
SED1520FAA	—	2kHz	SED1520FAA, SED1521FAA, HD44103CH	61	16
SED1521FAA	—	2kHz		80	0

■ BLOCK DIAGRAM



■ PINOUT



Model Name	Terminal No.	
	74	75
SED1520FO*	OSC1	OSC2
SED1520FA*	CS	CL

The Common output COM0 to COM15 of the Master LSI corresponds COM31 to COM16 on the Slave LSI.

■ PIN DESCRIPTION

Terminal Name	Function
DB0~DB7	Data input
A0	Selects display data or instructions. HIGH: Display data. LOW: Instructions.
$\overline{RES}$	Resets the system and selects the interface type for a 68-port/80-port MPU. HIGH: 68-port MPU interface. LOW: 80-port MPU interface.
$\overline{CS}$	Chip Select input. LOW: Active level sensing.
E (RD)	Read/Write Enable signal when a 68-port MPU is connected. (Active-LOW Read Enable signal when an 80-port MPU is connected.)
R/$\overline{W}$ ($\overline{WR}$)	Read/Write Select signal when a 68-port MPU is connected. HIGH: Read Select LOW: Write Select (Active-LOW Write Enable input when an 80-port MPU is connected. Rising edge sensing.)
CL	External clock input (only effective with external clock types).
FR	LCD Frame (AC-conversion) signal input/output.
SEG0~SEG60	Segment output for driving the LCD.
COM0~COM15 (COM31~COM16)	Common output for driving the LCD.
M/S	Master/Slave Select signal
V_{DD}	5V power supply.
V_{SS}	0V power supply (GND level).
V1, V2, V3, V4, V5	Power supplies for driving the LCD. $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

■ MODEL CLASSIFICATION

Model Name	Operating Clock		Connectable Drivers	SEG Driver	COM driver
	Internal oscillator	External clock			
SED1520FO*	18 KHz	18 kHz	SED1520FO*, SED1521FO*	61 ports	16 ports
SED1520FA*	—	2 KHz	SED1520FA*, SED1521FA*	61 ports	16 ports

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0V, $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–8.0 to 0.3	V
Supply voltage (2)	V5	–16.5 to 0.3	V
Supply voltage (3)	V1, V4 V2, V3	V5 to 0.3	V
Input voltage	V_I	V_{SS}–0.3 to 0.3	V
Output voltage	V_O	V_{SS}–0.3 to 0.3	V
Permissible loss	P_D	250	mV
Operating temperature	T_{opr}	–30 to 85	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature	T_{sol}	260°C for 10 s (at leads)	—

● DC Characteristics

V_{DD} = 0V, Ta = −20 to 75°C

Parameter		Symbol	Condition		Min	Typ	Max	Unit	Applicable Pin
Operating voltage (1)*1	Recommended	V_{SS}			−5.5	−5.0	−4.5	V	V_{SS}
	Potential				−7.0	—	−2.4		
Operating voltage (2)	Recommended	V5			−13.0	—	−3.5	V	V5
	Potential				−13.0	—	—		
	Potential	V1, V2			0.6×V5	—	V_{DD}	V	V1, V2
	Potential	V3, V4			V5	—	0.4×V_{DD}	V	V3, V4
HIGH input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	*2
		V_{IHC}			0.2×V_{SS}	—	V_{DD}	V	*3
LOW input voltage		V_{ILT}			V_{SS}	—	V_{SS}+0.8	V	*2
		T_{ILC}			V_{SS}	—	0.8×V_{SS}	V	*3
HIGH output voltage		V_{OHT}	I_{OH}= −3.0mA		V_{SS}+2.4	—	—	V	D0~D7 pins
		V_{OHC1}	I_{OH}= −2.0mA		V_{SS}+2.4	—	—	V	FR pins
		V_{OHC2}	I_{OH}= −120µA		0.2×V_{SS}	—	—	V	OSC2
LOW output voltage		V_{OLT}	I_{OL}=3.0mA		—	—	V_{SS}+0.4	V	D0~D7, FR pins
		V_{OLC1}	I_{OL}=2.0mA		—	—	V_{SS}+0.4	V	FR pins
		V_{OLC2}	I_{OL}=120µA		—	—	0.8×V_{SS}	V	OSC2
Input leak current		I_{LI}			−1.0	—	1.0	µA	*4
Output leak current		I_{LO}	Applicable when FR is in a high-impedance state		−3.0	—	3.0	µA	D0~D7, FR pins
LCD driver ON resistance		R_{ON}	Ta=25°C	V5=−5.0V	—	5.0	7.5	kΩ	SEG0~60
				V5=−3.5V	—	10.0	50.0		COM0~15
Static current consumption		I_{DDQ}	$\overline{CS}$=CL=V_{DD}		—	0.05	1.0	µA	V_{DD}
Dynamic current dissipation	External CLK Oscillator	During $I_{DD(1)}$	f_{CL}=2kHz display	—	2.0	5.0		µA	V_{DD}
				R_f=1MΩ	—	9.5	15.0		
				f_{CL}=18kHz	—	5.0	10.0		
		$I_{DD(2)}$	During access t_{cyc}=200kHz		—	300	500	µA	V_{DD}
Input terminal capacity		C_{IN}	Ta=25°C	f=1MHz	—	5.0	8.0	pF	All input terminals
Oscillation frequency		f_{OSC}	R_f=1.0MΩ±2%	V_{SS}= −5.0V	15	18	21	kHz	
			R_f=1.0MΩ±2%	V_{SS}= −3.0V	11	16	21		
Reset time		t_R			1.0	—	1000	µs	$\overline{RES}$

Notes:

*1. A wide range of operating voltages is guaranteed, except in case of abrupt voltage fluctuations during MPU access.

*2. A0, D0~D7, E, R/$\overline{W}$ and $\overline{CS}$ pins.

*3. CL, FR, M/$\overline{S}$ and $\overline{RES}$ pins.

*4. A0, E, R/$\overline{W}$, $\overline{CS}$, CL, $\overline{RES}$, M/$\overline{S}$ pins.

● AC Characteristics

○ Read/Write timing for the 80-port MPU

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

Parameter	Signal	Symbol	Condition	Rating			Unit
				Min	Typ	Max	
Address hold time	A0, $\overline{CS}$	t_{AHB}		10	—	—	ns
Address set-up time		t_{AWB}		20	—	—	ns
System cycle time	$\overline{WR}$, $\overline{RD}$	t_{CYC8}		1000	—	—	ns
Control pulse width		t_{CC}		200	—	—	ns
Data set-up time	D0 ~ D7	t_{DS8}		80	—	—	ns
Data hold time		t_{DH8}		10	—	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	—	—	90	ns
Output disable time		t_{OH8}		10	—	60	ns

*2. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

○ Read/Write timing for the 68-port MPU

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

Parameter		Signal	Symbol	Condition	Rating			Unit
					Min	Typ	Max	
System cycle time		A0, $\overline{CS}$ R/$\overline{W}$	t_{CYC6} *3		1000	—	—	ns
Address set-up time			t_{AW6}		20	—	—	ns
Address hold time			t_{AH6}		10	—	—	ns
Data set-up time		D0 ~ D7	t_{DS6}		80	—	—	ns
Data hold time			t_{DH6}		10	—	—	ns
Output disable time			t_{OH6}	C_L = 100pF	10	—	60	ns
Access time			t_{ACC6}		—	—	90	ns
Enable pulse width	READ	E	t_{EW}		100	—	—	ns
	WRITE				80	—	—	ns

*3. t_{CYC6} indicates the cycle during which $\overline{CS}$/E are HIGH; it does not indicate the cycle of the E signal.

*4. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

○ Control timing for 80-port/68-port display

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

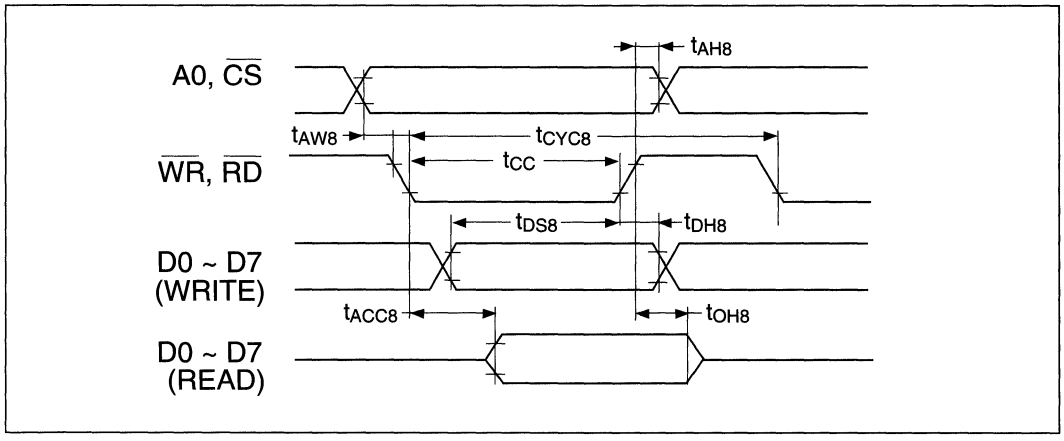
Parameter	Signal	Symbol	Condition	Rating			Unit
				Min	Typ	Max	
LOW pulse width	CL	t_{WLCL}		35	—	—	µs
HIGH pulse width		t_{WHCL}		35	—	—	µs
Rising time		t_r		—	30	150	ns
Falling time		t_f		—	30	150	ns
FR delay time	FR	t_{DFR}	(Input timing)	–2.0	0.2	2.0	µs
			(Output timing), C_L = 100pF	—	0.2	0.4	

*5. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

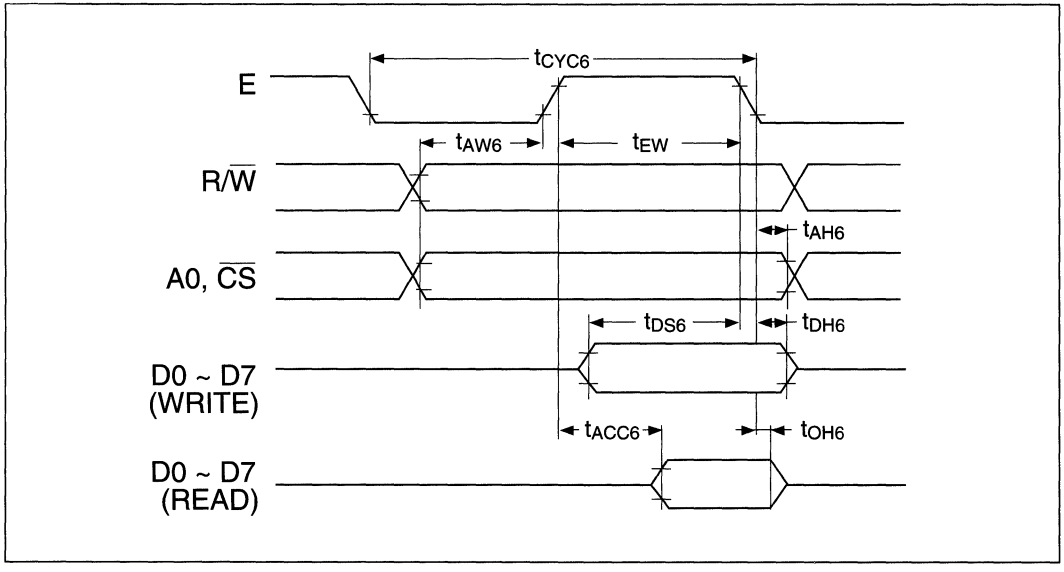
*6. The input timing of the FR delay time is determined by the SED1520 (Slave).
The output timing of the FR delay time is determined by the SED1520 (Master).

● **Timing Chart**

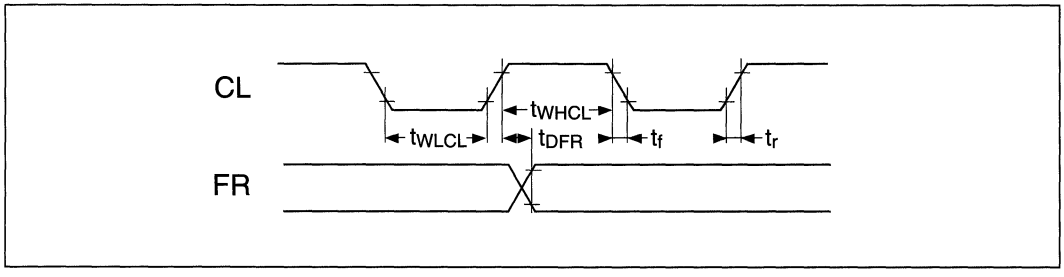
○ **Read/Write timing for the 80-port MPU**



○ **Read/Write timing for the 68-port MPU**



○ **Control timing for 80-port/68-port display**



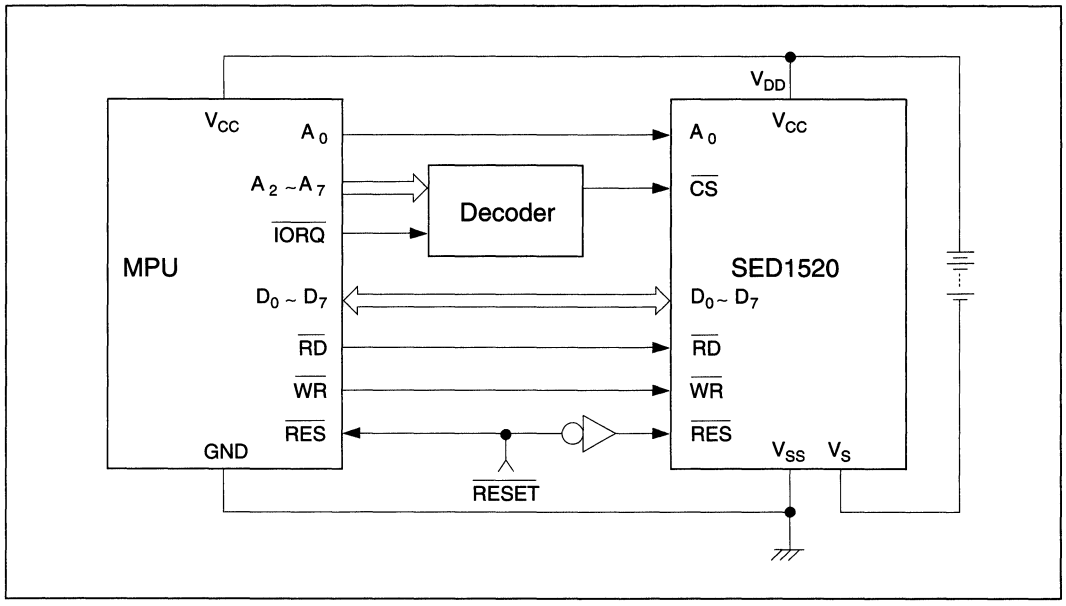
■ DISPLAY COMMANDS

(Based on the 80-port MPU; the $\overline{RD}$ and $\overline{WR}$ commands differ for the 68-port MPU.)

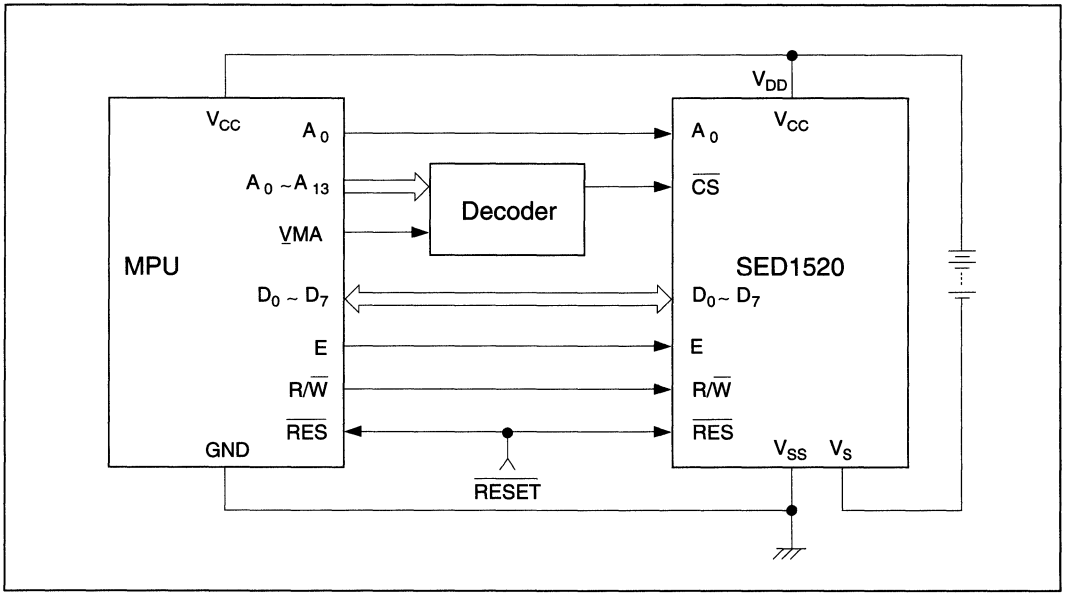
	Command	$\overline{RD}$ $\overline{WR}$ A0	D7	D6	D5	D4	D3	D2	D1	D0	Function
1	Display ON/OFF	1 0 0	1	0	1	0	1	1	1	0/1	Switches the entire display ON or OFF, regardless of the Display RAM's data or the internal status. *7
2	Display START Line	1 0 0	1	1	0	Display START address (0~31)					Determines the line of RAM data to be displayed at the display's top line (COM0).
3	Page Address Set	1 0 0	1	0	1	1	1	0	Page (0~3)		Sets the page of the Display RAM in the page address register.
4	Column (Segment) Address Set	1 0 0	0	Column address (0~79)							Sets the column address of the Display RAM in the column address register.
5	Status Read	0 1 0	BUSY	ACC	ON/OFF	RESET	0	0	0	0	Reads the status. BUSY 1: Busy (internal processing) 0: READY status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal
6	Write Display Data	1 0 1	Write Data								Writes the data on the data bus to RAM
7	Read Display Data	0 1 1	Read Data								Reads data from the Display RAM onto the data bus.
											These commands access a previously-specified address of the Display RAM, after which the column address is incremented by one.
8	ADC Select	1 0 0	1	0	1	0	0	0	0	0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse) output
9	Static Drive ON/OFF	1 0 0	1	0	1	0	0	1	0	0/1	Selects normal display operation or static all-lit drive display operation. 1: Static drive (Power Save) *7 0: Normal display operation
10	Duty Select	1 0 0	1	0	1	0	1	0	0	0/1	Selects the duty factor for driving LCD cells. 1: 1/32 duty 0: 1/16 duty
11	Read Modify Write	1 0 0	1	1	1	0	0	0	0	0	Increments the column address counter by one only when display data is written but not when it is read.
12	End	1 0 0	1	1	1	0	1	1	1	0	Cancels the Ready Modify Write mode.
13	Reset	1 0 0	1	1	1	0	0	0	1	0	Resets the Display START line to the 1st line in the register. Resets the column address counter to 0 and page address register to 3.

*7. Power Save mode is entered by selecting static drive in Display OFF status.

- **MPU INTERFACE (Reference)**
  - **(a) 80-family MPU**



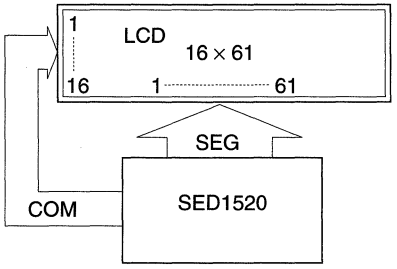
  - **(b) 68-family MPU**



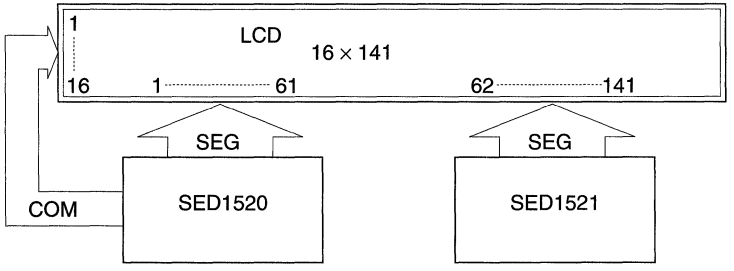
* The SED1520 (containing an oscillator) does not have pin $\overline{CS}$. The output ORed with $\overline{CS}$ must be applied to pins A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$).

● **Typical Connections With LCD Panel (Full dot LCD panel: 1 character = 6 × 8 dots)**

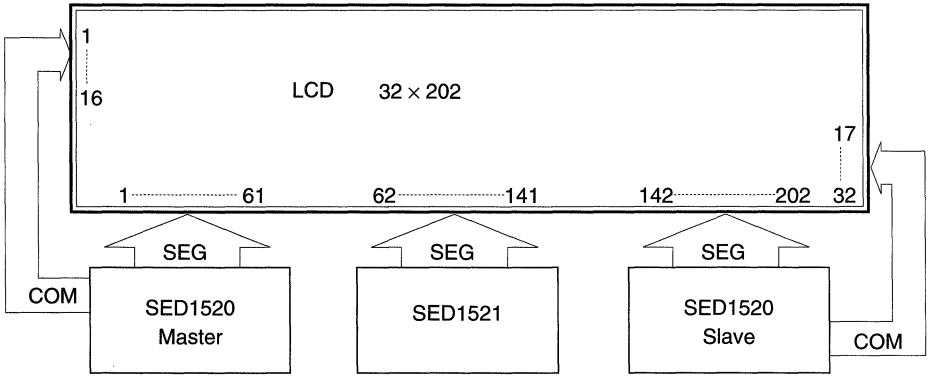
○ **(a) Duty 1/16, 10 characters × 2 lines**



○ **(b) Duty 1/16, 23 characters × 2 lines**



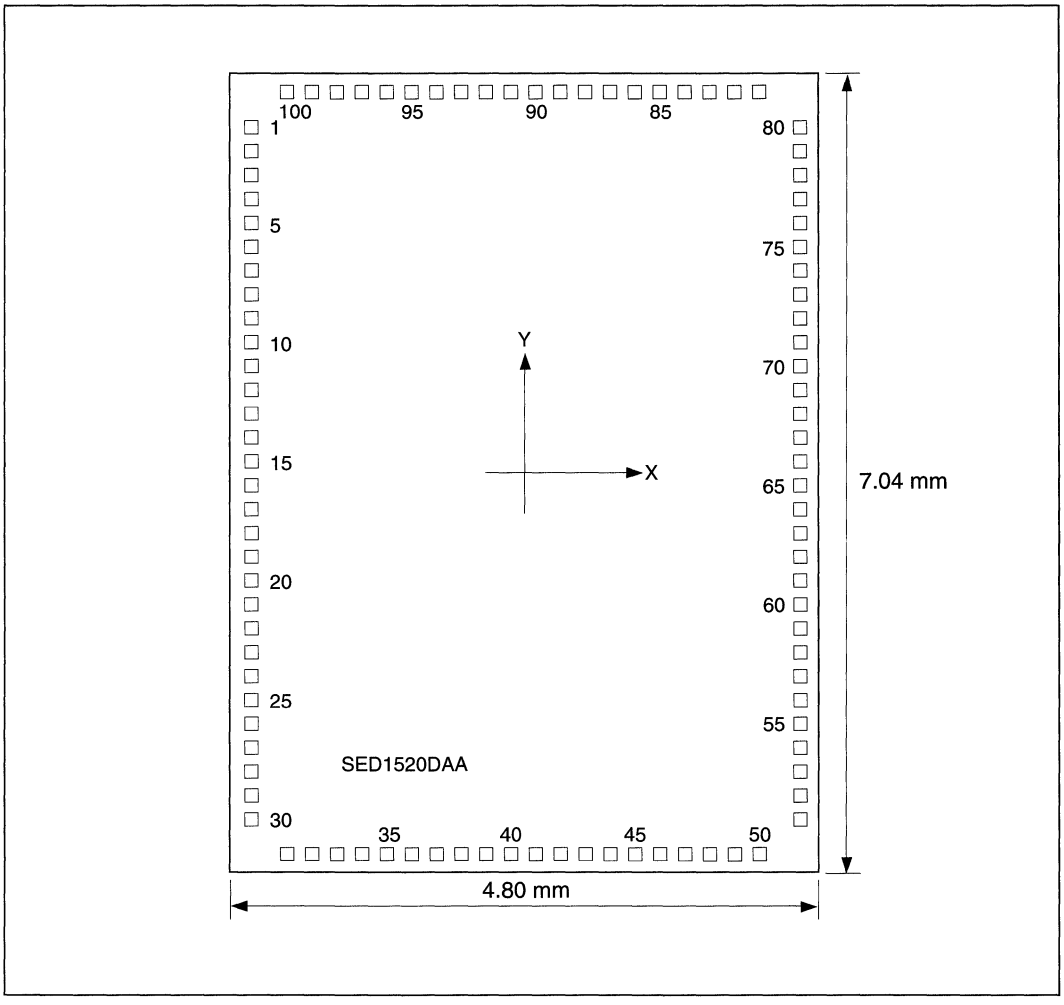
○ **(c) Duty 1/32, 33 characters × 4 lines**



* SED1521 may be omitted. If it is not used, the panel consists of 32 × 122 dots.

Note: Type AA (using external clock) and type 0A (containing an oscillator) cannot coexist for the same panel.

■ PAD LAYOUT (SED1520D/SED1521D)



● Al pad

Chip Specification	Dimensions (mm)
Chip size	7.04 × 4.80
Chip thickness	0.400 ± 0.025
Pad size	0.10 × 0.10

● Au bump pad

Chip Specification	Dimensions (mm)
Chip size	7.04 × 4.80
Chip thickness	0.525 ± 0.025
Pad size	0.132 × 0.111
Pad pitch	0.199 min
Bump height	0.020 +0.01 to –0.005

■ PAD COORDINATES (SED1520DAB)

Pad		X	Y
No.	Name		
1	COM5	159	6507
2	COM6	159	6308
3	COM7	159	6108
4	COM8	159	5909
5	COM9	159	5709
6	COM10	159	5510
7	COM11	159	5310
8	COM12	159	5111
9	COM13	159	4911
10	COM14	159	4712
11	COM15	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159

Pad		X	Y
No.	Name		
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	2696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948

Pad		X	Y
No.	Name		
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	$\overline{CS}$	4641	5247
75	CL	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{SS}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V5	2699	6884
91	V3	2300	6884
92	V2	2100	6884
93	M/S	1901	6884
94	V4	1701	6884
95	V1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	COM4	504	6884

CMOS DOT MATRIX LCD SEGMENT DRIVER

■ DESCRIPTION

The SED152A is the p-substrate version of the SED1521. It is used as an extension driver for the 8-bit or 16-bit MCUs.

Refer to the SED1521 section for more information.

■ FEATURES

- Direct display of data read from display data RAM
  RAM bit area "0" ..... LCD off
  "1" ..... LCD on
- Fast 8-bit MPU interface compatible with 80- and 68- family microcomputers
- On-chip LCD driving circuits .. 80 drive set (segment)
- Duty rations to choose from
  External input sync ..... 1/8 to 1/32
- Very low power dissipation 30μW at 2kHz external clock
- Supply voltages ..... V_{DD}-V_{SS}: 2.4V to 6.0V
  V_{C5}-V_{SS}: 3.5V to 6.0V
- A variety of command functions, including:
  Read/Write Display Data, Display ON/OFF, Set Address, Set Display Start Line, Set Column Address, Read Status, Static Drive ON/OFF, Select Duty, Read Modify Write, Select Segment, Driving Selection, Save Power, etc.

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■ DESCRIPTION

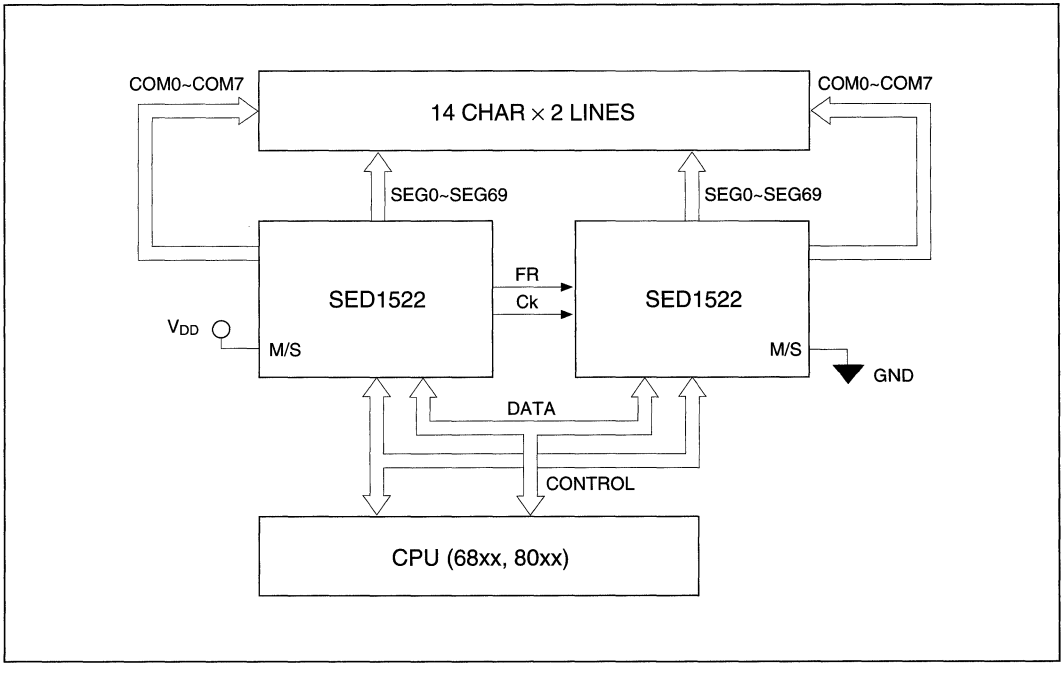
The SED1522 is a graphic LCD controller driver designed for use in a dot matrix LCD (Liquid Crystal Display) system capable of displaying characters and graphics. The bit-addressable display data which is sent from an 8-bit microcomputer is stored in a built-in display RAM which generates the signals required for driving the LCD. The circuitry has been designed to ensure low power consumption and a wide range of operating voltages, for use in high-performance handheld systems that run on batteries.

The SED1522 can use a single chip to drive an LCD of 13 characters by one line each plus an indicator. The SED1522 can be used in master-slave combination. Moreover, the SED1521 segment driver is available for expanding a system to enable 80-port output in order to construct mid-capacity displays using a minimal number of drivers.

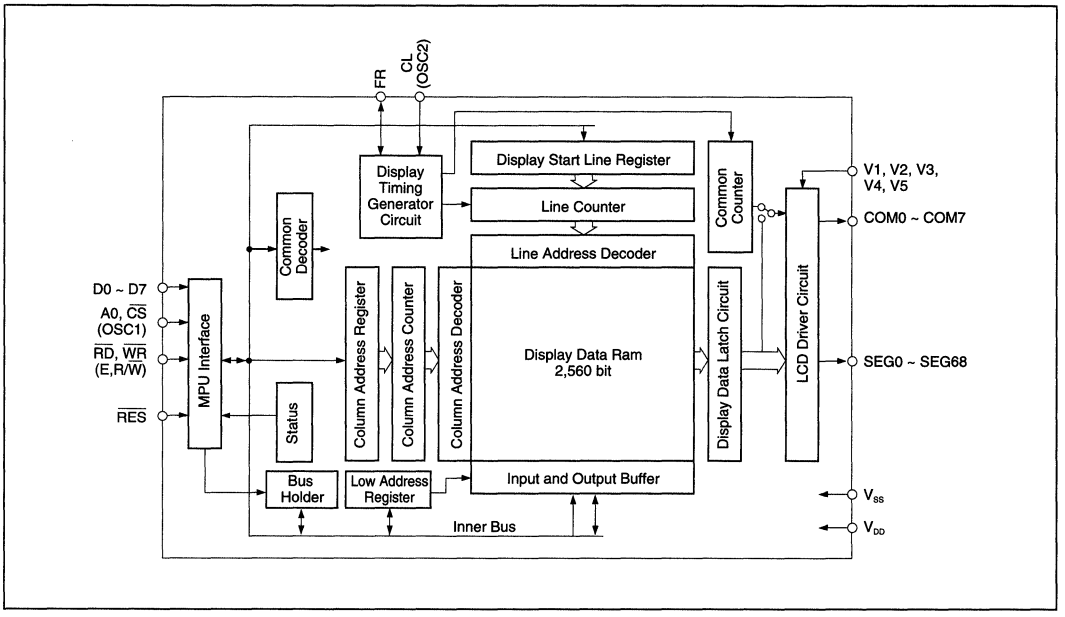
■ FEATURES

- Low-power CMOS technology 30μW
- Fast CPU 8-bit data interface (80xx, 68xx)
- 1/8 to 1/16 duty cycle
- Built-in LCD driver circuit ..... 69 segments
  8 commons
- Built-in display data RAM ..... 2560 bits
- Rich display command setting
- On-chip CR oscillation circuit
- Master/slave operation is supported
- LCD voltage ..... –3.5 to –13V
- Single power supply ..... 2.4 to 7.0V
- Package ..... QFP5-100 pin (FOA, FAA)
  QFP15-100 pin (FOC, FAC)
  Al pad (DOA, DAA)
  Au bump (DOB, DAB)

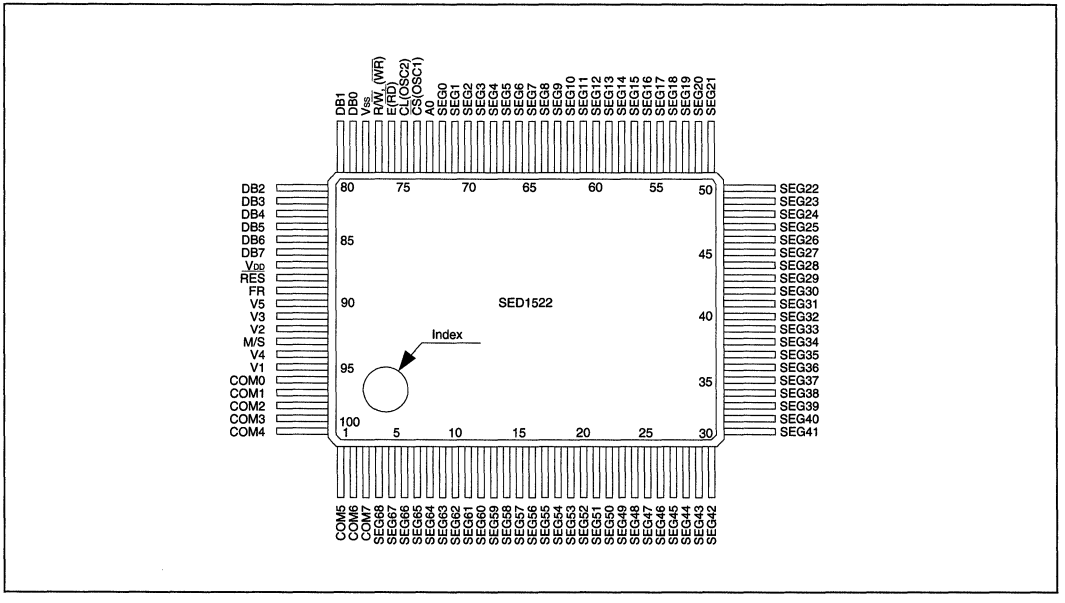
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



Model Name	Terminal No.	
	74	75
SED1522FOA	OSC1	OSC2
SED1522FAA	$\overline{CS}$	CL

* The Common output COM0 to COM7 of the Master LSI corresponds COM15 to COM8 on the Slave LSI.

■ PIN DESCRIPTION

Terminal Name	Function
DB0~DB7	Data input
A0	Selects display data or instructions. HIGH: Display data. LOW: Instructions.
$\overline{RES}$	Resets the system and selects the interface type for a 68-port/80-port MPU. HIGH: 68-port MPU interface. LOW: 80-port MPU interface.
$\overline{CS}$	Chip Select input. LOW: Active level sensing.
E ($\overline{RD}$)	Read/Write Enable signal when a 68-port MPU is connected. (Active-LOW Read Enable signal when an 80-port MPU is connected.)
R/$\overline{W}$ ($\overline{WR}$)	Read/Write Select signal when a 68-port MPU is connected. HIGH: Read Select LOW: Write Select (Active-LOW Write Enable input when an 80-port MPU is connected. Rising edge sensing.)
CL	External clock input (only effective with external clock types).
FR	LCD Frame (AC-conversion) signal input/output.
SEG0~SEG68	Segment output for driving the LCD.
COM0~COM7 (COM15~COM8)	Common output for driving the LCD.
M/S	Master/Slave Select signal.
V_{DD}	5V power supply.
V_{SS}	0V power supply (GND level).
V1, V2, V3, V4, V5	Power supplies for driving the LCD. $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

■ CLOCK OPTIONS

Model Name	Operating Clock		Connectable Drivers	Package
	Internal oscillator	External clock		
SED1522F$_{OA}$	18kHz	18kHz	SED1522F$_{OA}$, SED1521F$_{OA}$	QFP5-100pin
SED1522D$_{OA}$			SED1522D$_{OA}$, SED1521D$_{OA}$	AL pad chip
SED1522D$_{OB}$			SED1522D$_{OB}$, SED1521D$_{OB}$	Au Bump chip
SED1522F$_{AA}$	—	2kHz	SED1522F$_{AA}$, SED1521F$_{AA}$	QFP5-100pin
SED1522D$_{AA}$			SED1522D$_{AA}$, SED1521D$_{AA}$	AL pad chip
SED1522D$_{AB}$			SED1522D$_{AB}$, SED1521D$_{AB}$	Au Bump chip

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0V, $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$)

Parameter		Symbol	Ratings	Unit
Supply voltage (1)		V_{SS}	–8.0 to 0.3	V
Supply voltage (2)		V5	–16.5 to 0.3	V
Supply voltage (3)		V1, V2 V3, V4	V5 to 0.3	V
Input voltage		V_I	V_{SS}–0.3 to 0.3	V
Output voltage		V_O	V_{SS}–0.3 to 0.3	V
Permissable loss		P_D	250	mW
Operating temperature		T_{opr}	–30 to 85	°C
Storage temperature	FP	T_{stg}	–65 to 150	°C
	Die		–55 to 125	
Soldering temperature		T_{sol}	260°C for 10s (at the leads)	

● DC Characteristics

(V_{DD} = 0V, T_a = −20 to 75°C)

Parameter		Symbol	Condition	Applicable Terminals	Min	Typ	Max	Unit
Operating voltage (1)*1	Recommended operation	V_{SS}		V_{SS}	−5.5	−5.0	−4.5	V
	Potential operation				−7.0	—	−2.4	
Operating voltage (2)	Recommended operation	V5		V5	−13.0	—	−3.5	V
	Potential operation				−13.0	—	—	
	Potential operation	V1, V2		V1, V2	0.6×V5	—	V_{DD}	
	Potential operation	V3, V4		V3, V4	V5	—	0.4×V5	
HIGH input voltage		V_{IHT}		A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}+2.0	—	V_{DD}	V
		V_{IHC}		CL, FR, M/S, $\overline{RES}$	0.2×V_{SS}	—	V_{DD}	
		V_{IHT}	V_{SS}= −3V	A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$	0.2×V_{SS}	—	V_{DD}	V
		V_{IHC}	V_{SS}= −3V	CL, FR, M/S, $\overline{RES}$	0.2×V_{SS}	—	V_{DD}	
LOW input voltage		V_{ILT}		A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}	—	V_{SS}+0.8	V
		V_{ILC}		CL, FR, M/S, $\overline{RES}$	V_{SS}	—	0.8×V_{SS}	
		V_{ILT}	V_{SS}= −3V	A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}	—	0.85×V_{SS}	V
		V_{ILC}	V_{SS}= −3V	CL, FR, M/S, $\overline{RES}$	V_{SS}	—	0.8×V_{SS}	
HIGH output voltage		V_{OHT}	I_{OH}= −3mA	D0~D7	V_{SS}+2.4	—	—	V
		V_{OHC1}	I_{OH}= −2mA	FR	V_{SS}+2.4	—	—	
		V_{OHC2}	I_{OH}= −120μA	OSC2	0.2×V_{SS}	—	—	
		V_{OHT}	V_{SS}= −3V I_{OH}= −2mA	D0~D7	0.2×V_{SS}	—	—	V
		V_{OHC1}	V_{SS}= −3V I_{OH}= −2mA	FR	0.2×V_{SS}	—	—	
		V_{OHC2}	V_{SS}= −3V I_{OH}= −50μA	OSC2	0.2×V_{SS}	—	—	
LOW output voltage		V_{OLT}	I_{OL}=3mA	D0~D7	—	—	V_{SS}+0.4	V
		V_{OLC1}	I_{OL}=2mA	FR	—	—	V_{SS}+0.4	
		V_{OLC2}	I_{OL}=120μA	OSC2	—	—	0.8×V_{SS}	
		V_{OLT}	V_{SS}= −3V I_{OL}=2mA	D0~D7	—	—	0.8×V_{SS}	V
		V_{OLC1}	V_{SS}= −3V I_{OL}=2mA	FR	—	—	0.8×V_{SS}	
		V_{OLC2}	V_{SS}= −3V I_{OL}=50μA	OSC2	—	—	0.8×V_{SS}	
Input leak current		I_{LI}		A0,E,R/$\overline{W}$,$\overline{CS}$,CL,$\overline{RES}$,MS pins	−1.0	—	1.0	μA
Output leak current		I_{LO}	Applicable when FR is in a high-impedance state	D0~D7, FR pins	−3.0	—	3.0	
LCD driver ON resistance		R_{ON}	T_a=25°C V5= −5.0V	SEG0~68	—	5.0	7.5	kΩ
			T_a=25°C V5= −3.5V	COM0~7	—	10.0	50.0	
Static current consumption		I_{DDQ}	$\overline{CS}$=CL=V_{DD}	V_{DD}	—	0.05	1.0	
Active current consumption	External CLK	$I_{DD(1)}$	During display f_{CL}=2kHz V5= −5V R_f=1MΩ	V_{DD}	—	2.0	5.0	μA
	Oscillator				—	9.5	15.0	
	External CLK		During display f_{CL}=2kHz V5= −5V,V_{SS}= −3V R_f=1MΩ	V_{DD}	—	1.5	4.5	μA
	Oscillator				—	6.0	12.0	
		$I_{DD(2)}$	During access t_{cyc}=200kHz V_{SS}= −3V, During access t_{cyc}=200kHz		—	300	500	μA
					—	150	300	
Input terminal capacity		C_{IN}	T_a=25°C, f=1MHz	All input terminals	—	5.0	8.0	pF
Oscillating frequency		f_{OSC}	R_f=1.0MΩ±2%, V_{SS}= −5.0V		15	18	21	kHz
			R_f=1.0MΩ±2%, V_{SS}= −3.0V		11	16	21	
Reset time		t_R		$\overline{RES}$	1.0	—	1000	μs

*1. A wide range of operating voltages is guaranteed, except in case of abrupt voltage fluctuations during MPU access.

● AC Characteristics

○ Read/Write timing for the 80-port MPU

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

Parameter	Signal	Symbol	Condition	Min	Typ	Max	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		10	—	—	ns
Address set-up time		t_{AW8}		20	—	—	ns
System cycle time	$\overline{WR}$, $\overline{RD}$	t_{CYC8}		1000	—	—	ns
Control pulse width		t_{CC}		200	—	—	ns
Data set-up time	D0~D7	t_{DS8}		80	—	—	ns
Data hold time		t_{DH8}		10	—	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	—	90	ns
Output disable time		t_{OH8}		10	—	60	ns

*2. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

*3. The rise or fall time of input signals should be less than 15ns.

○ Read/Write timing for the 68-port MPU

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

Parameter		Signal	Symbol	Condition	Min	Typ	Max	Unit
System cycle time		A0, $\overline{CS}$ R/$\overline{W}$	t_{CYC6} *4		1000	—	—	ns
Address set-up time			t_{AW6}		20	—	—	ns
Address hold time			t_{AH6}		10	—	—	ns
Data set-up time		D0~D7	t_{DS6}		80	—	—	ns
Data hold time			t_{DH6}		10	—	—	ns
Output disable time			t_{OH6}	C_L=100pF	10	—	60	ns
Access time			t_{ACC6}		—	—	90	ns
Enable pulse width	READ	E	t_{EW}		100	—	—	ns
	WRITE				80	—	—	ns

*4 t_{CYC6} indicates the cycle during which $\overline{CS}$/E are HIGH; it does not indicate the cycle of the E signal.

*5 The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

*6 The rise or fall time of input signals should be less than 15ns.

○ Control timing for 80-port/68-port display

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

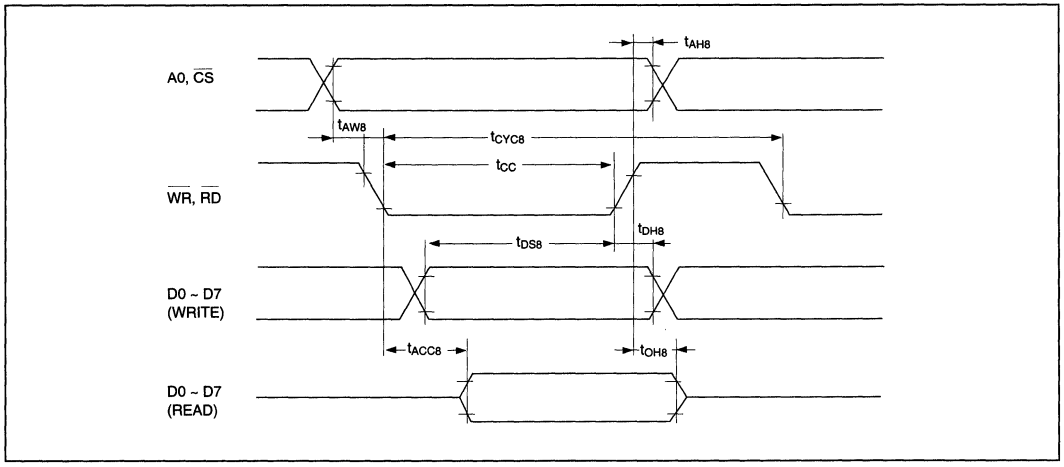
Parameter	Signal	Symbol	Condition	Min	Typ	Max	Unit
LOW pulse width	C_L	t_{WLCL}	(Input timing)	35	—	—	µs
HIGH pulse width		t_{WHCL}		35	—	—	µs
Rising time		t_r		—	30	150	ns
Falling time		t_f		—	30	150	ns
FR delay time	FR	t_{DFR}	(Input timing)	–2.0	0.2	2.0	µs
			(Output timing), C_L=100pF	—	0.2	0.4	µs

*7. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

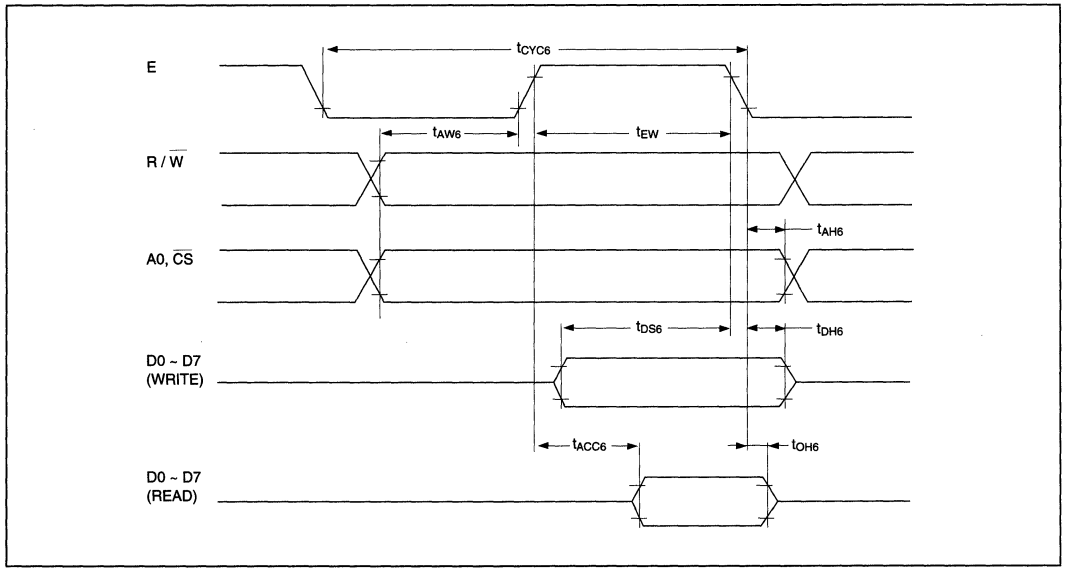
*8. The input timing of the FR delay time is determined by the SED1522 (Slave).
The output timing of the FR delay time is determined by the SED1522 (Master).

● Timing Chart

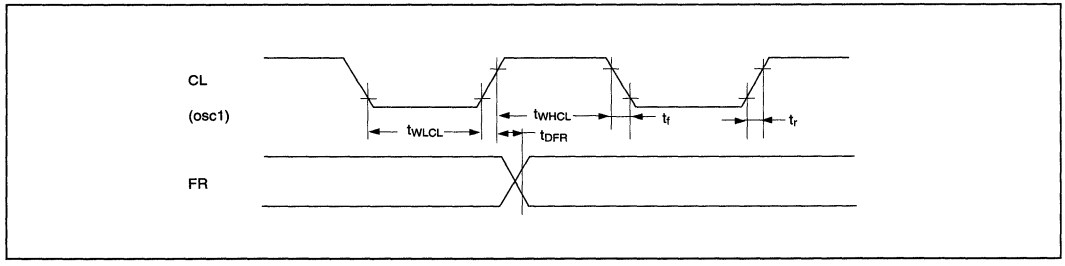
○ Read/Write timing for the 80-port MPU



○ Read/Write timing for the 68-port MPU



○ Control timing for 80-port/68-port display



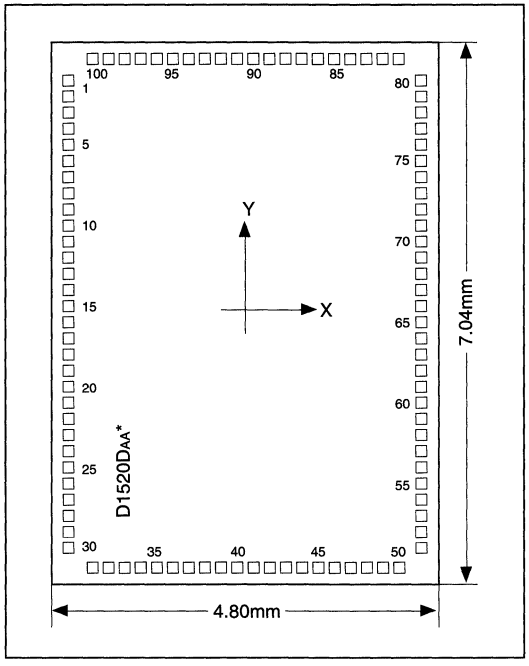
■ DISPLAY COMMANDS

(Based on the 80-port MPU; the $\overline{RD}$ and $\overline{WR}$ commands differ for the 68-port MPU)

	Command	$\overline{RD}$	$\overline{WR}$	A0	D7	D6	D5	D4	D3	D2	D1	D0	Function
1	Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	Switches the entire display ON or OFF, regardless of the Display RAM's data or the internal status.
2	Display START Line	1	0	0	1	1	0	Display START address (0~31)					Determines the line of RAM data to be displayed at the display's top line (COM0).
3	Page Address Set	1	0	0	1	0	1	1	1	0	Page (0~3)		Sets the page of the Display RAM in the page address register.
4	Column (Segment) Address Set	1	0	0	0	Column address (0~79)							Sets the column address of the Display RAM in the column address register.
5	Status Read	0	1	0	BUSY	ACC	ON/OFF	RESET	0	0	0	0	Reads the status. BUSY 1: Busy (internal processing) 0: READY status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal
6	Write Display Data	1	0	1	Write Data								Writes the data on the data bus to RAM
7	Read Display Data	0	1	1	Read Data								Reads data from the Display RAM onto the data bus.
													These commands access a previously-specified address of the Display RAM, after which the column address is incremented by one.
8	ADC Select	1	0	0	1	0	1	0	0	0	0	0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse) output
9	Static Drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Selects normal display operation or static all-lit drive display operation. 1: Static drive (Power Save) *9 0: Normal display operation
10	Duty Select	1	0	0	1	0	1	0	1	0	0	0/1	Selects the duty factor for driving LCD cells. 1: 1/16 duty 0: 1/8 duty
11	Read Modify Write	1	0	0	1	1	1	0	0	0	0	0	Increments the column address counter by one only when display data is written but not when it is read.
12	End	1	0	0	1	1	1	0	1	1	1	0	Cancels the Ready Modify Write mode.
13	Reset	1	0	0	1	1	1	0	0	0	1	0	Resets the Display START line to the 1st line in the register. Resets the column address counter to 0 and sets page address register to 3.

*9. Power Save mode is entered by selecting static drive in Display OFF status.

■ PAD LAYOUT



○ Aluminum pad chip specifications

Chip dimensions:	4.80 × 7.04 × 0.40mm
Pad surface area:	100 × 100μm

○ Gold bump chip specifications (reference only)

Minimum bump pitch:	199μm
Bump height:	20^{+10}_{-5} μm
Bump size:	132 × 111 μm (±20 μm)
Chip dimensions:	4.80 × 7.04 × 0.525mm

* The die shown is the SED1522DAA. The final A in the suffix indicates that the device is an aluminum pad product. Bump chip products share the same die part number as aluminum products; however, the last letter of the suffix is B.

■ PAD COORDINATES

Pin names are for the SED1522DAA/SED1522DAB, and those in brackets for the SED1522DOA/SED1522DOB.

Pad No.	Pin Name	X	Y
1	COM5	159	6507
2	COM6	159	6308
3	COM7	159	6108
4	SEG68	159	5909
5	SEG67	159	5709
6	SEG66	159	5510
7	SEG65	159	5310
8	SEG64	159	5111
9	SEG63	159	4911
10	SEG62	159	4712
11	SEG61	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159

Pad No.	Pin Name	X	Y
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	$\overline{CS}$ (OSC1)	4641	5247
75	CL (OSC2)	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/$\overline{W}$ ($\overline{WR}$)	4641	5846
78	V_{SS}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V5	2499	6884
91	V3	2300	6884
92	V2	2100	6884
93	M/S	1901	6884
94	V4	1701	6884
95	V1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	COM4	504	6884

Note: Values in the properties table are specified as Max or Min according to the comparison on the numerical coordinates.

All specifications of this device are subject to change without notice.

SED1526 Series

DOT MATRIX LCD DRIVER-CONTROLLER

■ DESCRIPTION

The SED1526 Series are intelligent CMOS LCD controller-drivers with the ability to drive alphanumeric and graphic displays. The LSI communicates with a high-speed microprocessor, such as the Intel 80xx and 68xx family, through either a serial or 8-bit parallel interface. It stores the data sent from the microprocessor in the built-in display data RAM (80 × 33 bits) and generates an LCD drive signal.

These devices incorporate an internal DC/DC converter to generate the negative voltage needed for the LCD contrast. The controller features software contrast adjusted by command setting.

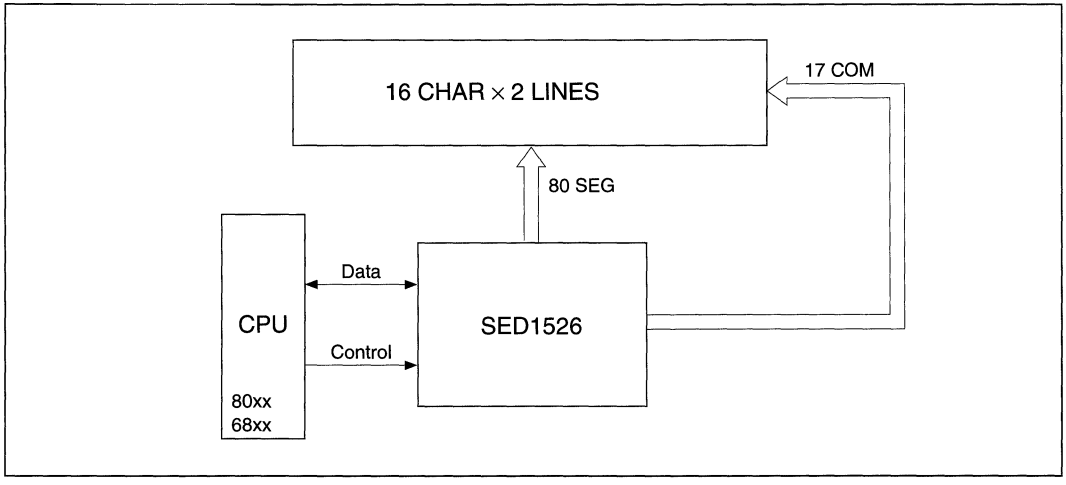
■ FEATURES

- Low-power CMOS technology
- Direct interface to both 80xx and 68xx MPU
- Support 8-bit parallel and serial interface
- On-chip display data RAM ..... 80 × 33 bits
- On-chip DC/DC converter for LCD voltage
- On-chip CR oscillator circuit
- Supports master/slave mode
- Voltage regulator, low-power voltage follower
- –.17%/°C temperature gradient
- 32-level contrast adjustment by software
- 2.4V to 6.0V supply voltage
- –4.0V to –12V LCD voltage
- Operating temperature ..... –40 to 85°C
- Low power consumption 100μA
- Package
  - QFP-5 ..... 128-pin (F0A)
  - Al pad Die D0A
  - Au bump Die D0B
  - TAB T0A

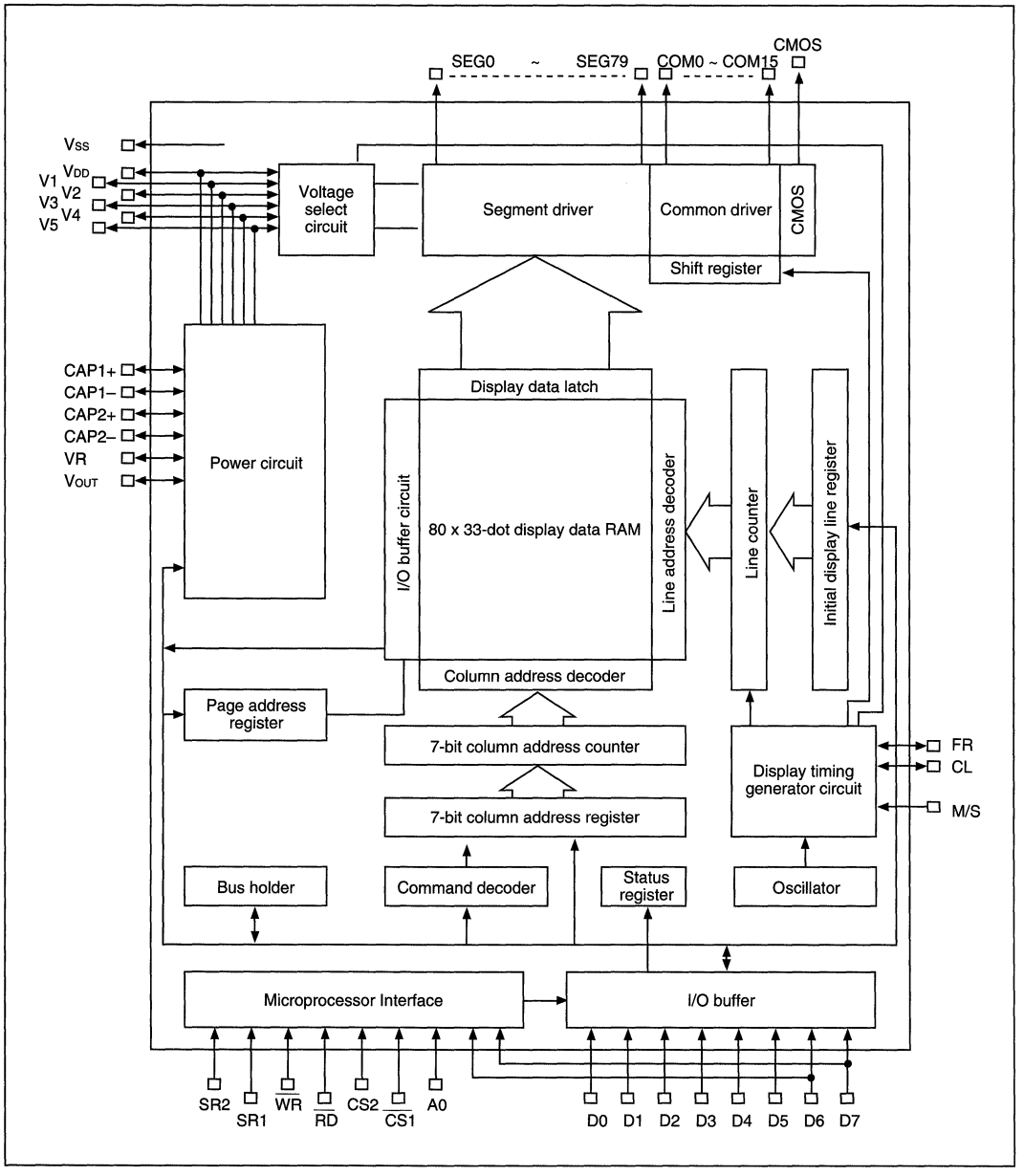
Available models

Models	Duty Cycle	LCD Bias	SEG Driver	COM Driver	Display Area
SED1526	1/8, 1/9, 1/16, 1/17	1/5	80	17	80 × 17
SED1527	1/16, 1/17, 1/32, 1/33	1/7	80	17	160 × 33
SED1528	1/32, 1/33	1/7	64	33	64 × 33

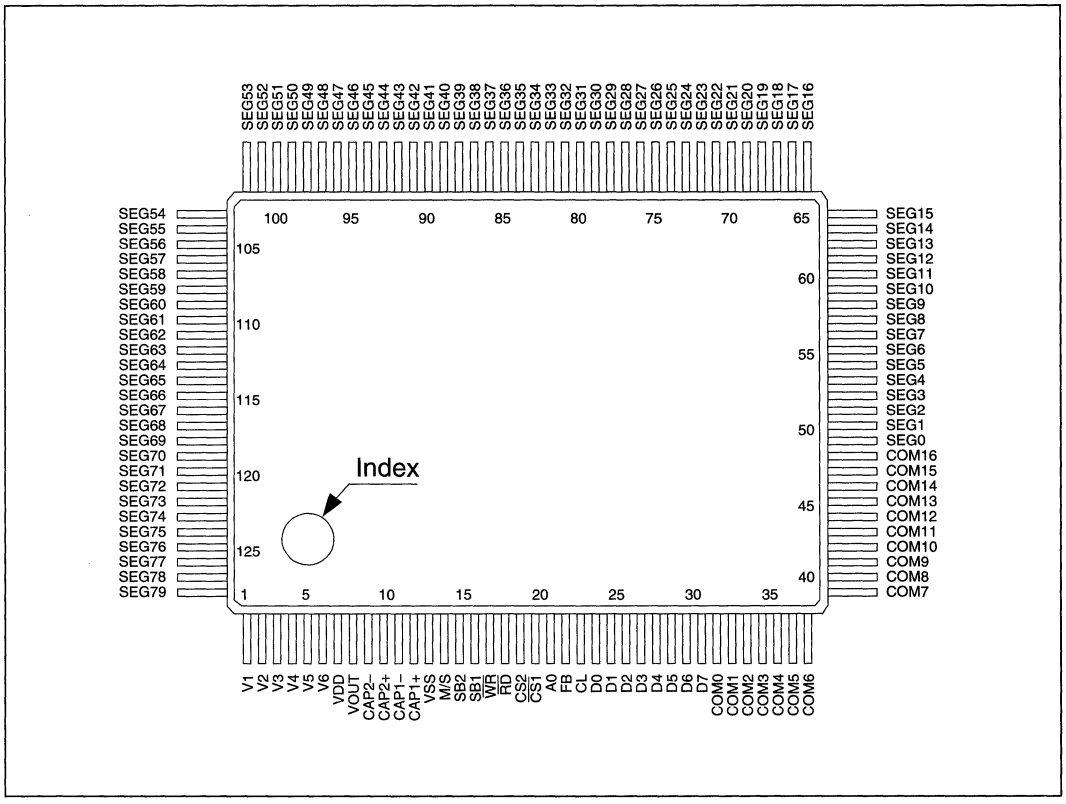
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ SED1526 AND SED1527 PIN ASSIGNMENT



■ PIN DESCRIPTION

● Power Supply

Pin	I/O	Function	Number of Pins
V_{DD}	Supply	+5V power supply. Common to microprocessor power supply V_{CC} pin	1
V_{SS}	Supply	Ground	1
V1 ~ V5	Supply	LCD driver supply voltages. The Set Power Control command can switch the master (internal) and external power supply modes of these pins. When external mode selects, the voltage determined by the LCD cell is impedance-converted through a resistive divider or an operational amplifier depending on application. Voltages should meet the following requirement: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ When master mode selects, these voltages are generated on the chip:	5

	SED1526	SED1527	SED1528
V1	1/5 V5	1/7 V5	1/7 V5
V2	2/5 V5	2/7 V5	2/7 V5
V3	3/5 V5	5/7 V5	5/7 V5
V4	4/5 V5	6/7 V5	6/7 V5

● LCD Driver Supplies

Pin	I/O	Function	Number of Pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1–	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2–	O	DC/DC voltage converter capacitor 2 negative connection	1
V_{OUT}	O	DC/DC voltage converter output	1
V_R	I	Voltage adjustment pin. Applies voltage between V_{DD} and V5 using a resistive divider.	1

● **Microprocessor Interface**

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Number of Pins</th></tr>
<tr><td>D0 ~ D7
(SI)
(SCL)</td><td>I/O</td><td>Data input/outputs. The 8-bit bidirectional data buses to be connected to the standard 4/8-bit microprocessor data buses. When the serial interface is selected, D7 is serial data input (SI) and D6 is serial clock input (SCL).</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Control/display data flag is input. It is connected to the LSB of microprocessor address bus. When low, the data on D0 to D7 is control data. When high, the data on D0 to D7 is display data</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>Chip select input. Data input/output is enabled when $\overline{CS1}$ is low and CS2 is high.</td><td>2</td></tr>
<tr><td>$\overline{RD}$ (E)</td><td>I</td><td>• Read enable input. When interfacing to an 8080-Series microprocessor and when $\overline{RD}$ is low, the SED1526 Series data bus output is enabled.
• When interfacing to a 6800-Series microprocessor and when R/W Enable E is high, R/$\overline{W}$ input is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$ (R/$\overline{W}$)</td><td></td><td>• Write enable input. When interfacing to an 8080-Series microprocessor, $\overline{WR}$ is active low.
• When interfacing to a 6800-Series microprocessor, it will be in read mode when R/$\overline{W}$ is high and it will be in write mode when R/$\overline{W}$ is low.
R/$\overline{W}$ = “1” : Read
R/$\overline{W}$ = “0” : Write</td><td>1</td></tr>
<tr><td>SR1, SR2</td><td>I</td><td>Microprocessor interface select, and parallel/serial data input select.
<table>
<tr><th>SR1</th><th>SR2</th><th>Type</th></tr>
<tr><td>0</td><td>1</td><td>8080 microprocessor bus (parallel input)</td></tr>
<tr><td>1</td><td>1</td><td>6800 microprocessor bus (parallel input)</td></tr>
<tr><td>1</td><td>0</td><td>Serial input</td></tr>
<tr><td>0</td><td>0</td><td>Reset</td></tr>
</table>
* In serial mode, no data can be read from RAM and D0 to D5 are HZ. $\overline{RD}$ and $\overline{WR}$ must be high or low.</td><td>2</td></tr>
</table>

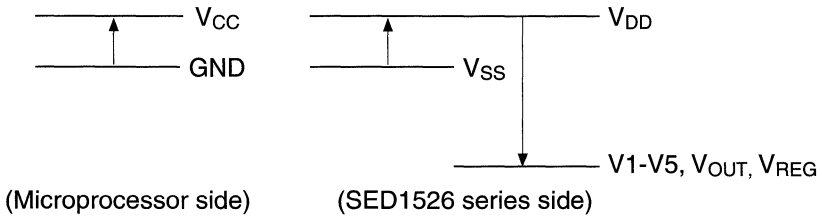
- **LCD Driver Outputs**

<table>
<tr><th>Pin</th><th>I/O</th><th>Functions</th><th>Number of Pins</th></tr>
<tr><td>M/S</td><td>I</td><td>SED1526 Series master/slave mode select input. Master mode selects when FR and CL are high, and slave mode selects when FR and CL are low. It will be master mode when M/S is high and it will be slave mode when M/S is low.
<table>
<tr><th>Model</th><th>Mode</th><th>OSC Circuit</th><th>FR</th></tr>
<tr><td rowspan="2">SED1526
SED1527
SED1528</td><td>Master</td><td>Valid</td><td>Output</td></tr>
<tr><td>Slave</td><td>Invalid</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Clock input/ouput when SED1526 Series selects master or slave mode. The Clock Stop command can disable CL output when SED1526 Series is in master mode. It will be in ouput mode when M/S is high and it will be in input mode when M/S is low.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD AC signal input/output. When SED1526 Series selects master mode, it must connect to LCD common driver FR pin. It will be output mode when M/S is high and it will be input mode when M/S is low.</td><td>1</td></tr>
<tr><td>SEGn</td><td>O</td><td>LCD segment driver output. The display RAM and FR signal select the segment driver output source.
<table>
<tr><th>RAM Data</th><th>FR Signal</th><th>Segment Driver-n Output</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td>V_{DD}</td></tr>
<tr><td>0</td><td>V5</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>V2</td></tr>
<tr><td>0</td><td>V3</td></tr>
</table></td><td>80 (SED1526/ 1527) or 64 (SED1528)</td></tr>
<tr><td>COMn</td><td>O</td><td>LCD common driver output. The IC internal scan signal and FR signal select the common driver output source. The common scan sequence is reversed in slave mode.
<table>
<tr><th>Internal Scan Signal</th><th>FR Signal</th><th>Common Driver-n Output</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td>V5</td></tr>
<tr><td>0</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>V1</td></tr>
<tr><td>0</td><td>V4</td></tr>
</table></td><td>80 (SED1526/ 1527) or 32 (SED1528)</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator COM output. COMS pin is equivalent to following COM output pin when DUTY+1 command is running:
<table>
<tr><th></th><th colspan="2">SED1526</th><th colspan="2">SED1527</th><th>SED1528</th></tr>
<tr><th></th><th>1/9 duty</th><th>1/17 duty</th><th>1/17 duty</th><th>1/33 duty</th><th>1/33 duty</th></tr>
<tr><td>Indicator COMS output</td><td>COM8</td><td>COM16</td><td>COM16</td><td>COM16 of slave chip</td><td>COM32</td></tr>
</table></td><td>1</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter		Symbol	Condition	Unit
Supply voltage range		V_{DD}	–0.3 to +7.0	V
	Triple voltage conversion	V_{DD}	–0.3 to +6.0	
Driver supply voltage range (1)		V5	–18.0 to +0.3	V
Driver supply voltage range (2)		V1, V2, V3, V4	V5 to +0.3	V
Input voltage range		V_{IH}	–0.3 to V_{DD} +0.3	V
Output voltage range		V0	–0.3 to V_{DD} + 0.3	V
Allowable loss		P_D	250	mW
Operating temperature range		T_{OPR}	–40 to +85	°C
Storage temperature	Flat package	T_{STG}	–65 to +150	°C
	Bear chip		–55 to +125	
Soldering temperature and time		T_{SOLDER}	260 • 10 (at leads)	°C • sec



Notes:

1. V1 to V5, V_{OUT}, and V_{REG} voltages are based on V_{DD} = 0V.
2. Voltages VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 must always be satisfied.
3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during normal operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.
4. The moisture resistance of the flat package may drop during soldering. Take care not to excessively heat the package resin during chip mounting.

● DC Characteristics

V_{DD} = 5V ±10%, V_{SS} = 0V, T_a = –40 to 85°C unless otherwise noted

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Pin
Power voltage (1)	Operational	V_{DD}		2.4	—	6.0	V	V_{DD} *1
Operating voltage (2)	Operational	V5		–V_{SS} × 3	—	–3.5	V	V5 *2
	Operational	V1, V2		0.6 × V5	—	V_{DD}	V	V1, V2
	Operational	V3, V4		V5	—	0.4 × V5	V	V3, V4
CMOS	High-level input voltage	V_{IHC}		0.7 × V_{DD}	—	V_{DD}	V	*3
			V_{DD} = 2.7V	0.8 × V_{DD}	—	V_{DD}		
	Low-level input voltage	V_{ILC}		V_{SS}	—	0.3 × V_{DD}	V	*3
			V_{DD} = 2.7V	V_{SS}	—	0.2 × V_{DD}		
	High-level output voltage	V_{OHC}	I_{OH} = –1mA	0.8 × V_{DD}	—	V_{DD}	V	*4
			V_{DD} = 2.7V I_{OH} = –0.5mA	0.8 × V_{DD}	—	V_{DD}		
	Low-level output voltage	V_{OLC}	I_{OH} = 1mA	V_{SS}	—	0.2 × V_{DD}	V	*4
			V_{DD} = 2.7V I_{OL} = 0.5mA	V_{SS}	—	0.2 × V_{DD}		
SCHMITT	High-level input voltage	V_{IHS}		0.4 × V_{DD}	—	0.8 × V_{DD}	V	*5
			V_{DD} = 2.7V	0.4 × V_{DD}	—	0.8 × V_{DD}		
	Low-level input voltage	V_{ILS}		0.2 × V_{DD}	—	0.6 × V_{DD}	V	*5
			V_{DD} = 2.7V	0.2 × V_{DD}	—	0.6 × V_{DD}		
	Schmitt voltage	V_H		0.2 × V_{DD}	—	—	V	*5
			V_{DD} = 2.7V	0.2 × V_{DD}	—	—		
Input leakage current		I_{LI}		–1.0	—	1.0	µA	*6
Output leakage current		I_{LO}		–3.0	—	3.0	µA	*7
LCD driver ON resistance		R_{ON}	T_a = 25°C V5 = –0.5V	—	5.0	7.5	kΩ	SEG0~79 COS0~15 COMS
			V5 = –3.5V	—	10.0	50.0		
Static current consumption		I_{DDQ}	$\overline{CS}$ = CL = V_{DD}	—	0.05	3.0	µA	V_{DD}
Input pin capacity		C_{IN}	T_a = 25°C, f = 1MHz	—	5.0	8.0	pF	Input pins
Built-in Power Circuit	Input voltage	V_{DD}		2.4	—	6.0	V	
	Booster output voltage	V_{OUT}	Triple voltage conversion	–16.5	—	—	V	V_{OUT}
	Voltage regulator operation voltage	V_{OUT}		–16.5	—	–4.0	V	V_{OUT}
	Voltage follower operation voltage	V5 (1)	Applied to SED1526	–12.0	—	–4.0	V	
		V5 (2)	Applied to SED1527	–16.0	—	(TBD)	V	
		V5 (3)	Applied to SED1528	–16.0	—	(TBD)	V	
	Reference voltage	V_{REG}	T_a = 25°C	–2.0	–3.1	–4.0	V	

*1. Although the wide range of operating voltage is guaranteed, a spike voltage change may have an effect on the voltage assurance during access to the microprocessor.

*2. VDD and V5 operating voltage range. The operating voltage range applies if an external power supply is used.

*3. Pins D0 to D5, A0, $\overline{CS1}$, CS2, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), M/S, CL and FR.

*4. Pins D0 to D7, FR and CL.

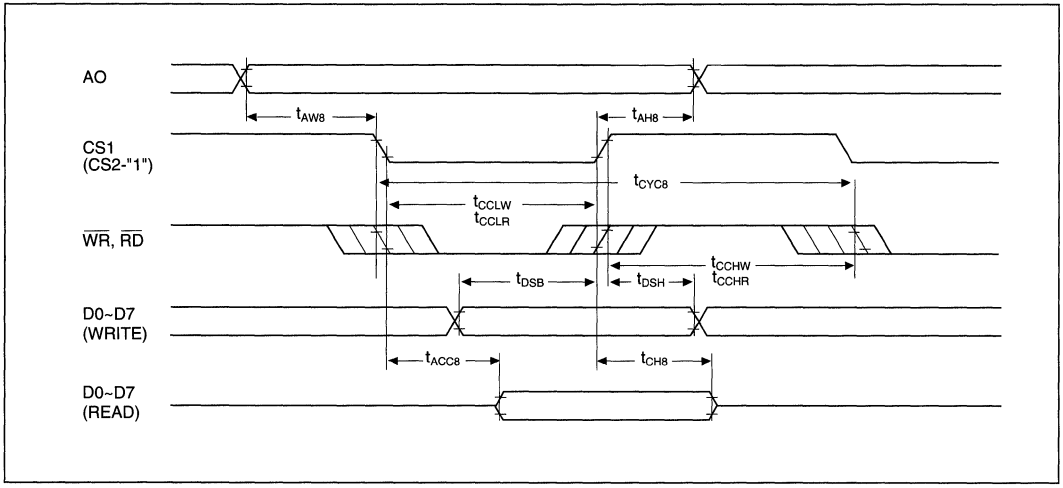
*5. Pins SI (D7), SCL (D5), SR1 and SR2.

*6. Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, M/S, SR1 and SR2.

*7. Applied if pins D0 to D7, FR and CL are high impedance.

- **Timing Characteristics**
  - **System Buses**

Read/write characteristics I (8080-Series microprocessor)



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = −40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	t_{AH8}		5	—	ns
Address setup time		t_{AW8}		5	—	ns
System cycle time		t_{CYC8}		250	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		75	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		75	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		145	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		145	—	ns
Data setup time		t_{DS5}		80	—	ns
Data hold time		t_{OH8}		10	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	80	ns
Output disable time		t_{CH8}		10	60	ns

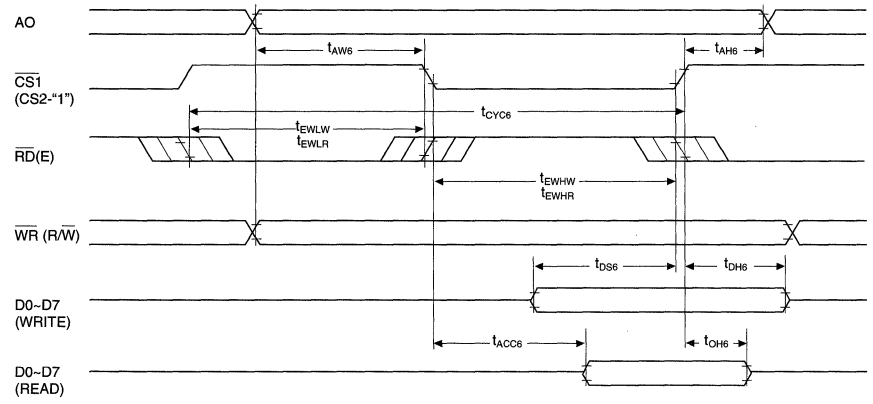
V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = −40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	t_{AH8}		10	—	ns
Address setup time		t_{AW8}		10	—	ns
System cycle time		t_{CYC8}		500	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		185	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		185	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		285	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		285	—	ns
Data setup time		t_{DS5}		160	—	ns
Data hold time		t_{OH8}		20	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	180	ns
Output disable time		t_{CH8}		20	120	ns

Notes:
1. t_{CCLW} and t_{CCLR} are limited depending on the overlap time of $\overline{CS1}$ low (CS2 high) and $\overline{WR}$ or $\overline{RD}$ low.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

○ **System Buses**

Read/write characteristics II (6800-Series microprocessor)



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to +85°C

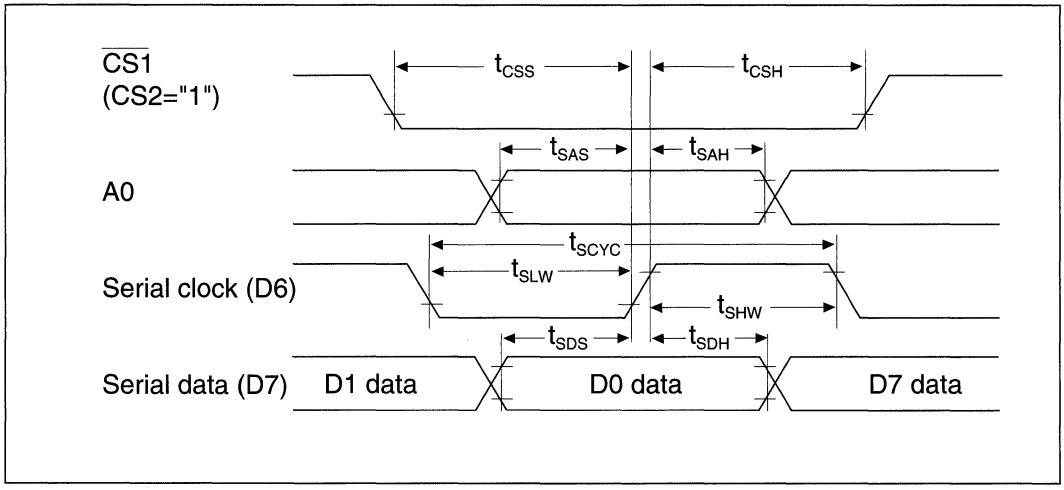
Parameter		Signal	Symbol	Conditions	Min	Max	Unit
System cycle time		A0	t_{CYC6}		250	—	ns
Address setup time		WR (R/W)	t_{AW6}		20	—	ns
Address hold time			t_{AH6}		10	—	ns
Data setup time		D0 ~ D7	t_{DS6}		80	—	ns
Data hold time			t_{DH6}		10	—	ns
Output disable time			t_{OH6}	CL = 100pF	10	60	ns
Access time			t_{ACC6}		—	90	ns
Enable low pulse width	Read	RD (E)	t_{EWLR}		85	—	ns
	Write		t_{EWLW}		75	—	ns
Enable high pulse width	Read	RD (E)	t_{EWHR}		135	—	ns
	Write		t_{EWHW}		145	—	ns

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to +85°C

Parameter		Signal	Symbol	Conditions	Min	Max	Unit
System cycle time		A0	t_{CYC6}		500	—	ns
Address setup time		WR (R/W)	t_{AW6}		40	—	ns
Address hold time			t_{AH6}		20	—	ns
Data setup time		D0 ~ D7	t_{DS6}		160	—	ns
Data hold time			t_{DH6}		20	—	ns
Output disable time			t_{OH6}	CL = 100pF	20	120	ns
Access time			t_{ACC6}		—	180	ns
Enable low pulse width	Read	RD (E)	t_{EWLR}		185	—	ns
	Write		t_{EWLW}		145	—	ns
Enable high pulse width	Read	RD (E)	t_{EWHR}		285	—	ns
	Write		t_{EWHW}		325	—	ns

Notes: 1. t_{EWHR} and t_{EWHW} are limited depending on the overlap time of $\overline{CS1}$ low (CS2 high) and $\overline{RD}$ (E) high.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

○ **Serial Interface**



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to +85°C

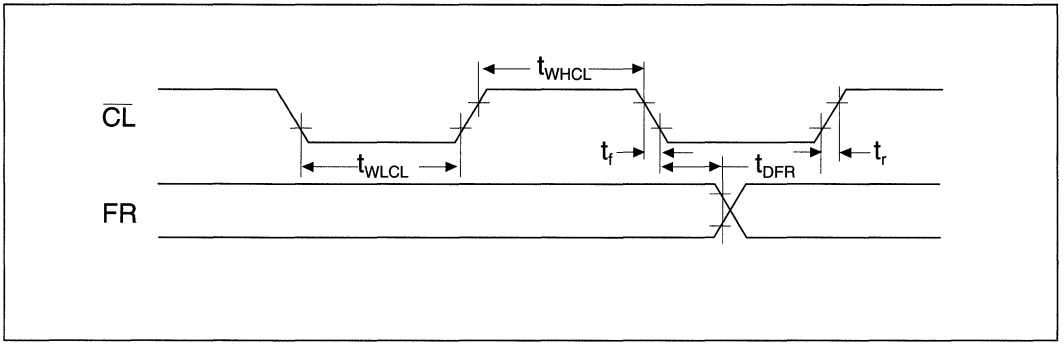
Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock cycle	Serial clock	t_{SCYC}		500	—	ns
Serial clock H pulse width		t_{SHW}		150	—	ns
Serial clock L pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		120	—	ns
Address hold time		t_{SAH}		200	—	ns
Data setup time	Serial data	t_{SDS}		120	—	ns
Data hold time		t_{SDH}		50	—	ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2 = "1")	t_{CSS}		30	—	ns
		t_{CSH}		400	—	ns

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock cycle	Serial clock	t_{SCYC}		1000	—	ns
Serial clock H pulse width		t_{SHW}		300	—	ns
Serial clock L pulse width		t_{SLW}		300	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		400	—	ns
Data setup time	Serial data	t_{SDS}		250	—	ns
Data hold time		t_{SDH}		100	—	ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2 = "1")	t_{CSS}		60	—	ns
		t_{CSH}		800	—	ns

Notes: 1. The input signal rise and fall times must be within 15 nanoseconds.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

○ **Display Control Timing**



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Low-level pulse width	CL	t_{WLCL}	(TBD)	(TBD)	—	—	µs
High-level pulse width		t_{WHCL}	(TBD)	(TBD)	—	—	µs
Rise time		t_r	—	—	30	120	ns
Fall time		t_f	—	—	30	120	ns
FR delay time	FR	t_{DFR}	—	–1.0	0.2	1.0	µs

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Low-level pulse width	CL	t_{WLCL}	(TBD)	(TBD)	—	—	µs
High-level pulse width		t_{WHCL}	(TBD)	(TBD)	—	—	µs
Rise time		t_r	—	—	60	240	ns
Fall time		t_f	—	—	60	240	ns
FR delay time	FR	t_{DFR}	—	–2.0	0.4	2.0	µs

○ **Output Timing**

V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

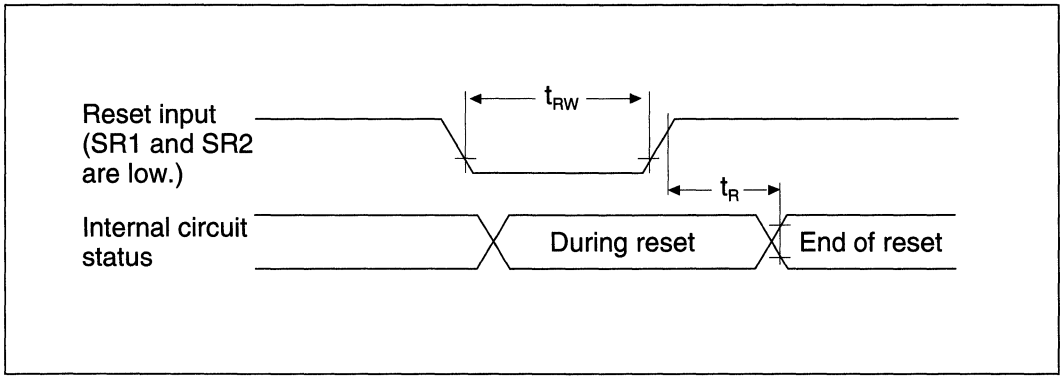
Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	t_{DFR}	CL = 100pF	—	0.2	0.4	µs

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	t_{DFR}	CL = 100pF	—	0.4	0.8	µs

Notes: 1. The FR delay input timing must be set in slave mode; the FR delay output timing must be set in master mode.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

○ **Reset Timing**



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t_R		1.0	—	—	µs
Reset low pulse width	Reset input	t_{RW}		1.0	—	—	µs

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t_R		3.0	—	—	µs
Reset low pulse width	Reset input	t_{RW}		30	—	—	µs

Notes:
1. t_R (reset time) represents the period from the rising edge of reset input to the end of internal circuit reset. The SED1526 Series can operate normally after t_R.
2. t_{RW} specifies the minimum pulse width of reset input. The low pulse exceeding t_{RW} is required for reset.
3. The input signal rise and fall times must be within 15 nanoseconds.
4. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

- **Commands**

The table below lists all available commands. The SED1526 Series uses a combination of A0, $\overline{RD}$ and $\overline{WR}$ (or R/$\overline{W}$) signals to identify data bus signals. Since the chip analyzes and executes each command using the internal clock only (no external clock is required), its processing speed is very high and its busy check is usually not required.

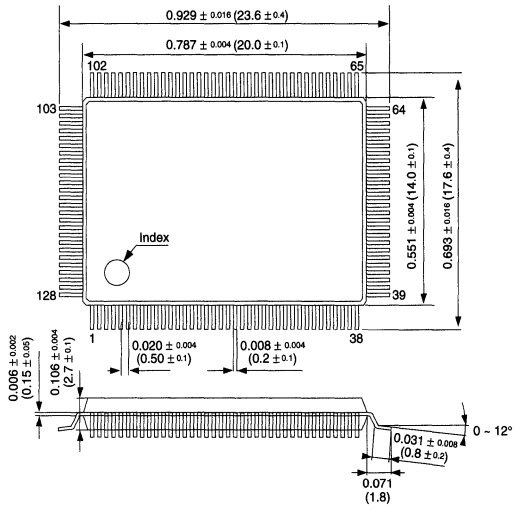
SED1526 Series Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns on LCD panel when goes high, and turns off when goes low.
(2) Initial Display Line	0	1	0	1	1	0	Initial display address					Specifies RAM display line for COM0.
(3) Set Page Address	0	1	0	1	0	1	1	1	Page address			Sets the display RAM page in Page Address register.
(4) Set Column Address	0	1	0	0	Column address							Sets RAM column address in Column register.
(5) Read Status	0	0	1	Status					0	0	0	Reads the status information.
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	D0 = 0 Normal D0 = 1 Inverse
(9) Static Drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Normal indication when low, but full indication when high.
(10) Duty Select	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD driver duty of 1/8 (1/16) when low, and 1/16 (1/32) when high.
(11) Duty+1	0	1	0	1	0	1	0	1	0	1	1	Selects normal LCD driver duty when low, and selects the duty added by 1 when high.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read/Modify/Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Power Control	0	1	0	1	0	1	1	0	Power control			Selects various power circuit functions.
(16) Set Electric Control	0	1	0	1	0	0	Electric control value					Sets V5 output voltage to Electronic Control register.
(17) Clock Stop	0	1	0	1	1	1	0	0	1	1	0/1	Stops clock output at CL when low, and stops clock when high.
(18) Power Save	—	—	—	—	—	—	—	—	—	—	—	A combination of Display OFF and Static Drive ON commands.

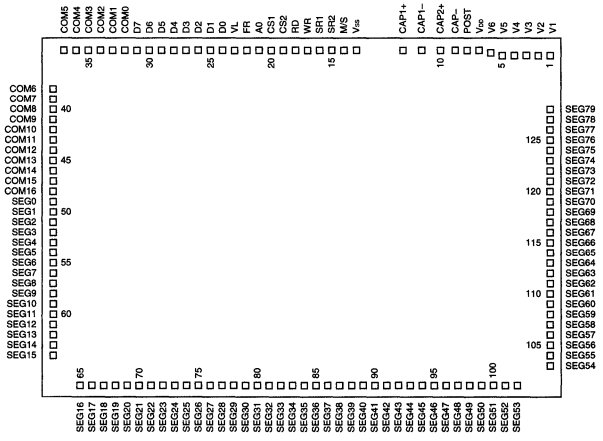
Note: Do not use any other command, or a system malfunction may result.

■ PACKAGE DIMENSIONS

Plastic QFP5-128pin-S1



Unit: inches (mm)



- Aluminum pad chip
  - Chip size ..... 5.92 × 4.86mm
  - Chip thickness .. 0.4mm
  - Pad opening ..... 81 × 85μm MIN
  - Pad pitch ..... 130μm MIN
- Gold bump chip (reference)
  - Chip size ..... 5.92 × 4.86mm
  - Chip thickness .. 0.4mm
  - Bump size ..... 70.9 × 74.7μm MIN
  - Bump height ..... 22.5 ± 5.5μm

■ PAD COORDINATES

PIN		X	Y
No.	Name		
1	V1	2767	2106
2	V2	2637	2106
3	V3	2507	2106
4	V4	2377	2106
5	V5	2246	2106
6	VR	2116	2149
7	V_{DD}	1985	2176
8	V_{OUT}	1857	2176
9	CAP2–	1727	2176
10	CAP2+	1522	2176
11	CAP1–	1318	2176
12	CAP1+	1113	2176
13	V_{SS}	553	2166
14	M/S	356	2185
15	SR1	226	2185
16	SR2	95	2185
17	WR	–35	2185
18	RD	–165	2185
19	CS2	–295	2185
20	CS1	–425	2185
21	A0	–555	2185
22	FR	–719	2185
23	CL	–849	2185
24	D0	–979	2185
25	D1	–1109	2185
26	D2	–1239	2185
27	D3	–1369	2185
28	D4	–1500	2185
29	D5	–1630	2185
30	D6	–1760	2185
31	D7	–1890	2185
32	COM0	–2069	2185
33	COM1	–2199	2185
34	COM2	–2329	2185
35	COM3	–2459	2185
36	COM4	–2589	2185
37	COM5	–2719	2185
38	COM6	–2802	1624
39	COM7	–2802	1524
40	COM8	–2802	1393
41	COM9	–2802	1263
42	COM10	–2802	1133
43	COM11	–2802	1003

PIN		X	Y
No.	Name		
44	COM12	–2802	873
45	COM13	–2802	743
46	COM14	–2802	612
47	COM15	–2802	482
48	COM16	–2802	352
49	SEG0	–2802	193
50	SEG1	–2802	63
51	SEG2	-2802	–67
52	SEG3	-2802	–197
53	SEG4	-2802	–327
54	SEG5	-2802	–457
55	SEG6	-2802	–588
56	SEG7	-2802	–718
57	SEG8	-2802	–848
58	SEG9	-2802	–978
59	SEG10	-2802	–1108
60	SEG11	-2802	–1238
61	SEG12	-2802	–1368
62	SEG13	-2802	–1499
63	SEG14	-2802	–1629
64	SEG15	-2802	–1759
65	SEG16	-2516	–2185
66	SEG17	-2367	–2185
67	SEG18	-2218	–2185
68	SEG19	-2088	–2185
69	SEG20	-1957	–2185
70	SEG21	-1827	–2185
71	SEG22	-1697	–2185
72	SEG23	-1567	–2185
73	SEG24	-1437	–2185
74	SEG25	-1307	–2185
75	SEG26	-1177	–2185
76	SEG27	-1046	–2185
77	SEG28	-916	–2185
78	SEG29	-786	–2185
79	SEG30	-656	–2185
80	SEG31	-526	–2185
81	SEG32	-396	–2185
82	SEG33	-266	-2185
83	SEG34	-135	-2185
84	SEG35	-5	-2185
85	SEG36	125	-2185
86	SEG37	255	-2185

PIN		X	Y
No.	Name		
87	SEG38	385	-2185
88	SEG39	515	-2185
89	SEG40	646	-2185
90	SEG41	776	-2185
91	SEG42	906	-2185
92	SEG43	1036	-2185
93	SEG44	1166	-2185
94	SEG45	1296	-2185
95	SEG46	1426	-2185
96	SEG47	1557	-2185
97	SEG48	1687	-2185
98	SEG49	1817	-2185
99	SEG50	1947	-2185
100	SEG51	2077	-2185
101	SEG52	2226	–2185
102	SEG53	2375	–2185
103	SEG54	2802	–1932
104	SEG55	2802	–1802
105	SEG56	2802	–1672
106	SEG57	2802	–1541
107	SEG58	2802	–1411
108	SEG59	2802	–1281
109	SEG60	2802	–1151
110	SEG61	2802	–1021
111	SEG62	2802	–891
112	SEG63	2802	–760
113	SEG64	2802	–599
114	SEG65	2802	–469
115	SEG66	2802	–339
116	SEG67	2802	–209
117	SEG68	2802	–78
118	SEG69	2802	52
119	SEG70	2802	182
120	SEG71	2802	312
121	SEG72	2802	442
122	SEG73	2802	572
123	SEG74	2802	703
124	SEG75	2802	833
125	SEG76	2802	963
126	SEG77	2802	1093
127	SEG78	2802	1223
128	SEG79	2802	1353

SED1530 Series

DOT MATRIX LCD DRIVER-CONTROLLER

■ DESCRIPTION

The SED1530 Series are intelligent CMOS LCD controller-drivers with the ability to drive alphanumeric and graphic displays. The LSI communicates with a high-speed microprocessor, such as the Intel 80xx and 68xx family, through either a serial or 8-bit parallel interface. It stores the data sent from the microprocessor in the built-in display data RAM (65 × 132 bits) and generates an LCD drive signal.

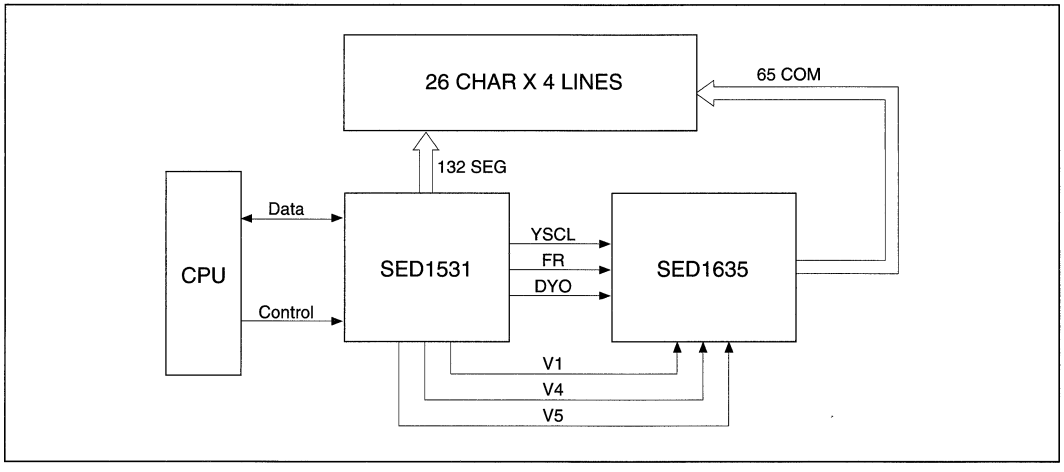
■ FEATURES

- Low-power CMOS technology
- Direct interface to both 80xx and 68xx MPU
- Support 8-bit parallel and serial interface
- On-chip display data RAM ..... 132 × 65 bits
- On-chip DC/DC converter for LCD voltage
- On-chip CR oscillator circuit
- Supports master/slave mode
- Voltage regulator, low-power voltage follower
- –.17%/°C temperature gradient
- 32-level contrast adjustment by software
- 2.4V to 6.0V supply voltage
- –4.5V to –16V LCD voltage
- Operating temperature ..... –40 to 85°C
- Low power consumption 80μA
- Package
  - TAB ..... T**
  - Al pad Die ..... D*A
  - Au bump Die ..... D*B

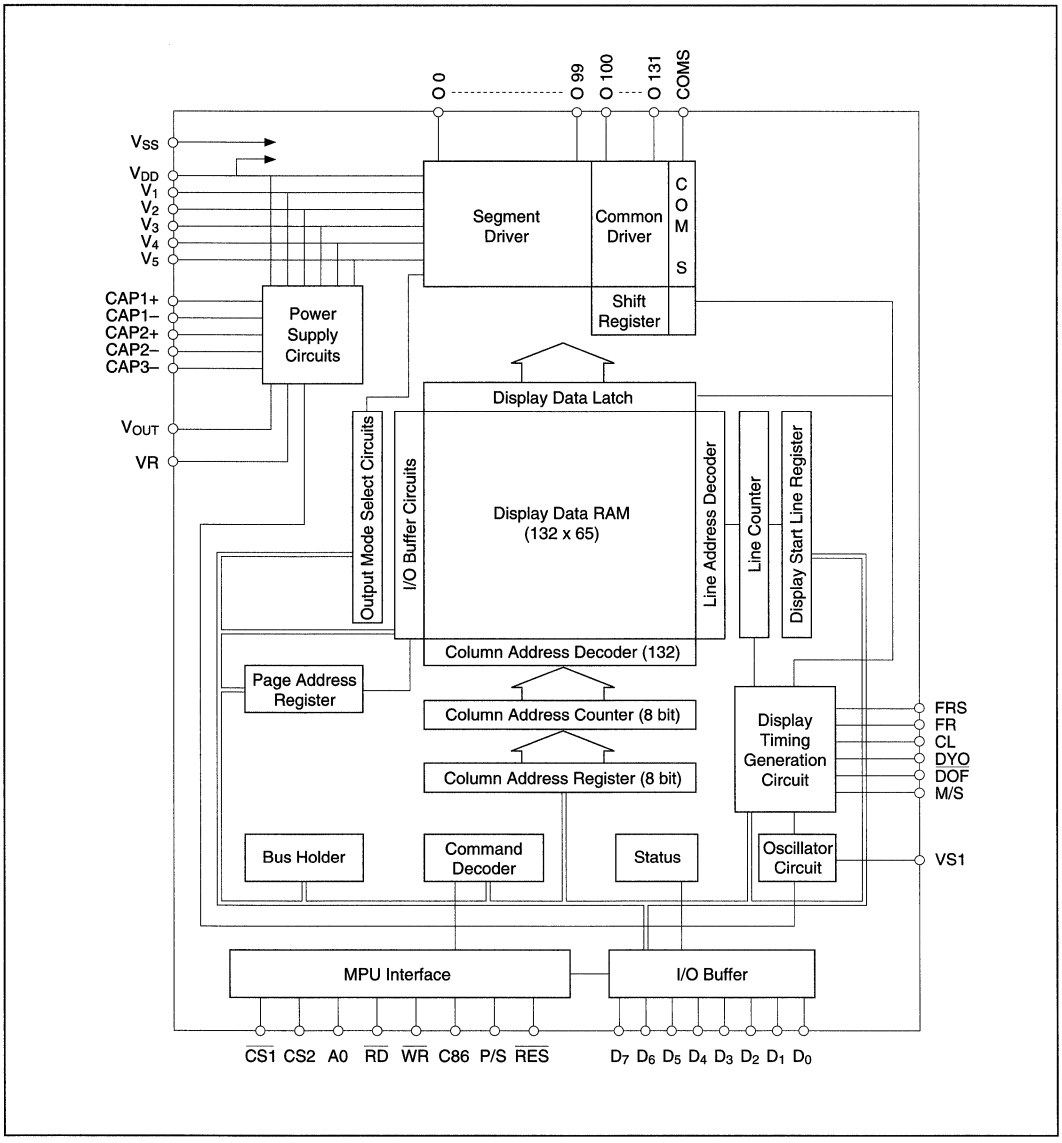
■ AVAILABLE MODELS

Name	Duty	LCD Bias	SEG Driver	COM Driver	Display Area	Remarks
SED1530D0*	1/33	1/5,1/6	100	33	33 × 100	COM single-side assignment
SED1530DA*	1/33	1/5,1/6	100	33	33 × 100	COM dual-side assignment
SED1531D0*	1/65	1/6,1/8	132	0	65 × 132	SED1635 is used for COM
SED1532D0*	1/65	1/6,1/8	100	33	65 × 200	COM single-side right assignment
SED1532DB*	1/65	1/6,1/8	100	33	65 × 200	COM single-side left assignment

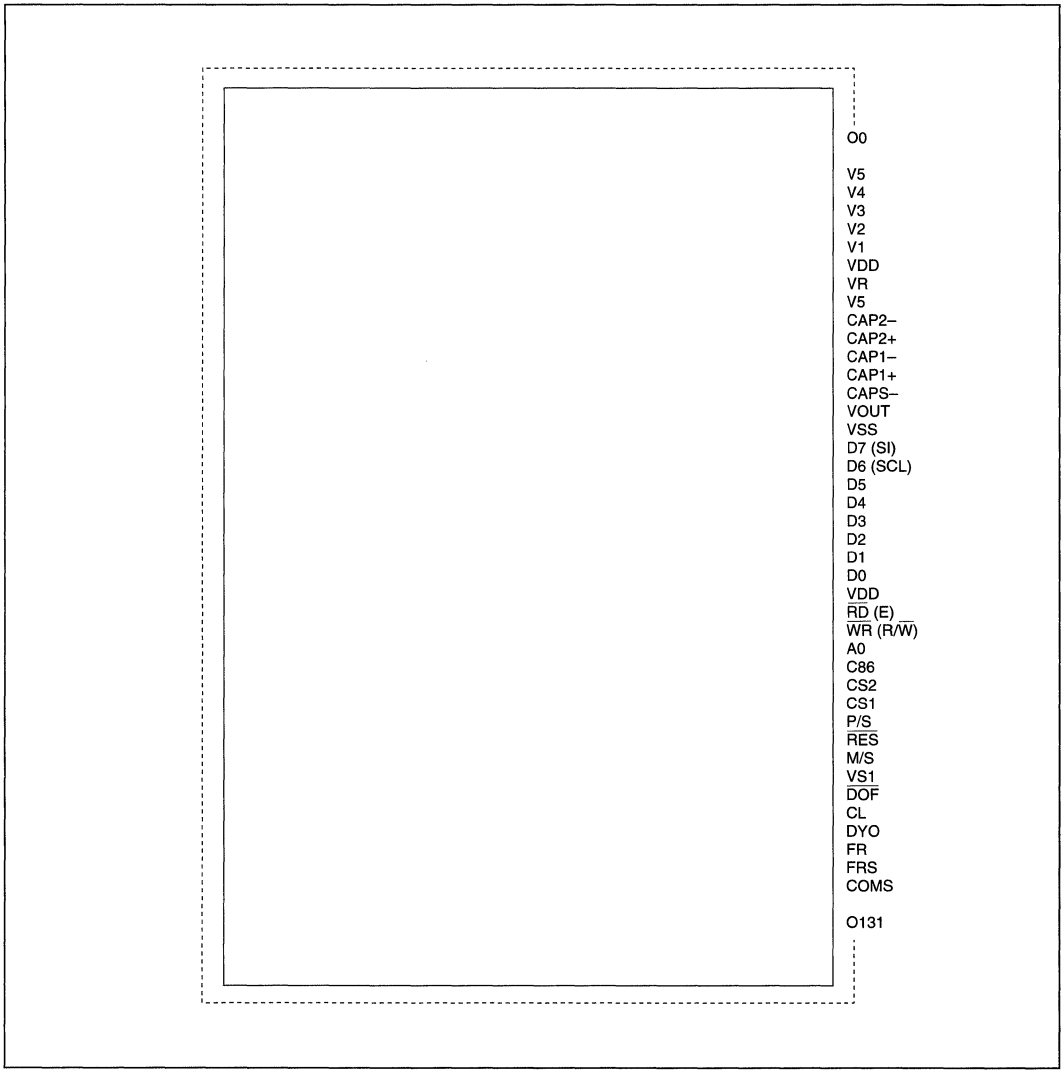
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PINOUT TABLE

Model	Output	O_0 to O_{15}	O_{15} to O_{31}	O_{32} ---------- O_{99}	O_{100} to O_{115}	O_{116} to O_{131}
SED1530*0*	0	SEG0 ---------- SEG99			COM0 ---------- 31	
	1				COM31 ---------- 0	
SED1530*A*	0	COM15 -- 0	SEG0 ---------- SEG99			COM16 31
	1	COM16 31				COM15 -- 0
SED1531*0*		SEG0 ---------- SEG131				
SED1532*0*	0	SEG99 ---------- SEG0				COM31 -- 0
	1					COM0 -- 31
SED1532*B*	0	COM0 -- 31	SEG0 ---------- SEG99			
	1	COM31 -- 0				

Note: * "0" and "1" indicate the mode of the D3 output mode select register.

■ PIN DESCRIPTION

● Power Signals

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of Pins</th></tr>
<tr><td>VDD</td><td>Power</td><td>Connected to +5V power. Connected with MPU power supply VCC pin.</td><td>2</td></tr>
<tr><td>VSS</td><td>Power</td><td>0V, connected to system GND.</td><td>1</td></tr>
<tr><td>V1 ~ V5</td><td>Power</td><td>Multi-level power for LC driver. Transforms impedance using resistive voltage divider or op amps in order to apply the voltage determined for each LC cell. The voltage levels are based on VDD, and must conform to the relationship below:
VDD ≥ V0 ≥ V2 ≥ V3 ≥ V4 ≥ V5
When the master operation power supply is ON, the internal power supply circuitry supplies the V1 ~ V4 voltages shown below. The voltage levels are selected using the LCD bias set command.
<table>
<tr><th></th><th>SED1530D0*</th><th>SED1530DA*, SED1531D0*, SED1532D**</th></tr>
<tr><td>V1</td><td>1/5 × V5 1/6 × V5</td><td>1/5 × V5 1/6 × V5</td></tr>
<tr><td>V2</td><td>2/5 × V5 2/6 × V5</td><td>2/5 × V5 2/6 × V5</td></tr>
<tr><td>V3</td><td>3/5 × V5 4/6 × V5</td><td>3/5 × V5 4/6 × V5</td></tr>
<tr><td>V4</td><td>4/5 × V5 5/6 × V5</td><td>4/5 × V5 5/6 × V5</td></tr>
</table>
</td><td>6</td></tr>
</table>

● LCD Power Circuit Pins

Pin	I/O	Function	Number of Pins
CAP1+	O	Voltage step-up capacitor, positive side connection pin. Connect the capacitor between this pin and CAP1–.	1
CAP1–	O	Voltage step-up capacitor, negative side connection pin. Connect the capacitor between this pin and CAP1+.	1
CAP2+	O	Voltage step-up capacitor, positive side connection pin. Connect the capacitor between this pin and CAP2–.	1
CAP2–	O	Voltage step-up capacitor, negative side connection pin. Connect the capacitor between this pin and CAP2+.	1
CAP3–	O	Voltage step-up capacitor, negative side connection pin. Connect the capacitor between this pin and CAP1+.	1
VOUT	O	Voltage step-up output pin. Connect the capacitor between this terminal and VSS.	1
VR	I	Voltage regulator pin. Use a resistive voltage divider to provide voltage between VDD and V5.	1

- **System Bus Interface Signals**

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of Pins</th></tr>
<tr><td>D7 ~ D0
(SI)
(SCL)</td><td>I/O</td><td>8-bit bi-directional data bus, normally connected to a standard 8-bit or 16-bit MPU data bus.
When serial interface is selected:
D7: Serial Data Input Pin (SI)
D6: Serial Clock Input Pin (SCL)</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Normally the LSB of the MPU address bus is connected to this pin to provide data/command selection:
0: D0 ~ D7 indicate display control data
1: D0 ~ D7 indicate display data</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset to initial settings by setting $\overline{RES}$ to “L”.
The reset operation is performed according to the $\overline{RES}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>Chip Select input pins. Data I/O is enabled by the combination below:
<table><tr><td>Pin Name</td><td>$\overline{CS1}$</td><td>CS2</td></tr><tr><td>State</td><td>“L”</td><td>“H”</td></tr></table></td><td>2</td></tr>
<tr><td>$\overline{RD}$ (E)</td><td>I</td><td>* When connected to an 80-series MPU:
Active “L”
This pin is connected to the $\overline{RD}$ signal from the MPU. When this signal is “L” the SED1530 Series data bus is in output mode.
* When connected to a 68-series MPU:
Active “H”
This is the 68-series MPU enable clock input pin.</td><td>1</td></tr>
<tr><td>$\overline{WR}$ (R/$\overline{W}$)</td><td>I</td><td>* When connected to an 80-series MPU:
Active “L”
This pin is connected to the $\overline{WR}$ signal from the MPU. The data bus signals are retrieved at the rising edge of the $\overline{WR}$ signal.
* When connected to a 68-series MPU:
This is the read/write control signal input pin.
R/$\overline{W}$ = “H”: Read
R/$\overline{W}$ = “L”: Write</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU interface select pin:
C86 = “H”: the 68-series MPU interface
C86 = “L”: the 80-series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Serial data input/parallel data input selection pin:
<table><tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial Clock</td></tr><tr><td>“H”</td><td>$\overline{CS1}$/CS2</td><td>A0</td><td>D0 ~ D7</td><td>$\overline{RD}$/$\overline{WR}$</td><td>—</td></tr><tr><td>“L”</td><td>$\overline{CS1}$/CS2</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table>Note: RAM data read cannot be performed by serial data input. When P/S = L, fix D0 ~ D5 to HZ $\overline{RD}$, and fix $\overline{WR}$ to either “H” or “L”.</td><td>1</td></tr>
</table>

- **LCD Drive Circuit Signals**

Pin	I/O	Function	Number of Pins
M/S	I	This pin selects the master/slave operation of the SED1530 series chips. The master operation outputs the signals necessary for the LCD display. The slave operations input the signals necessary to synchronize the LCD display.	1
CL	I/O	This is the display clock I/O terminal. When using the SED1530 Series chips in master/slave, the CL pins of the chips must be connected. When using in combination with a dedicated common driver, the common driver YSCL pin must be connected to this pin. M/S = "H": Output M/S = "L": Input	1
FR	I/O	This is the LCD alternating current signal I/O pin. When using the SED1530 Series chips in master/slave, the FR pins of the chips must be connected. When using an SED1530 Series chip in master mode, this pin must be connected to the FR pin of the dedicated common driver. M/S = "H": Output M/S = "L": Input	1
DYO	O	This is the common activation output pin. This pin is used only when the SED1530 Series chip is in master mode. This pin must be connected to the common driver DIO pin. This pin is HZ in slave mode.	1
VS1	O	This pin is used to monitor the voltage of the internal power supply.	1
$\overline{DOF}$	I/O	This is the LCD display blanking control pin. When using the SED1530 Series chips in master/slave, the $\overline{DOF}$ pins of the chips must be connected. When using in combination with a dedicated common driver (SED1635), the common driver $\overline{DOFF}$ pin must be connected to this pin. M/S = "H": Output M/S = "L": Input	1
FRS	O	Static drive output pin. This is effective only when in master mode, and is used with the FR pin. This pin is HZ in slave mode.	1

(continued)

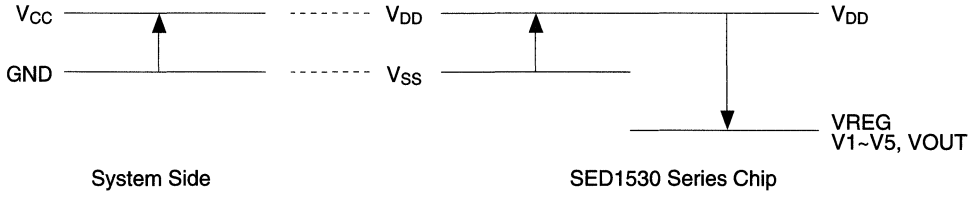
● **LCD Drive Circuit Signals (continued)**

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of Pins</th></tr>
<tr><td>On
(SEG n)
(COM n)</td><td>O</td><td>LC driver output
This output depends on the model type, as shown below:
<table>
<tr><th></th><th>Segment</th><th>Column</th></tr>
<tr><td>SED1530*0*</td><td>O0 ~ O99</td><td>O100 ~ O131</td></tr>
<tr><td>SED1530*A*</td><td>O16 ~ O115</td><td>O0 ~ O15,
O116 ~ O131</td></tr>
<tr><td>SED1531*0*</td><td>O0 ~ O131</td><td>\</td></tr>
<tr><td>SED1530*0*</td><td>O0 ~ O99</td><td>O100 ~ O131</td></tr>
<tr><td>SED1532*B*</td><td>O32 ~ O131</td><td>O0 ~ O31</td></tr>
</table>
Segment Output Terminal
This is the output for driving the LC segments. Through combining the contents of the display RAM with the FR signal, a single level can be selected from VDD, V2, V3, and V5:
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">On Output Voltage</th></tr>
<tr><th>Positive Display</th><th>Negative Display</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>VDD</td><td>V2</td></tr>
<tr><td>L</td><td>V5</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>VDD</td></tr>
<tr><td>L</td><td>V3</td><td>V5</td></tr>
<tr><td>Power Save</td><td>—</td><td colspan="2">VDD</td></tr>
</table>
Common Output Terminal
This is the output for driving the LC commons. Through combining the scan data with the FR signal, a single level can be selected from VDD, V1, V4, and V5:
<table>
<tr><th>Scan Data</th><th>FR</th><th>On Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V5</td></tr>
<tr><td>L</td><td>VDD</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
<tr><td>Power Save</td><td>—</td><td>VDD</td></tr>
</table></td><td>133</td></tr>
<tr><td>COMS</td><td>O</td><td>This is a common output pin dedicated for the indicator.
Leave open if not used. This pin is functional only for the SED1530 and SED1532. It is HZ for the SED1531.</td><td>1</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		V_{DD}	–0.3 to +7.0	V
	(at 3× step-up)		–0.3 to +6.0	V
	(at 4× step-up)		–0.3 to +4.5	V
Power supply voltage (2)	(V_{DD} reference)	V5	–18.0 to +0.3	V
Power supply voltage (3)	(V_{DD} reference)	V1, V2, V3, V4	V5 to +0.3	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V0	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{opr}	–30 to +85	°C
Storage temperature	TCP	T_{STR}	–55 to +100	°C
	Bare chip		–55 to +125	°C



Notes:

1. V1 ~ V5, V_{OUT}, and the V5 voltage are all values based on V_{DD} = 0V.
2. The voltages of V1, V2, V3 and V4 must always fulfill the relationship VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5.
3. Permanent damage to the LSI may result if the absolute maximum ratings are exceeded during use. Under normal operation, use should be within the range of the electrical characteristics listed. Violations of these conditions may cause the LSI to malfunction or may cause loss of reliability in the LSI.

● DC Characteristics

V_{SS} = 0V, V_{DD} = 5V ±10%, T_a = −40 to 85°C

Parameter		Symbol	Condition		Min	Typ	Max	Unit	Pin
Power supply voltage (1)	Recommended operation	V_{DD}			4.5	5.0	5.5	V	V_{SS} *1
	Possible operation	V_{DD}			2.4	—	6.0		
Operating voltage (2)	Possible operation	V5	V_{DD} reference (V_{DD} = 0V)		−16.0	—	−4.0	V	V5 *2
	Possible operation	V1, V2	V_{DD} reference (V_{DD} = 0V)		0.4 × V5	—	V_{DD}	V	V1, V2
	Possible operation	V3, V4	V_{DD} reference (V_{DD} = 0V)		V5	—	0.6 × V5	V	V3, V4
CMOS High-level input voltage		V_{IHC}			0.7 × V_{DD}	—	V_{DD}	V	*3
			V_{DD} = 2.7V		0.8 × V_{DD}	—	V_{DD}		
CMOS Low-level input voltage		V_{ILC}			V_{SS}	—	0.3 × V_{DD}	V	*3
			V_{DD} = 2.7V		V_{SS}	—	0.2 × V_{DD}		
CMOS High-level output voltage		V_{OHC}	I_{OH} = 1mA		0.8 × V_{DD}	—	V_{DD}	V	*5
			V_{DD} = 2.7V	I_{OH} = −0.5mA	0.8 × V_{DD}	—	V_{DD}		
CMOS Low-level output voltage		V_{OLC}	I_{OL} = 1mA		V_{SS}	—	0.2 × V_{DD}	V	*5
			V_{DD} = 2.7V	I_{OL} = 0.5mA	V_{SS}	—	0.2 × V_{DD}		
Schmidt High-level input voltage		V_{IHS}			0.85 × V_{DD}	—	V_{DD}	V	*4
			V_{DD} = 2.7V		0.8 × V_{DD}	—	V_{DD}		
Schmidt Low-level input voltage		V_{ILS}			V_{SS}	—	0.15 × V_{DD}	V	*4
			V_{DD} = 2.7V		V_{SS}	—	0.2 × V_{DD}		
Input leak current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		−1.0	—	1.0	µA	*6
Output leak current		I_{LO}			−3.0	—	3.0	µA	*7
LC driver ON resistance		R_{ON}	T_a = 25°C, V_{DD} ref.	V5 = −14.0V	—	2.0	3.0	kΩ	SEG*n*
				V5 = −8.0V	—	3.0	4.5	kΩ	COM*n*
Static consumption current		I_{SSQ}	V_{IN} = V_{DD} or V_{SS}		—	0.01	5.0	µA	V_{SS}
		I_{5Q}	V5 = −18.0V V_{DD} ref.		—	0.01	15.0	µA	V5
Input terminal capacitance		C_{IN}	T_a = 25°C f = 1MHz		—	5.0	8.0	pF	*3, *4
Oscillator frequency		f_{OSC}	T_a = 25°C	V_{DD} = 5.0V	19	22	25	kHz	
				V_{DD} = 2.7V	19	22	25		
Internal Power Supply Circuit Input voltage		V_{DD}	When 3× step-up		2.4	—	6.0	V	
			When 4× step-up		2.4	—	4.5		
Internal Power Supply Circuit Booster output voltage		V_{OUT}	When 3× set-up	V_{DD} Ref.	−18.0	—	—	V	V_{OUT}
Internal Power Supply Circuit Voltage regulator circuit operating voltage		V_{OUT}		V_{DD} Ref.	−18.0	—	−6.0	V	V_{OUT}
Internal Power Supply Circuit Voltage follower operating voltage		V5 (1)	When applied to the SED1530	V_{DD} Ref.	−16.0	—	−6.0	V	
		V5 (2)	When applied to the SED1531	V_{DD} Ref.	−16.0	—	−4.6	V	
Internal Power Supply Circuit Reference voltage		V_{REG}	T_a = 25°C	V_{DD} Ref.	−2.65	−2.5	−2.35	V	

- **Dynamic consumption current value (1) in display, internal power supply ON**

Unless otherwise specified, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remarks
SED1530	I_{DD} (1)	V_{DD} = 5.0V, V5 – V_{DD} = –8.0V, 2× Step-up	—	41	70	µA	
		V_{DD} = 3.0V, V5 – V_{DD} = –8.0V, 3× Step-up	—	48	80	µA	
SED1531		V_{DD} = 5.0V, V5 – V_{DD} = –11.0V, 3× Step-up	—	96	160	µA	
		V_{DD} = 3.0V, V5 – V_{DD} = –11.0V, 4× Step-up	—	118	190	µA	
SED1532		V_{DD} = 5.0V, V5 – V_{DD} = –11.0V, 3× Step-up	—	96	160	µA	
		V_{DD} = 3.0V, V5 – V_{DD} = –11.0V, 4× Step-up	—	114	190	µA	

- **Current consumption in power save mode**

(V_{SS} = 0V, V_{DD} = 2.7 to 5.5V, T_a = 25°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Standby	I_{DDS1}	SED1530, SED1531, SED1532	—	0.01	1.0	µA
	I_{DDS2}	SED1530, SED1531, SED1532	—	1.0	2.0	µA

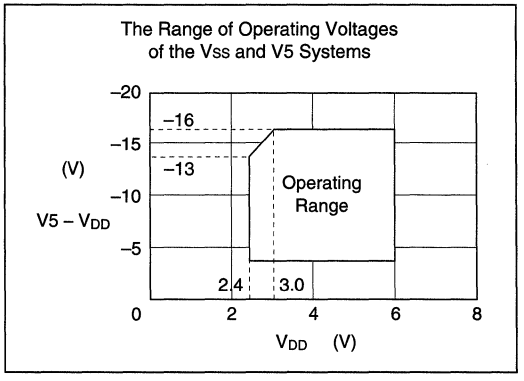
Typical current consumption characteristics:

Dynamic current consumption (1)
LCD display status using an external power supply

● Notes

*1. Although a broad operating voltage range is guaranteed, this does not guarantee against sudden voltage changes during MPU access.

*2. The range of operating voltages of the V_{DD} system and V5 system. See the figure below. The range of operating voltages applies when the external power supply is used.



*3. The A0, D0 to D5, D6, D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, M/S, C86, P/S and $\overline{DOF}$ pins.

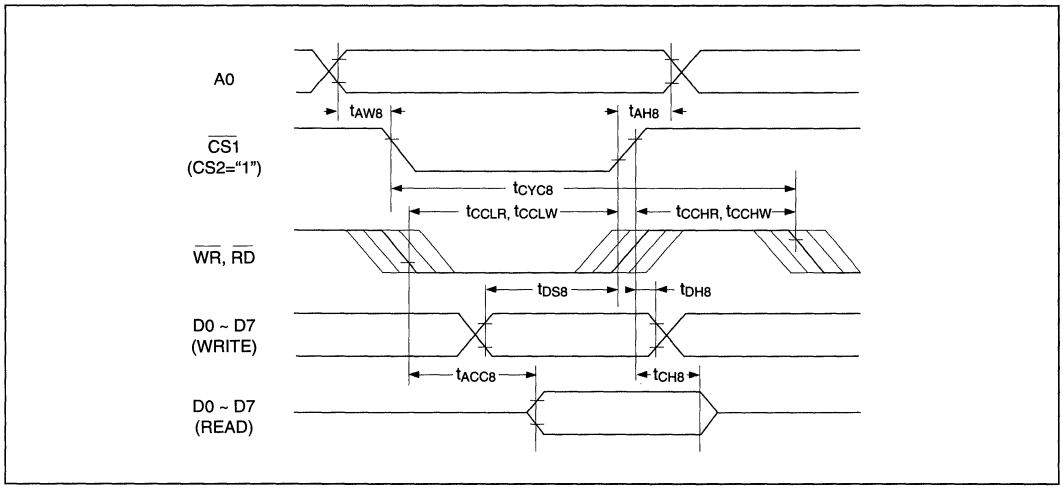
*4. The CL, SCL (D6) and $\overline{RES}$ pins.

*5. The D0 to D5, D6, D7 (SI), FR, FRS, DYO, $\overline{DOF}$ and CL pins.

*6. The A0, $\overline{RD}$, (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, M/S, $\overline{RES}$, C86 and P/S pins.

*7. Applicable when the D0 to D7, FR, CL, DYO and $\overline{DOF}$ pins are in a high impedance state.

- **Timing Characteristics**
  - **System Bus: Read/Write Characteristics I (80-Series MPU)**



V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	t_{AH8}		10	—	ns
Address setup time		t_{AW8}		10	—	ns
System cycle time		t_{CYC8}		200	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		22	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		77	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		172	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		117	—	ns
Data setup time	D0 ~ D7	t_{DS8}		20	—	ns
Data hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100pF	—	70	ns
Output disable time		t_{CH8}		10	50	ns

V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

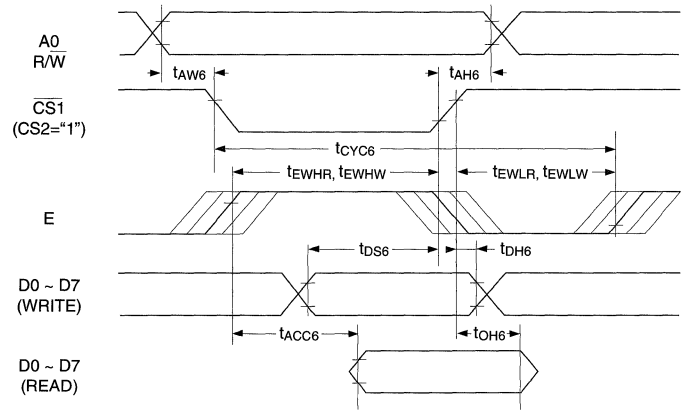
Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	t_{AH8}		25	—	ns
Address setup time		t_{AW8}		25	—	ns
System cycle time		t_{CYC8}		450	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		44	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		194	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		394	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		244	—	ns
Data setup time	D0 ~ D7	t_{DS8}		40	—	ns
Data hold time		t_{DH8}		20	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100pF	—	140	ns
Output disable time		t_{CH8}		10	100	ns

*1. The input signal rise time and fall time (tr, tf) are specified at 15ns or less. When the cycle time is used at high speed, the specification is tr + tf ≤ (t_{CYC8} – t_{CCLW} – t_{CCHW}) or tr + tf ≤ (t_{CYC8} – t_{CCLR} – t_{CCHR}).

*2. All timings are specified based on 20% and 80% of V_{DD}.

*3. t_{CCLW} and t_{CCLR} are specified by the overlap period of $\overline{CS1}$ = "0" (CS2 = "1") and $\overline{WR}$, $\overline{RD}$ = "0" level.

○ System Bus: Read/Write Characteristics I (68-Series MPU)



V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter		Signal	Symbol	Conditions	Min	Max	Unit
System cycle time			t_{CYC6}		200	—	ns
Address setup time		A0	t_{AW6}		10	—	ns
Address hold time		R/W	t_{AH6}		10	—	ns
Data setup time		D0 ~ D7	t_{DS6}		20	—	ns
Data hold time			t_{DH6}		10	—	ns
Output disable time			t_{OH6}	CL = 100pF	10	50	ns
Access time			t_{ACC6}		—	70	ns
Enable H pulse width	Read	E	t_{EWHR}		77	—	ns
	Write		t_{EWHW}		22	—	ns
Enable L pulse width	Read	E	t_{EWLR}		117	—	ns
	Write		t_{EWLW}		172	—	ns

V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

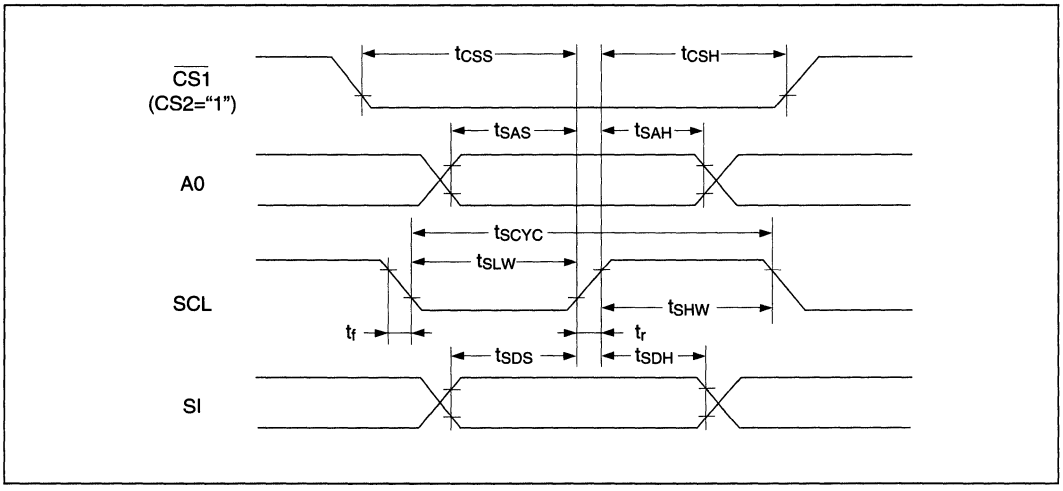
Parameter		Signal	Symbol	Conditions	Min	Max	Unit
System cycle time			t_{CYC6}		450	—	ns
Address setup time		A0	t_{AW6}		25	—	ns
Address hold time		R/W	t_{AH6}		25	—	ns
Data setup time		D0 ~ D7	t_{DS6}		40	—	ns
Data hold time			t_{DH6}		20	—	ns
Output disable time			t_{OH6}	CL = 100pF	20	50	ns
Access time			t_{ACC6}		—	70	ns
Enable H pulse width	Read	E	t_{EWHR}		194	—	ns
	Write		t_{EWHW}		44	—	ns
Enable L pulse width	Read	E	t_{EWLR}		244	—	ns
	Write		t_{EWLW}		394	—	ns

*1. The input signal rise time and fall time (tr, tf) are specified at 15ns or less. When the cycle time is used at high speed, the specification is $tr + tf \leq (t_{CYC8} - t_{EWLW} - t_{EWHW})$ or $tr + tf \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$.

*2. All timings are specified based on 20% and 80% of V_{DD}.

*3. t_{EWHR} and t_{EWHW} are specified by the overlap period of $\overline{CS1}$ = "0" (CS2 = "1") and E = "1" level.

○ Serial Interface



V_{DD} = 5.0V ± 10%, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock period	SCL	tSCYC		500	—	ns
SCL "H" pulse width		tSHW		150	—	ns
SCL "L" pulse width		tSLW		150	—	ns
Address setup time	A0	tSAS		120	—	ns
Address hold time		tSAH		200	—	ns
Data setup time	SI	tSDS		120	—	ns
Data hold time		tSDH		50	—	ns
CS-SCL time	CS	tCSS		30	—	ns
		tCSH		400	—	ns

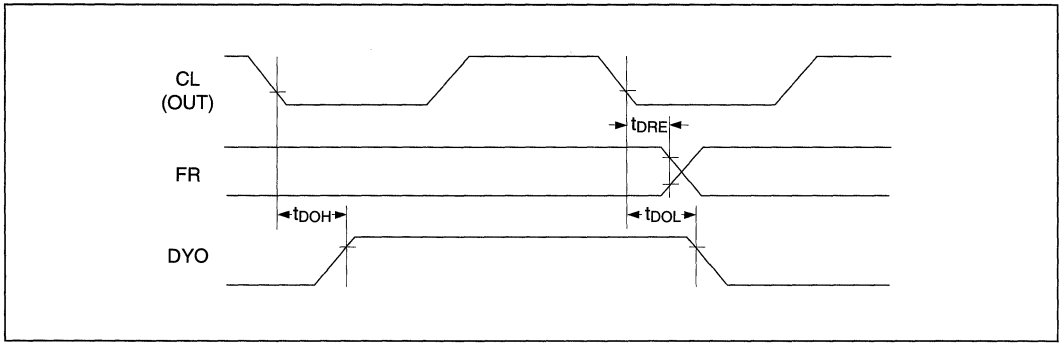
V_{DD} = 2.7 to 4.5V, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock period	SCL	tSCYC		1000	—	ns
SCL "H" pulse width		tSHW		300	—	ns
SCL "L" pulse width		tSLW		300	—	ns
Address setup time	A0	tSAS		250	—	ns
Address hold time		tSAH		400	—	ns
Data setup time	SI	tSDS		250	—	ns
Data hold time		tSDH		100	—	ns
CS-SCL time	CS	tCSS		60	—	ns
		tCSH		400	—	ns

*1. The input signal rise time and fall time (tr, tf) are specified at 15ns or less.

*2. All timings are specified based on 20% and 80% of V_{DD}.

○ Display Control Timing



V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	t_{DFR}	CL = 50pF	—	80	150	ns
DYO "H" delay time	DYO	t_{DOH}		—	70	160	ns
DYO "L" delay time		t_{DOL}		—	70	160	ns

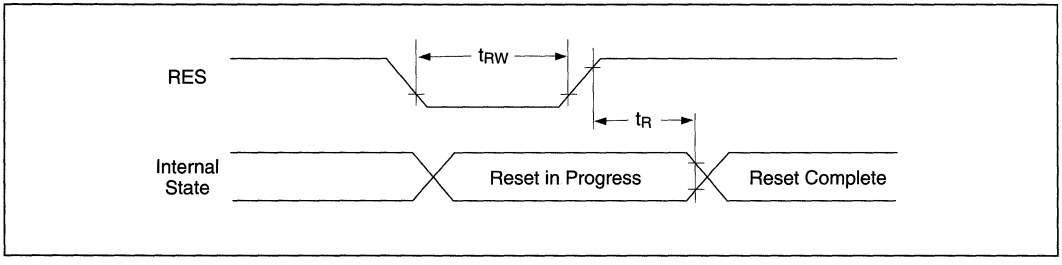
V_{DD} = 2.7 to 4.5V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	t_{DFR}	CL = 50pF	—	120	240	ns
DYO "H" delay time	DYO	t_{DOH}		—	140	250	ns
DYO "L" delay time		t_{DOL}		—	140	250	ns

*1. Effective only when operating in master mode.

*2. All timings are specified based on 20% or 80% of V_{DD}.

○ Reset Timing



V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t_R		1.0	—	—	ms
Reset "L" pulse width	RES	t_{RW}		1.0	—	—	ms

V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t_R		3.0	—	—	ms
Reset "L" pulse width	RES	t_{RW}		3.0	—	—	ms

*1. All timings are specified based on 10% and 90% of V_{DD}.

● Table of Commands for the SED1530 Series

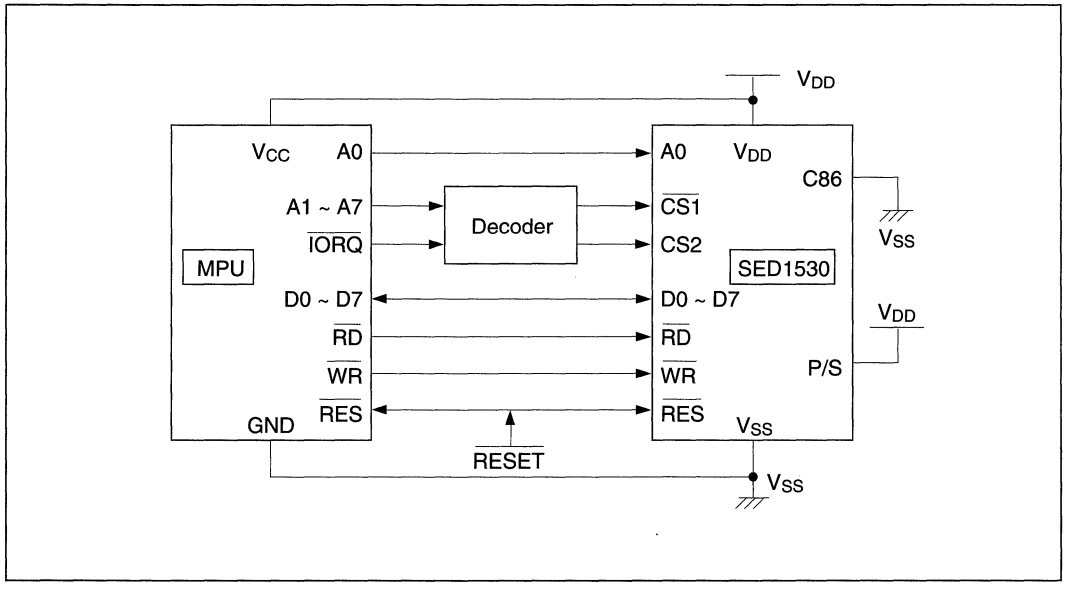
Command		Code											Function
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns the LCD display on and off. 0: OFF 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address						Determines the RAM display line displayed to COM0.
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page to the page address register.
(4)	Column address set, first 4 bits	0	1	0	0	0	0	1	Most significant column address bits				Sets the 4 most significant bits of the display RAM column address to the register.
(4)	Column address set, last 4 bits	0	1	0	0	0	0	0	Least significant column address bits				Sets the 4 least significant bits of the display RAM column address to the register.
(5)	Status read	0	0	1	Status				0	0	0	0	Read status data.
(6)	Write display data	1	1	0	Write data								Writes to the display RAM.
(7)	Reads display data	1	0	1	Read data								Reads from the display RAM.
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the relationship between the display RAM address and the SEG output 0: Normal 1: Reverse
(9)	Display: Normal/Reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display to normal/ reverse. 0: Normal 1: Reverse
(10)	Display: All Pixel Lit: ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display: All Pixels Lit 0: Normal display 1: All pixels lit
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage ratio.
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address counter by 1 when write, zero when read.
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Gets out of read/modify/write mode.
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset.
(15)	Output mode register set	0	1	0	1	1	0	0	0	*	*	*	Selects the direction of the COM output scan. * = disabled
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode			Selects the power supply circuit operating mode.
(17)	Electronic volume register set	0	1	0	1	0	0	Electronic volume level					Sets the V5 output voltage to the electronic volume register.
(18)	Standby set	0	1	0	1	0	1	0	1	1	0	0 1	Selects the standby mode. 0: OFF 1: ON
(19)	Power save												A composite command with display: OFF and Display: All Pixels On.

Note: Do not use any other command, or a system malfunction may result.

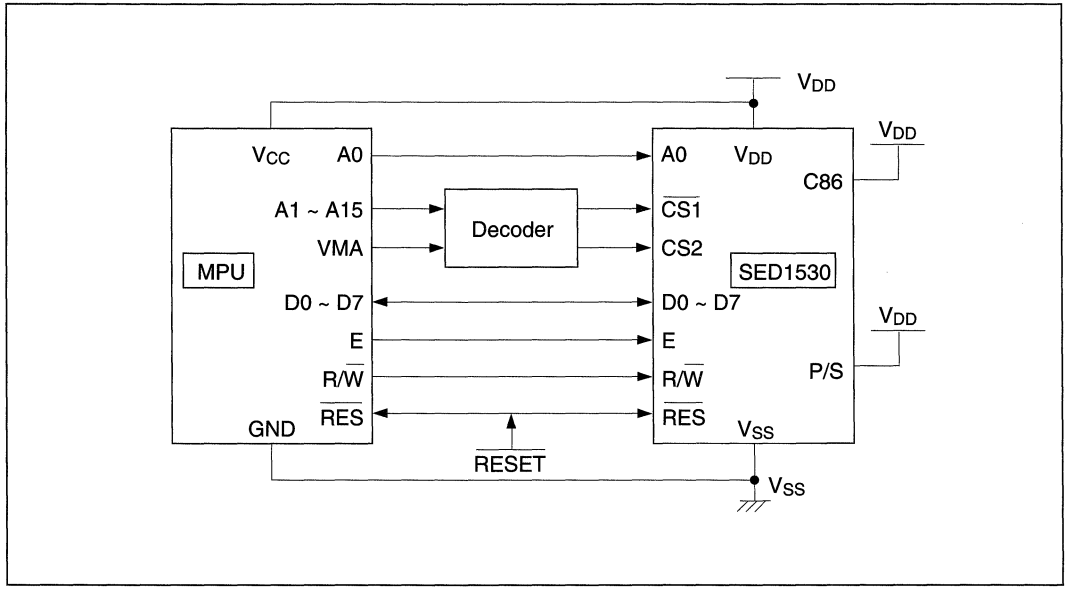
■ MPU INTERFACE (REFERENCE EXAMPLE)

The SED1530 Series chips can be connected to 80-series and 68-series MPUs. Moreover, by utilizing the serial interface, the connections can be made with fewer signal lines. When multiple SED1530 chips are used, each can be connected to the MPU and the chips can be selected using the chip select.

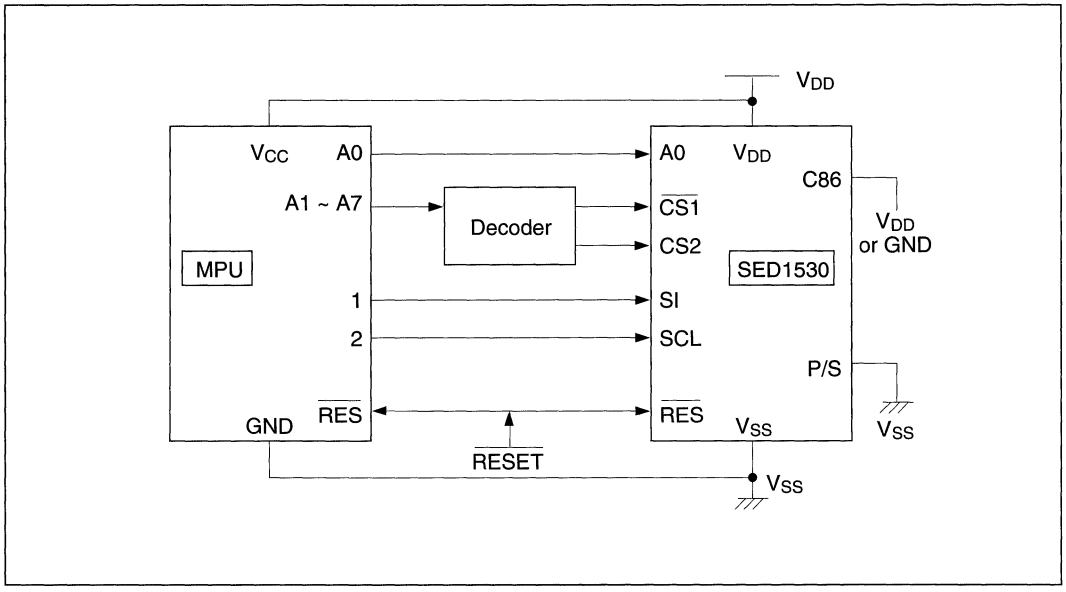
● 80-Series MPU



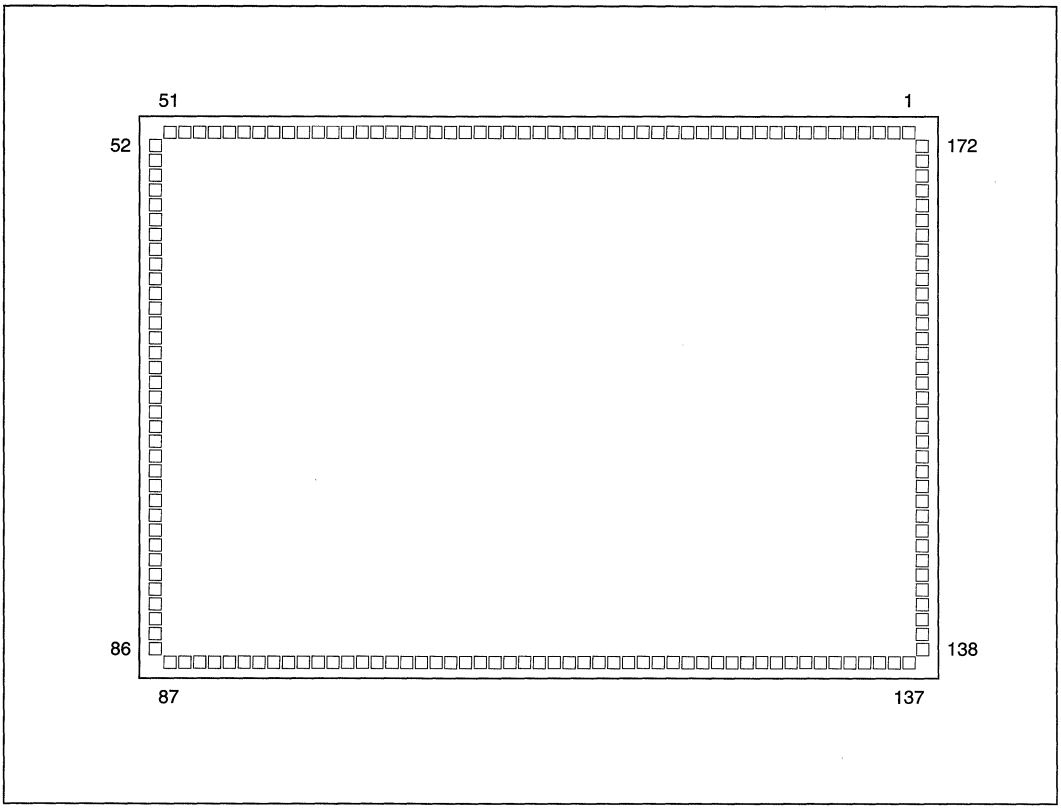
● 68-Series MPU



● **Serial Interface**



■ PIN LAYOUT



Chip Size:	6.65 X 4.57 mm
Pad Pitch:	118μm (Min.)
SED153*D-A	(Aluminum Pad Model)
Pad Center Size:	90 X 90 μm
Chip Thickness:	300 μm
SED153*D-B	(Gold Bump Model)
Bump Size:	76 X 76 μm
Bump Height:	17 to 28 μm (Typ)
Chip Thickness:	625 μm

■ PAD COORDINATES

Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	O127	2988	2142
2	O128	2860	2142
3	O129	2738	2142
4	O130	2614	2142
5	O131	2490	2142
6	COM3	2386	2142
7	FR5	2242	2142
8	FR	2124	2142
9	DYO	2006	2142
10	CL	1000	2142
11	$\overline{DOF}$	1770	2142
12	VSI	1652	2142
13	M/S	1534	2142
14	$\overline{REG}$	1416	2142
15	P/S	1298	2142
16	$\overline{CS1}$	1180	2142
17	CS2	1062	2142
18	C86	944	2142
19	A0	826	2142
20	$\overline{WR}$ (W/$\overline{R}$)	708	2142
21	$\overline{RD}$ ($\overline{E}$)	590	2142
22	V_{DD}	354	2142
23	D0	236	2142
24	D1	236	2142
25	D2	118	2142
26	D3	0	2142
27	D4	–118	2142
28	D5	–236	2142
29	D6 (SCL)	–354	2142
30	D7 (31)	–472	2142
31	V_{SS}	–590	2142
32	V_{OUT}	–708	2142
33	CAP3–	–826	2142
34	CAP1+	–944	2142
35	CAP1–	–1062	2142
36	CAP2+	–1180	2142
37	CAP2–	–1298	2142
38	V5	–1416	2142
39	VR	–1534	2142
40	V_{DD}	–1652	2142
41	V_1	–1770	2142
42	V_2	–1888	2142
43	V_3	–2006	2142
44	V_4	–2124	2142
45	V_5	–2242	2142
46	O0	–2366	2142
47	O1	–2490	2142
48	O2	–2614	2142
49	O3	–2738	2142
50	O4	–2862	2142
51	O5	–2986	2142
52	O6	–3178	2006
53	O7	–3178	1888
54	O8	–3178	1770
55	O9	–3178	1652
56	O10	–3178	1534
57	O11	–3178	1416
58	O12	–3178	1286
59	O13	–3178	1150
60	O14	–3178	1062
61	O15	–3178	944
62	O16	–3178	826
63	O17	–3178	708
64	O18	–3178	690
65	O19	–3178	472
66	O20	–3178	364
67	O21	–3178	238
68	O22	–3178	118
69	O23	–3178	0
70	O24	–3178	–118
71	O25	–3178	–236
72	O26	–3178	–354
73	O27	–3178	–472
74	O28	–3178	–590
75	O29	–3178	–708
76	O30	–3178	–826
77	O31	–3178	–944
78	O32	–3178	–1062
79	O33	–3178	–1180
80	O34	–3178	–1298
81	O35	–3178	–1418
82	O36	–3178	–1534
83	O37	–3178	–1652
84	O38	–3178	–1770
85	O39	–3178	–1888
86	O40	–3178	–2006
87	O41	–2986	–2142
88	O42	–2862	–2142
89	O43	–2738	–2142
90	O44	–2614	–2142
91	O45	–2490	–2142
92	O46	–2386	–2142
93	O47	–2242	–2142
94	O48	–2124	–2142
95	O49	–2006	–2142
96	O50	–1888	–2142
97	O51	–1770	–2142
98	O52	–1652	–2142
99	O53	–1534	–2142
100	O54	–1416	–2142
101	O55	–1298	–2142
102	O56	–1180	–2142
103	O57	–1062	–2142
104	O58	–944	–2142
105	O59	–826	–2142
106	O60	–708	–2142
107	O61	–590	–2142
108	O62	–472	–2142
109	O63	–354	–2142
110	O64	–236	–2142
111	O65	–118	–2142
112	O66	0	–2142
113	O67	118	–2142
114	O68	236	–2142
115	O69	354	–2142
116	O70	472	–2142
117	O71	590	–2142
118	O72	708	–2142
119	O73	826	–2142
120	O74	944	–2142
121	O75	1062	–2142
122	O76	1180	–2142
123	O77	1298	–2142
124	O78	1416	–2142
125	O79	1534	–2142
126	O80	1652	–2142
127	O81	1770	–2142
128	O82	1888	–2142
129	O83	2006	–2142
130	O84	2124	–2142
131	O85	2242	–2142
132	O86	2366	–2142
133	O87	2490	–2142
134	O88	2614	–2142
135	O89	2738	–2142
136	O90	2862	–2142
137	O91	2986	–2142
138	O92	3178	–2006
139	O93	3178	–1888
140	O94	3178	–1770
141	O95	3178	–1652
142	O96	3178	–1534
143	O97	3178	–1416
144	O98	3178	–1298
145	O99	3178	–1180
146	O100	3178	–1062
147	O101	3178	–944
148	O102	3178	–826
149	O103	3178	–708
150	O104	3178	–590
151	O105	3178	–472
152	O106	3178	–354
153	O107	3178	–236
154	O108	3178	–118
155	O109	3178	0
156	O110	3178	118
157	O111	3178	236
158	O112	3178	354
159	O113	3178	472
160	O114	3178	590
161	O115	3178	708
162	O116	3178	826
163	O117	3178	944
164	O118	3178	1062
165	O119	3178	1180
166	O120	3178	1298
167	O121	3178	1416
168	O122	3178	1534
169	O123	3178	1652
170	O124	3178	1770
171	O125	3178	1888
172	O126	3178	2006

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CMOS DOT MATRIX LCD CONTROLLER/DRIVER

■ DESCRIPTION

The SED1540 is an LCD driver-controller intended mainly for segment type liquid crystal displays. The device communicates with a host microprocessor through an 8-bit parallel data. The SED1540 stores the data that is sent from the microcomputer in the built-in data display RAM, and generates a liquid drive signal.

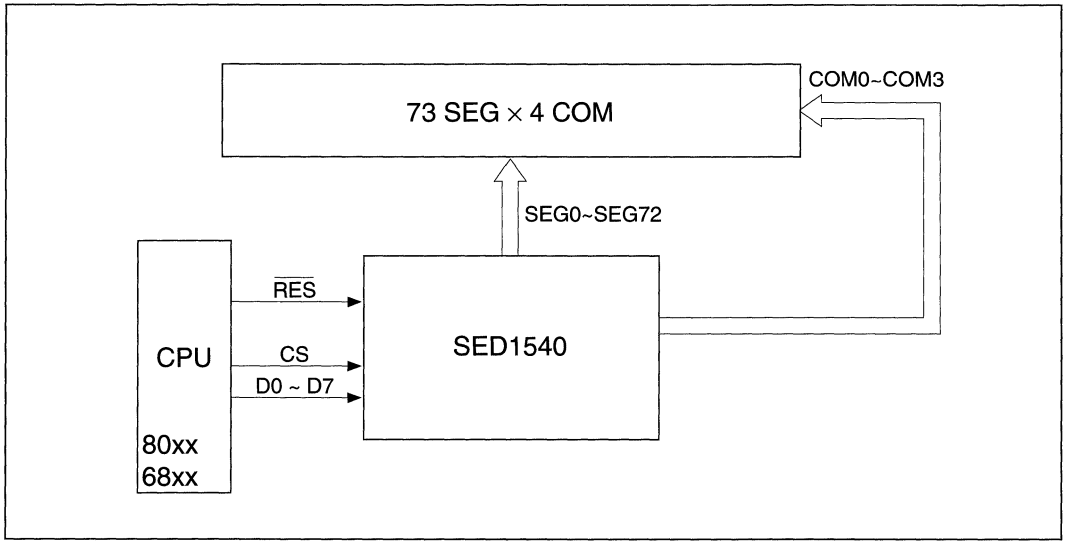
The device is manufactured with a low power consumption CMOS process. These features give the designer a flexible means of implementing a small to medium size LCD display for a compact, low power system.

■ FEATURES

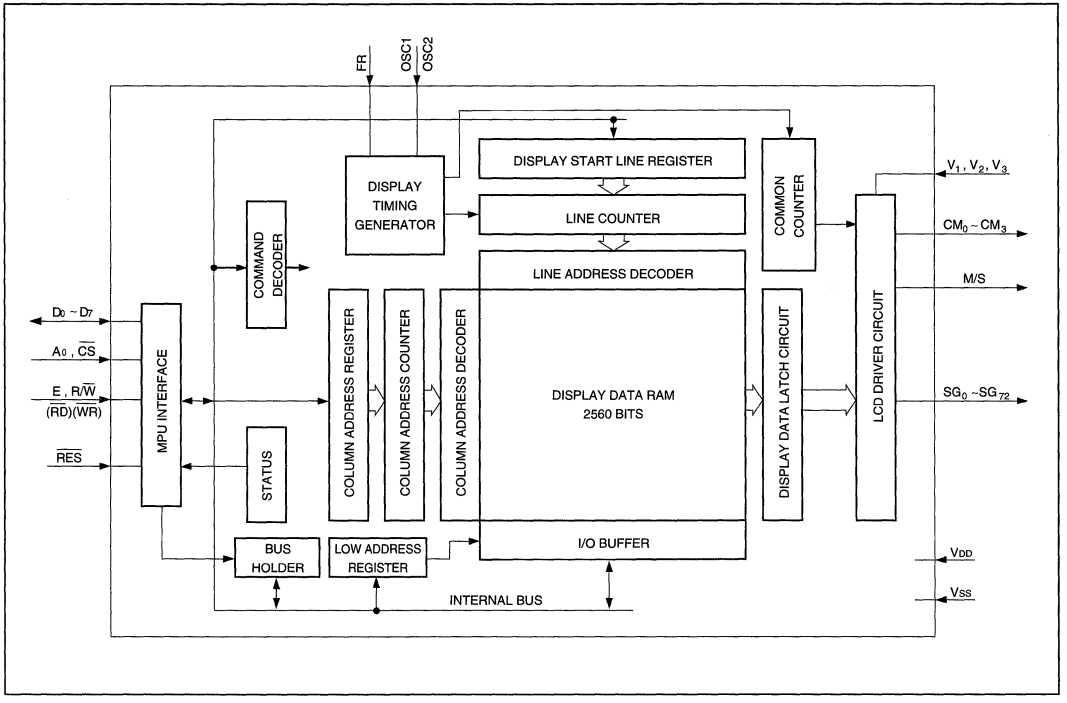
- Low-power CMOS technology
- Fast CPU 8-bit data interface (80xx, 68xx)
- 1/4 duty cycle
- Built-in LCD driver circuit ..... 73 segments
  4 commons
- Built-in display data RAM ..... 2560 bits
- Rich display command setting
- On-chip CR oscillation circuit
- Master/slave operation is supported
- Recommended expansion driver SED1521
  (80-segment driver)
- Low power consumption ..... 30μW max
- LCD voltage ..... 3.5 to 11V
- Single power supply ..... 2.4 to 7.0V
- Package ..... QFP5-100 pin (FOA)
  Al pad (DOA)
  Au bump (DOB)

Clock Source	fCL	Frame Frequency
External clock	4 kHz	85/64 Hz
Internal osc.	18 kHz	375/281 Hz

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



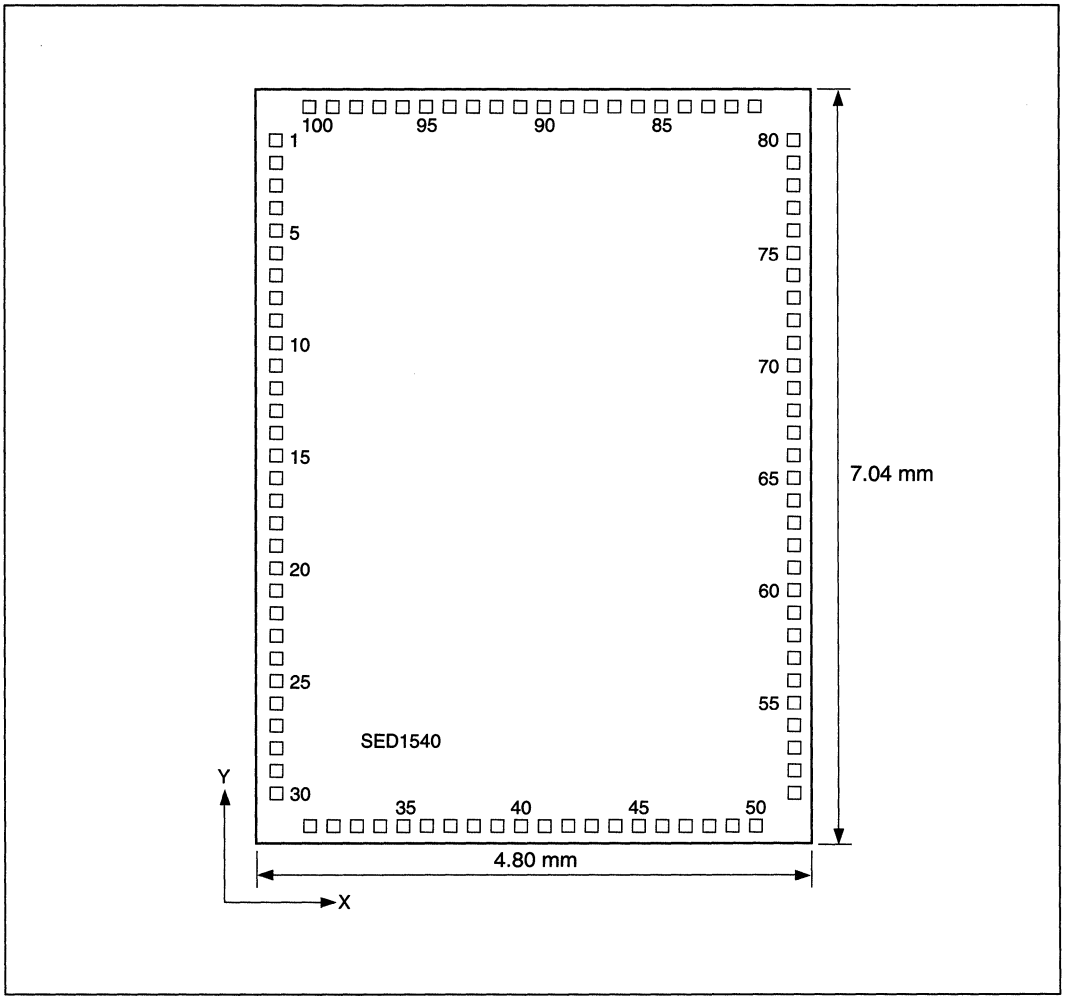
■ PIN DESCRIPTION

For chip pad locations see Mechanical Specifications.

Number	Name	Number	Name	Number	Name	Number	Name
1	SEG71	26	SEG46	51	SEG21	76	E ($\overline{RD}$)
2	SEG70	27	SEG45	52	SEG20	77	R/$\overline{W}$ ($\overline{WR}$)
3	SEG69	28	SEG44	53	SEG19	78	V_{SS}
4	SEG68	29	SEG43	54	SEG18	79	DB0
5	SEG67	30	SEG42	55	SEG17	80	DB1
6	SEG66	31	SEG41	56	SEG16	81	DB2
7	SEG65	32	SEG40	57	SEG15	82	DB3
8	SEG64	33	SEG39	58	SEG14	83	DB4
9	SEG63	34	SEG38	59	SEG13	84	DB5
10	SEG62	35	SEG37	60	SEG12	85	DB6
11	SEG61	36	SEG36	61	SEG11	86	DB7
12	SEG60	37	SEG35	62	SEG10	87	V_{DD}
13	SEG59	38	SEG34	63	SEG9	88	$\overline{RES}$
14	SEG58	39	SEG33	64	SEG8	89	FR
15	SEG57	40	SEG32	65	SEG7	90	V3
16	SEG56	41	SEG31	66	SEG6	91	$\overline{CS}$
17	SEG55	42	SEG30	67	SEG5	92	NC
18	SEG54	43	SEG29	68	SEG4	93	M/$\overline{S}$
19	SEG53	44	SEG28	69	SEG3	94	V2
20	SEG52	45	SEG27	70	SEG2	95	V1
21	SEG51	46	SEG26	71	SEG1	96	COM0
22	SEG50	47	SEG25	72	SEG0	97	COM1
23	SEG49	48	SEG24	73	A0	98	COM2
24	SEG48	49	SEG23	74	OSC1	99	COM3
25	SEG47	50	SEG22	75	OSC2	100	SEG72

Duty	Pin	
	98	99
1/4	COM2	COM3
1/3	NC	COM2

■ PAD LAYOUT



● Al pad

Chip Specification	Dimensions
Die size	4.80 × 7.04 × 0.525 mm
Pad size	100 × 100 μm

● Au bump pad

Chip Specification	Dimensions
Minimum bump pitch	199 μm
Bump height	20 μm +10/–5 μm
Bump size	132 × 111 μm ± 20 μm

■ PAD COORDINATES

Pad		X	Y
No.	Name		
1	SEG71	159	6507
2	SEG70	159	6308
3	SEG69	159	6108
4	SEG68	159	5909
5	SEG67	159	5709
6	SEG66	159	5510
7	SEG65	159	5310
8	SEG64	159	5111
9	SEG63	159	4911
10	SEG62	159	4712
11	SEG61	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	5041	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159

Pad		X	Y
No.	Name		
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	2696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948

Pad		X	Y
No.	Name		
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	OSC1	4641	5247
75	OSC2	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/$\overline{W}$ ($\overline{WR}$)	4641	5846
78	Vss	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	VDD	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V3	2499	6884
91	$\overline{CS}$	2300	6884
92	NC	2100	6884
93	M/$\overline{S}$	1901	6884
94	V2	1701	6884
95	V1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	SEG72	504	6884

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■ DESCRIPTION

The SED1560 Series are intelligent CMOS LCD driver-controllers with the ability to drive alphanumeric and graphic displays. The SED1560 Series communicates with a high-speed microprocessor, such as the Intel 80XX family or the Motorola 68XX family, through either a serial or an 8-bit parallel interface. It stores the data sent from the microprocessor in the built-in display data RAM (166 × 65 bits) and generates an LCD drive signal. These devices incorporate an internal DC/DC converter to generate the negative voltage needed for LCD contrast. The controllers feature software contrast adjustment by command setting.

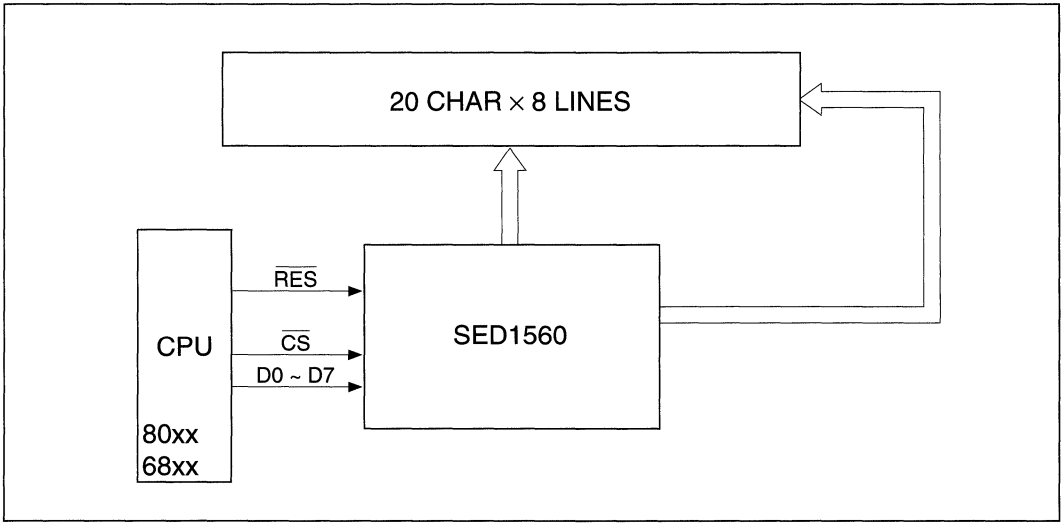
The three different versions of the SED1560 Series support the following duty ratios and display sizes:

Model	Duty Ratio	SEG × COM
SED1560	1/65, 1/64, 1/49, 1/48	102 × 65
SED1561	1/33, 1/32, 1/25, 1/24	134 × 33
SED1562	1/17, 1/16	150 × 17

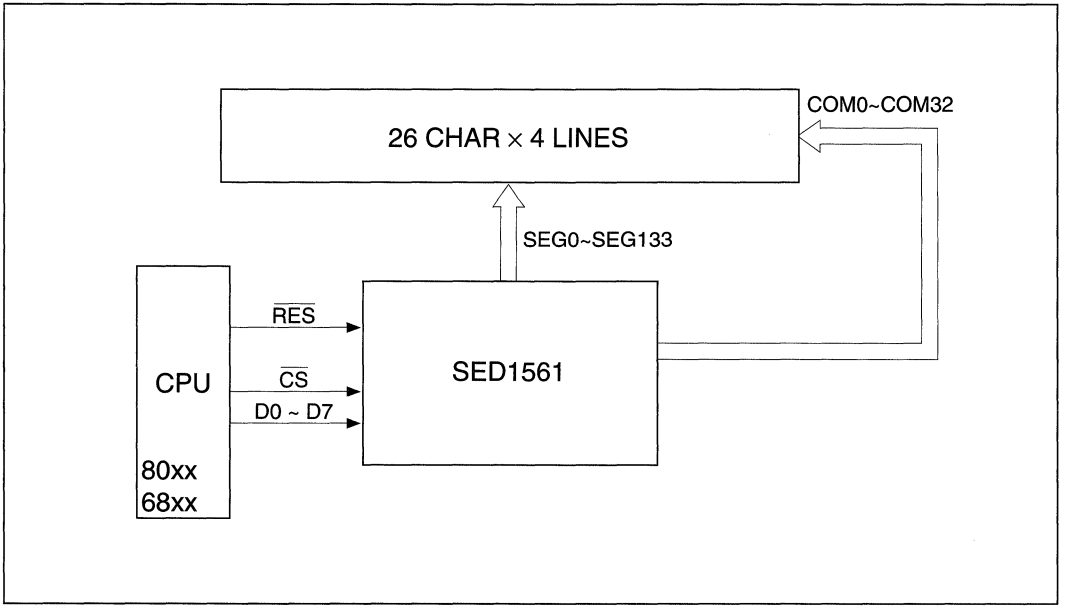
■ FEATURES

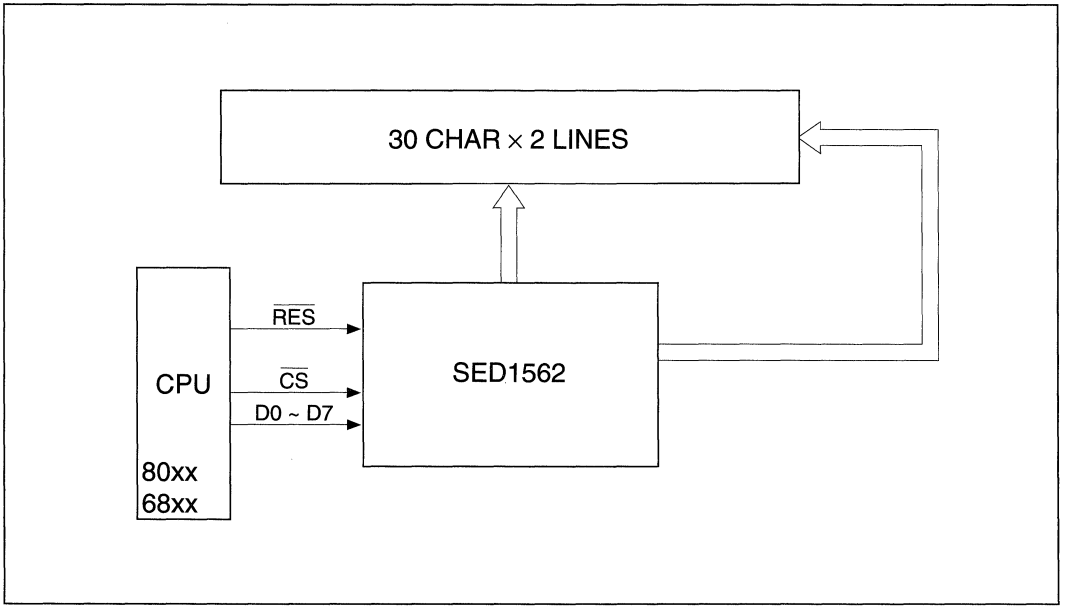
- Low-power operation: 8 µA @ 1 kHz, 6V LCD
- 350 µA current consumption during CPU access @ 200 kHz
- Direct interface to both 80XX and 68XX, 5 MHz, zero wait-state
- On-chip display data RAM (166 × 65 bits)
- On-chip DC/DC converter for LCD voltage
- On-chip voltage regulator and low-power voltage follower
- –.17% / °C temperature gradient
- On-chip oscillator with external resistor
- 32 levels of contrast adjustment by software
- Supports master/slave operation
- Selectable output configuration
- 2.4V to 6.0V supply voltage
- 3.5V to 16V LCD voltage
- Package: TAB ..... (TOB — 2-sided)
  (TQA — 4-sided)

■ SYSTEM BLOCK DIAGRAMS

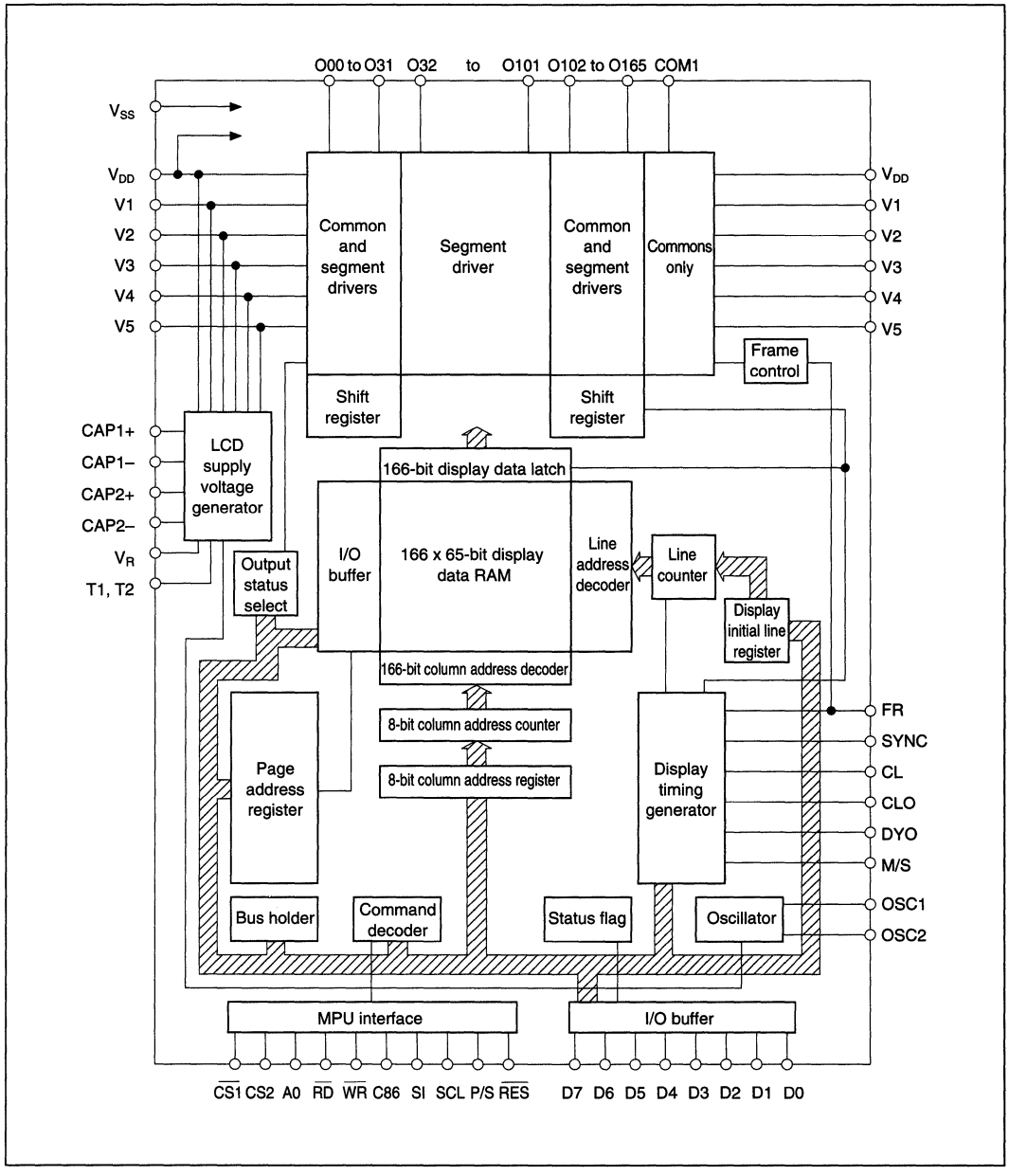


■ SYSTEM BLOCK DIAGRAMS (continued)





■ BLOCK DIAGRAM



■ PIN DESCRIPTION

● Power Supply

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>2</td><td>Supply</td><td>VDD</td><td>Common to MPU power supply pin VCC</td></tr>
<tr><td>2</td><td>Supply</td><td>VSS</td><td>Ground</td></tr>
<tr><td>11</td><td>Supply LCD voltage</td><td>V1 to V5</td><td>LCD driver supply voltages. The voltage determined by the LCD cell is impedance-converted by a resistive divider or an operational amplifier for application. Voltage levels are based on VDD. The voltages must satisfy the following relationship:
VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5
Master mode select: bias voltages are generated on-chip.
<table>
<tr><th></th><th>SED1560</th><th>SED1561</th><th>SED1562</th></tr>
<tr><td>V1</td><td>1/9 V5</td><td>1/7 V5</td><td>1/5 V5</td></tr>
<tr><td>V2</td><td>2/9 V5</td><td>2/7 V5</td><td>2/5 V5</td></tr>
<tr><td>V3</td><td>7/9 V5</td><td>5/7 V5</td><td>3/5 V5</td></tr>
<tr><td>V4</td><td>8/9 V5</td><td>6/7 V5</td><td>4/5 V5</td></tr>
</table>
</td></tr>
</table>

● LCD Driver Power Supplies

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>O</td><td>CAP1+</td><td>DC/DC voltage converter capacitor 1 positive connection</td></tr>
<tr><td>1</td><td>O</td><td>CAP1–</td><td>DC/DC voltage converter capacitor 1 negative connection</td></tr>
<tr><td>1</td><td>O</td><td>CAP2+</td><td>DC/DC voltage converter capacitor 2 positive connection</td></tr>
<tr><td>1</td><td>O</td><td>CAP2–</td><td>DC/DC voltage converter capacitor 2 negative connection</td></tr>
<tr><td>1</td><td>O</td><td>VOUT</td><td>DC/DC voltage converter output</td></tr>
<tr><td>1</td><td>I</td><td>VR</td><td>Voltage adjustment pin. Applies voltage between VDD and V5 using a resistive divider.</td></tr>
<tr><td>2</td><td>I</td><td>T1, T2</td><td>Liquid crystal power control terminals
<table>
<tr><th>T1</th><th>T2</th><th>Boosting Circuit</th><th>Voltage Regulation Circuit</th><th>V/F Circuit</th></tr>
<tr><td>L</td><td>L</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>L</td><td>H</td><td>Valid</td><td>Valid</td><td>Valid*</td></tr>
<tr><td>H</td><td>L</td><td>Invalid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>H</td><td>H</td><td>Invalid</td><td>Invalid</td><td>Valid</td></tr>
</table>
Note: * V/F circuit current capacity enhancement</td></tr>
</table>

● Microprocessor Interface

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>8</td><td>I/O</td><td>D0 to D7</td><td>Data is transferred between the controller and MPU via these pins</td></tr>
<tr><td>1</td><td>I</td><td>A0</td><td>Control/display data flag input. This is connected to the LSB of the microprocessor address bus.
• When LOW, the data on D0 to D7 is command data
• When HIGH, the data on D0 to D7 is display data</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RES}$</td><td>Reset input. Setting this pin low initializes the SED156X.</td></tr>
<tr><td>2</td><td>I</td><td>$\overline{CS1}$,
CS2</td><td>Chip select inputs. Data input/output is enabled when CS1 is LOW and CS2 is HIGH.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RD}$</td><td>Read enable input. See note 1.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{WR}$</td><td>Write enable input. See note 2.</td></tr>
<tr><td>1</td><td>I</td><td>C86</td><td>Microprocessor interface select input.
• LOW when interfacing to 8080-series
• HIGH when interfacing to 6800-series</td></tr>
<tr><td>1</td><td>I</td><td>SI</td><td>Serial data input</td></tr>
<tr><td>1</td><td>I</td><td>SCL</td><td>Serial clock input. Data is read on the rising edge of SCL and converted to 8-bit parallel data.</td></tr>
<tr><td>1</td><td>I</td><td>P/S</td><td>Parallel/serial data input select
<table>
<tr><th>P/S</th><th>Operating Mode</th><th>Chip Select</th><th>Data/ com-mand</th><th>Data I/O</th><th>Read/ write</th><th>Serial Clock</th></tr>
<tr><td>HIGH</td><td>Parallel</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>D0 to D7</td><td>RD, WR</td><td>—</td></tr>
<tr><td>LOW</td><td>Serial</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr>
</table>
In serial mode, data cannot be read from the RAM, and D0 to D7, HZ, $\overline{RD}$ and $\overline{WR}$ must be HIGH or LOW. In parallel mode, SI and SCL must be HIGH or LOW.</td></tr>
</table>

Notes:

1. When interfacing to 8080-series microprocessors, $\overline{RD}$ is active-LOW. When interfacing to 6800-series microprocessors, they are active-HIGH.
2. When interfacing to 8080-series microprocessors, $\overline{WR}$ is active-LOW. When interfacing to 6800-series microprocessors, read mode is selected when $\overline{WR}$ is HIGH, and write mode is selected when $\overline{WR}$ is LOW.

● Oscillator and Display Timing Control

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>2</td><td>I</td><td>OSC1</td><td>Using internal oscillator when M/S = "H", connect resistor Rf to the OSC1 and OSC2 pins. The OSC2 pin is used for output of the oscillator amplifier.</td></tr>
<tr><td>2</td><td>I/O</td><td>OSC2</td><td>When M/S = "L": the OSC2 pin is used for input of oscillation signal. The OSC1 pin should be left open. Fix the CL pin to the VSS level when using the internal oscillator circuit as the display clock.</td></tr>
<tr><td>1</td><td>I</td><td>CL</td><td>Display clock input. The line counter increments on the rising edge of CL, and the display pattern is output on the falling edge. When using the external display clock, OSC1 = "H", OSC2 = "L", and reset this LSI by $\overline{RES}$ pin.</td></tr>
<tr><td>1</td><td>O</td><td>CLO</td><td>Display clock output. When using the internal oscillator, the clock signal is output on this pin. Connect CLO to YSCL on the common driver.</td></tr>
<tr><td>1</td><td>I</td><td>M/S</td><td>Master/slave select input. Master produces signals for display, and slave receives them. This is for display synchronization.
<table>
<tr><th>Device</th><th>M/S</th><th>Operating Mode</th><th>Internal Oscillator</th><th>Power Supply</th><th>FR</th><th>SYNC</th><th>OSC1</th><th>OSC2</th><th>DYO</th></tr>
<tr><td rowspan="2">156X</td><td>LOW</td><td>Slave</td><td>OFF</td><td>OFF</td><td>I</td><td>I</td><td>Open</td><td>I</td><td>O</td></tr>
<tr><td>HIGH</td><td>Master</td><td>ON</td><td>ON</td><td>O</td><td>O</td><td>I</td><td>O</td><td>O</td></tr>
</table>
Note: I = input mode O = output mode</td></tr>
<tr><td>1</td><td>I/O</td><td>FR</td><td>LCD AC drive signal input/output. Output is selected when M/S is HIGH, and input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>I/O</td><td>SYNC</td><td>Display sync input/output. Output is selected when M/S is HIGH, and input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>O</td><td>DYO</td><td>Start-up output for common driver. Connect to DIO of the common driver, such as the SED1630.</td></tr>
</table>

* SED1630 has a DIO input.

● LCD Driver Outputs

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>166</td><td>O</td><td>O0 to
O165</td><td>LCD driver outputs. O0 to O31 and O102 to O165 are selectable segment or common outputs, determined by a selection command. O32 to O101 are segment outputs only.
For segment outputs, the ON voltage level is given as shown in the following table:
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">LCD ON Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverse Display</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V3</td><td>V5</td></tr>
<tr><td>HIGH</td><td>V2</td><td>VDD</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V5</td><td>V3</td></tr>
<tr><td>HIGH</td><td>VDD</td><td>V2</td></tr>
</table>
For common outputs, the ON voltage is given as shown in the following table:
<table>
<tr><th>Scan Data</th><th>FR</th><th>LCD ON Voltage</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V4</td></tr>
<tr><td>HIGH</td><td>V1</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>VDD</td></tr>
<tr><td>HIGH</td><td>V5</td></tr>
</table></td></tr>
<tr><td>1</td><td>O</td><td>COM1</td><td>LCD driver common output. Common outputs when the “DUTY + 1” command is executed are as follows:
<table>
<tr><th>Device</th><th>“DUTY + 1” ON</th><th>“DUTY + 1” OFF</th></tr>
<tr><td>SED1560</td><td>COM64, COM48</td><td>V1 or V4</td></tr>
<tr><td>SED1561</td><td>COM32, COM24</td><td>V1 or V4</td></tr>
<tr><td>SED1562</td><td>COM16</td><td>V1 or V4</td></tr>
</table>
Common output special for the indicator.</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{SS}	–7.0 to 0.03	V
		–6.0 to 0.3 (when triple voltage conversion)	
Driver supply voltage range (1)	V5	–18.0 to 0.3	V
Driver supply voltage range (2)	V1, V2, V3, V4	V5 to 0.3	V
Input voltage range	V_{IN}	V_{SS} – 0.3 to 0.3	V
Output voltage range	V0	V_{SS} – 0.3 to 0.3	V
Operating temperature range	T_{opr}	–30 to 85	°C
Storage temperature range (TCP)	T_{str}	–55 to 125	°C

Notes:

1. The voltages shown are based on V_{DD} = 0V.
2. Always keep the condition $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ for voltages V1, V2, V3 and V4.
3. If devices are used over the absolute maximum rating, the LSIs may be destroyed permanently. It is desirable to use them under the electrical characteristic conditions for general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.
4. For operating temperatures below –30°C, please consult an S-MOS engineer.

■ DC CHARACTERISTICS

V_{DD} = 0V, V_{SS} = –5 ± 10%, T_a = –30 to +85°C unless otherwise noted.

Parameter		Symbol	Condition		Min	Typ	Max	Unit	Pin
Power voltage (1)	Recommended operation	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Operational				–6.0	—	–2.4		V_{SS} *1
Operating voltage (2)	Operational	V5			–16.0	—	–3.5	V	V5 *2
	Operational	V1, V2			0.4 × V5	—	V_{DD}	V	V1, V2
	Operational	V3, V4			V5	—	0.6 × V5	V	V3, V4
High-level input voltage		V_{IHC1}			0.3 × V_{SS}	—	V_{DD}	V	*3
		V_{IHC2}			0.15 × V_{SS}	—	V_{DD}	V	*4
		V_{IHC1}	V_{SS} = –2.7V		0.2 × V_{SS}	—	V_{DD}	V	*3
		V_{IHC2}	V_{SS} = –2.7V		0.15 × V_{SS}	—	V_{DD}	V	*4
Low-level input voltage		V_{ILC1}			V_{SS}	—	0.7 × V_{SS}	V	*3
		V_{ILC2}			V_{SS}	—	0.85 × V_{SS}	V	*4
		V_{ILC1}	V_{SS} = –2.7V		V_{SS}	—	0.8 × V_{SS}	V	*3
		V_{ILC2}	V_{SS} = –2.7V		V_{SS}	—	0.85 × V_{SS}	V	*4
High-level output voltage		V_{OHC1}		I_{OH} = –1 mA	0.2 × V_{SS}	—	V_{DD}	V	*5
		V_{OHC2}		I_{OH} = –120 µA	0.2 × V_{SS}	—	V_{DD}	V	OSC2
		V_{OHC1}	V_{SS} = –2.7V	I_{OH} = –0.5 mA	0.2 × V_{SS}	—	V_{DD}	V	*5
		V_{OHC2}	V_{SS} = –2.7V	I_{OH} = –50 µA	0.2 × V_{SS}	—	V_{DD}	V	OSC2
Low-level output voltage		V_{OLC1}		I_{OL} = 1 mA	V_{SS}	—	0.8 × V_{SS}	V	*5
		V_{OLC2}		I_{OL} = 120 µA	V_{SS}	—	0.8 × V_{SS}	V	OSC2
		V_{OLC1}	V_{SS} = –2.7V	I_{OL} = 0.5 mA	V_{SS}	—	0.8 × V_{SS}	V	*5
		V_{OLC2}	V_{SS} = –2.7V	I_{OL} = 50 µA	V_{SS}	—	0.8 × V_{SS}	V	OSC2
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	—	1.0	µA	*6
Output leakage current		I_{LO}			–3.0	—	3.0	µA	*7
LCD driver ON resistance		R_{ON}	T_a = 25°C	V5 = –14.0V	—	2.0	3.0	kΩ	O0 ~ O166
				V5 = –8.0V	—	3.0	4.5	kΩ	*8
Static power consumption		I_{SSQ}			—	0.00	5.0	µA	V_{SS}
		I_{SQ}	V5 = –18.0V		—	0.01	15.0	µA	V5
Input terminal capacity		C_{IN}	T_a = 25°C	f = 1 MHz	—	5.0	8.0	pF	*3 *4
Oscillator frequency		f_{OSC}	R_f = 1MΩ±2%	V_{SS} = –5V	15	18	22	kHz	*9
				V_{SS} = –2.7V	11	16	21		

Reset time	t_R		1.0	—	—	µs	*10
Reset "L" pulse width	t_{RW}		10	—	—	µs	*11

Built-in power circuit	Input voltage	V_{SS}		–6.0	—	–2.4	V	*12
	Amplified output voltage	V_{OUT}	If amplified 3 times	–18.0	—	—	V	V_{OUT}
	Voltage regulator circuit operation voltage	V_{OUT}		–18.0	—	–6.0	V	V_{OUT}
	Voltage follower operation voltage	V5 ①	Supplied to SED1560	–16.0	—	–6.0	V	*13
		V5 ②	Supplied to SED1561	–16.0	—	–5.0	V	
		V5 ③	Supplied to SED1562	–16.0	—	–4.5	V	
	Reference voltage	V_{REG}	Ta = 25°C	–2.35	–2.5	–2.65	V	

Notes: * See Notes below.

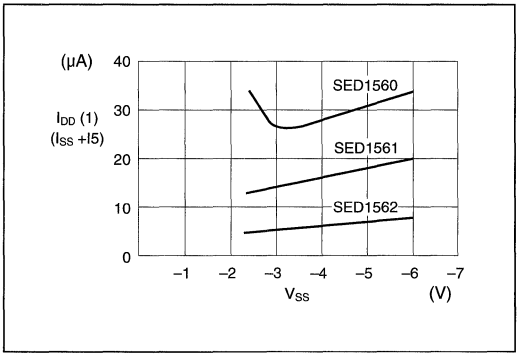
● **When dynamic current consumption (I) is displayed; the built-in power supply is on and T1 = T2 = Low**

Test conditions, unless otherwise specified: V_{DD} = 0V, V_{SS} = –5V ±10%, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remarks
SED1560	I_{DD} (1)	V5 = –12.5V; 3 times amplified	—	169	340	µA	*16
SED1561		V5 = –8.0V; 3 times amplified	—	124	250	µA	
SED1562		V5 = –6.0V; 2 times amplified	—	53	110	µA	
		V_{SS} = –2.7V; 3 times amplified V5 = –6.0V	—	66	130	µA	

● **Typical current consumption characteristics**

○ **Dynamic current consumption (I), if an external clock and an external power supply are used**



Conditions: The built-in power supply is off but the external one is used.

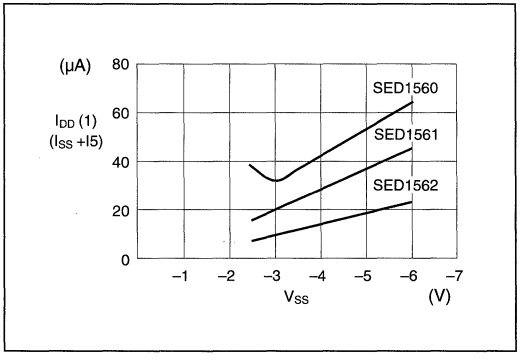
SED1560	V5	=	–12.5V
SED1561	V5	=	–8.0V
SED1562	V5	=	–6.0V

External clock:

SED1560	f_{CL}	=	4 kHz
SED1561	f_{CL}	=	2 kHz
SED1562	f_{CL}	=	1 kHz

Remarks: *14

○ **Dynamic current consumption (I), if the built-in oscillator and the external power supply are used**



Conditions: The built-in power supply is off but the external one is used.

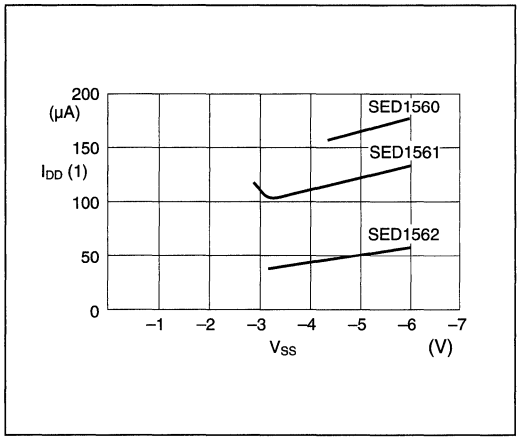
SED1560	V5	=	–12.5V
SED1561	V5	=	–8.0V
SED1562	V5	=	–6.0V

Internal oscillation:

SED1560	R_f	=	1 MΩ
SED1561	R_f	=	1 MΩ
SED1562	R_f	=	1 MΩ

Remarks: *15

○ **Dynamic current consumption (I), if the built-in power supply is used.**



Conditions: The built-in power supply is on and T1 = T2 = Low.

SED1560 V5 = –12.5V; 3 times amplified

SED1561 V5 = –8.0V; 3 times amplified

SED1562 V5 = –6.0V; 2 times amplified

Internal oscillation:

SED1560 Rf = 1 MΩ
SED1561 Rf = 1 MΩ
SED1562 Rf = 1 MΩ

Remarks: *16

Notes:

*1. Although the wide range of operating voltage is guaranteed, a spike voltage change during access to the MPU is not guaranteed.

*2. The operating voltage range of the VSS and V5 systems. The operating voltage range is applied if an external power supply is used.

*3. Pins A0, D0 to D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, SYNC, M/S, C86, SI, P/S, T1 AND T2.

*4. Pins CL, SCL, and $\overline{RES}$.

*5. Pins D0 to D7, FR, SYNC, CL0, and DY0

*6. Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CL, M/S, $\overline{RES}$, C86, SI, SCL, P/S, T1, and T2.

*7. Applied if pins D0 to D7, FR, and SYNC are high impedance.

*8. The resistance when the 0.1 -volt voltage is applied between the "On" output terminal and each power terminal (V1, V2, V3 or V4). It must be within the operating voltage (2).

*9. The relationship between the oscillation frequency, frame and Rf value.

10. "tr" (reset time) indicates the period between the time when the $\overline{RES}$ signal rises and when the internal circuit has been reset. Therefore, the SED156 is usually operable after "tr" time.

*11. Specifies the minimum pulse width of $\overline{RES}$ signal. The Low pulse greater than "tRW" must be entered for reset.

*12. If the voltage is amplified three times by the built-in power circuit, the primary power VSS must be used within the input voltage range.

*13. The V5 voltage can be adjusted within the voltage follower operating range by the voltage regulator circuit.

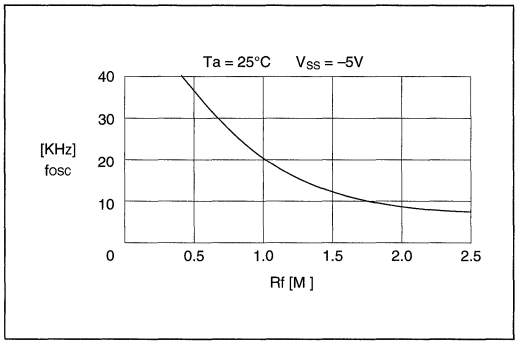
*14, 15, 16. Indicates the current consumed by the separate IC. The current consumption due to the LCD panel capacity and wiring capacity is not included.

The current consumption is shown if the checker is used, the display is turned on, the output status of Case 6 is selected, and the SED1560 is set to 1/64 duty, the SED1561 is set to 1/32 duty, and the SED1562 is set to 1/64 duty.

*14. Applied if an external clock is used and if not accessed by the MPU.

*15. Applied if the built-in oscillation circuit is used and if not accessed by the MPU.

*16. Applied if the built-in oscillation circuit and the built-in power circuit are used (T1 = T2 = Low) and if not accessed by the MPU.

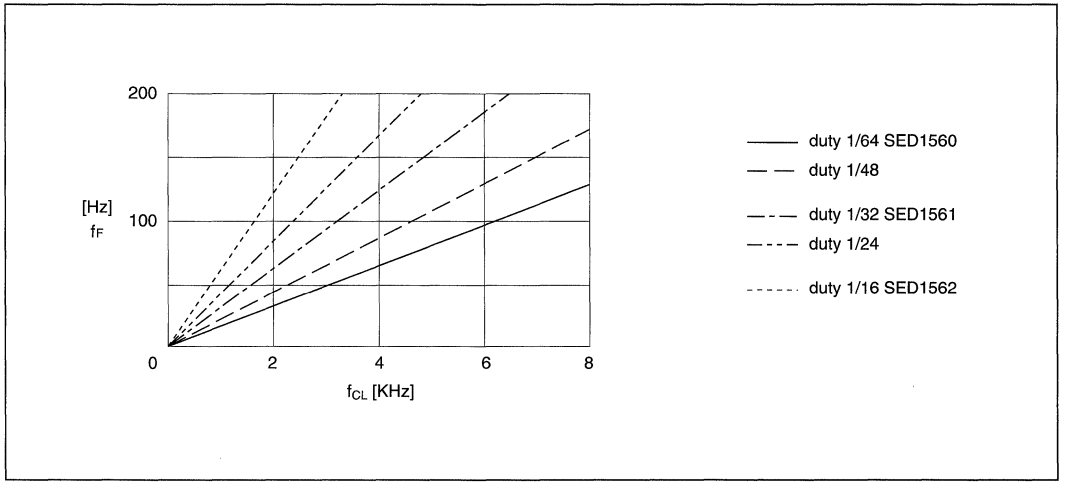


Oscillator frequency vs. frame vs. Rf
[SED156X]

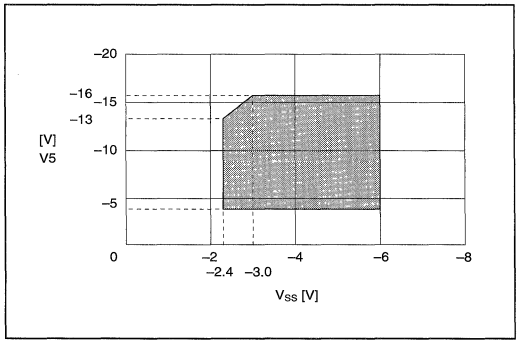
The relationship between oscillator frequency fosc and LCD frame frequency fF is obtained from the following expression:

Device	Duty	fF
SED1560	1/64	fosc/256
	1/48	fosc/192
SED1561	1/32	fosc/256
	1/24	fosc/192
SED1562	1/16	fosc/256

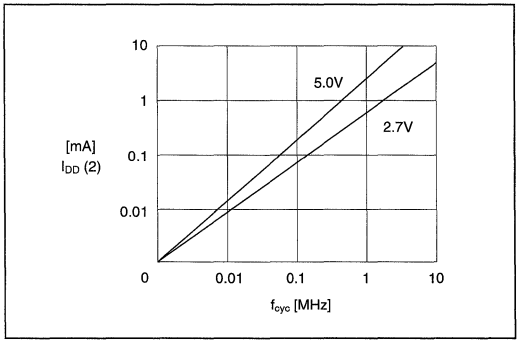
(fF indicates not fF signal cycle but cycle of LCD AC.)



External clock (fCL) vs. frame frequency [SED156X]



Operating voltage range for VSS and V5

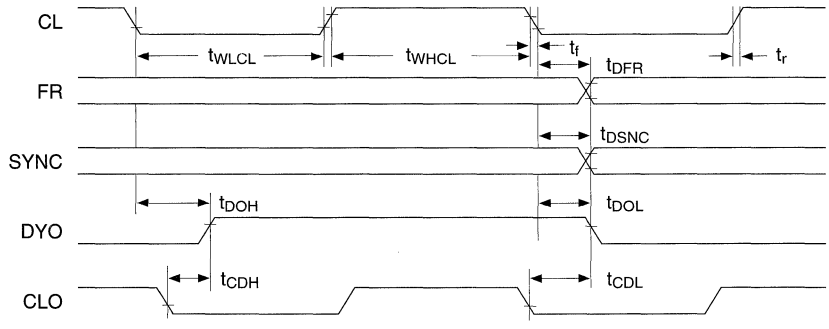


Power consumption during CPU access cycle
(IDD [2])

■ RESET

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reset time	t_R	t_R is measured from the rising edge of $\overline{RES}$. The SED156X resumes normal operating mode after a reset.	1.0	—	—	µs
Reset LOW-level pulsewidth	t_{RW}		1.0	—	—	µs

■ DISPLAY CONTROL TIMING



● Display Control Input Timing

V_{SS} = –5.5 to –4.5V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	t_r		—	30	—	ns
CL fall time	t_f		—	30	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

V_{SS} = –4.5 to –2.7V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	t_r		—	40	—	ns
CL fall time	t_f		—	40	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

Notes: 1. Effective only when the SED156X is in the master mode.

2. The FR/SYNC delay time input timing is provided in the slave operation.
   The FR/SYNC delay time output timing is provided in the master operation.

3. Each timing is based on 20% and 80% of V_{SS}.

- **Display Control Output Timing**

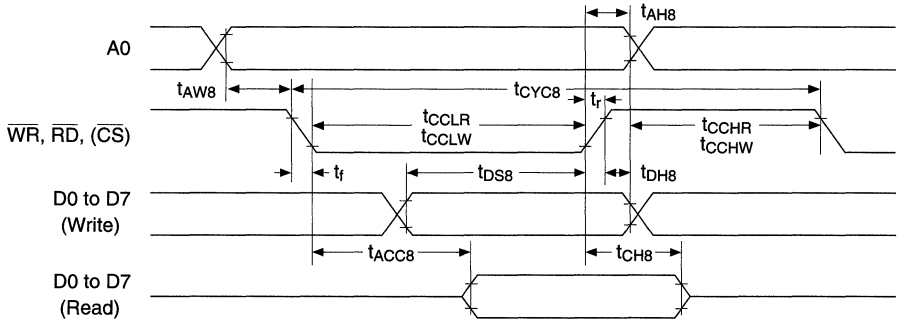
V_{SS} = –5.5 to –4.5V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
FR delay time	t_{DFR}	C_L = 50 pF	—	60	150	ns
SYNC delay time	t_{DSNC}	C_L = 100 pF	—	60	150	ns
DYO LOW-level delay time	t_{DOL}		—	70	160	ns
DYO HIGH-level delay time	t_{DOH}		—	70	160	ns
CLO to DYO LOW-level delay time	t_{CDL}	SED156X operating in master mode only	—	40	100	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156X operating in master mode only	—	40	100	ns

V_{SS} = –4.5 to –2.7V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
FR delay time	t_{DFR}	C_L = 50 pF	—	120	240	ns
SYNC delay time	t_{DSNC}	C_L = 100 pF	—	120	240	ns
DYO LOW-level delay time	t_{DOL}		—	140	250	ns
DYO HIGH-level delay time	t_{DOH}		—	140	250	ns
CLO to DYO LOW-level delay time	t_{CDL}	SED156X operating in master mode only	—	100	200	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156X operating in master mode only	—	100	200	ns

- **System Buses: Read/Write Characteristics I (80-Series MPU)**



V_{SS} = –5.0 ± 10%, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		10	—	ns
Address setup time		t_{AW8}		10	—	ns
System cycle time		t_{CYC8}		200	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		22	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		77	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		172	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		117	—	ns
Data setup time		t_{DS8}		20	—	ns
Data hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	70	ns
Output disable time		t_{CH8}		10	50	ns
Input signal change time		t_r, t_f		—	15	ns

V_{SS} = –2.7 to –4.5V, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		25	—	ns
Address setup time		t_{AW8}		25	—	ns
System cycle time		t_{CYC8}		450	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		44	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		194	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		394	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		244	—	ns
Data setup time		t_{DS8}		40	—	ns
Data hold time		t_{DH8}		20	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	140	ns
Output disable time		t_{CH8}		10	100	ns
Input signal change time		t_r, t_f		—	15	ns

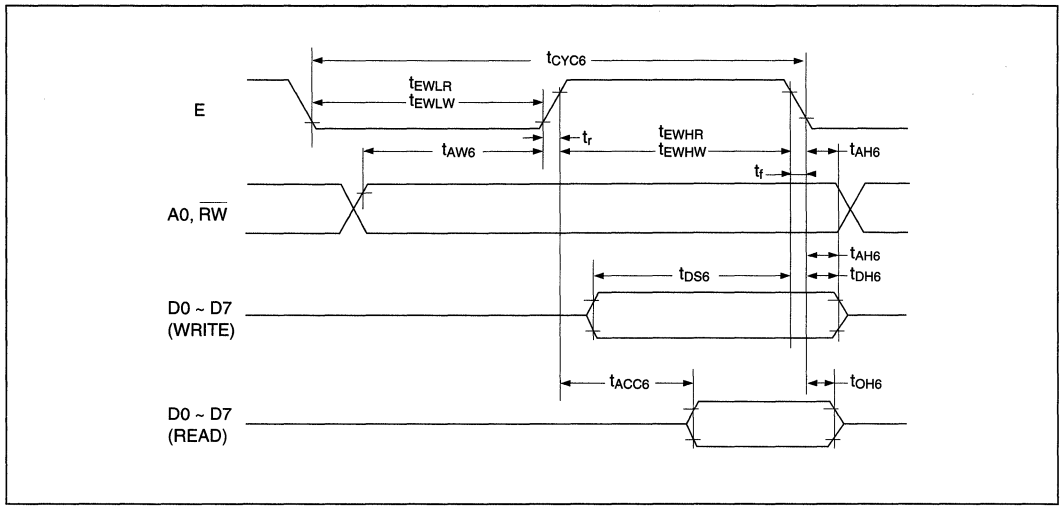
Notes:

1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$
2. All signal timings are limited based on 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while $\overline{CS}$ ($\overline{CS1}$ and CS2) is active and the $\overline{RD}$ or $\overline{WR}$ signal is in the low level.

   If read/write operation is performed by the $\overline{RD}$ or $\overline{WR}$ signal while $\overline{CS}$ is active, it is determined by the $\overline{RD}$ or $\overline{WR}$ signal timing.

   If read/write operation is performed by $\overline{CS}$ while the $\overline{RD}$ or $\overline{WR}$ signal is in the low level, it is determined by the $\overline{CS}$ active timing.

- **System Buses: Read/Write Characteristics II (68-Series MPU)**



V_{SS} = –5.0V ± 10%, T_a = –30 to 85°C

Parameter		Signal	Symbol	Condition	Min	Max	Unit
System cycle time			t_{CYC6}		200	—	ns
Address setup time		(A0)	t_{AW6}		10	—	ns
Address hold time		R/$\overline{W}$	t_{AH6}		10	—	ns
Data setup time		D0 ~ D7	t_{DS6}		20	—	ns
Data hold time			t_{DH6}		10	—	ns
Output disable time			t_{OH6}	CL = 100pF	10	50	ns
Access time			t_{ACC6}		—	70	ns
Enable H pulse width	READ	E	t_{EWHR}		77	—	ns
	WRITE		t_{EWHW}		22	—	ns
Enable L pulse width	READ	E	t_{EWLR}		117	—	ns
	WRITE		t_{EWLW}		172	—	ns
Input signal change time			t_r, t_f		—	15	ns

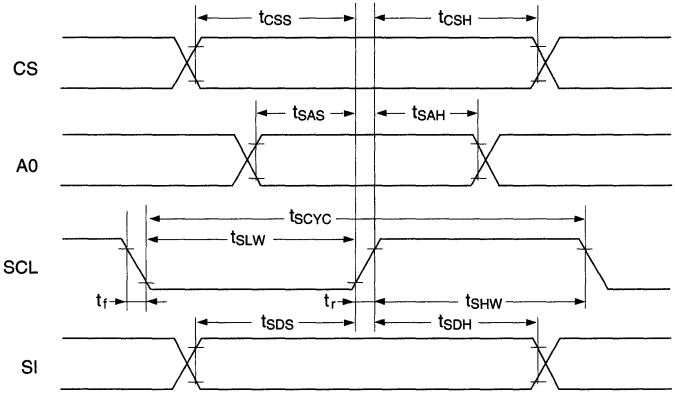
V_{SS} = –5.0V ± 10%, T_a = –30 to 85°C

Parameter		Signal	Symbol	Condition	Min	Max	Unit
System cycle time		A0, $\overline{CS}$	t_{CYC6}		450	—	ns
Address setup time		($\overline{CS1}$, CS2)	t_{AW6}		25	—	ns
Address hold time		R/$\overline{W}$	t_{AH6}		25	—	ns
Data setup time		D0 ~ D7	t_{DS6}		40	—	ns
Data hold time			t_{DH6}		20	—	ns
Output disable time			t_{OH6}	CL = 100pF	20	100	ns
Access time			t_{ACC5}		—	140	ns
Enable H pulse width	READ	E	t_{EWHR}		154	—	ns
	WRITE		t_{EWHW}		44	—	ns
Enable L pulse width	READ	E	t_{EWLR}		244	—	ns
	WRITE		t_{EWLW}		394	—	ns
Input signal change time			t_r, t_f		—	15	ns

Notes: 1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $t_r + t_f \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$

2. All signal timings are limited based on 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while $\overline{CS}$ ($\overline{CS1}$ and CS2) is active and the E signal is in the high level.
   If read/write operation is performed by the E signal while $\overline{CS}$ is active, it is determined by the E signal timing.
   If read/write operation is performed by $\overline{CS}$ while the E signal is in the high level, it is determined by the $\overline{CS}$ active timing.

● Serial Interface



V_{SS} = –5.0V ± 10%, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Serial clock cycle	SCL	t_{SCYC}		500	—	ns
SCL high pulse width		t_{SHW}		150	—	ns
SCL low pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		120	—	ns
Address hold time		t_{SAH}		200	—	ns
Data setup time	SI	t_{SDS}		120	—	ns
Data hold time		t_{SDH}		50	—	ns
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}		30	—	ns
		t_{CSH}		400	—	ns
Input signal change time		t_r, t_f		—	50	ns

V_{SS} = –5.0V ± 10%, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Serial clock cycle	SCL	t_{SCYC}		1000	—	ns
SCL high pulse width		t_{SHW}		300	—	ns
SCL low pulse width		t_{SLW}		300	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		400	—	ns
Data setup time	SI	t_{SDS}		250	—	ns
Data hold time		t_{SDH}		100	—	ns
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}		60	—	ns
		t_{CSH}		800	—	ns
Input signal change time		t_r, t_f		—	50	ns

Note: *2. All signal timings are limited based on 20% and 80% of V_{SS} voltage.

■ RESET

When power is turned ON, the SED1560 is initialized on the rising edge of $\overline{RES}$. Initial settings are as follows:

1. Display ..... OFF
2. Display mode ..... Normal
3. *n*-line inversion ..... OFF
4. Duty cycle 1/64
5. ADC select ..... Normal
6. Read/write modify ..... OFF
7. On-chip power supply ..... OFF
8. Serial interface register ..... Cleared
9. Display initial line register ..... Line 1
10. Column address counter 0
11. Page address register ..... Page 0
12. Output selection circuit ..... Case 6
13. *n*-line inversion register 16
14. Set the electronic control register to zero (0)

$\overline{RES}$ should be connected to the microprocessor reset terminal so that both devices are reset at the same time. $\overline{RES}$ must be LOW for at least 1 µs to correctly reset the SED1560. Normal operation starts 1 µs after the rising edge on $\overline{RES}$.

If the SED1560 is not properly initialized when power is turned ON, it can lock itself into a state that cannot be cancelled.

When the Reset command is used, only initial settings 9 to 14 are active.

■ COMMANDS

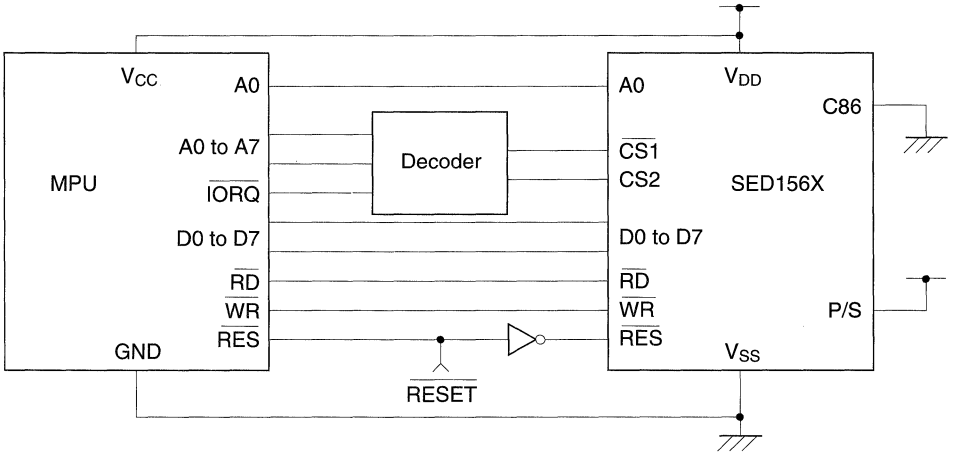
● The Command Set

A0, $\overline{RD}$ and $\overline{WR}$ identify the data bus commands. Interpretation and execution of commands are synchronized to the internal clock. Since a busy check is normally not needed, commands can be processed at high speed. When the serial interface is used, the order of data entry is D7 to D0.

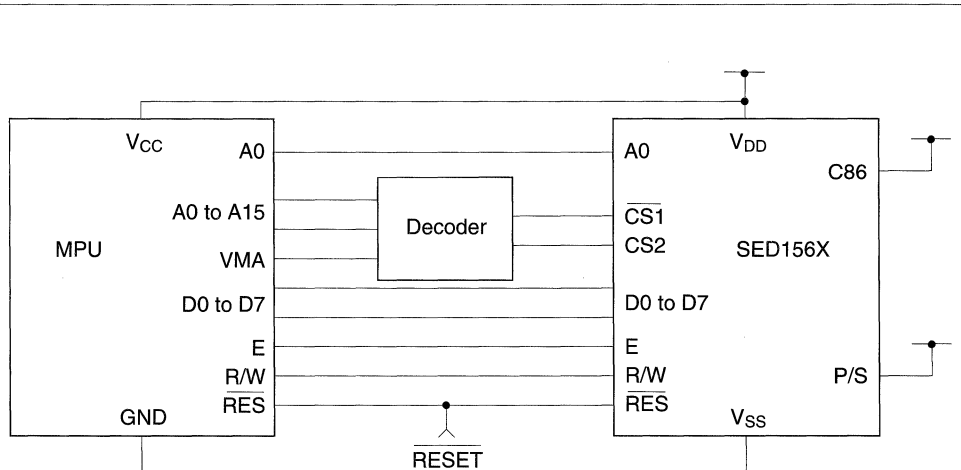
Command	Code											Description
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns the display ON and OFF. 0: OFF 1: ON
Display START Line set	0	1	0	0	1	Display line address						Determines the RAM display line for COM0.
Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM pages in the Page Address register.
Column address set high-order 4 bits	0	1	0	0	0	0	1	High-order column address				Sets the high-order 4 bits of the display RAM column address in the register.
Column address set low-order 4 bits	0	1	0	0	0	0	0	Low-order column address				Sets the low-order 4 bits of the display RAM column address in the register.
Status read	0	0	1	Status				0	0	0	0	Reads the status information.
Display data write	1	1	0	Write data								Writes data in the display RAM.
Display data read	1	0	1	Read data								Reads data from the display RAM.
ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Outputs the display RAM address for SEG. 0: Normal 1: Reversed
Normal/reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Display the LCD image in normal or reverse mode. 0: Normal 1: Reversed
All indicator ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Lights all indicators. 0: Normal display 1: All ON
Duty select	0	1	0	1	0	1	0	1	0	0	0 1	Sets LCD drive duty (1). 0: 1/24, 48 1: 1/32, 64
Duty + 1	0	1	0	1	0	1	0	1	0	1	0 1	Sets LCD drive duty (2). 0: Normal 1: Duty + 1
n-line reverse register set	0	1	0	0	0	1	1	No. of reversed *n*-lines				Sets the line reverse driving and no. of reverse lines in the line reverse register.
n-line reverse register release	0	1	0	0	0	1	0	0	0	0	0	Releases the line reverse driving.
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments by 1 during write of column address counter, and sets to 0 during read.
End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read Modify write mode.
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset.
Output status register set	0	1	0	1	1	0	0	Output status				Sets the COM and SEG status in registers.
Built-in power supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	0: Power OFF 1: Power ON
Power-on completion	0	1	0	1	1	1	0	1	1	0	1	Completes the turn-on sequence of built-in power supply.
Electronic control register set	0	1	0	1	0	0	Electronic control value					Sets the V5 output voltage in the electronic control register.
Power save												A complex command to turn off the display and light all indicators.

■ MICROPROCESSOR INTERFACE

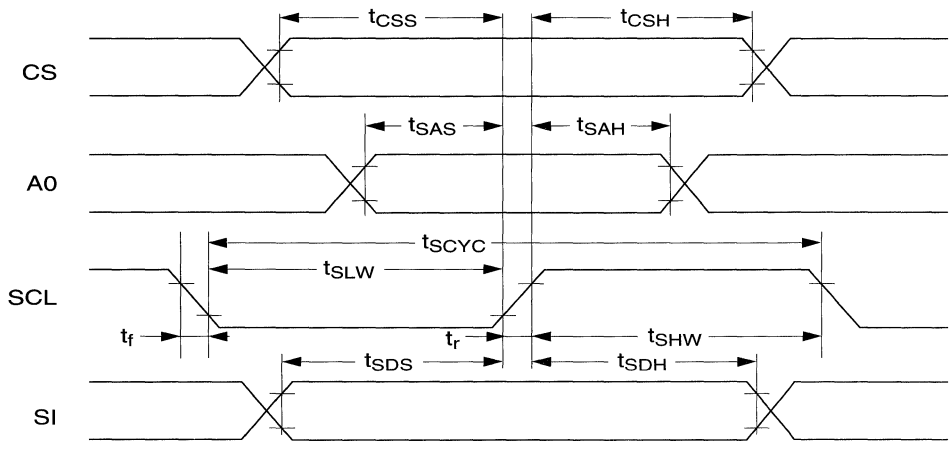
The SED1560 Series communicates with a high-speed microprocessor, such as the Intel 80XX family or the Motorola 68XX family, through 8-bit parallel data transfer. The number of connections to the microprocessor can be minimized by using a serial interface. When used in a multiple-chip configuration, the SED1560 Series is controlled by the chip select signals from the microprocessor.



8080-series microprocessors

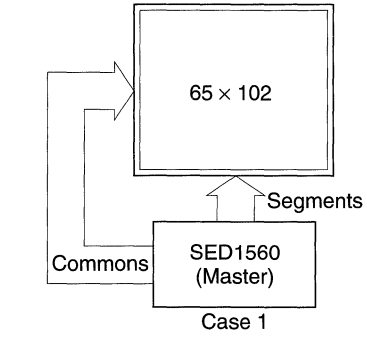


6800-series microprocessors

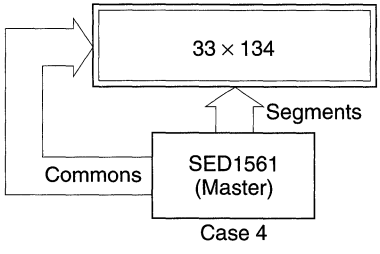


Serial interface

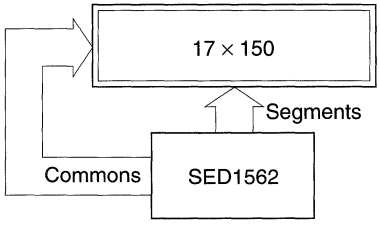
■ LCD PANEL INTERFACE EXAMPLES



Case 1

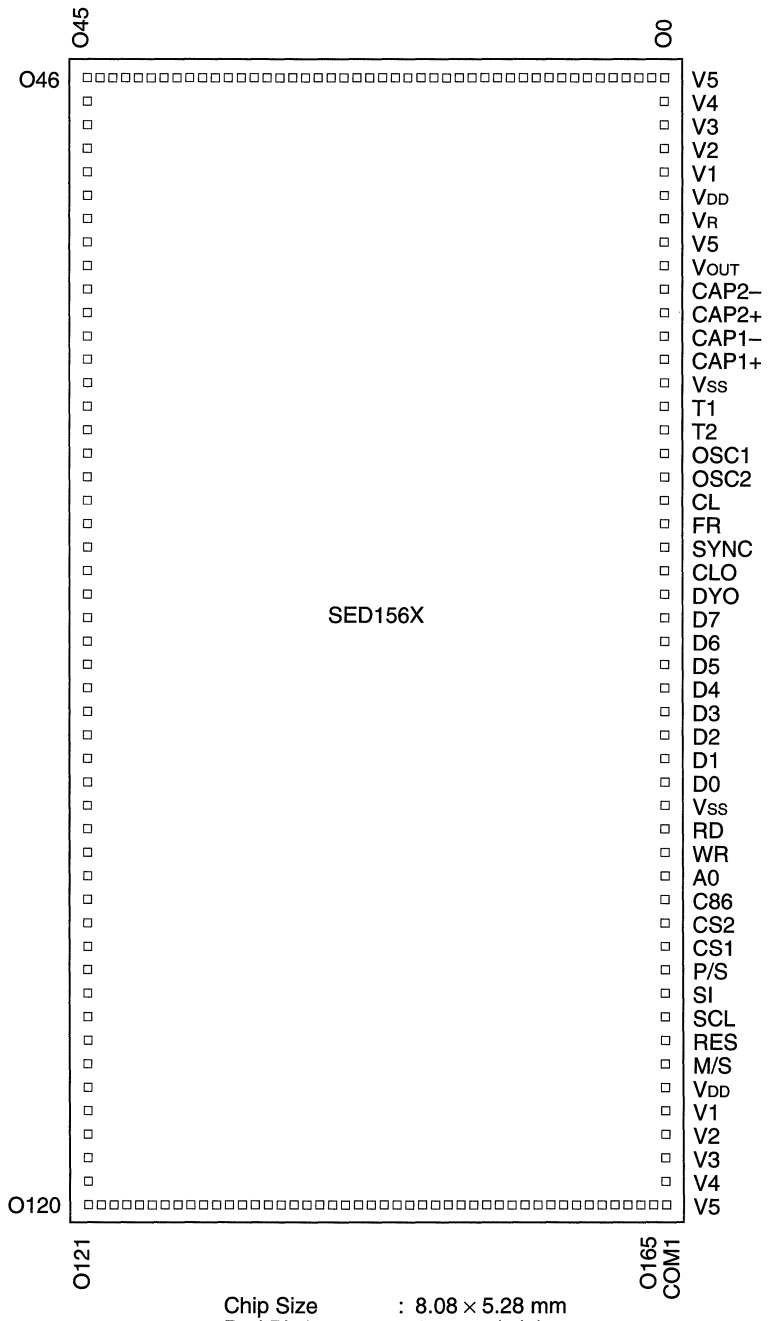


Case 4



Single-chip configurations

■ PAD LAYOUT



Chip Size : 8.08 × 5.28 mm
Pad Pitch : 100 µm (min)
Chip thickness : 625 µm ± 25 µm

● Pad Coordinates

Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	V5	3640	2487
2	V4	3489	2487
3	V3	3339	2487
4	V2	3188	2487
5	V1	3037	2487
6	V_{DD}	2889	2487
7	M/S	2755	2487
8	$\overline{RES}$	2604	2487
9	SCL	2453	2487
10	SI	2302	2487
11	P/S	2151	2487
12	$\overline{CS1}$	2001	2487
13	CS2	1850	2487
14	C86	1699	2487
15	A0	1548	2487
16	$\overline{WR}$	1397	2487
17	$\overline{RD}$	1247	2487
18	V_{SS}	1077	2487
19	D0	945	2487
20	D1	794	2487
21	D2	643	2487
22	D3	493	2487
23	D4	342	2487
24	D5	191	2487
25	D6	40	2487
26	D7	–111	2487
27	DYO	–261	2487
28	CLO	–412	2487
29	SYNC	–563	2487
30	FR	–714	2487
31	CL	–865	2487
32	OSC2	–1015	2487
33	OSC1	–1166	2487
34	T2	–1317	2487
35	T1	–1468	2487
36	VSS	–1638	2487
37	CAP1+	–1789	2487
38	CAP1–	–1939	2487
39	CAP2+	–2090	2487
40	CAP2–	–2241	2487
41	V_{OUT}	–2392	2487
42	V5	–2543	2487
43	VR	–2674	2487
44	V_{DD}	–2844	2487
45	V1	–2995	2487
46	V2	–3146	2487
47	V3	–3297	2487
48	V4	–3447	2487
49	V5	–3598	2487
50	O0	–3887	2294
51	O1	–3887	2194
52	O2	–3887	2094
53	O3	–3887	1994
54	O4	–3887	1894
55	O5	–3887	1794
56	O6	–3887	1694
57	O7	–3887	1594
58	O8	–3887	1494
59	O9	–3887	1394
60	O10	–3887	1294
61	O11	–3887	1194
62	O12	–3887	1094
63	O13	–3887	994
64	O14	–3887	894
65	O15	–3887	794
66	O16	–3887	694
67	O17	–3887	594
68	O18	–3887	494
69	O19	–3887	394
70	O20	–3887	294
71	O21	–3887	194
72	O22	–3887	94
73	O23	–3887	–6
74	O24	–3887	–106
75	O25	–3887	–206
76	O26	–3887	–306
77	O27	–3887	–406
78	O28	–3887	–506
79	O29	–3887	–606
80	O30	–3887	–706
81	O31	–3887	–806
82	O32	–3887	–906
83	O33	–3887	–1006
84	O34	–3887	–1106
85	O35	–3887	–1206
86	O36	–3887	–1306
87	O37	–3887	–1406
88	O38	–3887	–1506
89	O39	–3887	–1606
90	O40	–3887	–1706
91	O41	–3887	–1806
92	O42	–3887	–1906
93	O43	–3887	–2006
94	O44	–3887	–2106
95	O45	–3887	–2206
96	O46	–3711	–2487
97	O47	–3611	–2487
98	O48	–3511	–2487
99	O49	–3411	–2487
100	O50	–3311	–2487
101	O51	–3211	–2487
102	O52	–3111	–2487
103	O53	–3011	–2487
104	O54	–2911	–2487
105	O55	–2811	–2487
106	O56	–2711	–2487
107	O57	–2611	–2487
108	O58	–2511	–2487
109	O59	–2411	–2487
110	O60	–2311	–2487
111	O61	–2211	–2487
112	O62	–2111	–2487
113	O63	–2011	–2487
114	O64	–1911	–2487
115	O65	–1811	–2487
116	O66	–1711	–2487
117	O67	–1611	–2487
118	O68	–1511	–2487
119	O69	–1411	–2487
120	O70	–1311	–2487
121	O71	–1211	–2487
122	O72	–1111	–2487
123	O73	–1011	–2487
124	O74	–911	–2487
125	O75	–811	–2487
126	O76	–711	–2487
127	O77	–611	–2487
128	O78	–511	–2487
129	O79	–411	–2487
130	O80	–311	–2487
131	O81	–211	–2487
132	O82	–111	–2487
133	O83	–11	–2487
134	O84	89	–2487
135	O85	189	–2487
136	O86	289	–2487
137	O87	389	–2487
138	O88	489	–2487
139	O89	589	–2487
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141	O91	789	–2487
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161	O111	2789	–2487
162	O112	2889	–2487
163	O113	2989	–2487
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165	O115	3189	–2487
166	O116	3289	–2487
167	O117	3389	–2487
168	O118	3489	–2487
169	O119	3589	–2487
170	O120	3689	–2487
171	O121	3887	–2206
172	O122	3887	–2106
173	O123	3887	–2006
174	O124	3887	–1906
175	O125	3887	–1806
176	O126	3887	–1706
177	O127	3887	–1606
178	O128	3887	–1506
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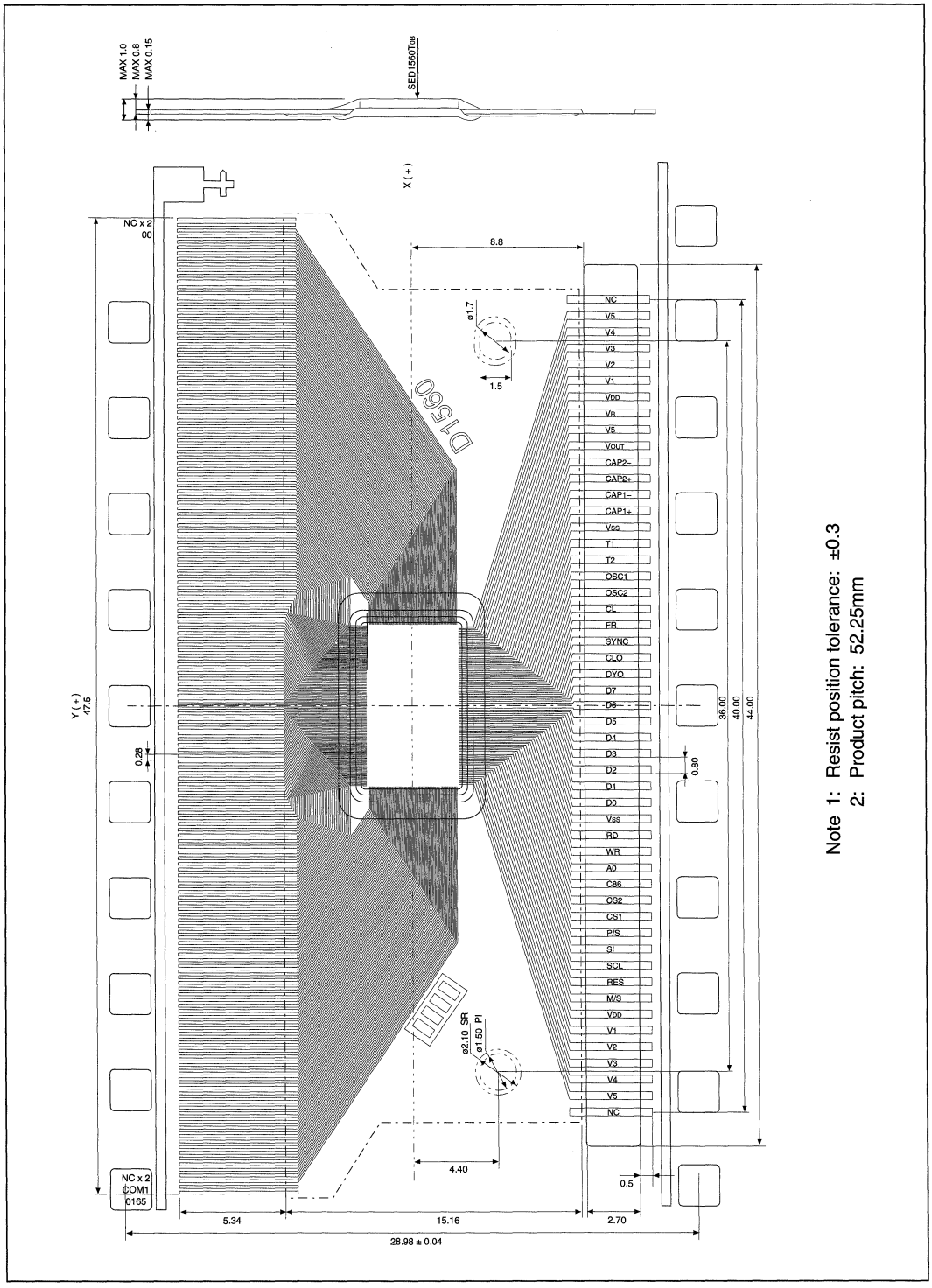
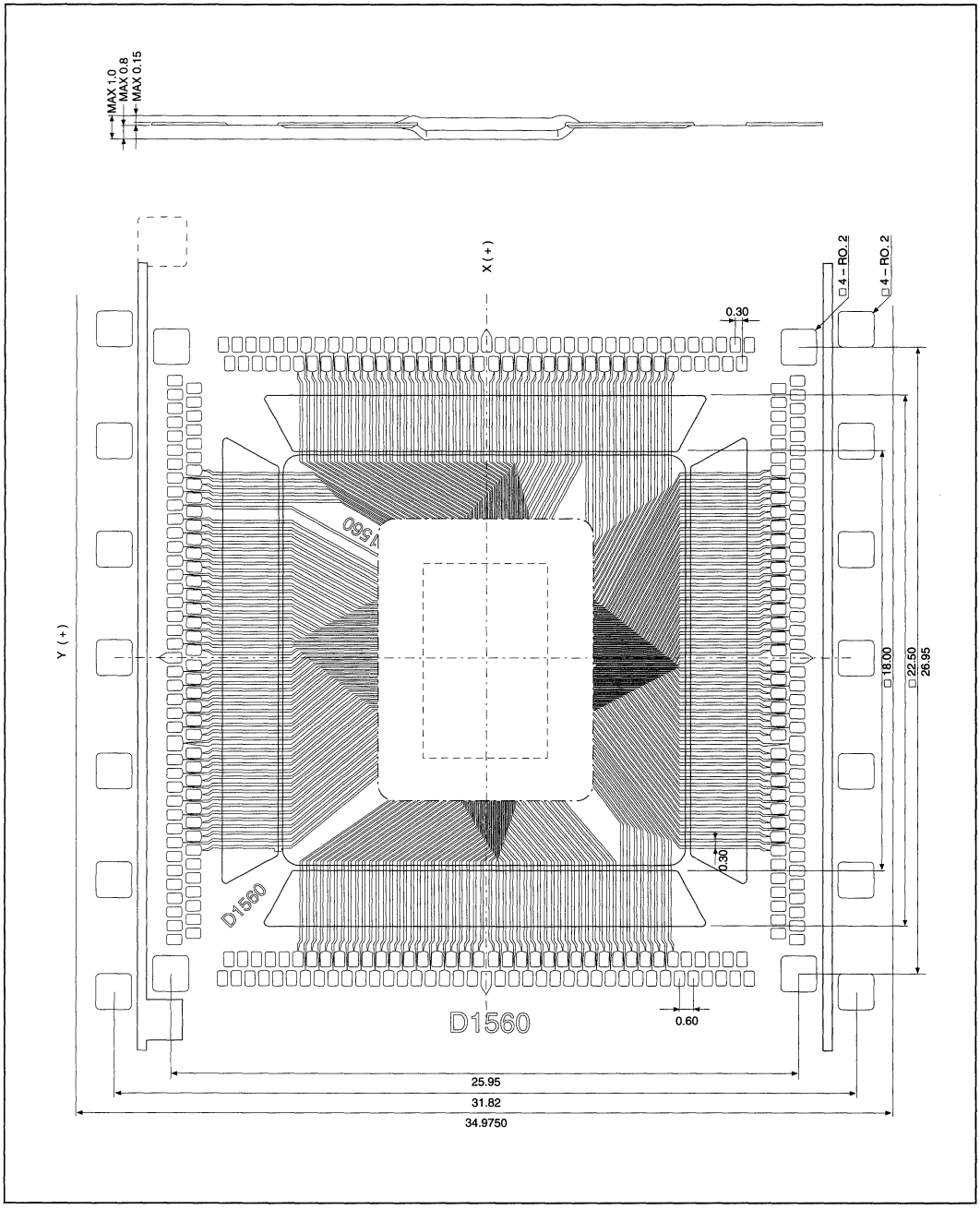
184	O134	3887	–906
185	O135	3887	–806
186	O136	3887	–706
187	O137	3887	–606
188	O138	3887	–506
189	O139	3887	–406
190	O140	3887	–306
191	O141	3887	–206
192	O142	3887	–106
193	O143	3887	–6
194	O144	3887	94
195	O145	3887	194
196	O146	3887	294
197	O147	3887	394
198	O148	3887	494
199	O149	3887	594
200	O150	3887	694
201	O151	3887	794
202	O152	3887	894
203	O153	3887	994
204	O154	3887	1094
205	O155	3887	1194
206	O156	3887	1294
207	O157	3887	1394
208	O158	3887	1494
209	O159	3887	1594
210	O160	3887	1694
211	O161	3887	1794
212	O162	3887	1894
213	O163	3887	1994
214	O164	3887	2094
215	O165	3887	2194
216	COMI	3887	2294

● TCP Dimensions (2-sided)



Note 1: Resist position tolerance: ±0.3
2: Product pitch: 52.25mm

● TCP Dimensions (4-sided)



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1996 DATABOOK

GRAPHICS PRODUCTS

V. HIGH-DUTY LCD SEGMENT DRIVERS

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■ HIGH-DUTY LCD SEGMENT DRIVERS

Part Number		SED 1180	SED 1181 xLA	SED 1181 F0A/ 5A	SED 1570	SED 1600	SED 1601	SED 1606	SED 1620	SED 1640	SED 1648	SED 1681	SED 1722	SED 1724	SED 1742	SED 1744	SED 1748	SED 1752	SED 1756	SED 1758	SED 1765	SED 1766	SED 1770	SED 1771
Discontinued?		Yes	Yes	Yes	No	Yes	Yes	No	Yes	No	No	Yes	No	No	No	No	No	No	No	No	No	No	No	No
Replacement		No	SED 168x	SED 168x	—	SED 1606	No	—	No	—	—	SED 168x	—	—	—	—	—	—	—	—	—	—	—	—
Resolution of segments		64	64	64	80	80	80	80	128	80	80	80	80	80	160	160	160	240	240	160	160	160	160	162
Duty Cycle		1/64 to 1/128	static to 1/32	1/64 to 1/128	1/64 to 1/200	1/100 to 1/300	1/100 to 1/300	1/100 to 1/300	1/64 to 1/200	1/100 to 1/300	1/100 to 1/300	1/8 to 1/32	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500
LCD Voltage (V)		–14 to –25	–3 to –12	–14 to –25	8 to 20	–12 to –28	–12 to –28	–8 to –28	–12 to –28	–8 to –28	–8 to –28	–3 to –12	14 to 40	14 to 40	14 to 40	14 to 40	8 to 42	8 to 42	14 to 42	14 to 42	14 to 40	14 to 40	5 to 17	5 to 17
Supply Voltage	5V	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	3V		x		x			x		x	x				x	x	x	x	x	x				
Display Data Bus (Bits)	1		x	x								x												
	2																							
	3 (R,G,B)																						x	x
	4	x			x	x		x	x	x	x		x		x									
	8						x							x		x	x	x	x	x	x	x		
Xscl,max (Mhz)		6	0.6	6	6.6	6.5	6.5	10	4	7.5	7.5	1	12	12	12	12	16	18		18	12	12	10	10
Companion Chips		1190	1210/ 78	1191	1635	1610/ 30/31	1610/ 30/31	1630/ 35	1631/ 32	1635	1651	1278	1733	1733	1743	1743	1743	1743	1755	1743	1703	1703	1743	1743
Panel Type	Passive	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x		
	MIM																				x		x	x
	TFT																						x	x

(continued)

■ HIGH-DUTY LCD SEGMENT DRIVERS (continued)

Part Number			SED 1180	SED 1181 xLA	SED 1181 F0A/ 5A	SED 1570	SED 1600	SED 1601	SED 1606	SED 1620	SED 1640	SED 1648	SED 1681	SED 1722	SED 1724	SED 1742	SED 1744	SED 1748	SED 1752	SED 1756	SED 1758	SED 1765	SED 1766	SED 1770	SED 1771
Package	Die	Al	D0A	DLA	D0A	D0A	DAA	DAA	D0A			D0A	D0A	D0A	D0A							D0A	D0A	D0A	D0A
		Au				D0B	DAB		D0B		D0B					D1B	D1B	D0B			D0B	D0B	D0B		
		COG								D0A										D0A					
		Pad Pitch (μm)		190	190	170	153	180	153	125	105	178	160	160	160	108	108	82				134	134	120	120
	QFP	Thin	F0A		F0A																				
		Thick	F5A	FLA	F5A		FAA	FAA					F0A	F0A	F0A										
		# of Pins	80	80	80		100	100					100	100	100										
	TAB	2 side														T0A	T0A	T0A					T0A		
		Lead Pitch (μm)														180	180								
		Slim									T0A#								T0A		T0A T0B (flex)				
Page number			425	443	435	453	469	479	489	503	513	525	539	551	551	563	563	583	599	615	627	645	657	673	673

Notes:
1. Some packages of certain parts labeld with # are still under development.

DISCONTINUED

SED1180

CMOS LCD 64-SEGMENT DRIVER

■ DESCRIPTION

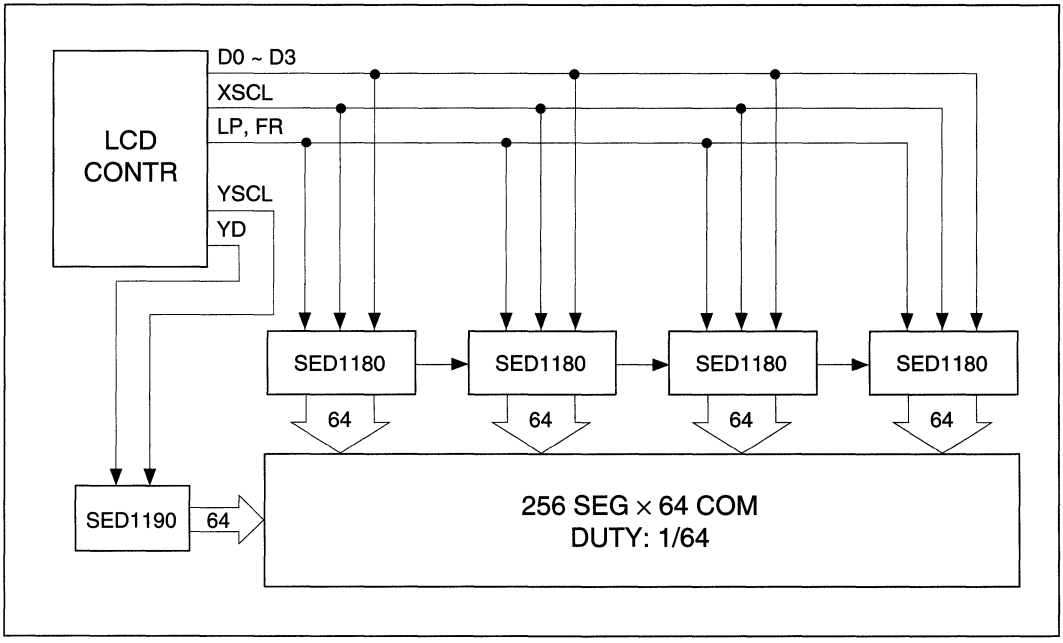
The SED1180 is a dot matrix LCD segment (column) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI contains 64-bit shift register for display data. The display data is supplied through 4-bit bus, and serially transferred through 16 × 4 bit shift register. The display data is held in a 64-bit latch circuit. The LSI converts the level of the latched data to an LCD drive waveform.

The SED1180 is used in conjunction with the SED1190 (64-bit row driver) to drive a large-capacity dot matrix LCD panel.

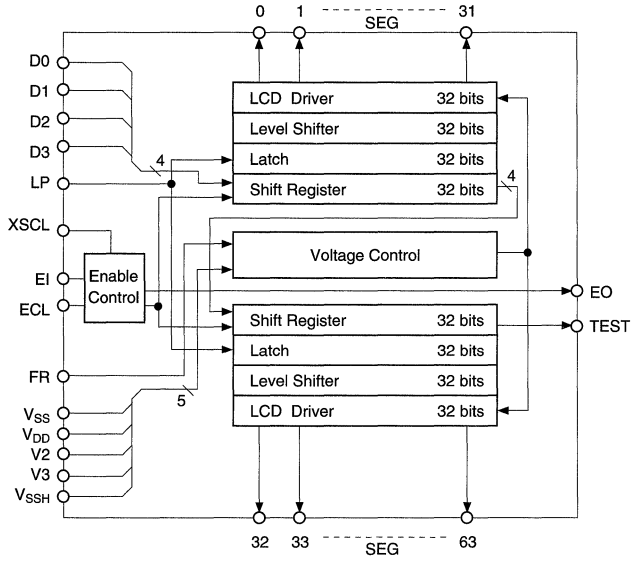
■ FEATURES

- Low-power CMOS technology
- 64-bit segment (column) driver
- High-speed 4-bit data
- Duty cycle ..... 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage ..... −14V to −25V
- Supply voltage ..... 5.0V ±10%
- Package ..... QFP1-80 pin (F0A)
  QFP5-80 pin (F5A)
  DIE: Al pad chip (D0A)

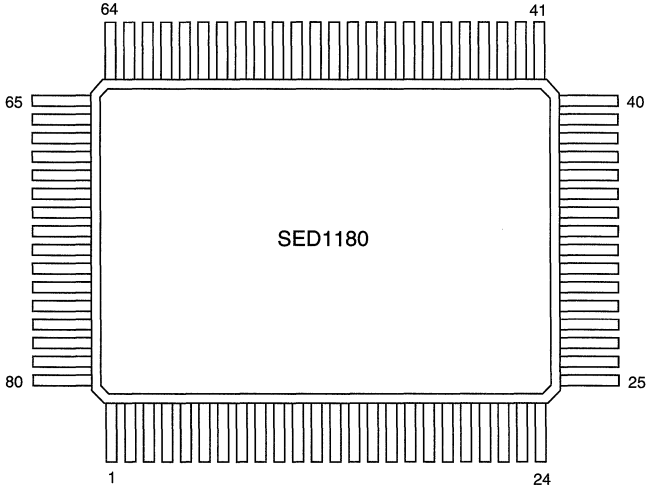
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	EO	49	SEG44	69	V_{SSH}
10	SEG18	30	D3	50	SEG45	70	V2
11	SEG17	31	D2	51	SEG46	71	V3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	TEST
15	SEG13	35	LP	55	SEG50	75	EI
16	SEG12	36	FR	56	SEG51	76	ECL
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ PIN DESCRIPTION

Pin Name	Function
SEG0 to SEG63	Outputs to segment pins of LCD. Output level changes at each latch pulse LP falling edge.
XSCL	Data shift clock input: display data is shifted in on the falling edge of this signal.
LP	Latch pulse for displayed data, falling edge trigger: display data is latched on the falling edge of this signal.
FR	LCD AC-drive signal
EI	Active high daisy chain enable input
EO	Active high daisy chain enable output
ECL	Daisy chain enable clock: the daisy chain enable is propagated on the falling edge of this clock.
D0 to D3	4-bit display data input
TEST	Test output
V_{DD}, V_{SS}	Logic power inputs
V2, V3, V_{SSH}	LCD drive power inputs V_{SSH}: −14V to −23V $V_{DD} \geq V2 \geq V3 \geq V_{SSH}$

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_{SSH}	–28.0 to +0.3	V
	V_2, V_3		
Input voltage	V_I	V_{SS} – 0.3 to +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C
Soldering temperature time	T_{sol}	260°C, 10 sec (at lead)	—

Notes:

1. All voltage measurements are based on V_{DD} = 0V.
2. V2 and V3 must always satisfy the condition $V_{DD} \geq V2, V3 \geq V_{SSH}$.
3. Exceeding the absolute maximum ratings can result in permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 0V, V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C)

Parameters	Symbol	Condition		Rating Min	Rating Typ	Rating Max	Unit
Supply voltage (1)	V_{SS}			–5.5	–5.0	–4.5	V
Supply voltage (2)	V_2			V_{SSH}	—	V_{DD}	V
	V_3			V_{SSH}	—	V_{DD}	V
	V_{SSH}	Recommended V_{SSH}		–25.0	—	–14.0	V
		Operable V_{SSH} (see note)		–25.0	—	–5.0	V
HIGH-level input voltage	V_{IH}			0.2V_{SS}	—	V_{DD}–0.3	V
LOW-level input voltage	V_{IL}			V_{SS}–0.3	—	0.8V_{SS}	V
HIGH-level output voltage	V_{OH}	I_{OH} = -0.6 ma		-0.4	—	—	V
LOW-level output voltage	V_{OL}	I_{OL} = 0.6 ma		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{SS}		—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{SS}		—	0.05	5.0	µA
Shift clock	XSCL			—	—	6.0	MHz
Frame signal	FR			—	1/60	—	S
Input capacitance	C_I	T_a = 25°C		—	5.0	8.0	pF
Segment output on resistance	R_{SEG}	V_{OH} = V_{DD} = –0.5 V V_{OL} = V_{SSH} = +0.5 V SEG bit	V_{SSH} = –20.0 V	—	1.9	2.9	kΩ
			V_{SSH} = –14.0 V	—	2.4	3.9	
			V_{SSH} = –9.0 V	—	3.6	7.0	
			V_{SSH} = –5.0 V	—	11.5	500.0	
Quiescent current	I_Q	V_{SSH} = –25 V, V_{SSH} = –5.5 V, V_I = V_{DD}		—	0.05	30	µA
Operating current for the logic	I_{SSO}	FR cycle = 16.7 ms ECL cycle = 13 µS	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, LP cycle=130 µS, XSCL=1.5 MHz, (duty 50%) All data input reversed bit by bit. All output pins are open.	—	90	200	µA
Operating current for the LCD	I_{SSHO}	FR cycle = 16.7 ms ECL cycle = 13 µS	V_{SS} = –4.5 V, V_2 = –4.0 V, V_1 = –16.0 V, V_{SSH} = –20.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, XSCL=1.5 MHz, (duty 50%), all data input reversed bit by bit. All output pins are open.	—	40	80	µA

(continued)

● **DC Electrical Characteristics (continued)**

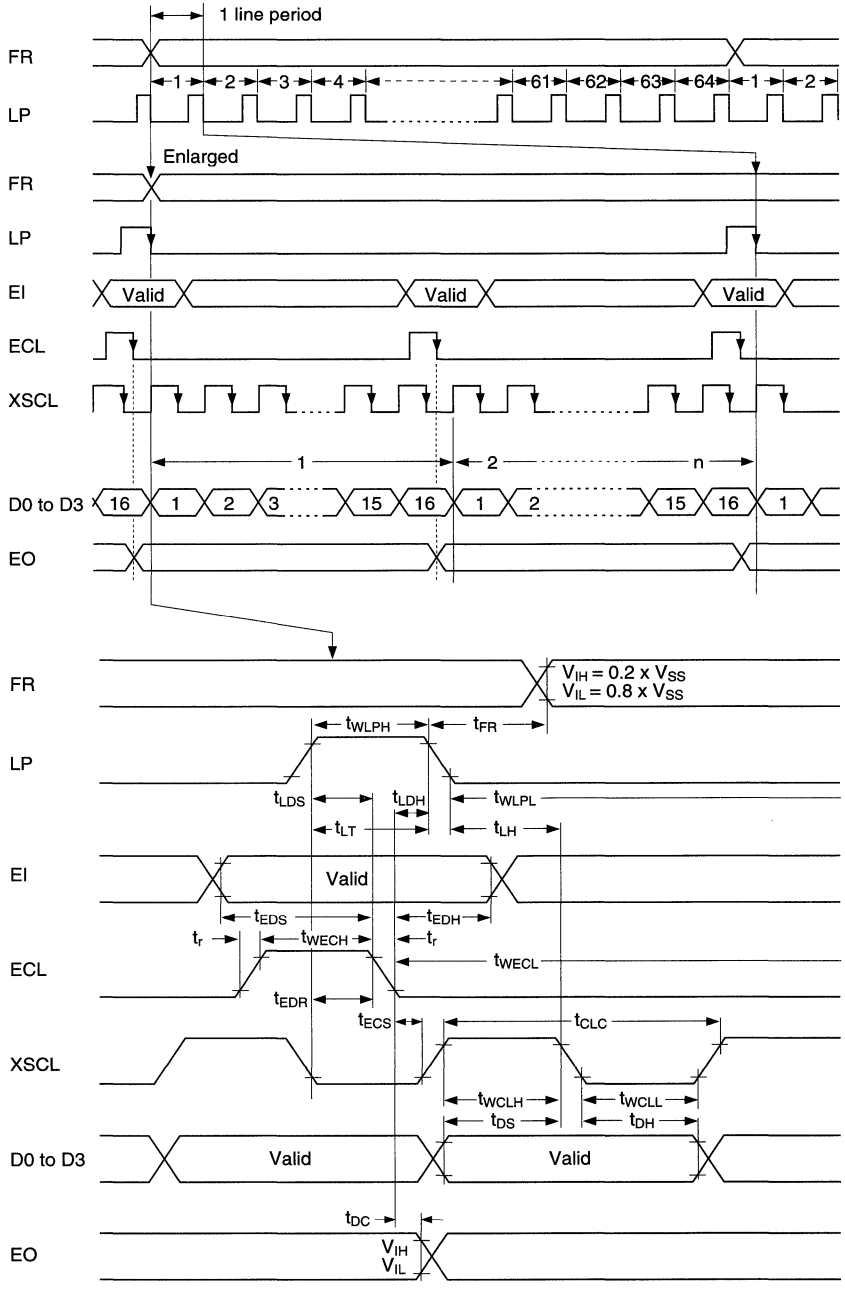
Parameters	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Shift clock cycle	t_{CLC}		166	—	—	ns
Shift clock "H" width	t_{WCLH}		63	—	—	ns
Shift clock "L" width	t_{WCLL}		63	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
Enable clock "H" width	t_{WECH}	See note 4	100	—	—	ns
Enable clock "L" width	t_{WECL}	See note 4	100	—	—	ns
Enable data setup time	t_{EDS}	See note 4	50	—	—	ns
Enable data hold time	t_{EDH}	See note 4	20	—	—	ns
Enable clock delay time	t_{EDR}	See note 4	–10	—	—	ns
Enable clock setup time	t_{ECS}	See note 4	70	—	—	ns
Latch pulse "H" width	t_{WLPH}	See note 2	110	—	—	ns
Latch pulse "L" width	t_{WLPL}		220	—	—	ns
Latch timing	t_{LT}		100	—	—	ns
Latch hold time	t_{LH}		0	—	—	ns
Latch pulse data setup time	t_{LDS}	See notes 3 & 4	140	—	—	ns
Latch pulse data hold time	t_{LDH}	See notes 3 & 4	50	—	—	ns
Permissible frame signal delay	t_{DFR}		–500	—	500	ns
Input signal rise time	t_r		—	—	See note 4	—
Input signal fall time	t_f		—	—	See note 4	—
Enable output delay	t_{PD}	See note 4	20	—	150	ns

Notes:

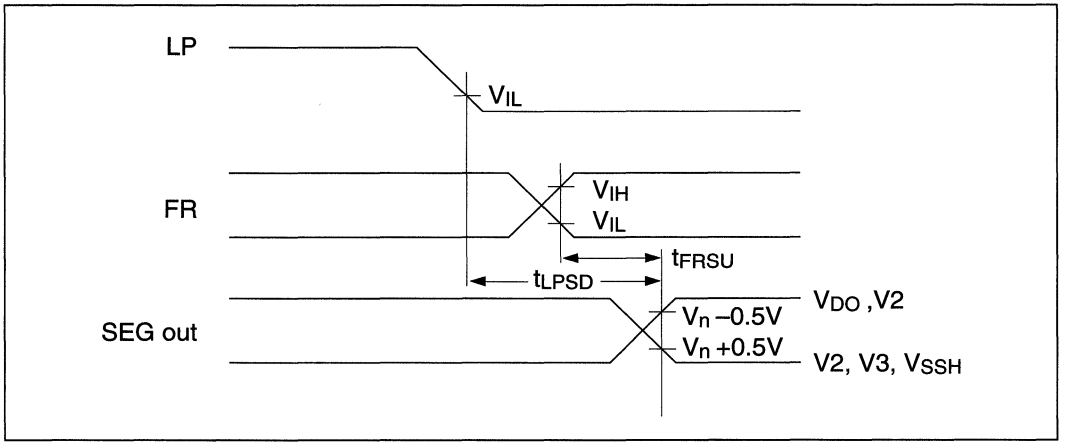
1. While the drive is guaranteed to operate without error within this voltage range, the output resistance of the segment drivers will be higher than that in the recommended operating range. It is suggested that the drive capability of the driver under these conditions is tested using the target panel.
2. t_{WLPH} = 160 ns (min) when LP is used as EI data.
3. t_{WLPH} = 250 ns (min) when EO is reset by LP.
4. Applies to the SED1180F only.
5. t_r, t_f < (t_{CLC} – t_{WCLH} – t_{WCLL}) / 2 and t_r, t_f ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS

● Data I/O Timing



● **Segment Drive Timing**

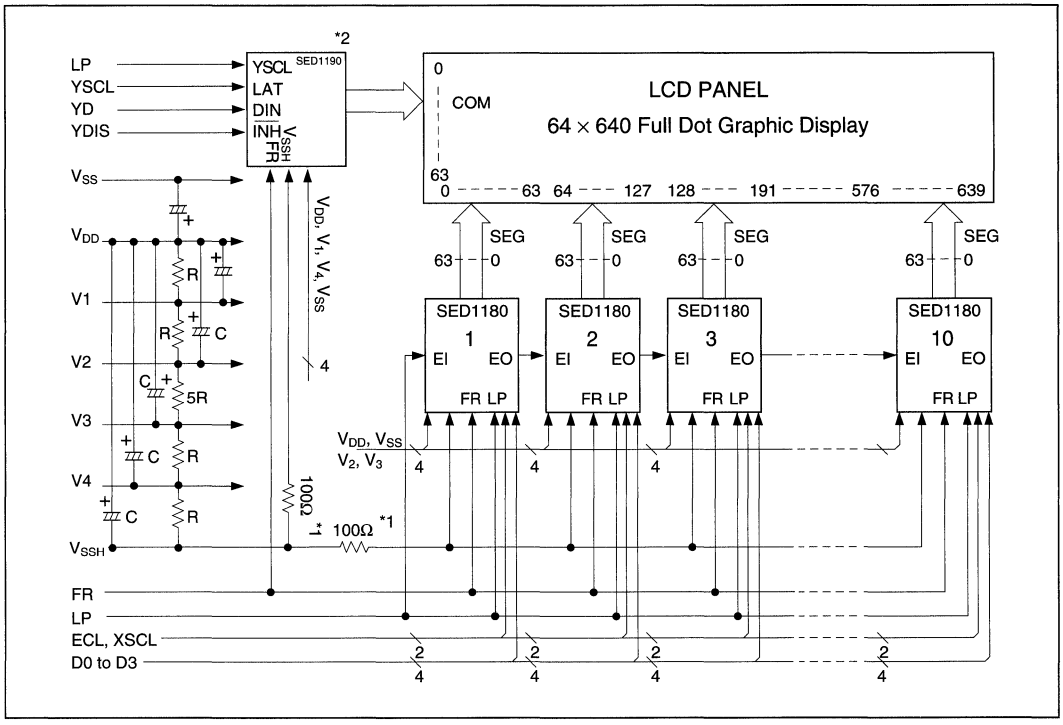


V_{IH} = 0.2V_{SS}; V_{IL} = 0.8V_{SS} (V_{DD} = 0V, V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameters	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
LP-SEG output delay time	t_{LPSD}	V_{SSH}=–14.0 to –25.0 V	—	—	4.5	µs
FR-SEG output delay time	t_{FRSD}	C_L= 100 pF	—	—	4.5	µs

■ TYPICAL SYSTEM CONNECTION

(64 × 640 pixels, 1/64 duty ratio)



Notes:

1. Current limiting resistors
2. Bypass V_{SS} and V_{SSH} with capacitors of at least 0.01 μF

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SED1181

CMOS LCD 64-SEGMENT DRIVER

■ DESCRIPTION

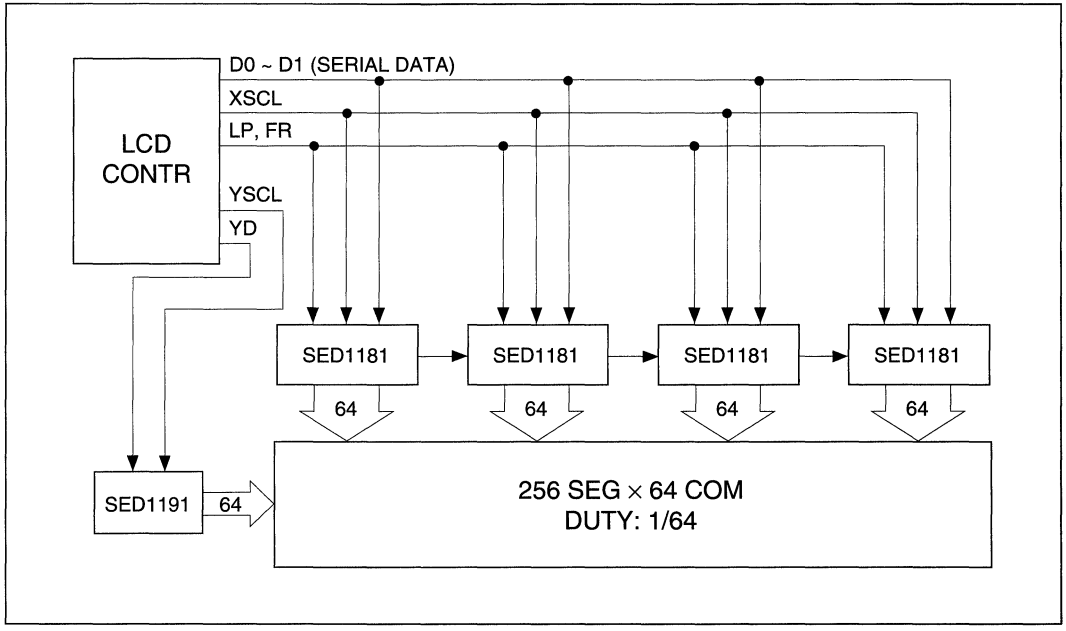
The SED1181 is a dot matrix LCD segment (column) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI contains 64-bit shift register for display data. The display data is supplied through LCD controller, and serially transferred through 16 × 4 shift register. The display data is held in a 64-bit latch circuit. The LSI converts the level of the latched data to an LCD drive waveform.

The SED1181 is used in conjunction with the SED1191 (64-bit row driver) to drive a large-capacity dot-matrix LCD panel.

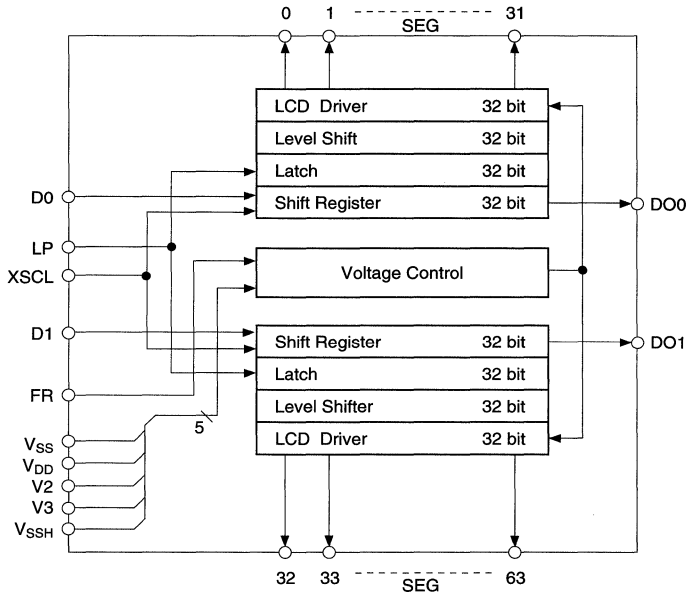
■ FEATURES

- Low-power CMOS technology
- 64-bit segment (column) driver
- Serial 2-bit input data
- Duty cycle ..... 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage ..... −14V to −25V
- Supply voltage ..... 5.0V ± 10%
- Package ..... QFP1-80 pin (F_{0A})
  QFP5-80 pin (F_{5A})

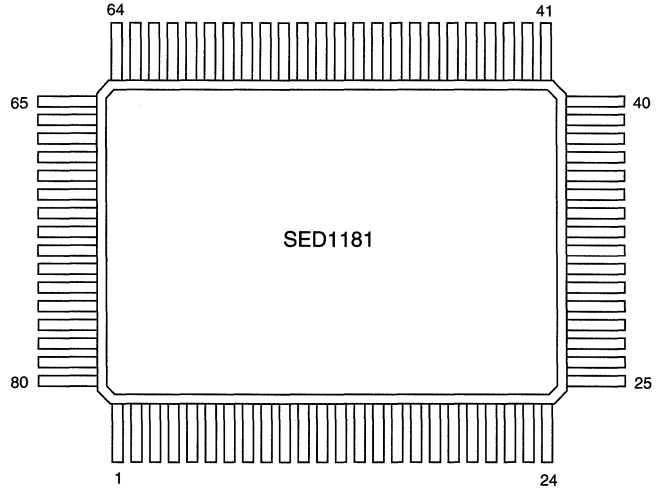
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	DO0	49	SEG44	69	V_{SSH}
10	SEG18	30	NC	50	SEG45	70	V2
11	SEG17	31	NC	51	SEG46	71	V3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	DO1
15	SEG13	35	LP	55	SEG50	75	NC
16	SEG12	36	FR	56	SEG51	76	NC
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ PIN DESCRIPTION

Pin Name	Function
D0	Serial data input to upper shift register
D1	Serial data input to lower shift register
SEG0 to SEG 31	Segment driver outputs supplied by the upper shift register
SEG 32 to SEG 63	Segment driver outputs supplied by the lower shift register
XSCL	Data shift clock input
LP	Data latch pulse input
FR	LCD frame signal input
DO0	Serial data output from upper shift register
DO1	Serial data output from lower shift register
V_{DD}, V_{SS}	Logic circuitry power inputs
V_{SSH}, V2, V3	LCD drive power inputs $V_{DD} > V2 > V3 > V_{SSH}$

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_{SSH}	–28.0 to +0.3	V
	V2, V3		
Input voltage	V_I	Vss -0.3 to +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature, time	T_{sol}	260°C, 10 sec (at lead)	°C / Sec

Notes:

1. All voltages are based on a V_{DD} of 0V.
2. V2 and V3 must satisfy the condition $V_{DD} \geq V2, V3 \geq V_{SSH}$.
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced during the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

● DC Electrical Characteristics

(V_{DD} = 0V, V_{SS} = –5.0V ± 10%, T_a = –20 to 75°C)

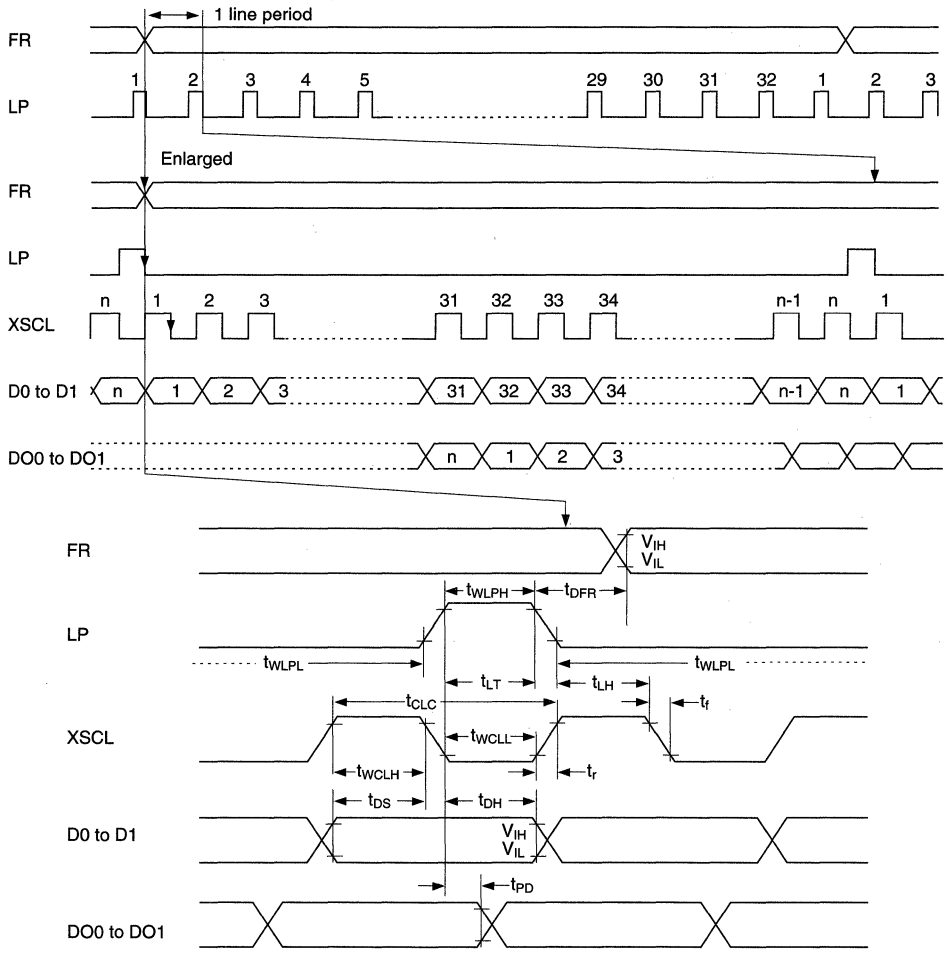
Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Supply voltage (1)	V_{SS}		–5.5	–5.0	–4.5	V
Supply voltage (2)	V2		V_{SSH}	—	V_{DD}	V
	V3		V_{SSH}	—	V_{DD}	V
	V_{SSH}		–25.0	—	–14.0	V
High level input voltage	V_{IH}		0.2V_{SS}	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}		V_{SS}–0.3	—	0.8V_{SS}	V
High level output voltage	V_{OH}	I_{OH} = –0.6 mA	–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 0.6 mA	—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{SS}	—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{SS}	—	0.05	5.0	µA
Shift clock	XSCL		—	—	6.0	MHz
Frame signal	FR		—	1/60	—	sec
Input capacitance	C_I	T_a = 25°C	—	5.0	8.0	pF
Segment output on resistance	R_{SEG}	V_{SSH} = –14.0 V V_{OH} = V_{DD} –0.5 V V_{OL} = V_{SSH} +0.5 V SEG./ bit	—	3.0	6.0	kΩ
Quiescent current	I_Q	V_{SSH} = –25.0V, V_{SS} = –5.5 V, V_I = V_{DD}	—	0.05	30	µA
Logic circuit	I_{SSOP}	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, FR period = 130 µs (duty 50%), LP period = 130 µS, XSCL frequency = 1.5 MHz (duty 50%)	—	850	1200	µA
LCD circuit operating current	I_{SSHOP}	V_{SS} = –4.5 V, V_2 = –4.0 V, V_3 = –16.0 V, V_{SSH} = –20.0 V, Other parameters as for I_{SSOP}	—	70	100	µA

Notes:

1. All voltages are based on a V_{DD} of 0V.
2. The driver will operate with a value of V_{SSH} in this range, however the "on" source impedance of a segment drive can be higher than at the recommended value of V_{SSH}. It is recommended that the drivers are tested with the LCD panel they will be used with to determine a suitable value for V_{SSH}.

■ AC ELECTRICAL CHARACTERISTICS

● Display Data Input/Output Timing



$V_{IH} = 0.2 \times V_{SS}$

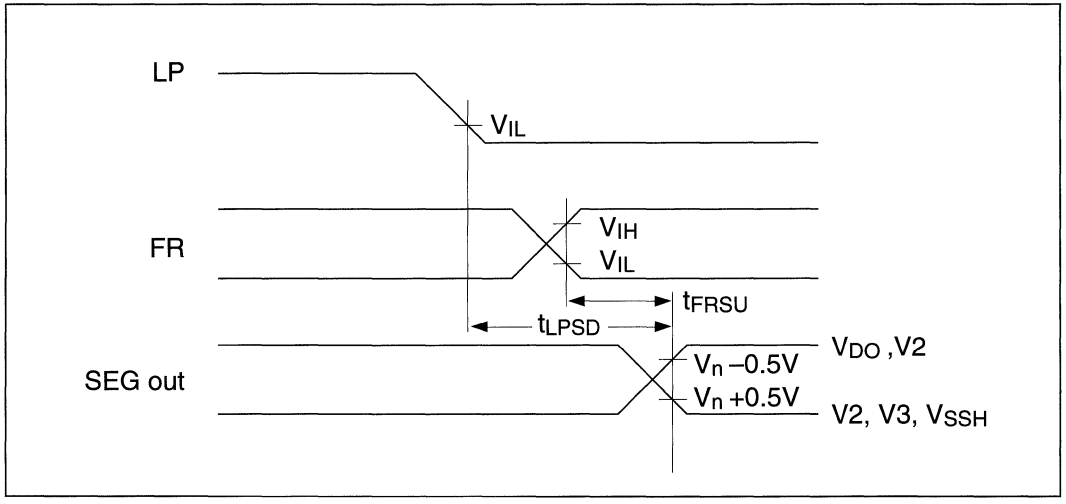
$V_{IL} = 0.8 \times V_{SS}$

● AC Electrical Characteristics

V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Shift clock cycle time	t_{CLC}		166	—	—	ns
Shift clock "H" width	t_{WCLH}		63	—	—	ns
Shift clock "L" width	t_{WCLL}		63	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
Latch pulse "H" time	t_{WLPH}		110	—	—	ns
Latch pulse "L" time	t_{WLPL}		220	—	—	ns
Latch hold time	t_{LT}		100	—	—	ns
XSCL to LP fall time	t_{LH}		0	—	—	ns
Permissible frame signal delay	t_{DFR}		–500	0	500	ns
Input signal rise time	t_r		—	—	—	ns
Input signal fall time	t_f		—	—	—	—
Data output delay time	t_{pD}		20	—	150	—

● Segment Drive Output Timing



V_{IH} = 0.2V_{SS}; VIL = 0.8V_{SS}; Vn: V_{DD}, V2, V3, V_{SSH}; (V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
LP-SEG output delay time	t_{LPSD}	V_{SSH}=–3.0 to –12.0 V,	—	—	4.5	µs
FR-SEG output delay time	t_{FRSD}	C_L= 100 pF	—	—	4.5	µs

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DISCONTINUED

SED1181FLA/DLA

Low Voltage Operation Products

CMOS DOT MATRIX EXTENSION LCD DRIVER

- **64-bit high voltage output**
- **Display duty factor: static to 1/32**
- **CMOS high-voltage process**

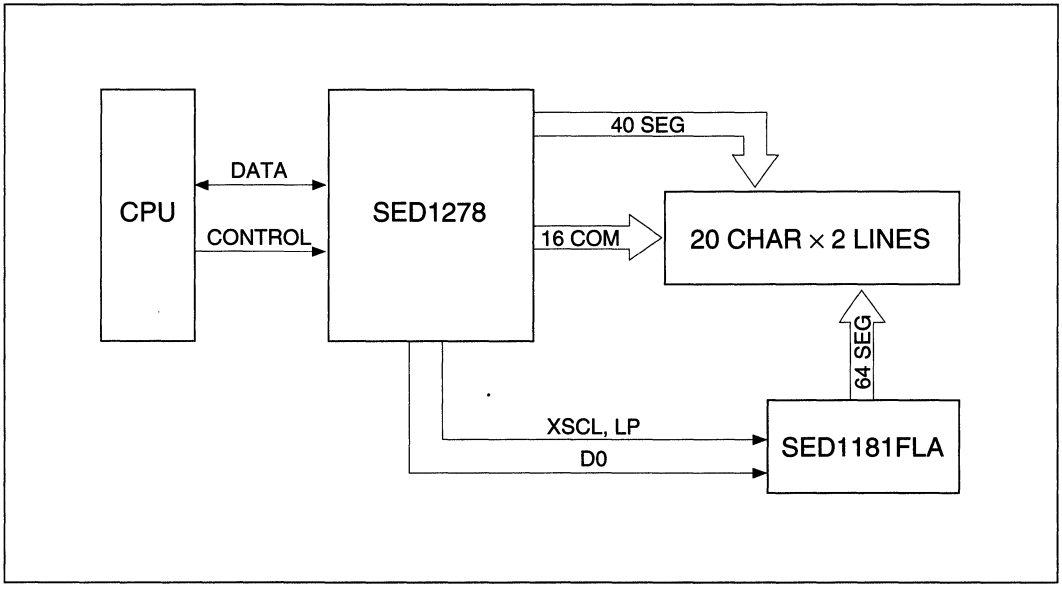
■ DESCRIPTION

The SED1181FLA is an expansion segment (column) driver suitable for driving high-contrast, small capacity dot matrix liquid crystal displays with a duty from static to 1/32. It is best suited for expanding the segment drive capability of LCD controllers such as the SED1278F, the SED1210F, or a 4-bit microcomputer.

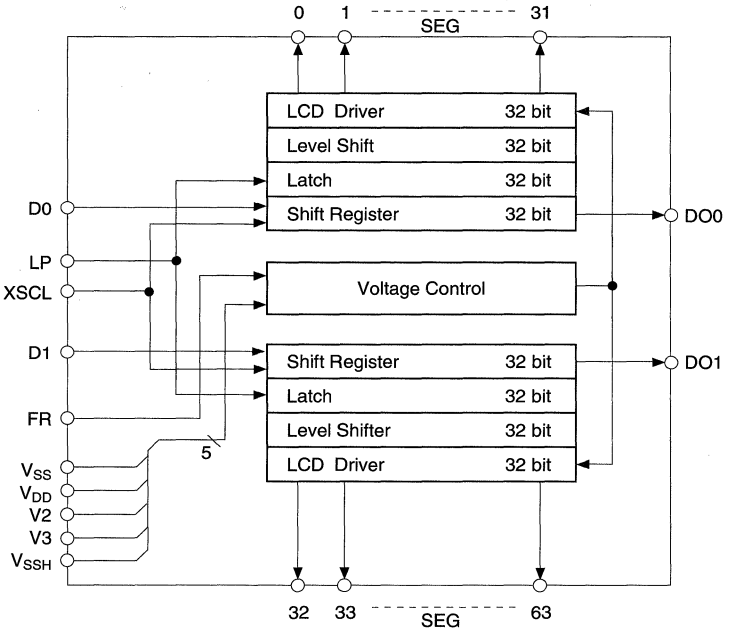
■ FEATURES

- Low-power CMOS technology
- 64-bit segment (column) driver
- Serial input data
- Duty cycle ..... Static to 1/32
- Suitable for use with a wide range of LCD controllers
- Capable of a serial cascade connection
- Wide range of LCD voltage .....–3.0V to –12V
- Supply voltage ..... 2.4V to 6.0V
- Package ..... QFP5-80 pin (FLA)
  DIE: Al pad chip (DLA)

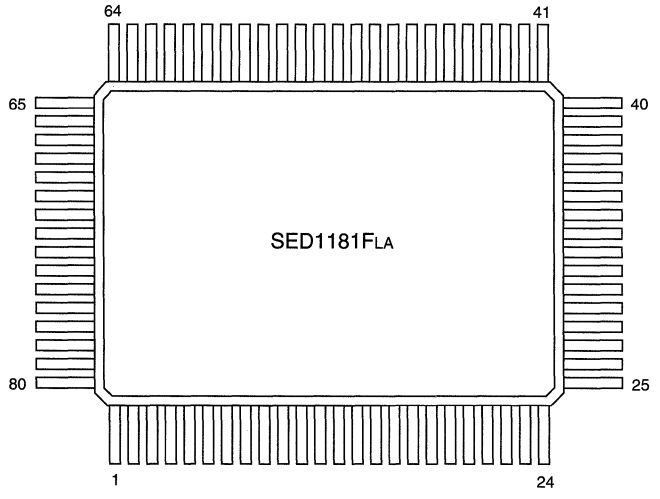
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	DO0	49	SEG44	69	V_{SSH}
10	SEG18	30	NC	50	SEG45	70	V2
11	SEG17	31	NC	51	SEG46	71	V3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	DO1
15	SEG13	35	LP	55	SEG50	75	NC
16	SEG12	36	FR	56	SEG51	76	NC
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ PIN DESCRIPTION

Pin Name	I/O	Function
D0	I	Serial data input to upper shift register
D1	I	Serial data input to lower shift register
SEG0 to SEG31	O	Segment driver outputs supplied by the upper shift register (output level changes at each latch pulse LP falling edge)
SEG32 to SEG65	O	Segment driver outputs supplied by the lower shift register
XSCL	I	Data shift clock input for display data - falling edge
LP	I	Data latch pulse input for display data - falling edge
FR	I	LCD frame signal input
DO0	O	Serial data output from upper shift register DO
DO1	O	Serial data output from lower shift register DI
V_{DD}, V_{SS}	I	Logic circuitry power inputs
V2, V3, V_{SSH}	I	LCD drive power inputs. $V_{DD} > V2 > V3 > V_{SSH}$

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to 0.3	V
Supply voltage (2)	V_{SSH}	–15.0 to 0.3	V
Supply voltage (3)	V2, V3	–15.0 to 0.3	V
Input voltage	V_{IN}	V_{SS} –0.3 to 0.3	V
Output voltage	V_O	V_{SS} –0.3 to 0.3	V
Permissible power dissipation	P_d	250	mW
Operating temperature	T_{opr}	–30 to 85	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature, time	T_{sol}	260°C, 10 sec	°C, s

Notes:

1. All voltages are based on a V_{DD} of 0V.
2. V2 and V3 must satisfy the condition $V_{DD} \geq V2, V3 \geq V_{SSH}$.
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

T_a = –30 to 85°C (unless otherwise specified)
V_{SS} = –5.0V ±10% (unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Supply voltage (1)	V_{SS}		–6.0	–5.0	–2.4	V
Supply voltage (2)	V_2		V_{SSH}	—	V_{DD}	V
	V_3		V_{SSH}	—	V_{DD}	V
	V_{SSH}	Recommended operation V_{SSH}	–12.0	—	–3.0	V
		Potential operation V_{SSH} *2	–12.0	—	–2.5	V
High-level input voltage	V_{IH}		0.2V_{SS}	—	V_{DD}+0.3	V
Low-level input voltage	V_{IL}		V_{SS}–0.3	—	0.8V_{SS}	V
High-level output voltage	V_{OH}	I_{OH} = –0.6 mA	–0.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 0.6 mA	—	—	V_{SS}+0.4	V
Input leak current	I_{LI}	0 V ≤ V_{IN} ≤ V_{SS}	—	0.05	2.0	µA
Output leak current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{SS}	—	0.05	5.0	µA
Transmission clock	XSCL		—	—	600	kHz
Frame cycle	FR		—	1/60	—	sec
Input pin capacity	C_{IN}	T_a = 25°C	—	5.0	8.0	pF
SEG output ON resistance	R_{SEG}	Δ V_{ON} = 0.1 V, T_a = 25°C, V_{SSH} = –8.0V	—	3.0	—	kΩ
		V_{SSH} = –5.0V	—	5.0	—	
		V_{SSH} = –3.0V	—	16.0	—	
Static current consumption	I_Q	V_{SSH} = –12.0 V, V_{SS} = –6.0 V, V_{IN} = V_{DD}	—	0.05	30.0	µA
Logic power supply's average current consumption	I_{SS} OP	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, FR cycle = 16.7 ms (duty 50%), LP cycle = 520 µS, XSCL = 400 kHz (duty 50%), All data input: Inverted at each bit, All output pins are open.	—	250	300	µA
LCD's average current consumption	I_{SSH} OP	V_{SS} = –4.5 V, V_2 = –4.8 V, V_3 = –7.2 V, V_{SSH} = –12.0 V, Other conditions are identical to those for I_{SS} OP	—	8	10	µA

Notes:

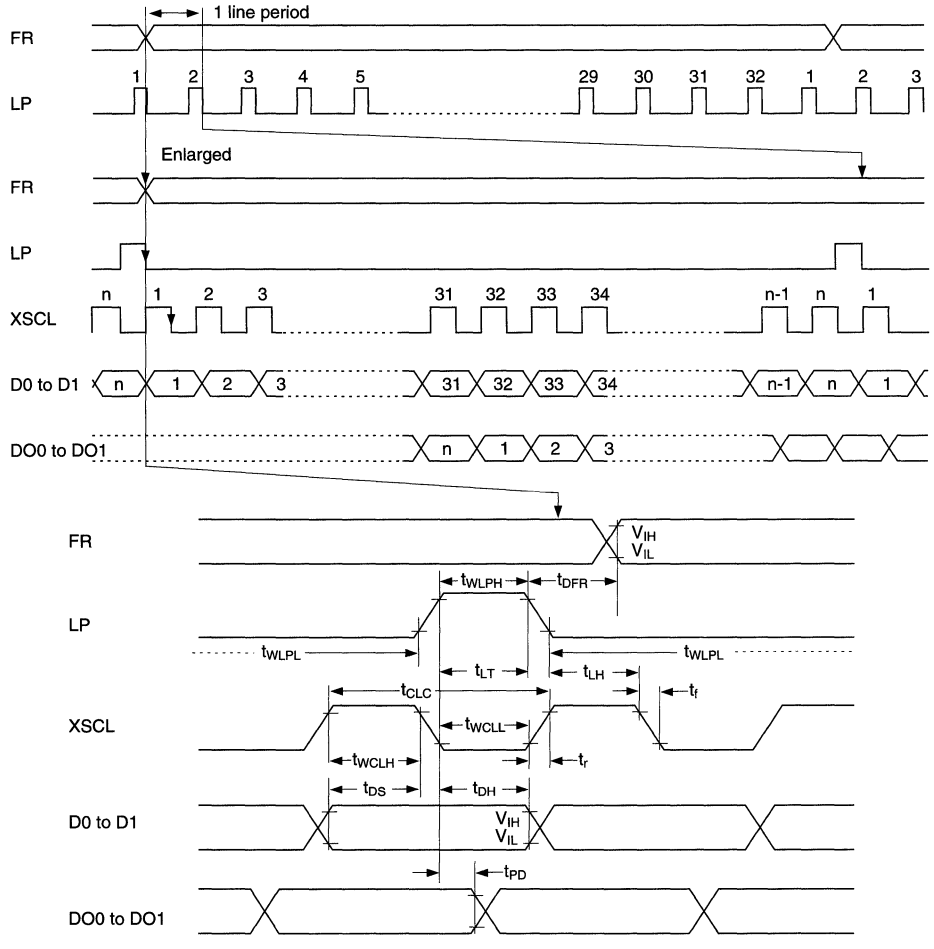
1. The voltage values are based on a V_{DD} of 0 V.
2. The driver will operate with a value of V_{SSH} in this range, however the ON source impedance of a segment drive can be higher than that at the recommended value of V_{SSH}. It is recommended that the drivers are tested with the LCD panel they will be used with, to determine a suitable value for V_{SSH}.

● **AC Electrical Characteristics**

(V_{SS} = –6.0 to –2.4V, T_a = –30 to 85°C)

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Shift clock cycle	t_{CLC}		1.66	—	—	µs
Shift clock pulse width (High)	t_{WCLH}		450	—	—	ns
Shift clock pulse width (Low)	t_{WCLL}		600	—	—	ns
Data set-up time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
Latch pulse width (High)	t_{WLPH}		200	—	—	ns
Latch pulse width (Low)	t_{WLPL}		600	—	—	ns
Latch timing cycle	t_{LT}		200	—	—	ns
Latch hold time	t_{LH}		100	—	—	ns
Permissible frame signal delay time	t_{DFR}		–500	0	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns
Serial data output delay time	t_{pD}		20	—	250	ns

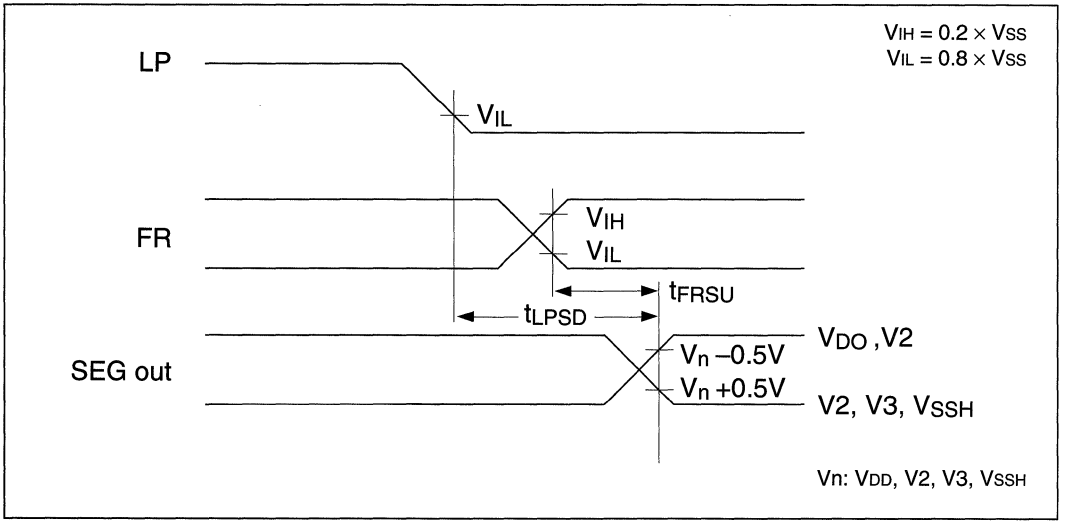
● Display Data Input/Output Timing



$V_{IH} = 0.2 \times V_{SS}$

$V_{IL} = 0.8 \times V_{SS}$

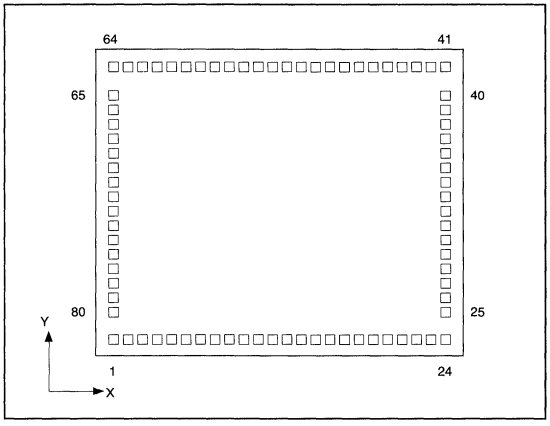
● **Segment Drive Output Timing**



(VSS = –6.0 to –2.4V, Ta = –30 to 85°C)

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
LP-SEG output delay time	tLPSD	VSSH= –3.0 to –12.0 V,	—	—	4.5	µs
FR-SEG output delay time	tFRSD	CL= 100 pF	—	—	4.5	µs

● PAD LAYOUT



Chip size ..... 4.85mm × 3.57mm
Chip thickness ..... 0.4 ± 0.03mm
Pad size ..... 0.104mm × 0.104mm
Pad pitch 0.19mm
Chip metalization ..... Al

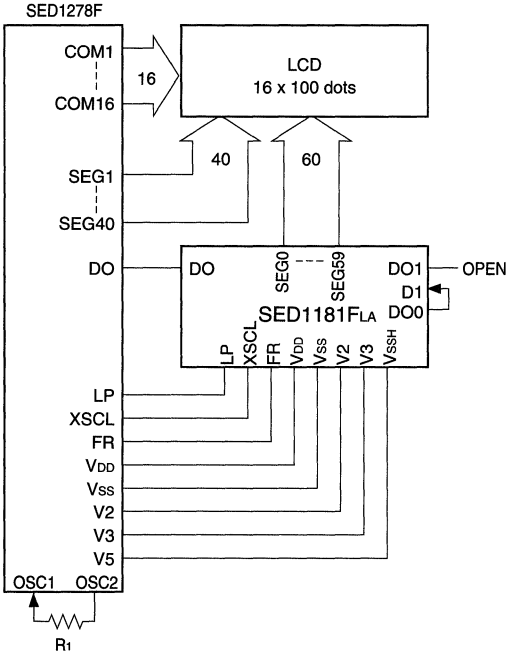
Note: Connect underside to GND or insulate

● PAD COORDINATION

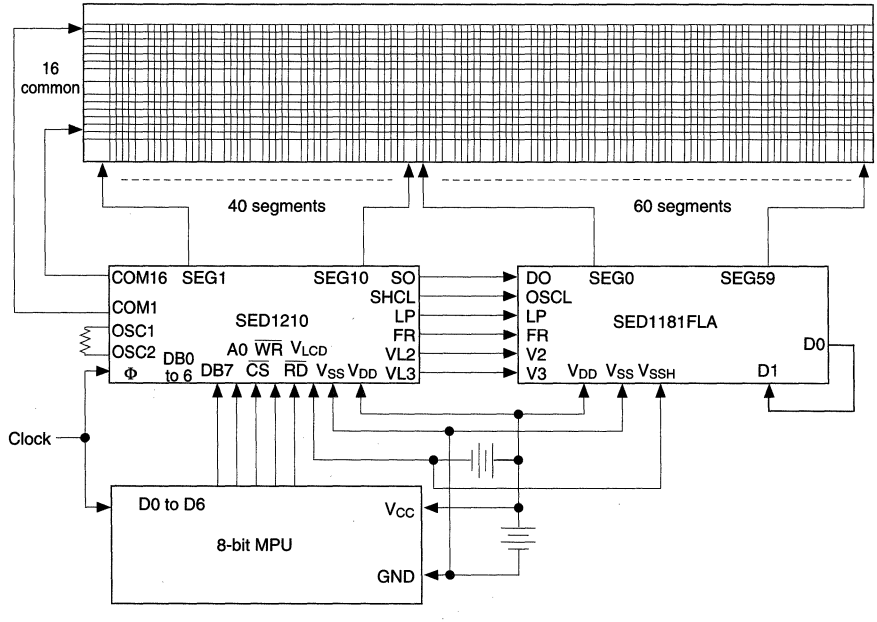
Pad		X (μm)	Y (μm)	Pad		X (μm)	Y (μm)	Pad		X (μm)	Y (μm)
Number	Name			Number	Name			Number	Name		
1	SEG27	155	155	28	SEG0	4690	916	55	SEG50	1947	3415
2	SEG26	423	155	29	DO0	4690	1107	56	SEG51	1756	3415
3	SEG25	614	155	30	NC	4690	1297	57	SEG52	1566	3415
4	SEG24	804	155	31	NC	4690	1488	58	SEG53	1375	3415
5	SEG23	995	155	32	D1	4690	1678	59	SEG54	1185	3415
6	SEG22	1185	155	33	D0	4690	1868	60	SEG55	995	3415
7	SEG21	1375	155	34	XSCL	4690	2059	61	SEG56	804	3415
8	SEG20	1566	155	35	LP	4690	2249	62	SEG57	614	3415
9	SEG19	1756	155	36	FR	4690	2440	63	SEG58	423	3415
10	SEG18	1947	155	37	SEG32	4690	2630	64	SEG59	155	3392
11	SEG17	2137	155	38	SEG33	4690	2820	65	SEG60	155	3201
12	SEG16	2327	155	39	SEG34	4690	3011	66	SEG61	155	3011
13	SEG15	2518	155	40	SEG35	4690	3201	67	SEG62	155	2820
14	SEG14	2708	155	41	SEG36	4690	3392	68	SEG63	155	2630
15	SEG13	2899	155	42	SEG37	4422	3415	69	V_{SSH}	155	2440
16	SEG12	3089	155	43	SEG38	4231	3415	70	V_2	155	2249
17	SEG11	3279	155	44	SEG39	4041	3415	71	V_3	155	2059
18	SEG10	3470	155	45	SEG40	3851	3415	72	V_{SS}	155	1868
19	SEG9	3660	155	46	SEG41	3660	3415	73	V_{DD}	155	1676
20	SEG8	3851	155	47	SEG42	3470	3415	74	DO1	155	1488
21	SEG7	4041	155	48	SEG43	3279	3415	75	NC	155	1297
22	SEG6	4231	155	49	SEG44	3089	3415	76	NC	155	1107
23	SEG5	4422	155	50	SEG45	2899	3415	77	SEG31	155	916
24	SEG4	4690	155	51	SEG46	2708	3415	78	SEG30	155	726
25	SEG3	4690	345	52	SEG47	2516	3415	79	SEG29	155	536
26	SEG2	4690	536	53	SEG48	2327	3415	80	SEG28	155	345
27	SEG1	4690	726	54	SEG49	2137	3415				

■ REFERENCE CIRCUIT EXAMPLES

(12 characters, 4 lines, 1/16 duty cycle)



(20 characters, 2 lines, 1/16 duty)



■ DESCRIPTION

The SED1570 is an 80-segment LCD driver for driving the LCD panel. The SED1570 features internal display RAM. The display data is stored in RAM and it generates the LCD waveforms.

The LSI offers the "self-refresh mode." It means that no data will transfer from the display controller to the SED1570 if the contents of the data do not change.

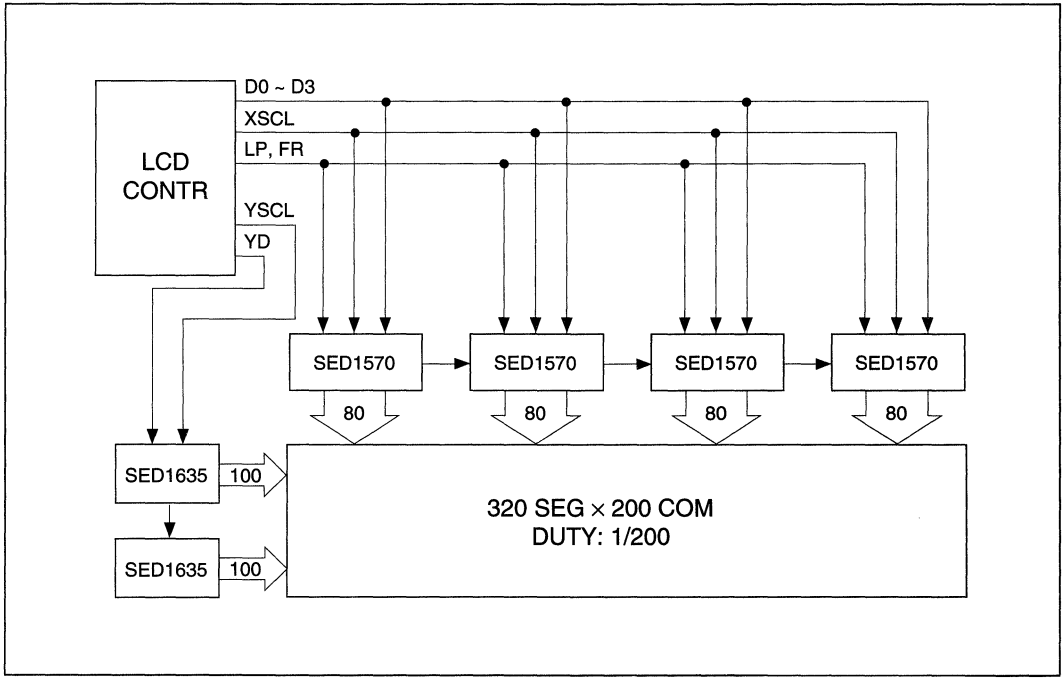
The device allows configuration of an ultra-low-power display system, since the display data is not transferred unless the display data is changed.

The SED1570 is used in conjunction with the SED1635 common (100 output row driver) to support LCD panels from midrange to VGA size. The device is suitable for applications that require low power consumption.

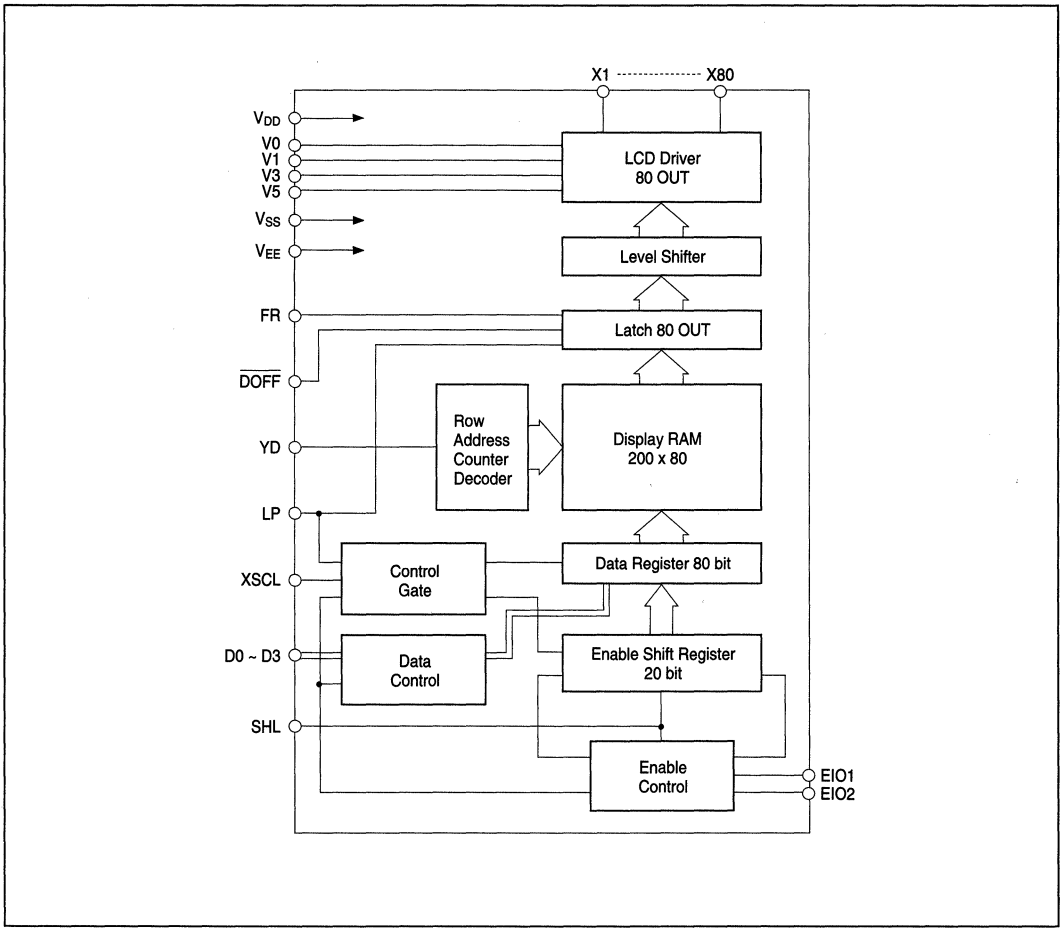
■ FEATURES

- Low-power CMOS process technology
- Supports the self-refresh mode
- LCD driver output 80
- Duty cycle ..... 1/64 to 1/200
- Display RAM ..... 200 × 80 bits
- Supply voltage ..... 2.7 to 5.5V
- LCD voltage ..... 8.0 to 20V
- High-speed data (4-bit parallel) transfer
- Daisy chain support
- Non-bias display off function
- Output shift direction—pin selection
- Optimize the LCD power offset bias for V_{DD}
- Package ..... Al pad (D_{0A})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Enable Shift Register

The order of the display data latched is reversed by the SHL input.

● Enable Control and Data Control

If the enable signal is disabled (EIO = "H"), the internal clock signal and the data bus are fixed to "L". This is a power-save mode.

To use multiple segment drivers, connect in cascade format the EIO pin of each driver, and connect the EIO pin of the first driver to the "Vss" pin.

The enable control circuit automatically detects when the 80-bit data has been read and automatically transfers the enable signal. As a result, a control signal by a control LSI is not necessary.

- **Display RAM**

  This is a static RAM (200 × 8 bits) that stores the LCD data.

  The display RAM data (80 bits) for the low address is read out to the latch with the trailing edge of the LP signal. In addition, with the trailing edge of the LP signal, the contents of the data register are moved to the write register. The contents of the write register are then written in the display RAM area for the low address. The low address is then incremented.

  If the XSCL signal does not come in after the trailing edge of the LP signal, the mode is changed to the self-refresh mode. The write register does not write data in the display RAM and the low address is incremented. The mode is then changed to the read-out mode to read the next line.

- **Low Address Counter Decoder**

  This selects a line of the display RAM in sequence. This decoder catches the "H" of the DY signal at the trailing edge of the LP signal, and resets the low address counter. It then initializes the selected address of the display RAM. In a normal operation, the decoder is incremented after the writing operation into the display RAM. (The writing operation is caused by the trailing edge of the LP signal.) In the self-refresh mode, the decoder is incremented without the writing operation into the display RAM.

- **Data Register**

  This 80-bit register controls the write operation into the display RAM. The data is written in the display RAM with the trailing edge of the LP signal. In the self-refresh mode, the data is not written in the display RAM.

- **Control Circuit**

  The control circuit detects the self-refresh mode, allows the write register to write the data into the display RAM, and controls the low address count signal.

- **Latch**

  This reads the 80-bit data for the low address of the display RAM with the trailing edge of the LP signal, and sends the output signal to the level shifter.

- **Level Shifter**

  This is the level interface circuit that converts the signal voltage level from $V_{DD} - V_{SS}$ to $V_{DD} - V_{EE}$ (LCD driver power).

- **LCD Driver**

  The LCD driver outputs the LCD driver voltage.

  The table to the right shows the relationship between the display signals (D3 – D0), LCD AC-drive waveform (FR) and the segment output voltage.

$\overline{DOFF}$	D0 – D3	FR	X Output Voltage
H	H	H	V0
		L	V5
	L	H	V2
		L	V3
L	—	—	V0

■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>X1 – X80</td><td>O</td><td>LCD drive segment (column) output
The output changes with the LP's trailing edge.</td><td>80</td></tr>
<tr><td>D0 – D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input
Reads the display data (D0 ~ D3) into the data register with a trailing edge.</td><td>1</td></tr>
<tr><td>LP</td><td>I/O</td><td>Display data latch clock input
● The display RAM data (specified by the low address shift register) is read into the latch with a leading edge, and the LCD display data is output.
● For a specified low address, the contents of the write register are written in the display RAM.
● Resets the enable control circuit.</td><td>1</td></tr>
<tr><td>EIO1, EIO2</td><td>I</td><td>Enable I/O
● Configured by SHL.
● Output is reset to "H" by LP input. When the 80-bit display data is read, the output falls to "L" automatically.
● To connect in cascade format, connect these pins to the next level EIO.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction and input/output select input
● If the display data is entered in the input (D3, D2, D1, D0) in the order of (a1, a2, a3, a4) (b1, b2, b3, b4) ... (t1, t2, t3, t4), the relationship of the display data and the segment output is as given in the table below.
<table>
<tr><th rowspan="2">SHL</th><th colspan="13">Xn (SEG output)</th><th colspan="2">EIO</th></tr>
<tr><th>80</th><th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>...</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a1</td><td>a2</td><td>a3</td><td>a4</td><td>b1</td><td>b2</td><td>...</td><td>s3</td><td>s4</td><td>t1</td><td>t2</td><td>t3</td><td>t4</td><td>O</td><td>I</td></tr>
<tr><td>H</td><td>t4</td><td>t3</td><td>t2</td><td>t1</td><td>s4</td><td>s3</td><td>...</td><td>b2</td><td>b1</td><td>a4</td><td>a3</td><td>a2</td><td>a1</td><td>I</td><td>O</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>Forced blank input
In the "L" level, the segment output is forced to the V0 level.
The display RAM data is maintained.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD AC drive signal input</td><td>1</td></tr>
<tr><td>YD</td><td>I</td><td>Scan start input
● Resets the low address counter decoder.
● The number of scanned lines (number of low addresses) for the display RAM is determined by the number of LP pulses, which are input in one YD cycle.</td><td>1</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power supply</td><td>LCD drive power input
$V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$</td><td>4</td></tr>
<tr><td>V_{EE}</td><td>Power supply</td><td>LCD drive power input $V_{DD} - V_{EE}$</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power input
V_{DD}: connect to the system V_{SS} pin.
V_{SS}: connect to the system GND.</td><td>2</td></tr>
</table>

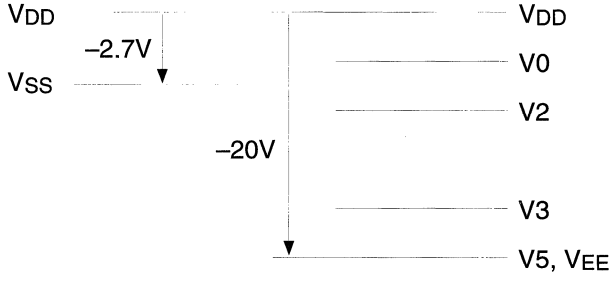
■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Supply voltage 1	V_{SS}	–7.0 to +0.3	V
Supply voltage 2	V_{EE}	–22.0 to +0.3	V
Supply voltage 3	V0, V2, V3, V5	V_{EE} – 0.3 to V_{DD} + 0.3	V
Input voltage	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	V_O	V_{SS} – 0.3 to V_{DD} + 0.3	V
EIO output current	IO1	20	mA
Operating temperature	T_{OPR}	–40 to +85	°C
Storage temperature 1	T_{STG1}	–65 to +150	°C
Storage temperature 2	T_{STG2}	–55 to +100	°C

Notes:

1. All voltages are given relative to V_{DD} = 0V.
2. For storage temperature 1 – Plastic package
   For storage temperature 2 – TAB mounted
3. V0, V2, V3 and V5 must satisfy the condition $V_{DD} \geq V0 \geq V2 \geq V3 \geq V5 \geq V_{EE}$



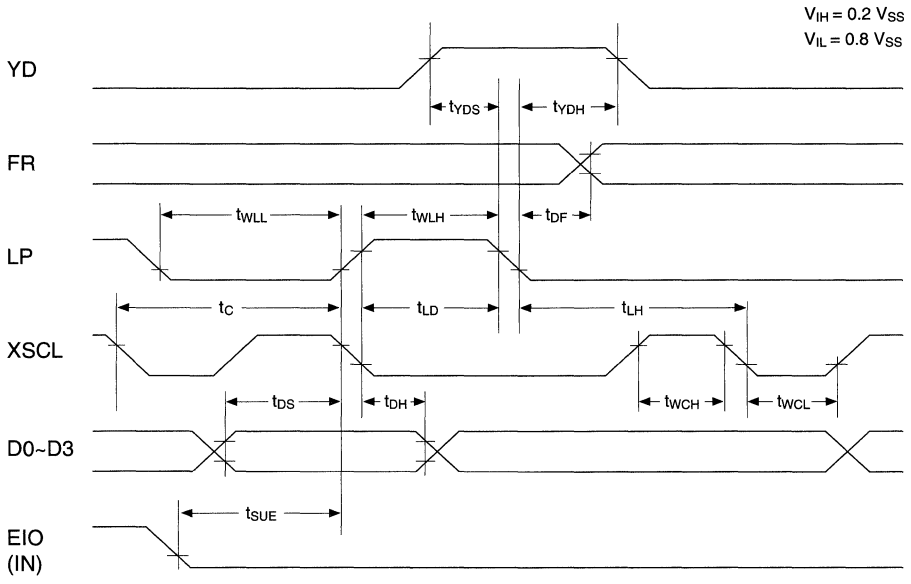
4. Exceeding the absolute maximum ratings can cause permanent damage to the device. Function operation under these conditions is not implied.

● DC Characteristics

V_{DD} = V0 = 0V, V_{SS} = –5.0V ±10%, T_a = –40 to 85°C

Parameter		Symbol	Condition		Min	Typ	Max	Unit	Pin
Supply voltage		V_{SS}			–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage		V_{EE}	V_{SS} = –2.7 to –5.5V		–20.0	—	–8.0	V	V_{EE}
Supply voltage (2)		V0	Recommended value		V_{DD} – 2.5	—	V_{DD}	V	V0
Supply voltage (3)		V2	Recommended value		2/9 V_{EE}	—	—	V	V2
Supply voltage (4)		V3	Recommended value		—	—	7/9 V_{EE}	V	V3
Supply voltage (5)		V5	Recommended value		V_{EE}	—	V_{EE} + 2.5	V	V5
Input high voltage		V_{IH}	V_{SS} = –2.7 to –5.5V		0.2 • V_{SS}	—	—	V	EIO1, EIO2, FR, D0 to D3, YD, LP, SHL, DOFF, XSCL
Input low voltage		V_{IL}			—	—	0.8 • V_{SS}	V	
Output high voltage		V_{OH}	V_{SS} = –2.7	I_{OH} = –0.6mA	V_{DD} – 0.4	—	—	V	EIO1, EIO2
Output low voltage		V_{OL}	to –5.5V	I_{OL} = 0.6mA	—	—	V_{DD} + 0.4	V	
Input leakage current		I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		—	—	2.0	µA	D0 to D3, LP, FR, YD, XSCL, SHL, DOFF
I/O leakage current		$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$		—	—	5.0	µA	EIO1, EIO2
Static current		I_{SS}	V5 = –20.0 to –10.0V V_{IH} = V_{DD}, V_{IL} = V_{SS}		—	—	25	µA	V_{SS}
On resistance		R_{SEG}	ΔVON = 0.5V, V0 = V_{DD}, V3 = 7/9 • V_{EE}, V2 = 2/9 • V_{EE}, V_{EE} = V5 = –14.0V		—	1.0	1.4	KΩ	X1 to X80
Average current consumption (1)	Data transfer mode	I_{DDT}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{XSCL} = 4.0MHz, F_{LP} = 14kHz, f_{FR} = 70Hz, Checkered pattern, non-burden		—	0.3	0.8	mA	V_{DD}
	Self-refresh mode	I_{DDS}	f_{XSCL} = 0 Hz = V_{SS}, Another place is same as I_{DDT} item		—	70	200	µA	
Average current consumption (2)		I_{EE}	V_{SS} = –5.0V, V0 = 0.0V, V2 = –4.0V, V3 = –16V, I_{EE} = V5 = –20.0V, Another place is same as I_{DDT} item		—	25	70	µA	V_{EE}
Input capacitance		C_I	Freq. = 1 MHz, T_a = 25°C, Simple substance of CHIP		—	—	8	pF	D0 to D3, LP, FR, YD, XSCL, SHL, DOFF
I/O capacitance		$C_{I/O}$			—	—	15	pF	EIO1, EIO2

- **AC Characteristics**
  - **Input Timing**

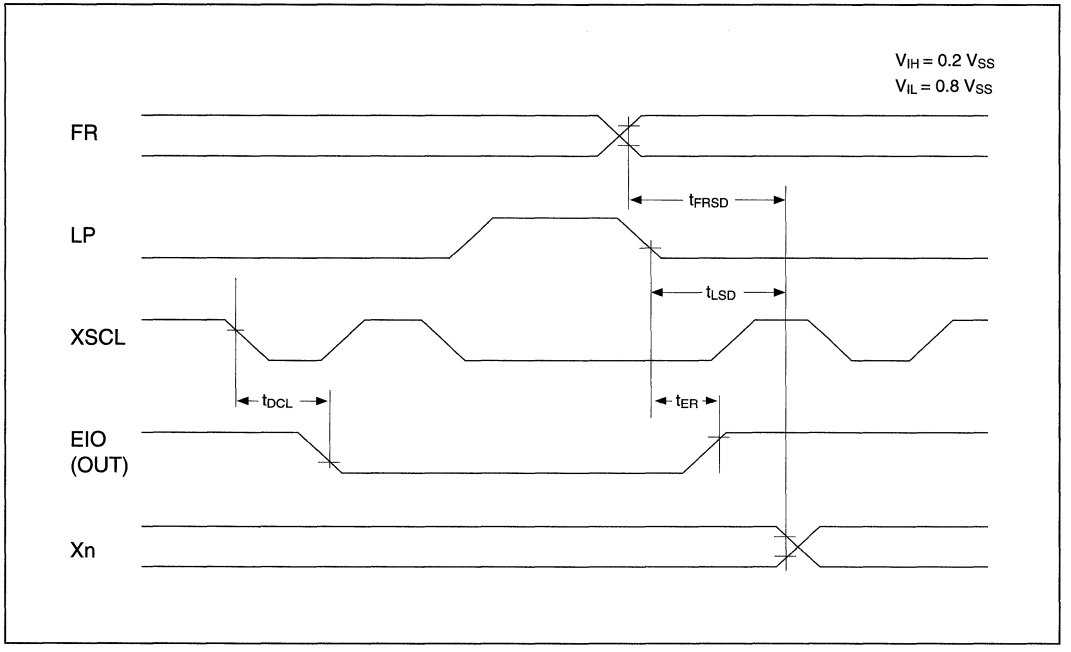


VSS = –5.5 to –2.7V, Ta = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
XSCL cycle time	tC		250	—	ns
XSCL high-level pulse width	tWCH		70	—	ns
XSCL low-level pulse width	tWCL		70	—	ns
Data setup time	tDS		50	—	ns
Data hold time	tDH		50	—	ns
XSCL ↓ → LP ↓	tLD		80	—	ns
LP ↓ → XSCL ↓	tLH		140	—	ns
LP high-level pulse width	tWLH		75	—	ns
LP low-level pulse width	tWLL		75	—	ns
FR phase difference	tDF		–300	+300	ns
EIO setup time	tSUE		50	—	ns
YD setup time	tYDS		80	—	ns
YD hold time	tYDH		80	—	ns
Rise/fall time	tr, tf		—	30	ns

* Recommended tWLH value ≈ tC

° **Output Timing**

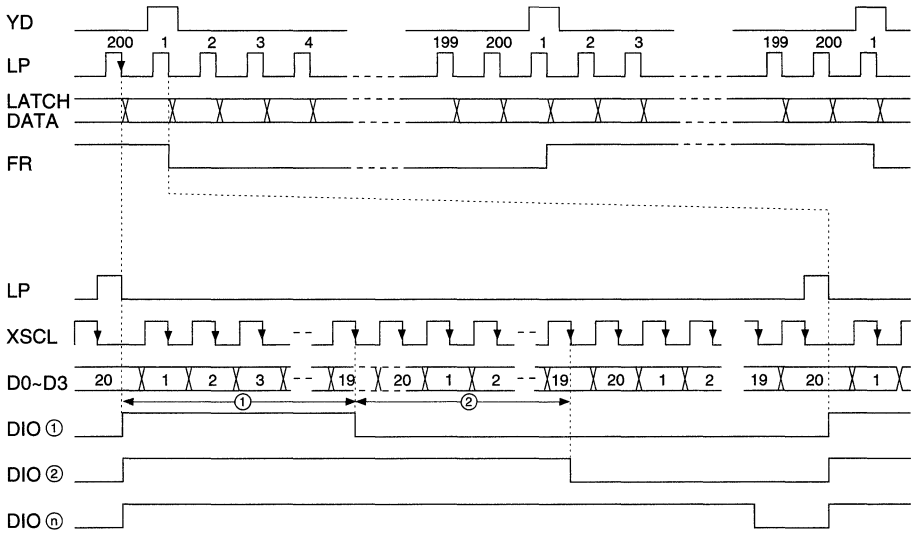


V_{DD} = –5.5 to –2.7V, V_{EE} = –8.0 to –20.0V, T_a = –40 to 85°C

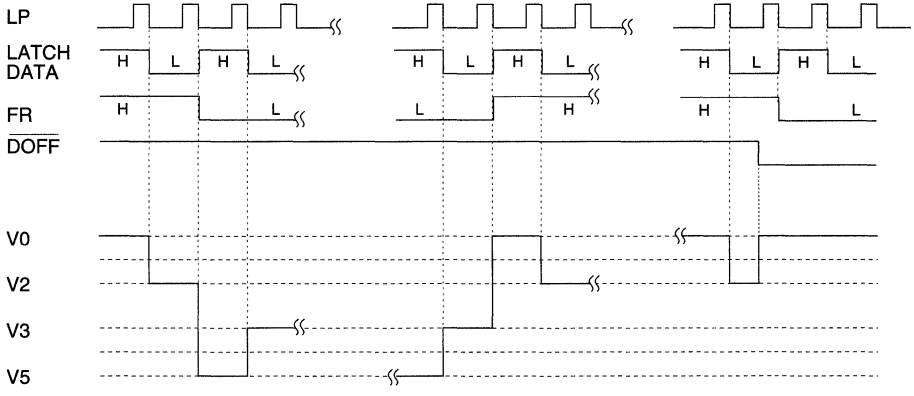
Parameter	Symbol	Conditions		Min	Max	Unit
EIO reset time	t_{ER}	C_L = 15pF (EIO)		—	150	ns
EIO output delay time	t_{DCL}		V_{SS} = –2.7V	—	95	ns
LP → Xn output delay time	t_{LSD}	C_L = 100pF		—	400	ns
FR → Xn output delay time	t_{FRSD}			—	400	ns

■ TIMING DIAGRAMS

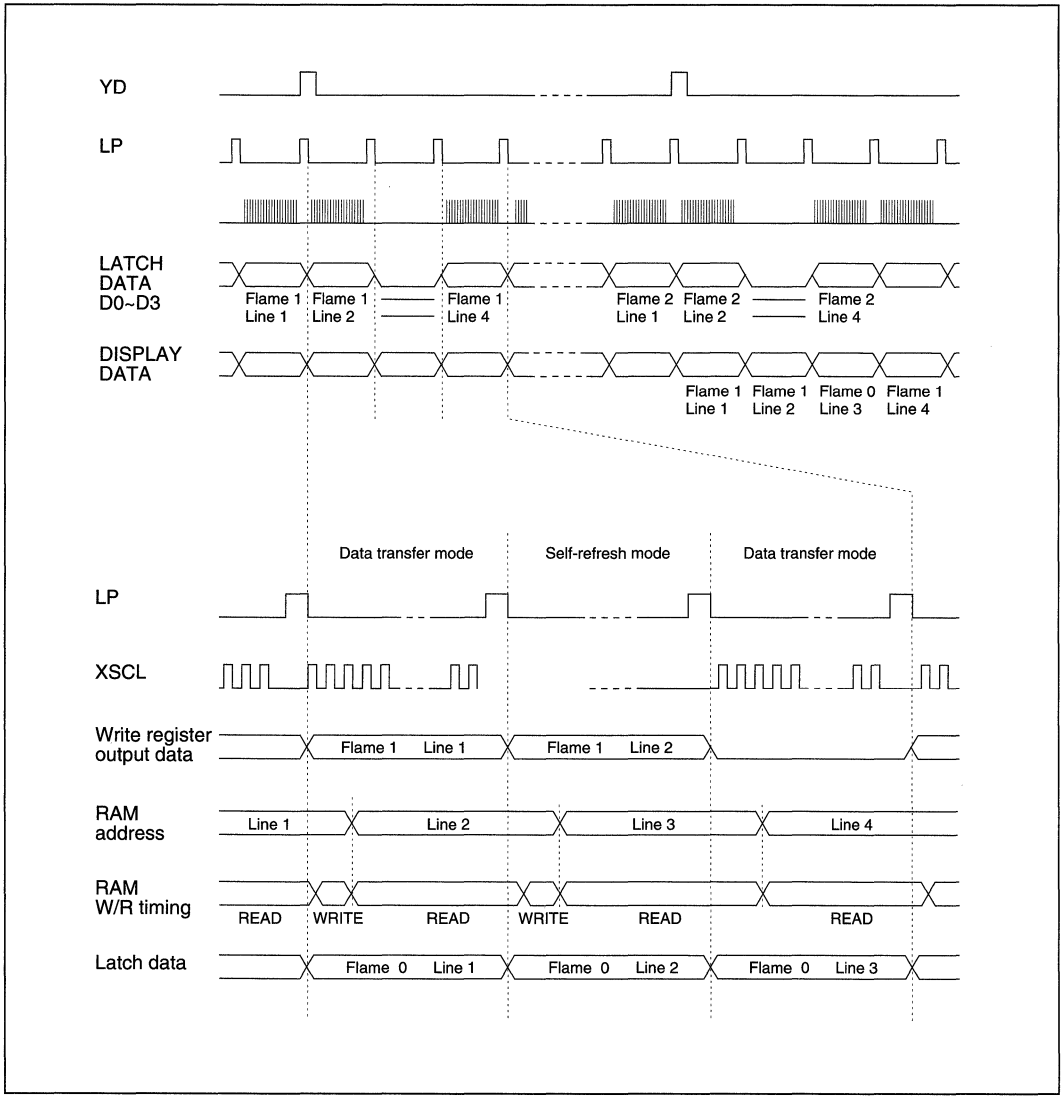
● Sample of 1/200 duty



① ~ ⓝ serial connection number of Driver IC



● **Self-Refresh Mode Timing**



■ SELF-REFRESH FUNCTION

● Setting Self-Refresh Mode

The self-refresh mode functions as follows:

If the displayed contents do not change, there is no transfer of the display data from the display controller to the SED1570. The SED1570 automatically detects this and power-down is displayed.

The SED1570 is set to the self-refresh mode by maintaining the shift clock (XSCLK) in the "L" level for 1 horizontal display period (LP signal cycle) after the row data for 1 line has been input. The SED1570 checks the mode (whether or not the mode is changed to the self-refresh mode) every 1 horizontal display period. During 1 horizontal display period in which XSCL stops working, the display data is not written into the SED1570 display RAM.

To stop XSCL, terminate display data (D0 ~ D3) transfer from the display controller (because of the power down), and set XSCL to "H" or "L". At this time, the display control must periodically send the LP, YD, and FR signals to the SED1570 the same way as when data is transferred. The SED1570 inputs these signals, reads the display data periodically from the internal display RAM and refreshes the display.

The display-off function is available in the self-refresh mode.

● Cancelling Self-Refresh Mode

The self-refresh mode is cancelled as follows:

The display controller inputs the shift clock (XSCL) into the SED1570 for one horizontal display period or longer. This should be down with the trailing edge of the LP signal and in the data transfer timing. After the mode is cancelled, the line data, which has been sent in the horizontal display period, is written in the display RAM at the time of the next trailing edge of the LP signal.

If the SED1570s are connected in cascade format, the self-refresh modes of all SED1570s are not cancelledunless the appropriate number of the XSCL clocks for the cascaded SED1570s are entered.

■ LCD DRIVER POWER SUPPLY

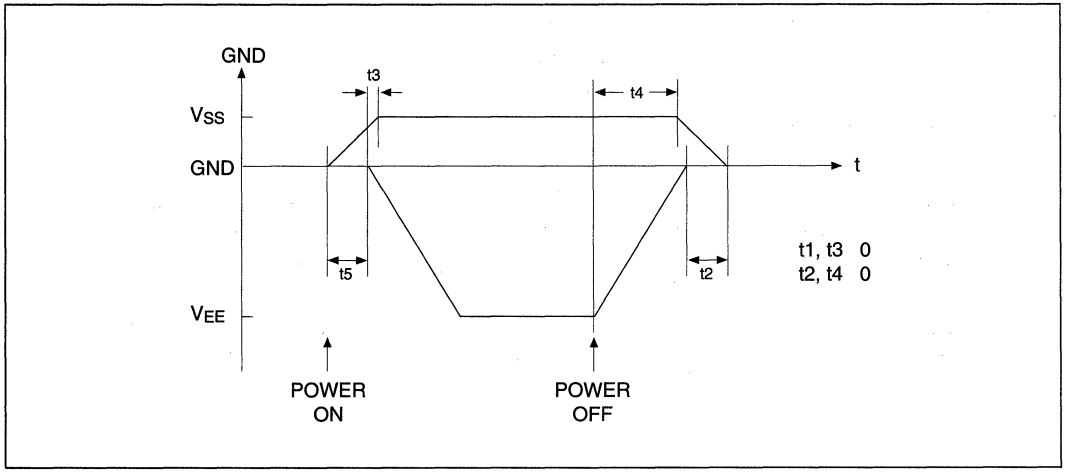
● Generating LCD Drive Voltages

To obtain individual voltage levels for LCD driver, register-split the potential between V5 – V_{DD} and drive the LCD with the voltage follower using the operation amplifier. When using an operation amplifier, V0 and V_{DD} are separated.

However, if the potential of V0 is lower than V_{DD} potential and the potential difference increases, the LCD driver capability decreases. To avoid this, set V_{DD} and V0 within the range between 0V and 2.5V. If an operation amplifier is not used, connect V0 and V_{DD}.

If there are direct resistors on the V5 (V_{DD}) power line, voltage falls in V5 (V_{DD}) at the LSI power pins. This is caused by I5 at the time of signal change. As a result, the relationship ($V_{DD} \geq V0 \geq V2 \geq V3 \geq V5 \geq V_{EE}$) for intermediate potential of LCD cannot be maintained and the LSI may be damaged.

To insert a protective resistor, the voltage must be stabilized according to the capacity.



● System Power-Up

This LSI has high-LCD drive voltage. As a result, if the logic power is being floated and high voltage is applied in the LCD driver, the LSI may be damaged because of the excess current.

Until the LCD drive voltage is stabilized, use the display off function ($\overline{DOFF}$) to set the potential of the LCD drive output to V0 level.

Follow the sequence given below when turning the power on/off.

To turn on the power:

- Turn on the logic power.

→ Turn the LCD driver on.
(or turn them on simultaneously)

To turn off the power:

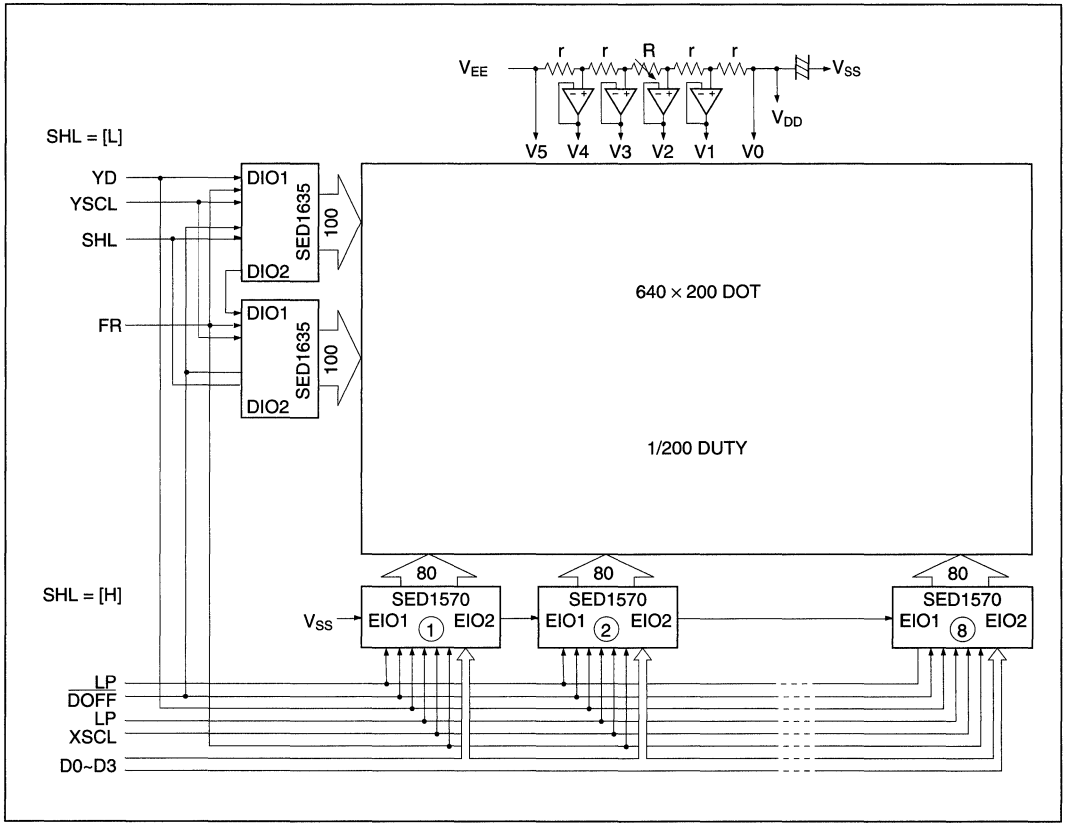
- Turn off the LCD driver.

→ Turn off the logic power.
(or turn them off simultaneously)

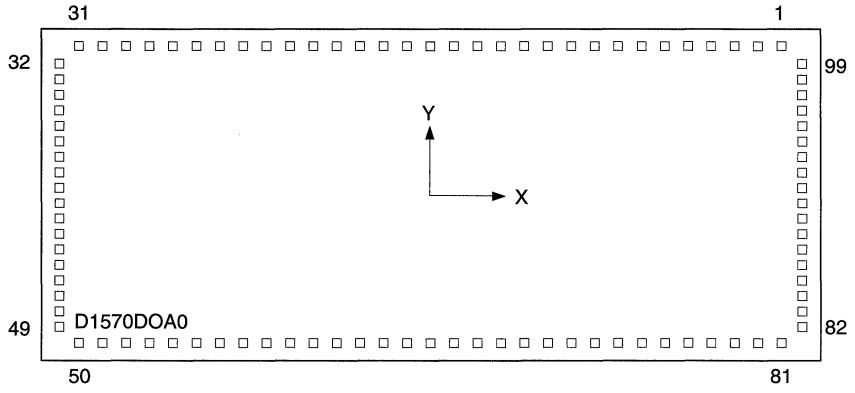
To avoid excess current, insert the high-speed fuse in series with the LCD power. Select the appropriate value for a protective resistor according to the capacity of an LCD cell.

■ EXAMPLE OF APPLICATION

● Constitution of LCD



■ PAD DIMENSIONS



Chip size ..... 8.04 mm × 3.51 mm

Pad center size ..... 100 μm × 100 μm

Pad pitch ..... 170 μm (min.)

Chip thickness ..... 400 μm ± 25 μm (Al pad)

■ PAD COORDINATES

● SED1570F Pad Center Coordinates

Pad No.	Pin Name	X	Y
1	X75	3640	1595
2	X76	3432	1595
3	X77	3224	1595
4	X78	3016	1595
5	X79	2808	1595
6	X80	2600	1595
7	EIO2	2340	1595
8	V_{DD}	2080	1595
9	SHL	1820	1595
10	D0	1560	1595
11	D1	1300	1595
12	D2	1040	1595
13	D3	780	1595
14	YD	520	1595
15	V_{EE}	260	1595
16	V5	0	1595
17	V3	–260	1595
18	V2	–520	1595
19	V0	–780	1595
20	FR	–1040	1595
21	XSCL	–1300	1595
22	$\overline{DOFF}$	–1560	1595
23	LP	–1820	1595
24	VSS	–2080	1595
25	EIO1	–2340	1595
26	X1	–2600	1595
27	X2	–2808	1595
28	X3	–3016	1595
29	X4	–3224	1595
30	X5	–3432	1595
31	X6	–3640	1595
32	X7	–3862	1452
33	X8	–3862	1282
34	X9	–3862	1112
35	X10	–3862	942
36	X11	–3862	772
37	X12	–3862	602
38	X13	–3862	432
39	X14	–3862	262
40	X15	–3862	92
41	X16	–3862	–78
42	X17	–3862	–248
43	X18	–3862	–418
44	X19	–3862	–588
45	X20	–3862	–758
46	X21	–3862	–928
47	X22	–3862	–1098
48	X23	–3862	–1268
49	X24	–3862	–1438
50	X25	–3641	–1595
51	X26	–3406	–1595
52	X27	–3171	–1595
53	X28	–2936	–1595
54	X29	–2701	–1595
55	X30	–2466	–1595
56	X31	–2231	–1595
57	X32	–1996	–1595
58	X33	–1761	–1595
59	X34	–1526	–1595
60	X35	–1291	–1595
61	X36	–1056	–1595
62	X37	–821	–1595
63	X38	–586	–1595
64	X39	–351	–1595
65	X40	–116	–1595
66	X41	119	–1595
67	X42	354	–1595
68	X43	589	–1595
69	X44	824	–1595
70	X45	1059	–1595
71	X46	1294	–1595
72	X47	1530	–1595
73	X48	1765	–1595
74	X49	2000	–1595
75	X50	2235	–1595
76	X51	2470	–1595
77	X52	2705	–1595
78	X53	2940	–1595
79	X54	3175	–1595
80	X55	3410	–1595
81	X56	3645	–1595
82	X57	3862	–1438
83	X58	3862	–1268
84	X59	3862	–1098
85	X60	3862	–928
86	X61	3862	–758
87	X62	3862	–588
88	X63	3862	–418
89	X64	3862	–248
90	X65	3862	–78
91	X66	3862	92
92	X67	3862	262
93	X68	3862	432
94	X69	3862	602
95	X70	3862	772
96	X71	3862	942
97	X72	3862	1112
98	X73	3862	1282
99	X74	3862	1452

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CMOS 80-SEGMENT LCD DRIVER

- **80-bit High Voltage Output**
- **1/100 to 1/300 Display Duty**

■ DESCRIPTION

The SED1600 is a dot matrix LCD segment (column) driver for driving a high-capacity LCD panel at duty cycles higher than 1/100 (up to 1/300). The LSI has a wide range of LCD driving voltages. Due to the architecture of the SED1600, the LCD driving voltage, V0, is isolated from the V_{DD} supply. This provides the ability to adjust the offset bias independently of V_{DD}. These unique features allow the SED1600 to interface with a variety of LCD panels. The SED1600 does not require a controller to output an enable signal to implement daisy chain technology. This provides for easy interfacing with the LCD controllers such as the SED1330, SED1351, SED1335, or the SED1341.

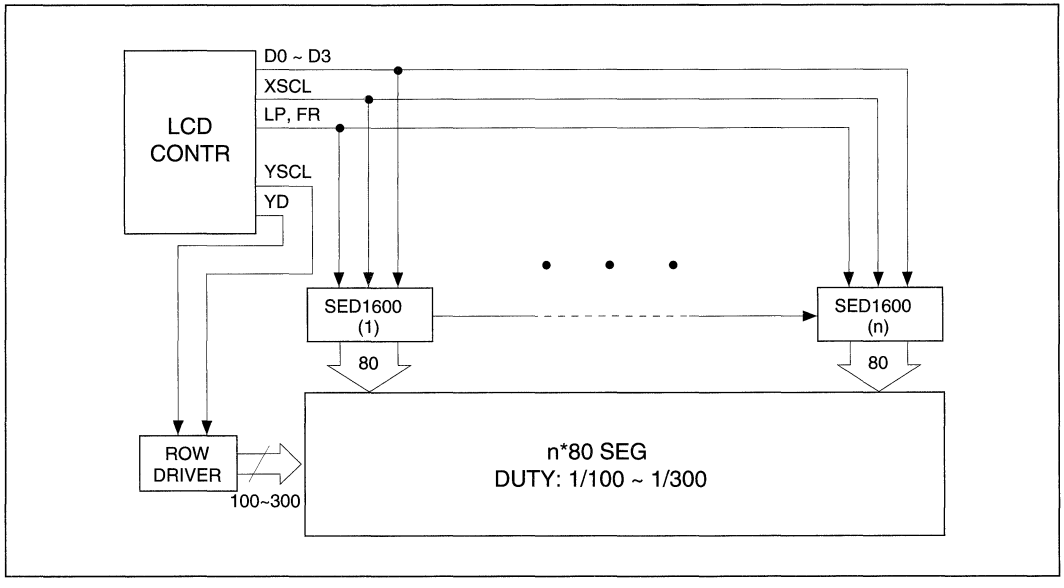
The SED1600 is used in conjunction with the SED1610 (86-row driver), SED1630 (68-bit row driver), SED1631 (100-row driver), SED1632 (86-bit row driver), SED1633 (100-bit row driver), and SED1634 (100-bit driver) to drive a large-capacity dot matrix LCD panel.

■ FEATURES

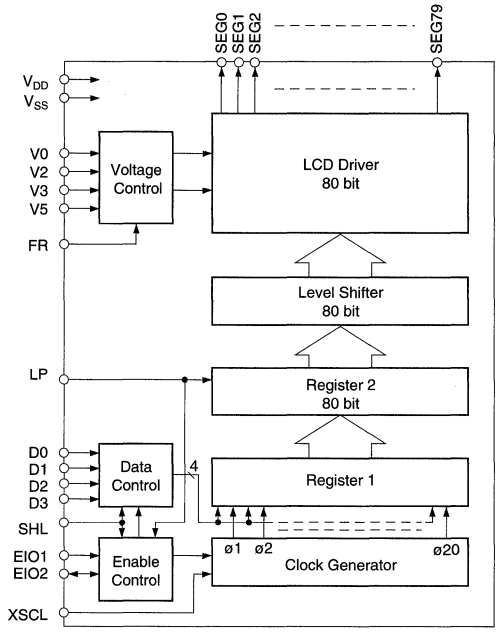
- Low-power CMOS technology
- 80-bit segment (column) driver
- High-speed 4-bit data bus with enable chain technology
- Duty cycle ..... 1/100 to 1/300
- Shift clock frequency ..... 6MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Daisy chain enable support
- Selectable output shift direction
- No enable signal by controller is required
- Wide range of LCD voltage .... –12 to –28V
- Supply voltage ..... 5.0V ± 10%
- Package ..... QFP5-100 pin (F_{AA})

  DIE: Al pad chip (D_{AA})
  Au bump (D_{AB})

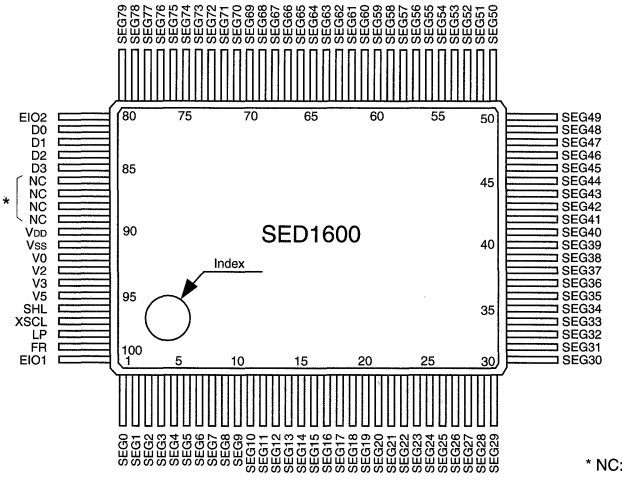
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



* NC: No Connection

■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>SEG0 to SEG79</td><td>O</td><td>LCD driving segment (column) outputs
Each output changes at the falling edge of LP.</td></tr>
<tr><td>D0 TO D3</td><td>I</td><td>Display data inputs.</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock of display data (falling edge trigger).</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse of display data (falling edge trigger).</td></tr>
<tr><td>EI01, EI02</td><td>I/O</td><td>Enable I/O, which is controlled by SHL input . Output is reset by LP, and automatically falls when 80 bits of data are taken in.</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO pin I/O control.
When data (a, b, c, d) (e, f, g, h)·····(w, x, y, z) are input to pins (D3, D2, D1, D0) respectively, the following relation is established between the data and segment outputs:
<table>
<tr><th rowspan="2">SHL</th><th colspan="12">SEG</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>74</th><th>73</th><th>72</th><th>.....</th><th>3</th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>.....</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>.....</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table></td></tr>
<tr><td>FR</td><td>I</td><td>AC signal of LCD driving outputs.</td></tr>
<tr><td>VDD, VSS</td><td>Power Supplies</td><td>Logic circuit power.
VDD: 0 V (GND)
VSS: –5.0 V</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power Supplies</td><td>LCD driving power.
V5: –12 to –28 V
VDD ≥ V0 ≥ V2 > V3 ≥ V5</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(VDD = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	VSS	–7.0 to +0.3	V
Supply voltage (2)	V5	–30.0 to +0.3	V
Supply voltage (2)	V0, V2, V3*	V5 –0.3 to +0.3	V
Input voltage (1)	VI	VSS –0.3 to +0.3	V
Output voltage (1)	VO	VSS –0.3 to +0.3	V
Output current (1)	IO	20	mA
Output current (2)	IOSEG	20	mA
Allowable power dissipation	PD	300	mW
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–65 to +150	°C
Soldering temperature, time	Tsol	260°C, 10 sec (at lead)	—

* V0, V2 and V3 must always satisfy the condition VDD ≥ V0 ≥ V2 ≥ V3 ≥ V5.

● DC Electrical Characteristics

(Unless otherwise specified, V_{DD} = V0 = 0V, V_{SS} = –5.0 V ± 10%, T_a = –20 to 85°C)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Operating voltage	V_{SS}		V_{SS}	–5.5	–5.0	–4.5	V
Recommended op. voltage Minimum operating voltage	V5		V5	–28.0	—	–12.0 –8.0	V
Operating voltage	—	Recommended value	V0	–2.5	—	0	V
Operating voltage	V2	Recommended value	V2	3/9·V5	—	V0	V
Operating voltage	V3	Recommended value	V3	V5	—	6/9·V5	V
"H" input voltage	V_{IH}		EI01, EI02, XSCL, LP, D0 to D3, FR, SHL	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}			—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH} = –0.6 mA	EI01, EI02	–0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_I \le 0$ V	D0 to D3, LP XSCL, SHL, FR	—	—	2.0	µA
	$I_{LI/O}$	$V_{SS} \le V_I \le 0$ V	EI01, EI02	—	—	5.0	µA
Stand–by current	I_{DDS}	V5 = –12.0 to –28.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{SEG}	|ΔVon| = 0.5V, V5 = –20.0V	SEG0 to SEG79	—	1.5	3.5	kΩ
		|ΔVon| = 0.5V, V5 = –14.0V		—	2.0	4.5	kΩ
		|ΔVon| = 0.5V, V5 = –8.0V		—	3.0	8.0	kΩ
Current dissipation (1)	I_{SSO1}	V_{SS} = –5.0 V, V_{IH} = V_{DD} V_{IL} = V_{SS}, f_{XSCL} =1.92 MHz f_{LP} = 12 kHz, Frame period = 60 Hz; Input data: Inverted bit by bit, No-load	V_{SS}	—	120	500	µA
Current dissipation (2)	I_{SSO2}	V_{SS} = –5.0 V, V2 = –4.0 V V3 = –16.0 V, V5 = –20.0 V All other conditions are same as I_{SSO1}	V5	—	20	100	µA
Input capacitance	C_I	T_a = 25°C	D0 to D3, LP XSCL, SHL, FR	—	—	8.0	pF
	$C_{I/O}$		EI01, EI02	—	—	15.0	pF

● AC Electrical Characteristics

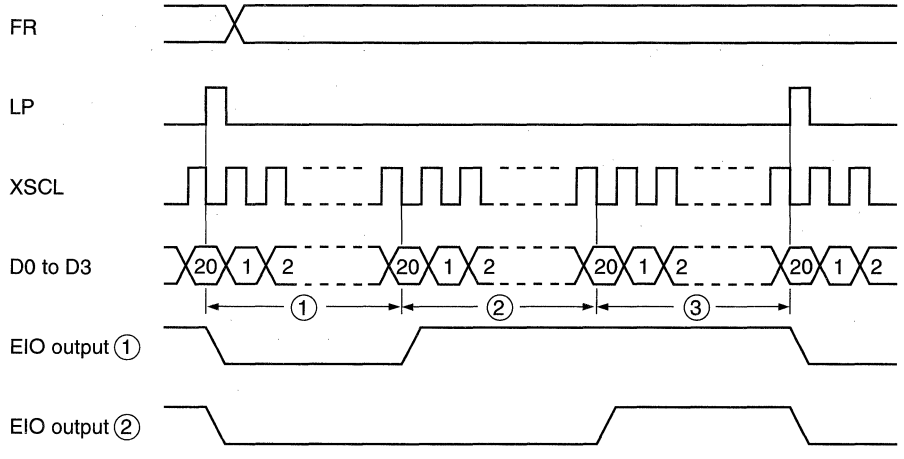
(V_{SS} = –5.0 V ±10%, T_a = –20 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XSCL period	t_{CCL}	t_r, $t_f \leq$ 10 ns	166	—	—	ns
XSCL "H" pulse width	t_{WCLH}		70	—	—	ns
XSCL "L" pulse width	t_{WCLL}		70	—	—	ns
Data setup time	t_{DS}		60	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
XSCL-rise to LP-rise time	t_{LD}		0	—	—	ns
XSCL-fall to LP-fall time	t_{SL}		70	—	—	ns
LP-rise to XSCL-rise time	t_{LS}		70	—	—	ns
LP-fall to XSCL-fall time	t_{LH}		70	—	—	ns
LP "H" pulse width	t_{WLPH}		70	—	—	ns
LP "L" pulse width	t_{WLPL}		230	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns
Enable "H" setup time	t_{suEIH}		40	—	—	ns
Enable "H" hold time	t_{hEIH}		0	—	—	ns
Enable "L" setup time	t_{suEIL}		0	—	—	ns
Enable "L" hold time	t_{hEIL}		0	—	—	ns
Input signal rise time	t_r		—	—	50*	ns
Input signal fall time	t_f		—	—	50*	ns

* Note: The specifications for t_r and t_f are provided to prevent a malfunction which may occur when noise is mixed with a slow-down signal. To assure high-speed XSCL, both t_r and t_f must satisfy the following relation:

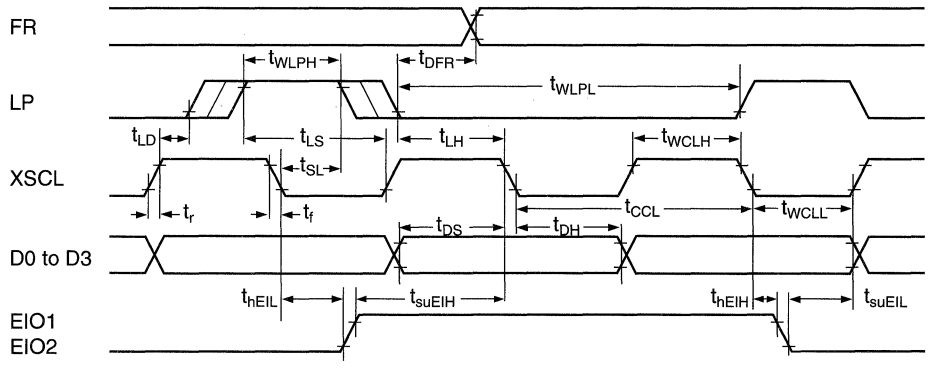
$$t_r, t_f < \frac{t_{CCL} - (t_{WCLH} + t_{WCLL})}{2}$$

● **Timing Chart**
○ **Input Timing**

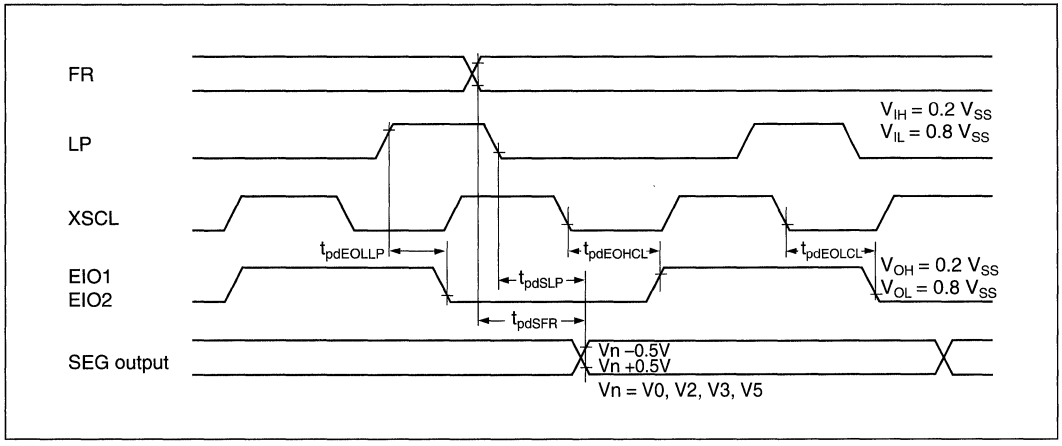


①through③each show a cascade number of the driver.

$V_{IH} = 0.2\ V_{SS}$
$V_{IL} = 0.8\ V_{SS}$



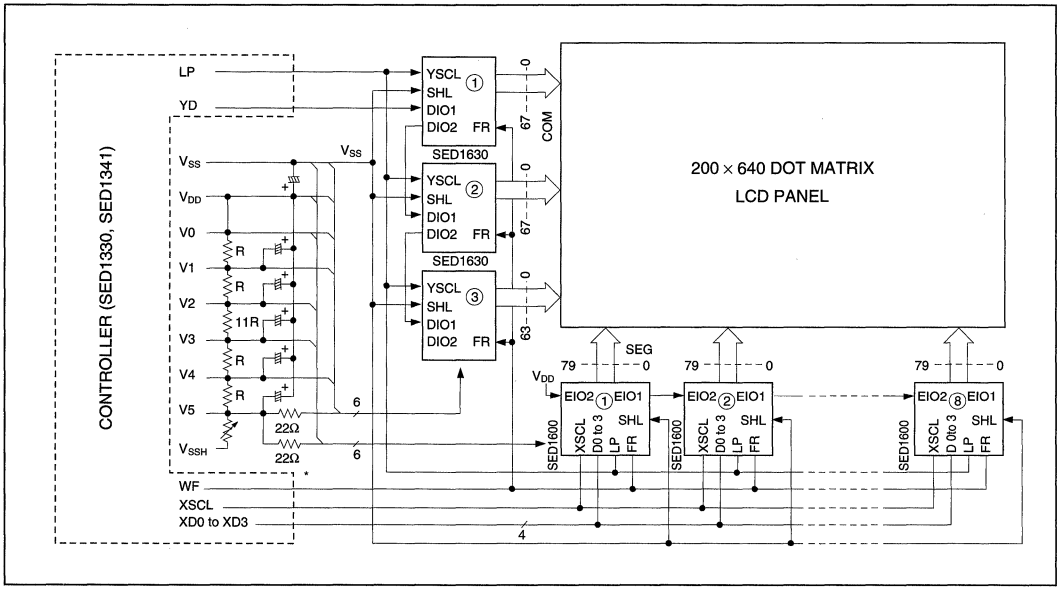
○ **Output Timing**



(V_{SS} = –5.0 V ±10%, T_a = –20 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(LP-rise to disable) time	$t_{pdEOLLP}$	XSCL = "L"	—	—	70	ns
(XSCL-fall to disable) time	$t_{pdEOLCL}$	LP = "H" C_L = 15 pF	—	—	70	ns
(XSCL-fall to enable) time	$t_{pdEOHCL}$		—	—	100	ns
(LP-fall to SEG output) time	t_{pdSLP}	V5 = –12.0 to –28.0 V	—	—	4.5	µs
(FR to SEG output) delay time	t_{pdSFR}	C_L = 100 pF	—	—	4.5	µs

■ EXAMPLE OF APPLICATION (SED1600) (for 200 × 640 DOT MATRIX LCD)

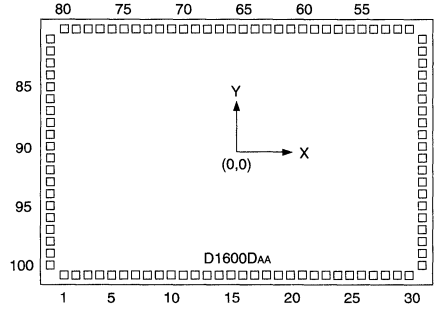


Note:

* Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01μF) near pins Vss and V5 of each LSI for noise protection.

■ PAD LAYOUT / PAD COORDINATION

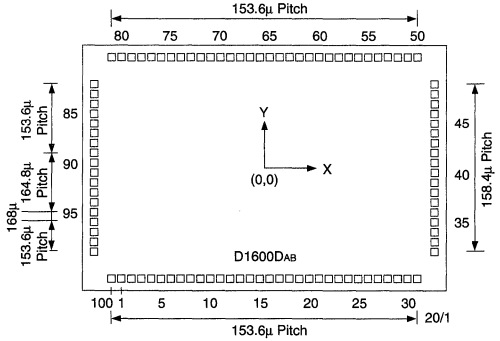
● SED1600DAA (AL PAD)



Chip Specification	Dimension (mm)
Chip size	5.59 × 3.50
Pad pitch	0.160 min.
Chip thickness	0.40 ±0.025
Pad surface area	0.10mm

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	SEG0	–2461	–1588	35	SEG34	2632	–881	69	SEG68	–560	1588
2	SEG1	–2261	–1588	36	SEG35	2632	–721	70	SEG69	–720	1588
3	SEG2	–2069	–1588	37	SEG36	2632	–561	71	SEG70	–880	1588
4	SEG3	–1886	–1588	38	SEG37	2632	–401	72	SEG71	–1040	1588
5	SEG4	–1709	–1588	39	SEG38	2632	–241	73	SEG72	–1203	1588
6	SEG5	–1538	–1588	40	SEG39	2632	–81	74	SEG73	–1366	1588
7	SEG6	–1366	–1588	41	SEG40	2632	79	75	SEG74	–1538	1588
8	SEG7	–1203	–1588	42	SEG41	2632	239	76	SEG75	–1709	1588
9	SEG8	–1040	–1588	43	SEG42	2632	399	77	SEG76	–1885	1588
10	SEG9	–880	–1588	44	SEG43	2632	559	78	SEG77	–2069	1588
11	SEG10	–720	–1588	45	SEG44	2632	719	79	SEG78	–2261	1588
12	SEG11	–560	–1588	46	SEG45	2632	879	80	SEG79	–2461	1588
13	SEG12	–400	–1588	47	SEG46	2632	1039	81	EI02	–2632	1546
14	SEG13	–240	–1588	48	SEG47	2632	1204	82	D0	–2632	1372
15	SEG14	–80	–1588	49	SEG48	2632	1372	83	D1	–2632	1204
16	SEG15	80	–1588	50	SEG49	2632	1546	84	D2	–2632	1039
17	SEG16	240	–1588	51	SEG50	2461	1588	85	D3	–2632	879
18	SEG17	400	–1588	52	SEG51	2261	1588	86	(D4)	–2632	719
19	SEG18	560	–1588	53	SEG52	2069	1588	87	(D5)	–2632	559
20	SEG19	720	–1588	54	SEG53	1885	1588	88	(D6)	–2632	399
21	SEG20	880	–1588	55	SEG54	1709	1588	89	(D7)	–2632	239
22	SEG21	1040	–1588	56	SEG55	1538	1588	90	VDD	–2632	79
23	SEG22	1203	–1588	57	SEG56	1366	1588	91	VSS	–2632	–81
24	SEG23	1366	–1588	58	SEG57	1203	1588	92	V0	–2632	–241
25	SEG24	1538	–1588	59	SEG58	1040	1588	93	V2	–2632	–401
26	SEG25	1709	–1588	60	SEG59	880	1588	94	V3	–2632	–561
27	SEG26	1885	–1588	61	SEG60	720	1588	95	V5	–2632	–721
28	SEG27	2069	–1588	62	SEG61	560	1588	96	SHL	–2632	–881
29	SEG28	2261	–1588	63	SEG62	400	1588	97	XSCL	–2632	–1041
30	SEG29	2461	–1588	64	SEG63	240	1588	98	LP	–2632	–1206
31	SEG30	2632	–1548	65	SEG64	80	1588	99	FR	–2632	–1374
32	SEG31	2632	–1374	66	SEG65	–80	1588	100	EI01	–2632	–1548
33	SEG32	2632	–1206	67	SEG66	–240	1588				
34	SEG33	2632	–1040	68	SEG67	–400	1588				

● SED1600DAB (AU PAD)



Chip Specification	Dimension (mm)
Chip size	5.59 × 3.50
Pad pitch	0.153 min.
Chip thickness	0.525 ±0.025

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	SEG0	–2227	–1578	35	SEG34	2622	–871	69	SEG68	–538	1578
2	SEG1	–2074	–1578	36	SEG35	2622	–713	70	SEG69	–691	1578
3	SEG2	–1920	–1578	37	SEG36	2622	–554	71	SEG70	–845	1578
4	SEG3	–1766	–1578	38	SEG37	2622	–396	72	SEG71	–998	1578
5	SEG4	–1613	–1578	39	SEG38	2622	–238	73	SEG72	–1152	1578
6	SEG5	–1459	–1578	40	SEG39	2622	–79	74	SEG73	–1305	1578
7	SEG6	–1305	–1578	41	SEG40	2622	79	75	SEG74	–1459	1578
8	SEG7	–1152	–1578	42	SEG41	2622	238	76	SEG75	–1613	1578
9	SEG8	–998	–1578	43	SEG42	2622	396	77	SEG76	–1766	1578
10	SEG9	–845	–1578	44	SEG43	2622	554	78	SEG77	–1920	1578
11	SEG10	–691	–1578	45	SEG44	2622	713	79	SEG78	–2074	1578
12	SEG11	–538	–1578	46	SEG45	2622	871	80	SEG79	–2227	1578
13	SEG12	–384	–1578	47	SEG46	2622	1030	81	EI02	–2381	1578
14	SEG13	–230	–1578	48	SEG47	2622	1188	82	D0	–2622	1346
15	SEG14	–77	–1578	49	SEG48	2622	1346	83	D1	–2622	1193
16	SEG15	77	–1578	50	SEG49	2381	1578	84	D2	–2622	1039
17	SEG16	230	–1578	51	SEG50	2227	1578	85	D3	–2622	886
18	SEG17	384	–1578	52	SEG51	2074	1578	86	(D4)	–2622	732
19	SEG18	538	–1578	53	SEG52	1920	1578	87	(D5)	–2622	578
20	SEG19	691	–1578	54	SEG53	1766	1578	88	(D6)	–2622	425
21	SEG20	845	–1578	55	SEG54	1613	1578	89	(D7)	–2622	271
22	SEG21	998	–1578	56	SEG55	1459	1578	90	VDD	–2622	106
23	SEG22	1152	–1578	57	SEG56	1305	1578	91	VSS	–2622	–58
24	SEG23	1305	–1578	58	SEG57	1152	1578	92	V0	–2622	–223
25	SEG24	1459	–1578	59	SEG58	998	1578	93	V2	–2622	–388
26	SEG25	1613	–1578	60	SEG59	845	1578	94	V3	–2622	–553
27	SEG26	1766	–1578	61	SEG60	691	1578	95	V5	–2622	–718
28	SEG27	1920	–1578	62	SEG61	538	1578	96	SHL	–2622	–886
29	SEG28	2074	–1578	63	SEG62	384	1578	97	XSCL	–2622	–1039
30	SEG29	2227	–1578	64	SEG63	230	1578	98	LP	–2622	–1193
31	SEG30	2381	–1578	65	SEG64	77	1578	99	FR	–2622	–1346
32	SEG31	2622	–1346	66	SEG65	–77	1578	100	EI01	–2381	–1578
33	SEG32	2622	–1188	67	SEG66	–230	1578				
34	SEG33	2622	–1030	68	SEG67	–384	1578				

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CMOS DOT MATRIX HIGH DUTY LCD DRIVER

- **80-bit High Voltage Resistant Output**
- **1/100 to 1/300 in Display Duty**
- **CMOS High Voltage Resistant Process**

■ DESCRIPTION

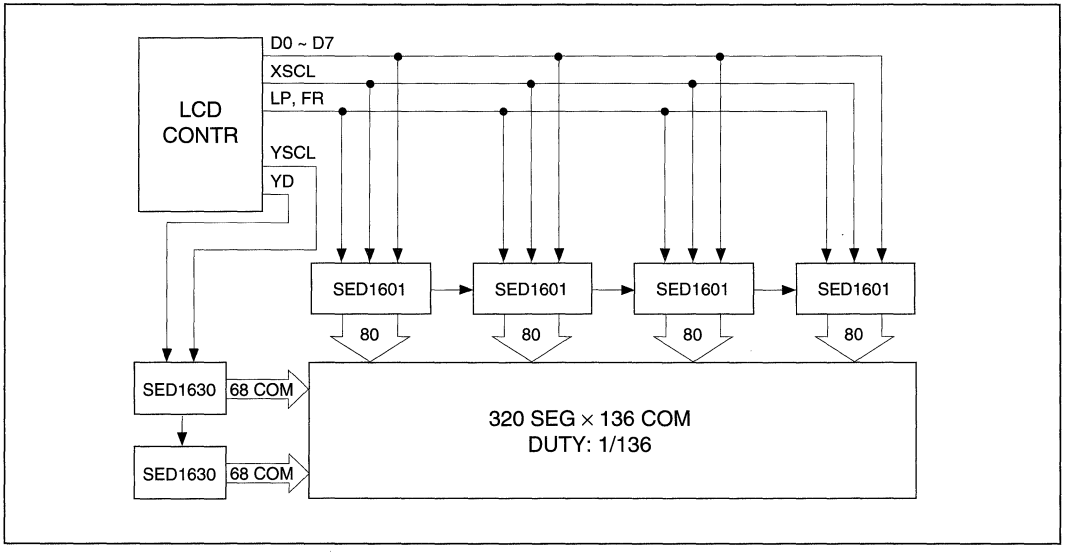
The SED1601 is an 80-output dot matrix LCD segment (column) driver for driving a high-capacity LCD panel at duty cycles higher than 1/100 (up to 1/300). The LSI has a wide range of the LCD driving voltages. Due to the architecture of the SED1601, the LCD driving voltage, V0, is isolated from V_{DD} supply. This provides the ability to adjust the offset bias independently of V_{DD}. These unique features allow the SED1601 to interface with a variety of LCD panels. The SED1601 does not require a controller to output an enable signal to implement daisy chain technology. This provides for easy interfacing with LCD controllers such as the SED1330, SED1351, SED1335 or the SED1341.

The SED1601 is used in conjunction with the SED1610 (86 row driver) or the SED1630 (68-bit row driver) and SED1631 (100 row driver) or the SED1632 (86-bit row driver), SED1633 (100-bit row driver) and SED1634 (100-bit row driver) to drive a large-capacity dot matrix LCD panel.

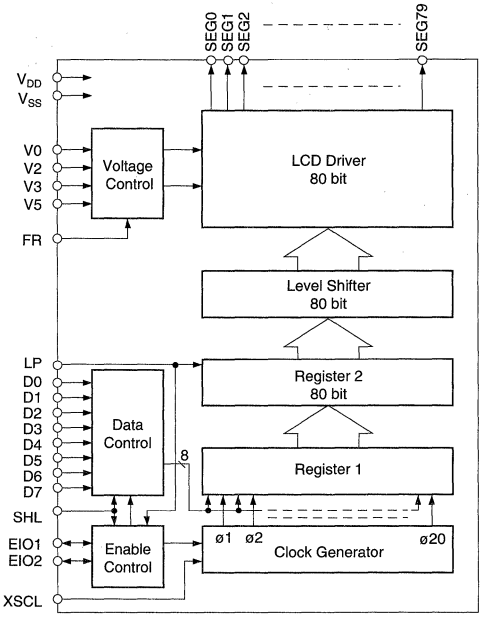
■ FEATURES

- Low-power CMOS technology
- 80-bit segment (column) driver
- High-speed 8-bit bus
- Duty cycle ..... 1/100 to 1/300
- Output shift direction pin selectable
- Shift clock frequency ..... 6.5MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Daisy chain enable support
- No enable signal by controller is required
- Wide range of LCD voltage .... –12V to –28V
- Supply voltage ..... 5.0V ± 10%
- Package ..... QFP5-100 pin (FAA)
  DIE: Al pad chip (DAA)

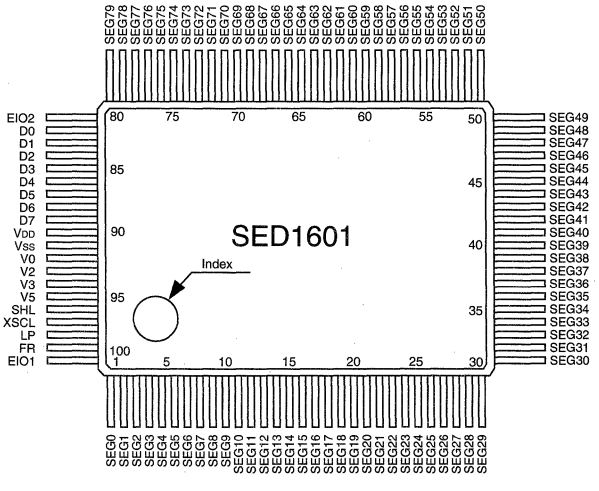
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>SEG0 to SEG79</td><td>O</td><td>LCD driving segment (column) outputs.
Each output changes at the falling edge of LP.</td></tr>
<tr><td>D0 TO D7</td><td>I</td><td>Display data inputs.</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock of display data (falling edge trigger).</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse of display data (falling edge trigger).</td></tr>
<tr><td>EI01, EI02</td><td>I/O</td><td>Enable I/O, which is controlled by SHL input. Output is reset by LP, and automatically falls when 80 bits of data are taken in.</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO pin I/O control.
When data (a, b, c, d, e, f, g, h) (i, j, k, l, m, n, o, p)·····(s, t, u, v, w, x, y, z) are input to pins (D7, D6, D5, D4, D3, D2, D1, D0) respectively, the following relation is established between the data and segment outputs:
<table>
<tr><th rowspan="2">SHL</th><th colspan="12">SEG</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>74</th><th>73</th><th>72</th><th>.....</th><th>3</th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>.....</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>.....</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Intput</td><td>Output</td></tr>
</table></td></tr>
<tr><td>FR</td><td>I</td><td>AC signal of LCD driving outputs.</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power Supplies</td><td>Logic circuit power.
V_{DD}: 0 V (GND)
V_{SS}: –5.0 V</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power Supplies</td><td>LCD driving power.
V5: –12 to –28 V
$V_{DD} \geq V0 \geq V2 > V3 \geq V5$</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V5	–30.0 to +0.3	V
Supply voltage (2)	V0, V2, V3*	V5 –0.3 to +0.3	V
Input voltage (1)	V_I	V_{SS} –0.3 to +0.3	V
Output voltage (1)	V_O	V_{SS} –0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OSEG}	20	mA
Allowable power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature, time	T_{sol}	260°C, 10 s (at lead)	—

* V0, V2 and V3 must always satisfy the condition: $V_{DD} \geq V0 \geq V2 \geq V3 \geq V5$.

● DC Electrical Characteristics

(Unless otherwise specified, V_{DD} = V0 = 0V, V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Operating voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–4.5	V
Recommended op. voltage Minimum operating voltage	V5		V5	–28.0	—	–12.0 –8.0	V
Operating voltage (2)	V0	Recommended value	V0	–2.5	—	0	V
Operating voltage (3)	V2	Recommended value	V2	5/9·V5	—	V0	V
Operating voltage (4)	V3	Recommended value	V3	V5	—	4/9·V5	V
"H" input voltage	V_{IH}		EI01, EI02, XSCL, LP, D0 to D7, FR, SHL	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}			—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH} = –0.6 mA	EI01, EI02	–0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_I \le 0$ V	D0 to D7, LP XSCL, SHL, FR	—	—	2.0	µA
	$I_{LI/O}$	$V_{SS} \le V_I \le 0$ V	EI01, EI02	—	—	5.0	µA
Stand-by current	I_{DDS}	V5 = –12.0 to –28.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{SEG}	|ΔVon| = 0.5V, V5 = –20.0V	SEG0 to SEG79	—	1.4	3.5	kΩ
		|ΔVon| = 0.5V, V5 = –14.0V		—	1.7	4.5	
		|ΔVon| = 0.5V, V5 = –8.0V		—	2.7	8.0	
Current dissipation (1)	I_{SSO1}	V_{SS} = –5.0 V, V_{IH} = V_{DD} V_{IL} = V_{SS}, f_{XSCL} = 1.92 MHz f_{LP} = 12 kHz, Frame period = 60 Hz; Input data: Inverted bit by bit; No-load	V_{SS}	—	120	500	µA
Current dissipation (2)	I_{SSO2}	V_{SS} = –5.0 V, V2 = –4.0 V V3 = –16.0 V, V5 = –20.0 V All other conditions are same as I_{SSO1}	V5	—	20	100	µA
Input capacitance	C_I	T_a = 25°C	D0 to D7, LP XSCL, SHL, FR	—	—	8.0	pF
	$C_{I/O}$		EI01, EI02	—	—	15.0	pF

● AC Electrical Characteristics

(V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

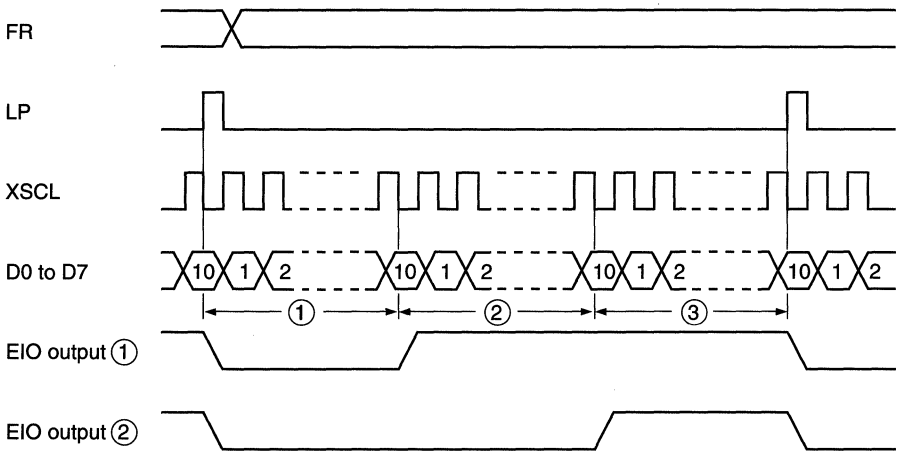
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XSCL period	t_{CCL}	t_r, $t_f \leq$ 10 ns	166	—	—	ns
XSCL "H" pulse width	t_{WCLH}		70	—	—	ns
XSCL "L" pulse width	t_{WCLL}		70	—	—	ns
Data setup time	t_{DS}		60	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
XSCL-rise to LP-rise time	t_{LD}		0	—	—	ns
XSCL-fall to LP-fall time	t_{SL}		70	—	—	ns
LP-rise to XSCL-rise time	t_{LS}		70	—	—	ns
LP-fall to XSCL-fall time	t_{LH}		70	—	—	ns
LP "H" pulse width	t_{WLPH}		70	—	—	ns
LP "L" pulse width	t_{WLPL}		230	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns
Enable "H" setup time	t_{suEIH}		40	—	—	ns
Enable "H" hold time	t_{hEIH}		0	—	—	ns
Enable "L" setup time	t_{suEIL}		0	—	—	ns
Enable "L" hold time	t_{hEIL}		0	—	—	ns
Input signal rise time	t_r		—	—	50*	ns
Input signal fall time	t_f		—	—	50*	ns

*** Note:**

The specifications for tr and tf are provided to prevent a malfunction which may occur when noise is mixed with a slow-down signal. To assure high-speed XSCL, both tr and tf must satisfy the following relation:

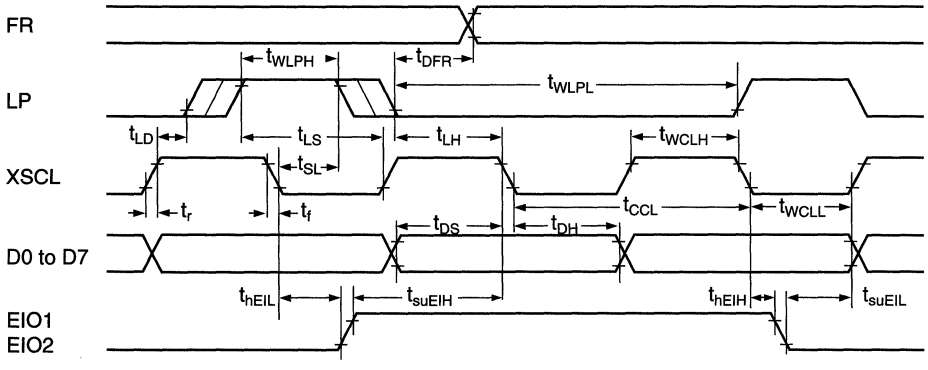
$$t_r, t_f < \frac{t_{CCL} - (t_{WCLH} + t_{WCLL})}{2}$$

- **Timing Chart**
  - **Input Timing**

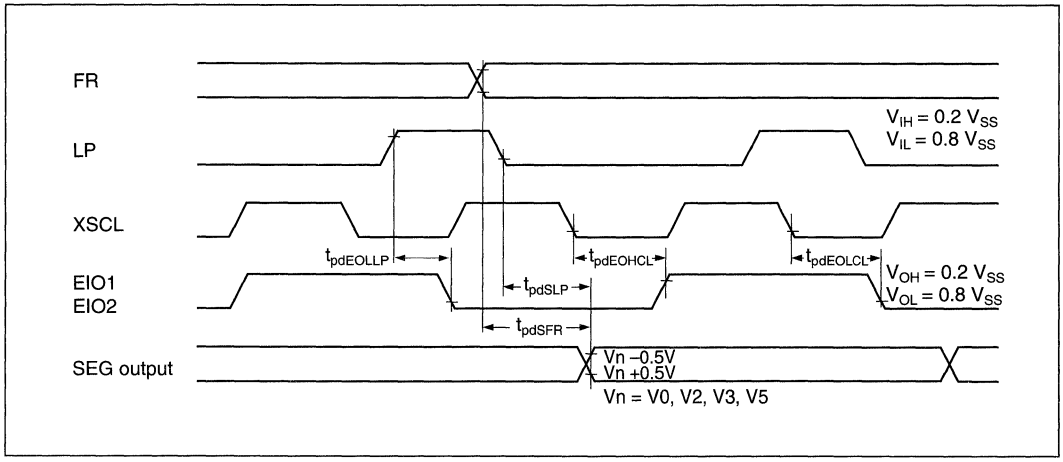


①through ③each show a cascade number of the driver.

$V_{IH} = 0.2\ V_{SS}$
$V_{IL} = 0.8\ V_{SS}$



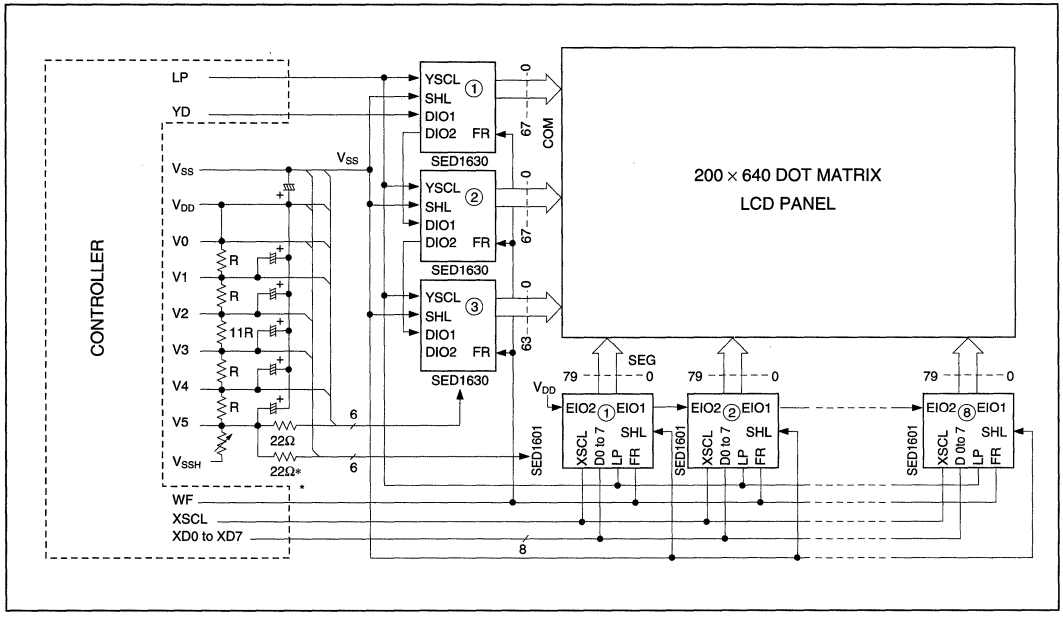
○ **Output Timing**



(V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

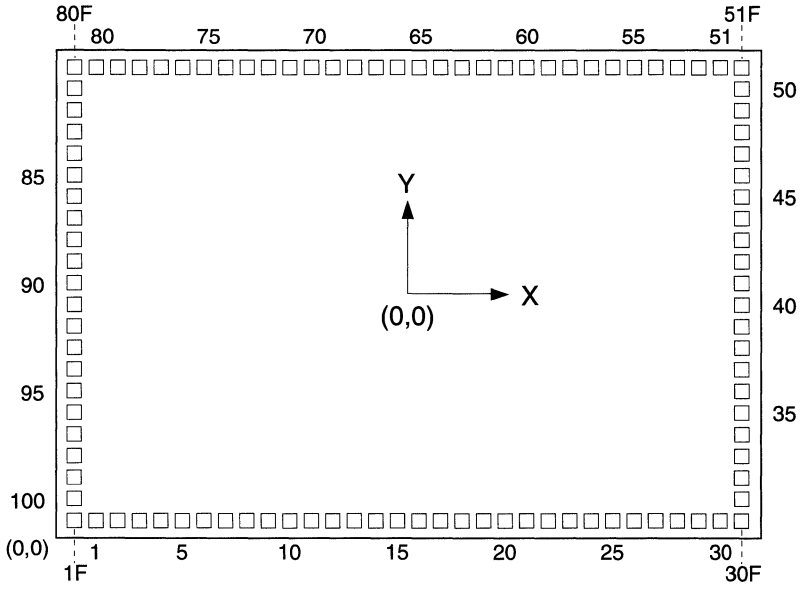
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(LP-rise to disable) time	$t_{pdEOLLP}$	XSCL = "L"	—	—	70	ns
(XSCL-fall to disable) time	$t_{pdEOLCL}$	LP = "H" C_L = 15 pF	—	—	70	ns
(XSCL-fall to enable) time	$t_{pdEOHCL}$		—	—	100	ns
(LP-fall to SEG output) time	t_{pdSLP}	V5 = –12.0 to –28.0 V	—	—	4.5	µs
(FR to SEG output) delay time	t_{pdSFR}	C_L = 100 pF	—	—	4.5	µs

■ EXAMPLE OF APPLICATION (SED1601) (for 200 × 640 DOT MATRIX LCD)



*** Note:** Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01μF) near pins Vss and V5 of each LSI for noise protection.

■ PAD LAYOUT (SED1601D$_{AA}$)



Chip Size	6.20mm × 4.59mm
Pad Pitch	0.18mm (MIN.)
Pad Dimension	0.1mm × 0.1mm
Chip Thickness	0.4mm±0.025mm

■ PAD COORDINATES (SED1601D$_{AA}$)

Pad No.	Pad Name	X	Y
1	SEG0	–2700	–2120
2	SEG1	–2503	–2120
3	SEG2	–2306	–2120
4	SEG3	–2109	–2120
5	SEG4	–1912	–2120
6	SEG5	–1714	–2120
7	SEG6	–1534	–2120
8	SEG7	–1354	–2120
9	SEG8	–1174	–2120
10	SEG9	–994	–2120
11	SEG10	–813	–2120
12	SEG11	–633	–2120
13	SEG12	–453	–2120
14	SEG13	–273	–2120
15	SEG14	–93	–2120
16	SEG15	88	–2120
17	SEG16	268	–2120
18	SEG17	448	–2120
19	SEG18	628	–2120
20	SEG19	808	–2120
21	SEG20	989	–2120
22	SEG21	1169	–2120
23	SEG22	1349	–2120
24	SEG23	1529	–2120
25	SEG24	1709	–2120
26	SEG25	1907	–2120
27	SEG26	2104	–2120
28	SEG27	2301	–2120
29	SEG28	2498	–2120
30	SEG29	2695	–2120
31	SEG30	2925	–1895
32	SEG31	2925	–1669
33	SEG32	2925	–1443
34	SEG33	2925	–1217
35	SEG34	2925	–991
36	SEG35	2925	–811
37	SEG36	2925	–631
38	SEG37	2925	–450
39	SEG38	2925	–270
40	SEG39	2925	–90

Pad No.	Pad Name	X	Y
41	SEG40	2925	90
42	SEG41	2925	270
43	SEG42	2925	451
44	SEG43	2925	631
45	SEG44	2925	811
46	SEG45	2925	991
47	SEG46	2925	1217
48	SEG47	2925	1443
49	SEG48	2925	1689
50	SEG49	2925	1896
51	SEG50	2685	2120
52	SEG51	2498	2120
53	SEG52	2301	2120
54	SEG53	2104	2120
55	SEG54	1907	2120
56	SEG55	1709	2120
57	SEG56	1529	2120
58	SEG57	1349	2120
59	SEG58	1169	2120
60	SEG59	989	2120
61	SEG60	808	2120
62	SEG61	628	2120
63	SEG62	448	2120
64	SEG63	268	2120
65	SEG64	88	2120
66	SEG65	–93	2120
67	SEG66	–273	2120
68	SEG67	–453	2120
69	SEG68	–633	2120
70	SEG69	–813	2120
71	SEG70	–994	2120
72	SEG71	–1174	2120
73	SEG72	–1354	2120
74	SEG73	–1534	2120
75	SEG74	–1714	2120
76	SEG75	–1912	2120
77	SEG76	–2109	2120
78	SEG77	–2306	2120
79	SEG78	–2503	2120
80	SEG79	–2700	2120

Pad No.	Pad Name	X	Y
81	EIO2	–2925	1896
82	D0	–2925	1669
83	D1	–2925	1443
84	D2	–2925	1217
85	D3	–2925	991
86	D4	–2925	811
87	D5	–2925	631
88	D6	–2925	451
89	D7	–2925	270
90	VDD	–2925	90
91	VSS	–2925	–90
92	V0	–2925	–270
93	V2	–2925	–450
94	V3	–2925	–631
95	V5	–2925	–811
96	SHL	–2925	–991
97	XSCL	–2925	–1217
98	LP	–2925	–1443
99	FR	–2925	–1669
100	EIO1	–2925	–1895

*1

Pad No.	Pad Name	X	Y
1F	SEG0	–2925	–2120
30F	SEG29	2925	–2120
51F	SEG50	2925	2120
80F	SEG79	–2925	2120

*1 These pads are located at the corner: Pad Nos. 1F, 30F, 51F, and 80F. They have the same function as Pad Nos. 1, 30, 51, and 80.

SED1606D0A/D0B

CMOS LCD SEGMENT DRIVER

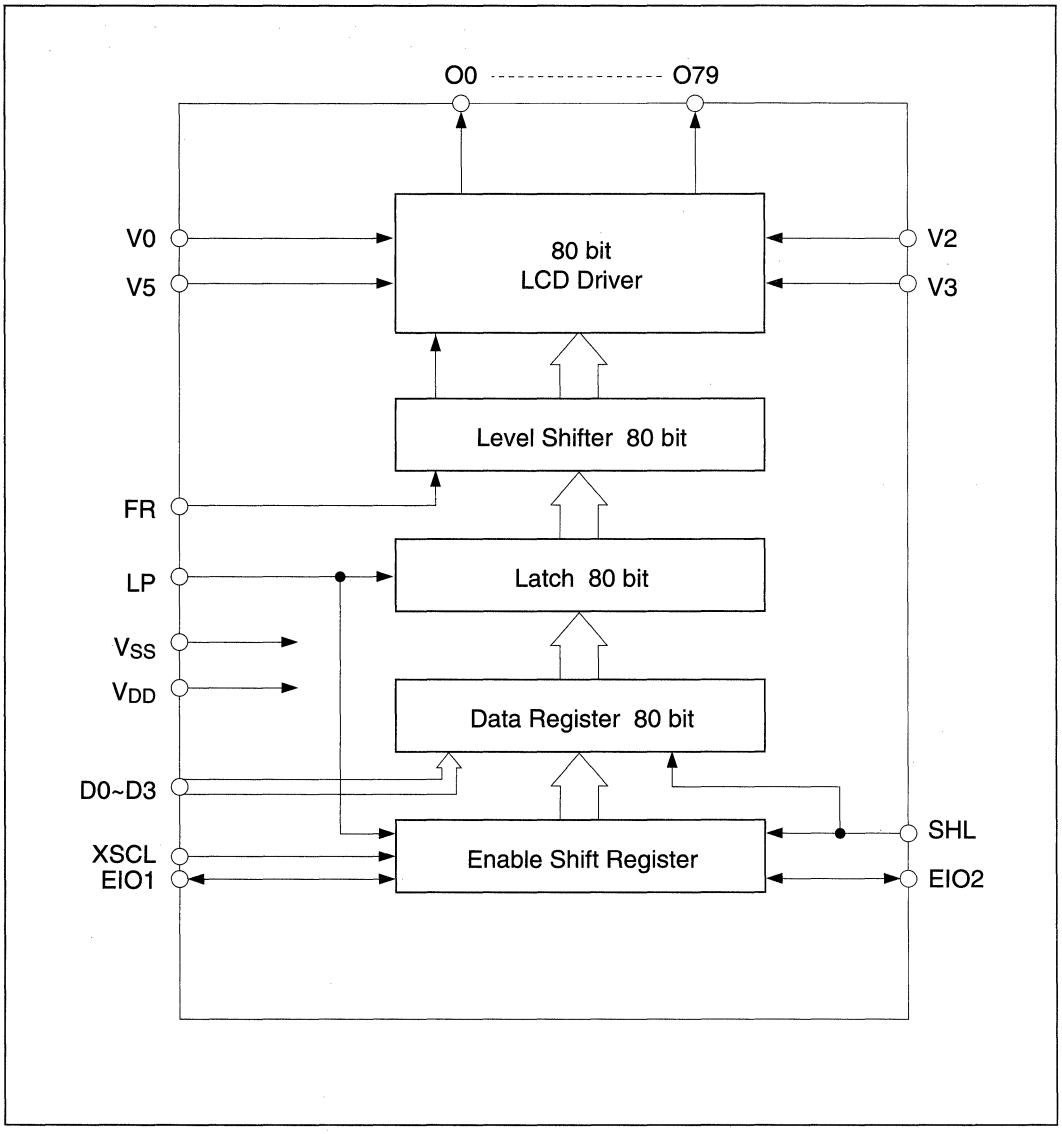
■ DESCRIPTION

The SED1606 is an 80-output segment (column) driver for use in combination with an SED1635. It is provided with high-vision measure of the LCD display and adopts high speed inable chain system for low power operation and slim chip shape suitable for minimizing of the LCD panel. Also, low voltage operation of the logic power source suits a wide range of applications.

■ FEATURES

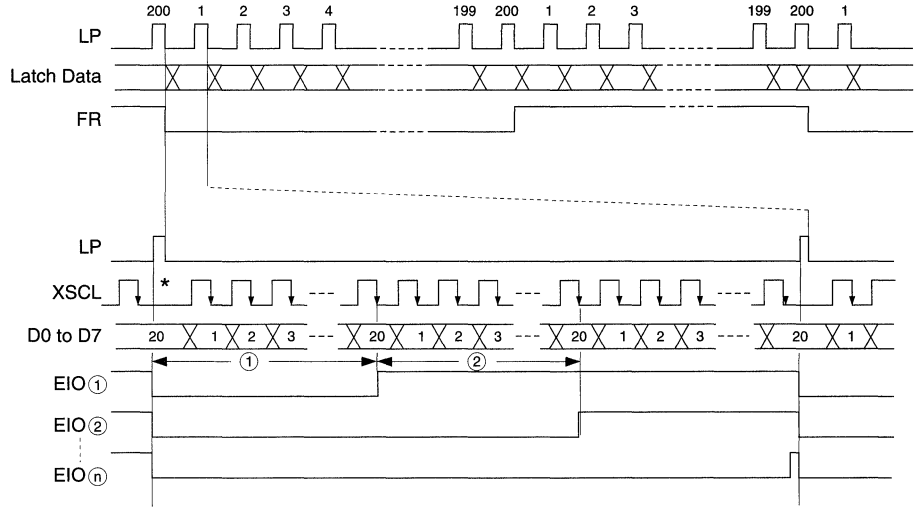
- LCD driver output number 80
- Ultra-slim chip
- Low current consumption
- Low voltage operation ..... –2.7V max.
- Wide range of liquid crystal drive voltage ..... –8 to –28V
- High speed and low power data transfer is possible by adoption of the 4-bit bus inable chain system.
  Shift clock frequency:
  6.5MHz (at –2.7V)
  10.0MHz (at –4.5V)
- Non-bias display off function
- Pin selection of the output shift direction is available
- Offset bias regulation of the liquid crystal power is possible depending on the V_{DD} level
- Logic system power source ..... –2.7 to –5.5V
- Product shapes

■ BLOCK DIAGRAM



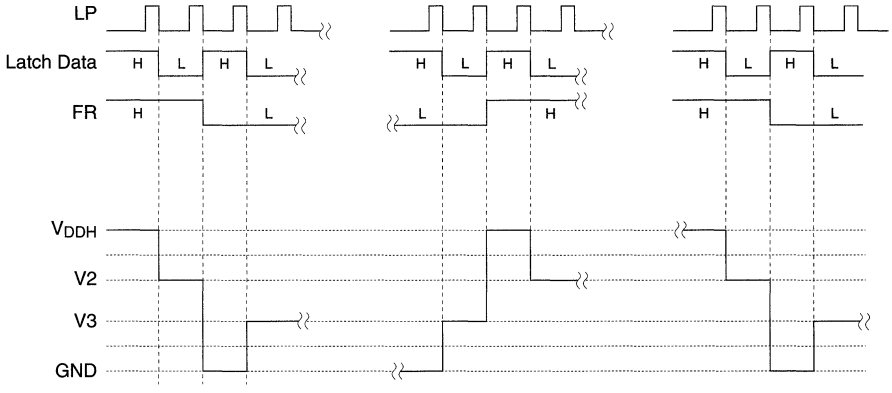
■ TIMING DIAGRAM

In case of 1/200 duty (an example)



◯ to ◯ indicate the cascade numbers of drivers.

*In case of high speed data transfer, it is necessary to secure a longer XSCL cycle in the timing of the LP pulse insertion in order to maintain the specified value of LP → XSCL (t_{LH}).



■ FUNCTIONS

● Inable Shift Register

The inable shift register is a bi-directional shift register wherewith the shift direction is determined by the SHL inputs and outputs of such shift register are used to store data bus signals to the data register. When inable signals are in the disable state, the internal clock signal and data bus are fixed to "L" to become the power save mode.

When using multiple units of the segment driver, EIO terminals of each driver should be connected by the cascade connection and the EIO terminals of the top end driver should be connected to "V_{DD}". (Refer to the connection example). Since the inable control circuit automatically detects when all the 80-bit data are taken in and automatically transfers the inable signal, control signals from a controlling LSI are not needed.

● Data Register

This is a register for serial and parallel conversion of data bus signals by means of the inable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independently from the shift clock input number.

● Latch

It takes in the contents of the data register by means of the trailing edge trigger of the LP to transmit the output to the level shifter.

● Level Shifter

This is a level interface circuit to convert the voltage level of signals from logic level to LCD driving level.

● LCD Driver

It outputs the LCD drive voltage.

Relations among data bus signals, alternating signals FR and the segment output voltage are given below.

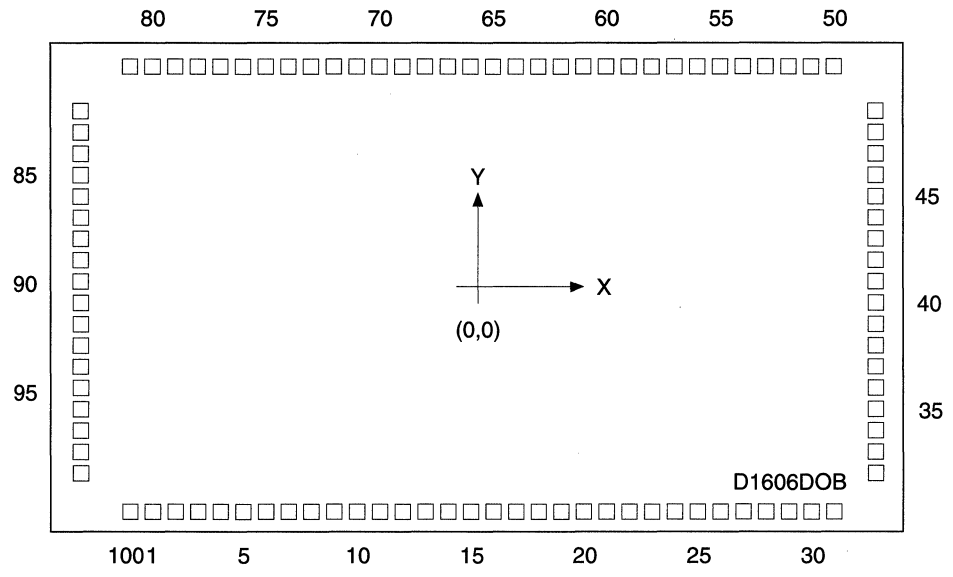
Data Bus Signals	FR	O Output Voltage
H	H	V_0
	L	V_5
L	H	V_2
	L	V_3

■ FUNCTIONS OF THE TERMINALS

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Description</th><th>Numbers of Pins</th></tr>
<tr><td>O 0 ~
O79</td><td>O</td><td>LCD driving segment (column) output
The output level varies at the trailing edge of the LP.</td><td>80</td></tr>
<tr><td>D0 ~ D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock input of display data (trailing edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse input of display data (trailing edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable input and output
Set to input or output depending on the SHL input level.
The output is reset by the LP input and, after recieving
80 bit data, it automatically rises to “H”</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shifting direction choice, and input/output controling input to the EIO terminal
When data is input to (D3, D2, ...D0)
terminals in the order of (a3, a2, a1, a0) (b3,b2,b1,b0).....
(t2, t2, t1, t0), relations between data and
segment outputs are as follows.
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>H</td><td>a3</td><td>a2</td><td>a1</td><td>....</td><td>t2</td><td>t1</td><td>t0</td><td>Output</td><td>Input</td></tr>
<tr><td>L</td><td>t0</td><td>t1</td><td>t2</td><td>....</td><td>a1</td><td>a2</td><td>a3</td><td>Input</td><td>Output</td></tr>
</table>
Note: Relations between the data and segment outputs are determined independent from the shift clock number.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Input of the alternating signal of the LCD drive output</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power source</td><td>Power supply for the logics V_{DD}: 0V
V_{SS}: –2.7 ~ –5.5V</td><td>2</td></tr>
<tr><td>V_0, V_2,
V_3, V_5</td><td>Power source</td><td>Power supply for the LCD driver circuit
V_{DD}: 0V V5: –8 ~ –28V
$V_{DD} \geq V_0 \geq V_2$ 6/9 V_5
*1 3/9 $V_5 \leq V_3 \leq V_5$</td><td>4</td></tr>
<tr><td></td><td></td><td>Total</td><td>100
(including NC4)</td></tr>
</table>

*1. Be sure to connect pairs of V0 – V5 to respective LCD power sources.

■ PAD LAYOUT



Chip Size:	5.59mm × 3.50 mm
Pad Pitch:	0.153mm (min)
Chip Thickness:	0.400mm (Al pad) 0.525mm (Au bump)

Au bump (for reference)

Bump size:	117μm × 109μm ± 20μm
Bump height:	17~28μm

■ PAD COORDINATES

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	$\overline{O}$ 0	–2227	–1578	35	$\overline{O}$ 34	2622	–871	69	$\overline{O}$ 68	–537	1578
2	$\overline{O}$ 1	–2073	↓	36	$\overline{O}$ 35	↓	–713	70	$\overline{O}$ 69	–691	↓
3	$\overline{O}$ 2	–1920		37	$\overline{O}$ 36		–554	71	$\overline{O}$ 70	–846	
4	$\overline{O}$ 3	–1766		38	$\overline{O}$ 37		–396	72	$\overline{O}$ 71	–998	
5	$\overline{O}$ 4	–1612		39	$\overline{O}$ 38		–238	73	$\overline{O}$ 72	–1152	
6	$\overline{O}$ 5	–1459		40	$\overline{O}$ 39		–79	74	$\overline{O}$ 73	–1305	
7	$\overline{O}$ 6	–1305		41	$\overline{O}$ 40		79	75	$\overline{O}$ 74	–1459	
8	$\overline{O}$ 7	–1152		42	$\overline{O}$ 41		238	76	$\overline{O}$ 75	–1613	
9	$\overline{O}$ 8	–998		43	$\overline{O}$ 42		396	77	$\overline{O}$ 76	–1766	
10	$\overline{O}$ 9	–845		44	$\overline{O}$ 43		554	78	$\overline{O}$ 77	–1920	
11	$\overline{O}$ 10	–891		45	$\overline{O}$ 44		713	79	$\overline{O}$ 78	–2073	
12	$\overline{O}$ 11	–537		46	$\overline{O}$ 45		871	80	$\overline{O}$ 79	–2227	
13	$\overline{O}$ 12	–384		47	$\overline{O}$ 46		1029	81	EIO2	–2381	↓
14	$\overline{O}$ 13	–230		48	$\overline{O}$ 47		1188	82	D0	–2622	1346
15	$\overline{O}$ 14	–76		49	$\overline{O}$ 48	↓	1346	83	D1	↓	1192
16	$\overline{O}$ 15	77		50	$\overline{O}$ 49	2381	1578	84	D2		1039
17	$\overline{O}$ 16	231		51	$\overline{O}$ 50	2228	↓	85	D3		885
18	$\overline{O}$ 17	384		52	$\overline{O}$ 51	2074		86			732
19	$\overline{O}$ 18	538		53	$\overline{O}$ 52	1921		87			578
20	$\overline{O}$ 19	692		54	$\overline{O}$ 53	1767		88			424
21	$\overline{O}$ 20	845		55	$\overline{O}$ 54	1613		89			271
22	$\overline{O}$ 21	999		56	$\overline{O}$ 55	1460		90	VDD		106
23	$\overline{O}$ 22	1152		57	$\overline{O}$ 56	1306		91	VSS		–58
24	$\overline{O}$ 23	1306		58	$\overline{O}$ 57	1152		92	V0		–224
25	$\overline{O}$ 24	1460		59	$\overline{O}$ 58	999		93	V2		–389
26	$\overline{O}$ 25	1613		60	$\overline{O}$ 59	845		94	V3		–553
27	$\overline{O}$ 26	1767		61	$\overline{O}$ 60	692		95	V5	↓	–718
28	$\overline{O}$ 27	1921		62	$\overline{O}$ 61	538		96	SHL	–2611	–885
29	$\overline{O}$ 28	2074		63	$\overline{O}$ 62	384		97	XSCL	↓	–1039
30	$\overline{O}$ 29	2228		64	$\overline{O}$ 63	231		98	LP		–1192
31	$\overline{O}$ 30	2381	↓	65	$\overline{O}$ 64	77		99	FR	↓	–1346
32	$\overline{O}$ 31	2622	–1346	66	$\overline{O}$ 65	–76		100	EIO1	–2381	–1578
33	$\overline{O}$ 32	2622	–1188	67	$\overline{O}$ 66	–230	↓				
34	$\overline{O}$ 33	2622	–1029	68	$\overline{O}$ 67	–384					

■ ELECTRICAL CHARACTERISTICS

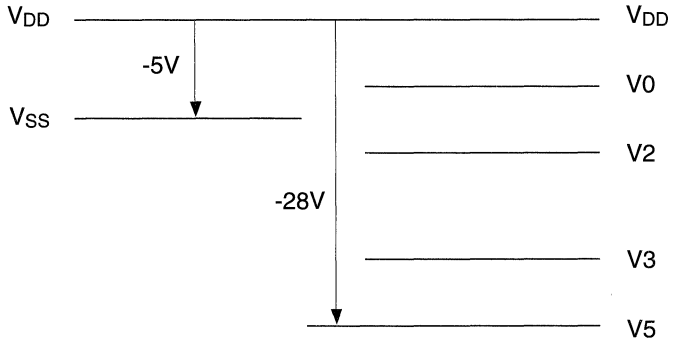
● Absolute Maximum Rating

Parameters	Codes	Ratings	Units
Power voltage (1)	V_{SS}	–7.0 ~ +0.3	V
Power voltage (1)	V_5	–30.0 ~ +0.3	V
Power voltage (3)	V_0, V_2, V_3	V_5 – 0.3 ~ V_{DD} +0.3	V
Input voltage	V_I	V_{SS} – 0.3 ~ V_{DD} +0.3	V
Output voltage	V_O	V_{SS} – 0.3 ~ V_{DD} +0.3	V
EIO output current	I_{O1}	20	mA
Working temperature	Topr	–40 ~ +85	°C
Storage temperature 1	Tstg1	–65 ~ +150	°C

Note 1. All the above voltages are based on V_{DD} = 0V.

Note 2. The storing temperature 1 specifies that of chips proper.

Note 3. Voltage of V0, V2 and V3 should always be maintained under a condition of $V_{DD} \geq V0 \geq V2 \geq V3 \geq V5$.



Note 4. When logic power becomes floating state or if V_{SS} = –2.6 or beyond while the LCD driver power source is being applied, the LSI may be permanently damaged and avoid such circumstances.

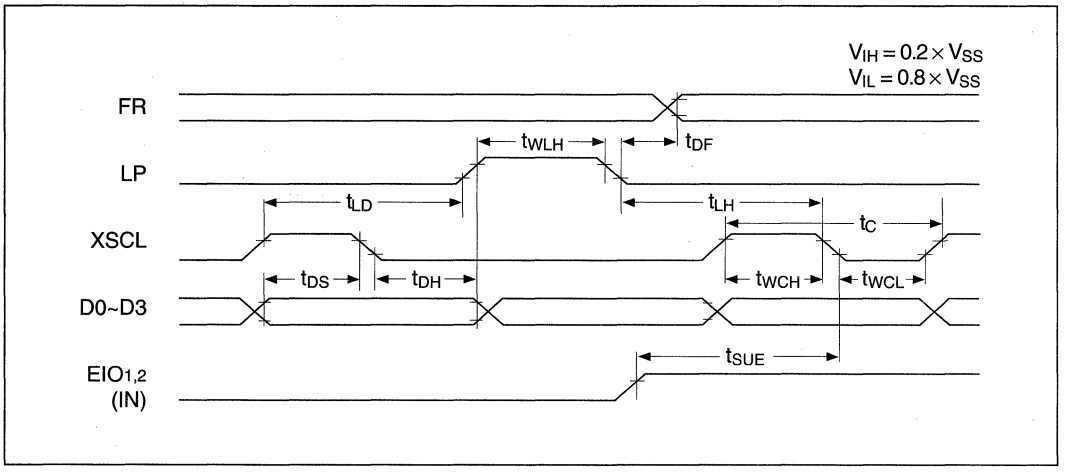
Pay extra attention to the power sequence at times of turning on and turning off the power supply.

● DC Characteristics

Unless otherwise designated, V_{DD} = V0 = 0V, V_{SS} = –5.0 ±10% and T_a = –40 to 85°C

Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
Power voltage (1)	V_{SS}	—	V_{SS}	–5.5	–5.0	–2.7	V
Recommended working voltage	V_5	—	V_5	–28.0	—	–12.0	V
Operable voltage	V_5	Function	V_5	—	—	–8.0	V
Power voltage (2)	V_0	Recommended value	V_0	V_{DD} –2.5	—	V_{DD}	V
Power voltage (3)	V_2	Recommended value	V_2	V_2	3/9 V_5	—	V
Power voltage (4)	V_2	Recommended value	V_3	V_3	—	6/9 V_5	V
High level input voltage	V_{IH}	V_{SS}= 2.7~ 5.5V	EIO1, EIO2, FR D0–D3, XSCL SHL, LP,	0.2V_{CC}	—	—	V
Low level input voltage	V_{IL}					0.8V_{SS}	V
High level output voltage	V_{OH}	V_{SS} = 2.7 – 5.5V, I_{OH} = –0.6mA	EIO1, EIO2	V_{DD} – 0.4	—	—	V
Low level output voltage	V_{OL}	V_{SS} = 2.7 – 5.5V, I_{OL} = 0.6mA		—	—	0.4	V
Input leak current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	D0–D3, LP, FR XSCL, SHL	—	—	2.0	µA
Input Output leak current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$	EIO1, EIO2	—	—	5.0	µA
Rest current	I_{SS}	V_5 = 28.0 ~ – 14.0V V_{IH} = GND, V_{IL} = GND	V_{SS}	—	—	25	µA
Output resistance	R_{SEG}	ΔV_{ON} = 0.5V , Ta = 25°C V_5 = –20.0V V_3 = 13/15 V_5 V_2 = 2/15 V_5 V0 = V_{DD}	O 0 ~ O 79		1.2	1.6	KΩ
Average operating current consumption (1)	I_{SS}	V_{SS} = +5.0V, V_{IH} = V_{DD} V_{IL} = V_{SS}, f_{XSCL} = 2.69MHz f_{LP} = 16.8KHz, f_{FR} = 70Hz input data: Diced display no-load	V_{SS}	—	0.10	0.2	mA
		V_{SS} = +3.0V Other conditons are the same as with V_{SS} = –5V		—	0.7	0.15	
Average operating current consumption (2)	I_5	V_{SS} + 5.0V, V_O = 0.0V V_2 = +9.30V, V_3 = –18.6V, V_5 = +28.0V Other conditions are the same as with the item I_{SS}.	V_5	—	0.05	0.04	mA
Input terminal capacity	CI	Freq. = 1 Mhz Ta = 25°C XSCL,SHL chips proper	D0–D3, LP, FR	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

- **AC Characteristics**
- **Input Timing Characteristics**



V_{SS} = –5.0V ± 0.5V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C		100	—	ns
XSCL high level pulse duration	t_{WCH}		30	—	ns
XSCL low level pulse duration	t_{WCL}		30	—	ns
Data setup time	t_{DS}		20	—	ns
Data hold time	t_{DH}		10	—	ns
XSCL → LP rise time	t_{LD}		0	—	ns
LP → XSCL fall time	t_{LH}		40	—	ns
LP high level pulse duration	t_{WLH}	*3	40	—	ns
FR delay allowance	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}		35	—	ns

V_{SS} = –4.5V to 2.7V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	V_{SS} = –2.7V *1	153	—	ns
		V_{SS} = –3.0V *2	133		
XSCL high level pulse duration	t_{WCH}		50	—	ns
XSCL low level pulse duration	t_{WCL}		50	—	ns
Data setup time	t_{DS}		30	—	ns
Data hold time	t_{DH}		15	—	ns
XSCL → LP rise time	t_{LD}		0	—	ns
LP → XSCL fall time	t_{LH}	V_{SS} = –2.7V	75	—	ns
		V_{SS} = –3.0V	65		
LP high level pulse duration	t_{WLH}	V_{SS} = –2.7V *3	75	—	ns
		V_{SS} = –3.0V *3	65		
FR delay allowance	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}	V_{SS} = –2.7V	60	—	ns
		V_{SS} = –3.0V	51		

Notes: *1. 6.5MHz equivalence

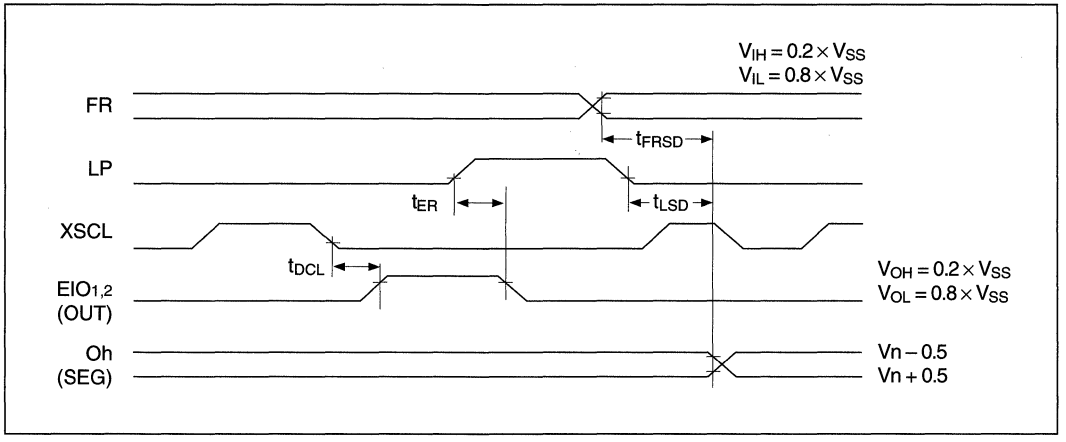
*2. 7.5MHz equivalence

*3. t_{WLH} specifies the time when LP is "H" and, at the same time, XSCL is "L".

*4. The input signal t_r, t_f is fixed to 20ns.

*5. High-speed operation of the shift clocks (XSCL) should only be made under a condition of tr or $t_f \leq \{t_c - (t_{DCL} + t_{SUE})\}/2$

○ Output Timing Characteristics



V_{DD} = –5.0 ± 5%V, V5 = –12.0 to –28.0V

Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pf (EIO)	—	90	ns
EIO output delay time	t_{DCL}		—	55	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pf (0 n)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	400	ns

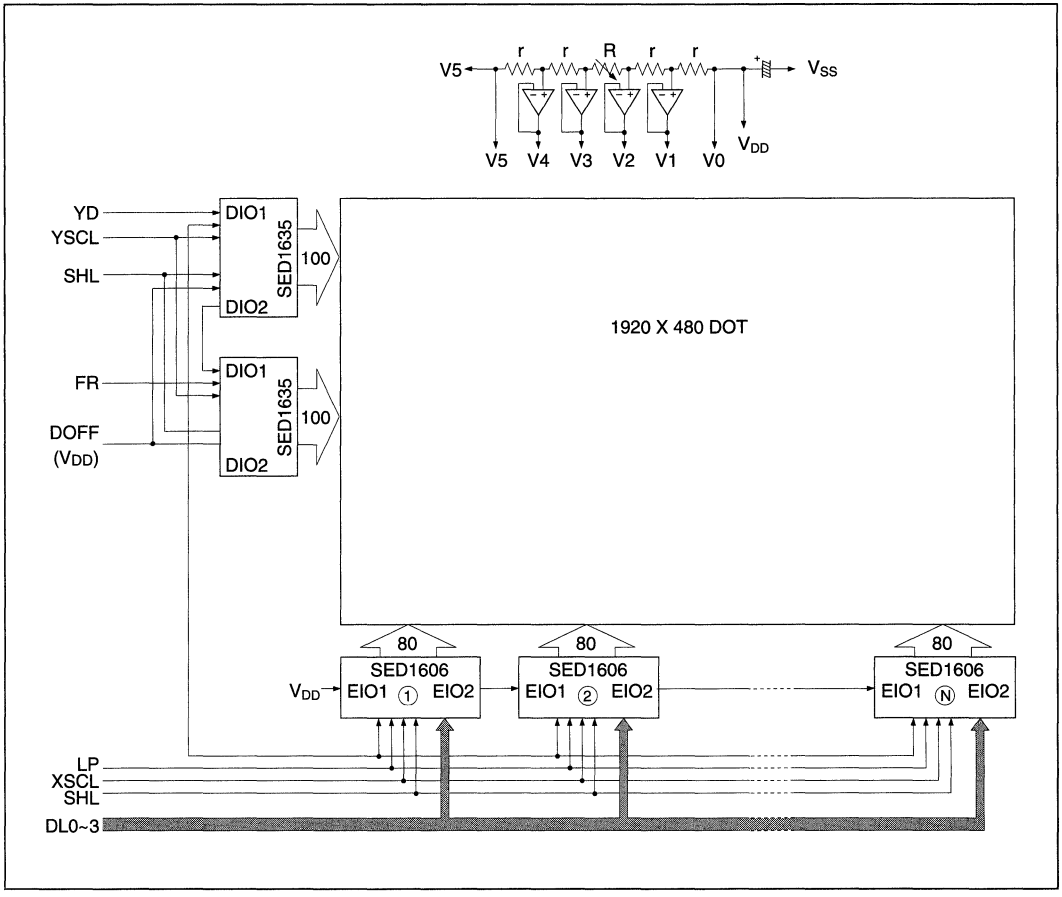
V_{DD} = –4.5 to –2.7V, V5 = –12.0 to –28.0V

Parameter	Symbol	Conditions		Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pf (EIO)		—	150	ns
EIO output delay time	t_{DCL}		V_{SS} = –2.7V	—	88	ns
			V_{SS} = –3.0V		77	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pf (0 n)		—	400	ns
FR → SEG output delay time	t_{FRSD}			—	800	ns

Notes: *1. The input signal t_r, t_f is fixed to 20ns.

*2. High speed operation of the shift clocks (XSCL) should be made only under a condition of t_f or $t_f \leq \{t_C - (t_{DCL} + t_{SUE})\}/2$.

■ CONNECTION EXAMPLE



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DISCONTINUED

SED1620

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

- **CMOS 128-Bit Segment Driver**
- **High Voltage Resistant Output**
- **1/100 to 1/300 in Display Duty**
- **CMOS High Voltage Resistant Process**

■ DESCRIPTION

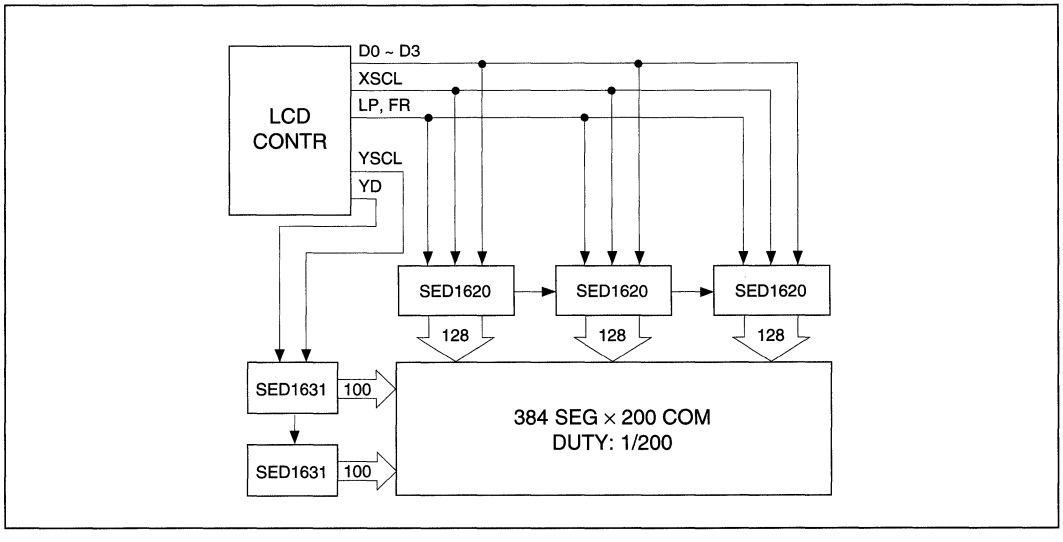
The SED1620 is a 128 output dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/300). The LSI has a wide range of LCD driving voltages. Due to the architecture of the SED1620, the LCD driving voltage V0 is isolated from V_{DD} supply. This provides the ability to adjust the offset bias independently of V_{DD}. These unique features allow the SED1620 to interface with a variety of LCD panels. The SED1620 does not require a controller to output an enable signal to implement daisy chain technology. This provides for easy interfacing with the LCD controllers such as the SED1330, SED1335, SED1351 or the SED1341.

The SED1620 is used in conjunction with the SED1610 (86 row driver) or the SED1630 (68-bit row driver) and SED1631 (100 row driver), SED1632 (86-row driver), SED1633 (100-row driver), SED1634 (100-row driver) to drive a large-capacity dot matrix LCD panel.

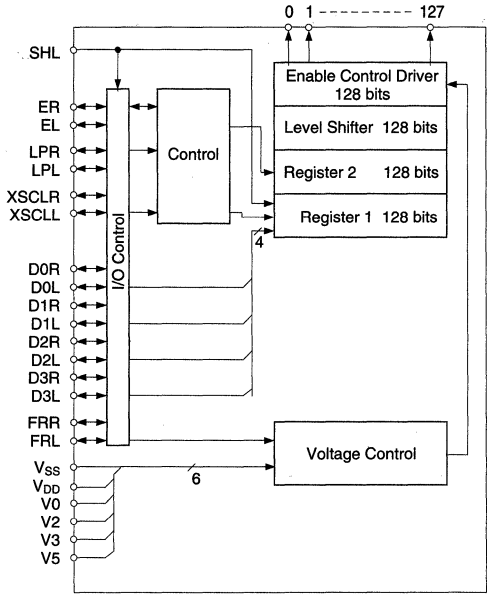
■ FEATURES

- Low-power CMOS technology
- 128-bit segment (column) driver
- High-speed 4-bit bus
- Duty cycle ..... 1/100 to 1/300
- Shift clock frequency ..... 4MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Daisy chain enable support
- No enable signal by controller is required
- Wide range of LCD voltage .... –12V to –28V
- Supply voltage ..... 5.0V ±10%
- Package ..... Al pad chip (D_{OA}) for chip on glass

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>Function</th></tr>
<tr><td>SEG0 to SEG127</td><td>LCD driving segment (column) outputs
Each output changes at the falling edge of LP</td></tr>
<tr><td>D0R to D3R
D0L to D3L</td><td>Display data inputs</td></tr>
<tr><td>XSCLR, XSCLL</td><td>Shift clock of display data (falling edge trigger).</td></tr>
<tr><td>LPR, LPL</td><td>Latch pulse of display data (falling edge trigger).</td></tr>
<tr><td>ER, EL</td><td>Enable I/O, which is controlled by SHL input. Output is reset by LP, and automatically falls when 128 bits of data are taken in</td></tr>
<tr><td>SHL</td><td>I/O terminal configuration and register 1 shift direction select input.
<table>
<tr><th>SHL</th><th>D0R to D3R</th><th>D0L to D3L</th><th>XSCLR</th><th>XSCLL</th><th>LPR</th><th>LPL</th><th>ER</th><th>EL</th><th>FRR</th><th>FRL</th></tr>
<tr><td>H</td><td>O</td><td>I</td><td>O</td><td>I</td><td>O</td><td>I</td><td>O</td><td>I</td><td>O</td><td>I</td></tr>
<tr><td>L</td><td>I</td><td>O</td><td>I</td><td>O</td><td>I</td><td>O</td><td>I</td><td>O</td><td>I</td><td>O</td></tr>
</table>
SHL = H
<table>
<tr><td>SEG0 –127</td><td>127</td><td>126</td><td>125</td><td>124</td><td>123</td><td>···</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Data</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>...</td><td>e</td><td>d</td><td>c</td><td>b</td><td>a</td></tr>
</table>
SHL = L
<table>
<tr><td>SEG0 –127</td><td>127</td><td>126</td><td>125</td><td>124</td><td>123</td><td>···</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Data</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>...</td><td>v</td><td>w</td><td>x</td><td>y</td><td>z</td></tr>
</table></td></tr>
<tr><td>FR</td><td>AC signal of LCD driving outputs.</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Logic circuit power. V_{DD}: 0 V (GND)
V_{SS}: –5.0 V</td></tr>
<tr><td>V1, V2, V3, V5</td><td>LCD driving power. V5: –12 to –28 V
$V_{DD} \geq V0 \geq V2 > V3 \geq V5$</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V5	–30.0 to +0.3	V
Supply voltage (2)	V0, V2, V3*	V5 –0.3 to +0.3	V
Input voltage (1)	V_I	V_{SS} –0.3 to +0.3	V
Output voltage (1)	V_O	V_{SS} –0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OSEG}	20	mA
Allowable power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +150	°C

* V0, V2 and V3 must always satisfy the condition $V_{DD} \geq V0 \geq V2 \geq V3 \geq V5$.

● **DC Electrical Characteristics**

(Unless otherwise specified, V_{DD} = V0 = 0 V, V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Pin	Min	Typ	Max	Unit
Operating voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–4.5	V
Recommended op. voltage Minimum operating voltage	V5		V5	–28.0	—	–12.0 –8.0	V
Operating voltage (2)	—	Recommended value	V0	–2.5	—	0	V
Operating voltage (3)	V2	Recommended value	V2	3/9·V5	—	V0	V
Operating voltage (4)	V3	Recommended value	V3	V5	—	6/9·V5	V
"H" input voltage	V_{IH}		EI01, EI02, XSCL, LP, D0 to D3, FR, SHL	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}			—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH} = –0.6 mA	EI01, EI02	–0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_I \le 0$ V	D0 to D3, LP XSCL, SHL, FR	—	—	2.0	µA
	$I_{LI/O}$	$V_{SS} \le V_I \le 0$ V	EI01, EI02	—	—	5.0	µA
Stand–by current	I_{DDS}	V5 = –12.0 to –28.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{SEG}	|ΔV_{ON}| = 0.5V V5 –14.0V	SEG0 to SEG127	—	2.0	4.5	kΩ
Current dissipation (1)	I_{SSO1}	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{XSCL} = 1.92 MHz., f_{LP} = 12 kHz, Frame period = 60 Hz; Input data: Inverted bit by bit; No-load	V_{SS}	—	180	500	µA
Current dissipation (2)	I_{SSO2}	V_{SS} = –5.0 V, V2 = –4.0 V V3 = –16.0 V, V5 = –20.0 V All other conditions are same as I_{SSO1}	V5	—	80	160	µA
Input capacitance	C_I	T_a = 25°C	D0 to D3, LP XSCL, SHL, FR	—	—	8.0	pF
	$C_{I/O}$		EI01, EI02	—	—	15.0	pF

● AC Electrical Characteristics

(V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

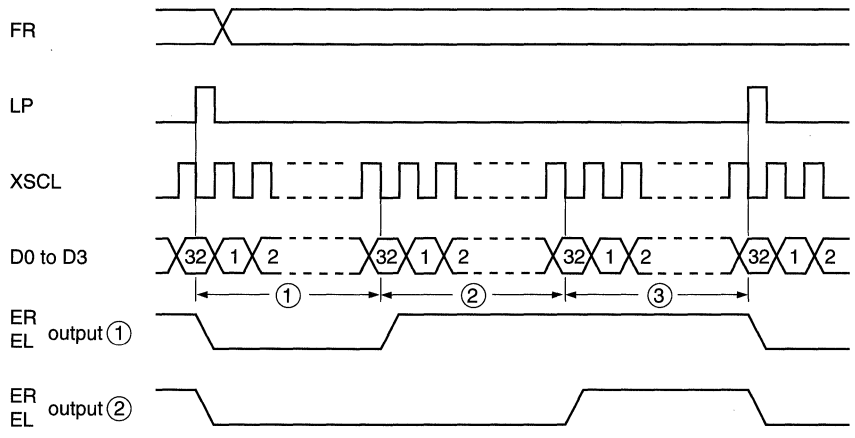
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XSCL period	t_{CCL}	t_r, $t_f \leq 10$ ns	250	—	—	ns
XSCL "H" pulse width	t_{WCLH}		100	—	—	ns
XSCL "L" pulse width	t_{WCLL}		100	—	—	ns
Data setup time	t_{DS}		80	—	—	ns
Data hold time	t_{DH}		60	—	—	ns
XSCL-rise to LP-rise time	t_{LD}		0	—	—	ns
XSCL-fall to LP-fall time	t_{SL}		100	—	—	ns
LP-rise to XSCL-rise time	t_{LS}		100	—	—	ns
LP-fall to XSCL-fall time	t_{LH}		100	—	—	ns
LP "H" pulse width	t_{WLPH}		100	—	—	ns
LP "L" pulse width	t_{WLPL}		260	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns
Enable "H" setup time	t_{suEIH}		70	—	—	ns
Enable "H" hold time	t_{hEIH}		40	—	—	ns
Enable "L" setup time	t_{suEIL}		0	—	—	ns
Enable "L" hold time	t_{hEIL}		0	—	—	ns
Input signal rise time	t_r		—	—	150*	ns
Input signal fall time	t_f		—	—	150*	ns

* Note: The specifications for t_r and t_f are provided to prevent a malfunction which may occur when noise is mixed with a slow-down signal. To assure high-speed XSCL, both t_r and t_f must satisfy the following relation:

$$t_r, t_f < \frac{t_{CCL} - (t_{WCLH} + t_{WCLL})}{2}$$

● **Timing Chart**

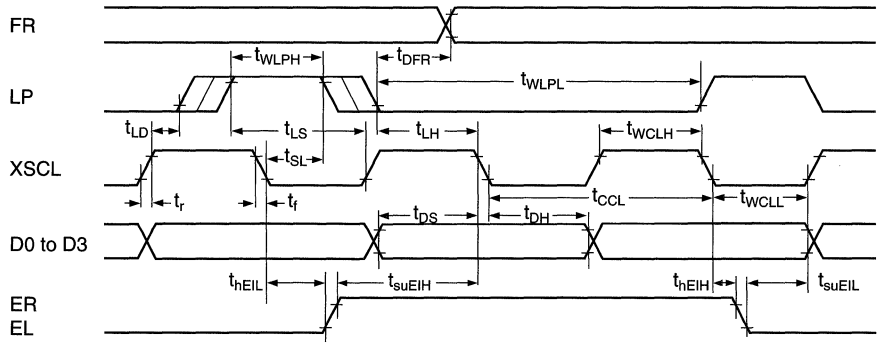
○ **Input Timing**



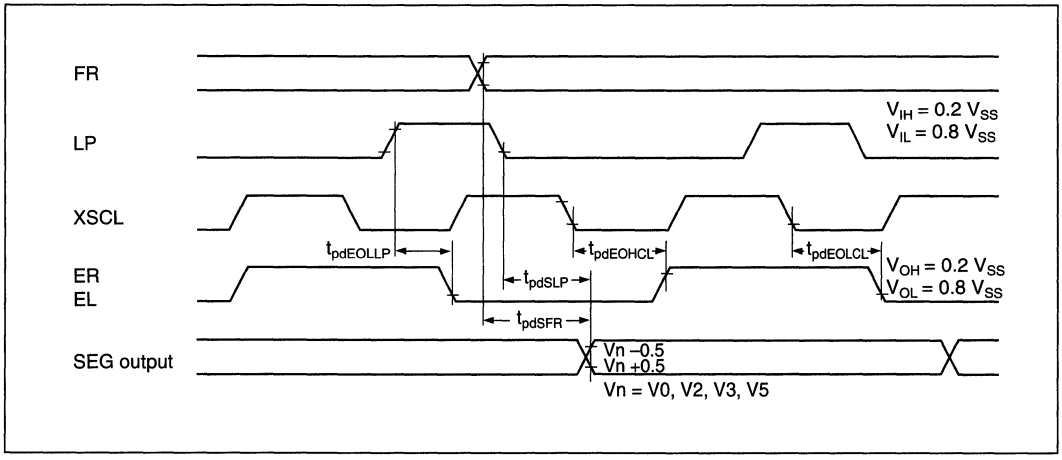
①through ③each show a cascade number of the driver.

$V_{IH} = 0.2\ V_{SS}$

$V_{IL} = 0.8\ V_{SS}$



○ Output Timing



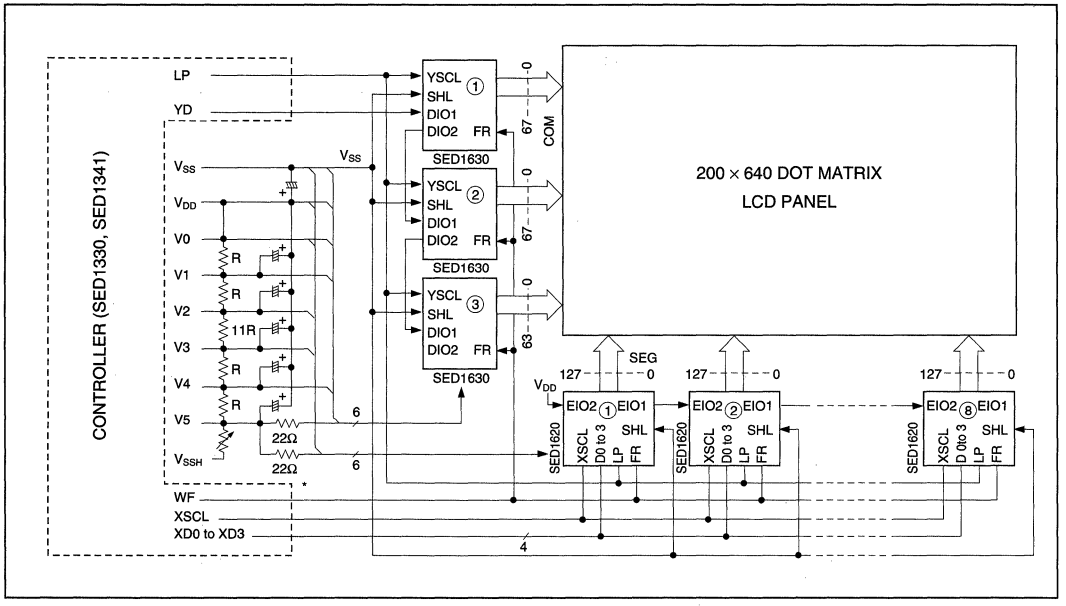
(V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(LP-rise to disable) time	$t_{pdEOLLP}$	XSCL = "L"	—	—	100	ns
(XSCL-fall to disable) time	$t_{pdEOLCL}$	LP = "H" C_L = 15 pF	—	—	100	ns
(XSCL-fall to enable) time	$t_{pdEOHCL}$		—	—	100	ns
(LP-fall to SEG output) time	t_{pdSLP}	V5 = –12.0 to –28.0 V	—	—	4.5	µs
(FR to SEG output) delay time	t_{pdSFR}	C_L = 100 pF	—	—	4.5	µs
(I/O to O/I) delay time		C_L = 15 pF *	—	—	30	µs

* Except for ER and EL

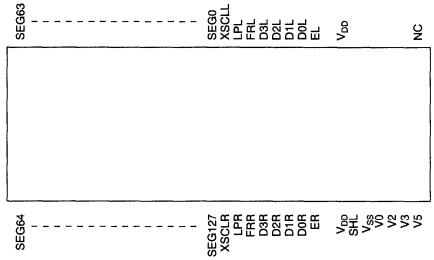
■ EXAMPLE OF APPLICATION (SED1620D0A)

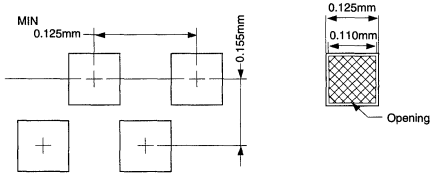
(for 200 × 640 DOT MATRIX LCD)



Note: * Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01 μF) near pins Vss and V5 of each LSI for noise protection.

■ PAD LAYOUT





Chip name D1620DOA (Aluminum pattern)

Chip size	10.5 × 3.88mm
Chip thickness	0.25 ±0.03mm
Pad size	0.11 × 0.11mm (Opening)
Pad pitch	Min. 0.125mm

■ PAD COORDINATES

Pad		X	Y	Pad		X	Y	Pad		X	Y
No.	Name	(μm)	(μm)	No.	Name	(μm)	(μm)	No.	Name	(μm)	(μm)
1	NC	4893	1793	52	SEG41	–2278	1793	103	SEG92	–1523	–1793
2	VDD	4138	1793	53	SEG42	–2404	1638	104	SEG93	–1397	–1638
3	EL	3886	1638	54	SEG43	–2530	1793	105	SEG94	–1272	–1793
4	D0L	3760	1793	55	SEG44	–2655	1638	106	SEG95	–1146	–1638
5	D1L	3635	1638	56	SEG45	–2781	1793	107	SEG96	–1020	–1793
6	D2L	3509	1793	57	SEG46	–2907	1638	108	SEG97	–894	–1638
7	D3L	3383	1638	58	SEG47	–3033	1793	109	SEG98	–768	–1793
8	FRL	3257	1793	59	SEG48	–3159	1638	110	SEG99	–643	–1638
9	LPL	3131	1638	60	SEG49	–3284	1793	111	SEG100	–517	–1793
10	XSCLL	3006	1793	61	SEG50	–3410	1638	112	SEG101	–391	–1638
11	SEG0	2880	1638	62	SEG51	–3536	1793	113	SEG102	–265	–1793
12	SEG1	2754	1793	63	SEG52	–3662	1638	114	SEG103	–139	–1638
13	SEG2	2628	1638	64	SEG53	–3788	1793	115	SEG104	–14	–1793
14	SEG3	2502	1793	65	SEG54	–3913	1638	116	SEG105	112	–1638
15	SEG4	2377	1638	66	SEG55	–4039	1793	117	SEG106	238	–1793
16	SEG5	2251	1793	67	SEG56	–4165	1638	118	SEG107	364	–1638
17	SEG6	2125	1638	68	SEG57	–4291	1793	119	SEG108	490	–1793
18	SEG7	1999	1793	69	SEG58	–4417	1638	120	SEG109	615	–1638
19	SEG8	1873	1638	70	SEG59	–4542	1793	121	SEG110	741	–1793
20	SEG9	1748	1793	71	SEG60	–4668	1638	122	SEG111	867	–1638
21	SEG10	1622	1638	72	SEG61	–4794	1793	123	SEG112	993	–1793
22	SEG11	1496	1793	73	SEG62	–4920	1638	124	SEG113	1119	–1638
23	SEG12	1370	1638	74	SEG63	–5046	1793	125	SEG114	1244	–1793
24	SEG13	1244	1793	75	SEG64	–5046	–1793	126	SEG115	1370	–1638
25	SEG14	1119	1638	76	SEG65	–4920	–1638	127	SEG116	1496	–1793
26	SEG15	993	1793	77	SEG66	–4794	–1793	128	SEG117	1622	–1638
27	SEG16	867	1638	78	SEG67	–4668	–1638	129	SEG118	1748	–1793
28	SEG17	741	1793	79	SEG68	–4542	–1793	130	SEG119	1873	–1638
29	SEG18	615	1638	80	SEG69	–4417	–1638	131	SEG120	1999	–1793
30	SEG19	490	1793	81	SEG70	–4291	–1793	132	SEG121	2125	–1638
31	SEG20	364	1638	82	SEG71	–4165	–1638	133	SEG122	2251	–1793
32	SEG21	238	1793	83	SEG72	–4039	–1793	134	SEG123	2377	–1638
33	SEG22	112	1638	84	SEG73	–3913	–1638	135	SEG124	2502	–1793
34	SEG23	–14	1793	85	SEG74	–3788	–1793	136	SEG125	2628	–1638
35	SEG24	–139	1638	86	SEG75	–3662	–1638	137	SEG126	2754	–1793
36	SEG25	–265	1793	87	SEG76	–3536	–1793	138	SEG127	2880	–1638
37	SEG26	–391	1638	88	SEG77	–3410	–1638	139	XSCLR	3006	–1793
38	SEG27	–517	1793	89	SEG78	–3284	–1793	140	LPR	3131	–1638
39	SEG28	–643	1638	90	SEG79	–3159	–1638	141	FRR	3257	–1793
40	SEG29	–768	1793	91	SEG80	–3033	–1793	142	D3R	3383	–1638
41	SEG30	–894	1638	92	SEG81	–2907	–1638	143	D2R	3509	–1793
42	SEG31	–1020	1793	93	SEG82	–2781	–1793	144	D1R	3635	–1638
43	SEG32	–1146	1638	94	SEG83	–2655	–1638	145	D0R	3760	–1793
44	SEG33	–1272	1793	95	SEG84	–2530	–1793	146	ER	3886	–1638
45	SEG34	–1397	1638	96	SEG85	–2404	–1638	147	VDD	4138	–1793
46	SEG35	–1523	1793	97	SEG86	–2278	–1793	148	SHL	4264	–1638
47	SEG36	–1649	1638	98	SEG87	–2152	–1638	149	VSS	4389	–1793
48	SEG37	–1775	1793	99	SEG88	–2026	–1793	150	V0	4515	–1638
49	SEG38	–1901	1638	100	SEG89	–1901	–1638	151	V2	4641	–1793
50	SEG39	–2026	1793	101	SEG90	–1775	–1793	152	V3	4767	–1638
51	SEG40	–2152	1638	102	SEG91	–1649	–1638	153	V5	4893	–1793

Note: 1. NC : Not connected
2. 2 pads VDD are supplied, and should be used to reduce the power source impedance

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■ DESCRIPTION

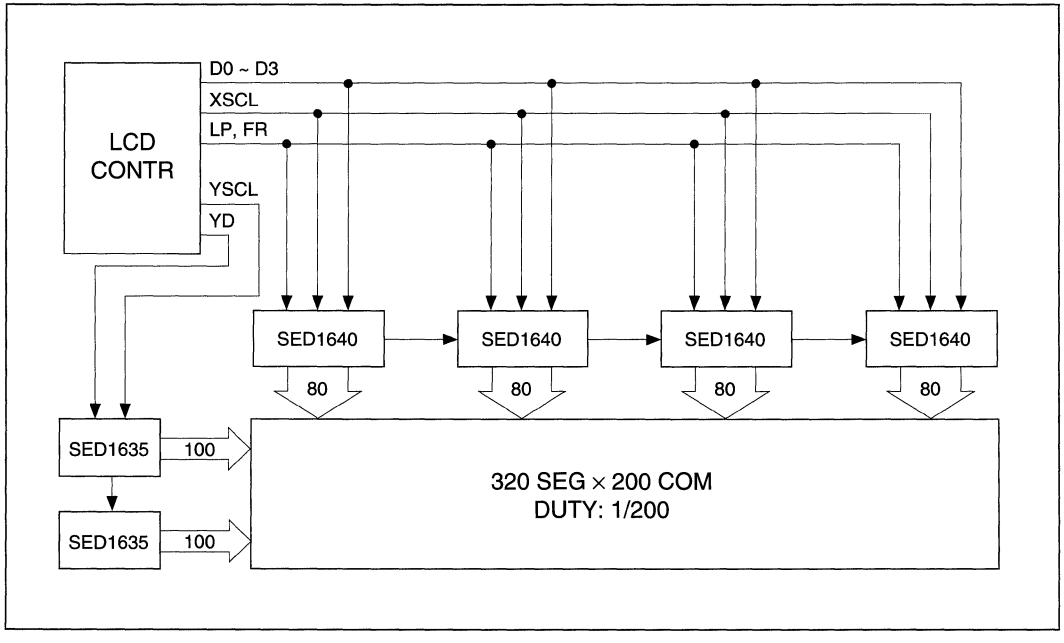
The SED1640 is an 80-output dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/300). The LSI has a wide range of LCD driving voltages. The offset bias regulation of the liquid crystal power is possible depending on the V_{DD} level. These unique features allow the SED1640 to interface with a variety of LCD panels. The device does not require a controller to implement an enable daisy chain technology.

The SED1640 is used in conjunction with the SED1651 (100-output row driver) or the SED1635 (100-bit row driver) to drive a large-capacity dot matrix LCD panel.

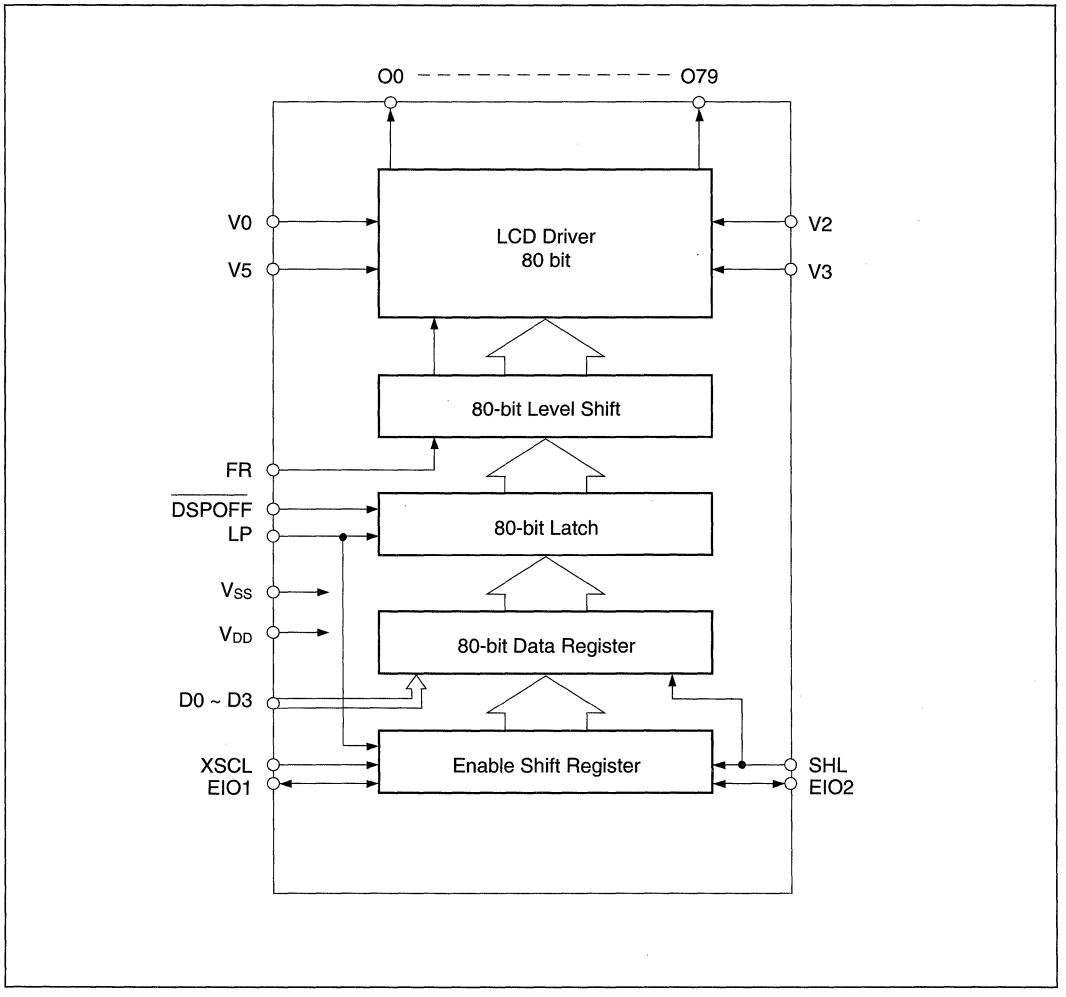
■ FEATURES

- Low-power CMOS technology
- 80-bit segment (column) driver
- High-speed 4-bit bus
- Duty cycle ..... 1/100 to 1/300
- Unbiased display off function
- Shift clock frequency ..... 10MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Daisy chain enable support
- Pin selection of the output shift direction
- LCD voltage ..... –8 to –28V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... Slim DIE (DOB)

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Enable Shift Register

The enable shift register is a bi-directional shift register where the direction of the shift is selected by the SHL input. The output of this shift register is used to store the data bus signals in the data register.

When the enable signal is in a disable state, the internal clock signal and data bus are fixed at "L", placing the chip in power save mode.

When multiple segment drivers are used, the EIO terminals of the various drivers are cascade connected and the EIO terminal of the first driver is connected to V_{DD}.

The enable control circuit automatically senses and sends the enable signal when 80 bits worth of data have been received, eliminating the need for a control signal from the control LSI.

● Data Register

This is a register to convert the data bus signal from serial to parallel using the output of the enable shift register. Consequently, the relationships between the serial display data and the segment output are determined independently of the shift clock input number.

● Latch

The latch receives the contents of the data registers when triggered by the falling edge of the LP, and outputs them to the level shifter.

● Level Shifter

The level shifter is a level interface circuit which converts the signal voltage level from a logic circuit level to the LC driver voltage level.

● LCD Driver

The LCD driver outputs the LC drive voltage.

The relationship between the data bus signal, the AC signal FR, and the segment output voltage is as follows:

$\overline{DSPOFF}$	Data Bus Signal	FR	O Output Voltage
H	H	H	V0
		L	V5
	L	H	V2
		L	V3
L	—	—	V0

■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>O0 to O79</td><td>O</td><td>LCD drive segment output; the output changes at the LP falling edge.</td><td>80</td></tr>
<tr><td>D0 to D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock input of display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse input of display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1</td><td>I/O</td><td>Enable I/O</td><td>2</td></tr>
<tr><td>EIO2</td><td></td><td>The terminals are set to the input or output according to the SHL input signal level. The output is reset by LP input. When the 80-bit data is read, the signal automatically goes high.</td><td></td></tr>
<tr><td>SHL</td><td>I</td><td>Used for shift direction selection and I/O control output of EIO terminal.
If data sets (a, b, c, d) (e, f, g, h) ... (w, x, y, z) are entered in this sequence in terminals (D3, D2, D1, D0), the data and segment output are processed as follows:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th>...</th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>...</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>...</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table>
Note: The relationship between the data and segment output is determined regardless of the number of shift clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>AC conversion signal input of LCD drive output</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD} : 0V, V_{SS}: –2.7 to –5.5V_{dc}</td><td>3</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power supply</td><td>Power supply for LCD drive circuit
V_{DD}: 0V V5: –8 to –28V_{dc}
$V_{DD} \geq V0 \geq V2 \geq 6/9\ V5$
*1 $3/9\ V5 \geq V3 \geq V5$</td><td>8</td></tr>
<tr><td>DSPOFF</td><td>I</td><td>Forced blank input
When the signal level is low, the output is forcibly set to V0 level.
Note: if this function is used, the SED1631 cannot be used as a pair.</td><td>1</td></tr>
</table>

*1. A pair of V0 to V5 must always be connected to their dedicated LCD power supplies.

Total: 107

■ ELECTRICAL CHARACTERISTICS

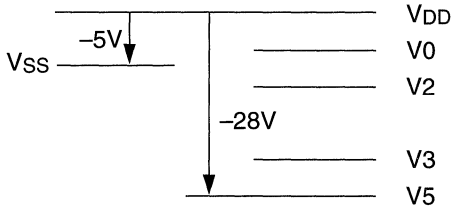
● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	V5	–30.0 to +0.3	V
Power voltage (3)	V0, V2, V3	V5 – 0.3 to V_{DD} + 0.3	V
Input voltage	VI	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	VO	V_{SS} – 0.3 to V_{DD} + 0.3	V
EIO output current	IO1	20	mA
Operating temperature	T_{OPR}	–40 to +85	°C
Storage temperature 1	T_{STG1}	–65 to +150	°C
Storage temperature 2	T_{STG2}	–55 to +100	°C

Notes:

1. All voltages are based on V_{DD} = 0V.
2. Storage temperature 1 defines the storage temperature of the separate chip, and storage temperature 2 defines the TAB mounted chip.
3. The V0, V2 and V4 voltages must always satisfy the following:

   $V_{DD} \geq V0 \geq C2 \geq C3 \geq V5$



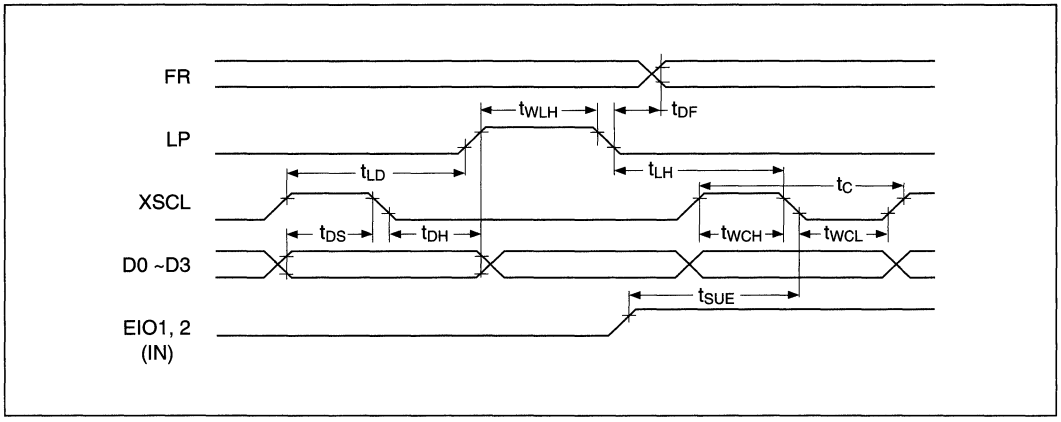
4. If the logic power supply is floating or if it exceeds $V_{SS} = -2.6V_{dc}$ when the LCD drive is powered, the LSI may be destroyed permanently. Care must be taken especially when the system power supply is turned on or off.

● DC Characteristics

V_{DD} = V0 = 0V, V_{SS} = –5.0 V_{dc} ± 10%, Ta = –40 to +85°C unless otherwise specified.

Parameter	Symbol	Conditions	Pin Name	Min	Typ	Max	Unit
Power voltage 1	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V5	V_{SS} = –2.7 to –5.5V_{dc}	V5	–28.0	—	–12.0	V
Operation voltage	V5	Function	V5	—	—	–8.0	V
Power voltage 2	V0	Recommended value	V0	V_{DD} – 2.5	—	V_{DD}	V
Power voltage 3	V2	Recommended value	V2	3/9 × V5	—	—	V
Power voltage 4	V3	Recommended value	V3	V5	—	6/9 × V5	V
High-level input current	V_{IH}	V_{SS} = –2.7 to –5.5V_{dc}	EIO1, EIO2, FR, D0 to D3, XSCL, SHL, LP, $\overline{DSPOFF}$	0.2 × V_{SS}	—	—	V
Low-level input current	V_{IL}			—	—	0.8 × V_{SS}	V
High-level output current	V_{OH}	V_{SS} = 2.7 to 5.5V, I_{OH} = 0.6mA	EIO1, EIO2	V_{DD} – 0.4	—	—	V
Low-level output voltage	V_{OL}	V_{SS} = 2.7 to 5.5V, I_{OL} = 0.6mA		—	—	V_{SS} + 0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	D0 to D3, LP, FR, XSCL, SHL, $\overline{DSPOFF}$	—	—	2.0	µA
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$	EIO1, EIO2	—	—	5.0	µA
Static current	I_{SS}	V5 = –28.0 to –14.0Vdc, V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{SS}	—	—	25	µA
Output resistance	R_{SEG}	ΔV_{ON} = 0.5, V5 = –20.0V, V3 = 13/15×V5, V2=2/15×V5, V0= V_{DD}	O0 to O79	—	1.5	2.5	KΩ
Deviation in chip ON resistance	ΔR_{SEG}	ΔV_{ON} = 0.5 V0 = +36.0V, 1/24	O0 to O159	—	—	90	Ω
Operating current (1)	I_{SS}	V_{SS} = –5.0V_{dc}, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{XSCL} = 2.69MHz, f_{LP} = 16.8KHz, f_{FR} = 70Hz, Input data: Stripe display, no load	V_{SS}	—	0.10	0.2	mA
		V_{SS} = –3.0V_{dc}, other conditions as above	V_{SS}	—	0.07	0.15	mA
Operating current (2)	I_5	V0 = 0.0V, V_{SS} = –5.0V, V3 = –18.6V_{dc}, V2 = –9.3V_{dc}, V5 = –28.0V_{dc}, others as for Iss	V5	—	0.02	0.05	mA
Input capacitance	C_I	Freq. = 1MHz, Ta = 25°C separate chip	D0 to D3, LP, FR, XSCL, SHL, $\overline{DSPOFF}$	—	—	8	pF
Input/output capacitance	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

- **AC Characteristics**
  - **Input Timing Characteristics**



V_{SS} = –5.0V ± 0.5V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
XSCL cycle time	t_C		100	—	ns
XSCL high-level pulse width	t_{WCH}		30	—	ns
XSCL low-level pulse width	t_{WCL}		30	—	ns
Data setup time	t_{DS}		30	—	ns
Data hold time	t_{DH}		20	—	ns
XSCL to LP rise time	t_{LD}		0	—	ns
LP to XSCL fall time	t_{LH}		40	—	ns
LP high-level pulse width	t_{WLH}	*3	40	—	ns
FR delay allowance time	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}		35	—	ns

V_{SS} = –4.5 to –2.7V, T_a = –40 to 85°C

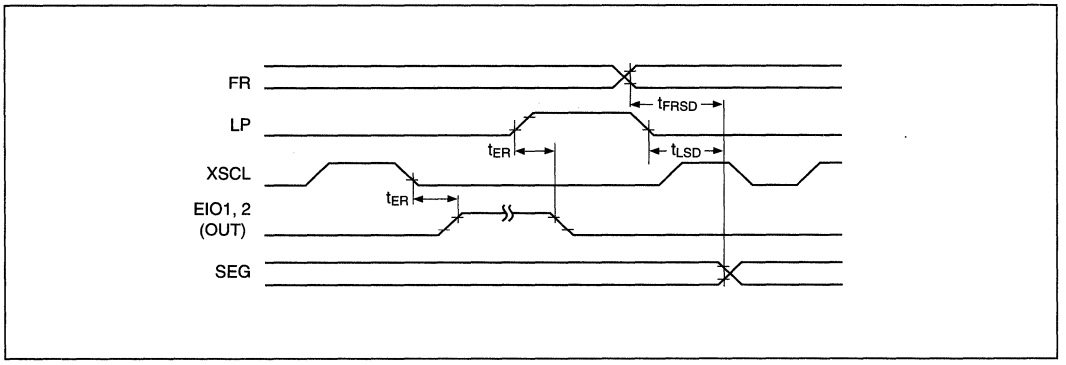
Parameter	Symbol	Conditions		Min	Max	Unit
XSCL cycle time	t_C	V_{SS} = –2.7V	*1	153	—	ns
		V_{SS} = –3.0V	*2	133	—	ns
XSCL high-level pulse width	t_{WCH}			50	—	ns
XSCL low-level pulse width	t_{WCL}			50	—	ns
Data setup time	t_{DS}			50	—	ns
Data hold time	t_{DH}			30	—	ns
XSCL to LP rise time	t_{LD}			0	—	ns
LP to XSCL fall time	t_{LH}	V_{SS} = –2.7V		75	—	ns
		V_{SS} = –3.0V		65	—	ns
LP high-level pulse width	t_{WLH}	V_{SS} = –2.7V	*3	75	—	ns
		V_{SS} = –3.0V	*3	65	—	ns
FR delay allowance time	t_{DF}			–900	+900	ns
EIO setup time	t_{SUE}	V_{SS} = –2.7V		50	—	ns
		V_{SS} = –3.0V		40	—	ns

*1. Equivalent to 6.5MHz

*2. Equivalent to 7.5MHz

*3. "t_{WLH}" defines the time when LP is high and XSCL is low.

- **AC Characteristics**
  - **Output Timing Characteristics**



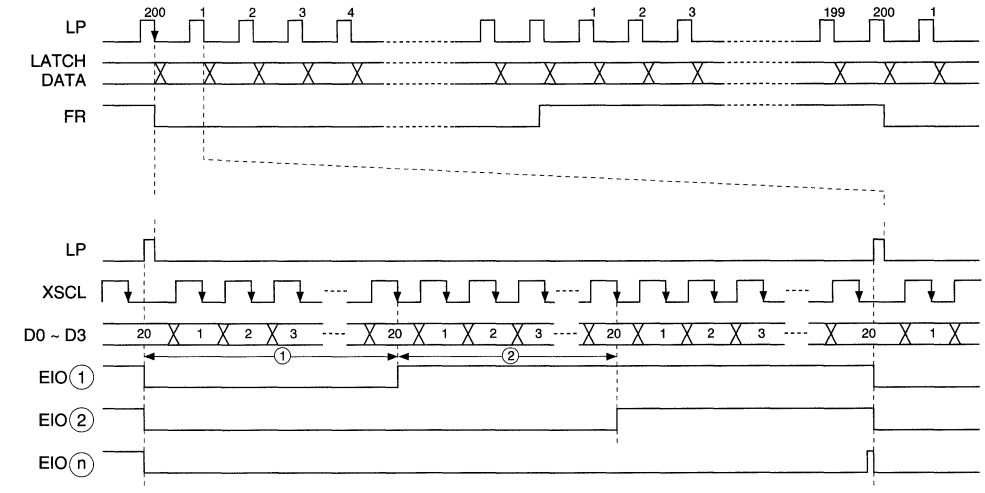
V_{SS} = –5.0V ± 0.5V, V5 = –12.0 to –28.0V

Parameter	Symbol	Conditions	Min	Max	Unit
EIO reset time	t_{ER}	C_L = 15pF (EIO)	—	90	ns
EIO output delay time	t_{DCL}		—	55	ns
Delay time from LP to segment output	t_{LSD}	C_L = 100pF (0...n)	—	200	ns
Delay time from FR to segment output	t_{FRSD}		—	400	ns

V_{SS} = –4.5 to –2.7V, V5 = –12.0 to –28.0V

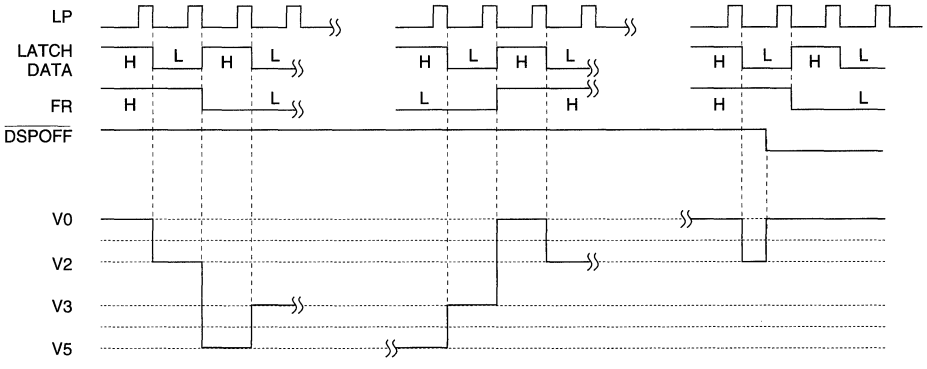
Parameter	Symbol	Conditions		Min	Max	Unit
EIO reset time	t_{ER}	C_L = 15pF (EIO)		—	150	ns
EIO output delay time	t_{DCL}		V_{SS} = –2.7V	—	95	ns
			V_{SS} = –2.7V	—	85	ns
Delay time from LP to segment output	t_{LSD}	C_L = 100pF (0...n)		—	400	ns
Delay time from FR to segment output	t_{FRSD}			—	800	ns

● **Timing Diagram (assuming 1/200 duty) (This diagram is provided only as a reference)**

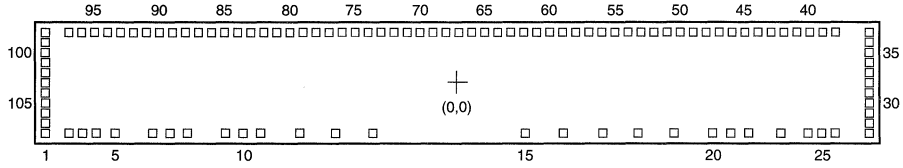


(1) to (n) indicate driver cascade numbers.

* For high-speed data transmission, it is necessary to lengthen the XSCL period in the LP pulse insertion timing to ensure the specified values of LP → XSCL (tLH).



■ PAD LAYOUT



- Chip size ..... 11.59 × 1.40 mm
- Pad pitch ..... 105 μm (Min)
- Chip thickness ..... 625 μm ± 25μm

(1) SED1640D$_{OB}$ Au bump specifications (reference)

Bump size A ..... 106 μm × 80 μm × 4 μm ..... (Pad Nos. 2 to 26)
Bump size B ..... 86 μm × 91 μm × 4 μm ..... (Pad Nos. 1, 27, 37, 98)
Bump size C ..... 86 μm × 68 μm × 4 μm ..... (Pad Nos. 28 to 36, 99 to 107)
Bump size D ..... 82 μm × 74 μm × 4 μm ..... (Pad Nos. 38 to 97)
Bump height A to D ..... 22.5 ± 5.5μm ..... (Pad Nos. 1 to 107)

■ PAD COORDINATES

Pad No.	Pin Name	X	Y
2	V0	–5345	–541
3	V2	–5164	–541
4	V3	–4984	–541
5	V5	–4594	–541
6	VSS	–4091	–541
7	Dummy	–3839	–541
8	SHL	–3587	–541
9	Dummy	–3065	–541
10	Dummy	–2828	–541
11	VDD	–2590	–541
12	$\overline{\text{DSPOFF}}$	–2086	–541
13	FR	–1583	–541
14	LP	–1079	–541
15	XSCL	1079	–541
16	D0	1583	–541
17	D1	2086	–541
18	D2	2590	–541
19	Dummy	3065	–541
20	D3	3587	–541
21	Dummy	3839	–541
22	VSS	4091	–541
23	V5	4594	–541
24	V3	4984	–541
25	V2	5164	–541
26	V0	5345	–541
27	EIO1	5644	–544
28	O0	5644	–426
29	O1	5644	–320
30	O2	5644	–215
31	O3	5644	–109
32	O4	5644	–4
33	O5	5644	102
34	O6	5644	207
35	O7	5644	313
36	O8	5644	418
37	O9	5644	546
38	O10	5269	553
39	O11	5090	553
40	O12	4912	553
41	O13	4733	553
42	O14	4554	553
43	O15	4376	553
44	O16	4197	553
45	O17	4019	553
46	O18	3840	553
47	O19	3661	553
48	O20	3483	553
49	O21	3304	553
50	O22	3126	553
51	O23	2947	553
52	O24	2768	553
53	O25	2590	553
54	O26	2411	553
55	O27	2233	553
56	O28	2054	553
57	O29	1875	553
58	O30	1697	553
59	O31	1518	553
60	O32	1340	553
61	O33	1161	553
62	O34	982	553
63	O35	804	553
64	O36	625	553
65	O37	447	553
66	O38	268	553
67	O39	89	553
68	O40	–89	553
69	O41	–268	553
70	O42	–447	553
71	O43	–625	553
72	O44	–804	553
73	O45	–982	553
74	O46	–1161	553
75	O47	–1340	553
76	O48	–1518	553
77	O49	–1697	553
78	O50	–1875	553
79	O51	–2054	553
80	O52	–2233	553
81	O53	–2411	553
82	O54	–2590	553
83	O55	–2768	553
84	O56	–2947	553
85	O57	–3126	553
86	O58	–3304	553
87	O59	–3483	553
88	O60	–3661	553
89	O61	–3840	553
90	O62	–4019	553
91	O63	–4197	553
92	O64	–4376	553
93	O65	–4554	553
94	O66	–4733	553
95	O67	–4912	553
96	O68	–5090	553
97	O69	–5269	553
98	O70	–5644	546
99	O71	–5644	418
100	O72	–5644	313
101	O73	–5644	207
102	O74	–5644	102
103	O75	–5644	–4
104	O76	–5644	–109
105	O77	–5644	–215
106	O78	–5644	–320
107	O79	–5644	–426
1	EIO2	–5644	–544

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LCD SEGMENT DRIVER

■ DESCRIPTION

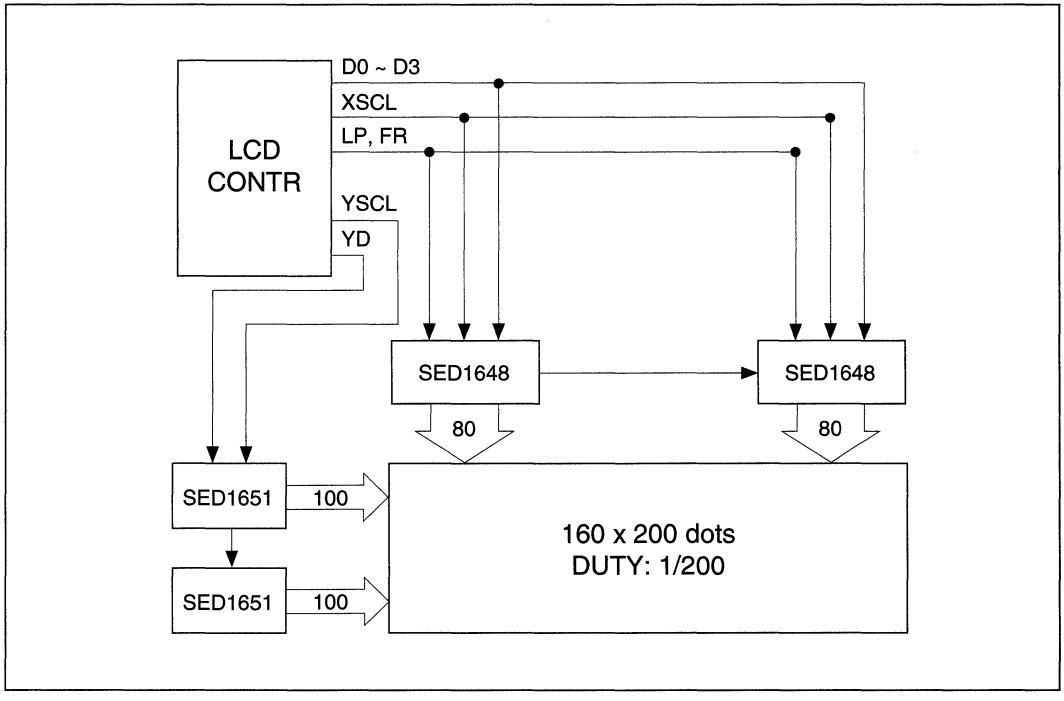
The SED1648 is an 80-output dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/300). The LSI has a wide range of the LCD driving voltages. The offset bias regulation of the liquid crystal power is possible depending on the V_{DD} level. These unique features allow the SED1648 to interface with a variety of LCD panels. The device does not require a controller to implement an enable daisy chain technology.

The SED1648 is used in conjunction with the SED1651 (100-output row driver) or the SED1635 (100-bit row driver) to drive a large-capacity dot matrix LCD panel.

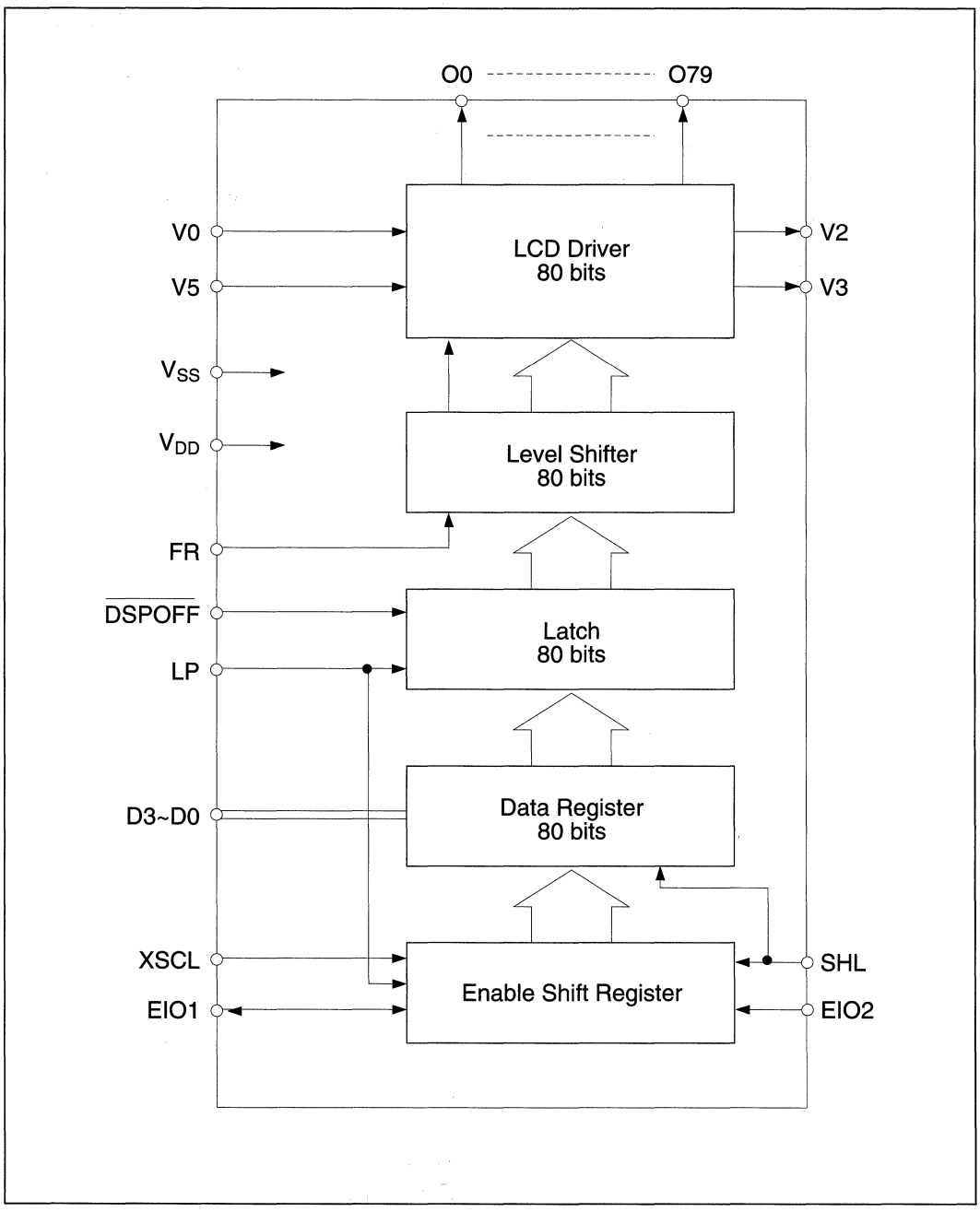
■ FEATURES

- Low-power CMOS technology
- 80-bit segment (column) driver
- High-speed 4-bit bus
- Duty cycle ..... 1/100 to 1/300
- Shift clock frequency ..... 10 MHz max
- Ability to adjust offset bias of the LCD source relative to V_{DD}
- Daisy chain enable support
- Pin selection of the output shift direction
- LCD voltage ..... –8 to –28V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... Al pad slim DIE (D_{OA})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Enable Shift Register

The enable shift register is a bidirectional shift register where the direction of the shift is selected by the SHL input. The output of this shift register is used to store the data bus signals in the data register.

When the enable signal is in a disable state, the internal clock signal and data bus are fixed at "L", placing the chip in power save mode.

When multiple segment drivers are used, the EIO terminals of the various drivers are cascade connected and the EIO terminal of the first driver is connected to V_{DD}.

The enable control circuit automatically senses when 80 bits worth of data have been received, and sends the enable signal, thus eliminating the need for a control signal from the control LSI.

● Data Register

This is a register to convert the data bus signal from serial to parallel using the output of the enable shift register. Consequently, the relationships between the serial display data and the segment output is determined independently of the shift clock input number.

● Latch

The latch receives the contents of the data registers when triggered by the falling edge of the LP, and outputs them to the level shifter.

● Level Shifter

The level shifter is a level interface circuit which converts the signal voltage level from a logic circuit level to the LC driver voltage level.

● LCD Driver

The LCD driver outputs the LC drive voltage.

The relationship between the data bus signal, the AC signal FR, and the segment output voltage is as follows:

$\overline{DSPOFF}$	Data Bus Signal	FR Voltage	O Output
H	H	H	V0
		L	V5
	L	H	V2
		L	V3
L	—	—	V0

■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>O0 to O79</td><td>O</td><td>Segment (column) output to drive LC.
Output transition occurs on falling edge of LP.</td><td>80</td></tr>
<tr><td>D0 to D3</td><td>I</td><td>Display data input.</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (triggers on falling edge)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (triggers on falling edge)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O
This is set to input or output depending on the level of the SHL input. The output is reset by the LP input, and once the 80-bit data reception is complete, the terminals automatically rise to “H”.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and EIO terminal I/O control input.
When the data has been input to terminals (D3, D2, ..., D0) in the order (a3, a2, a1, a0) (b3, b2, b1, b0) ... (t3, t2, t1, t0), the relationship between the data and the segment output is as shown in the table below:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th>...</th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a3</td><td>a2</td><td>a1</td><td>...</td><td>t2</td><td>t1</td><td>t0</td><td>O</td><td>I</td></tr>
<tr><td>H</td><td>t0</td><td>t1</td><td>t2</td><td>...</td><td>a1</td><td>a2</td><td>a3</td><td>I</td><td>O</td></tr>
</table>
Note: The relationship between the data and the segment output is independent of the shift clock number.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC drive output AC signal input</td><td>1</td></tr>
<tr><td>VDD, VSS</td><td>Power</td><td>Power source for logic: VDD : 0V VSS : –2.7 to –5.5V</td><td>4</td></tr>
<tr><td>V0, V2,
V3, V5</td><td>Power</td><td>LC drive circuit power:
VDD : 0V
V5 : –8 to –28V
VDD ≥ V0 ≥ V2 ≥ 6/9 × V5
3/9 × V5 ≥ V3 ≥ V5
*1</td><td>8</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>Forced blank input.
“L” level outputs are forced to the V0 level.</td><td>1</td></tr>
</table>

Total 107 (of which 5 are NC)

Note: *1. The pairs V0-V5 must each be attached to the LCD power source.

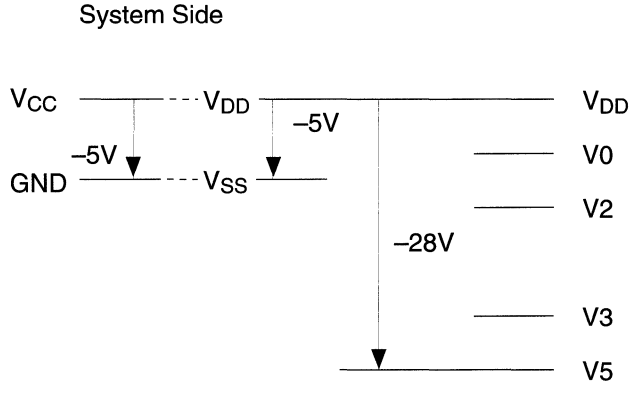
■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	V5	–30.0 to +0.3	V
Power voltage (3)	V0, V2, V3	V5 – 0.3 to V_{DD} + 0.3	V
Input voltage	VI	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	VO	V_{SS} – 0.3 to V_{DD} + 0.3	V
EIO output current	IO	20	mA
Operating temperature	T_{OPR}	–40 to +85	°C
Storage temperature 1	T_{STG1}	–65 to +150	°C

Notes:

1. All voltages are given relative to V_{DD} = 0V.
2. Storage temperature 1 is the recommendation for the chip itself.
3. Ensure that the relationship between V0, V2 and V3 is always as follows: $V_{DD} \geq V0 \geq V2 \geq V3 \geq V5$



4. The LSI may be permanently damaged if the logic system power is floating or V_{SS} is less than or equal to –2.6V when power is applied to the LC drive circuit system. Special caution must be paid to the power sequences when turning the power on and off.

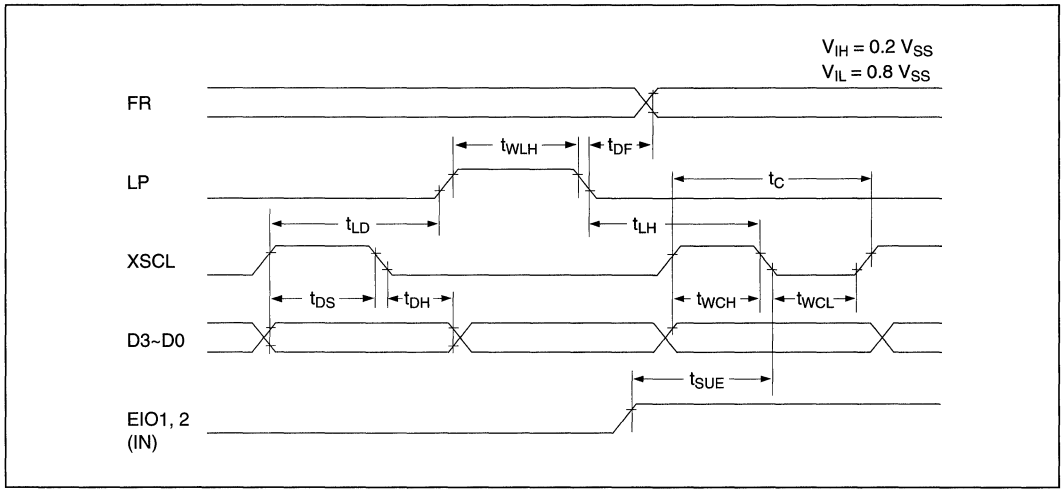
● DC Electrical Characteristics

Unless otherwise specified, V_{DD} = V0 = 0V, V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Applicable Pins	Min	Typ	Max	Unit
Power voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V5	V_{SS} = –2.7 to –5.5V	V5	–28.0	—	–12.0	V
Possible operating voltage	V5	Function	V5	—	—	–8.0	V
Power voltage (2)	V0	Recommended value	V0	V_{DD} – 2.5	—	V_{DD}	V
Power voltage (3)	V2	Recommended value	V2	3/9 × V5	—	V_{DD}	V
Power voltage (4)	V3	Recommended value	V3	V5	—	6/9 × V5	V
High-level input voltage	V_{IH}	V_{SS} = –2.7 to –5.5V	EIO1, EIO2, FR, D0 ~ D3, XSCL, SHL, LP, DSPOFF	0.2 × V_{SS}	—	—	V
Low-level input voltage	V_{IL}			—	—	0.8 × V_{SS}	V
High-level output voltage	V_{OH}	V_{SS} = –2.7 to –5.5V, I_{OH} = –0.6mA	EIO1, EIO2	V_{DD} – 0.4	—	—	V
Low-level output voltage	V_{OL}	V_{SS} = –2.7 to –5.5V, I_{OL} = 0.6mA		—	—	V_{SS} + 0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	D0 ~ D3, LP, FR, XSCL, SHL, DSPOFF	—	—	2.0	µA
I/O leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$	EIO1, EIO2	—	—	5.0	µA
Static current	I_{SS}	V5 = –28.0 to –14.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{SS}	—	—	25	µA
Output resistance	R_{SEG}	ΔVON = 0.5V, V5 = –20.0V, V3 = 13/15 × V5, V2 = 2/15 × V5, V0 = V_{DD}, T_a = 25°C	O0 ~ O79	—	1.5	1.9	KΩ
Average operating consumption current (1)	I_{SS}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{XSCL} = 2.69MHz, f_{LP} = 16.8KHz, f_{FR} = 70Hz; Input data: checker pattern display, no load	V_{SS}	—	0.10	0.2	mA
		V_{SS} = –3.0V; other parameters are the same as for V_{SS} = –5V		—	0.07	0.15	
Average operating consumption current (2)	I5	V_{SS} = –5.0V, V0 = 0.0V, V2 = –9.3V, V3 = –18.6V, V5 = –28.0V; other parameters are the same as for the I_{SS} item	V5	—	0.02	0.05	mA
Input terminal capacitance	C_I	Freq. = 1MHz, T_a = 25°C, Chip alone	D0 ~ D3, LP, FR, XSCL, SHL, DSPOFF	—	—	8	pF
I/O terminal capacitance	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

● AC Characteristics

○ Input Timing Characteristics



V_{SS} = –5.0 ± 0.5V, Ta = –40 to 85°C

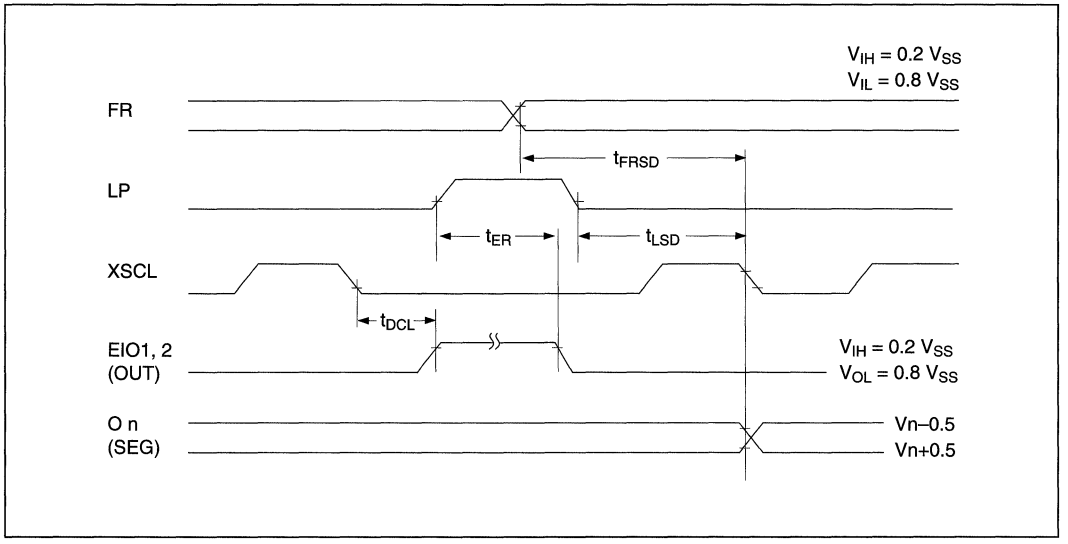
Parameter	Symbol	Conditions	Min	Max	Unit
XSCL frequency	tC	—	100	—	ns
XSCL high-level pulse width	tWCH	—	30	—	ns
XSCL low-level pulse width	tWCL	—	30	—	ns
Data setup time	tDS	—	20	—	ns
Data hold time	tDH	—	10	—	ns
XSCL → LP rising edge	tLD	—	0	—	ns
LP → XSCL falling edge	tLH	—	40	—	ns
LP high-level pulse width	tWLH	*3 —	40	—	ns
Allowable FR delay	tDF	—	–900	+900	ns
EIO setup time	tSUE	—	35	—	ns

VSS = –4.5 to –2.7V, Ta = –40 to 85°C

Parameter	Symbol	Conditions		Min	Max	Unit
XSCL frequency	tC	V_{SS} = –2.7V	*1	153	—	ns
		V_{SS} = –3.0V	*2	133	—	ns
XSCL high-level pulse width	tWCH	—		50	—	ns
XSCL low-level pulse width	tWCL	—		50	—	ns
Data setup time	tDS	—		30	—	ns
Data hold time	tDH	—		15	—	ns
XSCL → LP rising edge	tLD	—		0	—	ns
LP → XSCL falling edge	tLH	V_{SS} = –2.7V		75	—	ns
		V_{SS} = –3.0V		65	—	ns
LP high-level pulse width	tWLH	V_{SS} = –2.7V	*3	75	—	ns
		V_{SS} = –3.0V	*3	65	—	ns
Allowable FR delay	tDF	—		–900	+900	ns
EIO setup time	tSUE	V_{SS} = –2.7V		60	—	ns
		V_{SS} = –3.0V		50	—	ns

Notes: *1. At 6.5 MHz.
*2. At 7.5 MHz.
*3. tWLH specifies when LP is "H" and XSCL is "L".
*4. The tr and tf input signals are specified at 20 ns.

○ Output Timing Characteristics



V_{DD} = –5.0 ± 0.5V, V5 = –12.0 to –28.0V

Parameter	Symbol	Conditions	Min	Max	Unit
EIO reset time	t_{ER}	CL = 15pF (EIO)	—	90	ns
EIO output delay time	t_{DCL}		—	55	ns
LP → SEG output delay time	t_{LSD}	CL = 100pF (On)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	400	ns

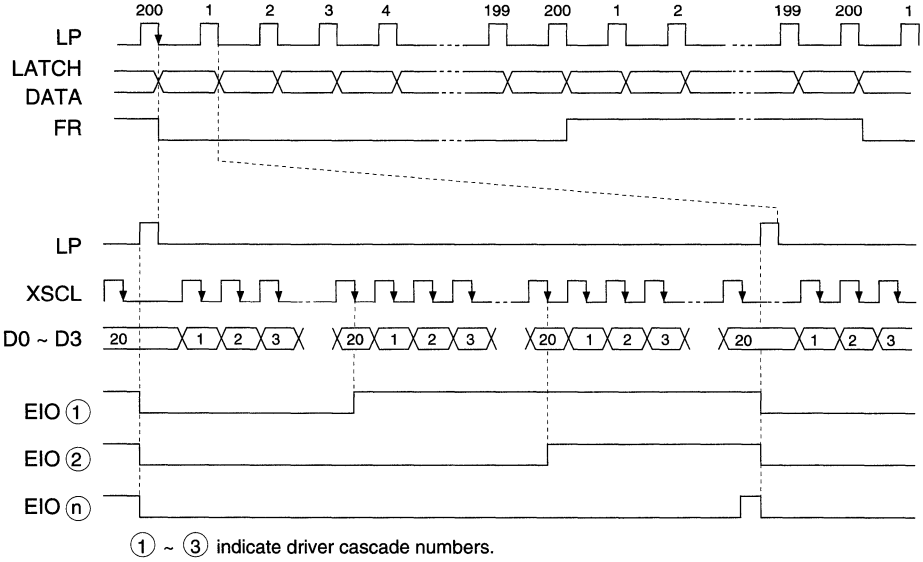
V_{DD} = –4.5 to –2.7V, V5 = –12.0 to –28.0V

Parameter	Symbol	Conditions		Min	Max	Unit
EIO reset time	t_{ER}	CL = 15pF (EIO)	—	—	150	ns
EIO output delay time	t_{DCL}		V_{SS} = –2.7V	—	85	ns
			V_{SS} = –3.0V	—	75	ns
LP → SEG output delay time	t_{LSD}	CL = 100pF (On)		—	400	ns
FR → SEG output delay time	t_{FRSD}			—	800	ns

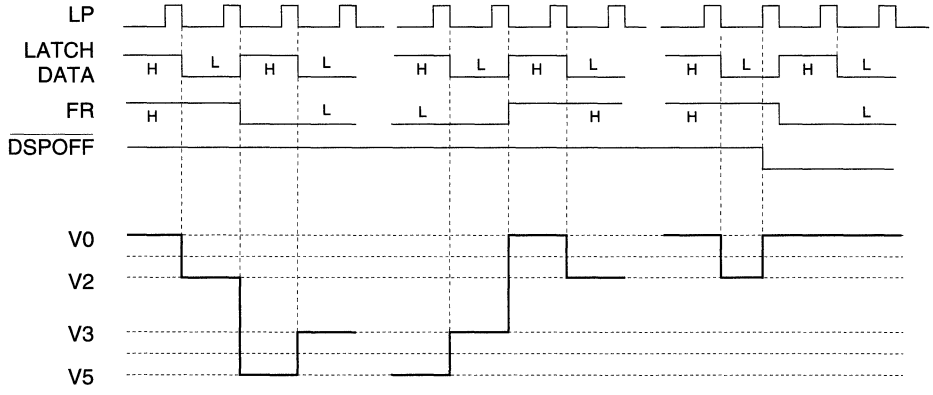
Notes: *1. The tr and tf input signals are specified at 20 ns.

● Timing Diagram

Timing diagram (assuming 1/200 duty). (This diagram provided only as a reference.)



① ~ ③ indicate driver cascade numbers.



■ LCD DRIVING POWER

● Method of Forming Each Voltage Level

The simplest way to obtain the voltage levels for driving the LCs is to use resistive voltage dividers between V5 and V_{DD}, and to drive the LCs with op amp voltage followers.

In consideration of the use of op amps, V0 (the highest electrical level) and V_{DD} are separated and given separate terminals.

However, when the voltage level of V0 is below V_{DD} and the voltage difference between the two is large, the performance of the LC output driver is reduced. Therefore, ensure that the voltage gap between V0 and V_{DD} is in the range of 0V – 2.5V.

When op amps are not going to be used, connect V0 to V_{DD}.

Permanent damage may result to the LSI when there is serial resistance in the V5 or V_{DD} power lines. This is because the voltage drop that will occur at V5 or V_{DD} when the signal changes will cause the power level relationships within the LCD (i.e., $V_{DD} \geq V0 \geq V2 \geq V3 \geq V5$) to fail.

When a guard resistance is inserted, voltage stabilization using a capacitance is necessary.

● Cautions During Power Up and Power Down

Because of the high voltage of the LC driving system of this LSI, if the power to the logic system is floating or if V_{SS} is greater than or equal to –2.6V when a high voltage is applied to the LC driving system, or if the LC driving signal is output before the LC driving system voltage stabilizes, then too much current will flow, causing damage to the LSI.

It is recommended that the display off function ($\overline{DSPOFF}$) be used to keep the LCD driver output level at V0 until the LCD drive system voltage stabilizes.

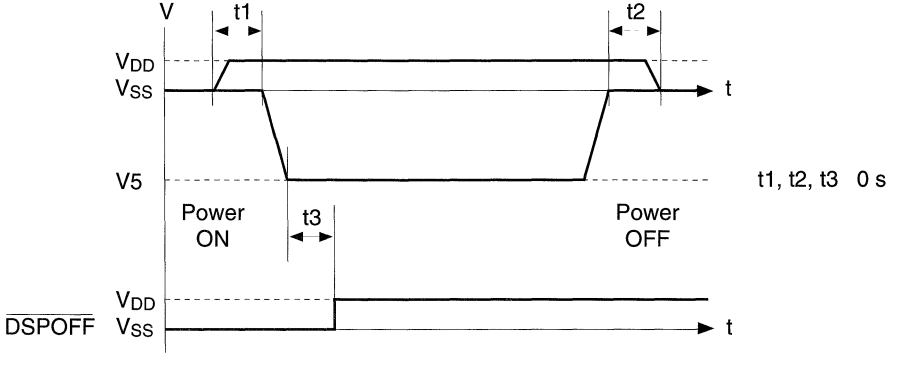
Follow the sequences below during power up and power down:

Power up: Logic system on → LC drive system on (or simultaneous)

Power down: LC drive system off → Logic system off (or simultaneous)

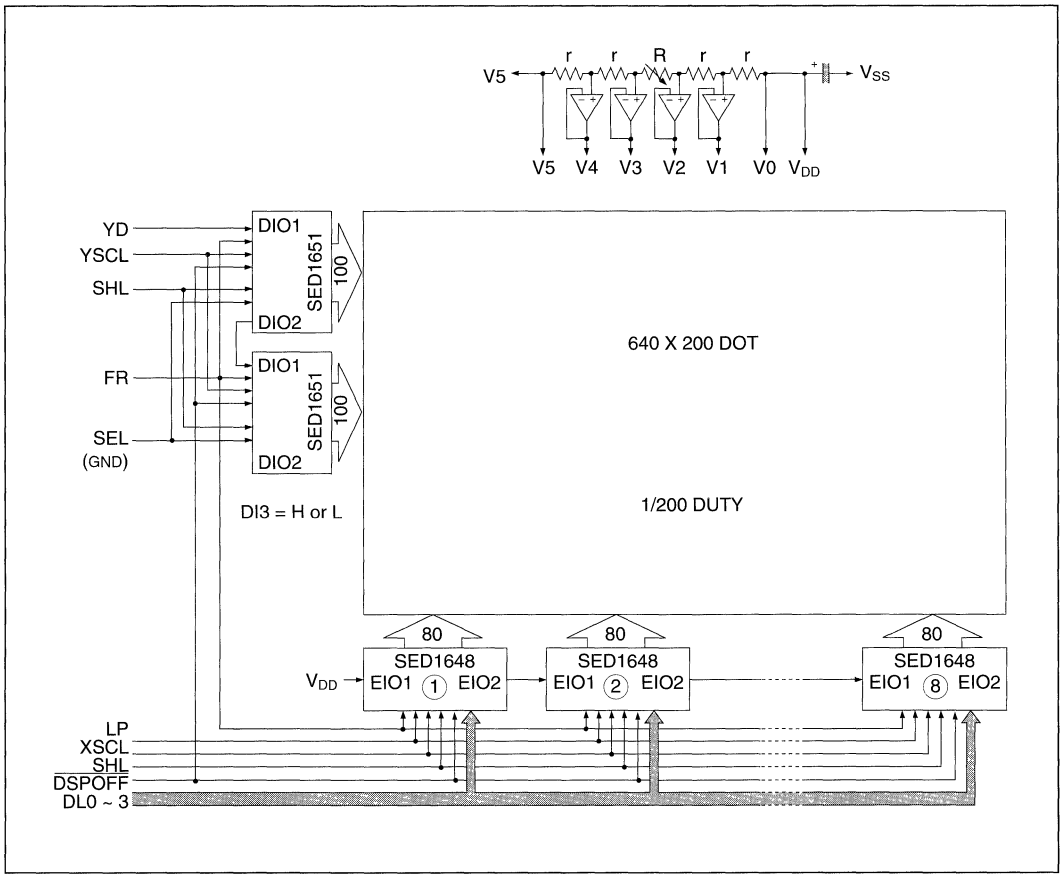
As a way to prevent excessive current, insert a high-speed fuse or guard resistance in series with the LC power source.

The optimal value of the guard resistance must be selected based on the capacitance of the LC cells.

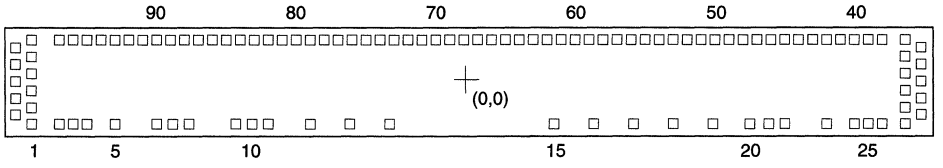


■ EXAMPLE OF CONNECTION

● Large Screen LCD Structure Diagram

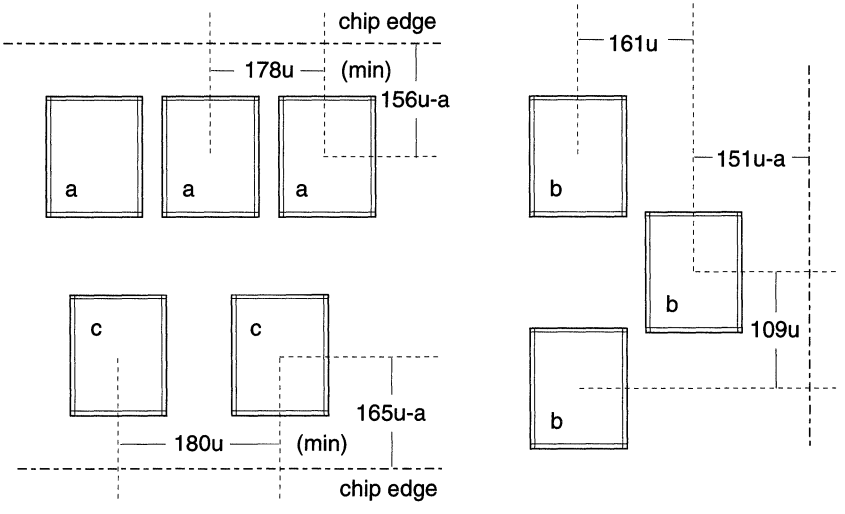


■ PAD LAYOUT



Chip size ..... 11.93 mm × 1.45 mm
Chip thickness ..... 400 μm (TYP)

Al Pad Specifications (SED1648D0A)



Pad a aperture (X, Y): ..... 100 × 120 μm PAD No. 38-97
Pad b aperture (X, Y): ..... 110 × 110 μm PAD No. 28-37, 98-107
Pad c aperture (X, Y): ..... 110 × 110 μm PAD No. 1-27

■ PAD COORDINATES

Unit: μm

Pad No.	Pad Name	X Coord.	Y Coord.
1	EIO2	–5653	–560
2	V0	–5297	–560
3	V2	–5117	–560
4	V3	–4936	–560
5	V5	–4547	–560
6	V_{SS}	–4091	–560
7	NC	–3839	–560
8	SHL	–3587	–560
9	NC	–3065	–560
10	NC	–2828	–560
11	V_{DD}	–2590	–560
12	$\overline{DSPOFF}$	–2086	–560
13	FR	–1583	–560
14	LP	–1079	–560
15	XSCL	1079	–560
16	D0	1583	–560
17	D1	2086	–560
18	D2	2590	–560
19	NC	3065	–560
20	D3	3587	–560
21	NC	3839	–560
22	V_{SS}	4091	–560
23	V5	4594	–560
24	V3	4984	–560
25	V2	5164	–560
26	V0	5345	–560
27	EIO1	5653	–560
28	O0	5814	–414
29	01	5653	–305
30	02	5814	–196
31	03	5653	–86
32	04	5814	23
33	05	5653	132
34	06	5814	241
35	07	5653	351
36	08	5814	460
37	09	5653	569
38	010	5268	569
39	011	5090	569
40	012	4911	569
41	013	4732	569
42	014	4554	569
43	015	4375	569
44	016	4197	569
45	017	4018	569
46	018	3839	569
47	019	3661	569
48	020	3482	569
49	021	3304	569
50	022	3125	569
51	023	2946	569
52	024	2768	569
53	025	2589	569
54	026	2411	569
55	027	2232	569
56	028	2053	569
57	029	1875	569
58	030	1696	569
59	031	1518	569
60	032	1339	569
61	033	1160	569
62	034	982	569
63	035	803	569
64	036	625	569
65	037	446	569
66	038	267	569
67	039	89	569
68	040	–89	569
69	041	–267	569
70	042	–446	569
71	043	–625	569
72	044	–803	569
73	045	–982	569
74	046	–1160	569
75	047	–1339	569
76	048	–1518	569
77	049	–1696	569
78	050	–1875	569
79	051	–2053	569
80	052	–2232	569
81	053	–2411	569
82	054	–2589	569
83	055	–2768	569
84	056	–2946	569
85	057	–3125	569
86	058	–3304	569
87	059	–3482	569
88	060	–3661	569
89	061	–3839	569
90	062	–4018	569
91	063	–4197	569
92	064	–4375	569
93	065	–4554	569
94	066	–4732	569
95	067	–4911	569
96	068	–5090	569
97	069	–5268	569
98	070	–5653	569
99	071	–5814	460
100	072	–5653	351
101	073	–5814	241
102	074	–5653	132
103	075	–5814	23
104	076	–5653	–86
105	077	–5814	–195
106	078	–5653	–305
107	079	–5814	–414

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SED1681

80-BIT EXPANSION LCD DRIVER

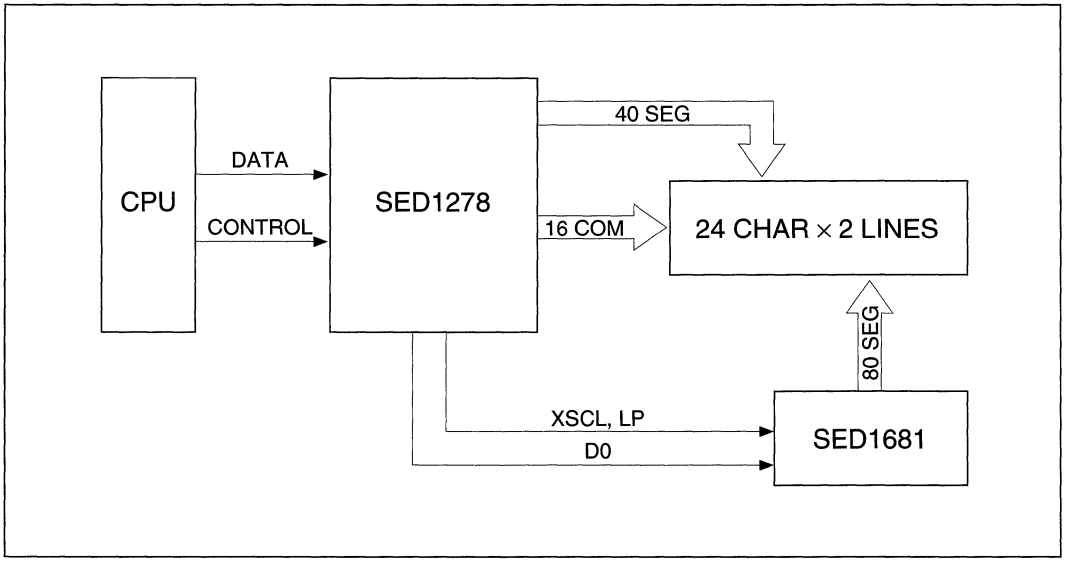
■ DESCRIPTION

The SED1681 is an 80-bit expansion segment (column) driver suitable for driving high-contrast, small-capacity dot matrix liquid crystal displays with a duty from 1/8 to 1/32. It is best suited for expanding the segment drive capability of LCD controllers such as the SED1278F, or a 4-bit microcomputer.

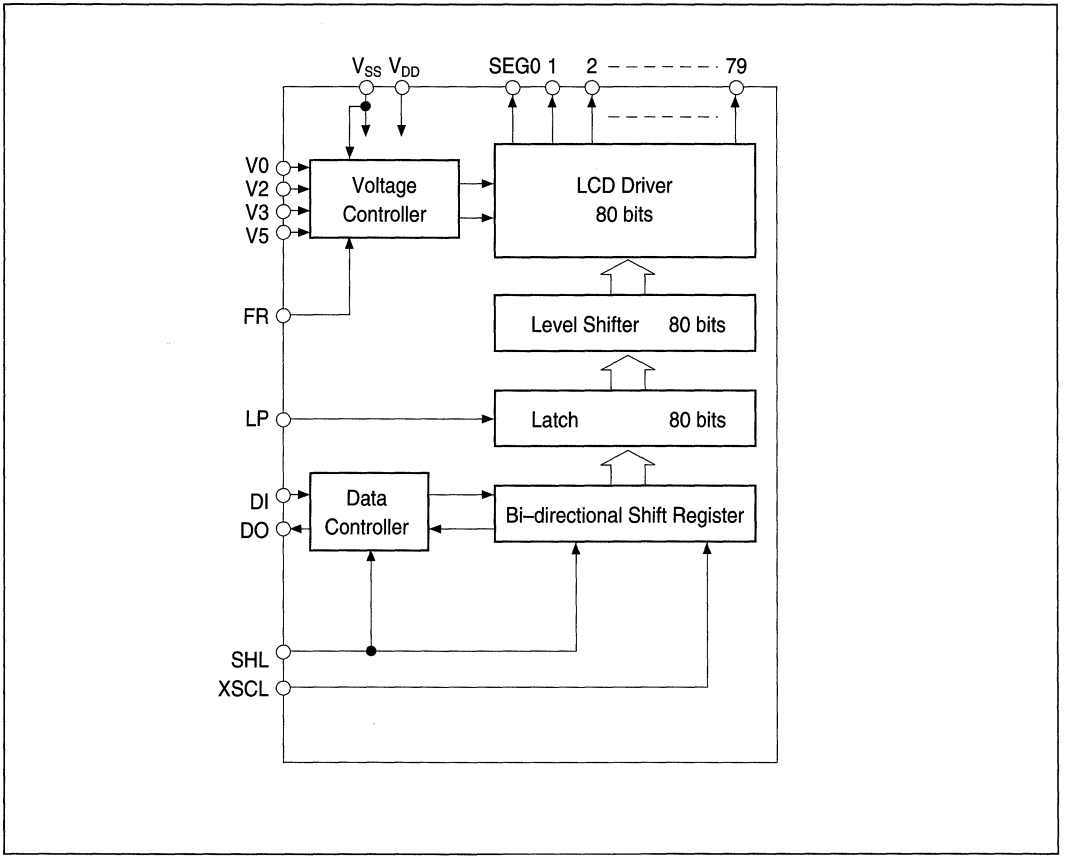
■ FEATURES

- Low-power CMOS technology
- 80-bit segment (column) driver
- Serial input data
- Duty cycle ..... 1/8 to 1/32
- Suitable for use with a wide range of LCD controllers
- Capable of a serial cascade connection
- Wide range of LCD voltage ..... –3.0V to –12V
- Supply voltage ..... 2.4V to 6.0V
- Package ..... QFP5-100 pin (F0A)
  DIE: Al pad chip (D0A)

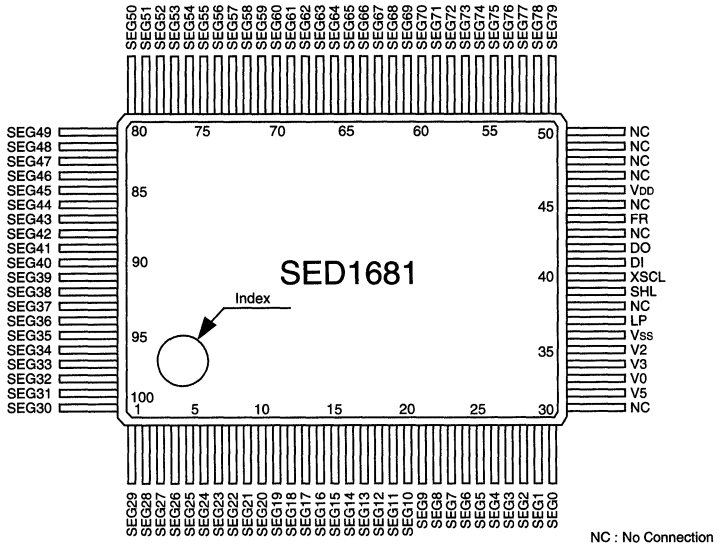
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTION

Pin/Pad		Input/ Output	Description
Number	Name		
1 to 30, 51 to 100	SEG0 to SEG79	O	Liquid crystal segment drive outputs Segment outputs change on the falling edge of the LP input signal.
40	XSCL	I	Shift clock input Shift register data is shifted on the falling edge of this signal.
37	LP	I	Display data strobe. Data from the shift register is strobed on to the display data latch on the falling edge of this signal.
41	DI	I	Serial data input
42	DO	O	Serial data output
39	SHL	I	Shift direction select This pin selects the data shift direction from bit 0 towards bit 79 or in reverse.
44	FR	I	Liquid crystal frame signal input
46	V_{DD}	—	Logic power supply
36	V_{SS}	—	Ground
32 to 35	V_0, V_2, V_3, V_5	—	LCD drive voltage supply inputs These voltages should satisfy the following conditions: $V_{DD} \geq V_0$, $V_{DD} \geq V_2 \geq 1/2 \times V_5$, $1/2 \times V_5 \geq V_3 \geq V_5$
31, 38, 43, 45, 47 to 50	NC	—	No connection

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to 0.3	V
Supply voltage (2)	V_5	–15.0 to 0.3	V
Supply voltage (3)	V_0, V_2, V_3	–15.0 to 0.3	V
Input voltage	V_{IN}	V_{SS} –0.3 to 0.3	V
Output voltage	V_O	V_{SS} –0.3 to 0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature, time	T_{sol}	260°C, 10 sec (at lead)	—

Notes:

1. All voltages are based on V_{DD} = 0V.

2. Never use wave soldering to mount packages, or any other method that applies excessive thermal stress to a package, as this will reduce its heat dissipation capacity.

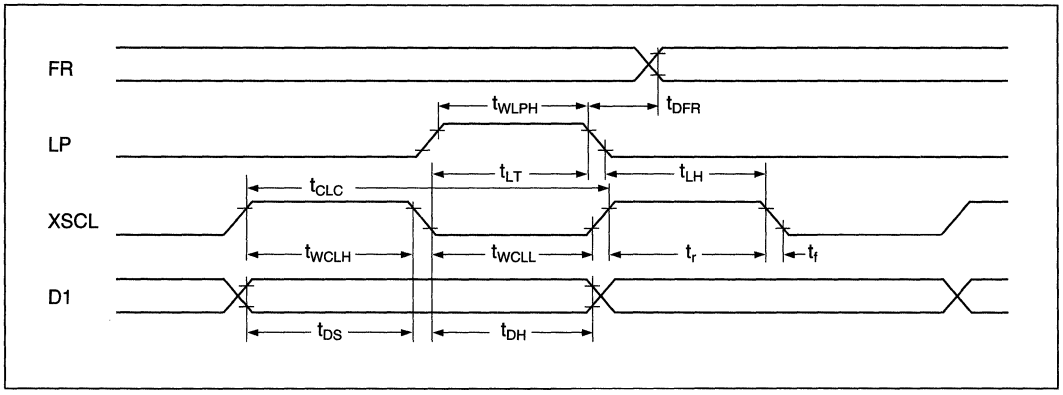
● DC Electrical Characteristics

(Unless otherwise specified, $V_{DD} = V_0 = 0$ V, $V_{SS} = -5.0$ V ± 10%, $T_a = -20$ to 75°C)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Supply voltage (1)	V_{SS}		V_{SS}	–6.0	–5.0	–2.4	V
Recommended operating voltage	V_5		V_5	–12.0	—	–3.0	V
Permitted operating voltage	V_5	Operational limits *1	V_5	–12.0	—	–2.5	V
Supply voltage (2)	V_2	Recommended value	V_2	$1/2 \times V_5$	—	V_{DD}	V
Supply voltage (3)	V_3	Recommended value	V_3	V_5	—	$1/2 \times V_5$	V
High-level input voltage	V_{IH}		DI, XSCL LP, SHL, FR	$0.2xV_{SS}$	—	V_{DD}	V
Low-level input voltage	V_{IL}			V_{SS}	—	$0.8xV_{SS}$	V
High-level output voltage	V_{OH}	$I_{OH} = -0.6$ mA	DO	–0.4	—	—	V
Low-level output voltage	V_{OL}	$I_{OL} = 0.6$ mA		—	—	$V_{SS}+0.4$	V
Input leakage current	I_{LI}	$0 V \le V_{IN} \le V_{SS}$	SHL, FR XSCL, LP	—	0.05	2.0	µA
Output leakage current	I_{LO}	$0 V \le V_{OUT} \le V_{SS}$	DO	—	0.05	5.0	µA
Quiescent current	I_Q	$V_5 = -12.0$ V, $V_{SS} = -6.0$ V, $V_{IH} = V_{CC}$	V_{DD}	—	0.05	30	µA
Output resistance	R_{SEG}	$\Delta V_{ON} = 0.1$ V, $T_a = 25°C$, $V_5 = -8.0$V	SEG0 to SEG79	—	1.5	3.0	kΩ
		$V_5 = -5.0$V		—	3.0	8.0	
		$V_5 = -3.0$V		—	10.0	50.0	
Supply current (1)	$I_{SS\ OP}$	$V_{SS} = -5.0$ V, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, LP = 520 µs, f_{XSCL} = 400 kHz., FR = 16.7 ms, all data inputs are alternate I and O data, all output open.	V_{SS}	—	250	350	µA
Supply current (2)	$I_{5\ OP}$	$V_{SS} = -4.5$V, $V_2 = -4.8$V, $V_3 = -7.2$ V, $V_{SSH} = -12.0$ V; Other conditions as for $I_{SS\ OP}$	V_5	—	10	16	µA
Input pin capacitance	C_{IN}	$T_a = 25°C$	SHL, FR XSCL, LP	—	5	8	pF

*1. This parameter specifies the range of V5 over which operation is possible. The driver ON-resistance for the particular LCD panel being used may result in V5 exceeding the recommended operating range. The V5 operating voltage should be determined experimentally and component changes made, if necessary, to ensure operation within the recommended range

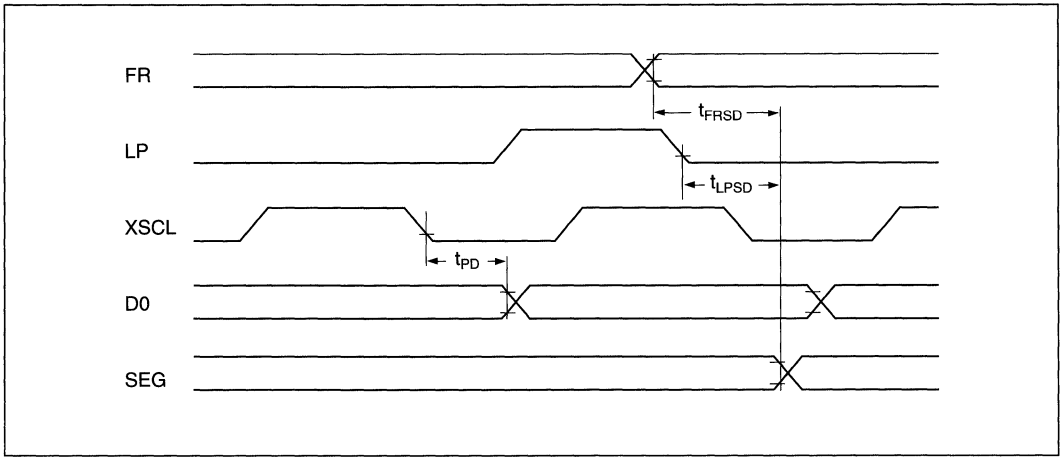
- **AC Electrical Characteristics**
  - **Input Timing**



(Vss = –6.0 V to –2.4 V, Ta = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Shift clock period	t_{CLC}		1.0	—	—	µs
Shift clock High-level pulse width	t_{WCLH}		450	—	—	ns
Shift clock Low-level pulse width	t_{WCLL}		450	—	—	ns
Data setup time	t_{DS}		140	—	—	ns
Data hold time	t_{DH}		100	—	—	ns
Latch pulse High-level pulse width	t_{WLPH}		200	—	—	ns
Shift clock to latch pulse interval	t_{LT}		200	—	—	ns
Latch hold time	t_{LH}		100	—	—	ns
Frame signal delay time	t_{DFR}		–500	—	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns

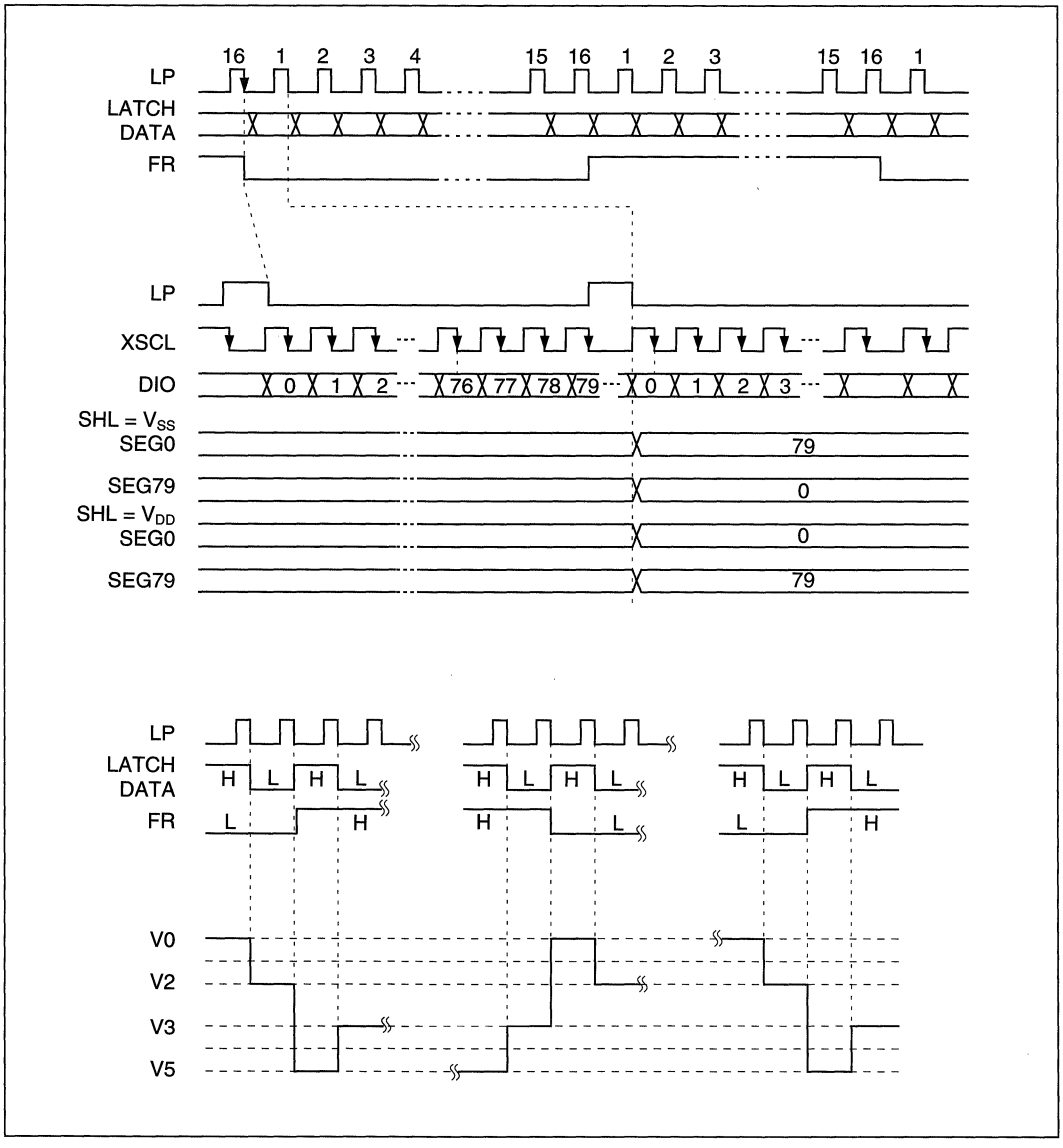
○ **Output Timing**



(V_{SS} = –6.0 V to –2.4 V, V_5 = –12.0 V to –3.0 V, T_a = –20 to 75°C)

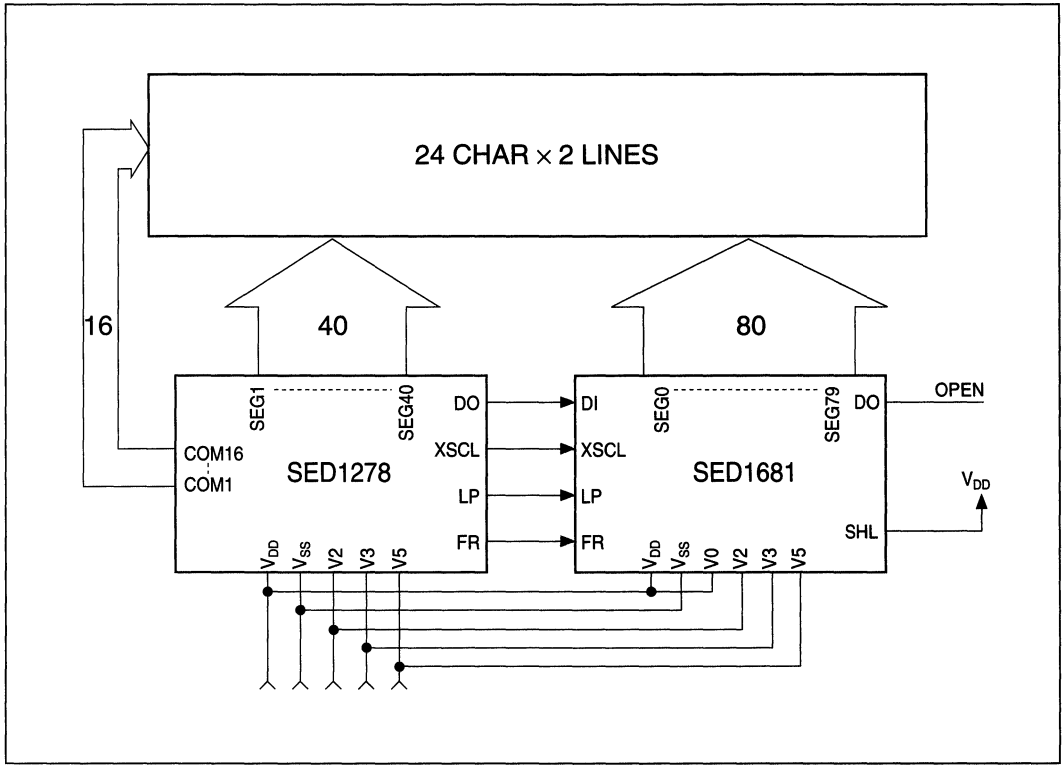
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Serial data output delay time	t_{PD}	C_L= 15 pF	—	—	250	ns
LP-SEG output delay time	t_{LPSD}	C_L= 100 pF	—	—	4.5	µs
FR-SEG output delay time	t_{FRSD}		—	—	4.5	µs

● **Timing Chart**

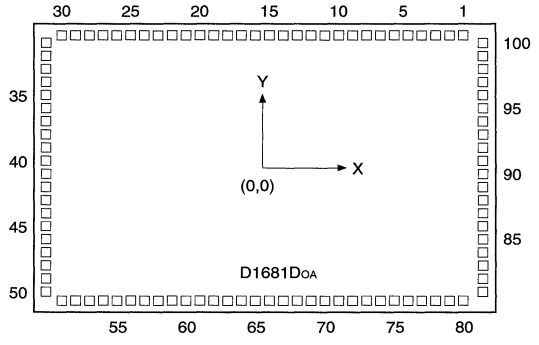


■ EXAMPLE OF APPLICATION

● SED1278



■ PAD LAYOUT



Chip Specification	Dimension (mm)
Chip size	5.59 × 3.50
Pad pitch	0.160 min.
Chip thickness	0.40 ±0.025
Pad size	0.10 × 0.10

● PAD COORDINATES

Unit = μm

Pad		X	Y	Pad		X	Y	Pad		X	Y
Number	Name	(μm)	(μm)	Number	Name	(μm)	(μm)	Number	Name	(μm)	(μm)
1	SEG29	–2461	–1588	35	V_2	2632	–881	69	SEG61	–560	1588
2	SEG28	–2261	–1588	36	V_{SS}	2632	–721	70	SEG60	–720	1588
3	SEG27	–2069	–1588	37	LP	2632	–561	71	SEG59	–880	1588
4	SEG26	–1885	–1588	38	NC	2632	–401	72	SEG58	–1040	1588
5	SEG25	–1709	–1588	39	SHL	2632	–241	73	SEG57	–1203	1588
6	SEG24	–1538	–1588	40	XSCL	2632	–81	74	SEG56	–1366	1588
7	SEG23	–1366	–1588	41	DI	2632	79	75	SEG55	–1538	1588
8	SEG22	–1203	–1588	42	DO	2632	239	76	SEG54	–1709	1588
9	SEG21	–1040	–1588	43	NC	2632	399	77	SEG53	–1885	1588
10	SEG20	–880	–1588	44	FR	2632	559	78	SEG52	–2069	1588
11	SEG19	–720	–1588	45	NC	2632	719	79	SEG51	–2261	1588
12	SEG18	–560	–1588	46	V_{DD}	2632	879	80	SEG50	–2461	1588
13	SEG17	–400	–1588	47	NC	2632	1039	81	SEG49	–2632	1546
14	SEG16	–240	–1588	48	NC	2632	1204	82	SEG48	–2632	1372
15	SEG15	–80	–1588	49	NC	2632	1372	83	SEG47	–2632	1204
16	SEG14	80	–1588	50	NC	2632	1546	84	SEG46	–2632	1039
17	SEG13	240	–1588	51	SEG79	2461	1588	85	SEG45	–2632	879
18	SEG12	400	–1588	52	SEG78	2261	1588	86	SEG44	–2632	719
19	SEG11	560	–1588	53	SEG77	2069	1588	87	SEG43	–2632	559
20	SEG10	720	–1588	54	SEG76	1885	1588	88	SEG42	–2632	399
21	SEG9	880	–1588	55	SEG75	1709	1588	89	SEG41	–2632	239
22	SEG8	1040	–1588	56	SEG74	1538	1588	90	SEG40	–2632	79
23	SEG7	1203	–1588	57	SEG73	1366	1588	91	SEG39	–2632	–81
24	SEG6	1366	–1588	58	SEG72	1203	1588	92	SEG38	–2632	–241
25	SEG5	1538	–1588	59	SEG71	1040	1588	93	SEG37	–2632	–401
26	SEG4	1709	–1588	60	SEG70	880	1588	94	SEG36	–2632	–561
27	SEG3	1885	–1588	61	SEG69	720	1588	95	SEG35	–2632	–721
28	SEG2	2069	–1588	62	SEG68	560	1588	96	SEG34	–2632	–881
29	SEG1	2261	–1588	63	SEG67	400	1588	97	SEG33	–2632	–1041
30	SEG0	2461	–1588	64	SEG66	240	1588	98	SEG32	–2632	–1206
31	NC	2632	–1548	65	SEG65	80	1588	99	SEG31	–2632	–1374
32	V_5	2632	–1374	66	SEG64	–80	1588	100	SEG30	–2632	–1548
33	V_0	2632	–1206	67	SEG63	–240	1588				
34	V_3	2632	–1040	68	SEG62	–400	1588				

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CMOS LCD DRIVER

● CMOS 80-Bit Segment Driver

■ DESCRIPTION

The SED1722/24 is an 80 dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of LCD drive voltages.

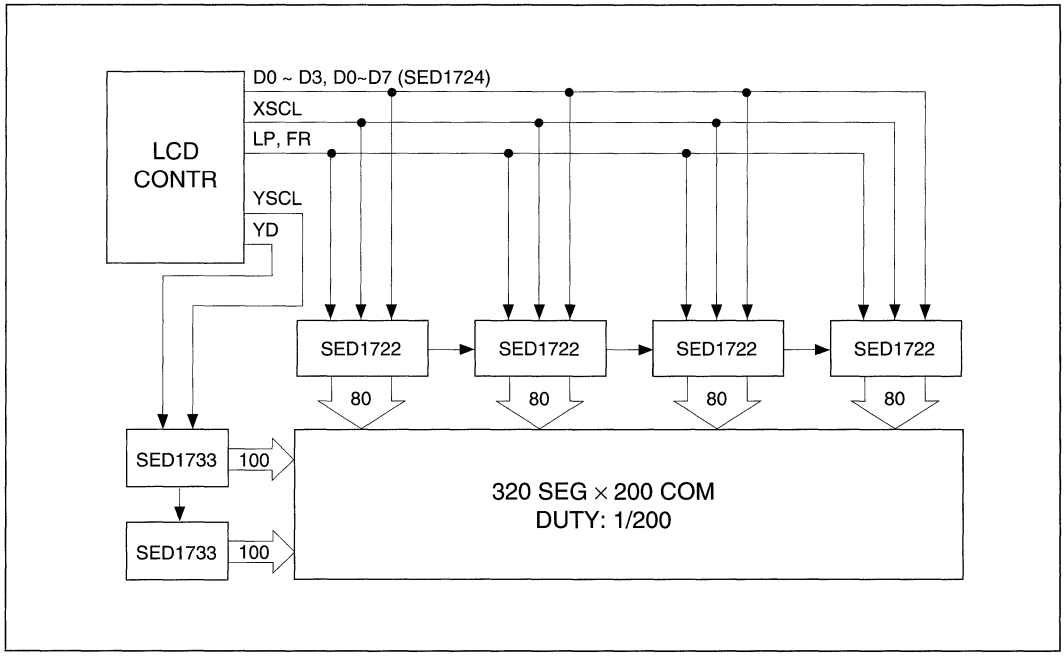
The device uses a high-speed daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1722/24 is used in conjunction with the SED1733F (100-bit output common driver) to drive a large-capacity dot matrix LCD panel.

■ FEATURES

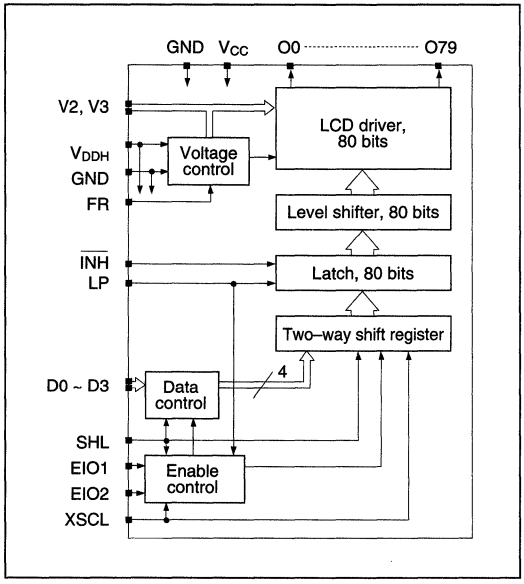
- Low-power high-speed CMOS technology
- 80-bit segment (column) driver
- High-speed data bus 4-bit (SED1722)
  8-bit (SED1724)
- Duty cycle ..... 1/100 to 1/500
- Shift clock frequency ..... 12 MHz
- Adjustable LCD drive voltages
- Selectable output shift direction
- Supports display blanking
- Low output resistance
- Ability to adjust offset bias of the LCD source from V_{DD}
- Low output impedance 1KΩ
- Wide range of LCD voltage .... 14 to 40V
- Supply voltage ..... 4.5 to 5.5V
- Package ..... QFP-5 100 pins (FOA)
  Al pad (DOA)

■ SYSTEM BLOCK DIAGRAM

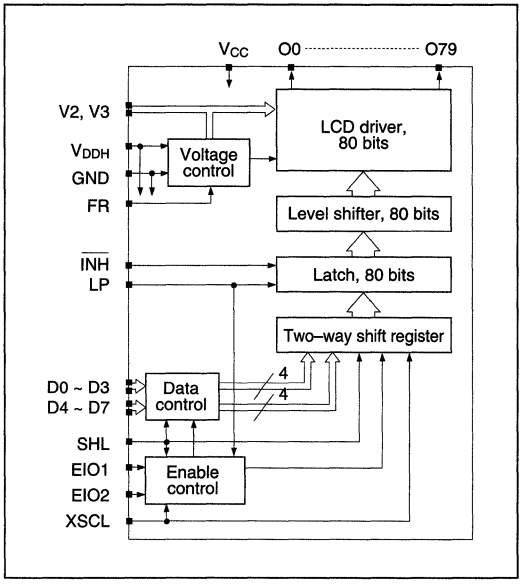


■ BLOCK DIAGRAM

● SED1722



● SED1724



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Q'ty</th></tr>
<tr><td>O0 to 79</td><td>O</td><td>To output the driving segment (column).
The output changes at the LP fall edge.</td><td>80</td></tr>
<tr><td>D0 to D3
(SED1722)</td><td>I</td><td>To input display data.
H: Selection data, L: Non-selection data</td><td>4</td></tr>
<tr><td>D0 to D7
(SED1724)</td><td>I</td><td>To input display data.
H: Selection data, L: Non-selection data</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>To input shift clock for display data (fall edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>To input latch pulse for display data (fall edge trigger)</td><td>1</td></tr>
<tr><td>EI01
EI02</td><td>I/O</td><td>Enable input and output:
Input or output is set on the SHL input level.
Output is reset by an input to LP and falls to "L" automatically when 80-bit data is completely fetched in.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>To select shift direction and to input input-output control data for the EIO terminal.
<In the case of SED1724>
When the data are input to (D0, D1,.. D7) terminals in the order of (a, b, .. g, h), (i,.. o, p) ... (s, t,.. y, z), relations between data and segment outputs come to be as per the following table:
<table>
<tr><th rowspan="2">SHL</th><th colspan="10">O (SEG Output)</th><th colspan="2">EIO</th></tr>
<tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>.....</th><th>77</th><th>78</th><th>79</th><th>1</th><th>2</th></tr>
<tr><td>H</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>.....</td><td>x</td><td>y</td><td>z</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>.....</td><td>c</td><td>b</td><td>a</td><td>Output</td><td>Input</td></tr>
</table>
Note: The relations between data and segment outputs are set irrespectively to number of shift locks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>To input AC signal for LCD driving output.</td><td>1</td></tr>
<tr><td>V_{CC}, GND</td><td>Power Supply</td><td>Logic power supply, GND: 0 V, V_{CC}: +5 V</td><td>2</td></tr>
<tr><td>V_{DDH}</td><td>Power Supply</td><td>Power supply for LCD driving circuit
V_{DDH}: +14 V to 40 V, (Liquid crystal driving selection level)</td><td>1</td></tr>
<tr><td>V2, V3</td><td>Power Supply</td><td>Power supply for driving liquid crystal
$V_{DDH} \geq V2 \geq 7/9\ V_{DDH}$, $2/9\ V_{DDH} \geq V3 \geq GND$</td><td>2</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Forced blank input
Output on the "L" level are forced to non-selection level.</td><td>1</td></tr>
</table>

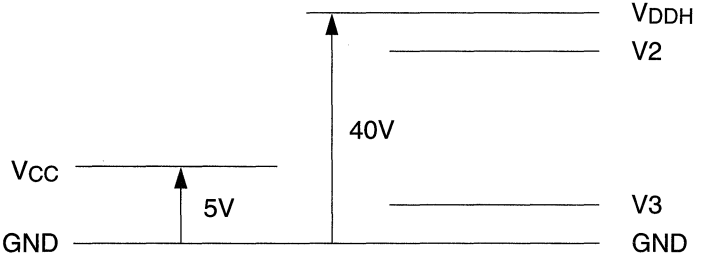
■ ELECTRICAL CHARACTERISITCS

● Absolute Maximum Ratings

(GND = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V2, V3	–0.3 to V_{DDH} +0.3	V
Input voltage	V_I	–0.3 to V_{CC} +0.3	V
Output voltage	V_O	–0.3 to V_{CC} +0.3	V
EIO output current	I_{O1}	20	mA
LCD circuit output current	I_{O2}	20	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–65 to +150	°C

Note 1. Let the V2 and V3 voltages maintain the condition, $V_{DDH} \geq V2 \geq V3 \geq GND$, all the time.



Note 2. If the logic circuit power supply comes to float power-supply voltage supply voltage is applied to the liquid crystal driving circuit, the LSI may be broken permanently. So, prevent the logic circuit power supply from floating. Pay special attention to the power supply sequence when the system is switched on or off.

● DC Electrical Characteristics

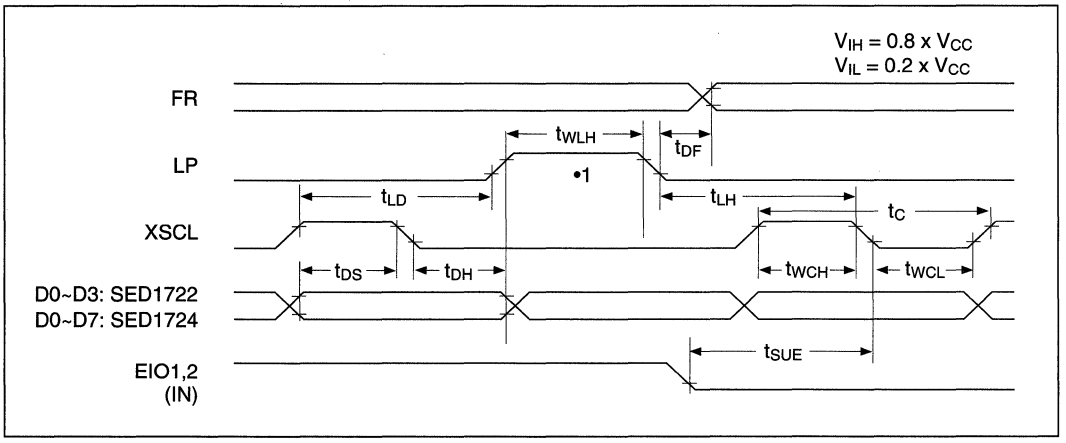
(Unless otherwise specified, GND=0V, V_{CC}= +5.0V±10%, T_a= –20 to 75°C)

Parameter	Symbol	Condition	Terminal	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}		V_{CC}	4.5	5.0	5.5	V
Recommended supply voltage	V_{DDH}		V_{DDH}	14.0	—	40.0	V
Operable voltage	V_{DDH}	Function	V_{DDH}	8.0	—	—	V
Supply voltage (2)	V2	Recommendation value	V2	7/9V_{DDH}	—	V_{DDH}	V
Supply voltage (3)	V3	Recommendation value	V3	GND	—	2/9V_{DDH}	V
High level input voltage	V_{IH}		EIO1, EIO2, D0 to D3: (SED1722) D0 to D7 (SED1724), XSCL, SHL, FR, LP, INH	0.8V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}			GND	—	0.2V_{CC}	V
High level output voltage	V_{OH}	I_{OH} = –0.6 mA	EIO1, EIO2	V_{CC} –0.4	—	V_{CC}	V
Low level output voltage	V_{OL}	I_{OL} = 0.6 mA		GND	—	0.4	V
Input leak current	I_{LI}	GND ≥ V_{IN} ≥ V_{CC}	D0 to D3: (SED1722) D0 to D7 (SED1724), SHL, XSCL, LP, FR, INH	—	—	2.0	µA
Input-output leak current	$I_{LI/O}$	GND ≥ V_{IN} ≥ V_{CC}	EIO1, EIO2	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 to 40.0 V V_{IH} = V_{CC}, V_{IL} = GND	GND	—	—	25	µA
Output resistance.	R_{SEG}	ΔVON = 0.5V, V_{DDH}=+30.0V	*1 O0 to O79	—	0.7	1.8	kΩ
		ΔVON = 0.5V, V_{DDH}=+20.0V		—	0.8	2.2	
		ΔVON = 0.5V, V_{DDH}=+14.0V		—	1.0	2.6	
Current consumed (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} =5.38 MHz, f_{LP} =33.6 kHz, f_{FR} =70 Hz; Input data: To be inverted 1 bit/1H. No load	V_{CC}	—	0.5	1.5	mA
Current consumed (2)	I_{DDH}	V_{CC} = +5.0 V, V3 = +4.0 V, V2 = +26.0 V, V_{DDH} =+30.0V Other conditions are same as those of I_{CC}	V_{DDH}	—	0.2	1.5	mA
Input terminal capacity	C_I	Freq.=1 MHz, T_a = 25°C	D0 to D3: (SED1722) D0 to D7 (SED1724), SHL, XSCL, LP, FR, INH	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

*1. The output resistance is specified within the ranges of the supply voltages (2) and (3).

● **AC Electrical Characteristics**

○ **Input Timing Characteristics**

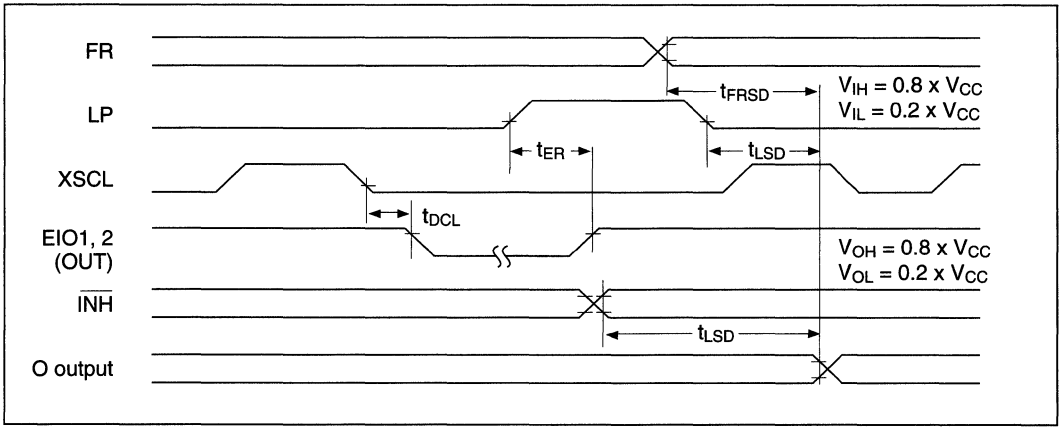


(VCC = 5.0 V ±10%, Ta = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
XSCL cycle	tC		83	—	—	ns
XSCL high level pulse width	tWCH		30	—	—	ns
XSCL low level pulse width	tWCL		30	—	—	ns
Data setup time	tDS		30	—	—	ns
Data hold time	tDH		20	—	—	ns
XSCL to LP rise time	tLD		0	—	—	ns
LP to XSCL fall time	tLH		200	—	—	ns
LP high level pulse width	tWLH	see note	70	—	—	ns
FR delay allowable time	tDF		–300	—	300	ns
EIO setup time	tSUE		36	—	—	ns

Note: tWLH is the time when LP is "H" and XSCL is "L"

o Output Timing Characteristics

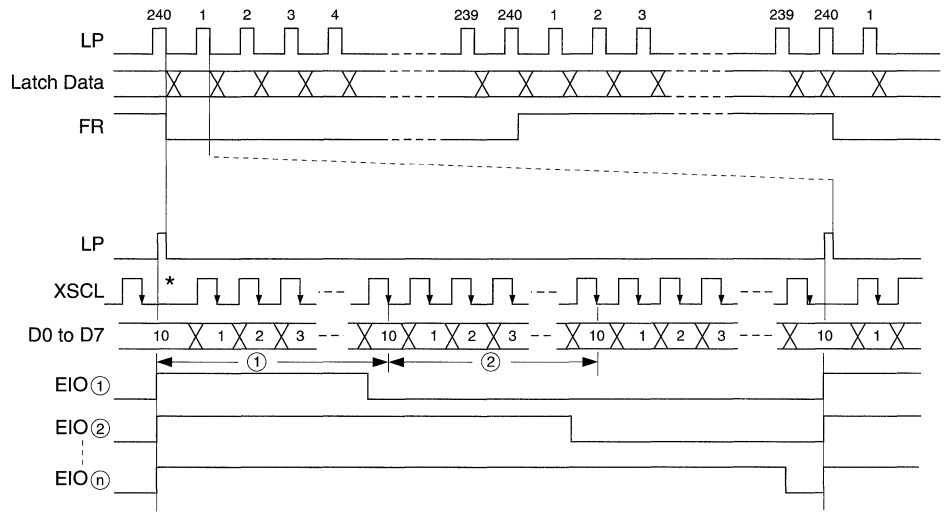


(VCC = +5.0 V ±10%, VDDH = 14.0 to 40.0 V, Ta = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
EIO reset time	t_{ER}	C_L = 15 pF	—	—	120	ns
EIO output delay time	t_{DCL}		—	—	45	ns
LP to output delay time	t_{LSD}	C_L = 100 pF	—	—	0.5	µs
FR to output delay time	t_{FRSD}		—	—	0.7	µs
$\overline{INH}$ to output delay time	t_{pdINH}		—	—	0.5	µs

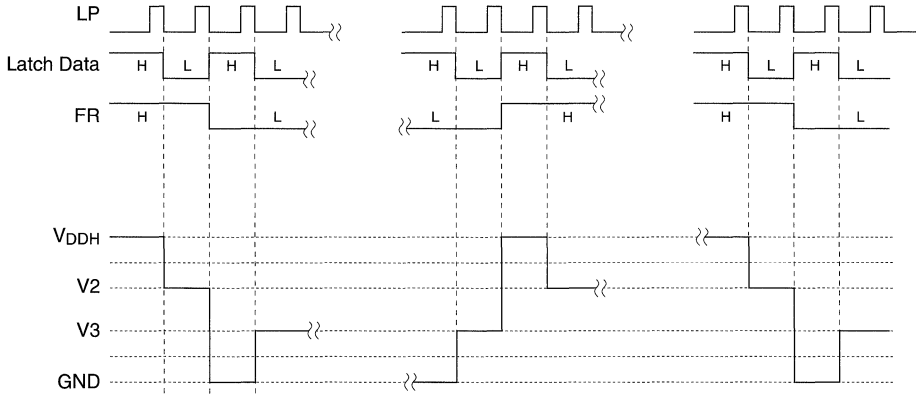
■ Timing Diagram

When it is 1/240 duty (example for reference)



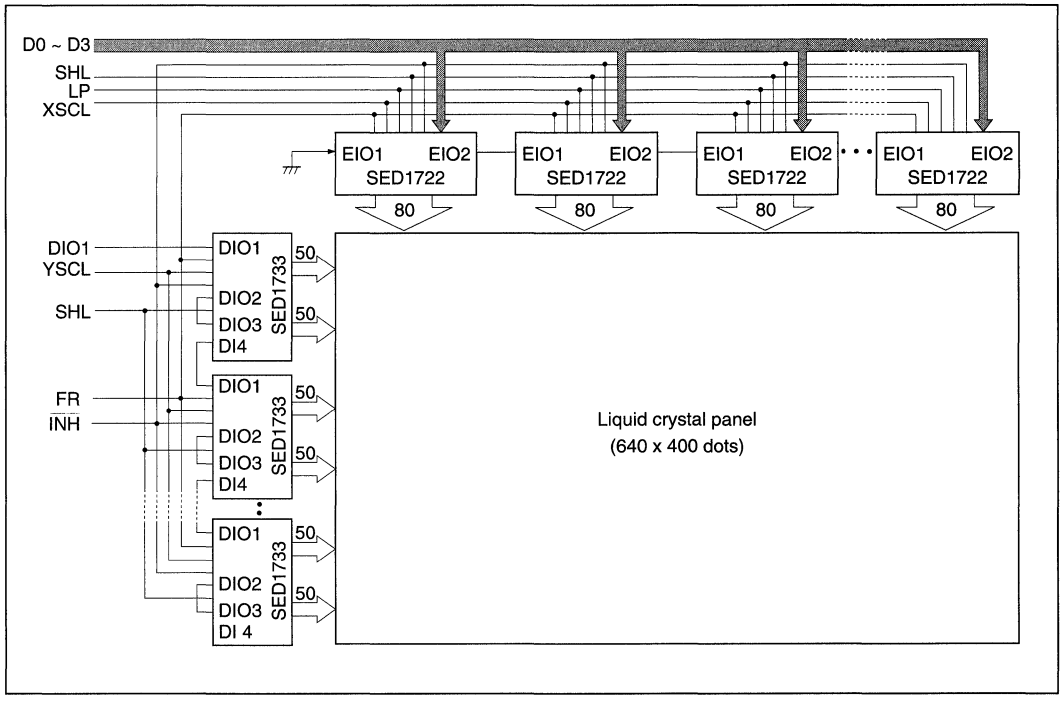
① to ⓝ are the driver's cascade numbers.

* In high-speed data transmission, the XSCL period may need to be longer in the LP pulse insertion timing, so as to secure the LP → XSCL (t_{LH}) standard.

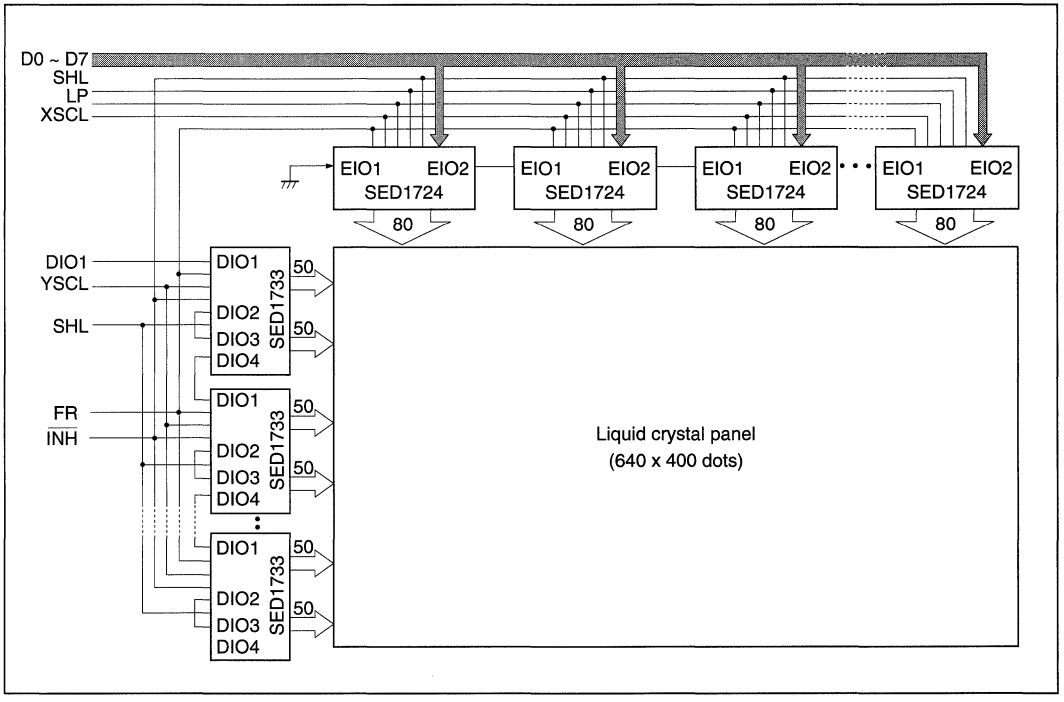


■ EXAMPLE OF REFERENCE CIRCUIT

(Combination of SED1722 with SED1733)

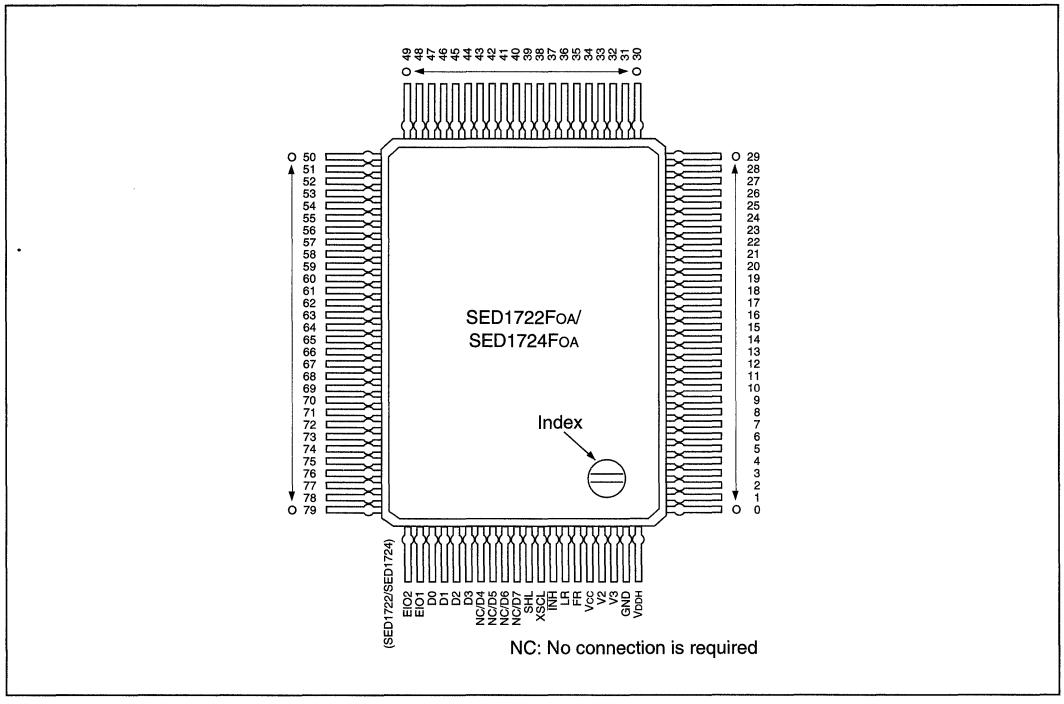


(Combination of SED1724 with SED1733)

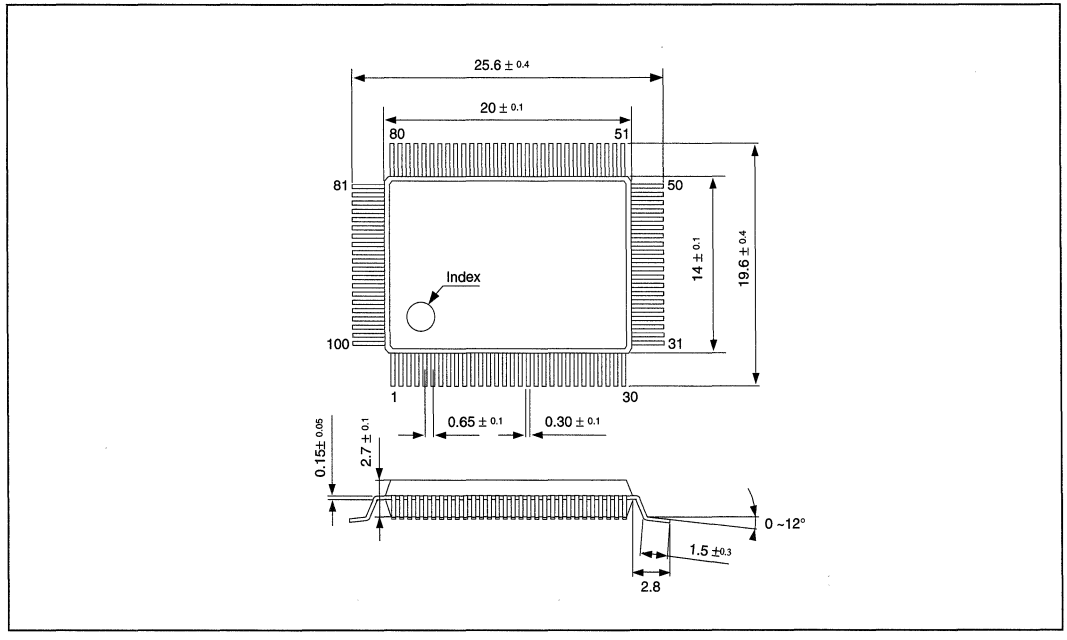


■ PACKAGE DIMENSIONS

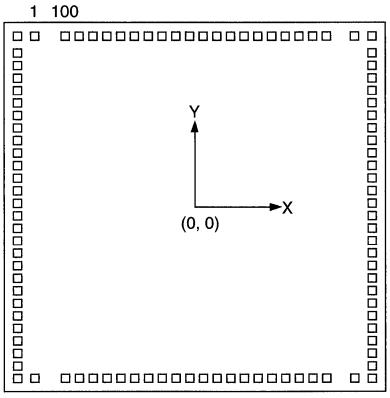
● SED1722F0A, SED1724F0A



● Plastic QFP5-100 pin



■ PAD LAYOUT (SED1722D0A, SED1724D0A)



Chip Dimensions	5.81 mm × 5.20 mm
Pad pitch	0.160 mm (Min.)
Chip thickness	0.400 ±0.025 mm
Aluminum pad opening	100 μm × 100 μm (all terminals)

■ PAD COORDINATES

Pad		X	Y
Number	Name	(μm)	(μm)
1	O 50	–2488	2432
2	O 51	–2488	2432
3	O 52	–2738	2222
4	O 53	–2738	2022
5	O 54	–2738	1835
6	O 55	–2738	1660
7	O 56	–2738	1485
8	O 57	–2738	1310
9	O 58	–2738	1135
10	O 59	–2738	960
11	O 60	–2738	785
12	O 61	–2738	610
13	O 62	–2738	435
14	O 63	–2738	260
15	O 64	–2738	85
16	O 65	–2738	–85
17	O 66	–2738	–260
18	O 67	–2738	–435
19	O 68	–2738	–610
20	O 69	–2738	–785
21	O 70	–2738	–960
22	O 71	–2738	–1135
23	O 72	–2738	–1310
24	O 73	–2738	–1485
25	O 74	–2738	–1660
26	O 75	–2738	–1835
27	O 76	–2738	–2022
28	O 77	–2738	–2222
29	O 78	–2738	–2432
30	O 79	–2488	–2432
31	EIO2	–2000	–2432
32	EIO1	–1750	–2432
33	D0	–1500	–2432
34	D1	–1300	–2432

Pad		X	Y
Number	Name	(μm)	(μm)
35	D2	–1100	–2432
36	D3	–900	–2432
37	NC/D4	–700	–2432
38	NC/D5	–500	–2432
39	NC/D6	–300	–2432
40	NC/D7	–100	–2432
41	SHL	100	–2432
42	XSCL	300	–2432
43	$\overline{INH}$	500	–2432
44	LP	700	–2432
45	FR	900	–2432
46	VCC	1100	–2432
47	V2	1300	–2432
48	V3	1500	–2432
49	GND	1750	–2432
50	VDDH	2000	–2432
51	O 0	2488	–2432
52	O 1	2738	–2432
53	O 2	2738	–2222
54	O 3	2738	–2022
55	O 4	2738	–1835
56	O 5	2738	–1660
57	O 6	2738	–1485
58	O 7	2738	–1310
59	O 8	2738	–1135
60	O 9	2738	–960
61	O 10	2738	–785
62	O 11	2738	–610
63	O 12	2738	–435
64	O 13	2738	–260
65	O 14	2738	–85
66	O 15	2738	85
67	O 16	2738	260
68	O 17	2738	435

Pad		X	Y
Number	Name	(μm)	(μm)
69	O 18	2738	610
70	O 19	2738	785
71	O 20	2738	960
72	O 21	2738	1135
73	O 22	2738	1310
74	O 23	2738	1485
75	O 24	2738	1660
76	O 25	2738	1835
77	O 26	2738	2022
78	O 27	2738	2222
79	O 28	2738	2432
80	O 29	2488	2432
81	O 30	2000	2432
82	O 31	1750	2432
83	O 32	1500	2432
84	O 33	1300	2432
85	O 34	1100	2432
86	O 35	900	2432
87	O 36	700	2432
88	O 37	500	2432
89	O 38	300	2432
90	O 39	100	2432
91	O 40	–100	2432
92	O 41	–300	2432
93	O 42	–500	2432
94	O 43	–700	2432
95	O 44	–900	2432
96	O 45	–1100	2432
97	O 46	–1300	2432
98	O 47	–1500	2432
99	O 48	–1750	2432
100	O 49	–2000	2432

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- **CMOS 160-bit Segment Driver**
- **High Voltage LCD Driver**

■ DESCRIPTION

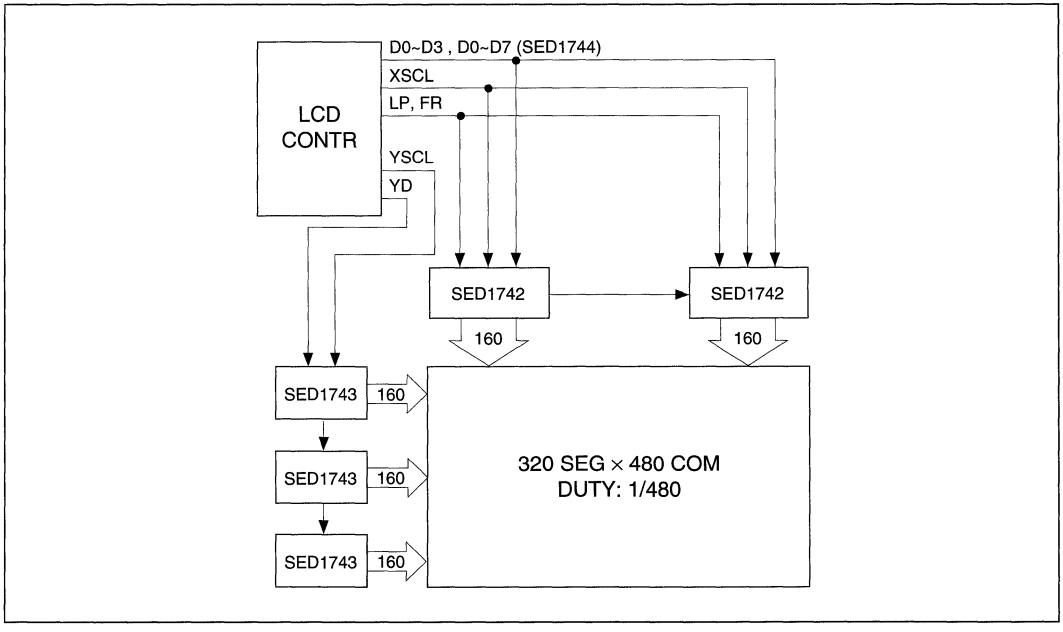
The SED1742/SED1744 is a 160 dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of LCD voltages. The upper and lower LCD drive voltages (V0, V5) are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. The device uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1742/44 is used in conjunction with the SED1743 (160-bit common driver) to drive a large-capacity dot matrix LCD panel.

■ FEATURES

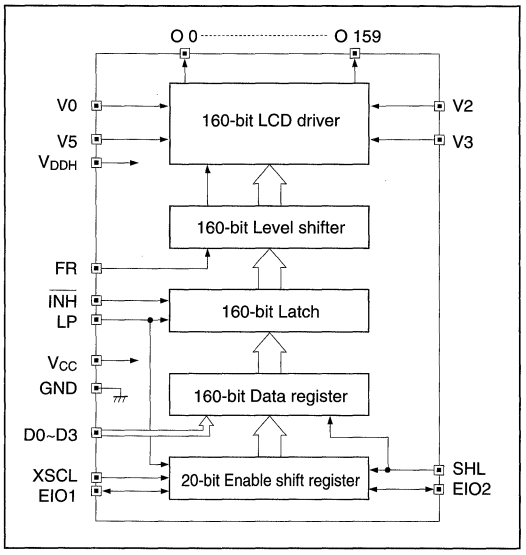
- Low-power high-speed CMOS technology
- 160-bit segment (column) driver
- High-speed data bus 4-bit (SED1742)
  8-bit (SED1744)
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Unbiased display off function
- Adjustable offset bias of the LCD according to VDDH and GND
- Shift clock frequency .... 12MHz max at V_{DD} = 5V
- Ability to adjust offset bias of the LCD source from V_{DD}
- Daisy chain enable support
- No enable signal by controller is required
- Wide range of LCD voltage .... 14 to 40V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... TAB (T_{OA})
  Au bump (D_{1B})

■ SYSTEM BLOCK DIAGRAM

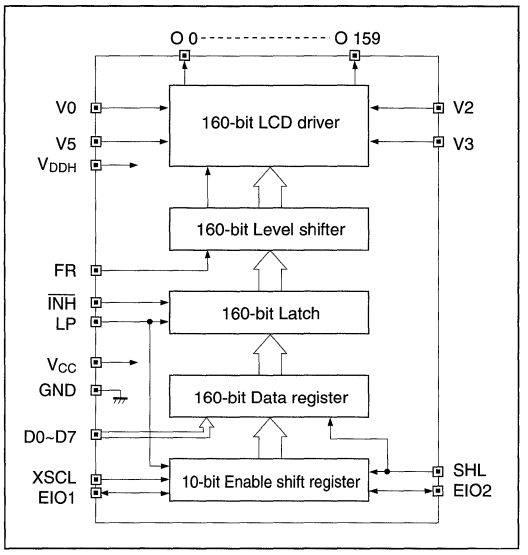


■ BLOCK DIAGRAM

● SED1742



● SED1744



■ PIN DESCRIPTION

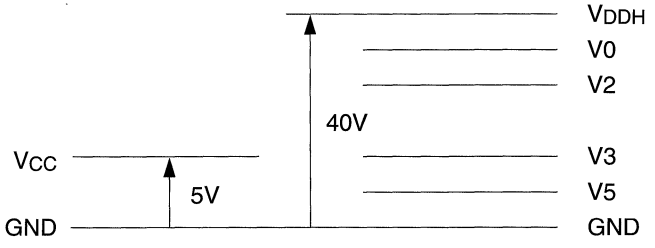
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Q'ty</th></tr>
<tr><td>O0 to 159</td><td>—</td><td>LCD crystal segment (column) output
The output varies at the LP trailing edge.</td><td>160</td></tr>
<tr><td>D0 to D3
(SED1742)</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>D0 TO D7
(SED1744)</td><td>I</td><td>Display data input</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (triggered at the trailing edge)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (triggered at the trailing edge)</td><td>1</td></tr>
<tr><td>EI01, EI02</td><td>I/O</td><td>Enable I/O. Set to input or output according to SHL input level.
The output is reset at the LP input and set to "L" when a 160-bit data fetch is complete.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO terminal I/O control input (SED1744)
When the data (a, b, .. g, h) (i, .. o, p) ... (s, t, .. y, z) are input in this sequence to the terminals (D0, D1, .. D7), the relation between the data and the segment output is as shown in the table below.
<table>
<tr><td rowspan="2">SHL</td><td colspan="10">O (SEG Output)</td><td colspan="2">EIO</td></tr>
<tr><td>159</td><td>158</td><td>157</td><td>156</td><td>155</td><td>.....</td><td>2</td><td>1</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>.....</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>.....</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table>
Note: The relation between the data and the segment output is determined independently of the number of shift locks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Input of signal to AC electrify the liquid crystal drive output</td><td>1</td></tr>
<tr><td>V_{CC}, GND</td><td>Power Source</td><td>Logic power source. GND: 0 V; V_{CC}: +3, +5 V</td><td>2</td></tr>
<tr><td>V0, V2, V3, V5
V_{DDH}</td><td>Power Source</td><td>Liquid crystal drive power source V_{DDH}: +14 V to 40 V; GND: 0 V
$V_{DDH} \geq V0 > V2 \geq 7/9\ V_{DDH}$, $2/9\ V_{DDH} \geq V3 > V5 \geq GND$</td><td>5</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Forced blank input
The signal forces the output to be set to V5 level at the "L" level.</td><td>1</td></tr>
<tr><td>TEST</td><td></td><td>Test input normally fixed at "L" level.</td><td>1</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage for LCD (1)	V_{DDH}	–0.3 to +45.0	V
Supply voltage for LCD (2)	V0, V2, V3, V5	GND –0.3 to VDDH +0.3	V
Input voltage (4)	V_I	GND –0.3 to VCC +0.3	V
Output voltage	V_O	GND –0.3 to VCC +0.3	V
EIO output current	IO1	20	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature 1 (3)	T_{stg1}	–65 to +150	°C
Storage temperature 2 (3)	T_{stg2}	–55 to +150	°C
Logic supply	V_{CC}	3*	V
Segment driver supply voltage range	V_{DDH}	14 to 28*	V

* T_a = 25°C



Notes: 1. The voltage is based at GND = 0 V
2. Voltage V0, V2, V3 and V5 should satisfy the condition: $V_{DDH} \geq V0 \geq V2 \geq V3 \geq V5 \geq GND$.
3. The storage temperature 1 is specified for a single chip and the storage temperature 2 is for TCP mounting.
4. WARNING: The LSI may be externally broken if the logic system power source floats or decreases below V_{CC} = 2.9 V while voltage is applied to the liquid crystal drive system power source. Special care should be taken for the power source sequence when turning the system power on and off.

● DC Electrical Characteristics

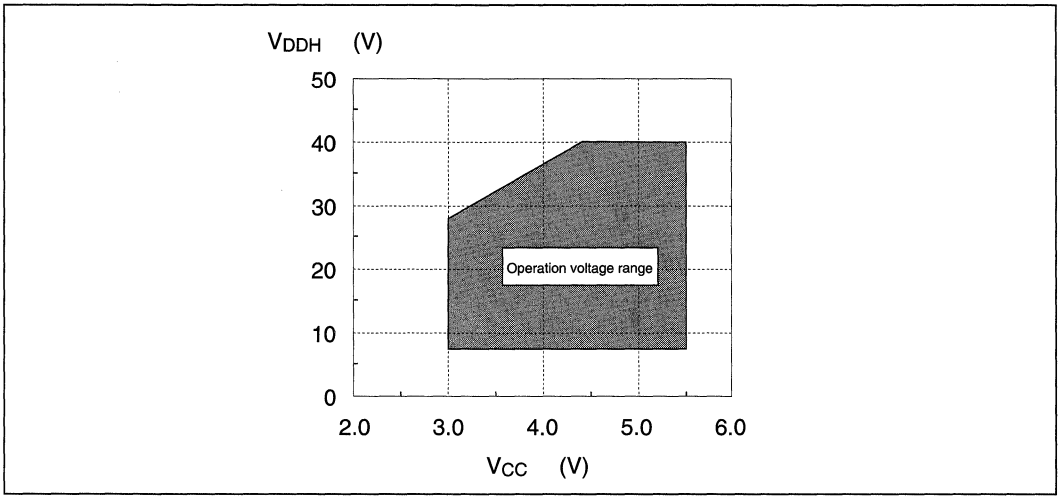
(Unless stated otherwise GND=V5=0V, V_{CC}= +5.0V±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Terminal	Min	Typ	Max	Unit
Logic supply voltage (1)	V_{CC}		V_{CC}	3.0	5.0	5.5	V
Operation voltage recommended	V_{DDH}		V_{DDH}	14.0	—	40.0	V
Segment driver input supply voltage	V_{DDH}	Function	V_{DDH}	8.0	—	—	V
Segment driver input supply voltage (2)	V0	Value recommended	V0	V_{DDH} –2.5	—	V_{DDH}	V
Segment driver input supply voltage (2)	V2	Value recommended	V2	7/9V_{DDH}	—	—	V
Segment driver input supply voltage (2)	V3, V5	Value recommended	V3, V5	GND	—	2/9V_{DDH}	V
High-level input voltage	V_{IH}	V_{CC} = 3.0 to 5.5 V	EIO1, EIO2, D0 to D3: SED1742 D0 to D7: SED1744 XSCL, LP, SHL, FR, $\overline{INH}$	0.8V_{CC}	—	—	V
Low-level input voltage	V_{IL}			—	—	0.2V_{CC}	V
High-level output voltage	V_{OH}	V_{CC} = 3 to 5.5 V, I_{OH} = –0.6 mA	EIO1, EIO2	V_{CC} –0.4	—	—	V
Low-level output voltage	V_{OL}	V_{CC} = 3 to 5.5 V, I_{OL} = 0.6 mA		—	—	0.4	V
Low-level input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	D0 to D3: SED1742 D0 to D7: SED1744 LP, FR, XSCL, SHL, $\overline{INH}$	—	—	2.0	µA
Input: leakage current output	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}	EIO1, EIO2	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 to 40.0 V, V_{IH} = V_{CC}, V_{IL} = GND	GND	—	—	25	µA
Output resistance	R_{SEG}	ΔVON = 0.5V condition recommended, V_{DDH}=+30.0V	O0 to O159	—	0.9	2.5	kΩ
		ΔVON = 0.5V condition recommended, V_{DDH}=+20.0V		—	1.0	3.0	kΩ
Average Operation current consumed (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} =5.38 MHz, f_{LP} =33.6 kHz, f_{FR} =70 Hz, Input data: Display checkered, No load	V_{CC}	—	0.4	1.2	mA
		V_{CC} = +3.0 V; Other conditions: same as V_{CC} = +5.0 V		—	0.2	0.6	mA
Average Operation current consumed (2)	I_{DDH}	V_{DDH} = V0 = +30.0 V, V_{CC} = +5.0 V, V3 = +4.0 V, V2 = +26.0 V, V5 = 0.0 V; Other conditions: same as V_{CC} = +5.0 V	V_{DDH}	—	0.5	1.5	mA
Input capacitance	C_I	Freq.=1 MHz, T_a = 25°C Single chip	D0 to D3: SED1742 D0 to D7: SED1744 LP, FR, XSCL, SHL, $\overline{INH}$	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

Notes: 1. The voltage is based at GND=0V.
2. Voltage V_0, V_2, and V_3 should satisfy the condition: V_{DDH}>V_0>V_2>V_3>V_5>GND

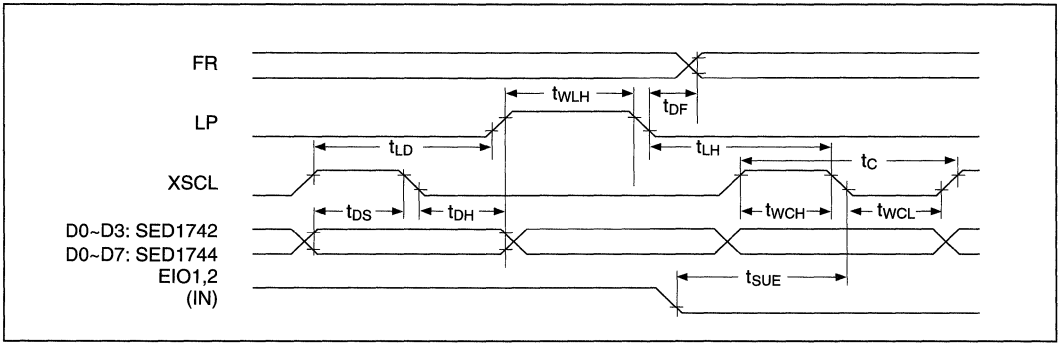
● **Operating Voltage Range V_{CC}–V_{DDH}**

The maximum LCD supply voltage, V_{DDH} depends on V_{CC} as shown in the following figure. Specify the V_{DDH} voltage within the V_{CC}–V_{DDH} operation.



● **AC Electrical Characteristics**

○ **Input Timing Characteristics**



Note: Adjust the timing of the LP pulse input at high-speed operation, excluding one clock of XSCL.

(V_{CC} = 5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
XSCL cycle	t_C		83	—	—	ns
XSCL high-level pulse width	t_{WCH}		30	—	—	ns
XSCL low-level pulse width	t_{WCL}		30	—	—	ns
Data setup time	t_{DS}		30	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
XSCL → LP rise time	t_{LD}		–5	—	—	ns
LP → XSCL breaking time	t_{LH}		60	—	—	ns
LP high-level pulse width (1)	t_{WLH}		45	—	—	ns
FR delay allowance time	t_{DF}		–300	—	300	ns
EIO setup time	t_{SUE}		35	—	—	ns

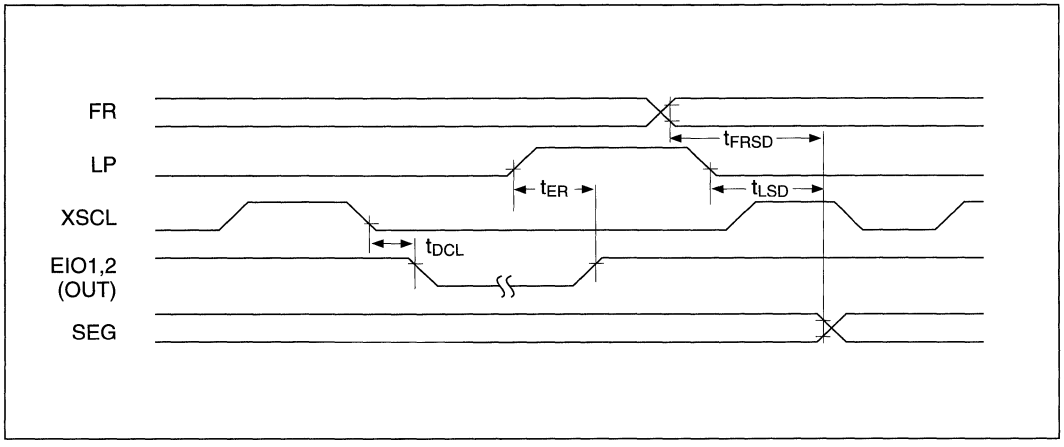
Note: t_{WLH} defines the time duration when the LP is "H" and the XSCL is "L".

(V_{CC} = 3.0 to 4.5 V, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
XSCL cycle	t_C		125	—	—	ns
XSCL high-level pulse width	t_{WCH}		50	—	—	ns
XSCL low-level pulse width	t_{WCL}		50	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
XSCL → LP rise time	t_{LD}		0	—	—	ns
LP → XSCL breaking time	t_{LH}		120	—	—	ns
LP high-level pulse width (1)	t_{WLH}		90	—	—	ns
FR delay allowance time	t_{DF}		–600	—	600	ns
EIO setup time	t_{SUE}		70	—	—	ns

Note: t_{WLH} defines the time duration when the LP is "H" and the XSCL is "L"

○ Output Timing Characteristics



(V_{CC} = +5.0 V ±10%, V_{DDH} = 14.0 to 40.0 V)

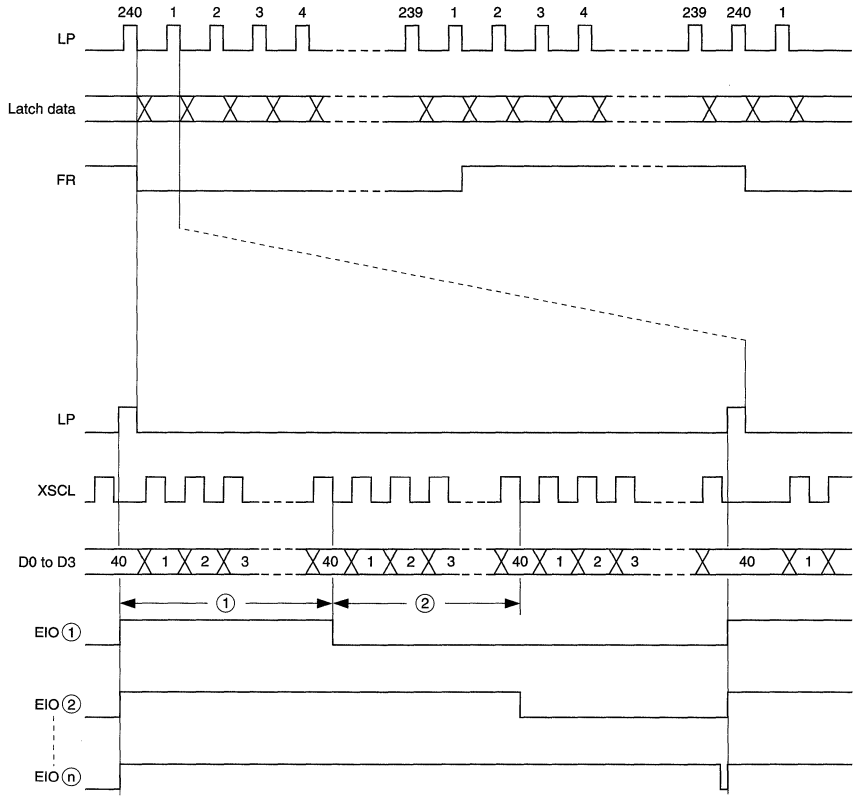
Parameter	Symbol	Condition	Min	Typ	Max	Unit
EIO reset time	t_{ER}	C_L = 15 pF (EIO)	—	—	120	ns
EIO output delay time	t_{DCL}		—	—	45	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (On)	—	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	—	400	ns

(V_{CC} = 3.0 to 4.5 V, V_{DDH} = 14.0 to 28.0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
EIO reset time	t_{ER}	C_L = 15 pF (EIO)	—	—	240	ns
EIO output delay time	t_{DCL}		—	—	72	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (On)	—	—	400	ns
FR → SEG output delay time	t_{FRSD}		—	—	800	ns

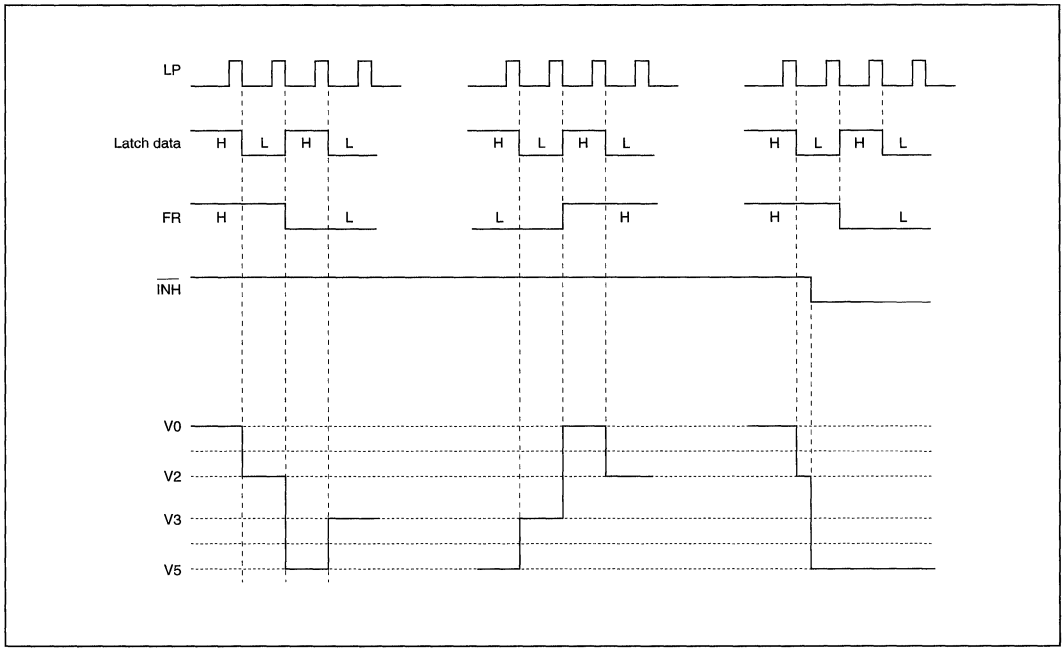
● Timing Diagrams

○ 1/240 Duty Cycle



Notes:

1. The circled numerals 1 to n denote the position of the device in the chain.
2. One cycle of XSCL should be lengthened tio satisfy t_{LH} when high-speed data transfer takes place.



■ FUNCTIONAL DESCRIPTION

● Enable Shift Register

The enable shift register is a bi-directional shift register, where the shift direction is selected by SHL. SHL is also used to latch data from the data bus into the data register. The effect of SHL on the shift direction and on the input data sequence is shown in the following table.

Data Sequence and Shift Direction

SHL	LCD Outputs							Shift Direction	
	O159	O158	O157	...	O2	O1	O0	EIO1	EIO2
L	a	b	c	...	x	y	z	Output	Input
H	z	y	x	...	c	b	a	Input	Output

When the enable signal is inactive, the SED1742 is in standby mode with the internal clock stopped and the data bus held LOW. When multiple SED1742s are used, the enable input of the first device should be connected to ground and the enable input of each successive device should be connected to the enable output of the preceding device.

When 160 data bits have been latched into the SED1742, the enable output edge goes LOW, eliminating the need for an external control circuit.

● Data Register

The data register converts the input data into parallel display driver data under the control of the enable shift register.

■ APPLICATION NOTES

● Voltage Levels

The recommended method of generating the LCD drive voltages, V0 to V5, is with a voltage divider between V_{DDH} and V_{GND}, buffered with voltage followers.

The lower drive level, V5, is not necessarily at V_{GND}, and separate pins are used for the voltage levels when op-amps are used. A maximum voltage differential between V5 and V_{GND} of 2.5V is recommended since the driver efficiency decreases as the differential increases. Connect V5 to GND when not using op-amps.

The resistances of the voltage divider resistors should be as low as possible and within power supply constraints.

Note that fluctuations in I_{DDH} can cause dips in the V_{DDH} supply. The device will be damaged if the voltage dips below the point where the relationship V_{DDH} (V0) ≥ V2 ≥ V3 ≥ V5 ≥ V_{GND} breaks down. A stabilized power supply may be required when using the resistor network.

● Data Latch

The data latch latches the data into the level shifter on the falling edge of LP.

● Level Shifter

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

● LCD Drivers

The LCD drivers generate the AC LCD drive waveforms. The output voltages are determined by the polarity of the FR signal, as shown in the following table.

Driver Output Voltage

$\overline{INH}$	Input Data	FR	Output Voltage
H	H	H	V0 (V_{DDH})
		L	V5
	L	H	V2
		L	V3
L	X	X	V5

x = don't care

- **Power-Up and Power-Down Precautions**

As the driver circuitry operates at high voltage, care should be taken when applying and removing power to the SED1742 to prevent damage. If the driver supply is applied when the logic supply is either not connected or below 2.9V, excess current will flow into the SED1742 and damage the device. Normal operation is guaranteed if the correct power-up and power-down sequences are followed.

Power-Up Sequence:

Power should be applied to Vcc before, or at the same time as, power is applied to the driver circuitry.

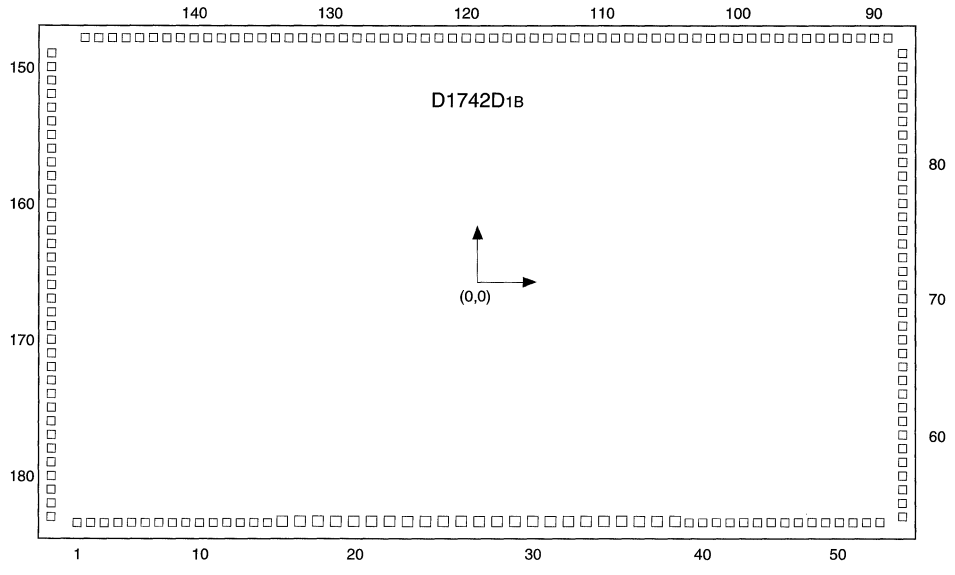
Power-Down Sequence:

Power should be removed from Vcc after, or at the same time as, power is removed from the driver circuitry.

The SED1742 can also be damaged if the LCD output drivers start operating before the driver supplies stabilize. INH should be held LOW to hold the driver outputs at V5 until the driver supplies have stabilized.

As an extra precaution, insert a fast-blow fuse in series with the driver supply.

■ PAD LAYOUT FOR SED1742D1B



Chip Size ..... 7.30mm × 4.48mm
Chip Thickness ..... 525μm ± 25μm
Pad Pitch ..... 108μm (Min.)
Gold bump dimensions (SED1742D1B):
Size A ..... 94 × 134 ± 20μm (pads 1~15, 39~183)
Size B ..... 115 × 148 ± 20μm (pads 16~33, 38)
Size C ..... 115 × 134 ± 20μm (pads 34~37)

unit: μm

■ PAD COORDINATES

Pad		Coordinates	
No.	Name	X	Y
1	O145	–3228	–2064
2	O146	–3120	–2064
3	O147	–3012	–2064
4	O148	–2903	–2064
5	O149	–2795	–2064
6	O150	–2687	–2064
7	O151	–2578	–2064
8	O152	–2470	–2064
9	O153	–2362	–2064
10	O154	–2253	–2064
11	O155	–2145	–2064
12	O156	–2037	–2064

Pad		Coordinates	
No.	Name	X	Y
13	O157	–1929	–2064
14	O158	–1820	–2064
15	O159	–1712	–2064
16	EIO2	–1550	–2058
17	EIO1	–1417	–2058
18	GND	–1284	–2058
19	D0	–1151	–2058
20	D1	–1018	–2058
21	D2	–885	–2058
22	D3	–752	–2058
23	NC	–619	–2058
24	NC	–486	–2058

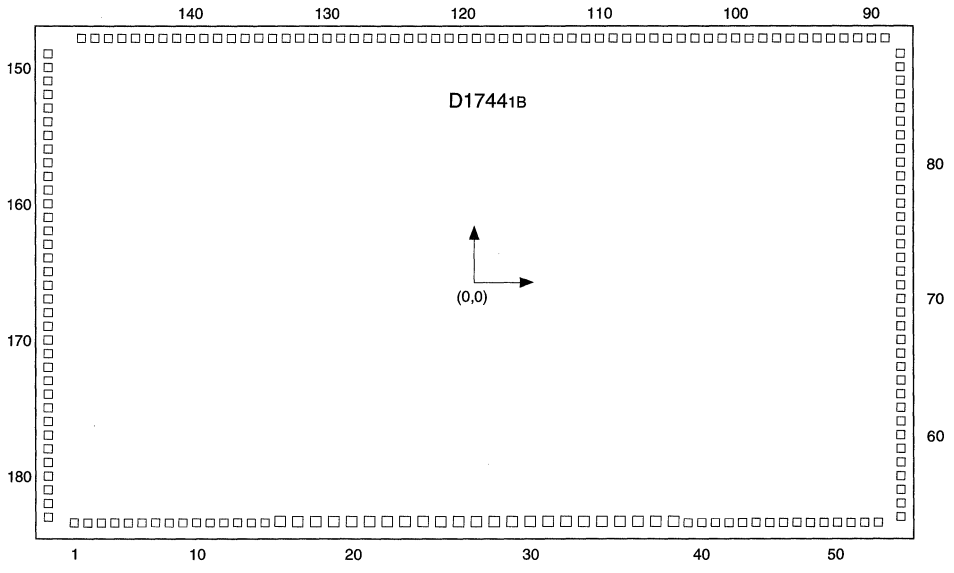
Pad		Coordinates	
No.	Name	X	Y
25	NC	–353	–2058
26	NC	–220	–2058
27	SHL	–87	–2058
28	XSCL	46	–2058
29	TEST	179	–2058
30	$\overline{INH}$	312	–2058
31	LP	445	–2058
32	V_{CC}	578	–2058
33	FR	711	–2058
34	V5	872	–2026
35	V3	1034	–2026
36	V2	1195	–2026

Pad		Coordinates	
No.	Name	X	Y
37	V0	1357	–2026
38	VDDH	1550	–2058
39	O0	1712	–2064
40	O1	1820	–2064
41	O2	1929	–2064
42	O3	2037	–2064
43	O4	2145	–2064
44	O5	2253	–2064
45	O6	2362	–2064
46	O7	2470	–2064
47	O8	2578	–2064
48	O9	2687	–2064
49	O10	2795	–2064
50	O11	2903	–2064
51	O12	3012	–2064
52	O13	3120	–2064
53	O14	3228	–2064
54	O15	3474	–1841
55	O16	3474	–1733
56	O17	3474	–1625
57	O18	3474	–1516
58	O19	3474	–1408
59	O20	3474	–1300
60	O21	3474	–1191
61	O22	3474	–1083
62	O23	3474	–975
63	O24	3474	–866
64	O25	3474	–758
65	O26	3474	–650
66	O27	3474	–542
67	O28	3474	–433
68	O29	3474	–325
69	O30	3474	–217
70	O31	3474	–108
71	O32	3474	0
72	O33	3474	108
73	O34	3474	217
74	O35	3474	325
75	O36	3474	433
76	O37	3474	542
77	O38	3474	650
78	O39	3474	758
79	O40	3474	866
80	O41	3474	975
81	O42	3474	1083
82	O43	3474	1191
83	O44	3474	1300
84	O45	3474	1408
85	O46	3474	1516

Pad		Coordinates	
No.	Name	X	Y
86	O47	3474	1625
87	O48	3474	1733
88	O49	3474	1841
89	O50	3195	2064
90	O51	3087	2064
91	O52	2978	2064
92	O53	2870	2064
93	O54	2762	2064
94	O55	2553	2064
95	O56	2545	2064
96	O57	2437	2064
97	O58	2328	2064
98	O59	2220	2064
99	O60	2112	2064
100	O61	2004	2064
101	O62	1895	2064
102	O63	1787	2064
103	O64	1679	2064
104	O65	1570	2064
105	O66	1462	2064
106	O67	1354	2064
107	O68	1245	2064
108	O69	1137	2064
109	O70	1029	2064
110	O71	921	2064
111	O72	812	2064
112	O73	704	2064
113	O74	596	2064
114	O75	487	2064
115	O76	379	2064
116	O77	271	2064
117	O78	162	2064
118	O79	54	2064
119	O80	–54	2064
120	O81	–162	2064
121	O82	–271	2064
122	O83	–379	2064
123	O84	–487	2064
124	O85	–596	2064
125	O86	–704	2064
126	O87	–812	2064
127	O88	–921	2064
128	O89	–1029	2064
129	O90	–1137	2064
130	O91	–1245	2064
131	O92	–1354	2064
132	O93	–1462	2064
133	O94	–1570	2064
134	O95	–1679	2064

Pad		Coordinates	
No.	Name	X	Y
135	O96	–1787	2064
136	O97	–1895	2064
137	O98	–2004	2064
138	O99	–2112	2064
139	O100	–2220	2064
140	O101	–2328	2064
141	O102	–2437	2064
142	O103	–2545	2064
143	O104	–2653	2064
144	O105	–2762	2064
145	O106	–2870	2064
146	O107	–2978	2064
147	O108	–3087	2064
148	O109	–3195	2064
149	O110	–3474	1841
150	O111	–3474	1733
151	O112	–3474	1625
152	O113	–3474	1516
153	O114	–3474	1408
154	O115	–3474	1300
155	O116	–3474	1191
156	O117	–3474	1083
157	O118	–3474	975
158	O119	–3474	866
159	O120	–3474	758
160	O121	–3474	650
161	O122	–3474	542
162	O123	–3474	433
163	O124	–3474	325
164	O125	–3474	217
165	O126	–3474	108
166	O127	–3474	0
167	O128	–3474	–108
168	O129	–3474	–217
169	O130	–3474	–325
170	O131	–3474	–433
171	O132	–3474	–542
172	O133	–3474	–650
173	O134	–3474	–758
174	O135	–3474	–866
175	O136	–3474	–975
176	O137	–3474	–1083
177	O138	–3474	–1191
178	O139	–3474	–1300
179	O140	–3474	–1408
180	O141	–3474	–1516
181	O142	–3474	–1625
182	O143	–3474	–1733
183	O144	–3474	–1841

■ PAD LAYOUT FOR SED1744D1B



Chip Size ..... 7.30mm × 4.48mm
Chip Thickness ..... 525μm ± 25μm
Pad Pitch ..... 108μm (Min.)
Gold bump dimensions (SED1744sD1B):
Size A ..... 94 × 134 ± 20μm (pads 1~15, 39~183)
Size B ..... 115 × 148 ± 20μm (pads 16~33, 38)
Size C ..... 115 × 134 ± 20μm (pads 34~37)

unit: μm

■ PAD COORDINATES

Pad		Coordinates	
No.	Name	X	Y
1	O145	–3228	–2064
2	O146	–3120	–2064
3	O147	–3012	–2064
4	O148	–2903	–2064
5	O149	–2795	–2064
6	O150	–2687	–2064
7	O151	–2578	–2064
8	O152	–2470	–2064
9	O153	–2362	–2064
10	O154	–2253	–2064
11	O155	–2145	–2064
12	O156	–2037	–2064

Pad		Coordinates	
No.	Name	X	Y
13	O157	–1929	–2064
14	O158	–1820	–2064
15	O159	–1712	–2064
16	EIO2	–1550	–2058
17	EIO1	–1417	–2058
18	GND	–1284	–2058
19	D0	–1151	–2058
20	D1	–1018	–2058
21	D2	–885	–2058
22	D3	–752	–2058
23	D4	–619	–2058
24	D5	–486	–2058

Pad		Coordinates	
No.	Name	X	Y
25	D6	–353	–2058
26	D7	–220	–2058
27	SHL	–87	–2058
28	XSCL	46	–2058
29	TEST	179	–2058
30	$\overline{INH}$	312	–2058
31	LP	445	–2058
32	V_{CC}	578	–2058
33	FR	711	–2058
34	V5	872	–2026
35	V3	1034	–2026
36	V2	1195	–2026

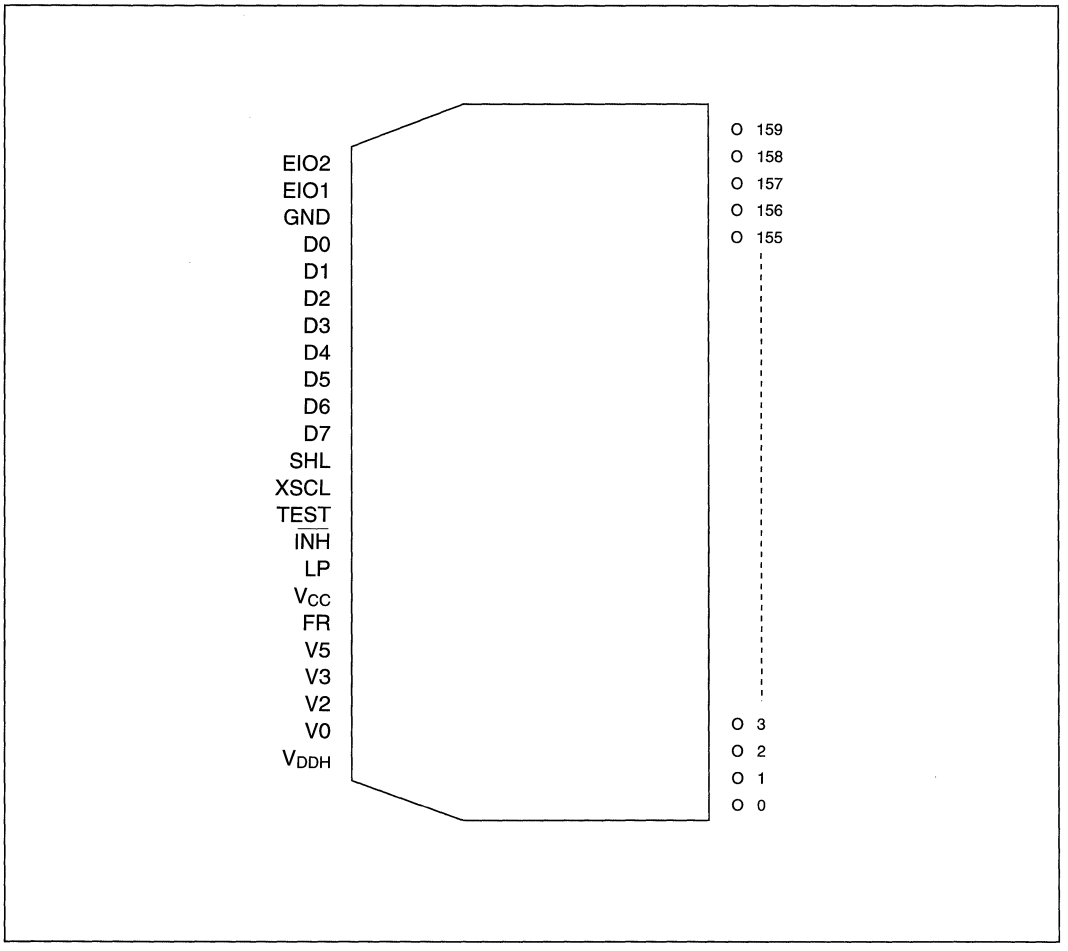
Pad		Coordinates	
No.	Name	X	Y
37	V0	1357	–2026
38	VDDH	1550	–2058
39	O0	1712	–2064
40	O1	1820	–2064
41	O2	1929	–2064
42	O3	2037	–2064
43	O4	2145	–2064
44	O5	2253	–2064
45	O6	2362	–2064
46	O7	2470	–2064
47	O8	2578	–2064
48	O9	2687	–2064
49	O10	2795	–2064
50	O11	2903	–2064
51	O12	3012	–2064
52	O13	3120	–2064
53	O14	3228	–2064
54	O15	3474	–1841
55	O16	3474	–1733
56	O17	3474	–1625
57	O18	3474	–1516
58	O19	3474	–1408
59	O20	3474	–1300
60	O21	3474	–1191
61	O22	3474	–1083
62	O23	3474	–975
63	O24	3474	–866
64	O25	3474	–758
65	O26	3474	–650
66	O27	3474	–542
67	O28	3474	–433
68	O29	3474	–325
69	O30	3474	–217
70	O31	3474	–108
71	O32	3474	0
72	O33	3474	108
73	O34	3474	217
74	O35	3474	325
75	O36	3474	433
76	O37	3474	542
77	O38	3474	650
78	O39	3474	758
79	O40	3474	866
80	O41	3474	975
81	O42	3474	1083
82	O43	3474	1191
83	O44	3474	1300
84	O45	3474	1408
85	O46	3474	1516

Pad		Coordinates	
No.	Name	X	Y
86	O47	3474	1625
87	O48	3474	1733
88	O49	3474	1841
89	O50	3195	2064
90	O51	3087	2064
91	O52	2978	2064
92	O53	2870	2064
93	O54	2762	2064
94	O55	2553	2064
95	O56	2545	2064
96	O57	2437	2064
97	O58	2328	2064
98	O59	2220	2064
99	O60	2112	2064
100	O61	2004	2064
101	O62	1895	2064
102	O63	1787	2064
103	O64	1679	2064
104	O65	1570	2064
105	O66	1462	2064
106	O67	1354	2064
107	O68	1245	2064
108	O69	1137	2064
109	O70	1029	2064
110	O71	921	2064
111	O72	812	2064
112	O73	704	2064
113	O74	596	2064
114	O75	487	2064
115	O76	379	2064
116	O77	271	2064
117	O78	162	2064
118	O79	54	2064
119	O80	–54	2064
120	O81	–162	2064
121	O82	–271	2064
122	O83	–379	2064
123	O84	–487	2064
124	O85	–596	2064
125	O86	–704	2064
126	O87	–812	2064
127	O88	–921	2064
128	O89	–1029	2064
129	O90	–1137	2064
130	O91	–1245	2064
131	O92	–1354	2064
132	O93	–1462	2064
133	O94	–1570	2064
134	O95	–1679	2064

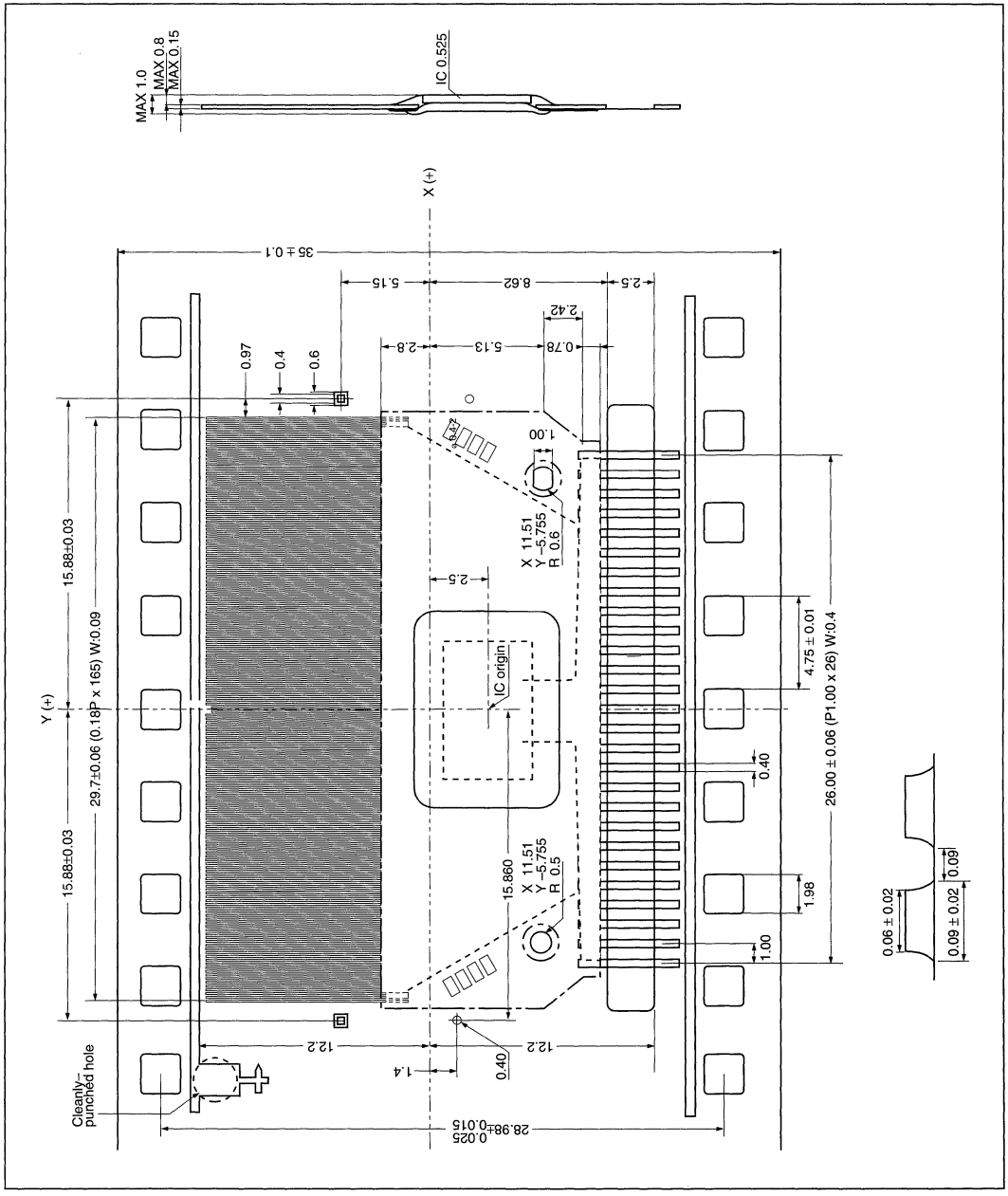
Pad		Coordinates	
No.	Name	X	Y
135	O96	–1787	2064
136	O97	–1895	2064
137	O98	–2004	2064
138	O99	–2112	2064
139	O100	–2220	2064
140	O101	–2328	2064
141	O102	–2437	2064
142	O103	–2545	2064
143	O104	–2653	2064
144	O105	–2762	2064
145	O106	–2870	2064
146	O107	–2978	2064
147	O108	–3087	2064
148	O109	–3195	2064
149	O110	–3474	1841
150	O111	–3474	1733
151	O112	–3474	1625
152	O113	–3474	1516
153	O114	–3474	1408
154	O115	–3474	1300
155	O116	–3474	1191
156	O117	–3474	1083
157	O118	–3474	975
158	O119	–3474	866
159	O120	–3474	758
160	O121	–3474	650
161	O122	–3474	542
162	O123	–3474	433
163	O124	–3474	325
164	O125	–3474	217
165	O126	–3474	108
166	O127	–3474	0
167	O128	–3474	–108
168	O129	–3474	–217
169	O130	–3474	–325
170	O131	–3474	–433
171	O132	–3474	–542
172	O133	–3474	–650
173	O134	–3474	–758
174	O135	–3474	–866
175	O136	–3474	–975
176	O137	–3474	–1083
177	O138	–3474	–1191
178	O139	–3474	–1300
179	O140	–3474	–1408
180	O141	–3474	–1516
181	O142	–3474	–1625
182	O143	–3474	–1733
183	O144	–3474	–1841

■ SED1742 TAPE-CARRIER PACKAGE

● Tape-Carrier Pinout

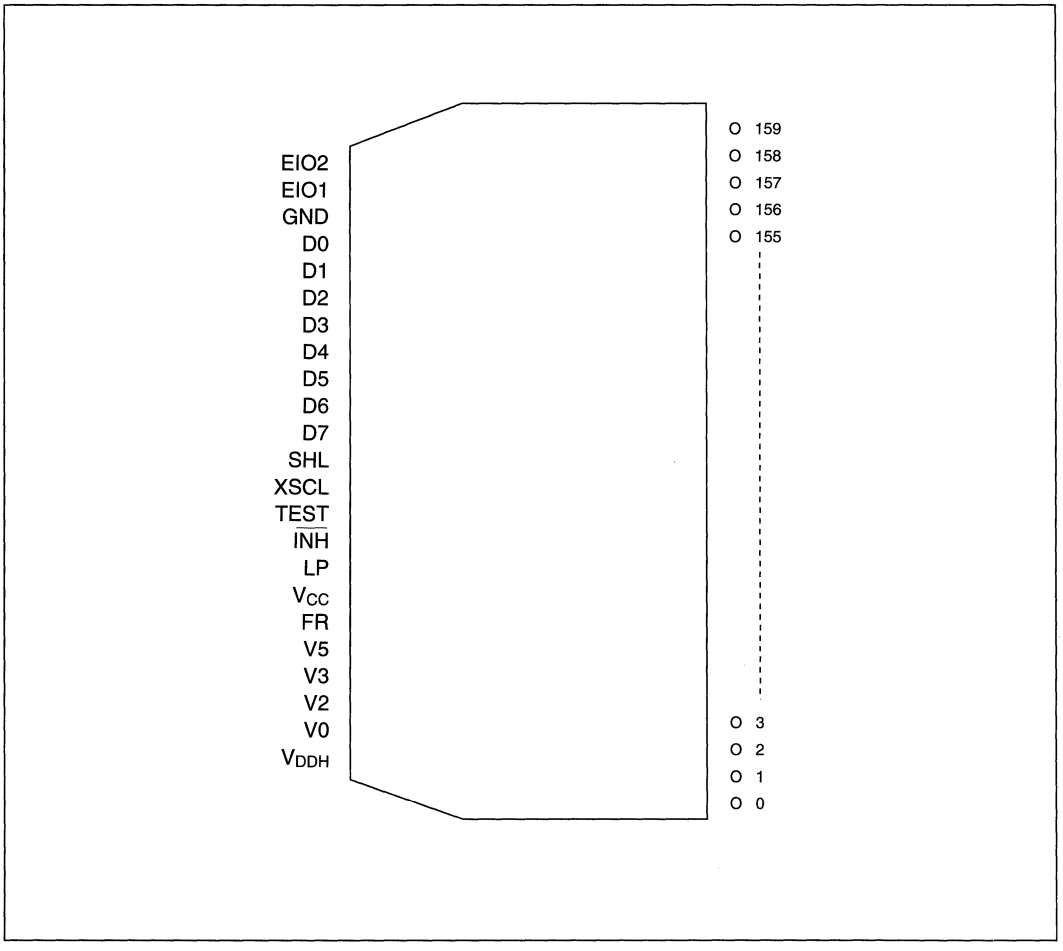


● Tape-Carrier Dimensions

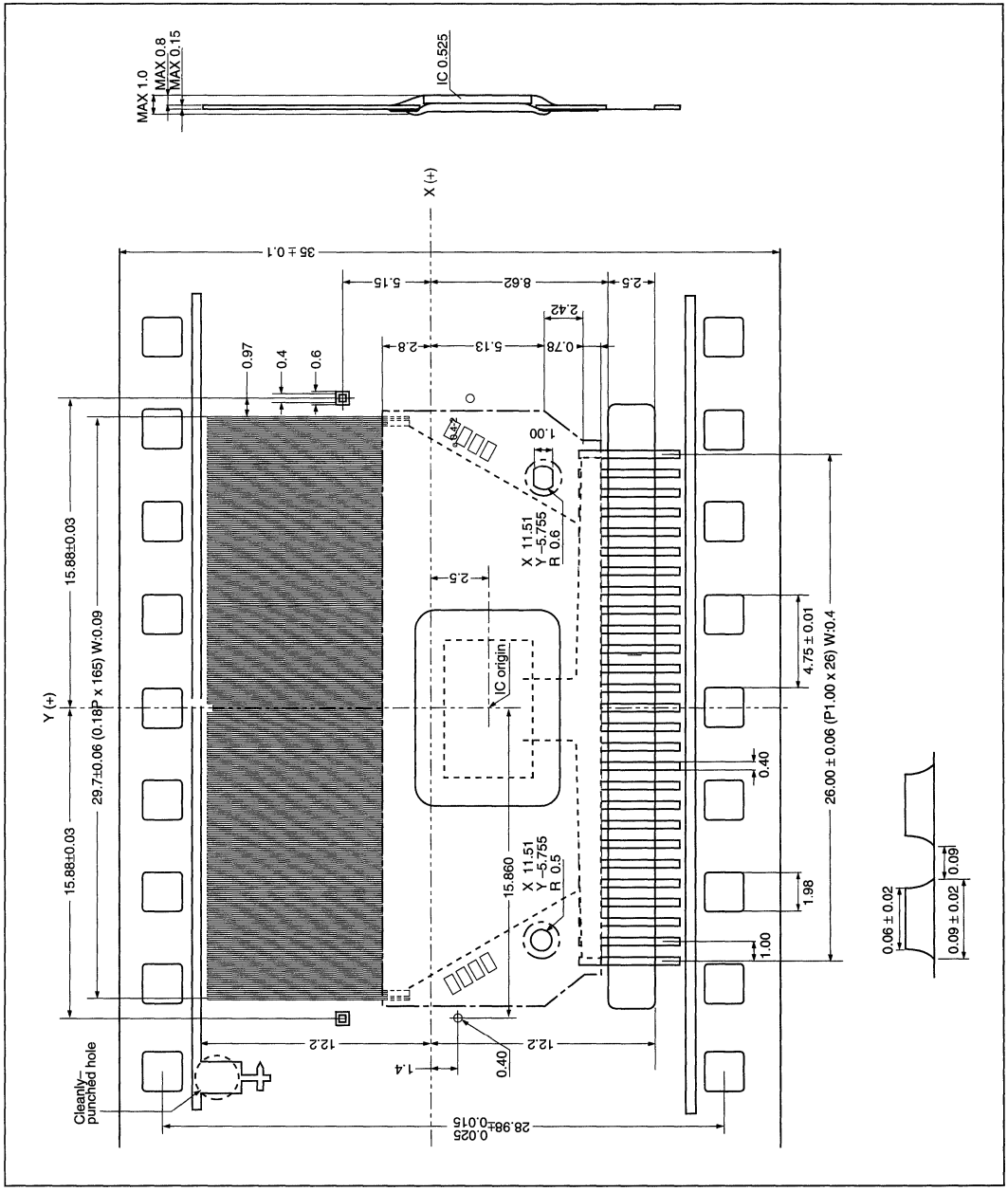


■ SED1744 TAPE-CARRIER PACKAGE

● Tape-Carrier Pinout



● Tape-Carrier Dimensions



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LOW-POWER 160-BIT LCD SEGMENT DRIVER

■ DESCRIPTION

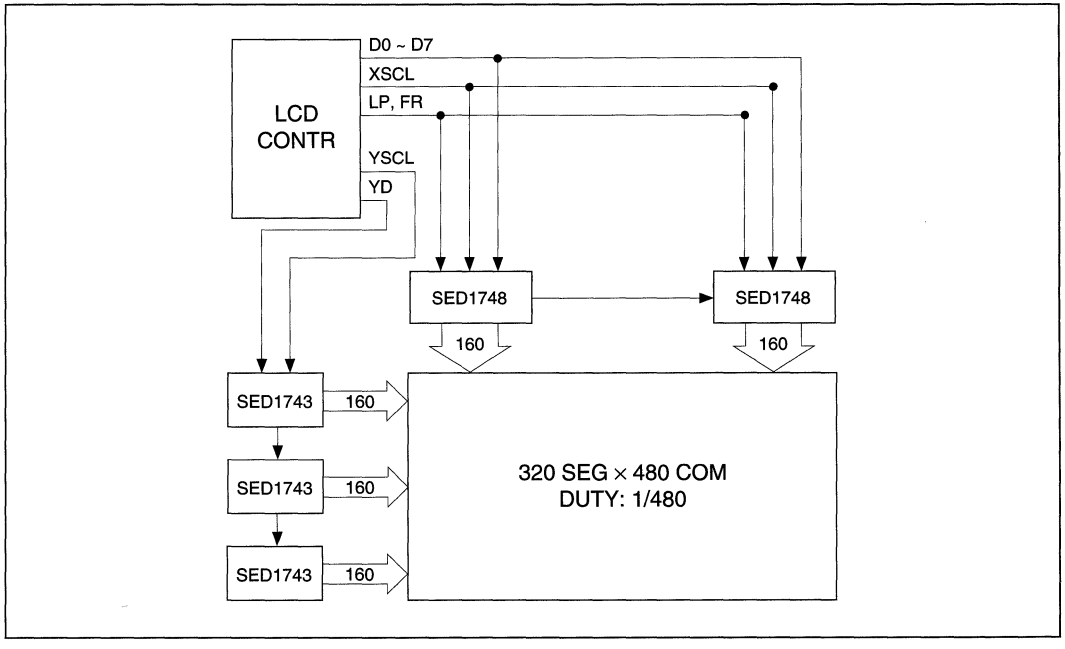
The SED1748 is a 160-bit dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of LCD drive voltages. The upper and lower LCD drive voltages (V0, V5) are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. The device uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate signals for each driver.

The SED1748 is used in conjunction with the SED1743 (160-bit common driver) to drive a large-capacity dot matrix LCD panel.

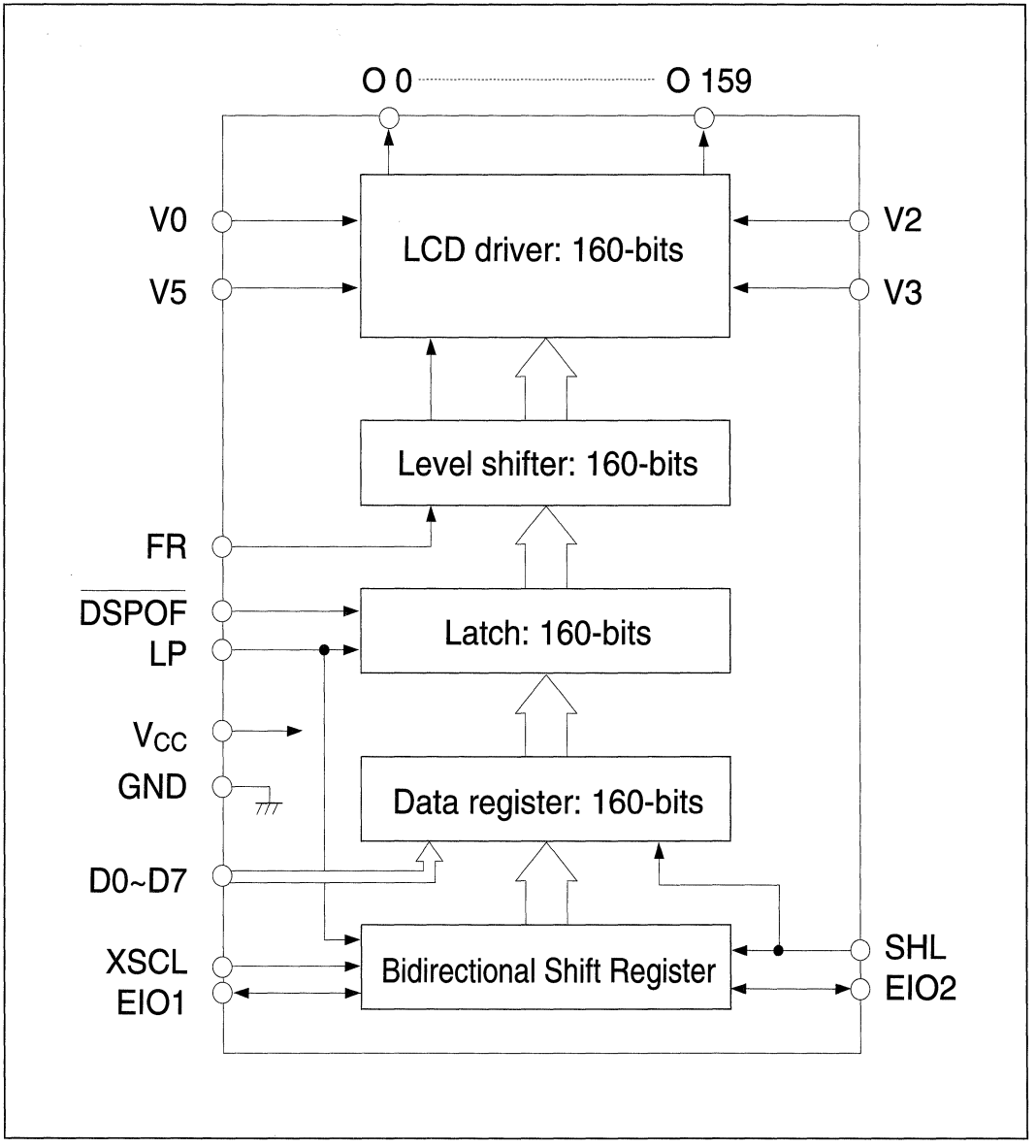
■ FEATURES

- Low-power, high-speed CMOS technology
- 160-bit segment (column) driver
- High-speed 8-bit data bus
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Unbiased display off function
- Adjustable offset bias of the LCD according to V_{DDH} and GND
- Shift clock frequency16MHz max at V_{DD} = 5V
- Ability to adjust offset bias of the LCD source from V_{DD}
- High-speed daisy chain enable support
- Adjustable offset bias of the liquid crystal according to the V0 and GND
- Wide range of LCD voltages ..... 8 to 42V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... Au bump (D_{OB})
  TAB (T_{OA})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Enable Shift Register

The enable shift register is a bi-directional shift register, where the shift direction is selected by SHL. When the enable signal is inactive, the SED1748 is in standby mode, where the internal clock is stopped and the data bus held LOW. When multiple SED1748s are used, the enable input of the first device should be connected to ground and the enable input of each successive device should be connected to the enable output of the preceding device. When 160 data bits have been latched into the SED1748, the enable output goes LOW, eliminating the need for an external control circuit.

● Data Register

The data register converts the input data into parallel display driver data under the control of the enable shift register.

● Data Latch

The data latch latches the data into the level shifter on the falling edge of LP.

● Level Shifter

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

● LCD Drivers

The LCD drivers generate the AC LCD driver waveforms. The output voltages are determined by the polarity of the FR signal, as shown in the following table:

$\overline{DSPOF}$	Input Data	FR	Output Voltage
H	H	H	V0
		L	V5
	L	H	V2
		L	V3
L	—	—	V5

■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>O0 to O159</td><td>O</td><td>LCD driver segment (column) output
The output changes with the LP's trailing edge.</td><td>160</td></tr>
<tr><td>D0 to D7</td><td>I</td><td>Display data input</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (trailing edge triggered)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch clock input (trailing edge triggered)</td><td>1</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>Enable I/O
● Configured by SHL.
● Output is reset to "H" by LP input. When the 160-bit display data is read, the output falls to "L" automatically.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction and input/output select input
● If the display data is entered in the input (D0, D1, ..., D7) in the order of (a0, a1, ..., a6, a7) (b0, b1, ..., b6, b7), ..., (t0, t1, ..., t6, t7), the relationship of the display data and the segment output is as given in the table below.
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">Output</th><th colspan="2">EIO</th></tr>
<tr><th>159</th><th>158</th><th>157</th><th>...</th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a0</td><td>a1</td><td>a2</td><td>...</td><td>t5</td><td>t6</td><td>t7</td><td>O</td><td>I</td></tr>
<tr><td>H</td><td>t7</td><td>t6</td><td>t5</td><td>...</td><td>a2</td><td>a1</td><td>a0</td><td>I</td><td>O</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD AC driver signal input</td><td>1</td></tr>
<tr><td>Vcc, GND</td><td>Power supply</td><td>Logic power input
GND: 0V, Vcc: +3.3V, +5V</td><td>2</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power supply</td><td>LCD driver power input
GND: 0V, V0: +14 to +42V
V0 ≥ V2 ≥ 7/9 × V0
2/9 × V0 ≥ V3 ≥ V5 ≥ GND</td><td>4</td></tr>
<tr><td>$\overline{\text{DSPOF}}$</td><td>I</td><td>Compulsion bias input
When the "L" level, the output is compelled to the V5 level.
* If you use this function, you cannot use to combine with the SED1703.</td><td>1</td></tr>
</table>

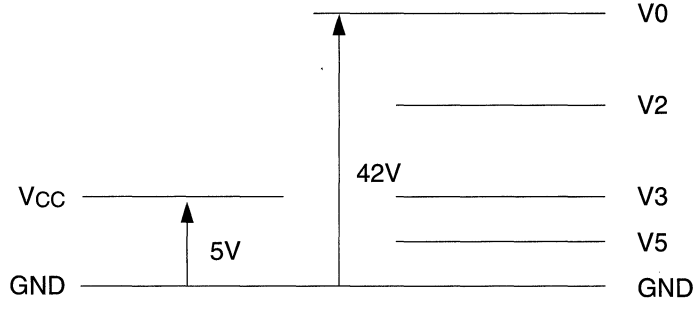
■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Supply voltage 1	V_{CC}	–0.3 to +7.0	V
Supply voltage 2	V0	–0.3 to +45.0	V
Supply voltage 3	V0, V2, V3, V5	GND – 0.3 to V0 + 0.3	V
Input voltage	VI	GND – 0.3 to V_{CC} + 0.3	V
Output voltage	VO	GND – 0.3 to V_{CC} + 0.3	V
EIO output voltage	IO1	20	mA
Operating temperature	T_{OPR}	–30 to +85	°C
Storage temperature 1	T_{STG1}	–65 to +150	°C
Storage temperature 2	T_{STG2}	–55 to +100	°C

Notes:

1. All voltages are given relative to GND = 0V.
2. For storage temperature 1 – Die
   For storage temperature 2 – TAB mounted
3. V0, V2, and V3 must satisfy the condition $V_{DD} \geq V0 \geq V2 \geq V3 \geq V5 \geq V_{EE}$

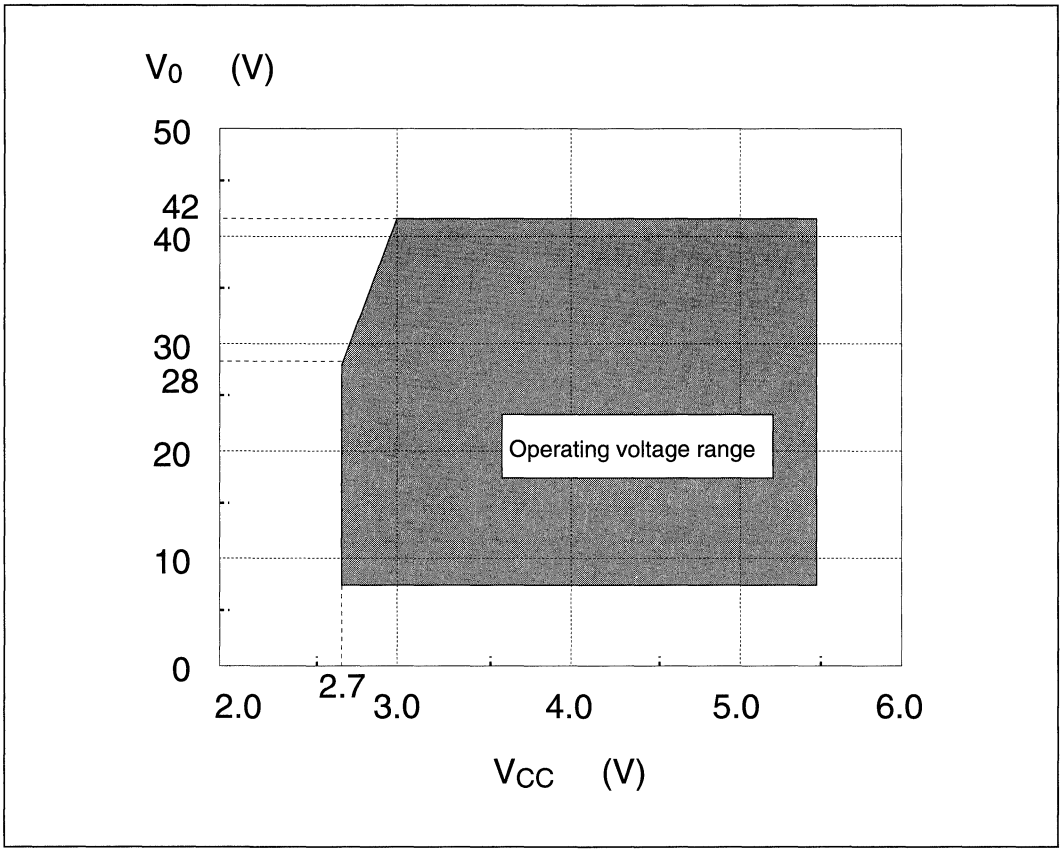


4. This LSI has high LCD driver voltage. As a result, if the logic power is being floated and $V_{CC} \leq 2.6V$ in the LCD driver, the LSI may be damaged because of the excess current.

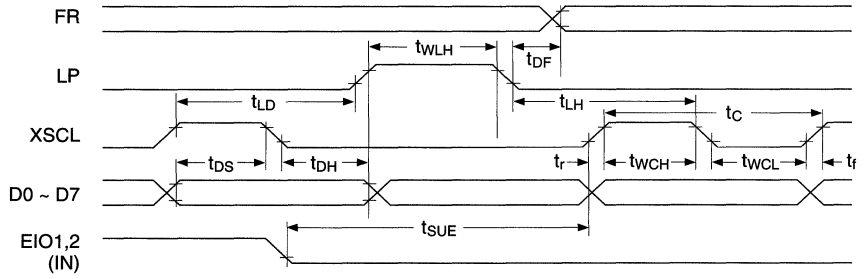
● DC Electrical Characteristics

Parameter	Symbol	Conditions		Pin Name	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}			V_{CC}	2.7	—	5.5	V
Recommended operating voltage	V0			V0	14.0	—	40.0	V
Operation voltage	V0	Function		V0	8.0	—	42.0	V
Supply voltage (2)	V2			V2	7/9 × V0	—	—	V
Supply voltage (3)	V3			V3	GND	—	2/9 × V0	V
High-level input current	V_{IH}			EIO1, EIO2, FR, D0 to D7, XSCL, SHL, LP, $\overline{DSPOF}$	0.8 × V_{CC}	—	—	V
Low-level input current	V_{IL}				—	—	0.2 × V_{CC}	V
High-level output current	V_{OH}	V_{CC} = 2.7 to 5.5V	I_{OH} = 0.6mA	EIO1, EIO2	V_{CC} – 0.4	—	—	V
Low-level output voltage	V_{OL}		I_{OL} = 0.6mA		—	—	0.4	V
Input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		D0 to D7, LP, FR, XSCL, SHL, $\overline{DSPOF}$	—	—	2.0	µA
Input/output leakage current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		EIO1, EIO2	—	—	5.0	µA
Quiescent current	I_{GND}	V0 = 14.0 to 42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Segment ON resistance	R_{SEG}	ΔV_{ON} =0.5V	V0 = +36.0V, 1/24	O0 to O159	—	0.62	1.9	KΩ
			V0 = +26.0V, 1/20		—	0.68	2.0	
Deviation in chip ON resistance	ΔR_{SEG}	ΔV_{ON} = 0.5 V0 = +36.0V, 1/24		O0 to O159	—	—	90	Ω
Operating current (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} + GND, f_{XSCL} = 5.38MHz, f_{LP}=33.6KHz, f_{FR} = 70Hz, Input data: Shimatsu display, no load		V_{CC}	—	0.5	1.1	mA
		V_{CC} = +3.0V, other conditions as above		V_{CC}	—	0.2	0.6	mA
Operating current (2)	I_O	V0=+30.0V, V_{CC}=+5.0V, V3=+4.0V, V2=+26.0V, V5 = 0.0V, other conditions as for I_{CC}		V0	—	0.15	0.9	mA
Input capacitance	C_I	Freq. = 1MHz, T_a = 25°C chip package		D0 to D7, LP, FR, XSCL, SHL, DSPOF	—	—	8	pF
Input/output capacitance	$C_{I/O}$			EIO1, EIO2	—	—	15	pF

● **Operating Voltage Range for Vcc and V0**



- **AC Electrical Characteristics**
  - **Input Timing**



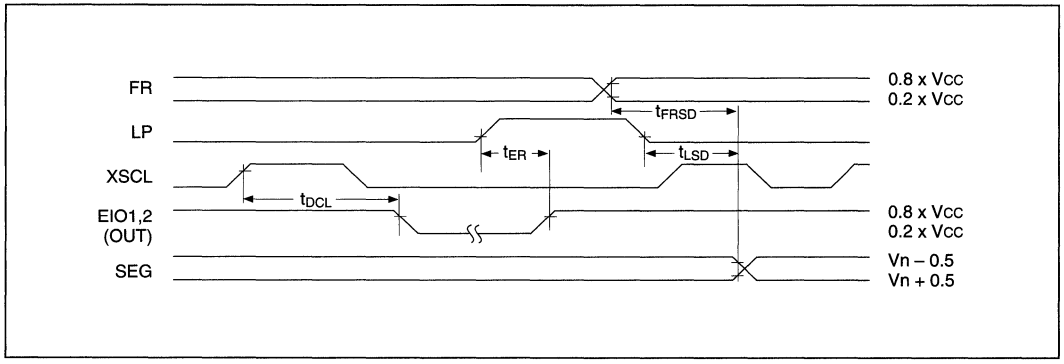
V_{CC} = 5.0V ± 10%, T_a = −30 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
XSCL cycle time	tC	tr, tf ≤ 11ns	62	—	ns
XSCL high-level pulse width	tWCH		20	—	ns
XSCL low-level pulse width	tWCL		20	—	ns
Data setup time	tDS		10	—	ns
Data hold time	tDH		10	—	ns
XSCL → LP rising edge	tLD		−5	—	ns
LP → XSCL falling edge	tLH		30	—	ns
LP high-level pulse width	tWLH		40	—	ns
			35	—	ns
FR phase difference	tDF		−300	+300	ns
EIO setup time	tSUE		30	—	ns
Input signal change time	tr, tf		—	50	ns

V_{CC} = 2.7 to 4.5V, T_a = −30 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
XSCL cycle time	tC	tr, tf ≤ 15ns	100	—	ns
XSCL high-level pulse width	tWCH		35	—	ns
XSCL low-level pulse width	tWCL		35	—	ns
Data setup time	tDS		15	—	ns
Data hold time	tDH		10	—	ns
XSCL → LP rising edge	tLD		−10	—	ns
LP → XSCL falling edge	tLH		60	—	ns
LP high-level pulse width	tWLH		75	—	ns
			65	—	ns
FR phase difference	tDF		−300	+300	ns
EIO setup time	tSUE		40	—	ns
Input signal change time	tr, tf		—	50	ns

○ **Output Timing**



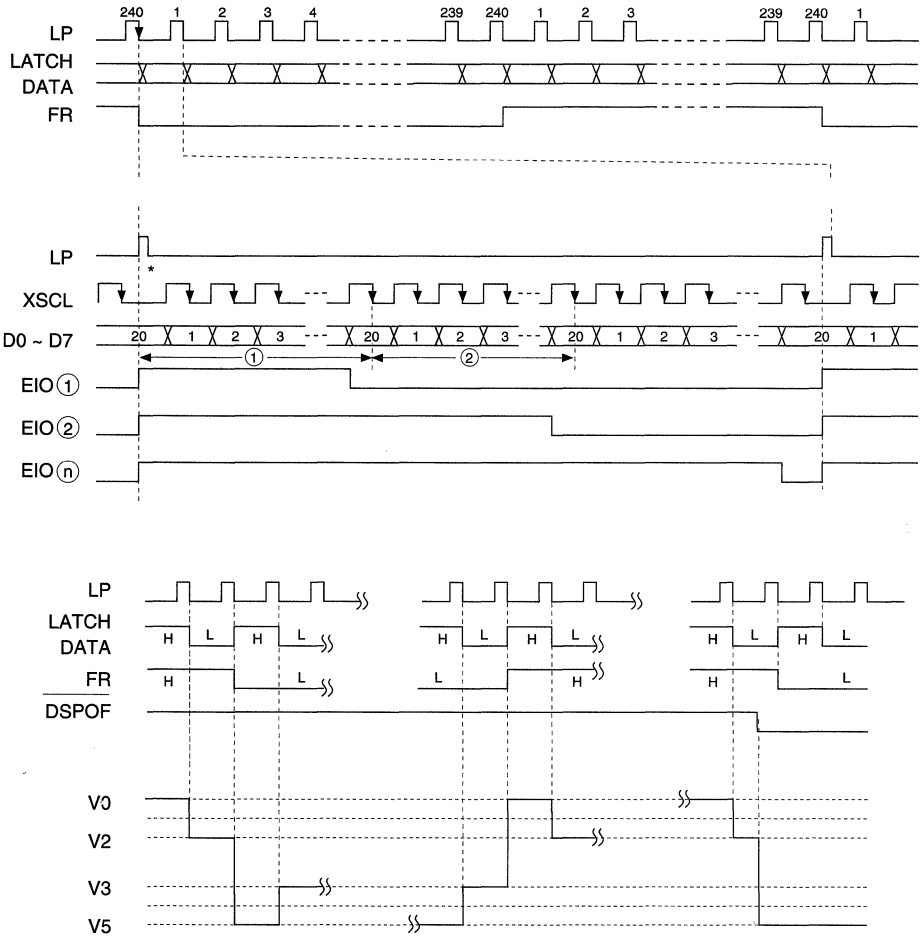
V_{CC} = 5.0V ± 10%, V0 = 14.0 to 42.0V

Parameter	Symbol	Conditions	Min	Max	Unit
EIO reset time	t_{ER}	CL = 15pF (EIO)	—	120	ns
EIO output delay time	t_{DCL}		—	45	ns
LP → SEG delay time	t_{LSD}	CL = 100pF (On)	—	200	ns
FR → SEG delay time	t_{FRSD}		—	400	ns

V_{CC} = 2.7 to 4.5V, V0 = 14.0 to 28.0V

Parameter	Symbol	Conditions	Min	Max	Unit
EIO reset time	t_{ER}	CL = 15pF (EIO)	—	240	ns
EIO output delay time	t_{DCL}		—	85	ns
LP → SEG delay time	t_{LSD}	CL = 100pF (On)	—	400	ns
FR → SEG delay time	t_{FRSD}		—	800	ns

- **Timing Diagrams**
  - **1/240 Duty Cycle**



NOTES:

1. The circled numerals ① to ⓝ denote the position of the device in the chain.
2. When transferring data at high speed, one cycle of XSCL must be lengthened to satisfy t_{LH}.

■ LCD DRIVER POWER SUPPLY

● Generating LCD Driver Voltage

To obtain individual voltage levels for LCD driver, register-split the potential between V0-GND and drive the LCD with the voltage follower using the operation amplifier. When using the operation amplifier, V5 and GND are separated. However, if the potential of V5 is higher than the GND potential and the potential difference increases, the LCD driver capability decreases. To above this, set V5 and GND within the range from 0 to 2.5V. If an operation amplifier is not used, connect V5 and GND. If there are direct resistors on the V0 (GND) power line, voltage falls in V0 (GND) at the LSI power pins. This is caused by IO at the time of signal change. As a result, the relationship ($V0 \geq V2 \geq V3 \geq V5 \geq GND$) for intermediate potential of LCD cannot be maintained and the LSI may be damaged.

To insert a protective resistor, the voltage must be stabilized according to the capacity.

● Power-Up/Power-Down Sequence

This LSI has high LCD driver voltage. As a result, if the logic power is being floated and $V_{CC} \leq 2.6V$ is applied in the LCD driver, the LSI may be damaged because of the excess current.

Until the LCD driver voltage is stabilized, use the display off function ($\overline{DSPOF}$) to set the potential of the LCD drive output to V5 level.

Follow the sequence given below when turning the power on/off.

To turn on the power:

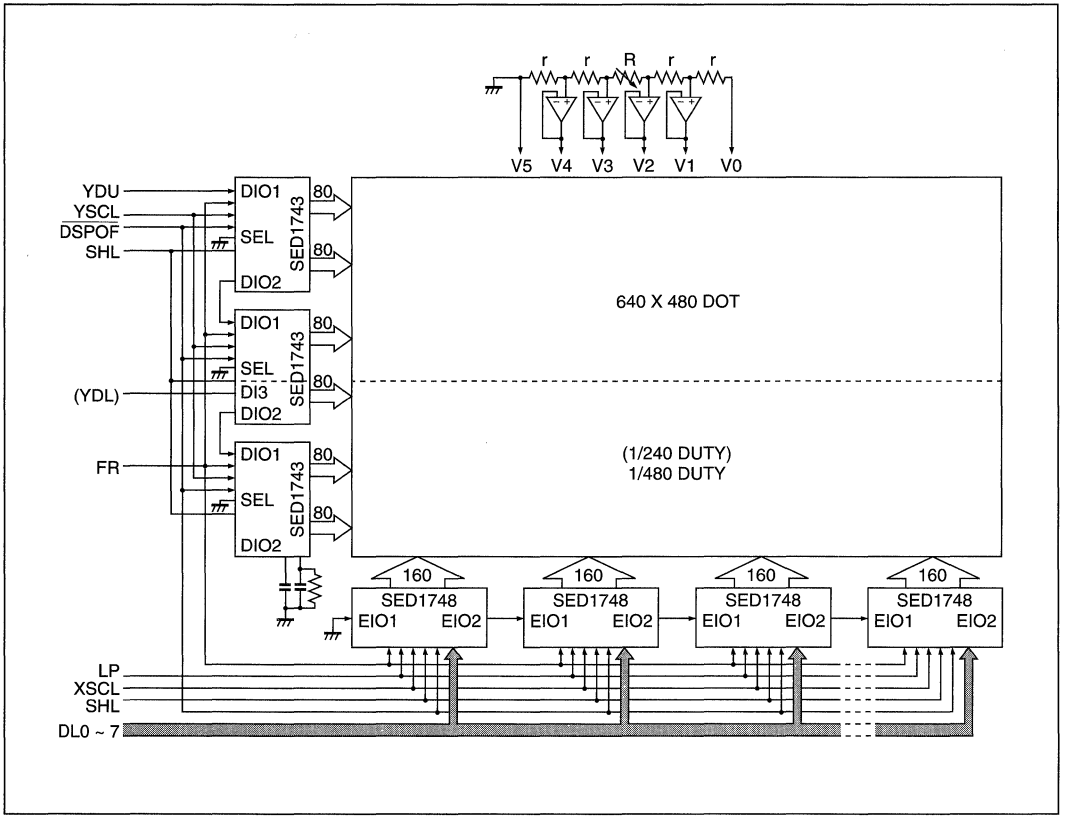
1. Turn on the logic power
2. Turn the LCD driver on
   (or turn them on simultaneously)

To turn off the power:

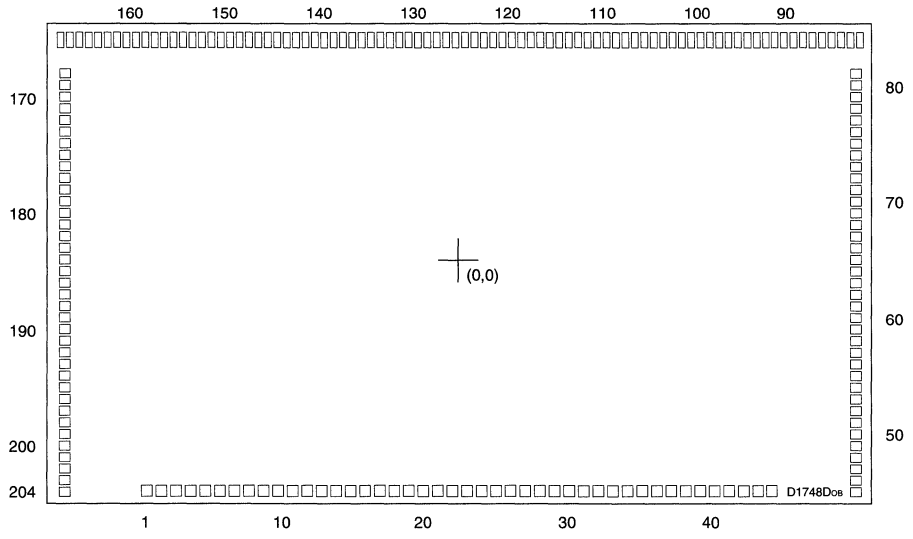
1. Turn off the LCD driver
2. Turn off the logic power
   (or turn them off simultaneously)

To avoid excess current, insert the high-speed fuse in series with the LCD power. Select the appropriate value for a protective resistor according to the capacity of an LCD cell.

■ TYPICAL APPLICATION



■ PAD LAYOUT



Chip size ..... 7.30mm × 4.48mm
Pad pitch ..... 81.7μm (Min.)
Chip thickness ..... 525μm ± 25μm

1) Au bump dimensions (SED1748D0B)

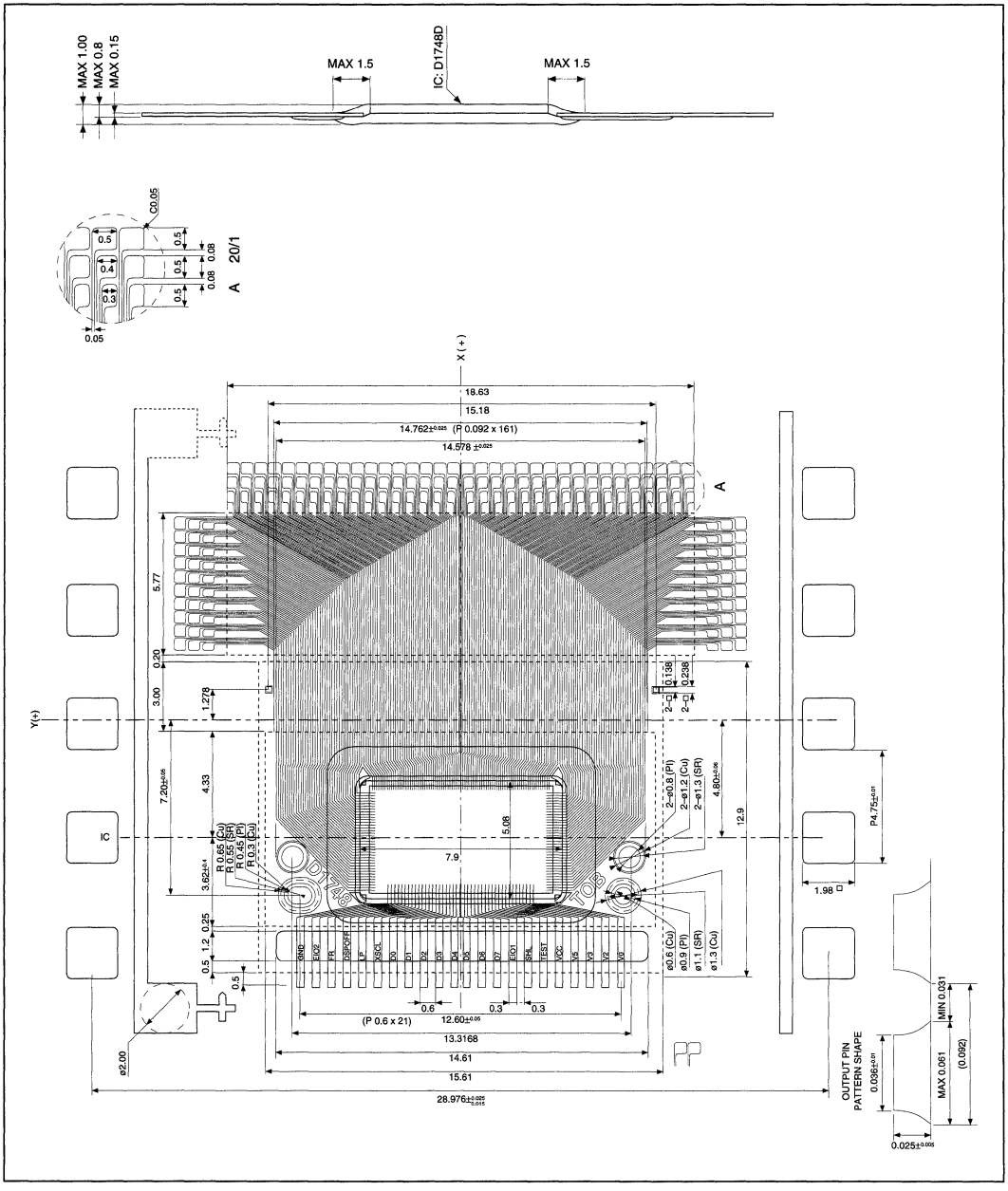
- Size A : 97μm × 88μm ± 4μm (pads 1 to 44)
- Size B : 82μm × 80μm ± 4μm (pads 45 to 48, 66 to 81, 168 to 183, 201 to 204)
- Size C : 82μm × 70μm ± 4μm (pads 49 to 65, 184 to 200)
- Size D : 65μm × 164μm ± 4μm (pads 82 to 85, 164 to 167)
- Size E : 53μm × 164μm ± 4μm (pads 86 to 163)

■ PAD COORDINATES

Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	GND	–2757	–2080
2	GND	–2630	–2080
3	EIO2	–2500	–2080
4	EIO2	–2373	–2080
5	FR	–2244	–2080
6	FR	–2117	–2080
7	DSPOFF	–1987	–2080
8	DSPOFF	–1860	–2080
9	LP	–1731	–2080
10	LP	–1604	–2080
11	XSCL	–1474	–2080
12	XSCL	–1347	–2080
13	D0	–1218	–2080
14	D0	–1091	–2080
15	D1	–961	–2080
16	D1	–834	–2080
17	D2	–705	–2080
18	D2	–578	–2080
19	D3	–448	–2080
20	D3	–321	–2080
21	D4	–192	–2080
22	D4	–65	–2080
23	D5	65	–2080
24	D5	192	–2080
25	D6	321	–2080
26	D6	448	–2080
27	D7	578	–2080
28	D7	705	–2080
29	EIO1	834	–2080
30	EIO1	961	–2080
31	SHL	1091	–2080
32	SHL	1218	–2080
33	NC	1347	–2080
34	NC	1474	–2080
35	Vcc	1604	–2080
36	Vcc	1731	–2080
37	V5	1860	–2055
38	V5	1987	–2055
39	V3	2117	–2040
40	V3	2244	–2040
41	V2	2373	–2024
42	V2	2500	–2024
43	V0	2630	–2009
44	V0	2757	–2009
45	O0	3492	–2088
46	O1	3492	–1978
47	O2	3492	–1868
48	O3	3492	–1758
49	O4	3492	–1652
50	O5	3492	–1551
51	O6	3492	–1451
52	O7	3492	–1350
53	O8	3492	–1249
54	O9	3492	–1149
55	O10	3492	–1048
56	O11	3492	–947
57	O12	3492	–846
58	O13	3492	–745
59	O14	3492	–645
60	O15	3492	–544
61	O16	3492	–444
62	O17	3492	–343
63	O18	3492	–242
64	O19	3492	–142
65	O20	3492	–41
66	O21	3492	65
67	O22	3492	175
68	O23	3492	285
69	O24	3492	395
70	O25	3492	505
71	O26	3492	616
72	O27	3492	726
73	O28	3492	836
74	O29	3492	946
75	O30	3492	1056
76	O31	3492	1167
77	O32	3492	1277
78	O33	3492	1387
79	O34	3492	1497
80	O35	3492	1607
81	O36	3492	1718
82	O37	3512	2051
83	O38	3419	2051
84	O39	3326	2051
85	O40	3233	2051
86	O41	3145	2051
87	O42	3064	2051
88	O43	2982	2051
89	O44	2900	2051
90	O45	2819	2051
91	O46	2737	2051
92	O47	2655	2051
93	O48	2574	2051
94	O49	2492	2051
95	O50	2410	2051
96	O51	2328	2051
97	O52	2247	2051
98	O53	2165	2051
99	O54	2083	2051
100	O55	2002	2051
101	O56	1920	2051
102	O57	1838	2051
103	O58	1757	2051
104	O59	1675	2051
105	O60	1593	2051
106	O61	1511	2051
107	O62	1430	2051
108	O63	1348	2051
109	O64	1266	2051
110	O65	1185	2051
111	O66	1103	2051
112	O67	1021	2051
113	O68	940	2051
114	O69	858	2051
115	O70	776	2051
116	O71	694	2051
117	O72	613	2051
118	O73	531	2051
119	O74	449	2051
120	O75	368	2051
121	O76	286	2051
122	O77	204	2051
123	O78	123	2051
124	O79	41	2051
125	O80	–41	2051
126	O81	–123	2051
127	O82	–204	2051
128	O83	–286	2051
129	O84	–368	2051
130	O85	–449	2051
131	O86	–531	2051
132	O87	–613	2051
133	O88	–694	2051
134	O89	–776	2051
135	O90	–858	2051
136	O91	–940	2051
137	O92	–1021	2051
138	O93	–1103	2051
139	O94	–1185	2051
140	O95	–1266	2051
141	O96	–1348	2051
142	O97	–1430	2051
143	O98	–1511	2051
144	O99	–1593	2051
145	O100	–1675	2051
146	O101	–1757	2051
147	O102	–1838	2051
148	O103	–1920	2051
149	O104	–2002	2051
150	O105	–2083	2051
151	O106	–2165	2051
152	O107	–2247	2051
153	O108	–2328	2051
154	O109	–2410	2051
155	O110	–2492	2051
156	O111	–2574	2051
157	O112	–2655	2051
158	O113	–2737	2051
159	O114	–2819	2051
160	O115	–2900	2051
161	O116	–2982	2051
162	O117	–3064	2051
163	O118	–3145	2051
164	O119	–3233	2051
165	O120	–3326	2051
166	O121	–3419	2051
167	O122	–3512	2051
168	O123	–3492	1718
169	O124	–3492	1607
170	O125	–3492	1497
171	O126	–3492	1587
172	O127	–3492	1277
173	O128	–3492	1167
174	O129	–3492	1056
175	O130	–3492	946
176	O131	–3492	836
177	O132	–3492	726
178	O133	–3492	616
179	O134	–3492	505
180	O135	–3492	395
181	O136	–3492	285
182	O137	–3492	175
183	O138	–3492	65
184	O139	–3492	–41
185	O140	–3492	–142
186	O141	–3492	–242
187	O142	–3492	–343
188	O143	–3492	–444
189	O144	–3492	–544
190	O145	–3492	–645
191	O146	–3492	–746
192	O147	–3492	–846
193	O148	–3492	–947
194	O149	–3492	–1048
195	O150	–3492	–1149
196	O151	–3492	–1249
197	O152	–3492	–1350
198	O153	–3492	–1451
199	O154	–3492	–1551
200	O155	–3492	–1652
201	O156	–3492	–1758
202	O157	–3492	–1868
203	O158	–3492	–1978
204	O159	–3492	–2088

■ EXTERNAL PACKAGE DIAGRAM



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CMOS LCD SEGMENT DRIVER

■ DESCRIPTION

The SED1752 Series is a single-chip LCD driver for high-capacity color dot-matrix STN liquid crystal display (LCDs). It incorporates 240 segment (column) driver outputs and is designed for use in conjunction with the SED1743 common (row) driver.

The SED1752 uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

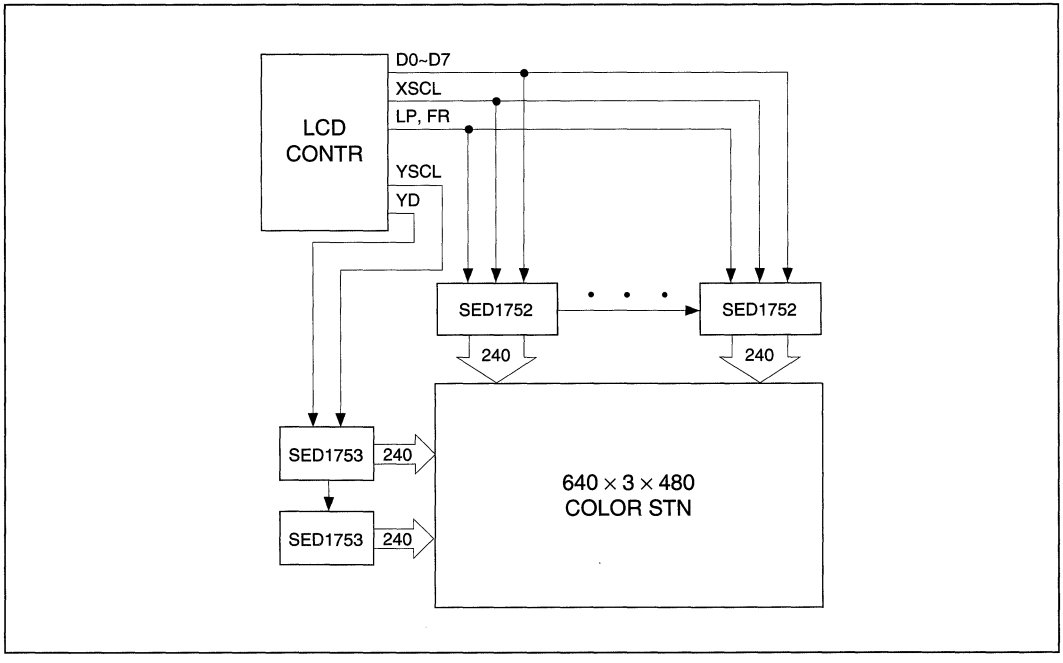
■ FEATURES

- 240 LCD segment drive outputs
- 8-bit data
- Wide +8 to +42 voltage of LCD drive voltages (V_{CC} = 3 to 5.5V)
- Daisy-chained input/output enables
- Low-power, high-speed data transfer—20MHz clock frequency at V_{CC} = 5V ± 10% and 10MHz clock frequency at V_{CC} = 2.7V.
- Duty cycles up to 1/500
- Adjustable LCD drive voltage relative to ground and V_{DDH}
- Zero-bias display disable function
- 2.7 to 5.5V supply
- Tape-carrier package

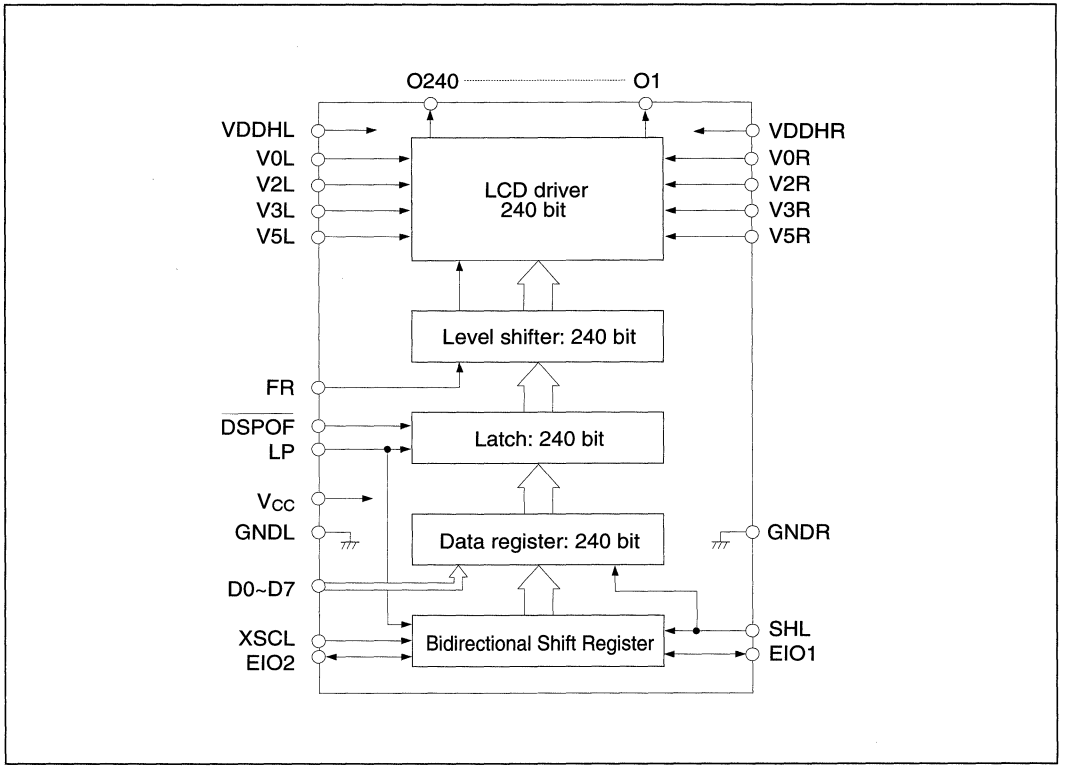
  T0A ..... Slim TAB (9.3mm)

  T0B ..... Ultra Slim TAB (7.3mm)

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ FUNCTION OF EACH BLOCK

● Enable Shift Register

The enable shift register is a bidirectional shift register of which the shift direction is being selected by the SHL input and the shift register output is used to store data bus signals into the data register.

When the enable signal is in disabled state, the internal clock signal and the data bus are fixed to "L", thus going into a power saving mode.

When using a multiple number of segment drivers, make cascade connections of EIO terminals of respective drivers to connect the EIO terminal of the top driver to "GND". Since the enable control circuit automatically senses completion of receiving 240 bit equivalent data to transfer the enable signal automatically, control signal of a separate control LSI is not needed.

● Data Register

This register works to make sseries or parallel conversion of data bus signals according to the enable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independent from the number of the shift clock inputs.

● Latch

It takes in the content of the data register at the falling edge trigger to transfer the output to the level shifter.

- **Level Shifter**

  This is a level interface circuit to convert the voltage level of signals from the logic operation level to LCD drive level.

- **LCD Driver**

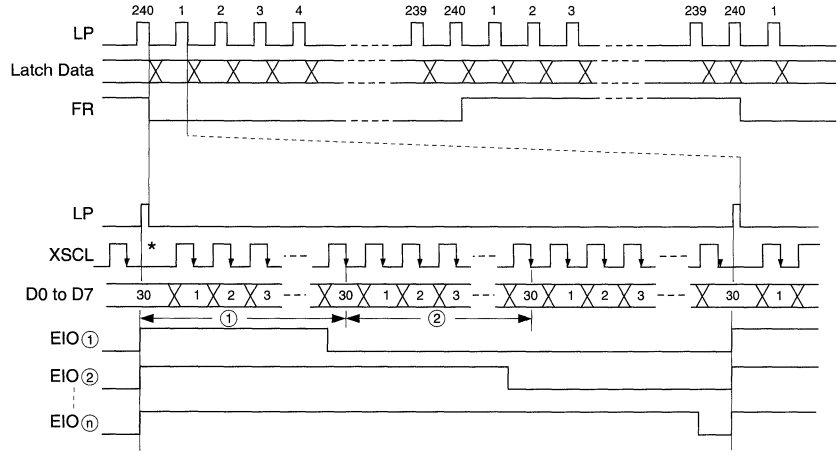
  It outputs the LCD driving voltage.

  In the table to the right are the relations between data bus signals, alternating current signal FR levels and segment output voltages.

$\overline{DSPOF}$	Data Bus Signals	FR	Voltage Outputs of the Driver
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_5

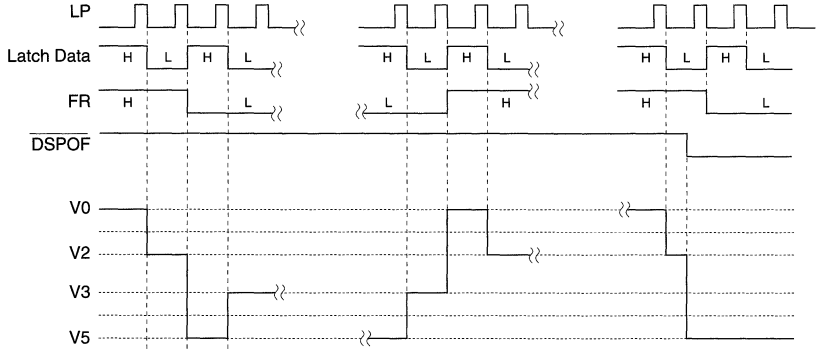
- **Timing Diagram**

In case of 1/240 Duty (an example)



① to ⓝ stands for the cascade numbers of the driver.

* When making high speed data transfer, it becomes necessary to secure a longer XSCL cycle when determining the LP pulse insertion timing in order to maintain the specified value of LP → XSCL (t_{LH}).



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Number of Pins</th></tr>
<tr><td>O1 ~ O240</td><td>O</td><td>LCD driving segment (column) output.
The output varies at the falling edge of LP.</td><td>240</td></tr>
<tr><td>D0 ~ D7</td><td>I</td><td>Display data input terminals</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>For input of the shift clock signals of the display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>For input of the latch pulse signals of the display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O.
Setting to I or O is determined by the SHL input level.
The output is reset by the LP input and when 240 bit equivalent data are received, it falls to “L” automatically.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO terminal I/O control signal input.
When data are input to terminals D_0, D_1, ..., D_7 in the order of F_0, F_1, ..., F_7 first, and in the order of L0, L1, outputs are as follows:
F (First), L(Last)
<table>
<tr><th rowspan="2">SHL</th><th colspan="8">Output</th><th colspan="2">EIO</th></tr>
<tr><th>0240</th><th>0239</th><th>0238</th><th></th><th>03</th><th>02</th><th>01</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>L0</td><td>L1</td><td>L2</td><td>...</td><td>F5</td><td>F6</td><td>F7</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>F7</td><td>F6</td><td>F5</td><td>...</td><td>L2</td><td>L1</td><td>L0</td><td>Output</td><td>Input</td></tr>
</table>
(Note) The relations between the data and segment outputs are determined independently from the number of the shift clocks.</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL, GNDR</td><td>Power supply</td><td>Logic operation power supply: GND: 0V
V_{CC}: +3.3, +5V</td><td>2</td></tr>
<tr><td>V_{DDHL}, V_{DDHR}</td><td rowspan="5">Power supply</td><td>LCD drive circuit power supply V_{DDH}</td><td rowspan="5">GND: 0V
V_{DDH}: 14~42V
$V_{DDH} \geq V_0 \geq V_2 \geq 7/9V_0$
$2/9V_0 \geq V_3 \geq V_5 \geq GND$</td><td rowspan="5">10</td></tr>
<tr><td>V0L, V0R</td><td>LCD drive circuit power supply V_0</td></tr>
<tr><td>V2L, V2R</td><td>LCD drive circuit power supply V_2</td></tr>
<tr><td>V3L, V3R</td><td>LCD drive circuit power supply V_3</td></tr>
<tr><td>V5L, V5R</td><td>LCD drive circuit power supply V_5</td></tr>
<tr><td>DSPOF</td><td>I</td><td>For forced bias fixed input.
“L” level output is forcefully made to V_5 level.
* When using this function, combined use with SED1703 is not applicable.</td><td>1</td></tr>
<tr><td colspan="3">Total</td><td>268</td></tr>
</table>

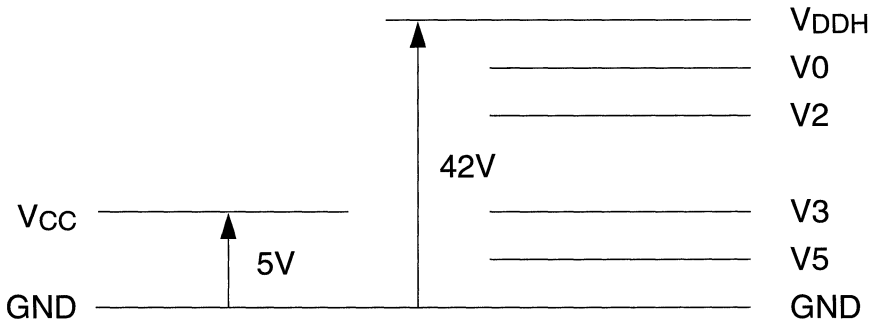
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	–0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	–0.3 to V_{CC} + 0.3	V
Output voltage	V_O	–0.3 to V_{CC} + 0.3	V
EIO output current	I_{O1}	20	mA
Working temperature	T_{OPR}	–30 to +85	°C
Storage temperature	T_{STG}	–55 to +100	°C

Notes: 1. All the voltage ratings are based on GND = 0V.

2. The storage temperature 1 is applicable to independent chips and the storage temperature 2 is applicable to the TCP modular state.

3. V_0, V_2, V_3 and V_5 should always be in the order of $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND.



4. If the logic operation power goes into a floating state or if V_{CC} drops to 2.6V or below while the LCD driving power is being applied, the LSI may be damaged. Therefore, keep from occurrence of the aforementioned status.

   Specifically, pay close attention to the power supply sequence at times of turning the system power on and off.

■ ELECTRICAL CHARACTERISTICS

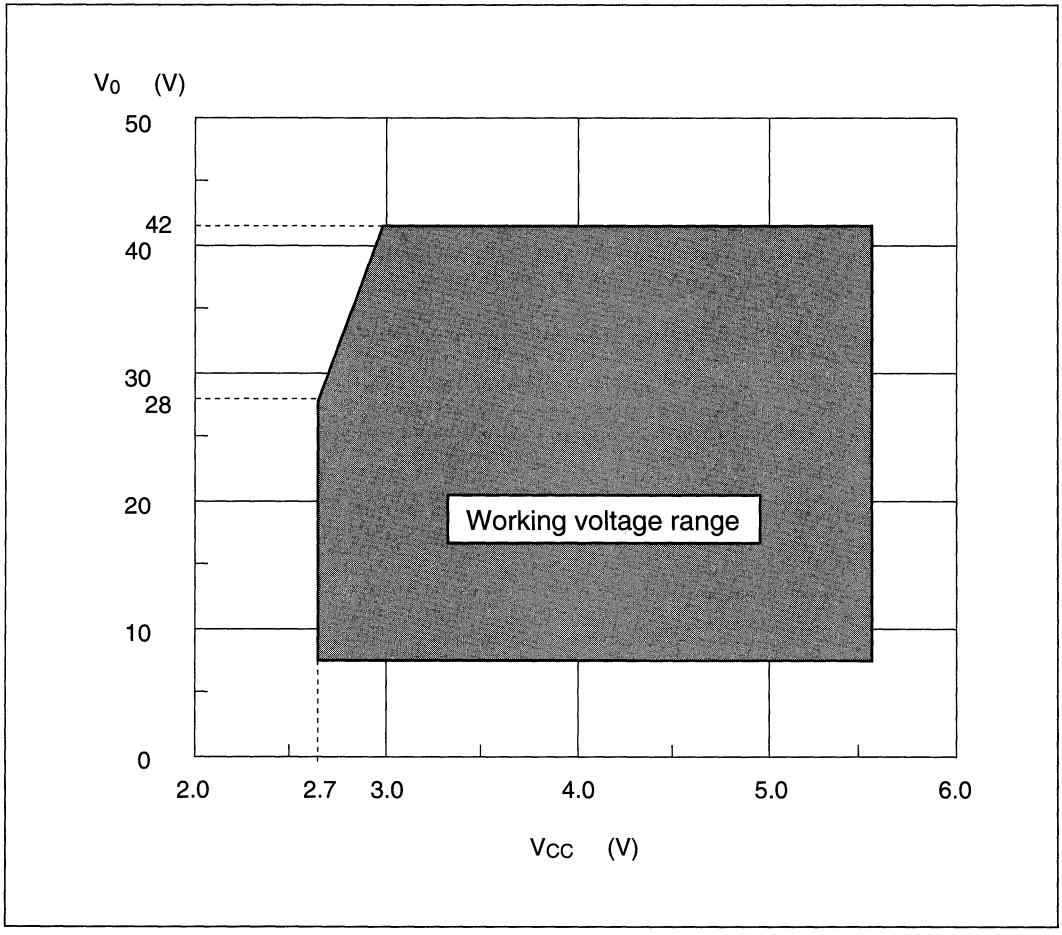
● DC Characteristics

Unless otherwise specified, GND = V_5 = 0, V_{CC} = +5.0V ±10%, T_a = –30 to ±85°C

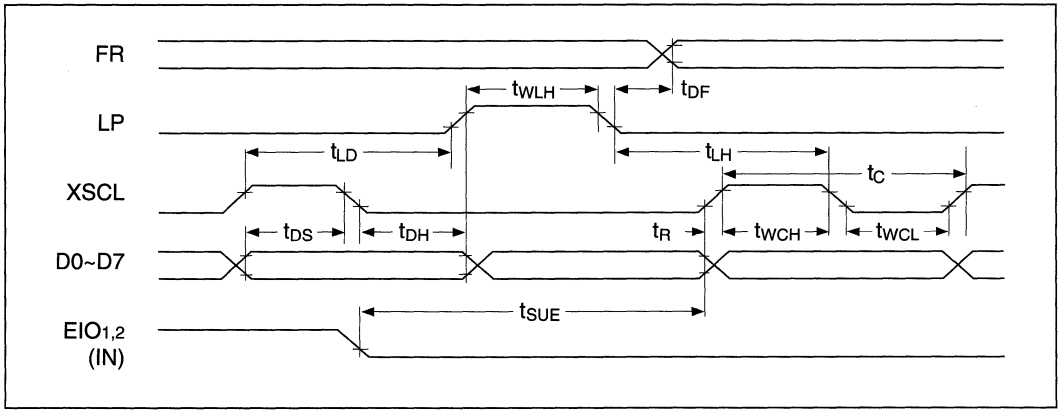
Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}	—	V_{CC}	2.7	—	5.5	V
Recommended working voltage	V0	—	V0L, VDDHL	14.0	—	40.0	V
Workable voltage	V0	Function only	V0R, VDDHL	8.0	—	42.0	V
Supply voltage (2)	V_2	Recommended value	V2L, V2R	7/9 V_0	—	V_0	V
Supply voltage (3)	V_3	Recommended value	V3L, V3R	GND	—	2/9 V_0	V
High level input voltage	V_{IH}	V_{DD}= 2.7~5.5V	EIO1, EIO2, FR D0–D7, XSCL SHL, LP, $\overline{DSPOF}$	0.8 V_{CC}	—	—	V
Low level input voltage	V_{IL}			—	—	0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC} = 2.7 – 5.5V, I_{OH} = –0.6mA	EIO1, EIO2	V_{CC}–0.4	—	—	V
Low level output voltage	V_{OL}	V_{CC} = 2.7 – 5.5V, I_{OL} = 0.6mA		—	—	0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	D0–D7, LP, FR XSCL, SHL $\overline{DSPOF}$	—	—	2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ GND	EIO1, EIO2	—	—	5.0	µA
Static current	IGND	V_0 = 14.0 – 42.0V, V_{IH} = GND, V_{IL} = GND	GND	—	—	25	µA
Output resistance	R_{SEG}	ΔV_{ON} = 0.5V Recommended condition; V_0 = +36.0V, 1/24; 01–0240		—	0.65	0.85	KΩ
		V_0 = +26.0V, 1/20; 01–0240		—	0.70	1.0	
In-chip deviation of output resistance	ΔR_{SEG}	ΔV_{ON} = 0.5V, V_0 = +36.0V, 1/24; 01–0240		—	—	95	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} = 5.38MHz, f_{LP} = 33.6KHZ, f_{FR} = 70Hz, input data: Checkered indication, no-load	V_{CC}	—	0.75	1.7	mA
		V_{CC} = +3.0V, Other conditons are the same as those when V_{CC} + 5V.		—	0.3	0.9	
Mean working current	Io	V_O = +30.0V, V_{CC} = +5.0V, V3 = +4.0V, V_2 = +26.0V, V5 = +0.0V, Other conditions are the same as those in the I_{DD} column	V_{OL}, V_{OR}	—	0.25	1.4	mA
Input terminal capacity	CI	Freq. = 1 Mhz, Ta = 25°C, Independent chips	D0–D7, LP, FR XSCL,SHL, $\overline{DSPOF}$	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

● **Working voltage range V_{CC} – V_0**

The V_0 voltage should be set up within the V_{CC} – V_0 working voltage range given below.



- **AC Characteristics**
  - **Input Timing Characteristics**



Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	*3, *5	55	—	ns
XSCL high level pulse duration	t_{WCH}	All timing signals are based on 20% and 80% of V_{CC}	20	—	ns
XSCL low level pulse duration	t_{WCL}		20	—	ns
Data setup time	t_{DS}		10	—	ns
Data hold time	t_{DH}		10	—	ns
XSCL → LP rise time	t_{LD}		0	—	ns
LP → XSCL fall time	t_{LH}		35	—	ns
LP high level pulse duration	t_{WLH}	*1	40	—	ns
		*2	35	—	ns
FR delay allowance	t_{DF}		-300	+300	ns
EIO setup time	t_{SUE}		30	—	ns
Input signal variation time	t_r, t_f	*4	—	50	ns

V_{CC} = 5.0V ± 10%, T_a = 30 to 85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	*3, *5	100	—	ns
XSCL high level pulse duration	t_{WCH}	All timing signals are based on 20% and 80% of V_{CC}	35	—	ns
XSCL low level pulse duration	t_{WCL}		35	—	ns
Data setup time	t_{DS}		15	—	ns
Data hold time	t_{DH}		10	—	ns
XSCL → LP rise time	t_{LD}		–10	—	ns
LP → XSCL fall time	t_{LH}		60	—	ns
LP high level pulse duration	t_{WLH}	*1	75	—	ns
		*2	65	—	ns
FR delay allowance	t_{DF}		-300	+300	ns
EIO setup time	t_{SUE}		40	—	ns
Input signal variation time	t_r, t_f	*4	—	50	ns

Notes: *1. The "t_{WLH}" specifies the time when the LP is at "H" and, at the same time, when XSCL is at "L", when LP is being input while the XSCL is at "L".

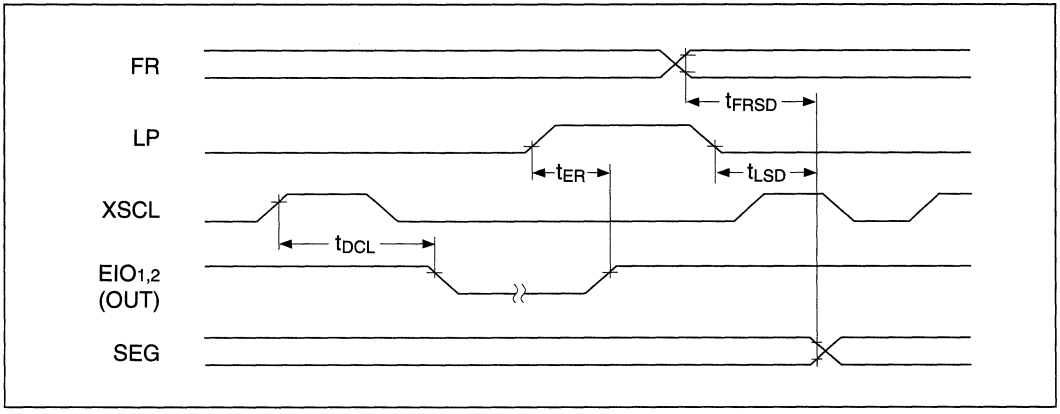
*2. The "t_{WLH}" (its definition is same as *1) when LP rises while XSCL is at "H".

*3. High speed operation of the shift clocks (XSCL) should only be made under a condition of $t_r + t_f \leq (t_C - t_{WCL} - t_{WCH})$.

*4. When making high speed data transfer using continuous shift clocks, $t_r + t_f$ of the LP signals should be up to ($t_C + t_{WCH} - t_{LD} - t_{WLH} - t_{LH}$) at the maximum.

*5. When "tc" is set to 60ns or less, "T_a" must be 55°C or less.

- **AC Characteristics**
  - **Output Timing Characteristics**



V_{CC} = 5.0V ± 10%, V_0 = +14.0 to +42.0V

Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pf (EI0)	—	120	ns
EIO output delay time	t_{DCL}		—	55	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pf (0 n)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	400	ns

V_{CC} = 2.7~4.5V, V_0 = +14.0 to +28.0V

Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pf (EI0)	—	240	ns
EIO output delay time	t_{DCL}		—	85	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pf (0 n)	—	400	ns
FR → SEG output delay time	t_{FRSD}		—	800	ns

■ LCD Driving Power Supply

● Setting up respective voltage levels

When setting up respective voltage levels for LCD drive, it is the best way to resistively divide the potential between V_0 – GND to drive the LCD by means of voltage follower using an operation amplifier.

In consideration of the case of using an operation amplifier, the LCD driving minimum potential level V5 and GND are separated and independent terminals are used.

However, since the efficacy of the LCD driving output driver deteriorates when the potential of V_5 goes up beyond the GND potential to enlarge the potential difference, always keep the potential difference of $V_5 - V_{SS}$ at 0V to 2.5V.

When a resistance exists in series in the power supply line of V_0 (GND), I_O at signal changes cause voltage drop at V_0 (GND) of the supply terminals of the LSI, disabling it to maintain the relations of the LCD with intermediate potentials of ($V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND), thus leading to breakdown or destruction of the LSI.

When using a protective resistor, do not fail to stabilize the voltage using an appropriate capacitance.

● Precautions when turning the power on and off

Since the LCD drive voltage of these LSIs is comparatively high, if a high voltage of 30V or more is applied to the LCD drive circuit with the logic operation power made floating or with the V_{CC} lowered to 2.6V or less, or when the LCD drive signals are output before applied voltage to the LCD drive circuits is stabilized, excess current flows through to possibly lead to breakdown or to destroy the LSI.

It is therefore suggested to maintain the potential of the LCD drive output to V_5 level until the LCD drive circuit voltage is stabilized, using the display off function ($\overline{DSPOFF}$).

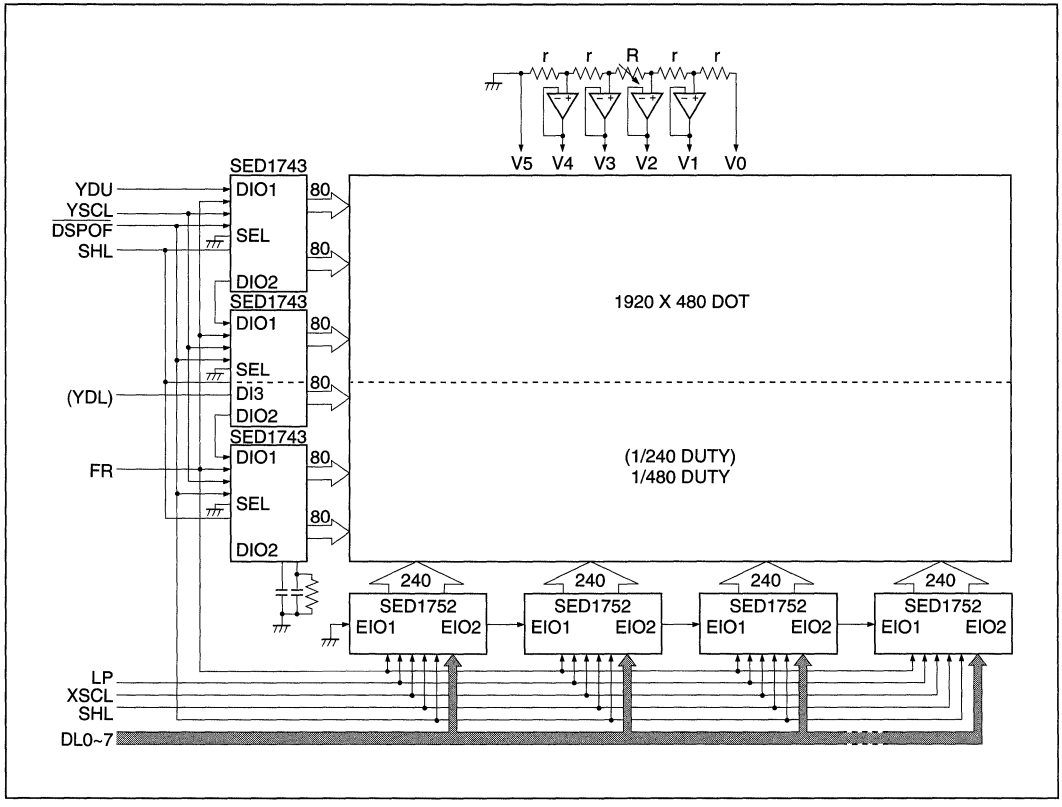
Maintain the following sequences when turning the power on and off:

- When turning the power on:
  Turn on the logic operation power → turn on the LCD drive power or turn them on simultaneously.
- When turning the power off:
  Turn off the LCD drive power → turn off the logic operation power or turn them off simultaneously.

For protection against excessive current, insert a quick melting fuse in series in the LCD drive power line. When using a protective resistor, select the optimum resistance value depending on the capacitance of the LCD cells.

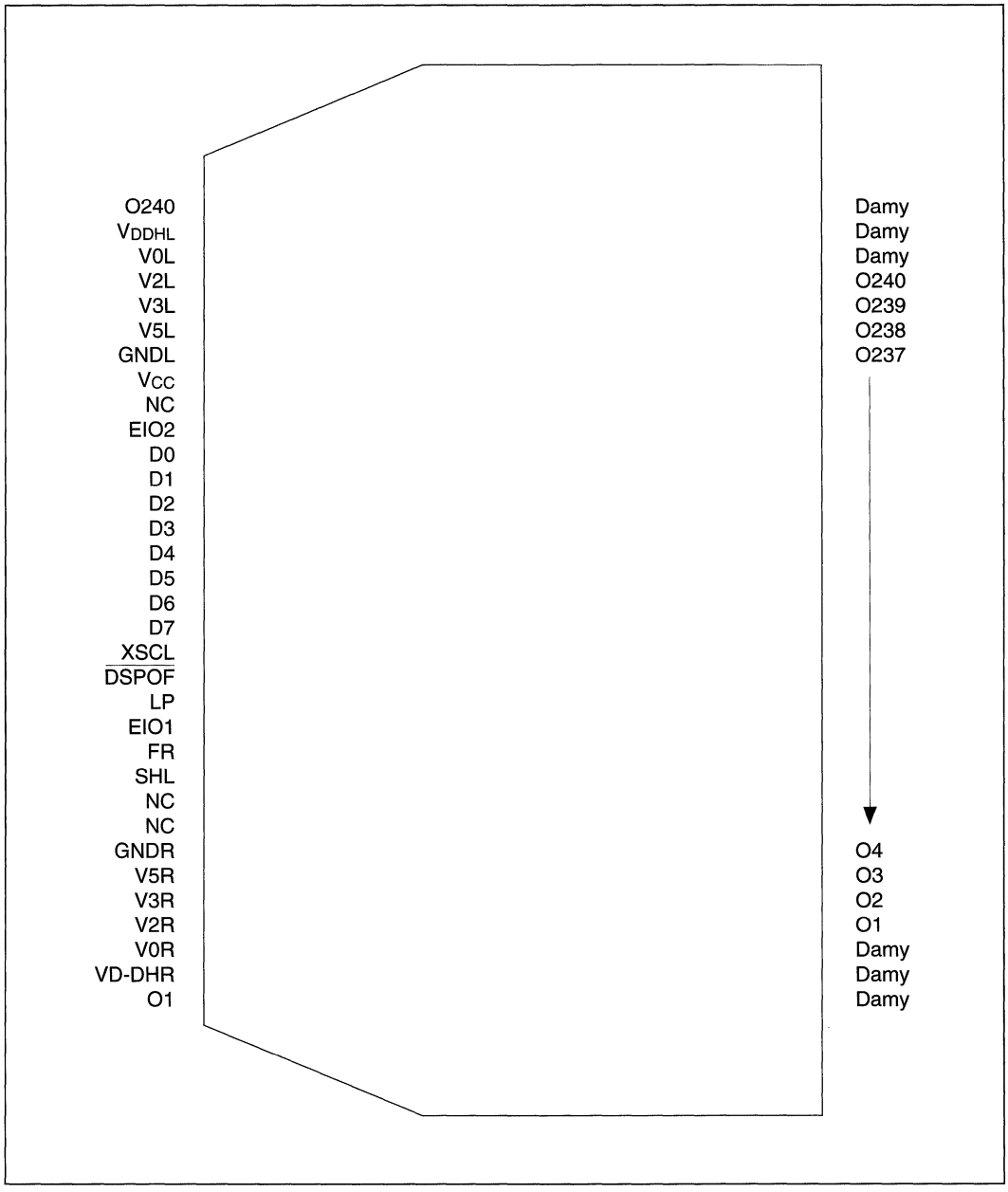
■ A Connection Example

● Block diagram of a large-plane LCD



■ SED1752T TCP Pin Arrangement Example

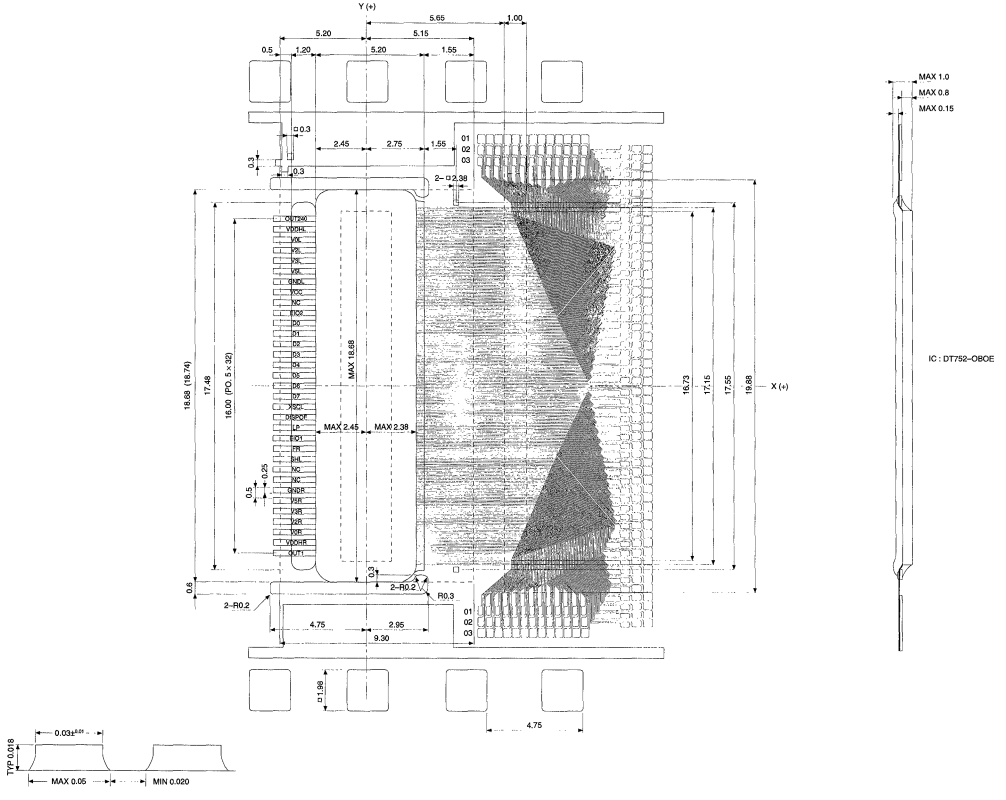
Note: This drawing is not meant to determine the contour of the TCP.



■ Dimensional Outline Drawing

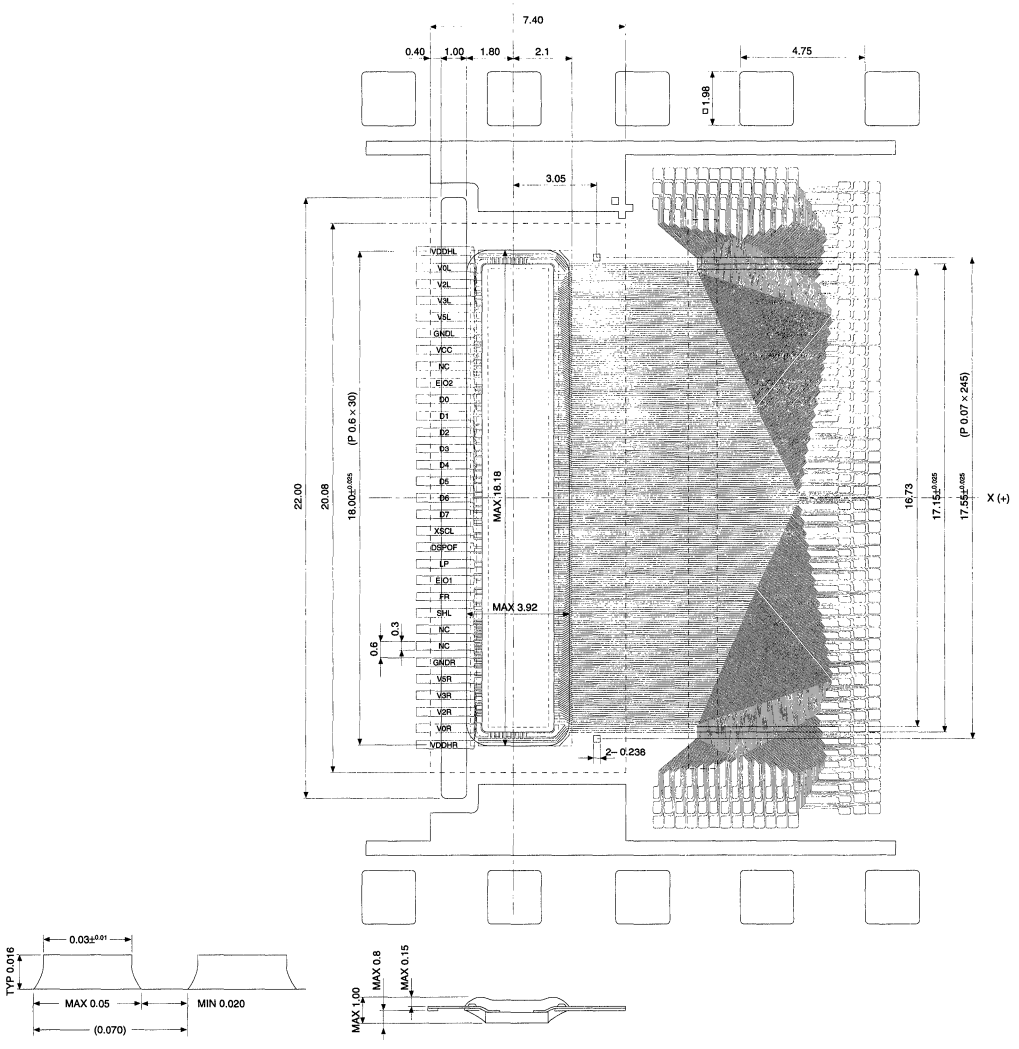
● SED1752T0A

For Reference



● SED1752T0B

For Reference



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CMOS LCD SEGMENT DRIVER

■ DESCRIPTION

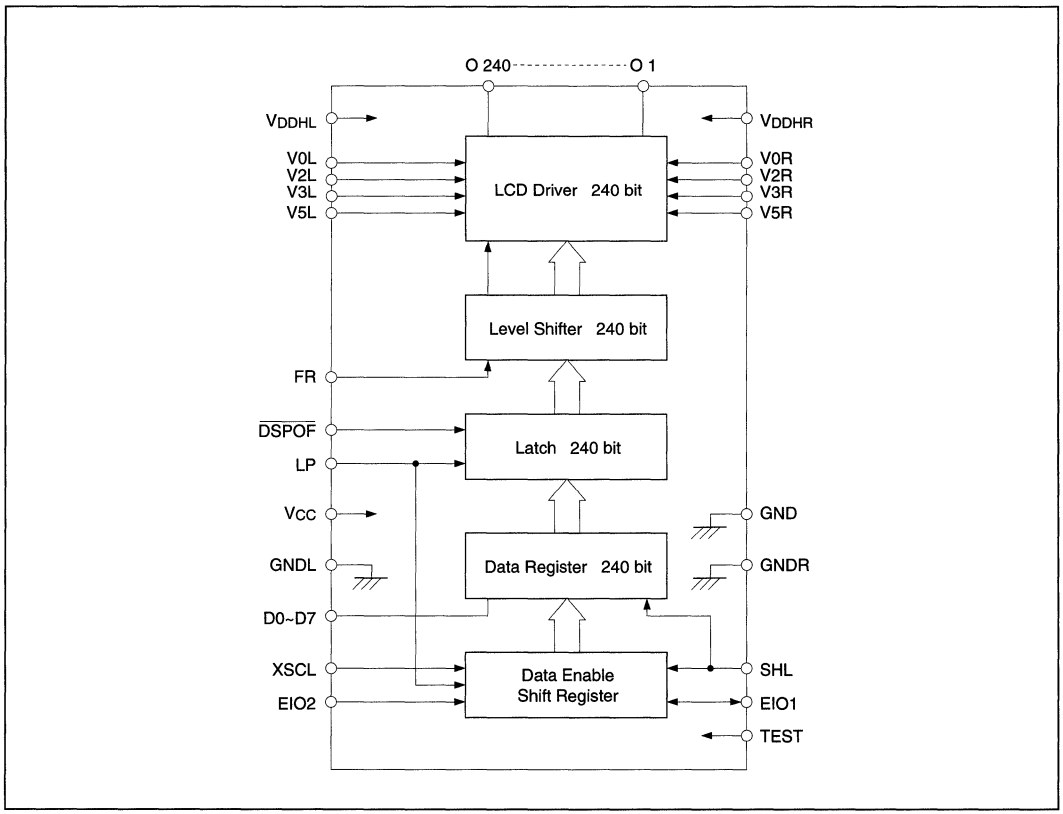
The SED1756 is an LCD segment (column) driver designed for extremely high-capacity dot-matrix liquid crystal panels. It is designed for use in conjunction with the SED1755 common (row) drivers.

The SED1756 features a wide range of liquid crystal drive voltages, LCD display of high quality, and daisy-chain enable system that decreases power consumption. It offers a wide range of applications.

■ FEATURES

- 240 LCD segment drive outputs
- Pin-selectable output shift direction
- Zero-bias display disable function
- Chip configuration long from side to side
- Adjustable LCD drive voltage relative to ground and V_{DDH}
- Liquid crystal drive in wide range of voltage: 8 to 24V
- Low-power, high-speed data transfer: 16MHz clock frequency at 5V ± 10% and 10MHz clock frequency at 3V
- 2.7 to 5.5V supply
- Chip Al pad die for C_{OG}

■ BLOCK DIAGRAM



■ BLOCK FUNCTIONS

● Enable Shift Register

The enable shift register is a bidirectional shift register which shift direction is selected by the SHL input.

The shift register output is used to store the data bus signal in the data register.

When the enable signal is disabled, the internal clock signal and data bus are fixed to "L", and it enters the power save mode.

When using multiple segment drivers, cascade connection is to be made on the EIO terminals of the drivers and the EIO terminal of the first driver is to be connected to the "GND".

The enable control circuit automatically detection that collection of the 240-bit data is completed, and automatically transmits the enable signal, so there is no need of the control signal by the control LSI.

● Data Register

This register is used for serial/parallel conversion of the data bus signal by the enable shift register output. Thus, the relation between the serial display data and the segment output is decided regardless of the shift clock inputs.

● Latch

Collects the contents of the data register at the LP fall edge trigger, and transmits the output to the level shifter.

● Level Shifter

Level interface circuit used to convert the voltage level of the signal from the logic system level to the liquid crystal drive level.

● LCD Driver

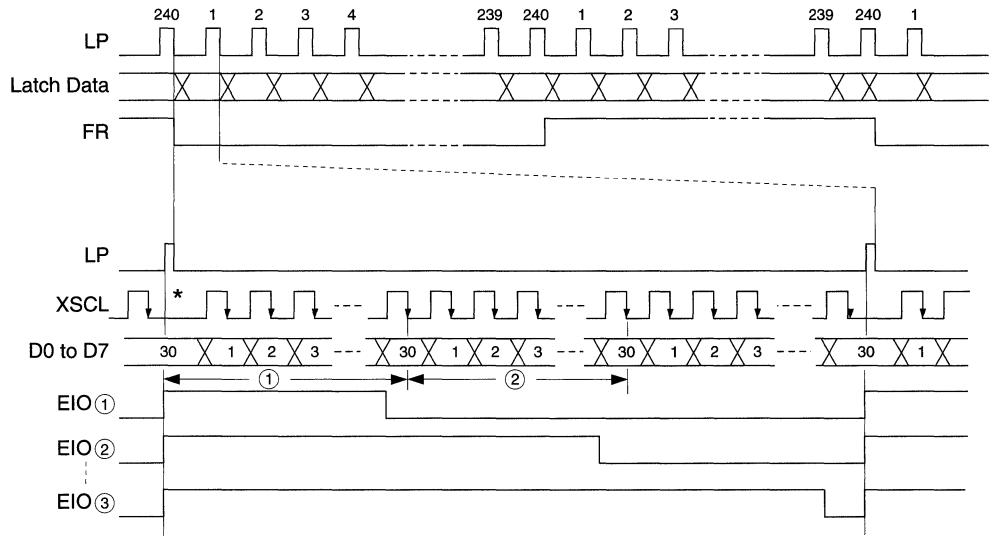
Outputs liquid crystal drive voltage.

The relation between the data bus signal, alternating signal FR, and segment output voltage is as shown below.

$\overline{DSPOF}$	Data Bus Signal	FR	Driver Output Voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_5

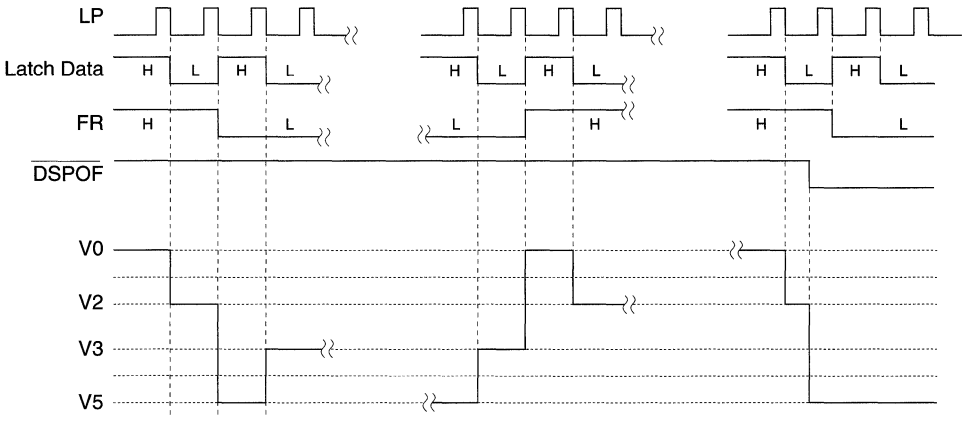
■ TIMING DIAGRAM

When it is 1/240 duty (example for reference)



① to ③ are the driver's cascade numbers.

* In high-speed data transmission, the XSCL period may need to be longer in the LP pulse insertion timing, so as to secure the LP → XSCL (t_{LH}) standard.

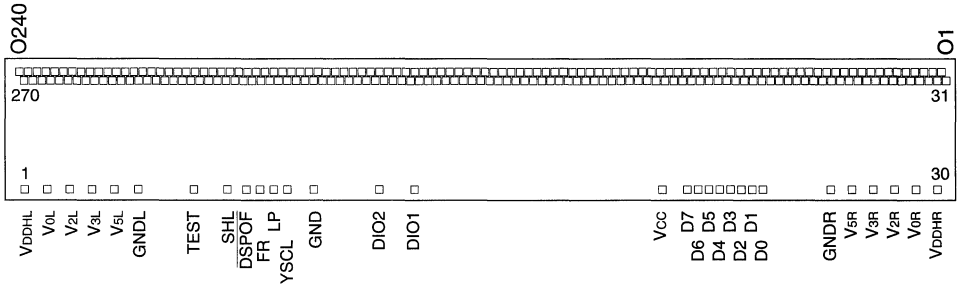


■ PIN DESCRIPTION

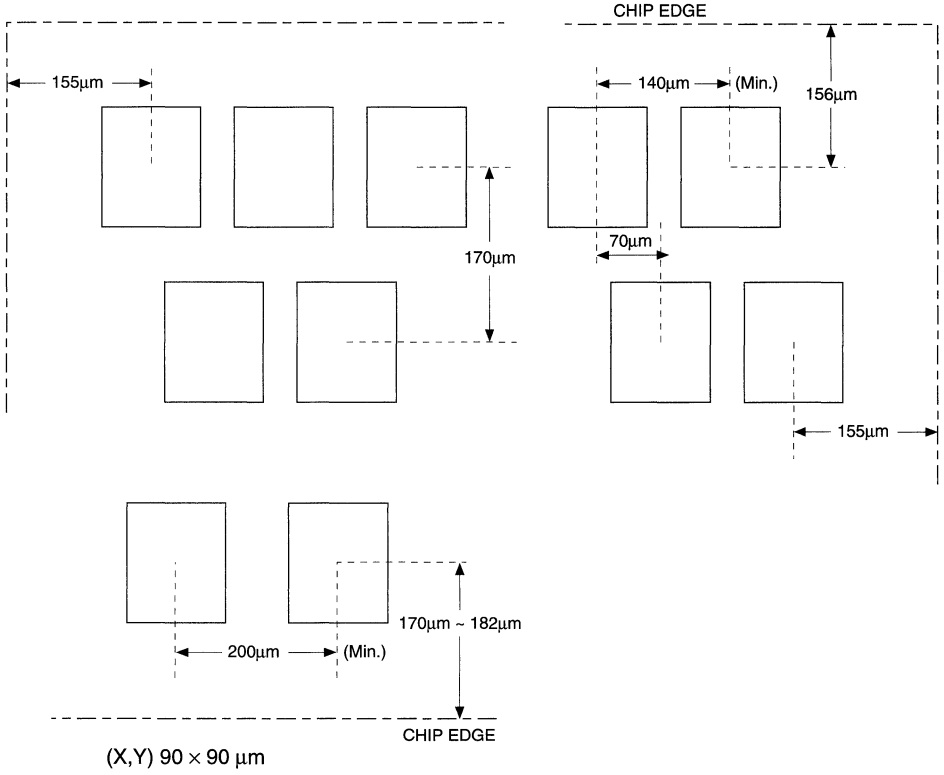
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Numbers of Pins</th></tr>
<tr><td>O 0 ~
O 240</td><td>O</td><td>Liquid crystal drive segment (column) output
The output changes at the edge of LP fall.</td><td>240</td></tr>
<tr><td>D0 ~ D7</td><td>I</td><td>Display data input</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock inpuit (Fall edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>display data latch puilse input (Fall edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable input.output
Set at input or output by the SHL input level.
Output is reset by input of LP, and automatically
falls to “L” as soon as 240 bits of data is collected.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift durection selection, and EIO terminal
input/output control input
When data is inpiut to the (D0, D1, ...D7)
terminals in sequence of (F0, F1, ...F6, F7)
(L0, L1, ...L6, L7), the relation between the data and the segmnent is as follows.
<table>
<tr><th rowspan="2">SHL</th><th colspan="8">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>240</th><th>239</th><th>238</th><th></th><th>3</th><th>2</th><th>1</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>H</td><td>L0</td><td>L1</td><td>L2</td><td>....</td><td>F5</td><td>F6</td><td>F7</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>F7</td><td>F6</td><td>F5</td><td>....</td><td>L2</td><td>L1</td><td>L0</td><td>Output</td><td>Input</td></tr>
</table>
Note: The relation between the data and shift segment output is decided regardless of the number of clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Liquid crystal drive output alternating signal input.</td><td>1</td></tr>
<tr><td>V_{CC}, GND</td><td>Power supply</td><td>Logical power supply GND: 0 V V_{CC}: +3.3, +5 V</td><td>2</td></tr>
<tr><td>V_{DDHL}, V_{DDHR}
V_{OL}, V_{OR}
V_{2L}, V_{2R}
V_{3L}, V_{3R}
V_{5L}, V_{5R}
GNDL, GNDR</td><td>Power supply</td><td>Liquid crystal drive power supply
GND: 0 V, V_{DDH}: + 14 to +42V
$V_0 \geq V_2 \geq 7/9\ V_0$
$2/9\ V_0 \geq V_3 \geq V_5 \geq$ GND</td><td></td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>Forced bias fixed input
The output is forced to the V5 level at the “L” level.</td><td>1</td></tr>
<tr><td>TEST</td><td>I</td><td>Non Connect</td><td>1</td></tr>
</table>

sTotal 182

■ PAD DIMENSIONS



Chip Size : 17.04mm × 2.30mm
Chip Thickness : 400µm (Typ.)



(X,Y) 90 × 90 µm

■ PAD COORDINATES

Pad No.	Pad Name	X	Y
1	V_{DDHL}	–8295	–980
2	V_{OL}	–7895	–968
3	V_{2L}	–7495	–968
4	V_{3L}	–7095	–968
5	V_{5L}	–6695	–980
6	GNDL	–6295	–980
7	TEST	–5095	–980
8	$\overline{SHL}$	–4495	–980
9	$\overline{DSPOF}$	–4095	–980
10	FR	–3895	–980
11	LP	–3695	–980
12	XSCL	–3495	–980
13	GND	–3095	–980
14	EIO2	–1895	–980
15	EIO1	–1295	–980
16	V_{CC}	3295	–980
17	D7	3695	–980
18	D6	3895	–980
19	D5	4095	–980
20	D4	4295	–980
21	D3	4495	–980
22	D2	4695	–980
23	D1	4895	–980
24	D0	5095	–980
25	GNDR	6295	–980
26	V_{5R}	6695	–980
27	V_{3R}	7095	–968
28	V_{2R}	7495	–968
29	V_{0R}	7895	–968
30	V_{DDHR}	8295	–980

Pad No.	Pad Name	X	Y
31	O1	8365	824
32	O2	8295	994
33	O3	8225	824
34	O4	8155	994
35	O5	8085	824
36	O6	8015	994
37	O7	7945	824
38	O8	7875	994
↓	↓	↓	↓
263	0233	–7875	824
264	0234	–7945	994
265	0235	–8015	824
266	0236	–8085	994
267	0237	–8155	824
268	0238	–8225	994
269	0239	–8295	824
270	0240	–8365	994

X of On : 8435– (70×n) µm

Y of On : n = odd 824 µm
n = even 994 µm

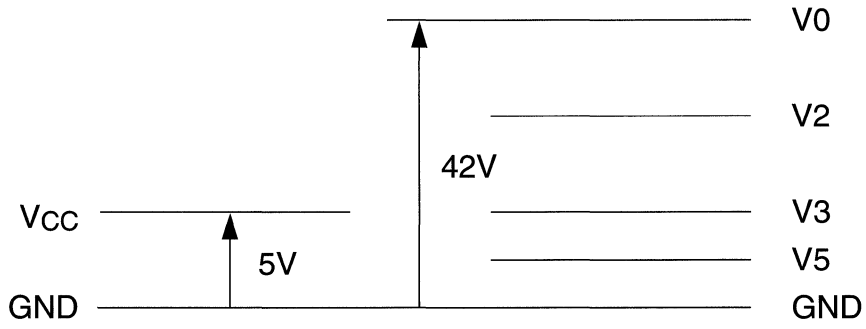
■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameters	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 ~ +7.0	V
Supply voltage (1)	V	–0.3 ~ +45.0	V
Supply voltage (3)	V_0, V_2, V3, V_5	GND–0.3 ~ V +0.3	V
Input voltage	V_I	GND–0.3 ~ V_{CC} +0.3	V
Output voltage	V_O	GND–0.3 ~ V_{CC} +0.3	V
EIO output current	I_O	20	mA
Working temperature	Topr	–40 ~ +85	°C
Storage temperature 1	Tstg1	–65 ~ +150	°C

Note 1: All stated voltages assume that GND = 0V.

Note 2: V0, V2, V3 voltages shall always maintain the condition of V0 ≥ V2 ≥ V3 ≥ V5 ≥ GND.



Note 3: Avoid floating status of the logical power supply during application of liquid crystal drive power, or fall of the power below V_{CC} = 2.6V; the LSI may be destroyed permanently. Special notice is required for the power sequence when turning on or off the system power.

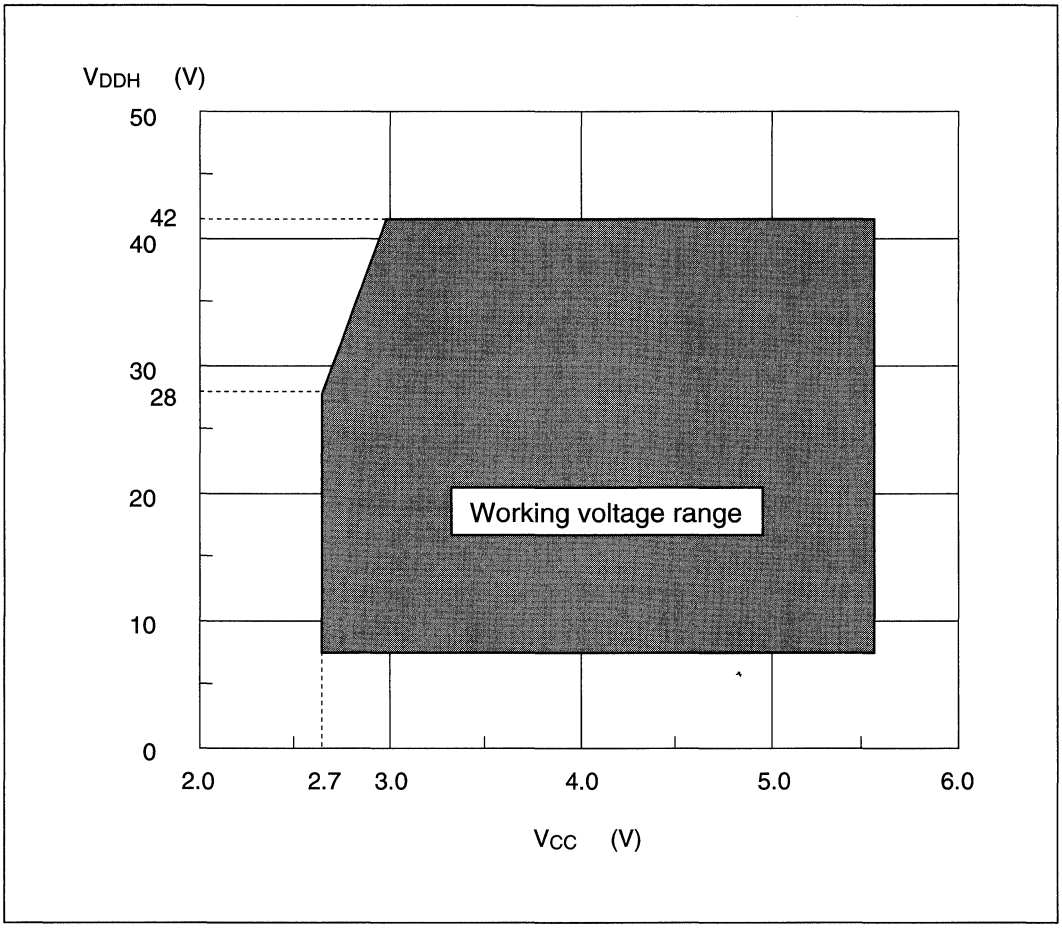
● DC Characteristics

Unless otherwise specified, GND = V_5 = 0V, V_{CC} = +5.0V ± 10%, T_a = –40 to 85°C

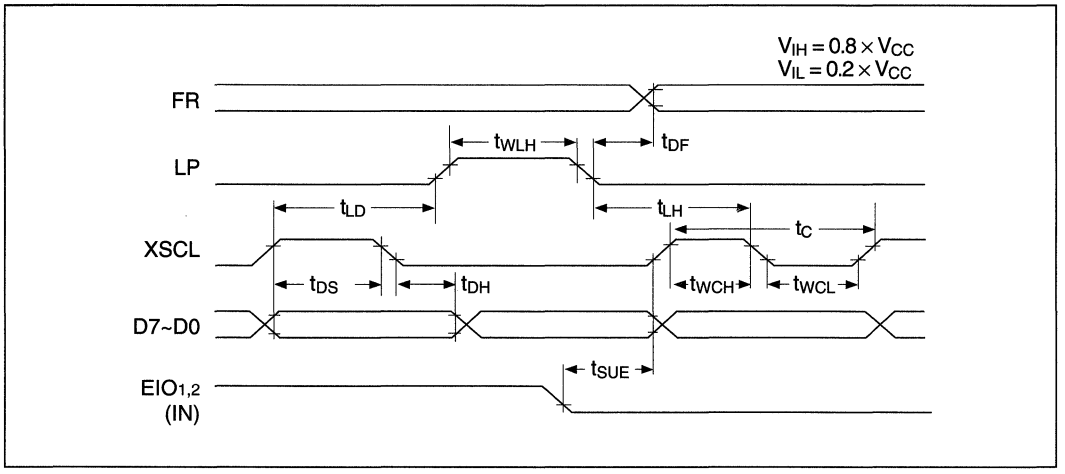
Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}	—	V_{CC}	2.7	5.0	5.5	V
Recommended working voltage	V_{DDH}	VCC = 2.7 to 5.5 V	$V_{DDH}L$, V_{DDHR}	14.0	—	40.0	V
Workable voltage	V_{DDH}	Function only	V_{0L}, V_{OR}	8.0	—	42.0	V
Supply voltage (2)	V_2	Recommended value	V2L, V2R	7/9 V_{DDH}	—	V_{DDH}	V
Supply voltage (3)	V_3	Recommended value	V3L, V3R	GND	—	2/9 V_{DDH}	V
High level input voltage	V_{IH}	V_{CC}= 2.7~ 5.5V	EIO1, EIO2, FR D0–D7, XSCL SHL, LP, DSPOF	0.8 V_{CC}	—	—	V
Low level input voltage	V_{IL}			—	—	0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC} = 2.7 – 5.5V, I_{OH} = –0.6mA	EIO1, EIO2	V_{CC}–0.4	—	—	V
Low level output voltage	V_{OL}	V_{CC} = 2.7 – 5.5V, I_{OL} = 0.6mA		—	—	GND+0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	D0–D7, LP, FR XSCL, SHL DSPOF	—	—	2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}	EIO1, EIO2	—	—	5.0	µA
Rest current	I_{GND}	V_0 = 14.0 – 42.0V, V_{IH} = V_{CC}, V_{IL} = GND	GND	—	—	25	µA
Output resistance	R_{SEG}	ΔVON = 0.5V Recommended condition: V_0 = +36.0V, 1/24	01–0240	—	0.9	1.4	KΩ
		V_0 = +26.0V, 1/20		—	1.0	1.5	
Output resistance In-chip deviation	ΔR_{SEG}	ΔVON = 0.5V, V_0 = +36.0V, 1/24	01–0240	—	—	95	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} = 5.38MHz, f_{LP} = 33.6KHZ, f_{FR} = 70Hz, input data: check display, no-load	V_{CC}	—	0.75	1.7	mA
		V_{CC} = +3.0V, Other conditons are the same as those when V_{CC} + 5V.		—	0.3	0.9	
Mean working current consumption (2)	I_{DDH}	V_0 = +30.0V, V_{CC} = +5.0V, V3 = +4.0V, V_2 = +26.0V, V5 = +0.0V, Other conditions are the same as those in the I_{CC} column	V_{DDHL}, V_{DDHR}	—	0.25	1.4	mA
Input terminal capacity	CI	Freq. = 1 Mhz, Ta = 25°C, Independent chips	D0–D7, LP, FR XSCL,SHL, DSPOF	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

● **Operation Voltage Range V_{CC} – V_{DDH}**

The V_{DDH} voltatge must be set within the following V_{CC} – V_{DDH} operation voltage range.



- **AC Characteristics**
  - **Input Timing**



V_{CC} = 5.0V ± 10%, Ta = –40 to 85°C

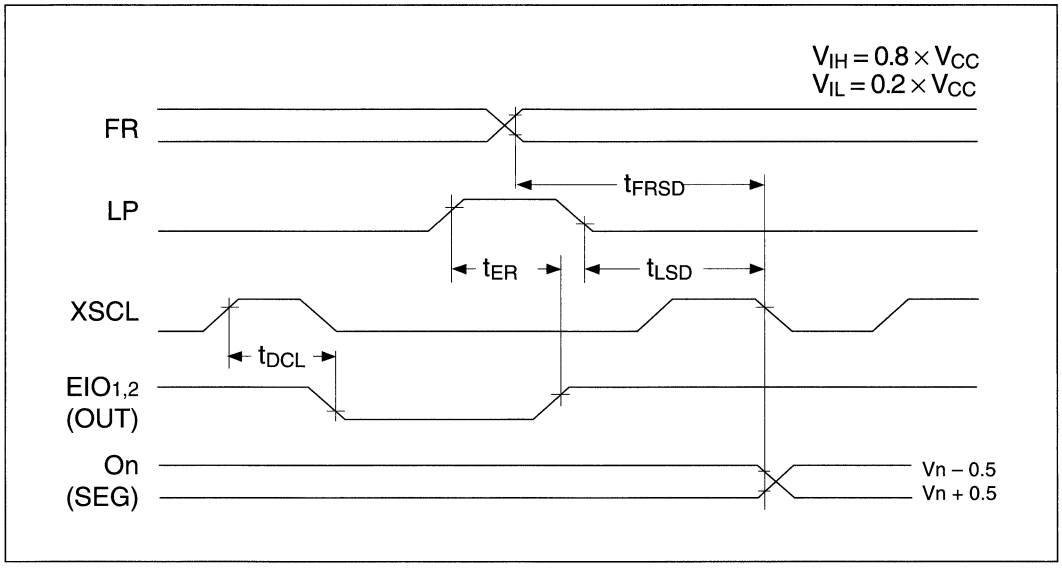
Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	—	62	—	ns
XSCL high level pulse duration	t_{WCH}	—	20	—	ns
XSCL low level pulse duration	t_{WCL}	—	20	—	ns
Data setup time	t_{DS}	—	15	—	ns
Data hold time	t_{DH}	—	10	—	ns
XSCL → LP rise time	t_{LD}	—	–5	—	ns
LP → XSCL fall time	t_{LH}	—	40	—	ns
LP high level pulse width	t_{WLH}	*1	35	—	ns
EIO setup time	t_{SUE}	—	15	—	ns

V_{CC} = 2.7 to 4.5V, Ta = –40 to 85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	V_{CC} = 2.7V	115	—	ns
		V_{CC} = 3.0V	100	—	
XSCL high level pulse duration	t_{WCH}	—	35	—	ns
XSCL low level pulse duration	t_{WCL}	—	35	—	ns
Data setup time	t_{DS}	—	20	—	ns
Data hold time	t_{DH}	—	10	—	ns
XSCL → LP rise time	t_{LD}	—	–5	—	ns
LP → XSCL fall time	t_{LH}	V_{CC} = 2.7V	75	—	ns
		V_{CC} = 3.0V	65	—	
LP high level pulse width	t_{WLH}	V_{CC} = 2.7V *1	75	—	ns
		V_{CC} = 3.0V *1	65	—	
EIO setup time	t_{SUE}	V_{CC} = 2.7V	30	—	ns
		V_{CC} = 3.0V	25	—	

*1.
- t_{WLH} prescribes the LP "H" and XSCL "L" time, when LP is input during the "L" period of XSCL.
- t_{WLH} when LP rises from the XSCL "H" period (the definition is the same as the above *1)
- It is limited to $t_r + t_{rf} \leq (t_C - t_{WCL} - t_{WCH})$, when the shift clock (XSCL) is operated in high-speed mode.
- When high-speed data transmission is done with continous shift clock, the maximum of the LP signal $t_r + t_f$ is $(t_C + t_{WCH} - t_{LD} - t_{WLH} - t_{LH})$.

- **AC Characteristics**
  - **Output Timing**



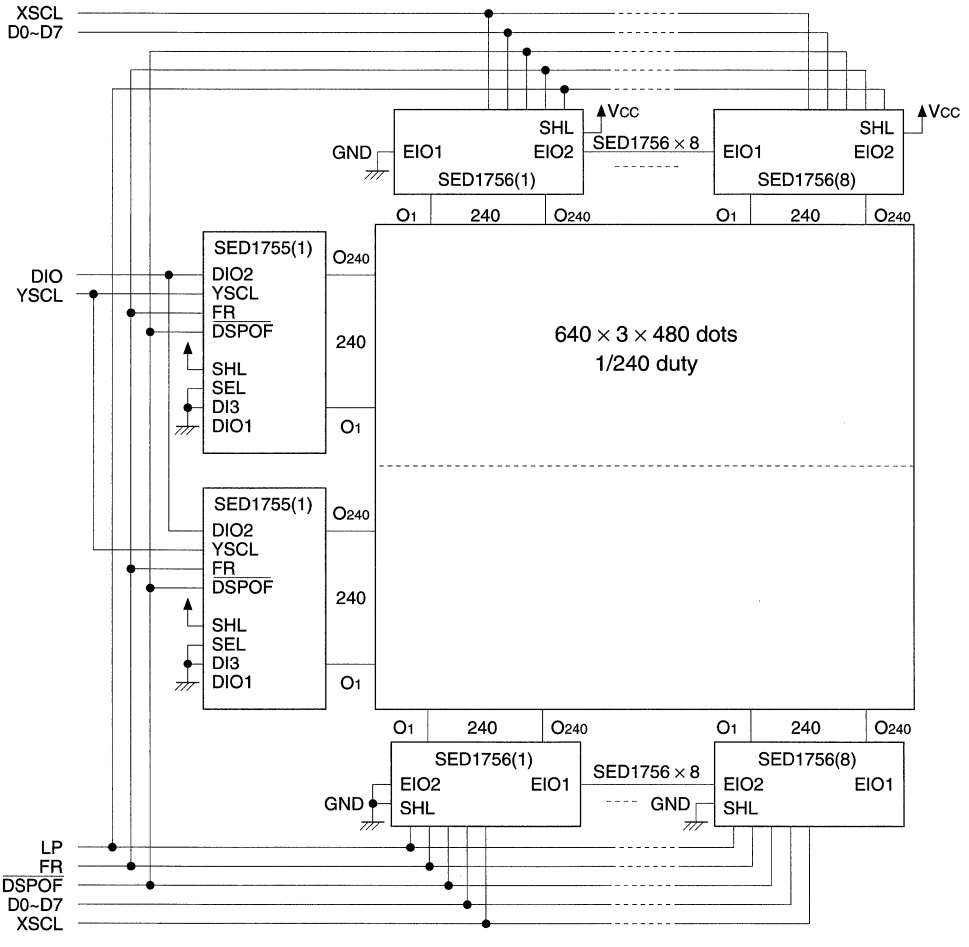
V_{CC} = 5.0V ± 10%, V_{DDH} = 14.0 to 42.0V, Ta = –40 to 85°C

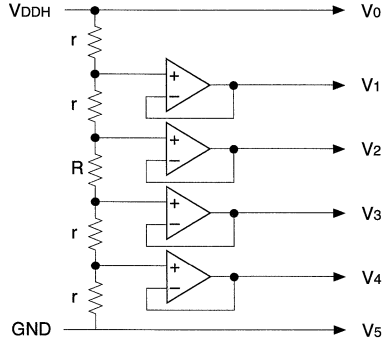
Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EIO)	—	90	ns
EIO output delay time	t_{DCL}		—	50	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (On)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	300	ns

V_{CC} = 2.7 to 4.5V, V_{DDH} = 14.0 to 28.0V, Ta = –40 to 85°C

Parameter	Symbol	Conditions		Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EIO)		—	240	ns
EIO output delay time	t_{DCL}		V_{CC} = 2.7V	—	85	ns
			V_{CC} = 3.0V	—	75	
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (On)		—	400	ns
FR → SEG output delay time	t_{FRSD}			—	600	ns

■ FOR REFERENCE





LOW-POWER 160-BIT LCD SEGMENT DRIVER

■ DESCRIPTION

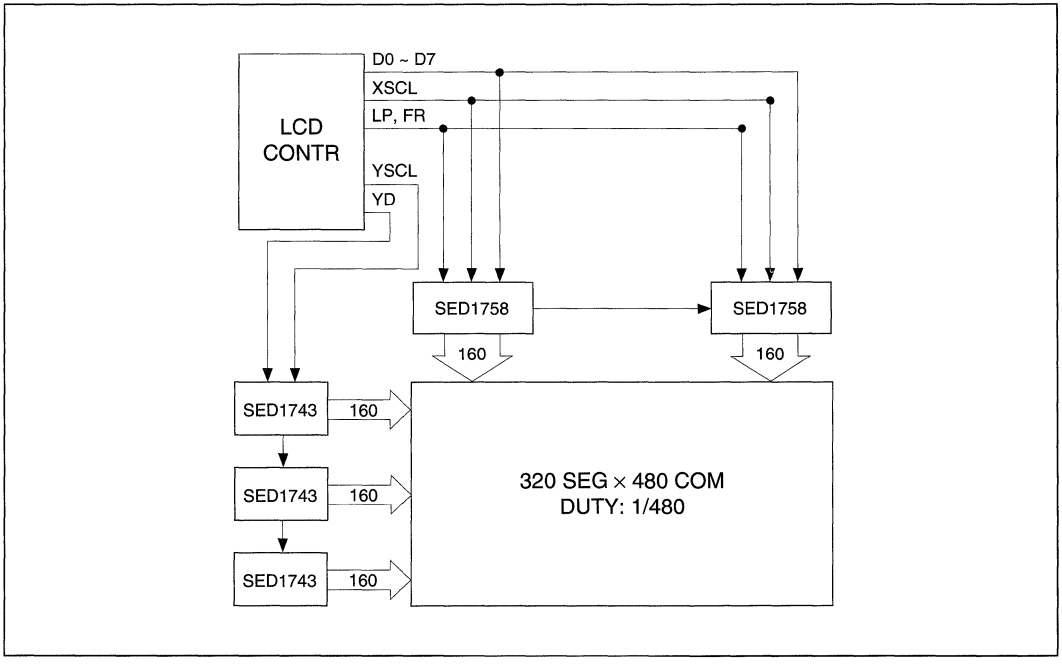
The SED1758 is a 160-bit dot matrix LCD segment (column) driver for driving high-resolution color STN LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of the LCD drive voltages. The device uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1758 is used in conjunction with the SED1743 (160-bit common driver) to drive a large-capacity dot matrix LCD panel.

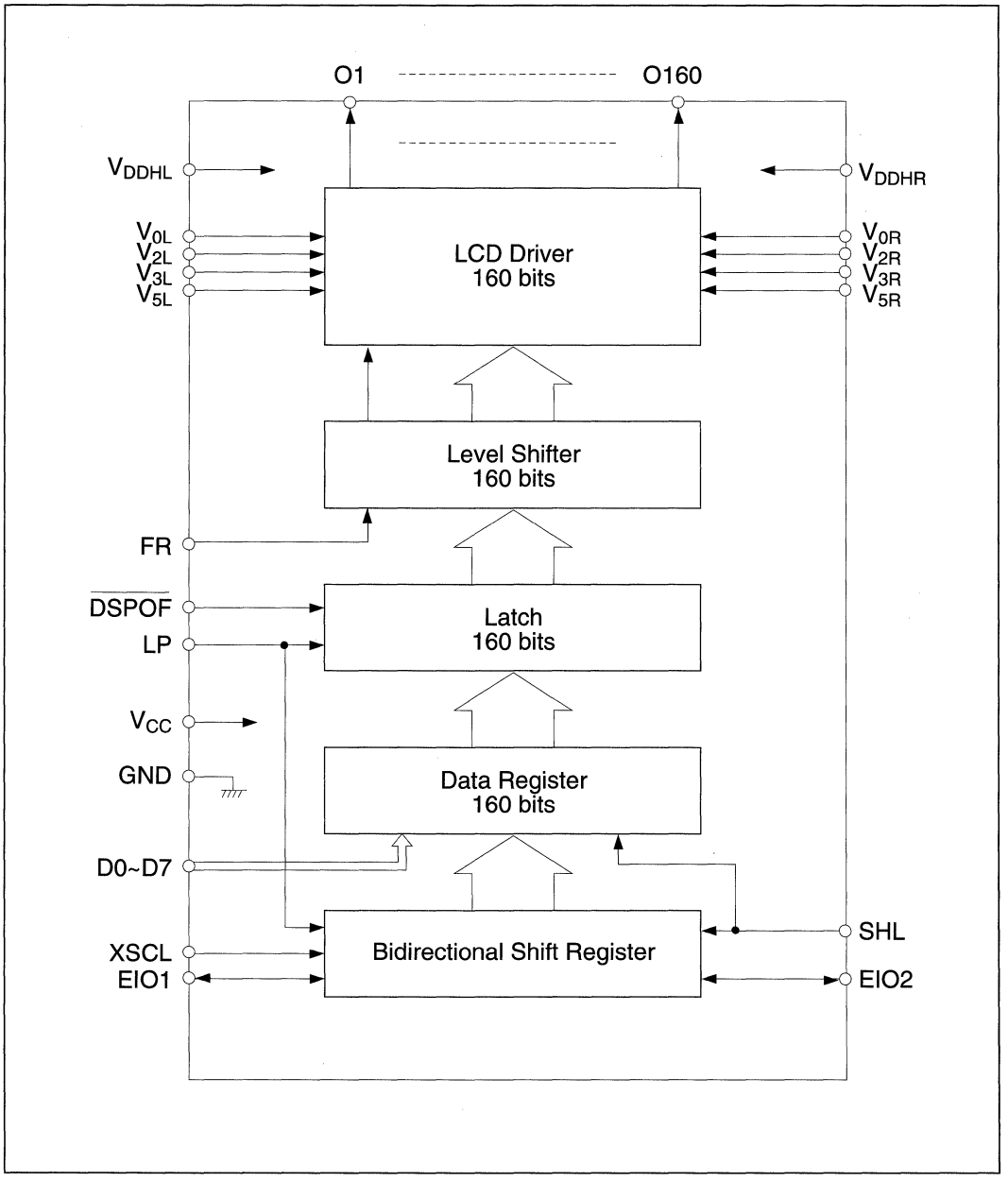
■ FEATURES

- Low-power, high-speed CMOS technology
- 160-bit segment (column) driver
- High-speed 8-bit data bus
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Unbiased display off function
- Adjustable offset bias of the LCD according to V_{DDH} and GND
- Shift clock frequency . 16MHz max at V_{DD} = 5V
- Ability to adjust offset bias of the LCD source from V_{DD}
- High-speed daisy chain enable support
- Adjustable offset bias of the liquid crystal according to the V_{DDH} and GND
- LCD voltage ..... 8 to 42V
- Supply voltage ..... 2.7 to 5.5V
- Package
  - T0A ..... Slim TAB (9.3mm)
  - T0B ..... Bending TAB
  - T0G ..... Ultra slim TAB (7.3mm)

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Enable Shift Register

The enable shift register is a bidirectional shift register where the direction of the shift is selected by the SHL input. The output of this shift register is used to store the data bus signals in the data register.

When the enable signal is in a disable state, the internal clock signal and data bus are fixed at "L", placing the chip in power save mode.

When multiple segment drivers are used, the EIO terminals of the various drivers are cascade connected and the EIO terminal of the first driver is connected to GND. (See the example of connection, below.)

The enable control circuit automatically senses when 160 bits worth of data have been received, and sends the enable signal, thus eliminating the need for a control signal from the control LSI.

● Data Register

This is a register to convert the data bus signal from serial to parallel using the output of the enable shift register. Consequently, the relationships between the serial display data and the segment output is determined independently of the shift clock input number.

● Latch

The latch receives the contents of the data registers when triggered by the falling edge of the LP, and outputs them to the level shifter.

● Level Shifter

The level shifter is a level interface circuit which converts the signal voltage level from a logic circuit level to the LC driver voltage level.

● LCD Driver

The LCD driver outputs the LC drive voltage.

The relationship between the data bus signal, the AC signal FR, and the segment output voltage is as follows:

$\overline{\text{DSPOFF}}$	Data Bus Signal	FR Voltage	Driver $\overline{O}$ Voltage
H	H	H	V0
		L	V5
	L	H	V2
		L	V3
L	—	—	V5

■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>O0 to O160</td><td>O</td><td>Segment (column) output to drive LC.
Output transition occurs on falling edge of LP.</td><td>160</td></tr>
<tr><td>D0 to D7</td><td>I</td><td>Display data input.</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (triggers on falling edge)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (triggers on falling edge)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O
This is set to input or output depending on the level of the SHL input. The output is reset by the LP input, and once the 160-bit data reception is complete, the terminals automatically fall to “L”.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and EIO terminal I/O control pin.
When the data has been input to terminals (D0, D1, ..., D7) in the order (a0, a1, ..., a6, a7) (b0, b1, ..., b6, b7) ... (t0, t1, ..., t6, t7), the relationship between the data and the segment output is as shown in the table below:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>O1</th><th>O2</th><th>O3</th><th></th><th>O158</th><th>O159</th><th>O160</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a7</td><td>a6</td><td>a5</td><td>...</td><td>t2</td><td>t1</td><td>t0</td><td>I</td><td>O</td></tr>
<tr><td>H</td><td>t0</td><td>t1</td><td>t2</td><td>...</td><td>a5</td><td>a6</td><td>a7</td><td>O</td><td>I</td></tr>
</table>
Note: The relationship between the data and the segment output is independent of the shift clock number.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC drive output AC signal input</td><td>1</td></tr>
<tr><td>VCC, GND</td><td>Power</td><td>Power source for logic: GND : 0V VCC : +3.3, +5V</td><td>2</td></tr>
<tr><td>VDDHL, VOL, V2L, V3L, V5L, VDDHR, VOR, V2R, V3R, V5R</td><td>Power</td><td>LC drive circuit power:
GND : 0V VDDH: +14 to +42V
VDDH ≥ V0 ≥ V2 ≥ 7/9 × V0
2/9 × V0 ≥ V3 ≥ V5 ≥ GND</td><td>10</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>Forced bias set input.
“L” level input forces the bias to the V5 level.
* When this function is used, it cannot be used in combination with the SED1703.</td><td>1</td></tr>
</table>

Total: 187

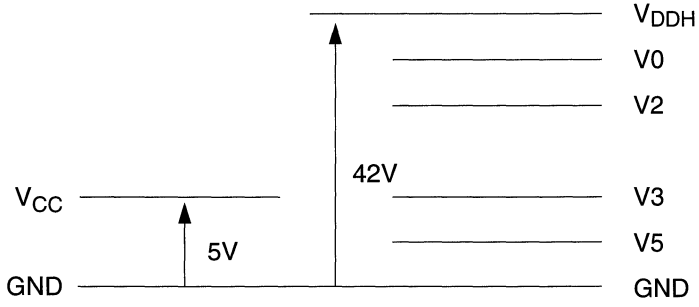
■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Power voltage (1)	V_{CC}	–0.3 to +7.0	V
Power voltage (2)	V_{DDH}	–0.3 to +45.0	V
Power voltage (3)	V0, V2, V3, V5	GND – 0.3 to V_{CC} + 0.3	V
Input voltage	VI	GND – 0.3 to V_{CC} + 0.3	V
Output voltage	VO	GND – 0.3 to V_{CC} + 0.3	V
EIO output current	IO1	20	mA
Operating temperature	T_{OPR}	–30 to +85	°C
Storage temperature 1	T_{STG1}	–65 to +150	°C
Storage temperature 2	T_{STG2}	–55 to +100	°C

Notes:

1. All voltages are given relative to GND = 0V.
2. Storage temperature 1 is the recommendation for the chip itself, and storage temperature 2 is the recommendation for the chip mounted on a TCP.
3. Ensure that the relationship between V0, V2, V3 and V5 is always as follows: $V_{DDH} \geq V0 \geq V2 \geq V3 \geq V5 \geq GND$.



4. The LSI may be permanently damaged if the logic system power is floating or V_{CC} is less than or equal to 2.6V when power is applied to the LC drive circuit system. Special caution must be paid to the power sequences when turning the power on and off.

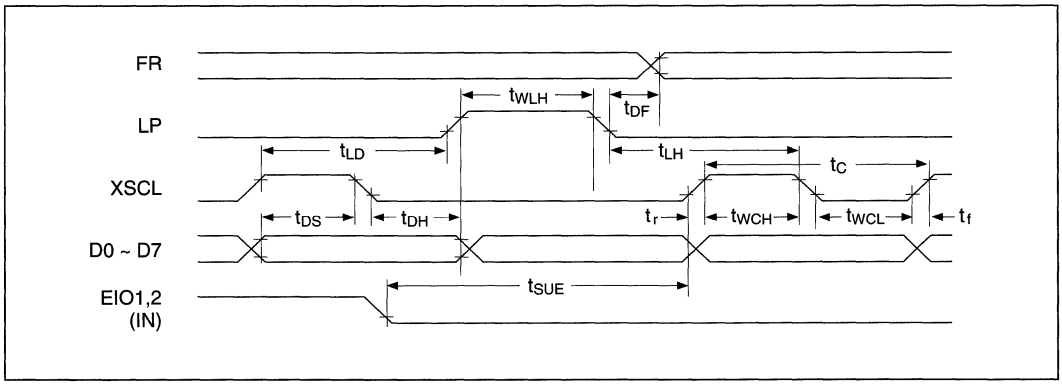
● DC Electrical Characteristics

Unless otherwise specified, GND = V5 = 0V,
V_{CC} = +5.0V ±10%, T_a = –30 to +85°C

Parameter	Symbol	Conditions		Applicable Pins	Min	Typ	Max	Unit
Power voltage (1)	V_{CC}			V_{CC}	2.7	—	5.5	V
Recommended operating voltage	V0			V_{OL}, V_{DDHL} V_{OR}, V_{DDHR}	14.0	—	40.0	V
Possible operating voltage	V0	Function			8.0	—	42.0	V
Power voltage (2)	V2	Recommended value		V2L, V2R	7/9 × V0	—	V0	V
Power voltage (3)	V3	Recommended value		V3L, V3R	GND	—	2/9 × V0	V
High-level input voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		EIO1, EIO2, FR, D0 ~ D7, XSCL, SHL, LP, DSPOFF	0.8 × V_{CC}	—	—	V
Low-level input voltage	V_{IL}				—	—	0.2 × V_{CC}	V
High-level output voltage	V_{OH}	V_{CC} = 2.7 to 5.5V	I_{OH} = –0.6mA	EIO1, EIO2	V_{CC} – 0.4	—	—	V
Low-level output voltage	V_{OL}		I_{OL} = 0.6mA		—	—	0.4	V
Input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		D0 ~ D7, LP, FR, XSCL, SHL, DSPOFF	—	—	2.0	µA
I/O leakage current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		EIO1, EIO2	—	—	5.0	µA
Static current	I_{GND}	V0 = 14.0 to 42.0V, V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Output resistance	R_{SEG}	ΔVON = 0.5V Recommended value	V0 = +36.0V, 1/24	O1 ~ O160	—	0.85	2.6	KΩ
			V0 = +26.0V, 1/20		—	0.90	2.6	
Output resistance deviation within the chip	ΔR_{SEG}	ΔVON = 0.5V V0 = +36.0V, 1/24		O1 ~ O160			90	Ω
Average operating consumption current (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} = 5.38MHz, f_{LP} = 33.6KHz, f_{FR} = 70Hz; Input data: checker pattern display, no load		V_{CC}	—	0.5	1.1	mA
		V_{CC} = +3.0V; other parameters are the same as for V_{CC} = 5V			—	0.2	0.6	mA
Average operating consumption current (2)	I_O	V0 = +30.0V, V_{CC} = +5.0V, V3 = +4.0V, V2 = +26.0V, V5 = 0.0V; other parameters are the same as for the I_{CC} item		V0	—	0.15	0.9	mA
Input terminal capacitance	C_I	Freq. = 1MHz, T_a = 25°C, Chip alone		D0 ~ D7, LP, FR, XSCL, SHL, DSPOFF	—	—	8	pF
I/O terminal capacitance	$C_{I/O}$			EIO1, EIO2	—	—	15	pF

● AC Characteristics

○ Input Timing Characteristics



V_{CC} = 5.0V ± 10%, T_a = –30 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
XSCL frequency	tC	tr, tf ≤ 11ns *3	62	—	ns
XSCL high-level pulse width	tWCH	—	20	—	ns
XSCL low-level pulse width	tWCL	—	20	—	ns
Data setup time	tDS	—	10	—	ns
Data hold time	tDH	—	10	—	ns
XSCL → LP rising edge	tLD	—	–5	—	ns
LP → XSCL falling edge	tLH	—	30	—	ns
LP high-level pulse width	tWLH	*1	40	—	ns
		*2	35	—	ns
Allowable FR delay	tDF	—	–300	+300	ns
EIO setup time	tSUE	—	30	—	ns
Input signal conversion time	tr, tf	*4	—	50	ns

V_{CC} = 2.7 to 4.5V, T_a = –30 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
XSCL frequency	tC	tr, tf ≤ 15ns *3	100	—	ns
XSCL high-level pulse width	tWCH	—	35	—	ns
XSCL low-level pulse width	tWCL	—	35	—	ns
Data setup time	tDS	—	15	—	ns
Data hold time	tDH	—	10	—	ns
XSCL → LP rising edge	tLD	—	–10	—	ns
LP → XSCL falling edge	tLH	—	60	—	ns
LP high-level pulse width	tWLH	*1	75	—	ns
		*2	65	—	ns
Allowable FR delay	tDF	—	–300	+300	ns
EIO setup time	tSUE	—	40	—	ns
Input signal conversion time	tr, tf	*4	—	50	ns

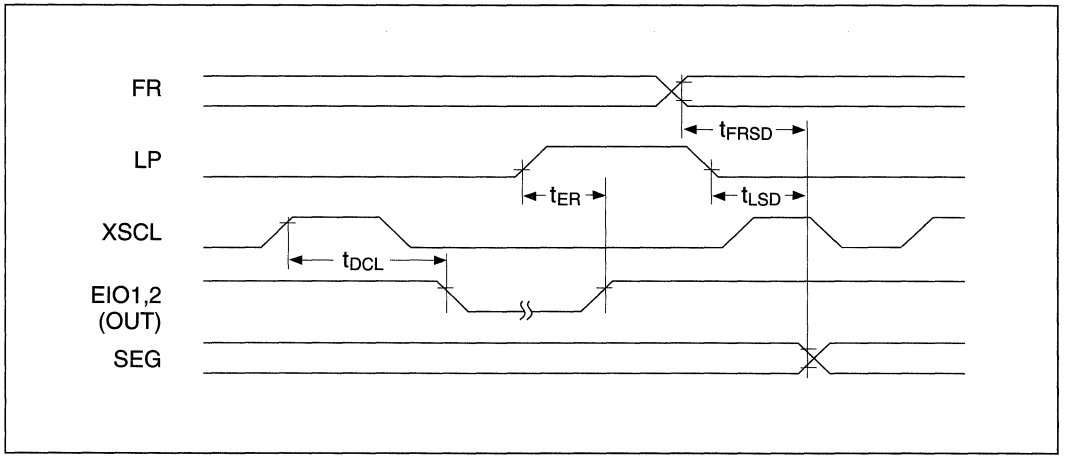
Notes: *1. t_{WLH} indicates the time when LP is "H" and XSCL is "L" when LP is input during the interval when XSCL is "L".

*2. t_{WLH} when LP rises beginning during the interval when XSCL is "H" (where the definition is the same as in "*1").

*3. When the shift clock (XSCL) is set to high-speed operation, the constraint that follows holds true:
$t_r + t_f \leq (t_C - t_{WCL} - t_{WCH})$.

*4. During high-speed data transfer with continuous shift clock, the maximum LP signal tr + tf is
$(t_C + t_{WCH} - t_{LD} - t_{WLH} - t_{LH})$.

○ Output Timing Characteristics



V_{CC} = +5.0V ± 10%, V0 = +14.0 to +42.0V

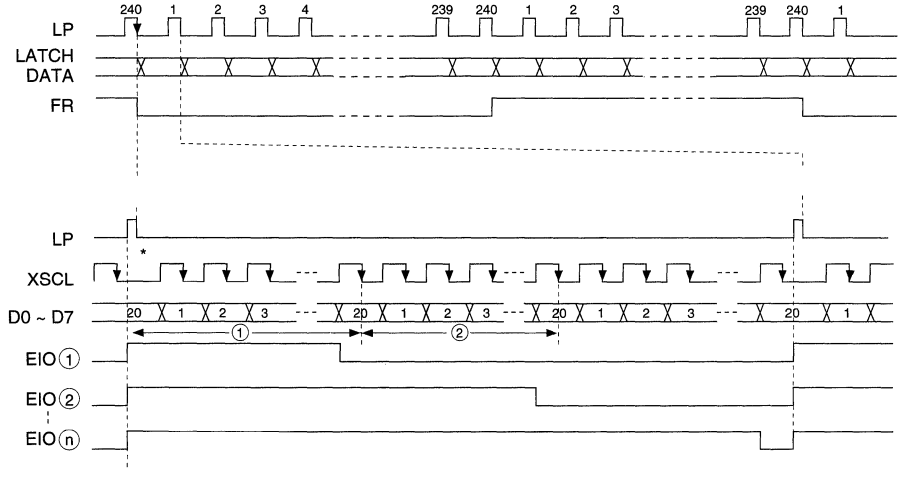
Parameter	Symbol	Conditions	Min	Max	Unit
EIO reset time	t_{ER}	CL = 15pF (EIO)	—	120	ns
EIO output delay time	t_{DCL}		—	55	ns
LP → SEG output delay time	t_{LSD}	CL = 100pF (On)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	400	ns

V_{CC} = +2.7 to 4.5V, V0 = +14.0 to +28.0V

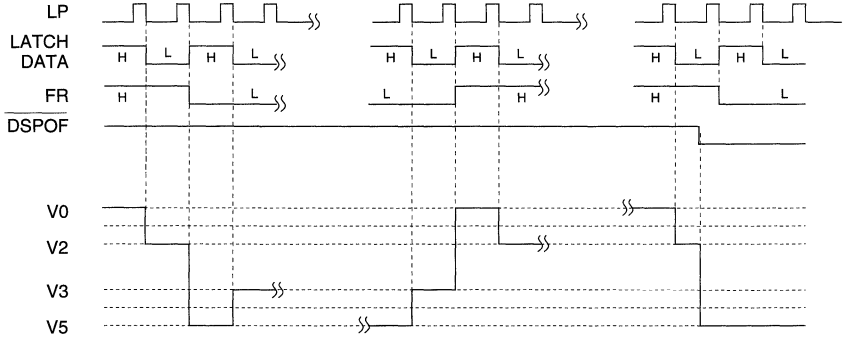
Parameter	Symbol	Conditions	Min	Max	Unit
EIO reset time	t_{ER}	CL = 15pF (EIO)	—	240	ns
EIO output delay time	t_{DCL}		—	85	ns
LP → SEG output delay time	t_{LSD}	CL = 100pF (On)	—	400	ns
FR → SEG output delay time	t_{FRSD}		—	800	ns

● Timing Diagram

Timing Diagram (assuming 1/240 duty). (This diagram provided only as a reference.)

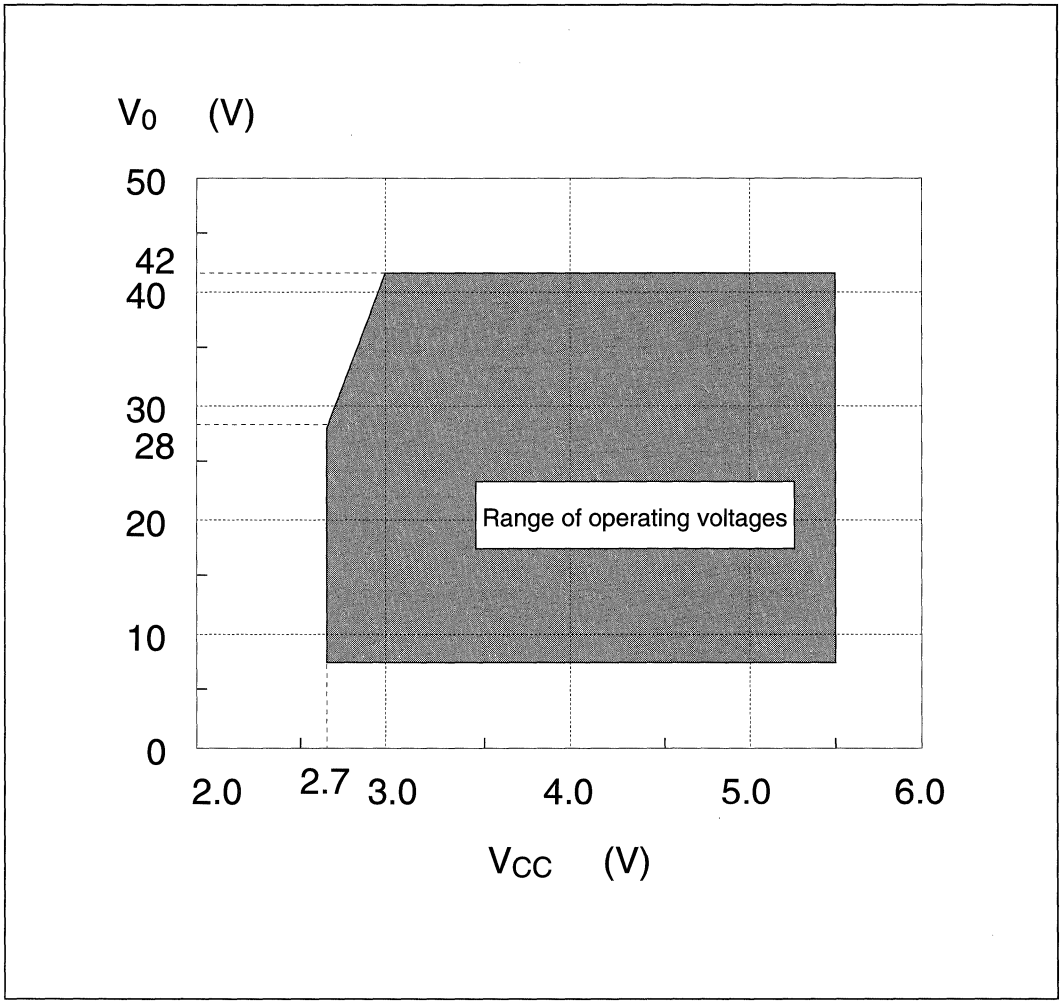


① ~ ⓝ indicate driver cascade numbers.
Under high-speed data transfer, it is necessary to make the XSCL frequency longer than the LP pulse delay timing to ensure the LP → XSCL (t_{LH}) standard values.



■ RANGE OF OPERATING VOLTAGES Vcc – V0

It is necessary to set the voltage of V0 in the range of voltages Vcc – V0 shown in the figure below:



■ LCD DRIVING POWER

● Method of Forming Each Voltage Level

The simplest way to obtain the voltage levels for driving the LCs is to use resistive voltage dividers between VO and GND, and to drive the LCs with op amp voltage followers.

In consideration of the use of op amps, V5 (the lowest voltage setting for driving LCs) and GND are separated and given separate terminals.

However, when the voltage level of V5 is above GND and the voltage difference between V5 and GND is large, the performance of the LC output driver is reduced. Therefore, ensure that the voltage gap between V5 and GND is in the range of 0V to 2.5V.

Permanent damage may result to the LSI when there is serial resistance in the V0 or GND power line. This is because, a voltage drop will occur at V0 or GND of the LSI power terminal (depending on the IO when the signal is changed), causing the power level relationships within the LCD (i.e., $V_{DDH} \geq V0 \geq V2 \geq V3 \geq V5 \geq$ GND) to fail.

When a guard resistance is inserted, voltage stabilization using a capacitance is necessary.

● Cautions During Power Up and Power Down

Because of the high voltage of the LC driving system of this LSI, if the power to the logic system is floating or if V_{CC} is less than or equal to 2.6V when a high voltage of 30V or more is applied to the LC driving system, or if the LC driving signal is output before the LC driving system voltage stabilizes, then too much current will flow, causing damage to the LSI.

It is recommended that the display off function ($\overline{DSPOF}$) be used until the LC drive system voltage stabilizes, and that the LC drive output voltage be put to the V5 level.

Follow the sequences below during power up and power down:

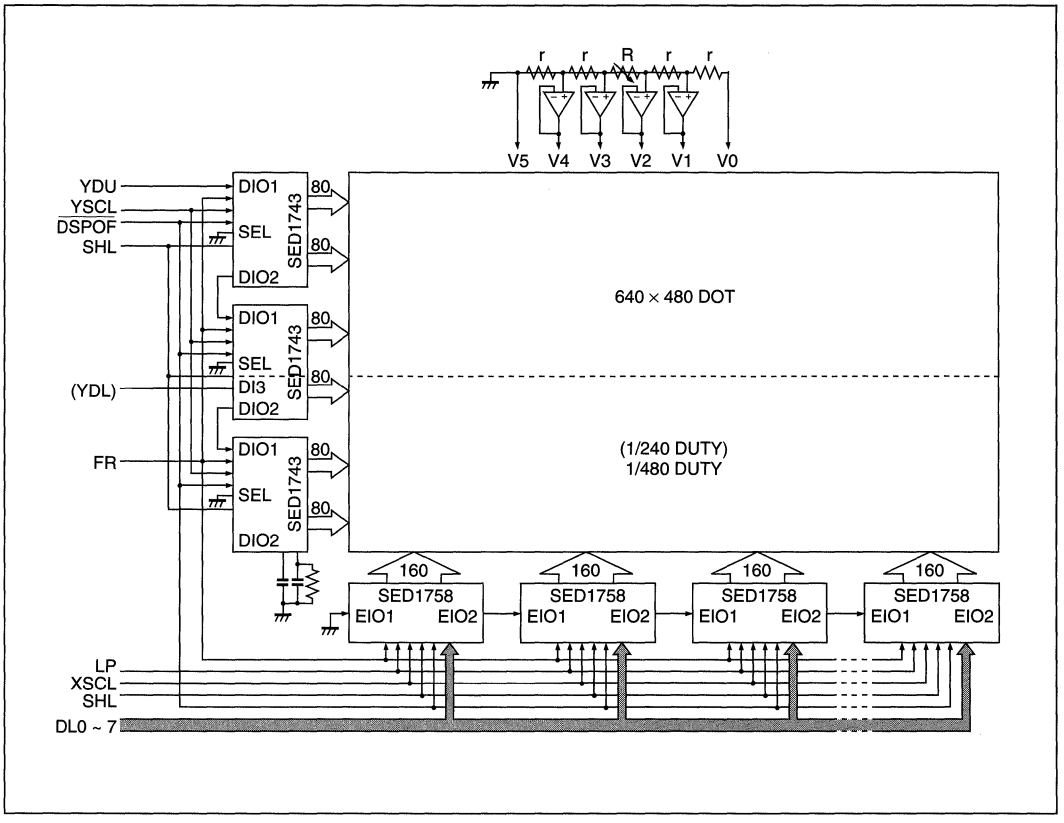
Power up: Logic system on → LC drive system on (or simultaneous)

Power down: LC drive system off → Logic system off (or simultaneous)

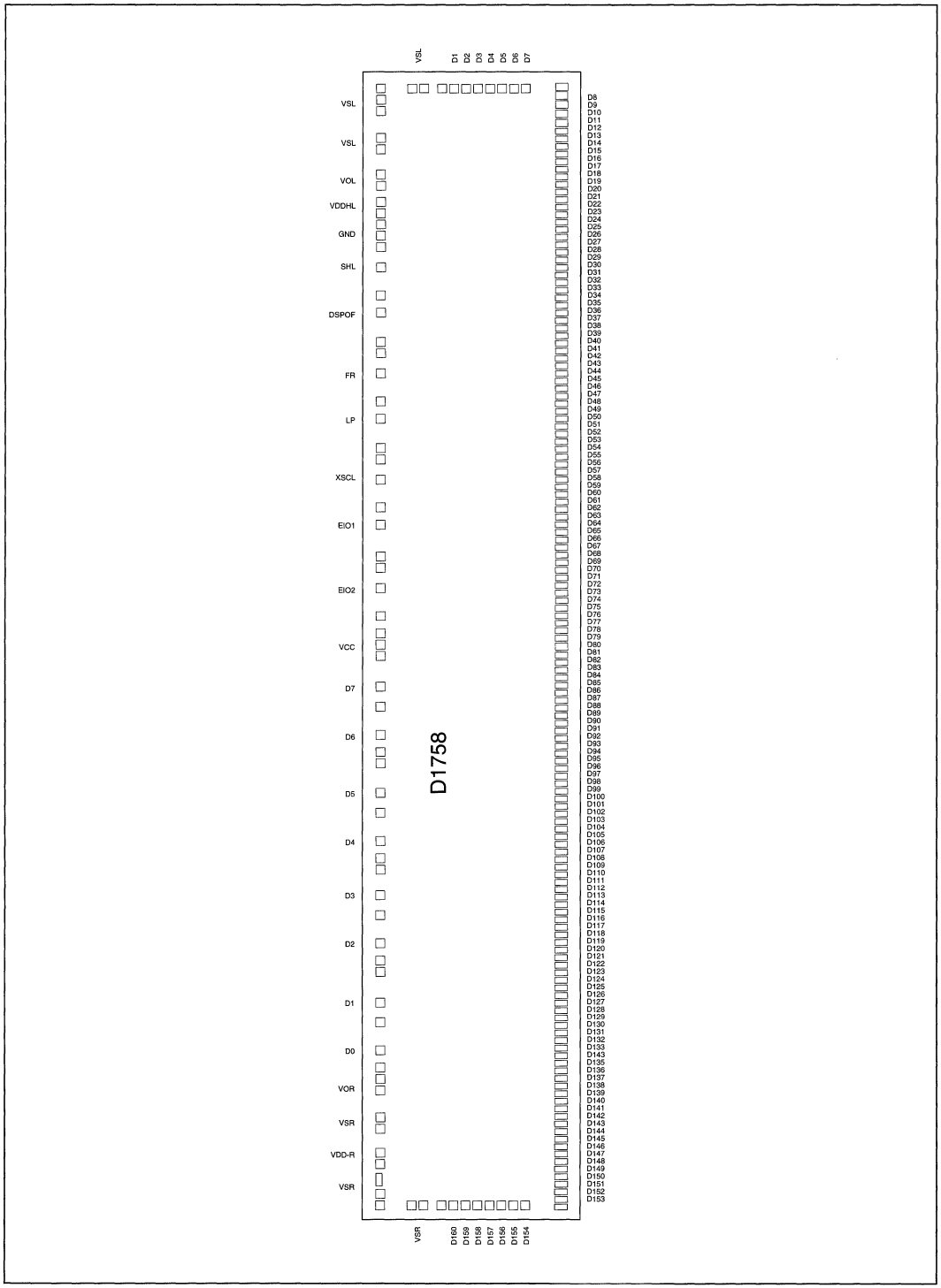
In order to prevent excessive current, insert a high-speed fuse in series with the LC power source. The optimal value of the guard resistance must be selected based on the capacitance of the LC cells.

■ EXAMPLE OF CONNECTION

● Large Screen LCD Structure Diagram



■ PAD LAYOUT


VSL
D1
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D8
D9
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D11
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D14
D15
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D150
D151
D152
D153
VSL
VSL
VOL
VDDHL
GND
SHL
DSPOF
FR
LP
XSCL
EIO1
EIO2
VCC
D7
D6
D5
D4
D3
D2
D1
D0
VOR
VSR
VDD-R
VSR
D1758
VSR
D160
D159
D158
D157
D156
D155
D154

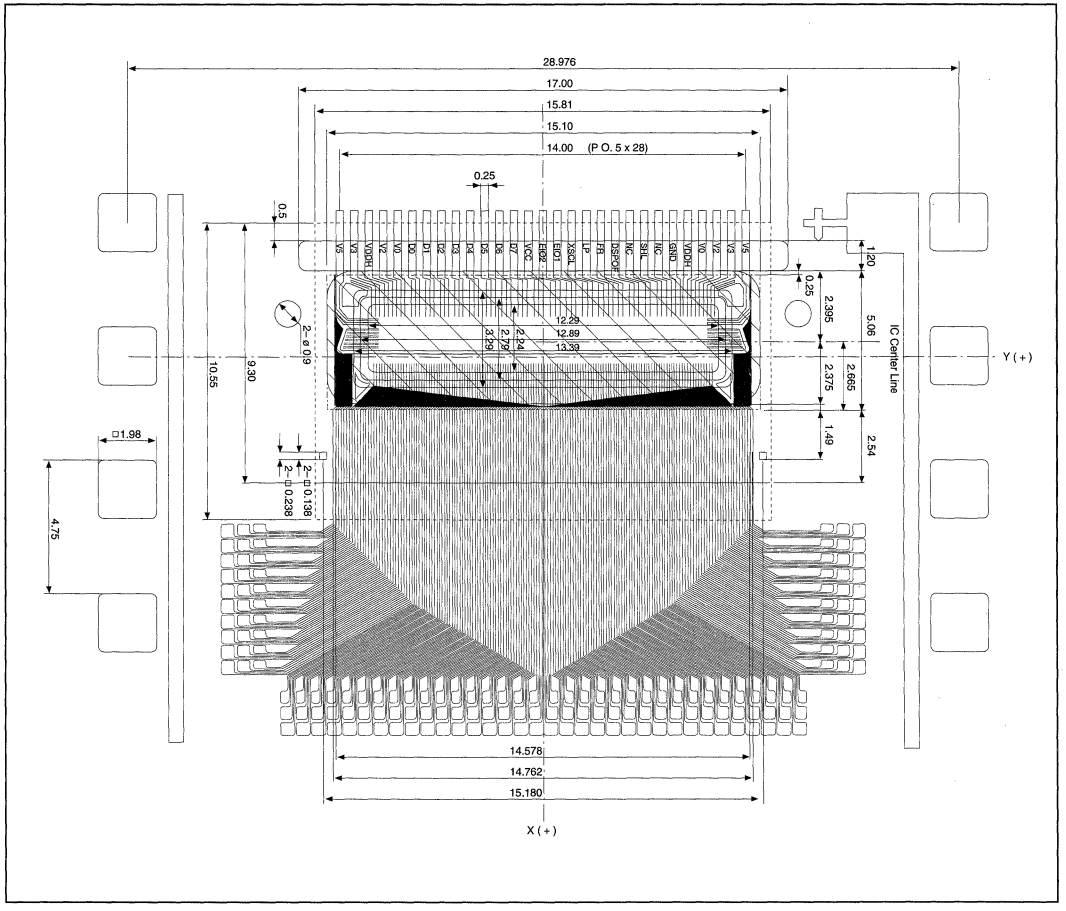
■ PAD COORDINATES

Pin No.	Pin Name	X	Y
1	NC	–5953	–915
2	V3L	–5834	–915
3	V3L	–5692	–927
4	V2L	–5419	–915
5	V2L	–5292	–915
6	V0L	–5035	–915
7	V0L	–4907	–915
8	VDDHL	–4748	–937
9	VDDHL	–4620	–937
10	GND	–4491	–937
11	GND	–4364	–937
12	NC	–4235	–937
13	SHL	–4033	–937
14	NC	–3743	–937
15	DSPOF	–3541	–937
16	NC	–3250	–937
17	NC	–3121	–937
18	FR	–2920	–937
19	NC	–2629	–937
20	LP	–2428	–937
21	NC	–2137	–937
22	NC	–2008	–937
23	XSCL	–1806	–937
24	NC	–1561	–937
25	EIO1	–1288	–937
26	NC	–994	–937
27	NC	–865	–937
28	EIO2	–637	–937
29	NC	–345	–937
30	VCC	–119	–937
31	VCC	7	–937
32	NC	136	–937
33	D7	427	–937
34	NC	628	–937
35	D6	919	–937
36	NC	1121	–937
37	NC	1250	–937
38	D5	1540	–937
39	NC	1742	–937
40	D4	2033	–937
41	NC	2234	–937
42	NC	2363	–937
43	D3	2654	–937
44	NC	2855	–937
45	D2	3146	–937
46	NC	3347	–937
47	NC	3477	–937
48	D1	3767	–937
49	NC	3969	–937
50	D0	4259	–937
51	NC	4461	–937
52	V0R	4620	–937
53	V0R	4748	–937
54	V2R	5005	–937
55	V2R	5132	–937
56	VDDHR	5390	–937
57	VDDHR	5517	–937
58	V3R	5692	–927
59	V3R	5834	–915
60	NC	5953	–915
61	V5R	5946	–604
62	V5R	5946	–497
63	NC	5967	–311
64	O160	5967	–188
65	O159	5967	–64
66	O158	5967	58
67	O157	5967	182
68	O156	5967	305
69	O155	5967	429
70	O154	5967	552
71	NC	5972	924
72	O153	5878	924
73	O152	5784	924
74	O151	5690	924
75	O150	5596	924
76	O149	5509	924
77	O148	5428	924
78	O147	5348	924
79	O146	5268	924
80	O145	5187	924
81	O144	5107	924
82	O143	5027	924
83	O142	4947	924
84	O141	4866	924
85	O140	4786	924
86	O139	4706	924
87	O138	4626	924
88	O137	4545	924
89	O136	4465	924
90	O135	4385	924
91	O134	4304	924
92	O133	4224	924
93	O132	4144	924
94	O131	4064	924
95	O130	3983	924
96	O129	3903	924
97	O128	3823	924
98	O127	3743	924
99	O126	3662	924
100	O125	3582	924
101	O124	3502	924
102	O123	3421	924
103	O122	3341	924
104	O121	3261	924
105	O120	3181	924
106	O119	3100	924
107	O118	3020	924
108	O117	2940	924
109	O116	2859	924
110	O115	2779	924
111	O114	2699	924
112	O113	2619	924
113	O112	2538	924
114	O111	2458	924
115	O110	2378	924
116	O109	2298	924
117	O108	2217	924
118	O107	2137	924
119	O106	2057	924
120	O105	1976	924
121	O104	1896	924
122	O103	1816	924
123	O102	1736	924
124	O101	1655	924
125	O100	1575	924
126	O99	1495	924
127	O98	1415	924
128	O97	1334	924
129	O96	1254	924
130	O95	1174	924
131	O94	1093	924
132	O93	1013	924
133	O92	933	924
134	O91	853	924
135	O90	772	924
136	O89	692	924
137	O88	612	924
138	O87	532	924
139	O86	451	924
140	O85	371	924
141	O84	291	924
142	O83	210	924
143	O82	130	924
144	O81	50	924
145	O80	–39	924
146	O79	–130	924
147	O78	–210	924
148	O77	–290	924
149	O76	–370	924
150	O75	–451	924

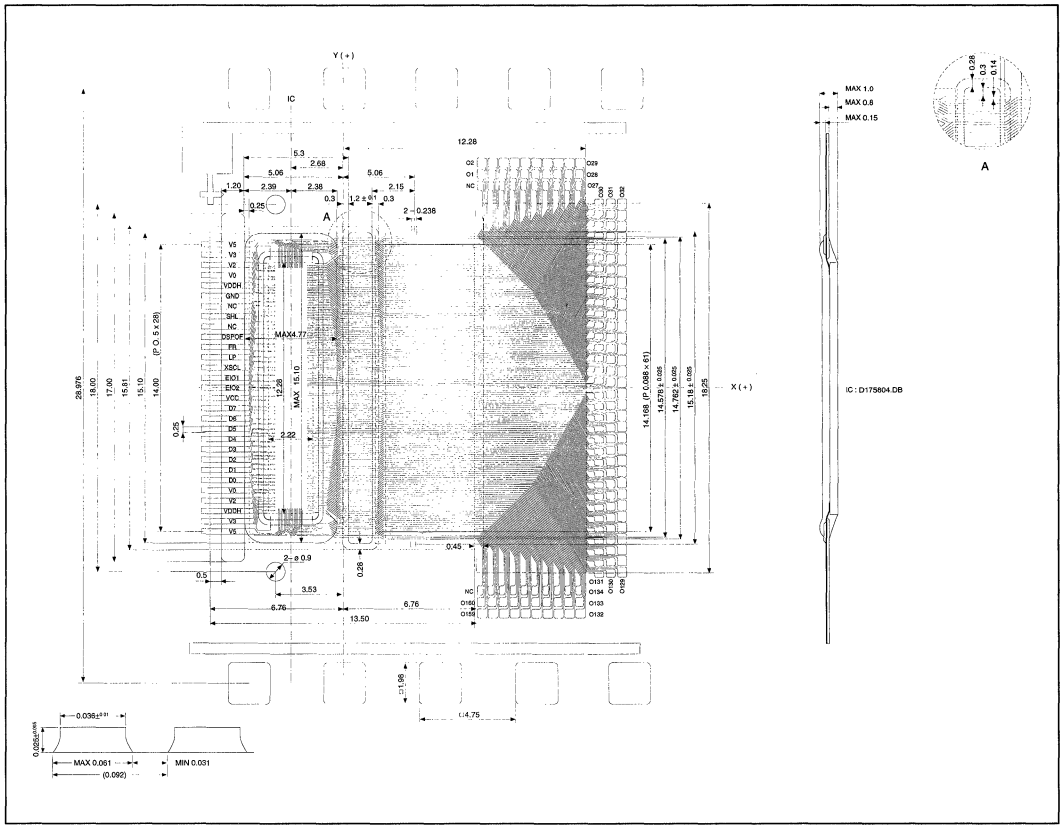
Pin No.	Pin Name	X	Y
151	O74	–531	924
152	O73	–611	924
153	O72	–692	924
154	O71	–772	924
155	O70	–852	924
156	O69	–932	924
157	O68	–1013	924
158	O67	–1093	924
159	O66	–1173	924
160	O65	–1254	924
161	O64	–1334	924
162	O63	–1414	924
163	O62	–1494	924
164	O61	–1575	924
165	O60	–1655	924
166	O59	–1735	924
167	O58	–1815	924
168	O57	–1896	924
169	O56	–1976	924
170	O55	–2056	924
171	O54	–2137	924
172	O53	–2217	924
173	O52	–2297	924
174	O51	–2377	924
175	O50	–2458	924
176	O49	–2538	924
177	O48	–2618	924
178	O47	–2698	924
179	O46	–2779	924
180	O45	–2859	924
181	O44	–2939	924
182	O43	–3020	924
183	O42	–3100	924
184	O41	–3180	924
185	O40	–3260	924
186	O39	–3341	924
187	O38	–3421	924
188	O37	–3501	924
189	O36	–3581	924
190	O35	–3662	924
191	O34	–3742	924
192	O33	–3822	924
193	O32	–3903	924
194	O31	–3983	924
195	O30	–4063	924
196	O29	–4143	924
197	O28	–4224	924
198	O27	–4304	924
199	O26	–4384	924
200	O25	–4465	924

Pin No.	Pin Name	X	Y
201	O24	–4545	924
202	O23	–4625	924
203	O22	–4705	924
204	O21	–4786	924
205	O20	–4866	924
206	O19	–4946	924
207	O18	–5026	924
208	O17	–5107	924
209	O16	–5187	924
210	O15	–5267	924
211	O14	–5348	924
212	O13	–5428	924
213	O12	–5508	924
214	O11	–5595	924
215	O10	–5690	924
216	O9	–5784	924
217	O8	–5878	924
218	NC	–5972	924
219	O7	–5967	552
220	O6	–5967	429
221	O5	–5967	305
222	O4	–5967	182
223	O3	–5967	58
224	O2	–5967	–64
225	O1	–5967	–188
226	NC	–5967	–311
227	V5L	–5946	–497
228	V5L	–5946	–604

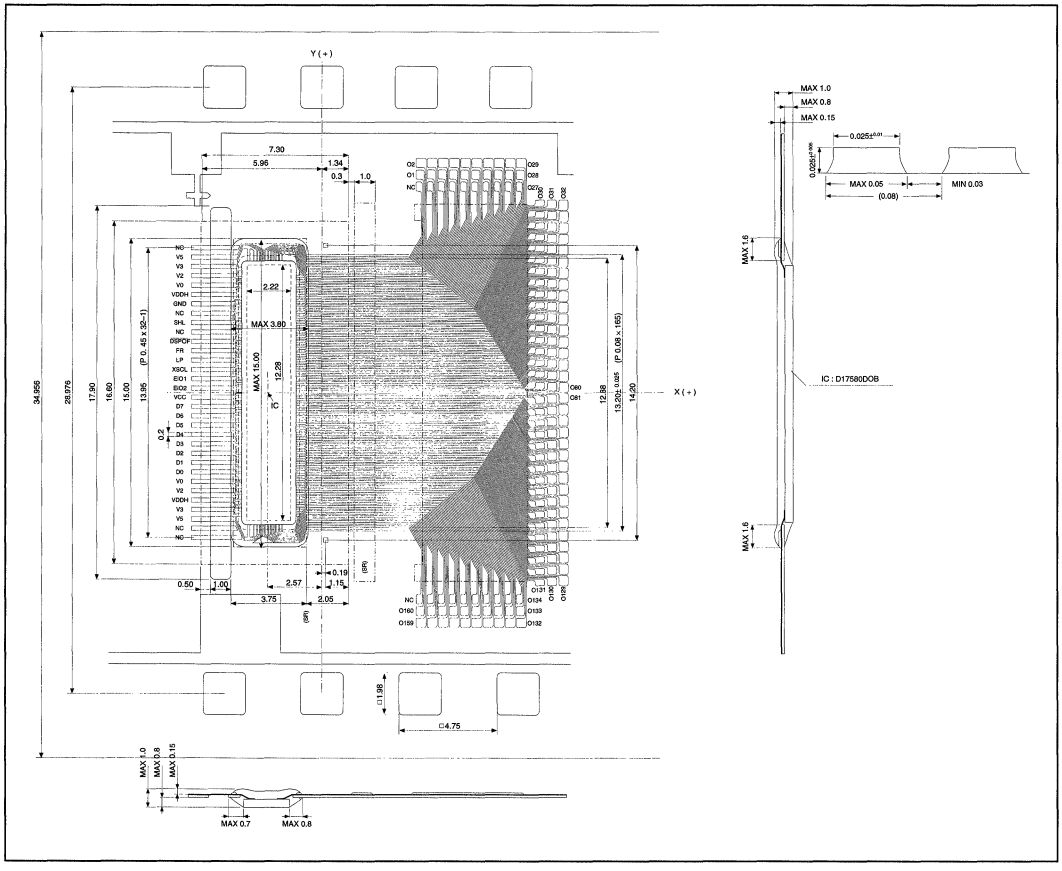
■ DIAGRAM OF EXTERNAL DIMENSIONS (for reference) (SED1758T$_{0A}$)



■ DIAGRAM OF EXTERNAL DIMENSIONS (for reference) (SED1758T$_{0B}$)



■ DIAGRAM OF EXTERNAL DIMENSIONS (for reference) (SED1758T$_{0G}$)



CMOS HIGH DUTY LCD SEGMENT DRIVER

■ DESCRIPTION

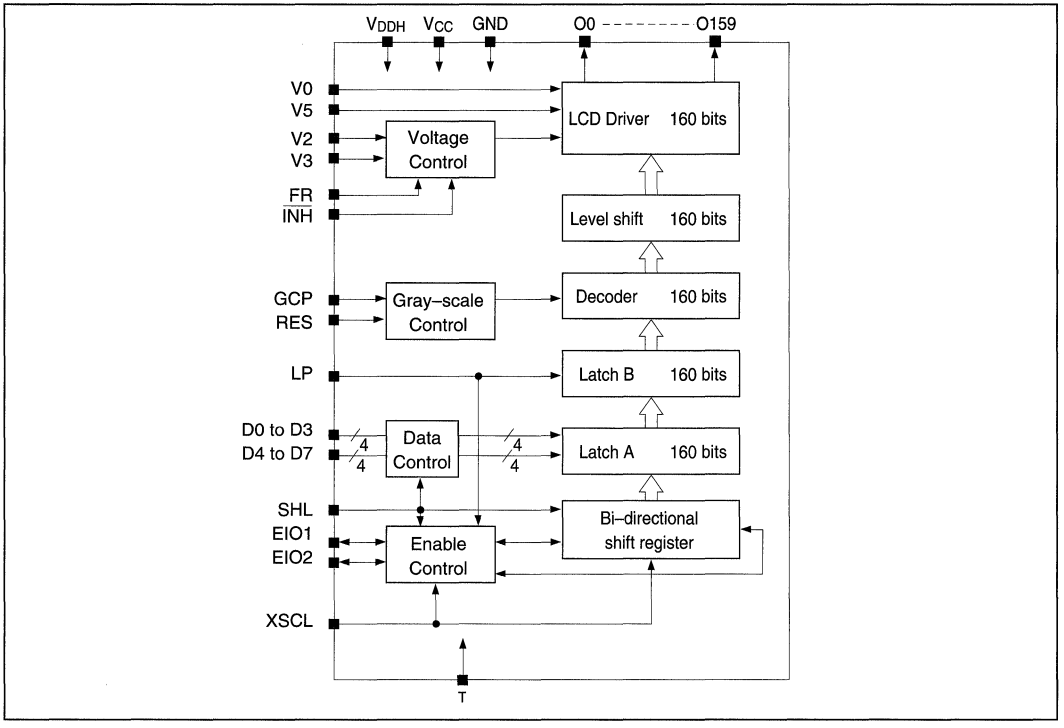
The SED1765 is a segment (column) driver for high-capacity dot matrix liquid crystal panels. It incorporates 160 high-voltage segment (column) drivers, and is designed for use in conjunction with the SED1703F common (row) driver device.

The SED1765 uses a PWM (Pulse Width Modulation) technique to provide 16, 8, or 4-level gray-scale displays without ghosting. The LCD drivers have been designed for low on output resistance making the SED1765 suitable for MIM LCD panels, and yielding gray-scale displays with few contrast disparities.

■ FEATURES

- 16, 8 or 4-level PWM gray-scale LCD driver
- Supports gray-scale gamma correction
- Two parallel 4-bit inputs
- 160 LCD drive outputs
- Maximum clock speed of 12 MHz allows a 640x480 pixel display with daisy-chain enable. Speeds up to 16 MHz are possible using external enable generation
- Wide 14 to 40 V range of LCD drive voltages
- Display blanking function
- Output shift direction is pin-selectable
- Automatic enable signal propagation allows cascade connection and decreases power consumption
- Adjustable LCD drive voltage offset relative to ground and supply
- Logic circuitry uses single 5.0V ±10% power supply
- CMOS Si-gate process
- Packages:
  Al pad chip: SED1765D0A
  Au bump pad chip: SED1765D0B
- Also available in tab

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

● 1.1 Gray-Scale Control Circuit

This circuit divides the gray-scale generation clock input on pin GCP, passes it to the decoder block. The divider circuit is reset on the falling edge of the RE3 or LP inputs or when the $\overline{\text{INH}}$ input is LOW.

● 1.2 Data Control Circuit

This circuit reorders the gray-scale data input on the D0 to D3 and D4 to D7 pins, into the order specified by the SHL input, and puts them on the internal data bus. It holds all data bus lines LOW if the device is disabled by the control signal from the enable controller.

● 1.3 Enable Controller

This circuit causes the data bus and the internal clock to be held LOW, and puts the device into power save mode, if the enable signal is inactive.

In systems with more than one segment driver, the enable inputs and outputs are cascaded, and the enable input at the head of the chain connected to ground. The enable controller counts the number of input data bits, and sets the enable output LOW to allow the next device in the chain to start loading data. This configuration eliminates the need for the controlling device to generate enable control signals.

The EIO output is reset HIGH by the LP input.

● 1.4 Shift Register

Segment data shift register. The latch A control signal is shifted by the shift clock. The direction of data shift is selected by the SHL pin as shown in the figure below.

SHL	O (SEG Output)							EIO	
	159	158	157	.....	2	1	0	1	2
L	A0	B0	A1	.....	B78	A79	B79	Output	Input
H	B79	A79	B78	.....	A1	B0	A0	Input	Output

● 1.5 Latch A

The gray-scale data present on the internal data bus is latched successively by the latch control signal from the shift register.

● 1.6 Latch B

The data in latch A is latched in on the falling edge of LP.

● 1.7 Decoder

This circuit is locked to the signal from the gray-scale controller, and generates a pulse width corresponding to the gray-scale data value.

● 1.8 Level Shifter

The level shifter converts the logic-level signal from latch B to the voltage levels required by the LCD drivers.

● 1.9 LCD Drivers and Voltage Control Circuit

The LCD drivers drive individual columns of the display matrix with the voltage determined by the inhibit signal $\overline{INH}$, the frame signal FR, and the latched display data. This is shown in the table below.

$\overline{INH}$	Data	FR	SEG Output Voltage
H	H	H	V0
		L	V5
	L	H	V2
		L	V3
L	—	H	V2
		L	V3

■ PIN DESCRIPTION

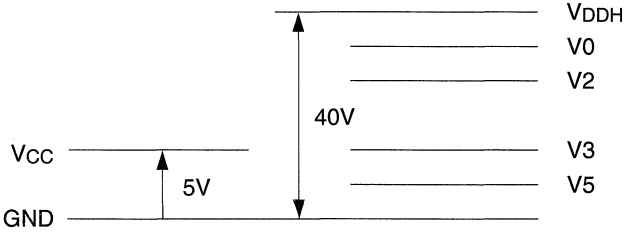
Pin Name	Function
O0 to O159	Segment drive outputs
D0 to D3, D4 to D7	4-bit gray-scale data inputs. D0 and D4 are the LSBs of each 4-bit nibble.
XSCL	Segment data shift clock input. Data is shifted into the driver on the falling edge of XSCL.
LP	Segment data latch strobe. Data is latched on the falling edge of LP.
EIO1, EIO2	Daisy chain enable input/outputs configured by SHL
GCP	Gray-scale reference clock input.
RES	PWM waveform reset input. The PWM waveform is reset to the OFF level by the falling edge of this input.
SHL	Shift direction select input. This signal configures EIO1, EIO2 and selects the shift register shift direction. An is input on D0 to D3 and Bn on D4 to D7.
FR	LCD AC-drive waveform input.
$\overline{INH}$	Display blanking input. When LOW, all outputs go to "off" levels.
V_{CC}, GND	Logic power supply inputs.
T	Test input. Tie low

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	-0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	-0.3 to +45.0	V
Supply voltage (3)	V0, V2, V3, V5	-0.3 to V_{DDH}+0.3	V
Input voltage	V_I	-0.3 to V_{CC}+0.3	V
Operating temperature	T_{opr}	-20 to +75	°C
Storage temperature 1	T_{stg}	-65 to +150	°C

Notes: 1. All voltages are with respect to ground.
2. Drive voltages should always be such that $V_{DDH} \geq V0 \geq V2 \geq V3 \geq V5 \geq$ ground.



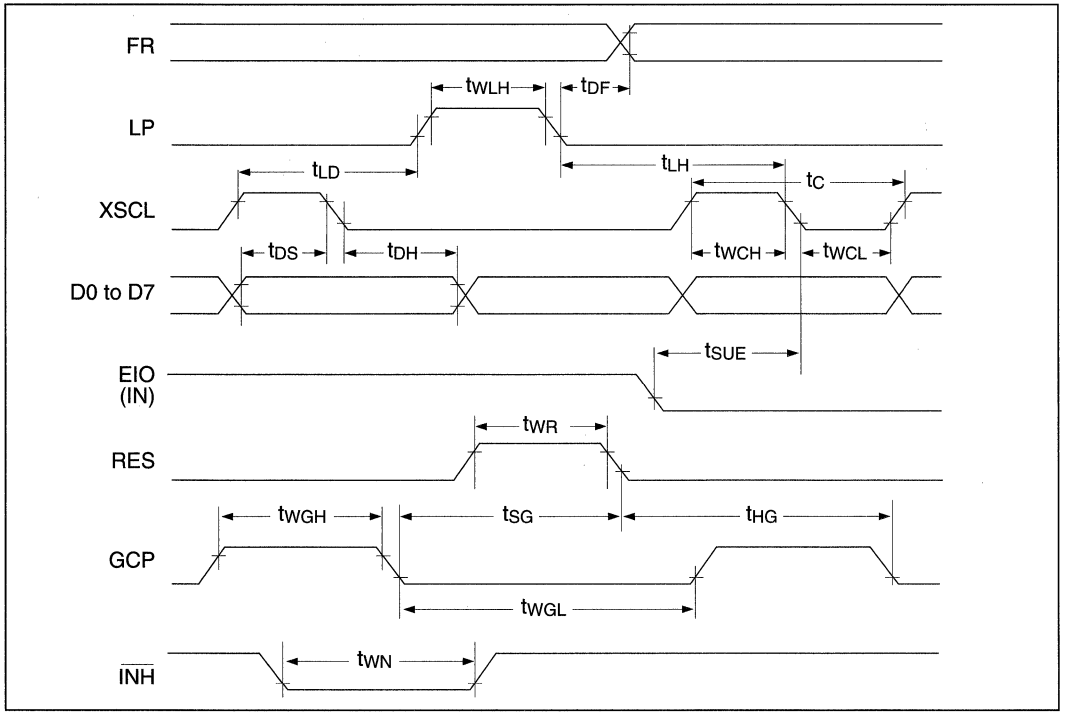
3. The device may be permanently damaged if the LCD power supplies are applied while the 5V logic supply is floating. Pay particular attention to the power-on and power-off sequence.

● **DC Characteristics** T_a=-20 to 75°C, V5=0V, V_{CC}=5.0V±10% unless otherwise noted

Parameter	Symbol	Condition	Applicable Signal	Rating Min	Rating Typ	Rating Max	Unit
Supply voltage (1)	V_{CC}		V_{CC}	4.5	5.0	5.5	V
Supply voltage (2)	V_{DDH}		V_{DDH}	14.0	—	40.0	V
Input voltage	V0	V0≥V2≥V3≥V5 Recommended	V0	V_{DDH}-2.5	—	V_{DDH}	V
Input voltage (1)	V2		V2	7/9xV_{DDH}	—	V_{DDH}	V
Input voltage (2)	V3, V5		V3, V5	GND	—	2.9xV_{DDH}	V
HIGH-level input voltage	V_{IH}		All input pins.	0.8xV_{CC}	—	0.2xV_{CC}	V
LOW-level input voltage	V_{IL}			GND	—	0.2xV_{CC}	V
HIGH-level output voltage	V_{OH}	I_{OH}=-0.4 mA	EIO1, EIO2	V_{CC}-0.4	—	V_{CC}	V
LOW-level output voltage	V_{OL}	I_{OH}=0.4 mA		GND	—	0.4	V
Input leakage current	I_{LI}	GND≤VI≤V_{CC}	All pins except EIO.	—	—	2.0	µA
I/O leakage current	$I_{LI/O}$	GND≤VI≤V_{CC}	EIO1, EIO2	—	—	5.0	µA
Quiescent current	I_{GND}	V_{DOH}=14.0 to 40.0 V, V_{IH}=V_{CC}, V_{IL}=GND	GND	—	—	25	µA
Segment output ON resistance See note 1.	R_O	V_{OH}=0.5V, V_{DDH}=10.0V	O0 to O159	—	2.0	6.5	kΩ
		V_{OH}=0.5V, V_{DDH}=20.0V		—	1.5	3.5	kΩ
		V_{OH}=0.5V, V_{DDH}=30.0V		—	1.3	3.0	kΩ
Operating current (1)	f_{CC}	V_{CC}=5.0V, V_{IH}=V_{CC}, V_{IL}=GND, f_{xaCL}=10.6MHz, f_{LP}=33.8kHz, I_{f16}=0.54 MHz, FR=70 Hz, D0 to D7=F0F0..., alternating	V_{CC}	—	2.5	5.0	mA
Operating current (2)	I_{DDH}	V_{CC}=5.0V, V5=0V, V3=4V, V2=26V, V0=V_{DDH}=30V, other conditions same as I_{CC}	V_{DDH}	—	0.5	1.2	mA
Input capacitance See note 2.	C_1	T_a=25°C, Freq.=1 MHz	All pins except E1O	—	—	8.0	pF
I/O capacitance See note 2.	C_{LO}	T_a=25°C, Freq.=1 MHz	EIO1, EIO2	—	—	15.0	pF

1. Within the specified ranges of V0, V2, V3 and V4
2. Applies to chip part only.

- **AC Characteristics**
- **Input Timing**



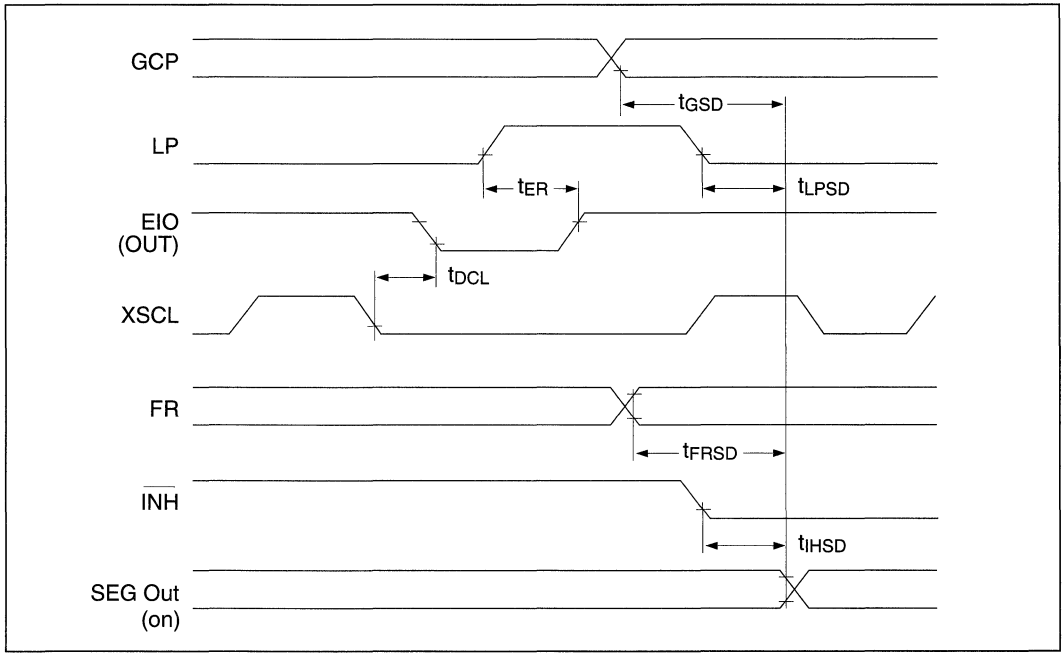
Note: For timing for LP pulse input, omit one XSCL clock cycle.

T_a=-20 to 75°C, V_{CC}=5.0V±10%

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
XSCL-period	t_C		71	—	—	ns
XSCL High pulse width	t_{WCH}		30	—	—	ns
XSCL Low pulse width	t_{WCL}		30	—	—	ns
EIO setup time	t_{SUE}		30	—	—	ns
Data setup time	t_{DS}		30	—	—	ns
Data hold time	t_{DH}		20	—	—	ns
XSCL→LP rising edge	t_{LD}		10	—	—	ns
LP→XSCL rising edge	t_{LH}		100	—	—	ns
LP pulse width	t_{WLH}	See note.	80	—	—	ns
RES pulse width	t_{WR}		100	—	—	ns
$\overline{INH}$ low pulse width	t_{WN}		100	—	—	ns
GCP high pulse width	t_{WGH}		80	—	—	ns
GCP low pulse width	t_{WGL}		80	—	—	ns
FR delay time	t_{DF}		-300	—	+300	ns
GCP setup time	t_{SG}		100	—	—	ns
GCP hold time	t_{HG}		100	—	—	ns

Note: t_{WLP} indicates the time XSLC is LOW as well as the time that LP is HIGH.

● **Output Timing**

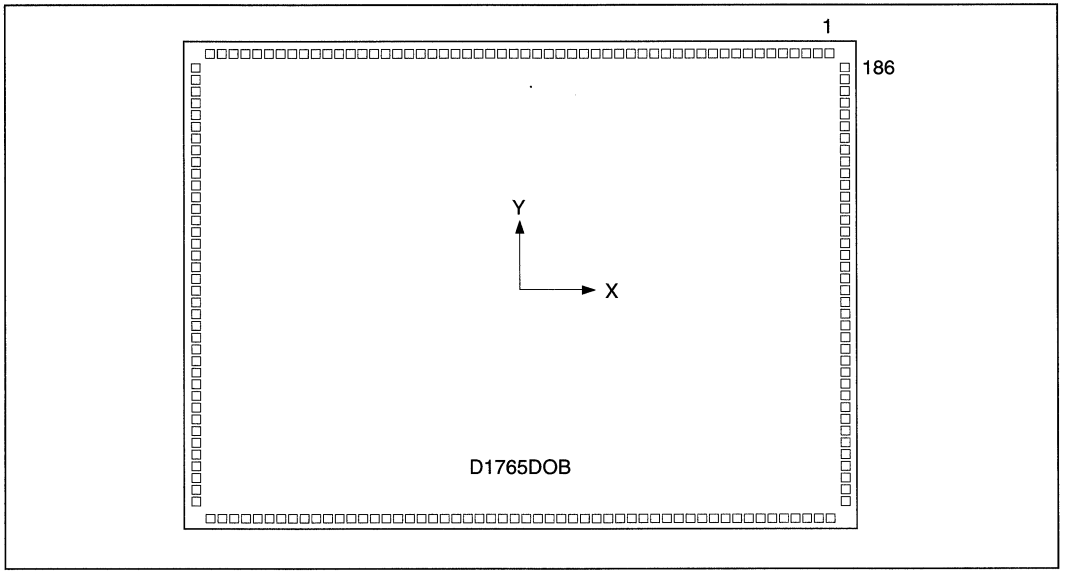


Ta=-20 to 75°C, VDDH=14.0V to 40.0V

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
EIO output reset time	tER	CL=15 pF	—	—	120	ns
EIO output delay time	tDCL		—	—	40	ns
LP→SEG (On) output delay time	tLPSD	CL=100 pF	—	—	2.0	µs
SEG→LP (On) output delay time	tFRSD		—	—	2.0	µs
$\overline{INH}$→SEG (On) output delay time	tIHSD		—	—	2.0	µs
GCP→SEG (On) output delay time	tGSD		—	—	2.0	µs

■ MECHANICAL SPECIFICATIONS

● Pad Layout



Chip size: 8.80 x 5.62

Pad pitch: 0.134 mm min.

* Al pad (SED1765DOA)

  Chip thickness: 0.400 ± 0.025 mm

  Pad size, type A: 100 x 100 μm (All pads except 36, 37, 38, 39, 40)

  Pad size, type B: 160 x 100 μm (Pads 36, 37, 38, 39, 40)

* Au bump pad (SED1765DOB)

  Chip thickness: 0.525 ± 0.025 mm

  Pad size, type A: 102 x 100 ± 20 μm (All pads except 36, 37, 38, 39, 40)

  Pad size, type B: 186 x 100 ± 20 μm (Pads 36, 37, 38, 39, 40)

Note: Sizes are specified as x-dimension x y-dimension. X is parallel to the scribe-line.

● Pad Coordinates

Pad		X	Y
Number	Name		
1	O146	3950	2643
2	O147	3814	2643
3	O148	3678	2643
4	O149	3542	2643
5	O150	3406	2643
6	O151	3270	2643
7	O152	3134	2643
8	O153	2998	2643
9	O154	2862	2643
10	O155	2726	2643
11	O156	2590	2643
12	O157	2454	2643
13	O158	2318	2643
14	O159	2182	2643
15	EIO2	1998	2643
16	EIO1	1858	2643
17	GND	1718	2643
18	D0	1578	2643
19	D1	1438	2643
20	D2	1298	2643
21	D3	1158	2643
22	D4	1018	2643
23	D5	878	2643
24	D6	738	2643
25	D7	598	2643
26	NC	458	2643
27	SHL	318	2643
28	XSCL	178	2643
29	TEST	38	2643
30	$\overline{INH}$	-102	2643
31	LP	-242	2643
32	RES	-382	2643
33	GCP	-522	2643
34	V_{CC}	-662	2643
35	FR	-802	2643
36	V0	-1032	2643
37	V5	-1262	2643
38	V3	-1492	2643
39	V2	-1722	2643
40	V_{DDH}	-1952	2643
41	O0	-2182	2643
42	O1	-2318	2643
43	O2	-2454	2643
44	O3	-2590	2643
45	O4	-2726	2643
46	O5	-2862	2643
47	O6	-2998	2643
48	O7	-3134	2643
49	O8	-3270	2643
50	O9	-3406	2643

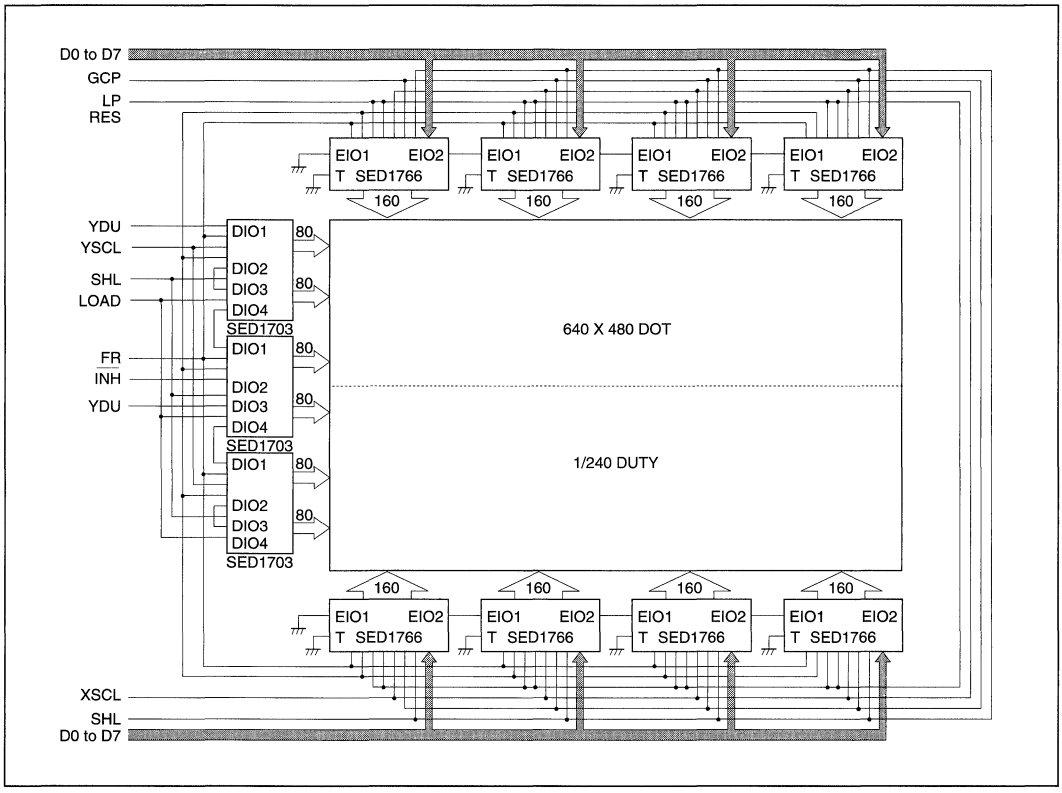
Pad		X	Y
Number	Name		
51	O10	-3542	2643
52	O11	-3678	2643
53	O12	-3814	2643
54	O13	-3950	2643
55	O14	-4230	2379
56	O15	-4230	2243
57	O16	-4230	2107
58	O17	-4230	1971
59	O18	-4230	1835
60	O19	-4230	1699
61	O20	-4230	1563
62	O21	-4230	1427
63	O22	-4230	1291
64	O23	-4230	1155
65	O24	-4230	1019
66	O25	-4230	883
67	O26	-4230	747
68	O27	-4230	611
69	O28	-4230	475
70	O29	-4230	339
71	O30	-4230	203
72	O31	-4230	67
73	O32	-4230	-69
74	O33	-4230	-205
75	O34	-4230	-341
76	O35	-4230	-477
77	O36	-4230	-613
78	O37	-4230	-749
79	O38	-4230	-885
80	O39	-4230	-1021
81	O40	-4230	-1157
82	O41	-4230	-1293
83	O42	-4230	-1429
84	O43	-4230	-1565
85	O44	-4230	-1701
86	O45	-4230	-1837
87	O46	-4230	-1973
88	O47	-4230	-2109
89	O48	-4230	-2245
90	O49	-4230	-2381
91	O50	-3954	-2643
92	O51	-3820	-2643
93	O52	-3686	-2643
94	O53	-3552	-2643
95	O54	-3418	-2643
96	O55	-3284	-2643
97	O56	-3150	-2643
98	O57	-3016	-2643
99	O58	-2882	-2643
100	O59	-2748	-2643

● **Pad Coordinates (cont.)**

Pad		X	Y
Number	Name		
101	O60	-2614	-2643
102	O61	-2480	-2643
103	O62	-2346	-2643
104	O63	-2212	-2643
105	O64	-2078	-2643
106	O65	-1944	-2643
107	O66	-1810	-2643
108	O67	-1676	-2643
109	O68	-1542	-2643
110	O69	-1408	-2643
111	O70	-1274	-2643
112	O71	-1140	-2643
113	O72	-1006	-2643
114	O73	-872	-2643
115	O74	-738	-2643
116	O75	-604	-2643
117	O76	-470	-2643
118	O77	-336	-2643
119	O78	-202	-2643
120	O79	-68	-2643
121	O80	68	-2643
122	O81	202	-2643
123	O82	336	-2643
124	O83	470	-2643
125	O84	604	-2643
126	O85	738	-2643
127	O86	872	-2643
128	O87	1006	-2643
129	O88	1140	-2643
130	O89	1274	-2643
131	O90	1408	-2643
132	O91	1542	-2643
133	O92	1676	-2643
134	O93	1810	-2643
135	O94	1944	-2643
136	O95	2078	-2643
137	O96	2212	-2643
138	O97	2346	-2643
139	O98	2480	-2643
140	O99	2614	-2643
141	O100	2748	-2643
142	O101	2882	-2643
143	O102	3016	-2643
144	O103	3150	-2643
145	O104	3284	-2643
146	O105	3418	-2643
147	O108	3552	-2643
148	O107	3686	-2643
149	O108	3820	-2643
150	O109	3954	-2643

Pad		X	Y
Number	Name		
151	O110	4230	-2381
152	O111	4230	-2245
153	O112	4230	-2109
154	O113	4230	-1973
155	O114	4230	-1837
156	O115	4230	-1701
157	O116	4230	-1565
158	O117	4230	-1429
159	O118	4230	-1293
160	O119	4230	-1157
161	O120	4230	-1021
162	O121	4230	-885
163	O122	4230	-749
164	O123	4230	-613
165	O124	4230	-477
166	O125	4230	-341
167	O126	4230	-205
168	O127	4230	-69
169	O128	4230	67
170	O129	4230	203
171	O130	4230	339
172	O131	4230	475
173	O132	4230	611
174	O133	4230	747
175	O134	4230	883
176	O135	4230	1019
177	O136	4230	1155
178	O137	4230	1291
179	O138	4230	1427
180	O139	4230	1563
181	O140	4230	1699
182	O141	4230	1835
183	O142	4230	1971
184	O143	4230	2107
185	O144	4230	2243
186	O145	4230	2379

■ TYPICAL APPLICATION CIRCUIT



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160 SEGMENT DRIVER WITH GRAY SCALE

■ DESCRIPTION

The SED1766 is a 160-bit output LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI uses a PWM (Pulse Width Modulation) algorithm to achieve 16-, 8- and 4-level gray-scale display without ghosting. Also, an external pulse controller circuit can be used to control the gray-scale pulse position within the horizontal interval.

This device has been designed for low output resistance, making the SED1766 suitable for STN-type LCD panels, and yielding gray-scale displays with few contrast disparities.

The LSI features a wide range of LCD drive voltages.

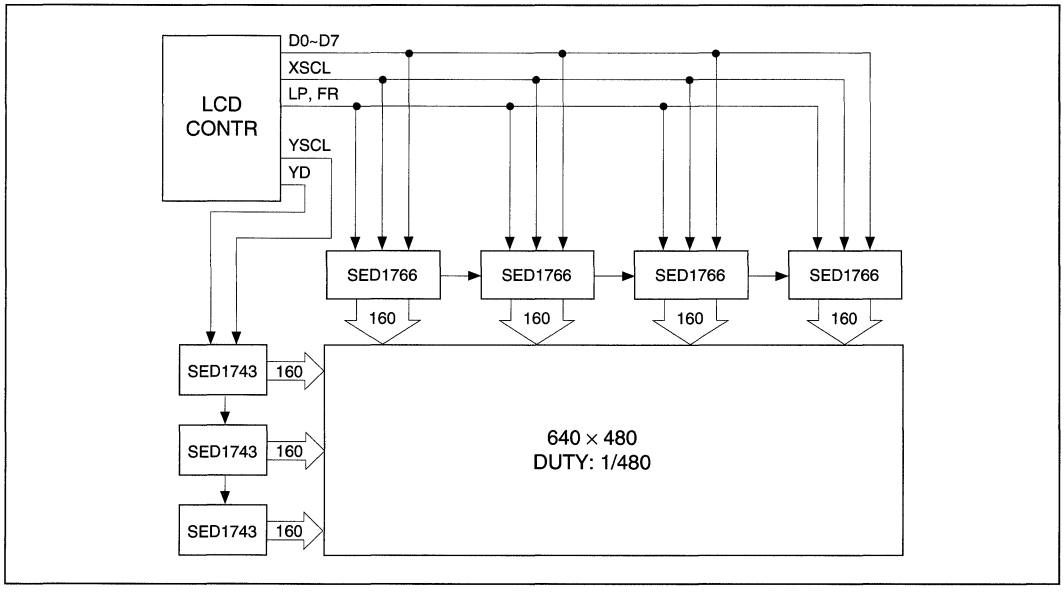
The device uses a high-speed daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1766 is used in conjunction with the SED1743 common drivers to support a large-capacity STN-type dot matrix LCD panel.

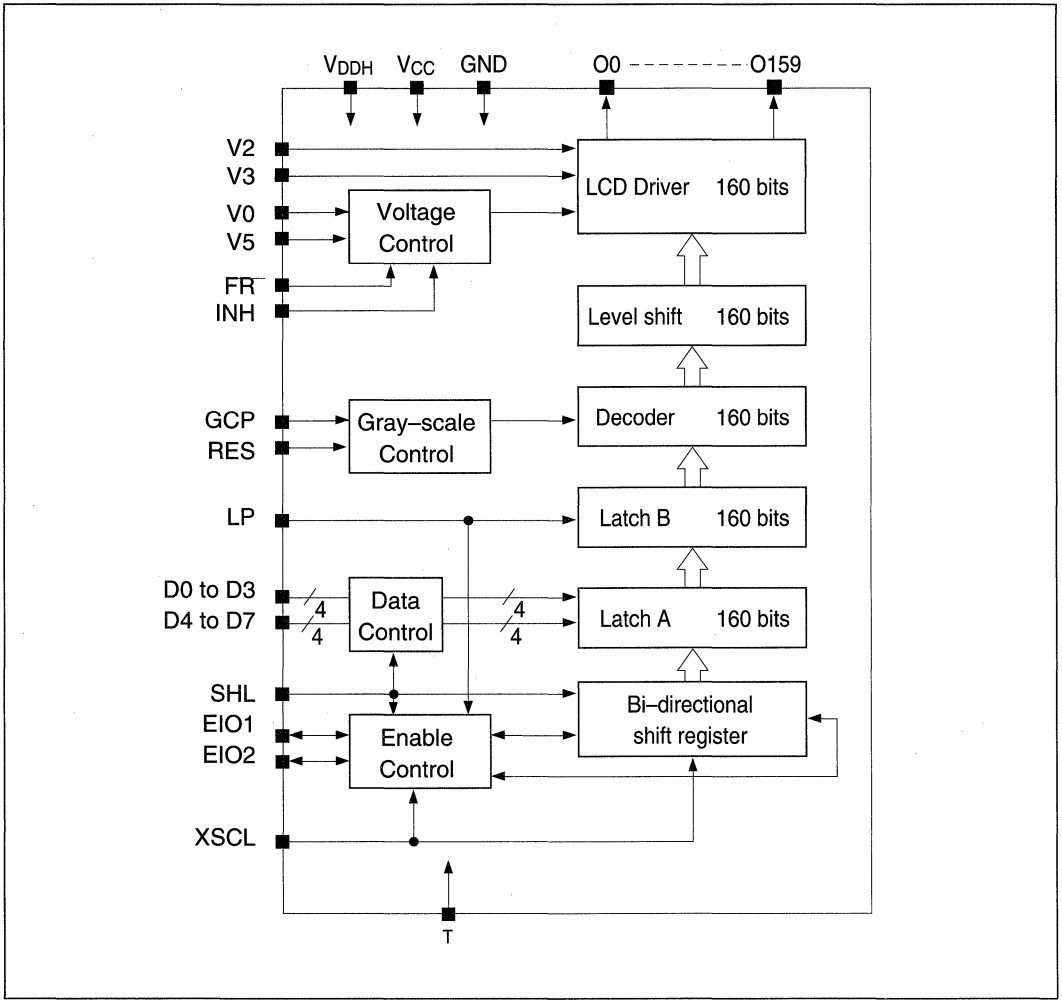
■ FEATURES

- Low-power high-speed CMOS technology
- 160-bit segment (column) driver
- Supports 4-, 8-, and 16-level gray scale
- Supports gray-scale gamma correction
- Two parallel 4-bit input data
- Shift clock frequency ..... 16 MHz
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Selectable output shift direction
- Supports display blanking
- Supports high-speed data transfer
- Low output resistance
- Ability to adjust offset bias of the LCD source from V_{DD}
- Wide range of LCD voltage .... 14 to 40V
- Supply voltage ..... 4.5 to 5.5V
- Package ..... TAB (T_{OA})
  Al pad (D_{OA})
  Au bump (D_{OB})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

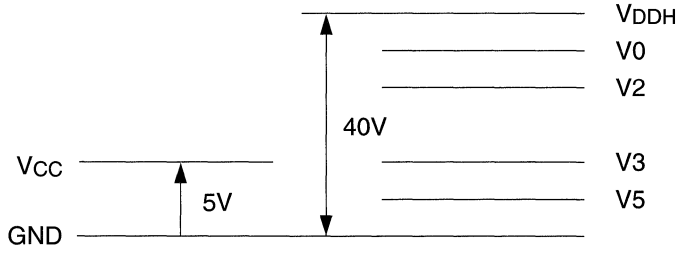
Pin Name	Input/Output	Function
O0 to O159	O	Segment drive outputs
D0 to D3, D4 to D7	I	4-bit gray-scale data inputs. D0 and D4 are the LSBs of each 4-bit nibble.
XSCL	I	Segment data shift clock input. Data is shifted into the driver on the falling edge of XSCL.
LP	I	Segment data latch strobe. Data is latched on the falling edge of LP.
EIO1, EIO2	I/O	Daisy chain enable input/outputs configured by SHL.
GCP	I	Gray-scale reference clock input.
RES	I	PWM mode control input See timing diagrams. V_{OFF} refers to drive voltages V2 and V3, V_{ON} refers to drive voltages V0 and V5. Before RES pulse: $V_{OFF} \rightarrow V_{ON}$ transition mode. After RES pulse: $V_{ON} \rightarrow V_{OFF}$ transition mode.
SHL	I	Shift direction select input. This signal configures EIO1, EIO2 and selects the shift register shift direction. A*n* is input on D0 to D3 and B*n* on D4 to D7.
FR	I	LCD AC-drive waveform input.
$\overline{INH}$	I	Display blanking input. When LOW, all outputs go to OFF levels.
GND	—	Ground
V_{CC}	—	Logic power supply
V_0, V_2, V_3, V_5, V_{DDH}	—	LCD drive voltage supply inputs These voltages should satisfy the following conditions. $V_{DDH} \geq V_0 > V_2 \geq 7/9V_{DDH}$, $2/9V_{DDH} \geq V_3 > V_5 \geq GND$
T	I	Test input Tie low.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V0, V2, V3, V5	–0.3 to V_{DDH}+0.3	V
Input voltage	V_I	–0.3 to V_{CC}+0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature 1	T_{stg}	–65 to +150	°C

Note: Drive voltages should satisfy the following conditions: $V_{DDH} \geq V0 \geq V2 \geq V3 \geq V5 \geq GND$



● **DC Characteristics**

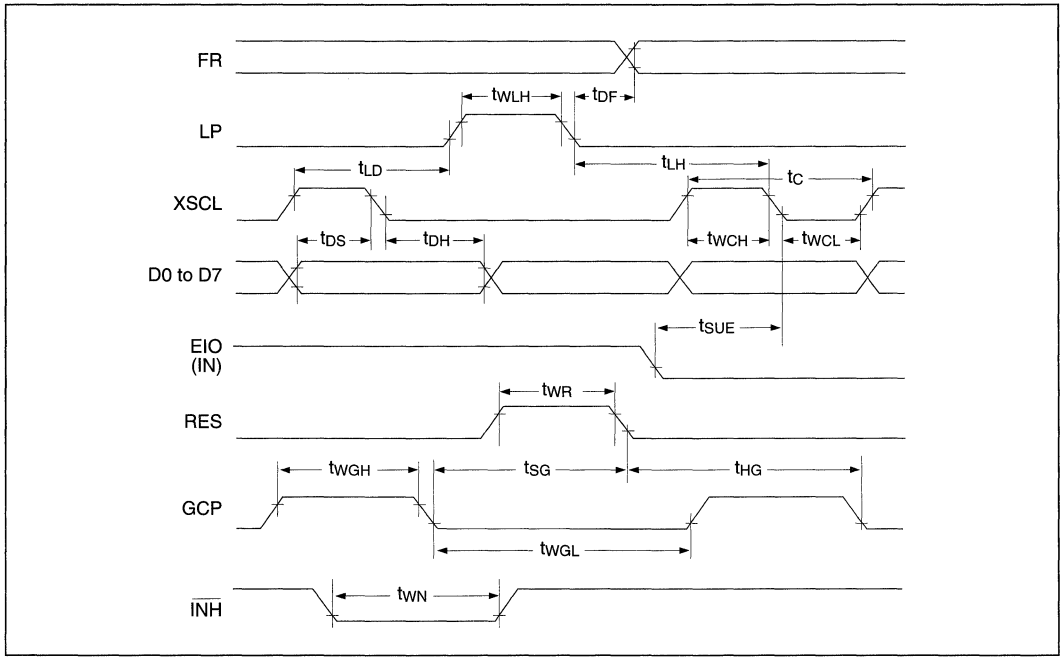
T_a=–20 to 75°C, V5=0V, unless stated otherwise

Parameter	Symbol	Condition	Pin	Rating			Unit
				Min	Typ	Max	
Supply voltage (1)	V_{CC}		V_{CC}	4.5	5.0	5.5	V
Supply voltage (2)	V_{DDH}		V_{DDH}	14.0	—	40.0	V
Input voltage	V0	V0≥V2≥V3≥V5	V0	V_{DDH}–2.5	—	V_{DDH}	V
Input voltage (1)	V2		V2	7/9×V_{DDH}	—	V_{DDH}	V
Input voltage (2)	V3, V5		V3, V5	GND	—	2.9×V_{DDH}	V
HIGH–level input voltage	V_{IH}		All input pins.	0.8×V_{CC}	—	V_{CC}	V
LOW-level input voltage	V_{IL}			GND	—	0.2×V_{CC}	V
HIGH-level output voltage	V_{OH}	I_{OH}=–0.4 mA	EIO1, EIO2	V_{CC}–0.4	—	V_{CC}	V
LOW-level output voltage	V_{OL}	I_{OH}=0.4 mA		GND	—	0.4	V
Input leakage current	I_{LI}	GND≤V_I≤V_{CC}	All pins except EIO.	—	—	2.0	µA
I/O leakage current	$I_{LI/O}$	GND≤V_I≤V_{CC}	EIO1, EIO2	—	—	5.0	µA
Quiescent current	I_{GND}	V_{DDH}=14.0 to 40.0 V, V_{IH}=V_{CC}, V_{IL}=GND	GND	—	—	25	µA
Segment output ON resistance See note 1.	R_O	V_{ON}=0.5V, V_{DDH}=10.0V	O0 to O159	—	2.0	6.5	kΩ
		V_{DDH}=20.0V		—	1.5	3.5	
		V_{DDH}=30.0V		—	1.3	3.0	
Operating current (1)	I_{CC}	V_{CC}=5.0V, V_{IH}=V_{CC}, V_{IL}=GND, f_{XSCL}=10.8MHz, f_{LP}=33.8kHz, f_{GCP}=0.54 MHz, FR=70 Hz, D0 to D7=F0F0..., alternating	V_{CC}	—	2.5	5.0	mA
Operating current (2)	I_{DDH}	V_{CC} = 5.0V, V5 = 0V, V3 = 4V, V2 = 26V, V0 = V_{DDH} = 30V, other conditions same as I_{CC}	V_{DDH}	—	0.5	1.2	mA
Input capacitance See note 2.	C_1	T_a=25°C, Freq.=1 MHz	All pins except E1O	—	—	8.0	pF
I/O capacitance See note 2.	$C_{I/O}$	T_a=25°C, Freq.=1 MHz	EIO1, EIO2	—	—	15.0	pF

Notes: 1. Within the specified ranges of V0, V2, V3 and V4.
2. Chip package only.

● AC Characteristics

○ Input Timing



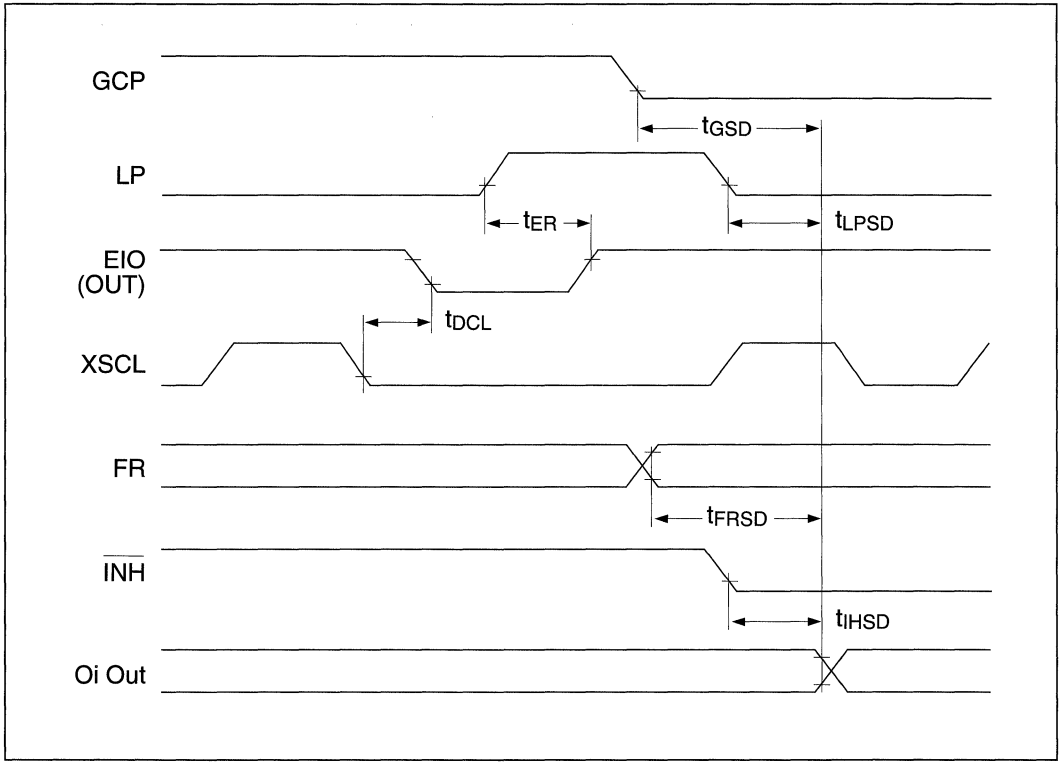
Note: For timing of LP pulse input, omit one XSCL clock cycle.

T_a=–20 to 75°C, V_{CC}=5.0V±10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Shift clock period	tC	IC operating alone	62	—	—	ns
		Using enable transfer function	83	—	—	
Shift clock HIGH-level pulsewidth	tWCH		25	—	—	ns
Shift clock LOW-level pulsewidth	tWCL		25	—	—	ns
EIO setup time	tSUE		36	—	—	ns
Data setup time	tDS		30	—	—	ns
Data hold time	tDH		20	—	—	ns
Shift clock to latch pulse interval	tLD		0	—	—	ns
Latch hold time	tLH		200	—	—	ns
LP pulsewidth	tWLH	See note	80	—	—	ns
RES pulsewidth	tWR		100	—	—	ns
$\overline{\text{INH}}$ pulsewidth	tWN		100	—	—	ns
GCP HIGH-level pulsewidth	tWGH		80	—	—	ns
GCP LOW-level pulsewidth	tWGL		80	—	—	ns
FR delay time	tDF		–300	—	+300	ns
GCP setup time	tSG	Applicable to	200	—	—	ns
GCP hold time	tHG	LP and RES signal	200	—	—	ns

Note: tWLP indicates the time XSLC is LOW as well as the time that LP is HIGH.

● **Output Timing**

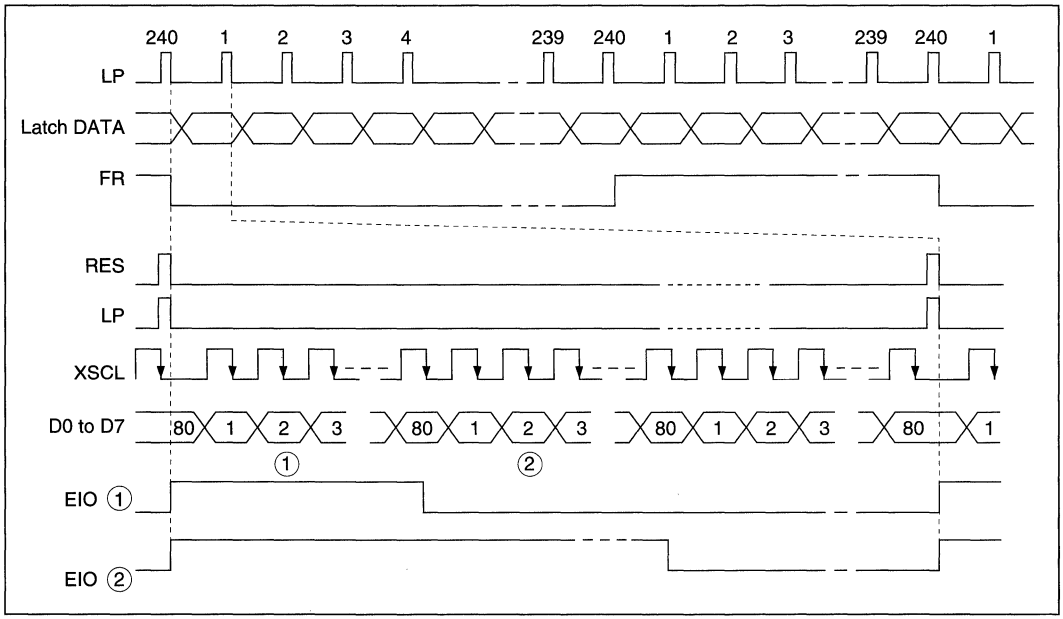


V_H=0.8xV_{CC}, V_L=0.2xV_{CC}, T_a=–20 to 75°C, V_{DDH}=14.0 to 40.0V unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
EIO output reset time	t_{ER}	C_L=15 pF	—	—	120	ns
EIO output delay time	t_{DCL}		—	—	45	
LP to segment output delay time	t_{LPSD}	C_L=100 pF	—	—	0.6	µs
FR to segment output delay time	t_{FRSD}		—	—	0.8	µs
$\overline{INH}$ to segment output delay time	t_{IHSD}		—	—	0.6	µs
GCP to segment output delay time	t_{GSD}		—	—	0.6	µs

● Timing Diagrams

○ 1/240 Duty Cycle



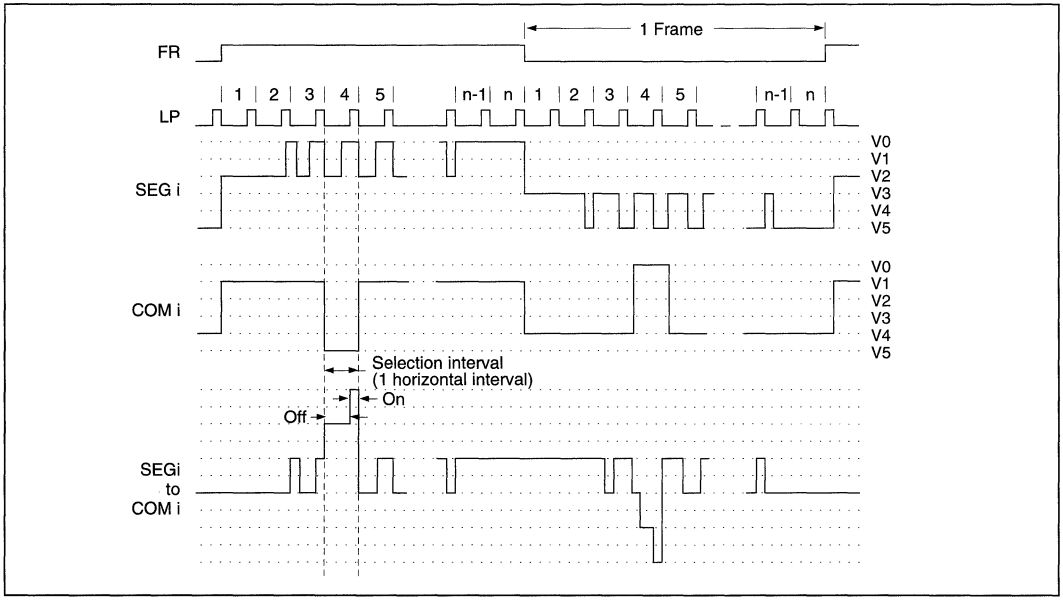
V_H=0.8xV_{CC}

V_L=0.2xV_{CC}

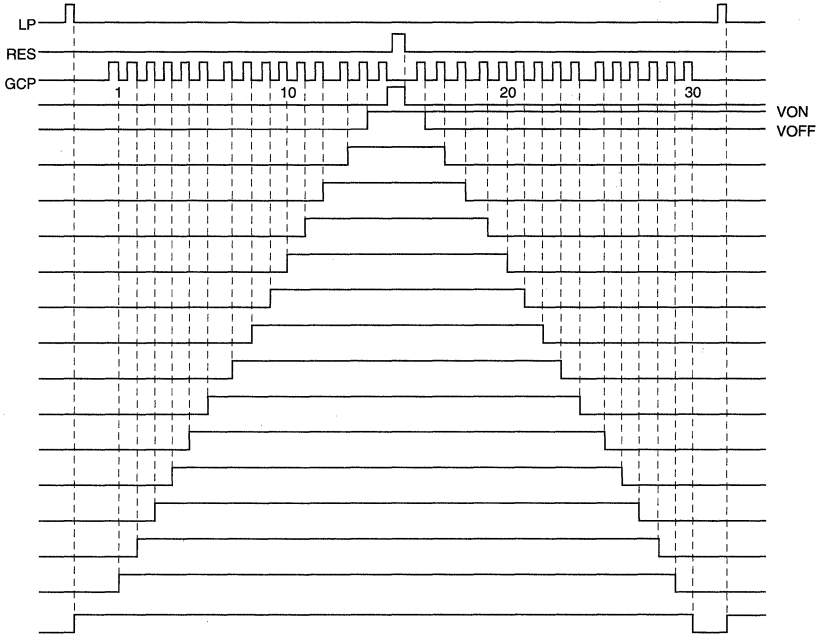
Notes:

1. Circled numerals denote the position of the device in the cascade chain.
2. With high-speed data transfer, it is necessary to delay the transition of XSCL following the LP pulse falling edge, to ensure that the minimum LP to XSCL time specification is met.

○ 16-level gray-scale data and LCD output waveforms



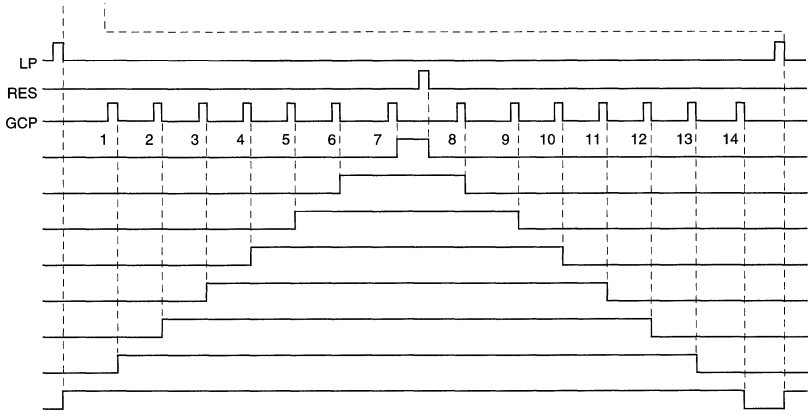
Gray scale	Gray scale data			
	D3	D2	D1	D0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1



Note: (D0, D1, D2, D3) also refer to (D4, D5, D6, D7)

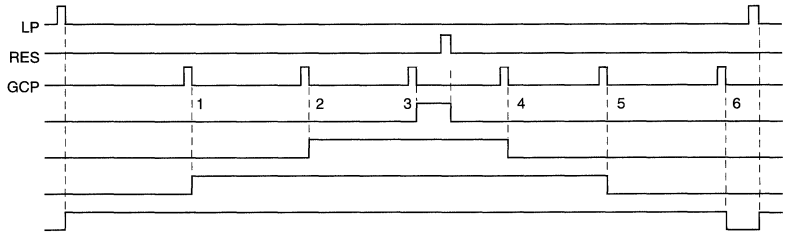
○ 8-level gray-scale data and LCD output waveforms

Gray scale	Gray scale data			
	D3	D2	D1	D0
0	1	0	0	0
1	1	0	0	1
2	1	0	1	0
3	1	0	1	1
4	1	1	0	0
5	1	1	0	1
6	1	1	1	0
7	1	1	1	1



○ 4-level gray-scale data and LCD output waveforms

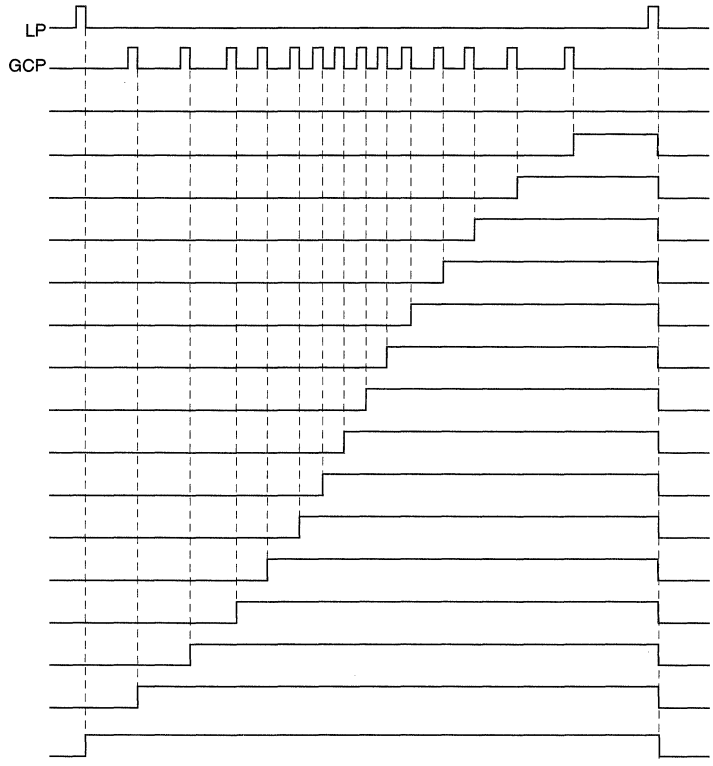
Gray scale	Gray scale data			
	D3	D2	D1	D0
0	1	1	0	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1



Note: The segment outputs change state on the falling edge of the fifteenth GCP pulse following an LP or RES pulse, regardless of the value of the gray-scale data.

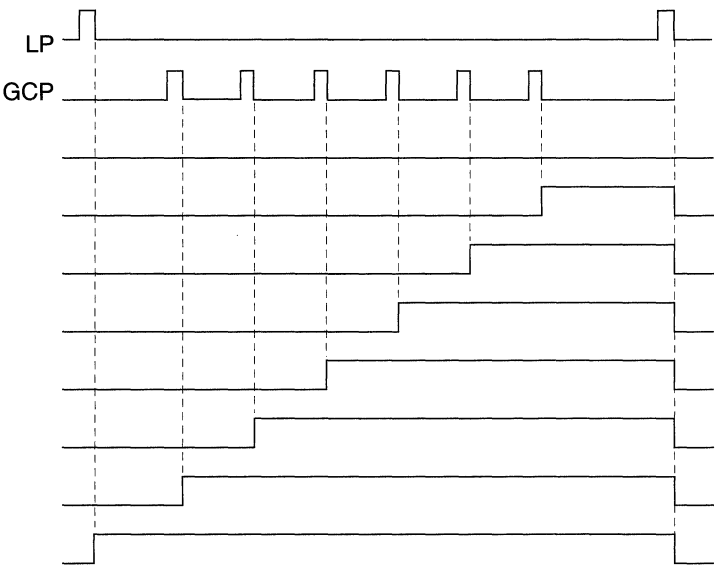
○ **Right-hand PWM mode 16-level gray-scale data and LCD output waveforms**

Gray scale	Gray scale data			
	D3	D2	D1	D0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1



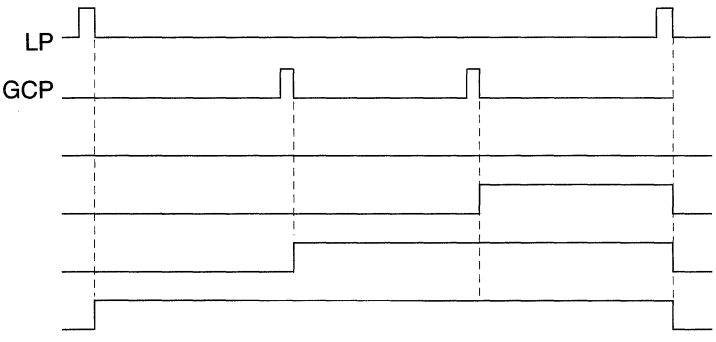
○ **Right-hand PWM mode 8-level gray-scale data and LCD output waveforms**

Gray scale	Gray scale data			
	D3	D2	D1	D0
0	1	0	0	0
1	1	0	0	1
2	1	0	1	0
3	1	0	1	1
4	1	1	0	0
5	1	1	0	1
6	1	1	1	0
7	1	1	1	1



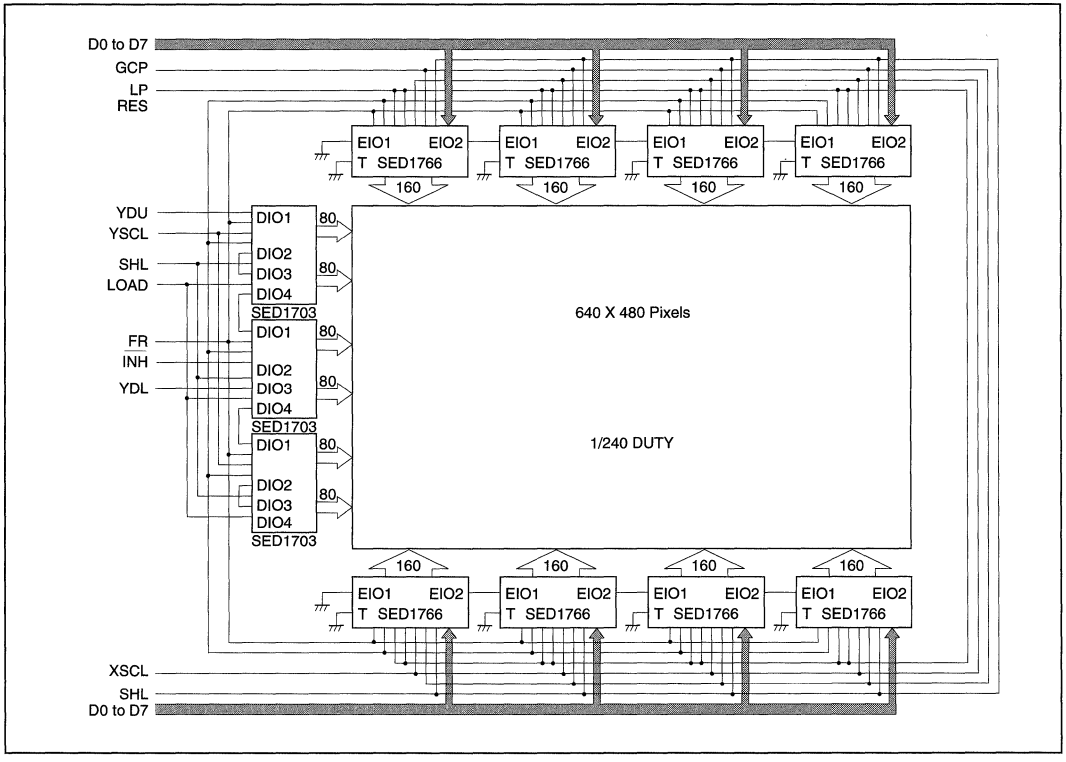
○ **Right-hand PWM mode 4-level gray-scale data and LCD output waveforms**

Gray scale	Gray scale data			
	D3	D2	D1	D0
0	1	1	0	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1

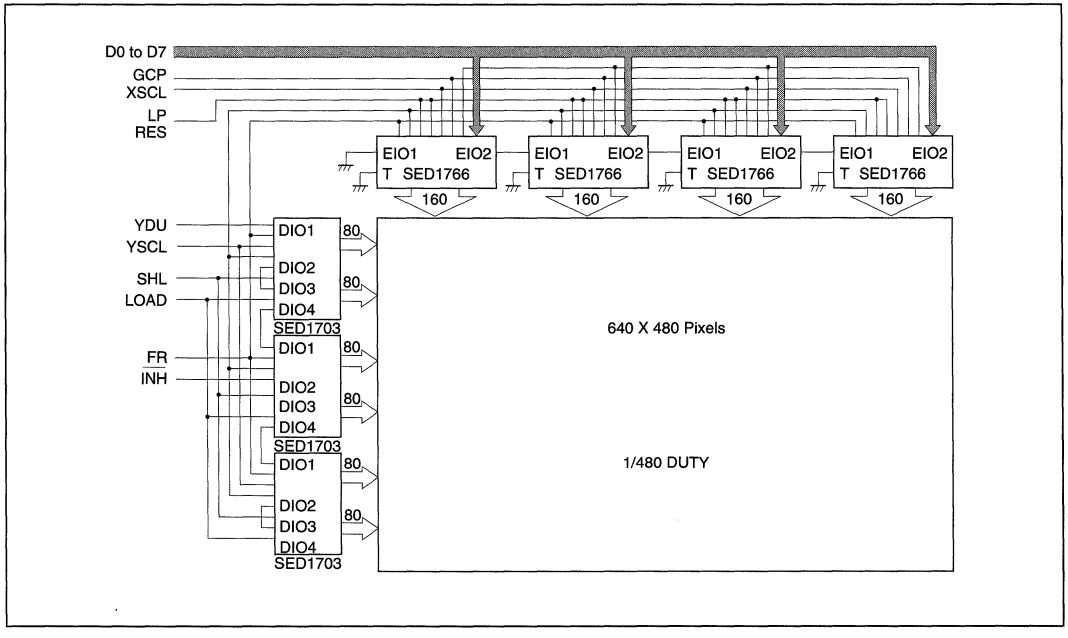


■ TYPICAL APPLICATION CIRCUITS

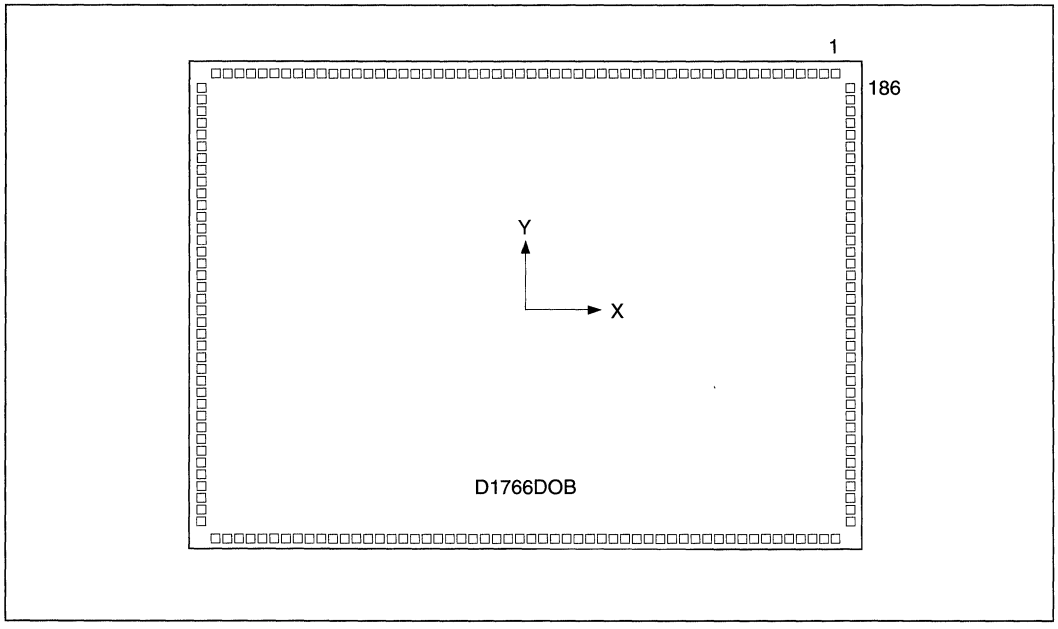
● Large-screen LCD, 1/240 duty cycle



● Large-screen LCD, 1/480 duty cycle



■ PAD LAYOUT (SED1766D0A and SED1766D0B)



Chip size: 8.80 × 5.62
Pad pitch: 0.134 mm min.

* Al pad (SED1766D0A)
  Chip thickness: 0.525 ± 0.025 mm
  Pad size, type A: 100 µm × 100 µm (All pads except 36, 37, 38, 39, 40)
  Pad size, type B: 160 µm × 100 µm (Pads 36, 37, 38, 39, 40)

* Au bump pad (SED1766D0B)
  Chip thickness: 0.525 mm ± 0.025 mm
  Pad size, type A: 102 µm × 100 µm ± 20 µm (All pads except 36, 37, 38, 39, 40)
  Pad size, type B: 186 µm × 100 µm ± 20 µm (Pads 36, 37, 38, 39, 40)

Note: Sizes are specified as x-dimension × y-dimension. X is parallel to the scribe-line.

■ PAD COORDINATES

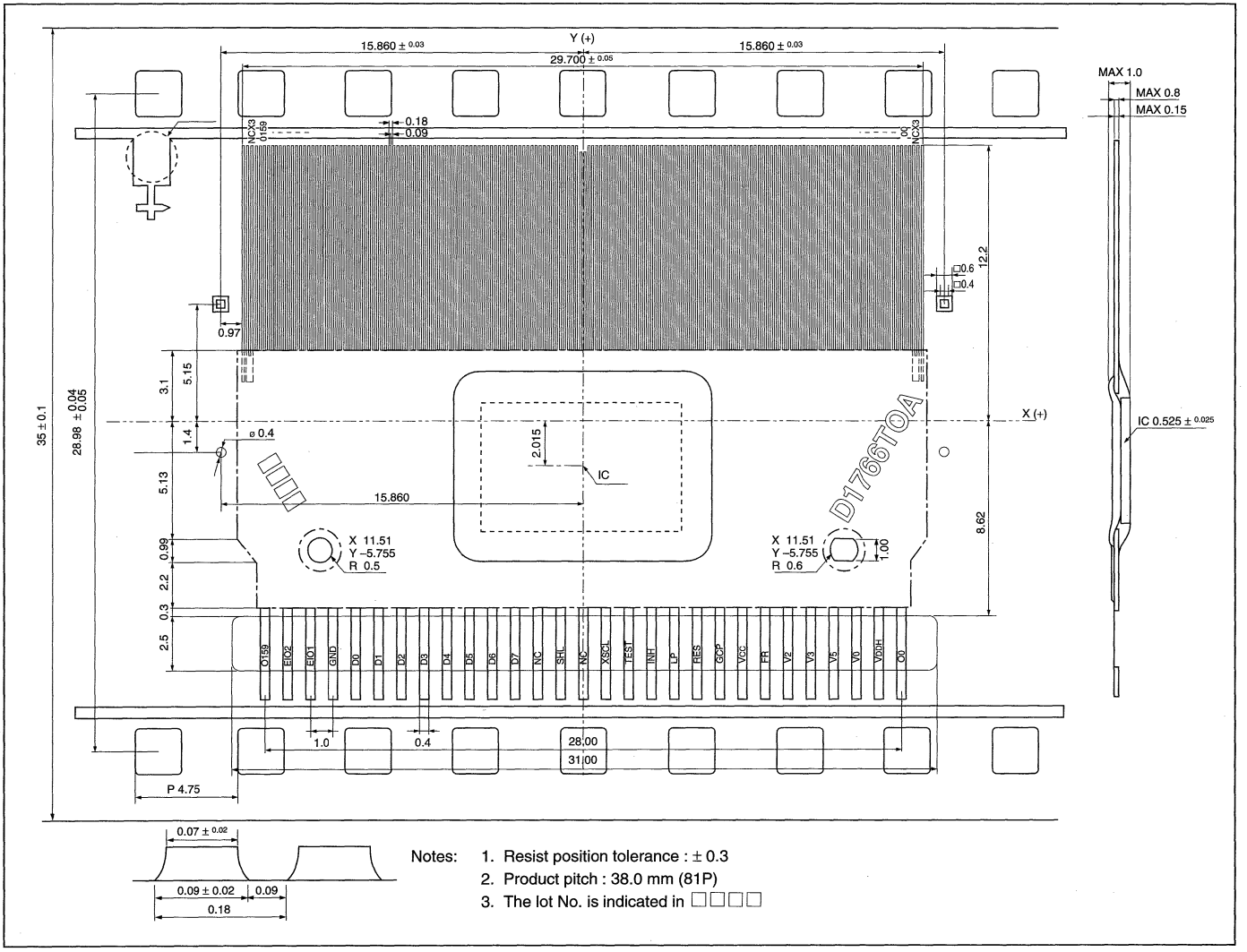
Pad		X	Y
Number	Name		
1	O146	3950	2643
2	O147	3814	2643
3	O148	3678	2643
4	O149	3542	2643
5	O150	3406	2643
6	O151	3270	2643
7	O152	3134	2643
8	O153	2998	2643
9	O154	2862	2643
10	O155	2726	2643
11	O156	2590	2643
12	O157	2454	2643
13	O158	2318	2643
14	O159	2182	2643
15	EIO2	1998	2643
16	EIO1	1858	2643
17	GND	1718	2643
18	D0	1578	2643
19	D1	1438	2643
20	D2	1298	2643
21	D3	1158	2643
22	D4	1018	2643
23	D5	878	2643
24	D6	738	2643
25	D7	598	2643
26	NC	458	2643
27	SHL	318	2643
28	XSCL	178	2643
29	TEST	38	2643
30	$\overline{INH}$	–102	2643
31	LP	–242	2643
32	RES	–382	2643
33	GCP	–522	2643
34	V_{CC}	–662	2643
35	FR	–802	2643
36	V2	–1032	2643
37	V3	–1262	2643
38	V5	–1492	2643
39	V0	–1722	2643
40	V_{DDH}	–1952	2643
41	O0	–2182	2643
42	O1	–2318	2643
43	O2	–2454	2643
44	O3	–2590	2643
45	O4	–2726	2643
46	O5	–2862	2643
47	O6	–2998	2643
48	O7	–3134	2643
49	O8	–3270	2643
50	O9	–3406	2643

Pad		X	Y
Number	Name		
51	O10	–3542	2643
52	O11	–3678	2643
53	O12	–3814	2643
54	O13	–3950	2643
55	O14	–4230	2379
56	O15	–4230	2243
57	O16	–4230	2107
58	O17	–4230	1971
59	O18	–4230	1835
60	O19	–4230	1699
61	O20	–4230	1563
62	O21	–4230	1427
63	O22	–4230	1291
64	O23	–4230	1155
65	O24	–4230	1019
66	O25	–4230	883
67	O26	–4230	747
68	O27	–4230	611
69	O28	–4230	475
70	O29	–4230	339
71	O30	–4230	203
72	O31	–4230	67
73	O32	–4230	–69
74	O33	–4230	–205
75	O34	–4230	–341
76	O35	–4230	–477
77	O36	–4230	–613
78	O37	–4230	–749
79	O38	–4230	–885
80	O39	–4230	–1021
81	O40	–4230	–1157
82	O41	–4230	–1293
83	O42	–4230	–1429
84	O43	–4230	–1565
85	O44	–4230	–1701
86	O45	–4230	–1837
87	O46	–4230	–1973
88	O47	–4230	–2109
89	O48	–4230	–2245
90	O49	–4230	–2381
91	O50	–3954	–2643
92	O51	–3820	–2643
93	O52	–3686	–2643
94	O53	–3552	–2643
95	O54	–3418	–2643
96	O55	–3284	–2643
97	O56	–3150	–2643
98	O57	–3016	–2643
99	O58	–2882	–2643
100	O59	–2748	–2643

Pad		X	Y
Number	Name		
101	O60	–2614	–2643
102	O61	–2480	–2643
103	O62	–2346	–2643
104	O63	–2212	–2643
105	O64	–2078	–2643
106	O65	–1944	–2643
107	O66	–1810	–2643
108	O67	–1676	–2643
109	O68	–1542	–2643
110	O69	–1408	–2643
111	O70	–1274	–2643
112	O71	–1140	–2643
113	O72	–1006	–2643
114	O73	–872	–2643
115	O74	–738	–2643
116	O75	–604	–2643
117	O76	–470	–2643
118	O77	–336	–2643
119	O78	–202	–2643
120	O79	–68	–2643
121	O80	68	–2643
122	O81	202	–2643
123	O82	336	–2643
124	O83	470	–2643
125	O84	604	–2643
126	O85	738	–2643
127	O86	872	–2643
128	O87	1006	–2643
129	O88	1140	–2643
130	O89	1274	–2643
131	O90	1408	–2643
132	O91	1542	–2643
133	O92	1676	–2643
134	O93	1810	–2643
135	O94	1944	–2643
136	O95	2078	–2643
137	O96	2212	–2643
138	O97	2346	–2643
139	O98	2480	–2643
140	O99	2614	–2643
141	O100	2748	–2643
142	O101	2882	–2643
143	O102	3016	–2643
144	O103	3150	–2643
145	O104	3284	–2643
146	O105	3418	–2643
147	O108	3552	–2643
148	O107	3686	–2643
149	O108	3820	–2643
150	O109	3954	–2643

Pad		X	Y
Number	Name		
151	O110	4230	–2381
152	O111	4230	–2245
153	O112	4230	–2109
154	O113	4230	–1973
155	O114	4230	–1837
156	O115	4230	–1701
157	O116	4230	–1565
158	O117	4230	–1429
159	O118	4230	–1293
160	O119	4230	–1157
161	O120	4230	–1021
162	O121	4230	–885
163	O122	4230	–749
164	O123	4230	–613
165	O124	4230	–477
166	O125	4230	–341
167	O126	4230	–205
168	O127	4230	–69
169	O128	4230	67
170	O129	4230	203
171	O130	4230	339
172	O131	4230	475
173	O132	4230	611
174	O133	4230	747
175	O134	4230	883
176	O135	4230	1019
177	O136	4230	1155
178	O137	4230	1291
179	O138	4230	1427
180	O139	4230	1563
181	O140	4230	1699
182	O141	4230	1835
183	O142	4230	1971
184	O143	4230	2107
185	O144	4230	2243
186	O145	4230	2379

■ EXTERNAL PACKAGE DIMENSIONS



Notes:
1. Resist position tolerance : ± 0.3
2. Product pitch : 38.0 mm (81P)
3. The lot No. is indicated in □□□□

SED1770/71

CMOS LCD DRIVER

■ DESCRIPTION

The SED1770 and the SED1771 are 160-bit output LCD segment (column) analog drivers for driving high-capacity active matrix LCD MIM- or TFT-type panels. These devices take 3-bit analog input (VA, VB, VC) which are (R, G, B) signals, and can support duty cycle higher than 1/100 (up to 1/500). Also, the LSI features a wide range of LCD voltages from 5 to 17V.

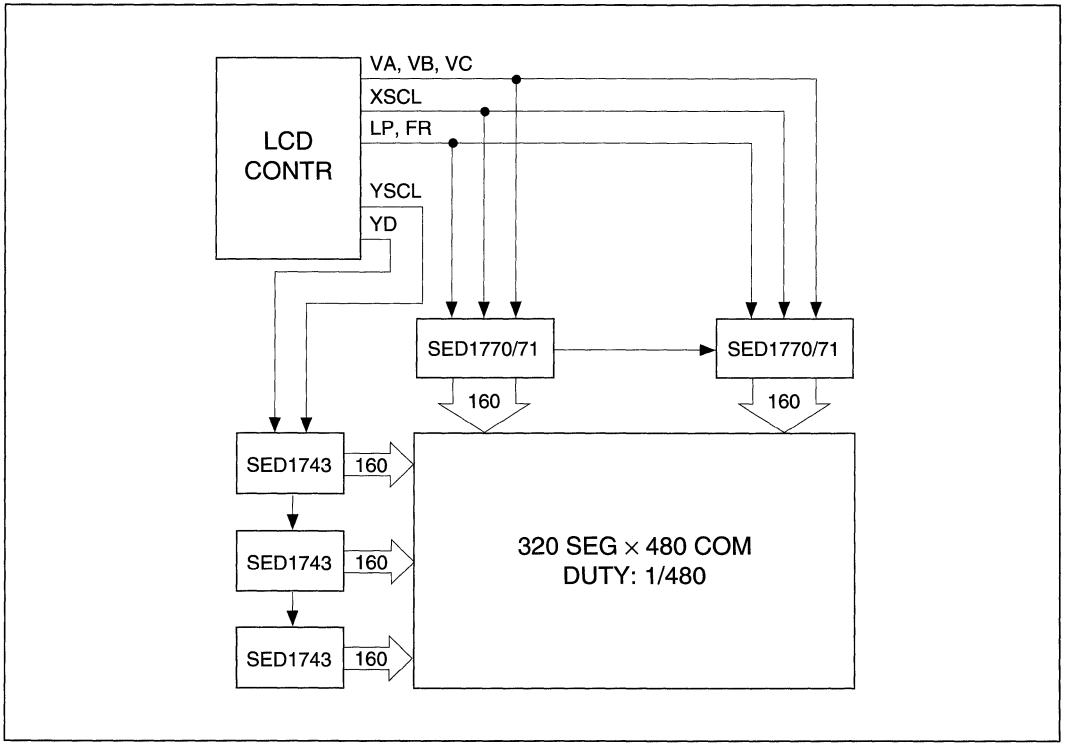
The device uses a high-speed daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1770/71 is used in conjunction with the SED1743F common drivers to support a large-capacity TFT/MIM active matrix LCD panel.

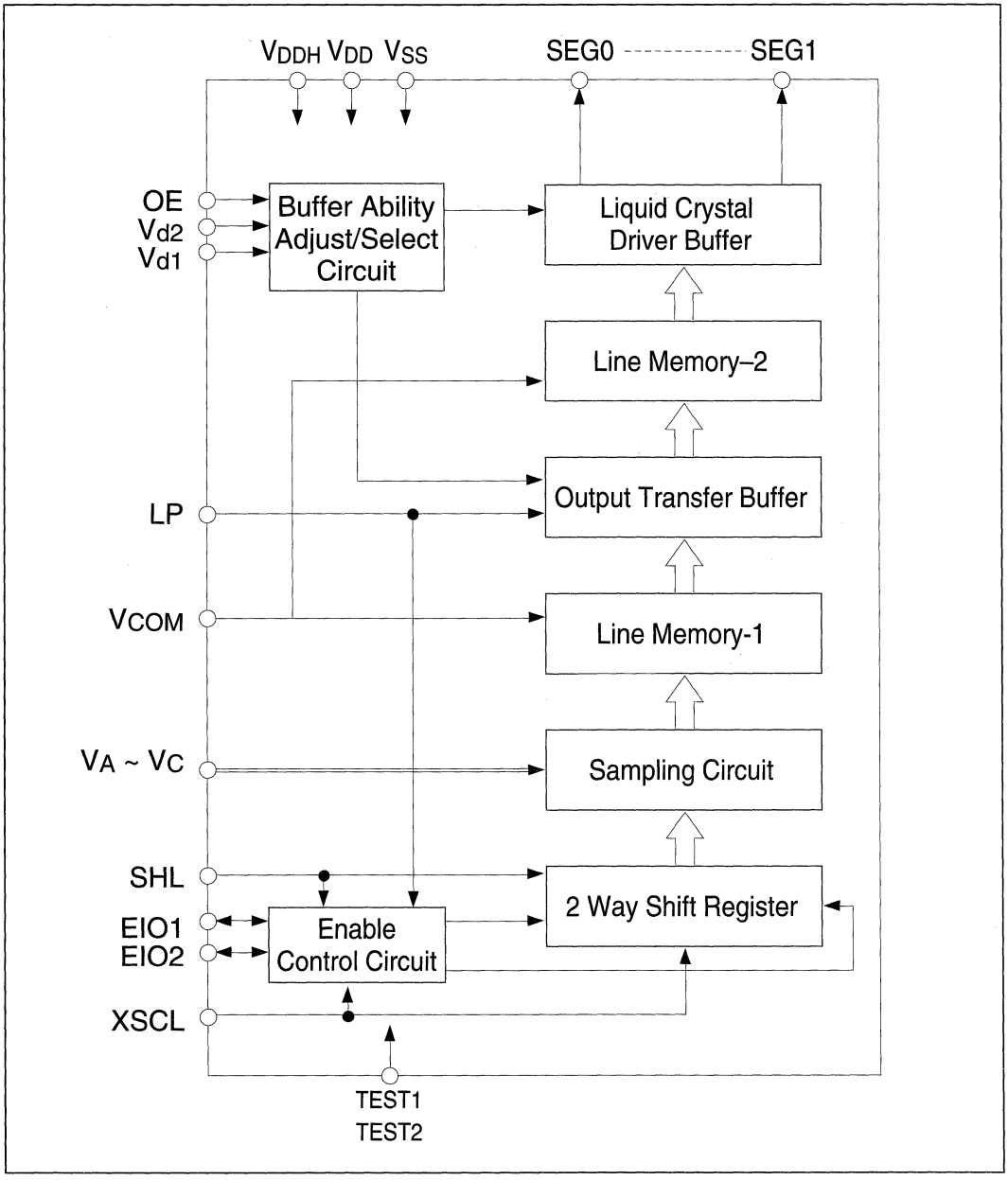
■ FEATURES

- Low-power, high-speed CMOS technology
- LCD driver output 160 (SED1770)
  162 (SED1771)
- High-speed data transfer 10MHz
- Support high-speed daisy-chain data transfer which reduces power consumption
- Takes 3-bit video inputs (VA, VB, VC)
- Built-in high-speed sampling circuitry
- Selectable output shift direction
- Low output resistance
- Wide range of LCD voltage .... 5 to 17V
- Supply voltage ..... 4.5 to 5.5V
- Package ..... TAB (2-sided)
  Al pad (DOA)

■ SYSTEM BLOCK DIAGRAM



■ **BLOCK DIAGRAM**



■ FUNCTIONS OF BLOCKS

● Enable control circuit

If the enable signal is in the disable status, the internal clock signal is fixed to "L" and placed in the POWER SAVE mode.

When using multiple segment drivers, the EIO terminals of the drivers should be cascade-connected while the EIO terminal of the front driver is connected to V_{SS}. In this case, the sampling of the front driver starts from XSCL's initial rising. As the enable control circuit automatically detects that sampling of data of the portion of 160 outputs has been finished thus automatically transferring the enable signal, the control signal by the control LSI is not necessary.

The EIO output is reset by LP input.

● Shift register

The shift register shifts the sampling signal by shift clock input. And it selects the shift direction by SHL input.

● Sampling circuit

The sampling circuit samples analog input signals sequentially by means of the sampling signals from the shift register. At this time, input/output are corresponded as follows: V_A with SEG0, 3, 6 --- 159; V_B with SEG1, 4, 7 ---157; and V_C with SEG2, 5, 8 --- 158.

● Line memory - 1

The line memory-1 stores the analog data sampled by the sampling circuit.

● Output transfer buffer

With the rising of LP, the output transfer buffer transfers the data of line memory-1 to line memory-2 and at the same time switches over to another liquid crystal drive output. When LP = H, make sure that XSCL = L. While sampling the data, make sure that LP = L. The ability of this buffer can be adjusted by V_{d1}.

● Line memory - 2

The line memory-2 holds the voltage of the liquid crystal drive output for the period until the next switching.

● Liquid crystal drive buffer

The crystal drive buffer outputs the liquid crystal drive voltage. The ability of this buffer can be adjusted by V_{d2} and switched over by OE.

● Buffer ability adjustment and switching circuit

This circuit performs two types of buffer ability adjustment and switching. The buffer abilities of both V_{d1} and V_{d2} reach their lowest level when they are equivalent to V_{DDH}; the respective abilities can be increased by lowering the electric potential, thus enabling them to cope with various liquid crystal panels.

The ability (output current) of the liquid crystal drive buffer is switched over by the OE to be used. With the time of writing data in the panel set at OE = "H", the large current is used to drive the buffer; after writing the data, the small current is used to drive the buffer at OE = "L". This not only improves the data write ability but also prevents the leakage of the hold time, thus making it possible to save power.

■ PIN DESCRIPTION

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Power</th><th>Number of Terminals</th></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Shift register data input/output;
Connected to the lower-stage EIO in cascade connection;
Changes at XSCL's rising edge</td><td>VDD
~
VSS</td><td>2</td></tr>
<tr><td>XSCL</td><td>I</td><td>Clock signal input;
Shift register operation at rising and falling edges</td><td>↑</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch signal input; switches the output data at rising edge.</td><td>↑</td><td>1</td></tr>
<tr><td>OE</td><td>I</td><td>Liquid crystal drive buffer ability switching signal input:
H: Large current drive
L: Small current drive</td><td>↑</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select signal input of shift register
<table>
<tr><th>SHL</th><th>EIO1</th><th>EIO2</th><th>SEG Output</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td><td>01-> 1 -> 2 --- -> 158 -> 159</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td><td>159 -> 158 -> --- -> 2 -> 1 -> 0</td></tr>
</table></td><td>↑</td><td>1</td></tr>
<tr><td>TEST1
TEST2</td><td>I</td><td>Test input: Normally L.
Pulldown is not built in.</td><td>↑</td><td>2</td></tr>
<tr><td>Vd1
Vd2</td><td>I</td><td>Buffer ability adjustment input:
The buffer ability for output transfer and that for liquid crystal drive can be varied by the voltage applied to the terminal.
Vd1: Output transfer buffer ability adjustment
Vd2: Liquid crystal drive buffer ability adjustment</td><td>VDDH
~
VSS</td><td>2</td></tr>
<tr><td>VA
VB
VC</td><td>I</td><td>Analog signal input:
Inputs image signals (R, G, and B).</td><td>↑</td><td>3</td></tr>
<tr><td>SEG0
~
SEG159*</td><td>O</td><td>Liquid crystal drive segment output:
Outputs the level, based on the analog signal input (VA, VB and VC) data as a sample holder.
The input/output are corresponded as
VA ->SEG0, 3, 6···, VB -> SEG1, 4, 7···, VC -> SEG2, 5, 8 ···.</td><td>↑</td><td>160</td></tr>
<tr><td>VCOM</td><td>I</td><td>Sample hold reference voltage input;
Reference power of the sample hold circuit;
To input the central electric potential of the analog signal input (VA, VB, VC) is the standard.</td><td>↑</td><td>1</td></tr>
<tr><td>VDDH</td><td>P</td><td>Power supply for high voltage LCD drive circuit.</td><td>—</td><td>2</td></tr>
<tr><td>VDD</td><td>P</td><td>Power supply for logic circuit.</td><td>—</td><td>1</td></tr>
<tr><td>VSS</td><td>P</td><td>LSI's common GND:
Shall be externally connected among VSS terminals.</td><td>—</td><td>3</td></tr>
</table>

(*) In the case of SED1771DOA, this is up to 162 outputs and SEG 162, and the number of terminals increases by two.

Total: 183 (NC 3)

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +25.0	V
Input voltage *1	V_{ID}	–0.3 to V_{DD}+0.3	V
Input voltage *2	V_{IA}	–0.3 to V_{DDH}+0.3	V
Storage temperature	T_{stg}	–65 to +150	°C
Operating temperature	T_{opr}	–20 to +75	°C

Notes: 1. Applies to EIO1, EIO2, XSCL, LP, OE, SHL, TEST1, and TEST2.
2. Applies to V_A, V_B, V_C, V_{d1}, V_{d2}, and V_{COM}.

● DC Characteristics

(V_{SS}=0V, V_{DD}=5V±10%, V_{DDH}=15V, and T_a= –20 to +75°C unless otherwise noted)

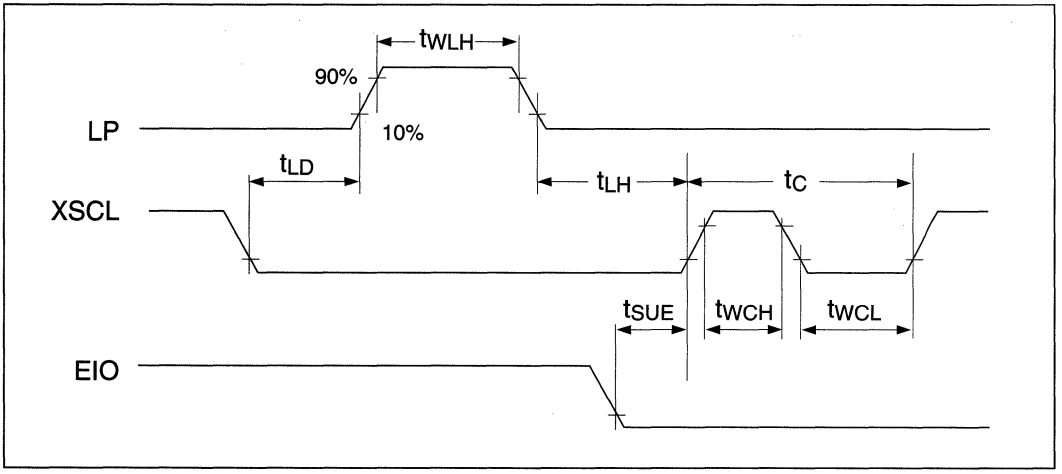
Parameter	Symbol	Condition	Applicable Signal	Rating Min	Rating Typ	Rating Max	Unit
Supply voltage (1)	V_{DD}		V_{DD}	4.5	—	5.5	V
Supply voltage (2)	V_{DDH}		V_{DDH}	V_{DD}	—	17.0	V
"H" input voltage	V_{IH}		*1	0.8•V_{DD}	—	V_{DD}	V
"L" input voltage	V_{IL}			V_{SS}	—	0.2•V_{DD}	V
Input terminal capacity	CID	T_a = 25°	*2	—	—	8.0	pF
Input leak current	ILID	0 < VI < V_{DD}		—	—	2.0	µA
"H" output voltage	V_{OH}	I_{OH} = –0.4mA	EIO1 EIO2	V_{DD}–0.4	—	V_{DD}	V
"L" output voltage	V_{OL}	I_{OL} = 0.4mA		V_{SS}	—	0.4	V
Input/output terminal capacity	CI/O	T_a = 25°C		—	—	15.0	pF
Input/output leak current	ILI/O	0 < VI < V_{DD}		—	—	15.0	µA
Analog input voltage	V_{video}		V_A, V_B, V_C	V_{SS}+1.5	—	V_{DDH}–1.5	V
Analog input capacity	CIA			—	—	80	pF
Between-output voltage deviation	dVO		SEG 0 ~ SEG 161	MAX – MIN = 100			mV
Input/output gain	G_V			95	—	105	%
"1" output current	I_{OH}	*3		—	0.1	—	mA
"0" output current	I_{OL}	*4		—	0.1	—	mA
Current consumption (1)	I_{DD}	*5	—	—	—	5	mA
Current consumption (2)	I_{DDH}	*5	—	—	—	15	mA

Notes: 1. EIO1, EIO2, XSCL, LP, OE, SHL, TEST1, TEST2
2. XSCL, LP, OE, SHL, TEST1, TEST2
3. Vd2 = 12V, V_{video} = 13V, OE = H
4. Vd2 = 12V, V_{video}=2V, OE=H
5. f_{XSCL} = 10MHz, 1H = 63.5µs, V_{video}=+2~+13V, TOE (OE=H) = 10µs, without load

● AC Characteristics

V_{SS} = 0V, V_{DD} = 5V±10%, V_{DDH} = 15V, and T_a = –20 to +75°C unless otherwise noted.

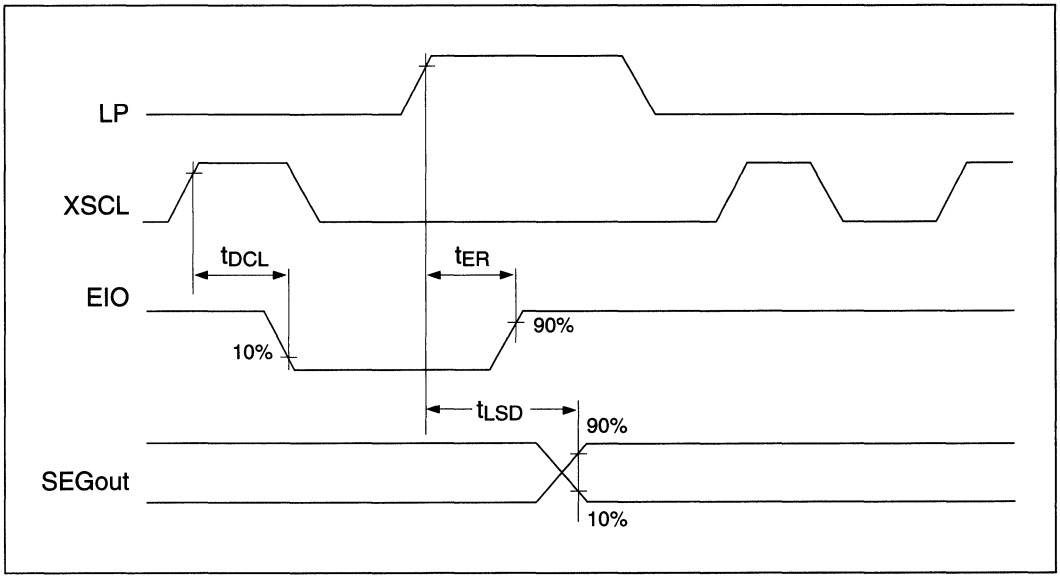
○ Input Timing Characteristics



Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
XSCL cycle	t_C		100	—	—	ns
XSCL "H" pulse width	t_{WCH}		40	—	—	ns
XSCL "L" pulse width	t_{WCL}		40	—	—	ns
XSCL-to-LP rise time	t_{LD}		40	—	—	ns
LP pulse width	t_{WLH}	*1	2.5	—	—	µs
LP-to-XSCL time	t_{LH}		1	—	—	µs
EIO setup time	t_{SUE}		50	—	—	ns

Notes: 1. Time of XSCL=L and LP=H.

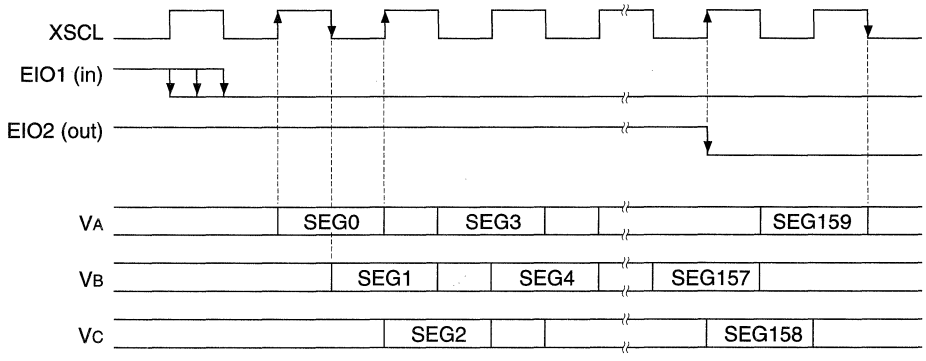
o Output Timing Characteristics



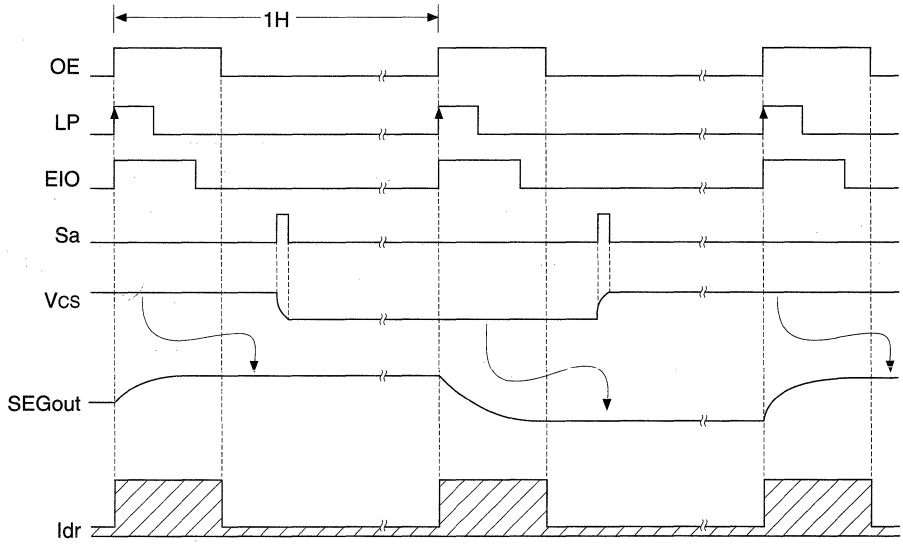
Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
EIO output delay time	t_{DCL}	CL = 15pF	—	—	40	ns
EIO output reset time	t_{ER}		—	—	12.0	ns
LP-to-SEGout delay time	t_{LSD}		Variable by V_{d1} and V_{d2}			
		*1	—	—	15	µs

Notes: 1. $V_{d1} = V_{d2} = 12V$, $V_{video} = 2 \sim 13V$, load capacity = 100pF, OE = "H".

● **Signal Timing Example (with specifications of SHL = H, 160 outputs, 1:1 correspondence)**



Sampling is started from the rising edge of the next XSCL after EIO1 has fallen.



Sa : Analog switch input of the sampling circuit
Vcs : Electric potential of the sampling capacitor
Idr : Size of the drive current

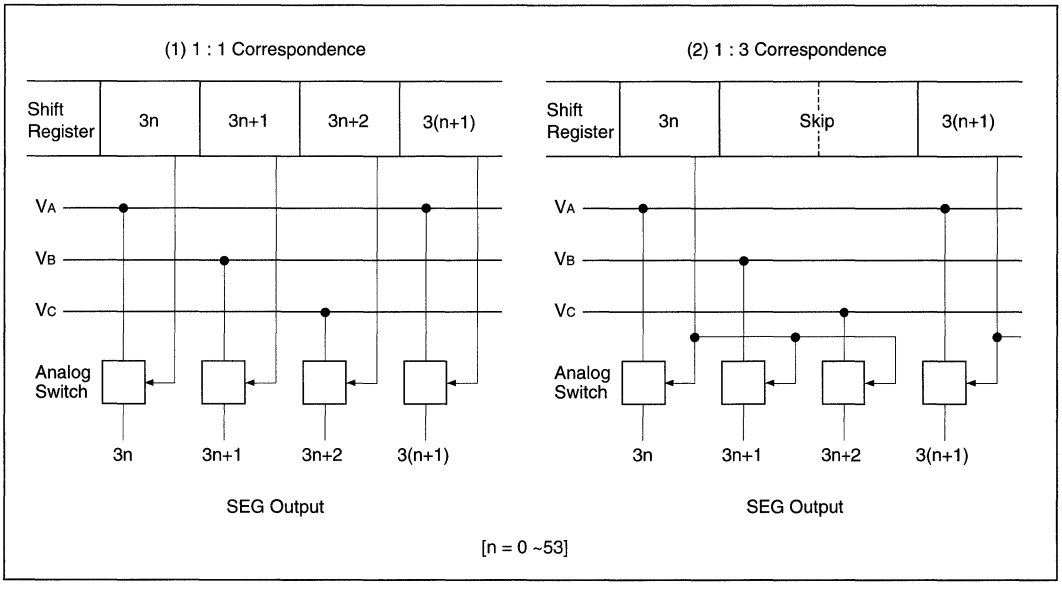
■ ALUMINUM MASTER SLICE OPTIONS

On this LSI, the following switchings are available by the aluminum master slice options.

- **Switching of number of output pins**
  (1) 160 outputs : Outputs EIO at the time of SEG158 sampling.
  At this time, the SEG160 and 161 terminals are placed in the NC status.
  (2) 162 outputs : Outputs EIO at the time of SEG160 sampling.

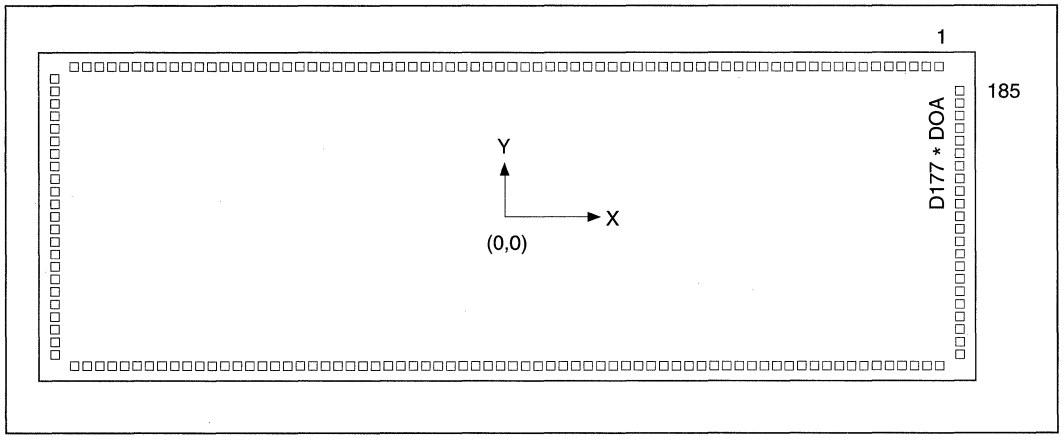
  Note: This applies if SHL = H. If SHL = L, the first output becomes SEG159 with (1), and SEG161 with (2).

- **Correspondence between the shift register and the sampling analog switch**
  (1) Shift registers and analog switches shall be corresponded at the ratio of 1:1.
  (2) One shift register stage shall be connected with three analog switches; and the shift register shall operate for every 3 stages.



- **Correspondence with product names**
  SED1770DOA: Selects 160 outputs for 1) and 1:1 correspondence for 1)
  SED1771DOA: Selects 162 outputs for 1) and 1:3 correspondence for 2)

■ PAD LAYOUT



	X	Y
Die size:	11.27mm	× 3.79mm
Pad pitch:	0.12mm (min)	

* Metallic bump specifications

Die thickness: 0.25mm ± 0.025mm

Bump Size	X Y	PAD No.
Bump size A	350μm × 150μm ± 20μm	23, 24, 28, 29, 30, 31
Bump size B	200μm × 150μm ± 20μm	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 32, 33, 34, 35, 36, 37
Bump size C	95μm × 150μm ± 20μm	Other than above

(The X in X and Y of the bump size shall be the direction parallel to the scribe line.)

■ PAD COORDINATES

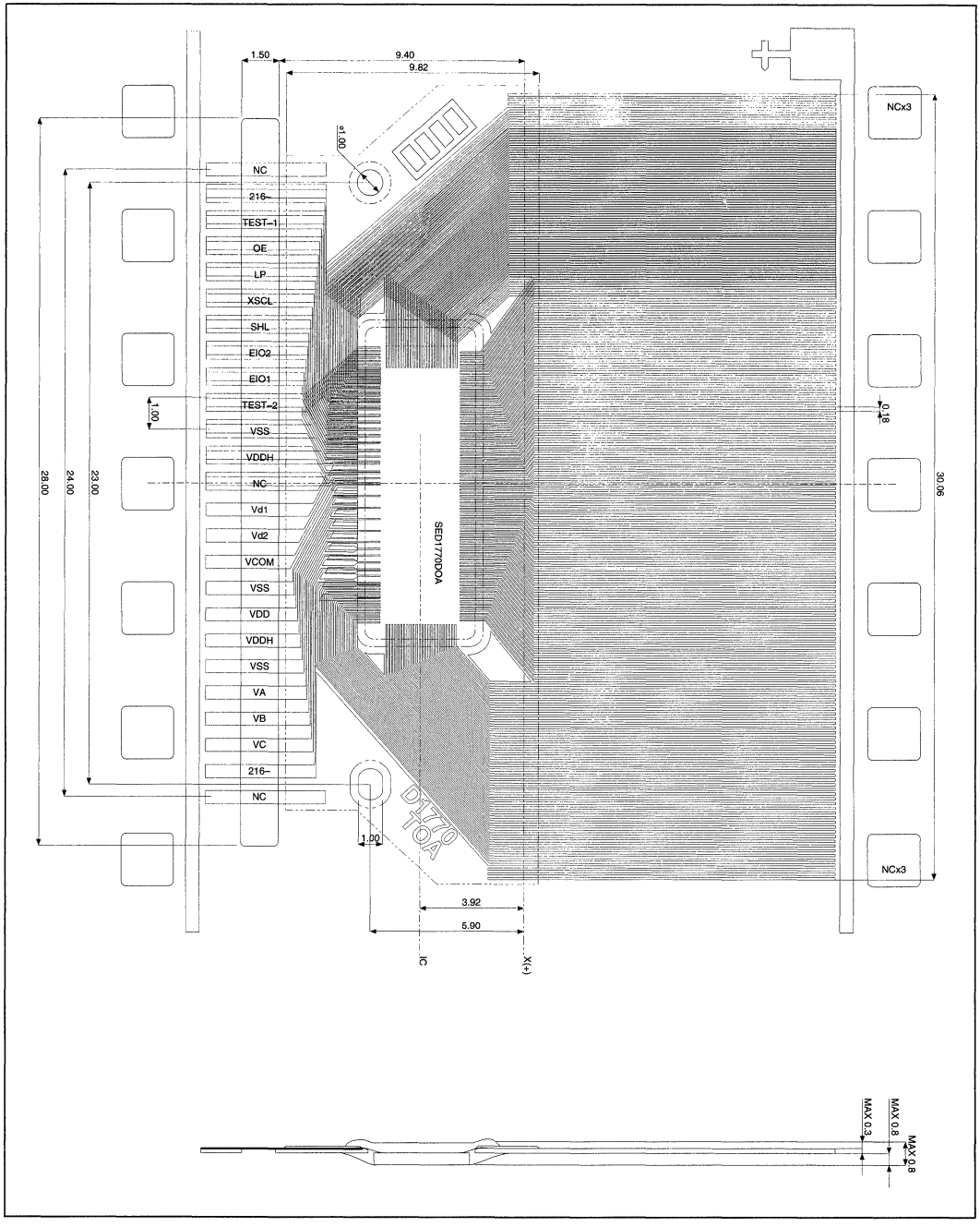
Unit = μm

Pad		X	Y	Pad		X	Y	Pad		X	Y
Number	Name			Number	Name			Number	Name		
1	SEG148	5210	1699	45	SEG7	–4490	1699	89	SEG51	–3540	–1699
2	SEG149	5090	1699	46	SEG8	–4610	1699	90	SEG52	–3420	–1699
3	SEG150	4970	1699	47	SEG9	–4730	1699	91	SEG53	–3300	–1699
4	SEG151	4850	1699	48	SEG10	–4850	1699	92	SEG54	–3180	–1699
5	SEG152	4730	1699	49	SEG11	–4970	1699	93	SEG55	–3060	–1699
6	SEG153	4610	1699	50	SEG12	–5090	1699	94	SEG56	–2940	–1699
7	SEG154	4490	1699	51	SEG13	–5210	1699	95	SEG57	–2820	–1699
8	SEG155	4370	1699	52	SEG14	–5436	1343	96	SEG58	–2700	–1699
9	SEG156	4250	1699	53	SEG15	–5436	1223	97	SEG59	–2580	–1699
10	SEG157	4130	1699	54	SEG16	–5436	1103	98	SEG60	–2460	–1699
11	SEG158	4010	1699	55	SEG17	–5436	983	99	SEG61	–2340	–1699
12	SEG159	3890	1699	56	SEG18	–5436	863	100	SEG62	–2220	–1699
13	SEG160*	3770	1699	57	SEG19	–5436	743	101	SEG63	–2100	–1699
14	SEG161*	3650	1699	58	SEG20	–5436	623	102	SEG64	–1980	–1699
15	TEST1	3400	1699	59	SEG21	–5436	503	103	SEG65	–1860	–1699
16	OE	3150	1699	60	SEG22	–5436	383	104	SEG66	–1740	–1699
17	LP	2900	1699	61	SEG23	–5436	263	105	SEG67	–1620	–1699
18	XSCL	2650	1699	62	SEG24	–5436	143	106	SEG68	–1500	–1699
19	SHL	2400	1699	63	SEG25	–5436	23	107	SEG69	–1380	–1699
20	EIO2	2150	1699	64	SEG26	–5436	–97	108	SEG70	–1260	–1699
21	EIO1	1900	1699	65	SEG27	–5436	–217	109	SEG71	–1140	–1699
22	TEST2	1650	1699	66	SEG28	–5436	–337	110	SEG72	–1020	–1699
23	V_{SS}	1270	1699	67	SEG29	–5436	–457	111	SEG73	–900	–1699
24	V_{DDH}	830	1699	68	SEG30	–5436	–577	112	SEG74	–780	–1699
25	V_{d1}	440	1699	69	SEG31	–5436	–697	113	SEG75	–660	–1699
26	V_{d2}	190	1699	70	SEG32	–5436	–817	114	SEG76	–540	–1699
27	VCOM	–60	1699	71	SEG33	–5436	–937	115	SEG77	–420	–1699
28	V_{SS}	–450	1699	72	SEG34	–5436	–1057	116	SEG78	–300	–1699
29	V_{DD}	–890	1699	73	SEG35	–5436	–1177	117	SEG79	–180	–1699
30	V_{DDH}	–1330	1699	74	SEG36	–5436	–1297	118	SEG80	–60	–1699
31	V_{SS}	–1770	1699	75	SEG37	–5436	–1417	119	SEG81	60	–1699
32	V_A	–2150	1699	76	SEG38	–5100	–1699	120	SEG82	180	–1699
33	(NC)	–2400	1699	77	SEG39	–4980	–1699	121	SEG83	300	–1699
34	V_B	–2650	1699	78	SEG40	–4860	–1699	122	SEG84	420	–1699
35	(NC)	–2900	1699	79	SEG41	–4740	–1699	123	SEG85	540	–1699
36	V_C	–3150	1699	80	SEG42	–4620	–1699	124	SEG86	660	–1699
37	(NC)	–3400	1699	81	SEG43	–4500	–1699	125	SEG87	780	–1699
38	SEG0	–3650	1699	82	SEG44	–4380	–1699	126	SEG88	900	–1699
39	SEG1	–3770	1699	83	SEG45	–4260	–1699	127	SEG89	1020	–1699
40	SEG2	–3890	1699	84	SEG46	–4140	–1699	128	SEG90	1140	–1699
41	SEG3	–4010	1699	85	SEG47	–4020	–1699	129	SEG91	1260	–1699
42	SEG4	–4130	1699	86	SEG48	–3900	–1699	130	SEG92	1380	–1699
43	SEG5	–4250	1699	87	SEG49	–3780	–1699	131	SEG93	1500	–1699
44	SEG6	–4370	1699	88	SEG50	–3660	–1699	132	SEG94	1620	–1699

Pad		X	Y	Pad		X	Y	Pad		X	Y
Number	Name			Number	Name			Number	Name		
133	SEG95	1740	–1699	151	SEG113	3900	–1699	169	SEG131	5436	–577
134	SEG96	1860	–1699	152	SEG114	4020	–1699	170	SEG132	5436	–457
135	SEG97	1980	–1699	153	SEG115	4140	–1699	171	SEG133	5436	–337
136	SEG98	2100	–1699	154	SEG116	4260	–1699	172	SEG134	5436	–217
137	SEG99	2220	–1699	155	SEG117	4380	–1699	173	SEG135	5436	–97
138	SEG100	2340	–1699	156	SEG118	4500	–1699	174	SEG136	5436	23
139	SEG101	2460	–1699	157	SEG119	4620	–1699	175	SEG137	5436	143
140	SEG102	2580	–1699	158	SEG120	4740	–1699	176	SEG138	5436	263
141	SEG103	2700	–1699	159	SEG121	4860	–1699	177	SEG139	5436	383
142	SEG104	2820	–1699	160	SEG122	4980	–1699	178	SEG140	5436	503
143	SEG105	2940	–1699	161	SEG123	5100	–1699	179	SEG141	5436	623
144	SEG106	3060	–1699	162	SEG124	5436	–1417	180	SEG142	5436	743
145	SEG107	3180	–1699	163	SEG125	5436	–1297	181	SEG143	5436	863
146	SEG108	3300	–1699	164	SEG126	5436	–1177	182	SEG144	5436	983
147	SEG109	3420	–1699	165	SEG127	5436	–1057	183	SEG145	5436	1103
148	SEG110	3540	–1699	166	SEG128	5436	–937	184	SEG146	5436	1223
149	SEG111	3660	–1699	167	SEG129	5436	–817	185	SEG147	5436	1343
150	SEG112	3780	–1699	168	SEG130	5436	–697				

(*) SEG160 and 161 become NC in the case of SED1770D0A

■ EXTERNAL PACKAGE DIMENSIONS



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SED17A0T

CMOS LCD SEGMENT DRIVER

■ DESCRIPTION

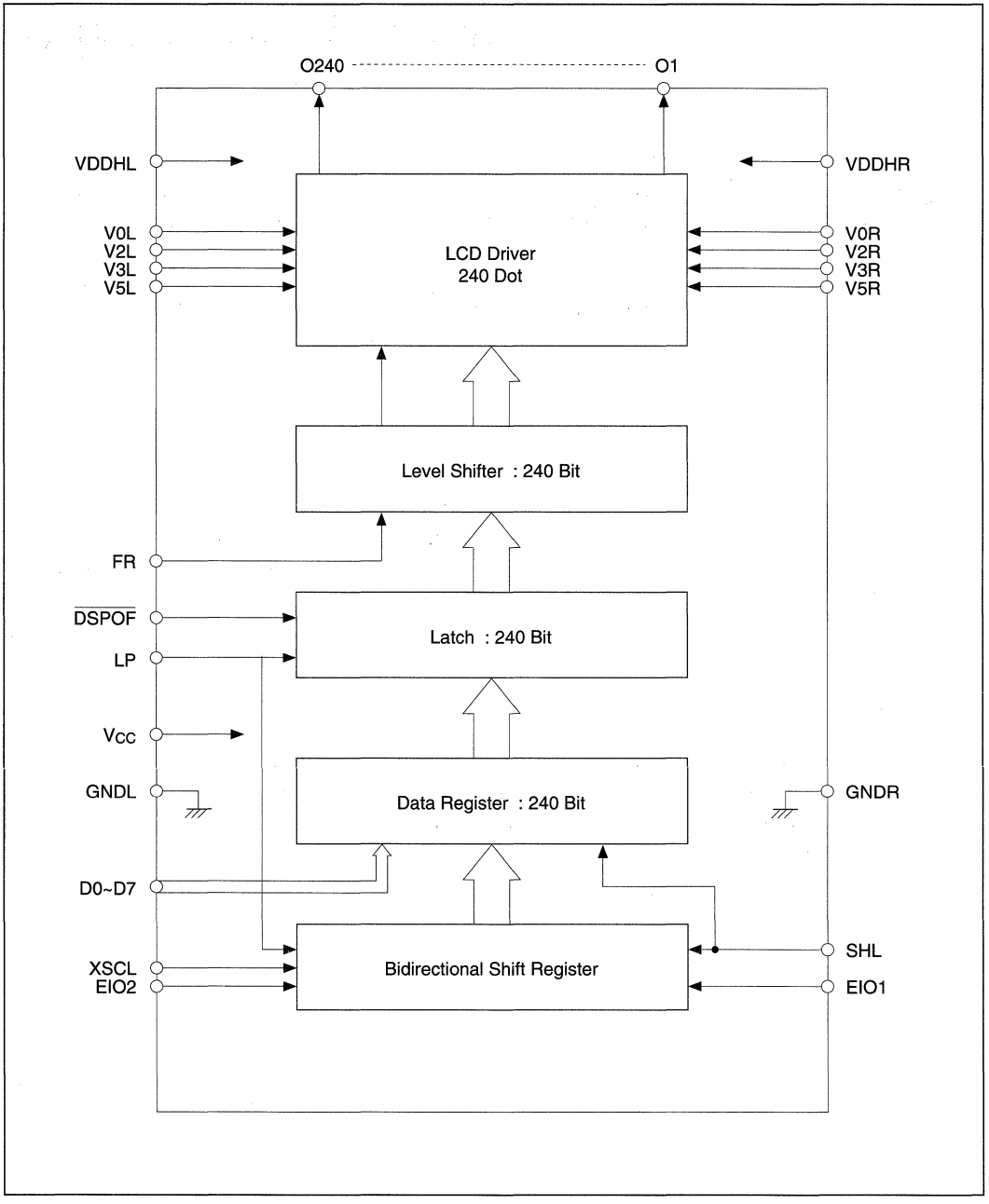
The SED17A0T is a segment LCD driver for dot-matrix STN liquid crystal display (LCDs). It incorporates 240 segment (column) driver outputs and is designed for use in conjunction with the SED1753 common (row) driver.

Contributing to making clearer LCD picture quality, this IC employs the high-speed enable chain method and is slim-chip configuration which is more advantageous for miniaturization of the LCD panel. SED17A0T is also capable of low-voltage and high-speed logic operations and fits to a wide range of applications.

■ FEATURES

- Number of LCD drive output segments 240
- Low voltage operation ..... 2.7V min.
- High duty drive ..... 1/500 (an example)
- Wide LCD drive voltage range ..... +8 to +42V (V_{DD} = 3 to 5.5V)
- High speed and low power consumption data transfer is possible by adoption of the 8-bit bus enable chain method:
  Shift clock frequencies: ..... 30.0MHz (5V±10%)
  20.0MHz (3.0V)
  18.0MHz (2.7V)
- Slim-chip configuration
- Non-bias display-off function
- Pin-selection of the output shift direction is available
- Offset bias regulation of LCD power for respective V_{DDH} and GND levels is possible
- Logic operation power supply ..... 2.7 to 5.5V
- Shipped status ..... TCP SED17A0T**
- This IC is not radiation resistant

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Numbers of Pins</th></tr>
<tr><td>O 1 ~
O 240</td><td>O</td><td>LCD driveing segment (column) output
The output varies at the falling edge of LP .</td><td>240</td></tr>
<tr><td>D0 ~ D7</td><td>I</td><td>Display data input terminals</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>For input of the shift clock signals of the display data
(Falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>For input of the latch pulse signals of the display data
(Falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O
Set to I or O is determined by the SHL input level.
The output is reset by the LP input and when 240 bit
equivalent data are recieved, it falls to “L” automatically</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift durection selection, and EIO terminal I/O control
signal input
When data are input to terminals D0, D1, ...D7
in order of F0, F1, ...F7 first, and in the order of
L0, L1, outputs are as follows is as follows:
F (First), L (Last)
<table>
<tr><th>SH</th><th colspan="7">Output</th><th colspan="2">EIO</th></tr>
<tr><td>L</td><td>0240</td><td>0239</td><td>0238</td><td></td><td>03</td><td>02</td><td>01</td><td>EIO1</td><td>EIO2</td></tr>
<tr><td>L</td><td>F7</td><td>F6</td><td>F5</td><td>....</td><td>L2</td><td>L1</td><td>L0</td><td>O</td><td>I</td></tr>
<tr><td>H</td><td>L0</td><td>L1</td><td>L2</td><td>....</td><td>F5</td><td>F6</td><td>F7</td><td>I</td><td>O</td></tr>
</table>
Note: The relation between the data and segment output are determined independently from the number of the shift clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>For input of alternating current LCD drive signals</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL,
GNDR</td><td>Power
supply</td><td>Logic operation power supply : GND: 0 V V_{CC}: +3, +5 V</td><td>3</td></tr>
<tr><td>V_{DDHL}, V_{DDHR}
V_{OL}, V_{OR}
V_{2L}, V_{2R}
V_{3L}, V_{3R}
V_{5L}, V_{5R}</td><td>Power
supply</td><td>LCD drive circuit power supply V_{DDH}
“ V0
“ V2
“ V3
“ V5</td><td>GND: 0 V, V_{DDH}: 14 –42V
$V_{DDH} \geq V_0 \geq V_2 \geq 7/9\ V_0$
$2/9\ V_0 \geq V_3 \geq V_5 \geq$ GND</td><td>10</td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>For forced bias fixed input
“L” level output is forcefully made to V5 level.
* When using this function, comvined use with SED1703
is not applicable</td><td>1</td></tr>
<tr><td></td><td></td><td>Total</td><td>268</td></tr>
</table>

■ FUNCTION OF EACH BLOCK

● Enable Shift Register

The enable shift register is a bidirectional shift register of which the shift direction is being selected by the SHL input and the shift register output is used to store data bus signals into the data register.

When the enable signal is in disabled state, the internal clock signal and the data bus are fixed to "L", thus going into a power saving mode.

When using multiple number of segment drivers, make cascade connection of EIO terminals of respective drivers to connect the EIO terminal of the top driver to "GND".

Since the enable control circuit automatically senses completion of receiving 240 bit equivalent data to transfer the enable signal automatically, control signal of a separate control LSI is not needed.

● Data Register

This register works to make series or parallel conversion of data bus signals according to the enable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independently from the number of shift clock inputs.

● Latch

It takes in the content of the data register at the falling edge trigger to transfer the output to the level shifter.

● Level Shifter

This is a level interface circuit to convert the voltage level of signals from the logic operation level to LCD drive level.

● LCD Driver

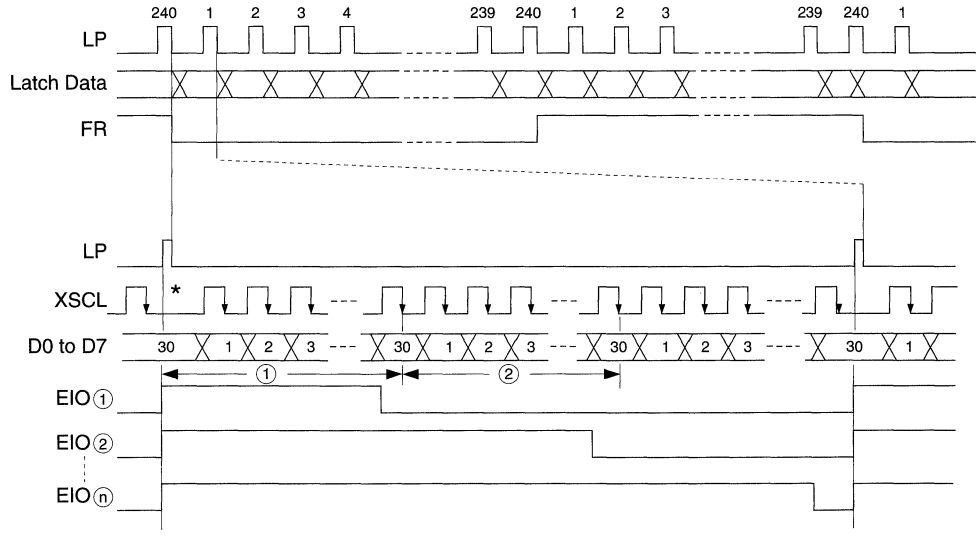
It outputs the LCD driving voltage.

Given below are the relations between data bus signals, alternating current signal FR levels and segment output voltages.

$\overline{DSPOF}$	Data Bus Signal	FR	Driver Output Voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_5

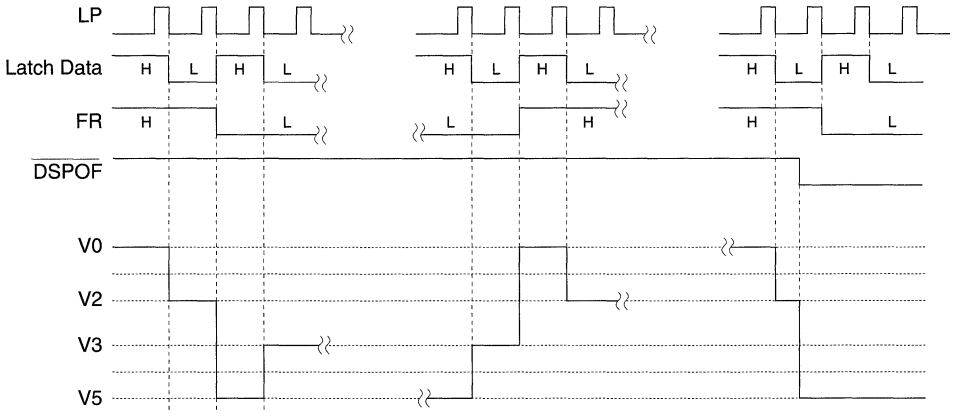
■ TIMING DIAGRAM

In case of 1/240 Duty (an example)



① to ⓝ stands for the cascade numbers of the driver.

* When making high speed data transfer, it becomes necessary to secure a longer XSCL cycle when determining the LP pulse insertion timing in order to maintain the specified value of LP → XSCL (t_{LH}).



■ ELECTRICAL CHARACTERISTICS

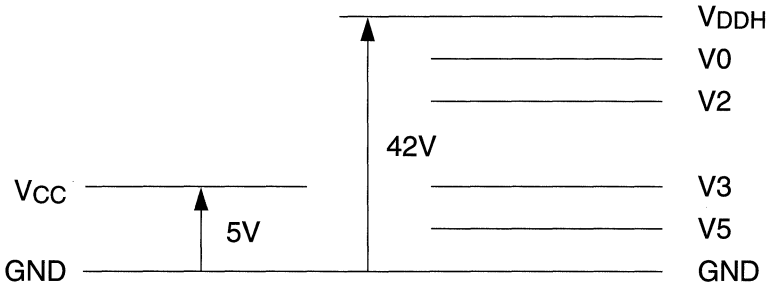
● Absolute Maximum Ratings

Parameters	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	–0.3 to V_{DDH} +0.3	V
Input voltage	V_I	–0.3 to V_{CC} +0.3	V
Output voltage	V_O	–0.3 V_{CC} +0.3	V
EIO output current	I_{O1}	20	mA
Working temperature	Topr	–30 to +85	°C
Storage temperature	Tstg	–55 to +100	°C

Note 1: All the voltage ratings are based on GND = 0V.

Note 2: The storage temperature 1 is applicable to independent chips and the storage temperature 2 is applicable to the TCP modular state.

Note 3: V_0, V_2, V_3 and V_5 should always be in the order of $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq GND$.



Note 4: If the logic operation power goes into a floating state or if V_{CC} drops to 2.6V or below while the LCD driving power is being applied, the LSI may be damaged. Therefore, keep from occurrence of the aforementioned status.
Specifically, pay close attention to the power supply sequence at times of turning the system power on and off.

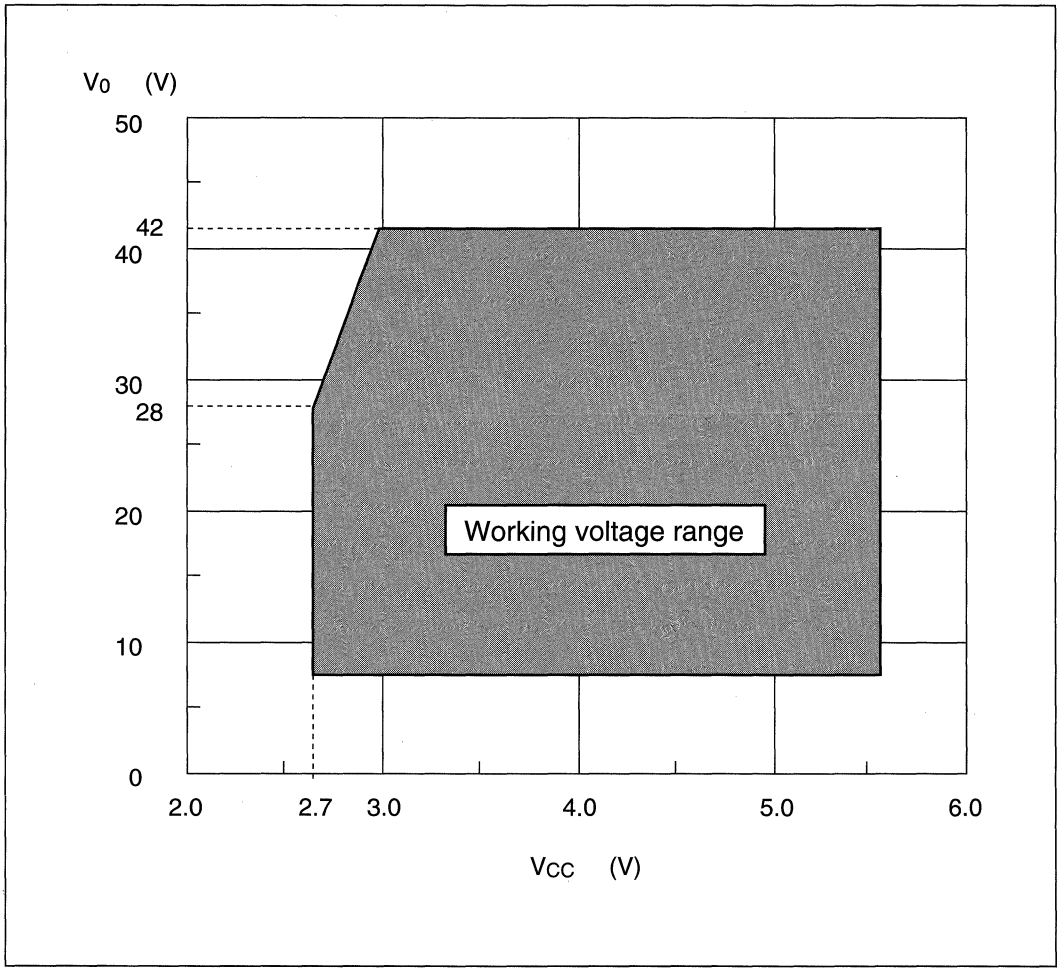
● DC Characteristics

Unless otherwise specified, GND = V5 = 0V, V_{CC} = +5.0V ± 10%, Ta = –30 to 85°C

Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}	—	V_{CC}	2.7	—	5.5	V
Recommended working voltage	V0	—	V0L, VDDHL	14.0	—	40.0	V
Workable voltage	V0	Function only	V0R, VDDHL	8.0	—	42.0	V
Supply voltage (2)	V_2	Recommended value	V2L, V2R	7/9 V_0	—	V_0	V
Supply voltage (3)	V_3	Recommended value	V3L, V3R	GND	—	2/9 V_0	V
High level input voltage	V_{IH}	V_{DD}= 2.7~5.5V	EIO1, EIO2, FR D0–D7, XSCL	0.8 V_{CC}	—	—	V
Low level input voltage	V_{IL}		SHL, LP, DSPOF	—	—	0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC} = 2.7 – 5.5V, I_{OH} = –0.6mA	EIO1, EIO2	V_{CC}–0.4	—	—	V
Low level output voltage	V_{OL}	V_{CC} = 2.7 – 5.5V, I_{OL} = 0.6mA		—	—	0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	D0–D7, LP, FR XSCL, SHL DSPOF	—	—	2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ GND	EIO1, EIO2	—	—	5.0	µA
Static current	IGND	V_0 = 14.0 ~ 42.0V, V_{IH} = GND, V_{IL} = GND	GND	—	—	25	µA
Output resistance	R_{SEG}	ΔV$_{ON}$ = 0.5V, V_0 = +36.0V, 1/24, O0–O240		—	0.80	1.1	KΩ
		Recommended condition, V_0 = +26.0V, 1/20		—	0.85	1.2	
In-chip deviation of output resistance	ΔR_{SEG}	ΔV$_{ON}$ = 0.5V, V_0 = +36.0V, 1/24, 01–0240		—	—	95	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} = 5.38MHz, f_{LP} = 33.6KHZ, f_{FR} = 70Hz, input data: Checkered indication, no-load	V_{CC}	—	0.75	1.7	mA
		V_{CC} = +3.0V, Other conditons are the same as those when V_{CC} + 5V.		—	0.3	0.9	
Mean working current consumption (2)	I_O	V_O = +30.0V, V_{CC} = +5.0V, V3 = +4.0V, V_2 = +26.0V, V5 = +0.0V, Other conditions are the same as those in the I_{CC} column	V_0	—	0.25	1.4	mA
Input terminal capacity	CI	Freq. = 1 Mhz, Ta = 25°C, Independent chips	D0~D7, LP, FR XSCL,SHL, DSPOF	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

- **Working Voltage Range V_{CC} – V_0**

The V_0 voltage should be set up within the V_{CC} – V_0 working voltage range given below.



- **AC Characteristics**
  - **Input Timing Characteristics**

Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	*2	33	—	ns
XSCL high level pulse duration	t_{WCH}	All timing signals are based on 20% and 80% of V_{CC}	9	—	ns
XSCL low level pulse duration	t_{WCL}		9	—	ns
Data setup time	t_{DS}		5	—	ns
Data hold time	t_{DH}		5	—	ns
XSCL → LP rise time	t_{LD}		–0	—	ns
LP → XSCL fall time	t_{LH}		25	—	ns
LP high level pulse duration	t_{WLH}	*1	15	—	ns
FR delay allowance	t_{DF}		-300	+300	ns
EIO setup time	t_{SUE}		5	—	ns
Input signal variation time	t_{r1}, t_{f1}	*3	—	50	ns
DSPOF signal variation time	fr_2, tf_2		—	100	ns

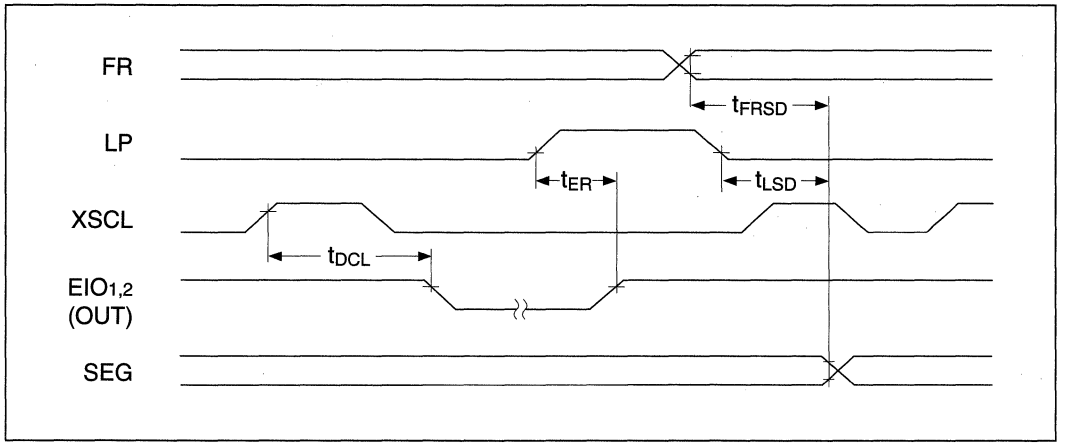
Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	V_{CC} = 3.0 to 4.5V	50	—	ns
		*2	55	—	ns
XSCL high level pulse duration	t_{WCH}	All timing signals are based on 20% and 80% of V_{CC}	15	—	ns
XSCL low level pulse duration	t_{WCL}		15	—	ns
Data setup time	t_{DS}		10	—	ns
Data hold time	t_{DH}		10	—	ns
XSCL → LP rise time	t_{LD}		–0	—	ns
LP → XSCL fall time	t_{LH}		30	—	ns
LP high level pulse duration	t_{WLH}	*1	25	—	ns
FR delay allowance	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		10	—	ns
Input signal variation time	t_r, t_f	*3	—	50	ns
DSPOF signal variation time	fr_2, tf_2		—	100	ns

Notes: *1. The "t_{WLH}" specifies the time when the LP is set at "H" and, at the same time, when XSCL is at "L", when LP is being input while XSCL is at "L".

*2. High speed operation of the shift clocks (XSCL) should only be made under a condition of $t_r + t_f \leq (t_C - t_{WCL} - t_{WCH})$.

*3. When the making high speed data transfer using conditions shift clocks, $t_r + t_f$ of the LP signals should be up to $(t_C + t_{WCH} - t_{LD} - t_{WLH} - t_{LH})$ at the maximum.

○ **Output Timing Characteristics**



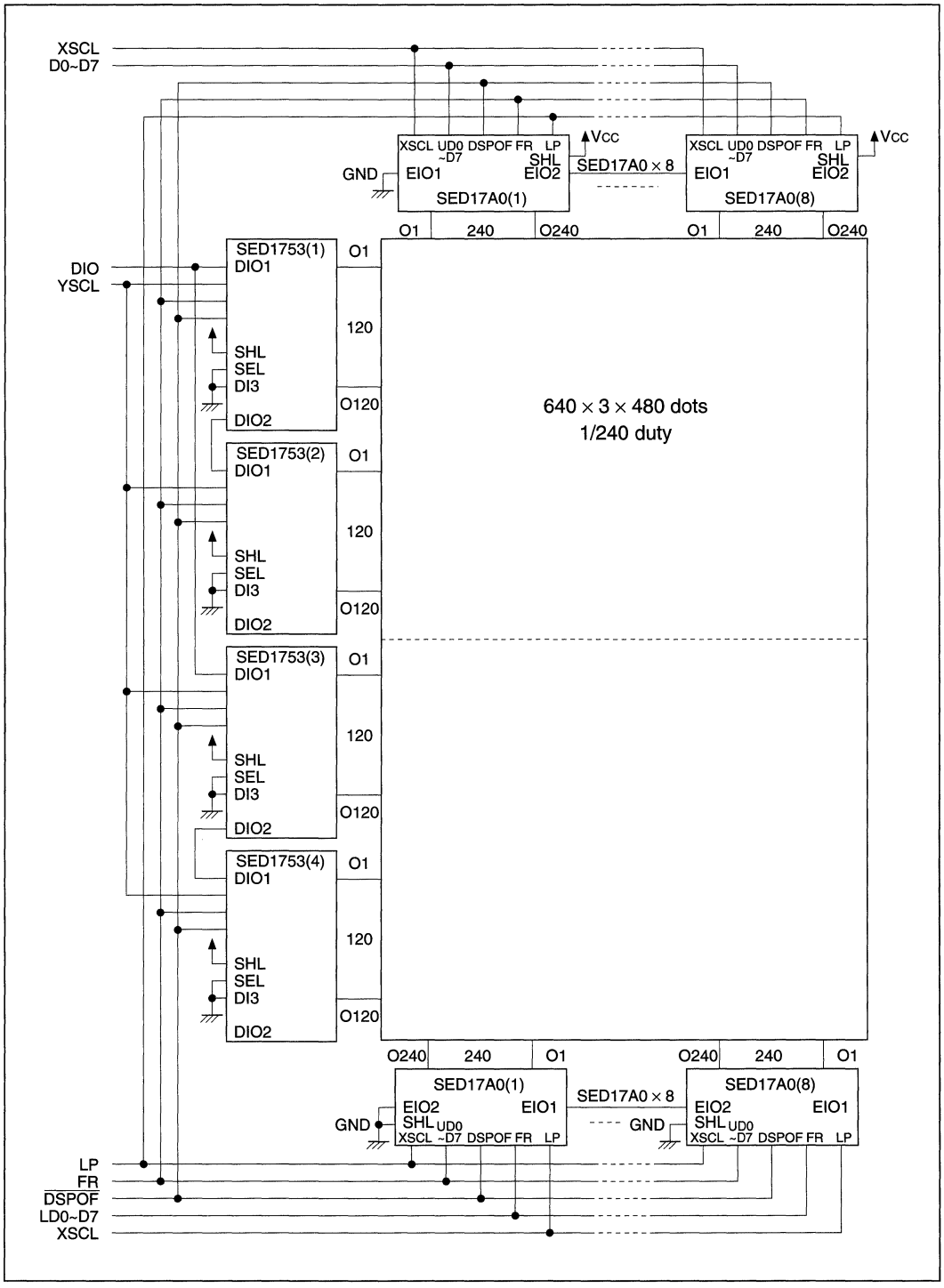
V_{CC} = +5.0V ± 10%, V_O = +14.0 to +42.0V

Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EI0)	—	50	ns
EIO output delay time	t_{DCL}		—	25	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (0 n)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	400	ns

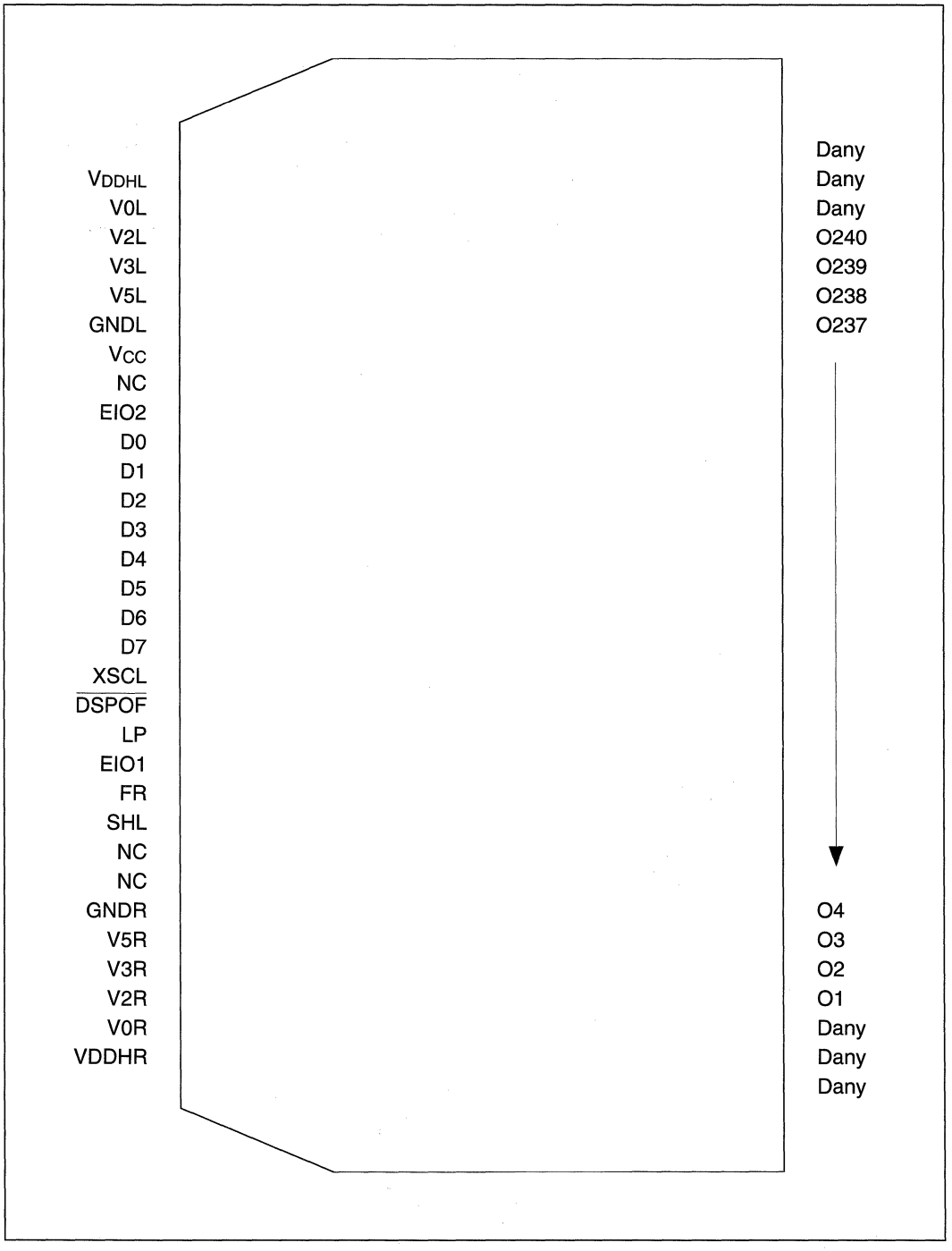
V_{CC} = +2.7 to 4.5V, V_O = +14.0 to +28.0V

Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EI0)	—	80	ns
EIO output delay time	t_{DCL}		—	50	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (0 n)	—	400	ns
FR → SEG output delay time	t_{FRSD}		—	800	ns

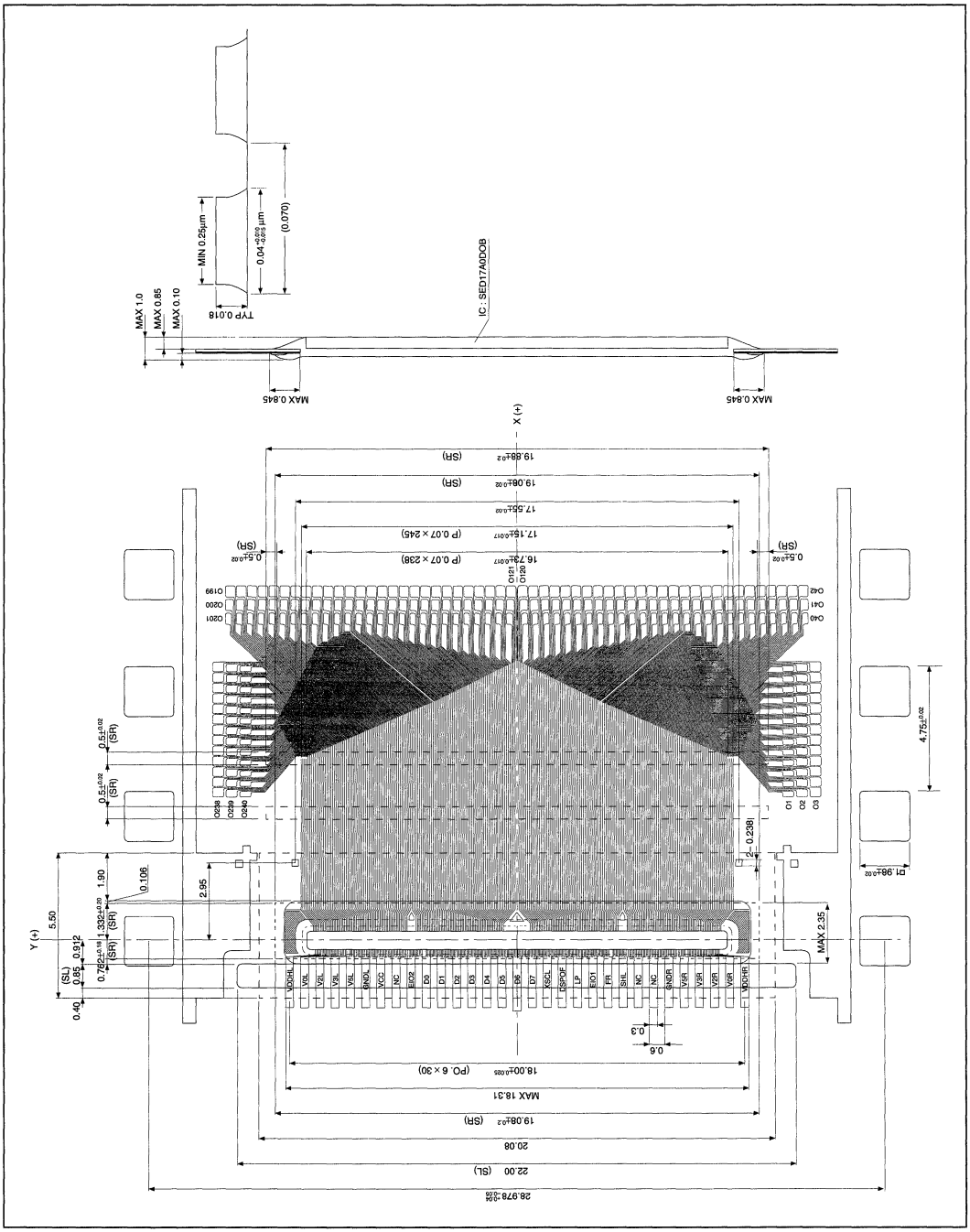
■ A CONNECTION EXAMPLE



■ TCP PIN ARRANGEMENT EXAMPLE (FOR REFERENCE)



■ PACKAGE DIMENSIONS



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1996 DATABOOK

GRAPHICS PRODUCTS

VI. HIGH-DUTY LCD COMMON DRIVERS

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■ HIGH-DUTY LCD COMMON DRIVERS

Part Number		SED 1190	SED 1191	SED 1610	SED 1630	SED 1631	SED 1632	SED 1633	SED 1634	SED 1635	SED 1651	SED 1733	SED 1741	SED 1743	SED 1753	SED 1755
Discontinued?		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No
Replacement		No	No	No	SED 167x	SED 167x	SED 167x	SED 167x	SED 167x	SED 167x	—	—	—	—	—	—
Resolution of commons		64	64	86	68	100	86	100	100	100	100	100	100	160	120	240
Duty Cycle		1/64 to 1/128	1/64 to 1/128	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/64 to 1/300	1/100 to 1/400	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500	1/100 to 1/500
LCD Voltage (V)		−14 to −25	−14 to −25	−12 to −28	−12 to −28	−12 to −28	−12 to −28	−12 to −28	−12 to −28	−8 to −28	−8 to −28	14 to 40	14 to 42	14 to 40	8 to 42	8 to 42
Supply Voltage	5V	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	3V				x			x	x	x	x		x	x	x	x
Data Bus (bits)	1	x	x	x	x	x	x	x	x	x	x	x	x	x		
	4															
Clock Frequency, max (MHz)		2.5	2.5	2.0	2.0	2.0	2.0	2.0 (5V), 1.0 (3V)	2.0 (5V), 1.0 (3V)	2.0 (5V), 1.0 (3V)	2.0 (5V), 1.0 (3V)	2.5	2.5 (5V), 1.25 (3V)	2.5 (5V), 1.25 (3V)		
Companion Chips		1180/ 81	1181	1600/ 01	1600/ 01	1600/ 01/20	1600	1600	1600	1570, 1600	1648	1722/ 24	1742/ 44	1742/ 44	1752/ 58	1756
Panel Type	Passive	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	MIM															
	TFT															

(continued)

■ HIGH-DUTY LCD COMMON DRIVERS (continued)

Part Number			SED 1190	SED 1191	SED 1610	SED 1630	SED 1631	SED 1632	SED 1633	SED 1634	SED 1635	SED 1651	SED 1733	SED 1741	SED 1743	SED 1753	SED 1755
Package	Die	Al	D0A	D0B		D0A	D0A	D0A	D1A	D1A	D1A	D0A	D0A				
		Au					D0B		D1B	D1B	D1B			D1B	D1B	D0B	
		COG															D0A
		Pad Pitch (μm)		190			149	240	149	149	149	153	170	108	108		
	TAB	2 Sided												T0A	T0A	T0A	
		Lead Pitch (μm)													180		
	QFP	Thin	F0A, F0B	F0B													
		Thick	F5A, F5B2	F5B	FAA	F0A							F0A				
		# of Pins	80	80	100	80							128				
Page number			705	713	721	727	733	741	747	759	771	783	795	805	819	835	849

Notes:
1. Some packages of certain parts labeled with # are still under development.

CMOS LCD 64-COMMON DRIVERS

■ DESCRIPTION

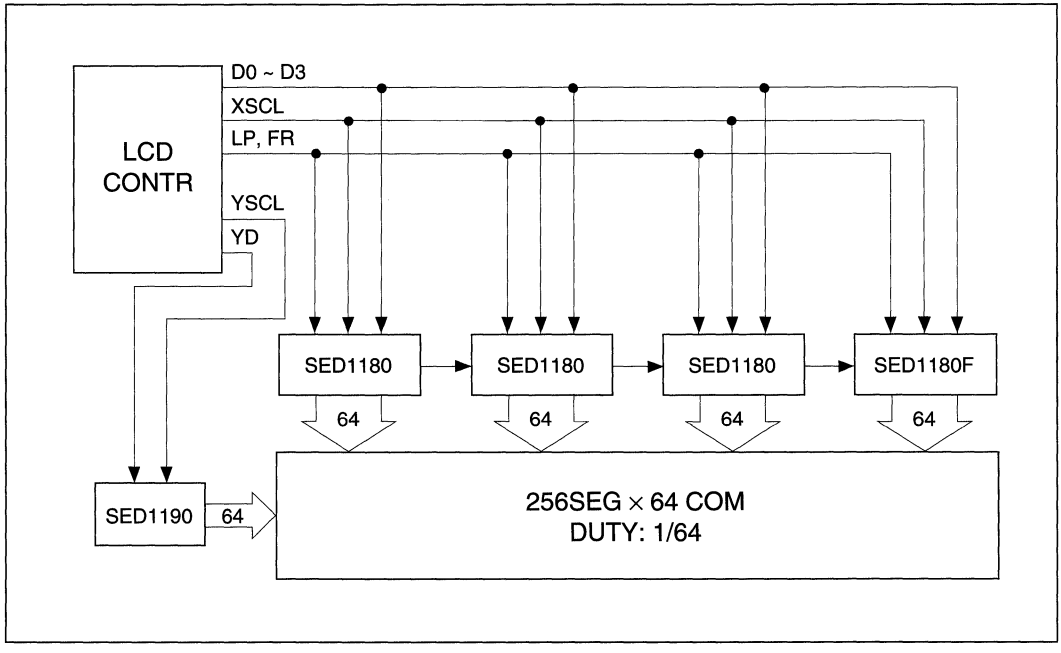
The SED1190 is a dot matrix LCD common (row) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI uses two serially connected, 32-bit shift registers to hold the display data, and level shifter converts the TTL level 64-bit parallel data from the shift registers to levels suitable for use by the LCD drive circuitry. The SED1190 generates common drive signals using the voltages supplied to LCD drive voltages pins.

The SED1190 is used in conjunction with the SED1180 (64-bit row driver) to drive a large capacity dot matrix LCD panel.

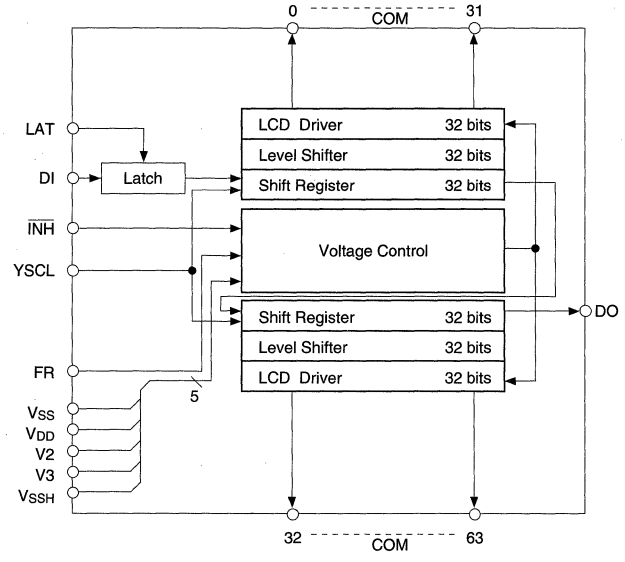
■ FEATURES

- Low-power CMOS technology
- 64-bit common (row) driver
- Display blanking
- Duty cycle: 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage: –14V to –25V
- Supply voltage: 5.0V ±10%
- Package: ..... QFP1-80 pin (F0A)
  QFP5-80 pin (F5A)
  DIE: Al pad chip (D0A)

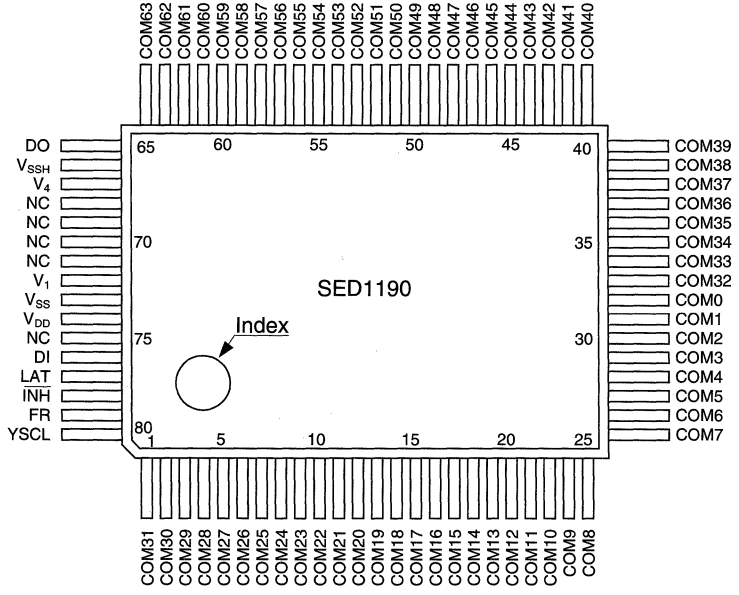
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	COM31	21	COM11	41	COM40	61	COM60
2	COM30	22	COM10	42	COM41	62	COM61
3	COM29	23	COM 9	43	COM42	63	COM62
4	COM28	24	COM 8	44	COM43	64	COM63
5	COM27	25	COM 7	45	COM44	65	DO
6	COM26	26	COM 6	46	COM45	66	V_{SSH}
7	COM25	27	COM 5	47	COM46	67	V4
8	COM24	28	COM 4	48	COM47	68	NC
9	COM23	29	COM 3	49	COM48	69	NC
10	COM22	30	COM 2	50	COM49	70	NC
11	COM21	31	COM 1	51	COM50	71	NC
12	COM20	32	COM 0	52	COM51	72	V1
13	COM19	33	COM32	53	COM52	73	V_{SS}
14	COM18	34	COM33	54	COM53	74	V_{DD}
15	COM17	35	COM34	55	COM54	75	NC
16	COM16	36	COM35	56	COM55	76	DI
17	COM15	37	COM36	57	COM56	77	LAT
18	COM14	38	COM37	58	COM57	78	$\overline{INH}$
19	COM13	39	COM38	59	COM58	79	FR
20	COM12	40	COM39	60	COM59	80	YSCL

NC = Not connected

■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>Function</th></tr>
<tr><td>COM0 to COM63</td><td>LCD common drive outputs</td></tr>
<tr><td>DI</td><td>Serial data input</td></tr>
<tr><td>LAT</td><td>Transparent latch control input:
<table>
<tr><th>LAT</th><th>DI</th><th>DI latch output</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>H</td></tr>
<tr><td>L</td><td>L</td></tr>
<tr><td>L</td><td>X</td><td>DI latch</td></tr>
</table></td></tr>
<tr><td>DO</td><td>Serial data output</td></tr>
<tr><td>YSCL</td><td>Serial data shift clock. Data is shifted through the controller on the falling edge of this clock</td></tr>
<tr><td>FR</td><td>LCD AC-drive signal input</td></tr>
<tr><td>$\overline{INH}$</td><td>Active-low blanking input</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Logic power supply inputs</td></tr>
<tr><td>V1, V4, V_{SSH}</td><td>LCD drive power inputs
$V_{DD} \geq V1 \geq V4 \geq V_{SSH}$</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_{SSH}	–28.0 to +0.3	V
	V1, V4		
Input voltage	V_I	V_{SS} –0.3 to +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C
Soldering temperature and time	T_{sol}	260, 10	°C, s

Notes:

1. All voltages referenced to a V_{DD} of 0 V.
2. V1 and V4 must satisfy the relationship $V_{DD} \geq V1, V4 \geq V_{SSH}$
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

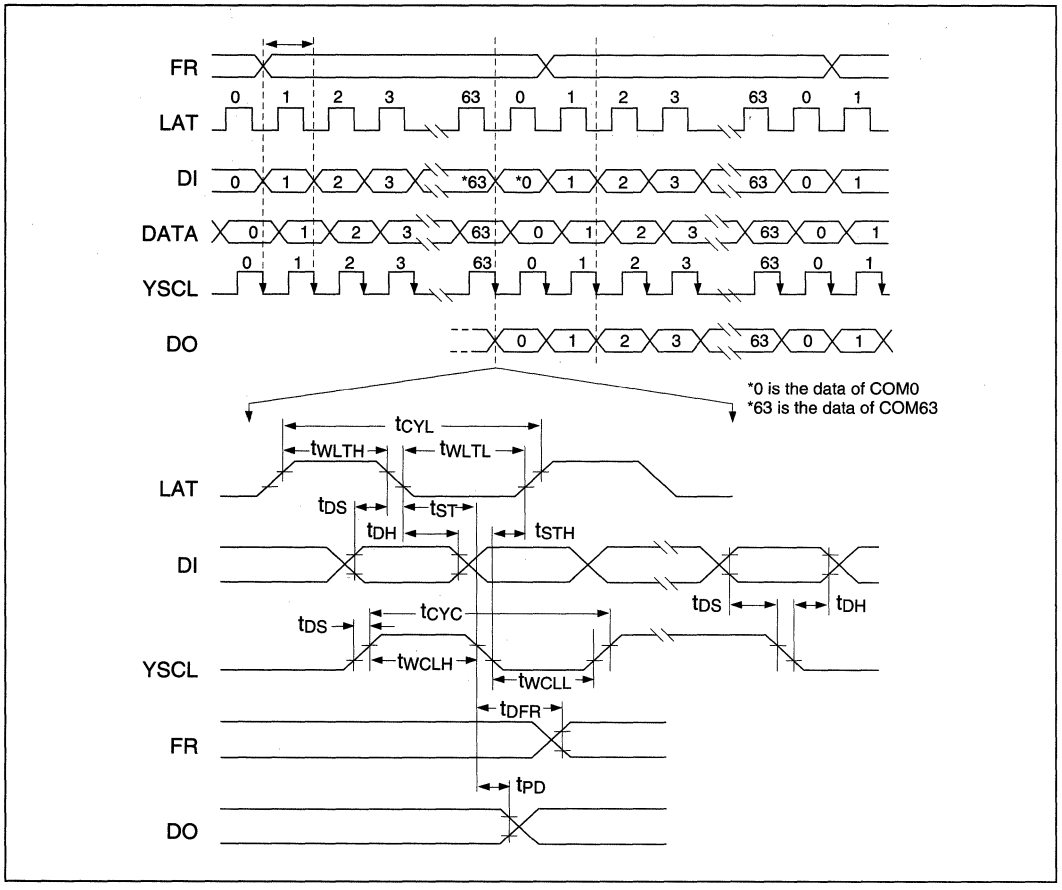
● DC Characteristics

(V_{DD} = 0V, V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions		Rating Min	Rating Typ	Rating Max	Unit
Supply voltage (1)	V_{SS}			–5.5	–5.0	–4.5	V
Supply voltage (2)	V1			V_{SSH}	—	V_{DD}	V
	V4			V_{SSH}	—	V_{DD}	V
	V_{SSH}	Recommended V_{SSH}		–25.0	—	–14.0	V
		Operable V_{SSH} (see note)		–25.0	—	–5.0	V
High level input voltage	V_{IH}			0.2V_{SS}	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}			V_{SS}–0.3	—	0.8V_{SS}	V
High level output voltage	V_{OH}	I_{OH} = –0.6 mA		–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≥ V_I ≥ V_{SS}		—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≥ V_O ≥ V_{SS}		—	0.05	5.0	µA
Shift clock	YSCL			—	—	2.5	MHz
Frame signal	FR			—	1/60	—	s
Input capacitance	C_I	T_a = 25°C		—	5.0	8.0	pF
Common output on resistance	R_{COM}	V_{OH} = V_{DD} –0.5 V V_{OL} = V_{SSH} +0.5 V COM bit	V_{SSH} = –20.0 V	—	0.8	1.0	kΩ
			V_{SSH} = –14.0 V	—	0.9	1.3	
			V_{SSH} = –9.0 V	—	1.3	2.0	
			V_{SSH} = –5.0 V	—	3.0	30.0	
Quiescent current	I_Q	SED 1190	V_{SSH} = –25 V, V_{SSH} = –5.5 V, V_I = V_{DD}	—	0.05	30	µA
Operating current for the logic	I_{SS}	FR cycle = 16.7 ms	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, YSCL cycle = 130 µs (duty 50%), All "H" output terminals are opened at every data input all 1/128 duty.	—	3.0	8.0	µA
Operating current for LCD	I_{SSH}	FR cycle = 16.7 ms	V_{SS} = –4.5 V, V_1 = –2.0 V, V_4 = –18.0 V, YSCL cycle = 130 µs (duty 50%), All "H" output terminals are opened at every data input of 1/128 duty.	—	3.0	8.0	µA
Pull up MOS current	$-I_p$	V_{SS} = –5.0 V, V_{IL} = –5.0 V Applicable to LAT input terminals		10.0	25.0	50.0	µA

Note: Error free operation is guaranteed in this range but the output resistance of the LCD drivers is higher than in the recommended operating range. It is suggested that the driver is tested with the target LCD panel to determine if performance is acceptable.

- **AC Electrical Characteristics**
  - **I/O Signal Timing**

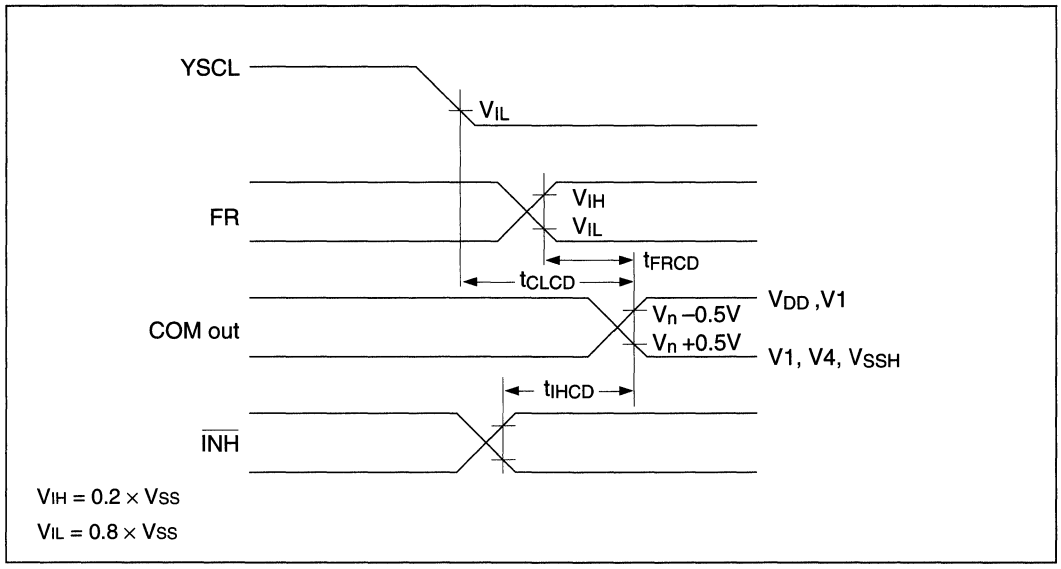


V_{DD} = 0V, V_{SS} = –5.0V ± 10%, T_a = –20 to 75°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Latch pulse cycle time	t_{CYL}	—	400	—	—	ns
Latch pulse "H" width	t_{WLTH}	—	180	—	—	ns
Latch pulse "L" width	t_{WLL}	—	180	—	—	ns
Shift clock cycle time	t_{CYC}	—	400	—	—	ns
Shift clock "H" time	t_{WCLH}	—	110	—	—	ns
Shift clock "L" time	t_{WCLL}	—	110 (240)	—	—	ns
Data setup time	t_{DS}	—	100 (70)	—	—	ns
Data hold time	t_{DH}	—	30	—	—	ns
Data shift timing	t_{ST}	—	0	—	—	ns
Data shift hold time	t_{STH}	—	125	—	—	ns
Permissible frame signal delay	t_{DFR}	—	–500	0	500	ns
Input signal rise time	t_r	—	—	—	*	ns
Input signal fall time	t_f	—	—	—	*	ns
Data output delay time	t_{PD}	C_L = 15pF	30	—	170	ns

* t_r, t_f = (t_{CYL} – t_{WLH} – t_{WLTL}) / 2 where $t_f \geq$ 50ns.

● **Common Drive**

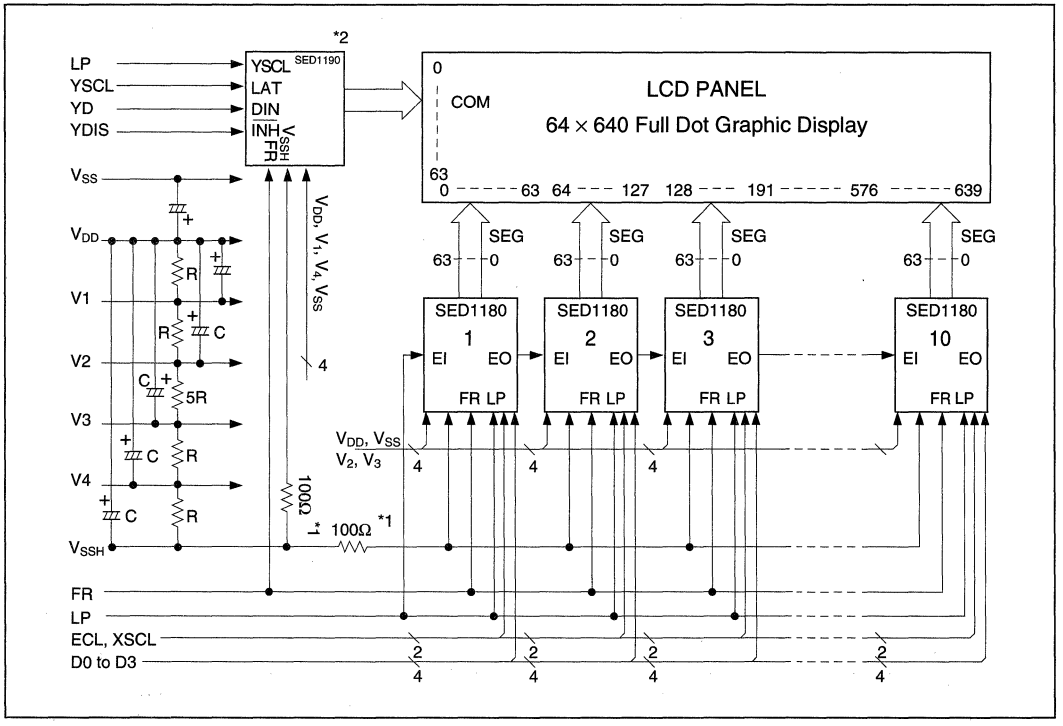


V_{DD} = 0V, V_{SS} = –5.0V ± 10%, T_a = –20 to 75°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL – COM output delay time	t_{CLCD}	V_{SSH} = –14.0 to –25.0V C_L = 100pF	—	—	3.0	µs
RF – COM output delay time	t_{FRCD}		—	—	3.0	µs
INH – COM output delay time	t_{IHCD}		—	—	3.0	µs

■ EXAMPLE OF APPLICATION

(64 × 640 pixels, 1/64 duty ratio)



Notes:

1. Current limiting resistors
2. Bypass V_{SS} and V_{SSH} with capacitors of at least 0.01 μF

CMOS LCD 64-COMMON DRIVER

■ DESCRIPTION

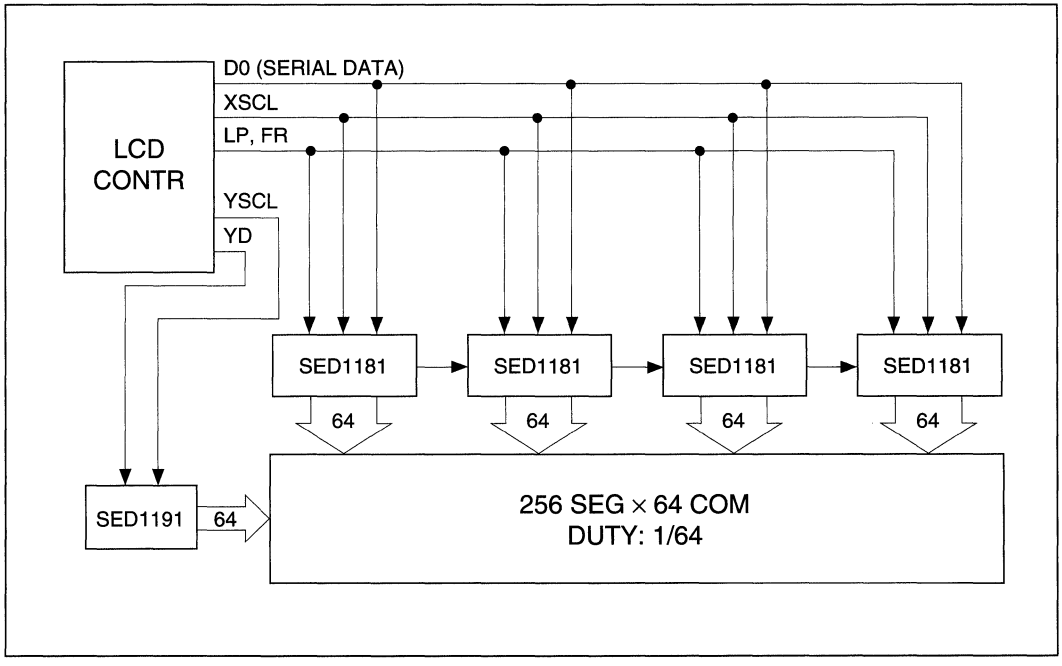
The SED1191 is a dot matrix LCD common (row) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI uses two serially connected, 32-bit shift registers to hold the display data, and level shifter converts the TTL level 64-bit parallel data from the shift registers to levels suitable for use by the LCD drive circuitry. The SED1191 generates common drive signals using the voltages supplied to LCD drive voltages pins.

The SED1191 is used in conjunction with the SED1181 (64-bit row driver) to drive a large-capacity dot-matrix LCD panel.

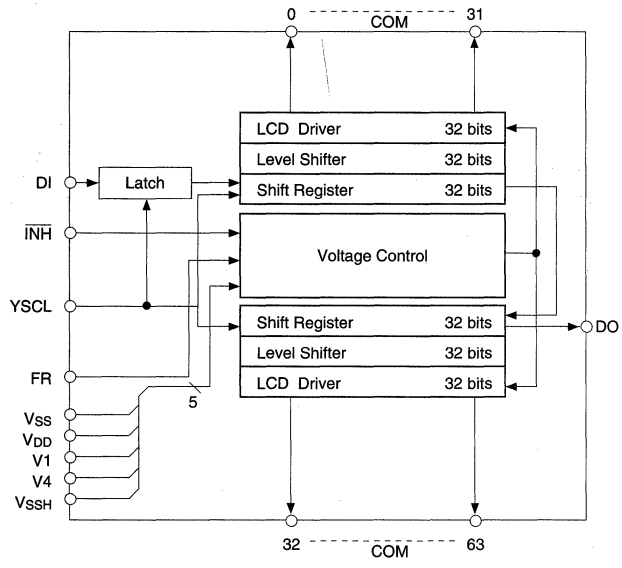
■ FEATURES

- Low-power CMOS technology
- 64-bit common (row) driver
- Display blanking
- Duty cycle: 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage: –14V to –25V
- Supply voltage: 5.0V ± 10%
- Package: ..... QFP1-80 pin (F_{0B})
  QFP5-80 pin (F_{5B})
  DIE: Al pad (D_{0A})

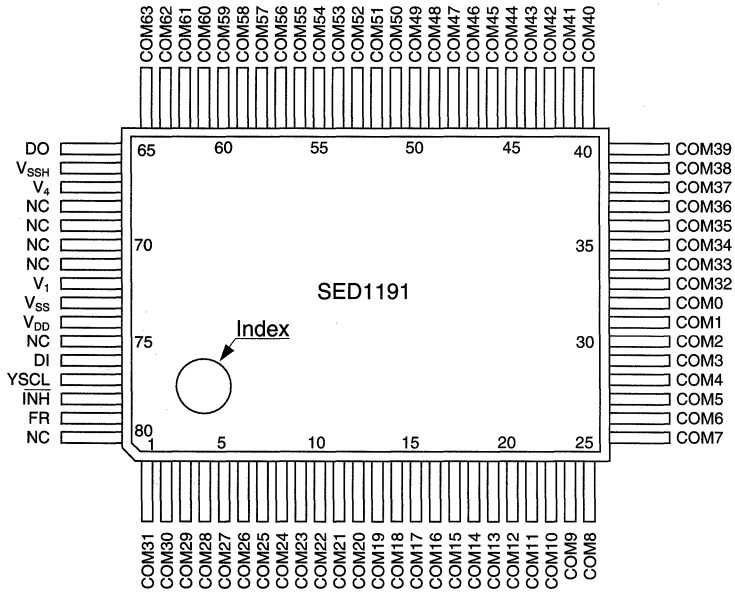
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



Number	Name	Number	Name	Number	Name	Number	Name
1	COM31	21	COM11	41	COM40	61	COM60
2	COM30	22	COM10	42	COM41	62	COM61
3	COM29	23	COM 9	43	COM42	63	COM62
4	COM28	24	COM 8	44	COM43	64	COM63
5	COM27	25	COM 7	45	COM44	65	DO
6	COM26	26	COM 6	46	COM45	66	V_{SSH}
7	COM25	27	COM 5	47	COM46	67	V4
8	COM24	28	COM 4	48	COM47	68	NC
9	COM23	29	COM 3	49	COM48	69	NC
10	COM22	30	COM 2	50	COM49	70	NC
11	COM21	31	COM 1	51	COM50	71	NC
12	COM20	32	COM 0	52	COM51	72	V1
13	COM19	33	COM32	53	COM52	73	V_{SS}
14	COM18	34	COM33	54	COM53	74	V_{DD}
15	COM17	35	COM34	55	COM54	75	NC
16	COM16	36	COM35	56	COM55	76	DI
17	COM15	37	COM36	57	COM56	77	YSCL
18	COM14	38	COM37	58	COM57	78	$\overline{INH}$
19	COM13	39	COM38	59	COM58	79	FR
20	COM12	40	COM39	60	COM59	80	NC

■ PIN DESCRIPTION

Pin Name	Function
COM0 to COM63	LCD common drive outputs
DI	Serial data input
DO	Serial data output
YSCL	Serial data shift clock. Data is shifted through the controller on the falling edge of this clock
FR	LCD AC-drive signal input
$\overline{INH}$	Active-low blanking input
V_{DD}, V_{SS}	Logic power supply inputs
V1, V4, V_{SSH}	LCD drive power supply inputs $V_{DD} \geq V1 \geq V4 \geq V_{SSH}$

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_{SSH}	–28.0 to +0.3	V
	V1, V4		
Input voltage	V_I	V_{SS} –0.3 to +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C
Soldering temperature and time	T_{sol}	260, 10	°C, s

Notes:

1. All voltages referenced to a V_{DD} of 0 V.
2. V1 and V4 must satisfy the relationship $V_{DD} \geq V1, V4 \geq V_{SSH}$
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

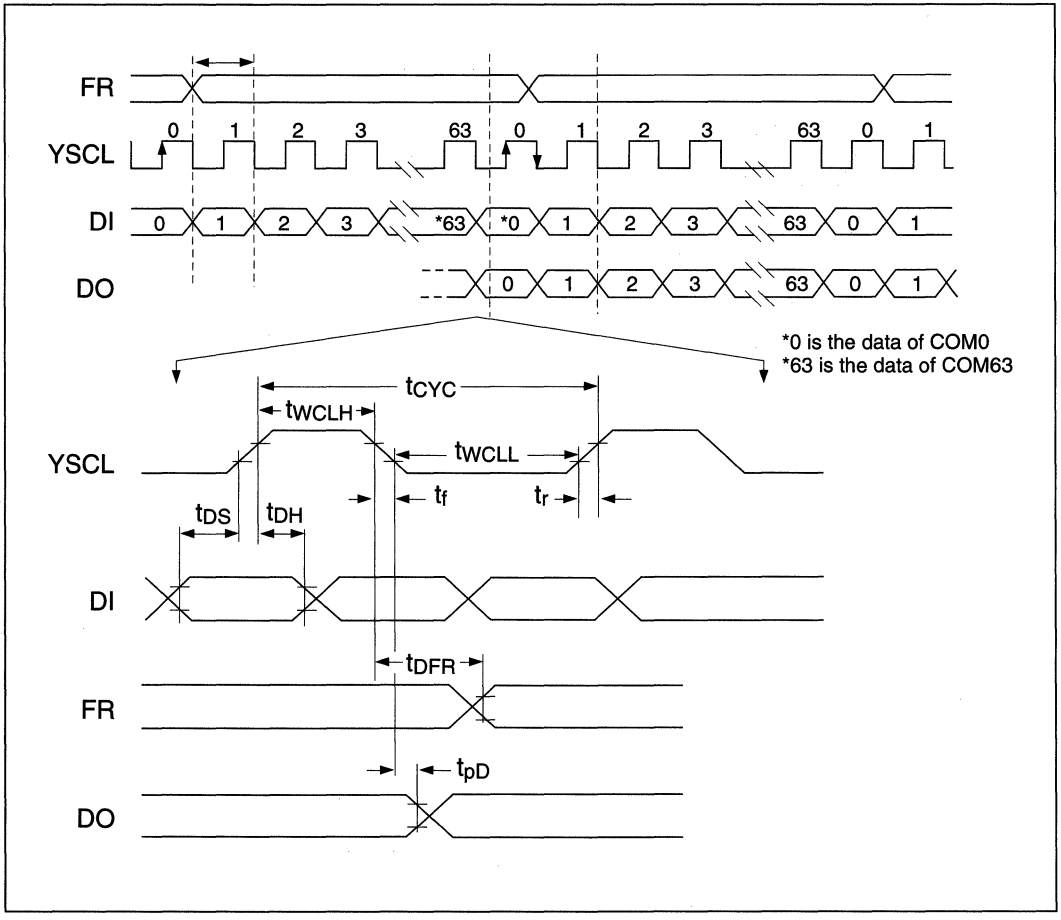
● DC Characteristics

(V_{DD} = 0V, V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameters	Symbol	Condition		Rating			Unit
				Min	Typ	Max	
Supply voltage (1)	V_{SS}			–5.5	–5.0	–4.5	V
Supply voltage (2)	V1			V_{SSH}	—	V_{DD}	V
	V4			V_{SSH}	—	V_{DD}	V
	V_{SSH}			–25.0	—	–14.0	V
High level input voltage	V_{IH}			0.2xV_{SS}	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}			V_{SS}–0.3	—	0.8xV_{SS}	V
High level output voltage	V_{OH}	I_{OH} = –0.6 mA		–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{SS}		—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{SS}		—	0.05	5.0	µA
Shift clock	YSCL			—	—	2.5	MHz
Frame signal	FR			—	1/60	—	Sec
Input capacitance	C_I	T_a = 25°C		—	5.0	8.0	pF
COM output on resistance	R_{COM}	V_{SSH} = –14.0 V, V_{OH} = V_{DD}–0.5 V, V_{OL} = V_{SSH}+0.5 V COM./ bit		—	2.0	4.0	kΩ
Quiescent current	I_Q	V_{SSH} = –18.0 V, V_{SS} = –5.5 V, V_I = V_{DD}		—	0.05	30.0	µA
Operating current for the logic	I_{SSOP}	FR cycle = 130 µs	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, YSCL cycle = 130 µs (duty 50%), All "H" output terminals are opened at every data input all 1/128 duty.	—	3.0	8.0	µA
Operating current for LCD	I_{SSHOP}	FR cycle = 130 µs	V_{SS} = –4.5 V, V_1 = –1.8 V, V_4 = –16.2 V, V_{SSH} = –18.0 V, YSCL cycle = 130 µs (duty 50%), All "H" output terminals are opened at every data input of 1/128 duty.	—	70	100	µA

Note: Error free operation is guaranteed in this range but the output resistance of the LCD drivers is higher than in the recommended operating range. It is suggested that the driver is tested with the target LCD panel to determine if performance is acceptable.

- **AC Characteristics**
  - **I/O Signal**

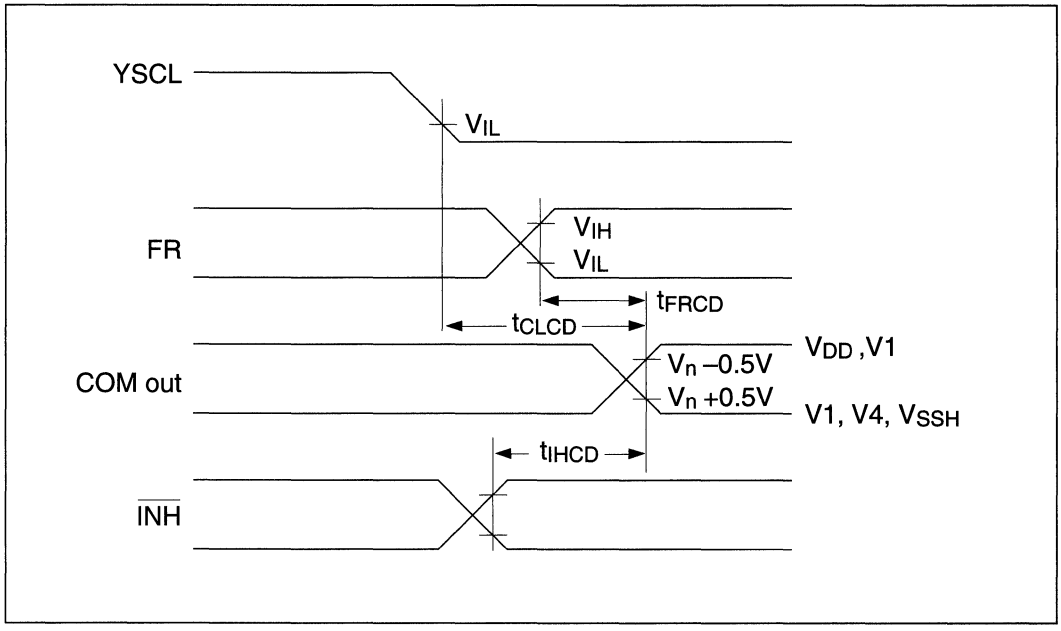


(V_{DD} = 0V, V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Shift lock cycle time	t_{CYC}		500	—	—	ns
Shift lock "H" width	t_{WCLH}		110	—	—	ns
Shift lock "L" width	t_{WCLL}		240	—	—	ns
Data setup time	t_{DS}		70	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
Permissible frame signal delay	t_{DFR}		–500	0	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns
Data output delay time	t_{pD}	C_L = 15 pF	30	—	170	ns

Note: t_r, t_f = (t_{CYL} – t_{WLH} – t_{WLTL}) / 2 where $t_r \geq$ 50 ns.

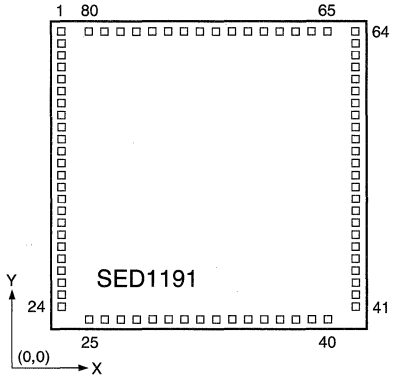
○ **Common Drive**



$V_{IH} = 0.2 \times V_{SS}$; $V_{IL} = 0.8 \times V_{SS}$ (V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
YSCL-COM output delay time	t_{CLCD}	V_{SSH}=–14.0 to –18.0V	—	—	3.0	µs
RF-COM output delay time	t_{FRCD}	C_L= 100 pF	—	—	3.0	µs
INH-COM output delay time	t_{IHCD}		—	—	3.0	µs

■ PAD LAYOUT



Die size ..... 4.80 × 4.98 mm
Pad pitch ..... 190 µm (min.)
Die thickness ..... 400 µm

■ PAD COORDINATES

µm

No.	Name	X	Y
1	COM31	152	4826
2	COM30	152	4636
3	COM29	152	4446
4	COM28	152	4255
5	COM27	152	4065
6	COM26	152	3874
7	COM25	152	3684
8	COM24	152	3494
9	COM23	152	3303
10	COM22	152	3113
11	COM21	152	2922
12	COM20	152	2732
13	COM19	152	2542
14	COM18	152	2351
15	COM17	152	2181
16	COM16	152	1970
17	COM15	152	1780
18	COM14	152	1590
19	COM13	152	1399
20	COM12	152	1209
21	COM11	152	1018
22	COM10	152	828
23	COM9	152	570
24	COM8	152	379
25	COM7	516	155
26	COM6	762	155
27	COM5	1009	155

No.	Name	X	Y
28	COM4	1255	155
29	COM3	1502	155
30	COM2	1748	155
31	COM1	1995	155
32	COM0	2241	155
33	COM32	2488	155
34	COM33	2734	155
35	COM34	2981	155
36	COM35	3227	155
37	COM36	3474	155
38	COM37	3720	155
39	COM38	3967	155
40	COM39	4213	155
41	COM40	4645	379
42	COM41	4645	570
43	COM42	4645	828
44	COM43	4645	1018
45	COM44	4645	1209
46	COM45	4645	1399
47	COM46	4645	1590
48	COM47	4645	1780
49	COM48	4645	1970
50	COM49	4645	2161
51	COM50	4645	2351
52	COM51	4645	2542
53	COM52	4645	2732
54	COM53	4645	2922

No.	Name	X	Y
55	COM54	4645	3113
56	COM55	4645	3303
57	COM56	4645	3494
58	COM57	4645	3684
59	COM58	4645	3874
60	COM59	4645	4065
61	COM60	4645	4255
62	COM61	4645	4446
63	COM62	4645	4636
64	COM63	4645	4826
65	DO	4254	4826
66	VSSH	4008	4826
67	V4	3761	4826
68	NC	3515	4826
69	NC	3268	4826
70	NC	3022	4826
71	NC	2775	4826
72	V1	2529	4826
73	VSS	2282	4826
74	VDD	2036	4826
75	NC	1789	4826
76	DI	1543	4826
77	LAT	1296	4826
78	$\overline{\text{INH}}$	1050	4826
79	FR	803	4826
80	YSCL	557	4826

DISCONTINUED

SED1610

CMOS 86 ROWS LCD DRIVER

■ DESCRIPTION

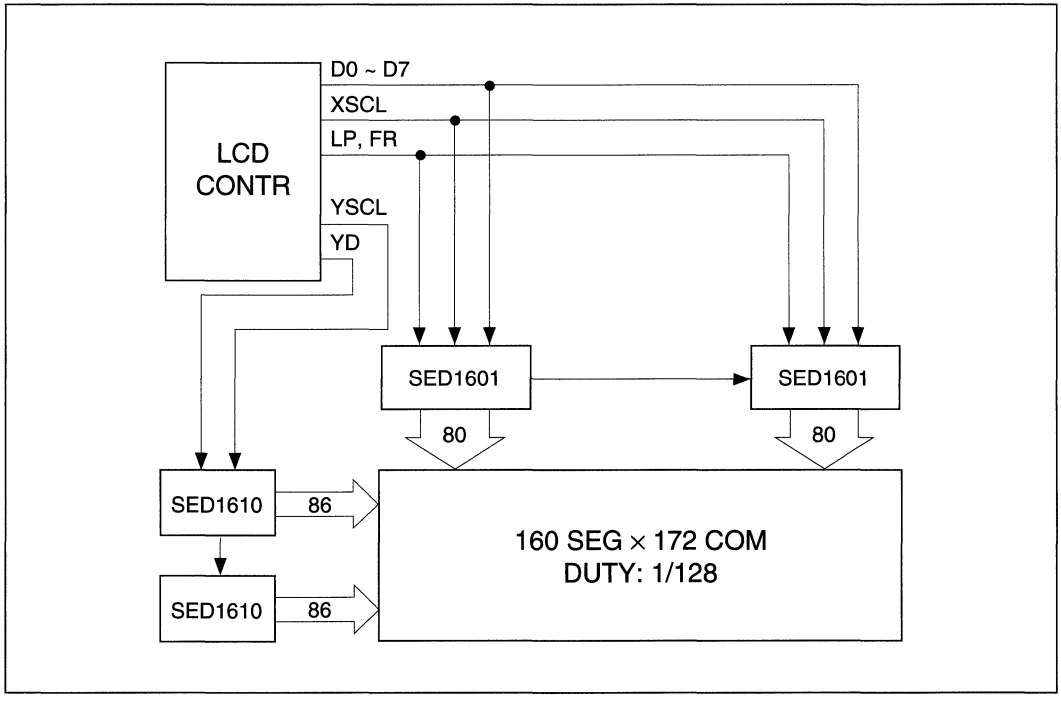
The SED1610 is an 86 output dot matrix LCD common (row) driver for driving a high-capacity LCD panel at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of LCD driving voltages. Due to the architecture of the SED1610, the LCD driving voltage V0 is isolated from V_{DD}. This provides the ability to adjust the offset bias independently of V_{DD}. These unique features allow the SED1610 to interface with a variety of LCD panels.

The SED1610 is used in conjunction with the SED1600 (80 segment driver) or the SED1601 (80 segment driver) to drive a large-capacity dot matrix LCD panel.

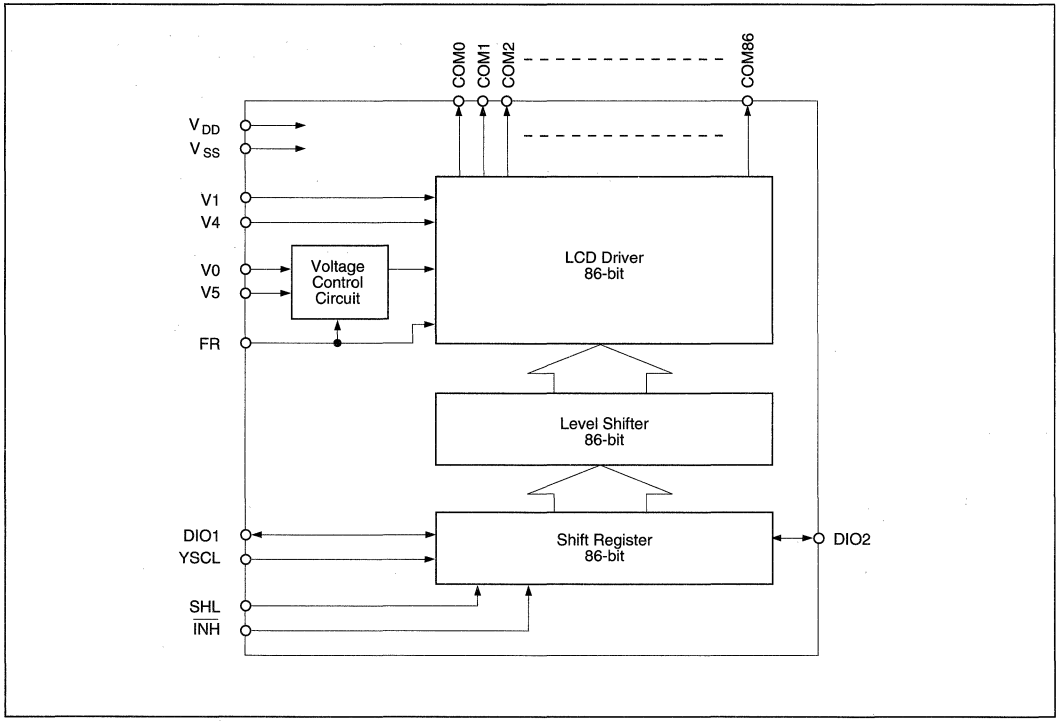
■ FEATURES

- Low-power CMOS technology
- 86-bit common (row) driver
- Duty cycle ..... 1/64 to 1/300
- Display blanking available
- Shift clock frequency ..... 2MHz max.
- Ability to adjust offset bias of the LCD source from V_{DD}
- Selectable output shift direction
- Wide range of LCD voltage .... –12 to –28V
- Supply voltage ..... 5.0V ± 10%
- Package ..... QFP5-100 pins (F_{AA})

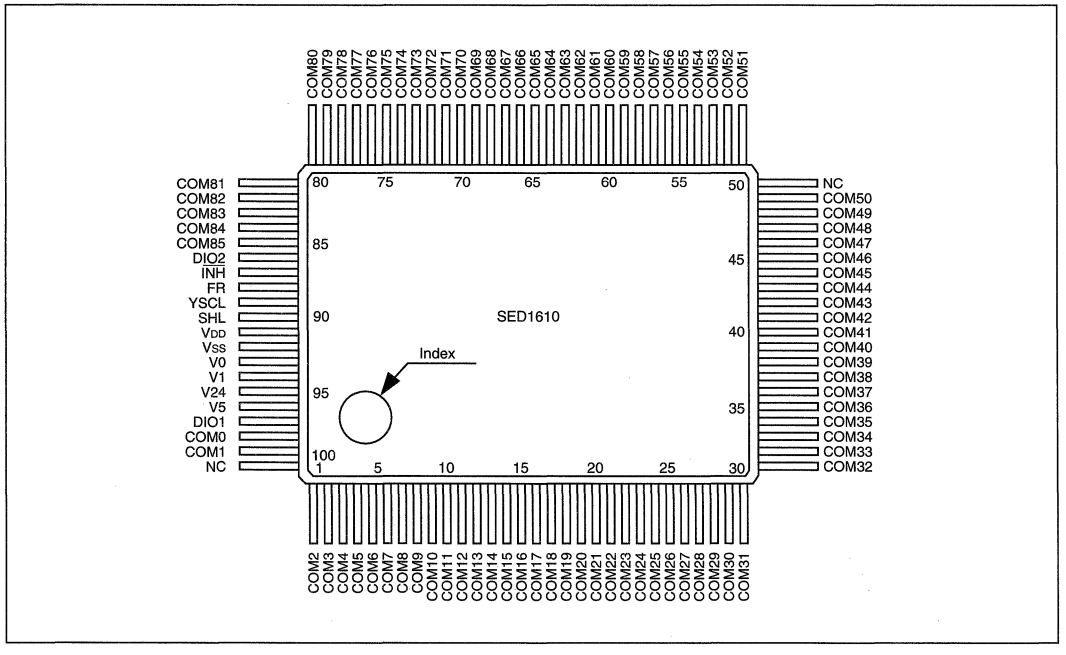
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTION

Pin name	Functions
COM0 to COM 85	LCD driving common (row) outputs. Each output changes at the falling edge of YSCL.
$\overline{INH}$	Controls all common outputs to nonselect level (V4 when FR = L, V1 when FR = H) (low active)
YSCL	Shift clock of serial data (falling edge trigger).
DIO1, DIO2	Serial transfer data I/O, which is controlled by SHL input. Output changes at falling edge of YSCL.
SHL	Shift direction selection and DI0 pin control.

SHL	COM output shift direction	DIO 1	DIO 2
L	85 ◄——— 0	Input	Output
R	85 ———► 0	Output	Input

FR	AC signal of LCD driving outputs.
V_{DD}, V_{SS}	Logic circuit power. V_{DD}: 0 V (GND) V_{SS}: −5.0 V
V0, V1, V4, V5	LCD driving power. V5: −12 to −28 V $V_{DD} \geq V0 > V1 > V4 > V5$

INH	Contents of Shift Register	FR	COM0 ~ 85	
H	H	H	V5	(Select level)
		L	V0	
	L	H	V1	(Non select level)
		L	V4	
L	Fixed to "L"	H	V1	(Non select level)
		L	V4	

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	−7.0 to +0.3	V
Supply voltage (2)	V5	−30.0 to +0.3	V
Supply voltage (2)	V0, V1, V4	V5 −0.3 to +0.3	V
Input voltage (1)	V_I	V_{SS} −0.3 to +0.3	V
Output voltage (1)	V_O	V_{SS} −0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OSEG}	20	mA
Operating temperature	T_{opr}	−20 to +75	°C
Storage temperature	T_{stg}	−65 to +150	°C
Soldering temperature, time	T_{sol}	260°C, 10 s (at lead)	—
Allowable power dissipation	P_D	300	mW

● DC Electrical Characteristics

(Unless otherwise specified, V_{DD} = V0 = 0 V, V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Operating voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–4.5	V
Recommended operating voltage Minimum operating voltage	V5		V5	–28.0	—	–12.0 –8.0	V
Operating voltage (2)	V0		V0	–2.5	—	0	V
"H" input voltage	V_{IH}		DI01, DI02, YSCL, FR, SHL, INH	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}			—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH} = –0.6 mA	DI01, DI02	–0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_I \le 0$ V	YSCL, SHL, INH, FR	—	—	2.0	µA
	$I_{LI/O}$	$V_{SS} \le V_I \le 0$ V	DI01, DI02	—	—	5.0	µA
Stand-by current	I_{DDS}	V5 = –12.0 to –28.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{SEG}	|ΔV_{ON}| =0.5 V, V5 = –20.0V	COM0 to COM85	—	1.1	1.8	kΩ
		V5 = –14.0V		—	1.2	2.0	
		V5 = –8.0V		—	2.0	4.0	
Current dissipation (1)	I_{SSO1}	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 7.7kHz., Frame period = 60 Hz; Input data: "H" every 1/128 duty No-load	V_{SS}	—	7	15.0	µA
Current dissipation (2)	I_{SSO2}	V_{SS} = –5.0 V, V1 = –2.0 V V4 = –18.0 V, V5 = –20.0 V All other conditions are same as I_{SSO1}	V5	—	7	15.0	µA
Input capacitance	C_I	T_a = 25°C	YSCL, SHL, INH, FR	—	—	8.0	pF
	$C_{I/O}$		DI01, DI02	—	—	15.0	pF

● AC Characteristics

○ Input Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL period	t_{CCL}		500	—	—	ns
YSCL "H" pulse width	t_{WCLH}		70	—	—	ns
YSCL "L" pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns

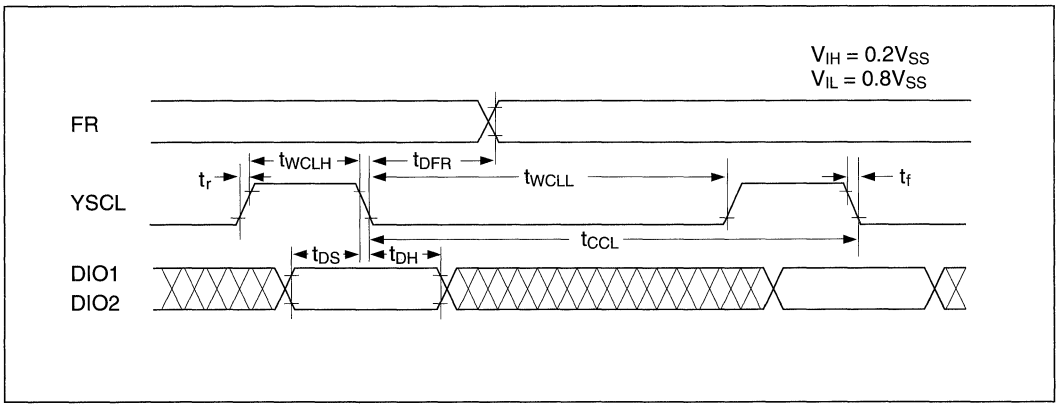
○ **Output Timing**

(V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

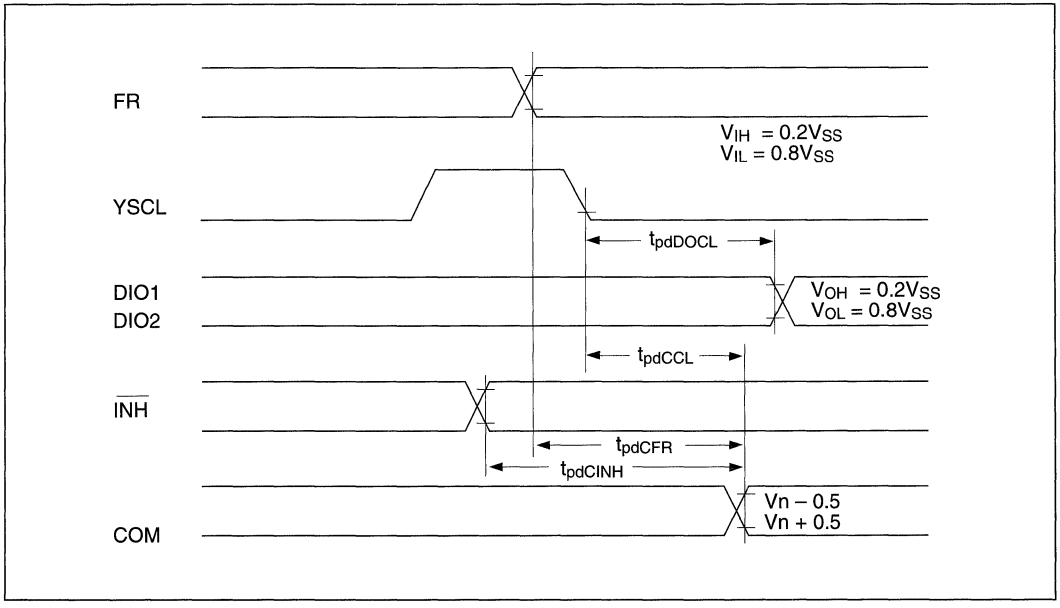
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(YSCL-fall to DIO) Delay time	t_{pdDOCL}	C_L = 15 pF	30	—	300	ns
(YSCL-fall to COM output) Delay time	t_{pdCCL}	V5 = –12.0 to –28.0 V C_L = 100 pF	—	—	3.0	µs
($\overline{INH}$ to COM output) Delay time	t_{pdCINH}					
(FR to COM output) Delay time	t_{pdCFR}		—	—	3.0	µs

● **Timing Chart**

○ **Input Timing**

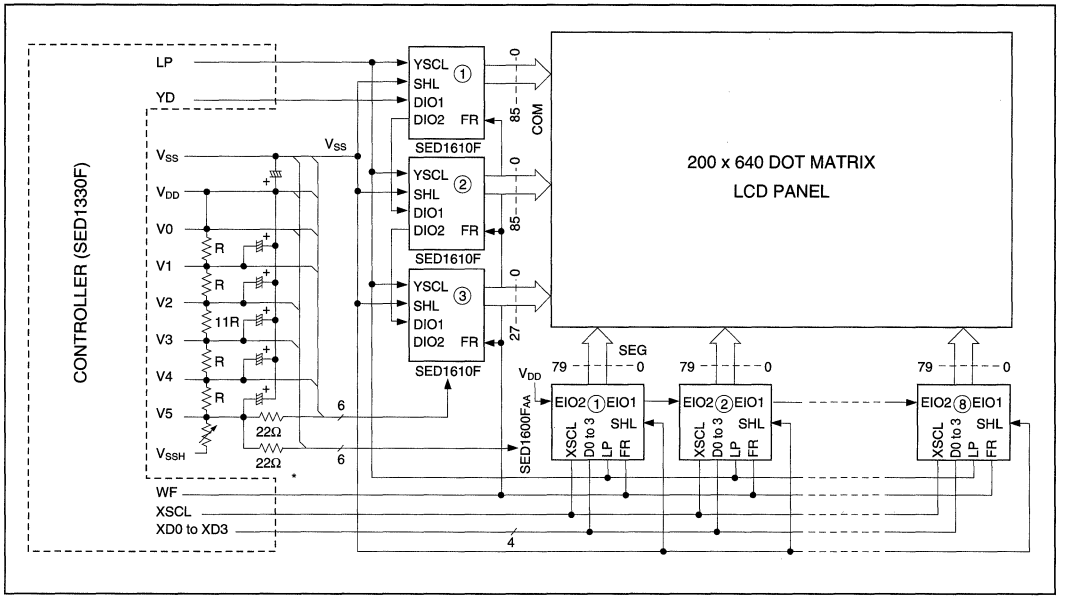


○ **Output Timing**



■ EXAMPLE OF APPLICATION (SED1610FAA)

(for 200 × 640 DOT MATRIX LCD)



Note: * Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01 μF) near pins Vss and V5 of each LSI for noise protection.

DISCONTINUED

SED1630

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

- **CMOS 68-bit Common Driver**
- **High Voltage Resistant Output**
- **CMOS High Voltage Resistant Process**

■ DESCRIPTION

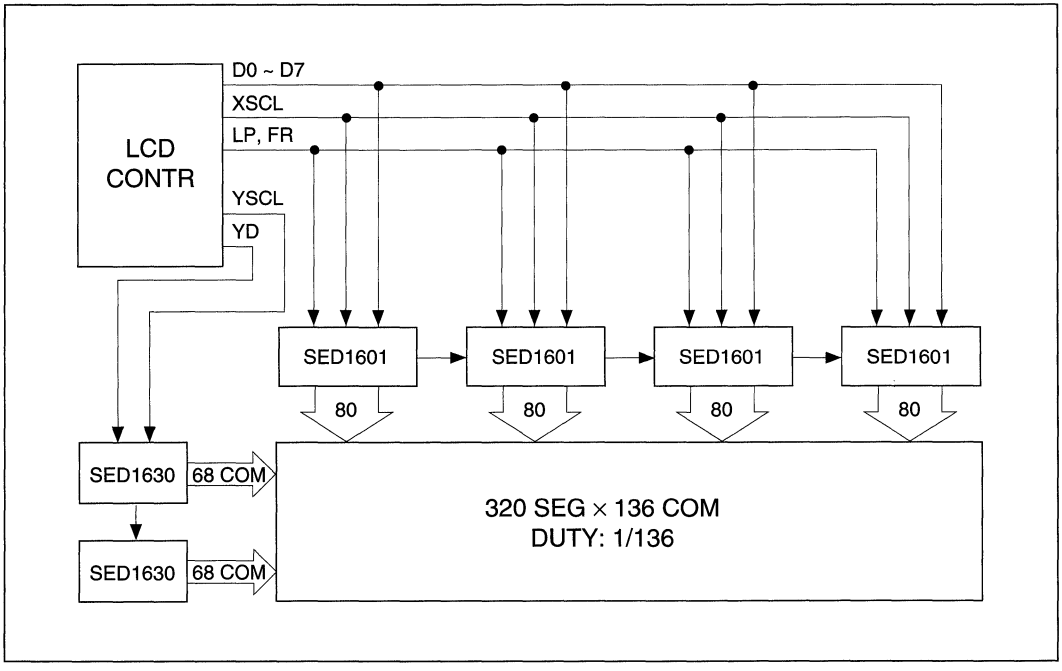
The SED1630 is a 68 output dot matrix LCD common (row) driver for driving a high-capacity LCD panel at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of LCD driving voltages. Due to the architecture of the SED1630, the LCD driving voltage V0 is isolated from V_{DD}. This provides the ability to adjust the offset bias independently of V_{DD}. These unique features allow the SED1610 to interface with a variety of LCD panels.

The SED1630 is used in conjunction with the SED1600 (80 segment driver) or the SED1601 (80 segment driver) or the SED1620 (128-bit segment driver) to drive a large-capacity dot matrix LCD panel.

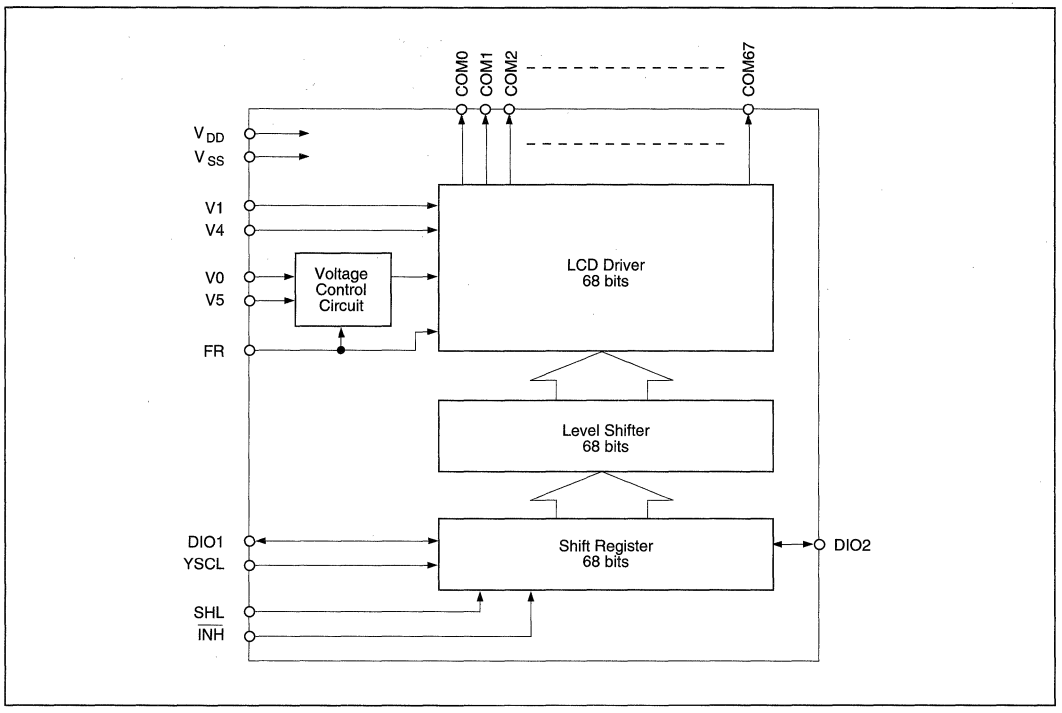
■ FEATURES

- Low-power CMOS technology
- 68-bit common (row) driver
- Duty cycle ..... 1/64 to 1/300
- Display blanking available
- Shift clock frequency ..... 2MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Selectable output shift direction
- Wide range of LCD voltage .... 12V to 28V
- Supply voltage ..... 5.0V ± 10%
- Package ..... QFP5-80 pins (FOA)

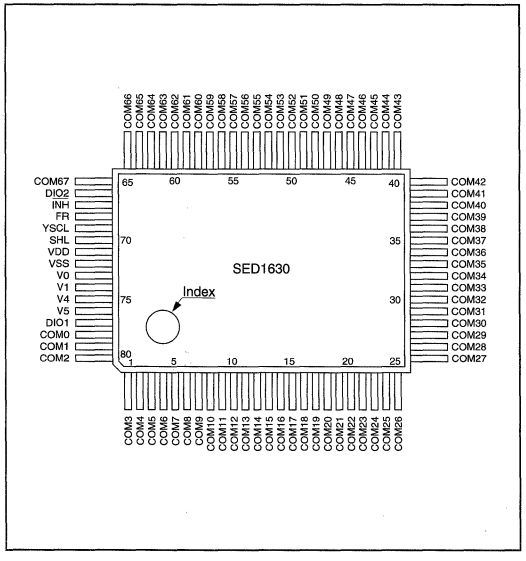
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin name	Functions
COM0 to COM 67	LCD drive common outputs.
$\overline{INH}$	Active low Blanking controlled input.
YSCL	Data is shifted into the driver on the falling edge of this signal.
DIO1, DIO2	Serial data input/output pins. Configured by SHL.
SHL	Shift direction and input/output select input

SHL	COM output shift direction	DIO 1	DIO 2
L	0 → 67	Input	Output
R	67 → 0	Output	Input

FR	LCD AC drive signal input.
V_{DD}, V_{SS}	Logic power inputs
V0, V1, V4, V5	LCD drive power inputs. $V_{DD} \geq V0 \geq V1 \geq V4 \geq V5$

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Characteristics

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to 0.3	V
Supply voltage (2)	V5	–30.0 to 0.3	V
	V0, V1, V4	V5 –0.3 to 0.3	V
Input pin voltage	V_I	V_{SS} –0.3 to 0.3	V
Output pin voltage	V_O	V_{SS} –0.3 to 0.3	V
Output pin current (1)	I_O	20	mA
Output pin current (2)	I_{OCOM}	20	mA
Allowable power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature, time	T_{sol}	260°C, 10 s	—

Notes: 1. All voltages are given relative to V_{DD} = 0 V
2. V0,V1 and V4 must satisfy the condition
$V_{DD} \geq V0 \geq V1 \geq V4 \geq V5$
3. Exceeding the absolute maximum ratings can cause permanent damage to the device.
Functional operation under these conditions is not implied.
4. Moisture resistance of flat package can be reduced by the soldering process.
Care should be taken to avoid thermally stressing the package during board assembly.

● DC Electrical Characteristics

(Unless otherwise specified, V_{DD} = V0 = 0 V, V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Supply voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–4.5	V
Recommended operating voltage	V5		V5	–2.8	—	–12.0	V
Supply voltage (3)	V0	Recommended value	V0	–2.5	—	0	V
Supply voltage (4)	V1	Recommended value	V1	2/9·V5	—	V_{DD}	V
Supply voltage (5)	V4	Recommended value	V4	V5	—	7/9·V5	V
High-level input voltage	V_{IH}		DIO1, DIO2, YSCL, FR, SHL, $\overline{INH}$	0.2V_{SS}	—	—	V
Low-level input voltage	V_{IL}			—	—	0.8V_{SS}	V
High-level output voltage	V_{OH}	I_{OH} = –0.3 mA	DIO1, DIO2	–0.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 0.3 mA		—	—	V_{SS}+0.4	V
Input, I/O leakage current	V_{LI}	$V_{SS} \le V_I \le 0$ V	YSCL, SHL,$\overline{INH}$,FR	—	—	2.0	µA
	$V_{LI/O}$	$V_{SS} \le V_I \le 0$ V	DIO1, DIO2	—	—	5.0	µA
Static current	I_{DDS}	V5 = –12.0 to –28.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{COM}	|ΔV_{ON}| = 0.5V, V5=–20.0V	COM0 to COM67	V1, V4, output level	0.40	0.80	kΩ
		V5=–14.0V			0.50	1.00	
		V5=–8.0V			0.60	1.20	
		V5=–20.0V	COM0 to COM67	V0, V5, output level	0.60	1.20	
		V5=–14.0V			0.70	1.40	
		V5=–8.0V			0.90	1.80	
Current dissipation (1)	I_{SS1}	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 12 kHz, Frame frequency = 60 Hz; Input data: "H" every 1/200 duty no-load	V_{SS}	—	7	15.0	µA
Current dissipation (2)	I_{SS2}	V_{SS} = –5.0 V, V1 = –2.0 V, V4 = –18.0 V, V5 = –20.0 V, All other conditions are same as I_{SS1}	V5	—	7	15.0	µA
Input, I/O pin capacitance	C_I	T_a = 25°C	YSCL, SHL, $\overline{INH}$,FR	—	—	8.0	pF
	$C_{I/O}$		DIO1, DIO2	—	—	15.0	pF

● AC Electrical Characteristics

○ Input Timing

(V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL period	t_{CCL}		500	—	—	ns
YSCL "H" pulse width	t_{WCLH}		70	—	—	ns
YSCL "L" pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns

● AC Electrical Characteristics

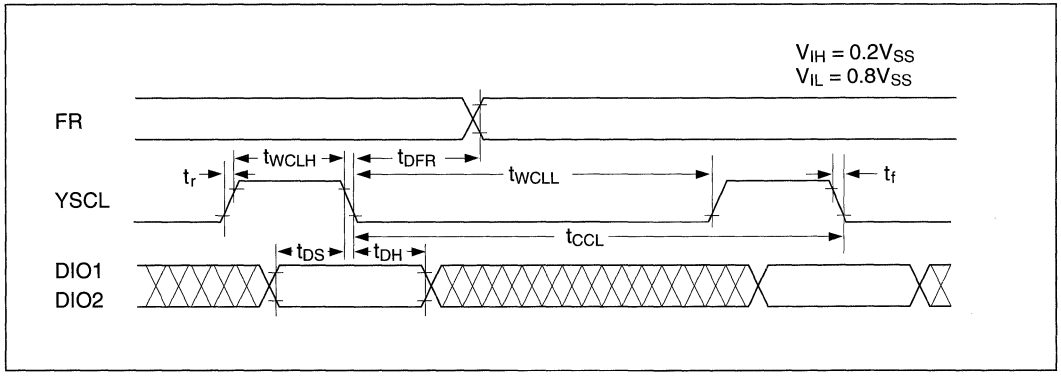
○ Output Timing

(V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

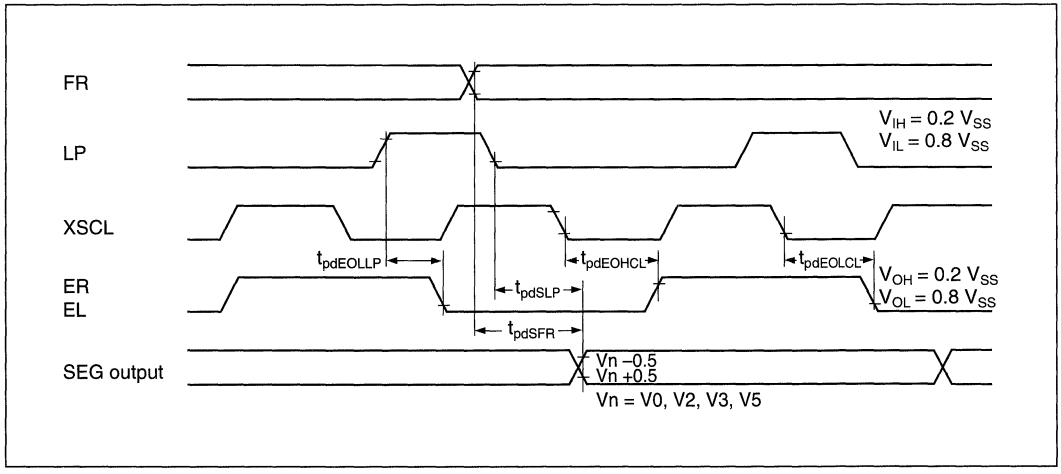
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL falling edge to DIO delay	t_{pdDOCL}	C_L = 15 pF	30	—	300	ns
YSCL falling edge to COM delay	t_{pdCCL}	V5 = –12.0 to –28.0 V C_L = 100 pF	—	—	3.0	µs
$\overline{INH}$ to COM delay	t_{pdCINH}		—	—	3.0	µs
FR to COM delay	t_{pdCFR}		—	—	3.0	µs

● Timing Chart

○ Input Timing

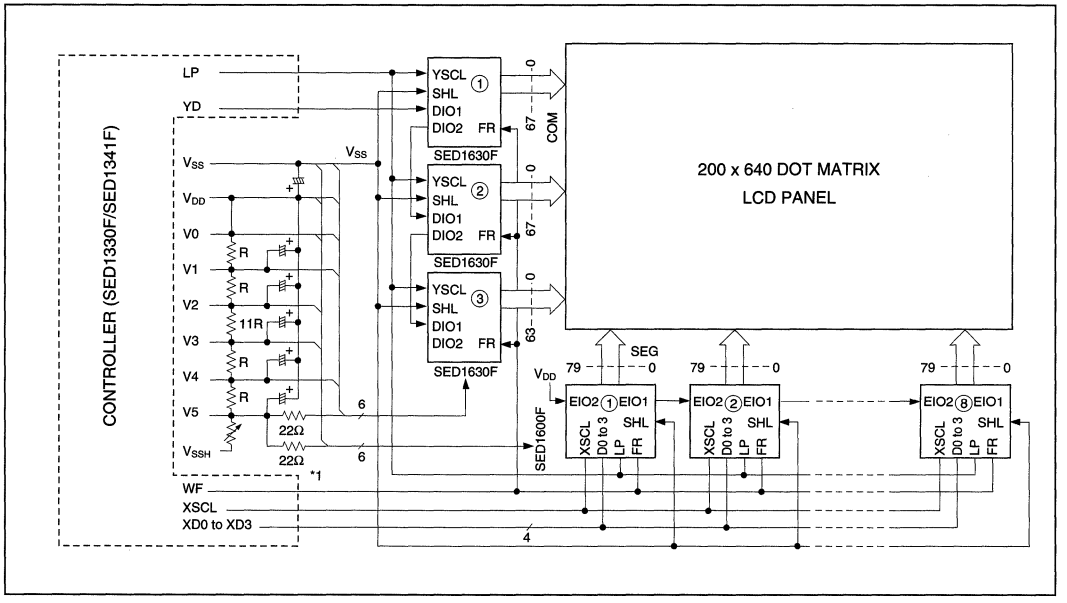


○ Output Timing



■ EXAMPLE OF APPLICATION (SED1610AA)

(for 200 × 640 DOT MATRIX LCD)



Note: * Be sure to connect an overcurrent protection resistor. Also, connect bypass capacitors (c) (0.01 μF) near pins Vss and V5 of each LSI for noise protection.

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

- **CMOS 100-bit Common Driver**
- **High Voltage Resistant Output**
- **CMOS High Voltage Resistant Process**

■ DESCRIPTION

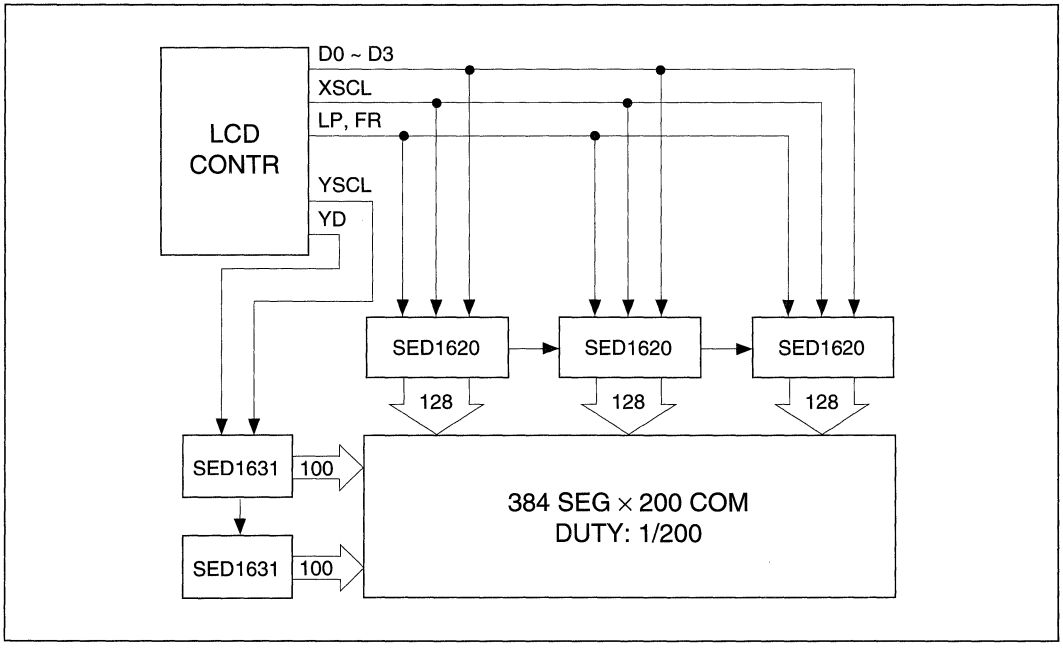
The SED1631 is a 100 output dot matrix LCD common (row) driver for driving a high-capacity LCD panel at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of LCD driving voltages. Due to the architecture of the SED1631, the LCD driving voltage V0 is isolated from V_{DD}. This provides the ability to adjust the offset bias independently of V_{DD}. These unique features allow the SED1631 to interface with a variety of LCD panels.

The SED1631 is used in conjunction with the SED1600 (80 segment driver), the SED1601 (80 segment driver) and the SED1620 (128 segment driver) to drive a large-capacity dot matrix LCD panel.

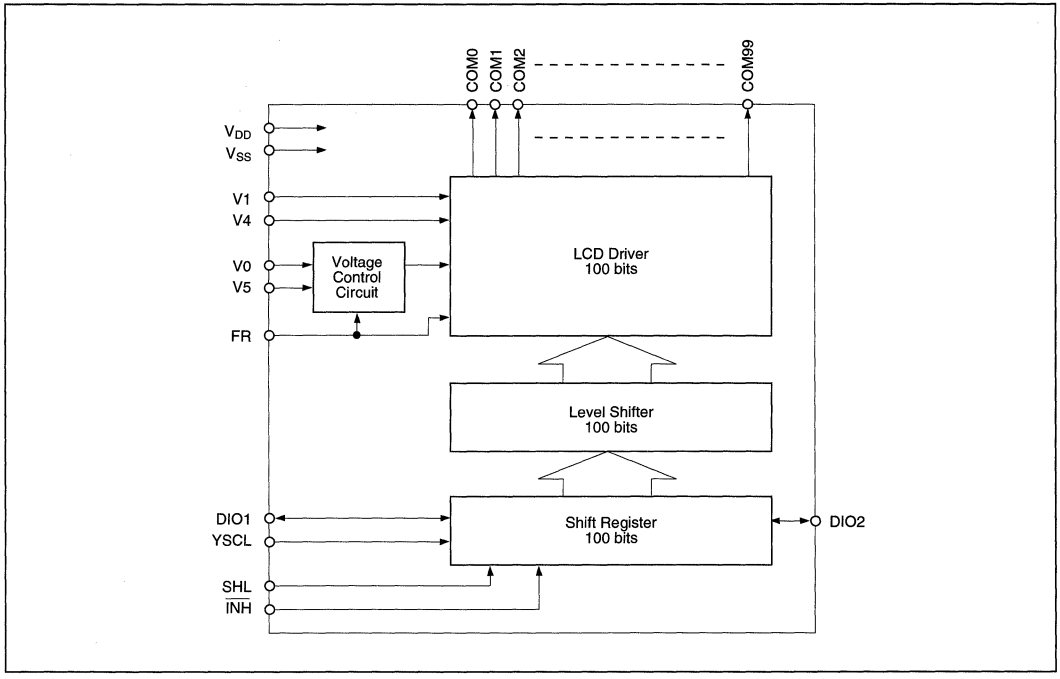
■ FEATURES

- Low-power CMOS technology
- 100-bit common (row) driver
- Duty cycle ..... 1/64 to 1/300
- Display blanking available
- Shift clock frequency ..... 2MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Selectable output shift direction
- Wide range of LCD voltage .... 12V to 28V
- Supply voltage ..... 5.0V ± 10%
- Package ..... DIE: .. Al pad (D_{0A})
  Au bump (D_{0B})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Pin Name	I/O	Function
COM0 to COM99	100 to 112 1 to 96	LCD drive common outputs.
$\overline{INH}$	98	Active low blanking control input.
YSCL	100	Data is shifted into the driver on the falling edge of this signal.
DI01,DI02	108, 97	Serial data input/output pins. Configured by SHL.
SHL	101	Shift direction and input/output select input.
FR	99	LCD AC drive signal input.
VDD, VSS	102, 103	Logic power inputs.
V0, V1, V4, V5	104, 105, 106, 107	LCD drive power inputs.

SHL	COM Data Shift Direction	DIO	
		1	2
L	0 → 99	input	output
H	99 → 0	output	input

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to 0.3	V
Supply voltage (2)	V5	–30.0 to 0.3	V
Supply voltage (3)	V0, V1, V4	V5 –0.3 to 0.3	V
Input voltage	V_I	V_{SS} –0.3 to 0.3	V
Output voltage	V_O	V_{SS} –0.3 to 0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OCOM}	20	mA
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–65 to 150	°C

Notes: 1. All voltages are given relative to V_{DD} = 0 V
2. V0,V1 and V4 must satisfy the condition $V_{DD} \geq V0 \geq V1 \geq V4 \geq V5$
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat package can be reduced by the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

● DC Electrical Characteristics

(Unless otherwise stated, V_{DD} = V0 = 0V, V_{SS} = –5.0V ± 10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Operating voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–4.5	V
Recommended operating voltage	V5		V5	–28.0	—	–12.0	V
Minimum operating voltage				—	—	–8.0	V
Operating voltage (2)	V0	Recommended value	V0	–2.5	—	0	V
Operating voltage (3)	V1	Recommended value	V1	2/9·V5	—	V_{DD}	V
Operating voltage (4)	V4	Recommended value	V4	V5	—	7/9·V5	V
High level input voltage	V_{IH}		DIO1, DIO2, YSCL, FR, SHL, INH	—	—	—	V
Low level input voltage	V_{IL}			—	—	0.8V_{SS}	V
High level output voltage	V_{OH}	I_{OH} = –0.3 mA	DIO1, DIO2	–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 0.3 mA		—	—	V_{SS}+0.4	V
Input leakage current	V_{LI}	$V_{SS} \le V_I \le 0V$	YSCL, SHL, INH, FR	—	—	2.0	µA
	$V_{LI/O}$	$V_{SS} \le V_I \le 0V$	DIO1, DIO2	—	—	5.0	µA
Stand-by current	I_{DDS}	V5 = –12.0 to –28.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{COM}	|ΔVON| = 0.5V, V5=–20.0V	V1, V4 Output level	—	0.40	0.80	kΩ
		V5=–14.0V	COM0 to COM99		0.50	1.00	
		V5=–0.8V			(0.60)	(1.20)	
		V5=–20.0V	V0, V5 Output level	—	0.60	1.20	
		V5=–14.0V			0.70	1.40	
		V5=–8.0V	COM0 to COM99		(0.90)	(1.20)	
Current dissipation (1)	I_{SS1}	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V = V_{SS}, f_{YSCL} = 12 kHz, Frame frequency = 60 Hz; Input data inverted bit by bit, No-load	V_{SS}	—	7	15.0	µA
Current dissipation (2)	I_{SS2}	V_{SS} = –5.0 V, V1 = –2.0 V, V4 = –18.0 V, V5 = –20.0 V, All other conditions are same as I_{SS1}	V5	—	7	15.0	µA
Input capacitance	C_I	T_a = 25°C	YSCL, SHL, INH, FR	—	—	8.0	pF
	$C_{I/O}$		DIO1, DIO2	—	—	15.0	pF

● AC Electrical Characteristics

○ Input Timing

(V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL period	t_{CCL}		500	—	—	ns
YSCL High-level pulse width	t_{WCLH}		70	—	—	ns
YSCL Low-level pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns

● AC Electrical Characteristics

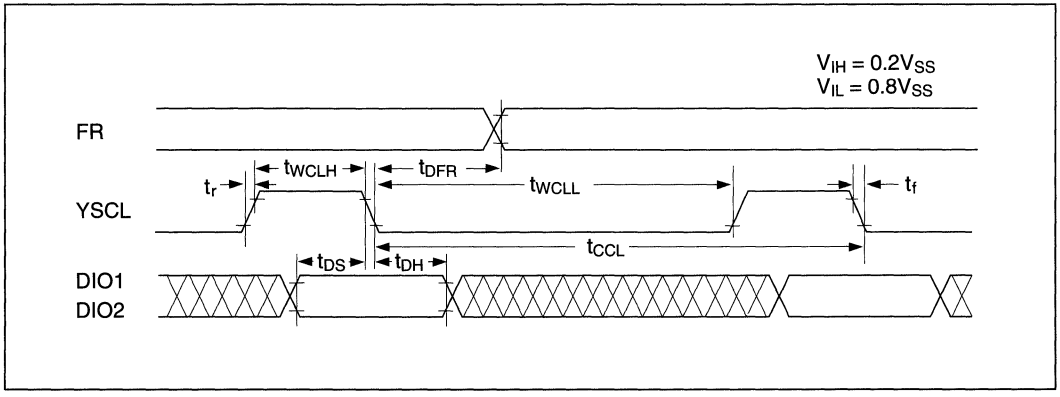
○ Output Timing

(V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

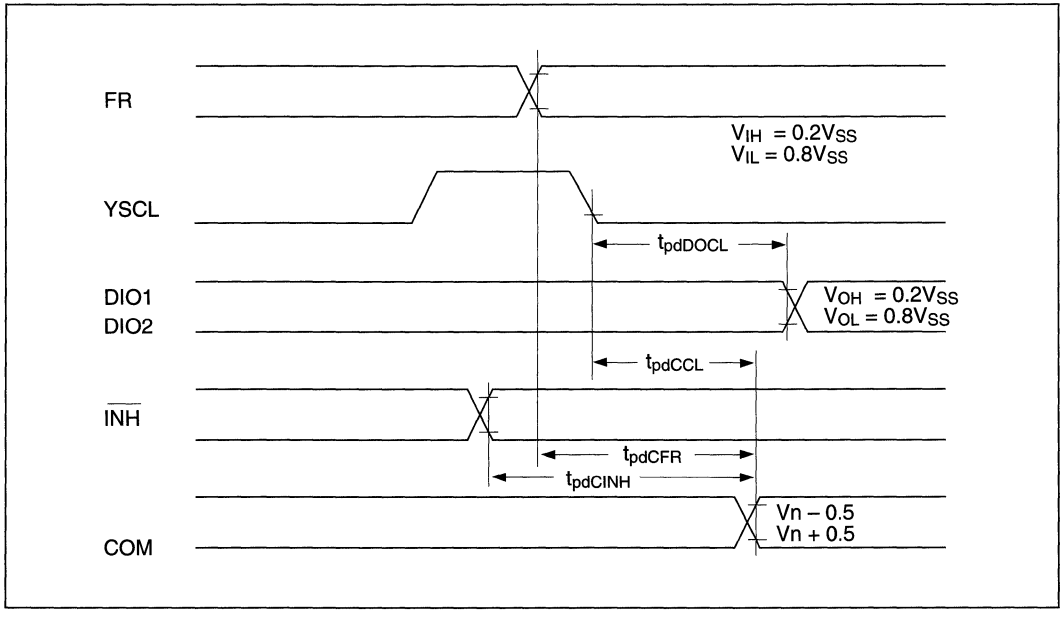
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(YSCL-fall to DIO) Delay time	t_{pdDOCL}	C_L = 15 pF	30	—	300	ns
(YSCL-fall to COM output) Delay time	t_{pdCCL}	V5 = –12.0 to –28.0 V C_L = 100 pF	—	—	3.0	µs
($\overline{INH}$ to COM output) Delay time	t_{pdCINH}		—	—	3.0	µs
(FR to COM output) Delay time	t_{pdCFR}		—	—	3.0	µs

● Timing Chart

○ Input Timing

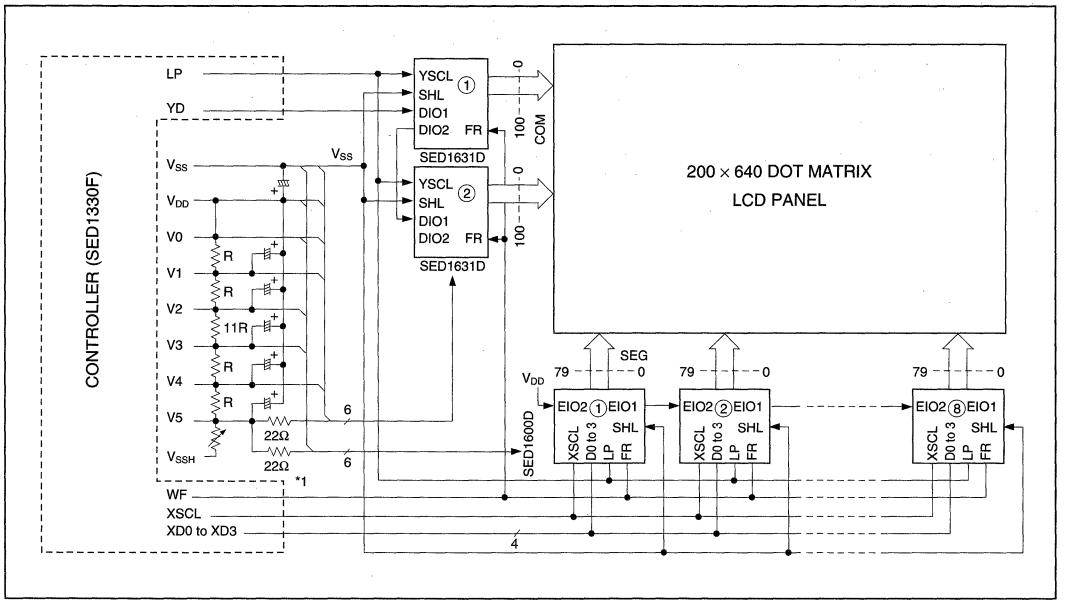


○ Output Timing



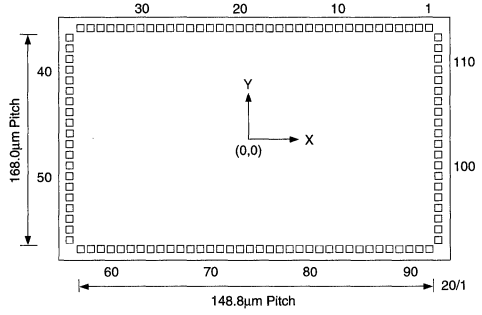
■ EXAMPLE OF APPLICATION

(for 200 × 640 DOT MATRIX LCD)



Note: * Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01 μF) near pins Vss and V5 of each LSI for noise protection.

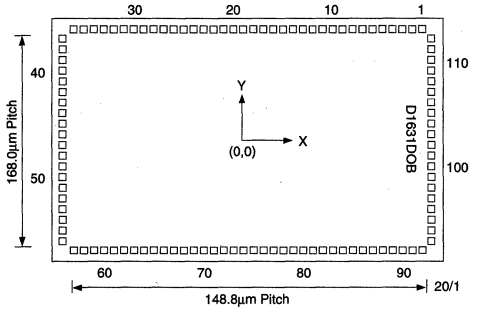
■ PAD LAYOUT (SED1631DOA)



Chip size	6.03mm × 4.01mm
Chip thickness	0.400mm ±0.025mm
Pad Size	108mm × 110mm (X) (Y)

Pad No.	Name	X (µm)	Y (µm)	Pad No.	Name	X (µm)	Y (µm)	Pad No.	Name	X (µm)	Y (µm)
1	COM5	2604	1839	39	COM43	–2847	1260	77	COM81	372	–1839
2	COM6	2455	1839	40	COM44	–2847	1092	78	COM82	521	–1839
3	COM7	2306	1839	41	COM45	–2847	924	79	COM83	670	–1839
4	COM8	2158	1839	42	COM46	–2847	756	80	COM84	818	–1839
5	COM9	2009	1839	43	COM47	–2847	588	81	COM85	967	–1839
6	COM10	1860	1839	44	COM48	–2847	420	82	COM86	1116	–1839
7	COM11	1711	1839	45	COM49	–2847	252	83	COM87	1265	–1839
8	COM12	1562	1839	46	COM50	–2847	84	84	COM88	1414	–1839
9	COM13	1414	1839	47	COM51	–2847	–84	85	COM89	1562	–1839
10	COM14	1265	1839	48	COM52	–2847	–252	86	COM90	1711	–1839
11	COM15	1116	1839	49	COM53	–2847	–420	87	COM91	1860	–1839
12	COM16	967	1839	50	COM54	–2847	–588	88	COM92	2009	–1839
13	COM17	818	1839	51	COM55	–2847	–756	89	COM93	2158	–1839
14	COM18	670	1839	52	COM56	–2847	–924	90	COM94	2306	–1839
15	COM19	521	1839	53	COM57	–2847	–1092	91	COM95	2455	–1839
16	COM20	372	1839	54	COM58	–2847	–1260	92	COM96	2604	–1839
17	COM21	223	1839	55	COM59	–2847	–1428	93	COM97	2847	–1596
18	COM22	74	1839	56	COM60	–2847	–1596	94	COM98	2847	–1428
19	COM23	–74	1839	57	COM61	–2604	–1834	95	COM99	2847	–1260
20	COM24	–223	1839	58	COM62	–2455	–1834	96	DIO2	2847	–1092
21	COM25	–372	1839	59	COM63	–2306	–1834	97	INH	2847	–924
22	COM26	–521	1839	60	COM64	–2158	–1834	98	FR	2847	–756
23	COM27	–670	1839	61	COM65	–2009	–1839	99	YSCL	2847	–588
24	COM28	–818	1839	62	COM66	–1860	–1839	100	SHL	2847	–420
25	COM29	–967	1839	63	COM67	–1711	–1839	101	VDD	2847	–252
26	COM30	–1116	1839	64	COM68	–1562	–1839	102	VSS	2847	–84
27	COM31	–1265	1839	65	COM69	–1414	–1839	103	V0	2847	84
28	COM32	–1414	1839	66	COM70	–1265	–1839	104	V1	2847	252
29	COM33	–1562	1839	67	COM71	–1116	–1839	105	V4	2847	420
30	COM34	–1711	1839	68	COM72	–967	–1839	106	V5	2847	588
31	COM35	–1860	1839	69	COM73	–818	–1839	107	DIO1	2847	756
32	COM36	–2009	1839	70	COM74	–670	–1839	108	COM0	2847	924
33	COM37	–2158	1839	71	COM75	–521	–1839	109	COM1	2847	1092
34	COM38	–2306	1839	72	COM76	–372	–1839	110	COM2	2847	1260
35	COM39	–2455	1839	73	COM77	–223	–1839	111	COM3	2847	1428
36	COM40	–2604	1839	74	COM78	–74	–1839	112	COM4	2847	1596
37	COM41	–2847	1596	75	COM79	74	–1839				
38	COM42	–2847	1428	76	COM80	223	–1839				

■ PAD LAYOUT (SED1631D0B)



Chip size	6.03mm × 4.01mm
Chip thickness	0.525mm ±0.025mm
Bump size	117µm × 105µm ±20µm
Bump height	20mm + 10/5µm

Pad No.	Pad Name	X (µm)	Y (µm)	Pad No.	Pad Name	X (µm)	Y (µm)	Pad No.	Pad Name	X (µm)	Y (µm)
1	COM5	2604	1834	39	COM43	–2842	1260	77	COM81	372	–1834
2	COM6	2455	1834	40	COM44	–2842	1092	78	COM82	521	–1834
3	COM7	2306	1834	41	COM45	–2842	924	79	COM83	670	–1834
4	COM8	2158	1834	42	COM46	–2842	756	80	COM84	818	–1834
5	COM9	2009	1834	43	COM47	–2842	588	81	COM85	967	–1834
6	COM10	1860	1834	44	COM48	–2842	420	82	COM86	1116	–1834
7	COM11	1711	1834	45	COM49	–2842	252	83	COM87	1265	–1834
8	COM12	1562	1834	46	COM50	–2842	84	84	COM88	1414	–1834
9	COM13	1414	1834	47	COM51	–2842	–84	85	COM89	1562	–1834
10	COM14	1265	1834	48	COM52	–2842	–252	86	COM90	1711	–1834
11	COM15	1116	1834	49	COM53	–2842	–420	87	COM91	1860	–1834
12	COM16	967	1834	50	COM54	–2842	–588	88	COM92	2009	–1834
13	COM17	818	1834	51	COM55	–2842	–756	89	COM93	2158	–1834
14	COM18	670	1834	52	COM56	–2842	–924	90	COM94	2306	–1834
15	COM19	521	1834	53	COM57	–2842	–1092	91	COM95	2455	–1834
16	COM20	372	1834	54	COM58	–2842	–1260	92	COM96	2604	–1834
17	COM21	223	1834	55	COM59	–2842	–1428	93	COM97	2842	–1596
18	COM22	74	1834	56	COM60	–2842	–1596	94	COM98	2842	–1428
19	COM23	–74	1834	57	COM61	–2604	–1834	95	COM99	2842	–1260
20	COM24	–223	1834	58	COM62	–2455	–1834	96	DIO2	2842	–1092
21	COM25	–372	1834	59	COM63	–2306	–1834	97	INH	2842	–924
22	COM26	–521	1834	60	COM64	–2158	–1834	98	FR	2842	–756
23	COM27	–670	1834	61	COM65	–2009	–1834	99	YSCL	2842	–588
24	COM28	–818	1834	62	COM66	–1860	–1834	100	SHL	2842	–420
25	COM29	–967	1834	63	COM67	–1711	–1834	101	VDD	2842	–252
26	COM30	–1116	1834	64	COM68	–1562	–1834	102	VSS	2842	–84
27	COM31	–1265	1834	65	COM69	–1414	–1834	103	V0	2842	84
28	COM32	–1414	1834	66	COM70	–1265	–1834	104	V1	2842	252
29	COM33	–1562	1834	67	COM71	–1116	–1834	105	V4	2842	420
30	COM34	–1711	1834	68	COM72	–967	–1834	106	V5	2842	588
31	COM35	–1860	1834	69	COM73	–818	–1834	107	DIO1	2842	756
32	COM36	–2009	1834	70	COM74	–670	–1834	108	COM0	2842	924
33	COM37	–2158	1834	71	COM75	–521	–1834	109	COM1	2842	1092
34	COM38	–2306	1834	72	COM76	–372	–1834	110	COM2	2842	1260
35	COM39	–2455	1834	73	COM77	–223	–1834	111	COM3	2842	1428
36	COM40	–2604	1834	74	COM78	–74	–1834	112	COM4	2842	1596
37	COM41	–2842	1596	75	COM79	74	–1834				
38	COM42	–2842	1428	76	COM80	223	–1834				

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

- **CMOS 86-bit Common Driver**
- **High Voltage Resistant Output**
- **Max 1/300 in Display Duty**
- **CMOS High Voltage Resistant Process**

■ DESCRIPTION

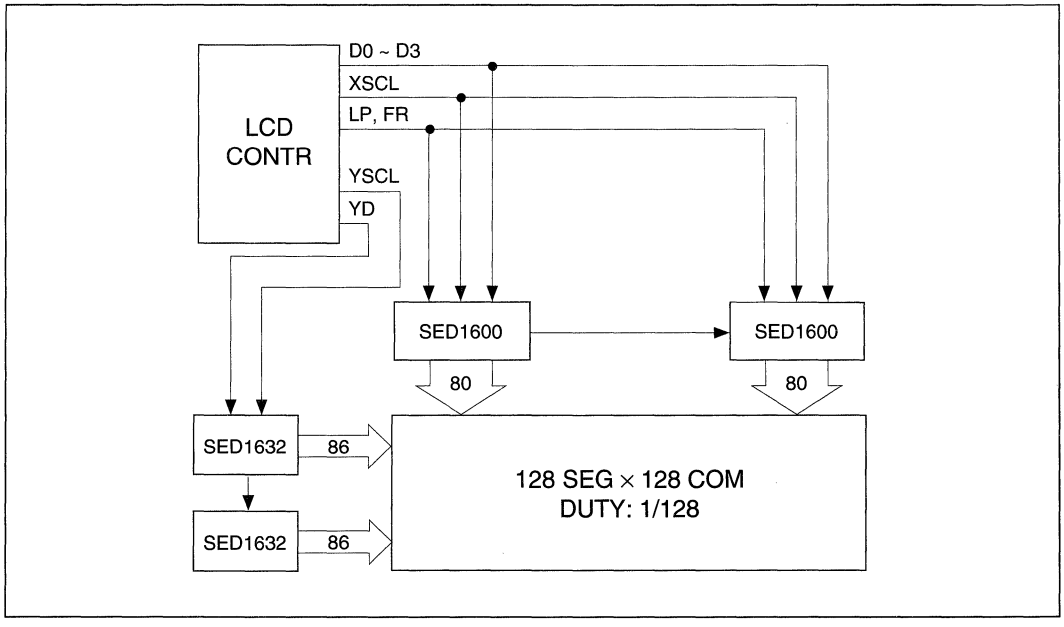
The SED1632 is an 86 output dot matrix LCD common (row) driver for driving a high-capacity LCD panel at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of LCD driving voltages. Due to the architecture of the SED1632, the LCD driving power is isolated from V_{DD}. This provides the ability to adjust the offset bias independently of V_{DD}. These unique features allow the SED1632 to interface with a variety of LCD panels.

The SED1632 is used in conjunction with the SED1600 (80 segment driver), the SED1601 (80 segment driver) and the SED1620 (128 segment driver) to drive a large-capacity dot matrix LCD panel.

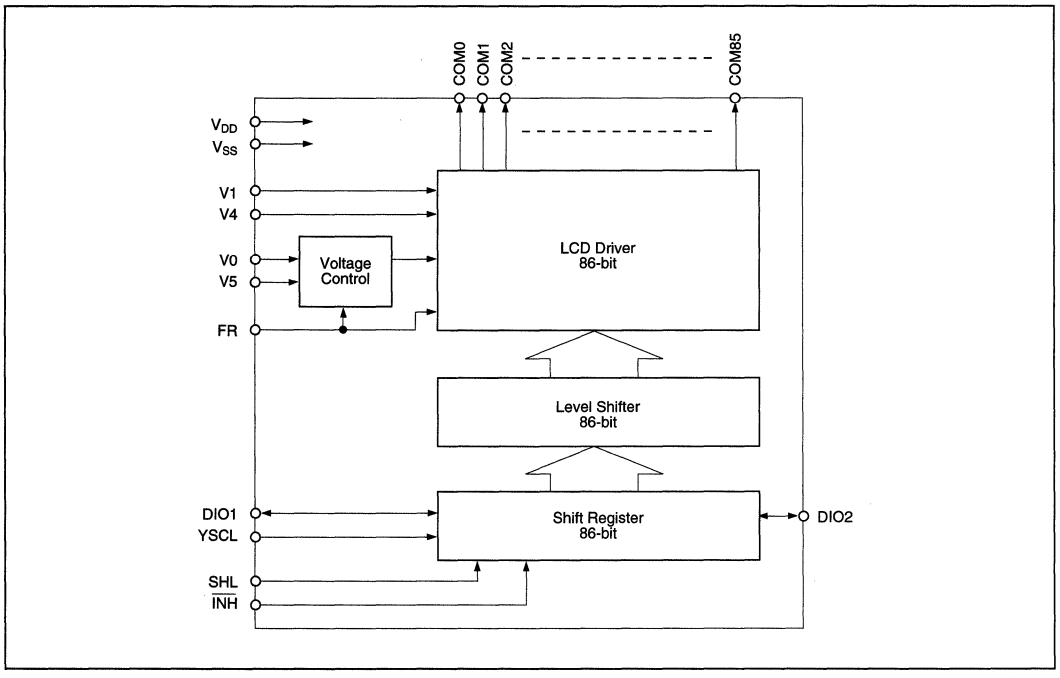
■ FEATURES

- Low-power CMOS technology
- 86-bit common (row) driver
- Duty cycle ..... 1/64 to 1/300
- Display blanking available
- Shift clock frequency ..... 2MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Selectable output shift direction
- Wide range of LCD voltage .... –12 to –28V
- Supply voltage ..... 5.0V ± 10%
- Package ..... DIE: Al pad (D_{OA})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Pin Name	Function
COM0 to COM85	LCD driving common (row) outputs. Each output changes at the falling edge of YSCL.
$\overline{INH}$	Controls all common outputs to nonselect level (V4 when FR = L, V1 when FR = H) (low active). Contents of shift register are cleared.
YSCL	Shift clock of serial data (falling edge trigger).
DI01,DI02	Serial transfer data I/O, which is controlled by SHL input. Output changes at falling edge of YSCL.
SHL	Shift direction selection and DIO pin control.
FR	AC signal of LCD driving outputs.
V_{DD}, V_{SS}	Logic circuit power. V_{DD}: 0V (GND) V_{SS}: –5.0 V
V0, V1, V4, V5	LCD driving power. V5: –12 to –28V $V_{DD} \geq V0 \geq V1 > V4 \geq V5$

SHL	COM Data Shift Direction	DIO	
		1	2
L	85 ← 0	Input	Output
H	85 → 0	Output	Input

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V5	–30.0 to +0.3	V
Supply voltage (2)	V0, V1, V4	V5 –0.3 to +0.3	V
Input voltage (1)	V_I	V_{SS} –0.3 to +0.3	V
Output voltage (1)	V_O	V_{SS} –0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OSEG}	20	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature, time	T_{sol}	260°C, 10s (at lead)	—
Allowable power dissipation	P_D	300	mW

Notes: 1. V0, V1 and V4 must always satisfy the condition $V_{DD} \geq V0 \geq V1 \geq V4 \geq V5$.
2. If the power supply for the logic circuit is floated while the liquid crystal driving power supply is applied, the LSI can be irreparably damaged. Be especially careful when the system power is being turned on or off.

● DC Electrical Characteristics

(Unless otherwise specified, V_{DD} = V0 = 0 V, V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Operating voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–4.5	V
Recommended operating voltage Minimum operating voltage	V5		V5	–28.0	—	–12.0 –8.0	V
Operating voltage (2)	V0	Recommended value	V0	–2.5	—	0	V
Operating voltage (4)	V1	Recommended value	V1	2/9·V5	—	V_{DD}	V
Operating voltage (5)	V4	Recommended value	V4	V5	—	7/9·V5	V
"H" input voltage	V_{IH}		DIO1, DIO2, YSCL, FR, SHL, INH	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}			—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH} = –0.3 mA	DIO1, DIO2	–0.4	—	—	V
"L" level output voltage	V_{OL}	I_{OL} = 0.3 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_I \le 0$ V	YSCL, SHL, INH,FR	—	—	2.0	µA
	$I_{LI/O}$	$V_{SS} \le V_I \le 0$ V	DIO1, DIO2	—	—	5.0	µA
Stand–by current	I_{DDS}	V5 = –12.0 to –28.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{SEG}	|ΔV_{ON}| = 0.5 V, V5=–20.0V V1	COM0 to COM85	—	0.40	0.80	kΩ
		|ΔV_{ON}| = 0.5 V, V5=–14.0V V4		—	0.50	1.00	
		|ΔV_{ON}| = 0.5 V, V5=–20.0V V0,		—	0.60	1.20	
		|ΔV_{ON}| = 0.5 V, V5=–14.0V V5		—	0.70	1.40	
Current dissipation (1)	I_{SSO1}	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 12 kHz, Frame period = 60 Hz; Input data: "H" every 1/200 duty No-load	V_{SS}	—	7	15.0	µA
Current dissipation (2)	I_{SSO2}	V_{SS} = –5.0 V, V1 = –2.0 V V4 = –18.0 V, V5 = –20.0 V All other conditions are same as I_{SSO1}	V5	—	7	15.0	µA
Input capacitance	C_I	T_a = 25°C	YSCL, SHL, INH,FR	—	—	8.0	pF
	$C_{I/O}$		DIO1, DIO2	—	—	15.0	pF

● AC Characteristics

○ Input Timing

(V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL period	t_{CCL}		500	—	—	ns
YSCL "H" pulse width	t_{WCLH}		70	—	—	ns
YSCL "L" pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns

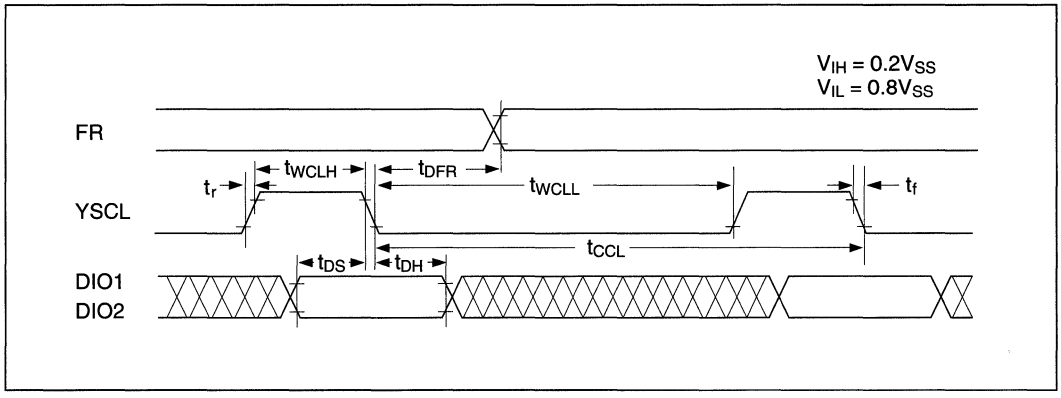
○ Output Timing

(V_{SS} = –5.0 V ±10%, Ta = –20 to 75°C)

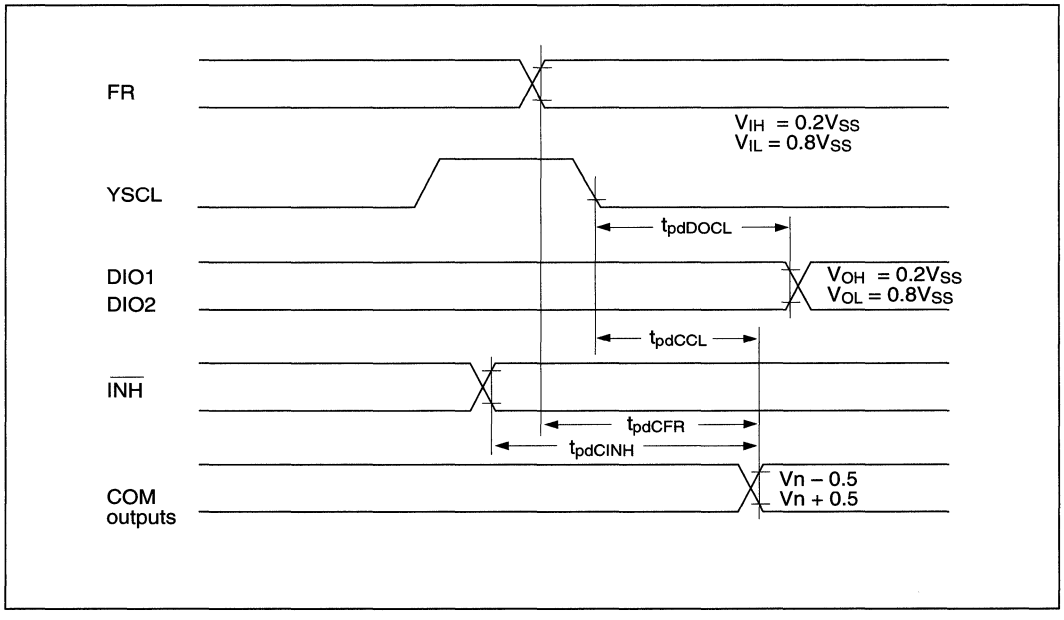
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(YSCL-fall to DIO) Delay time	t_{pdDOCL}	C_L = 15 pF	30	—	300	ns
(YSCL-fall to COM output) Delay time	t_{pdCCL}	V5 = –12.0 to –28.0 V C_L = 100 pF	—	—	3.0	µs
($\overline{INH}$ to COM output) Delay time	t_{pdCINH}					
(FR to COM output) Delay time	t_{pdCFR}		—	—	3.0	µs

● Timing Chart

○ Input Timing

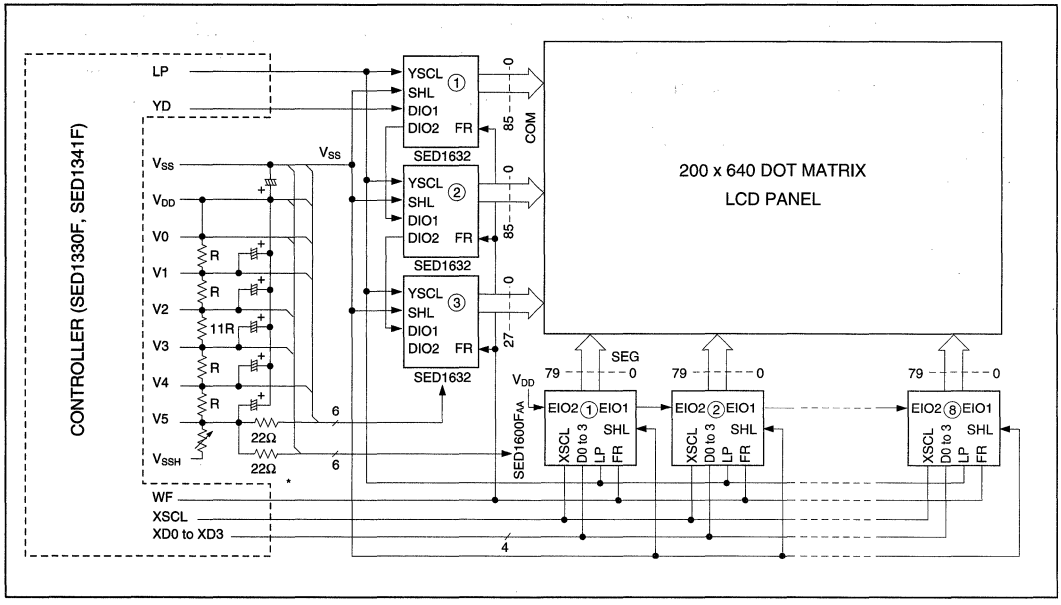


○ Output Timing



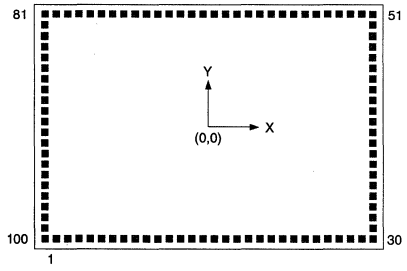
■ EXAMPLE OF APPLICATION

(for 200 × 640 DOT MATRIX LCD)



Note: * Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01 μF) near pins Vss and V5 of each LSI for noise protection.

■ PAD LAYOUT



Chip size	6.03mm × 4.01mm
Chip thickness	0.400mm ±0.025mm
Pad surface area	100mm × 100mm

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	COM2	–2852	–1844	35	COM36	2852	–944	69	COM69	–593	1844
2	COM3	–2612	–1844	36	COM37	2852	–764	70	COM70	–762	1844
3	COM4	–2382	–1844	37	COM38	2852	–594	71	COM71	–932	1844
4	COM5	–2162	–1844	38	COM39	2852	–425	72	COM72	–1112	1844
5	COM6	–1942	–1844	39	COM40	2852	–255	73	COM73	–1292	1844
6	COM7	–1742	–1844	40	COM41	2852	–86	74	COM74	–1472	1844
7	COM8	–1542	–1844	41	COM42	2852	86	75	COM75	–1652	1844
8	COM9	–1342	–1844	42	COM43	2852	255	76	COM76	–1832	1844
9	COM10	–1142	–1844	43	COM44	2852	425	77	COM77	–2012	1844
10	COM11	–962	–1844	44	COM45	2852	594	78	COM78	–2212	1844
11	COM12	–782	–1844	45	COM46	2852	764	79	COM79	–2412	1844
12	COM13	–602	–1844	46	COM47	2852	944	80	COM80	–2632	1844
13	COM14	–422	–1844	47	COM48	2852	1124	81	COM81	–2852	1844
14	COM15	–252	–1844	48	COM49	2852	1304	82	COM82	–2852	1666
15	COM16	–82	–1844	49	COM50	2852	1484	83	COM83	–2852	1489
16	COM17	82	–1844	50	NC	2852	1664	84	COM84	–2852	1313
17	COM18	252	–1844	51	COM51	2852	1844	85	COM85	–2852	1137
18	COM19	422	–1844	52	COM52	2612	1844	86	DIO2	–2852	961
19	COM20	602	–1844	53	COM53	2382	1844	87	$\overline{INH}$	–2852	794
20	COM21	782	–1844	54	COM54	2162	1844	88	FR	–2852	628
21	COM22	962	–1844	55	COM55	1942	1844	89	YSCL	–2852	462
22	COM23	1142	–1844	56	COM56	1742	1844	90	SHL	–2852	295
23	COM24	1342	–1844	57	COM57	1542	1844	91	VDD	–2852	129
24	COM25	1542	–1844	58	COM58	1342	1844	92	Vss	–2852	–38
25	COM26	1742	–1844	59	COM59	1142	1844	93	Vo	–2852	–425
26	COM27	1942	–1844	60	COM60	962	1844	94	V1	–2852	–594
27	COM28	2162	–1844	61	COM61	782	1844	95	V4	–2852	–764
28	COM29	2382	–1844	62	COM62	602	1844	96	V5	–2852	–944
29	COM30	2612	–1844	63	COM63	422	1844	97	DIO1	–2852	–1124
30	COM31	2852	–1844	64	COM64	252	1844	98	COM0	–2852	–1304
31	COM32	2852	–1664	65	COM65	84	1844	99	COM1	–2852	–1484
32	COM33	2852	–1484	66	COM66	–84	1844	100	NC	–2852	–1664
33	COM34	2852	–1304	67	COM67	–254	1844				
34	COM35	2852	–1124	68	COM68	–423	1844				

LOW-POWER 100-BIT LCD COMMON DRIVER

■ DESCRIPTION

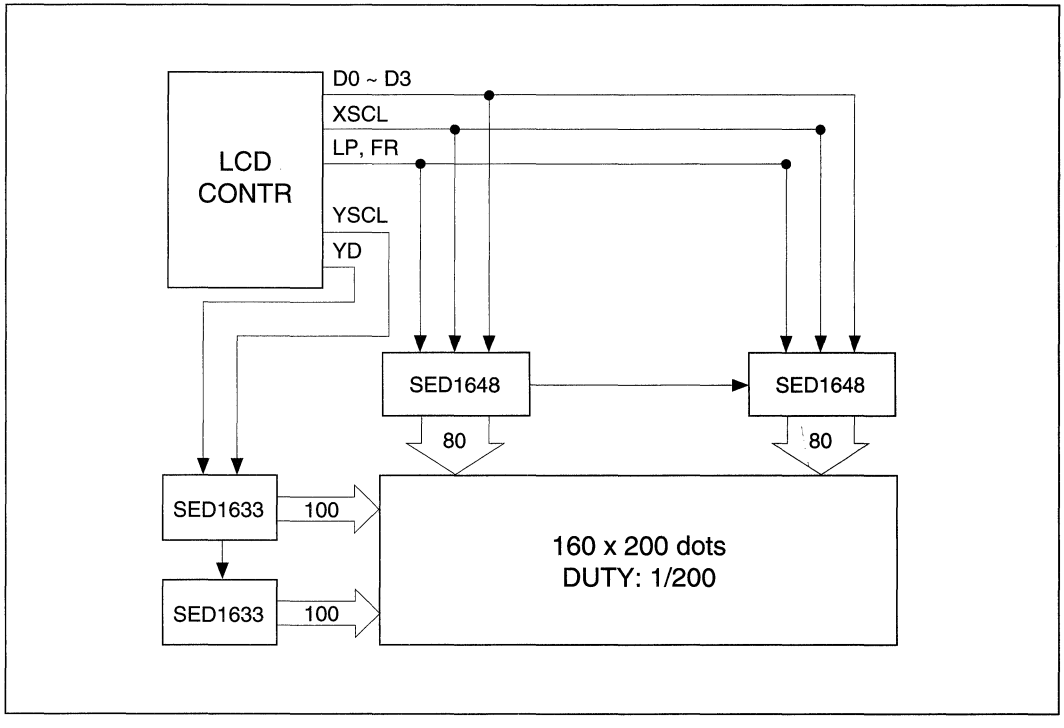
The SED1633 is a 100-output dot matrix LCD common (row) driver for driving high-capacity LCD panels at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of LCD driving voltages, and has its maximum drive voltage, VO, isolated from V_{DD} for flexibility of bias voltage generation.

The SED1633 is used in conjunction with the SED1648 (80-output segment driver) or the SED1600 (80-bit segment driver) to drive a large-capacity dot matrix LCD panel).

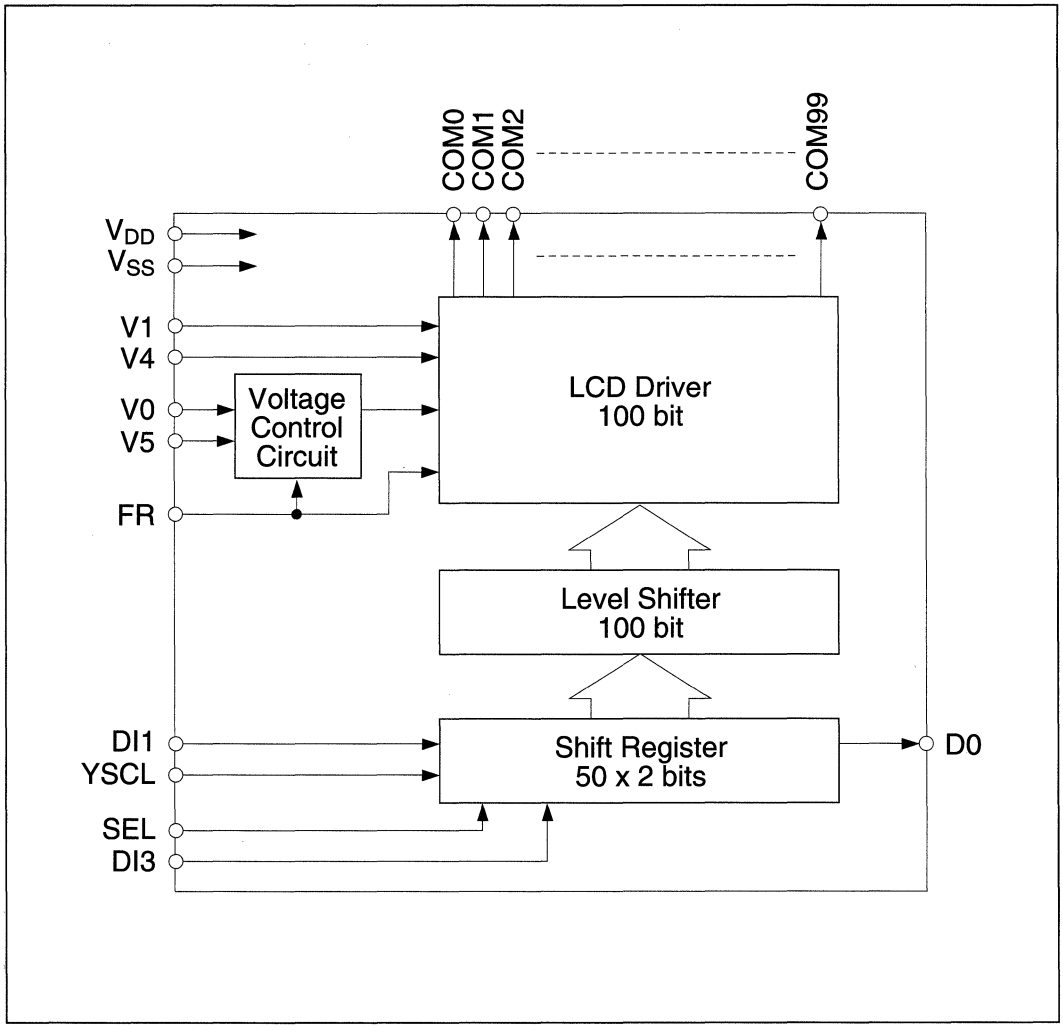
■ FEATURES

- Low-power CMOS technology
- 100-bit (50 × 2 structure) common (row) driver
- Duty cycle ..... 1/64 to 1/300
- Low output impedance 500Ω typ (V1, V4 level)
  700Ω typ (VO, V5 level)
- Duty cycle ..... 1/100 to 1/300
- Ability to adjust offset bias of the LCD relative to V_{DD}
- Non-biased display off function
- Pin selection of the output shift direction
- LCD voltage ..... –8 to –28V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... Al pad (D_{1A})
  Au bump (D_{1B})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Shift Register

This is a bidirectional shift register for common data transmission.

● Shift Direction

SED1633	COM 0 → COM 99	
SED1634	COM 99 → COM 0	Reference

● Level Shifter

This is a level interface circuit for shifting the signal voltage from the logic system level to the LCD driver system level.

● LCD Drivers and Voltage Controller Circuit

Outputs the LCD driver voltage.

The relationships between the content of the shift register, the alternating signal FR, and the common output voltage are as shown in the table below:

Contents of Shift Register	FR	COM Output Voltage	
H	H	V5	Select level
	L	V0	
L	H	V1	Non-select level
	L	V4	

■ PIN DESCRIPTION

Pin Name	I/O	Function	No. of Pins
COM0-COM99	O	LCD driver common (row) output Changes on the falling edge of the YSCL signal.	100
DI1, DI3	I	Serial data input for the 100 bit shift register. DI3 is the intermediate shift input. (When DI3 is unused, tie it to V_{DD} or V_{SS}.)	2
YSCL	I	Serial data shift clock input. Scanning data is shifted at the falling edge.	1
FR	I	LCD driver output AC signal input	1
V_{DD}, V_{SS}	Power	Power source for logic. V_{DD}: 0V (GND). V_{SS}: –5.0V	2
V0, V1, V4, V5	Power	Power source for LCD driver. V5: –12 to –28 V $V_{DD} \geq V0 \geq V1 > V4 \geq V5$	4
SEL	I	Shift Register Operating Configuration Selection:	1
DO	O	Shift register data output. The output changes with the falling edge of the YSCL signal.	1

SEL	Shift Register Configuration	DI3
H	50 × 2	Input
L	100 × 1	H/L

Total: 112

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Power voltage (1)	Vss	–7.0 to +0.3	V
Power voltage (2)	V5	–30.0 to +0.3	V
Power voltage (3)	V0, V1, V4	V5 – 0.3 to + 0.3	V
Input voltage	VI	Vss – 0.3 to + 0.3	V
Output voltage	VO	Vss – 0.3 to + 0.3	V
Output current (1)	IO	20	mA
Output current (2)	IOCOM	20	mA
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–65 to +150	°C

Notes: *1. The voltages are all relative to V_{DD} = 0V.

*2. Ensure that the relationship between V0, V1, and V4 is always as follows: $V_{DD} \geq V0 \geq V1 \geq V4 \geq V5$.

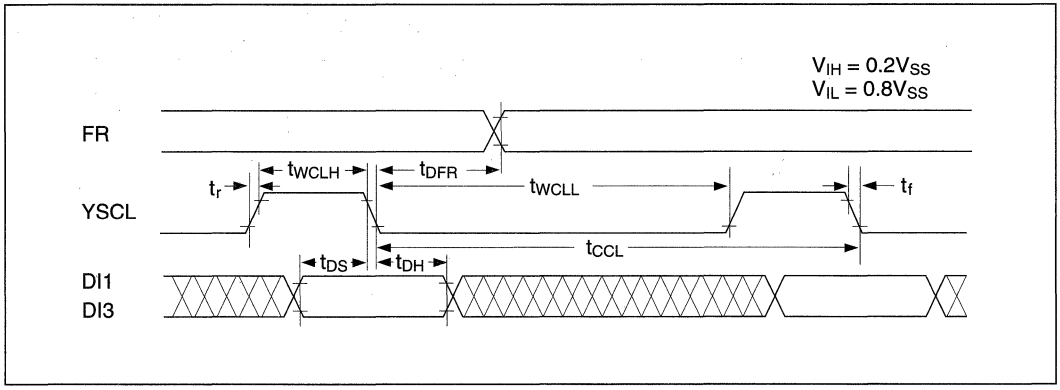
*3. The LSI may be permanently damaged if the logic system power is floating or Vss is less than or equal to –2.6V when power is applied to the LC drive circuit system. Special caution must be paid to the power sequences when turning the power on and off.

● DC Electrical Characteristics

Unless otherwise specified, V_{DD} = V0 = 0V, V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Applicable Pins	Min	Typ	Max	Unit
Power voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V5		V5	–28.0	—	–12.0	V
Possible operating voltage	V5	Function	V5	—	—	–8.0	V
Power voltage (2)	V0	Recommended value	V0	–2.5	—	0	V
Power voltage (3) Power voltage (4)	V1 V4	Recommended value	V1 V4	2/9 × V5 V5	—	V_{DD} 7/9 × V5	V
High-level input voltage	V_{IH}	V_{SS} = –2.7 to –5.5V	DI1, YSCL, SEL, DI3, FR	0.2 × Vss	—	—	V
Low-level input voltage	V_{IL}			—	—	0.8 × Vss	V
High-level output voltage	V_{OH}	I_{OH} = –0.3mA	DO	–0.4	—	—	V
		I_{OH} = –0.2mA (V_{SS} = –2.7 to –4.5V)					
Low-level output voltage	V_{OL}	I_{OL} = 0.3mA		—	—	Vss + 0.4	V
		I_{OL} = 0.2mA (V_{SS} = –2.7 to –4.5V)					
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	YSCL, SEL, DI3, FR	—	—	2.0	µA
I/O leakage current	I_{LO}	$V_{SS} \le V_{IN} \le 0V$	DI1, DO	—	—	5.0	µA
Static current	I_{DDS}	V5 = –12.0 to –28.0V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{COM}	$\Delta\lvert V_{ON}\rvert$ = 0.5V, V5 = –20.0V	When outputting the V1, V4 levels; COM0 ~ COM99	—	0.40	0.80	KΩ
		V5 = –14.0V			0.50	1.00	
		*(V5 = –8.0V)			(0.60)	(1.20)	
		V5 = –20.0V	When outputting the V0, V5 levels; *Reference value	—	0.60	1.20	
		V5 = –14.0V			0.70	1.40	
		*(V5 = –8.0V)			(0.90)	(1.80)	
Average operating current consumption (1)	I_{SS1}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 12KHz, Frame frequency = 60KHz, Input data: 1/200, "H" is without load on each duty cycle	Vss	—	7	15	µA
		V_{SS} = –3.0V; other parameters are identical		—	5	10	
Average operating current consumption (2)	I_{SS2}	V_{SS} = –5.0V, V1 = –2.0V, V4 = –18.0V, V5 = –20.0V; other parameters are the same as for I_{SS1}	V5	—	7	15	µA
Input terminal capacitance	C_I	T_a = 25°C	YSCL, SEL, DI3, FR	—	—	8	pF
I/O terminal capacitance	$C_{I/O}$		DI1, DO	—	—	15	pF

- **AC Characteristics**
  - **Input Timing Characteristics**



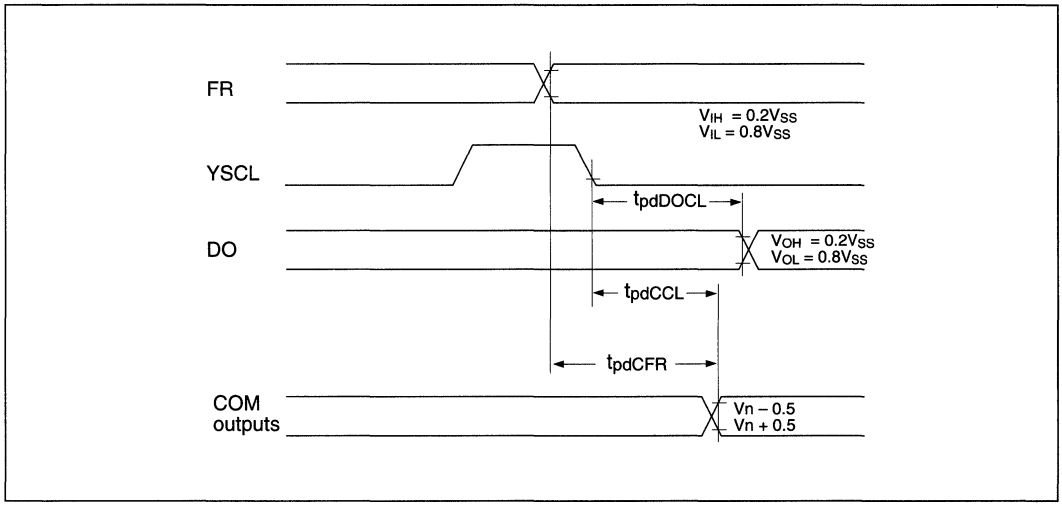
V_{SS} = –5.0 ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	tr		—	50	ns
Input signal fall time	tf		—	50	ns
YSCL frequency	t_{CCL}		500	—	ns
YSCL high-level pulse width	t_{WCLH}		70	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		100	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		–500	500	ns

V_{SS} = –2.7 to –4.5V, Ta = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	tr		—	50	ns
Input signal fall time	tf		—	50	ns
YSCL frequency	t_{CCL}		1000	—	ns
YSCL high-level pulse width	t_{WCLH}		160	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		200	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		–500	500	ns

○ Output Timing Characteristics



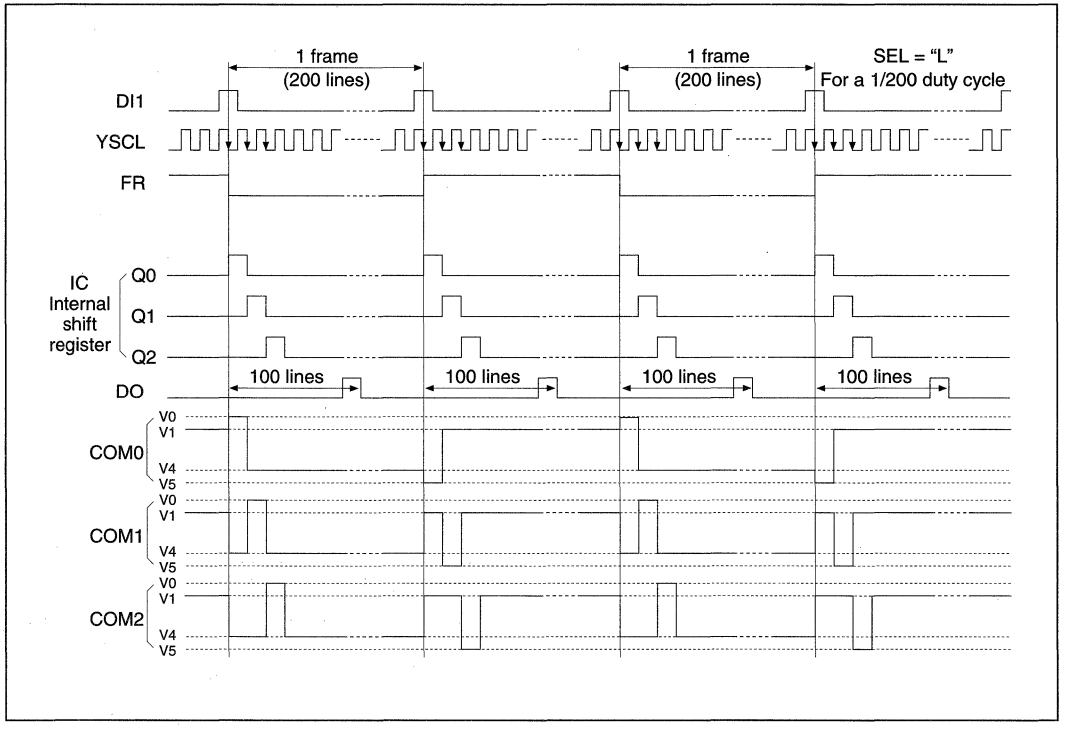
V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → D0) delay time	t_{pdDOCL}	CL = 15pF	30	300	ns
(YSCL fall → COM output) delay time	t_{pdCCL}	V5 = –12.0 to –28.0V	—	3.0	µs
(FR → COM output) delay time	t_{pdCFR}	CL = 100pF	—	3.0	µs

V_{SS} = –2.7 to –4.5V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → D0) delay time	t_{pdDOCL}	CL = 15pF	60	600	ns
(YSCL fall → COM output) delay time	t_{pdCCL}	V5 = –12.0 to –28.0V	—	3.0	µs
(FR → COM output) delay time	t_{pdCFR}	CL = 100pF	—	3.0	µs

- **Timing Diagram**



■ LCD DRIVING POWER

- **Method of Forming Each Voltage Level**

The simplest way to obtain the voltage levels for driving the LCs is to use resistive voltage dividers, as shown in the example connection figure. Because a high quality display requires precise and stable voltage levels, the values of the dividing resistances must be set at the low end of the tolerance range of the power capacity.

When there is the need to operate with low power, the values of the voltage dividing resisters must be set high, and the LCs must be driven by an op amp voltage follower. In consideration of the use of op amps, V0 (the highest voltage setting for driving LCs) and V_{DD} are separated and given separate terminals.

However, when the voltage level of V0 is below V_{DD} and the voltage difference between the two is large, the performance of the LC output driver is reduced. Therefore ensure that the voltage gap between V0 and V_{DD} is in the range of 0V to 2.5V.

Connect V0 and V_{DD} when an op amp is not used.

- **Cautions During Power Up and Power Down**

Because of the high voltage of the LC driving system of this LSI, if the power to the logic system is floating when a high voltage is applied to the LC driving system, then too much current will flow, causing damage to the LSI.

Follow the sequences below during power up and power down:

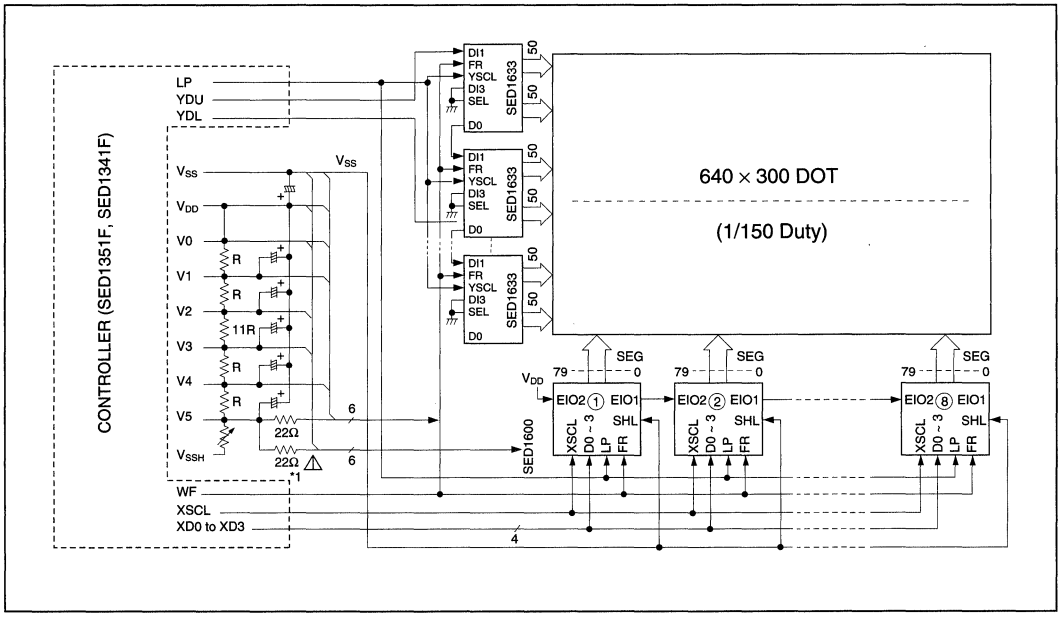
Power up: Logic system on → LC drive system on (or simultaneous)

Power down: LC drive system off → Logic system off (or simultaneous)

In order to prevent excessive current, insert a guard resistance of at least 22 Ω in series with V5.

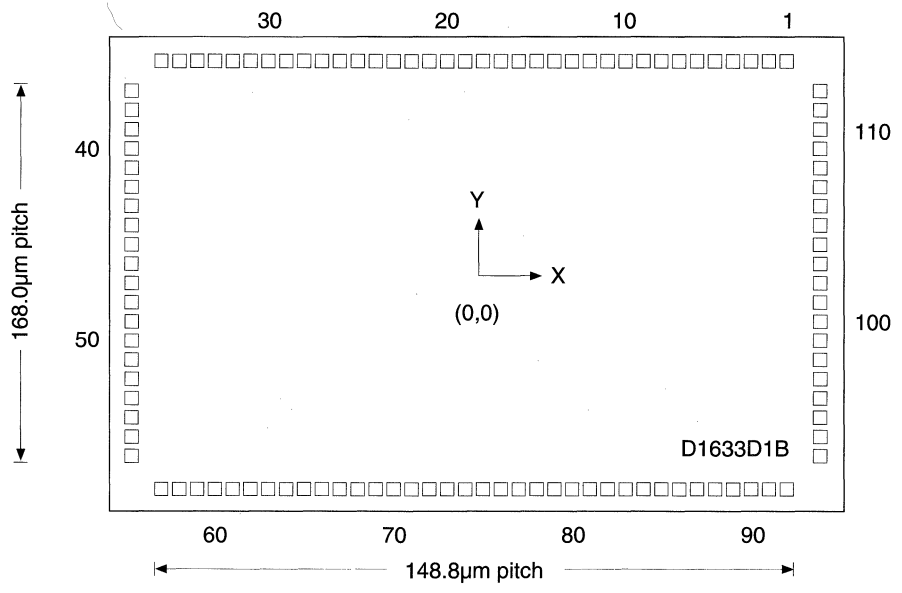
■ EXAMPLE OF CONNECTION

● Connections for a 640 × 300 dot matrix LCD



Note: *1. A guard resistance must be used to prevent excessive current. Moreover, a bypass capacitor (0.01μF) should be used near the Vss and V5 pins of each LSI to prevent noise.

■ PAD LAYOUT



SED1663D1A Specifications (The Al Pad Model)

Chip size ..... 6.03 mm × 4.01 mm
Chip thickness ..... 0.400 mm
Pad opening ..... 101 mm (X) × 110 mm (Y)
(where the Y direction is the direction of the chip center line)

SED1663D1B Specifications (The Au Bump Model)

Chip size ..... 6.03 mm × 4.01 mm
Chip thickness ..... 0.525 mm
Bump size ..... 117 µm × 105 µm
+10 µm
Bump height: ..... 20 µm
(reference values) –5 µm

■ PAD COORDINATES

Applicable to the SED1633D1A and SED1633D1B.

Unit: µm

Pad No.	Pad Name	X Coord.	Y Coord.
1	COM5	2604	1834
2	COM6	2455	1834
3	COM7	2306	1834
4	COM8	2158	1834
5	COM9	2009	1834
6	COM10	1860	1834
7	COM11	1711	1834
8	COM12	1562	1834
9	COM13	1414	1834
10	COM14	1265	1834
11	COM15	1116	1834
12	COM16	967	1834
13	COM17	818	1834
14	COM18	670	1834
15	COM19	521	1834
16	COM20	372	1834
17	COM21	223	1834
18	COM22	74	1834
19	COM23	–74	1834
20	COM24	–223	1834
21	COM25	–372	1834
22	COM26	–521	1834
23	COM27	–670	1834
24	COM28	–818	1834
25	COM29	–967	1834
26	COM30	–1116	1834
27	COM31	–1265	1834
28	COM32	–1414	1834
29	COM33	–1562	1834
30	COM34	–1711	1834
31	COM35	–1860	1834
32	COM36	–2009	1834
33	COM37	–2158	1834
34	COM38	–2306	1834
35	COM39	–2455	1834
36	COM40	–2604	1834
37	COM41	–2842	1596
38	COM42	–2842	1428
39	COM43	–2842	1260
40	COM44	–2842	1092
41	COM45	–2842	924
42	COM46	–2842	756
43	COM47	–2842	588
44	COM48	–2842	420
45	COM49	–2842	252
46	COM50	–2842	84
47	COM51	–2842	–84
48	COM52	–2842	–252
49	COM53	–2842	–420
50	COM54	–2842	–588
51	COM55	–2842	–756
52	COM56	–2842	–924
53	COM57	–2842	–1092
54	COM58	–2842	–1260
55	COM59	–2842	–1428
56	COM60	–2842	–1596
57	COM61	–2604	–1834
58	COM62	–2455	–1834
59	COM63	–2306	–1834
60	COM64	–2158	–1834
61	COM65	–2009	–1834
62	COM66	–1860	–1834
63	COM67	–1711	–1834
64	COM68	–1562	–1834
65	COM69	–1414	–1834
66	COM70	–1265	–1834
67	COM71	–1116	–1834
68	COM72	–967	–1834
69	COM73	–818	–1834
70	COM74	–670	–1834
71	COM75	–521	–1834
72	COM76	–372	–1834
73	COM77	–223	–1834
74	COM78	–74	–1834
75	COM79	74	–1834
76	COM80	223	–1834
77	COM81	372	–1834
78	COM82	521	–1834
79	COM83	670	–1834
80	COM84	818	–1834
81	COM85	967	–1834
82	COM86	1116	–1834
83	COM87	1265	–1834
84	COM88	1414	–1834
85	COM89	1562	–1834
86	COM90	1711	–1834
87	COM91	1860	–1834
88	COM92	2009	–1834
89	COM93	2158	–1834
90	COM94	2306	–1834
91	COM95	2455	–1834
92	COM96	2604	–1834
93	COM97	2842	–1596
94	COM98	2842	–1428
95	COM99	2842	–1260
96	D0	2842	–1092
97	DI3	2842	–924
98	FR	2842	–756
99	YSCL	2842	–588
100	SEL	2842	–420
101	V_{DD}	2842	–252
102	V_{SS}	2842	–84
103	V0	2842	84
104	V1	2842	252
105	V4	2842	420
106	V5	2842	588
107	DI1	2842	756
108	COM0	2842	924
109	COM1	2842	1092
110	COM2	2842	1260
111	COM3	2842	1428
112	COM4	2842	1596

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SED1634

LOW-POWER 100-BIT LCD COMMON DRIVER

■ DESCRIPTION

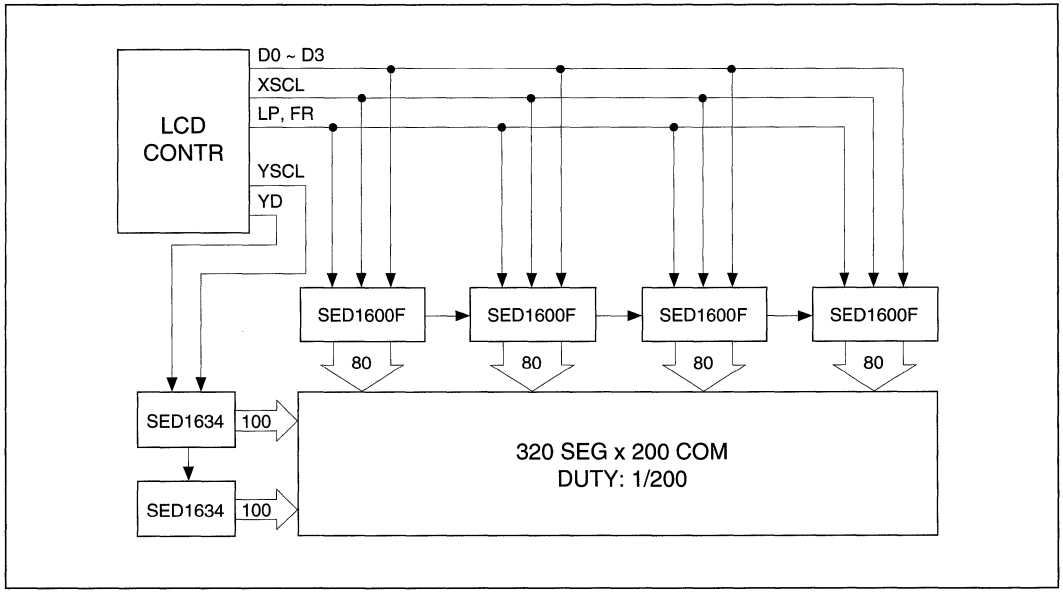
The SED1634 is a 100 (50 × 2) output dot matrix LCD common (row) driver for driving high-capacity LCD panels at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of the LCD driving voltages, and has its maximum drive voltage, VO, isolated from V_{DD} for flexibility of bias voltage generation.

The SED1634 is used in conjunction with the SED1648 (80-output segment driver) or the SED1600 (80-bit segment driver) to drive a large-capacity dot matrix LCD panel.

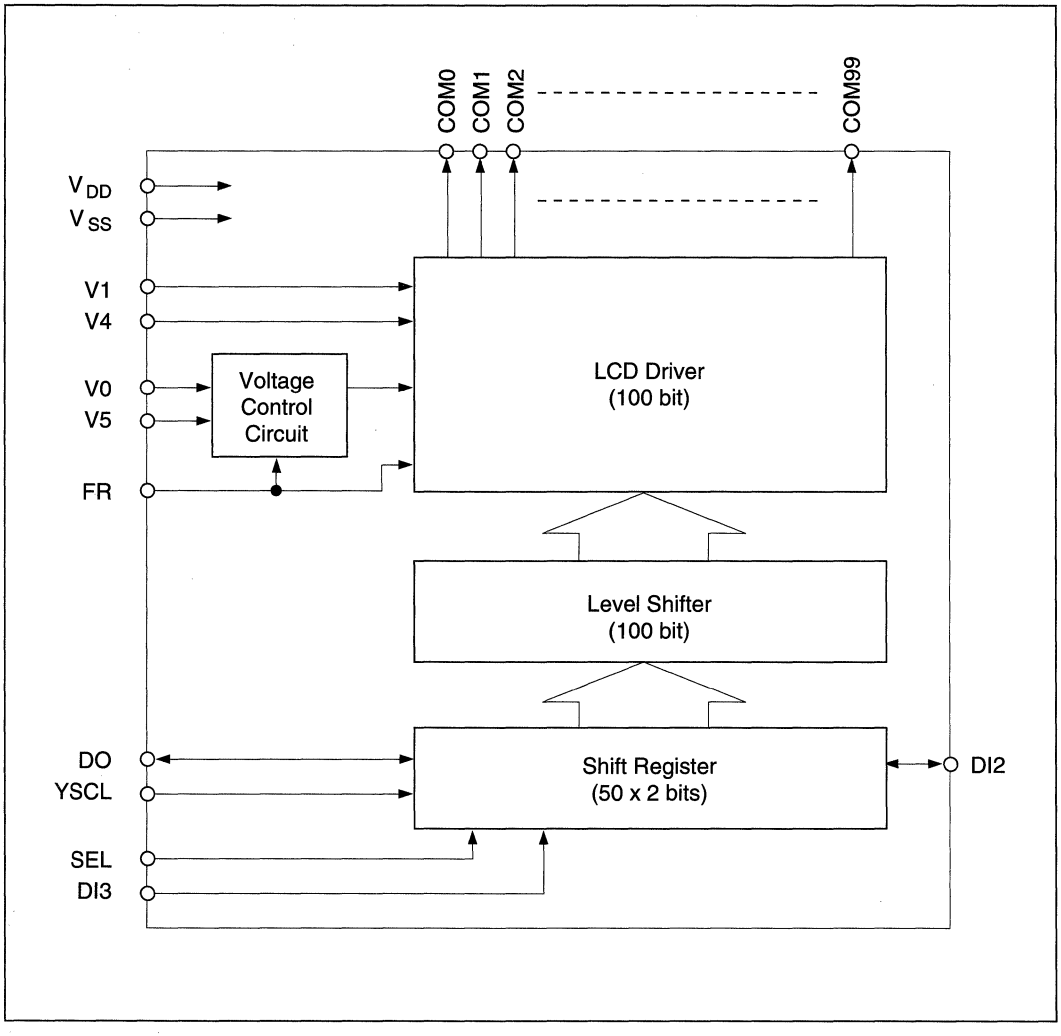
■ FEATURES

- Low-power CMOS technology
- 100-bit (50 × 2 structure) common (row) driver
- Duty cycle: ..... 1/64 to 1/300
- Low output impedance:
  500Ω typ (V1, V4 level)
  700Ω typ (V0, V5 level)
- Ability to adjust offset bias of the LCD relative to V_{DD}
- Non-biased display-off function
- Pin selection of the output shift direction
- LCD voltage: ..... –12 to –28V
- Supply voltage: ..... 2.7 to 5.5V
- Package: ..... Al pad (D_{1A})
  Au bump (D_{1B})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Shift Register

This is a bidirectional shift register for common data transmission.

● Shift Direction

SED1634	COM 99 → COM 0	
SED1633	COM 0 → COM 99	Reference

● Level Shifter

This is a level interface circuit for shifting the signal voltage from the logic system level to the LCD driver system level.

● LCD Drivers and Voltage Controller Circuit

Outputs the LCD driver voltage.

The relationships between the contents of the shift register, the alternating signal FR, and the common output voltage are as shown in the table below:

Contents of Shift Register	FR	COM Output Voltage	
H	H	V5	Select level
	L	V0	
L	H	V1	Non-select level
	L	V4	

■ PIN DESCRIPTION

Pin Name	I/O	Function	No. of Pins
COM0 – COM99	O	LCD driver common (row) output. Changes on the falling edge of the YSCL signal.	100
DI2, DI3	I	Serial data input for the 100 bit shift register. DI3 is the intermediate shift input. (When DI3 is unused, tie it to V_{DD} or V_{SS}.)	2
YSCL	I	Serial data shift clock input. Scanning data is shifted at the falling edge.	1
FR	I	LCD driver output AC signal input	1
V_{DD}, V_{SS}	Power	Power source for logic. V_{DD}: 0V (GND). V_{SS}: –5.0V	2
V0, V1, V4, V5	Power	Power source for LCD driver. V5: –12 to –28 V $V_{DD} \geq V0 \geq V1 > V4 \geq V5$	4
SEL	I	Shift Register Operating Configuration Selection: SEL: H → 50 × 2, Input; L → 100 × 1, H/L	1
DO	O	Shift register data output. The output changes with the falling edge of the YSCL signal.	1

Total: 112

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Power voltage (1)	Vss	–7.0 to +0.3	V
Power voltage (2)	V5	–30.0 to +0.3	V
Power voltage (3)	V0, V1, V4	V5 – 0.3 to + 0.3	V
Input voltage	VI	Vss – 0.3 to + 0.3	V
Output voltage	VO	Vss – 0.3 to + 0.3	V
Output current (1)	IO	20	mA
Output current (2)	IOCOM	20	mA
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–65 to +150	°C

Notes: *1. The voltages are all relative to V_{DD} = 0V.

*2. Ensure that the relationship between V0, V1, and V4 is always as follows: $V_{DD} \geq V0 \geq V1 \geq V4 \geq V5$.

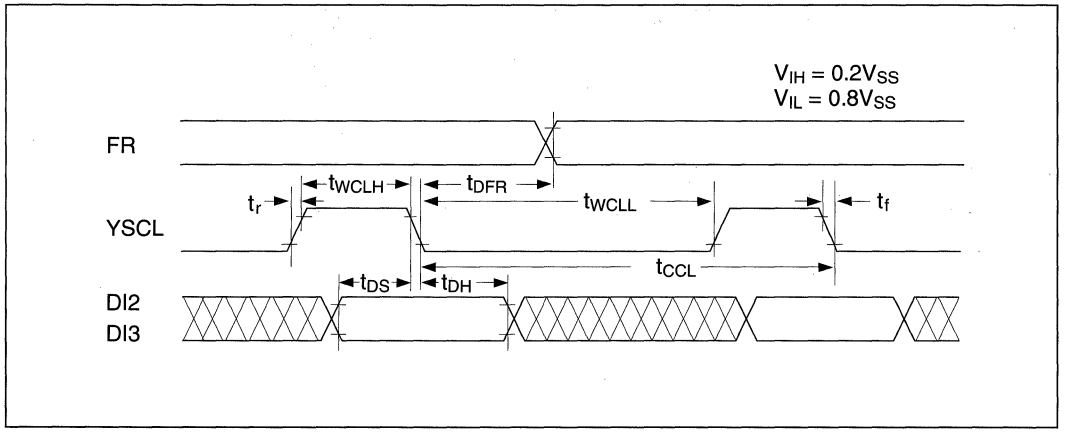
*3. The LSI may be permanently damaged if the logic system power is floating or Vss is greater than or equal to –2.6V when power is applied to the LC drive circuit system. Special caution must be paid to the power sequences when turning the power on and off.

● DC Electrical Characteristics

Unless otherwise noted, V_{DD} = V0 = 0V, V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Applicable Pins	Min	Typ	Max	Unit
Power voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V5		V5	–28.0	—	–12.0	V
Possible operating voltage	V5	Function	V5	—	—	–8.0	V
Power voltage (2)	V0	Recommended value	V0	–2.5	—	0	V
Power voltage (3) Power voltage (4)	V1 V4	Recommended value Recommended value	V1 V4	2/9 × V5 V5	—	V_{DD} 7/9 × V5	V
High-level input voltage	V_{IH}	V_{SS} = –2.7 to –5.5V	DI2, YSCL, SEL, DI3, FR	0.2 × V_{SS}	—	—	V
Low-level input voltage	V_{IL}			—	—	0.8 × V_{SS}	V
High-level output voltage	V_{OH}	I_{OH} = –0.3mA I_{OH} = –0.2mA (V_{SS} = –2.7 to –4.5V)	DO	–0.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 0.3mA I_{OL} = 0.2mA (V_{SS} = –2.7 to –4.5V)		—	—	V_{SS} + 0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	YSCL, SEL, DI3, FR	—	—	2.0	µA
I/O leakage current	I_{LO}	$V_{SS} \le V_{IN} \le 0V$	DI2, DO	—	—	5.0	µA
Static current	I_{DDS}	V5 = –12.0 to –28.0V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{COM}	$\Delta\lvert V_{ON}\rvert$ = 0.5V, V5 = –20.0V V5 = –14.0V *(V5 = –8.0V)	When outputting the V1, V4 levels; COM0 ~ COM99	—	0.40 0.50 (0.60)	0.80 1.00 (1.20)	KΩ
		V5 = –20.0V V5 = –14.0V *(V5 = –8.0V)	When outputting the V0, V5 levels; *Reference value	—	0.60 0.70 (0.90)	1.20 1.40 (1.80)	
Average operating consumption current (1)	I_{SS1}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 12KHz, Frame frequency = 60KHz, Input data: 1/200, "H" is without load on each duty cycle	V_{SS}	—	7	15	µA
		V_{SS} = –3.0V; other parameters are identical		—	5	10	
Average operating consumption current (2)	I_{SS2}	V_{SS} = –5.0V, V1 = –2.0V, V4 = –18.0V, V5 = –20.0V; other parameters are the same as for I_{SS1}	V5	—	7	15	µA
Input terminal capacitance	C_I	T_a = 25°C	YSCL, SEL, DI3, FR	—	—	8	pF
I/O terminal capacitance	$C_{I/O}$		DI2, DO	—	—	15	pF

- **AC Characteristics**
  - **Input Timing Characteristics**



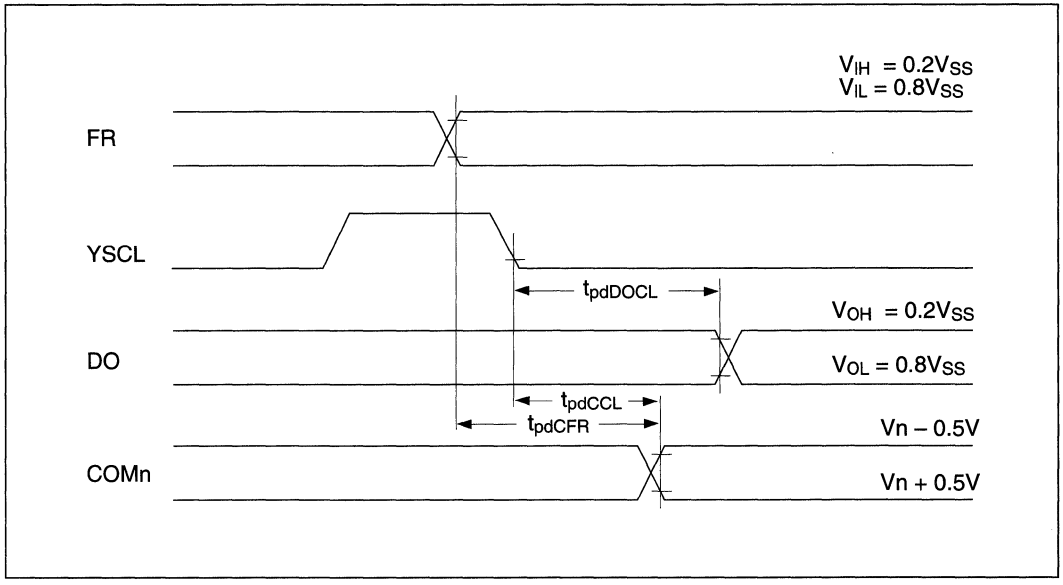
Unless otherwise noted, V_{SS} = –5.0 ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	t_r		—	50	ns
Input signal fall time	t_f		—	50	ns
YSCL frequency	t_{CCL}		500	—	ns
YSCL high-level pulse width	t_{WCLH}		70	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		100	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		–500	500	ns

Unless otherwise noted, V_{SS} = –2.7 to –4.5V, Ta = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	t_r		—	50	ns
Input signal fall time	t_f		—	50	ns
YSCL frequency	t_{CCL}		1000	—	ns
YSCL high-level pulse width	t_{WCLH}		160	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		200	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		–500	500	ns

○ Output Timing Characteristics



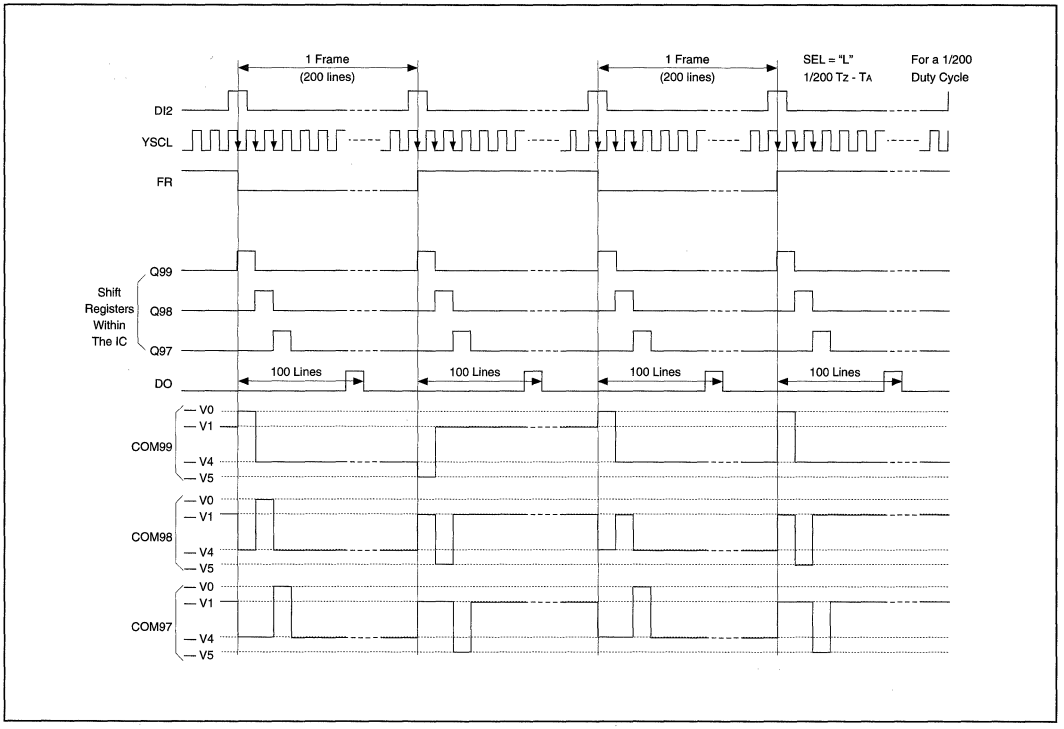
Unless otherwise noted, V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → D0) delay time	t_{pdDOCL}	CL = 15pF	30	300	ns
(YSCL fall → COM output) delay time	t_{pdCCL}	V5 = –12.0 to –28.0V CL = 100pF	—	3.0	µs
(FR → COM output) delay time	t_{pdCFR}		—	3.0	µs

Unless otherwise noted, V_{SS} = –2.7 to –4.5V, T_a = –40 to 85°C

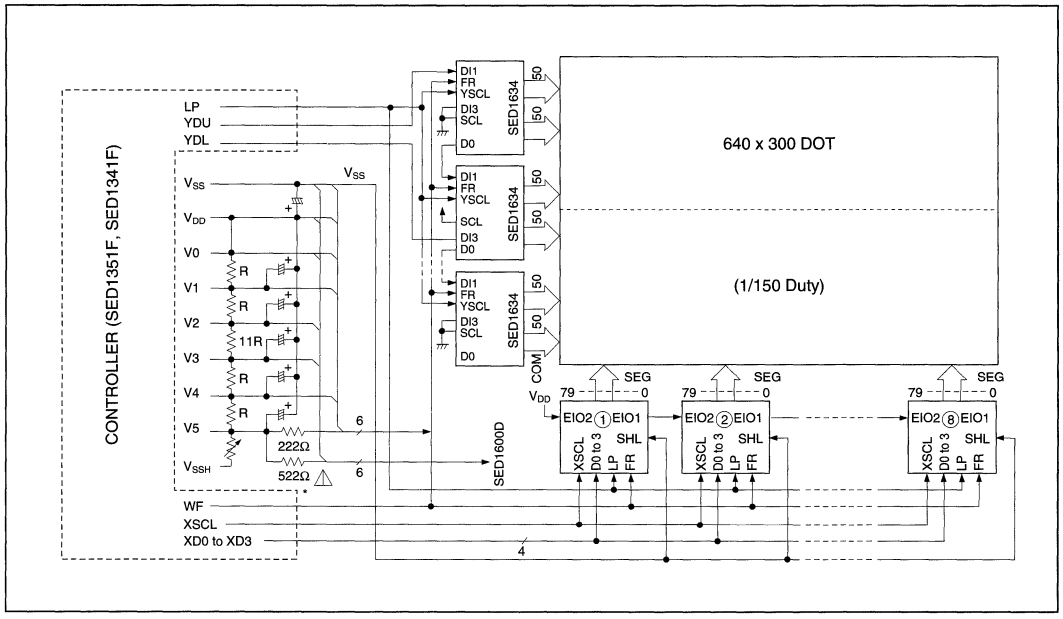
Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → D0) delay time	t_{pdDOCL}	CL = 15pF	60	600	ns
(YSCL fall → COM output) delay time	t_{pdCCL}	V5 = –12.0 to –28.0V CL = 100pF	—	3.0	µs
(FR → COM output) delay time	t_{pdCFR}		—	3.0	µs

● Timing Diagram



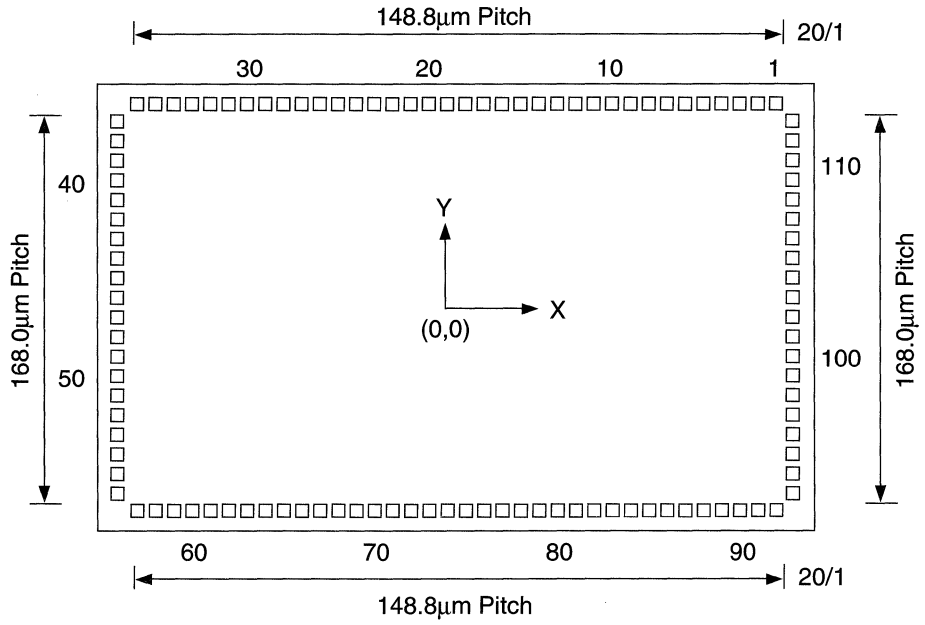
■ EXAMPLE OF CONNECTION

● Connections for a 640 × 300 dot matrix LCD



Note: *1. A guard resistance must be used to prevent excessive current. A bypass capacitor (0.01μF) should be used near the VSS and V5 pins of each LSI to prevent noise.

■ PAD LAYOUT



SED1634D1A Specifications (The Al Pad Model)

Chip size ..... 6.03 mm × 4.01 mm
Chip thickness ..... 0.400 mm
Pad opening ..... 101 mm (X) × 110 mm (Y)
(where the Y direction is the direction of the chip center line)

SED1634D1B Specifications (The Au Bump Model)

Chip size ..... 6.03 mm × 4.01 mm
Chip thickness ..... 0.525 mm
Bump size ..... 117 µm × 105 µm
+10 µm
Bump height: ..... 20 µm
(reference values) −5 µm

■ PAD COORDINATES

Applicable to the SED1634D1A and SED1634D1B.

Units: µm

Pad No.	Pin Name	X Coord.	Y Coord.
1	COM5	2604	1834
2	COM6	2455	1834
3	COM7	2306	1834
4	COM8	2158	1834
5	COM9	2009	1834
6	COM10	1860	1834
7	COM11	1711	1834
8	COM12	1562	1834
9	COM13	1414	1834
10	COM14	1265	1834
11	COM15	1116	1834
12	COM16	967	1834
13	COM17	818	1834
14	COM18	670	1834
15	COM19	521	1834
16	COM20	372	1834
17	COM21	223	1834
18	COM22	74	1834
19	COM23	–74	1834
20	COM24	–223	1834
21	COM25	–372	1834
22	COM26	–521	1834
23	COM27	–670	1834
24	COM28	–818	1834
25	COM29	–967	1834
26	COM30	–1116	1834
27	COM31	–1265	1834
28	COM32	–1414	1834
29	COM33	–1562	1834
30	COM34	–1711	1834
31	COM35	–1860	1834
32	COM36	–2009	1834
33	COM37	–2158	1834
34	COM38	–2306	1834
35	COM39	–2455	1834
36	COM40	–2604	1834
37	COM41	–2842	1596
38	COM42	–2842	1428
39	COM43	–2842	1260
40	COM44	–2842	1092
41	COM45	–2842	924
42	COM46	–2842	756
43	COM47	–2842	588
44	COM48	–2842	420
45	COM49	–2842	252
46	COM50	–2842	84
47	COM51	–2842	–84
48	COM52	–2842	–252
49	COM53	–2842	–420
50	COM54	–2842	–588
51	COM55	–2842	–756
52	COM56	–2842	–924
53	COM57	–2842	–1092
54	COM58	–2842	–1260
55	COM59	–2842	–1428
56	COM60	–2842	–1596
57	COM61	–2604	–1834
58	COM62	–2455	–1834
59	COM63	–2306	–1834
60	COM64	–2158	–1834
61	COM65	–2009	–1834
62	COM66	–1860	–1834
63	COM67	–1711	–1834
64	COM68	–1562	–1834
65	COM69	–1414	–1834
66	COM70	–1265	–1834
67	COM71	–1116	–1834
68	COM72	–967	–1834
69	COM73	–818	–1834
70	COM74	–670	–1834
71	COM75	–521	–1834
72	COM76	–372	–1834
73	COM77	–223	–1834
74	COM78	–74	–1834
75	COM79	74	–1834
76	COM80	223	–1834
77	COM81	372	–1834
78	COM82	521	–1834
79	COM83	670	–1834
80	COM84	818	–1834
81	COM85	967	–1834
82	COM86	1116	–1834
83	COM87	1265	–1834
84	COM88	1414	–1834
85	COM89	1562	–1834
86	COM90	1711	–1834
87	COM91	1860	–1834
88	COM92	2009	–1834
89	COM93	2158	–1834
90	COM94	2306	–1834
91	COM95	2455	–1834
92	COM96	2604	–1834
93	COM97	2842	–1596
94	COM98	2842	–1428
95	COM99	2842	–1260
96	DI2	2842	–1092
97	DI3	2842	–924
98	FR	2842	–756
99	YSCL	2842	–588
100	SEL	2842	–420
101	V_{DD}	2842	–252
102	V_{SS}	2842	–84
103	V0	2842	84
104	V1	2842	252
105	V4	2842	420
106	V5	2842	588
107	DI0	2842	756
108	COM0	2842	924
109	COM1	2842	1092
110	COM2	2842	1260
111	COM3	2842	1428
112	COM4	2842	1596

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SED1635

LCD COMMON DRIVER

■ DESCRIPTION

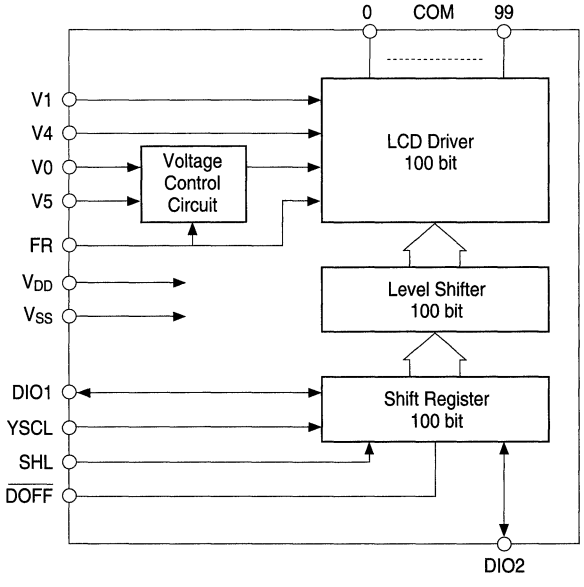
The SED1635 is a dot matrix LCD common (row) driver for use with high-capacity, high duty cycle LCD panels. The SED1635 has 100 common driver outputs and can operate at a duty cycle of up to 1/300. The driver is used with the SED1640D. The driver is designed to work over a wide range of LCD drive voltages and has its maximum drive voltage, V0, isolated from V_{DD} for flexibility of bias voltage generation.

The driver's pad layout is designed for easy mounting on boards and the bi-direction of driver output order can be selected. The driver has 100 LCD outputs with high resistance voltage and low output impedance. As a result, the driver achieves the maximum driver usage for the 1/200 duty panel.

■ FEATURES

- 100 common drive outputs
- Output resistance:
  500Ω typical, at V1 and V4 levels
  700Ω typical, at V0 and V5 levels
- Duty ratio from 1/64 to 1/300
- Maximum configuration: 640 × 480 pixels when used with the SED1640D
- Selectable shift direction
- Adjustable offset bias of LCD power for V_{DD} level
- Wide range of LCD drive voltages: 12 ~ 28V (absolute maximum rated voltage is 30V)
- Logic power supply: –2.7V to –5.5V
- CMOS Si-Gate process
- Package chip
  SED1635D_{1A}: Al pad
  SED1635D_{1B}: Gold bump

■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Shift Register

The shift register shifts common data bi-directionally through the driver.

● Level Shifter

This is the level interface circuit that converts a signal voltage level from the logic level to the LCD driver level.

● LCD Driver and Voltage Control Circuit

The LCD driver voltage is output.

The relationship among the blanking control signal ($\overline{DOFF}$), shift register contents, the LCD AC-drive waveform (FR) and the common output level are given in the table below.

$\overline{DOFF}$	Shift Register Data	FR	COM Output Level	
H	H	H	V5	(Selected level)
		L	V0	
	L	H	V1	(Not selected level)
		L	V4	
L	Fixed to L	—	V0	

■ PIN DESCRIPTION

Pin Name	I/O	Functions	No. of pins
COM0 to COM99	O	LCD drive common low. Changes with YSCL falling edge.	100
DIO1, DIO2	I/O	Serial data I/O of 100-bit bidirectional shift register. Serial data input/output pin. Configured by SHL. Output changes with YSCL falling edge.	2
YSCL	I	Serial data shift clock input. Data is shifted into the driver on the falling edge of this signal.	1
SHL	I	Shift direction and input/output selection input. SHL: L → COM data shift direction: 0 → 99, DIO1: Input, DIO2: Output SHL: H → COM data shift direction: 99 → 0, DIO1: Output, DIO2: Input	1
$\overline{DOFF}$	I	Active low blanking control input. The shift register contents are cleared by low-level input, and all common output instantly changes to the V0 level.	1
FR	I	LCD AC drive signal input.	1
V_{DD}, V_{SS}	Power supply	Logic power input. V_{DD}: 0V (GND) V_{SS}: –5.0V	2
V0, V1, V4, V5	Power supply	LCD drive power input. V5: –12V ~ –28V $V_{DD} \geq V- \geq V1 \geq V4 \geq V5$	4

Total 112

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Supply voltage 1	V_{SS}	–7.0 to +0.3	V
Supply voltage 2	V5	–30.0 to +0.3	V
Supply voltage 3	V0, V1, V4	V5 – 3.0 to +0.3	V
Input voltage	V_I	V_{SS} – 0.3 to +0.3	V
Output voltage	V_O	V_{SS} – 0.3 to +0.3	V
Output current 1	V0	20	mA
Output current 2	I_{OCOM}	20	mA
Power dissipation	PD	300	mW
Operating temperature	T_{OPR}	–40 to +85	°C
Storage temperature	T_{STG}	–65 to +150	°C

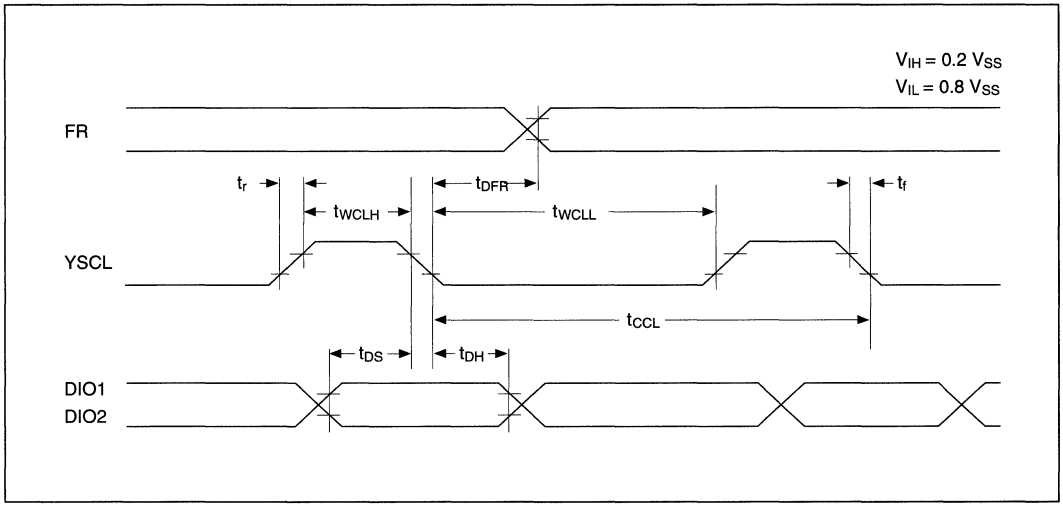
1. All voltages are given relative to V_{DD} = 0V.
2. V0, V1, and V4 must satisfy the condition $V_{DD} \geq V0 \geq V1 \geq V4 \geq 5$
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Function operation under these conditions is not implied.

● DC Electrical Characteristics

Unless otherwise stated, V_{DD} = V0 = 0V, V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Pin	Min	Typ	Max	Unit
Supply voltage 1	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V5	V_{SS} = –2.7 to –5.5V	V5	–28.0	—	–12.0	V
Minimum operating voltage	V5		V5	—	—	–8.0	V
Supply voltage 2	V0	Recommended value	V0	–2.5	—	0	V
Supply voltage 3	V1	Recommended value	V1	2/9 × V5	—	V_{DD}	V
Supply voltage 4	V4	Recommended value	V4	V5	—	7/9 × V5	V
High-level output voltage	V_{IH}	V_{SS} = –2.7 to –5.5V	DIO1, DIO2, YSCL, SHL, $\overline{DOFF}$, FR	0.2 × V_{SS}	—	—	V
Low-level output voltage	V_{IL}			—	—	0.8 × V_{SS}	V
High-level output voltage	V_{OH}	I_{OH} = –0.3 mA I_{OH} = –0.2 mA (V_{SS} = –2.7 to –4.5V)	DIO1, DIO2	–0.4	—	—	V
Low-level output voltage	V_{OH}	I_{OL} = –0.3 mA I_{OL} = –0.2 mA (V_{SS} = –2.7 to –4.5V)		—	—	V_{SS} + 0.4	V
Input, I/O leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	YSCL, SHL, $\overline{DOFF}$, FR	—	—	2.0	µA
	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$	DIO1, DIO2	—	—	5.0	µA
Static current	I_{DDS}	V5 = –12.0 to –28.0 V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{COM}	#VON = 0.5V, V5 = –20.0V	V1, V4 Output Level, COM0 to COM99	—	0.40	0.80	KΩ
		#VON = 0.5V, V5 = –14.0V		—	0.50	1.00	
		#VON = 0.5V, (V5 = –8.0V)		—	(0.60)	(1.20)	
		#VON = 0.5V, V5 = –20.0V	V0, V5 Output Level, COM0 to COM99	—	0.60	1.20	
		#VON = 0.5V, V5 = –14.0V		—	0.70	1.40	
		#VON = 0.5V, (V5 = –8.0V)		—	(0.90)	(1.80)	
Current consumption (1)	I_{SS1}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 12 kHz, Frame frequency = 60 Hz, Input data: "H" every 1/200 no-load	V_{SS}	—	7	15	µA
		V_{SS} = –3.0V		—	5	10	
Current consumption (2)	I_{SS2}	V_{SS} = –5V, V1 = –2V, V4 = –18V, V5 = –20V, other conditions are same as I_{SS1}	V5	—	7	15	µA
Input capacitance	C_I	T_a = 25°C	YSCL, SHL, $\overline{DOFF}$, FR	—	—	8	pF
	$C_{I/O}$		DIO1, DIO2	—	—	15	pF

- **AC Electrical Characteristics**
  - **Input Timing**



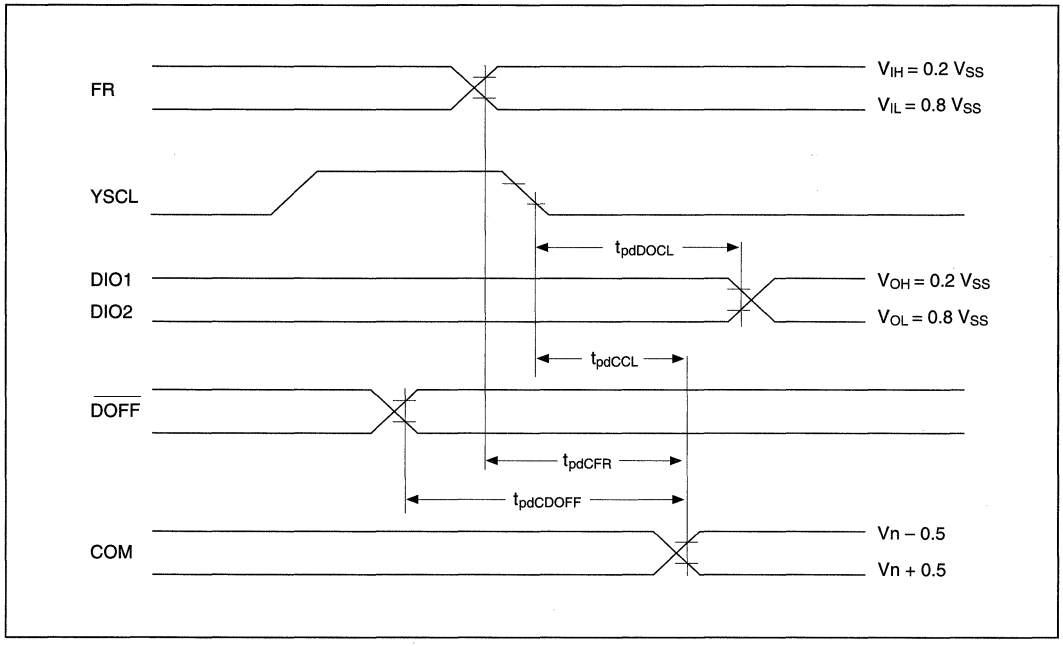
V_{SS} = –5.0 ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns
YSCL period	t_{CCL}		500	—	—	ns
YSCL "H" pulse width	t_{WCLH}		70	—	—	ns
YSCL "L" pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns

V_{SS} = –2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns
YSCL period	t_{CCL}		1000	—	—	ns
YSCL "H" pulse width	t_{WCLH}		160	—	—	ns
YSCL "L" pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		200	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns

○ Output Timing



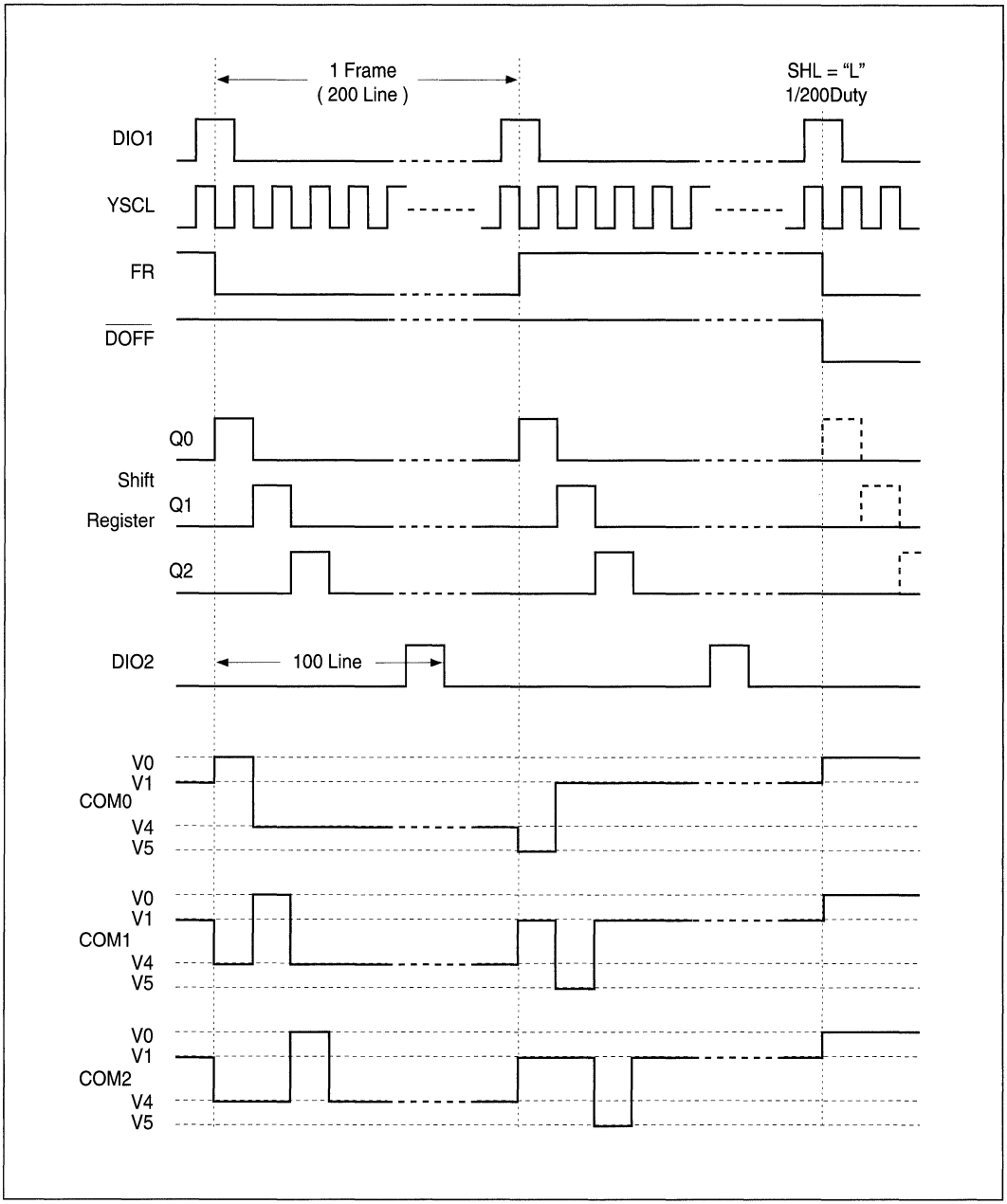
V_{SS} = –5.0 ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL fall edge to DIO delay	t_{pdDOCL}	CL = 15pF	30	—	300	ns
YSCL fall edge to COM delay	t_{pdCCL}	V5 = –12.0 to –28.0V CL = 100pF	—	—	3.0	µs
$\overline{DOFF}$ to COM delay	$t_{pdCDOFF}$					
FR to COM delay	t_{pdCFR}		—	—	3.0	µs

V_{SS} = –2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL fall edge to DIO delay	t_{pdDOCL}	CL = 15pF	60	—	400	ns
YSCL fall edge to COM delay	t_{pdCCL}	V5 = –12.0 to –28.0V CL = 100pF	—	—	3.0	µs
$\overline{DOFF}$ to COM delay	$t_{pdCDOFF}$					
FR to COM delay	t_{pdCFR}		—	—	3.0	µs

● **Timing Chart**



■ LCD DRIVER POWER SUPPLY

● Generating LCD Drive Voltages

The easiest way to generate LCD drive voltage is by the split resistors. To obtain a high quality display, it is mandatory that voltage levels be precise and stable. Set the split resistor values as low as the system's power capacity allows. In particular, when low power is required, set the split resistors high and, instead, drive each level with the voltage follower using the operation amplifier. To use an operation amplifier, V0 and V_{DD} are separated in this device. (V0 is the maximum potential level for the LCD driver.) However, if the V0 potential falls below the V_{DD} potential and, as a result, the potential difference is large, the LCD driver capability decreases. To avoid this, set the V_{DD} and V0 within 0V to 2.5V. If an operation amplifier is not used, connect the V0 and V_{DD}.

● System Power-Up

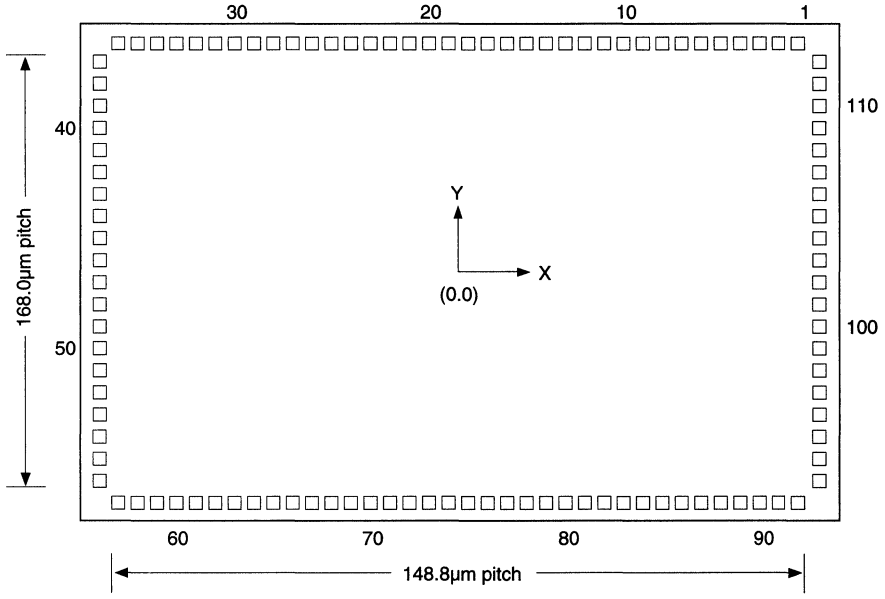
This LSI has high LCD drive voltage. As a result, if the logic power is being floated and high voltage is applied in the LCD driver, the LSI may be damaged because of the excess current.

Follow the sequence given below when turning power on or off.

To turn on the power – Turn on the logic power → Turn the LCD driver on
(or turn them on simultaneously)

To turn off the power – Turn off the LCD driver → Turn off the logic power
(or turn them off simultaneously)

■ PAD DIMENSIONS



(1) Aluminum pad chip specification

Chip size ..... 6.03 × 4.01 × 0.400 mm
Hole in pad ..... 108 × 110 µm

(2) Gold bumped chip specification (reference)

Chip size ..... 6.03 × 4.01 × 0.525 mm
Bumping size ..... 117 × 105 µm (±20 µm)
Bumping height ..... 20 $^{+10}_{-5}$ µm

■ PAD COORDINATES

● SED1635D0A PAD COORDINATES

Unit: μm

Pad No.	Pin Name	X	Y
1	COM5	2604	1839
2	COM6	2455	1839
3	COM7	2306	1839
4	COM8	2158	1839
5	COM9	2009	1839
6	COM10	1860	1839
7	COM11	1711	1839
8	COM12	1562	1839
9	COM13	1414	1839
10	COM14	1265	1839
11	COM15	1116	1839
12	COM16	967	1839
13	COM17	818	1839
14	COM18	670	1839
15	COM19	521	1839
16	COM20	372	1839
17	COM21	223	1839
18	COM22	74	1839
19	COM23	–74	1839
20	COM24	–223	1839
21	COM25	–372	1839
22	COM26	–521	1839
23	COM27	–670	1839
24	COM28	–818	1839
25	COM29	–967	1839
26	COM30	–1116	1839
27	COM31	–1265	1839
28	COM32	–1414	1839
29	COM33	–1562	1839
30	COM34	–1711	1839
31	COM35	–1860	1839
32	COM36	–2009	1839
33	COM37	–2158	1839
34	COM38	–2306	1839
35	COM39	–2455	1839
36	COM40	–2604	1839
37	COM41	–2847	1596
38	COM42	–2847	1428
39	COM43	–2847	1260
40	COM44	–2847	1092
41	COM45	–2847	924
42	COM46	–2847	756
43	COM47	–2847	588
44	COM48	–2847	420
45	COM49	–2847	252
46	COM50	–2847	84
47	COM51	–2847	–84
48	COM52	–2847	–252
49	COM53	–2847	–420
50	COM54	–2847	–588
51	COM55	–2847	–756
52	COM56	–2847	–924
53	COM57	–2847	–1092
54	COM58	–2847	–1260
55	COM59	–2847	–1428
56	COM60	–2847	–1596
57	COM61	–2604	–1839
58	COM62	–2455	–1839
59	COM63	–2306	–1839
60	COM64	–2158	–1839
61	COM65	–2009	–1839
62	COM66	–1860	–1839
63	COM67	–1711	–1839
64	COM68	–1562	–1839
65	COM69	–1414	–1839
66	COM70	–1265	–1839
67	COM71	–1116	–1839
68	COM72	–967	–1839
69	COM73	–818	–1839
70	COM74	–670	–1839
71	COM75	–521	–1839
72	COM76	–372	–1839
73	COM77	–223	–1839
74	COM78	–74	–1839
75	COM79	74	–1839
76	COM80	223	–1839
77	COM81	372	–1839
78	COM82	521	–1839
79	COM83	670	–1839
80	COM84	818	–1839
81	COM85	967	–1839
82	COM86	1116	–1839
83	COM87	1265	–1839
84	COM88	1414	–1839
85	COM89	1562	–1839
86	COM90	1711	–1839
87	COM91	1860	–1839
88	COM92	2009	–1839
89	COM93	2158	–1839
90	COM94	2306	–1839
91	COM95	2455	–1839
92	COM96	2604	–1839
93	COM97	2847	–1596
94	COM98	2847	–1428
95	COM99	2847	–1260
96	DIO2	2847	–1092
97	$\overline{\text{DOFF}}$	2847	–924
98	FR	2847	–756
99	YSCL	2847	–588
100	SHL	2847	–420
101	V_{DD}	2847	–252
102	V_{SS}	2847	–84
103	V0	2847	84
104	V1	2847	252
105	V4	2847	420
106	V5	2847	588
107	DIO1	2847	756
108	COM0	2847	924
109	COM1	2847	1092
110	COM2	2847	1260
111	COM3	2847	1428
112	COM4	2847	1596

● SED1635D0B PAD COORDINATES

Unit: μm

Pad No.	Pin Name	X	Y
1	COM5	2604	1834
2	COM6	2455	1834
3	COM7	2306	1834
4	COM8	2158	1834
5	COM9	2009	1834
6	COM10	1860	1834
7	COM11	1711	1834
8	COM12	1562	1834
9	COM13	1414	1834
10	COM14	1265	1834
11	COM15	1116	1834
12	COM16	967	1834
13	COM17	818	1834
14	COM18	670	1834
15	COM19	521	1834
16	COM20	372	1834
17	COM21	223	1834
18	COM22	74	1834
19	COM23	–74	1834
20	COM24	–223	1834
21	COM25	–372	1834
22	COM26	–521	1834
23	COM27	–670	1834
24	COM28	–818	1834
25	COM29	–967	1834
26	COM30	–1116	1834
27	COM31	–1265	1834
28	COM32	–1414	1834
29	COM33	–1562	1834
30	COM34	–1711	1834
31	COM35	–1860	1834
32	COM36	–2009	1834
33	COM37	–2158	1834
34	COM38	–2306	1834
35	COM39	–2455	1834
36	COM40	–2604	1834
37	COM41	–2847	1596
38	COM42	–2847	1428
39	COM43	–2847	1260
40	COM44	–2847	1092
41	COM45	–2847	924
42	COM46	–2847	756
43	COM47	–2847	588
44	COM48	–2847	420
45	COM49	–2847	252
46	COM50	–2847	84
47	COM51	–2847	–84
48	COM52	–2847	–252
49	COM53	–2847	–420
50	COM54	–2847	–588
51	COM55	–2847	–756
52	COM56	–2847	–924
53	COM57	–2847	–1092
54	COM58	–2847	–1260
55	COM59	–2847	–1428
56	COM60	–2847	–1596
57	COM61	–2604	–1834
58	COM62	–2455	–1834
59	COM63	–2306	–1834
60	COM64	–2158	–1834
61	COM65	–2009	–1834
62	COM66	–1860	–1834
63	COM67	–1711	–1834
64	COM68	–1562	–1834
65	COM69	–1414	–1834
66	COM70	–1265	–1834
67	COM71	–1116	–1834
68	COM72	–967	–1834
69	COM73	–818	–1834
70	COM74	–670	–1834
71	COM75	–521	–1834
72	COM76	–372	–1834
73	COM77	–223	–1834
74	COM78	–74	–1834
75	COM79	74	–1834
76	COM80	223	–1834
77	COM81	372	–1834
78	COM82	521	–1834
79	COM83	670	–1834
80	COM84	818	–1834
81	COM85	967	–1834
82	COM86	1116	–1834
83	COM87	1265	–1834
84	COM88	1414	–1834
85	COM89	1562	–1834
86	COM90	1711	–1834
87	COM91	1860	–1834
88	COM92	2009	–1834
89	COM93	2158	–1834
90	COM94	2306	–1834
91	COM95	2455	–1834
92	COM96	2604	–1834
93	COM97	2842	–1596
94	COM98	2842	–1428
95	COM99	2842	–1260
96	DIO2	2842	–1092
97	$\overline{\text{DOFF}}$	2842	–924
98	FR	2842	–756
99	YSCL	2842	–588
100	SHL	2842	–420
101	V_{DD}	2842	–252
102	V_{SS}	2842	–84
103	V0	2842	84
104	V1	2842	252
105	V4	2842	420
106	V5	2842	588
107	DIO1	2842	756
108	COM0	2842	924
109	COM1	2842	1092
110	COM2	2842	1260
111	COM3	2842	1428
112	COM4	2842	1596

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LOW-POWER 100-BIT LCD COMMON DRIVER

■ DESCRIPTION

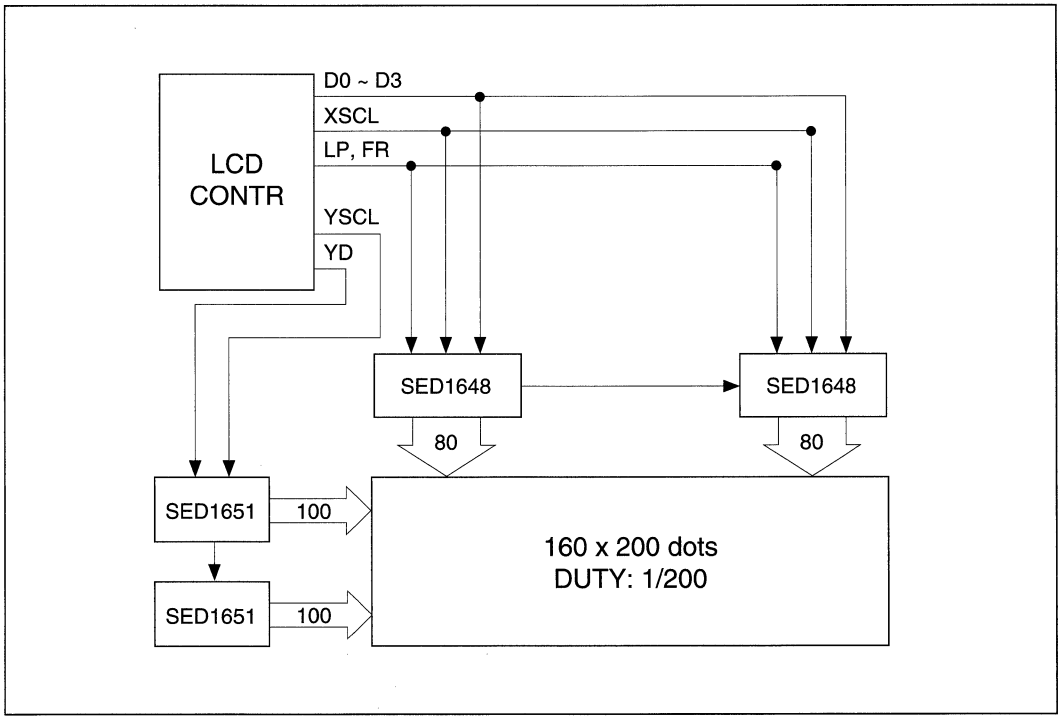
The SED1651 is a 100-output dot matrix LCD common (row) driver for driving high-capacity LCD panels at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of the LCD driving voltages, and has its maximum drive voltage, VO, isolated from V_{DD} for the flexibility of bias voltage generation.

The SED1651 is used in conjunction with the SED1648 (80-output segment driver) or the SED1640 (80-bit segment driver) to drive a large-capacity dot matrix LCD panel.

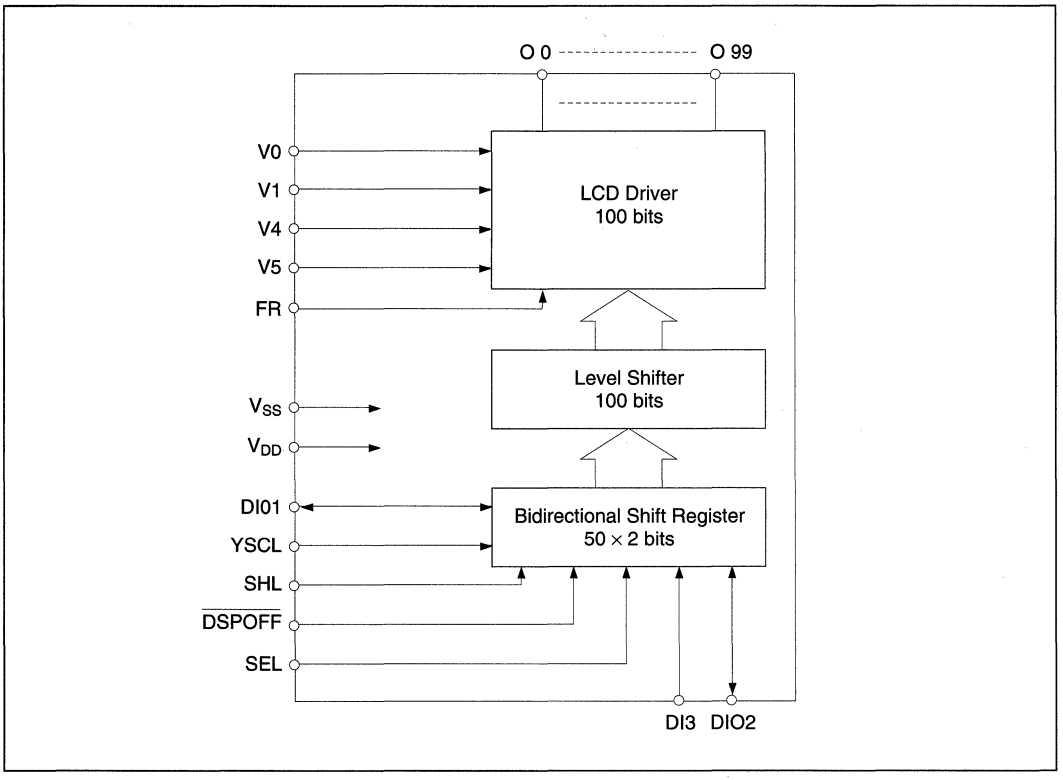
■ FEATURES

- Low-power CMOS technology
- 100-bit common (row) driver
- Low output impedance ..... 750Ω (typ)
- Duty cycle ..... 1/64 to 1/300
- Ability to adjust offset bias of the LCD relative to V_{DD}
- Non-biased display off function
- Pin selection of the output shift direction
- LCD voltage ..... –8 to –28V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... Slim Al pad DIE (DOA)

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Enable Shift Register

This is a bidirectional shift register used for transmitting common data. The shift register has a 50 × 2 bit structure, and is selectable to 50 × 2 bits or 100 bits depending on the setting of SEL.

When the 50 × 2 bit configuration is selected, the input for the second 50 bit shift register is DI3.

● Level Shifter

The level shifter is a level interface circuit which converts the signal voltage level from a logic circuit level to the LC driver voltage level.

● LCD Driver

The LCD driver outputs the LC drive voltage.

The relationship between the display blanking signal $\overline{\text{DSPOFF}}$, the contents of the shift register, the AC signal FR, and the On output voltage is as follows:

$\overline{\text{DSPOFF}}$	Contents of Shift Register	FR	O Output Voltage	
H	H	H	V5	(Select level)
		L	V0	
	L	H	V1	(Non-select level)
		L	V4	
L	—	—	V0	—

■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>O0 to O99</td><td>O</td><td>Common (row) output to drive LC.
Output transition occurs on falling edge of YSCL.</td><td>100</td></tr>
<tr><td>DIO1
DIO2</td><td>I/O</td><td>50 × 2 bit bi-directional shift register serial data I/O.
This is set to input or output depending on the level of the SHL input.
Output transition occurs on falling edge of YSCL.</td><td>2</td></tr>
<tr><td>DI3</td><td>I</td><td>Scan pulse input terminal of the 50 × 2 structure.
When SEL = L, DI3 = VSS or GND.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Bi-directional shift register operating mode select input
H: 50 × 2 (DI3 input) L: 100</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input (shifts scan data on falling edge).</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and DIO terminal I/O control input.
<table>
<tr><th rowspan="2">SHL</th><th colspan="5" rowspan="2">O Output Shift Direction</th><th colspan="2">DIO</th></tr>
<tr><th>1</th><th>2</th></tr>
<tr><td>L</td><td>0</td><td>→</td><td>49</td><td>50</td><td>→</td><td>99</td><td>I</td><td>O</td></tr>
<tr><td>H</td><td>99</td><td>→</td><td>50</td><td>49</td><td>→</td><td>0</td><td>O</td><td>I</td></tr>
</table>
When SEL = “H”, the DI3 input is input to O50 (SHL = “L”) or O49 (SHL = “H”).
When SEL = “L”, the DI3 input is ignored and the DIO input is continuously shifted.</td><td>1</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>LC display blanking control input. A low level clears the shift register, immediately causing all common outputs to go to V0.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC drive output AC signal input.</td><td>1</td></tr>
<tr><td>VDD, VSS</td><td>Power</td><td>Power source for logic:
VDD: 0V (GND)
VSS: –2.7 to –5.5V</td><td>3</td></tr>
<tr><td>V0, V1,
V4, V5</td><td>Power</td><td>LC Drive Circuit Power:
V5: –8 to –28V
VDD ≥V0 ≥ V1 > V4 ≥ V5</td><td>8</td></tr>
</table>

Total 119

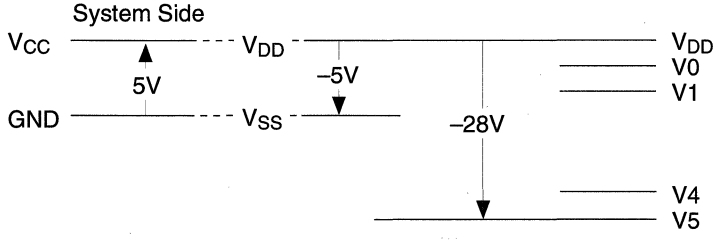
■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	V5	–30.0 to +0.3	V
Power voltage (3)	V0, V1, V4	V5 – 0.3 to + 0.3	V
Input voltage	VI	V_{SS} – 0.3 to + 0.3	V
Output voltage	VO	V_{SS} – 0.3 to + 0.3	V
Output current (1)	IO	20	mA
Output current (2)	IOCOM	20	mA
Operating temperature	Topr	–40 to +85	°C
Storage temperature (1)	Tstg1	–65 to +150	°C

Notes: *1. The voltages are all relative to V_{DD} = 0V.

*2. Ensure that the relationship between V0, V1, V4, and V5 is always as follows: $V_{DD} \geq V0 \geq V1 \geq V4 \geq V5$.



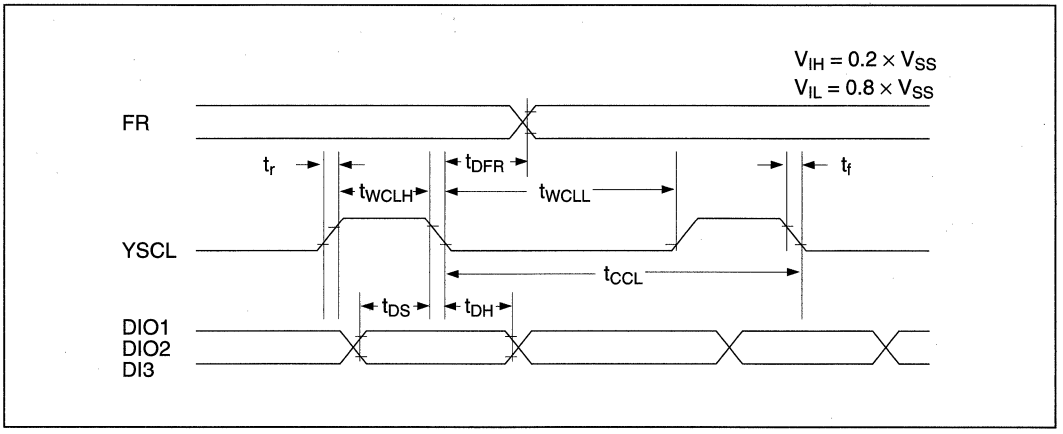
*3. The LSI may be permanently damaged if the logic system power is floating or V_{SS} is less than or equal to –2.6V when power is applied to the LC drive circuit system. Special caution must be paid to the power sequences when turning the power on and off.

● DC Electrical Characteristics

Unless otherwise specified, V_{DD} = V0 = 0V,
V_{SS} = –5.5 to –2.7V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Applicable Pins	Min	Typ	Max	Unit
Power voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V5		V5	–28.0	—	–12.0	V
Possible operating voltage	V5	Function operation	V5	—	—	–8.0	V
Power voltage (2)	V0		V0	–2.5	—	0	V
Power voltage (3) Power voltage (4)	V1 V4		V1 V4	2/9 × V5 V5	—	V_{DD} 7/9 × V5	V
High-level input voltage	V_{IH}		DIO1, DIO2, FR, YSCL, SHL, DI3, DSPOFF, SEL	0.2 × V_{SS}	—	—	V
Low-level input voltage	V_{IL}			—	—	0.8 × V_{SS}	V
High-level output voltage	V_{OH}	I_{OH} = –0.3mA	DIO1, DIO2	V_{DD} – 0.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 0.3mA		—	—	V_{SS} + 0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	YSCL, SHL, DI3, DSPOFF, FR, SEL	—	—	2.0	µA
I/O leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$	DIO1, DIO2	—	—	5.0	µA
Static current	I_{DDS}	V5 = –12.0 to –28.0V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{COM}	$\Delta\lvert V_{ON}\rvert$ = 0.5V, V0 = V_{DD}, V1 = –1.5V, V4 = –18.5V, V5 = –20.0V	O0 to O99	—	0.75	1.0	KΩ
Average operating consumption current (1)	I_{SS1}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 12KHz, Frame frequency = 60 Hz, Input data: 1/200; Ta = 25°C, Each duty cycle is "H", no load	V_{SS}	—	7	15	µA
		V_{SS} = –3.0V; other parameters are the same as for V_{SS} = –5.0V		—	5	10	µA
Average operating consumption current (2)	I_{SS2}	V_{SS} = –5.0V, V0 = 0V, V1 = –1.5V, V4 = –18.5V, VEE =V5 = –20.0V; other parameters are the same as for I_{SS1}	V5	—	7	15	µA
Input terminal capacitance	C_I	Ta = 25°C	YSCL, SHL, SEL, DSPOFF, FR, DI3	—	—	8	pF
I/O terminal capacitance	$C_{I/O}$		DIO1, DIO2	—	—	15	pF

- **AC Characteristics**
  - **Input Timing Characteristics**



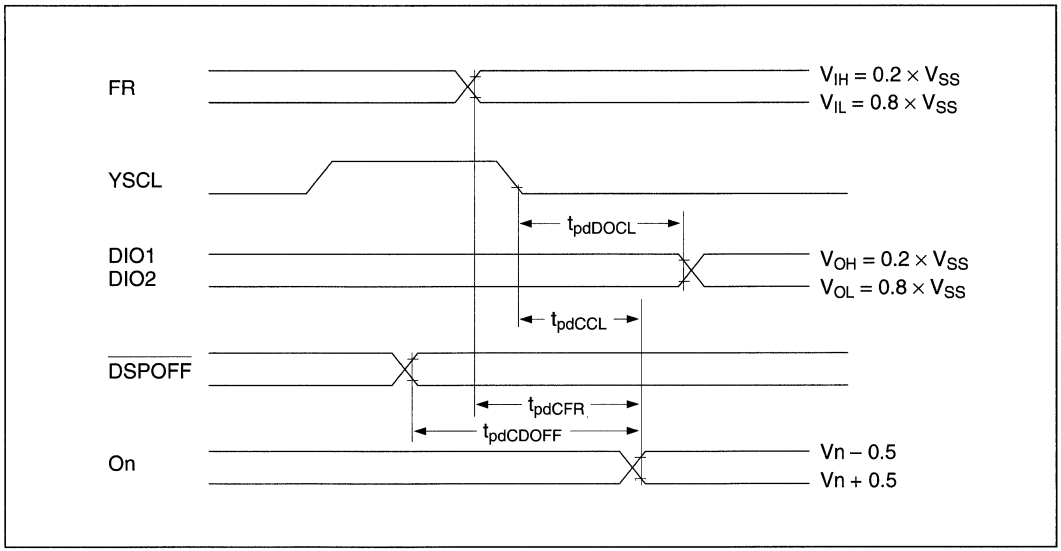
V_{SS} = –5.0 ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	tr		—	50	ns
Input signal fall time	tf		—	50	ns
YSCL frequency	t_{CCL}		500	—	ns
YSCL high-level pulse width	t_{WCLH}		70	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		100	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		–300	300	ns

V_{SS} = –4.5 to –2.7V, Ta = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	tr		—	50	ns
Input signal fall time	tf		—	50	ns
YSCL frequency	t_{CCL}		1000	—	ns
YSCL high-level pulse width	t_{WCLH}		160	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		200	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		–500	500	ns

○ Output Timing Characteristics



V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

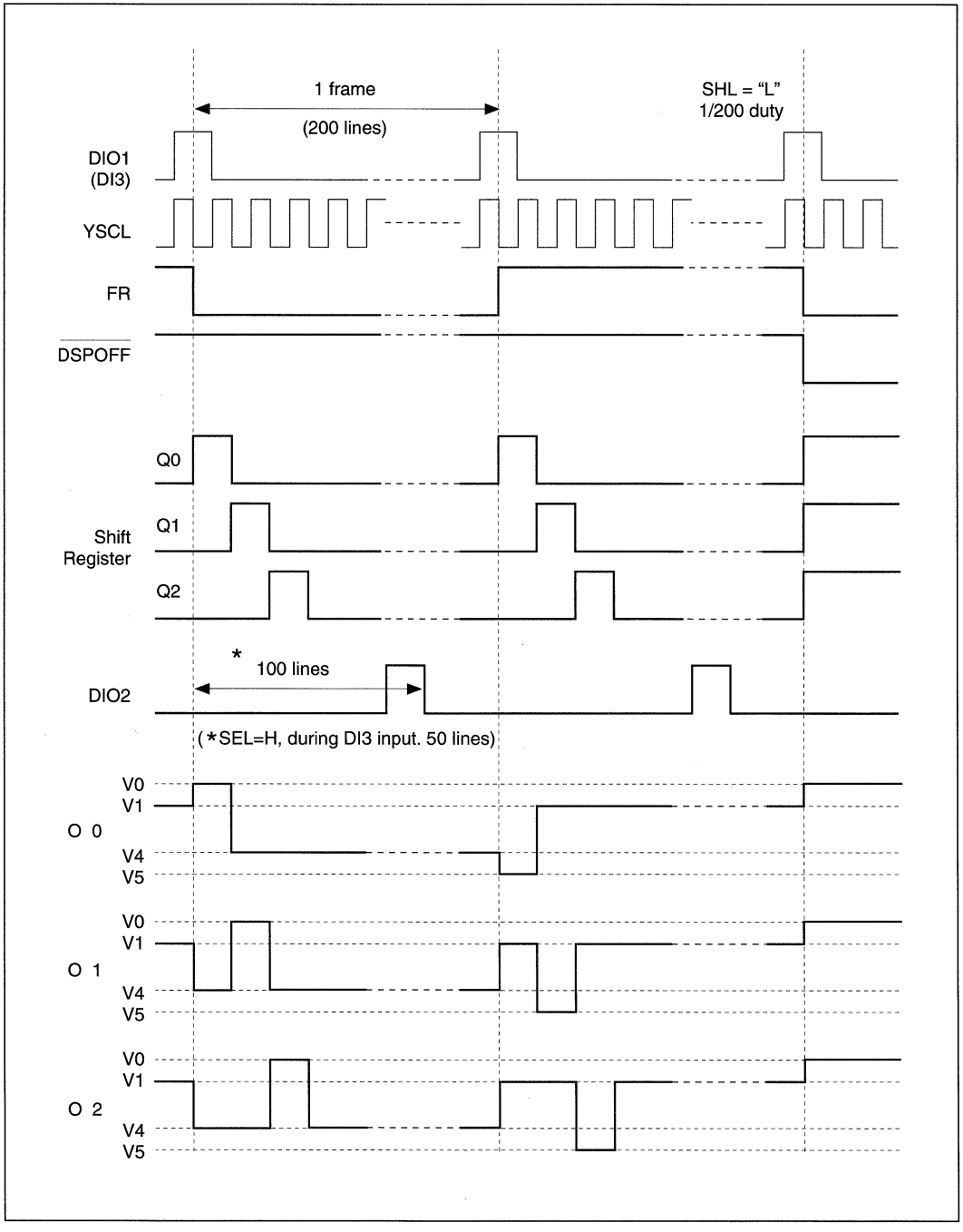
Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → DIO) delay time	t_{pdDOCL}	CL = 15pF	—	350	ns
(YSCL fall → On output) delay time	t_{pdCCL}	V5 = –12 to –28.0V	—	1.0	µs
($\overline{DSPOFF}$ → On output) delay time	$t_{pdCDOFF}$				
(FR → On output) delay time	t_{pdCFR}	CL = 100pF	—	1.0	µs

V_{SS} = –4.5 to –2.7V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → DIO) delay time	t_{pdDOCL}	CL = 15pF	—	400	ns
(YSCL fall → On output) delay time	t_{pdCCL}	V5 = –12 to –28.0V	—	2.0	µs
($\overline{DSPOFF}$ → On output) delay time	$t_{pdCDOFF}$				
(FR → On output) delay time	t_{pdCFR}	CL = 100pF	—	2.0	µs

○ **Timing Diagram**

Timing diagram (assuming 1/200 duty). (This diagram provided only as a reference)



■ LCD DRIVING POWER

● Method of Forming Each Voltage Level

The simplest way to obtain the voltage levels for driving the LCs is to use resistive voltage dividers between V5 and V_{DD}, and to drive the LCs with op amp voltage followers.

In consideration of the use of op amps, V0 and V_{DD} are separated and given separate terminals. When op amps are not going to be used, connect V0 to V_{DD}.

When a resistive voltage divider is used, select the lowest resistances allowed by the system power supply tolerances.

Permanent damage may result to the LSI when there is serial resistance in the V_{DD} power line. This is because the voltage drop that will occur at V_{DD} will cause the power level relationships within the LCD (i.e., $V_{DD} \geq V0 \geq V1 > V4 \geq V5$) to fail.

When a guard resistance is inserted, voltage stabilization using a capacitance is necessary.

● Cautions During Power Up and Power Down

Because of the high voltage of the LC driving system of this LSI, if the power to the logic system is floating or if V_{SS} is less than or equal to –2.5V when a high voltage is applied to the LC driving system, then too much current will flow, causing damage to the LSI.

It is recommended that the display off function ($\overline{DSPOFF}$) be used to keep the LCD driver output level at V0 until the LCD drive system voltage stabilizes.

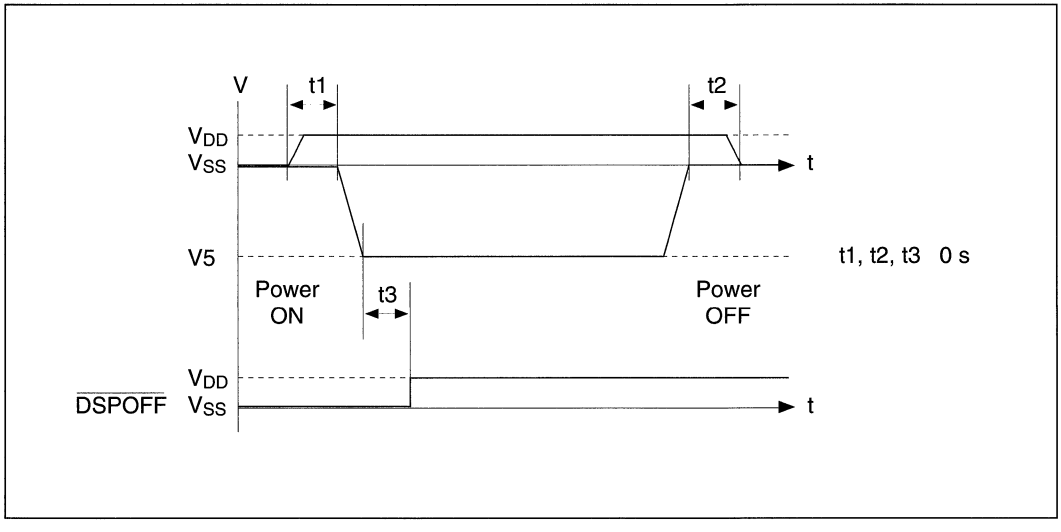
Follow the sequences below during power up and power down:

Power up: Logic system on → LC drive system on (or simultaneous)

Power down: LC drive system off → Logic system off (or simultaneous)

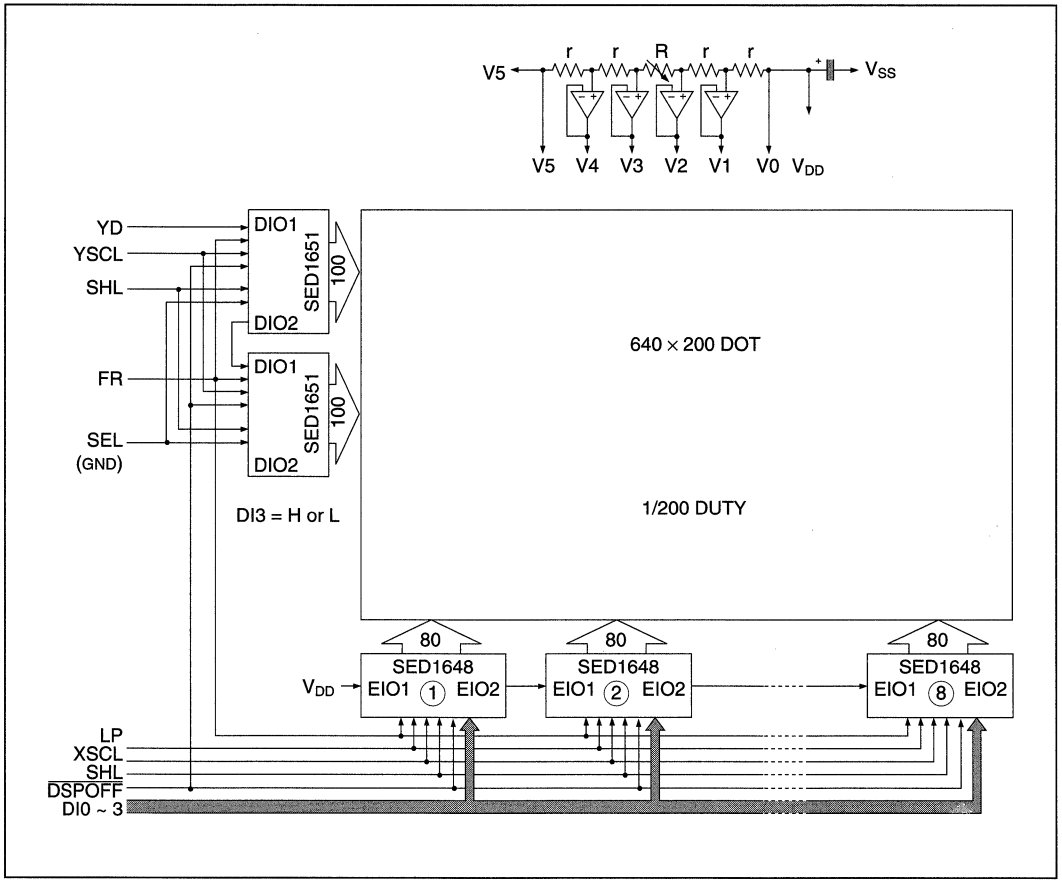
As a way to prevent excessive current, insert a high-speed fuse or guard resistance in series with the LC power source.

The optimal value of the guard resistance must be selected based on the capacitance of the LC cells.

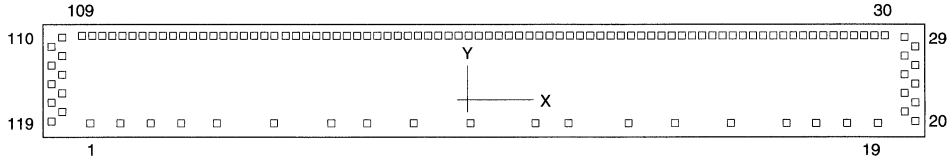


■ EXAMPLE OF CONNECTION

● Large Screen LCD Structure Diagram

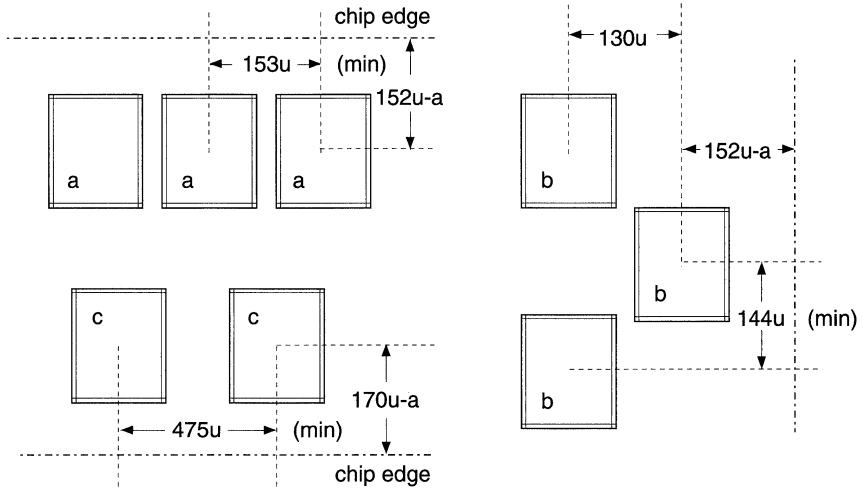


■ PAD LAYOUT



Chip size ..... 13.43 mm × 1.76 mm
Chip thickness ..... 400 μm (TYP)

Al Pad Specifications (SED1651D0A)



Pad a aperture (X, Y): ..... 110 × 110 μm PAD No. 30-109
Pad b aperture (X, Y): ..... 110 × 110 μm PAD No. 20-29, 110-119
Pad c aperture (X, Y): ..... 110 × 110 μm PAD No. 1-19

■ PAD COORDINATES

Unit: μm

Pad No.	Pad Name	X Coord.	Y Coord.
1	DIO2	–5985	–709
2	V0	–5510	–709
3	V1	–5035	–709
4	V4	–4560	–709
5	V5	–4038	–709
6	V_{SS}	–3164	–709
7	SEL	–2280	–709
8	SHL	–1767	–709
9	DI3	–1064	–709
10	YSCL	–181	–709
11	V_{DD}	770	–709
12	$\overline{DSPOFF}$	1283	–709
13	FR	2176	–709
14	V_{SS}	2879	–709
15	V5	3753	–709
16	V4	4560	–709
17	V1	5035	–709
18	V0	5510	–709
19	DIO1	5985	–709
20	O0	6560	–610
21	O1	6430	–466
22	O2	6560	–321
23	O3	6430	–177
24	O4	6560	–32
25	O5	6430	112
26	O6	6560	257
27	O7	6430	401
28	O8	6560	545
29	O9	6430	690
30	O10	6079	727
31	O11	5925	727
32	O12	5771	727
33	O13	5617	727
34	O14	5463	727
35	O15	5310	727
36	O16	5156	727
37	O17	5002	727
38	O18	4848	727
39	O19	4694	727
40	O20	4540	727
41	O21	4386	727
42	O22	4232	727
43	O23	4078	727
44	O24	3924	727
45	O25	3771	727
46	O26	3617	727
47	O27	3463	727
48	O28	3309	727
49	O29	3155	727
50	O30	3001	727
51	O31	2847	727
52	O32	2693	727
53	O33	2539	727
54	O34	2385	727
55	O35	2232	727
56	O36	2078	727
57	O37	1924	727
58	O38	1770	727
59	O39	1616	727
60	O40	1462	727
61	O41	1308	727
62	O42	1154	727
63	O43	1000	727
64	O44	846	727
65	O45	693	727
66	O46	539	727
67	O47	385	727
68	O48	231	727
69	O49	77	727
70	O50	–77	727
71	O51	–231	727
72	O52	–385	727
73	O53	–539	727
74	O54	–693	727
75	O55	–846	727
76	O56	–1000	727
77	O57	–1154	727
78	O58	–1308	727
79	O59	–1462	727
80	O60	–1616	727
81	O61	–1770	727
82	O62	–1924	727
83	O63	–2078	727
84	O64	–2232	727
85	O65	–2385	727
86	O66	–2539	727
87	O67	–2693	727
88	O68	–2847	727
89	O69	–3001	727
90	O70	–3155	727
91	O71	–3309	727
92	O72	–3463	727
93	O73	–3617	727
94	O74	–3771	727
95	O75	–3924	727
96	O76	–4078	727
97	O77	–4232	727
98	O78	–4386	727
99	O79	–4540	727
100	O80	–4694	727
101	O81	–4848	727
102	O82	–5002	727
103	O83	–5156	727
104	O84	–5310	727
105	O85	–5463	727
106	O86	–5617	727
107	O87	–5771	727
108	O88	–5925	727
109	O89	–6079	727
110	O90	–6430	690
111	O91	–6560	545
112	O92	–6430	401
113	O93	–6560	257
114	O94	–6430	112
115	O95	–6560	–32
116	O96	–6430	–177
117	O97	–6560	–321
118	O98	–6430	–466
119	O99	–6560	–610

SED1733

- **CMOS 100-Bit Common Driver**
- **High-Voltage LCD Driver**

■ DESCRIPTION

The SED1733 is a 100-bit output LCD common (row) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of LCD drive voltages.

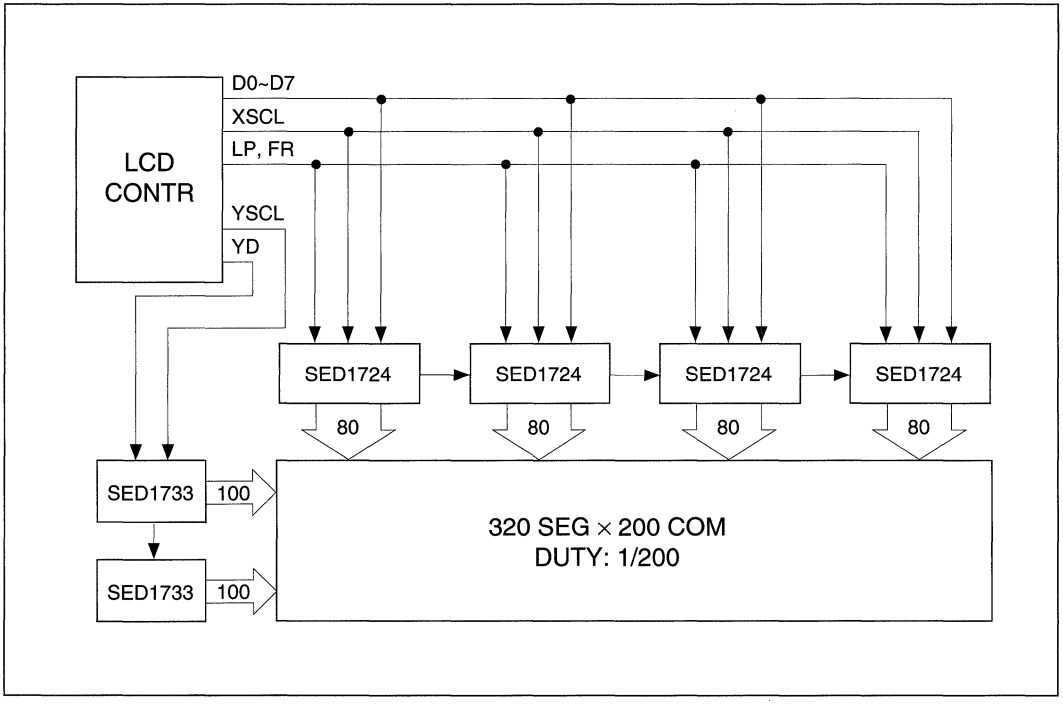
The device uses a high-speed daisy-chain enable system which decreases power consumption and eliminates the need for separate signals for each driver.

The SED1733 is used in conjunction with the SED1722 or SED1724 segment drivers to support a large-capacity dot matrix LCD panel.

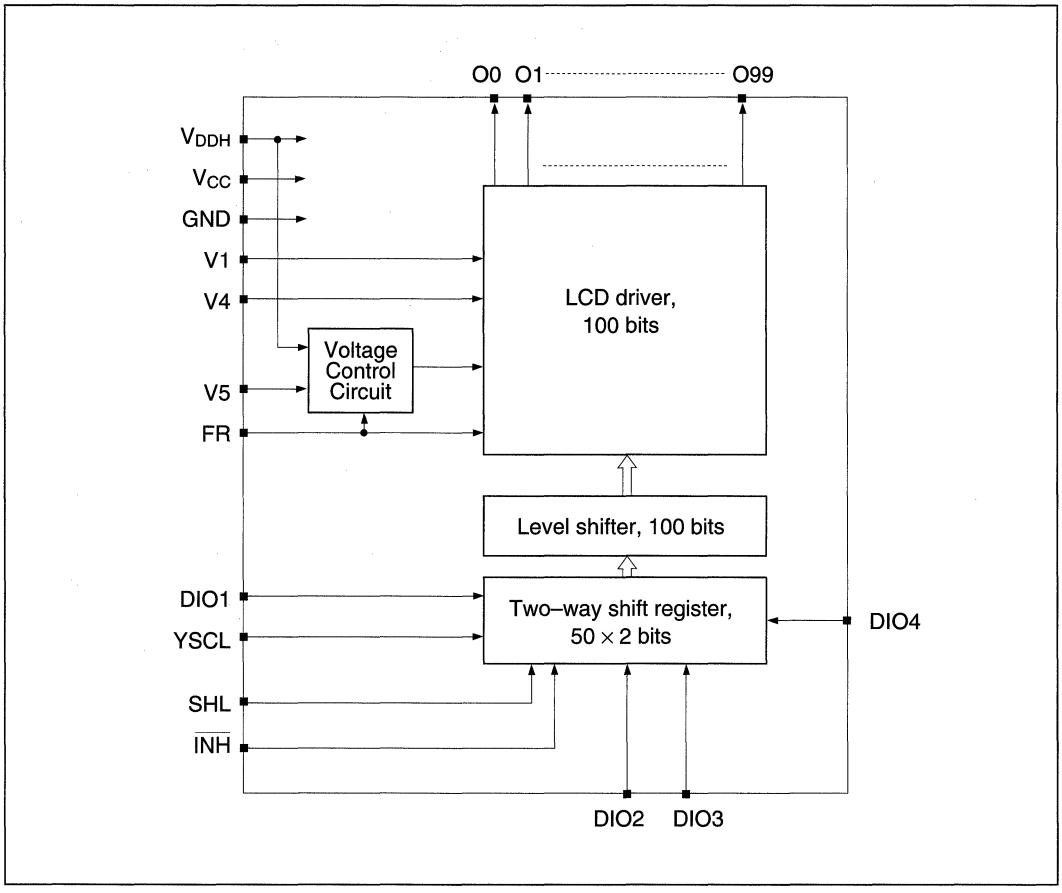
■ FEATURES

- Low-power high-speed CMOS technology
- 100-bit common (row) driver
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Selectable output shift direction
- Supports display blanking
- Supports high-speed data transfer
- Low output resistance
- Ability to adjust offset bias of the LCD source from V_{DD}
- Wide range of LCD voltage .... 14 to 40V
- Supply voltage ..... 4.5 to 5.5V
- Package ..... QFP-5 128 pins (F_{OA})
  Al pad (D_{OA})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Q'ty</th></tr>
<tr><td>O0 to O99</td><td>O</td><td>LCD crystal common (row) outputs
The output changes at the YSCL fall edge.</td><td>100</td></tr>
<tr><td>DIO1, DIO2
DIO3, DIO4</td><td>I/O</td><td>To input and output serial data of 50 × 2 bits two-way shift register.
Input or output is set by SHL input. Output changes at the YSCL fall edge.</td><td>4</td></tr>
<tr><td>YSCL</td><td>I</td><td>To input shift clock of serial data. Scanning data is shifted at the fall edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>To input the selection of shift direction and input-output control of DIO terminal.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">O (Output shift direction)</th><th colspan="2">DIO</th></tr>
<tr><th>1,3</th><th>2,4</th></tr>
<tr><td>L</td><td>0 → 99</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>99 → 0</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>To input blanking control of liquid crystal display.
Low level input brings all common outputs to non-section level.
<table>
<tr><th>$\overline{INH}$</th><th>FR</th><th>O0 to O99</th></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>To Input AC signal of liquid crystal driving output.</td><td>1</td></tr>
<tr><td>VCC, GND</td><td>Power Supply</td><td>Logic power supply. GND: 0 V; VCC: +5.0 V</td><td>2</td></tr>
<tr><td>V1, V4, V5, VDDH</td><td>Power Supply</td><td>Power supply for liquid crystal driving
VDDH: +14 V to +40 V; VDDH ≥ V1 ≥ 8/9 VDDH; 1/9 VDDH ≥ V4 ≥ V5 ≥ VDDH,
VDDH, V5: Selection level, V1, V4: Non-selection level</td><td>4</td></tr>
</table>

Total: 114 pins

■ FUNCTIONAL DESCRIPTION

● Shift Register

Bidirectional data shift register.

● Level Shifter

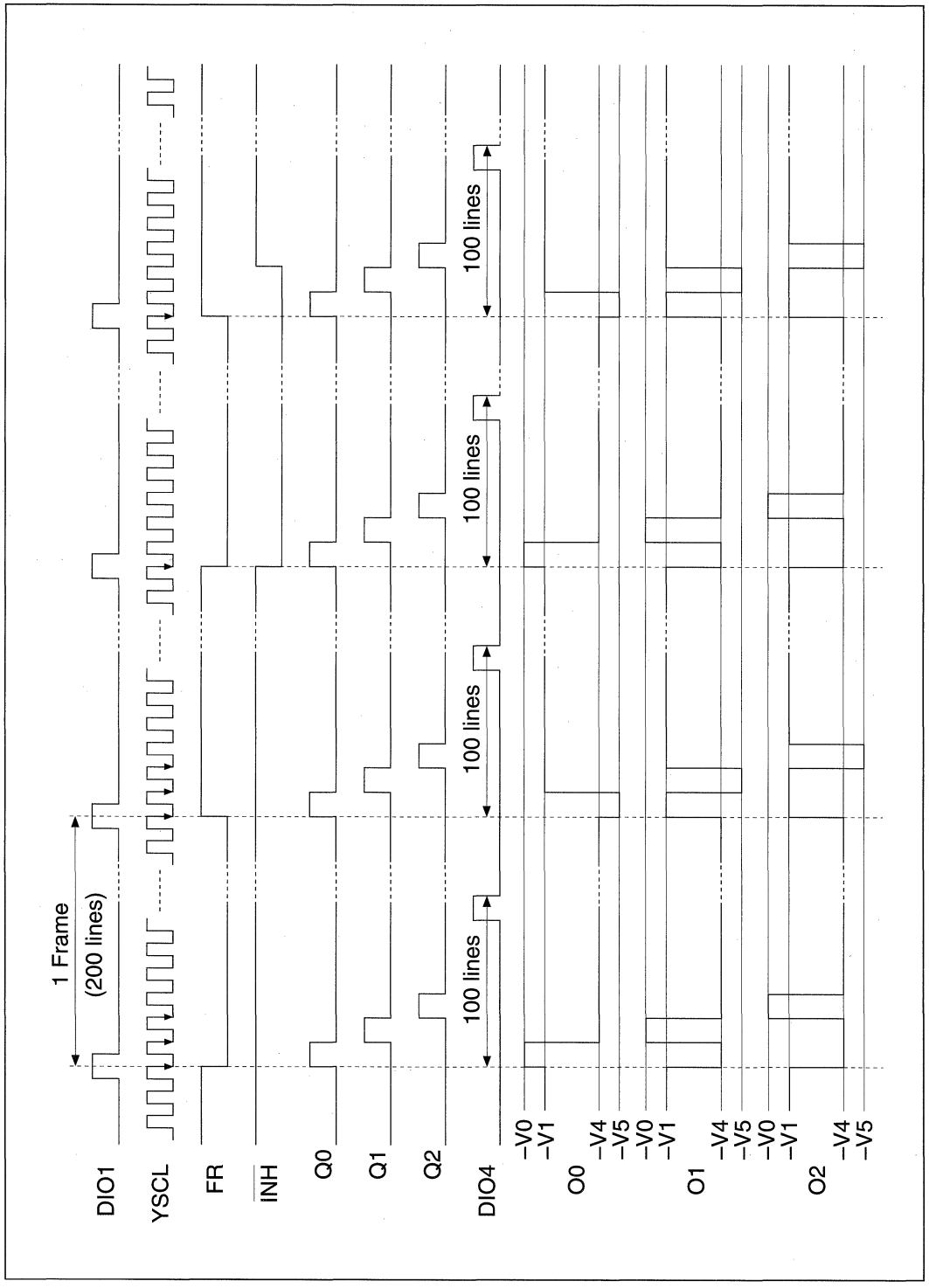
The level shifter converts the logic-level signals from the latch to the voltage levels required by the LCD drivers.

● LCD Drivers and Voltage Control Circuit

The LCD drivers drive individual columns of the display matrix with the voltage determined by the inhibit signal /INH, the frame signal FR, and the latched display data. This is shown in the table below.

/INH	Data	FR	SEG Output Voltage	
H	H	H	V5	Selected
		L	VDDH	
	L	H	V1	Deselected
		L	V4	
L	—	H	V1	Deselected
		L	V4	

■ TIMING CHART

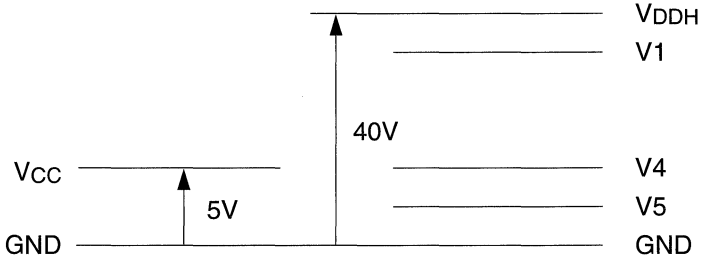


■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V1, V4, V5	–0.3 to V_{DDH} +0.3	V
Input voltage	V_I	–0.3 to V_{CC} +0.3	V
Output voltage	V_O	–0.3 to V_{CC} +0.3	V
DIO output current	I_{O1}	20	mA
LCD circuit output current	I_{O2}	20	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–65 to +150	°C

Note 1. Let the V_{DDH}, V1, V4 and V5 voltages maintain the condition, $V_{DDH} \geq V1 \geq V4 \geq V5 \geq GND$, all the time.



Note 2. If the logic circuit power supply comes to float while voltage is applied to the power supply of the liquid crystal driving circuit, the LSI may be broken permanently. So, prevent the logic circuit power supply from floating. Pay special attention to the power supply sequence when the system is switched on or off.

● **DC Electrical Characteristics**

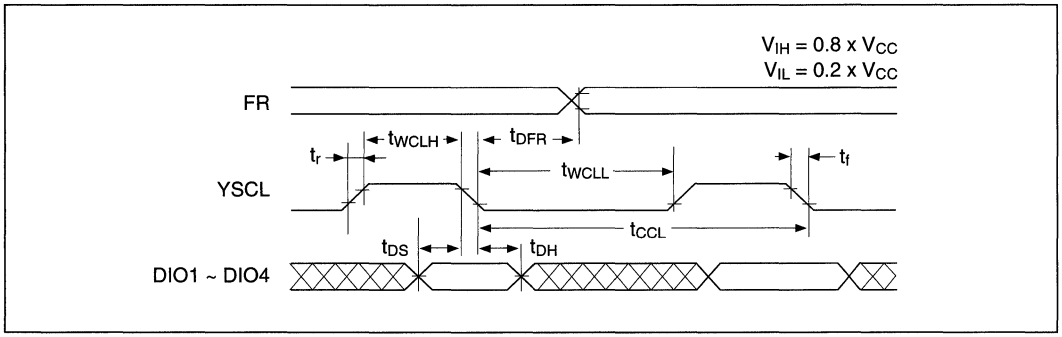
(Unless otherwise specified, GND = 0 V, V_{CC} = +5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Applicable Terminal	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}		V_{CC}	4.5	5.0	5.5	V
Recommended supply voltage	V_{DDH}		V_{DDH}	14.0	—	40.0	V
Operable voltage	V_{DDH}	Function	V_{DDH}	8.0	—	—	V
Supply voltage (2)	V1	Recommendation value	V1	8/9V_{DDH}	—	V_{DDH}	V
Supply voltage (3)	V4, V5	Recommendation value	V4, V5	GND	—	1/9V_{DDH}	V
High level input voltage	V_{IH}		DIO1 to DIO4	0.8V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}		$\overline{FR}$, YSCL, $\overline{INH}$, SHL	GND	—	0.2V_{CC}	V
High level output voltage	V_{OH}	I_{OH} = –0.3 mA	DIO1 to DIO4	V_{CC}–0.4	—	V_{CC}	V
Low level output voltage	V_{OL}	I_{OL} = 0.3 mA		GND	—	0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	$\overline{FR}$, YSCL, $\overline{INH}$, SHL	—	—	2.0	µA
Input–output leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}	DIO1 to DIO4	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 to 40.0 V V_{IH} = V_{CC}, V_{IL} = GND	GND	—	—	25	µA
Output resistance	R_{COM}	ΔV_{ON} = 0.5V, V_{DDH}=+30.0V	*1 O0 to O99	—	0.7	1.8	kΩ
		ΔV_{ON} = 0.5V, V_{DDH}=+20.0V		—	0.8	2.2	kΩ
		ΔV_{ON} = 0.5V, V_{DDH}=+14.0V		—	1.0	2.6	kΩ
Current consumed (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC}, V_{IL} = GND, f_{YSCL} =33.6 kHz, f_{FR} =70 Hz; Input data: 1/480, "H" is input every duty. Common has no load.	V_{CC}	—	30	60	µA
Current consumed (2)	I_{DDH}	V_{CC} = +5.0 V, V4 = +4.0 V, V1 = +26.0 V, V_{DDH} =+30.0V, Other conditions are same as those of I_{DD}	V_{DDH}	—	45	120	µA
Input terminal capacity	C_I	Freq.=1 MHz, T_a = 25°C Solid chip	$\overline{FR}$, YSCL, $\overline{INH}$, SHL	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		DIO1 to EIO4	—	—	15	pF

*1 The output resistance is specified within the ranges of the supply voltages (2) and (3).

● AC Electrical Characteristics

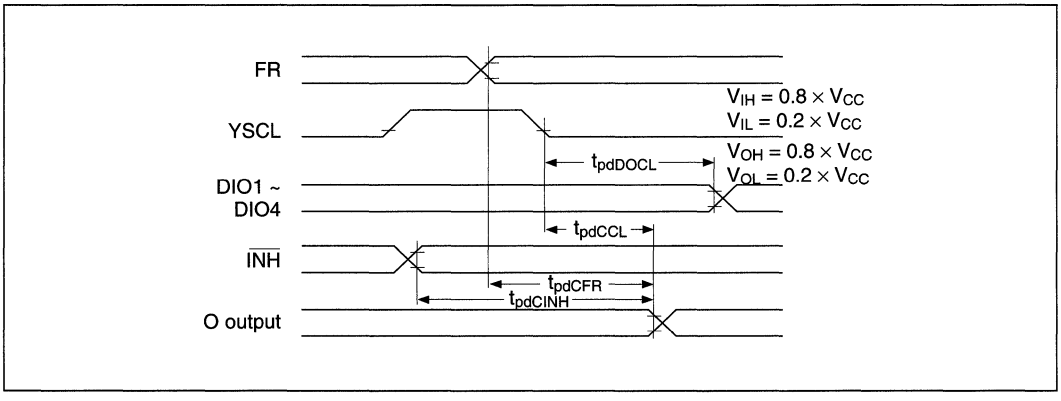
○ Input Timing Characteristics



(VCC = 5.0 V ±10%, Ta = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input signal rise time	t_r		—	—	50	ns
Input signal rise time	t_f		—	—	50	ns
YSCL cycle time	t_{CCL}		400	—	—	ns
YSCL high level pulse width	t_{WCLH}		70	—	—	ns
YSCL low level pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
FR delay allowable time	t_{DFR}		–300	—	300	ns

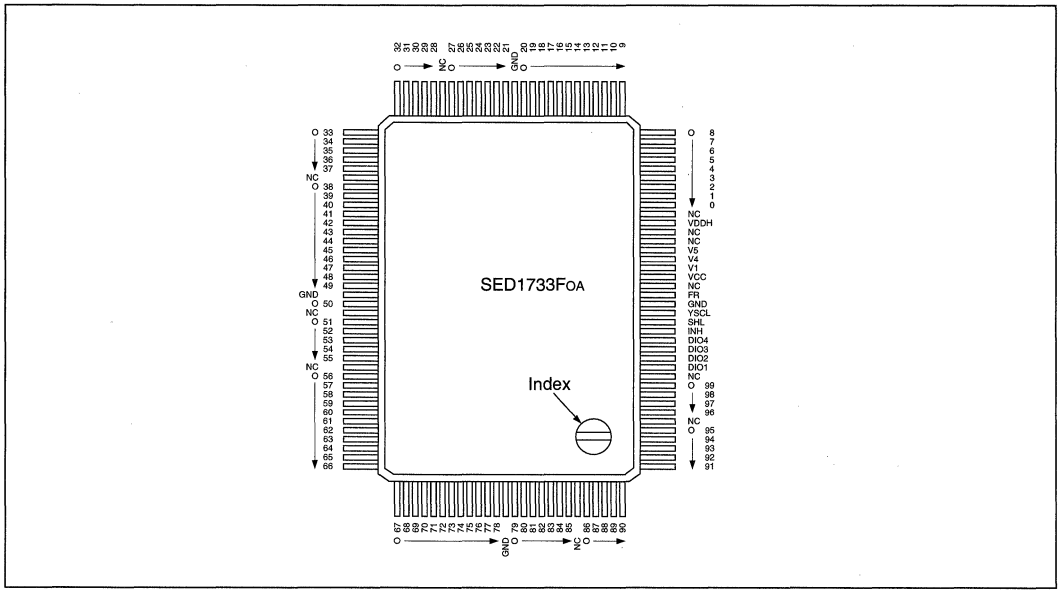
○ Output Timing Characteristics



(VCC = +5.0 V ±10%, VDDH = +40.0 V, Ta = –20 to 75°C)

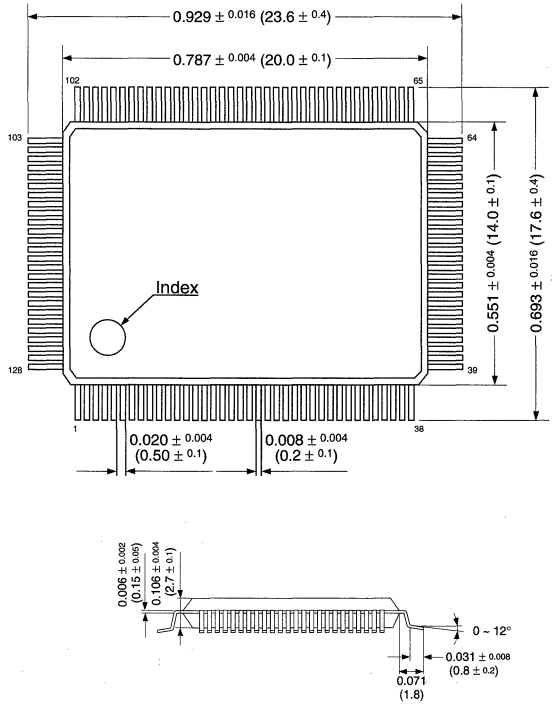
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL fall to DIO delay time	t_{pdDOCL}	C_L = 15 pF	—	—	300	ns
YSCL fall to O delay time	t_{pdCCL}		—	—	0.7	µs
$\overline{INH}$ to O output delay time	t_{pdCINH}	C_L = 100 pF	—	—	0.7	µs
FR to O output delay time	t_{pdCFR}		—	—	0.7	µs

■ PACKAGE DIMENSIONS (SED1733F0A)

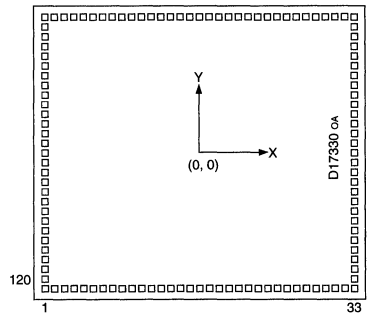


■ PLASTIC QFP5-128PIN-S1

Unit: inch (mm)



■ PAD LAYOUT



Chip Dimensions	6.10 mm × 5.30 mm
Pad pitch	0.170 mm (Min.)
Chip thickness	0.400 ±0.025 mm
Aluminum pad opening	100 μm × 100 μm (all terminals)

■ PAD COORDINATES

Pad		X	Y
Number	Name	(μm)	(μm)
1	O 92	–2882	–2482
2	O 93	–2620	–2482
3	O 94	–2420	–2482
4	O 95	–2230	–2482
5	O 96	–2050	–2482
6	O 97	–1870	–2482
7	O 98	–1700	–2482
8	O 99	–1530	–2482
9	NC	–1360	–2482
10	DIO1	–1190	–2482
11	DIO2	–1020	–2482
12	DIO3	–850	–2482
13	DIO4	–680	–2482
14	$\overline{INH}$	–510	–2482
15	SHL	–340	–2482
16	YSCL	–170	–2482
17	GND	0	–2482
18	FR	170	–2482
19	V_{CC}	340	–2482
20	V1	510	–2482
21	V4	680	–2482
22	V5	850	–2482
23	NC	1020	–2482
24	V_{DDH}	1190	–2482
25	NC	1360	–2482
26	O 0	1530	–2482
27	O 1	1700	–2482
28	O 2	1870	–2482
29	O 3	2050	–2482
30	O 4	2230	–2482
31	O 5	2420	–2482
32	O 6	2620	–2482
33	O 7	2882	–2482
34	O 8	2882	–2482
35	O 9	2882	–2060
36	O 10	2882	–1880
37	O 11	2882	–1700
38	O 12	2882	–1530
39	O 13	2882	–1360
40	O 14	2882	–1190

Pad		X	Y
Number	Name	(μm)	(μm)
41	O 15	2882	–1020
42	O 16	2882	–850
43	O 17	2882	–680
44	O 18	2882	–510
45	O 19	2882	–340
46	O 20	2882	–170
47	GND	2882	0
48	O 21	2882	170
49	O 22	2882	340
50	O 23	2882	510
51	O 24	2882	680
52	O 25	2882	850
53	O 26	2882	1020
54	O 27	2882	1190
55	O 28	2882	1360
56	O 29	2882	1530
57	O 30	2882	1700
58	O 31	2882	1880
59	O 32	2882	2060
60	O 33	2882	2250
61	O 34	2882	2482
62	O 35	2620	2482
63	O 36	2420	2482
64	O 37	2230	2482
65	O 38	2050	2482
66	O 39	1870	2482
67	O 40	1700	2482
68	O 41	1530	2482
69	O 42	1360	2482
70	O 43	1190	2482
71	O 44	1020	2482
72	O 45	850	2482
73	O 46	680	2482
74	O 47	510	2482
75	O 48	340	2482
76	O 49	170	2482
77	GND	0	2482
78	O 50	–170	2482
79	O 51	–340	2482
80	O 52	–510	2482

Pad		X	Y
Number	Name	(μm)	(μm)
81	O 53	–680	2482
82	O 54	–850	2482
83	O 55	–1020	2482
84	O 56	–1190	2482
85	O 57	–1360	2482
86	O 58	–1530	2482
87	O 59	–1700	2482
88	O 60	–1870	2482
89	O 61	–2050	2482
90	O 62	–2230	2482
91	O 63	–2420	2482
92	O 64	–2620	2482
93	O 65	–2882	2482
94	O 66	–2882	2250
95	O 67	–2882	2060
96	O 68	–2882	1880
97	O 69	–2882	1700
98	O 70	–2882	1530
99	O 71	–2882	1360
100	O 72	–2882	1190
101	O 73	–2882	1020
102	O 74	–2882	850
103	O 75	–2882	680
104	O 76	–2882	510
105	O 77	–2882	340
106	O 78	–2882	170
107	GND	–2882	0
108	O 79	–2882	–170
109	O 80	–2882	–340
110	O 81	–2882	–510
111	O 82	–2882	–680
112	O 83	–2882	–850
113	O 84	–2882	–1020
114	O 85	–2882	–1190
115	O 86	–2882	–1360
116	O 87	–2882	–1530
117	O 88	–2882	–1700
118	O 89	–2882	–1880
119	O 90	–2882	–2060
120	O 91	–2882	–2250

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■ DESCRIPTION

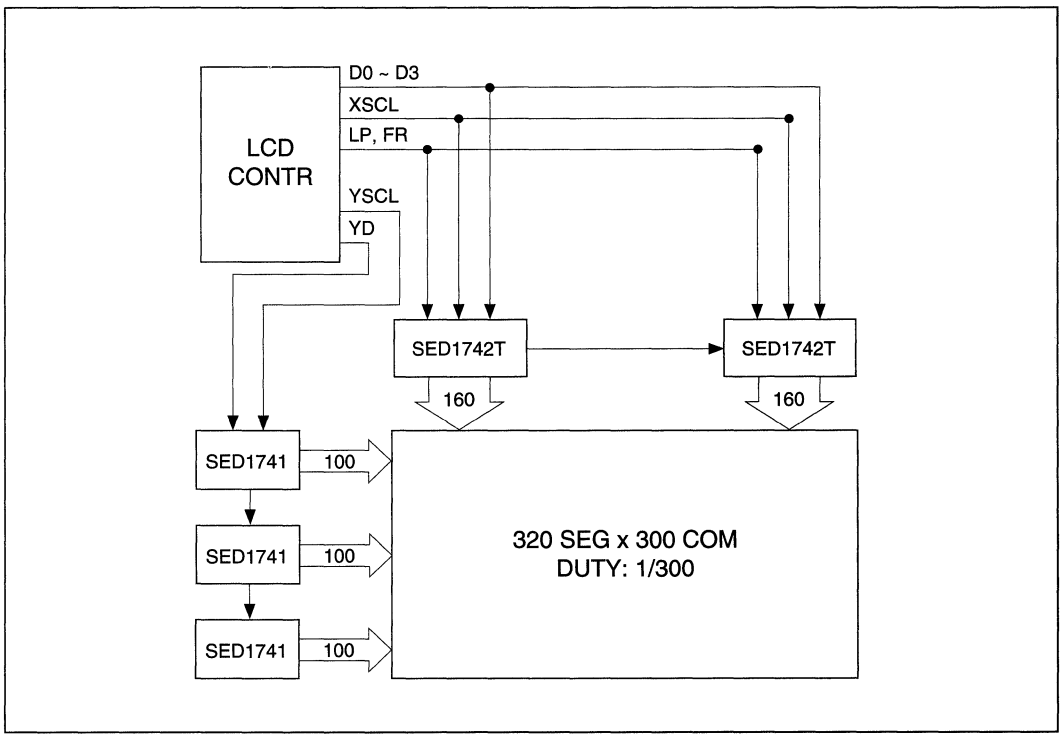
The SED1741 is a 100 (50 × 2) dot matrix LCD common (row) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of LCD drive voltages. The device uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1741 is used in conjunction with the SED1742/44 (160-bit segment driver) to drive a large-capacity dot matrix LCD panel.

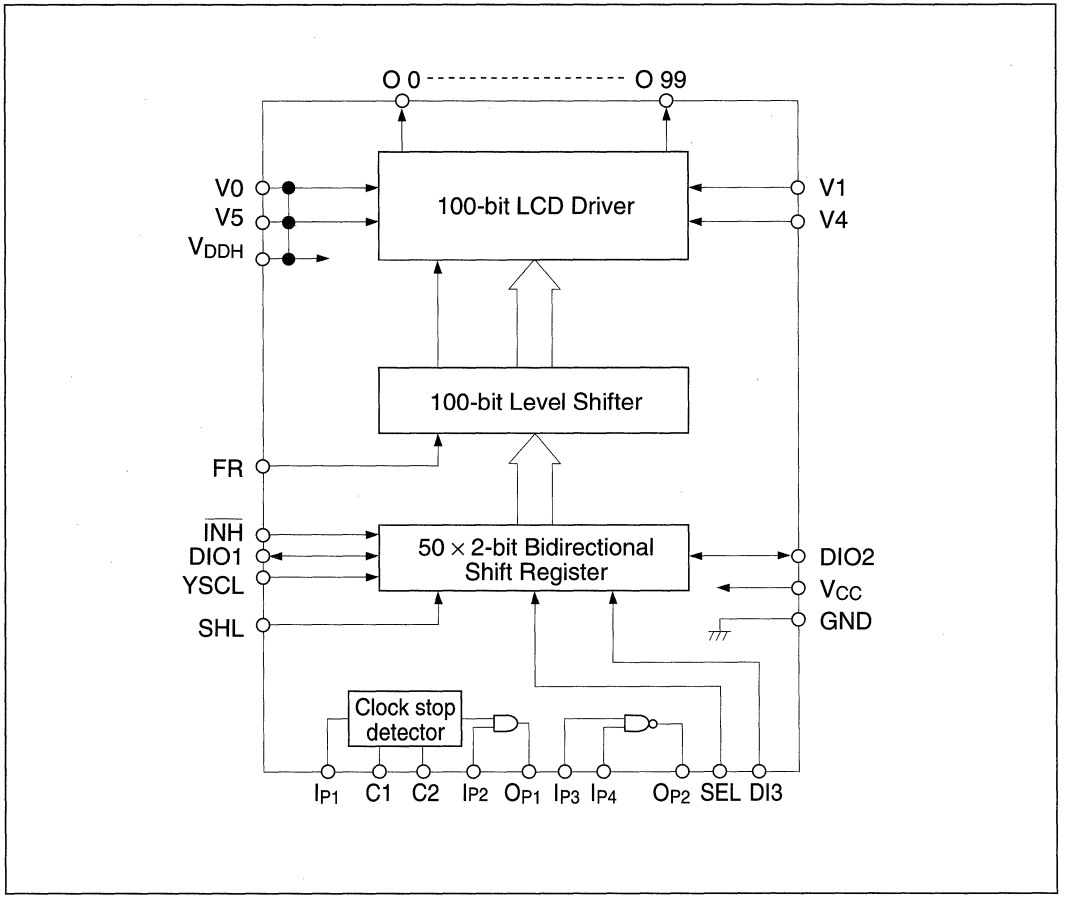
■ FEATURES

- Low-power high-speed CMOS technology
- 100-bit (50 × 2) common (row) driver
- Duty cycle ..... 1/100 to 1/500
- Adjustable LCD drive voltages
- Unbiased display off function
- Adjustable offset bias of the LCD according to V_{DDH} and GND
- Built-in circuit for clock stop detection
- Ability to adjust offset bias of the LCD source from V_{DD}
- Pin selectable output shift direction
- Low output impedance 1KΩ
- LCD voltage ..... 14 to 42V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... Au bump (D_{1B})
  TAB (T_{OA})

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Shift Register

This is a bidirectional shift register for common data transmission.

● Level Shifter

This is a voltage level interface circuit for shifting the signal voltage from the logic system level to the LCD driver system level.

● LCD Driver

This outputs the LCD driver voltage.

The table below shows the relationships between the display blanking signal $\overline{INH}$, the contents of the shift register, the alternating current signal FR, and the common output voltage.

$\overline{INH}$	Contents of Shift Register	FR	O Output Voltage
H	H	H	V5
		L	V0 (V_{DDH})
	L	H	V1
		L	V4
L	—	—	V5

● Clock Stopped Detection Circuit

When the alternating current drive clock stops during the time when a voltage is applied to a liquid crystal cell, the liquid crystal cell may experience DC deterioration. This circuit is able to detect alternating current drive clock stoppages and removes the voltage from the liquid crystal cell by supplying an input to the $\overline{INH}$ terminal as a detection signal.

■ PIN DESCRIPTION

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Q'ty</th></tr>
<tr><td>O0 to 99</td><td>O</td><td>Common (row) output for LCD drive. The signal changes at the falling edge of YSCL.</td><td>100*</td></tr>
<tr><td>DIO1, DIO2
DI3</td><td>I/O
I</td><td>Scan pulse of 50 × 2-bit bi-directional shift register.
They are set to the input or output depending on the SHL input.
The output changes at the falling edge of YSCL.
Input terminal of scan pulse in 50 × 2-bit configuration.
If SEL = low, DI3 = Vcc or GND.</td><td>3</td></tr>
<tr><td>SEL</td><td>I</td><td>Selective input of bi-directional shift register operation mode.
High: 50 × 2 (SI3 input); low: 100.</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Shift clock input of serial data. The scan data is shifted at the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Used for shift direction selection and I/O control input of DIO terminal.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">Output Shift Direction</th><th colspan="2">DIO</th></tr>
<tr><th>DIO1</th><th>DIO2</th></tr>
<tr><td>L</td><td>0 ——► 99</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>99 ——► 0</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>AC conversion signal input of LCD drive output.</td><td>1</td></tr>
<tr><td>Vcc, GND</td><td>Power supply</td><td>Logic power supply GND : 0V Vcc : +3, +5V</td><td>2</td></tr>
<tr><td>V0, V1, V4,
V5, VDDH</td><td>Power supply</td><td>LCD drive power supply GND : 0V VDDH : +14 to +40V
VDDH (V0) ≥ V1 ≥ 8/9 VDDH
1/9 VDDH ≥ V4 ≥ V5 ≥ GND</td><td>5</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Blanking control input of LCD display. All common outputs are set to the V5 level during low level input.</td><td>1</td></tr>
<tr><td>IP1</td><td>I</td><td>Clock stop detect input.</td><td>1</td></tr>
<tr><td>IP2</td><td>I</td><td>Signal input ANDed with clock stop detect output; the pull-down resistor is provided.</td><td>1</td></tr>
<tr><td>C1</td><td>O</td><td>First charge hold terminal. An external capacitor must be added to the GND.</td><td>1</td></tr>
<tr><td>C2</td><td>O</td><td>Second charge hold terminal. An external capacitor and resistor must be added to the GND.</td><td>1</td></tr>
<tr><td>OP1</td><td>O</td><td>Clock stop detect output.</td><td>1</td></tr>
<tr><td>IP3</td><td>I</td><td>NAND gate input with pull-down resistor.</td><td>1</td></tr>
<tr><td>IP4</td><td>I</td><td>NAND gate input.</td><td>1</td></tr>
<tr><td>OP2</td><td>O</td><td>NAND gate output.</td><td>1</td></tr>
</table>

* NC: 60.

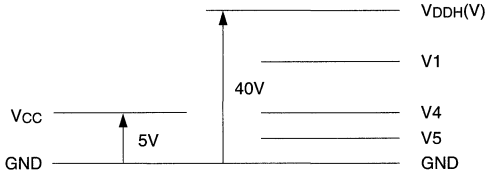
■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power voltage (1)	V_{CC}	–0.3 to +7.0	V
Power voltage (2)	V_{DDH}	–0.3 to +45.0	V
Power voltage (3)	V0, V1, V4, V5	GND – 0.3 to V_{DDH} + 0.3	V
Input voltage	V1	GND – 0.3 to V_{CC} + 0.3	V
Output voltage	V0	GND – 0.3 to V_{CC} + 0.3	V
DIO output current	IO1	20	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature 1	T_{stg1}	–65 to +150	°C
Storage temperature 2	T_{stg2}	–55 to +100	°C

Notes:

1. The voltage is based at GND = 0 V.
2. The storage temperature 1 is specified for a single chip and the storage temperature 2 is specified for TCP mounting.
3. Voltages V0, V1 and V4 must satisfy the following condition: V_{DDH} (V0) ≥ V1 ≥ V4 ≥ V5 ≥ GND.



4. If the logic power supply is floating or if it drops below V_{SS} = 2.9V_{dc} when the LCD drive is powered, the LSI may be destroyed permanently. Care must be taken especially during the on/off sequence of the system power supply.

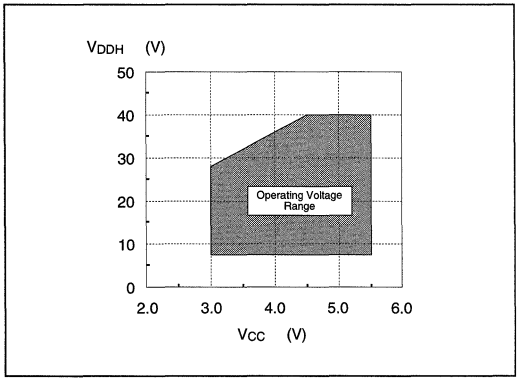
● DC Electrical Characteristics

Unless otherwise noted, GND = V5 = 0V, V_{CC} = +5.0V_{dc} ± 10%, T_a –20 to +75°C

Parameter	Symbol	Conditions		Applicable Pins	Min	Typ	Max	Unit
Power voltage (1)	V_{CC}			V_{CC}	3.0	5.0	5.5	V
Recommended operating voltage	V_{DDH}			V_{DDH}	14.0	—	40.0	V
Operable voltage	V_{DDH}	Function		V_{DDH}	8.0	—	—	V
Power voltage (2)	V1	Recommended value		V1	8/9 × V_{DDH}	—	—	V
Power voltage (3)	V4, V5	Recommended value		V4, V5	GND	—	1/9 × V_{DDH}	V
High-level input voltage	V_{IH}	V_{CC} = +3.0 to +5.5V		DIO1, DIO2, DI3, IP1 to 4, SEL, FR, YSCL, SHL, INH	0.8 × V_{CC}	—	—	V
Low-level input voltage	V_{IL}				—	—	0.2 × V_{CC}	V
High-level output voltage	V_{OH}	V_{CC} = +3 to +5.5V	I_{OH} = –0.3mA	DIO1, DIO2, OP1, OP2	V_{CC} – 0.4	—	—	V
Low-level output voltage	V_{OL}		I_{OL} = 0.3mA		—	—	0.4	V
Input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		DI3, SEL, FR, YSCL, SHL, INH	—	—	2.0	µA
Input current	I_{IH}	V_{IN} ≤ V_{CC} (IP4 = C2 = GND)		IP2, IP3	40	80	180	µA
I/O leakage current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		DIO1, DIO2	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = +14.0 to +40.0V V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Output resistance	R_{COM}	$\Delta\lvert V_{ON}\rvert$ = 0.5V Recommended conditions	V_{DDH} = +30.0V	O0 to O99	—	1.0	2.3	KΩ
			V_{DDH} = +20.0V		—	1.2	2.8	KΩ
Average operating consumption current (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} = GND, f_{YSCL} = 33.6kHz, t_{FR} = 70Hz, Input data: 1/480, no load		V_{CC}	—	9	20	µA
		V_{CC} = +3.0V_{dc}; other parameters are the same as for V_{CC} = +5.0V			—	6	10	
Average operating consumption current (2)	I_{DDH}	V_{DDH} = V0 = +30.0V V1 = +28.0V, V4 = +2.0V, V5 = 0.0V; other parameters are the same as for I_{CC}		V_{DDH}	—	18	40	µA
Input terminal capacity	C_I	Freq. = 1 MHz, T_a = 25°C, separate chip		DI3, IP1 to 4, SEL, FR, YSCL, SHL, INH	—	—	8	pF
I/O terminal capacity	$C_{I/O}$			DIO1, DIO2	—	—	15	pF

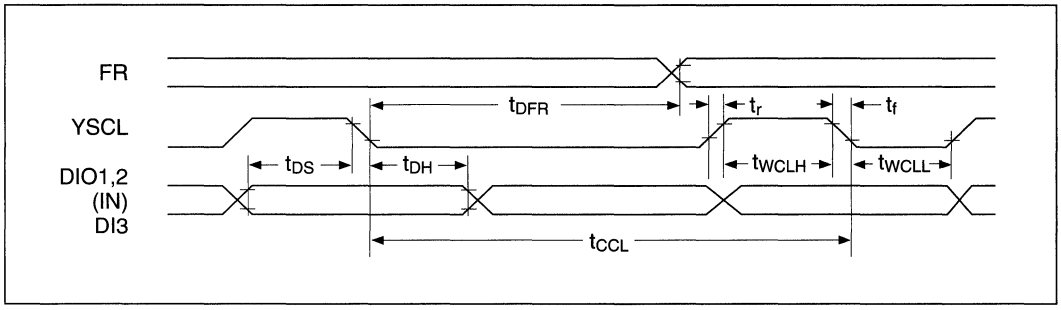
● Operating Voltage Range (V_{CC}–V_{DDH})

The V_{DDH} voltage must be set within the following operating voltage range of V_{CC} to V_{DDH}.



● AC Electrical Characteristics

○ Input Timing Characteristics



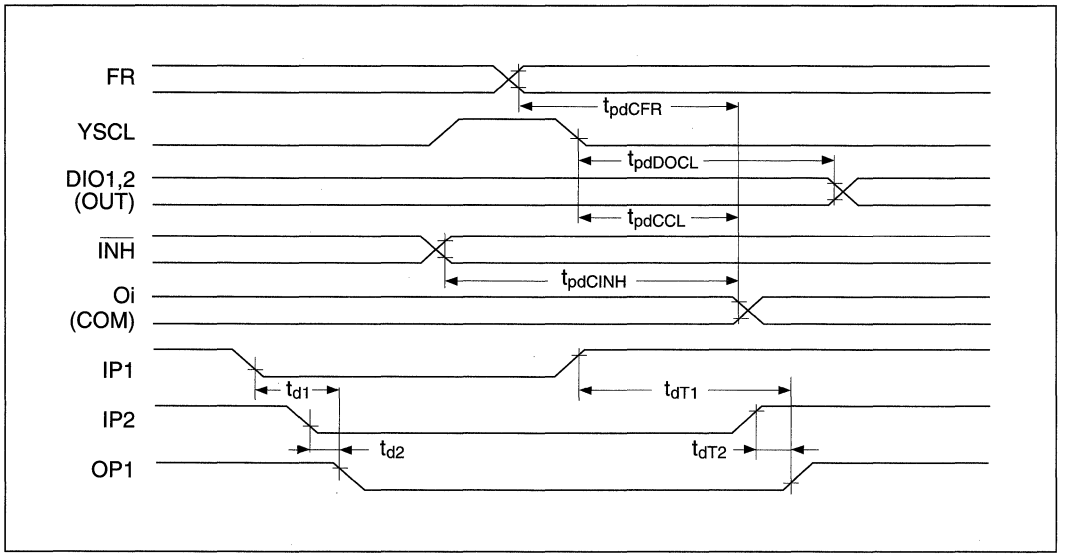
V_{CC} = +5.0V ± 10%, T_a = –20 to 75°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL cycle	t_{CCL}		400	—	—	ns
YSCL high-level pulse width	t_{WCLH}		70	—	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
FR delay allowance time	t_{DFR}		–300	—	+300	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns

V_{CC} = +5.0V ± 10%, T_a = –20 to 75°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL cycle	t_{CCL}		800	—	—	ns
YSCL high-level pulse width	t_{WCLH}		140	—	—	ns
YSCL low-level pulse width	t_{WCLL}		660	—	—	ns
Data setup time	t_{DS}		200	—	—	ns
Data hold time	t_{DH}		80	—	—	ns
FR delay allowance time	t_{DFR}		–600	—	+600	ns
Input signal rise time	t_r		—	—	100	ns
Input signal fall time	t_f		—	—	100	ns

○ Output Timing Characteristics



V_{CC} = +5.0V ± 10%, V_{DDH} = +14.0 to +40.0V

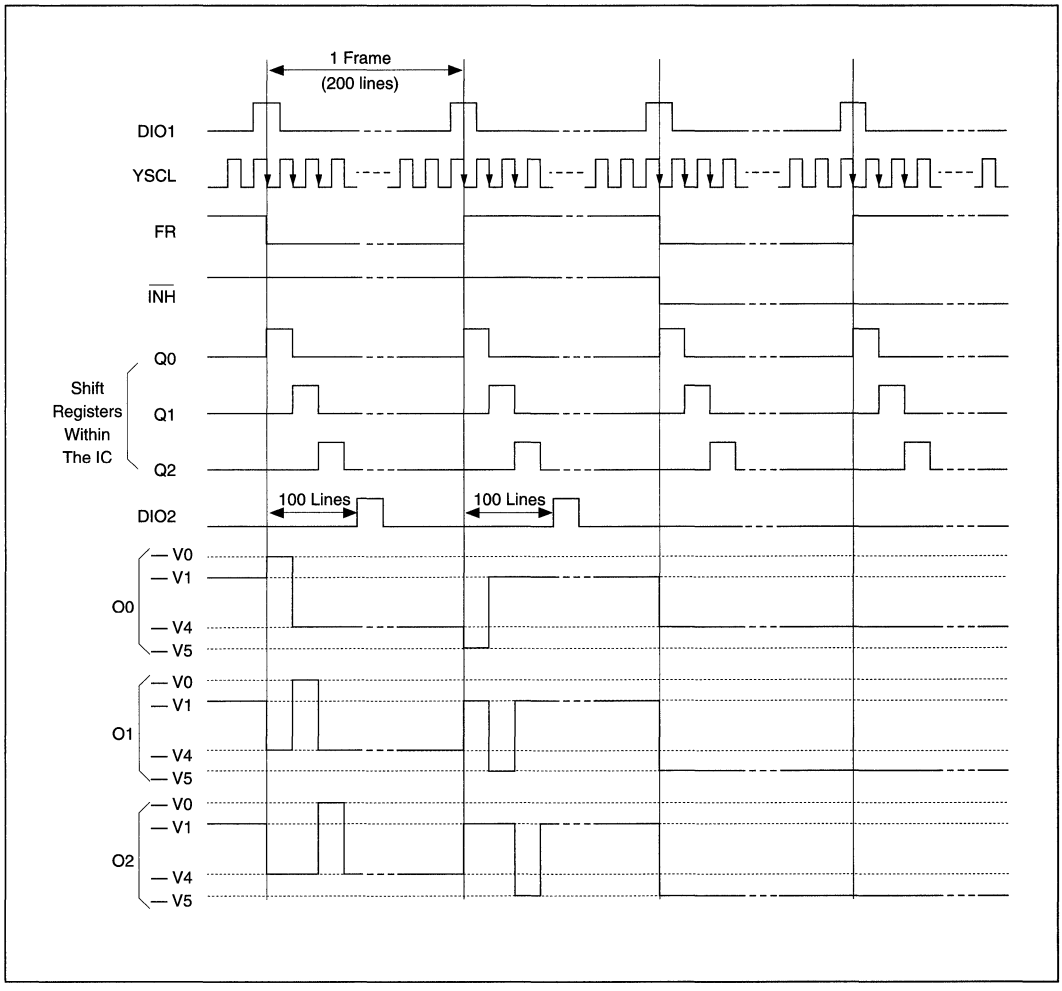
Parameter	Symbol	Condition	Min	Max	Unit
Output delay time from YSCL to DIO	t_{pdDOCL}	CL = 15pF	—	300	ns
Output delay time from YSCL to COM	t_{pdCCL}	V_{DDH} = +14.0 to +40.0V, CL = 100pF	—	700	ns
Output delay time from $\overline{INH}$ to COM	t_{pdCINH}		—	700	ns
Output delay time from FR to COM	t_{pdCFR}		—	700	ns
Output delay time from IP1 to OP1	t_{d1}	CL = 15pF	—	4C2R2	ns
Output release time from IP1 to OP1	t_{dT1}		—	—	ns
Output delay time from IP2 to OP1	t_{d2}		—	100	ns
Output release time from IP2 to OP1	t_{dT2}		—	100	ns

V_{CC} = +3.0 to 4.5V, V_{DDH} = +14.0 to +28.0V

Parameter	Symbol	Condition	Min	Max	Unit
Output delay time from YSCL to DIO	t_{pdDOCL}	CL = 15pF	—	600	ns
Output delay time from YSCL to COM	t_{pdCCL}	V_{DDH} = +14.0 to +40.0V, CL = 100pF	—	1400	ns
Output delay time from $\overline{INH}$ to COM	t_{pdCINH}		—	1400	ns
Output delay time from FR to COM	t_{pdCFR}		—	1400	ns
Output delay time from IP1 to OP1	t_{d1}	CL = 15pF	—	4C2R2	ns
Output release time from IP1 to OP1	t_{dT1}		—	—	ns
Output delay time from IP2 to OP1	t_{d2}		—	200	ns
Output release time from IP2 to OP1	t_{dT2}		—	200	ns

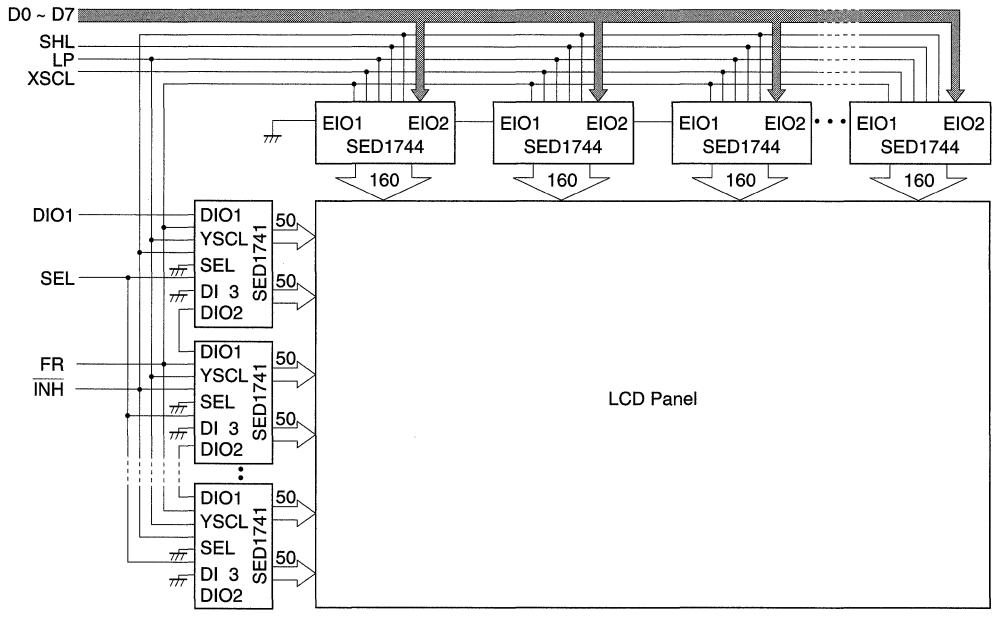
○ Timing Diagram

In this timing diagram, SHL = "L", and assumes a 1/200 duty cycle. (This diagram is provided only as a reference.)

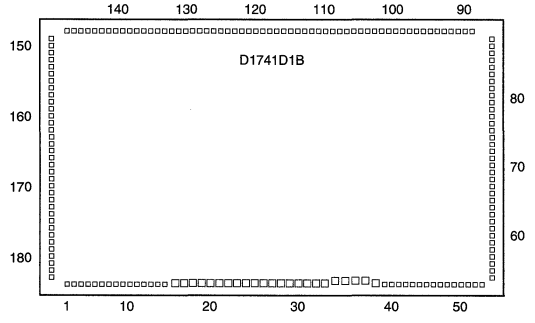


■ EXAMPLE OF APPLICATION

Large screen LCD schematic diagram



■ PAD LAYOUT



Chip Size	:	7.30 mm × 4.48 mm
Pad pitch	:	108 μm (Min.)
Chip thickness	:	525 μm ± 25μm

● **Au Bump (SED1741D1B) reference**

Au vertical bump
Parallel scribe × Vertical scribe ± Tolerance

Bump size A: 72μm × 93μm ± 4μm
(Pad Nos. 1 to 15, 39 to 183)

Bump size B: 93μm × 106μm ± 4μm
(Pad Nos. 16 to 33, 38)

Bump size C: 93μm × 93μm ± 4μm
(Pad Nos. 34 to 37)

Bump height: 17 to 28μm

● Pad Coordinates

Unit: μm

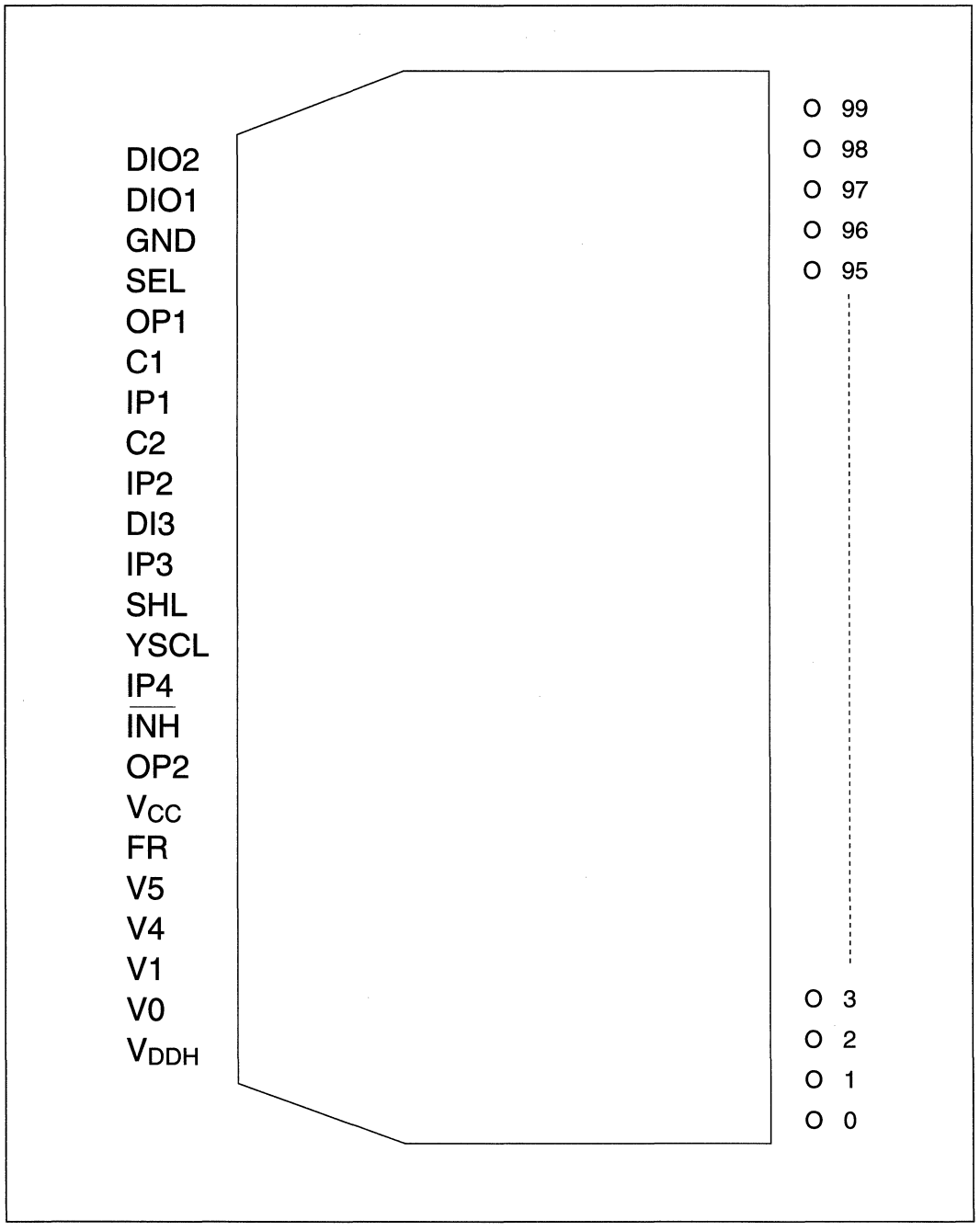
No.	Pin Name	X Coord.	Y Coord.
1	NC	–3228	–2064
2	NC	–3120	–2064
3	NC	–3012	–2064
4	NC	–2903	–2064
5	NC	–2795	–2064
6	NC	–2687	–2064
7	NC	–2578	–2064
8	NC	–2470	–2064
9	NC	–2362	–2064
10	NC	–2253	–2064
11	NC	–2145	–2064
12	NC	–2037	–2064
13	NC	–1929	–2064
14	NC	–1820	–2064
15	NC	–1712	–2064
16	DIO2	–1550	–2058
17	DIO1	–1417	–2058
18	GND	–1284	–2058
19	SEL	–1151	–2058
20	OP1	–1018	–2058
21	C1	–885	–2058
22	IP1	–752	–2058
23	C2	–619	–2058
24	IP2	–486	–2058
25	DI3	–353	–2058
26	IP3	–220	–2058
27	SHL	–87	–2058
28	YSCL	46	–2058
29	IP4	179	–2058
30	$\overline{INH}$	312	–2058
31	OP2	445	–2058
32	V_{CC}	578	–2058
33	FR	711	–2058
34	V5	872	–2026
35	V4	1034	–2026
36	V1	1195	–2026
37	V0	1357	–2026
38	V_{DDH}	1550	–2058
39	NC	1712	–2064
40	NC	1820	–2064
41	NC	1929	–2064
42	NC	2037	–2064
43	NC	2145	–2064
44	NC	2253	–2064
45	NC	2362	–2064
46	NC	2470	–2064
47	NC	2578	–2064
48	NC	2687	–2064
49	NC	2795	–2064
50	NC	2903	–2064

No.	Pin Name	X Coord.	Y Coord.
51	NC	3012	–2064
52	NC	3120	–2064
53	NC	3228	–2064
54	NC	3474	–1841
55	NC	3474	–1733
56	NC	3474	–1625
57	NC	3474	–1516
58	NC	3474	–1408
59	NC	3474	–1300
60	NC	3474	–1191
61	NC	3474	–1083
62	NC	3474	–975
63	NC	3474	–866
64	–NC	3474	–758
65	NC	3474	–650
66	NC	3474	–542
67	NC	3474	–433
68	NC	3474	–325
69	O0	3474	–217
70	O1	3474	–108
71	O2	3474	0
72	O3	3474	108
73	O4	3474	217
74	O5	3474	325
75	O6	3474	433
76	O7	3474	542
77	O8	3474	650
78	O9	3474	758
79	O10	3474	866
80	O11	3474	975
81	O12	3474	1083
82	O13	3474	1191
83	O14	3474	1300
84	O15	3474	1408
85	O16	3474	1516
86	O17	3474	1625
87	O18	3474	1733
88	O19	3474	1841
89	O20	3195	2064
90	O21	3087	2064
91	O22	2978	2064
92	O23	2870	2064
93	O24	2762	2064
94	O25	2653	2064
95	O26	2545	2064
96	O27	2437	2064
97	O28	2328	2064
98	O29	2220	2064
99	O30	2112	2064
100	O31	2004	2064

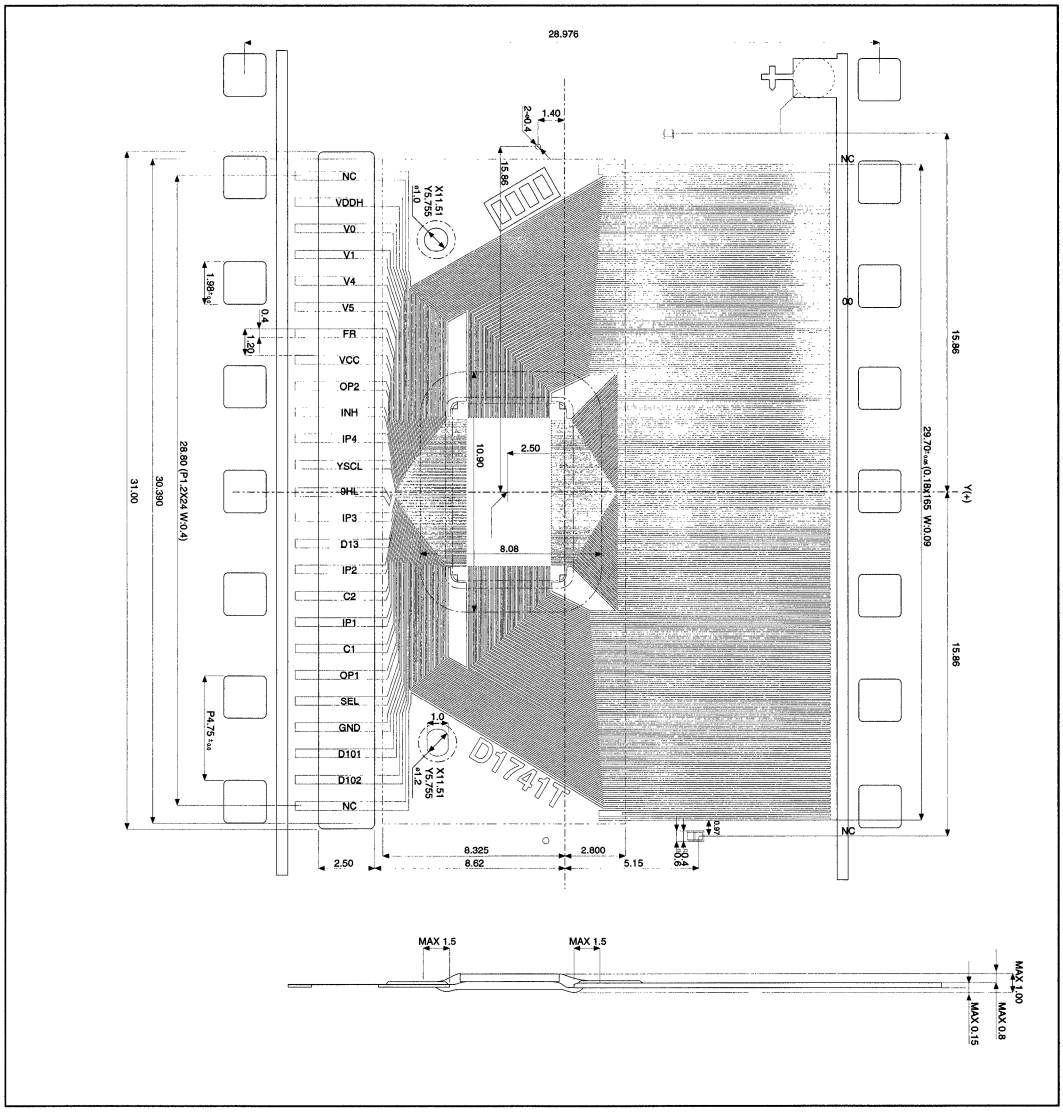
No.	Pin Name	X Coord.	Y Coord.
101	O32	1895	2064
102	O33	1787	2064
103	O34	1679	2064
104	O35	1570	2064
105	O36	1462	2064
106	O37	1354	2064
107	O38	1245	2064
108	O39	1137	2064
109	O40	1029	2064
110	O41	921	2064
111	O42	812	2064
112	O43	704	2064
113	O44	596	2064
114	O45	487	2064
115	O46	379	2064
116	O47	271	2064
117	O48	162	2064
118	O49	54	2064
119	O50	–54	2064
120	O51	–162	2064
121	O52	–271	2064
122	O53	–379	2064
123	O54	–487	2064
124	O55	–596	2064
125	O56	–704	2064
126	O57	–812	2064
127	O58	–921	2064
128	O59	–1029	2064
129	O60	–1137	2064
130	O61	–1245	2064
131	O62	–1354	2064
132	O63	–1462	2064
133	O64	–1570	2064
134	O65	–1679	2064
135	O66	–1787	2064
136	O67	–1895	2064
137	O68	–2004	2064
138	O69	–2112	2064
139	O70	–2220	2064
140	O71	–2328	2064
141	O72	–2437	2064
142	O73	–2545	2064
143	O74	–2653	2064
144	O75	–2762	2064
145	O76	–2870	2064
146	O77	–2978	2064
147	O78	–3087	2064
148	O79	–3195	2064
149	O80	–3474	1841
150	O81	–3474	1733

No.	Pin Name	X Coord.	Y Coord.
151	O82	–3474	1625
152	O83	–3474	1516
153	O84	–3474	1408
154	O85	–3474	1300
155	O86	–3474	1191
156	O87	–3474	1083
157	O88	–3474	975
158	O89	–3474	866
159	O90	–3474	758
160	O91	–3474	650
161	O92	–3474	542
162	O93	–3474	433
163	O94	–3474	325
164	O95	–3474	217
165	O96	–3474	108
166	O97	–3474	0
167	O98	–3474	–108
168	O99	–3474	–217
169	NC	–3474	–325
170	NC	–3474	–433
171	NC	–3474	–542
172	NC	–3474	–650
173	NC	–3474	–758
174	NC	–3474	–866
175	NC	–3474	–975
176	NC	–3474	–1083
177	NC	–3474	–1191
178	NC	–3474	–1300
179	NC	–3474	–1408
180	NC	–3474	–1516
181	NC	–3474	–1625
182	NC	–3474	–1733
183	NC	–3474	–1841

■ TAB LAYOUT


DIO2
DIO1
GND
SEL
OP1
C1
IP1
C2
IP2
DI3
IP3
SHL
YSCL
IP4
INH
OP2
VCC
FR
V5
V4
V1
V0
VDDH
O 99
O 98
O 97
O 96
O 95
O 3
O 2
O 1
O 0

■ EXTERNAL DIMENSIONS



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- **CMOS 160-bit LCD Common Driver**
- **Low Power**

■ DESCRIPTION

The SED1743 is an LCD common driver for high-resolution dot-matrix panels, which incorporates 160 row driver outputs. It is designed for use in conjunction with the SED1742 and SED1744 column drivers.

The SED1743 features a wide range of LCD drive voltages. The upper and lower drive voltages, V_0 and V_5 are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. As a result, the SED1743 is compatible with a large range of LCD panels.

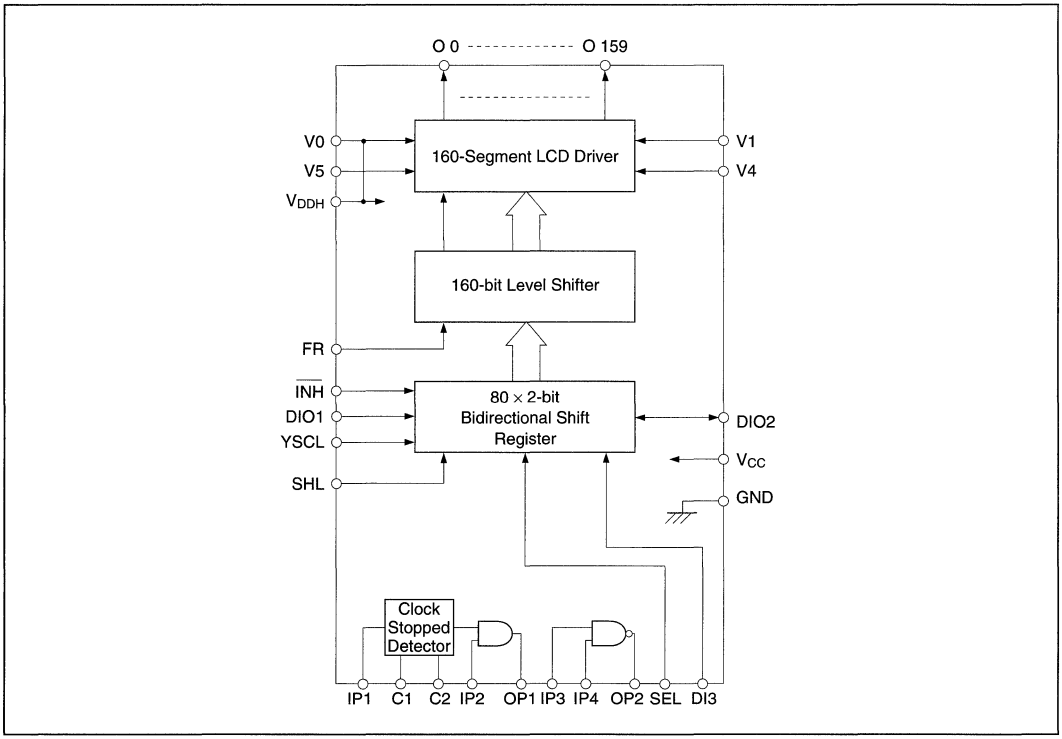
The SED1743 uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1743 operates from a 2.7 to 5.5V supply and is available in both chip packages and tape-carrier packages (TCPs).

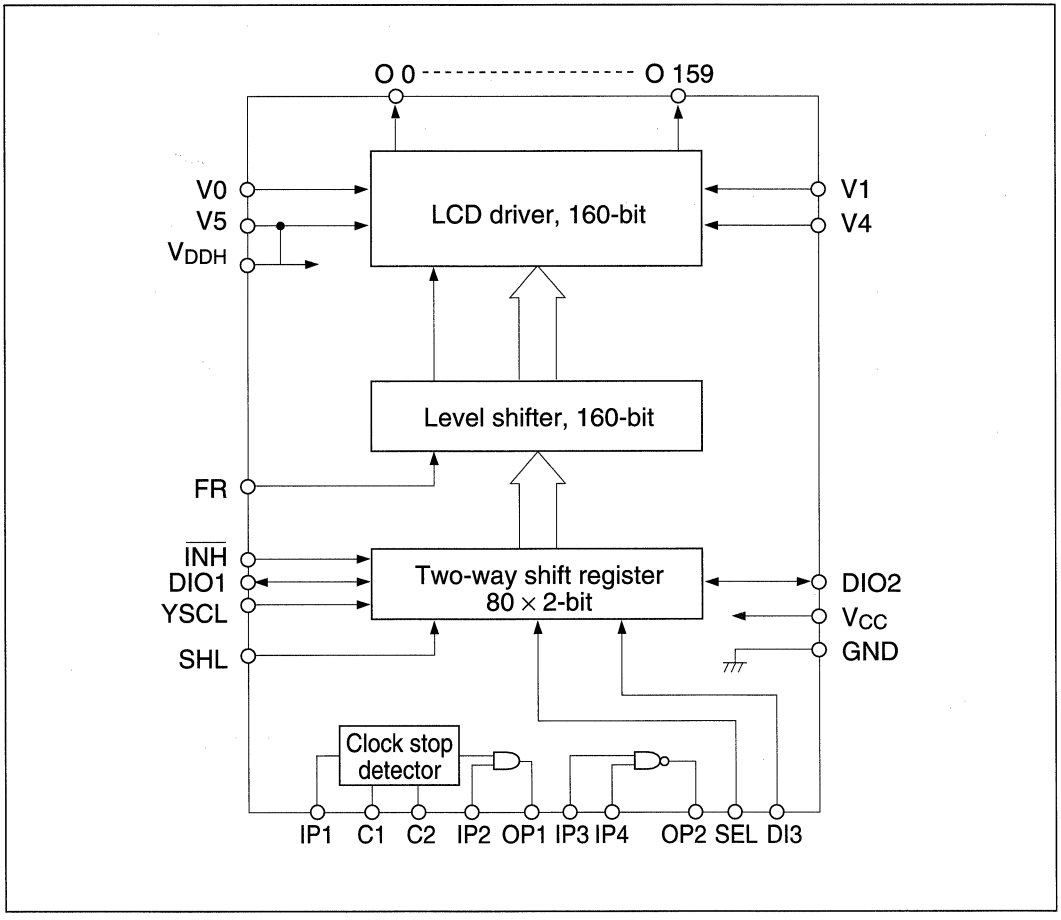
■ FEATURES

- 160 (80 × 2) LCD common drive outputs
- Pin-selectable output shift direction
- Adjustable LCD drive voltages
- Duty cycles up to 1/480
- Zero-bias display disable function
- Silicon-gate CMOS technology
- 1 kΩ typical output impedance
- 14 to 40V LCD drive voltages
- 2.7 to 5.5V supply
- Chip (SED1743D$_{1B}$) or tape-carrier (SED1743T$_{0A}$) packages

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



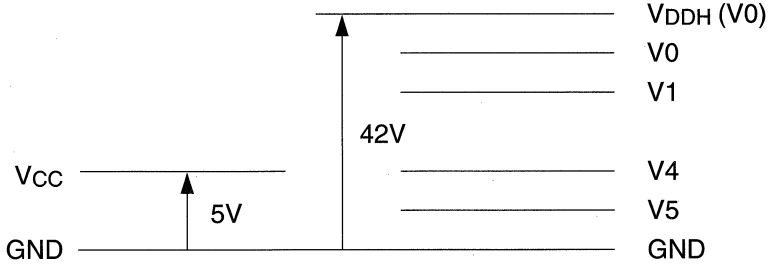
■ PIN DESCRIPTION

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Q'ty</th></tr>
<tr><td>O0 to 159</td><td>O</td><td>Common (row) output for liquid crystal display</td><td>160</td></tr>
<tr><td>DIO2
DIO1</td><td>I/O</td><td>DI01 ans DI02 are data onput/output to a bi-directional shift register; either one can be selected as input or output by setting. 80 × 2-bit two-way shift register scan pulse SHL input sets the terminal to input or output. The output varies at the YSCL trailing edge. The DI3 is the input terminal of the scan pulse when 80 × 2 configuration is used.</td><td>3</td></tr>
<tr><td>SEL</td><td>I</td><td>Shift register mode selection input
H: 80 × 2 (DI3 input) L: 160, also connect DI3 = GND</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input; negative edge triggered</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select input
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">O (Output shift direction)</th><th colspan="2">DIO</th></tr>
<tr><th>DIO1</th><th>DIO2</th></tr>
<tr><td>L</td><td>0 ⟶ 159</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>159 ⟶ 0</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Common drive signal polarity select input</td><td>1</td></tr>
<tr><td>VCC, GND</td><td>Power Source</td><td>Logic power source. GND: 0 V; VCC: +3 V, +5 V</td><td>2</td></tr>
<tr><td>V5, V4, V1, V0 and VDDH</td><td>Power Source</td><td>Liquid crystal drive power source GND: 0 V; VDDH: 8V to 42V
VDDH (V0) ≥ V1 ≥ 8/9 VDDH, 1/9 VDDH ≥ V4 ≥ V5 ≥ GND</td><td>5</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Display blanking input
Low-level input sets all the common outputs to V5 level.</td><td>1</td></tr>
<tr><td>IP1</td><td>I</td><td>Stop detector clock input</td><td>1</td></tr>
<tr><td>IP2</td><td>I</td><td>Signal input to be AND-ed with the stop detect output, equipped with internal pull-down resistor</td><td>1</td></tr>
<tr><td>C1</td><td>O</td><td>1st charge hold terminal, Capacitor externally mounted between GND</td><td>1</td></tr>
<tr><td>C2</td><td>O</td><td>2nd charge hold terminal, Capacitor and resistor externally mounted between GND</td><td>1</td></tr>
<tr><td>OP1</td><td>O</td><td>Clock stop detector output</td><td>1</td></tr>
<tr><td>IP3</td><td>I</td><td>NAND gate input internal pull-down resistor</td><td>1</td></tr>
<tr><td>IP4</td><td>I</td><td>NAND gate input</td><td>1</td></tr>
<tr><td>OP2</td><td>O</td><td>NAND gate output</td><td>1</td></tr>
<tr><td>DI3</td><td>I</td><td>Scan pulse input when 2 × 80 mode</td><td>1</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage for LCD	V_{DDH}	–0.3 to +45.0	V
Supply voltage for LCD (3)	V0, V1, V4, V5	GND –0.3 to V_{DDH} +0.3	V
Input voltage (4)	V_I	GND –0.3 to V_{CC} +0.3	V
Output voltage	V_O	GND –0.3 to V_{CC} +0.3	V
EIO output current	I_{O1}	20	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature 1 (2)	$T_{stg\,1}$	–65 to +150	°C
Storage temperature 2 (2)	$T_{stg\,2}$	–55 to +100	°C



Notes: 1. The voltage is based at GND = 0 V.
2. The storage temperature 1 is specified for a single chip and the storage temperature 2 is for TCP mounting.
3. Voltage V0, V1 and V4 should satisfy the condition: V_{DDH} (V0) ≥ V1 ≥ V4 ≥ V5 ≥ GND.
4. **CAUTION**: The LSI may be externally broken if the logic system power source floats or decreases below V_{CC}=2.6 V while voltage is applied to the liquid crystal drive system power source. Special care should betaken for the power source sequence when turning the system power on and off.

● Recommended Operating Conditions

T_a = 25°C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	5	V
Segment driver supply voltage range	V_{DDH}	14 to 40	V

T_a = 25°C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	3	V
Segment driver supply voltage range	V_{DDH}	14 to 28	V

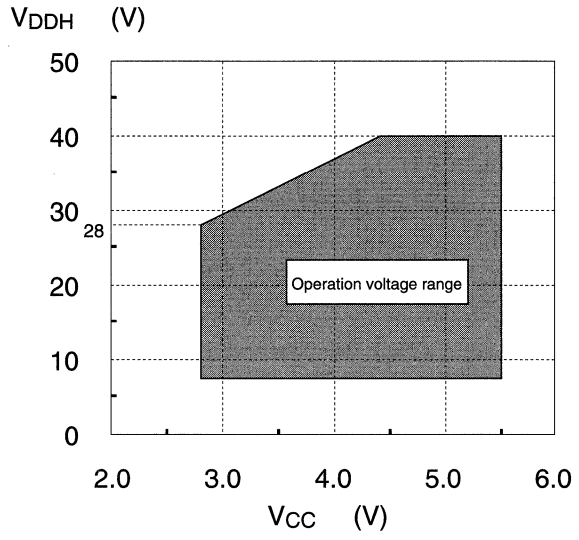
● DC Electrical Characteristics

(Unless otherwise specified, GND=V5=0V, V_{CC}= +5.0V ±10%, T_a= –20 to 75°C)

Parameter	Symbol	Condition		Terminal	Min	Typ	Max	Unit
Logic supply voltage (1)	V_{CC}			V_{CC}	2.7	5.0	5.5	V
Operation voltage recommended	V_{DDH}			V_{DDH}	8.0	—	42	V
Common driver supply voltage	V_{DDH} (V0)	Function		V_{DDH}	8.0	—	42	V
Common driver supply voltage	V1	Value recommended		V1	8/9V_{DDH}	—	—	V
Common driver supply voltage	V4, V5	Value recommended		V4	GND	—	1/9V_{DDH}	V
High level input voltage	V_{IH}	V_{CC} = 3.0 to 5.5 V		DIO1, DIO2, DI3, IP1 to 4, SEL, FR, YSCL, SHL, $\overline{INH}$	0.8V_{CC}	—	—	V
Low level input voltage	V_{IL}				—	—	0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC} = 3 to 5.5 V	I_{OH} = –0.3 mA	DIO1, DIO2	V_{CC} –0.4	—	—	V
Low level output voltage	V_{OL}		I_{OL} = 0.3 mA	OP1, OP2	—	—	0.4	V
Low–level input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		DI3, SEL, FR, YSCL, SHL, $\overline{INH}$	—	—	2.0	µA
High-level input leakage current	I_{IH}	V_{IN} ≤ V_{CC}		IP2, IP3	40	80	180	µA
Input/Output leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		DIO1, DIO2	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 to 40.0 V V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Output resistance	R_{COM}	ΔVON = 0.5V condition recommended	V_{DDH}=+30.0V	O0 to O159	—	0.65	2.0	kΩ
			V_{DDH}=+20.0V		—	0.7	2.1	
Average operation current consumed (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} =33.6 kHz, f_{FR} =70 Hz; Input data: 1/480, No load		V_{CC}	—	9	20	µA
		V_{CC} = +3.0 V Other condition: Same as V_{CC} = 5V			—	6	10	
Average operation current consumed (2)	I_{DDH}	V_{DDH} = V0 = +30.0 V, V1 = +28.0 V, V4 = +2.0 V, V5 = +0.0 V, V_{CC} = +5.0 V; Other condition: same as I_{CC}		V_{DDH}	—	4	25	µA
Input capacitance	C_I	Freq.=1 MHz, T_a = 25°C Single chip		DI3, IP1 TO 4, SEL, FR, YSCL, SHL, $\overline{INH}$	—	—	8	pF
I/O terminal capacity	$C_{I/O}$			DIO1, DIO2	—	—	15	pF

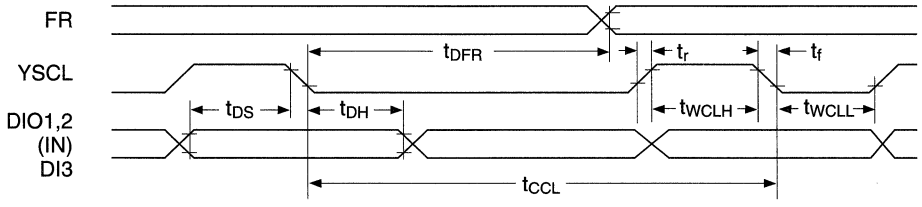
● **Operation Voltage Range V_{CC}–V_{DDH}**

The maximum LCD supply voltage, V_{DDH}, depends on V_{CC} as shown in the following figure. Specify the V_{DDH} voltage within the V_{CC}–V_{DDH} operation.



● **AC Electrical Characteristics**

○ **Input Timing Characteristics**



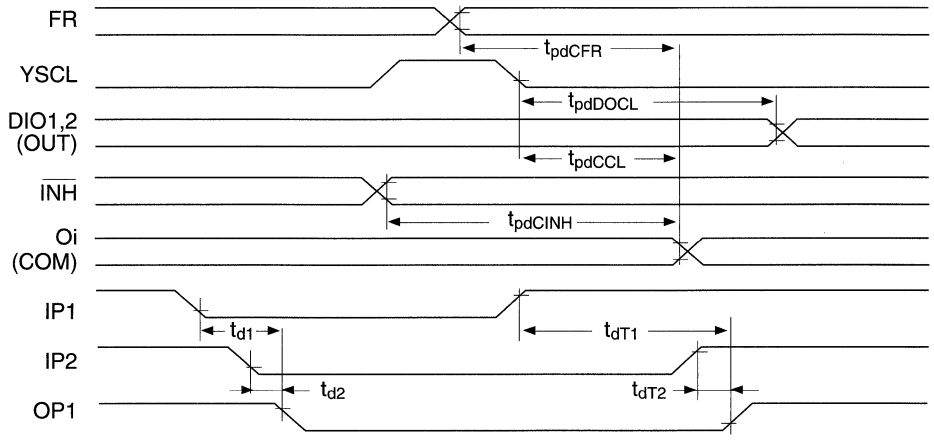
(V_{CC} = 5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL cycle	t_{CCL}		400	—	—	ns
YSCL high-level pulse width	t_{WCLH}		60	—	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		40	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
FR delay allowance time	t_{DFR}		–300	—	+300	ns
Input signal rise time	t_r		—	—	50	ns
Input signal breaking time	t_f		—	—	50	ns

(V_{CC} = 3.0 to 4.5 V, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL cycle	t_{CCL}		800	—	—	ns
YSCL high-level pulse width	t_{WCLH}		80	—	—	ns
YSCL low-level pulse width	t_{WCLL}		660	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		50	—	—	ns
FR delay allowance time	t_{DFR}		–400	—	400	ns
Input signal rise time	t_r		—	—	100	ns
Input signal breaking time	t_f		—	—	100	ns

○ Output Timing Characteristics



(V_{CC} = +5.0 V ±10%, V_{DDH} = 40.0 V)

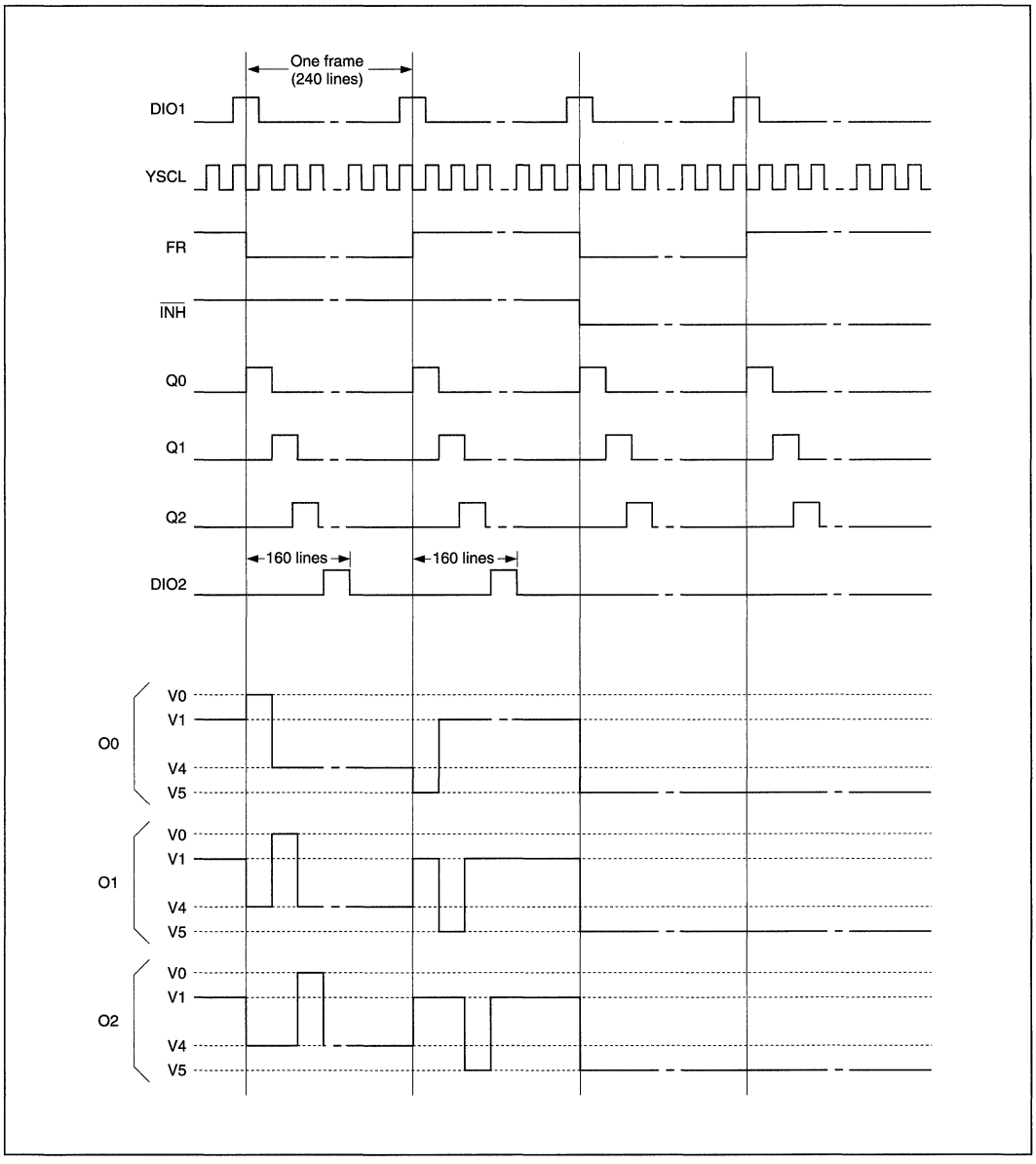
Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL → DIO output delay time	t_{pdDOCL}	C_L = 15 pF	—	—	100	ns
YSCL → COM output delay time	t_{pdCCL}	V_{DDH} = 14.0 to 40.0 V C_L = 100 pF	—	—	160	ns
$\overline{INH}$ → COM output delay time	t_{pdCINH}		—	—	160	ns
FR → COM output delay time	t_{pdCFR}		—	—	160	ns
IP1 → OP1 output delay time	t_{d1}	C_L = 15 pF	—	—	4C2R2	ns
IP1 → OP1 output release time	t_{dT1}		—	—	2 × YD cycle	ns
IP2 → OP1 output delay time	t_{d2}		—	—	100	ns
IP2 → OP1 output release time	t_{dT2}		—	—	100	ns

(V_{CC} = 3.0 to 4.5 V, V_{DDH} = 140.0 to 28.0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL → DIO output delay time	t_{pdDOCL}	C_L = 15 pF	—	—	200	ns
YSCL → COM output delay time	t_{pdCCL}	V_{DDH} = 14.0 to 40.0 V C_L = 100 pF	—	—	300	ns
$\overline{INH}$ → COM output delay time	t_{pdCINH}		—	—	300	ns
FR → COM output delay time	t_{pdCFR}		—	—	300	ns
IP1 → OP1 output delay time	t_{d1}	C_L = 15 pF	—	—	4C2R2	ns
IP1 → OP1 output release time	t_{dT1}		—	—	2 × YD cycle	ns
IP2 → OP1 output delay time	t_{d2}		—	—	200	ns
IP2 → OP1 output release time	t_{dT2}		—	—	200	ns

Note: YD: Scan Start Pulse
For C2R2, see 11. Clock stop detector circuit.

- **Timing Diagrams**
  - 1/240 Duty Cycle



■ FUNCTIONAL DESCRIPTION

● Shift Register

The shift register is a bi-directional shift register, where the shift direction is selected by SHL. The effect of SHL on the shift direction and on the input data sequence is shown in the following table.

Data Sequence and Shift Direction

SHL	LCD Outputs							Shift Direction	
	O159	O158	O157	...	O2	O1	O0	DIO1	DIO2
L	a	b	c	...	x	y	z	Input	Output
H	z	y	x	...	c	b	a	Output	Input

SEL is used to select the operating mode of the shift register. When SEL is HIGH, 2 × 80 mode is selected. When SEL is LOW, 1 × 160 mode is selected.

● Level Shifter

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

● LCD Drivers

The LCD drivers generate the AC LCD drive waveforms. The output voltages are determined by the polarity of the FR signal, as shown in the following table.

Driver Output Voltage

$\overline{INH}$	Input Data	FR	Output Voltage
H	H	H	V5
		L	V0 (V_{DDH})
	L	H	V1
		L	V4
L	X	X	V5

X = don't care

■ APPLICATION NOTES

● Voltage Levels

The recommended method of generating the LCD drive voltages, V0 to V5, is with a voltage divider between V_{DDH} and V_{GND}, buffered with voltage followers.

The lower drive level, V5, is not necessarily at V_{GND}, and separate pins are used for the voltage levels when op-amps are used. A maximum voltage differential between V5 and V_{GND} of 2.5V is recommended since the driver efficiency decreases as the differential increases. Connect V5 to GND when not using op-amps.

The resistances of the voltage divider resistors should be as low as possible and within power supply constraints.

Note that fluctuations in I_{DDH} can cause dips in the V_{DDH} supply. The device will be damaged if the voltage dips below the point where the relationship V_{DDH} (V0) ≥ V1 ≥ V4 ≥ V5 ≥ V_{GND} breaks down. A stabilized power supply may be required when using the resistor network.

- **Clock Monitor**

The LCD panel can be damaged if a DC signal is applied to the segments. This situation can occur when the AC drive clock stops while power is applied to the display. The clock monitor circuit detects this condition and sends OP1 LOW. If OP1 is connected to INH, the display is protected from damage.

- **Power-Up and Power-Down Precautions**

As the driver circuitry operates at high voltage, care should be taken when applying and removing power to the SED1743 to prevent damage. If the driver supply is applied when the logic supply is either not connected or below 2.9V, excess current will flow into the SED1742 and damage the device. Normal operation is guaranteed if the correct power-up and power-down sequences are followed.

Power-Up Sequence:

Power should be applied to Vcc before, or at the same time as, power is applied to the driver circuitry.

Power-Down Sequence:

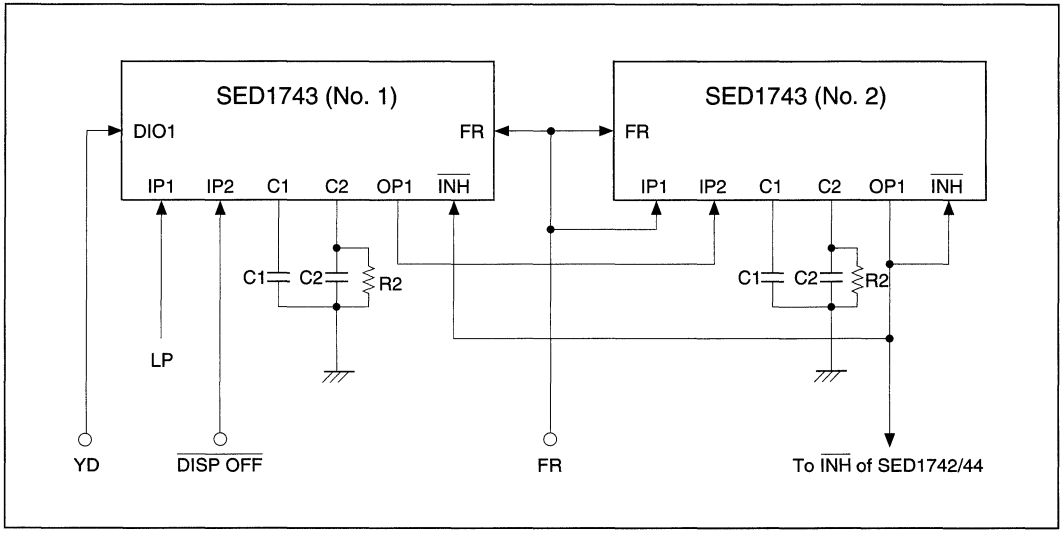
Power should be removed from Vcc after, or at the same time as, power is removed from the driver circuitry.

The SED1743 can also be damaged if the LCD output drivers start operating before the driver supplies stabilize. $\overline{INH}$ should be held LOW to hold the driver outputs at V5 until the driver supplies have stabilized.

As an additional protective measure, insert a fast-blow fuse in series with the driver supply.

- **Clock Monitor Circuit**

The clock monitor circuit sets OP1 LOW whenever the clock signals from the controller stops. Connecting OP1 to $\overline{INH}$ ensures that DC does not flow into the LCD panel.



R2 is typically several MΩ and C1 and C2 are determined while monitoring OP1. C1 should be much larger than C2. Typical values under various signal conditions are shown in the following table.

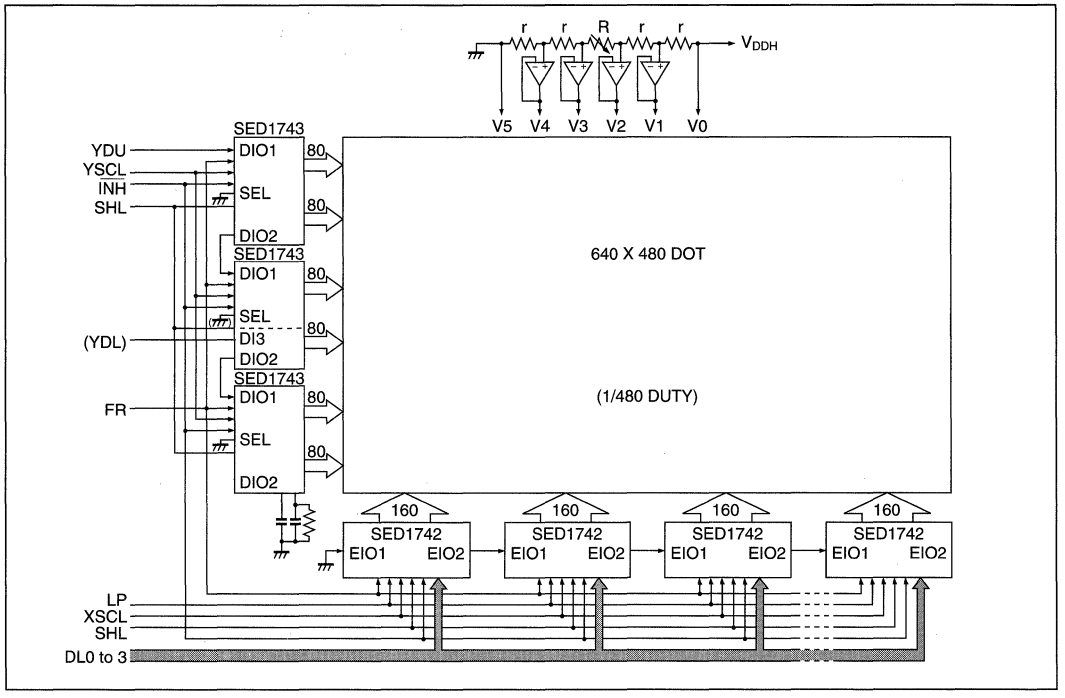
Input Signal	C1	C2	R2
LP = IP1	0.1 µF	.01 ~ .1µF	3.3 MΩ
FR = IP1	0.1 µF	.01 ~ .1µF	3.3 MΩ

Notes: YD: tc = 17.8 ms, duty = 0.14%
LP: tc = 40.4 ms, duty = 0.35%
FR: tc = 3.53 ms, duty = 50%

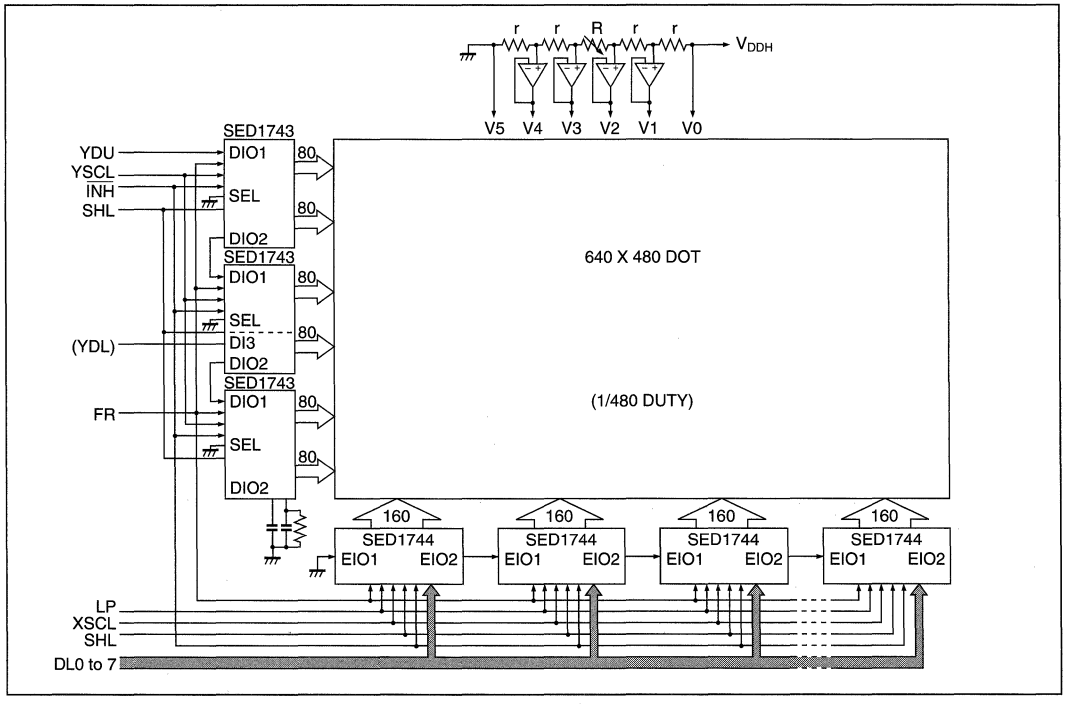
When the clock monitor feature is not required, tie IP1, IP2, IP3 and C2 LOW, and leave OP1, OP2 and C1 OPEN.

■ CIRCUIT DIAGRAM FOR REFERENCE

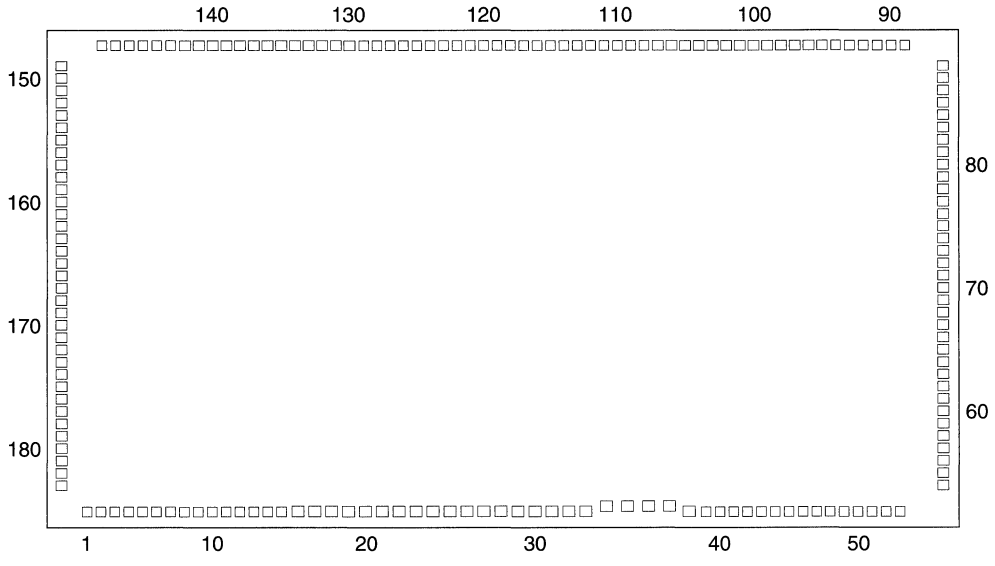
(Combination of SED1742 with SED1743)



(Combination of SED1744 with SED1743)



■ PAD LAYOUT FOR SED1742/3/4 (D_{1B} Version)



Chip Size ..... 7.30mm × 4.48mm
Pad Pitch ..... 108μm (Min.)
Chip Thickness ..... 525μm ± 25μm

1) Au Bump

Bump Size A	72μm × 93μm ± 4μm	(Pad Nos. 1~15, 39~183)
Bump Size B	93μm × 106μm ± 4μm	(Pad Nos. 16~33, 38)
Bump Size C	93μm × 93μm ± 4μm	(Pad Nos. 34~37)

Bump Height 17 ~ 28μm

■ PAD COORDINATES

Pad No.	Pin Name	X	Y
1	NC	–3228	–2064
2	NC	–3120	–2064
3	NC	–3012	–2064
4	NC	–2903	–2064
5	NC	–2795	–2064
6	NC	–2687	–2064
7	NC	–2578	–2064
8	NC	–2470	–2064
9	NC	–2362	–2064
10	NC	–2253	–2064
11	NC	–2145	–2064
12	NC	–2037	–2064
13	NC	–1929	–2064
14	NC	–1820	–2064
15	NC	–1712	–2064
16	DIO2	–1550	–2058
17	DIO1	–1417	–2058
18	GND	–1284	–2058
19	SEL	–1151	–2058
20	OP1	–1018	–2058
21	C1	–885	–2058
22	IP1	–752	–2058
23	C2	–619	–2058
24	IP2	–486	–2058
25	DI3	–353	–2058
26	IP3	–220	–2058
27	SHL	–87	–2058
28	YSCL	46	–2058
29	IP4	179	–2058
30	INH	312	–2058
31	OP2	445	–2058
32	VCC	578	–2058
33	FR	711	–2058
34	V5	872	–2026
35	V4	1034	–2026
36	V1	1195	–2026
37	V0	1357	–2026
38	VDDH	1550	–2058
39	NC	1712	–2064
40	NC	1820	–2064

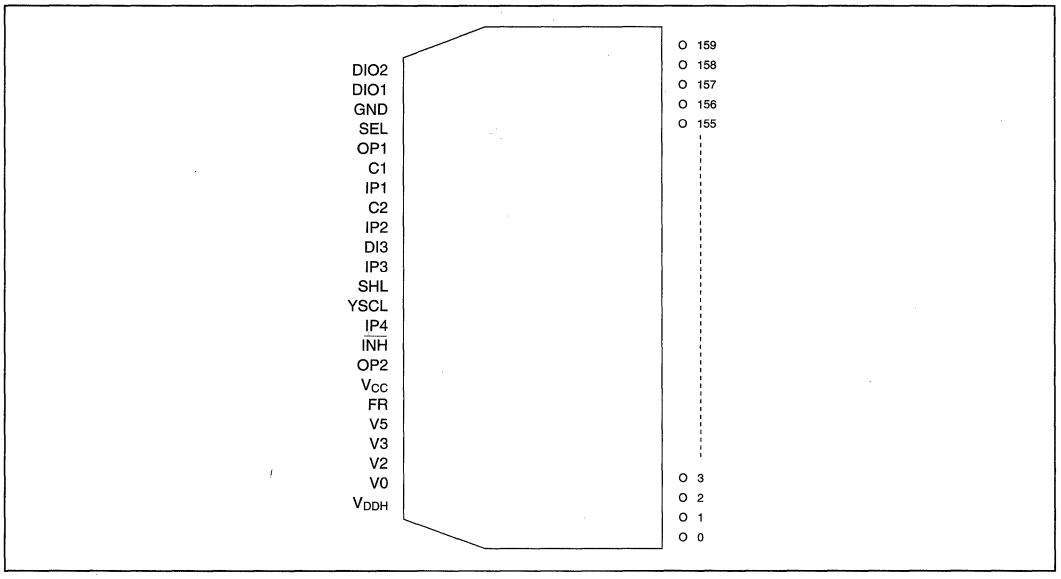
Pad No.	Pin Name	X	Y
41	NC	1929	–2064
42	NC	2037	–2064
43	NC	2145	–2064
44	NC	2253	–2064
45	NC	2362	–2064
46	NC	2470	–2064
47	NC	2578	–2064
48	NC	2687	–2064
49	NC	2795	–2064
50	NC	2903	–2064
51	NC	3012	–2064
52	NC	3120	–2064
53	NC	3228	–2064
54	NC	3474	–1841
55	NC	3474	–1733
56	NC	3474	–1625
57	NC	3474	–1516
58	NC	3474	–1408
59	NC	3474	–1300
60	NC	3474	–1191
61	NC	3474	–1083
62	NC	3474	–975
63	NC	3474	–866
64	NC	3474	–758
65	NC	3474	–650
66	NC	3474	–542
67	NC	3474	–433
68	NC	3474	–325
69	O0	3474	–217
70	O1	3474	–108
71	O2	3474	0
72	O3	3474	108
73	O4	3474	217
74	O5	3474	325
75	O6	3474	433
76	O7	3474	542
77	O8	3474	650
78	O9	3474	758
79	O10	3474	866
80	O11	3474	975

Pad No.	Pin Name	X	Y
81	O12	3474	1083
82	O13	3474	1191
83	O14	3474	1300
84	O15	3474	1408
85	O16	3474	1516
86	O17	3474	1625
87	O18	3474	1733
88	O19	3474	1841
89	O20	3195	2064
90	O21	3087	2064
91	O22	2978	2064
92	O23	2870	2064
93	O24	2762	2064
94	O25	2653	2064
95	O26	2545	2064
96	O27	2437	2064
97	O28	2328	2064
98	O29	2220	2064
99	O30	2112	2064
100	O31	2004	2064
101	O32	1895	2064
102	O33	1787	2064
103	O34	1679	2064
104	O35	1570	2064
105	O36	1462	2064
106	O37	1354	2064
107	O38	1245	2064
108	O39	1137	2064
109	O40	1029	2064
110	O41	921	2064
111	O42	812	2064
112	O43	704	2064
113	O44	596	2064
114	O45	487	2064
115	O46	379	2064
116	O47	271	2064
117	O48	162	2064
118	O49	54	2064
119	O50	–54	2064
120	O51	–162	2064

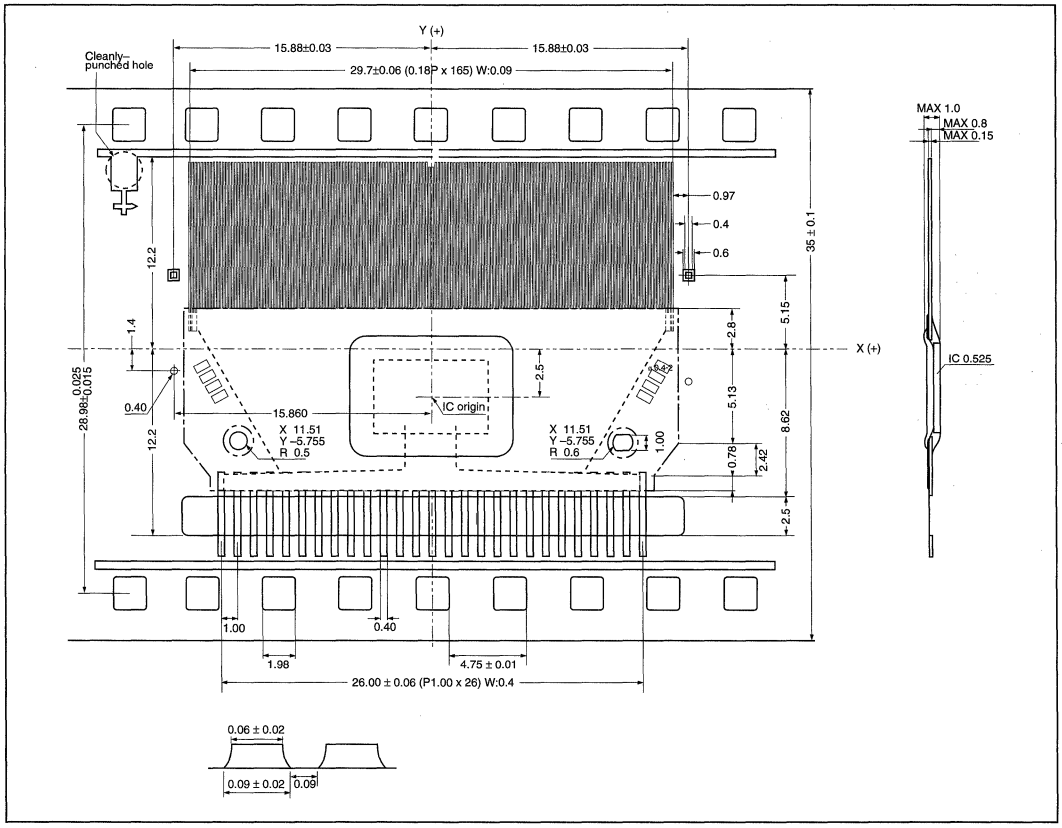
Pad No.	Pin Name	X	Y
121	O52	–271	2064
122	O53	–379	2064
123	O54	–487	2064
124	O55	–596	2064
125	O56	–704	2064
126	O57	–812	2064
127	O58	–921	2064
128	O59	–1029	2064
129	O60	–1137	2064
130	O61	–1245	2064
131	O62	–1354	2064
132	O63	–1462	2064
133	O64	–1570	2064
134	O65	–1679	2064
135	O66	–1787	2064
136	O67	–1895	2064
137	O68	–2004	2064
138	O69	–2112	2064
139	O70	–2220	2064
140	O71	–2328	2064
141	O72	–2437	2064
142	O73	–2545	2064
143	O74	–2653	2064
144	O75	–2762	2064
145	O76	–2870	2064
146	O77	–2978	2064
147	O78	–3087	2064
148	O79	–3195	2064
149	O80	–3474	1841
150	O81	–3474	1733
151	O82	–3474	1625
152	O83	–3474	1516
153	O84	–3474	1408
154	O85	–3474	1300
155	O86	–3474	1191
156	O87	–3474	1083
157	O88	–3474	975
158	O89	–3474	866
159	O90	–3474	758
160	O91	–3474	650

Pad No.	Pin Name	X	Y
161	O92	–3474	542
162	O93	–3474	433
163	O94	–3474	325
164	O95	–3474	217
165	O96	–3474	108
166	O97	–3474	0
167	O98	–3474	–108
168	O99	–3474	–217
169	NC	–3474	–325
170	NC	–3474	–433
171	NC	–3474	–542
172	NC	–3474	–650
173	NC	–3474	–758
174	NC	–3474	–866
175	NC	–3474	–975
176	NC	–3474	–1083
177	NC	–3474	–1191
178	NC	–3474	–1300
179	NC	–3474	–1408
180	NC	–3474	–1516
181	NC	–3474	–1625
182	NC	–3474	–1733
183	NC	–3474	–1841

■ TAPE CARRIER PACKAGE – PINOUT



■ TAPE CARRIER PACKAGE – DIMENSIONS



SED1753

CMOS LCD COMMON DRIVER

■ DESCRIPTION

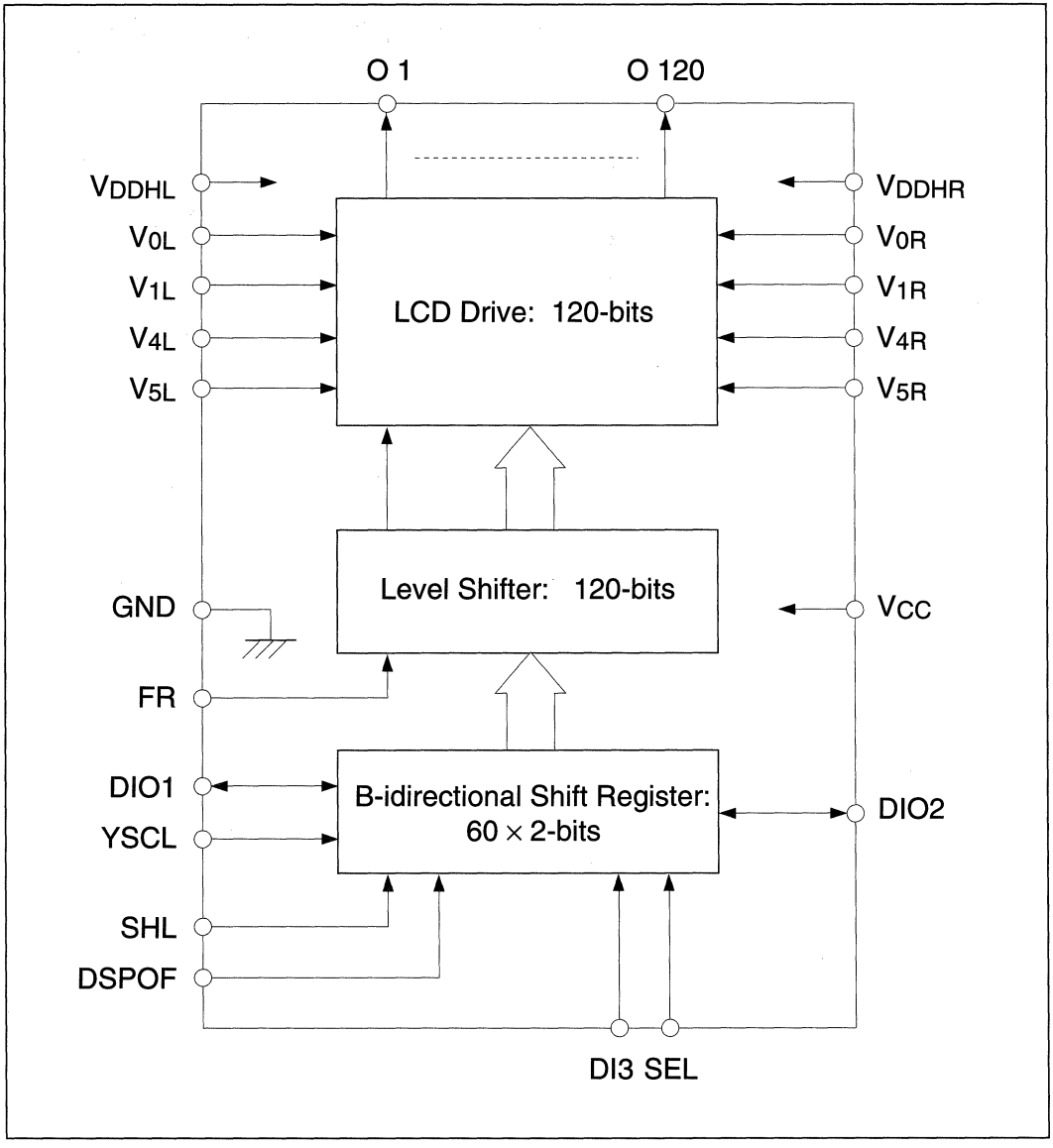
The SED1753 is an LCD common (row) driver designed for extremely high-capacity dot matrix liquid crystal panels. It incorporates 120 high-voltage, low-impedance common drivers in a 2 × 60 format, enabling high driver effectiveness with displays of 1/240, 1/300 and 1/480 duty cycles. It is designed for use in conjunction with the SED1752 and SED1758 segment (column) drivers.

The SED1753 features a wide range of liquid crystal drive voltages, an LCD display of high quality and slim configuration to minimize the LCD panel. It offers a wide range of applications.

■ FEATURES

- 120 (60 × 2) LCD common drive outputs
- 0.3KΩ (typ.) low output impedance
- High-duty drive available 1/480
- Pin-selectable output shift direction
- Zero-bias display disable function
- Slim configuration
- Adjustable LCD drive voltage
- Liquid crystal drive in wide range of voltage: 8 to 42V
- 2.7 to 5.5V supply
- Package:..... D0B ..... Au bump die
  T0A ..... TAB package

■ BLOCK DIAGRAM



■ FUNCTIONS

● Shift Register

This is a bi-directional shift register for transmitting common data. The shift register has a 60 × 2 bit structure, and a 60 × 2 bit or 120-bit structure can be selected depending on the state of SEL.

When a 60 × 2 bit structure is selected, the lower-stage 60-bit shift register input becomes DI3.

● Level Shifter

This is a voltage level interface circuit for converting the signal voltage level from a logic-system level to an LCD drive-system level.

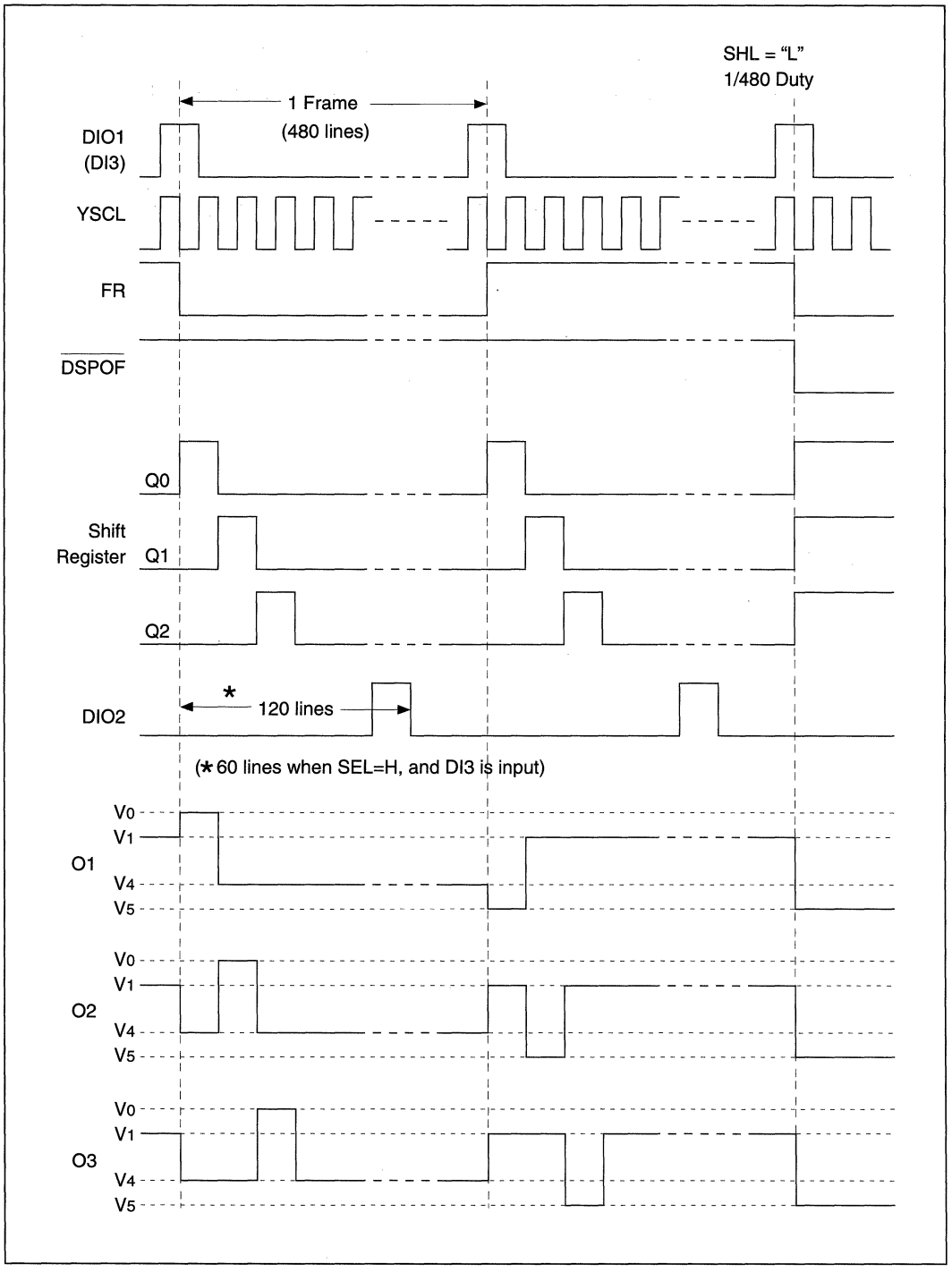
● LCD Driver

These output the LCD driver voltages.

The relationship between the display blanking signal $\overline{DSPOF}$, the contents of the shift register, the alternating signal FR, and the common output voltage is as shown below:

$\overline{DSPOF}$	Contents of Shift Register	FR	ON Output Voltage	
H	H	H	V_5	(Selected level)
		L	V_0	
	L	H	V_1	(Non-selected level)
		L	V_4	
L	—	—	V_5	—

■ TIMING CHART



■ EXPLANATION OF TERMINALS

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>No. of Terminals</th></tr>
<tr><td>O 1 to
O 120</td><td>O</td><td>LCD drive common (row) output.
Changes on the falling edge of YSCL</td><td>120</td></tr>
<tr><td>DIO1
DIO2</td><td>I/O</td><td>Set to input or to output by the scanning pulse SHL Input
of the 60 x 2 bit bi-directional shift register.
The output changes on the falling edge of YSCL</td><td>2</td></tr>
<tr><td>DI3</td><td>I</td><td>DI3 is a scan pulse input when a 60 x 2 structure is used.
When SEL = L, DI3 is connected to ground.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Bi-directional shift register operating mode select input.
H: 60 x 2 (DI3 input); L: 120</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input.
The scan data is shifted with the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and DIO terminal input/output
control output
<table>
<tr><th>SHL</th><th>0 Ouput Shift Direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>H</td><td>1 → 60 61 → 120</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>120 → 61 60 → 1</td><td>Output</td><td>Input</td></tr>
</table></td><td></td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>LCD display blanking control input.
When “L”, all common outputs are set to the V5 level.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output alternating signal input.</td><td>1</td></tr>
<tr><td>GND, V_{CC}</td><td>Power supply</td><td>Power supply for logic: GND: 0V V_{CC} + 2.7 to 5.5V</td><td>2</td></tr>
<tr><td>V_{OL}, V_{IL}, V_{4L},
V_{5L}, V_{DDH},
V_{OR}, V_{1R}, V_{4R},
V_{5R}, V_{DDHR},</td><td>Power supply</td><td>Power supply LCD drive
GND: 0V, V_{DDH}: 8V to 42V
$V_{DDH} \geq V0 \geq 8/9V_{DDH}$
$1/9V_{DDH} \leq V4 \geq V5 \geq GND$
*1</td><td>10</td></tr>
<tr><td></td><td></td><td>Total</td><td>140 pins</td></tr>
</table>

*1. V_{DDH} and V_0 to V_5 pairs must be connected to their respective LC power supplies. The LC drive circuit power supply voltage ranges are specification recommended values.

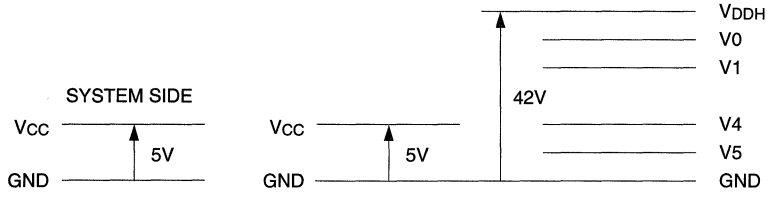
■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Rating

Parameters	Symbol	Rating	Units
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Power supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Power supply voltage (3)	V_0, V_1, V_4, V_5	GND – 0.3 to V_{DDH} +0.3	V
Input voltage	V_I	GND – 0.3 to V_{CC} +0.3	V
Output voltage	V_O	GND – 0.3 to V_{CC} +0.3	V
DIO output current	I_{O1}	20	mA
Operating temperature	Topr	–40 to +85	°C
Chip storage temperature	Tstg[1]	–65 to +150	°C
TCP product storage temperature	Tstg[2]	–55 to +125	°C

Note 1. All the above voltages are based on GND = 0V.

Note 2. V_0, V_1, V_4 and V_5 voltages must always fulfill the following relationship: $V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq GND$



Note 3. Permanent damage to the LSI may result if the logic power supply is floating or falls below V_{CC} = 2.6V when the LCD drive power supply is supplied. Special caution is required during the System Power OFF and System Power ON sequencing.

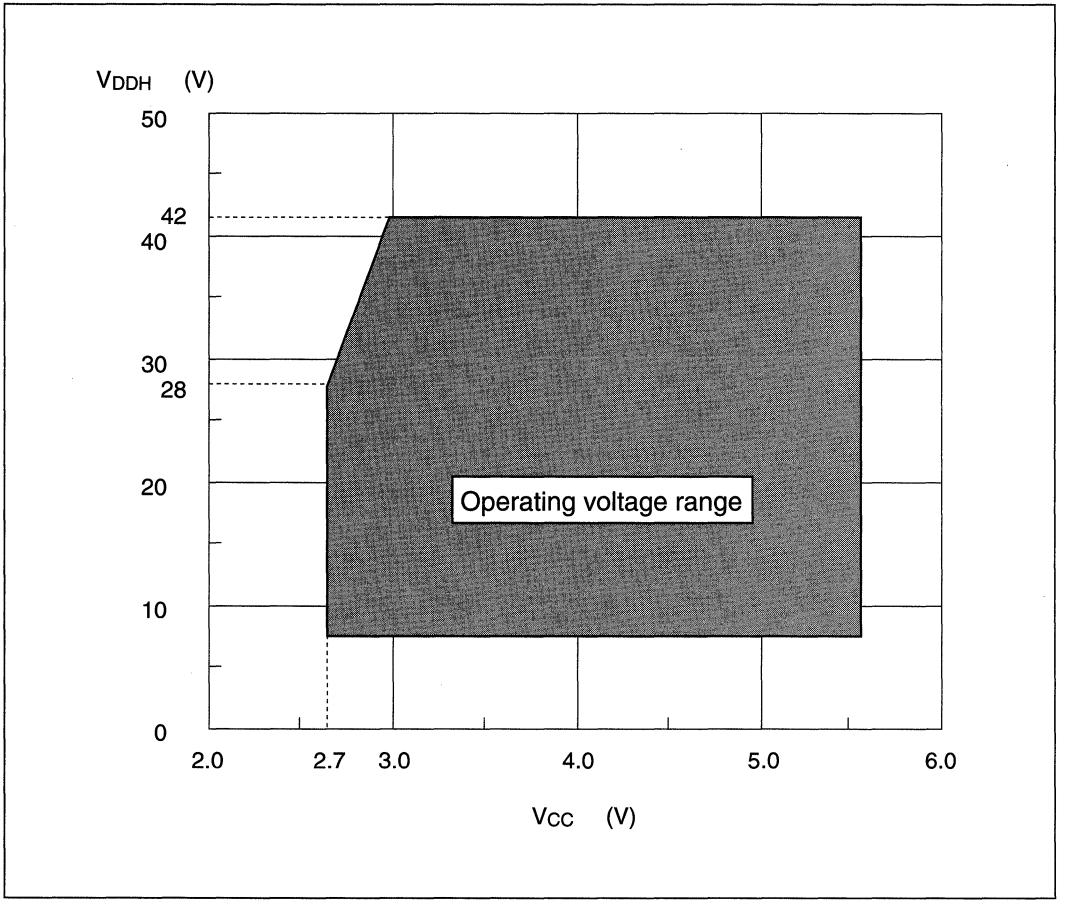
● DC Characteristics

Unless otherwise designated, GND = V_5 = 0V, V_{CC} = 5.0V ± 10%, T_a = −40 to 85°C

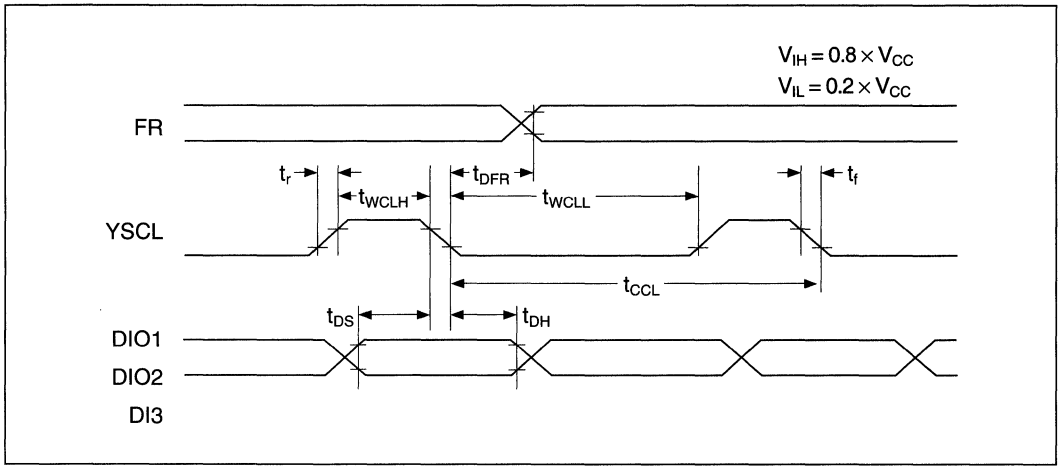
Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
Electrical voltage (1)	V_{CC}	—	V_{CC}	2.7	5.0	5.5	V
Recommended working voltage	V_{DDH}	V_{CC} = 2.7 to 5.5 V	V_{DDHL}, V_{DDHL}	14.0	—	40.0	V
Possible operating voltage	V_{DDH}	Function	V_{0L}, V_{OR}	8.0	—	42.0	V
Power supply voltage (2)	V_1	Recommended value	V_1L, V_1R	8/9 V_{DDH}	—	V_{DDH}	V
Power supply voltage (3)	V_4	Recommended value	V_4L, V_4R	GND	—	1/9 V_{DDH}	V
High level input voltage	V_{IH}	V_{CC}= 2.7~ 5.5V	DIO1,DIO2, FR	0.8 V_{CC}	—	—	V
Low level input voltage	V_{IL}	V_{CC}= 2.7~ 5.5V	YSCL, SHL, DI3 $\overline{DSPOF}$, SEL	—	—	0.2 V_{CC}	V
High level output voltage	V_{OH}	V_{CC} = 2.7~5.5V, I_{OH} = −0.3mA	EIO1, EIO2,	V_{CC}−0.4	—	—	V
Low level output voltage	V_{OL}	V_{CC} = 2.7~5.5V, I_{OL} = 0.3mA	EIO1, EIO2,	—	—	GND+0.4	V
Input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	YSCL, SHL, DI3 $\overline{DSPOF}$, FR, SEL	—	—	2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}	EIO1, EIO2	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 ~ 42.0V, V_{IH} = V_{CC}, V_{IL} = GND	GND	—	—	25	µA
Output resistance	R_{COM}	ΔVON = 0.5V, V_{DDH} = +36.0V, 1/24	O1~ O120	—	0.29	0.48	KΩ
		Ta = 25°C, V_{DDH} = +26.0V, 1/20	O1~ O120	—	0.3	0.5	KΩ
Resistance chip-internal BIOS	ΔR_{COM}	V_{DDH} = +36.0V, 1/24	O1~ O120	—	—	50	Ω
Average operating current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} = GND, f_{YSCL} = 33.6KHz, f_{LP} = 70Hz, Input data: 1/480, Ta = 25°C No load	V_{CC}	—	TBD	TBD	µA
		V_{CC} = +3.0V, All other conditons are the same as with V_{CC} = −5.0V	V_{CC}	—	TBD	TBD	µA
Average operating current consumption (2)	I_{DDH}	V_{DDH} = V_0 = 30.0V V_1 = 28.0V, V_4 = 2.0V, V_5 = 0.0V, V_{CC} = 5.0V, Other conditions are the same as with the item I_{CC}.	V_{DDHL}, V_{DDHR}	—	TBD	TBD	µA
Input terminal capacity	CI	Freq. = 1 MHz, Ta = 25°C, Chips alone	YSCL, SHL, $\overline{DSPOF}$, FR, DI3, SEL	—	—	8	pF
I/O terminal capacity	$C_{I/O}$	Freq. = 1 MHz, Ta = 25°C, Chips alone	DIO1, DIO2	—	—	15	pF

- **Range of Operating Voltages: V_{CC} – V_{DDH}**

  It is necessary to set the voltage for V_{DDH} within the V_{CC} – V_{DDH} operating voltage range shown in the diagram below.



- **AC Characteristics**
  - **Input Timing Characteristics**



V_{CC} = +5.0V ± 10%, T_a = –40 to 85°C

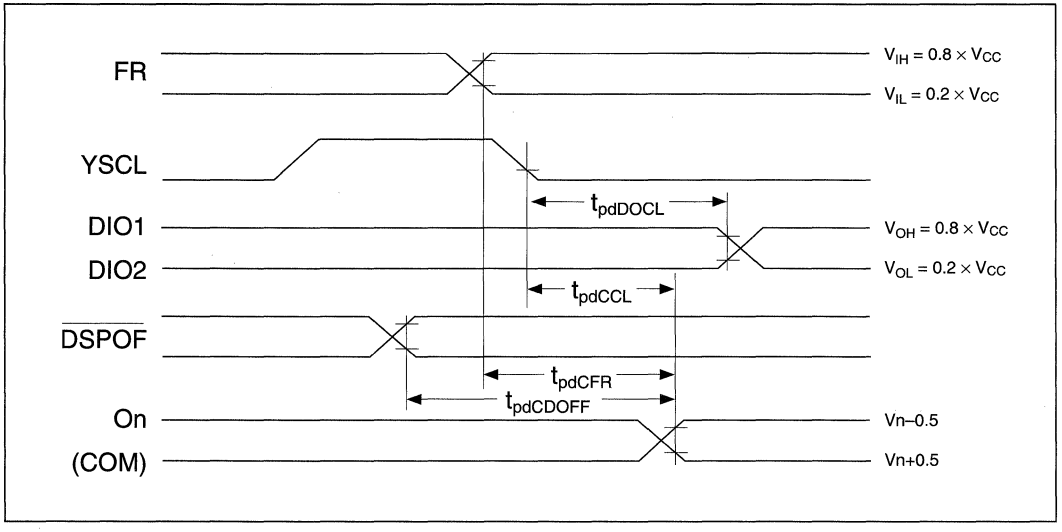
Parameter	Symbol	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	—	400	—	ns
YSCL high level pulse duration	t_{WCLH}	—	60	—	ns
YSCL low level pulse duration	t_{WCLL}	—	330	—	ns
Data setup time	t_{DS}	—	50	—	ns
Data hold time	t_{DH}	—	40	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns

V_{CC} = 2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	—	800	—	ns
YSCL high level pulse duration	t_{WCLH}	—	80	—	ns
YSCL low level pulse duration	t_{WCLL}	—	660	—	ns
Data setup time	t_{DS}	—	90	—	ns
Data hold time	t_{DH}	—	70	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns

Note: *1. The timing for the FR signal transition point (t_{DFR}: FR) and the LP signal falling edge is, essentially, 0 ns; set these in a range where the ON output wave form is not distorted.

○ **Output Timing Characteristics**



V_{CC} = 5.0V ± 10%, V_{DDH} = 14.0 to 42.0V, ta = –40 to +85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
Delay time from YSCL falling edge to DIO	t_{pdDOCL}	C_L = 15 pf	—	100	ns
Delay time from YSCL falling edge to ON output	t_{pdCCL}	C_L = 100 pf	—	200	ns
Delay time from $\overline{DSPOF}$ to ON output	$t_{pdCDOFF}$				
Delay time from FR to ON output	t_{pdCFR}		—	300	ns

V_{CC} = 2.7V to 4.5V, V_{DDH} = 14.0 to 28.0V, ta = –40 to +85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
Delay time from YSCL falling edge to DIO	t_{pdDOCL}	C_L = 15 pf	—	200	ns
Delay time from YSCL falling edge to ON output	t_{pdCCL}	C_L = 100 pf	—	400	ns
Delay time from $\overline{DSPOF}$ to ON output	$t_{pdCDOFF}$				
Delay time from FR to ON output	t_{pdCFR}		—	600	ns

Notes: *1. The input signal t_r, t_f is fixed to 20ns.

*2. High speed operation of the shift clocks (XSCL) should be made only under a condition of t_r or $t_f \leq \{t_C - (t_{DCL} + t_{SUE})\}/2$.

■ THE LIQUID CRYSTAL DRIVE POWER SUPPLY

● Forming the Various Voltage Levels

The most appropriate method for obtaining the various voltage levels for driving the LCD is to use resistive voltage dividers for the voltage levels between V_{DDH} and GND, and to drive the voltage levels using voltage followers employing op amps.

Considering the use of the op amp, V_{DDH} and V_0, the lowest voltage level for driving the LCD, and GND and V_5, the lowest voltage for driving the LCD, are separated from each other and given separate pins.

Normally, V_0 and V_{DDH} are connected, as are V_5 and GND, and V_1 and V_4 are driven using voltage followers. When V_0 is driven using a voltage follower, the ability of the LSI to drive the LCD outputs diminishes when the level of V_0 is higher than that of V_{DDH} and the difference in the voltage levels is great; thus the voltage difference between V_{DDH} and V_0 should be kept in the range of 0V to 2.5V.

When there is a serial resistance between the GND and V_{DDH} power supply lines, the voltage between GND and V_{DDH} is reduced at the LSI power terminals because of the I_{DDH} when the signals change, which may lead to permanent damage to the LSI if the relationships between the LCD voltage levels does not follow the formula: $V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq GND$.

When a guard resistance is used, it is necessary to stabilize the voltage with a capacitor.

● Power Supply Stabilization

When necessary to prevent the effects of noise arising from the power supply signal line leads in packaging on the circuit board, a bypass capacitor between the power supplies (GND – V_{CC}, GND – V_{DDH}) may be required in order to stabilize the voltages.

● Cautions Regarding Turning the Power Supply ON and OFF

Because the voltage in the LCD drive system of this LSI is high, the LSI may be permanently damaged by an overcurrent situation when LCD drive signals are output before the LCD drive system applied voltage is stabilized, or when the LCD drive system high-voltage is applied while the logic system power supply is floating or when V_{CCS} is less than 2.6V. It is recommended that the display OFF function $\overline{DSPOFF}$ be used until the LCD drive system voltage stabilized, and that the LCD drive output voltage level be at the V_5 level.

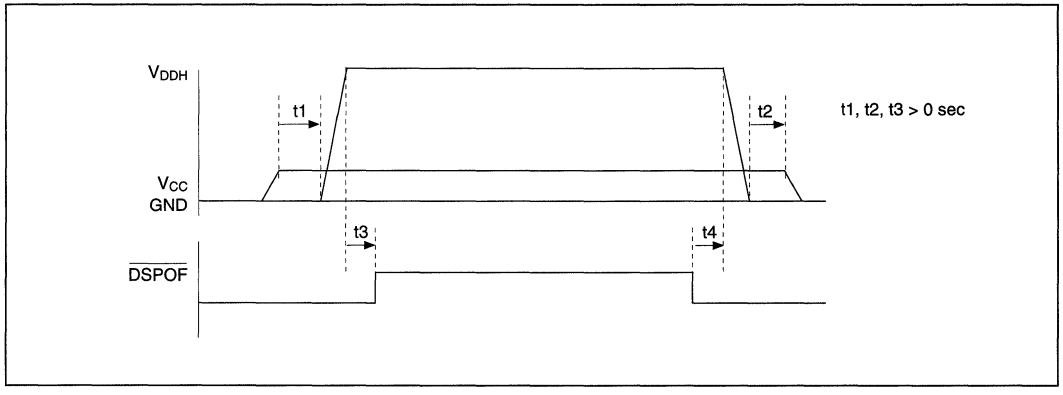
Please follow the following sequences when turning the power supplies ON and OFF:

Power Supply ON:

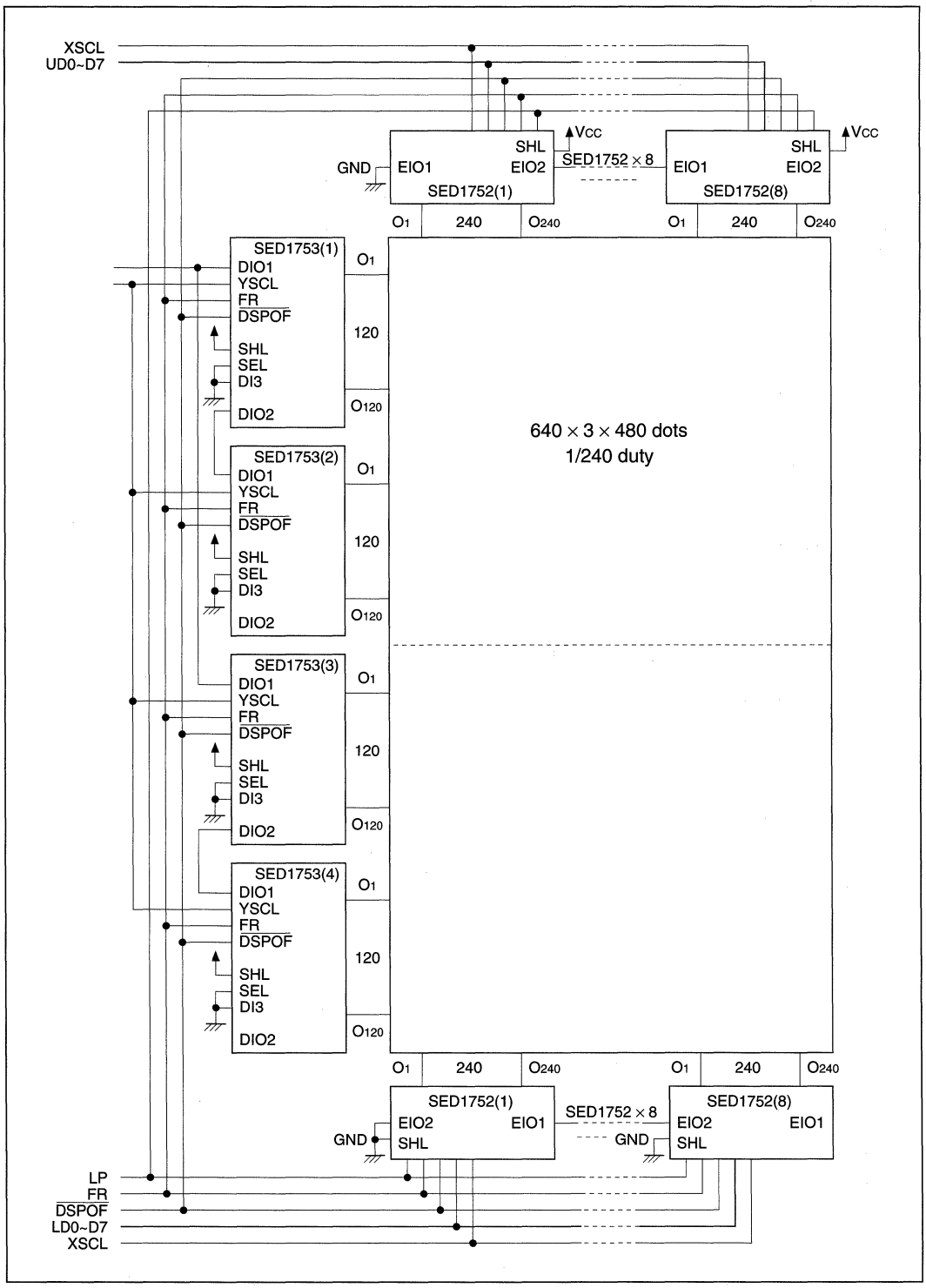
Logic system ON → LCD drive system ON (or simultaneous)

Power Supply OFF:

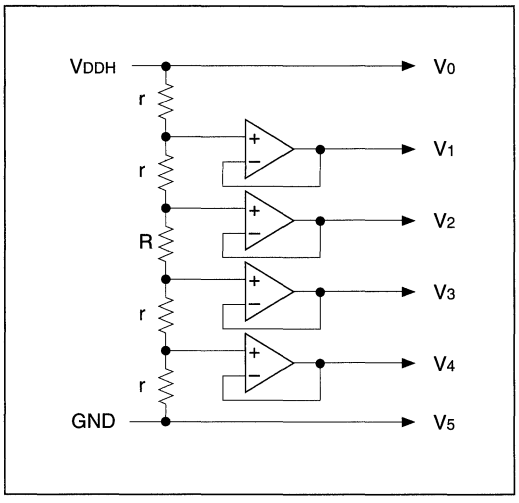
LCD drive system OFF → Logic system OFF (or simultaneous)



■ EXAMPLE OF REFERENCE CIRCUIT

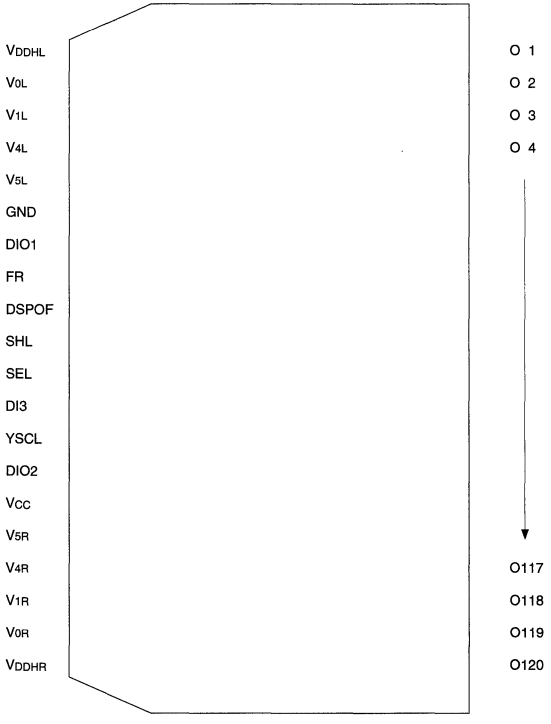


- **Example of LCD Power Supply Circuits**



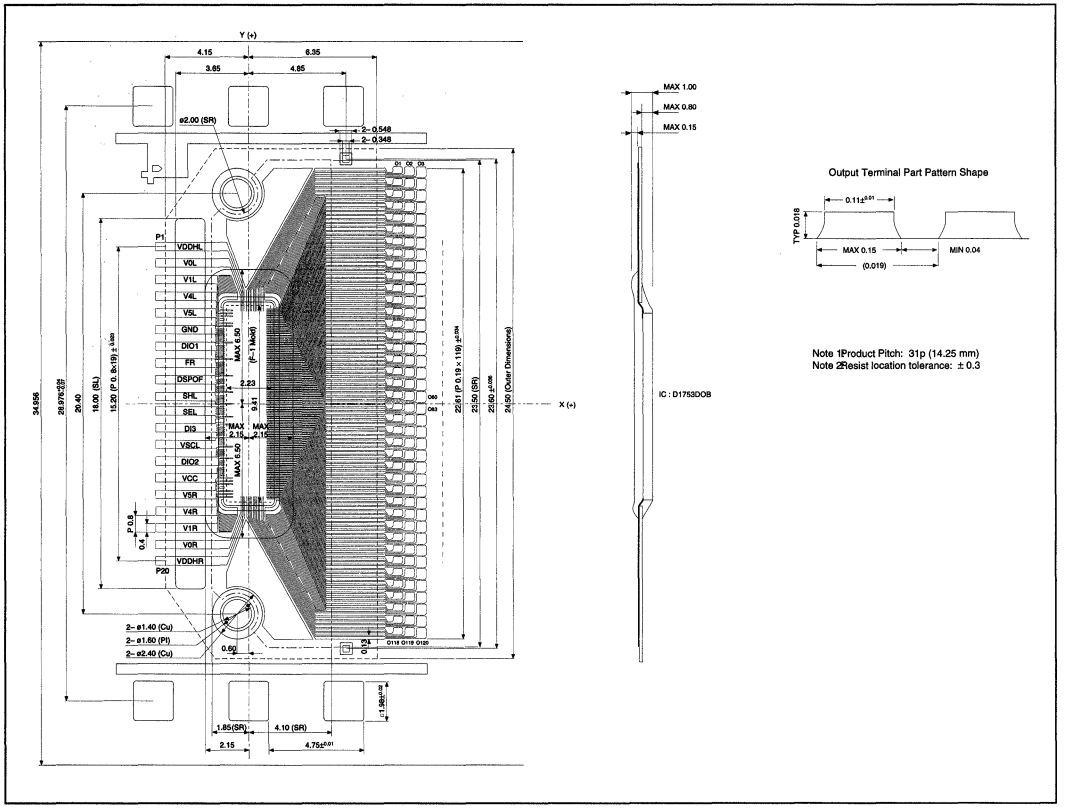
- The LCD drive power supply ($V_0 - V_5$) requires the addition of smoothing capacitors on the appropriate places in the LCD module.
- V_0, V_1, V_4 and V_5 are supplied to SED1753, and V_0, V_2, V_3 and V_5 are supplied to SED1752.
- The logic power supply V_{CC} is supplied to all ICs.
- It is necessary to add bypass capacitors to the appropriate locations between GND – V_{CC} and GND – V_{DDH} to eliminate noise, thereby stabilizing the power supply voltage. It is recommended that the power supplies for high-voltage application (GNDR, GNDL) use a different system than the lines for the power supplies for logic (GND).

- **TCP**
- **An SED1753T** TCP Pinout Example**



Note: The external dimensions of the TCP are not specified.

● External Dimension Diagram



CMOS LCD COMMON DRIVER

■ DESCRIPTION

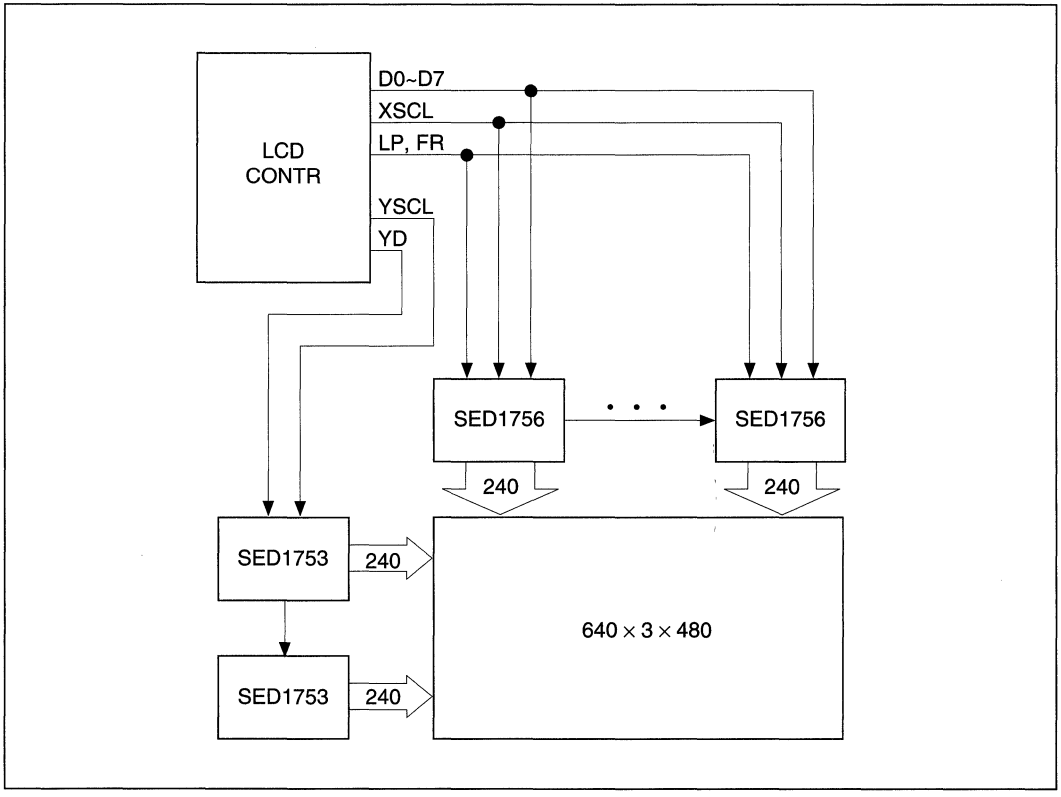
The SED1755 is an LCD common (row) driver designed for extremely high-capacity dot matrix liquid crystal panels. It incorporates 240 high-voltage, low-impedance common drivers in a 2 × 120 format, enabling high driver effectiveness with displays of 1/240, 1/300 and 1/480 duty cycles. It is designed for use in conjunction with the SED1756 segment (column) driver.

The SED1755 features a wide range of liquid crystal drive voltages, an LCD display of high quality and chip layout long from side to side to minimize the LCD panel. It offers a wide range of applications.

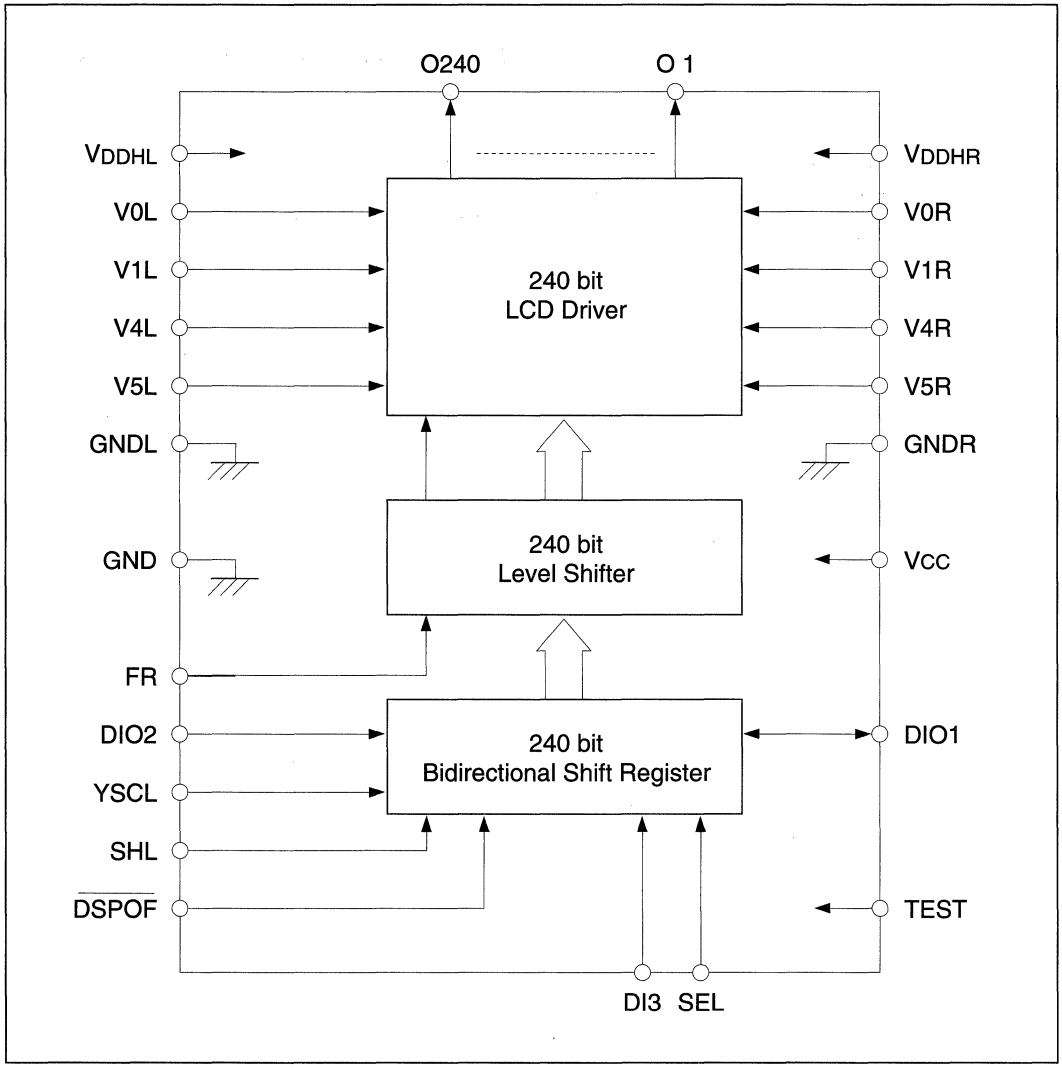
■ FEATURES

- 240 (120 × 2) LCD common drive outputs
- 0.3KΩ (typ.) low output impedance
- High-duty drive available 1/480
- Pin-selectable output shift direction
- Zero-bias display disable function
- Chip configuration long from side to side
- Adjustable LCD drive voltage
- Liquid crystal drive in wide range of voltage
  8 to 42V
- 2.7 to 5.5V supply
- Package: .... D0A .... Al pad die for chip on glass

■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

● Shift Register

The shift register is a bidirectional shift register. SEL is used to select the operating mode (120 × 20-bit or 240-bit) of the shift register. The input of the lower 120-bit will be the DI3 when the 120 × 20-bit is selected.

The effect of SHL on the shift direction and on the input data sequence is shown in the following table.

SHL	Output Shift Direction	DIO1	DIO2
H	240 → 121 120 → 1	Output	Input
L	1 → 120 121 → 240	Input	Output

● Level Shifter

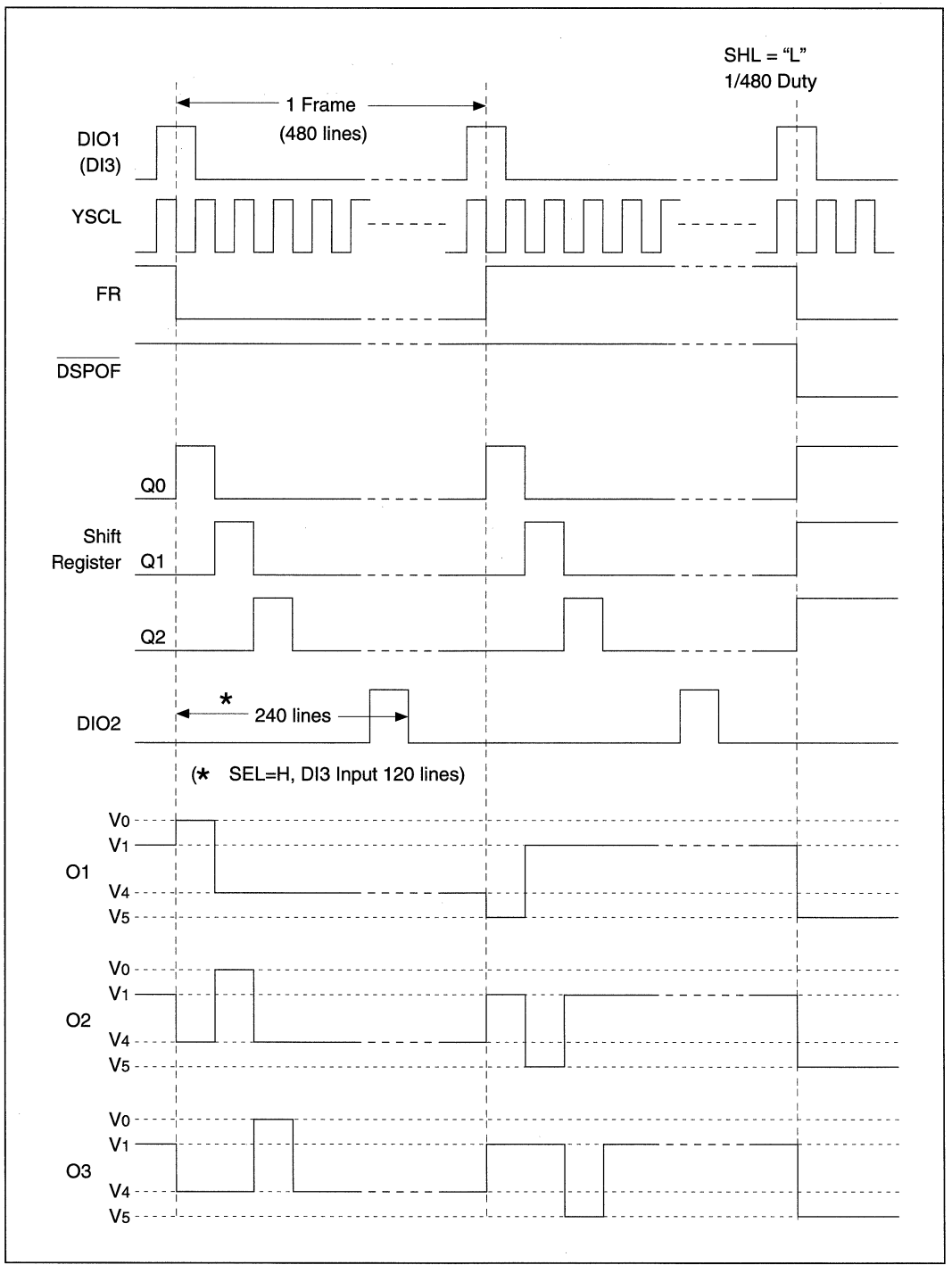
The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

● LCD Drivers

It outputs the LCD driving voltage. Given below are the relations between data bus signals, alternating current signal FR levels and segment output voltages.

/DSPOF	Data	FR	Output Voltage	
H	H	H	V5	Selected
		L	V0	
	L	H	V1	Deselected
		L	V4	
L	—	—	V5	—

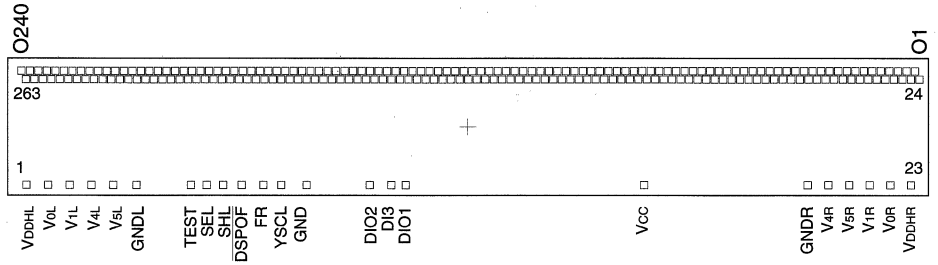
■ TIMING CHART



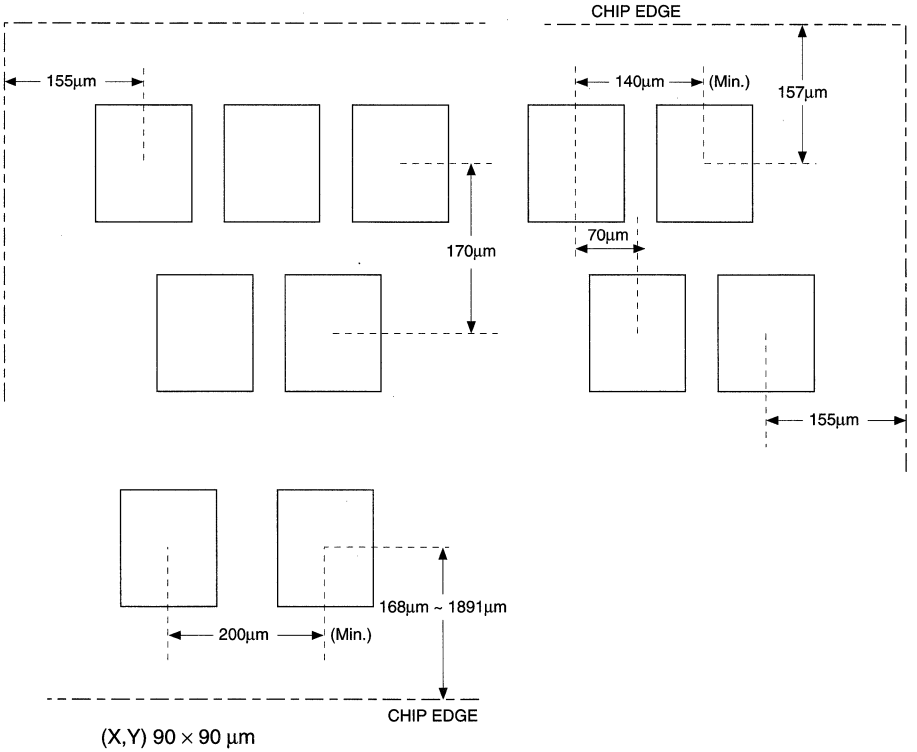
■ PIN DESCRIPTION

Pin Name	I/O	Description	Numbers of Pins
O 1 to O 240	O	Common (low) output for LCD drive Changes at the falling edge of YSCL	240
DIO1 DIO2	I/O	120x2bit bidirectional shift register scan pulse. Set at the input or output by SHL input. The output changes at the falling edge of YSCL	2
DI3	I	The input of scan pulsre whrn 120x20 mode. DI3 is tied to GND when SEL is LOW.	1
SEL	I	Cidirectional shift register operation mode Selection input H: 120x2 (DI3 input L: 240	1
YSCL	I	Serial data shift clock input. Shifts the scan data at the falling edge.	1
SHL	I	Shift durection selection, and DIO terminal I/O control output	
DSPOF	I	The blankimg control input for the display of LCD. All common outputs are made to ?V5 level by "L" input	1
FR	I	For input of alternating current LCD drive signals.	1
GND, V_{CC}	Power supply	Logic operation power supply: GND: 0V, V_{CC}: 2.7 to 5.5V	2
V_{OL}, V_{IL}, V_{4L}, V_{5L}, V_{DDHL}, V_{4L}, V_{OR}, V_{1R}, V_{4R}, V_{5R}, V_{DDHR}, GNDL, GNDR	Power supply	LCD drive curcuit power supply GND: 0V, V_{DDH}: 8V4 to 42V $V_{DDH} \geq V0 \geq V1 \geq 8/9V$ $1/9V_{DDH} \geq V4 \geq V5 \geq GND$	12
TEST	I	Non connect	1

■ PAD DIMENSION



Chip Size : 17.04mm × 2.50mm
Chip Thickness 400µm (Typ.)



(X,Y) 90 × 90 µm

■ PAD COORDINATES

Pad No.	Pad Name	X	Y
1	V_{DDHL}	–8295	–1059
2	V_{OL}	–7895	–1059
3	V_{2L}	–7495	–1059
4	V_{3L}	–7095	–1059
5	V_{5L}	–6695	–1059
6	GNDL	–6295	–1059
7	TEST	–5095	–1082
8	SHL	–4895	–1082
9	$\overline{DSPOF}$	–4495	–1082
10	FR	–4095	–1082
11	LP	–3895	–1082
12	YSCL	–3695	–1082
13	GND	–3095	–1082
14	DIO2	–1895	–1082
15	DI3	–1495	–1082
16	DI01	–1295	–1082
17	V_{CC}	3295	–1082
18	GNDR	6295	–1059
19	V4R	6695	–1059
20	V5R	7095	–1059
21	V1R	7495	–1059
22	V0R	7895	–1059
23	V_{DDHR}	8295	–1059

Pad No.	Pad Name	X	Y
24	O1	8365	923
25	O2	8295	1093
26	O3	8225	923
27	O4	8155	1093
28	O5	8085	923
29	O6	8015	1093
30	O7	7945	923
31	O8	7875	1093
↓	↓	↓	↓
256	0233	–7875	923
257	0234	–7945	1093
258	0235	–8015	923
259	0236	–8085	1093
260	0237	–8155	923
261	0238	–8225	1093
262	0239	–8295	923
263	0240	–8365	1093

X of 0n : 8435– (70 × n) μm

Y of 0n : h = odd : 923 μm
n = even : 1093 μm

■ ELECTRICAL CHARACTERISTICS

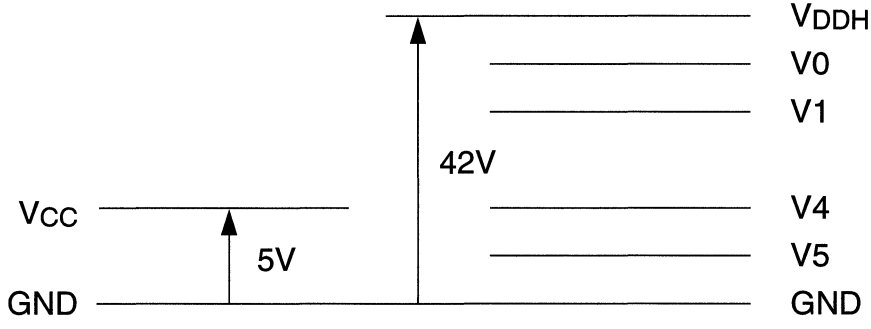
● Absolute Maximum Ratings

Parameters	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_1, V_4, V_5	GND –0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	GND –0.3 to V_{CC} + 0.3	V
Output voltage	V_O	GND –0.3 to V_{CC} + 0.3	V
EIO output current	I_O	20	mA
Working temperature	Topr	–40 to +85	°C
Storage temperature	Tstg 1	–65 to +150	°C

(Note 1): All the voltage ratings are based on GND = 0V.

(Note 2): The storage temperature 1 is applicable to independent chips and the storage temperature 2 is applicable to the TCP modular state.

(Note 3): V_0, V_2, V_3, and V_5 should always be in the order of $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND.



(Note 4): If the logic operation power goes into a floating state or if V_{CC} drops to 2.6V or below while the LCD driving power is being applied, the LSI may be damaged. Therefore, keep from occurrence of the aforementioned status.
Specifically, pay close attention to the power supply sequence at times of turning the system power on and off.

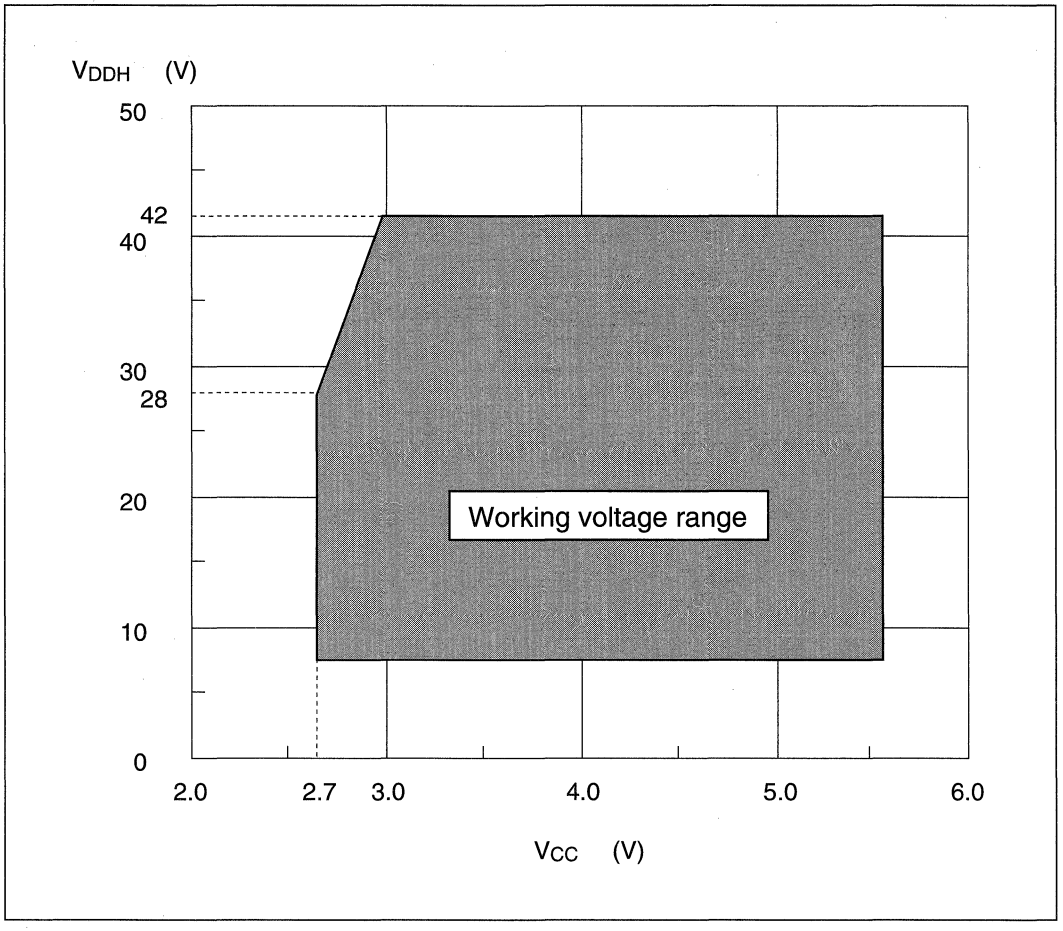
● DC Characteristics

Unless otherwise specified, GND = V_5 = 0V, V_{CC} = +5.0V ± 10%, Ta = –40 to +85°C

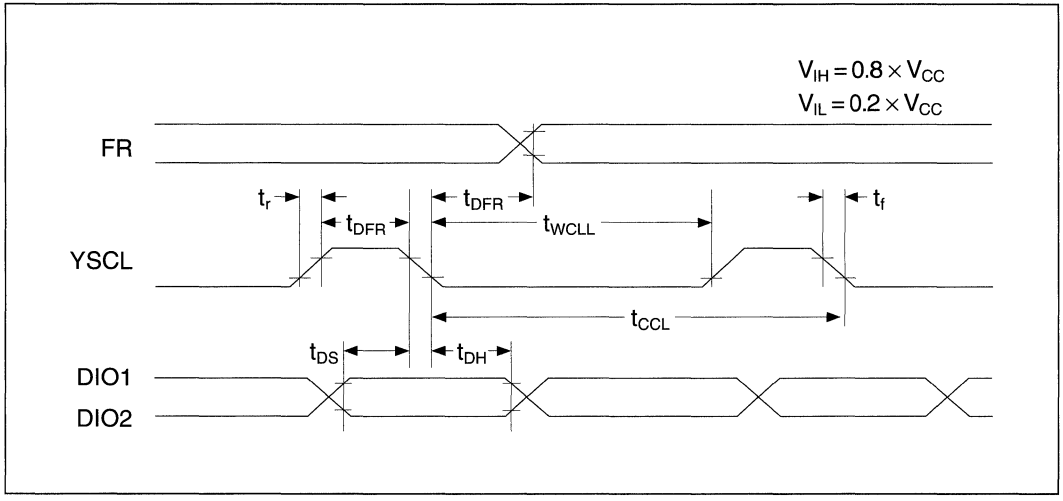
Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}	—	V_{CC}	2.7	—	5.5	V
Recommended working voltage	V_{DDH}	V_{CC} = 2.7 TO 5.5V	V_{0L}, V_{DDHL}	14.0	—	40.0	V
Workable voltage	V_{DDH}	Function only	V_{0R}, V_{DDHL}	8.0	—	42.0	V
Supply voltage (2)	V_1	Recommended value	V_{1L}, V_{1R}	8/9 V_0	—	V_{DDH}	V
Supply voltage (3)	V_4	Recommended value	V_{4L}, V_{4R}	GND	—	1/9 V_{DDH}	V
High level input voltage	V_{IH}	V_{CC}= 2.7~5.5V	DIO1, DIO2, FR YSCL, SHL, SEL, DI3 $\overline{DSPOF}$	0.8 V_{CC}	—	—	V
Low level input voltage	V_{IL}			—	—	0.2 V_{CC}	V
High level output voltage	V_{OH}	V_{CC} = 2.7 – 5.5V, I_{OH} = –0.3mA	DIO1, DIO2	V_{CC}–0.4	—	—	V
Low level output voltage	V_{OL}	V_{CC} = 2.7 – 5.5V, I_{OL} = 0.3mA		—	—	—	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	1 YSCL, SHL, DI3, FR, SEL $\overline{DSPOF}$	—	—	2.0	µ/A
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}	DIO1, DIO2	—	—	5.0	µA
Rest current	IGND	V_0 = 14.0 – 42.0V, V_{IH} = V_{IL} = GND	GND	—	—	25	µA
Output resistance	R_{COM}	ΔVON = 0.5V, Recommended condition: V_0 = +36.0V, 1/24, 01–0240		—	0.35	0.48	KΩ
		V_0 = +26.0V, 1/20		—	0.37	0.5	
In-chip deviation of output resistance	ΔRCOM	ΔVON = 0.5V, V = +36.0V, 1/24		—	—	95	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} = GND, f SCL = 5.38MHz, 1/480, f_{FR} = 70Hz, input data: Checkered indication, no-load	V_{CC}	—	0.15	30	µA
					9	20	
		V_{CC} = +3.0V, Other conditons are the same as those when V_{CC} + 5V.		—	0.3	0.9	
Mean working current consumption (2)	I_{DDH}	V_0 = +30.0V = V_{DDH}, V_{CC} = +5.0V, V1 = 28.0V, V_4 = +2.0V, V5 = +0.0V, Other conditions are the same as those in the I_{DD} column	V_{DDHL}, V_{DDHR}	—	8	20	µA
Input terminal capacity	CI	Freq. = 1 Mhz, Ta = 25°C, Independent chips	SHL, FR YSCL,SEL, $\overline{DSPOF}$	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		DIO1, DIO2	—	—	15	pF

- **Working Voltage Range V_{CC} – V_{DDH}**

The V_{DDH} voltage should be set up within the V_{CC} – V_{DDH} working voltage range given below.



- **AC Characteristics**
  - **Input Timing**



(V_{CC} = 5.0V ± 10%, Ta = –40 to 85°C)

Parameter	Symbol	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	–	400	—	ns
YSCL high level pulse duration	t_{WCLH}		55	—	ns
YSCL low level pulse duration	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		50	—	ns
Data hold time	t_{DH}		40	—	ns
Input signal rise time	t_r		—	50	ns
Input signal fall time	t_r		—	50	ns

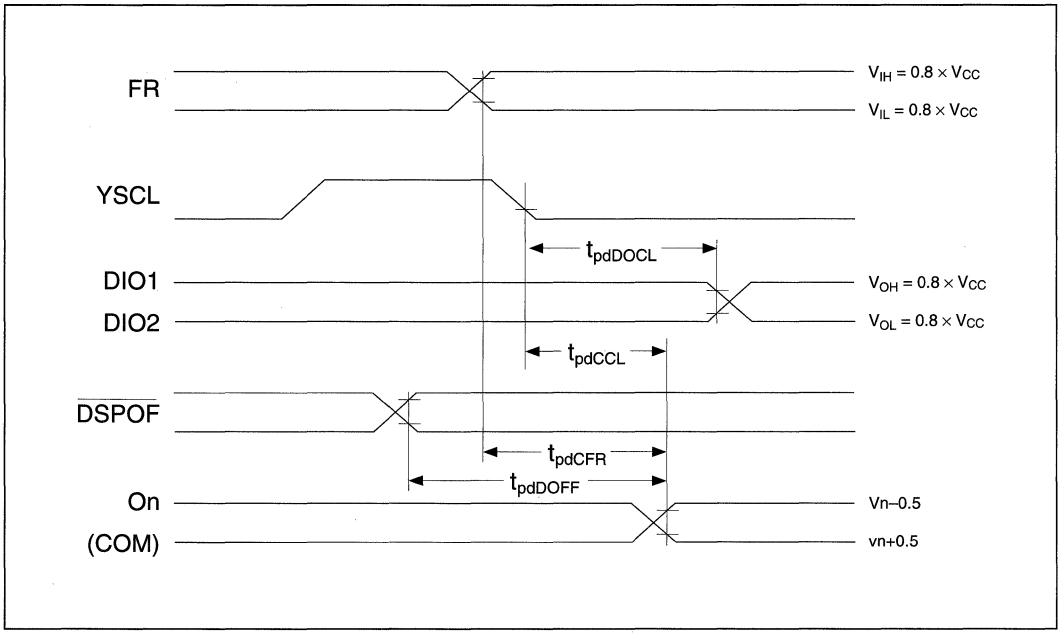
(V_{CC} = 2.7 to 4.5V, Ta = –40 to 85°C)

Parameter	Symbol	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	–	800	—	ns
YSCL high level pulse duration	t_{WCLH}	V_{CC} = 2.7V	100	—	ns
		V_{CC} = 3.0V	80		
YSCL low level pulse duration	t_{WCLL}	—	660	—	ns
Data setup time	t_{DS}	—	90	—	ns
Data hold time	t_{DH}	—	70	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_r		—	50	ns

Note:

t_{DFR}: The changing point and the timing of LP falling are basically 0 ns.

- **AC Characteristics**
  - **Output Timing**



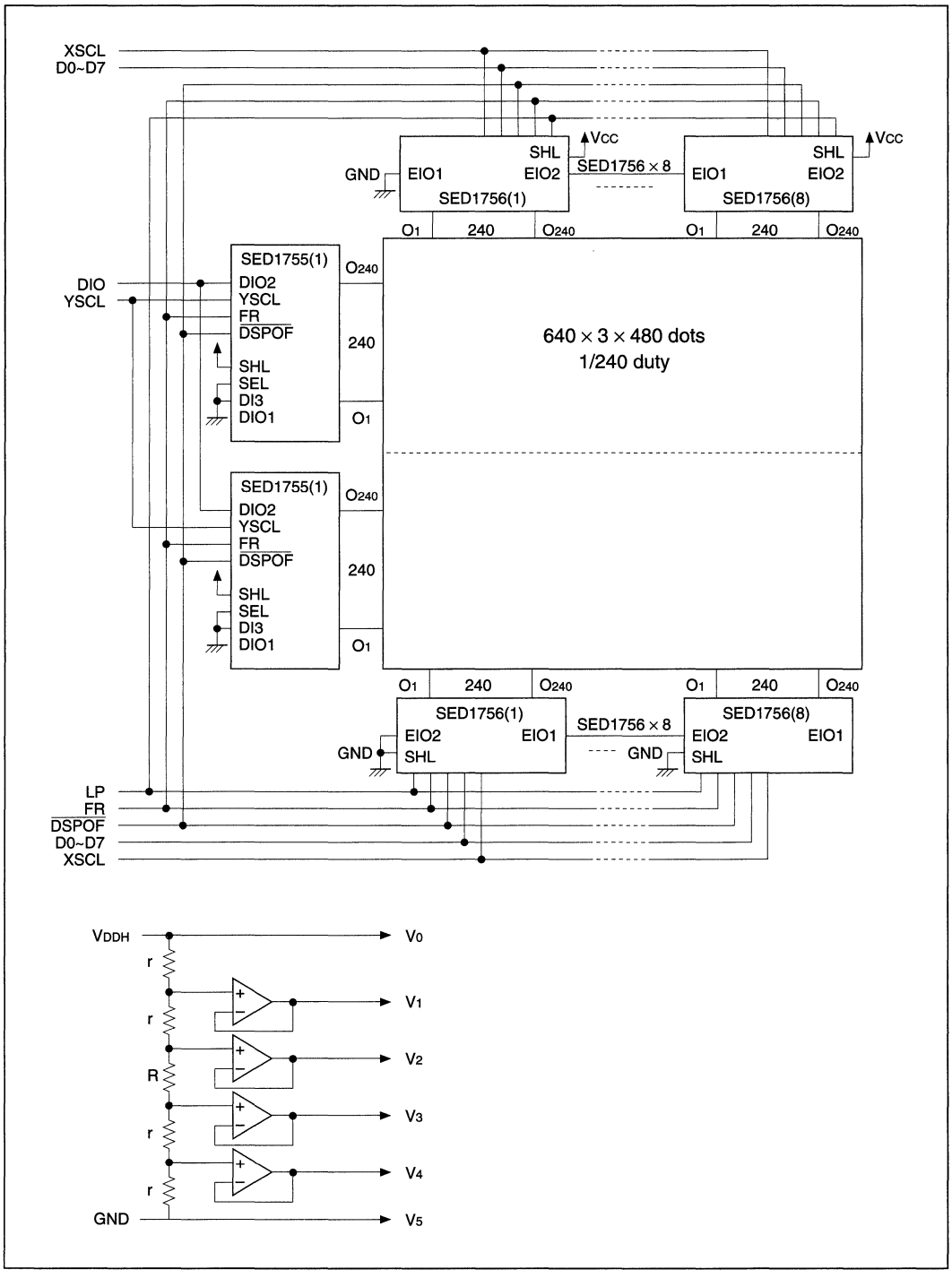
(V_{CC} = 5.0V ± 10%, V_{DDH} = 14.0 to 42.0V, Ta = –40 to 85°C)

Parameter	Symbol	Conditions	Min.	Max.	Units
YSCL→ DIO output delay time	tpdDOCL	C_L = 15 pf	—	100	ns
YSCL→ On output delay time	tpdCCL	C_L = 100 pf	—	200	ns
/DSPOF → On output delay time	tpdCDOFF		—	500	ns
FR → On output delay time	tpdCFR		—	350	ns

(V_{CC} = 2.7 to 4.5V, V_{DDH} = 14.0 to 28.0V, Ta = –40 to 85°C)

Parameter	Symbol	Conditions	Min.	Max.	Units
YSCL→ DIO output delay time	tpdDOCL	C_L = 15 pf	—	200	ns
YSCL→ On output delay time	tpdCCL	C_L = 100 pf	—	400	ns
/DSPOF → On output delay time	tpdCDOFF		—	750	ns
FR → On output delay time	tpdCFR		—	600	ns

■ CONNECTION EXAMPLE (FOR REFERENCE)



■ LCD DRIVING POWER SUPPLY

● Setting Up Respective Voltage Levels

When setting up respective voltage levels for LCD drive, it is the best way to resistively divide the potential between V_0 – GND to drive the LCD by means of voltage follower using an operation amplifier.

In consideration of the case of using an operation amplifier, the LCD driving minimum potential level V_5 and GND are separated and independent terminals are used.

However, since the efficacy of the LCD driving output driver deteriorates when the potential of V_5 goes up beyond the GND potential to enlarge the potential difference, always keep the potential difference of $V_5 - V_{SS}$ at 0V to 2.5V.

When a resistance exists in series in the power supply line of V_0 (GND), I_O at signal changes causes voltage drop at V_0 (GND) of the supply terminals of the LSI disabling it to maintain the relations of the LCD with intermediate potentials of ($V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND), thus leading to breakdown or destruction of the LSI.

When using a protective resistor, do not fail to stabilize the voltage using an appropriate capacitance.

● Precautions When Turning the Power On and Off

Since the LCD drive voltage of these LSIs is comparatively high, if a high voltage of 30V or more is applied to the LCD drive circuit with the logic operation power made floating or with the V_{CC} lowered to 2.6V or less, or when LCD drive signals are output before applied voltage to the LCD drive circuits is stabilized, excess current flows through to possibly lead to breakdown or to destroy the LSI.

It is therefore suggested to maintain the potential of the LCD drive output to V_5 level until the LCD drive circuit voltage is stabilized, using the display off ($\overline{DSPOF}$).

Maintain the following sequences when turning the power on and off:

When turning the power on:

Turn on the logic operation power → turn on the LCD drive power or turn them on simultaneously

When turning the power off:

Turn off the LCD drive power → turn off the logic operation power or turn them off simultaneously

For protection against excess current, insert a quick melting fuse in series in the LCD drive power line. When using a protective resistor, select the optimum resistance value depending on the capacitance of the LCD cells.

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GRAPHICS PRODUCTS

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■ DC/DC CONVERTERS

Part Number	SCI7660	SCI7661	SCI7654
Part Name	CMOS DC/DC Converter	DC/DC Converter with voltage regulator and temperature compensation	DC/DC Converter with voltage regulator and temperature compensation
Discontinued?	No	No	No
Replacement	—	—	—
Maximum output voltage	−20V	−20V	−22V
Maximum output current	30 mA	20 mA	80/N mA
Voltage doubler	yes	yes	yes
Voltage tripler	no	yes	yes
Voltage quadrupler	no	no	yes
Input Voltage	−1.2 to −8.0V	−1.2 to −6.0V	−2.0 to −11.0V
Number of Output Voltage Levels	2	4	4
Conversion Efficiency	95%	95%	95%
Package	DIP-8pin(C0A) SOP4-8pin(M0A)	DIP-14pin(C0A) SOP5-14pin(M0A) SSOP2-16pin(MAA)	SSOP2-16pin (M0A) Al pad Die (D0A)
Page number	867	873	879

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SCI7660C/M Series

CMOS DC/DC CONVERTER

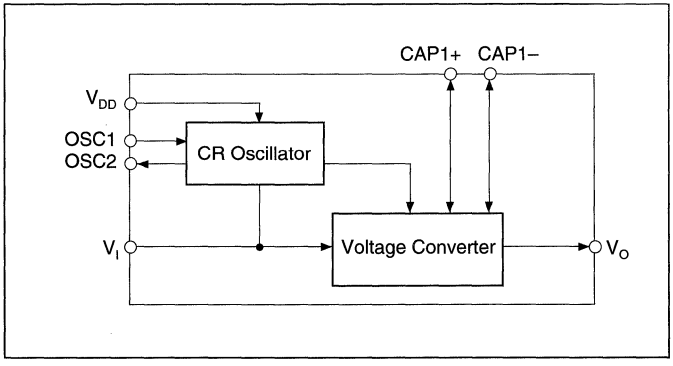
■ DESCRIPTION

The SCI7660C/M CMOS DC/DC Converter features high operational performance with low power dissipation. The booster generates a doubled output voltage from the input.
It is possible to drive an LSI that needs another power supply other than the main power supply (LCD drivers, Analog LSI, etc.). Its very low power requirement makes it ideal to supply handy equipments with power.

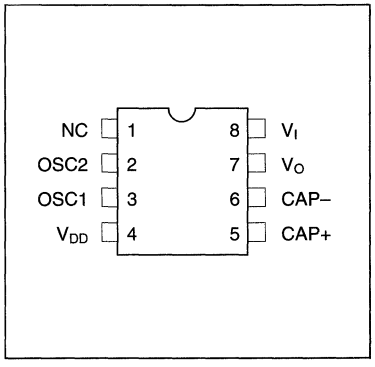
■ FEATURES

- High performance with low power dissipation
- Simple conversion of V_{DD}(+5V) to $-V_I$(–5V), $+2V_I$ (+10V)
- Output current ..... 30mA Max (V_{DD}=5V)
- Power conversion efficiency ..... 95% Typ
- Cascade connection (two device connected V_{DD}=5V, V_O=–10V)
- Low power ..... Ideal for dry cell battery
- On–chip CR oscillator
- Package ..... SCI7660C$_{OA}$ ..... DIP–8pin (plastic)
  SCI7660M$_{OA}$ ..... SOP4–8pin (plastic)
  SCI7660D$_{OA}$ ..... DIE

■ BLOCK DIAGRAM



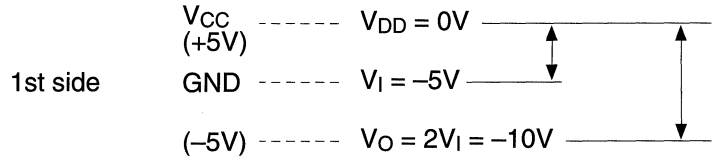
■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin Name	Pin No.	Function
OSC1	3	Oscillation resistor connection terminal
OSC2	2	
V_{DD}	4	Power supply terminal (positive, system supply V_{CC})
CAP1+	5	Terminal for connection of capacitor for booster (positive)
CAP1–	6	Terminal for connection of capacitor for booster (negative)
V_O	7	Output terminal at doubling
V_I	8	Power supply terminal (negative, system supply GND)

■ VOLTAGE RELATIONS



■ ABSOLUTE MAXIMUM RATINGS

(V_{DD}=0V, T_a=25°C)

Parameter	Symbol	Ratings	Unit
Input voltage	V_I	–10.0 to 0.5	V
Output voltage	V_O	–20.0 to V_I	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–30 to 85	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

Note: When this IC is soldered in the solder–reflow process, be sure to maintain the reflow furnace temperature at the curve shown in "Figure 3–5 Reflow Furnace Temperature Curve" of DATA BOOK. And this IC cannot be exposed to high temperature of the solder dipping.

■ ELECTRICAL CHARACTERISTICS

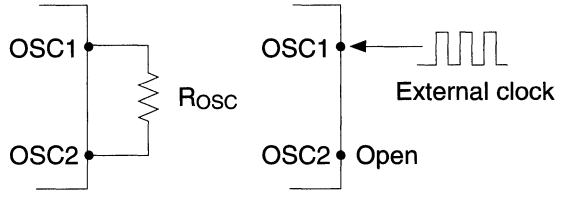
(V_{DD}=0V, T_a=–30° to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_I		–8.0	—	–1.2	V
Output voltage	V_O		–16.0	—	—	V
Booster current consumption	I_{opr}	R_L=∞, R_{OSC}=1MΩ, V_I=–5V	—	40	70	μA
Stationary current	I_Q	R_L=∞, V_I=–8V	—	—	2.0	μA
Output impedance	R_O	I_O=10mA, V_I=–5V	—	80	120	Ω
Booster power conversion efficiency	P_{eff}	I_O=5mA, V_I=–5V	90	95	—	%
Input leakage current	I_{LI}	OSC1 terminal, V_I=–8V	—	—	2.0	μA
Oscillation frequency	f_{OSC}	R_{OSC}=1MΩ, V_I=–5V	16	20	24	kHz

■ CIRCUIT DESCRIPTION

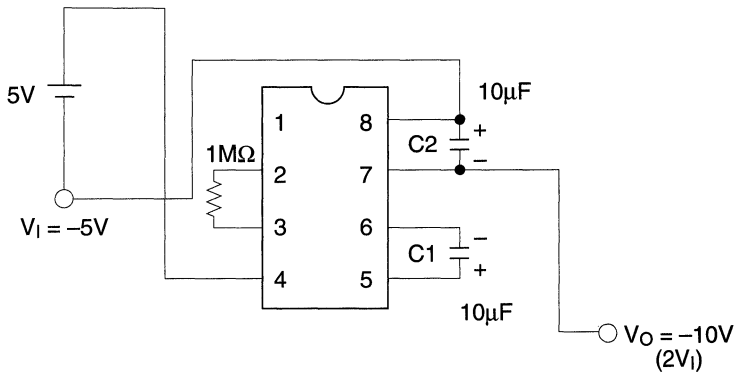
● C–R Oscillator

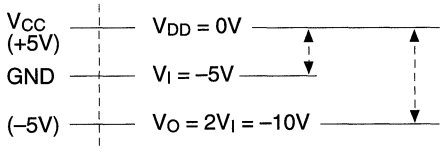
The SCI7660C/M contains a C–R oscillator for internal oscillation. It consists of an external resistor Rosc connected between the OSC1 pin and OSC2 pin.



● Voltage Converters

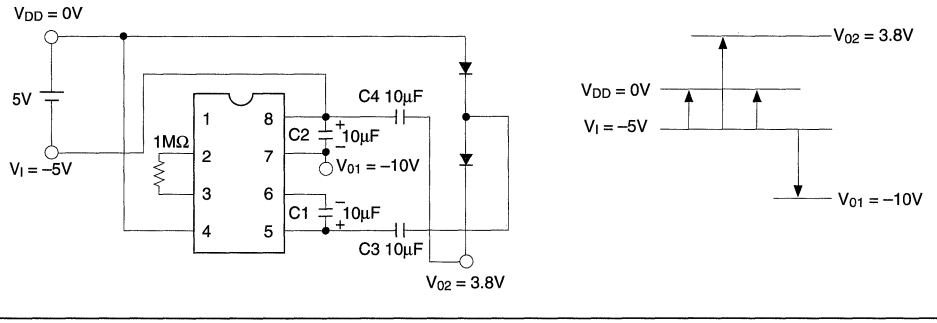
The voltage converters double the input supply voltage (V_I) using clocks generated by the C-R oscillator. A doubled voltage can be obtained with a booster capacitor between CAP+ and CAP–, and with an external smoothing capacitor between V_I and V_O.





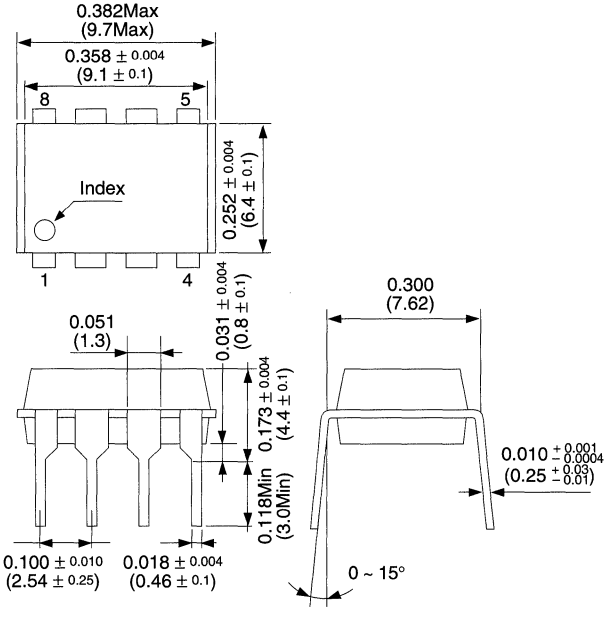
Typical doubled voltage relations

- **Negative Voltage Conversion + Positive Voltage Conversion** (This circuit produces outputs of –10V and +3.8V from the –5V input by combination of voltage doubler circuit and positive voltage conversion circuit.)



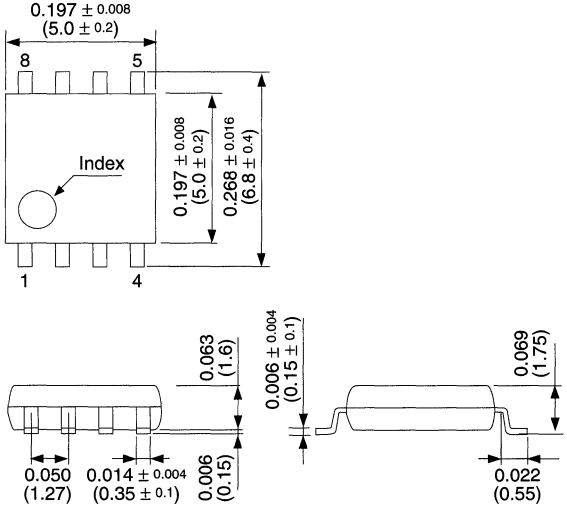
■ PACKAGE DIMENSIONS

Plastic DIP–8pin



unit : inch (mm)

Plastic SOP4–8pin



unit : inch (mm)

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CMOS DC/DC CONVERTER

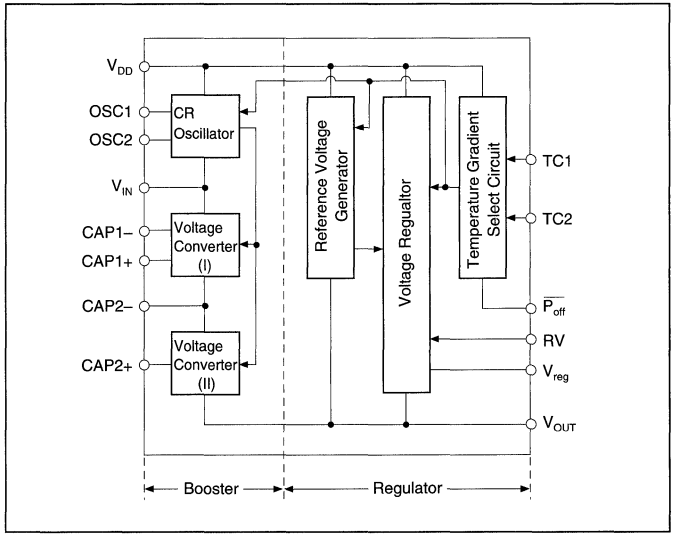
■ DESCRIPTION

The SCI7661C/M CMOS DC/DC Converter features high operational performance with low power dissipation. It consists of two major parts: the booster circuitry and the regulator circuitry. The booster generates a doubled output voltage (–2.4V to –12V) or tripled output voltage (–3.6V to –18V) from the input (–1.2V to –6V). The regulator is capable of setting the output to any desired voltage. The regulated voltage can be given one of three threshold temperature gradients.

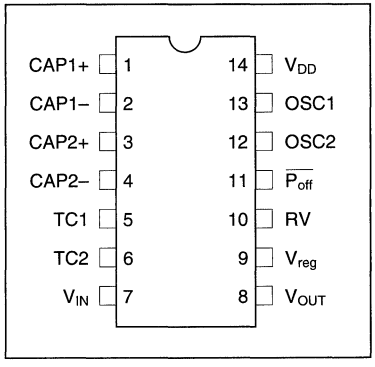
■ FEATURES

- High performance with low power dissipation
- Simple conversion of V_{IN} (–5V) to |V_{IN}| (+5V), 2 |V_{IN}| (+10V), 2 V_{IN} (–10V) or 3 V_{IN} (–15V)
- On–chip output voltage regulator
- Power conversion efficiency ..... Typ 95%
- Temperature gradient for LCD power supply ..... 0.1%/°C, 0.4%/°C or 0.6%/°C
- Power off by external signals — Stationary current at power off ... Max 2μA
- Cascade connection — two devices connected ..... V_{IN}=–5V, V_{OUT}=–20V
- On–chip C–R oscillator
- Package ..... SCI7661C$_{OA}$ .. DIP–14pin (plastic)
  SCI7661M$_{OA}$ .. SOP5–14pin (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



The same pin configuration in DIP and SOP

■ PIN DESCRIPTION

Pin Name	Pin No.	Function
CAP1+, CAP1–	1, 2	Terminal for connection of capacitor for doubler
CAP2+, CAP2–	3, 4	Terminal for connection of capacitor for tripler
TC1, TC2	5, 6	Temperature gradient selection terminal
V_{IN}	7	Power supply terminal (negative, system supply GND)
V_{OUT}	8	Output terminal at tripling
V_{reg}	9	Regulated voltage output terminal
RV	10	Regulated voltage control terminal
$\overline{P_{off}}$	11	V_{reg} output ON/OFF control terminal
OSC2, OSC1	12, 13	Oscillation resistor connection terminal
V_{DD}	14	Power supply terminal (positive system supply V_{CC})

■ ABSOLUTE MAXIMUM RATINGS

(V_{DD}=0V)

Parameter	Symbol	Ratings	Unit
Input supply voltage	V_I	–20/N*1 to 0.5	V
Input terminal voltage	V_I	V_{IN}–0.5 to 0.5 *2	V
		V_{OUT}–0.5 to 0.5 *3	V
Output voltage	V_O	min. –20.0	V
Allowable loss	P_d	300	mW
Operating temperature	T_{opr}	–30 to 85 *4	°C
Storage temperature	T_{stg}	–55 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

***1** N=2: Doubler; N=3: Tripler ***2** OSC1, $\overline{P_{off}}$ ***3** TC1, TC2, RV ***4** Plastic package

Additional Note: When this IC is soldered in the solder–reflow process, be sure to maintain the reflow furnace temperature at the curve shown in "Figure 3–5 Reflow Furnace Temperature Curve" of DATA BOOK. And this IC cannot be exposed to high temperature of the solder dipping.

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=0V, V_{IN}=–5V, Ta=–30° to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input supply voltage	V_I		–6.0		–1.2	V
Output voltage	V_O		–18.0			V
	V_{reg}	R_L=∞, R_{RV}=1MΩ, V_O=–18V	–18.0		–2.6	V
Regulator operating voltage	V_{OUT}		–18.0		–3.2	V
Booster current consumption	I_{opr1}	R_L=∞, R_{OSC}=1MΩ		60	100	μA
Regulator current consumption	I_{opr2}	R_L=∞, R_{RV}=1MΩ, V_O=–15V		5.0	12.0	μA
Stationary current	I_Q	TC2=TC1=V_{OUT}, R_L=∞			2.0	μA
Oscillation frequency	f_{OSC}	R_{OSC}=1MΩ	16	20	24	kHz
Output impedance	R_{OUT}	I_{OUT}=10mA		150	200	Ω
Booster power conversion efficiency	P_{eff}	I_{OUT}=5mA	90	95		%
Regulated output voltage fluctuation	$\frac{\Delta V_{reg}}{\Delta V_{OUT} \cdot V_{reg}}$	–18V<V_{OUT}<–8V, V_{reg}=–8V, R_L=∞, Ta=25°C		0.2		%/V
Regulated output load fluctuation	$\frac{\Delta V_{reg}}{\Delta I_{OUT}}$	V_{OUT}=–15V, V_{reg}=–8V, 0<I_{OUT}<10mA, Ta=25°C, TC1=V_{DD}, TC2=V_O		5		Ω
Regulated output saturation resistance	R_{SAT}	R_{SAT}=Δ(V_{reg}–V_{OUT})/ΔI_{OUT}, 0<I_{OUT}<10mA, R_V=V_{DD}, Ta=25°C		8		Ω
Reference voltage	V_{RV0}	TC2=V_{OUT}, TC1=V_{DD}, Ta=25°C	–2.3	–1.5	–1.0	V
	V_{RV1}	TC2=TC1=V_{OUT}, Ta=25°C	–1.7	–1.3	–1.1	V
	V_{RV2}	TC2=V_{DD}, TC1=V_{OUT}, Ta=25°C	–1.1	–0.9	–0.8	V
Temperature Gradient	C_{T0}	$CT=\frac{\lvert V_{reg}(50°C)\rvert - \lvert V_{reg}(0°C)\rvert}{50°C - 0°C} \times \frac{1}{\lvert V_{reg}(25°C)\rvert} \times 100$	–0.25	–0.1	–0.06	%/°C
	C_{T1}		–0.5	–0.4	–0.3	%/°C
	C_{T2}		–0.7	–0.6	–0.5	%/°C
Input leakage current	I_L	$\overline{P_{off}}$, TC1, TC2, OSC1, RV pins			2.0	μA

■ RECOMMENDED OPERATING CONDITIONS

(Ta=–30° ~ 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Booster start voltage	V_{STA1}	R_{OSC}=1MΩ, C_3 ≥ 10μF *2 C_L/C_3 ≤ 1/20, Ta=–20° to 85°C			–1.2	V
	V_{STA2}	R_{OSC}=1MΩ			–2.2	V
Booster stop voltage	V_{STP}	R_{OSC}=1MΩ	–1.2			V
Output load resistance	R_L		R_L min *3			Ω
Output load current	I_{OUT}				20	mA
Oscillation frequency	f_{OSC}		10		30	kHz
External resistance for oscillation	R_{OSC}		680		2000	kΩ
Capacitor for booster	C_1, C_2, C_3		3.3			μF
Regulated output adjustable resistance	R_{RV}		100		1000	kΩ

*1 V_{DD}=0V

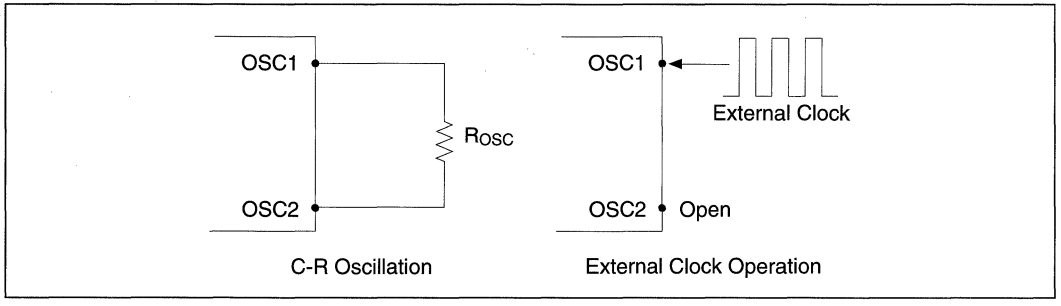
*2 Recommended circuitry in low voltage operation is shown below (next page, diagram on left) (V_{IN}=–1.2V~–2.2V)

*3 R_L min depends on input voltage as shown below (next page, diagram on right)

■ CIRCUIT DESCRIPTION

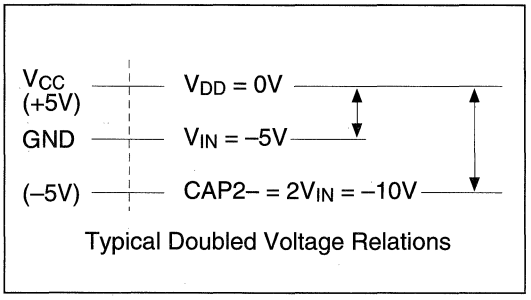
● C–R Oscillator

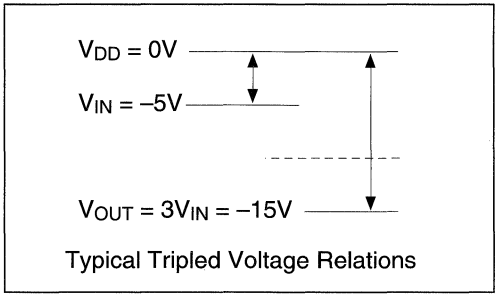
The SCI7661C/M contains a C–R oscillator for internal oscillation. It consists of an external resistor R_{OSC} connected between the OSC1 pin and OSC2 pin.



● Voltage Converters

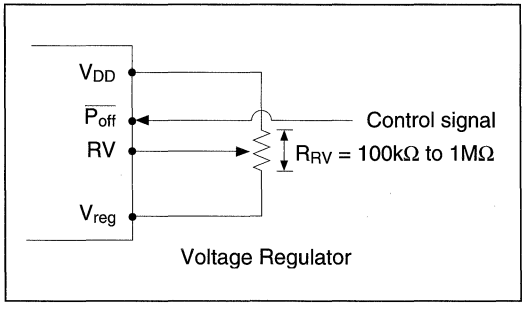
The voltage converters double/triple the input supply voltage (V_{IN}) using clocks generated by the C–R oscillator.





● Reference Voltage Generator and Voltage Regulator

The reference voltage generator produces reference voltage needed for operation of regular circuit. The voltage regulator is used to regulate a boosted output voltage and its circuit contains a power–off function which uses signals from the system for on–off control of the V_{reg} output.



● Temperature Gradient Selector Circuit

The SCI7661C/M provides the V_{reg} output with a temperature gradient suitable for LCD driving (between V_{DD} and V_{reg}).

- **Temperature Gradient Assignment**

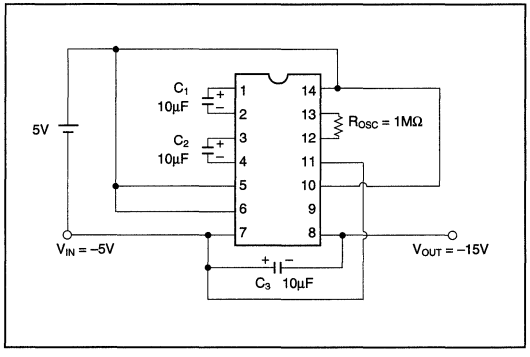
$\overline{Poff}$	TC2	TC1	Temp. Gradient	Vreg Output	CR oscillation	Remarks
1 (VDD)	L (VOUT)	L (VOUT)	–0.4% / °C	ON	ON	
1	L	H (VDD)	–0.1% / °C	ON	ON	
1	H (VDD)	L	–0.6% / °C	ON	ON	
1	H	H	–0.6% / °C	ON	OFF	Cascade connection
0 (VIN)	L	L	—	OFF (Hi-Z)	OFF	
0	L	H	—	OFF (Hi-Z)	OFF	
0	H	L	—	OFF (Hi-Z)	OFF	
0	H	H	—	OFF (Hi-Z)	ON	Without regulation

NOTE: The potential at Low level is different between the $\overline{Poff}$ pin and the TC1/TC2 pin.

■ EXAMPLE OF APPLICATIONS

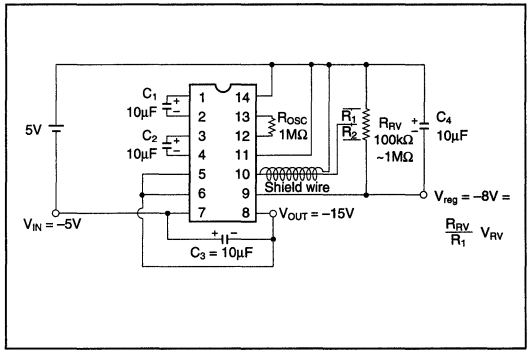
- **Voltage Doubler and Tripler**

A doubled voltage can be obtained at VOUT (CAP2–) by disconnecting capacitor C2 from the tripler configuration and shorting CAP2– (pin 4) and VOUT (pin 8).



- **Voltage Tripler + Regulator**

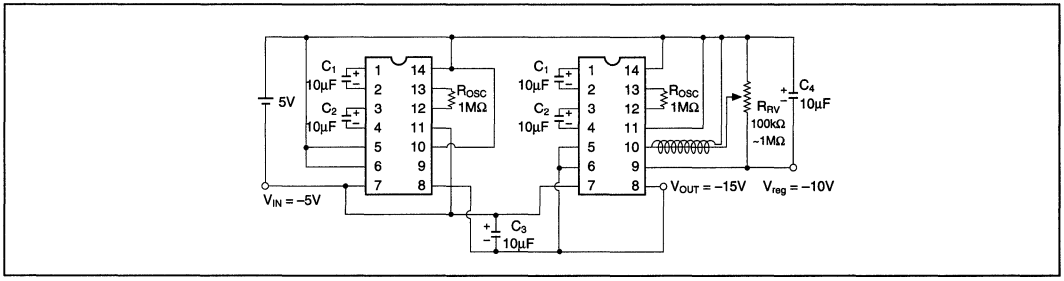
Vreg output is given a temperature gradient, after boosted output VOUT regulated. In this connection, both VOUT and Vreg can be taken out at the same time.



- **Parallel Connection**

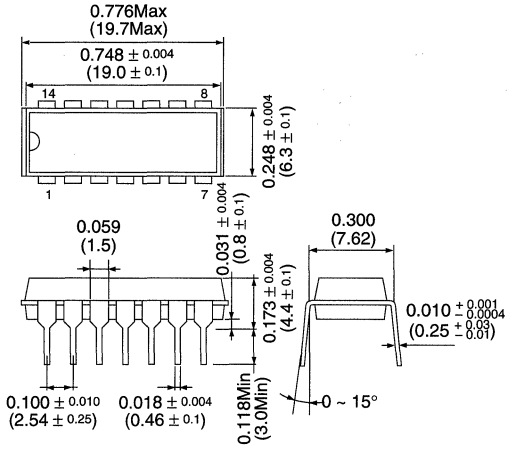
Parallel connection of n circuits can reduce ROUT to about 1/n, that output impedance ROUT can be reduced by connecting serial configuration. A single smoothing capacitor C3 can be used commonly for all parallelly connected circuits.

In parallel connection, a regulated output can be obtained by applying the regulation circuit to only one of the n parallelly connected circuits.



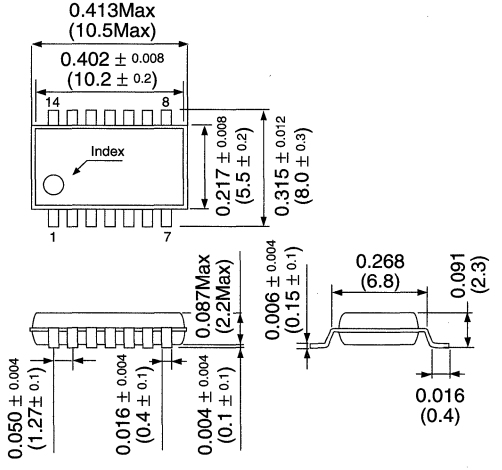
■ PACKAGE DIMENSIONS

Plastic DIP-14 pin



unit : inch (mm)

Plastic SOP5-14 pin



unit : inch (mm)

CMOS DC/DC CONVERTER

■ DESCRIPTION

The SCI7654 is a high-efficiency low-power consumption charge pump-style DC/DC converter and voltage regulator which uses a CMOS process. The charge pump-type DC/DC converter can generate an output voltage of 4 times (or 3 times or 2 times) the input voltage in the negative direction using 4 (or 3 or 2) external capacitors.

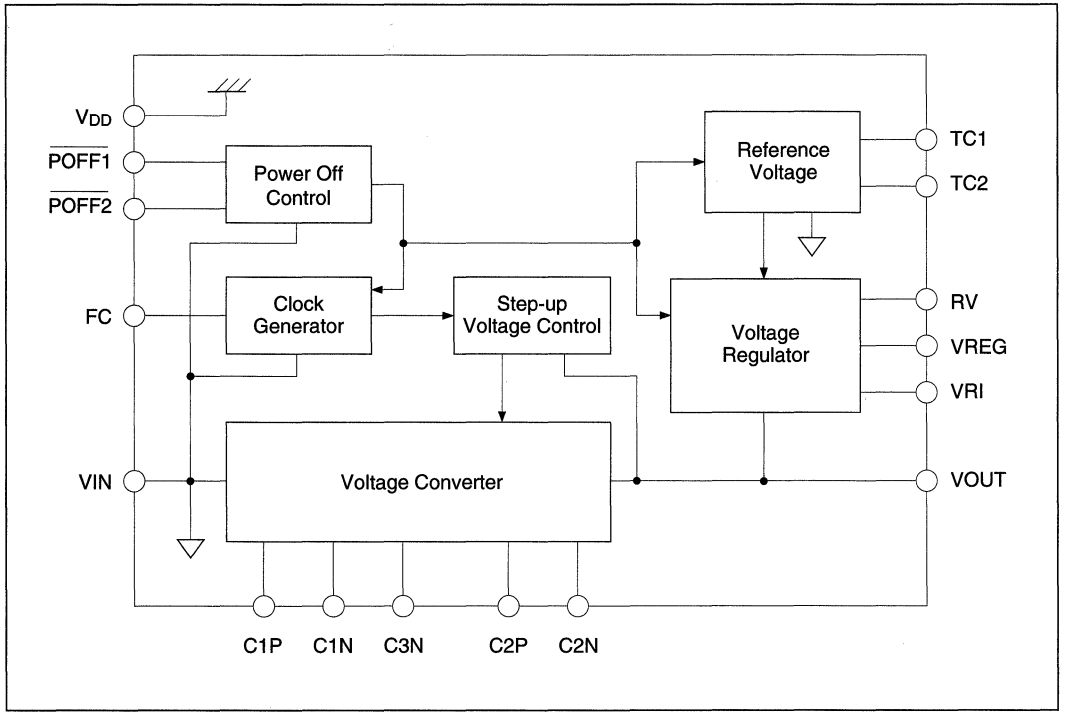
The voltage regulator is able to regulate the voltage output generated by the DC/DC converter at a selectable voltage using 2 external resistors. The regulated output of the voltage regulator can also be equipped with the negative temperature gradient characteristics required by liquid crystal panels.

The outputs of the SCI 7654 can be powered down by an external signal, thereby reducing wasted power during temporary system shutdowns, etc., making it an ideal power source for battery-operated portable devices and LCD panels.

■ FEATURES

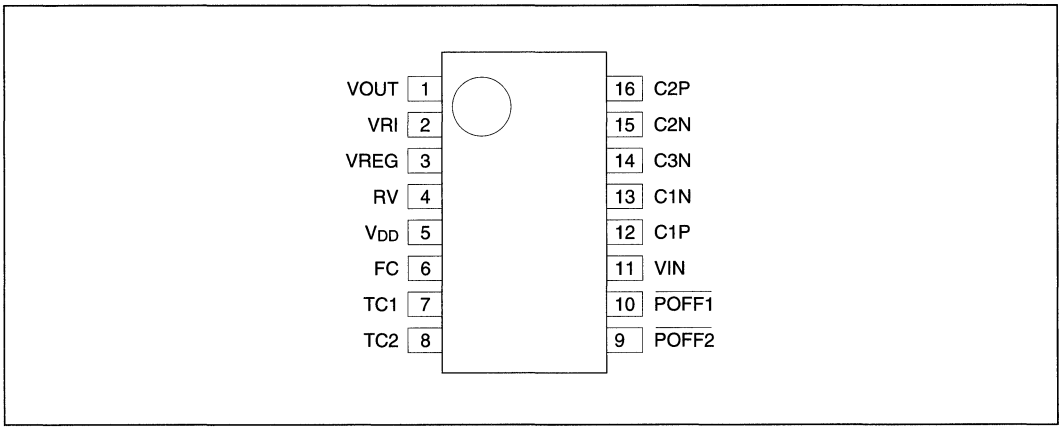
- DC converter (negative-direction 4X/3X/2X)
- Equipped with a voltage regulator (voltage-regulated output circuit)
- High voltage conversion efficiency 95%
- Low consumption current ..... 150 μA (VIN =–5.0 V when using 4X voltage step-up)
- High output capability ..... 20 mA
- Input voltage ..... –2.0 to –5.5 volts (when using 4 X voltage step-up)
–2.0 to –7.3 volts (when using 3 X voltage step-up)
–2.0 to –11. volts (when using 2 X voltage step-up)
- DC/DC converter output voltage ..... (VIN) X 4 (MAX)
- Internal reference voltage for high-precision regulator ..... –1.5 volts ± 0.05 volts (when CTO)
- Regulator output voltage temperature gradient function ..... –0.04, –0.15, –0.35, –0.55 (%/°C)
- Low standby current (when power is off)
- High-multiplier voltage step-up and regulation also possible through series connections and additional components
- External-signal power-function
- Oscillator function is completely internal
- Small, slim package (SSOP2-16) SCI7654MOA
- Chip product ..... SCI7654 DOA
- This product is not designed for resistance to radiation

■ BLOCK DIAGRAM



■ CONFIGURATION

● Pin Configuration (SCI7654M0A)



● Pin Description

Terminal Name	SCI7654MOA Pin No.	SCI7654DOA Pad No.	Function
VOUT	1	18	4 X step-up voltage output terminal
VRI	2	19	Regulated voltage input terminal
VREG	3	20	Regulated voltage output terminal
RV	4	21	Regulated output voltage control terminal
VDD	5	22,23	Power supply terminal (positive side)
FC	6	24	Internal clock frequency cutover input terminal Serial/parallel connection clock input terminal (used for both)
TC1	7	3	Temperature gradient set input terminal (1)
TC2	8	4	Temperature gradient set input terminal (2)
$\overline{\text{POFF2}}$	9	5	Power off control input terminal (2)
$\overline{\text{POFF1}}$	10	6	Power off control input terminal (1)
VIN	11	11,12	Power supply voltage (negative side)
C1P	12	13	2 X voltage step-up, 4 X voltage step-up capacitor positive-side connection terminal
C1N	13	14	2 X voltage step-up capacitor negative-side connection terminal
C3N	14	15	4 X voltage step-up capacitor negative-side connection terminal
C2N	15	16	3 X voltage step-up capacitor negative-side connection terminal
C2P	16	17	3 X voltage step-up capacitor positive-side connection terminal

■ ABSOLUTE MAXIMUM RATINGS

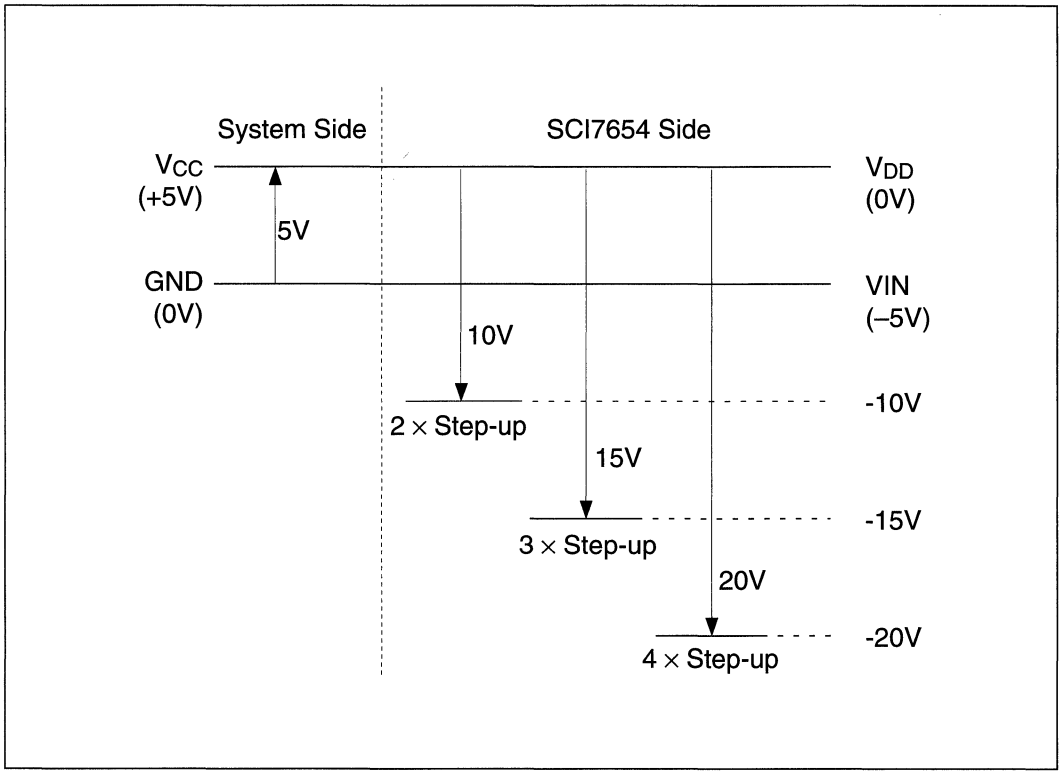
Parameter	Symbol	Read Values		Units	Notes
		Minimum	Maximum		
Input power supply voltage	V_{IN}	–26.0 /N	V_{DD} + 0.3	V	N= step-up voltage multiplier VIN terminal
Input terminal voltage	V_I	V_{IN} –0.3	V_{DD} + 0.3	V	POFF1, POFF2, TC1, TC2, FC terminals
Output terminal voltage 1	V_{OC1}	V_{IN} –0.3	V_{DD} + 0.3	V	C1P, C2P terminals
Output terminal voltage 2	V_{OC2}	2 X V_{IN}–0.3	V_{IN} + 0.3	V	C1N terminals
Output terminal voltage 3	V_{OC3}	3 X V_{IN}–0.3	2 X V_{IN} + 0.3	V	C2N terminal
Output terminal voltage 4	V_{OC4}	4 X V_{IN}–0.3	3 X V_{IN} + 0.3	V	C3N terminal
Regulator input power	V_{RI}	N X V_{IN}–0.3	V_{DD} + 0.3	V	N = step-up voltage multiplier, V_{RI} supply voltage terminal
Regulator input terminal	V_{RV}	N X V_{IN}–0.3	V_{DD} + 0.3	V	N = step-up voltage multiplier, R_V voltage terminal
Output voltage	V_O	N X V_{IN}–0.3	V_{DD} + 0.3	V	N = step-up voltage multiplier. V_{OUT}. V_{REG} terminal
Input current	I_{IN}		80	mA	V_{IN} terminal
Output current	I_{OUT}		N <= 4: 20 N > 4: 80/N	mA	N = step-up voltage multiplier V_{OUT}. V_{REG} terminal
Allowable loss	Pd		210	mW	
Operating temperature	T_{OPR}	–30	85	°C	
Storage temperature	T_{STG}	–55	150	°C	
Soldering temperature/time	T_{SOL}		260 X 10	°C•S	At the leads

Note 1: Operating the chip under conditions exceeding the absolute rated values above may result in misoperation and permanent damage to the chip. Moreover, the reliability of the chip will be seriously compromised even if the chip appears to function normally for a time.

Note 2: Relationships of voltage levels with the external system

The common power supply for the SCI7654 is the highest voltage level (V_{DD}). Because of this, the values in this specification are all expressed in terms of a V_{DD} = 0 V reference, and consequently caution is required regarding voltage levels when connecting to the external system.

● **Relationship of Voltage Levels**



■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

If not otherwise indicated, T_a = –30°C to +85°C, V_{DD} = 0V, V_{IN} = –5.0V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input power supply voltage 1	V_{IN1}	For 4X step-up voltage	–5.5		–2.0	V
Input power supply voltage 2	V_{IN2}	For 3X step-up voltage	–7.3		–2.0	V
Input power supply voltage 3	V_{IN3}	For 2X step-up voltage	–11		–2.0	V
Input power supply voltage N	V_{INN}	When used with high multiplier step-up voltages using an external diode. "N" is the step-up multiplier.	–22/N		–2.0	V
Step-up initial input power supply voltage	V_{STA}	"N" is the step-up multiplier, I_{OUT}<200 µA FC = V_{DD}	–22/N		–2.4	V
Step-up output voltage	V_{OUT}		–22			V
Regulator input voltage	V_{RI}		–22		–2.0	V
Regulator output voltage	V_{REG}	REG = 0, V_{RI} =–22V, R_{RV} = 1MΩ			–2.0	V
Step-up output impedance	R_{OUT}	I_{OUT} = 10 mA, for 4X step-up voltage		180	250	Ω
Step-up output conversion efficiency	P_{eff}	I_{OUT} = 2 mA For 4X step-up voltage C1, C2, C3, C_{OUT} = 10 µF (tantalum)		95		%
Step-up converter operating consumption current 1	I_{OPR1}	FC = V_{DD}, P_{OFF1} = V_{IN}, P_{OFF2} = V_{DD} with no load C1, C2, C3, C_{OUT} = 10 µF (tantalum)		150	220	µA
Step-up converter operating consumption current 2	I_{OPR2}	FC = V_{IN}, P_{OFF1} = V_{IN}, P_{OFF2} = V_{DD} with no load C1, C2, C3, C_{OUT} = 10 µF (tantalum)		600	800	µA
Regulator operating consumption current	I_{OPVR}	V_{RI} =–20V, with no load R_{RV} = 1MΩ		10	15	µA
Idle current	I_Q	P_{OFF1} = V_{IN}, P_{OFF2} = V_{IN} FC = V_{DD}			5.0	µA
Input leakage current	I_{LIN}	Applicable terminals: P_{OFF1}, P_{OFF2}, FC TC1, TC2			0.5	µA
Regulated output saturation resistance	R_{SAT} (Note 1)	0<I_{REG}<20 mA R_V = V_{DD} Ta = 25 °C		10		Ω
Regulated output voltage regulation	D_{VR} (Note 2)	–20V<V_{RI}<–10V, I_{REG} = 1 mA V_{REG} =–15V Ta = 25 °C		0.2		%/V
Regulated output load deviation	D_{V0} (Note 3)	V_{RI} =–20V V_{REG} =–15V Ta = 25 °C 0<I_{REG} < 20mA		50		mV
Reference Voltage (Ta = 25 °C)	V_{REF0}	TCI = V_{DD}, TC2 = V_{DD}	–1.55	–1.50	–1.45	V
	V_{REF1}	TC1 = V_{DD}, TC2 = V_{DD}	(TBD)	–1.50	(TBD)	V
	V_{REF2}	TC1 = V_{DD}, TC2 = V_{DD}	(TBD)	–1.50	(TBD)	V
	V_{REF3}	TC1 = V_{DD}, TC2 = V_{DD}	(TBD)	–1.50	(TBD)	V
Reference Voltage Temperature Coefficient (Note 4) (Note 5)	CT0	TC1 = V_{DD}, TC2 = VDD, SSOP Product	(TBD)	–0.04	0	%/°C
	CT1	TC1 = V_{DD}, TC2 = V_{IN}, SSOP Product	(TBD)	–0.15	(TBD)	%/°C
	CT2	TC1 = V_{IN}, TC2 = V_{DD}, SSOP Product	(TBD)	–0.35	(TBD)	%/°C
	CT3	TC1 = V_{IN}, TC2 = V_{IN}, SSOP Product	(TBD)	–0.55	(TBD)	%/°C
Input voltage level	V_{IH}	V_{IN} =–2.0 V to –5.5V Applicable terminals: P_{OFF1}, P_{OFF2}, FC, TC1, TC2	0.2 V_{IN}			V
	V_{IL}	V_{IN} =–2.0 V to –5.5V Applicable terminals:P_{OFF1}, P_{OFF2}, FC, TC1, TC2			0.8 V_{IN}	V
Step-up capacitor	C_{MAX}	Applicable capacitors: C1, C2, C3			47	µF

(Note 1): $R_{SAT} = \frac{\Delta(V_{REG} - V_{OUT})}{\Delta I_{REG}}$

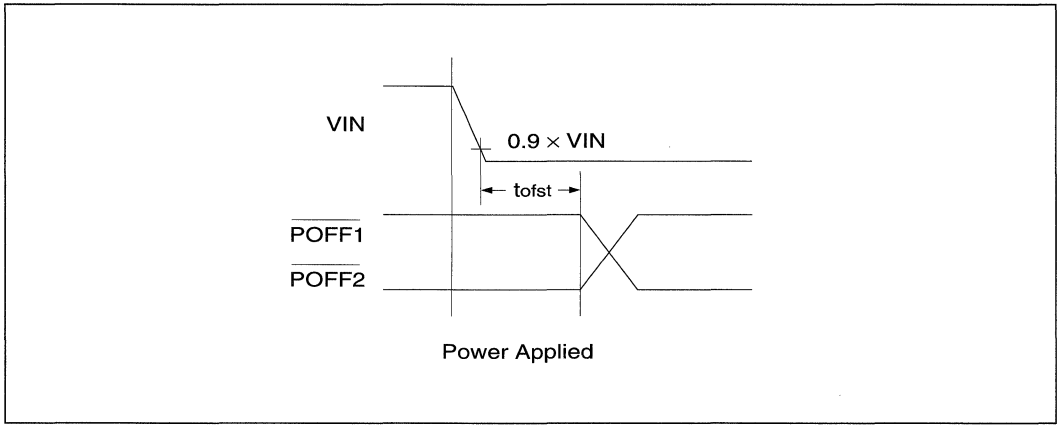
(Note 2): $\Delta V_R = \frac{\Delta V_{REG}}{\Delta V_{OUT \cdot REG}}$

(Note 3): $\Delta V0 = \frac{\Delta V_{REG}}{\Delta I_{REG}}$

(Note 4): $\Delta CT = \frac{|V_{REF}(50°C)| - |V_{REF}(0°C)|}{50°C - 0°C} \times \frac{100}{|V_{REF}(25°C)|}$

(Note 5): The reference voltage temperature coefficient of the chip product may change depending on the molding material and the packaging. Use only after performing temperature tests.

- **AC Characteristics**



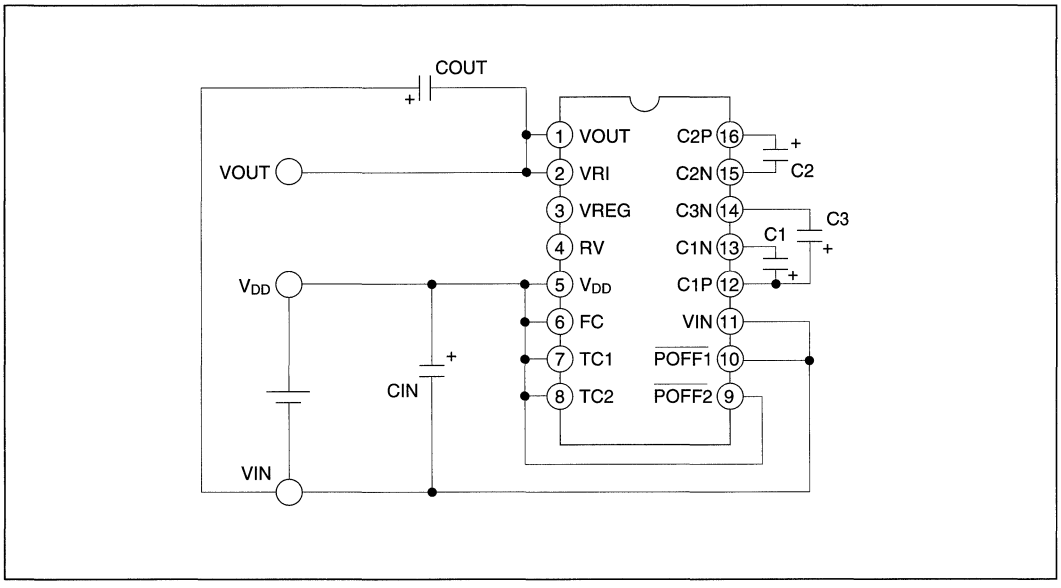
Power off control timing characteristics

If not otherwise indicated, T_a = –30°C to +85°C, V_{DD} = 0V, V_{IN} =–5.0V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal clock frequency 1	f_{CL1}	FC = V_{DD}, P_{OFF1} = V_{DD}, P_{OFF2} = V_{IN} Applicable terminals: C2P terminal	3.0	4.0	6.0	kHz
Internal clock frequency 2	f_{CL2}	FC = VIN, P_{OFF1} = V_{DD}, P_{OFF2} = V_{IN} Applicable terminals: C2P terminal	12.0	16.0	24.0	kHz
Power off control begin time	t_{ofst}	Applicable terminals: P_{OFF1}, P_{OFF2}	(TBD)			ms

■ 4X STEP-UP

Only the step-up circuit is made to function and the chip generates a regulated voltage equal to 4 times the input voltage V_{IN} (but in the negative direction), outputting it to the V_{OUT} terminal. However, because the regulator circuit is not used, the voltage at the V_{OUT} terminal includes some ripple component. The figure below shows an example of the connections.



Conditions for Above Figure

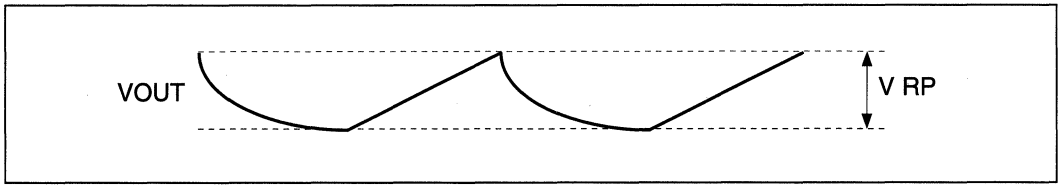
- Internal clock: ON (high output mode)
- Step-up circuit: ON
- Regulator: OFF

Power Off Method

- Through setting the $\overline{\text{POFF2}}$ terminal to "L" level (VIN), all circuits can be turned off.

The Ripple Voltage

- Because the output voltage generated at VOUT terminal is not regulated, it includes a ripple component such as shown in the figure below. The ripple voltage VRP increases with load current, and can be calculated roughly using the equation below.



$$V_{RP} = \frac{I_{OUT}}{2 \cdot f_{CL} \cdot C_{OUT}} + I_{OUT} \cdot R_{COUT}$$

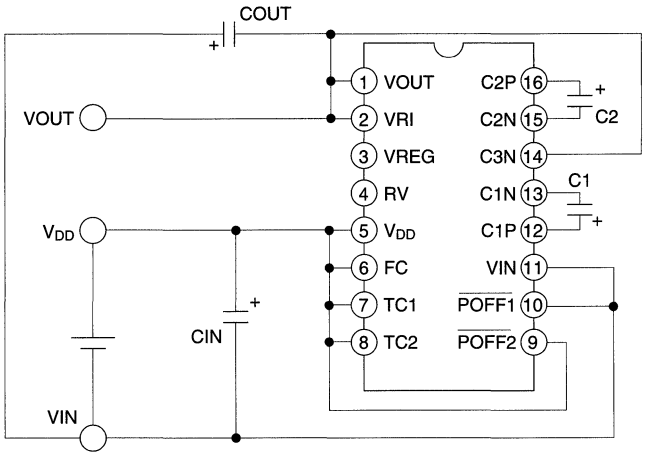
I_{OUT}: Load current (A)
f_{CL}: Clock frequency (Hz)
R_{Cout}: Output capacitor Cout serial equivalent resistance (Ω)

Use With Other Settings

1. Use in high output mode
   * Connect the FC terminal to VIN

■ 3X STEP-UP

Only the step-up circuit is made to function and the chip generates a regulated voltage equal to 3 times the input voltage VIN (but in the negative direction), outputting it to the VOUT terminal. However, because the regulator circuit is not used, the voltage at the VOUT terminal includes some ripple component. The figure below shows an example of the connections.



Conditions for Above Figure

- Internal clock: ON (high output mode)
- Step-up circuit: ON
- Regulator: OFF

Power Off Method

- Through setting the POFF2 terminal to "L" level (VIN), all circuits can be turned off.

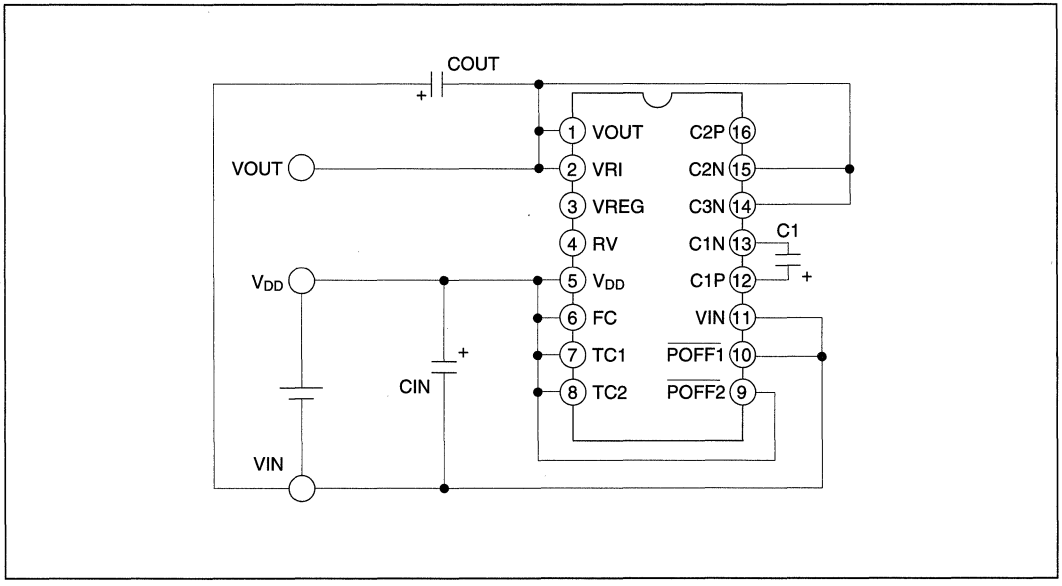
Use With Other Settings

1. Use in high output mode

* Connect the FC terminal to VIN

■ 2X STEP-UP

Only the step-up circuit is made to function and the chip generates a regulated voltage equal to 2 times the input voltage VIN (but in the negative direction), outputting it to the VOUT terminal. However, because the regulator circuit is not used, the voltage at the VOUT terminal includes some ripple component. The figure below shows an example of the connections.



Conditions for Above Figure

- Internal clock: ON (high output mode)
- Step-up circuit: ON
- Regulator: OFF

Power Off Method

- Through setting the POFF2 terminal to "L" level (VIN), all circuits can be turned off.

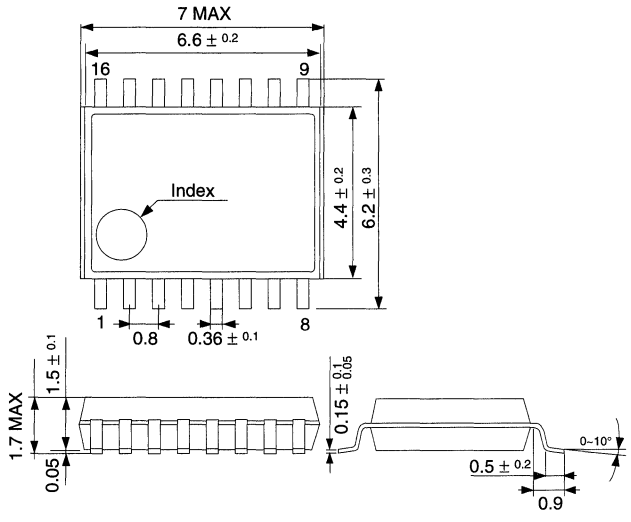
Use With Other Settings

1. Use in high output mode

* Connect the FC terminal to VIN

■ EXTERNAL DIMENSIONS (SCI7654M$_{OA}$)

SSOP2-16



Unit : mm

Note: To allow improvement, these dimensions may change without notice.

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1996 DATABOOK

GRAPHICS PRODUCTS

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PLASMA-DISPLAY/VFD ANODE DRIVER

■ DESCRIPTION

The SED2000FOA/OB is a CMOS LSI dot-matrix plasma-display VFD anode driver. It has 64 high-voltage outputs in 4 × 16 blocks.

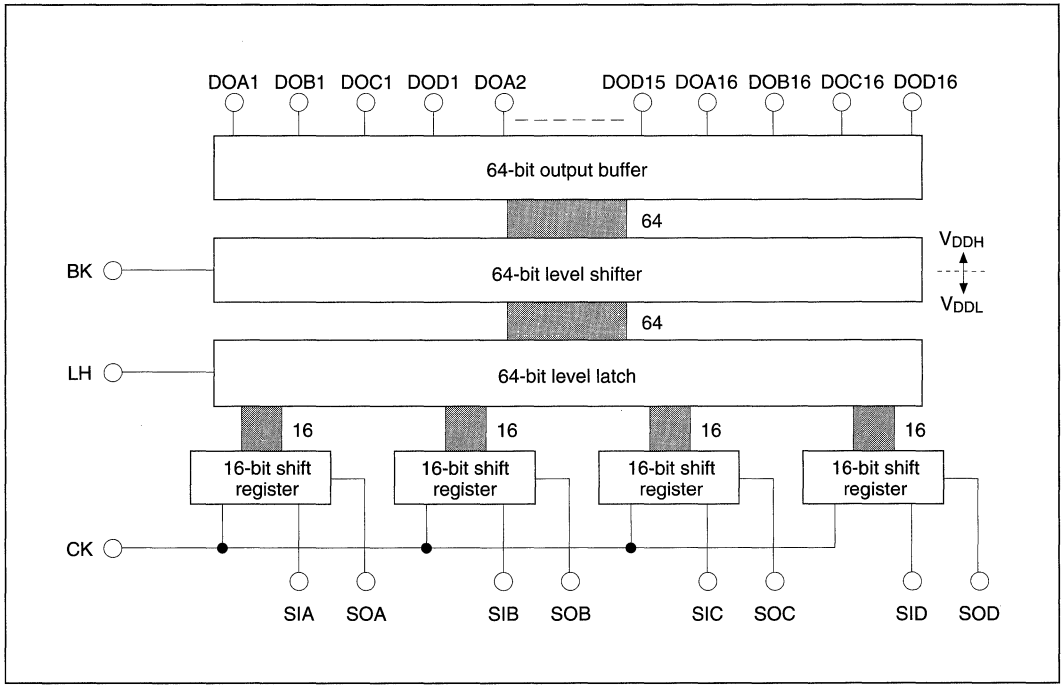
The SED2000FOA/OB has independent serial inputs and outputs for each 16-element block which feature data transfer rates of up to 5 Mbits/s.

SED2000FOA and SED2000FOB are functionally identical except that their pin arrangements are transposed. They use a 5V logic supply and a 30 to 70V display supply, and are available in 80-pin plastic flatpacks.

■ FEATURES

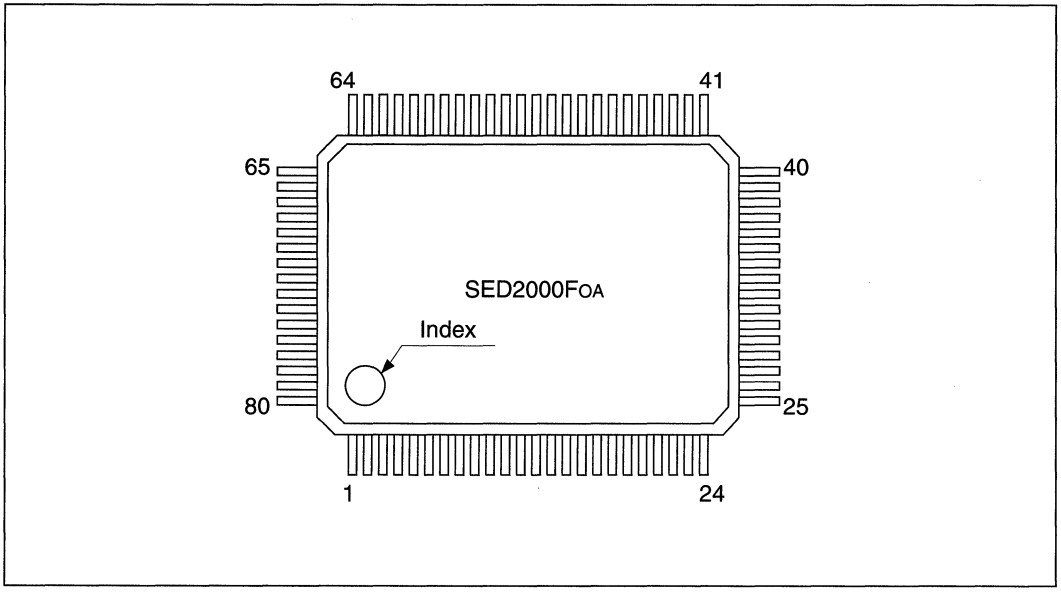
- 64 output drivers
- 70V, 1mA anode drive capability
- Up to 5 Mbits/s data transfer rate (4-bit transfer mode)
- Silicon-gate CMOS technology
- 5V logic supply
- 30 to 70V display supply
- 80-pin plastic flatpack (QFP-80pin) (FOA, FOB)

■ BLOCK DIAGRAM



■ PINOUTS

● SED2000FOA



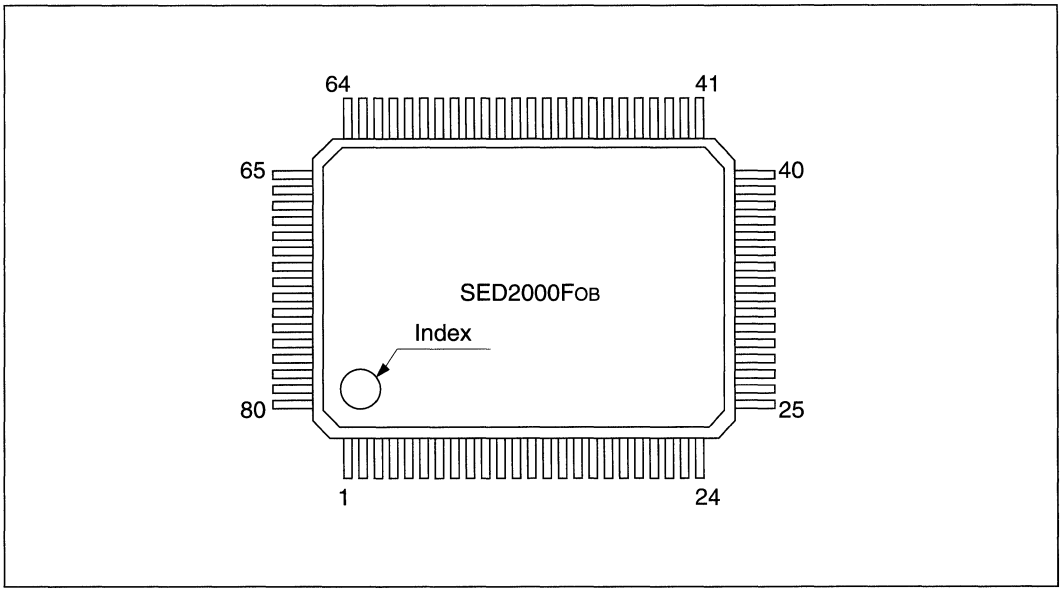
Pin	
Number	Name
1	DOD16
2	DOC16
3	DOB16
4	DOA16
5	DOD15
6	DOC15
7	DOB15
8	DOA15
9	DOD14
10	DOC14
11	DOB14
12	DOA14
13	DOD13
14	DOC13
15	DOB13
16	DOA13
17	DOD12
18	DOC12
19	DOB12
20	DOA12

Pin	
Number	Name
21	DOD11
22	DOC11
23	DOB11
24	DOA11
25	DOD10
26	DOC10
27	DOB10
28	DOA10
29	DOD9
30	DOC9
31	DOB9
32	DOA9
33	DOD8
34	DOC8
35	DOB8
36	DOA8
37	DOD7
38	DOC7
39	DOB7
40	DOA7

Pin	
Number	Name
41	DOD6
42	DOC6
43	DOB6
44	DOA6
45	DOD5
46	DOC5
47	DOB5
48	DOA5
49	DOD4
50	DOC4
51	DOB4
52	DOA4
53	DOD3
54	DOC3
55	DOB3
56	DOA3
57	DOD2
58	DOC2
59	DOB2
60	DOA2

Pin	
Number	Name
61	DOD1
62	DOC1
63	DOB1
64	DOA1
65	VDDH
66	VSS
67	VDDL
68	SIA
69	SIB
70	SIC
71	SID
72	CK
73	LH
74	BK
75	SOD
76	SOC
77	SOB
78	SOA
79	VSS
80	VDDH

● **SED2000FOB**



Pin	
Number	Name
1	DOA1
2	DOB1
3	DOC1
4	DOD1
5	DOA2
6	DOB2
7	DOC2
8	DOD2
9	DOA3
10	DOB3
11	DOC3
12	DOD3
13	DOA4
14	DOB4
15	DOC4
16	DOD4
17	DOA5
18	DOB5
19	DOC5
20	DOD5

Pin	
Number	Name
21	DOA6
22	DOB6
23	DOC6
24	DOD6
25	DOA7
26	DOB7
27	DOC7
28	DOD7
29	DOA8
30	DOB8
31	DOC8
32	DOD8
33	DOA9
34	DOB9
35	DOC9
36	DOD9
37	DOA10
38	DOB10
39	DOC10
40	DOD10

Pin	
Number	Name
41	DOA11
42	DOB11
43	DOC11
44	DOD11
45	DOA12
46	DOB12
47	DOC12
48	DOD12
49	DOA13
50	DOB13
51	DOC13
52	DOD13
53	DOA14
54	DOB14
55	DOC14
56	DOD14
57	DOA15
58	DOB15
59	DOC15
60	DOD15

Pin	
Number	Name
61	DOA16
62	DOB16
63	DOC16
64	DOD16
65	VDDH
66	VSS
67	SOA
68	SOB
69	SOC
70	SOD
71	BK
72	LH
73	CK
74	SID
75	SIC
76	SIB
77	SIA
78	VDDL
79	VSS
80	VDDH

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SED2000FVB

CMOS VFD DRIVER

■ DESCRIPTION

The SED2000FVB is a CMOS LSI dot-matrix vacuum fluorescent display anode and grid driver. It has 40 high-voltage anode outputs in 2 × 20 blocks and 20 high-voltage grid outputs.

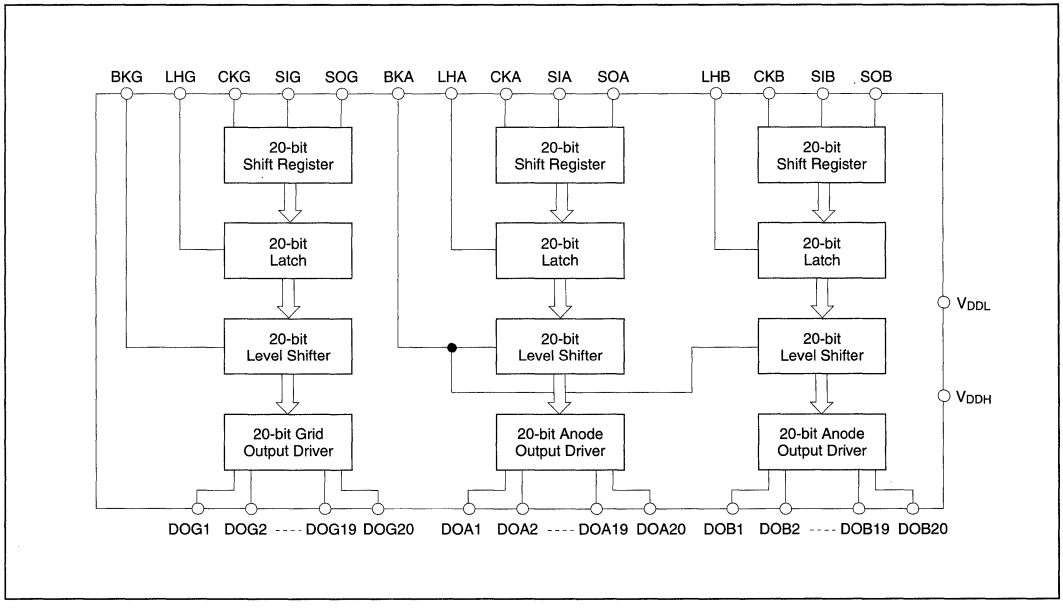
The SED2000FVB has independent serial inputs and outputs for each 20-element block which feature data transfer rates of up to 4 Mbits/s. The daisy-chain serial data transfer system simplifies controller requirements. An automatic shutdown circuit turns off output drivers when power is removed from the logic circuits, simplifying power supply design.

SED2000FVB uses a 5V logic supply and a 30 to 70V display supply, and is available in 80-pin plastic flatpacks.

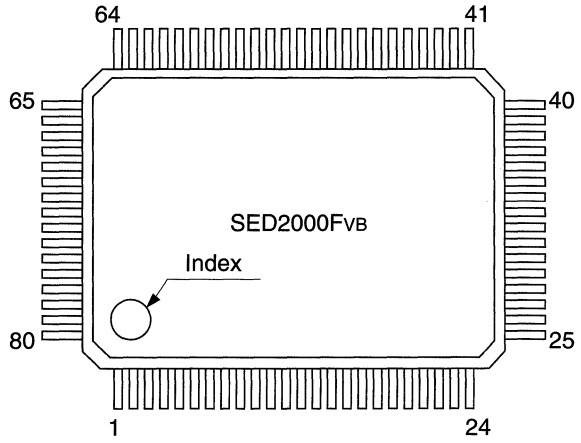
■ FEATURES

- 40 anode and 20 grid output drivers
- 70V, 10mA grid drive capability
- 70V, 2mA anode drive capability
- Automatic shutdown circuit
- Up to 4 Mbits/s serial data transfer rate
- Daisy-chain data transfer system for cascaded operation
- Silicon-gate CMOS technology
- 5V logic supply
- 30 to 70V display supply
- 80-pin plastic flatpack (QFP5-80pin [FVB])

■ BLOCK DIAGRAM



■ PINOUT



Pin	
Number	Name
1	VDDH
2	NC
3	DOB20
4	DOB19
5	DOB18
6	DOB17
7	DOB16
8	DOB15
9	DOB14
10	DOB13
11	DOB12
12	DOB11
13	DOB10
14	DOB9
15	DOB8
16	DOB7
17	DOB6
18	DOB5
19	DOB4
20	DOB3

Pin	
Number	Name
21	DOB2
22	DOB1
23	DOA20
24	DOA19
25	DOA18
26	DOA17
27	DOA16
28	DOA15
29	DOA14
30	DOA13
31	DOA12
32	DOA11
33	DOA10
34	DOA9
35	DOA8
36	DOA7
37	DOA6
38	DOA5
39	DOA4
40	DOA3

Pin	
Number	Name
41	DOA2
42	DOA1
43	DOG20
44	DOG19
45	DOG18
46	DOG17
47	DOG16
48	DOG15
49	DOG14
50	DOG13
51	DOG12
52	DOG11
53	DOG10
54	DOG9
55	DOG8
56	DOG7
57	DOG6
58	DOG5
59	DOG4
60	DOG3

Pin	
Number	Name
61	DOG2
62	DOG1
63	NC
64	VDDH
65	SIB
66	SOB
67	VDDL
68	BKG
69	LHG
70	SOG
71	SIG
72	CKG
73	BKA
74	LHA
75	SOA
76	SIA
77	CKA
78	VSS
79	LHB
80	CKB

SED2020FOA/OB

CMOS VFD DRIVER

■ DESCRIPTION

The SED2020FOA/OB is a CMOS LSI dot-matrix vacuum fluorescent display anode and grid driver. It has 20 high-voltage anode outputs in 2 × 10 blocks.

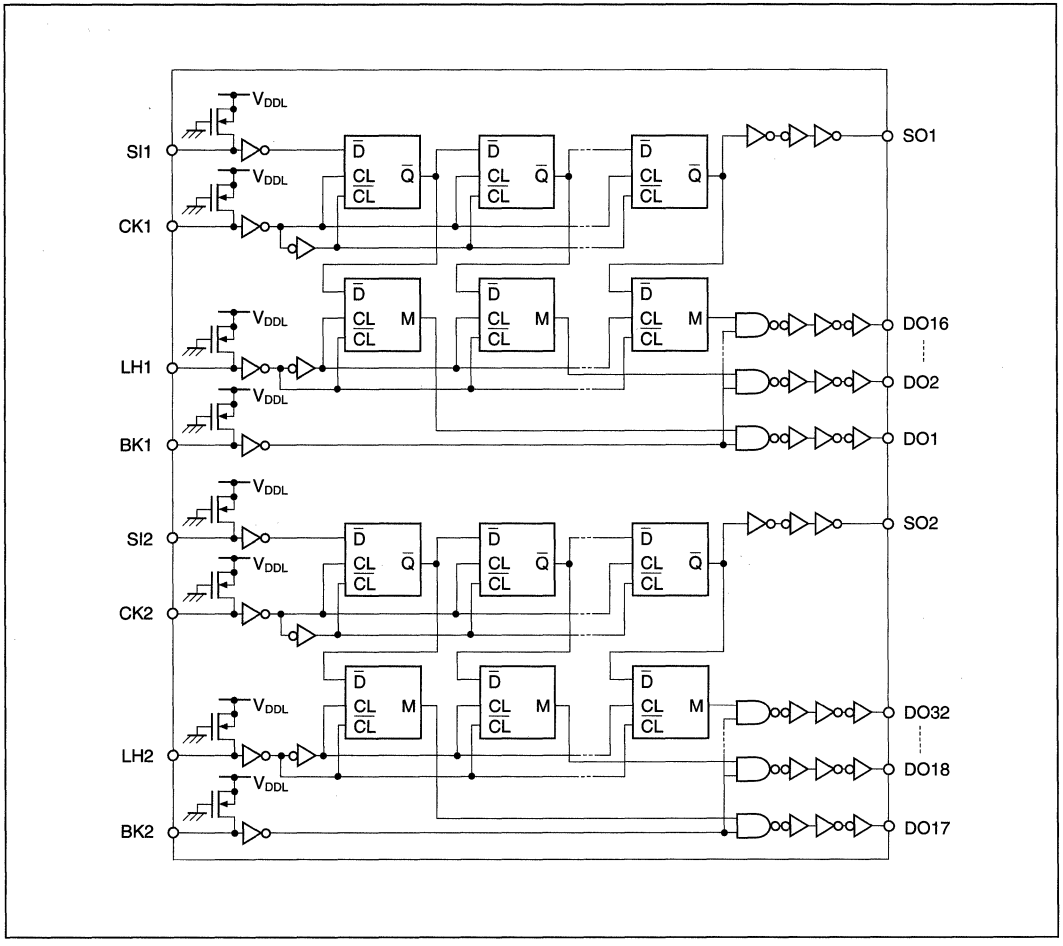
The SED2020FOA/OB is TTL, LSTTL, CMOS and HSCMOS compatible, allowing direct interface to a wide range of standard devices. It has independent serial inputs and outputs for each 10-element block which feature data transfer rates of up to 4 Mbits/s. All inputs have internal pull-ups and serial outputs have a minimum fanout of one standard TTL load. The serial data transfer system simplifies controller requirements. The SED2020FOA/OB can also be configured for 4-bit parallel data transfer.

SED2020FOA/OB uses a 5V logic supply and a 30 to 70V display supply, and is available in 44- or 46-pin plastic flatpacks.

■ FEATURES

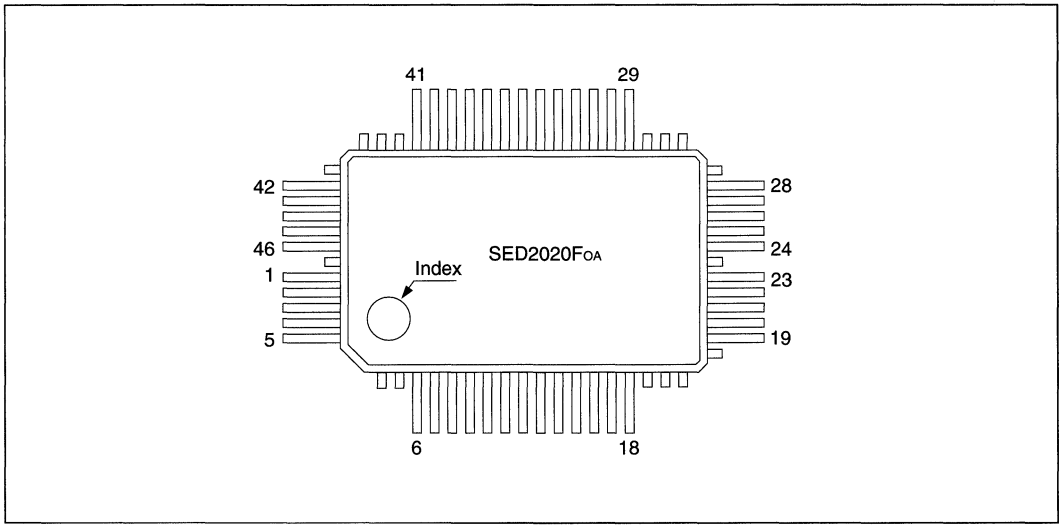
- 20 anode or grid output drivers
- 70V, 10mA grid drive capability
- Up to 4 Mbits/s serial data transfer rate
- Daisy-chain data transfer system for cascaded operation
- Can be configured for 4-bit parallel data transfer
- Silicon-gate CMOS technology
- 5V logic supply
- 30 to 70V display supply
- 44- or 46-pin plastic flatpack (QFP2-44pin [FOB] and QFP1-46pin [FOA])

■ BLOCK DIAGRAM



■ PINOUT

● SED2020FOA



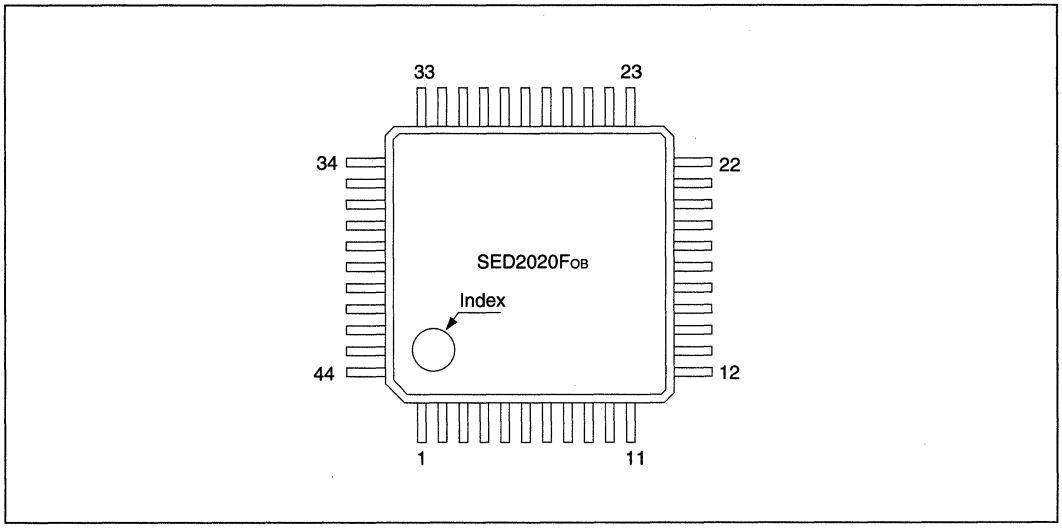
Pin	
Number	Name
1	SI2
2	CK2
3	LH2
4	VDDL
5	VSS
6	VDDH
7	NC
8	DO11
9	DO12
10	DO13
11	DO14
12	DO15

Pin	
Number	Name
13	DO16
14	DO17
15	DO18
16	DO19
17	DO20
18	NC
19	NC
20	NC
21	SO2
22	NC
23	NC
24	NC

Pin	
Number	Name
25	NC
26	SO1
27	NC
28	NC
29	NC
30	DO10
31	DO9
32	DO8
33	DO7
34	DO6
35	DO5
36	DO4

Pin	
Number	Name
37	DO3
38	DO2
39	DO1
40	NC
41	NC
42	BK2
43	BK1
44	LH1
45	CK1
46	SI1

● **SED2020FOB**



Pin	
Number	Name
1	VDDH
2	DO11
3	DO12
4	DO13
5	DO14
6	DO15
7	DO16
8	DO17
9	DO18
10	DO19
11	DO20

Pin	
Number	Name
12	NC
13	NC
14	NC
15	SO2
16	NC
17	NC
18	NC
19	NC
20	SO1
21	NC
22	NC

Pin	
Number	Name
23	DO10
24	DO9
25	DO8
26	DO7
27	DO6
28	DO5
29	DO4
30	DO3
31	DO2
32	DO1
33	NC

Pin	
Number	Name
34	BK2
35	BK1
36	NC
37	LH1
38	CK1
39	SI1
40	SI2
41	CK2
42	LH2
43	VDDL
44	VSS

■ PIN DESCRIPTION

Number		Name	Description
SED2020FOA	SED2020FOB		
1	40	SI2	Serial data input 2
2	41	CK2	Serial data input clock 2
3	42	LH2	Active-HIGH data latch input 2
4	43	VDDL	5V logic supply input
5	44	VSS	Ground
6	1	VDDH	30 to 70V output driver supply input. Referenced to VSS
7	36	NC	No connection
8 to 17	2 to 11	DO11 to DO20	Parallel data outputs
18 to 20	12 to 14	NC	No connection
21	15	SO2	Serial data output 2
22 to 25	16 to 19	NC	No connection
26	20	SO1	Serial data output 2
27 to 29	21, 22	NC	No connection
30 to 39	23 to 32	DO10 to DO1	Parallel data outputs
40, 41	33	NC	No connection
42	34	BK2	Active-HIGH blanking input 2. Used to disable output circuitry while parallel data is being latched.
43	35	BK1	Active-HIGH blanking input 1. Used to disable output circuitry while parallel data is being latched.
44	37	LH1	Active-HIGH data latch input 1
45	38	CK1	Serial data input clock 1
46	39	SI1	Serial data input 1

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SED2032F$_{OB}$

CMOS VFD DRIVER

■ DESCRIPTION

The SED2032F$_{OB}$ is a CMOS LSI dot-matrix vacuum fluorescent display anode or grid driver. It has 32 high-voltage outputs in 2 × 16 blocks.

The SED2032F$_{OB}$ is TTL, LSTTL, CMOS and HSCMOS compatible, allowing direct interface to a wide range of standard devices. It has independent serial inputs and outputs for each 16-element block which feature data transfer rates of up to 4 Mbits/s. All inputs have internal pull-ups and serial outputs have a minimum fanout of one standard TTL load.

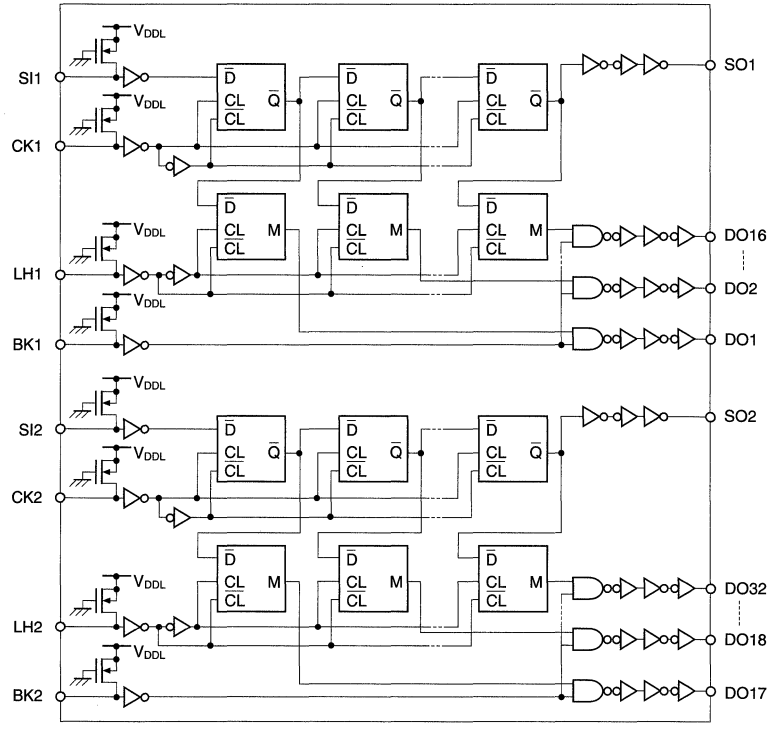
The serial data transfer system simplifies controller requirements. The SED2032F$_{OB}$ can also be configured for 4-bit parallel data transfer.

The SED2032F$_{OB}$ uses a 5V logic supply and a 30 to 70V display supply, and is available in 60-pin plastic flatpacks.

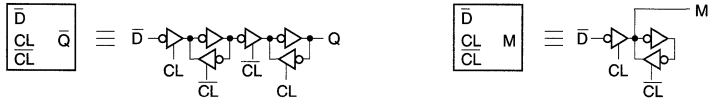
■ FEATURES

- 32 anode or grid output drivers
- 70V, 10mA anode or grid drive capability
- Automatic shutdown circuit
- Up to 4 Mbits/s serial data transfer rate
- Diasy-chain data transfer system for cascaded operation
- Can be configured for 4-bit parallel data transfer
- Silicon-gate CMOS technology
- 5V logic supply
- 30 to 70V display supply
- 60-pin plastic flatpack (QFP2-60pin [F$_{OB}$])

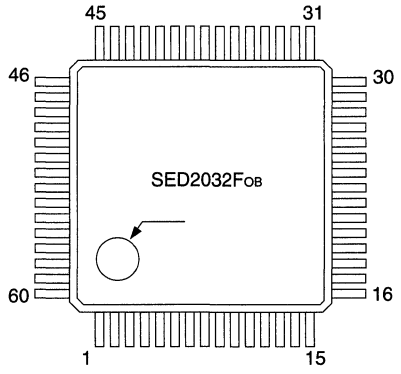
■ BLOCK DIAGRAM



● Internal Circuitry



■ PINOUT



Pin	
Number	Name
1	DO15
2	DO14
3	DO13
4	DO12
5	DO11
6	DO10
7	DO9
8	DO8
9	DO7
10	DO6
11	DO5
12	DO4
13	DO3
14	DO2
15	DO1

Pin	
Number	Name
16	NC
17	NC
18	NC
19	BK2
20	BK1
21	LH1
22	CK1
23	SI1
24	SI2
25	CK2
26	LH2
27	VDDL
28	VSS
29	NC
30	VDDH

Pin	
Number	Name
31	DO17
32	DO18
33	DP19
34	DO20
35	DO21
36	DO22
37	DO23
38	DO24
39	DO25
40	DO26
41	DO27
42	DO28
43	DO29
44	DO30
45	DO31

Pin	
Number	Name
46	DO32
47	NC
48	NC
49	NC
50	NC
51	SO2
52	NC
53	NC
54	NC
55	SO1
56	NC
57	NC
58	NC
59	NC
60	DO16

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GRAPHICS PRODUCTS

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IX. RELATED PRODUCTS

S-MOS carries a line of 4- and 8-bit MCU ICs with built-in LCD drive and control functions, as summarized below. Contact S-MOS for more information.

Part Number SMC	LCD Driver	Voltage Range (V)	Twin Clock	ROM (×12)	RAM (×4)	**I/O	Features	Package *QFP	Available
621A	32 SEG 3/4 COM	2.2 to 3.5	32KHz 455KHz	4096	208	22	Infrared remote control circuit, analog comparator, LCD driver, watchdog timer, SVD	80	Yes
6215 (Previously 6214)	50 SEG 3/4 COM	2.2 to 3.5	32KHz 455KHz	4096	488	25	Infrared remote control circuit, 2 analog comparators, LCD driver, programmable timer, watchdog timer, BLD	100	Yes
621C	34/44 SEG 1–4 COM	2.2 to 5.5	32KHz 455KHz	4096	256	18 (80pin) 24 (100pin)	Resistance to frequency converter, LCD driver, infrared remote control circuit, watchdog timer	80/100	10/94
623A 623LA	20 SEG 3/4 COM	1.8 to 3.5 0.9 to 2.0	N N	1024	80	12	Low cost, stopwatch timer, clock synchronous serial port, LCD driver, SVD	48/60	Yes
6232 62L32 62A32	38 SEG 3/4 COM	1.8 to 3.5 0.9 to 1.7 2.2 to 3.5	N N 32K, 500K	2048	144	21	Event counter, analog comparator, stopwatch timer, LCD driver, watchdog timer, BLD	80	Yes
6233 62L33 62A33	40 SEG 3/4 COM	1.8 to 3.5 0.9 to 1.7 2.2 to 3.5	N N 32K, 500K	3072	256	21	Event counter, analog comparator, stopwatch timer, LCD driver, watchdog timer, BLD, SVD	100	Yes
6235 62L35 62A35	48 SEG 3/4 COM	1.8 to 3.5 0.9 to 1.7 2.2 to 3.5	N N 32K, 500K	4096	576	25	Event counter, 2 analog comparators, stopwatch timer, LCD driver, watchdog timer, sound generator	100	Yes
6237 62L37	26 SEG 3/4 COM	1.8 to 3.5 0.9 to 2.0	N N	1024	80	12	Low cost, stopwatch timer, LCD driver, SVD	60	Yes
624A	40 SEG 8/16 COM	1.8 to 5.5	32 KHz 500K–2M	6144	640	44	Dot matrix LCD driver, external data memory access, watchdog timer, counter, SIO, stopwatch timer	128	Yes
624C (Previously 6214)	51 SEG 8/16 COM	1.8 to 5.5	32KHz 500K–2M	5120	1152	44	Dot matrix LCD driver, external data memory access, watchdog timer, serial port, sound generator	144	Yes
6244	40 SEG 8/16 COM	1.8 to 5.5	32KHz 500K–2M	4096	384	32	Dot matrix LCD driver, watchdog timer, sound generator, SVD, SIO	128	Yes
6247	64 SEG 8/16 COM	0.9 to 3.6	32KHz 200KHz	8192	data 1792 disp 256	48	Dot matrix LCD driver, external memory device control, watchdog timer, serial port	160	Yes
6248	51 SEG 8/16 COM	1.8 to 5.5	32KHz 500K–2M	8192	768	44	Dot matrix LCD driver, external data memory access, watchdog timer, SIO, SVD	144	Yes

(continued)

(continued)

Part Number SMC	LCD Driver	Voltage Range (V)	Twin Clock	ROM (×12)	RAM (×4)	**I/O	Features	Package *QFP	Available
6251 62L51	26 SEG 2-4 COM	1.8 to 3.5 0.9 to 2.0	N N	1024	80	12	Low cost, resistance to frequency converter, LCD driver, SVD, counter, stopwatch timer	60/64	Yes
6256	60 SEG 2-5 COM	1.2 to 3.6	32KHz 1MHz	6144	640	24	2 sensors (2 channels) R/F converters, LCD driver circuit, timebase counter, SVD circuit	Die only	Yes
6262 62L62 62A62	NONE	2.2 to 5.0 0.8 to 3.5 2.2 to 5.0	N N 32K 500K–1M	2048	128	32	No LCD driver, synchronous serial port, programmable timer, watchdog timer, SIO, event counter	44/88	Yes
6266	NONE	2.2 to 3.5	38.4K 500K	6144	1024	40	No LCD driver, asynchronous & synchronous serial ports, 2 analog comparators, watchdog timer event counter, 2 timers, BLD	60	Yes
6274	32 SEG 1-4 COM	2.4 to 5.5	32KHz 500KHz	4096	512	21	Dual slope A/D, stopwatch timer, LCD driver, two op-amps, watchdog timer, SIO	100	Yes
6281 62L81	26 SEG 3/4 COM	1.8 to 3.5 0.9 to 3.5	N N	1024	96	15	Low cost, melody circuit, analog comparator, LCD driver, stopwatch timer, counter, BLD	64	Yes
6282 62L82 62A82	42/38 SEG 4/8 COM	2.2 to 5.5 0.9 to 3.5 2.2 to 3.5	N N 32K, 1M	2048	144	15	Melody circuit, analog comparator, LCD driver, counter, stopwatch timer	80	Yes
62T3	32 SEG 1-4 COM	2.2 to 5.5	N	3072	488	21	DTMF circuit, pulse generator, LCD driver, stopwatch timer, watchdog timer, counter, BLD	80	6/94
6292	22 SEG 2-4 COM	2.2 to 5.5	Y	2048	128	13	LCD driver, supply voltage detector, measure temperature and humidity by external sensor	64	9/94

88316	67 SEG 16 COM	1.8 to 5.5	32KHz 8.2MHz	16K × 8	2K × 8	27	8-bit MCU with dot matrix LCD driver, external program and data memory access, stopwatch timer, watchdog timer, analog comparator	160	Yes w/ Assembler 7/94 C compiler
88112	None	1.8 to 5.5	32KHz 8.2MHz	12K × 8	256 × 8	24	Power generator, voltage detector, MCU built especially for connection external LCD drivers	80	9/94
88308	57 SEG	1.8 to 5.5	32KHz	8K × 8	256 × 8	22	Up to 8.2 MHz (5V) operation 16 levels of LCD contrast controlled by software	160	7/94

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GRAPHICS PRODUCTS

X. QA & PACKAGE INFORMATION

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1. SPECIFICATIONS AND CHARACTERISTICS

1.1 Electrical Characteristics

To fully utilize the CMOS IC it is important to understand the circuit, its characteristics and its specifications. This chapter discusses the absolute maximum ratings, the recommended operating conditions and the electrical characteristics of CMOS integrated circuits.

Please note that the voltage value is based on a high level power supply (V_{DD}) or on a low level power supply (V_{SS}).

1.1.1 Absolute Maximum Ratings

The absolute maximum ratings of a specification are the highest levels at which the circuit will safely operate. Exceeding this level may result in damage to, or destruction of, the circuit. It is, therefore, necessary to monitor such things as supply voltage, input voltage and the ambient temperature.

(1) Operating Voltage

This is the maximum voltage allowed at the power supply terminals. It is important not to let the voltage exceed the specification, not only in the stationary state, but also in the transient state, during power supply turn on, and includes noise on the power supply line. When the voltage exceeds the specification, it may cause some damage to the IC and may adversely effect its reliability.

(2) Input Voltage

This is the maximum voltage allowed into the input terminal. When voltage exceeding the specification is applied, the IC may lose functions because of damage to the input protection resistors or diodes.

(3) Output Current

This is the maximum value of current flow to or from the output. Generally, this is not specified for devices which have small output capacity. This value is provided for ICs, such as drivers which require a large amount of current.

(4) Power Dissipation

This value shows the allowable dissipation for the device. It depends on the thermal characteristics of its package. For devices which must supply large amounts of output, this specifies the limitation of the output current.

(5) Operating Temperature

The ambient temperature range at which the IC will function reliably.

(6) Storage Temperature

The range of storage temperatures when no voltage is being applied on the IC. This is a very important factor, especially during air transportation.

(7) Soldering Temperature and Time

Maximum temperature and time allowed for soldering.

1.1.2 Recommended Operating Conditions

The recommended operating conditions, such as supply voltage, input conditions, and external components, are the conditions necessary for the IC to function properly to meet the electrical characteristics. The operating conditions may be in the same column as the electrical characteristics.

1.1.3 Electrical Characteristics

AC and DC electrical characteristics are provided for each input pin and power supply pin. These characteristics are measured at either the ambient temperature specified or in the range of the operating temperatures specified under the worst conditions.

1.2 Symbol Definitions

SYMBOLS	PARAMETERS	EXPLANATION
C_D	Drain Capacitance	Static capacitance between output terminal and power supply terminal on the oscillation circuit.
C_G	Gate Capacitance	Static capacitance between input terminal and power supply terminal on the oscillation circuit.
C_I	Input Capacitance	Static capacitance between the input terminal and the power supply terminal.
$C_{I/O}$	Input/Output Capacitance	Static capacitance between the I/O terminal and the power supply terminal.
C_L	Loading Capacitance	Loading static capacitance for the external components
C_O	Output Capacitance	Static capacitance between the output terminal and the power supply terminal
f_{xxx}	XXX Frequency	XXX indicates either the function or the terminal name
f_{max}	Maximum Clock Frequency	Maximum Frequency input to the IC from an external pin
f_{CLK}	Clock Frequency	Clock Frequency input to the IC from an external pin
f_{OSC}	Oscillation Frequency	Oscillation Frequency
H	High level	Logical "H" level
I_{DD}	(V_{DD}) Supply Current	Supply current flows into the IC from the V_{DD} external terminal
I_{DDA}	Average Operating Current	Average supply current flows into the IC from the V_{DD} external terminal
I_{DDO}	Operating Supply Current	V_{DD} supply current while operating
I_{DDS}	Standby Supply Current	V_{DD} supply current while standby
I_I	Input Current	Current which flows to the input terminal
I_{LI}	Input Leakage Current	Leakage current which flows to the input terminal
I_{IH}	High Level Input Current	The input current at the "H" level input
I_{IL}	Low Level Input Current	The input current at the "L" level input
I_O	Output Current	Current which flows through the output terminal
I_{OH}	High Level Output Current	Output current when the output terminal voltage is V_{OH}
I_{OL}	Low Level Output Current	Output current when the output terminal voltage is V_{OL}
I_{LO}	Output Leakage Current	Leak current flowed when the power voltage is applied to the output terminal when in the 'off (high impedance)' condition
I_{SS}	(V_{SS}) Supply Current	Current flowed out of the V_{SS} terminal
L	Low Level	Logical "L" level
P_D	Power Dissipation	Allowable consumption of the electric power
R_I	Input Resistance	Built-in resistance for pulling up and pulling down the input
R_L	Loading Resistance	Loading resistance for the external components
T_a	Ambient Temperature	Ambient temperature of the IC
T_j	Junction Temperature	Junction temperature of the IC
T_{opr}	Operating Temperature	Surrounding temperature of the IC in operation
T_{stg}	Storage Temperature	Temperature of storage area the IC
T_{sol}	Soldering Temperature and Time	Soldering temperature and time
V_{DD}	(V_{DD}) Supply Voltage	Supply voltage or the operating voltage applied to the V_{DD} terminal
V_I	Input Voltage	Voltage applied to the input terminal

1.2 Symbol Definitions (cont.)

SYMBOLS	PARAMETERS	EXPLANATION
$V_{I/O}$	Input/Output Voltage	Voltage applied to the I/O terminal
V_{IH}	High Level Input Voltage	Input voltage which can be judged as "H" level
V_{IL}	Low Level Input Voltage	Input voltage which can be judged as "L" level
V_O	Output Voltage	Voltage generated from or applied to the output terminal
V_{OH}	High Level Output Voltage	Voltage at the "H" level output
V_{OL}	Low Level Output Voltage	Voltage at the "L" level output
V_{rip}	Ripple Voltage	Ripple voltage Amplitude
V_{SS}	(V_{SS}) Supply Voltage	Supply voltage applied to the V_{SS} terminal
V_{SSn}	V_{SSn} Supply Voltage	N times pressurized power supply terminal or its voltage level
V_{STA}	Oscillation Start Voltage	Voltage for automatic starting
V_{STP}	Oscillation Stop Voltage	Voltage when oscillation stops
—	"H", "L" or High Impedance	Unfixed or unprovided level or high impedance
X	"H" or "L"	Unfixed or unprovided level
Z	High Impedance	High impedance condition in three states
t_a	Access Time	Time between the input of prescription and the output of the valid data
t_{ACC}	Address Access Time	Time required for obtaining the output of valid data after the address is given
t_{ACE}	Chip Enable Access Time	Time required for obtaining the output of the valid data after the chip enable signal is given
t_{ACS}	Chip Select Access Time	Time required for obtaining the output of the valid data after chip select signal is given
t_C	Cycle Time	Time from the start point of a complete operation to the start point of the next operation
t_{RC}	Read Cycle Time	Time required for one read cycle
t_{WC}	Write Cycle Time	Time required for one write cycle
t_f	Fall Time	Time required for the signal changed from "H" to "L"
t_h	Hold Time	Time required for the synchronous input to be held stable after the active clock edge
t_{DH}	Data Hold Time	Time required for the data input to be held stable after the active clock edge
t_{AH}	Address Hold Time	Time required for the address input to be held stable after the active clock edge
t_{OE}	Output Enable Delay Time	Time required for obtaining a valid output data after the output enable signal is given
t_{OH}	Output Hold Time	Time required for the output data to be held stable after the active clock edge
t_{pd}	Propagation Delay Time	Delay time between the active clock edge and the output change
t_{pHL}	Low Level Propagation Time	Delay time between the active clock edge and the output change from High to Low
t_{pLH}	High Level Propagation Time	Delay time between the active clock edge and the output change from Low to High
t_r	Rise Time	Time for changing the signal from Low to High
t_{su}	Set-up Time	Time required for the synchronous input remained stable before the next clock edge
t_{AS}	Address Set-up Time	Time required for the address input remained stable before the next clock edge
t_{DS}	Data Set-up Time	Time required for the data input remained stable before the next clock edge
t_{PW}	Pulse Width	Pulse width
t_{RP}	Read Pulse Width	Pulse width of the read signal
t_{WP}	Write Pulse Width	Pulse width of the write signal
t_{WR}	Write Recovery Time	Same as the address hold time t_{AH}

2. QUALITY ASSURANCE

S-MOS Systems, Inc., supported by the foundation of results acquired through experience in the adoption of low-power CMOS LSI for SEIKO quartz watches, has been providing highly reliable products that have set new standards in the industry.

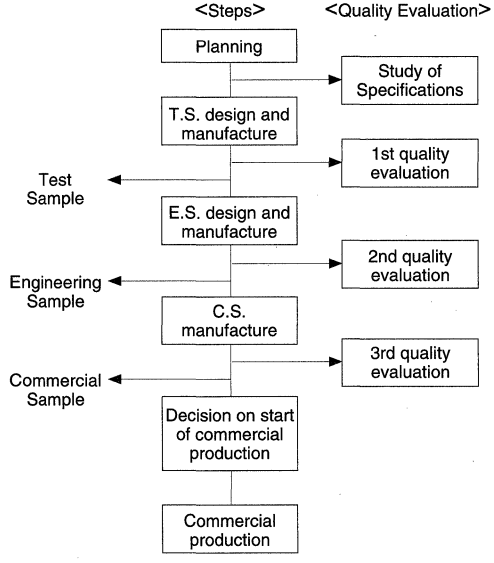
Today extremely high reliability is demanded of our customers' products. In step with this trend, extremely high reliability is demanded of semiconductor components.

To meet this demand in the market, we utilize a product quality assurance program which guarantees the highest quality in our products.

Our quality assurance program is as follows:

2.1 Quality Assurance System for Development of New Products

Our quality assurance efforts begin with a market survey to determine the user's specific needs. After the survey is completed, an analysis is made. Based on this analysis, an initial design is made. Next the initial design goes through prototype production and quality evaluation stages. Once these steps are completed, a new product, made according to the user's specifications is created. Fig. 2-1 shows the typical stages of new product development from initial planning to commercial production.



- Test Data, Field Data and Process Capabilities are used to compare the preliminary specs with the user's requirements. Market potential is also checked at this time.
- The test sample is evaluated for basic design capabilities and for conformance to the product specifications.
- The engineering sample is evaluated for quality assurance within the scope of the manufacturing conditions.
- The Production Sample is evaluated to determine if the quality level is achievable with the equipment available and under the existing manufacturing conditions.

Fig. 2-1 New Product Development Flow

2.1.1 Design

Market surveys are done so the designers know the exact specifications required by the user. Based on the information received, designs for the projected product are made. A "reliability" design is made using the data from reliability tests, field quality studies, past problems and available quality or reliability related information. Design staffs are given the purpose, environment and other factors relating to the application of a product to aid in its design.

2.1.2 Quality Evaluation

The quality evaluation is in two parts, the design evaluation and the reliability evaluation. The design evaluation determines if the target functions and performance level have been reached. The reliability evaluation verifies that long term quality is assured.

The reliability evaluation is done based on the particular objectives of the product. The evaluation is carried out under pre-established guidelines. It is performed according to EIAJ-IC-121 (Electronics Industries Association) standards and with MIL-STD-750B/883C and JIS-C7021 (Japanese Industrial Standards) where applicable. The application, environment and uniqueness of the manufacturing process are also taken into consideration.

2.1.3 Decision to Start Commercial Production

The decision is made whether or not to start commercial production after the sample or prototype production and quality evaluation are completed. This decision is based upon production capabilities, data verification on yield, reliability test results and the user's evaluation of the engineering sample.

2.2 Quality Assurance Systems for Commercial Production

Quality and reliability are assured by design checks in the Engineering and Manufacturing Departments and with verification of the finished product. Once in commercial production, quality control checks are made at various stages. Quality control begins at the assembly line. Inspections follow during the intermediate and final processes, ending with the shipping inspection. A quality assurance flow chart is shown in Fig. 2-2.

2.2.1 Manufacturing Environment Control

Due to the sensitive nature of semiconductor devices, extreme care must be used during the manufacturing process. The manufacturing is done in a "clean room" where temperature, humidity and dust are carefully monitored and controlled.

2.2.2 Control of Manufacturing and Measuring Equipment

Important elements of building reliability into a product are maintaining and controlling the manufacturing and measuring equipment. This equipment is used to monitor and control line conditions and/or to do intermediate inspections. With the evolution of devices to higher integrations and improved reliability, the production process must be controlled at a higher level. Routine checks and periodic inspections insure that we achieve these high standards.

2.2.3 Process Inspection

Quality Assurance is based on the theory that quality is built into the product. The inspection at each processing stage assures high quality. The inspection results are fed back into each process in order to stabilize the entire operation. These inspections also prevent defective parts from moving to the next process stage.

Figs. 2-3 and 2-4 show typical wafer process and assembly flow.

2.2.4 Shipping Inspection

The final inspection is performed when the product is ready to ship to reverify that the product meets our high standards. The electrical characteristics are 100% tested, and the environmental characteristics are tested on a lot sample basis. External visual inspection is also performed.

The shipping inspection is performed according to the category of the product. An example of the inspection process is shown in Table 2-1.

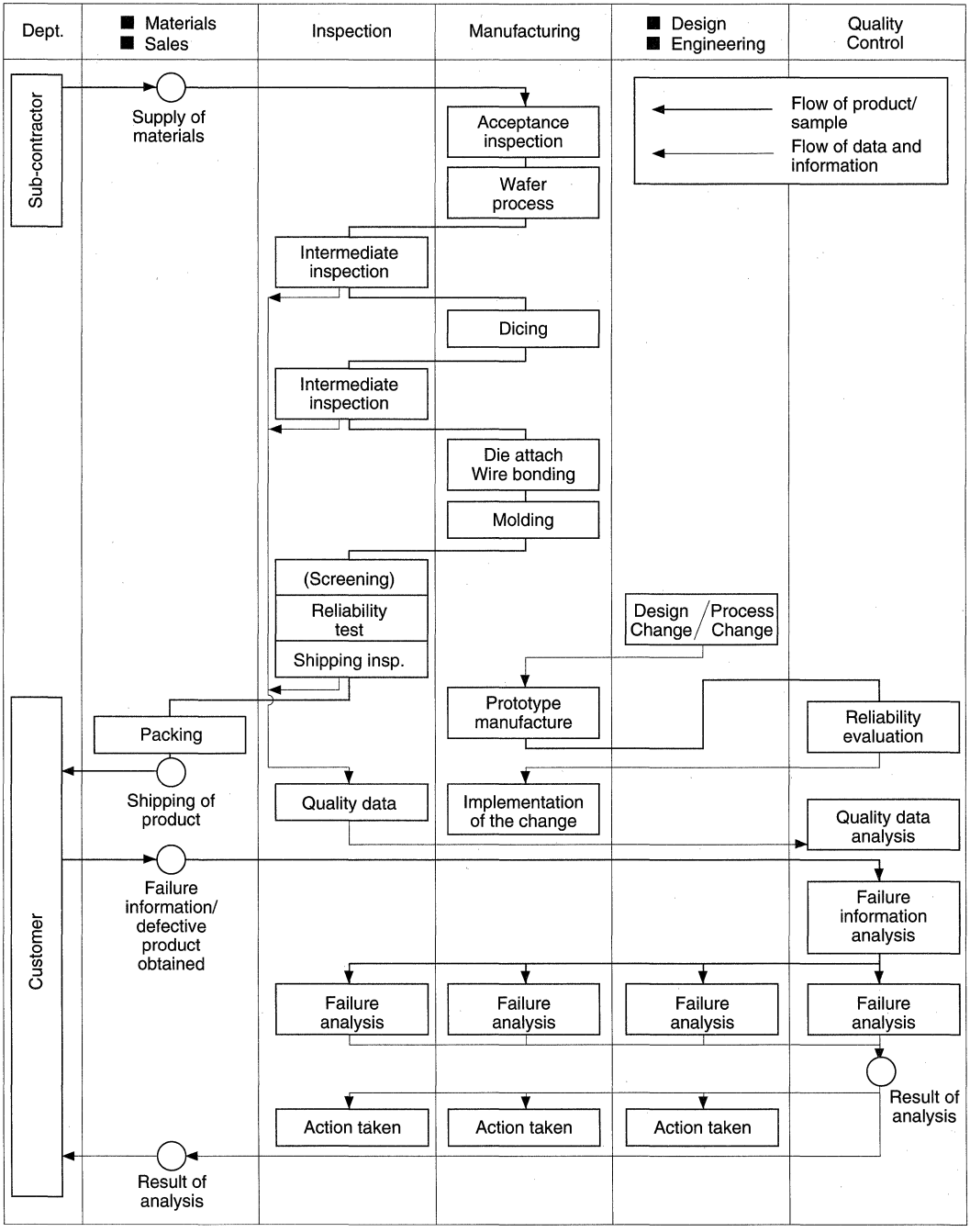


Fig. 2-2 Flow of Quality Assurance Activities in Commercial Production

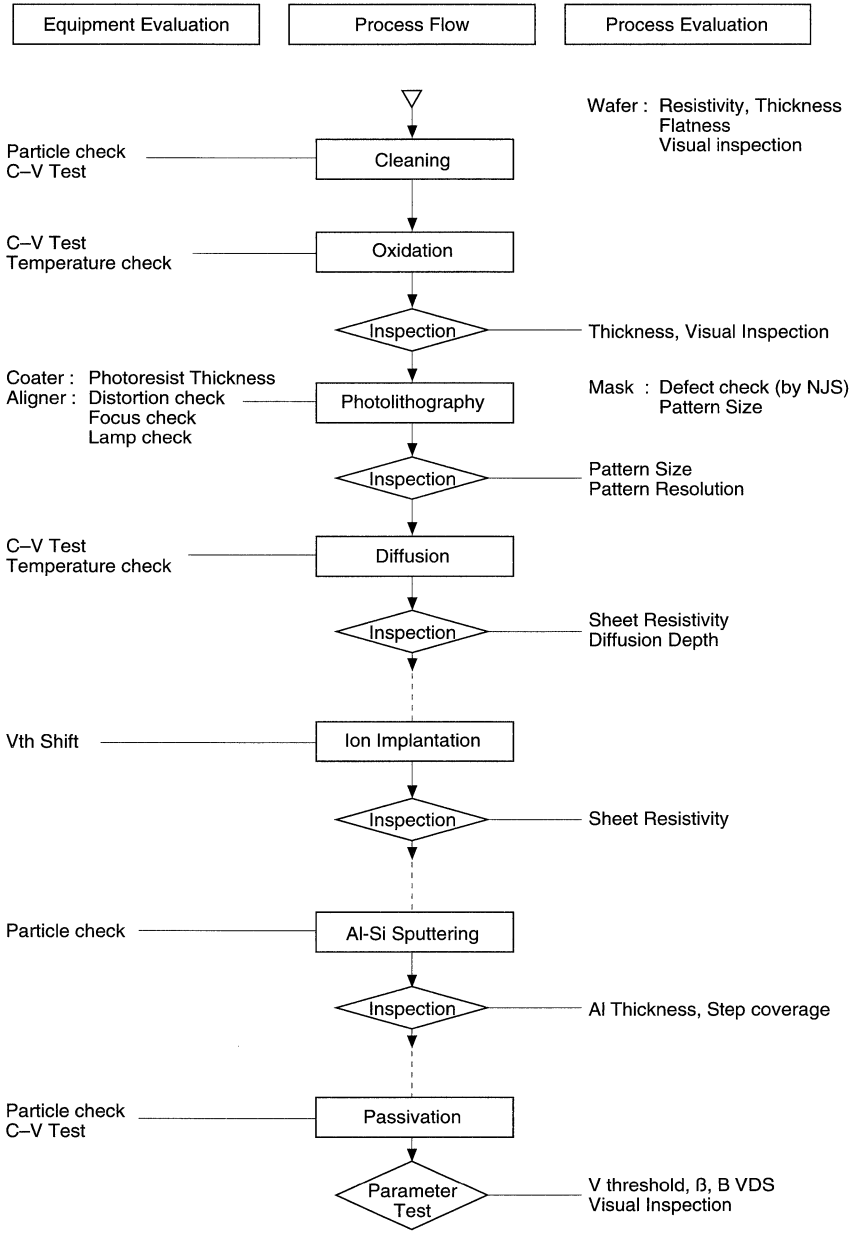


Fig. 2-3 Quality Assurance System for Wafer Production

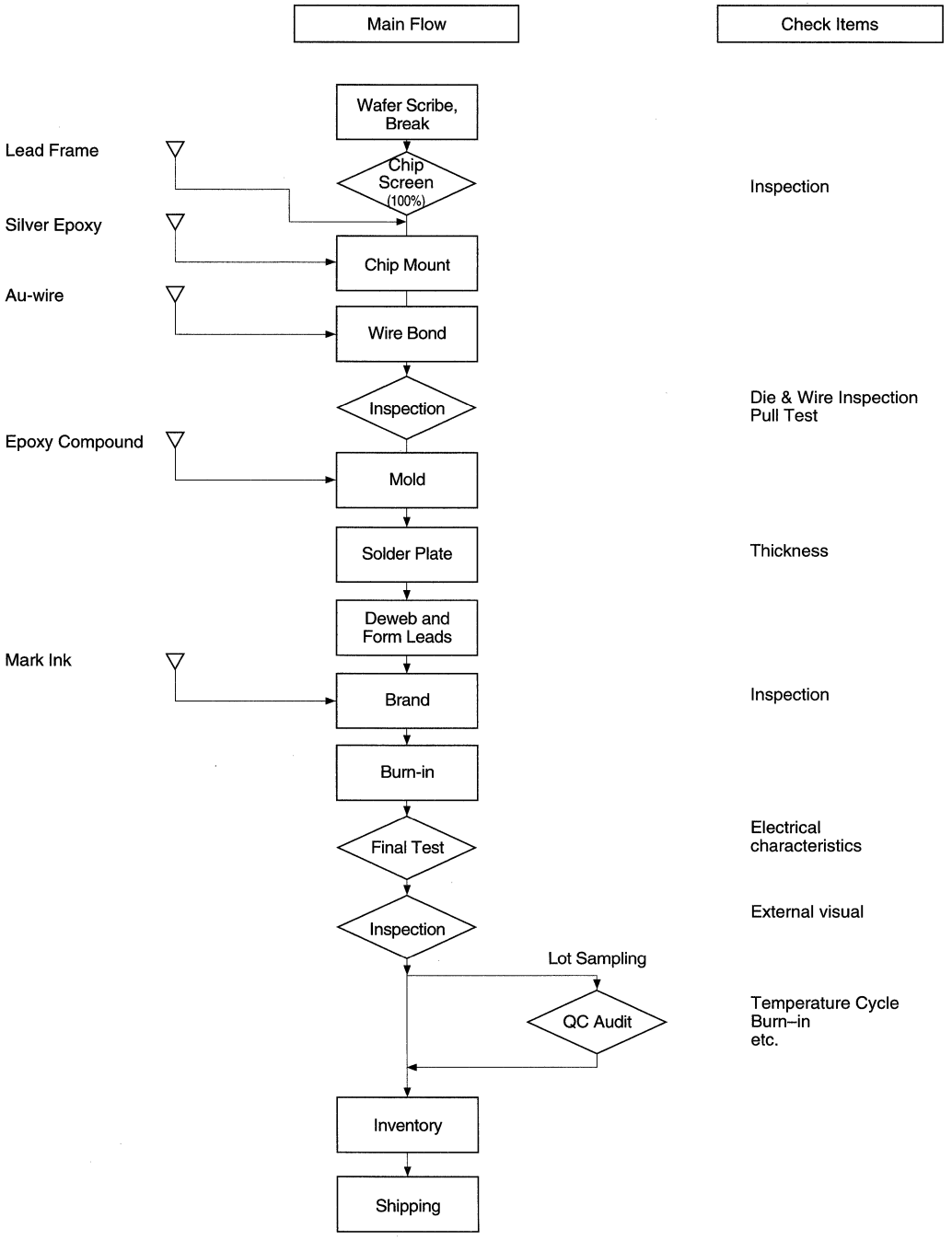
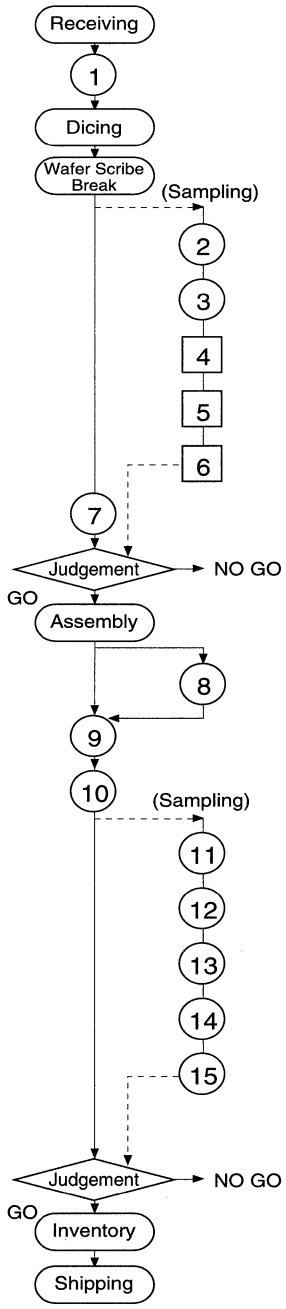


Fig. 2-4 Plastic Package Assembly Flowchart

Table 2-1 Example of Shipping Inspection

○ : Each lot is inspected for quality assurance.
□ : Specific lot is inspected to understand process levels.



Shipping Inspection for Pellet

No.	Process	Control Point	Standard condition (method)
1	Electrical characteristics (100%)	Wafer process	Determined by product type
2	Resistance to heat	↑	Exposed to high temperature for short time
3	Bondability	↑	Wire pull Die shear strength
4	Electrical characteristics/	↑	Determined by product types
5	Temperature cycle	↑	-55°C to 125°C (for 30 Min. at each temperature)
6	High temperature with bias	↑	125°C with Max. rated voltage applied
7	Visual inspection	Wafer process/ inspection process	Microscope

Shipping Inspection for Plastic package

No.	Process	Control Point	Standard condition (method)
8	Screening	Wafer process/ Assembling process	Burn-in Determined by product types
9	Electrical characteristics (100%)	↑	Determined by product types
10	Visual inspection (100%)	Assembling process	Visually checked
11	Temperature cycle	↑	-55°C to 125°C (for 30 minutes at each temperature)
12	Electrical characteristics/ Visual inspection	Wafer process/ Assembling process	Determined by product types/ visually checked
13	High temperature with bias	↑	125°C with Max. rated voltage applied
14	Pressure cooking	Assembling process	2 atmospheric (vapor) pressure (at 121°C)
15	Moisture resistance (with bias)	Wafer process/ Assembling process	85°C, 85% RH with Max. rated voltage applied

2.3 Reliability Testing

The reliability test includes environmental testing, life testing and mechanical testing. These tests are made in accordance with EIAJ-IC-121 as the prime standard, and with MIL-STD-750B/883C and JIS where applicable. The way the product is used, the application and the environment in which the product is operated are some of the factors taken into consideration when the conditions are set for the reliability test. It is important to conduct tests of new products under conditions that simulate how the product is to be used. In addition, standard tests are performed.

Table 2-2 summarizes the reliability test items and the factors associated with defects. Table 2-3 gives an example of typical conditions for reliability testing.

Table 2-2 Reliability Test Items and Factors Associated with Defects

Factors associated with defects / Reliability test items	Junction isolation	Oxides	Metallization	Passivation	Die bonding	Wire bonding	Seal	Lead integrity	Solderability	Marking
High temperature bias	○	○	○	○	○	○	○			
High temperature storage	○	○	○	○		○	○			
Low temperature storage						○	○			
Boil	○	○	○	○	○	○	○			
Temperature cycle	○	○	○	○	○	○	○			
Mechanical shock						○	○	○		
Salt atmosphere							○	○	○	○
Thermal shock		○	○	○	○	○	○			
Vibration variable frequency			○		○	○				
Vibration constant frequency			○		○	○				
Lead integrity								○		
Bond strength			○		○	○				
Resistance to solvents							○			○

Table 2-3 Typical Conditions for Reliability Test

Test items		Test Method		Purpose of test
		Reference standard	Test conditions	
Environmental test	Temperature cycle	EIAJ-IC-121 04 MIL-STD-883C 1010•5	-65°C to 150°C 100 cycles	Checks resistance to high and low temperatures, and varying temperatures
	Thermal shock	EIAJ-IC-121 03 MIL-STD-883C 1011•4	0°C to 100°C 10 cycles	Checks resistance to rapid temperature changes
	High temperature storage	EIAJ-IC-121 15 MIL-STD-883C 1008•2	t_a=150°C 1,000 hours	Checks resistance to heat when exposed to high temperature
	Low temperature storage	EIAJ-IC-121 16	t_a= -65°C 1,000 hours	Checks resistance to cold when exposed to low temperature
	Moisture resistance	EIAJ-IC-121 17	t_a=85°C, 85% RH 1,000 hours	Checks resistance to long-time operation and storage in the environment with high relative humidity
	Salt atmosphere	JIS-C7021 A-12 MIL-STD-202E 101D	35°C, 5% brine spray, 48 hours	Checks resistance to corrosion through acceleration test with coastal environment simulated atmosphere
	Pressure cooker	EIAJ-IC-121 18	2 atmospheric pressures (121°C) 96 hours	Checks resistance to accelerated humidity changes
	Resistance to soldering heat	EIAJ-IC-121 01	260°C, 10 seconds (solder bath)	Checks resistance to heat during soldering
	Resistance to solvents	EIAJ-IC-121 14 MIL-STD-883C 2015•4	Freon Trichloroethylene 10 minutes	Checks resistance of printed marking to solvent
Life test	High temperature steady state	EIAJ-IC-121 51 MIL-STD-883C 1005•4	t_a=125°C (steady operation) 1,000 hours	Checks resistance to electrical stress and thermal stress applied for extended time periods
	Moisture resistance (with bias)	EIAJ-IC-121 17	T_a=85°C, 85% RH (rated voltage applied) 1,000 hours	Checks resistance to long-time use with high relative humidity

(continued)

Table 2-3 Typical Conditions for Reliability Test (cont.)

Test items		Test Method		Purpose of test
		Reference standard	Test conditions	
Mechanical test	Vibration variable frequency	EIAJ-IC-121 10 MIL-STD-883C 2007•1	100 Hz to 2,000 Hz 4 minutes/back and forth 4 times each for X, Y and Z (at 20G)	Checks resistance to vibration during transportation or operation
	Vibration fatigue	EIAJ-IC-121 10 MIL-STD-883C 2005•1	60 Hz 20G 32 hours each for X, Y and Z	Checks resistance to vibration during transportation or operation
	Mechanical shock	EIAJ-IC-121 08	1,500G 3 falls each for X, Y and Z	Checks resistance to shocks applied when the product is being handled, transported or operated
	Lead integrity	EIAJ-IC-121 11 MIL-STD-883C 2004•4	Tension 1.0 kg 10 seconds (DIP) Tension 0.3 kg 10 seconds (FP)	Checks resistance to forces to which the lead is subject during installation or operation
		EIAJ-IC-121 11 MIL-STD-883C 2004•4	Bend 90° 2 cycles: 42 Alloy	
	Solderability	EIAJ-IC-121 02 MIL-STD-202E 208C	230°C, 5 seconds flux used	Checks solderability to leads

2.4 Defective Product Policy

S-MOS Systems requests the user to return defective products. It is important to S-MOS that when a problem arises it be brought to our attention. Any product information, positive or negative, is valuable data which enables us to improve the quality of our product.

We will make a thorough investigation of the problem with the user's assistance. Where the problem occurred, how it developed and any other related information will be reviewed. The product's manufacturing process and reliability test data will also be reviewed.

The Quality Control Department will check all available information for solutions to prevent the problem from happening in the future. Quality Control will report the results of the investigation to the user through the Sales Department. The Manufacturing Department will be given the report so corrective action can be taken as necessary.

Fig. 2-5 shows that RMA (Returned Material Authorization) process.

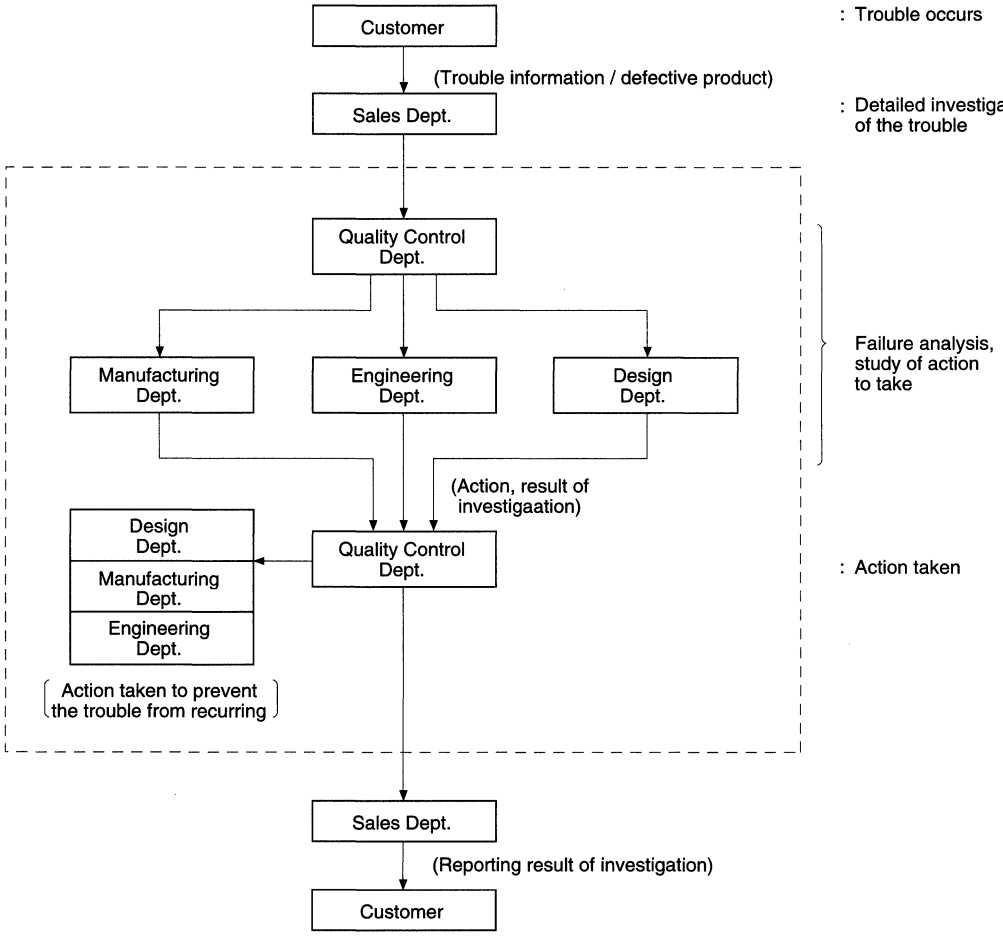


Fig. 2-5 Route of Actions against Trouble Occurring outside the Company

2.5 Operating Precautions

S-MOS System's plastic molded CMOS LSI devices are designed and manufactured for trouble free operation when used under normal operating conditions. Our products are subjected to stringent electrostatic, mechanical strength, and environmental tests for assured reliability. When working with our product the user should observe the following precautions:

(1) Use the product in the range of rated operating voltage, operating temperature, operating input/output voltage and input/output current. If the product is used outside these operating parameters, the user may experience high failure rates.

(2) Excessive electrical noise applied to the power or input pin of the device could cause it to latch up, resulting in malfunction or damage. If this occurs, turn the power off immediately, isolate the problem and turn the power on again.

(3) Do not expose the product to excessive mechanical vibration, repetitive shock stress, rapid or cyclic temperature changes. These factors can cause the wires in the plastic package to break.

(4) Although all terminals have electrostatic protection, damage may still occur if very high electrostatic potentials are applied. Use of a conductive container or aluminum foil for packaging and transportation is recommended. (Untreated plastic containers are NOT recommended.) Use grounded soldering tools and test equipment.

2.6 Solder-reflow Process of Plastic Flat Packages

During the solder-reflow process, the plastic flat package is exposed to high temperatures (such as far-infrared) inside the reflow furnace. Therefore, the following precautions should be observed when packages are in the solder-reflow process:

(1) Maintain the maximum temperature of the resin of the package at 245°C for not more than 10 seconds.

(2) Maintain the outer surface of the reflow furnace temperature (resin surface temperature) at the curve shown in Fig. 2-6.

(3) The resin on plastic flat packages is prone to absorb moisture. Even at room temperature, the amount of moisture absorbed increases with time. If a wet package is put in the solder-reflow furnace, the resin may crack or the adhesiveness of the resin to the frame may be decreased.

(4) Items (1) through (3) are intended as a guideline based on our laboratory experience and are for reference only since packages will be stored in different environments and different types of reflow furnaces will be used. Thus, it is important that packages be checked for quality at the solder-reflow process before entering mass production.

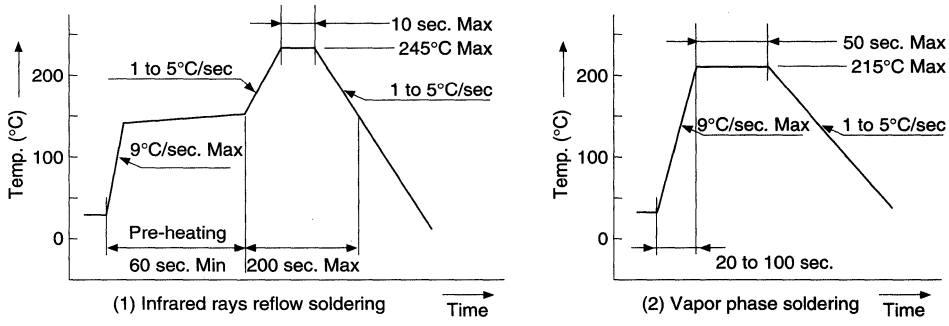


Fig. 2-6 Reflow Furnace Temperature Curve

2.7 Package Storage Guidelines

(1) Packages should be stored in the recommended environment. Maximum storage conditions for temperature and humidity are shown in Table 2-6.

(2) Packages which exceed the storage limits specified in Table 2-6, or which have absorbed too much moisture due to high temperature or high humidity, should be baked before the reflow process. The recommended procedures for drying the packages are shown in Table 2-7. This drying process will prevent the resin from cracking during the reflow process.

Table 2-6 Maximum Storage Conditions for Surface Mount Component (SMC)

PLASTIC FLAT PACKAGE & SOP

Storage Conditions		Allowable period
Before open dry-pack (≤35°C)		6 month
After open dry-pack	25°C, 60%	1.5 month
	30°C, 80%	12 day
	35°C, 90%	3 day (72 hour)

PLASTIC PLCC

Storage Conditions		Allowable period
Before open dry-pack (≤35°C)		6 month
After open dry-pack	25°C, 60%	2 month
	30°C, 80%	12 day
	35°C, 90%	3 day (72 hour)

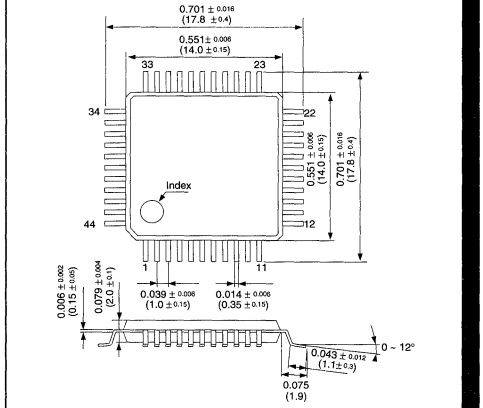
Table 2-7 Dryout conditions for SMC

Package type \ Temperature	125°C	150°C
PLASTIC QFP, SOP	5 hour	2 hour
PLASTIC PLCC	20 hour	8 hour

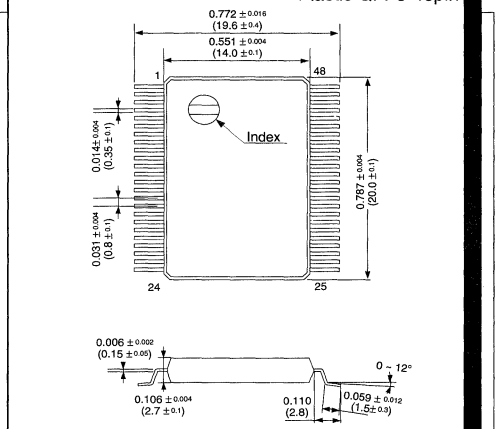
Unit: inch (mm)

Plastic QFPs

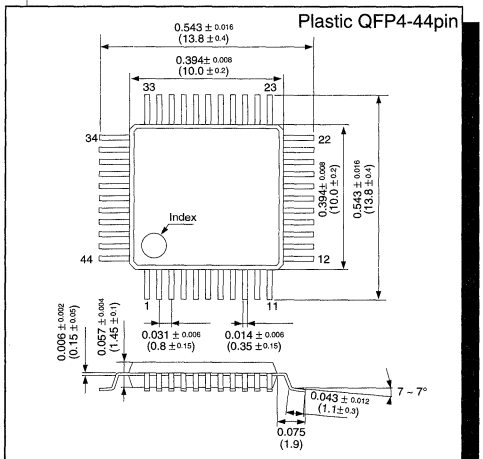
Plastic QFP2-44pin



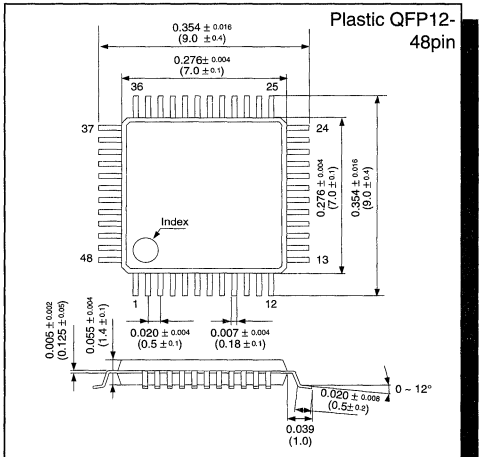
Plastic QFP5-48pin



Plastic QFP4-44pin



Plastic QFP12-48pin



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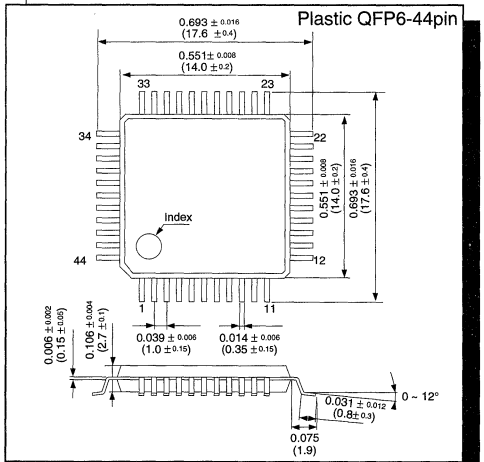
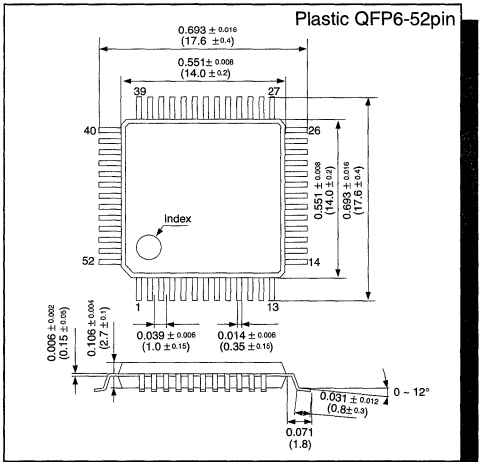


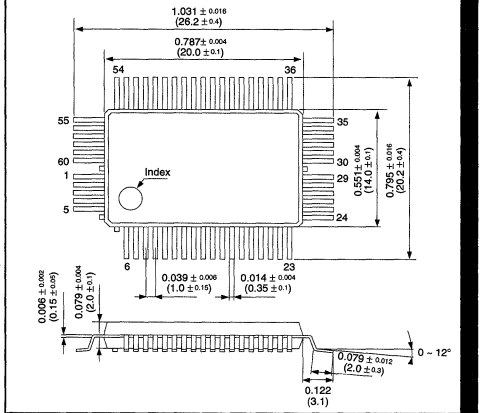
Plastic QFP6-52pin



Unit: inch (mm)

Plastic QFPs

Plastic QFP1-60pin



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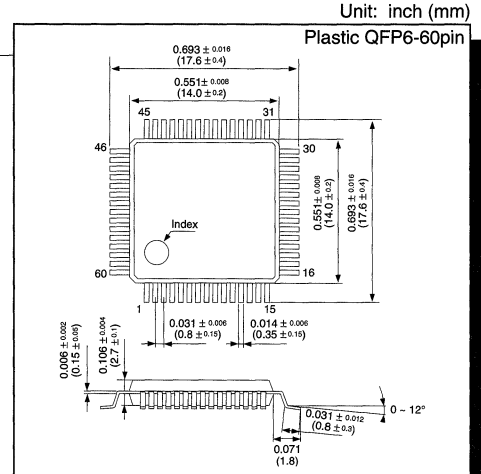
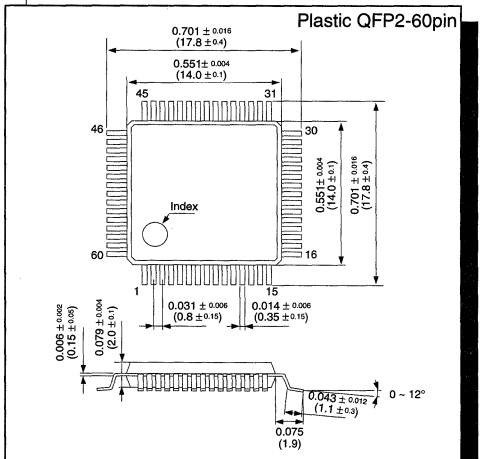
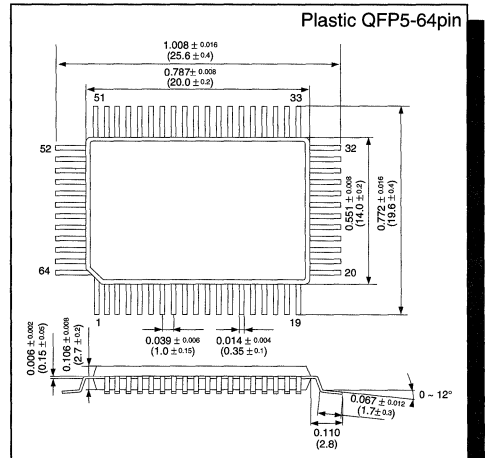


Plastic QFP2-60pin



Plastic QFP5-64pin



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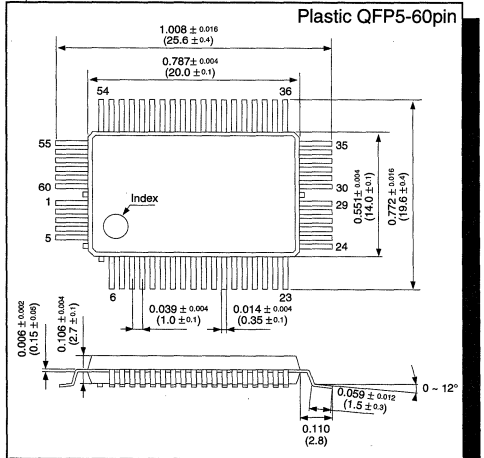
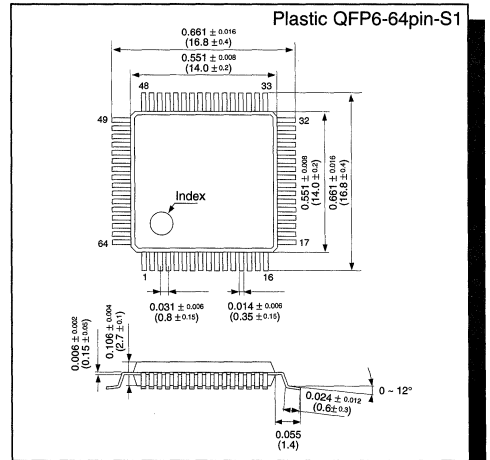


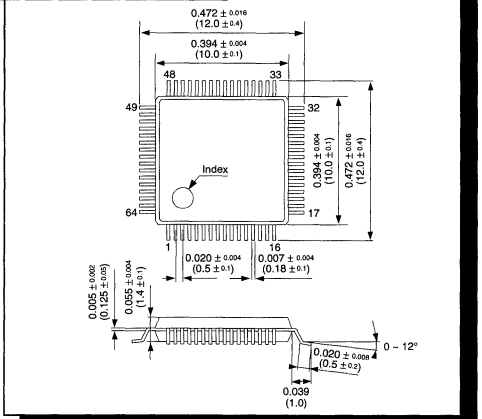
Plastic QFP6-64pin-S1



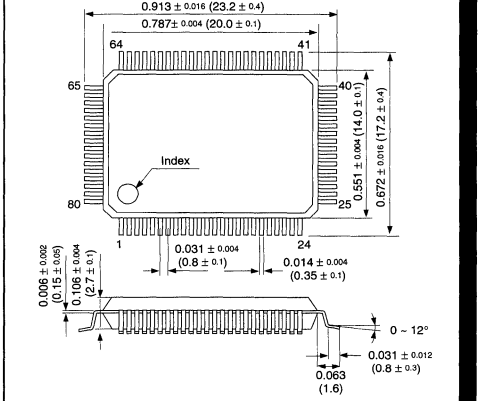
Unit: inch (mm)

Plastic QFPs

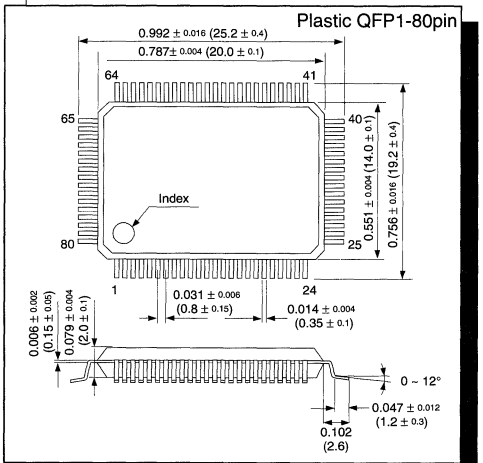
Plastic QFP13-64pin



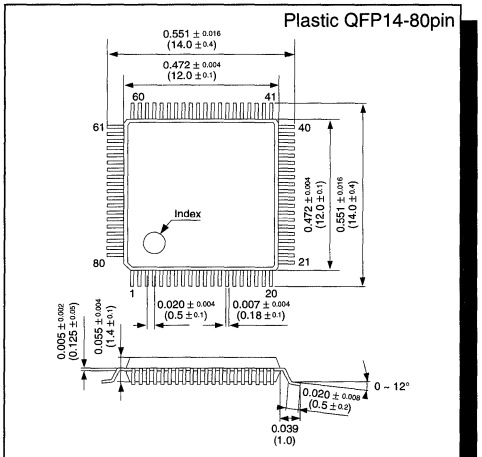
Plastic QFP5-80pin-S2



Plastic QFP1-80pin



Plastic QFP14-80pin



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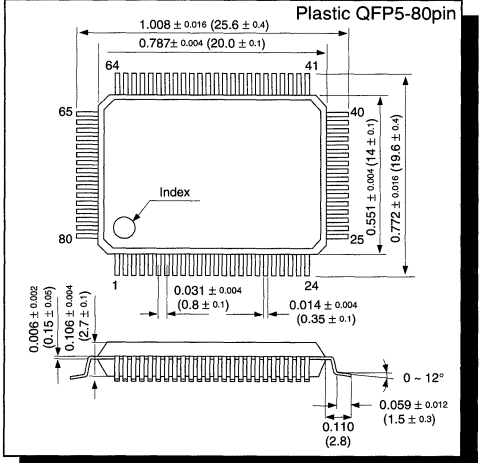

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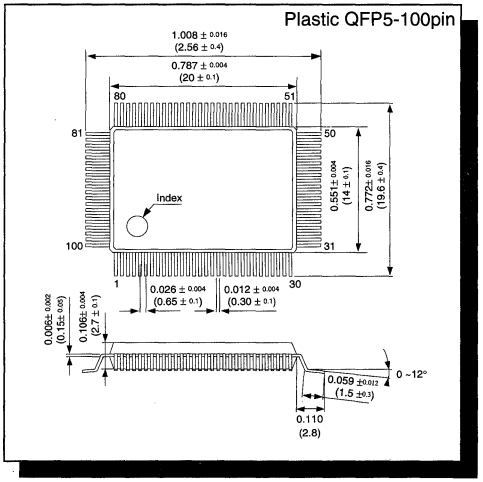
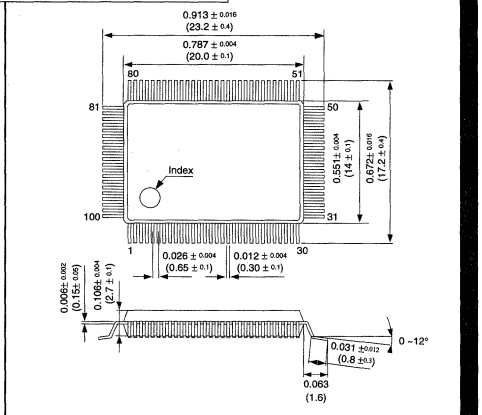


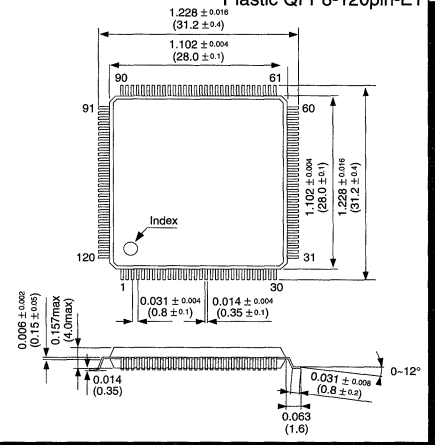
Unit: inch (mm)

Plastic QFPs

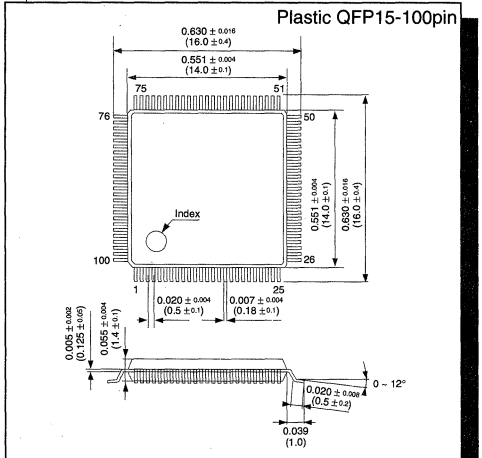
Plastic QFP5-100pin-S2



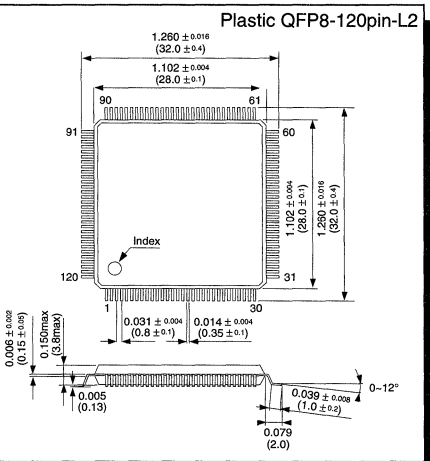
Plastic QFP8-120pin-E1



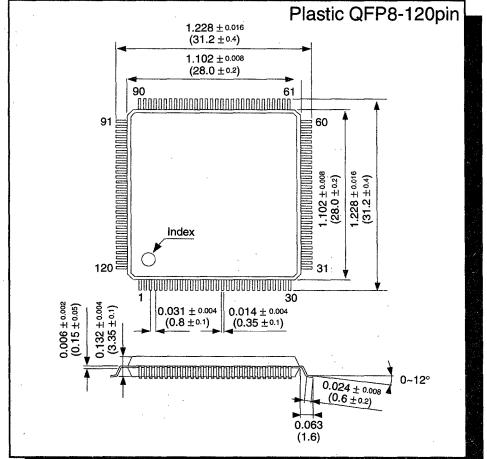
Plastic QFP15-100pin



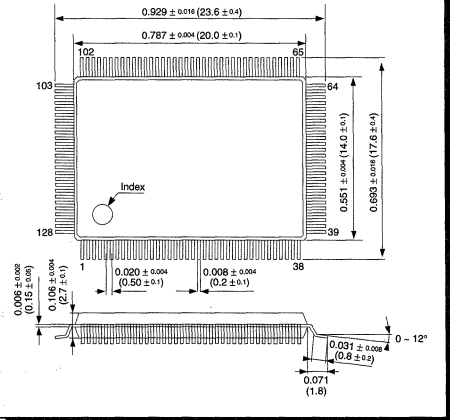
Plastic QFP8-120pin-L2



Plastic QFP8-120pin



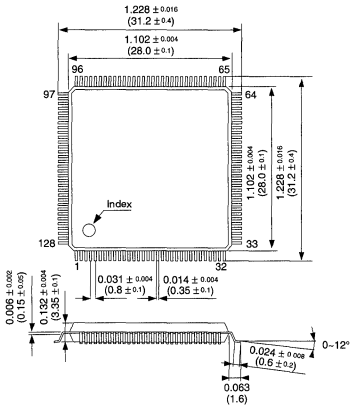
Plastic QFP5-128pin-S1



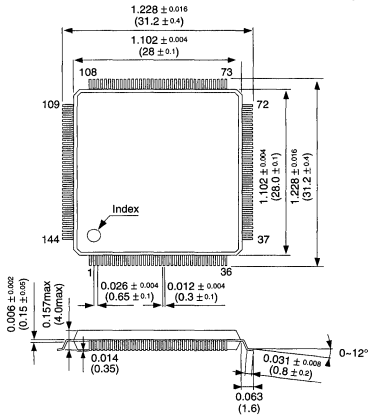
Unit: inch (mm)

Plastic QFPs

Plastic QFP8-128pin



Plastic QFP8-144pin-E1



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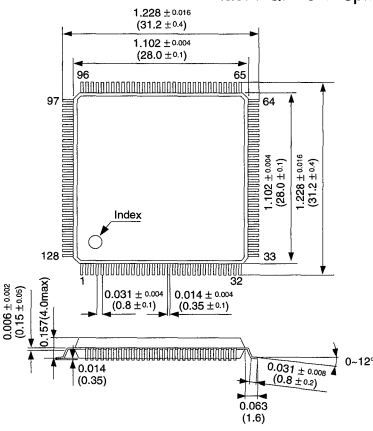
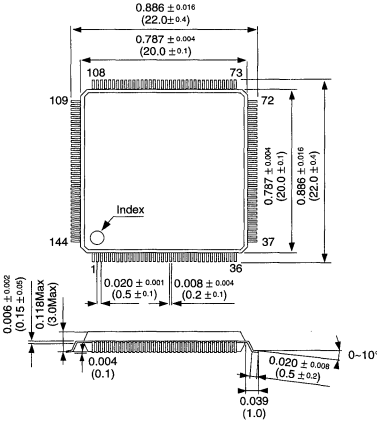
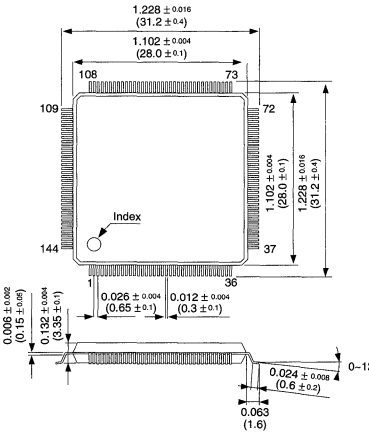


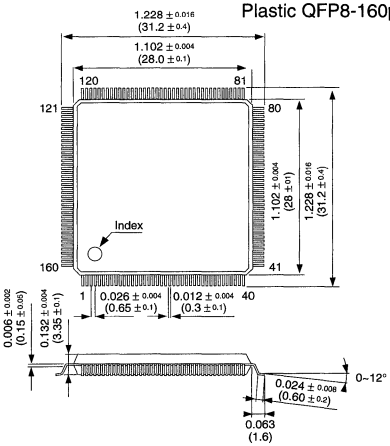
Plastic QFP17-144pin



Plastic QFP8-144pin



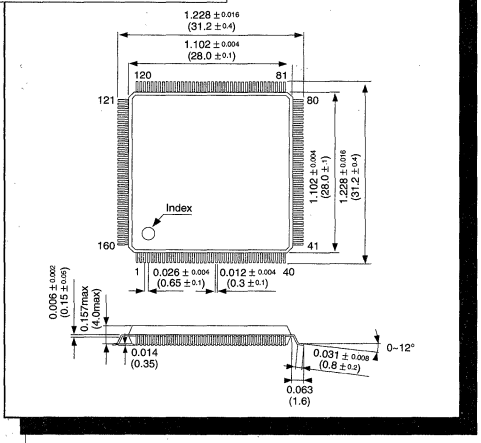
Plastic QFP8-160pin



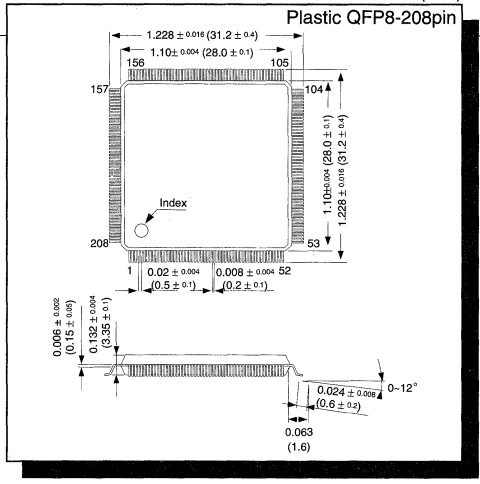
Unit: inch (mm)

Plastic QFPs

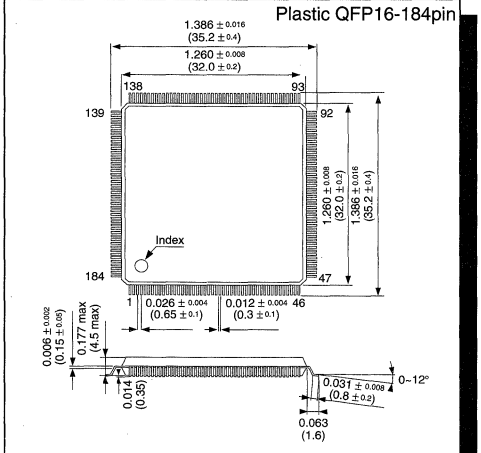
Plastic QFP8-160pin-E1



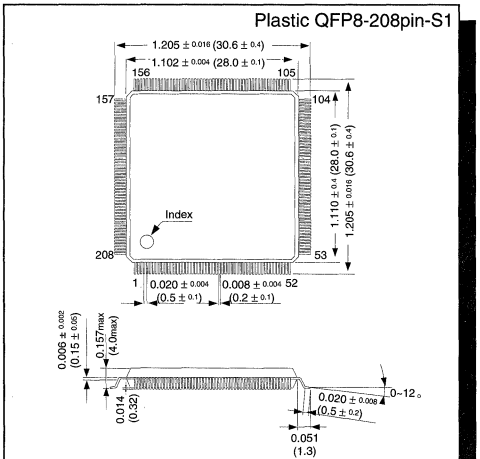
Plastic QFP8-208pin



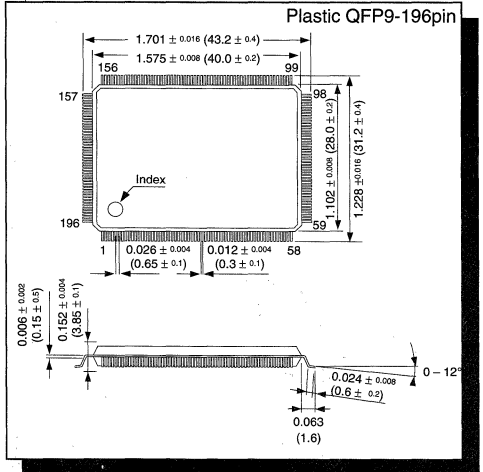
Plastic QFP16-184pin



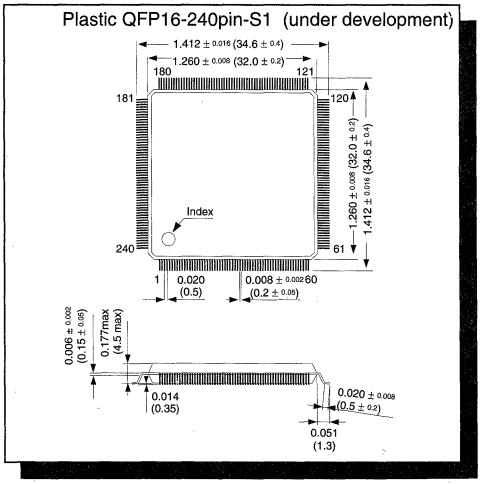
Plastic QFP8-208pin-S1



Plastic QFP9-196pin



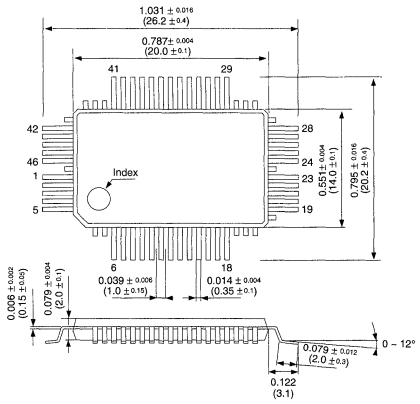
Plastic QFP16-240pin-S1 (under development)



Plastic QFPs

Unit: inch (mm)

Plastic QFP1-46pin



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