ROCKWELL PARALLEL PROCESSING SYSTEM (PPS)

PPS-4/1 ONE-CHIP MICROCOMPUTERS

PRODUCT DESCRIPTION
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SERIES MM76

ONE-CHIP MICROCOMPUTERS

Rockwell International

Rockwell Microelectronic Devices
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PPS-4/1 SUPPORTING DOCUMENT

The following documents provide related design information aiding implementation of this device in your system:

- MM76 Programming Manual — Document No. 29410N44
- PPS-4/1 Prototyping using the PROM Evaluation Module — Document #29410N20
- PPS-4/1 Operator's Manual for Universal Assemulator — Document #29400N37

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INTRODUCTION

The PPS-4/1 microcomputers, Series MM76 are members of a growing family of single circuit microcomputers from Rockwell International. The circuits contain a read only memory for the program memory functions, a random access memory for data, parameter and working storage, and a sophisticated input/output capability which provides a high degree of flexibility for microcomputer and controller applications. The MM76 is the basic device described. The appendices describe the dedicated features of other devices in this series.

FEATURES

- MM76 - 640 8-bit bytes of program memory (5120 bits)
- 48 4-bit data words (192 bits)
- Automatic code conversion
- Two 4-bit input channels
- Two 4-bit input/output channels
- 10 discrete input/output lines
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Pulse output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and three working registers
- On-chip resistor controlled 80 kHz (nominal) clock generator which may be externally synchronized
- One clock cycle execution (nominal 12.5 microseconds) for most instructions
- Large instruction set – over 50 instructions
- Multifunction instructions increase throughput
- Single power supply operation (15 volts ±5%)
- Compact quad-in-line 42-pin package
- Sophisticated development aids
  - General Electric Software Assembler
  - Development Circuit with PROM Module for Program Memory
  - PPS Universal Assemulator with PPS-4/1 Personality Board for Program and Hardware Development
  - XPO-1, PPS-4/1 Emulator (System Development Microcomputer)
  - Scheduled and Special Training Courses
  - International Applications Engineering Support
- Low power (75 milliwatts typical, 125 milliwatts max)

SYSTEM DESCRIPTION

The PPS-4/1, Series MM76 circuits have been designed to be used by themselves, in conjunction with other PPS-4/1 circuits, or in conjunction with other PPS families of circuits (PPS-4/2, PPS-4, or PPS-8). The series MM76 may be used as compact stand-alone microcomputers, as a low cost special controller, as a programmable peripheral controller for one of the larger PPS systems, as a sophisticated appliance controller, or as a universal logic element. The series MM76 as a universal logic element can economically perform functions such as counting, time delays, comparisons, sequencing, function generating, etc., to control a set of output lines based upon conditions presented on a set of input lines.

Any of the PPS-4/1 systems may be operated in tandem to perform parallel processing functions in multi-microcomputer configurations.

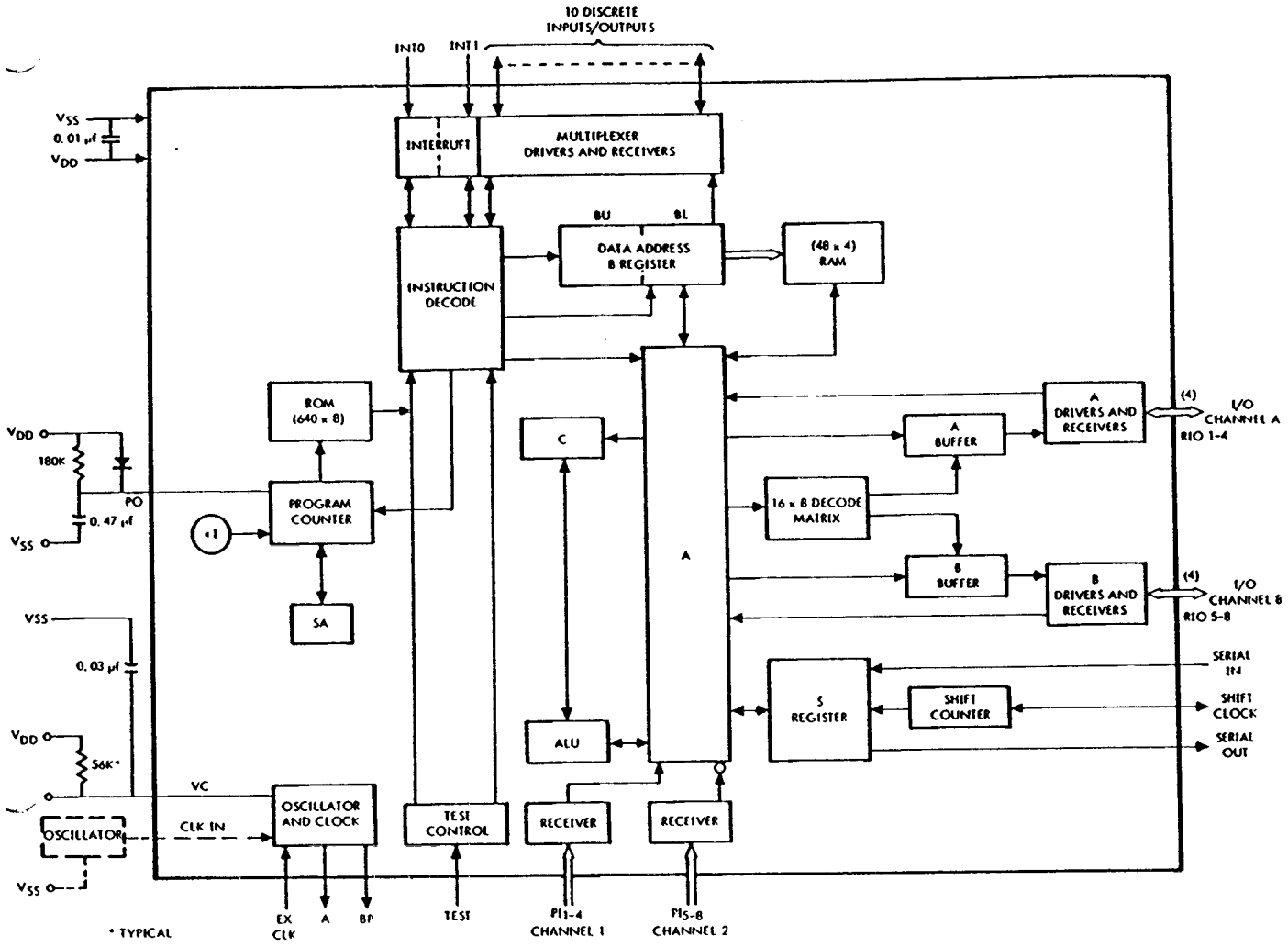
A block diagram of the PPS-4/1 MM76 is shown in Figure 1.

ACCUMULATOR AND ARITHMETIC LOGIC UNIT (A, ALU, AND C)

The primary working register in the PPS-4/1 MM76 is the Accumulator (A Register). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the carry flip-flop (C) to perform either binary or decimal arithmetic. Constants may be loaded into the Accumulator by appropriate instructions from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data although the S Register may also be involved.

A BUFFER

The contents of the Accumulator may be output for control or data transfer purposes through the A Buffer via the Output A command. The A Buffer consists of four latched open drain circuits which will hold the data output until new data is output or power is turned off. The electrical characteristics of these and other signal lines are in the section on Electrical Interface.



Note: The evaluation circuit for the PPS-4/1 (Part No. A7699) is identical to the PPS-4/1 MM76 production circuits (Part No. A76XX) except that, in place of the ROM, terminals are brought out to an external memory and control system.

Figure 1. PPS-4/1 MM76 SYSTEM BLOCK DIAGRAM

DRIVER AND RECEIVER CIRCUITS

The outputs of each of the latches in the A Buffer, B Buffer and discrete input output flip-flops are through open drain drivers which drive to either the VSS logic level or float. When power is applied, the power on reset circuit (PO) causes all of the outputs to be automatically set to a float condition. (All output flip-flops are reset.)

-put signals may share the same lines as outputs for the and B channels (RI/O 1-8) and the discrete input/ output lines. To use one of these lines as an input, it is necessary to set the output on that line into a float condition. The external signal may then either take the line high to VSS or to the appropriate low logic level. The input command, in effect, samples the logic level on the pin and inputs it appropriately.

The mechanization of the PPS-4/1 MM76 allows a software masked input capability. To mask out any input bits, the Accumulator bit in that bit position is set to 0. The external input in that position will always be input as a zero while other bits input to bit positions pre-conditioned by a 1 in the Accumulator will be at logic one or zero levels as determined by the external system. This is in effect a logical AND between the initial contents of the Accumulator and the input signal.

B BUFFER

The output B instruction causes the contents of the Accumulator to be transferred to the B Buffer. The B Buffer comprises four latches which will output the last bit pattern loaded until either a new Output B command is executed or power is turned off. The power on reset signal resets all of the latches so the outputs float.

16 x 8 DECODE MATRIX

The MM76 microcomputer can output any of 16 eight-bit codes, as determined by the four-bit contents of the addressed memory and the two's complement of those four bits in the Accumulator. The carry flip-flop may also be used to set one of the output terms. The 16 eight-bit codes in the decode matrix are specified by the user at the time he orders the microcomputer.

The SEG1 and SEG2 instructions cause the lower and upper four bits of the selected decode matrix term to be output on I/O Channels A and B, respectively.

The four-bit contents of the addressed memory and its complement in the Accumulator are decoded to select which of the 16 eight-bit will be output by the SEG1 and SEG2 instruction.

The MM76 development circuits (A7698, A7699, A7999, B7698 and B7699) have a BCD-to-seven-segment-display conversion mask programmed in the decode matrix. Hexadecimal digits F,E,...1,0 in memory and their associated complements 0,1...F in the Accumulator produce segment control signals for 0 through 9, A, -, P, d, E and "blank", respectively. In the development circuits, the carry flip-flop controls RI/O8.

S REGISTER - SERIAL INPUT/OUTPUT - SHIFT COUNTER

The S Register is a 4-bit parallel-in/parallel-out, serial shift register which is used as either an auxiliary storage register or a buffer for the simultaneous serial-in/serial-out capabilities in the microcomputer. The 4 bits to be serially output are loaded into the S Register either by exchanging the contents of the Accumulator and the S Register or directly loading the S Register from the Accumulator. The state of the serial output line is immediately set by the contents of the most significant bit position. When an Input/Output Serial instruction is executed, or an external shift clock input is provided the four bit contents of the S Register are shifted out (most significant bit first). The data shift rate is under control of the Shift Counter, and is one-half the rate of the internal clock frequency when the IOS instruction is used. The Input/Output Serial instruction also causes the Shift Counter to provide four shift clock signals to the external system. Under external shift control on the same shift clock line, the shift rate may be any value at or below the clock frequency. Both the serial data and shift clock outputs are open drain drivers which are set to the float state when power is turned on.

At the same time that the 4-bit data is being shifted out through the serial output line, 4 bits of data are shifted into the S Register from the serial input line. An exchange of the Accumulator and S Register brings the 4 bits of serial input data into the Accumulator where it can be processed or stored. The S Register may be simultaneously reloaded if more than 4 bits of data are being transmitted.

When the external clocking mode is used it may be necessary for the system designer to establish a handshake protocol to establish when data is to be moved and when the move is completed.

DISCRETE INPUT/OUTPUT PORTS (DI/00 THROUGH DI/09)

There are ten discrete input or output lines. Buffer flip-flops associated with all ten of these channels may be individually set, or reset under program control. They are all reset when power is applied. There is a buffer flip-flop associated with each of these channels which is selected by the least significant 4 bits of the Data Address (B) Register. A Set Output Selected instruction causes the selected output to be at the VSS level and a Reset Output Selected instruction causes it to float. When the output is floating, an input signal level on that port may be tested by a Skip on Input Selected Low instruction. When the Buffer flip-flops are not used specifically for input/output functions, they may be used as one bit status registers. In this case external pull up resistors connected to V_{DD} must be used.

CONDITIONAL INTERRUPTS (INT0 AND INT1)

The conditional interrupt request lines may be used in a number of different ways. These ports are different from the discrete input/output channels in that they may be addressed directly and not by the B Lower portion of the B Register.

To test the state of the signal on the input line it is not necessary to set a flip-flop to any predetermined state as there is no output driver on these signal lines. The level on these two lines may be tested directly by an INT0L or INT1H instruction for INT0 and INT1 inputs respectively without any pre-conditioning. This gives the PPS-4/1 a pseudo interrupt capability by allowing a direct test of the input signal. The INT0L instruction causes the next instruction to be skipped if the input on INT0 is low and the INT1H instruction will cause it to skip if the signal on the INT1 line is high.

Another difference in these two signals is that they may be used to detect a pulse input of a duration longer than one clock cycle. In this case, for INT1 the associated flip-flop is preset to the set state by testing so that any subsequent incoming negative transition pulse on INT1 which lasts longer than one clock cycle will reset the flip-flop. The state of the flip-flop may then be tested by addressing it with a DIN1 instruction which will cause the next instruction to be skipped if the flip-flop is reset. Testing the

p-flop automatically restores it to the set state so that is ready for the next test via the DIN1 instruction.

'N0 instruction similarly may be used to test for a sitive transition or pulse on INT0.

IANNEL 1

ıannel 1 is a 4-bit input port which automatically loads e input value to the contents of the Accumulator.

ANNEL 2

ıannel 2 is a 4-bit input port which on command replaces e contents of the Accumulator with the complement of e value on the input lines. If the input value is from L or CMOS logic, the inversion causes the equivalent lue to appear in the Accumulator.

OGRAM COUNTER (P)

e 10-bit Program Counter is set to a specific initial value exadecimal address ICO) when power is applied to the crocomputer. The contents of the Program Counter ldresses read-only memory to identify the specific struction to be executed. Then, unless the instruction a transfer instruction, the contents of the Program ɔunter are incremented so that the next instruction may lected. This process repeats until a transfer or transfer ıark instruction is executed. The transfer instruction ay set a specific location into the least significant 6 bits) while leaving the upper bits fixed or may set the mplete 10 bits with a Transfer Long (TL) instruction.

milar alternatives are available for the transfer and mark structions which are used to call subroutines. The TM struction selects one of 64 locations in a specific area ıd the TML sets the complete 10 bits. These instructions, owever, mark a return location so that the subroutines ay return to the next instruction location after the one ıat called it. This is accomplished by incrementing the ogram Counter prior to setting the new value into it, nd saving the incremented value in the SA Register.

A REGISTER

/hen a subroutine call is executed by one of the transfer nd mark instructions, the contents of the SA Register are eplaced by the incremented value of the Program Counter.

/hen a return instruction is executed in the subroutine, ıe contents of the SA Register are popped into the Program ounter.

D ONLY MEMORY (ROM)

he Read Only Memory (ROM) provides the storage for nstructions and constants (as immediate field portions of instructions) for the microcomputer. It contains 640 instruction bytes of 8 bits each. It is controlled by the Program Counter to read out each instruction to be executed.

INSTRUCTION DECODE

The instructions are decoded in the Instruction Decode circuits which then issue control signals to all appropriate portions of the microcomputer as necessary to perform the desired operations.

DATA ADDRESS REGISTER (BU AND BL)

The Data Address Register is 6 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data memory in RAM is addressed by all 6 bits and discrete input/output ports are addressed by the 4 bits in BL when the value in B Upper is three.

The BL portion may be automatically incremented or decremented and tested for overflow or underflow by the Exchange Increment and Skip, Exchange Decrement and Skip, Increment B, or Decrement B instructions.

DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory consists of 48 characters of 4 bits each. This memory is used to buffer input or output values, hold intermediate results and also may be used as registers used for timers, counters, comparators, etc. when the microcomputer is used as a universal logic element.

CLOCK CONTROL (VC, CLKIN, EXCLK, AND OSCILLATOR)

The microcomputer may be driven by either its internal clock or an external clock source. Regardless of the source, a resistor must be connected between the VC input and VDD. The resistor value may be used to slightly vary the operating frequency; typical values are 56K ohms for 80 kHz and 47K ohms for 100 kHz.

The nominal 80 kHz internal clock may be used to drive the microcomputer in systems where precise timing is not required. The internal clock is selected by tying the CLKIN pin to VDD and the EXCLK pin to VSS. The A and $\overline{B}$ clock terms are brought out so external logic can be synchronized.

An external frequency reference in the range 40 kHz to 100 kHz may be used in systems when precise timing is required. When the EXCLK pin is tied to VDD, the microcomputer will be driven by an external square wave oscillator input through the CLKIN pin.

A specific definition of the clock waveforms is discussed in the section on Electrical Interface.

PPS-4/1 TESTABILITY (TEST)

Another advantage of the PPS-4/1 microcomputer family is testability both at the factory and user levels. When a test state is indicated by the TEST input line, the PPS-4/1 goes into a test mode which tests ROM and allows testing of the RAM and instruction logic.

POWER SUPPLY

When inputs and outputs interface with other PMOS devices, or CMOS devices, VSS = GND and VDD = -15V ±5% provide proper interface levels. When interfacing with TTL devices, VSS should be +5 and VDD at -10 volts.

POWER ON RESET (PO)

The PO signal is derived from an external resistor, diode, and capacitor pulse shaping network which is tied to the power supply as shown in Figure 1. When power comes on, this circuit automatically sets the Program Counter to a fixed starting location and all outputs are set to a "float" (-V) state. The Program Counter then initiates the first instruction (which must be a Set Carry, Reset Carry or NOP instruction) to be read from the read only memory (ROM) into the instruction decode logic. After executing the first instruction the Program Counter increments so that the second and subsequent instructions may be recalled from memory and executed.

PPS-4/1 MM76 INSTRUCTIONS

The PPS-4/1 MM76 has an extremely sophisticated instruction set which is summarized in Table 1.

Table 1. PPS-4/1 MM76 INSTRUCTION SET

Op Code	Bytes	Cycles	Description
RAM Addressing Instructions			
XAB	1	1	Exchange Accumulator with B Lower (least significant 4 bits)
LBA	1	1	Load B Lower from Accumulator
*LB**	1	1	Load B Upper with zero and B Lower with immediate field
*EOB**	1	1	Exclusive OR B-Upper with two bit immediate field
†*LBL**	2	2	Load B Register Long with 6 bits (4 bits 1st byte, 2 bits 2nd byte) immediate field. This instruction should not be skipped.
†*INCB	2	2	Increment B Lower and modify B Upper with 2 bit immediate field; Skip if BL counts to 0. This instruction should not be skipped.
†*DECB	2	2	Decrement B Lower and modify B Upper with 2 bit immediate field; Skip if BL counts to 15. This instruction should not be skipped.
Bit Manipulation Instructions			
*SB	1	1	Set bit in word in memory. Specific bit designated by 2 bit immediate field and specific word addressed by B Register
*RB	1	1	Reset bit in word in memory. Specific bit designated by 2 bit immediate field and specific word addressed by B Register
*SKBF	1	1	Skip on designated bit in addressed memory when bit is false (zero). Bit is selected by 2-bit immediate field.

Table 1. PPS-4/1 MM76 INSTRUCTION SET (continued)

Op Code	Bytes	Cycles	Description
Register to Register Instructions			
XAS	1	1	Exchange Accumulator and S Register contents
LSA	1	1	Load S Register from Accumulator
Register Memory Instructions			
*L	1	1	Load Accumulator from memory and modify B Upper with 2-bit immediate field
*X	1	1	Exchange Accumulator with memory and modify B Upper with 2-bit immediate field
*XDSK	1	1	Exchange Accumulator with memory and modify B Upper with 2-bit immediate field; Decrement B Lower and skip if BL counts to 15
*XNSK	1	1	Exchange Accumulator with memory and modify B Upper with 2-bit immediate field; increment B Lower and skip if BL counts to 0
Arithmetic Instructions			
A	1	1	Add memory to Accumulator (carry not used or set)
AC	1	1	Add memory and carry to Accumulator; form sum and carry
ACSK	1	1	Add memory and carry to Accumulator; skip if No carry is generated
ASK	1	1	Add memory to Accumulator and skip if No overflow occurs (carry not used or set)
DC	1	1	Decimal correct (same as AISK 6 so it must always be followed by NOP)
COM	1	1	Complement Accumulator
RC	1	1	Reset carry
SC	1	1	Set carry
SKNC	1	1	Skip on no carry
*LAI***	1	1	Load Accumulator with contents of immediate field
*AISK	1	1	Add accumulator and immediate field, skip on no overflow. No carry is set or used.
ROM Addressing Instructions			
RT	1	2	Return from subroutine
RTSK	1	2	Return from subroutine and Skip first instruction of one or two bytes in length. Do not skip macro instructions marked with a †
T	1	2	Transfer on-page to 6 bit immediate field location
NOP	1	1	No operation

Table 1. PPS-4/1 MM76 INSTRUCTION SET (continued)

Op Code	Bytes	Cycles	Description
ROM Addressing Instructions (continued)			
TL	2	3	Transfer Long off page to pages 0 through 7 (addresses #000 thru #1FF)
TM	1	2	Transfer and Mark to special subroutine pages SR0 (addresses #3C0 thru #3FF)
TML	2	3	Transfer and Mark Long to subroutine on pages 0 through 7 (addresses #000 thru #1FF)
Logical Comparison Instructions			
SKMEA	1	1	Skip on memory equals Accumulator
*SKBEI	2	2	Skip on B Lower equals immediate field
*SKAEI	2	2	Skip on Accumulator equals immediate field
Input/Output Instructions			
SOS	1	1	Set output, bit selected by B Lower (B Upper = 3) to VSS
ROS	1	1	Reset output, bit selected by B Lower (B Upper = 3) to -V
SKISL	1	1	Skip on Input Selected Low on bit selected by B Lower (B Upper = 3) Bit sampled during prior cycle.
IBM	1	1	Input Channel B ANDed with Accumulator, results to Accumulator
OB	1	1	Output from Accumulator to Channel B
IAM	1	1	Input Channel A, ANDed with Accumulator, results to Accumulator
OA			Output from Accumulator to Channel A
IOS	1	1	Serial input and output from S – shifting takes 8 cycles concurrent with other instruction operations
I1	1	1	Input Channel 1 to Accumulator
I2C	1	1	Input Channel 2 to Accumulator and complement
INT1H	1	1	Skip on INT1 equals VSS on input pad
DIN1	1	1	Skip if INT1 flip-flop is reset and set INT1 flip-flop
INT0L	1	1	Skip on INT0 equals -V on input pad
DIN0	1	1	Skip if INT0 flip-flop is reset and set INT0 flip-flop
SEG1	1	1	Decode combined memory, Carry flip-flop, and Accumulator and output 4 bits to Channel A
SEG2	1	1	Decode combined memory, Carry flip-flop, and Accumulator and output 4 bits to Channel B

Table 1. PPS-4/1 MM76 INSTRUCTION SET (continued)

Op Code	Bytes	Cycles	Description
Conditional Transfer Instructions†			
† TC	2	3-2	Transfer within page on Carry Set
† TNC	3	4-3	Transfer within page on No Carry Set
† TLC	3	4-3	Transfer Long on Carry Set
† TLNC	4	5-3	Transfer Long on No Carry Set
† TBF	3	4-3	Transfer within page on Bit in Memory False
† TBT	2	3-2	Transfer within page on Bit in Memory True
† TLBF	4	5-3	Transfer Long on Bit in Memory False
† TLBT	3	4-3	Transfer Long on Bit in Memory True
† TE	3	4-3	Transfer within page on Accumulator Equals Memory
† TNE	2	3-2	Transfer within page on Accumulator Not Equal Memory
† TLE	4	5-3	Transfer Long on Accumulator Equals Memory
† TLNE	3	4-3	Transfer Long on Accumulator Not Equal Memory
† TIH	2	3-2	Transfer within page if input selected by B Lower is High
† TIL	3	4-3	Transfer within page if input selected by B Lower is Low
† TLIH	3	4-3	Transfer Long on Input Selected High
† TLIL	4	5-3	Transfer Long on Input Selected Low

*The immediate field (IF) is two, four or six bits which are included as part of the 8-bit instruction. If not specified otherwise the immediate field is 4 bits.

**When LB, EOB or LBL instructions appear in sequence as a string of LB, EOB or LBL or mixtures of LB and LBL instructions only the first one of them will be executed. The remainder of the LB, EOB or LBL instructions in the sequence will be ignored except that the first EOB after an executed LB instruction will also be executed.

***When more than one LAI instruction occurs in sequence, only the first LAI instruction encountered will be executed. The remainder of the LAI instructions in the string will be ignored.

†These are all macro instructions which must not be preceded by an instruction which executes a skip. For the conditional transfer instructions the first number in the cycles column indicates number of cycles when condition is met and second number indicates number of cycles when the condition for transfer is not met.

Numbers preceded by # are hexadecimal numbers.

Note 1: Whenever an instruction is skipped (i. e., ignored) the number of cycles required is equal to the number of bytes in the skipped instruction (e. g. TL takes two cycles to skip).

Note 2: A subroutine called by a TM may not execute an SKBEI or SKAEI when they are followed by a transfer from SR0 to SR0 or from SR1 to SR0 prior to executing the return (RT or RTSK) instruction.

MULTIFUNCTION INSTRUCTIONS

Much of the power of the PPS-4/1 MM76 instruction set comes from a group of multifunction instructions which in addition to performing a basic function such as load or exchange also set up the next address and perhaps test to see if the function is complete so a computational loop may be terminated automatically.

To understand these instructions it is necessary to understand the operation of the Data Address Register B. The B Register has two segments, B Upper and B Lower. B Lower is four bits in capacity and B Upper is two as shown in Figure 2. The bits in the B Register may be modified in groups of 2, 4 or 6 bits as shown in Table 2. It can be seen from the data memory map (Figure 3), that B Upper addresses a row and B Lower selects the column within that row.

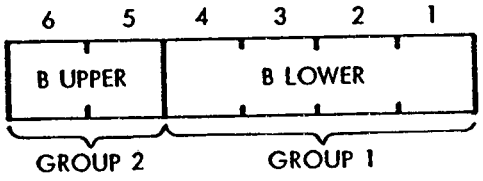


Figure 2. ADDRESS REGISTER ORGANIZATION

Suppose that a number is in a register, REGISTER 2, which occupies Row 2 Columns 0 through 5. The program to initially set the B Register address to Row 2, Column 5, and then shift the contents of the register left 1 decimal place with a zero loaded into the vacated position is as follows:

```
ONE     LBL     #25
TWO     LAI     0
LSFT    XDSK    0
FOUR    T       LSFT
```

Instruction ONE sets the B Register to hexadecimal 25 (the # symbol indicates a hexadecimal number rather than a decimal number). Instruction TWO loads zero into the Accumulator. The instruction in location LSFT (XDSK) causes the contents of the Accumulator to be exchanged with the addressed memory cell (initially #25), decrements the B Lower address to point to #24 and leaves the B Upper register alone since 0 Exclusively ORed with anything leaves it unchanged.

The XDSK instruction also tests to see if the complete register has been shifted by checking the decremented B Lower. If B Lower decrements from zero to #F, then the next instruction will be skipped. Since, after completion of the 1st XDSK instruction, B Lower is 4, no skip occurs. Consequently the transfer instruction is not skipped and the

Table 2. DATA ADDRESS MODIFICATION

Instruction		Address Bits Modified		Condition to Automatically Terminate Process
Op Code	Immediate Field	Group 2 2 Bits of BU**	Group 1 BL	
XAB*	—	—	Exchanged with A	—
LBA*	—	—	Replaced with A	—
LBL	Upper/Lower	Replaced (2nd)	Replaced (first)	—
LB	Lower	Zero	Replaced	—
EOB	Upper	Exclusive OR	No Change	—
INCB*	2 bit Upper	Exclusive OR	Increment and Test for 0	BL counts to 0
DECB*	2 bit Upper	Exclusive OR	Decrement and Test for #F	BL counts to #F
L	2 bit Upper	Exclusive OR	No Change	—
X	2 bit Upper	Exclusive OR	No Change	—
XDSK*	2 bit Upper	Exclusive OR	Decrement and Test for #F	BL counts to #F
XNSK*	2 bit Upper	Exclusive OR	Increment and Test for 0	BL counts to 0

*In the cycle immediately following these instructions, the contents of BU and BL Registers are correct as modified. However, in the cycle immediately following the address and modification instruction, instructions which address memory will have B Upper modifications completed but the old value of BL will be used in forming the effective memory address.

**RAM-DIO Timing. When changing BU from addressing RAM (0, 1, or 2) to DIO (3), the B Register value is updated in the cycle immediately following the modification instruction, but neither RAM nor DIO accessing instructions are valid. In the second cycle following, the DIO selected by the modified BU and BL may be set, reset, or tested. When changing BU from addressing DIO (3) to RAM (0, 1, or 2) the B Register value is updated in the cycle immediately following the modification and RAM addressing instructions are valid (subject to the timing related to changing BL) except for SB, RB, SKBF instructions. During the one cycle immediately following changing BU the SB and RB instructions will set or reset a bit in RAM as well as the DIO bit. The SKBF instruction is undefined during this cycle. In the second cycle following, these three instructions are valid.

rocess is repeated. The prior contents of #25 which are n the Accumulator are exchanged with #24 and the address ·ecremented and tested again. Subsequently the ents of #24 are moved to #23, #23 to #22, #22 to #21 nd #21 to #20. Note that when this last operation is erformed the B Lower register will decrement from 0 to #F ausing the transfer instruction to be skipped and the rocess terminated.

uppose that the contents of REGISTER 2 are to be comple- ented and moved to the register called REGISTER 1 in ow 1. The program to do this follows:

```
ONE   LBL    #25    Point to hex 25
TWO   L      3      Load and point to hex 15
THREE COM           Complement
FOUR  XDSK   3      Exchange, Point to #24, test
FIVE  T      TWO    Not thru, repeat
```

he Exclusive OR function between 11 from the immediate ield of instruction TWO (L 3) and 10 in bits 6 and 5 of he B Register converts the B Register address to 01 0101 #15) as well as loading the Accumulator. Similarly the 11 in the immediate field of the instruction in location OUR causes the 01 bits in locations 6 and 5 to be onverted to 10 (2) and the B Lower is also decremented nd tested in addition to performing the exchange. onsequently, the B Register at the conclusion of this ruction is 10 0100 (#24) which is pointing at the next a to be complemented.

he process is repeated again until the complemented alue of memory cell #20 is stored in #10 and then the rocess automatically terminates because B Lower will decrement from 0 to #F after the exchange.

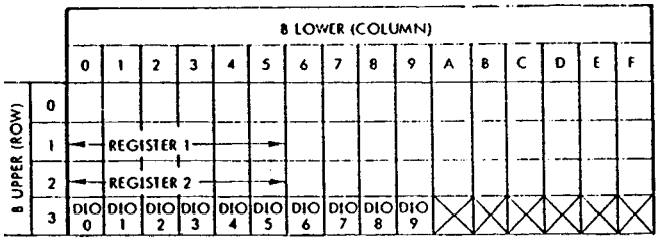


Figure 3. DATA MEMORY MAP FOR PPS-4/1 MM76

A program to move the data from REGISTER 2 to REGISTER 1 is as follows:

```
      LBL    #25
MOVE  L      3
      XDSK   3
      T      MOVE
```

The same program will move 16 four-bit words if the process is started at #2F instead of #25:

```
      LBL    #2F
MOVE  L      3
      XDSK   3
      T      MOVE
```

The PPS-4/1 MM76 is particularly efficient for using subroutines which may operate for different lengths of data registers in memory. For instance if it is desired to use one subroutine with two entry points to either move 6 characters or 16 characters respectively, the following program may be used:

```
      TM     MOVF    subroutine call to
RETN  [NEXT  INSTR]  move 16 characters

MOVF  LBL    #2F
MOV6  LBL    #25
MOVE  L      3
      XDSK   3
      T      MOVE
      RT
```

The PPS-4/1 ignores LBL instructions in a string except for the first one executed. Consequently, for this example, the B Register is loaded with #2F and the LBL #25 is ignored so 16 bytes will be moved. A TM MOV6 instruction would load the B Register with #25 so that 6 characters would be moved. After moving the 16 or 6 characters the T MOVE instruction will be ignored and the RT instruction causes the program counter to return to the next instruction after the TM MOVF or TM MOV6 instruction so that the main program can continue from that point. If more than one subroutine call is used in the program (the usual case for subroutines) the program will always continue with the next instruction after the specific one which called the subroutine when the subroutine has completed its process.

There are two types of unconditional transfer instructions (T and TL) and two types of transfer and mark instructions (TM and TML). The ROM Map Table (Table 3) will help explain their usage.

There are 64 program memory bytes on a page. An unconditional transfer to another location on the same page requires a one byte T instruction which contains as part of the instruction the specific location for the next instruction to be executed. If the next instruction is not on the same page and is not in the primitive subroutine page, then a two byte instruction TL is used.

The subroutine call instruction TML is similar. However, the TML instruction is used when the first instruction of the subroutine is on any of the general program area pages (even if it is the same page).

The TM instruction operates differently. The TM instruction is one byte long and always transfers to a subroutine on page SR0 of the primitive subroutine area. The primitive subroutine area (SR0 and SR1) is special in that it comprises two 64 byte sections, 15 and 14 respectively. One byte transfers are used to go between the two sections. This area is intended for easy access to primitive subroutines which are often used.

The subroutine may be self-contained within that area or the subroutine may perform an unconditional transfer to anywhere in memory via a TL instruction.

The PPS-4/1 MM76 conserves ROM by allowing these simplified one byte subroutine calls to be used for the high usage subroutines. This is a unique capability in the PPS family which effectively increases the amount of ROM available for other functions.

A more complete description of programming techniques are shown in the PPS-4/1 Programming and Applications Manual. Features of the assembly, editing, and emulation capabilities on the PPS Universal Assemulator development hardware are discussed in the PPS-4/1 Operators Manual for Universal Assemulator. An assembly capability for the MM76 is also available in FORTRAN IV and on the General Electric Information Services system. That assembler is described in the PPS-4/1 Single Circuit Microcomputer Series Programming Manual.

Table 3. ROM MAP

Page No.	Program Memory (ROM) Allocation		
0	64 bytes general program area	on page transfers (T) — one byte	Subroutines called by TML are located in this area
1	64 bytes general program area		
2	64 bytes general program area		
3	64 bytes general program area		
4	64 bytes general program area	off page transfers (TL) — two bytes	
5	64 bytes general program area		
6	64 bytes general program area		
7	byte 0 = power on location — remainder general area		
8-13	Not used		
14 (SR1)	Extension of primitive subroutine area from page SR0 (15)		
15 (SR0)	TM address area (1 byte subroutine calls start here and extend to page SR1 (14) or to other sections of memory)		

Note: The development circuit for the PPS-4/1 MM76 (Part No. A7699) can use all 1024 addressable bytes for developing programs. Consequently, pages 8 through 13 may be used as necessary during the development and the final programs condensed to the addresses shown above for the production program.

ECIMAL ADDITION

MPLE

o further illustrate the flexibility and efficiency of the PS-4/1 MM76 instruction set, a decimal addition sub-utine which has multiple entry points will be discussed. hese different entry points allow the contents of different emory registers to be added together and the resulting m left in the designated one of the two registers volved in the addition and also illustrate decimal ddition with differing numbers of decimal digits. In the PS-4/1 system the same subroutine may be used for both pes of functions. This decimal add subroutine is as llows:

D10	LB	#29	Entry to Add 10 digit register Pair 1*
D12	LBL	#1B	Entry to Add 12 digit Register Pair 2*
D5	LBL	#14	Entry to Add 5 digit Register Pair 3*
ADD	RC		Reset carry for initial digit add
OOP	L	3	Load digit from 1st register and point to 2nd
	AISK	6	Decimal correct (add 6)
	NOP		Always is skipped
	ACSK		Add digit from 2nd register, skip if no carry is generated
	T	STOR	Answer is correct so transfer to store digit
	AISK	10	Recorrect if no carry (add 10 with no carry - bypassed if a carry from ACSK instruction)
TOR	XDSK	3	Store answer digit point to next digit in first register, skip if BL=15
	T	LOOP	Repeat until last digit added
	RT		Through so return from subroutine to next location after subroutine call

*Register pair 1 adds Register #20-#29 to #10-#19 and puts answer in #10-#19.

Register pair 2 adds Register #10-#1B to #20-#2B and puts answer in #20-#2B.

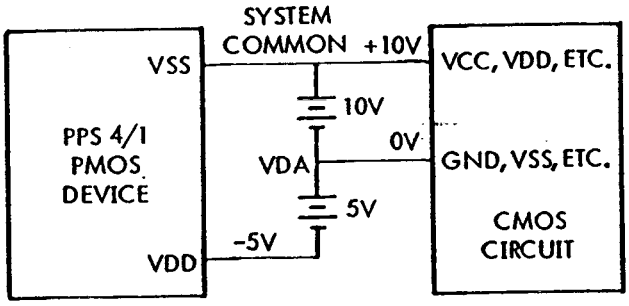
Register pair 3 adds Register #10-#14 to #20-#24 and puts answer in #20-#24.

DADD is a general subroutine entry which may be used to add from 1 to 16 decimal digits in rows 2 to 1 or 1 to 2. The specific registers and the number of decimal digits to added are dependent upon the initial value in the Register.

ELECTRICAL INTERFACE

This section and Table 4 defines the electrical specifications.

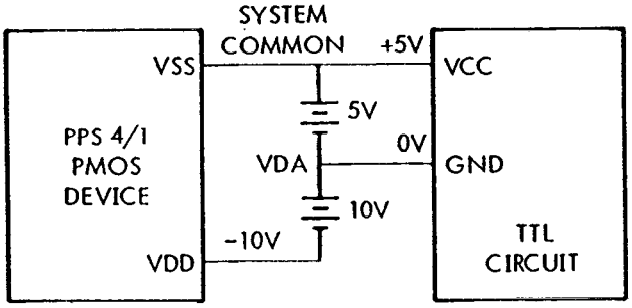
The power supply for the PPS-4/1 microcomputer requires a 15 volt ±5% supply. This may be obtained by a single 15 volt or +10, 0, -5 volt supply when the input/output system is interfacing with CMOS as shown in Figure 4 or may be obtained from +5, 0, -10 volt supply when interfacing with TTL circuits as shown in Figure 5.



NOTE: The PPS-4/1 VSS must be connected to most positive CMOS terminal.

The PPS-4/1 requires a 15 volt supply. CMOS operates with an 8V to 15V input. (If CMOS is only receiving PMOS inputs, the input can range from 3V to 15V.)

Figure 4. TYPICAL PMOS TO CMOS POWER INTERFACE



NOTE: The PPS-4/1 requires a 15 volt supply. TTL uses a 5 volt supply.

Figure 5. TYPICAL PMOS TO TTL POWER INTERFACE

Table 4. MM76 ELECTRICAL SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:
VDD = -15 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)

VSS = 0 Volts (GND)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies:
80 kHz ± 50% with external resistor

Device Power Consumption:
75 mw, typical

Input Capacitance:
<5 pf

Input Leakage:
<10 μa

Open Drain Driver Leakage (R OFF):
<10 μa at -30 Volts

Operating Ambient Temperature (TA):
0°C to 70°C (TA = 25°C unless otherwise specified)

Storage Temperature:
-55°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +0.3 volts.

Input/Output	Symbol	Limits (VSS = 0) Min	Typ	Max	Limits (VSS = +5V) Min	Typ	Max	Timing (Sample/ Good)	Test Conditions
Supply Current (Average) for VDD	IDD		5 ma	8 ma		5 ma	8 ma		VDD = -15.75V T = 25°C
Discrete I/O's DI/O0-DI/O9	V_{IH}	-1.0V			+4.0V			Ø3 & Ø4	
	V_{IL}			-4.2V			+0.8V		
DI/O0-5	R_{ON}			500 ohms			500 ohms	Ø2*	3.0 ma max.
DI/O6-9	R_{ON}			400 ohms			400 ohms		
Channel 1 Input PI1-PI4	V_{IH}	-1.5V			+3.5V			Ø1	
	V_{IL}			-4.2V			+0.8V		
Channel 2 Input PI5-PI8	V_{IH}	-1.5V			+3.5V			Ø3	
	V_{IL}			-4.2V			+0.8V		
I/O Channel A RI/O1-RI/O4	V_{IH}	-1.5V			+3.5V			Ø3	
	V_{IL}			-4.2V			+0.8V		
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max.
I/O Channel B RI/O5-RI/O8	V_{IH}	-1.5V			+3.5V			Ø3	
	V_{IL}			-4.2V			+0.8V		
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max.
DATAI	V_{IH}	-1.0V			+4.0V			Ø4	
	V_{IL}			-4.2V			+0.8V		
DATAO	R_{ON}			500 ohms			500 ohms	Ø4**	3.0 ma max.
INT0	V_{IH}	-1.5V			+3.5V			Ø3	
	V_{IL}			-4.2V			+0.8V		
INT1	V_{IH}	-1.5V			+3.5V			Ø1	
	V_{IL}			-4.2V			+0.8V		
Clock A, BP, $(\overline{B})$	V_{OH}	-1.0V			+4.0V			-5.0V	CL = 50 pf (max)
	V_{OL}			-10.0V			-5.0V		
EXCLK	V_{IH}	-1.5V			+3.5V			-4.0V	F max. = 80 kHz
	V_{IL}			-9.0V			-4.0V		
CLK IN	V_{IH}	-1.0V			+4.0V				
	V_{IL}			-10.0V			-5.0V		
Shift Clock Clock	V_{IH}	-1.0V			+4.0V			Ø3 & Ø4	
	V_{IL}			-4.2V			+0.8V		
	R_{ON}			500 ohms			500 ohms	Ø4**	2.0 ma max.
VC***	V_{IH}								56K ±5%
	V_{IL}								
PO	V_{IH}	-2.0V			+3.0V				Special circuit
	V_{IL}			-6.0V			-1.0V		

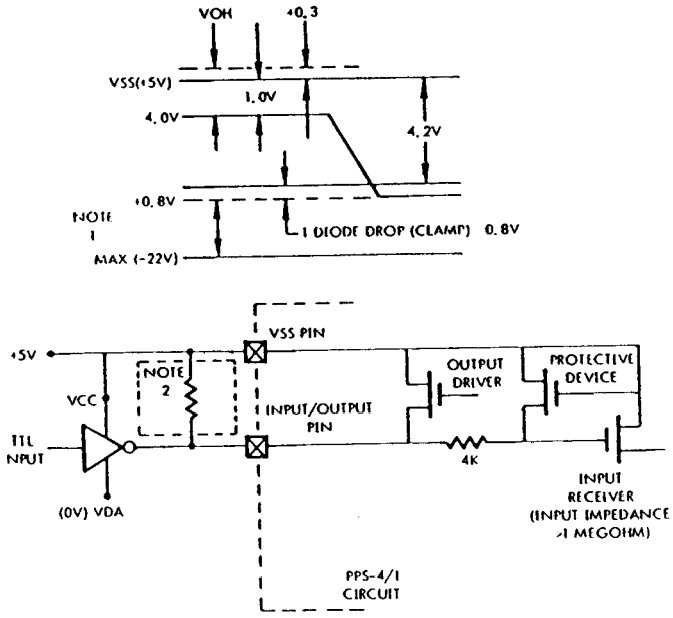
*State established by Ø2 (minimum impedance after Ø4).
**Same as above except Ø4 minimum at Ø2 of next cycle.
***Connect VC to VDD through a resistor: 56KΩ for 80 kHz or 47KΩ for 100 kHz.

SCRETE I/O PORTS

he ten discrete I/O ports (DI/O 0 through DI/O 9) are
:ted by setting B Upper of the B Register to three and
-ower to the appropriate value (i. e., #31 will select
)I/O 1). Issuing a Set Output Selected (SOS) instruction
/ill connect the output port to VSS through 500 ohms (or
00 ohms) maximum. Issuing a Reset Output Selected (ROS)
nstruction will cause the output to float, allowing an
:xternal resistance to pull the output to a -V level. The
)utput will be stable by Ø2 of the following instruction.
Minimum impedance is reached after Ø4. The output circuit
s capable of sinking 3 ma maximum when all the output
:ircuits are in use. To use as an input, the port must be
elected by BL and the Skip on Input Selected Low instruc-
ion issued. A skip will be produced if the input is more
legative, relative to VSS, than -4. 2 volts. The inputs are
ully synchronized so that an asynchronous input signal may
e used. The sampling occurs during phase 3 (see Figure 9).
The technique for interfacing with TTL logic is shown in
Figures 6 and 7.

ARALLEL I/O PORTS (RIO1-RIO4)

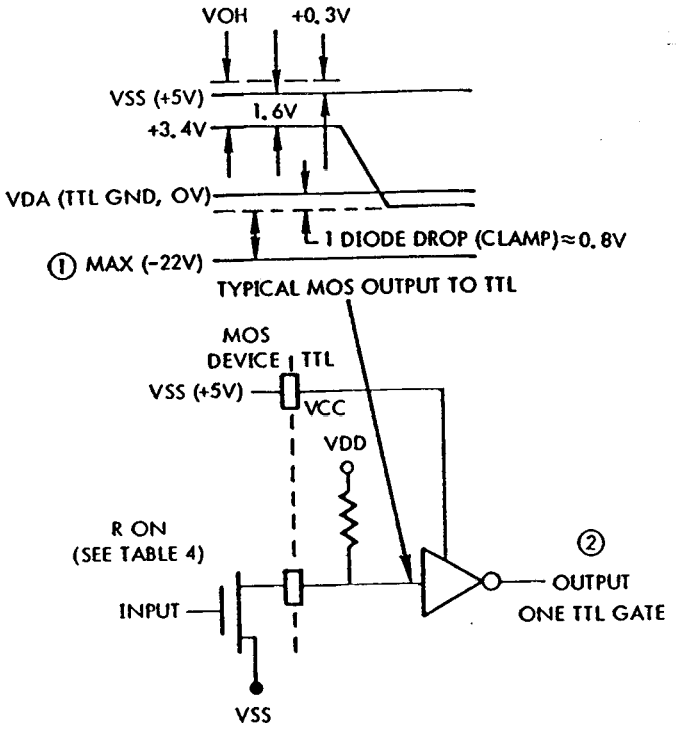
The parallel input/output ports RIO1 through RIO4 provide
a masked input capability and an output capability either
from the 16 x 8 matrix or directly from the Accumulator.
In either event the A Buffer is loaded via a SEG1 or an
OA instruction. When used as an output a "1" in any bit
position in the A Buffer will cause the corresponding output



NOTES:

1. Maximum voltage which may be applied to any input/output pin is -30 volts relative to VSS.
2. Only an Open Collector Driver requires the Pull-Up Resistor.

Figure 6. TTL to PPS-4/1 SYNCHRONIZED INPUT RECEIVER INTERFACE



NOTES:

1. Maximum voltage which may be applied to any input/output pin is -30V relative to VSS.
2. SOS command causes gate output to be low. "1" in A or S causes the gate output to be high.

Figure 7. PPS-4/1 OUTPUT DRIVER TO TTL INTERFACE

bit to float, while a "0" in the A Buffer will cause the output to be connected to VSS through 250 ohms maximum. The outputs will be stable by the following Ø2 time and the impedance to VSS when the output is in the high state will be less than 250 ohms after Ø4. The outputs are buffered through a register such that any state will be held until another exchange is executed. The output drivers will sink 6 milli-amperes when all circuits are sinking a current.

In order to use any bit position as an input, the corresponding bit of the output buffer must be loaded with a "1" before the operation is performed so that the output driver will be floated and may be set high or low by the external signal to be input. The contents of the Accumulator provide a masking capability. The contents of the Accumulator must be set to one in each bit position to be input. A zero in the Accumulator masks the input bit so that independent of the RIO signal the resulting value in the Accumulator is zero. The inputs are fully synchronized (sampled at Ø3 time) and will recognize a voltage more negative than -4. 2 volts (related to VSS) as a "1" and a voltage between +0. 3 and -1. 5 as a "0". The outputs will be initialized to the float state with power on.

PARALLEL I/O PORTS (RIO5-RIO8)

The parallel input/output ports RIO5 through RIO8 work in exactly the same manner except OB, SEG2, and IBM instructions are used.

PARALLEL INPUT PORTS (PI1-PI4)

The parallel input ports PI1 through PI4 will be loaded into the Accumulator upon execution of an input channel 1 instruction (I1). The inputs are fully synchronized during phase 1 and are TTL compatible. An input signal more negative then -4.2 volts will be a logic "1" and a "0" range is from +0.3 to -1.5 volts.

PARALLEL INPUT PORTS (PI5-PI8)

The inverted state of the parallel inputs PI5 through PI8 will be copied into the Accumulator upon receipt of an I2C instruction. The inputs are synchronized during phase 3 and are TTL compatible.

CONDITIONAL INTERRUPTS (INT0 AND INT1)

The conditional interrupt ports may be utilized in two different ways. The first way is that the input logic level can be tested directly by means of the conditional interrupt 0 or conditional interrupt 1 instructions, INT0L or INT1H. A skip will be produced when the INT0 signal is a -V and when the INT1 signal is at VSS.

The second way of using the conditional interrupt capability is to test the state of a flip-flop associated with each input in a manner similar to the discrete I/O ports. The flip-flops are selected and set by DIN0 for INT0 and DIN1 for INT1. If the flip-flop for INT0 is in the set state and a transition occurs on the input from the -V state to the V_{SS} state for one bit time or more, the flip-flop will be reset. Consequently, the signal to activate a conditional interrupt may be a pulse as long as it is at least one clock period long.

The state of the flip-flop may then be tested and set by the DIN0 command. If the next instruction skips, it will indicate that a -V to V_{SS} level pulse did occur even though the V_{SS} level has gone away. The INT1 signal performs in the same manner except that a transition from a V_{SS} level to a -V level for one bit time will cause the flip-flop to be reset so that it may be tested and set by the DIN1 command.

The inputs are sampled at phase 1 for INT1 and phase 3 for INT0 and are TTL level compatible as shown in Figure 6.

SERIAL I/O

A serial register, designated S Register, is built into the circuit which may be used as a serial IN/OUT buffer and may also be used for parallel exchange with the Accumulator. Data to be output is loaded into the Accumulator and transferred to the serial register by the Exchange A and S (XAS) command. The serial I/O (IOS) command causes the data to be shifted out along with a clock for clocking external devices. Each bit of data is presented at the output for two bit times and a data clock pulse is provided as shown in Figure 8a for clocking external shift registers. Data may be input at the same time and then transferred to the Accumulator.

The data and clock outputs are 500 ohm maximum open ended devices capable of sinking 3 milli-amperes maximum and are TTL compatible as shown in Figure 7. The serial input is sampled during phase 4 and TTL compatible as shown in Figure 6.

Data may also be shifted into or out of the S Register under external shift clock control. A shift clock signal may be applied to the CLOCK signal line to cause the internal register, S, to shift and perform a serial input output function at the MM76 clock rate. If shift rates lower than this are desired, the shifting must be done in synchronism with the A clock signal for the particular shift pulse. The shift clock input is sampled at Ø4 time and is TTL compatible as shown in Figure 6.

The basic timing for the serial input/output capability is shown in Figure 8.

The pin connections for the MM76 microcomputer are summarized in Table 5. The pin connections for the A7699 personality module development circuits are shown in Table 6. The pin connections for the A7698 development circuits are shown in Table 7. The basic timing for the PPS-4/1 is summarized in Figure 9.

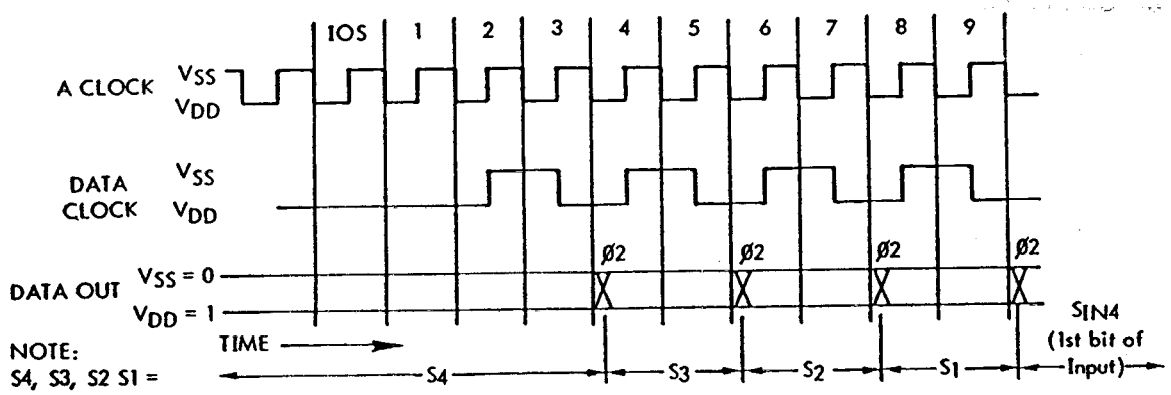


Figure 8a. INTERNALLY CONTROLLED SERIAL INPUT/OUTPUT

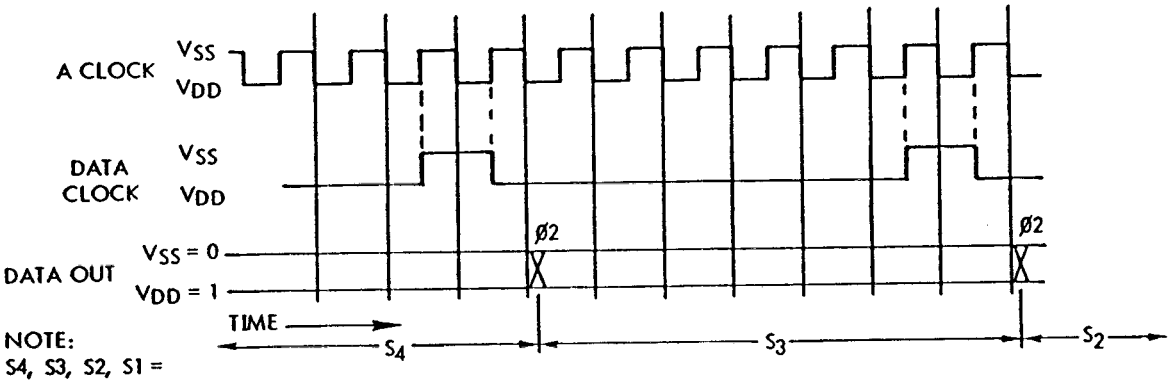


Figure 8b. EXTERNALLY CONTROLLED SERIAL INPUT/OUTPUT WITH DATA CLOCK SYNCHRONIZED WITH A CLOCK SIGNAL

Figure 8. TIMING OF SERIAL DATA INPUT/OUTPUT

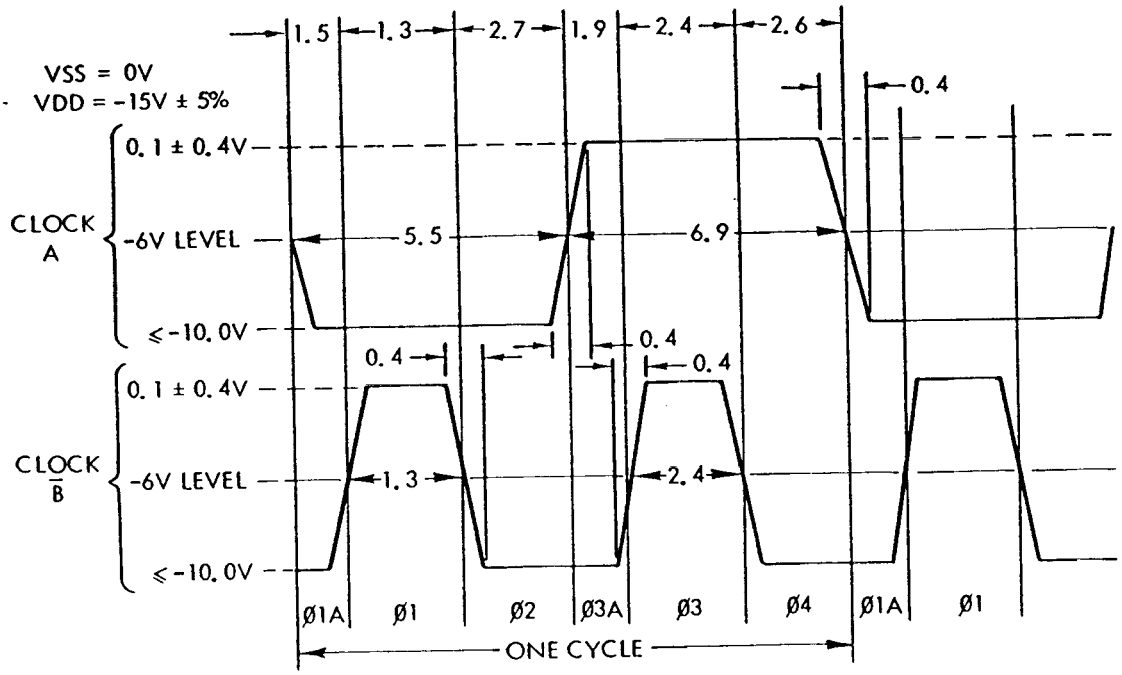


Figure 9. TYPICAL CLOCK WAVEFORMS WITH EXTERNAL 56K OHM RESISTOR

Table 5. PPS-4/1 MM76 SIGNALS (Part No. A76XX)

Pin No.	Signal Name	Function
1	A	A System Clock
2	EXCLK	External Clock selection (VDD = External VSS = Internal)
3	CLKIN	External Clock square wave input (VDD when not used)
4	VC	Resistor frequency control
5	VDD*	-15 Volt Supply (1st pin)
6	VSS	VSS positive power supply terminal
7	TEST (VSS)	Commands Test Mode (VSS for Normal Operation)
8	PI2	Channel 1 bit 2
9	PI6	Channel 2 bit 2
10	PI1	Channel 1 bit 1 (least significant bit)
11	PI5	Channel 2 bit 1
12	PI7	Channel 2 bit 3
13	PI3	Channel 1 bit 3
14	PI8	Channel 2 Most Significant Bit (4)
15	PI4	Channel 1 bit 4
16	VDD*	-15 Volt Supply (2nd pin)
17	PO	Power On reset input
18	INT0	Interrupt 0 input
19	INT1	Interrupt 1 input
20	RIO5	B I/O Channel Least Significant Bit (1)
21	RIO6	B I/O Channel bit 2
22	RIO7	B I/O Channel bit 3
23	RIO8	B I/O Channel bit 4
24	RIO1	A I/O Channel bit 1 (least significant bit)
25	RIO2	A I/O Channel bit 2
26	RIO3	A I/O Channel bit 3
27	RIO4	A I/O Channel bit 4
28	DATAI	Serial Input signal
29	DATAO	Serial Output signal
30	CLOCK	Shift Clock Input/Output (VDD if serial register not used)
31	DI/O0	Discrete I/O line 0
32	DI/O1	Discrete I/O line 1
33	DI/O2	Discrete I/O line 2
34	DI/O3	Discrete I/O line 3
35	DI/O4	Discrete I/O line 4
36	DI/O5	Discrete I/O line 5
37	DI/O6	Discrete I/O line 6
38	DI/O7	Discrete I/O line 7
39	—	—
40	DI/O8	Discrete I/O line 8
41	DI/O9	Discrete I/O line 9
42	BP	B Prime System Clock

*VDD must be connected to both Pins 5 and 16 since they are not connected internally.

Note: Connect all unused inputs to VSS to prevent transient signals/noise. Except if serial register is used in data storage, then connect Pin 30 through 24 KΩ to VDD.

Table 6. PPS-4/1 MM76 PERSONALITY MODULE DEVELOPMENT CIRCUIT SIGNALS
(Part No. A7699)

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	VSS	Same as A76XX	33	(I8)	Instruction bit 8
2	RIO5	Same as A76XX	34	(I7)	Instruction bit 7
3	RIO6	Same as A76XX	35	EXCLK	Same as A76XX
4	RIO7	Same as A76XX	36	CLKIN	Same as A76XX
5	RIO8	Same as A76XX	37	VC	Same as A76XX
6	RIO1	Same as A76XX	38	VDD	Same as A76XX
7	RIO2	Same as A76XX	39	Not Used	—
8	RIO3	Same as A76XX	40	(P6B4)	PC bit 6, BL bit 4
9	Not Used	—	41	(P3B1)	PC bit 3, BL bit 1
10	Not Used	—	42	(P1I1)	PC bit 1, Inst bit 1
11	Not Used	—	43	(P2I2)	PC bit 2, Inst bit 2
12	RIO4	Same as A76XX	44	(P10I5)	PC bit 10, Inst bit 5
13	DATAI	Same as A76XX	45	(P9I6)	PC bit 9, Inst bit 6
14	DATAO	Same as A76XX	46	(P8I4)	PC bit 8, Inst bit 4
15	CLOCK	Same as A76XX	47	(P7I3)	PC bit 7, Inst bit 3
16	DI/O0	Same as A76XX	48	TEST	Same as A76XX
17	DI/O1	Same as A76XX	49	PI2	Same as A76XX
18	DI/O2	Same as A76XX	50	PI6	Same as A76XX
19	DI/O3	Same as A76XX	51	PI1	Same as A76XX
20	DI/O4	Same as A76XX	52	PI5	Same as A76XX
21	DI/O5	Same as A76XX	53	PI7	Same as A76XX
22	DI/O6	Same as A76XX	54	PI3	Same as A76XX
23	DI/O7	Same as A76XX	55	PI8	Same as A76XX
24	Not Used	—	56	PI4	Same as A76XX
25	DI/O8	Same as A76XX	57	VDD	Same as A76XX
26	DI/O9	Same as A76XX	58	PO	Same as A76XX
27	Not Used	—	59	INT0	Same as A76XX
28	(P4B2)	PC bit 4, BL bit 2	60	(B6)	Buffer bit 6
29	(P5B3)	PC bit 5, BL bit 3	61	(B5)	Buffer bit 5
30	Not Used	—	62	(SKIP)	Skip Indicator
31	BP	Same as A76XX	63	INT1	Same as A76XX
32	A	Same as A76XX	64	Not Used	—

Program Control (P) outputs during phase 2 are in complement form. (0 = -V, 1 = VSS)
B outputs during phase 4. BL is in complement form, BU is in true form.
Instruction (I) inputs at end of phase 4 are in true form.
Skip output is -V during Ø4 if an instruction is to be skipped.

Table 7. PPS-4/1 MM76 DEVELOPMENT CIRCUIT SIGNALS
(Part No. A7698)

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	DI/O1	Same as A76XX	27	(P7I3)	PC bit 7, Inst bit 3
2	DI/O2	Same as A76XX	28	PI2	Same as A76XX
3	DI/O3	Same as A76XX	29	PI6	Same as A76XX
4	DI/O4	Same as A76XX	30	PI1	Same as A76XX
5	DI/O5	Same as A76XX	31	PI5	Same as A76XX
6	DI/O6	Same as A76XX	32	PI7	Same as A76XX
7	DI/O7	Same as A76XX	33	PI3	Same as A76XX
8	DI/O8	Same as A76XX	34	PI8	Same as A76XX
9	DI/O9	Same as A76XX	35	PI4	Same as A76XX
10	(P4B2)	PC bit 4, BL bit 2	36	VDD	Same as A76XX
11	(P5B3)	PC bit 5, BL bit 3	37	PO	Same as A76XX
12	BP	Same as A76XX	38	INT0	Same as A76XX
13	A	Same as A76XX	39	INT1	Same as A76XX
14	(I8)	Inst. bit 8	40	RIO5	Same as A76XX
15	(I7)	Inst. bit 7	41	RIO6	Same as A76XX
16	EXCLK	Same as A76XX	42	RIO7	Same as A76XX
17	CLKIN	Same as A76XX	43	RIO8	Same as A76XX
18	VC	Same as A76XX	44	RIO1	Same as A76XX
19	VDD	Same as A76XX	45	RIO2	Same as A76XX
20	(P6B4)	PC bit 6, BL bit 4	46	RIO3	Same as A76XX
21	(P3B1)	PC bit 3, BL bit 1	47	RIO4	Same as A76XX
22	(P1I1)	PC bit 1, Inst bit 1	48	VSS	Same as A76XX
23	(P2I2)	PC bit 2, Inst bit 2	49	DATAI	Same as A76XX
24	(P10I5)	PC bit 10, Inst bit 5	50	DATAO	Same as A76XX
25	(P9I6)	PC bit 9, Inst bit 6	51	CLOCK	Same as A76XX
26	(P8I4)	PC bit 8, Inst bit 4	52	DI/O0	Same as A76XX

Program Control (P) outputs during phase 2 are in complement form (0 = -V, 1 = VSS)
BL outputs during phase 4 are in complement form.
Instruction (I) inputs at end of phase 4 are in true form.

IASK OPTIONS

well offers several mask options for the MM76 series microcomputers. These options are selected by the ustomer at ROM order time, and may be used to simplify particular application.

NOTE

The mask options are not incorporated into the MM76 development circuits, so customers requiring these options in their production devices may wish to simulate them during development with either external circuitry or program modifications.

NTERRUPT OPTIONS

These options effect four skip instructions: DIN0, DIN1, INT0L and INT1H. In the development circuits, these nstructions perform as follows:

- DIN0 — The flip-flop associated with DIN0 will be reset with a positive-going pulse at the input. Upon testing, the skip will occur if the flip-flop is reset.

  DIN1 — Same as DIN0, except that the flip-flop is reset with a negative-going pulse at the input.

- INT0L — The skip will occur if the input level is low (-V).

- INT1H — The skip will occur if the input level is high (VSS).

Mask options are available which will invert these inputs as shown below.

	Standard	Option 1	Option 2
DIN0 Reset F/F	⌐¬	¬_	⌐¬
DIN1 Reset F/F	¬_	¬_	⌐¬
INT0L Skip On	-V	VSS	-V
INT1H Skip On	VSS	VSS	-V

Note that if the reset of the flip-flop is inverted, the Skip on Input Selected Low (SKISL) test is also inverted.

PROGRAMMABLE LOGIC ARRAY (PLA) OPTIONS

The decode matrix can be coded to output any combination of signals on lines RIO1 through RIO8, based on the contents of the accumulator and the carry (C) flip-flop. Development circuits A7698, A7699, A7999, B7698 and B7699 are coded to output the combinations shown below. Note that RIO8 is a copy of the C flip-flop.

Carry	Accumulator					RIO Outputs								7-Segment Display
	8	4	2	1	Hex	8	7	6	5	4	3	2	1	
0/1	0	0	0	0	0	0/1	0	1	1	1	1	1	1	0
0/1	0	0	0	1	1	0/1	0	0	0	0	1	1	0	1
0/1	0	0	1	0	2	0/1	1	0	1	1	0	1	1	2
0/1	0	0	1	1	3	0/1	1	0	0	1	1	1	1	3
0/1	0	1	0	0	4	0/1	1	1	0	0	1	1	0	4
0/1	0	1	0	1	5	0/1	1	1	0	1	1	0	1	5
0/1	0	1	1	0	6	0/1	1	1	1	1	1	0	0	6
0/1	0	1	1	1	7	0/1	0	0	0	0	1	1	1	7
0/1	1	0	0	0	8	0/1	1	1	1	1	1	1	1	8
0/1	1	0	0	1	9	0/1	1	1	0	0	1	1	1	9
0/1	1	0	1	0	A	0/1	1	1	1	0	1	1	1	A
0/1	1	0	1	1	B	0/1	1	0	0	0	0	0	0	-
0/1	1	1	0	0	C	0/1	1	1	1	0	0	1	1	P
0/1	1	1	0	1	D	0/1	1	0	1	1	1	1	0	d
0/1	1	1	1	0	E	0/1	1	1	1	1	0	0	1	E
0/1	1	1	1	1	F	0/1	0	0	0	0	0	0	0	Blank

In the above table, a "1" is a program logic "1". A "0" in the carry flip-flop indicates the reset state. The RIO outputs are positive output logic; that is, a "1" output is the more positive state, the VSS level.

The customer selects the output pattern on RIO1 through RIO8 at ROM order time, and can specify either the above "standard" (emulator) pattern or any desired alternate pattern that meets the needs of his particular application.

SYSTEM DEVELOPMENT AIDS

ASSEMULATOR

A sophisticated Universal Assemulator (assembler and emulator unit) is available for PPS-4/1 systems development. A personality module which is compatible with all members of the PPS-4/1 family connects the Universal Assemulator to a functioning PPS-4/1 microcomputer with very flexible development aids. This unit converts a program written in an easy to use assembler language to the machine language code which is interpreted by a special development version of the PPS-4/1 circuit. The Assemulator also has flexible editing capabilities for modifying the assembly language program and sophisticated debugging capabilities for aiding in checking out the computer program and integrating the microcomputer into the final system configuration.

XPO-1

The XPO-1 is a complete microprocessor system with keyboard and display on a single printed circuit board. XPO-1 is an effective system development tool for the PPS-4/1 microcomputers. XPO-1 provides a cost effective method of familiarizing personnel with the operation, programming, and capabilities of the PPS-4/1 microcomputers. It can be used to develop and debug the software program including assembly, and it can then be used to exercise the program in real-time in prototype equipment.

DEVELOPMENT CIRCUIT AND EVALUATION MODULES

This special development version of the PPS-4/1 MM76 circuit is identical to the production version of the MM76 microcomputer except that there is no read only memory. In place of the read only memory area on the circuit chip, address and memory output bonding points are provided so that leads are brought out to an external memory interface. This allows the program for the PPS-4/1 MM76 development circuit to be stored in an external PROM or RAM memory. The external memory may be as large as 1024 bytes. Consequently, the program may be loaded, debugged and modified as necessary to perform the desired functions for each specific system application until a final program for that application is satisfactory. The program may then be formed in ROM on the production circuit.

The development PPS-4/1 A7699 circuit is available on a module for development and evaluation which may be incorporated directly into the user's equipment for demonstration, product evaluation, etc.

SOFTWARE AND TRAINING

Other system support includes application and programming service software packages and training programs to facilitate easy introduction of the PPS-4/1 microcomputer into the user's system. PPS-4/1 programs may be assembled using FORTRAN IV. The FORTRAN IV program is also available on the General Electric Information Services timesharing system.

THE ULTIMATE LOWEST COST SYSTEM

Rockwell is the microcomputer company which has a full spectrum of microcomputer capabilities ranging from custom circuits at one end of the spectrum to the extremely flexible, almost minicomputer capability of the PPS-8 system. Rockwell is the microcomputer company which has the broad spectrum and the applications staff to assist its customers in obtaining the lowest cost total system to do each specific total system requirements. Rockwell makes use of sophisticated microcomputer architecture using the lowest cost technology so that whatever the complexity of the application, a specific Rockwell system will always be the lowest cost.

THE PPS-4/1 APPLICATION AREAS

The PPS-4/1 family of single circuit microcomputers fits the spectrum of microcomputer application requirements by forming a bridge between the custom circuits at one end of its application area and the PPS-4/2 family of circuits at the other end. The PPS-4/1 family fills in an application niche between the more sophisticated microcomputer families and the less costly custom circuits specifically tailored to specific applications.

The PPS-4/1 allows new low cost products to be conceived, developed, and put into production in moderate quantities. Thereby it meets a specific need in the marketplace for low cost, readily tailorable controller systems.

The PPS-4/1 also provides an opportunity for low cost market evaluation of products which may have a potential of very large production quantities. In these cases, the PPS-4/1 provides a low cost stepping stone to establish demand prior to initiating a custom design for a still more lower cost production custom circuit. The system cost is minimized because the custom circuit can strip away any unneeded capabilities in the PPS-4/1 system to provide the lowest cost most competitive ultimate product and may also have the input output modified to incorporate some of the external hardware in the production version. The final production system development cost is also reduced because the final custom microcomputer can still make use of all of the software developed on the trial production unit.

The PPS-4/1 also provides a capability for a low cost version of a product which may be available in systems having more features and more flexibility when implemented in the larger scale PPS-4/2 or PPS-4 families.

POTENTIAL APPLICATIONS

The PPS-4/1 microcomputer family is designed to facilitate communication with a variety of different kinds of systems ranging from general purpose monitoring and control functions through peripheral equipment controller and multi PPS-4/1 microcomputer systems.

The specific selection of which member of the PPS-4/1 microcomputer family may be used for any specific application is a function of the computational complexity or the specific application. The input/output capabilities of all of the current members of the family are basically identical so that the differences in speacial features and the software to perform the associated functions are the determining factors. For this reason, the applications are unspecific as to which member of the PPS-4/1 family should be used. A few of these applications are discussed in this section.

GENERAL PURPOSE MONITOR/CONTROLLER

A block diagram of the general purpose monitor/controller is shown in Figure 10. This controller makes use of the extensive input and output capabilities of the PPS-4/1 microcomputer circuit and illustrates a possible hierarchy in the assignments of primary and secondary control functions and primary and secondary status inputs.

Input Examples

The signals labeled interrupt inputs are the highest priority inputs and these could be used in control systems where virtually immediate action is called for by the microcomputer.

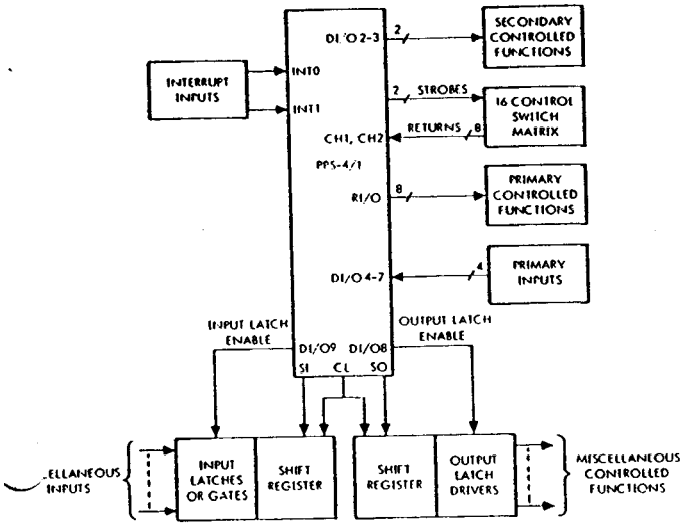


Figure 10. PPS-4/1 GENERAL PURPOSE MONITOR/CONTROLLER

The next level of inputs are the primary inputs that in this example have been assigned to discrete I/O lines of 4 through 7. These would be inputs that require a response from the system but perhaps not as quick a response as the interrupt inputs would.

A 16 control switch matrix such as the one shown in the block diagram could be used to detect momentary switch contacts, limit switches, etc. where not more than one contact would be closed at a time.

The last type of input is illustrated in the general purpose monitor/controller as miscellaneous inputs that feed in through input latches which are enabled from one of the discrete output lines to a serial shift register which is shifted in to be processed on demand.

Output Examples

In the example general purpose monitor/controller, the primary control functions are obtained from the buffered output from the decode matrix or the Accumulator, and the secondary control functions are output from discrete input/output lines (in this particular example, lines 2 and 3).

If more control functions are required, a serial shift register which is loaded from the serial output from the PPS-4/1 may be used. A discrete I/O line is used to transfer the contents from the serial to the parallel external register latches so that they may be held stationary until it is time to change the control functions in some way.

Of course, in a real system application with differing ratios of input to output requirements, the input and output functions of the discrete input/output lines could be completely reassigned. An indefinite number of miscellaneous inputs and miscellaneous outputs may be obtained by adding external parallel-to-serial or serial-to-parallel shift registers as required to get the desired number of input or output parameter signals.

MICROWAVE OVEN CONTROLLER

A microwave oven controller example of a PPS-4/1 microcomputer application is illustrated in Figure 11. In this case, one interrupt line is used to provide real time clock inputs so that cooking time may be accurately measured. The other interrupt is used as an interlock input so that if the microwave oven door is opened a signal is provided to the controller which indicates that cooking is not proceeding. Opening the door will automatically cut off power to the oven without action from the microcomputer; consequently a time out situation exists. Since the real time, 50 or 60 cycles input frequency has a possibility of two values, the discrete input/output line zero identifies to the controller which frequency is actually being applied. For instance, if the oven is being shipped to a country that has 50-cycle power, the selector line could be set to VSS and if it is being sold in a country which has 60-cycle power, the input line could be set to the VDD voltage.

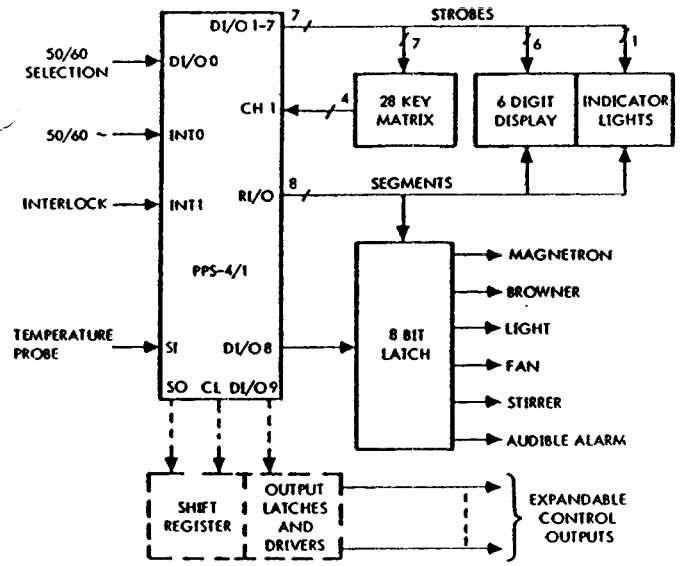


Figure 11. PPS-4/1 MICROWAVE OVEN CONTROLLER

In this controller it is assumed that input parameters are entered by means of a 28-key keyboard. These parameters include: (1) time settings, (2) indications of the type of food being cooked so that cooking rate can be established, (3) whether or not the food placed in the oven is frozen, (4) the desired degree of doneness, etc.

In this example, it is assumed that time information and perhaps other status information is to be displayed in a 6 digit, seven segment decimal display and status indication in 8 status indicator lights. The strobe lines for the key matrix, the 6-digit display and the indicator lights are obtained from one set of seven discrete output lines (DI/O 1-7). The four-bit parallel input to channel one is used for the return lines from the key matrix.

The buffered outputs from the Accumulator or the decode matrix are used as segment drivers for the digit and indicator light sections and also are used as an input to an 8-bit latch circuit which is enabled by the discrete input/output 8 line to provide control signals to the magnitron, browner, light, fan, stirrer and audible alarm devices.

In this specific example, no requirements are specifically identified for the use of the serial input/output capability; however, if there is a requirement for further controls or if the timing function which is available in the circuit is used to control other devices such as a conventional oven or surface cooking units, the shift register outputs may be used as desired.

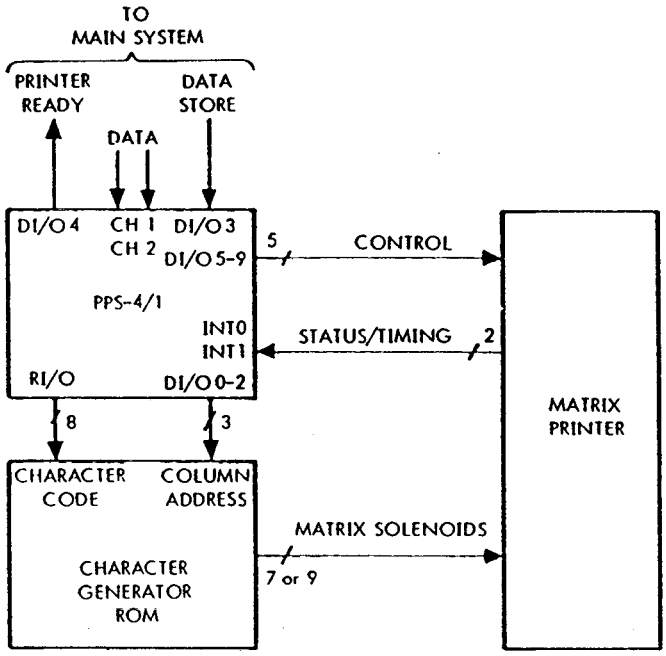
MATRIX PRINTER CONTROLLER

The next potential application shows the use of a PPS-4/1 microcomputer coupled to an external read only memory for character generation for a matrix printer. This is illustrated in Figure 12.

In this case 8-bit data comes to the PPS-4/1 controller over the channel 1 and channel 2 input ports and any necessary handshaking is accomplished through the discrete input/output lines signifying that the printer is ready or that the data is available to be input to the printer controller system.

Control lines to the printer come from discrete input/output lines 5 through 9 and the status and timing information comes back from the printer over the interrupt 0 and interrupt 1 lines. The 8 lines out from the buffered RIO outputs are used to supply a character code to the external ROM and discrete input/output lines zero through 2 are used to identify the vertical column through the character that is to be output to control the matrix solenoid drivers directly from the character generator ROM.

This same general technique could be used any time that there is some type of code conversion and, when necessary, the output from the read only memory could be loaded back into the PPS-4/1 through the serial input port.



NOTES:

1. Self Scan Display 32 Characters
2. AN 101__ Alphanumeric Printer

Figure 12. PPS-4/1 MATRIX PRINTER CONTROLLER

COPIER CONTROLLER

Figure 13 shows another potential application of a PPS-4/1 microcomputer circuit as the primary control element in a copier. Functionally, this block diagram resembles that of the microwave oven controller (Figure 11). The major differences are the use of an external clock, the number of keys in the keyboard, and the number of seven segment displays and status lamps. Of course, the controller program and the significance of each of the input/output lines is tailored specifically to the copier control functions.

In this system, the discrete input/output lines 0 through 5 are used as strobe lines to a 24-key keyboard and four displays and as many as 16 status lamps. The four return lines from the keyboard return to the channel 1 input and the outputs from the Accumulator or the decode matrix are used for selection of the segment and the status lines. These two buffered outputs also provide the input to an 8-bit latch circuit when enabled by the discrete input/output line 6 signal. Preliminary status inputs come in through channel 2 and the primary control functions are output from the 8-bit latch circuit. Another input comes in through discrete input/output line 8 and the motor on/off control is a discrete output from discrete input/output 7. An interrupt line is used as an interlock that will inhibit operation of the system when a cabinet door is opened.

This example illustrates the use of an external square wave oscillator to provide clock signals to the controller so that instruction operation time is precisely controlled. Internal timing functions may be accomplished to a precision equivalent to the precise clock cycle time by counting instruction cycles and adjusting appropriate internal counters as required.

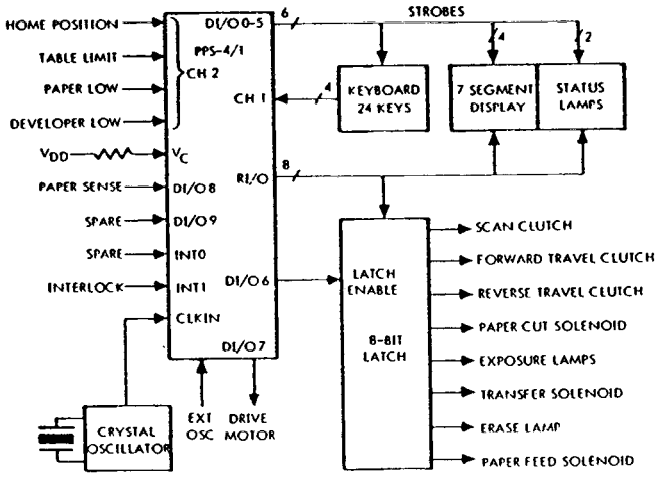


Figure 13. PPS-4/1 COPIER CONTROLLER

CREDIT CHECKING TERMINAL

A block diagram of a PPS-4/1 microcomputer circuit applied to a credit checking terminal is shown in Figure 14. The functions of this terminal are to accept information from a 48-key matrix which inputs the customer identification number and amount of purchase, to display this information on a 6-digit display and to transmit this information through a UART and a modem over a telephone line to a central credit agency. The controller then is implemented to receive credit verification information over a telephone line through a modem back to the UART and to display the results of that verification on indicator lights associated with the display.

Most of the techniques used with this application have been discussed in earlier examples with one exception. The DS signal going from the PPS-4/1 to the UART is derived from the serial output channel using that output as an additional discrete output. The status of the most significant bit in the S Register is always available on the serial output channel so that when the serial output capability is not required that line may be used as an

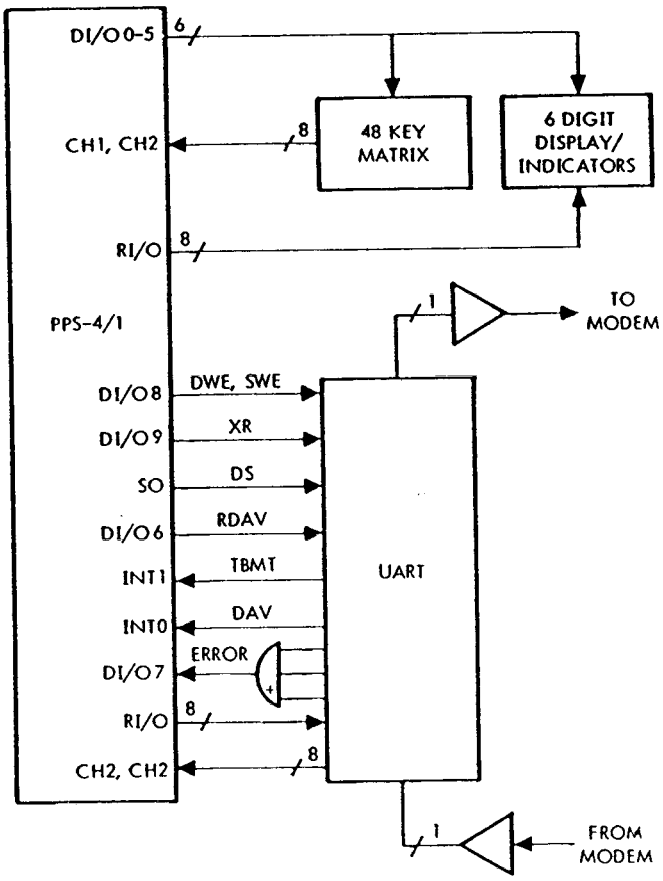


Figure 14. PPS-4/1 CREDIT CHECKING TERMINAL (PARALLEL INTERFACE)

additional discrete. Note that the serial output capability can also be used as a pulse output which is 2 or 4 or 6 clock cycles wide. This is accomplished by outputting serial four bit word with one of the following bit patterns: 0100, or 0110 or 0111.

The error indication on discrete input/output line 7 is derived from an OR gate which combines the three classes of error indications provided by the UART. If more detailed information is required, then the serial input/output capability could be used for providing the control and status information between the UART and the PPS-4/1 circuit.

ANALOG INTERFACE

A PPS-4/1 system may also be used in applications which have a primary interface which is analog. There are many digital to analog and analog to digital converters available which may be interfaced with a PPS-4/1. A PPS-4/1 may provide this interface directly when coupled with an appropriate network. A block diagram for such a system is shown in Figure 15.

In this example, the buffered outputs from the Accumulator or decode matrix are used to drive a resistor network. This network ratios the voltage reference into the network as controlled by the bit pattern supplied from the Accumulator or decode matrix. The voltage generated is applied to an operational amplifier. The resulting voltage is directly proportional to the 8-bit number output.

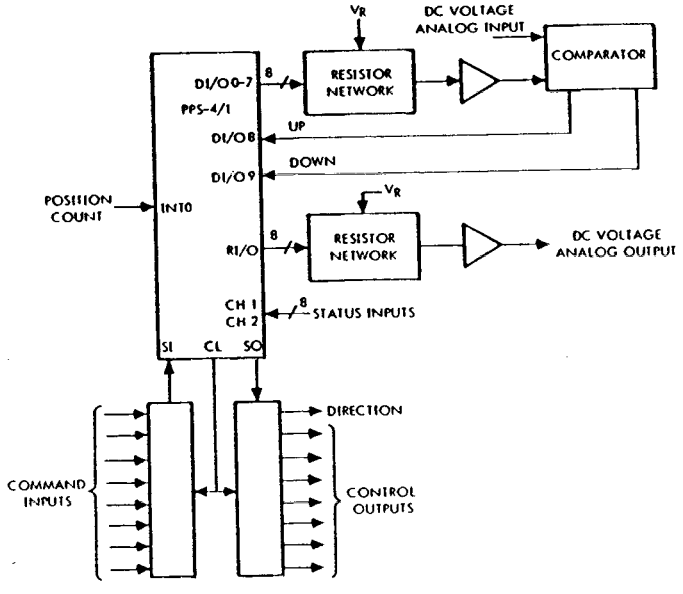


Figure 15. PPS-4/1 ANALOG INTERFACE

A similar network is driven from discrete input/output lines zero through 7 through an operational amplifier to a comparator to provide a DC voltage analog to digital conversion capability. In this case, the unknown analog voltage is compared with the voltage derived from the resistor network. The output of the comparator provides up or down control signals through discrete input/output lines 8 or 9. The software in the PPS-4/1 then modifies the number output to the resistor network in a successive approximation technique until the voltage derived from the network matches the unknown analog input. When the match occurs, the digital number output through the discrete channels is identical to the representation of the analog input.

If the DC voltage analog output is driving a servo motor and its shaft provides an incremental feedback as the shaft rotates, the interrupt zero (INT0) line may be used to provide continuous updating to the PPS-4/1 system so that the servo can be controlled by an internally stored profile of error magnitude versus output voltage control signal desired. Since the motor may be driven in either direction, an output from the serial output is used to indicate direction. The remaining input/outputs from the serial I/O are used in this example as status inputs, command inputs and control outputs. The control outputs may be controlling an external analog multiplexer and sample and hold circuits so that the digital to analog conversion and the analog to digital conversion networks shown may be multiplied over several channels.

LOW COST CASH REGISTER

The low cost cash register example shown in Figure 16 illustrates another capability which is available in the PPS-4/1 microcomputer system. This capability allows more than one PPS-4/1 microcomputer to be used in a system.

Communication between PPS-4/1 microcomputers can be accomplished over any of the input/output lines. In this specific example, the communication is accomplished through the serial input and output lines of both PPS-4/1 units.

Handshaking information and status information is communicated over the discrete input/output lines 8 and 9 in one unit and 3 and 4 in the other unit to establish a communications protocol between the two units. The unit that has data ready to transmit indicates over its data ready I/O line and the unit which will receive the data indicates over its receiver ready line that communication can now occur. The transmitting PPS-4/1 then outputs the contents of its S Register to the receiving PPS-4/1 S Register. The clock circuits may be tied together without interference since in a nonoperating status the clock lines float. The transmitting unit clocks the information into the receiving unit and turns off the data ready signal. The receiving system shifts the information into its S Register under control of the external shift clock and turns off the

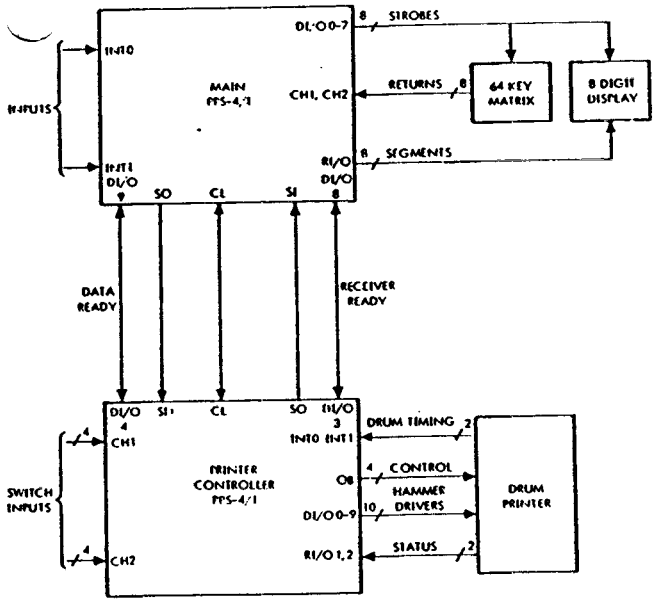


Figure 16. PPS-4/1 LOW COST CASH REGISTER

receiver ready signal until the data is removed from the S Register. Of course, at the same time that the second unit is shifting information in, it may be shifting information out so that an exchange of information may be readily accomplished at the same time.

In this particular application, one of the PPS-4/1 microcomputers is used as the primary controller for the cash register and handles the primary inputs and the display functions. The second unit provides the primary control for a print mechanism and may provide additional computations such as tax tables.

APPLICATIONS SUMMARY

The potential applications which have been outlined are intended to illustrate various techniques which may be used in specific applications in any combination as required. The examples illustrate the input/output flexibility, expandability, and compatibility with both analog and digital external systems. The flexibility of the PPS-4/1 microcomputer family allows incorporation as a complete controller, as a shared controller with other PPS-4/1 microcomputers or as a peripheral control device for working in more sophisticated computer systems.

APPENDIX A
MM76E EXTENDED INSTRUCTION MEMORY VERSION

INTRODUCTION

The MM76E extended instruction memory version of the MM76 has all of the features of the basic MM76 but provides 1024 8-bit bytes of program memory (8192 bits).

READ ONLY MEMORY (ROM)

The extended ROM is mapped as shown in Table 3, page 11 with the addition of pages 8 through 13 to the general program area. The off page transfers (TL) and subroutine calls by TML extend to all of the pages from 0 through 13 (Hex 000 thru 37F). The power-on location (#1CO) is unchanged.

DEVELOPMENT AIDS

The development circuits, part nos. A7699 and A7698, have pin-outs for the 10-bit program counter which allows them to exactly emulate the MM76E with 1024 bytes of external memory. Consequently all development aids for the MM76 are applicable to the MM76E without modification.

APPENDIX B
MM75 28-PIN PACKAGE VERSION

INTRODUCTION

The MM75 one-chip microcomputer is a reduced I/O version of the basic MM76. The reduction in I/O allows packaging in a 28-pin dual in-line configuration to fit the lowest cost requirements of equipment designers. The ROM, RAM, and CPU are identical to the basic MM76. The modified I/O is described herein.

MM75 MODIFIED FEATURES

The reduced pin-out configuration results in the following changes to the basic MM76.

S REGISTER - SERIAL INPUT/OUTPUT - SHIFT COUNTER

The S Register is retained as a 4-bit auxiliary storage register. The serial in, out, and shift clock have been eliminated. The IOS, serial input/output instruction should not be executed at any time.

DISCRETE INPUT/OUTPUT PORTS

One discrete input/output port DI/O9 was eliminated. The remaining nine DI/O ports are as described for the basic MM76.

CONDITIONAL INTERRUPTS

The conditional interrupt request pin, INT1, has been eliminated. Internally to the MM75 device the INT1 line and associated flip-flop are connected to the most significant bit of channel B (RIO8). This allows the use of the INT1H and DIN1 instructions as described for the basic MM76 with a modified procedure. Whereas the MM76 INT1 signal was only available as an input, the RIO8 signal may be used for input or output. To use RIO8 as an input to be tested by the INT1H or DIN1 instructions a logic 1 in the most significant bit position must first be output in order to float the RIO8 output driver. If the flip-flop is to be tested, then following floating the RIO8 output, a DIN1 should be executed to set the flip-flop while ignoring the skip condition. The flip-flop is now preconditioned to be reset if the RIO8 input makes a negative transition, which can be sensed by a subsequent DIN1 instruction.

CHANNEL 2

The channel 2 4-bit input port is removed. The associated instruction, I2C, should not be executed at any time.

CLOCK CONTROL

The $\overline{B}$ clock output was removed. This signal was intended for possible use in synchronizing external logic. Equivalent information may be derived from the A clock output if required. The EXCLK and CLKIN pins were removed and the signals internally masked to cause operation on internal clock.

MM75 DEVELOPMENT AIDS

The development circuits, part nos. A7699 and A7698, are available to support MM75 program development and prototyping.

Use of the A7699 in the Universal Assemulator requires the use of EXCLK and CLKIN to synchronize with the rest of the Assemulator. The INT1 condition can be simulated by connecting the RIO8 line to the INT1 line. The serial clock should be tied to VDD to insure that the S Register is not shifted because of external clocking. The remainder of the modified I/O signals can be accurately emulated simply by not executing the associated I/O instruction.

The A7698 can be used for prototyping purposes in the same manner but in this case the EXCLK and CLKIN can be tied to VSS and VDD respectively to run with the internal clock.

ELECTRICAL INTERFACE

The electrical specification and pin-out information is in Tables B-1 and B-2.

Table B-1. MM75 ELECTRICAL SPECIFICATIONS

RATING CHARACTERISTICS

Supply Voltage:
VDD = -15 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)
VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies:
80 kHz ±50% with external resistor

Device Power Consumption:
75 mw, typical

Input Capacitance:
<5 pf

Input Leakage:
<10 μa

Open Drain Driver Leakage (R OFF):
⩽ 10 μa at -30 Volts

Operating Ambient Temperature (TA):
0°C to 70°C (TA = 25°C unless otherwise specified)

Storage Temperature:
-55°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +0.3 volts.

Input/Output	Symbol	Limits (VSS = 0) Min	Typ	Max	Limits (VSS = +5V) Min	Typ	Max	Timing (Sample/ Good)	Test Conditions
Supply Current (Average) for VDD	I_{DD}		5 ma	8 ma		5 ma	8 ma		VDD = -15.75V T = 25°C
Discrete I/O's	V_{IH}	-1.0V			+4.0V			Ø3 & Ø4	
DI/O 0-DI/O 8	V_{IL}			-4.2V			+0.8V		
DI/O 0-5	R_{ON}			500 ohms			500 ohms	Ø2*	3.0 ma max.
DI/O 6-8	R_{ON}			400 ohms			400 ohms		
Channel 1 Input	V_{IH}	-1.5V			+3.5V			Ø1	
PI1-PI4	V_{IL}			-4.2V			+0.8V		
I/O Channel A	V_{IH}	-1.5V			+3.5V			Ø3	
RI/O1-RI/O4	V_{IL}			-4.2V			+0.8V		
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max.
I/O Channel B	V_{IH}	-1.5V			+3.5V			Ø3	
RI/O5-RI/O8	V_{IL}			-4.2V			+0.8V		
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max.
INT0	V_{IH}	-1.5V			+3.5V			Ø3	
	V_{IL}			-4.2V			+0.8V		
Clock	V_{OH}	-1.0V			+4.0V			-5.0V	CL = 50 pf (max)
A	V_{OL}			-10.0V			-5.0V		
VC***	V_{IH}								56K ±5%
	V_{IL}								
PO	V_{IH}	-2.0V			+3.0V				Special circuit
	V_{IL}			-6.0V			-1.0V		

*State established by Ø2 (minimum impedance after Ø4).
**Same as above except Ø4 minimum at Ø2 of next cycle.
***Connect VC to VDD through a resistor: 56 KΩ for 80 kHz or 47 KΩ for 100 kHz.

Table B-2. PPS-4/1 MM75 SIGNALS (Part No. A75XX)

Pin No.	Signal Name	Function
1	RIO8/INT1	B I/O Channel bit 4/Interrupt 1
2	RIO1	A I/O Channel bit 1 (least significant bit)
3	RIO2	A I/O Channel bit 2
4	RIO3	A I/O Channel bit 3
5	RIO4	A I/O Channel bit 4
6	DI/O0	Discrete I/O line 0
7	DI/O1	Discrete I/O line 1
8	DI/O2	Discrete I/O line 2
9	DI/O3	Discrete I/O line 3
10	DI/O4	Discrete I/O line 4
11	DI/O5	Discrete I/O line 5
12	DI/O6	Discrete I/O line 6
13	DI/O7	Discrete I/O line 7
14	VSS	VSS positive power supply
15	DI/O8	Discrete I/O line 8
16	A	A System Clock
17	VC	Resistor frequency control
18	VDD	-15 Volt Supply (1st pin)
19	TEST (VSS)	Commands Test Mode (VSS Normal Operation)
20	PI1	Channel 1 bit 1
21	PI2	Channel 1 bit 2
22	PI3	Channel 1 bit 3
23	PI4	Channel 1 bit 4
24	PO	Power On Reset Input
25	INT0	Interrupt 0 Input
26	RIO5	B I/O Channel bit 1
27	RIO6	B I/O Channel bit 2
28	RIO7	B I/O Channel bit 3

APPENDIX C
MM76C HIGH SPEED COUNTER VERSION

INTRODUCTION

The MM76C one-chip microcomputer, Part No. A79XX, is based on the MM76 microcomputer, but has the added capability of a high speed counter system and an increased number of I/O ports associated with the counter. Because of the increase in I/O, the MM76C is packaged in a 52-pin, quad in-line, plastic package. The ROM, RAM, and CPU functions are identical to the basic MM76. The additional and modified features of this versatile device are described in this Appendix.

The socket for the 52-pin MM76C is Burndy Corporation, P/N DILE-52P1. It is available from Burndy Corporation; 931 South Douglas; El Segundo, California 90245.

MM76C ADDITIONAL/MODIFIED FEATURES

1. High Speed Counter, which can be programmed to function as one 16-bit counter or two independent 8-bit counters.
2. Counter operates at 1 MHz, counts up or down.
3. Operates in two input modes: Event input and quadrature inputs.
4. Automatic preset operation (Automatic reload of counter with preset value).
5. Serial 8-bit input/output option with start pulse detection capability.
6. Multiple programmable operating modes.
7. Three modes of clock operation (External crystal input capability for precision clock frequency).
8. Eight additional I/O lines associated with high speed counter.
9. Slightly modified instruction set functions and additional I/O functions related to counter system operation. Instruction set is identical to MM76 allowing use of same assembler.

The changes to the instruction set combines the functions of the SEG1 and SEG2 instructions into a single SEG1 instruction and adds a new instruction using the SEG2 operation code. The SEG1 instruction outputs 8 bits from the Decode Matrix into Channel A and Channel B. The new instruction function for SEG2 initiates the counter mode of operation.

SYSTEM DESCRIPTION

GENERAL

The high speed counter can be program-controlled to function as one 16-bit counter or as two independent 8-bit counters. The two portions of the counter, designated as the Lower Counter and the Upper Counter, are shown in the MM76C Block Diagram, Figure C-1.

When configured as one 16-bit counter the Lower Counter accepts the input(s) and provides a carry to the Upper Counter. The Upper Counter provides the most significant 8-bits and a carry output to CA16/D.

Each counter has a corresponding data holding register designated Upper Data Register and Lower Data Register. The data in either or both counters can be parallel transferred to the corresponding data holding register when the SEG2 instruction is executed. This transfer is performed without disturbing the count in the counter.

The Lower Counter and Lower Data Register and the Upper Counter and Upper Data Register can be operated independently (each with its own carry output), and each has certain unique operating characteristics. These unique operations of the counters and data registers are controlled by the 4-bit Control Register and the three Control Flip-Flops, (CR1, CR2, and CR3).

The Lower Counter can accept two different types of serial data inputs and count them either up or down. In one input mode (Event), any data input at PC1 will be counted at rates up to 1 MHz, and the control input at PC2 determines if the count is to be up or down. In the other input mode (quadrature), the Lower Counter Input Logic decodes the quadrature input prior to counting. The quadrature input is typical of inputs received from standard incremental pickoffs and consists of two signals 90 degrees out of phase. One signal is input at PC1 and the other at PC2. Reversing these two inputs or shifting the phase relationship of the signals will reverse the up/down direction of the counter. In this mode, the counter counts each transition of both inputs at rates up to 250 kHz on each input.

In the quadrature mode, when reversing the direction of count, certain minimum timing requirements must be considered. Figure C-2 shows a count reversal from an up-count to a down-count. Note that an up/down reversal occurs at point B. This reversal cannot occur sooner than 1 µs after the last up-count. The next count (the first down-count) occurs concurrently with the reversal since the logic now indicates a count-down state.

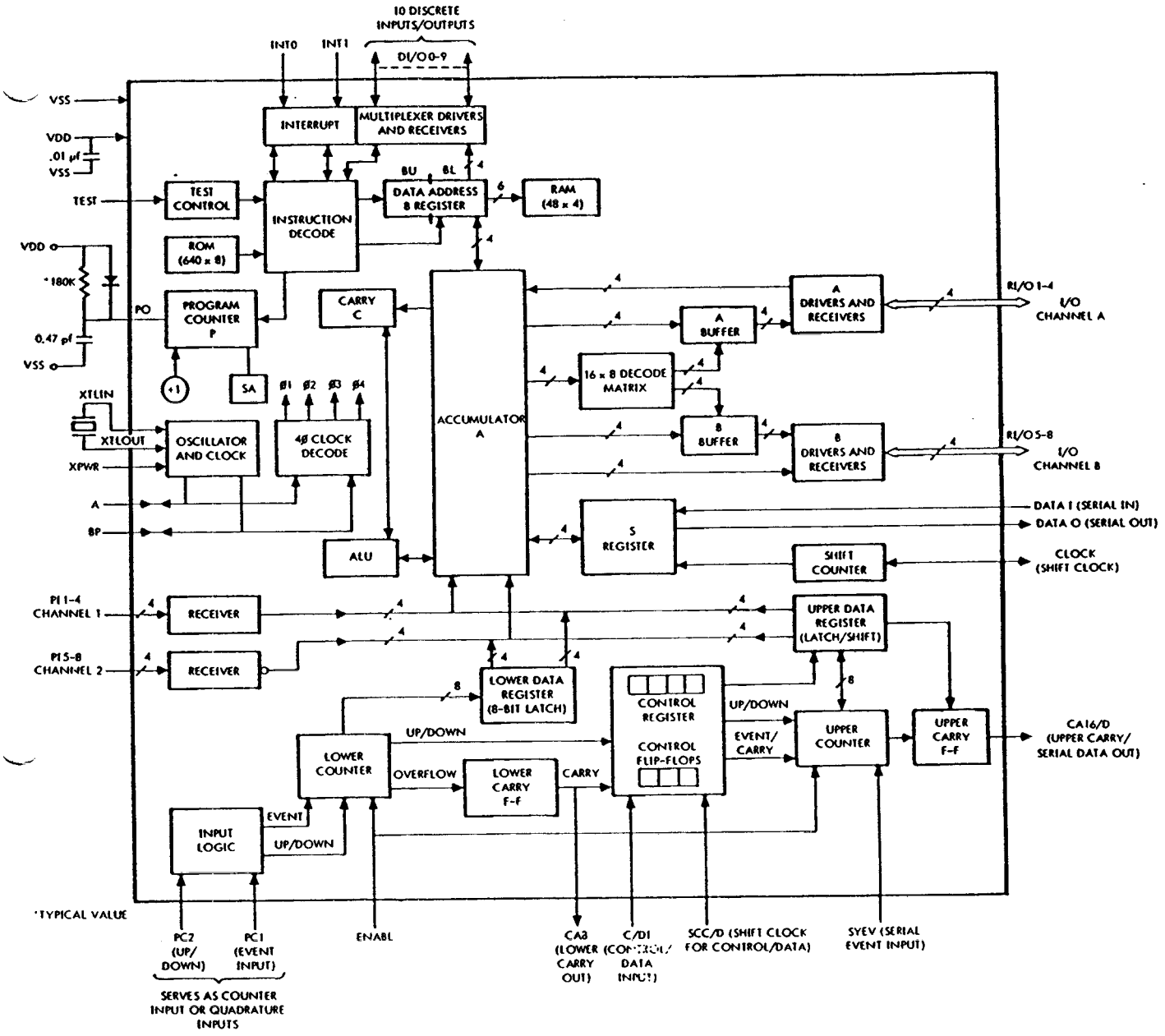


Figure C-1. PPS-4/1 MM76C BLOCK DIAGRAM

A special count/reversal case exists when operating as a 16-bit counter. If the last up-count (point A in Figure C-3) produces a carry from the Lower Counter to the Upper Counter, the reversal and first down-count (point B) will occur as described in the preceding paragraph. However, a second reversal (point C) cannot be permitted for at least 3-bit times of the microprocessor A clock, or the carry from the Lower Counter to the Upper Counter may not be propagated properly.

The count in the Lower Counter is parallel transferred to the Lower Data Register on command without disturbing the counting operation. The transfer occurs during Phase 1 time when no ripple carry is being propagated.

The Lower Data Register is an 8-bit DC latching register which will retain the data received from the Lower Counter until another load transfer is executed. The data can be copied into the Accumulator on command.

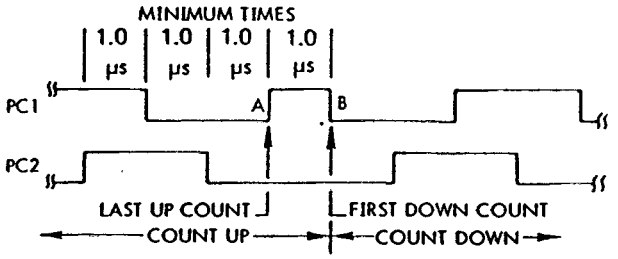


Figure C-2. COUNT REVERSAL TIMING

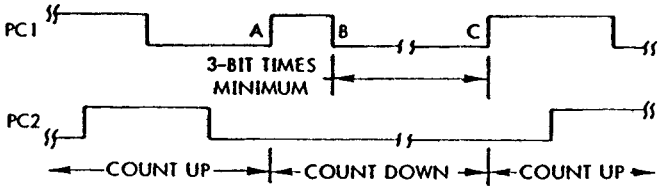


Figure C-3. COUNT DOUBLE REVERSAL TIMING

The Upper Data Register has two major functions. First, it can accept 8-bit parallel data from the Upper Counter for subsequent transfer to the Accumulator or external circuits by shifting the data through the carry port, or it can transfer data to the Upper Counter to preset that counter to any required value. Second, it can operate as a shift register. External data may be shifted into the Upper Data Register from the C/DI input under control of the SCC/D shift clock, and data may be shifted out through the Upper Carry Flip-Flop under control of the same SCC/D shift clock.

The Upper Counter can accept three different inputs: an event input (overflow) from the Lower Counter when in the 16-bit counter mode, an external event input (SYEV) when in the two 8-bit counter mode, and an 8-bit parallel input from the Upper Data Register. The parallel input from the Upper Data Register allows the Upper Counter to be preset with the value that has been shifted into the Upper Data Register.

COUNTER OPERATION AND CONTROL

Operation of the counter is controlled by the 4-bit Control Register and three Control Flip-Flops (CR1, CR2, and CR3).

The Counter Read Instruction SEG2 initiates the Counter Mode. The Counter Mode transfers the Upper and Lower Counter data to corresponding Upper and Lower Data Registers (see Figure C-1) without losing any counts and enables the Control Flip-Flops and Control Register to perform as follows:

1. Configures the Upper and Lower Counters into one 16-bit counter or two 8-bit counters (8-bit Lower Counter and 8-bit Upper Counter).

2. Allows input to the Lower Counter to be clocked with either UP/DOWN control or operate in quadrature mode.

3. Allows inputs to the Upper Counter to count either up or down when in the two 8-bit counters mode.

4. Allows an automatic transfer of preset data from the Upper Data Register to the Upper Counter when the Upper Counter overflows.

5. Allows the software to preset Upper Counter via the IBM instruction.

6. Allows the Upper Data Register to be loaded serially via Control/Data Clock ports and to be serially shifted out through the Upper Carry/Data output, or transfer its preset data in parallel into the Upper Counter.

7. Allows resetting of Lower, Upper, or both Counters independently as required via the IAM instruction and the control situation.

8. Allows reading of the Lower and Upper portions of the Counter without resetting, inhibiting, or disturbing the count in either the corresponding Data Register or Counter by properly sequencing I1 and I2C instructions.

Instruction SEG2 followed by an I1 instruction reads the four least significant bits of Lower Data Register into Accumulator. When followed by I2C instruction, it reads the four most significant bits of the Lower Data Register. Similarly, when followed by a second I1 and I2C instructions, the Upper Data Register is read into the Accumulator in 4-bit increments. The program will exit the counter mode after accomplishing the execution of a second I2C. See sample flow chart, Figure C-4.

By means of one SEG2, I2C instruction, the Upper Data Register may be loaded serially via the Serial Control Data input and its corresponding Shift Clock Control/Data input. By using two SEG2 instructions, control data may be shifted serially into the 4-bit Control Register (see Figure C-1) to set up the control functions.

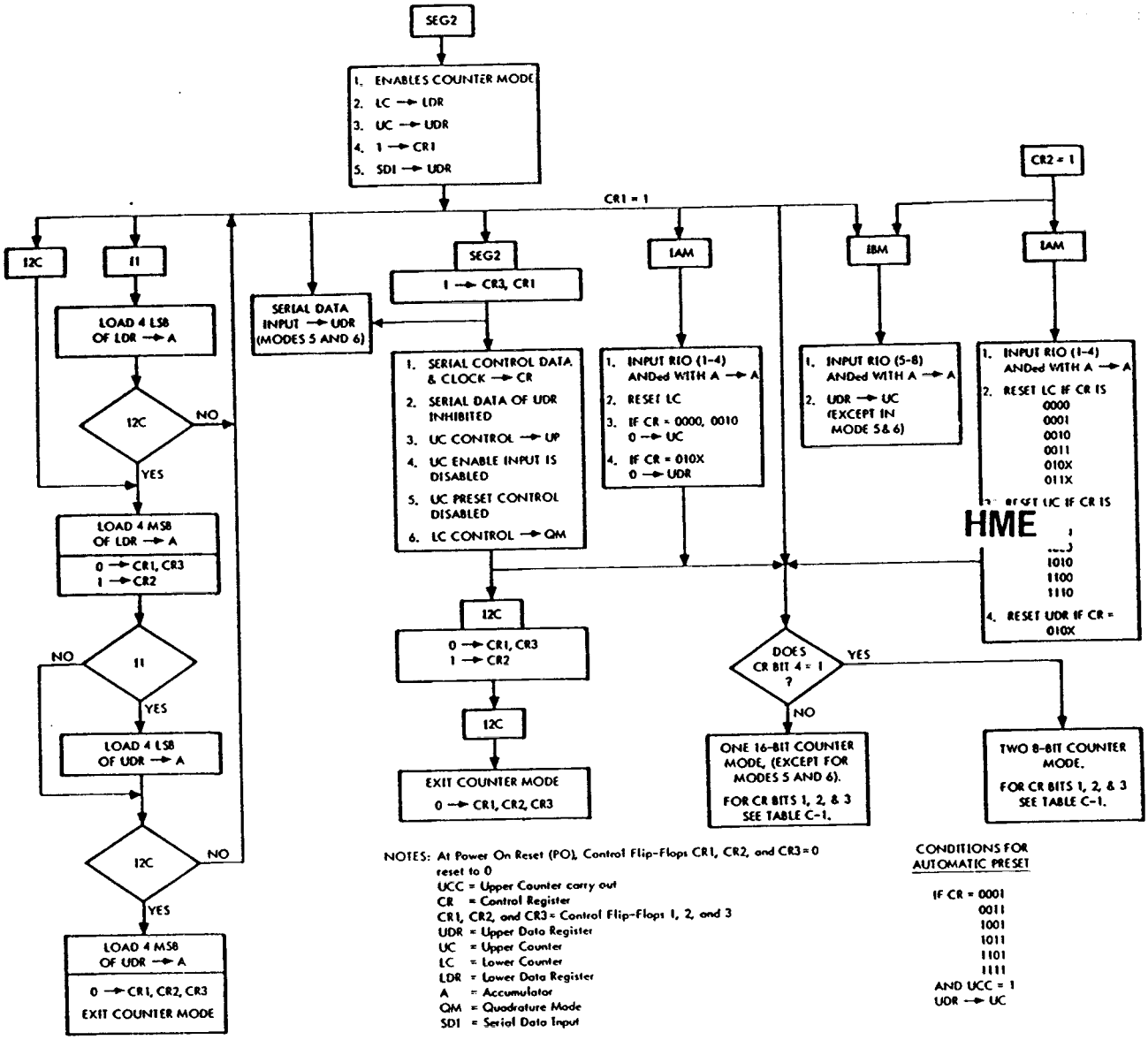


Figure C-4. OPERATION EXAMPLE, SEQUENCE DIAGRAM

The Lower Counter has an external Enable Input. When this Enable Input is high (VSS), the Lower Counter counts all inputs. When low (VDD), the Lower Counter input is disabled. The Enable Input also controls the Upper Counter in the 16-bit counter mode. The Upper Counter Event input is only enabled when in the two 8-bit counter mode.

CONTROL FLIP-FLOPS OPERATION

The Control Flip-Flops set up three states (CR1, CR2, and CR3) and is entered by issuing a SEG2 instruction. This truction stores the present count of the Lower and Upper unters in the respective Lower and Upper Data Registers (see Figures C-1 and C-5) and sets Control Flip-Flops state to CR1. The functions of each of the three states are described in the following paragraphs.

CR1 F/F

A. Instruction I1 causes the least significant 4 bits of the Lower Data Register to be loaded into the Accumulator.

B. Instruction I2C causes the most significant 4 bits of Lower Data Register to be loaded into the Accumulator. Resets CR1 and CR3. Sets CR2.

C. Instruction IAM loads inputs RI/O 1-4 into Accumulator and resets the Lower Counter or when in the two 8-bit

counter mode the Upper Counter, or both counters when in the 16-bit counter mode.

D. Instruction IBM causes the Upper Counter to be loaded with the data in the Upper Data Register in accordance with the control Register states and also loads Accumulator with inputs RI/O 5-8.

E. Instruction SEG2 sets control flip-flop CR3.

F. Causes the serial data input C/DI (with Clock) to be loaded serially into the Upper Data Register unless CR3 is true.

G. All other instructions are performed in the normal way.

CR2 F/F

A. Instruction I1 causes the least significant 4 bits of the Upper Data Register to be loaded into the Accumulator.

B. Instruction I2C causes the most significant 4 bits of the Upper Data Register to be loaded into the Accumulator and resets CR2 and exits the counter mode.

C. Statements C, D, F, and G under CR1 mode above also apply.

CR3 F/F

A. Serial Data Input C/DI (with Clock) is loaded into Control Register and inhibited from loading into Upper Data Register.

B. If no serial control information is loaded,

1. the Upper Counter up/down control is forced to up, the
2. Lower Counter input control is forced to Quadrature Mode, the
3. Upper Counter enable control is disabled, and the
4. Upper Counter preset control is disabled.

CONTROL REGISTER FUNCTIONS

The Control Register provides the 14 different counter modes listed in Table C-1. The 14 states of the Control Register, combined with the three Control Flip-Flop states, sets up logic to control the configurations and functions of the Upper and Lower Counters (two 8-bit counters or one 16-bit counter) and functions of the Upper and Lower Counters and associated Data Registers as shown in Figure C-5. Table C-1 provides a brief description of each of the 14 modes of counter operation.

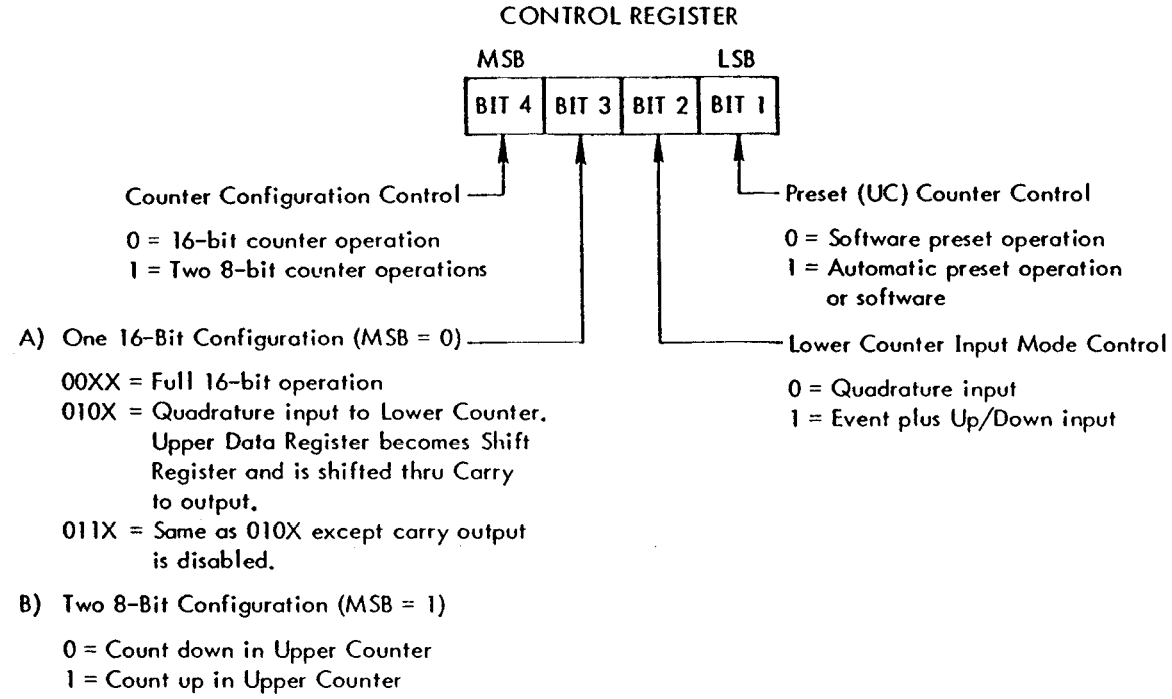


Figure C-5. CONTROL REGISTER OPERATION

Table C-1. DESCRIPTION OF THE 14 MODES OF COUNTER OPERATION

Mode	Control Register Bit Config. 8 4 2 1	One 16-Bit Counter	Two 8-Bit Counters	UDR is Shift Register	Lower Counter Input	Upper Counter Input	*Reset By: Lower	*Reset By: Upper	Preset Upper Counter	Up/Down Control: Lower	Up/Down Control: Upper	Enable Input: Lower	Enable Input: Upper
1	0 0 0 0	X			Q	LC	(1) (2)	(1) (2)	(3)	QPR	LC	X	X
2	0 0 0 1	X			Q	LC	(1) (2)		(3) (4)	QPR	LC	X	X
3	0 0 1 0	X			E	LC	(1) (2)	(1) (2)	(3)	PC2	LC	X	X
4	0 0 1 1	X			E	LC	(1) (2)		(3) (4)	PC2	LC	X	X
5	0 1 0 X	X**		X***	Q		(1) (2)			QPR		X	
6	0 1 1 X	X**		X***	E		(1) (2)			PC2		X	
7	1 0 0 0		X		Q	E	(1)	(2)	(3)	QPR	Down	X	X
8	1 0 0 1		X		Q	E	(1)		(3) (4)	QPR	Down	X	
9	1 0 1 0		X		E	E	(1)	(2)	(3)	PC2	Down	X	X
10	1 0 1 1		X		E	E	(1)		(3) (4)	PC2	Down	X	X
11	1 1 0 0		X		Q	E	(1)	(2)	(3)	QPR	Up	X	X
12	1 1 0 1		X		Q	E	(1)		(3) (4)	QPR	Up	X	
13	1 1 1 0		X		E	E	(1)	(2)	(3)	PC2	Up	X	X
14	1 1 1 1		X		E	E	(1)		(3) (4)	PC2	Up	X	X

*Both Lower and Upper Counters and Data Registers are reset by POI, and Control Register is forced to Mode 1.

**In Modes 5 and 6, since the UDR is functioning as a Serial Shift Register, only the LC can be read. If UC needs to be read, exit Modes 5 or 6 and enter Mode 1, 2, 3, or 4.

***IAM (CR1+CR2) Resets UDR

(1) = IAM CR1
(2) = IAM CR2
(3) = IBM (CR1+CR2)
(4) = Automatic Preset (UDR → UC)

UDR = Upper Data Register
Q = Quadrature Input
E = Event Input
LCC = Carry from Lower Counter
UCC = Carry from Upper Counter

D = Down (count down)
U = Up (count up)
QPR = Quadrature phase relationship

CLOCK CONTROL (XTLIN, XTLOUT, XPWR, AND OSCILLATOR)

The clock system in the MM76C device can be configured in the following three modes:

A, BP Mode (Slave)
Internal OSC Operation (A, BP Out)
Crystal Driven

The first mode allows the chip to be driven by the external A and BP clocks. The second mode permits internal clock operation. The third mode allows a crystal input into the chip. The chip is designed to interface to a TV crystal (3.57 MHz) and is scaled down inside the chip to 89 kHz operation. Crystal driven clock allows for precision in timing whenever necessary. Internal clock operation is centered around 100 kHz ±25% tolerance.

The specific definition of the clock waveforms is shown in Figure C-6 and is basically the same as the MM76 device as discussed in the MM76 section on Electrical Interface.

The connections required to select the desired mode of clock operation are provided in the following matrix:

Mode	A I/O Pin 26	BP I/O Pin 25	XPWR Pin 23	XTLIN Pin 22	XTLOUT Pin 24
Slave (A, BP external input)	A In	BP In	VSS	VSS	NC
Internal Osc. (A, BP Output)	Output	Output	VSS	VDD	NC
External Crystal Driven (A, BP Output)	Output	Output	VDD	XTL	XTL

NC = No Connection (not used)
XTL = Connection to external crystal

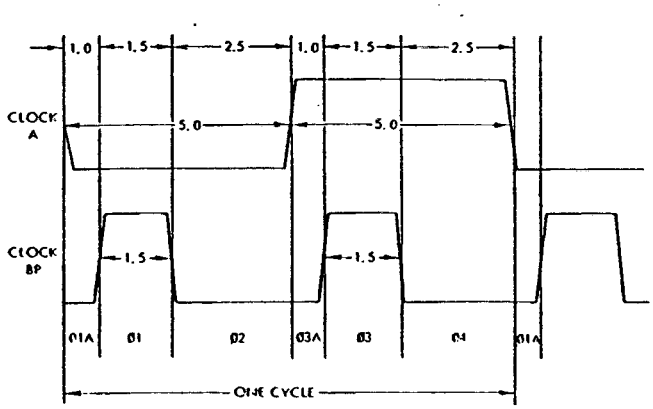


Figure C-6. TYPICAL CLOCK WAVEFORM (Normalized)

PPS-4/1 MM76C INSTRUCTIONS

The instruction set for the MM76C is essentially the same for the MM76 except functions of the SEG1 and SEG2 instructions have been combined into a single SEG1 instruction and a Counter Control instruction has been added which uses the SEG2 operation code.

Execution of the SEG2 instruction will cause the MM76C to enter the Counter Mode of operation and in this mode four of the input/output instructions will execute specialized functions as shown in Table C-2.

Table C-2 gives a brief description of the input/output instructions in the "Non Counter Mode" as well as in the "Using Counter Mode". A more detailed description of the function of these instructions is provided in the SYSTEM DESCRIPTION paragraph.

Table C-2. PPS-4/1 MM76C INPUT/OUTPUT INSTRUCTION SET

Op Code	Bytes	Cycles	Description
Input/Output Instructions (Non-Counting Mode)			
SOS	1	1	Set output, bit selected by B Lower (B Upper = 3) to VSS
ROS	1	1	Reset output, bit selected by B Lower (B Upper = 3) to -V
SKISL	1	1	Skip on Input Selected Low on bit selected by B Lower (B Upper = 3) Bit sampled during prior cycle.
IBM	1	1	Input Channel B ANDed with Accumulator, results to Accumulator
OB	1	1	Output from Accumulator to Channel B
IAM	1	1	Input Channel A, ANDed with Accumulator, results to Accumulator
OA			Output from Accumulator to Channel A
IOS	1	1	Serial input and output from S — shifting takes 8 cycles concurrent with other instruction operations

Table C-2. PPS-4/1 MM76C INPUT/OUTPUT INSTRUCTION SET (continued)

)p Code	Bytes	Cycles	Description
Input/Output Instructions (Non-Counting Mode) - (continued)			
I1	1	1	Input Channel 1 to Accumulator
I2C	1	1	Input Channel 2 to Accumulator and complement
INT1H	1	1	Skip on INT1 equals VSS on input pad
DIN1	1	1	Skip if INT1 flip-flop is reset and set INT1 flip-flop
INT0L	1	1	Skip on INT0 equals -V on input pad
DIN0	1	1	Skip if INT0 flip-flop is reset and set INT0 flip-flop
SEG1	1	1	Decode combined memory, Carry flip-flop, and Accumulator and output 8 bits to Channel A and Channel B
Input/Output Instructions (Using Counter Mode)			
SEG2	1	1	Transfers Upper and Lower Counter data to corresponding Upper and Lower Data Registers, and enables Counter Read mode. If in Automatic Preset mode, SEG2 does not transfer Upper Counter. **NOTE** A second SEG2 instruction will switch input serial Control/Data line from the 8-bit Upper Data Register to the 4-bit counter Control Register.
IAM	1	1	Input Channel A, ANDed with Accumulator results to Accumulator. Clears appropriate counters as follows: (A) In 16-bit counter mode, IAM clears both counters (B) In two 8-bit counters mode, IAM clears the counter selected as follows: IAM · CR1 clears Lower Counter IAM · CR2 clears Upper Counter
IBM	1	1	Input Channel B, ANDed with Accumulator, results to Accumulator. Presets Upper Counter with data from Upper Data Register.
I1	1	1	If before I2C instruction, reads LS4 bits of Lower Data Register into Accumulator. If after I2C instruction, reads LS4 bits of Upper Data Register into Accumulator.
I2C	1	1	The first I2C instruction reads MS4 bits of Lower Data Register into Accumulator and sets up read of Upper Data Register. The second I2C instruction reads MS4 bits of Upper Data Register and exits Counter mode.

ELECTRICAL INTERFACE

The electrical specifications are the same as those for the MM76 device, except for the additional input/outputs associated with the high speed counter. These differences are shown in Table C-3.

Complete pin-out information for the MM76C is provided in Table C-4 and pin-out information for the MM76C Personality Module Development Circuit is provided in Table C-5.

NOTE

All unused inputs on the PMOS devices should be connected to VSS to prevent transient signals/noise.

Table C-3. PPS-4/1 MM76C ELECTRICAL SPECIFICATIONS

52-PIN IN-LINE SOCKET

Burndy P/N: DILE-52P1
Burndy Corp., 931 S. Douglas
El Segundo, Calif. 90245

OPERATING CHARACTERISTICS

VDD = -15 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL})

VSS = 0 Volts (GND)
(Logic "0" = most positive voltage V_{IH} and V_{OH})

System Operating Frequencies:
100 kHz ±40% (internal clock)

Device Power Consumption:
200 mw, typical, INT, EXT
250 mw, typical, XTAL

Input Capacitance:
<5 pf

Input Leakage:
<10 μa

Open Drain Driver Leakage (R OFF):
⩽10 μa at -30 Volts

Operating Ambient Temperature (TA):
0°C to 70°C (TA = 25°C unless otherwise specified)

Storage Temperature:
-55°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS
(with respect to VSS)

Maximum negative voltage on any pin -30 volts.
Maximum positive voltage on any pin +0.3 volt.

Input/Output	Symbol	Limits (VSS = 0) Min	Typ	Max	Limits (VSS = +5V) Min	Typ	Max	Timing (Sample/ Good)	Test Conditions
Supply Current (Average) for VDD	I_{DD}		12 ma (INT) 16 ma (XTAL)						VDD = -15.75V T = 25°C
Discrete I/O's DI/O0-DI/O9	V_{IH} V_{IL}	-1.0V		-4.2V	+4.0V		+0.8V	Ø3 & Ø4	
DI/O0-5	R_{ON}			500 ohms			500 ohms	Ø2*	3.0 ma max.
DI/O6-9	R_{ON}			400 ohms			400 ohms		
Channel 1 Input PI1-PI4	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	Ø1	
Channel 2 Input PI5-PI8	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	Ø3	
I/O Channel A RI/O1-RI/O4	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	Ø3	
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max.
I/O Channel B RI/O5-RI/O8	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	Ø3	
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max.

Table C-3. PPS-4/1 MM76C ELECTRICAL SPECIFICATIONS (continued)

Input/Output	Symbol	Limits (VSS = 0) Min	Typ	Max	Limits (VSS = +5V) Min	Typ	Max	Timing (Sample/ Good)	Test Conditions
DATAI	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	Ø4	
DATAO	RON			500 ohms			500 ohms	Ø4**	3.0 ma max.
INT0	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	Ø3	
INT1	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	Ø1	
Clock A, BP, ($\overline{B}$)	V_{OH} V_{OL}	-1.0V		-10.0V	+4.0V		-5.0V	-5.0V	CL= 50pf (max)
XPWR	V_{IH} V_{IL}	VSS		VDD	VSS		VDD		
XTLIN, XTLOUT	V_{IH} V_{IL}								Crystal 3.579 MHz
Shift Clock CLOCK	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	Ø3 & Ø4	
	RON			500 ohms			500 ohms	Ø4**	2.0 ma max.
ↄ	V_{IH} V_{IL}	-2.0V		-6.0V	+3.0V		-1.0V		Special circuit
PC1	V_{IH} V_{IL}	-1.5V		-4.2V	+4.5V		+0.8V	DC	
PC2	V_{IH} V_{IL}	-1.5V		-4.2V	+4.5V		+0.8V	DC	
CA8 LOWER CARRY OUT	RON			500 ohms			500 ohms	DC	
CA16/D UPPER CARRY SERIAL DATA OUT	RON			500 ohms			500 ohms	Ø3 & Ø4	
SYEV SERIAL EVENT INPUT	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	Ø3	
SCC/D SHIFT CLOCK CONTROL/DATA	V_{IH} V_{IL}	-1.0V		-10.0V	+4.0V		+0.8V	Ø3 & Ø4	
C/DI CONTROL/DATA INPUT	V_{IH} V_{IL}	-1.0V		-10.0V	+4.0V		+0.8V	Ø3	
ENABL	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	DC	

*State established by Ø2 (minimum impedance after Ø4).
**Same as above except Ø4 minimum at Ø2 of next cycle.

Table C-4. PPS-4/1 MM76C SIGNALS (PART NO. A79XX)

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	RI/O5	B I/O Channel Bit 1 (LSB)	28	VDD	-15 Volt Supply
2	RI/O6	B I/O Channel Bit 2	29	PC1	Lower Counter Event Input Quadrature Input
3	RI/O7	B I/O Channel Bit 3	30	PC2	Lower Counter Up/Down Quadrature Input
4	RI/O8	B I/O Channel Bit 4	31	ENABL	Enable Input
5	RI/O1	A I/O Channel Bit 1 (LSB)	32	CA8	Carry output of Lower Counter
6	RI/O2	A I/O Channel Bit 2	33	NC	Not Used
7	RI/O3	A I/O Channel Bit 3	34	NC	Not Used
8	RI/O4	A I/O Channel Bit 4	35	NC	Not Used
9	DATAI	Serial Input Signal	36	PI1	Input Channel 1, Bit 1 (LSB)
10	DATAO	Serial Output Signal	37	PI5	Input Channel 2, Bit 1
11	CLOCK	Shift Clock Input/Output	38	PI2	Input Channel 1, Bit 2
12	DI/O0	Discrete I/O Line 0	39	PI6	Input Channel 2, Bit 2
13	DI/O1	Discrete I/O Line 1	40	PI7	Input Channel 2, Bit 3
14	DI/O2	Discrete I/O Line 2	41	PI3	Input Channel 1, Bit 3
15	DI/O3	Discrete I/O Line 3	42	PI8	Input Channel 2, Bit 4 (MSB)
16	DI/O4	Discrete I/O Line 4	43	NC	Not Used
17	DI/O5	Discrete I/O Line 5	44	PI4	Input Channel 1, Bit 4
18	DI/O6	Discrete I/O Line 6	45	SYEV	Upper Counter Event Input
19	DI/O7	Discrete I/O Line 7	46	C/DI	Control/Data Input
20	DI/O8	Discrete I/O Line 8	47	SCC/D	Shift Clock for Control/Data
21	DI/O9	Discrete I/O Line 9	48	CA16/D	Carry output of Upper Counter
22	XTLIN	Crystal Input	49	TEST	Commands Test Mode
23	XPWR	Crystal Power	50	PO	Power On Reset Input
24	XTLOUT	Crystal Output	51	INT0	Interrupt 0 Input
25	BP	B Prime I/O System Clock	52	INT1	Interrupt 1 Input
26	A	A I/O Clock			
27	VSS	VSS Positive Power Supply Terminal			

NOTES: NC indicates pin not used.

Connect all unused inputs to VSS to prevent transient signals/noise. Except if serial register is used for data storage, then connect Pin 11 through 24 KΩ to VDD.

Pin 49, TEST, must be strapped to VSS for normal operation.

Table C-5. PPS-4/1 MM76C DEVELOPMENT CIRCUIT (PART NO. A7999) SIGNALS

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	VSS	VSS Positive Power Supply Terminal	34	(P1I1)	PC Bit 1, Inst. Bit 1
2	RI/O5	B I/O Channel Bit 1 (LSB)	35	(P2I2)	PC Bit 2, Inst. Bit 2
3	RI/O6	B I/O Channel Bit 2	36	(P1015)	PC Bit 10, Inst. Bit 5
4	RI/O7	B I/O Channel Bit 3	37	(P9I6)	PC Bit 9, Inst. Bit 6
5	RI/O8	B I/O Channel Bit 4	38	(P8I4)	PC Bit 8, Inst. Bit 4
6	RI/O1	A I/O Channel Bit 1 (LSB)	39	(P7I3)	PC Bit 7, Inst. Bit 3
7	RI/O2	A I/O Channel Bit 2	40	VDD	-15 Volt Supply
8	RI/O3	A I/O Channel Bit 3	41	PC1	Lower Counter Event Quadrature Input
9	RI/O4	A I/O Channel Bit 4	42	PC2	Lower Counter Up/Down Quadrature Input
10	DATAI	Serial Input Signal	43	ENABL	Enable Input
11	DATAO	Serial Output Signal	44	CA8	Carry output of Lower Counter
12	CLOCK	Shift Clock Input/Output	45	PI1	Input Channel 1, Bit 1 (LSB)
13	DI/O0	Discrete I/O Line 0	46	PI5	Input Channel 2, Bit 1
14	DI/O1	Discrete I/O Line 1	47	PI2	Input Channel 1, Bit 2
15	DI/O2	Discrete I/O Line 2	48	PI6	Input Channel 2, Bit 2
16	DI/O3	Discrete I/O Line 3	49	PI7	Input Channel 2, Bit 3
17	DI/O4	Discrete I/O Line 4	50	PI3	Input Channel 1, Bit 3
18	DI/O5	Discrete I/O Line 5	51	PI8	Input Channel 2, Bit 4 (MSB)
19	DI/O6	Discrete I/O Line 6	52	PI4	Input Channel 1, Bit 4
20	DI/O7	Discrete I/O Line 7	53	SYEV	Upper Counter Event Input
21	DI/O8	Discrete I/O Line 8	54	C/DI	Control/Data Input
22	DI/O9	Discrete I/O Line 9	55	SCC/D	Shift Clock Control/Data
23	XTLIN	Crystal Input	56	CA16/D	Carry output of Upper Counter
24	XPWR	Crystal Power	57	TEST	Commands Test Mode
25	XTLOUT	Crystal Output	58	PO	Power On Reset Input
26	BP	B Prime I/O System Clock	59	(B6P)	B Upper, Bit 6
27	A	A I/O Clock	60	(B5P)	B Upper, Bit 5
28	(P4B2)	PC Bit 4, BL Bit 2	61	INT0	Interrupt 0 Input
29	(P5B3)	PC Bit 5, BL Bit 3	62	(SKIP)	Skip Indicator
30	(P6B4)	PC Bit 6, BL Bit 4	63	INT1	Interrupt 1 Input
31	(P3B1)	PC Bit 3, BL Bit 1	64	NC	Not Used
32	(I8)	Instruction Bit 8			
33	(I7)	Instruction Bit 7			

NOTES: NC indicates pin not used.

Connect all unused inputs to VSS to prevent transient signals/noise.

Pin 57, TEST must be strapped to VSS for normal operation.

MM76C SYSTEM DEVELOPMENT AIDS

Development Circuit, Part No. A7999, is available to support MM76C Microcomputer Program Development and Prototyping. The A7999 is used with the MM76 Personality Board, the same as with the MM76 Development Circuit (P/N A7699), except that the A7999 also requires an Expansion Board. The Expansion Board provides A and BP clock inputs for synchronizing the A7999 with the rest of the Assemulator Circuitry.

Pin-out information for the A7999 Development Circuit is provided in Table C-5. Additional information on the Personality Board and the Expansion Board are available from Rockwell on special request.

APPLICATIONS

In addition to being able to be used in a wide variety of applications normally associated with one-chip microcomputers, the high speed counter in the MM76C allows this unique microcomputer to be used in many special applications.

A few of these special applications are listed below and several counter applications are provided in the following paragraphs:

- Frequency Counters
- Timers
- Synthesizers
- Digital-to-Analog Conversion
- Analog-to-Digital Conversion
- Open/Closed Loop Control Systems

Example 1. 16-Bit Counter with Quadrature Input

A typical example of using quadrature input to control the speed, position, or direction of a motor is shown in Figure C-7. The input logic to the Lower Counter will decode the two inputs of the quadrature input and determine if the count is to up or down by the phase relationship of the two inputs. Each up or down transition of both inputs will be counted. The Motor Speed/Position Controller shown in Figure C-7 shows the development and application of a typical quadrature input.

A theoretical velocity/position curve is shown in Figure C-8. The value of the counter, indicating shaft position, is compared with the corresponding error position. As each error position count is passed, a lower voltage (lower speed) is output. By controlling in this manner the shaft may be positioned rapidly and accurately.

The Control Register is automatically set to 0000 when power is applied to the MM76C. It is, therefore, not necessary to load the Control Register for this mode of operation.

To read the counter value it is necessary to execute the following sequence of instructions:

```
•
•
SEG2     Transfer Counter Data to Data Register
LBL #13  Point to initial data location (#13)
I1       Transfer LDR LS 4 bits to Accumulator
XDSK     Store in memory and point to next address
I2C      Transfer LDR 2nd MS 4 bits to Accumulator
XDSK     Store in memory and point to next address
I1       Transfer UDR 3rd MS 4 bits to Accumulator
XDSK     Store in memory and point to next address
I2C      Transfer UDR MS 4 bits to Accumulator and exit
           Counter Mode
X        Store in memory
•
•
```

This program does not disturb the counting operation; no counts are lost, and any counts accumulated while data is being transferred to memory are retained in the counter without affecting the Data Register bits which are being transferred to the Accumulator and stored.

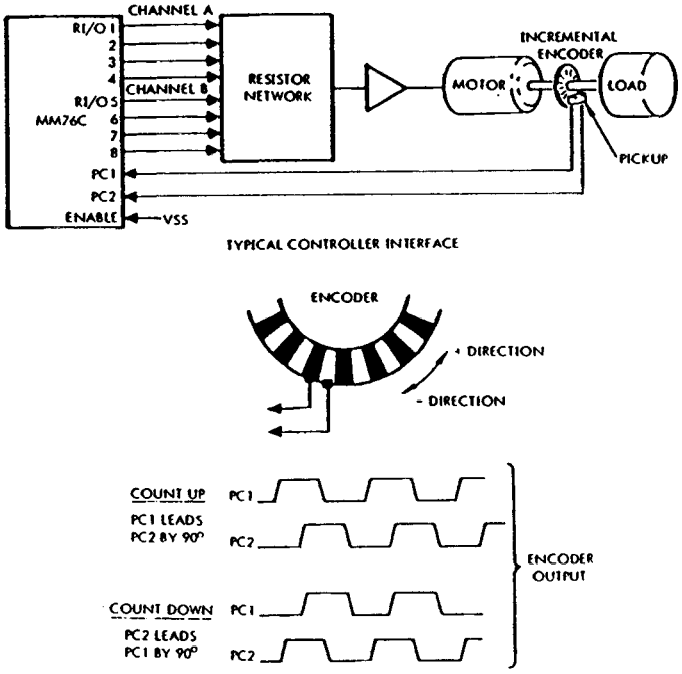


Figure C-7. MOTOR SPEED/POSITION CONTROLLER

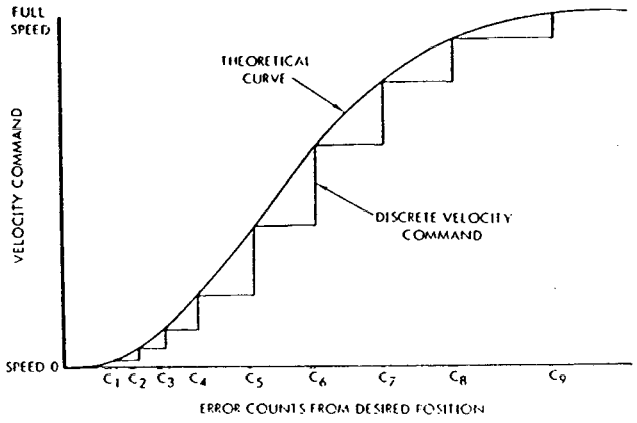


Figure C-8. DC MOTOR VELOCITY/POSITION DECELERATION PROFILE

Example 2. 16-Bit Up/Down Event Counter

is application, the Counter will count each positive-
g input at PC1 and the up/down direction of the count can be program controlled by the input at PC2. Figure C-9 shows a typical Event Counter arrangement.

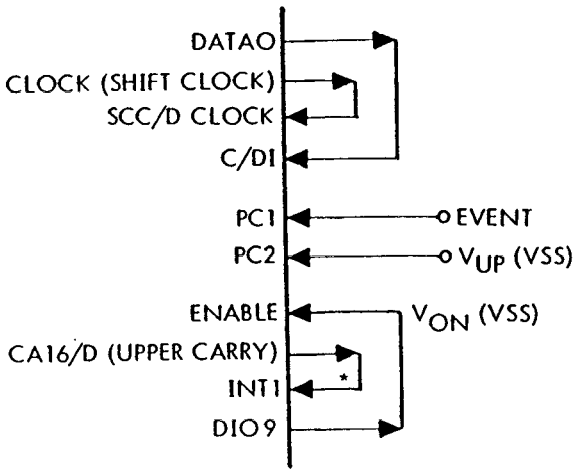
For this application the Control Register must be loaded with 0010, which sets the Input Logic to the Lower Counter so that counter will operate in the Event Count Mode. In this mode the counter will count each positive-going edge input at PC1 and will count up if the PC2 input is at VSS or count down if PC2 is at VDD (PC2 connected to DI/O9).

Loading the Control Register may be accomplished in the first sequence of instructions after power is applied to the MM76C. The input to the counter can also be disabled at this time and the counter cleared in preparation for the first counting operation. Both of these functions are accomplished with the following sequence of instructions:

```
ONE     LBL     #39     Point to Counter Enable (DI/O9)
        SEG2            Put MM76C into Counter Mode
        ROS             Disable Input
        IAM             Clear Counter
        SEG2            Put into Load Control Mode
        LAI     2       Form Control Word
        LSA             Put in S-REG
        IOS             Output to Control Register

TWO     T       *+1  }  Delay 10 Cycles
        T       *+1  }  (Any useful thing okay here)
        T       *+1  }
        T       *+1  }
        T       *+1  }
        I2C          }  Exit Counter Mode
        I2C          }
        DIN1            Initialize Interrupt 1 Flip-Flop
                        (INT1) if using Extended Event
                        Counter
        •
        •
        •
        •
THREE   LBL     #39     Point to Enable      }
        NOP             Enable Input         }  Enable Input
        SOS             Enable Input         }  Routine
        •
        •
        •
```

```
        •
        •
        •
FOUR    LBL     #39     Point to Enable*
        SEG2            Put MM76C into Counter Mode
        ROS             Disable Counter*
                        *These two instructions only
                         necessary if it is desired to
                         disable the counter after
                         reading the count value.
        LBL     #13     Point to Data Storage Location
                        (#13)
        I1              Transfer LDR LS 4-Bits to
                        Accumulator
        XDSK            Store Point to Next Location
        I2C             Transfer LDR 2nd 4 Bits
        XDSK            Store, Point to Next Location
        I1              Transfer UDR 3rd 4 Bits
        XDSK            Store, Point to Next Location
        I2C             Transfer UDR MS 4 Bits, Exit
                        Counter Mode
        X               Store MS value
        RT              Return to Call Routine
```



*This connection only necessary for the extended event counter.

NOTE: All outputs require a pull-down resistor to -V.

Figure C-9. EVENT AND EXTENDED EVENT COUNTER

Example 3. Extended Event Counter

The 16-bit counter can be extended to almost any desired bit length by the implementation of a program that uses the MM76C RAM data memory as the most significant portion of the counter. This may be implemented by inputting the carry out of the Upper Counter (CA16/D) into the interrupt input INT1 as shown in Figure C-9. Upon receiving a carry, the program increments a register in Data memory.

The following example extends the counter 8 bits (to 24 bits or 25 bits if the CPU carry is used) allowing a count of 16,777,216 (or 33,554,432 with the carry used) events.

Applications:

Event Counter
Frequency Counter
Event Counter (Period)
Bursting a Predetermined Number of Pulses
Frequency to Analog Converter
Timer
Synthesizer

ONE, TWO, and THREE of the previous example remains the same for this example:

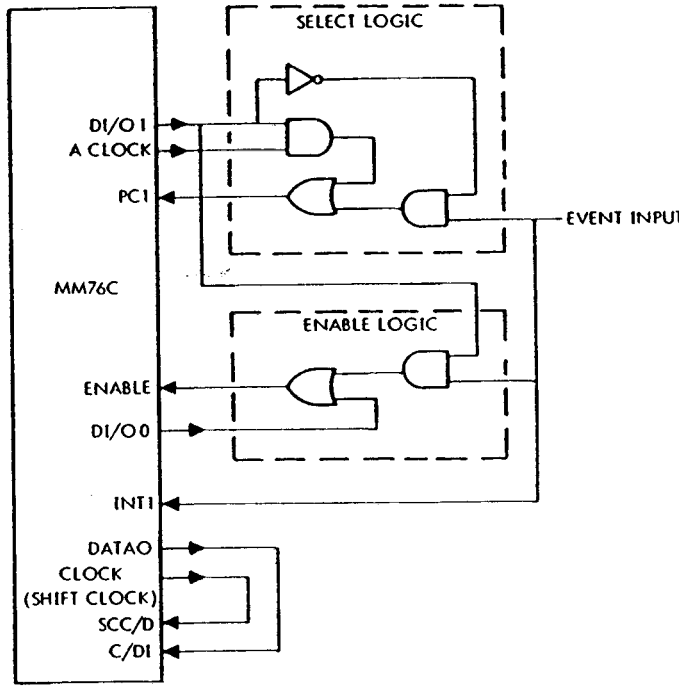
```
FOUR    DINT            Has there been a carry out?
        RT              No, Return to Call Routine
        LBL     #11     Yes, Point to Extended Counter
                        Data Memory Location
FIVE    L               Load data into Accumulator
        AISK    1       Add 1 to Extended Count
                        Register and check carry.
                        Carry present?
        T       Six     Yes, Go store new value
        X               No, Store new value
        RT              Return to Call Routine
SIX     XDSK            Store new value, point to MSD
        T       Five    Go Increment MSD
        T       Seven   Go Process Overflowed
```

Example 4. High-Low Frequency Counter

The following program example and setup, shown in Figure C-10, demonstrates a method of determining if an input to the MM76C counter is a high frequency (up to 1 MHz) or low frequency, and then counting that frequency and storing the count value in data memory for processing as needed. Although this example shows only one method of selecting a high frequency band count or a low frequency band count, both the program and external hardware could be easily expanded to allow for a precise determination of the frequency of the input, covering a wide spectrum.

Possible Applications:

Auto Ranging Frequency Counter
Feedback Control Systems



NOTE: All outputs require a pull-down resistor to -V

Figure C-10. HIGH-LOW FREQUENCY COUNTER

High-Low Frequency Counter

```
        LBL     #31
        NOP
NE      ROS             Disable Count, Put into
                        High Frequency Mode
        DECB
        T       ONE
        SEG2            Put MM76C into Counter
                        Mode
        IAM             Clear 16-Bit Counter
        SEG2            Put in Load Control Mode
        LAI     2       Form Control Word
        LSA             Put in S-Register
        IOS             Shift Control Word into
                        Control Register
        LBL     #30     Point to DI/O0
        T       *+1     Delay (2 Cycles)
        SOS             Enable Count Input (DI/O0)
        T       *+1   }
        T       *+1   } Delay (6 Cycles)
        T       *+1   }
        I2C           }
        I2C           } Exit Counter Mode
        TM      Delay   Delay for Desired Count
                        Interval
        TM      Input   Input Count Data and store
                        in Memory
        LBL     #10     Point to Data Memory
                        Address (#10)
        LAI     0       Load Accumulator with 0
        SKMEA           Count Input greater than 4096?
        T       Process Yes, Process High Frequency
                        Data
        INCB            No, Check next 4-Bit group
        SKMEA           Count Input greater than 512?
        T       Process Yes, Process High Frequency
                        Data
        T       LOWF    No, Input in Low Frequency
                        Mode
Process •               Process as required
        •
        •
        •
        •
        •
        TL Back
```

```
LOWF    SEG2            Put into Counter Mode
        IAM             Clear 16-Bit Counter
        I2C           }
        I2C           } Exit Counter Mode
        LBL     #31     Point to Data Memory (#31)
        NOP
        SOS             Select Low Frequency Counter
        DECB
        NOP
        ROS             Allow the Event to Enable and
                        Disable Mode Counter
        DIN1            Preset INT1 F/F
                        Continue with other functions
        •
        •
        •
        •
COUNTD  DIN1            Low Frequency Count Done?
        RTSK            No, Return and Skip
INPUT   LBL     #13     Yes, Point to Data Memory
                        Address (#13)
        SEG2            Put Chip into Counter Mode.
                        Transfer stable Data
        I1              Read LS 4-Bits
        XDSK            Store and Decrement Data
                        Pointer
        I2C             Read 2nd 4-Bits
        XDSK            Store and Decrement
        I1              Read 3rd 4-Bits
        XDSK            Store and Decrement
        I2C             Read MS 4-Bits
        X               Store
        RT              Return to Process Data
```

MAIN PROGRAM

```
START   TL      HILO
BCK0    •
        •
        •
        •
        TM      COUNTD  Is Low Frequency
                        Count Done?
        T       PROCESS Yes, Go Process Low
        •               Frequency Data
        •               No, Continue with
BACK    •               other functions
        •
        •
        •
        T       BCK0
PROCESS •
        •
        •
        T       START
```

Example 5. Digital-to-Analog Converter (DAC)

One way that the MM76C can be used to perform digital-to-analog conversion (DAC) is to generate a variable duty cycle square-wave output. The variable duty cycle setup provided in Figure C-11 shows how the digital value to be converted (value XY) is placed in the Upper Counter and counted down by the A clock (maximum frequency of Upper Counter is A/2), while the Lower Counter is counted up by the same A Clock. The underflow from the Upper Counter and the overflow from the Lower Counter are used to reset and set an external RS Flip-Flop to provide the variable duty cycle square-wave output.

The analog value is obtained by filtering out the DC component of the variable duty cycle square wave. The longer the duty cycle, the greater the DC value. The duty cycle is defined as KT/T as shown in the waveform in Figure C-11.

The table in Figure C-11 shows that variations of KT cause a proportional change of the DC output value. Note that in this example T is fixed at 256 units.

The following program is used to generate a KT/T duty cycle output waveform, where K equals the XY value loaded into the Upper Counter. The Upper Counter will count down and generate an underflow carry after "XY" A clocks. The carry out automatically reloads the XY value into the Upper Counter and resets the RS Flip-Flop, causing gate G1 to inhibit any further A Clock inputs to the Upper Counter. The Lower Counter will continue to count A Clocks and will carry out after 256 counts. The Lower Counter carry sets the RS Flip-Flop, which completes one full square-wave output. Setting the RS Flip-Flop starts the next cycle and both counters will start counting A Clocks. Once initialized, the MM76C counter will operate in this mode continuously without using or requiring CPU time.

Variable Duty Cycle DAC

```
SEG2          Put MM76C in Counter Mode
LAI    X      Preset for Upper Counter
              4 MSD Bits
TM     LOAD   Load MSD of Upper Counter
LAI    Y      Preset for Upper Counter
              4 LSD Bits
TM     LOAD   Load LSD of Upper Counter
SEG2          Put in Load Control Mode
LAI    #B     Form Control Word
TM     LOAD   Load Control Word (Upper Counter
              counts down and Auto presets on
              Underflow)
I2C   }       Exit Counter Mode
I2C   }
 •
 •
 •
 •
LOAD   LSA    Load Accumulator value to
              S Register
       IOS    Shift into Control Register or
              preset Upper Counter
       T  *+1 }
       T  *+1 } Delay for 6 Cycles
       T  *+1 }
       RT     Return to Call Routine
```

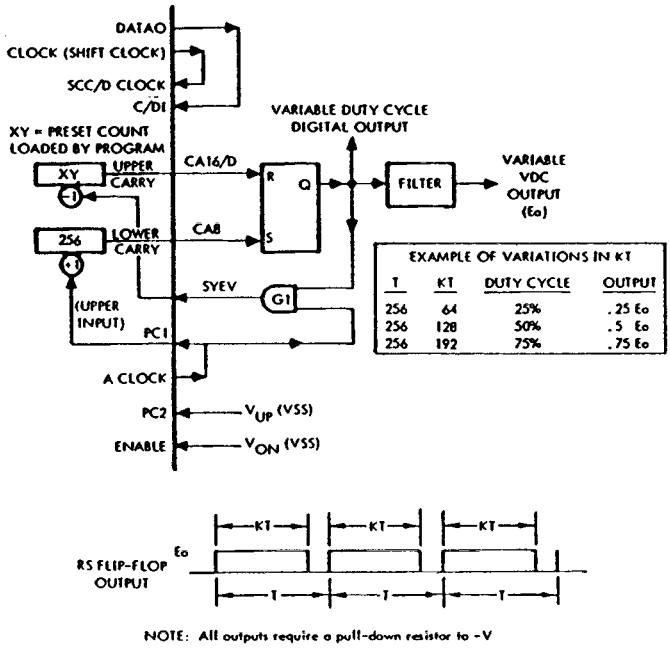


Figure C-11. VARIABLE DUTY CYCLE SETUP

APPENDIX D
MM76L AND MM76EL LOW VOLTAGE, LOW POWER VERSIONS

INTRODUCTION

The MM76L and MM76EL are functionally the same as the MM76 and MM76E respectively. The major electrical difference is that the MM76L and EL operate on any voltage between -6.5 volts and -11 volts and require only 15 milliwatts nominal power at -8.5 volts. This wide voltage range and low power requirement is compatible with standard 9-volt battery outputs making the MM76L and EL ideal for portable equipment or equipment requiring a battery back-up power supply.

The clock circuit has been modified to operate in any of four modes. Complete information on the clock is provided in a following paragraph.

Another added electrical feature is that mask programmable pull-down resistor options are available on the inputs and outputs. Refer to the Notes on the SPECIFICATION page for details. The desired coding information is provided along with the ROM coding information on the ROM Code order form.

The major physical difference is that the MM76L and EL are packaged in a standard 40-pin DIP instead of 42-pin quad package used for the MM76. This package is available with an operating range of -40°C to 85°C on special order.

SPECIAL ELECTRICAL FEATURES

- Battery Compatible (-6.5 to -11 volt operation)
- Low Power 15 milliwatts nominal @ -8.5 volts
- Four Clock Modes including external crystal
- Low Impedance Drivers
  - DI/O less than 100 ohm @ 10 ma
  - RIO less than 250 ohm @ 6 ma
- Mask Programmed Pull-ups on Outputs, (five values)
- Mask Programmed Pull-ups on Inputs

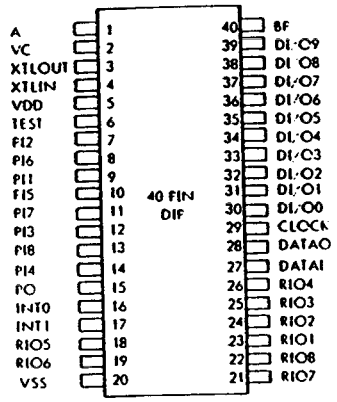


Figure D-1. MM76L AND MM76EL PIN CONFIGURATION

CLOCK CONTROL (VC, XTLIN, XTLOUT, A, AND BP)

The internal Oscillator and Clock circuit generates a four-phase A BP clock signal used for all internal logic functions. The A BP clock terms are also brought out so external logic can be synchronized. The clock for the MM76L and EL can be selected to operate in one of four modes as shown by the table below. These options are selected by control voltages applied to the VC and XTLIN pins.

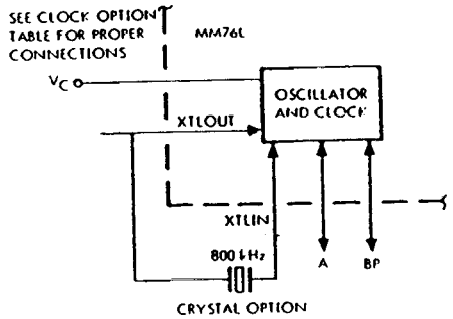


Figure D-2. MM76L AND MM76EL CLOCK CIRCUIT

Mode	Pins					Frequency
	V_C	XTLIN	XTLOUT	A I/O	BP I/O	
INTERNAL	*V_C	V_{SS}	–	OUT	OUT	100 kHz ±30% @ 8.5V
EXTERNAL	GRD	CLOCK	–	OUT	OUT	400 – 800 kHz @ 8.0V
CRYSTAL	GRD	XTAL	XTAL	OUT	OUT	400 – 800 kHz @ 8.0V
SLAVE	V_{DD}	V_{DD}	–	IN	IN	100 kHz – 50 kHz @ 8.5V

*Can be adjusted to vary frequency – Normally set to V_{DD}

SYSTEM DEVELOPMENT AIDS

All of the development aids described for the MM76 are useful in support of MM76L and EL program development. However, due to the lower operating voltage, the optional pull-down selections, and the physically different package, the MM76 development aids cannot directly simulate the MM76L electrical interfaces. The B7698 Development Circuit is made specifically for the MM76L and EL and will simulate the electrical interfaces where required.

Table D-1. MM76L AND EL ELECTRICAL SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:
VDD = -8.5 Volts -2.5, +2.0 Volts
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)

VSS = 0 Volts (GND)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies:
(1) Internal: 100 kHz Nominal at VDD = -8.5V

(2) External 800 kHz Crystal: 100 kHz

Device Power Consumption:
15 mw, typical

Input Capacitance:
<5 pf

Input Leakage:
<10 μa

Open Drain Driver Leakage (R OFF):
<10 μa at -30 Volts

Operating Ambient Temperature (T_A):
0°C to 70°C (Commercial)
-40°C to +85°C (Industrial)

Storage Temperature:
-55°C to 120°C

ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +0.3 volts.

TEST CONDITIONS: VDD = 8.5V, T = 25°C

Input/Output	Symbol	Limits (VSS = 0)			Limits (VSS = +5V)			Timing (Sample/ Good)	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Supply Current (Average) for VDD	I_{DD}		1.75 ma	3 ma		1.75 ma	3 ma		
Discrete I/O's DI/O0-DI/O9	V_{IH} V_{IL}	-1.0V		 -4.2V	+3.0V		 +0.8V	Ø3, 4	
DI/O0-9	R_{ON}			100 ohms			100 ohms	Ø2*	10.0 ma max.
Channel 1 Input PI1-PI4	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	Ø1	
Channel 2 Input PI5-PI8	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	Ø3	
I/O Channel A RIO1-RIO4	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	Ø4	
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max.
I/O Channel B RIO5-RIO8	V_{IH} V_{IL}	-1.5V		 -4.2V	+3.5V		 +0.8V	Ø4	
	R_{ON}			250 ohms			250 ohms	Ø2*	6.0 ma max.

Table D-1. MM76L AND EL ELECTRICAL SPECIFICATIONS (continued)

Input/Output	Symbol	Limits (VSS = 0)			Limits (VSS = +5V)			Timing (Sample/ Good)	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
DATAI	V_{IH} V_{IL}	-1.0V		-4.2V	+4.0V		+0.8V	ø4	
DATAO	RON			500 ohms			500 ohms	ø4**	3.0 ma max.
INT0	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	ø3	
INT1	V_{IH} V_{IL}	-1.5V		-4.2V	+3.5V		+0.8V	ø1	
Clock A, BP, ($\overline{B}$)	V_{OH} V_{OL}	-1.0V		-5.0V	+4.0V		0V		CL=50 pf (max)
XTLIN	V_{IH} V_{IL}	-1.0V		-6.0V	+3.5V		-1.0V	-4.0V	
Shift Clock Clock	V_{IH} V_{IL}	-1.0V		-4.2V	+4.0V		+0.8V	ø3, 4	
	RON			500 ohms			500 ohms	ø4**	2.0 ma max.
VC	V_{IH} V_{IL}								V=11.0V max.
PO	V_{IH} V_{IL}	-2.5V		-5.0V	+2.5V		0V		Special circuit

*State established by ø2 (minimum impedance after ø4).
**Same as above except ø4 minimum at ø2 of next cycle.

NOTES:

Mask Programmed Pull-Down Resistors on Outputs

Resistor pull-downs are available as an option on all RIO and DI/O outputs. These pull-downs are connected to VDD. The following values ± 25% are available: 3K, 5K, 10K, 15K, 25K, and Open Circuit.

Pull-Downs on Inputs

MOS FET pull-downs are also available as an option on the PI, INT, and DATAI inputs. The output cirrent is 50 μa ± 25 μa with the input grounded and VDD at -8.5 volts.

Table D-2. PPS-4/1 MM76L/MM76EL SIGNALS
(Part Nos. B76XX, B86XX)

No.	Signal Name	Function	Pin No.	Signal Name	Function
1	BP	B Prime System Clock	21	RIO7	B I/O Channel bit 3
2	VC	Resistor frequency control	22	RIO8	B I/O Channel bit 4
3	XTLIN	Crystal input	23	RIO1	A I/O Channel bit 1 (LSB)
4	XTLOUT	Crystal output	24	RIO2	A I/O Channel bit 2
5	VDD	-15 Volt Supply	25	RIO3	A I/O Channel bit 3
6	PI2	Channel 1 bit 2	26	RIO4	A I/O Channel bit 4
7	TEST	Commands Test Mode (VSS for Normal Operation)	27	DATAI	Serial Input signal
			28	DATAO	Serial Output signal
8	PI6	Channel 2 bit 2	29	CLOCK	Shift Clock Input/Output (VDD if Serial Register is Not Used)
9	PI1	Channel 1 bit 1 (LSB)			
10	PI5	Channel 2 bit 1	30	DI/O0	Discrete I/O line 0
11	PI7	Channel 2 bit 3	31	DI/O1	Discrete I/O line 1
12	PI3	Channel 1 bit 3	32	DI/O2	Discrete I/O line 2
13	PI8	Channel 2 bit 4 (MSB)	33	DI/O3	Discrete I/O line 3
14	PI4	Channel 1 bit 4	34	DI/O4	Discrete I/O line 4
15	PO	Power On reset input	35	DI/O5	Discrete I/O line 5
16	INT0	Interrupt 0 input	36	DI/O6	Discrete I/O line 6
17	INT1	Interrupt 1 input	37	DI/O7	Discrete I/O line 7
18	RIO5	B I/O Channel bit 1 (LSB)	38	DI/O8	Discrete I/O line 8
19	RIO6	B I/O Channel bit 2	39	DI/O9	Discrete I/O line 9
20	VSS	VSS Positive Power Supply (Ground)	40	A	A System Clock

Table D-3. PPS-4/1 MM76L/MM76EL DEVELOPMENT CIRCUIT SIGNALS
(Part No. B7699)

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	VSS	Same as B76XX	33	(I8)	Instruction bit 8
2	RIO5	Same as B76XX	34	(I7)	Instruction bit 7
3	RIO6	Same as B76XX	35	XTLIN	Same as B76XX
4	RIO7	Same as B76XX	36	XTLOUT	Same as B76XX
5	RIO8	Same as B76XX	37	VC	Same as B76XX
6	RIO1	Same as B76XX	38	VDD	Same as B76XX
7	RIO2	Same as B76XX	39	Not Used	—
8	RIO3	Same as B76XX	40	(P6B4)	PC bit 6, BL bit 4
9	Not Used	—	41	(P3B1)	PC bit 3, BL bit 1
10	Not Used	—	42	(P1I1)	PC bit 1, inst bit 1
11	Not Used	—	43	P2I2)	PC bit 2, Inst bit 2
12	RIO4	Same as B76XX	44	(P10I5)	PC bit 10, Inst bit 5
13	DATAI	Same as B76XX	45	(P9I6)	PC bit 9, Inst bit 6
14	DATAO	Same as B76XX	46	(P8I4)	PC bit 8, Inst bit 4
15	CLOCK	Same as B76XX	47	(P7I3)	PC bit 7, Inst bit 3
16	DI/O0	Same as B76XX	48	TEST	Same as B76XX
17	DI/O1	Same as B76XX	49	PI2	Same as B76XX
18	DI/O2	Same as B76XX	50	PI6	Same as B76XX
19	DI/O3	Same as B76XX	51	PI1	Same as B76XX
20	DI/O4	Same as B76XX	52	PI5	Same as B76XX
21	DI/O5	Same as B76XX	53	PI7	Same as B76XX
22	DI/O6	Same as B76XX	54	PI3	Same as B76XX
23	DI/O7	Same as B76XX	55	PI8	Same as B76XX
24	Not Used	—	56	PI4	Same as B76XX
25	DI/O8	Same as B76XX	57	VDD	Same as B76XX
26	DI/O9	Same as B76XX	58	PO	Same as B76XX
27	Not Used	—	59	INT0	Same as B76XX
28	(P4B2)	PC bit 4, BL bit 2	60	(B6)	Buffer bit 6
29	(P5B3)	PC bit 5, BL bit 3	61	(B5)	Buffer bit 5
30	Not Used	—	62	(SKIP)	Skip Indicator
31	BP	Same as B76XX	63	INT1	Same as B76XX
32	A	Same as B76XX	64	Not Used	—

Program Control (P) outputs during phase 2 are in complement form. (0 = -V, 1 = VSS)
B outputs during phase 4. BL is in complement form, BU is in true form.
Instruction (I) inputs at end of phase 4 are in true form.
Skip output is -V during Ø4 if an instruction is to be skipped.

Table D-4. PPS-4/1 MM76L/MM76EL DEVELOPMENT CIRCUIT SIGNALS
(Part No. B7698)

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	DI/O1	Same as B76XX	27	(P7I3)	PC bit 7, Inst bit 3
2	DI/O2	Same as B76XX	28	PI2	Same as B76XX
3	DI/O3	Same as B76XX	29	PI6	Same as B76XX
4	DI/O4	Same as B76XX	30	PI1	Same as B76XX
5	DI/O5	Same as B76XX	31	PI5	Same as B76XX
6	DI/O6	Same as B76XX	32	PI7	Same as B76XX
7	DI/O7	Same as B76XX	33	PI3	Same as B76XX
8	DI/O8	Same as B76XX	34	PI8	Same as B76XX
9	DI/O9	Same as B76XX	35	PI4	Same as B76XX
10	(P4B2)	PC bit 4, BL bit 2	36	VDD	Same as B76XX
11	(P5B3)	PC bit 5, BL bit 3	37	PO	Same as B76XX
12	BP	Same as B76XX	38	INT0	Same as B76XX
13	A	Same as B76XX	39	INT1	Same as B76XX
14	(I8)	Inst. bit 8	40	RIO5	Same as B76XX
15	(I7)	Inst. bit 7	41	RIO6	Same as B76XX
16	XTLIN	Same as B76XX	42	RIO7	Same as B76XX
17	XTLOUT	Same as B76XX	43	RIO8	Same as B76XX
18	VC	Same as B76XX	44	RIO1	Same as B76XX
19	VDD	Same as B76XX	45	RIO2	Same as B76XX
20	(P6B4)	PC bit 6, BL bit 4	46	RIO3	Same as B76XX
21	(P3B1)	PC bit 3, BL bit 1	47	RIO4	Same as B76XX
22	(P1I1)	PC bit 1, Inst bit 1	48	VSS	Same as B76XX
23	(P2I2)	PC bit 2, Inst bit 2	49	DATAI	Same as B76XX
24	(P10I5)	PC bit 10, Inst bit 5	50	DATAO	Same as B76XX
25	(P9I6)	PC bit 9, Inst bit 6	51	CLOCK	Same as B76XX
26	(P8I4)	PC bit 8, Inst bit 4	52	DI/O0	Same as B76XX

Program Control (P) outputs during phase 2 are in complement form. (0 = -V, 1 = VSS)
BL outputs during phase 4 are in complement form.
Instruction (I) inputs at end of phase 4 are in true form.