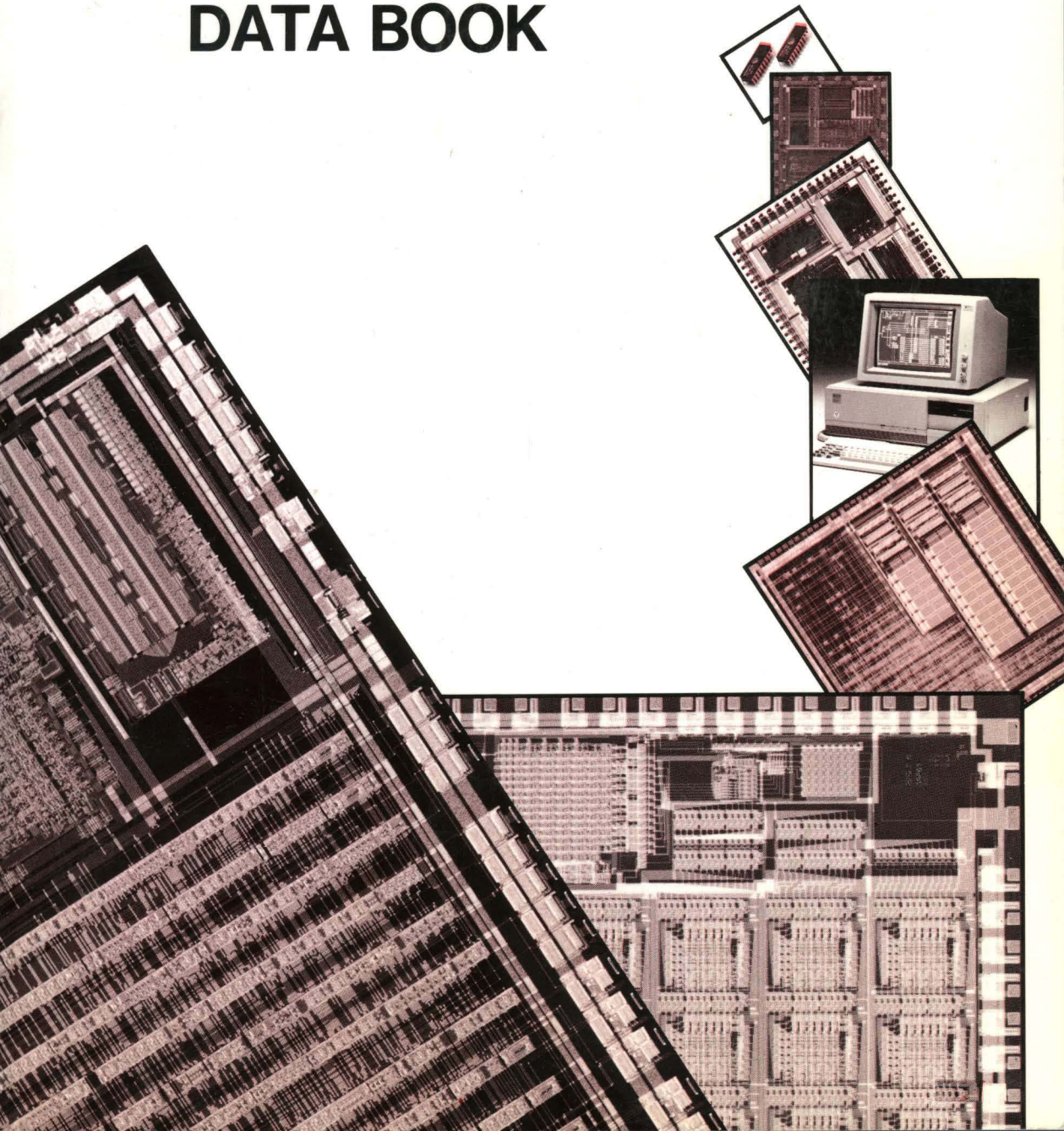
RICOH

ELECTRONIC DEVICES DATA BOOK



ELECTRONIC DEVICES
DATA BOOK

RICOH

RICOH COMPANY, LTD.
ELECTRONIC DEVICES DIVISION

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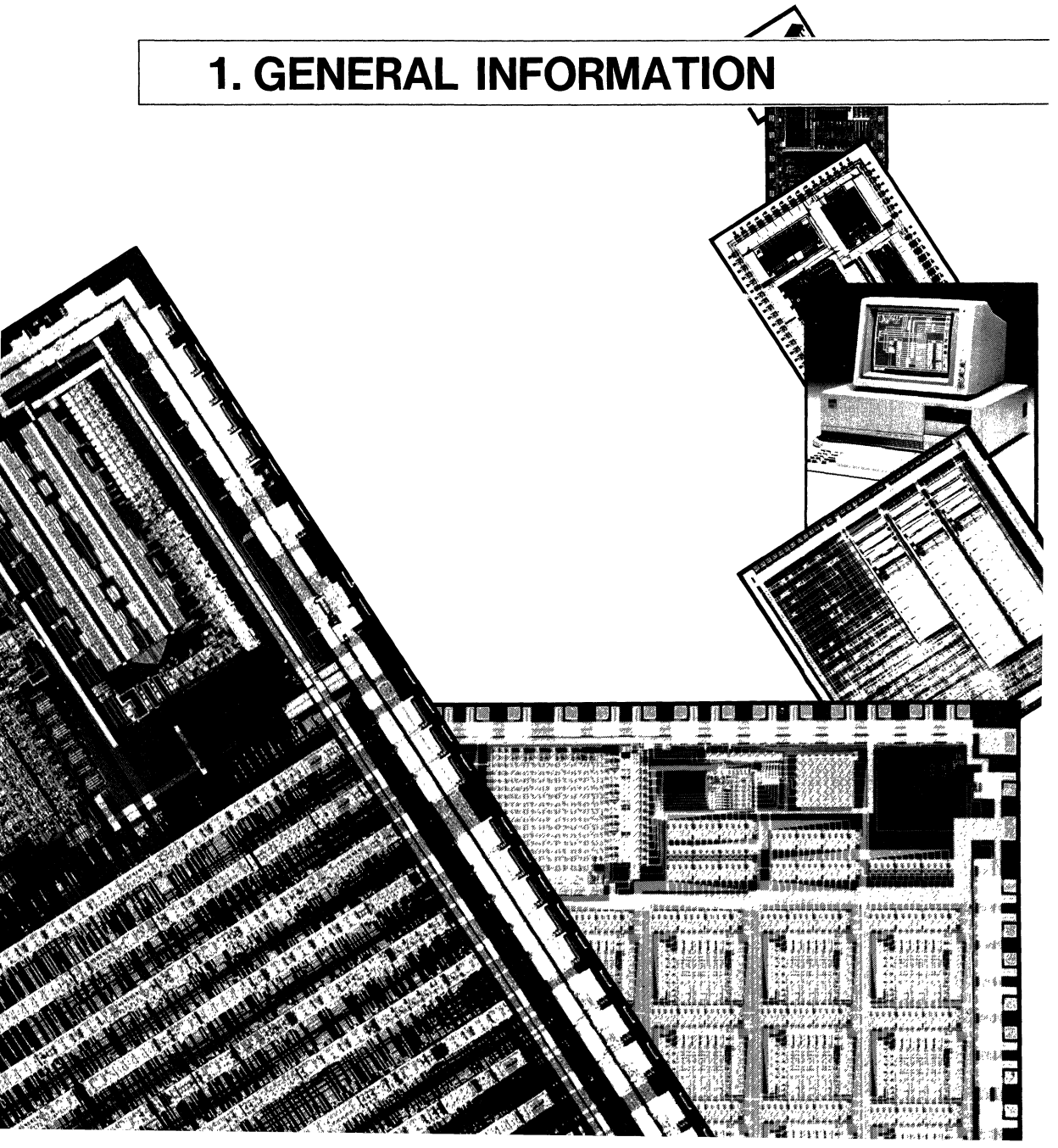
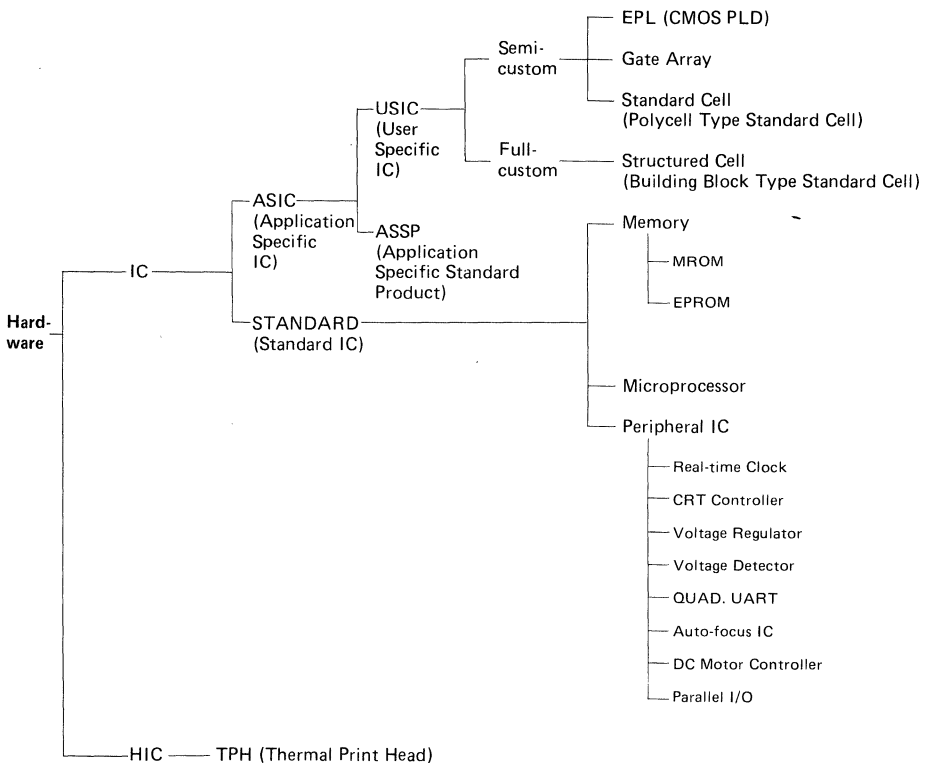
1. GENERAL INFORMATION



■ Synoptical table describing IC among our products.

System of RICOH's products



Soft-ware — CAD System

Hardware	Personal Computer	RICOH supports the CAD system, an extensive VLSI Design package that operates on IBM personal computers or EWS (Engineering Work Stations).
Cell Library	Engineering Work Station	
Development software	EPL Programer	

Service-ware

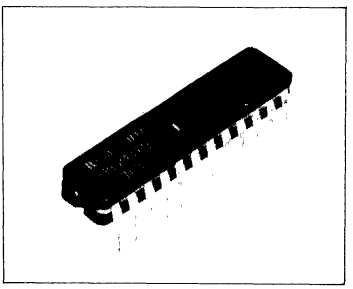
Proposal Service	RICOH will always provide proposals for the design and development of any ASIC device, EPL to gate array conversion, Gate Array, or Standard Cell.
Design Center Service	RICOH offers a turn-key design environment, CAD system seminars and consulting service. RICOH engineers will train customers to develop and design I.C.'s.
Maintenance Service	RICOH will service or repair CAD systems purchased from RICOH and Maintain all software.

EPL

Features

This is the ASIC which allows the user to program optional logic circuits with many standard PAL programmers. This is optimum replacement for small-scale logic and CPU peripheral devices. EPL's provide a quick evaluation and correction of logic circuits.

- Upward compatible to AMD/MMI PALS.
- CMOS EPROM process
  - Low current consumption and high programmability.
  - Erasable by ultraviolet light (ceramic window package).
- Maximum access time 25/35ns
- 20pin, 24pin types
- Up to 900 gate equivalents
- Security fuse
- Output polarities are programmable.



Lineup

	Model name	Configuration	Power supply	Electrical characteristics				Package	Compatible products
				Max. Icc		Max. access time	Max. operating freq.		
				Operation	Standby				
GI	EPL10P8 B	10 input 8 output AND-OR/XOR Array	5V±5%	50mA*	40mA*	35ns	20MHz	20DIP (plastic, ceramic with window)	PAL10L8, 10H8
	EPL12P6 B	12 input 6 output AND-OR/XOR Array							PAL12L6, 12H6
	EPL14P4 B	14 input 4 output AND-OR/XOR Array							PAL14L4, 14H4
	EPL16P2 B	16 input 2 output AND-OR/XOR Array							PAL16L2, 16H2
GII	EPL16P8 B	10 input 6 input/output AND-OR/XOR Array		70mA	60mA				PAL16L8
	EPL16RP8 B	8 input 8 feedback 8 output 8 register AND-OR/XOR Array							PAL16R8
	EPL16RP6 B	8 input 6 feedback 2 input/ output 6 output 6 register AND-OR/XOR Array							PAL16R6
	EPL16RP4 B	8 input 4 feedback 4 input/ output 4 output 4 register AND-OR/XOR Array							PAL16R4
	EPL241ED/ EP/EJ	6 input 16 input/output 16 microcell built-in clock select asychronous reset attached/6 register		140mA**	120mA**	25ns	20MHz	24DIP 28PLCC	22V10 & others

GI : Group I GII : Group II

* Since Group I has twice as many product terms as PAL products, typical currents will be reduced to a half of the above specification values by power-down circuits in RICOH's EPL.

** It will proportional to the product term usage. (40 mA at 35% utilization)

Note) A high speed version of 20pin EPL's with access time of 15ns is under development.

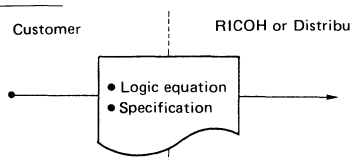
Support Tool

Software
- ◉EPLASM (RICOH)
- ◉ABEL (Data I/O)

Hardware
- ◉Universal Programmer UNISITE40, 29B (Data I/O)
- ◉Model 60A (Data I/O)
- ◉Model PW98-20 (RICOH) (Board Writer)
- Packer 30 (AVAL)
- PROMAC Model 11 (Japan Macnics)

Hardware
- SW16 (Ricoh) (RICOH)
- IBM-PC AT (IBM)
- PC9801 (NEC)

Interface

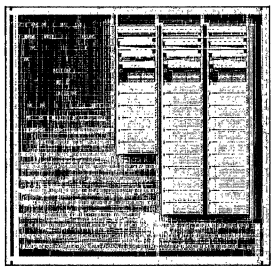


- If the customer has the programer, it can be programed by the customer.

◉mark: Products handled by RICOH's sales

GATE ARRAY

Features



This is the ASIC which performs wiring operation in matching with user's specification upon preparing the master arranged with the fixed number of gates beforehand by the manufacturer. For this reason, large-scale circuit can be developed at a moderate cost and in short period of time.
Three series of Gate Arrays are available:
- 5GH CMOS (1.5ns/gate propagation delay)
- 5GF CMOS (1.0ns/gate propagation delay)
- 3G Analog/Digital Bi-CMOS

RICOH's cell libraries can be designed on Daisy, Mentor and P.C. CAD stations (FutureNet)

5GH Series (CMOS Gate Array, 2.0μ Design Rule)

Model name	No. of gate	No. of I/O	Gate delay time	Power supply	Input output level	Package (No. of PINs)			
						DIP	Shrink DIP	FLAT	PLCC
5GH05	560	40	1.5ns/gate Load condition 2 input NAND, FAN OUT = 3, wire length = 3 mm	5V±10%	CMOS/TTL compatible	14, 16, 18, 20, 22, 24, 28, 40	42	–	–
5GH10	1000	60				24, 28, 40, 48	28	60, 44	44
5GH16	1600	72				24, 28, 40, 48	28	60, 80, 44	44
5GH23	2300	88				28, 40, 48	64	60, 80, 100	28, 68, 84
5GH29	2900	98				28, 40, 48	64	80, 100	68, 84
5GH38	3800	108				28, 40, 48	64	60, 80, 100	68, 84
5GH55	5500	120				–	–	–	–

Note) For the packages other than above, please inquire to RICOH.

5GF Series (CMOS Gate Array, 1.5μ Design Rule)

Model name	No. of gate	Max. loading memory capacity RAM (ROM) (bit)	No. of I/O	Gate delay time	Power supply	Input output level	Package (No. of PINs)			
							DIP	Shrink DIP	FLAT	PLCC
5GF21	2100	2 K (4 K)	84	1.0ns/gate Load condition 2 input NAND FAN OUT = 3 wire length = 3 mm	5V±10%	CMOS/TTL compatible	40	64	44,60,64,80,100	68
5GF26	2600	2 K (4 K)	94				40	64	44,60,64,80,100	68
5GF32	3200	2 K (4 K)	102				40	64	44,60,64,80,100	68
5GF45	4500	4 K (8 K)	120				40	64	60,64,80,100	68
5GF58	5800	8 K (16 K)	138				40	64	64,80,100	68
5GF82	8200	16 K (32 K)	168				40	64	80,100	68

Note) In case of memory integrated, the total number of usable gate will decrease compared to the above-mentioned numbers. For the number of usable gate when memory is integrated, and Test PINs to check memory or logic, please consult your RICOH design center.

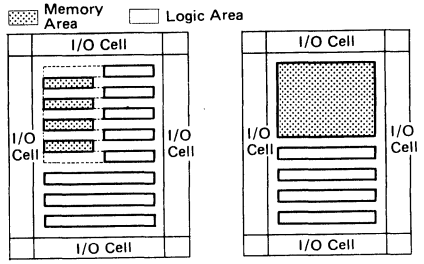
3G Series (Bi-CMOS/CMOS Gate Array)

Model name	No. of gate	No. of I/O	Gate delay time	Power supply	Analog circuit scale	Package (No. of PINs)			
						DIP	FLAT	PLCC	PIP
3G01	250	37 (with NPNTr)	6ns/gate	5V±5% (CMOS) ~ 15V (bipolar)	8 op-AMP eq.	28,40,64	44,54,60	–	–
3G02	400+ decorder	16 (with NPNTr) 14 (with PNPTr)	4ns/gate		12 op-AMP eq.	24,28,40,64	44,54,60	–	–

Note) Since input and output sections contain bipolar NPN transistors, it will allow the direct drive of externally mounting elements such as LED, fluorescent indication tube, mini-motor, etc.

Features of 5GF Series

5GF Series Gate Arrays allow memory (ROM, RAM) in conjunction with Logic requirements.
RICOH's unique system of constituting the memory using wired area, as shown on the right diagram. Since it does not require the master for memory, the cost for development can be kept down in case of memory integrated.



5GF Series　　Example of other systems

Development Tool (for CAD Interface)

Hardware

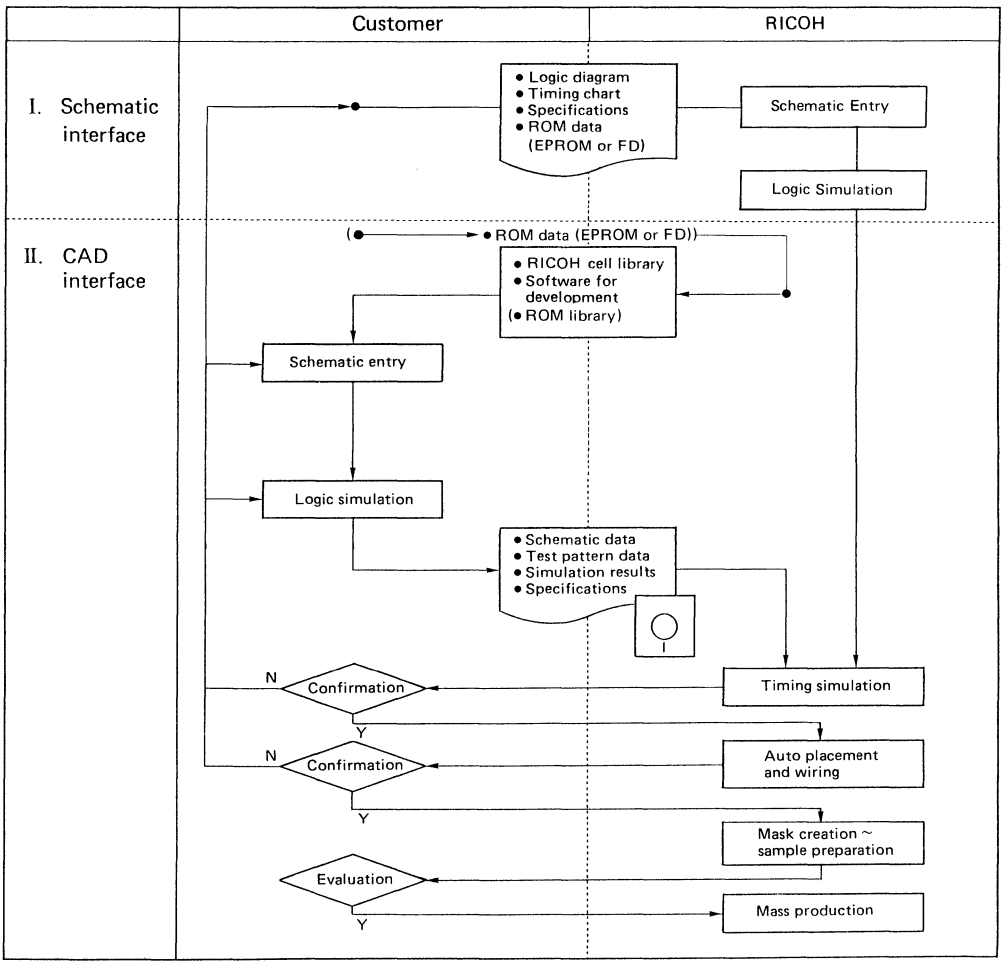
- EWS　LOGICIAN (Daisy)
  IDEA1000 (Mentor)
- Personal computer　IBM-PC AT (IBM)
  ◉SW16 (RICOH)

Software

◉RICOH cell library and simulation data
◉RICOH's development software
◉DASH, CADAT (Data I/O Co. provided that development only on personal computer)

◉Mark: Products handled by RICOH sales

Interface



STANDARD CELL·STRUCTURED CELL

Features

This kind of ASIC allows maximum flexibility without full custom expense. Development time and fabrication costs are more than gate arrays but allow integration of analog cells, CPU peripherals, memory cells (ROM and SRAM), and D.S.P. functions (multipliers, Micro-program Sequencer, dual port SRAM).
RICOH's standard cell design rules are 2 micron or 1.5 micron which allow *2.0ns per gate delays or 1.0ns per gate delays.
When Bi-CMOS is integrated on the 2 micron design rules, I.C.'s provide high current options, high voltage options and other common analog functions not possible with standard digital processes.
The Structured Cell system is comprised of three types of Cells.

1. Basic logic and registers
2. Compiled Cells synthesizing the basic Cells (Inc. ROM and SRAM Blocks)
3. Mega cells that perform complex functions

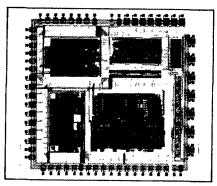
〈 Cell Library 〉

- 2.0μ design rule
  - Macro cell, Macrofunction cell (Basic cell) ..... 103 cells
  - Mega cell (Large cell)
    Logic cell for CPU peripheral ..... 6 cells
  - Compiled cell (Large cell)
    MROM, SRAM
  - Analog cell ..... 5 cells
  - Bipolar analog cell ..... 180 cells
- 1.5μ design rule
  - Macro cell, Macrofunction cell (Basic cell) ..... 411 cells
  - Mega cell (Large cell)
    Logic cell for CPU peripheral ..... 5 cells
  - Compiled cell (Large cell)
    DSP cell ..... 9 cells
    MROM, SRAM, PLA
  - Analog cell ..... 2 cells

Example of Development

Bi-CMOS Standard Cell

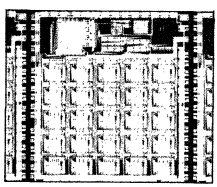
The 2 micron design rule Standard Cells can be further enhanced by combining high voltage and high current capability. All cells common to the 2 micron library are compatible with the Bi-CMOS process. Analog cells can be implemented in this process. The analog cells integrate popular functions such as operational amplifiers, comparators, voltage references, and specialized buffer cells.



Example of development
(IC for controller)

ASIC DSP (Digital Signal Processor)

RICOH has the cell library for DSP available as mega-cell and is, therefore, prepared to develop DSP as ASIC. (Cell for DSP can be automatically prepared in line with user's specification, using CAD.) Accordingly, it will materialize the function most suited for user's specification without any excess and lack and thus, will materialize high performance 1 chip DSP that can not be materialized with general-purpose DSP.



Example of development
(IC for image processing)

CMOS Standard Cell · Structured Cell (1.5μ Design Rule)

Process		CMOS
Gate delay		1.0ns /gate (load condition: 2 input NAND, FAN OUT = 3, wire length = 3mm)
Power supply voltage		5V (5V±10%)
Package		Same as 2.0μ design rule
Cell library	Basic cell	Micro-cell-----180 cells Micro-function cell-----231 cells
	Large-scale cell	〈 Mega-cell 〉 • CPU peripheral cells TCC (Timer/Counter) ACI (Asynchronous communication interface) PIO (Parallel input/output) HS (Hand shake) INTC (Interrupt controller) 〈 Compiled cell 〉 • Cell for DSP Multiplexer Multiplier Multiplier/Accumulator ALU Pipeline register Addition subtraction cell Barrel shifter Register file Microprogram sequencer • MROM, SRAM, PLA
	Analog cell	A/D converter (8bit) D/A converter (8bit)

CMOS, Bi-CMOS Standard Cell (2.0μ Design Rule)

Process		CMOS	Bi-CMOS (si gate)
Gate delay		2.0ns/gate (CMOS logic section) (Load condition: 2 input NAND, FAN OUT = 3, wire length = 3mm)	
Power supply voltage		5V (5V±10%)	5V ± 10%, ±5V (Bipolar section)
Package	DIP	14, 16, 18, 20, 22, 24, 28, 40, 42, 48	
	Shrink DIP	28, 42, 64	
	FLAT	44, 60, 64, 80, 100, 128, 144, 160	
	PLCC	18, 20, 28, 44, 68, 84	
	SOP	20, 24, 28	
	PGA	68, 84, 100, 120, 132, 144, 160, 180	
Cell library	Basic cell	Macro-cell-----71 cells Macro-function cell-----32 cells	
	Compiled cell	• MROM, SRAM	
	Large-scale cell	〈 Mega-cell 〉 • CPU peripheral cells RTC (Real-time clock) SCI (Communication interface) TCC (Timer/Counter) Timer (8bit)* Multiplier (8 x 8)* CRT controller* 〈 Compiled cell 〉 • MROM, SRAM * under development	
	Analog cell (Bipolar)		• Operational amplifier-----5 cells • Comparator-----4 cells • I/O cell-----3 cells • VRFE, Analog switch, Transistor, Resistor, Capacitor-----Many kinds for each
	Analog cell (CMOS)	A/D converter (8bit) Flash type A/D converter* D/A converter (8bit) Operational amplifier SCF (Switched capacitor filter)* * under development	

Development Tool (for CAD interface)

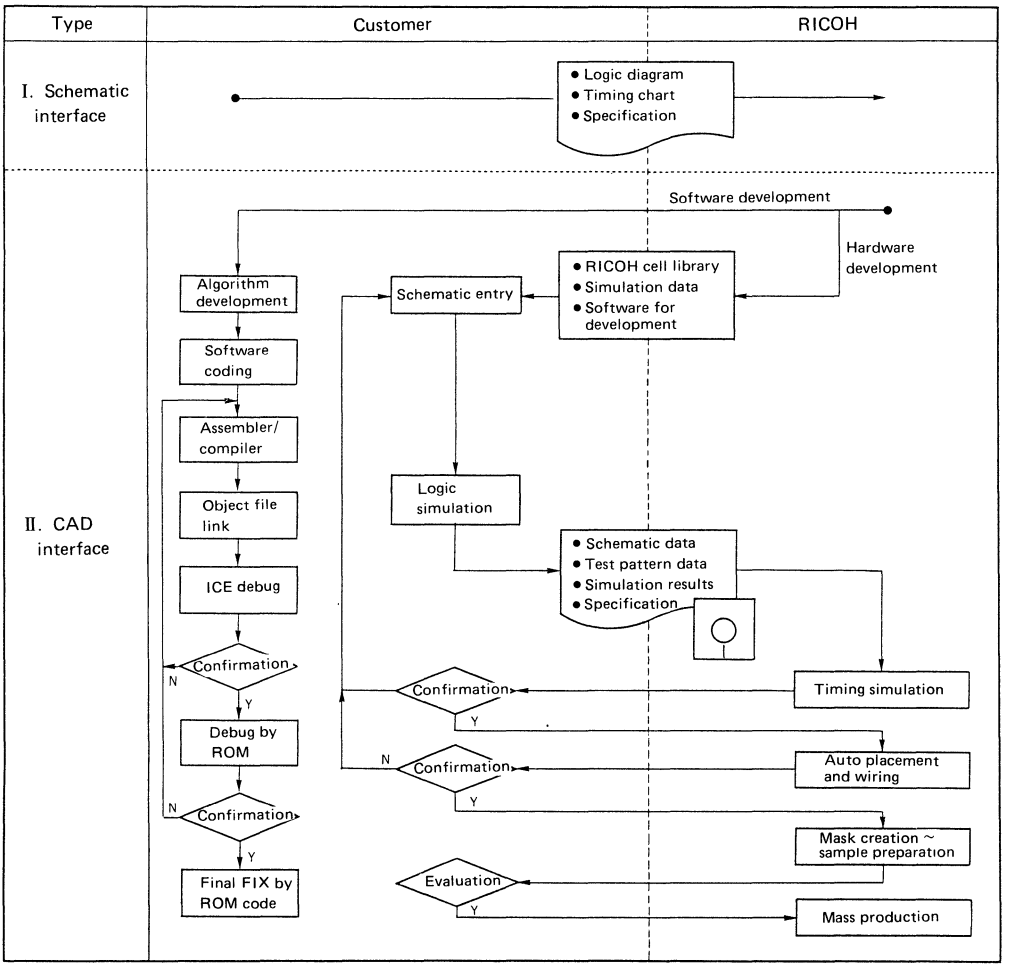
CAD interface supports the following systems.

- 2.0μ design rule
  CMOS Standard cell with basic cell
- 1.5μ design rule
  CMOS Standard cell with basic cell

The systems in which other cells are used will be schematic interface.

Hardware development tools required in the case of CAD interface are same as gate arrays.

Interface



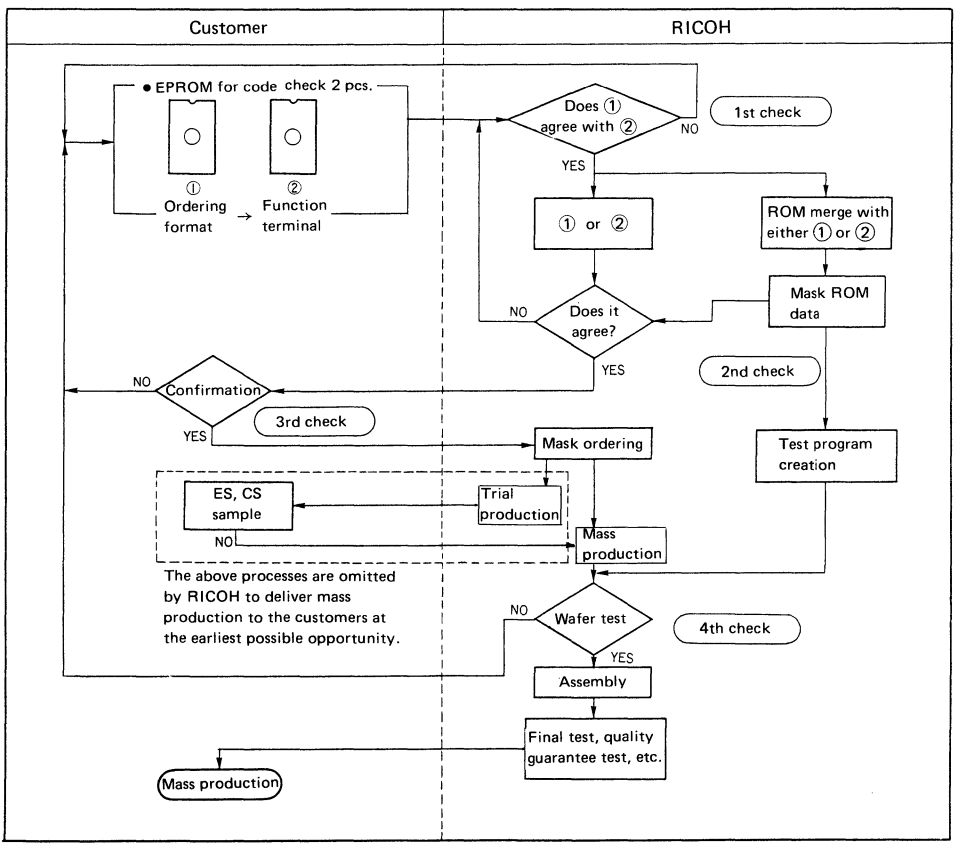
Note) The CAD interface system provides software development for any practical circuit.

MASK ROM

Lineup

Model name	Type	Memory capacity	Configu-ration	Access time (ns)	Power supply voltage	Max. power consumption (mW)		No. of pin	Pin compatible
						Operation	Standby		
RP2D32	NMOS	32K	4096x8	250	5V±10%	440	–	24	TI
RP2D33				250		440	–	24	INTEL
RP2364E		64K	8192x8	200		550	110	28	INTEL
RP2D129		128K	16384x8	250		550	110	28	INTEL
RP2D130				250		550	110	28	TI
RP23128E		128K	16384x8	200		550	110	28	INTEL
RP23256D/E		256K	32768x8	250/200		550	110	28	INTEL
RP23257D/E				250/200		550	110	28	TI
RP231026D/E		1M	131072x8	250/200		550	165	28	INTEL
RP23C4000	CMOS	4M	524288x8 262144x16	200		220	0.55	40	

Interface



EPROM

Model name	Type	Memory capacity	Configu-ration	Access time (μs)	Power supply voltage	Max. power consumption (mW)		No. of pin	Pin compatible
						Operation	Standby		
RP/RF5H01	CMOS	64 bits	64x1	1	5V±5%	55	0.55	8	–

MICROPROCESSOR

Model name	Circuit function	Power supply voltage	Max. power consumption	Motion frequency	Cycle time	Package
RP65C02	8bit CMOS CPU (Rockwell Compatible)	5V±5%	20mW/MHz	1 ~ 4MHz	1μs ~ 250ns	40-DIP
RP65C02A	8bit CMOS CPU (NCR Compatible)		20mW/MHz			40-DIP

REAL-TIME CLOCK

Model name	Circuit function	Power supply voltage	Max. current consumption		Backup power voltage	Package
			Operation	During backup		
RP/RF/RJ5C15	REAL TIME CLOCK	5V±10%	250μA	15μA	2.0V	18DIP/18SOP/28PLCC
RP5C01	REAL TIME CLOCK with RAM		250μA	15μA	2.2V	18-DIP
RP/RF5C62	REAL TIME CLOCK	5V±10%	50μA	3μA	2.0V	18DIP/18SOP

CRT CONTROLLER

Model name	Circuit function	Power supply voltage	Power supply current	Package
RF5C16A/RP5C16	CRT DISPLAY CONTROLLER (All in One Type) 640x200 or 80x25 (chalacter x line)	5V±10%	50mA	64-FLAT 64-DIP

* The 5C16 can display graphics in 16 colors and multiple screens by commands from popular CPU's (65C02, 8085, Z80). This VLSI CRT Controller only needs one or two DRAMS and CPU to function.

VOLTAGE REGULATOR

Model name	Circuit function	Output voltage accuracy	Operation voltage range	Power consumption	Package
RX5RA	IC for power (output can be set at 0.1V step)	±2.5%	1.5 ~ 10V	1μA	Mini-power mold/TO-92

VOLTAGE DETECTOR

Model name	Circuit function	Voltage detection accuracy	Operation voltage range	Current consumption	Package
RX5VA	IC for voltage detection (detection voltage can be set at 0.1V step)	±2.5%	1.5 ~ 10V	1μA	Mini-power mold/TO-92

QUAD. UART

Model name	Circuit function	Power supply voltage	Max. power current	Package
RF5C59	Asynchronous receiver transmitter with 4 channel ports.	5V	20mA	60-FLAT

AUTOFOCUS IC

Model name	Circuit function	Power supply voltage	Max. power current	Light emitting interval	Max. measuring path time (After Vcc ON)	Package
RF3L06	AUTO FOCUS IC FOR 35mm LENS SHUTTER CAMERA & VTR CAMERA	3V±10%	4.5mA	0.5s	32ms	44-FLAT
RF3L11						

* RF3L06 and RF3L11 are the IC for autofocus of projection and light reception system under which near infrared LED and linear line senser are combined together.

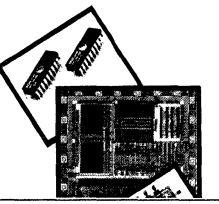
DC MOTOR CONTROLLER

Model name	Circuit function	Power supply voltage	Max. power current	Package
RF3P01	DC SERVO MOTOR CONTROLLER (Can be connected direct to PWM output, 8bit CPU)	5V±5%	30mA	60-FLAT

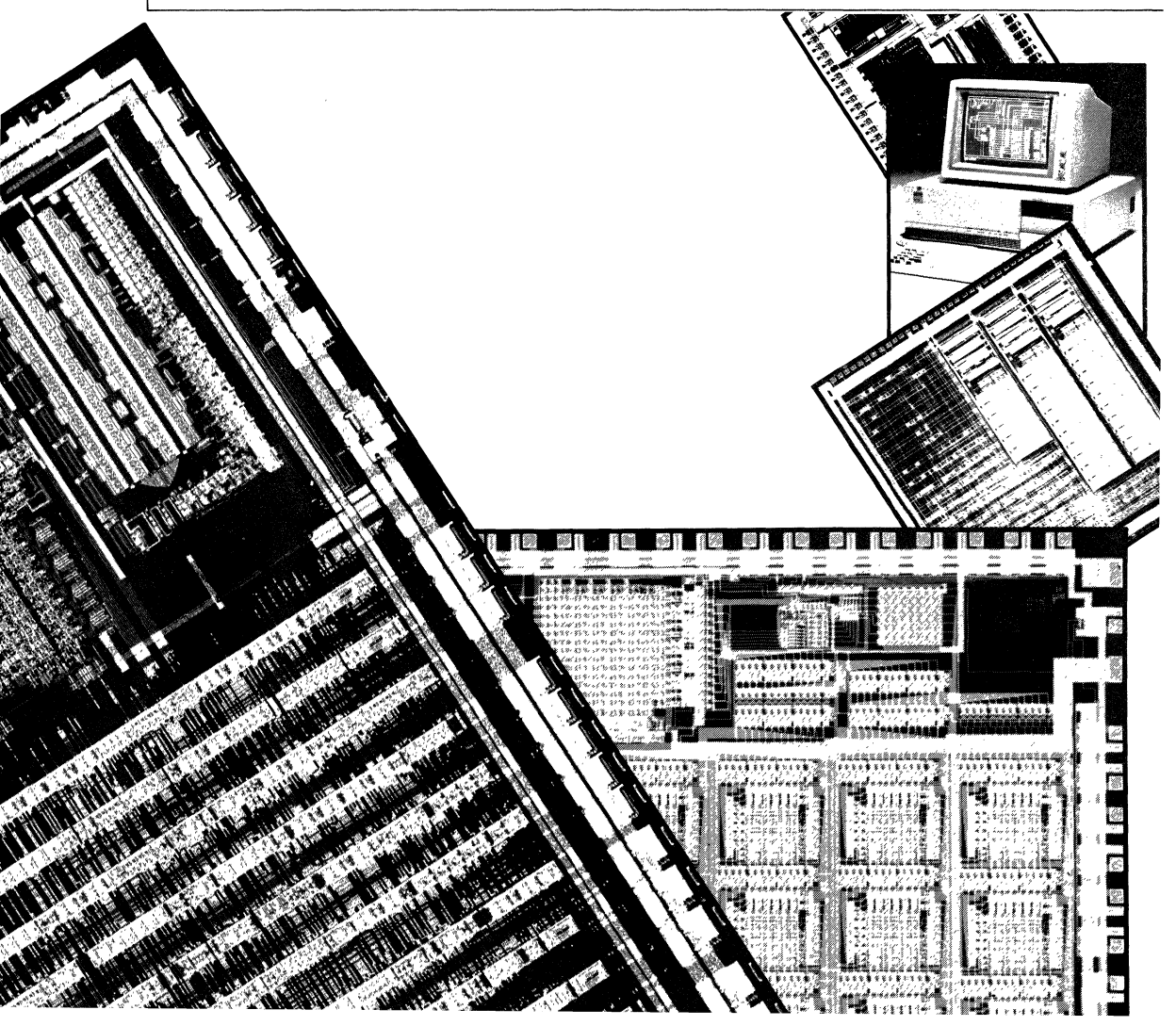
* RF3P01 can control the speed of DC motor in extensive ranges and at high accuracy by connecting it with 8bit CPU.

PARALLEL I/O

Model name	Circuit function	Power supply voltage	Max. power current	Package
RF5C60	6 I/O Port (8bit I/O Port x 5, 5bit I/O Port x 1)	5V±10%	30mA	60-FLAT

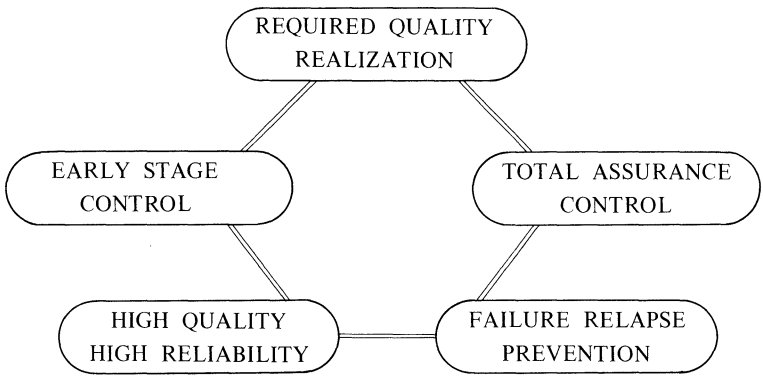


2. QUALITY ASSURANCE SYSTEM



THE POLICY OF QUALITY ASSURANCE

RICOH, Electronic Devices Division, keeps in mind to develop devices and assure the quality putting ourselves in customers' place. RICOH pursuits following 5 points night and day to offer the best quality timely with the optimum cost to the customers.



1. Accomplish the quality aim satisfying the use condition and requirements of customers.

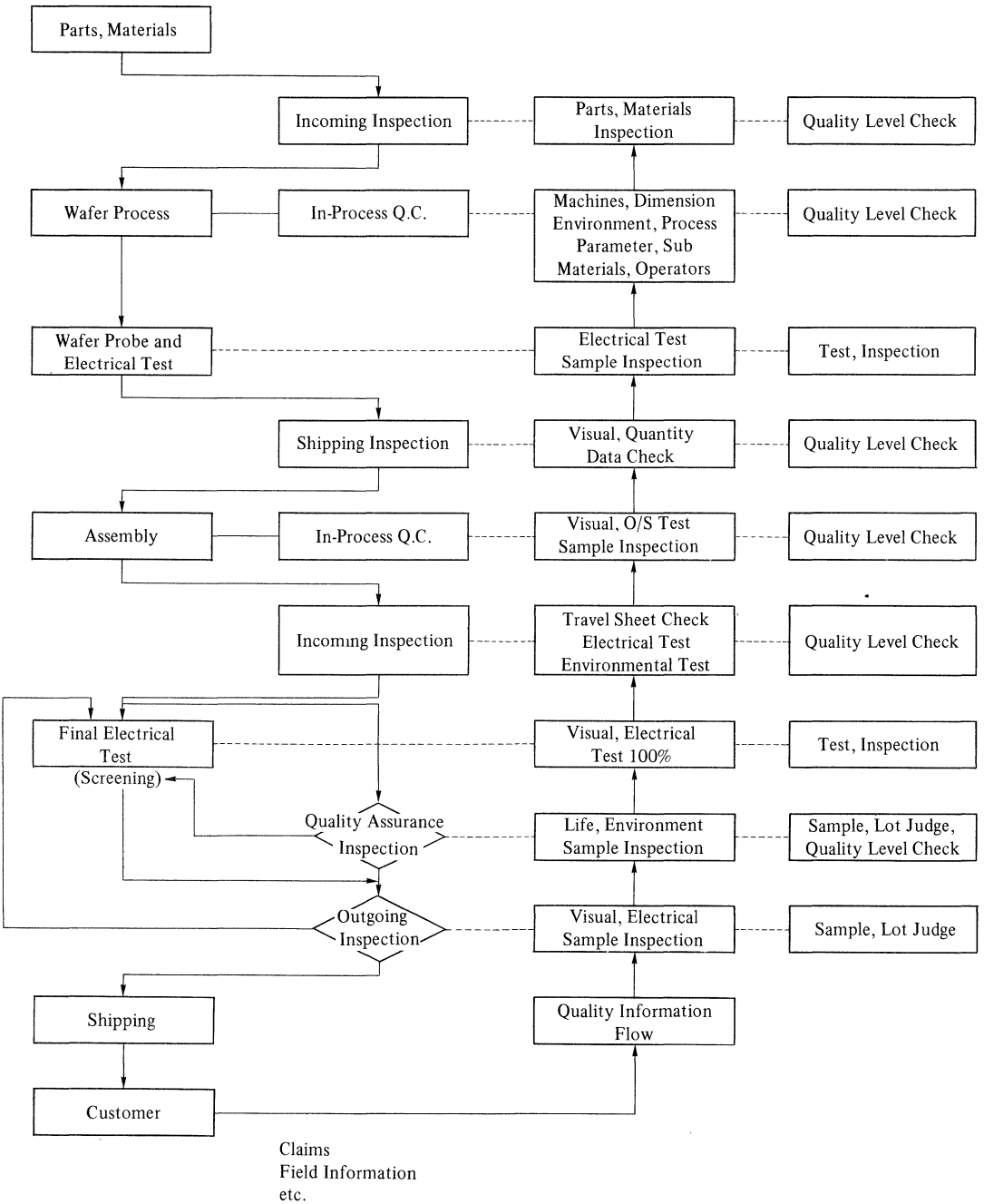
2. Control the first stage thoroughly to make in the quality on development and manufacturing steps.

3. Recognize the importance of quality through quality improvements and quality educations, and then aim at the high quality and high reliability.

4. Inquire into the cause of failure in cooperation with other sections and take measures immediately and completely not to meet the recurrence.

5. Complete the synthetic assurance and control system which satisfy quality, cost, and delivery.

QUALITY CONTROL FLOW CHART IN MANUFACTURE



QUALITY ASSURANCE SYSTEM

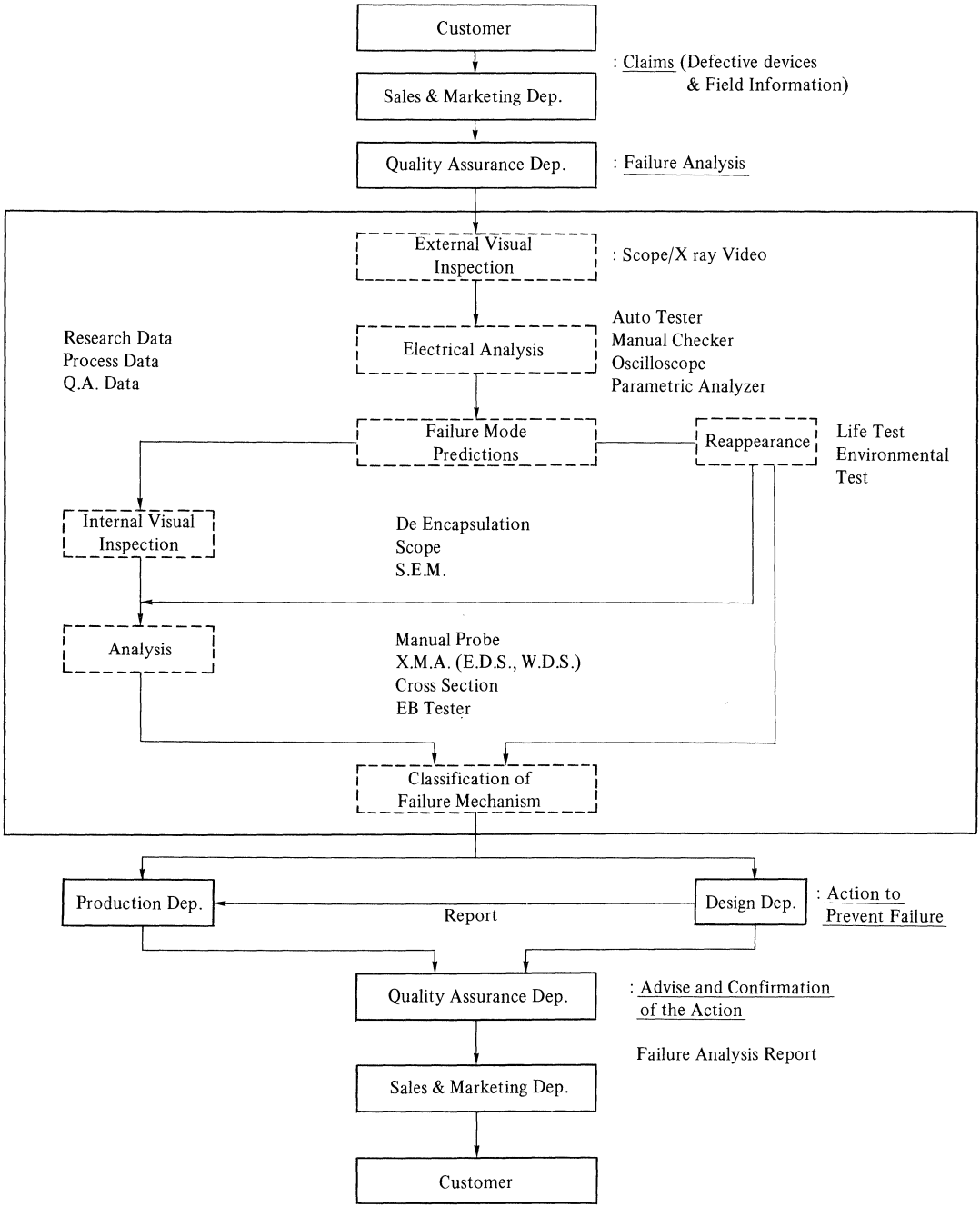
An effective quality assurance system cannot be undertaken on an individual basis. Only a cooperative effort among all divisions can consistently achieve a solid guarantee of top quality. Put into practical use, a system of this type must be functional, it must be based on the idea of standardization, and it must quickly accommodate the data and feedback that continually pass between departments.

We have developed a Quality Assurance System that incorporates these concepts. Our Quality Assurance Department is set up to ensure fast, accurate relay of information between divisions and prompt execution of quality assurance tasks at each step in the manufacturing process – from product development to mass production.

At the product development stage, the tasks required in all succeeding stages are defined and responsibility for their execution is assigned. The Quality Assurance Department then undertakes inspections from a comprehensive point of view, through its inquiry groups. Our quality and reliability criteria are geared to meet reliability and qualification testing standards such as MIL, EIAJ, and JIS to ensure that our product designs, processes, and conformity to standards are approved.

At the mass-production stage, the Manufacturing Department undertakes strict control of processes, product quality within processes, equipment, and the environment, in order to build in quality at each step. The Quality Assurance Department safeguards overall quality by inspecting incoming materials, controlling product amendments, maintaining accuracy in measurement devices, inspecting wafers and making final checks, monitoring quality, and undertaking quality assurance checks which ensure that no defective products reach the market.

FAILURE ANALYSIS FLOW CHART



LOT ASSURANCE INSPECTION

(+ASSEMBLY INCOMING INSPECTION)

Sampling: Every Wafer Lot

No.	TEST ITEMS	TEST METHODS			LTPD (%)	Maximum Accept No.
1	ELECTRICAL (Open, Short check)	Auto Tester QAT Specification			5	0
2	HIGH TEMPERATURE OPERATING LIFE	Ta = T jmax 125°C 20 Hrs. Dynamic Operation			10	0
3	THERMAL SHOCK (liquid)	Ta = T stgmin ~ T stgmax (5′ –10″ –5′) 10 Cycles			20	0
	MIX PCT	TYPE A DIL package	TYPE B FPP-1H package	TYPE C FPP-2, 3 package		
	SOLDERING HEAT	260°C Lead only 10 sec.	260°C Full dip 5 sec.	260°C Lead only 10 sec. (2.5 x 4)		
	THERMAL SHOCK	T stgmin ~ T stgmax 5 Cycles	T stgmin ~ T stgmax 5 Cycles	T stgmin ~ T stgmax 5 Cycles	20	0
	PRESSURE COOKER	121°C 2 atms 20 Hrs.	121°C 2 atms 20 Hrs.	121°C 2 atms 20 Hrs.		

OUTGOING INSPECTION

Sampling Method: MIL-STD 105D

No.	DIVISION	TEST ITEMS	CRITERIA	LEVEL
1	ELECTRICAL	Function DC AC	QAT Specification	AQL 0.25% *1)
2	APPEARANCE	Heavy Defect Light Defect	Visual Inspection Criteria	0.65% 1.0%

*1) Catastrophic Failures (short, open, or functially inoperative) AQL 0.065%

RELIABILITY TEST REQUIREMENTS

TABLE I RELIABILITY/ENVIRONMENTAL

No.	TEST ITEMS	TEST CONDITION	PACKAGE TYPE		QUALIFY TEST TIME
			PLASTIC	CERAMIC	
1	High Temp. Operating Life	125°C (150°C) Vcc Max	M	M	1000 Hrs.
2	High Temp. Reverse Bias	125°C (150°C) Max	O	O	1000 Hrs.
3	High Temp. Storage	125°C (150°C)	M	M	1000 Hrs.
4	Low Temp. Storage	−40°C (−65°C)	O	O	1000 Hrs.
5	85/85 Temp. Humidity Bias	85°C/85% RH Vcc Max	M	M	1000 Hrs.
6	Low Temp. Operating Life	−20°C (−55°C)	O	O	1000 Hrs.
7	Pressure Cooker	121°C/15PSIG/100% RH	M	*	200 Hrs.
8	Thermal Shock	−40~125°C(−65~150°C)	M	M	200 Cycles
9	Temp. Cycle	−40~125°C(−65~150°C)	M	M	1000 Cycles
10	ESD Sensitivity	2000V/200V	M	M	–
11	Latch Up (CMOS Device Only)	–	M	M	–
12	Mechanical Shock	1500g/Z1, Y1, X1	*	M	–
13	Vibration	20 ~ 2 kHz	*	M	4 Cycles

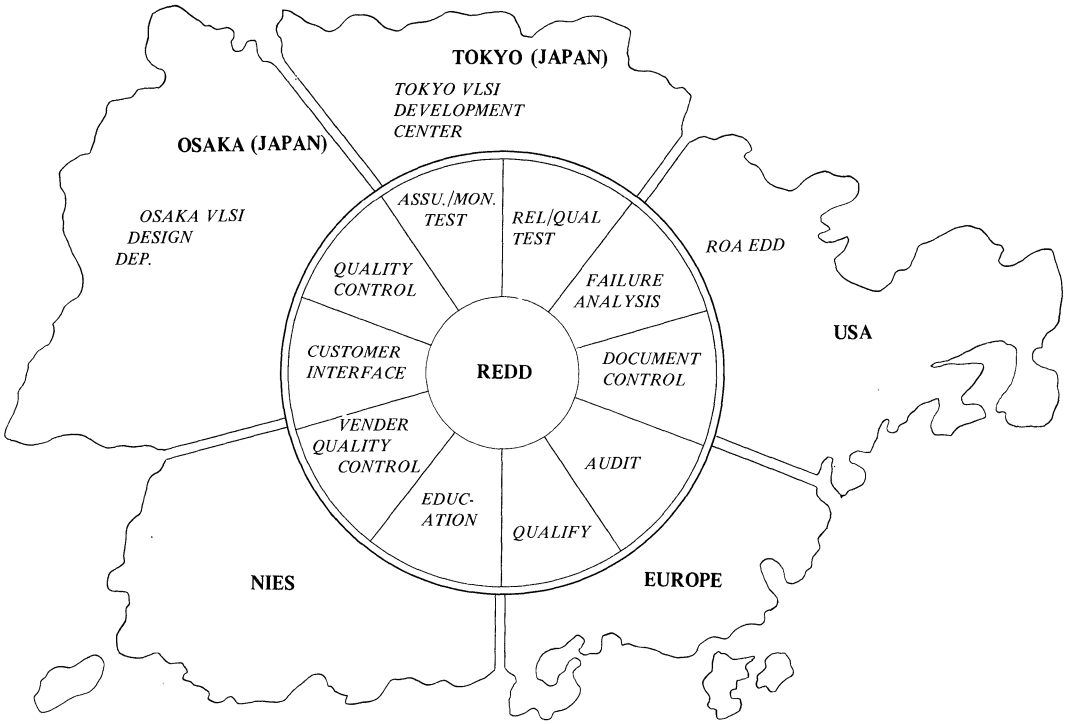
( ): Option

TABLE II MECHANICAL

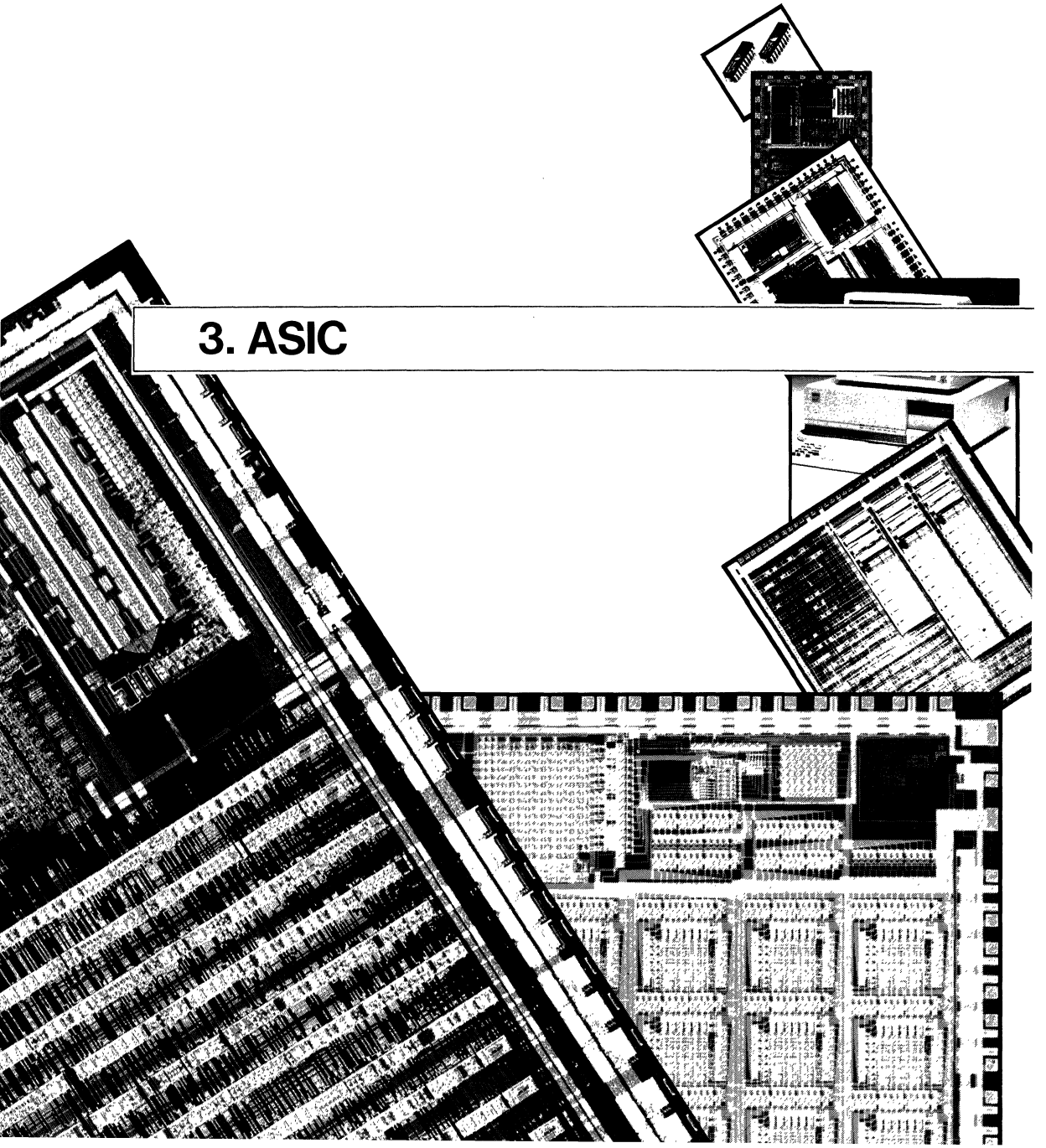
No.	TEST ITEMS	TEST CONDITION	PACKAGE TYPE		QUALIFY TEST TIME
			PLASTIC	CERAMIC	
14	Physical Dimensions	–	M	M	–
15	Marking Permanency	COND.B or D	M	M	–
16	Visual and Mechanical	–	M	M	–
17	Solderability	260°C	M	M	–
18	Lead Integrity (Fatigue, Forming, Pull)	–	O	O	–
19	Hermeticity (Fine, Gross)	F/L: 5×10^{-8} ATMcc/sec G/L: 2 Hrs. at 60 PSIG	*	M	–

M: Mandatory O: Optional *: Not Applicable

QUALITY & RELIABILITY ASSURANCE FUNCTION



REDD RICOH ELECTRONIC DEVICE DLV.



3. ASIC

EPL 20B SERIES

CMOS ELECTRICALLY PROGRAMMABLE LOGIC

■ GENERAL DESCRIPTION

RICOH EPL 20B Series are Field-programmable logic arrays by CMOS EPROM process technology.

Tow product groups make up the EPL 20B Series family.

Group I consists of AND-FIXED OR, XOR Arrays. (EPL 10P8, 12P6, 14P4, 16P2)

Group II consists of AND-FIXED OR, XOR Array, (EPL 16P8) and three Registered AND-FIXED OR, XOR Arrays. (EPL 16RP8, 16RP6, 16RP4)

EPL 20B Series allows users to program easily by programming EPROM Memory Cell, available in both plastic packages for one-shot and reprogrammable Cerdip window packages.

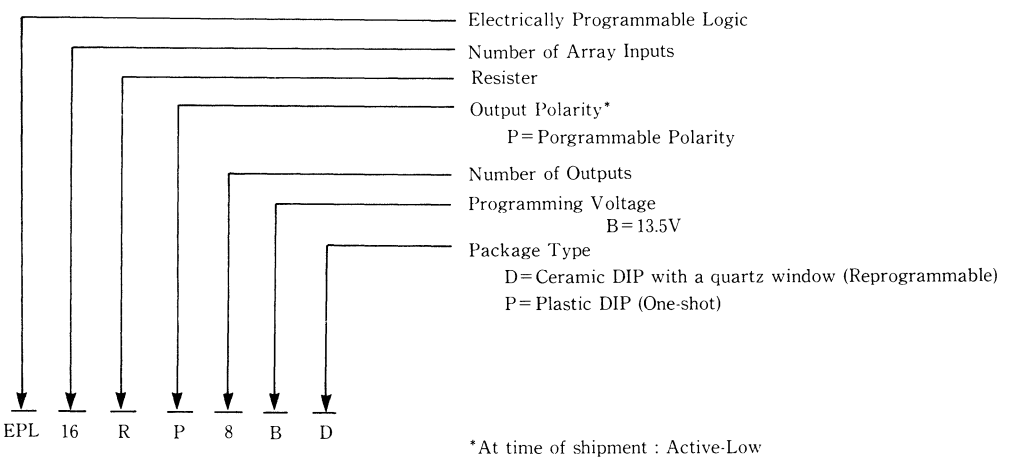
Therefore, it is possible to shorten the development term and check and correct the circuits easily.

■ FEATURES

- CMOS process technology ensures the low power consumption, and higher reliability
- Available in both plastic and Cerdip window packages
- Data copying protection
- Flexibility of logic structure
- Package Type
  20-pin 300mil Plastic DIP (One-shot)
  20-pin 300mil Ceramic DIP with a window (Reprogrammable)
- Product Term : 32 line (Group I)
  : 64 line (Group II)
- Propagation Delay Time
  : 35ns (MAX)
- Each pin has Programmable Polarity
- Up-ward compatibility with MMI PAL

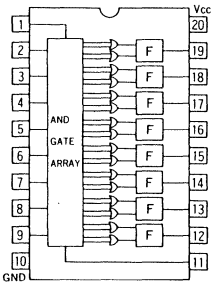
EPL 20B Series FAMILY

PART NUMBER		CONFIGURATION
GROUP I	EPL 10P8 B	10-INPUT, 8-OUTPUT, AND-OR/XOR ARRAY
	EPL 12P6 B	12-INPUT, 6-OUTPUT, AND-OR/XOR ARRAY
	EPL 14P4 B	14-INPUT, 4-OUTPUT, AND-OR/XOR ARRAY
	EPL 16P2 B	16-INPUT, 2-OUTPUT, AND-OR/XOR ARRAY
GROUP II	EPL 16P8 B	10-INPUT, 6-INPUT/OUTPUT, 2-OUTPUT, AND-OR/XOR ARRAY
	EPL 16RP8 B	8-INPUT,8-FEEDBACK,8-OUTPUT,8-REGISTERED,AND-OR/XOR ARRAY
	EPL 16RP6 B	8-INPUT,6-FEEDBACK,2-INPUT/OUTPUT,8-OUTPUT,6-REGISTERED,AND-OR/XOR ARRAY
	EPL 16RP4 B	8-INPUT,4-FEEDBACK,4-INPUT/OUTPUT,8-OUTPUT,4-REGISTERED AND-OR/XOR ARRAY

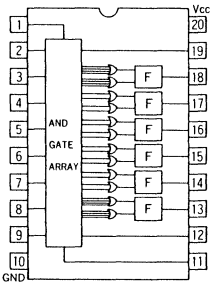


*At time of shipment : Active-Low

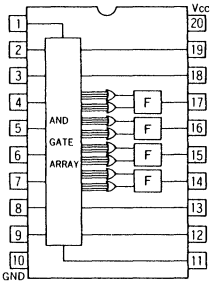
EPL10P8B



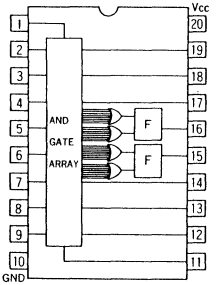
EPL12P6B



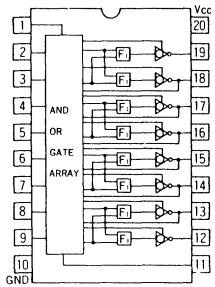
EPL14P4B



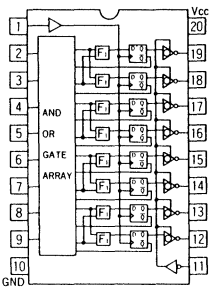
EPL16P2B



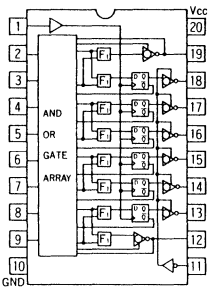
EPL16P8B



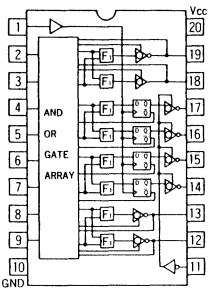
EPL16RP8B



EPL16RP6B



EPL16RP4B



(Note) F : FEATURE Cell
(OR, XOR, POLARITY)

F1 : FEATURE1 Cell
(OR, XOR)

: FEATURE2 Cell
(POLARITY)

■ Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc	Vcc supply voltage	With respect to GND	−0.3~ 7.0	V
Vpp	Vpp supply voltage		−0.3~14.5	V
V_I	Input voltage		−0.3~Vcc+0.3	V
V_O	Output voltage		−0.3~Vcc+0.3	V
Pd	Maximum power consumption	Ta=25℃	700	mW
Topr	Ambient operating temperature		0~70	℃
Tstg	Storage temperature		−40~125	℃

■ Capacitance

Symbol	Parameter		Condition	Value			Unit
				Min	Typ.	Max	
C_{IN}	Input capacitance	2~9, 11 pin	V_{IN}=0V to Vcc			6	pF
		1 pin				20	pF
C_{OUT}	Output capacitance (12~19 pin)		V_{OUT} = 0V, f = 1MHz			12	pF

D.C.Characteristics (Ta=0 to 70℃, V_{CC}=5V±5%)

Symbol	Parameter		Condition	Value			Unit
				Min	Typ.	Max	
I_{LI}	Input current leakage		V_{IN}=0V to Vcc	−20		20	μA
V_{IL}	"L" input voltage			−0.3		0.8	V
V_{IH}	"H" input voltage			2.0		Vcc+0.3	V
V_{OL}	"L" output voltage		V_{CC}= Min, I_{OL}=8mA		0.3	0.5	V
V_{OH}	"H" output voltage		V_{CC}= Min, I_{OH}=−3.2mA	2.4	4.4		V
I_{LO}	Output current leakage in OFF status	Group II	V_O= 0V to V_{CC}	−20		20	μA
Icc1	Source current (Stationary status)	Group I	V_{CC}=Max, Output=open V_I=GND or V_{CC}			40	mA
			V_{CC}=Max, Output=open V= 2.4V			50	mA
		Group II	V_{CC}=Max, Output=open V_I=GND or V_{CC}			60	mA
			V_{CC}=Max, Output=open V_I=2.4V			70	mA
Icc2	Source current (Operating status)	Group I	V_{CC}= Max, Output=open			50	mA
		Group II	f=10MHz, V_I=0.8V or 2.4V			70	mA

Note 1. Group I is equipped with a power-down circuit. When neither "OR" nor "XOR" in the FEATURE cell is used, current for the unused product term is cut off.

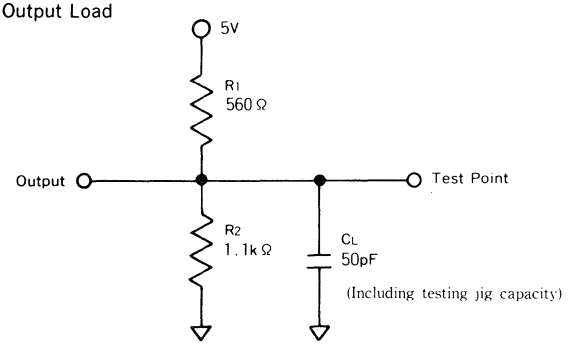
2. Group I has two times as many product terms as PAL™, therfore, Power consumption is reduced to approximately half value when the user replace PAL™ with Group I

(Above mentioned specifications are in the condition of use all product terms.)

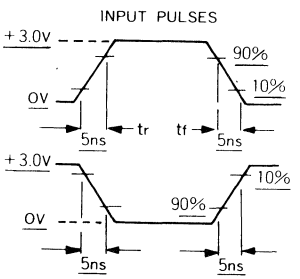
A.C.Characteristics (Ta = 0 to 70°C, V_{CC} = 5V ± 5%)

Symbol	Item			Condition	Typical Min	Typical Std	Typical Max	Unit
t_{PD}	Propagation Delay Time	Input or feedback to output	Group II	R_1 = 560Ω, R_2 = 1.1KΩ, C_L = 50pF		25	35	ns
t_{CLK}		Clock to output or feedback				15	25	ns
t_{PZX}		Pin11 to output enable				15	25	ns
t_{PXZ}		Pin11 to output disable				15	25	ns
t_{PIZ}		Input to output enable				25	35	ns
t_{PIX}		Input to output disable				25	35	ns
f_{MAX}	Maximum frequency				20			MHz
t_{WL}	Minimum clock time width		Low		20			ns
t_{WH}			High		20			ns
t_{SU}	Input set-up time				25			ns
t_H	Input hold time				0			ns

Output Load

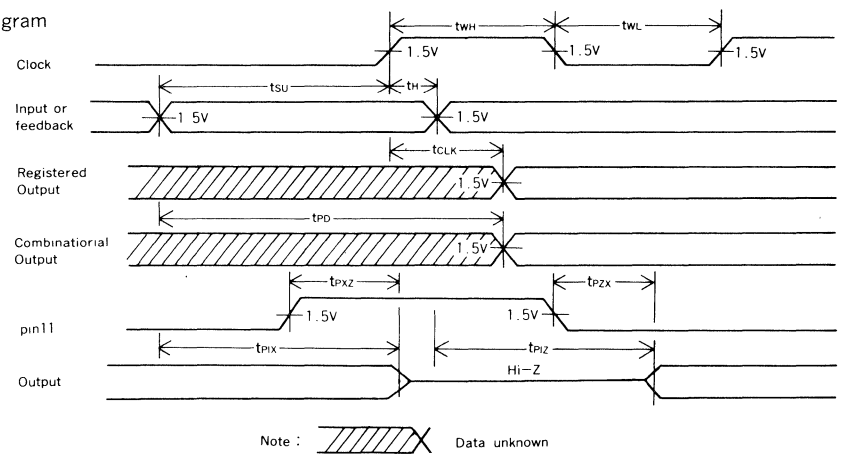


Input Waveform



NOTE : This is the A.C. characteristic measurement with a voltage of 1.5V on both the input and output.

Timing Diagram



■ Configurations of EPL Logic

RICOH EPL **20B Series** Group I provides 32 input **terms and 32 product terms.**

RICOH EPL **20B Series** Group II provides 32 input terms and 64 product terms.

Input pins in both groups are activated for regular logical operation at a TTL level.

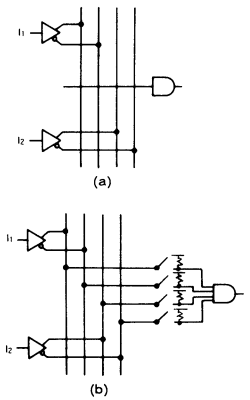
All intersection points of the input terms and product terms are provided with an EPROM cell connection. These intersections are connected prior to delivery.

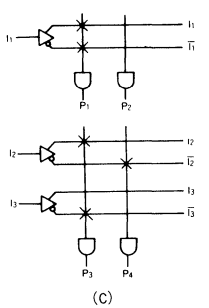
The AND gate are illustrated in logic diagram (a) below. The switches indicated in logic diagram (b) correspond to the EPROM cell connections. All switches are closed when the devices are unprogrammed.

As illustrated in logic diagram (c), when neither positive input (I) nor negative input ($\overline{I}$) is programmed, the AND output (P1) becomes "inactive".

When both positive input (I) and negative input ($\overline{I}$) are programmed, the AND output (P2) becomes "don't care" logically.

Each output includes a FEATURE cell in addition to the programmable AND-FIXED OR logic. The FEATURE cell enables the user to program the logic polarity (active-high/active low) and the logical OR, Exclusive-OR case.



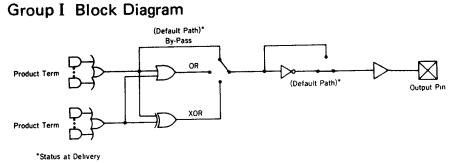


I1	P1	P2
0	0	1
1	0	1

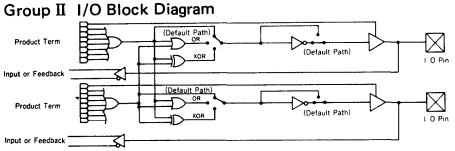
: Programmed (Open)

: Unprogrammed (Connected)

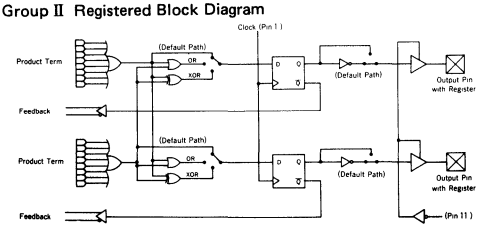
Group I Block Diagram



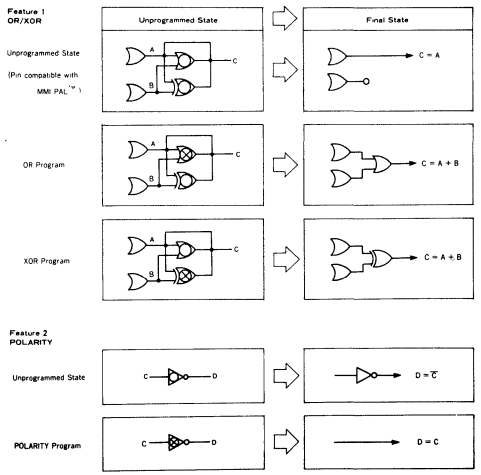
Group II I/O Block Diagram



Group II Registered Block Diagram

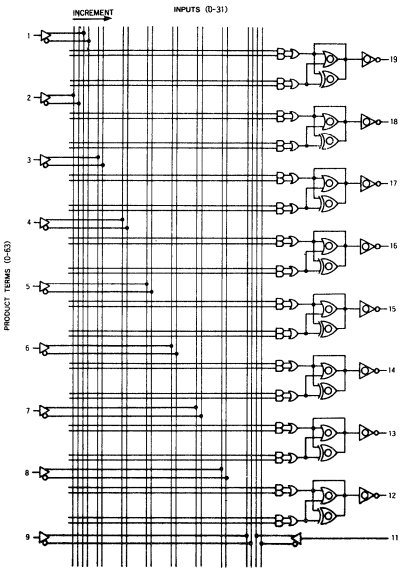


FEATURE CELL



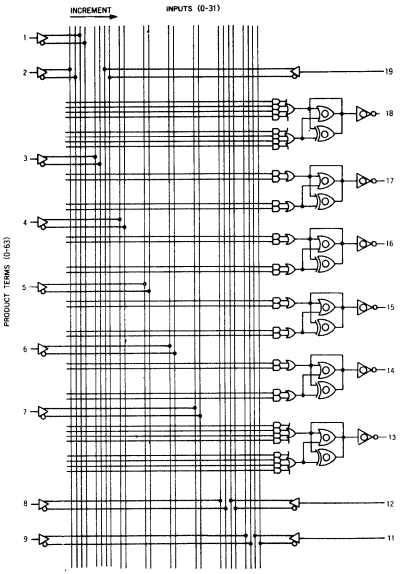
Logic Diagram

EPL10P8B



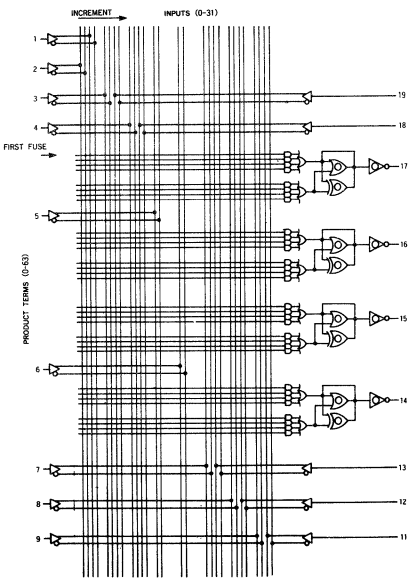
Logic Diagram

EPL12P6B



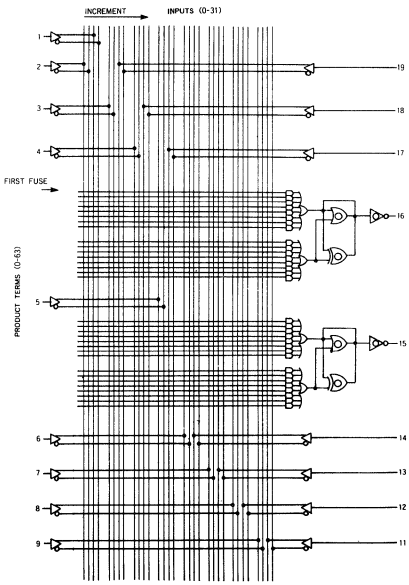
Logic Diagram

EPL14P4B



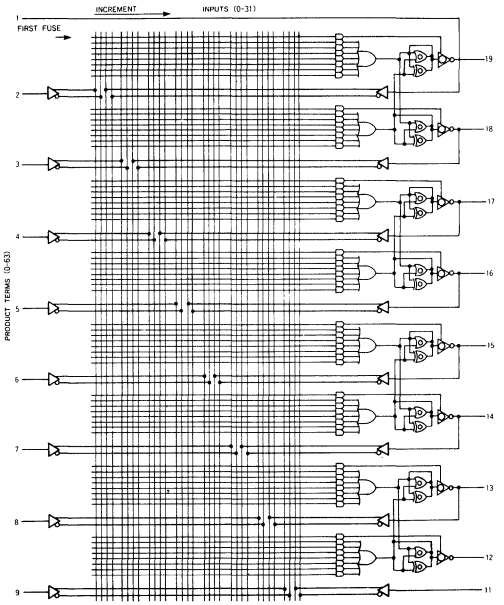
Logic Diagram

EPL16P2B



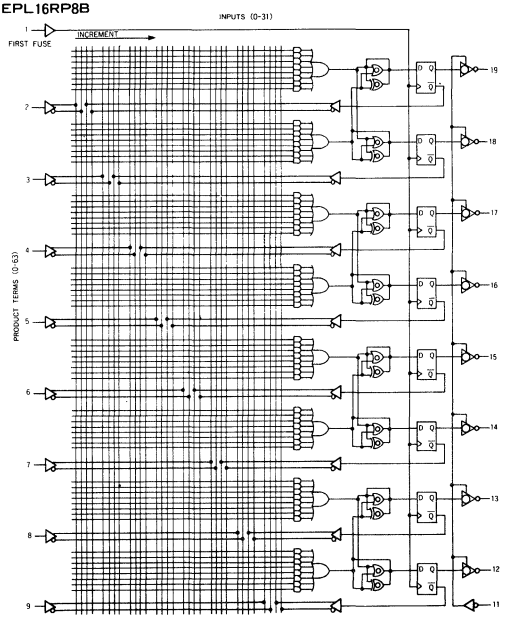
Logic Diagram

EPL16P8B



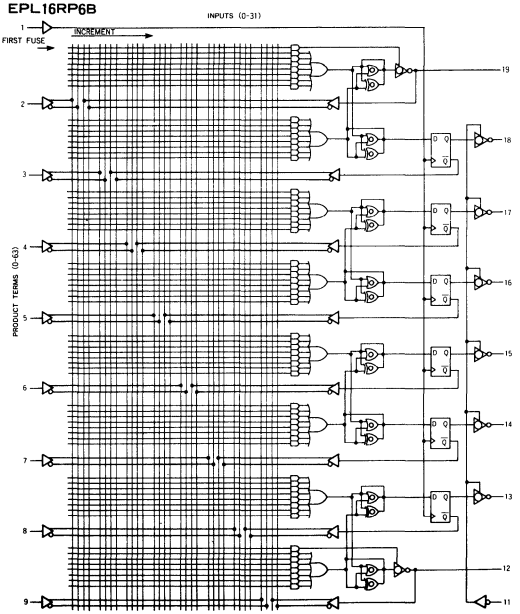
Logic Diagram

EPL16RP8B



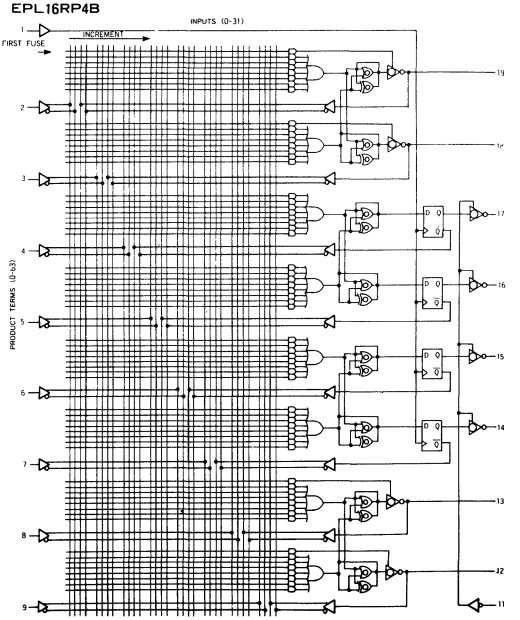
Logic Diagram

EPL16RP6B



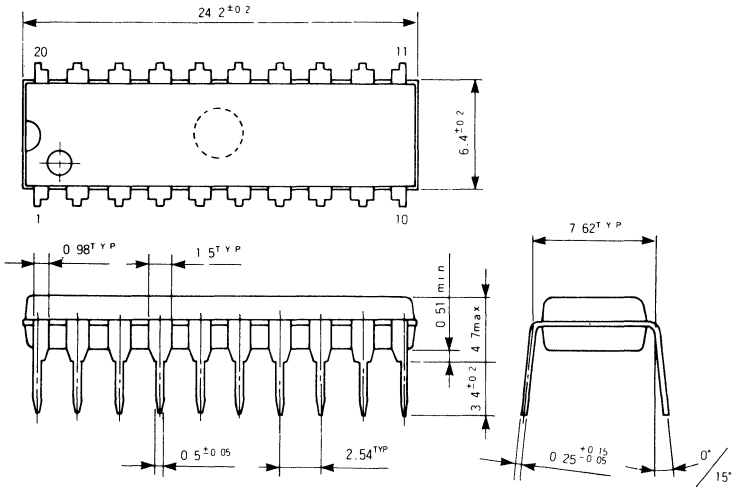
Logic Diagram

EPL16RP4B

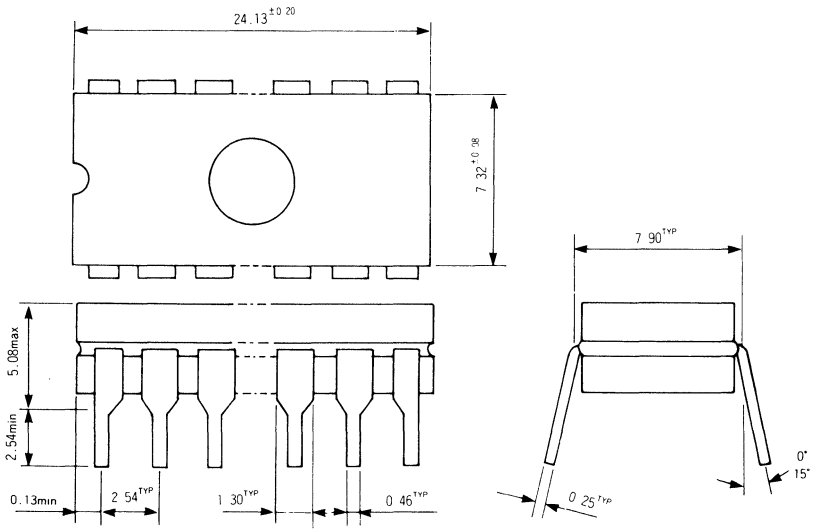


Packaging

20-Pin Plastic DIP Packaging 1-Shot (Unit : mm)



20-Pin Ceramic DIP Reprogrammable (Glass Seaied with a quartz window) (Unit : mm)



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APPLICATION MANUAL

Version 0.1

EPL APPLICATION MANUAL
《INDEX》

Issued on December 1, 1987

CHAPTER 1

CHAPTER 2

CHAPTER 1

1 – 1 Introduction

PLD (Programmable Logic Devices) is the logic IC which allows user to program the specification of his own, and allows to realize the logic equivalent to several pieces of standard TTL logic ICs.

Computer system consists of microprocessor, memory and peripheral circuits. The integrity of memory, processor and etc. with improved general-purpose properties has been enhanced, and system is compact and provides high performance. However, since the inherent peripheral circuits, which constitute the system, can not be used in common with other systems, a number of TTL have been incorporated. PLD is the one that meets the requirement for making peripheral circuits inherent to this system LSI.

The fundamental configuration of PLD is based on the theory of "Any Boolean expression, no matter how complex, may be written in sum-of-products form". In other words, PLD is configurated from AND Array, which generates product term of input signal, and OR Array, which takes the sum of product term.

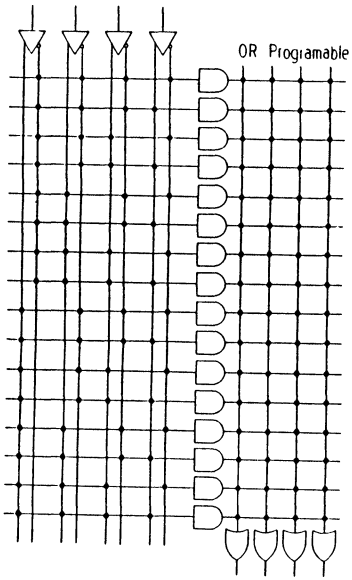
Generating method of this AND-OR Array is classified in the following 3 kinds.

(1) AND fixing, OR programmable (PROM)
(2) OR fixing, AND programmable (PAL)
(3) AND · OR programmable (FPLA)

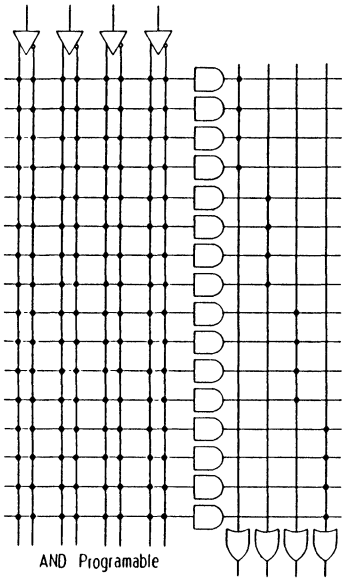
AND fixing, OR programmable PLD of (1) fixes decode logic on AND Array beforehand, as shown on Diagram 1–1–1–(a) and allows user to program OR Array. To configulate logic circuits with PROM, truth table is written as it is.

In the OR fixing, programmable PLD of (2), OR Array have been connected beforehand, as shown on Diagram 1–1–1–(b) and AND Array is already user programmable. EPL offered by RICOH is of this configuration and allows erase and rewrite since it uses EPROM memory cell.

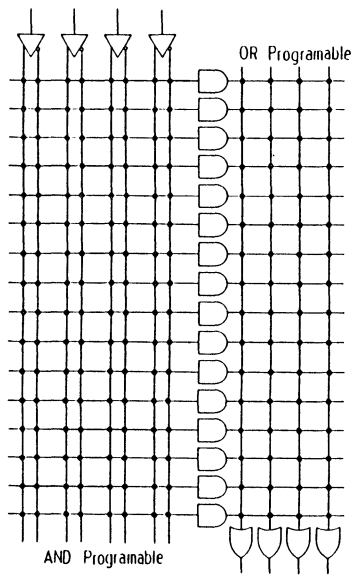
AND-OR programmable PLD allows both arrays programmable, as shown on Diagram 1–1–1–(c), and offers high level of flexibility to the user, nevertheless, undergoes delay in 2 step array and provides complexity in design compared to PAL.



(a) PROM



(b) PAL



(c) FPLA

Diagram 1 – 1 – 1 Configuration diagram of various PLD

1 – 2 Architecture of EPL

1 – 2 – 1 Feature

(1) Lower power consumption and higher reliability with CMOS EPROM process
(2) Ceramic packaged product is capable of erasing ultraviolet rays
(3) Number of product term : 32 (Group I) Twice as much as the counterpart of PAL offered by MMI Co.
: 64 (Group II)
(4) Replaceable with general-purpose logic
(5) Package : 20 pins 300 mil plastic DIP
: 20 pins 300 mil ceramic DIP (with window)
(6) Output polarity is programmable for each pin
(7) Data copy preventive function attached
(8) Input to output propagation delay time : Series 20B 35 ns (MAX)
(9) FEATURE CELL (OR, XOR) increases flexibility in logic configuration.
(10) Upper compatible with PAL of MMI Co. at pin level

1 – 2 – 2 Configuration of EPL

EPL is the programmable logic device (PLD), using CMOS EPROM process technology. With EPL, it contributes to the compactness of the system, reduction in cost and saving in power consumption when "FEATURE CELL" architecture is induced.

Group I consists of AND-OR (fixed), while Group II consists of 2 configurations of AND-OR (fixed) and AND-OR (fixed) – Register.

Block diagram of EPL is shown on Diagram 1–2–1.

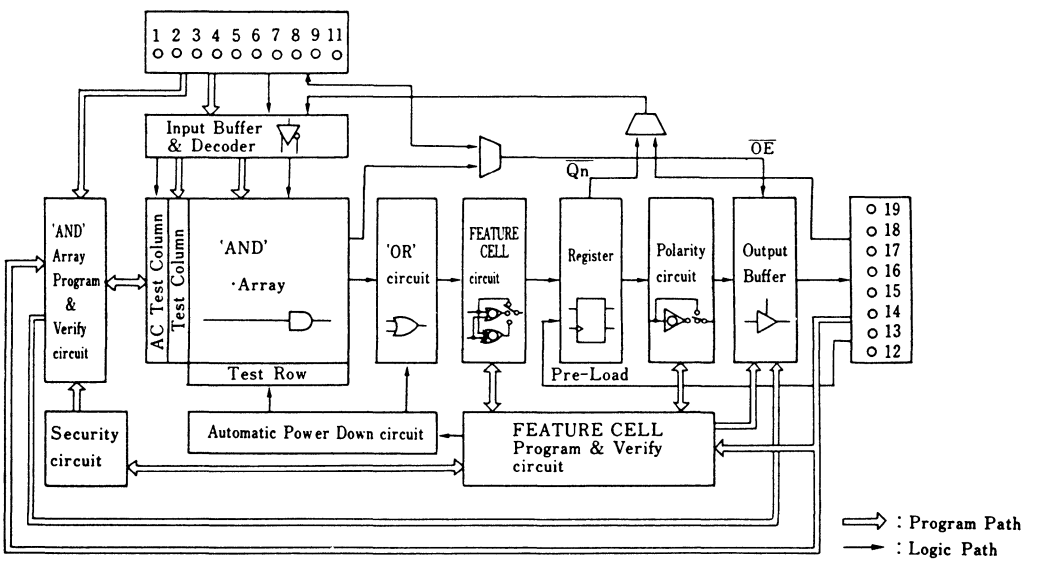


Diagram 1 – 2 – 1 Block diagram of EPL

In the block diagram, the flow of signal during logic mode (during operation as logic circuit) is represented by →, while the flow of signal during program mode by ⇒. EPL makes the flow of signal during logic mode completely independent, and is so designed that the delay in signal during logic mode is minimized.

Fundamental configuration components are input buffer, AND Array, OR circuits and output buffer. Reciprocal signals are generated at input buffer for all inputs and becomes the signals to AND Array. The program of AND Array means to select the required signal among signals from input buffer and generate the product term desired by user. By passing the output of this product term through OR circuits, product sum Boolean equations is executed on the device. In addition to this fundamental PLD configuration, the setup of register and feedback input will materialize sequential circuit.

"FEATURE CELL" circuit, polarity circuit, AC test circuit, automatic powerdown circuit are not found in the conventional PAL.

"FEATURE CELL" circuit is the circuit which allows the user to select each condition of "BYPASS" "OR" and "XOR". "BYPASS" provides the same function as for the PAL equivalent product, while "OR" allows to double the number of input product term to OR circuit, and "XOR" executes excessive OR, or else of OR circuit output. With polarity circuit, it allows to select the output polarity independently for each output pin. Powerdown circuit executes power cutdown corresponding to the applicable condition of product term at EPL · GI. AC test circuit allows to run the test at the plant (inspection for delayed time after assembling of mainly plastic product.)

Security circuit is the circuit which prevents others from copying. Also, as mentioned at the beginning, memory cell of EPROM is used as fuse for EPL, which eliminates the use of microscopic observation, thus, complete confidentiality is maintained.

These are the configulations being features of EPL. Meanwhile, EPL Series 20 family is shown below and simple block diagram on Diagram 1–2–2.

Table 1 EPL Series 20 family

Product name		Function
Group I	EPL 10P8 B	10 input 8 output AND-OR/XOR Array
	EPL 12P6 B	12 input 6 output AND-OR/XOR Array
	EPL 14P4 B	14 input 4 output AND-OR/XOR Array
	EPL 16P2 B	16 input 2 output AND-OR/XOR Array
	EPL 16P8 B	10 input 6 input output 2 output AND-OR/XOR Array
Group II	EPL 16RP8 B	8 input 8 feedback 8 output 8 register AND-OR/XOR Array
	EPL 16RP6 B	8 input 6 feedback 2 input output 6 output 6 register AND-OR/XOR Array
	EPL 16RP4 B	8 input 4 feedback 4 input output 4 output 4 register AND-OR/XOR Array

1 – 3 Specification of EPL

1 – 3 – 1 Absolute maximum rating

Absolute maximum rating of EPL is as follows.

Symbol	Parameters	Conditions	Value	Unit
Vcc	Vcc power supply voltage	With respect to GND	-0.3~7.0	V
Vpp	Vpp power supply voltage Series 20B		-0.3~14.5	V
VI	Input voltage		-0.3~Vcc+0.3	V
Vo	Output voltage		-0.3~Vcc+0.3	V
Pd	Power dissipation	Ta = 25°C	700	mW
Topr	Operating ambient temperature		0~70	°C
Tstg	Storage temperature		-40~125	°C

1 – 3 – 2 Characteristics of EPL

DC characteristics as well as AC characteristics of EPL, which uses CMOS · EPROM process technology, have been highly improved compared to the conventional bipolar type PLD.
DC, AC characteristics of Series 20B are shown below.

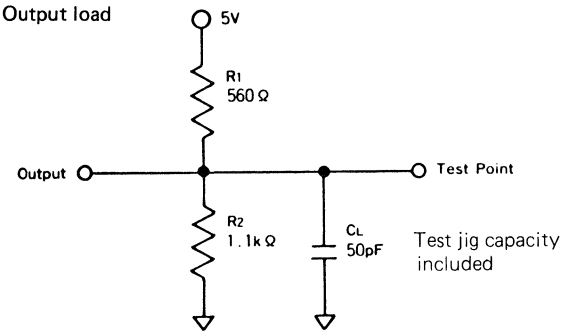
D.C. characteristics EPL Series 20B (Ta=0~70°C, Vcc=5V±5%)

Symbol	Parameters		Conditions	Limits			Unit
				Min.	Typ.	Max.	
ILI	Input leak current		VIN=OV~Vcc	-20		20	μA
VIL	"L" input voltage			-0.3		0.8	V
VIH	"H" input voltage			2.0		Vcc+0.3	V
VOL	"L" output voltage		Vcc=MIN, IOL=8mA		0.3	0.5	V
VOH	"H" output voltage		Vcc=MIN, IOH=-3.2mA	2.4	4.4		V
ILO	OFF state output leak current	GII	Vo=OV~Vcc	-20		20	μA
Iccl	Supply current current (standby)	GI	Vcc=MAX, output =open, Vi=GND or Vcc			40	mA
			Vcc=MAX, output =open, Vi=2.4V			50	mA
		GII	Vcc=MAX, output =open, Vi=GND or Vcc			60	mA
			Vcc=MAX, output =open, Vi=2.4V			70	mA
Icc2	Supply current current (operation)	GI	Vcc=MAX, output =open, f=10MHz, Vi=0.8V or 2.4V			50	mA
		GII				70	mA

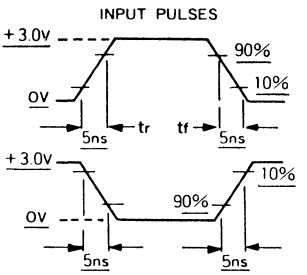
A.C. characteristics of EPL Series 20B (Ta=0~70°C, Vcc=5V±5%)

Symbol	Parameters			Conditions	Limits			Unit
					Min.	Typ.	Max.	
t_{PD}	Propagation delay time	Input or feedback to output	Group II	R_1=560Ω R_2=1.1kΩ C_L=50pF		25	35	nS
t_{CLK}		Clock to output or feedback				15	25	nS
t_{PZX}		Pin 11 to output enable				15	25	nS
t_{PXZ}		Pin 11 to output disable				15	25	nS
t_{PIZ}		Input to output enable				25	35	nS
t_{PIX}		Input to output disable				25	35	nS
f_{MAX}	Max. frequency				20			MHz
t_{WL}	Min. clock width		Low		20			nS
t_{WH}			High		20			nS
t_{SU}	Input setup time				25			nS
t_H	Input hold time				0			nS

Output load

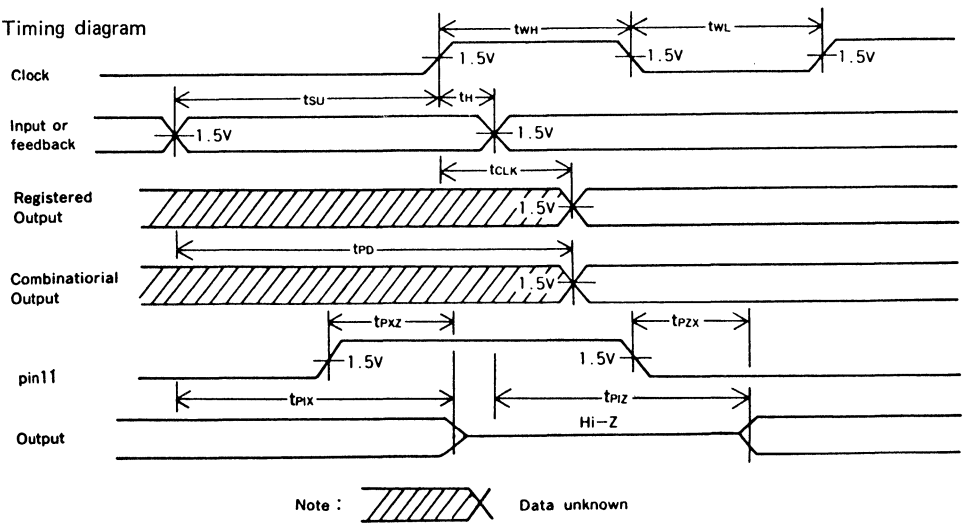


Input wave shape (During measurement of A.C. characteristics)



A.C. characteristics is measured at 1.5V point of both input and output.

Timing diagram



Series 20B is fabricated under the same process technology as for 256K · CMOS · EPROM (RD27C256). This process is the latest CMOS two-layer polysilicone gate process which has materialized high performance of access time 150 ns with 27C256 upon adoption of 1.5μ rule EPROM CELL. Thanks to this, the same delay time of 35 ns as for the standard product of bipolar PAL has materialized.

Power supply voltage dependence characteristics of input to output propagation delay time (tPD) at room temperature is shown on Diagram 1–3–1, while temperature dependence characteristics at Vcc=4.7V on Diagram 1–3–2. It is readily seen from Diagram 1–3–1 that Series 20B gives tPD-20 ns under the standard operating condition (Vcc= 5.0V, room temperature : 25°C).

Diagram 1–3–3 illustrates the characteristics of current consumption (Icc) in the case where 16 pieces and 32 pieces of product term are respectively used. From Diagram 1–3–3, when EPL · GI is used in place of PAL (when 16 pieces of product term are in use), Icc1=5.5mA (in static) and Icc2=8mA (in motion : at 10MHz) (standard operating condition).

Diagram 1–3–4 and 1–3–5 illustrate the output drive capacity. From Diagram 1–3–4 and 1–3–5, Ioh=3.5mA (at Voh=4.4V) and Iol=10mA (at Vol=0.3V) at Vcc=4.7V, room temperature.

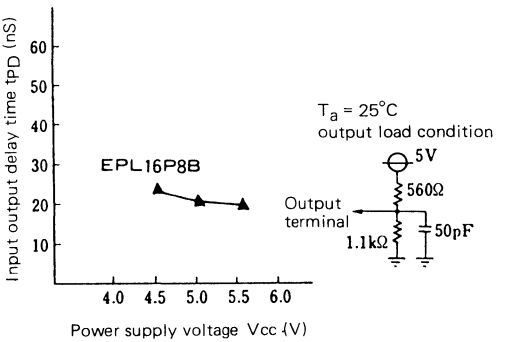


Diagram 1–3–1 **Power supply voltage and input output delayed time characteristics**

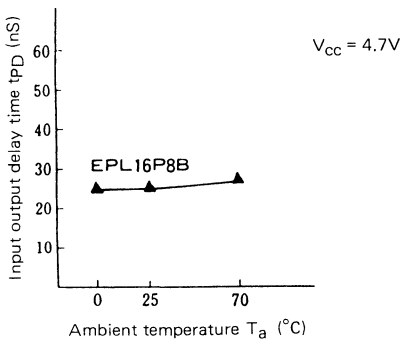


Diagram 1–3–2 **Temperature characteristics of input output delay time**

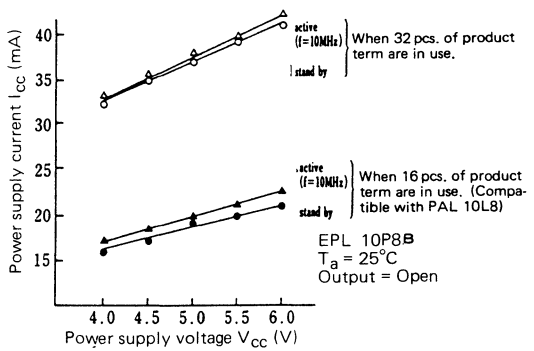


Diagram 1–3–3 **Power supply current characteristics**

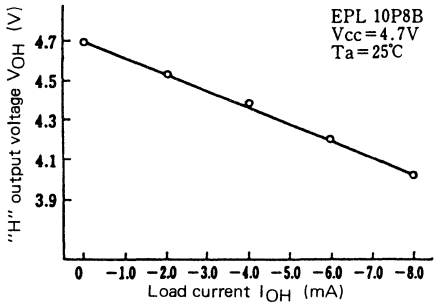


Diagram 1 – 3 – 4 **Load current and "H" output voltage characteristics**

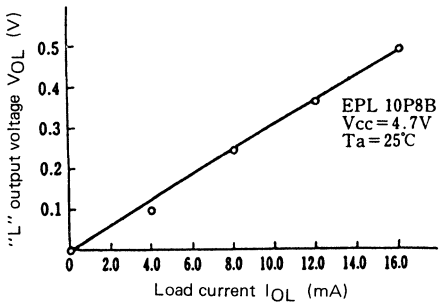


Diagram 1 – 3 – 5 **Load current and "L" output voltage characteristics**

1 – 4 EPL logic Mode

EPL has EPROM memory cells at all intersections of product term on the AND Array and input term. For example, when converting Boolean equation, that is, Z1 = A * B * $\overline{C}$ + A * $\overline{B}$ * D (* • • AND, + • • OR), to gate level, it is described as Diagram 1–4–1. 1–4–1.

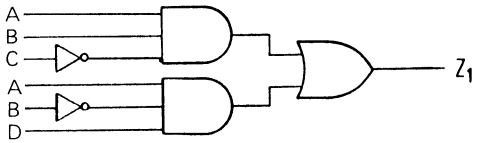


Diagram 1 – 4 – 1 $Z1 = A * B * \overline{C} + A * \overline{B} * D$

Then, when representing Z1 as input term, A,$\overline{A}$ B,$\overline{B}$ C,$\overline{C}$ D,$\overline{D}$ and as logic diagram of 2 pieces of product term, it is readily seen that Z1 = A * B * $\overline{C}$ + A * $\overline{B}$ * D is represented when connecting intersections, as shown on Diagram 1–4–2.

X mark on the logic diagram represents the condition under which CELL of EPROM remains unprogrammed.

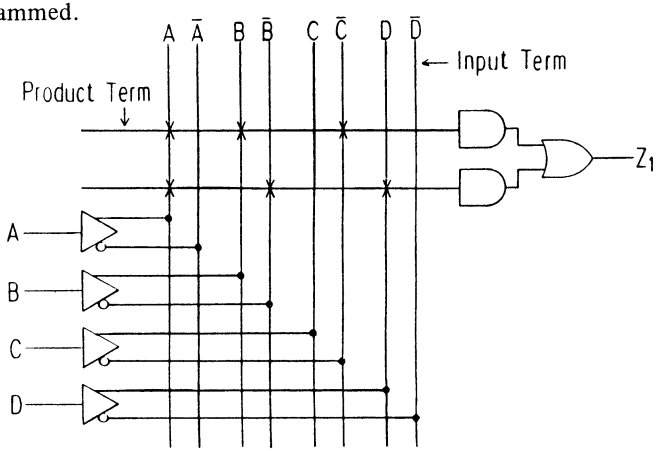


Diagram 1 – 4 – 2 Logic diagram of Z1

As shown on Diagram 1–4–3, CELL of EPROM corresponds to the switch of AND gate input, and when it is programmed, switch opens. Here, if all SW1 ~ SW4 are kept OFF condition, that is, if EPROM is programmed AND gate outputs "H" since it is PULL-UP, as shown on Diagram 1–4–3.

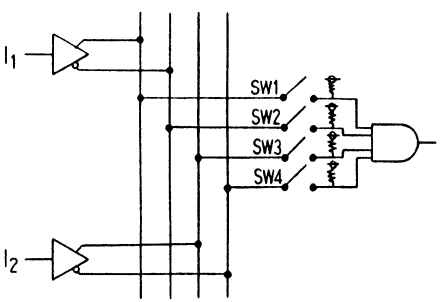


Diagram 1–4–3 EPROM connection

As shown on Diagram 1–4–4, if intersection is (a), switch is OPEN, which indicates the programmed condition. If intersection is (b), switch is closed, which indicates the unprogrammed condition. Therefore, it readily suggests to program EPROM CELL at the intersection not required by design (turn the switch OFF). For example, as shown on Diagram 1–4–5, if I 1 and $\overline{I\,1}$ are not programmed together at (a), AND output P 1 turns to non-active ($P\,1 = I\,1 * \overline{I\,1} = O$), and if I 1 and $\overline{I\,1}$ are programmed together, AND output P 2 turns logically to "Don't care" ($P2 = I\,1 * \overline{I\,1} = 1$).

(a) ┼ : Program (open)

(b) ✳ : Not Program (connected)

Diagram 1–4–4 Status of intersection

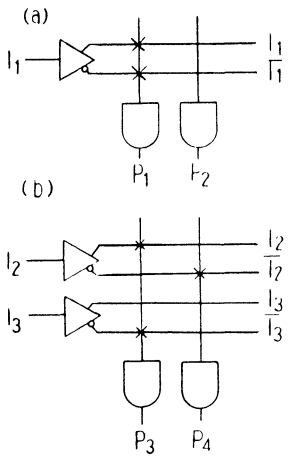


Diagram 1–4–5 Relationship between intersection and output

1 – 4 – 1 FEATURE CELL

FEATURE CELL architecture has been adopted to EPL to allow user to enhance integrity and handle easier.

FEATURE CELL consists of logic gate of "OR" and "XOR", logic gate of "POLARITY" and PROM switch which selects those. Furthermore, EPL · GI has the product term of 32 which is twice of PAL of 16. EPL · GII allows adjacent output channels to obtain share. In other words, EPL has the integrity 2 times to 4 times more than PAL.

Next, output block configuration of EPL is described. Diagram 1–4–6 illustrates the output block of EPL · GI, Diagram 1–4–7 for output input block of EPL · GII and Diagram 1–4–8 for register block of EPL · GII. The position of switch shown as (DEFAULT PATH) in the diagram is set at the time of shipment (erase condition). Under the erase condition, output polarity is ACTIVE LOW, and FEATURE CELL is unused, which is under the same condition as for the equivalent products of PAL.

Group I

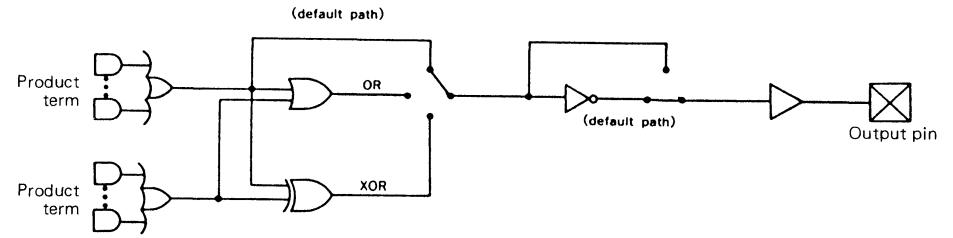


Diagram 1–4–6 Output block of EPL · GI

Group II (I/O Block)

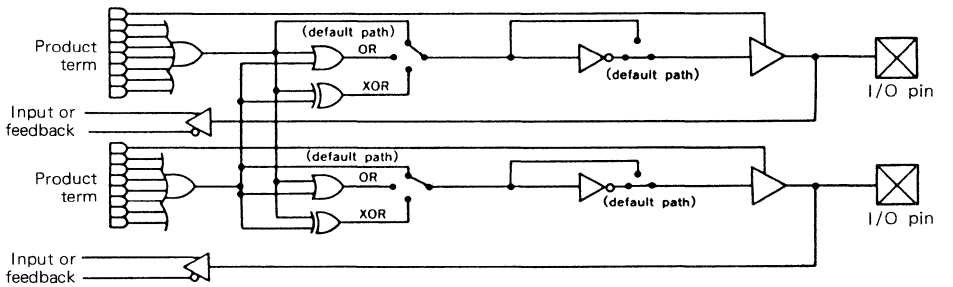


Diagram 1–4–7 Input output block of EPL · GII

Group II (Register · block)

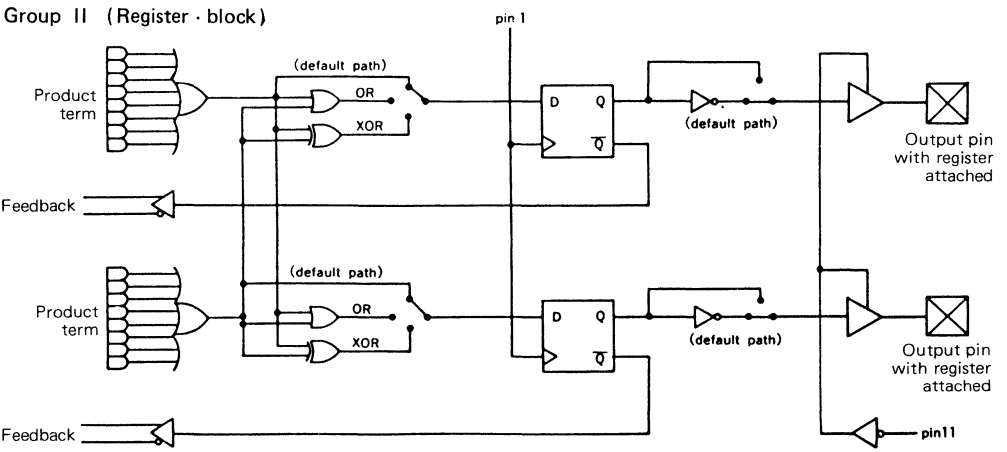


Diagram 1–4–8 Register block of EPL · GII

1 – 4 – 2 Security

After the data has been programmed by user, EPL will for the first time execute semantic logic operation. In other words, for the system in which EPL is used, copy is impossible unless the data programmed in EPL is read-out. (Even copy print substrate, it will not operate unless correct data are programmed in EPL) EPL is equipped with security circuit for prevention of copy. After programming the data in EPL, once security fuse is programmed, it will no longer be able to read the data subsequently programmed. Diagram 1–4–9 illustrates the operation of security circuit. Memory cell signal of AND Array selected by X–Y decoder is read-out by AND Array Sense Amp. On the other hand, the signal of Security Fuse is read-out by Security Sense Amp. The output SEQ of Security Sense indicates "H" if Security Fuse is not programmed, while indicates "L" if programmed. As shown on Diagram 1–4–9, the output of AND Array and AND signal of SEQ equal to the input of output buffer. Accordingly, if Security Fuse is programmed, it gives SEQ = "L" and output becomes "L" regardless of the condition of read-out signal of AND Array. diagram), EPL has independent flow of signal during programming and independent flow of signal during operation as logic circuit. Since security circuit only controls flow of signal during programming, it will give no influence to the operation as logic circuit.

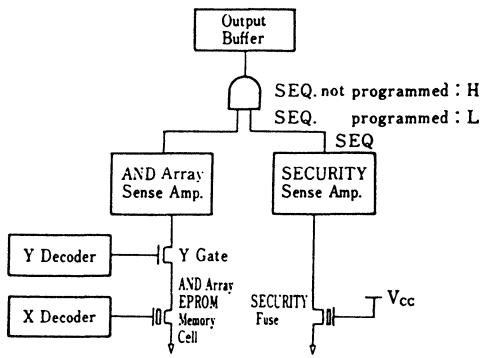


Diagram 1–4–9 Security Circuit

The conventional PAL has also similar function available which is called last fuse. However, in case of PAL in which blown type fuse is used, the programmed fuse is physically blown and if IC chip is microscopically observed, it enables to decode the programmed data. Contrary to this, in case of EPL, memory cell of EPROM is used and programming is executed by movement of electron. Therefore, it is impossible to decode the data through microscopic observation. Accordingly, the use of EPL will completely wipe out the sense of insecurity against leak of security remaining with the system configurated with standard IC and PAL of TTL and etc.

1 – 5 Program mode

1 – 5 – 1 Programming mode

Programming of EPL is executed in the same manner as usual EPROM. Pin out of program mode is illustrated on Diagram 1–5–1. For EPL, application of program voltage (V_{ihp}) to pin 1 (V_{pp}) will change it from usual logic mode to program mode and at which time, Group I turns to 128 X 8 bit EPROM, while Group II to 256 X 8 bit EPROM.

Meanwhile, there are two different program modes available as follows. (Mode table is shown on Diagram 1–5–1).

- Program/Verify mode of AND Array
- Program/Verify mode of FEATURE CELL

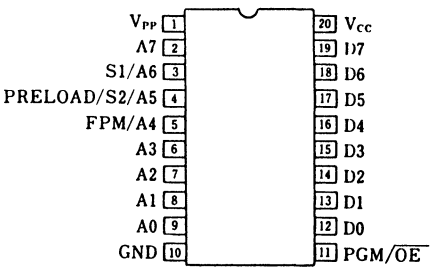


Diagram 1–5–1 Pin out for program mode

1 – 5 – 2 Program/Verify mode of AND Array

This mode operates program and verify of AND Array.

(1) Program

① Program voltage (V_{ihp}) is applied to pin 1 (V_{pp}).
② The address is set up.
③ The data is set up.
④ Program is executed by applying program "H" input voltage (V_{ihh}) in width of 1 ms to pin 11 (PGM/$\overline{OE}$) as program pulse. Program mode is executed in accordance with the flow chart (high speed program mode) shown on Diagram 1–5–2.

(2) Verify

① Program voltage (V_{ihp}) is applied to pin 1 (V_{pp}).
② Address is set up.
③ Verify is accomplished by making pin 11 (PGM/$\overline{OE}$) to "L" input voltage (Vil) level.

Note 1) The data during programming are –
"0" : write "1" : no write

Note 2) When non-specified INPUT LINE NO is selected, output data turns to LOW.

Note 3) During Program/Verify, fix pin 2 (A7) firmly to LOW.
(provided that Note 2 and Note 3 cover only Group I)

1 – 5 – 3 Program/Verify mode of FEATURE CELL

This mode operates program and verify of FEATURE CELL (OR, XOR, POLARITY AND SECURITY).

(1) Program

① Program voltage (V_{ihp}) is applied to pin 1 (V_{pp}).
② Program "H" input voltage (V_{ihh}) to pin 5 (FPM).
③ FEATURE CELL is selected with pin 3 (S1) and pin 4 (S2).
(Refer Table 1–5–2)
④ Data corresponding to each output pin are set.
⑤ Program is executed by applying "H" input voltage (V_{ihh}) in width of 1 ms to pin 11 (PGM/$\overline{OE}$) as program pulse. Program mode is executed in accordance with the flow chart (high speed mode) shown on Diagram 1–5–2.

(2) Verify

① Program voltage (V_{ihp}) is applied to pin 1 (V_{pp}).
② Program "H" input voltage (V_{ihh}) is applied to pin 5 (PGM).
③ FEATURE CELL is selected with pin 3 (S1) and pin 4 (S2).
(Refer Table 1–5–2)
④ Verify is accomplished by making pin 11 (PGM/$\overline{OE}$) to "L" input voltage (V_{il}) level.

Note 1) The data during programming are –
"0" : write, "1" : no write

Note 2) Program/Verify of "SECURITY" CELL uses only pin 12 (D0). Once "SECURITY" CELL is programmed, it allows usual logic operation, but does not allow verify of AND Array. If verify of AND Array is executed under this condition, output data turns to LOW.
(Verify of FEATURE CELL is possible)

Table 1–5–1 Mode table (Pin connection and function)

	1	2	3	4	5	6	7	8	9	11	12–19
AND ARREY PROGRAM	HP	A7	A6	A5	A4	A3	A2	A1	A0	HH	DATA INPUT
AND ARREY VERIFY	HP	A7	A6	A5	A4	A3	A2	A1	A0	L	DATA OUTPUT
FEATURE PROGRAM	HP	×	S1	S2	HH	×	×	×	×	HH	DATA INPUT
FEATURE VERIFY	HP	×	S1	S2	HH	×	×	×	×	L	DATA OUTPUT
PRE LOAD	L	×	×	HH	×	×	×	×	×	H	DATA INPUT
LOGIC MODE	ALL INPUTS IS TTL LEVEL										

(Note) HP = V_{IHP} (Series 20B 13.5V)
HH = V_{IHH} (Series 20B 13.5V)
H = V_{IH}
L = V_{IL}
× = Don't care (TTL Level)

Table 1–5–2

S1	S2	FEATURE CELL
0	0	OR
0	1	XOR
1	0	POLARITY
1	1	SECURITY

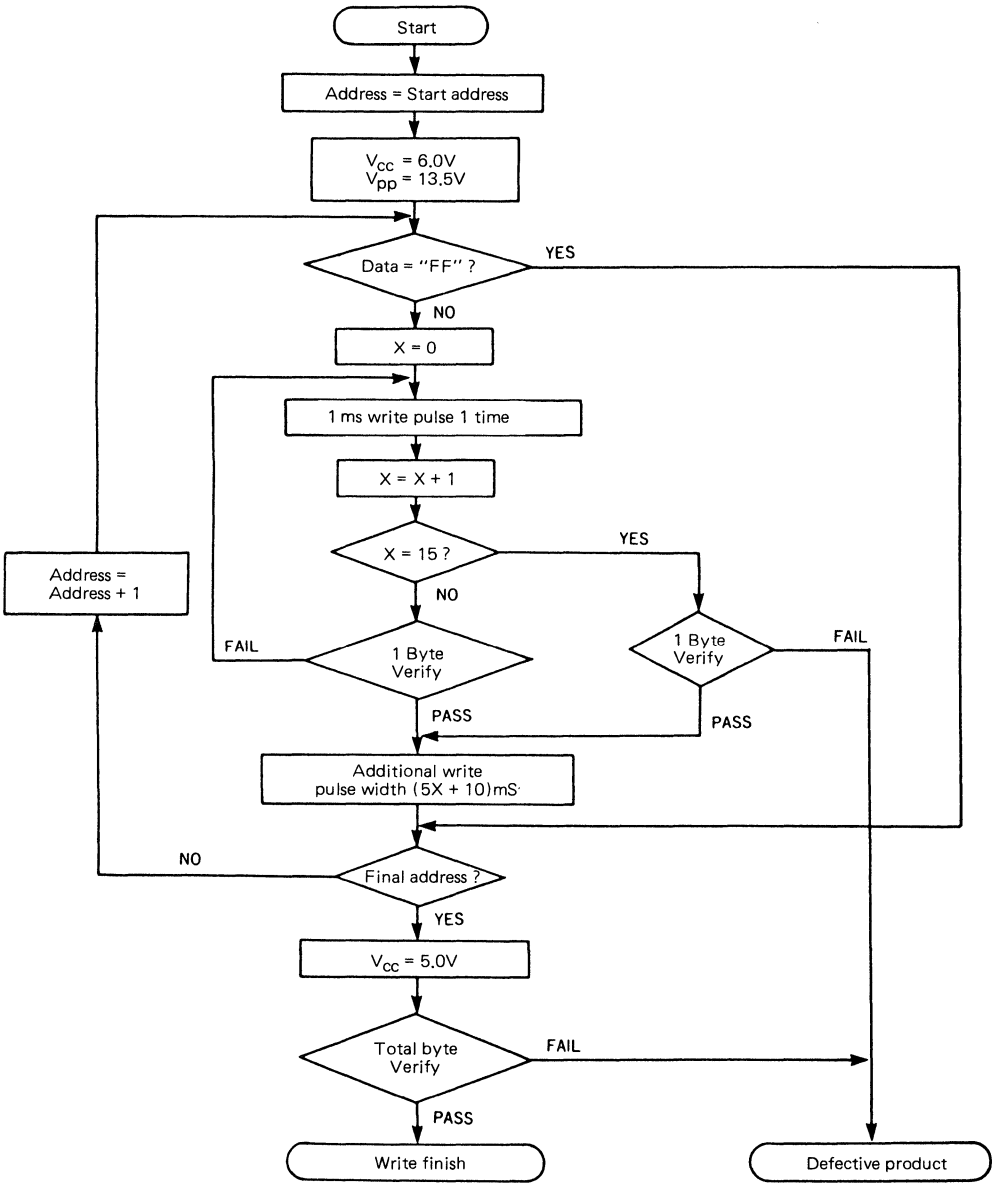


Diagram 1–5–2 High speed program mode flow chart

1 – 5 – 4 Programming characteristics and timing diagram

Programming characteristics

D.C. characteristics ($T_a = 20 \sim 30°C$, $V_{CC} = 6.0 \pm 0.25V$)

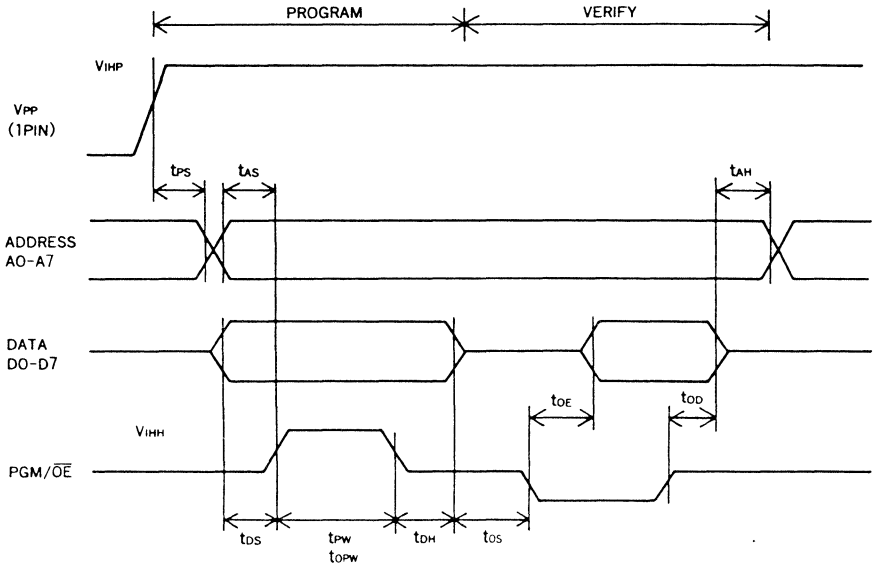
Symbol	Parameters		Conditions	Limits			Unit
				Min.	Typ.	Max.	
I_{LI}	Input leak current		V_I = OV ~ V_{CC}	-20		20	μA
I_{LO}	Output leak current		V_O = OV ~ V_{CC} Chip non-selection	-20		20	μA
V_{IL}	"L" input voltage			-0.3		0.8	V
V_{IH}	"H" input voltage			2.5		V_{CC} + 0.3	V
V_{IHH}	Program "H" input voltage	Series 20B		13.0	13.5	14.0	V
V_{IHP}	Program power supply voltage	Series 20B		13.0	13.5	14.0	V
I_{HH}	V_{IHH} power supply current		PGM/$\overline{OE}$, FPM=V_{IHH}			5	mA
I_{HP}	V_{IHP} power supply current		V_{PP}=V_{IHP}			30	mA
I_{CC}	V_{CC} power supply current					5	mA

A.C. characteristics ($T_a = 20 \sim 30°C$, $V_{CC} = 6.0 \pm 0.25V$)

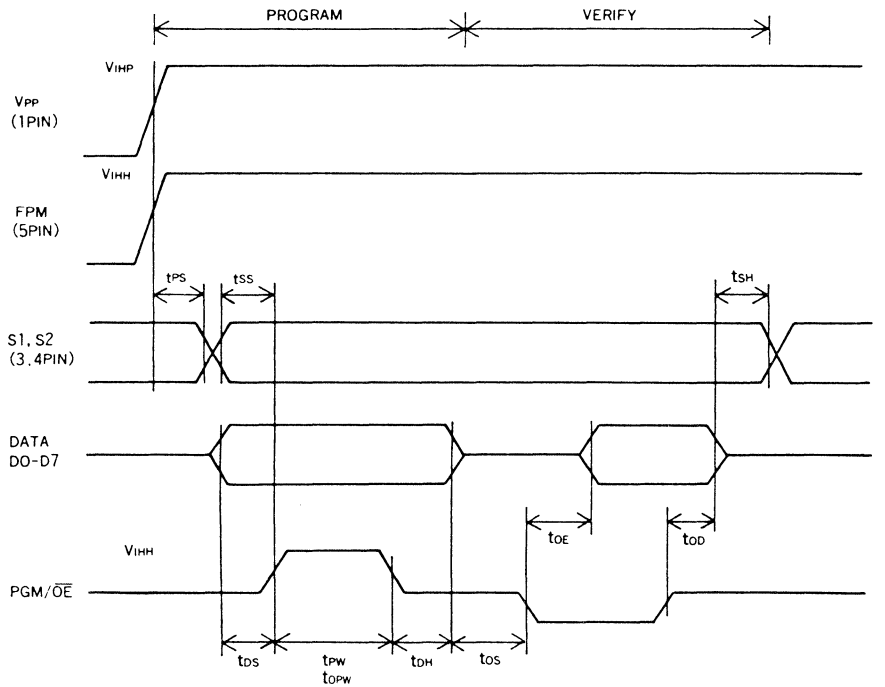
Symbol	Parameters	Min.	Typ.	Max.	Unit
t_{PS}	V_{IHP} setup time	2			μS
t_{AS}	Address setup time	2			μS
t_{DS}	Data setup time	2			μS
t_{PW}	Program pulse width	0.95	1.0	1.05	mS
t_{DH}	Data hold time	2			μS
t_{OS}	$\overline{OE}$ setup time	2			μS
t_{OE}	$\overline{OE}$ access time			2	μS
t_{OD}	Data valid after $\overline{OE}$	0		2	μS
t_{AH}	Address hold time	2			μS
t_{SS}	Select setup time	2			μS
t_{SH}	Select hold time	2			μS
t_{PLW}	Preload pulse width	2			μS
t_{OPW}	Additional program pulse width	14.75		88.75	mS

Timing diagram

1. AND Array Program/Verify



2. FEATURE CELL Program/Verify



1 – 5 – 5 Address table

Address table (Group I)

INPUT LINE No. VS. ADDRESS

INPUT LINE NUMBER	ADDRESS PIN STATE				
	A4	A3	A2	A1	A0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1	1	1	0
31	1	1	1	1	1

Address table (Group II)

INPUT LINE No. VS. ADDRESS

INPUT LINE NUMBER	ADDRESS PIN STATE				
	A4	A3	A2	A1	A0
0	1	1	1	1	1
1	1	1	1	1	0
2	0	0	0	0	1
3	0	0	0	0	0
4	1	1	1	0	1
5	1	1	1	0	0
6	0	0	0	1	1
7	0	0	0	1	0
8	1	1	0	1	1
9	1	1	0	1	0
10	0	0	1	0	1
11	0	0	1	0	0
12	1	1	0	0	1
13	1	1	0	0	0
14	0	0	1	1	1
15	0	0	1	1	0
16	1	0	1	1	1
17	1	0	1	1	0
18	0	1	0	0	1
19	0	1	0	0	0
20	1	0	1	0	1
21	1	0	1	0	0
22	0	1	0	1	1
23	0	1	0	1	0
24	1	0	0	1	1
25	1	0	0	1	0
26	0	1	1	0	1
27	0	1	1	0	0
28	1	0	0	0	1
29	1	0	0	0	0
30	0	1	1	1	1
31	0	1	1	1	0

PRODUCT LINE No. VS. ADDRESS

PRODUCT LINE NUMBER								ADDRESS PIN STATE		
D0	D1	D2	D3	D4	D5	D6	D7	A7	A6	A5
56	48	40	32	24	16	8	0	0	0	0
57	49	41	33	25	17	9	1	0	0	1
58	50	42	34	26	18	10	2	0	1	0
59	51	43	35	27	19	11	3	0	1	1
60	52	44	36	28	20	12	4	1	0	0
61	53	45	37	29	21	13	5	1	0	1
62	54	46	38	30	22	14	6	1	1	0
63	55	47	39	31	23	15	7	1	1	1

PRODUCT LINE No. VS. ADDRESS

PRODUCT LINE NUMBER								ADDRESS PIN STATE		
D0	D1	D2	D3	D4	D5	D6	D7	A7	A6	A5
56	48	40	32	24	16	8	0	0	0	0
57	49	41	33	25	17	9	1	0	0	1
58	50	42	34	26	18	10	2	0	1	0
59	51	43	35	27	19	11	3	0	1	1
60	52	44	36	28	20	12	4	1	0	0
61	53	45	37	29	21	13	5	1	0	1
62	54	46	38	30	22	14	6	1	1	0
63	55	47	39	31	23	15	7	1	1	1

▨ : Unused area

1 – 5 – 6 Preload mode

Since EPL with register attached executes inspection of logic operation including register, it is equipped with preload function of register. With this function, it is possible to load any optional data on the register pin (output pin with register attached: e.g. for EPL16RP6, 6 terminals from pin 13 through pin 18) to the register.

For EPL with register attached, input of AND Array is determined by the signal from input terminal and feedback signal from the register. With preload function and by determining the condition of this feedback signal, it enables to execute initial setting of AND Array and inspection of logic operation.

- Preload

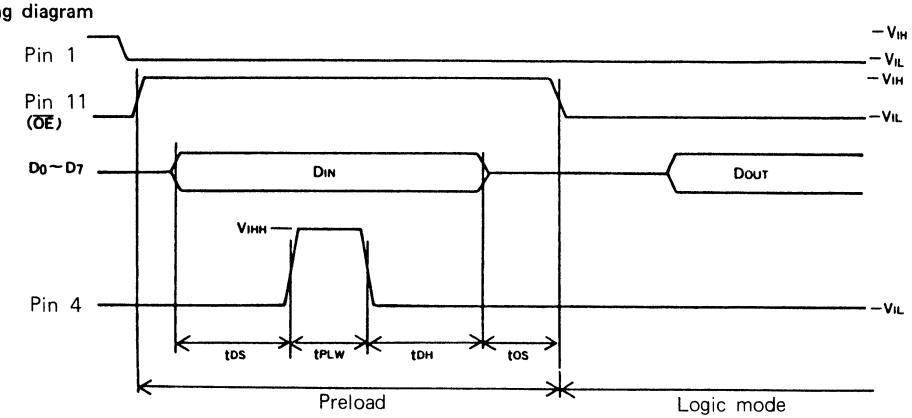
  ① "L" input voltage (V_{il}) is applied to pin 1 (CLK).
  ② "H" input voltage (V_{ih}) is applied to pin 11 ($O\overline{E}$).
  ③ Preload data is set to data pin.
  ④ Preload pulse in width of 2μs of program "H" input voltage is applied to pin 4 (PRELOAD/S2/A5).

  With the above, the data of each pin are preloaded to F/F.

- Read

  It is same as F/F read operation under normal logic mode.

Timing diagram



1 – 6 Upper compatibility of EPL

RICOH's EPL has the upper compatibility with the following grades offered by various manufacturers.

As of June, 1986

	RICOH's EPL 20	Compatible products			
		M M I	N S	A M D	T I
Group I	10P8 B	PAL 10L8 PAL 10H8 PAL 10P8	PAL 10L8 PAL 10H8		
	12P6 B	PAL 12L6 PAL 12H6 PAL 12P6	PAL 12L6 PAL 12H6		
	14P4 B	PAL 14L4 PAL 14H4 PAL 14P4	PAL 14L4 PAL 14H4		
	16P2 B	PAL 16L2 PAL 16H2 PAL 16P2 PAL 16C1	PAL 16L2 PAL 16H2 PAL 16C1		
Group II	16P8 B	PAL 16L8 PAL 16L8A–2 PAL 16P8 PAL 16P8A–2	PAL 16L8	AmPAL 16L8 AmPAL 16H8	PAL 16L8
	16RP8 B	PAL 16RP8 PAL 16RP8A–2 PAL 16R8 PAL 16R8B–4	PAL 16R8	AmPAL 16R8	PAL 16R8
	16RP6 B	PAL 16RP6 PAL 16RP6A–2 PAL 16R6 PAL 16R6B–4	PAL 16R6	AmPAL 16R6	PAL 16R6
	16RP4 B	PAL 16RP4 PAL 16RP4A–2 PAL 16R4 PAL 16R4B–4 PAL 16X4 PAL 16A4	PAL 16R4	AmPAL 16R4	PAL 16R4

MMI ···· Monlithic Memories Inc
NS ····· National Semiconductor
AMD ···· Adovanced Micro Devices
TI ····· Texas Instruments

CHAPTER 2

2 – 1 "EPLASM" design method

When briefly classifying design process using EPL, it is classified in 3 categories of : System design → Logic design → EPL program. (Refer Diagram 2–1–2) As shown on the diagram, there are Top down method and Bottom up method available as the method of preparing Boolean equations.

(1) Top down method

Boolean equation is implemented on the basis of circuit function intended by designer. First of all, if circuit function is sequential, state transition diagram and state transition table are implemented, and if it is combinational circuit, truth table is implemented, and on the basis of which, preparation and simplification of Boolean equations is exercised.

(2) Bottom up method

As well as the gate array, it is implemented on the basis of circuit diagram assembled with TTL and etc. From circuit diagram, determine with the number of input and output as well as with the number of flip-flop as to which kind of EPL will materialize and then, proceed to preparation and simplification of Boolean equations.

Boolean equation thus prepared under the methods of (1) and (2) are converted to product term logical expression, and input file to "EPLASM" is prepared. Input file is prepared, as shown on Diagram 2–1–1.

```
EPL16RP8                        EPL DESIGN SPECIFICATION
PART NUMBER XYZ                 A.T  NOV.20 1984
XOR EXAMPLE
RICOH CO,LTD.                   OSAKA,JAPAN
A B C D E F G H I    GND
J K L M N O P Q R    VCC
O=B:+:C
FUNCTION TABLE
B C O
;     BC O   COMMENT
----------------------
      LL L   XOR
      LH H   XOR
      HL H   XOR
      HH L   XOR
----------------------
DESCRIPTION
  THIS IS AN EXAMPLE OF THE FORMAT OF THE EPL
 DESIGN SPECIFICATION.
END
```

Diagram 2–1–1 Input file

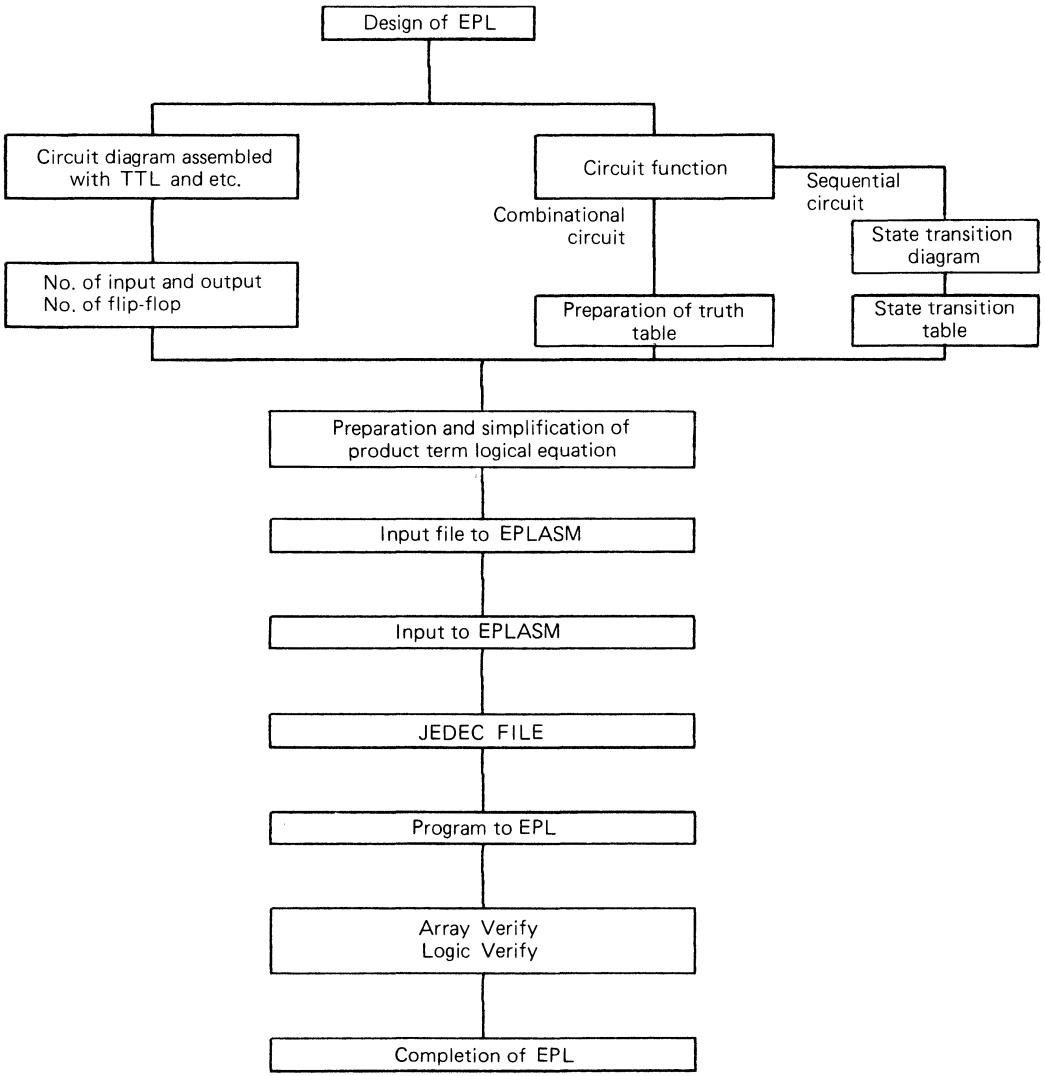


Diagram 2–1–2 EPL design process

1) 1st line

It defines the device to be used.

2) 2nd line

It defines the parts number and the date of preparation within the company of user.

3) 3rd line

It defines the title of application.

4) 4th line

It defines the name and address of the company of user.

5) 5th and 6th lines

They define the names of all 20 pins in the order of Pin 1 through Pin 20. Meanwhile, Pin 10 is named GND and Pin 20 is V_{CC}.

6) 7th line

This line represents Boolean equation. Boolean equation defines logical function, using Boolean equation.

① **Logical operator**

Priority	Operator	Explanation
1	/	NOT (indicated on the head of pin name)
2	*	AND : Product
3	+	OR : Sum
4	: + :	XOR : Exclusive OR, or else

② **Other operators**

Operator	Explanation
( )	3-state condition (Used at IF statement)
=	Assignment without clock (Combinational circuit type)
: =	Assignment with clock attached (Sequential circuit type)

IF (Product) PIN NAME = Expression

It represents the assignment without clock with condition of 3-state. When the logical value of "Product" (Combination of Symbol with AND operator "*") is true, the Boolean equation of righthand side "Expression" (combination of Symbol with logical operator) is assigned to the output defined under lefthand side pin name. If logical value of "Product" is false, high impedance condition is assigned to the output.

7) 8th line

Function table represents the function of device in form of table. It is also used for TEST function of EPLASM.

If there is a difference between the value calculated from Boolean equation and the value of function table, error message comes out as a result of TEST function.

Configuration of Function Table Section is illustrated on Diagram 2−1−3.

```
FUNCTION TABLE                                                    ①
pin list                                                          ②
(; Comment)                                                       ③
------------------------------------------------------------------④
functional vector                                                 ⑤
            .
            .
            .

------------------------------------------------------------------⑥
```

Diagram 2–1–3 Function Table

① It declares the start of Function Table Section.
② PIN LIST
③ Comment line
④ 1st dash line
⑤ This is the vector which expresses the function of device and the 1st line corresponds to the vector.
⑥ 2nd dash line

Symbol	Explanation
L	LOW level
H	HIGH level
X	Uncertain *
C	Rise from 'L' to 'H'
Z	High impedance condition

8) 17th line

This is the part following the Function Table and declared by reserved word "DESCRIPTION". In this part, the operation of device, its application and etc. are described.

9) 20th line

It writes the reserved word "END" at the final of input file.

Note) Function table Section is omissible. Describe all others. In case where the content of description is not required, it is even necessary to describe only reserved word "DESCRIPTION".

Next, the function of EPLASM is described. (Refer Diagram 2–1–4 and Diagram 2–1–5)

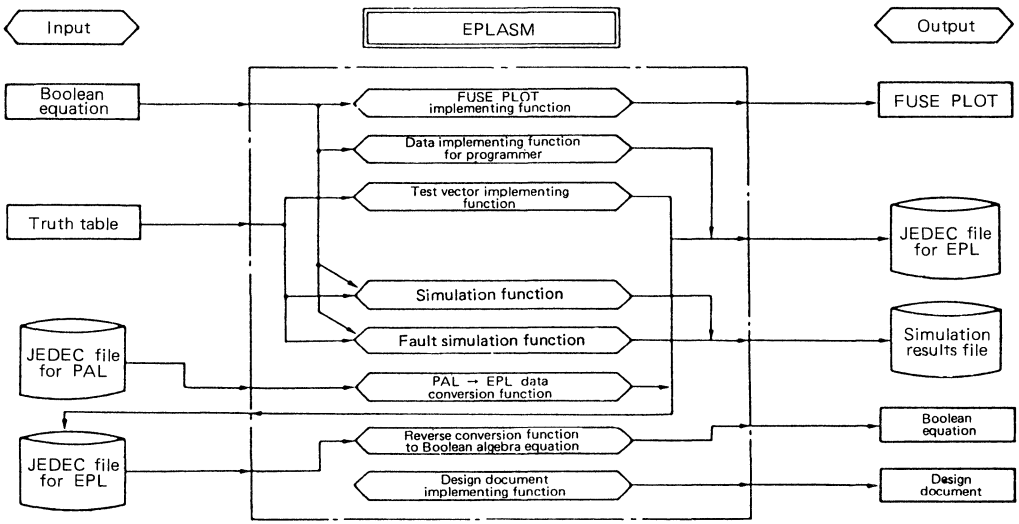


Diagram 2–1–4 Function of EPLASM

```
E=ECHOES EPL DESIGN SPECIFICATION
P=PRINTS THE ENTIRE FUSE PLOT
B=PRINTS ONLY THE USED PRODUCT LINES OF THE FUSE PLOT
J=GENERATES JEDEC PROGRAMMING FORMAT
A=PRINTS ALL NECESSARY OUTPUTS
C=CONVERTS MMI JEDEC FILE TO RICOH JEDEC FILE
M=GENERATES BOOLEAN EQUATIONS FROM AN MMI JEDEC FILE
V=GENERATES BOOLEAN EQUATIONS FROM A RICOH JEDEC FILE
T=SIMULATES FUNCTION TABLE VECTORS IN THE LOGIC EQ.S AND GENERATES TEST VECTORS
F=PERFORMS FAULT TESTING
R=PROCESSES ANOTHER EPL
Q=EXIT EPLASM
```

Diagram 2–1–4 Example of command of "EPLASM"

"EPLASM" will confirm through simulation whether or not there is a contradiction between product sum Boolean equation input by user and truth table, and convert it to "JEDEC FILE" which is readable form of writing device (programmer) to EPL. Also, it implements fuse plot, executes fault test and confirms whether or not the test vector implemented from truth table suffices operation of complete logic test. (Command "F")

In addition to these functions, it has the following functions, i.e., data conversion function from PAL-use to EPL-use (used to convert the data of written PAL to EPL-use, Command "C"), and the function of reverse conversion of data read-out from programmed EPL to Boolean equation (Command "M", "V"). In addition, the input of source file can be implemented either through disc file or direct input by interactive form. Those directly input can be saved as file. Furthermore, the resulted output can be implemented as file form of disc or direct output to CRT. (Execute for command other than "C", "M" and "V". Command "R").

Since "EPLASM" having these functions is written in FORTRAN 77, it allows an easy conversion among different types of machines.

Once "JEDEC FILE" is implemented by EPLASM, it transmits to programmer and programs EPL. Following are the programmer approved by RICOH at present.

EPL programmer list

As of April, 1987

Name of company	Body	Required accessories	Feature
Minato Electronics	Model 1870A Model 1900	7SP−EPL20 0U−193	
DATA I/O	Model 29B Model 60A	LOGICPACK + 303A−009 360A−001V05	
Advantest	TR 4931	TR 49301	Operation possible without personal computer and software thereof is coordinative.
Japan Macnics	PROMAC P3 (Ver 3.0)		
R & D	FLEXY SYPLA III	PALPACK PAL 2040	EPLASM class assembler built-in
AVAL	Packer 10	EX−1	
Hyrel	EPL writer Ver 1.2		
Yashiro Denki	EPL writer 20		

PLD development supporting system and development tool

Name of company	Name of software Name of system	Required accessories	Feature
Yokogawa Hewlett Packard	9000 Series PLD development system	DATA I/O Model 60A/29B	Execution possible from circuit diagram input Automatic logic fragmentation/ optimization up to 5 pcs. possible
RICOH Co., Ltd.	EPLASM	IBM−PC NEC PC 9800 Series	Operation on MS−DOS
DATA I/O	ABEL	IBM−PC NEC PC 9800 Series	Operation on MS−DOS Input from state transition diagram and truth table possible
Japan Macnics Co., Ltd.	CUPL	IBM−PC NEC PC 9800 Series	Operation on MS−DOS Input from state transition diagram and truth table possible

2 – 2 Example of design using "EPLASM"

2 – 2 – 1 Design of 4-Bit-Shift-Register

(1) Relating to circuit function

The example of design of 4-Bit-Shift-Register is shown, which has 4 circuit functions of Shift Right, Shift Left, Load (Load signals of D0 ~ D3) and Hold (maintain the condition as it is) with selective signals S1 and S0. Collected circuit functions are shown on Table 2–2–1.

Selective signal		Circuit function
S1	S0	
0	0	Load
0	1	Shift–Right
1	0	Shift–Left
1	1	Hold

Table 2–2–1 Circuit function

As shown on Table 1–2–2, it enables to materialize sequential circuit since EPL16RP8, 16RP6 and 16RP4 have register and feedback installed. 4-Bit-Shift-Register requires 7 input (Clock pin, selective pin S1, S0, Load pin D3 ~ D0) pins, 4 output (Q0 ~ Q3) pins and input output (Right-In & Left-out, Left-In & Right-Out). Those which satisfy this requirement are EPL16RP6 and 16RP4. Here, design takes place, using EPL16RP6.

(2) Relating to each STATE

Load ($\overline{S1}$ * $\overline{S0}$) means to Load D3, D2, D1 and D0 to each output (Q3, Q2, Q1 and Q0). Shift-Right ($\overline{S1}$ * S0) means to shift right at the next step (next condition with clock attached).

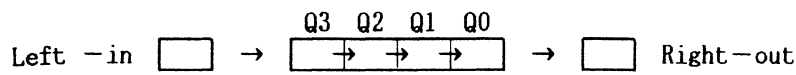


Diagram 2–2–1 Shift-Right

In other words, as shown on Diagram 2–2–2, the signal of Right-in is output to Q3, while the signal of Q0 to Right-out at the next step.

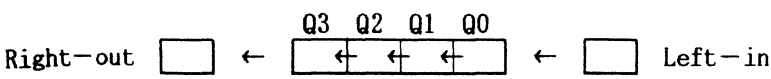


Diagram 2–2–2 Shift-Left

At Hold (S1 * S0), previous condition is output at the next step.

(3) Input file implementation to "EPLASM"

Diagram 2–2–3 shows the architecture of EPL16RP6. As readily seen from the diagram, pin 19 and pin 12 have the archtecture of 3-STATE. Accordingly, these 2 pins are used as input output pin (LIRO: Left-in & Right-out, RILO: Right-in & Left-out).

Also, each output (4 pins within pin 13 ~ pin 18) is Active Low. In the design of this time, Boolean equation (expresses the input of D flip-flop) is expressed by $\overline{Q0}$, $\overline{Q1}$ and $\overline{Q3}$, taking into consideration Active Low. Also, it is always necessary for input to pin 11 to be "L".

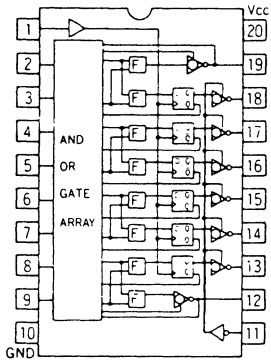


Diagram 2–2–3 Architecture of EPL16RP6

Then, designate each pin as shown on Table 2–2–2.

Pin No	Pin Name	Pin No	Pin Name
1	CK	20	VCC
2	S1	19	LIRO
3	S0	18	NC
4	D3	17	Q0
5	D2	16	Q1
6	D1	15	Q2
7	D0	14	Q3
8	NC	13	NC
9	NC	12	RILO
10	GND	11	OE

Table 2–2–2 EPL16RP6 PIN assignment

Selective signal		Circuit function	Input Output		Output				
S0	S1		LIRO	RILO		Q3	Q2	Q1	Q0	
0	0	Load	×	×		D3	D2	D1	D0	
0	1	Shift−Right	×	1		1	D3	D2	D1	D0
0	1		×	0		0	1	D3	D2	D1
1	0	Shift−Left	1	0	0	1	D3	D2	1	
1	0		0	1	1	D3	D2	1	0	
1	1	Hold	×	×		D3	D2	1	0	

Table 2–2–3 State transition table (×: Uncertain)

Boolean equation is implemented on the basis of Table 2–2–3. Let's think of output Q3.

Load	$(\overline{S1} * \overline{S0})$	$\overline{Q3} := \overline{S1} * \overline{S0} * \overline{D3}$ (D3 turns to input of D–FF)
Shift–Right	$(\overline{S1} * S0)$	$\overline{Q3} := \overline{S1} * S0 * \overline{RILO}$ (Right-in turns to input of D–FF)
Shift–Left	$(S1 * \overline{S0})$	$\overline{Q3} := S1 * \overline{S0} * \overline{Q2}$ (Q2 turns to input of D–FF)
Hold	$(S1 * S0)$	$\overline{Q3} := S1 * S0 * \overline{Q3}$ (Q3 turns to input of D–FF)

As well, when thinking of $\overline{Q2}$, $\overline{Q1}$ and $\overline{Q0}$, they are as follows.

$$\overline{Q3} := \overline{S1} * \overline{S0} * \overline{D3} + S1 * \overline{S0} * \overline{RILO} + S1 * \overline{S0} * \overline{Q2} + S1 * S0 * \overline{Q3}$$

$$\overline{Q2} := \overline{S1} * \overline{S0} * \overline{D2} + S1 * \overline{S0} * \overline{Q3} + S1 * \overline{S0} * \overline{Q1} + S1 * S0 * \overline{Q2}$$

$$\overline{Q1} := \overline{S1} * \overline{S0} * \overline{D1} + S1 * \overline{S0} * \overline{Q2} + S1 * \overline{S0} * \overline{Q0} + S1 * S0 * \overline{Q1}$$

$$\overline{Q0} := \overline{S1} * \overline{S0} * \overline{D0} + S1 * \overline{S0} * \overline{Q1} + S1 * \overline{S0} * \overline{LIRO} + S1 * S0 * \overline{Q0}$$

With regards to 2 input output pins of RILO and LIRO, RILO is used as input pin, while LIRO as output pin at the time of Shift-Right. Accordingly, RILO is turned to high impedance condition (Z). When Shift-Left, LIRO is turned to high impedance condition. Above will represent as follows in case of input file to "EPLASM".

```
IF (/S1 * S0) /LIRO = /Q0
IF (S1 * /S0) /RILO = /Q3
```

If Boolean equation of IF statement in the next parenthesis is false, it indicates that high impedance condition is allocated to the output. If Boolean equation in parenthesis is true, it indicates that Boolean equation of right side is allocated to the output specified under the next pin name.

	INPUT				OUTPUT					
	S1	S0	R·in	L·in	Q3	Q2	Q1	Q0	R·out	L·out
Load	0	0	×	×	0	0	0	0	Z	Z
Shift—Right	0	1	1	0	1	0	0	0	0	Z
	0	1	0	×	0	1	0	0	0	Z
	0	1	0	×	0	0	1	0	0	Z
	0	1	0	×	0	0	0	1	0	Z
	0	1	0	×	0	0	0	0	1	Z
Shift—Left	1	0	×	0	0	0	0	1	Z	0
	1	0	×	0	0	0	1	0	Z	0
	1	0	×	0	0	1	0	0	Z	0
	1	0	×	0	1	0	0	0	Z	0
	1	0	×	0	0	0	0	0	Z	0
Hold	1	1	×	×	0	0	0	0	Z	Z

Table 2–2–4 Truth table of 4-Bit-Shift-Register

(X : Uncertain, Z : High impedance, R·in : Right-in, L·in : Left-in, R·out : Right-out, L·out : Left-out)

As mentioned heretofore, the configuration of 4-Bit-Shift-Register is as shown on Diagram 2–2–4

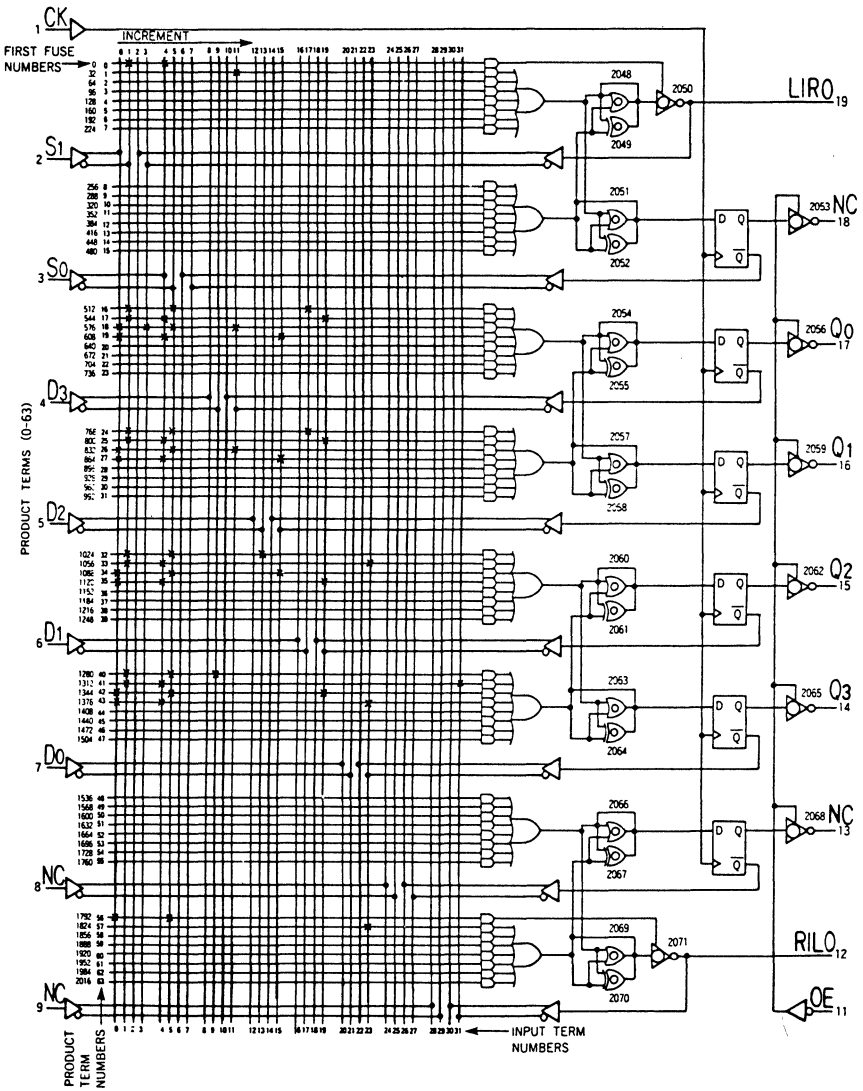


Diagram 2–2–4 Configuration of 4-Bit-Shift-Register

Input file to EPL support software "EPLASM" is shown on Diagram 2–2–5.

```
EPL16RP6                          DESIGN SPECIFICATION
S.R                               A.T JUR.18 1985
SHIFT REGISTER
RICOH CO,LTD.                     OSAKA,JAPAN
CK  S1 S0 D3 D2 D1 D0 NC NC GND
OE RILO NC Q3 Q2 Q1 Q0 NC LIRO VCC
/Q3  :=/S1*/S0*/D3     +
       /S1*S0*/RILO    +
        S1*/S0*/Q2     +
        S1*S0*/Q3
/Q2  :=/S1*/S0*/D2     +
       /S1*S0*/Q3      +
        S1*/S0*/Q1     +
        S1*S0*/Q2
/Q1  :=/S1*/S0*/D1     +
       /S1*S0*/Q2      +
        S1*/S0*/Q0     +
        S1*S0*/Q1
/Q0  :=/S1*/S0*/D0     +
       /S1*S0*/Q1      +
        S1*/LIRO*/S0   +
        S1*S0*/Q0
IF(/S1*S0)/LIRO=/Q0
IF(S1*/S0)/RILO=/Q3
FUNCTION TABLE
CK  S1 S0 D3 D2 D1 D0 OE      RILO  LIRO    Q3 Q2 Q1 Q0
-----------------------------------------------------------
;LOAD
C   L  L  L  L  L  L  L       Z     Z       L  L  L  L
C   H  H  X  X  X  X  L       Z     Z       L  L  L  L
;SHIFT RIGHT
C   L  H  X  X  X  X  L       H     L       H  L  L  L
C   L  H  X  X  X  X  L       L     L       L  H  L  L
C   L  H  X  X  X  X  L       L     L       L  L  H  L
C   L  H  X  X  X  X  L       L     H       L  L  L  H
C   L  H  X  X  X  X  L       L     L       L  L  L  L
;SHIFT LEFT
C   H  L  X  X  X  X  L       L     H       L  L  L  H
C   H  L  X  X  X  X  L       L     L       L  L  H  L
C   H  L  X  X  X  X  L       L     L       L  H  L  L
C   H  L  X  X  X  X  L       H     L       H  L  L  L
C   H  L  X  X  X  X  L       L     L       L  L  L  L
;HOLD
C   H  H  X  X  X  X  L       Z     Z       L  L  L  L
-----------------------------------------------------------
DESCRIPTION
 THIS EXAPLE ILLUTRATES THE USE OF EPL TO IMPLEMENT THE SHIFT REGISTER.
END
```

Diagram 2–2–5 Input file to "EPLASM"

"JEDEC FILE" which is the execution result of "EPLASM" is shown on Diagram 2–2–6.

```
EPL16RP6                          DESIGN SPECIFICATION
S.R                               A.T JUR.18 1985
SHIFT REGISTER
RICOH CO,LTD.                     OSAKA,JAPAN
*F0*
L0000 1011 0111 1111 1111 1111 1111 1111 1111 *
L0032 1111 1111 1110 1111 1111 1111 1111 1111 *
L0512 1011 1011 1111 1111 1111 1011 1111 1111 *
L0544 1011 0111 1111 1110 1111 1111 1111 1111 *
L0576 0110 1011 1111 1111 1111 1111 1111 1111 *
L0608 0111 0111 1110 1111 1111 1111 1111 1111 *
L0768 1011 1011 1111 1111 1011 1111 1111 1111 *
L0800 1011 0111 1111 1111 1110 1111 1111 1111 *
L0832 0111 1011 1110 1111 1111 1111 1111 1111 *
L0864 0111 0111 1111 1110 1111 1111 1111 1111 *
L1024 1011 1011 1111 1011 1111 1111 1111 1111 *
L1056 1011 0111 1111 1111 1111 1110 1111 1111 *
L1088 0111 1011 1111 1110 1111 1111 1111 1111 *
L1120 0111 0111 1111 1111 1110 1111 1111 1111 *
L1280 1011 1011 1011 1111 1111 1111 1111 1111 *
L1312 1011 0111 1111 1111 1111 1111 1111 1110 *
L1344 0111 1011 1111 1111 1110 1111 1111 1111 *
L1376 0111 0111 1111 1111 1111 1110 1111 1111 *
L1792 0111 1011 1111 1111 1111 1111 1111 1111 *
L1824 1111 1111 1111 1111 1111 1110 1111 1111 *
L2048 000  000  000  000  000  000  000  000  *
C49E9*
V0001 C000000XXN0ZXLLLLXZN *
V0002 C11XXXXXXN0ZXLLLLXZN *
V0003 C01XXXXXXN01XHLLLXLN *
V0004 C01XXXXXXN00XLHLLXLN *
V0005 C01XXXXXXN00XLLHLXLN *
V0006 C01XXXXXXN00XLLLHXHN *
V0007 C01XXXXXXN00XLLLLXLN *
V0008 C10XXXXXXN0LXLLLHX1N *
V0009 C10XXXXXXN0LXLLHLX0N *
V0010 C10XXXXXXN0LXLHLLX0N *
V0011 C10XXXXXXN0HXHLLLX0N *
V0012 C10XXXXXXN0LXLLLLX0N *
V0013 C11XXXXXXN0ZXLLLLXZN *
35AE
```

Diagram 2–2–6 "JEDEC FILE"

"JEDEC FILE" records the fuse information (information giving which fuse to write) and test vector for logic test. For fuse information, for example, L0032 represents the 32nd fuse, followed by 33, 34 to the right and it is readily seen that it comes to 0 at the 43rd. "1" represents write and "0" represents no write.

Test vector represents the truth table. It indicates pin 1 ~ pin 20 from the left. C represents the rise (from L to H) of Clock, N for V_{CC} (+5V) and GND (Ground) and Z for high impedance condition. Logic verify is executed on the basis of this test vector. That is, to examine if actually written EPL agrees with logic of test vector.

Diagram 2–2–7 graphically shows which fuse to write on the basis of input file.

SHIFT REGISTER

```
:OUT:FUNC:LINE:              11 1111 1111 2222 2222 2233
:PUT:TION: NO  : 0123 4567 8901 2345 6789 0123 4567 8901

:/19: IF :  0 : -X-- X--- ---- ---- ---- ---- ---- ---- /S1*S0
:/19:    :  1 : ---- ---- ---X ---- ---- ---- ---- ---- /Q0
:    :   :  2 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   :  3 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   :  4 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   :  5 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   :  6 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   :  7 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:    :   :  8 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   :  9 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 10 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 11 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 12 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 13 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 14 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 15 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:/17:    : 16 : -X-- -X-- ---- ---- ---- -X-- ---- ---- /S1*/S0*/D0
:/17:  + : 17 : -X-- X--- ---- ---X ---- ---- ---- ---- /S1*S0*/Q1
:/17:  + : 18 : X--X -X-- ---- ---- ---- ---- ---- ---- S1*/LIR0*/S0
:/17:  + : 19 : X--- X--- ---X ---- ---- ---- ---- ---- S1*S0*/Q0
:    :   : 20 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 21 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 22 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 23 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:/16:    : 24 : -X-- -X-- ---- ---- -X-- ---- ---- ---- /S1*/S0*/D1
:/16:  + : 25 : -X-- X--- ---- ---- ---X ---- ---- ---- /S1*S0*/Q2
:/16:  + : 26 : X--- -X-- ---X ---- ---- ---- ---- ---- S1*/S0*/Q0
:/16:  + : 27 : X--- X--- ---- ---X ---- ---- ---- ---- S1*S0*/Q1
:    :   : 28 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 29 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 30 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 31 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:/15:    : 32 : -X-- -X-- ---- -X-- ---- ---- ---- ---- /S1*/S0*/D2
:/15:  + : 33 : -X-- X--- ---- ---- ---- ---X ---- ---- /S1*S0*/Q3
:/15:  + : 34 : X--- -X-- ---- ---X ---- ---- ---- ---- S1*/S0*/Q1
:/15:  + : 35 : X--- X--- ---- ---- ---X ---- ---- ---- S1*S0*/Q2
:    :   : 36 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 37 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 38 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 39 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:/14:    : 40 : -X-- -X-- -X-- ---- ---- ---- ---- ---- /S1*/S0*/D3
:/14:  + : 41 : -X-- X--- ---- ---- ---- ---- ---- ---X /S1*S0*/RILO
:/14:  + : 42 : X--- -X-- ---- ---- ---X ---- ---- ---- S1*/S0*/Q2
:/14:  + : 43 : X--- X--- ---- ---- ---- ---X ---- ---- S1*S0*/Q3
:    :   : 44 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 45 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 46 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 47 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:    :   : 48 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 49 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 50 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 51 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 52 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 53 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 54 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 55 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:/12: IF : 56 : X--- -X-- ---- ---- ---- ---- ---- ---- S1*/S0
:/12:    : 57 : ---- ---- ---- ---- ---- ---X ---- ---- /Q3
:    :   : 58 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 59 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 60 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 61 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 62 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :   : 63 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```

Diagram 2–2–7 FUSE PLOT

Also, "X" represents the fuse with no write, while "−" for fuse with write. Boolean equation on the right represents the Boolean equation of Q0 ~ Q3. For example, LINE NO 16 represents the product term of $\overline{S1} * \overline{S0} * \overline{D0}$. OUTPUT represents the line of product term to connect with which output pin. "1" of pin NO represents that output is Active Low. "+" of FUNCTION represents OR logic, "IF" for output condition term of 3-State.

2 – 2 – 2 Example of application of incorporating logic circuit diagram into EPL

Example of design of incorporating circuit diagram of 10 inputs 2 outputs shown on Diagram 2–2–26 is illustrated.

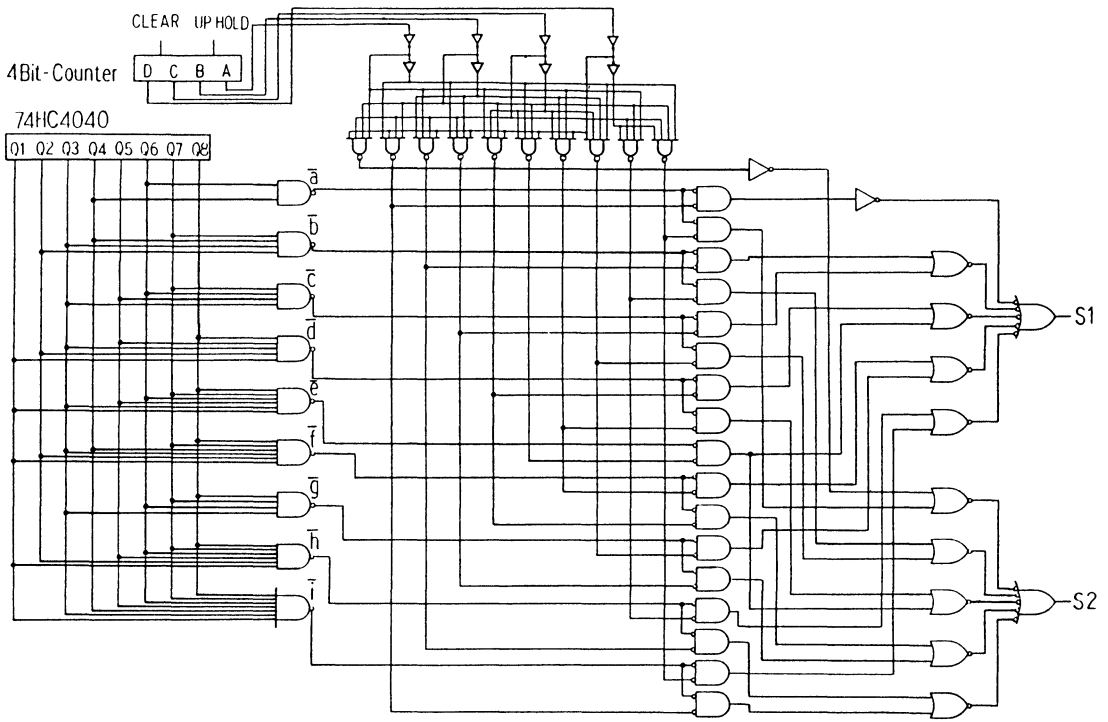


Diagram 2–2–26 10 input 2 output circuit diagram

(1) Outline of circuit

The output shown on Diagram 2–2–26 is 10 output of Clear, Count up, Hold signal of Q1 ~ Q8, 4-Bit-Counter which is the output of TTL 74HC4040. Also, the output is 2 outputs of S 1 and S 2. The output A, B, C and D represent the input of TTL 74HC42 (Refer Diagram 2–2–27). The output Y0 ~ Y9 of TTL 74HC42 and the output of NAND gate of input Q1 ~ Q8 represent the input of NOR gate and output to S 1 and S 2.

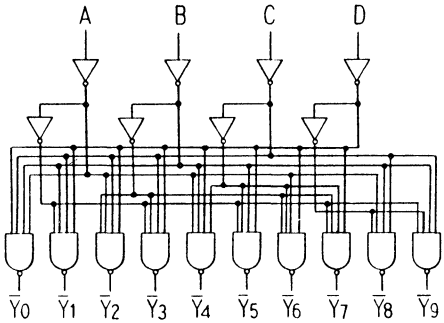


Diagram 2–2–27 TTL 74HC42

Since the circuit of 4-Bit-Counter must be configurated, D flip flop is necessary. As input pin, a total 11 pins consisting of Clock, Q1～Q8, Clear, Count or Hold of Counter is necessary. The ELP that satisfies this requirement is EPL16RP4. Also, since 11 input pins are required, 12 pins of EPL16RP4 and 18 pins of input output pin are used as input pin. (The use of 3-State inverter offers possibility of materialization Refer Diagram 2–2–15)
Next, each pin designation of EPL16RP4 is shown on Table 2–2–9.

Pin No	Pin Name	Pin No	Pin Name
1	CLK (Clock)	20	VCC (+5V)
2	Q1	19	S1
3	Q2	18	CLR (Counter, clear In)
4	Q3	17	A
5	Q4	16	B (4−Bit−Counterの
6	Q5	15	C Output)
7	Q6	14	D
8	Q7	13	S2
9	Q8	12	CNT (Counter, Up, Hold In)
10	GND (Ground)	11	OE

Table 2–2–9 Each pin designation of EPL16RP4

(2) Implementation of product sum Boolean equation

To implement product sum Boolean equation relating to output S1 and S2, first of all, the output of TTL 74HC42 by output A, B, C and D of 4-Bit-Counter is shown on Table 2–2–10. Also, from the circuit diagram of Diagram 2–2–26, the output Q1～Q8 of TTL 74HC4040 represents the input of 9 pieces of NAND gate (a～i) and the output of TTL 74HC42 is also configurated with NAND gate. The output of this a～i and the output Y1～Y9 of TTL 74HC42 represent the input of NOR gate. Accordingly, NAND gate and NOR gate are assumed as AND gate. (Refer Diagram 2–2–28). As well, NOR gate is assumed to output to S1 and S2 as OR gate.

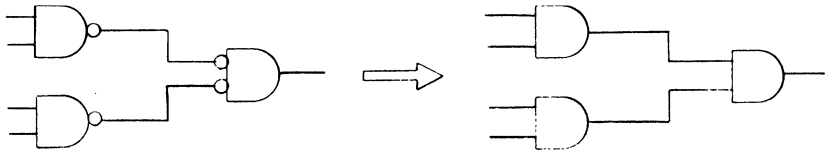


Diagram 2–2–28 Logic conversion

	INPUT				OUTPUT									
STATE	D	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1	1	1
2	0	0	1	0	1	1	0	1	1	1	1	1	1	1
3	0	0	1	1	1	1	1	0	1	1	1	1	1	1
4	0	1	0	0	1	1	1	1	0	1	1	1	1	1
5	0	1	0	1	1	1	1	1	1	0	1	1	1	1
6	0	1	1	0	1	1	1	1	1	1	0	1	1	1
7	0	1	1	1	1	1	1	1	1	1	1	0	1	1
8	1	0	0	0	1	1	1	1	1	1	1	1	0	1
9	1	0	0	1	1	1	1	1	1	1	1	1	1	0
10	1	0	1	0	1	1	1	1	1	1	1	1	1	1
11	1	0	1	1	1	1	1	1	1	1	1	1	1	1
12	1	1	0	0	1	1	1	1	1	1	1	1	1	1
13	1	1	0	1	1	1	1	1	1	1	1	1	1	1
14	1	1	1	0	1	1	1	1	1	1	1	1	1	1
15	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 2–2–10 Output results of TTL 74HC42

As mentioned heretofore, the output results of TTL 74HC42 are described as follows.

$$Y0 = \overline{A} * \overline{B} * \overline{C} * \overline{D}$$
$$Y1 = A * \overline{B} * \overline{C} * \overline{D}$$
$$Y2 = \overline{A} * B * \overline{C} * \overline{D}$$
$$Y3 = A * B * \overline{C} * \overline{D}$$
$$Y4 = \overline{A} * \overline{B} * C * \overline{D}$$
$$Y5 = A * \overline{B} * C * \overline{D}$$
$$Y6 = \overline{A} * B * C * \overline{D}$$
$$Y7 = A * B * C * \overline{D}$$
$$Y8 = \overline{A} * \overline{B} * \overline{C} * D$$
$$Y9 = A * \overline{B} * \overline{C} * D$$

a ~ i, using circuit input of Q1 ~ Q8, are described as follows.

$$
\begin{aligned}
a &= Q4 * Q6 \\
b &= Q2 * Q3 * Q4 * Q7 \\
c &= Q3 * Q5 * Q6 * Q7 \\
d &= Q1 * Q2 * Q3 * Q5 * Q8 \\
e &= Q1 * Q3 * Q5 * Q6 * Q8 \\
f &= Q1 * Q2 * Q3 * Q4 * Q7 * Q8 \\
g &= Q3 * Q6 * Q7 * Q8 \\
h &= Q1 * Q2 * Q5 * Q6 * Q7 * Q8 \\
i &= Q1 * Q3 * Q4 * Q5 * Q6 * Q7 * Q8
\end{aligned}
$$

Hence, product sum Boolean equation relating to the output S1 and S2 are described as follows.

$$
\begin{aligned}
S1 = {} & Q4 * Q6 * A * \overline{B} * \overline{C} * \overline{D} \\
& + Q2 * Q3 * Q4 * Q7 * \overline{A} * B * \overline{C} * \overline{D} \\
& + Q3 * Q5 * Q6 * Q7 * A * \overline{B} * \overline{C} * \overline{D} \\
& + Q1 * Q2 * Q3 * Q5 * Q8 * \overline{A} * \overline{B} * C * \overline{D} \\
& + Q1 * Q3 * Q5 * Q6 * Q8 * A * \overline{B} * C * \overline{D} \\
& + Q1 * Q2 * Q3 * Q4 * Q7 * Q8 * \overline{A} * B * C * \overline{D} \\
& + Q3 * Q6 * Q7 * Q8 * A * B * \overline{C} * \overline{D} \\
& + Q1 * Q2 * Q5 * Q6 * Q7 * Q8 * \overline{A} * \overline{B} * \overline{C} * D \\
& + Q1 * Q3 * Q4 * Q5 * Q6 * Q7 * Q8 * A * \overline{B} * \overline{C} * D
\end{aligned}
$$

$$
\begin{aligned}
S2 = {} & \overline{A} * \overline{B} * \overline{C} * \overline{D} \\
& + Q4 * Q6 * A * \overline{B} * \overline{C} * D \\
& + Q2 * Q3 * Q4 * Q7 * \overline{A} * B * \overline{C} * D \\
& + Q3 * Q5 * Q6 * Q7 * A * \overline{B} * C * \overline{D} \\
& + Q1 * Q2 * Q3 * Q5 * Q8 * \overline{A} * B * C * \overline{D} \\
& + Q1 * Q3 * Q5 * Q6 * Q8 * A * \overline{B} * \overline{C} * \overline{D} \\
& + Q1 * Q2 * Q3 * Q4 * Q7 * Q8 * \overline{A} * \overline{B} * C * D \\
& + Q3 * Q6 * Q7 * Q8 * A * B * \overline{C} * \overline{D} \\
& + Q1 * Q2 * Q5 * Q6 * Q7 * Q8 * \overline{A} * B * \overline{C} * \overline{D} \\
& + Q1 * Q3 * Q4 * Q5 * Q6 * Q7 * Q8 * A * \overline{B} * \overline{C} * \overline{D}
\end{aligned}
$$

(3) Input file to truth table and "EPLASM"

Truth table implemented on the basis of product sum Boolean equation derived from (2) is illustrated on Table 2–2–11.

Counter of State	Counter Input		Counter Output				Input of Circuit (TTL74HC42)								Output of Circuit	
	CLR	CNT	D	C	B	A	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	S1	S2
Clear	1	×	0	0	0	0	×	×	×	×	×	×	×	×	×	×
Hold	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Count up	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1
	0	1	0	0	1	1	0	0	1	0	1	1	1	1	1	1
	0	1	0	1	0	0	1	1	1	1	1	0	1	1	1	1
	0	1	0	1	0	1	1	0	1	0	1	1	0	1	1	1
	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1
	0	1	0	1	1	1	0	0	1	0	1	1	1	1	1	1
	0	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
	0	1	1	0	0	1	1	0	1	1	1	1	1	1	1	1
	0	1	1	0	1	0	1	1	1	1	1	1	1	1	0	0
	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
	0	1	1	1	0	0	1	1	1	1	1	1	1	1	0	0
	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	0	1	1	1	1	0	1	1	1	1	1	1	1	1	0	0
	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	1
Hold	0	0	0	0	0	0	×	×	×	×	×	×	×	×	×	×

Table 2–2–11 Truth table (× Uncertain)

Input file to "EPLASM" is shown on Diagram 2–2–29.

```
EPL16RP4                    EPL DESIGN SPECIFICATION
EX.UP                       M.B. 8/2/1985
EXAMPLE LOGIC
RICOH CO,LTD                OSAKA,JAPAN


;PIN NAME TYPE     DESCRIPTION

 CLK ;  1  IN      SYSTEM CLOCK
  Q1 ;  2  IN      INPUT DATA
  Q2 ;  3  IN      INPUT DATA
  Q3 ;  4  IN      INPUT DATA
  Q4 ;  5  IN      INPUT DATA
  Q5 ;  6  IN      INPUT DATA
  Q6 ;  7  IN      INPUT DATA
  Q7 ;  8  IN      INPUT DATA
  Q8 ;  9  IN      INPUT DATA
 GND ; 10          GROUND
 /EN ; 11  IN      ENABLE COUNTER OUTPUTS (ACTIVE LOW)
 CNT ; 12  IN      COUNTER (UP AND HOLD)
  S2 ; 13  OUT     LOGIC OUTPUT
   A ; 14  OUT     COUNTER OUTPUT
   B ; 15  OUT     COUNTER OUTPUT
   C ; 16  OUT     COUNTER OUTPUT
   D ; 17  OUT     COUNTER OUTPUT
 CLR ; 18  IN      CLEARS COUNTER
  S1 ; 19  OUT     LOGIC OUTPUT
 VCC ; 20          +5 VOLTS

;
; 4-BIT UP  COUNTER
;
 /A  :=      CLR
      + CNT*/CLR*A
      +/CNT*/CLR*/A

 /B  :=      CLR
      + CNT*/CLR* A* B
      + CNT*/CLR*/A*/B
      +/CNT*/CLR*   /B

 /C  :=      CLR
      + CNT*/CLR*/A*   /C
      + CNT*/CLR*   /B*/C
      + CNT*/CLR* A* B* C
      +/CNT*/CLR*      /C

 /D  :=      CLR
     + CNT*/CLR*/A*      /D
     + CNT*/CLR*   /B*   /D
     + CNT*/CLR* A* B*/C*/D
     + CNT*/CLR* A* B* C* D
     +/CNT*/CLR*         /D

;
;LOGIC OUTPUT S1,S2
;

IF (GND) CLR =Q1*Q2*Q5*Q6*Q7*Q8*/A*/B*/C*D
             +Q1*Q3*Q4*Q5*Q6*Q7*Q8*A*/B*/C*D

IF (VCC)  S1   =          Q4*   Q6*        A*/B*/C*/D
               +   Q2*Q3*Q4*       Q7*    /A* B*/C*/D
               +       Q3*   Q5*Q6*Q7*     A* B*/C*/D
               +Q1*Q2*Q3*   Q5*       Q8*/A*/B* C*/D
               +Q1*   Q3*   Q5*Q6*   Q8* A*/B* C*/D
               +Q1*Q2*Q3*Q4*       Q7*Q8*/A* B* C*/D
               +       Q3*       Q6*Q7*Q8* A* B* C*/D
               +Q1*Q2*       Q5*Q6*Q7*Q8*/A*/B*/C* D
               +Q1*   Q3*Q4*Q5*Q6*Q7*Q8* A*/B*/C* D
```

```
IF (GND) CNT =Q3*Q6*Q7*Q8*A*B*/C*/D
             +Q1*Q2*Q5*Q6*Q7*Q8*/A*B*/C*/D
             +Q1*Q3*Q4*Q5*Q6*Q7*Q8*A*/B*/C*/D

IF (VCC)  S2   =                          /A*/B*/C*/D
               +          Q4*    Q6*       A*/B*/C*  D
               +    Q2*Q3*Q4*       Q7*    /A*/B*/C*  D
               +       Q3*    Q5*Q6*Q7*     A*  B*  C*/D
               +Q1*Q2*Q3*    Q5*       Q8*/A*  B*  C*/D
               +Q1*    Q3*    Q5*Q6*    Q8*  A*/B*  C*/D
               +Q1*Q2*Q3*Q4*       Q7*Q8*/A*/B*  C*/D
               +       Q3*       Q6*Q7*Q8*  A*  B*/C*/D
               +Q1*Q2*       Q5*Q6*Q7*Q8*/A*  B*/C*/D
               +Q1*    Q3*Q4*Q5*Q6*Q7*Q8*  A*/B*/C*/D

FUNCTION TABLE

;FUNCTION TABLE PIN LISTS
CLK CLR CNT D C B A Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 S1 S2

;:--- COUNTER --------!-----INPUT DATA ---------: OUTPUTS
;CLK CLR CNT D C B A    Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8   S1 S2
-------------------------------------------------------------
;TEST CLEAR
 C   H   X  L L L L    X  X  X  X  X  X  X  X    X  X
 C   L   L  L L L L    L  L  L  L  L  L  L  L    L  H
;
;COUNT UP
;
 C   L   H  L L L H    H  H  H  H  H  H  H  H    H  H
 C   L   H  L L H L    H  H  H  H  H  H  H  H    H  H
 C   L   H  L L H H    L  L  H  L  H  H  H  H    H  H
 C   L   H  L H L L    H  H  H  H  H  L  H  H    H  H
 C   L   H  L H L H    H  L  H  L  H  H  L  H    H  H
 C   L   H  L H H L    H  H  H  H  H  H  H  H    H  H
 C   L   H  L H H H    L  L  H  L  H  H  H  H    H  H
 C   L   H  H L L L    H  H  H  H  H  H  H  H    H  H
 C   L   H  H L L H    H  L  H  H  H  H  H  H    H  H
 C   L   H  H L H L    H  H  H  H  H  H  H  H    L  L
 C   L   H  H L H H    L  L  L  L  L  L  L  L    L  L
 C   L   H  H H L L    H  H  H  H  H  H  H  H    L  L
 C   L   H  H H L H    L  L  L  L  L  L  L  L    L  L
 C   L   H  H H H L    H  H  H  H  H  H  H  H    L  L
 C   L   H  H H H H    L  L  L  L  L  L  L  L    L  L
 C   L   H  L L L L    H  H  H  H  H  H  H  H    L  H
;
;HOLD
;
 C   L   L  L L L L    X  X  X  X  X  X  X  X    X  X
-------------------------------------------------------------
DESCRIPTION
END
```

Diagram 2–2–29 Input file to "EPLASM"

(4) Relating to execution results of "EPLASM" and fault testing "JEDEC FILE", which is the execution results, is shown on Diagram 2–2–30.

```
EPL16RP4                    EPL DESIGN SPECIFICATION
EX.UP                       M.B. 8/2/1985
EXAMPLE LOGIC
RICOH CO,LTD                OSAKA,JAPAN
*F0*
L0000 1111 1111 1111 1111 1111 1111 1111 1111 *
L0032 1111 1111 1110 0110 1110 0101 1111 1111 *
L0064 1111 0111 0110 0110 1101 1110 0111 1111 *
L0096 1111 1111 0110 1110 0101 0101 0111 1111 *
L0128 0111 0111 0110 1101 0110 1110 1111 0111 *
L0160 0111 1111 0110 1101 0110 0101 1111 0111 *
L0192 0111 0111 0110 0101 1101 1110 0111 0111 *
L0224 1111 1111 0110 1101 1101 0101 0111 0111 *
L0288 0111 0111 1101 1110 0110 0110 0111 0111 *
L0320 0111 1111 0101 0110 0110 0101 0111 0111 *
L0512 1111 1101 1111 1111 1111 1111 1111 1111 *
L0544 1111 1110 1110 1111 1111 1110 1111 1101 *
L0576 1111 1110 1110 1111 1110 1111 1111 1101 *
L0608 1111 1110 1110 1110 1101 1101 1111 1101 *
L0640 1111 1110 1101 1101 1101 1101 1111 1101 *
L0672 1111 1110 1110 1111 1111 1111 1111 1110 *
L0768 1111 1101 1111 1111 1111 1111 1111 1111 *
L0800 1111 1110 1111 1110 1111 1110 1111 1101 *
L0832 1111 1110 1111 1110 1110 1111 1111 1101 *
L0864 1111 1110 1111 1101 1101 1101 1111 1101 *
L0896 1111 1110 1111 1110 1111 1111 1111 1110 *
L1024 1111 1101 1111 1111 1111 1111 1111 1111 *
L1056 1111 1110 1111 1111 1101 1101 1111 1101 *
L1088 1111 1110 1111 1111 1110 1110 1111 1101 *
L1120 1111 1110 1111 1111 1110 1111 1111 1110 *
L1280 1111 1101 1111 1111 1111 1111 1111 1111 *
L1312 1111 1110 1111 1111 1111 1101 1111 1101 *
L1344 1111 1110 1111 1111 1111 1110 1111 1110 *
L1536 1111 1111 1111 1111 1111 1111 1111 1111 *
L1568 1111 1111 1110 1110 1110 1110 1111 1111 *
L1600 1111 1111 1101 0110 1110 0101 1111 1111 *
L1632 1111 0111 0101 0110 1110 1110 0111 1111 *
L1664 1111 1111 0110 1101 0101 0101 0111 1111 *
L1696 0111 0111 0110 1101 0101 1110 1111 0111 *
L1728 0111 1111 0110 1101 0110 0101 1111 0111 *
L1760 0111 0111 0110 0101 1110 1110 0111 0111 *
L1824 1111 1111 0110 1110 1101 0101 0111 0111 *
L1856 0111 0111 1110 1110 0101 0110 0111 0111 *
L1888 0111 1111 0110 0110 0110 0101 0111 0111 *
L2048 101  001  000  000  000  000  101  001  *
C775B*
U0001 CXXXXXXXXNXXXLLLL1XN *
U0002 C00000000NX0HLLLL0LN *
U0003 C11111111NX1HHLLL0HN *
U0004 C11111111NX1HLHLL0HN *
U0005 C00101111NX1HHHLL0HN *
U0006 C11111011NX1HLLHL0HN *
U0007 C10101101NX1HHLHL0HN *
U0008 C11111111NX1HLHHL0HN *
U0009 C00101111NX1HHHHL0HN *
U0010 C11111111NX1HLLLH0HN *
U0011 C10111111NX1HHLLH0HN *
U0012 C11111111NX1LLHLH0LN *
U0013 C00000000NX1LHHLH0LN *
U0014 C11111111NX1LLLHH0LN *
U0015 C00000000NX1LHLHH0LN *
U0016 C11111111NX1LLHHH0LN *
U0017 C00000000NX1LHHHH0LN *
U0018 C11111111NX1HLLLL0LN *
U0019 CXXXXXXXXNX0XLLLL0XN *
F321
```

Diagram 2–2–30 JEDEC FILE

FUSE PLOT is shown on Diagram 2–2–31.

```
:OUT:FUNC:LINE:              11 1111 1111 2222 2222 2233
:PUT:TION: NO  : 0123 4567 8901 2345 6789 0123 4567 8901

: 19: IF :  0 : ---- ---- ---- ---- ---- ---- ---- ----
: 19:    :  1 : ---- ---- ---X X--X ---X X-X- ---- ---- Q4*Q6*A*/B*/C*/D
: 19:  + :  2 : ---- X--- X--X X--X --X- ---X X--- ---- Q2*Q3*Q4*Q7*/A*B*/C*/D
: 19:  + :  3 : ---- ---- X--X ---X X-X- X-X- X--- ---- Q3*Q5*Q6*Q7*A*B*/C*/D
: 19:  + :  4 : X--- X--- X--X --X- X--X ---X ---- X--- Q1*Q2*Q3*Q5*Q8*/A*/B*C*/D
: 19:  + :  5 : X--- ---- X--X --X- X--X X-X- ---- X--- Q1*Q3*Q5*Q6*Q8*A*/B*C*/D
: 19:  + :  6 : X--- X--- X--X X-X- --X- ---X X--- X--- Q1*Q2*Q3*Q4*Q7*Q8*/A*B*C*/
: 19:  + :  7 : ---- ---- X--X --X- --X- X-X- X--- X--- Q3*Q6*Q7*Q8*A*B*C*/D

: 18: IF :  8 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
: 19:  + :  9 : X--- X--- --X- ---X X--X X--X X--- X--- Q1*Q2*Q5*Q6*Q7*Q8*/A*/B*/C
: 19:  + : 10 : X--- ---- X-X- X--X X--X X-X- X--- X--- Q1*Q3*Q4*Q5*Q6*Q7*Q8*A*/B*
:    :    : 11 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 12 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 13 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 14 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 15 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:/17:    : 16 : ---- --X- ---- ---- ---- ---- ---- ---- CLR
:/17:  + : 17 : ---- ---X ---X ---- ---- ---X ---- --X- CNT*/CLR*/A*/D
:/17:  + : 18 : ---- ---X ---X ---- ---X ---- ---- --X- CNT*/CLR*/B*/D
:/17:  + : 19 : ---- ---X ---X ---X --X- --X- ---- --X- CNT*/CLR*A*B*/C*/D
:/17:  + : 20 : ---- ---X --X- --X- --X- --X- ---- --X- CNT*/CLR*A*B*C*D
:/17:  + : 21 : ---- ---X ---X ---- ---- ---- ---- ---X /CNT*/CLR*/D
:    :    : 22 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 23 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:/16:    : 24 : ---- --X- ---- ---- ---- ---- ---- ---- CLR
:/16:  + : 25 : ---- ---X ---- ---X ---- ---X ---- --X- CNT*/CLR*/A*/C
:/16:  + : 26 : ---- ---X ---- ---X ---X ---- ---- --X- CNT*/CLR*/B*/C
:/16:  + : 27 : ---- ---X ---- --X- --X- --X- ---- --X- CNT*/CLR*A*B*C
:/16:  + : 28 : ---- ---X ---- ---X ---- ---- ---- ---X /CNT*/CLR*/C
:    :    : 29 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 30 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 31 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:/15:    : 32 : ---- --X- ---- ---- ---- ---- ---- ---- CLR
:/15:  + : 33 : ---- ---X ---- ---- --X- --X- ---- --X- CNT*/CLR*A*B
:/15:  + : 34 : ---- ---X ---- ---- ---X ---X ---- --X- CNT*/CLR*/A*/B
:/15:  + : 35 : ---- ---X ---- ---- ---X ---- ---- ---X /CNT*/CLR*/B
:    :    : 36 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 37 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 38 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 39 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

:/14:    : 40 : ---- --X- ---- ---- ---- ---- ---- ---- CLR
:/14:  + : 41 : ---- ---X ---- ---- ---- ---X ---- --X- CNT*/CLR*A
:/14:  + : 42 : ---- ---X ---- ---- ---- ---X ---- ---X /CNT*/CLR*/A
:    :    : 43 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 44 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 45 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 46 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 47 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

: 13: IF : 48 : ---- ---- ---- ---- ---- ---- ---- ----
: 13:    : 49 : ---- ---- ---X ---X ---X ---X ---- ---- /A*/B*/C*/D
: 13:  + : 50 : ---- ---- --X- X--X ---X X-X- ---- ---- Q4*Q6*A*/B*/C*D
: 13:  + : 51 : ---- X--- X-X- X--X ---X ---X X--- ---- Q2*Q3*Q4*Q7*/A*/B*/C*D
: 13:  + : 52 : ---- ---- X--X --X- X-X- X-X- X--- ---- Q3*Q5*Q6*Q7*A*B*C*/D
: 13:  + : 53 : X--- X--- X--X --X- X-X- ---X ---- X--- Q1*Q2*Q3*Q5*Q8*/A*B*C*/D
: 13:  + : 54 : X--- ---- X--X --X- X--X X-X- ---- X--- Q1*Q3*Q5*Q6*Q8*A*/B*C*/D
: 13:  + : 55 : X--- X--- X--X X-X- ---X ---X X--- X--- Q1*Q2*Q3*Q4*Q7*Q8*/A*/B*C*

: 12: IF : 56 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
: 13:  + : 57 : ---- ---- X--X ---X --X- X-X- X--- X--- Q3*Q6*Q7*Q8*A*B*/C*/D*Q*Q
: 13:  + : 58 : X--- X--- ---X ---X X-X- X--X X--- X--- Q1*Q2*Q5*Q6*Q7*Q8*/A*B*/C*
: 13:  + : 59 : X--  ---- X--X X--X X--X X-X- X--- X--- Q1*Q3*Q4*Q5*Q6*Q7*Q8*A*/B*
:    :    : 60 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 61 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 62 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
:    :    : 63 : XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```

Diagram 2–2–31 FUSE PLOT

After implementation of test vector, "EPLASM" execution command "F" is subjected to fault test. Fault test is to examine whether or not SAO (0 degeneracy fault) and SA1 (1 degeneracy fault) are detectable for all product terms which use the test vector.

In case of SAO, wiring are short-circuited and connected to the Ground, and "L" is output even expected value is at "H" level. To detect SAO, determine the expected value so that one product term becomes "H" level and determine the rest of product terms to become "L" level. If the output is "L" at this point, it is readily seen that this product term is in 0 degeneracy fault. For example, the 3rd product term of Boolean equation of S 1 derived from (2) is :

$$Q3 * Q5 * Q6 * Q7 * A * B * \overline{C} * \overline{D}$$

When determining expected value so that this product term becomes "H" level, they are :

Q 1 → L	Q 2 → L	Q 3 → H	Q 4 → L	Q 5 → H	Q 6 → H
Q 7 → H	Q 8 → L	A → H	B → H	C → L	D → L

The rest of product terms are all "L" and hence, SAO is detectable.

In case of SA1, wiring are short-circuited and connected to V_{CC}, therefore, "H" is output even output expected value is at "L" level. In this occasion, this is reverse to SAO and determine expected value so that all product terms become "L". Fault test results are shown on Diagram 2–2–32. As readily seen from the test results, fault undetectable product terms (equation 5 1st and 2nd product term, equation 7 1st, 2nd and 3rd product term) are shown. Input output pins of pin 12 and pin 18, being collected pins of equation 5 and 7, are used as input pin and are indicated as detection impossible. However, since these product terms are output to pin 13 and pin 19, using share function of product term, practical fault detecting percent is 100%.

```
IF (GND) CLR =Q1*Q2*Q5*Q6*Q7*Q8*/A*/B*/C*D                    ⑤
             +Q1*Q3*Q4*Q5*Q6*Q7*Q8*A*/B*/C*D

IF (VCC)  S1   =          Q4*    Q6*        A*/B*/C*/D          ⑥
               +   Q2*Q3*Q4*       Q7*    /A* B*/C*/D
               +       Q3*    Q5*Q6*Q7*     A* B*/C*/D
               +Q1*Q2*Q3*    Q5*       Q8*/A*/B* C*/D
               +Q1*   Q3*    Q5*Q6*    Q8* A*/B* C*/D
               +Q1*Q2*Q3*Q4*       Q7*Q8*/A* B* C*/D
               +       Q3*       Q6*Q7*Q8* A* B* C*/D
               +Q1*Q2*       Q5*Q6*Q7*Q8*/A*/B*/C* D
               +Q1*   Q3*Q4*Q5*Q6*Q7*Q8* A*/B*/C* D

IF (GND) CNT =Q3*Q6*Q7*Q8*A*B*/C*/D                           ⑦
             +Q1*Q2*Q5*Q6*Q7*Q8*/A*B*/C*/D
             +Q1*Q3*Q4*Q5*Q6*Q7*Q8*A*/B*/C*/D

IF (VCC)  S2   =                         /A*/B*/C*/D          ⑧
               +          Q4*    Q6*        A*/B*/C* D
               +   Q2*Q3*Q4*       Q7*    /A*/B*/C* D
               +       Q3*    Q5*Q6*Q7*     A* B* C*/D
               +Q1*Q2*Q3*    Q5*       Q8*/A* B* C*/D
               +Q1*   Q3*    Q5*Q6*    Q8* A*/B* C*/D
               +Q1*Q2*Q3*Q4*       Q7*Q8*/A*/B* C*/D
               +       Q3*       Q6*Q7*Q8* A* B*/C*/D
               +Q1*Q2*       Q5*Q6*Q7*Q8*/A* B*/C*/D
               +Q1*   Q3*Q4*Q5*Q6*Q7*Q8* A*/B*/C*/D
```

```
PASS SIMULATION
 PRODUCT:   1 OF EQUATION.   5 UNTESTED(SA1) FAULT
 PRODUCT:   2 OF EQUATION.   5 UNTESTED(SA1) FAULT
 PRODUCT:   1 OF EQUATION.   7 UNTESTED(SA1) FAULT
 PRODUCT:   2 OF EQUATION.   7 UNTESTED(SA1) FAULT
 PRODUCT:   3 OF EQUATION.   7 UNTESTED(SA1) FAULT
 PRODUCT:   1 OF EQUATION.   5 UNTESTED(SA0) FAULT
 PRODUCT:   2 OF EQUATION.   5 UNTESTED(SA0) FAULT
 PRODUCT:   1 OF EQUATION.   7 UNTESTED(SA0) FAULT
 PRODUCT:   2 OF EQUATION.   7 UNTESTED(SA0) FAULT
 PRODUCT:   3 OF EQUATION.   7 UNTESTED(SA0) FAULT

NUMBER OF STUCK AT ONE (SA1) FAULTS ARE = 37

NUMBER OF STUCK AT ZERO (SA0) FAULTS ARE = 37

PRODUCT TERM COVERAGE                    =  88%
```

Diagram 2–2–32 Fault test

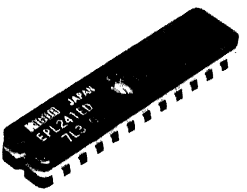
EPL241E

CMOS ELECTRICALLY PROGRAMMABLE LOGIC

■ OUTLINE

The EPL241 is a field-programmable logic array with CMOS-EPROM processing and AND-OR(fixed)-Register configuration.

Programming is easily handled, even on the user's side, by writing to the EPROM memory cells arranged on the array. This programming technique shortens the development period greatly and simplifies circuit corrections.



Each output configuration is individually defined using 16 programmable macro I/O cells. This means you can specify either combination output or register output, and the polarity. Each macro cell has two feedback signals, with which you can simultaneously feedback both the combination and register outputs, or can feedback one of the combination and register outputs while using an I/O pin as an input pin. The power consumption varies with the product term use efficiency (40mA when 35% use).

■ FEATURES

- Low power consumption and high reliability thanks to the CMOS-EPROM process
- 24 pins, 22 inputs, 16 outputs
- Ultraviolet ray deletion is available in ceramic-packaged products
- Package

EPL241ED	24 pins	300 mil	CERDIP (with window)
EPL241EP	24 pins	300 mil	MOLD DIP
EPL241EJ	28 pins		PLCC (under development)

- Data copy prevention function
- Input/output propagation delay 25ns (max)
- Improved functions with macro I/O cells
  - A. Selection of combination outputs and register outputs
  - B. Selection of feedback signals
  - C. Selection of synchronous $\overline{OE}$ and asynchronous $\overline{OE}$
  - D. Selection of output polarity
  - E. Selection of clock signals (CLK1, CLK2, Internal CLK)
  - F. Asynchronous reset (AR1, AR2, AR3)
  - G. Synchronous preset (SP1, SP2, SP3)

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Conditions	Limits	Unit
Vcc	Vcc Supply Voltage	With respect to GND	-0.3 ~ 7.0	V
Vpp	Vpp Supply Voltage		-0.3 ~ 14.5	V
Vi	Input Voltage		-0.3 ~ Vcc+0.3	V
Vo	Output Voltage		-0.3 ~ Vcc+0.3	V
Pd	Maximum Power Consumption	Ta=25°C	0.8	W
Topr	Operating Ambient Temperature		-20 ~ 70	°C
Tstg	Storage Temperature		-40 ~ 125	°C

■ CAPACITANCE

Symbol	Parameters	Conditions	min.	typ.	max.	Unit
	Input Pin	f = IMHz Vcc = OV		5		pF
	I/O Pin			8		
	Vpp Pin			10		

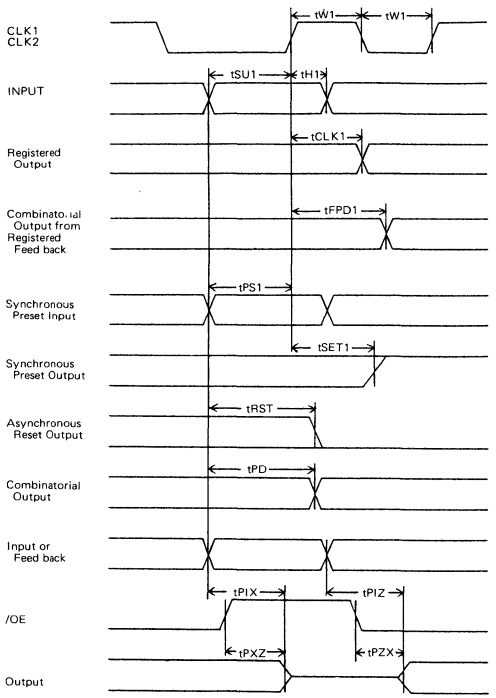
■ D.C. CHARACTERISTICS (Ta = 0 ~ 70°C Vcc = 5V ± 5%)

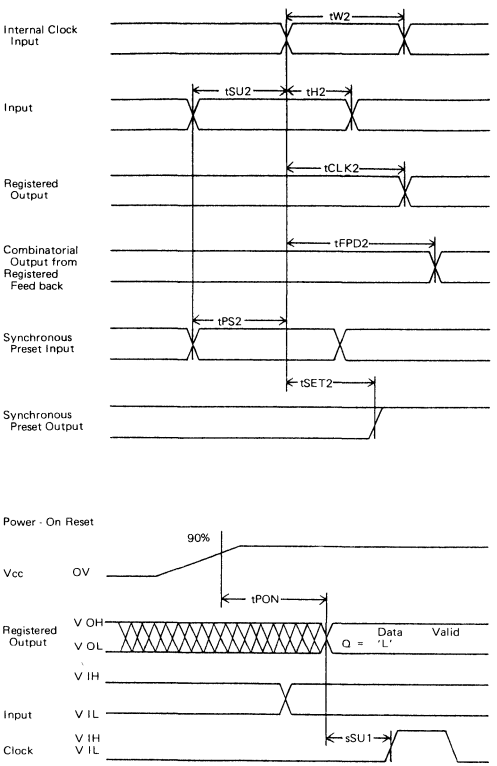
Symbol	Parameters	Conditions	Specified Value			Unit
			min.	typ.	max.	
I_{LI}	Input leak current	Vin=OV ~ Vcc	-20		20	μA
I_{LO}	Output leak current for OFF state	Vo=OV ~ Vcc	-20		20	μA
V_{IL}	"L" Input Voltage		-0.3		0.8	V
V_{IH}	"H" Input Voltage		2.0		Vcc+0.3	V
V_{OL}	"L" Output Voltage	Vcc=MIN Iol=8mA			0.5	V
V_{OH}	"H" Qutput Voltage	Vcc=MIN Ioh=-3.2mA	2.4			V
Icc1	Supply Voltage (standby)	Vcc=MAX f=OMHz Vin=GND or Vcc			120	mA
Icc2	Supply Voltage (operation)	Vcc=MAX f=10MHz Vin=GND or Vcc			140	mA

■ A.C. CHARACTERISTICS (Ta = 0 ~ 70°C Vcc = 5V ± 5%)

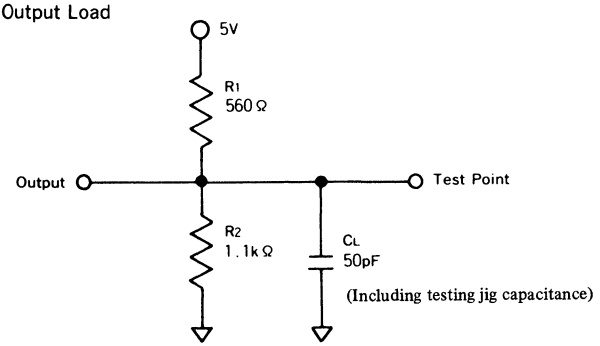
Symbol	Parameters		Conditions	Specified Value			Unit
	Clock	Parameter		min.	typ.	max.	
Tpd		Input or I/O input to non-registered output				25	nS
Tpix		Input or I/O input to output disable				25	nS
Tpiz		Input or I/O input to output enable				25	nS
Tpxz		OE to output disable				20	nS
Tpzx		OE to output enable	C1 = 50pF			20	nS
Tsu1		Input or I/O input setup time		18			nS
Th1		Input or I/O input hold time		0			nS
Tclk1	External Clock	Clock to output delay	R1 = 560 Ω			15	nS
Tfpd1		Clock to non-registered output from registered feedback				35	nS
Tw1	CLK1 (1pin)	External clock width	R2 = 1.1 kΩ	15			nS
Tps1		Synchronous preset input setup time		18			nS
Tset1	CLK2 (11pin)	Clock to register preset				15	nS
Trst		Input or I/O input to asynchronous reset				25	nS
Tp1		Minimum clock period				33	nS
f1		Maximum frequency		30			MHz
Tsu2		Input or I/O input setup time		5			nS
Thz		Input or I/O input hold time		10			nS
Tclk2	Internal Clock	Clock P.T. input to output delay				30	nS
Tfpd2		Clock P.T. input to non-registered output from registered feedback				50	nS
Tw2	CKP1 CKP2 CKP3	Clock P.T. input width		15			nS
Tps2		Synchronous preset input setup time		5			nS
Tset2		Clock P.T. input to register preset				30	nS
Tp2		Minimum clock period				35	nS
f2		Minimum frequency		28.6			MHz
Tpon		Power On Reset Time		45			μs

■ TIMING DIAGRAM

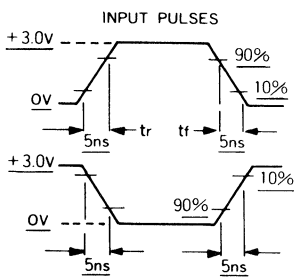




Output Load



Input Waveform



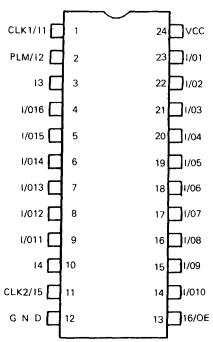
NOTE : This is the A.C. characteristic measurement with a voltage of 1.5V on both the input and output.

■ PIN DESCRIPTION

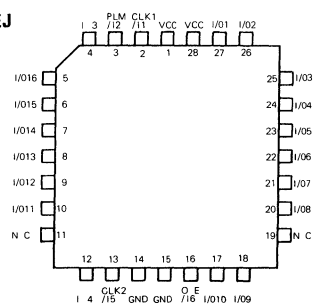
Pin No.		Pin Name		Function		
DIP	PLCC	Operating	Programming	Operating		Programming
1	2	CLK1/I1	Vpp		Clock 1	Programming Power Supply
2	3	PLM/I2	CA4		Pre-load	Column Address Input
3	4	I3	CA3	Input		
4	5	I/016	CA2			
5	6	I/015	CA1			
6	7	I/014	CA0	Input/Output		
7	8	I/013	RA6			Row Address Input
8	9	I/012	RA5			
9	10	I/011	RA4			
10	12	I4	RA3	Input		
11	13	CLK2/I5	RA2		Clock 2	
12	14 • 15	GND	GND	GND		GND
13	16	$\overline{OE}$/16	PGM/$\overline{OE}$	Output Enable/Input		Programming Control /Output Enable
14	17	I/010	RA1			Row Address Input
15	18	I/09	D7			Data Input/Output
16	20	I/08	D6			
17	21	I/07	D5			
18	22	I/06	D4	Input/Output		
19	23	I/05	D3			
20	24	I/04	D2			
21	25	I/03	D1			
22	26	I/02	SEQ/D0			Security Data
23	27	I/01	RA0			Row Address Input
24	1 • 28	Vcc	Vcc	Vcc		Vcc

■ PIN CONFIGURATION

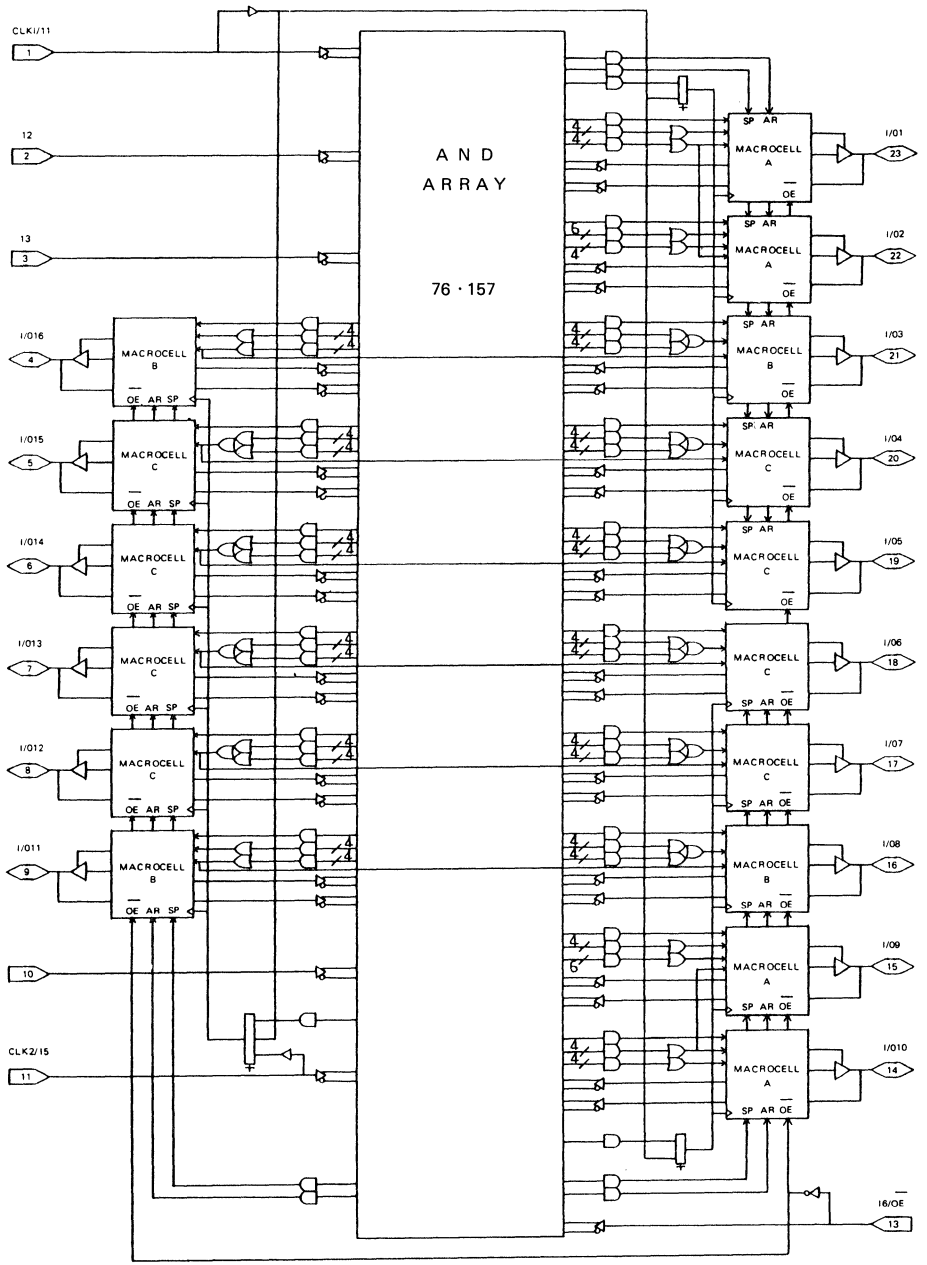
EPL241ED
EPL241EP



EPL241EJ

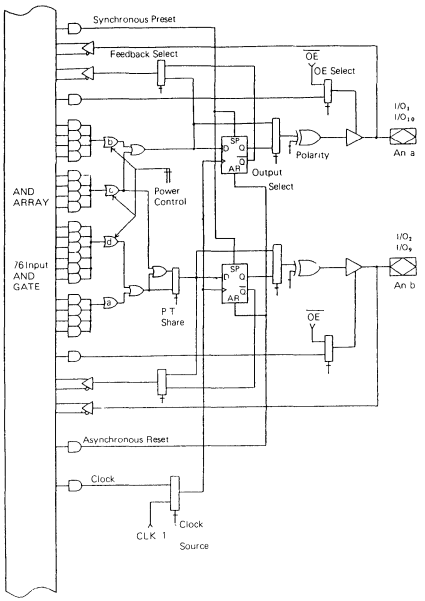


■ BLOCK DIAGRAM

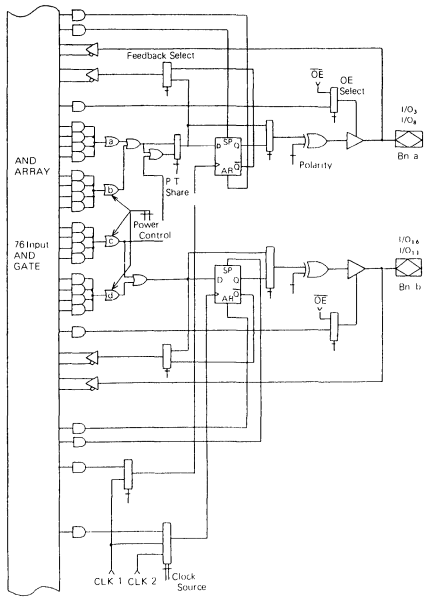


■ MACRO I/O CELL

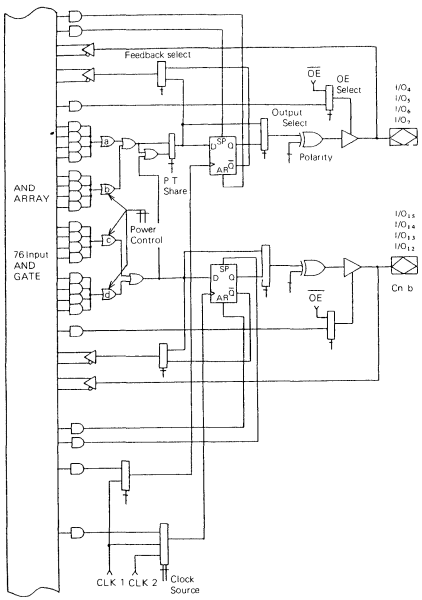
MACRO I/O CELL A



MACRO I/O CELL B



MACRO I/O CELL C



■ FUNCTIONS AND OPERATIONS

The EPL241 is a logic array that can delete and rewrite. It uses CMOS-EPROM and has 76 input terms (22 inputs and 16 feedbacks) and 157 product terms.

All input pins conduct normal logic operation in TTL level. Use and unuse of registers and polarity of output can be selected by I/O macro cells.

Every intersection of a product term and an input term on AND array has an EPROM cell connection. When delivered, all the intersections are connected.

As shown in figure 1, AND output (P1) becomes inactive if neither positive input (I) nor negative input ($\overline{I}$) is written, and AND output (P2) becomes logically Don't Care if both positive input (I) and negative input ($\overline{I}$) are written.

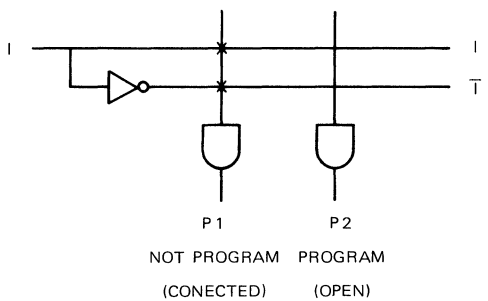


Figure 1

Macro I/O cell

The macro I/O cell has power control, feedback select, and other control functions, and operates by writing to an optional bit (O.B) EPROM CELL.

Each control function is explained below (The switch positions are when not writing to the O.B.).

(a) Power Control (P.C)

P.C supplies power to OR section of the product term that is logically used. Power consumption is drastically reduced thanks to this.

(About 40 mA when the product term use efficiency is 35%)

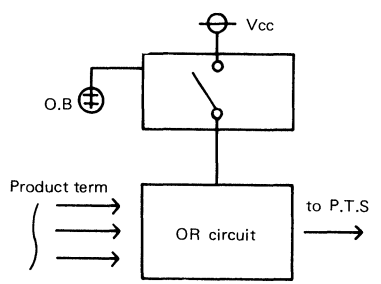


Figure 2 Power Control

(b) Product Term Share (P.T.S)

P.T.S controls share or no share function of the OR output of adjacent product terms.
In figure 3, the output is as follows:

Share : A + B + C
No Share : A + B

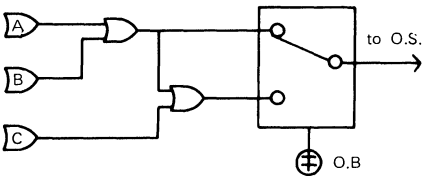


Figure 3 Product Term Share

(c) Output Select (O.S) Feed Back Select (F.B.S)

O.S controls whether a signal to output uses a register, and F.B.S controls whether a signal to feedback uses a register (See figure 4). The EPL241 has 16 available registers and two CLOCK phases. The O.B. controls the switching of phase 1/ phase 2 of the CLOCK.

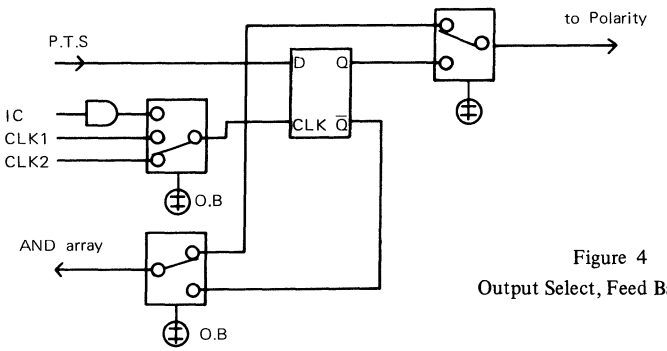


Figure 4
Output Select, Feed Back Select

(d) Polarity

Polarity controls the polarity of the output signals (See figure 5).

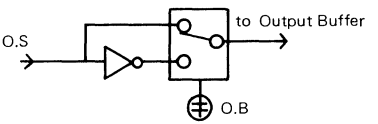


Figure 5 Polarity

(e) Output Enable Select (O.E.S)

O.E.S controls the choice of the output buffer OE signal. Either the external signal input to pin 13 or the signal according to internal logic is chosen (See figure 6).

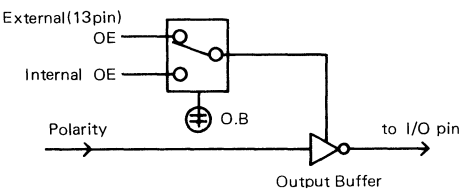
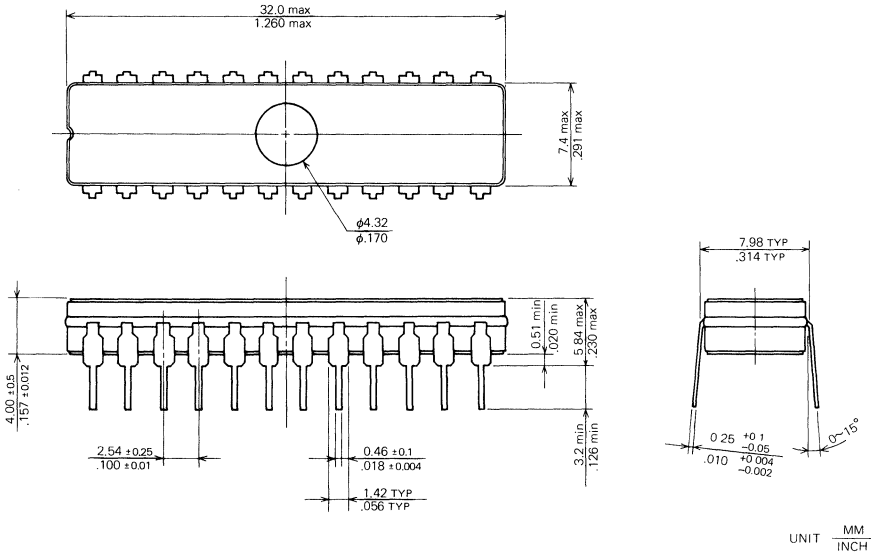


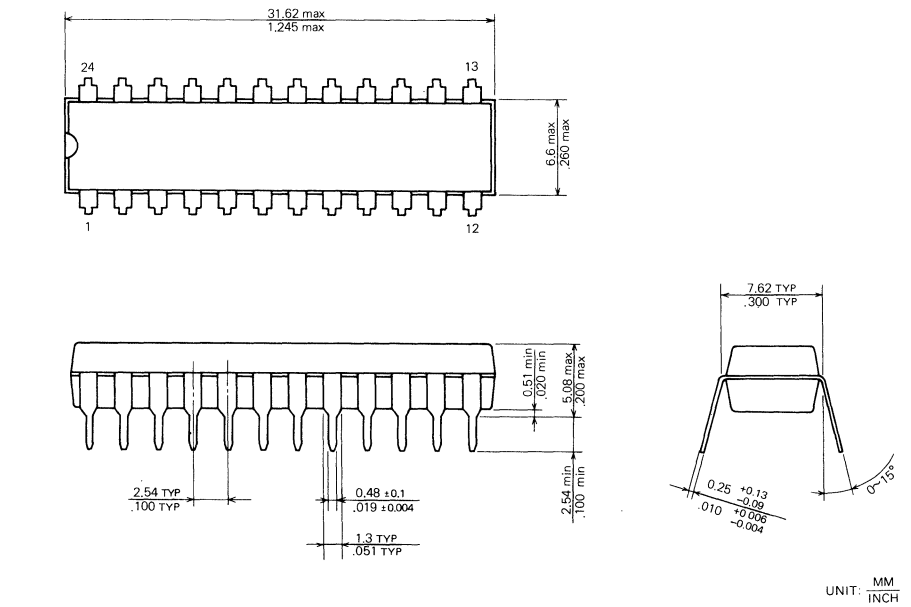
Figure 6 Output Enable Select

■ PACKAGE DIMENSION

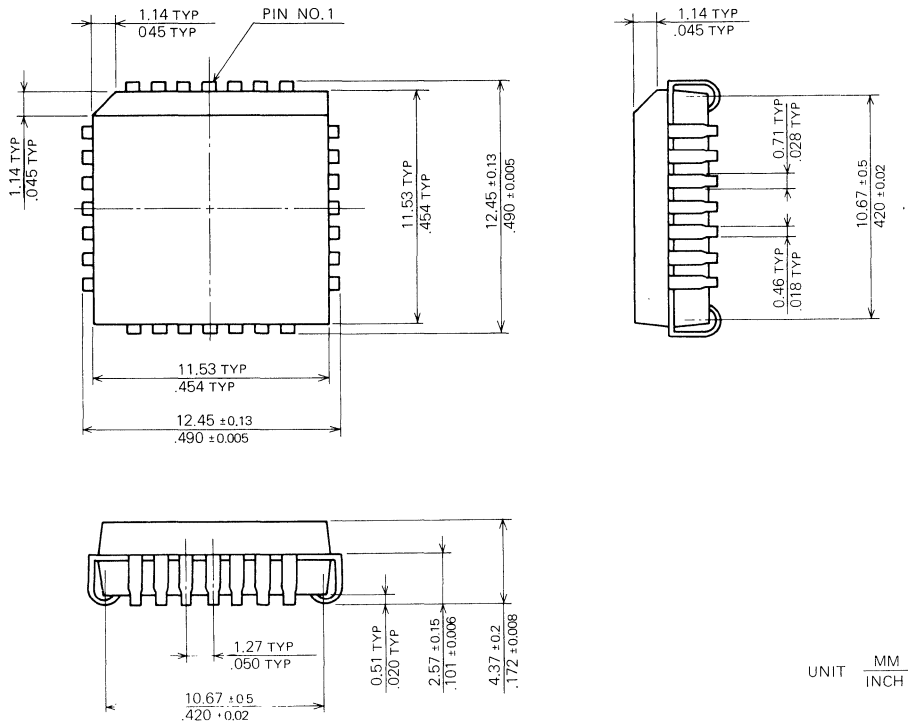
- EPL241ED (24 PIN 300mil CERDIP)



- EPL241EP (24 PIN 300mil MOLD DIP)



● EPL241EJ (28 PIN PLCC)



Microelectronic Specification

CMOS GATE ARRAY 5GH SERIES

■GENERAL DESCRIPTION

RP5GH05/10/16/23/29/38/55 are gate array LSIs by using 2μm silicon gate C-MOS technology.

It is possible to develop LSI by utilizing the fully CAD support and the abundant function cell library.

The RP5GH series also allows users to realize the one chip system board easily and realize high-speed access and high-reliability.

■FEATURES

- High Speed 2μm C-MOS Process.
- Fully CAD Support System.
- Abundant Cell Library for Easy Design.
- TTL/CMOS I/O Compatibility.
- Input with Pull-up/Pull-down Resister.
- Open Drain Output.

TYPE	GATE COUNT	I/O COUNT	PACKAGE (PIN COUNT)			
			DIP	FLAT	PLCC	PIP
RP5GH05	560	40	16, 24, 28, 40	—	—	—
RP5GH10	1000	60	24, 28, 40, 48	60	44	—
RP5GH16	1600	72	24, 28, 40, 48	60, 80	44	—
RP5GH23	2300	88	28, 40, 48, 64	60, 80, 100	68, 84	—
RP5GH29	2900	98	28, 40, 48, 64	60, 80, 100	68, 84	—
RP5GH38	3800	108	40, 48, 64	60, 80, 100	68, 84	108
RP5GH55	5500	120	64	—	—	100, 120

■ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Condition	Limits	Unit
Vcc	Supply Voltage	With respect to GND	−0.3~7	V
VI	Input Voltage		−0.3~Vcc+0.3	V
Vo	Output Voltage		−0.3~Vcc+0.3	V
Topr	Operating Ambient Temperature		0~70	℃
Tstg	Storage Temperature		−40~125	℃

■ELECTRICAL CHARACTERISTICS

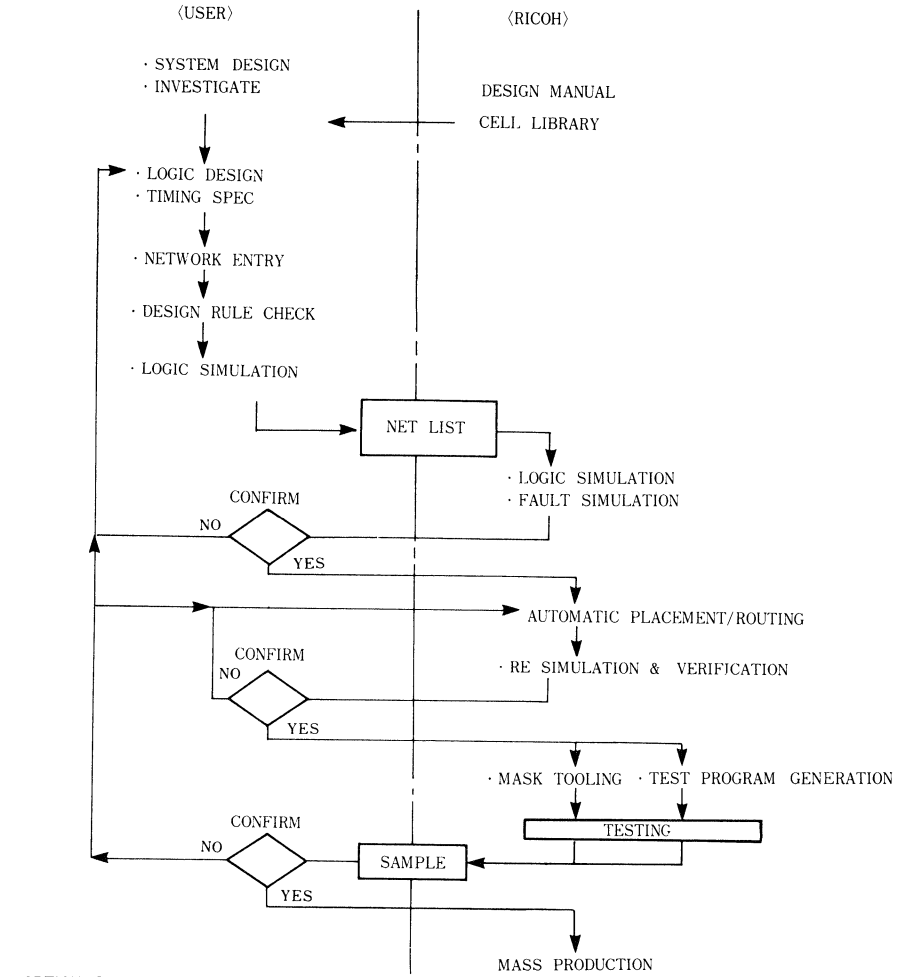
DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

Symbol	Parameters	Measuring Conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	Input "H"Voltage (TTL compatible)		2.2		Vcc+0.3	V
V_{IL}	Input "L"Voltage (TTL compatible)		−0.3		0.8	V
V_{IH}	Input "H"Voltage (C-MOS compatible)		3.5		Vcc+0.3	V
V_{IL}	Input "L"Voltage (C-MOS compatible)		−0.3		1.5	V
V_{OH}	Output "H"Voltage	I_{OH}=−4mA	2.4			V
V_{OL}	Output "L"Voltage	I_{OL}=4mA			0.4	V
I_{LI}	Input Leakage Current	VI=0~Vcc	−10		10	μA
I_{Lo}	Output Leakage Current	Vo=0~Vcc	−10		10	μA

AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

Symbol	Parameters	Measuring Conditions	Limits			Unit
			Min	Typ	Max	
tpd	Basic Gate Delay Time	2 Input NAND (FAN OUT=3)		1.5		ns
tpdo	Output Buffer Delay Time	CL=100pF		10		ns

■DEVELOPMENT FLOW CHART

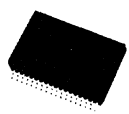


※OPTION : LOGIC DIAGRAM AND LOGIC SIMULATION DATA INTERFACE IS AVAILABLE AS AN OPTION.

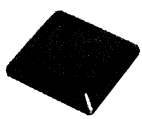
■PACKAGE

DIP 16,24,28,40,48,64 PIN

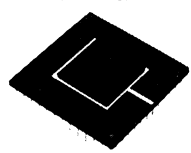
FLAT 60,80,100 PIN



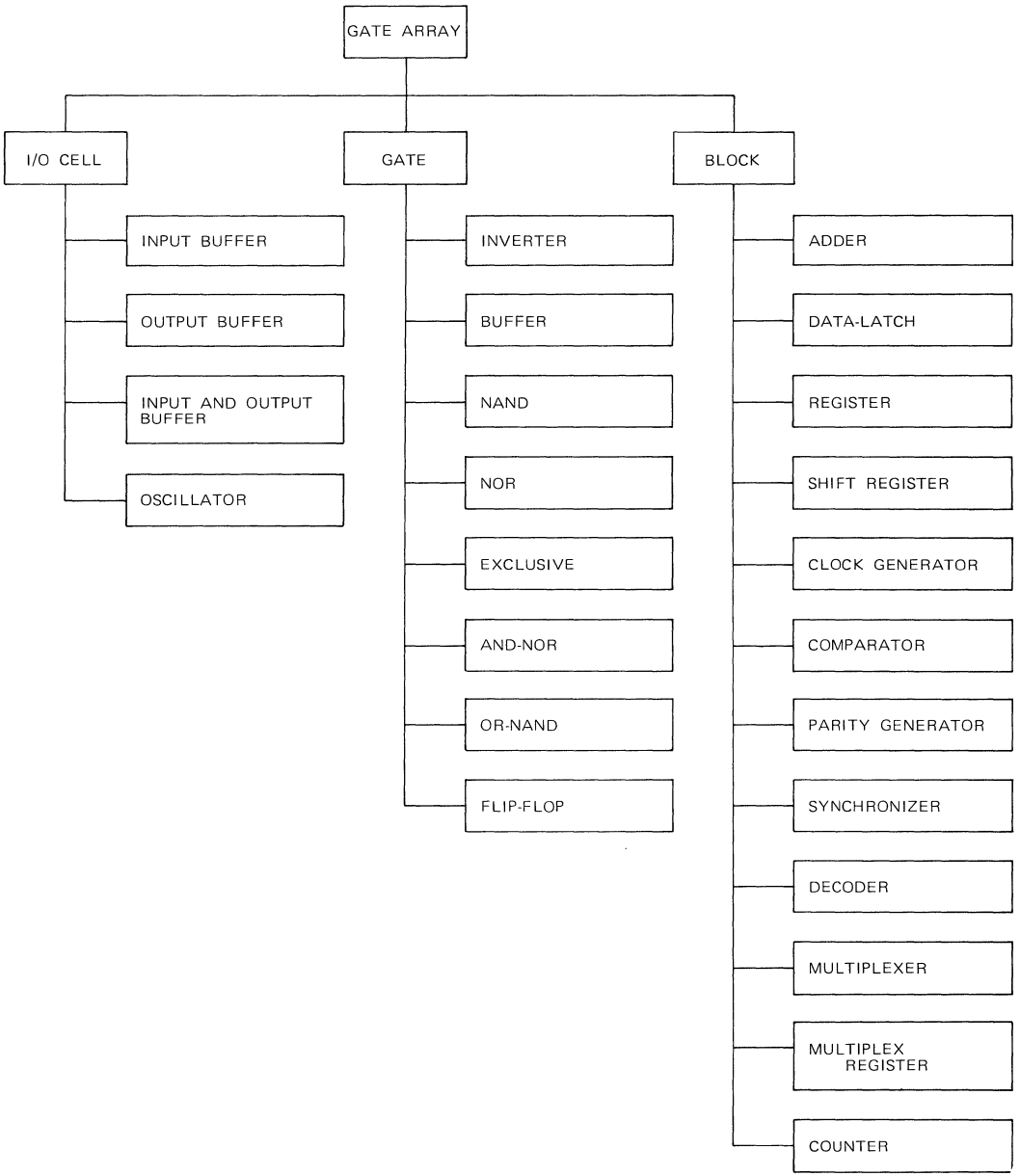
PLCC 44,68,84



PIP 100,108,120 PIN



CMOS GATE ARRAY 5GH series
CELL LIST



I/O CELL

INPUT BUFFER

STANDARD

CELL	FUNCTION	
INT01	TTL Compatible	Inverter
INT02	TTL	Buffer
INTSCH	TTL	Schmitt Trigger
INC01	CMOS Compatible	Inverter
INC02	CMOS	Buffer
INCSCH	CMOS	Schmitt Trigger

with RESISTANCE for Pull-Up

INT1U1	TTL Compatible	Inverter
INT2U1	TTL	Buffer
INTSU1	TTL	Schmitt Trigger
INC1U1	CMOS Compatible	Inverter
INC2U1	CMOS	Buffer
INCSU1	CMOS	Schmitt Trigger

with RESISTANCE for Pull-Down

INT1D1	TTL Compatible	Inverter
INT2D1	TTL	Buffer
INTSD1	TTL	Schmitt Trigger
INC1D1	CMOS Compatible	Inverter
INC2D1	CMOS	Buffer
INCSD1	CMOS	Schmitt Trigger

OUTPUT BUFFER

OUTINV	Inverter
OUTTRI	3-State Output
OUTOPN	Open Drain Output

OUTPUT AND INPUT BUFFER

STANDARD

IOT01 IOT1	TTL Compatible	Inverter & 3-State Output
IOT02 IOT2	TTL Compatible	Buffer & 3-State Output
IOTSCH IOTSH	TTL Compatible	Schmitt Trigger & 3-State Output
IOC01 IOC1	CMOS Compatible	Inverter & 3-State Output
IOC02 IOC2	CMOS Compatible	Buffer & 3-State Output
IOCSCH IOCSH	CMOS Compatible	Schmitt Trigger & 3-State Output

with RESISTANCE for Pull-Up

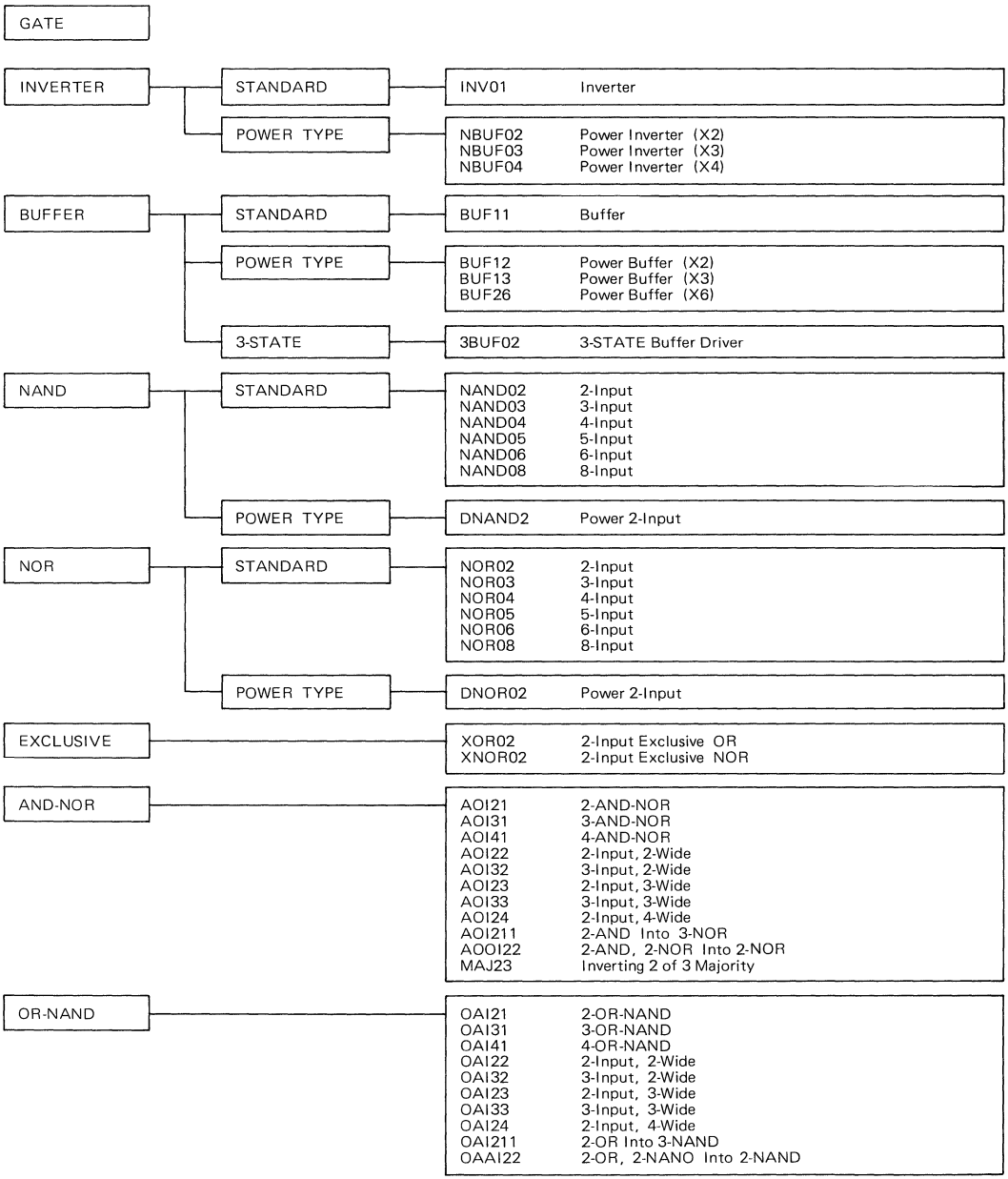
IOT1U1 IOTU1	TTL Compatible	Inverter & 3-State Output
IOC1U1 IOCU1	CMOS Compatible	Inverter & 3-State Output

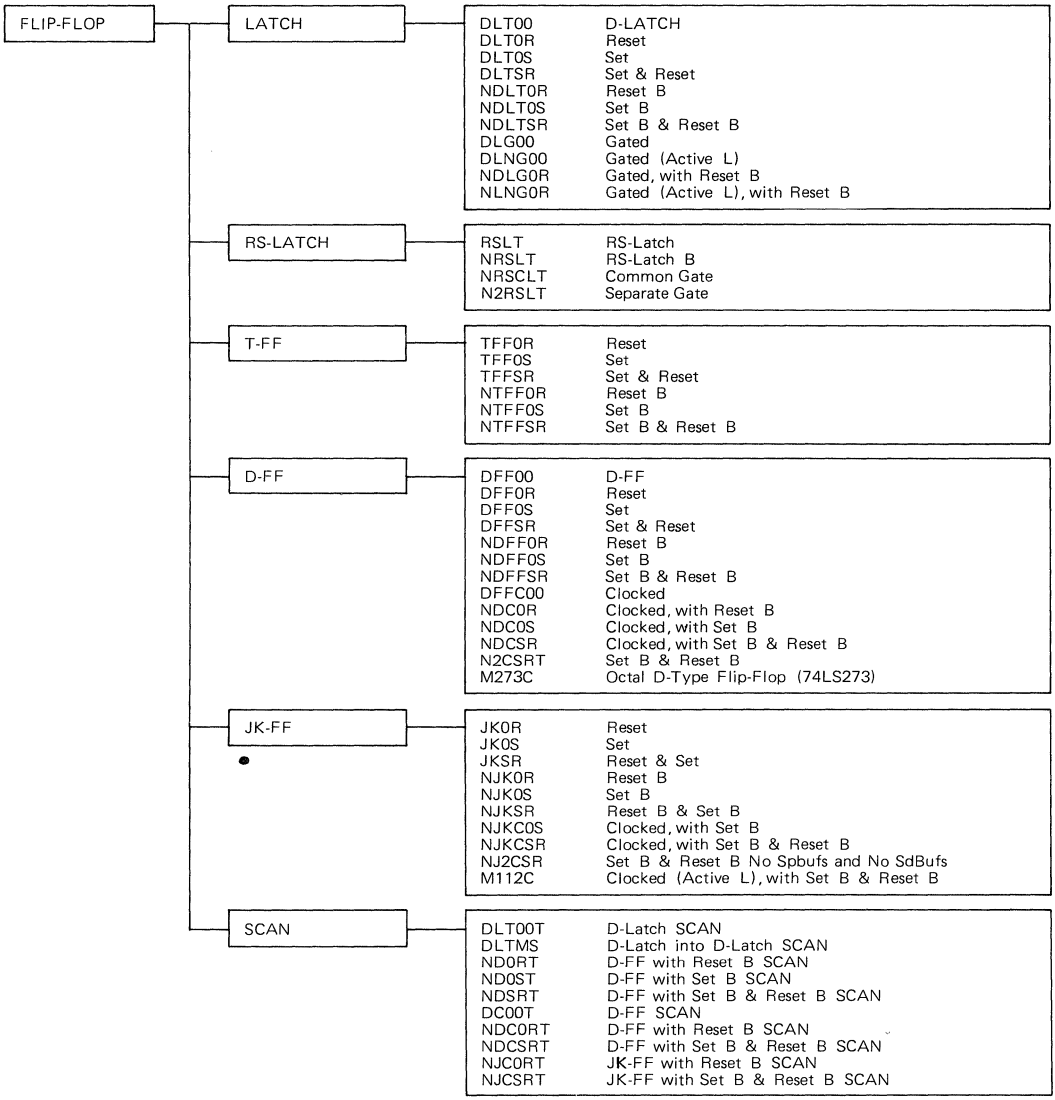
with RESISTANCE for Pull-Down

IOT1D1 IOTD1	TTL Compatible	Inverter & 3-State Output
IOC1D1 IOCD1	CMOS Compatible	Inverter & 3-State Output

OSCILLATOR

XIN01	Input
XOUT	Oscillater Output
XIO	Oscillator


GATE
INVERTER
STANDARD
INV01 Inverter
POWER TYPE
NBUF02 Power Inverter (X2)
NBUF03 Power Inverter (X3)
NBUF04 Power Inverter (X4)
BUFFER
STANDARD
BUF11 Buffer
POWER TYPE
BUF12 Power Buffer (X2)
BUF13 Power Buffer (X3)
BUF26 Power Buffer (X6)
3-STATE
3BUF02 3-STATE Buffer Driver
NAND
STANDARD
NAND02 2-Input
NAND03 3-Input
NAND04 4-Input
NAND05 5-Input
NAND06 6-Input
NAND08 8-Input
POWER TYPE
DNAND2 Power 2-Input
NOR
STANDARD
NOR02 2-Input
NOR03 3-Input
NOR04 4-Input
NOR05 5-Input
NOR06 6-Input
NOR08 8-Input
POWER TYPE
DNOR02 Power 2-Input
EXCLUSIVE
XOR02 2-Input Exclusive OR
XNOR02 2-Input Exclusive NOR
AND-NOR
AOI21 2-AND-NOR
AOI31 3-AND-NOR
AOI41 4-AND-NOR
AOI22 2-Input, 2-Wide
AOI32 3-Input, 2-Wide
AOI23 2-Input, 3-Wide
AOI33 3-Input, 3-Wide
AOI24 2-Input, 4-Wide
AOI211 2-AND Into 3-NOR
AOOI22 2-AND, 2-NOR Into 2-NOR
MAJ23 Inverting 2 of 3 Majority
OR-NAND
OAI21 2-OR-NAND
OAI31 3-OR-NAND
OAI41 4-OR-NAND
OAI22 2-Input, 2-Wide
OAI32 3-Input, 2-Wide
OAI23 2-Input, 3-Wide
OAI33 3-Input, 3-Wide
OAI24 2-Input, 4-Wide
OAI211 2-OR Into 3-NAND
OAAI22 2-OR, 2-NANO Into 2-NAND


FLIP-FLOP
LATCH
DLT00 D-LATCH
DLT0R Reset
DLT0S Set
DLTSR Set & Reset
NDLT0R Reset B
NDLT0S Set B
NDLTSR Set B & Reset B
DLG00 Gated
DLNG00 Gated (Active L)
NDLG0R Gated, with Reset B
NLNG0R Gated (Active L), with Reset B
RS-LATCH
RSLT RS-Latch
NRSLT RS-Latch B
NRSCLT Common Gate
N2RSLT Separate Gate
T-FF
TFF0R Reset
TFF0S Set
TFFSR Set & Reset
NTFF0R Reset B
NTFF0S Set B
NTFFSR Set B & Reset B
D-FF
DFF00 D-FF
DFF0R Reset
DFF0S Set
DFFSR Set & Reset
NDFF0R Reset B
NDFF0S Set B
NDFFSR Set B & Reset B
DFFC00 Clocked
NDC0R Clocked, with Reset B
NDC0S Clocked, with Set B
NDCSR Clocked, with Set B & Reset B
N2CSRT Set B & Reset B
M273C Octal D-Type Flip-Flop (74LS273)
JK-FF
JK0R Reset
JK0S Set
JKSR Reset & Set
NJK0R Reset B
NJK0S Set B
NJKSR Reset B & Set B
NJKC0S Clocked, with Set B
NJKCSR Clocked, with Set B & Reset B
NJ2CSR Set B & Reset B No Spbufs and No SdBufs
M112C Clocked (Active L), with Set B & Reset B
SCAN
DLT00T D-Latch SCAN
DLTMS D-Latch into D-Latch SCAN
ND0RT D-FF with Reset B SCAN
ND0ST D-FF with Set B SCAN
NDSRT D-FF with Set B & Reset B SCAN
DC00T D-FF SCAN
NDC0RT D-FF with Reset B SCAN
NDCSRT D-FF with Set B & Reset B SCAN
NJC0RT JK-FF with Reset B SCAN
NJCSRT JK-FF with Set B & Reset B SCAN

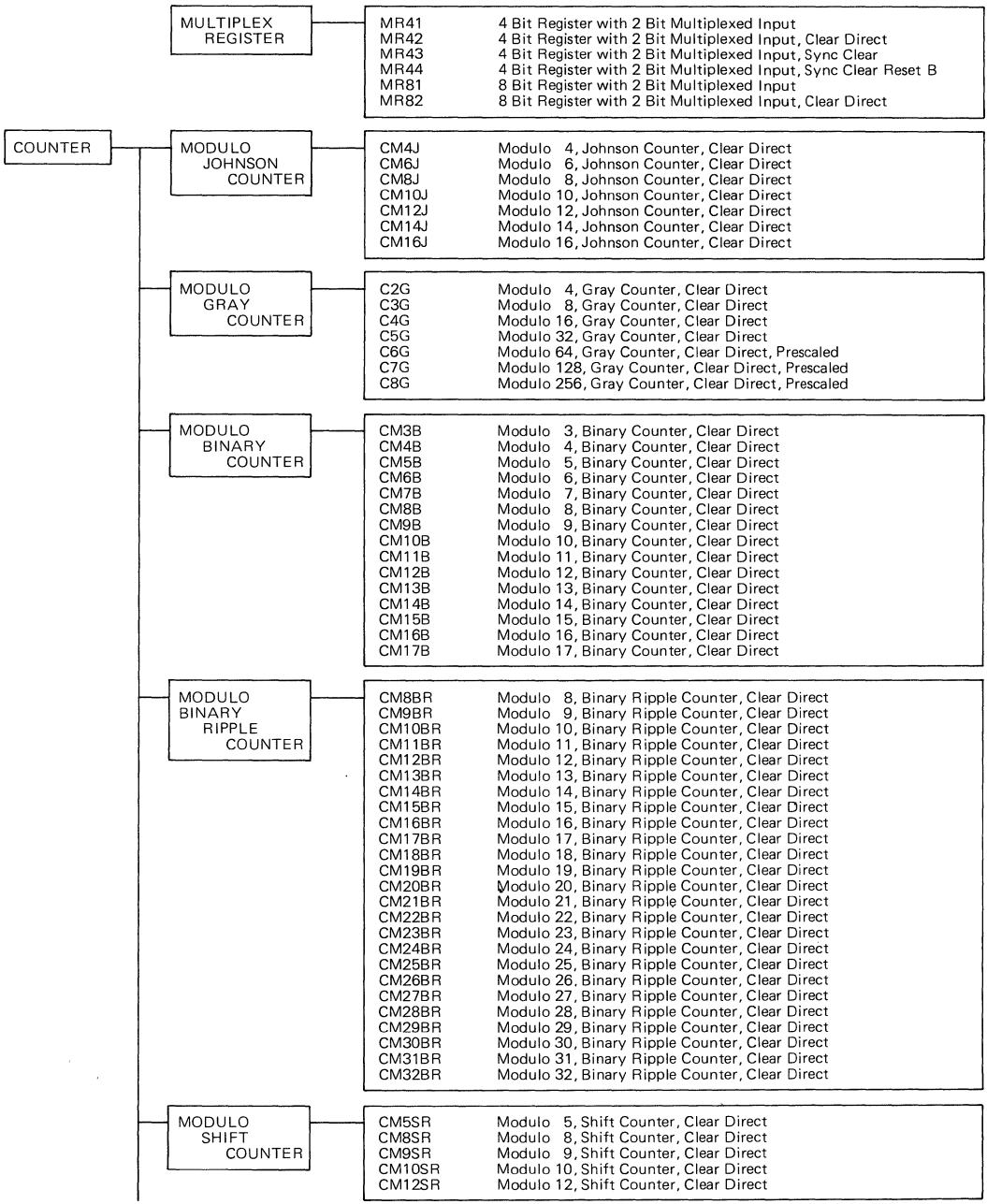
BLOCK		
ADDER	HA1	Half Adder
	FA1	Full Adder
	M80C	Gated Full Adder (7480)
	FA2	2 Bit Binary Full Adder
	FAS2	2 Bit Binary 2's Complement Full Adder, or substractor
	M82C	2 Bit Binary Full Adder (7482)
	FA4	4 Bit Binary Full Adder
	M83C	4 Bit Binary Full Adder with Fast Carry (74LS83)
	CLA1	Carry Look Ahead for 4 Bit Adder (Least Significant Nibble)
	CLA2	Carry Look Ahead for 4 Bit Adder
	FA16	16 Bit Fast Adder
DATA-LATCH	L4	4 Bit Data Latch
	L8	8 Bit Data Latch
REGISTER	R41	4 Bit Data Register
	R42	4 Bit Data Register, Clear Direct
	R81	8 Bit Data Register
	R82	8 Bit Data Register, Clear Direct
SHIFT RESISTER	SR41	4 Bit Shift Register
	SR42	4 Bit Shift Register, Clear Direct
	M95C	4 Bit Shift Register (74LS95)
	SR43	4 Bit Shift Register, Set Direct
	SR44	4 Bit Shift Register, Synchronous Parallel Load
	SR45	4 Bit Shift Register, Synchronous Parallel Load and Clear
	SR46	4 Bit Shift Register, Asynchronous Parallel Load
	SR47	4 Bit Shift Register, Sync Clear
	M94C	4 Bit Shift Register (7494)
	M179C	4 Bit Parallel Access Shift Register (74179)
	M195C	4 Bit Parallel-Access Shift Register (74LS195)
	M96C	5 Bit Shift Register (74LS96)
	M91C	8 Bit Shift Register (74LS91)
	M164C	8 Bit Parallel Output Serial Shift Register (74LS164)
	M165C	Parallel Load 8 Bit Shift Register (74LS165)
	M166C	8 Bit Shift Register (74LS166)
	M198C	8 Bit Bidirectional Universal Shift Register (74198)
	M199C	8 Bit Bidirectional Universal Shift Register (74199)
CLOCK GENERATOR	CPG1	Two Phase Clock Generator, Unbuffered, Hi Underlap, Lo Drive
	CPG2	Two Phase Clock Generator, Unbuffered, Lo Underlap, Lo Drive
	CPG3	Two Phase Clock Generator, Unbuffered, Hi Underlap, Hi Drive
	CPG4	Two Phase Clock Generator, Unbuffered, Lo Underlap, Hi Drive
COMPARATOR	MAG2H	2 Bit Magnitude Comparator
	MAG2	2 Bit Extendable Magnitude Comparator
	MAG4	4 Bit Extendable Magnitude Comparator
	CMP4	4 Bit Equality Comparator
	M85C	4 Bit Magnitude Comparator Expandable
	CMP8	8 Bit Equality Comparator
PARITY GENERATOR	PAR8	8 Bit Odd Parity Detector
	PAR9	9 Bit Odd Parity Detector
	M180C	9 Bit Odd/Even Parity Generator (74180)
SYNCHRONIZER	SYNC01	Synchronizer for Asynchronous 0 to 1 Event
	SYNC10	Synchronizer for Asynchronous 1 to 0 Event

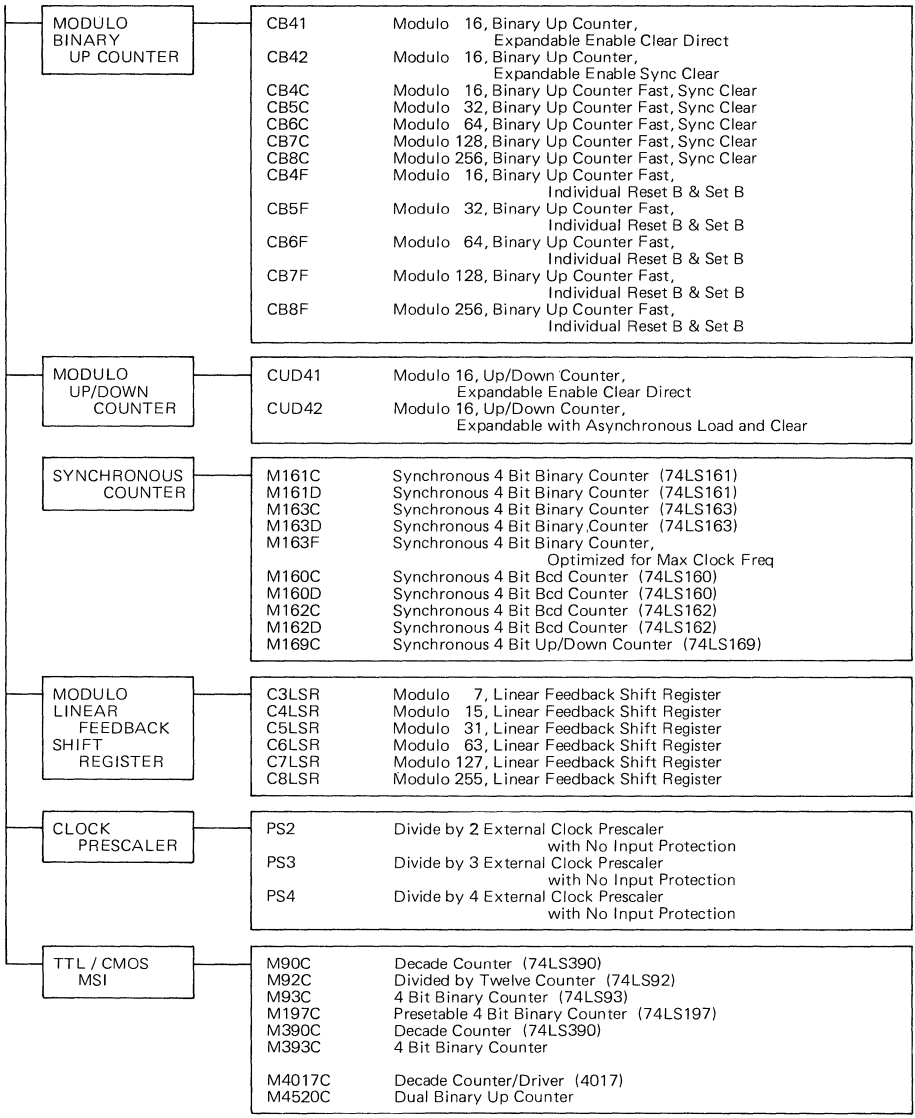
DECODER

M4555C	Binary to 1 of 4 Decoder
M139C	2 to 4 Decoder (74LS139)
M155C	Dual 2 to 4 Decoders
D24H	2 to 4 Decoder, Output Active Hi
D24L	2 to 4 Decoder, Output Active Lo
D24GH	2 to 4 Decoder, Gated Output Active Hi
D24GL	2 to 4 Decoder, Gated Output Active Lo
D38H	3 to 8 Decoder, Output Active Hi
D38L	3 to 8 Decoder, Output Active Lo
D38GH	3 to 8 Decoder, Gated Output Active Hi
D38GL	3 to 8 Decoder, Gated Output Active Lo
M138C	Gated 3 to 8 Decoder (74LS138)
M138D	Gated 3 to 8 Decoder (74LS138)
D410H	4 to 10 Decoder, Output Active Hi
D410L	4 to 10 Decoder, Output Active Lo
M154C	4 to 16 Decoder (74LS154)
DM6JH	Spike Free Decoder for MOD 6 Johnson Counter, Active Hi
DM6JL	Spike Free Decoder for MOD 6 Johnson Counter, Active Lo
DM8JH	Spike Free Decoder for MOD 8 Johnson Counter, Active Hi
DM8JL	Spike Free Decoder for MOD 8 Johnson Counter, Active Lo
DM10JH	Spike Free Decoder for MOD 10 Johnson Counter, Active Hi
DM10JL	Spike Free Decoder for MOD 10 Johnson Counter, Active Lo
DM12JH	Spike Free Decoder for MOD 12 Johnson Counter, Active Hi
DM12JL	Spike Free Decoder for MOD 12 Johnson Counter, Active Lo
DM14JH	Spike Free Decoder for MOD 14 Johnson Counter, Active Hi
DM14JL	Spike Free Decoder for MOD 14 Johnson Counter, Active Lo
DM16JH	Spike Free Decoder for MOD 16 Johnson Counter, Active Hi
DM16JL	Spike Free Decoder for MOD 16 Johnson Counter, Active Lo
M43C	Excess-3 to Decimal Decoder (7443)
M44C	Excess-3 Gray to Decimal Decoder (74LS44)
M47C	Bcd to 7 Segment Decoder/Driver (74LS47)
M49C	Bcd to 7 Segment Decoder/Driver (74LS49)
M42C	Bcd to Decimal Decoder (7442)
M145C	Bcd to Decimal Decoder (74LS145)
M4028C	Bcd to Decimal Decoder (4028)

MULTIPLEXER

M298C	Quad 2-Input Multiplexer with Storage (74LS298)
M157C	Quad 2 Bit Gated Non Inverting Mux
M158C	Quad 2 Bit Gated Inverting Mux
M153C	Dual 4 Bit Gated Non Inverting Mux
M151C	8 Bit Gated Mux
M152C	8 Bit Inverting Mux
M150C	16 Bit Gated Inverting Mux (74LS150)
MUX31H	3 Bit Non Inverting Mux
MUX31L	3 Bit Inverting Mux
MUX41H	4 Bit Non Inverting Mux
MUX41GH	4 Bit Gated Non Inverting Mux
MUX41L	4 Bit Inverting Mux
MUX51H	5 Bit Non Inverting Mux
MUX51L	5 Bit Inverting Mux
MUX61H	6 Bit Non Inverting Mux
MUX61L	6 Bit Inverting Mux
MUX71H	7 Bit Non Inverting Mux
MUX71L	7 Bit Inverting Mux
MUX81H	8 Bit Non Inverting Mux
MUX22H	Dual 2 Bit Non Inverting Mux
MUX32H	Dual 3 Bit Non Inverting Mux
MUX42H	Dual 4 Bit Non Inverting Mux
MUX52H	Dual 5 Bit Non Inverting Mux
MUX62H	Dual 6 Bit Non Inverting Mux
MUX72H	Dual 7 Bit Non Inverting Mux
MUX82H	Dual 8 Bit Non Inverting Mux
MUX24H	Quad 2 Bit Non Inverting Mux
MUX24L	Quad 2 Bit Inverting Mux
MUX34H	Quad 3 Bit Non Inverting Mux
MUX44H	Quad 4 Bit Non Inverting Mux
MUX54H	Quad 5 Bit Non Inverting Mux
MUX64H	Quad 6 Bit Non Inverting Mux
MUX74H	Quad 7 Bit Non Inverting Mux
MUX84H	Quad 8 Bit Non Inverting Mux


COUNTER
MULTIPLEX REGISTER
MR41 4 Bit Register with 2 Bit Multiplexed Input
MR42 4 Bit Register with 2 Bit Multiplexed Input, Clear Direct
MR43 4 Bit Register with 2 Bit Multiplexed Input, Sync Clear
MR44 4 Bit Register with 2 Bit Multiplexed Input, Sync Clear Reset B
MR81 8 Bit Register with 2 Bit Multiplexed Input
MR82 8 Bit Register with 2 Bit Multiplexed Input, Clear Direct
MODULO JOHNSON COUNTER
CM4J Modulo 4, Johnson Counter, Clear Direct
CM6J Modulo 6, Johnson Counter, Clear Direct
CM8J Modulo 8, Johnson Counter, Clear Direct
CM10J Modulo 10, Johnson Counter, Clear Direct
CM12J Modulo 12, Johnson Counter, Clear Direct
CM14J Modulo 14, Johnson Counter, Clear Direct
CM16J Modulo 16, Johnson Counter, Clear Direct
MODULO GRAY COUNTER
C2G Modulo 4, Gray Counter, Clear Direct
C3G Modulo 8, Gray Counter, Clear Direct
C4G Modulo 16, Gray Counter, Clear Direct
C5G Modulo 32, Gray Counter, Clear Direct
C6G Modulo 64, Gray Counter, Clear Direct, Prescaled
C7G Modulo 128, Gray Counter, Clear Direct, Prescaled
C8G Modulo 256, Gray Counter, Clear Direct, Prescaled
MODULO BINARY COUNTER
CM3B Modulo 3, Binary Counter, Clear Direct
CM4B Modulo 4, Binary Counter, Clear Direct
CM5B Modulo 5, Binary Counter, Clear Direct
CM6B Modulo 6, Binary Counter, Clear Direct
CM7B Modulo 7, Binary Counter, Clear Direct
CM8B Modulo 8, Binary Counter, Clear Direct
CM9B Modulo 9, Binary Counter, Clear Direct
CM10B Modulo 10, Binary Counter, Clear Direct
CM11B Modulo 11, Binary Counter, Clear Direct
CM12B Modulo 12, Binary Counter, Clear Direct
CM13B Modulo 13, Binary Counter, Clear Direct
CM14B Modulo 14, Binary Counter, Clear Direct
CM15B Modulo 15, Binary Counter, Clear Direct
CM16B Modulo 16, Binary Counter, Clear Direct
CM17B Modulo 17, Binary Counter, Clear Direct
MODULO BINARY RIPPLE COUNTER
CM8BR Modulo 8, Binary Ripple Counter, Clear Direct
CM9BR Modulo 9, Binary Ripple Counter, Clear Direct
CM10BR Modulo 10, Binary Ripple Counter, Clear Direct
CM11BR Modulo 11, Binary Ripple Counter, Clear Direct
CM12BR Modulo 12, Binary Ripple Counter, Clear Direct
CM13BR Modulo 13, Binary Ripple Counter, Clear Direct
CM14BR Modulo 14, Binary Ripple Counter, Clear Direct
CM15BR Modulo 15, Binary Ripple Counter, Clear Direct
CM16BR Modulo 16, Binary Ripple Counter, Clear Direct
CM17BR Modulo 17, Binary Ripple Counter, Clear Direct
CM18BR Modulo 18, Binary Ripple Counter, Clear Direct
CM19BR Modulo 19, Binary Ripple Counter, Clear Direct
CM20BR Modulo 20, Binary Ripple Counter, Clear Direct
CM21BR Modulo 21, Binary Ripple Counter, Clear Direct
CM22BR Modulo 22, Binary Ripple Counter, Clear Direct
CM23BR Modulo 23, Binary Ripple Counter, Clear Direct
CM24BR Modulo 24, Binary Ripple Counter, Clear Direct
CM25BR Modulo 25, Binary Ripple Counter, Clear Direct
CM26BR Modulo 26, Binary Ripple Counter, Clear Direct
CM27BR Modulo 27, Binary Ripple Counter, Clear Direct
CM28BR Modulo 28, Binary Ripple Counter, Clear Direct
CM29BR Modulo 29, Binary Ripple Counter, Clear Direct
CM30BR Modulo 30, Binary Ripple Counter, Clear Direct
CM31BR Modulo 31, Binary Ripple Counter, Clear Direct
CM32BR Modulo 32, Binary Ripple Counter, Clear Direct
MODULO SHIFT COUNTER
CM5SR Modulo 5, Shift Counter, Clear Direct
CM8SR Modulo 8, Shift Counter, Clear Direct
CM9SR Modulo 9, Shift Counter, Clear Direct
CM10SR Modulo 10, Shift Counter, Clear Direct
CM12SR Modulo 12, Shift Counter, Clear Direct



MODULO BINARY UP COUNTER	CB41	Modulo 16, Binary Up Counter, Expandable Enable Clear Direct
	CB42	Modulo 16, Binary Up Counter, Expandable Enable Sync Clear
	CB4C	Modulo 16, Binary Up Counter Fast, Sync Clear
	CB5C	Modulo 32, Binary Up Counter Fast, Sync Clear
	CB6C	Modulo 64, Binary Up Counter Fast, Sync Clear
	CB7C	Modulo 128, Binary Up Counter Fast, Sync Clear
	CB8C	Modulo 256, Binary Up Counter Fast, Sync Clear
	CB4F	Modulo 16, Binary Up Counter Fast, Individual Reset B & Set B
	CB5F	Modulo 32, Binary Up Counter Fast, Individual Reset B & Set B
	CB6F	Modulo 64, Binary Up Counter Fast, Individual Reset B & Set B
	CB7F	Modulo 128, Binary Up Counter Fast, Individual Reset B & Set B
	CB8F	Modulo 256, Binary Up Counter Fast, Individual Reset B & Set B
MODULO UP/DOWN COUNTER	CUD41	Modulo 16, Up/Down Counter, Expandable Enable Clear Direct
	CUD42	Modulo 16, Up/Down Counter, Expandable with Asynchronous Load and Clear
SYNCHRONOUS COUNTER	M161C	Synchronous 4 Bit Binary Counter (74LS161)
	M161D	Synchronous 4 Bit Binary Counter (74LS161)
	M163C	Synchronous 4 Bit Binary Counter (74LS163)
	M163D	Synchronous 4 Bit Binary Counter (74LS163)
	M163F	Synchronous 4 Bit Binary Counter, Optimized for Max Clock Freq
	M160C	Synchronous 4 Bit Bcd Counter (74LS160)
	M160D	Synchronous 4 Bit Bcd Counter (74LS160)
	M162C	Synchronous 4 Bit Bcd Counter (74LS162)
	M162D	Synchronous 4 Bit Bcd Counter (74LS162)
	M169C	Synchronous 4 Bit Up/Down Counter (74LS169)
MODULO LINEAR FEEDBACK SHIFT REGISTER	C3LSR	Modulo 7, Linear Feedback Shift Register
	C4LSR	Modulo 15, Linear Feedback Shift Register
	C5LSR	Modulo 31, Linear Feedback Shift Register
	C6LSR	Modulo 63, Linear Feedback Shift Register
	C7LSR	Modulo 127, Linear Feedback Shift Register
	C8LSR	Modulo 255, Linear Feedback Shift Register
CLOCK PRESCALER	PS2	Divide by 2 External Clock Prescaler with No Input Protection
	PS3	Divide by 3 External Clock Prescaler with No Input Protection
	PS4	Divide by 4 External Clock Prescaler with No Input Protection
TTL / CMOS MSI	M90C	Decade Counter (74LS390)
	M92C	Divided by Twelve Counter (74LS92)
	M93C	4 Bit Binary Counter (74LS93)
	M197C	Presetable 4 Bit Binary Counter (74LS197)
	M390C	Decade Counter (74LS390)
	M393C	4 Bit Binary Counter
	M4017C	Decade Counter/Driver (4017)
	M4520C	Dual Binary Up Counter

CMOS Gate Array 5GF Series

Outline

The Ricoh gate array 5GF series complies with the CMOS 1.5μ rule, and offers high speed operation with a gate delay time of 1.0 ns.

The 5GF series inherits the rich library of the 5GH series, and the SRAM and mask ROM can be used as a memory cell. The cell library is compatible with standard cell RSC-15 series. It enables LSI development to suit any system and production scale.

Features

1. **Number of gates**

   6 types, from 2100 to 8200 gates

2. **High speed operation (CMOS 1.5μ design rule)**

   Gate delay time ..... 1.0 ns (Typ.)
   I/O cell delay time ..... 3.0 ns (Typ.)
   SRAM access time ..... 55 ns (Max.)
   Mask ROM access time.... 60 ns (Max.)
   *Typ.: F.O. = 3, wiring length = 3 mm

3. **Extensive cell library**

   Macro cell ..... 137 types
   Macro function cell ..... 251 types
   Total ..... 388 types

   This library is perfectly compatible with the cell library of the conventional gate array 5GH series and the standard cell RSC-15 series. It is easy to convert from the gate array to the standard cell.

4. **Memory cell**

   The SRAM and the mask ROM can be used as a memory cell. The memory and the logic circuit can be configured on one chip.

5. **Test cell**

   10 types of scan-path format test cells are prepared.

6. **Perfect design support by CAD**

   As a user design tool, the 5GF series supports the user with a system based on IBM-PC, logic diagram generation software, and logic simulation software (DASH-CADAT system). The series can interface with EWS of MENTOR Co. and DAISY Co.

   DASH and CADAT are registered trade mark of FutureNet Co. and HHB-Systems Co.

■ Absolute Maximum Ratings

Symbol	Parameter	Condition	Value	Unit
Vcc	Power supply voltage	for GND	−0.3 ~ 7	V
VI	Input voltage		−0.3 ~ Vcc + 0.3	V
VO	Output voltage		−0.3 ~ Vcc + 0.3	V
Topr	Operating temperature		−40 ~ 85	°C
Tstg	Storage temperature		−55 ~ 125	°C

■ Recommended Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Power supply voltage	4.75	5.00	5.25	V
Ta	Operating temperature	0	25	70	°C

■ DC Characteristics

(Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

Symbol	Parameter	Condition	Value			Unit
			Min.	Typ.	Max.	
VIH	"H" input voltage (TTL)		2.2		Vcc + 0.3	V
VIL	"L" input voltage (TTL)		−0.3		0.8	V
VIH	"H" input voltage (CMOS)		Vcc x 0.7		Vcc + 0.3	V
VIL	"L" input voltage (CMOS)		−0.3		Vcc x 0.3	V
VOH	"H" output voltage	IOH = −4mA	2.4			V
VOL	"L" output voltage	IOL = 4mA			0.4	V
ILI	Input current	VI = 0 ~ Vcc	−10		10	μA
IOZ	Output current for off state	VO = 0 ~ Vcc	−10		10	μA
Icc	Power supply current			*		mA

* Power supply current depends on gete number, clock frequency.

■ AC Characteristics

(Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

Symbol	Parameter	Condition	Value			Unit
			Min.	Typ.	Max.	
Tpdo	I/O output delay time	CL = 15pF		3.0		ns
Tpdi	I/O input delay time	FO = 3, Wire length = 3mm		3.0		ns
Tpd	Inner gate delay time	FO = 3, Wire length = 3mm		1.0		ns

■ Memory Cell DC Characteristics

(Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

Memory	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
SRAM	Icc1	Stand-by current			50	μA/4bit
	Icc2	Operation current		16	30	mA/4bit
MaskROM	Icc1	Stand-by current			50	μA/4bit
	Icc2	Operation current		10	20	mA/4bit

■ Memory Cell AC Characteristics

(Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
tACC	Address access time	(SRAM)			55	ns
		(Mask ROM)			60	ns

■5GF Series Line Up

Series			5GF21	5GF26	5GF32	5GF45	5GF58	5GF82
Gate number			2100	2600	3200	4500	5800	8200
Memory configuration *1	SRAM only (bit)	4-bit config.	4 x 512	4 x 512	4 x 512	4 x 1024	4 x 2048	4 x 2048
		8-bit config.	8 x 256	8 x 256	8 x 256	8 x 512	8 x 1024	8 x 1024
		16-bit config.				16 x 256	16 x 512	16 x 768
		24-bit config.						24 x 768
	Mask ROM only (bit)	4-bit config.	4 x 1024	4 x 1024	4 x 1024	4 x 2048	4 x 4096	4 x 4096
		8-bit config.	8 x 512	8 x 512	8 x 512	8 x 1024	8 x 2048	8 x 2048
		16-bit config.				16 x 512	16 x 1024	16 x 1536
		24-bit config.						24 x 1536
	Memory mix SRAM Mask ROM		4 x 256 4 x 512	4 x 256 4 x 512	4 x 256 4 x 512	8 x 256 8 x 512	8 x 512 8 x 1024	8 x 512 16 x 1024 16 x 512 8 x 1024
	Number of remaining gates (see *2)		290	660	1060	1050	1440	1980
Number of I/O (see *3)			84	94	102	120	138	168
Package	DIP		24, 28, 40, 48	24, 28, 40, 48	24, 28, 40, 48	24, 28, 40, 48	40, 48	
	Shrink DIP		42, 64	42, 64	42, 64	64	64	
	FLAT		44, 60, 64, 80, 100	44, 60, 64, 80, 100	44, 60, 64, 80, 100	44, 60, 64, 80, 100, 128*4	64, 80, 100, 128*4, 144*4, 160*4	80, 100, 128*4, 144*4, 160*4
	LCC		44, 68	44, 68, 84	44, 68, 84	44, 68, 84	44, 68, 84	44, 68, 84
	PLCC		28, 44, 68	28, 44, 68, 84	28, 44, 68, 84	28, 44, 68, 84	44, 68, 84	44, 68, 84

*1: The memory capacities noted above are the maximum values that can be mounted on the chip.

*2: The number of logic gates that can be mixed varies with the mounted memory capacity.

*3: Four of the I/O pads are dedicated to Vcc and GND.

*4: Under development.

■Development tool (for CAD interface)

Hardware

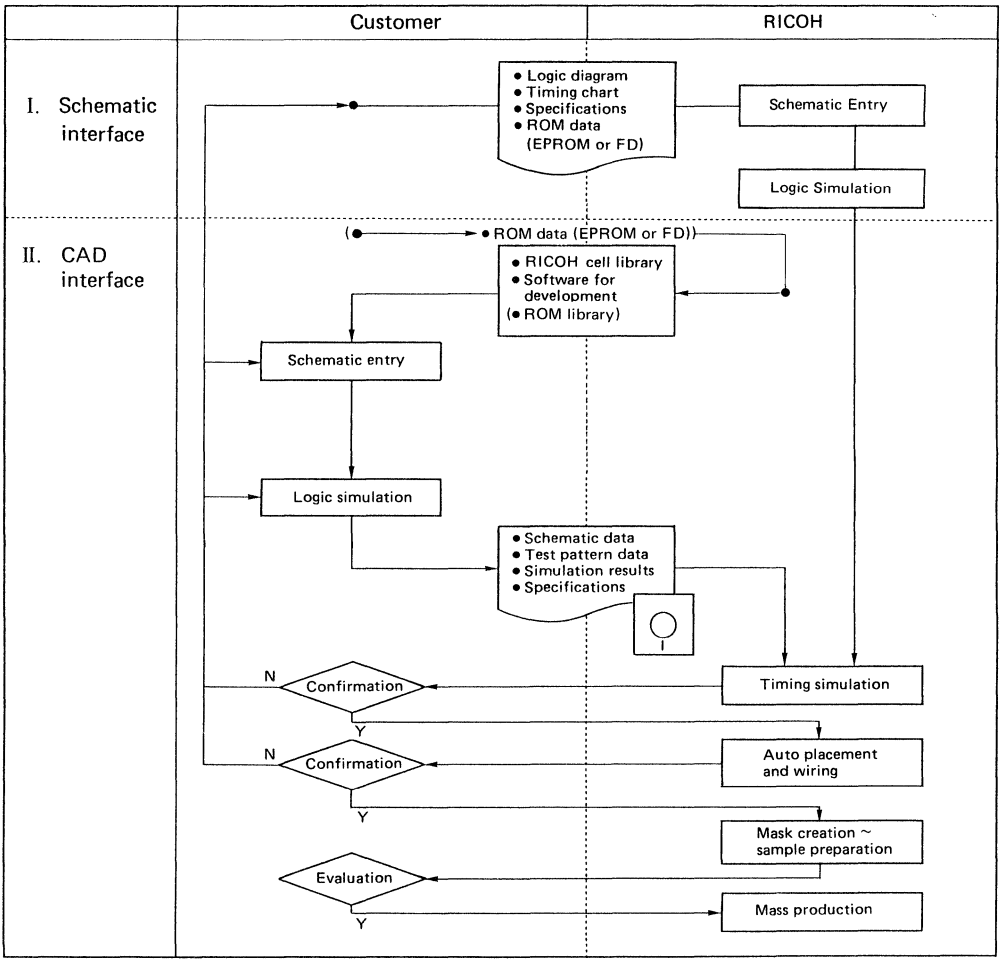
- EWS ..... LOGICIAN (Daisy)
  IDEA1000 (Mentor)
- Personal computer . IBM-PC/AT(IBM)
  - SW16 (Ricoh)

Software

- ◉ Ricoh cell library and simulation data
- ◉ Ricoh development software
- ◉ DASH, CADAT (Date I/O Co., only for development on personal computers)

◉ : sold by Ricoh

5GF Series Development Flow



Notice: Specifications in the data sheet are subject to change without notice.

■ 5GF MEMORY ARRANGEMENT

Using SRAM only

SRAM Specs.		Available Gate Count (Memory Structure Efficiency: Gate Count/Bits Count)					
Bit	Word	5GF21	5GF26	5GF32	5GF45	5GF58	5GF82
4	32	1120 (7.7)	1490 (8.9)	1890 (10.2)	2870 (13.4)	3710 (16.3)	5450 (22.1)
4	64	1070 (4.0)	1440 (4.6)	1840 (5.3)	2820 (6.9)	3660 (8.4)	5400 (11.3)
4	128	980 (2.2)	1340 (2.5)	1750 (2.8)	2720 (3.7)	3610 (4.3)	5350 (5.7)
4	256	780 (1.3)	1150 (1.4)	1550 (1.6)	2520 (2.0)	3470 (2.3)	5200 (3.0)
4	512	290 (0.9)	660 (1.0)	1060 (1.0)	2030 (1.3)	3220 (1.3)	4960 (1.6)
4	1024	( )	( )	( )	1050 (0.9)	2630 (0.8)	4360 (1.0)
4	2048	( )	( )	( )	( )	1440 (0.5)	3170 (0.6)
4		( )	( )	( )	( )	( )	( )
8	32	880 (4.8)	1240 (5.4)	1650 (6.0)	2620 (7.7)	3470 (9.1)	5200 (12.0)
8	64	790 (2.6)	1160 (2.9)	1560 (3.2)	2540 (4.0)	3380 (4.7)	5120 (6.2)
8	128	630 (1.4)	990 (1.6)	1400 (1.8)	2370 (2.2)	3300 (2.4)	5040 (3.2)
8	256	290 (0.9)	660 (1.0)	1060 (1.0)	2030 (1.3)	3050 (1.3)	4780 (1.7)
8	512	( )	( )	( )	1060 (0.9)	2630 (0.8)	4360 (1.0)
8	1024	( )	( )	( )	( )	1440 (0.5)	3170 (0.6)
8		( )	( )	( )	( )	( )	( )
16	32	( )	( )	( )	2130 (4.8)	2980 (5.5)	4710 (7.0)
16	64	( )	( )	( )	1980 (2.5)	2820 (2.9)	4560 (3.6)
16	128	( )	( )	( )	1670 (1.4)	2670 (1.5)	4410 (1.9)
16	256	( )	( )	( )	1050 (0.9)	2210 (0.9)	3940 (1.0)
16	512	( )	( )	( )	( )	1440 (0.5)	3170 (0.6)
16	768	( )	( )	( )	( )	( )	2400 (0.5)
16		( )	( )	( )	( )	( )	( )
24	32	( )	( )	( )	( )	( )	4200 (5.3)
24	64	( )	( )	( )	( )	( )	3970 (2.8)
24	128	( )	( )	( )	( )	( )	3740 (1.5)
24	256	( )	( )	( )	( )	( )	3020 (0.9)
24	512	( )	( )	( )	( )	( )	1860 (0.5)
24	768	( )	( )	( )	( )	( )	710 (0.4)

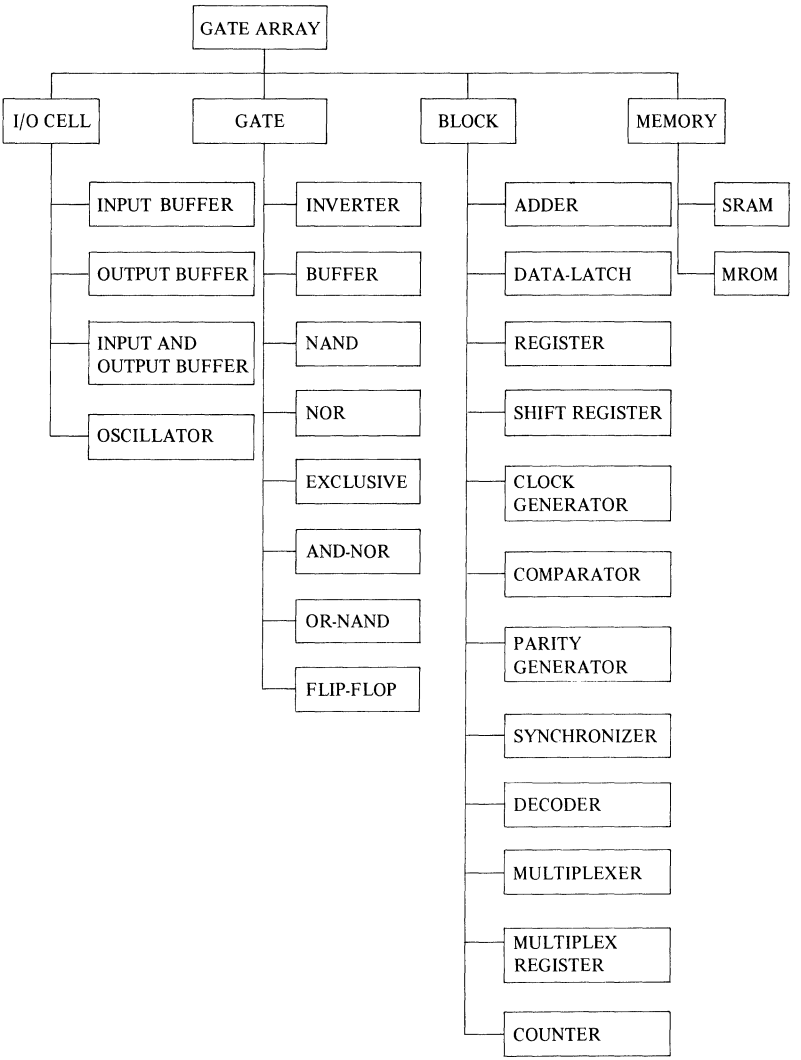
Note: If no value is found under "Available Gate Count", those memory specifications are not possible.

Using MROM only

MROM Specs.		Available Gate Count (Memory Structure Efficiency: Gate Count/Bits Count)					
Bit	Word	5GF21	5GF26	5GF32	5GF45	5GF58	5GF82
4	128	1070 (2.0)	1440 (2.3)	1840 (2.7)	2820 (3.5)	3660 (4.2)	5400 (5.6)
4	256	980 (1.1)	1340 (1.3)	1750 (1.4)	2720 (1.8)	3610 (2.1)	5350 (2.9)
4	512	780 (0.6)	1150 (0.7)	1550 (0.8)	2520 (1.0)	3470 (1.1)	5200 (1.5)
4	1024	290 (0.4)	660 (0.5)	1060 (0.5)	2030 (0.6)	3220 (0.6)	4960 (0.8)
4	2048	( )	( )	( )	1050 (0.4)	2630 (0.4)	4360 (0.5)
4	4096	( )	( )	( )	( )	1440 (0.3)	3170 (0.3)
4		( )	( )	( )	( )	( )	( )
4		( )	( )	( )	( )	( )	( )
8	128	790 (1.3)	1160 (1.4)	1560 (1.6)	2540 (2.0)	3380 (2.4)	5120 (3.1)
8	256	630 (0.7)	990 (0.8)	1400 (0.9)	2370 (1.1)	3300 (1.2)	5040 (1.6)
8	512	290 (0.4)	660 (0.5)	1060 (0.5)	2030 (0.6)	3050 (0.7)	4780 (0.9)
8	1024	( )	( )	( )	1050 (0.4)	2630 (0.4)	4360 (0.5)
8	2048	( )	( )	( )	( )	1440 (0.3)	3170 (0.3)
8		( )	( )	( )	( )	( )	( )
8		( )	( )	( )	( )	( )	( )
16	128	( )	( )	( )	1980 (1.3)	2820 (1.5)	4560 (1.8)
16	256	( )	( )	( )	1670 (0.7)	2670 (0.8)	4410 (0.9)
16	512	( )	( )	( )	1050 (0.4)	2210 (0.4)	3940 (0.5)
16	1024	( )	( )	( )	( )	1440 (0.3)	3170 (0.3)
16	1536	( )	( )	( )	( )	( )	2400 (0.2)
16		( )	( )	( )	( )	( )	( )
16		( )	( )	( )	( )	( )	( )
24	128	( )	( )	( )	( )	( )	3970 (1.4)
24	256	( )	( )	( )	( )	( )	3740 (0.7)
24	512	( )	( )	( )	( )	( )	3020 (0.4)
24	1024	( )	( )	( )	( )	( )	1860 (0.3)
24	1536	( )	( )	( )	( )	( )	710 (0.2)
24		( )	( )	( )	( )	( )	( )

Note: If no value is found under "Available Gate Count", those memory specifications are not possible.

CMOS GATE ARRAY 5GF series
CELL LIST



I/O CELL

INPUT BUFFER — STANDARD

CELL	FUNCTION	
INT01	TTL Compatible	Inverter
INT02	TTL	Buffer
INTSCH	TTL	Schmitt Trigger
INC01	CMOS Compatible	Inverter
INC02	CMOS	Buffer
INCSCH	CMOS	Schmitt Trigger

INPUT BUFFER — with Resistance for pull-up

INT1U1	TTL Compatible	Inverter
INT2U1	TTL	Buffer
INTSU1	TTL	Schmitt Trigger
INC1U1	CMOS Compatible	Inverter
INC2U1	CMOS	Buffer
INCSU1	CMOS	Schmitt Trigger

INPUT BUFFER — with Resistance for pull-down

INT1D1	TTL Compatible	Inverter
INT2D1	TTL	Buffer
INTSD1	TTL	Schmitt Trigger
INC1D1	CMOS Compatible	Inverter
INC2D1	CMOS	Buffer
INCSD1	CMOS	Schmitt Trigger

OUTPUT BUFFER

OUTINV	Inverter
OUTTRI	3-State Output
OUTOPN	Open Drain Output

OUTPUT AND INPUT BUFFER — STANDARD

IOT01 IOT1	TTL Compatible	Inverter & 3-State Output
IOT02 IOT2	TTL Compatible	Buffer & 3-State Output
IOTSCH IOTSH	TTL Compatible	Schmitt Trigger & 3-State Output
IOC01 IOC1	CMOS Compatible	Inverter & 3-State Output
IOC02 IOC2	CMOS Compatible	Buffer & 3-State Ouptut
IOCSCH IOCSH	CMOS Compatible	Schmitt Trigger & 3-State Output

OUTPUT AND INPUT BUFFER — with Resistance for pull-up

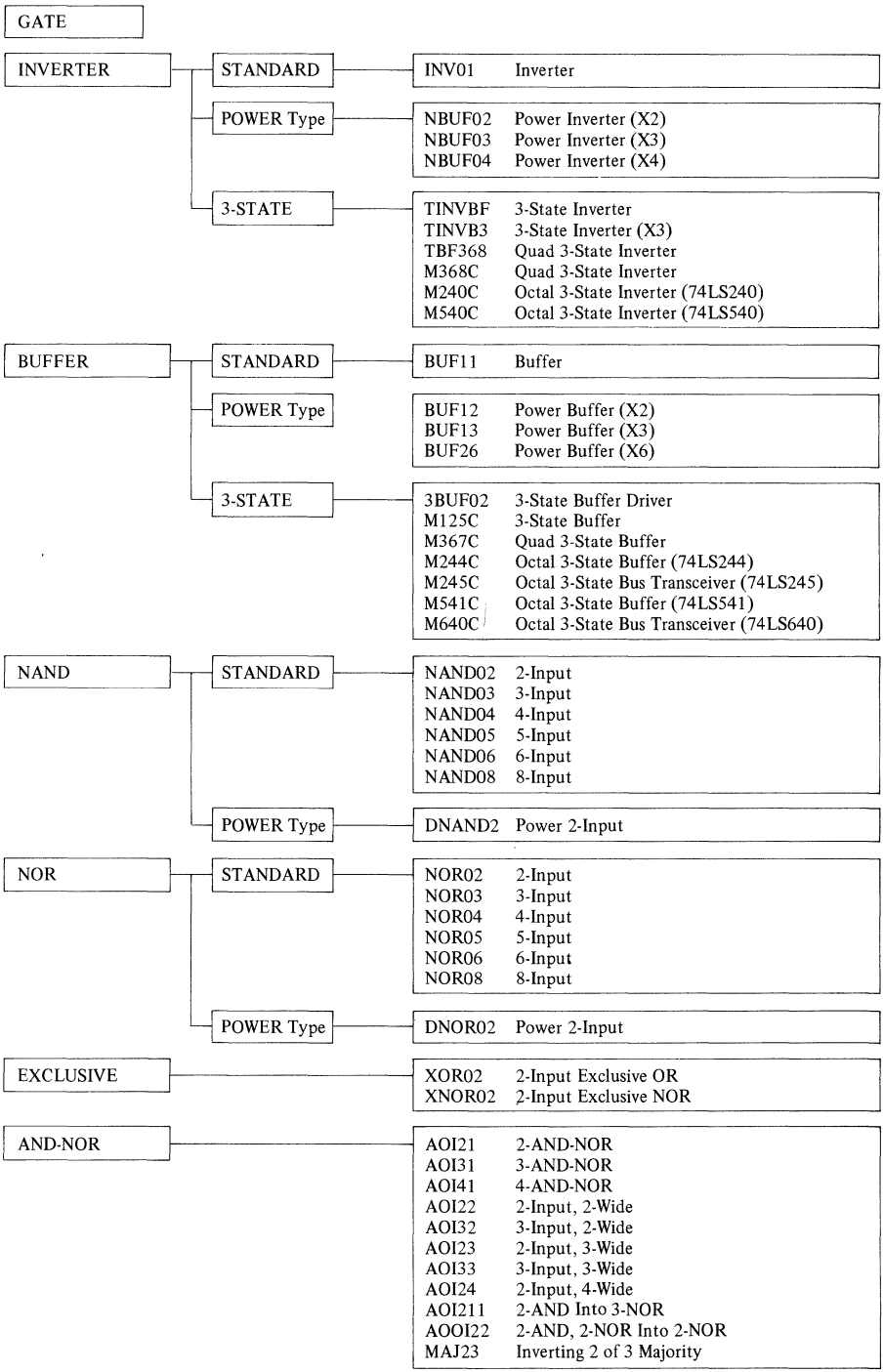
IOT1U1 IOTU1	TTL Compatible	Inverter & 3-State Output
IOT2U1	TTL Compatible	Buffer & 3-State Output
IOC1U1 IOCU1	CMOS Compatible	Inverter & 3-State Output
IOC2U1	CMOS Compatible	Buffer & 3-State Output

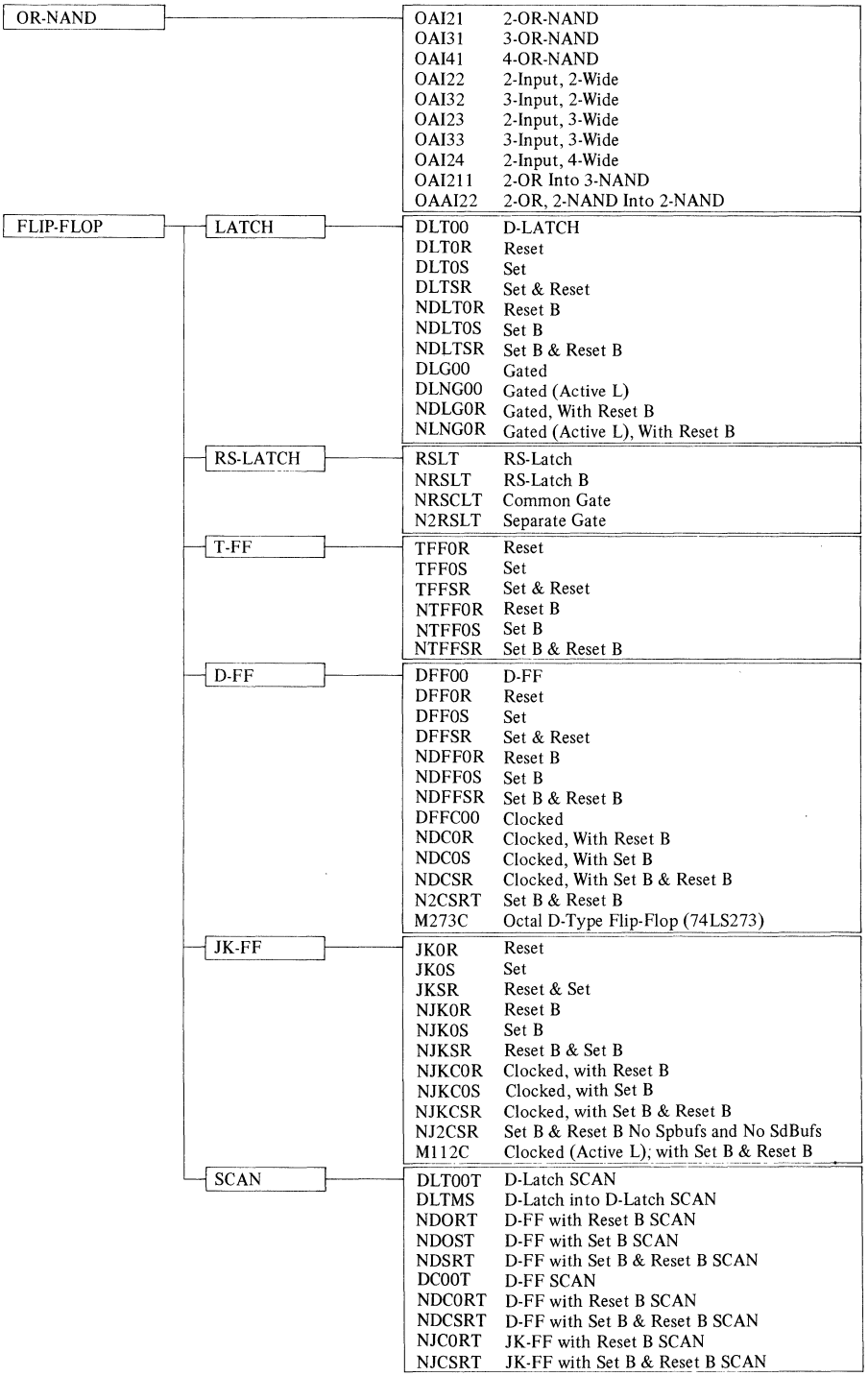
OUTPUT AND INPUT BUFFER — with Resistance for pull-down

IOT1D1 IOTD1	TTL Compatible	Inverter & 3-State Ouptut
IOC1D1 IOCD1	CMOS Compatible	Inverter & 3-State Output

OSCILLATOR

XIN01	Input
XOUT	Oscillator Output
XIO	Oscillator


GATE
INVERTER
STANDARD
INV01 Inverter
POWER Type
NBUF02 Power Inverter (X2)
NBUF03 Power Inverter (X3)
NBUF04 Power Inverter (X4)
3-STATE
TINVBF 3-State Inverter
TINVB3 3-State Inverter (X3)
TBF368 Quad 3-State Inverter
M368C Quad 3-State Inverter
M240C Octal 3-State Inverter (74LS240)
M540C Octal 3-State Inverter (74LS540)
BUFFER
STANDARD
BUF11 Buffer
POWER Type
BUF12 Power Buffer (X2)
BUF13 Power Buffer (X3)
BUF26 Power Buffer (X6)
3-STATE
3BUF02 3-State Buffer Driver
M125C 3-State Buffer
M367C Quad 3-State Buffer
M244C Octal 3-State Buffer (74LS244)
M245C Octal 3-State Bus Transceiver (74LS245)
M541C Octal 3-State Buffer (74LS541)
M640C Octal 3-State Bus Transceiver (74LS640)
NAND
STANDARD
NAND02 2-Input
NAND03 3-Input
NAND04 4-Input
NAND05 5-Input
NAND06 6-Input
NAND08 8-Input
POWER Type
DNAND2 Power 2-Input
NOR
STANDARD
NOR02 2-Input
NOR03 3-Input
NOR04 4-Input
NOR05 5-Input
NOR06 6-Input
NOR08 8-Input
POWER Type
DNOR02 Power 2-Input
EXCLUSIVE
XOR02 2-Input Exclusive OR
XNOR02 2-Input Exclusive NOR
AND-NOR
AOI21 2-AND-NOR
AOI31 3-AND-NOR
AOI41 4-AND-NOR
AOI22 2-Input, 2-Wide
AOI32 3-Input, 2-Wide
AOI23 2-Input, 3-Wide
AOI33 3-Input, 3-Wide
AOI24 2-Input, 4-Wide
AOI211 2-AND Into 3-NOR
AOOI22 2-AND, 2-NOR Into 2-NOR
MAJ23 Inverting 2 of 3 Majority


OR-NAND
OAI21 2-OR-NAND
OAI31 3-OR-NAND
OAI41 4-OR-NAND
OAI22 2-Input, 2-Wide
OAI32 3-Input, 2-Wide
OAI23 2-Input, 3-Wide
OAI33 3-Input, 3-Wide
OAI24 2-Input, 4-Wide
OAI211 2-OR Into 3-NAND
OAAI22 2-OR, 2-NAND Into 2-NAND
FLIP-FLOP
LATCH
DLT00 D-LATCH
DLT0R Reset
DLT0S Set
DLTSR Set & Reset
NDLT0R Reset B
NDLT0S Set B
NDLTSR Set B & Reset B
DLG00 Gated
DLNG00 Gated (Active L)
NDLG0R Gated, With Reset B
NLNG0R Gated (Active L), With Reset B
RS-LATCH
RSLT RS-Latch
NRSLT RS-Latch B
NRSCLT Common Gate
N2RSLT Separate Gate
T-FF
TFF0R Reset
TFF0S Set
TFFSR Set & Reset
NTFF0R Reset B
NTFF0S Set B
NTFFSR Set B & Reset B
D-FF
DFF00 D-FF
DFF0R Reset
DFF0S Set
DFFSR Set & Reset
NDFF0R Reset B
NDFF0S Set B
NDFFSR Set B & Reset B
DFFC00 Clocked
NDC0R Clocked, With Reset B
NDC0S Clocked, With Set B
NDCSR Clocked, With Set B & Reset B
N2CSRT Set B & Reset B
M273C Octal D-Type Flip-Flop (74LS273)
JK-FF
JK0R Reset
JK0S Set
JKSR Reset & Set
NJK0R Reset B
NJK0S Set B
NJKSR Reset B & Set B
NJKC0R Clocked, with Reset B
NJKC0S Clocked, with Set B
NJKCSR Clocked, with Set B & Reset B
NJ2CSR Set B & Reset B No Spbufs and No SdBufs
M112C Clocked (Active L); with Set B & Reset B
SCAN
DLT00T D-Latch SCAN
DLTMS D-Latch into D-Latch SCAN
NDORT D-FF with Reset B SCAN
NDOST D-FF with Set B SCAN
NDSRT D-FF with Set B & Reset B SCAN
DC00T D-FF SCAN
NDC0RT D-FF with Reset B SCAN
NDCSRT D-FF with Set B & Reset B SCAN
NJC0RT JK-FF with Reset B SCAN
NJCSRT JK-FF with Set B & Reset B SCAN

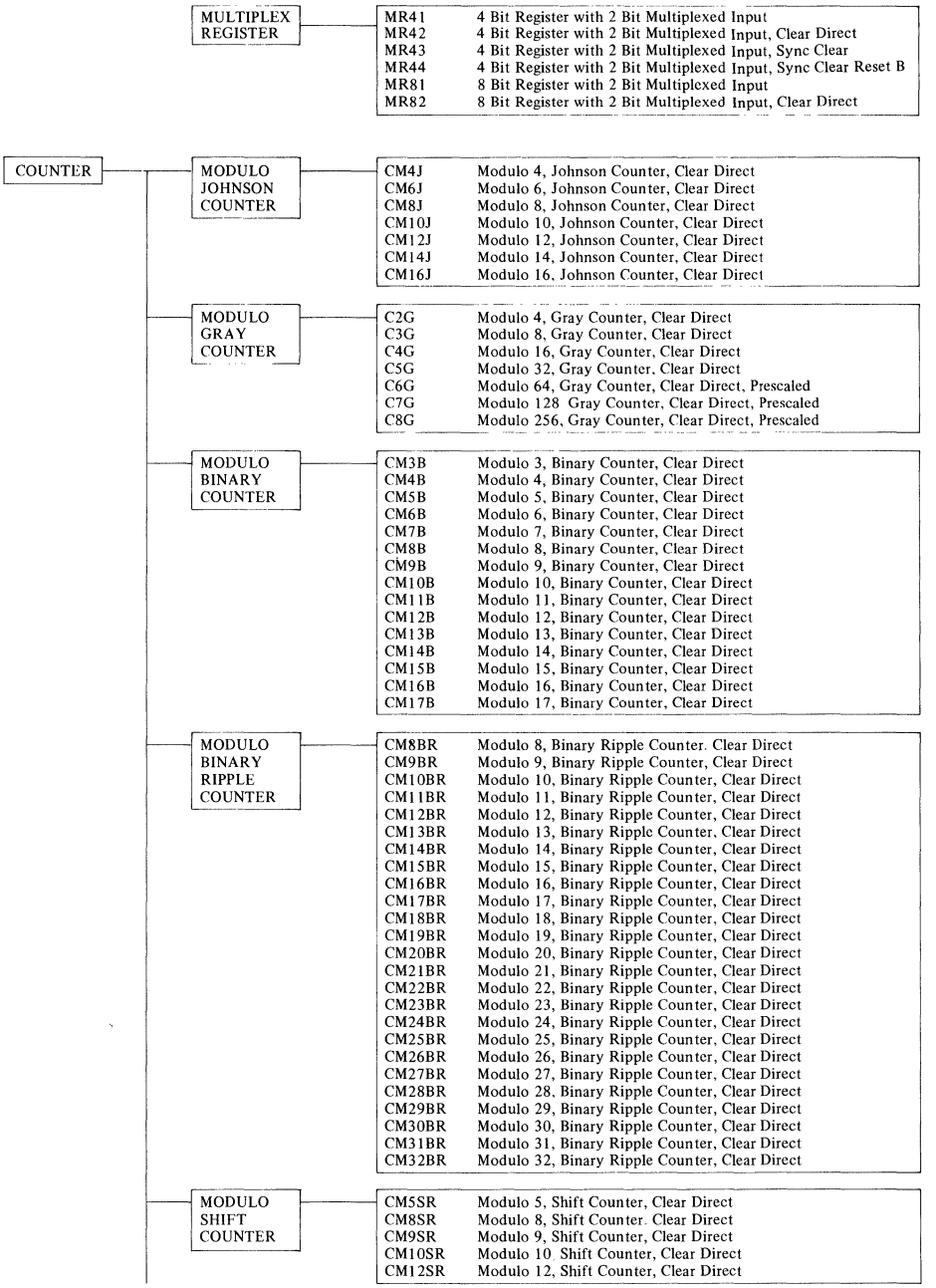
BLOCK		
ADDER	HA1	Half Adder
	FA1	Full Adder
	M80C	Gated Full Adder (7480)
	FA2	2 Bit Binary Full Adder
	FAS2	2 Bit Binary 2's Complement Full Adder, or Substractor
	M82C	2 Bit Binary Full Adder (7482)
	FA4	4 Bit Binary Full Adder
	M83C	4 Bit Binary Full Adder with Fast Carry (74LS83)
	CLA1	Carry Look Ahead for 4 Bit Adder (Least Significant Nibble)
	CLA2	Carry Look Ahead for 4 Bit Adder
	FA16	16 Bit Fast Adder
DATA-LATCH	L4	4 Bit Data Latch
	L8	8 Bit Data Latch
REGISTER	R41	4 Bit Data Register
	R42	4 Bit Data Register, Clear Direct
	R81	8 Bit Data Register
	R82	8 Bit Data Register, Clear Direct
SHIFT REGISTER	SR41	4 Bit Shift Register
	SR42	4 Bit Shift Register, Clear Direct
	M95C	4 Bit Shift Register (74LS95)
	SR43	4 Bit Shift Register, Set Direct
	SR44	4 Bit Shift Register, Synchronous Parallel Load
	SR45	4 Bit Shift Register, Synchronous Parallel Load and Clear
	SR46	4 Bit Shift Register, Asynchronous Parallel Load
	SR47	4 Bit Shift Register, Sync Clear
	M94C	4 Bit Shift Register (7494)
	M179C	4 Bit Parallel Access Shift Register (74179)
	M195C	4 Bit Parallel-Access Shift Register (74LS195)
	M96C	5 Bit Shift Register (74LS96)
	M91C	8 Bit Shift Register (74LS91)
	M164C	8 Bit Parallel Output Serial Shift Register (74LS164)
	M165C	Parallel Load 8 Bit Shift Register (74LS165)
	M166C	8 Bit Shift Register (74LS166)
	M198C	8 Bit Bidirectional Universal Shift Register (74198)
	M199C	8 Bit Bidirectional Universal Shift Register (74199)
CLOCK GENERATOR	CPG1	Two Phase Clock Generator, Unbuffered, Hi Underlap, Lo Drive
	CPG2	Two Phase Clock Generator, Unbuffered, Lo Underlap, Lo Drive
	CPG3	Two Phase Clock Generator, Unbuffered, Hi Underlap, Hi Drive
	CPG4	Two Phase Clock Generator, Unbuffered, Lo Underlap, Hi Drive
COMPARATOR	MAG2H	2 Bit Magnitude Comparator
	MAG2	2 Bit Extendable Magnitude Comparator
	MAG4	4 Bit Extendable Magnitude Comparator
	CMP4	4 Bit Equality Comparator
	M85C	4 Bit Magnitude Comparator Expandable
	CMP8	8 Bit Equality Comparator
PARITY GENERATOR	PAR8	8 Bit Odd Parity Detector
	PAR9	9 Bit Odd Parity Detector
	M180C	9 Bit Odd/Even Parity Generator (74180)
SYNCHRONIZER	SYNC01	Synchronizer for Asynchronous 0 to 1 Event
	SYNC10	Synchronizer for Asynchronous 1 to 0 Event

DECODER

M4555C	Binary to 1 of 4 Decoder
M139C	2 to 4 Decoder (74LS139)
M155C	Dual 2 to 4 Decoders
D24H	2 to 4 Decoder, Output Active Hi
D24L	2 to 4 Decoder, Output Active Lo
D24GH	2 to 4 Decoder, Gated Output Active Hi
D24GL	2 to 4 Decoder, Gated Output Active Lo
D38H	3 to 8 Decoder, Output Active Hi
D38L	3 to 8 Decoder, Output Active Lo
D38GH	3 to 8 Decoder, Gated Output Active Hi
D38GL	3 to 8 Decoder, Gated Output Active Lo
M138C	Gated 3 to 8 Decoder (74LS138)
M138D	Gated 3 to 8 Decoder (74LS138)
D410H	4 to 10 Decoder, Output Active Hi
D410L	4 to 10 Decoder, Output Active Lo
M154C	4 to 16 Decoder (74LS154)
DM6JH	Spike Free Decoder for MOD 6 Johnson Counter, Active Hi
DM6JL	Spike Free Decoder for MOD 6 Johnson Counter, Active Lo
DM8JH	Spike Free Decoder for MOD 8 Johnson Counter, Active Hi
DM8JL	Spike Free Decoder for MOD 8 Johnson Counter, Active Lo
DM10JH	Spike Free Decoder for MOD 10 Johnson Counter, Active Hi
DM10JL	Spike Free Decoder for MOD 10 Johnson Counter, Active Lo
DM12JH	Spike Free Decoder for MOD 12 Johnson Counter, Active Hi
DM12JL	Spike Free Decoder for MOD 12 Johnson Counter, Active Lo
DM14JH	Spike Free Decoder for MOD 14 Johnson Counter, Active Hi
DM14JL	Spike Free Decoder for MOD 14 Johnson Counter, Active Lo
DM16JH	Spike Free Decoder for MOD 16 Johnson Counter, Active Hi
DM16JL	Spike Free Decoder for MOD 16 Johnson Counter, Active Lo
M43C	Excess-3 to Decimal Decoder (7443)
M44C	Excess-3 Gray to Decimal Decoder (74LS44)
M47C	Bcd to 7 Segment Decoders/Drivers (74LS47)
M49C	Bcd to 7 Segment Decoders/Drivers (74LS49)
M42C	Bcd to Decimal Decoder (7442)
M145C	Bcd to Decimal Decoder (74LS145)
M4028C	Bcd to Decimal Decoder (4028)

MULTIPLEXER

M298C	Quad 2-Input Multiplexer with Storage (74LS298)
M157C	Quad 2 Bit Gated Non Inverting Mux
M158C	Quad 2 Bit Gated Inverting Mux
M257C	Quad 2 Bit Gated Non Inverting Mux with 3-State Output
M258C	Quad 2 Bit Gated Inverting Mux with 3-State Output
M153C	Dual 4 Bit Gated Non Inverting Mux
M353C	Dual 4 Bit Gated Inverting Mux with 3-State Output
M253C	Dual 4 Bit Gated Non Inverting Mux with 3-State Output (74LS253)
M251C	8 Bit Gated Mux with 3-State Output (74LS251)
M151C	8 Bit Gated Mux
M152C	8 Bit Inverting Mux
M150C	16 Bit Gated Inverting Mux (74LS150)
MUX31H	3 Bit Non Inverting Mux
MUX31L	3 Bit Inverting Mux
MUX41H	4 Bit Non Inverting Mux
MUX41GH	4 Bit Gated Non Inverting Mux
MUX41L	4 Bit Inverting Mux
MUX51H	5 Bit Non Inverting Mux
MUX51L	5 Bit Inverting Mux
MUX61H	6 Bit Non Inverting Mux
MUX61L	6 Bit Inverting Mux
MUX71H	7 Bit Non Inverting Mux
MUX71L	7 Bit Inverting Mux
MUX81H	8 Bit Non Inverting Mux
MUX22H	Dual 2 Bit Non Inverting Mux
MUX32H	Dual 3 Bit Non Inverting Mux
MUX42H	Dual 4 Bit Non Inverting Mux
MUX52H	Dual 5 Bit Non Inverting Mux
MUX62H	Dual 6 Bit Non Inverting Mux
MUX72H	Dual 7 Bit Non Inverting Mux
MUX82H	Dual 8 Bit Non Inverting Mux
MUX24H	Quad 2 Bit Non Inverting Mux
MUX24L	Quad 2 Bit Inverting Mux
MUX34H	Quad 3 Bit Non Inverting Mux
MUX44H	Quad 4 Bit Non Inverting Mux
MUX54H	Quad 5 Bit Non Inverting Mux
MUX64H	Quad 6 Bit Non Inverting Mux
MUX74H	Quad 7 Bit Non Inverting Mux
MUX84H	Quad 8 Bit Non Inverting Mux



MULTIPLEX REGISTER

MR41	4 Bit Register with 2 Bit Multiplexed Input
MR42	4 Bit Register with 2 Bit Multiplexed Input, Clear Direct
MR43	4 Bit Register with 2 Bit Multiplexed Input, Sync Clear
MR44	4 Bit Register with 2 Bit Multiplexed Input, Sync Clear Reset B
MR81	8 Bit Register with 2 Bit Multiplexed Input
MR82	8 Bit Register with 2 Bit Multiplexed Input, Clear Direct

COUNTER

MODULO JOHNSON COUNTER

CM4J	Modulo 4, Johnson Counter, Clear Direct
CM6J	Modulo 6, Johnson Counter, Clear Direct
CM8J	Modulo 8, Johnson Counter, Clear Direct
CM10J	Modulo 10, Johnson Counter, Clear Direct
CM12J	Modulo 12, Johnson Counter, Clear Direct
CM14J	Modulo 14, Johnson Counter, Clear Direct
CM16J	Modulo 16, Johnson Counter, Clear Direct

MODULO GRAY COUNTER

C2G	Modulo 4, Gray Counter, Clear Direct
C3G	Modulo 8, Gray Counter, Clear Direct
C4G	Modulo 16, Gray Counter, Clear Direct
C5G	Modulo 32, Gray Counter, Clear Direct
C6G	Modulo 64, Gray Counter, Clear Direct, Prescaled
C7G	Modulo 128 Gray Counter, Clear Direct, Prescaled
C8G	Modulo 256, Gray Counter, Clear Direct, Prescaled

MODULO BINARY COUNTER

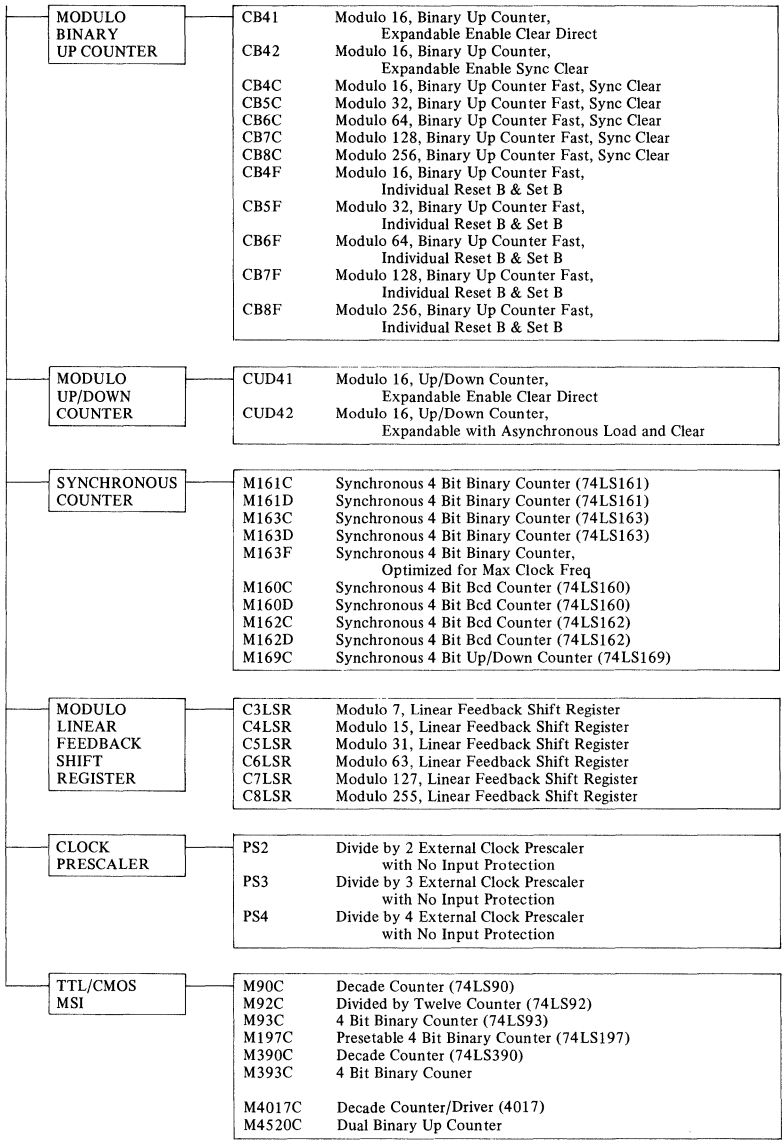
CM3B	Modulo 3, Binary Counter, Clear Direct
CM4B	Modulo 4, Binary Counter, Clear Direct
CM5B	Modulo 5, Binary Counter, Clear Direct
CM6B	Modulo 6, Binary Counter, Clear Direct
CM7B	Modulo 7, Binary Counter, Clear Direct
CM8B	Modulo 8, Binary Counter, Clear Direct
CM9B	Modulo 9, Binary Counter, Clear Direct
CM10B	Modulo 10, Binary Counter, Clear Direct
CM11B	Modulo 11, Binary Counter, Clear Direct
CM12B	Modulo 12, Binary Counter, Clear Direct
CM13B	Modulo 13, Binary Counter, Clear Direct
CM14B	Modulo 14, Binary Counter, Clear Direct
CM15B	Modulo 15, Binary Counter, Clear Direct
CM16B	Modulo 16, Binary Counter, Clear Direct
CM17B	Modulo 17, Binary Counter, Clear Direct

MODULO BINARY RIPPLE COUNTER

CM8BR	Modulo 8, Binary Ripple Counter. Clear Direct
CM9BR	Modulo 9, Binary Ripple Counter, Clear Direct
CM10BR	Modulo 10, Binary Ripple Counter, Clear Direct
CM11BR	Modulo 11, Binary Ripple Counter, Clear Direct
CM12BR	Modulo 12, Binary Ripple Counter, Clear Direct
CM13BR	Modulo 13, Binary Ripple Counter, Clear Direct
CM14BR	Modulo 14, Binary Ripple Counter, Clear Direct
CM15BR	Modulo 15, Binary Ripple Counter, Clear Direct
CM16BR	Modulo 16, Binary Ripple Counter, Clear Direct
CM17BR	Modulo 17, Binary Ripple Counter, Clear Direct
CM18BR	Modulo 18, Binary Ripple Counter, Clear Direct
CM19BR	Modulo 19, Binary Ripple Counter, Clear Direct
CM20BR	Modulo 20, Binary Ripple Counter, Clear Direct
CM21BR	Modulo 21, Binary Ripple Counter, Clear Direct
CM22BR	Modulo 22, Binary Ripple Counter, Clear Direct
CM23BR	Modulo 23, Binary Ripple Counter, Clear Direct
CM24BR	Modulo 24, Binary Ripple Counter, Clear Direct
CM25BR	Modulo 25, Binary Ripple Counter, Clear Direct
CM26BR	Modulo 26, Binary Ripple Counter, Clear Direct
CM27BR	Modulo 27, Binary Ripple Counter, Clear Direct
CM28BR	Modulo 28, Binary Ripple Counter, Clear Direct
CM29BR	Modulo 29, Binary Ripple Counter, Clear Direct
CM30BR	Modulo 30, Binary Ripple Counter, Clear Direct
CM31BR	Modulo 31, Binary Ripple Counter, Clear Direct
CM32BR	Modulo 32, Binary Ripple Counter, Clear Direct

MODULO SHIFT COUNTER

CM5SR	Modulo 5, Shift Counter, Clear Direct
CM8SR	Modulo 8, Shift Counter. Clear Direct
CM9SR	Modulo 9, Shift Counter, Clear Direct
CM10SR	Modulo 10 Shift Counter, Clear Direct
CM12SR	Modulo 12, Shift Counter, Clear Direct



MODULO BINARY UP COUNTER	CB41	Modulo 16, Binary Up Counter, Expandable Enable Clear Direct
	CB42	Modulo 16, Binary Up Counter, Expandable Enable Sync Clear
	CB4C	Modulo 16, Binary Up Counter Fast, Sync Clear
	CB5C	Modulo 32, Binary Up Counter Fast, Sync Clear
	CB6C	Modulo 64, Binary Up Counter Fast, Sync Clear
	CB7C	Modulo 128, Binary Up Counter Fast, Sync Clear
	CB8C	Modulo 256, Binary Up Counter Fast, Sync Clear
	CB4F	Modulo 16, Binary Up Counter Fast, Individual Reset B & Set B
	CB5F	Modulo 32, Binary Up Counter Fast, Individual Reset B & Set B
	CB6F	Modulo 64, Binary Up Counter Fast, Individual Reset B & Set B
	CB7F	Modulo 128, Binary Up Counter Fast, Individual Reset B & Set B
	CB8F	Modulo 256, Binary Up Counter Fast, Individual Reset B & Set B
MODULO UP/DOWN COUNTER	CUD41	Modulo 16, Up/Down Counter, Expandable Enable Clear Direct
	CUD42	Modulo 16, Up/Down Counter, Expandable with Asynchronous Load and Clear
SYNCHRONOUS COUNTER	M161C	Synchronous 4 Bit Binary Counter (74LS161)
	M161D	Synchronous 4 Bit Binary Counter (74LS161)
	M163C	Synchronous 4 Bit Binary Counter (74LS163)
	M163D	Synchronous 4 Bit Binary Counter (74LS163)
	M163F	Synchronous 4 Bit Binary Counter, Optimized for Max Clock Freq
	M160C	Synchronous 4 Bit Bcd Counter (74LS160)
	M160D	Synchronous 4 Bit Bcd Counter (74LS160)
	M162C	Synchronous 4 Bit Bcd Counter (74LS162)
	M162D	Synchronous 4 Bit Bcd Counter (74LS162)
	M169C	Synchronous 4 Bit Up/Down Counter (74LS169)
MODULO LINEAR FEEDBACK SHIFT REGISTER	C3LSR	Modulo 7, Linear Feedback Shift Register
	C4LSR	Modulo 15, Linear Feedback Shift Register
	C5LSR	Modulo 31, Linear Feedback Shift Register
	C6LSR	Modulo 63, Linear Feedback Shift Register
	C7LSR	Modulo 127, Linear Feedback Shift Register
	C8LSR	Modulo 255, Linear Feedback Shift Register
CLOCK PRESCALER	PS2	Divide by 2 External Clock Prescaler with No Input Protection
	PS3	Divide by 3 External Clock Prescaler with No Input Protection
	PS4	Divide by 4 External Clock Prescaler with No Input Protection
TTL/CMOS MSI	M90C	Decade Counter (74LS90)
	M92C	Divided by Twelve Counter (74LS92)
	M93C	4 Bit Binary Counter (74LS93)
	M197C	Presetable 4 Bit Binary Counter (74LS197)
	M390C	Decade Counter (74LS390)
	M393C	4 Bit Binary Couner
	M4017C	Decade Counter/Driver (4017)
	M4520C	Dual Binary Up Counter

MEMORY

SRAM

	MASTER (A5GF –)									
	21	26	32	45	58	82	FUNCTION			
G4B32	A	B	C	D	E	F	SRAM	4 bit	*	32 words
G4B64	A	B	C	D	E	F	SRAM	4 bit	*	64 words
G4B128	A	B	C	D	E	F	SRAM	4 bit	*	128 words
G4B256	A	B	C	D	E	F	SRAM	4 bit	*	256 words
G4B512	A	B	C	D	E	F	SRAM	4 bit	*	512 words
G4B1K	/	/	/	D	E	F	SRAM	4 bit	*	1024 words
G4B2K	/	/	/	/	E	F	SRAM	4 bit	*	2048 words
G8B32	A	B	C	D	E	F	SRAM	8 bit	*	32 words
G8B64	A	B	C	D	E	F	SRAM	8 bit	*	64 words
G8B128	A	B	C	D	E	F	SRAM	8 bit	*	128 words
G8B256	A	B	C	D	E	F	SRAM	8 bit	*	256 words
G8B512	/	/	/	D	E	F	SRAM	8 bit	*	512 words
G8B1K	/	/	/	/	E	F	SRAM	8 bit	*	1024 words
G16B32	/	/	/	D	E	F	SRAM	16 bit	*	32 words
G16B64	/	/	/	D	E	F	SRAM	16 bit	*	64 words
G16B128	/	/	/	D	E	F	SRAM	16 bit	*	128 words
G16B256	/	/	/	D	E	F	SRAM	16 bit	*	256 words
G16B512	/	/	/	/	E	F	SRAM	16 bit	*	512 words
G16B786	/	/	/	/	/	F	SRAM	16 bit	*	768 words
G24B32	/	/	/	/	/	F	SRAM	24 bit	*	32 words
G24B64	/	/	/	/	/	F	SRAM	24 bit	*	64 words
G24B128	/	/	/	/	/	F	SRAM	24 bit	*	128 words
G24B256	/	/	/	/	/	F	SRAM	24 bit	*	256 words
G24B512	/	/	/	/	/	F	SRAM	24 bit	*	512 words
G24B768	/	/	/	/	/	F	SRAM	24 bit	*	768 words

MROM

	MASTER (A5GF –)									
	21	26	32	45	58	82	FUNCTION			
G4S128	A	B	C	D	E	F	MROM	4 bit	*	128 words
G4S256	A	B	C	D	E	F	MROM	4 bit	*	256 words
G4S512	A	B	C	D	E	F	MROM	4 bit	*	512 words
G4S1024	A	B	C	D	E	F	MROM	4 bit	*	1024 words
G4S2K	/	/	/	D	E	F	MROM	4 bit	*	2048 words
G4S4K	/	/	/	/	E	F	MROM	4 bit	*	4096 words
G8S128	A	B	C	D	E	F	MROM	8 bit	*	128 words
G8S256	A	B	C	D	E	F	MROM	8 bit	*	256 words
G8S512	A	B	C	D	E	F	MROM	8 bit	*	512 words
G8S1K	/	/	/	D	E	F	MROM	8 bit	*	1024 words
G8S2K	/	/	/	/	E	F	MROM	8 bit	*	2048 words
G16S128	/	/	/	D	E	F	MROM	16 bit	*	128 words
G16S256	/	/	/	D	E	F	MROM	16 bit	*	256 words
G16S512	/	/	/	D	E	F	MROM	16 bit	*	512 words
G16S1K	/	/	/	/	E	F	MROM	16 bit	*	1024 words
G16S1K5	/	/	/	/	/	F	MROM	16 bit	*	1536 words
G24S128	/	/	/	/	/	F	MROM	24 bit	*	128 words
G24S256	/	/	/	/	/	F	MROM	24 bit	*	256 words
G24S512	/	/	/	/	/	F	MROM	24 bit	*	512 words
G24S1K	/	/	/	/	/	F	MROM	24 bit	*	1024 words
G24S1K5	/	/	/	/	/	F	MROM	24 bit	*	1536 words

TTL/RICOH CELL CORRESPONDENCE TABLE

TTL Name	RICOH Cell		TTL Name	RICOH Cell		TTL Name	RICOH Cell	
74LS00	NAND02		74LS138	M138C		74LS244	M244C	F
74LS02	NOR02			M138D		74LS245	M245C	F
74LS04	INV01		74LS139	M139C		74LS251	M251C	F
74LS10	NAND03		74LS145	M145C		74LS253	M253C	F
74LS20	NAND04		74150	M150C		74LS257C	M257C	F
7425	NOR04*1		74LS151	M151C		74LS258	M258C	F
74LS27	NOR03		74LS152	M152C		74S260	NOR05	
74LS30	NAND08		74LS153	M153C		74LS273	M273C	
7442	D410L		74LS154	M154C			R82	
	M42C		74LS155	M155C		74LS279	NRSLT*10	
74LS43	M43C		74LS157	M157C		74LS298	M298C	
74LS44	M44C		74LS158	M158C		74LS353	M353C	F
74LS47	M47C		74LS160	M160C*6		74LS367A	M367C	F
74LS49	M49C			M160D		74LS368A	M368C	F
74LS51	AOI22		74LS161	M161C*7			TINVBF	F
74LS54	AOI24			M161D			TBF368	F
74LS73	NJKCOR*2	F	74LS162	M162C*8		74LS390	M390C	
7474	NDCSR			M162D		74LS393	M393C	
7476	NJKCSR*3		74LS163	M163C*9			CM16BR*11	
74LS80	M80C*4			M163D		74LS399	MR41	
7482	M82C			M163F		74LS540	M540C	F
	FA2		74LS164	M164C		74LS541	M541C	F
74LS83	M83C		74LS165	M165C		74LS640	M640C	F
74LS85	M85C		74LS166	M166C		4017	M4017C	
74LS86	XOR02		74LS169	M169C		4028	M4028C	
74LS90	M90C		74LS171	R42		4520	M4520C	
74LS91	M91C		74LS174	R82		4555	M4555C	
74LS92	M92C		74LS175	R42				
74LS93	M93C		74LS179	M179C				
74LS94	M94C		74LS180	M180C				
74LS95	M95C		74LS195	M195C				
74LS96	M96C		74LS197	M197C				
74100	L4		74LS198	M198C				
74LS113A	NJKCOS*5		74LS199	M199C				
74LS125	M125C	F	74LS240	M240C	F			

F: Only 5GF Series

*1: NOR04 has no strobe terminal.

*2 *3 and *5: 7473, 7476, and 74LS113A are negative edge triggers, but NJKCOR, NJKCSR and NJKCOS are positive edge triggers.

4: M80C has no 74LS80 A or B* terminals.

*6, *7, *8 and *9: M160C, M161C, M162C and M163C have inverted outputs.

*10: NRSLT has a QB terminal.

*11: 74LS393 is a negative edge trigger, but CM16BR is a positive edge trigger.

Microelectronic Specification

CMOS STANDARD CELL RSC-20 SERIES

■GENERAL DESCRIPTION

RSC-20 series is a Standard Cell series using 2μm silicon gate CMOS with double layer metal interconnection.

It is possible to develop full custom LSIs quickly by utilizing the full CAD support system and the abundant function cell library.

RSC-20 series also allows user to utilize the one chip system easily and utilize high-speed, high-reliability and cost-reduction.

■FEATURES

- Advanced CMOS Technology for high Speed, High Density and Low Power Dissipation.
- Abundant Cell Library for Easy Design.
- Full CAD Support System.
- Various CAD Interface Support. (FUTURE NET, MENTOR IDEA 1000, DAISY LOGICIAN etc.)

■STANDARD FUNCTIONAL SPECIFICATION ＊1

GRID COUNT ＊2 (internal cells)	GATE COUNT (typical)	I/O COUNT (maximum)	AVAILABLE PACKAGE			
			DIP	FLAT	PLCC	PGA
200×20	900	40	14, 16, 18, 20, 22, 24, 28, 40	44	18, 20, 28, 44	68
300×30	1900	60	24, 28, 40, 42, 48, 64-S	44, 60	18, 20, 28, 44, 68	68
400×40	3250	80	24, 28, 40, 42, 48, 64-S	44, 60, 80	20, 28, 44, 68, 84	68, 84
500×50	4700	100	40, 42, 48, 64-S	80, 100	28, 44, 68, 84	68, 84, 100
600×60	6250	120	40, 48, 64-S	80, 100	44, 68, 84	68, 84, 100, 120

＊1・・This table indicates nominal value for reference purpose, because routing area is depend on the complexity of designed circuit.

＊2・・GRID COUNT = COLUMN GRID number × ROW GRID number

■ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Condition	Limits	Units
V_{CC}	Supply Voltage	With respect to GND	−0.3 ~ 7	V
V_I	Input Voltage		−0.3 ~ Vcc+0.3	V
V_O	Output Voltage		−0.3 ~ Vcc+0.3	V
Topr	Operating Ambient Temperature		0 ~ 70	℃
Tstg	Storage Temperature		−40 ~ 125	℃

■ELECTRICAL CHARACTERISTICS

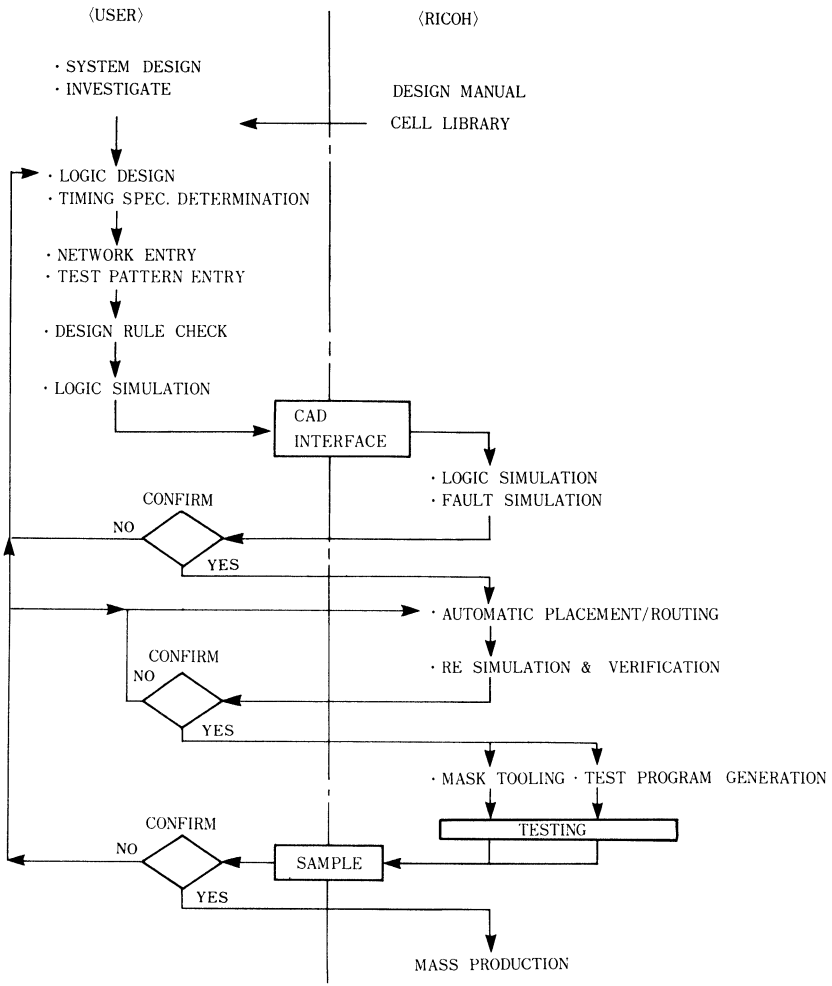
I/O CELL'S DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

Symbol	Parameters	Measuring Condition	Limits			Units
			Min.	Typ.	Max.	
V_{IH}	Input "H" Voltage (TTL compatible)		2.0		Vcc+0.3	V
V_{IL}	Input "L" Voltage (TTL compatible)		−0.3		0.8	V
V_{OH}	Output "H" Voltage	I_{OH} = −4mA	2.4			V
V_{OL}	Output "L" Voltage	I_{OL} = 4mA			0.4	V
I_{LI}	Input Leakage Current	V_I = 0~Vcc	−10		10	μA
I_{LO}	Output Leakage Current	V_O = 0~Vcc	−10		10	μA

AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

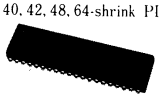
Symbol	Parameters	Measuring Condition	Limits			Units
			Min.	Typ.	Max.	
tpdo	Output Buffer's Delay Time	C_L = 50pF		5.9		ns
tpdi	Input Buffer's Delay Time	FAN OUT= 1, Wire length= 3mm		2.9		ns
tpd	Internal Gate's Delay Time	FAN OUT= 3, Wire length= 3mm		2.0		ns
tacc1	RAM's Address Access Time	FAN OUT= 3, Wire length= 3mm			50	ns
tacc2	ROM's Address Access Time	FAN OUT= 3, Wire length= 3mm			50	ns

■DEVELOPMENT FLOW CHART

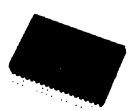


■PACKAGE

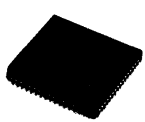
DIP 14, 16, 18, 20, 22, 24, 28, 40, 42, 48, 64-shrink PIN



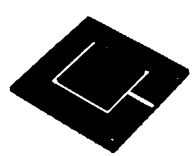
FLAT 44, 60, 80, 100 PIN



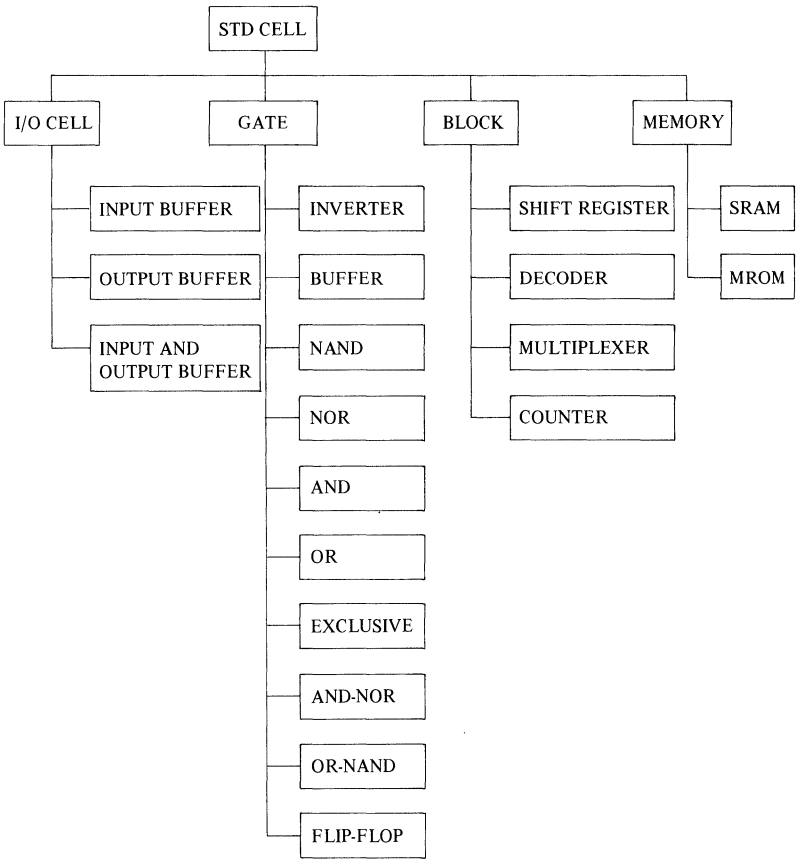
PLCC 18, 20, 28, 44, 68, 84 PIN



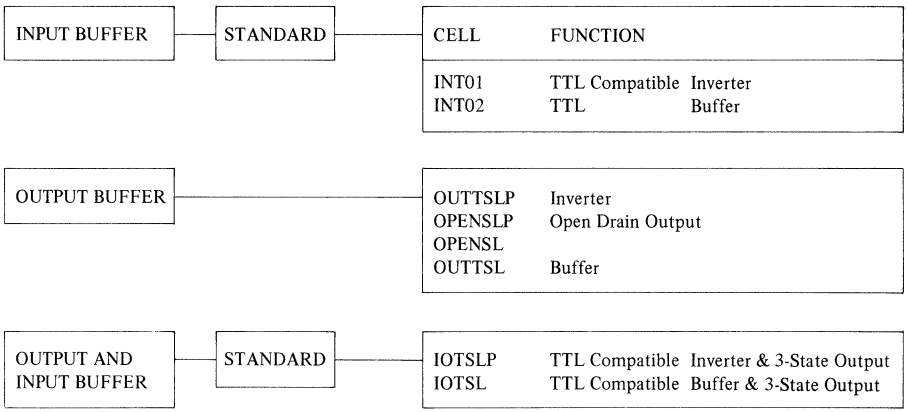
PGA 68, 84, 100, 120 PIN

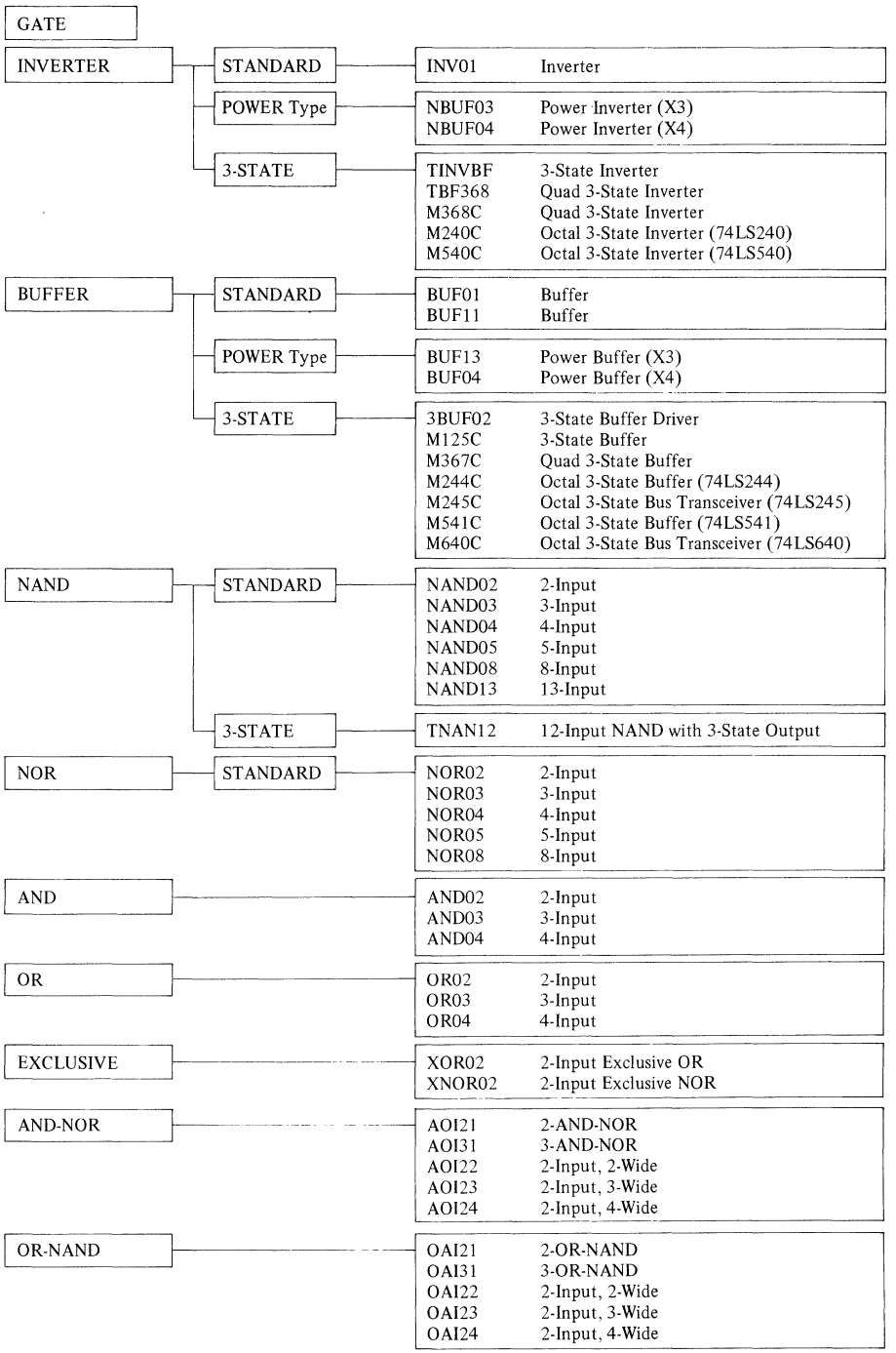


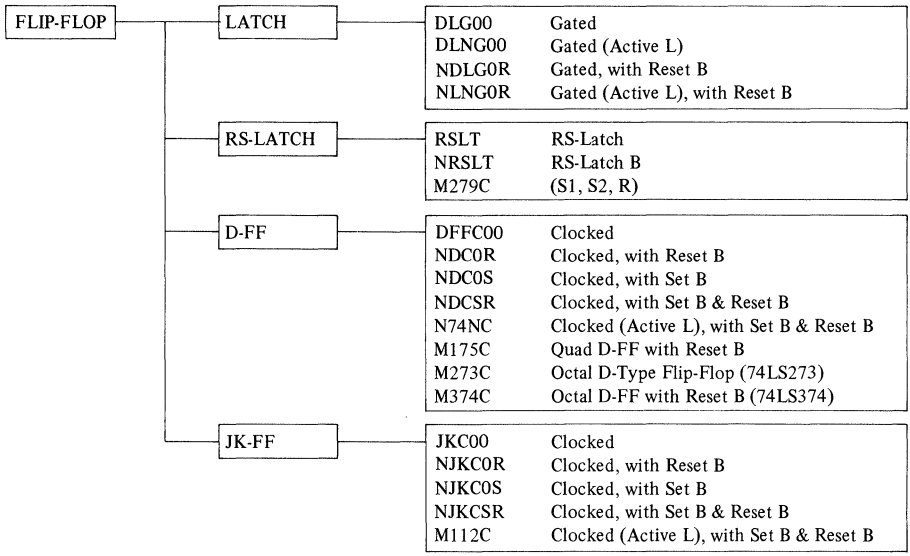
CMOS STANDARD CELL RSC-20 series
CELL LIST

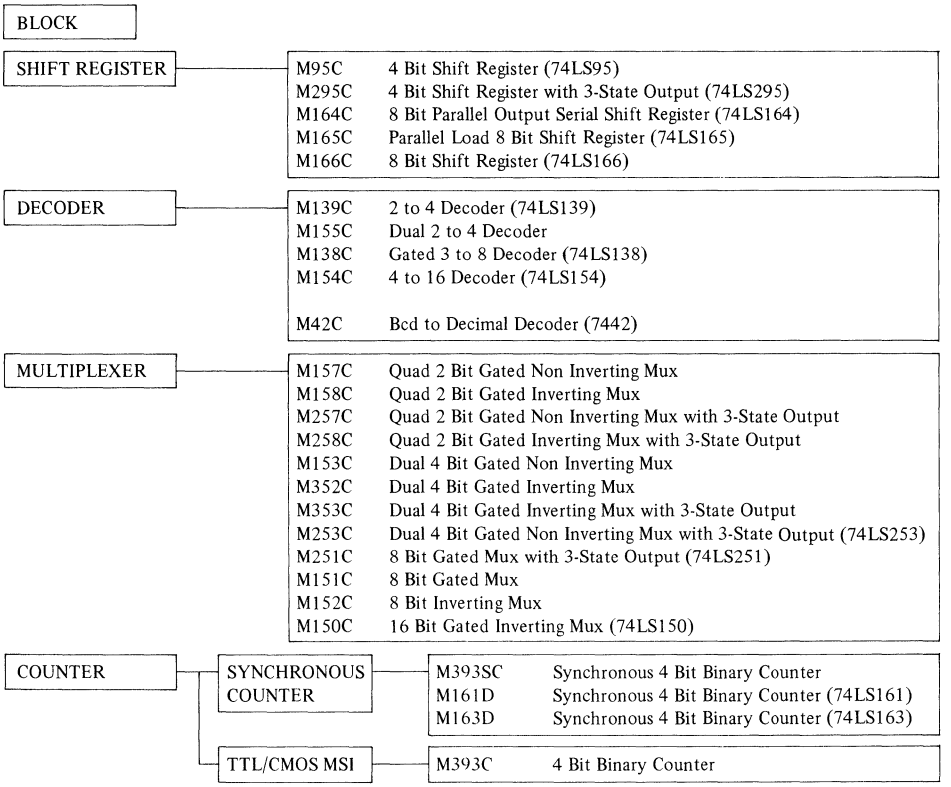


I/O CELLS


INPUT BUFFER
STANDARD
CELL FUNCTION
INT01 TTL Compatible Inverter
INT02 TTL Buffer
OUTPUT BUFFER
OUTTSLP Inverter
OPENSLP Open Drain Output
OPENSL
OUTTSL Buffer
OUTPUT AND INPUT BUFFER
STANDARD
IOTSLP TTL Compatible Inverter & 3-State Output
IOTSL TTL Compatible Buffer & 3-State Output


GATE
INVERTER
STANDARD
INV01 Inverter
POWER Type
NBUF03 Power Inverter (X3)
NBUF04 Power Inverter (X4)
3-STATE
TINVBF 3-State Inverter
TBF368 Quad 3-State Inverter
M368C Quad 3-State Inverter
M240C Octal 3-State Inverter (74LS240)
M540C Octal 3-State Inverter (74LS540)
BUFFER
STANDARD
BUF01 Buffer
BUF11 Buffer
POWER Type
BUF13 Power Buffer (X3)
BUF04 Power Buffer (X4)
3-STATE
3BUF02 3-State Buffer Driver
M125C 3-State Buffer
M367C Quad 3-State Buffer
M244C Octal 3-State Buffer (74LS244)
M245C Octal 3-State Bus Transceiver (74LS245)
M541C Octal 3-State Buffer (74LS541)
M640C Octal 3-State Bus Transceiver (74LS640)
NAND
STANDARD
NAND02 2-Input
NAND03 3-Input
NAND04 4-Input
NAND05 5-Input
NAND08 8-Input
NAND13 13-Input
3-STATE
TNAN12 12-Input NAND with 3-State Output
NOR
STANDARD
NOR02 2-Input
NOR03 3-Input
NOR04 4-Input
NOR05 5-Input
NOR08 8-Input
AND
AND02 2-Input
AND03 3-Input
AND04 4-Input
OR
OR02 2-Input
OR03 3-Input
OR04 4-Input
EXCLUSIVE
XOR02 2-Input Exclusive OR
XNOR02 2-Input Exclusive NOR
AND-NOR
AOI21 2-AND-NOR
AOI31 3-AND-NOR
AOI22 2-Input, 2-Wide
AOI23 2-Input, 3-Wide
AOI24 2-Input, 4-Wide
OR-NAND
OAI21 2-OR-NAND
OAI31 3-OR-NAND
OAI22 2-Input, 2-Wide
OAI23 2-Input, 3-Wide
OAI24 2-Input, 4-Wide


FLIP-FLOP
LATCH
DLG00 Gated
DLNG00 Gated (Active L)
NDLG0R Gated, with Reset B
NLNG0R Gated (Active L), with Reset B
RS-LATCH
RSLT RS-Latch
NRSLT RS-Latch B
M279C (S1, S2, R)
D-FF
DFFC00 Clocked
NDC0R Clocked, with Reset B
NDC0S Clocked, with Set B
NDCSR Clocked, with Set B & Reset B
N74NC Clocked (Active L), with Set B & Reset B
M175C Quad D-FF with Reset B
M273C Octal D-Type Flip-Flop (74LS273)
M374C Octal D-FF with Reset B (74LS374)
JK-FF
JKC00 Clocked
NJKC0R Clocked, with Reset B
NJKC0S Clocked, with Set B
NJKCSR Clocked, with Set B & Reset B
M112C Clocked (Active L), with Set B & Reset B


BLOCK
SHIFT REGISTER
M95C 4 Bit Shift Register (74LS95)
M295C 4 Bit Shift Register with 3-State Output (74LS295)
M164C 8 Bit Parallel Output Serial Shift Register (74LS164)
M165C Parallel Load 8 Bit Shift Register (74LS165)
M166C 8 Bit Shift Register (74LS166)
DECODER
M139C 2 to 4 Decoder (74LS139)
M155C Dual 2 to 4 Decoder
M138C Gated 3 to 8 Decoder (74LS138)
M154C 4 to 16 Decoder (74LS154)
M42C Bcd to Decimal Decoder (7442)
MULTIPLEXER
M157C Quad 2 Bit Gated Non Inverting Mux
M158C Quad 2 Bit Gated Inverting Mux
M257C Quad 2 Bit Gated Non Inverting Mux with 3-State Output
M258C Quad 2 Bit Gated Inverting Mux with 3-State Output
M153C Dual 4 Bit Gated Non Inverting Mux
M352C Dual 4 Bit Gated Inverting Mux
M353C Dual 4 Bit Gated Inverting Mux with 3-State Output
M253C Dual 4 Bit Gated Non Inverting Mux with 3-State Output (74LS253)
M251C 8 Bit Gated Mux with 3-State Output (74LS251)
M151C 8 Bit Gated Mux
M152C 8 Bit Inverting Mux
M150C 16 Bit Gated Inverting Mux (74LS150)
COUNTER
SYNCHRONOUS COUNTER
M393SC Synchronous 4 Bit Binary Counter
M161D Synchronous 4 Bit Binary Counter (74LS161)
M163D Synchronous 4 Bit Binary Counter (74LS163)
TTL/CMOS MSI
M393C 4 Bit Binary Counter

MEMORY

ASYNCHRONOUS SRAM

COMPILED CELL

Data (D)	$2 < D < 8, D = 16$	
Words (W)	$32 \leqq W \leqq 1024$	(D = 2, 3, 5, 6, 7, 16)
	$32 \leqq W \leqq 2048$	(D = 8)
	$32 \leqq W \leqq 4096$	(D = 4)
MAX. Size		16 K bit

SYNCHRONOUS SRAM *

* under development

COMPILED CELL

Data	2 bit ~ 64 bit	
Words	8 ~ 2048	($2 \leqq$ bits $\leqq 16$)
	8 ~ 1024	($17 \leqq$ bits $\leqq 32$)
	8 ~ 512	($33 \leqq$ bits $\leqq 64$)
MAX. Size		32 K bit

MROM

COMPILED CELL

Data	2 ~ 16	
Words	128 ~ 32 K	
MAX. Size		64 K bit

CMOS STANDARD CELL
RSC-15 Series

■ OUTLINE

RSC-15 series are a Standard Cell series using 1.5 μm CMOS process and allow high speed operation. RSC-15 series have Abundant Cell Library for easy design. The Cell Library is upper-compatible with GATE ARRAY 5GF series.

■ FEATURES

1. High Speed Operation (1.5 μm CMOS process)

Gate Delay Time	1.0 ns[1)]	(Typ.)
I/O Buffer Delay Time	3.0 ns	(Typ.)
SRAM Access Time	65 ns	(Max.)
MASK ROM Access Time	60 ns	(Max.)
EPROM[2)] Access Time	150 ns	(Max.)

1) F.O. = 3 , wire length = 3mm
2) under development

2. Cell Library

Macro Cell	180 cells	(including 38 I/O cells)
Macrofunction Cell	231 cells	(including 11 I/O cells)
total	411 cells	

It is easy to transfer the Gate Array 5GF to Standard Cell RSC-15 because the cell library of RSC-15 is upper compatible with that of 5GF

3. Memory Cell

Memory Cells are available and it is possible to integrate your system on one chip.

4. CAD Support

CAD tool : IBM-PC, MENTOR, DAISY
Soft ware : DASH-CADAT
(DASH and CADAT are trademark of FutureNet Co. and HHB Systems Co.)

■ PACKAGE

DIP	14, 16, 20, 24, 28, 40, 48, 64 pins
QFP	44, 60, 64, 80, 100, 128, 144, 160 pins
PLCC	28, 44, 68, 84 pins
SOP	20, 24, 28 pins
PGA	68 ~ 180 pins

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Conditions	Specified Value	Unit
Vcc	Supply Voltage	With Respect to GND	-0.3 ~ 7	V
VI	Input Voltage		-0.3 ~ Vcc + 0.3	V
VO	Output Voltage		-0.3 ~ Vcc + 0.3	V
Topr	Operating Ambient Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-40 ~ 125	°C

■ D.C. CHARACTERISTICS

(Ta = 0~70°C, Vcc = 5V±10%)

Symbol	Parameters	Conditions	Specified Value			Unit
			min.	typ.	max.	
VIH	"H" Input Voltage (TTL)		2.2		Vcc + 0.3	V
VIL	"L" Input Voltage (TTL)		-0.3		0.8	V
VIH	"H" Input Voltage (CMOS)		Vcc x 0.7		Vcc + 0.3	V
VIL	"L" Input Voltage (CMOS)		-0.3		Vcc x 0.3	V
VOH	"H" Output Voltage	IOH = -8mA	2.4			V
VOL	"L" Output Voltage	IOL = 8mA			0.4	V
ILI	Input Leakage Current	VI = 0 ~ Vcc	-10		10	μA
IOZ	Output Leakage Current (Off state)	VO = 0 ~ Vcc	-10		10	μA
Icc	Vcc Current		*			mA

* Vcc Current Depends on Used Gate Count.

■ A.C. CHARACTERISTICS

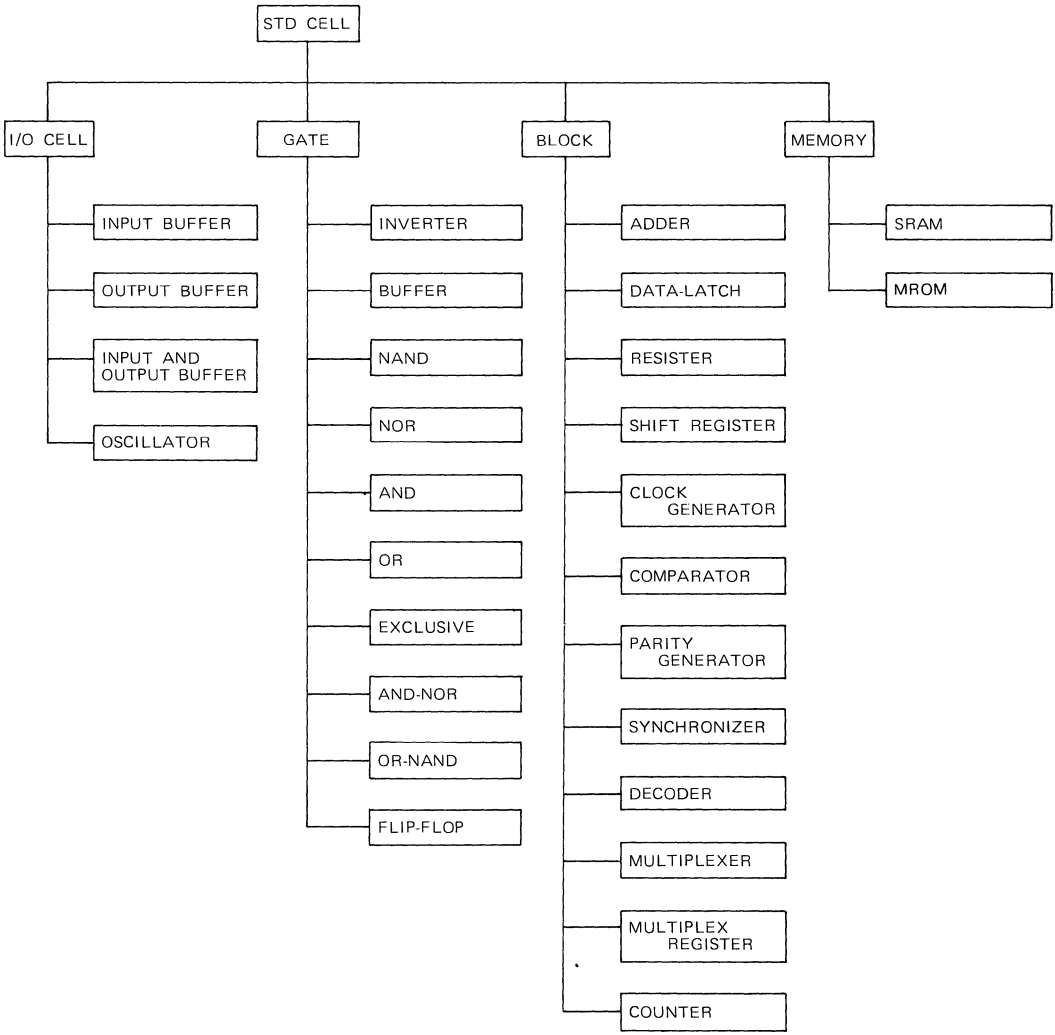
Symbol	Parameters	Conditions	Specified Value			Unit
			min.	typ.	max.	
Tpdo	Output Buffer Delay Time	CL = 15pF		3.0		ns
Tpdi	Input Buffer Delay Time	FO = 3, Wire length = 3mm		3.0		ns
Tpd	Internal Gate Delay Time	FO = 3, Wire length = 3mm		1.0		ns

■ MEMORY ACCESS TIME

Name	Organization		Access Time	
	Width (bit)	Density (bit)	max. (ns)	Conditions*
SRAM	2 ~ 8, 16	MAX. 16K	65	Density : 16K
MASK ROM	2 ~ 16	MAX. 64K	60	Density : 64K
EPROM	8	64K, 128K, 256K	150	Density : 256K

* Access Time Depends on Density.

CMOS STANDARD CELL RSC-15 series
CELL LIST



I/O CELL

INPUT BUFFER

STANDARD

CELL	FUNCTION	
INT01	TTL Compatible	Inverter
INT02	TTL	Buffer
INTSCH	TTL	Schmitt Trigger
INC01	CMOS Compatible	Inverter
INC02	CMOS	Buffer
INCSCH	CMOS	Schmitt Trigger

with RESISTANCE for Pull-Up

INT1U1	TTL Compatible	Inverter
INT2U1	TTL	Buffer
INTSU1	TTL	Schmitt Trigger
INC1U1	CMOS Compatible	Inverter
INC2U1	CMOS	Buffer
INCSU1	CMOS	Schmitt Trigger

with RESISTANCE for Pull-Down

INT1D1	TTL Compatible	Inverter
INT2D1	TTL	Buffer
INTSD1	TTL	Schmitt Trigger
INC1D1	CMOS Compatible	Inverter
INC2D1	CMOS	Buffer
INCSD1	CMOS	Schmitt Trigger

OUTPUT BUFFER

OUTINV	Inverter
OUTTRI	3-State Output
OUTOPN	Open Drain Output
OUTBUF	Buffer

OUTPUT AND INPUT BUFFER

STANDARD

IOT01	TTL Compatible	Inverter & 3-State Output
IOT1		
IOT02	TTL Compatible	Buffer & 3-State Output
IOT2		
IOTSCH	TTL Compatible	Schmitt Trigger & 3-State Output
IOTSH		
IOC01	CMOS Compatible	Inverter & 3-State Output
IOC1		
IOC02	CMOS Compatible	Buffer & 3-State Output
IOC2		
IOCSCH	CMOS Compatible	Schmitt Trigger & 3-State Output
IOCSH		

with RESISTANCE for Pull-Up

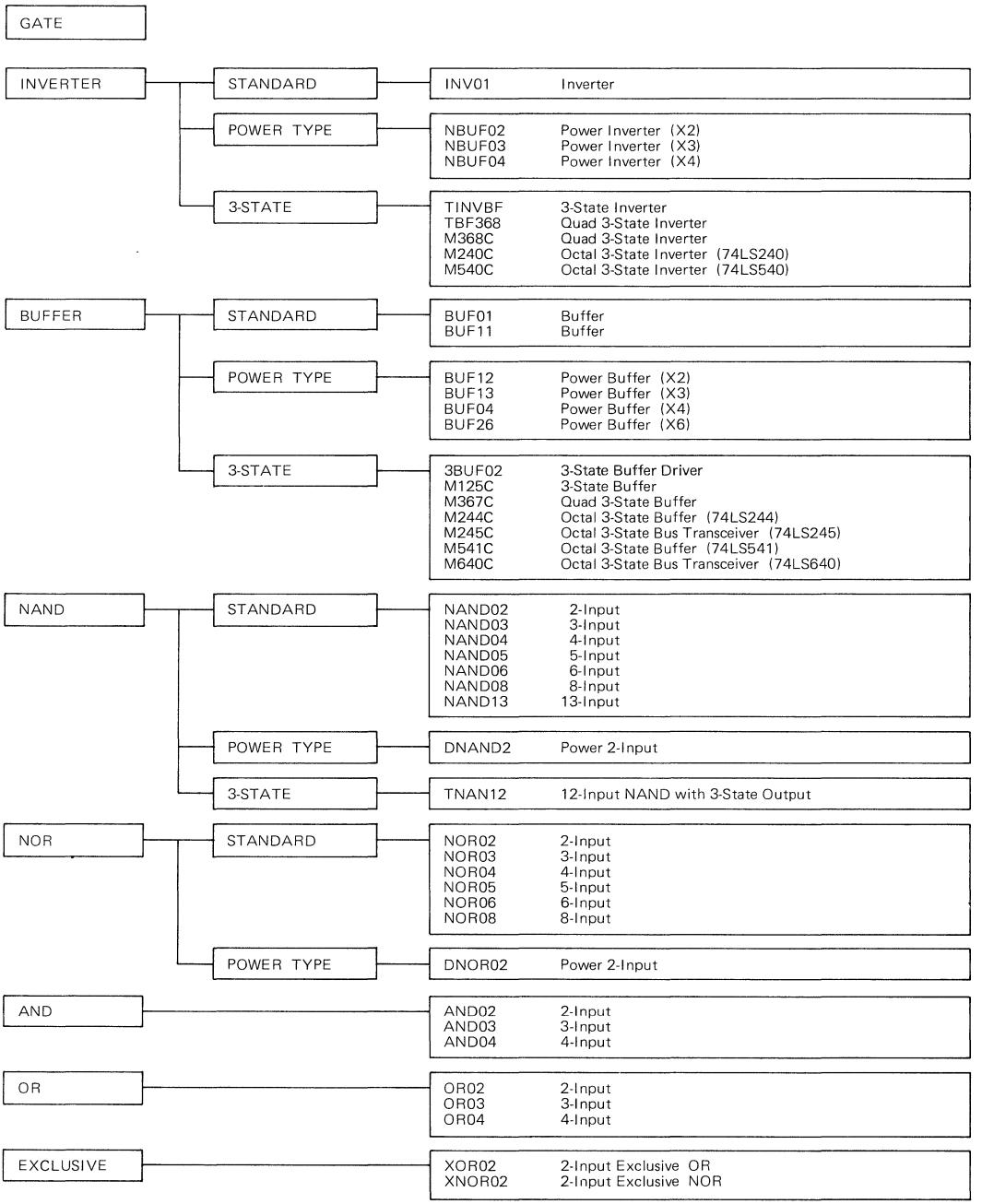
IOT1U1	TTL Compatible	Inverter & 3-State Output
IOTU1		
IOT2U1	TTL Compatible	Buffer & 3-State Output
IOC1U1	CMOS Compatible	Inverter & 3-State Output
IOCU1		
IOC2U1	CMOS Compatible	Buffer & 3-State Output

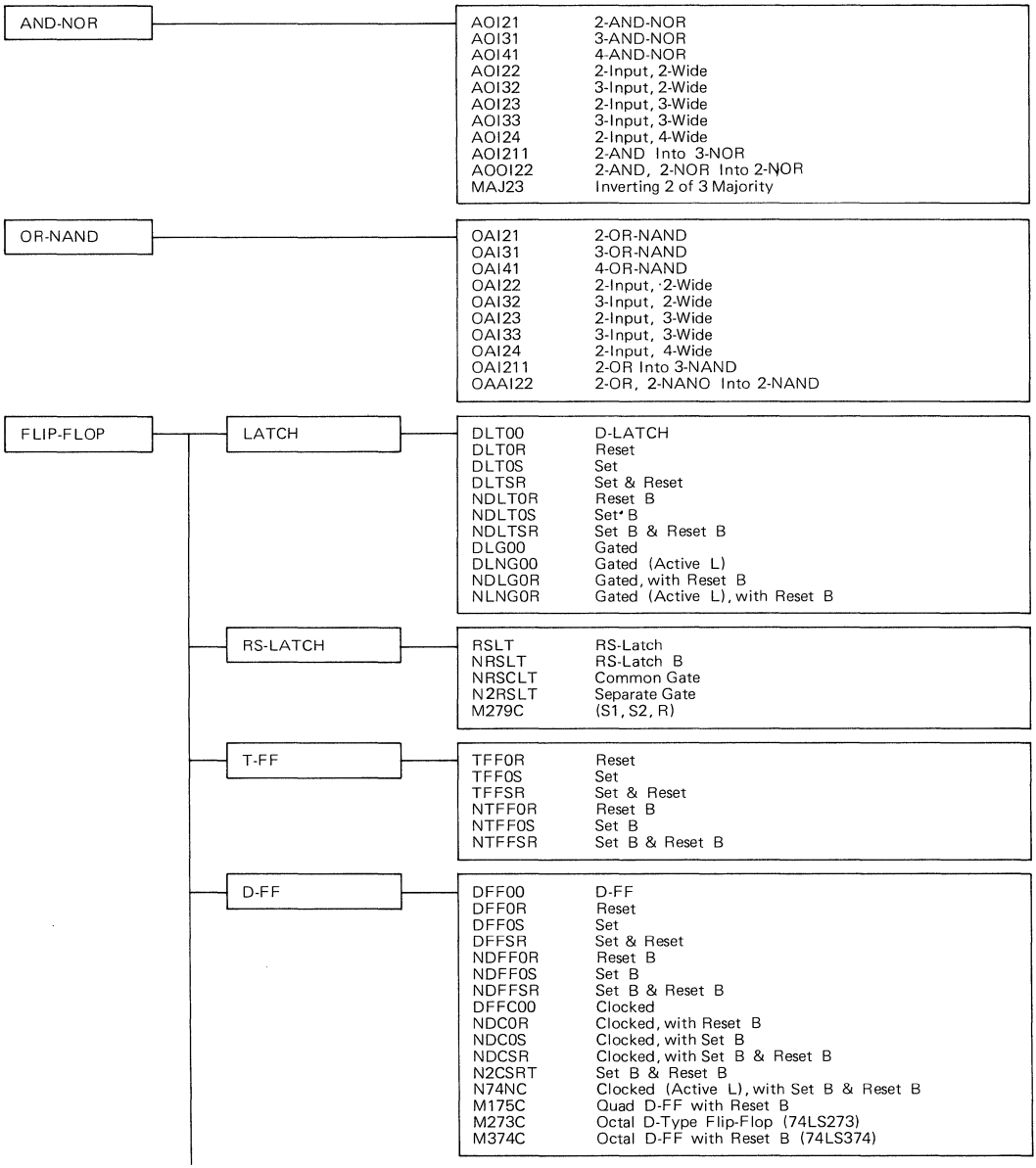
with RESISTANCE for Pull-Down

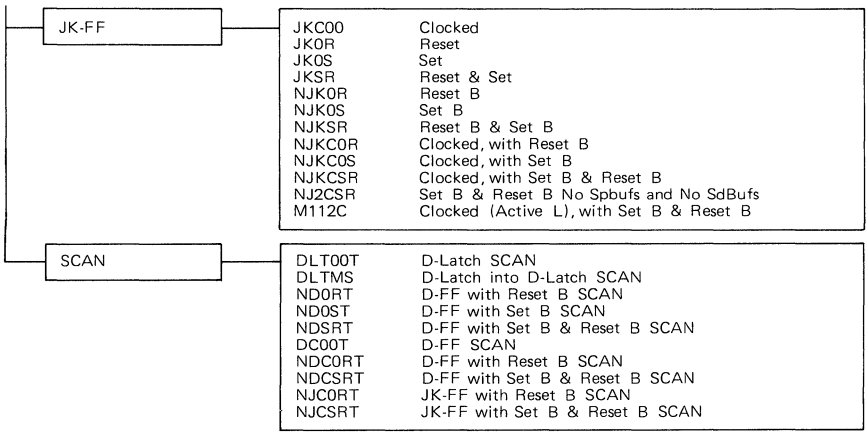
IOT1D1	TTL Compatible	Inverter & 3-State Output
IOTD1		
IOC1D1	CMOS Compatible	Inverter & 3-State Output
IOCD1		

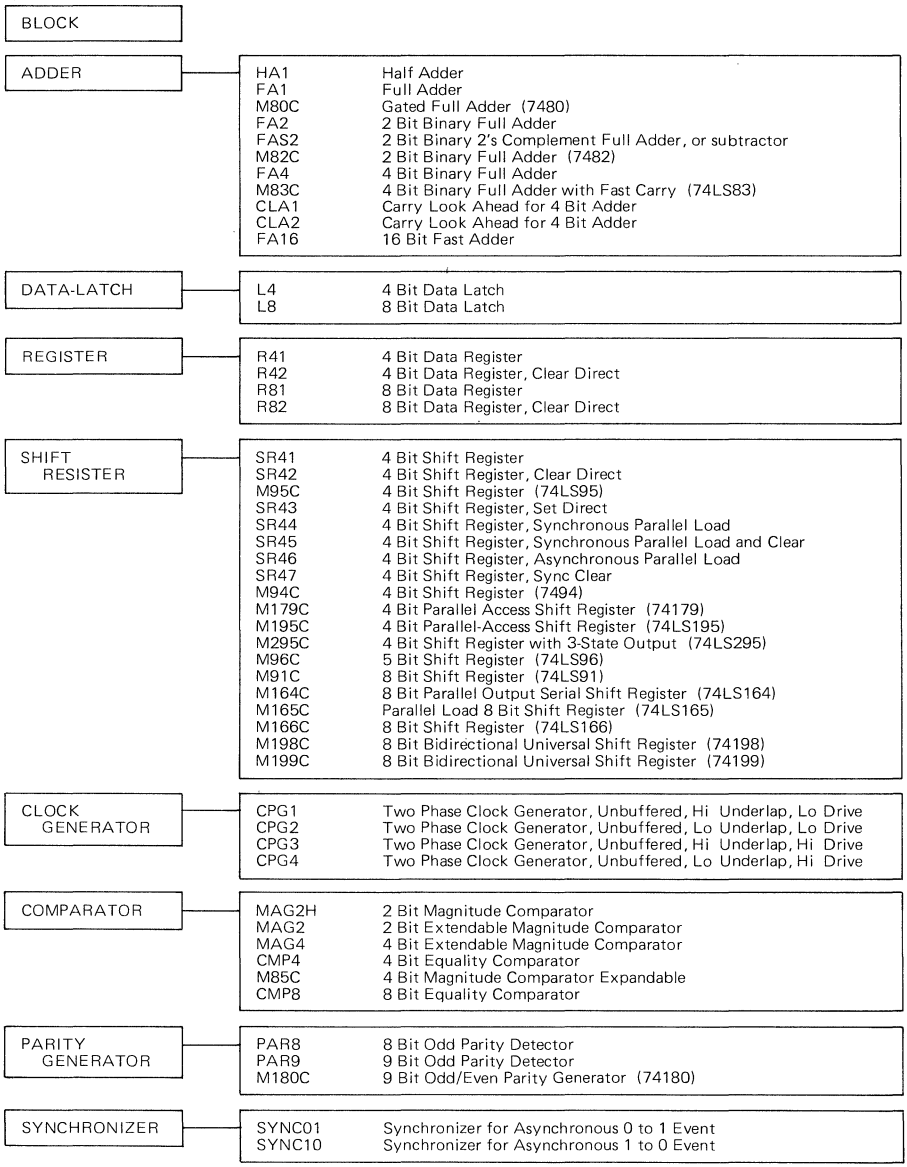
OSCILLATOR

XIN01	Input
XIN02	Input (For High Frequency)
XOUT01	Output
XOUT02	Output (For High Frequency)
XOUT	Oscillator


GATE
INVERTER
STANDARD
INV01 Inverter
POWER TYPE
NBUF02 Power Inverter (X2)
NBUF03 Power Inverter (X3)
NBUF04 Power Inverter (X4)
3-STATE
TINVBF 3-State Inverter
TBF368 Quad 3-State Inverter
M368C Quad 3-State Inverter
M240C Octal 3-State Inverter (74LS240)
M540C Octal 3-State Inverter (74LS540)
BUFFER
STANDARD
BUF01 Buffer
BUF11 Buffer
POWER TYPE
BUF12 Power Buffer (X2)
BUF13 Power Buffer (X3)
BUF04 Power Buffer (X4)
BUF26 Power Buffer (X6)
3-STATE
3BUF02 3-State Buffer Driver
M125C 3-State Buffer
M367C Quad 3-State Buffer
M244C Octal 3-State Buffer (74LS244)
M245C Octal 3-State Bus Transceiver (74LS245)
M541C Octal 3-State Buffer (74LS541)
M640C Octal 3-State Bus Transceiver (74LS640)
NAND
STANDARD
NAND02 2-Input
NAND03 3-Input
NAND04 4-Input
NAND05 5-Input
NAND06 6-Input
NAND08 8-Input
NAND13 13-Input
POWER TYPE
DNAND2 Power 2-Input
3-STATE
TNAN12 12-Input NAND with 3-State Output
NOR
STANDARD
NOR02 2-Input
NOR03 3-Input
NOR04 4-Input
NOR05 5-Input
NOR06 6-Input
NOR08 8-Input
POWER TYPE
DNOR02 Power 2-Input
AND
AND02 2-Input
AND03 3-Input
AND04 4-Input
OR
OR02 2-Input
OR03 3-Input
OR04 4-Input
EXCLUSIVE
XOR02 2-Input Exclusive OR
XNOR02 2-Input Exclusive NOR


AND-NOR
AOI21 2-AND-NOR
AOI31 3-AND-NOR
AOI41 4-AND-NOR
AOI22 2-Input, 2-Wide
AOI32 3-Input, 2-Wide
AOI23 2-Input, 3-Wide
AOI33 3-Input, 3-Wide
AOI24 2-Input, 4-Wide
AOI211 2-AND Into 3-NOR
AOOI22 2-AND, 2-NOR Into 2-NOR
MAJ23 Inverting 2 of 3 Majority
OR-NAND
OAI21 2-OR-NAND
OAI31 3-OR-NAND
OAI41 4-OR-NAND
OAI22 2-Input, 2-Wide
OAI32 3-Input, 2-Wide
OAI23 2-Input, 3-Wide
OAI33 3-Input, 3-Wide
OAI24 2-Input, 4-Wide
OAI211 2-OR Into 3-NAND
OAAI22 2-OR, 2-NANO Into 2-NAND
FLIP-FLOP
LATCH
DLT00 D-LATCH
DLT0R Reset
DLT0S Set
DLTSR Set & Reset
NDLT0R Reset B
NDLT0S Set B
NDLTSR Set B & Reset B
DLG00 Gated
DLNG00 Gated (Active L)
NDLG0R Gated, with Reset B
NLNG0R Gated (Active L), with Reset B
RS-LATCH
RSLT RS-Latch
NRSLT RS-Latch B
NRSCLT Common Gate
N2RSLT Separate Gate
M279C (S1, S2, R)
T-FF
TFF0R Reset
TFF0S Set
TFFSR Set & Reset
NTFF0R Reset B
NTFF0S Set B
NTFFSR Set B & Reset B
D-FF
DFF00 D-FF
DFF0R Reset
DFF0S Set
DFFSR Set & Reset
NDFF0R Reset B
NDFF0S Set B
NDFFSR Set B & Reset B
DFFC00 Clocked
NDC0R Clocked, with Reset B
NDC0S Clocked, with Set B
NDCSR Clocked, with Set B & Reset B
N2CSRT Set B & Reset B
N74NC Clocked (Active L), with Set B & Reset B
M175C Quad D-FF with Reset B
M273C Octal D-Type Flip-Flop (74LS273)
M374C Octal D-FF with Reset B (74LS374)


JK-FF
JKC00 Clocked
JK0R Reset
JK0S Set
JKSR Reset & Set
NJK0R Reset B
NJK0S Set B
NJKSR Reset B & Set B
NJKC0R Clocked, with Reset B
NJKC0S Clocked, with Set B
NJKCSR Clocked, with Set B & Reset B
NJ2CSR Set B & Reset B No Spbufs and No SdBufs
M112C Clocked (Active L), with Set B & Reset B
SCAN
DLT00T D-Latch SCAN
DLTMS D-Latch into D-Latch SCAN
ND0RT D-FF with Reset B SCAN
ND0ST D-FF with Set B SCAN
NDSRT D-FF with Set B & Reset B SCAN
DC00T D-FF SCAN
NDC0RT D-FF with Reset B SCAN
NDCSRT D-FF with Set B & Reset B SCAN
NJC0RT JK-FF with Reset B SCAN
NJCSRT JK-FF with Set B & Reset B SCAN



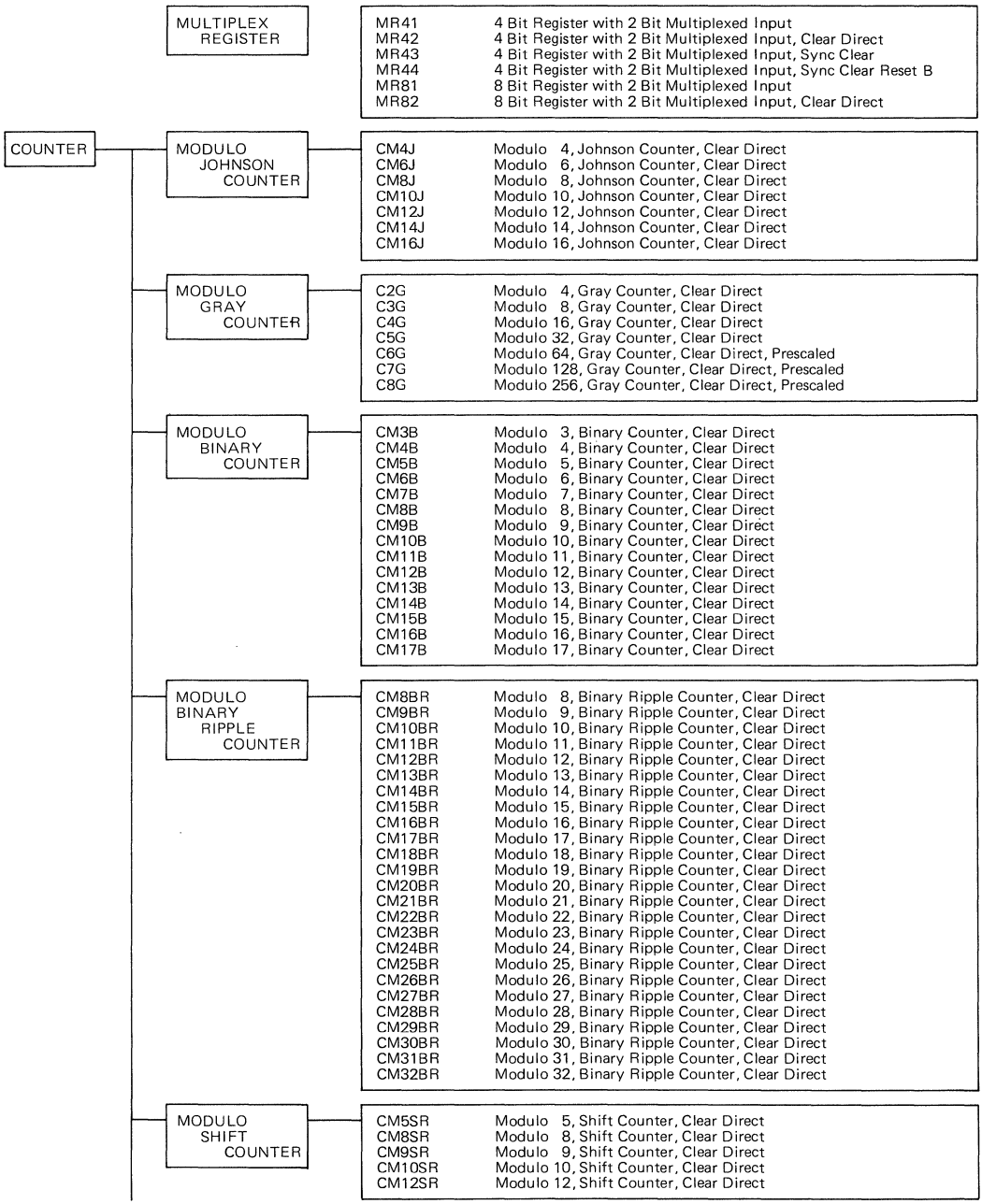
BLOCK		
ADDER	HA1	Half Adder
	FA1	Full Adder
	M80C	Gated Full Adder (7480)
	FA2	2 Bit Binary Full Adder
	FAS2	2 Bit Binary 2's Complement Full Adder, or subtractor
	M82C	2 Bit Binary Full Adder (7482)
	FA4	4 Bit Binary Full Adder
	M83C	4 Bit Binary Full Adder with Fast Carry (74LS83)
	CLA1	Carry Look Ahead for 4 Bit Adder
	CLA2	Carry Look Ahead for 4 Bit Adder
	FA16	16 Bit Fast Adder
DATA-LATCH	L4	4 Bit Data Latch
	L8	8 Bit Data Latch
REGISTER	R41	4 Bit Data Register
	R42	4 Bit Data Register, Clear Direct
	R81	8 Bit Data Register
	R82	8 Bit Data Register, Clear Direct
SHIFT RESISTER	SR41	4 Bit Shift Register
	SR42	4 Bit Shift Register, Clear Direct
	M95C	4 Bit Shift Register (74LS95)
	SR43	4 Bit Shift Register, Set Direct
	SR44	4 Bit Shift Register, Synchronous Parallel Load
	SR45	4 Bit Shift Register, Synchronous Parallel Load and Clear
	SR46	4 Bit Shift Register, Asynchronous Parallel Load
	SR47	4 Bit Shift Register, Sync Clear
	M94C	4 Bit Shift Register (7494)
	M179C	4 Bit Parallel Access Shift Register (74179)
	M195C	4 Bit Parallel-Access Shift Register (74LS195)
	M295C	4 Bit Shift Register with 3-State Output (74LS295)
	M96C	5 Bit Shift Register (74LS96)
	M91C	8 Bit Shift Register (74LS91)
	M164C	8 Bit Parallel Output Serial Shift Register (74LS164)
	M165C	Parallel Load 8 Bit Shift Register (74LS165)
	M166C	8 Bit Shift Register (74LS166)
	M198C	8 Bit Bidirectional Universal Shift Register (74198)
	M199C	8 Bit Bidirectional Universal Shift Register (74199)
CLOCK GENERATOR	CPG1	Two Phase Clock Generator, Unbuffered, Hi Underlap, Lo Drive
	CPG2	Two Phase Clock Generator, Unbuffered, Lo Underlap, Lo Drive
	CPG3	Two Phase Clock Generator, Unbuffered, Hi Underlap, Hi Drive
	CPG4	Two Phase Clock Generator, Unbuffered, Lo Underlap, Hi Drive
COMPARATOR	MAG2H	2 Bit Magnitude Comparator
	MAG2	2 Bit Extendable Magnitude Comparator
	MAG4	4 Bit Extendable Magnitude Comparator
	CMP4	4 Bit Equality Comparator
	M85C	4 Bit Magnitude Comparator Expandable
	CMP8	8 Bit Equality Comparator
PARITY GENERATOR	PAR8	8 Bit Odd Parity Detector
	PAR9	9 Bit Odd Parity Detector
	M180C	9 Bit Odd/Even Parity Generator (74180)
SYNCHRONIZER	SYNC01	Synchronizer for Asynchronous 0 to 1 Event
	SYNC10	Synchronizer for Asynchronous 1 to 0 Event

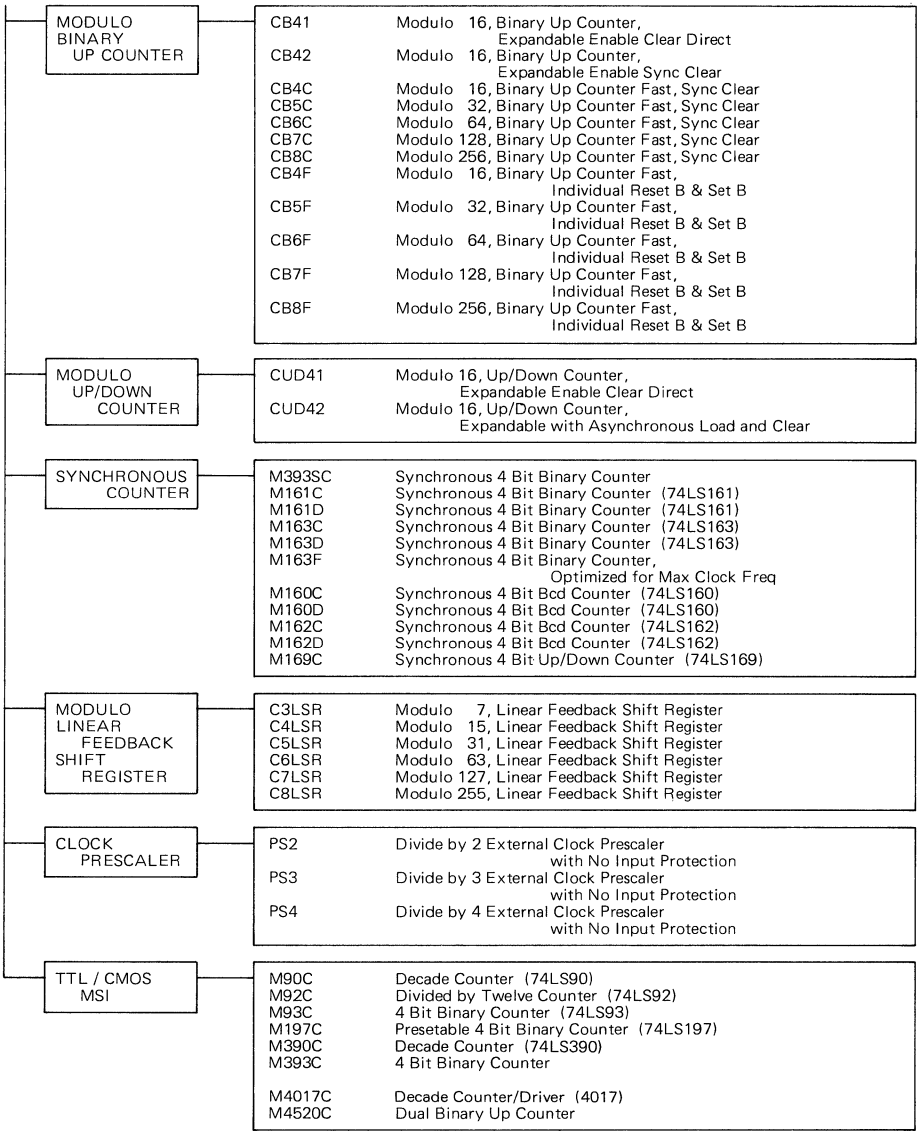
DECODER

M4555C	Binary to 1 of 4 Decoder
M139C	2 to 4 Decoder (74LS139)
M155C	Dual 2 to 4 Decoders
D24H	2 to 4 Decoder, Output Active Hi
D24L	2 to 4 Decoder, Output Active Lo
D24GH	2 to 4 Decoder, Gated Output Active Hi
D24GL	2 to 4 Decoder, Gated Output Active Lo
D38H	3 to 8 Decoder, Output Active Hi
D38L	3 to 8 Decoder, Output Active Lo
D38GH	3 to 8 Decoder, Gated Output Active Hi
D38GL	3 to 8 Decoder, Gated Output Active Lo
M138C	Gated 3 to 8 Decoder (74LS138)
M138D	Gated 3 to 8 Decoder (74LS138)
D410H	4 to 10 Decoder, Output Active Hi
D410L	4 to 10 Decoder, Output Active Lo
M154C	4 to 16 Decoder (74LS154)
DM6JH	Spike Free Decoder for MOD 6 Johnson Counter, Active Hi
DM6JL	Spike Free Decoder for MOD 6 Johnson Counter, Active Lo
DM8JH	Spike Free Decoder for MOD 8 Johnson Counter, Active Hi
DM8JL	Spike Free Decoder for MOD 8 Johnson Counter, Active Lo
DM10JH	Spike Free Decoder for MOD 10 Johnson Counter, Active Hi
DM10JL	Spike Free Decoder for MOD 10 Johnson Counter, Active Lo
DM12JH	Spike Free Decoder for MOD 12 Johnson Counter, Active Hi
DM12JL	Spike Free Decoder for MOD 12 Johnson Counter, Active Lo
DM14JH	Spike Free Decoder for MOD 14 Johnson Counter, Active Hi
DM14JL	Spike Free Decoder for MOD 14 Johnson Counter, Active Lo
DM16JH	Spike Free Decoder for MOD 16 Johnson Counter, Active Hi
DM16JL	Spike Free Decoder for MOD 16 Johnson Counter, Active Lo
M43C	Excess-3 to Decimal Decoder (7443)
M44C	Excess-3 Gray to Decimal Decoder (74LS44)
M47C	Bcd to 7 Segment Decoder/Driver (74LS47)
M49C	Bcd to 7 Segment Decoder/Driver (74LS49)
M42C	Bcd to Decimal Decoder (7442)
M145C	Bcd to Decimal Decoder (74LS145)
M4028C	Bcd to Decimal Decoder (4028)
M247C	Bad to Seven-Segment Decoder/Driver, Active Lo (74LS247)
M249C	Bad to Seven-Segment Decoder/Driver, Active Hi (74LS249)

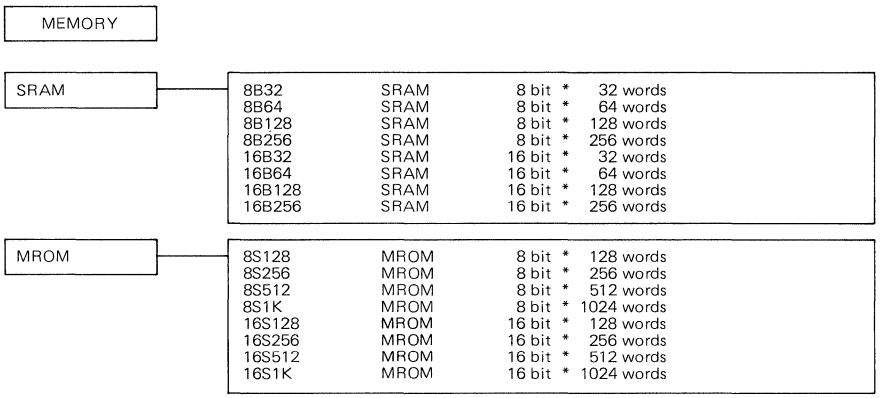
MULTIPLEXER

M298C	Quad 2-Input Multiplexer with Storage (74LS298)
M157C	Quad 2 Bit Gated Non Inverting Mux
M158C	Quad 2 Bit Gated Inverting Mux
M257C	Quad 2 Bit Gated Non Inverting Mux with 3-State Output
M258C	Quad 2 Bit Gated Inverting Mux with 3-State Output
M153C	Dual 4 Bit Gated Non Inverting Mux
M352C	Dual 4 Bit Gated Inverting Mux
M353C	Dual 4 Bit Gated Inverting Mux with 3-State Output
M253C	Dual 4 Bit Gated Non Inverting Mux with 3-State Output (74LS253)
M251C	8 Bit Gated Mux with 3-State Output (74LS251)
M151C	8 Bit Gated Mux
M152C	8 Bit Inverting Mux
M150C	16 Bit Gated Inverting Mux (74LS150)
MUX31H	3 Bit Non Inverting Mux
MUX31L	3 Bit Inverting Mux
MUX41H	4 Bit Non Inverting Mux
MUX41GH	4 Bit Gated Non Inverting Mux
MUX41L	4 Bit Inverting Mux
MUX51H	5 Bit Non Inverting Mux
MUX51L	5 Bit Inverting Mux
MUX61H	6 Bit Non Inverting Mux
MUX61L	6 Bit Inverting Mux
MUX71H	7 Bit Non Inverting Mux
MUX71L	7 Bit Inverting Mux
MUX81H	8 Bit Non Inverting Mux
MUX22H	Dual 2 Bit Non Inverting Mux
MUX32H	Dual 3 Bit Non Inverting Mux
MUX42H	Dual 4 Bit Non Inverting Mux
MUX52H	Dual 5 Bit Non Inverting Mux
MUX62H	Dual 6 Bit Non Inverting Mux
MUX72H	Dual 7 Bit Non Inverting Mux
MUX82H	Dual 8 Bit Non Inverting Mux
MUX24H	Quad 2 Bit Non Inverting Mux
MUX24L	Quad 2 Bit Inverting Mux
MUX34H	Quad 3 Bit Non Inverting Mux
MUX44H	Quad 4 Bit Non Inverting Mux
MUX54H	Quad 5 Bit Non Inverting Mux
MUX64H	Quad 6 Bit Non Inverting Mux
MUX74H	Quad 7 Bit Non Inverting Mux
MUX84H	Quad 8 Bit Non Inverting Mux


MULTIPLEX REGISTER
MR41 4 Bit Register with 2 Bit Multiplexed Input
MR42 4 Bit Register with 2 Bit Multiplexed Input, Clear Direct
MR43 4 Bit Register with 2 Bit Multiplexed Input, Sync Clear
MR44 4 Bit Register with 2 Bit Multiplexed Input, Sync Clear Reset B
MR81 8 Bit Register with 2 Bit Multiplexed Input
MR82 8 Bit Register with 2 Bit Multiplexed Input, Clear Direct
COUNTER
MODULO JOHNSON COUNTER
CM4J Modulo 4, Johnson Counter, Clear Direct
CM6J Modulo 6, Johnson Counter, Clear Direct
CM8J Modulo 8, Johnson Counter, Clear Direct
CM10J Modulo 10, Johnson Counter, Clear Direct
CM12J Modulo 12, Johnson Counter, Clear Direct
CM14J Modulo 14, Johnson Counter, Clear Direct
CM16J Modulo 16, Johnson Counter, Clear Direct
MODULO GRAY COUNTER
C2G Modulo 4, Gray Counter, Clear Direct
C3G Modulo 8, Gray Counter, Clear Direct
C4G Modulo 16, Gray Counter, Clear Direct
C5G Modulo 32, Gray Counter, Clear Direct
C6G Modulo 64, Gray Counter, Clear Direct, Prescaled
C7G Modulo 128, Gray Counter, Clear Direct, Prescaled
C8G Modulo 256, Gray Counter, Clear Direct, Prescaled
MODULO BINARY COUNTER
CM3B Modulo 3, Binary Counter, Clear Direct
CM4B Modulo 4, Binary Counter, Clear Direct
CM5B Modulo 5, Binary Counter, Clear Direct
CM6B Modulo 6, Binary Counter, Clear Direct
CM7B Modulo 7, Binary Counter, Clear Direct
CM8B Modulo 8, Binary Counter, Clear Direct
CM9B Modulo 9, Binary Counter, Clear Direct
CM10B Modulo 10, Binary Counter, Clear Direct
CM11B Modulo 11, Binary Counter, Clear Direct
CM12B Modulo 12, Binary Counter, Clear Direct
CM13B Modulo 13, Binary Counter, Clear Direct
CM14B Modulo 14, Binary Counter, Clear Direct
CM15B Modulo 15, Binary Counter, Clear Direct
CM16B Modulo 16, Binary Counter, Clear Direct
CM17B Modulo 17, Binary Counter, Clear Direct
MODULO BINARY RIPPLE COUNTER
CM8BR Modulo 8, Binary Ripple Counter, Clear Direct
CM9BR Modulo 9, Binary Ripple Counter, Clear Direct
CM10BR Modulo 10, Binary Ripple Counter, Clear Direct
CM11BR Modulo 11, Binary Ripple Counter, Clear Direct
CM12BR Modulo 12, Binary Ripple Counter, Clear Direct
CM13BR Modulo 13, Binary Ripple Counter, Clear Direct
CM14BR Modulo 14, Binary Ripple Counter, Clear Direct
CM15BR Modulo 15, Binary Ripple Counter, Clear Direct
CM16BR Modulo 16, Binary Ripple Counter, Clear Direct
CM17BR Modulo 17, Binary Ripple Counter, Clear Direct
CM18BR Modulo 18, Binary Ripple Counter, Clear Direct
CM19BR Modulo 19, Binary Ripple Counter, Clear Direct
CM20BR Modulo 20, Binary Ripple Counter, Clear Direct
CM21BR Modulo 21, Binary Ripple Counter, Clear Direct
CM22BR Modulo 22, Binary Ripple Counter, Clear Direct
CM23BR Modulo 23, Binary Ripple Counter, Clear Direct
CM24BR Modulo 24, Binary Ripple Counter, Clear Direct
CM25BR Modulo 25, Binary Ripple Counter, Clear Direct
CM26BR Modulo 26, Binary Ripple Counter, Clear Direct
CM27BR Modulo 27, Binary Ripple Counter, Clear Direct
CM28BR Modulo 28, Binary Ripple Counter, Clear Direct
CM29BR Modulo 29, Binary Ripple Counter, Clear Direct
CM30BR Modulo 30, Binary Ripple Counter, Clear Direct
CM31BR Modulo 31, Binary Ripple Counter, Clear Direct
CM32BR Modulo 32, Binary Ripple Counter, Clear Direct
MODULO SHIFT COUNTER
CM5SR Modulo 5, Shift Counter, Clear Direct
CM8SR Modulo 8, Shift Counter, Clear Direct
CM9SR Modulo 9, Shift Counter, Clear Direct
CM10SR Modulo 10, Shift Counter, Clear Direct
CM12SR Modulo 12, Shift Counter, Clear Direct



MODULO BINARY UP COUNTER	CB41	Modulo 16, Binary Up Counter, Expandable Enable Clear Direct
	CB42	Modulo 16, Binary Up Counter, Expandable Enable Sync Clear
	CB4C	Modulo 16, Binary Up Counter Fast, Sync Clear
	CB5C	Modulo 32, Binary Up Counter Fast, Sync Clear
	CB6C	Modulo 64, Binary Up Counter Fast, Sync Clear
	CB7C	Modulo 128, Binary Up Counter Fast, Sync Clear
	CB8C	Modulo 256, Binary Up Counter Fast, Sync Clear
	CB4F	Modulo 16, Binary Up Counter Fast, Individual Reset B & Set B
	CB5F	Modulo 32, Binary Up Counter Fast, Individual Reset B & Set B
	CB6F	Modulo 64, Binary Up Counter Fast, Individual Reset B & Set B
	CB7F	Modulo 128, Binary Up Counter Fast, Individual Reset B & Set B
	CB8F	Modulo 256, Binary Up Counter Fast, Individual Reset B & Set B
MODULO UP/DOWN COUNTER	CUD41	Modulo 16, Up/Down Counter, Expandable Enable Clear Direct
	CUD42	Modulo 16, Up/Down Counter, Expandable with Asynchronous Load and Clear
SYNCHRONOUS COUNTER	M393SC	Synchronous 4 Bit Binary Counter
	M161C	Synchronous 4 Bit Binary Counter (74LS161)
	M161D	Synchronous 4 Bit Binary Counter (74LS161)
	M163C	Synchronous 4 Bit Binary Counter (74LS163)
	M163D	Synchronous 4 Bit Binary Counter (74LS163)
	M163F	Synchronous 4 Bit Binary Counter, Optimized for Max Clock Freq
	M160C	Synchronous 4 Bit Bcd Counter (74LS160)
	M160D	Synchronous 4 Bit Bcd Counter (74LS160)
	M162C	Synchronous 4 Bit Bcd Counter (74LS162)
	M162D	Synchronous 4 Bit Bcd Counter (74LS162)
	M169C	Synchronous 4 Bit Up/Down Counter (74LS169)
MODULO LINEAR FEEDBACK SHIFT REGISTER	C3LSR	Modulo 7, Linear Feedback Shift Register
	C4LSR	Modulo 15, Linear Feedback Shift Register
	C5LSR	Modulo 31, Linear Feedback Shift Register
	C6LSR	Modulo 63, Linear Feedback Shift Register
	C7LSR	Modulo 127, Linear Feedback Shift Register
	C8LSR	Modulo 255, Linear Feedback Shift Register
CLOCK PRESCALER	PS2	Divide by 2 External Clock Prescaler with No Input Protection
	PS3	Divide by 3 External Clock Prescaler with No Input Protection
	PS4	Divide by 4 External Clock Prescaler with No Input Protection
TTL / CMOS MSI	M90C	Decade Counter (74LS90)
	M92C	Divided by Twelve Counter (74LS92)
	M93C	4 Bit Binary Counter (74LS93)
	M197C	Presetable 4 Bit Binary Counter (74LS197)
	M390C	Decade Counter (74LS390)
	M393C	4 Bit Binary Counter
	M4017C	Decade Counter/Driver (4017)
	M4520C	Dual Binary Up Counter


MEMORY
SRAM
8B32 SRAM 8 bit * 32 words
8B64 SRAM 8 bit * 64 words
8B128 SRAM 8 bit * 128 words
8B256 SRAM 8 bit * 256 words
16B32 SRAM 16 bit * 32 words
16B64 SRAM 16 bit * 64 words
16B128 SRAM 16 bit * 128 words
16B256 SRAM 16 bit * 256 words
MROM
8S128 MROM 8 bit * 128 words
8S256 MROM 8 bit * 256 words
8S512 MROM 8 bit * 512 words
8S1K MROM 8 bit * 1024 words
16S128 MROM 16 bit * 128 words
16S256 MROM 16 bit * 256 words
16S512 MROM 16 bit * 512 words
16S1K MROM 16 bit * 1024 words

TTL/RICOH CELL CORRESPONDENCE TABLE

TTL Name	RICOH Cell		TTL Name	RICOH Cell		TTL Name	RICOH Cell	
74LS00	NAND02		74LS112	M112C		74LS198	M198C	*
74LS02	NOR02		74LS113A	NJKC0S*6		74LS199	M199C	*
74LS04	INV01		74LS125	M125C		74LS240	M240C	
74LS08	AND02		74LS133	NAND13		74LS244	M244C	
74LS10	NAND03		74LS134	TNAN12		74LS245	M245C	
74LS11	AND03		74LS138	M138C	*	74LS251	M251C	
74LS20	NAND04			M138D		74LS253	M253C	
74LS21	AND04		74LS139	M139C		74LS257	M257C	
7425	NOR04*1		74LS145	M145C	*	74LS258	M258C	
74LS27	NOR03		74150	M150C		74LS260	NOR05	
74LS30	NAND08		74LS151	M151C		74LS273	M273C	
74LS32	OR02		74LS152	M152C			R82	*
7442	D410L	*	74LS153	M153C		74LS279	NRSLT*11	
	M42C		74LS154	M154C			M279C	
74LS43	M43C	*	74LS155	M155C		74LS295	M295C	
74LS44	M44C	*	74LS157	M157C		74LS298	M298C	*
74LS47	M47C	*	74LS158	M158C		74LS352	M352C	
74LS49	M49C	*	74LS160	M160C*7	*	74LS353	M353C	
74LS51	AOI22			M160D	*	74LS367A	M367C	
74LS54	AOI24		74LS161	M161C*8		74LS368A	M368C	*
7473	NJKCOR*2			M161D			TINVBF	
7474	NDCSR		74LS162	M162C*9	*		TBF368	
	N74NC*3			M162D	*	74LS374	M374C	*
7476	NJKCSR*4		74LS163	M163C*10	*	74LS390	M390C	*
74LS80	M80C*5	*		M163D		74LS393	M393C	
74LS82	M82C	*		M163F	*		M393SC*12	
	FA2	*	74LS164	M164C			CM16BR*13	*
74LS83	M83C	*	74LS165	M165C		74LS399	MR41	*
74LS85	M85C	*	74LS166	M166C		74LS540	M540C	
74LS86	XOR02		74LS169	M169C	*	74LS541	M541C	
74LS90	M90C	*	74LS171	R42	*	74LS640	M640C	
74LS91	M91C	*	74LS174	R82	*	4017	M4017C	*
74LS92	M92C	*	74LS175	R42		4028	M4028C	*
74LS93	M93C	*		M175C	*	4520	M4520C	*
74LS94	M94C	*	74LS179	M179C	*	4555	M4555C	*
74LS95	M95C		74LS180	M180C	*			
74LS96	M96C	*	74LS195	M195C	*			
74100	L4	*	74LS197	M197C	*			

* Only RSC-15 Series

*1 NOR04 has no strobe terminal.

*2, *4, *6
7473, 7476, and 74LS113A are negative edge triggers, but NJKC0R, NJKCSR and NJKC0S are positive edge triggers.

*3 7474 is a positive edge trigger, but N74NC is a negative edge trigger.

5 M80C has no 74LS80 A or B* terminals.

*7, *8, *9 and *10
M160C, M161C, M162C and M163C have inverted outputs.

*11 NRSLT has a QB terminal.

*12 M393SC is the sync equivalent of 74LS393.

*13 74LS393 is a negative edge trigger, but CM16BR is a positive edge trigger.

MEGA Cell Family

RICOH offers MEGA Cell Family of CMOS 1.5μ process. The optimal system design is obtained by using them with RICOH RSC15 Series standard cells.

We are currently developing additional cells. And, we also offer a service of developing customer-specific mega and super cells and adding them to the customer's library.

Mega Cell List

- TCC (Timer Counter)
- ACI (Asynchronous Communication Interface)
- PIO & HS (Parallel Input/Output and Handshake)
- INTC0, INTC1, INTC2 (Interrupt)
- ADC (Analog to Digital Converter)
- DAC (Digital to Analog Converter)

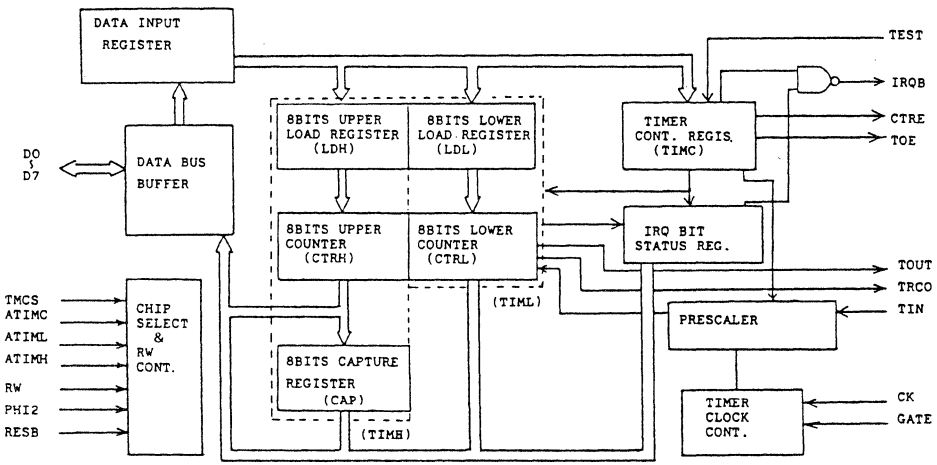
TCC Cell (Timer Counter)

The TCC cell is a 16-bit programmable timer-counter with the following features:

- **Four timer-counter modes**
  1. Interval timer mode : Normal timer-counter
  2. Pulse generation mode : Symmetrical or asymmetrical waveform pulses are generated.
  3. Event counter mode : The counter value is decremented according to input signals.
  4. Pulse width measurement mode : The low level period of input signals is measured.

- **1/16 prescaler**

Block Diagram



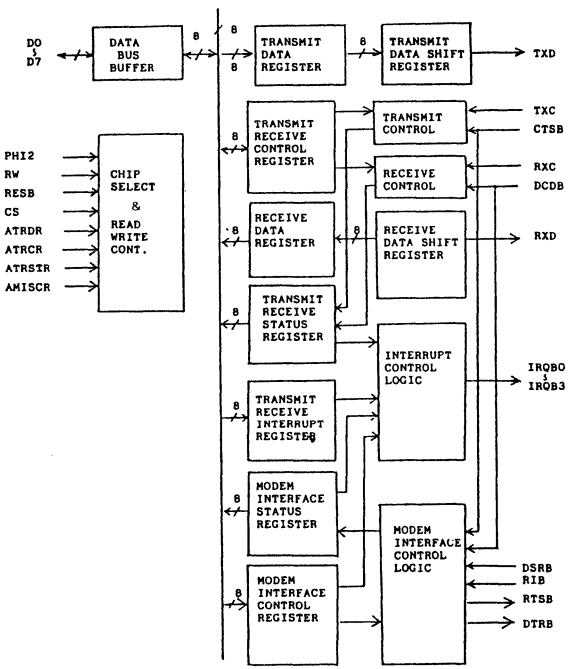
ACI Cell

(Asynchronous Communication Interface)

The ACI cell interfaces asynchronous communications for conversion between parallel and serial. The features are as follows:

- Choice between 7 or 8 data bits
- Choice of use of parity
- Choice between even or odd parity
- Choice of 1 or 2 bits for the stop bit
- Six modem control I/Fs: CTS, DCD, DSR, RI, RTS, and DTR.
- Break can be detected and transmitted.

Block Diagram



PIO & HS Cell

(Parallel Input / Output and Handshake)

The PIO cell is an 8-bit parallel input/output I/F cell.

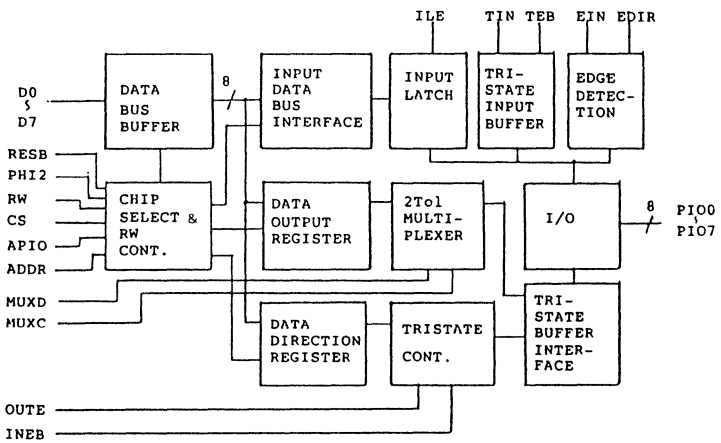
Its features are as follows:

- Input or output can be specified for each bit of input or output ports.
- It has an input latch.
- Edges can be detected.
- It supports the HS cell.

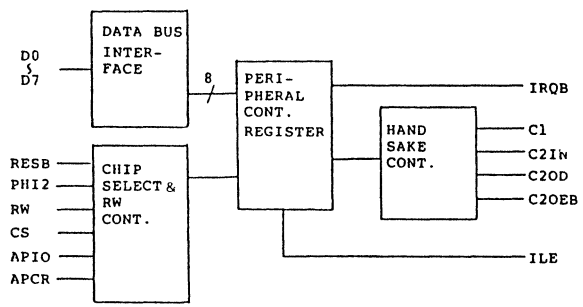
The HS cell is intended for controlling handshake. This cell is used with the PIO cell.

Block Diagram

(1) PIO



(2) HS



INTC0, INTC1, INTC2

(Interrupt Control)

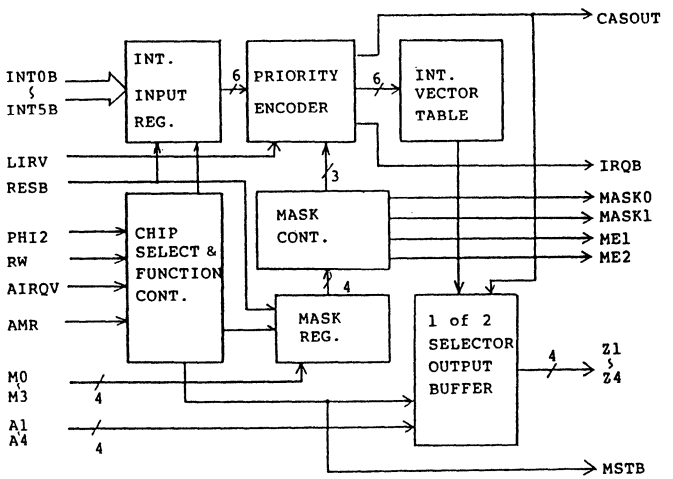
The INTC* cell is used exclusively for interrupt.

Its features are as follows:

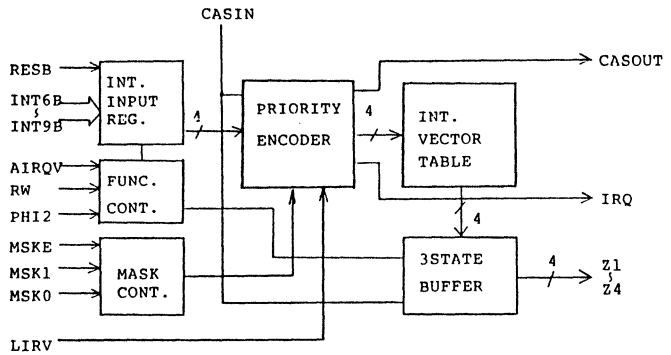
- The interrupt level can be chosen from 6, 10, or 14. The INTC0 cell is used for 6 or less. The INTC0 and INTC1 are connected and used for 7 to 10. The INTC0, INTC1, and INTC2 are connected and used for 11 to 14.
- The interrupt mask level can be specified.

Block Diagram

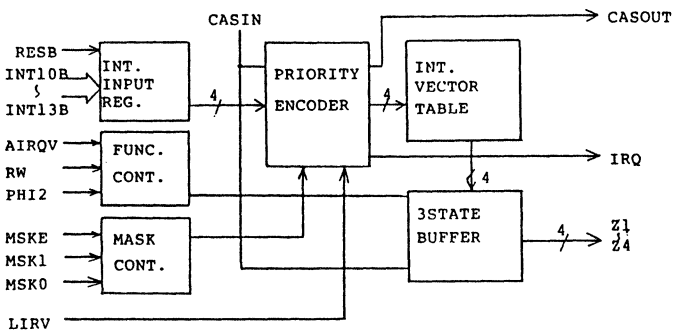
(1) INTC0



(2) INTC1



(3) INTC2



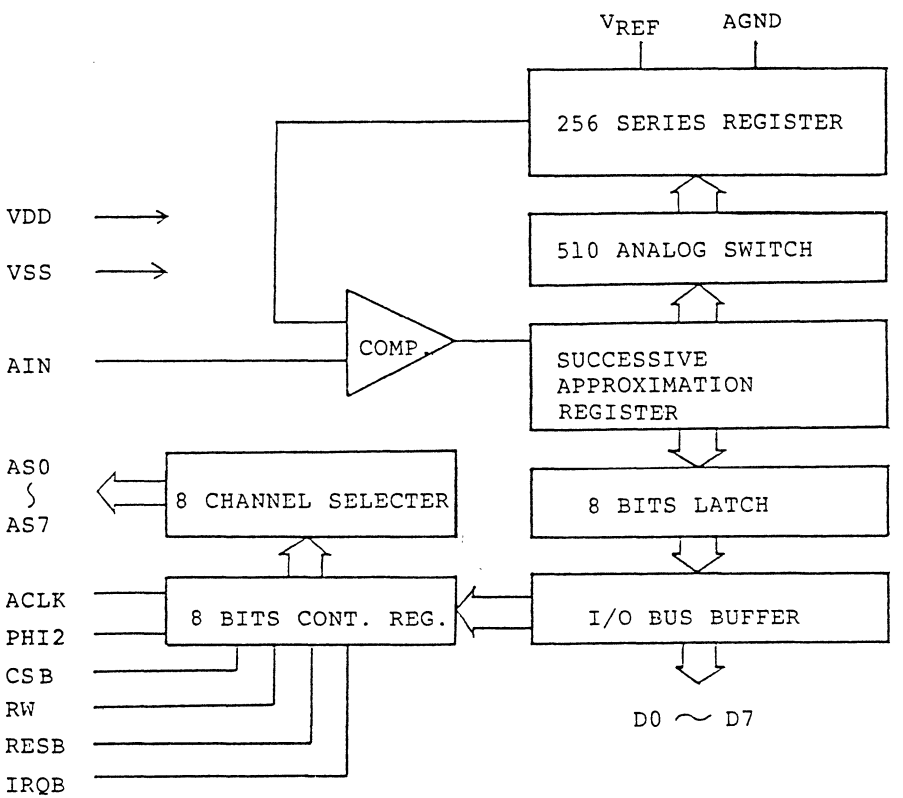
ADC Cell

(Analog to Digital Converter)

The ADC cell is an 8-bit analog to digital converter cell.
Its features are as follows:

- Succesive Approximation type
- High accuracy (nonlinear error ±1 LSB)
- High-speed conversion (71 μsec for fck = 2 MHz)
- 8-channel analog input
- 3-state output with latch
- 6-bit built-in control register

Block Diagram



DAC Cell

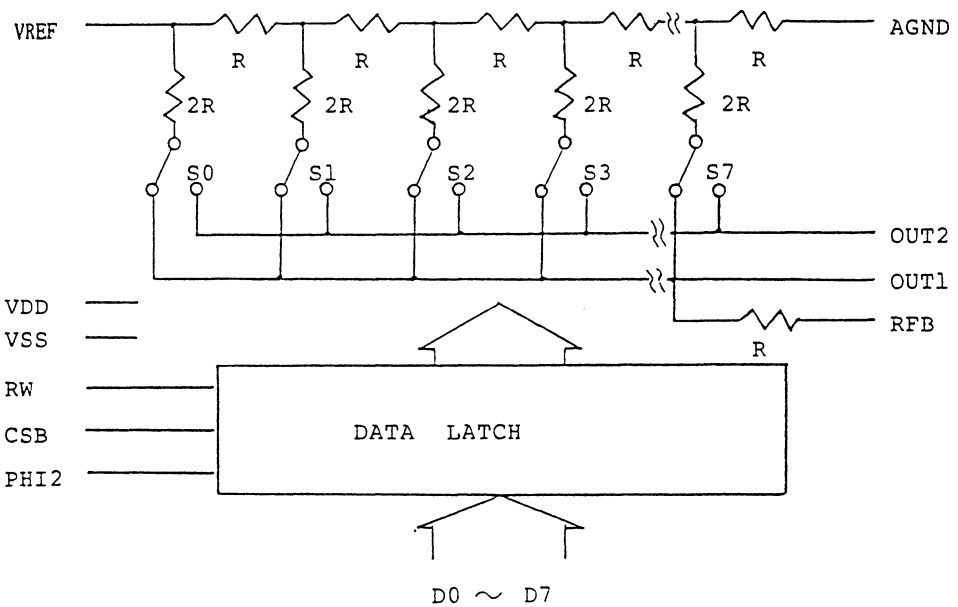
(Digital to Analog Converter)

The DAC cell is an 8-bit digital to analog converter.

Its features are as follows:

- R-2R type
- High accuracy in linearity (nonlinear error ±1 LSB)
- High-speed conversion (settling time: 1 μsec)
- 5V single power supply

Block Diagram



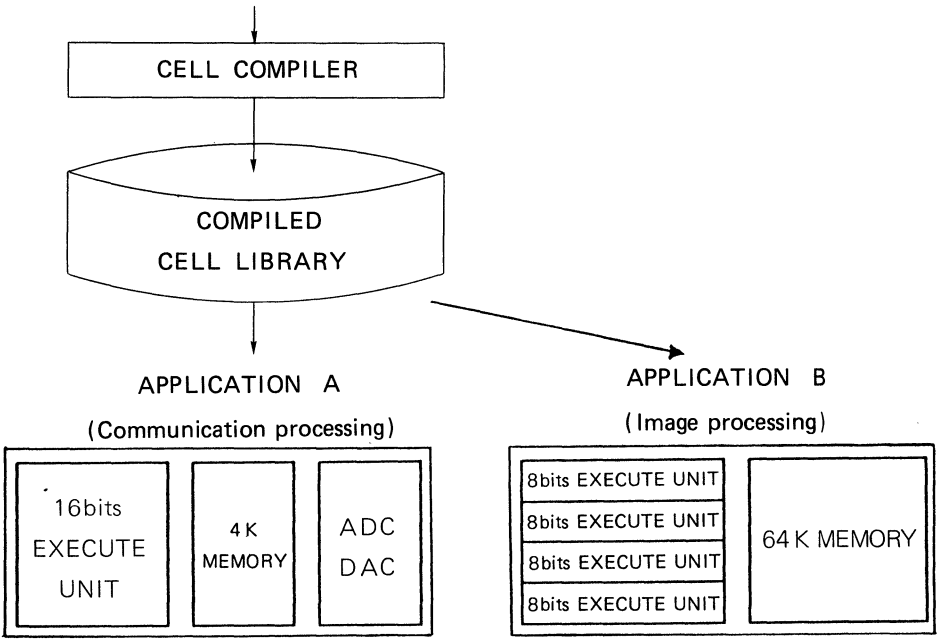
♦ Overview ♦

RICOH has added a cell library for Digital Signal Processing (DSP) to the standard cell family.

These cells are automatically generated by the cell compiler as the cell having an optional configuration, on the basis of parameter specified by the user. In addition, by combining these DSP cells with macro-cell and macro-function cell of 1.5μ standard cell RSC−15 Series, custom DSP which suit the customer's system can be developed easily.

Also, in the case where the application is limited to narrow range, Application Specific DSP can eliminate the redundant functions included in general-purpose DSP.

This makes it possible to design the circuit with more high speed and simplified configuration



(Example) Design of IIR Filter

In case where the conventional general-purpose DSP is used, its input/output bit width and internal register width have previously been fixed and they will sometimes fail to meet the specifications in respect of overflow in internal computation results, execution accuracy, etc., and at which time, it will require general-purpose DSP which has more capability than it should have, or require the change in specification due to lowered accuracy in execution. The use of RICOH DSP cell will solve such a problem as this.

♦ Features ♦

1. High speed operation is possible because CMOS 1.5μ design rules are used.
2. Each cell's processing data length is designed (using the cell complier) on a CAD basis. DSP can therefore be developed for any purpose.
3. The control unit uses the micro-programming, enabling it to handle any architecture.

♦ DSP Applications ♦

High performance of 10 to 20MHz can be achieved by using RICOH's DSP cells to answer various needs in digital signal processing.

- ○ Voice signal processing
  Analysis and synthesis, coding and decoding, recognition
- ○ Sound signal processing
  Digital analyzer, digital encorder, effector
- ○ Communication processing
  Modem, echo canceller, cryptograph
- ○ Image processing
  Medical and industrial image processing, character recognition
- ○ Measuring instruments
  Signal generating device, detection device
- ○ Machine control
  Motor control, robot arm control
- ○ High-speed numeric computing
  FFT computing, digital filter
- ○ Graphics

♦ Specifications common to each cell ♦

- Input/output I/F

Input	CMOS	fan-in	1
Output	CMOS	fan-out	3 (for wire length 3mm)

- Absolute maximum ratings

Vcc :	supply voltage	-0.3 ~ 7V
Topr:	operating temperature	0 ~ 70°C
Tstg :	storage temperature	-40 ~ 125°C

- Operation

Vcc :	supply voltage	5V±10%
Ta :	temperature	0 ~ 70°C

- DC characteristics

I/O cell of RSC-15 Series is used for external interface. For detail, refer the "DESIGN MANUAL".

D.C. electrical characteristics of I/O cell (Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

Symbol	Paramaters	Measuring Conditions	Limits			Unit
			Min	Typ	Max	
VIH	Input High Voltage(TTL)		2.0		Vcc+0.3	V
VIL	Input Low Voltage(TTL)		-0.3		0.8	V
VOH	Output High Voltage	IOH=-4mA	2.4			V
VOL	Output Low Voltage	IOL= 4mA			0.4	V
ILI	Input Leakage Current	VI=0~Vcc	-10		10	μA
ILO	Output Leakage Current	VO=0~Vcc	-10		10	μA

♦ DSP cell library list ♦

1. **MUL** (MULTIPLIER)
   MAX. 32 x 32bits operation (expandable by 2bits)
   option: ACCUMULATOR
2. **ALU** (ARITHMETIC LOGIC UNIT)
   MAX. 60bits operation (expandable by 4bits)
3. **ADS** (ADDER SUBTRUCTOR)
   MAX. 64bits operation (expandable by 4bits)
   option: RIPPLE CARRY/CARRY LOOK AHEAD
4. **BRS** (BARREL SHIFTER)
   MAX. I/O 32bits (expandable by 1bit)
   MAX. shift±32bits (expandable by 1bit)
5. **RGF** (REGISTER FILE)
   MAX. file 64bits x 256 words
   option: 1 port/2 ports
6. **DMX** (MULTIPLEXER)
   MAX. input 32bits x 8
7. **SEQ** (MICRO-PROGRAM SEQUENCER)
   MAX. address bit width 24bits
8. **PIP** (PIPE LINE REGISTER)
   MAX. data bit width 64bits
9. **MRO** (MASK ROM asynchronous)
   MAX. size 64K bits
   MAX. bits per word 16bits
   MAX. word length 32K words
10. **SRA** (SRAM asynchronous)
    MAX. size 16K bits
    MAX. bits per word 16bits
    MAX. word length 4K words

11. **S S R** (SRAM synchronous)
    MAX. size 8K bits
    MAX. bits per word 16bits
    MAX. word length 2K words

12. **H S R** (SRAM synchronous)
    MAX. size 32K bits
    MAX. bits per word 64bits
    MAX. word length 4K words

♦ DSP Cell Library ♦

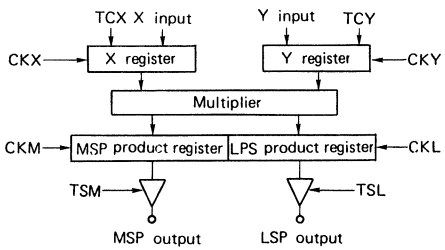
1. M U L (MULTIPLIER)

< Features >

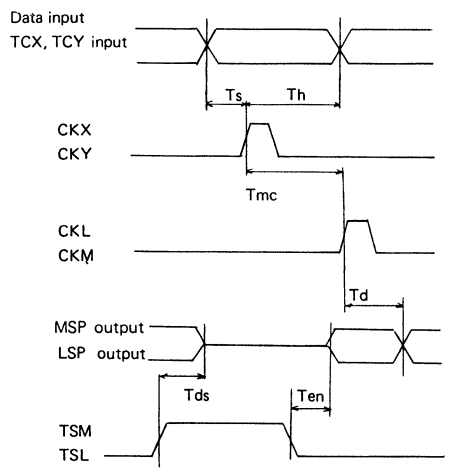
- An optional combination of data length from 6bits x 8bits minimum to 32bits x 32bits maximum is possible in unit of 2bits. (Example) 12 x 24, 8 x 16 and so on.
- Accumulator can be built-in for cumulative multiplication and addition. In this occasion, the maximum 8bits can be selected as an expandable bit. (Example) 12 x 12 + 32 → 32bits output.
- The output has 3-state control attached to enable an easy connection to the bus.
- It allows to use two's-complement or sign-magnitude numbers, while switching them with control terminals TCX & TCY.

(1) Multiplier

< Block diagram >



< AC characteristics >

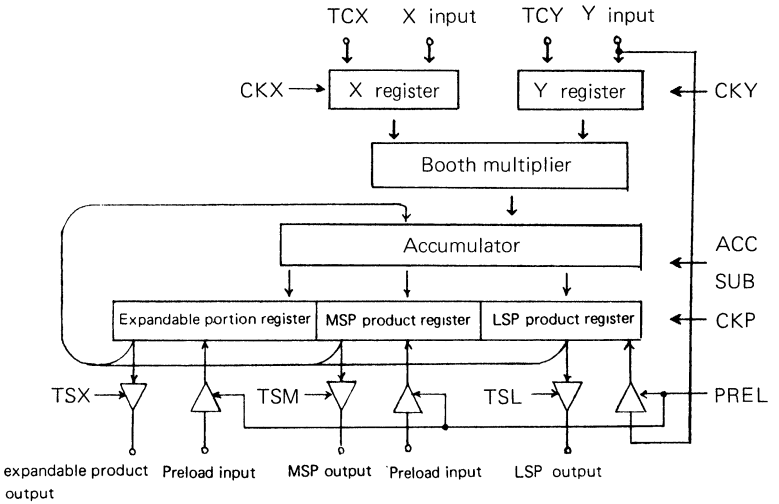


(Example) 16bits x 16bits multiplier

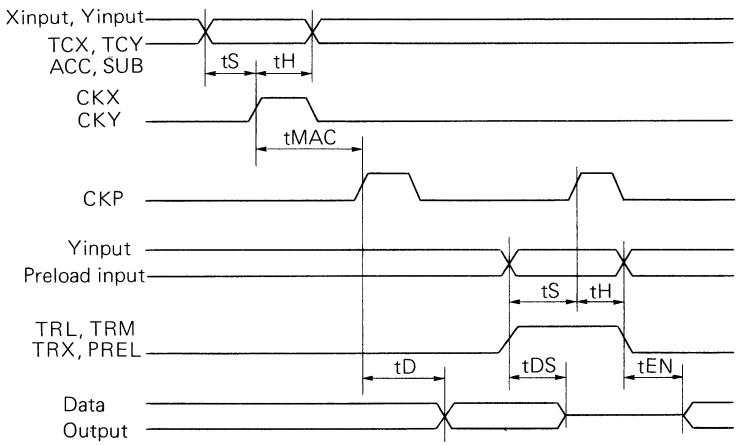
Ts	:	Bitup time	10nS
Th	:	Hold time	5nS
Tmc	:	Multiplication time	62nS
Td	:	Output delay time	15nS
Tds	:	Output disable time	20nS
Ten	:	Output enable time	20nS

(2) Multiplier/Accumulator

< Block diagram >



< AC characteristics >



(Example) 16bits x 16bits + expandable by 3bits, multiplier/accumulator

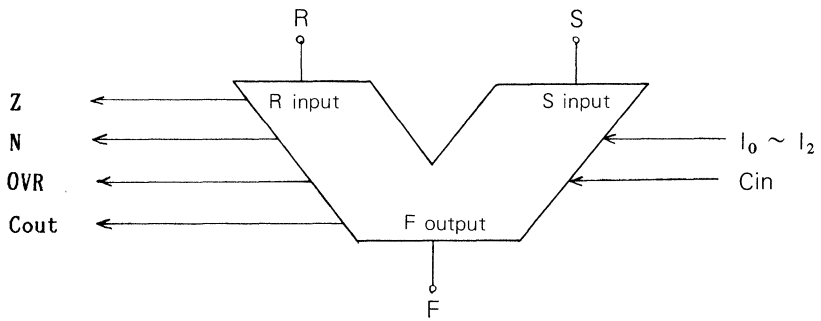
Ts	:	Setup time	10nS
Th	:	Hold time	5nS
Tmac	:	Cumulative multiplication addition time	72nS
Td	:	Output delay time	15nS
Tds	:	Output disable time	20nS
Ten	:	Output enable time	20nS

2. ALU (ARITHMETIC LOGIC UNIT)

< Features >

- Data length can be selected from 4bits minimum to 60bits maximum in unit of 4bits at option.

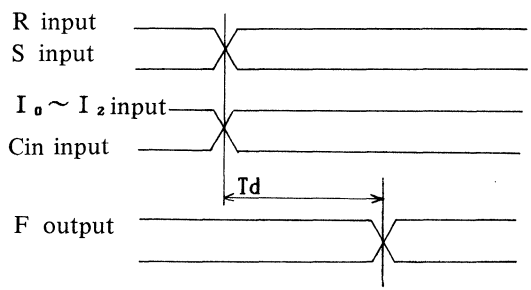
< Block diagram >



I_2	I_1	I_0	Function	
0	0	0	R + S + Cin	Arithmetic operation*
0	0	1	S − R − 1 + Cin	
0	1	0	R − S − 1 + Cin	
0	1	1	R or S	Logic operation
1	0	0	R AND S	
1	0	1	$\overline{R}$ AND S	
1	1	0	R ⊕ S	
1	1	1	$\overline{R \oplus S}$	

*Note: Two's-complement method

< AC characteristics >



(Example) 16bits ALU

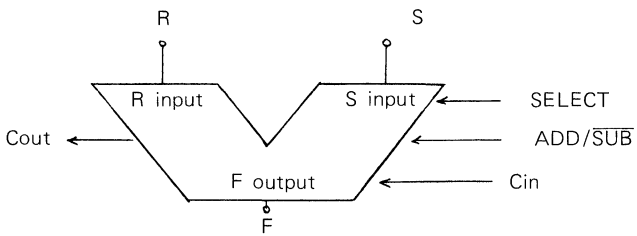
Td : ALU operation time 55nS

3. ADS (ADDER SUBTRACTOR)

< Features >

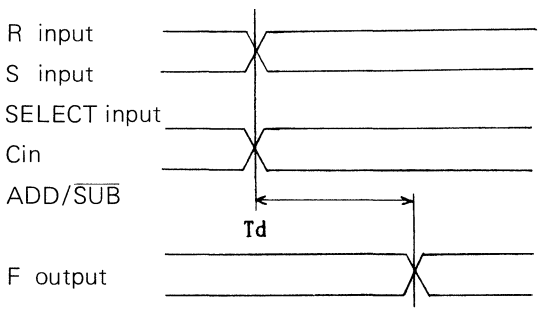
- Data length can be selected from 4bits minimum to 64bits maximum in unit of 4bits at option.
- In case of more than 36bits, ripple connection in 2 rows of 4bits CLA or hierarchical structure in 3row of 4bits CLA can be selected.

< Block diagram >



SELECT	ADD/SUB	ADS function
0	0	R + S + Cin
0	1	R − S − 1 + Cin
1	0	R + S
1	1	R − S

< AC characteristics >



(Example)

16bits Adder Subtractor

Td : Addition subtraction time 40nS

4. BRS (BARREL SHIFTER)

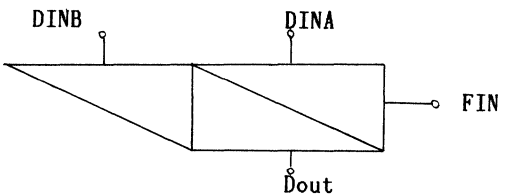
< Features >

- The number of input/output bits can be selected from 1 bit to 32 bits in unit of 1 bit at option.
- The number of shift can be set in optional number of shift from 1 bit shift to 32 bits shift at an optional interval.

Example 1) Number of input/output bit 18 bits
Number of shift 0, 1, 2, 4, 8, 16, 17, 18, 32

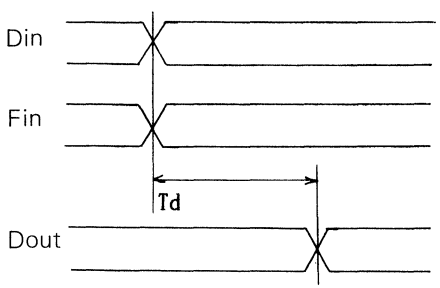
Example 2) Number of input/output bit 21 bits
Number of shift 0, 1, 2, 3, 30, 31, 32

< Block diagram >



Shift is controlled by Fin. Fin corresponds to the number of pieces of the number of shift and has 9 pieces in case of Example 1, while 7 pieces in case of Example 2. In addition, the number of shift is arranged in the order of smaller number such as Fin0, Fin1 . . .. In case of operating 8 bits shift in Example 1, arrange only Fin4 to "1" and Fin0~Fin3, Fin5~Fin9 to "0"

< AC characteristics >



(Example) 16bits width 16shifts function barrel shifter

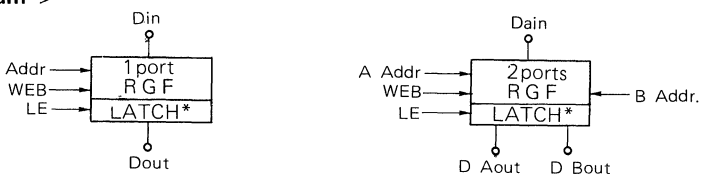
Td : Barrel shifter delay time 18nS

5. RGF (REGISTER FILE)

< Features >

- For file configuration, the word length from 6words minimum to 256words in unit of 2words and bit length from 1bit minimum to 64bits can be independently selected at option.
- 1port and 2ports can be selected.

< Block diagram >

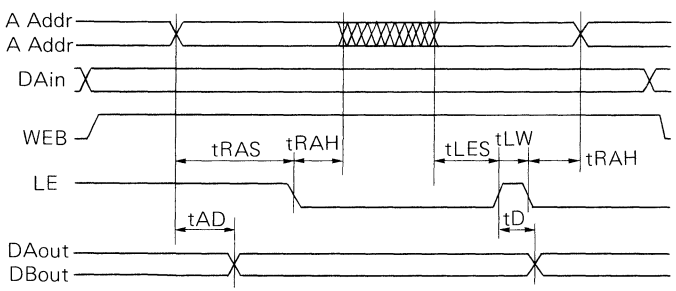


In case of 2ports, write to register is made to the address of A address. In case of read, the data specified by A address is output to A output port, while the data specified by B address is B output port respectively.

*Note: LE = 1, Output Latch is transparent.
LE = 0, Output Latch hold data

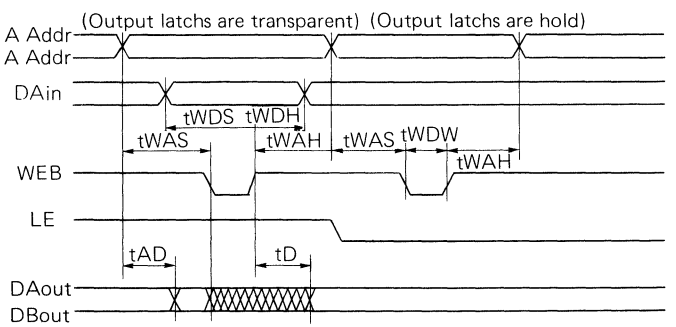
< AC characteristics >

***Read Cycle**



Note: When tLES is not satisfied spec, outputs are fixed from Address.

***Write Cycle**



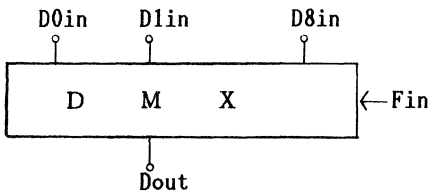
(Example) 32bits 32words 2ports register file

Tras	: Read address setup	28nS	Twds	: Write data setup	5nS
Trah	: Read address hold	1nS	Twdh	: Write data hold	3nS
Twas	: Write address setup	10nS	Td	: Clock → Output	29nS
Twah	: Write address hold	3nS	Tad	: Address → Output	39nS

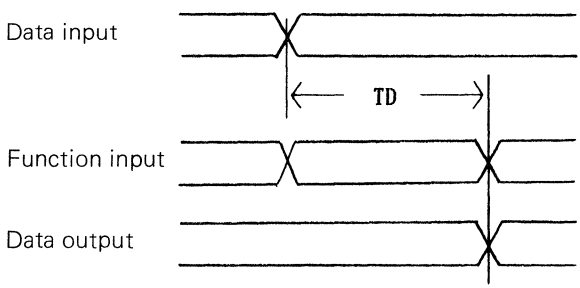
6. DMX (MULTIPLEXER)

< Features >

- Input bit length can be selected from 1 bit to 64 bits in unit of 1 bit at option.
- The number of input to be selected can be selected from 2 to 8 at option.



< AC characteristics >



(Example) 16bits 4inputs multiplexer

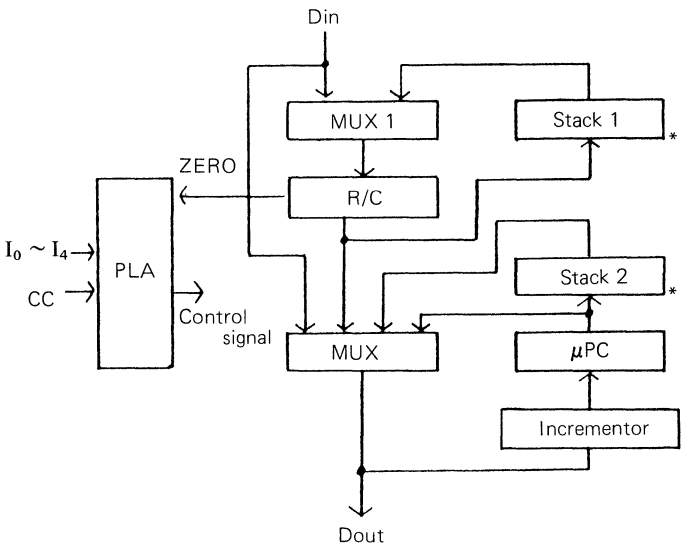
TD : Multiplexer data passing time 22nS

7. SEQ (MICRO-PROGRAM SEQUENCER)

< Features >

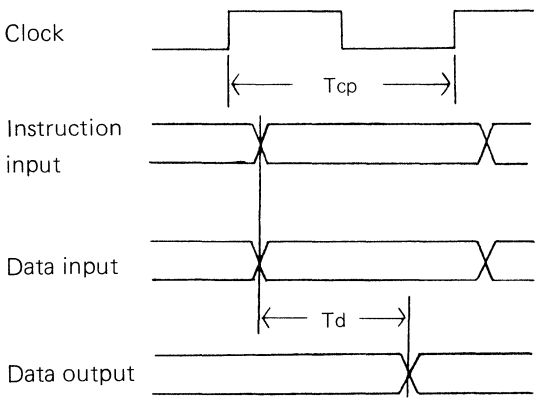
- Address width can be selected from 1 bit minimum to 24 bits maximum at option.
- Stack depth of micro-program counter (μPC) can be selected from 2 minimum to 14 maximum in unit of 1 at option.
- Since the register counter (R/C) is equipped with stack, it enables to nest the loop using R/C as loop counter.
- Stack depth of register counter can be selected from 2 minimum to 14 maximum in unit of 1 at option.

< Block diagram >



*Note: Each Stack can be set indevendently.

< AC characteristics >



(Example)

Sequence controller with address width 12 bits, stack depth at PC side 8 and stack depth at R/C side 6

Tcp :	Clock cycle	52nS
Td :	Instruction → Output	23nS

Table of the function

I_4 I_3 I_2 I_1 I_0	MNE-MONIC	R/C	MUX 1				MUX 2				R/C	ENABLE	
			FAIL		PASS		FAIL		PASS				
			DIN	Stack 1	DIN	Stack 1	Y	Stack 2	Y	Stack 2			
X 0 0 0 0	JZ	X	D	CLEAR	D	CLEAR	0	CLEAR	0	CLEAR	HOLD	PL	
X 0 0 0 1	CJS	X	D	HOLD	D	HOLD	PC	HOLD	D	PUSH	HOLD	PL	
X 0 0 1 0	JMAP	X	D	HOLD	D	HOLD	D	HOLD	D	HOLD	HOLD	MAP	
X 0 0 1 1	CJP	X	D	HOLD	D	HOLD	PC	HOLD	D	HOLD	HOLD	PL	
0 0 1 0 0	PUSH	X	D	HOLD	D	HOLD	PC	PUSH	PC	PUSH	NOTE1	PL	
X 0 1 0 1	JSRP	X	D	HOLD	D	HOLD	R	PUSH	D	PUSH	HOLD	PL	
X 0 1 1 0	CJV	X	D	HOLD	D	HOLD	PC	HOLD	D	HOLD	HOLD	VECT	
X 0 1 1 1	JRP	X	D	HOLD	D	HOLD	R	HOLD	D	HOLD	HOLD	PL	
0 1 0 0 0	RFCT	≠0	D	HOLD	D	HOLD	F	HOLD	F	HOLD	DEC	PL	
		=0	D	HOLD	D	HOLD	PC	POP	PC	POP	HOLD	PL	
0 1 0 0 1	RPCT	≠0	D	HOLD	D	HOLD	D	HOLD	D	HOLD	DEC	PL	
		=0	D	HOLD	D	HOLD	PC	HOLD	PC	HOLD	HOLD	PL	
X 1 0 1 0	CRTN	X	D	HOLD	D	HOLD	PC	HOLD	F	POP	HOLD	PL	
X 1 0 1 1	CJPP	X	D	HOLD	D	HOLD	PC	HOLD	D	POP	HOLD	PL	
0 1 1 0 0	LDCT	X	D	HOLD	D	HOLD	PC	HOLD	PC	HOLD	LOAD	PL	
X 1 1 0 1	LOOP	X	D	HOLD	D	HOLD	F	HOLD	PC	POP	HOLD	PL	
X 1 1 1 0	CONT	X	D	HOLD	D	HOLD	PC	HOLD	PC	HOLD	HOLD	PL	
X 1 1 1 1	TWB	≠0	D	HOLD	D	HOLD	F	HOLD	PC	POP	DEC	PL	
		=0	D	HOLD	D	HOLD	D	POP	PC	POP	HOLD	PL	
1 0 1 0 0	NPUSH	X	D	HOLD	D	PUSH	PC	PUSH	PC	PUSH	NOTE1	PL	
1 1 0 0 0	NRFCT	≠0	D	HOLD	D	HOLD	F	HOLD	F	HOLD	DEC	PL	NOTE2
		=0	F	POP	F	POP	PC	POP	PC	POP	LOAD	PL	
1 1 0 0 1	NRPCT	≠0	D	HOLD	D	HOLD	D	HOLD	D	HOLD	DEC	PL	
		=0	F	POP	F	POP	PC	HOLD	PC	HOLD	LOAD	PL	
1 1 1 0 0	NLDCT	X	D	PUSH	D	PUSH	PC	HOLD	PC	HOLD	LOAD	PL	

X: Don't care.

NOTE1: When $\overline{CCEN}$ = 'L' & $\overline{CC}$ = 'H': HOLD
Otherwise LOAD

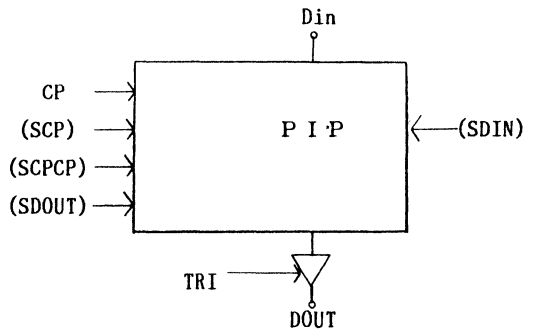
NOTE2: These instructions are for the nested loop using register counter.

8. PIP (PIPE LINE REGISTER)

< Features >

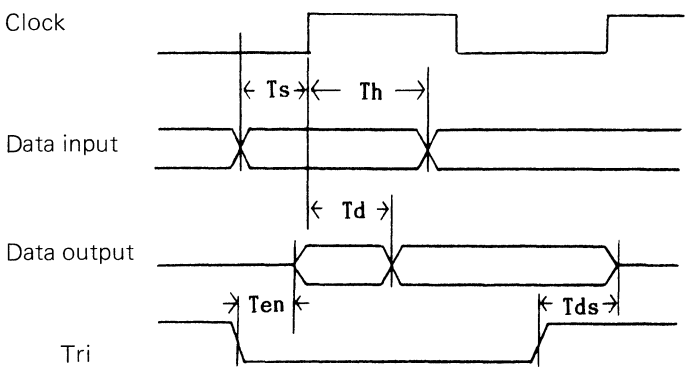
- Data bit length can be selected from 1 bit minimum to 64 bits maximum in unit of 1 bit at option.
- It enables to select whether or not to have scanpath function.
- Since the output has 3-state control attached, it enables to connect to bus easily.

< Block diagram >



Paraenthesis ( ) is used when selecting scanpath function.

< AC characteristics >



(Example) 32bits pipe line register with scanpath attached

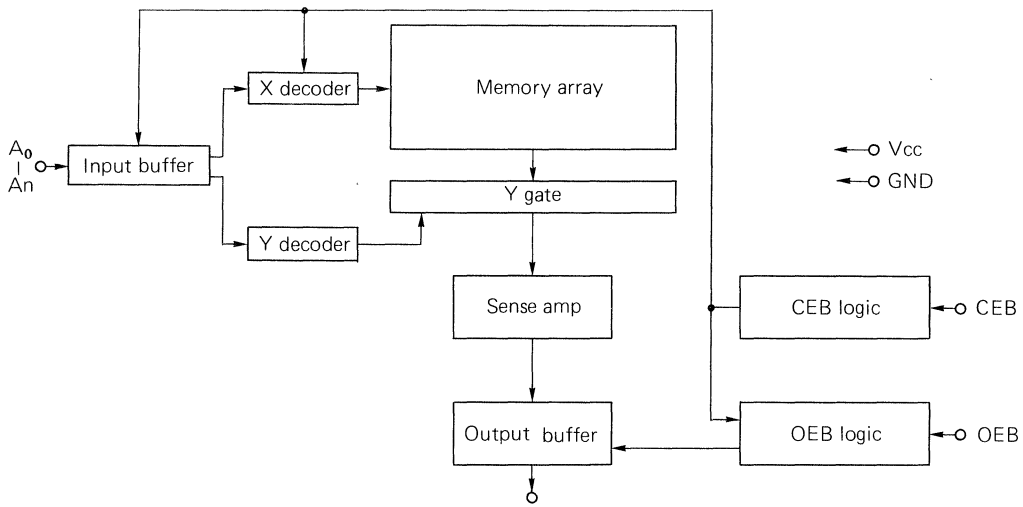
Ts	: Setup time	5nS
Th	: Hold time	0nS
Td	: Clock → Output	18nS
Ten	: 3-state enable	15nS
Tds	: 3-state disable	15nS

9. M R O (Asynchronous Mask ROM)

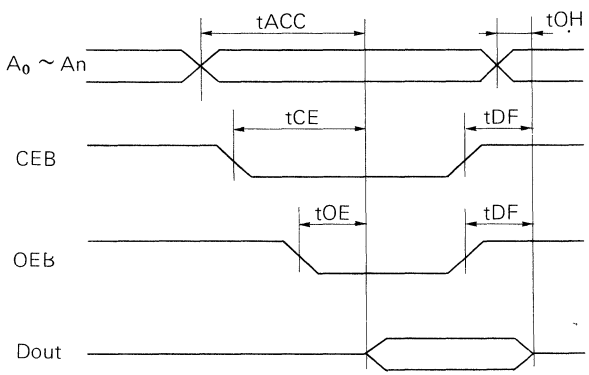
< Features >

- Word by bits organization can be selected within the following range.
  - Maximum size 64K bits
  - Bits per word 8 ~ 16bits
  - Word length 128 ~ 32K words
- Fast access time 55nS (4K x 16)
- Low power dissipation (Active) 28mA (Output data 16bits, f = 20 MHz)
  (Standby) 10μA
- Two control inputs CEB, OEB

< Block diagram >



< AC characteristics >



10. S R A (Asynchronous SRAM)

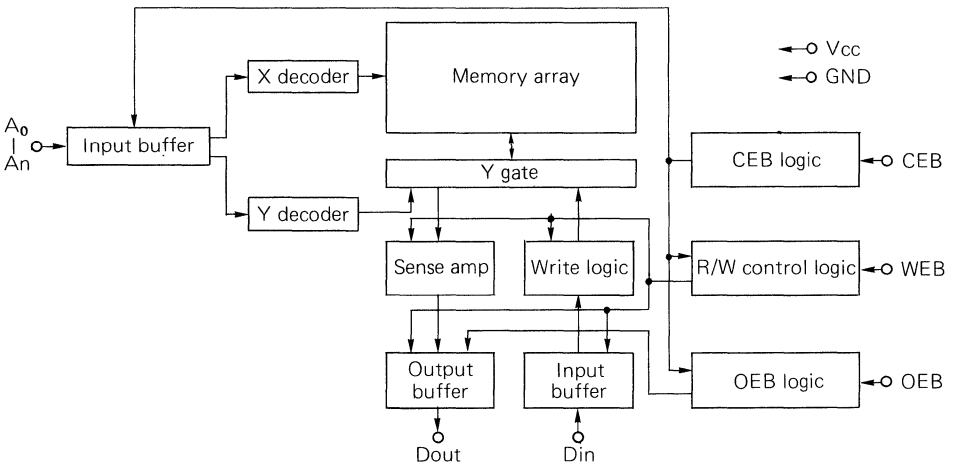
< Features >

- Word by bits organization can be selected within the following range.

Maximum size	16K bits
Bits per word	2 ~ 8, 16bits
Word length	32 ~ 4K words

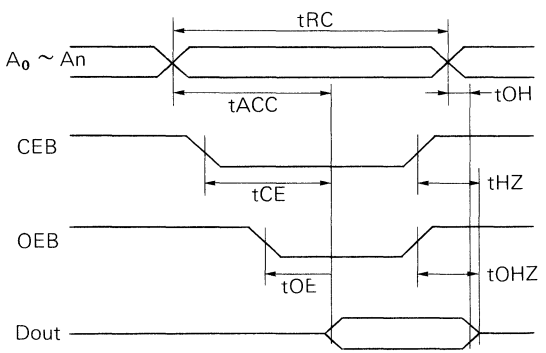
- Fast access time 65nS (Bit width 16bits)
- Low power dissipation (Active) 40mA (Output data 8bits, f = 10 MHz)
  (Standby) 10μA
- Three control inputs CEB OEB, WEB

< Block diagram >



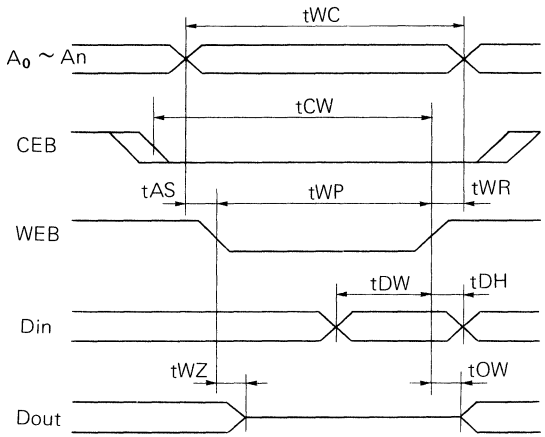
< AC characteristics >

***Read Cycle**

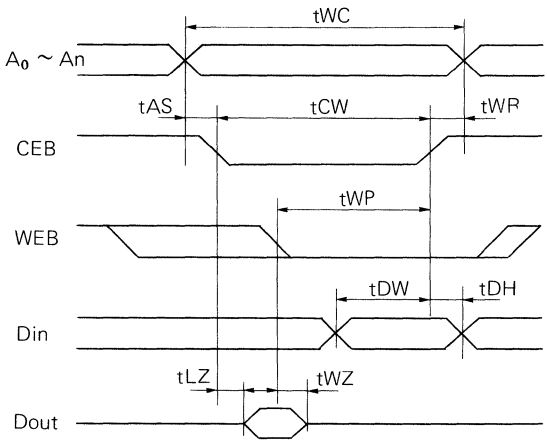


***Write Cycle**

WEB control



CEB control



11. S S R (Synchronous SRAM)

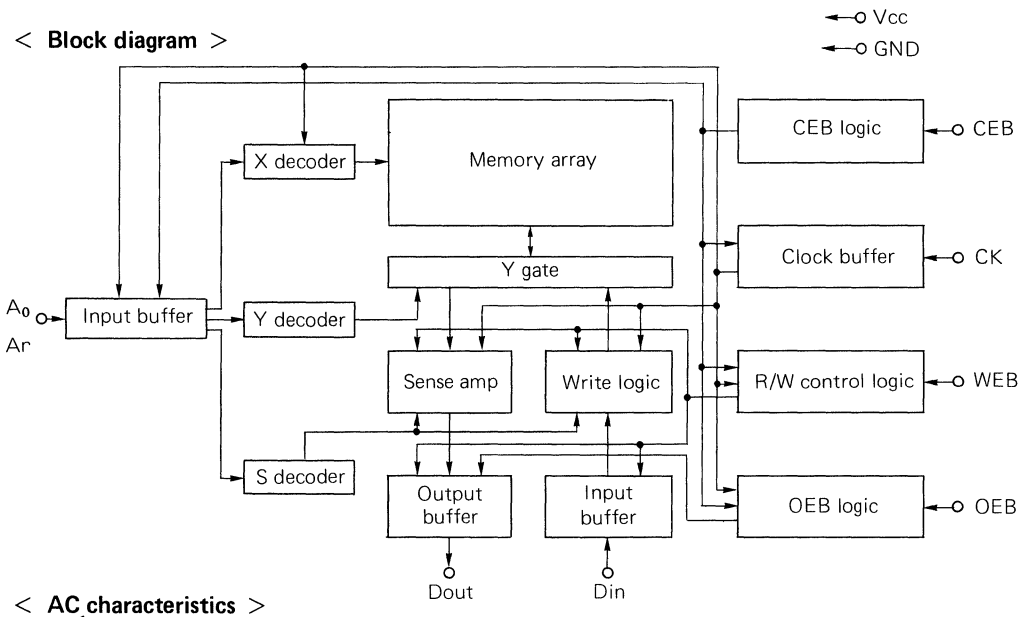
< Features >

- Word by bits organization can be selected within the following range.

Maximum size	8K bits
Bits per word	2 ~ 16bits
Word length	32 ~ 2K words

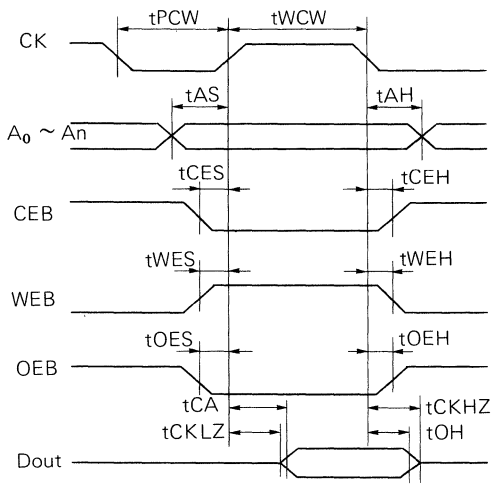
- Fast access time 50nS (256 x 16)
- Low power dissipation (Active) 15mA (Output data 16bits, f = 10 MHz)
  (Standby) 10μA
- One clock input & Three control inputs CK, CEB, OEB, WEB

< Block diagram >

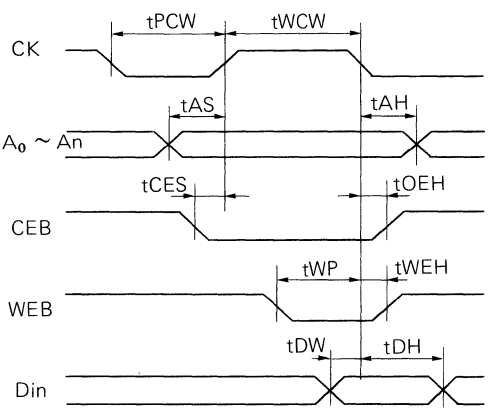


< AC characteristics >

***Read Cycle**



***Write Cycle**



12. H S R (Synchronous SRAM)

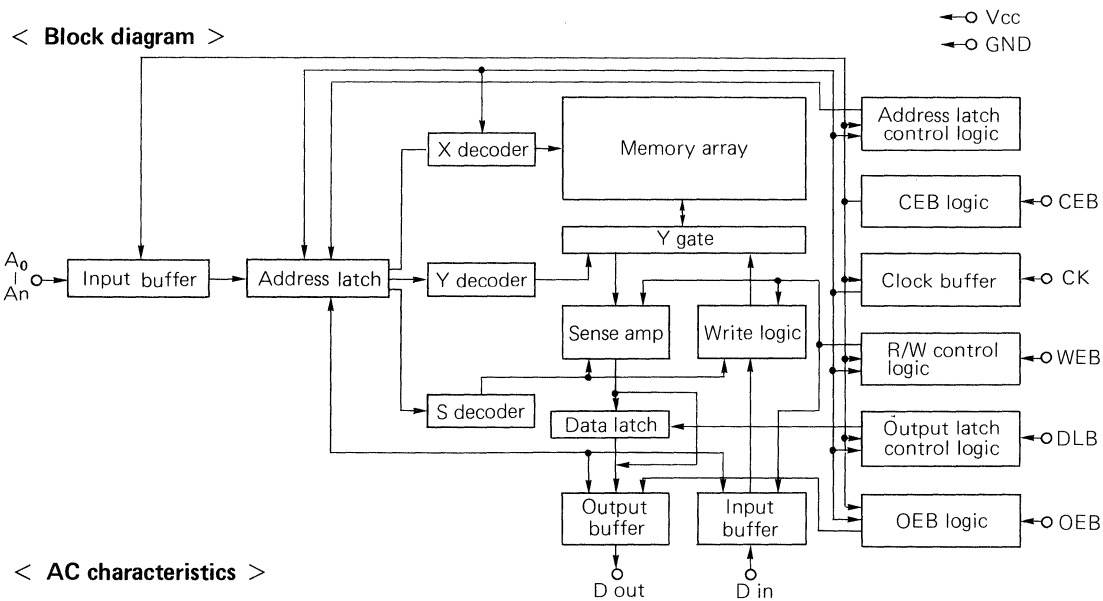
< Features >

- Word by bits organization can be selected within the following range.

Maximum size	32K bits
Bits per word	2 ~ 64bits
Word length	32 ~ 4K words

- Fast access time 25nS (256 x 16)
- Low power dissipation (Active) 15mA (Output data 16bits, f = 10 MHz)
  (Standby) 10μA
- One clock input & Three control inputs CK, CEB, OEB, WEB
- Either Data Latch Mode or Non Data Latch Mode can be selected. Latch Mode will be fixed after compilation.

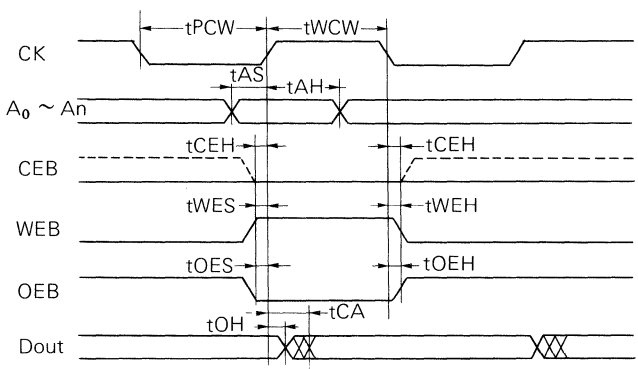
< Block diagram >



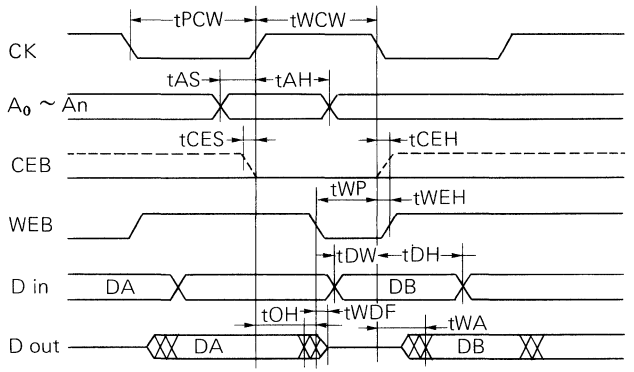
< AC characteristics >

i) Data Latch Mode (DLB = "L")

***Read Cycle**



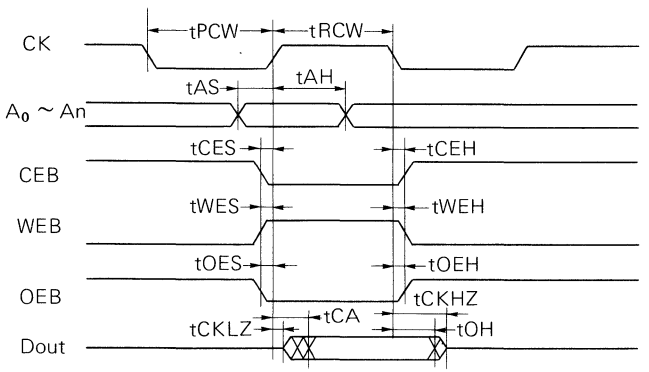
***Write Cycle**



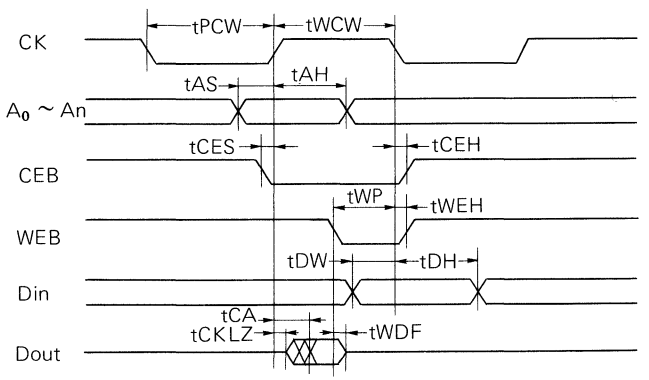
Note: tWDF is specified from CK or WEB, whichever occurs last.

ii) Non Data Latch Mode (DLB = "H")

***Read Cycle**



***Write Cycle**



Note: tWDF is specified from CK or WEB, whichever occurs last.

♦ AC characteristics table ♦

1. MUL (MULTIPLIER)

Symbol	Parameter	AC characteristics
Ts	Data setup time	MIN 10nS
Th	Data hold time	MIN 5nS
Td	Output delay time (Clock → Output)	MAX 15nS
Tds	Output disable time	MAX 20nS
Ten	Output enable time	MAX 20nS
Tmc	Multiplication time	In case of multiplier (i) When the larger one of X input and Y input is below 16bits, X + Y + 30nS (ii) When the larger one of X input and Y input is above 18bits and below 24bits, (X+Y) * 1.25 + 30nS (iii) When the larger one of X input and Y input is above 26bits and below 32bits, (X+Y) * 1.25 + 40nS
Tmac	Cumulative multiplication addition time	In case of multiplier/accumulator (i) When the larger one of X input and Y input is below 16bits, Y + Y + 40nS (ii) When the larger one of X input and Y input is above 18bits and below 24bits, (X+Y) * 1.25 + 40nS (iii) When the larger one of X input and Y input is above 26bits and below 32bits, (X+Y) * 1.25 + 50nS

2. ALU (ARITHMETIC LOGIC UNIT)

Symbol	Parameter	AC characteristics
Td	ALU operation time	Bit length 4, 8 — 50 [nS] 12, 16 — 55 [nS] 20, 24 — 65 [nS] 28, 32 — 70 [nS] 36, 40 — 80 [nS] 44, 48 — 90 [nS] 52, 56 — 100 [nS] 60, 64 — 110 [nS]

3. ADS (ADDER SUBTRACTOR)

Symbol	Parameter	AC characteristics
Td	Addition substraction excution time (Ripple)	$5 * m/16 + 35$ [nS] $(4 \leqq m \leqq 64$, m: bit length)
	Addition subtraction excution time (Carry look ahead)	$5 * m/16 + 35$ $(4 \leqq m \leqq 32)$ $5 * m/16 + 30$ $(36 \leqq m \leqq 48)$ [nS] $5 * m/16 + 25$ $(52 \leqq m \leqq 64)$ (m: bit length)

4. BRS (BARREL SHIFTER)

Symbol	Parameter	AC characteristics
Td	Barrel shifter passing time	$0.5 * m + 10$ [nS] (m is bit length)

5. RGF (REGISTER FILE)

Symbol	Parameter	AC characteristics	
Tras	Read address setup time	A + B/4 + 5	[nS]
Trah	Read address hold time	1	[nS]
Twas	Write address setup time	A + 5	[nS]
Twah	Write address hold time	A/4 + 1	[nS]
Twds	Write data setup time	A	[nS]
Twdh	Write data hold time	A/4 + 1	[nS]
Td	Clock → output delay time WEB → output delay time	B/4 + 21	[nS]
Tad	Address→output delay time	A * 2 + B/4 + 21	[nS]
Tles	Latch enable setup time	A * 2	[nS]
Twdw	Write enable pulse width	B/4 + 1	[nS]
Tlw	Latch enable pulse width	B/4 + 1	[nS]

Note: When word length is below:

6 ~ 8 words	A = 3	34 ~ 64 words	A = 6
10 ~ 16 words	A = 4	66 ~ 128 words	A = 7
18 ~ 32 words	A = 5	130 ~ 256 words	A = 8

6. DMX (MULTIPLEXER)

Symbol	Parameter	AC characteristics	
Td	Multiplexer passing time	m/4 + 18 (m is bit length)	[nS]

7. SEQ (MICRO-PROGRAM SEQUENCER)

Symbol	Parameter	AC characteristics	
Td	Instruction input → output delay	23	[nS]
Tcp	Clock cycle	m + 40 (m is address width)	[nS]

8. PIP (PIPE LINE REGISTER)

Symbol	Parameter	AC characteristics	
Ts	Setup time	5	[nS]
Th	Hold time	0	[nS]
Ten	Output enable time	15	[nS]
Tds	Output disable time	15	[nS]
Td	Clock → output delay	m/16 + 16 (m is bit length)	[nS]

9. MRO (Asyncronous Mask ROM)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
tACC	Address access time	Fan Out = 3 Wire length = 3mm			Note1	nS
tCE	CEB access time				Note1	nS
tOE	OEB access time				20	nS
tDF	OEB or CEB to output in high Z		0			nS
tOH	Output hold from address change		0			nS

Note 1: $0.46 \times (V-1) + 0.26 \times (H-2) + 37.1$

$9 \leqq$ Bit $\leqq 16$ ..... V = WORD/128, H = Bit

$5 \leqq$ Bit $\leqq 8$

$256 \leqq$ WORD ..... V = WORD/256, H = 2 x Bit

$128 \leqq$ WORD < 256 ..... V = WORD/128, H = Bit

$3 \leqq$ Bit $\leqq 4$

$512 \leqq$ WORD ..... V = WORD/512, H = 4 x Bit

$256 \leqq$ WORD < 512 ..... V = WORD/256, H = 2 x Bit

$128 \leqq$ WORD < 256 ..... V = WORD/128, H = Bit

Bit = 2

$1024 \leqq$ WORD ..... V = WORD/1024, H = 8 x Bit

$512 \leqq$ WORD < 1024 ..... V = WORD/512, H = 4 x Bit

$256 \leqq$ WORD < 512 ..... V = WORD/256, H = 2 x Bit

$128 \leqq$ WORD < 256 ..... V = WORD/128, H = Bit

10. S R A (Asyncronous SRAM)

*Read Cycle

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
tRC	Read cycle time	Fan Out = 3 Wire length = 3mm	Note2			nS
tACC	Address access time				Note2	nS
tCE	CEB access time				Note2	nS
tOE	OEB access time				30	nS
tOH	Output hold from address change		0			nS
tHZ	CEB-output disable time		0		30	nS
tOHZ	OEB-output disable time		0		30	nS

Note 2: Bit = 2, 3 ..... tACC/tCE = 60nS
Bit = 4, 8, 16 ..... tACC/tCE = 65nS
Bit = 5, 6, 7 ..... tACC/tCE = 70nS

*Write Cycle

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
tWC	Write cycle time		60			nS
tWP	Write pulse width		45			nS
tCW	Chip selection to end of write		45			nS
tAS	Address setup time		0			nS
tWR	Write recovery time		15			nS
tDW	Data valid to end of write		15			nS
tDH	Data hold time		10			nS
tWZ	WEB to output in high Z		5			nS
tOW	WEB to output in low Z				30	nS
tLZ	CEB to output in low Z				30	nS

11. S S R (Syncronous SRAM)

***Read Cycle**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
tPCW	Clock width for precharge cycle	Fan Out = 3 Wire length = 3mm	60			nS
tRCW	Clock width for read cycle		60			nS
tCA	Clock access time				Note3	nS
tAS	Address setup time		20			nS
tAH	Address hold time		3			nS
tCES	CEB setup time		10			nS
tCEH	CEB hold time		0			nS
tWES	WEB setup time		0			nS
tWEH	WEB hold time		0			nS
tOES	OEB setup time		0			nS
tOEH	OEB hold time		0			nS
tCKLZ	CK to output in low Z				5	nS
tCKHZ	CK to output in high Z		0		10	nS
tOH	Output hold from CK change		2			nS

Note 3: Less than 4K bits: 50nS
More than 4K bits: 59nS

***Write Cycle**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
tPCW	Clock width for precharge cycle		60			nS
tWCW	Clock width for write cycle		60			nS
tWP	Write pulse width		30			nS
tAS	Address setup time		20			nS
tAH	Address hold time		0			nS
tDW	Data valid to end of write		20			nS
tDH	Data hold time		5			nS
tCES	CEB setup time		0			nS
tCEH	CEB hold time		0			nS
tWEH	WEB hold time		0			nS

12. H S R (Synchronous SRAM)

***Read Cycle**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
tPCW	Clock width for prechange cycle	Fan Out = 3 Wire length = 3mm	25			nS
tRCW	Clock width for read cycle		Note4			nS
tCA	Clock access time				Note4	nS
tAS	Address setup time		10			nS
tAH	Address hold time		5			nS
tCES	CEB setup time		10			nS
tCEH	CEB hold time		0			nS
tWES	WEB setup time		0			nS
tWEH	WEB hold time		0			nS
tOES	OEB setup time		0			nS
tOEH	OEB hold time		0			nS
tCKLZ	CK to output in low Z				10	nS
tCKHZ	CK to output in high Z		0		10	nS
tOH	Output hold from CK change		5			nS

***Write Cycle**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
tPCW	Clock width for prechange cycle		25			nS
tWCW	Clock width for write cycle		Note4			nS
tWP	Write pulse width		Note4			nS
tAS	Address setup time		10			nS
tAH	Address hold time		5			nS
tDW	Data valid to end of write		15			nS
tDH	Data hold time		10			nS
tCES	CEB setup time		0			nS
tCEH	CEB hold time		0			nS
tWEH	WEB hold time		0			nS
tWA	WEB access time				10	nS
tWDF	CK or WEB to output in high Z		0			nS

Note 4: tCA, tWP = 2 x BITS x SHAPE/16 + 1.2 x WORDS/SHAPE/256 + 31.8 [nS]
tRCW, tWCW = 2 x BITS x SHAPE/16 + 1.2 x WORDS/SHAPE/256 + 36.8 [nS]

BITS ..... Bits per word
WORDS ..... Word length
SHAPE ..... See right table

Word length	SHAPE
32 ~ 512	1
513 ~ 1024	2
1025 ~ 2048	4
2059 ~ 4096	8

♦ DSP EMULATION CHIP SET LIST ♦

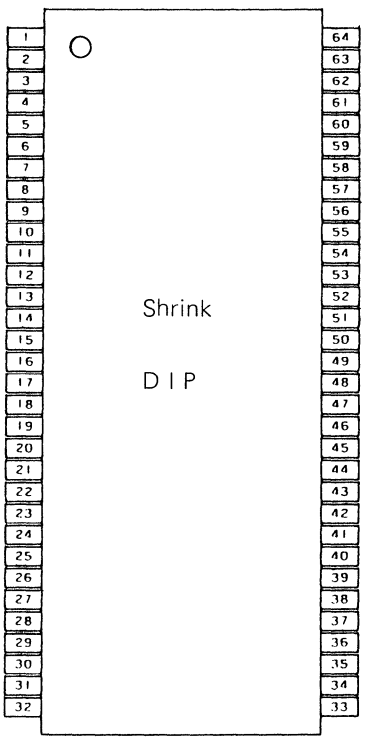
RICOH can offer emulation chip set for the preparation of breadboard required for the development of product, using DSP cell library.

There are 6 different kinds of emulation chips available as follows.

1. RP5S1016 ..... 16bits x 16bits multiplier
2. RP5S1010 ..... 16 bits x 16bits expandable by 3bits multiplier/accumulator
3. RP5S3910 ..... Address width 16bits micro-program sequencer
   μPC side stack depth 8
   R/C side stack depth 6
4. RP5S3030 ..... 16bits width barrel shifter (optional shift from 0 to 16bits)
5. RP5S3010 ..... 16bits length arithmetic logic operation unit
6. RP5S3020 ..... 16bits 32words 2ports register file

These chips are all offered in 64pins shrink DIP package or 64pins flat package.

Pin configuration diagram



♦ EMULATION CHIP ♦

1. RP5S1016 (16bits x 16bits multiplier)

< Features >

- TTL compatible low power consumption CMOS multiplier
- Multiplication time 50nS
- Complements display of 2
  Display of absolute values and their mixed mode multiplication
- Single + 5V power supply
- Suppliable with shrink DIP 64pins or flat package 64pins.

< General description >

RP5S1016 is high speed low power consumption 16 x 16 parallel multiplier. X and Y input registers are independently controlled positive edge trigger D type flip-flop respectively. Each input data can be used for either complement of 2 or absolute value display. Since the product register has 3-state output and input and input register can also be controlled independently, it enables to connect RP5S1016 with external bus easily.

By adding 1 to MSB of RP5S1016, RND control, which rounds the product, is incorporated to MSP. To control FA, shift MSP by 1bit, then, repeat sign bit on MSB of LSP, to change data format for the output of complement of 2. FA control must be used only for calculation of complement of 2. FT control makes output latch transparent.

RP5S1016 makes high speed operation possible by using modified Booth algorithm, carry save adapter, CLA (carry foresight circuit), etc.

RP5S1016

No	Pin name	No	Pin name	No	Pin name	No	Pin name
1	X4	17	P8, Y8	33	P8, Y24	49	Vcc
2	X3	18	P9, Y9	34	P9, Y25	50	TCY
3	X2	19	P10, Y10	35	P10, Y26	51	TCX
4	X1	20	P11, Y11	36	P11, Y27	52	RND
5	X0	21	P12, Y12	37	P12, Y28	53	CLKX
6	$\overline{OEL}$	22	P13, Y13	38	P13, Y29	54	X15
7	CLKL	23	P14, Y14	39	P14, Y30	55	X14
8	CLKY	24	P15, Y15	40	P15, Y31	56	X13
9	P0, Y0	25	P0, Y16	41	CLKM	57	X12
10	P1, Y1	26	P1, Y17	42	$\overline{OEP}$	58	X11
11	P2, Y2	27	P2, Y18	43	FA	59	X10
12	P3, Y3	28	P3, Y19	44	FT	60	X9
13	P4, Y4	29	P4, Y20	45	HSPSEL	61	X8
14	P5, Y5	30	P5, Y21	46	GND	62	X7
15	P6, Y6	31	P6, Y22	47	GND	63	X6
16	P7, Y7	32	P7, Y23	48	Vcc	64	X5

2. RP5S1010 (16bits x 16bits + expandable by 3bits multiplier/accumulator)

< Features >

- 16 x 16bits parallel multiplication/cumulative addition
- Multiplication/Cumulative addition time 65nS
- Data format displaying complement of 2 or absolute value
- Single 5V power supply
- Suppliable with shrink DIP 64pins or flat package 64pins

< General description >

RP5S1010 is TTL compatible high speed low power consumption 16 x 16bits multiplier/accumulator.

Low power consumption has been achieved by CMOS, and high speed operation has been achieved by modified Booth algorithm, carry save adapter, CLA (carry foresight circuit), etc.

RP5S1010 has 16bits input bus of 2 systems, 16bits MSP product bus of 1 system and 3bits expandable bus.

Input register is the same D type positive edge trigger fli-flop as the product register. Since the product register has 3-state function and input/output clock can also be controlled independently, it enables to connect direct with 16bits external bus. RP5S1010 has RND control and by adding 1 to MSB of LSP of the multiplier, product can be rounded to MSP. By using preload control together with 3-state control, it initializes the content of output register. RP5S1010 executes multiplication and addition, multiplication and subtraction and only multiplication depending upon the control condition of ACC and SUB. It performs switching between complement of 2 and absolute value display with TC control.

RP5S1010

No	Pin name	No	Pin name	No	Pin name	No	Pin name
1	X6	17	P8, Y8	33	P24	49	Vcc
2	X5	18	P9, Y9	34	P25	50	CLKY
3	X4	19	P10, Y10	35	P26	51	CLKX
4	X3	20	P11, Y11	36	P27	52	ACC
5	X2	21	P12, Y12	37	P28	53	SUB
6	X1	22	P13, Y13	38	P29	54	RND
7	X0	23	P14, Y14	39	P30	55	TSL
8	P0, Y0	24	P15, Y15	40	P31	56	X15
9	P1, Y1	25	P16	41	P32	57	X14
10	P2, Y2	26	P17	42	P33	58	X13
11	P3, Y3	27	P18	43	P34	59	X12
12	P4, Y4	28	P19	44	CLKP	60	X11
13	P5, Y5	29	P20	45	TSM	61	X10
14	P6, Y6	30	P21	46	PREL	62	X9
15	P7, Y7	31	P22	47	TSX	63	X8
16	GND	32	P23	48	TC	64	X7

3. RP5S3910 (16bits micro-program sequencer)

< Features >

- Since address width is 16bits, it enables to use micro-cord up to 64K words.
- 16bits down counter for loop statement and repeat statement is built-in.
- The address of micro-program can be selected among 4 including micro-program counter, branch address bus, 8 level μPC side stack and internal retention register.
- Output bus is 3-state output.
- Clock cycle 50nS

< General description >

RP5S3910 is the address sequencer which controls the execution sequence of micro-instruction stored in the micro-program memory. In addition to the successive sequence, it enables to perform the conditional branch under optional address in 64K microwords. The stack of last-in first-out makes return of micro sub-routine and nesting loop possible. It allows micro sub-routine up to 8 levels and nesting of loop up to 6 levels. The loop of micro-instruction is countable up to 65536 times.

With individual micro-instruction, micro-program sequencer can select 16bits address from the following 4 sources.

As source, there are ① micro-program address register (μPC) retaining 1 additionally incremented value from the current address, ② Direct input (D) from external bus, ③ register counter (R/C) which retains load data that have been prepared beforehand and ④ 8 levels last-in first-out stack (F).

RP5S3910

No	Pin name	No	Pin name	No	Pin name	No	Pin name
1	$\overline{RLD}$	17	$\overline{FULL2}$	33	Y0	49	D0
2	$\overline{FULL1}$	18	Y15	34	CI	50	D1
3	$\overline{SCP}$	19	Y14	35	SDIN	51	D2
4	SCPCP	20	Y13	36	CP	52	D3
5	SDOUT	21	Y12	37	–	53	D4
6	$\overline{PL}$	22	Y11	38	–	54	D5
7	$\overline{MAP}$	23	Y10	39	–	55	D6
8	$\overline{VECT}$	24	Y9	40	–	56	D7
9	$\overline{CCEN}$	25	Y8	41	–	57	D8
10	$\overline{CC}$	26	Y7	42	–	58	D9
11	I4	27	Y6	43	–	59	D10
12	I3	28	Y5	44	–	60	D11
13	I2	29	Y4	45	–	61	D12
14	I1	30	Y3	46	$\overline{OE}$	62	D13
15	I0	31	Y2	47	GND	63	D14
16	$\overline{CE}$	32	Y1	48	Vcc	64	D15

4. RP5S3030 (16bits barrel shifter)

< Features >

- Data width 16bits
- Shift can be set at option from 0 to 16 in unit of 1bit.
- High speed operation 30nS

< General description >

RP5S3030 is the barrel shifter which shifts the data with optional number of bits in the optional direction. Data width is 16bits, and the number of shift can be set at option from 0 to 16 in unit of 1bit.

Input is 32bits, and output is 16bits. When setting the input data to the rightend of barrel shifter, rightward shift can be set from 0 to 16 at option. When setting the input data to the leftend, leftward shift can be set from 0 to 16 at option. When setting the input data at the center, it sets each 8bits leftward and rightward at option.

RP5S3030

No	Pin name	No	Pin name	No	Pin name	No	Pin name
1	I 15	17	Y 0	33	S 4	49	I 31
2	I 14	18	Y 1	34	S 3	50	I 30
3	I 13	19	Y 2	35	S 2	51	I 29
4	I 12	20	Y 3	36	S 1	52	I 28
5	I 11	21	Y 4	37	S 0	53	I 27
6	I 10	22	Y 5	38	–	54	I 26
7	I 9	23	Y 6	39	–	55	I 25
8	I 8	24	Y 7	40	–	56	I 24
9	I 7	25	Y 8	41	–	57	I 23
10	I 6	26	Y 9	42	–	58	I 22
11	I 5	27	Y 10	43	–	59	I 21
12	I 4	28	Y 11	44	–	60	I 20
13	I 3	29	Y 12	45	–	61	I 19
14	I 2	30	Y 13	46	–	62	I 18
15	I 1	31	Y 14	47	GND	63	I 17
16	I 0	32	Y 15	48	Vcc	64	I 16

5. RP5S3010 (16bits arithmetic logic operation)

< Features >

- Data are 16bits width
- High speed operation 45nS

< General description >

RP5S3010 is the high speed low power consumption arithmetic logic unit developed under CMOS technology of 16bits data width with 8 functions. High speed has been achieved by using CLA (carry foresight circuit) in the inside.

RP5S3010 has 3 kinds of arithmetic logic functions and 5 kinds of logic operation functions. Since it has carry propagation signal ($\overline{P}$) and carry generation signal ($\overline{G}$), hierarchical structure of CLA can be fabricated by connecting it with external CLA chips.

RP5S3010

No	Pin name	No	Pin name	No	Pin name	No	Pin name
1	S 7	17	C I N	33	F 12	49	S 15
2	R 7	18	I 2	34	F 13	50	R 15
3	S 6	19	I 1	35	F 14	51	S 14
4	R 6	20	I 0	36	F 15	52	R 14
5	S 5	21	F 0	37	–	53	S 13
6	R 5	22	F 1	38	–	54	R 13
7	S 4	23	F 2	39	–	55	S 12
8	R 4	24	F 3	40	–	56	R 12
9	S 3	25	F 4	41	–	57	S 11
10	R 3	26	F 5	42	$\overline{P}$	58	R 11
11	S 2	27	F 6	43	$\overline{G}$	59	S 10
12	R 2	28	F 7	44	C O U T	60	R 10
13	S 1	29	F 8	45	O V R	61	S 9
14	R 1	30	F 9	46	Z E R O	62	R 9
15	S 0	31	F 10	47	G N D	63	S 8
16	R 0	32	F 11	48	V c c	64	R 8

6. RP5S3020 (32words x 16bits 2ports register file)

< Features >

- Memory capacity of 32words 16bits
- 2ports configuration of write input 1 and read output 2
- High speed access 45nS
- Low power consumption

< General description >

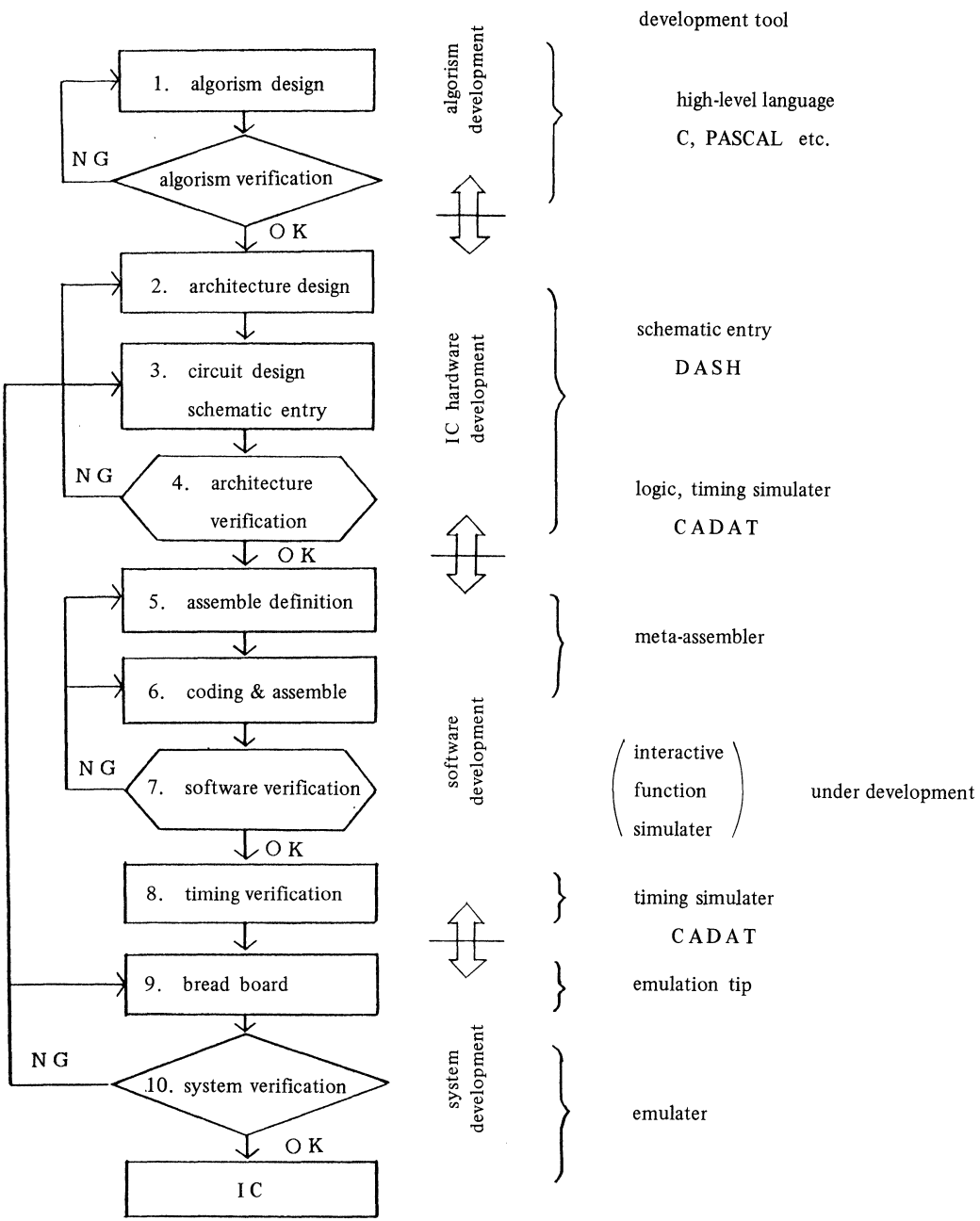
RP5S3020 is the register file configulated with 32words 16bits 2ports. Low power consumption operation is possible under CMOS technology. It has 1 write port and 2 read ports. Since 2 read ports have 3-state output independently, they allow connection with different external bus.

The write operation of RP5S3020 is such that, when write enable signal ($\overline{WE}$) is "L", the write data (D) in the write port is written in word line specified by address control input A. The read operation is such that, when latch enable (LE) of the data of word line specified by address control inputs A and B is "H", each is output from each port A and B. Read port A and B are 3-state output respectively and controlled by 3-state control signal $\overline{OEA}$ and $\overline{OEB}$.

RP5S3020

No	Pin name	No	Pin name	No	Pin name	No	Pin name
1	A 0	17	Y B 3	33	Y B 11	49	D 0
2	A 1	18	Y A 4	34	Y A 12	50	D 1
3	A 2	19	Y B 4	35	Y B 12	51	D 2
4	A 3	20	Y A 5	36	Y A 13	52	D 3
5	A 4	21	Y B 5	37	Y B 13	53	D 4
6	L E	22	Y A 6	38	Y A 14	54	D 5
7	$\overline{WE}$	23	Y B 6	39	Y B 14	55	D 6
8	$\overline{OEA}$	24	Y A 7	40	Y A 15	56	D 7
9	$\overline{OEB}$	25	Y B 7	41	Y B 15	57	D 8
10	Y A 0	26	Y A 8	42	B 4	58	D 9
11	Y B 0	27	Y B 8	43	B 3	59	D 10
12	Y A 1	28	Y A 9	44	B 2	60	D 11
13	Y B 1	29	Y B 9	45	B 1	61	D 12
14	Y A 2	30	Y A 10	46	B 0	62	D 13
15	Y B 2	31	Y B 10	47	G N D	63	D 14
16	Y A 3	32	Y A 11	48	V c c	64	D 15

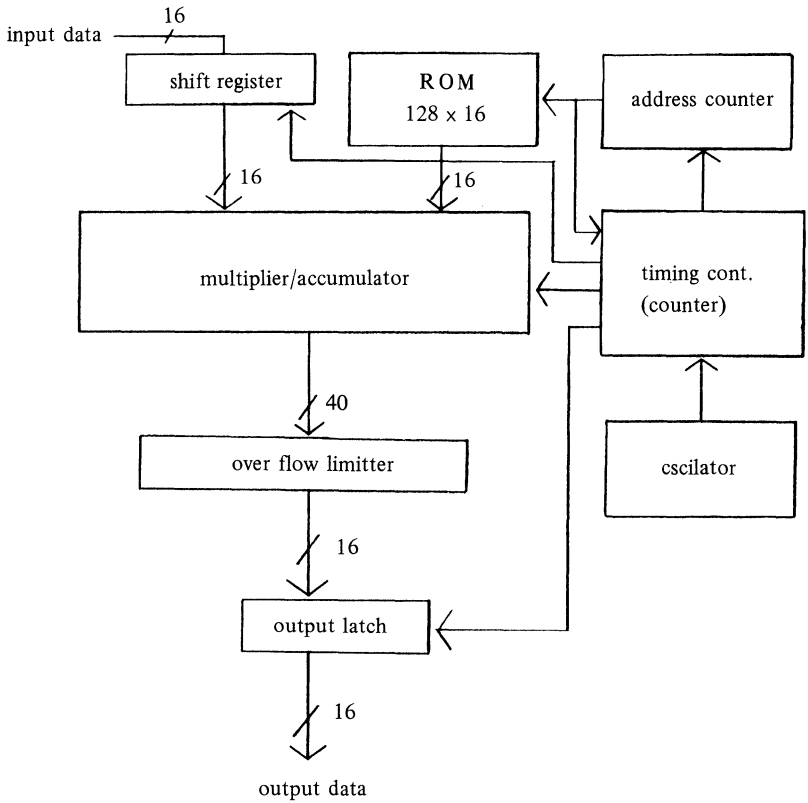
Application Specific DSP development flow chart

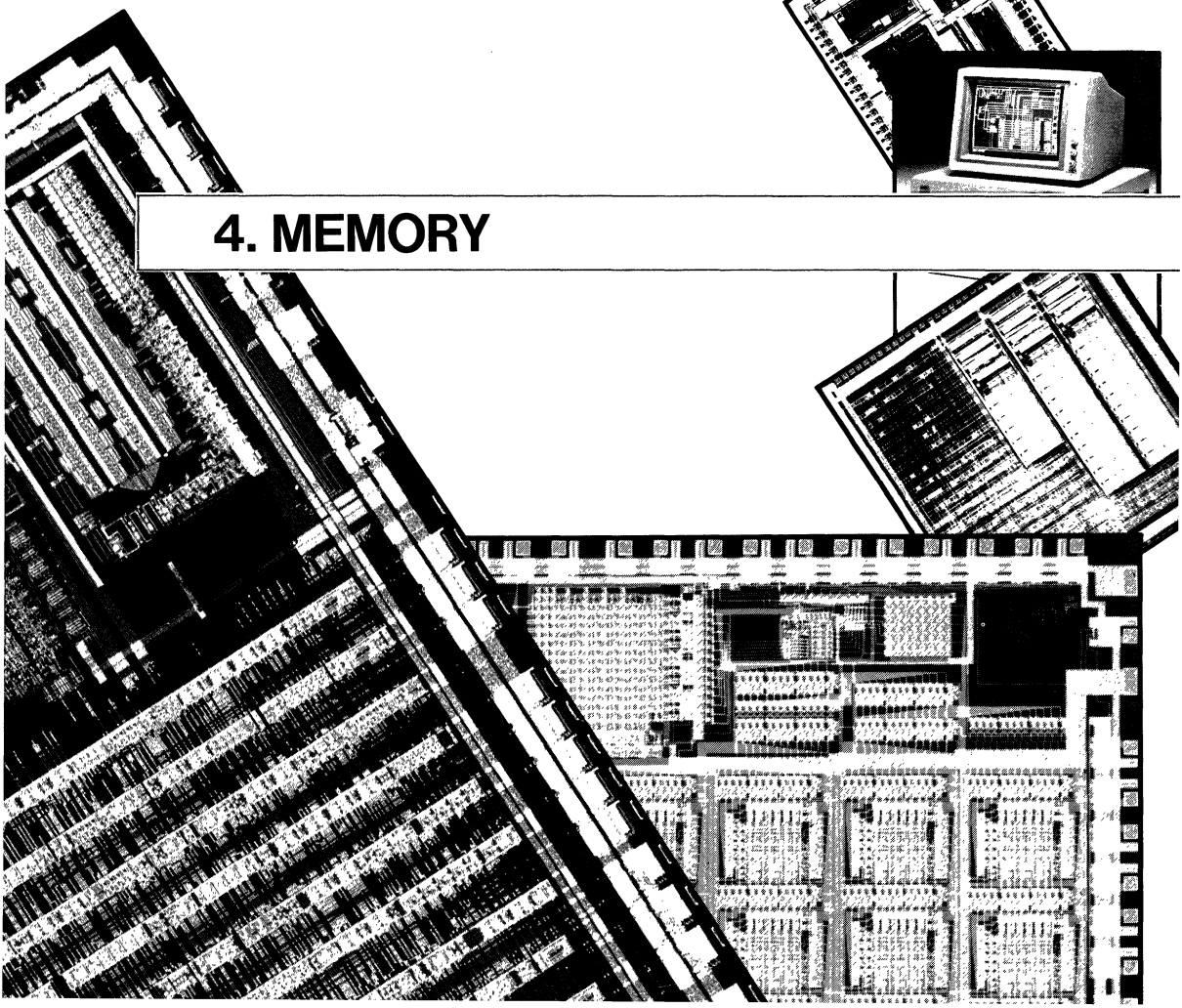


♦ Application Example ♦

This is an example of a digital filter using DSP and RSC−15 series cells.

A sampling frequency of up to 139 KHz can be achieved by constructing a filter of more than 100 degree FIR. (The CD sampling frequency is 44.1 KHz)





4. MEMORY

RICOH

RP2364E

NMOS 64 Kbit MASK ROM
(8,192 word × 8 bit)

■ GENERAL DESCRIPTION

The RP2364E is static NMOS Read Only Memory organized as 8,192 words by 8-bits and operate from a single +5V supply.

The RP2364E features automatic power-down mode. When Chip Enable ($\overline{CE}$) goes HIGH level, the supply current is reduced from 100mA (max.) to 20mA (max.).

The device has Chip Enable ($\overline{CE}$) input and output Enable (OE/$\overline{OE}$) inputs allowing up to 32 wired ORs to be tied without external decoding.

According to your order, logic of the following pins may be selected ACTIVE LOW or ACTIVE HIGH or NC.

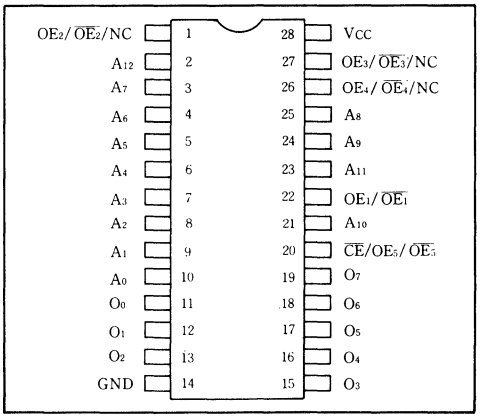
Pins 1, 22, 26 and 27.

and Pin 20 may be selected as $\overline{CE}$ or $\overline{OE}$.

■ FEATURES

- 8,192 words×8 bits organization
- Low power dissipation: Active 550mW max.
  Standby 110mW max.
- Fast access time: 200ns max.
- Single +5V(±10%) power supply
- Completely TTL compatible: All outputs and inputs

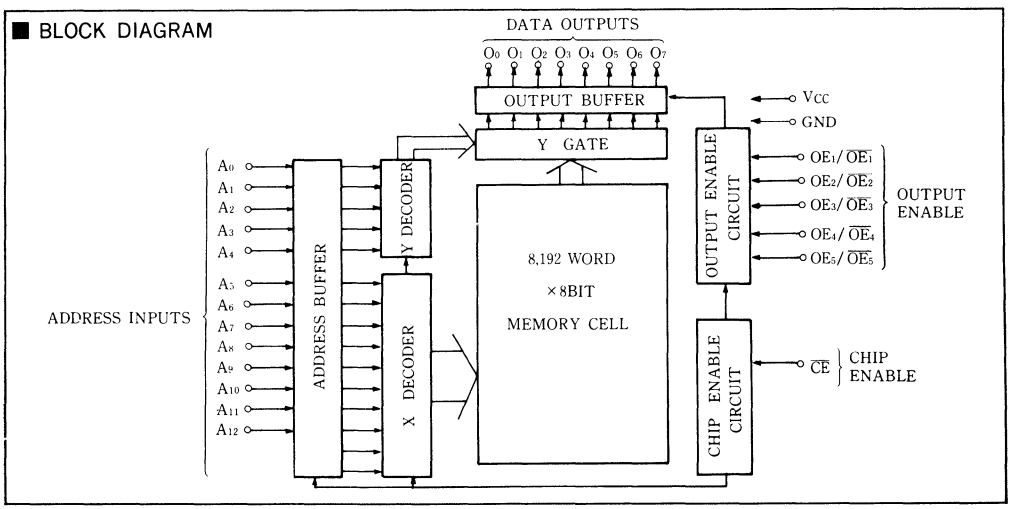
■ PIN CONFIGURATION (Top view)



■ PIN DESCRIPTION

PIN NAME	FUNCTION
A0 ~ A12	Address Input
O0 ~ O7	Data Output
$\overline{OE}_1$ ~ $\overline{OE}_5$	Output Enable
$\overline{CE}$	Chip Enable
NC	No Connection
Vcc	Power Supply
GND	GND

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.5~7	V
V_I	Input Voltage		−0.5~7	V
V_O	Output Voltage		−0.5~7	V
Pd	Maximum Power Dissipation	Ta=25℃	700	mW
Topr	Operating Ambient Temperature		0~70	℃
Tstg	Storage Temperature		−40~125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=0~70℃)

Symbol	Parameter	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.5		0.8	V

■ ELECTRICAL CHARACTERISTICS

●DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{CC}$			20	mA
I_{CC2}	Supply Current (Active)	I_O=0mA			100	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=3.2mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
I_{LI}	Input Leakage Current	V_I=0V~V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current	V_O=0V~V_{CC} Chip Deselected	−10		10	μA

●AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Valve			Unit
			Min	Typ	Max	
t_{RC}	Read Cycle Time	Output Load= 1TTL+100pF	200			ns
t_{ACC}	Address Access Time				200	ns
t_{CE}	Chip Enable Access Time				200	ns
t_{OE}	Output Enable Access Time				80	ns
t_{DF}	Output Hold Time after Output Enable Change				80	ns
t_{OH}	Output Hold Time after Address Change		0			ns
t_{CH}	Output Hold Time after Chip Enable Change				80	ns

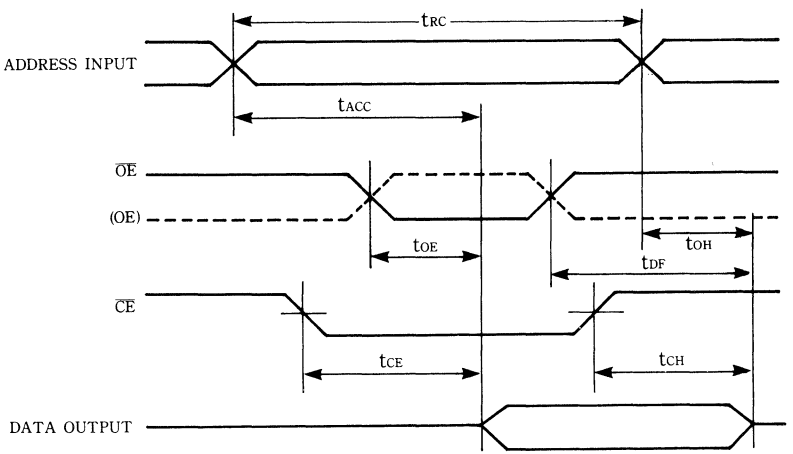
Notes : 1. Input Pulse Levels : V_{IL}=0.6V, V_{IH}=2.2V

2. Output Timing Reference Level : V_{OL}=0.8V, V_{OH}=2.0V

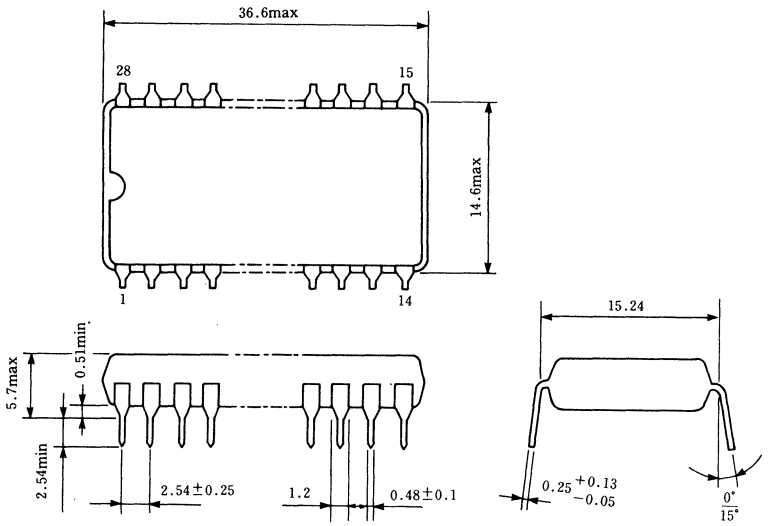
● TERMINAL CAPACITANCE

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
Ci	Input Capacitance	f = 1MHz			8	pF
Co	Output Capacitance				12	pF

■ TIMING CHART



■ 28 PIN PLASTIC PACKAGE (Unit: mm)



NMOS 128kbit MASK ROM

(16,384word×8bit)

RP23128E

■ GENERAL DESCRIPTION

The RP23128E is static NMOS Read Only Memory organized as 16,384 words by 8-bits and operate from a single + 5V supply.

The RP23128E features automatic power-down mode. When Chip Enable ($\overline{CE}$) goes HIGH level, the supply current is reduced from 100mA (max.) to 20mA (max.).

These devices have Chip Enable ($\overline{CE}$) input and output Enable (OE/$\overline{OE}$) inputs allowing up to 16 wired ORs to be tied without external decoding.

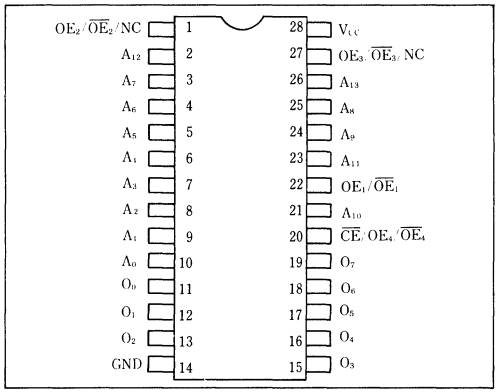
According to your order, logic of the following pins may be selected.

Pin 22 (active low/active high)
Pin 1, 27 (active low/active high/No Connection)
Pin 20 (Chip Enable/active low/active high)

■ FEATURES

- 16,384 words × 8 bits organization
- Low power dissipation: Active 550mW max.
  Standby 110mW max.
- Fast access time: 200ns max.
- Single + 5V (±10%) power supply
- Completely TTL compatible: All outputs and inputs

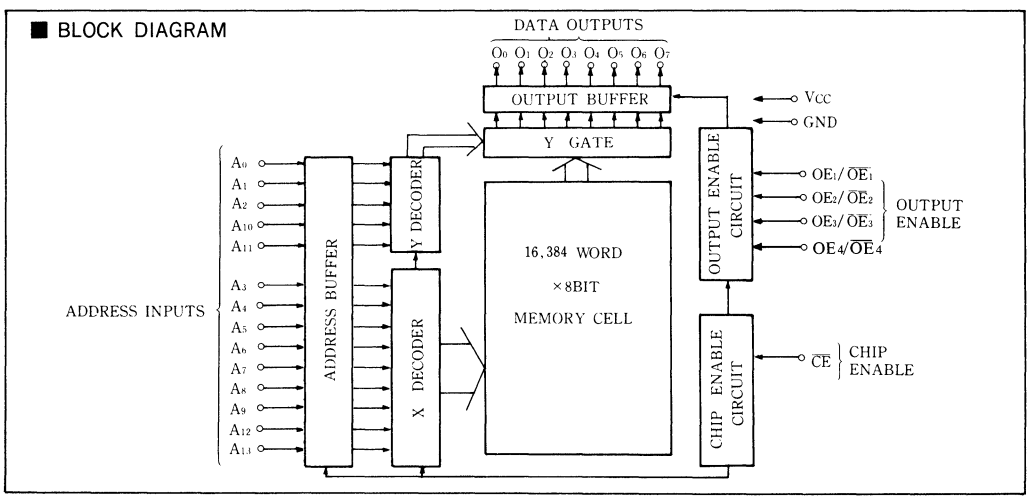
■ PIN CONFIGURATION (Top view)



■ PIN DESCRIPTION

PIN NAME	FUNCTION
$A_0 \sim A_{13}$	Address Input
$O_0 \sim O_7$	Data Output
$\overline{OE}_1 \sim \overline{OE}_4$	Output Enable
$\overline{CE}$	Chip Enable
NC	No Connection
Vcc	Power Supply
GND	GND

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.3～7	V
V_I	Input Voltage		−0.3～Vcc+0.3	V
V_O	Output Voltage		−0.3～Vcc+0.3	V
Pd	Maximum Power Dissipation	Ta=25℃	700	mW
Topr	Operating Ambient Temperature		0～70	℃
Tstg	Storage Temperature		−40～125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃)

Symbol	Parameter	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{CC}$			20	mA
I_{CC2}	Supply Current (Active)	I_O=0mA			100	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=2.0mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		−0.3		0.8	V
I_{LI}	Input Leakage Current	V_I=0V～V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current	V_O=0V～V_{CC} Chip Deselected	−10		10	μA

● AC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

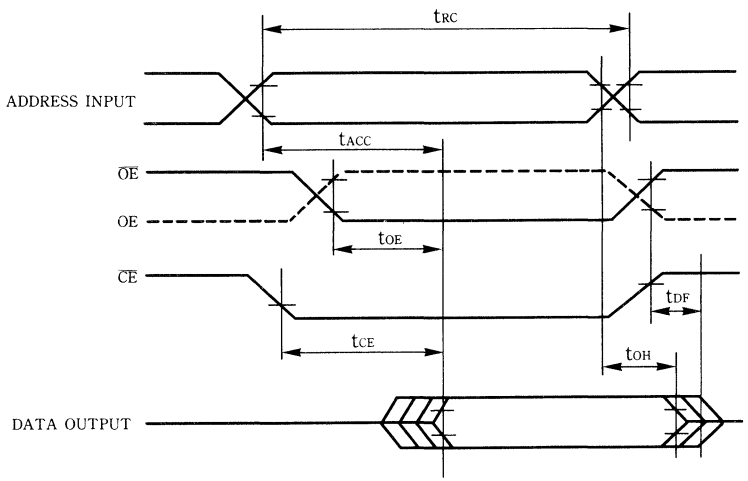
Symbol	Parameter	Specified Valve			Unit
		Min	Typ	Max	
t_{RC}	Read Cycle Time	200			ns
t_{ACC}	Address Access Time			200	ns
t_{CE}	Chip Enable Access Time			200	ns
t_{OE}	Output Enable Access Time			80	ns
t_{DF}	Output Floating Delay Time			80	ns
t_{OH}	Output Hold Time	0			ns

Note) Test Condition
Input Pulse Voltage: V_{IL}=0.6V, V_{IH}=2.4V
Input Pulse Rise/Fall Time: 10ns
Timing Measuring Voltage:
Input V_{IL}=0.8V, V_{IH}=2.2V
Output V_{OL}=0.8V, V_{OH}=2.0V
Output Load: 1TTL + 100pF
(including jig capacitance)

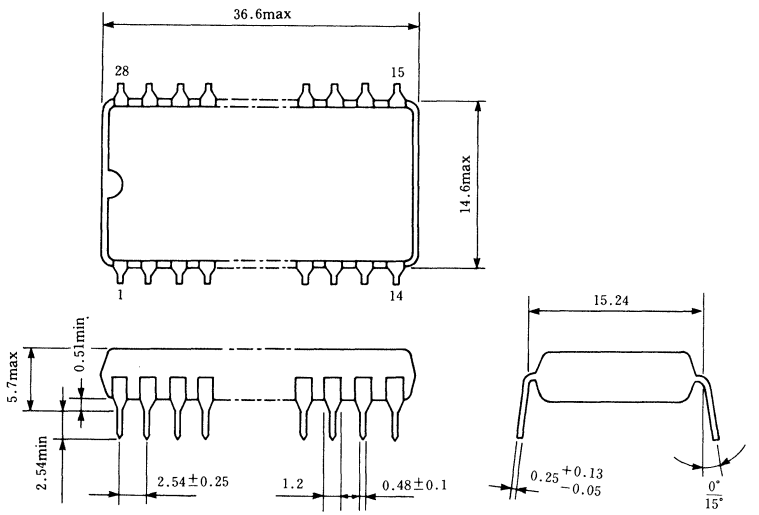
● TERMINAL CAPACITANCE

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
Ci	Input Capacitance	f = 1MHz			8	pF
Co	Output Capacitance				12	pF

■ TIMING CHART



■ 28 PIN PLASTIC PACKAGE (Unit: mm)



NMOS 256 Kbit MASK ROM
(32,768 word × 8 bit)

RP23256D/E, RP23257D/E

■ GENERAL DESCRIPTION

The RP23256D/E and RP23257D/E are static NMOS Read Only Memories organized as 32,768 words by 8-bits and operate from a single +5V supply.

The RP23256D/E and RP23257D/E features automatic power-down mode. When Chip Enable ($\overline{CE}$) goes HIGH level, the supply current is reduced from 100mA (max.) to 20mA (max.).

These devices have Chip Enable ($\overline{CE}$) input and two output Enable (OE/$\overline{OE}$) inputs allowing up to eight wired ORs to be tied without external decoding.

According to your order, logic of the following pins may be selected ACTIVE LOW or ACTIVE HIGH.

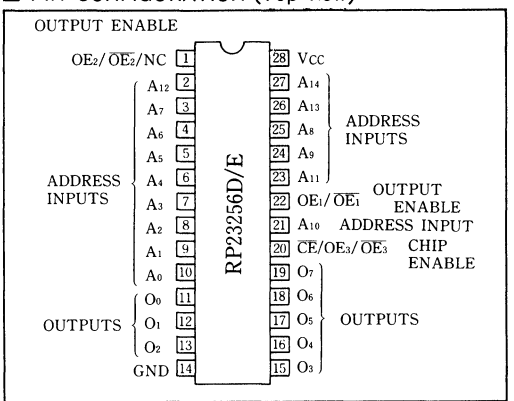
Pins 1, and 22 for RP23256D/E
Pins 1, and 26 for RP23257D/E

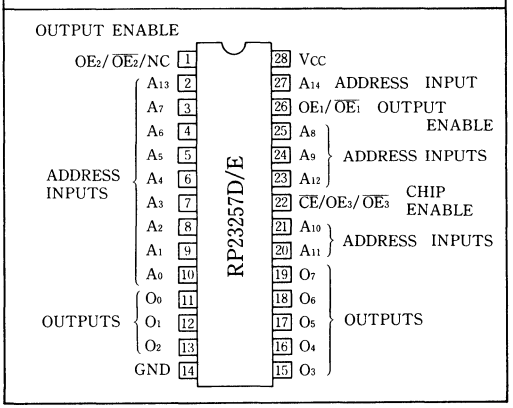
and OE_2 may be changed to NC (No Connection), $\overline{CE}$ may be selected to OE_3.

■ FEATURES

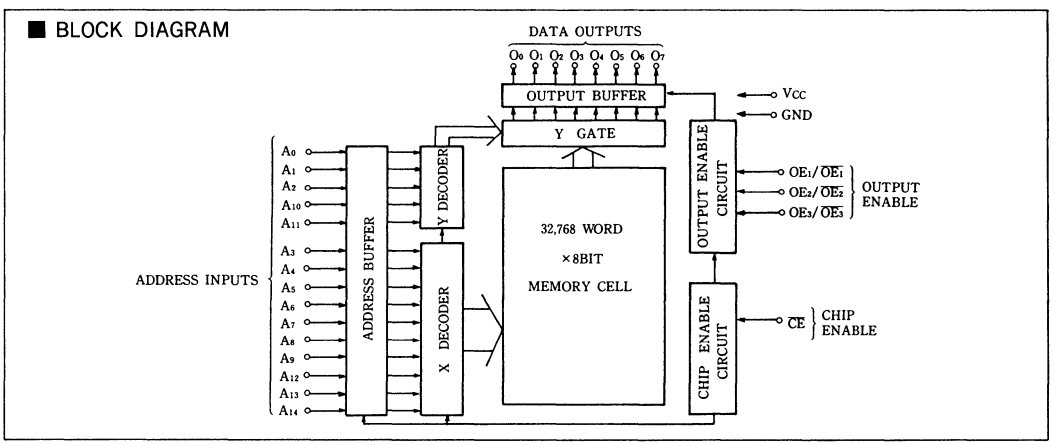
- 32,768 words×8 bits organization
- Low power dissipation: Active 550mW max.
  Standby 110mW max.
- Fast access time: RP23256D/257D 250ns max.
  RP23256E/257E 200ns max.
- Single +5V(±10%) power supply
- Completely TTL compatible: All outputs and inputs
- 3-state outputs for wired-OR expansion
- Pin compatible with: Intel 27256 EPROM (RP23256D/E)
  TI 2564 EPROM (RP23257D/E)

■ PIN CONFIGURATION (Top view)





■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.5～7	V
V_I	Input Voltage		−0.5～7	V
V_O	Output Voltage		−0.5～7	V
Pd	Maximum Power Dissipation	Ta=25℃	700	mW
Topr	Operating Ambient Temperature		0～70	℃
Tstg	Storage Temperature		−40～125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃)

Symbol	Parameter	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.5		0.8	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{CC}$			20	mA
I_{CC2}	Supply Current (Active)	I_O=0mA			100	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=3.2mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
I_{LI}	Input Leakage Current	V_I=0V～V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current	V_O=0V～V_{CC} Chip Deselected	−10		10	μA

● AC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

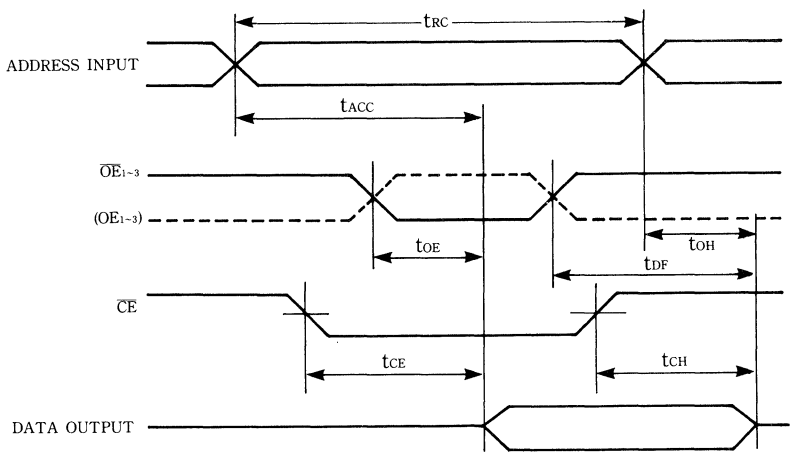
Symbol	Parameter	Test Condition	RP23256D/257D			RP23256E/257E			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	Output Load= 1TTL+100pF	250			200			ns
t_{ACC}	Address Access Time				250			200	ns
t_{CE}	Chip Enable Access Time				250			200	ns
t_{OE}	Output Enable Access Time				100			80	ns
t_{DF}	Output Hold Time after Output Enable Change				100			80	ns
t_{OH}	Output Hold Time after Address Change		0			0			ns
t_{CH}	Output Hold Time after Chip Enable Change				100			80	ns

Notes : 1. Input Pulse Levels : V_{IL}=0.6V, V_{IH}=2.2V
2. Output Timing Reference Level : V_{OL}=0.8V, V_{OH}=2.0V

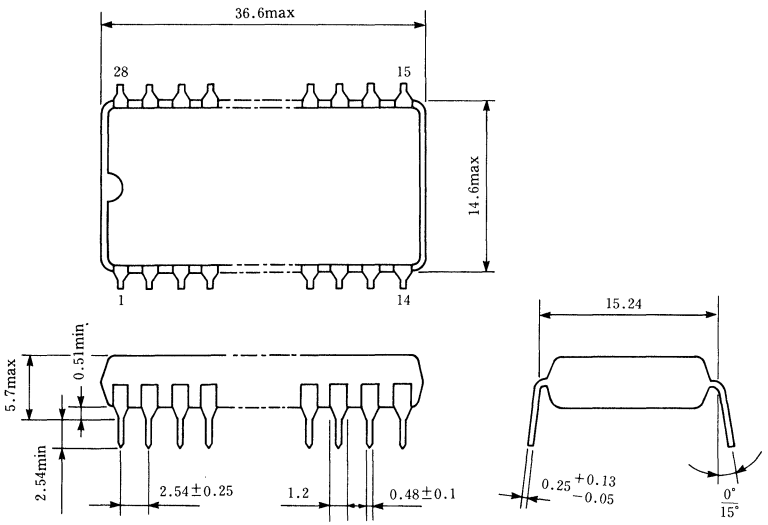
● TERMINAL CAPACITANCE

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
Ci	Input Capacitance	f=1MHz			8	pF
Co	Output Capacitance				12	pF

■ TIMING CHART



■ 28 PIN PLASTIC PACKAGE (Unit: mm)



RP231026D/E

NMOS 1Mbit MASK ROM
(131,073 word × 8 bit)

■ GENERAL DESCRIPTION

The RP231026D/E is a static NMOS read only Memory organized as 131,072 words by 8 bits and operates from a single+5V supply.

The RP231026D/E features automatic power-down mode. When Chip Enable ($\overline{CE}$) goes HIGH level, the supply current is reduced from 100mA (max.) to 30mA (max.).

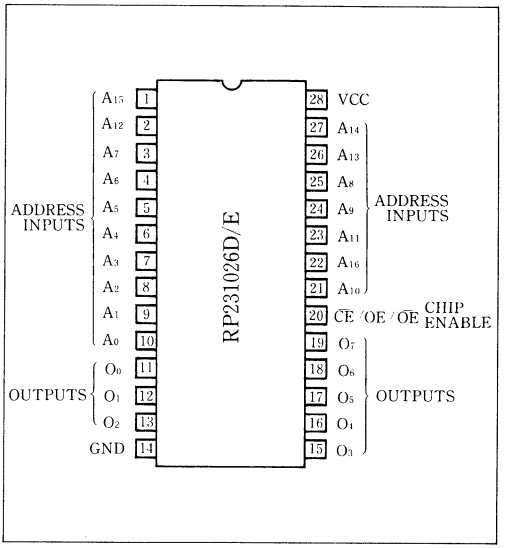
Pin 20 can be used as OE.

According to your order, Logic of the OE pin may be selected ACTIVE LOW or ACTIVE HIGH.

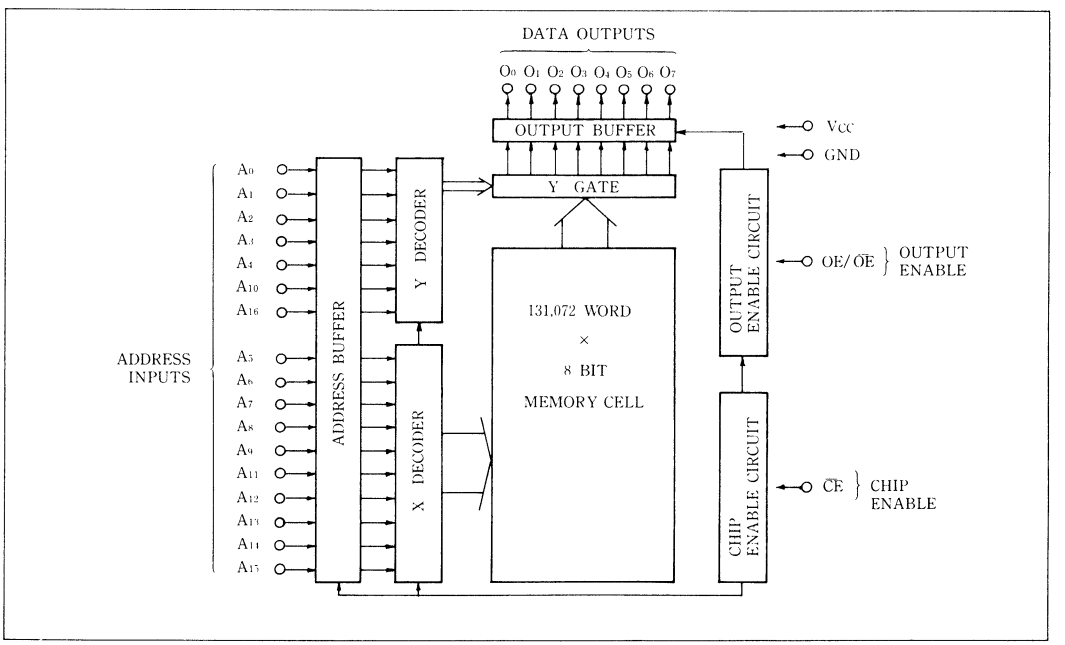
■ FEATURES

- 131,072 words×8 bits organization
- Low power dissipation Active 550mW max.
  Standby 165mW max.
- Fast access time RP231026D 250ns max.
  RP231026E 200ns max.
- Single +5V (±10%) power supply
- Completely TTL compatible: All outputs and inputs
- 3-state outputs for wired-OR expansion
- Pin compatible with Intel 27512

■ PIN CONFIGURATION (Top view)



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.3～7	V
V_I	Input Voltage		−0.3～Vcc+0.3	V
V_O	Output Voltage		−0.3～Vcc+0.3	V
Pd	Maximum Power Dissipation	Ta=25℃	700	mW
Topr	Operating Ambient Temperature		0～70	℃
Tstg	Storage Temperature		−40～125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃)

Symbol	Parameter	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V

■ ELECTRICAL CHARACTERISTICS

●DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{CC}$			30	mA
I_{CC2}	Supply Current (Active)	I_O=0mA			100	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4		V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL}=2.0mA			0.4	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage		−0.3		0.8	V
I_{LI}	Input Leakage Current	V_I=0V～V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current	$V_O=V_{CC}$, Chip Deselected	−10		10	μA

●AC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

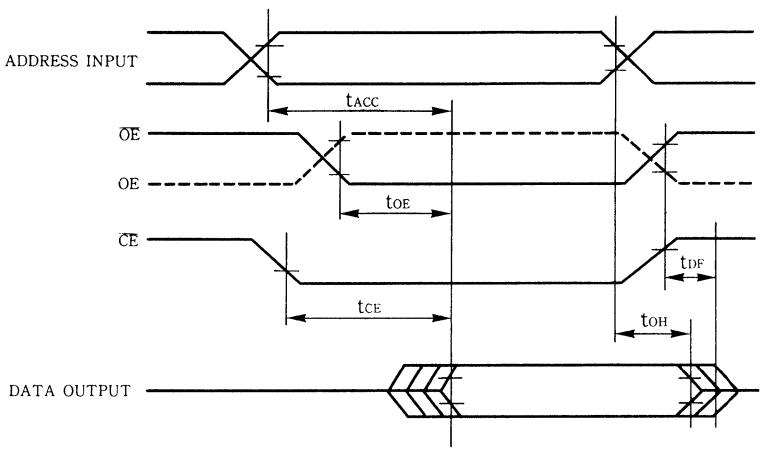
Symbol	Parameter	Specified Value						Unit
		RP231026D			RP231026E			
		Min	Typ	Max	Min	Typ	Max	
t_{ACC}	Address Access Time			250			200	ns
t_{CE}	Chip Enable Access Time			250			200	ns
t_{OE}	Output Enable Access Time			100			80	ns
t_{DF}	Output Floating Delay Time	0		100	0		80	ns
t_{OH}	Output Hold Time	0			0			ns

Note) Test Condition
Input Pulse Voltage: V_{IL}=0.6V, V_{IH}=2.4V
Input Pulse Rise/Fall Time: 10ns
Timing Measuring Voltage: Input V_{IL}=0.8V, V_{IH}=2.2V
Output V_{OL}=0.8V, V_{OH}=2.0V
Output Load: 1TTL + 100pF (including jig capacitance)

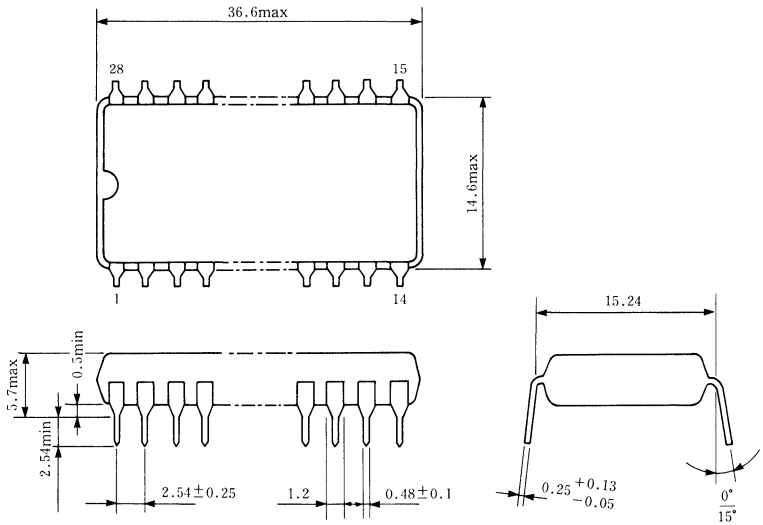
● TERMINAL CAPACITANCE

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
Ci	Input Capacitance	f=1MHz			8	pF
Co	Output Capacitance				12	pF

■ TIMING CHART



■ 28 PIN PLASTIC PACKAGE (Unit:mm)



RICOH

RP23C4000

CMOS 4M bit MASK ROM

(524,288 word × 8 bit / 262,144 word × 16 bit)

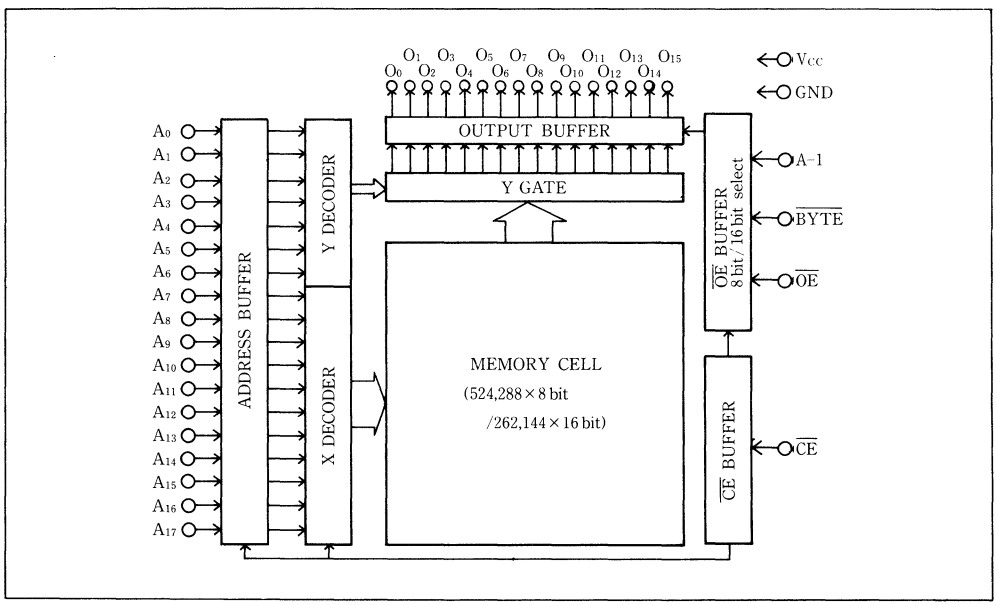
■ OUTLINE

The RP23C4000 is a static CMOS read only Memory organized as 524,288 words by 8 bits or 262,144 words by 16 bits and operates from a single +5V supply. The bit organization can be selected electrically. The RP23C4000 has 3-state output and TTL compatible Output/Input, and can be connected to CPU busline directly.

■ FEATURES

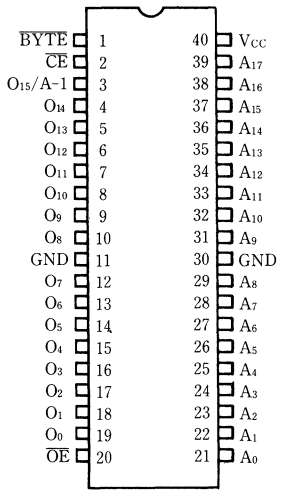
- 524,288 words × 8 bits (8 bit mode)/262,144 words × 16 bits (16 bit mode) organization (electrically selected)
- Low power dissipation — Active 220 mW max. / Standby 550 μW max.
- Fast access time 200 ns max.
- Single +5V (±10%) power supply
- Completely TTL compatible : All outputs and inputs
- 3-state outputs
- Package : 40 pin DIP

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

(TOP View)



■ PIN DESCRIPTION

PIN NAME	FUNCTION
$\overline{BYTE}$	8 bit/16 bit mode select input
$\overline{CE}$	Chip enable input
O_{15} /A−1	(16 bit mode) data output/ (8 bit mode) LSB address
$O_0 \sim O_{14}$	Data output
$A_0 \sim A_{17}$	Address input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	GND

■ TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A − 1 (O_{15})	Standby/ Active	$O_0 \sim O_7$	$O_8 \sim O_{15}$	mode	LSB	MSB
H	X	X	X	Standby	Hi−Z	Hi−Z	output	–	–
L	H	X	X	Active	Hi−Z	Hi−Z	Hi−Z		
L	L	H	input inhibition		$O_0 \sim O_7$	$O_8 \sim O_{15}$	16 bit	A_0	A_{17}
L	L	L	L		$O_0 \sim O_7$	Hi−Z	8 bit	A−1	A_{17}
L	L	L	H		$O_8 \sim O_{15}$	Hi−Z			

L : Low level
H : High level
X : No effect

Hi−Z : High impedance output

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Limit	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.3～7	V
V_I	Input Voltage		−0.3～Vcc+0.3	V
V_O	Output Voltage		−0.3～Vcc+0.3	V
Topr	Operating Ambient Temperature		0～70	℃
Tstg	Storage Temperature		−40～125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃)

Symbol	Parameter	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

Symbol	Parameter	Test Condition	Specified Value			Unit
			Min	Typ	Max	
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{CC}$			100	μA
I_{CC2}	Supply Current (Active)	I_O=0mA			40	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=2.0mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		−0.3		0.8	V
I_{LI}	Input Leakage Current	V_I=0V～V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current	V_O=0V～V_{CC} Chip Deselected	−10		10	μA

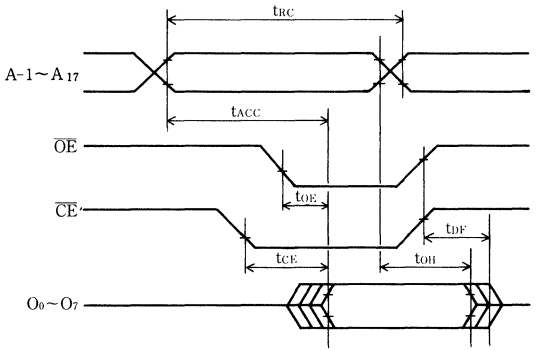
● AC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, V_{CC}=5V±10%)

Symbol	Parameter	Specified Valve			Unit
		Min	Typ	Max	
t_{RC}	Read Cycle Time	200			ns
t_{ACC}	Address Access Time			200	ns
t_{CE}	Chip Enable Access Time			200	ns
t_{OE}	Output Enable Access Time			80	ns
t_{DF}	Output Floating Delay Time	0		80	ns
t_{OH}	Output Hold Time	0			ns
t_{BYT}	Byte Access Time			200	ns

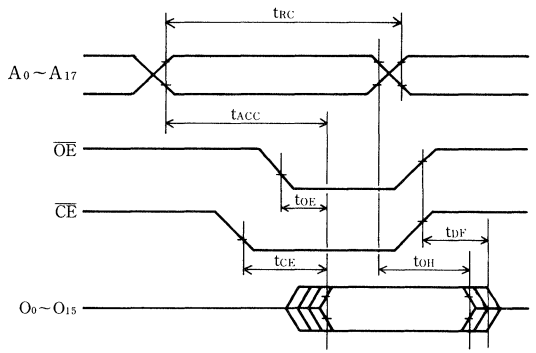
Note) Test Condition
Input Pulse Voltage: V_{IL}=0.6V, V_{IH}=2.4V
Input Pulse Rise/Fall Time: 10ns
Timing Measuring Voltage:
Input V_{IL}=0.8V, V_{IH}=2.2V
Output V_{OL}=0.8V, V_{OH}=2.0V
Output Load: 1TTL + 100pF
(including jig capacitance)

■ TIMING CHART

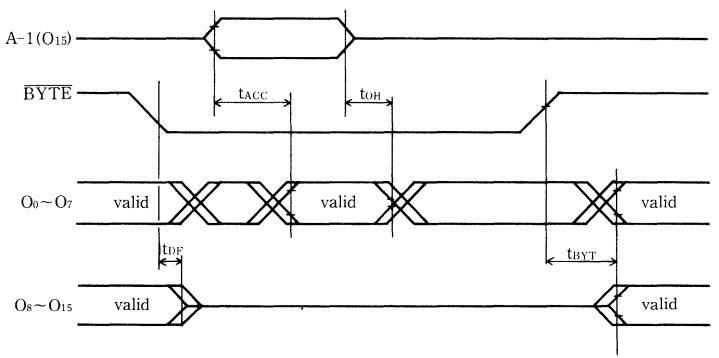
● **8 bit mode** ($\overline{BYTE}$ = V_{IH})



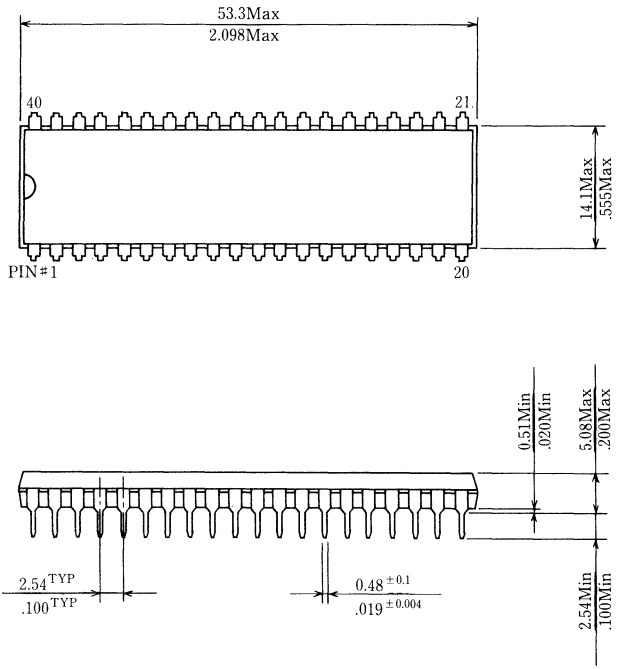
● **16 bit mode** ($\overline{BYTE}$ = V_{IL})



● **8 bit mode/16 bit mode Select** (for A_0~A_{17}, $\overline{CE}$ = "L", $\overline{OE}$ = "L")



■ PACKAGE DIMENSION (mm/inch)



Microelectronic Specification

RF5H01/RP5H01

64-bit CMOS PROM WITH 6/7-bit BINARY COUNTER

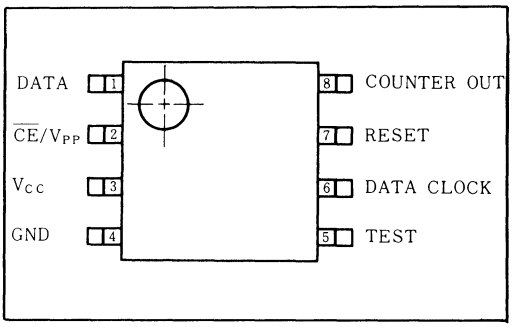
■ GENERAL DESCRIPTION

RF5H01/RP5H01 is a PROM with 64 × 1bit organization (+ dummy 8 bits), employing 2-layer silicon gate CMOS processing technology.

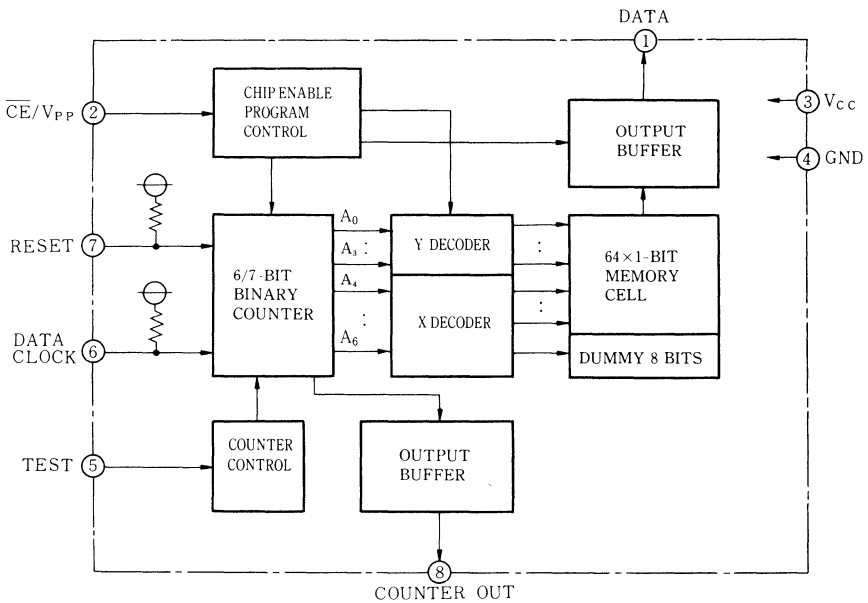
■ FFEATURES

- 64× 1bit organization (+ dummy 8 bits)
- Low power dissipation
  - Active 55mW (max)
  - Standby 550μW (max)
- Access time 1μs (max)
- Single power supply 5V±10%
- Serial outputs
- Inputs and outputs TTL level
- 3-state (Tri-state) outputs

■ PIN CONFIGURATION (Top view)



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Conditions	Limits	Unit
V_{CC}	V_{CC} Supply Voltage	With respect to GND	−0.3～7	V
V_{PP}	V_{PP} Supply Voltage		−0.3～22	V
V_I	Input Voltage		−0.3～7	V
V_O	Output Voltage		−0.3～7	V
P_d	Maximum Power Dissipation	Ta=25℃	0.3	W
T_{opr}	Operating Temperature Range		−20～70	℃
T_{stg}	Storage Temperature		−40～125	℃

■ RECOMMENDED OPERATING CONDITIONS (Ta=−20～70℃)

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	−0.1		0.8	V

■ ELECTRICAL CHARACTERISTICS

● READ OPERATION D.C. CHARACTERISTICS (Ta=−20～70℃, V_{CC}=5V±10%)

Symbol	Parameters		Test Conditions	Limits			Unit
				Min	Typ	Max	
I_{CC1}	Standby V_{CC} Supply Current		$\overline{CE}/V_{PP}=V_{CC}\pm0.3V$ DATA CLOCK,RESET=V_{CC} or Open TEST=GND or $V_{CC}\pm0.3V$			100	μA
I_{CC2}	Operating V_{CC} Supply Current		I_{OUT}=0mA			10	mA
V_{OH}	Output High Voltage		$I_{OH}=-400\mu A$	2.4			V
V_{OL}	Output Low Voltage		I_{OL}=2.1mA			0.45	V
V_{IH}	Input High Voltage	Except TEST		2.0		V_{CC}+0.3	V
		TEST		4.0		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	Except TEST		−0.1		0.8	V
		TEST		−0.1		1.0	V
I_{LI}	Input Leakage Current	RESET,DATA CLOCK	V_I=0V,V_{CC}=5.5V	−180		−20	μA
		TEST,$\overline{CE}/V_{PP}$	V_I=0V～V_{CC}	−10		10	μA
I_{LO}	Output Leakage Current		V_O=0V～V_{CC}	−10		10	μA

● READ OPERATION, A.C. CHARACTERISTICS (Ta=−20～70℃, V_{CC}=5V±10%)

Symbol	Parameters	Test Conditions		Limits			Unit
				Min	Typ	Max	
t_{ACC}	Clock to Output Delay	$\overline{CE}/V_{PP}=V_{IL}$	Load= 1TTL+100pF			1	μs
t_{CE}	$\overline{CE}$ to Output Delay					1	μs
t_{DF}	$\overline{CE}$ High to Output Float			0		200	ns
t_{RW}	Reset pulse width			2			μs
t_{CW}	Clock pulse width			2			μs

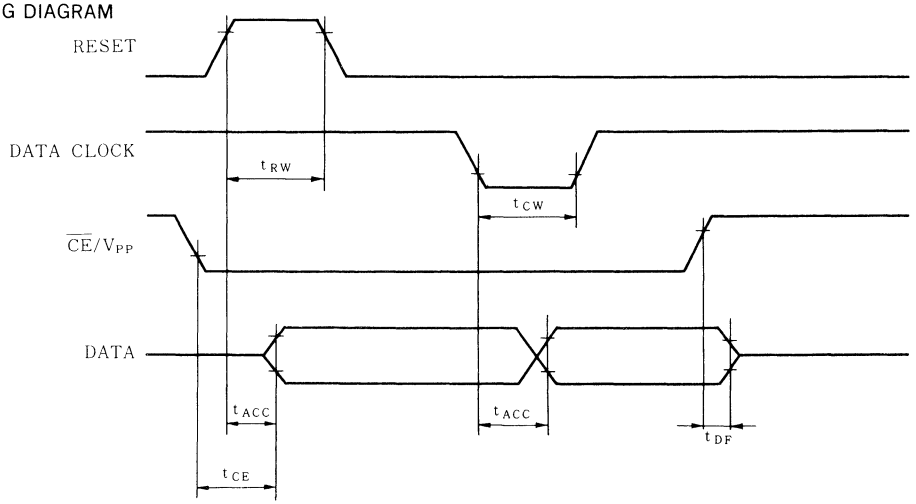
● D.C. PROGRAMMING CHARACTERISTICS ($Ta = 25℃ \pm 5℃$, $V_{CC} = 5V \pm 5\%$)

Symbol	Parameters		Test Conditions	Limits			Unit
				Min	Typ	Max	
I_{PP}	V_{PP} Supply Current		$\overline{CE}/V_{PP} = V_{IHP}$			5	mA
I_{CC}	V_{CC} Supply Current					0.5	mA
V_{IH}	Input High Voltage	Except TEST		2.0		$V_{CC}+0.3$	V
		TEST		4.0		$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	Except TEST		−0.1		0.8	V
		TEST		−0.1		1.0	V
V_{IHP}	Program pulse Input High Voltage			20.5	21.0	21.5	V
V_{ILP}	Program pulse Input Low Voltage			2.0	V_{CC}	6.0	V
I_{LI}	Input leakage Current	RESET,DATA CLOCK	$V_I = 0V, V_{CC} = 5.25V$	−170		−20	μA
		TEST	$V_I = 0V \sim V_{CC}$	−10		10	μA

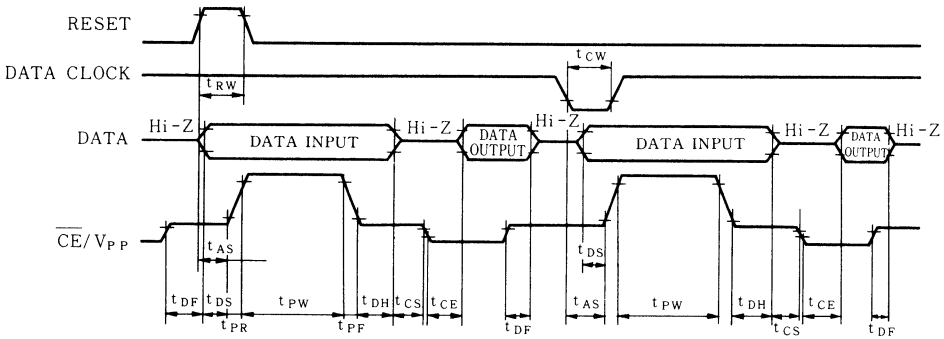
● PROGRAMMING CHARACTERISTICS ($Ta = 25℃ \pm 5℃, V_{CC} = 5V \pm 5\%$)

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
t_{AS}	Address Set-up Time	2			μs
t_{CS}	$\overline{CE}$ Set-up Time	2			μs
t_{DS}	Data Set-up Time	2			μs
t_{DH}	Data Hold Time	2			μs
t_{DF}	$\overline{CE}$ to Output Float	0		200	ns
t_{CE}	$\overline{CE}$ to Output Delay			1	μs
t_{PW}	Program pulse width	45	50	55	ms
t_{PR}	V_{PP} Pulse rise time	0.5		100	μs
t_{PF}	V_{PP} Pulse fall time	0.5		100	μs
t_{RW}	Reset pulse width	2			μs
t_{CW}	Clock pulse width	2			μs

■ TIMING DIAGRAM



● PROGRAM MODE



■ OPERATING MODES

Mode \ Pins	Data 1	Counter output 8	$\overline{CE}/V_{PP}$ 2	V_{CC} 3	GND 4
Read	Data Output	Clock (A5) Output	V_{IL}	V_{CC}	GND
Standby	High impedance	High impedance	V_{IH}	V_{CC}	GND
Program	Data Input	High impedance	V_{IHP}	V_{CC}	GND

	Counter operation mode
TEST (5) = GND	6 bits
TEST (5) = V_{CC}	7 bits

■ EXPLANATION ON OPERATION

● READ MODE

RF5H01/RP5H01 is a serial address type PROM with 6-bit/7-bit counter. The first bit can be read out by adding reset pulse after $\overline{CE}/V_{PP} = V_{IL}$. The 2nd bit~the 64th bit can be sequencially read out by adding data clock pulse. The output data is valid after a delay of t_{ACC} from reset rise up or data clock fall down, in the state of $\overline{CE}/V_{PP} = V_{IL}$.

In the state of TEST=GND, the counter operates as a 6-bit counter. It returns to the reset condition (address 000000), if it is added with 64-time data clock pulses after the reset pulse is applied.

The counter output pin is for operation test of the built-in counter. It puts out the highest output (A5) of the 6-bit counter.

● STANDBY MODE

RF5H01/RP5H01 is provided with power down function that is controlled by $\overline{CE}$ input. If TTL high level is given to the chip enable input ($\overline{CE}$), the device comes to be the Standby Mode, and the output is in the state of high impedance.

● PROGRAM MODE

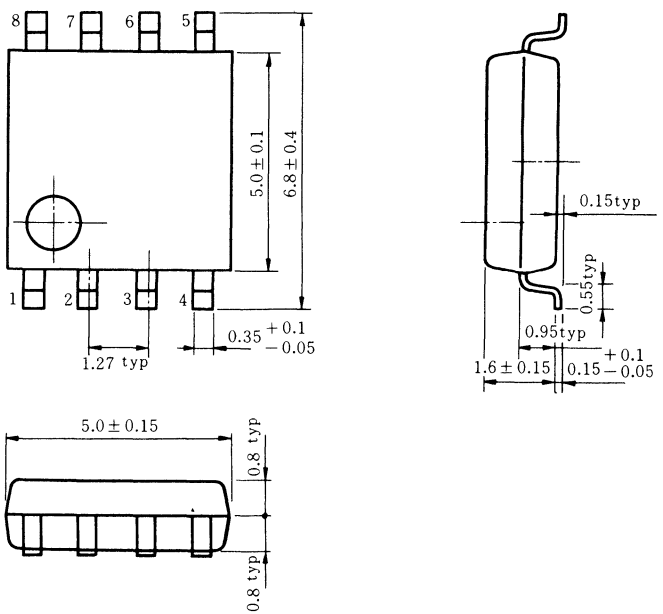
Initially, all bits of RF5H01/RP5H01 are in the "1" state. Data is introduced by selectively programming "0"into the desired bit locations.

The program is operated by setting up $\overline{CE}/V_{PP}=V_{IH}$, and adding the reset pulse, and then applying the 50mS 21V program pulse. The data are verified by making $\overline{CE}/V_{PP}=V_{IL}$. The 2nd bit~the 64th bit are programmed by progressing the addresses in sequence by means of adding the data clock pulse.

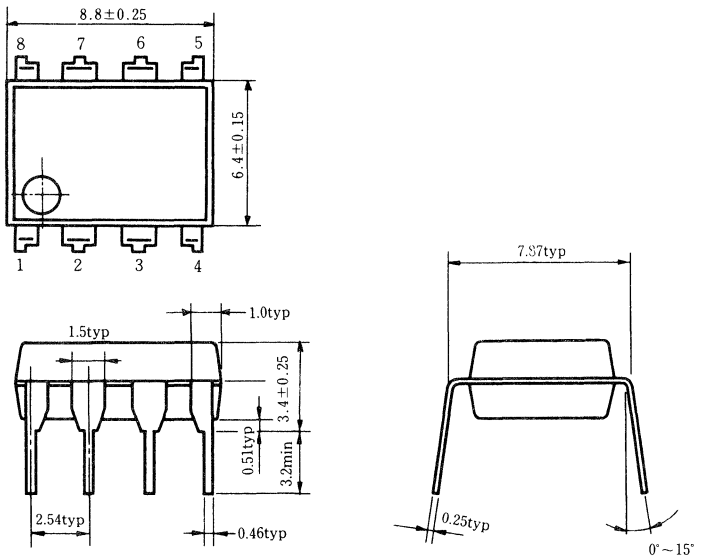
● DUMMY BITS

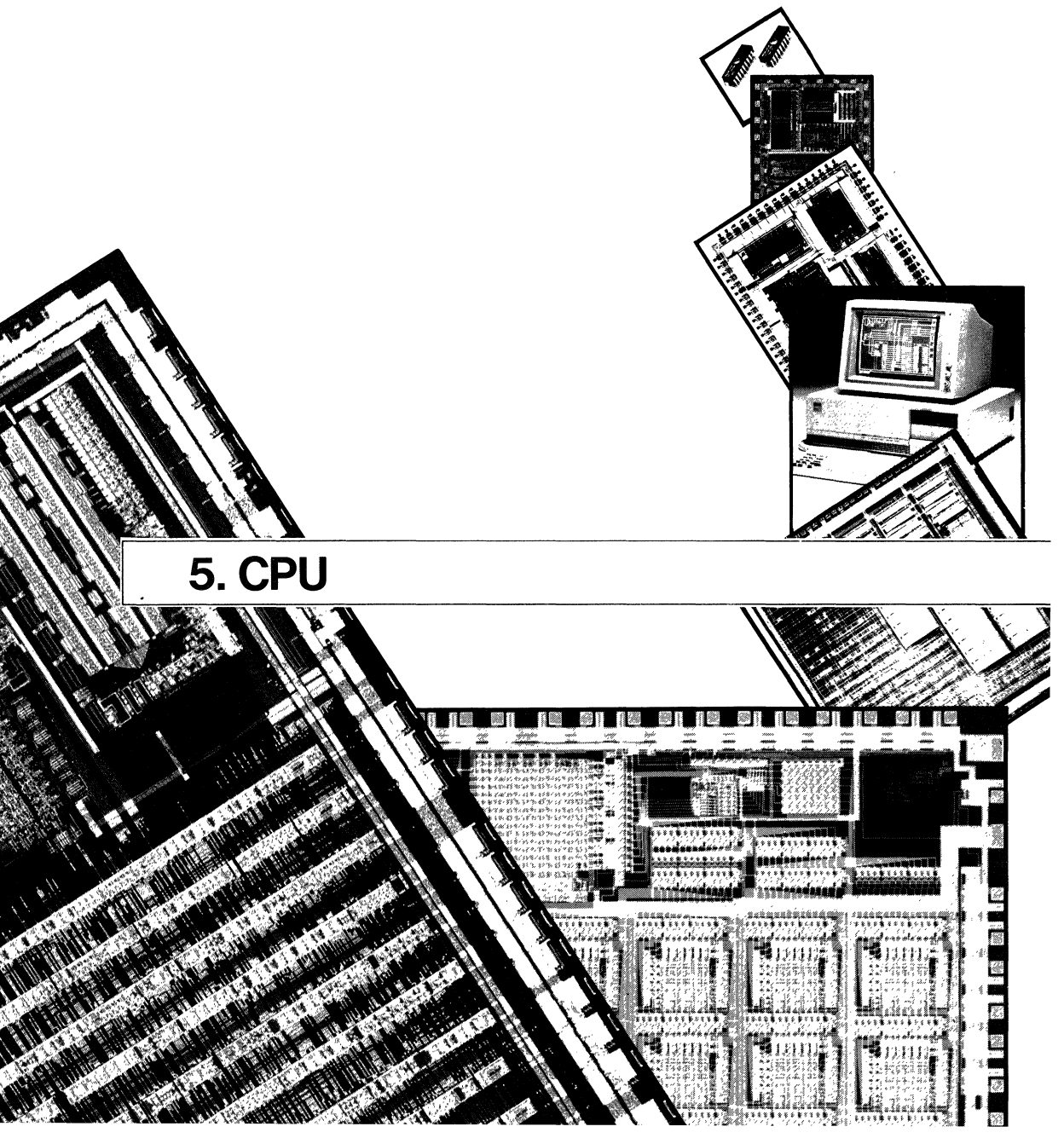
RF5H01/RP5H01 is a one-time PROM. For this reason, it is provided with a dummy bit of 8 bits for test programming. The dummy bit is located after the practical use 64th bit. The address is 8 bits of 1000000~1000111. The built-in counter operates as a 7-bit counter when "Test" (5 pins) is set at V_{CC} level, enabling to select the dummy bit. In the case of the "Test" being GND level, the counter operates as the 6-bit counter, being unable to select the dummy bit. In the 7-bit counter, when the clock pulse is added in sequence, the address progresses from 0000000 to 1111111, and then returns to 0000000.

■ 8-PIN PLASTIC FLAT PACKAGE (EXTERNAL VIEW) (UNIT : mm)



■ 8-PIN PLASTIC DIL PACKAGE (EXTERNAL VIEW) (UNIT : mm)





5. CPU

RICOH

Microelectronic Specification

RP65C02

CMOS 8-bit MICROCOMPUTER SYSTEM

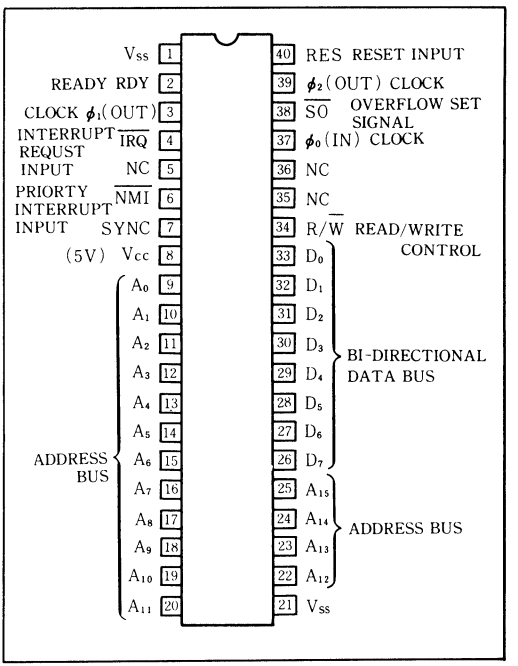
■ GENERAL DESCRIPTION

The RP65C02 is 8-bit CMOS CPU. It has the instruction set and pins which are fully compatible with the NMOS 6502 CPU, and in addition, with 59 new instructions. It is provided with the features of the CMOS such as the powerdown, standby mode, etc.

■ FEATURES

- Single power supply 5V operation
- CMOS silicon gate process
- Low power dissipation
- 8-bit bi-directional data bus, parallel processing
- 68-type 210 instructions
- Powerful 13-type addressing modes
- Programmable stack pointer
- Maskable interrupt and non-maskable interrupt
- 6-type internal registers
- Enable to connect the external memory with up to 64Kbytes
- Reference clock 1~4 MHz
- Executable single-instruction
- Computable decimal and binary
- Bus compatible with M6800
- Pin compatible with ROCKWELL R65C02

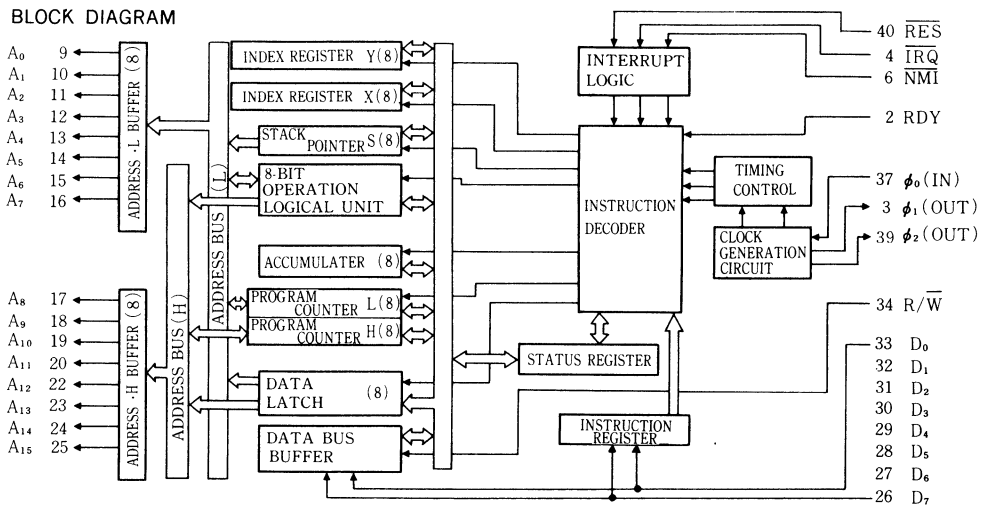
■ PIN CONFIGURATION (Top view)



■ APPLICATIONS

- Hand-held computer, etc.

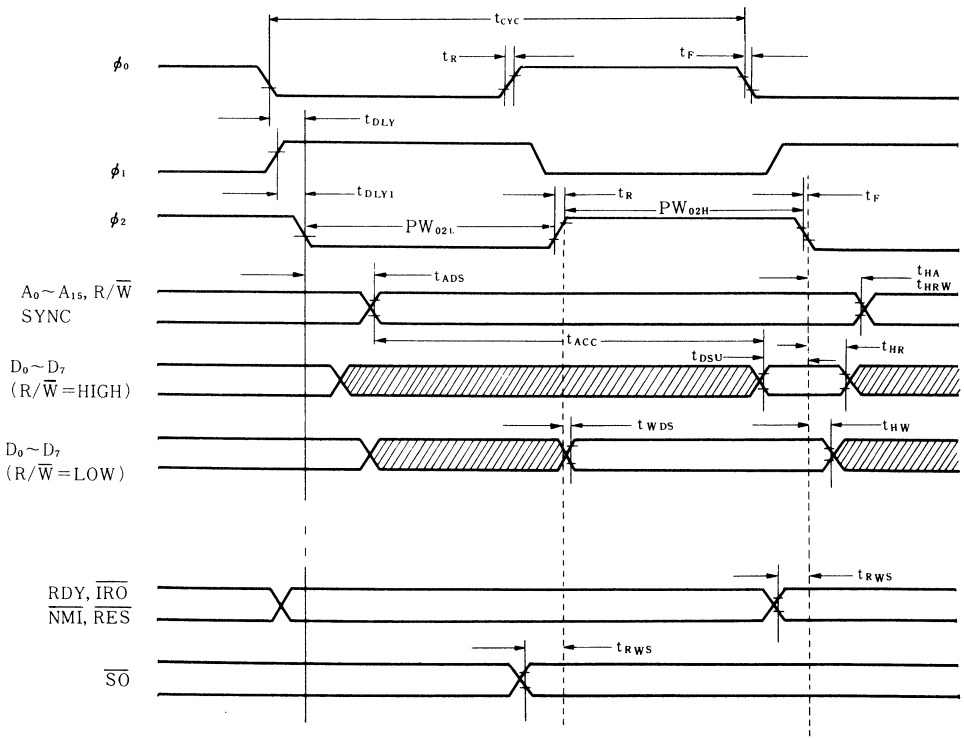
■ BLOCK DIAGRAM



● AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0±5%, Ta = 0℃ ~ 70℃, load 130pF)

Symbol	Parameters	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CYC}	Cycle time	1000		500		333		250		ns
PW_{02L}	ϕ_2 "Low" Clock Pulse Width	430	5000	210	5000	150	5000	100	5000	ns
PW_{02H}	ϕ_2 "High" Clock Pulse Width	450		220		160		110		ns
t_R, t_F	Clock rising time, Clock Falling Time		25		15		12		10	ns
t_{ADS}	Address Delay Time		225		140		110		90	ns
t_{HA}	Address Hold Time	20		20		15		15		ns
t_{HRW}	R/$\overline{W}$ Hold Time	30		30		30		30		ns
t_{DSU}	Read Data Setup Time	100		50		50		50		ns
t_{HR}	Read Data Hold Time	10		10		10		10		ns
t_{HW}	Write Data Hold Time	30		30		30		30		ns
t_{ACC}	Read Access Time	695		340		254		168		ns
t_{RWS}	Processor Control Setup Time (RDY, S.O, $\overline{IRO}$, $\overline{NMI}$, $\overline{RES}$)	200		110		80		60		ns
t_{WDS}	Write Data Delay Time		175		100		75		70	ns
t_{DLY}	Delay Time ϕ_0 to ϕ_2		100		100		100		100	ns
t_{DLY1}	Delay Time ϕ_1 to ϕ_2		50		50		50		50	ns

■ TIMING CHART



※ "H" 2.4V, "L" 0.4V

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Limits	Unit
V_{CC}	Supply Voltage	−30～+7.0	V
V_I	Input Voltage	−0.3～+7.0	V
P_d	Power Dissipation	500	mW
T_{opr}	Operating Ambient Temperature	0～+70	℃
T_{stg}	Storage Temperature	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\pm5\%$, $V_{SS}=0V$, Ta=0～+70℃)

Symbol	Parameters		Measuring Conditions	Specified Value Min	Typ	Max	Unit
V_{IH}	Input High Voltage	ϕ_0(in)		2.4		$V_{CC}+0.3$	V
		Logic		2.0		$V_{CC}+0.3$	
V_{IL}	Input Low Voltage	ϕ_0(in)		−0.3		0.4	V
		Logic		−0.3		0.8	
I_{IL}	Input Leak Current	Logic	$V_{CC}=5.25V$	−30		+10	μA
		ϕ_0(in)	$V_I=0$～5.25V	−10		+10	
I_{OL}	Output Floating Leakage Current Data Line		$V_I=0.4$～2.4V	−10		+10	μA
V_{OH}	Output High Voltage ϕ_1, ϕ_2, SYNC, D_0～D_7, A_0～A_{15}, R/$\overline{W}$		$I_{LOAD}=-100\mu A$ $V_{CC}=4.75V$	2.4			V
V_{OL}	Output Low Voltage ϕ_1, ϕ_2, SYNC, D_0～D_7, A_0～A_{15}, R/$\overline{W}$		$I_{LOAD}=1.6mA$ $V_{CC}=4.75V$			0.4	V
P_d	Power Disspation (no-load)		$I_C=0MHz$ (standby)		0.1	0.15	mW
			=1MHz		20	30	mW
			=2MHz		40	60	mW
			=3MHz		60	90	mW
			=4MHz		80	120	mW
			Low Power (RDY=0)		10	15	mW/MHz
C	Input Capacitance Logic					10	pF
	D_0～D_7					10	
	SYNC, A_0～A_{15}, R/$\overline{W}$		$V_I=0V$			10	
	ϕ_0(in)		f=1MHz			10	
	ϕ_1					30	
	ϕ_2					50	

Note : $\overline{IRQ}$, $\overline{NMI}$ need pull-up resistor.

■ EXPLANATION ON PIN FUNCTION

● Clock Input (ϕ_{0in})

It is the input terminal to generate the system clock in the inside and input the reference clock from the outside. The operating frequency is between 1 and 4 MHz. And when ϕ_{0in} stops at highlevel, the CPU becomes the stand-by mode.

● Clock Output (ϕ_{1out}, ϕ_{2out})

The two signal ϕ_{1out} or ϕ_{2out} output for the system-clock output. These are provided with each device for one part of control bus synchronous signal. ϕ_{1out} is address-time and the address becomes valid at ϕ_{1out} time. ϕ_{2out} is data-time and the data becomes valid at ϕ_{2out} time.

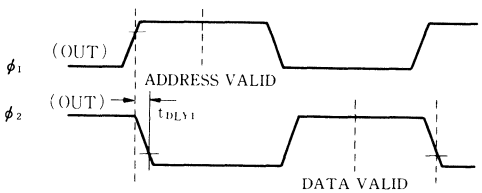


Fig.1 PHASE RELATION BY SYSTEM-CLOCK ϕ_{1OUT}, ϕ_{2OUT}

● Address Bus ($A_0 \sim A_{15}$)

$A_0 \sim A_{15}$ constiute a 16-bit address bus. The address that is indicated with these bits are hexadecimal \$0000~FFFF. (decimal 0~65535)

All TTL compatible, these address bus is capable of driving one-standard TTL and 130 pF.

● Data Bus ($D_0 \sim D_7$)

$D_0 \sim D_7$ constitute the 8-bit bidirectional data bus, input or output. All TTL compatible, these address bus is capable of driving one-standard TTL and 130pF.

● Bus Direction Indicative Signal ($R/\overline{W}$)

It is the signal to decide the direction of data bus.

In reading (input data from other device to the CPU) "1" is output, and in writing (output data from the CPU to other) "0" is output. Read or write timing are as shown in Fig.2, Fig.3.

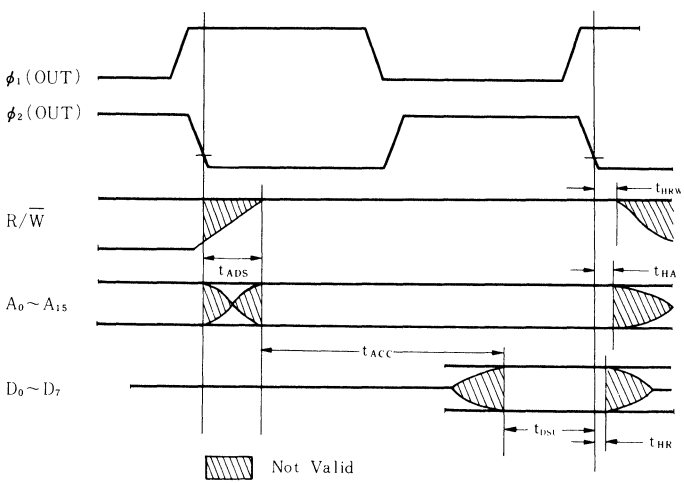


Fig.2 READ MODE TIMING

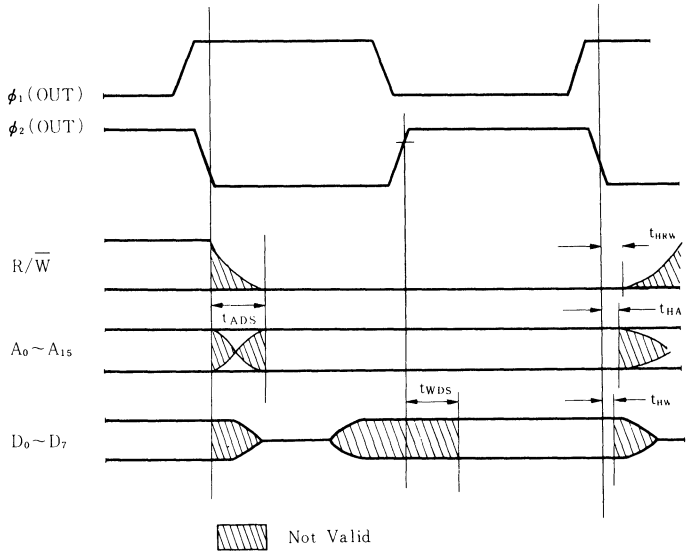


Fig.3 WRITE MODE TIMING

● Ready Signal (RDY)

This input allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state, during or coincident with ϕ_1, will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent ϕ_2 in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

● System Reset ($\overline{RES}$)

The input is used to reset the CPU in a power down state and to start. During that the input is Low level, READ/WRITE to the CPU is not all accepted. When the rising time signal of the pin is detected, the CPU becomes the reset mode at once.

After initial setting time of the 6 clock time, the interrupt mask flag is set, the CPU reads the vector address from each location (FFFC)(FFFD), and sets the program-counter.

The input consists of the Schmitt trigger circuit as which power on reset is acted by only CR.

● Interrupt Request Signal ($\overline{IRQ}$, $\overline{NMI}$)

$\overline{IRQ}$ (Interrupt Request)

If the TTL compatible input is the low level, the CPU starts the interrupt operation. When the instruction in execution is finished, the CPU allows the interrupt request, but at the same time, the interrupt mask bit in the status code register is checked, and if not set, the CPU begins the execution of the interrupt sequence. The program -counter and status register are loaded with stack, the interrupt mask flag is set so as not to accept any other interrupts. At the end of this cycle, the content of location FFFF load into high order 8-bit of program-counter, and the content of location FFFE load into low order 8-bit of programcounter. The program control is changed a memory vector which is stored these location.

To accept an interrupt, RDY signal should be high level. These are just same with all interruptions. When it is used to the wired OR with this pin, it must use a pullup resistor.

● $\overline{NMI}$ (Nonmaskable Interrupt)

When the falling signal is input in pin, the CPU detects this edge, and starts the nonmaskable interrupt operation.

$\overline{NMI}$ is unconditional interrupt request. When the instruction in execution becomes end, the similar

operation to IRQ is executed regardless of the state of interrupt mask flag.

In the vector address which is loaded to program counter, high order 8-bit are contents of location FFFB, and low order 8-bit are contents of location FFFA. The program counter changes to these addresses. When it uses the wired OR with this pin, it must use the pullup resistor.

$\overline{IPQ}$ and $\overline{NMI}$ are interrupt inputs of hardware which is sampled in the inside of the CPU during ϕ_2 time. After a instruction in execution comes at the end, it executes next interrupt routine from the first ϕ_1 time.

● Overflow Flag Set Signal ($\overline{SO}$)

The overflow flag bit (V) in the status code register is set by the falling edge input to this pin. As this signal is sampled by the rising edge, the input must be synchronized outside.

● Instruction Fetch Cycle Synchronous Signal (SYNC)

This output signal indicates the cycle that microprocesser fetch the instruction code.

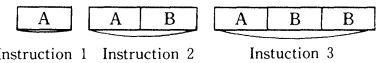
It becomes "High Level" at the ϕ_1 time that the instruction is load. During cycle time that SYNC is a high level, if RDY input is set at the low level, the CPU halts with the state until RDY becomes high level.

The single step execution is enabled by control of RDY.

Vector Address		Signal Names
MSB	LSB	
FFFF	FFFE	$\overline{IRQ}$
FFFD	FFFC	$\overline{RES}$
FFFB	FFFA	$\overline{NMI}$

■ ADDRESSING MODE

The Fig.4 shows a sample of pattern which machine language is stored in the memory. Generally the instruction consists of OP-code and operand (modifies the OP-code). The operand gives the information of address. Instruction 1 consists of the OP-code, and instruction 2 consists of the 1-byte OP-code and operand. Instruction 3 consists 1-byt OP-code, 2-byte operand. The CPU is informed the length of each instruction by the OP-code and is fetch the operand of the number of the required bytes by this information. The OP-code have the information which shows the kind of the operand. The kind of this operand is equivalent to the addressing mode.



A : OP-code

B : Operand

Fig.4 A SAMPLE OF PATTERN WHICH MACHINE LANGUAGE IS STORED IN MEMORY.

● Accumulator Addressing

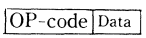
This type includes the addressing in the single byte and is equivalent to the execution in the accumulator.

The execution on the accumulator.

Fig.5 ACCUM

● Immediate Addressing

This type is 2-byte instructions having the OP -code and operand. The operand has not information of addressing, but describes the data itself.

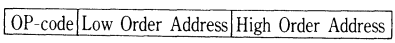


Address is nod needed.

Fig.6 IMMEDIATE

● Absolute Addressing

This type is 3-byte instruction (OP-code is 1-byte and operand is 2-byte). The 2-byte address indicates the low order , the third byte address the high order, all of 64 Kbytes is accessed.



Describes directly the execution address.

Fig.7 ABSOLUTE

● Zero Page Addressing

This type is 2-byte instruction of OP-code and operand. The high oder address is automatically set "00". With addressing a low oder address, it is able to code and the short of the execution. It is able to use efficiently the memory space and execute time by using the addressing suitably.

OP-code	Low Order Address

Execution high order address becomes "00"

Fig.8 ZERO PAGE

● Implied Addressing

The instruction code is 1-byte order. Almost all of the instruction control registers which is the internal memory equipment of the CPU. and needs no addressing.

OP-code

Without address.

Fig.9 IMPLIED

● Indexed Zero Page Addressing

This is 2-byte instruction of OP-code and operand. It is called as "ZERO PAGE X" or "ZERO PAGE Y" because the execution address is addressed with the indexed register (X or Y).

This is one of the zero page addressing. The high order addressing is set automaticaly "00", and low address is added with the content of the 2-byte. As the carry after the calculation is not added, the execute address does not exceed zero page.

OP-code	LOW Order Address

Execution High Order Address : 00

Execution Low Order Address :

Low Order Address	+	Index register (X or Y)

Neglect the carry.

Fig.10 Z PAGE X; ZPAGE Y

● Indxed Absolute Addressing

This is 3-byte instruction of 1-byte OP-code, 2 -byte operand. The execute addressing is addressed with the index (X or Y). It is called as "absolute X" or "absolute Y".

This is one of the absolute addressing. Execute address is added with the content of index register. The count of index and content of count are stored in the index register. And it is able to address the base address by the OP-code. It is able to modify the plural areas by using some base address and index, and the code and exceution time can be shortened.

OP-code	Low Order Address	High Order Address

Execution address :

High Order Address	Low Order Address	+	Index Register (X or Y)

Fig.11 ABS, X; ABS, Y

● Relative Addressing

This is 2-byte instruction of OP-code and operand. It is used only for the jump OP-code, and appoints the jump address, 2-byte oder of OP-code is called as "offset" and is added with the content of offset to the low oder 8-bit of program-counter set to the location of next instruction.

It has the range of-128 to +127-byte. The range of the branch is -128 to 127 byte from the head address of next instruction.

OP-code	Offset

Offset value is-128(80H)~+127(7FH)

Fig.12 RELATIVE

● Indexed Indirect Addressing

This is 2-byte instruction of OP-code and operand. As execute address is indirectly addressed, it is called as "Indirect X".

The execute address is added with 2-byte of instruction and content of X-register, and the carry is neglected. When the contcnt of calculation is the address of Zero page, the content stored in the address becomes the low order 8-bit of effective address, and the content of next address becomes the high order. The address of stored memory (high and low order) that appoints the effective address must be in the zero-page.

The content is stored in the address is low oder 8 bit of efffective address.

OP-code	Low Order Address

Execution Address Low Order :

00	Low Order Address + X register	content of address

Execution Address High Order :

00	Low Order Address + X register + 1	content of the address

Fig.13 (IND, X)

● Indirect Indexed Addressing

This is 2-byte instruction of OP-code and

operand. It is called as "Indirect, Y" as it appoints indirectly effective address. The 2-byte of OP-code shows the address of Zero page. The content of Y register is added with the content of memory, and the result becomes the low 8-bit of effective address. Carry is added to the content of next memory in the zero-page and it becomes the high oder 8-bit of effective address.

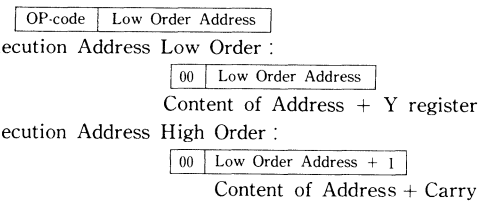


Fig.14 (IND),Y

● Indirect Addressing

This instruction is 2-byte of OP-code and operand. Execution address is address of Zero page.

Contents of this address becomes low oder 8-bit of execution address, and contents of the next address becomes high order 8-bit of execution address. This is the same operation as in the ease of X being zero in "indirect, X".

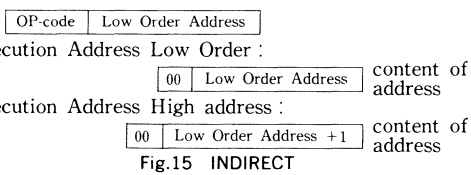
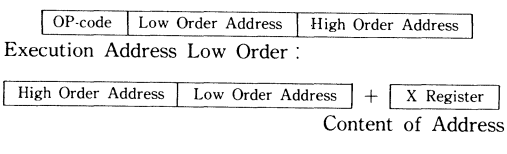


Fig.15 INDIRECT

● Indexed Absolute Indirect Addressing

This is 3-byte instruction (OP-code is 1-byte, operand is 2-byte). The result which adds the content of 2-byte or 3-byte to content of X register becomes the memory address that stores information of execution low order address 8-bit. The content of next address becomes high order 8 -bit of the execution address.



Execution Address High Order :

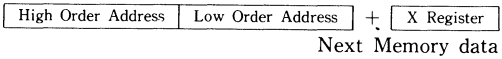


Fig.16 JMP (IND), X

● Absolute Indirect Addressing

The 2-byte of the instruction contains the low order 8-bit of a memory location. The high order 8-bit of that memory location are contained in the 3-byte of the instruction.

The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of effective address, which is loaded into the 16-bit of the program counter.

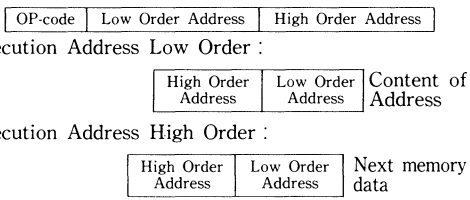


Fig.17 JMP (IND)

● Bit Addressing

In the instruction set (BBR, BBS, RMB, SMB), OP-code corresponds to bit OP-code.

〔BBR, BBS〕 This is 3-byte instruction (OP-code is 1-byte, operand is 2-byte). Execution address is zero page. Low order address is 2-byte of instruction.

3-byte of-instruction is offset content which points the address of branching.

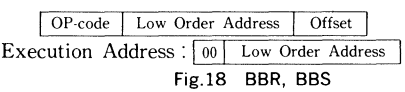


Fig.18 BBR, BBS

〔RMB, SMB〕 This is 2-byte instruction of OP-code, operand. Execution address is zero page, low order address is 2-byte of instruction.

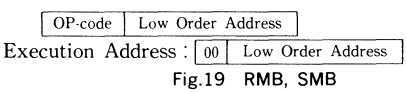
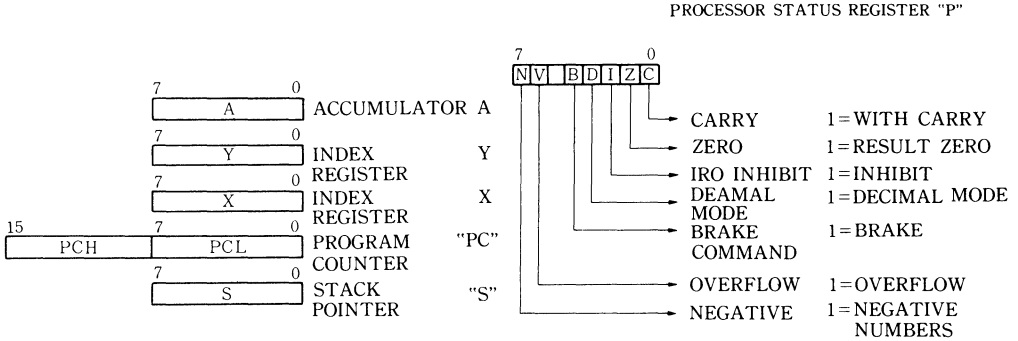


Fig.19 RMB, SMB

■ INTERNAL REGISTER



■ INSTRUCTION SET(Alphabetical order)

(2) ADC Add memory and accumulator with carry
(2) AND Logical AND memory and accumulator
ASL One bit left shift (memory or accumulator)
(1) BBR Branch if bit reset
(1) BBS Branch if bit is set
BCC Branch if carry is cleared
BSC Branch if carry is set
BEQ Branch if result is zero
(2) BIT Test memory bit with accumulator
BMI Branch if result is negative
BNE Branch if result is not zero
BPL Branch if result is positive
(1) BRA Unconditional branch
BRK Forced break
BVC Branch if overflow is cleared
BVS Branch if overflow is set
CLC Clear carry flag
CLD Clear decimal mode
CLI Clear disable interrupt
CLV Clear overflow flag
(2) CMP Compare memory with accumulator
CPX Compare memory with index registerX
CPY Compare memory with index registerY
(2) DEC Decrement memory
DEX Decrement index register X
DEY Decrement index register Y
(2) EOR Exclusive OR memory or accumulator
(2) INC Increment memory
INX Increment index register X
INY Increment index register Y
(2) JMP Jump to new location
JSR Jump to new location, hold return address
(2) LDA Load memory into accumulator
LDX Load memory into index register X
LDY Load memory into index register Y
LSR One bit right shift
(memory or accumulater)
NOP No operation
(2) ORA Logical OR memory and accumulator
PHA Push accumulator on stack
PHP Push processer status on stack
(1) PHX Push X register on stack
(1) PHY Push Y register on stack
PLA Pull accumulator from stack
PLP Pull processer status from stack
(1) PLX Pull X register from stack
(1) PLY Pull Y register from stack
(1) RMB Reset memory bit
ROL Rotate left circular of one bit (memory or accumulator)
ROR Rotate right circular of one bit (memory or accumulator)
RTI Return from interrupt
RTS Return from subroutine
(2) SBC Subtract memory and borrow from accumulator
SEC Set carry flag
SED Set decimal
SEI Set disable interrupt status
(1) SMB Set memory bit
(2) STA Store accumulator to memory
STX Store index register X to memory
STY Store index register Y to memory
(1) STZ Zero store
TAX Transfer accumulator to index register X
TAY Transfer accumulator to index registor Y
(1) TRB Test or reset bit
TSB Test or set bit
TSX Transfer stack pointer to accumulator
TXA Transfer index register to accumulator
TXS Transfer index register to stack pointer
TYA Transfer index register to accumulator

Note (1): the instructions are newly designed in 65C02
(2): the instructions are added addressing in 65C02

■ INSTRUCTION SET (Matrix map)

BRK Implied 17	-Operation Code -Addressing Mode -Byts : Cycles

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK Implied 1 7	ORA (IND,X) 2 6			TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**
1	BPL Relative 2 2**	ORA (IND),Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP,X 2 4	ASL ZP,X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS,Y 3 4*	INC Instruction 1 2		TRB ABS 3 6	ORA ABS,X 3 4*	SAL ABS,X 3 7	BBR1 ZP 3 5**
2	JSR Absolute 3 6	AND (IND,X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Instruction 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**
3	BMI Relative 2 2**	AND (IND),Y 2 5*	AND (IND) 2 5		BIT ZP,X 2 4	AND ZP,X 2 4	ROL ZP,X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS,Y 3 4*	DEC Instruction 1 2		BIT ABS,X 3 4*	AND ABS,X 3 4*	ROL ABS,X 3 7	BBR3 ZP 3 5**
4	RTI Implied 1 6	EOR (IND,X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Instruction 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**
5	BVC Relative 2 2**	EOR (IND),Y 2 5*	EOR (IND) 2 5			EOR ZP,X 2 4	LSR ZP,X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS,Y 3 4*	PHY Implied 1 3			EOR ABS,X 3 4*	LSR ABS,X 3 7	BBR5 ZP 3 5**
6	RTS Implied 1 6	ADC (IND,X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2†	ROR Instruction 1 2		JMP Indliect 3 5	ADC ABS 3 4†	ROR ABS 3 6	BBR6 ZP 3 5**
7	BVS Relative 2 2**	ADC (IND),Y 2 5*†	ADC (IND) 2 5†		STZ ZP,X 2 4	ADC ZP,X 2 4†	ROR ZP,X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS,Y 3 4*†	PLY Implied 1 4		JMP (IND),X 3 6	ADC ABS,X 3 4*†	ROR ABS,X 3 7	BBR7 ZP 3 5**
8	BRA Relative 2 3	STA (IND,X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY. Implied 1 2	BIT IMM 2 2	TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**
9	BCC Relative 2 2**	STA (IND),Y 2 6	STA (IND) 2 5		STY ZP,X 2 4	STA ZP,X 2 4	STX ZP,Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS,Y 3 5	TXS Implied 1 2		STZ ABS 3 4	STA ABS,X 3 5	STZ ABS,X 3 5	BBS1 ZP 3 5**
A	LDY IMM 2 2	LDA (IND,X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**
B	BCS Relative 2 2**	LDA (IND),Y 2 5*	LDA (IND) 2 5		LDY ZP,X 2 4	LDA ZP,X 2 4	LDX ZP,Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS,Y 3 4*	TSX Implied 1 2		LDY ABS,X 3 4*	LDA ABS,X 3 4*	LDX ABS,Y 3 4*	BBS3 ZP 3 5**
C	CPY IMM 2 2	CMP (IND,X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2	CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	
D	BNE Relative 2 2**	CMP (IND),Y 2 5*	CMP (IND) 2 5			CMP ZP,X 2 4	DEC ZP,X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS,Y 3 4*	PHX Implied 1 3			CMP ABS,X 3 4*	DEC ABS,X 3 7	BBS5 ZP 3 5**
E	CPX IMM 2 2	SBC (IND,X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INNX Implied 1 2	SBC IMM 2 2†	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**
F	BEO Relative 2 2**	SBC (IND),Y 2 5*†	SBC (IND) 2 5†			SBC ZP,X 2 4†	INC ZP,X 2 6	SMB7 ZP 2 5	SED Implied 1 2 ·	SBC ABS,Y 3 4*†	PLX Implied 1 4			SBC ABS,X 3 4*†	INC ABS,X 3 7	BBS7 ZP 3 5**
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

† Cycles Add 1 when decimal mode

* Cycles Add 1 when page crossing occurs

** Cycles Add 1 when branch in same page

LSD 0 0 Add 2 when branch in different page

Newly Designed Instruction

■ INSTRUCTION SET

ADDRESSING

Mnemomc	Operation	Immediate			Absolute			Zeropage			Accum			Implied			(IND,X)			(IND),Y		
		op	n	0	op	n	0	op	n	0	op	n	0	op	n	0	op	n	0	op	n	0
ADC	A + MIC→A (1)(5)	69	2	2	6D	4	3	65	3	2							81	6	2	71	5	2
AND	AAM→A A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2
ASL	C−				0E	6	3	06	5	2	0A	2	1									
BBR(#0·n)	Branch on Mb=0							−	5	3												
BBS(#0·n)	Branch on Mb=1							−	5	3												
BCC	Branch on C=0 (2)																					
BCS	Branch on C=1 (2)																					
BEQ	Branch on Z=1 (2)																					
BIT	AAM (b)	89	2	2	2C	4	3	24	3	2												
BMI	Branch on N=1 (2)																					
BNE	Branch on Z=0 (2)																					
BPL	Branch on N=0 (2)																					
BRA	Branch Alloys (2)																					
BRK	Broak													00	7	1		6				
BVC	Branch on V=0 (2)																					
BVS	Branch on V=1 (2)																					
CLC	0−C													18	2	1						
CLD	0−D													D8	2	1						
CLI	0−1													58	2	1						
CLV	0−V													B8	2	1						
CMP	A−M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2
CPX	X−M	E0	2	2	EC	4	3	E4	3	2												
CPY	Y−M	C0	2	2	CC	4	3	C4	3	2												
DEC	M−1→M				CE	6	3	C6	5	2	3A	2	1									
DEX	X−1→X													CA	2	1						
DEY	Y−1→Y													88	2	1						
EOR	AYM→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	
INC	M+1→M				EE	6	3	E6	5	2	1A	2	1									
INX	X+1→X													E8	2	1						
INY	Y+1→Y													C8	2	1						
JMP	Jumo to New Loc				4C	3	3										7C	6	3			
JSR	Jump Sub				20	6	3															
LDA	M−A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2
LDX	M−X (1)	A2	2	2	AE	4	3	A6	3	2												
LDY	M−Y (1)	A0	2	2	AC	4	3	A4	3	2												
LSR	0− −C				4E	6	3	A6	5	2	4A	2	1									
NOP	No Operation													EA	2	1						
ORA	AVM−A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11		2
PHA	A−Ms S−1→S													48	3	1						
PHP	P−Ms S−1→S													08	3	1						
PHX	X−Ms S−1→S													DA	3	1						
PHY	Y−Ms S−1→S													5A	3	1						
PLA	S+1→S Ms→A													68	4	1						
PLP	S+1→S Ms→P													28	4	1						
PLX	S+1→S Ms→X													FA	4	1						
PLY	S+1 Ms→Y													7A	4	1						
RMB(#0·n)	0→Mb (4)							−	5	2												
ROL					2E	6	3	26	5	2	2A	2	1									
ROR					6E	6	3	66	5	2	6A	2	1									
RTI	Rtrn Int Isoo Frg 11													40	6	1						
RTS	Rtrn Sub Isee.Frg 21													60	6	1						
SBC	A−M−C→A (1)(5)	E9	2	2	ED	4	4	E5	3	2							E1	6	2	F1	5	2
SEC	I→C													38	2	1						
SED	I→D													F8	2	1						
SEI	I→I													78	2	1						
SMB(#0·n)	I→Mg (4)							−	5	2							81	6	2	91	6	2
STA	A→M				8D	4	3	85	3	2												
STX	X→M				8E	4	3	86	3	2												
STY	Y→M				8C	4	3	84	3	2												
STZ	0→M				9C	4	3	64	3	2												
TAX	A→X													AA	2	1						
TAY	A→Y													A8	2	1						
TRB	A/\M→M				1C	6	3	14	5	2												
TSB	AVM→M				0C	6	3	04	5	2												
TSX	S→X													BA	2	1						
TXA	X→A													8A	2	1						
TXS	X→S													9A	2	1						
TYA	Y→A													98	2	1						

(Symbol Description)

X : Index X
Y : Index Y
A : Accumulator
M : Designated Memory with Effective Address

Ms : Designated Memory with Stack pointer
Mb : Zero page Memory Bit
M_7 : Memory Bit 7
M_6 : Memory Bit 6

+ : Add
− : Subtract
/\ : Logical AND
\/ : Logical OR
V : Exclusive OR
n : Machine Cycles
: Bytes

MODE

Zpage. X			ABS.X			ABS.Y			Relative			Indirect			Zpage. Y			Bit Addressing (OP by Bit 0)								Processor Status Codes							
op	n	0	op	n	0	op	n	0	op	n	0	op	n	0	op	n	0	0	1	2	3	4	5	6	7	7	6	5	4	3	2	1	0
																										N	V	·	B	D	I	Z	C
75	4	2	7D	4	3	79	4	3				72	5	2												N	V	·	·	·	·	Z	C
35	4	2	3D	4	3	39	4	3				32	5	2												N	·	·	·	·	·	Z	
16	6	2	1E	7	3																					N	·	·	·	·	·	Z	C
																		0F	1F	2F	3F	4F	5F	6F	7F	·	·	·	·	·	·	·	·
																		8F	9F	AF	BF	CF	DF	EF	FF	·	·	·	·	·	·	·	·
									90	2	2															·	·	·	·	·	·	·	·
									B0	2	2															·	·	·	·	·	·	·	·
									F0	2	2															·	·	·	·	·	·	·	·
34	4	2	3C	4	3																					M_7	M_6	·	·	·	·	Z	·
									30	2	2															·	·	·	·	·	·	·	·
									D0	2	2															·	·	·	·	·	·	·	·
									10	2	2															·	·	·	·	·	·	·	·
									8ø	3	2															·	·	·	·	·	·	·	·
																										·	·	·	1	·	1	·	·
									50	2	2															·	·	·	·	·	·	·	·
									70	2	2															·	·	·	·	·	·	·	·
																										·	·	·	·	·	·	·	0
																										·	·	·	·	0	·	·	·
																										·	·	·	·	·	0	·	·
																										·	0	·	·	·	·	·	·
D5	4	2	DD	4	3	D9	4	3				D2	5	2												N	·	·	·	·	·	Z	C
																										N	·	·	·	·	·	Z	C
																										N	·	·	·	·	·	Z	C
D6	6	2	DE	7	3																					N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
55	4	2	5D	4	3	59	4	3				52	5	2												N	·	·	·	·	·	Z	·
F6	6	2	FE	7	3																					N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
												6C	5	3												·	·	·	·	·	·	·	·
																										·	·	·	·	·	·	·	·
B5	4	2	BD	4	3	B9	4	3				B2	5	2												N	·	·	·	·	·	Z	·
						BE	4	3							B6	4	2									N	·	·	·	·	·	Z	·
B4	4	2	BC	4	3																					N	·	·	·	·	·	Z	·
56	6	2	5E	7	3																					O	·	·	·	·	·	Z	C
																											·	·	·	·	·	·	·
15	4	2	1D	4	3	19	4	3				12	5	2												N	·	·	·	·	·	Z	·
																											·	·	·	·	·	·	·
																											·	·	·	·	·	·	·
																											·	·	·	·	·	·	·
																											·	·	·	·	·	·	·
																										N	·	·	·	·	·	Z	·
																													(Restored)				
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																		07	17	27	37	47	57	67	77	·	·	·	·	·	·	·	·
36	6	2	3E	7	3																					N	·	·	·	·	·	Z	C
76	6	2	7E	7	3																					N	·	·	·	·	·	Z	C
																													(Restored)				
F5	4	2	FD	4	3																					·	·	·	·	·	·	·	·
						F9	4	3				F2	5	2												N	V	·	·	·	·	Z	(3)
																										·	·	·	·	·	·	·	1
																										·	·	·	·	1	·	·	·
																										·	·	·	·	·	1	·	·
95	4	2	9D	3	3													87	97	A7	B7	C7	D7	E7	F7	·	·	·	·	·	·	·	·
						99	5	3				92	5	2	96	4	2									·	·	·	·	·	·	·	·
94	4	2																								·	·	·	·	·	·	·	·
74	4	2	9E	3	3																					·	·	·	·	·	·	·	·
																										·	·	·	·	·	·	·	·
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										·	·	·	·	·	·	Z	·
																										·	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										N	·	·	·	·	·	Z	·
																										·	·	·	·	·	·	·	·
																										N	·	·	·	·	·	Z	·

NOTE (1) Add 1 to "N" when machine cycles or zero page crossing

(2) Add 1 to "N" when branch in same page
Add 2 to "N" when branch in different page

(3) Not carry = borrow

(4) Effect when zero page address

(5) Add 1 when decimal mode

(6) When the BIT (IMM mode), not related to M_7 or M_6 bit (N, V flag) of register P

■ Instruction Description (Alphabetical Order)

Descrption of symbol using in list

A	Accumulator	−	Subtract
X,Y	Index Register	∀	Exclusive OR
M	Memory	→	Transfer
P	Processor Status Register	←	Transfer
S	Stack Pointer	∨	Logical OR
Ms	Stack Memory	PCH	Program Counter High
Mb	Memory Bit	PCL	Program Counter Low
+	Add		
∧	Logical AND		

ADC Add with carry of memory and accumulator.
Operation : A+M+C → A "P" Register : N,V,Z,C

AND Logical AND of memory and accumulator. The result is stored in accumulator.
Operation : A∧M → A "P" Register : N,Z

ASL One bit left shift. LSB is placed "0". Contents of MSB is placed C.
Operation : C ← [7][6][5][4][3][2][1][0] ← "0" "P" Register : N,Z,C

BBR If specific bit of zero page is a reset state, branch relatively.

OP-Code	Low Order Address	Offset	3-byte instruction

If the specific bit (a bit is decided on the instruction code) of effective address [00][Low Order Address] is a reset state, relative branch by the [Offset] value on the basis of lead address of next instruction.
Operation : branch when $M_b = 0$ "P" Register : not affected

BBS If specific bit of zero page is a set state, branch relatively.

OP-code	Low Order Address	Offset	3-byte instruction

If the specific bit (a bit is decided on the instruction code) of effective address [00][Low Order Address] is a set state, relative branch by the [Offset] value to base with lead address of next instruction.
Operation : branch when $M_b = 1$ "P" Register : Not affected

BCC Branch if the carry is reset.
Operation : branch when C = 0 "P" Register : Not affected

BCS Branch if the carry is set.
Operation : branch when C = 1 "P" Register : Not affected

BEQ Branch if the zero flag is set.
Operation : branch when Z = 1 "P" Register : Not affected

BIT Test the memory bit by the accumulator.
Operation : $A \wedge M, M_7 \rightarrow N, M_6 \rightarrow V$
The bit 6 and bit 7 of the memory are transferred to "P" Register.
If the result of A∧M is zero, Z = 1 "P" Register : N, V, Z
$(M_7)(M_6)$

BMI Branch if result is negative.
Operation : branch when N = 1 "P" Register : Not affected

BNE Branch if result is not zero.
Operation : branch when Z = 0 "P" Register : Not affected

BPL Branch if result is positive.
Operation : branch when N ≒ 0 "P" Register : Not affected

BRA Unconditional branch. "P" Register : Not affected

BRK Forced break
Operation: Execute the interrupt. In this instruction, a lead address (2-byte) of next instruction is stored in the stack. At the same time, it is stored into contents of "P" Register. Program-counter (FFFE) → PCL, (FFFF) → PCH, and Execution of program is same vector address with IRQ. The difference from the IRQ interrupt is that in the BKK operation, the B flag of "P" register is set "1" and can't mask by the I flag.
"P" Register : $\overset{B}{1}$

BVC Branch if the overflow flag is reset.
Operation : branch when V = 0 "P" Register : Not affected

BVS Branch if the overflow flag is set.
Operation : branch when V = 1 "P" Register : Not affected

CLC Clear the carry flag (C)
Operation : 0 → C "P" Register : $\overset{C}{0}$

CLD Clear the decimal mode.
Operation : 0 → C "P" Register : $\overset{D}{0}$

CLI Clear the interrupt disenable flag (I).
Operation : 0 → I "P" Register : $\overset{V}{0}$

CLV Clear overflow flag.
Operation : 0 → V "P" Register : $\overset{V}{0}$

CMP Compare memory with accumulator.
Operation: A-M
The result is not stored. If it is nagative, N flag is set 1. If it is positive, C flag is set 1.
And if it is zero, Z and C flags are respectively 1. "P" Register : N, Z, C

CPX Compare memory with the index register X
Operation: Y-M
Flag condition of "P" Register is the same as CMP.
"P" Register : N, Z, C

CPY Compare memory with the index register Y.
Operation: Y-M
Flag condition of "P" Register is the same as CMP.
"P" Register : N, Z, C

DEC Decrement the contents of memory.
Operation : M − 1 → M "P" Register : N, Z

DEX Decrement the contents of index register X.
Operation : X − 1 → X "P" Register : N, Z

DEY Decrement the contents of index register Y.
Operation : Y − 1 → Y "P" Register : N, Z

EOR Execute the exclusive OR of memory and accumulator.

Operation : A∀M → A "P" Register : N, Z

INC Increment the contents of memory.
Operation : M+1 → M "P" Register : N, Z

INX Increment the contents of index register X.
Operation : X+1 → X "P" Register : N, Z

INY Increment the contents of index register Y.
Operation : Y+1 → Y "P" Register : N, Z

JMP Execution of program jumps to designation address.

Operation : | OP-Code | Operand | Operand | "P"Register : Not affected

The designation address by operands with 2-bytes is placed in PCL and PCH.

JSR The execution of program jumps to designation address.
Operation : When jump to designation address, return address (lead address of next instruction) is stored into stack. The return is executed by RTS.

OP-Code	Operand	Operand	"P"Register : Not affected

The disignation address by operands with 2 bytes is stored into the PCL and PCH.
Lead address of next instruction(2-byte)——M_S, S − 1 → S
└——M_S, S − 1 → S

LDA Load the contents of memory to the accumulator.
Operation : M → A "P" Register : N, Z

LDX Load the contents of memory to index register X.
Operation : M→X "P" Register : N, Z

LDY Load the contents of memory to index register Y.
Operation : M → Y "P" Register : N, Z

LSR One bit right shift. MSB (7bit) is placed to 0, LSB (0 bit) is loaded the C.
Operation : 0 → |7|6|5|4|3|2|1|0| → C "P" Register : $\overset{N}{0}$, Z, C

NOP No-operation
Operation : No operation "P" Register : Not affected

ORA Logical OR of memory and accumulator. The result is stored into the accumulator.
Operation : A∨M → A "P" Register : N, Z

PHA Store the contents of the accumulator into the memory stack.
Operation : A → Ms, S−1 → S "P" Register : Not affected

PHP Store the contents of the register P into the stack.
Operation : P → Ms, S−1 → S "P" Register : Not affected

PHX Store the contents of the index register X into the stack.
Operation : X → Ms, S−1 → S "P" Register : Not affected

PHY Store the contents of the index register Y into the stack.
Operation : Y → Ms, S−1 → S "P" Register : Not affected

PLA Pull accumulator from stack.
Operation : Ms → A, S+1 → S "P" Register : N, Z

PLP Pull processer status from stack.
Operation : Ms → P, S+1 → S "P" Register : Restore

PLX Pull X register from stack.
Operation : Ms → X, S+1 → S "P" Register : N, Z

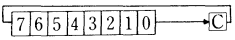
PLY Pull Y register from stack.
Operation : Ms → Y, S+1 → S "P" Register : N, Z

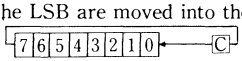
RMB Reset the specific bit in the zero page address.

OP-Code	Low Order Bit

2-byte instruction

The specific bit (a bit is decided by the instruction code) of execution address
00	Low Order Address
is reset.
Operation : 0 → M_b "P" Register : Not affected

ROL Rotate left circular of one bit. The contents of the MSB are moved into the C, the contents of the C are moved into the LSB.
Operation :  "P" Register : N, Z, C

ROR Rotate right circular of one bit. The contents of the C are moved into the MSB, the contents of the LSB are moved into the C.
Operation :  "P" Register : N, Z, C

RTI Return from interrupt. The return address in stack is loaded into the program counter, and it becomes the lead address of a next instruction of the interrupt.
Operation : M_S→P, S+1→S "P" Register : Restore
M_S→PCL, S+1→S
M_S→PCH, S+1→S

RTS Return from subroutine.
The return address in stack is loaded into the program counter. It becomes the lead address of a next instruction of the JSR.
Operation : M_S→PCL, S+1→S "P" Register : Not affected
M_S→PCH, S+1→S

SBC Subtract memory and borrow from accumulator, and the result is stored into the accumulator.
Operation : $\underset{\overline{C}=\text{borrow}}{A-M-\overline{C}} \rightarrow A$ "P" Register : N, V, Z, C

SEC Set carry flag.
Operation : 1 → C "P" Register : $\overset{C}{1}$

SED Set decimal flag.
Operation : 1 → D "P" Register : $\overset{D}{1}$

SEI Set disable interrupt status.
Operation : 1 → I "P" Register : $\overset{I}{1}$

SMB Set the specific bit of zero page address.

OP-Code	Low Order Bit

2-byte instruction

It sets the specific bit (a bit is decided on the instruction code) of effective address
00	Low Order Address
Operation : 1 → M_b "P" Register : Not affected

STA Store the contents of the accumulator into the memory.
Operation : A → M "P" Register : Not affected

STX Store the contents of the index register X into the memory.
Operation : X → M "P" Register : Not affected

STY Store the contents of the index register Y into the memory.
Operation : Y → M "P" Register : Not affected

STZ Clear the contents of memory.
Operation : 0 → M "P" Register : Not affected

TAX Transfer the contents of the accumulator to the index register X.
Operation : A → M "P" Register : N, Z

TAY Transfer the contents of the accumulator to the index register Y.
Operation : A → Y "P" Register : N, Z

TRB Reset the contents of memory by accumulator, and test at the same time.
Operation : A∧M → M
If the result is zero, Z flag=1 "P" Register : Z

TSB Set the contents of memory by accumulator, and test at the same time.
Operation : A∨M → M
If the result is zero, Z flag = 1 "P" Register : Z

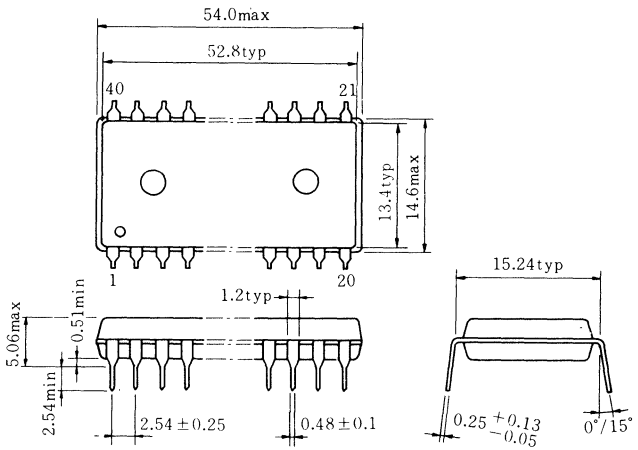
TSX Transfer stack pointer to the index register X.
Operation : S → X "P" Register : N, Z

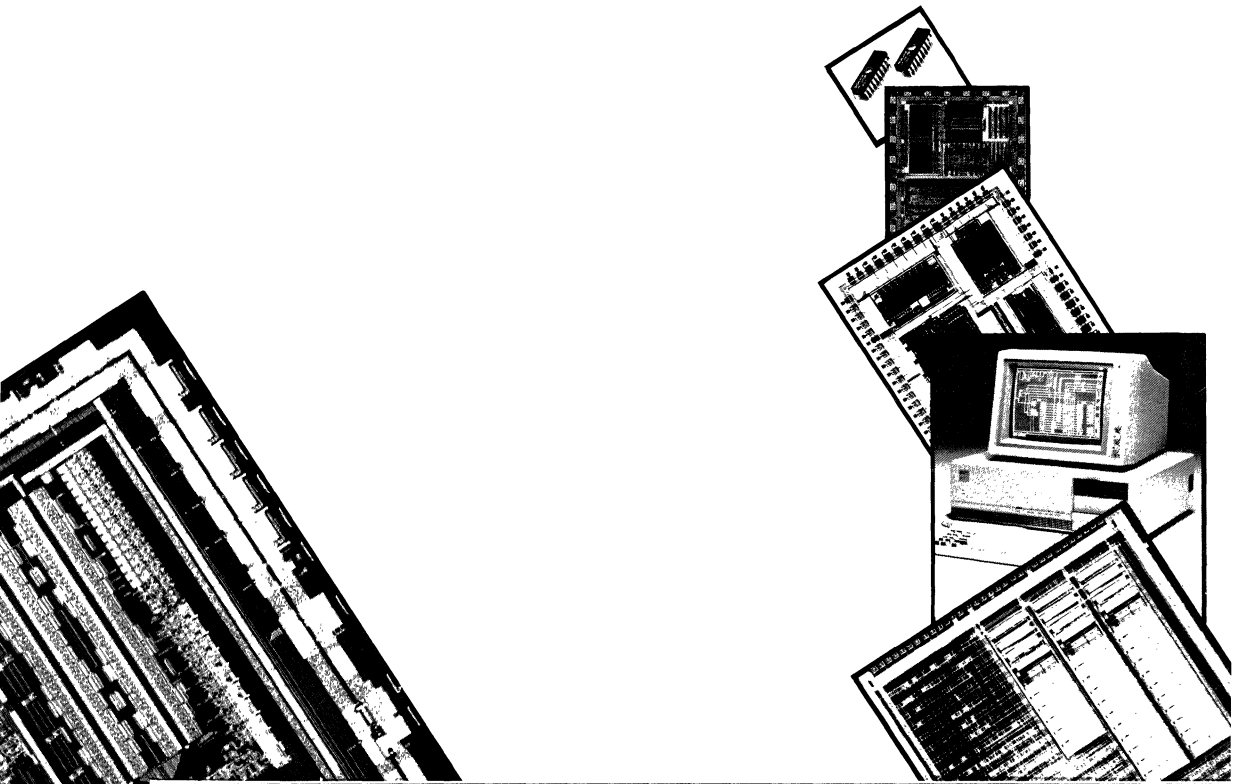
TXA Transfer the contents of the index register X to the accumulator.
Operation : X → A "P" Register : N, Z

TXS Transfer the contents of the index register X to stack pointer.
Operation : X → S "P" Register : Not affected

TYA Transfer the contents of the index register Y to the accumulator.
Operation : Y → A "P" Register : N, Z

■ 40-PIN DUAL-IN-LINE PACKAGE (UNIT : mm)





6. PERIPHERAL

REAL TIME CLOCK

RP/RF/RJ5C15

■ GENERAL DESCRIPTION

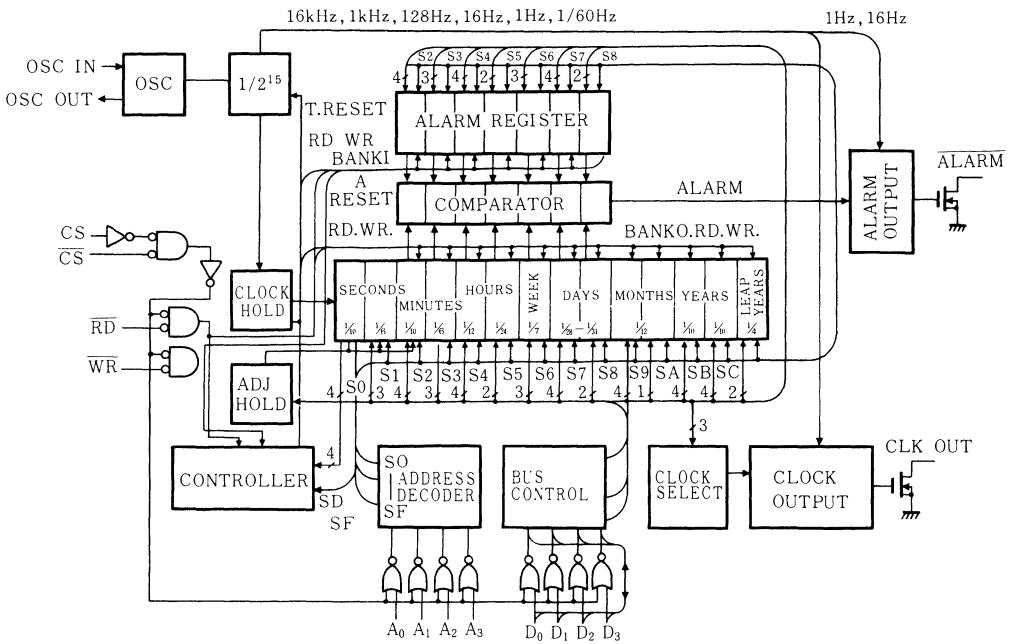
The 5C15 is a real-time clock for microcomputer that can be connected directly with the data bus of 16-bit CPUs such as 8086, Z8000 and 68000 as well as 8-bit CPUs such as 8085, Z-80, 6809 and 6502, and is able to set up and read a time in the same process with READ/WRITE of the memory.

It is provided with alarm function in addition to basic functions of time and calendar, and the battery backup is possible.

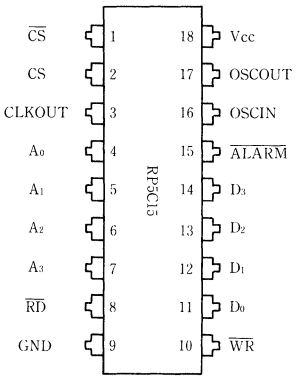
■ FEATURES

- Direct connection with CPU, and high speed access time.
- 4-bit bi-directional data bus $D_0 \sim D_3$
- 4-bit address input $A_0 \sim A_3$
- Counters for Time (hour, minute, second) and Calendar (leap year, year, month, date, day of the week) are built in.
- All the clock data are expressed with BCD code.
- ± 30 second adjustment function is built in.
- Battery backup is possible. (min. 2.0V)
- 16kHz, 1kHz, 128Hz, 16Hz, 1Hz, 1/60Hz are selectable as the reference clock.
- Alarm signal or timing pulse (16Hz or 1Hz) can be put out.

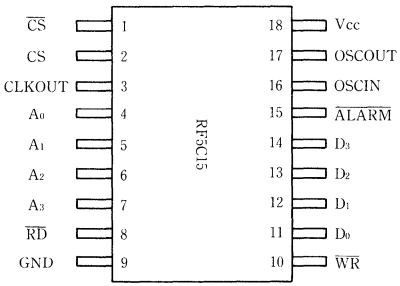
■ BLOCK DIAGRAM



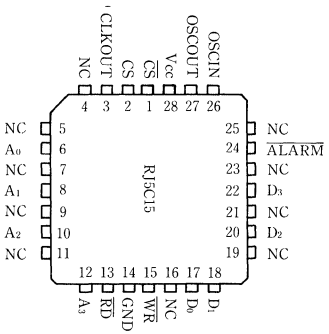
■ PIN CONFIGURATION



RP5C15



RF5C15



RJ5C15

■ PIN DESCRIPTION

Symbol	Function
$\overline{CS}$, CS	Terminals for external interfacing. Valid when CS=H, $\overline{CS}$=L. CS is connected to the power-down detector of peripheral power supply circiut and $\overline{CS}$ is connected to the microcomputer.
CLK OUT	Reference clock output terminal. Open drain output. 8 kinds of mode are selectable as seen in the table, according to content of the clock select register.
$A_0 \sim A_3$	ADDRESS pin. Connected to ADDRESS bus of CPU.
$\overline{RD}$	I/O control input. L when CPU←RP5C15.
GND	0 V
$\overline{WR}$	I/O control input. L when CPU→RP5C15.
$D_0 \sim D_3$	Bi-directional data bus. Connected to the data bus of CPU.
$\overline{ALARM}$	Alarm signal and pulse (16Hz CK or 1HzCK) are put out. Open drain output.
OSC IN, OSC OUT	Crystal resonator connecting terminal. 32.768kHz.
V_{CC}	+5V power supply.

■ ABSOLUTE MAXIMUM RATING

Symbol	Parameters	Conditions	Limits	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.3~7	V
V_I	Input Voltage		−0.3~7	V
V_O	Output Voltage		−0.3~7	V
P_d	Maximum Power Dissipation	Ta=25℃	400	mW
T_{opr}	Operating Ambient Temperature		−20~70	℃
T_{stg}	Storage Temperature		−40~125	℃

■ RECOMMENDED OPERATING CONDITIONS (Unless Noted : Ta=−20~70℃)

Symbol	Parameters	Specified Value			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{DH}	Data Hold Voltage	2.0		5.5	V
f_{XT}	Crystal Oscillation Frequency		32.768		kHz

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Unless Noted : Ta=−20~70℃, V_{CC}=5V±10%)

Symbol	Parameters	Measuring Conditions	Specified Value			Unit
			Min	Typ	Max	
V_{IH}	Input High Voltage		2.0		V_{CC}+0.3	V
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=2mA			0.4	V
I_{LI}	Input Leakage Current	V_I=0~5.5V			±10	μA
I_{OZ}	Output-off Leakage Current	V_{OZ}=0~5.5V			±10	μA
I_{CC1}	Standby Supply Current	f_{XT}=32.768kHz, V_{CC}=2.0V			15	μA
I_{CC2}	Operating Supply Current	f_{XT}=32.768kHz, V_{CC}=5.5 (NOTE1)			250	μA
V_{ILCS}	CS Pin Input "L" Voltage at Backup	V_{CC}=2.0V	−0.2		0.2	V
V_{IHCS}	$\overline{CS}$ Pin Input "H" Voltage at Backup	V_{CC}=2.0V	1.8		2.0	V

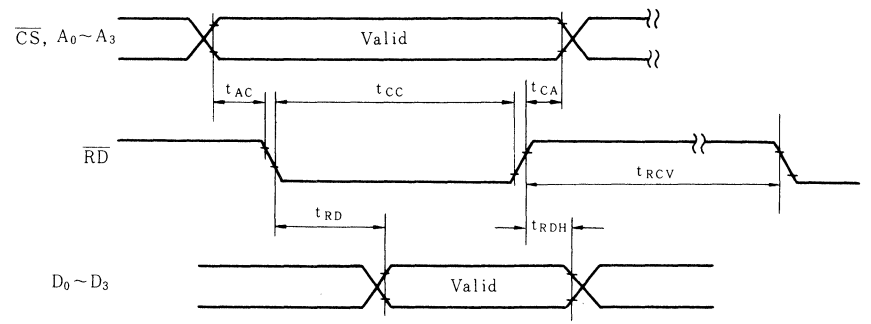
(NOTE 1) $\overline{RD}$, $\overline{WR}$ Signal Frequency : 100kHz, Input Terminal fixed V_{CC}, or GND level, Output Terminal Open

● AC ELECTRICAL CHARACTERISTICS (Unless Noted : Ta=−20~70℃, V_{CC}=5V±10%)

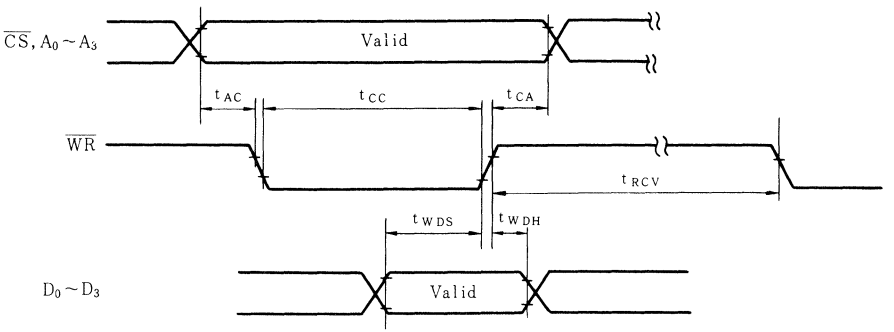
Symbol	Parameters	Measuring Conditions	Specified Value			Unit
			Min	Typ	Max	
t_{AC}	Address ~ $\overline{RD}$/$\overline{WR}$ Delay Time		50			ns
t_{CC}	$\overline{RD}$/$\overline{WR}$ Pulse Width		120		13,000	ns
t_{CA}	Address Valid Time After $\overline{RD}$/$\overline{WR}$ Rise		10			ns
t_{RD}	Data Delay Time After $\overline{RD}$ Fall	1TTL+100pF Load			120	ns
t_{RDH}	Data Hold Time After $\overline{RD}$ Rise		10			ns
t_{WDS}	Data Setup Time at Write in		100			ns
t_{WDH}	Data Hold Time at Write in		10			ns
t_{TED}	Timer Enable~Timer Disable		100			μs
t_{ADJ}	Adjust Completed Time				100	μs
t_{AINH}	Alarm Write Inhibit Time after Alarm set		100			μs
t_{RCV}	$\overline{RD}$/$\overline{WR}$ Recovery Time		1			μs

■ TIMING DIAGRAM

● READ CYCLE



● WRITE CYCLE



■ ADDRESS ASSIGNMENT

MODE		BANK 0				BANK 1				
$A_3 \sim A_0$		D_3	D_2	D_1	D_0	Contents	D_3	D_2	D_1	D_0
0	1 Sec. Counter					CLK OUT Select Register	×			
1	10 Sec. Counter	×				adjust	×	×	×	
2	1 Min. Counter					Alarm 1 Min. Register				
3	10 Mins. Counter	×				Alarm 10 Mins Register	×			
4	1 Hr. Counter					Alarm 1 Hr. Register				
5	10 Hrs. Counter	×	×			Alarm 10 Hrs. Register	×	×		
6	Week Counter	×				Alarm Week Register	×			
7	1 Day Counter					Alarm 1 Day Register				
8	10 Days Counter	×	×			Alarm 10 Days Register	×	×		
9	1 Month Counter						×	×	×	×
A	10 Months Counter	×	×	×		12/24 Hour Selecter	×	×	×	
B	1 Year Counter					Leap Year Counter	×	×		
C	10 Years Counter						×	×	×	×
D	MODE Register	Timer EN	Alarm EN	×	BANK 1/0		Timer EN	Alarm EN	×	BANK 1/0
E	TEST Register	Test 3	Test 2	Test 1	Test 0		Test 3	Test 2	Test 1	Test 0
F	RESET Register	$\overline{1Hz}$ ON	$\overline{16Hz}$ ON	Timer RESET	Alarm RESET		$\overline{1Hz}$ ON	$\overline{16Hz}$ ON	Timer RESET	Alarm RESET

× : Don't care for WR, always 0 for RD.

■ CLOCK OUTPUT SELECT REGISTER

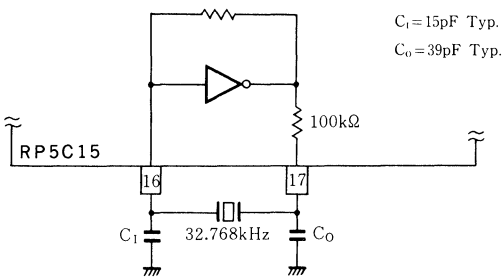
D_3	D_2	D_1	D_0	CLK OUT	Remark
×	0	0	0	"Z"	High Impedance
×	0	0	1	16.384kHz	duty 50%
×	0	1	0	1.024kHz	duty 50%
×	0	1	1	128 Hz	duty 50%
×	1	0	0	16 Hz	duty 50%
×	1	0	1	1 Hz	∫ Second Counter Count up, duty 50%
×	1	1	0	1/60 Hz	∫ Minute Counter Count up, duty 50%
×	1	1	1	"L"	

■ ADJUST FUNCTION

BANK 1 Address (A_3, A_2, A_1, A_0)=(0, 0, 0, 1) Data (D_3, D_2, D_1, D_0)=(×, ×, ×, 1)	If adjusted during the Second counter being 0~29, the Second comes to be 0, and if adjusted during 30~59, the minute is counted up, and the Second comes to be 0.

■ OSCILLATION CIRCUIT

As the output stabilizer resistor ($\approx$100kΩ) is built in, it is not necessary to fix it externally.



● MODE REGISTER $(A_3, A_2, A_1, A_0) = (1, 1, 0, 1) = D$

D_3	D_2	D_1	D_0	
Timer EN	Alarm EN			
		×	0	BANK 0 : Setup and Read of time
		×	1	BANK 1 : Setup and Read of Alarm, $\overline{12h}$/24h and Leap year, Selection of CLK OUT Operation of Adjust.
	1			: Alarm output ENABLE
	0			: Alarm output DISABLE (16Hz and 1Hz signals are independent)
1				: Time count starts
0				: Time count after Second stops

● LEAP YEAR COUNTER

Leap year when $D_1 = D_2 = 0$. It counts up simultaneously with Year Counter.

● $\overline{12h}$/24h SELECTOR

24-hour counter when $D_0 = 1$

12-hour counter when $D_0 = 0$

PM when $D_1 = 1$, and AM when $D_1 = 0$ respectively of 10h counter

● RESET CONTROLLER 16 Hz · 1HzCK REGISTER

$(A_3, A_2, A_1, A_0) = (1, 1, 1, 1) = F$

$D_0 = 1$: Resetting of all alarm registers

$D_1 = 1$: Resetting of frequency divisions before Second

$D_2 = 0$: 16Hz CK pulse ON

$D_3 = 0$: 1Hz CK pulse ON

● ADDRESS 0~D

Both READ and WRITE are possible.

● ADDRESS E~F

WRITE only is possible.

● TEST REGISTER $(A_3, A_2, A_1, A_0) = (1, 1, 1, 0,) = E$

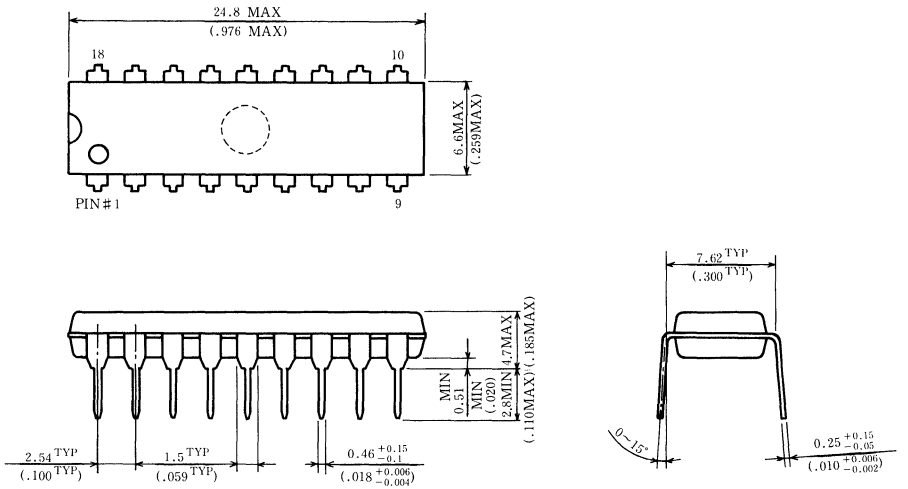
Register to be used for our inspection.

Normal count is operated by setting up data $(D_3, D_2, D_1, D_0) = (0, 0, 0, 0)$.

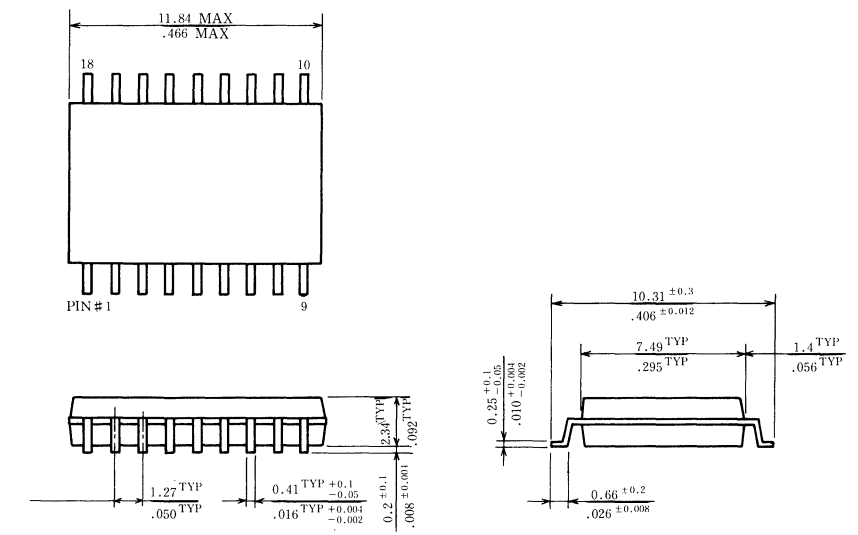
*Please refer to "Application Manual" that we offer.

■ PACKAGE DIMENSION (Unit: mm/inch)

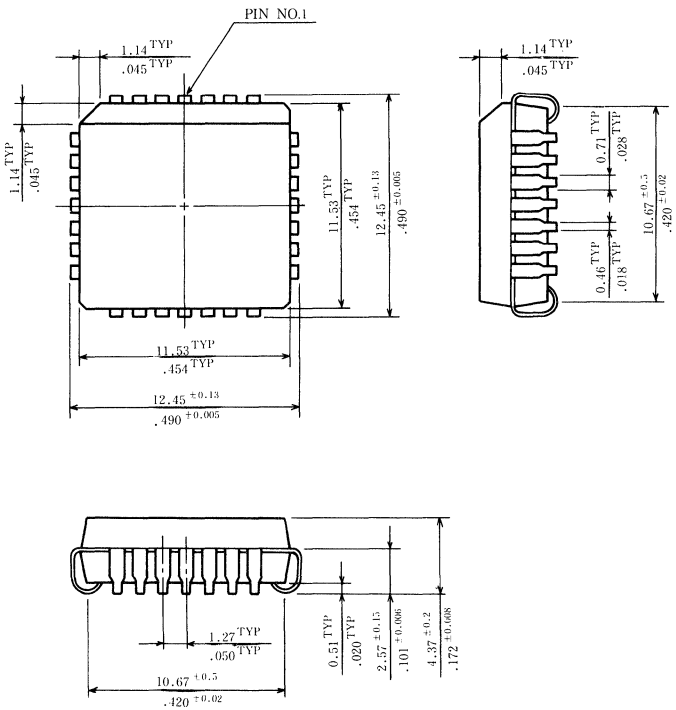
● RP5C15(18pin DIP)



● RF5C15(18pin FLAT)



● RJ5C15(24pin PLCC)



Microelectronic Specification

RP5C01

REAL TIME CLOCK WITH RAM

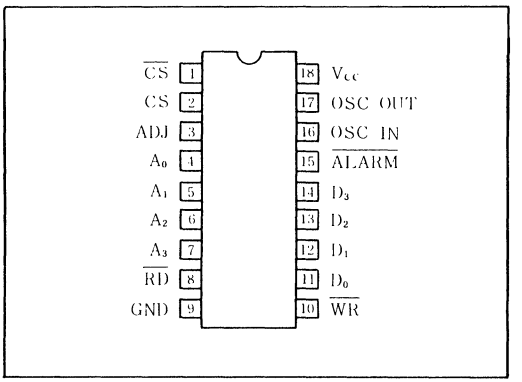
■ GENERAL DESCRIPTION

The RP5C01 bus compatible real-time clock is designed for use with most of the popular microprocessors such as the 8085A, Z-80 and others. Time setting and readout can be readily done in the same manner as writing/readout in and from memory. This RTC device features : counters for complete time-of-day clock alarm, a hundred year calendar, also a 26 × 4-bit RAM providing battery backed-up functions and applications as an involatile RAM.

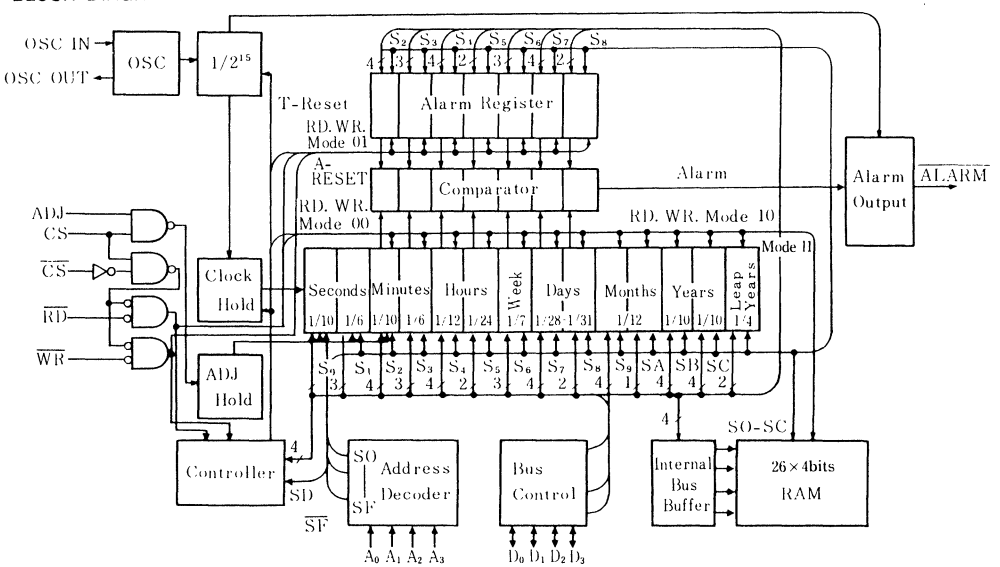
■ FEATURES

- Direct connection with CPU-Bus
- 4-bit bi-directional bus ; D_0-D_3
- 4-bit address input ; A_0-A_3
- Counters for Time (hour, minute, second) and Calendar (leap year, year, month, date, day of the week) are built in.
- 24 Hours, or 12 Hours am/pm display
- All the clock data is BCD encoded
- ADJ terminal for ±30 seconds adjustment
- Provision for battery-backup
- Self contained 26 × 4 bit RAM
- Provision for Alarm signal, or 16Hz or 1Hz Timing pulse output.

■ PIN CONFIGURATION (Top view)



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Conditions	Limits	Unit
V_{CC}	Supply Voltage	With respect to GND	−0.3~7	V
V_I	Input Voltage		−0.3~7	V
V_O	Output Voltage		−0.3~7	V
P_d	Power Dissipation	Ta=25℃	700	mW
T_{OPR}	Operating Ambient Temperature		0~70	℃
T_{STG}	Storage Temperature		−40~125	℃

■ RECOMMENDED OPERATING CONDITIONS (Unless Noted : Ta=0~70℃)

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{DH}	Data Hold Voltage	2.2		5.5	V
f_{XT}	Crystal Oscillation Frequency		32.768		kHz

■ ELECTRICAL CHARACTERISTICS

● DC ELECTRICAL CHARACTERISTICS (Unless Noted : Ta=0~70℃, V_{CC}=5V±10%)

Symbol	Parameters	Measuring Conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=2mA			0.4	V
I_I	Input Current	V_I=0~5.5V			±10	μA
I_{LO}	Output Leakage Current				±10	μA
I_{CC1}	Standby Supply Current	f_{XT}=32.768kHz V_{CC}=2.2V			15	μA
I_{CC2}	Operating Supply Current	f_{XT}=32.768kHz V_{CC}=5.0V (N2)			250	μA

(NOTE 1) : Current flow is 'positive' when flowing toward the IC.
(NOTE 2) : When connected to a CPU R/W cycle-time is 10μs.

● AC ELECTRICAL CHARACTERISTICS (Unless Noted : Ta=0~70℃, V_{CC}=5V±5%)

Symbol	Parameters	Measuring Conditions	Limits			Unit
			Min	Typ	Max	
t_{AC}	Address−$\overline{RD}$/$\overline{WR}$ Delay Time		170			ns
t_{CC}	$\overline{RD}$/$\overline{WR}$ Pulse Width		400		10000	ns
t_{CA}	Address Valid Time After $\overline{RD}$/$\overline{WR}$ Pulse Rise		10			ns
t_{RD}	Data Delay Time After $\overline{RD}$ Fall				340	ns
t_{RDH}	Data Hold Time After $\overline{RD}$ Rise		0			ns
t_{WDL}	Data Delay Time After $\overline{WR}$ Fall				40	ns
t_{WD}	Data Hold Time After $\overline{WR}$ Rise		20			ns

SPECIFICATIONS Under $V_{CC}=5V\pm10\%$ are as follows.

● **AC ELECTRICAL CHARACTERISTICS** (Unless Noted : Ta = 0~70℃, $V_{CC}=5V\pm10\%$)

Symbol	Parameters	Measuring Conditions	Limits			Unit
			Min	Typ	Max	
t_{AC}	Adress−$\overline{RD}/\overline{WR}$ Delay Time		170			ns
t_{CC}	$\overline{RD}/\overline{WR}$ Pulse Width		450		10000	ns
t_{CA}	Effective Address Time After $\overline{RD}/\overline{WR}$ Pulse Rise		10			ns
t_{RD}	Data Delay Time After$\overline{RD}$ Fall				400	ns
t_{RDH}	Data Hold Time After $\overline{RD}$ Rise		0			ns
t_{WDL}	Data Delay Time After $\overline{WR}$ Fall				40	ns
t_{WD}	Data Hold Time After $\overline{WR}$ Rise		20			ns

■ PIN DESCRIPTION

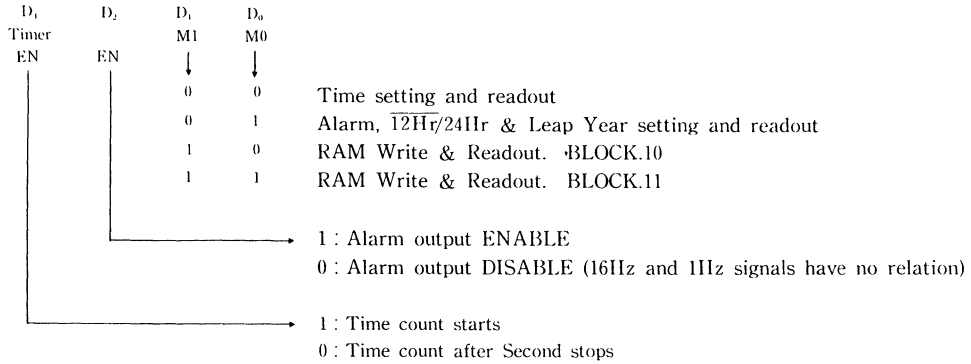
Symbol	Pin No.	Function
$\overline{CS}$, CS	1, 2	Terminals for external interfacing. Valid when CS=H, $\overline{CS}$=L. CS is connected to the power-down detector of peripheral circiut power supply, and $\overline{CS}$ is connected to the microcomputer.
ADJ	3	This pin provides easy zero setting for the "seconds" independently of the CPU. When ADJ=H in the range of from 0 to 29 secs, the "seconds" are preset at zero and not released in the range of 30 to 59 secs by countup until the full minute expires.
A_0~A_3	4, 5, 6, 7	ADDRESS pin. Connected to ADDRESS bus of CPU.
$\overline{RD}$	8	I/O control input. L when CPU← RP5C01.
GND	9	0 V
$\overline{WR}$	10	I/O control input. L when CPU→RP5C01.
D_0~D_3	11, 12, 13, 14	Bi-directional data bus. Connected to the data bus of CPU.
$\overline{ALARM}$	15	Alarm signal and pulse (16Hz CK or 1HzCK) are put out. Open drain output.
OSC_{IN}, OSC_{OUT}	16, 17	Crystal resonator connecting terminal. 32.768kHz.
V_{CC}	18	+5V power supply.

■ ADDRESS MODES

MODE	MODE 00					MODE 01					10	11
$A_3 \sim A_0$	Contents	D_3	D_2	D_1	D_0	Contents	D_3	D_2	D_1	D_0	Contents	Contents
0	1 Sec Counter						×	×	×	×		
1	10 Sec Counter	×					×	×	×	×		
2	1 Min Counter					Alarm 1 Min Register					block 10	block 11
3	10-Min Counter	×				Alarm 10 Min Register	×					
4	1-Hr Counter					Alarm 1 Hr Register						
5	10 Hr Counter	×	×			Alarm 10 Hr Register	×	×			4bit	4bit
6	Day Counter	×				Alarm Day Register	×				×	×
7	1 Day Counter					Alarm 1 Day Register					13	13
8	10 Day Counter	×	×			Alarm 10 Day Register	×	×				
9	1 Mo Counter						×	×	×	×	RAM	RAM
A	10-Mo Counter	×	×	×		$\overline{12\ Hr}$/24 Hr Selector	×	×	×			
B	1-Yr Counter					Leap Year Counter	×	×				
C	10-Yr Counter						×	×	×	×		
D	MODE Register	Timer EN	Alarm EN	MODE Register M1	M0		Timer EN	Alarm EN	MODE Register M1	M0	As at left	As at left
E	TEST Register	Test 3	Test 2	Test 1	Test 0		Test 3	Test 2	Test 1	Test 0	As at left	As at left
F	RESET Controller and Others	1Hz ON	16Hz ON	Timer RESET	Alarm RESET		1Hz ON	16Hz ON	Timer RESET	Alarm RESET		

× indicates : don't care for WR, always zero for RD.

● MODE REGISTER (A_3, A_2, A_1, A_0) = (1, 1, 0, 1) = D



● LEAP YEAR Counter

Leap year when $D_1 = D_2 = 0$. It counts up simultaneously with Year Counter.

● 12h/24h Selector

24-hour counter when $D_0 = 1$

12-hour counter when $D_0 = 0$

PM when $D_1 = 1$, and AM when $D_1 = 0$ respectively of 10h counter

● RESET Controller 16Hz · 1HzCK Register

(A_3, A_2, A_1, A_0)=(1, 1, 1, 1)=F

$D_0 = 1$: Resetting of all alarm registers

$D_1 = 1$: Resetting of frequency divisions before Second

$D_2 = 0$: 16Hz CK pulse ON

$D_3 = 0$: 1Hz CK pulse ON

● ADDRESS 0~D

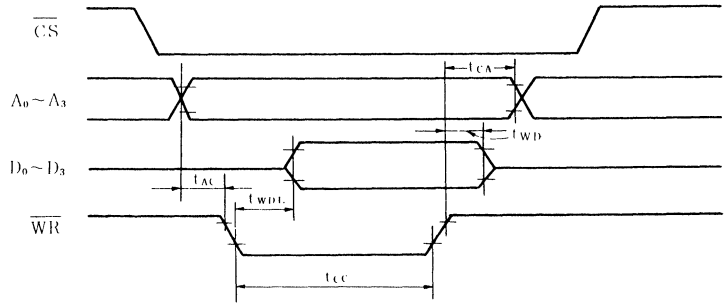
Both READ and WRITE are possible.

● ADRESS E~F

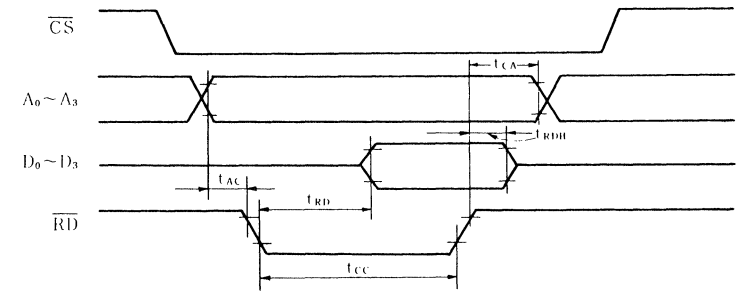
WRITE only is possible.

■ TIMING DIAGRAM

• WRITE CYCLE (CS="H")



READ CYCLE (CS="H")



■ APPLICATION NOTES

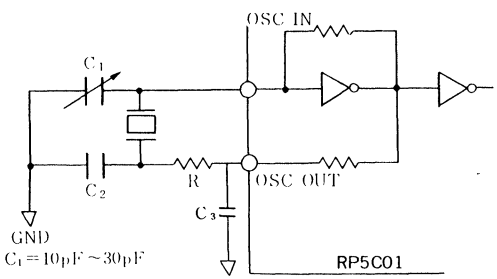
1. Oscillating Circuit

1-1 When using a crystal oscillating element.

The oscillator circuit is shown in Figure 1. Externally connected parts consist of : a resistor, capacitors and a trimmer capacitor. To adjust the frequency, use the trimmer capacitor (The 16Hz or 1Hz signal output at the $\overline{ALARM}$ pin should be used), for calibration.

When calibrating with the 16Hz signal :
The Address is $(A_3, A_2, A_1, A_0)=(1, 1, 1, 1)$.
The Data is $(1, 0, 0, \times)$.

When calibrating with the 1 Hz signal:
The Address is $(A_3, A_2, A_1, A_0)=(1, 1, 1, 1)$
The Data is $(0, 1, 0, \times)$.



$C_1 = 10pF \sim 30pF$
$C_2 = 30pF$
$C_3 = 56pF$
$R = 100k\Omega$

(The crystal employed is Nippon Dempa Kogyo MX38Tor equivalent)

Fig. 1

1-2 When using an external Clock

The external clock should be connected through the circuits shown in Fig.2(a), and (b). The OSCOUT pin should be left with no connection.

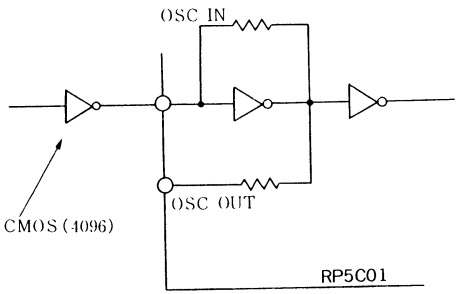


Fig.2 (a) CMOS INVERTER CONNECTION

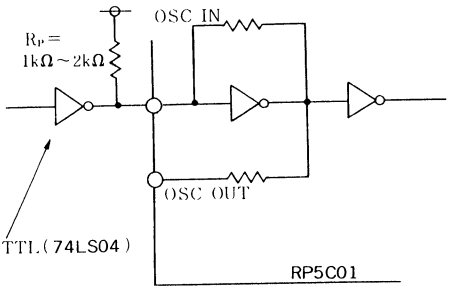


Fig.2 (b) TTL INVERTER CONNECTION

2. Input/Output, and Chip selection Pins.

2-1 Input/Output Pins

In order to stabilize the potential at the Input/Output Pins during 'battery backup' operation, and a pull -down resistor (100~300kΩ), and a pull up resistor (4.7~47kΩ)

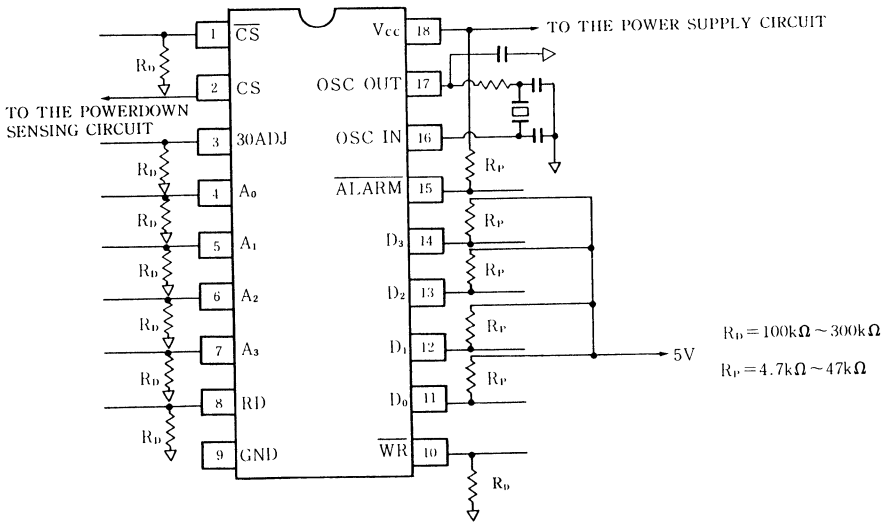


Fig. 3

2-2 Chip selection Pins

There are two chip selection Pins. The CS pin should be connected to the powerdown sensing circuit, and the $\overline{CS}$ pin to the CPU. CS is active "H", whereas $\overline{CS}$ is active "L".

3. Interfacing with typical CPU

3-1 Applicable CPU

CPU	External Circuit
Z-80A	Nil
8085A	74LS74 (NOTE 1)
6800	74LS00, 74LS04

(NOTE 1) Not needed when the X'tal used is below 5MHz

3-2 Standard Interfacing examples.

Examples of Interfacing the RTC with typical CPU (Z80,8085,6800) are presented hereunder.

(1) Z80

The Data Bus, Address Bus, and $\overline{RD}$, $\overline{WR}$ pins are connected to the corresponding pins of the Z-80 (the same symbols are used). The $\overline{CS}$ pin of the RP5C01 should connect with the IORQ pin, or one Bit of the Address Bus (e.g.A_0).

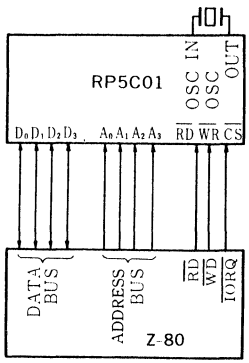
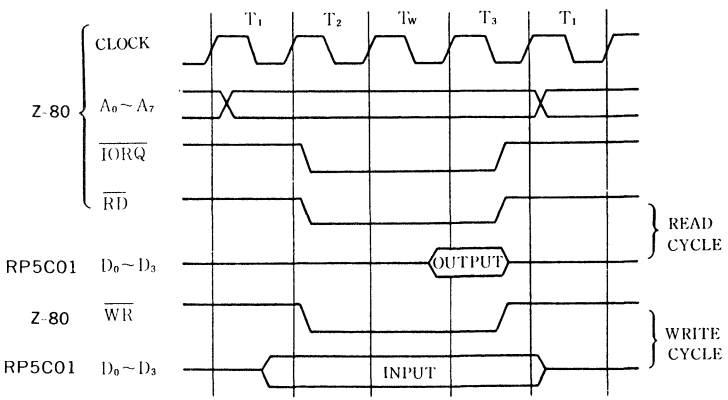


Fig. 4 CONNECTION DIAGRAM WITH Z-80

TIMING CHART



(2) 8085

The Data Bus, Address Bus, and $\overline{RD}$, $\overline{WR}$ pins of the RTC correspond with those of the 8085 (the same symbols are used). The $\overline{CS}$ pin of the RP5C01 should connect with one Bit of the 8085 Address Bus (e.g.pin A_0).

When the crystal oscillator used has a frequency of 6MIIz, a 74LS74 (externally connected circuit shown in the dotted line) should be added to provide 1 Wait.

Connection Diagram

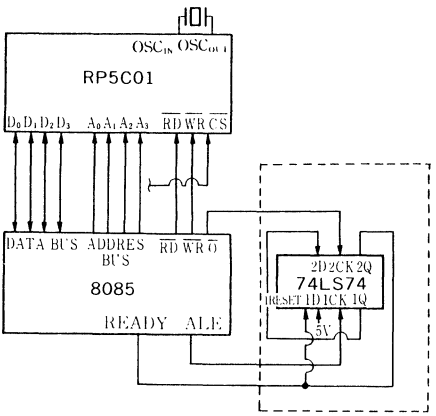
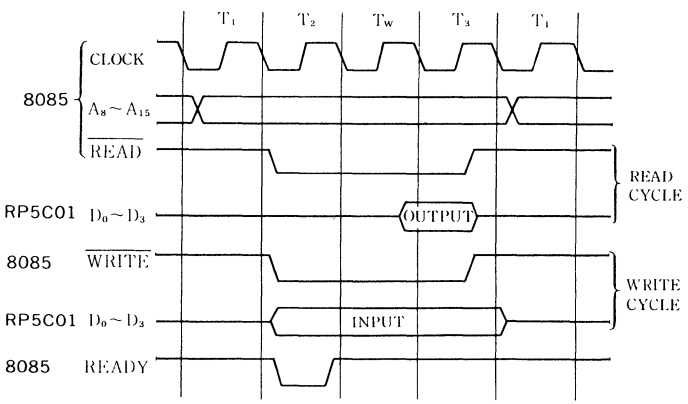


Fig. 5 CONNECTION EXAMPLE WITH 8085

Timing Chart



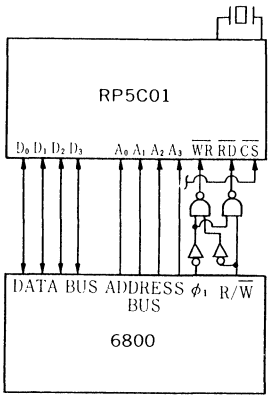
(3) 6800

The pin connections for the RTC are compatible with the Data Bus, Address Bus of the 6800. (The symbols are the same).

The $\overline{RD}$, $\overline{WR}$, pins of the RP5C01 should be connected to the ϕ_1, and R/W pins of the 6800, but with the addition of the following : two 74LS04 inverters, two input NANDs and two 74LSOO.

Besides, the $\overline{CS}$ pin of the RTC should be connected to one Bit of the 6800 Address Bus (e.g.A_0).

Connection Diagram



Timing Chart

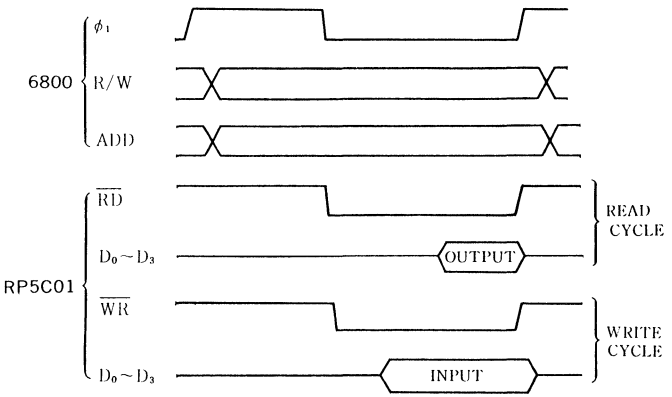
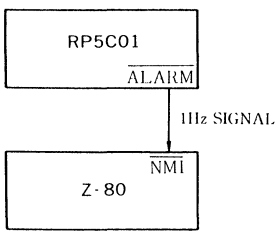


Fig. 6

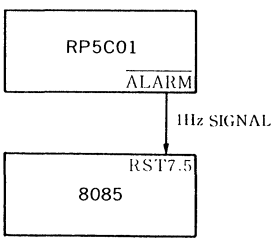
3-3 Interrupt into the CPU

The Data of RP5C01 is read-out by using Interrupt to the CPU at the rate of once every second.

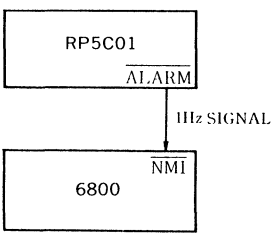
(1) Z80



(2) 8085



(3) 6800



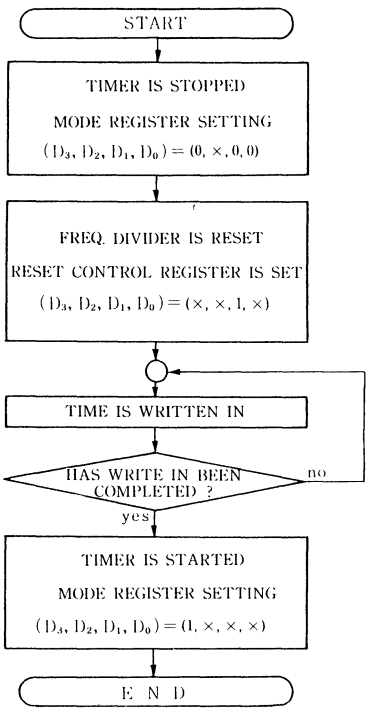
4. Example of a program for setting Time/Alarm

4-1 Flowchart for the time setting operation

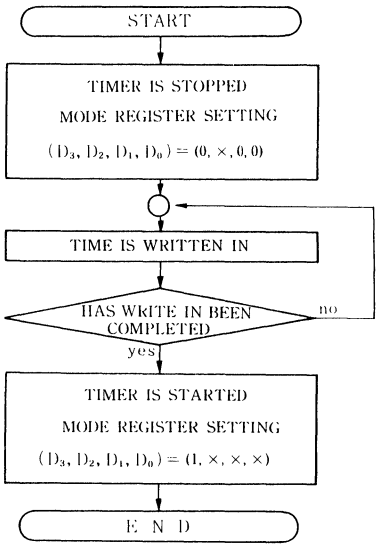
By setting Data (D_3, D_2, D_1, D_0) in the test register (Address (A_3, A_2, A_1, A_0)=(1, 1, 1, 0)), operation of the clock is maintained.

For Time setting, the Timer is stopped, and readout and write-in should be executed within one second.

(1) Timer Setting Program

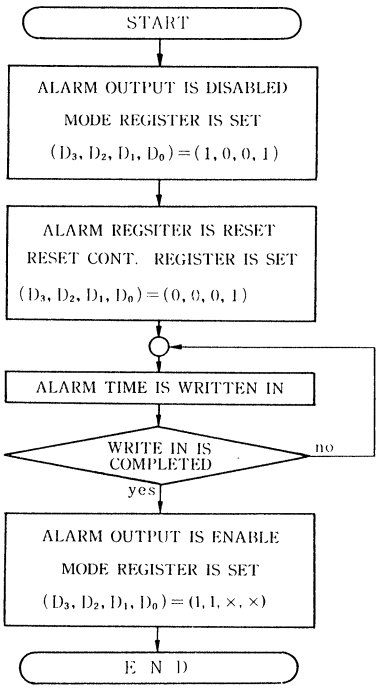


(2) Time Readout Program

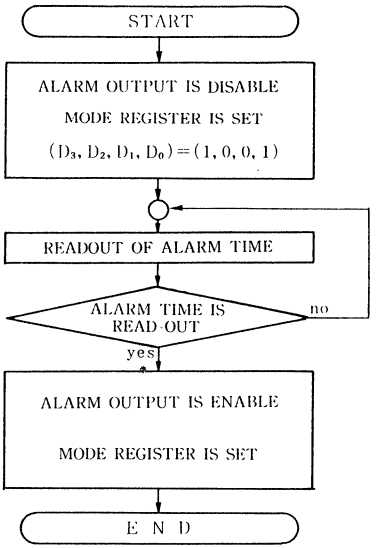


4-2 Alarm Setting Flowchart

(1) Alarm Time Write-in Program



(2) Read-out of Alarm Time

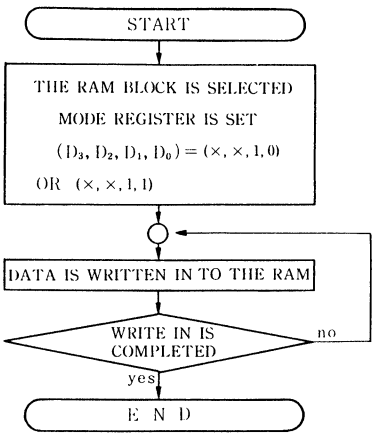


5. Read/Write With RAM Program

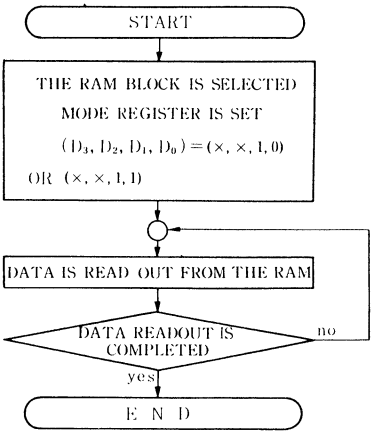
The 26 × 4 Bit User RAM, has provisions for Battery Backup, and can be used as a non-volatile RAM.

The RAM consists of two Blocks (1 Block : 13×4 Bits). A Mode Register enables Selecting the needed Block.

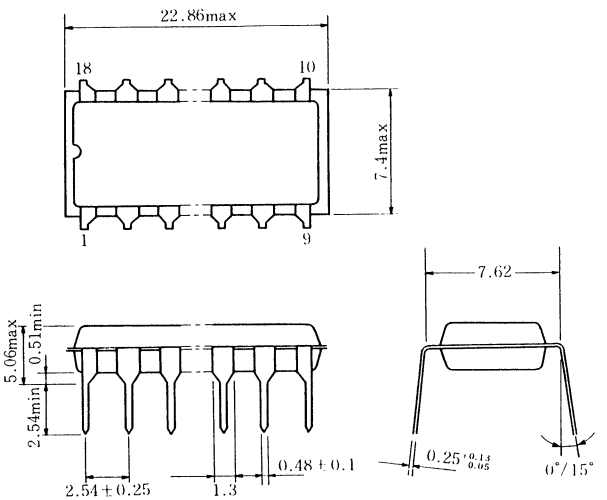
(1) Write-in



(2) Read-out



■ 18 PIN PLASTIC PACKAGE (UNIT : mm)



REAL TIME CLOCK
RP5C62/RF5C62

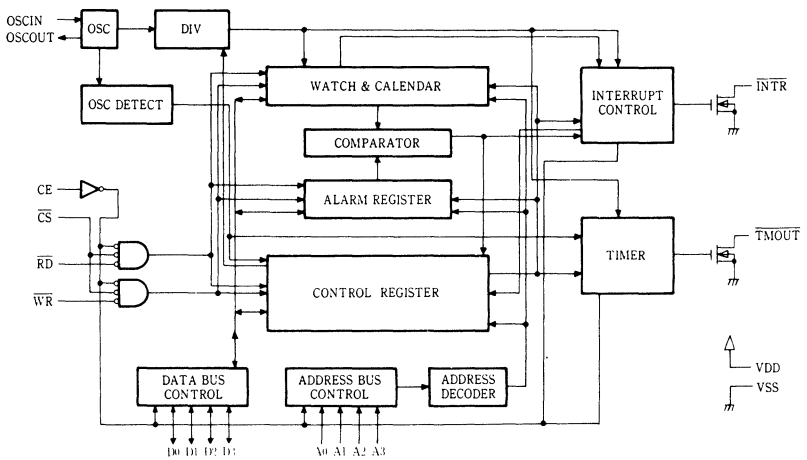
■ OUTLINE

RP5C62/RF5C62 can be connected directly to 8086, 68000, and other CPU data buses. RP5C62/RF5C62 are CMOS realtime clock LSIs with time, calendar, and alarm functions for microcomputer. The built-in timer counter allows the clocks to be used as watchdog timers or interrupt timers.

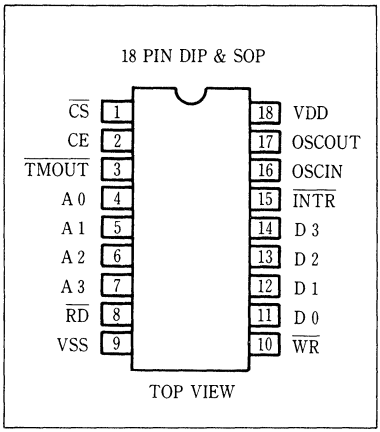
■ FEATURES

- RP5C62/RF5C62 can be connected directly to the CPU, and have high-speed access.
- Four-bit bi-directional data bus and four-bit address bus
- The oscillation circuit is driven by rated voltage, giving excellent oscillation frequency stability for power supply voltage fluctuation (within ±1 ppm)
- Built-in timer clock
- Regular period interrupts and alarm match interrupts to the CPU
- Interrupt flag and interrupt inhibit
- Time (hour, minute, and second), calendar (leap year, ordinary year, month, day, and day of week), and alarm (hour and minute) functions.
- Choice of 12-hour or 24-hour time
- Automatic recognition of leap year
- All watch and alarm data expressed in BCD code
- ±30 second adjustment
- Automatic discrimination between valid and invalid clock data
- CMOS gives low power consumption, allowing battery backup
- Single 5V power supply
- 18-pin DIP (RP5C62) or 18-pin SOP (RF5C62) packaging

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Symbol	Name	Function
$\overline{CS}$ CE	Chip select Chip enable input	$\overline{CS}$ and CE are used when interfacing external devices. They may be accessed when $\overline{CS}$ is low and CE is high. CE is connected to a power down detector on the system power supply side, and $\overline{CS}$ is connected to the microcomputer address bus.
$\overline{TMOUT}$	Timer output	Timer output may be used as an interrupt free-run timer or watchdog timer. When CE is low (running on battery backup), operation stops (there is no output). It is N-ch open drain output.
A0 ~ A3	Address input	Address input is connected to the CPU address bus. It is gated internally with CE.
$\overline{RD}$	Read control input	When RD is set low, the contents of the counters or registers specified by A0~A3 are output to D0~D3. It is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
$\overline{WR}$	Write control input	When WR is low or rises from low to high, the contents of D0~D3 are written to registers or counters specified by A0~A3. WR is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
D0~D3	Bi-directional data bus	D0~D3 are connected to the CPU data bus. The input section is gated internally with CE. It is CMOS input/output.
$\overline{INTR}$	Interrupt output	INTR outputs regular alarm interrupts or alarm match interrupts to CPU. It also operates when CE is low (at battery backup). It is N-ch open drain output.
OSCIN OSCOUT	Oscillator circuit input/output	Crystal oscillator of 32.768 KHz must be connected between OSCIN and OSCOUT. Capacitance is connected externally between VDD and OSCIN and VDD and OSCOUT, forming the oscillator circuit.
VDD VSS	Power supply	VDD connects to +5V and VSS to ground.

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
VDD	Supply Voltage	VSS=0	−0.3 ~ +7.0	V
VI	Input Voltage		−0.3 ~ VDD+0.3	V
VO	Output Voltage		−0.3 ~ VDD+0.3	V
PD	Maximum Power Consumption	TA = 25°C	300	mW
TA	Operating Temperature		−20 ~ +70	°C
TSTG	Storage Temperature		−40 ~ +125	°C

■ RECOMMENDED OPERATING CONDITION

(VSS = 0V, TA = −20 ~ +70°C)

Symbol	Parameter	Condition	MIN.	Typ.	MAX.	Unit
VDD	Supply Voltage		4.0	5.0	6.0	V
VCLK	Supply Voltage of Clock		2.0		6.0	V
fXT	Crystal Oscillation Frequency			32.768		kHz

■ DC CHARACTERISTICS

Symbol	Parameter	Pin Name	Condition		MIN.	Typ.	MAX.	Unit
VIH1	"H" input voltage	A0~A3, D0~D3			2.0		VDD+0.3	V
VIL1	"L" input voltage	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$			−0.3		0.8	V
VIH2	"H" input voltage	CE			0.8*VDD		VDD+0.3	V
VIL2	"L" input voltage				−0.3		0.2*VDD	V
VOH1	"H" output voltage	D0~D3	IOH1 = −400μA		2.4			V
VOL1	"L" output voltage		IOL1 = 2mA				0.4	V
VOL2	"L" output voltage	$\overline{INTR}$, $\overline{TMOUT}$	IOL2 = 2mA				0.4	V
IILK	Input leak current	A0~A3, CE, CS, RD, WR	VILK = VDD or VSS		−1		1	μA
IOZ1	Output off leak current	D0~D3	VOZ1 = VDD or VSS		−5		5	μA
IOZ2		$\overline{INTR}$, $\overline{TMOUT}$	VOZ2 = VDD		−2		2	μA
IDD1	Consumption current for back-up	VDD	VDD=2.5V	Input: VDD or VSS			3	μA
IDD2	Consumption current for stand-by	VDD	VDD=5.5V	Output: OPEN			8	μA
∂f	Oscillation frequency drift for voltage drift	OSCIN OSCOUT	VDD=2.5~5.5V		−1		1	PPM

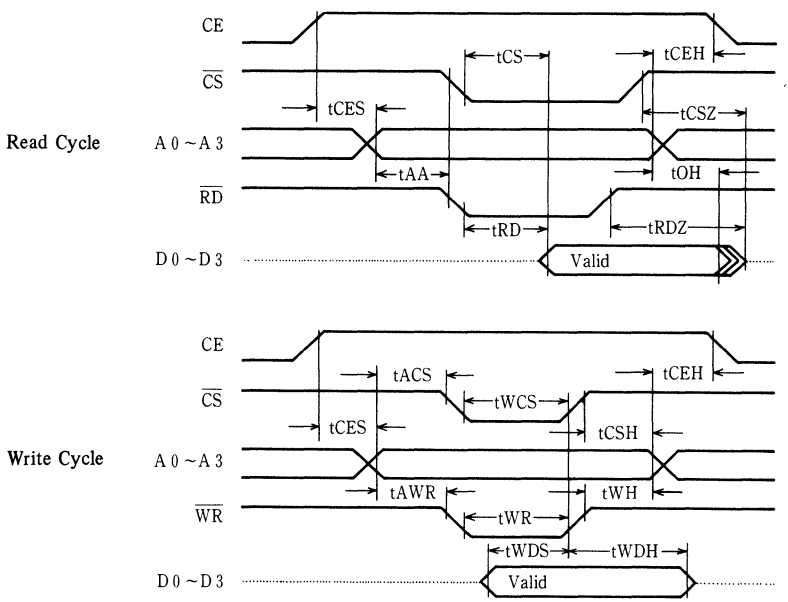
(Unless Noted, VSS=0V, VDD=5V±10%, TA=−20 ~ +70°C, X'tal=32.768KHz(CI≦35KΩ), CG=CD=33pF)

■ AC CHARACTERISTICS

(VSS=OV, VDD=5V±10%, TA=−20~+70°C)

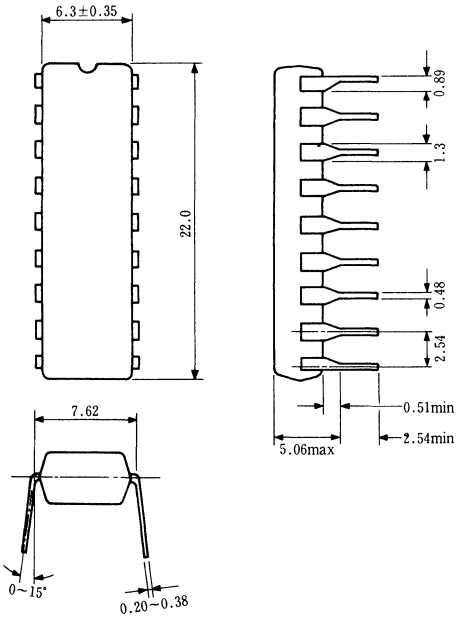
Symbol	Parameter	Description	Value	Unit
tCES	CE setup time	Time that CE must be held high before the address is established	MIN 200	nS
tCEH	CE hold time	Time that CE must be held high until the address changes	MIN 200	nS
tAA	Address setup time (RD)	Time when the address must be established before $\overline{CS}$ = $\overline{RD}$ = low	MIN 50	nS
tCS	$\overline{CS}$ setup time (RD)	Time taken from when $\overline{CS}$ becomes low to when data is output when $\overline{RD}$ is low after the address is established	MAX 120	nS
tRD	$\overline{RD}$ setup time (RD)	Time taken from when $\overline{RD}$ becomes low to when data is output when $\overline{CS}$ is low after the address is established	MAX 120	nS
tOH	Data hold time (RD)	Time when data does not change even though the address changes when $\overline{CS}$ = $\overline{RD}$ = L	MIN 10	nS
tCSZ	$\overline{CS}$ output delay time (RD)	Time taken for the data bus line to become high impedance after $\overline{CS}$ becomes high	MAX 70	nS
tRDZ	$\overline{RD}$ output delay time (RD)	Time taken for the data bus line to become high impedance after $\overline{RD}$ becomes high	MAX 70	nS
tACS	$\overline{CS}$ setup time (WR)	Time when the address must be established before $\overline{CS}$ becomes low when $\overline{WR}$ is low	MIN 50	nS
tAWR	$\overline{WR}$ setup time (WR)	Time when the address must be established before $\overline{WR}$ becomes low when $\overline{CS}$ is low	MIN 50	nS
tWCS	$\overline{CS}$ pulse width (WR)	Pulse width at write by $\overline{CS}$ when $\overline{WR}$ is low	MIN 120	nS
tWR	$\overline{WR}$ pulse width (WR)	Pulse width at write by $\overline{WR}$ when $\overline{CS}$ is low	MIN 120	nS
tWDS	Data setup time (WR)	Time that data must be established before $\overline{CS}$ or $\overline{RD}$ becomes high	MIN 60	nS
tCSH	Address $\overline{CS}$ hold time (WR)	Time that the address must be held after $\overline{CS}$ becomes high	MIN 10	nS
tWH	Address $\overline{WR}$ hold time (WR)	Time that the address must be held after $\overline{WR}$ becomes high	MIN 10	nS
tWDH	Data hold time (WR)	Time that data must be held after $\overline{CS}$ or $\overline{WR}$ becomes high	MIN 10	nS

■ TIMING DIAGRAM

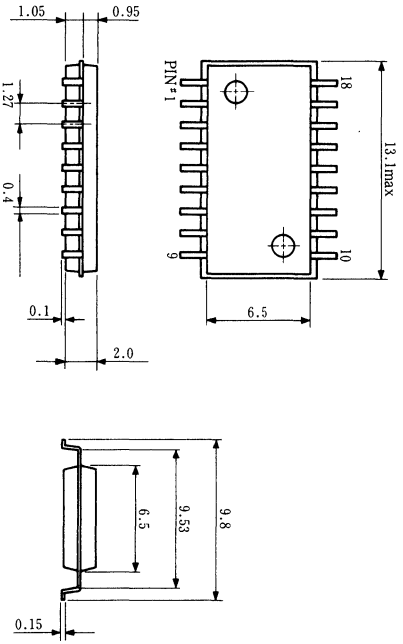


■ PACKAGE DIMENSIONS (Unit : mm)

1) RP5C62



2) RF5C62



QUAD.UART
RF5C59

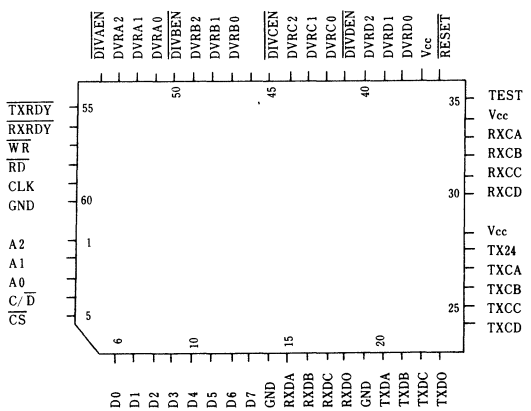
■ GENERAL DESCRIPTION

RF5C59 is the CMOS LSI with 4 channels of serial port built-in for application to asynchronous communication. The operations including transfer rate, transmit/receive of communication and etc. can be specified by program independently for each channel and it allows the use as peripheral circuit of CPU.

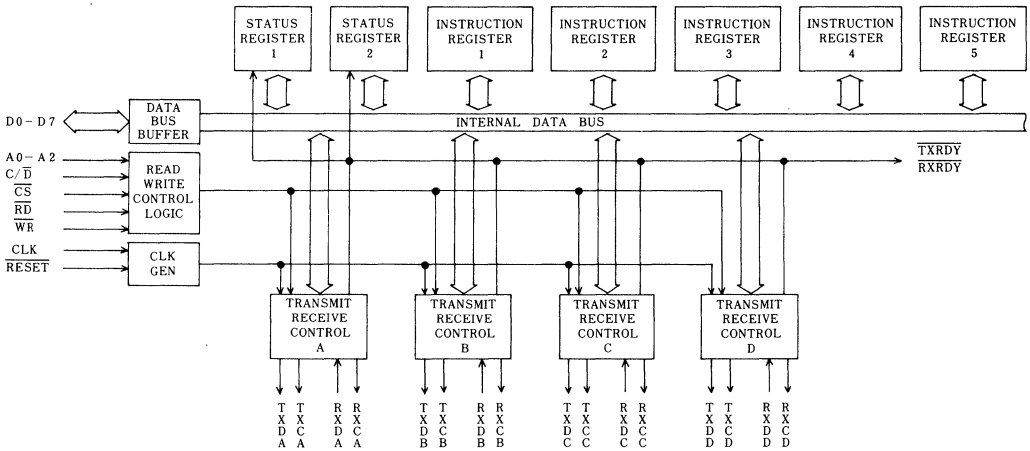
■ FEATURES

- Double-buffer mode transmitter/receiver
- Dual transmit/receive of communication is practicable for all 4 channels.
- Setting of transfer rate at each channel for both hardware and software is practicable.
  When input clock is 14.7456 MHz, the following rates are applicable.
  614.4 KHz, 307.2 KHz, 153.6 KHz, 76.8 KHz, 38.4 KHz, 19.2 KHz, 9.6 KHz and 4.8 KHz.
- Freedom of combination of logical address with physical address for 4 channels.
- Data length 8 bit, stop bit 1 bit fixed.
- Overrun and framing error are detectable.
- Error start bit is detectable.
- Direct connection to 8 bit bidirectional data bus and data bus is practicable.
- 4 bit address input.
- Hardware interrupt signal of $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ that can be masked.
- Connection to high speed CPU is practicable.
- 5V single voltage supply.
- 60 pin flat package.

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ DESCRIPTION OF FUNCTION

RF5C59, which is the UART for data communication, is used as peripheral circuit of CPU, and operation under serial data transfer mode can be specified with program.

RF5C59 has the transmit/receive ports with 4 channels, which receive parallel data from CPU, convert them into serial data and feed them out from TXD * terminal. In addition, RF5C59 receives data fed to RDX * terminal and feed them to CPU.

All 4 channels are controllable independently. Reading of status register 1 will not only make it possible to find the condition of transmit/receive operation but also allow to notify CPU of hardware interrupt signal from $\overline{\text{TXRDY}}$ terminal and $\overline{\text{RXRDY}}$ terminal.

The combination of logical port with physical port can be freely set with instruction register 3. In other words, logical ports in plural number can be assigned to one physical port. The transfer rate is 1/(24 * n) of input clock. (n : 1, 2, 4, 8, 16, 32, 64, 128)

■ PIN DESCRIPTION

PIN No.	Symbol	I/O	Function
6,7,8,9 10, 11 12, 13	D0 ~ D7	I	Bidirectional 3 state data bus used for transfer of command, data and status between RF5C59 and CPU. TTL compatible input.
36	$\overline{RESET}$	I	Reset input. Active LOW. During reset, • All internal registers turn to reset or default value. • Transmit outputs TXDA and TXDD turn to mark (HIGH) condition. • All transmit/receive ports are enabled. • $\overline{TXRDY}$ and $\overline{RXRDY}$ lines turn to active. (CMOS compatible Schumit input)
5	$\overline{CS}$	I	Chip select input. Active LOW. When $\overline{CS}$ is at LOW level, it allows data transfer with CPU. TTL compatible.
57	$\overline{WR}$	I	$\overline{WR}$ input. When $\overline{WR}$ is LOW and $\overline{CS}$ is LOW, the data on D0~D7 are written in this LSI. TTL compatible.
58	$\overline{RD}$	I	$\overline{RD}$ input. When $\overline{RD}$ is LOW and $\overline{CS}$ is LOW, the content of internal register of specified address is read on D0~D7. TTL compatible.
4	C/$\overline{D}$	I	C/$\overline{D}$ represents the input which informs whether the data on the bus is control information or status information. TTL compatible.
1,2,3	A2, A1 A0	I	Address input. TTL compatible.
56	$\overline{RXRDY}$	O	Interrupt signal to CPU which informs the receipt of data. If the data exist in any one of the receive ports being unmasked by RIM* flag of instruction register 1, it turns to LOW. When the data are read from all unmasked receive ports and each receive buffer has the space, it turns to HIGH. When RIM* flags are all turned to 1, it also turns to HIGH. Meanwhile, aparting from this signal, CPU is also able to confirm the existence of receive data by reading $\overline{RXRDY}$ bit of status register.
59	CLK	I	System clock input. CMOS compatible.
20 21 22 23	TXDA TXDB TXDC TXDD	O O O O	Transmit receive section of channel A~D serial data output. Following the start bit, it is output from LSB and after MSB, 1 bit of stop bits is added. During disable of port or during idle, it holds the "MARK" condition. With 'Mark' at HIGH level and 'Space' at LOW level, it performs Enable/Disable of coordinate ports with bit 7 and bit 3 of instruction register 4 and 5.
15 16 17 18	RXDA RXDB RXDC RXDD	I I I I	Receive section of channel A~D serial data input. Receive from LSB. 'Mark' is HIGH and 'Space' is LOW. It performs Enable/Disable of coordinate ports with bit 7 and bit 3 of instruction register 4 and 5.
29 34, 37	Vcc Vcc		+5V power supply. Make sure 29 Pin is connected with power supply.
14 19, 60	GND GND		
55	$\overline{TXRDY}$	O	Interrupt signal to CPU which informs that the data are transmissible. If any one of the transmit ports unmasked by TIM* flag of instruction register 1 is in transmissible condition, LOW output. (NOR output of TXRDY flag of each port) When TXRDY flags of all ports are masked, it turns to HIGH. Meanwhile, aparting from this signal, CPU is also able to confirm the condition of transmit register buffer by reading TXRDY* flag of status register 1.
28	TX 24	O	1/24 frequency division output of CLK input.
54 53 52 51 50 49 48 47 45 44 43 42 41 40 39 38	$\overline{DIVAEN}$ DVRA2 DVRA1 DVRA0 $\overline{DIVBEN}$ DVRB2 DVRB1 DVRB0 $\overline{DIVCEN}$ DVRC2 DVRC1 DVRC0 $\overline{DIVDEN}$ DVRD2 DVRD1 DVRD0	I I I I I I I I I I I I I I I I	Preset input by hardware of transfer rate. When $\overline{DIV*EN}$ is LOW, transfer rate of coordinate port is decided by input condition of DVR*2, DVR*1 and DVR*0. When $\overline{DIV*EN}$ is HIGH, transfer rate is decided by the data written in instruction register 4 and 5. All pull-up Schumit input. When CLK input is 14.7454 MHz, the transmit rates are: DVR*2 / DVR*1 / DVR*0 / Frequency division ratio (vs. CLK/24) / Transmit rate L / L / L / 1 / 614.4 KHz L / L / H / 1/2 / 307.2 L / H / L / 1/4 / 153.6 L / H / H / 1/8 / 76.8 H / L / L / 1/16 / 38.4 H / L / H / 1/32 / 19.2 H / H / L / 1/64 / 9.6 H / H / H / 1/128 / 4.8
27 26 25 24	TXCA TXCB TXCC TXCD	O O O O	Transfer clock output during transmit of each port. Transmit data are output in synchronizing with the rise of this clock.
33 32 31 30	RXCA RXCB RXCC RXCD	O O O O	Transfer clock output during receive of each port. Frame synchronization is taken in synchronizing with the rise of start bit.
35	TEST	I	It turns to test mode at HIGH active. 1/24 frequency division circuit of CLK is bypassed under the test mode. Normally, it is kept LOW.

■ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Test condition	Value	Unit
V_{CC}	Supply voltage	GND = 0V	−0.3 ~ 7	V
V_I	Input voltage		−0.3 ~ Vcc +0.3	V
V_O	Output voltage		−0.3 ~ Vcc +0.3	V
Pd	Power consumption		200	mW
Topg	Operating ambient temperature		0 ~ 70	℃
Tstg	Storage ambient temperature		−40 ~ 125	℃

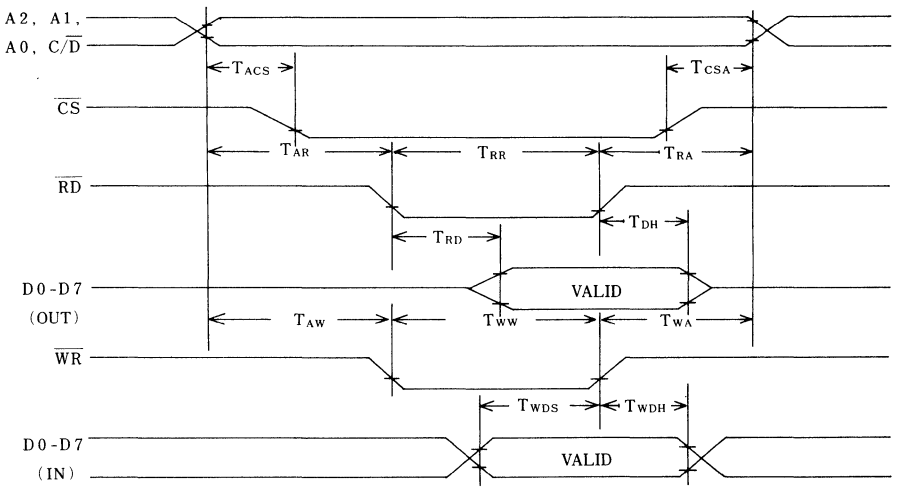
■ DC CHARACTERISTICS (Ta = 0 ~ 70℃, Vcc = 5 V ± 10%)

Symbol	Parameter	Test condition	Value			Unit
			MIN.	TYP.	MAX.	
V_{IH}	"H" input voltage (TTL)		2.2		Vcc +0.3	V
V_{IL}	"L" input voltage (TTL)		−0.3		0.8	V
V_{IH2}	"H" input voltage (CMOS)		Vcc × 0.7		Vcc +0.3	V
V_{IL2}	"L" input voltage (CMOS)		−0.3		Vcc × 0.3	V
V_{OH}	"H" output voltage	I_{OH} = −4mA	2.4			V
V_{OL}	"L" output voltage	I_{OL} = 4mA			0.4	V
I_{LI}	Input leakage current	0 ≦ VI ≦ Vcc			±10	μA
I_{LO}	Output leakage current	0 ≦ VO ≦ Vcc			±10	μA
V_{T+}	Input rise threshold voltage				3.8	V
V_{T-}	Input fall threshold voltage		1.3			V
I_{CC}	Supply current				20	mA

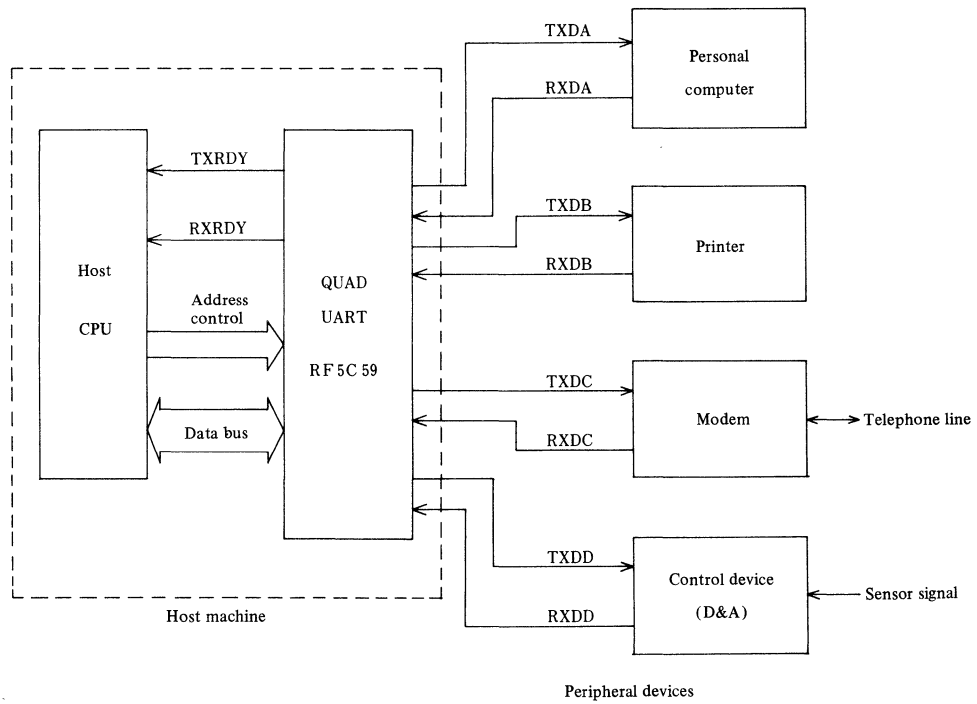
■ AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Value			Unit
			MIN	TYP.	MAX.	
Tww	$\overline{WR}$ pulse width		200			ns
Twds	$\overline{WR}$ data setup time		60			ns
Twdh	$\overline{WR}$ data hold time		45			ns
Taw	$\overline{WR}$ before rise ~ address setup time		50			ns
Twa	$\overline{WR}$ after rise ~ address hold time		80			ns
Tacs	$\overline{CS}$ after fall ~ address setup time		0			ns
Tcsa	$\overline{CS}$ before rise ~ address hold time		0			ns
Trr	$\overline{RD}$ pulse width		200			ns
Trd	$\overline{RD}$ data delay time	CL = 100pF			105	ns
Tdh	$\overline{RD}$ data hold time		10			ns
Tar	$\overline{RD}$ before rise ~ address setup time		50			ns
Tra	$\overline{RD}$ after rise ~ address hold time		80			ns

■ TIME CHART



■ EXAMPLE OF APPLICATION



■ REGISTER MAP

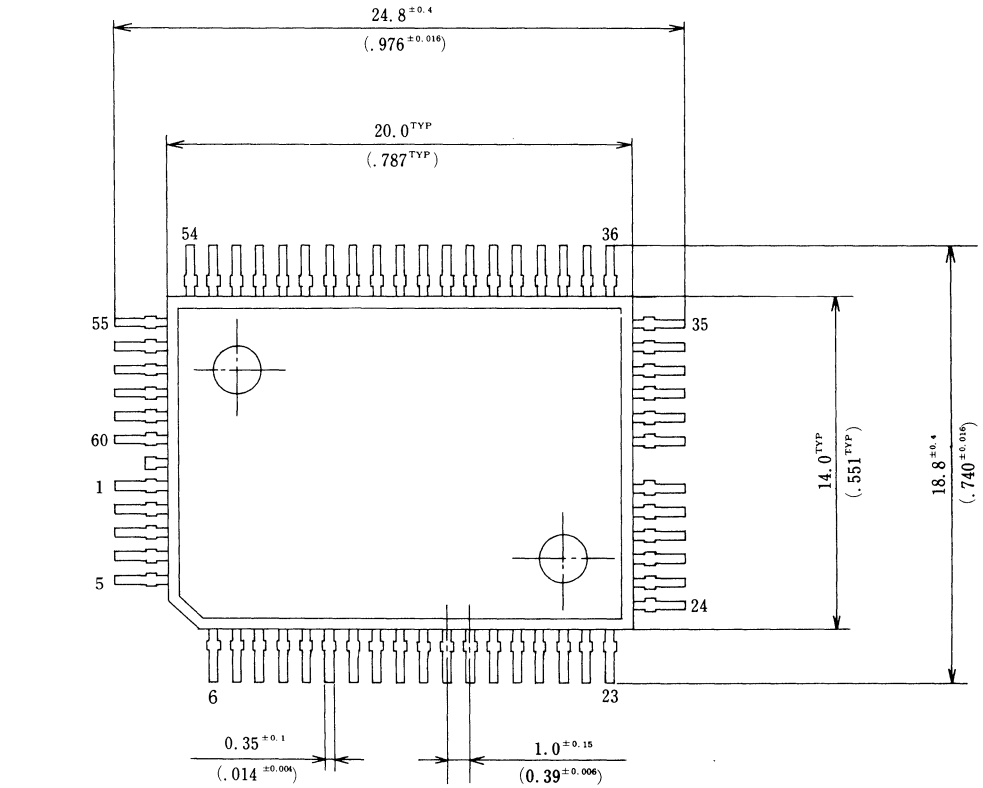
register	b7	b6	b5	b4	b3	b2	b1	b0
instr. 1	RIMA	RIMB	RIMC	RIMD	TIMA	TIMB	TIMC	TIMD
	L. P. A	L. P. B	L. P. C	L. P. D	L. P. A	L. P. B	L. P. C	L. P. D
	0 : non mask 1 : mask							
instr. 2	INIRER				ERSTA	ERSTB	ERSTC	ERSTD
	0 : NOP 1 : Initial Reset				0 : NOP 1 : Error Flag Reset			
instr. 3	LPAb1	LPAb0	LPBb1	LPBb0	LPCb1	LPCb0	LPDb1	LPDb0
	11 : physical port A 10 : physical port B 01 : physical port C 00 : physical port D							
instr. 4	ENLPA	ADIV2	ADIV1	ADIV0	ENLPB	BDIV2	BDIV1	BDIV0
	L. P. A	physical port A			L. P. B	physical port B		
	0 : DIS 1 : ENA	note 1			0 : DIS 1 : ENA	note 1		
instr. 5	ENLPC	CDIV2	CDIV1	CDIV0	ENLPD	DDIV2	DDIV1	DDIV0
	0 : DIS 1 : ENA	note 1			0 : DIS 1 : ENA	note 1		
stat. 1	RXRDYA	RXRDYB	RXRDYC	RXRDYD	TXRDYA	TXRDYB	TXRDYC	TXRDXD
	L. P. A	L. P. B	L. P. C	L. P. D	L. P. A	L. P. B	L. P. C	L. P. D
	0 : no receive data 1 : receive data in buffer				0 : transmit busy 1 : transmit ready			
stat. 2	FREA	FREB	FREC	FRED	OVEA	OVEB	OVED	OVEE
	L. P. A	L. P. B	L. P. C	L. P. D	L. P. A	L. P. B	L. P. C	L. P. D
	0 : no error 1 : framing error				0 : no error 1 : over run error			

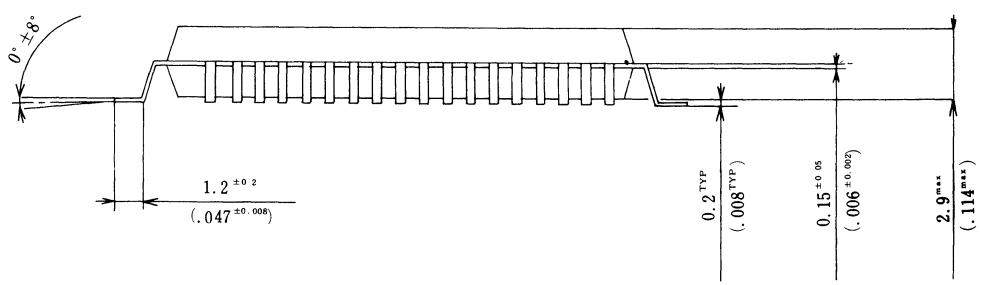
L. P. * : Logical Port *
note 1 : 000 : 1/1, 001 : 1/2, 010 : 1/4, 011 : 1/8, 100 : 1/16, 101 : 1/32, 110 : 1/64, 111 : 1/128

■ ADDRESS ASSIGNMENT OF REGISTER

C/D	A 2	A 1	A 0	write register	read register
L	L	L	L	TXDA (Logical port)	RXDA (Logical port)
L	L	L	H	TXDB (Logical port)	RXDB (Logical port)
L	L	H	L	TXDC (Logical port)	RXDC (Logical port)
L	L	H	H	TXDD (Logical port)	RXDD (Logical port)
H	L	L	L	instruction register 1	instruction register 1
H	L	L	H	instruction register 2	instruction register 2
H	L	H	L	instruction register 3	instruction register 3
H	L	H	H	instruction register 4	instruction register 4
H	H	L	L	instruction register 5	instruction register 5
H	H	L	H		status register 1
H	H	H	L		status register 2

■ PACKAGE DIMENSIONS (60 pin FLAT)





RF5C16A/RP5C16

CRT CONTROLLER

■ General description

RP5C16/RF5C16A are LSI developed under CMOS process technology for application to CRT controller. They allow to display the various patterns on the CRT by control commands and image data fed from 8 bit CPU including 8085, Z80, etc. With use of this 5C16, CRT controller system can be configurated by merely connecting DRAM.

Note)

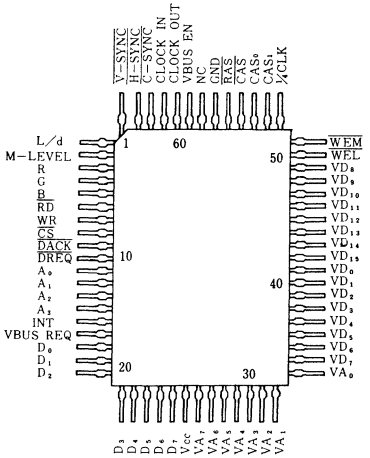
RF5C16A is the 64 pin FLAT packaged product.
RP5C16 is the 64 pin DIL packaged product.

■ Features

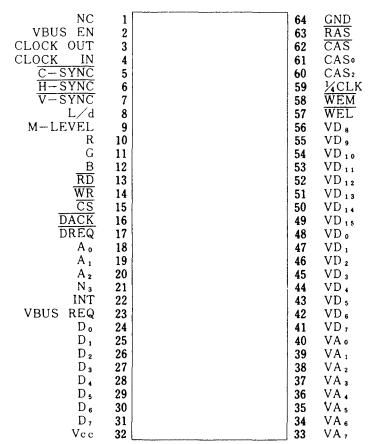
- 4 modes
  - ·Color picture with 80 X 25 characters
  - ·Color picture with 640 X 200 dots
  - ·2 color pictures with 40 X 25 characters and 40 X 25 characters
  - ·2 color pictures with 320 X 200 dots and 40 X 25 characters
- Display of maximum 15 colors with RGB output (2 values or 3 values)
- Virtual screen
- Smooth scroll to horizontal and vertical directions are practicable.
- Abundant attribute function (transverse invert, longitudinal invert, vertical invert and black white invert)
- Cursor built-in (for mouse)
- Master/Slave mode (Superimpose practicable)
- Redefinable character set
- Buffer register and address counter built-in for updating of V-RAM (Video RAM)
- Low power consumption for the sake of CMOS process
- 60 Hz non-interlace display

■ Pin configuration

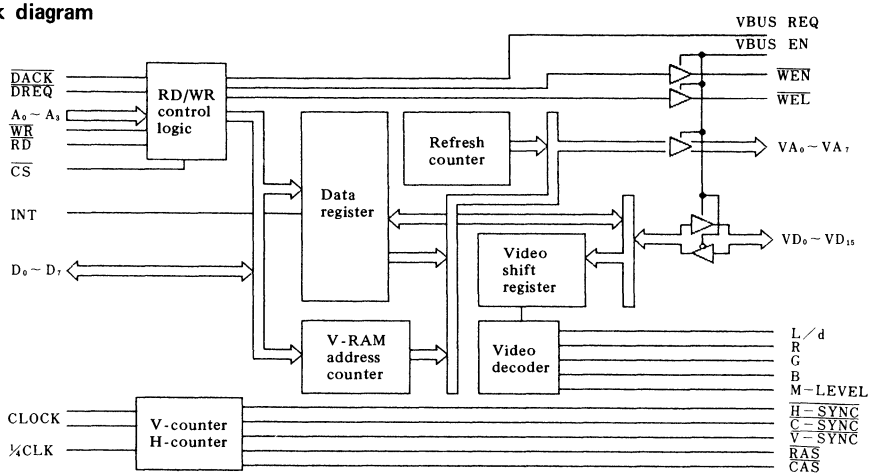
RF5C16A



RP5C16



■ Block diagram



■ Pin description

(1) CPU interface

Symbol	Name	Input/output	Logic	Function
$\overline{CS}$	Chip Select	IN	Active L	Make it possible to Read and Write of control register, address register and buffer register
$\overline{RD}$	Read Strobe	IN	L	
$\overline{WR}$	Write Strobe	IN	L	
$A_0 \sim A_3$	Address 0 ~ Address 3	IN	(positive)	Selective line of control register
$D_0 \sim D_7$	Data 0 ~ Data 7	IN/OUT	(positive)	Data bus Data 0 = LSB Data 7 = MSB
INT	Interrupt	OUT	Active H	
$\overline{DREQ}$	DMA Request	OUT	L	
$\overline{DACK}$	DMA Acknowledge	IN	L	

(2) V–RAM interface

Symbol	Name	Input/output	Logic	Function
$\overline{RAS}$	ROW Address Strobe	OUT	Active L	Set Row Address, Provide Timing
$\overline{CAS}$	Column Address Strobe	OUT	L	Set Column Address, Provide Timing
$\overline{CAS_0}$	Column Address Strobe 0	OUT	L	$\overline{CAS}$ which turns to active only when address is 0 ~ 3 FFFH.
$\overline{CAS_1}$	Column Address Strobe 1	OUT	L	$\overline{CAS}$ which turns to active only when active is 4000H ~ 7 FFFH.
VBUS EN	VIDEO BUS ENABLE	IN	H	When L, it turns $\overline{CAS}$, $\overline{CAS_0}$, $\overline{CAS_1}$, $\overline{RAS}$, $\overline{WEL}$, $\overline{WEM}$, $VA_{0\sim7}$ and $VD_{0\sim15}$ to Hi-Z.
VBUS REQ	VIDEO BUS REQUEST	OUT	H	5C16 accesses VBUS, it turns to active before 4 clock.
$\overline{WEM}$	Write Enable MSB	OUT	L	Write is early write operation
$\overline{WEL}$	Write Enable LSB	OUT	L	Write is early write operation
$VA_0 \sim VA_7$	Video Memory Address 0 ~ 7	OUT	(positive)	
$VD_0 \sim VD_{15}$	Video Memory Data 0 ~ 15	IN/OUT	(positive)	Data 0 = LSB Data 15 = MSB

(3) Clock and Video output

Symbol	Name	Input/output	Logic	Function
CLOCK IN CLOCK OUT	Clock In Clock Out			14.31818 MHz which connects quartz crystal.
M-LEVEL	Middle Level	IN		When RGB3 value output, it provides CRTC with intermediate level
Vcc, GND	Vcc, GND	–	–	
R, G, B L/d	Red, Green, Blue Light and dark	OUT	(positive)	Video output (2 values or 3 values)
$\overline{\text{C-SYNC}}$	Composite Synchronous	OUT/IN	(negative)	Output (open drain output) when master mode and input H-SYNC when slave mode
$\overline{\text{V-SYNC}}$	Vertical Synchronous	OUT/IN	(negative)	Output (open drain output) when master mode and input V-SYNC when slave mode
$\overline{\text{H-SYNC}}$	Horizontal Synchronous	OUT/IN	(negative)	Output (open drain output) when master mode and input H-SYNC when slave mode
¼ CLK	¼ CLOCK	OUT		Clock ¼ frequency division output

■ Absolute maximum rating

Symbol	Parameter	Condition	Value	Unit
Vcc	Supply voltage		−0.3 ~ +7.0	V
VI	Input voltage		−0.3 ~ +7.0	V
VO	Output voltage		−0.3 ~ +7.0	V
Pd	Maximum power consumption	Ta = 25°C	300	mW
Ta	Operating ambient temperature		−10 ~ 70	°C
Tstg	Storage temperature		−40 ~ 125	°C

■ Recommended operating condition

Symbol	Parameter	Condition	Value	Unit
Vcc	Supply voltage		4.5 ~ 5.5	V
Vss	Supply voltage		0	V
VIH	"H" input voltage		2.0 ~ Vcc + 0.3	V
VIL	"L" input voltage		−0.3 ~ 0.8	V
Ta	Ambient temperature		−10 ~ 70	°C

■ DC electrical characteristics (Vcc = 5.0V ± 10%, Ta = −10 ~ 70°C)

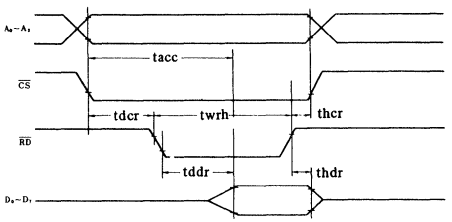
Symbol	Parameter	Condition	Value			Unit
			Min.	Typ.	Max.	
VIH	"H" input voltage		2.0		Vcc + 0.3	V
VIL	"L" input voltage		−0.3		0.8	V
VOH	"H" output voltage	IOH = −400 μA	2.4			V
VOL	"L" output voltage	IOL = 3.2 mA			0.4	V
ILI	Input leakage current	0 ≦ VI ≦ Vcc			10	μA
ILO	3-state floating current	0.4 ≦ VI ≦ 2.4			10	μA
Icc	Supply current				50	mA
VINφ	Clock input "H" input voltage		0.7 x Vcc			V
ViLφ	Clock input "L" input voltage				0.3 x Vcc	V

■ AC characteristics (Vcc = 5.0V ± 10%, Ta = −10~70°C). and Timing diagram (Unit : ns)

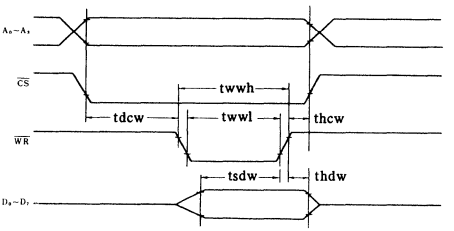
(1) CPU-5C16 READ/WRITE

No.	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
1	tacc	Access time from $\overline{CS}$, A_0~A_3 and $\overline{DACK}$			200	ns
2	tdcr	$\overline{RD}$ delay time from $\overline{CS}$, A_0~A_3 and $\overline{DACK}$	30			ns
3	twrh	$\overline{RD}$ pulse width (H-threshold)			10	ns
4	thcr	$\overline{CS}$, A_0~A_3 and $\overline{DACK}$ hold time during read	5			ns
5	tddr	Data delay time from $\overline{RD}$			120	ns
6	thdr	Data hold time during read	0		85	ns
7	tdcw	$\overline{WR}$ delay time from $\overline{CS}$, A_0~A_3 and $\overline{DACK}$	30			ns
8	twwh	$\overline{WR}$ pulse width (H-threshold)			10	ns
9	twwl	$\overline{WR}$ pulse width (L-threshold)	150			ns
10	thcw	$\overline{CS}$, A_0~A_3 and $\overline{DACK}$ hold time from $\overline{WR}$	10			ns
11	tsdw	Data setup time	150			ns
12	thdw	Data hold time during write	10			ns
13	tddgl	$\overline{DREQ}$ ↓ delay time from CLK OUT			90	ns
14	tddgh	$\overline{DREQ}$ ↑ delay time from CLK OUT			60	ns
15	tdinl 1	INT ↓ delay time from $\overline{RD}$ or $\overline{WR}$ (End of INT by Buffer Ready)			410	ns
16	tdinl 2	INT ↓ delay time from CLK OUT			120	ns
17	tdinh	INT ↑ delay time from CLK OUT			90	ns

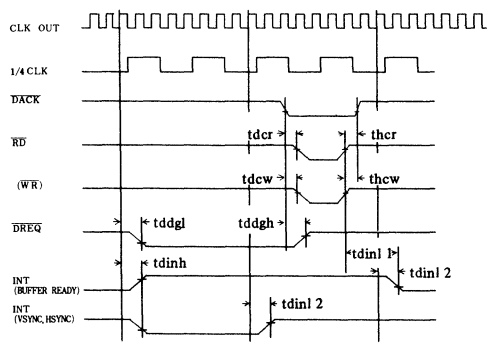
(1−1) CPU READ 5C16



(1−2) CPU WRITE IN 5C16



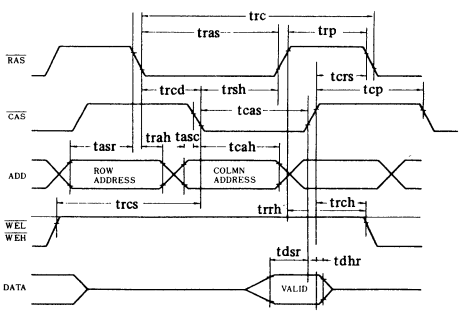
(1−3) INT, $\overline{DREQ}$, $\overline{DACK}$



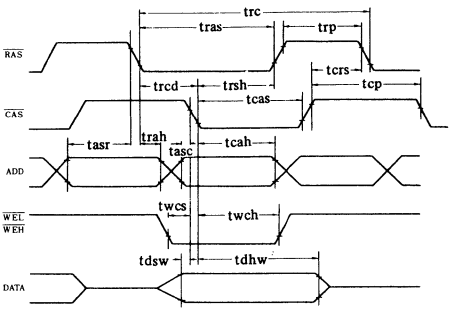
(2) 5C16-V-RAM READ/WRITE

No.	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
1	trc	Read cycle time		279		ns
2	tras	$\overline{RAS}$ pulse width	150			ns
3	trp	$\overline{RAS}$ pre-charge time	90			ns
4	trcd	$\overline{RAS}$-$\overline{CAS}$ delay time	40			ns
5	trsh	$\overline{RAS}$ hold time	80			ns
6	tcrs	$\overline{CAS}$-$\overline{RAS}$ setup time	0			ns
7	tcas	$\overline{CAS}$ pulse width	150			ns
8	tcp	$\overline{CAS}$ pre-charge time	60			ns
9	tasr	Line address setup time	0			ns
10	trah	Line address hold time	20			ns
11	tasc	Column address setup time	0			ns
12	tcah	Column address hold time ($\overline{CAS}$ reference)	40			ns
13	trcs	Read command setup time	0			ns
14	trch	Read command hold time ($\overline{CAS}$ reference)	0			ns
15	trrh	Read command hold time ($\overline{RAS}$ reference)	0			ns
16	tdsr	Data input setup time ($\overline{CAS}$ reference)	60			ns
17	tdhr	Data input hold time ($\overline{CAS}$ reference)	0			ns
18	twcs	Write command setup time	0			ns
19	twch	Write command hold time ($\overline{CAS}$ reference)	60			ns
20	tdsw	Data input setup time ($\overline{CAS}$ reference)	0			ns
21	tdhw	Data input hold time ($\overline{CAS}$ reference)	60			ns
22	tdvr	VBUS REQ delay time from CLK OUT			90	ns
23	thve	Hold time of VBUS EN against CLK OUT	40			ns
24	tsve	Setup time of VBUS against CLK OUT	0			ns
25	tdral	$\overline{RAS}$ ↓ delay time from CLK OUT			100	ns
26	tdraf	Delay time for $\overline{RAS}$ from CLK OUT to turn to floating	0		60	ns
27	tdwev	Delay time for $\overline{WEL}$ or $\overline{WEM}$ from CLK OUT to turn to valid			70	ns
28	tdwef	Delay time for $\overline{WEL}$ or $\overline{WEM}$ from CLK OUT to turn to floating	0		60	ns
29	tdcav	Delay time for $\overline{CAS}$, $\overline{CAS_0}$ and $\overline{CAS_1}$ from CLK OUT to turn from floating to valid			30	ns
30	tdcaf	Delay time for $\overline{CAS}$, $\overline{CAS_0}$ and $\overline{CAS_1}$ from CLK OUT to turn to floating	30		130	ns
31	tdvav	Delay time for $VA_{0\sim7}$ and $VD_{0\sim15}$ from CLK OUT to turn from floating to valid			70	ns
32	tdvaf	Delay time for $VA_{0\sim7}$ and $VD_{0\sim15}$ from CLK OUT to turn to floating	0		60	ns

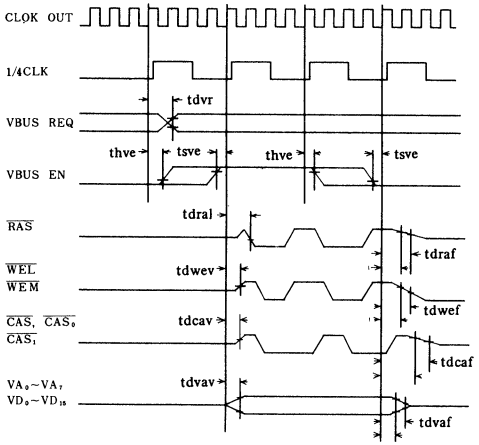
(2–1) 5C16 READ V-RAM



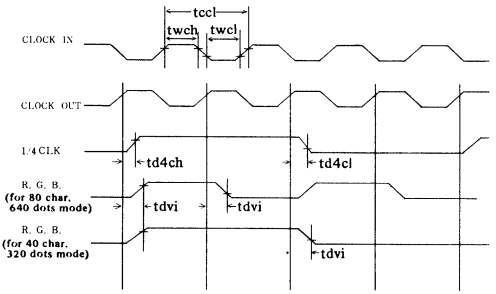
(2–2) 5C16 WRITE V-RAM



(2–3) VBUS REQ, VBUS EN



(3–1) CLK IK, CLK OUT



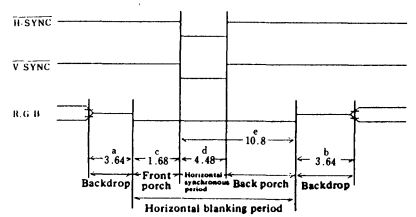
(3) CLK IN, CLK OUT

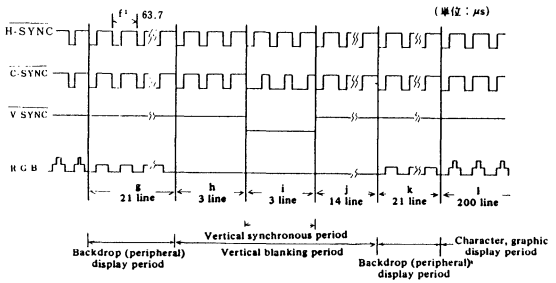
No.	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
1	tccl	Clock frequency	−300	14.318 18	+300	MHz ppm.
2	twch	Clock pulse width (H period)	32			ns
3	twcl	Clock pulse width (L period)	32			ns
4	td4ch	¼ CLK ↑ delay time from CLK OUT			60	ns
5	td4cl	¼ CLK ↓ delay time from CLK OUT			60	ns
6	tdvi	RGB dèlay time from CLK OUT			60	ns

(4) SYNC wave, R.G.B. output

No.	Symbol	Parameter	Value	Unit
7	a	Backdrop (peripheral) display period front porch side	3.64±0.50	μs
8	b	Backdrop (peripheral) display period back porch side	3.64±0.50	μs
9	c	Front porch	1.68±0.30	μs
10	d	Horizontal synchronous period	4.48±0.30	μs
11	e	Horizontal synchronous period + back porch	10.80±0.30	μs
12	f	Horizontal synchronous signal cycle	63.70±0.50	μs
13	g	Display period of backdrop (peripheral)	21	line
14	h	Blanking period before vertical synchronous period	3	line
15	i	Vertical synchronous period	3	line
16	j	Blanking period after vertical synchronous period	14	line
17	k	Display period of backdrop (peripheral)	21	line
18	l	Display period of character and graphic	200	line

(4–1) SYNC wave, R.G.B. output (Unit : μs)





■ Connectible CPU

8085	6MHz	8085AH-2	8085A-2
Z-80	6MHz	Z-80B	
6502	3MHz	65C02B	

16bitCPU

■ Usable memory

64 X 1bit, 16k X 4bit or 64k X 4bit
- Use Tacc (access time) of below 120 ns.
- Memory at maximum 128K byte is usable.

■ Table of control register

〈WR〉

Register No.	Data b7 b6 b5 b4 b3 b2 b1 b0	CONTENTS
0	TR-L	Transfer Register – L
1	TR-M	Transfer Register – M
2	Add-L	Transfer Address – L
3	Add-M	Transfer Address – M
4	MV MH MB DMA 1/2 byWR byRD ML/L	Transfer mode interrupt mask
5	MODE FG-on BG-on R-on M/S AH	Display mode
6	CsHL	Cursor coordinate HL
7	CsV	Cursor coordinate V
8	BCG-M X CsHm	Chara. Gen. Base Address M cursor coordinate CsHm
9	BFG-M × ×	Fore Ground Base Address M
A	BBG-L	Back Ground Base Address L
B	BBG-M	Back Ground Base Address M
C	CFG3 CFG2	FG 3rd color FG 2 color
D	CBG3 CBG2	BG 3rd color BG 2 color
E	CBD-p CBD-c	BD color (peripheral) BD color (center)
F	SL SV × SH	Dot Scroll V direction H direction

〈RD〉

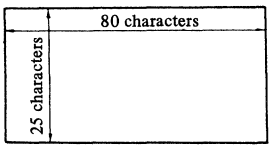
0	TR-L	Transfer Register – L
1	TR-M	Transfer Register – M
2	Add-L	Transfer Address – L
3	Add-M	Transfer Address – M
4	MV MH MB X FV FH FB X	Interrupt flag

■ Description of function

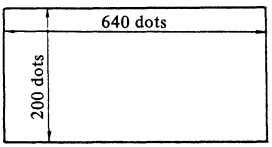
(1) Display mode

- Following 4 display modes are available.

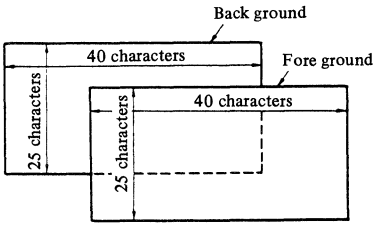
A. 80 character X 25 line character display mode (only back ground)



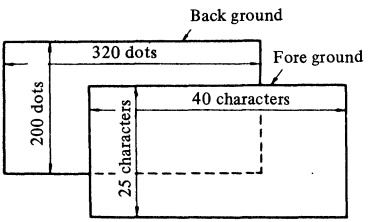
B. 640 X 200 dot graphic dispaly mode (only back ground)



C. 40 characters – 40 character display mode

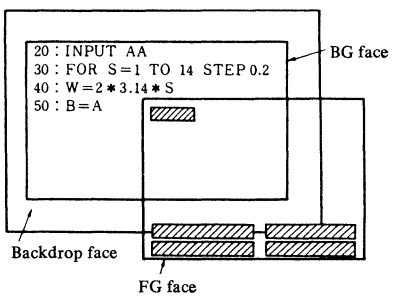


D. 40 character – 320 dot display



(2) Picture simultaneous display (display mode 3 and 4)

- 2 pictures of fore ground face and back ground face are simultaneously displayed.
- When overlapping of FG face pattern with BG face pattern, FG face is displayed.
- In case where there is neither pattern present on FG face nor on BG face, backdrop color (CBD-C) is displayed.
- As far as the distance ranging from the outside of display window to the edge of cathode ray tube, the color of backdrop face (CBD-P) is displayed. (Backdrop color is specified by register E)



(3) 15 color display

15 colors can be displayed.

Color code				Color	Color code				Color
L/d	B	G	R		L/d	B	G	R	
0	0	0	0	Black	1	0	0	0	Black
0	0	0	1	Red	1	0	0	1	Pink
0	0	1	0	Green	1	0	1	0	Light Green
0	0	1	1	Yellow	1	0	1	1	Light Yellow
0	1	0	0	Blue	1	1	0	0	Light Blue
0	1	0	1	Magenta	1	1	0	1	Light Magenta
0	1	1	0	Cyan	1	1	1	0	Light Cyan
0	1	1	1	Gray	1	1	1	1	White

(4) R, G, B output

- Following outputs are held as image signal. R, G, B, L/d, $\overline{\text{C-SYNC}}$, $\overline{\text{V-SYNC}}$ and $\overline{\text{H-SYNC}}$
- RGB terminal takes the following output levels at 3 value output.

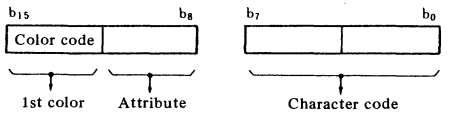
	Min.	Max.
High	4.4	Vcc
Middle	M-LEVEL−0.6	M-LEVEL+0.4
Low	—	0.4

Vcc = 5V, M-LEVEL = 2.5V, Io = ±1mA

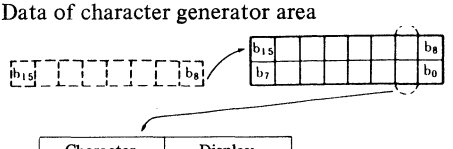
- $\overline{\text{V-SYNC}}$, $\overline{\text{C-SYNC}}$ and $\overline{\text{H-SYNC}}$ terminals turn to output terminal (open drain) under master mode and to input terminal under slave mode.
  (Refer "Terminal function (3) Clock and Video output")

(5) Character display

- The size of character at character display is 8 X 8 dots.
- Fonts are kept in memory area of 2K words from character generator base address (BCG-M). (Max. 256 kinds)
- Data of code area



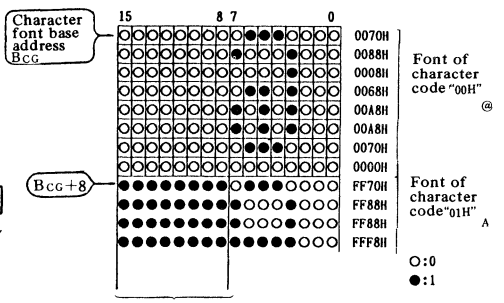
- Data of character generator area



Character generator value	Display color
00	Clear
01	1st color
10	2nd color
11	3rd color

2nd and 3rd colors are specified by control register (C, D).

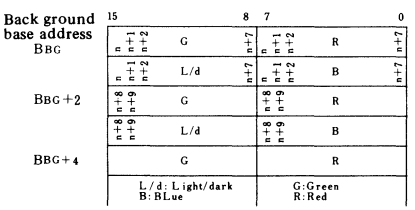
- Configuration of character font

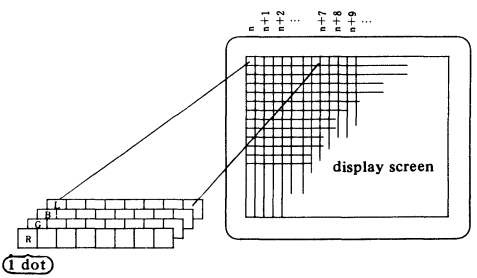


▶ When displaying MSByte in single color such as alphanumeric character, etc., all "0" or all "1" is used.
▶ When drawing the picture such as game, etc, 4 colors can be displayed at each dot with 2 bit of combination such as bit 15 with bit 7, bit 14 with bit 6 and so on.

(6) Graphic display

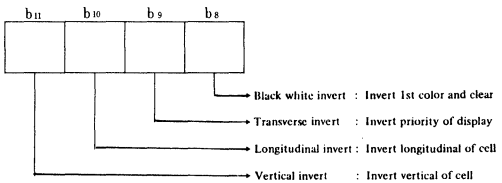
- 1 dot is consisted of 4 bits, and 8 dots are allocated as 1 block.
- Display color is decided by 4 face synthesis of R, G, B and L/d.

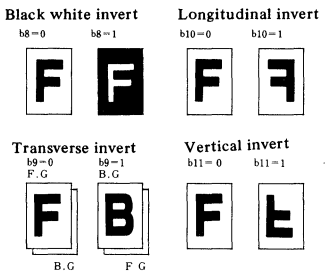




(7) Attribute (character display)

- 4 kinds of attribute can be decided with bit 8 ~ bit 11 of code area data.

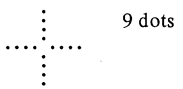




(8) Cursor

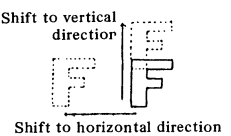
- Cross hair cursor is displayed. The coordinate of cursor in the horizontal direction is specified with 10 bits of cursor register CsHm and CsHL while in the vertical direction with 8 bits of CsV. 2 bits of cursor register CsHm will not become effective unless CsHL is written.

Shape of cursor



(9) Dot scroll (only back ground)

- It allows scroll of 0~7 dots in the horizontal and vertical directions. The number of shift to the horizontal and vertical directions is specified by respective dot scroll register SH and SV.



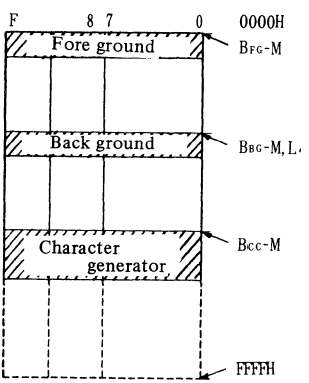
(10) Control of video memory area

- Base address

  BG base address (BBG-M, BBG-L) is consisted of 16 bits and allows to specify by 1 character unit. Therefore, the change of BG base address allows scroll in the column or line direction. BBG-M becomes effective when BBG-L is written. Those subsequent to this address area fall in code data of back ground. In case of graphic, too, data are stored here.

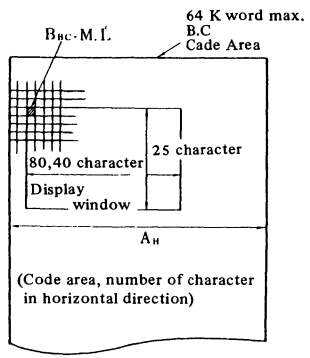
  FG base address (BFG-M) allows paging of each 1,024 characters with 6 bit. Subsequent to this address, code data of fore ground are stored in 1,000 words (40 character X 25 line).

  Character generator base address (BCG-M) is able to specify the start address of character font for each 2,048 words with 5 bit. Character font is consisted of 1 cell 8 words and is able to select 256 patterns. (Refer diagram) It will not be used for only graphic display.



- Width of code area (No. of character AH)

  FG is fixed with 40 characters. BG can be selected from 40 characters (320 dots), 64 characters (512 dots), 80 characters (640 dots) and 128 characters (1,024 dots). With this, the width of virtual screen is set.



(11) Updating function of frame buffer

- Since it has the transfer register and address counter, it allows read/write of frame buffer data, making use of retrace line section in horizontal/vertical direction without relying on externally mounted circuit.
- Write mode/read mode/read modify write mode (see diagram below)
- Word transfer/Byte transfer (see diagram below)

	Write mode		Read mode		Read modify write	
	Word transfer	Byte transfer	Word transfer	Byte transfer	Word transfer	Byte transfer
Read TR-M	–	–	–	Add+1-RT	–	–
Read TR-L	–	–	Add+1-RT	Add+1-RT	–	–
Write TR-M	–	WT-Add+1	–	WT	–	WT-Add+1 -RT
Write TR-L	WT-Add+1	WT-Add+1	WT	WT	WT-Add+1 -RT	WT-Add+1 -RT
Read Add-M	–	–	–	–	–	–
Read Add-L	–	–	–	–	–	–
Write Add-M	–	–	–	–	–	–
Write Add-L	–	–	RT	RT	RT	RT

TR : Transfer register
Add : Address counter
RT : Read transfer (frame buffer read)
WT : (frame buffer write)

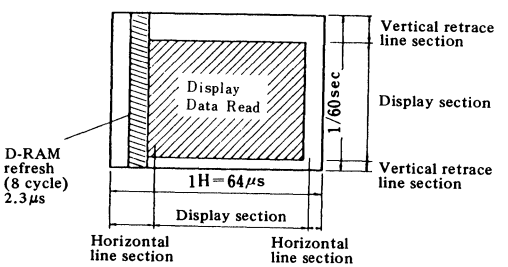
The relationship " – " between read/write operation of transfer register and read/write toward frame buffer represents the sequence of process. For example, when CPU side read TR-L register under (read mode), first of all, number of address counter is set as +1, then, perform read of frame buffer. " – " represents that no steps are being taken for frame buffer.

- The mode of increment +1/+2+2 of address counter is used in graphic display, for example, only the face of BLUE is rewritten in sequence.
- DMA transfer

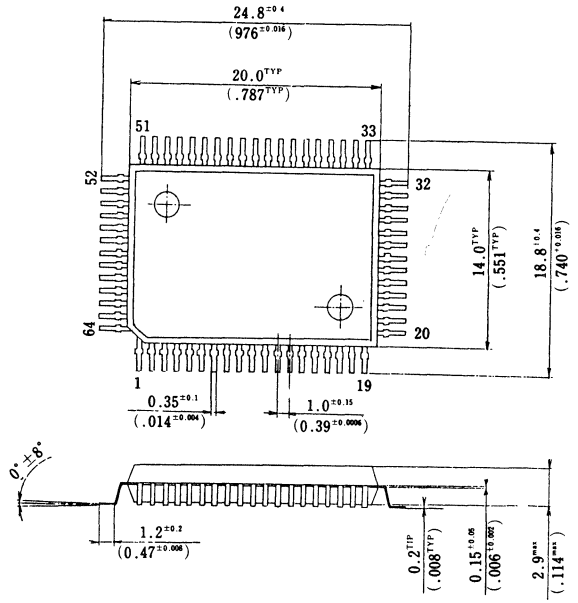
  In case of DMA transfer, it is necessary to set whether to read or write to LSB of transfer register, or to read or write to MSB. In case of word transfer, TR-L and TR-M vary at every 1 byte. In case of byte transfer, it is always written in the register that has been set.

(12) D-RAM refresh

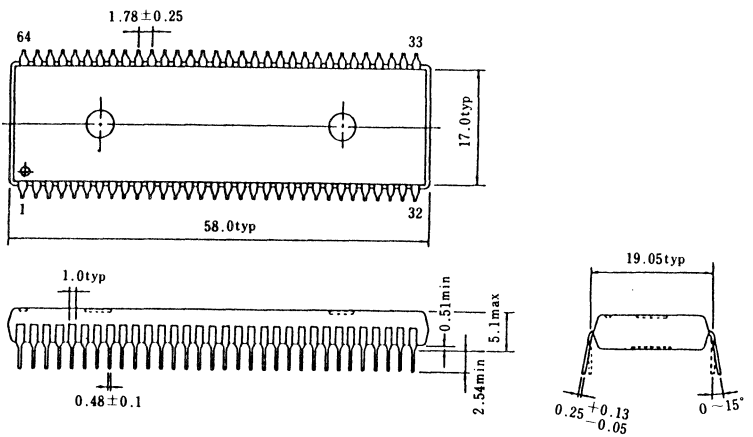
- 8 addresses per 1 H (64 μs) are refreshed within retrace line section.



■ 64 pin flat package dimension (Unit : mm)



■ 64pin DIL package dimension (Unit : mm)



VOLTAGE REGULATORS
RX5RA Series

■ OUTLINE

The RX5RA series, developed with C-MOS processing technology, are highly accurate, low-power-consumption, fixed three terminal voltage regulators. They include reference voltage supply, error amplifier, control transistor, and resistor network to control the output voltage. The output voltage is fixed in the IC.

The RX5RA series are both available in two different types of package : mini-power-mold and TO-92.

■ FEATURES

- Extremely low power consumption ..... TYP. 1.0μA Vout = 3.0V
- Small input-output voltage difference ..... TYP. 60mV Iout = 1.0mA
- Low temperature coefficient for output voltage ..... TYP. ±100PPM/°C
- Stable input rate ..... TYP. 0.1%/V
- Accurate output voltage ..... ±2.5%
- Variety of output voltage levels ..... 0.1V step
- Compact package ..... TO-92, mini power mold

■ APPLICATIONS

- Constant-voltage power supply for battery-powered devices
- Constant-voltage power supply for camera, communication, and video equipment
- Stable standard voltage supply

■ BLOCK DIAGRAMS

Type RX5RAXXXX
(positive-voltage regulator)

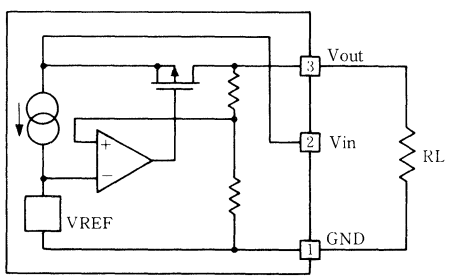


Figure 1

■ SELECTION GUIDE

You can define the output voltage and package of the RX5RA series.
The devices are defined by the following characters.

RX5RAXXXX ← Type number

↑ ↑ ↑↑

a b c d

No.	Meaning
a	Defines the packaging type E : TO-92 H : Mini power mold (SOT-89)
b	Defines output voltage (Vout) The range for Vout is 2.0V to 6.0V in units of 0.1V, with an accuracy of ±2.5%.
c	Defines the output current type A : Standard type
d	Defines the packaging method for shipment A-T1 : Taping-T1 type (See Fig. 2) A-T2 : Taping-T2 type (See Fig. 2) A-RF : Taping-RF type (See Fig. 2) A-RR : Taping-RR type (See Fig. 2) B : Gluing (Gluing is for mini power mold package as a sample) C : Electric conductive bagging (for TO-92)

Table 1

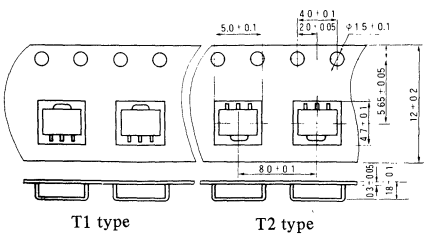
Example : positive-voltage regulator

Type numbers	output voltage(Vout)			Package	Packing method
	MIN.(V)	TYP.(V)	MAX.(V)		
RX5RA21AX	2.048	2.100	2.152	E:TO-92 H:Mini power mold	A:Taping B:Gluing C:Electric conductive bagging
RX5RA30AX	2.925	3.000	3.075		
RX5RA33AX	3.218	3.300	3.382		
RX5RA37AX	3.608	3.700	3.792		
RX5RA40AX	3.900	4.000	4.100		
RX5RA50AX	4.875	5.000	5.125		
RX5RA60AX	5.850	6.000	6.150		

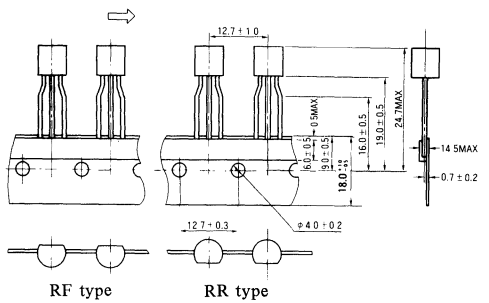
Table 2

* Following the selection guide, determine specification other than those shown in Table 2. Use the type number.

■ TAPING METHODS



mini-power-mold



TO-92

Figure 2

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage	Vin	+12	V
Output Current	Iout	150	mA
Output Voltage	Vout	Vin+0.3～−0.3	V
Power Dissipation	Pd	300	mW
Operating Temperature Range	Topr	−30～+80	℃
Storage Temperature Range	Tstg	−40～+125	
Soldering Temperature	Tsolder	260℃ 10Sec	

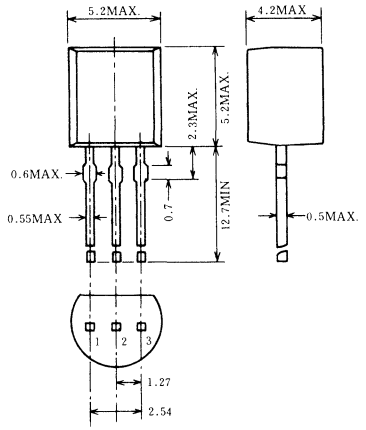
■ ELECTRICAL CHARACTERISTICS

Topr : 25℃

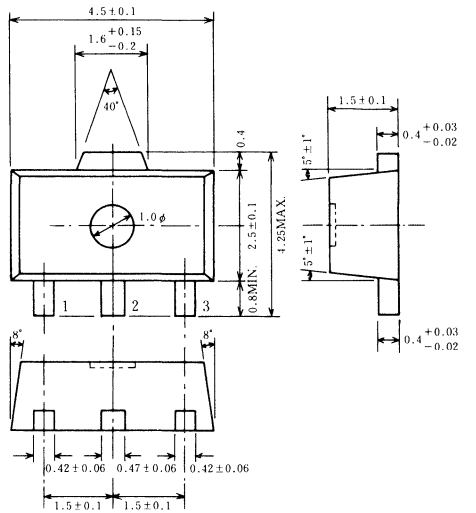
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vout	Iout=10mA	(Vout) ×0.975		(Vout) ×1.025	V
Output Current	Iout	Vin−Vout =2.0V Vout =3.0V Vout =5.0V		40 60		mA
Load Regulation	△Vout	Vin−Vout =2.0V Vout =3.0V 1mA≦Iout≦20mA Vout =5.0V 1mA≦Iout≦40mA		60 40		mV
Input-Output Voltage Difference	Vdif	Iout=1mA Vout =3.0V =5.0V		60 30		mV

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	Iss	Vin−Vout =2.0V Vout =3.0V =5.0V		1.1 1.3	3.3 3.9	μA
Line Regulation	$\frac{\triangle Vout}{Vout \cdot \triangle Vin}$	Iout=1mA Vout +0.5V≦ Vin ≦10V		0.1		%/V
Input Voltage	Vin				10	V
Temperature Coefficient	△Vout/△Topr	Iout=10mA −30℃≦Topr≦80℃		±100		PPM/℃

■ PACKAGE INFORMATION



TO-92



mini-power-mold

1	GND
2	Vin
3	Vout

VOLTAGE DETECTORS
RX5VA Series

■ OUTLINE

RX5VA series, developed with C-MOS processing technology, are accurate, low-power-consumption voltage detectors. The detectors include comparators, output drivers and hysteresis circuit.
The value of detect voltage is set internally, and is accurately controlled by Laser Trimming.
There are three types of output : N-ch open-drain, P-ch open-drain, and C-MOS. There are two convenient packages : mini-power-mold and TO-92. The RX5VA series can be used as a reference voltage supply for ICs in many applications.

■ FEATURES

- Extremely low power consumption ..... TYP. 1.0μA (VDD = 3.0V)
- Wide voltage range ..... 1.5V to 10.0V
- Variety of detect voltage ..... 0.1V step
- High accuracy ..... ±2.5%
- Good temperature characteristic for detect voltage ..... TYP. ±100 PPM/°C
- Output Options ..... N-ch open drain,
  P-ch open drain,
  CMOS
- Compact Package ..... TO-92, min-power-mold

■ APPLICATIONS

- Resets circuit of P-ch, N-ch, and C-MOS microcomputers
- Battery checker
- Logic circuit reset
- Level discriminator
- Waveform shaping circuit
- Switching circuit for battery backup
- Power failure detector

■ SELECTION GUIDE

You can define several options, including output driver type, package and packing method with the RX5VA series.

The devices are defined by the following characters.

R X 5 V A X X X X ← Type number

↑ ↑ ↑ ↑

a b c d

Character	Meaning
a	Defines the packaging type E : TO-92 H : Mini-power-mold
b	Defines the voltage value that is to be monitored (−VDET) The monitor range is 2.00V to 6.00V in 0.1V units, with an accuracy of ±2.5%.
c	Defines the output type A : N-ch open drain B : P-ch open drain C : C-MOS
d	Defines the packing method A-T1 : Taping-T1 type (See Fig. 1) A-T2 : Taping-T2 type (See Fig. 1) A-RF : Taping-RF type (See Fig. 1) A-RR : Taping-RR type (See Fig. 1) B : Gluing (Gluing is for mini power mold package as a sample) C : Electric conductive bagging (for TO-92)

Table 1

Example

Type number	Voltage Detect (−VDET)			Output Driver			Package	Packing method
	MIN.(V)	TYP.(V)	MAX.(V)	N-ch Open-Drain	P-ch Open-Drain	C-MOS		
RX5VA20AX	1.950	2.000	2.050	○			E:TO-92 H:Minipower mold (SOT-89)	A:Taping B:Gluing C:Electric Conductive bagging
RX5VA20BX					○			
RX5VA20CX						○		
RX5VA21AX	2.048	2.100	2.152	○				
RX5VA21BX					○			
RX5VA21CX						○		
RX5VA27AX	2.633	2.700	2.767	○				
RX5VA27BX					○			
RX5VA27CX						○		
RX5VA45AX	4.388	4.500	4.612	○				
RX5VA45BX					○			
RX5VA45CX						○		
RX5VA47AX	4.583	4.700	4.817	○				
RX5VA47BX					○			
RX5VA47CX						○		
RX5VA55AX	5.363	5.500	5.637	○				
RX5VA55BX					○			
RX5VA55CX						○		

Table 2

* Consult the guide to determine specifications other than those shown in Table 2. Use the type number.

■ TAPING METHODS

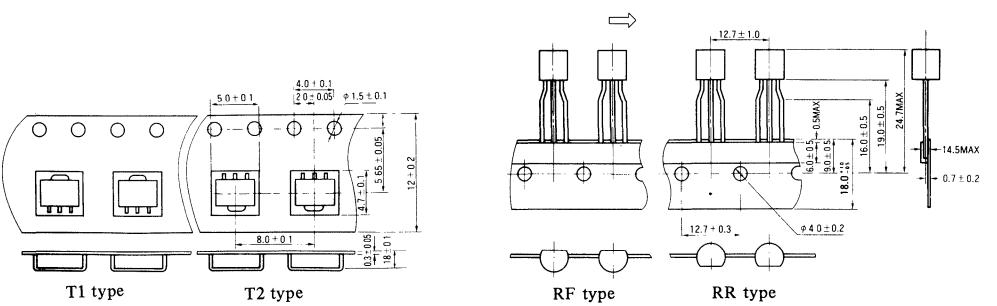


Figure 1

■ SYSTEM BLOCK DIAGRAMS

Figure 2 is block diagrams of RX5VA series and shows the system with three terminals. The system has three types of output drive : N-ch open-drain, P-ch open-drain, and C-MOS.

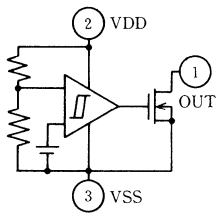
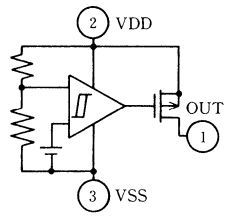
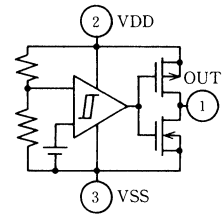
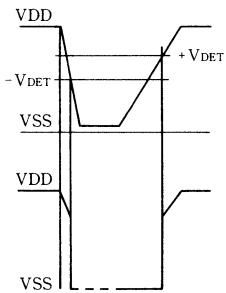
	N-ch open-drain (RX5VAXXAX)	P-ch open-drain (RX5VAXXBX)	C-MOS (RX5VAXXCX)
Block Diagrams			
Time Chart			
Package	3-terminals mini-power-mold TO-92		

Figure 2

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYNBOL	RATINGS	UNIT
Supply Voltage	VDD	12	V
Output Voltage	VOUT	VSS−0.3～VDD+0.3	
Output Current	IOUT	70	mA
Power Dissipation	Pd	300	mW
Operating Temperature Range	Topr	−30～+80	℃
Storage Temperature Range	Tstg	−40～+125	
Soldering Temperature	Tsolder	260℃ (10Sec)	

■ ELECTRICAL CHARACTERISTICS

Topr : 25℃

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Detect Voltage	−VDET		(−VDET) ×0.975		(−VDET) ×1.025	V
Hysteresis	VHYS			(−VDET) ×0.05		V
Supply Current	Iss	VDD= 2.0V		0.9	2.7	μA
		3.0V		1.0	3.0	
		4.5V		1.15	3.45	
		6.0V		1.3	3.9	
		10.0V		1.7	5.1	
Operating Voltage	VDD		1.5		10.0	V
Output Current	IOUT	Nch VDS=0.5V VDD:1.0V		0.5		mA
		2.4V		3.6		
		3.6V		6.5		
		4.6V		8.6		
		6.0V		11.6		
		10.0V		19.6		
		Pch VDS=2.1V VDD:4.5V	0.04			
Temperature Coefficient	△(−VDET) /△Ta	−30℃≦Ta≦80℃		±100		PPM/℃

■ PACKAGE INFORMATION

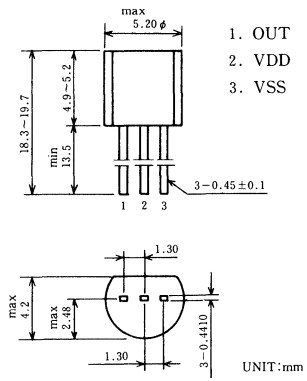


Figure 3. TO-9
(3-terminal)

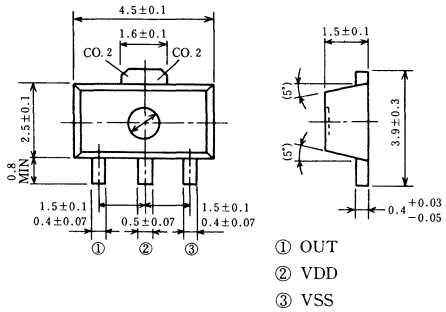
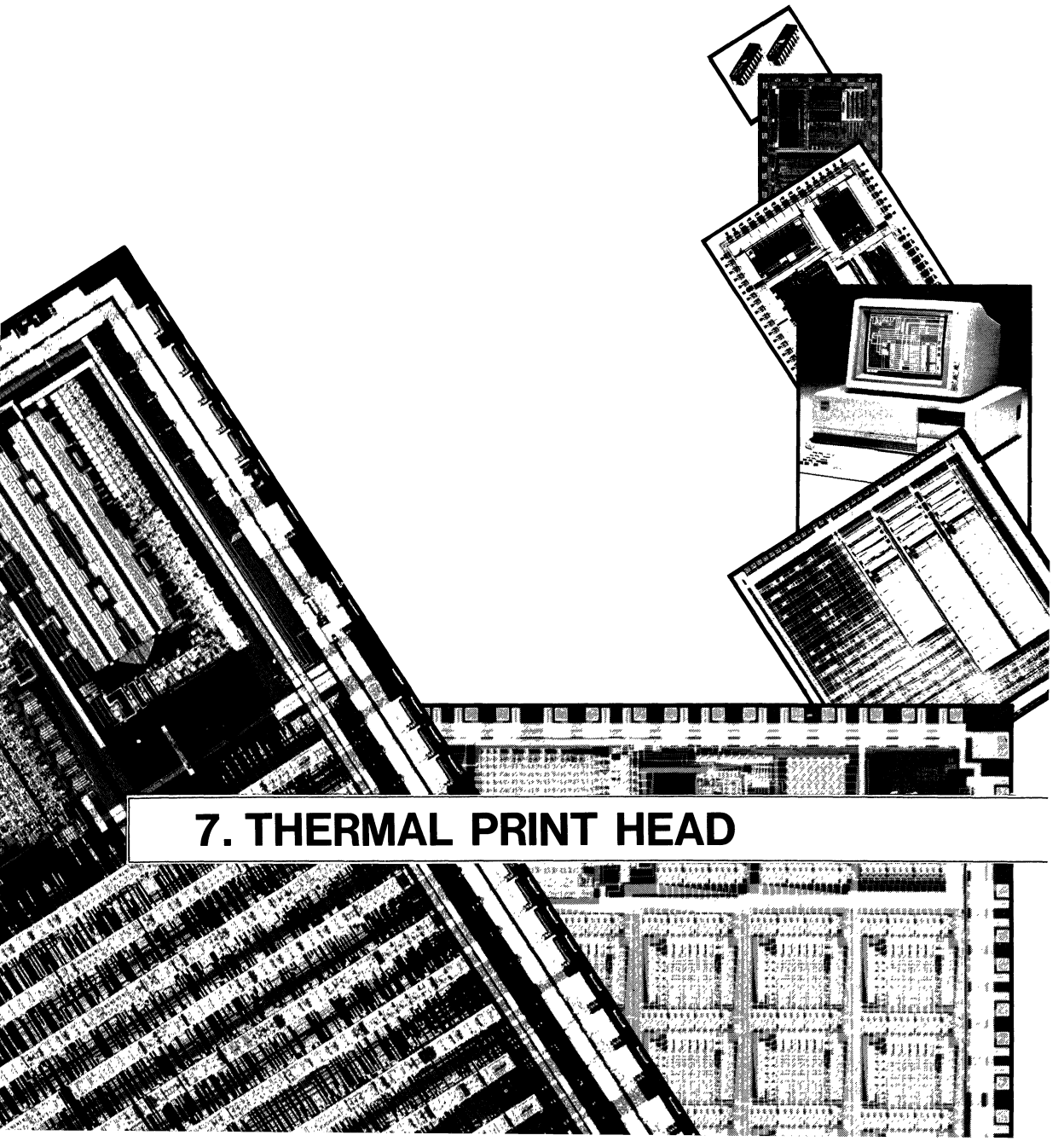


Figure 4. Mini-power-mold
(3-terminal)



7. THERMAL PRINT HEAD

RICOH is capable of meeting customer's needs on designing and manufacturing of IC, Thermal Print Head and also Heatsenstive paper, related machine.

For the RICOH Thermal Print Head, our large area thin film technology, high density and high precision photographic technology based on LSI process, and high density chip assembly technology have been mobilized to meet the needs for a great variety of recording densities, recording widths, sizes, forms, and other parameters.

In addition, thermal transfer printing, label printing, and other special applications may also be accommodated for our partially glazed types and label printing-oriented hard coated types.

[FEATURES]

- ○ With a high speed shift register driver mounted on, enables high speed printing operations to be achieved.
- ○ A totally new head structure has been employed to achieve the physical compact at about 15% (as compared with our earlier NH series).
- ○ The partially glazed types permit effective thermal transfer recording operations, and may also be applied to color printing requirements.
- ○ By mobilizing hard coating technology, the wear abrasion life at above 30km has successfully been attained even for the label printing process with its stringent operating requirements.
- ○ By virtue of a reduced voltage drop within the head and a structure for uniform heat dissipation, assures high picture quality with minimized density disuniformities.
- ○ In addition, Custom versions for application to special physical configurations may also be supplied upon request.

[PRODUCT LINEUP]

Series	Recommended Applications	Features
SH I	Facsimile, Recorders, Graphic Printers, and Plotters	Numerous types ranging from A1(24") to B9 (2") and from 16dpm to 4dpm have been made available to meet a wide range of requirements.
SH II	Same applications as the above, of which further compaction is demanded	The compact design with depth at 36mm will be effective in achieving the compaction of end equipment. Low cost types for general purpose.
Partially Glazed Types*	Thermal transfer Printers, Thermal transfer Facsimile	The resistor area has been made convex to achieve high speed and high picture quality for thermaltransfer recordings.
Hard Coated Types*	Bar Code Printers, and Ticket Vendors	Durability against label paper at above 30km is assured by a ultra hardness protective film.

* Partially glazed and hard coated types may be supplied for any of the SH I and SH II series models with extra-cost.

High performance can be achieved by our advanced technology.

[MODEL IDENTIFICATION]

Type I

SH – B4 8 – 4 I P
① ② ③ ④ ⑤ ⑥

1 Model No.
2 Effective printing width (B4 = 256mm)
3 Dot density (dots/mm)
4 Heater-element figure
5 Products series No.
6 Variation of glaze
(No marks = Full grazed type.
P = Partial grazed type.)

Type II

SH – 256 – 08 F S 4 I
① ② ③ ④ ⑤ ⑥ ⑦

1 Model No.
2 Effective printing width (mm)
3 Dot density (dots/mm)
4 Variation of glaze
(F = Full grazed type.
P = Partial grazed type.)
5 Wear film coated on heater element
(S = General protective film.
C = Ultra-hard coating for Label printer.)
6 Resistor value for heater element
7 Products series No.

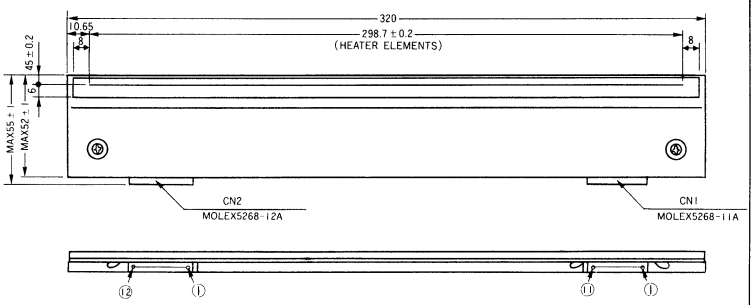
Type	Parts No.	Effective printing width (mm)	Dot density (dots/mm)	Total dots number (dots)	Heater element figure (μm x μm)	Resistor value typ. (Ω)	Standard power voltage	Printing condition				Clock frequency fc (MHz)	Outer dimension (mm) except for connecter
								Energy (mJ)	Cycle time (ms/ℓ)	Pulse width (ms)	Strobe number		
I	SH-A316-41	296	16	4736	50×100	1100	21	0.19	5	0.5	8	4	320×55 ×10.1
	SH-B416-41	256	16	4096	50×100	1100	21	0.19	5	0.5	8	4	275×45.7×10.1
	SH-A416-41*	216	16	3456	50×100	1100	21	0.19	5	0.5	8	4	234×55 ×10.1
	SH-A312-41*	298.7	12	3584	70×140	1100	24	0.25	5	0.5	8	4	320×55 ×10.1
	SH-B412-41*	256	12	3072	70×140	1100	24	0.25	5	0.5	8	4	276×55 ×10.1
	SH-A412-41	213.3	12	2560	70×140	1100	24	0.25	5	0.5	8	4	234×55 ×10.1
	SH-A48-44	216	8	1728	100×175	700	18	0.45	10	1	8	4	236×46.5×10.6
	SH-A68-42	104	8	832	100×175	230	11.6	0.45	5	1	4	4	124×46.5×10.6
	SH-B98-42	48	8	384	100×175	230	9.3	0.35	5	1	3	5	68×46.5×10.6
	SH-A66-44	106.7	6	640	150×230	670	22	0.84	5	1.2	4	4	124×46.5×10.6
	SH-A64-44	104	4	416	230×320	700	23.2	1.7	10	2.5	4	4	124×46.5×10.6
II	SH-400-08FS-41*	400	8	3200	100×175	1100	24	0.425	10	0.86	8	4	426×80 ×19.6
	SH-256-08FS41	256	8	2048	110×175	1320	22.4	0.35	5	1	8	4	274×36 ×10
	SH-216-08FS41	216	8	1728	110×175	1320	22.4	0.35	5	1	8	4	234×36 ×10
	SH-104-08FS41	104	8	832	110×175	1320	22.4	0.35	5	1	4	4	126×36 ×10
	SH-213-06FS31*	213.3	6	1280	150×230	630	21	0.6	5	1	4	4	234×36 ×10

* : under development

Configuration & Dimension

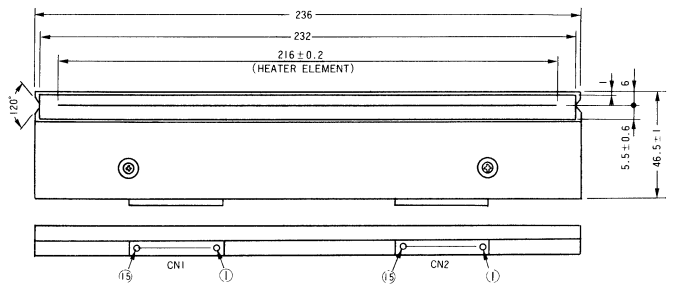
Pin Assignment

SH-A316-41



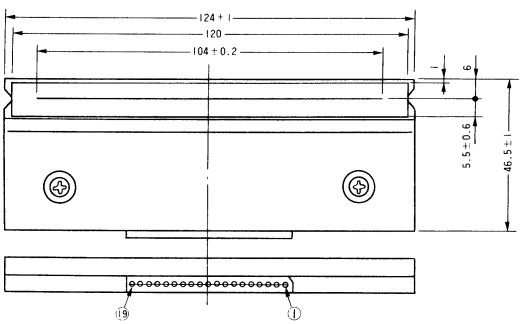
CN 1		CN 2	
PIN	SIGNAL	PIN	SIGNAL
1	V_{HD}	1	NC
2	V_{HD}	2	$\overline{SB}$ 4
3	GND	3	$\overline{SB}$ 3
4	GND	4	$\overline{SB}$ 2
5	V_{DD}	5	$\overline{SB}$ 1
6	V_{SS}	6	CK
7	$\overline{SB}$ 8	7	$\overline{LD}$
8	$\overline{SB}$ 7	8	DI
9	$\overline{SB}$ 6	9	GND
10	$\overline{SB}$ 5	10	GND
11	TH	11	V_{HD}
12		12	V_{HD}
13			
14			

SH-A48-44



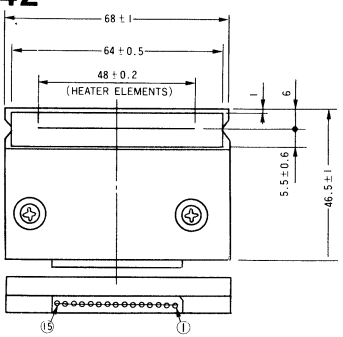
CN 1		CN 2	
PIN NO.	SIGNAL	PIN NO	SIGNAL
1	V_{HD}	1	V_{SS}
2	V_{HD}	2	V_{DD}
3	V_{HD}	3	$\overline{SB}$ 8
4	V_{HD}	4	$\overline{SB}$ 7
5	GND	5	$\overline{SB}$ 6
6	GND	6	$\overline{SB}$ 5
7	GND	7	$\overline{SB}$ 4
8	GND	8	$\overline{SB}$ 3
9	GND	9	$\overline{SB}$ 2
10	GND	10	$\overline{SB}$ 1
11	GND	11	DI
12	GND	12	V_{HD}
13	TH	13	V_{HD}
14	$\overline{LD}$	14	V_{HD}
15	CK	15	V_{HD}

SH-A68-42

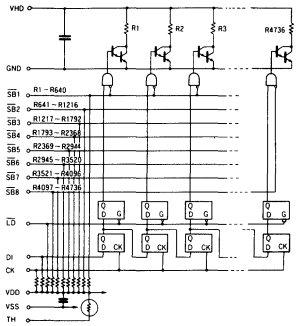


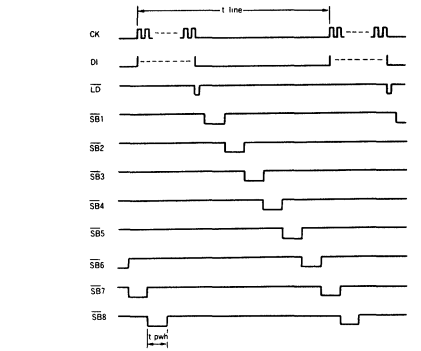
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	V_{HD}	11	$\overline{SB}$ 1
2	V_{HD}	12	$\overline{LD}$
3	GND	13	CK
4	GND	14	DI
5	GND	15	V_{DD}
6	GND	16	V_{SS}
7	TH	17	NC
8	$\overline{SB}$ 4	18	V_{HD}
9	$\overline{SB}$ 3	19	V_{HD}
10	$\overline{SB}$ 2		

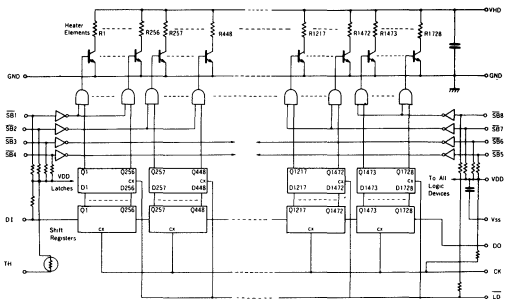
SH-B98-42

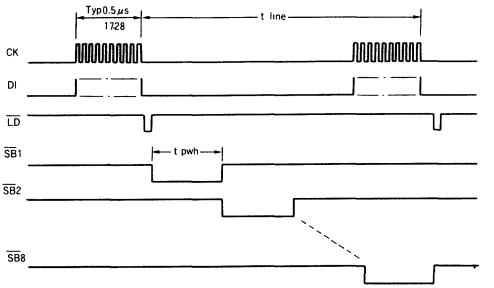


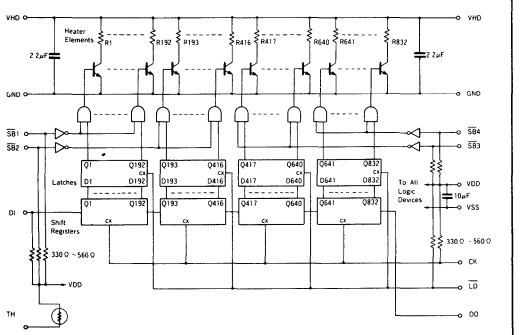
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	V_{HD}	11	$\overline{LD}$
2	V_{HD}	12	CK
3	V_{HD}	13	Din
4	GND	14	V_{DD}
5	GND	15	V_{SS}
6	GND		
7	TH		
8	$\overline{SB}$ 3		
9	$\overline{SB}$ 2		
10	$\overline{SB}$ 1		

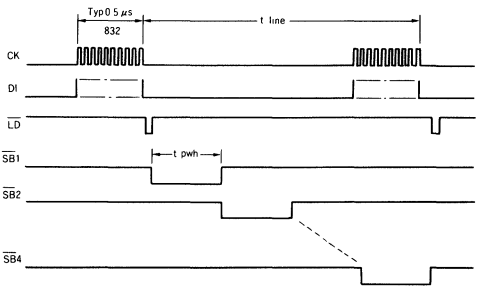

VHD
GND
R1
R2
R3
R4736
SB1
SB2
SB3
SB4
SB5
SB6
SB7
SB8
R1 ~ R640
R641 ~ R1216
R1217 ~ R1792
R1793 ~ R2368
R2369 ~ R2944
R2945 ~ R3520
R3521 ~ R4096
R4097 ~ R4736
LD
DI
CK
VDD
VSS
TH

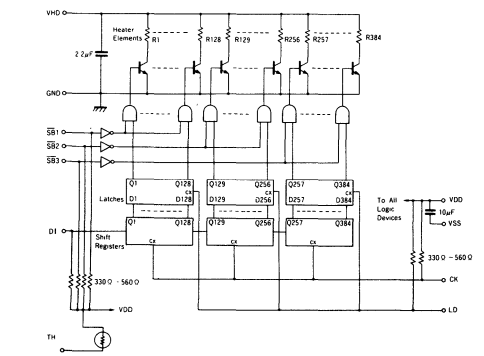

t line
CK
DI
LD
SB1
SB2
SB3
SB4
SB5
SB6
SB7
SB8
t pwh

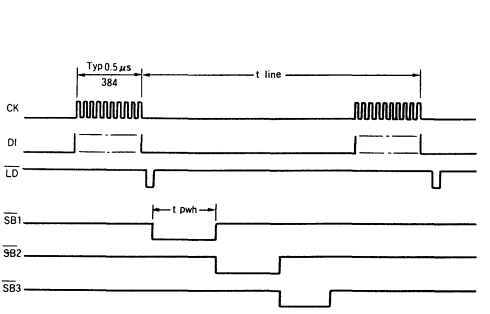

Heater Elements
R1
R256
R257
R448
R1217
R1472
R1473
R1728
VHD
GND
SB1
SB2
SB3
SB4
SB8
SB7
SB6
SB5
VDD
Latches
Shift Registers
To All Logic Devices
DI
TH
Vss
DO
CK
LD


Typ 0.5 μs
1728
t line
CK
DI
LD
SB1
t pwh
SB2
SB8


VHD
Heater Elements
R1
R192
R193
R416
R417
R640
R641
R832
2.2μF
GND
SB1
SB2
SB4
SB3
Latches
Shift Registers
To All Logic Devices
VDD
10μF
VSS
DI
330Ω - 560Ω
CK
LD
DO
TH


Typ 0.5 μs
832
t line
CK
DI
LD
SB1
t pwh
SB2
SB4

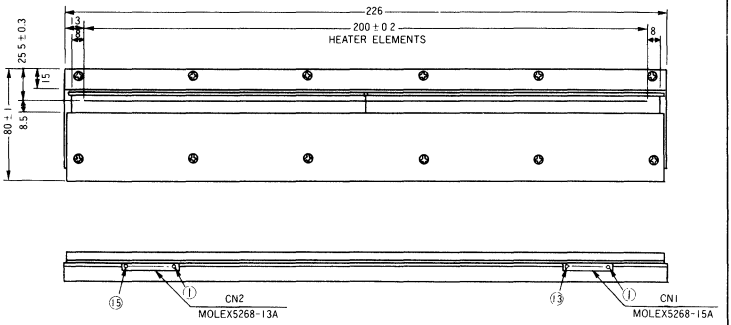

VHD
Heater Elements
R1
R128
R129
R256
R257
R384
2.2μF
GND
SB1
SB2
SB3
Latches
Shift Registers
To All Logic Devices
VDD
10μF
VSS
DI
330Ω - 560Ω
CK
LD
TH


Typ 0.5 μs
384
t line
CK
DI
LD
SB1
t pwh
SB2
SB3

Configuration & Dimension

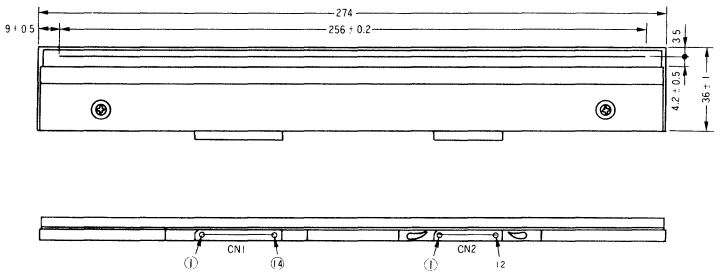
Pin Assignment

SH-400-08FS41



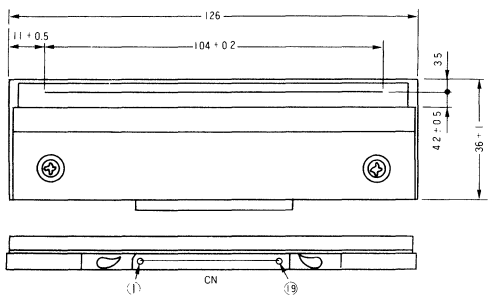
CN1		CN2	
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	V_{HD}	1	NC
2	V_{HD}	2	TH2
3	V_{HD}	3	$\overline{SB}$4
4	GND	4	$\overline{SB}$3
5	GND	5	$\overline{SB}$2
6	GND	6	$\overline{SB}$1
7	V_{DD}	7	CK
8	V_{SS}	8	$\overline{LD}$
9	$\overline{SB}$8	9	DI
10	$\overline{SB}$7	10	GND
11	$\overline{SB}$6	11	GND
12	$\overline{SB}$5	12	GND
13	TH1	13	V_{HD}
14		14	V_{HD}
		15	V_{HD}

SH-256-08FS41



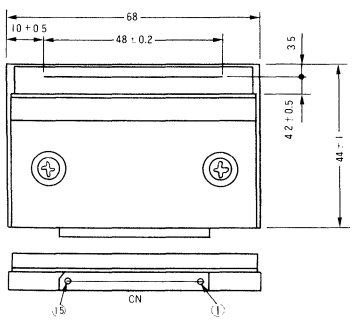
CN1		CN2	
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	TH	1	V_{HD}
2	NC	2	V_{HD}
3	DO	3	V_{HD}
4	$\overline{SB}$8	4	V_{HD}
5	$\overline{SB}$7	5	V_{HD}
6	$\overline{SB}$6	6	GND
7	$\overline{SB}$5	7	GND
8	$\overline{SB}$4	8	GND
9	$\overline{SB}$3	9	GND
10	$\overline{SB}$2	10	GND
11	$\overline{SB}$1	11	V_{SS}
12	CK	12	V_{DD}
13	$\overline{LD}$		
14	DI		

SH-104-08FS41

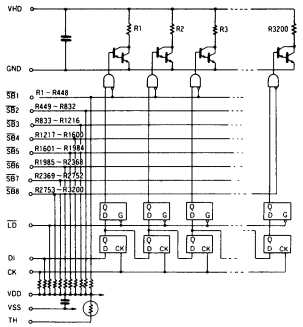


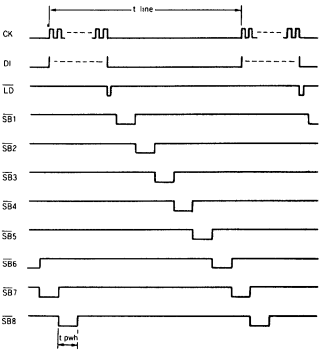
PIN NO.	SIGNAL	PIN NO	SIGNAL
1	V_{HD}	11	$\overline{LD}$
2	V_{HD}	12	CK
3	DO	13	DI
4	TH	14	GND
5	V_{SS}	15	GND
6	V_{DD}	16	GND
7	$\overline{SB}$4	17	GND
8	$\overline{SB}$3	18	V_{HD}
9	$\overline{SB}$2	19	V_{HD}
10	$\overline{SB}$1		

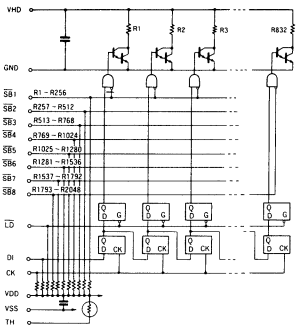
SH-48-08FS41

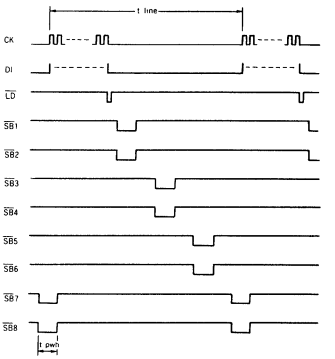


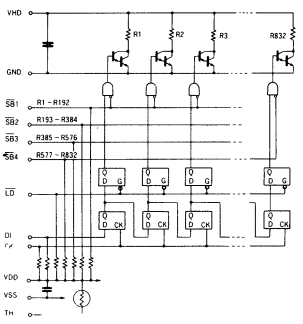
PIN NO.	SIGNAL
1	V_{HD}
2	V_{HD}
3	V_{HD}
4	GND
5	GND
6	GND
7	TH
8	NC
9	$\overline{SB}$2
10	$\overline{SB}$1
11	$\overline{LD}$
12	CK
13	DI
14	V_{DD}
15	V_{SS}

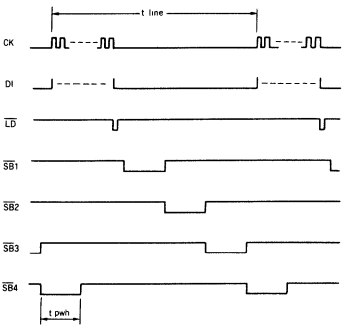

VHD
GND
R1
R2
R3
R3200
SB1 R1 – R448
SB2 R449 – R832
SB3 R833 – R1216
SB4 R1217 – R1600
SB5 R1601 – R1984
SB6 R1985 – R2368
SB7 R2369 – R2752
SB8 R2752 – R3200
LD
DI
CK
VDD
VSS
TH

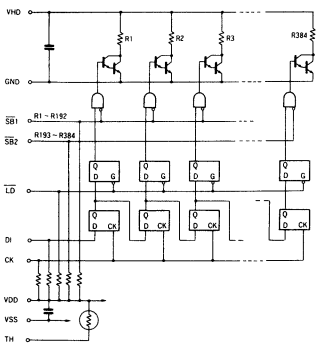

t line
CK
DI
LD
SB1
SB2
SB3
SB4
SB5
SB6
SB7
SB8
t pwh

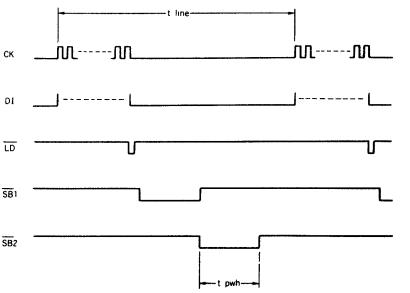

VHD
GND
R1
R2
R3
R832
SB1 R1 – R256
SB2 R257 – R512
SB3 R513 – R768
SB4 R769 – R1024
SB5 R1025 – R1280
SB6 R1281 – R1536
SB7 R1537 – R1792
SB8 R1793 – R2048
LD
DI
CK
VDD
VSS
TH


t line
CK
DI
LD
SB1
SB2
SB3
SB4
SB5
SB6
SB7
SB8
t pwh


VHD
GND
R1
R2
R3
R832
SB1 R1 – R192
SB2 R193 – R384
SB3 R385 – R576
SB4 R577 – R832
LD
DI
VDD
VSS
TH

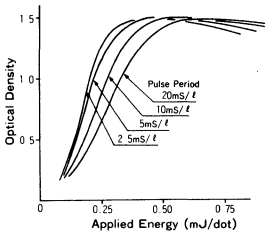

t line
CK
DI
LD
SB1
SB2
SB3
SB4
t pwh


VHD
GND
R1
R2
R3
R384
SB1 R1 – R192
SB2 R193 – R384
LD
DI
CK
VDD
VSS
TH


t line
CK
DI
LD
SB1
SB2
t pwh

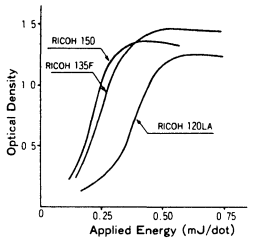
SH-Series Technical Data

Printing Characteristics (1)
(Full Glaze Type)



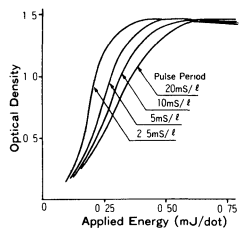
dot density	8dpm
pulse width	0.6ms
paper	RICOH 135F
platen weight	300g/cm
rubber thickness	5mm
rubber hardness	40°
platen diameter	20mmϕ
ambient temp.	22℃

Printing Characteristics (2)
(Full Glaze Type)



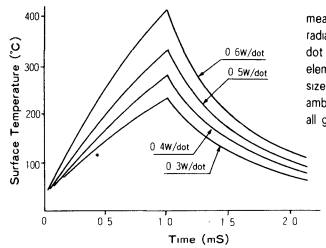
dot density	8dpm
pulse width	0.6ms
paper	RICOH 135F
platen weight	300g/cm
rubber thickness	5mm
rubber hardness	40°
platen diameter	20mmϕ
ambient temp	22℃

Printing Characteristics (3)
(Par (Partial Glaze Type)



dot density	8dpm
pulse width	0.6ms
paper	RICOH 135F
platen weight	150g/cm
rubber thickness	5mm
rubber hardness	40°
platen diameter	20mmϕ
ambient temp.	22℃

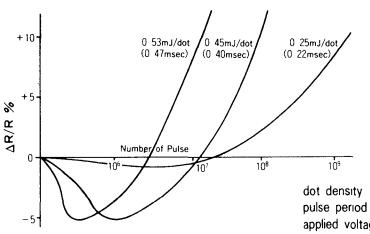
Thermal Response



measured by infrared radiation microscopy

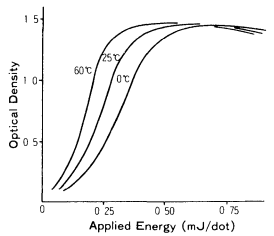
dot density	8dpm
element shape	rectangle
size	110×170mm
ambient temp.	23℃
all glaze	

Pulse Durability



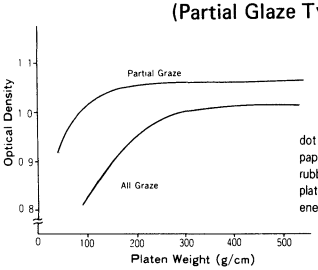
dot density	8dpm
pulse period	5msec/line
applied voltage	15V

Ambient Temperature & Optical Density
(Full Glaze Type)



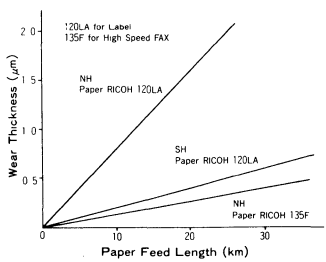
dot density	8dpm
pulse width	0.6ms
paper	RICOH 135F
platen weight	300g/cm
rubber thickness	5mm
rubber hardness	40°
platen diameter	20mmϕ

Platen weight & Optical Density
(Partial Glaze Type)



dot density	8dpm
paper	RICOH 135F
rubber thickness	5mm
platen diameter	20mmϕ
energy	0.28mj/dot

Wear Durability (Full Glaze Type)



platen weight	300g/cm
paper feed speed	100mm/sec
dot density	8dpm
without printing	

Typical Specification

1. Pulse Resistance

Type		SH I	SH II
Pulse Number	(MIN)	4×10^7	1×10^8
Cycle Time	(ms/line)	10	5
Pulse Width	(ms)	1	1
Applied Power	(w/dot)	0.65	0.35

○ Firing One Dot in Open Air, Room Temp., Room Humi.

2. Wear Resistance

Type		SH I	SH II
Paper Feed Length	(km)	MIN 40	MIN 30
Cycle Time	(ms/line)	10	5
Pulse Width	(ms)	1	1
Applied Power	(w/dot)	0.45	0.35
Paper Feed Speed	(mm/sec)	12.5	25
Platen Pressure	(g/cm)	300	300

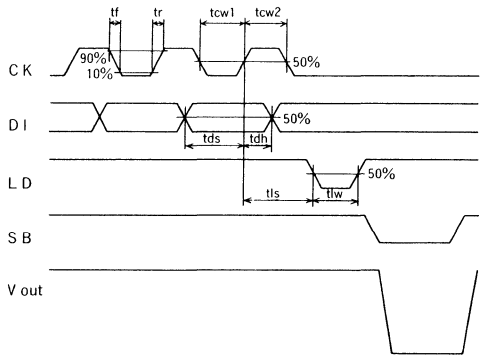
3. Environmental Condition

Type		SH I	SH II
Operating Temp.	(C°)	5~40	0~40
Operating Humi.	(%)	30~85	30~85
Storage Temp.	(C°)	−10~50	−20~60
Storage Humi.	(%)	30~85	30~85

4. Platen Condition

Type		SH I	SH II
Roller Diameter	(mm)	MAX 25	MAX 18
Roller Pressure	(g/cm)	300±50	300±50
Roller Rubber Hardness	(deg)	45±10	40±5
Rubber Thickness	(mm)	t 2~5	t 2~4

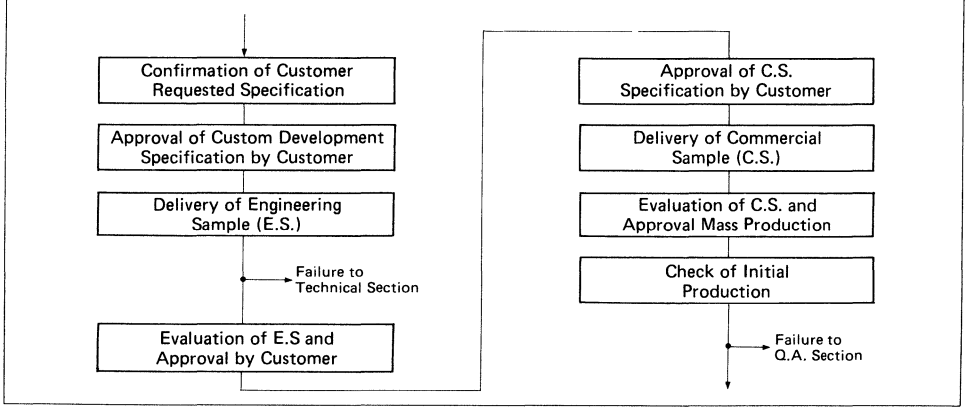
5. Timing Wave Form



Type		SH I	SH II
tcw 1	MIN (ns)	100	100
tcw 2	MIN (ns)	100	100
tds	MIN (ns)	100	100
tdh	MIN (ns)	100	100
tls	MIN (ns)	500	1500
tlw	MIN (ns)	250	350
tf	MAX (ns)	250	50
tr	MAX (ns)	250	50

* Typical specification discribed on this page is for SH I (SH-A48-44) and SH II (SH-216-08FS-41).

RICOH CUSTOM PRODUCT DEVELOPMENT FLOW CHART



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