RC 70 THE SYSTEMS COMPUTER

REDCOR CORPORATION

PRODUCT BROCHURE

RC 70

HARDWARE

- 860-nanosecond memory cycle time
- 8192-word memory expandable to 32,768 words
- 16-bit memory word
- Memory parity
- 6.2-microsecond multiply
- 11.4-microsecond divide
- Memory write protection
- External interrupt
- Hardware bootstrap loader
- Hardware index register
- 8 sense switches
- Direct memory access
  (1.1 million words per second transfer)
- Power shutdown and restart
- ASR 33 Teletype
- Choice of cabinet or 19-inch rack
- 32 priority interrupt levels*
- 4 block-transfer channels*
- Real-time clock*

SOFTWARE

- Single-pass assembler
- FORTRAN IV (USASI Standard)
- Math subroutines
- Utility package

ASSEMBLER

The REDCOR 70 Assembler is a single-pass symbolic assembler which operates in a basic 4K system configuration. The output may be either absolute or relocatable.

FORTRAN IV

The FORTRAN IV is a single-pass compiler meeting all USASI specifications.

MATH SUBROUTINES

The Math Subroutine Library includes routines for logarithmic, exponential, trigonometric functions, and arithmetic routines for single and double-precision calculations.

UTILITY PACKAGE

The Utility Package includes a tape edit program, debug package, loader and a tape copy/verify program.

*Optional

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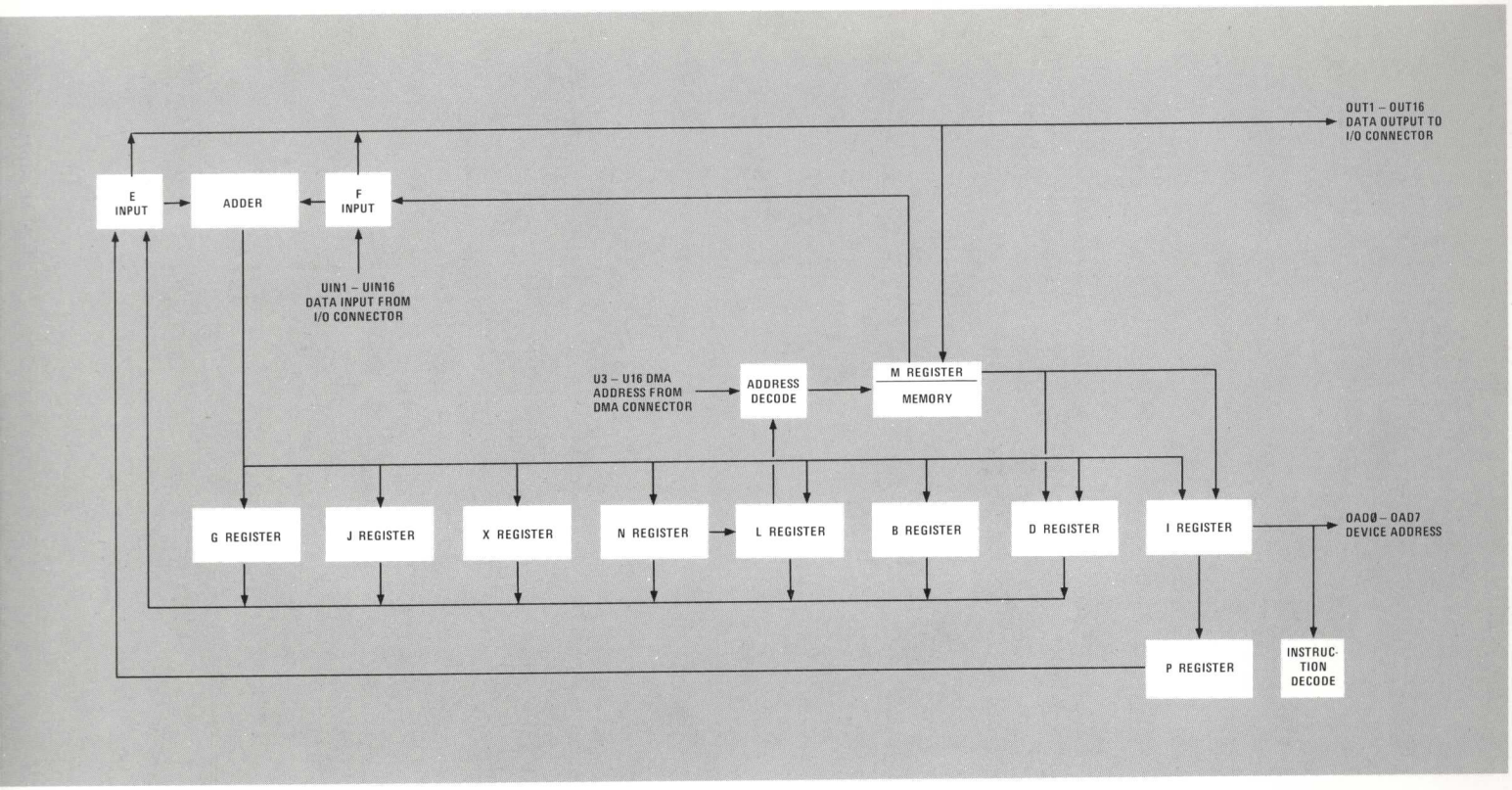


GENERAL DESCRIPTION

The capability of the REDCOR 70 to be incorporated in varied applications coupled with outstanding price/performance characteristics make it the leader in its class.

MEMORY

The internal core memory, consisting of 8,192 16-bit words plus parity, has a cycle time of 860 nanoseconds. Prewiring allows up to 16,384 words of memory (in 4096-word blocks) to be installed without additional cabinets or power supplies.

MEMORY ADDRESSING

There are four modes of addressing:

Direct: Single-word instruction—256 locations
Double-word instruction—32,768 locations

Indirect: Capable of full memory addressing

Indexed: Utilization of the X-register allows address modification without affecting execution time

Relative: To page register
To next instruction address register, forward and reverse 256 locations

REGISTERS AVAILABLE TO THE PROGRAMMER

UBA-Register: Upper accumulator
The upper accumulator (memory location 0008) is used as an extension of the lower accumulator for multiply and divide operations.

X-Register: Index register
The index register is a 16-bit flip-flop register.

R-Register: Roll arrow register
The roll arrow register (memory location 0007) provides for unlimited nesting of subroutines.

B-Register: Lower accumulator
The lower accumulator (16-bit flip-flop register) provides one of the operands to the adder and also stores the result.

P-Register: Page register
The page register (6-bit flip-flop register) selects the page in which the operand address is located.

REGISTERS NOT AVAILABLE TO PROGRAMMER

L-Register: Memory address register
The memory address register (14-bit flip-flop register) contains the address of the memory cell being accessed.

D-, G-, J-Registers: Working registers
These 16-bit flip-flop registers are temporary storage registers and working buffer registers.

I-Register: Instruction register
The instruction register (16-bit flip-flop register) contains the stored operation code.

N-Register: Next instruction address register
The next instruction address register (16-bit flip-flop register) contains the address of the next instruction to be executed.

INPUT/OUTPUT

Party-Line I/O Systems

16 Data output lines	8 Device address lines
16 Data input lines	9 Control lines

Four basic methods are used for input/output and control:

- Single word transfer under program control to/from accumulator
- Word transfers through direct memory access
- Discrete signals
- External interrupt

The direct memory access feature allows connecting up to 4 block transfer channels*; each allowing the control of 16 high-speed I/O devices without direct program intervention. Parallel data transfers of one word per memory cycle can be accomplished at a rate of up to 1.1 million words per second.

An external interrupt signal causes the program to branch to hexadecimal address 000F to pick up the location of the instruction to be executed.

Priority interrupts* are expandable in groups of 8, with group enable/disable and individual arm/disarm. Each interrupt level has a unique memory destination address.

PHYSICAL SPECIFICATIONS

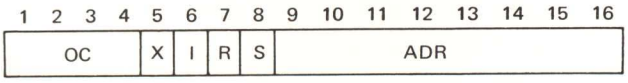
The REDCOR 70, with self-contained power supply, is 19 inches high, 19 inches wide, 19 inches deep, excluding front panel.

Weight: 90 lb
Temperature: 0° to 55°C
Relative humidity: 0% to 90%
Power requirements: 115 (±10)V
47 to 63 Hz
Power dissipation: 400W

Mounts in standard 19-inch cabinet

INSTRUCTION FORMAT

Single Word Instruction

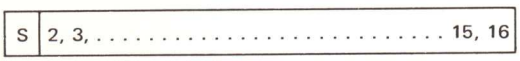


OC		Operation code
X		ADR is modified by the contents of the index register.
I		Indicates that word specified by ADR (as modified by RS) contains actual address of operand.
RS	00	ADR is absolute address in page 0.
	01	ADR is absolute address in page referenced by page register.
	10	ADR is an absolute value added to address of next instruction.
	11	ADR is an absolute value subtracted from address of next instruction.
ADR		Operand address

Double Word Instruction

LG	Long instruction identification
EOC	Extended operation code field
I	Indicates indirect addressing
R	Indicates relative addressing
OC	Instruction operation code
X	Indicates indexed addressing
ADR	Operand address

DATA FORMAT



16 bits

Two's Complement Magnitude
S = 1 (Negative)

INSTRUCTION LIST

Mnemonic	Name	Microseconds
ADB	Add	1.9
ALB	Arithmetic Left	1.9 - 4.5
ANB	And	1.9
ARB	Arithmetic Right	1.9 - 4.5
BBK	Branch Back	3.5
BEQ	Branch Equal	1.0
BGE	Branch Greater Than or Equal	1.0
BGT	Branch Greater Than	1.0
BLE	Branch Less Than or Equal	1.0
BLK	Branch and Link	3.6
BLT	Branch Less Than	1.0
BNE	Branch Unequal	1.0
BNO	Branch No Overflow	1.0
BPT	Branch and Put	5.5
BUC	Branch Unconditional	1.0
BXB	Branch Index	3.0
CMB	Compare	1.9
DVB	Divide	11.4

Mnemonic	Name	Microseconds
ELB	End Left	1.9 - 7.0
ELD	Double Length Shift	3.8 - 10.0
HLT	Halt	1.0
IOR	Inclusive Or	2.1
LDB	Load	1.9
LDP	Load Page	2.1
LDX	Load Index	2.1
LRB	Logical Right	1.9 - 4.5
MPB	Multiply	6.2
PIP	Parallel Input	2.7
POP	Parallel Output	2.7
SBB	Subtract	1.9
SET	Set Discrete	2.7
SNS	Sense	2.7
STB	Store	1.9
XMB	Exchange Accumulator and Memory	3.0
XOR	Exclusive Or	2.1

*Optional

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