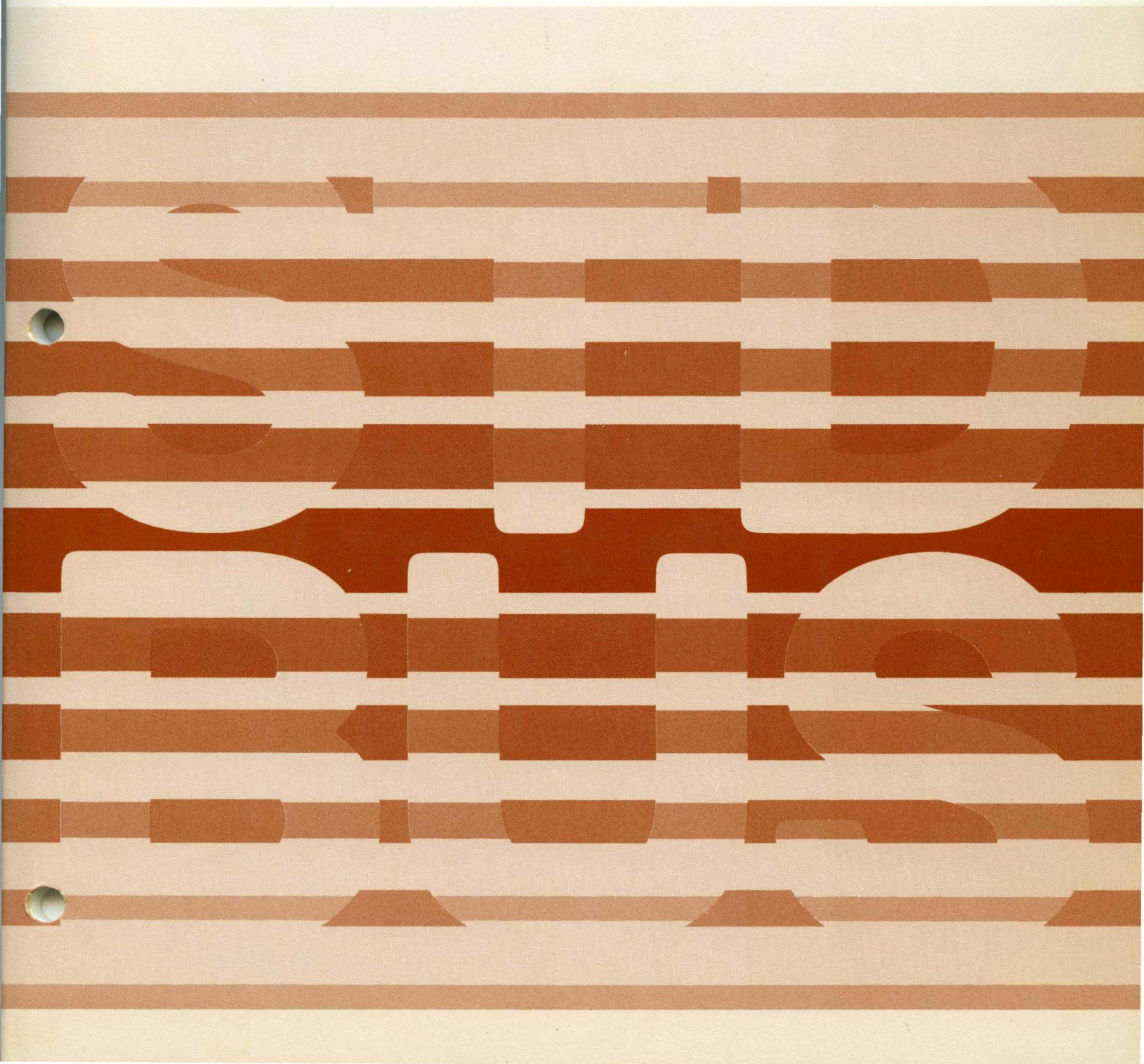
PRO-LOG
CORPORATION

STD 7000

7703
Battery-Backed
CMOS RAM Card

USER'S MANUAL



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7703
Battery-Backed CMOS RAM Card
USER'S MANUAL

PRO-LOG CORPORATION

8/81

FOREWORD

This manual explains how to use Pro-Log's 7703 Battery-Backed CMOS RAM Card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7703. We welcome your suggestions on how we can improve our instructions.

The 7703 is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of utilizing his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use, microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: *Microprocessor User's Guide* and the *Series 7000 STD BUS Technical Manual*. If you would like a copy of these documents, please submit your request on your company letterhead.

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SECTION 1
Purpose and Main Features

Purpose

The 7703 Card (Fig. 1-1) provides up to 16,384 bytes of high-speed (250ns), nonvolatile static CMOS RAM. It has a lithium battery backup that allows it to retain data for a minimum of two years; also, it generates a low-battery status signal (with an LED indicator) that may be jumpered to the STD nonmaskable interrupt. (See Fig. 1-2 for the block diagram.)

An onboard, memory-protected circuit in the 7703 monitors the +5V power and automatically generates a memory-save signal before switching to the lithium battery backup.

Write-protect switches (4K blocks) are available in the 7703 for preserving critical data and for nonvolatile program execution. The card decodes all 16 address lines. On-board jumpers permit mapping in any consecutive 4K, 8K, or 16K address blocks within 16K boundaries. All 7703 cards are shipped with starting address C000.

Main Features

- **Up to 16,384 bytes of nonvolatile static CMOS RAM**
- **Available in five configurations: 1K, 2K, 4K, 8K, and 16K bytes**
- **Lithium backup battery (guaranteed to give two years of data retention, five years typical)**
- **Automatic memory protection upon loss of +5V power**
- **Transportable without loss of data**
- **Write-inhibit switches (4K blocks)**
- **Temperature range: 0 to 55°C ambient**
- **Single +5V power requirements**
- **Full 64K address decoding**
- **Industry-standard multisourced components**
- **LED for replace-battery indication**
- **Instant operation (no battery-charging time required)**
- **Universal processor compatibility: Z80, 8085A, 6800, and others.**

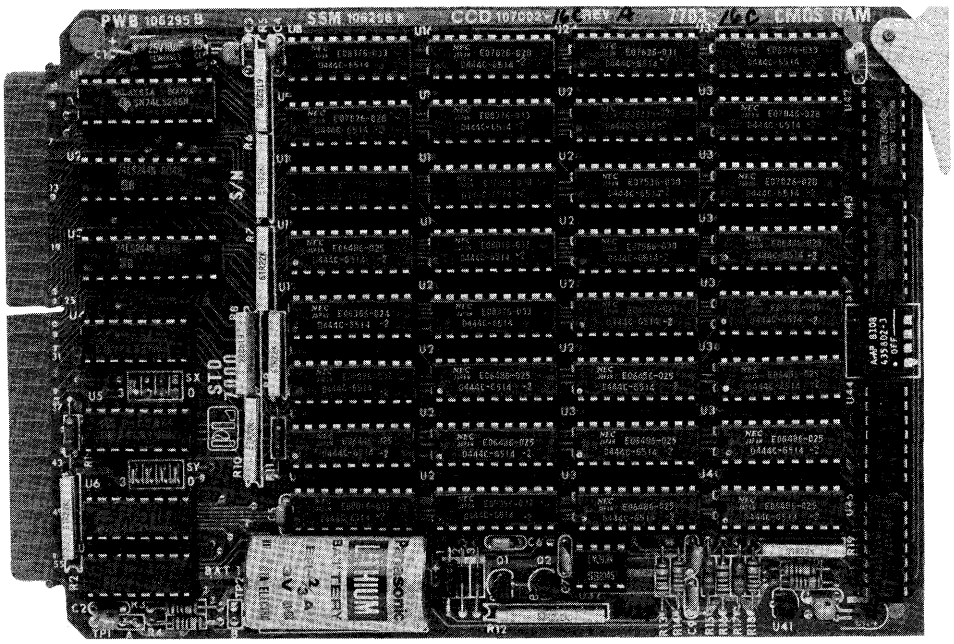
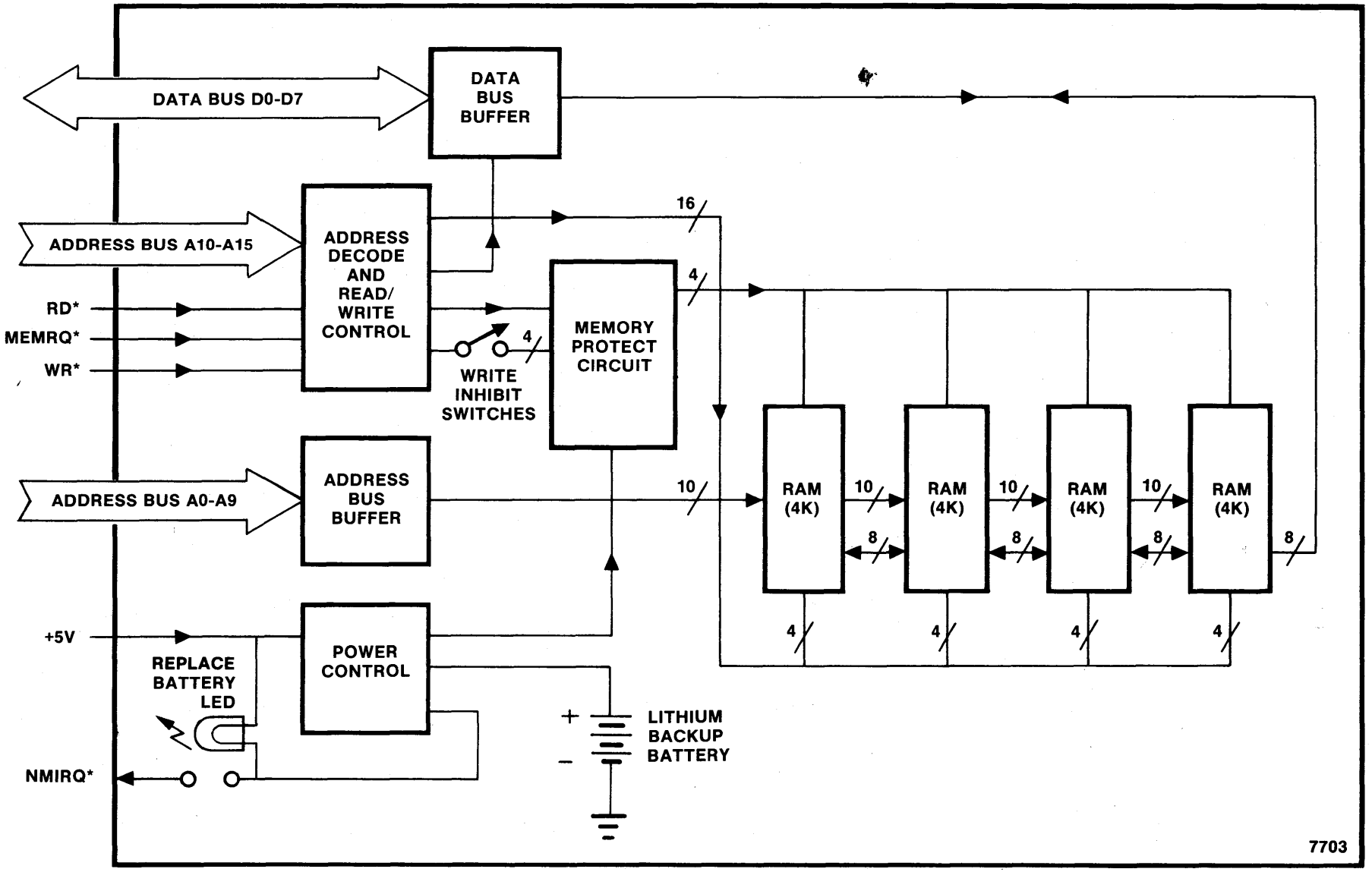


Figure 1-1. 7703 Battery-Backed CMOS RAM Card.



* Active low-level logic.

Figure 1-2. Block Diagram of 7703 Battery-Backed CMOS RAM Card.

SECTION 2
Installation and Specifications

Introduction

The 7703 operates as part of an STD BUS card rack system. You can plug in directly into any card slot on the motherboard, provided that the slot next to the battery is unoccupied. Optionally, you can plug the 7703 into a 7901 extender card, which in turn may be plugged into any vacant card slot on the motherboard; this configuration allows you to access the 7703 for testing or other purposes.

CAUTION

To prevent possible damage to your STD BUS system, make sure that power is off before inserting a card into the card rack, or before removing a card from the card rack.

At installation, the 7703's card ejector must be positioned towards the top of the card rack (see Fig. 2-1).

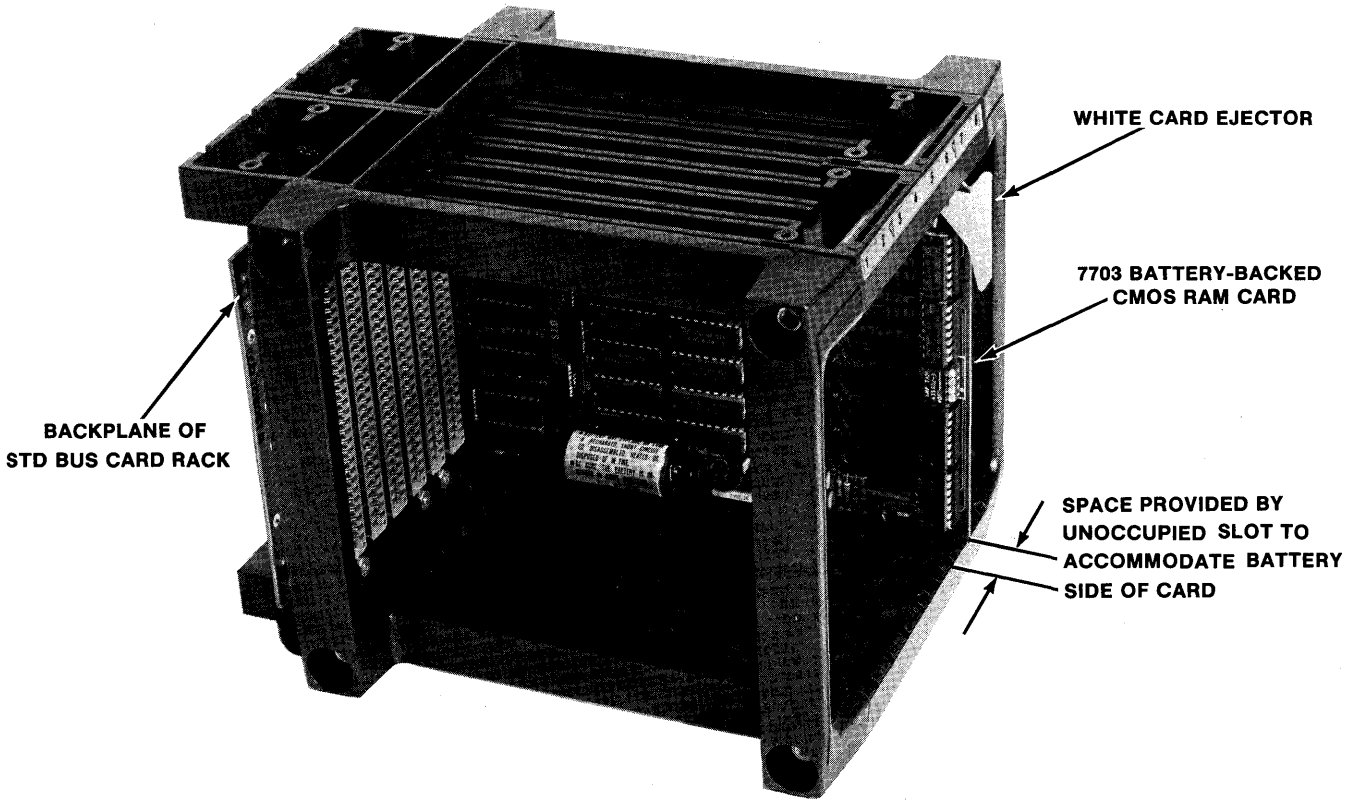


Figure 2-1. Installation of 7703 Card in STD BUS Card Rack.

You may configure the 7703 to operate within any one of the four 16K-byte address ranges available within the addressable 64K memory space. The 7703's 16K range is subdivided into four 4K blocks. Any combination of these 4K blocks may be enabled or disabled by appropriate jumpering of the 7703. You may order the 7703 in any of the standard configurations shown in Fig. 2-2. The boundaries established for each of the standard configurations for the 1K, 2K, 4K, 8K, and 16K options are shown in Fig. 2-3.

PRODUCT NUMBER	MEMORY SIZE	ADDRESS RANGE AS SHIPPED[1]
7703-1C	1Kx8	C000 - C3FF
7703-2C	2Kx8	C000 - C7FF
7703-4C	4Kx8	C000 - CFFF
7703-8C	8Kx8	C000 - DFFF
7703-16C	16Kx8	C000 - FFFF

[1] Address range may be remapped by the user, within any 16K boundaries.

Figure 2-2. Standard Configurations of 7703 Card (250ns CMOS RAM).

ADDRESS RANGE			RAM PAIRS ENABLED (Fig. 2-4)	SY TRACES TO BE LEFT INTACT OR CUT (X = CUT TRACE)				SX JUMPER POSITION			
START	END	SIZE BLOCK		3	2	1	0	3	2	1	0
0000	**03FF**	**1K**	0	X	X	X	I				I
0000	**07FF**	**2K**	0-1	X	X	X	I				I
0000	**0FFF**	**4K**	0-3	X	X	X	I				I
0000	**1FFF**	**8K**	0-7	X	X	I	I				I
0000	**3FFF**	**16K**	0-15	I	I	I	I				I
4000	**43FF**	**1K**	0	X	X	X	I			I	
4000	**47FF**	**2K**	0-1	X	X	X	I			I	
4000	**4FFF**	**4K**	0-3	X	X	X	I			I	
4000	**5FFF**	**8K**	0-7	X	X	I	I			I	
4000	**7FFF**	**16K**	0-15	I	I	I	I			I	
8000	**83FF**	**1K**	0	X	X	X	I		I		
8000	**87FF**	**2K**	0-1	X	X	X	I		I		
8000	**8FFF**	**4K**	0-3	X	X	X	I		I		
8000	**9FFF**	**8K**	0-7	X	X	I	I		I		
8000	**BFFF**	**16K**	0-15	I	I	I	I		I		
C000	**C3FF**	**1K**	0	X	X	X	I	I			
C000	**C7FF**	**2K**	0-1	X	X	X	I	I			
C000	**CFFF**	**4K**	0-3	X	X	X	I	I			
C000	**DFFF**	**8K**	0-7	X	X	I	I	I			
C000	**EFFF**	**16K**	0-15	I	I	I	I	I			

Figure 2-3. Mapping the 7703 Card.

Mapping Card Addressing

Figure 2-4 shows the location of the SX jumpers, the SY jumpers, and the RAM pairs on the 7703 card. The CMOS RAMs are NEC 6514-2, with 250ns access time. Each RAM device is 1Kx4 bits; therefore, each RAM pair provides 1Kx8 bits of memory. Up to 32 devices may be placed on the 7703, allowing a maximum of 16K bytes on one card. Four 7703 cards provide a full backup of 64K bytes of memory.

Alternatives to Soldered Wire Jumpers

If you anticipate making frequent changes in your 7703 memory address mapping, you may replace the wire jumpers for SX and SY with 0.025 in. (0.635 mm) square posts. These posts are available individually or in single or double strips that correspond to the 0.001 in. (0.025 mm) grid jumper-pad spacing. You then connect the posts by wirewrap or by jumper clips. Be sure you check the height that the posts extend above the board to insure they do not interfere with an adjacent card. The recommended wirewrap square post for SX and SY is AMP No. 87215-1, or equivalent. The recommended jumper clip is AMP No. 530153-2, or equivalent.

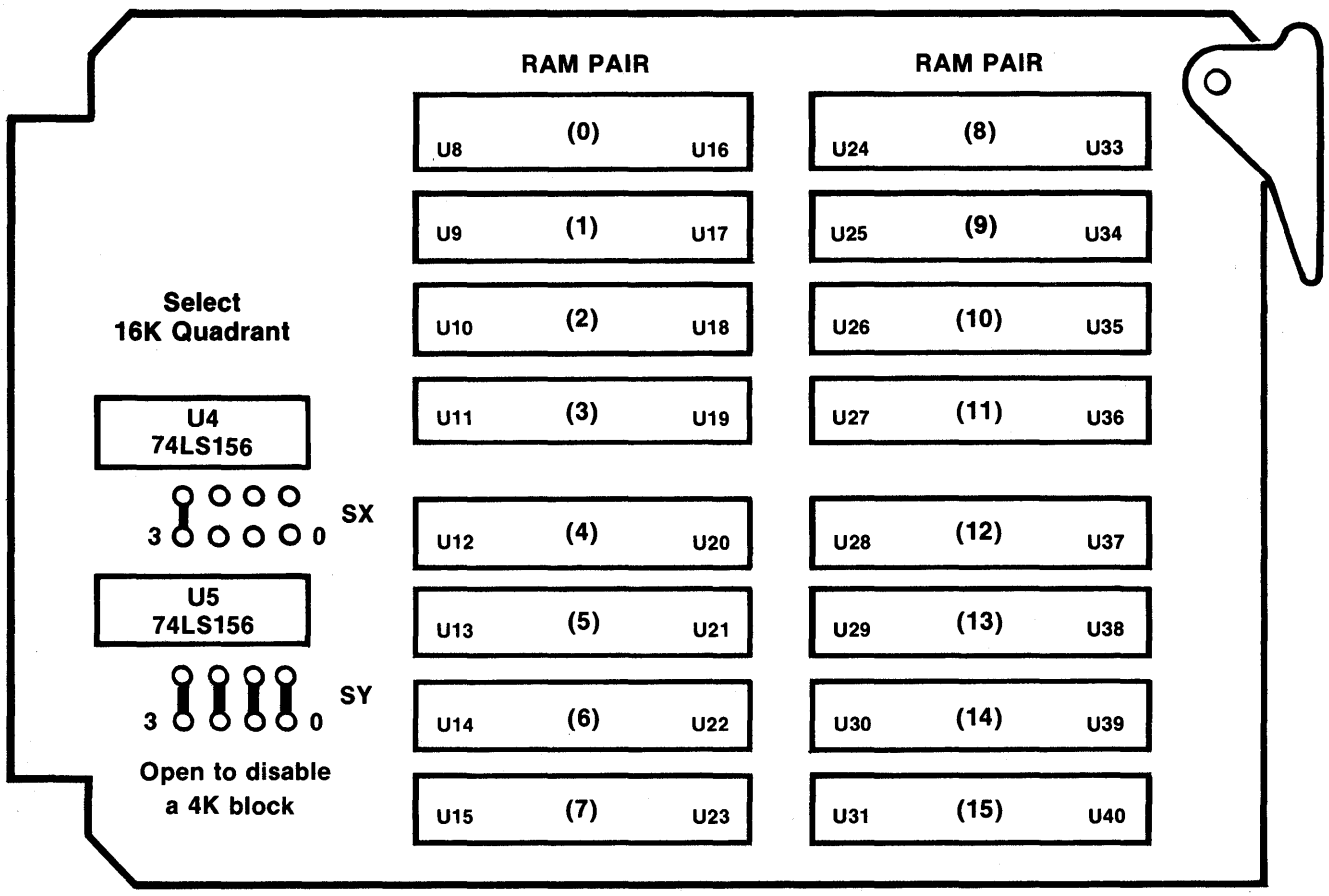


Figure 2-4. Location of RAM Pairs on 7703 Card.

SYMBOL	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
		MIN	TYP	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0	5.50	V
T_A	Free-air temperature	0	+25	+55	-20	+70	°C
R_H	Humidity [1]	5	—	95	0	95	%RH

[1] Noncondensing.

Figure 2-5. Operating Limits of Electrical and Environmental Parameters for 7703 Card.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Icc	Vcc supply current	—	145	230	mA
—	Data retention	2	5	—	yr
—	Battery life (shelf)	—	10	—	yr
—	STD BUS input load	See Fig. 2-7		See Fig. 2-7	
—	STD BUS output load	See Fig. 2-7		See Fig. 2-7	

Figure 2-6. STD BUS Electrical Specifications Over Recommended Operating Limits.

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5V	Vcc		2	1		Vcc	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15	1		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	1		22	21		1	A4
A11	1		24	23		1	A3
A10	1		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*	1		34	33			IORQ*
MEMEX	1		36	35			IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*		20[1]	46	45			WAITRQ*
PBRESET*		OUT	48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic [1] Open-collector driver

Figure 2-7. Edge Connector Pin List for 7703 Card.

Mechanical Specifications

The 7703 Card meets all general mechanical specifications of the STD BUS except for battery height, which is 0.678 in. (16.9 mm) maximum above center line of the card thickness. It requires two card slots when mounted in an STD BUS card rack — one additional open slot next to the component side for clearance of the lithium battery.

The 7703 is shipped with a Series 7000 insulating shield covering the back side of the card, providing protection for the CMOS chips on board.

SECTION 3
Operation and Programming

Introduction

This section explains how to operate the 7703. It also describes how to retain or preserve critical data on the 7703 if power fails, and how to remove the card without losing data. The 7703 operates under program control from the CPU.

Preparing the 7703 for Initial Use

First select the jumpering required for use of your card configuration (1, 2, 4, 8, or 16K) in the desired address space (see Fig. 2-3). Also, check Fig. 2-3 to determine which SY traces to leave intact and which SY traces to cut, to enable the various 4K byte memory segments. The last column in the figure specifies which of the SX jumpers must be activated to select the desired 16K byte segment.

NOTE

SX-3 is default-jumpered on all 7703 boards shipped. This activates the 7703 for operations in the upper 16K bytes of memory, starting at C000.

After completing the memory mapping, install the battery activation jumper (jumper A), if it is not already installed. (This jumper is located in grid B6 of the assembly drawing for the 7703, Fig. 5-2.)

To verify that standby memory current is within specification, connect a voltmeter across the test points TP1 and TP2. (These points are located in grids B7 and B6, respectively, of the assembly drawing for the 7703, Fig. 5-2.) The voltage should read not more than 0.003 VDC, although the reading may be considerably less. A proper reading at this point verifies that the lithium backup battery is properly installed and operating. If the voltage is more than 0.003, disconnect the battery and return the card to the factory (see "Return for Repair Procedures" in Section 5.) Set all the write-inhibit switches to the write-enable position (if required), in preparation for using the 7703 (see Section 4). (These switches are located in grid C4 of the assembly drawing for the 7703, Fig. 5-2.)

Activating the 7703

With the 7703 installed as outlined in Section 2:

1. Apply system power.
2. As part of system initialization, perform a memory-read operation or a memory-write operation to a random address within the address space allocated to the 7703 card. The first time a memory-read or memory-write operation is performed, memory-inhibit is removed. This "dummy" memory reference step is extremely important to insure that the system memory is enabled before it is actually referenced. The memory reference sets the operate flip-flop, which then enables the 7703 card operation. The operate flip-flop is reset automatically at power-down and again at power-up to insure data integrity on the 7703. Further details on this operation are provided in Section 5.
3. Use the write-inhibit switches to inhibit writing to any of the four 4K-byte blocks within the 7703 card address space. (See Fig. 5-3 for the location of the write-inhibit switches.) Figure 2-3 shows the enable-jumpering required for the onboard memory devices.
4. You may now use the software provided in Section 4 to exercise the 7703.

Saving Data When Power Fails

The most effective method to insure that essential data is saved in event of system power failure is to store such data, including the system stack, on the 7703 card. However, the user must provide the hardware for monitoring system power failure at his +5V power supply.

The circuitry and software for detecting system power failure should monitor the user's power supply to detect any deviation from normal power behavior. The hardware must then generate a nonmaskable interrupt and allow time for the interrupt software to execute its power failure data-save functions. The interrupt software should allow all essential CPU register data to be stored and all address and data bus activity to be halted; this must be accomplished before the system power falls below the minimum operating level. A flowchart for a suggested power failure system is depicted in Fig. 3-1.

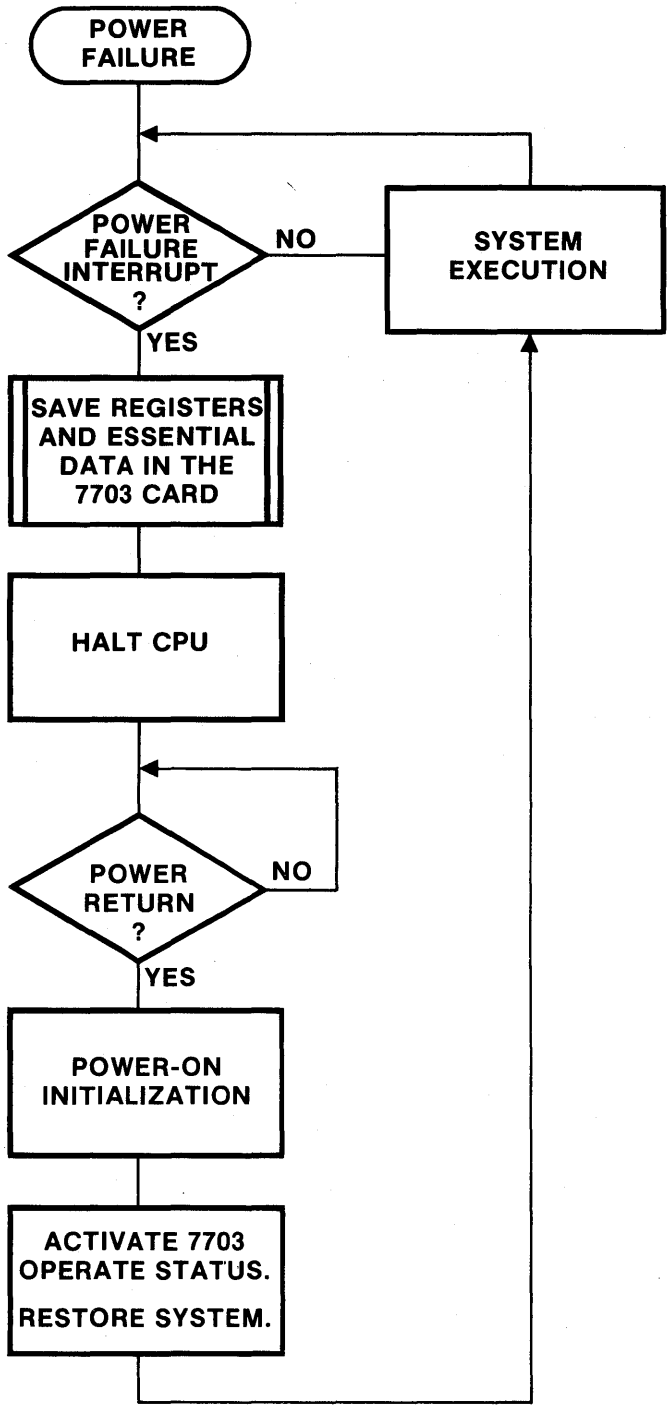


Figure 3-1. Flowchart Showing Power Failure Procedure for 7703 Card.

7703 Power Monitor

The 7703 has a "Low Vcc Detect" circuit on board. This circuit generates the LOW Vcc* signal, which is used to inhibit memory if Vcc falls below 4.52V. The low Vcc detect circuit is used to save the 7703 card memory only, **not** the entire system.

Removing the 7703 Card without Losing Data

To remove the 7703 card from the card cage without losing data, follow these steps:

1. Halt the CPU.
2. Set all write-inhibit switches to the inhibit position.
3. Power-down the system.
4. Gently remove the 7703 card from the rack. Now the stored data is protected by the card's battery backup.

You may now transport or store the 7703 card for future use. When you do use it again in another system, follow the installation procedure detailed in Section 2.

Figure 3-2 flowchart shows how to remove and insert the 7703, insuring full data retention.

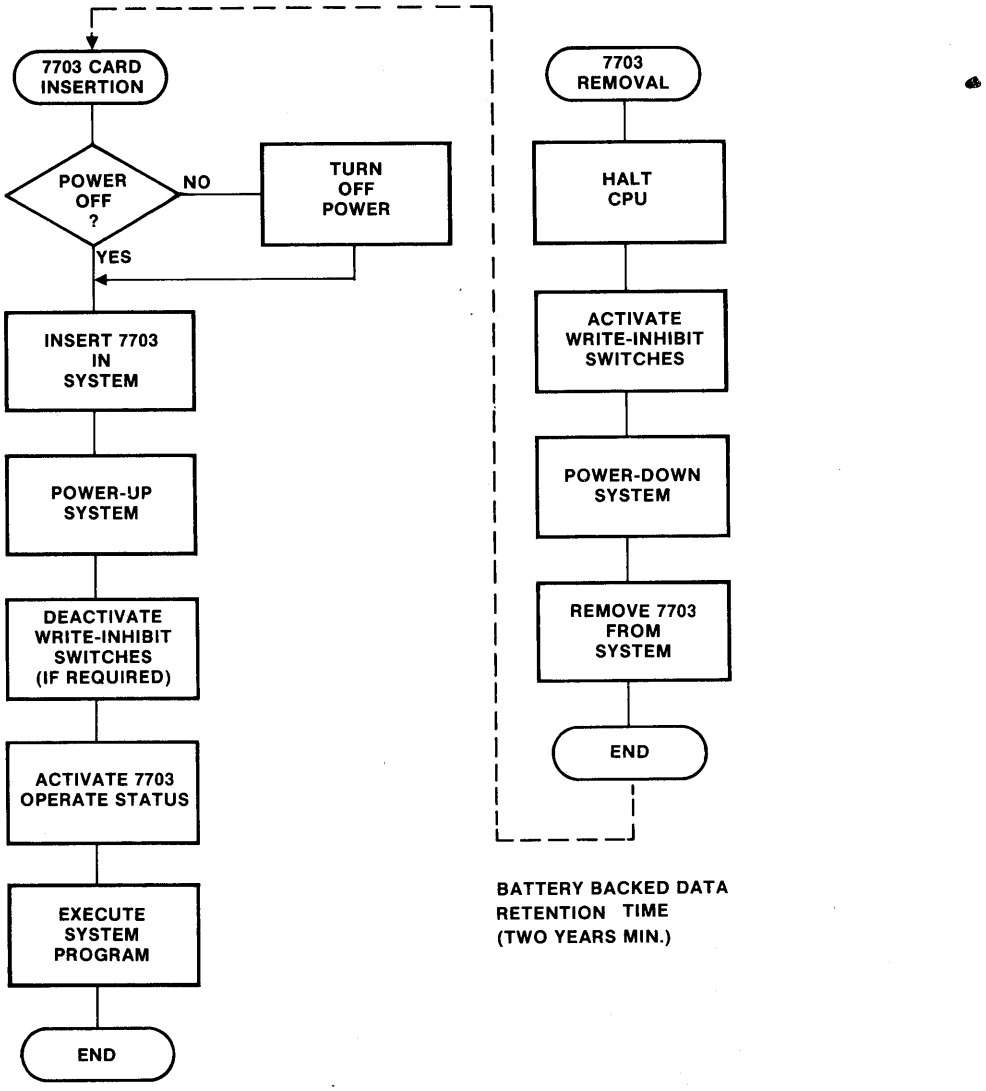


Figure 3-2. Flowchart Showing Insertion and Removal Procedure for 7703 Card.

SECTION 4
Operating Software

Introduction

This section contains hardware-level subroutines that can be used for testing the 7703 CMOS RAM card or for diagnosing malfunctions. They are designed with the user in mind and assume that your 7703 card can be mapped for use in other than the first 16K quadrant (0000-3FFF). See Fig. 4-1 for the subroutine index.

SUBROUTINE NAME	FUNCTION	SEE FIGURES
(MOVE BLOCK)	Moves a block of data from one location in memory to a user-specified location in RAM.	4-5, 4-6, 4-7
(-(HL))	Forms 2's complement of HL register pair contents.	4-8, 4-9, 4-10
(COMPARE BLOCK)	Compares two blocks of data in memory.	4-11, 4-12, 4-13, 4-14, 4-15
(LOAD BLOCK)	Loads a designated data word into a specified block of RAM. (Used with (MOVE BLOCK) and (COMPARE BLOCK) to test memory's retention and erasure of particular bit patterns.)	4-16, 4-17, 4-18
(LOAD A = D)	Loads a specified block of memory with an address equal to the data format.	4-19, 4-20, 4-21
(VERIFY A = D)	Verifies that correct address is contained within specified data byte. Used in conjunction with (LOAD A = D).	4-22, 4-23, 4-24, 4-25, 4-26

( ) Denotes subroutine labels.

Figure 4-1. Index of Subroutines for 7703 Card.

The software in the section can be used without license from Pro-Log. It has been tested and is believed to be correct; however, we do not represent it to be free from errors or possible copyright infringement, nor is it represented as being appropriate for any specific application.

The subroutines are written in STD instruction mnemonics, using 8080 assembly codes. They will execute in 8080, 8085, Z80, NSC 800, and other 8080 code-compatible microprocessor systems. The coding forms are grouped at the end of this section (Fig. 4-27), following the subroutine specifications.

Flowcharts are included that do not refer to microprocessor characteristics; thus, they allow the routines to be easily adapted to other types of microprocessors.

Individual subroutine specifications show memory requirements, entry requirements, and exit characteristics for each path in the program. Timing and other necessary information are also provided.

Memory Addresses

Full memory addresses are shown in the subroutine documentation. They are the preferred addresses that allow the subroutines to work with those provided for other Series 7000 STD BUS cards from Pro-Log. The program addresses correspond to those used by the 7801 and 7803 processor cards for their onboard ROM/EPROM and RAM devices.

If your system cannot use the memory addresses in the 7703's software package, simply change the memory page addresses, as required, when loading these subroutines into your system. Memory addresses that **must** be located in RAM are identified on the program coding forms. Other memory addresses shown are intended to be ROM locations, but they may also be RAM locations.

Diagnostic Use

The error routines place relevant data in the various registers and set an error flag. The memory location where the error occurred and the erroneous data can be retrieved by examining the registers containing the error information.

Shakedown (Confidence Level) Test

A flowchart and an example program module are provided to demonstrate a sequence of operations you may use to perform a quick shakedown or confidence level test of the 7703. (See Figs. 4-28 and 4-29 at the end of the section.)

Memory Maps

Figure 4-2 shows a 64K memory map, which is divided into 256-byte pages and gives the location of the 7703's software package, the location of the stack, and the location of the 7703's memory space, as shipped (C000-FFFF).

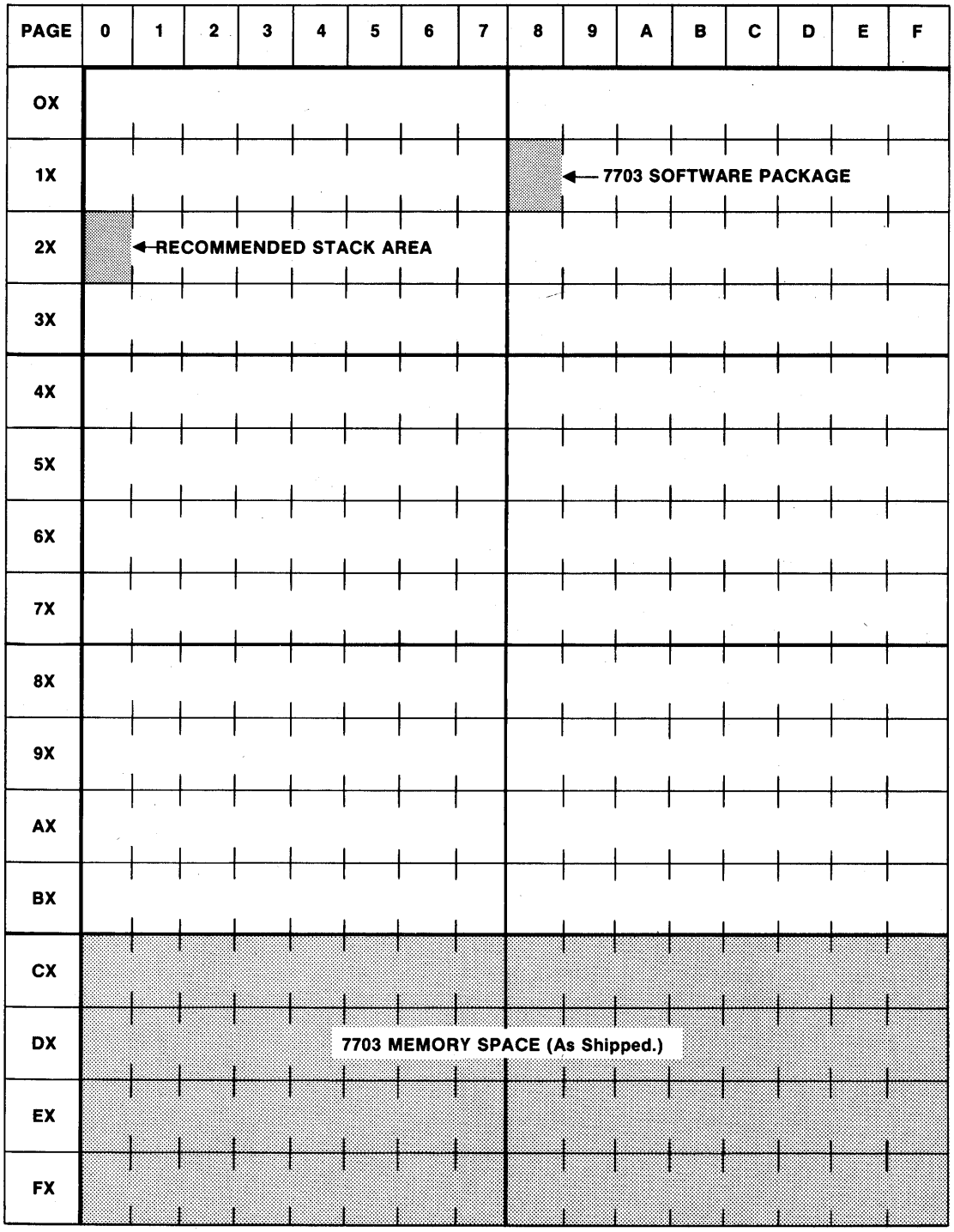
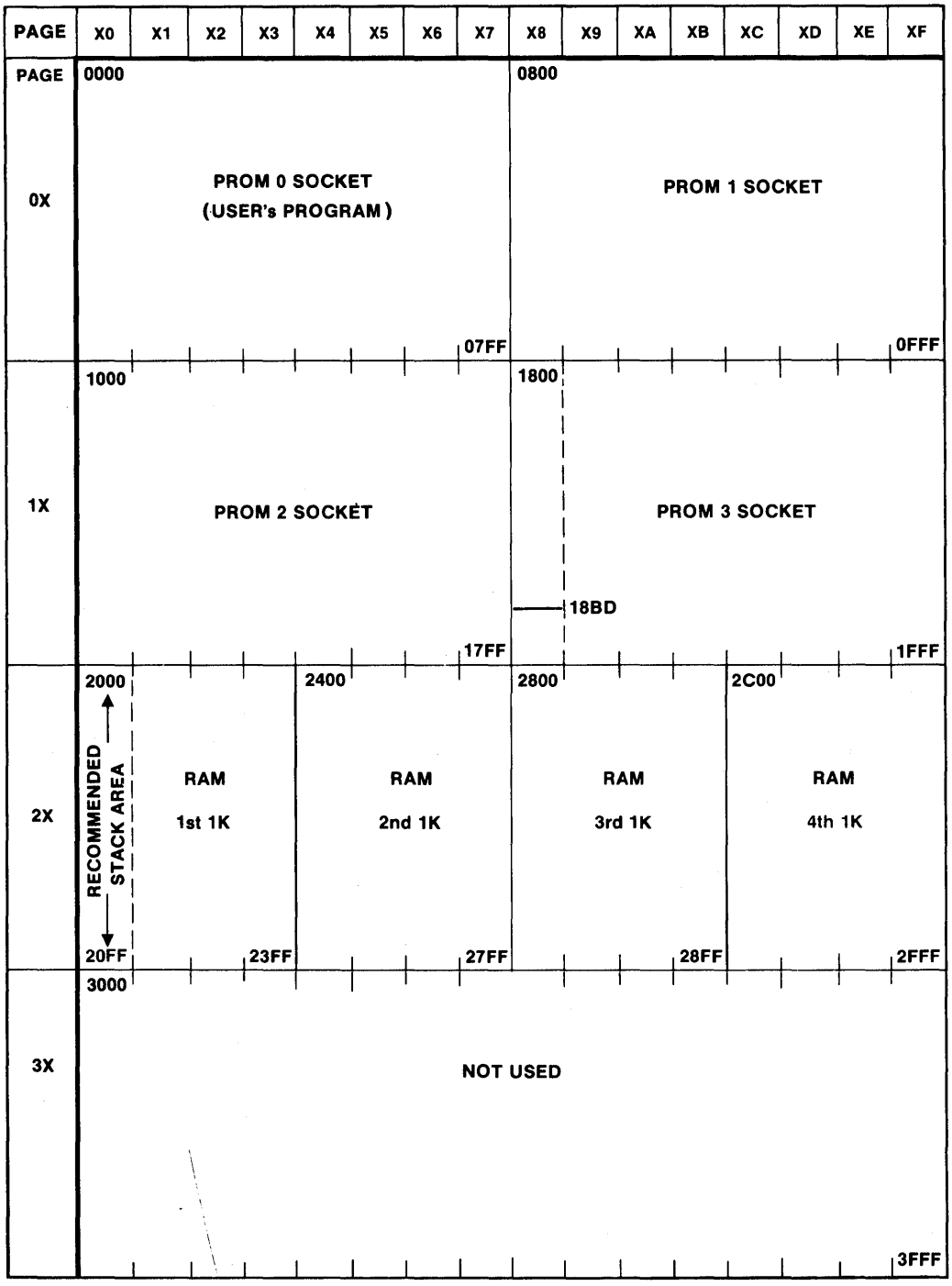


Figure 4-2. 64K Memory Map for 7703 Software Package.

Figure 4-3 displays a 16K memory map, showing the location of the user's programs, the 7703 subroutines, and the stack. It also shows the locations of the EPROM and RAM memory spaces on the 7801 and 7803 processor cards.



NOTES

1. 7801 (8085A) and 7303 (Z80) processor cards have sockets for 8K ROM/PROM (sockets labeled PROM 0 - PROM 3). These cards are shipped with these sockets empty. Also, the cards have sockets for 4K RAM, and the card is shipped with 1st 1K loaded and 2nd, 3rd, and 4th 1K sockets empty.
2. This map shows the 7303 software loaded in user-supplied PROM 2. Page 20 (memory addresses 2000-20FF) is recommended for subroutine return address stack.

Figure 4-3. 16K Memory Map for 7703 Software Package.

Figure 4-4 illustrates a one-page memory map, subdivided into individual addresses, showing the 7703's subroutines starting at address 1800 and ending at 18BD.

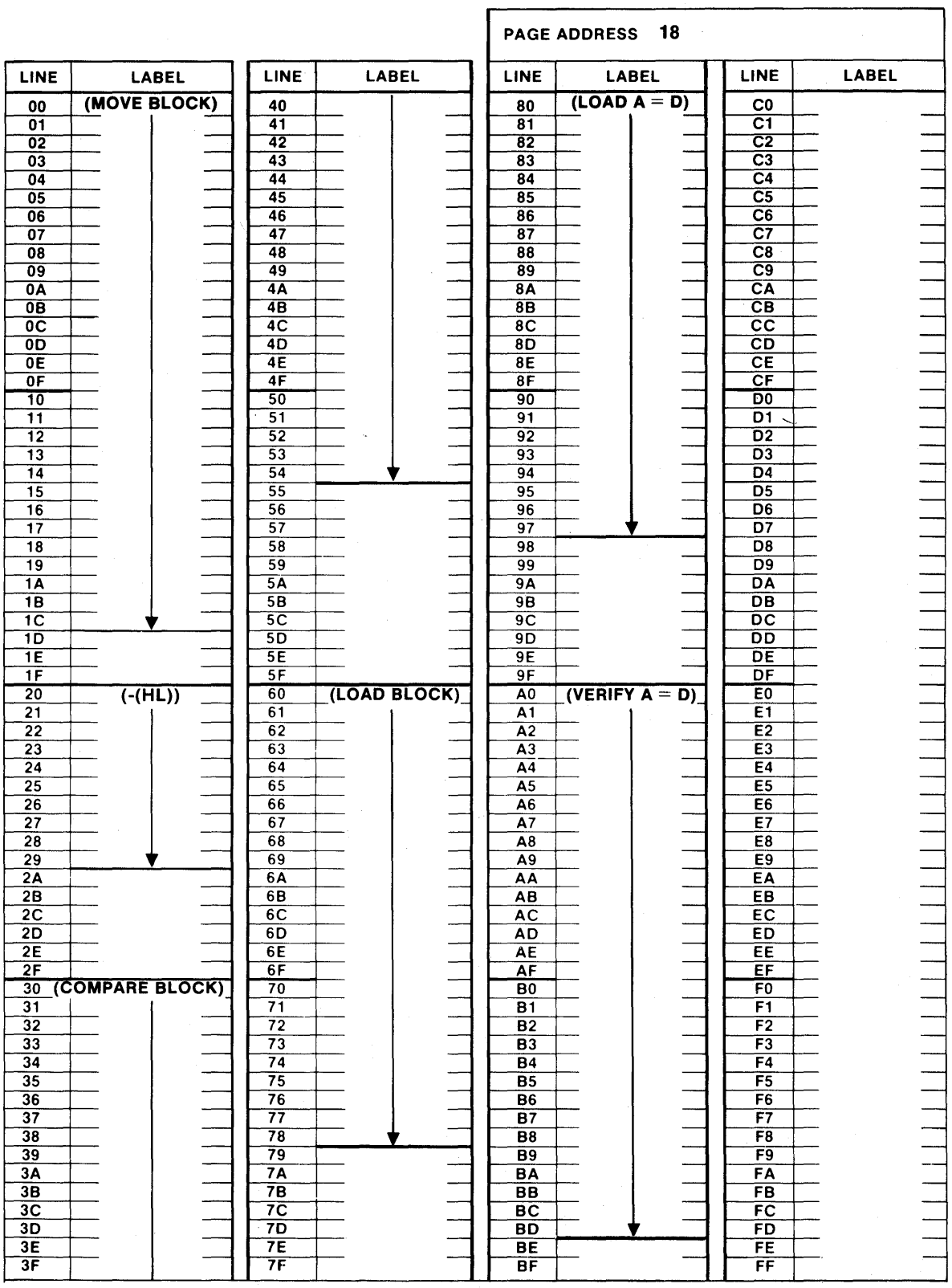


Figure 4-4. One-Page Memory Map for 7703 Software Package.

This subroutine moves a specified block of memory to a designated RAM area. The start and end addresses of the source block and the start address of the destination block must be specified in the calling program as follows:

ADR	JS	Cx
ADR+1	—	(MOVE BLOCK)
ADR+2	—	
ADR+3 ADR+4	mL mP	Source block start address
ADR+5 ADR+6	mL mP	Source block end address
ADR+7 ADR+8	mL mP	Destination block start address
ADR+9	..	Next instruction upon return from (MOVE BLOCK), where mL refers to a memory line address and mP refers to a memory page address.

(MOVE BLOCK) uses subroutine (-(HL))

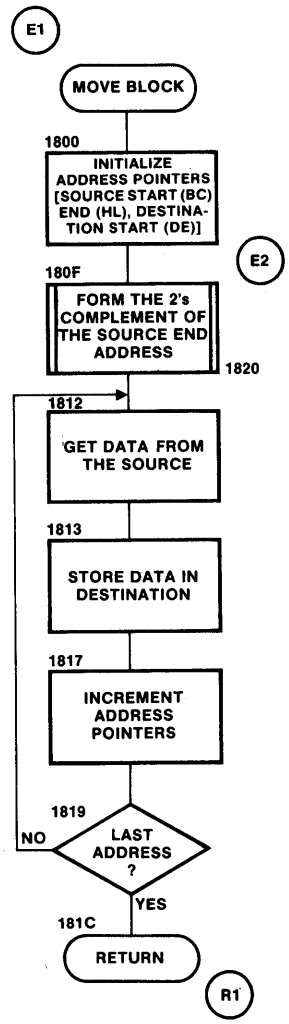


Figure 4-5. Flowchart - Subroutine (MOVE BLOCK) for 7703.

REGISTER AND MEMORY ALLOCATION				
PARAMETER		ENTRY REQUIREMENT	EXIT CONDITION	COMMENTS
ELEMENT	ADDRESS			
Register pair	BC	XX	??	
Register pair	DE	XX	??	
Register pair	HL	XX	??	
Register	A	XX	??	
Register	F	XX	??	

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-6. Register and Memory Allocation for 7703 Subroutine (MOVE BLOCK), Entry 1 and Return 1.

PROGRAM SPECIFICATIONS						
SYMBOL	PARAMETER		LIMITS		UNITS	COMMENTS
			MIN	MAX		
N_s	Stack memory		4		Bytes	Uses (-(HL))
N_p	Program memory		29		Bytes	
N_{pt}	Total program memory		39		Bytes	Uses (-(HL))
N_r	RAM memory		0		Bytes	
N_e	Execution time	8085	271 + (N-1)68		Time states	N = total number of bytes in the block.
		Z80	274 + (N-1)68			

Figure 4-7. Characteristics of 7703 Subroutine (MOVE BLOCK), Entry 1 and Return 1.

This subroutine forms the two's complement of the contents of the HL register pair. Enter this subroutine with the 16-bit value that is to be complemented in the HL register pair. The two's complement of the original value will be in the HL register pair upon exit from (-(HL)) .

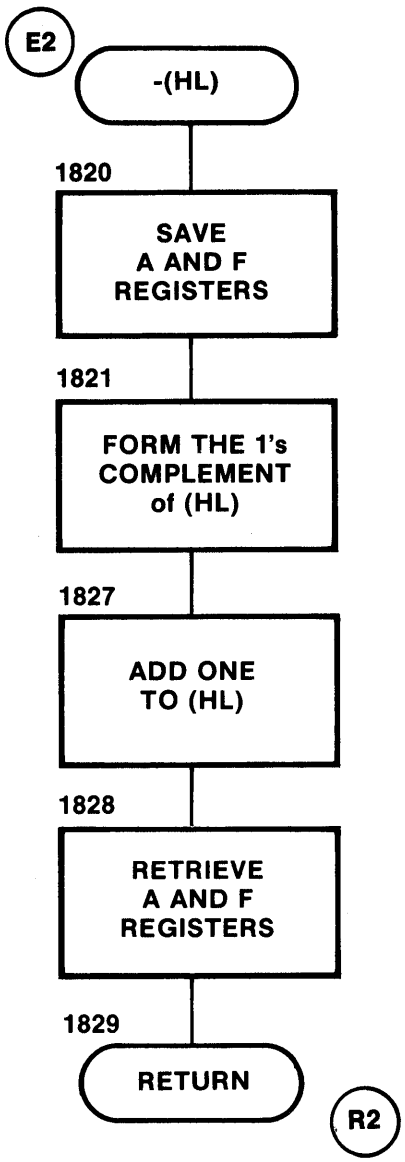


Figure 4-8. Flowchart - Subroutine (-(HL)) for 7703.

REGISTER AND MEMORY ALLOCATION				
PARAMETER		ENTRY REQUIREMENT	EXIT CONDITION	COMMENTS
ELEMENT	ADDRESS			
Register pair	HL	16-bit value to be 2's complemented	2's complement of original value	

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-9. Register and Memory Allocation for 7703 Subroutine (-(HL)), Entry 2 and Return 2.

PROGRAM SPECIFICATIONS						
SYMBOL	PARAMETER		LIMITS		UNITS	COMMENTS
			MIN	MAX		
N_s	Stack memory		2		Bytes	
N_p	Program memory		10		Bytes	
N_{pt}	Total program memory		10		Bytes	
N_r	RAM memory		0		Bytes	
N_e	Execution time	8085	62		Time states	
		Z80	68			

Figure 4-10. Characteristics of 7703 Subroutine (-(HL)), Entry 2 and Return 2.

This subroutine compares two blocks of memory. The start and end addresses of one block (the first block) and the start address of the other block (the second block) must be specified in the calling program as follows:

ADR	JS	Cx
ADR+1	—	(COMPARE BLOCK)
ADR+2	—	
ADR+3 ADR+4	mL mP	First block start address
ADR+5 ADR+6	mL mP	First block end address
ADR+7 ADR+8	mL mP	Second block start address
ADR+9	..	Next instruction upon return from (COMPARE BLOCK), where mL refers to a memory line address and mP refers to a memory page address.

(COMPARE BLOCK) uses subroutine (-(HL). It utilizes the carry flag to indicate whether or not the two blocks of memory are identical. If the two memory blocks are identical, the carry flag is cleared (C0) upon exit from (COMPARE BLOCK). If the two memory blocks are not the same, the carry flag is set (C1) upon exit from the subroutine. The BC register pair holds the address of the error location in the first block, the A register holds the data from the first block's error location, and the HL register pair holds the address of the error location in the second block.

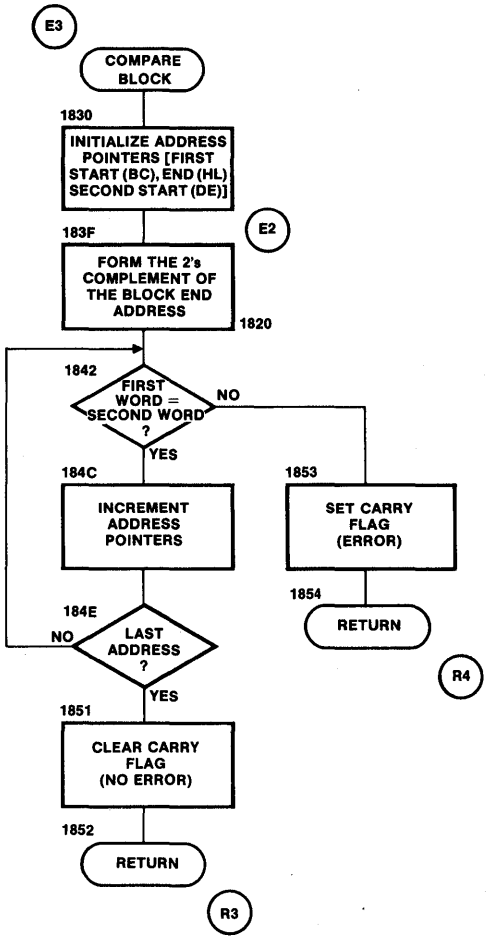


Figure 4-11. Flowchart - Subroutine (COMPARE BLOCK) for 7703.

REGISTER AND MEMORY ALLOCATION				
PARAMETER		ENTRY REQUIREMENT	EXIT CONDITION	COMMENTS
ELEMENT	ADDRESS			
Register pair	BC	XX	??	
Register pair	DE	XX	??	
Register pair	HL	XX	??	
Register pair	A	XX	??	
Register pair	F	XX	CO	The two blocks compared - **no** error.

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-12. Register and Memory Allocation for 7703 Subroutine (COMPARE BLOCK), Entry 3 and Return 3.

PROGRAM SPECIFICATIONS						
SYMBOL	PARAMETER		LIMITS		UNITS	COMMENTS
			MIN	MAX		
N_s	Stack memory		4		Bytes	Uses (-(HL))
N_p	Program memory		37		Bytes	
N_{pt}	Total program memory		47		Bytes	Uses (-(HL))
N_r	RAM memory		0		Bytes	
N_e	Execution time	8085	290 + (N-1)83		Time states	N = total number of bytes in the block.
		Z80	296 + (N-1)86			

Figure 4-13. Characteristics of 7703 Subroutine (COMPARE BLOCK), Entry 3 and Return 3.

REGISTER AND MEMORY ALLOCATION				
PARAMETER		ENTRY REQUIREMENT	EXIT CONDITION	COMMENTS
ELEMENT	ADDRESS			
Register pair	BC	XX	First block error address	
Register pair	DE	XX	??	
Register pair	HL	XX	Second block error address	
Register	A	XX	First block error data	
Register	F	XX	C1	Error - discrepancy in the two blocks.

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-14. Register and Memory Allocation for 7703 Subroutine (COMPARE BLOCK), Entry 3 and Return 4.

PROGRAM SPECIFICATIONS						
SYMBOL	PARAMETER		LIMITS		UNITS	COMMENTS
			MIN	MAX		
N_s	Stack memory		4		Bytes	Uses (-(HL))
N_p	Program memory		37		Bytes	
N_{pt}	Total program memory		47		Bytes	Uses (-(HL))
N_r	RAM memory		0		Bytes	
N_e	Execution time	8085	—		Time states	Execution time depends on error. No value to user.
		Z80	—			

Figure 4-15. Characteristics of 7703 Subroutine (COMPARE BLOCK), Entry 3 and Return 4.

This subroutine allows the user to load a designated block of memory with a designated data byte. The start and end addresses of the memory block and the data byte must be specified in the calling program as follows:

ADR	JS	Cx
ADR+1	—	(LOAD BLOCK)
ADR+2	—	
ADR+3 ADR+4	mL mP	Block start address
ADR+5 ADR+6	mL mP	Block end address
ADR+7	dd	Data byte to be loaded into memory block
ADR+8	..	Next instruction upon return from (LOAD BLOCK), where mL refers to a memory line address and mP refers to a memory page address.

(LOAD BLOCK) uses subroutine (-(HL)).

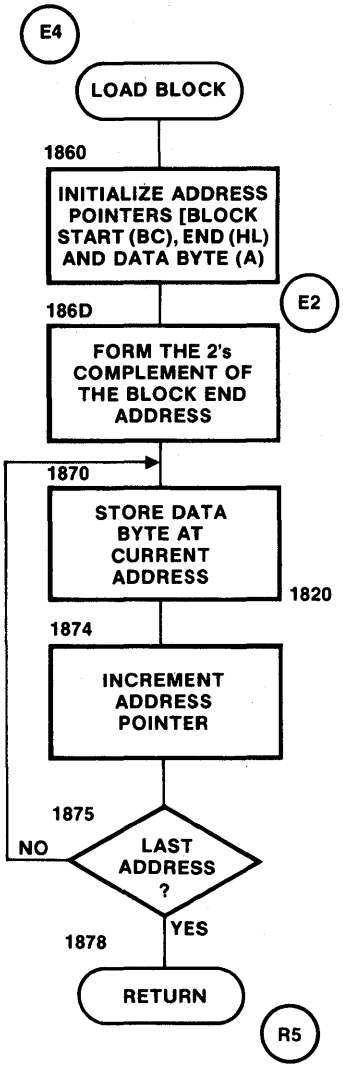


Figure 4-16. Flowchart - Subroutine (LOAD BLOCK) for 7703.

REGISTER AND MEMORY ALLOCATION				
PARAMETER		ENTRY REQUIREMENT	EXIT CONDITION	COMMENTS
ELEMENT	ADDRESS			
Register pair	BC	XX	??	
Register pair	DE	XX	??	
Register pair	HL	XX	??	
Register	A	XX	??	
Register	F	XX	??	

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-17. Register and Memory Allocation for 7703 Subroutine (LOAD BLOCK), Entry 4 and Return 5.

PROGRAM SPECIFICATIONS						
SYMBOL	PARAMETER		LIMITS		UNITS	COMMENTS
			MIN	MAX		
N_s	Stack memory		4		Bytes	Uses (-(HL))
N_p	Program memory		25		Bytes	
N_{pt}	Total program memory		35		Bytes	Uses (-(HL))
N_r	RAM memory		N		Bytes	
N_e	Execution time	8085	245 + (N-1)55		Time states	N = total number of bytes in the block.
		Z80	248 + (N-1)55			

Figure 4-18. Characteristics of 7703 Subroutine (LOAD BLOCK), Entry 4 and Return 5.

This subroutine loads a designated block of RAM memory with an "address equals data" format. The memory block's start and end addresses must be specified in the calling program as follows:

ADR	JS	Cx
ADR+1	—	(LOAD A = D)
ADR+2	—	
ADR+3 ADR+4	mL mP	Memory block start address
ADR+5 ADR+6	mL mP	Memory block end address
ADR+7	..	Next instruction upon return from (LOAD A = D), where mL refers to a memory line address and mP refers to a memory page address.

(LOAD A = D) uses subroutine (-(HL)).

The data loaded into each memory location is equal to the line address of that location.

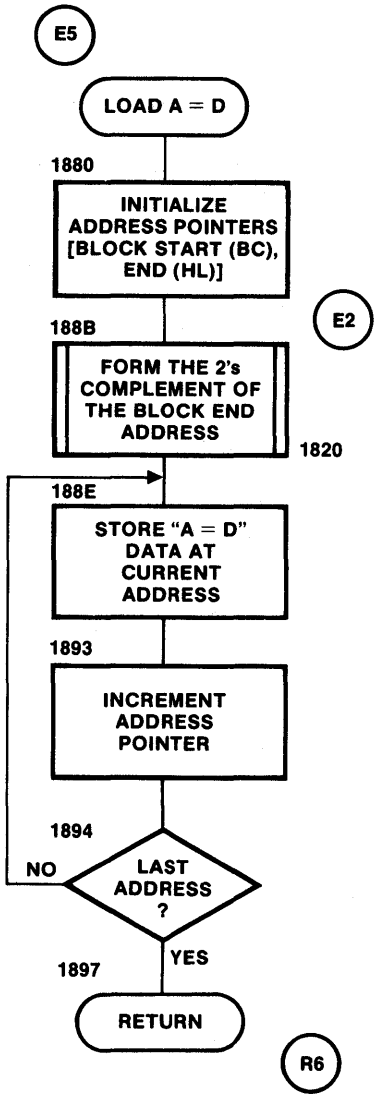


Figure 4-19. Flowchart - Subroutine (LOAD A = D) for 7703.

REGISTER AND MEMORY ALLOCATION				
PARAMETER		ENTRY REQUIREMENT	EXIT CONDITION	COMMENTS
ELEMENT	ADDRESS			
Register pair	BC	XX	??	
Register pair	DE	XX	??	
Register pair	HL	XX	??	
Register	A	XX	??	
Register	F	XX	??	

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-20. Register and Memory Allocation for 7703 Subroutine (LOAD A = D), Entry 5 and Return 6.

PROGRAM SPECIFICATIONS						
SYMBOL	PARAMETER		LIMITS		UNITS	COMMENTS
			MIN	MAX		
N_s	Stack memory		4		Bytes	Uses (-(HL))
N_p	Program memory		24		Bytes	
N_{pt}	Total program memory		34		Bytes	Uses (-(HL))
N_r	RAM memory		N		Bytes	
N_e	Execution time	8085	236 + (N-1)59		Time states	N = total number of bytes in the block.
		Z80	239 + (N-1)59			

Figure 4-21. Characteristics of 7703 Subroutine (LOAD A = D), Entry 5 and Return 6.

This subroutine tests a memory block for "address equals data" format. The start and end addresses of the memory block must be specified in the calling program as follows:

ADR	JS	Cx
ADR+1	—	(VERIFY A = D)
ADR+2	—	
ADR+3 ADR+4	mL mP	Memory block start address
ADR+5 ADR+6	mL mP	Memory block end address
ADR+7	..	Next instruction upon return from (VERIFY A = D), where mL refers to a memory line address and mP refers to a memory page address.

(VERIFY A = D) uses subroutine (-(HL)). It utilizes the carry flag to indicate whether or not the memory block is in the "address equals data" format. If the block contains all A = D data, the carry flag is cleared (C0) upon exit from (VERIFY A = D). If there is a location that does not have the A = D format, the carry flag is set (C1) upon exit from the subroutine. The BC register pair holds the address of the location with the error, and the A register holds the error data.

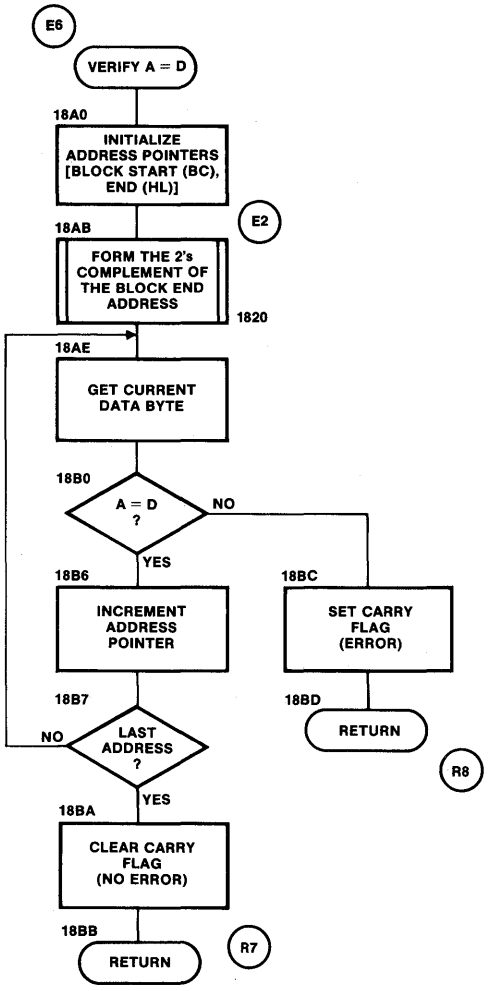


Figure 4-22. Flowchart - Subroutine (VERIFY A = D) for 7703.

REGISTER AND MEMORY ALLOCATION				
PARAMETER		ENTRY REQUIREMENT	EXIT CONDITION	COMMENTS
ELEMENT	ADDRESS			
Register pair	BC	XX	??	
Register pair	DE	XX	??	
Register pair	HL	XX	??	
Register	A	XX	??	
Register	F	XX	CO	A = D throughout block — **no** error.

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-23. Register and Memory Allocation for 7703 Subroutine (VERIFY A = D), Entry 6 and Return 7.

PROGRAM SPECIFICATIONS						
SYMBOL	PARAMETER		LIMITS		UNITS	COMMENTS
			MIN	MAX		
N_s	Stack memory		4		Bytes	Uses (-(HL))
N_p	Program memory		30		Bytes	
N_{pt}	Total program memory		40		Bytes	Uses (-(HL))
N_r	RAM memory		0		Bytes	
N_e	Execution time	8085	247 + (N-1)66		Time states	N = total number of bytes in the block.
		Z80	247 + (N-1)69			

Figure 4-24. Characteristics of 7703 Subroutine (VERIFY A = D), Entry 6 and Return 7.

REGISTER AND MEMORY ALLOCATION				
PARAMETER		ENTRY REQUIREMENT	EXIT CONDITION	COMMENTS
ELEMENT	ADDRESS			
Register pair	BC	XX	Address of error location	
Register pair	DE	XX	??	
Register pair	HL	XX	??	
Register	A	XX	Error data (A ≠ D)	
Register	F	XX	C1	Error, A ≠ D at same location.

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-25. Register and Memory Allocation for 7703 Subroutine (VERIFY A = D), Entry 6 and Return 8.

PROGRAM SPECIFICATIONS						
SYMBOL	PARAMETER		LIMITS		UNITS	COMMENTS
			MIN	MAX		
N_s	Stack memory		4		Bytes	Uses (-(HL))
N_p	Program memory		30		Bytes	
N_{pt}	Total program memory		40		Bytes	Uses (-(HL))
N_r	RAM memory		0		Bytes	
N_e	Execution time	8085	—		Time states	N = total number of bytes in the block.
		Z80	—			

Figure 4-26. Characteristics of 7703 Subroutine (VERIFY A = D), Entry 6 and Return 8.

Program Listing

Figure 4-27 shows the machine language code and the assembly language mnemonics, together with extensive comments, for all of the preceding subroutines.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR.	HEXADECIMAL LINE ADR.	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / DATE / COMMENTS
18	00	E1	(MOVE BLOCK)	PLP	HL	INITIALIZE SOURCE BLOCK START
	1	4E		LDCN	(HL)	ADDRESS.
	2	23		ICP	HL	
	3	46		LDBN	(HL)	
	4	23		ICP	HL	INITIALIZE SOURCE BLOCK END
	5	5E		LDEN	(HL)	ADDRESS.
	6	23		ICP	HL	
	7	56		LDDN	(HL)	
	8	D5		PSP	DE	SAVE SOURCE END ADDRESS.
	9	23		ICP	HL	INITIALIZE DESTINATION BLOCK START
	A	5E		LDEN	(HL)	ADDRESS.
	B	23		ICP	HL	
	C	56		LDDN	(HL)	
	D	23		ICP	HL	SAVE RETURN ADDRESS AND RETRIEVE
	E	E3		XCPT	HL	SOURCE END ADDRESS.
	F	CD		JS		NEGATE THE VALUE OF THE SOURCE
	10	20		-	(-(HL))	END ADDRESS.
	1	18		-		
	12	0A	NEXT	LDAN	(BC)	GET SOURCE DATA.
	3	12		STAN	(DE)	STORE SOURCE DATA AT DESTINATION.
	4	E5		PSP	HL	TEST FOR LAST ADDRESS OF BLOCK.
	5	09		ADP	HL, BC	
	6	E1		PLP	HL	
	7	03		ICP	BC	SET UP NEXT SOURCE AND DESTINATION
	8	13		ICP	DE	ADDRESSES.
	9	D2		JP	CO	LAST ADDRESS ?
	A	12		-	NEXT	NO, MOVE THE NEXT DATA WORD.
	B	18		-		
	C	C9		RTS		YES, RETURN.
	D					
	E					
	F					
18	20	F5	(-(HL))	PSP	AF	
	1	7C		LDA	H	FORM TWO'S COMPLEMENT OF THE
	2	2F		CMA		VALUE IN THE HL REGISTER
	3	67		LDH	A	PAIR.
	4	7D		LDA	L	(TWO'S COMPLEMENT = ONE'S COM-
	5	2F		CMA		PLEMENT + 1)
	6	6F		LDL	A	
	7	23		ICP	HL	
	8	F1		PLP	AF	
	9	C9		RTS		RETURN.
	A					
	B					
	C					
	D					
	E					
	F					
	30	E1	(COMPARE BLOCK)	PLP	HL	INITIALIZE FIRST BLOCK START
	1	4E		LDCN	(HL)	ADDRESS.
	2	23		ICP	HL	
	3	46		LDBN	(HL)	
	4	23		ICP	HL	INITIALIZE FIRST BLOCK END
	5	5E		LDEN	(HL)	ADDRESS.
	6	23		ICP	HL	
	7	56		LDDN	(HL)	
	8	D5		PSP	DE	SAVE BLOCK END ADDRESS.
	9	23		ICP	HL	INITIALIZE SECOND BLOCK START
	A	5E		LDEN	(HL)	ADDRESS.
	B	23		ICP	HL	
	C	56		LDDN	(HL)	
	D	23		ICP	HL	SAVE RETURN ADDRESS AND RETRIEVE
	E	E3		XCPT	HL	BLOCK END ADDRESS.
	F	CD		JS		NEGATE THE VALUE OF THE BLOCK

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Figure 4-27. Program Listing for 7703 Subroutines.

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS
18	40	20		–	(-(HL))	END ADDRESS.
	1	18		–		
	42	0A	SCAN	LDAN	(BC)	GET FIRST BLOCK DATA WORD.
	3	EB		XCP	HL,DE	COMPARE FIRST BLOCK DATA WITH
	4	BE		CPAN	(HL)	SECOND BLOCK DATA.
	5	C2		JP	≥0	FIRST DATA = SECOND DATA ?
	6	53		–	ERROR C	NO, ERROR.
	7	18		–		
	8	EB		XCP	HL,DE	YES, CHECK FOR LAST ADDRESS
	9	E5		PSP	HL	
	A	09		ADP	HL,BC	
	B	E1		PLP	HL	
	C	03		ICP	BC	SET UP NEXT ADDRESSES FOR FIRST
	D	13		ICP	DE	AND SECOND BLOCKS.
	E	D2		JP	C0	LAST ADDRESS ?
	F	42		–	SCAN	NO, COMPARE NEXT DATA WORDS.
	50	18		–		
	1	B7		CLC		YES, NO ERROR. (C0)
	2	C9		RTS		RETURN.
	53	37	ERROR C	SEC		ERROR. (C1)
	4	C9		RTS		RETURN. (FIRST BLOCK ERROR ADR, (BC); FIRST BLOCK ERROR DATA, (A); SECOND BLOCK ERROR ADR, (HL))
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					
18	60	E1	(LOAD BLOCK)	PLP	HL	INITIALIZE BLOCK START ADDRESS.
	1	4E		LDCN	(HL)	
	2	23		ICP	HL	
	3	46		LDBN	(HL)	
	4	23		ICP	HL	INITIALIZE BLOCK END ADDRESS.
	5	5E		LDEN	(HL)	
	6	23		ICP	HL	
	7	56		LDDN	(HL)	
	8	D5		PSP	DE	SAVE END ADDRESS.
	9	23		ICP	HL	GET DATA BYTE.
	A	7E		LDAN	(HL)	
	B	23		ICP	HL	SAVE RETURN ADDRESS AND RETRIEVE
	C	E3		XCPT	HL	END ADDRESS.
	D	CD		JS		NEGATE THE VALUE OF THE END
	E	20		–	(-(HL))	ADDRESS.
	F	18		–		
	70	02	REPEAT	STAN	(BC)	STORE DATA BYTE IN MEMORY.
	1	E5		PSP	HL	TEST FOR LAST ADDRESS OF BLOCK.
	2	09		ADP	HL,BC	
	3	E1		PLP	HL	
	4	03		ICP	BC	SET UP NEXT MEMORY ADDRESS.
	5	D2		JP	C0	LAST ADDRESS ?
	6	70		–	REPEAT	NO, LOAD NEXT LOCATION.
	7	18		–		
	8	C9		RTS		YES, RETURN.
	9					
	A					
	B					
	C					
	D					
	E					
	F					

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Figure 4-27. Program Listing for 7703 Subroutines (continued)

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS
18	80	E1	(LOAD A=D)	PLP	HL	INITIALIZE BLOCK START ADDRESS.
	1	4E		LDCN	(HL)	
	2	23		ICP	HL	
	3	46		LDBN	(HL)	
	4	23		ICP	HL	INITIALIZE BLOCK END ADDRESS.
	5	5E		LDEN	(HL)	
	6	23		ICP	HL	
	7	56		LDDN	(HL)	
	8	D5		PSP	DE	SAVE END ADDRESS.
	9	23		ICP	HL	SAVE RETURN ADDRESS AND RETRIEVE
	A	E3		XCPT	HL	END ADDRESS.
	B	CD		JS		NEGATE THE VALUE OF THE END
	C	20		—	(-(HL))	ADDRESS.
	D	18		—		
	8E	79	LOOP	LDA	C	DATA = MEMORY LINE ADDRESS.
	F	02		STAN	(BC)	STORE DATA BYTE IN MEMORY. (A=D)
	90	E5		PSP	HL	TEST FOR LAST ADDRESS.
	1	09		ADP	HL, BC	
	2	E1		PLP	HL	
	3	03		ICP	BC	SET UP NEXT MEMORY ADDRESS.
	4	D2		JP	CO	LAST ADDRESS?
	5	8E		—	LOOP	NO, LOAD NEXT LOCATION.
	6	18		—		
	7	C9		RTS		YES, RETURN.
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					
18	A0	E1	(VERIFY A=D)	PLP	HL	INITIALIZE BLOCK START ADDRESS.
	1	4E		LDCN	(HL)	
	2	23		ICP	HL	
	3	46		LDBN	(HL)	
	4	23		ICP	HL	INITIALIZE BLOCK END ADDRESS.
	5	5E		LDEN	(HL)	
	6	23		ICP	HL	
	7	56		LDDN	(HL)	
	8	D5		PSP	DE	SAVE END ADDRESS.
	9	23		ICP	HL	SAVE RETURN ADDRESS AND RETRIEVE
	A	E3		XCPT	HL	END ADDRESS.
	B	CD		JS		NEGATE THE VALUE OF THE END
	C	20		—	(-(HL))	ADDRESS.
	D	18		—		
	AE	0A	AGAIN	LDAN	(BC)	GET CURRENT DATA BYTE
	F	B9		CPA	C	ADDRESS = DATA FORMAT?
	B0	C2		JP	≠0	NO, ERROR.
	1	BC		—	ERROR A	
	2	18		—		
	3	E5		PSP	HL	YES, TEST FOR LAST ADDRESS.
	4	09		ADP	HL, BC	
	5	E1		PLP	HL	
	6	03		ICP	BC	SET UP NEXT MEMORY ADDRESS.
	7	D2		JP	CO	LAST ADDRESS?
	8	AE		—	AGAIN	NO, CHECK NEXT DATA BYTE.
	9	18		—		
	A	B7		CLC		YES, NO ERROR. (CO)
	B	C9		RTS		RETURN.
	BC	37	ERROR A	SEC		ERROR. (C1)
	D	C9		RTS		RETURN. {ERROR ADDRESS, (BC) {ERROR DATA, (A)
	E					
	F					

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Figure 4-27. Program Listing for 7703 Subroutines (continued)

Demonstration/Test Program:
Shakedown (Confidence Level) Test Start Address: 0000

This program provides a quick test of the 7703 RAM. It programs all RAM bits with different patterns and tests for valid data, giving the user a level of confidence in the 7703.

The program loads and tests for a known data pattern in the 7703 RAM, then loads and tests for a new data pattern, and finally loads and tests for the complement of the second data pattern.

Error routines store any error parameters (address of memory location with error, data contained in the error location). If there are no errors for a particular segment of the program, the program stores zeros for the error addresses and data. Error data may be examined with a user-provided routine, which should test the error storage locations to determine whether an error occurred. The user's routine must provide a means of displaying or communicating any error data.

This program uses all of the subroutines presented in the preceding pages. RAM locations 2110 through 211E, inclusive, are used as error storage locations.

> NOTE
>
> This is a demonstration/test program; it is not a subroutine.

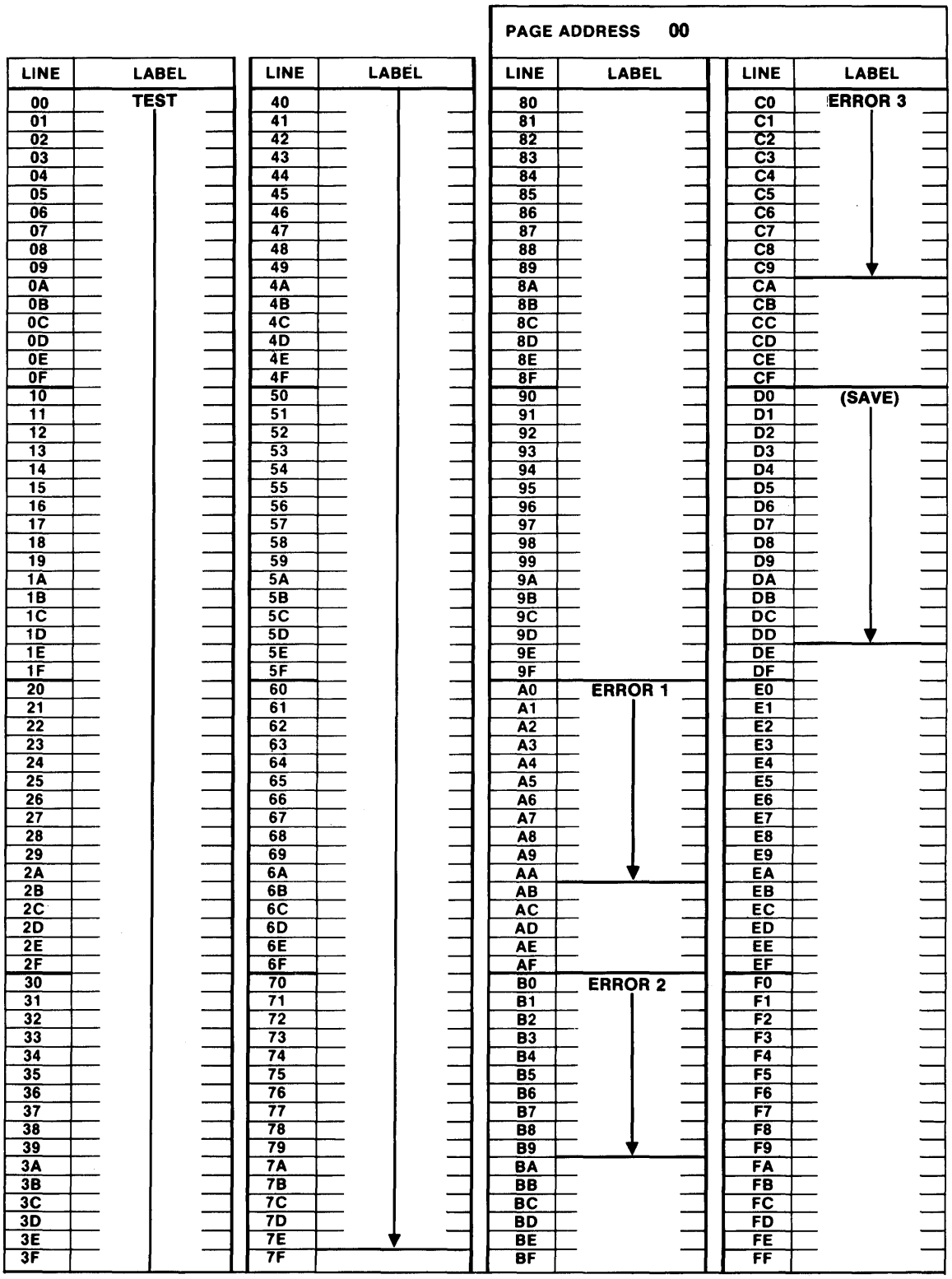

Figure 4-28. Memory Map for Shakedown (Confidence Level) Test — 7703.

PAGE ADDRESS 21

LINE	LABEL
00	
01	
02	
03	
04	
05	
06	
07	
08	
09	
0A	
0B	
0C	
0D	
0E	
0F	
10	ERROR 1 DATA
11	
12	
13	ERROR 2 DATA
14	
15	
16	
17	
18	
19	ERROR 3 DATA
1A	
1B	
1C	
1D	
1E	
1F	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
2A	
2B	
2C	
2D	
2E	
2F	
30	
31	
32	
33	
34	
35	
36	
37	
38	
39	
3A	
3B	
3C	
3D	
3E	
3F	

LINE	LABEL
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
4A	
4B	
4C	
4D	
4E	
4F	
50	
51	
52	
53	
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58	
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5A	
5B	
5C	
5D	
5E	
5F	
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6A	
6B	
6C	
6D	
6E	
6F	
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72	
73	
74	
75	
76	
77	
78	
79	
7A	
7B	
7C	
7D	
7E	
7F	

LINE	LABEL
80	
81	
82	
83	
84	
85	
86	
87	
88	
89	
8A	
8B	
8C	
8D	
8E	
8F	
90	
91	
92	
93	
94	
95	
96	
97	
98	
99	
9A	
9B	
9C	
9D	
9E	
9F	
A0	
A1	
A2	
A3	
A4	
A5	
A6	
A7	
A8	
A9	
AA	
AB	
AC	
AD	
AE	
AF	
B0	
B1	
B2	
B3	
B4	
B5	
B6	
B7	
B8	
B9	
BA	
BB	
BC	
BD	
BE	
BF	

LINE	LABEL
C0	
C1	
C2	
C3	
C4	
C5	
C6	
C7	
C8	
C9	
CA	
CB	
CC	
CD	
CE	
CF	
D0	
D1	
D2	
D3	
D4	
D5	
D6	
D7	
D8	
D9	
DA	
DB	
DC	
DD	
DE	
DF	
E0	
E1	
E2	
E3	
E4	
E5	
E6	
E7	
E8	
E9	
EA	
EB	
EC	
ED	
EE	
EF	
F0	
F1	
F2	
F3	
F4	
F5	
F6	
F7	
F8	
F9	
FA	
FB	
FC	
FD	
FE	
FF	

Figure 4-29. Memory Map for Error Storage Locations (Shakedown Test) — 7703.

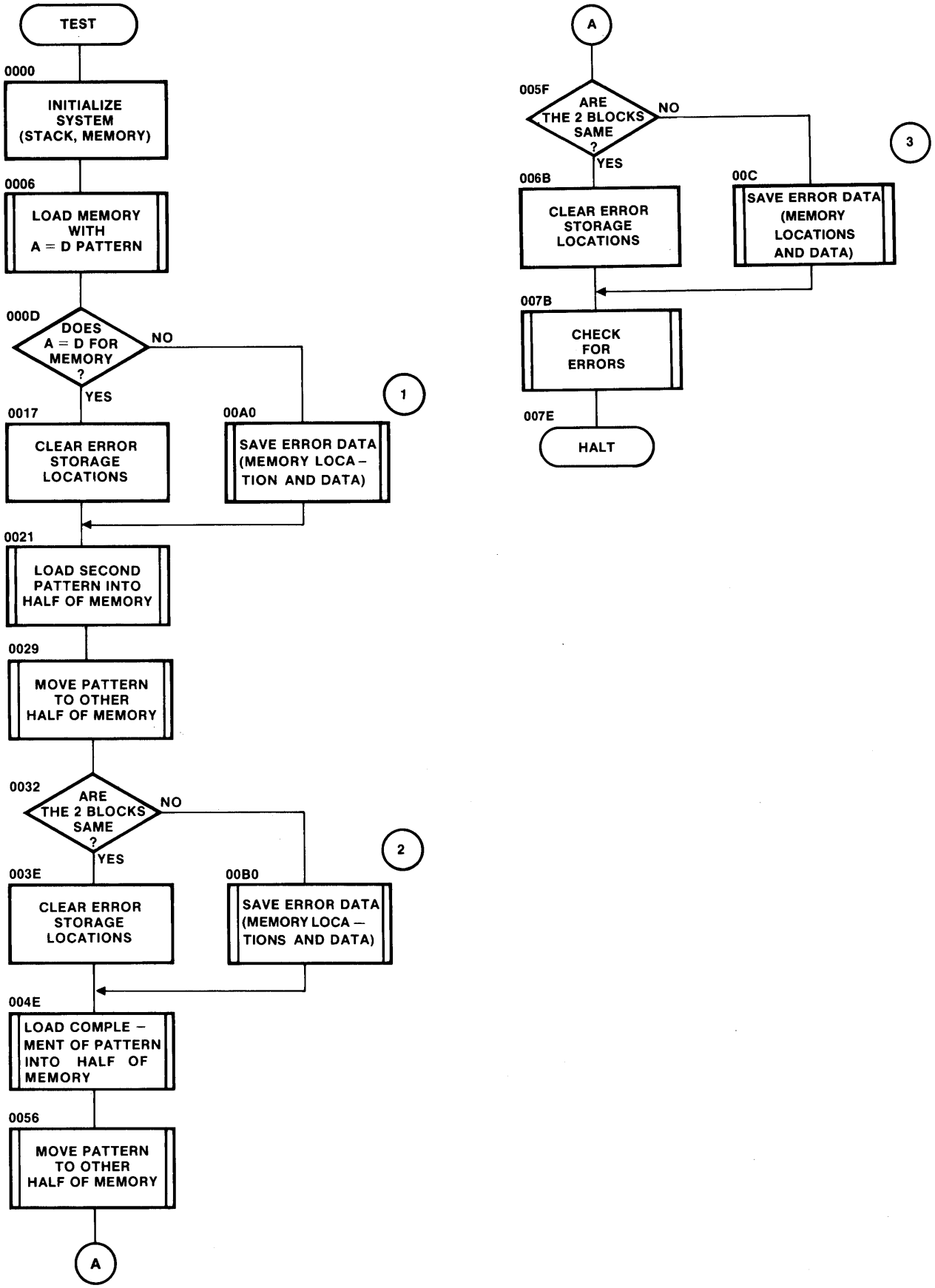

Figure 4-30. Flowchart — Demonstration/Test Program for 7703.

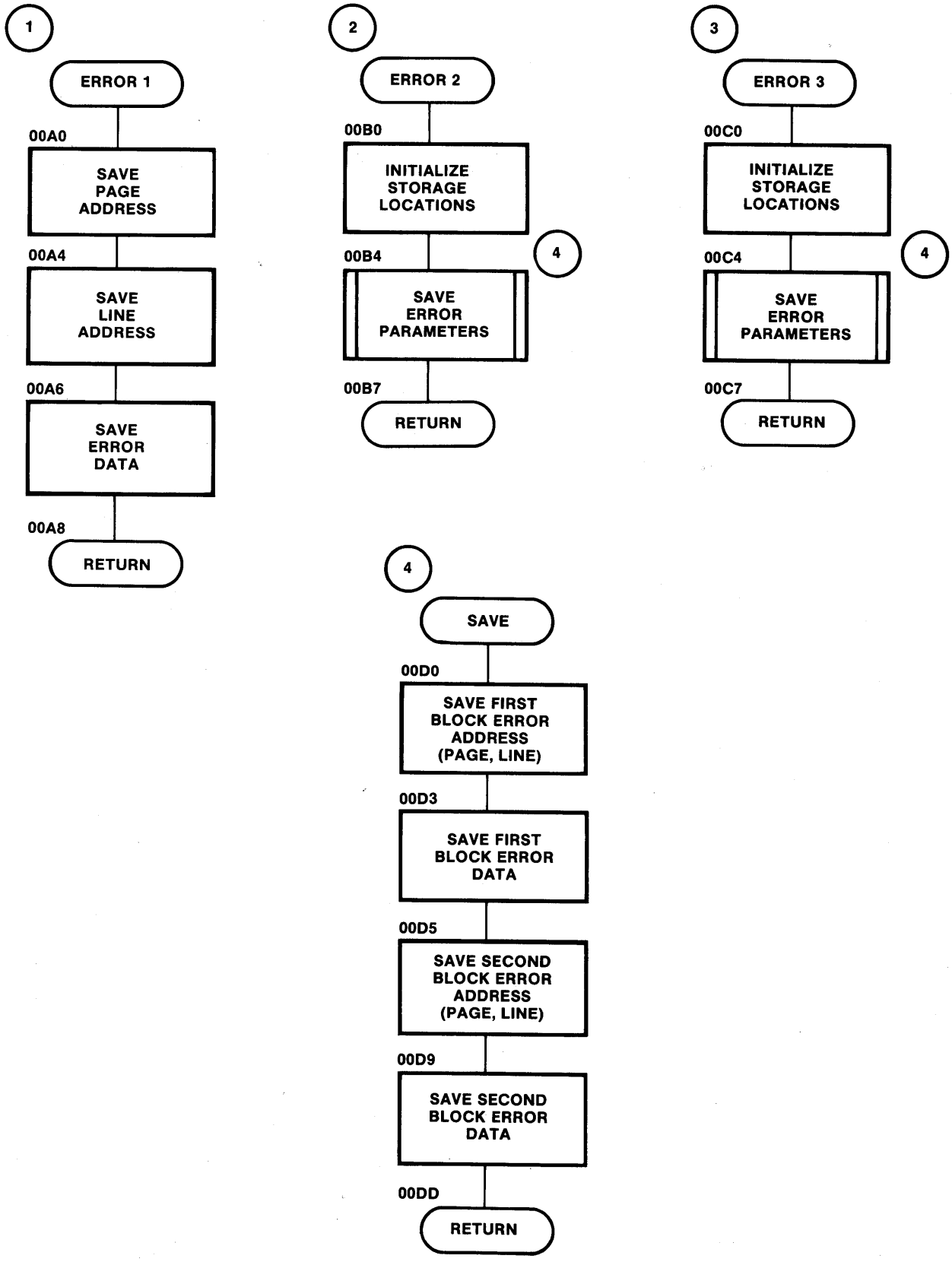

Figure 4-30. Flowchart—Demonstration/Test Program for 7703 (continued).

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PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS
						TITLE DATE
00	00	31	TEST	LDPI	SP	INITIALIZE STACK
	1	00		–	2100	
	2	21		–		
	3	3A		LDAD		PERFORM MEMORY REFERENCE (TO SET
	4	00		–	C000	OPERATE FLIP FLOP ON 7703 CARD)
	5	C0		–		
	6	CD		JS		LOAD 7703 MEMORY (16K IN THIS CASE)
	7	80		–	(LOAD A=D)	WITH A=D DATA PATTERN
	8	18		–		
	9	00		–	C000	
	A	C0		–		
	B	FF		–	FFFF	
	C	FF		–		
	D	CD		JS		DOES MEMORY CONTAIN A=D PATTERN?
	E	A0		–	(VERIFY A=D)	
	F	18		–		
	10	00		–	C000	
	1	C0		–		
	2	FF		–	FFFF	
	3	FF		–		
	4	DA		JP	C1	NO, SAVE ERROR PARAMETERS
	5	A0		–	ERROR 1	
	6	00		–		
	7	21		LDPI	HL	YES, CLEAR THE ERROR STORAGE
	8	10		–	2110	LOCATIONS
	9	21		–		(2110, 2111, 2112)
	A	3E		LDAI		
	B	00		–	00	
	C	77		STAN	(HL)	
	D	23		ICP	HL	
	E	77		STAN	(HL)	
	F	23		ICP	HL	
00	20	77		STAN	(HL)	
	21	CD	NEW PATTERN	JS		LOAD HALF OF MEMORY WITH DATA
	2	60		–	(LOAD BLOCK)	PATTERN
	3	18		–		(10101010 = AA H)
	4	00		–	C000	
	5	C0		–		
	6	FF		–	DFFF	
	7	DF		–		
	8	AA		–	AA	
	9	CD		JS		MOVE PATTERN TO OTHER HALF OF
	A	00		–	(MOVE BLOCK)	MEMORY
	B	18		–		
	C	00		–	C000	
	D	C0		–		
	E	FF		–	DFFF	
	F	DF		–		
	30	00		–	E000	
	1	E0		–		
	2	CD		JS		ARE THE TWO MEMORY BLOCKS THE
	3	30		–	(COMPARE BLOCK)	SAME?
	4	18		–		
	5	00		–	C000	
	6	C0		–		
	7	FF		–	DFFF	
	8	DF		–		
	9	00		–	E000	
	A	E0		–		
	B	DA		JP	C1	NO, SAVE ERROR PARAMETERS
	C	B0		–	ERROR 2	
	D	00		–		
	E	21		LDPI	HL	YES, CLEAR THE ERROR STORAGE
	F	13		–	2113	LOCATIONS

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Figure 4-31. Program Listing for 7703 Shakedown (Confidence Level) Test .

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / DATE / COMMENTS
00	40	21		—		(2113, 2114, 2115, 2116, 2117
	1	3E		LDAI		2118)
	2	00		—	00	
	3	77		STAN	(HL)	
	4	23		ICP	HL	
	5	77		STAN	(HL)	
	6	23		ICP	HL	
	7	77		STAN	(HL)	
	8	23		ICP	HL	
	9	77		STAN	(HL)	
	A	23		ICP	HL	
	B	77		STAN	(HL)	
	C	23		ICP	HL	
	D	77		STAN	(HL)	
	4E	CD	INVERT PATTERN	JS		— LOAD HALF OF MEMORY WITH COMPLEMENT
	F	60		—	(LOAD BLOCK)	OF LAST DATA PATTERN
	50	18		—		(01010101 = 55H)
	1	00		—	C000	
	2	C0		—		
	3	FF		—	DFFF	
	4	DF		—		
	5	55		—	55	
	6	CD		JS		— MOVE PATTERN TO OTHER HALF OF
	7	00		—	(MOVE BLOCK)	MEMORY
	8	18		—		
	9	00		—	C000	
	A	C0		—		
	B	FF		—	DFFF	
	C	DF		—		
	D	00		—	E000	
	E	E0		—		
	F	CD		JS		— ARE THE TWO MEMORY BLOCKS THE
00	60	30		—	(COMPARE BLOCK)	SAME?
	1	18		—		
	2	00		—	C000	
	3	C0		—		
	4	FF		—	DFFF	
	5	DF		—		
	6	00		—	E000	
	7	E0		—		
	8	DA		JP	C1	— NO, SAVE ERROR PARAMETERS
	9	C0		—	ERROR 3	
	A	00		—		
	B	21		LDPI	HL	— YES, CLEAR THE ERROR STORAGE
	C	19		—	2119	LOCATIONS
	D	21		—		(2119, 211A, 211B, 211C, 211D,
	E	3E		LDAI		211E)
	F	00		—	00	
	70	77		STAN	(HL)	
	1	23		ICP	HL	
	2	77		STAN	(HL)	
	3	23		ICP	HL	
	4	77		STAN	(HL)	
	5	23		ICP	HL	
	6	77		STAN	(HL)	
	7	23		ICP	HL	
	8	77		STAN	(HL)	
	9	23		ICP	HL	
	A	77		STAN	(HL)	
	7B	CD	CHECK	JS		— TEST FINISHED. EXAMINE ERROR STOR-
	C			—	(CHECK ERROR)	AGE LOCATIONS TO DETERMINE ERROR
	D			—		CONDITIONS.
	E	76		HLT		
	F					

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Figure 4-31. Program Listing for 7703 Shakedown (Confidence Level) Test (continued).

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS	DATE
00	80						
	81						
	82						
	83						
	84						
	85						
	86						
	87						
	88						
	89						
	8A						
	8B						
	8C						
	8D						
	8E						
	8F						
	90						
	91						
	92						
	93						
	94						
	95						
	96						
	97						
	98						
	99						
	9A						
	9B						
	9C						
	9D						
	9E						
	9F						
00	A0	21	ERROR 1	LDPI	HL	SAVE ERROR LOCATION PAGE ADDRESS	
	A1	10		—	2110		
	A2	21		—			
	A3	70		STBN	(HL)		
	A4	23		ICP	HL	SAVE ERROR LOCATION LINE ADDRESS	
	A5	71		STCN	(HL)		
	A6	23		ICP	HL	SAVE ERROR DATA	
	A7	77		STAN	(HL)		
	A8	C3		JP		RETURN	
	A9	21		—	NEW PATTERN		
	AA	00		—			
	AB						
	AC						
	AD						
	AE						
	AF						
	B0	EB	ERROR 2	XCP	HL, DE	SAVE SECOND BLOCK ERROR ADDRESS	
	B1	21		LDPI	HL	INITIALIZE ERROR STORAGE LOCATIONS	
	B2	13		—	2113		
	B3	21		—			
	B4	CD		JS		SAVE ERROR PARAMETERS	
	B5	D0		—	(SAVE)		
	B6	00		—			
	B7	C3		JP		RETURN	
	B8	4E		—	INVERT PATTERN		
	B9	00		—			
	BA						
	BB						
	BC						
	BD						
	BE						
	BF						

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Figure 4-31. Program Listing for 7703 Shakedown (Confidence Level) Test (continued).

PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR.	HEXADECIMAL LINE ADR.	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS
00	C0	EB	ERROR3	XCP	HL, DE	SAVE SECOND BLOCK ERROR ADDRESS
	1	21		LDPI	HL	INITIALIZE ERROR STORAGE LOCATIONS
	2	19		—	2119	
	3	21		—		
	4	CD		JS		SAVE ERROR PARAMETERS
	5	DO		—	(SAVE)	
	6	00		—		
	7	C3		JP		RETURN
	8	7B		—	CHECK	
	9	00		—		
	A					
	B					
	C					
	D					
	E					
	F					
	D0	70	(SAVE)	STBN	(HL)	SAVE FIRST BLOCK ERROR PAGE ADDRESS
	1	23		ICP	HL	SAVE FIRST BLOCK ERROR LINE ADDRESS
	2	71		STCN	(HL)	
	3	23		ICP	HL	SAVE FIRST BLOCK ERROR DATA
	4	77		STAN	(HL)	
	5	23		ICP	HL	SAVE SECOND BLOCK ERROR PAGE ADDRESS
	6	72		STDN	(HL)	
	7	23		ICP	HL	SAVE SECOND BLOCK ERROR LINE ADDRESS
	8	73		STEN	(HL)	
	9	23		ICP	HL	RESTORE SECOND BLOCK ERROR ADDRESS
	A	EB		XCP	HL, DE	
	B	7E		LDAN	(HL)	RETRIEVE SECOND BLOCK ERROR DATA
	C	12		STAN	(DE)	AND SAVE IT
	D	C9		RTS		RETURN
	E					
	F					
00	E0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					
	F0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

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Figure 4-31. Program Listing for 7703 Shakedown (Confidence Level) Test (continued).

SECTION 5
Maintenance

Reference Drawings

The schematic (Fig. 5-1) and assembly drawing (Fig. 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. They may differ in some respects from the card and documentation that the user received from Pro-Log. The schematic and assembly drawings shipped by Pro-Log with the card are those from which the card was manufactured.

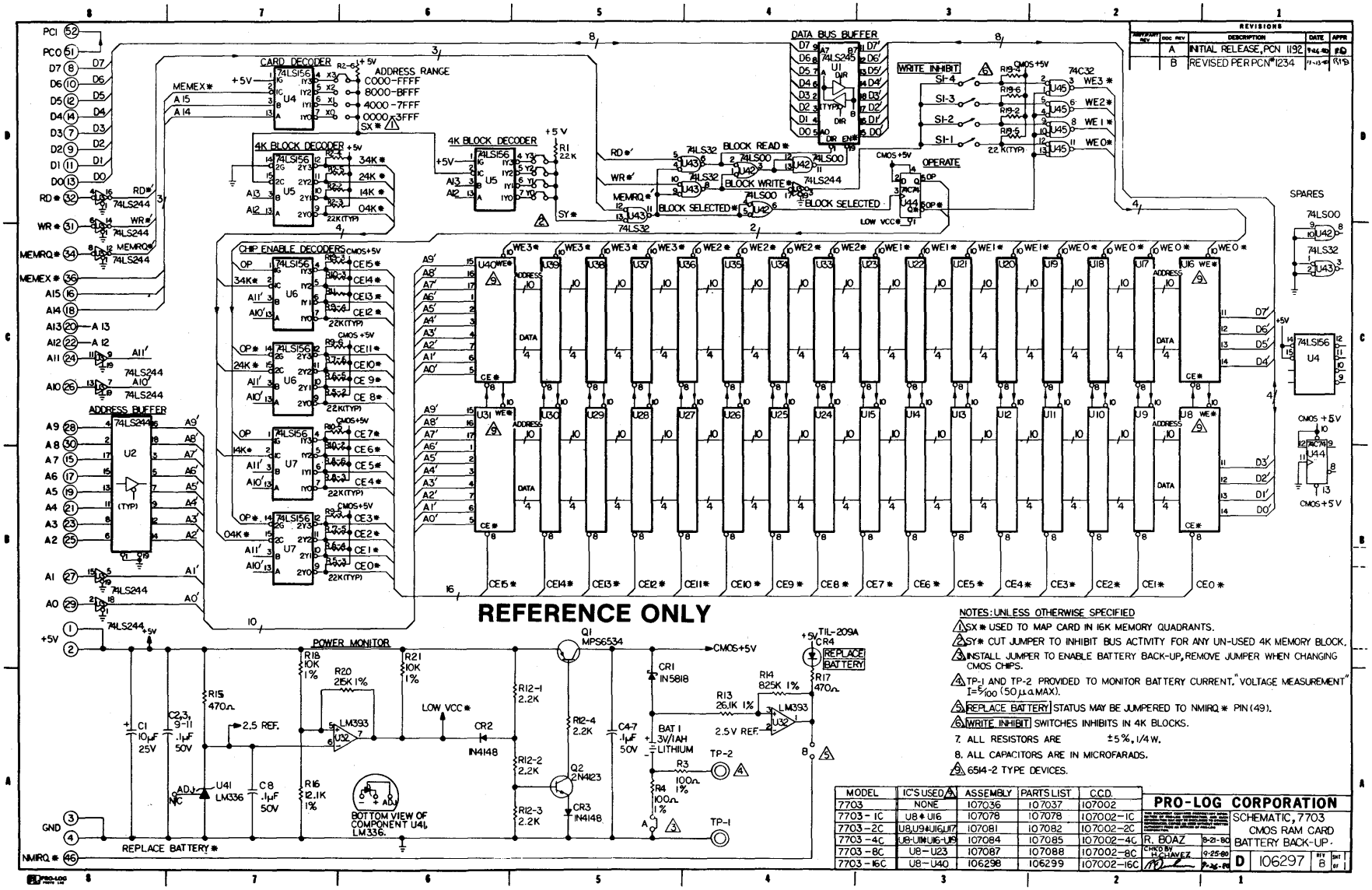


Figure 5-1. Schematic for 7703 (Reference Only).

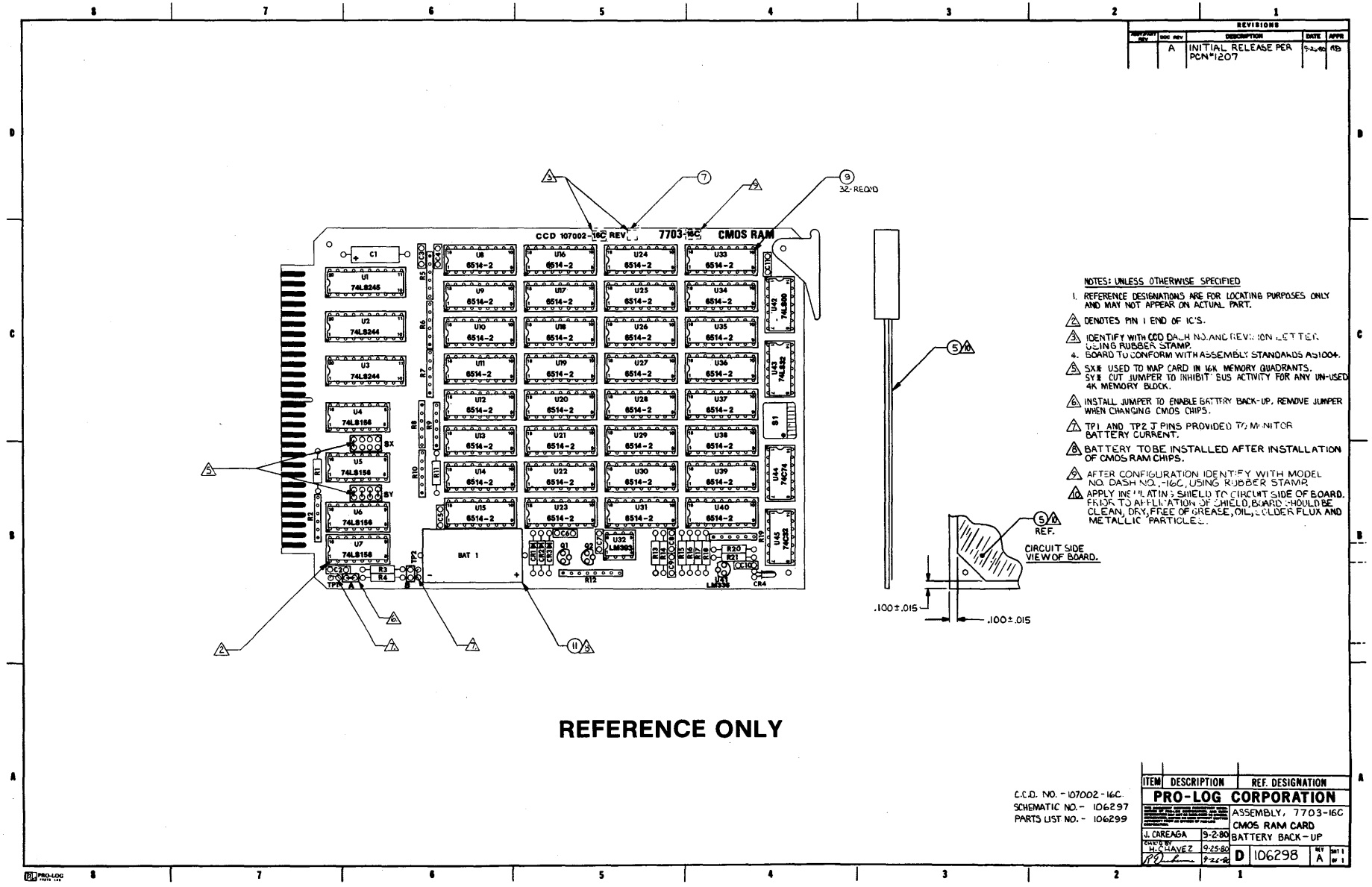


Figure 5-2. Assembly for 7703 (Reference Only).

Card Layout

Figure 5-3 shows the physical location of the 7703's main components: the various switches, indicators, and jumpers on the card. The functions of the various components are identified. Note the position of pin 1 on the RAM elements and the other ICs. When replacing chips, be careful to insert them only with pin 1 positioned as shown in the figure; also, make sure that no pins are bent beneath the body of the chip.

CAUTION

Remove jumper A from the battery-enable pad before removing or replacing any RAM chips on the 7703 card. After RAM chip removal and/or replacement, replace Jumper A before reinserting card into the card cage connector. If jumper A is not replaced, the contents of the RAM on the 7703 card are destroyed.

Read Timing Diagram

Figure 5-4 displays a read timing diagram for a Z80-based CPU. The timing sequence is based on a 400-ns clock. Because of slow propagation time through the read and write decoding circuitry, do not use the 7703 with 4-MHz (or faster) CPU cards.

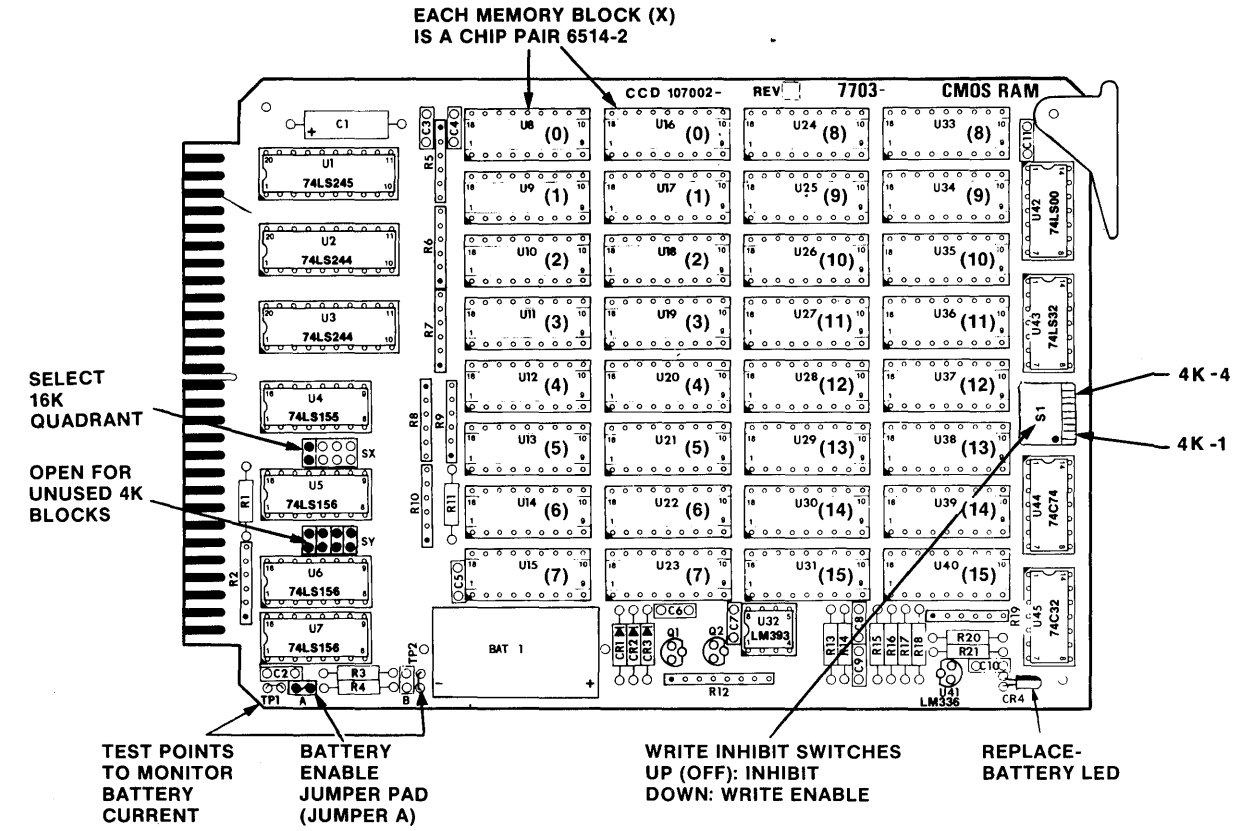


Figure 5-3. Location and Functions of Main Components for 7703.

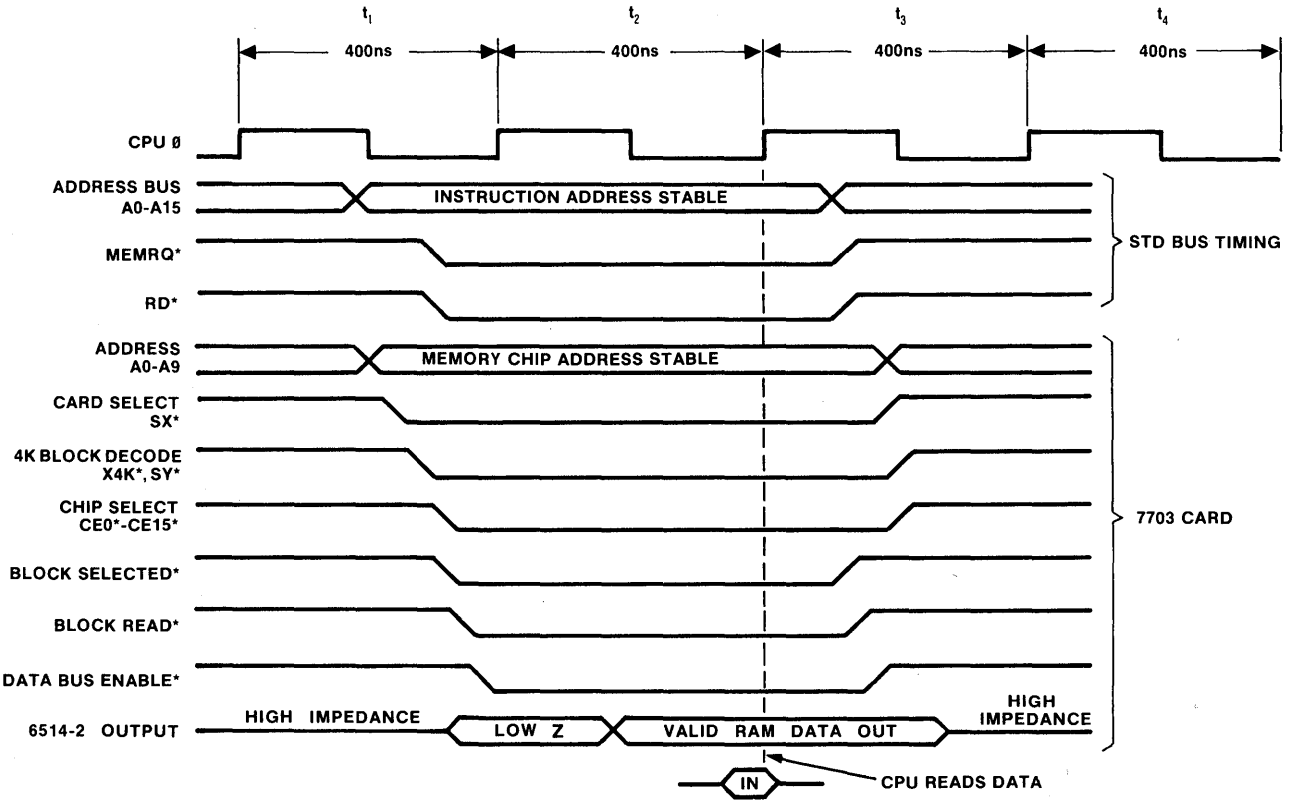


Figure 5-4. Read Timing Diagram for 7703 (used with Pro-Log's 7803 2.5-MHz Z80 CPU card).

Address Decoding Circuit

See Fig. 5-5. Address lines A15 and A14 are decoded by U4 to select the 16K memory space in which the 7703 operates. A15 and A14 decode the 64K address space as shown in Fig. 5-6.

The 16K address range that the 7703 will respond to is determined by the jumpering of SX as indicated in Fig. 5-6 and as specified in Section 2. Jumper SX is in the X3 position when the 7703 is initially shipped to you from the factory.

Address lines A13 and A12 are decoded by U5 to select the active 4K block from the 16K bank controlled by A15 and A14. The outputs from one-half of U5 are wire-ORed together to form the SY* signal, which must be active to access the selected 4K block. The unused 4K block or blocks are disabled by cutting one or more of the traces at SY0, SY1, SY2, or SY3. The outputs from the other half of U5 are used in the chip-enable decoding operation.

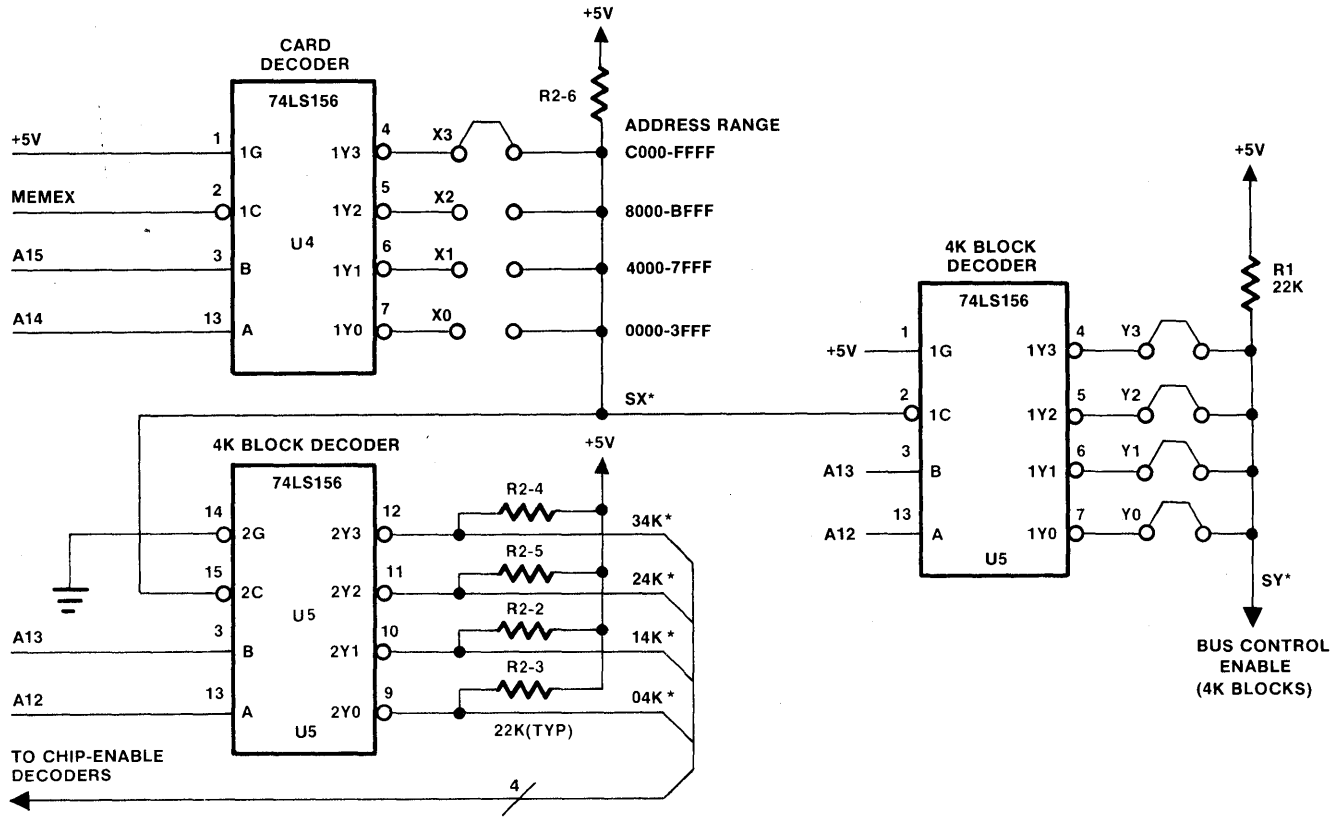


Figure 5-5. Address Decoding Circuit for 7703.

ADDRESS LINE A15	ADDRESS LINE A14	MEMORY ADDRESS RANGE	SX JUMPERS
0	0	0000-3FFF	X0
0	1	4000-7FFF	X1
1	0	8000-BFFF	X2
1	1	C000-FFFF	X3

Figure 5-6. Decoding the 7703's 64K Address Space.

Chip-Enable Decoding Circuit

See Fig. 5-7. The block enables generated by U5 (04K, 14K, 24K, and 34K) are decoded (with address lines A11 and A10) by U6 and U7. The CEX* signals select the 1K byte RAM pair that is to be accessed. (Fig. 5-8).

Signal OP is derived from the operate flip-flop, which is reset by power failure, or by power-up and power-down of the system. U6 and U7 are open collector devices and are pulled up to CMOS +5V.

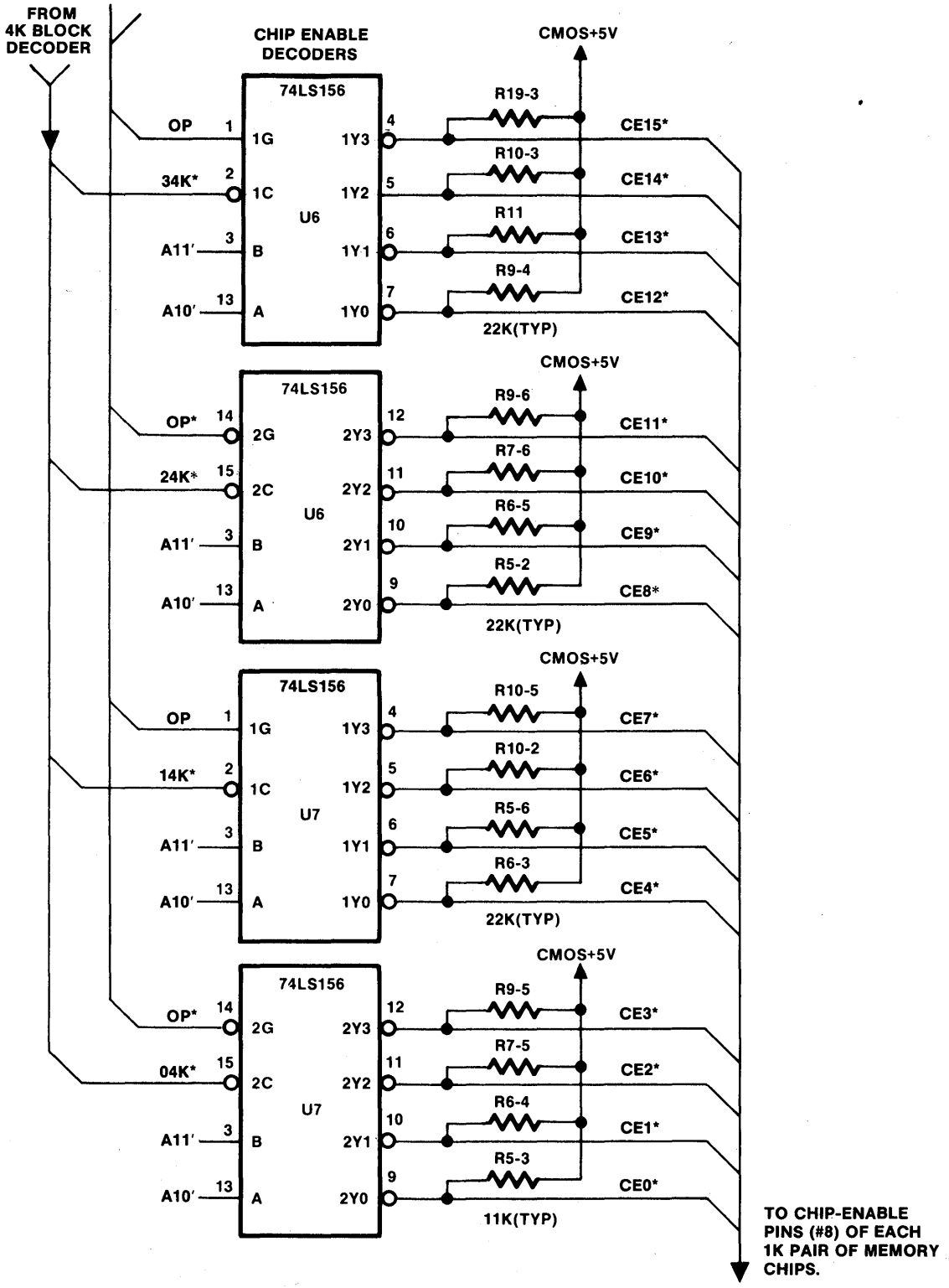


Figure 5-7. Chip-Enable Decoding Circuit for 7703.

OPERATE SIGNAL	X4K	CEX*	4K SELECTED
OP* - 0	04K	CE0*-3 *	Lowest
OP - 1	14K	CE4*-7 *	Next lowest
OP* - 0	24K	CE8*-11*	Next to highest
OP - 1	34K	CE12*-15*	Highest

Figure 5-8. CEX* Signal Selection of 1K Byte RAM Pair to be Accessed — 7703.

Data Bus Buffer Circuit

See Fig. 5-9. The 7703 data bus buffering and directional control are provided by U1, which is a three-state bidirectional bus controller. When the read (RD*) signal is active and when SY* and MEMRQ* are both active, U1 is enabled to pass data from the 7703 card to the STD BUS (i.e., read operation). When the RD* signal is inactive and when WR*, SY*, and MEMRQ* are all active, U1 allows data to be transferred from the STD BUS to the 7703 card (write operation). Otherwise, U1 is in a high impedance state.

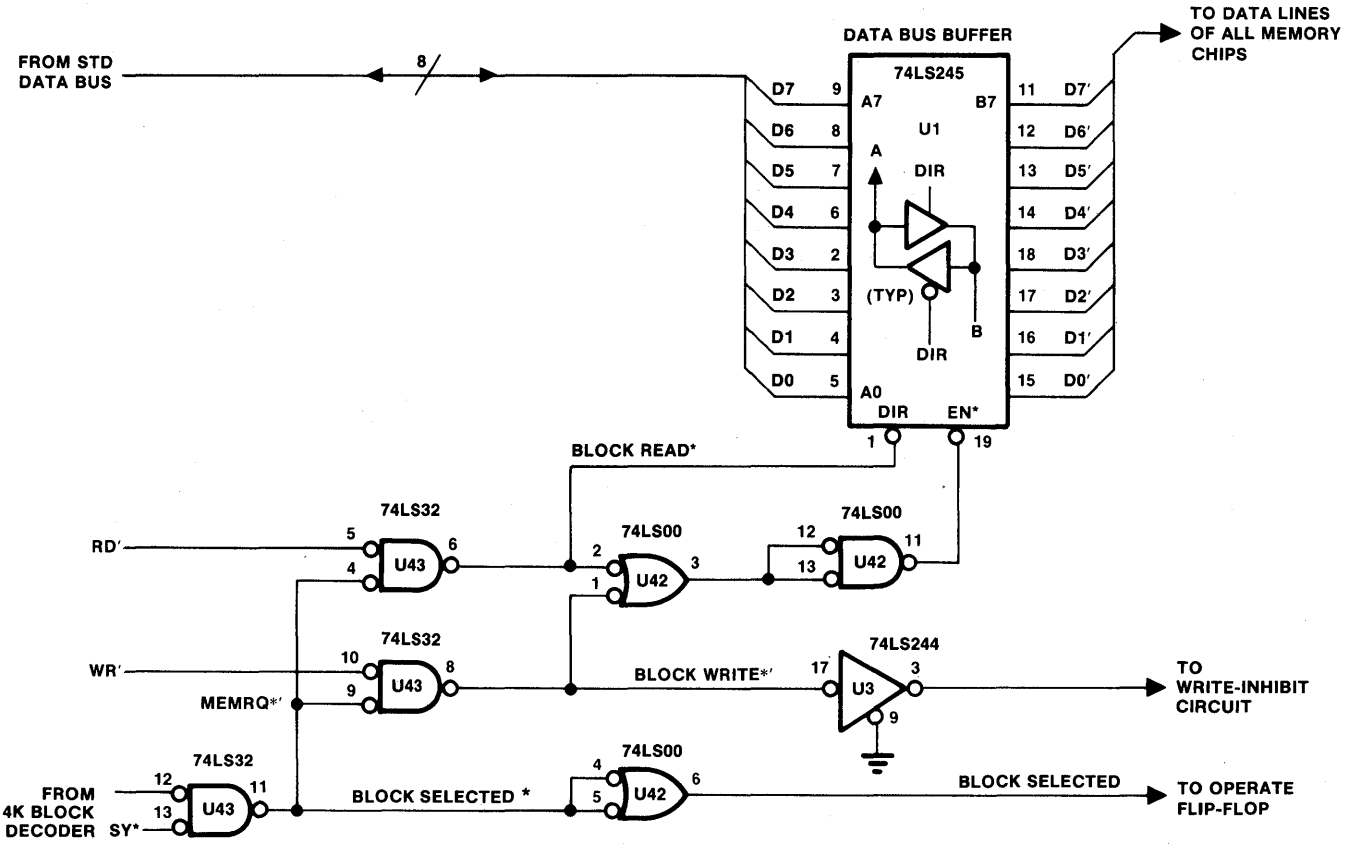


Figure 5-9. Data Bus Buffer Circuit for 7703.

Write-Control Circuit

See Fig. 5-10. The BLOCK WRITE* signal is applied to the four write-inhibit switches (S1-1, S1-2, S1-3, and S1-4). Each switch setting enables or disables write protection for the appropriate 4K memory block, from the lowest 4K block (S1-1) to the highest 4K block (S1-4) (see Fig. 5-11). The WEX* signals (WE0*, WE1*, WE2*, and WE3*) are applied to the write-enable input (pin 10) of the memory chips. When the operate flip-flop is reset, the 74C32 CMOS buffer is disabled, which insures the data integrity on the 7703 during power-up and power-down, as well as during power failure.

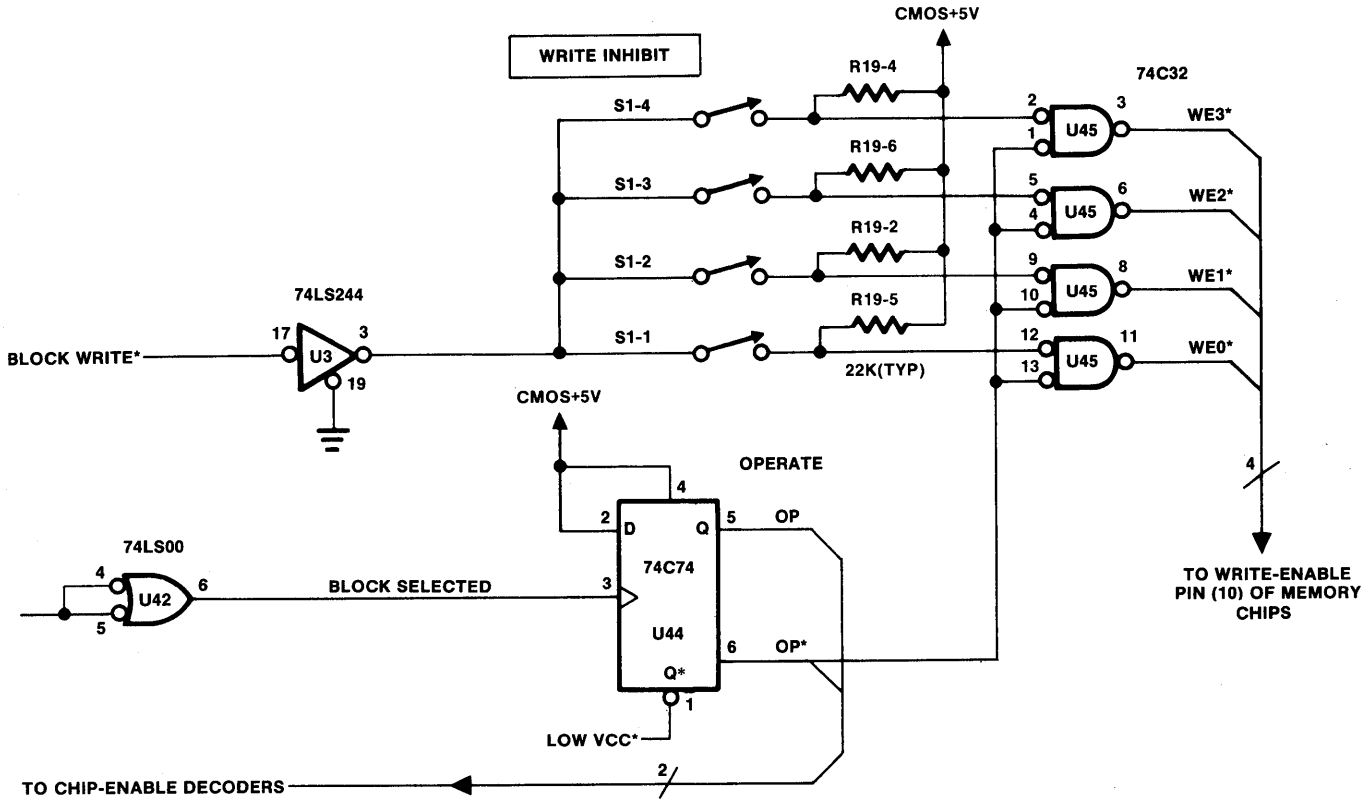


Figure 5-10. Write-Control Circuit for 7703.

SWITCH	CONTROLS 4K MEMORY BLOCK	CONTROLS RAM PAIRS (see Fig. 5-3)
S1-1	0	0-3
S1-2	1	4-7
S1-3	2	8-11
S1-4	3	10-15

Figure 5-11. Write-Inhibit Switches for 7703.

7703 Save Circuit

Figure 5-12 shows the sequence for activating the 7703's data-save circuitry. As shown in Fig. 5-10, the operate flip-flop is reset by the low Vcc* signal. When in a reset condition, the operate flip-flop disables both the chip-select lines (CE0*-CE15*) and the write-enable lines (WE0-WE3). The memory chips are thereby forced into the standby mode, assuring retention of the 7703 data contents. The operate flip-flop can be set only by executing a memory reference. This action results in a block selected signal that clocks the operate flip-flop select. This, in turn, re-enables both the chip-select lines and the write-enable lines.

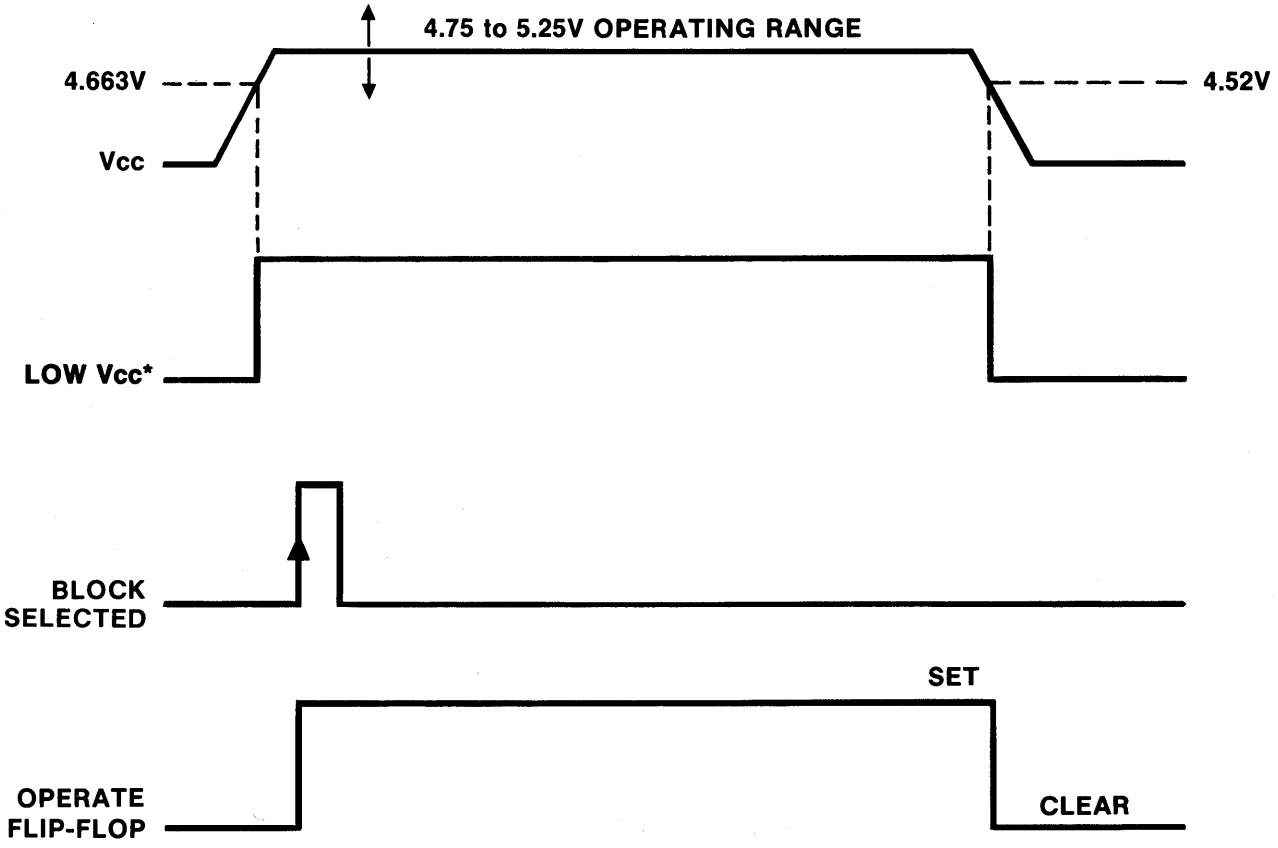


Figure 5-12. Sequence Diagram for 7703's Data-Save Circuit.

Power Monitoring Circuit

See Fig. 5-13. One half of U32 (LM393, dual linear comparator) monitors the +5V line. When power is lost (i.e., drops below 4.52V), low Vcc* is generated and is used to reset the operate flip-flop. This action activates the data-save circuitry described previously. The other half of the LM393 monitors the voltage from the lithium battery. An LED illuminates when this voltage falls below 2.40V. A jumper pad (jumper B) is available to activate the NMIRQ* line, when low voltage is detected in the backup battery.

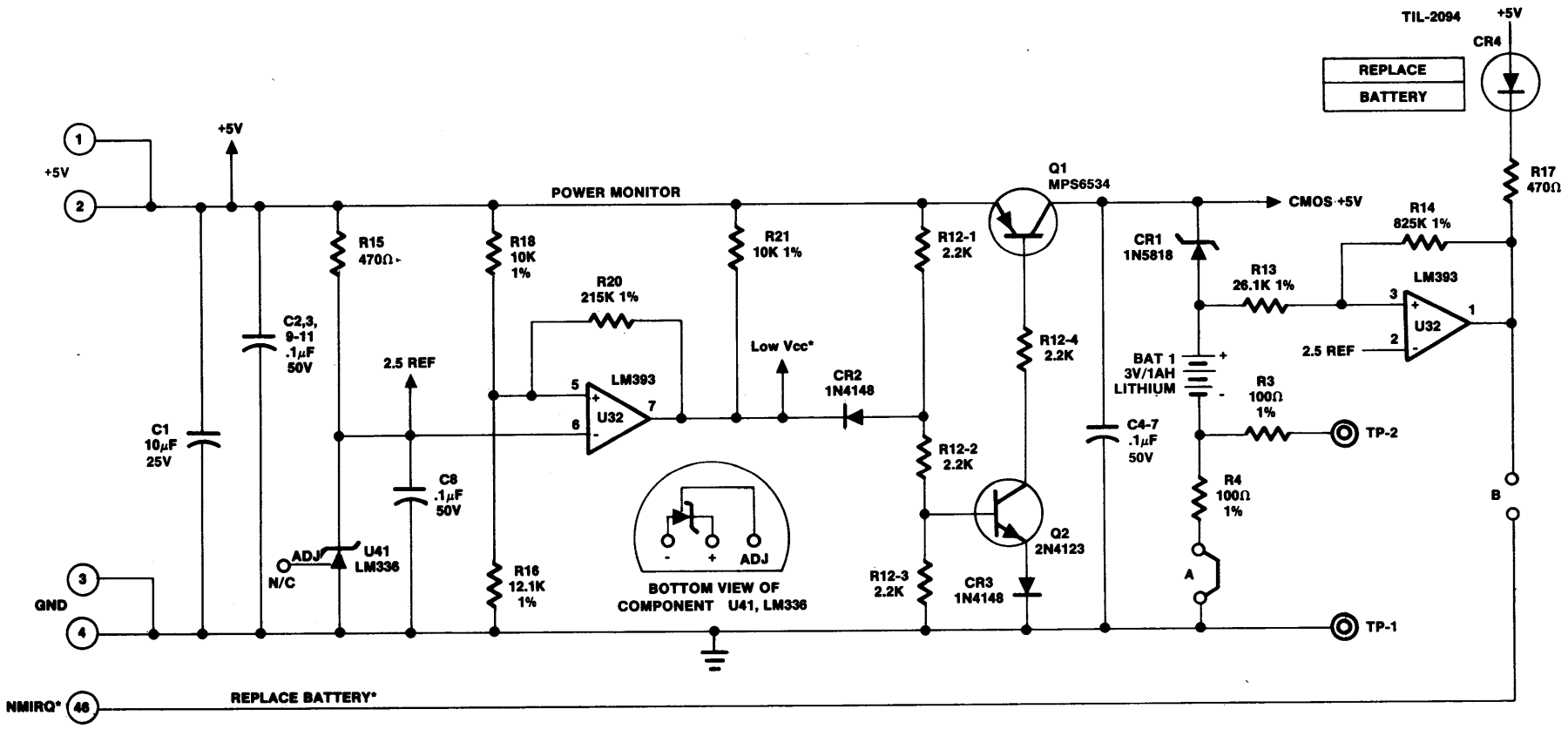
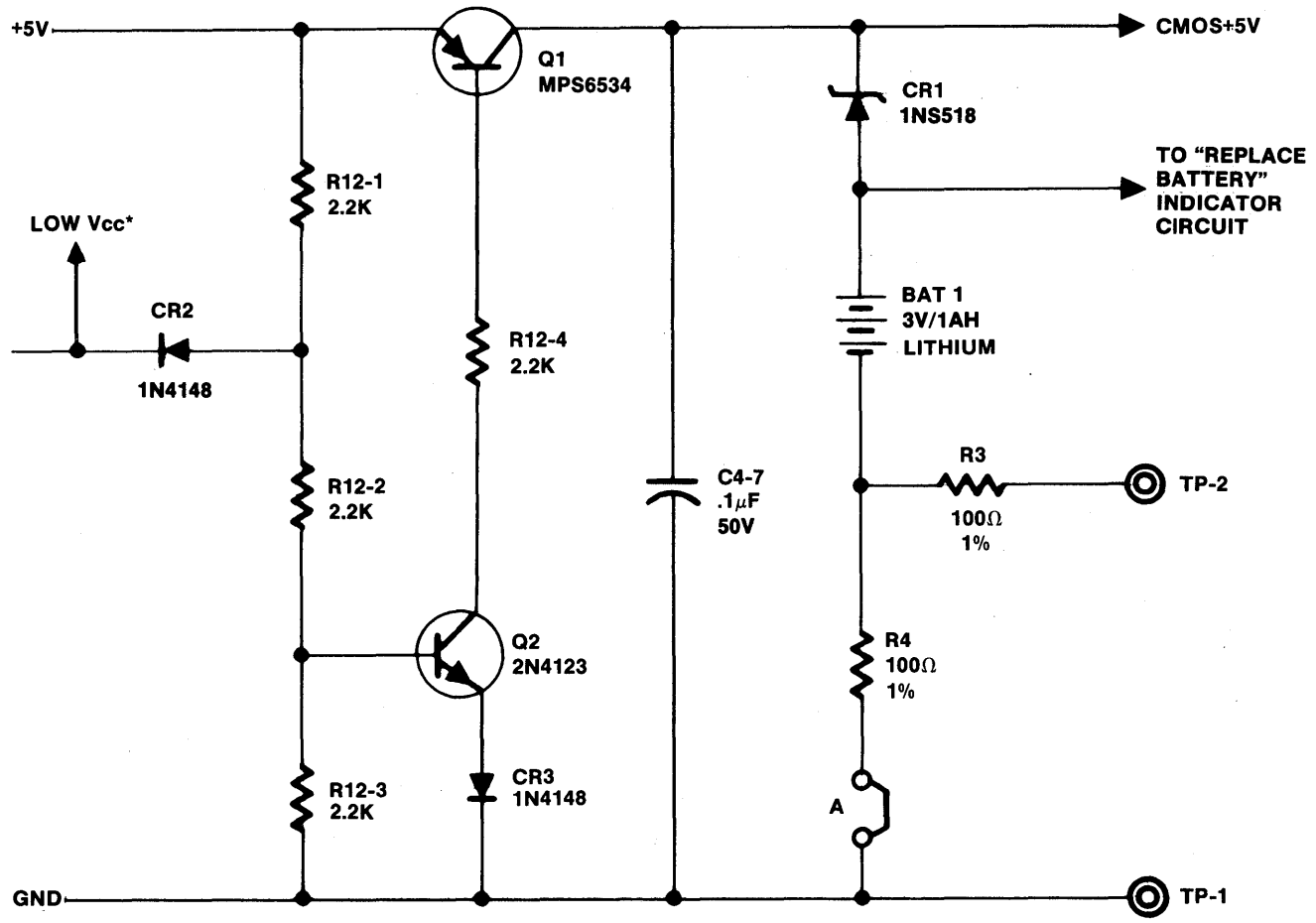


Figure 5-13. Monitoring Circuit for 7703.

Backup Battery Circuit

See Fig. 5-14. The backup battery is a lithium primary cell rated at 3V, 1 ampere hour. The battery's shelf life is 10 years and its operating range is from -40 to 70°C. A Schottky diode protects the battery from system power. You can monitor the battery current by measuring the voltage drop across the 100-Ω resistor (R4) that is in series with the battery. Battery drain or back leakage should never exceed 30 μA. See Appendix A for guidelines on handling lithium batteries.



NOTE: Short circuit of traces or exposure of the card to strong radiation shortens data retention and necessitates early battery replacement.

Figure 5-14. Battery Backup Circuit for 7703.

Changing the Lithium Battery

To change the lithium battery on the 7703 card, follow these steps:

1. Remove the battery activation jumper (jumper A).
2. Desolder the battery's leads from the card. DO **NOT** TRY TO REMOVE THE LEADS FROM THE BATTERY!
3. Remove the battery.
4. Place the new battery in position, checking for proper polarity.
5. Solder the battery leads to the card at the appropriate pads.
6. Replace jumper A.
7. Connect a voltmeter across the test points TP1 and TP2. The voltage should not be more than 0.003V, although it may be considerably less. A proper reading at this point verifies that the lithium battery is properly installed and operating. If the voltage is more than 0.003V, disconnect the battery and call the Customer Service department at Pro-Log (see "Return for Repair Procedures").

Signal Glossary

MNEMONIC	MEANING	PIN(S)	DESCRIPTION	FUNCTION
D0-D7	Data bus	7-14	High-active	8-bit, 3-state bidirectional data bus
A15, A14	Address bus	16,18	High-active	Decode 64K address space through 16K bank decoder
A13, A12	Address bus	20,22	High-active	Select active 4K block from 16K bank controlled by A15 and A14
A11, A10	Address bus	24,26	High-active	Decode block enables
A0-A9	Address bus	15, 17, 19 21,23,25 27,28,29,30	High-active	Address bus for 1Kx8 CMOS RAM
MEMEX	Memory expansion	36	High-active	Expands or enables memory addressing
WR*	Write	31	Low-active	Indicates that the bus holds valid data to be written in addressed memory
MEMRQ*	Memory address select	34	Low-active	Indicates address bus holds valid address for memory read/write operations
RD*	Read	32	Low-active	Indicates that processor is reading data from memory
+5V	Voltage (bused)	2	—	Provides main logic voltage

Note: Unused pins are open; pads are provided on some unused pins for user signals.

Figure 5-15. STD BUS Edge Connector Signals for the 7703. (See also edge connector pin list, Fig. 2-7.)

MNEMONIC	SCHEMATIC GRID LOCATION	MEANING	DESCRIPTION/FUNCTION
SX*	D-6	16K bank select	User-selectable. Defines 16K address range by decoding A15, A14. Block decode enable.
SY*	D-5	4K block select	Indicates that one of the 4K banks has been selected by decoding A13, A12 qualified by SX*. BUS control enable.
34K*	D-6	Block 3 selected	Enables decoding circuitry for memory block 3 (RAM pairs 12-15) by decoding A13, A12 qualified by SX*.
24K*	D-6	Block 2 selected	Enables decoding circuitry for memory block 2 (RAM pairs 8-11) by decoding A13, A12 qualified by SX*.
14K*	D-6	Block 1 selected	Enables decoding circuitry for memory block 1 (RAM pairs 4-7) by decoding A13, A12 qualified by SX*.
04K*	D-6	Block 0 selected	Enables decoding circuitry for memory block 0 (RAM pairs 0-3) by decoding A13, A12 qualified by SX*.
BLOCK SELECTED*	D-5,4	Block selected	Qualified with MEMRQ* to indicate that a memory block has been selected.
BLOCK SELECTED	D-4,3	Block selected	Complement of above signal. Used to set the operate flip-flop upon a memory reference (enable memory).
BLOCK READ*	D-4	Read strobe	Provides direction control for the data bus buffer.
BLOCK WRITE*	D-4	Write strobe	Provides direction control for the data bus buffer. Provides write-enable signals via the write-inhibit switches.
OP	D-3	Chip-enable decode strobe	Acts as strobe to the chip-enable decoder (Blocks 1 and 3).
OP*	D-3	Chip-enable decode strobe	Acts as strobe to the chip-enable decoder (Blocks 0 and 2). Also, qualifies BLOCK WRITE* to generate the write-enable signals.
WE3*	D-2	Write-enable blocks	Provides write-enable for memory block 3 (RAM pairs 12-15). S1-4 must be closed.
WE2*	D-2	Write-enable block 2	Provides write-enable for memory block 2 (RAM pairs 8-11). S1-3 must be closed.
WE1*	D-2	Write-enable block 1	Provides write-enable for memory block 1 (RAM pairs 4-7). S1-2 must be closed.

Figure 5-16. 7703 Internal Signals (see Schematic, Fig. 5-1, for reference).

MNEMONIC	SCHEMATIC GRID LOCATION	MEANING	DESCRIPTION/FUNCTION
WE0*	D-2	Write-enable block 1	Provides write enable for memory block 0 (RAM pairs 0-3). S1-2 must be closed.
CE15*	C-6	Chip-enable RAM pair 15	Provides chip enable to RAM pair 15 by decoding A11, A10 qualified by 34K* and OP.
CE0*	B-6	Chip-enable RAM pair 0	Provides chip enable to RAM pair 0 by decoding A11, A10 qualified by 04K* and OP*.
2.5 REF	A-7	2.5V reference voltage	Reference voltage used in the power monitor circuit (to test Vcc) and in the circuit that monitors the battery.
LOW VCC*	A-6	Low Vcc voltage	Used to clear the operate flip-flop when Vcc (+5V) is too low (power-down <4.52V, power-up <4.663V). Disables memory.
CMOS +5V	B-4	CMOS voltage supply	Voltage supply for the CMOS devices. Alternate power source to allow data retention when system power is not provided.

Figure 5-16. 7703 Internal Signals (continued).

Return for Repair Procedures

Domestic Customers:

1. Call our factory direct at (408) 372-4593, and ask for CUSTOMER SERVICE.
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, reason for return, and the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Package the equipment in a solid cardboard box secured with packing material.

   CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.
5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, California 93940

   Reference CRO # _____ .

International Customers:

Equipment repair is handled by your local Pro-Log Distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for one year from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

APPENDIX A
Guidelines for Handling Lithium Batteries

NOTE

The information in this appendix is provided for reference only. Pro-Log does not assume any liability that may arise out of the application or use of the information that follows.

Introduction

This appendix provides guidelines for utilizing lithium batteries. Lithium cells utilize lithium organic electrolytes, which produce much higher energy densities (capacity) than do conventional primary cells (carbon zinc). This high capacity and the use of lithium require handling procedures more stringent than those required for conventional cells. The cells used by Pro-Log are equipped with a pressure-sensitive vent mechanism designed to safely deactivate a cell under the most abusive thermal environment, test, or operating condition.

CAUTION

To prevent recharge, short circuit, and puncture or exposure to high temperature or incineration, do not store, test, or handle lithium cells near flammable solvents or materials.

Exposure to Short Circuit Conditions

Any cell that has been exposed to short circuit conditions should not be used in shippable equipment. The cells should be hand inserted and soldered. No special precautions are required.

NOTE

If a wire breaks loose from the body of the lithium cell, do not attempt to resolder it.

The accidental short circuiting of a lithium cell will cause the internal temperature of the lithium cell to rise. If the short remains long enough, one of the two following conditions will occur:

Either

Dissipated heat, burning, or glowing electrical connections will be evident with an accompanying loss of cell output voltage.

Action: Remove the cause of the short circuit as soon as possible. Allow the cell to cool and remove it from service. For disposal, see disposal recommendations on page A-2.

Or

40-50% of the cell's fumes will vent due to the internal temperature buildup. NOTE: Upon venting, the cell chemistry will stop and the cell will become inactive.

Action: Remove the cause of the short circuit immediately, if possible without exposure to the venting fumes. Evacuate the immediate area until venting has stopped. Move the cell or assembly to a dry ventilated area and let it stabilize for 24 hours. After stabilization, dispose of the cell (see disposal recommendations on page A-2).

Electrolyte Leakage

Characteristics: A leaking and/or vented cell can be readily detected by the presence of sulfur dioxide and residual electrolyte solvents. The electrolyte consists primarily of sulfur dioxide, a highly irritating, nonflammable, colorless gas at room temperature and atmospheric pressure.

Toxicity: Gaseous sulfur dioxide is highly irritating and is practically irrespirable. It is readily detected in concentrations of 3-5 ppm and thus provides ample warning of its presence. Acute exposure to sulfur dioxide has the following effects: throat irritation, coughing, constriction of the chest, tearing and smarting of the eyes. There are **no** systemic effects of acute exposure to sulfur dioxide.

Action: Electrically disconnect the suspected cell if it is under load. Store the cell or hardware in a ventilated, dry area under ambient thermal conditions. After the concentrations of sulfur dioxide are reduced to a tolerable value (approximately 5 ppm, i.e., when the irritating odor is significantly diminished), carefully unpack the suspected cell or hardware and visually examine it to determine the source of electrolyte leakage. Segregate acceptable cells and get rid of the unacceptable ones (see disposal recommendations below).

Disposal Recommendations

1. Prepare the cell for disposal by packaging it in a suitable container that will prevent short circuiting or crushing of the cell.
2. Dispose of low quantities of cells (10 or less) in the same manner as carbon zinc cells (flashlight batteries) are disposed of.

CAUTION
Do not incinerate or compact the cells!

3. Dispose of larger quantities of cells as follows:

   To effect the most environmentally safe disposal, place the cells in secured landfills or disposal ponds with provisions for leachate control and monitoring, documentation, and runoff control.

   Sanitary landfills or special landfills can be used, where the cells can be dispersed in large quantities of solid waster. When transporting the used cells or batteries for disposal, handle them in a safe manner to prevent short circuiting.

CAUTION
Do not incinerate or compact the cells!

Shipping the Product

Shipping regulation requirements: Quantities less than 200 units/shipment are exempt from domestic regulation DOT-E-7042 and International Regulation IATA and may be shipped unrestricted. The shipping package should prevent short circuit or crushing the product.

Quantities greater than 200 units require that the following label be affixed:

Lithium - not restricted per DOT-E-7042, Section 173.206, Par. F; or IATA, Section 10.

USER'S MANUAL

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