READ

theory
and
operation

PHILCO

Communications and Electronics Division, Philadelphia, Pa.

PHILCO
A subsidiary of Ford Motor Company

REMOTE ELECTRONIC ACCESS DEVICE

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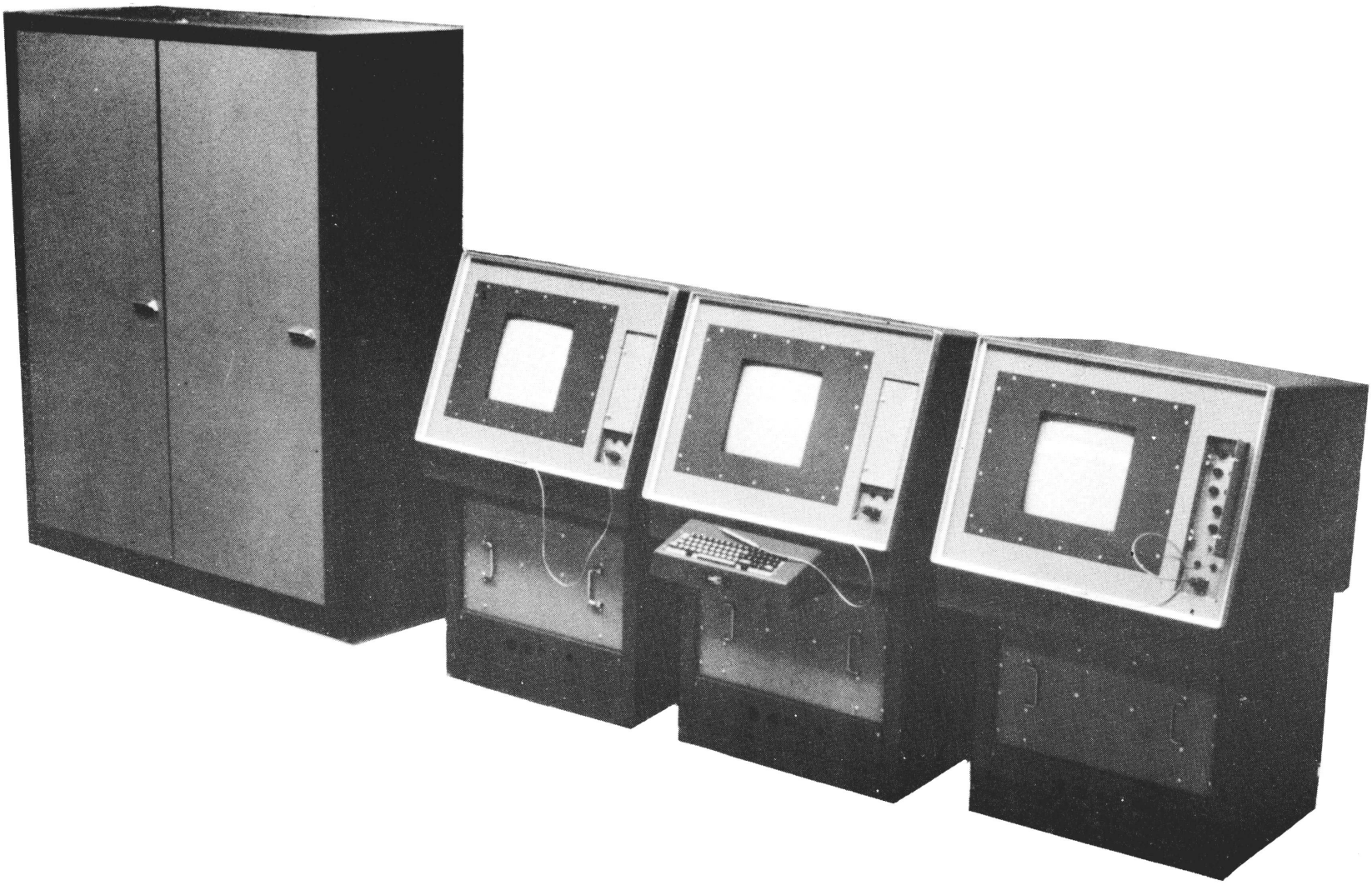


READ Console

SECTION 1

INTRODUCTION

The Philco Remote Electronic Access and Display System (READ) provides the facilities for transferring data to and from the PDP-1. Data input to READ is via the DEC type 131 input/output channel. Data output from READ is via the break-sequence channel.

The READ system consists of a common logic cabinet and 12 remote console stations. The common logic contains the display controller and keyboard multiplexer. Each remote console station consists of a display console, 64-key keyboard, multiple voltage power supply, and light pen.

The display controller contains the system logic for the common vector, format and character generators. It also contains the system logic for generating light pen program interrupts. The keyboard multiplexer contains the system logic for identifying and transferring keyboard generated data to the PDP-1.

A block diagram of this system is shown in Figure 1-1.

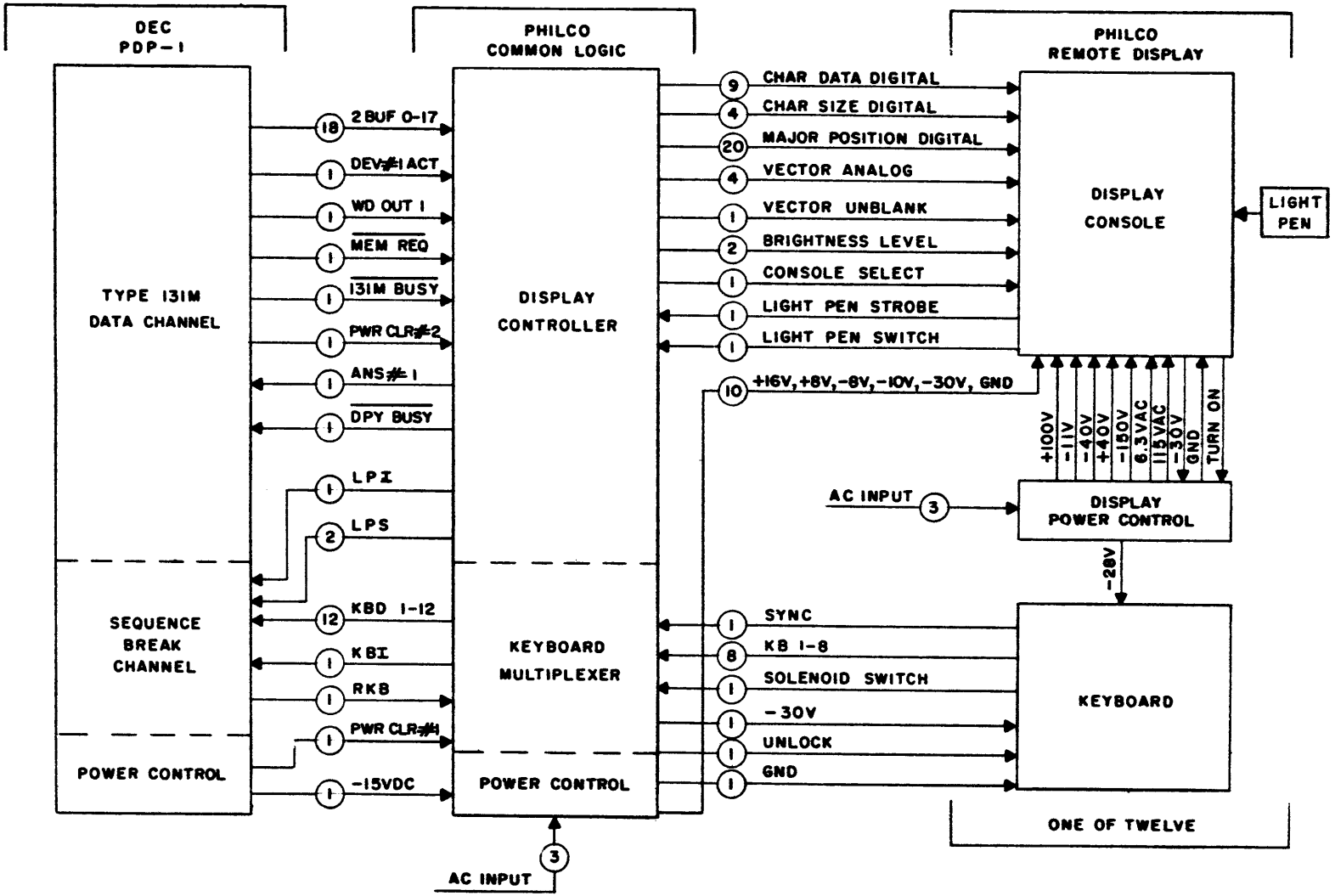


Figure 1-1. READ Block Diagram

SECTION 2

SPECIFICATIONS

2.1 CONSOLES

Twelve consoles contain:

a. 16-inch magnetic CRT

b. Single 64-key keyboard. The keyboard will be removable.

c. Light pen

d. Maximum 75-foot spacing from consoles to common display logic.

e. The CRT shall provide a character stroke brightness essentially equivalent to that attained by a commercial Tektronix Model 535 oscilloscope having:

(1) CRT with a P7 or P7 equivalent phosphor

(2) Trace set to sweep at 2 microseconds/cm

(3) Oscilloscope synchronized to sweep at 60 cps

2.2 CHARACTER GENERATOR

a. 176-kc average character rate with 13 strokes per character.

b. 128-character capacity; however, 116 printable characters are provided.

c. Characters may be specified by Stanford within allowed rules for character generation.

d. Seven character sizes with approximate ratios of 1, 1.6, 2, 3.4, 4, 6 and 8 to 1.

2.3 VECTOR GENERATOR

a. Generates a vector up to 1/8 screen diameter in length connecting two points in a 1024 x 1024 matrix of points, defining the full scale dimensions of the display.

b. Vector drawing time variable from 5 to 15 microseconds dependent on vector length.

c. Point plotting implemented by intensifying CRT momentarily at the completion of a vector drawing cycle with the CRT blanked.

d. Allows major positioning without intensifying display.

2.4 COMMON DISPLAY LOGIC

a. Provides interface to PDP-1 through type 131 I/O channel and "break sequence" channel.

b. Keyboard multiplexer input to "break sequence" channel.

(1) Provides "level" when a character is entered from any keyboard.

(2) Locks the keyboard and places the 6-bit code for the character to be entered on the processor input lines.

(3) Places a 4-bit code designating the console at which the data originated.

(4) Requires a level input specifying the processor has accepted the data to initiate rescanning of keyboards and to unlock the locked keyboard.

2.5 TYPE 131 CHANNEL DATA TRANSFER TO DISPLAY

a. Places a level on a data ready line when correct information is ready to be input to the display.

b. Accepts a new data request level from the display to initiate a memory cycle.

c. Word format.

2.5.1 Typewriter Format

Char. 1	Char. 2	Char. 3

a. Contains three 6-bit character codes.

b. Prints the characters defined by the three character codes in successive locations on the line with:

(1) Size specified by data input from a control word

(2) Spacing proportional to character size

c. Accepts and operates as required on the codes:

(1) Carriage return

(2) Space

(3) No-Op

(4) Case Shift - separate codes to specify both up and down shifts

2.5.2 Vector Format

Type 1

Control	ΔX Sign	ΔX	ΔY Sign	ΔY

a. Control is a two bit pattern which specifies:

(1) 00 - Display vector

(2) 01 - Display point at end of vector

(3) 10 - Trace vector without displaying the vector

b. ΔX sign and ΔY sign - 1 bit specifying plus or minus direction

c. ΔX and ΔY - 7 bit number specifying the vector magnitude (length) up to 1/8 of screen diameter.

Type 2

Control	"0"	Set X	X	Set Y	Y

a. Control is the 2-bit pattern - 11 - which specifies a position word when in vector mode. The CRT is positioned by this word without display of data on the CRT.

b. "0" - this bit must be set to binary zero for proper interpretation of the word.

c. X position and Y position - 6 bits setting the high order 6 bits of X and Y position register, independently.

d. Set X and Set Y control - 1 bit specifying whether the data contained in this word should set the high order 6 bits of the position with the low order 4 bits reset to allow X and Y positions to be set to new values independently without affecting each other.

e. Center of screen is binary zero

[+1 unit is binary 0000000001

-1 unit is binary 1111111110]

2.5.3 Control Word Format

a. Escape Character - 6-bit nonprintable and illegal code in both Typewriter and Vector Format words, e.g., Octal Code 74.

b. Console Designation - 5-bit code

(1) Octal code 0 blanks all consoles.

(2) Octal codes 1 through 14 specify that the correspondingly numbered console should be added to the list of those currently intensified.

(3) Octal Codes 20 through 27 specify that no changes in consoles intensified should be made.

c. Size Control - 3 bits

(1) Octal Code 0 - do not change character size.

(2) Octal Codes 1 through 7 - set to the corresponding character size.

d. Mode Control - 2 bits

(1) Octal Code 0, 1 - re-enter previous mode.

(2) Octal Code 2 - enter typewriter mode.

(3) Octal Code 3 - enter vector mode.

e. Brightness Control - 2 bits

(1) Octal Code 0 - no change in brightness level.

(2) Octal Codes 1 through 3 - set to corresponding brightness level.

SECTION 3

GENERAL DESCRIPTION

3.1 EQUIPMENT

The READ system consists of a common logic frame and 12 remote console stations.

3.1.1 Common Logic Frame

The common logic frame is a two-bay equipment cabinet. Bay 1 contains the dc power supplies, ac sequencer and the dc distribution panel for the 12 remote stations. Bay 2 contains the logic modules, two fixed memories, and the signal cable distribution rack for the 12 remote stations. The arrangement of this equipment is shown on Figures 3-1, 3-2, and 3-3.

3.1.1.1 Bay 1 Equipment

The equipment contained in Bay 1 is as follows:

Equipment	Philco Part No.	Schematic Dwg. No.
ac Sequencer	398-6618-1	9LO-8601
-30-v Power Supply	398-5653-1	See Instruction Manual 398-5653-3
-10-v Power Supply	398-5653-4	See Instruction Manual
+16-v Power Supply	398-5653-2	See Instruction Manual
-30-v Power Supply	398-5653-3	See Instruction Manual
+8-v Power Supply	398-6258-1	See Instruction Manual
-8-v Power Supply	398-6258-1	See Instruction Manual
dc Distribution Panel	398-6342-1	See Figures 3-3 and 3-4

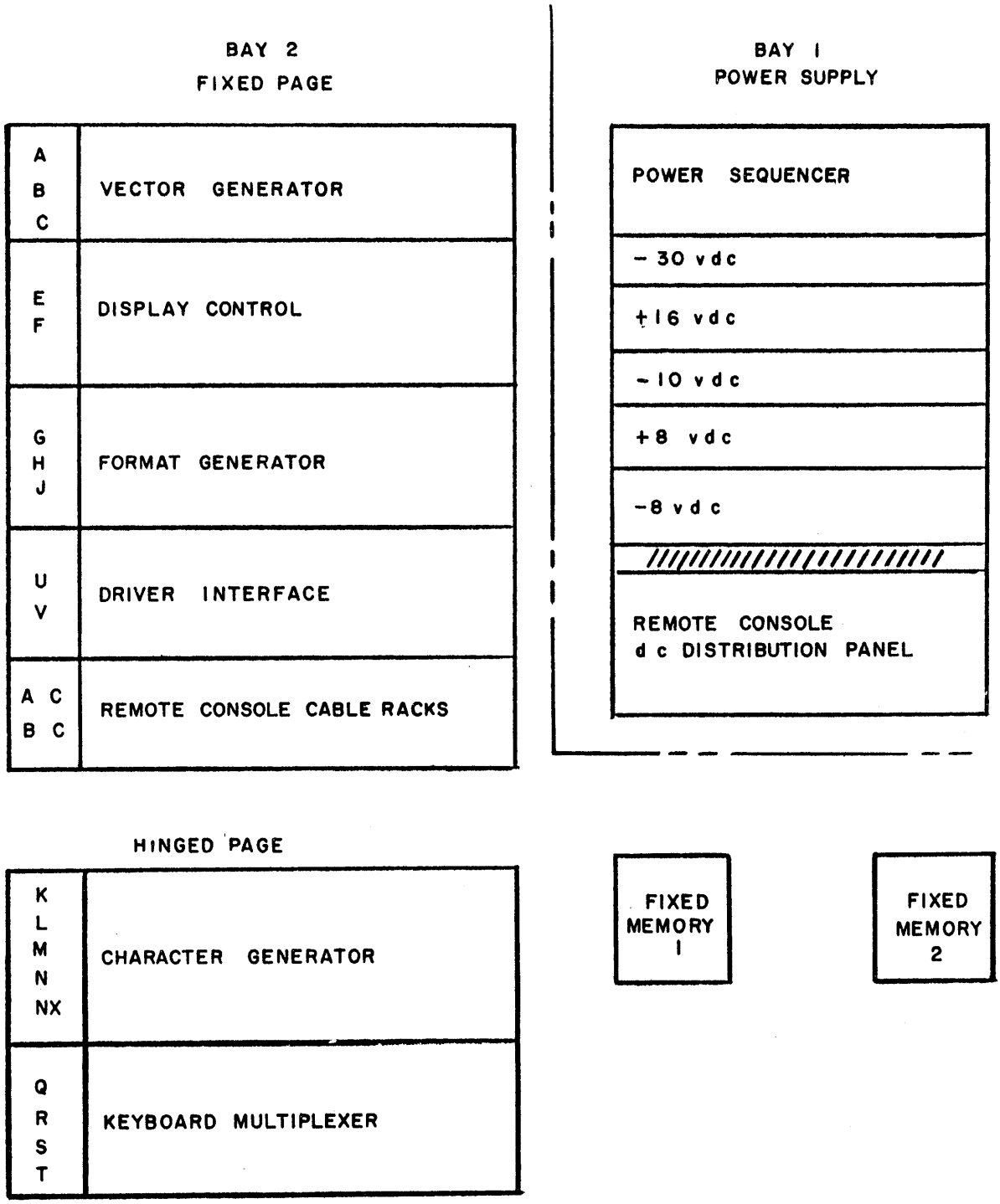


Figure 3-1. READ Common Logic Frame

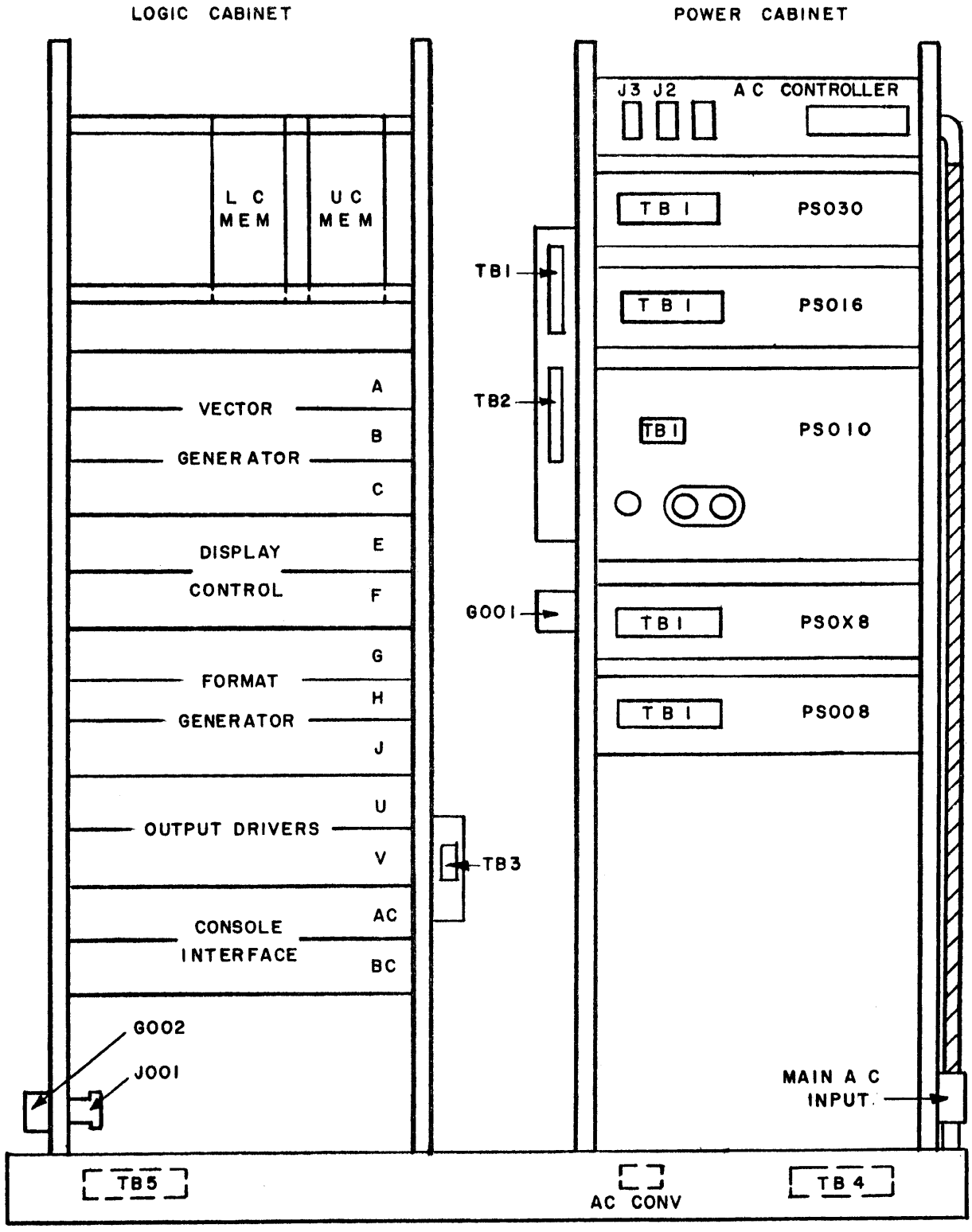


Figure 3-2. Common Logic and Control Unit, Rear View

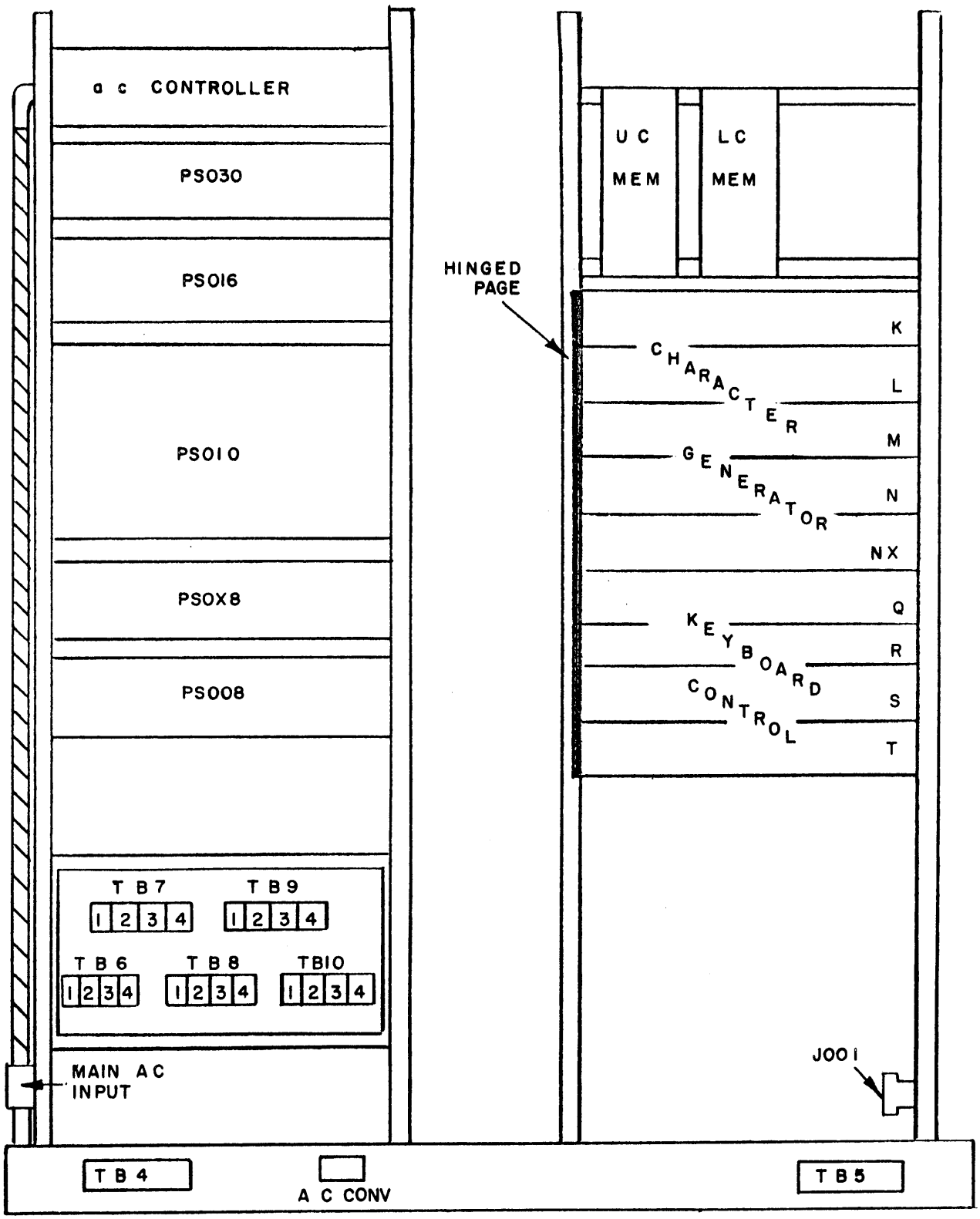
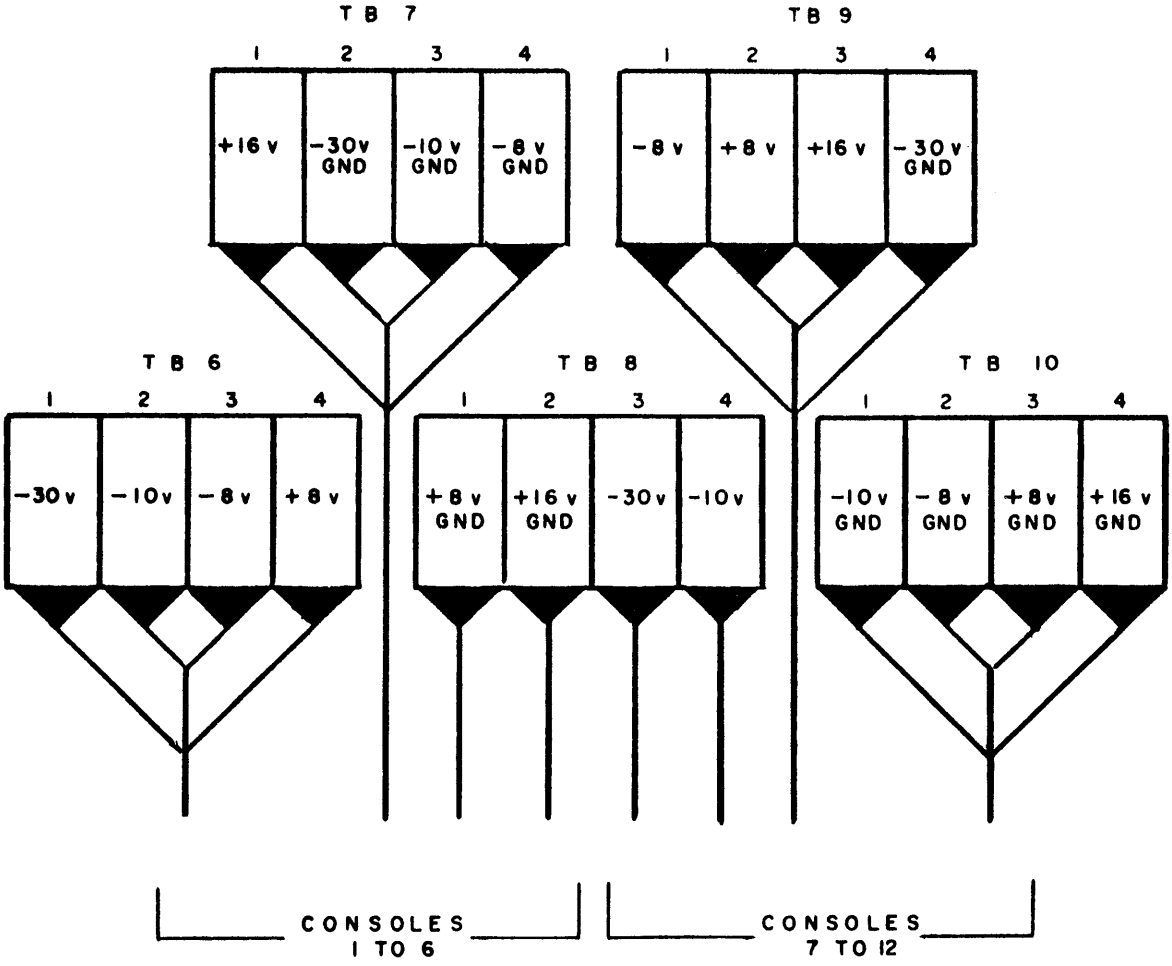


Figure 3-3. Common Logic and Control Unit, Front View



EACH D C POWER CABLE IS NUMBERED 1 THROUGH 10

1 – 8 vdc	6 – 10v GND
2 – 8 vGND	7 – 30vdc
3 + 8 vdc	8 – 30v GND
4 + 8 vGND	9 + 16vdc
5 – 10vdc	10 + 16 v GND

Figure 3-4. Console Power Distribution Blocks

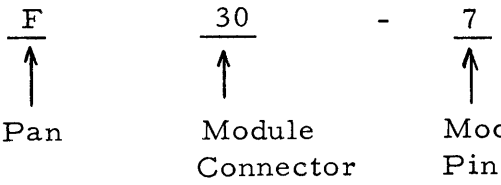
3.1.1.2 Bay 2 Equipment

The equipment contained in Bay 2 is as follows:

Equipment	Philco Part No.	Schematic Dwg. No.	(page)
Vector Generator	398-6615-1	9LO-8594	37-51
Display control	398-6615-1	9LO-8594	5-13
Format generator	398-6615-1	9LO-8594	14-23
Driver interface	398-6615-1	9LO-8594	67-75
Remote console cable rack	398-6317-1	See Table 3-1	
Character generator	398-6616-1	9LO-8594	24-36
Keyboard multiplexer	398-6616-1	9LO-8594	52-66
Fixed memories (2)	398-6617-1, 2		

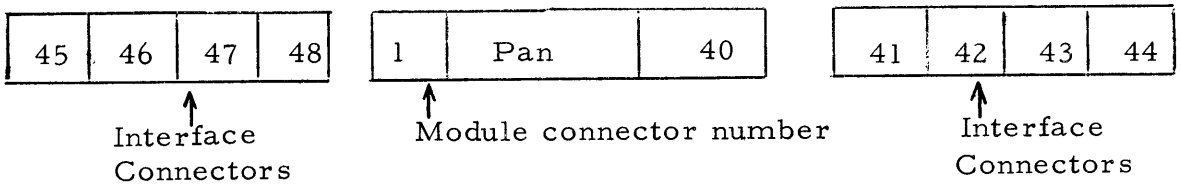
Schematic drawing 9LO-8594 is the logic schematic of the READ system. Included with the logic schematics are module location sheets (see 9LO-8594, sheets A, B, C). A row of modules is called a pan. Each pan is given a designation letter which is listed on the logic schematic. A pan contains 40 possible module connectors and each module connector contains 16 possible pin connections. The pin connections are numbered from 1 to 16.

A specific module connector and pin number is designated as follows:



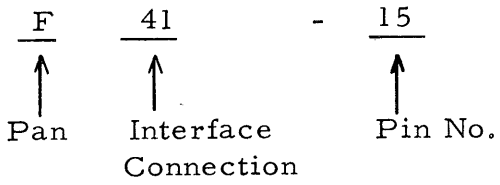
A listing of module types issued in the READ system is shown in Table 3-2. The Philco part number includes the logic symbol and circuit schematic of the printed circuit assembly. Only the symbol is shown in the logic schematics.

Interface connectors located adjacent to the left or right of the logic pan are given designations the same as the logic pans. The numbering of these connectors is as follows:



(Viewed from Front)

The cable connectors which are inserted in these positions are CON6 connectors referred to as "paddles." For example, an interface connection is designated



Note: 1. Pin connections for the interface connectors are numbered 1 to 15. Letters are used for adjacent pins.

2. Pin connections on the cable connectors are numbered 1 to 30.

3.1.2 Remote Console

The READ Remote Console provides a 9-inch by 9-inch visual display of alphanumeric data on a magnetically deflected 16-inch cathode ray tube. The deflection system consists of a 25-microhenry single-ended yoke for major positioning and a 7-microhenry single-ended yoke for character writing. Both the major position and the character yokes are driven by wide-band dc coupled amplifiers comprising ample negative feedback and operating from highly regulated power supplies.

The cathode ray tube is a 52-degree magnetic deflection, electrostatic focus type. The tube is designed specifically to utilize the two yokes and to operate at a high electrostatic focus voltage for increased reliability. The CRT contains an integral protective faceplate for operator protection.

The equipment contained in a remote console is as follows:

Equipment	Philco or Manufacturer Part No.	Schematic Dwg. No.
Power Sequence chassis		9LO-8550
Power pack	398-6299-1	see instruction manual
D18 Amplifier Z axis	398-6197-1	398-6197
D19 Amplifier Character	398-6198-1	398-6198
D20 Amplifier Major position	398-6199-1	398-6199
Logic pan assembly		9LO-8594
Light pen assembly		398-6343
HV power supply	Universal Voltronics BPE-16-5.5	
Cathode ray tube	Thomas Electronics Inc. 16M31P-28	
Major deflection yoke	CELCO type HD428-S670	
Character deflection yoke	CELCO type AW414-S730	

Schematic drawing 9LO-8594 is the logic schematic and module location sheet for the remote console. Schematic drawing 9LO-8550 is the signal and power wiring schematic.

TABLE 3-1

SIGNAL CABLE INTERFACE

From Drivers (Control Unit)	To Console Interface	
AC3	1A41	
AC5	1A42	
AC7	1A43	
AC9	2A41	
AC11	2A42	
AC13	2A43	
AC15	3A41	
AC17	3A42	
AC19	3A43	Consoles 1 through 6 in sound proof room
AC22	4A41	
AC24	4A42	
AC26	4A43	
AC28	5A41	
AC30	5A42	
AC32	5A43	
AC34	6A41	
AC36	6A42	
AC38	6A43	

TABLE 3-1

SIGNAL CABLE INTERFACE (Continued)

From Drivers (Control Unit)	To Console Interface	
BC3	7A41	
BC5	7A42	
BC7	7A43	
BC9	8A41	
BC11	8A42	
BC13	8A43	
BC15	9A41	Consoles 7 through 12 in computer area
BC17	9A42	
BC19	9A43	
BC22	10A41	
BC24	10A42	
BC26	10A43	
BC28	11A41	
BC30	11A42	
BC32	11A43	
BC34	12A41	
BC36	12A42	
BC38	12A43	

TABLE 3-2

READ MODULE TYPES

Module Type	Philco Part No.	Description
1GAA	398-4320-1	Inverter (6 per module)
2GAA	398-4070-1	2 input gate (4 per module)
3GAA	398-4340-1	3 input gate (3 per module)
5GAA	398-4071-1	5 input gate (2 per module)
11GAA	398-4326-1	11 input gate (1 per module)
4FAA	398-4066-1	Flip-flop (set-reset) (2 per module)
5DAA	398-4073-1	Logic gate driver (2 per module)
2IS	398-4628-1	Integrating single shot (1 per module)
52GA	398-5736-1	2 input gate, common line (5 per module)
4CFAA	398-4520-1	Flip-flop(set-reset-trigger) (2 per module)
OS24	398-4346	Oscillator (1 per module), 3 Mc
4SSAA	398-5071-1	Single shot (2 per module)
3MDBB	398-4556-2	Magnet driver (3 per module)
DD3	398-4701-1	Level converter (6 per module)
D1	398-6103-1	Sense amplifier-resistor memory (3 per module)
D2	398-6104-1	Segment driver-resistor memory (6 per module)
D3	398-6105-1	Character select driver-resistor memory (3 per module)

TABLE 3-2

READ MODULE TYPES (Continued)

Module Type	Philco Part No.	Description
D4	398-6170-1	Analog driver preamp (4 per module)
D5	398-6171-1	Ramp generator-negative (1 per module)
D6	398-6172-1	Ramp generator-positive (1 per module)
D7	398-6173-1	Zero crossing detector (1 per module)
D8	398-6174-1	Character size control (2 per module)
D9A	398-6175-1	D/A driver-negative (3 per module)
D9C	398-6175-3	D/A driver-negative (3 per module)
D9D	398-6175-4	D/A driver-positive (3 per module)
D10A	398-6176-1	Ladder network (1 per module)
D10C	398-6176-3	Ladder network-negative (1 per module)
D10D	398-6176-4	Ladder network-positive (1 per module)
D11	398-6177-2	Cable driver (4 per module), digital
D12	398-6178-1	Cable driver (6 per module), analog
D13	398-6302-1	Summing amplifier (2 per module)
D14	398-6180-1	Integrator (1 per module)
D15	398-6181-1	Preamplifier-integrator (4 per module)
D16	398-6212-1	Preamplifier-size (4 per module)
D17	398-6246-1	Regulator - 16v (1 per module)
D18	398-6197-1	Amplifier Z axis (1 per module)

TABLE 3-2

READ MODULE TYPES (Continued)

Module Type	Philco Part No.	Description
D19	398-6198-1	Amplifier-character (1 per module)
D20	398-6199-1	Amplifier-major position (1 per module)
D23	398-6331	Light pen amplifier (1 per module)
CCM1	398-5539-1	Standard gate-inverter (6 per module)
CCM5	398-5543-1	Flip-flop No. 1 (3 per module)
CCM11	398-5549-1	Single shot (2 per module)
CCM12	398-5550-1	Logic driver (6 per module)

SECTION 4

DETAILED DESCRIPTION

4.1 KEYBOARD OPERATION

The keyboard control circuit shown in Figure 4-1 operates as follows: When the operator presses a key, solenoid switch contacts SIA and SIB close. Contacts SIB energizes the keyboard solenoid through the normally closed contacts KIC of the antirepeat relay K1. When the solenoid is energized, code contacts KC_{1-6} and the keyboard common contact KCC are locked. Contacts KC_{1-6} present data to the multiplexer and KCC presents the SYNC signal.

When the UNLOCK signal is presented to the keyboard, relay K1 is energized. With K1 energized, the SYNC and KB signals are removed via the opening of contacts K1B. Relay K1 is also energized via the multiplexer logic and K1A contacts. If SIA is closed when the keyboard is unlocked, K1 will remain energized until SIA is released.

Keyboard switches KS1 and KS2 are located on the left and right of the space bar respectively. These switches must be closed during operation of the keyboard keys in order to transfer KB_7 and KB_8 data to the multiplexer.

For a further description of the keyboard operation, refer to Soroban Manual, Model FK-2 and Soroban drawings numbers C-15549 and B-15461.

4.2 KEYBOARD MULTIPLEXER OPERATION

The keyboard multiplexer consists of keyboard control logic, priority control, timing, and data control gates. The functions of the keyboard control logic are to insure that data code contacts have settled when the SYNC signal is presented to priority control and to unlock the respective keyboard after its data has been transferred to the PDP-1. The functions of priority control are to generate the proper keyboard identifier (KBD_{1-4}) and select the respective keyboard via the PRT signals. The timing circuits generate the keyboard interrupt and present the timing phases to the keyboard and priority control. For the following description, refer to the keyboard multiplexer logic schematics 9LO-8594, sheets 52 to 66 and Figure 4-2.

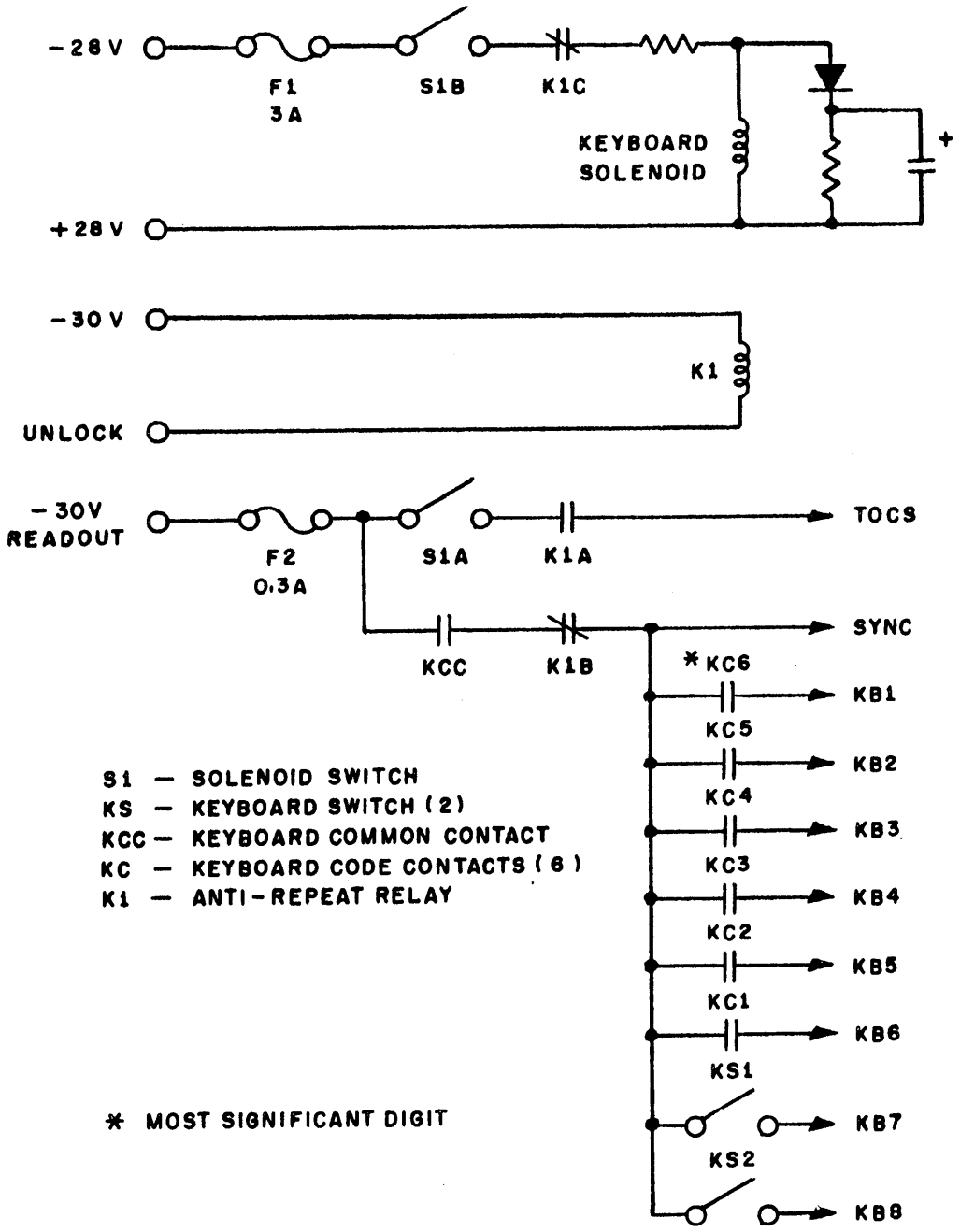


Figure 4-1. Keyboard Control Circuit

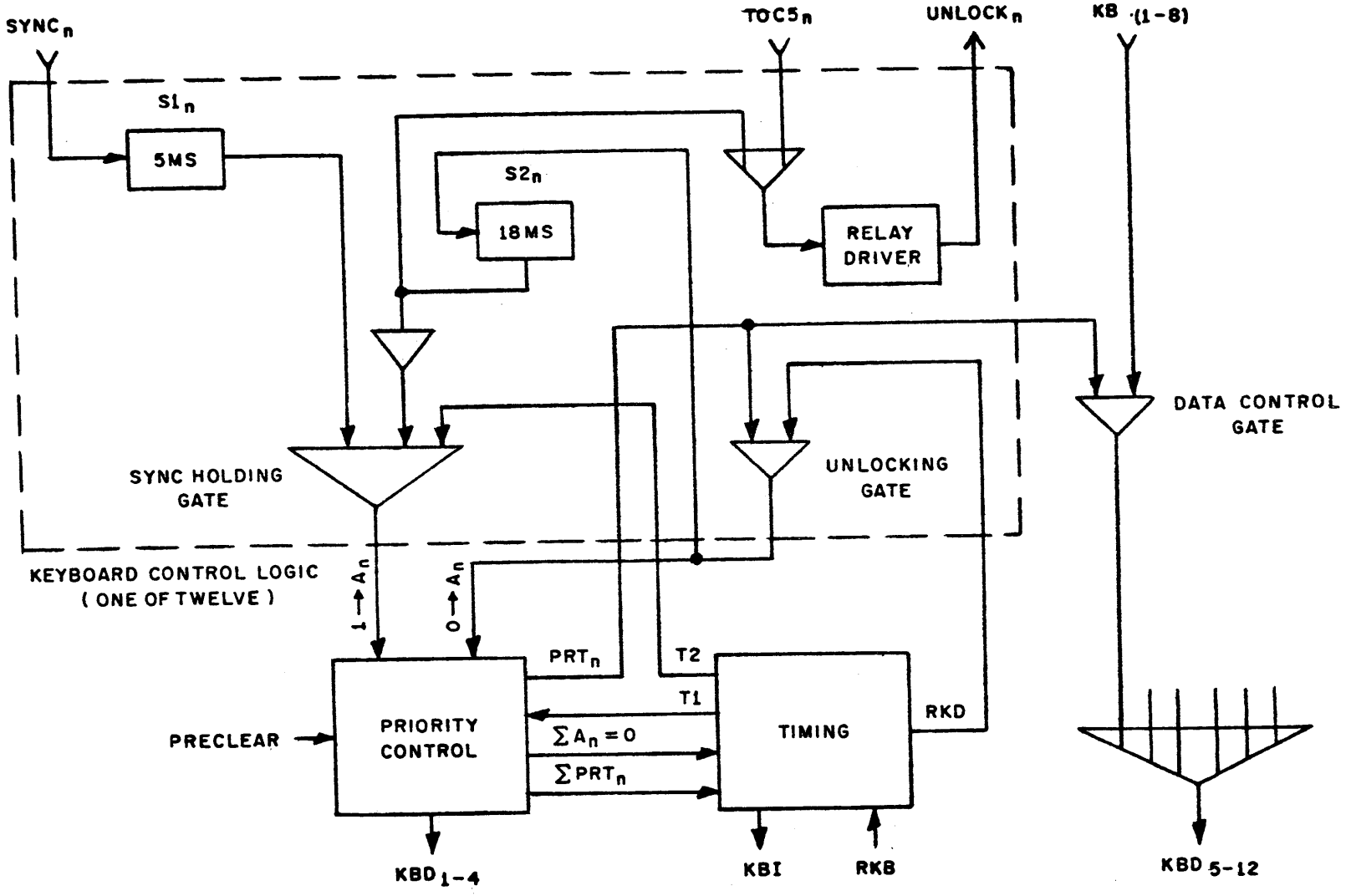


Figure 4-2. Keyboard Multiplexer Block Diagram

When power is initially applied, all flip-flops are cleared to "zero" such that timing phase T2 is set active. When an operator presses a key, the SYNC signal presented to the control logic fires timing S1. Timing S1 (5 milliseconds) is an integrating single shot set for maximum contact bounce frequency. When S1 recovers, the SYNC holding gate is enabled. With timing phase T2 active, all enabled SYNC holding gates generate a $1 \rightarrow A_n$ signal which sets the A_n flip-flop associated with the respective keyboard. With any A_n flip-flop set, the timing phase is set to T1. Note that T1 will remain active until all A_n flip-flops are cleared to zero.

With T1 active, the PRT_n signals are generated. Priority is such that the lowest numbered active A_n flip-flop is selected for the first data transfer. The PRT_n signals set the keyboard identifier (KBD_{1-4}) and enable the locked keyboard data gates (KBD_{5-12}). The PRT_n signals also are used to fire the KBI single shots which generate the keyboard interrupt for the PDP-1.

The RKB pulses received from the PDP-1 are gated with the active PRT_n signals to clear the A_n flip-flops and to fire timing S2 (18 milliseconds). Timing S2 energizes relay K1 in the respective keyboard. If the operator still has his finger on a key when the keyboard is unlocked, K1 will remain energized such that only one output is obtained from any depressed key.

For data transferred to the PDP-1, KBD_{1-4} contains the keyboard identifier with KBD_1 the most significant digit. Keyboard data KBD_{5-10} corresponds to KB_{1-6} respectively, with KBD_5 the most significant digit of the keyboard code. Keyboard switch data KS_{1-2} corresponds to KBD_{11-12} with KBD_{11} being associated with KS_1 (located to the left of the space bar).

4.3 DISPLAY CONTROLLER

The display controller consists of five major elements as shown on Figure 4-3. These elements are: (1) display control, (2) format generator, (3) vector generator, (4) character generator, and (5) drivers. The functions and the method of operation of each of these major elements are discussed in the following paragraphs. The signal notation shown in Figure 4-3 is the same as that used on READ logic schematics 9LO-8594.

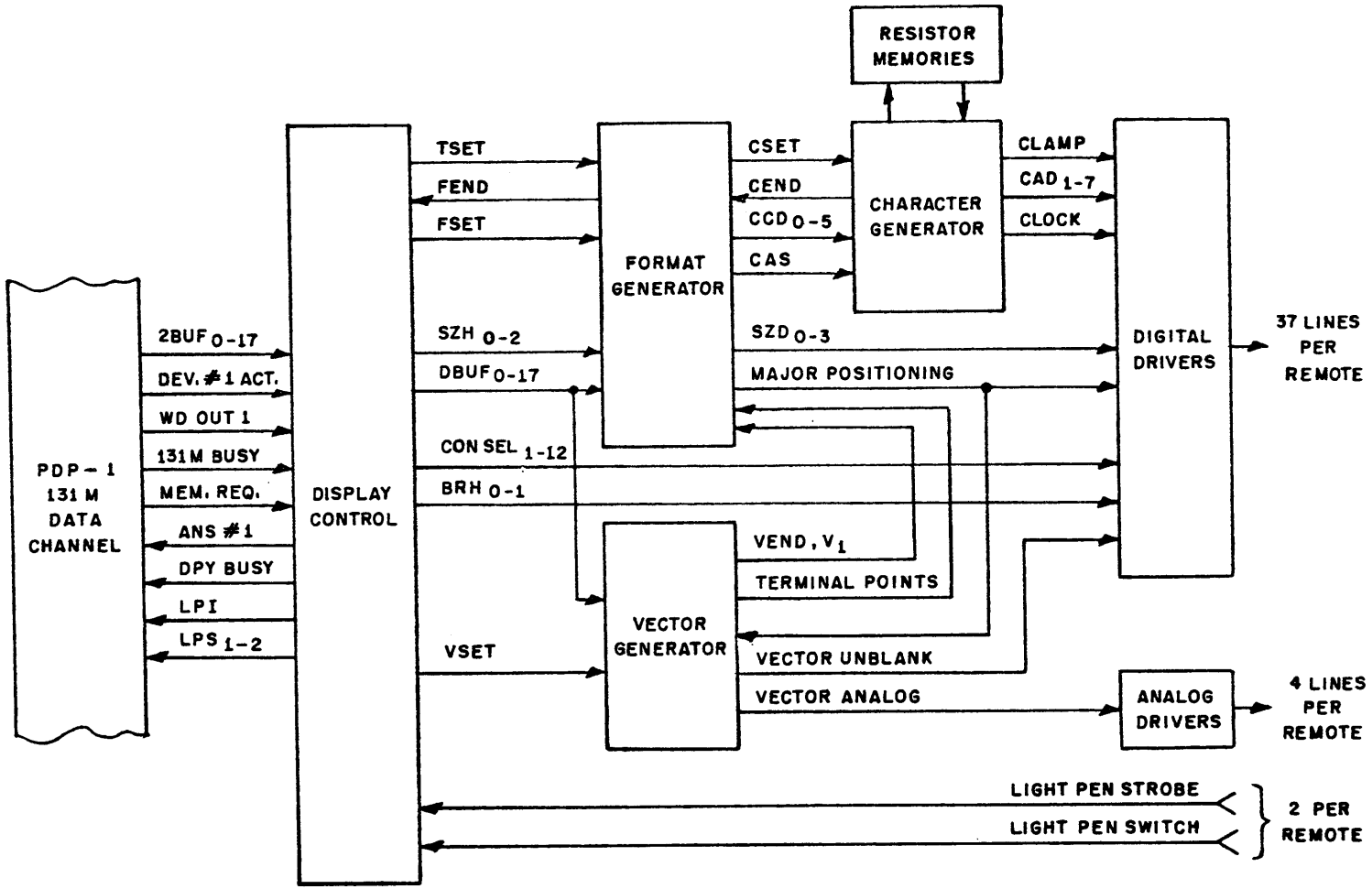


Figure 4-3. Display Controller Block Diagram

4.3.1 Display Control

The functions of the display control are to effect the data transfer between READ and the PDP-1 type 131M data channel and to set the operating modes in order to perform the display features. The display control contains an 18-bit data register ($DBUF_{0-17}$), timings T1-5 and M1-3, storage flip-flops (SZH_{0-2}, BRH_{0-1}, CMH_{0-1}), control flip-flops (DPC, WAV, DPB) and gating logic. Shown on Figure 4-4 is a combined timing and flow chart of the display control operation. The notations used on the chart are the same as on the display control logic schematics 9LO-8594, sheets 5 to 13.

When power is initially applied to the display control, the control flip-flops are cleared. The Device #1 Active and Word Out 1 signals received from the 131M are gated to set the display connected (DPC) flip-flop. Word Out 1 also fires timing T1 which sets the word available (WAV) flip-flop. WAV, memory request and display not busy (DPB=0) are gated to fire sequential timings T2 through T4. At time T2, DBUF is cleared and at time T3 the contents of 2BUF are transferred to DBUF. Display busy is set to one and WAV reset at time T4. If DPC is set and the 131M busy signal is active, the ANS#1 pulse is returned such that the 131M can put new data in the 2BUF and generate the Word Out 1 signal. Timing T4 also fires timing M1 in order that the contents of DBUF may be decoded.

If $DBUF_{0-5} = 74$, the escape signal is active and M1 fires sequential timings M2 and M3. At time M1, the command hold (CMH), size hold (SZH) and brightness hold (BRH) storage flip-flops are cleared provided new conditions are to be entered at time M2. At time M3, the Con Sel flip-flops are set or cleared consistent with the decoding of $DBUF_{5-10}$. In addition, if $DBUF_{5-10} = 0$, the light pen status (LPS_{1-2}) flip-flops are cleared. Also, if $DBUF_6 \neq 1$ and $DBUF_{7-10} \neq 0$, LPS_2 is set by M3 provided any intensified console light pen switch is on.

4.3.2 Format Generator

The major function of the format generator is to provide the digital information for positioning the CRT. In performing this function, the format generator also provides the control information for the character generator. For the following description refer to 9LO-8594, sheets 14 to 23 and to the format generator block diagram shown in Figure 4-5. In summary, the format generator operation begins when one of the control signals TSET, FSET, or V1 are received and ends when the FEND signal is returned to the display control.

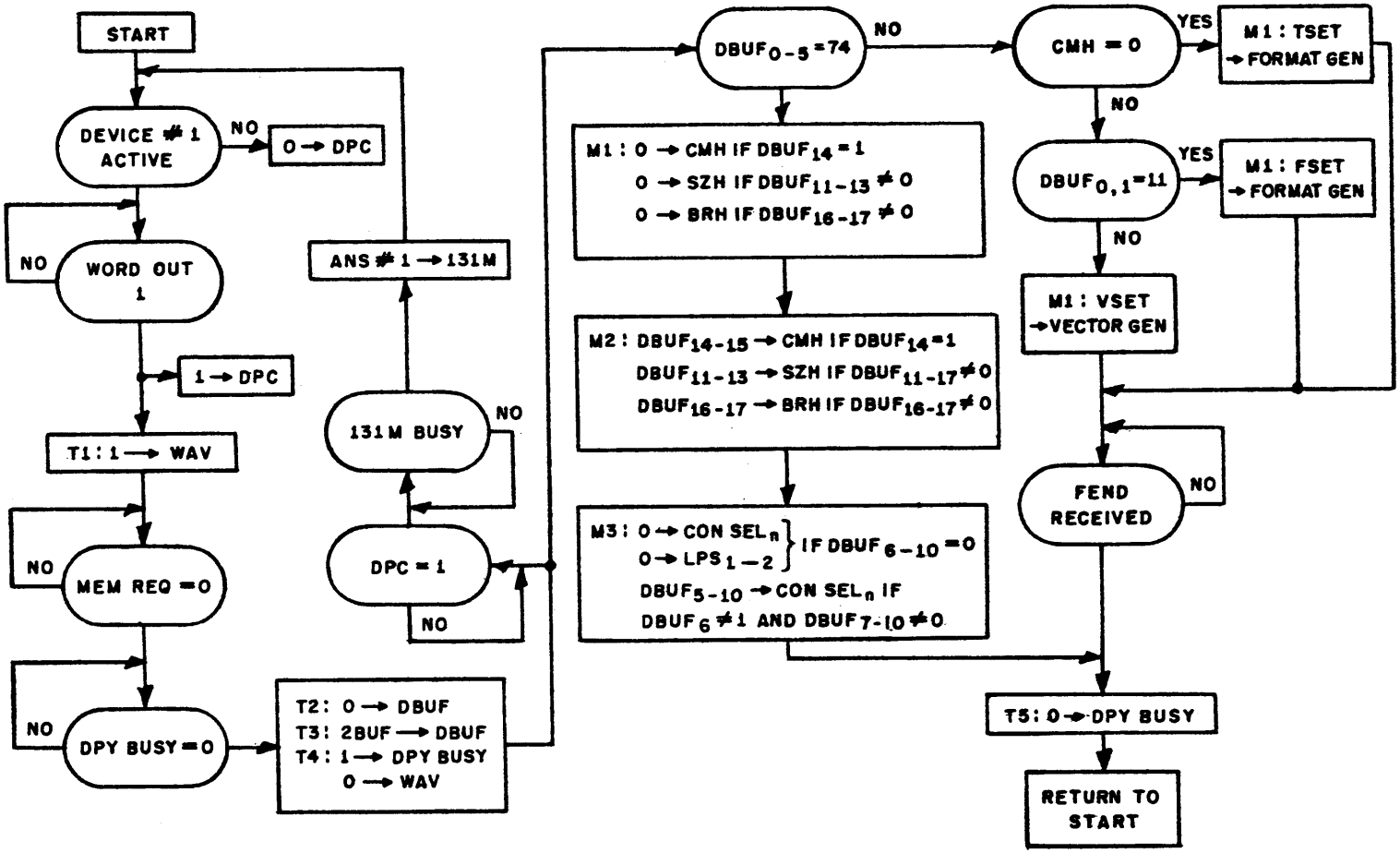


Figure 4-4. Display Control Flow Chart

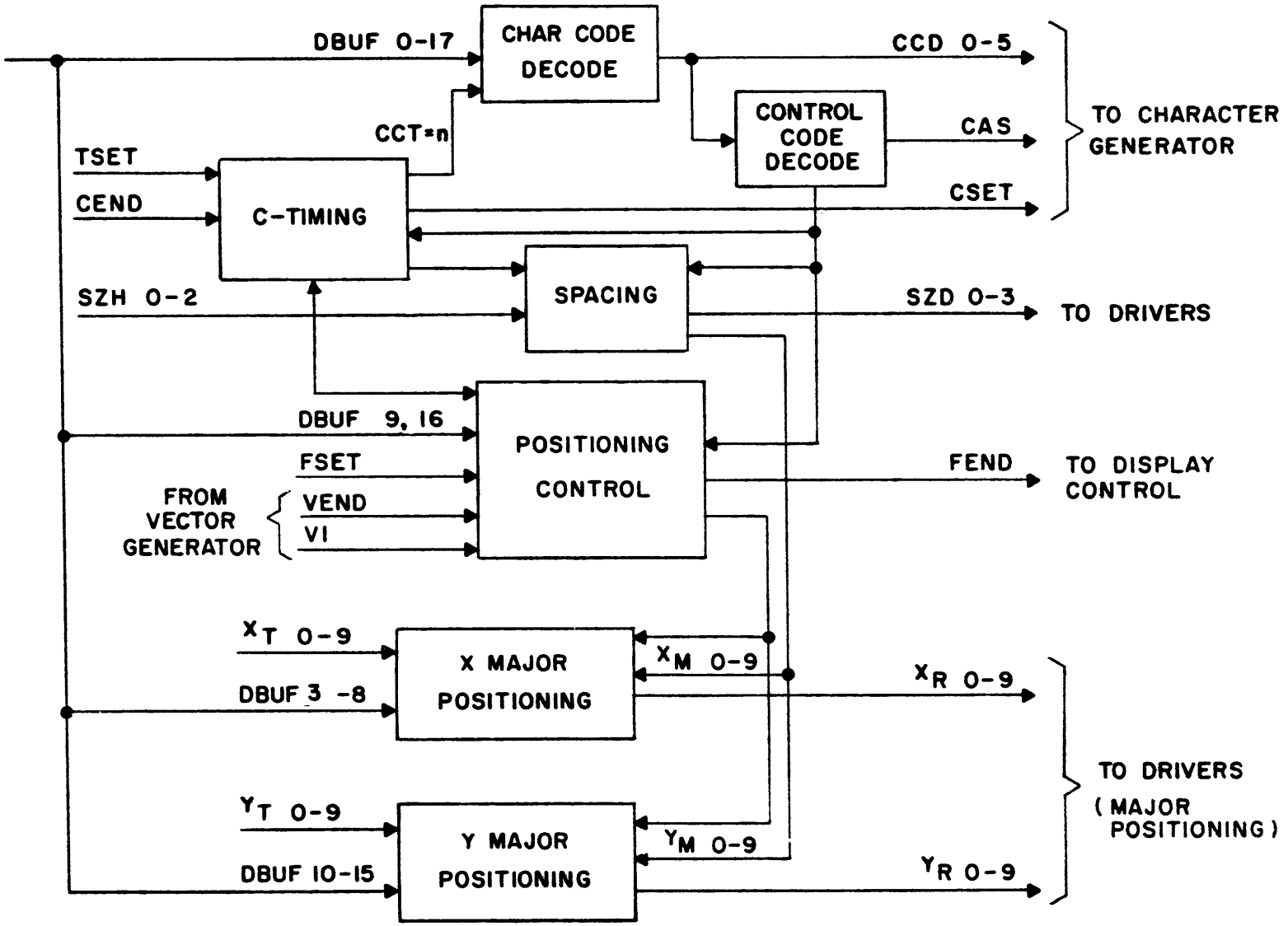


Figure 4-5. Format Generator Block Diagram

When the TSET signal is received, the format generator is set to typewriter format mode (TFM). In this mode, the C-timing block controls the format generator until the operations as specified by the three 6-bit characters contained in $DBUF_{0-17}$ are completed. The C-timing block contains timings C1-4, character counter CCT, control flip-flops (TFM, SP1, SCH2), and gating logic. The operation of typewriter format mode continues as follows:

The TSET pulse sets TFM to one and at its trailing edge fires timing C4. If a control code is not active, TSET furnishes the CSET pulse to the character generator to initiate the character drawing as specified by the character code CCD_{0-5}. (Note: Bit CCD_0 is most significant.) During times TSET and C4, the X_M counter (in the spacing block) is incremented according to the size bits SZH_{0-2}. When the CEND pulse is received, the contents of X_M are transferred to X major positioning register X_R. If the control flip-flop SCH2 $\neq 1$ and a control code is not active, the trailing edge of CEND fires C1 which furnishes the CSET pulse to the character generator. The trailing edge of C1 fires C4 such that these pulses increment the X_M counter mentioned above.

If the control code space (SPC) is active at time TSET or C1, these pulses will set the control flip-flop SPI and cause timings C3, C4, F4 and C2 to fire sequentially. Timings C3 and C4 increment the X_M counter. Timing C2 clears SPI; transfers X_M to X_R; increments CCT; and fires C1, provided SCH2 $\neq 1$.

If the control code carriage return (CAR) is active at time TSET or C1, the leading edge of these pulses fires F3 and their trailing edge causes F1 and F2 to fire sequentially. During time TSET or C1, X_M is cleared and the Y_M counter incremented according to the size bits. At time F1, X_{M0} and X_{M9} are set to one. At time F2, X_M is gated to X_R and Y_M gated to Y_R. Timings F3, at its trailing edge, causes F4 and C2 to fire sequentially, provided SCH2 $\neq 1$; C2 increments CCT and on its trailing edge fires C1.

If the control code NO-OP or case shifting (CASU, CASD) is active, TSET or C1 on its trailing edge fires F4 and C2 sequentially. At time TSET or C1, the CAS flip-flop is set consistent with control codes $(70)_8$ or $(72)_8$. Timing C2 increments CCT and fires C1 on its trailing edge.

When the last character is detected, i.e., CCT=2, C1 sets the SCH2 flip-flop. With SCH2 set to one, at time F4 or C4, TFM is cleared to zero. If the CEND pulse is received, SCH 2 and CCT are cleared and the FEND pulse generated by CEND. If F4 fires, TFM and CCT are cleared. The FEND pulse is generated by F4 and C2 clears SCH2.

When the FSET pulse is received, the format generator is set to random position the CRT. The leading edge of FSET causes F3 and F4 to fire sequentially. The trailing edge of FSET fires F1 and F2 sequentially. FSET clears X_M or Y_M if new data is to be entered at time F1. At time F2, X_M and Y_M are gated to X_R and Y_R respectively. In this mode, the FEND signal is generated by F4.

During vector generator operation, the V1 pulse clears both X_M and Y_M. At time VEND, the terminal points (X_T, Y_T) computed in the vector generator are gated to both X_M, X_R and Y_M, Y_R. The trailing edge of VEND fires F4 which generates the FEND signal.

When power is initially applied, the control flip-flops, major positioning counters and registers are cleared such that the initial starting point for the CRT is the center of the screen.

4.3.3 Vector Generator

The vector generator contains an adder, two 10-bit storage registers (X_T and Y_T), timings V1-6, control flip-flops (VEM, ADX and ADY) and the analog circuits necessary to generate the delta X and delta Y components of the vector waveforms. For the following description, refer to the vector generator block diagram shown in Figure 4-6 and logic schematics 9LO-8594, sheets 37 to 51. In summary, the vector generation operation begins when the VSET pulse is received and ends when the VEND pulse is returned to the format generator.

The VSET pulse sets control flip-flops, VEM and ADX, and rires sequential timings V1-6. The setting of VEM activates the analog circuits and enables data gates to the adder. With ADX set, $DBUF_{3-8}$ bits and X_R are gated to the adder. At time V1, both X_T and Y_T are cleared. At time V2, the outputs of the adder are gated to X_T. At time V3, ADX is cleared and ADY set. V3 also increments X_T by one, provided the sign of delta X is negative ($DBUF_2 = 1$). With ADY set, $DBUF_{11-17}$ bits and Y_R are gated to the adder. At time V5, the outputs of the adder are gated to Y_T. V6 clears ADY and increments Y_T by one, provided the sign of delta Y is negative ($DBUF_{10} = 1$). The adder contains a complement network such that if the vector sign bits are negative, the complements of the respective DBUF bits are gated to the adder. The adder performs straight binary addition with overflow in the most significant digit ignored.

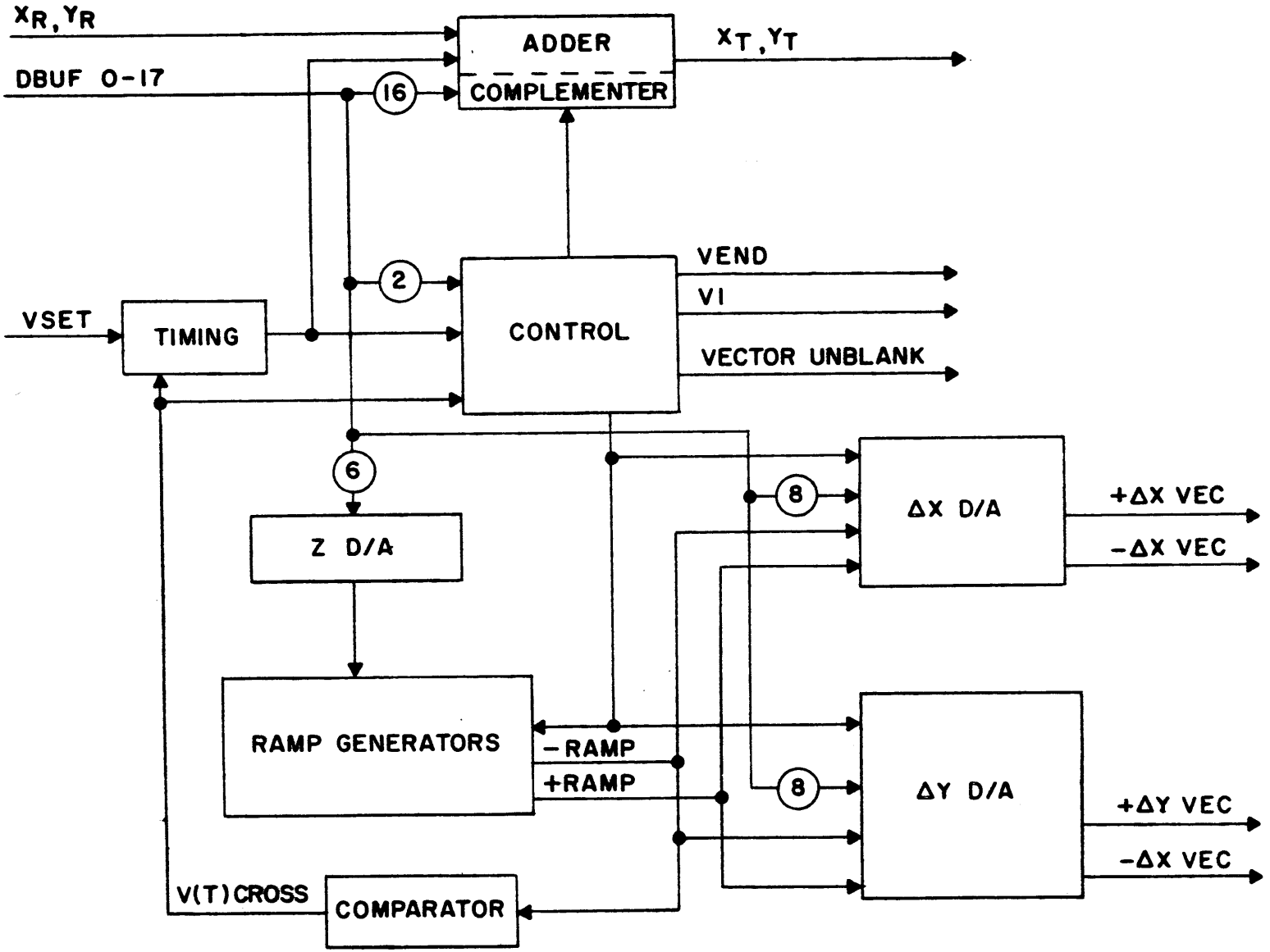


Figure 4-6. Vector Generator Block Diagram

As mentioned previously, the setting of VEM activates the analog circuits. VEM and the respective sign bits of the vector are gated with DBUF to form the digital data for the delta X and delta Y digital-to-analog converter circuits. The reference voltages for these circuits are linear ramp voltages which start when VEM is set to one. The slopes of the linear ramps are derived from the Z D/A whose inputs are the three most significant digits of both the delta X and delta Y vectors. The period T of the linear ramp is controlled by the comparator circuits. When the ramp reaches a fixed voltage denoted by V_{MAX}, the signal from the comparator fires sequential timings V6 and V7 and causes the ramp to maintain the V_{MAX} level until V7, at which time VEM is cleared causing the levels of the ramps to be clamped to their minimum voltages. Denoting the decimal value of the three most significant digits of the delta X or delta Y vector by D, the period T of the linear ramp is

$$T = 10 \frac{(D+2)}{6} \text{ microseconds for } D \neq 0, \text{ and}$$

$$T = 5 \text{ microseconds for } D = 0.$$

The vector unblanking signal is active between V_{MIN} and V_{MAX} signals if an intensified line is to be drawn. V_{MIN} is a signal from the comparator that becomes active when the reference ramp crosses ground voltage. If the end point is to be intensified, the vector unblanking signal is generated by V6. For blanked vectors, the vector unblanking signal is not made active during the above operation.

The comparator circuits located on module D7 (398-6173-1) are two adjustable Schmitt triggering circuits that detect V_{MIN} and V_{MAX} levels. The ramp generators are located on modules D5 (398-6171-1) and D6 (398-6172-1). The adjustment located on module D5 is for centering the period T between the limits specified by the above equation. The adjustments on module D6 (positive ramp generator) are for setting the levels of the positive ramp such that the output swings from -2 volts to +8 volts when the output level of the negative ramp generator swings from +2 volts to -8 volts.

4.3.4 Character Generator

This section of the character generator described in the paragraph generates the digital data as required to effect character drawing. The conversions of the digital data to the X and Y analog voltages as accomplished in the remote consoles are described in paragraph 4.4. A block diagram of

the part of the character generator located in the display controller is shown in Figure 4-7. For the following description, refer to logic schematic 9LO-8594, sheets 24 to 36.

The 3-megacycle oscillator fires timings T1-3 sequentially on the positive transition of its square wave output. When the CSET pulse is received, the SCT flip-flop is set to one. At the trailing edge of the CSET pulse flip-flop, CST is set to one. With both of these flip-flops set, the trailing edge of T2 sets the CLP flip-flop. When SCT is set to one, the CLAMP signal to the remote consoles is set to ground level. The timing pulses, T1 and T2, when gated with CLP are denoted B1 and B2 respectively. Timing T3, when gated with CLP, generates the CLOCK signals to the remote console.

The MCC counter is a 2-bit counter which is incremented by timings B1 and B2. When the counter reaches binary 11, it is immediately reset to binary zero by an MCC pulse before the next B1 and B2 pulses occur. This MCC pulse also increments the 4-bit segment counter by one. If the selected character does not contain a "wired-in" character end code, the CEND pulse is generated when the segment counter equals $(1000)_2$ at time B2.

The inputs to the fixed memories for selecting the character to be drawn and the corresponding segment digital data for the respective character are obtained by an X-Y addressing scheme. The Y part of the address contains the character code; the X part of the address is sequentially accessed during character drawing. All characters have the same X addresses for any given position of the segment counter.

Each fixed memory contains seven resistor-diode matrices such that a word read out from a specified address contains seven bits of character drawing information. A typical "wired-in" memory is shown in Figure 4-8. An X-Y intersection (memory address) is selected when the Y_D output is at -30 volts and the X_D output is at -10 volts. Where these intersections contain a resistor R, a "one" is read from the memory. Where these intersections do not contain a resistor, a "zero" is read out.

The seven matrices are denoted +X, 2X, -X, +Y, 2Y, -Y and Z. A bit read from each of these matrices from a specified address constitutes a 7-bit word. The 7-bit word when gated into the character analog data register forms the character drawing data for the "wired-in" segments of the character. The outputs of the character analog data register CAD_{1-7} correspond respectively to the order of the matrices noted above.

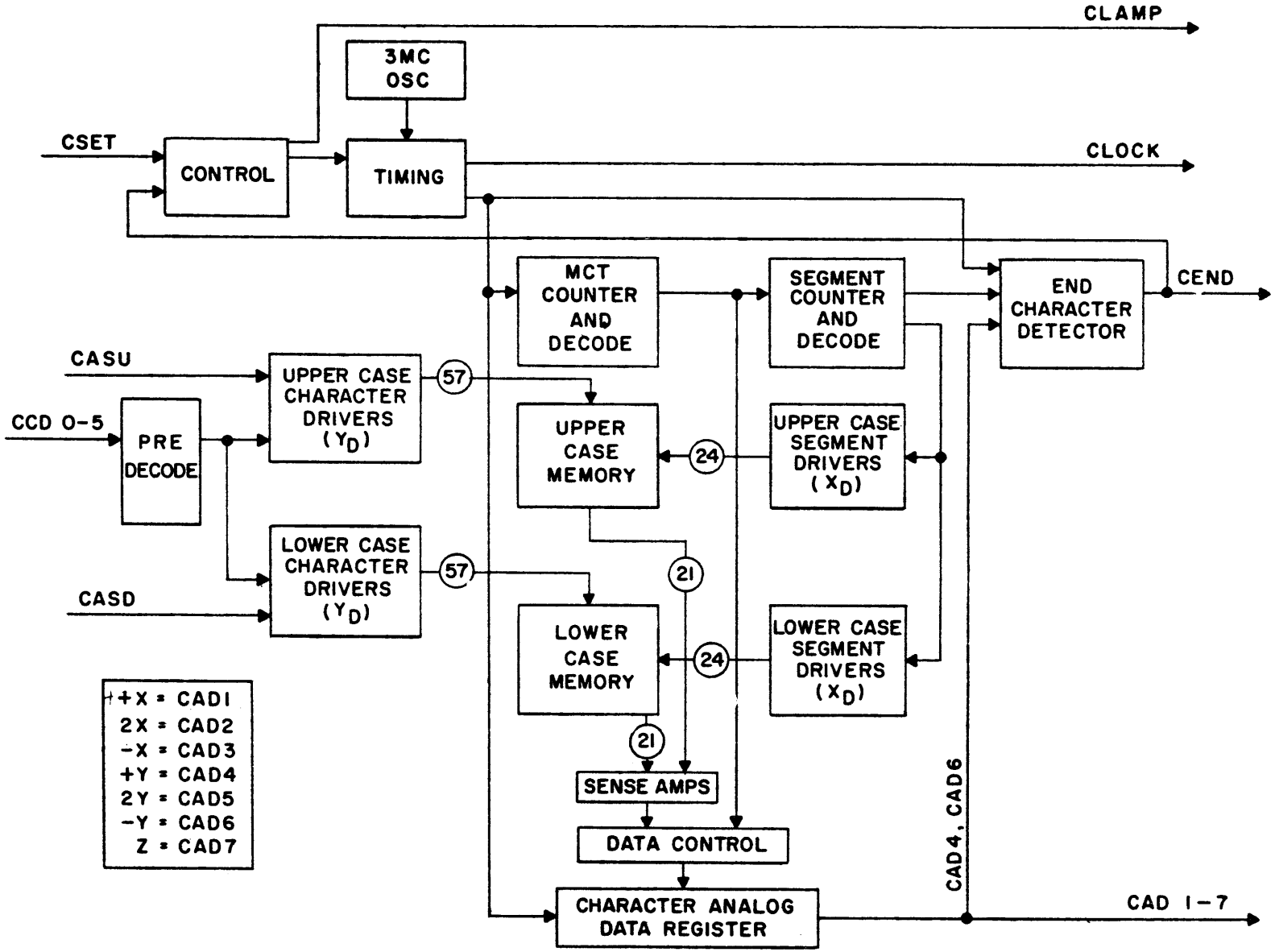


Figure 4-7. Character Generator Block Diagram

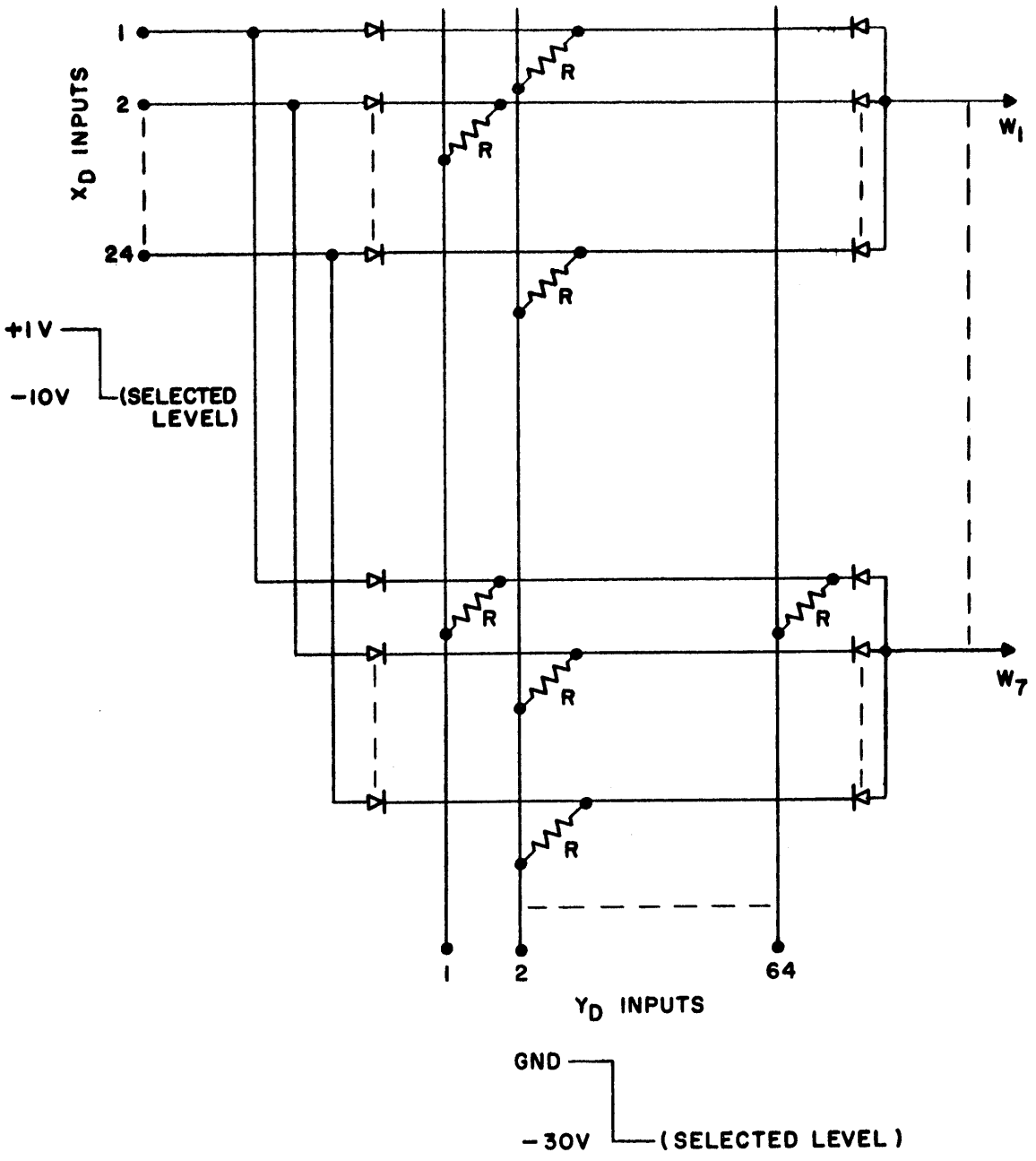


Figure 4-8. Typical Resistor Memory

The READ character generator is wired such that the segment counter selects three successive X addresses from each of its eight possible states. The memories are wired such that the corresponding three data words are active as specified by the state of the counter. The wiring of the memories are shown on schematics 590-1082-4, sheets 20 to 23, for each of the 14 printed circuit assemblies.

In summary, the character generator begins operating when the CSET pulse is received. The setting of the CLP flip-flop synchronizes the B1-3 timing chain such that each segment of the character is drawn in the same amount of time. The character analog data register converts the stored memory data to that digital data as required by the remote consoles. The end character detector generates the CEND pulse either by the wired-in code or detecting overflow in the segment counter. The wired-in code that denotes character drawing is complete in the condition where both CAD_4 (+Y) and CAD_6 (-Y) are both equal to one. The CEND pulse is furnished to the format generator and also clears the character generator to accept the next subsequent CSET signal.

4.3.5 Driver Interface

The driver interface contains those driver circuits necessary to drive the remote console signals the required distance of 75 foot coax (RG/915U). The block diagram of the driver interface is shown in Figure 4-9. Logic schematic 9LO-8594, sheets 67 to 75, show the wiring of the individual circuits.

The digital signals are driven by cable driver module D11 (398-6177-2). The digital signals are driven on a one-to-one basis, i.e., one driver per remote signal, except for the major positioning, brightness and size levels. For these latter signals, the digital signals are driven to six remote consoles in parallel. The vector analog signals are driven by analog driver module D12 (398-6178-1). The adjustments located on these modules are for setting the vector unblanking signals relative to position accuracy for each remote console. The preanalog driver module D4 (398-6170-1) drives six D12 modules.

4.4 REMOTE CONSOLE LOGIC

The remote console logic shown in Figure 4-10 are those portions of the remote console electronics which are contained in the two pan logic rack. For the following description, refer to logic schematic 9LO-8594, sheets 1 to 4.

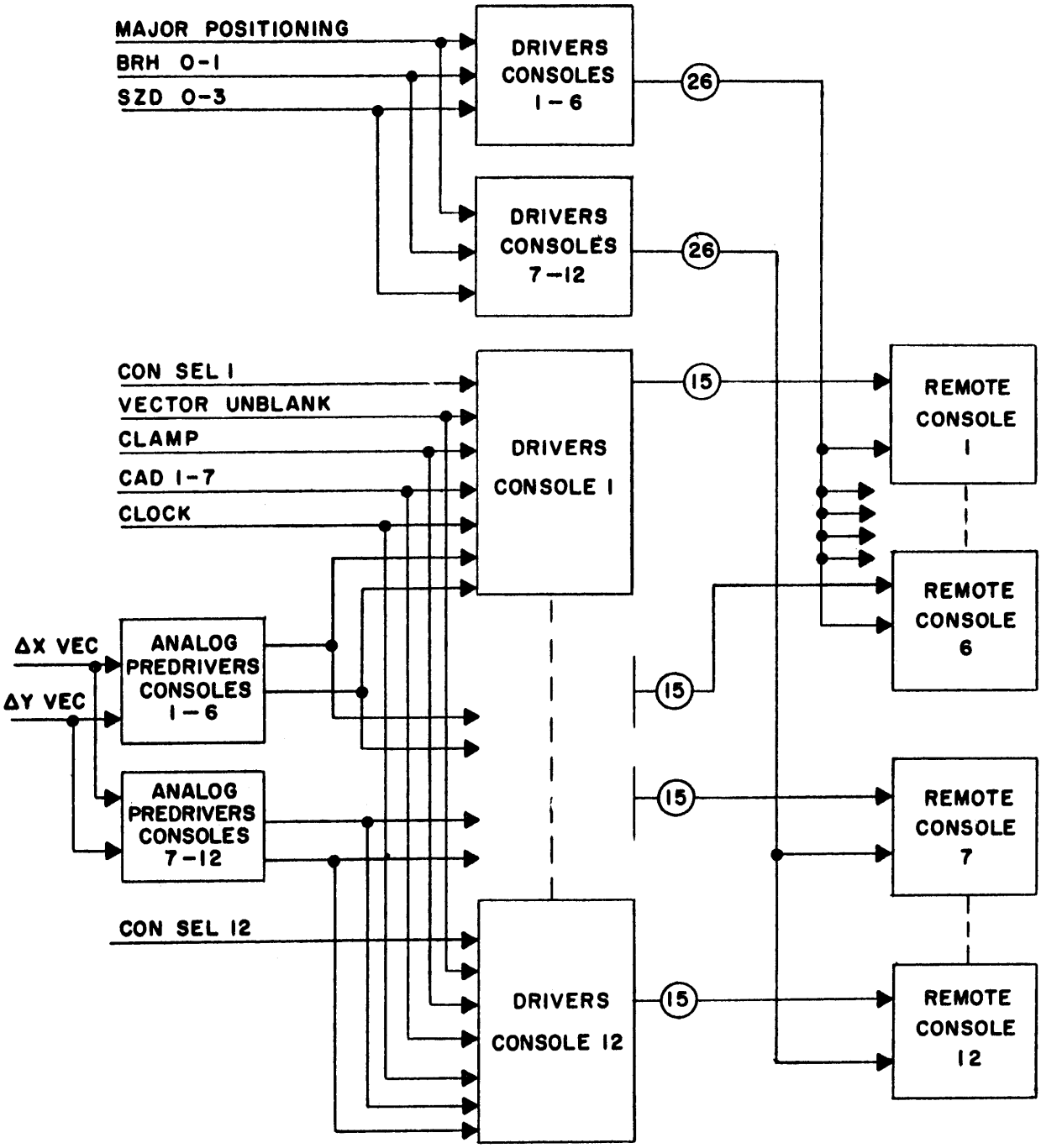


Figure 4-9. Driver Interface Block Diagram

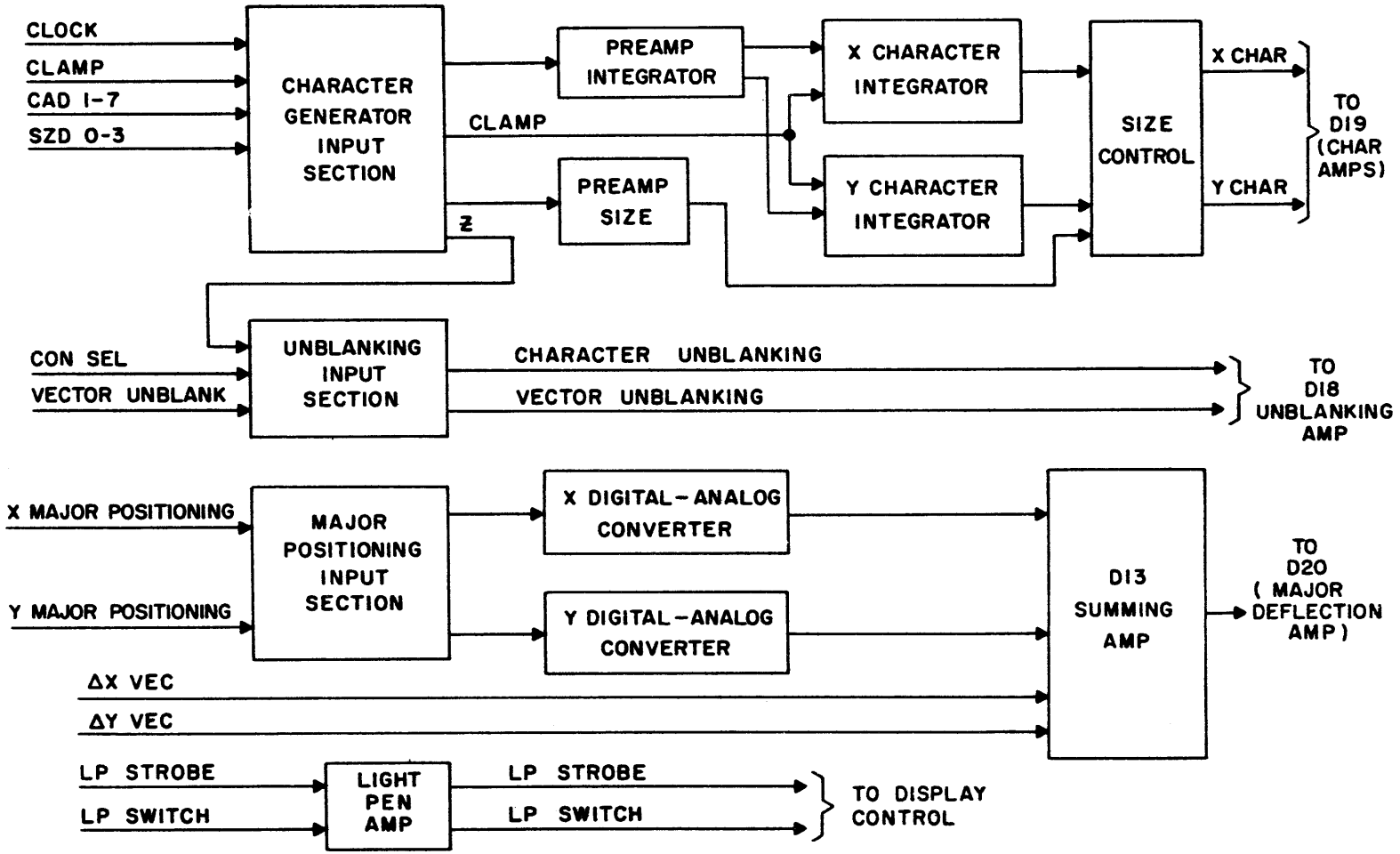


Figure 4-10. Remote Console Logic Block Diagram

The character generator input section contains storage flip-flop (CLP), timings X1-2 and a 7-bit data register. When the CLP flip-flop is set, the CAD_{1-7} data is gated into the data registers with the clock signal. The CLP flip-flop is set when the clamp signal is at -5 volts. The timing chain X1-2 is used to reset CAD_7 (character unblanking) relative to the delay differences in the character deflection and unblanking amplifiers. The CLP flip-flop (when set to one) turns off the clamping transistors in the integrators allowing the integrators to produce the waveforms as specified by the CAD_{1-6} data chain. The outputs of the data register drive the integrator preamplifier module D15 (398-6181-2). This module converts the logic levels of the data register to those required by the integrator. The waveform generated by the integrator modules D14 (398-6180-1) are attenuated on the size control module D8 (398-6174-1) consistent with the decoding of the four transmitted size bits SZD_{0-3}. The signal levels of the size bits are converted, on module D16 (398-6212-1), to those required by the size control module. The outputs of the size control module are the inputs to the character amplifier modules D19 (398-6197-1). The character amplifier modules are not located in the logic rack and are described in paragraph 4.6.1.

The major positioning input section contains the digital-to-analog ladder driver modules D9A (398-6175-1). The outputs of these modules drive the digital-to-analog ladder network module D10A (398-6176-1). The outputs of the driver modules connect the ladder inputs either to ground or to the reference voltage (-10 volts). The outputs of the ladder networks are the inputs to the summing amplifier module D13 (398-6179-1). This module is described in paragraph 4.5.1. The four vector transmitted signals are fed directly to the inputs of the summing amplifier.

The unblanking sections are gating logic circuits which inhibit character and vector unblanking unless that remote console is selected to be intensified.

The light pen signals transmitted to the display control are furnished by the light pen amplifier module D23 (398-6331). The inputs to the amplifier are from the light pen assembly as described in paragraph 5.2.5.

4.5 MAJOR AXES DEFLECTION

The major deflection consists of D13 (X and Y summing amplifiers), D20-X (X axis yoke driver), D20-Y (Y axis yoke driver) and a 25-microhenry single ended deflection coil.

4.5.1 D13 (Summing Amplifier 398-6302)

The X and Y summing amplifiers are dc coupled, wideband amplifiers which sum the plus and minus vector ramps with the major position steps as determined by the X and Y D/A ladder networks. In addition, the amplifiers provide the means to center the CRT display by adjusting the dc level of the composite deflection waveforms with the X and Y DISPLAY CENTER front panel controls and to adjust the display size by varying the gain with the X and Y DISPLAY SIZE front panel controls. R4 and R5 potentiometers match the vector ramp amplitudes with the major position steps. R1 potentiometer sets the dc level at the junction of resistors R8 and R9 to the same as the dc level at the junction of R3 and R15.

4.5.2 D20-X and D20-Y (X and Y Axis Yoke Drivers)

The yoke drivers, D20-X and D20-Y, are direct-coupled feedback amplifiers which convert to the composite X and Y deflection voltage outputs of D13 into equivalent current waveforms through their yoke loads. The amplifiers sense the yoke currents through a 1-ohm resistor in series with the yokes and compare these signals with the input voltage signals to reduce the resulting difference voltages to zero.

The input stage (Q_5) of the D20 circuits has the input signal applied to the base and the feedback voltage applied to the emitter; thus, Q_5 provides both comparison of the output current to the voltage input and amplification. Q_1 provides level translation and voltage gain while Q_6, Q_7, and Q_2 provide the necessary current gain to drive the output transistors. The eight transistors in the output stage operate with approximately 1-ampere quiescent current; therefore, the yoke current is zero. When a positive input signal is applied, the current in the power transistors connected to the +40-volt power supply increases while the current through the power transistors connected to -40-volt power supply decreases. The result is a net current flow through the yoke such that approximately 1/2-volt change at the input provides approximately 1/2 ampere change through the yoke and approximately 1/2 inch change in deflection at the CRT presentation.

4.5.3 Deflection Yoke

The major axis deflection yoke is a high resolution, precision deflection yoke manufactured by Constantine Engineering Laboratories Company and is designated HD428-5670. The yoke is single-ended for 42° deflection in both the X and Y axis at 20 kv. Each coil is 25 microhenries such that when the CRT is operated at 16 kv, the current to deflect one radius is approximately 4.5 amperes.

The only adjustment necessary for the major yoke is rotation. This is accomplished by loosening the yoke mounting clamp and rotating the yoke until a horizontal trace is aligned.

4.6 CHARACTER DEFLECTION

The character deflection consists of D19-X (X axis yoke driver) D19-Y (Y axis yoke driver) and a seven microhenry single-ended character deflection coil.

4.6.1 D19-X and D19-Y (X and Y Yoke Drivers)

The X and Y yoke drivers are direct-coupled feedback amplifiers to convert analog deflection voltages into identical yoke current waveforms. R4 of the D19 circuits adjusts the bias of Q4 for operation in the class A region and provides the feedback for dc stability. The X and Y character size potentiometers, R103 and R104, adjust the attenuation of the input signal and, therefore, the character size of the CRT presentation.

4.6.2 Character Deflection Yoke

The character deflection yoke, designated AW414-730, is a high-frequency writing yoke manufactured by Constantine Engineering Laboratories Company. The yoke is single-ended for 2 degrees deflection in both the X and Y axes at 10 kv. Each coil is 7 microhenries and requires approximately 1.2 amperes to deflect approximately 1/2 inch at the CRT.

The only yoke adjustment necessary is rotation. This is accomplished by loosening the character yoke mounting clamp and aligning the character in the Y axis.

4.7 UNBLANKING AMPLIFIER

The unblanking amplifier, designated D18, provides the cathode drive to unblank the CRT at character or vector time. The amplifier is dc-coupled, Class A, and operated with the output or CRT cathode at +100 volts during blank time. During unblank time, a negative signal at the input causes the output to swing more negative (to approximately +30 volts) and reduce the grid to cathode cut-off voltage and turn on the tube. R4 and R5 potentiometers adjust the relative brightness of characters and vectors. Inputs designated B1 and B2 select one of three levels of brightness by summing their input levels through R7 and R17. Potentiometer R1 adjusts the relative difference between the three brightness levels. R6 potentiometer sets the output transistors, Q4 and Q5, just out of cut-off for high-speed switching.

The CRT tube socket is mounted directly on the D18 printed circuited board, therefore, as inputs to the D18 card there are also filaments, G1 voltage, G2 voltage, and the 3-4 kv focus voltage.

4.8 CATHODE RAY TUBE AND HIGH VOLTAGE CIRCUITS

The cathode ray tube is a 16-inch, magnetic deflection, electrostatic focus type with the following characteristics:

Phosphor	P28
Deflection Angle	52°
Focus Electrode Voltage	3, 000 to 4, 000 volts dc
Accelerator Voltage	16, 000 volts dc
Grid Cut-off Voltage G1	-40 to -70 volts dc
G2 Voltage	200 volts dc

The tube, designated 16M31P-28, is designed specifically to utilize the two yokes and to operate at a high electrostatic focus voltage to eliminate arcing within the gun structure of the tube.

The accelerator voltage is generated by a 16-kv power supply located in the rear right-hand corner of the console. The 16 kv is divided down by high voltage resistor divider networks located in the high voltage chassis to provide the G2 voltage and electrostatic focus voltage. The voltage regulator tube, GVA-3000, regulates the focus voltage and enables the front panel FOCUS CONTROL to be operated at a low potential. The G2 voltage is adjusted by the potentiometer accessible at the top of the high voltage chassis. Minimum G2 voltage is obtained when the pot is turned fully clockwise.

4.9 DISPLAY POWER CONTROL

4.9.1 Remote Power

The following are voltages supplied to the console from power supplies located in the READ common logic unit.

+16 vdc	+8 vdc	-30 vdc
-10 vdc	-8 vdc	

In the power sequence operation of the common logic, the -30 volts dc is the last voltage to come ON and will do so only after all other voltages in the common logic unit are on. All remote voltages are fused at the rear of the console by 3-ampere fuses.

4.9.2 Local Power

The following voltages are supplied by a power pack located below each console.

6.3 vac at 1 ampere	unregulated
+40 vdc at 12 amperes	±0.5% regulation
-40 vdc at 12 amperes	±0.5% regulation
+100 vdc at 0.2 ampere	±0.5% regulation
+28 vdc at 2 amperes	±5% regulation

The 6.3 volts ac provides the filament voltage for the CRT. The +40 volts dc are the deflection voltages for both the character amplifiers and major position amplifiers. The +100 volts dc provides the unblanking and overall intensity voltage for the CRT. The +28 volts dc provides power for the keyboard.

The power packs' voltages with the exception of 6.3 volts ac and 28 volts dc are monitored to detect a power failure. Should a voltage fail, relay contacts K1, K2, or K3 will open and turn off the CRT high voltage power supply and cause the CRT to be cut off.

The power pack is manufactured by Deltron, Incorporated, Philadelphia, Pennsylvania, and is designated Model 2616.

4.9.3 Power Sequence Chassis

The power sequence chassis is located in the power pack cabinet and performs the following functions. See Figure 4-11 and schematic drawing 9LO-8550.

4.9.3.1 Power Sequence

When all remote voltages from the common logic unit are ON, the -30 volts is present. The -30 volts closes K1 which enables the high voltage to be turned on and energizes L101 in the control panel indicating LOGIC is ON.

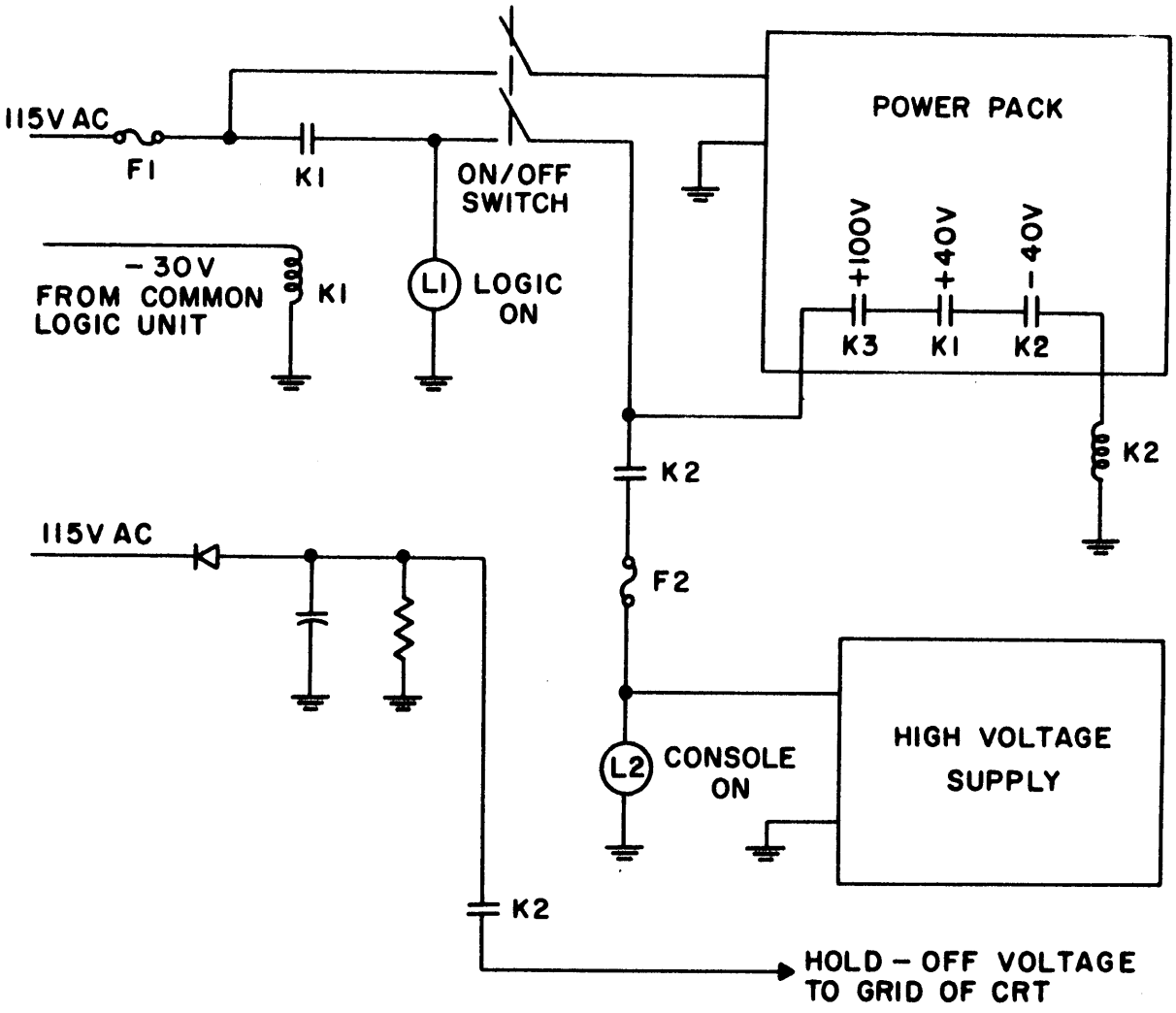


Figure 4-11. Power Sequence Chassis Simplified Diagram

When the ON-OFF switch is switched ON, the primary 115 volts ac is applied to the power pack. If all voltages come ON, relay K2 is energized which applies primary power to the high voltage power supply and removes the CRT hold-off voltage from the grid. L102 on the control panel is energized indicating the console and high voltage is on.

4.9.3.2 CRT Protection

Should a power failure occur in either the common logic or console power pack, a negative hold-off voltage will be applied to the grid of the CRT. The hold-off voltage is rectified 115-volts ac line voltage and will be present at the CRT grid as long as the power card is connected to a 115 volts ac receptacle. The CRT, therefore, cannot come out of cut-off until (1) the common logic unit is turned ON, (2) the console ON/OFF switch is ON, (3) all voltages in the power pack are on.

SECTION 5

PROGRAMMING

5.1 PDP-1 INPUT/OUTPUT INSTRUCTIONS

READ is wired to the PDP-1 as follows:

a. The display controller is wired-in as Device No. 1 on the DEC type 131M Input/Output Channel.

b. The keyboard multiplexer is wired such that the keyboard interrupt (KBI) occurs on sequence break channel 11. On the execution of the rkb instruction (720037) by the computer, the keyboard identifier, the auxiliary buttons, and the code for the character struck are transferred to the computer's I/O register.

c. The light pen is wired such that the light pen interrupt (LPI) occurs on sequence break channel 3. Two light pen status bits are set in the I/O register on check status instruction CKS (720033). Bit 14 is 1 if the light pen switch is depressed and bit 15 is 1 if the light pen has seen a point.

5.2 DISPLAY CONTROLLER CONTROL AND DATA FORMAT

The display controller operates on the 18-bit computer word received from the DEC 131M Data Channel in three basic data formats. These data formats are control word, vector, and typewriter modes.

5.2.1 Control Word Format

The control word format is defined as an 18-bit word having octal 74 as the first character in the data channel word. Wherever this character is detected in the position stated, the display controller will operate on the remaining 12 bits as follows:

5.2.1.1 Console Designation (Data Channel Word$_{6-10}$)

a. Octal code 00 blanks all consoles and clears the light pen status bits.

b. Octal codes 01 through 17 specify that the corresponding number console should be added to the list of those currently intensified. They also connect the light pen and light pen switch to the status bits.

c. Octal codes 20 through 27 specify that no change in consoles intensified should be made.

5.2.1.2 Size Control (Data Channel $_{11-13}$)

a. Octal code 0 does not change.

b. Octal codes 1 through 7 set the corresponding character size.

Octal 1 sets the smallest character size.

Octal 7 sets the largest character size.

5.2.1.3 Mode Control (Data Channel $_{14-15}$)

a. Octal codes 0, 1 do not change mode.

b. Octal code 2 enters typewriter mode.

c. Octal code 3 enters vector mode.

5.2.1.4 Brightness Control (Data Channel $_{16-17}$)

a. Octal code 0 does not change brightness level.

b. Octal codes 1 through 3 set the corresponding brightness level.

Octal 1 sets minimum brightness.

Octal 3 sets maximum brightness.

The time required to operate on a control word is approximately 1.3 microseconds.

5.2.2 Vector Mode Format (See Figure 5-1)

Two vector mode formats are utilized in the READ display system. Type 1 vector words cause display controller to trace vectors, plot points and fine positioning of the CRT. Type 2 vector words position the CRT to points specified by the data word. The time required to operate on a Type 1 word varies with vector length from 5 to 15 microseconds. The time required to operate on Type 2 word is approximately 18 microseconds.

5.2.2.1 Vector Mode 1

The vector mode 1 format word is operated as follows:

5.2.2.1.1 Control (Data Channel Word $_{0-1}$)

a. Octal code 0 - display vector from starting point to ending point.

b. Octal code 1-1 display end point.

c. Octal code 2 - position beam to end point. Do not intensify.

5.2.2.1.2 Delta X Sign (Data Channel Word $_{2}$) - If data channel word $_{2}$ is equal to one, the delta X vector component is drawn in the negative direction.

5.2.2.1.3 Delta X Magnitude (Data Channel Word $_{3-9}$) - Specifies the magnitude of the delta X vector component. Delta X is a 7-bit number which is added (during vector drawing) to the X major position coordinate.

5.2.2.1.4 Delta Y Sign (Data Channel Word $_{10}$) - If data channel word $_{10}$ is equal to one, the delta Y vector component is drawn in the negative direction.

5.2.2.1.5 Delta Y Magnitude (Data Channel Word $_{11-17}$) - Specifies the magnitude of the delta Y vector component. Delta Y is a 7-bit number which is added (during vector drawing) to the Y major position coordinate.

5.2.2.1.6 Arithmetic - Note the vector data above are given in sign magnitude arithmetic, not the one's complement arithmetic used in the PDP-1

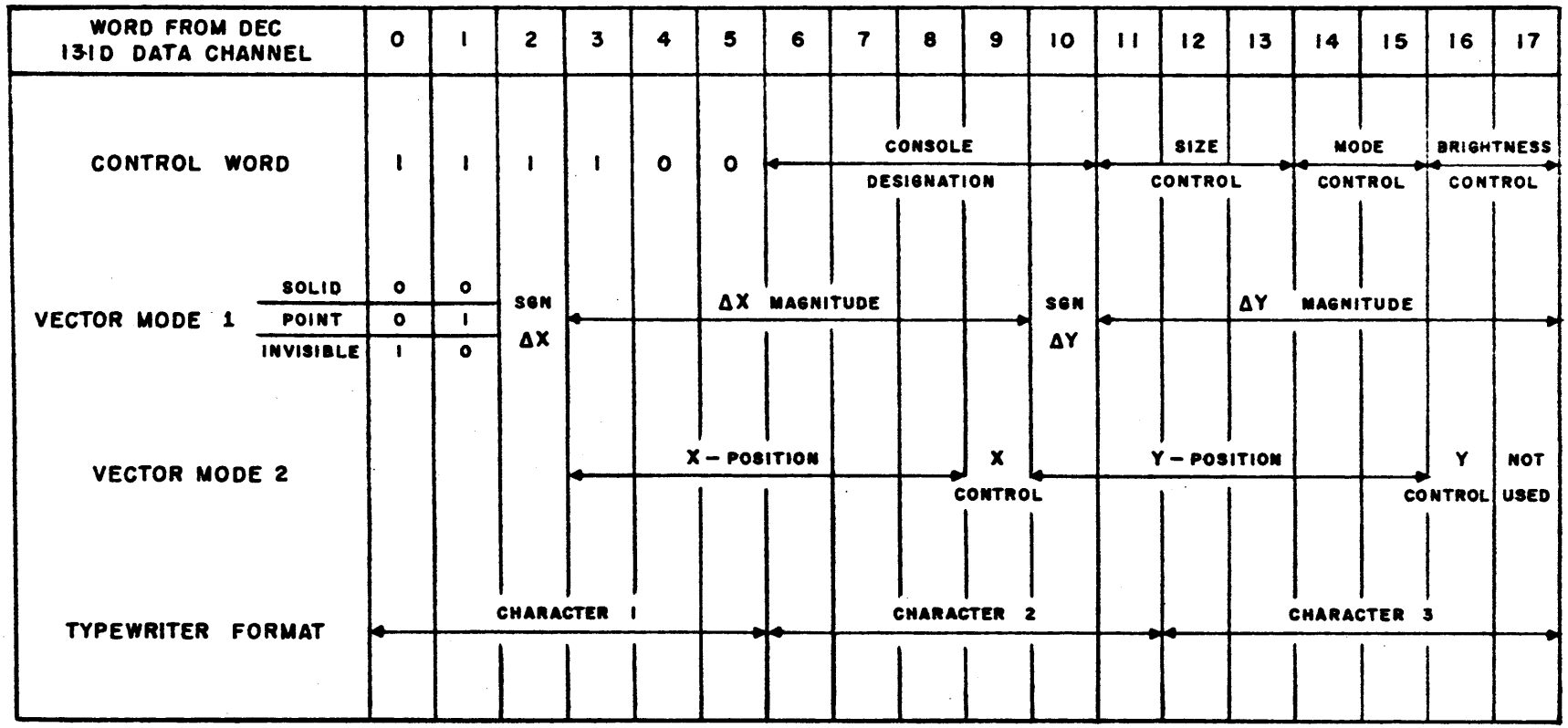


Figure 5-1. READ Display Codes

5.2.2.2 Vector Mode 2

The Vector Mode 2 format word is interpreted as one's complement and is operated as follows:

5.2.2.2.1 Control (Data Channel Word 0-2) - Control should be set to octal 6 in order that Vector Mode 2 words may be interpreted.

5.2.2.2.2 X Position (Data Channel Word 3-8) - Sets the six high order bits of the X major positioning subject to the setting of X control.

5.2.2.2.3 X Control (Data Channel Word 9) - If data channel word 9 is equal to one, the ten bits of the X major positioning are cleared and the data contained in X position are set in the six high order bits.

5.2.2.2.4 Y Position (Data Channel Word 10-15) - Sets the six high order bits of the Y major positioning subject to the setting of Y control.

5.2.2.2.5 Y Control (Data Channel Word 16) - If data channel word 16 is equal to one, the ten bits of the Y major positioning are cleared and the data contained in Y position are set in the six high order bits.

5.2.3 Typewriter Format Words

The typewriter format word contains three 6-bit characters. The first character is in bit positions 0-5. The character codes are shown in Figure 5-1. (Note: These codes are identical to the keyboard generated data codes.)

Included in the character code set are the following command codes.

a. Carriage Return

b. Space

c. No-op

d. Upper Case

e. Lower Case

The codes TAB (71) and CALL (74) are treated as spaced, provided CALL does not appear in the first character position mentioned above. The time required to operate on these codes is approximately 8 microseconds.

The carriage return command causes the X positioning of the CRT to be set to the left of the display and the Y positioning to be advanced down by the space of one printing line (the actual distance is a function of the current character size setting). The time required to effect a carriage return is approximately 18 microseconds. (Note: Automatic carriage return is not implemented in this system.) The space command causes a horizontal spacing to be left at one character location. The distance of the horizontal spacing is a function of the current character size setting. The time required for space and TAB (71) commands is approximately 1.6 microseconds.

The character/line and lines/frame attainable with the seven size codes are as follows:

Size Code	Characters/Line	Lines/Frame
octal		
1	127	63
2	85	31
3	63	31
4	42	15
5	31	15
6	21	7
7	15	7

The control code No-op (77) causes no operation to be performed. The case codes (upper and lower) cause a shift to the case indicated. The case selected will remain in effect until changed by the program. The time required to operate on these codes is approximately 1.6 microseconds.

5.2.4 Display Coordinates

The display coordinates are specified by 10-bit positioning registers for both X and Y axis. With respect to the center of the screen, plus one unit is binary 00 00 00 00 01 and minus one unit is binary 11 11 11 11 10 such that the following positions given in P (X, Y) binary define these specific points:

Center of screen	(00 00 00 00 00, 00 00 00 00 00)
Upper left corner	(10 00 00 00 00, 01 11 11 11 11)
Upper right corner	(01 11 11 11 11, 01 11 11 11 11)
Lower left corner	(10 00 00 00 00, 10 00 00 00 00)
Lower right corner	(01 11 11 11 11, 10 00 00 00 00)

5.2.5 Light Pen Interrupt and Status

The light pen information furnished to the PDP-1 consists of 2 status bits (LPS_1 and LPS_2) and a program interrupt.

When a light pen has detected light from an intensified console, the light pen interrupt (LPI) is generated and LPS_1 (status bit 15) set to one. With LPS_1 set to one no further interrupts can occur unless the bit is cleared by the program. The elapsed time from detection of light to program interrupt varies from 2 to 5 microseconds within the READ equipment and from 20 to 40 microseconds within the PDP-1.

The setting of LPS_2 (status bit 14) to one occurs during control word operations provided any intensified console has the light pen switch in the ON position.

The clearing of LPS_1 and LPS_2 is program controlled except for initial clearing when power is applied. The control word having octal code 00 as the console designation code causes LPS 1 and 2 to be cleared.

5.2.6 Display Refresh Rate

The READ equipment brightness levels are preadjusted to give a flicker-free display (under controlled ambient lighting conditions) at a display refresh rate of 30 cps. Inasmuch as the refresh rate is program controlled, it is cautioned that the refresh rate must not exceed 60 cps since the increase in brightness level may cause damage to the CRT. Conversely, a decrease in refresh rate from 30 cps will cause flicker and dimming in the display.

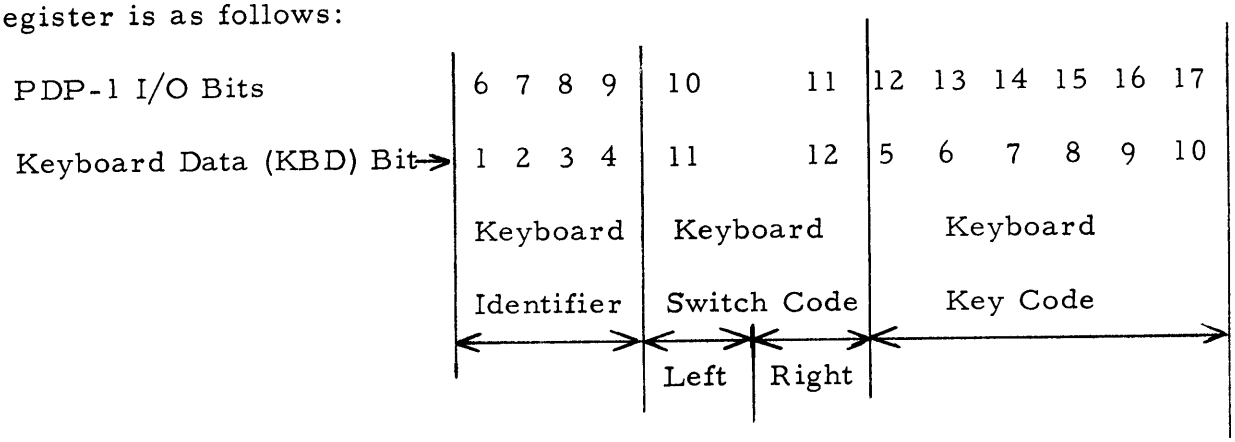
The following operation times for the READ equipment are summarized in order that the program may provide the required 30-cps refresh rate:

Display Data Mode	Operation Time
Control word	1.6 microseconds
Vector Type 1 word	5-15 microseconds (dependent on vector length)
Vector Type 2 word	18 microseconds
Typewriter format words	
Character drawing	5.65 microseconds (average)
Spacing (octal code 00)	1.6 microseconds
No-op, upper case, lower case	1.6 microseconds (each)
Tab, Call	8 microseconds (each)
Carriage Return	18 microseconds

5.3 KEYBOARD MULTIPLEXER CONTROL AND DATA FORMAT

5.3.1 Keyboard Data Format

The keyboard generated data and identifier are furnished to the PDP-1 I/O register. The format of the keyboard information and the PDP-1 I/O register is as follows:



5.3.1.1 Keyboard Identifier

The keyboard identifier is a 4-bit code designating the keyboard from which the data was obtained. The binary codes 0001 through 1111 identify the respective keyboard.

5.3.1.2 Keyboard Key Codes

The keyboard key codes listed in Table 5-1 are shown in octal. For example, binary code $(111000)_2$ appearing in the positions shown is octal 70.

5.3.1.3 Keyboard Switch Codes

Associated with each keyboard are two switch closures. The switch closure to the left of the SPACE bar sets KBD_{11} to one. The switch closure to the right of the SPACE bar sets KBD_{12} to one. These switches must be closed before depressing a key and remain closed until the keyboard is unlocked in order to transfer switch data to the PDP-1.

5.3.2 Keyboard Control

When READ has detected that keyboard generated data is to be furnished to the PDP-1, the keyboard program interrupt KBI is generated.

Depressing a key on any keyboard locks that keyboard until the data transferred to the PDP-1 is acknowledged via the read display keyboard instruction.

5.4 PROGRAMMING EXAMPLES

5.4.1 Programming the DEC 131M Data Channel

The DEC 131M data channel has only three central processor instructions associated with it. They are:

a. swm + 5000 (725546) - Sets word count in 131M data channel, resets the data channel and transfers bits 6-17 of the I/O register to the word counter of the data channel. Selects the Philco display. Word count must be one greater than the actual number of words desired to be transferred.

b. sim (720346) - Sets initial address in 131 data channel transfers bits 2-17 of the I/O register to the 131M location counter, where they are used as the extended address of the block to be transferred. The instruction also causes the channel to start transferring data.

c. rlm (720036) - Reads location counter of 131M. This transfers the channel idle bit to bit 0 of the I/O register and the channel location counter to bits 2-17.

WARNING: Attempts to transfer data from core addresses greater than 37777 octal through the 131M fail.

The example program to transfer 1000_8 words starting at location 34000_8 to the Philco display follows:

```
lio wc              /word count +1 to I/O register
swm + 5000          /set word count and select Philco
lio loc             /starting location
sim                 /set initial location and go
lp, rlm             /read and locate
spi i               /test if idle bit 1
jmp lp              /no, busy. Wait for idle.
hlt                 /yes, done
loc, 34000          /initial location - extended
wc, 1001            /word count desired plus 1
```

5.4.2 Programming the Keyboards

A simple program to service the keyboards follows. This program uses the fact that rkb instructions will completely clear the I/O register.

```
1,  rkb                 /transfer keyboard data to I/O register
    sni                 /skip if I/O not equal 0
    jmp 1               /I/O zero, no key struck
    ril 6s              /pull off zero bits
    cla                 /clear ac
    scl 4s              /console designator to ac
    dac con             /save console designator
    cla                 /peel off special buttons
    rcl 2s
    dac but             /save special buttons
    cla                 /peel off character
    rcl 6s
    dac char            /character typed
    hlt
```

A sequence break program to read the keyboards is:

```
        471/  jmp   kbs
100/    kbs,        rkb       /read keyboard
        di,         dio .     /save data
                    idx di    /put next word in next
                    lio 46    /restore I/O
                    lac 44    /restore ac
                    jmp i 45  /debreak
```

```
start,  lsm             /leave sequence break mode
        cac             /clear out sequence break system
        cbs             /clear out sequence break system
        asc   1100      /turn on keyboard sequence
        law   bal       /initialize break program dio instruction
        dap   di
        esm             /enter sequence break mode
        jmp   .         /wait .
bal,    0 .             /data area.
```

TABLE 5-1

READ CHARACTER AND KEYBOARD CODES

Octal Code	Character	Octal Code	Character
00	Space	23	B/b
01	≡/>	24	C/c
02	⊆/]	25	D/d
03	⊃//	26	E/e
04	↔/ ≥	27	F/f
05	< / [:	30	G/g
06	} / :	31	H/h
07	↑ / ÷	32	I/i
10	α / 0	33	J/j
11	δ / 1	34	K/k
12	∈ / 2	35	L/l
13	Π / 3	36	M/m
14	λ / 4	37	N/n
15	$ / 5	40	O/o
16	* / 6	41	P/p
17	' / 7	42	Q/q
20	" / 8	43	R/r
21	' / 9	44	S/s
22	A/a	45	T/t

TABLE 5-1 (Continued)

Octal Code	Character	Octal Code	Character
46	U/u	63	V/$\leq$
47	V/v	64	U/$\leftarrow$
50	W/w	65	| /+
51	X/x	66	$\wedge$/<
52	Y/y	67	? / ,
53	Z/z	70	Upper Case
54	$\rightarrow$/$\neq$	71	Tab
55	$\cap$ /)	72	Lower Case
56	{ / ;	73	Carriage Return
57	$\forall$ / x	74	Call
60	$\neg$/ =	75	&/ ·
61	~ / (	76	δ / !
62	$\exists$ / -	77	No-op

Note: Characters shown above as upper case/lower case.

SECTION 6

FUNCTIONS OF CONTROLS

6.1 CHARACTER SIZE

Front panel potentiometers R-103 and R-104, labeled X and Y CHARACTER SIZE, respectively, provide continuously variable adjustment of X and Y character size over a range of approximately 0 to approximately 0.6 inch. Maximum character size is obtained when the controls are turned fully clockwise. Adjustment of the controls will vary the size of all seven programmable character sizes in the same proportion.

6.2 DISPLAY SIZE

Front panel potentiometers R-101 and R-102, labeled X and Y DISPLAY SIZE, provide continuously variable adjustment of X and Y display size over a range of approximately ± 12 percent. The display size is increased when the controls are turned in a clockwise direction. Adjustment of the display size controls will expand or contract both the character spacing and vector size in the proper proportion. When expanding the display size, it may be necessary to readjust the display center controls in order to position the CRT presentation within the 9-inch by 9-inch viewing area.

6.3 DISPLAY CENTER

Front panel potentiometers R-105 and R-106, labeled X and Y DISPLAY CENTER, provide continuously variable adjustment of X and Y display position over a range greater than ± 1.0 inch. Adjustment of the display center within ± 1.0 inch will cause no change in the linearity of the CRT presentation.

6.4 INTENSITY

Potentiometer R-107 provides continuously variable adjustment of the CRT presentation's overall intensity over the range of zero to where the maximum permissible intensity is obtained when the control is turned fully clockwise and is set internally by the Z-axis amplifier cathode drive. Adjustment of the intensity control potentiometer varies the grid voltage between +10 and +30 volts which is effectively a change in the grid cathode bias and beam current of the CRT.

6.5 FOCUS

The focus potentiometer R-108 adjusts the focus of the CRT spot by changing the dc voltage at the focus electrode of the CRT. The dc focus electrode voltage is 4,000 volts; however, by the use of a divider network and voltage regulator, the maximum voltage on R-108 is 200 volts.

6.6 ON-OFF SWITCH

The ON-OFF switch controls the primary ac power to the remote console. However, before the CRT high voltage can go on, all low voltage power supplies in both the controller and remote console power supply must be "up." All voltages "up" in the controller is indicated by the Logic ON indicator, L-101. All low voltages "up" in the remote console power supply are indicated by the Display ON indicator, L-102.

SECTION 7

OPERATING INSTRUCTIONS

7.1 FIRST TIME OPERATION

When turning on the Remote Console for the first time, proceed as follows:

7.1.1 Visual Inspection

Perform a visual inspection to see that all connectors, fuses, and wires are securely in place.

7.1.2 Front Panel Control Settings

Turn the ON/OFF switch OFF. Connect the power cord to a source of 117 volts ac, 60 cycle power. Set the front panel controls as follows:

Intensity	Full counterclockwise (CCW)
Focus	Center
Display Size X and Y	Center
Character Size X and Y	Full clockwise (CW)
Display Center X and Y	Center
Power ON/OFF	OFF

7.1.3 Internal Control Settings

Turn the second grid (G2) potentiometer R-207 full CW and remove fuse F-102 from the Power Sequence chassis to prevent the high voltage from coming on.

7.1.4 Display Controller

The Display Controller must be ON and all power supplies must be "up" before attempting to align the Remote Display. All voltages "up" in the

Display Controller are indicated by the presence of -30 volts at the display which lights L-101 "Logic ON" through relay K-102.

The PDP-1 computer must be programmed to provide a control word to specify:

a. Console to be intensified

b. Largest character size

c. Brightest character level

d. Typewriter mode

The character "M" is displayed in a 31 x 8 character array at a 30-cycle-per-second refresh rate.

Prior to display turn-on and alignment, the following signals should be present at the display logic:

Signal	Approximate Amplitude	Location
X major position	0 to -8 volts	NA 22-7
Y major position	0 to -8 volts	NA 22-X10
X character	0 to -3 volts	NA 21-3
Y character	0 to -3 volts	NA 21-X3
Z-axis unblanking	0 to -4 volts	NA 31-X14

The amplitude of the Z-axis unblanking signal is dependent on the setting of potentiometer R4 of D-18. R4 should be adjusted until the Z-axis unblanking signal at NA 31-X14 is approximately -4 volts in amplitude.

7.1.5 Display Alignment

With the power switch ON, the following adjustments are performed:

7.1.5.1 Z-Axis Amplifier (D-18)

R6 of the D-18 printed circuit board is adjusted for maximum unblank signal as measured at R16 of D-18. The base line of the signal should be just less than +100 volts while the unblank pulse should go from approximately +100 volts to less than +30 volts.

7.1.5.2 Character Amplifier (D-19X and D-19Y)

R4 on each of the D-19 printed circuit boards is adjusted to obtain maximum character deflection signal as measured at R2 of D-19. The base line of the character deflection signal is between -30 and -40 volts while the signal goes positive to approximately -5 volts. The maximum amplitude signal should be adjusted such that there is no clipping or rounding of the signal due to overdriving of the amplifier.

7.1.5.3 Major Position Amplifier (D-20X and D-20Y)

Major position deflection signals are observed with an oscilloscope connected across the output resistor of the amplifier (two 2-ohm resistors in parallel) where 1 volt equals 1 ampere deflection current. The display center controls should move the center of the observed waveform approximately ± 1 ampere. The display size control should contract the deflection signal to approximately ± 2 amperes and expand the deflection to ± 5 amperes. It is important that the deflection current signal go both plus and minus about ground. Failure to do so indicates faulty operation in either the major position deflection amplifier or the D-13 printed circuit board.

7.1.6 CRT Display Alignment

With the power ON/OFF switch OFF, replace fuse F-102 in the power sequence chassis and connect the high voltage lead to the CRT anode cap.

WARNING - OBSERVE SHOCK HAZARD

Particular care should be exercised in avoiding contact with the 16-kv power supply, CRT anode cap, and focus voltage power supply as personnel contact may be lethal.

7.1.6.1 Second Grid (G2) Voltage Adjustment

Turn Power ON/OFF switch to ON. If spot appears on CRT face, turn OFF power immediately and recheck all voltages, signals, and control settings. Should no spot or display appear on the CRT face, adjust intensity

control potentiometer CW while observing CRT face. If a display should appear, adjust potentiometer R4 of D-18 until trace disappears. The intensity control should be turned fully CW with no visual CRT presentation. Adjust G2 control, potentiometer R204, CCW until desired display intensity is reached. The G2 setting will determine the maximum display intensity permissible.

CAUTION IN USE OF INTENSITY CONTROL

There is a possibility of burning the phosphor screen if too high an intensity is used, particularly when the display is operated at high refresh rates, or when the display is stationary due to loss of deflection. Care should therefore be exercised in maintaining the intensity control setting consistent with adequate brightness.

7.1.6.2 CRT Focus Alignment

The focus control on the front panel should be varied to determine that the CRT display goes through focus. If the display tries to focus with the focus control fully CW, the focus voltage must be reduced or the anode voltage increased to reduce the focus voltage, short out the two 1-megohm resistors on the focus power supply chassis and/or increase the high voltage by adjusting the input taps on the high voltage power pack.

Power Pack Input Taps	Relative High Voltage Output
2-3	Highest Output
1-3	
2-4	
1-4	
2-5	
1-5	
2-6	
1-6	Lowest Output

7.2 PRECAUTIONS

The following precautions should be observed in particular to realize proper operation and to avoid damaging the equipment:

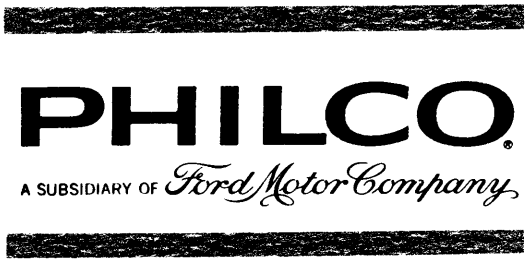
7.2.1 External Magnetic Fields

The CRT display is sensitive to stray magnetic fields; therefore the equipment should not be placed in the vicinity of ac motors, or "SOLA" type line voltage regulators.

Stray magnetic fields will cause the CRT line width to increase and give the appearance of 60-cycle modulation of the trace.

7.2.2 Intensity Control

Care must be exercised in the use of the console intensity control to prevent burning of the CRT phosphor screen. Before turn-on and turn-off, it is desirable that the intensity control be turned fully CCW. Also, should a power failure occur in either the console or the controller, the console power switch should be turned to OFF. To prevent damage to the equipment, the remote console should not be turned ON for any extended period while controller is turned OFF.


PHILCO
A SUBSIDIARY OF Ford Motor Company