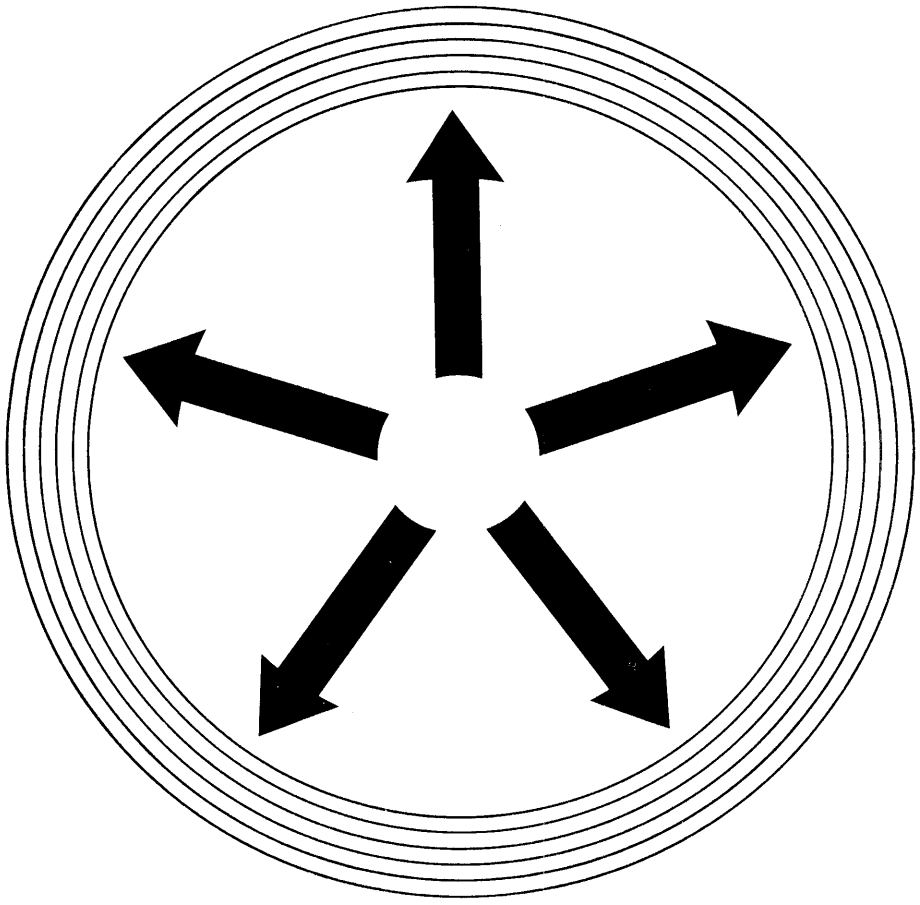
PERIPHERAL EQUIPMENT CORPORATION



PEC

INCREMENTAL WRITE
TAPE TRANSPORT

PEC

PERIPHERAL EQUIPMENT CORPORATION
9551 Irondale Avenue, Chatsworth, Calif. 91311
Telephone (213) 882-0030 TWX: (910) 494-2093

OPERATING AND SERVICE MANUAL

MANUAL NO. 100392

EQUIPMENT SERIAL NO.

MODEL 1207

INCREMENTAL WRITE

TAPE TRANSPORT

SERVICE AND WARRANTY

This tape unit has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected from manufacturers "off the shelf" stock. Should a component fail, it may be readily replaced from PEC or your local supplier. The tape unit has been designed for "plug-in" replacement of circuit boards or major components which will insure a minimum of equipment down time.

Please read the instruction manual thoroughly as to operation, maintenance, and component reference list. Should you require additional assistance in servicing this equipment, please contact your local representative or the following regional Service Center. A trained service representative will be pleased to assist you.

PERIPHERAL EQUIPMENT CORPORATION
9551 Irondale Avenue
Chatsworth, California 91311
Telephone (213) 882-0030

PEC warrants its equipment and materials to be free from defects in material and workmanship under normal use and service for a period of 12 months from the original date of shipment. The company's obligation being limited to repairing or replacing any defective part of such product.

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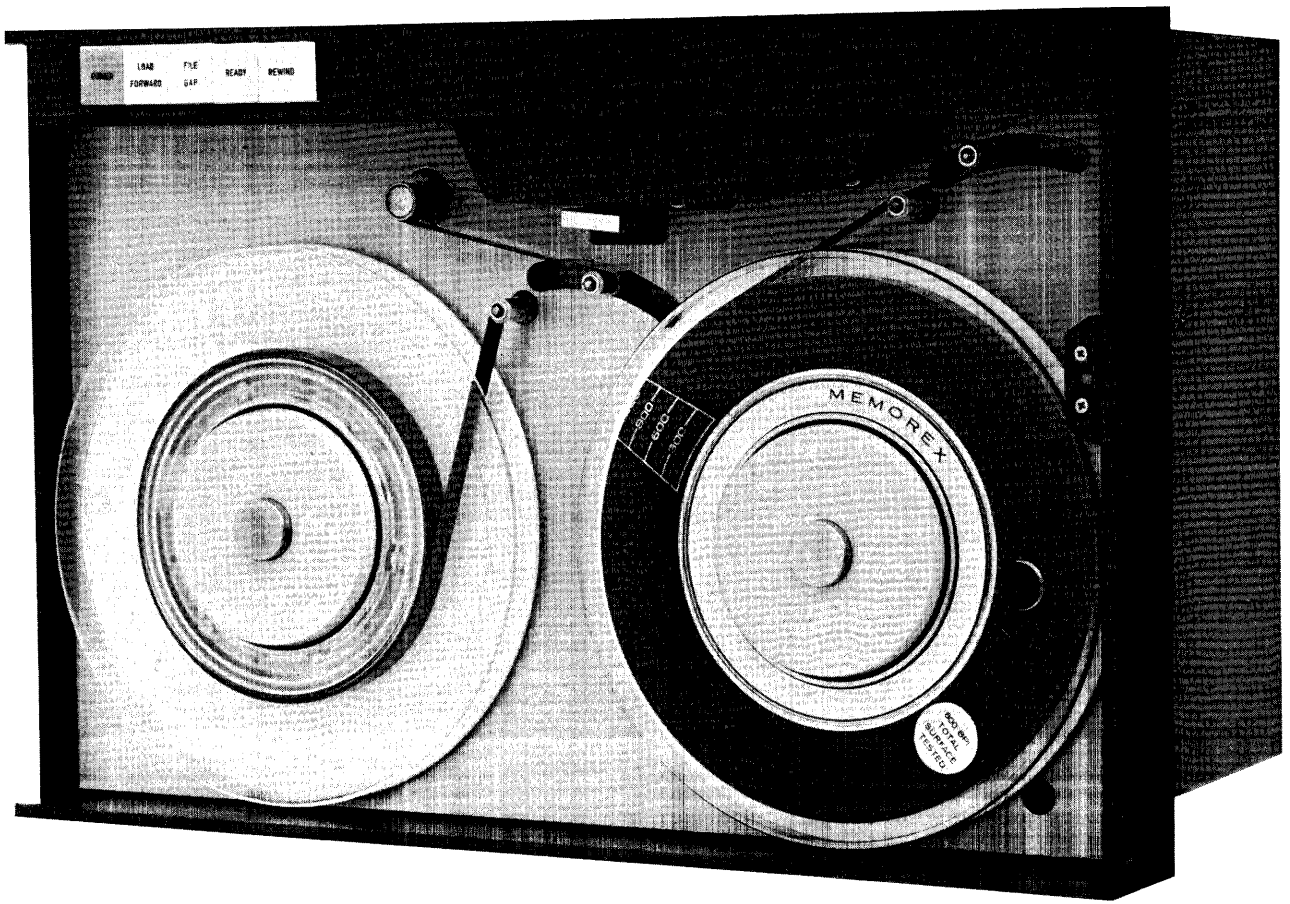

FIGURE 1-1A. TAPE TRANSPORT (8-1/2 INCH REEL)

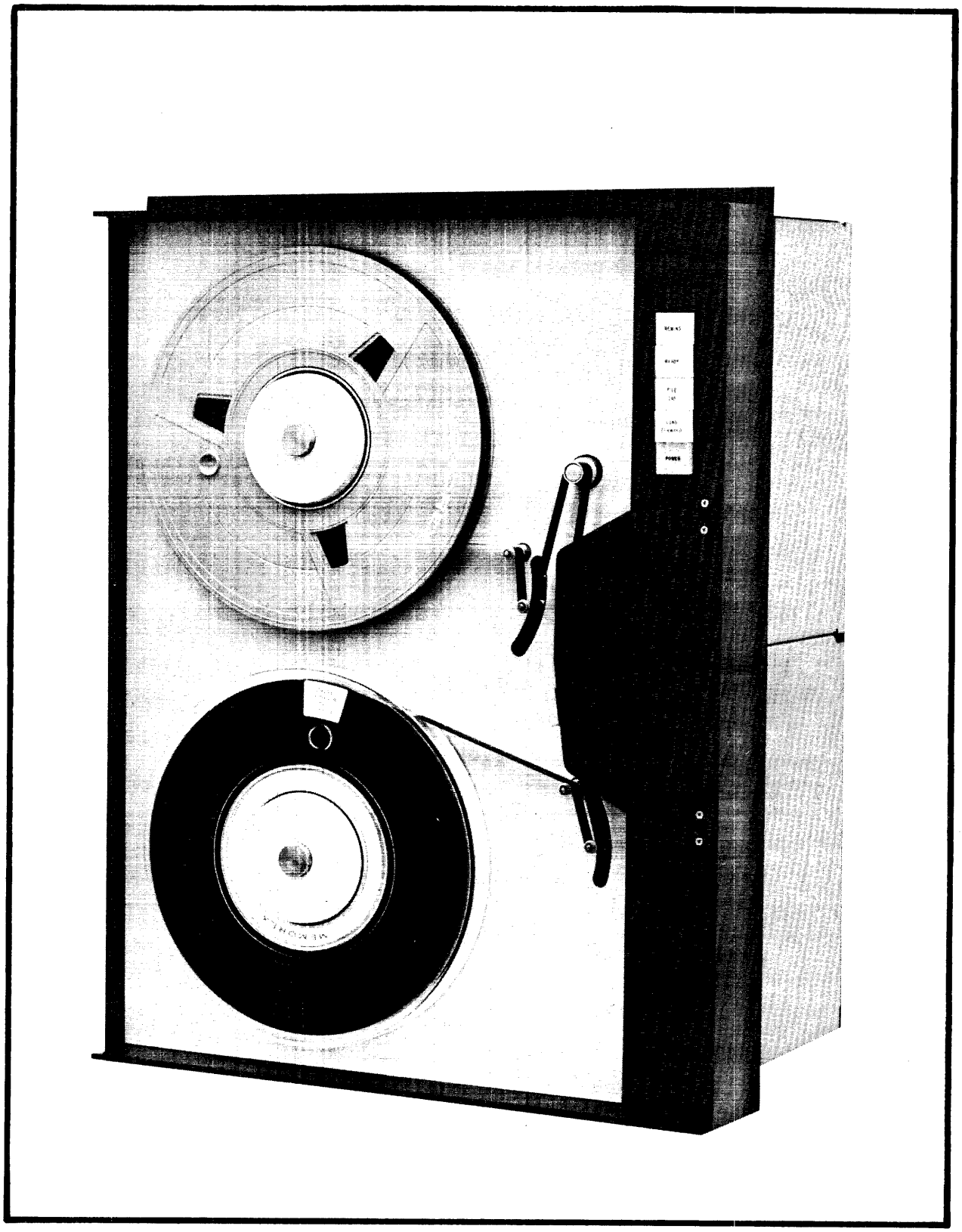

FIGURE 1-1B. TAPE TRANSPORT (10-1/2 INCH REEL)

SECTION I - DESCRIPTION AND SPECIFICATIONS

1.1 Scope of Manual. This manual provides specifications, operating and service instructions for incremental Tape Transports manufactured by PERIPHERAL EQUIPMENT CORPORATION.

1.2 Function of Equipment. The incremental tape transports have the capability of recording digital data on magnetic tape in IBM format. The magnetic tape should be computer grade 0.5 inches wide, 1.5 mil. thick. The data source may have a variable or fixed data rate of 0-350 sps, 0-500 sps, or 0-700 sps (steps per second) depending upon the tape transport model.

The transport operates directly from 117 volts AC single phase 50 to 60 Hz power.

1.3 Description of Equipment. All electrical and mechanical components have been selected to insure reliable operation in laboratory conditions.

The transport utilizes a single capstan drive for controlling tape motion during the normal recording mode and during rewind. This gives several important operating advantages. It minimizes the number of mechanical components required to handle magnetic tape and completely eliminates such troublesome components as pinch rollers - a major skew-producing component.

Tape is always under a constant tension of 8 ounces thus eliminating the possibility of tape cinch when the tape reel is placed on a computer

transport.

The capstan is controlled by a velocity servo utilizing position information as shown in the Block diagram of Figure 1-2.

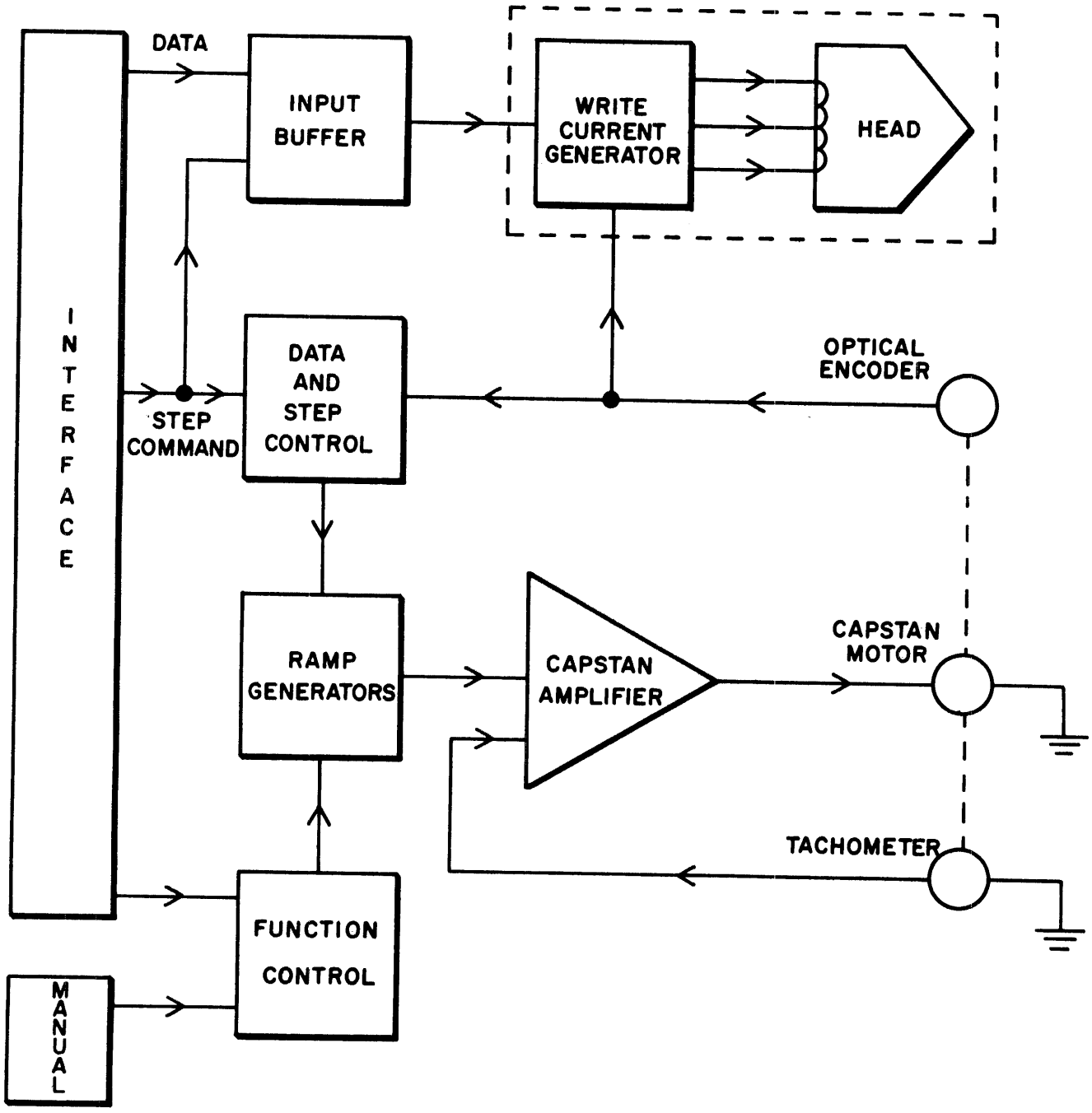

FIGURE 1-2. BLOCK DIAGRAM

The position information is derived from a highly reliable optical shaft encoder coupled directly to the capstan motor shaft and is used to accurately place the data on the tape. It also gives a stop command to the capstan drive system if no additional data is to be written on the tape.

The velocity information is generated using a DC tachometer which is directly coupled to the capstan motor shaft and produces a voltage which is directly proportional to the rotational velocity of the capstan. This voltage is compared to a reference voltage from the ramp generators using operational amplifier techniques and the difference is used to control the capstan motor. This capstan control technique gives precise control of tape accelerations and tape velocities, thus minimizing tape tension transients, and completely eliminating the requirement for a gear box in the drive system. This technique allows a great deal of flexibility including the generation of inter-record gaps at high speed (60 msec. IRG time).

As each data character is received, it is held in a buffer register while the tape is being brought up to speed and moved the required distance. When the proper tape displacement has been achieved, this being determined by the optical shaft encoder, the data held in the buffer is recorded on the tape. The tape is brought to a controlled stop awaiting the next WRITE STEP command. If another WRITE STEP command with its associated data is received before the tape has come to a stop, the tape will be brought back up to speed and remain on speed until the proper displacement has been made.

In essence, the transport is commanded to move tape at a speed determined by the capstan velocity servo whenever data is in the buffer register.

Transports having higher stepping rate capability use additional buffering and more than one tape velocity.

Along with the capstan control system, the transport consists of the mechanical tape storage system, supply and take-up reel servo system, record head and its associated electronics and the control logic.

The mechanical storage system buffers the relatively fast starts and stops of the capstan from the high inertia of the supply and take-up reels. As tape is taken from or put into the storage system, a long-life potentiometer measures the displacement of the storage arm and feeds an error signal to the reel motor amplifier. This signal is amplified and used to control the reel motor such that the reel will either supply or take-up tape to maintain the storage arm in its nominal operating position. The storage arm system is designed to give a constant tape tension as long as the arm is within its operating region.

This tape path design minimizes tape wear as there is only relative motion of the tape oxide at the record head and the head guides. All other guides in the tape path rotate during tape motion.

The record head writes the flux transitions on the tape under control of the data electronics. The point at which the data is written is determined by the shaft encoder.

The control logic operates on manual or remote commands and controls

tape motion for writing IBM compatible tapes.

Manual controls necessary for loading tape, bringing tape to BOT tab, bringing the transport to the READY state, rewinding tape, and unloading tape are located on the transport. All of these controls are accessible with the dust cover door closed as these transports are designed and intended to operate with the dust cover door closed.

CAUTION

AFTER TAPE HAS BEEN LOADED ON THE TRANSPORT, THE DUST COVER DOOR SHOULD REMAIN CLOSED DURING RECORDING AND UNTIL THE TAPE HAS BEEN REWOUND TO THE 'BEGINNING OF TAPE' TAB. THIS WILL MINIMIZE THE POSSIBILITY OF TAPE CONTAMINATION AND LOSS OF DATA RELIABILITY.

All manual controls except POWER may be locked out remotely. These controls may also be supplied remotely. WRITE STEP and IRG commands must be supplied remotely.

The transport is supplied with a photoelectric sensor for detection of the BOT tab and EOT (end of tape) tab. BOT commands are used internally in the transport for control, and both the BOT and the EOT are sent as levels to the customer.

Section II, Figures 2-1 and 2-2, show a complete list of all interface-lines.

These incremental transports are interlocked to protect against tape damage due to component failure and inadvertent power failure.

Tape may be easily loaded on the transport by loading the take-up

reel and supply reel as outlined in Paragraph 3.2.1.1. This will place the oxide in contact with the head. The transport is provided with quick-release reel retainers for both the supply reel and take-up reel. This makes possible rapid changing of reels on the transport. The Incremental Tape Transports are designed to mount in a standard 19-inch retma rack.

The 1000 series occupies a 12 1/4 inch panel space and the 2000 series a 24 1/2 inch panel space. See Section II for mounting instructions. Complete specifications are provided in Table 1-1.

Table 1-1. MODEL SPECIFICATIONS

Model 1000 Series	Model 2000 Series	Bit Packing Density	Characters Per Second	Number Channels
1807-9	2807-9	800	0-700	9
1805-9	2805-9	800	0-500	9
1803-9	2803-9	800	0-350	9
1807-7	2807-7	800	0-700	7
1805-7	2805-7	800	0-500	7
1803-7	2803-7	800	0-350	7
1507	2507	556	0-700	7
1505	2505	556	0-500	7
1503	2503	556	0-350	7
1207	2207	200	0-700	7
1205	2205	200	0-500	7
1203	2203	200	0-350	7

1.4 General Specifications

	1000 Series	2000 Series
Tape (computer grade)		
Width	0.5 inches	0.5 inches
Thickness	1.5 mil.	1.5 mil.
Tape Tension	8 ounces	8 ounces
Reel Size Diameter	8.5 inches	10.5 inches
Interchannel Displacement Error		
Dynamic	±200 uinches	±200 uinches
Static	±100 uinches	±100 uinches
REWIND Speed	75 ips	75 ips
800 bpi	50 ips	50 ips
Weight	60 pounds	85 pounds
Dimensions		
Height	12.25 inches	24.5 inches
Width	19.0 inches	19.0 inches
Depth (from mounting surface)	11.7 inches	11.7 inches
Depth (Total)	14.0 inches	15.0 inches
Recording Mode (IBM compatible)	NRZI	NRZI
INTER-RECORD GAP Time	60 msec.	60 msec.
FILE GAP Time (3.5 inches with file mark internally generated)	500 msec.	500 msec.
Bit Spacing Accuracy		
Worse case	±4%	±4%
Typically	±2%	±2%
Operating Temperature	35°F to 122°F	35°F to 122°F
Altitude	0-20,000 feet	0-20,000 feet
Power	117 vac 120 watts 48-400 Hz	117 vac 120 watts 48-400 Hz

Mounting	Standard retma rack mount	
Electronics	All silicon Logic DTL	All silicon Logic DTL

1.5 Interface and Controls

1.5.1 Manual Controls (located on tape transport)

POWER ON-OFF	Alternate action
LOAD FORWARD	Momentary
REWIND	Momentary
FILE GAP	Momentary
READY	Momentary

All these are push-button controls which illuminate when function requested is being performed.

1.5.2 Interface Inputs

WRITE STEP	Pulse
INTER-RECORD GAP	Pulse When an IRG command is given, it should occur at least 2 usec after the last WRITE STEP command.
READY	Pulse
FILE GAP	Pulse
LOAD FORWARD	Level
REWIND	Pulse
REMOTE RESET	Level for duration of reset
ECHO CHECK RESET	Level for duration of reset

6 Data Lines (7 channel system)	Level	True coincident with WRITE STEP command
8 Data Lines (9 channel system)	Level	True coincident with WRITE STEP command
DISABLE Manual Controls	Level	Disables manual controls while true
WRITE DATA PARITY (Only when internal parity generation not required)	Level	Levels must be true before or coincident with leading edge of WRITE STEP command. Minimum duration 20 usec.

1.5.3 Interface Outputs

EOT (End of Tape)	Level	(for duration of EOT tab)
BOT (Beginning of Tape)	Level	(for duration of BOT tab)
GAP IN PROCESS	Level	
TAPE NOT TENSIONED	Level	
TRANSPORT READY	Level	(transport can accept data)
BUFFER 1 BUSY	Level	(data still to be recorded is in the transport buffer)
ECHO CHECK PARITY ERROR (optional)	Level	
MOTION CHECK (optional)	Transition	Alternately true to false and false to true on consecutive encoder pulses

1.6 Interfaces Two standard interfaces are available with PERIPHERAL EQUIPMENT CORPORATION Incremental Transports.

1.6.1 Slow Interface The slow interface is designed so that all signal inputs can be included in one harness together with a single ground and all signal outputs can be included in a second harness together with a single

1-A

ground. The maximum transmission distance is 20 feet. The two harnesses can be run in close proximity. The effects of cross talk are eliminated by:

1. Providing input filters on the interface receivers.

2. Slowing the rise and fall times of the interface transmitters.

These measures result in a delay of approximately 6 usec in the transmission of signals in either direction.

Slow interface specifications are as follows:

1.6.1.1 Interface Receivers (Figure 1-3)

Levels	Positive Logic	False	0 to +0.5V
		True	+5V to +15V with 0 to 5K source impedance
	Negative Logic	False	0 to -0.5V
		True	-5V to -15V with 0 to 5K source impedance
Pulses	Positive or negative going with above levels; leading edge triggering		
	Maximum rise and fall times 5 usec 10% to 90%		
	Maximum width 20 usec		
	Maximum width 10 millisec EXCEPT WRITE STEP command which must have a duty ratio of less than 20%		

1.6.1.2 Interface Transmitters (Figure 1-4)

Levels	Positive Logic	False	0 +0.7V (can sink 5mA maximum from external source)
		True	+10V with 1K source impedance
	Negative Logic	False	0 -0.7V (can sink 5mA maximum from external source)
		True	-10V with 1K source impedance
	Rise and fall times up to 5 usec		

1-A

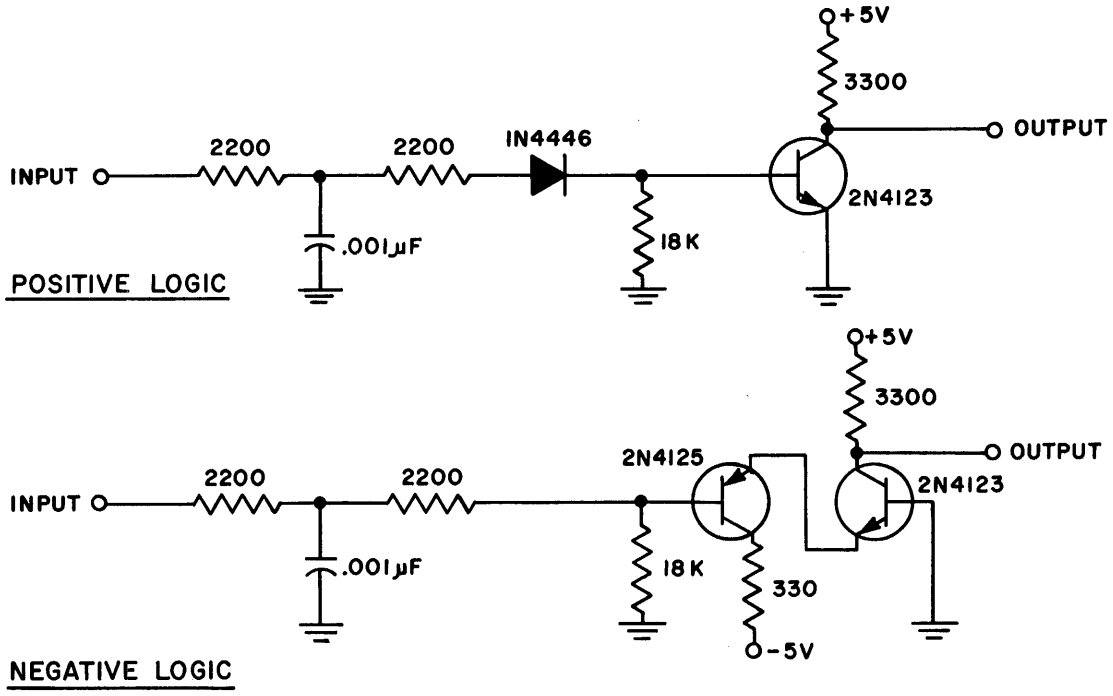

FIGURE 1-3. SLOW INTERFACE (RECEIVER)

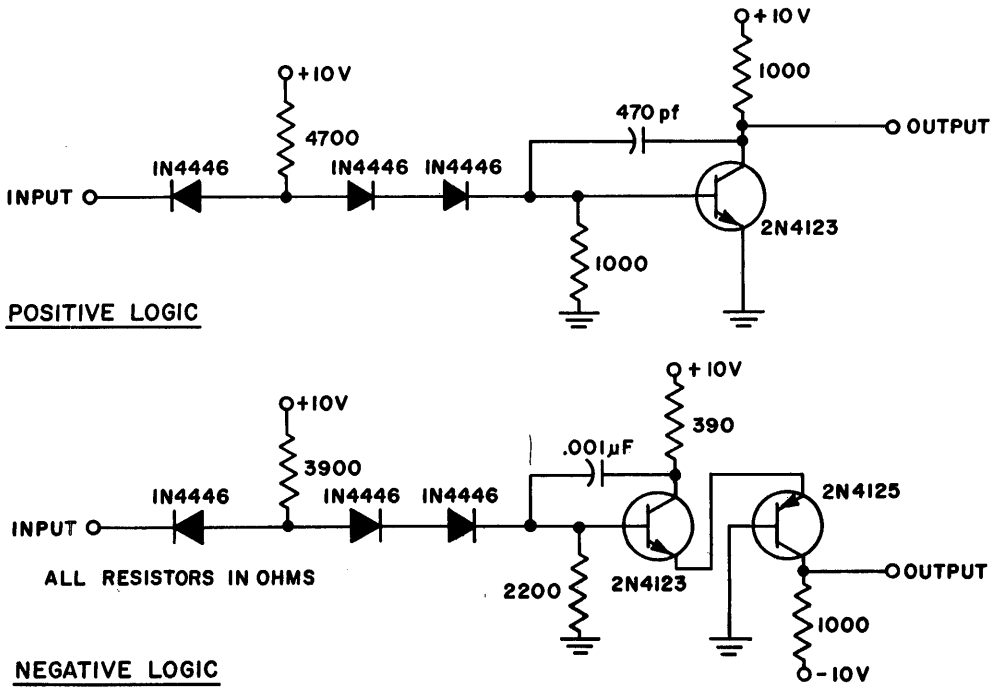

FIGURE 1-4. SLOW INTERFACE (TRANSMITTERS)

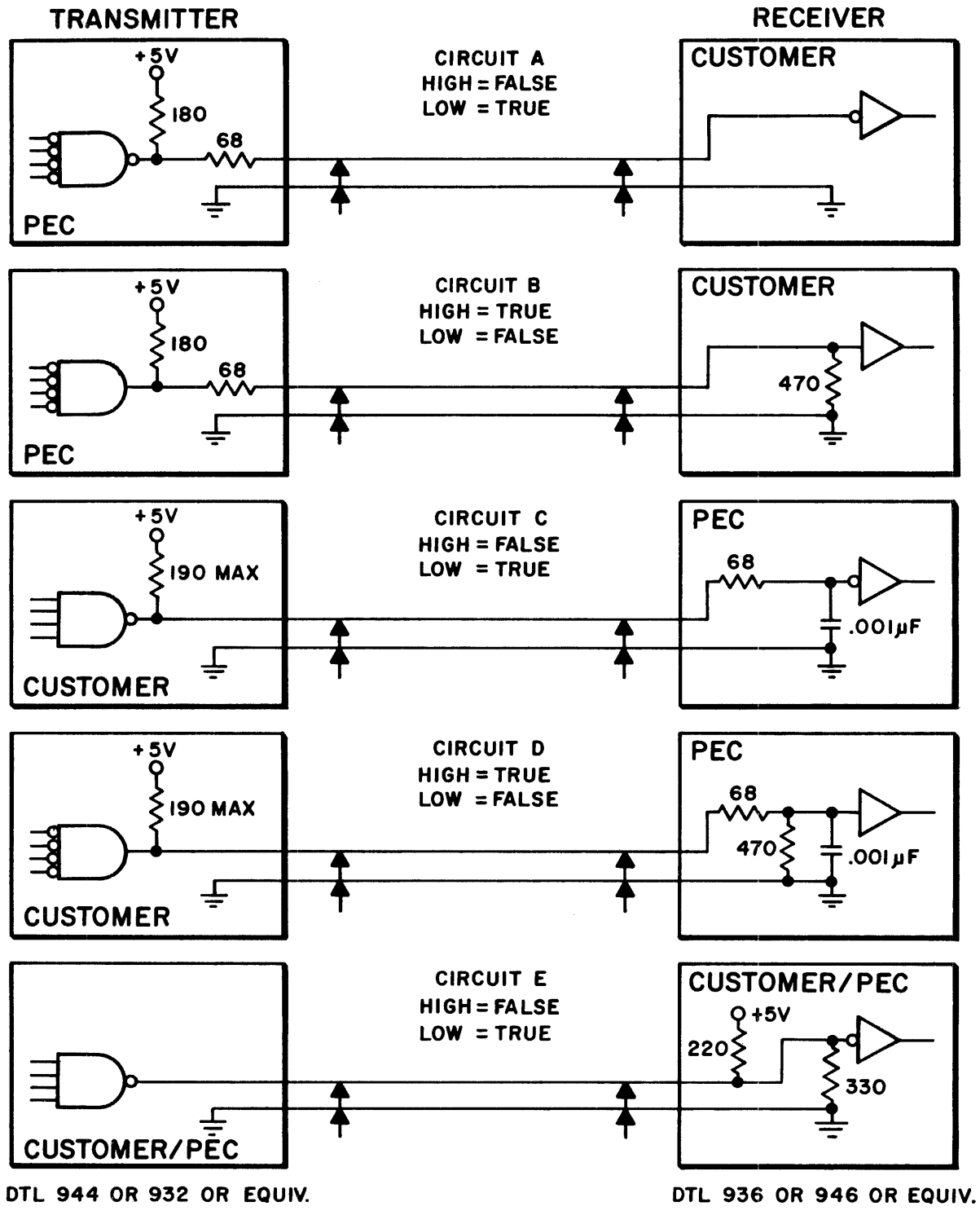

FIGURE 1-5. FAST INTERFACE

1.6.2 Fast (DTL) Interface The design of the fast interface is based on the limited temperature range (0 to 75°C) Series of DTL (Diode Transistor Logic) dual in line modules. DTL 944 or 932 power gates are used as transmitters and DTL 936 invertors or DTL 946 dual input gates are used as receivers. The system is also suitable for using equivalent TTL (Transistor Transistor Logic) modules.

The fast interface is designed so that all signal inputs can be included in one harness and all signal outputs can be included in a second harness. The maximum transmission distance is 20 feet. The two harnesses can be run in close proximity. The signals are transmitted via individual twisted pairs to reduce cross talk.

The high edge speeds involved result in considerable distortion of the signal and matching techniques must be employed to avoid spurious signals due to the distortion.

To give maximum flexibility, the interface transmitters and receivers used in PERIPHERAL EQUIPMENT CORPORATION transports incorporate the matching necessary to interface satisfactorily with unmatched transmitters and receivers in customers equipment.

The interface circuits are designed so that a disconnected wire results in a false signal being interpreted at the receiver end of the wire. This leads to two possible configurations both of which are available to the customer.

1. Interface wire high = true
   Interface wire low = false

2. Interface wire high = false
   Interface wire low = true

The customer must specify which alternative is required.

1.6.3 Interface Specifications

Levels — Consistent with circuit configurations shown in Figure 1-5. Noise margins are as shown on the following page.

Pulses — Leading edge triggering with above levels
Minimum pulse width 1 usec
Maximum width 10 millisecs except WRITE STEP command which must have a duty ratio of less than 20%.

Edge transmission delay not greater than 200 ns.

It is assumed that interconnection of PERIPHERAL EQUIPMENT CORPORATION and customer equipment uses a harness of individual twisted pairs each with the following characteristics:

1. Maximum length 20 feet.

2. Not less than 1 twist per inch.

3. 22 gauge or 24 gauge conductor with minimum insulation thickness of 0.01 inches.

It is important that the ground side of each twisted pair be grounded within a few inches of the interface card to which it is connected.

Figure 1-5 shows the configurations for which the PERIPHERAL EQUIPMENT CORPORATION transmitters and receivers have been designed. Noise margins will depend on the circuit configuration, ambient temperature and whether the interface line is in a high or low state.

In the high state, the relative movement of the transmitter +5 volt line and receiver ground is important. In the low state, transmitter ground to receiver ground relative movement is important.

Table 1-2 below shows worst case noise margins for the various configurations.

Table 1-2. NOISE MARGINS

Circuit State	0°C	25°C	50°C
A&C low	500 mv	400 mv	200 mv
A&C high	2.0 v	2.1 v	2.25 v
B&D low	650 mv	550 mv	350 mv
B&D high	600 mv	700 mv	850 mv
B&E low	550 mv	300 mv	200 mv
B&E high	300 mv	450 mv	550 mv

SECTION II - INSTALLATION AND CHECKOUT

2.1 Uncrating the Transport The transport is shipped in a protective container to minimize the possibility of damage during shipping.

Place the shipping container as indicated on the container.

Open the shipping container and remove the packing material so that the transport and its metal mounting frame can be lifted from the container.

Lift the transport out of the container by use of the metal shipping frame.

This metal shipping frame may be used to check out the transport if desired, however, it should be operated with the tape deck closed.

Check the contents of the shipping container against the packing slip and investigate for possible damage. If there is any damage, notify the carrier.

Open the tape deck and check that all cards are secured in their respective card slots. Also check for any visable mechanical damage.

CAUTION

THE TAPE DECK MAY BE OPENED BUT PRECAUTION SHOULD BE TAKEN TO PREVENT THE TRANSPORT FROM TIPPING FORWARD AND POSSIBLY SUSTAINING DAMAGE.

The tape deck is opened by releasing the screw which secures it to the sheet metal electronic chassis. This may be accomplished by using a large, flat-head screwdriver, turning the screw counterclockwise. This locking screw is located on the right-hand side of the transport near the

supply reel, under the dust cover door.

2.2 Electrical Connections

2.2.1 Power A power cord is supplied for plugging into a polarized 117 volt outlet. Power requirement is 125 watts.

2.2.2 Interface Controls Remote controls are made through the interface connector. Figures 2-1 and 2-2 show the pin number assignments for all interface lines respectively.

2.3 Checkout Procedure Section III contains a detailed description of all controls. To check the proper operation of the transport before placing it in the system, the following procedure should be followed:

1. Connect the power cord.
2. Place tape on the transport as described in Paragraph 3.2.1.1.
3. Turn transport power ON.
4. Depress the LOAD FWD control momentarily to apply capstan motor and reel motor power.
5. Depress the LOAD FWD control and hold it in until tape reaches BOT tab and stops. Then release LOAD FWD control. The READY indicator will be illuminated.
6. The transport is now ready to receive remote or local commands.
7. To check FILE GAP, depress FILE GAP control and check that the tape moves approximately 4.25 inches and stops.

TRANSPORT CONNECTOR	MS 3102A-28-15S
MATING CONNECTOR	MS 3106A-28-15P
CABLE CLAMP	AN3057-16

PIN	SIGNAL
A	INTER-RECORD GAP Command
B	FILE GAP Command
C	WRITE STEP Command
D	TRANSPORT READY
E	DISABLE MANUAL CONTROLS
F	
G	0 VOLTS LOGIC
H	WRITE DATA 0
J	WRITE DATA 1
K	WRITE DATA 2
L	WRITE DATA 3
M	WRITE DATA 4
N	WRITE DATA 5
P	
R	REMOTE RESET
S	WRITE DATA 6
T	WRITE DATA 7
U	MOTION CHECK
V	ECHO CHECK RESET
W	ECHO CHECK ERROR
X	BUFFER 1 BUSY
Y	END OF TAPE MARKER
Z	BEGINNING OF TAPE MARKER
a	TAPE NOT TENTIONED
b	READY Command
c	REWIND Command
d	WRITE DATA PARITY
e	GAP IN PROCESS
f	-10 VOLTS } For Monitoring Only
g	+10 VOLTS } Not For Customer Use
h	CHASSIS GROUND
j	
k	
l	
m	LOAD FORWARD Command
	INTERFACE INPUT
	INTERFACE OUTPUT

FIGURE 2-1. INCREMENTAL WRITE SLOW INTERFACE SIGNALS

TRANSPORT CONNECTOR	Winchester MRAC 104S-J6
MATING CONNECTOR	Winchester MRAC 104P-JTC6H

LIVE PIN	GROUND PIN		SIGNAL
A	E	→	LOAD FWD Command
K	P	→	READY Command
U	Y	→	REWIND Command
c	h	→	REMOTE RESET
m	r	→	DISABLE MANUAL CONTROLS
v	z	→	INTER-RECORD GAP Command
AD	AJ	→	FILE GAP Command
AN	AT	→	WRITE STEP Command
AX	BB	→	WRITE DATA 0
BF	BL	→	WRITE DATA 1
BR	BV	→	WRITE DATA 2
BZ	CD	→	WRITE DATA 3
CJ	CN	→	WRITE DATA 4
B	F	→	WRITE DATA 5
L	R	→	WRITE DATA 6
V	Z	→	WRITE DATA 7
d	i	→	WRITE DATA PARITY
n	s	→	ECHO CHECK RESET
D	J	←	END OF TAPE Marker
N	T	←	BEGINNING OF TAPE Marker
X	b	←	TAPE NOT TENTIONED
g	k	←	TRANSPORT READY
q	u	←	BUFFER 1 BUSY
y	AC	←	GAP IN PROCESS
AH	AM	←	ECHO CHECK PARITY ERROR
AR	AV	←	MOTION CHECK
CP		←	CHASSIS GROUND
CE		←	0 VOLTS LOGIC
CA		←	+5 VOLTS } For Monitoring Only
BW		←	-5 VOLTS } Not For Customer
CR		←	+10 VOLTS } Use
CL		←	-10 VOLTS }
		→	INTERFACE INPUT
		←	INTERFACE OUTPUT

FIGURE 2-2. INCREMENTAL WRITE DTL INTERFACE SIGNALS

8. REWIND can be checked by running additional tape on the take-up reel using the LOAD FWD control.

After several feet of tape have been run on the take-up reel, momentarily depress the REWIND control. The tape will rewind to BOT.

9. A WRITE STEP command applied to the correct pin of the remote connector will cause the transport to move the tape one bit space. The magnitude and polarity of the command depend upon the interface chosen by the customer.

10. An IRG command applied to the correct pin of the interface connector will cause the transport to execute an IBM compatible IRG. The magnitude and polarity of the command depend upon the interface chosen by the customer.

11. Assuming tape has been rewound to BOT, tape is removed by depressing the REWIND control and holding it down until all the tape has rewound onto the supply reel. The reel can then be removed as outlined in Paragraph 3.2.2.

2.4 Rack Mounting the 1000 Series Transport

CAUTION

WHEN REMOVING TRIM FROM THE DECK, CARE MUST BE TAKEN TO AVOID CONTACT BETWEEN THE HEAD AND GUIDES AND THE OVERLAY PLATE.

The physical dimensions of the transport are such that it may be mounted in a standard retma rack. A 12 1/4 inch panel space is required. It requires a depth behind the mounting surface of at least 12 inches.

The following procedure should be followed to rack mount the transport. Figure 2-3 shows the relevant mounting dimensions.

1. Place the transport in the normal operating position with the reels facing the operator.

2. Open the dust cover door and remove the capstan using the spline drive wrench supplied. Unlock tape deck as described in Paragraph 2.1. Clost dust cover door.

3. Open tape deck taking care that the transport does not tip forward.

4. Remove dust cover door and rim by removing 5 flat-head screws located at the perimeter on the back of the tape deck. Lift cover door and rim off.

5. Close tape deck and lock in place.

6. Place transport on its back so that reels are facing up.

7. Remove screws which mount transport to metal shipping frame.

8. Lift transport out of shipping frame and place in new cabinet.

9. Line up mounting holes of transport and cabinet and bolt transport to cabinet.

NOTE

TRANSPORT MOUNTING HOLES ARE FOR STANDARD RETMA RACK MOUNTING.

10. Open tape deck and replace dust cover door and rim and capstan.

11. Clean the deck as described in the maintenance procedure.

12. Close dust cover door.

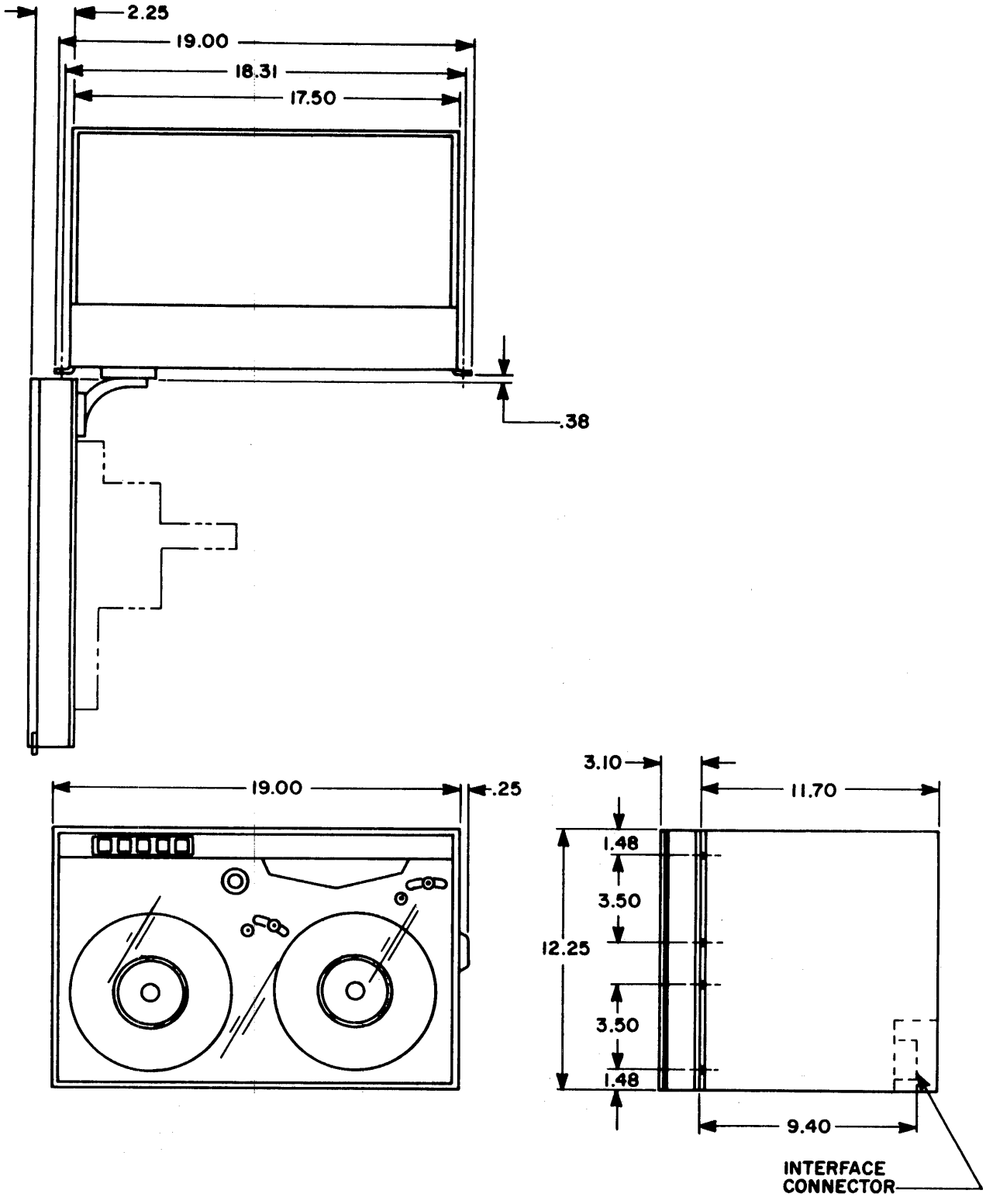

FIGURE 2-3. MOUNTING DIMENSIONS (8-1/2 INCH TRANSPORT)

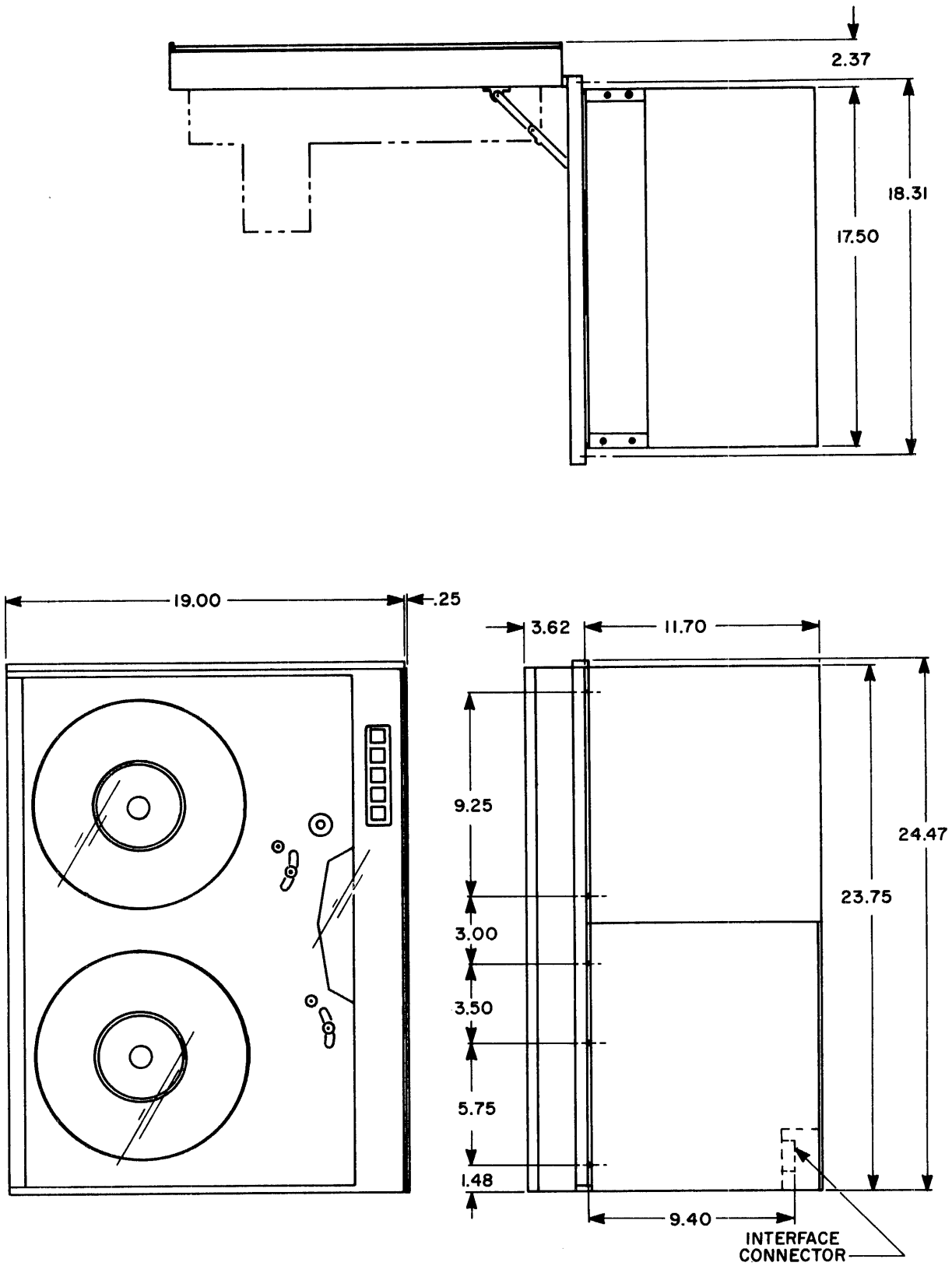

FIGURE 2-4. MOUNTING DIMENSIONS (10-1/2 INCH TRANSPORT)

2.5 Rack Mounting the 2000 Series Transport

CAUTION

WHEN REMOVING TRIM FROM THE DECK, CARE MUST BE TAKEN TO AVOID CONTACT BETWEEN THE HEAD AND GUIDES AND THE OVERLAY PLATE.

The physical dimensions of the transport are such that it may be mounted in a standard retma rack. A 24 1/2 inch panel space is required. It requires a depth behind the mounting surface of at least 12 inches.

The following procedure should be followed to rack mount the transport. Figure 2-4 shows the relevant mounting dimensions.

1. Place the transport, still in its shipping frame, in the normal operation position with the reels facing the operator.

2. Open the dust cover door, unlatch the tape deck by rotating the fastener.

3. From the inside of the deck plate disconnect the inter-chassis connector and the head cable connector bracket. Disconnect the deck retaining linkage.

4. Remove the two hinge retainers located at the bottom of the hinge blocks. Lift the deck plate assembly until the painted arm of the hinge (attached to the deck plate) clears the hinge pins and the deck is free of the chassis.

5. Separate the electronic chassis from the hinge frame and the shipping supports.

6. Mount the electronic chassis in the rack with four screws positioned opposite the relief holes in the hinge frame.

7. Mount the hinge frame over the chassis utilizing the remaining mounting holes.

8. Hang the deck on its hinges. Replace the hinge retainer, deck retaining linkage, the interchassis connector and the head connector.

SECTION III - OPERATOR INSTRUCTIONS

3.1 Operating Controls Operation of the tape transport is performed by Manual Controls located on the transport and remote controls furnished by the customer. Along with the control lines, there are additional lines sent to the customer which indicated transport status such as READY, EOT, BOT, etc.

3.1.1 Manual Controls Five operational controls with indicators are located on the front of the tape transport. These controls are used to apply AC power to the transport, bring the tape to BOT (Beginning of Tape), rewind the tape to BOT, insert a File Gap and bring the transport to the READY state.

3.1.1.1 POWER The POWER control is an alternate-action switch and supplies AC power to the power transformer. The indicator is illuminated when the switch is engaged. Both sides of the power line are switched. This applies power to the power supplies, however, it DOES NOT apply power to the capstan motor or reel motors. The LOAD FWD switch must be depressed momentarily in order to supply capstan motor and reel motor power.

3.1.1.2 LOAD FWD The LOAD FWD control is a momentary switch which is illuminated when depressed after power has been applied to the capstan motor and reel motors. After power has been applied to the transport and tape has been loaded, momentarily depressing the LOAD FWD switch closes the interlock relay, applying ground returns to the capstan motor and reel motors. When tape is loaded on the transport but has not been tensioned

so that the limit switch on the take-up storage arm is still open; momentary depression of the LOAD FWD control by-passes the switch and allows the reel motors to bring the storage arms to their nominal operating position.

After the tape has been loaded and power applied to the capstan motor and reel motors, both reel servos will maintain the storage arm in the nominal operating position.

To bring the tape to BOT, the LOAD FWD control must again be depressed and held depressed until the BOT tab has passed the phototab detector. After the BOT tab has been detected, the tape will be brought to a controlled stop with the BOT tab displaced the proper distance from the RECORD head even though the LOAD FWD control is still depressed. Detecting the BOT tab also places the transport in the READY condition and illuminates the READY indicator. When the tape has come to a stop, the LOAD FWD control may be released.

After the tape has been brought to BOT, when the LOAD FWD control is again depressed, the tape will move at 12 ips (inches per second) until the control is released.

CAUTION

WHEN THE READY INDICATOR IS ILLUMINATED, WRITE CURRENT IS FLOWING IN THE HEAD. THEREFORE, ANY TAPE MOTION WILL RESULT IN TAPE ERASURE.

3.1.1.3 FILE GAP The FILE GAP control is a momentary switch which is illuminated when depressed. Pressing the FILE GAP control generates a

standard IBM compatible file gap on the tape.

3.1.1.4 REWIND The REWIND control is a momentary switch which when depressed initiates a REWIND command to the transport. When the REWIND control is depressed, the transport goes into the REWIND state and will continue in REWIND until the BOT tab is detected. When the BOT tab is detected, the tape comes to a controlled stop. When the REWIND control is again depressed, after having rewound to BOT, the tape will run in reverse until the control is released. This technique can be used to assist in unloading the tape from the take-up reel when the supply reel is to be removed.

3.1.1.5 READY The READY control is a momentary switch which is illuminated when the transport is in the READY state. READY state indicates write current is on and the transport is ready to receive commands.

The transport can be placed in the READY state by:

1. Loading tape on the transport and bringing tape to BOT by use of the LOAD FWD control.

2. Applying power to the transport and momentarily depressing the LOAD FWD control to apply capstan and reel motor power, then momentarily depressing the READY control. This is useful when bringing the transport to READY in an IRG.

3. Applying power to the transport and momentarily depressing the LOAD FWD control. Depress the LOAD FWD control again and then momentarily depress the READY control. Using this procedure, the transport goes through

the same sequence as if this were a BOT command. This is useful when bringing the transport to READY when a BOT tab is not used.

To remove the READY state, one of the following must be done.

1. Turn power OFF.

2. Apply external RESET.

3. Place the transport in the REWIND mode.

All of the MANUAL CONTROLS except POWER may be inhibited remotely.

3.1.2 Interface Inputs Certain operational controls must be provided remotely. These are WRITE STEP command, the IRG command, REMOTE RESET and ECHO CHECK RESET. All manual control functions except POWER may be supplied remotely.

3.1.2.1 WRITE STEP The WRITE STEP command requires a pulse on the WRITE STEP line to initiate a write sequence. The voltage level, and polarity depend upon the interface card selected by the customer. When a WRITE STEP command is received, the tape is moved the proper displacement to give the required bit spacing, the data is recorded on tape and the tape stopped.

3.1.2.2 IRG (INTER-RECORD GAP) The IRG command requires a pulse be given on the IRG line of sufficient width, magnitude and polarity.

After all the data in a record has been received, an IRG command is received and the transport generates an IBM compatible IRG.

3.1.2.3 REMOTE RESET REMOTE RESET requires a level which when true resets all relevant flip-flops in the control logic.

3.1.2.4 ECHO CHECK RESET The ECHO CHECK RESET requires a level which when true, holds the ECHO CHECK ERROR flip-flop reset.

3.1.3 INTERFACE OUTPUTS Outputs are available from the transport interface which indicate certain operations have been performed or conditions exist.

3.1.3.1 EOT This line is true when the EOT tab is being detected. When the tab moves away from the detector, the line is false.

3.1.3.2 BOT This line is true when the BOT tab is being detected.

3.1.3.3 GAP IN PROCESS This line is true when an IRG or FILE GAP is in process.

3.1.3.4 TAPE NOT TENSIONED This line is true when the tape storage arms are not in the nominal operating position.

3.1.3.5 TRANSPORT READY This line is true when the input buffer is in a condition to receive data.

3.1.3.6 BUFFER 1 BUSY This line is true as long as there is data to be recorded in the input buffer.

3.1.3.7 ECHO CHECK PARITY ERROR (optional) This line is true when

a parity error in the echo check output is detected. This line must be reset by the customer.

3.1.3.8 MOTION CHECK (optional) This line changes from true to false or from false to true each time the capstan shaft is rotated through one bit space.

3.2 Operation

3.2.1 Loading Tape on Transport The 1000 Series transport in the position shown in Figure 3-1 has the take-up reel on the left side as one faces the transport located below the manual controls. The supply reel (reel to be recorded) is located on the right-hand side.

The 2000 Series transport in the position shown in Figure 3-2 has the take-up reel on the top as one faces the transport, located to the left of the manual controls. The supply reel (reel to be recorded) is located below.

CAUTION

BE SURE THE SUPPLY REEL IS SUCH THAT TAPE WILL UNWIND FROM THE REEL WHEN THE REEL IS TURNED CLOCKWISE WHILE FACING THE TRANSPORT. THIS IS SHOWN IN FIGURE 3-1 or FIGURE 3-2.

3.2.1.1 Reel Loading To load the supply reel, position the reel over the reel retainer hub, then depress the center plunger. This will allow the reel to slip over the rubber rim on the reel retainer. Press the reel evenly and firmly against the back of the reel retainer hub while the center plunger is de-

1-A

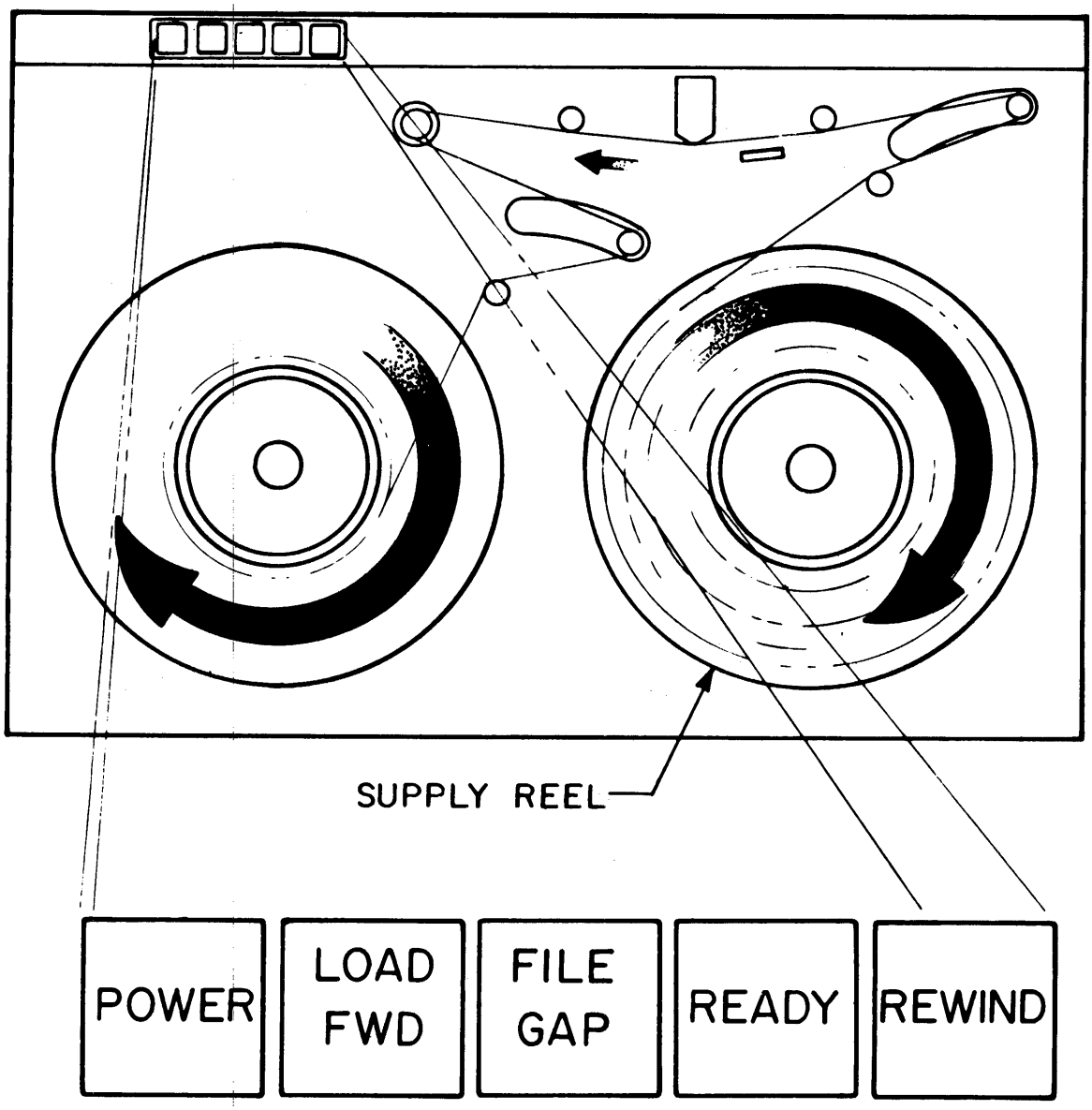

FIGURE 3-1. TAPE PATH AND CONTROLS 8-1/2 INCH TRANSPORT

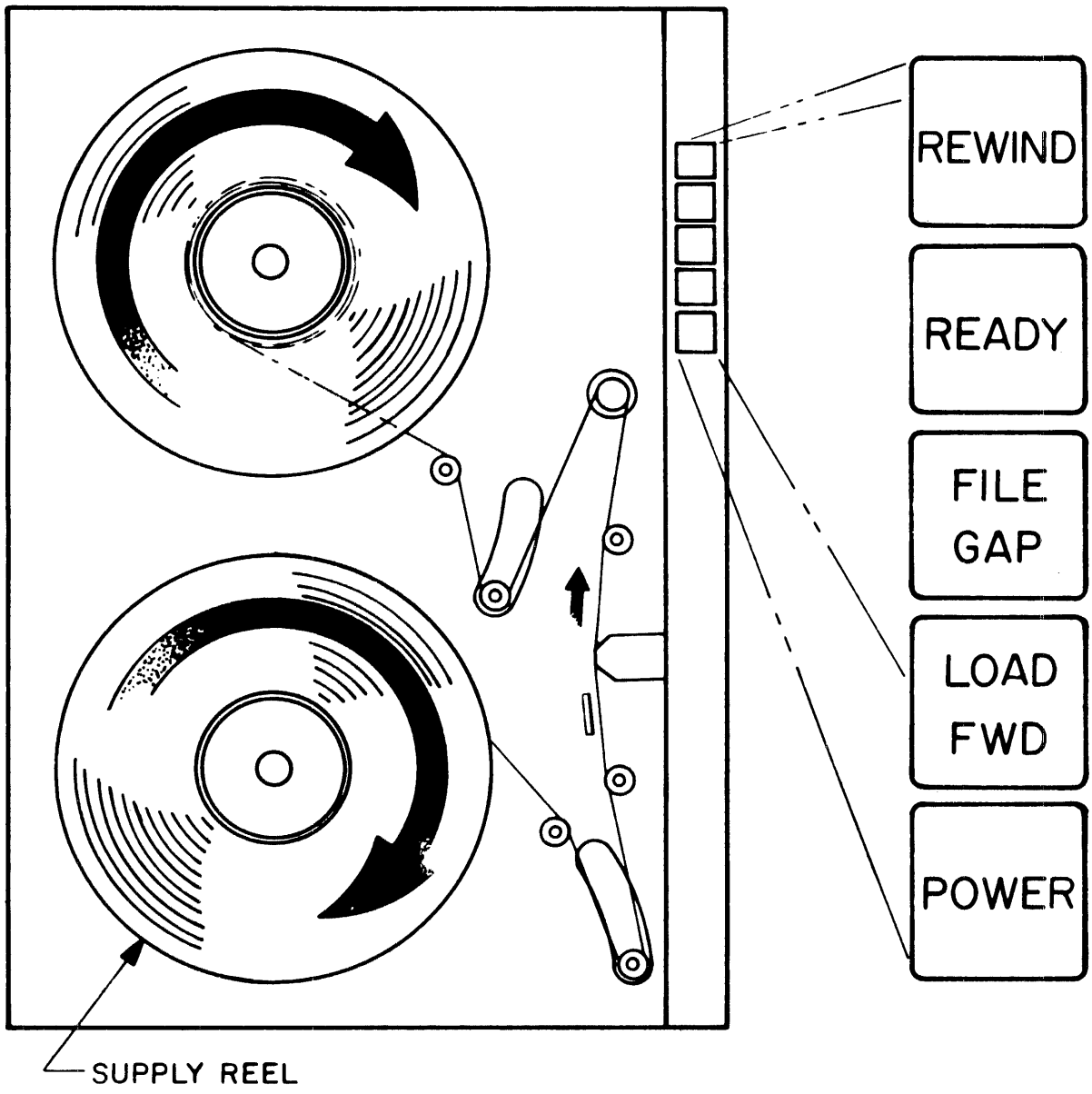

FIGURE 3-2. TAPE PATH AND CONTROLS 10-1/2 INCH TRANSPORT

pressed. While holding the reel in this position, release the center plunger. The reel is now properly aligned in the tape path and ready for tape threading.

3.2.1.2 Tape Threading Thread the tape through the transport as shown in Figure 3-1 or Figure 3-2.

Wrap the tape leader on the take-up reel such that the tape will be wound on the reel when the reel is rotated clockwise.

Wind several turns on the take-up reel, then turn the supply reel counter-clockwise until slack tape has been taken up.

CAUTION

IF SLACK IS LEFT IN THE TAPE, TAPE DAMAGE MAY RESULT WHEN POWER IS APPLIED.

CAUTION

AFTER THE TAPE HAS BEEN MANUALLY TENSIONED, CHECK TO BE SURE THE TAPE IS PROPERLY LOCATED IN ALL GUIDES OR TAPE DAMAGE MAY RESULT.

CAUTION

CLOSE THE DUST COVER DOOR AND KEEP IT CLOSED EXCEPT WHEN CHANGING TAPE REELS. DATA RELIABILITY WILL BE IMPAIRED DUE TO TAPE CONTAMINATION IF THE DOOR IS LEFT OPEN.

3.2.1.3 Bring Tape to BOT After the tape has been loaded on the transport, the following steps should be followed to bring the tape to BOT.

1. Turn power on by depressing the POWER control on the Manual Control Panel. The POWER control indicator will be illuminated.

2. Momentarily depress the LOAD FWD control. This will apply power to the capstan motor and reel motors. This allows the reel servos to operate bringing the tape storage arms to the nominal operating position.

CAUTION

CHECK TO SEE THAT THE TAPE IS POSITIONED PROPERLY ON ALL GUIDES GUIDES OR TAPE DAMAGE MAY RESULT.

3. Depress the LOAD FWD control. This will move the tape forward at a velocity of 12 ips. When the BOT tab is detected, the tape will come to a controlled stop with an IBM compatible displacement between the tab and the record head.

The LOAD FWD control may now be released.

When the above sequence has been followed, the READY indicator will be illuminated when the BOT tab is detected.

The transport is now ready to record data.

CAUTION

CLOSE THE DUST COVER DOOR AND KEEP IT CLOSED EXCEPT WHEN EXCHANGING TAPE REELS. DATA RELIABILITY WILL BE IMPAIRED DUE TO TAPE CONTAMINATION IF THE DOOR IS LEFT OPEN.

3.2.1.4 Bring the Transport to the READY State Bringing the transport to the READY state when a new tape has been put on the transport is described in Paragraph 3.2.1.3.

CAUTION

IF RECORDS HAVE BEEN RECORDED ON THE TAPE AND TRANSPORT POWER IS TURNED OFF, THE FOLLOWING SEQUENCE IS TO BE FOLLOWED:

BE SURE TAPE TENSION IS MAINTAINED WHEN POWER IS OFF TO INSURE NO TAPE MOTION ACROSS THE HEAD. TAPE MOTION COULD RESULT IN LOSS OF DATA WHEN THE TRANSPORT IS RETURNED TO THE READY STATE.

1. Turn power on by depressing the POWER control.

2. Momentarily depress the LOAD FWD control.

3. At this point, one of two procedures may be followed:

a. Depressing the READY control places the transport in a READY state without tape motion. This procedure is used if the succeeding data is to be separated from that already recorded by an IRG.

b. Depress the LOAD FWD control, then momentarily depress the READY control. This acts like a BOT tab command and moves the tape approximately 4.25 inches before stopping. This piece of tape will be erased. This procedure is used if the succeeding data is to constitute a new file.

3.2.2 Unloading the Tape To unload a recorded tape, the following procedure should be followed if the power has been switched off (if power has been switched off and the READY indicator is illuminated, enter the procedure at Step 3).

1. Turn the transport power on.

2. Momentarily depress the LOAD FWD control to apply capstan

motor and reel motor power.

3. Momentarily depress the REWIND control. When the tape has rewound to BOT, the tape will come to a controlled stop.

NOTE

WHEN REWIND HAS BEEN INITIATED, THE TAPE CANNOT BE STOPPED UNTIL IT REACHES BOT UNLESS TRANSPORT POWER IS TURNED OFF. AFTER DETECTING BOT, THE LAST FEW FEET OF TAPE CAN BE REWOUND UNDER CONTROL OF THE REWIND CONTROL. WHEN THE REWIND CONTROL IS RELEASED, THE TAPE WILL STOP. DEPRESS THE REWIND CONTROL AND ALLOW THE TAPE LEADER TO WIND ONTO THE SUPPLY REEL. WHEN THE TAPE LEADER HAS EMPTIED FROM THE TAKE-UP REEL, TAPE TENSION WILL BE LOST ALLOWING THE TENSION ARMS TO MOVE TO THE UNLOAD POSITION. WHEN THE STORAGE ARMS MOVE TO THIS POSITION, AN INTERLOCK SWITCH IS ACTIVATED WHICH REMOVES POWER FROM THE CAPSTAN MOTOR AND REEL MOTORS.

Open the dust cover door, depress the reel hub retainer plunger and remove the supply reel. Close the dust cover door.

SECTION IV - THEORY OF OPERATION

4.1 Introduction. This section provides a general theory of operation of the Incremental Write Tape Transport and a detailed description of the operation of the printed circuit boards used in the tape transport.

4.2 General Theory. The transport consists of mechanical and electronic components necessary to generate a tape from which the data can be completely recovered when played back on an IBM digital tape transport or its equivalent. The systems that comprise the transport are

- The power supplies
- The capstan drive system
- The mechanical tape storage systems and associated reel servos
- The magnetic recording head and associated tape guides
- The data recording electronics
- The control logic required to bring the transport to operational status, the logic to generate IBM compatible INTER-RECORD and FILE gaps with appropriate mark and check characters, and the logic to generate lateral parity.

4.2.1 Power Supplies. Figure 4-1 is a block diagram of the power supplies. The AC power lines, both live and neutral, are controlled by the POWER switch. A series 20-ohm resistor in the neutral line limits the surge of current into the power supply capacitors. This resistor is shorted when the

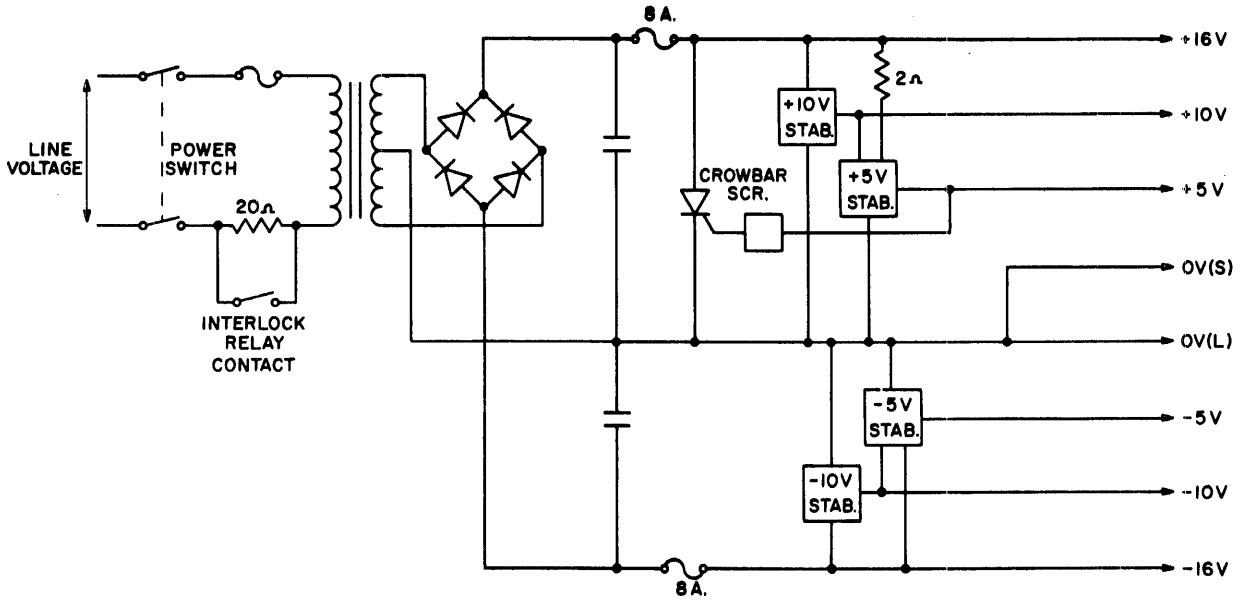

FIGURE 4-1. BLOCK DIAGRAM POWER SUPPLY

interlock relay contacts are closed. Unregulated DC, at a nominal ± 16 volts is used to drive the motors and the regulated supplies. Four regulated supplies are generated. The ± 10-volts lines are regulated to ± 7% and can supply 300 milliamps each. The reference diodes in the ± 5-volt regulators are driven from the ± 10-volt lines. The ± 5-volt lines are adjusted and regulated to within ± 1% and can supply 2.0 amps.

Since DTL integrated circuits are widely used, it is necessary to employ a SCR for "crowbar" protection against over-voltages on the +5-volt line. The circuits used can withstand up to 12 volts for 1 second. When the +5-volts line rises above 8 volts, the SCR connected between the +16 volts and 0 volts

on the regulator side of the + 16 volt fuse is turned on. This holds the voltage on the integrated circuits down until the fuse blows a few milliseconds later. A separate 0-volt line is used for the high current circuitry and is called OV (S) (S for servo). The logic circuitry 0-volt line is called OV(L) (L for logic). They are eventually connected together at the power-distribution terminal block (TB201).

4.2.2 Capstan Drive System. Figure 4-2 is a diagram of the capstan drive system. The tape drive mechanism consists of a DC motor, a capstan,

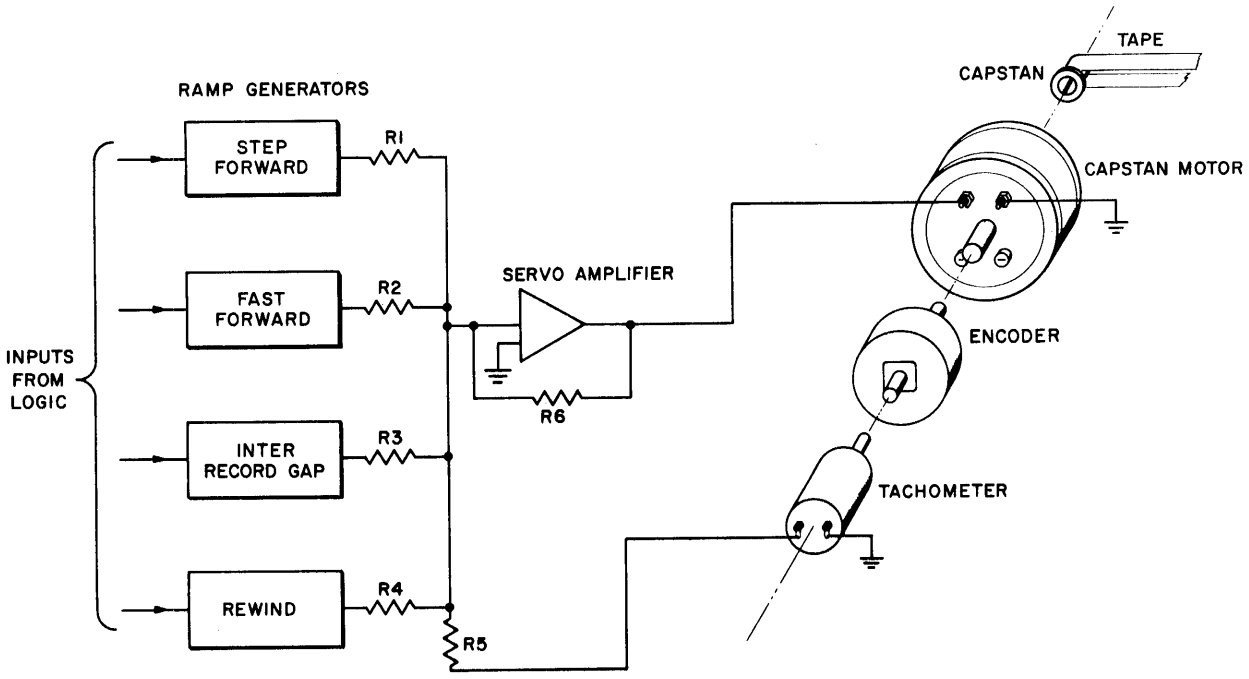

FIGURE 4-2. BLOCK DIAGRAM CAPSTAN SERVO

an optical shaft encoder and a DC tachometer, coupled such that the encoder indicates the angular position of the capstan and the tachometer its angular velocity. The output of the encoder is processed to generate a pulse corresponding to each angular increment indication. The pulse is used to position the magnetic transitions on the tape and to generate the stop commands to the capstan drive amplifier.

The motor and tachometer are used in a conventional velocity servo which is under the control of a ramp generator. In operation, the receipt of a WRITE STEP command enables the ramp generator, permitting the tape to accelerate to a prescribed velocity. The velocity is maintained until the encoder pulse arrives, at wnich time the ramp generator is disabled causing the tape to decelerate. Unless another WRITE STEP command is received within about 2 milliseconds, the capstan velocity will reach zero. The characteristics of the ramp generator are such that the capstan comes to rest with the encoder midway between two angular indications. Figure 4-3 illustrates the relevant waveforms. In the stand-by condition, the capstan position is maintained by the motor friction.

Ramp generators corresponding to the STEP FWD, INTER-RECORD GAP, LOAD FWD, FILE GAP and REWIND functions drive the servo amplifier. Only one of these is enabled at a time. The LOAD FWD and FILE GAP functions are provided by the same ramp generator labelled FAST FWD.

The ramp generators use the +5-volt line as a voltage reference and the resistors R1, R2, R3 and R4, in Figure 4-2 are selected to give the required

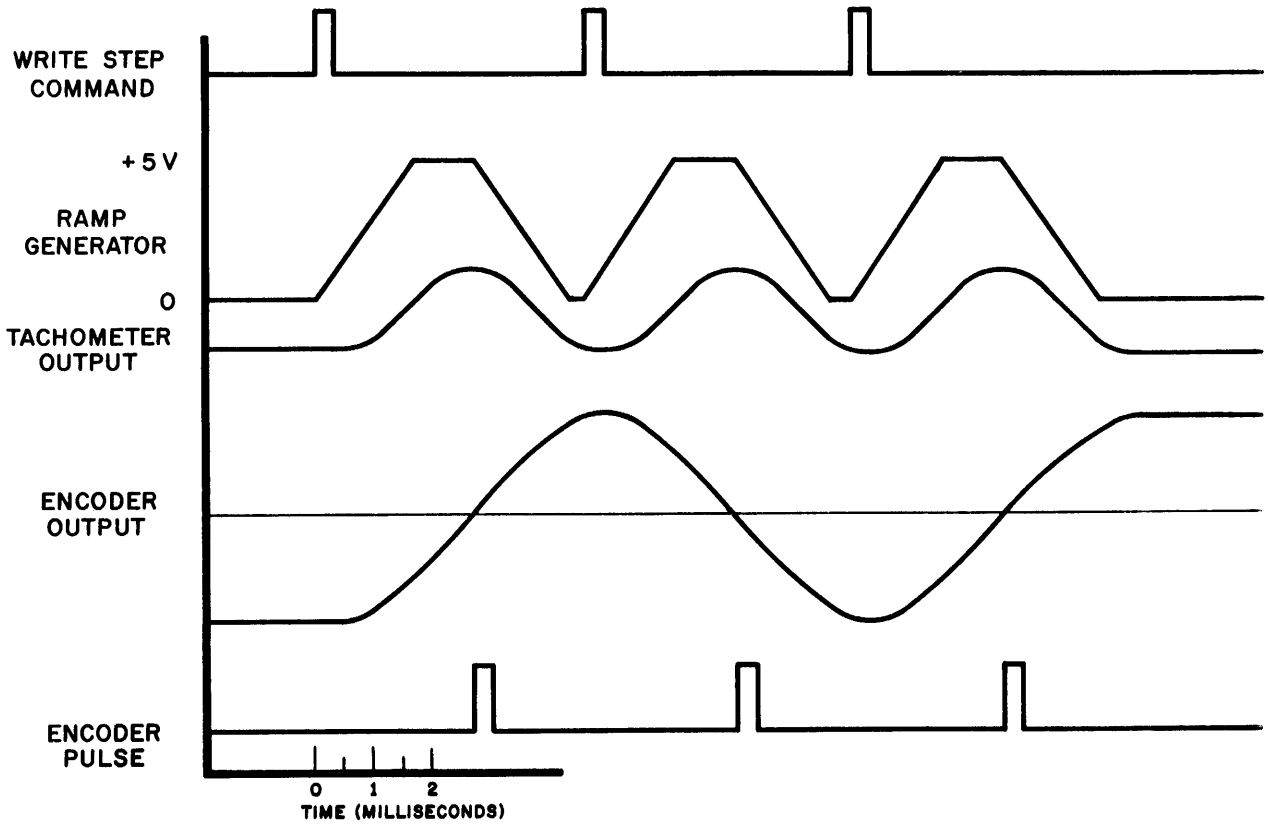

FIGURE 4-3. CAPSTAN DRIVE WAVEFORMS

capstan velocity. The STEP FWD ramp generator rises and falls in 1.0 to 1.5 milliseconds to generate a tape velocity which depends on the bit density and maximum data rate (generally of the order of 1 ips). The FAST FWD ramp generator rises and falls in 35 milliseconds to generate a velocity of 12 ips. The INTER-RECORD GAP ramp generator rises and falls in 18 milliseconds and

generates a velocity of 25 ips. The REWIND ramp generator rises and falls in between 0.5 and 1.0 seconds to generate a reverse velocity of 75 ips (some transports operate at 50 ips). The long rise and fall times of the REWIND ramp generator are required to prevent the tape storage arms moving outside their operating region during the tape acceleration and deceleration.

Tape is held on the capstan by friction and is in contact with the capstan through an angle of 180°. A tape tension of 8 ounces assures no possibility of slippage.

4.2.3 Reel Servo System. Figure 4-4 is a diagram of a reel servo. Identical linear position servos control the supply and take-up of tape by the reels. The storage arms isolate the inertia of the reels from the capstan. Low-friction ball-bearing guides are used to minimize tape tension variations. The position of the storage arm is sensed by a long-life potentiometer. The potentiometer output, after amplification, drives the reel motor in the direction to center the arm. The geometry of the storage arm and spring ensure that negligible tape tension changes occur as the storage arm moves through its approximately 30° arc.

With tape stationary, the storage arms take up a position such that the amplified potentiometer output, when applied to the reel motor, produces enough torque to balance the spring torque. Initially the potentiometers have been set by rotating the body of the potentiometers so that the tension arms operate in the center of their range. The position of the storage arm changes slightly for different steady-state capstan velocities. This occurs because

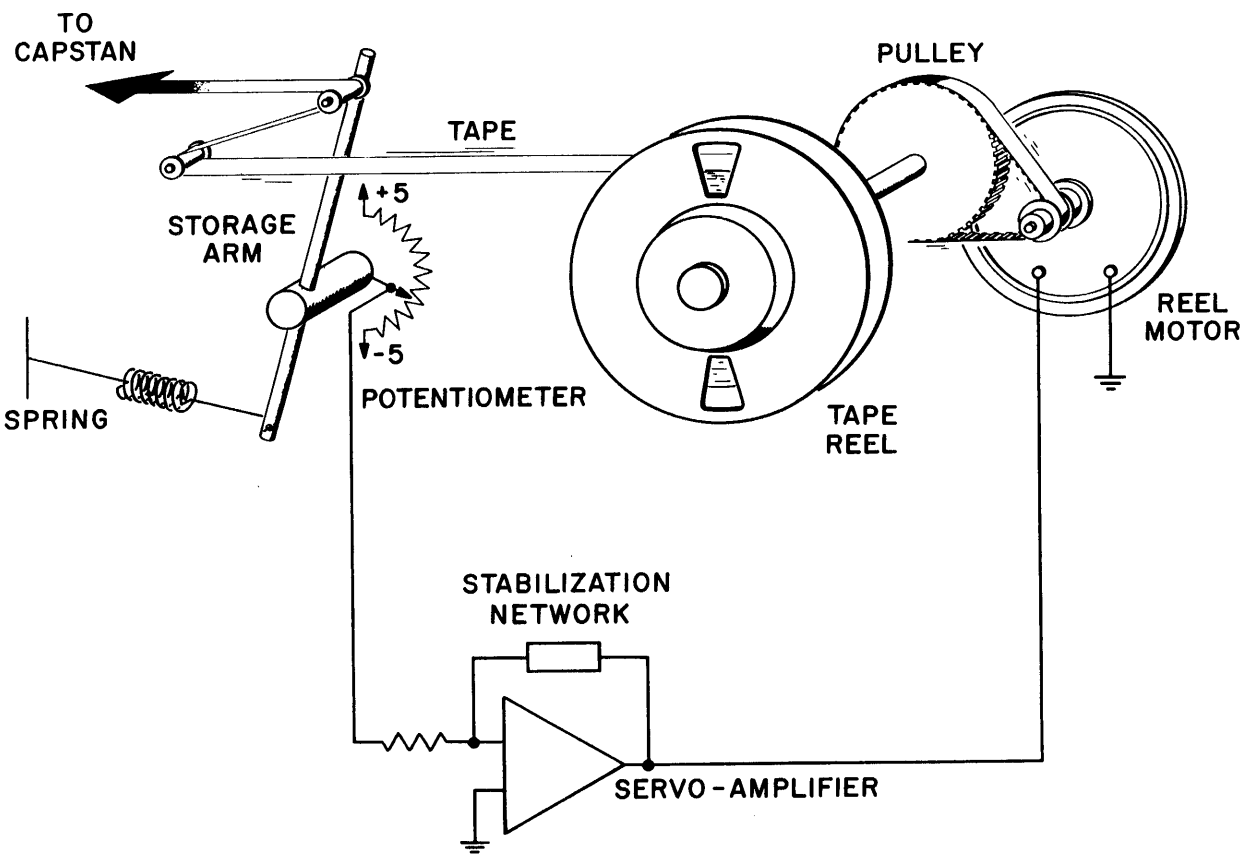

FIGURE 4-4 REEL SERVO DIAGRAM

the amplifier output varies with the back EMF of the motor requiring corresponding input voltages from the potentiometer.

When the capstan injects a tape velocity transient in either direction, the arm moves and the potentiometer output changes, driving the reel motors in the direction to recenter the arm.

Without tape, the arms rest against the stops and the tension-arm limit switch is open removing power to all motors.

Each motor is driven by a linear amplifier with transitional-lead servo stabilization. The low frequency gain of the amplifier is 18 volts-per-volt. The zero of the stabilization network is at 1.5 Hz, and the pole at 7.5 Hz.

With 10 volts across the potentiometer, the gain is 1.6 volts/radian. The amplifier gain is 18 volts/volt and the motor gain is 30 radians/second/volt. The motor velocity is stepped down by a pulley ratio of 5 : 1, so that the open loop gain (reel velocity divided by arm displacement) is 175 radians/second/radian. From the above it can be seen that in order to rewind at 75 ips, i.e., 30 radians/second, the arm will be displaced about 1/6 of a radian.

4.2.4 Data Recording and Control Systems. The data recording and control components must enable the following functions to be performed.

- Bring the transport from a switched off state to a state in which it can receive and record data.
- Enable the transport to be switched on and off in such a manner that no significant movement of the tape occurs.
- Rewind tape.
- Record data of asynchronous origin in a NRZI format.
- Insert such gaps and special characters as are required by IBM compatability.

The first three functions are performed by manual (or remote) controls in conjunction with the BOT (Beginning of Tape) sensor, an interlock relay, and the control logic as described in the following paragraphs.

4.2.4.1 Bringing Machine to Operational Status. Operation is best understood by considering the sequence required to achieve operational status. Figure 4-5 is a basic logic diagram illustrating the necessary components and interconnections. When the recorder is located some distance from the associated equipment, it is desirable, after bringing the machine to operational status, to ensure that the manual controls cannot be inadvertently operated. When the DISABLE MANUAL CONTROLS signal (which is generated externally) is high, operation of any of the manual controls (except the POWER switch) cannot generate the low signal required to set the associated flip-flops.

4.2.4.1.1 Press POWER Control. This actuates an alternate action switch which applies AC power to the power supply via the 20 - ohm resistor. The value of this resistor is chosen to limit the input surge caused by the condenser-input filter network, but it is not sufficient to disturb the regulation of the stabilized power supplies when under the following conditions, which now exist.

- All power supplies are established; namely ±16 v, ±10 v, ±5 v.
- The interlock relay is de-energized and contacts K-A, K-B, K-C, K-D and K-E are open.
- The return lines for the two reel motors and the capstan motor are open circuited via contacts K-C, K-D and K-E.
- A GENERAL RESET signal (GRS) is applied to all relevant flip-flops. GRS can also be initiated externally.

- The TRANSPORT READY line is false.
- The TAPE NOT TENSIONED line is true.

Tape can be loaded and threaded while in this condition since power is not applied to the motors.

4.2.4.1.2 Press LOAD FWD Control (First Time). This by-passes the tension-arm limit switch and the relay-latching contact K-B, energizing the interlock relay. Providing that the tape is correctly loaded, power is now applied to the reel motors. The motors move the reels in such a direction so as to establish tape tension. The tension arms move into their operational region and the tension-arm limit switch closes allowing the interlock relay to latch. The LOAD FWD control may now be released. At this time the GRS signal is removed and the TAPE NOT TENSIONED signal becomes false.

If at any time the tension arms move outside their operating region, the interlock relay de-energizes, power is disconnected from the motors, and the GRS signal is applied. The tension-arm limit switch opens at both extremes of the arm travel. This provides protection against over-tension as well as under-tension conditions.

4.2.4.1.3 Press LOAD FWD Control (Second Time). If the LOAD FWD control is depressed and held, the following sequence occurs:

- Flip-flop 5A is set via OR gate 501 and the $\overline{Q}$ output is differentiated by differentiator 5d1. The output pulse sets flip-flop 5B. Flip-flop 5A is used in conjunction with the LOAD FWD-DPDT switch to eliminate the effects of contact bounce.

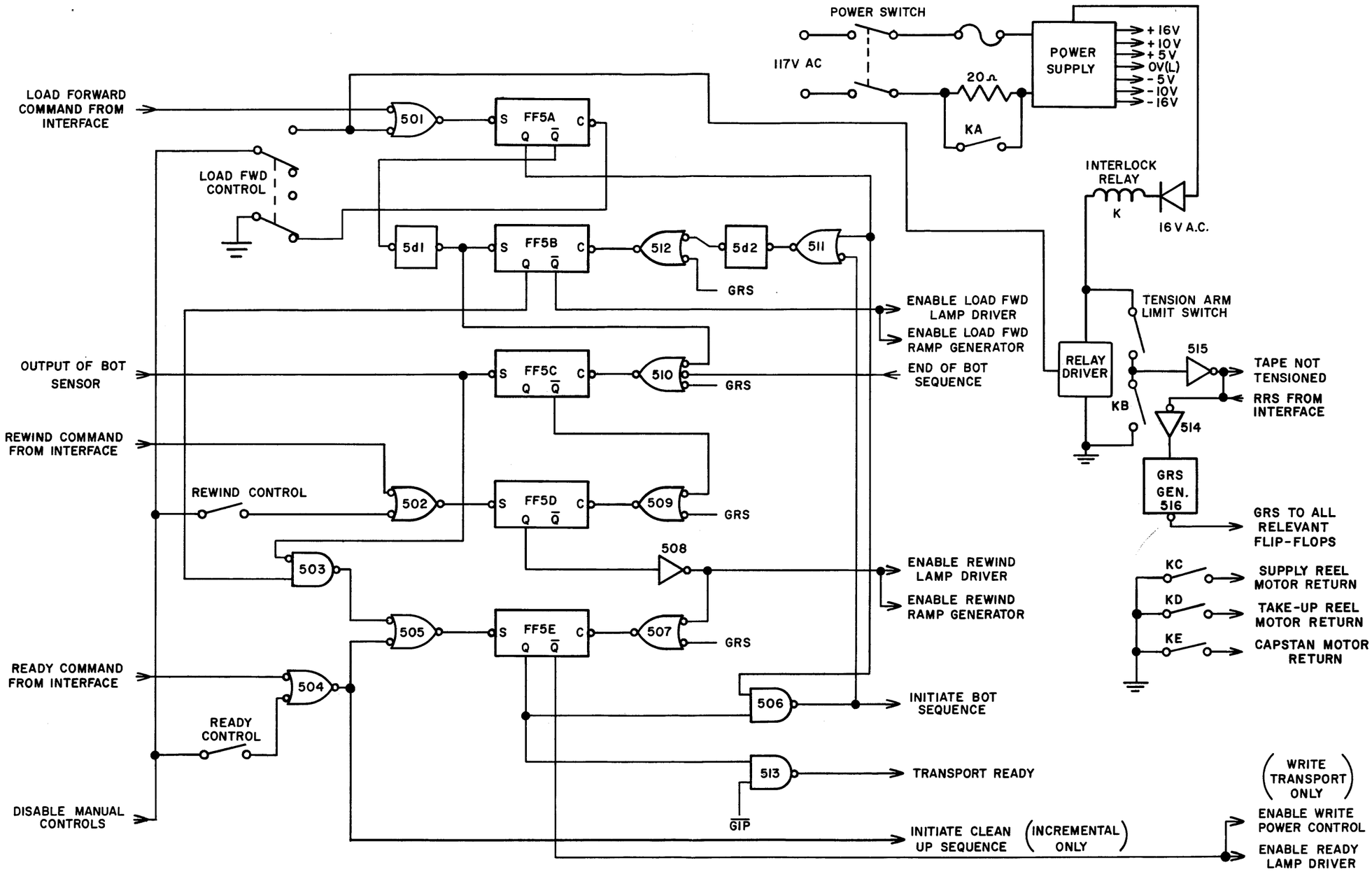

FIGURE 4-5. CONTROL LOGIC TO BRING TRANSPORT TO OPERATIONAL STATUS

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- The $\overline{Q}$ output of flip-flop 5B enables the LOAD FWD lamp driver and the FAST FWD ramp generator causing the tape to accelerate to 12 ips. One input of AND gate 503 is enabled by the Q output of flip-flop 5B.
- Tape motion will continue until the BOT tab reaches the BOT sensor at which time the second input of AND gate 503 is enabled.
- The output of AND gate 503 sets flip-flop 5E via OR gate 505.
- The $\overline{Q}$ output of flip-flop 5E enables the WRITE POWER control so that WRITE current is switched on and also enables the READY lamp driver. The WRITE current turn-on times and turn-off times are made sufficiently long so that no spurious signals are recorded due to overshoots and eddy-current effects in the head.
- Since the LOAD FWD Control is still depressed, the BOT sequence is initiated via AND gate 506 and flip-flop 5B is reset via OR gates 511 and 512 disabling the FAST FWD ramp generator and lamp driver. The BOT sequence is identical to the FILE GAP sequence described later in Paragraph 4.2.4.6.4 except that no file mark is written. Thus the tape moves a further 4.50 inches past the BOT tab.
- Just prior to the time that the BOT is initiated, the record head is adjacent to the tape forward of the BOT tab. Since the WRITE-current generator flip-flops are held reset when the BOT is initiated, this portion forward of the BOT tab plus a portion of

the tape behind the tab is erased. The total length of erased tape is approximately 4.50 inches which establishes IBM compatibility.

- While the BOT sequence is in process, the not GAP IN PROCESS $\overline{(GIP)}$ signal will be false. When flip-flop 5E is set, one input to AND gate 513 is true. After completion of the BOT sequence, $\overline{GIP}$ is true enabling AND gate 513 which indicates TRANSPORT READY. Since the TRANSPORT READY signal is true the transport is now ready to receive data.

If at any time before the BOT tab arrives the LOAD FWD control is released, flip-flop 5A resets flip-flop 5B via OR gate 511, differentiator 5d2 and OR gate 512. When flip-flop 5B is reset, the FAST FWD ramp generator is disabled. Depressing the LOAD FWD control again will restart tape motion.

4.2.4.1.4 Special Case When a BOT Tab is not Attached. Sometimes a BOT tab is not attached to the tape. It is then possible to bring the machine to operational status by the following sequence:

- After the operations described in Paragraph 4.2.4.1.1 and 4.2.4.1.2 is performed, tape motion will be initiated as described in the first two steps of Paragraph 4.2.4.1.3. After an adequate amount of tape has moved and is set.
- The READY control is depressed, flip-flop 5E is set via OR gates 504 and 505 and results in the conditions described in the last three steps of Paragraph 4.2.4.1.3.

In essence, depressing the READY control simulates the occurance of the BOT tab.

4.2.4.1.5 Special Case When Operational Status is Required Without Tape Motion. Provision has been made to cover the following situation.

After recording data, it may be required to turn power off, and at a later time turn power on and re-establish operational status without tape motion. The end of a data record will always be followed by an IRG, and any tape motion which occurs during re-establishment of operational status must still leave the tape within the confines of the IRG dimensions.

No tape motion on 'switch off' is ensured since when power is turned off, the interlock relay which de-energizes rapidly, opens the three motor returns, removing power from the capstan and reel motors. However, the power supplies remain for approximately 100 milliseconds (due to the storage capability of the capacitors) and, therefore, no transients are generated by the servo amplifier until after the motors are disconnected.

When power is off, tape movement is prevented by system friction. Care must be taken that the system is not disturbed manually or by vibration in order to ensure the tape remaining within the confines of an IRG.

Operational status is re-established by the following procedure.

- When POWER control is on and the LOAD FWD control momentarily depressed, tape tension is established and GRS is removed from all flip-flops.

- Depressing the READY control sets flip-flop 5E via OR gates 504 and 505 enabling the WRITE POWER CONTROL and READY lamp driver. However, since the LOAD FWD control is not depressed, AND gate 506 is not enabled and the BOT sequence is omitted. Note, however, the output of gate 504 which initiates the CLEAN UP sequence. The purpose of this sequence is to ensure the proper positioning of the optical shaft encoder between consecutive angular indications and is explained more fully in Paragraph 4.2.2. As a result, the tape moves the equivalent of four character spaces which still leaves the tape within the confines of the IRG. This CLEAN UP sequence is automatically entered at the end of the BOT sequence.

4.2.4.2 Rewinding Tape. The necessary logic and interconnections are shown in Figure 4-5.

4.2.4.2.1 Press REWIND Control. When the REWIND control is momentarily depressed, the following sequence occurs:

- Flip-flop 5D is set via OR gate 502.
- The REWIND ramp generator is enabled and the tape accelerates to the rewind speed.
- Flip-flop 5E is reset disabling the WRITE POWER CONTROL and the READY lamp driver. The TRANSPORT READY signal becomes false.

Once initiated in this manner, REWIND CANNOT BE STOPPED until a BOT tab is detected or power is switched off.

When the BOT tab is detected, flip-flop 5C is set, and flip-flop 5D is reset. The REWIND ramp generator is disabled and the tape comes to a halt. Since flip-flop 5B is not set AND gate 503 is not enabled. The output of invertor 508 is used instead of the $\overline{Q}$ output of flip-flop 5D because the permanent clear input clamps $\overline{Q}$ in the false sense and only Q can respond to the set signal from OR gate 502.

Since flip-flop 5C is set, the REWIND flip-flop 5D has a permanent clear input and further REWIND operation is now under the control of the REWIND switch. Thus if the control is depressed, tape moves in reverse until it is released. This mode of operation assists in unloading tape from the take-up reel.

Flip-flop 5C is reset when the LOAD FWD control is depressed via flip-flop 5A differentiator 5d1 and OR gate 510. The other input to OR gate 510 is to reset flip-flop 5C after the BOT tab has been detected when bringing the transport to operational status as described in Paragraph 4.2.4.1.

4.2.4.3 GENERAL RESET Generation. Due to the complexity of the GENERAL RESET (GRS) wiring, the generation of this signal and its path through the applicable circuit boards are now discussed. Figure 4-5 in conjunction with Table 4-1 will assist in understanding the circuit.

On examination of Figure 4-5, it can be seen that a GRS signal can be generated by either one of two methods; when the interlock relay is open or by a REMOTE RESET (RRS) signal from the customer via the interface.

COMPONENT SHOWN in FIGURE 4-5	BOARD ON WHICH CIRCUIT IS LOCATED		
	INPUT PIN	CIRCUIT BOARD	OUTPUT PIN
Inverter 515	C	Function Control J203	B
Inverter 514	N	Receiver, Slow Interface J205	P
	Y	Receiver, DTL Interface J205	25
GRS Generator 516	L	Capstan Drive J202	M

TABLE 4-1. CROSS REFERENCE CHART

Since the input of invertor 515 is floating when the interlock relay is open, the output of invertor 515 is low, providing a true TAPE NOT TENSIONED (TNT) signal. The output of invertor 515 is also fed to invertor 514 whose output becomes high and in turn is fed to GRS generator 516. The output of GRS generator 516 being low, provides a GRS signal to all relevant flip-flops in the system. Actually the output of the GRS generator is at - 0.7 volts, however, this voltage is compensated for by the diodes at the GRS inputs of each flip-flop requiring setting.

When the customer initiates a RRS, the signal, which is collector

OR'd to the TNT signal at the connector of the Receiver (J205), is true at the input of invertor 514. The GRS signal is then generated as explained in the previous paragraph.

4.2.4.4 Recording Information.

4.2.4.4.1 Digit Representation. Information is recorded in the NRZI mode, i.e., a '1' on the information line causes a change of direction of magnetization between positive and negative saturation levels. Two tape formats are in general use. They are the IBM 727/729 - 7-track format which can operate at 200, 556 and 800 bpi, and the IBM 2400 - 9-track format which operates at 800 bpi only. Figure 4-6 illustrates the relevant 7- and 9-track allocations and spacing. In the 9-track system consecutive data channels are not allocated to consecutive tracks. This organization increases tape system reliability since the most used data channels are located in the center of the tape and consequently are least subject to errors caused by contamination of the tape.

Illustrated in Figure 4-7 are wave forms which occur on a channel during a WRITE operation and, for reference, the read-back waveforms obtainable when played back at a constant speed on a read instrument. Magnetization transitions recorded on the tape are not perfectly sharp due to the limited resolution of the magnetic recording process.

During reading, the amplifier read-back voltage is full wave rectified (since no significance is attributable to the sign of the read-back

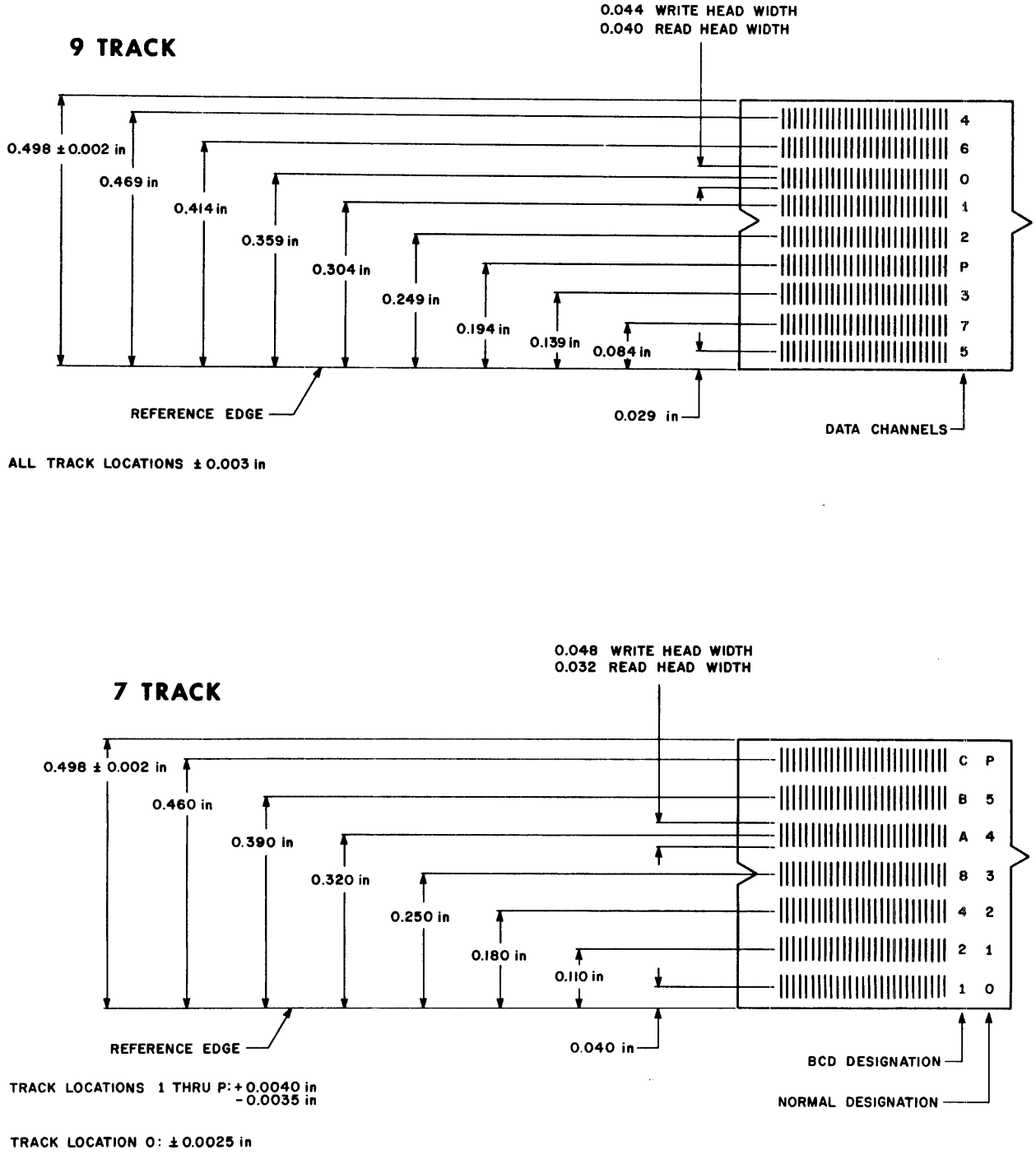


FIGURE 4-6. TRACK ALLOCATION FOR 7- AND 9-TRACK TAPE

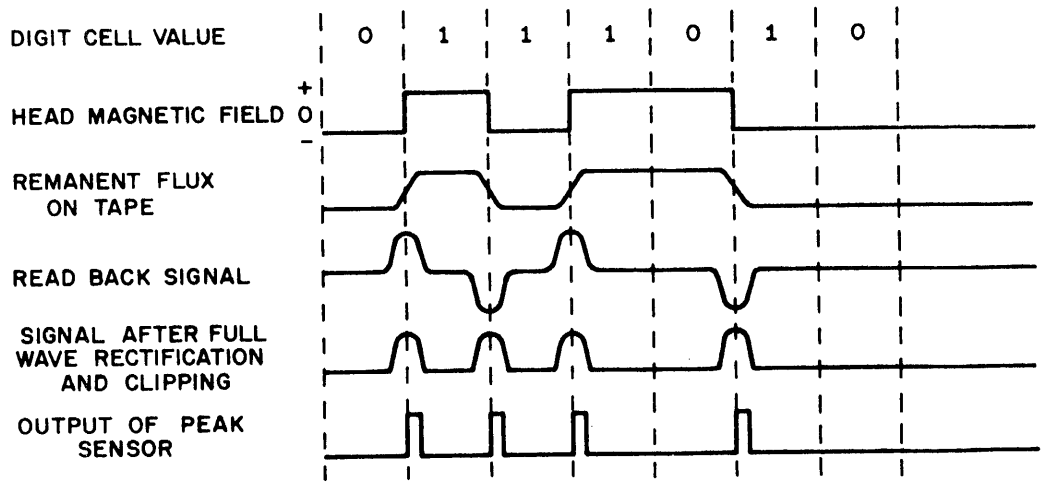


FIGURE 4-7. WRITE AND READ WAVEFORMS

voltage) and clipped to remove base line noise. This is necessary since there is no read signal output for a recorded '0'. The output of the rectifier is peak detected and a pulse generated for each '1' recorded.

4.2.4.4.2 Data Recording. The tape transports are operated at asynchronous data rates up to 1000 steps per second (sps). As previously described in Section I, this involves buffering the data while the tape is being brought to the proper speed and moved the required distance. At low data rates only one stage of buffering and one tape velocity is required, however, at higher speeds multiple stages of buffering and levels of tape velocity are necessary. The exact number depends on the maximum data rate. To cover the requirements, various printed circuit boards are provided.

The theory of operation of a double buffer system capable of 700 sps

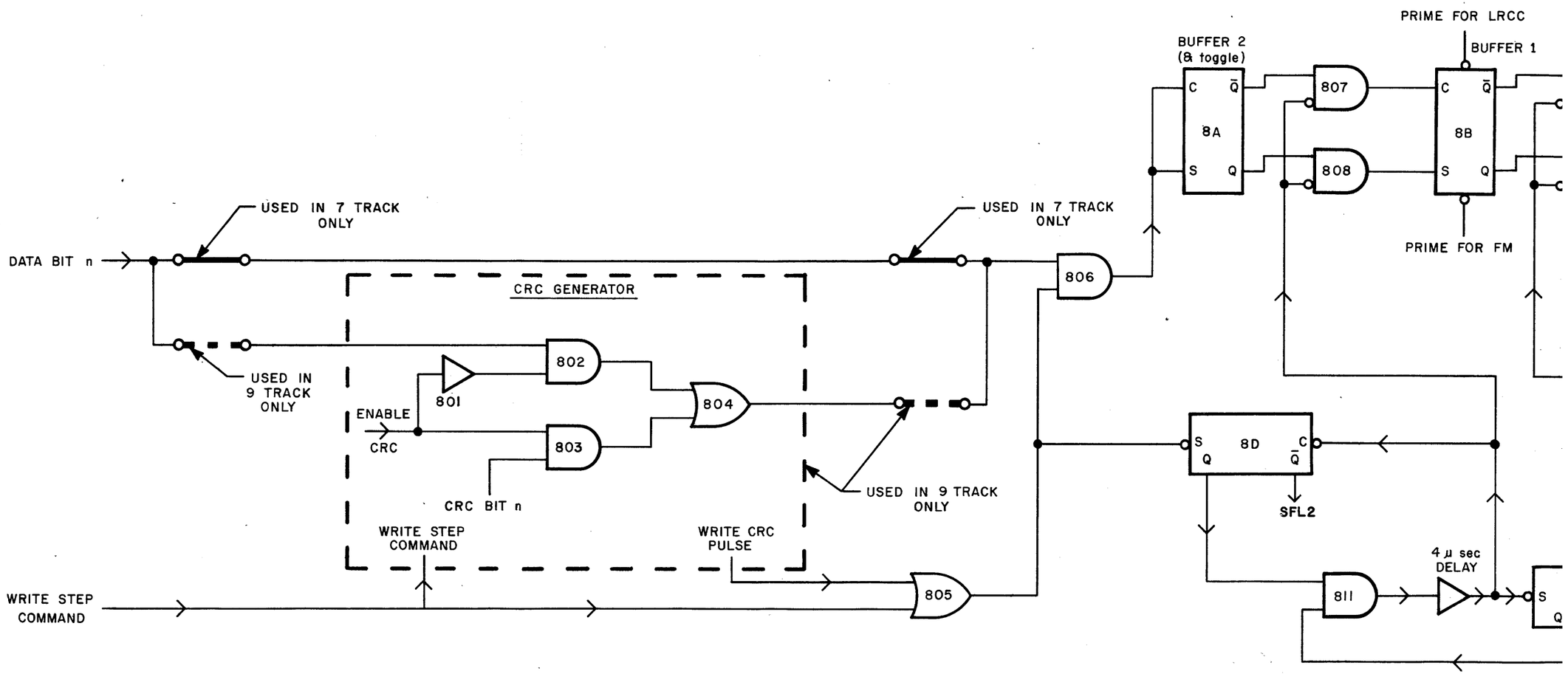
is described in the following. Operation at higher speeds involves the same principles and therefore is not described.

A description of the printed circuit boards are provided in Paragraph 4.3.

Figure 4-8 is a logic diagram of the data and step control together with one channel of data recording electronics. Not shown in this figure is a parity generation circuit which can generate odd or even parity depending on the setting of a switch and a special circuit to provide Binary 0 to BCD 10 conversion. This can be required since in some 7-track systems '0' is represented by all '0's on the data lines. This will result in an invalid character if BCD recording with even parity is being used. In this case, a special circuit is arranged to detect all '0' input condition and force the 1 and 3 channels to a '1' state so that BCD 10 is recorded. The details of the circuits are discussed fully in Paragraphs 4.3.6 and 4.3.8.

Referring to Figure 4-8, flip-flops 8A and 8B constitute the two-stage input buffer and flip-flop 8C is the WRITE current generator which in conjunction with the center tapped head maintains the magnetization on the tape in the appropriate direction between change-overs as required by the NRZI format. In a 7-track system data bit N is routed directly to gate 806. In a 9-track system, data bit N is routed to the CRC generator. During data recording gate 802 is enabled and this data bit is transferred to gate 806 via AND gate 802 and OR gate 804. It is also used to generate the CRCC.

During a gapping sequence, gate 802 is disabled and gate 803 is


DATA BIT n
USED IN 7 TRACK ONLY
USED IN 9 TRACK ONLY
CRC GENERATOR
ENABLE CRC
CRC BIT n
801
802
803
804
805
806
807
808
811
8A
8B
8D
BUFFER 2 (8 toggle)
BUFFER 1
PRIME FOR LRCC
PRIME FOR FM
SFL2
WRITE STEP COMMAND
WRITE CRC PULSE
4 μ sec DELAY
USED IN 7 TRACK ONLY
USED IN 9 TRACK ONLY
WRITE STEP COMMAND

1035

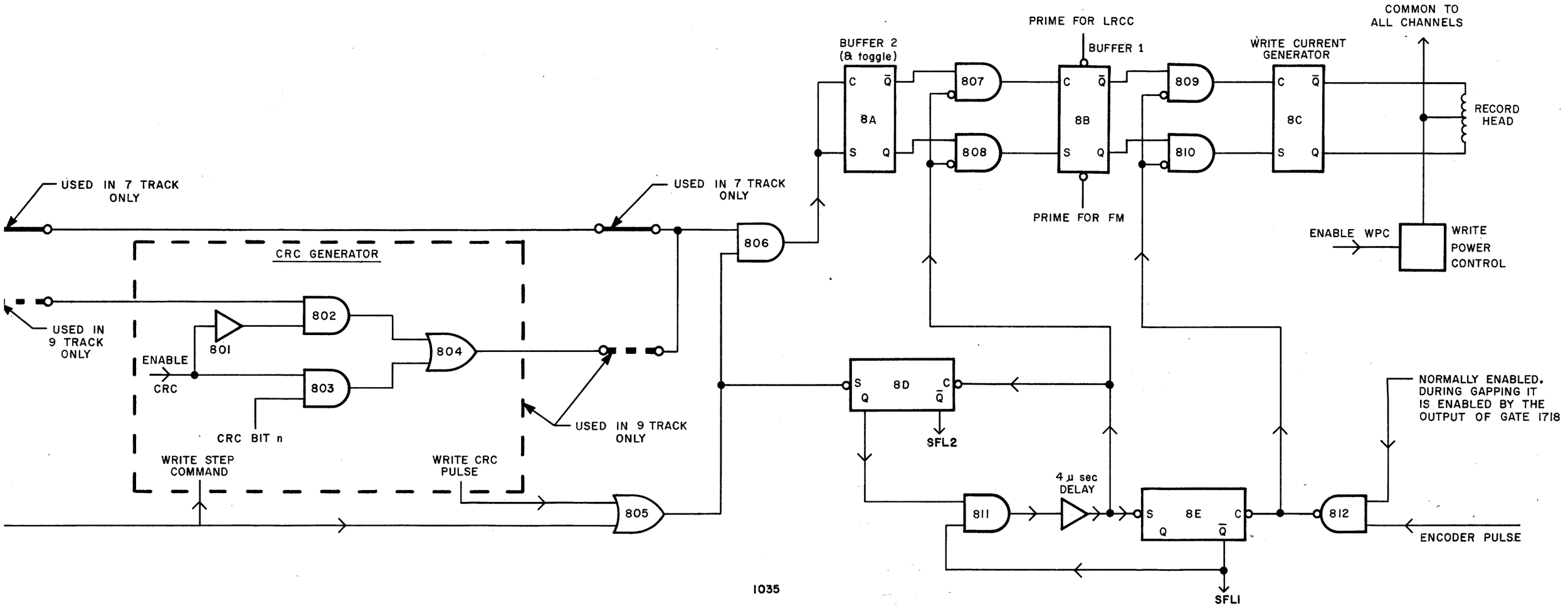


Figure 4-8. One Channel of Data Electronics

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enabled by the ENABLE CRCC waveform so that CRCC bit N is transferred to gate 806. The lines marked PRIME FOR LRCC and PRIME FOR FM are also required by the gapping sequence. Details of this gapping sequence are discussed in Paragraph 4.2.4.6.

Flip-flops 8D and 8E together with gate 806 and the 4-usec delay constitute the control loop. The outputs of flip-flops 8D and 8E are used to control the STEP FWD ramp generator. When flip-flop 8E is set, the STEP FWD ramp generator ramps to a first level of terminal voltage causing the tape to be accelerated to a slew velocity corresponding to 400 sps. Whenever flip-flop 8D is set, as well as flip-flop 8E, the ramp generator ramps to a higher second level of terminal voltage causing the tape to be accelerated to a slew velocity corresponding to 700 sps.

Operation of the system is understood by considering what happens during a recording operation. It is assumed that

- The transport has been brought to operational status so that the WRITE POWER CONTROL is enabled.
- Current is flowing in the heads.
- The encoder has come to rest halfway between two angular indications.

Three cases are now described.

4.2.4.4.2.1 Recording a Single Character. Relevant waveforms are illustrated in Figure 4-9. Initially all flip-flops are reset so that their outputs

are false. On receipt of a WRITE STEP command, the data level on the input wire is strobed into the buffer-2 flip-flop for each channel via AND gate 806. In the transport, a '1' on the data line causes buffer 2 to toggle (a '0' leaves it unchanged).

Flip-flop 8D is set and the Q output is transmitted via AND gate 811 (since flip-flop 8E is reset) to the 4-usec delay. The output of the delay resets flip-flop 8D and sets flip-flop 8E. The output of the delay is a pulse delayed 4 usec from the leading edge of the WRITE STEP command. This output also enables AND gates 807 and 808 which transfers the status of buffer 2 to buffer 1. The $\overline{Q}$ output of flip-flop 8E enables the STEP FWD ramp generator and the tape is now under control of the capstan drive system. After the tape has moved the proper distance for recording this data (this being determined by the shaft encoder) a pulse is generated by the shaft encoder circuitry which resets flip-flop 8E via AND gate 812 and copies the status of buffer 1 into flip-flop C via AND gates 809 and 810. Flip-flop 8C is the WRITE current generator and the magnetization direction is changed on the tape whenever a '1' is to be recorded. Resetting flip-flop 8E disables the STEP FWD ramp generator and the tape is decelerated. The characteristics of the ramp generator are such that the tape comes to rest nominally one-half a-character space forward of the last recorded character.

4.2.4.4.2.2 Recording Characters up to 400 sps. As the character rate is increased, the sequence described in the previous section is repeated

at the WRITE STEP command rate. As the WRITE STEP command rate is increased, flip-flop 8E will be set again before the STEP FWD ramp generator has ramped down to zero. Under these circumstances, the STEP FWD ramp generator is enabled before reaching zero. The control waveforms are illustrated in Figure 4-10. As the character rate is further increased, the output of STEP FWD ramp generator spends an increased time at the slew value. At 400 sps the STEP FWD ramp generator is set very soon after it is reset which results in a nearly constant tape velocity. In essence, flip-flop 8E in conjunction with the capstan drive and the encoder, constitute a feedback system which maintains the velocity of the tape such that the average recording rate (rate of encoder pulses) equals the WRITE STEP command rate.

4.2.4.4.2.3 Operation Above 400 sps. Consider the tape initially at rest and that a WRITE STEP command rate of between 400 sps and 700 sps is initiated. Reference to the waveforms (Figure 4-3) shows that the time from a WRITE STEP command to the arrival of the first encoder pulse is approximately 2.5 msec. Therefore, two WRITE STEP commands and their associated two characters of data can be received before the first encoder pulse occurs. The relevant control loop waveforms for this case is illustrated in Figure 4-11.

On receipt of the first WRITE STEP command, the data levels on the input wires are strobed into buffer 2 which toggles if the input data is a '1'. As described previously, flip-flop 8D is set and 4-usec later is reset, while flip-flop 8E is set. The output of the 4-usec delay transfers the contents of

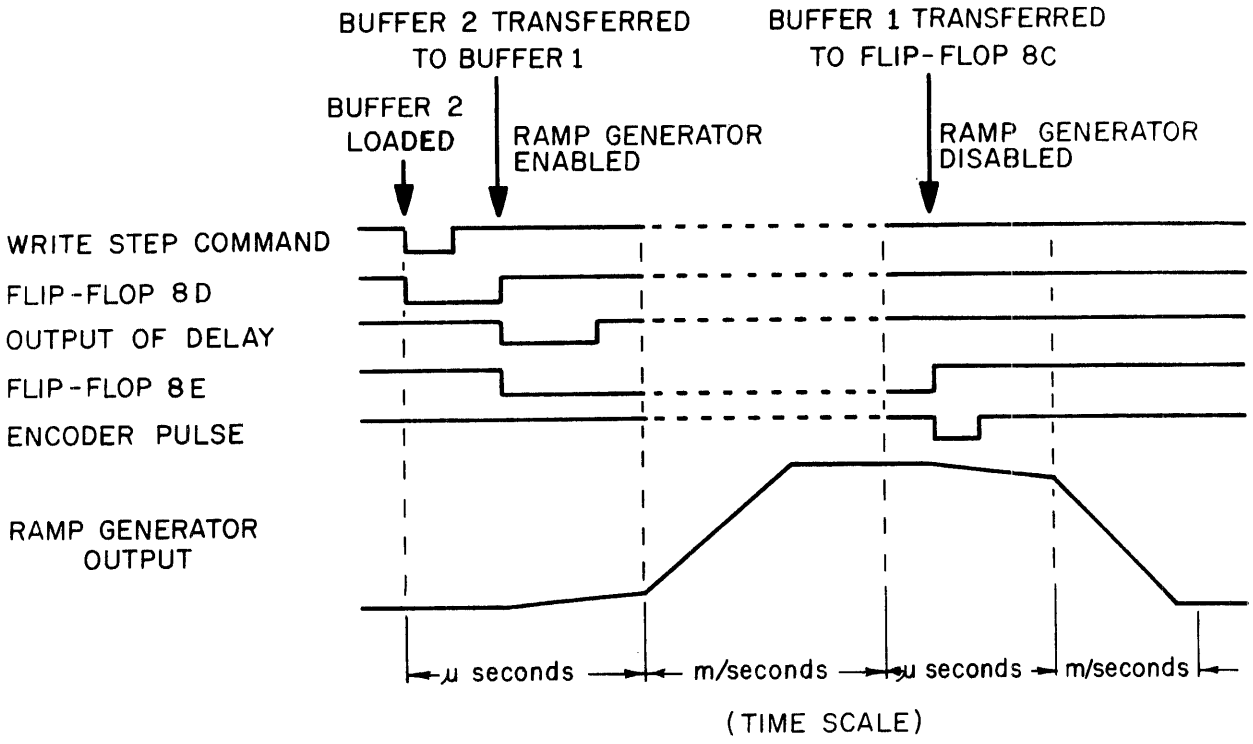


FIGURE 4-9. CONTROL WAVEFORMS WHEN RECORDING A SINGLE CHARACTER

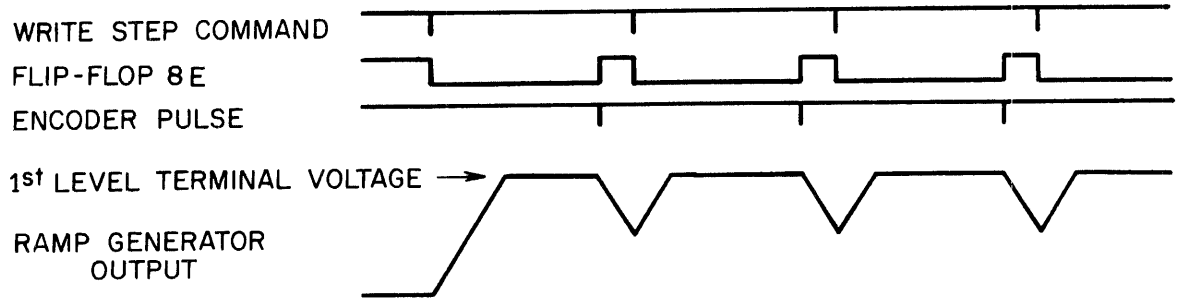


FIGURE 4-10. CONTROL WAVEFORMS WHEN RECORDING CHARACTERS UP TO 400 SPS.

buffer 1 and the $\overline{Q}$ output of the flip-flop enables the STEP FWD ramp generator.

On receipt of the second WRITE STEP command with its associated data, the new data is transferred into buffer 2 which as before toggles if the input data is a '1' and flip-flop 8D is set. However, AND gate 811 is disabled by the $\overline{Q}$ output of flip-flop 8E since an encoder pulse has not been generated to reset flip-flop 8E. Thus flip-flop 8D remains set and the $\overline{Q}$ is used to enable the STEP FWD ramp generator to continue to ramp upwards (at the same rate as before) toward the second terminal voltage which demands the higher tape velocity. When the encoder pulse occurs, the contents of buffer 1 is transferred into the WRITE current generator and flip-flop 8E is reset via gate 812. When flip-flop 8E resets, gate 811 is enabled. The output of gate 806 is delayed 4 usec and then resets flip-flop 8D, sets flip-flop 8E and transfers the status of buffer 2 into buffer 1. Buffer 2 and flip-flop 8D are now able to receive additional data and commands. When flip-flop 8D is reset, the $\overline{Q}$ output disables the second level of the STEP FWD ramp generator which starts ramping down to its normal terminal voltage. The relevant waveforms are illustrated in Figure 4-12. It can be seen that the second level of ramping is enabled whenever flip-flop 8D is set. At low stepping rates, it is only set for 4 usec every command time and the contribution of the second level of ramping is negligible.

As the WRITE STEP command rate approaches 700 sps, flip-flop 8D is set for longer periods of time and the STEP FWD ramp generator has a higher average output which causes a higher-average tape speed consistant

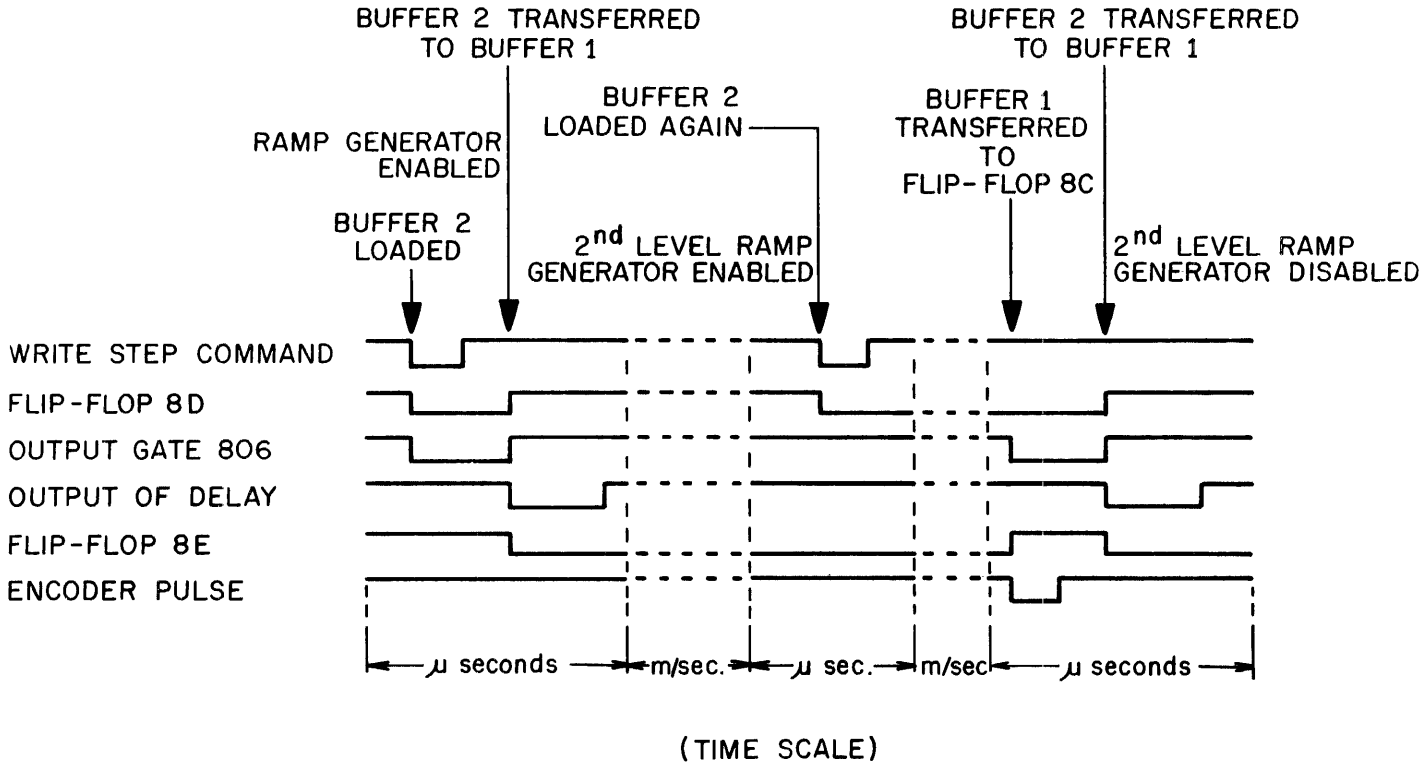


FIGURE 4-11. CONTROL WAVEFORMS - 400 SPS TO 700 SPS.

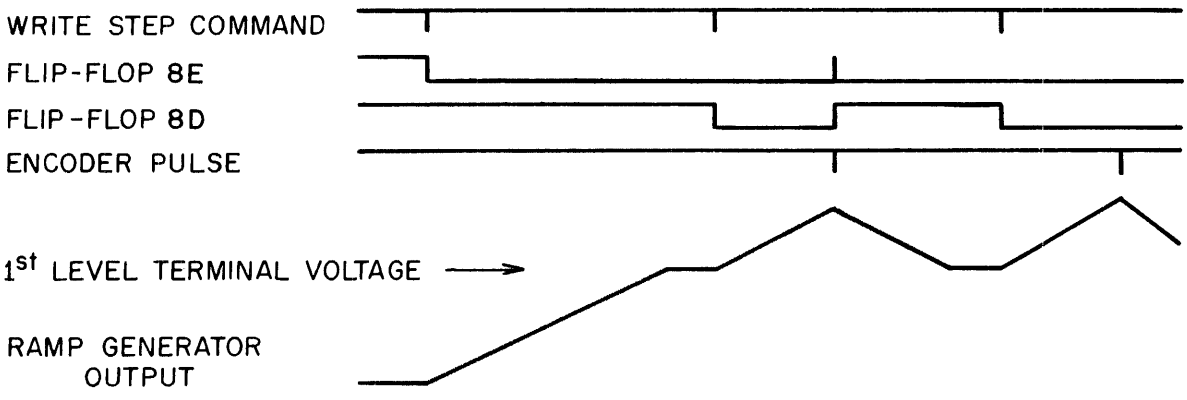


FIGURE 4-12. CONTROL AND VELOCITY WAVEFORMS FOR 400 SPS TO 700 SPS OPERATION

with the higher recording rates.

4.2.4.5 Error Checking Systems.

4.2.4.5.1 General. In any information recording system, it is desirable to provide safeguards against loss of information during the recording process and also to provide error detection and correction during the subsequent reproducing process.

The most satisfactory way to check the recording process is to read back the recorded information and check it against the data source before discarding the original data. Alternatively the parity of the readback information can be checked.

These techniques require a read facility and for efficient operation, a read-after-write system in particular. In the absence of read facilities, an echo check system can be used and this is offered as an option with PEC recorders.

In order to provide facilities for error detection and correction during the reproducing process, a parity bit is recorded with each data character and at the end of a record, CYCLIC REDUNDANCY CHECK characters (CRCC) and/or LONGITUDINAL REDUNDANCY CHECK characters (LRCC) are recorded. Parity, LRCC, and where appropriate, CRCC generation facilities are provided in all PEC Incremental Write Transports. An additional system safeguard, Motion Check, is also provided.

These error checking systems are now briefly described.

4.2.4.5.2 Echo Check System. Information is recorded in the NRZI mode i.e., reversal of magnetization on the tape occurs for each '1' recorded. This is accomplished by feeding current into either one or the other half of a center-tapped head. Whenever current is switched off in one half of the head (and switched on in the other half) the voltage at the end of that half swings below the return voltage of the center tap due to the inductive nature of the recording head. The negative swings from each half of the head associated with a particular channel are used to generate pulses. These pulses trigger a flip-flop associated with that channel. The outputs of these flip-flops are fed to a parity-tree check system whose output is interrogated at the appropriate time. If the parity is incorrect a flip-flop is set and the output, ECHO CHECK ERROR (ECE), is fed to the interface. This flip-flop will remain set until re-set by a customer. The occurrence of an ECE signal does not cause any internal action in the transport. The circuitry and control logic associated with the ECHO CHECK system is fully described in Paragraph 4.3.11.

4.2.4.5.3 Error Correction Characters. In addition to the usual parity bit associated with each character, additional error detection and correction characters are provided. In a 7-track system one LRCC is written at the end of a record. This character is used to give a longitudinal parity check on each track and is such that the total number of '1's (i.e., transitions) in any one track including the LRCC bit is even.

1-B

In a 9-track system two check characters are written at the end of each record. The first character is the CRCC; the second character is an LRCC similar to the one used in 7-track operation. The use of a CRCC is the basis of an error correction technique which employs a modified cyclic code in conjunction with the character parity to correct error bursts of unlimited length in any one of the 9 tracks. Errors involving more than one track with the same record are detected but cannot be corrected.

The CRCC is generated in the CRC Register (CRCR) (see Paragraph 4.3.12) according to the following rules:

- All data characters in the record are added to the contents of the CRCR without carry. Each data bit is exclusive OR'd to the corresponding bit of the CRCR.
- Between additions the CRCR is shifted one position (CRCP to CRCO, etc., and CRC7 to CRCP).
- If shifting will cause CRCP to become a '1', the bits being shifted into positions CRC2, CRC3, CRC4, and CRC5 are inverted.
- After the last data character has been added, the CRCR is shifted once more in accordance with the first two steps.
- The contents of all the CRCR positions except CRC2 and CRC4 are inverted and the resultant character written on the tape.

4.2.4.5.4 Motion Check. This signal provides an indication that

the capstan has rotated through the appropriate angle as a result of a WRITE STEP command.

The encoder waveform, amplifier and 'squared' by a Schmitt Trigger Circuit, is fed to the interface. Each transition (whether positive or negative) indicates that one step has been accomplished. Due to the buffering system, more than one command may be issued before a transition occurs in the MOTION CHECK signal. Thus, a one-to-one correspondence of WRITE STEP commands and MOTION CHECK transitions may not exist but the total number of transitions will equal the total number of commands.

4.2.4.6 Insertion of IBM Compatible Gaps and Special Characters. Two types of gaps are used when writing IBM compatible tapes. These are the INTER-RECORD GAP and the FILE GAP.

4.2.4.6.1 INTER-RECORD GAP. An INTER-RECORD GAP (IRG) is used to separate groups of characters which constitute a record of information. Records may be of variable length. Since in many applications data may be lost unless auxiliary buffering is used during the IRG generation, a fast gapping time is required.

In a 7-track system, the IRG control generates a standard 3/4 inch IBM-compatible IRG in 60 msec (See Figure 4-13). This is accomplished by accelerating the tape to 25 ips in a controlled manner, running at this speed for 12 msec and then decelerating to zero velocity. The acceleration and deceleration time of the tape is approximately 18 msec.

When an IRG is inserted, an LRCC is written four character spaces after the last data character of the record as shown in Figure 4-13.

In a 9-track system, the IRG control generates a standard 0.6 inch IBM-compatible IRG in 60 msec. This is accomplished by accelerating the tape to 25 ips in a controlled manner, running at this speed for 6 msec and then decelerating to zero velocity. The acceleration and deceleration time of the tape is approximately 18 msec. When an IRG is inserted, a CRCC is written four character spaces after the last data character of the record. This is followed, after a further four-character spaces, by the LRCC as shown in Figure 4-14.

4.2.4.6.2 FILE GAP. A FILE GAP is used to separate files of information and is identified by a special character on the tape. In general, the number of different files on a single reel of tape will be small and the FILE GAP time is not critical. The FILE GAP control is designed to generate a standard IBM-compatible FILE GAP with appropriate identification.

In a 7-track system the sequence is writing an LRCC for the last record, moving approximately 3.8 inches, writing the file mark character (binary 15) and then inserting an IRG. This IRG contains the LRCC associated with the file mark character (See Figure 4-15). The first 3.8 inches displacement of the file mark is carried out at the tape velocity in approximately 35 msec.

In a 9-track system the sequence is writing the CRCC and the LRCC

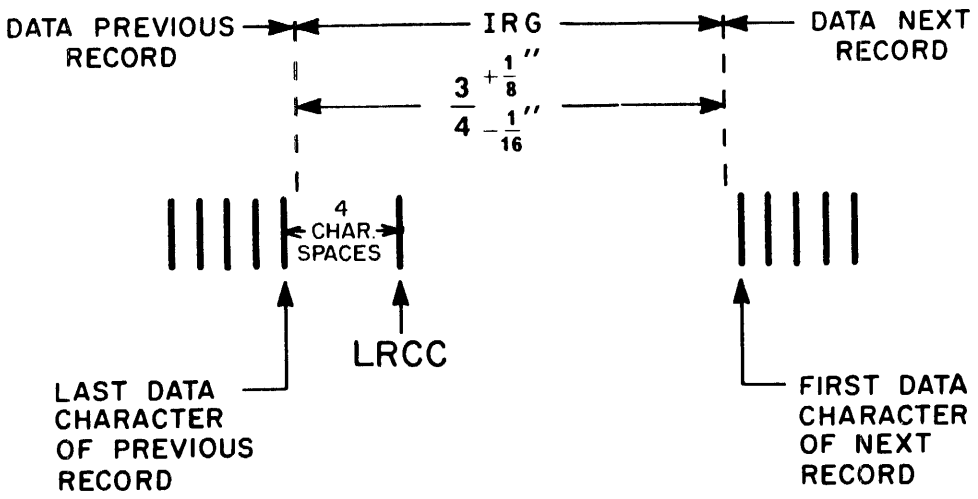


FIGURE 4-13. IRG FORMAT - 7 TRACK

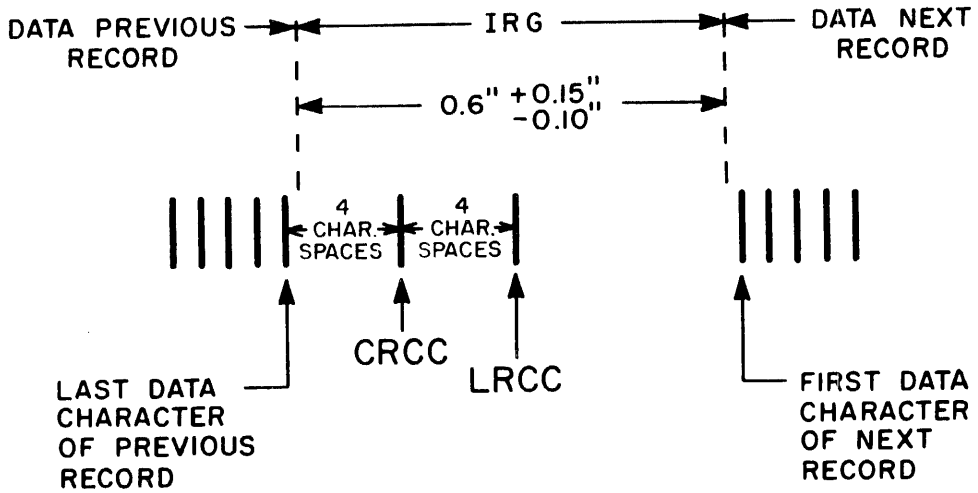


FIGURE 4-14. IRG FORMAT - 9 TRACK

for the last record, moving approximately 3.8 inches, writing the file mark character (a '1' digit in data channels 3, 6, and 7) and then inserting an IRG. This IRG contains the LRCC associated with the file mark character but no CRCC is written. The first 3.8 inches displacement of the file mark is carried out at the tape velocity of 12 ips with the tape accelerating to and decelerating from this velocity in approximately 35 msec, as illustrated in Figure 4-16.

4.2.4.6.3 IRG Sequence. Assuming that transport has been brought to operational status, the IRG sequence is as follows:

- An IRG command is generated. (This may only be accomplished remotely.)
- The TRANSPORT READY signal goes false, GIP signal goes true and the IRG ramp generator is enabled.
- In a 7-track system, four character spaces after IRG initiation (determined by counting four encoder pulses), the LRCC for the previous record is recorded.

  In a 9-track system, four character spaces after IRG initiation (determined by counting four encoder pulses), the CRCC for the previous record is recorded. After a further four character spaces (determined by counting four more encoder pulses, i.e., 8 total), the LRCC is recorded.
- The tape finishes accelerating to its terminal velocity and continues to move at this speed for a period defined by the IRG Single Shot (IRGSS).

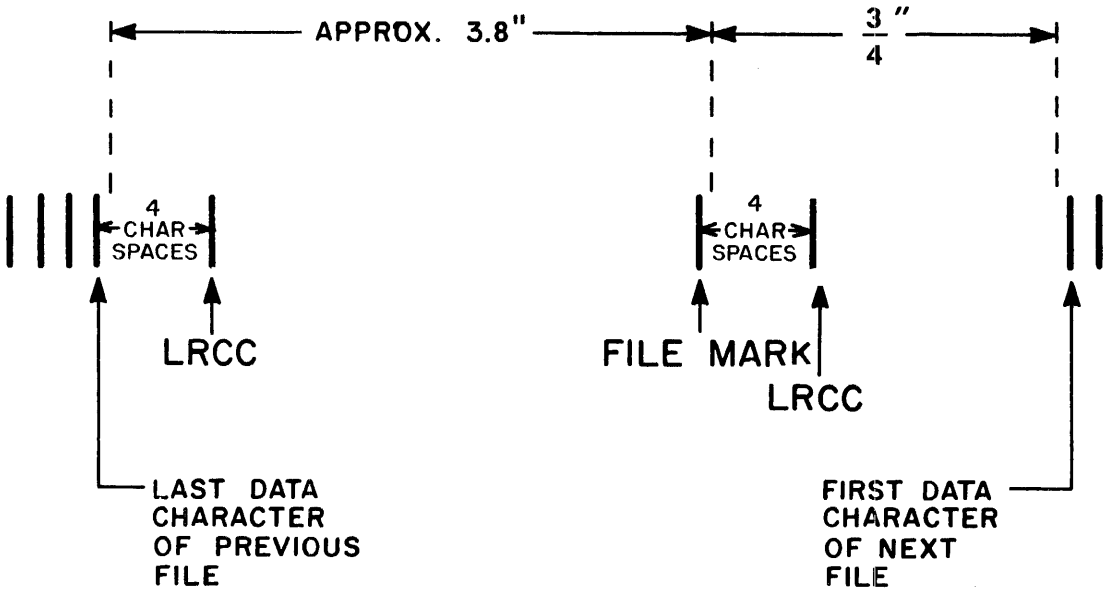


FIGURE 4-15. FILE GAP FORMAT - 7 TRACK

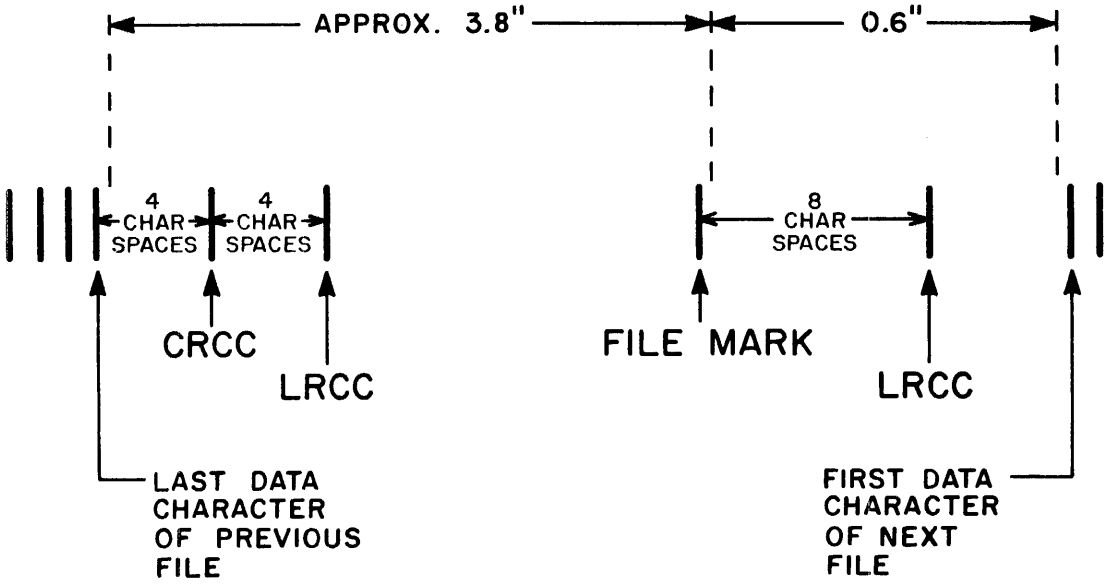


FIGURE 4-16. FILE GAP FORMAT - 9 TRACK

- At the end of this period, the IRGSS is reset, the IRG ramp generator is disabled, and the tape decelerates. When the velocity reduces to a value that enables the MPD circuit (approximately 2000 sps), the CLEAN-UP sequence is entered. This sequence is to ensure proper positioning of the optical shaft encoder prior to additional data recording. The CLEAN-UP sequence consists of enabling the STEP FORWARD ramp generator which adds a velocity component equivalent to 400 sps to the tape velocity at this time, and counting four encoder pulses.

  The velocity at which the MPD is enabled and the CLEAN-UP sequence entered is chosen so that under the worst tolerance conditions, the net tape velocity is equal to the equivalent of 400 sps by the time the fourth encoder pulse is detected (i.e., the velocity component due to the IRG ramp generator is zero).

  On the fourth pulse, the STEP FORWARD ramp generator is disabled and the tape decelerates such that the encoder comes to rest half way between two angular indications. The total distances moved is 3/4 (+1/8, -1/16) inch for a 7-track system and 0.6 (+0.15, -0.10) inch for a 9-track system.

- The GIP signal becomes false and the TRANSPORT READY signal becomes true. The transport is now ready to receive additional data.

4.2.4.6.4 FILE GAP Sequence. The sequence of events required to perform a FILE GAP depends upon whether the gap is initiated remotely in the

interface or manually by the FILE GAP control.

4.2.4.6.4.1 FILE GAP Sequence - Remote Initiation. In this case it is assumed that the remote control recognizes the requirement for the generation of a FILE GAP in lieu of an IRG. Under these circumstances the FILE GAP sequence must cause the check characters for the previous record to be written. The appropriate sequence is as follows:

- The TRANSPORT READY signal goes false, the GIP goes true and the FAST FWD ramp generator is enabled causing the tape to accelerate to 12 ips.
- a. In a 7-track system, four character spaces after initiation of the FILE GAP (determined by counting four encoder pulses), the LRCC for the previous record is recorded on the tape.

  b. In a 9-track system, four character spaces after initiation of the FILE GAP (determined by counting four encoder pulses), the CRCC for the previous record is recorded on tape. After a further four character spaces (determined by counting four more encoder pulses, i.e., 8 total), the LRCC is recorded.
- The tape continues to move at 12 ips for a period defined by the FGSS.
- When the FGSS resets, the FAST FWD ramp generator is disabled, the tape decelerates, and during the ensuing time the rate of pulses from the encoder is monitored by the MPD. When the rate

drops below the appropriate value the CLEAN-UP sequence is entered as described in Paragraph 4.2.4.6.3, and the tape comes to rest such that the encoder is approximately half way between angular indications. The total distance moved up to this point is approximately 3.8 inches.

- At the end of the FILE GAP CLEAN-UP sequence, the IRG sequence is automatically entered, the GIP signal remains true and the TRANSPORT READY signal remains false. At this point the sequence of events is the same as that described in Paragraph 4.2.4.6.3 (except that in the case of 9-track operation no CRCC is written). In a 7-track system this results in the writing of the LRCC for the file mark four characters after the file mark. This is followed by a further tape movement of 0.75 inch. In a 9-track system, the LRCC is written eight character spaces after the file mark followed by a tape movement of 0.60 inch.

4.2.4.6.4.2 FILE GAP sequence - Manual Initiation. At times it is

convenient to insert a FILE GAP manually. For example; at the end of a data collection. In this case it is assumed that records together with IRG's have been written automatically, and that the last record has also been terminated with an IRG which include the check characters for that record. The FILE GAP sequence in this case after the FILE GAP control has been depressed is identical to that in Paragraph 4.2.4.6.4.1 except that the third item is omitted.

4.2.4.7 Detailed Operation of Gapping Control Logic. Figure 4-17 is a block diagram of the gapping control logic.

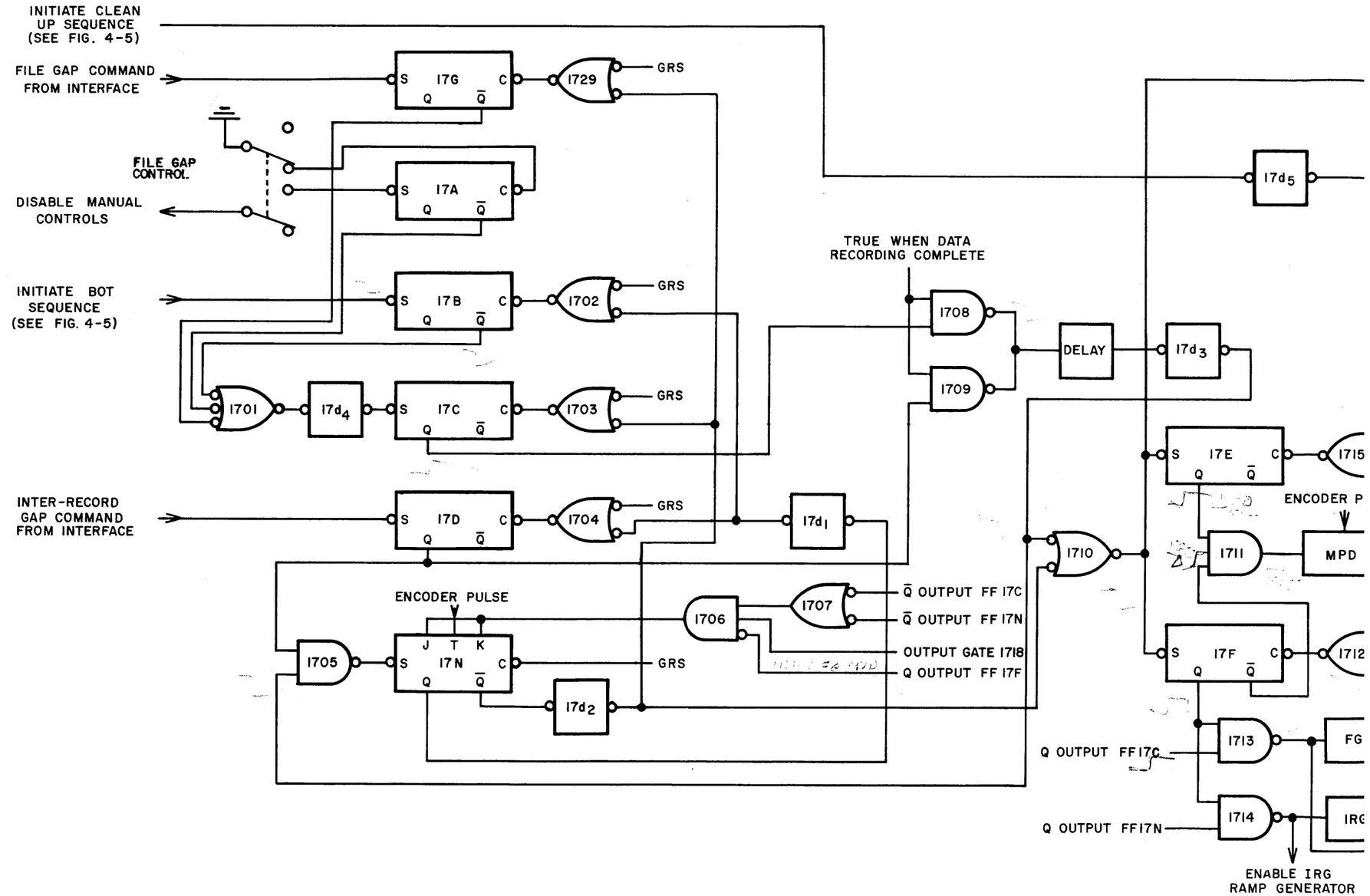
Flip-flops 17A, 17B, 17C, 17D, 17E and 17G are set and reset type flip-flops and 17H, 17J, 17K, 17L, 17M and 17N are J-K type flip-flops.

Two operating modes are provided: The first is for 7-track systems in which only a LRCC is written. In this case, the $\overline{Q}$ output of flip-flop 17M is wired to be permanently false (J203 pin 13 to ground) and this flip-flop plays no part in the operation.

The second mode is for 9-track systems in which both CRCC and LRCC are written and flip-flops 17M is operational.

4.2.4.7.1 INTER-RECORD GAP Sequence - 7-Track. Figure 4-18 is the relevant timing diagram.

The sequence is initiated by setting flip-flop 17D via the interface (plot 1). The Q output of flip-flop 17D (plot 2) enables one input of AND gate 1709 and awaits the completion of data recording. (This arises since, as explained in Paragraph 4.2.4.4 data may be stored in the information buffer. Thus


INITIATE CLEAN UP SEQUENCE (SEE FIG. 4-5)
FILE GAP COMMAND FROM INTERFACE
FILE GAP CONTROL
DISABLE MANUAL CONTROLS
INITIATE BOT SEQUENCE (SEE FIG. 4-5)
INTER-RECORD GAP COMMAND FROM INTERFACE
ENCODER PULSE
17G
17A
17B
17C
17D
17N
17E
17F
1729
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1718
1701
GRS
TRUE WHEN DATA RECORDING COMPLETE
DELAY
17d1
17d2
17d3
17d4
17d5
Q OUTPUT FF 17C
Q OUTPUT FF 17N
OUTPUT GATE 1718
Q OUTPUT FF 17F
ENCODER P
MPD
FG
IRG
ENABLE IRG RAMP GENERATOR

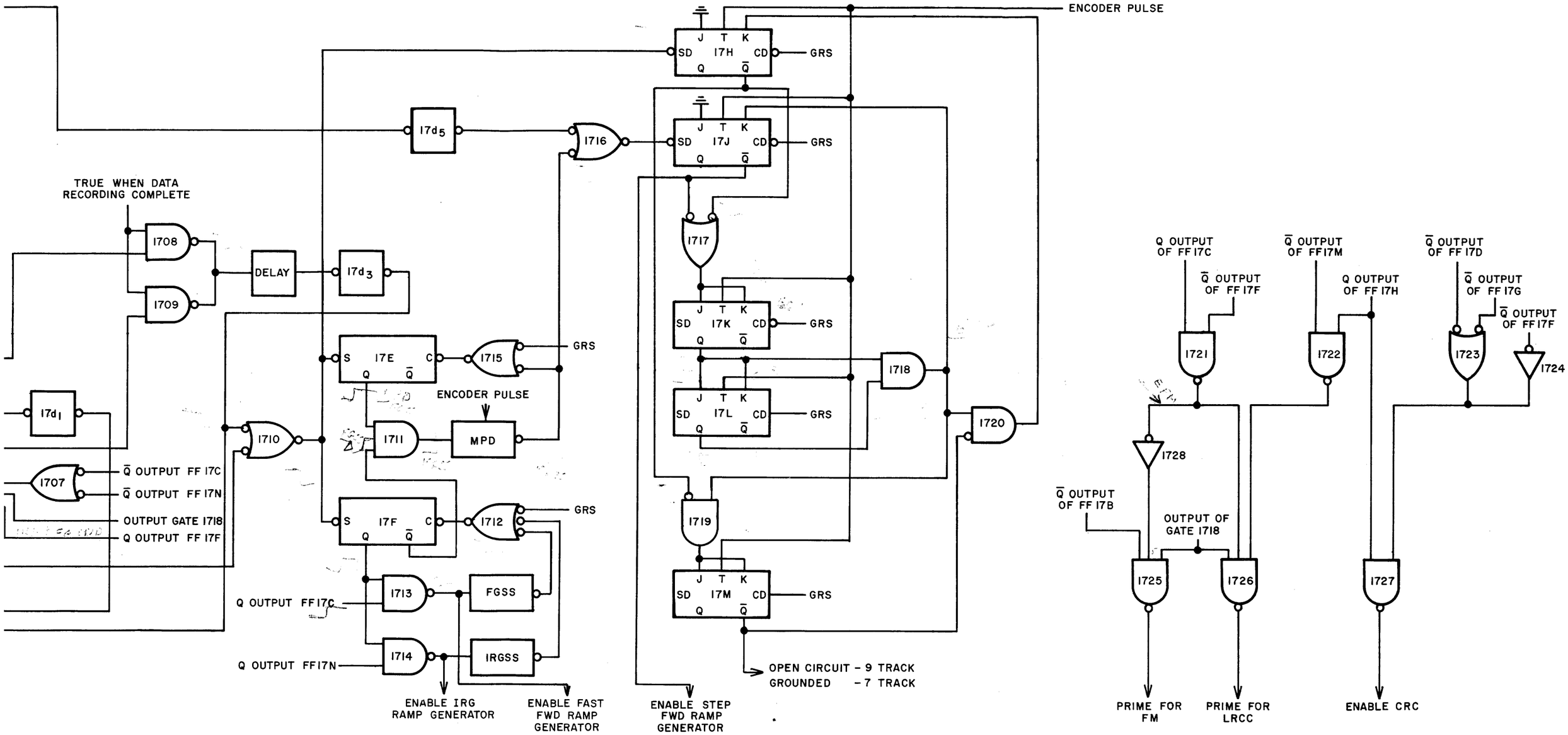


FIGURE 4-17. GAPPING CONTROL LOGIC

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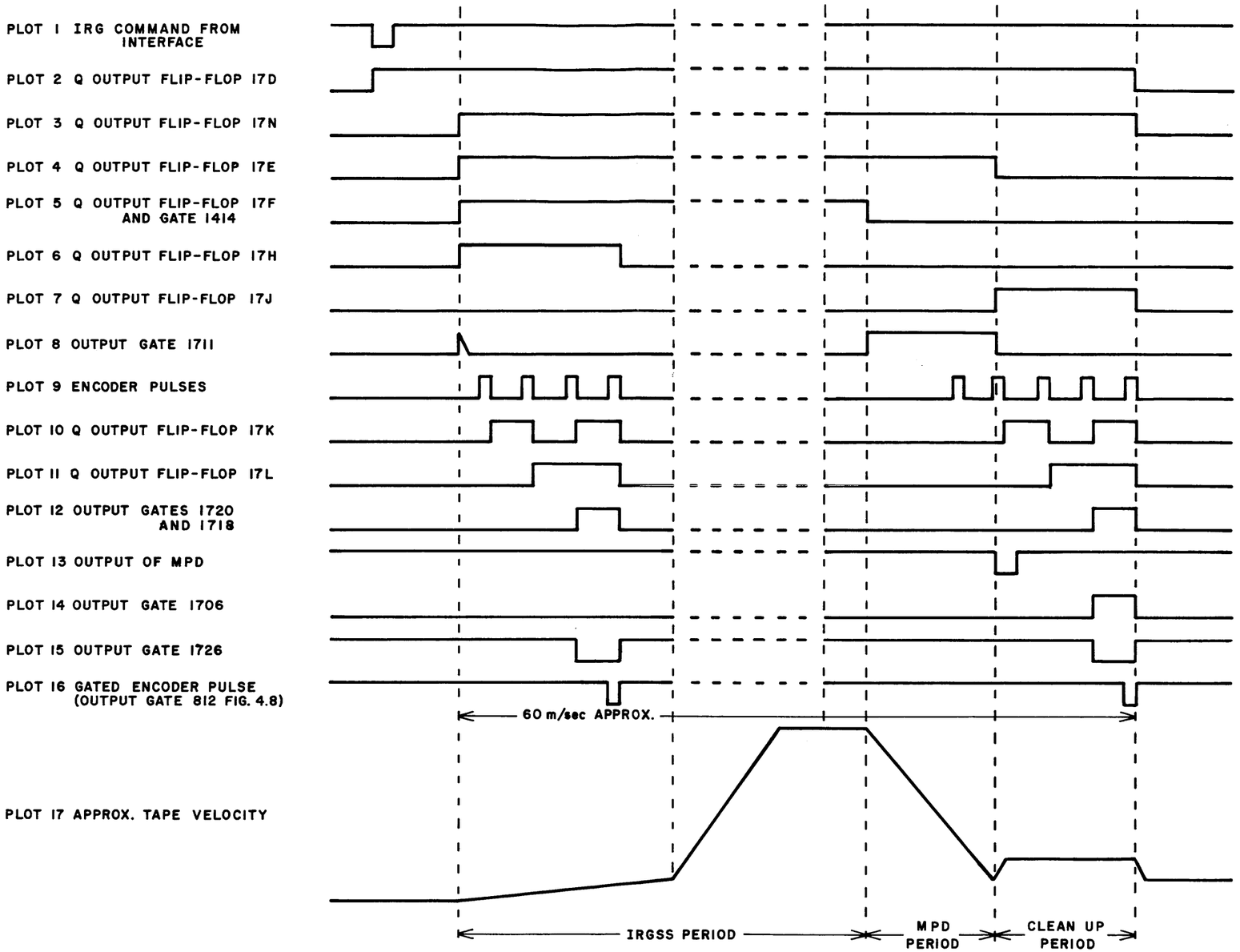

(TIMES NOT TO SCALE)

FIGURE 4-18.
IRG SEQUENCE TIMING DIAGRAM - 7 TRACK

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if an IRG command is given immediately after the last WRITE STEP command for that record, the IRG command must not be acted upon until the last information character has been recorded.)

After all the data has been recorded AND gate 1709 is enabled and the output is delayed and then differentiated. The differentiator-17d3 output pulse initiates the following sequence:

- The pulse output sets the following flip-flops.
  a. 17N via AND gate 1705 (plot 3).
  b. 17E, 17F and 17H via OR gate 1710 (plots 4, 5 & 6).
- The output of gate 1714 (plot 5) enables the INTER-RECORD GAP ramp generator causing the tape to be accelerated toward 25 ips (plot 17).
- Motion of the capstan causes encoder pulses to be generated (plot 9) and these are fed to the toggle inputs of the counter (flip-flops 17K, 17L and 17M) which is enabled by flip-flop 17H via OR gate 1717. The Q outputs of flip-flops 17K, and 17L are shown in plots 10 and 11 and the output of gate 1720 (and 1718) in plot 12. The output of gate 1720, when high, enables the 'K' input of flip-flop 17H so that on the fourth encoder pulse this flip-flop is reset (remember FF17M output is permanently low).
  Since an IRG is being generated, the Q output of flip-flop 17C is low and therefore the output of gate 1721 is high. Also, since the $\overline{Q}$ output of flip-flop 17M is low the output of gate 1722 is high.

Two of the inputs of gate 1726 are therefore enabled and the output of gate 1726, as shown in plot 15, will therefore follow the output of gate 1718.

This output (PRIME FOR LRCC) is used to reset all the buffer 1 flip-flops in the recording electronics (see Figure 4-8) using the leading edge.

The output of gate 1718 is also used to permit one encoder pulse when it is true (plot 16) which transfers the contents of buffer 1 (which has just been reset by the PRIME FOR LRCC signal) to the WRITE current generator.

In this way, the LRCC is written four character spaces after the last information character such that the total number of magnetization transitions in any one tape track is EVEN. This follows since the record starts and finishes with the WRITE current generators reset.

- The tape accelerates to 25 ips and continues to move at this speed for a period defined by the IRGSS. At the end of this period, flip-flop 17F is reset (plot 5) via OR gate 1712 enabling gate 1711 (plot 8). This enables the MPD which monitors the encoder pulse rate as the tape decelerates. When this rate drops below 400 pulses/second, a pulse is generated by the MPD circuit (plot 13).
- This initiates the CLEAN-UP sequence by:

  a. Resetting flip-flop 17E via OR gate 1715.

b. Setting flip-flop 17J (plot 7) via OR gate 1716 which enables the counter via OR gate 1717. The Q output of flip-flop 17J enables the STEP FORWARD ramp generator.

The tape continues to move until four encoder pulses have been counted. The output of gate 1718 (plot 12) then enables the 'K' input of flip-flop 17J and this flip-flop is reset on the trailing edge of the fourth encoder pulse. The STEP FORWARD ramp generator is disabled and the tape comes to rest in approximately half-a-character-space.

In addition, the output of gate 1706 becomes true as shown in plot 14 and flip-flop 17N toggles to the reset state (plot 3). The Q output of flip-flop 17N is differentiated by differentiator 17d1 and resets flip-flop 17D (plot 2).

Note, that the output of gate 812 goes true again during the CLEAN-UP sequence and another encoder pulse is permitted (plot 16). However, since the WRITE flip-flops are already reset no further action takes place.

4.2.4.7.2 INTER-RECORD GAP Sequence - 9-Track. Figure 4-19 is the relevant timing diagram.

The sequence is initiated as already described by setting flip-flop 17D via the interface (plot 1). The Q output of flip-flop 17D (plot 2) enables one input of AND gate 1709 and awaits the completion of data recording as before.

After all the data has been recorded AND gate 1709 is enabled and the output is delayed and then differentiated. The differentiator-17d3 output pulse initiates the following sequence:

- The pulse output sets the following flip-flops.

  a. 17N via AND gate 1705 (plot 3).

  b. 17E, 17F and 17H via OR gate 1710 (plots 4,5 and 6).

- The output of gate 1714 (plot 5) enables the INTER-RECORD GAP ramp generator causing the tape to be accelerated toward 25 ips (plot 17).

- Motion of the capstan causes encoder pulses to be generated (plot 9) and these pulses are fed to the toggle inputs of the counter (flip-flops 17K, 17L and 17M) which is enabled by flip-flop 17H via OR gate 1717. The Q outputs of flip-flops 17K, 17L and 17M are shown in plots 10, 11 and 12 and the outputs of gates 1718 and 1720 in plots 13 and 14.

  The output of gate 1720 enables the 'K' input of flip-flop 17H so that on the eighth encoder pulse, this flip-flop is reset.

  Now, the $\overline{Q}$ outputs of flip-flops 17D and 17F are low so that the outputs of gate 1723 and invertor 1724 are high and one input of gate 1727 is enabled. The output of gate 1727 is thus an inverted version of flip-flop 17H and goes low when flip-flop 17H is high. The leading edge of this output (ENABLE CRC) is used to initiate the CRCC control circuits (see Paragraph 4.3.12) causing the CRCC which has been generated in the CRCR to be loaded into

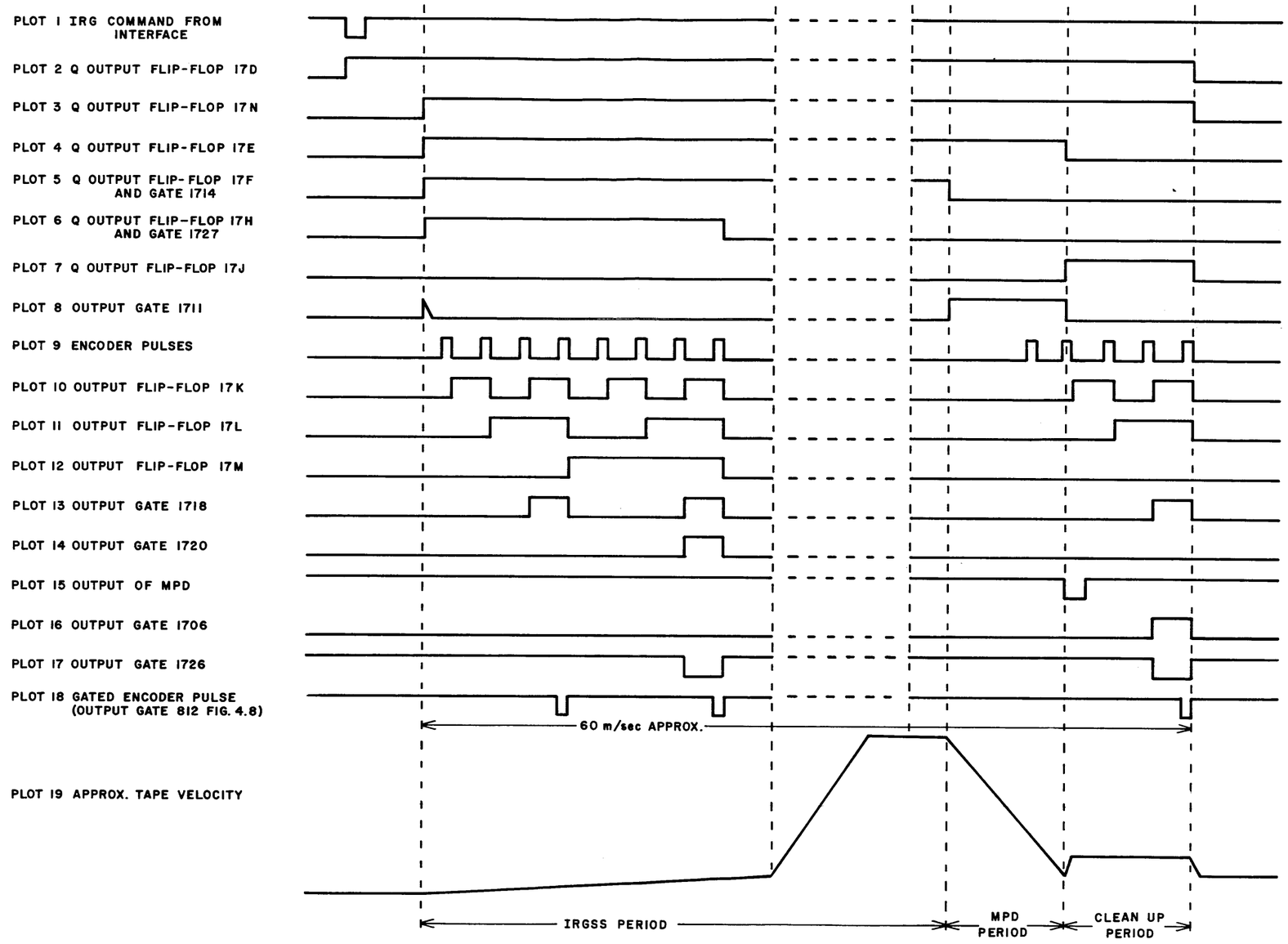

FIGURE 4-19.
IRG SEQUENCE TIMING DIAGRAM - 9 TRACK

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buffer 2 and then into buffer 1 in the recording electronics.

The output of gate 1718 goes true after four encoder pulses and again after eight encoder pulses (plot 13). This output is used to gate-out appropriate encoder pulses (plot 18). The first of these is the fourth pulse which transfers the contents of buffer 1 (containing the CRCC) to the WRITE CURRENT generator causing this character to be written.

Since an IRG is being generated, the Q output of flip-flop 17C is low so that the output of gate 1721 is high. After the fourth encoder pulse has occurred, the $\overline{Q}$ output of flip-flop 17M goes low (and the Q output true, plot 12) causing the output gate 1722 to go high. The output of gate 1726 will therefore be as shown in plot 17. This output (PRIME FOR LRCC) is used to reset all buffer 1 flip-flops in the recording electronics (see Figure 4-8) using the leading edge.

The second time the output of gate 1718 goes true it gates-out another encoder pulse which transfers the content of buffer 1 flip-flops (which have just been reset) to the WRITE current generator.

In this way, the CRCC is written four character spaces after the last information character of the record and the LRCC is written eight character spaces after the last information character of the record such that the total number of magnetization transistions in

any one track on the tape is EVEN. This follows since the record starts and finishes with the WRITE current generators reset.

- The tape accelerates to 25 ips and continues to move at this speed for a period defined by the IRGSS. At the end of this period, flip-flop 17F is reset (plot 5) via OR gate 1712 enabling gate 1711 (plot 8) and thus enabling the MPD which monitors the encoder pulse rate as the tape decelerates. When the rate drops below the appropriate value as described in Paragraph 4.2.4.6.3, a pulse is generated by the MPD circuit (plot 15).

- This initiates the CLEAN-UP sequence by:

  a. Resetting flip-flop 17E via OR gate 1715.

  b. Setting flip-flop 17J (plot 7) via OR gate 1716 which enables the counter via OR gate 1717. The $\overline{Q}$ output of flip-flop 17J enables the STEP FWD ramp generator.

  The tape continues to move until four encoder pulses have been counted. The output of gate 1718 then enables the 'K' input of flip-flop 17J and this flip-flop is reset on the fourth encoder pulse. The STEP FWD ramp generator is disabled and the tape comes to rest in approximately half-a-character-space.

In addition, the output of gate 1706 becomes true as shown in plot 16 and flip-flop 17N toggles to the reset state (plot 3). The Q output of flip-flop 17N is differentiated by differentiator 17d1 and resets flip-flop 17D (plot 2).

Note that the output of gate 1718 goes true again during the CLEAN-UP sequence and a third encoder pulse permitted (plot 18). However, since the WRITE flip-flops are already reset, no further action takes place.

4.2.4.7.3 FILE GAP Sequence - 7-Track. Figure 4-20 is the relevant timing diagram.

The FILE GAP sequence can be initiated either via the interface or manually using the FILE GAP control.

4.2.4.7.3.1 Remote Initiation. A pulse input from the interface sets flip-flop 17G. The $\overline{Q}$ output of flip-flop 17G is transmitted via OR gate 1701 to differentiator 17d4 whose output pulse (plot 1) sets flip-flop 17C. The Q output of flip-flop 17C (plot 2) enables one input of AND gate 1708 where it awaits the completion of data recording.

At the end of data recording AND gate 1708 is enabled and the output of flip-flop 17C is transmitted via the delay to differentiator 17d3. The output pulse initiates the following sequence:

- The pulse output sets flip-flops 17E, 17F and 17H (plots 3, 4 and 5) via OR gate 1710.
- The output of gate 1713 enables the FAST FORWARD ramp generator causing the tape to be accelerated towards 12 ips (plot 19).
- Motion of the capstan causes encoder pulses to be generated (plot 8) and these are fed to the toggle inputs of the counter flip-

flops 17K, 17L and 17M, which are enabled by flip-flop 17H via OR gate 1717, The Q outputs of flip-flops 17K and 17L are shown in plots 9 and 10 and the output of gate 1720 (and 1718) in plot 11. The output of gate 1720, when high, enables the 'K' input of flip-flop 17H so that on the fourth encoder pulse, this flip-flop is reset (remember flip-flop 17M output is permanently low in a 7-track mode).

Since flip-flop 17F has been previously set, the $\overline{Q}$ output is low and the output of gate 1721 is high. And, since the $\overline{Q}$ output of flip-flop 17M is low the output of gate 1722 is high. Two of the inputs of gate 1726 are therefore enabled and the output of gate 1726 (plot 14) will therefore follow the output of gate 1718 as shown in plot 11.

This output (PRIME FOR LRCC) is used to reset all buffer 1 flip-flops in the recording electronics (see Figure 4-8) using the leading edge.

The output of gate 1718 is also used to permit one encoder pulse when it is true (plot 15) which transfers the contents of buffer 1 (which has just been reset by the PRIME FOR LRCC signal) to the WRITE current generator. In this way the LRCC is written four character spaces after the last information character such that the total number of magnetization transistions in any one channel on the tape is EVEN. This follows since the record starts and

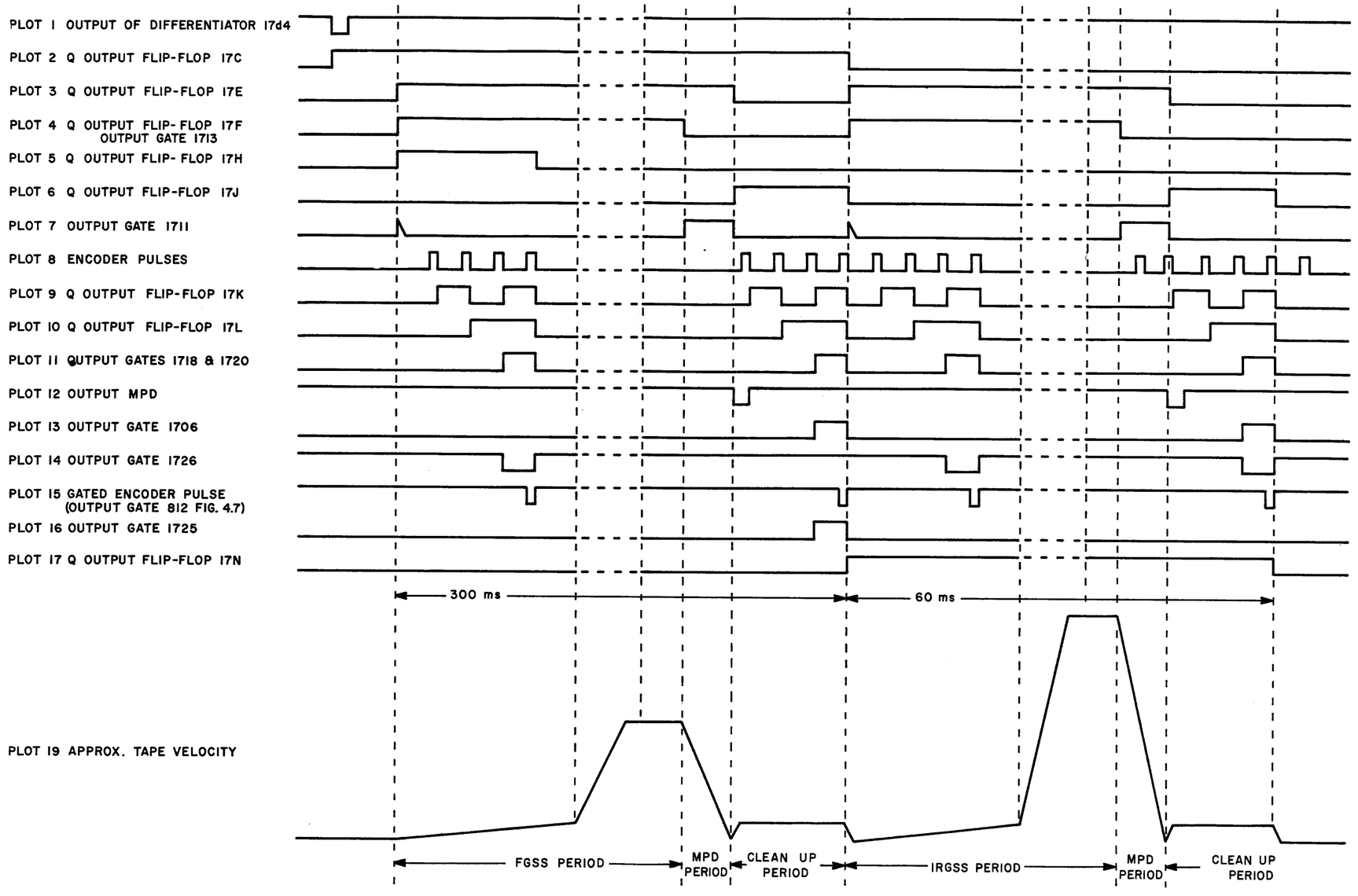

FIGURE 4-20.
FILE GAP SEQUENCE TIMING DIAGRAM - 7 TRACK

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finishes with the WRITE current generators reset.

- The tape accelerates to 12 ips and continues to move at this speed for a period defined by the FGSS. At the end of this period flip-flop 17F is reset (plot 4) via OR gate 1712 enabling gate 1711 (plot 7) and thus enabling the MPD which monitors the encoder pulse rate as the tape decelerates. When the rate drops below the appropriate value as described in Paragraph 4.2.4.6.3, a pulse is generated by the MPD circuit (plot 12).

- The MPD pulse initiates the CLEAN-UP sequence by:

  a. Resetting flip-flop 17E via OR gate 1715.

  b. Setting flip-flop 17J (plot 6) via OR gate 1716, which enables the counter via OR gate 1717 and also enables the STEP FWD ramp generator.

  The tape continues to move until four encoder pulses have been counted. Since flip-flop 17F is now reset the flip-flop 17C is still set, the output of gate 1721 is low; gate 1726 is disabled and one input of gate 1725 enabled via 1728. Also the $\overline{Q}$ output of flip-flop 17B is high (not in a BOT sequence) so that the output of gate 1725 is as shown in plot 17. This output (PRIME FOR FM) is used to set the relevant buffer-1 flip-flops (channels 0, 1, 2, 3) in the recording electronics (Figure 4-8) using the leading edge. The output of gate 1718 is used to release a second encoder pulse when it is true which transfers the contents of buffer 1 to the WRITE current generator. This writes a FILE MARK.

In addition, the output of gate 1718 enables the 'K' input of flip-flop 17J and this flip-flop is reset on the fourth encoder pulse (plot 6). Also the output of gate 1706 (plot 13) becomes true and flip-flop 17N toggles to the set state (plot 17). The $\overline{Q}$ output of flip-flop 17N is differentiated by differentiator 17d2 and the output pulse of the differentiator initiates the following sequence:

- a. Resets flip-flop 17C (plot 2)

  b. Sets flip-flop 17E via OR gate 1710 (plot 3)

  c. Sets flip-flop 17F via OR gate 1710 (plot 4)

  d. Sets flip-flop 17H via OR gate 1710 (plot 5)

- The output of gate 1714 enables the INTER-RECORD GAP ramp generator causing the tape to be accelerated toward 25 ips (plot 19).

- Motion of the capstan causes encoder pulses to be generated (plot 8) and these are fed to the toggle inputs of the counter (flip-flops 17K, 17L and 17M) which is enabled by flip-flop 17H via OR gate 1717. The Q outputs of flip-flops 17K, and 17L are shown in plots 9 and 10 and the output of gate 1720 (and 1718) in plot 11. The output of gate 1720, when high, enables the 'K' input of flip-flop 17H so that on the fourth encoder pulse this flip-flop is reset (remember FF17M output is permanently low).

  Since an IRG is being generated, the Q output of flip-flop 17C is low and therefore the output of gate 1721 is high. And, since the $\overline{Q}$ output of flip-flop 17M is low the output of gate 1722 is high.

Two of the inputs of gate 1726 are therefore enabled and the output of gate 1726, as shown in plot 14, will therefore follow the output of gate 1718.

This output (PRIME FOR LRCC) is used to reset all the buffer 1 flip-flops in the recording electronics (see Figure 4-8) using the leading edge.

The output of gate 1718 is also used to permit one encoder pulse when it is true (plot 11) which transfers the contents of buffer 1 (which has just been reset by the PRIME FOR LRCC signal) to the WRITE current generator.

In this way, the LRCC is written four character spaces after the last information character such that the total number of magnetization transitions in any one tape track is EVEN. This follows since the record starts and finishes with the WRITE current generators reset.

- The tape accelerates to 25 ips and continues to move at this speed for a period defined by the IRGSS. At the end of this period, flip-flop 17F is reset (plot 4) via OR gate 1712 enabling gate 1711 (plot 7) enabling the MPD which monitors the encoder pulse rate as the tape decelerates. When the rate drops below the appropriate value as described in Paragraph 4.2.4.6.3, a pulse is generated by the MPD circuit (plot 12).

- This initiates the CLEAN-UP sequence by:

  a. Resetting flip-flop 17E via OR gate 1715.

  b. Setting flip-flop 17J (plot 6) via OR gate 1716 which enables the counter via OR gate 1717. The Q output of flip-flop 17J enables the STEP FORWARD ramp generator.

The tape continues to move until four encoder pulses have been counted. The output of gate 1718 (plot 11) enables the 'K' input of flip-flop 17J and this flip-flop is reset by the fourth encoder pulse. The STEP FWD ramp generator is disabled and the tape comes to rest in approximately half-a-character-space.

In addition, the output of gate 1706 becomes true as shown in plot 13 and flip-flop 17N toggles to the reset state (plot 17). Note that the output of gate 1718 goes true again during the CLEAN-UP sequence and another encoder pulse is permitted (plot 15). However, since the WRITE flip-flops are already reset no further action takes place.

4.2.4.7.3.2 Manual Initiation. When the FILE GAP control is depressed, flip-flop 17A is set. The DPDT FILE GAP control switch is used in conjunction with flip-flop 17A to eliminate the effects of contact bounce. The output of flip-flop 17A is transmitted via OR gate 1701 to differentiator 17d4 whose output pulse sets flip-flop 17C.

The remainder of the sequence is identical with that described in Paragraph 4.2.4.7.3.1.

4.2.4.7.4 FILE GAP Sequence in 9-Track Mode. Figure 4-21 is the relevant timing diagram. The FILE GAP sequence can be initiated either via the interface or manually using the FILE GAP control.

4.2.4.7.4.1 Remote Initiation. A FILE GAP command pulse from the interface sets flip-flop 17G. The $\overline{Q}$ output from flip-flop 17G is transmitted via OR gate 1701 to differentiator 17d4 whose output pulse (plot 1) sets flip-flop 17C. The Q output of flip-flop 17C (plot 2) enables one input of AND gate 1708 where it awaits the completion of data recording.

At the end of data recording AND gate 1708 is enabled and the output of flip-flop 17C is transmitted via the delay to differentiator 17d3. The output pulse initiates the following sequence:

- The pulse output sets flip-flops 17E, 17F and 17H (plots 3, 4, and 5) via OR gate 1710.
- The output of gate 1713 enables the FAST FORWARD ramp generator causing the tape to be accelerated towards 12 ips (plot 21).
- Motion of the capstan causes encoder pulses to be generated (plot 8) and these are fed to the toggle inputs of the counter flip-flops 17K, 17L and 17M which are enabled by flip-flop 17H via OR gate 1717. The Q outputs of flip-flops 17K, 17L and 17M are shown in plots 9, 10, and 11, and the outputs of gates 1718 and 1720 in plots 12 and 13.

The output of gate 1720, when high, enables the 'K' input of flip-flop 17H so that on the eighth encoder pulse, this flip-flop is reset.

The $\overline{Q}$ outputs of flip-flops 17G and 17F are low so that the outputs of gate 1723 and invertor 1724 are high and one input of gate 1727 is enabled. The output of gate 1727 is thus an inverted version of flip-flop 17H and goes low when flip-flop 17H is high. The leading edge of this output (ENABLE CRC) is used to initiate the CRCC control circuits (see Paragraph 4.3.12) causing the CRCC which has been generated in the CRCR to be loaded into buffer 2 and then into buffer 1 in the recording electronics.

The output of gate 1718 goes true after four encoder pulses and again after eight encoder pulses (plot 12). This output is used to gate-out appropriate encoder pulses (plot 17). The first of these is the fourth pulse which transfers the contents of buffer 1 (containing the CRCC) to the WRITE current generator causing this character to be written.

Since flip-flop 17F has previously been set, the $\overline{Q}$ output is low and the output of gate 1721 is high. And, since the $\overline{Q}$ output of flip-flop 17M is low the output of gate 1722 will be high. Two of the inputs of gate 1726 are therefore enabled and the output of gate 1726 will therefore follow the output of gate 1718 as shown in plot 16.

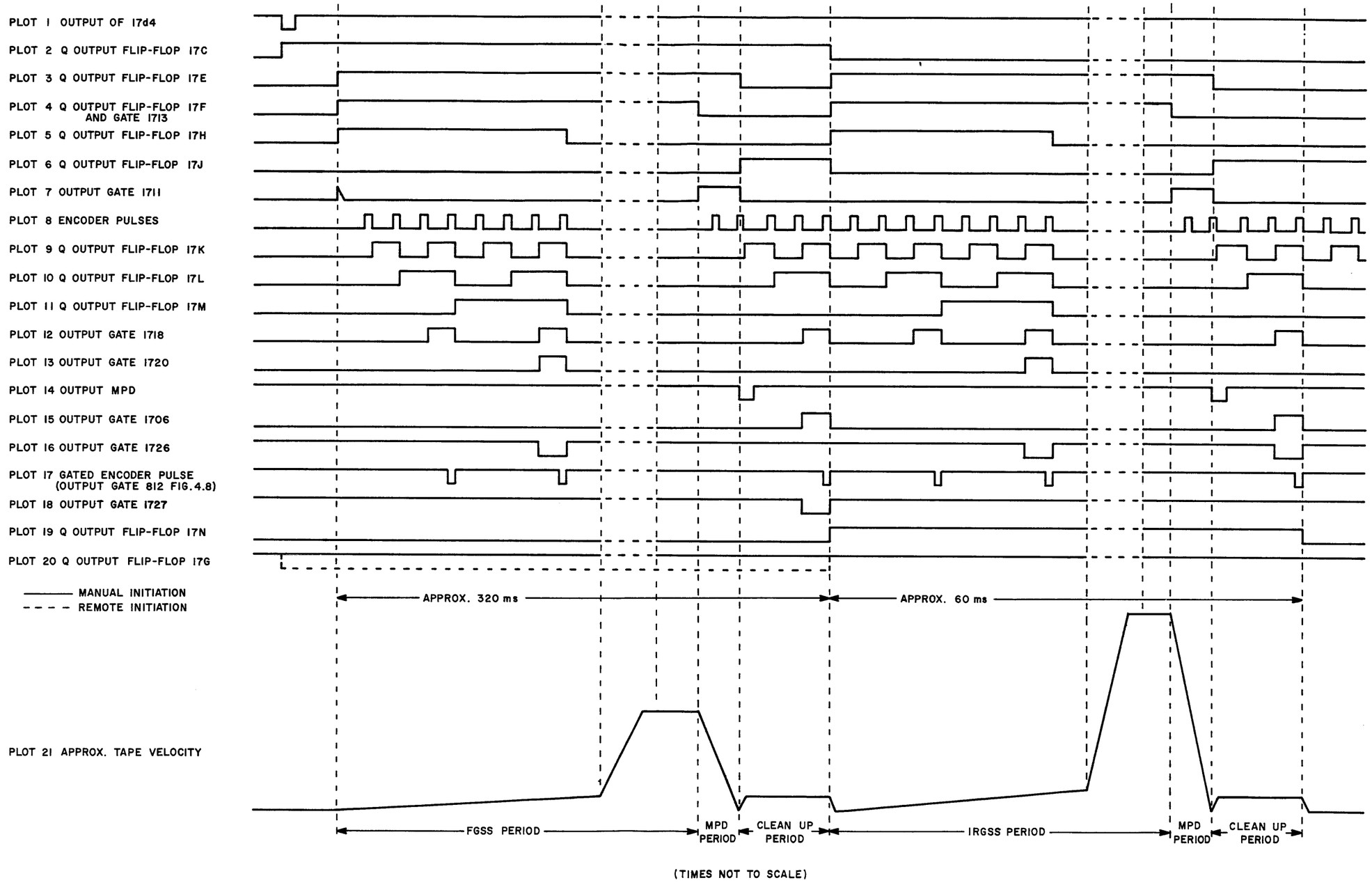

FIGURE 4-21.
FILE GAP SEQUENCE TIMING DIAGRAM - 9 TRACK

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This output (PRIME FOR LRCC) is used to reset all buffer 1 flip-flops in the recording electronics (see Figure 4-8) using the leading edge.

The second time the output of gate 1718 goes true it gates out another encoder pulse which transfers the contents of buffer 1 flip-flops which have just been reset to the WRITE current generator.

In this way, the CRCC is written four character spaces after the last information character record and the LRCC is written eight character spaces after the last information character of the record such that the total number of magnetization transitions in any one track on the tape is EVEN. This follows since the record starts and finishes with the WRITE current generators.

- The tape accelerates to 12 ips and continues to move at this speed for a period defined by the FGSS. At the end of this period, flip-flop 17F (plot 4) is reset via OR gate 1712 enabling gate 1711 (plot 7) and thus enabling the Missing Pulse Detector (MPD) which monitors the encoder pulse rate as the tape decelerates. When this rate drops below 400 pulses/second, a pulse is generated by the MPD circuit (plot 14).
- This pulse initiates the CLEAN-UP sequence by

  a. Resetting flip-flop 17E via OR gate 1715.

  b. Setting flip-flop 17J (plot 6) via OR gate 1716 which enables

the STEP FORWARD ramp generator.

The tape moves until four encoder pulses have been counted. Since flip-flop 17F is now reset and flip-flop 17C is still set, the output of gate 1721 is low, gate 1726 is disabled and one input of gate 1725 enabled via invertor 1728. Also the $\overline{Q}$ output of flip-flip 17B is high (not in a BOT sequence) so that the output of gate 1725 is as shown in plot 18. This output (PRIME FOR FM) is used to set the relevant buffer 1 flip-flops (channels 3, 6, 7) in the recording electronics (Figure 4-8) using the leading edge. The output of gate 1718 is used to release a third encoder pulse (when it is true) which transfers the contents of buffer 1 to the WRITE current generator. This writes a FILE MARK.

In addition, the output of gate 1718 enables the 'K' input of flip-flop 17J and this flip-flop is reset on the fourth encoder pulse (plot 6). Also, the output of gate 1706 (plot 15) becomes true and flip-flop 17N toggles to the set state (plot 19). The $\overline{Q}$ output of flip-flop 17N is differentiated by differentiator 17d2 and the output pulse

- a. Resets flip-flops 17C and 17G (plots 2 and 20).

  b. Sets flip-flop 17E, 17F and 17H via OR gate 1710 (plots 3, 4, and 5).
- The output of gate 1714 enables the INTER-RECORD GAP ramp generator causing the tape to be accelerated towards 25ips (plot 21).

- Motion of the capstan causes the encoder pulses to be generated (plot 8) and these pulses are fed to the toggle inputs of the counter (flip-flops 17K, 17L and 17M) which is enabled by flip-flop 17H via OR gate 1717. The Q outputs of flip-flop 17K, 17L, and 17M are shown in plots 3, 4, and 5, and the outputs of gates 1718 and 1720 in plots 12 and 13. The output of gate 1720 enables the 'K' input of flip-flop 17H so that on the eight encoder pulse, after writing the file mark, this flip-flop is reset. Since flip-flops 17D and 17G have been previously reset, the $\overline{Q}$ outputs of both these flip-flops are high and the output of gate 1723 will be low disabling gate 1727. Thus the ENABLE CRC signal is not generated and therefore the CRCC character is not loaded into the buffer 1 flip-flops in the recording electronics. Referring to plot 12 of Figure 4-21, it can be seen that the output of gate 1718 goes true for the fourth time, four encoder pulses after the writing of the file mark and for the fifth time, eight encoder pulses after writing the file mark. This output is used to gate out appropriate encoder pulses (plot 17). The fourth of these gated encoder pulses transfers the contents of buffer 1 (which still contains the file mark character) to the WRITE current generator. This, of course, does not change any of the WRITE current generators and therefore no transitions are recorded at this time and no character is written.

Since the $\overline{Q}$ output of flip-flop 17F is low at this time, the output of gate 1721 is high. On the trailing edge of the fourth encoder pulse after the writing of the file mark $\overline{Q}$ output of flip-flop 17M goes low (and the Q output high, plot 11) causing the output of gate 1722 to go high. The output of gate 1726 will therefore be as shown in plot 16. This output (PRIME FOR LRCC) is used to reset all buffer 1 flip-flops in the recording electronics, (see Figure 4-8), using the leading edge.

The fifth time the output of gate 1718 goes true, it gates out another encoder pulse which transfers the contents of buffer 1 flip-flops (which have just been reset) to the WRITE current generator.

In this way, the CRCC is omitted and the LRCC is written eight character spaces after the file mark character.

- The tape accelerates to 25 ips and continues to move at this speed for a period defined by the IRGSS. At the end of this period, flip-flop 17F is reset (plot 4) via OR gate 1712 enabling gate 1711 (plot 7) and thus enabling the MPD which monitors the encoder pulse rate as the tape decelerates. When the rate drops below the appropriate value as described in Paragraph 4.2.4.6.3, a pulse is generated by the MPD circuit (Plot 14).

- This initiates the CLEAN-UP Sequence by

  a. Resetting flip-flop 17E via OR gate 1715.

b. Setting flip-flop 17J (plot 6) via OR gate 1716.

The Q output of flip-flop 17J enables the counter via OR gate 1717 and enables the STEP FORWARD ramp generator.

The tape continues to move until four encoder pulses have been counted. Then, the output of gate 1718 enables the 'K' input of flip-flop 17J and this flip-flop is reset on the fourth encoder pulse. The STEP FORWARD ramp generator is disabled and the tape comes to rest in approximately half-a-character-space.

In addition, the output of gate 1706 becomes true as shown in plot 15 and flip-flop 17N toggles to the reset state (plot 19). The Q output of flip-flop 17N is differentiated by differentiator 17d1 and resets flip-flop 17D.

Note that the output of gate 1718 goes true for the sixth time during the CLEAN-UP sequence and a sixth encoder pulse permitted (plot 17). However, since the WRITE current flip-flops are already reset, no further action takes place.

4.2.4.7.5 BEGINNING OF TAPE GAP Sequence. The output marked INITIATE BOT SEQUENCE (Figure 4-5) sets flip-flop 17B whose output is transmitted via OR gate 1701 and differentiator 17d4 to flip-flop 17C. The sequence which follows is identical with the FILE GAP sequence except that gate 1725 is disabled by the $\overline{Q}$ output of flip-flop 17B so that no FILE MARK character is recorded on the tape. The BOT sequence will attempt to record LRCC but since buffer 1 flip-flops in the WRITE electronics are initially reset, no character is recorded at the LRCC time.

4.2.4.7.6 Special Case When Operational Status is Required Without Tape Motion. This has already been described in Paragraph 4.2.4.1.5 to the point where the CLEAN-UP sequence is requested. The input to differentiator 17d5 initiates this sequence via OR gate 1716. The sequence is described in the last section of Paragraph 4.2.4.7.1 except that flip-flop 17N is not toggled since neither flip-flop 17C or flip-flop 17N are true and therefore AND gate 1706 is disabled.

4.3 Detailed Theory - Printed Circuit Boards. The following contains the detailed theory of operation of the printed circuit boards used in the tape transport. All standard boards are included. A list of the specific boards and the relevant versions used in a particular transport is contained in the Circuit Board Location Chart located on the inside of the front cover. The schematic and parts list for each board is contained in Section VI. Also contained in Section VI are the system wiring diagrams.

4.3.1 Reel Servo and Voltage Regulator (See Schematic 100128). This circuit board contains reel servo amplifiers and four voltage regulators (+10, +5, -10, and -5 Volts) that function in conjunction with several externally mounted power transistors and power resistors shown in Schematic 100338.

4.3.1.1 Reel Servo Amplifiers Identical DC linear position servo amplifiers are used for both the take-up and supply storage systems. The amplifiers are conventional DC, class-B type. The feedback network defines a voltage gain of 18 at frequencies below 1.5 Hz and a gain of 90 at frequencies

above 15 Hz. Two external heatsink-mounted output transistors are associated with each amplifier. (See Schematic 100338.) Q201 and Q202 are used in the take-up amplifier and Q203 and Q204 in the supply amplifier. In addition, a 1-ohm power resistor, R201, is placed in series with the - 16-volt line to the output stage of the take-up amplifier and is used to reduce the power in the amplifier output transistor, Q202. This is necessary since the take-up motor may require up to 2.5 amps to balance the tape tension while the transport is in standby condition. The input resistors, R1 and R2 (Schematic 100128) are driven by the 1000-ohm tension-arm potentiometers, R101 and R102 (Schematic 100338) connected across the +5-volt and -5-volt lines.

4.3.1.2 Voltage Regulators

- +10 Volts - A 10-volt breakdown diode, CR1, in series with diode CR2, supplied with current from a 100-ohm resistor, R31, to the +16 volt unregulated line, is the voltage reference for the +10-volt supply. A power transistor, Q210 connected as an emitter follower with the follower with the voltage reference on the base completes the circuit. The +10-volt line is taken from the emitter of Q210 to the circuit board under discussion, where it drives the 6.8-volt breakdown diode, CR5, for the +5-volt regulator.

- +5 Volts - The +5-volt regulator supplies the bulk of the power to the circuit boards and stabilized within 1%. A 500-ohm

potentiometer, R36, is connected across the 6.8-volt reference diode, CR5, and an emitter coupled comparator, Q16 and Q17, compares the +5-line with the voltage on the potentiometer wiper. The difference is amplified by transistor Q20 and again by power transistor Q207. A 2-ohm power resistor R202 is placed in series with the +16-volt line to reduce the power dissipated in Q207. Test point 1 is connected to the +5-volt line. The +5-volt regulator can supply 2.5 amps.

- -10 Volts - Except for the additional inverting pnp transistor, Q15, operation of the -10-volt regulator is similar to the +10-volt regulator. The -10-volt line is returned from the collector of Q208 to the voltage regulator circuit board where it drives the 6.8-volt breakdown diode, CR5, for the -5-volt regulator.
- -5 Volts - Operation of the -5-volt regulator is identical in principal to that of the +5-volt regulator. However, since less current is carried by this supply, no series power resistor is required. Q209 is the power transistor associated with the -5-volt regulator. Test point 2 is connected to the -5-volt line and test point 3 is connected to Ov(L),

4.3.2 Capstan Drive, Low Speed (See Schematic 100133). This circuit board contains a capstan servo amplifier and stabilization network, ramp generators, an encoder amplifier, lamp drivers, a GENERAL RESET circuit and an interlock relay driver.

4.3.2.1 Capstan Servo Amplifier and Stabilization Network. The capstan servo amplifier consists of an integrated circuit input stage, U1-A, and a discrete component output stage with externally-mounted power transistors Q205 and Q206 shown in Schematic 100338. The low frequency gain from the tachometer to the amplifier output is defined by the ratio of resistor R13 to resistors R51 and R54, i.e. 36. The dead band of the amplifier is large enough so that with no input the input-offset voltage is not sufficient to produce any output voltage.

A 1-ohm resistor, R203, is placed in series with the -16-volt line to the output stage to reduce power dissipation in transistor Q206. Stabilization is accomplished by the filter inductor L1 and capacitor C16.

Test point 2 is connected to the amplifier output and test point 4 to the filtered tachometer output.

4.3.2.2 Ramp Generators

- STEP FORWARD. This circuit is used to generate the command voltage for moving tape incrementally. Test point 5 can be brought to +5-volts by application of the zero-volt level to the STEP FORWARD inputs. The rate at which the voltage on test point 5 changes is controlled by the integrator consisting of transistor Q3, capacitor C1, and resistors R1, R2, and R6. The voltage level is controlled by the +5-volt line and the base-emitter voltage drops of transistors Q1 and Q2. The resulting tape velocity is determined by resistor R8.

- INTER-RECORD GAP. The command voltage for motion of the tape through a distance equal to the standard INTER-RECORD GAP is generated by this circuit. The voltage at the emitter of transistor Q9 rises to +5-volts in 18 milliseconds at a rate controlled by resistor R24 and capacitor C8 on application of a zero volt signal to pin 25. The velocity is 25 ips.
- FILE GAP. This circuit generates the command voltage for motion of the tape at 12 ips with rise and fall times of 35 milliseconds. Zero volts applied to either pin 21 or 22 results in the emitter of transistor Q14 rising to +5 volts.
- REWIND. This circuit generates the command voltage which results in tape speed of 75 ips in the reverse direction. Rise and fall times are about 0.5 seconds, determined by resistors R52, R49, and capacitor C15. When zero volts is applied to pin 20, the emitter of transistor Q19 reaches -5-volts.

4.3.2.3 Encoder Amplifier Linear integrated circuit U1-B is used in a positive feedback mode to produce fast edges at the zero crossings of the sinusoidal encoder output. Transistor Q10 is used to shift the signal level to standard DTL signals.

Test point 3 is connected to one side of the encoder voltage and test point 1 to the amplifier output.

4.3.2.4 Lamp Drivers. The four lamp drivers connect the lamps between +5-volts and -16-volts when the relevant input H, K, 8 or 5 is taken to zero volts. The circuit is designed to supply 60 milliamps and to operate with DTL inputs.

4.3.2.5 GENERAL RESET Circuit. When input L is high or open, a GENERAL RESET signal is applied to the control flip-flops by turning on transistor Q13 such that the output, pin M, is taken to -0.8-volts.

4.3.3 Capstan Drive, Multi-Speed (See Schematic 100260). This circuit board contains a capstan servo amplifier and stabilization networks, ramp generators, an encoder amplifier, lamp drivers, a GENERAL RESET circuit, and an interlock relay driver.

4.3.3.1 Capstan Servo Amplifier and Stabilization Network. The capstan servo amplifier consists of an integrated circuit input stage, U3-A, and a discrete-component output stage with externally-mounted power transistors Q205 and Q206 shown in Schematic 100338. The low frequency gain from the tachometer to the amplifier output is defined by the ratio of resistor R34 and resistors R62 and R63, i.e., 36. The dead band of the amplifier is large enough so that with no input the input-offset voltage is not sufficient to produce any output voltage.

A 1-ohm power resistor, R203, is placed in series with the -16-volt line to the output stage to reduce power dissipation in transistor Q206. Stabilization is accomplished by the filter, inducter L1 and capacitor C16.

Test point 1 is connected to the amplifier output and test point 5 to the filtered tachometer output.

4.3.3.2 Ramp Generators.

- STEP FORWARD. This circuit is used to generate the command voltage for moving tape incrementally. Test point 4 can be brought to two voltage levels by application of a zero-volt level to the STEP FORWARD inputs. The rate at which the voltage on test point 4 changes is controlled by the integrator consisting of integrated circuit U2-B, capacitor C3, and resistors R13, 14, and 17. The voltage level is controlled by the ratio of resistor R15 to resistor R3 when zero volts is applied to pin 23 or 24. This turns off transistor Q1 and allows current from resistor R3 to flow through diode CR1 into the 'virtual ground' point. The resulting tape velocity is determined by resistors R21 and R22.
- INTER-RECORD GAP. The command voltage for motion of the tape through a distance equal to the standard INTER-RECORD GAP is generated by this circuit. The voltage at the emitter of transistor Q3 rises to +5-volts in 18 milliseconds at a rate controlled by resistor R26 and capacitor C5 on application of a zero-volt signal to pin 25. The velocity is 25 ips.
- FILE GAP. This circuit generates the command voltage for motion of the tape at 12 ips with rise and fall times of 35

milliseconds. Zero volts applied to either pin 21 or 22 results in the emitter of transistor Q13 rising to +5 volts.

- REWIND. This circuit generates the command voltage which results in tape speed of 75 ips (some transports operate at 50 ips) in the reverse direction. Rise and fall times are about 0.5 seconds, determined by resistors R58, R64, and capacitor C15. When zero volts is applied to pin 20, the emitter of transistor Q16 reaches -5 volts.

4.3.3.3 Encoder Amplifier. Linear integrated circuit U3-B is used in a positive feedback mode to produce fast edges from the 300-millivolt peak-to-peak encoder output. Transistor Q17 is used to shift the signal level to standard DTL signals.

Test point 2 is connected to one side of the encoder voltage and test point 3 is connected to the amplifier output.

4.3.3.4 Lamp Drivers. The four lamp drivers connect the lamps between +5-volts and -16-volts when the relevant input H, K, 8 or 5 is taken to zero volts. The circuit is designed to supply 60 milliamps and to operate with DTL inputs.

4.3.3.5 GENERAL RESET Circuit. When input L is high or open, a GENERAL RESET signal is applied to the control flip-flops by turning on transistor Q22 such that the output, pin M, is taken to -0.8-volts.

4.3.4 Function Control (See Schematic 100223). This circuit board contains the logic required to bring the machine to operational status in

conjunction with the manual and remote controls and the photo sensors, and also the logic required to generate IBM compatible gaps.

Operation of the logic is described in detail in Paragraph 4.2.4 using Figures 4-5 and 4-17. The Cross Reference Chart, Table 4-2 will assist in identifying the major components in the system, however, 100% correspondence is not possible since the figures 4-5 and 4-17 are logic diagrams while the schematics show every component used.

In addition to the integrated circuit logic, the circuit board contains the following descrete component circuits: A switch-contact filter circuit, differentiator circuits, a delay circuit, photo sensor circuits, a single shot circuit, and a missing-pulse detector circuit (MPD).

4.3.4.1 Switch Contact Filter Circuit. The combination resistor R2, capacitor C3, and resistor R3 is a typical switch-contact filter circuit. The main purpose of the circuit is to filter out spikes caused by capacitive cross-talk between the switch lines which are cabled together in the same harness. R2 and C3 form the filter while R3 ensures that the input to pin 5 of U5 is at +5-volts when the switch contact is open. Since the threshold of the IC is approximately 1.8 volts, considerable noise protection is available.

4.3.4.2 Differentiators. A typical differentiator is designated 5d1 in Figure 4-5 and consists of components C7, R12, R10 and R11 in Schematic 100223. Resistors R10 and R12 set the static level at the output of the differentiator at +3 volts, giving a noise immunity of 1.2 volts typically. C7 is the differentiating

FIGURE 4-5	REFERENCE DESIGNATION SCHEMATIC 100223
Flip-flop 5A	U1-A, U1-B
Flip-flop 5B	U1-C, U1-D
Flip-flop 5C	U4-A, U4-B
Flip-flop 5D	U4-C, U4-D
Flip-flop 5E	U2-A, U2-B
Invertor 515	Q2 and associated components

FIGURE 4-17	REFERENCE DESIGNATION SCHEMATIC 100223
Flip-flop 17A	U5-A, U5-B
Flip-flop 17B	U5-C, U5-D
Flip-flop 17C	U6-A, U6-B
Flip-flop 17D	U6-C, U6-D
Flip-flop 17E	U7-C, U7-D
Flip-flop 17F	U11-A, U11-B
Flip-flop 17G	U11-C, U11-D
Flip-flop 17H	U18-A
Flip-flop 17J	U18-B
Flip-flop 17K	U16-B
Flip-flop 17L	U16-A
Flip-flop 17M	U17-B
Flip-flop 17N	U17-A

TABLE 4-2. CROSS REFERENCE CHART

input capacitor, and resistor R11 limits the current which flows when the IC input is driven below 0 volts by capacitor C7, causing the substrate diode to conduct.

4.3.4.3 Delay Circuit. Referring to Figure 4-17 a delay is inserted between gate 1708 and differentiator 17d3. Resistor R59 and capacitor C19, provide this delay for positive going edges. When U9-A cuts off, the output pull-up resistor (6000 ohms) and the input pull-up resistor in U9-B charges capacitor C19 toward the input threshold of U9-B. The 0.015 uf capacitor provides a nominal 9-usecond delay. When U9-A switches on, capacitor C19 is discharged to approximately 0 volts by resistor R59, limiting the peak current to 33 milliamps.

4.3.4.4 Photo Sensor Circuits. Two photo sensor circuits are provided, one to detect the BOT tab and one to detect the EOT tab.

Two photo transistors and a lamp make up the Photo Sensor Assembly which is located on the head plate. The collector loads for the two transistors are potentiometers R15 and R31 which allow the sensitivity of the circuit to be adjusted. The photo transistor outputs drive emitter followers Q1 and Q3, and capacitors C9 and C26 filter out any spurious signals picked up in the harness. Resistors R14 and R32 limit the charging current which flows on positive going edges.

4.3.4.5 Single Shot. This circuit provides two delay periods for timing the INTER-RECORD GAP and the FILE GAP. C12, C13, C14 are the timing

capacitors and R40 is the timing resistor for the FILE GAP. The FILE GAP time is adjusted by varying the potential from which the capacitors start discharging. In order to generate the IRG, transistor Q4 is cut off and additional discharge current is provided by resistors R36 and R37.

Consider the circuit when generating a FILE GAP. Normally flip-flop U11-B, U11-A is reset and input B of the single shot is low. Transistor Q5 is turned on clamping the timing capacitors to a potential defined by the resistor chain R39, R38 and R85. When the FILE GAP command is given the flip-flop is set, transistor Q5 is turned off and diode CR6 cuts off. The capacitors discharge on an exponential toward -5 volts with time constant (C12+C13+C14) (R40). Transistors Q6, Q7, and Q8 constitute a comparator whose threshold is approximately OV.

Normally transistor Q6 and diode CR9 are cut off, transistor Q7 is on, and transistor Q8 is off so that the collector of transistor Q8 is high. When the potential of the capacitors is approximately -0.7 volts, transistor Q6 starts to conduct and begins to turn off transistor Q7. Positive feedback provided by capacitor C15 and resistor R45 latches the comparator. The collector of transistor Q8 goes low, resetting flip-flop U11-B, U11-A. As a result transistor Q5 is turned on and the capacitors are charged to their starting potential through the 220-ohm resistor, R39. After a time determined by resistors R42 and and R45 and capacitor C15, the comparator switches back to the quiescent state.

Operation for IRG generation is identical except that Q4 is cut off and resistors R37 and R36 provide a faster discharge time for capacitors C12, C13, and C14.

4.3.4.6 Missing Pulse Detector (MPD). This circuit is required to detect the time when the frequency of an incoming encoder pulse train becomes lower then the appropriate value (see Paragraph 4.2.4.6.3). The circuit is similar in operation to the single shot except that after initial enabling, the capacitors are returned to the quiescent state by each encoder pulse.

C24 is the timing capacitor and R78 the timing resistor. Transistors Q13 and Q14 are the comparator and transistors Q11 and Q12 constitute a pulse-stretching monostable flip-flop which lengthens the 6-usecond encoder pulse to about 120 useconds. This longer pulse allows adequate time for capacitor C24 to be charged back to the quiescent state.

In operation, flip-flop U7-C, U7-D is triggered by the gapping command, providing the enable signal to the MPD. At the time when MPD operation is required, signal input C is high and the capacitor starts to discharge. On every encoder pulse flip-flop Q11 and Q12 fires, charging the capacitor back up again. When the time between successive pulses is long enough (greater than 0.5 milliseconds) the capacitor level moves more negative than the comparator threshold causing the comparator to fire, resetting flip-flop U7-C, U7-D. The comparator resets automatically after a time determined by resistor R81 and R78 and capacitor C25.

Two versions of the Function Control Circuit Board are available. The -01 version is for use in the incremental write only transport. This version requires a jumper for connecting the READY flip-flop (U2-B, U2-A) to the WRITE POWER CONTROL amplifier (Q9, Q10).

In the -02 version, which is used for read/write transports, the jumper is omitted. In this case the WRITE POWER CONTROL amplifier is enabled via pin $\overline{C}$ (EWPC).

4.3.5 Transmitter - Slow Interface (See Schematic 100253). This circuit board is designed to convert the transport internal logic levels to levels suitable for transmission over an interface cable up to 20 feet in length with single wires for each signal and common zero-volts reference. It operates with the Receiver - Slow Interface circuit board or its equivalent.

The input is compatible with DTL integrated circuits (0 volts - TRUE, +5 volts-FALSE).

The outputs for configurations A and B are as follows:

Configuration A

- TRUE: +10 volts, 1000-ohms impedance

  FALSE: 0 volts

Configuration B

- TRUE: -10 volts, 1000-ohms impedance

  FALSE: 0 volts

4.3.5.1 Configuration A. Configuration A is a conventional invertor with capacitor C1 slowing down the rise and fall times to around 6 useconds to reduce the capacitive crosstalk found in single-wire transmission systems.

4.3.5.2 Configuration B. Configuration B converts the positive-input DTL levels to negative output levels by employing transistor Q1 as a saturating emitter follower whose emitter current flows into the emitter of the grounded base output transistor Q2. When the input is taken to 0 volts, transistor Q1 is turned off, removing emitter current from transistor Q2 whose collector voltage falls to -10 volts. Capacitor C1 is again used to slow down the rise and fall times of the output wave-form.

The slow rise and fall times result in considerable delay but allow the receiver to dispense with any filtering assuming 1.0 volts noise margin.

4.3.6 Receiver - Slow Interface (See Schematic 100248). This circuit board is designed to convert high level (0 volts-FALSE;+5 to +15 volts-TRUE or 0 volts-FALSE; -5 to -15 volts-TRUE) interface signals to standard DTL levels (+5 volts-FALSE; 0 volts-TRUE).

The circuit operates in conjunction with the Transmitter - Slow Interface board or its equivalent. The circuit uses a single wire cable with a common zero-volt reference. The input filter, consisting of resistors R1 and R2 and capacitor C3 is designed to remove the spikes produced by fast transmitters driving several adjacent wires.

In addition the following is provided: Some DTL invertors (U11), a binary zero to BCD10 convertor (U3) which is disabled by tying pin $\overline{E}$ to 0 volts and a parity tree that can be switched to provide odd, even or external parity. 7- or 9-track facilities are optional.

On WRITE transports the parity tree is included; on READ transports the data receivers and parity tree are omitted and only circuits 200 through 1000 are included.

4.3.6.1 Configuration A (positive logic). Configuration A is a conventional invertor with an input filter and 1-volt noise rejection. In response to a TRUE input signal (+5 to +15 volts), the output goes to 0 volts.

4.3.6.2 Configuration B (negative logic). Configuration B in response to a TRUE signal (-5 to -15 volts) turns on transistor Q2 driving the emitter of transistor Q1, a grounded base amplifier, resulting in the output going to 0 volts as transistor Q1 saturates.

4.3.6.3 Binary Zero to BCD Convertor. The binary zero to BCD convertor is required when 'even parity' might result in an all zero signal failing to produce a transition in any track at that character. An 'all zero' input is detected by the DTL invertors U1, U2, and U3 producing a +5-volt level at pin $\overline{E}$. Unless pin $\overline{E}$ is tied to 0 volts, the 'all zero' character will force '1's in bits 21 and 23 (U3-C and U3-A).

4.3.6.4 Parity Generator. The operation of the parity tree can be understood by considering one stage, e.g., U6-D, U7-A and U7-B. Here the first two bits of the character are "added." The truth table is as follows.

Bit 0	1	0	1	0
Bit 1	1	0	0	1
Level at U10-A-2	0	0	1	1

Thus, when the two bits are identical a '0' results and when different, a '1' results. Pairs are checked in this way and the operation is continued on the results until all of the bits have been 'added'. The switch S1 is used to select either the result of the addition or its inverse depending on whether even or odd parity generation is required. For 7-track operation U4 and U8 are omitted and shunted by jumper A.

The third switch-position allows external parity generation.

4.3.7 Transmitter - DTL (See Schematic 100338). This circuit board is designed to convert the transport internal logic levels to levels suitable for transmission over an interface cable consisting of twisted pairs up to 20 feet in length. It operates with the Receiver - DTL circuit board or equivalent.

The input is compatible with DTL integrated circuits (0 volts-TRUE and +5 volts-FALSE). Two configurations are available resulting in HIGH-TRUE or LOW-TRUE outputs. The high level as measured at test points is between +3 or +5 volts depending on the receiver configuration. The low level is between 0 and +0.4 volts.

The invertors U1, U2, U3 and U7 are used only in the LOW-TRUE configuration when the 'dotted' jumper wire is inserted. In the HIGH-TRUE configuration invertors U1, U2, U3 and U7 are omitted and the solid jumper wires are inserted. The 180-ohm pull-up resistors are connected to +5 volts externally except where a pull-up resistor is used at the receiver end of the cable; in this case, they are omitted. The series 68-ohm resistor is included in certain versions to provide a partial source termination for negative going edges.

The output stage uses the DTL power gate type 944 or 844.

4.3.8 Receiver - DTL (See Schematic 100333). This circuit board is designed to convert interface signals at standard logic levels. It terminates interface cable consisting of multiple twisted pairs, up to 20 feet in length. It operates with the Transmitter - DTL circuit board or its equivalent. The board is also used to generate the parity bit for 6- or 8-bit characters in certain versions.

Three configurations are used in different verions:

4.3.8.1 Configuration A. Configuration A is used for HIGH-TRUE logic where at 180-ohm pull-up is used at the transmitter output. The 68-ohm resistor, R1, and capacitor C1 reduce the reflections due to imperfect termination. The 470-ohm resistor, R2, makes the input signal LOW-FALSE when the cable is removed. The two invertors in each input circuit are used in the parity generator circuit, U2, U3, U4, U5, U6, and U7. By using jumpers the output polarity of the receiver is always LOW-TRUE. (See Note 1 of Schematic 100333.)

4.3.8.2 Configuration B. Configuration B is used for LOW-TRUE logic where a 180-ohm pull-up resistor is used at the transmitter output. The 68-ohm resistor, R1, and capacitor C1 reduce the reflections due to imperfect termination. The 470-ohm resistor, R2, of configuration A is removed so that the input goes HIGH-FALSE on removal of the cable. Note, however, that the removal of power at the transmitter results in a LOW-TRUE condition if the

180 ohms on the transmitter is allowed to 'turn off' the input invertor of the receiver.

4.3.8.3 Configuration C. Configuration C is used for LOW-TRUE logic and circumvents the possibility of interpreting the removal of power at the transmitter as a LOW-TRUE signal. The pull-up for the input invertor of the receiver is located at the receiver end of the cable and a high resistance at the transmitter output ensures that loss of transmitter power or interruption of the interface cable cannot be interpreted as anything but a HIGH-FALSE signal. The parallel combination of resistors R1 and R2 results in the termination of the line with close to the characteristic impedance.

4.3.8.4 Parity Generator. The parity generation circuit, used in certain versions, consists of cascaded 'half-adders' which produce the parity bit at pins 8 and 11 of U7. If the total number of '1's' in the 6- or 8-bit character is odd a low level results at this point, and by throwing S1 to the 'E' position (for EVEN parity) a '1' is written in the check bit track. If the total number of '1's in 6- or 8-bit character is even, a low level appears at U7-3, and by throwing S1 to the '0' position (for ODD parity) a '1' is written in the check bit track. The third switch position 'X' is used when the parity bit is included with the data character and internal generation is not required. The externally generated parity bit must be brought into circuit 100.

4.3.8.5 Binary Zero to BCD 10 Conversion. Invertors U4-F, U4-E, U1-A, U1-B, U1-D, U1-F form an AND gate which produces a high output at

pin $\overline{E}$ when the data character consists of six 'O's. Unless pin $\overline{E}$ is tied to zero volts externally, bit 2^1 and 2^3 will be forced to the '1' state by invertors U4-C and U1-C to produce the BCD 1010 character. Unless specified otherwise, pin $\overline{E}$ is connected externally to zero volts, removing this facility.

4.3.9 Double Buffer - Write Amplifier (See Schematic 100233). This circuit board is comprised of seven write amplifiers, two buffer registers for temporary storage of the write data, and control circuits.

The two buffer registers consist of seven J-K flip-flops, each of which is comprised of a master and a slave flip-flop. These correspond to flip-flops 8A and 8B of Figure 4-8. The master flip-flop toggles on receipt of a '1' and the output is copied successively into the slave flip-flops and then to the WRITE amplifiers Q4 through Q17 (8C of Figure 4-8). The WRITE amplifier is a resistor-transistor flip-flop which defines the write current by means of resistors R26, etc., in series with the head windings. The head winding center tap is taken to -5 volts when the WRITE current is enabled. Test points 1 through 7 are connected to the WRITE amplifier outputs.

At the WRITE DATA inputs, WDO through WDP, 0 volts represents a '1'. The pulse which toggles the master flip-flop in response to write data '1' is generated from the WRITE STEP command. The 2-usecond pulse at the test point 8 is generated from the trailing edge of the output of the single-shot Q1 and Q2. This pulse, after being delayed 4 useconds by U12-A, U12-B, R20, C8 and R21, C9, sets the control flip-flop, U13-D, U13-C (7E of Figure 4-8). This delayed pulse also copies the contents of the master flip-flops into the

slave flip-flop register. This pulse is visible at test point 9.

During power-up, and until write current is turned on, the buffer slave flip-flops are reset and gates U7, U8, U9 and U10 are held enabled to force the state of the WRITE amplifier flip-flops when the WRITE CURRENT ENABLE waveform takes the head center taps to -5 volts. After WRITE current is turned on, the flip-flop, U18-A and U18-B, is reset by the CT4 pulse thus returning control of these gates to the encoder pulse.

Data is copied into the WRITE amplifiers by enabling gates U7, U8, U9 and U10 for 2 useconds. This copy pulse appears on test point 10 and is generated on both the positive and negative going edges of the encoder waveform by gates and discrete capacitors and resistors.

The negative going enable check character (ECC) pulse resets all buffer slave flip-flops when a LRCC is required. The presence of an enable file mark signal and an ECC pulse sets the first four (WDO - WD3) buffer slave flip-flops to write a file mark character on receipt of the following encoder pulse.

4.3.10 Double Buffer, 9 Channel Write Amplifier (See Schematic 100238). The Double Buffer, 9 Channel Write Amplifier contains 9 channels of write electronics capable of recording data at rates up to 700 steps per second. It also has the capability of providing electronic deskewing facilities if required. Each channel is comprised of

- Two buffer registers for temporary storage of the write data; these correspond to flip-flops 8-A and 8-B of Figure 4-8.
- A write waveform generator (which can also be used as a deskewing buffer) and a write amplifier circuit; these are combined

into flip-flop 8-C of Figure 4-8.

- Control circuits

The two data buffer registers consist of the master and slave sections of the J-K flip-flops U4-A, U4-B, U5-A, U5-B, U6-A, U6-B, U7-A, U7-B. The write waveform generator is constituted by the J-K flip-flops U9 through Q21. Test points 1 through 9 are connected to the WRITE amplifier outputs.

In operation, the WRITE STEP Command (WSC) pulse at pin 13 triggers the 5-usec single shot Q1, Q2. A 2-usec pulse is generated from the back edge of the single shot and fed to power gate U21-B via invertors U25-C and U25-D. The output of U21-B is used to strobe the low-true data inputs WDO through WDP into the master section of the buffer J-K flip-flops via AND gates U1-B, U1-C; U1-D, U1-A through U3-F, U3-E. This pulse is visible at test point 10. If the data input is a '1', the corresponding master section of the flip-flop toggles.

The pulse also triggers the control loop consisting of flip-flop U20-A, U20-B, flip-flop U20-D, U20-C, gate U24-A and R20, U19-B, R21, and U19-A which constitute the 4-usec delay. As previously explained in Paragraph 4.2.4.4, waveforms STEP FORWARD LEVEL 1 (SFL1) and STEP FORWARD LEVEL 2 (SFL2) are generated at the $\overline{Q}$ outputs of flip-flops U20-D, U20-C and U20-A, U20-B and control the STEP FORWARD ramp generators. A 2-usec shift pulse is also generated by this control loop which is fed to power gate U21-A. The output of U21-A, which is visible at test point 11, copies the contents of the master section of the buffer flip-flops into the slave section. Tape motion results in a signal ENCODER AMPLIFIER OUTPUT (EAO) being fed to pins $\overline{E}$ and $\overline{F}$.

Either sign of transition results in a 6-usec positive-going pulse ENCODER PULSE WIDE (EPW) at pin 24 and a 2-usec positive-going pulse ENCODER PULSE NARROW POWERFUL (EPNP) at pin 22 (visible at test point 12) provided that gate U24-D is enabled by the ENABLE ENCODER PULSE (EEP) signal.

The EPNP pulse copies the output of the buffer flip-flops into the master sections of the write-waveform generator flip-flops. Normally EPNP is also fed to the toggle inputs DSSO through DSSP of these flip-flops so that, at the falling edge of EPNP, the contents of the master sections of the J-K flip-flops is transferred to the slave sections. The slave outputs feed the WRITE amplifiers. EPNP from U24-D also resets flip-flop U20-D, U20-C.

The system can be used for electronic deskewing if ever required by feeding the EPNP pulse to nine single shots each adjusted to give a positive pulse of length equal to the required deskew time for the appropriate channel. These pulses are fed to the DSSO through DSSP inputs.

Waveforms ENABLE FILE MARK (EFM) and ENABLE CHECK CHARACTERS (ECC) are combined to produce signals at the outputs of U23-B and U24-B which correspond to PRIME FOR LRCC and PRIME FOR FM as described in Paragraph 4.2.4.5. These signals are respectively used to reset the second stage of the buffer flip-flops for LRCC generation and those stages relevant for FILE MARK generation.

The WRITE CRC (WCRC) pulse on pin 28 is OR'd into the WSC channel and is used to copy CRCC into the buffer during a 9-track gapping sequence. This is explained fully in Paragraph 4.3.12.

4.3.11 Quad Buffer and Write Amplifier (See Schematic 100569). The following description of the Quad Buffer and Write Amplifier circuit board is condensed. A full understanding will depend upon the more detailed descriptions contained in 4.3.9 and 4.3.10, for the Double Buffer - Write Amplifiers. That is, when the operation of the Double Buffer is fully understood the Quad Buffer should be interpreted as an extension of the basic principles involved. Utilization of both theories of operation will enable the reader to understand the total system for input data rates from 0 to 1000 steps per second asynchronous operation.

The Quad Buffer and Write Amplifier circuit board, which can be adapted for either 7- or 9-track operation, contains the electronics that provides the transport with the capability to record asynchronous data at a rate from zero to 1000 steps per second without the need to accelerate the capstan at an excessive rate. This is accomplished by the use of four data buffer registers which temporarily store the write data.

The circuit board is comprised of four data buffer registers and a write waveform generator and amplifier circuit for each channel and the control logic, which consists of a single-shot and three delay loops; each delay is approximately 4-useconds.

For simplicity, the following description of operation is confined to a single channel since all 7 (or 9) channels operate identically.

The first two stages of buffering are accomplished by the use of J-K flip-flop, which operates on a "master-slave" principal. The third and fourth stages utilizes a S-C flip-flop which also employs the "master-slave" principal.

The write waveform generator consists of a J-K flip-flop; the write amplifier is a transistor output stage which drives current through the magentic head.

On receipt of a WRITE STEP Command, a 5-usecond single-shot Q1, Q2, is triggered. The 2-usecond pulse generated from the trailing edge of the single-shot is fed to power gate U30-B. The output of gate U30-B performs two functions; one of these functions will be discussed now, the other function will be dealt with later.

The output of power gate U30-B (TP10) strobes the low-true input data (WDO) into the "master" section of the data buffer J-K flip-flop U15-B (first stage) via AND gates U16-C, U16-D.

The initial Write Data bit (WDO for example) is strobed into the "master" section of J-K flip-flop U15-B, by the output of power gate U30-B. After a delay of 4-useconds, the Write Data is transferred into the "slave" section of the S-C flip-flop, U6, by a delay pulse from the output of U29-A. Once again, after another 4-usecond delay, the information is transferred into the final data buffer, the "slave" section of the S-C flip-flop, U6 by a delay pulse from the output of U29-B. The data awaits the arrival of an encoder pulse to trigger flip-flop U1-B and subsequently write a '1' on the tape via transistors Q4 and Q5.

This final delay pulse also sets flip-flop U26-A, U26-B and the STEP FORWARD LEVEL (SFL1) waveform is generated at the output of the flip-flop. Tape motion results, and when the capstan has moved the appropriate distance an Enable Encoder Pulse (EEP) is generated enabling AND gate U32-B. The

output of AND gate U32-B is fed to power gate U30-A and the leading edge of the pulse generated at the output of this gate, Encoder Pulse Narrow Powerful (EPNP), causes the data stored in the final stage of the data buffer register to be transferred to the write waveform generator and the write amplifier, thus to toggle the write amplifier if the write waveform generator flip-flop had been enabled by a data '1'.

While the information in the final data buffer is waiting for the EPNP pulse to occur, the second Write Data bit has filled up the preceding buffer U15-B. The delay pulse which transferred the data into this third data buffer had also set flip-flop U27-C, U27-D. The second level ramp velocity was conditioned by SFL2, generated by the output of flip-flop U27-C, U27-D.

Subsequently, the second data buffer (the "slave" section of U15-B) was filled with the third Write Data bit by a delay pulse which also set flip-flop U24-C, U24-B, and enabled the third level ramp generator (SFL3). Finally, the first data buffer (the "master" section of U15-B) was filled with the fourth Word Data bit by the output of gate U30-B. The other function of gate U30-B, which was mentioned previously, sets flip-flop U23-B, U24-D and enables the fourth level ramp generator (SFL4).

By the time the fifth Word Data bit is received, the capstan will have moved the correct distance to generate the EPNP pulse and:

1. The data in the final data buffer has transferred its output to the write waveform generator and the write amplifier.
2. The data in the third data buffer has transferred to the final data buffer after the generation of a delay pulse. This occurred when the encoder pulse reset flip-flop U26-A, U26-B via gate U32-B enabling the 4-usecond delay loop (U27-A, U28-A, U29-B and associated components).

3. The data in the second data buffer has transferred to the third data buffer after the generation of a delay pulse. This occurred when a delay pulse reset flip-flop U27-C, U27-D enabling a 4-usecond delay loop (U27-B, U28-F, U28-E and associated components).
4. The data in the first data buffer has transferred to the third data buffer after the generation of a delay pulse. This occurred when a delay pulse reset flip-flop U24-C, U24-B enabling a 4-usecond delay loop (U23-A, U28-D, U25-B and associated components).
5. The fifth Word Data bit is strobed into the first data buffer by the output of gate U30-B.

Waveforms ENABLE FILE MARK (EFM) and ENABLE CHECK CHARACTERS (ECC) are combined to produce signals at the outputs of U31-A, B and U32-D which correspond to PRIME FOR LRCC and PRIME FOR FM as described in Paragraph 4.2.4.5. These signals are respectively used to reset the second stages of the data buffer flip-flops for LRCC generation and those stages relevant for FILE MARK generation.

The WRITE CRC (WCRC) pulse on pin 28 is OR'd into the WSC channel and is used to copy CRCC into the data buffer during a 9-track gapping sequence. This is explained fully in Paragraph 4.3.12.

Flip-flops U24-A, U26-B, gates U25-A and U26-C and inverters U10-D and U10-E are used to generate a BUFFER 1 BUSY (B1B) signal which is mainly used in the gapping logic to prevent a gapping sequence from being initiated before all the data has been recorded on the tape.

Two versions of the Quad Buffer and Write Amplifier circuit board are available which are suitable for 7-track or 9-track operation. The appropriate FILE MARK generation is selected by jumpers W1 and W2. The components within the dotted box are omitted in the 7-track versions.

Flip-flops U18-A, U18-B; gates U18-C and U22-C and invertors U19-D and U19-E are used to generate a BUFFER 1 BUSY (BIB) signal which is mainly used in the gapping logic to prevent a gapping sequence being initiated before all the data has been recorded on the tape.

Two versions of the Double Buffer, 9-Channel Write Amplifier circuit board are available which are suitable for 7-track and 9-track operation. The appropriate FILE MARK generation is selected by jumpers W1 and W2. The components within the dotted box are omitted in the 7-track versions.

4.3.12 Echo Check Parity (See Schematic 100363). This circuit board contains the facilities for detecting an error during the recording process.

Information is recorded in the NRZI mode, i.e., reversal of magnetization on the tape occurs for each '1' recorded. This is accomplished by feeding current into one-half of a center-tapped recording head. The center tap of the head is returned to -5 volts and current is supplied to the relevant half-winding from a PNP transistor connected to +5 volts through a current defining resistor. Both the PNP transistor and current defining resistor are located on the WRITE Amplifier circuit board.

Whenever current is switched off in one-half of the head (and switched on in the other), the voltage at the end of that half swings negative, relative to -5 volts due to the inductive nature of the recording head. The negative swings from each half of the head windings are fed to diodes CR1 and CR2, cutting off transistor Q1. A positive going pulse is thus generated at the junction of resistors R3 and R4 for each '1' bit recorded. The typical circuits,

designated 100 through 900 provide this function for each of the nine possible heads. In a 7-track system, circuits 100 through 600 and circuit 900 are used. The positive pulses are inverted by U1-B, U1-A, etc., and fed to flip-flops U2-C, U2-D, etc.,and in turn are fed to a parity-tree check system where the appropriate output of gate U13-B (EVEN parity) or gate U17-D (ODD parity) is selected by parity switch S1. If the parity is incorrect, pin 12 of AND gate U13-D is enabled.

Input ENCODER PULSE WIDE (EPW) is an 8-microsecond positive-going pulse whose leading edge is used to trigger the write flip-flops, located on the double buffer circuit board, and whose negative trailing edge is used to generate a positive pulse at transistor Q2. This, in turn, is fed to pin 13 of AND gate U13-D. Thus, if the echo parity is incorrect, flip-flop U13-C, U12-B will be set and its output fed to the interface transmitter.

The negative trailing edge of EPW also triggers the single-shot consisting of transistors Q3 and Q4. The output of the single-shot is inverted by U9-D where the trailing edge is differentiated by capacitor C7 and inverted by transistor Q5. This pulse resets flip-flops U2-D, U2-C; etc. via invertor U9-E, OR gate U10-D and inverters U11-E and U11-C. The ECHO-CHECK ERROR flip-flop U13-C, U13-B is reset externally via pin $\overline{F}$ (ECR).

It is necessary to disable the echo check system under three circumstances. The first condition occurs when WRITE current is switched on during the time the transport is being brought up to operational status. This could cause spurious signals to inputs 1 and 2 which could set the flip-flops prematurely. Flip-flop U12-D, U12-C prevents this situation as follows. The

flip-flop is reset initially by GENERAL RESET signal (GRS) disabling the system by holding flip-flop U13-C, U12-B reset. After the encoder pulses have occurred during the generation of the BOT gap, the CT4 signal goes true and sets flip-flop U12-D, U12-C enabling the echo check system.

The second occurs during REWIND; here, encoder pulses are occuring throughout the REWIND operation, but the absence of WRITE current transitions leave all the echo check flip-flops reset which yields EVEN parity. Consequently, flip-flop U12-D, U12-C is held reset by ECHO CHECK DISABLE (ECD) which is generated from the REWIND signal. This disables the echo check system as already described.

The third condition occurs during a gapping sequence. The parity of the check characters (LRCC and CRCC) and the file mark depends on the number of characters in the record and whether 7- or 9-track recording is being used. It is therefore not always the same as the data and for that reason the echo check system must be disabled during gapping. The output of invertor U11-B is used to disable AND gate U13-D preventing the setting of flip-flop U13-C, U12-B and simultaneously holding the echo-check flip-flops reset. The invertor is energized whenever GAP IN PROCESS (GIP) is true and the BUFFER ONE BUSY (BIB) signal is false, i.e., when a gap command is being given and all the data in the previous record has been recorded.

Capacitors C3 and C8 delays the leading and trailing edges of the GIP signals to avoid 'race' conditions.

4.3.13 **Cyclic Redundancy Check Generator (CRC Generator)** (See Schematic 100264). The CRC Generator circuit board comprises the following:

- The CRC Register (CRCR)
- Twenty-two Exclusive OR Gates (EO)
- Two Single Shots

The operating rules for generating the CRC characters (CRCC) have already been discussed in Paragraph 4.2.4.5. The actual mechanization of the system is as follows.

Each bit of the 9-bit character (8 plus parity) is presented to one input of each of the nine low-true two-input AND gates, U8-B, U8-E; U8-A, U8-F; etc. During data recording, the second input of each of these gates is enabled and the output of each gate is fed to one input of each of the nine AND gates, U9-B, U9-C, U7-B, U7-C, U5-B, U5-C, U4-B, U4-C, and U2-B. The other inputs of each of these gates are enabled at this time and the outputs of these gates feed the Double Buffer and Write Amplifier circuit board.

The output of gates U8-B, U8-E; U8-A, U8-F; etc., are inverted by U20-A, U20-F, etc., and two phases of each bit of the character fed to the first level of EO circuits. In the case of bits P, 0, 1, 6, and 7, the other input is from the adjacent position in the CRCR. Thus, for example, data-bit P is exclusively OR'd with CRCC bit 7 by U29-C, U29-D, and U20-B, etc. In the case of bits 2, 3, 4, and 5, two other inputs are OR'd with each data input using three-way EO circuits. Thus, for example, data-bit 2 is exclusively OR'd with CRCC bit 7 and with CRCC bit 1 using U31-A, U31-B, and U19-F and U26-C, U26-D and U19-E.

The second level of EO circuits U29-A, U29-B and U20-C; U28-A, U28-B and U20-D, are alike for all nine positions. The first level EO circuit outputs form one input, the other input is from the same bit position of the CRCR. The outputs of the second level EO circuits are each fed to one of the nine J-K flip-flops U15-A, U15-B, U14-A, U14-B, etc., which constitute the CRCR.

The WRITE STEP command corresponding to each data character is fed via OR gate U16-C, U16-A, U16-B to the single shot, Q4, Q5, Q6, which delays the WRITE STEP command five microseconds before it is fed to the clock input of each J-K flip-flop. This pulse can be observed at test point 2. If the output of the second level EO circuit for a particular bit is true, the J-K flip-flop for that bit is toggled by the delayed WRITE STEP command. The status of each bit of the CRCR can be observed at test points 11, 12, 10, 8, 9, 5, 7, 3 and 4.

After the termination of data recording, the IRG or FILE GAP command is given, causing the ENABLE CRC (ECRC) wave form to go low. This negative-going edge is delayed approximately ten microseconds via R1, C2, U33-A, and U33-C, and used to trigger the 10 microsecond single shot Q1 and Q2. As a result, a 10-microsecond positive going pulse is generated at the outputs of the invertors U32-A and U33-F. This pulse disables the low-true AND gates U8-B, U8-E; U8-A, U8-F; etc., so that the nine data inputs in the first level EO circuits are guaranteed false,i.e.,'0'. The positive going edge of the 10-microsecond pulse is OR'd into the WSC line and triggers single shot Q4, Q5, and Q6 generating an artificial WSC 5 microseconds later. This generates the extra shift referred to in Paragraph 4.2.4.5.3.

The delayed ECRC wave form which is inverted by power gate U1-B and can be observed at test point 6, enables one input of each of the nine AND gates U9-A, U9-D, U7-A, U7-D, U5-A, U5-D, U4-A, U4-D and U2-A. The other input to these gates is from the J-K flip-flops constituting the CRCR. In this way the output of the CRCR is routed to the Double Buffer and Write Amplifier circuit board. Note that the $\overline{Q}$ outputs of the J-K flip-flops are used except CRC2 and CRC4 which use the Q outputs.

The negative-going edge of the 10-microsecond positive-going pulse is differentiated by resistor R9, capacitor C5, resistor R10, and transistor Q3 generating a negative going pulse WRITE CRC (WCRC) at the output of invertor U33-B. This pulse, observed at test point 13, is used to copy the contents of the CRCR into the Double Buffer and Write Amplifier circuit board where it is held until the appropriate encoder pulse (fourth pulse after gap initiation) causes the CRCC to be written.

Four character spaces after the CRCC has been written, the LRCC is written. This is accomplished on the Double Buffer and Write Amplifier circuit board by the ECC wave form. This information is also fed to pin 6 of the CRC Generator circuit board and inverted by U2-D. The output of U2-D is fed to power gate U10-A. The output of gate U10-A, which can be observed at test point 14, resets the CRCR ready for CRC generation during the next record.

SECTION V - MAINTENANCE AND TROUBLE-SHOOTING

5.1 Introduction. This section provides the information necessary to perform electrical adjustments, mechanical adjustments, parts replacement and trouble shooting.

Section VI contains the schematic diagrams required for reference when electrical adjustments or trouble-shooting is necessary.

5.2 Replacement.

5.2.1 Fuses.

Line Fuse: 110-125 VAC Line; 2.0 amps, 3AG, slow-blow

200-250 VAC Line; 1.0 amp, 3AG, slow-blow

XF201: 8 amps, 3AG

XF202: 8 amps, 3AG

5.3 Electrical Adjustments.

5.3.1 STEP FORWARD Ramp Generator. Adjustment of the STEP FORWARD ramp generator is required only when the Capstan Drive circuit board or one of the generator components on the circuit board is replaced.

5.3.1.1 Required Test Equipment.

Oscilloscope

Pulse Generator

5.3.1.2 350 or 500 Steps per Second Transport Adjustment Procedure. (See Schematic 100133 - Capstan Drive, Slow Speed.)

a. Set the gain of oscilloscope at 50 millivolt/cm and connect to test point 3.

b. Set the pulse generator to 100 Hz and connect to WRITE STEP command pin of interface connector. (Refer to Paragraph 1.6.1 Slow Interface or Paragraph 1.6.3 DTL Interface for required pulse specification and to Figure 2-1, Slow Interface or Figure 2-2, DTL Interface for appropriate WRITE STEP command interface pin).

c. Bring transport to READY status.

NOTE

MAKE CERTAIN THAT THE TAPE USED DOES NOT CONTAIN INFORMATION THAT MUST NOT BE DESTROYED. THIS PROCEDURE WILL OVERWRITE ANY EXISTING DATA ON THE TAPE.

d. Observe the waveform on the oscilloscope.

e. Adjust trim-pot R2 until waveform has flat tops and bottom or until the peaks on the leading and trailing edges are minimized.

f. Check INTER-RECORD GAP for proper length. (Refer to Paragraph 5.3.2.5).

5.3.1.3 700 and Greater Steps per Second Adjustment Procedure. (See Schematic 100259 - Capstan Drive, Multi-Speed.)

a. Set the gain of oscilloscope at 1 volt/cm and connect to test point 4.

b. Set the pulse generator to 100 Hz and connect to WRITE STEP command pin of interface connector. (Refer to Paragraph 1.6.1 Slow Interface or Paragraph 1.6.3 DTL Interface for required pulse specification and to Figure 2-1 Slow Interface or Figure 2-2, DTL Interface for appropriate WRITE STEP command interface pin.)

c. Bring transport to READY status.

NOTE

MAKE CERTAIN THAT THE TAPE DOES NOT CONTAIN INFORMATION THAT MUST NOT BE DESTROYED. THIS PROCEDURE WILL OVERWRITE ANY EXISTING DATA ON THE TAPE.

d. Observe the waveform on the oscilloscope.

e. Adjust trim-pot R16 (upper) until rise time of waveform is 1.3 milliseconds.

f. Set the pulse generator to run the transport at 10 percent above its rated speed e.g., 770 steps per second for the 700 steps per second transport.

g. Adjust trim-pot R21 (lower) until a triangular waveform with a flat top is observed. The amplitude of the waveform should be approximately 0.3 volts.

NOTE

AT NO TIME DURING A CAPSTAN REVOLUTION SHOULD THE VOLTAGE OF THE WAVEFORM EVER DROP SHARPLY.

h. Set pulse generator to 100 Hz.

i. Connect oscilloscope to test point 2 and observe waveform.

j. Adjust trim-pot R16 (upper) until waveform has flat top and bottom or until the peak on the leading and trailing edge is minimized.

k. Check INTER-RECORD GAP for proper length. (Refer to Paragraph 5.3.2.5.)

5.3.2 Gapping. Adjustment of the FILE GAP affects the setting of the Inter-Record Gap. After adjustment of the FILE GAP is accomplished, it is necessary to perform the procedure outlined in Paragraph 5.3.2.5.

5.3.2.1 Required Test Equipment.

Pulse Generator

Pulse Counter

5.3.2.2 FILE GAP Adjustment Procedures for Transports Using Multi-Speed Capstan Drive.

a. Connect pulse counter to test point 3 of J202 (Capstan Drive Circuit Board. See Schematic 100259).

b. Bring transport to READY status.

c. Depress FILE GAP control switch.

d. Pulse counter will display the number of encoder pulses generated. Adjust trim-pot R38 of J203 (Function Control Circuit Board. See Schematic 100223) until counter indicates the number of required pulses for the specific transport as shown in the following chart.

TRANSPORT DENSITY	REQUIRED NUMBER OF ENCODER PULSES
200 BPI	450 ± 13
556 BPI	1250 ± 35
800 BPI	1755 ± 50

e. Perform INTER-RECORD Adjustment Procedures, Paragraph 5.3.2.5.

5.3.2.3 FILE GAP Adjustment Procedures for Transports Using Slow-Speed Capstan Drive. Adjustment for transports using Slow-Speed Capstan Drive is identical to transports using Multi-Speed Capstan Drive except for step a. Pulse counter is connected to test point 1 of J202 (Capstan Drive Circuit Board. See Schematic 100133).

5.3.2.4 (Alternate Method). FILE GAP Adjustment Procedures for Transports Using Multi-Speed or Slow-Speed Capstan Drive.

a. Remove trim from transport. (Refer to Paragraph 2.4.)

b. Bring transport to READY status.

c. Using left edge of head as a reference point, mark tape with a pencil.

d. Depress FILE GAP control switch.

e. Mark tape with pencil using same reference point.

f. Repeat steps d. and e. three or four times.

g. Measure distance between each pencil mark. If distance is not consistantly 4.50 ±1/8 inches, adjust trim-pot R38 of J203 (Function Control Circuit Board. See Schematic 100223.)

h. Repeat steps d. through g. until required tape displacement is achieved.

i. Perform INTER-RECORD GAP Adjustment Procedures, Paragraph 5.3.2.7.

5.3.2.5 INTER-RECORD GAP Adjustment Procedures for Transports Using Multi-Speed Capstan Drive.

a. Set pulse generator to 1 (one) Hz, single step, and connect to INTER-RECORD GAP command pin of interface connector. (Refer to Paragraph 1.6.1, Slow Interface or Paragraph 1.6.3, DTL Interface for required pulse specification and to Figure 2-1, Slow Interface or Figure 2-2, DTL Interface for appropriate INTER-RECORD GAP command interface pin.)

b. Connect pulse counter to test point 3 of J202 (Capstan Drive Circuit Board. See Schematic 100259.)

c. Bring transport to READY status.

d. Apply a single pulse from pulse generator.

e. Pulse counter will display the number of encoder pulses generated. Adjust trim-pot R36 of J203 (Function Control Circuit Board. See Schematic 100223) until counter indicates the number of required pulses for the specific transport as shown in the following chart.

TRANSPORT DENSITY	REQUIRED NUMBER OF ENCODER PULSES
200 BPI	75 ± 6
556 BPI	208 ± 17
800 BPI	300 ± 25

5.3.2.6 INTER-RECORD GAP Adjustment Procedures for Transports Using Slow-Speed Capstan Drive. Adjustments for transports using Slow-Speed Capstan Drive is identical to adjustment for transports using Multi-Speed Capstan Drive except for step a. Pulse counter is connected to test point 1 of J202 (Capstan Drive Circuit Board. See Schematic 100133).

5.3.2.7 (Alternate Method) INTER-RECORD GAP Adjustment Procedures for Transports Using Multi-Speed or Slow-Speed Capstan Drive.

a. Remove trim from transport. (Refer to Paragraph 2.4.)

b. Bring transport to READY status.

c. Set pulse generator to 1 (one) Hz, single step, and connect to INTER-RECORD GAP command pin of interface connector. (Refer to Paragraph 1.6.1, Slow Interface or Paragraph 1.6.3, DTL Interface for required pulse specification and to Figure 2-1, Slow Interface or Figure 2-2, DTL Interface for appropriate INTER-RECORD GAP command interface pin.)

d. Using left edge of head as a reference point, mark tape with a pencil.

e. Apply a single pulse from pulse generator.

f. Mark tape with pencil using same reference point.

g. Repeat steps e. and f. three or four times.

h. Measure distance between each pencil mark. If distance is not 3/4 ± 1/16 inches, adjust trim-pot R36 of J203 (Function Control Circuit Board, See Schematic 100223).

i. Repeat steps d. through h. until required tape displacement is achieved.

5.3.3 Reel Servo Potentiometers. The adjustment procedures are applicable to both the take-up and supply servo potentiometers. The potentiometers are located directly behind the shaft of the respective tension arm.

CAUTION

MAKE CERTAIN THAT TAPE USED DURING THIS ADJUSTMENT DOES NOT CONTAIN INFORMATION THAT MUST NOT BE DESTROYED. THIS PROCEDURE WILL ERASE ANY EXISTING DATA ON THE TAPE.

5.3.3.1 Reel Servo Potentiometer Adjustment Procedures.

a. Bring transport to READY status.
b. Using a 3/32 Allen wrench, loosen Allen screws securing clamps to potentiometer housing.
c. Depress LOAD FWD control switch and keep depressed.
d. Turn housing of potentiometer in appropriate direction until tension arm is operating in the approximate center of the slotted area.
e. Release LOAD FWD control switch.
f. Momentarily depress REWIND control switch.
g. If transport operates in REWIND mode, depress POWER switch and tighten Allen screws securing clamps to potentiometer housing. If the transport does not operate in REWIND mode continue to step h.
h. Turn housing of take-up potentiometer 1 or 2 degrees in the counter clockwise direction.

i. Bring transport to READY status.

j. Repeat steps f. through h. until transport operates in REWIND mode.

5.3.4 BOT Photo Sensor Amplifier

5.3.4.1 Required Test Equipment

Multimeter

5.3.4.2 Adjustment Procedure.

a. Bring transport to READY status.

b. Making certain the BOT tab is not over Photo Senser, connect multimeter to TP1 of J203 (Function Control Circuit Board. See Schematic 100223).

c. Adjust trimpot R15 for +3 volts.

d. Bring BOT tab over Photo Sensor.

e. Voltage should drop to less than +0.4 volt.

5.3.5 EOT Photo Sensor Amplifier. Adjustment of EOT Photo Senser Amplifier is identical to BOT adjustment except that voltage is measured at TP2 and adjusted by trimpot R31.

5.3.6 Power Supply

5.3.6.1 Required Test Equipment

VTVM

5.3.6.2 Adjustment Procedures.

NOTE

MAKE CERTAIN THAT TRANSPORT DOES NOT CONTAIN ANY OTHER CIRCUIT BOARD THAN J201.

a. Depress POWER control.

b. Connect VTVM to TP1 (ground on TP3) of J201 (Reel Servo and Voltage Regulator Circuit Board. See Schematic 100128)

c. Adjust trimpot R36 for +5 ± 0.05 volts.

d. Connect VTVM to TP2 (ground on TP3) of J201.

e. Adjust trimpot R37 for -5 ± 0.05 volts.

5.3.7 Parity Selection. To select desired parity, align slot of S1 (Receiver, Slow Interface Circuit Board. See Schematic 100248 or Receiver, DTL Interface Circuit Board. See Schematic 100333) with appropriate letter etched on circuit board.

O - ODD Parity (internally generated)

E - EVEN Parity (internally generated)

X - Externally Supplied Parity

5.3.8 Echo Check Parity Selection. To select desired parity generated from the Echo Check signals, align slot of S1 (Echo Check Parity Circuit Board. See Schematic 100363) with appropriate letter etched on circuit board.

O - ODD Parity

E - EVEN Parity

5.4 Mechanical Adjustments.

5.4.1 Reel Servo Belt Tension. The belts should not be over-tightened or low motor bearing life and over-heating will result. Tension is applied by loosening the four screws retaining the reel motor, moving the motor until the belt is at the required tension and tightening the screws. The force required to rotate a reel hub should lie between 18 and 20 ounces. This measurement is made by wrapping a line several times around the rubber retaining ring and measuring the force required to rotate the reel hub with a spring balance or force gauge.

5.4.2 Tape Path Guide Alignment. All tape guiding elements in the tape path are referenced to the outer edge of the head guides. It is assumed that the tension arm spring tension has been set up as in Section 5.4.3.

5.4.2.1 Fixed Guides. With the trim removed, measure distance to outer tape-guiding edge of each head guide from the tape deck. These measurements will normally be within 0.001 inches of each other. Measure the distance from tape deck to the outer tape-guiding edge of the supply and take-up fixed guides. Shim the guides between the guide post and roller to within 0.002 inches of the head guide dimensions. This places the outer edge of all fixed guides the same distance from the tape deck.

5.4.2.2 Tension Arm Guides. With the trim removed from the deck, the tension arms should be rotated so that the tape guides are as nearly as possible perpendicular to the tape deck and secured. The reel retainer hubs should be positioned so that reel locating edge is located 0.625 ± 0.005 inches from the tape deck. Secure the reel retainer hubs with the two set screws on the shaft flats.

5.4.2.2.1 Supply Tension Arm Guide. Remove the head retaining screws and move the head from between the head guides. Lay a 6-inch steel scale across the head guides as shown in Figure 5-1. The scale should preferably be narrower than 1/2 inch so that it can easily be held against the outer edges of the guides at A and B. The tension arm guide-shaft set screw is loosened and the guide positioned so that the outer edge lines up with the scale. Secure the guide-shaft set screw and replace the head.

5.4.2.2.2 Take-up Tension Arm Guide. Lay a 6 inch steel scale across the fixed guides as shown in Figure 5-2. The scale should be held against the outer edge of the guides. Rotate the take-up tension arm counter-clockwise until the roller contacts the guide. Move the guide so that the outer edge lines up with the scale. Secure the guide shaft set screw.

5.4.2.2.3 Guide Perpendicularity. The head is replaced and tape threaded in the normal path. Power is turned on and the final adjustment is made to the tension arm guide perpendicularity by running the tape and noting the tension distribution across the tape at the tension arm rollers. When the guides are perpendicular, the tape has an even tension across the guide with no buckling at the flanges. After adjustment, secure tension arm very tightly to ensure no rotation during operation.

CAUTION

USE EXTREME CARE TO AVOID CONTACT WITH THE HEAD AND GUIDES WHEN REPLACING TRIM.

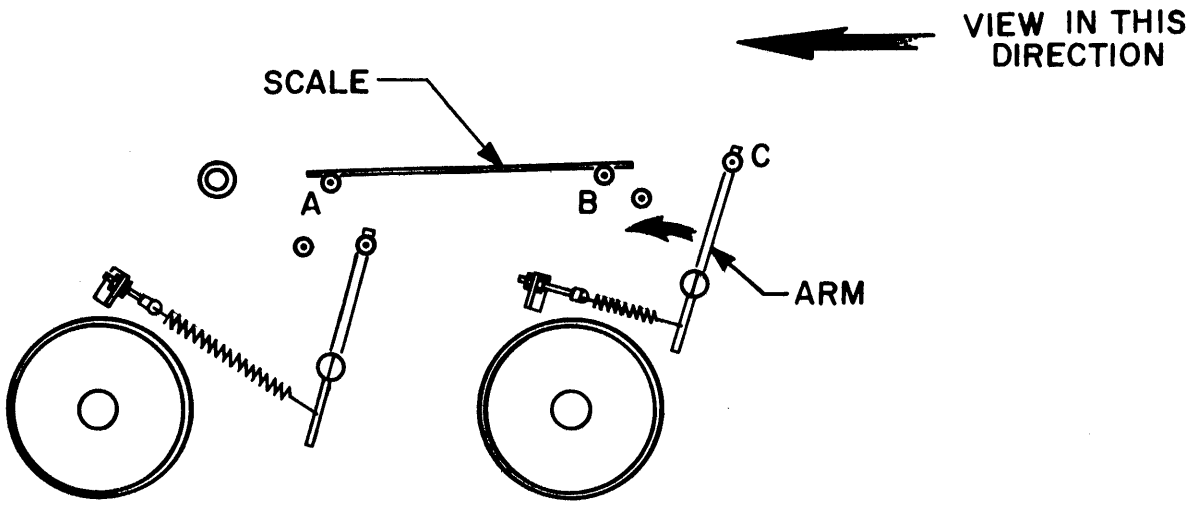


FIGURE 5-1. SUPPLY TENSION SPRING MEASUREMENT

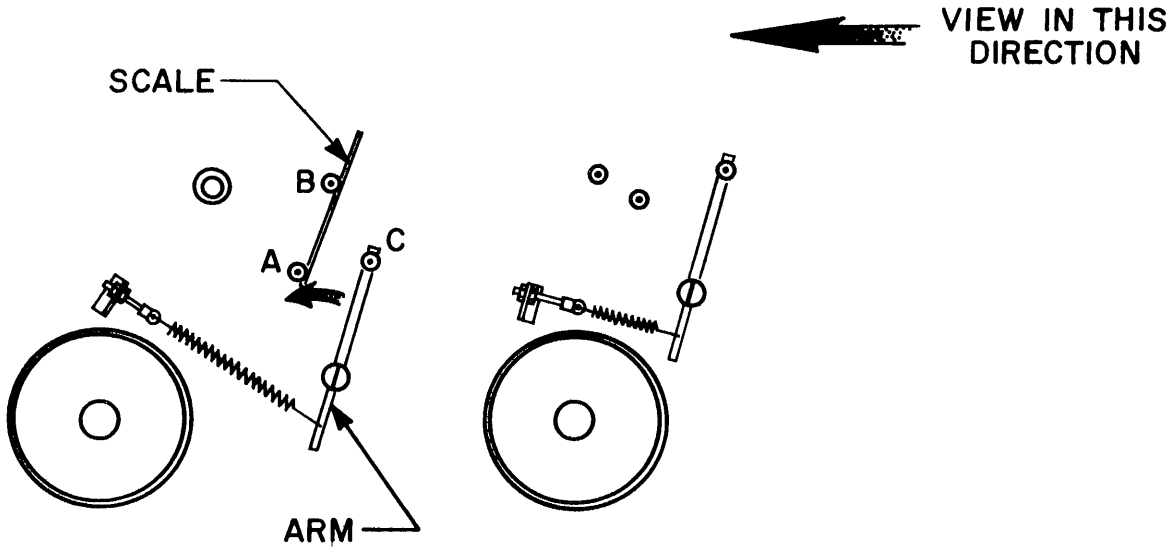


FIGURE 5-2. TAKE-UP TENSION SPRING MEASUREMENT

5.4.3 Tape Tension.

5.4.3.1 Supply Tension Arm. With the trim removed from the deck, thread a loop of tape as shown in Figure 5-3. Using a force gauge, measure the force required to pull the tension arm off its backstop and slowly through its stroke. The force required should not vary by more than a total of 0.3 ounces as the motion of the arm is slowly reversed at any part of the stroke. Adjust the spring tension screw, A, until the average force, as measured above, is 8 ounces. Tighten the lock nuts.

5.4.3.2 Take-Up Tension Arm. Thread the tape as shown in Figure 5-4. Using a force gauge, measure the force required to pull the tension arm off the backstop and slowly through its stroke. The force required should not vary by more than a total of 0.3 ounces as the motion of the arm is slowly reversed at any point of the stroke. Adjust the spring tension screw, A, until the average force as measured above is 9 ounces. Tighten the lock nuts. Tension should be adjusted with the transport oriented in the direction of intended use.

5.4.4 Limit Switch (Take-Up Tension Arm). In normal operation this switch is closed, shorting the inputs. When the take-up tension arm is resting on its backstop, or at the other end of its stroke, the switch should be open indicating that the tension arm is out of the normal operating region. The cam on the tension arm shaft should be positioned so that the switch roller is moved enough to open the switch just before the tension arm contacts the backstop. A pin prevents the switch roller from contacting the cam surface when the tension arm is in the normal operating area. The over-size mounting holes for the switch are used to position the switch so that it is

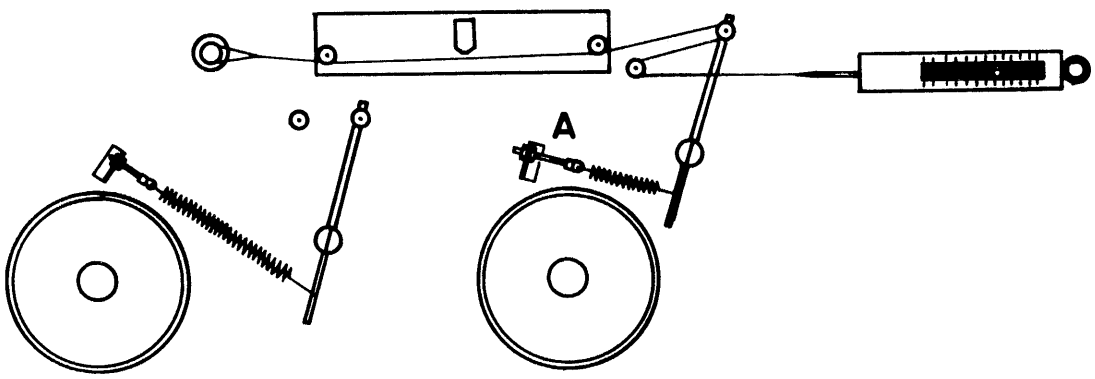


FIGURE 5-3. SUPPLY TENSION ARM GUIDE ADJUSTMENT

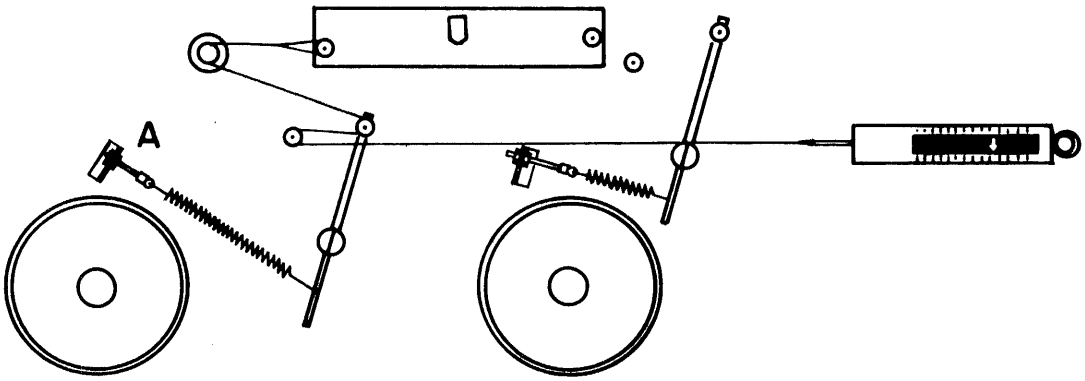


FIGURE 5-4. TAKE-UP TENSION ARM GUIDE ADJUSTMENT

positively closed in the normal operating region and is opened before the arm reaches the limits of its stroke. Care should be taken to see that the cam does not contact the roller in a line drawn along the lever and through the center of the roller.

5.5 Mechanical Maintenance. The tape transport is designed to operate with a minimum of maintenance and adjustments. Replacement of parts is designed to be as simple as possible. Repair equipment needed is kept to a minimum, and only simple tools are required in most cases. Paragraph 5.6 lists tools required to maintain the tape transport.

5.5.1 Preventive Maintenance Schedule. To assure that the transport operates at its design potential and to assure long life, a program of planned preventive maintenance is recommended. A suitable schedule is shown in Table 5-1.

5.5.2 Cleaning the Transport. The transport requires cleaning in three major areas: head and head guides, capstan, and Delrin roller guides.

To clean the head and head guides, use a lint-free cloth or cotton swab moistened in head cleaner solvent. Wipe the heads carefully to remove all accumulated oxide and dirt.

CAUTION

ROUGH OR ABRASIVE CLOTHS SHOULD NOT BE USED TO CLEAN THE HEAD AND HEAD GUIDES. USE ONLY ISOPROPYL ALCOHOL. OTHER SOLVENTS, SUCH AS CARBON TETRACHLORIDE, MAY RESULT IN DAMAGE TO THE HEAD LAMINATION ADHESIVE.

MAINTENANCE OPERATION	FREQUENCY (HOURS)	QTY TO MAINTAIN	TIME REQD (MINS)	MANUAL SECTION
Clean Transport	16 (or end of operating day)		5	5.5.2
Check Roller Guides	While cleaning	4	3	
Check Capstan Surface	While cleaning	1	2	
Check Tape Tracking	200		5	5.4.2.2.2
Check Tape Tension	500		15	5.4.3
Replace Reel Motor	5,000	2	10	5.4.1
Replace Capstan Drive Assy	10,000	1	10	

TABLE 5-1. PREVENTIVE MAINTENANCE SCHEDULE

To clean the capstan, use only a cotton swab moistened with isopropyl alcohol to remove accumulated oxide and dirt.

To clean the Delrin roller guides, use a lint-free cloth or cotton swab moistened in isopropyl alcohol. Wipe the guide surfaces carefully to remove all accumulated oxide and dirt.

CAUTION

DO NOT SOAK THE GUIDES WITH EXCESSIVE SOLVENT. EXCESSIVE SOLVENT MAY SEEP INTO THE PRECISION GUIDE BEARINGS, CAUSING CONTAMINATION AND A BREAKDOWN OF THE BEARING LUBRICANT.

5.6 Maintenance Tools. The following list of tools is required to maintain the tape transport:

Socket wrench set for 4-40, 10-32 cap screws
Socket wrench set for 4-40, 6-32, 10-32 set screws
Splined socket wrenches for 4-40, 6-40, set screws
Open end wrenches for 3/16", 1/4", 5/16", 3/8" bolts
Long-nose pliers
Phillips screwdriver set
Standard screwdriver set
Soldering aid
Soldering iron
1 pound force gauge
Lint-free cloth
Cotton swabs
Isopropyl alcohol

5.7 Trouble Shooting. Table 5-2. System Trouble-Shooting Chart provides a means of isolating faults, the possible causes and the remedies. The Trouble Shooting Chart is used in conjunction with the schematic, part lists and wiring diagrams located in Section VI.

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Tape does not tension and capstan shaft rotates freely when LOAD FWD is depressed for the first time	Interlock relay K201 does not close	Check operation of relay. Replace if necessary	Schematic 100338
	LOAD FWD switch S103 not operative	Check operation of switch. Replace if necessary	Schematic 100338
	Relay driver defective	With POWER on, check for a maximum of 0.5V at Pin E. If greater replace defective relay driver component.	Schematic 100133 or Schematic 100259
Tape tension is present when LOAD FWD control is depressed but is removed when control is released	Limit switch S101 not operative	Replace switch if defective	Schematic 100338
	Limit switch S101 not adjusted properly	Adjust switch	Paragraph 5.4.4
Tapr runs away when LOAD FWD control is depressed or Tape speed is excessive	Fuse XF202 blown	Replace fuse	Paragraph 5.2.1
	No tachometer feedback	Check resistance between pins 7 and 8 of TB301 for approximately 150 ohms. Replace entire capstan assembly if tachometer is defective.	Schematic 100338
		Check ramp generator for proper output. Replace defective component	Schematic 100133 or Schematic 100259 Paragraph 4.2.2

TABLE 5-2. SYSTEM TROUBLE-SHOOTING

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Tape unwinds or Tension armhits stops when LOAD FWD control is depressed	Tape improperly threaded	Rethread tape	Paragraph 3.2.1
	No +5V at pin 4 of J201	Repair or replace Reel Servo Circuit Board	Schematic 100128
Tape continues to run when BOT tab reaches photo sensor.	BOT tab dirty or tarnished	Replace tab or increase sensitivity of photo tab amplifier	Paragraph 5.3.2
	Photo sensor not properly adjusted	Adjust photo sensor	Paragraph 5.3.2
	Photo sensor or amplifier defective	Check for approximately +3.7V at pin D of J203 with tab not over photo sensor. Repair or replace defective parts	Schematic 100223 Paragraph 5.3.2
Transport does not respond to WRITE STEP command	Interface cable defective	Repair or replace cable	
	Receiver defective	Check relevant receiver test point. Repair or replace J205	Schematic 100248 or Schematic 100333
	Double buffer, write amplifier defective	Check relevant write amplifier test point. Repair or replace J206	Schematic 100233 or Schematic 100238

TABLE 5-2. SYSTEM TROUBLE-SHOOTING (Continued)

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Transport responds to WRITE STEP command but tape is not written	Write current not enabled	With transport in READY state, check for -5V at TP3 of J203.	Schematic 100223
	Double buffer, write amplifier defective	With all receiver outputs tied to 0 Volts and external WRITE STEP commands, check that waveforms at write amplifier output test points alternate between +5V and -5V.	Schematic 100248 or Schematic 100333 Schematic 100233 or Schematic 100238
Parity is written incorrectly	Parity generator switch set incorrectly on J205	Set switch to correct output.	Schematic 100248 or Schematic 100333 Paragraph 5.3.6
Transport does not read back correctly	Incorrect data format	Use correct format	IBM Form A22-6589-3 (729 or 727 Series) or IBM Form A22-6866-3 (2400 Series)
	Record length too long	Check available computer memory.	

TABLE 5-2. SYSTEM TROUBLE-SHOOTING (Continued)

SECTION VI - SCHEMATICS, PART LISTS, AND WIRING DIAGRAMS

6.1 Introduction. Table 6-1 lists the schematics for the Incremental Write Transport. These schematics are presented in the same order as listed in Table 6-1.

Table 6-2 is a Part Number Cross Reference that lists the manufacturer's part number in reference to PEC part numbers.

INCREMENTAL WRITE PCBA'S

TITLE	SCHEMATIC NUMBER	PCBA NUMBER
Reel Servo and Voltage Regulator	100128	100129
Capstan Drive, Low Speed	100133	100134
Capstan Drive, Multi-Speed	100259	100260
Function Control	100223	100224
Transmitter, Slow Interface	100253	100254
Transmitter, DTL Interface	100338	100339
Receiver, Slow Interface	100248	100249
Receiver, DTL Interface	100333	100334
Double Buffer Write Amplifier	100233	100234
Double Buffer, 9-Channel Write Amplifier	100238	100239
Quad Buffer, Write Amplifier		
Echo Check Parity	100363	100364
CRC Generator	100264	100265
GENERAL		
Schematic - Power and Harness Wiring	100388	
Wiring Diagram - Incremental Write, Slow Interface, Echo Check	100496 or 100756	
Wiring Diagram - Incremental Write, DTL Interface, Echo Check	100493 or 100757	
Wiring Diagram - Incremental Write, Slow Interface, Echo Check and CRC	100497 or 100758	
Wiring Diagram - DTL, Slow Interface, Echo Check and CRC	100494 or 100759	

TABLE 6-1. LIST OF SCHEMATICS

PEC Part Number	MANUFACTURER (or equivalent)	Description or Part No.*
Carbon Comp. Resistors		
101 - 1525	Allen Bradley, Speer, Stancore	RC20 (1500 ohms, 5%, 1/2 W)
102 - 1525		RC32 (1500 ohms, 5%, 1 W)
107 - 1525		RC42 (1500 ohms, 5%, 2 W)
Precision Resistor		
104 - 2612	Corning, IRC	RL20C, (26100 ohms, 1%, 1/4 W)
Variable Resistors		
121 - 1010	Beckman Helipot	79PR100, (100 ohms, 3/4 W 10%)
121 - 1020		79PR1K, (1000 ohms, 3/4 W, 10%)
Dipped Mica Capacitors		
130 - 1515	El Menco	CM05CJ03 (150 pF, 500v, 5%
Mylar Capacitors		
131 - 1540	Cornell - Dubilier	WMF1P15 (0.15 uF, 100v, 10%)
Solid Tantalum Capacitors		
132 - 2752	Kemet	TK2R7W35 (2.7 uF, 35v, 20%)
Aluminum Electrolytic Capacitors		
133 - 7060	Mallory	MTA70E20 (70 uF, 20v, -10 +100%

*For resistors and capacitors typical part numbers only are shown.

TABLE 6-2. PART NUMBER CROSS REFERENCE

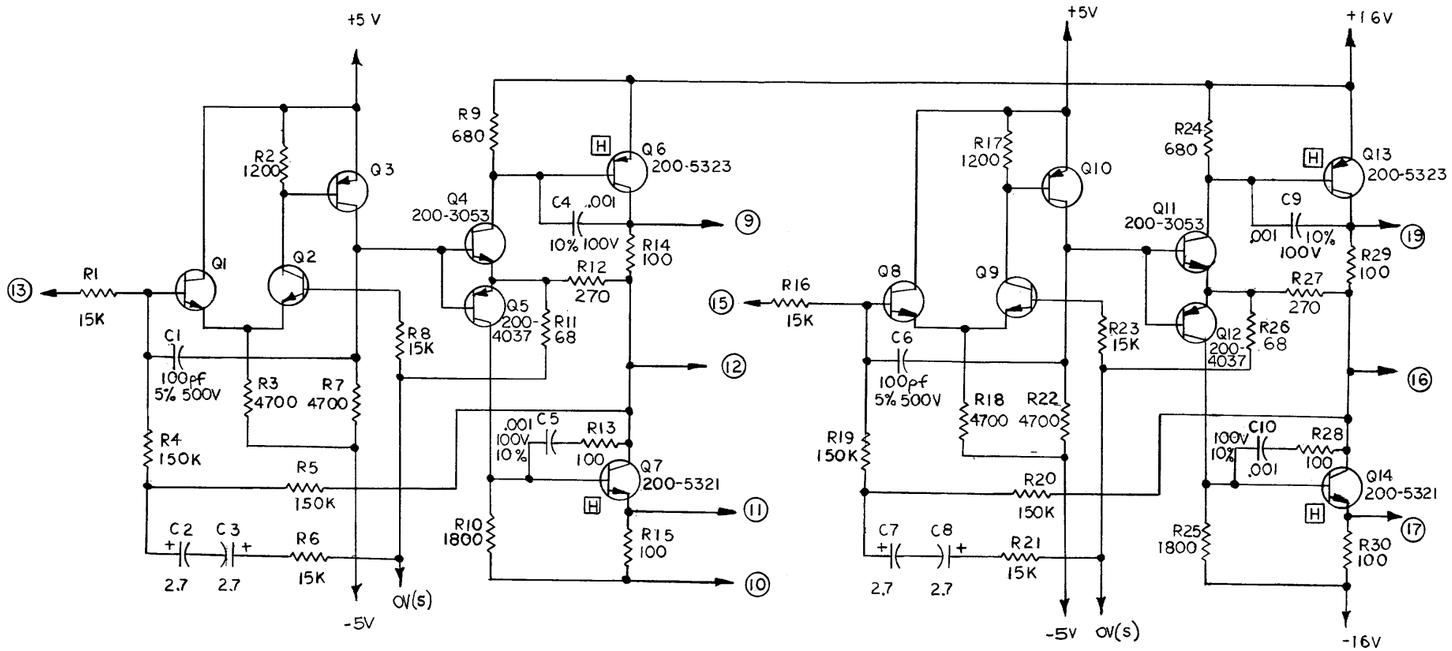
PEC Part Number	MANUFACTURER (or equivalent)	Description or Part No.*
Transistors		
200 - 4123	Motorola	2N4123 (npn switching)
200 - 4125	Motorola	2N4125 (pnp switching)
200 - 3053	RCA	2N3053 (npn T05, medium power)
200 -4037	RCA	2N4037 (pnp, T05, medium power)
200 - 3055	RCA	2N3055 (npn, T03, power)
Diodes		
300 - 4446	TI	1N4446 (logic diode)
Rectifier Bridge		
320 - 9622	Motorola	MDA 962-2 (100v, 10A)
Zener Diodes		
330 - 0685	Motorola	1N4736A (6.8v, 5%)
330 - 1005	Motorola	1N4740A (10.0v, 5%)
OP Amplifier		
400 - 1435	Motorola	MC1435P
Digital IC		
700 - 8360	Fairchild	U6A993659
700 - 8440	Fairchild	U6A994459
700 - 8450	Fairchild	U6A994559
700 - 8460	Fairchild	U6A994659
700 - 8520	Fairchild	U6A995259

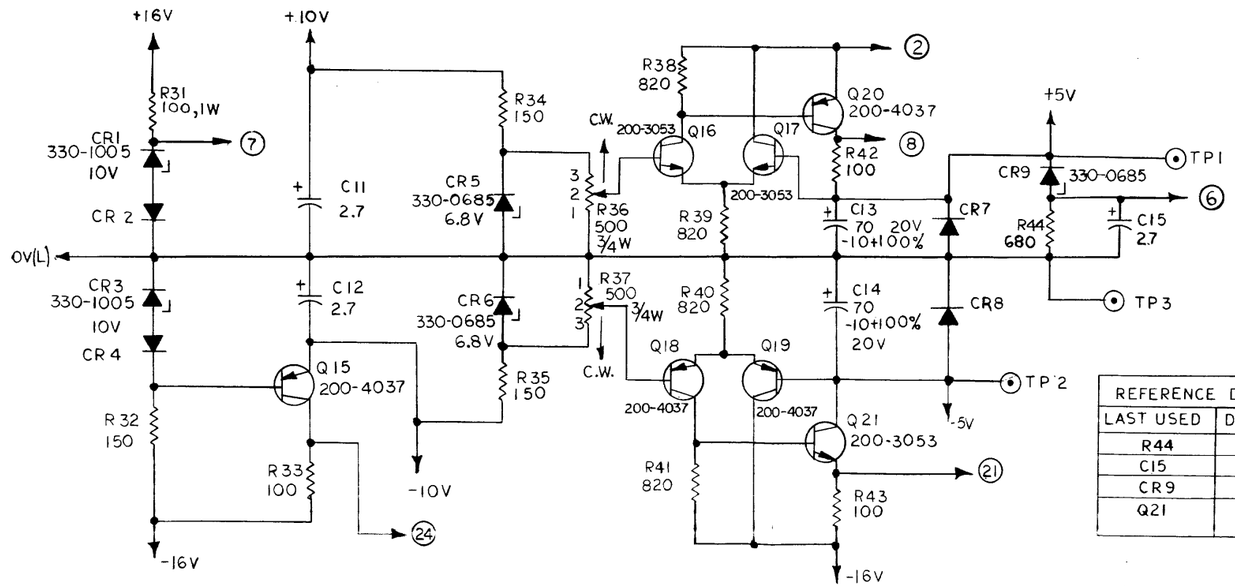
*For resistors and capacitors typical part numbers only are shown.

TABLE 6-2. PART NUMBER CROSS REFERENCE (Continued)

DATE	ITR	REVISION RECORD	AUTH.	DR.	CK.
11/28/67	F	ECN 1-847	[illegible]	[illegible]	[illegible]
12/8/67	G	ECN 119	[illegible]	[illegible]	[illegible]
1/26/68	H	ECN 316	TCL	JT	[illegible]

+16V	A	1
PWR. SUP. COL. (+5)	B	2
+10V	C	3
+5V	D	4
0V(L)	E	5
0/V OUTPUT	F	6
PWR. SUP. BASE (+10)	H	7
PWR. SUP. BASE (+5)	J	8
T.U. BASE (POS.)	K	9
T.U. EMIT. (NEG.)	L	10
T.U. BASE (NEG.)	M	11
T.U. OUTPUT	N	12
T.U. POT.	P	13
0V(S)	R	14
SUP. POT.	S	15
SUP OUTPUT	T	16
SUP. BASE (NEG.)	U	17
	V	18
SUP. BASE (POS)	W	19
	X	20
PWR. SUP. BASE (-5)	Y	21
	Z	22
	$\overline{A}$	23
PWR. SUP. BASE (-10)	$\overline{B}$	24
0V(L)	$\overline{C}$	25
-5V	$\overline{D}$	26
-10V	$\overline{E}$	27
-16V	$\overline{F}$	28





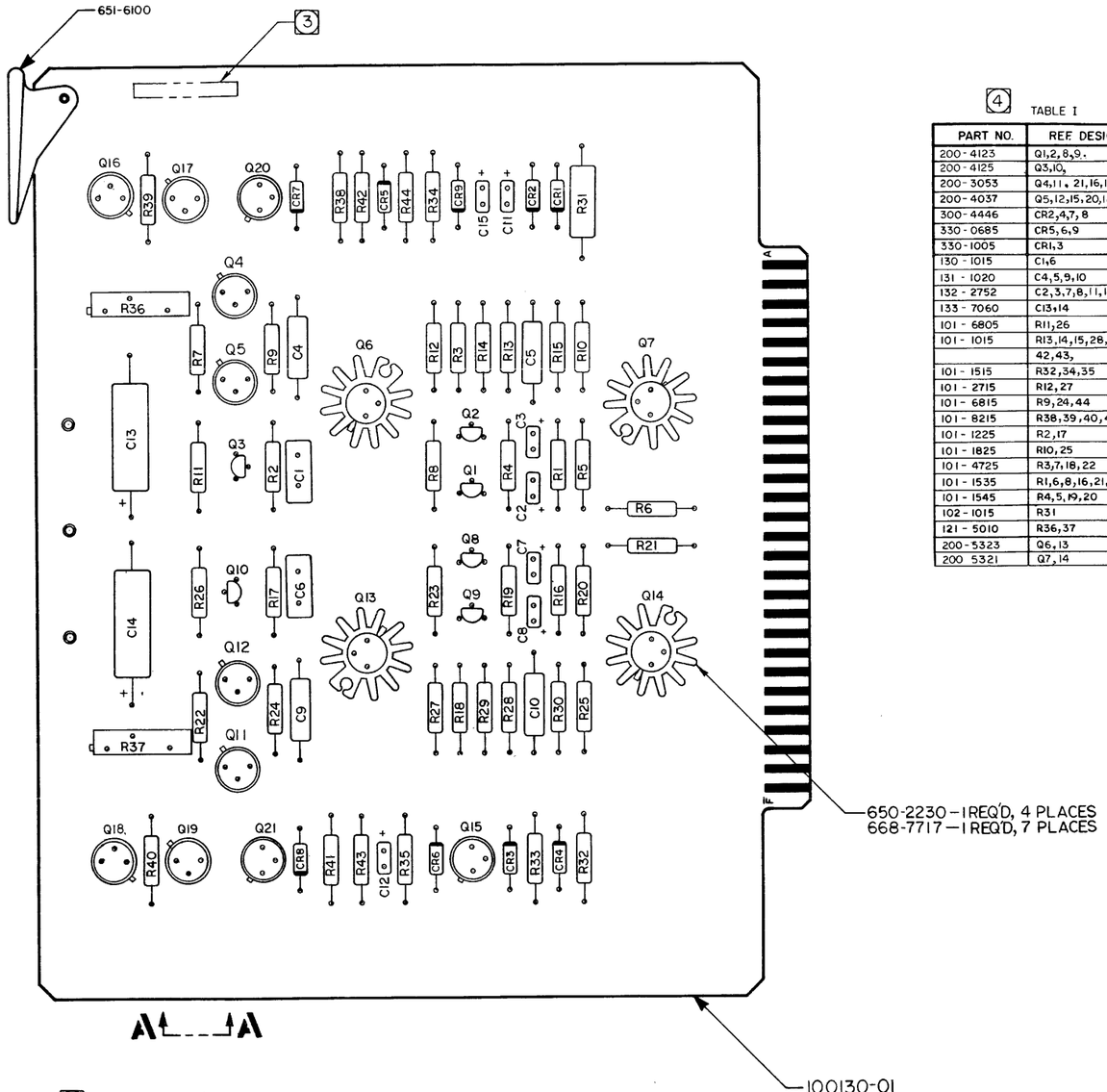
REFERENCE DES.	
LAST USED	DELETED
R44	
C15	
CR9	
Q21	

8. SCHEMATIC APPLIES TO 100129-01.
7. [H] INDICATES HEAT SINK.
6. FOR ASSY. DRAWING SEE 100129.
5. ALL PNP TRANSISTORS 200-4125.
4. ALL NPN TRANSISTORS 200-4123.
3. ALL DIODES ARE 300-4446.
2. ALL CAPACITORS IN MICOFARADS, 20%, 20V
1. ALL RESISTORS IN OHMS, ±5%, ½WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±	SCALE	DRAWN BY [illegible]	
FRACTIONAL ±		APPROVED BY [illegible]	
ANGULAR ±	TITLE SCHEMATIC: REEL SERVO & VOLTAGE REGULATOR		
100129 | 1000 SERIES	DATE 11-17-67	DRAWING NUMBER 100128	ISSUE H
NEXT ASSY | 1ST USED ON			

DATE	BY	REVISION RECORD	AUTH.	DR	CK
8-2	A	I-EM	YM	MK	MK
10-28	B	ECN 316	TC	MK	MK

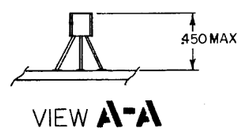


4 TABLE I

PART NO.	REF DESIGNATION
200-4123	Q1,2,8,9.
200-4125	Q3,10,
200-3053	Q4,11, 21,16,17
200-4037	Q5,12,15,20,18,19
300-4446	CR2,4,7,8
330-0685	CR5,6,9
330-1005	CR1,3
130-1015	C1,6
131-1020	C4,5,9,10
132-2752	C2,3,7,8,11,12,15
133-7060	C13,14
101-6805	R11,26
101-1015	R13,14,15,28,29,30,33,
	42,43,
101-1515	R32,34,35
101-2715	R12,27
101-6815	R9,24,44
101-8215	R38,39,40,41
101-1225	R2,17
101-1825	R10,25
101-4725	R3,7,18,22
101-1535	R1,6,8,16,21,23
101-1545	R4,5,19,20
102-1015	R31
121-5010	R36,37
200-5323	Q6,13
200 5321	Q7,14

TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09



VIEW A-A

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

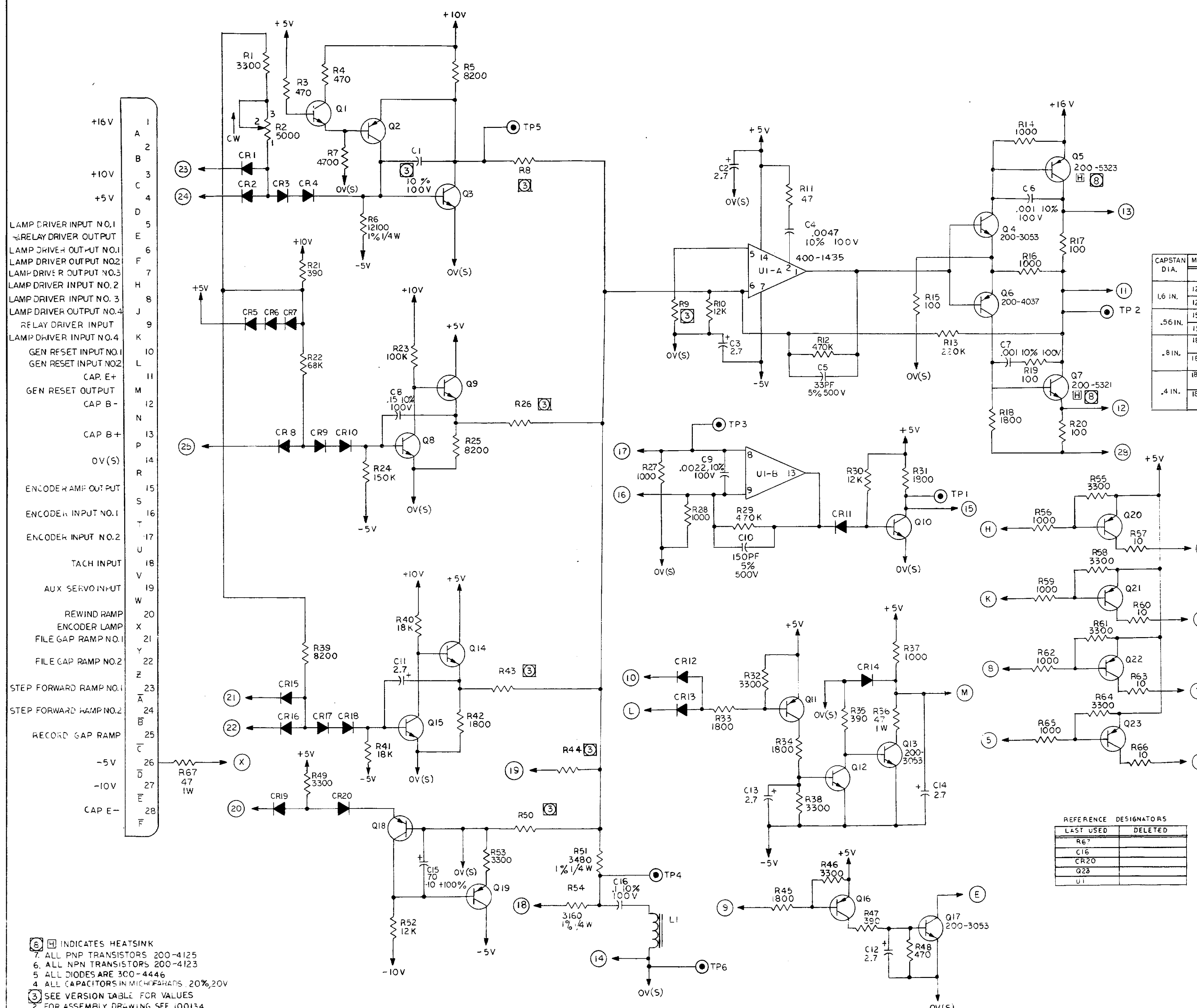
3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100128
SPEC-100132

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE 2/1	DRAWN BY
FRACTIONAL ±	TITLE PCBA REEL SERVO VOLTAGE REGULATOR		SHEET 1 OF 1
ANGULAR ±	DATE	DRAWING NUMBER 100129	ISSUE B



VERSION TABLE

CAPSTAN DIA.	MODEL	ASSEMBLY	R8	R9	R26	R43	R44	R50	C1
1.6 IN.	1203	100134-01	162K,1%	2200	15 K	33 K	22 K	4700	.15
	1205	-02	121K,1%	2200	15 K	33 K	22 K	4700	.1
.56 IN.	1503	-03	162K,1%	1800	5600	12 K	8200	1800	.15
	1505	-04	121K,1%	1800	5600	12 K	8200	1800	.1
.8 IN.	1803-7 -9	-05	316K,1%	1800	8200	18 K	12 K	2700	.15
	1805-7 -9	-06	237K,1%	1800	8200	18 K	12 K	2700	.1
.4 IN.	1803-7 -9	-07	162K,1%	1800	4700	10 K	8200	1800	.15
	1805-7 -9	100134-08	121K,1%	1800	4700	10 K	8200	1800	.1

REFERENCE DESIGNATORS

LAST USED	DELETED
R67	
C16	
CR20	
Q23	
U1	

8 H INDICATES HEATSINK
7. ALL PNP TRANSISTORS 200-4125
6. ALL NPN TRANSISTORS 200-4123
5 ALL DIODES ARE 300-4446
4 ALL CAPACITORS IN MICROFARADS 20%,20V
3 SEE VERSION TABLE FOR VALUES
2. FOR ASSEMBLY DRAWING SEE 100134
1 ALL RESISTORS IN OHMS, ±5%, 1/2W

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION
DECIMAL ±	SCALE / DRAWN BY J. ERINGER
FRACTIONAL ±	TITLE SCHEMATIC - CAPSTAN DRIVE, LOW SPEED
ANGULAR ±	DATE 24 JAN 68 / DRAWING NUMBER 100133 / ISSUE F

DATE	SYM	REVISION RECORD	AUTH	CK
7/26/67	B	ERN 1-ER	[illegible]	[illegible]
9/21/67	C	ECN 212	[illegible]	[illegible]
2/5/68	D	ECN 313	[illegible]	[illegible]
4/2/68	E	ECN 350	[illegible]	[illegible]

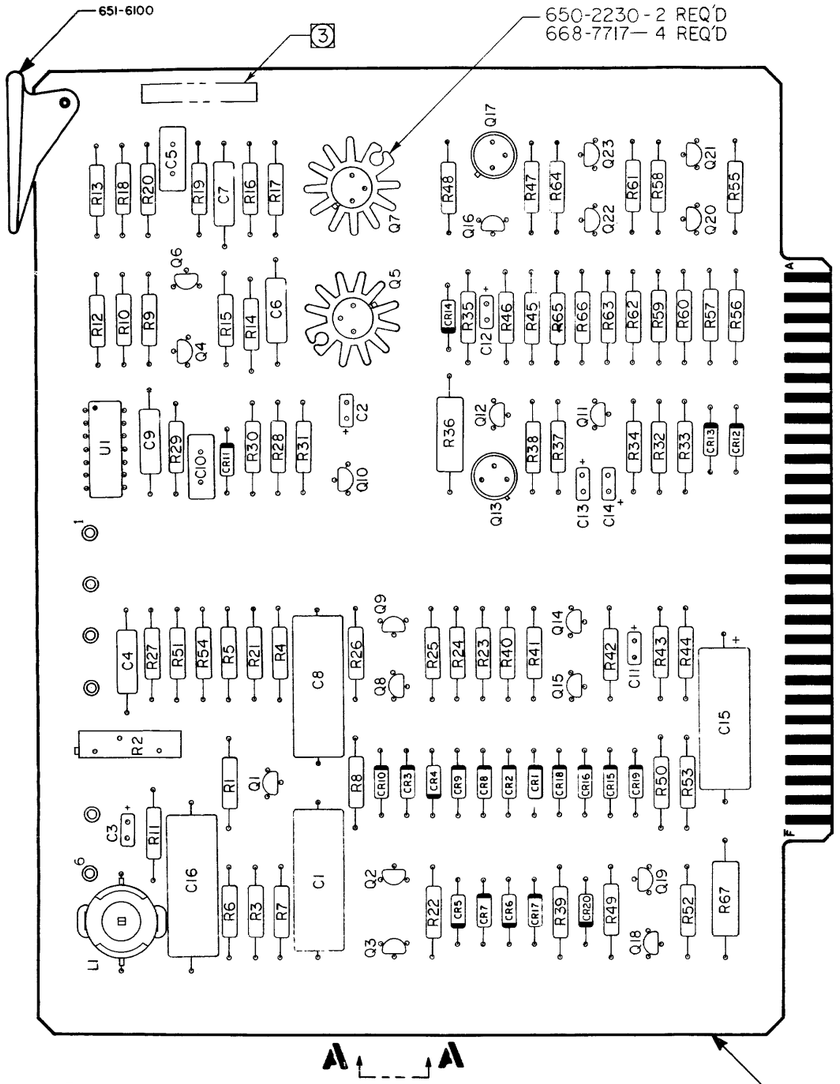
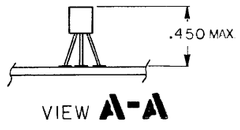


TABLE I (4)

PART NO.	REF DESIGNATION
400-1435	U1
200-4123	Q1,3, 8,9,10, 12,14,15
200-4125	Q2, 11,16,18,19,20,21,22,23
200-3053	Q4,13,17
200-5323	Q5
300-4446	CR1-CR20
130-3305	C5
131-1020	C6,7
131-4720	C4
131-1040	C16
131-1540	C8
132-2752	C2,3,11,12,13,14
133-7060	C15
101-1005	R57,60,63,66
101-4705	R11
101-1015	R15,17,19,20
101-3915	R21,35,47
101-4715	R3,4,48
101-1025	R14,16,27,28,37,56,59,62,65
101-1825	R18,31,33,34,42,45
101-3325	R1,32,38,46,49,53,55, 58,61,64
101-4725	R7
101-8225	R5,25,39
101-1235	R10,30,52
101-1835	R40,41
101-6835	R22
101-1045	R23
101-1545	R24
101-2245	R13
104-3161	R54
104-3481	R51
104-1212	R6
102-4705	R36,67
121-5020	R2
101-4745	R12,29
100212-01	L1
131-2220	C9
130-1515	C10
200-4037	Q6
200-5321	Q7

TABLE II (5)

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL 1203 / VER. -01	1205 -02	1503 -03	1505 -04	1803-7 -9 -05	1805-7 -9 -06	1803 -7 -8 -07	1805 -7 -9 -08	-09
R8	104-1623	104-1213	104-1623	104-1213	104-3163	104-2373	104-1623	104-1213	
R9	101-2225	101-2225	101-1825	101-1825	101-1825	101-1825	101-1825	101-1825	
R26	101-1535	101-1535	101-5625	101-5625	101-8225	101-8225	101-4725	101-4725	
R43	101-3335	101-3335	101-1235	101-1235	101-1835	101-1835	101-1035	101-1035	
R44	101-2235	101-2235	101-8225	101-8225	101-1235	101-1235	101-8225	101-8225	
R50	101-4725	101-4725	101-1825	101-1825	101-2725	101-2725	101-1825	101-1825	
C1	131-1540	131-1040	131-1540	131-1040	131-1540	131-1040	131-1540	131-1040	



(5) FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO'S SEE TABLE II.

(4) FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

(3) RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLY PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC, 100133
SPEC, 100137

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION			
DECIMAL ±		SCALE 2/1	DRAWN BY [illegible]	
FRACTIONAL ±	TITLE PCBA LOW CAPSTAN DRIVE -SPEED			SHEET 1 OF 1
ANGULAR ±	DATE 4-2-68	DRAWING NUMBER 100134		ISSUE E
FINAL ASSY				
NEXT ASSY	USED ON			

EOTI A
LFR 2
EOTO B
TNT 3
EPS C
INTERLOCK 4
+5V D
BOTI 5
OV(L) E
LFNC 6
BOTO F
LFNO 7
WPC H
LFC 8
WPC J
RWNO 9
RYC K
WPC 10
RYNO L
RWR 11
CUR M
RWC 12
CT4 N
WPC ANCHOR POINT P
DBCT 13
BCL R
14
ECC S
15
WLO ANCHOR POINT 16
TRR T
GRS 17
DMC U
RTNI 18
SFL2 V
GIP 19
EEP W
EPW 20
RGR X
FGR 21
FGL Y
EFM 22
ECRC Z
IRGC 23
BIB $\overline{A}$
FGNC 24
FGNO $\overline{B}$
OV(L) 25
EWPC $\overline{C}$
-5V 26
ANHOR POINT $\overline{D}$
27
$\overline{E}$
FGC 28
$\overline{F}$

R1 220 → (3) EPS

→ X (9)

TP14

C1 2.7
C2 2.7
-5V
OV(L)

+5V
R3 4700
R2 180
FGNO (B)
U5-B
U5-A
FGNC (24)
R4 180
R5 4700
C3 .01 100V, 10%
OV(L)

R6 4700
LFNO (F)
R7 180
U1-A
U1-B
R8 180
R9 4700
LFNC (E)
C5 .01 100V, 10%
OV(L)

U3-A

C7 .01 100V, 10%
R10 10K
R11 270
LFC (H)
U1-C
R12 15K
A LFR
U1-D
CR1
X GRS
R18 10K
R19 270
R16 270
R17 15K
C8 .01 100V 10%
OV(L)

R13 120
R14 150
BOTI (D)
R15 5K CW
Q1
R20 270
CR2
X GRS
U3-B

BOTO (6)
U4-A
U4-B
U4-C
U4-D
U3-D
RWR (L)
CR3
GRS X
R21 820
C9 2.7
TP1
-5V
OV(L)

R22 4700
RWNO (J)
R23 180
C10 2.7
OV(L)
RWC (M)

R24 4700
U3-F
U2-C
U2-B
U2-A
CR4
X GRS
U2-D
U3-E
RYNO (10)
R25 180
C11 .01 10% 100V
OV(L)
RYC (9)

(8) TNT
R26 1200
R28 4700
INTERLOCK (C)
CR5
R27 2200
Q2
R29 10K
OV(L)
-5V

+5V
R30 120
R31 K
CW
R32 150
Q3
EOTI (1)
EOTO (7)
TP2
C26 2.7
R33 820
OV(L)
-5V

+5V
TP6
FGC (28)
CR15
U11-C
U11-D
CR22
X GRS

R50 10K
R51 270
C17 .01 100V 10%
U5-C
U5-D
CR16
CR17
X GRS
TP13
R52 15K
OV(L)

R53
C18 .01 100V 10%
R54 270
R55
U6-B
U6-A
R58 270
R57 270
CR18
X GRS
TP12
OV(L)

R56 4700
IRGC (23)
U7-A
U7-B
R60 10K
C20 .01 100V
U6-C
U6-D
R86 270
CR19
X GRS
R61 15K
OV(L)
TP11

BIB ($\overline{A}$)

A
B
R34 2200
R35 2200
Q4
Q5
R41 3300 K
R42 100K
R43 18K
R44 4700
R45 100K
C15 100PF 500V 5%
Q8
OC
Q7
Q6
R37 5110 1%
R39 220
R36 10K
CW
R38 5K CW
R85 220
CR6
CR7
CR8
CR9
R40 1K 1%
C12 2.7
C13 2.7
C14 2.7
OV(L)
-5V
(SS) SINGLE SHOT

A
B
C
CR10
CR11
CR12
R70 2200
R71 2200
R72 2200
R73 10K
R74 2200
Q11
CR1
OV(L)

13. ALL GATES ARE 700-8468, INVERTERS ARE 700-8360 AND POWER GATES ARE 700-8440
(12) JUMPER NOT USED IN ALL ASSEMBLIES. SEE VERSION TABLE
(11) SEE DETAIL SCHEMATIC ZONE 16-A
(10) SEE DETAIL SCHEMATIC ZONE 12-A
(9) CONNECTED TO ALL POINTS MARKED 'X' 14 PLACES
8. ON ALL IC'S PIN 14 IS +5V, PIN 7 IS OV(L)
7. ALL J/K FLIPFLOPS ARE 700-8520
6. ALL DIODES ARE 300-4446
5. ALL PNP TRANSISTORS ARE 200-4125; NPN 200-4123
4. ALL CAPACITORS IN MICROFARADS, 20V, 20%
3. ALL RESISTORS IN OHMS, 5%, 1/2 WATT
(2) [H] INDICATES HEATSINK
1. FOR ASSEMBLY DRAWING SEE 100224

NOTES UNLESS OTHERWISE SPECIFIED

14 13 12 11 10 9 8 7 6 5

+5V R88 4700 TP6 U11-C U11-D CR22 'X' GRS

U5-C U5-D CR17 'X' GRS TP13 R57 270 R65 270 B18 A

U6-B U6-A R58 270 CR18 'X' GRS TP12

U6-C U6-D R86 270 CR19 'X' GRS TP11

+5V R60 10K U7-A U7-B R61 15K OV(L) C20 .01 100V 10% U9-A R59 150 C19 .015 100V 10% OV(L) U9-B

TP4 C21 .01 100V 10% R62 15K OV(L) +5V R63 10K +5V R64 10K R66 270 R67 270 R68 15K OV(L) C22 .01 100V 10% R69 270 U8-A U9-C

U7-C U7-D CR20 'X' GRS TP10 MPD 10 U8-C U9-D

U8-D U9-F

U11-B U11-A CR21 'X' GRS TP7 SS 11

U10-A U10-C U10-B

EPW (20) U12-A U13-A +5V R83 1K TP8

TP5

U18-A CR23 'X' GRS OV(L) TP9

U18-B OV(L)

U19-D

(11) CUR

U16-B CR24 'X' GRS

U16-A U19-C U20-F

U20-D U20-E

U17-B

U20-C U20-B

U10-D U20-A U15-A

U17-A CR25 'X' GRS

U14-D (X) RGR

U14-C (21) FGR

U14-A (22) EFM

U14-B (Y) FGL

U12-D U12-C U12-F (19) GIP U12-E

+5V R84 1K

DMC (U) U13-B R87 100 (18) RTNI C27 2.7 OV(L)

SFL2 (V) U8-B U10-F

U3-C U10-E (T) TRR

EWPC (C) R47 820 JUMPER (12)

+5V R46 1200 Q9 C16 .022 100V 10% TP3 (7) (8) (K) WPC

R48 180 1W Q10 2C10-3053 (2) (H) R49 470 -5V

Q8 C

A B C CR10 CR11 CR12 R70 2200 R71 2200 R72 2200 Q11 R75 2200 CR13 Q12 R73 10K R74 2200 C23 .01 100V 10% R76 220 CR14 R77 2200 R78 100K OV(L) -5V CR15 R79 220K C25 47PF 500V 5% R80 18K R81 220K R82 4700 Q13 Q14 C24 .047 100V 10% OV(L) D

+5V

(MPD) MISSING PULSE DETECTOR

14 13 12 11 10 9 8 7 6 5

DATE	SYM	REVISION RECORD	AUT	DR	CH
6 JAN 84	A	RELEASED		JS	
MAR	B	REVISED EPN NEW		JE	
9 Jan	C	ECN 122		JE	
8 MAY	D	ECN 309		JT	
15 JUN	E	ECN 309		JT	

VERSION TABLE

ASSEMBLY	MODEL	JUMPER	C12
100224-01	WRITE ONLY	USED	NOT USED
100224-02	READ/WRITE	NOT USED	NOT USED
100224-03	WRITE ONLY	USED	USED
100224-04	READ/WRITE	NOT USED	USED

REFERENCE DESIGNATORS

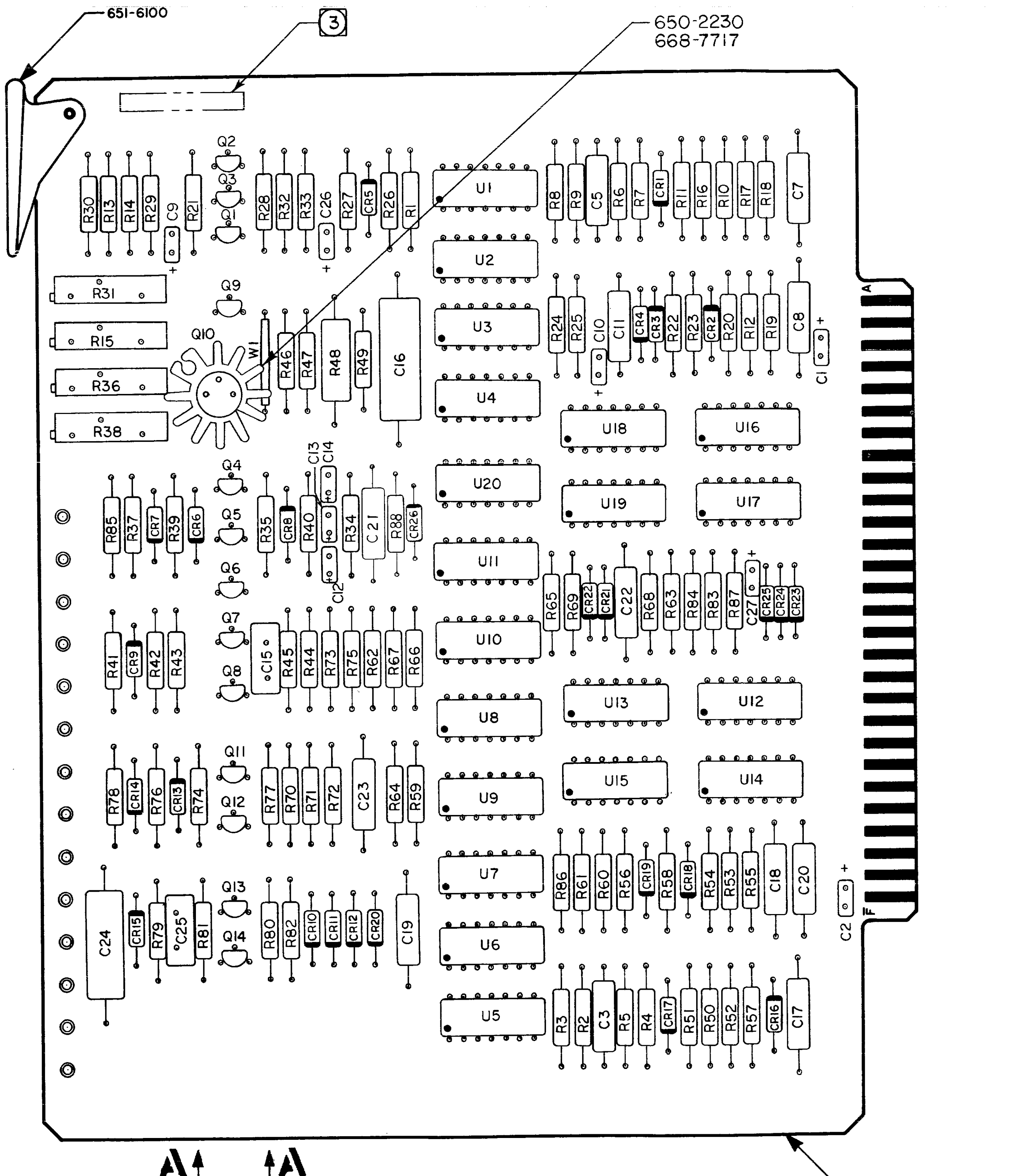
LAST USED	DELETED
R88	
CR26	
C27	C4, C6,
Q14	
U20	
TP14	

PERIPHERAL EQUIPMENT CORPORATION

SCHEMATIC FUNTION CONTROL

100223 ISSUE E

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
5 MAY	A	ERN 1-BX	EMD		
25 JUNE	B	ECN 122	SM	JE	
8 AUG '68	C	ECN 169	EMD	UK	JT
10-22	D	ECN 309	RL	JT	UK

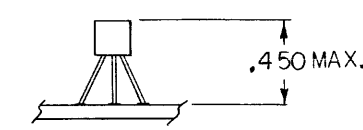


④ TABLE I

PART NO.	REF. DESIGNATION
200-4123	Q1,2,3,7,8,13,14
200-4125	Q4,5,6,9,11,12
200-3053	Q10
300-4446	CR1-26
700-8360	U3,9,10,12,20,
700-8440	U13
700-8460	U1,2,4,5,6,7,8,11,14,15,19,
101-1015	R87
101-1515	R14,32,59
101-1815	R2,4,7,8,23,25
101-2215	R1,39,76,85
101-2715	R11,16,19,20,51,54,57,58,
	65,66,67,69,86
101-4715	R49
101-8215	R21,33,47
101-1025	R83,84
101-1225	R26,46
101-2225	R27,34,35,70,71,72,74,
	77,75
101-4725	R3,5,6,9,22,24,28,44,82
	R56, 88
101-1035	R10,18,29,50, 60,64,
	63,73
101-1535	R12,17,52, 61,62,68
101-1835	R43,80
101-1045	R42,45,78
101-2245	R81,79
101-3355	R41
102-1815	R48
104-5111	R37
104-1213	R40
121-5020	R15,31,38
121-1030	R36
130-4705	C25
130-1015	C15
131-1030	C3,5,7,8,11,17,18,20,21,
	22,23
131-1530	C19
131-4730	C24
131-2240	C16
132-2752	C1,2,9,10,13,14,26,27
700-8520	U16,17,18
101-1215	R13,30
101-6825	R53
101-5635	R55

⑤ TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL: WRITE	READ WRITE	WRITE	READ WRITE					
VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09
W1	100373-01		100373-01						
C12			132-2752	132-2752					



VIEW A-A

⑤ FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.

④ FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

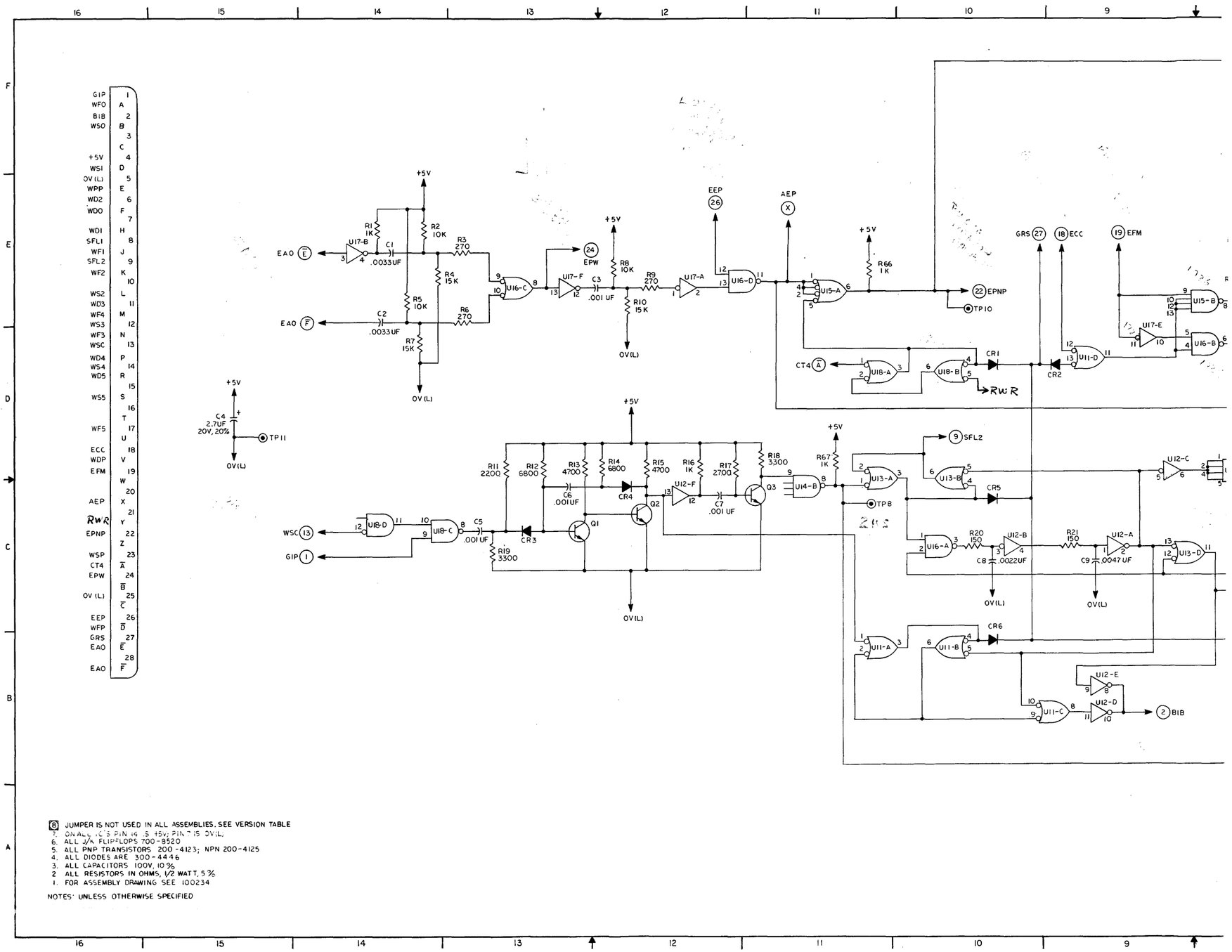
③ RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100223
   SPEC-100227

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE 2/1	DRAWN BY / APPROVED BY EMD
FRACTIONAL ±	TITLE PCBA FUNCTION CONTROL		SHEET 1 OF 1
ANGULAR ±	DATE 5-7-68	DRAWING NUMBER 100224	ISSUE D



8. JUMPER IS NOT USED IN ALL ASSEMBLIES. SEE VERSION TABLE
7. ON ALL IC'S PIN 14 IS +5V; PIN 7 IS 0V(L)
6. ALL J/K FLIP-FLOPS 700-8520
5. ALL PNP TRANSISTORS 200-4123; NPN 200-4125
4. ALL DIODES ARE 300-4446
3. ALL CAPACITORS 100V, 10%
2. ALL RESISTORS IN OHMS, 1/2 WATT, 5%
1. FOR ASSEMBLY DRAWING SEE 100234

NOTES: UNLESS OTHERWISE SPECIFIED

DATE	SYM	REVISION RECORD	AUTH	DR	CH
2/1/80	A	ERN 1-AL	EKP	JE	
3-9-88	B	ECN 017		JE	

VERSION TABLE

MODEL	ASSEMBLY	JUMPER
WRITE ONLY	100234-01	USED
READ & WRITE	100234-02	NOT USED

REFERENCE DESIGNATORS

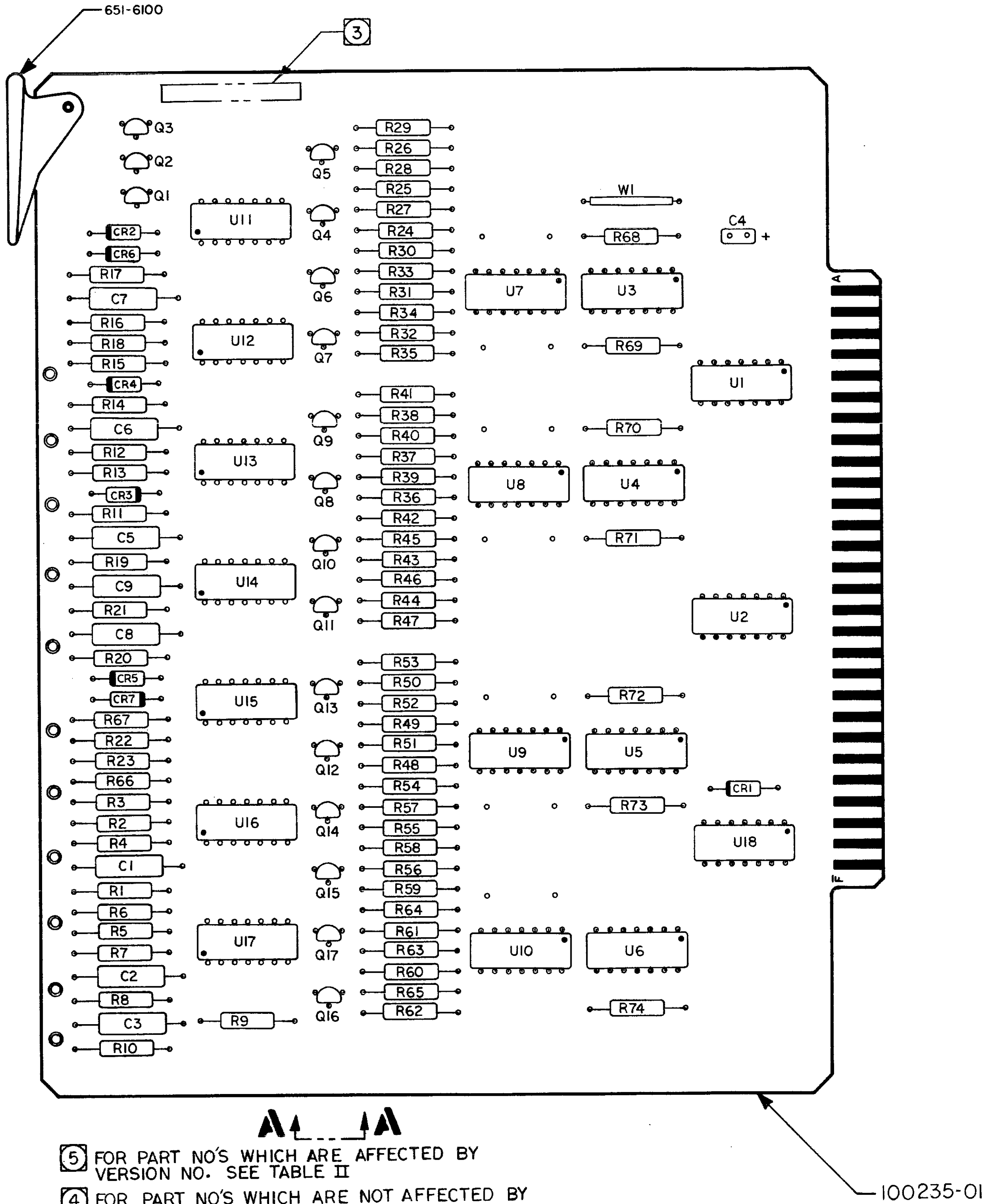
LAST USED	DELETED
R74	
C9	
CR7	
Q17	
U18	
TP11	

PERIPHERAL EQUIPMENT CORPORATION

SCHEMATIC - DOUBLE BUFFER WRITE AMPLIFIER

100233 ISSUE B

DATE	SYM.	REVISION RECORD	AUTH.	DR.	CK.
[illegible]	A	ERN 1-CR	EMD		
[illegible]	B	ECN 264	[illegible]	[illegible]	[illegible]

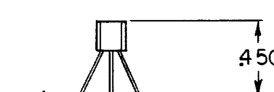


4 TABLE I

PART NO.	REF DESIGNATION
200-4123	Q1,2,3
200-4125	Q4,5,6,7,8,9,10,11,12,13,14,
	15,16,17
700-8360	U1,2,12,17
700-8440	U14,15
700-8460	U7,8,9,10,11,13,16,18
700-8520	U3,4,5,6
300-4446	CR1,2,3,4,5,6,7
101-1515	R20,21
101-2215	R26,29,32,35,38,41,44,
	47,50,53,56,59,62,65
101-2715	R3,6,9
101-1025	R1,16,22,23,66,67
101-1225	R24,27,30,33,36,39,42,
	45,48,51,54,57,60,63
101-2225	R11,25,28,31,34,37,40,43,
	46,49,52,55,58,61,64
101-2725	R17
101-3325	R18,19
101-4725	R13,15
101-6825	R12,14
101-1035	R2,8, 5
101-1535	R4, ,7,10
101-1825	R68,69,70,71,72,73,74
131-1020	C3,5,6,7
131-2220	C8
131-3320	C1,2
131-4720	C9
131-2752	C4
100373-01	W1

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09



VIEW A-A

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I

3 RUBBER STAMP PART NO., INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC, 100233
   SPEC, 100237

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE FULL	DRAWN BY [illegible] / APPROVED BY EMD
FRACTIONAL ±	TITLE PCBA DOUBLE BUFFER W AMP		SHEET 1 OF 1
ANGULAR ±	DATE	DRAWING NUMBER 100234	ISSUE B

GIP 1
WF0 A
BIB 2
WS0 B
DSS1 3
DSS0 C
+5V 4
WSI D
OV(L) 5
E
WD2 6
WD0 F
DSS2 7
WD1 H
SFL1 8
WF1 J
SFL2 9
WF2 K
DSS3 10
WS2 L
WD3 11
WF4 M
WS3 12
WF3 N
WSC 13
WD4 P
WS4 14
WD5 R
DSS4 15
WS5 S
DSS5 16
WS6 T
WF5 17
WD6 U
ECC 18
WDP V
EFM 19
WD7 W
WF6 20
AEP X
DSS7 21
DSSP Y
EPNP 22
WF7 Z
WSP 23
ECRC A
EPW 24
WS7 B
OV(L) 25
DSS6 C
EEP 26
WFP D
GRS 27
EAO E
WCRC 28
EAO F

+5V
R1 1K
R2 10K
R4 270
U25-B
C1 .0033
R3 15K
EA0 (E)
OV(L)
24 EPW
EEP 26
AEP X
+5V
R8 1K
U23-A
22 EPNP
TP12
+5V
R24 10K
R26 270
C3 .0033
R25 15K
EA0 (F)
U24-C
U25-F
C2 .001
+5V
R5 10K
R6 15K
OV(L)
R7 270
U25-A
U24-D
GRS 27
ECC 18
EFM 19
C10 .0022
OV(L)
U25-
CR6
U22-B
+5V
C9 2.7 20V, 20%
TP13
OV(L)
R9 1K
R11 3300
R12 6800
R13 4700
R14 6800
R15 4700
R16 1K
R17 2700
R18 3300
C5 .001
CR2
U19-F
C6 .001
Q3
Q2
Q1
CR1
R10 2200
C4 .001
U18-D
U22-A
WSC 13
GIP 1
OV(L)
+5V
WCRC 28
U25-C
U25-D
U21-B
R19 1K
TP10
9 SFL2
U20-A
U20-B
CR3
R20 150
U19-B
R21 150
U19-A
U24-A
C7 .0022
C8 .0047
OV(L)
OV(L)
U19-
U20-
CR5
U18-A
U18-B
U19-D
U18-C
U22-C
U19-E
ECRC (A)

(11) SEE VERSION TABLE FOR RESISTOR VALUES.

(10) THIS PORTION OF CIRCUIT IS NOT USED IN ALL ASSEMBLIES SEE VERSION TABLE.

(9) SEE VERSION TABLE FOR RESISTOR VALUES.

8. ON ALL IC'S PIN 14 IS +5V, PIN 7 IS OV(L)
7. ALL DUAL FLIPFLOPS ARE 700-8520, SINGLE FLIPFLOPS ARE 700-8450, AND GATES 700-8460, INVERTERS 700-8360, POWER GATES 700-8440
6. ALL PNP TRANSISTORS ARE 200-4125; NPN 200-4123
5. ALL DIODES ARE 300-4446
4. ALL CAPACITORS IN MICOFARADS, 100V, 10%
3. ALL RESISTOR IN OHMS, 5 %, 1/2 WATT

(2) JUMPER IS NOT USED IN ALL ASSEMBLIES. SEE VERSION TABLE

1. FOR ASSEMBLY DRAWING SEE 100234

NOTES: UNLESS OTHERWISE SPECIFIED

DATE	SYM	REVISION RECORD	AUTH	DR	CH
7/17/68	A	ERN 1-DJ	EMD	JE	
9/9/68	B	ECN 145	EMD	JT	
8/13/69	C	ECN 184	[illegible]	[illegible]	
11/13/69	D	ECN 297	[illegible]	JK	

VERSION TABLE

ASSEMBLY	JUMPER POSITION (2)			(10)	(11)	(9)
	W1	W2				
100239-01	USED	OMIT		USED	390	2200
100239-02	OMIT	USED		OMIT	270	1800

REFERENCE DESIGNATORS

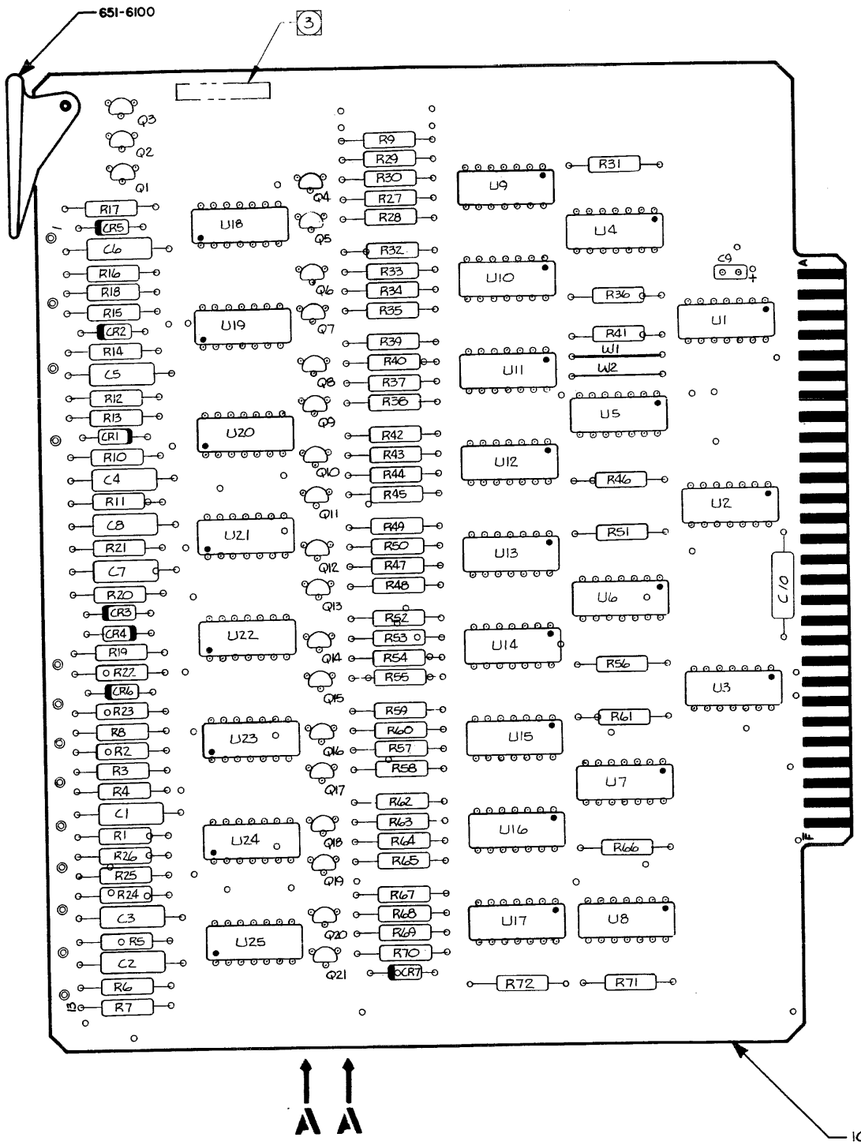
LAST USED	DELETED
R72	
C10	
Q21	
CR7	
U25	
TP13	
W2	

PERIPHERAL EQUIPMENT CORPORATION

SCHEMATIC - DOUBLE BUFFER - 9 CHANNEL WRITE AMPLIFIER

100238 ISSUE D.

DATE	SYM	REVISION RECORD	APPVD	DR	CK
7-31	A	ERN 1-EC	EMD	MK	MK
8-8	B	ECN 170	EMD	MK	MK
9-4-68	C	ECN 237	EMD	MK	MK

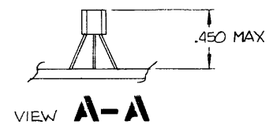


4 TABLE I

PART NO.	REF. DESIGNATION
101-1515	R20, 21
101-2715	R4, 7, 26
101-1025	R1, 8, 9, 16, 19, 22, 23
101-1225	R27, 28, 32, 33, 37, 38, 42, 43, 47, 48, 52, 53, 68, 67
101-2225	R10
101-2725	R17
101-3325	R11, R18, R72
101-4725	R13, R16
101-6825	R12, 14
101-1035	R2, 5, 24
101-1535	R3, 6, 25
131-1020	C2, 4, 5, 6
131-2220	C7, 10
131-3320	C1, 3
131-4720	C8
132-2752	C9
200-4123	Q1, 2, 3
200-4125	Q4-Q15, 20, 21
200-4446	CR1-CR7
700-8360	U1, 2, 3, 19, 25
700-8440	U21, 23
700-8450	U9-U14, 17
700-8460	U18, 20, 22, 24
700-8620	U4-U6, 8

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL 9TK / 7TRACK								
	VER. -01	-02	-03	-04	-05	-06	-07	-08	-09
R29,30,34,35,39,40,44,45,	101-3915	101-2715							
49,50,54,55,69,70		101-2715							
R59,60,64,65	101-3915								
R31,36,41,46,51,56,71	101-2225	101-1825							
R61,66	101-2225								
R57,58,62,63	101-1225								
W1	100373-01								
W2		100373-01							
Q16-19	200-4125								
U15,16	700-8450								
U7	700-8620								



3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100238.
SPEC-100242.

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION	
DECIMAL ±	SCALE 2/1	DRAWN BY G. FICKEN
		APPROVED BY ERD
FRACTIONAL ±	TITLE PCBA-DOUBLE BUFFER 9 CHANNEL WRITE AMP.	SHEET 1 OF 1
ANGULAR ±	DATE 7/10/68	DRAWING NUMBER 100239
		ISSUE C

DATE	SYM	REVISION RECORD	AUTH	DR	CH
8/13	A	ERN 1-AK	SAM	JT	SAM
AUG 17	B	ECN 044	SAM	JT	JT
7-29	C	ECN 156	SAM	JT	JT
9-10	D	ECN 224	JT	JT	JT

OUTPUT 200 I
PARITY OUTPUT A
OUTPUT 300 2
OUTPUT 100 B
OUTPUT 500 3
OUTPUT 400 C
+5V 4
INPUT 400 D
0V (L) 5
INPUT 200 E
OUTPUT 600 6
INPUT 300 F
INPUT 600 7
INPUT 500 H
INPUT 100 8
J
OUTPUT 800 9
K
OUTPUT 700 10
L
OUTPUT 900 11
INPUT 700 M
INPUT 900 12
ENTER INPUT 1 N
INPUT 800 13
RTER OUTPUT 1 P
OUTPUT 1300 14
ERTER OUTPUT 2 R
OUTPUT 1000 15
ERTER INPUT 2 S
OUTPUT 1400 16
RTER OUTPUT 3 T
OUTPUT 1700 17
ERTER INPUT 3 U
INPUT 1300 18
RTER OUTPUT 4 V
INPUT 1400 19
ERTER INPUT 4 W
OUTPUT 1600 20
RTER OUTPUT 5 X
OUTPUT 1500 21
ERTER INPUT 5 Y
22
INPUT 1000 Z
INPUT 1600 23
INPUT 1500 $\overline{A}$ 24
INPUT 1200 $\overline{B}$
$\overline{C}$ 25
0V (L)
INPUT 1100
-5V 26
INPUT 1700 $\overline{D}$
INPUT 1800 27
ISABLE BCD 10 $\overline{E}$
OUTPUT 1800 28
OUTPUT 1100 $\overline{F}$

+5V
C1 2.7 UF 20V, 20%
TP20
2.7 UF 20V, 20% C2
8
0V(L)
-5V

U11-D 9 8 P
U11-E 11 10 R
U11-F 13 12 T
U11-C 3 4 V
U11-B 5 6 X

U1-B 3 4
U1-A 1 2
U1-C 5 6
U6-D 13 12 11
U7-A 1 2 3
U7-B 4 5 6
U10-A 1 2
U1-D 9 8
U1-F 13 12
U1-E 11 10
U2-A 1 2
U6-A 1 2 3
U6-B 4 5 6
U6-C 9 10 8
U10-B 3 4
U9-D 12 13 11
U7-C 9 10 8
U7-D 12 13 11
U10-E 11 10
U2-B 3 4
U2-D 9 8
U2-C 5 6
U2-E 11 10
U5-A 1 2 3
U5-B 4 5 6
U5-C 9 10 8
U10-C 5 6
W'A'
U9-A 1 2 3
U9-B 4 5 6
U9-C 10 9 8
U10-D 9 8
2
W'B'
U2-F 13 12
U3-E 11 10
U4-A 1 2 3
U4-B 4 5 6
U4-C 9 10 8
U4-D 12 11
U8-A 1 2 3
U8-B 4 5 6
U8-C 9 10 8
U8-D 12 11
U3-F 13 12
DISABLE
E
BCD 10
6
U3-C 5 6
U3-A 1 2
U3-D 9 8
U3-B 3 4

CIRCUIT 1600 23
CIRCUIT 1200 24
CIRCUIT 1500 A
CIRCUIT 1100 C
CIRCUIT 1700 D
CIRCUIT 1800 27
CIRCUIT 1400 19
CIRCUIT 1300 18
CIRCUIT 100 B
CIRCUIT 200 E
CIRCUIT 300 F
CIRCUIT 400 D
CIRCUIT 500 H
CIRCUIT 600 7
CIRCUIT 700 M
CIRCUIT 800 13
CIRCUIT 900 12
CIRCUIT 1000 Z

TP16 20
TP12 17
TP15 21
TP11 F
TP17 B
TP18 28
TP14 16
TP13 14
TP1 B
1
TP2
2
TP3
C
TP4
3
TP5
6
TP6
10
TP7
9
TP8
11
TP9
15
TP10

+5V
R4 3300
OUTPUT
INPUT
R1 7 R2
CR1 300-4446
Q1 200-4123
C3 .001 UF 100V, 10%
R3 18K
W1
0V(L)
CONFIGURATION A
POSITIVE LOGIC

+5V
R4 3300
OUTPUT
Q1 200-4123
INPUT
R1 7 R2
W2
Q2 200-4125
C3 .001 UF 100V, 10%
R3 18K
R5 330
0V (L)
-5V
CONFIGURATION B
NEGATIVE LOGIC

X O E
5 S1
TP19
A
PARITY OUTPUT

VERSION TABLE

MODEL	ASSEMBLY	CIRCUITS CONSISTING OF CONFIG A	CIRCUITS CONSISTING OF CONFIG B	JUMPER	2	6	R1 & R2
WRITE ONLY 7 TRACK	100249-01	100 THRU 1200, 1500 THRU 1800	NONE	A	NOT USED	USED	2200
READ ONLY 7 & 9 TRACK	100249-02	200 THRU 1000	NONE	NOT USED	NOT USED	NOT USED	2200
WRITE ONLY 9 TRACK	100249-03	ALL 100 THRU 1800	NONE	B	USED	USED	2200
WRITE ONLY 7 TRACK	100249-04	NONE	100 THRU 1200, 1500 THRU 1800	A	NOT USED	USED	2200
WRITE ONLY 9 TRACK	100249-05	ALL 100 THRU 1800	NONE	B	USED	USED	680
WRITE ONLY 9 TRACK	100249-06	NONE	ALL 100 THRU 1800	B	USED	USED	2200
READ ONLY 7 TRACK	100249-07	NONE	200 THRU 1000	NOT USED	NOT USED	NOT USED	2200

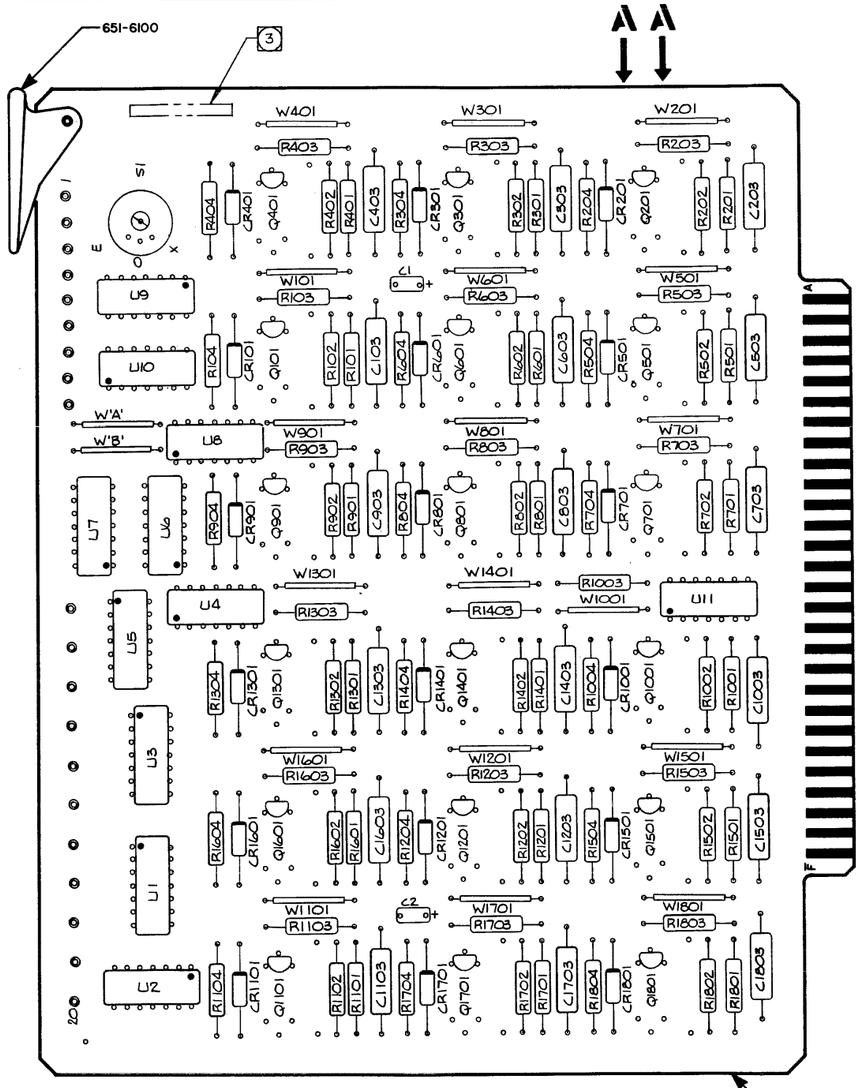
REFERENCE DESIGNATORS

LAST USED	DELETED
R5	
C3	
CR1	
Q2	
U11	
TP20	
S1	

6 & 07
BLE FOR VALUE
F CIRCUIT (ENCLOSED IN BROKEN LINE —·—·—)
OME ASSEMBLIES. SEE VERSION
)
H X=EXTERNAL, E=EVEN, O=ODD
) 14 IS +5V. PIN 7 IS 0V(L)
OHMS, 1/2 WATT, 5%
F CIRCUIT IS OMITTED IN SOME ASSEMBLIES.
JUMPER 'A' IS USED WHEN INCLUDED
SED. SEE VERSION TABLE ZONE 4C
GNATIONS ARE INCOMPLETE FOR COMPLETE
D CIRCUIT NO. TO COMPONENT NO. SUCH AS;
00 IS C103; R5 IN CIRCUIT 1800 IS R1805
HERWISE SPECIFIED

PERIPHERAL EQUIPMENT CORPORATION
TITLE RECEIVER, SLOW INTERFACE
DRAWING NUMBER 100248
ISSUE D
DATE 8-6-68

DATE	SYM	REVISION RECORD	AUTH.	QA	CK.
7-29	A	ERN 1-EC	[illegible]	[illegible]	[illegible]
8-26	B	ECN 203	[illegible]	[illegible]	[illegible]



INFORMATION ON SH.1 APPLIES ONLY TO VERSIONS-01, -02, -03, -05.

4 TABLE I

PART NO.	REF DESIGNATION
100373-01	W201-1001
101-3325	R204-1004
101-1835	R203-1003
131-1020	C203-1003
132-2752	C1
200-4123	Q201-1001
300-4446	CR201-1001
700-8360	U11

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09
W'A'	100373-01			SEE		SEE			
W'B'			100373-01	SH 2	100373-01	SH 2			
W101, 1101, 1201, 1501-1801	100373-01		100373-01		100373-01				
W1301, 1401			100373-01		100373-01				
R101, 1101, 1201, 1501-1801, 102,	101-2225		101-2225		101-6815				
R1102, 1202, 1502-1802	101-2225		101-2225		101-6815				
R1301, 1401, 1302, 1402			101-2225		101-6815				
R104, 1104, 1204, 1504-1804	101-3325		101-3325		101-3325				
R1304, 1404			101-3325		101-3325				
R103, 1103, 1203, 1503-1803	101-1835		101-1835		101-1835				
R1303, 1403			101-1835		101-1835				
C103, 1103, 1203, 1503-1803	131-1020		131-1020		131-1020				
C1303, 1403			131-1020		131-1020				
C2									
Q101, 1101, 1201, 1501-1801	200-4123		200-4123		200-4123				
Q1301, 1401			200-4123		200-4123				
CR101, 1101, 1201, 1501-1801	300-4446		300-4446		300-4446				
CR1301, 1401			300-4446		300-4446				
U1, 2, 3, 10	700-8360		700-8360		700-8360				
U5, 6, 7, 9	700-8460		700-8460		700-8460				
U4, 8			700-8460		700-8460				
S1	514-8711		514-8711		514-8711				
R201-1001 202-1002	101-2225	101-2225	101-2225		101-6815				

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO., SEE TABLE II.

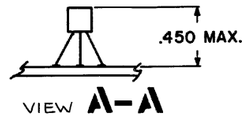
4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO., SEE TABLE I.

3 RUBBER STAMP PART NO., INCLUDING VERSION NO. AND ISSUE LETTER.

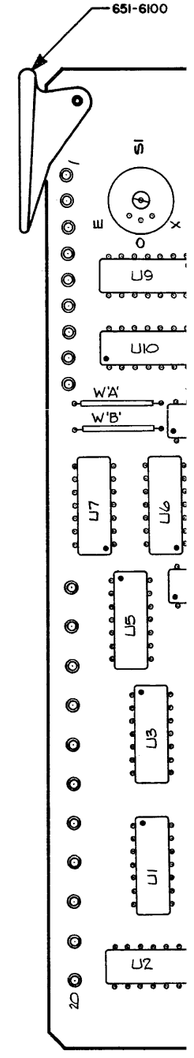
2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF. DWGS: SCHEMATIC - 100248.
SPEC - 100252.

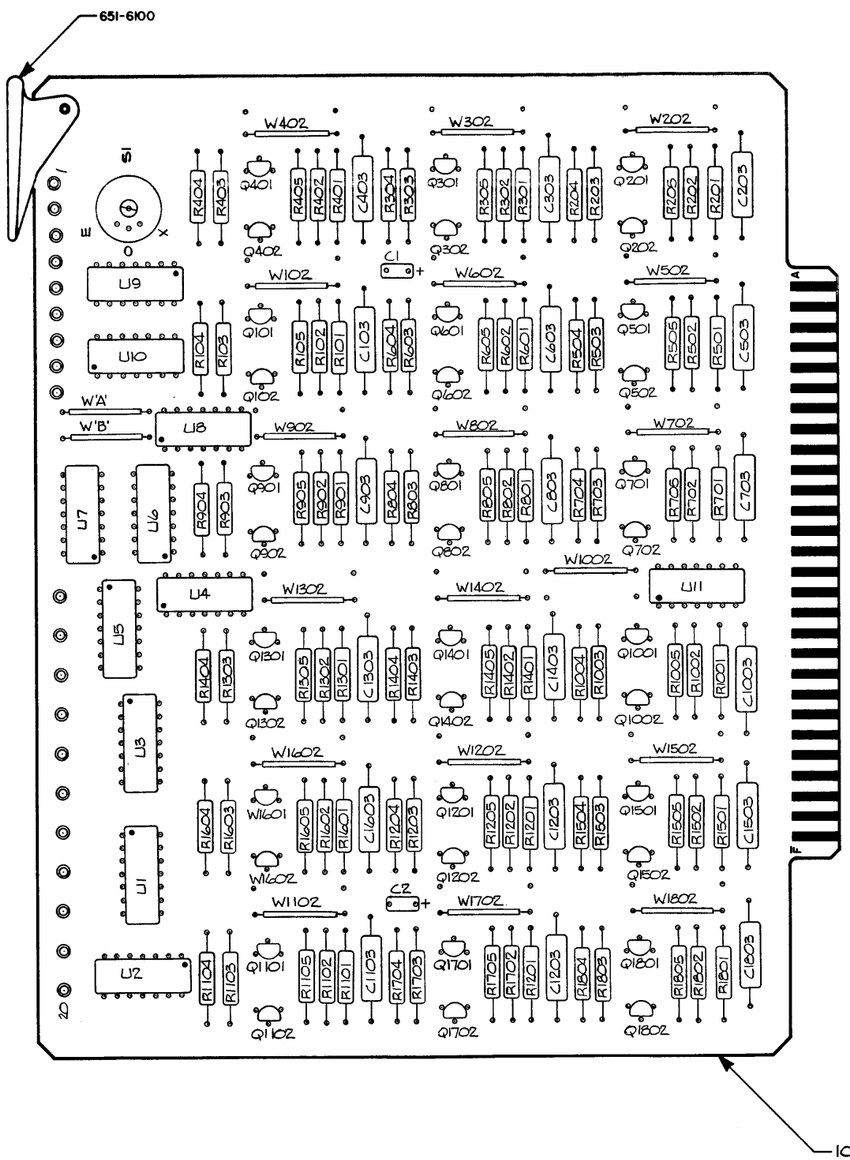
NOTES: UNLESS OTHERWISE SPECIFIED



TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION	
DECIMAL ±	SCALE 2/1	DRAWN BY FKK
FRACTIONAL ±	TITLE PCBA RECEIVER, SLOW INTERFACE	SHEET 1 OF 2
ANGULAR ±	DATE 6/17/68 / DRAWING NUMBER 100249	ISSUE B



DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
7-21	A	ERN 1-EC			
8-2	B	ECN 203			



INFORMATION ON SH 2 APPLIES ONLY TO VERSIONS -04, -06, -07

TABLE I

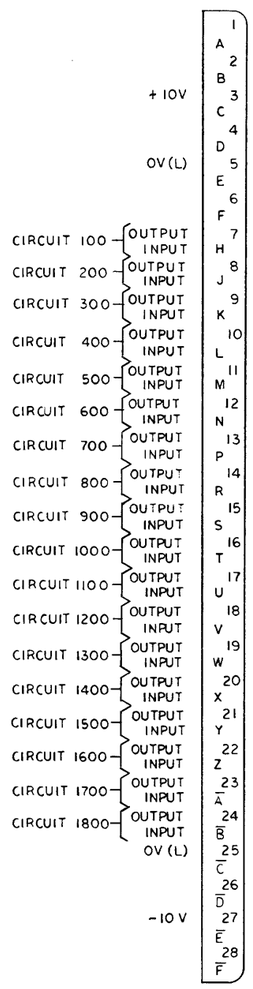
PART NO.	REF. DESIGNATION
132-2752	C1, C2
101-2225	R201-1001
101-2275	R202-1002
101-1835	R203-1003
101-3325	R204-1004
101-3315	R205-1005
200-4123	Q201-1001
200-4125	Q202-1002
131-1020	C203-1003
100373-01	W202-1002

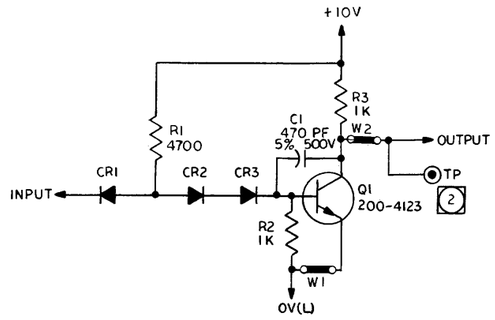
TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09
W'A'				100373-01			NO		
W'B'						100373-01	ADDITIONS		
U4,8						700-8460			
R1301,1401,1302,1402						101-2225			
R1303,1403						101-1835			
R1304,1404						101-3325			
R1305,1405						101-3315			
Q1301,1401						200-4123			
Q1302,1402						200-4125			
C1303,1403						131-1020			
W1302,1402						100373-01			
U1,2,3,10				700-8360		700-8360			
U5,6,7,9				700-8460		700-8460			
R101,1101,1201,1501-1801				101-2225		101-2225			
R102,1102,1202,1502-1802				101-2225		101-2225			
R103,1103,1203,1503-1803				101-1835		101-1836			
R104,1104,1204,1504-1804				101-3325		101-3325			
R105,1105,1205,1505-1805				101-3315		101-3315			
Q101,1101,1201,1501-1801				200-4123		200-4123			
Q102,1102,1202,1502-1802				200-4125		200-4125			
C103,1103,1203,1503-1803				131-1020		131-1020			
W102,1102,1202,1502-1802				100373-01		100373-01			
S1				541-8711		541-8711			

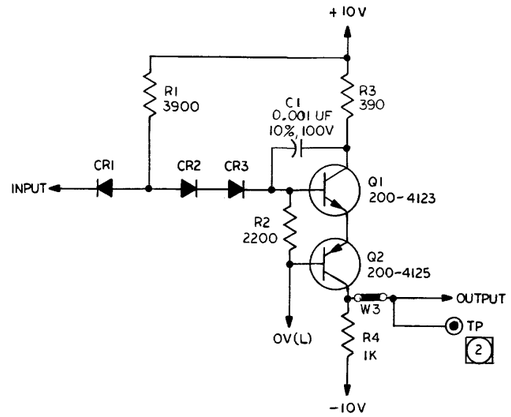
TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE 2/1	DRAWN BY G. FIKKEN
FRACTIONAL ±	TITLE PCBA RECEIVER SLOW INTERFACE		APPROVED SHEET 2 OF 2
ANGULAR ±	DATE 7/16/68	DRAWING NUMBER 100249	ISSUE B

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
2/8	A	ECN 1-24	[illegible]	JC	[illegible]
4/17	B	ECN 043	[illegible]	JG	[illegible]
9/25	C	ECN 120	[illegible]	[illegible]	[illegible]
12/18	D	ECN 140	[illegible]	TF	[illegible]





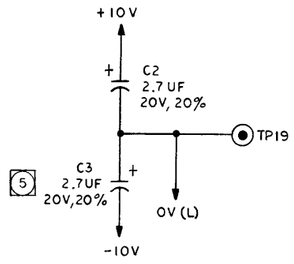
CONFIGURATION A
POSITIVE LOGIC (TYPICAL)



CONFIGURATION B
NEGATIVE LOGIC (TYPICAL)

VERSION TABLE

MODEL	ASSEMBLY	CIRCUITS CONSISTING OF	
		CONFIG A	CONFIG B
WRITE ONLY	100254-01	100 THRU 800	NONE
READ ONLY	100254-02	ALL	NONE
WRITE ONLY	100254-03	NONE	100 THRU 800
READ ONLY	100254-04	NONE	ALL



REFERENCE DESIGNATORS

LAST USED	DELETED
R4	
C3	
CR3	
Q2	
TP 19	

5 USED ON -03 & -04 ONLY

4. ALL DIODES ARE 300-4446

3. ALL RESISTORS IN OHMS, 5%, 1/2 WATT

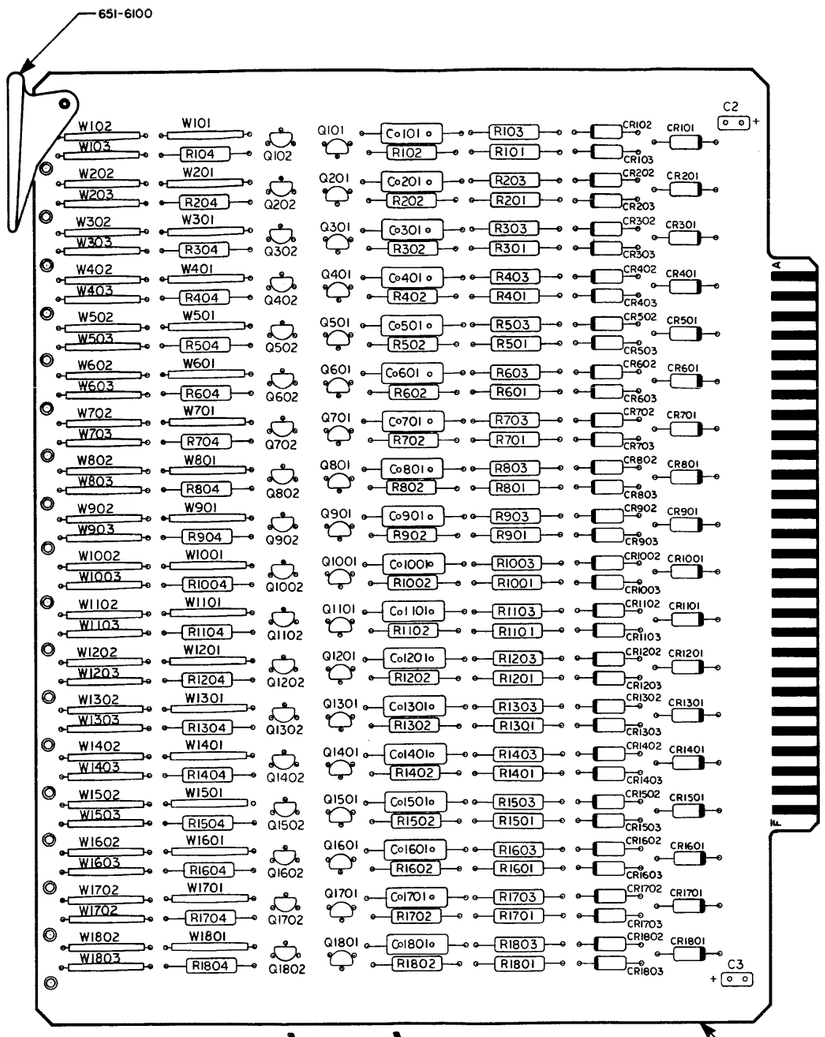
2 NUMBERS ASSIGNED TO TEST POINTS ARE THE PREFIX OF THE CIRCUIT NO. THEY ARE CONTAINED IN. SUCH AS: TEST POINT OF CIRCUIT 100 IS TP1; CIRCUIT 1800 IS TP18

1. REFERENCE DESIGNATORS ARE NOT COMPLETE. FOR COMPLETE DESIGNATION ADD CIRCUIT NO. TO COMPONENT NO. SUCH AS: CR3 OF CIRCUIT 100 IS CR103; R2 OF CIRCUIT 1800 IS R1802

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ± —		SCALE —	DRAWN BY J. ERINGER
FRACTIONAL ± —	TITLE SCHEMATIC - TRANSMITTER, SLOW INTERFACE		APPROVED [illegible]
ANGULAR ± —	DATE Feb 8 '68	DRAWING NUMBER 100253	ISSUE D

DATE	ITR	REVISION RECORD	AUTH	DR	CK
7/67	A				
4/68	C	ECN 120			
7/68	D	ECN 140			

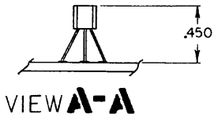


(4) TABLE I

PART NO.	REF DESIGNATION
200-4123	Q101-Q801
300-4446	CR101-CR801, CR102-CR802
	CR103-CR803
132-2752	C2

(5) TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / WRITE / VER.	-01	READ POS LOGIC -02	WRITE NEG LOGIC -03	READ NEG LOGIC -04	-05	-06	-07	-08	-09
Q901-Q1801		200-4123		200-4123					
Q102-Q802			200-4125	200-4125					
Q902-Q1802				200-4125					
CR901-CR1801		300-4446		300-4446					
CR902-CR1802		300-4446		300-4446					
CR903-CR1803		300-4446		300-4446					
R101-R801	101-4725	101-4725	101-3925	101-3925					
R901-R1801		101-4725		101-3925					
R102-R802	101-1025	101-1025	101-2225	101-2225					
R902-R1802		101-1025		101-2225					
R103-R803	101-1025	101-1025	101-3915	101-3915					
R903-R1803		101-1025		101-3915					
R104-R804			101-1025	101-1025					
R904-R1804				101-1025					
C101-C801	130-4715	130-4715	131-1020	131-1020					
C901-C1801		130-4715		131-1020					
W101-W801	100373-01	100373-01							
W901-W1801		100373-01							
W102-W802	100373-01	100373-01							
W902-W1802		100373-01							
W103-W803			100373-01	100373-01					
W903-W1803				100373-01					
C3			132-2752	132-2752					



(5) FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II

(4) FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I

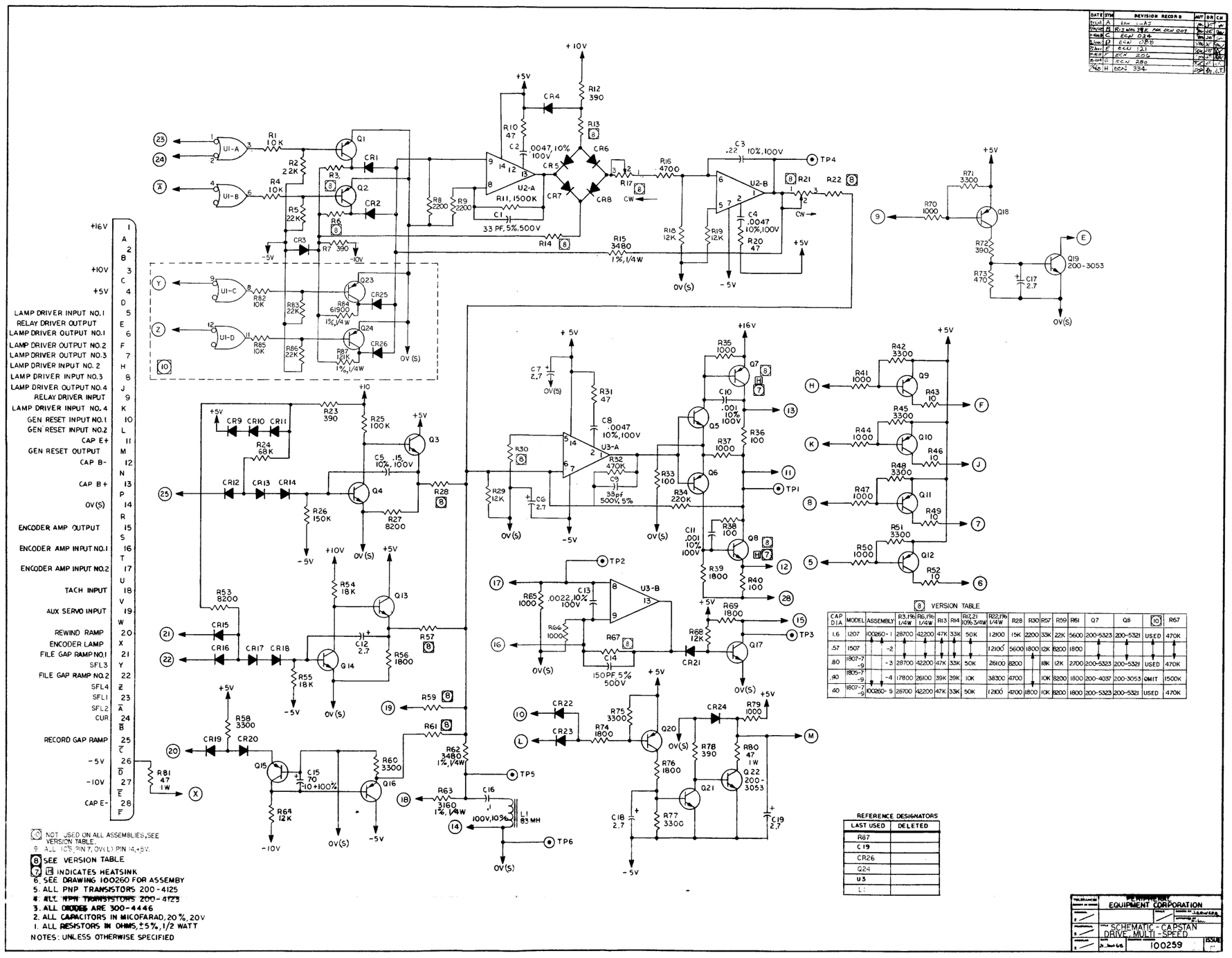
(3) RUBBUR STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLY PER STANDARD MANUFACTURING METHODS.

1. REF. DWGS: SCHEMATIC, 100253
SPEC, 100137

NOTES: UNLESS OTHERWISE SPECIFIED

FINAL ASSY		TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION
NEXT ASSY	USED ON	DECIMAL ±	SCALE 2:1 DRAWN BY APPROVED BY
		FRACTIONAL ±	TITLE PCBA TRANSMITTERS, SLOW INTERFACE
		ANGULAR ±	DATE 4-17-68 DRAWING NUMBER 100254
			SHEET 1 OF 1 ISSUE D



DATE	SYM	REVISION RECORD	ANT	DR	CH
11/67	A	ECN ...A2	PC	JC	PC
2/4/68	B	R13 WAS 39K PER ECN 009	PC	JC	PC
4 MAR	C	ECN 034	PC	JC	PC
5 JUN	D	ECN 078	PC	JC	PC
7/24/68	E	ECN 121	PC	JC	PC
9 AUG	F	ECN 206	PC	JC	PC
11 OCT	G	ECN 289	PC	JC	PC
2/6	H	ECN 334	PC	JC	PC

8 VERSION TABLE

CAP DIA	MODEL	ASSEMBLY	R3,1% 1/4W	R6,1% 1/4W	R13	R14	R12,2% 10% 3/4W	R22,1% 1/4W	R28	R30	R57	R59	R61	Q7	Q8	10	R67
1.6	1207	100260-1	28700	42200	47K	33K	50K	12100	15K	2200	33K	22K	5600	200-5323	200-5321	USED	470K
.57	1507	-2						12100	5600	1800	12K	8200	1800				
.80	1807-7 -9	-3	28700	42200	47K	33K	50K	26100	8200		18K	12K	2700	200-5323	200-5321	USED	470K
.40	1805-7 -9	-4	17800	26100	39K	39K	10K	38300	4700		10K	8200	1800	200-4037	200-3053	OMIT	1500K
.40	1807-7 -5	100260-5	28700	42200	47K	33K	50K	12100	4700	1800	10K	8200	1800	200-5323	200-5321	USED	470K

REFERENCE DESIGNATORS

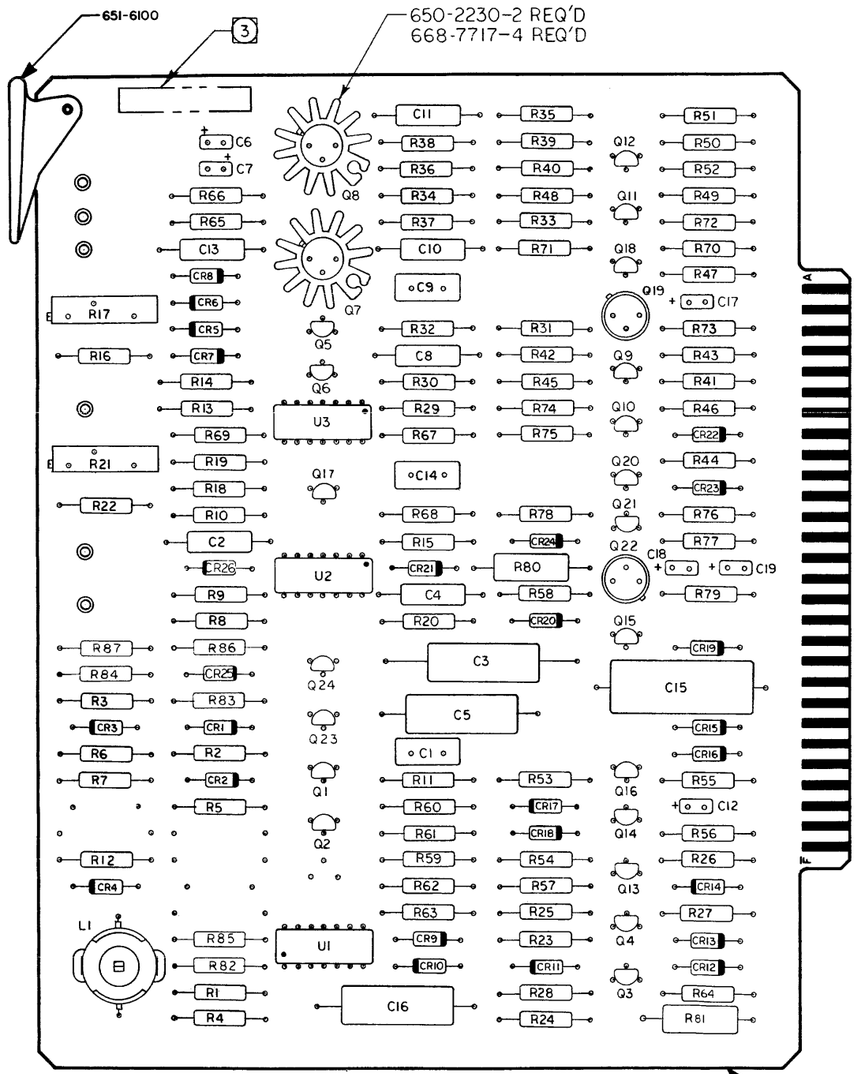
LAST USED	DELETED
R87	
C19	
CR26	
Q24	
U3	
L1	

PERIPHERAL EQUIPMENT CORPORATION

SCHEMATIC - CAPSTAN DRIVE, MULTI-SPEED

100259 ISSUE

DATE	SYM	REVISION RECORD	AUTH	DR	CK
8-3	C	ERN-1-EP	[illegible]	[illegible]	[illegible]
8-16	D	ECN 193	[illegible]	[illegible]	[illegible]
9-26	E	ECN 208	[illegible]	[illegible]	[illegible]
1-6	F	ECN 280	[illegible]	[illegible]	[illegible]
1-14	G	ECN 333	[illegible]	[illegible]	[illegible]



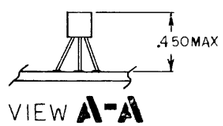
INFORMATION ON SH I APPLIES TO VERSIONS -01,-02,-03 & -05

4 TABLE I

PART NO.	REF. DESIGNATION
200-4123	Q3,4,5,13,14,17,21
200-4125	Q6,9,10,11,12,15,16,18,20,1,2,23,24
200-3053	Q19,22
300-4446	CR1-26
130-3305	C1,9,
131-1020	C10,11,
131-4720	C2,4,8
131-1040	C16
131-1540	C5
132-2752	C6,7,12,17,18,19
133-7060	C15
101-1005	R43,46,49,52
101-4705	R10,20,31
101-1015	R33,36,38,40
101-3915	R7,12,23,72,78
101-4715	R73
101-1025	R35,37,41,44,47,50,65,66,79
200-5321	Q8
101-1825	R39,56,69,70,74,76
101-2225	R8,9
101-3325	R42,45,48,51,58,60,71,75,77
200-5323	Q7
101-4725	R16
101-8225	R27,53
101-1035	R1,4,82,85
101-1235	R18,19,29,64,68
101-1835	R54,55
101-2235	R2,5,83,86
101-3335	R14
101-6835	R24
101-1045	R25
101-1545	R26
101-2245	R34
101-1555	R11
104-3161	R63
104-3481	R15,62
104-2872	R3
104-4222	R6
102-4705	R80,81
121-5030	R17,21
400-1435	U2,3
100212-01	L1
101-4735	R13
700-8460	U1
130-1515	C14
131-2220	C13
131-2240	C3
101-4745	R67,32
104-6192	R84
104-1213	R87

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	1207 -01	1507 -02	1807-7 -9 -03	-04	1807-7 -9 -05	-06	-07	-08	-09
R22	104-1212	104-1212	104-2612	SEE	104-1212				
R30	101-2225	101-1825	101-1825	SHEET 2	101-1825				
R28	101-1535	101-5625	101-8225		101-4725				
R57	101-3335	101-1235	101-1835		101-1035				
R59	101-2235	101-8225	101-1235		101-8225				
R61	101-5625	101-1825	101-2725		101-1825				



5 FOR PART NO'S WHICH ARE ARE AFFECTED BY VERSION NO'S SEE TABLE II.

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

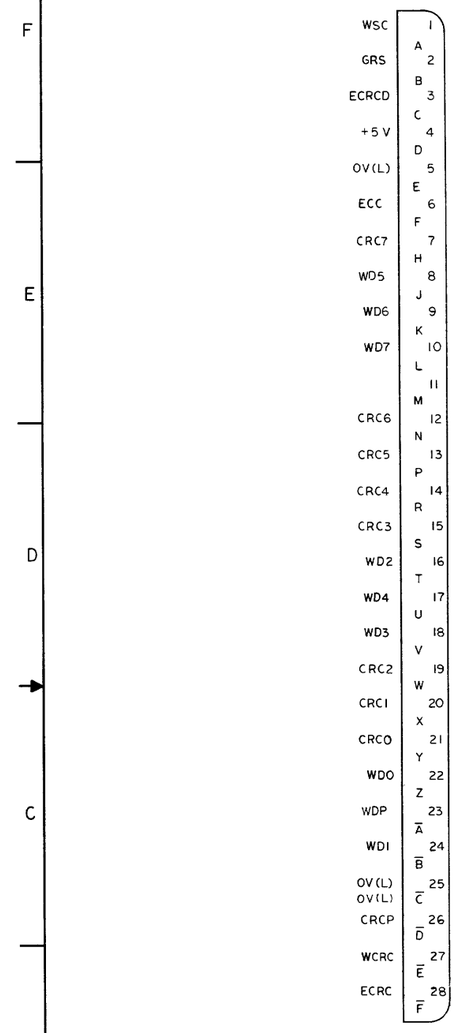
3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

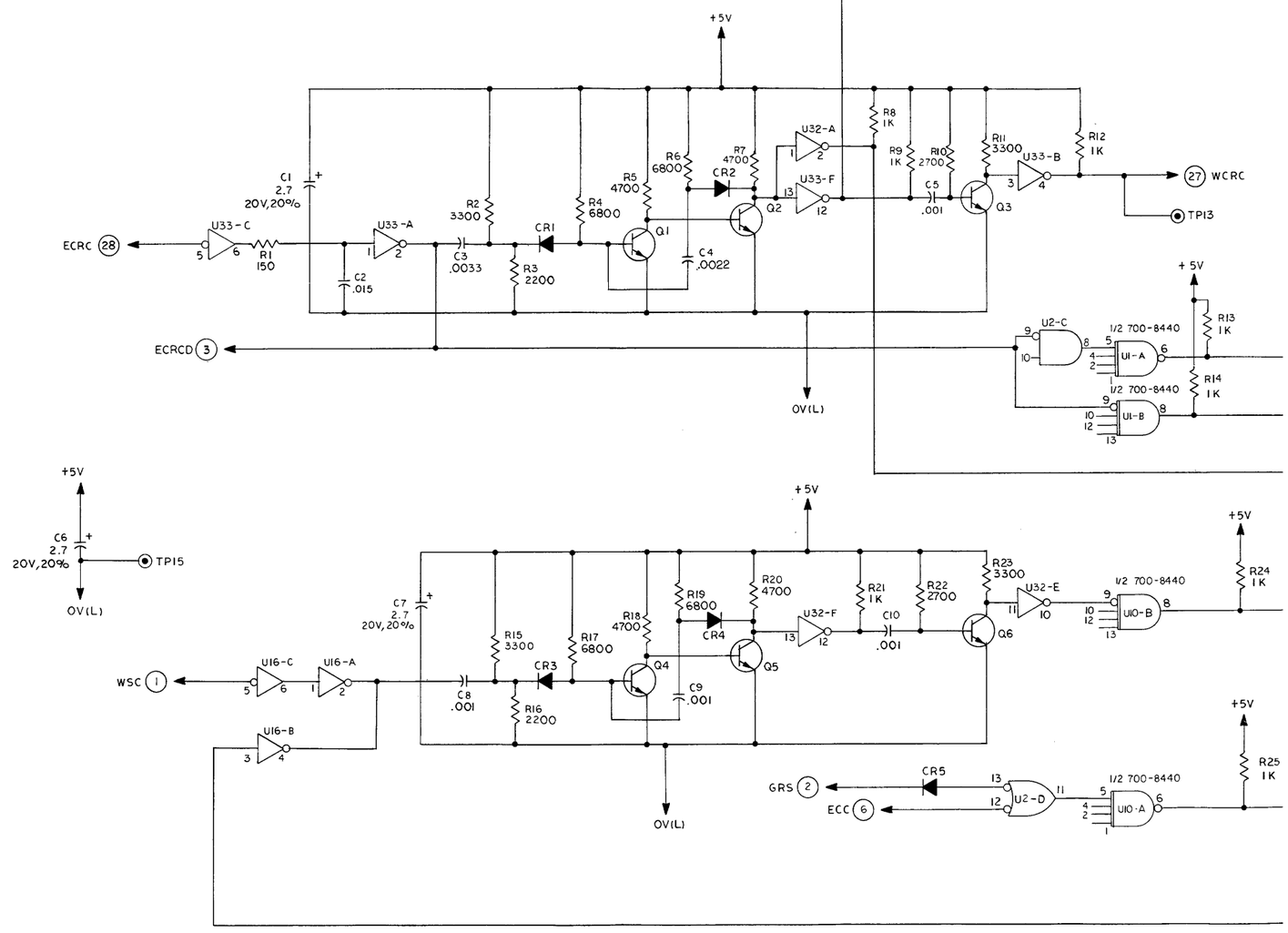
2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC, 100259
SPEC, 100263

NOTES: UNLESS OTHERWISE SPECIFIED

		TOLERANCES (EXCEPT AS NOTED) DECIMAL ± FRACTIONAL ± ANGULAR ±	PERIPHERAL EQUIPMENT CORPORATION	SCALE 2:1	DRAWN BY [illegible] APPROVED BY [illegible]
FINAL ASSY			TITLE PCBA CAPSTAN DRIVE, MULTI-SPEED		SHEET 1 OF 2
NEXT ASSY	USED ON		DATE 4-10-68	DRAWING NUMBER 100260	ISSUE G





9. ON ALL IC'S PIN 14 IS +5V, PIN 7 OV(L)
8. ALL INVERTERS 700-8360
7. ALL GATES 700-8460
6. ALL J/K FLIPFLOPS 700-8520
5. ALL PNP TRANSISTORS 200-412 , NPN 200-412
4. ALL DIODES ARE 300-4446
3. ALL CAPACITORS 100V, 10%
2. ALL RESISTORS IN OHMS, 1/2 WATT 5%
1. FOR ASSEMBLY DRAWING SEE 100265

NOTES: UNLESS OTHERWISE SPECIFIED

+5V
C2 .015
U33-A
C3 .0033
R2 3300
R3 2200
CR1
R4 6800
R5 4700
R6 6800
Q1
C4 .0022
R7 4700
CR2
Q2
U32-A
U33-F
R8 1K
R9 1K
R10 2700
C5 .001
R11 3300
U33-B
Q3
R12 1K
27 WCRC
TPI3
OV(L)
+5V
U2-C
1/2 700-8440
U1-A
U1-B
R13 1K
R14 1K
TPI
TP6
+5V
C7 2.7 20V, 20%
U16-A
C8 .001
R15 3300
R16 2200
CR3
R17 6800
R18 4700
Q4
Q5
C9 .001
R19 6800
CR4
R20 4700
U32-F
R21 1K
C10 .001
R22 2700
R23 3300
U32-E
Q6
1/2 700-8440
U10-B
R24 1K
TP2
OV(L)
+5V
GRS 2
ECC 6
CR5
U2-D
1/2 700-8440
U10-A
R25 1K
TP14
WDP 23
U8-B
U8-E
U20-A
WDO 22
U8-A
U8-F
U20-F
WDI 24
U8-C
U8-D
U19-A
WD2 16
U6-C
U6-D
U33-D
WD3 18
U6-A
U6-F
U33-E
WD4 17
U6-B
U6-E
U32-C
WD5 8
U3-C
U3-D
U32-D
WD6 9
U3-B
U3-E
U17-F
WD7 10
U3-F
U16-F
U29-C
U29-D
U28-C
U28-D
U27-C
U27-D
U31-A
U31-B
U19-F
U26-C
U26-D
U31-D
U31-C
U18-A
U25-C
U25-D
U30-A
U30-B
U18-F
U24-C
U24-D
U30-D
U30-C
U17-A
U23-C
U23-D
U22-C
U22-D
U21-C
U21-D

DATE	SYM	REVISION RECORD	AUTH	DR	CH
6 MAY	A	ERN 1-BW		JE	
19 MAY	B	ECN 085	EMD		

U29-C, U29-D, U20-B, U29-A, U29-B, U20-C, TP11, U15-A
U28-C, U28-D, U20-E, U28-A, U28-B, U20-D, TP12, U15-B
U27-C, U27-D, U19-B, U27-A, U27-B, U19-C, TP10, U14-A
U19-F, U26-C, U26-D, U19-E, U26-A, U26-B, U19-D, TP8, U14-B
U18-A, U25-C, U25-D, U18-B, U25-A, U25-B, U18-C, TP9, U13-A
U18-F, U24-C, U24-D, U18-E, U24-A, U24 B, U18-D, TP5, U13-B
U17-A, U23-C, U23-D, U17-B, U23-A, U23-B, U17 C, TP7, U12-A
U22-C, U22-D, U17-E, U22-A, U22-B, U17-D, TP3, U12-B
U21-C, U21-D, U16-E, U21-A, U21-B, U16-D, TP4, U11-A

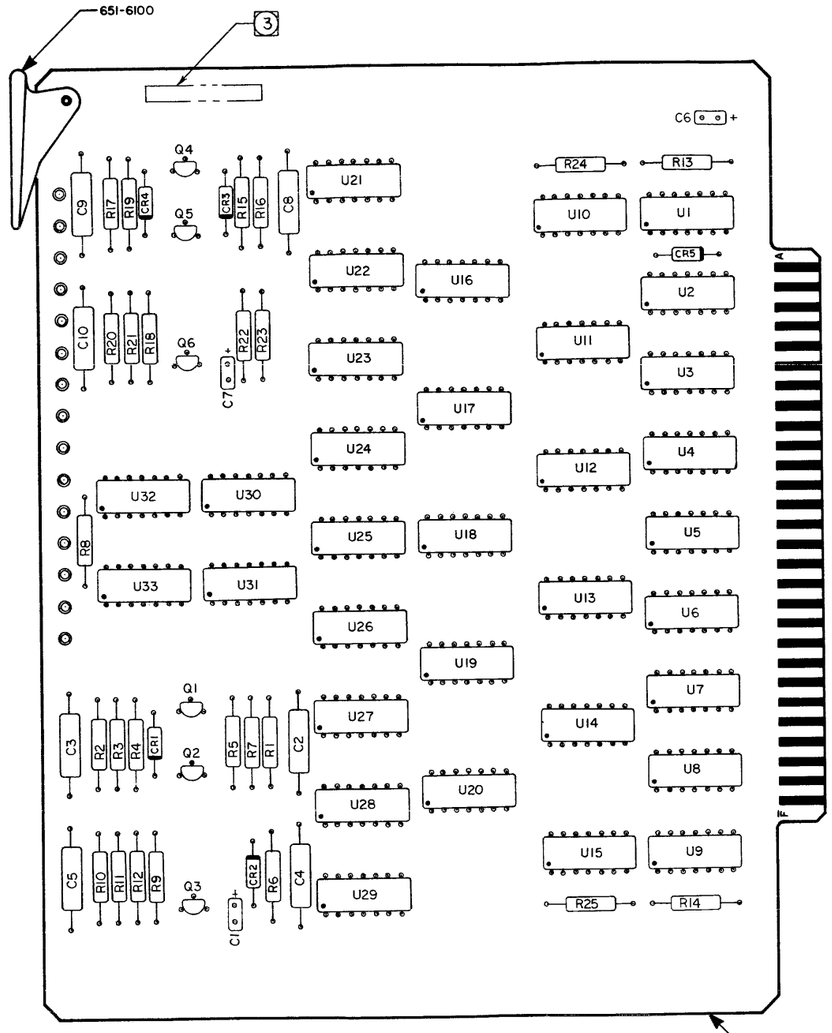
U9-A, U9-B → (26) CRCP
U9-D, U9-C → (21) CRC 0
U7-A, U7-B → (20) CRC 1
U7-D, U7-C → (19) CRC 2
U5-A, U5-B → (15) CRC 3
U5-D, U5-C → (14) CRC 4
U4-A, U4-B → (13) CRC 5
U4-D, U4-C → (12) CRC 6
U2-A, U2-B → (7) CRC 7

REFERENCE DESIGNATORS

LAST USED	DELETED
R25	
C10	
CR5	
Q6	
U33	
TP15	

TOLERANCES	PERIPHERAL EQUIPMENT CORP
DRAWN: EMD	
TITLE	SCHEMATIC, CRC GENERATOR
DATE	6-5-68
DRAWING NUMBER	100264
ISSUE	B

DATE	SYM	REVISION RECORD	AUTH	DR.	CK.
7/24/68	A	ECN 1-82	EMD	JC	WJA
8/1/68	B	ECN 100	VM	[illegible]	[illegible]
11/26/68	C	ECN 182	EMD	[illegible]	WJA

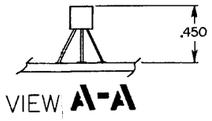


4 TABLE I

PART NO.	REF. DESIGNATION
200-4123	Q1-6
300-4446	CR1-5
131-1020	C5,8,9,10
131-2220	C4
131-3320	C3
131-1530	C2
132-2752	C1,6,7
101-1515	R1
101-1025	R8,9,12,13,14,21,24,25
101-2725	R10,22
101-3325	R2,11,15,23
101-4725	R5,7,18,20
101-6825	R4,6,17,19
700-8360	U3,6,8,16,17,18,19,20,32,
	33
700-8440	U1,10
700-8460	U2,4,5,7,9,21,22,23,24,
	25,26,27,28,29,30,31
700-8520	U11,12,13,14,15
101-2225	R3,16

TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09



4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

3 RUBBER STAMP PART NO., INCLUDING VERSION NO. AND ISSUE NO.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100264
SPEC-100268

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE 2/1	DRAWN BY [illegible]
			APPROVED BY EMD
FRACTIONAL ±	TITLE PCBA CRC GENERATOR		SHEET 1 OF 1
ANGULAR ±	DATE 4-30-68	DRAWING NUMBER 100265	ISSUE C

DATE	SYM	REVISION RECORD	AUTH	DR	CH
[illegible]	A	ECN 1-AN	[illegible]	[illegible]	[illegible]
[illegible]	B	ECN-067	[illegible]	[illegible]	[illegible]
[illegible]	C	ECN 078	[illegible]	[illegible]	[illegible]
8-2	D	ECN-167	[illegible]	[illegible]	[illegible]

5 CONNECTIONS

CIRCUIT	100	200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000	2100
IC	U14	U14	U14	U13	U13	U13	U12	U12	U12	U11	U11	U11	U10	U10	U10	U9	U9	U9	U8	U8	U8
A	13	11	9	13	11	9	13	11	9	13	11	9	13	11	9	13	11	9	13	9	11
B	12	10	8	12	10	8	12	10	8	12	10	8	12	10	8	12	10	8	12	8	10
C	1	3	5	1	3	5	1	3	5	1	3	5	1	3	5	1	3	5	1	5	3
D	2	4	6	2	4	6	2	4	6	2	4	6	2	4	6	2	4	6	2	6	4
W	1	2	3	4	5	6	7	8	9	10	11	12,13	14	15,16	17,18	19	20,21	22	23	24,25	26,27

VERSION TABLE

MODEL	ASSEMBLY	CIRCUITS USED			7	6
		CONFIG A	CONFIG B	CONFIG C		
HIGH-TRUE WRITE	100334-01	100 THRU 1700, 1900 THRU 2100	1800	NONE	USED	NOT USED
LOW-TRUE WRITE	100334-02	NONE	ALL	NONE	USED	NOT USED
HIGH-TRUE READ	100334-03	200 THRU 900, 1300, 1600	1800	NONE	NOT USED	NOT USED
LOW-TRUE READ	100334-04	NONE	200 THRU 900, 1300 1600, 1800	NONE	NOT USED	NOT USED
LOW-TRUE READ	100334-05	NONE	1800	200 THRU 900, 1300, 1600	NOT USED	USED
LOW-TRUE WRITE	100334-06	NONE	1800	100 THRU 1700, 1900 THRU 2100	USED	USED

REFERENCE DESIGNATORS

LAST USED	DELETED
R3	
C9	
U14	
TP23	
S1	
W27	

SEE DWG 100334 FOR ASSEMBLY

ALL CAPACITORS IN MICOFARADS, 20V, 20%

THIS PORTION OF CIRCUIT (ENCLOSED IN BROKEN LINE) IS OMITTED IN SOME ASSEMBLIES. SEE VERSION TABLE ZONE 2E

C3 THRU C8 ARE NOT USED IN ALL ASSEMBLIES. SEE VERSION TABLE

SEE CONNECTION CHART FOR PIN NUMBERS AND WIRE NUMBERS

REFERENCE DESIGNATORS ARE NOT COMPLETE. FOR COMPLETE DES. AND PREFIX OF CIRCUIT TO DESIGNATOR. FOR EXAMPLE: R1 OF CIRCUIT 500 IS R501; C1 OF CIRCUIT 2100 IS C2101
O = ODD PARITY, E = EVEN PARITY, X = EXTERNAL PARITY

TYPICAL OF CIRCUITS 200, 300, 400, 500, 600, 700, 800, 900, 1300, 1600 AND 1900. SEE CONNECTOR FOR PINS USED FOR EACH CIRCUIT. TEST POINTS ARE IDENTIFIED BY CIRCUIT NO. FOR EXAMPLE: TEST POINT OF CIRCUIT 200 IS TP2, CIRCUIT 1600 IS TP16

WHEN CONFIGURATION A IS USED, THE REQUIRED JUMPER CONNECTIONS ARE REPRESENTED THUS: o——o, CONFIGURATION 'B' OR 'C': o= =o. SEE VERSION TABLE FOR CONNECTIONS USED.

ES: UNLESS OTHERWISE SPECIFIED

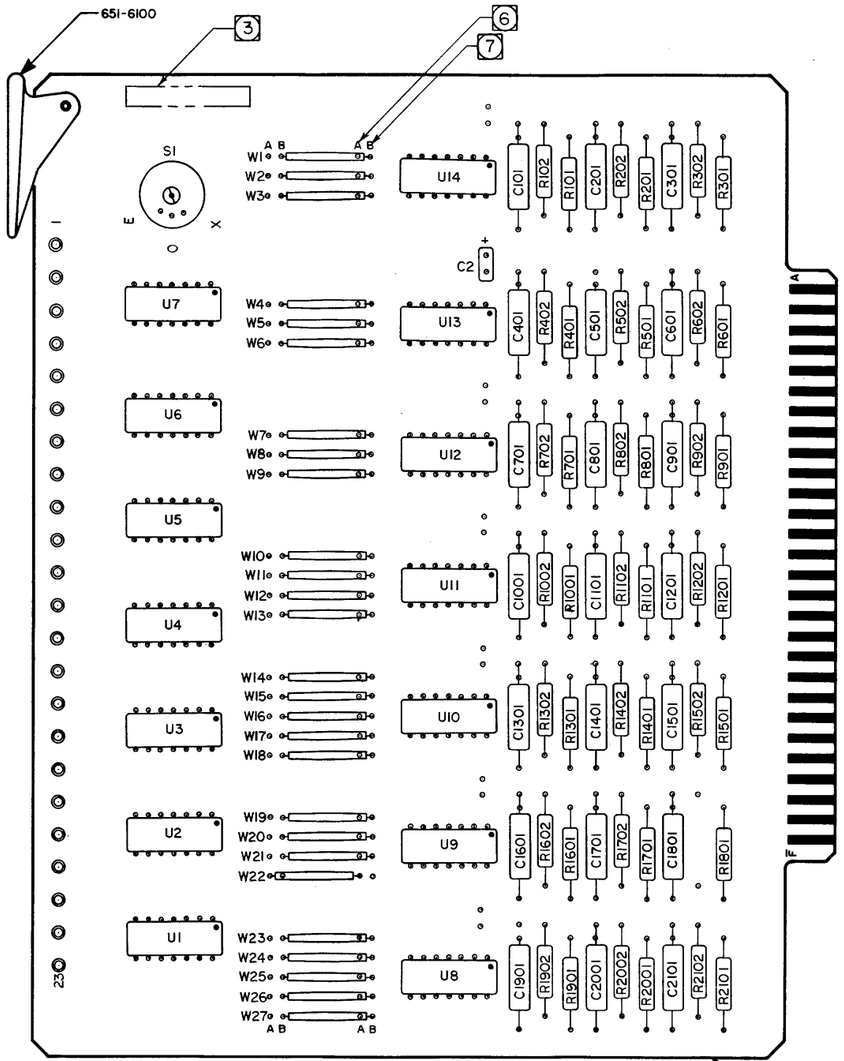
PERIPHERAL EQUIPMENT CORPORATION

SCHEMATIC - RECEIVER, DTL

19 FEB 68 | 100333 | ISSUE D

DATE	BY	REVISION RECORD	AUTH.	QA	CK
2 Jan	A	ERN 1-CC	[illegible]		

INFORMATION ON SHEET 1 APPLIES TO VERSIONS -01,-02,-03,-04.



4 TABLE I

PART NO.	REF DESIGNATION
700-8360	U9,10,12,13,14
132-2752	C2
131-1020	C201-901,1301,1601,1801
101-6805	R201-901,1301,1601,1801
100373-01	W2-9,14,19,22

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL / H-T WRITE / VER. -01	LOW TRUE WRITE -02	HIGH TRUE READ -03	LOW TRUE READ -04	LOW TRUE READ -05	LOW TRUE WRITE -06	-07	-08	-09
U1,4,5,8,11	700-8360	700-8360		NO	SEE	SEE			
U2,3,6,7	700-8460	700-8460		ADDITIONS	SHT 2	SHT 2			
S1	514-8711	514-8711							
C101,1001,1101,1201,1401	131-1020	131-1020							
C1501,1701,1901-2101									
R101,1001,1101,1201 1401	101-6805	101-6805							
R1501,1701,1901-2101									
R202-902,1302,1602	101-4715		101-4715						
R102,1002,1102,1202,	101-4715								
R1402,1502,1702,									
R1902-2102									
W1,10-13,15-18,20,21,	100373-01	100373-01							
W23-27									

6 ALL JUMPERS USED IN VERSIONS -01 AND -03 ARE TO BE INSERTED IN HOLES MARKED "A".

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100333
SPEC-100337

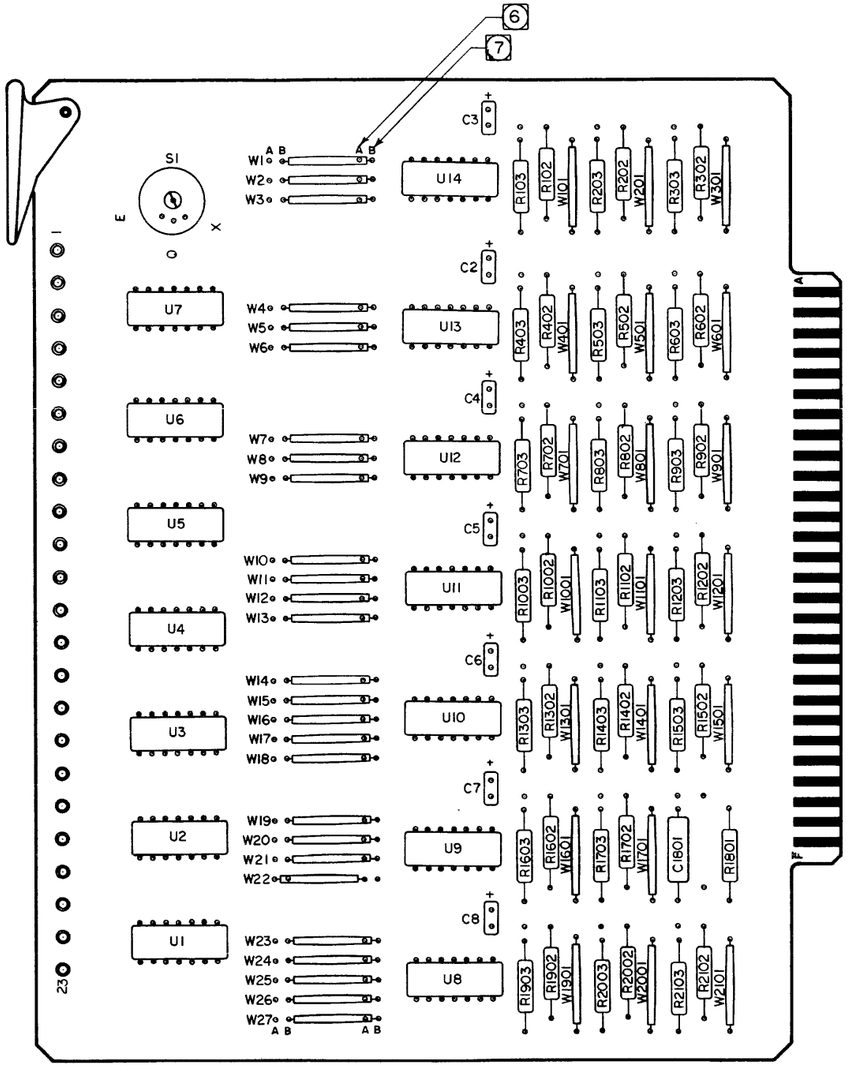
7 ALL JUMPERS USED IN VERSIONS -02,-04,-05, AND -06, EXCEPT W22, ARE TO BE INSERTED IN HOLES MARKED "B".

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE 2/1	DRAWN BY
FRACTIONAL ±	TITLE PCBA RECEIVER DTL		SHEET 1 OF 2
ANGULAR ±	DATE 1/24/66	DRAWING NUMBER 100334	ISSUE A

DATE	BY	REVISION RECORD	APPR.	CHK.	CK.
	A	SEE SHEET 1	CAM	MA	MA

INFORMATION ON SHEET 2 APPLIES TO VERSIONS -05,06.



4 TABLE I

PART NO.	REF DESIGNATION
700-8360	U9,10,12,13,14
131 - 1020	C1801
132 - 2752	C2-8
101 - 6805	R1801
101 - 2215	R203-903,1303,1603
101 - 3315	R202-902,1302,1602
100373-01	W2-9,14,19,22
	W201-901,1301,1601

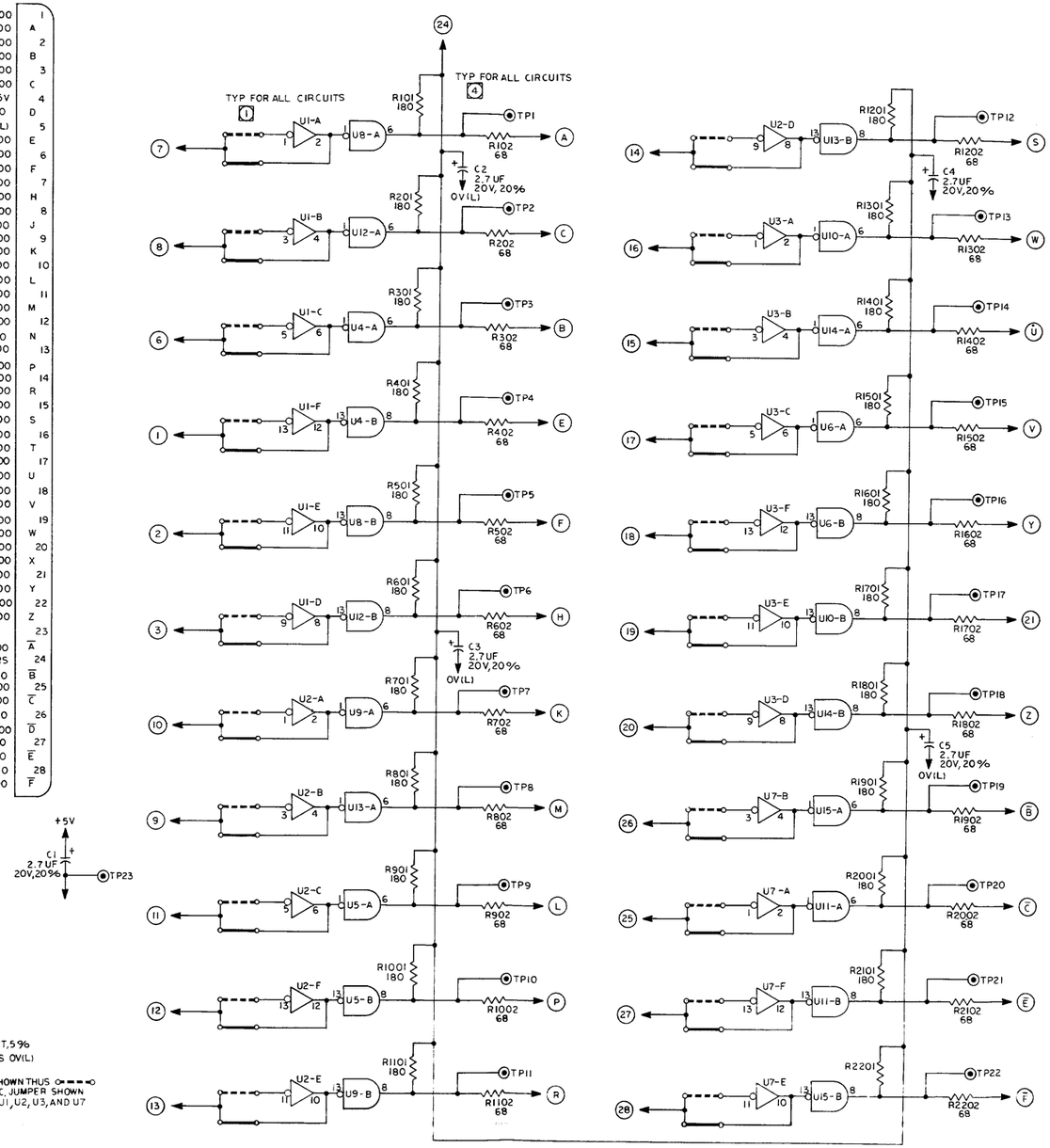
5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05 LOW-TRUE READ	-06 LOW-TRUE WRITE	-07	-08	-09
U1,4,5,8,11					NO ADDITIONS	700-8360			
U2,3,6,7						700-8460			
S1						514-8711			
R102,1002-1202,1402						101 3315			
R1502,1702,1902-2102									
R103,1003-1203,1403,						101 2215			
R1503,1703,1903-2103									
W1,10,11,12,15,16,17,18,						100373-01			
W20,21,23-27									
W101, 1001-1201,1401,									
W1501,1701,1901-2101									

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE 2/1	DRAWN BY / APPROVED
FRACTIONAL ±	TITLE PCBA RECEIVER DTL		SHEET 2 OF 2
ANGULAR ±	DATE May 23, 1983	DRAWING NUMBER 100334	ISSUE A

DATE	SYM	REVISION RECORD	AUTH	DR	CH
1/14/68	A	ECN 1-AN	SW	JS	SW
3/4/68	B	ECN 023	SW	JS	SW

INPUT CIRCUIT 400	1
OUTPUT CIRCUIT 100	A
INPUT CIRCUIT 500	2
OUTPUT CIRCUIT 300	B
INPUT CIRCUIT 600	3
OUTPUT CIRCUIT 200	C
+5V	4
GROUND RETURN CIRCUITS 100,200,300	D
0V(L)	5
OUTPUT CIRCUIT 400	E
INPUT CIRCUIT 300	6
OUTPUT CIRCUIT 500	F
INPUT CIRCUIT 100	7
OUTPUT CIRCUIT 600	H
INPUT CIRCUIT 200	8
GROUND RETURN CIRCUITS 400,500,600	J
INPUT CIRCUIT 800	9
OUTPUT CIRCUIT 700	K
INPUT CIRCUIT 700	10
OUTPUT CIRCUIT 900	L
INPUT CIRCUIT 900	11
OUTPUT CIRCUIT 800	M
INPUT CIRCUIT 1000	12
GROUND RETURN CIRCUITS 700,800,900	N
INPUT CIRCUIT 1100	13
OUTPUT CIRCUIT 1000	P
INPUT CIRCUIT 1200	14
OUTPUT CIRCUIT 1100	R
INPUT CIRCUIT 1400	15
OUTPUT CIRCUIT 1200	S
INPUT CIRCUIT 1300	16
GROUND RETURN CIRCUITS 1000,1100,1200	T
INPUT CIRCUIT 1500	17
OUTPUT CIRCUIT 1400	U
INPUT CIRCUIT 1600	18
OUTPUT CIRCUIT 1500	V
INPUT CIRCUIT 1700	19
OUTPUT CIRCUIT 1300	W
INPUT CIRCUIT 1800	20
GROUND RETURN CIRCUITS 1300,1400,1500	X
OUTPUT CIRCUIT 1700	21
OUTPUT CIRCUIT 1600	Y
GROUND RETURN CIRCUIT 2200	22
OUTPUT CIRCUIT 1800	Z
	23
GROUND RETURN CIRCUITS 1600,1700,1800	$\overline{A}$
PULL-UP RESISTORS	24
OUTPUT CIRCUIT 1900	$\overline{B}$
INPUT CIRCUIT 2000	25
OUTPUT CIRCUIT 2000	$\overline{C}$
INPUT CIRCUIT 1900	26
GROUND RETURN CIRCUITS 1900,2000,2100	$\overline{D}$
INPUT CIRCUIT 2100	27
OUTPUT CIRCUIT 2100	$\overline{E}$
INPUT CIRCUIT 2200	28
OUTPUT CIRCUIT 2200	$\overline{F}$



VERSION TABLE

MODEL	ASSEMBY	CIRCUITS USED	R1	R2	C2 THRU C5
HIGH TRUE	100339-01	100 THRU 1200	USED	USED	USED
HIGH TRUE	100339-02	100 THRU 2200	USED	USED	USED
LOW TRUE	100339-03	100 THRU 1200	USED	USED	USED
LOW TRUE	100339-04	100 THRU 2200	USED	USED	USED
LOW TRUE	100339-05	100 THRU 2200	NOT USED	NOT USED, SUBSTITUTED WITH JUMPER	NOT USED
LOW TRUE	100339-06	100 THRU 1200	NOT USED	NOT USED, SUBSTITUTED WITH JUMPER	NOT USED

REFERENCE DESIGNATOR

LAST USED	DELETED
R2	
C5	
U15	
TP23	

4. SEE VERSION TABLE
3. ALL RESISTORS IN OHMS, 1/2 WATT, 5%
2. ON ALL IC'S PIN14 IS +5V; PIN7 IS 0V(L)
1. FOR LOW-TRUE LOGIC, JUMPER SHOWN THUS ○---○ IS USED. FOR HIGH-TRUE LOGIC, JUMPER SHOWN THUS ○——○ IS USED AND IC U1, U2, U3, AND U7 ARE OMITTED

NOTES: UNLESS OTHERWISE SPECIFIED

PERIPHERAL EQUIPMENT CORPORATION

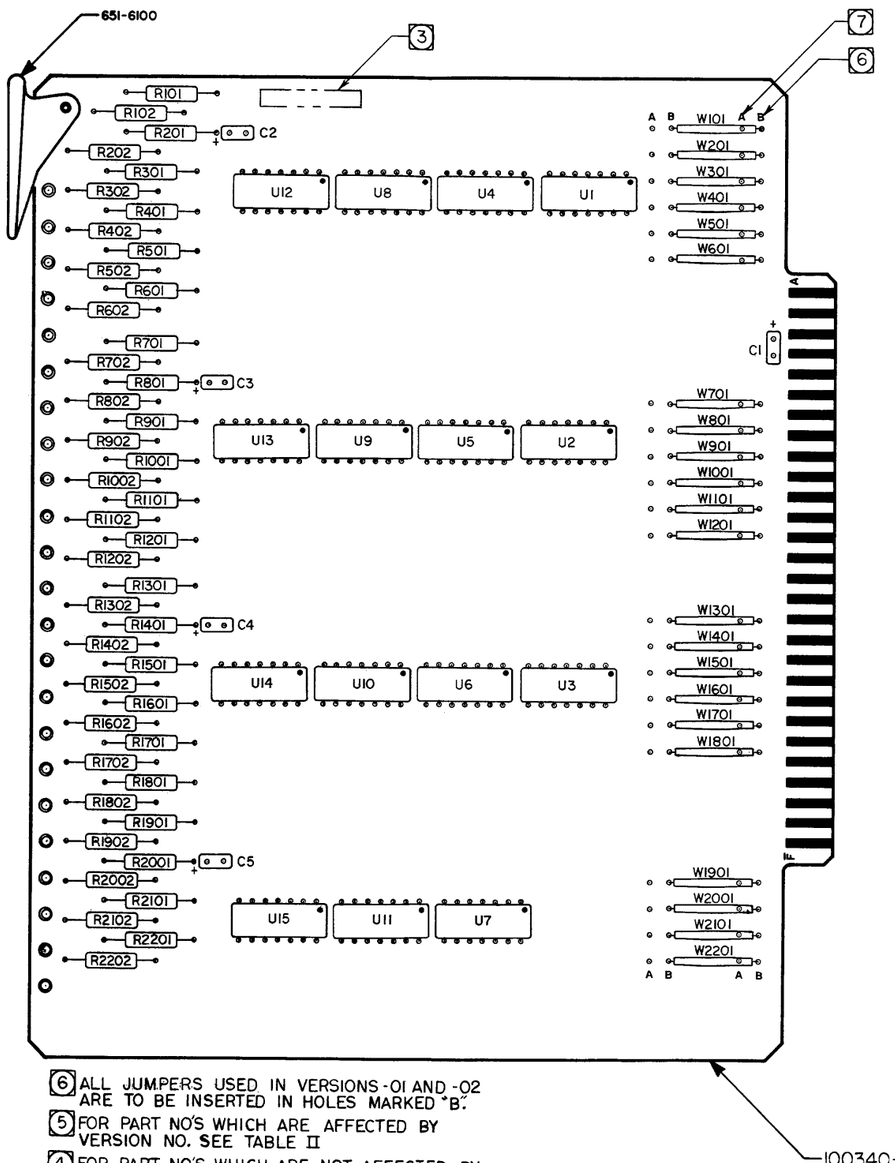
SCHEMATIC-TRANSMITTER DTL

23 FEB 68

100338

ISSUE B

DATE	ETR	REVISION RECORD	AUTH	DR.	CK.
7-21	A	ERN 1-EC	[illegible]	[illegible]	[illegible]



INFORMATION IN TABLES ON SH I APPLIES TO VERSIONS 01,02,03 AND 04

4 TABLE I

PART NO.	REF DESIGNATION
700-8440	U4,5,8,9,12,13
132-2752	C1,2,3
101-1815	R101-1201
101-6805	R102-1202
100373-01	W101-1201

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL / HI-TRUE VER.	HI-TRUE	LOW-TRUE	LOW-TRUE					
	-01	-02	-03	-04	-05	-06	-07	-08	-09
U6,10,11,14,15	NO	700-8440		700-8440					
U1,2	ADDITIONS		700-8360	700-8360					
U3,7				700-8360					
C4,5		132-2752		132-2752					
R1301-2201		101-1815		101-1815					
R1302-2202		101-6805		101-6805					
W1301-2201		100373-01		100373-01					

6 ALL JUMPERS USED IN VERSIONS -01 AND -02 ARE TO BE INSERTED IN HOLES MARKED "B".

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

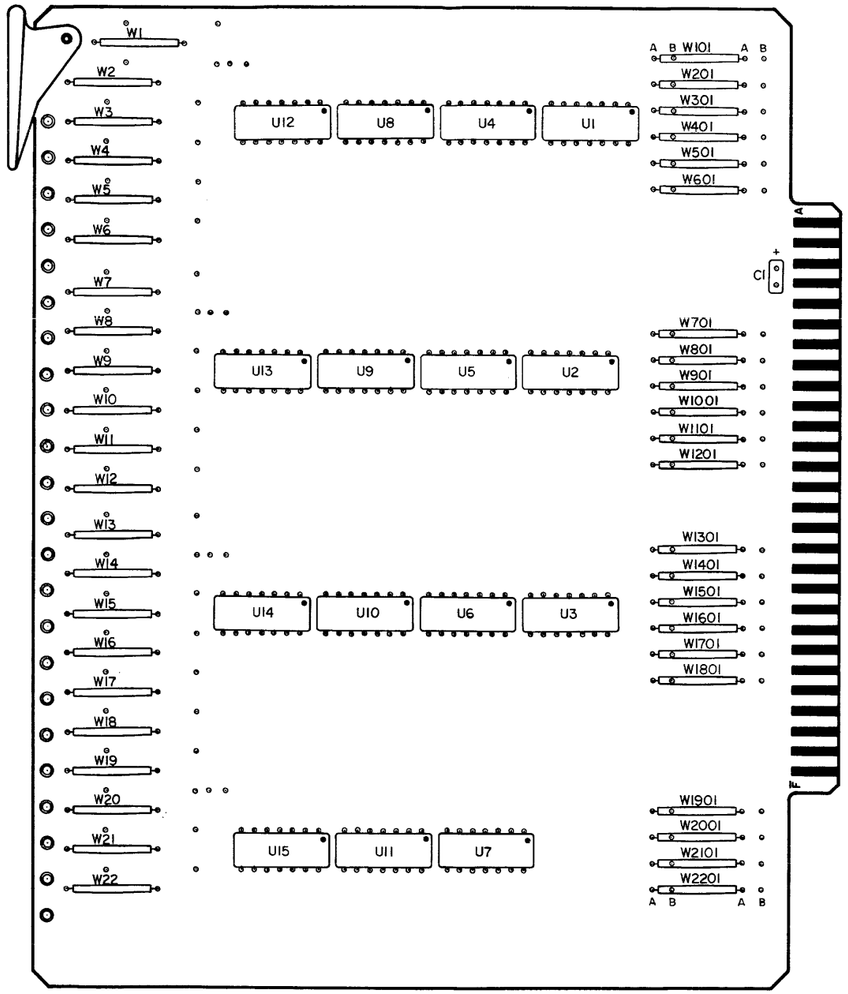
1. REF DWGS: SCHEMATIC-100338
SPEC-100342

7 ALL JUMPERS USED IN VERSIONS -03,04,05 AND -06. ARE TO BE INSERTED IN HOLES MARKED "A".

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED) DECIMAL ±	PERIPHERAL EQUIPMENT CORPORATION	
	SCALE 2/1	DRAWN BY [illegible] APPROVED [illegible]
FRACTIONAL ±	TITLE PCBA TRANSMITTER, DTL	SHEET 1 OF 2
ANGULAR ±	DATE 5-28-68 DRAWING NUMBER 100339	ISSUE A

DATE	BY	REVISION RECORD	AUTH.	ENG.	CHK.
7-29	A	ERN 1-EC			



INFORMATION IN TABLES ON SH 2 APPLIES TO VERSIONS 05 AND 06.

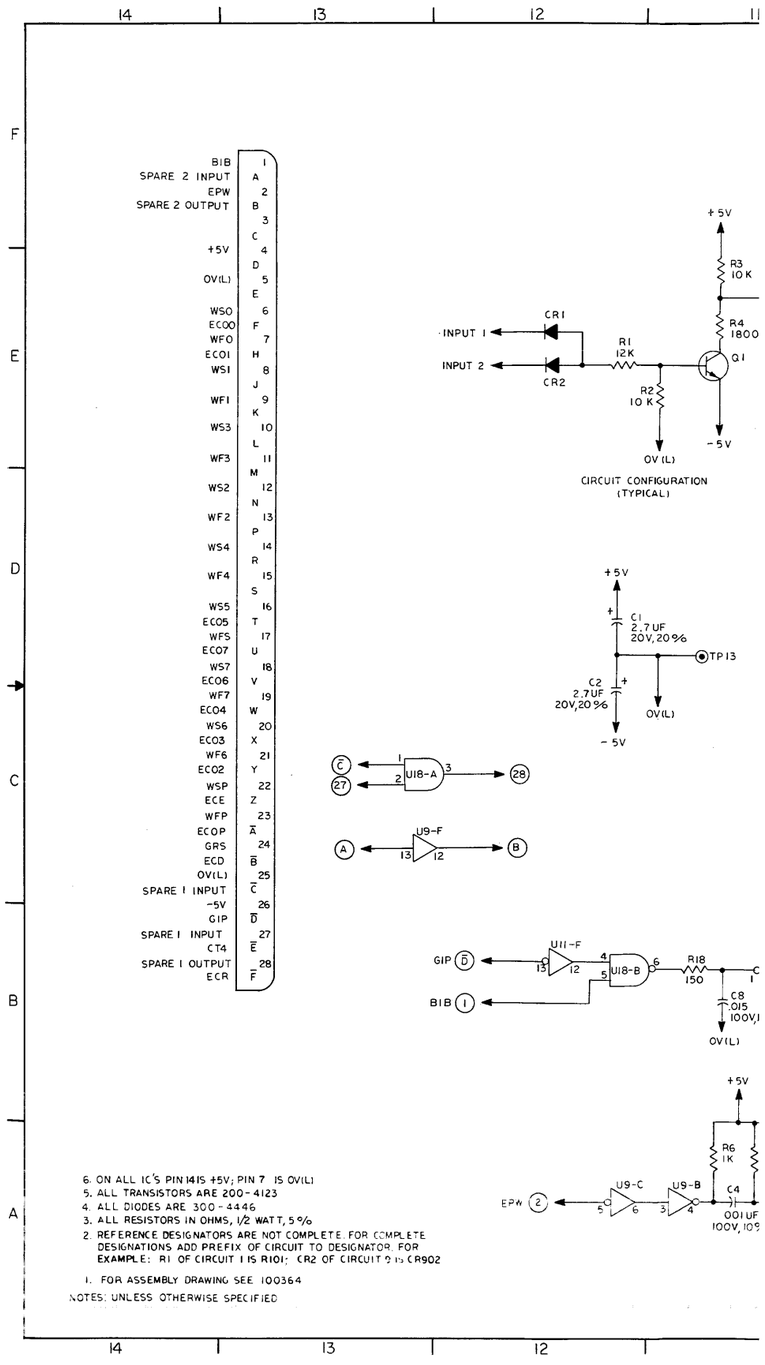
TABLE I

PART NO.	REF DESIGNATION
700-8360	U1,2
700-8440	U4,5,8,9,12,13
132-2752	C1
100373-01	W1-12, 101-1201

TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05 LOW TRUE	-06 LOW TRUE	-07	-08	-09
U3,7					700-8360	NO			
U6,10,11,14,15					700-8440	ADDITIONS			
W13-22,1301-2201					100373-01				

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE 2/1	DRAWN BY
FRACTIONAL ±	TITLE PCBA TRANSMITTER DTL		SHEET 2 OF 2
ANGULAR ±	DATE 5-28-68	DRAWING NUMBER 100339	ISSUE A



6. ON ALL IC'S PIN 14 IS +5V; PIN 7 IS OV(L)
5. ALL TRANSISTORS ARE 200-4123
4. ALL DIODES ARE 300-4446
3. ALL RESISTORS IN OHMS, 1/2 WATT, 5%
2. REFERENCE DESIGNATORS ARE NOT COMPLETE. FOR COMPLETE DESIGNATIONS ADD PREFIX OF CIRCUIT TO DESIGNATOR. FOR EXAMPLE: R1 OF CIRCUIT 1 IS R101; CR2 OF CIRCUIT 9 IS CR902
1. FOR ASSEMBLY DRAWING SEE 100364

NOTES: UNLESS OTHERWISE SPECIFIED

DATE	SYM	REVISION RECORD	AUTH	DR	CH
2-28-68	A	ERN 1-AN	YM	JK	SM
3-14-68	B	ECN 921	EGD	VE	EGD

CIRCUIT CONFIGURATION (TYPICAL)

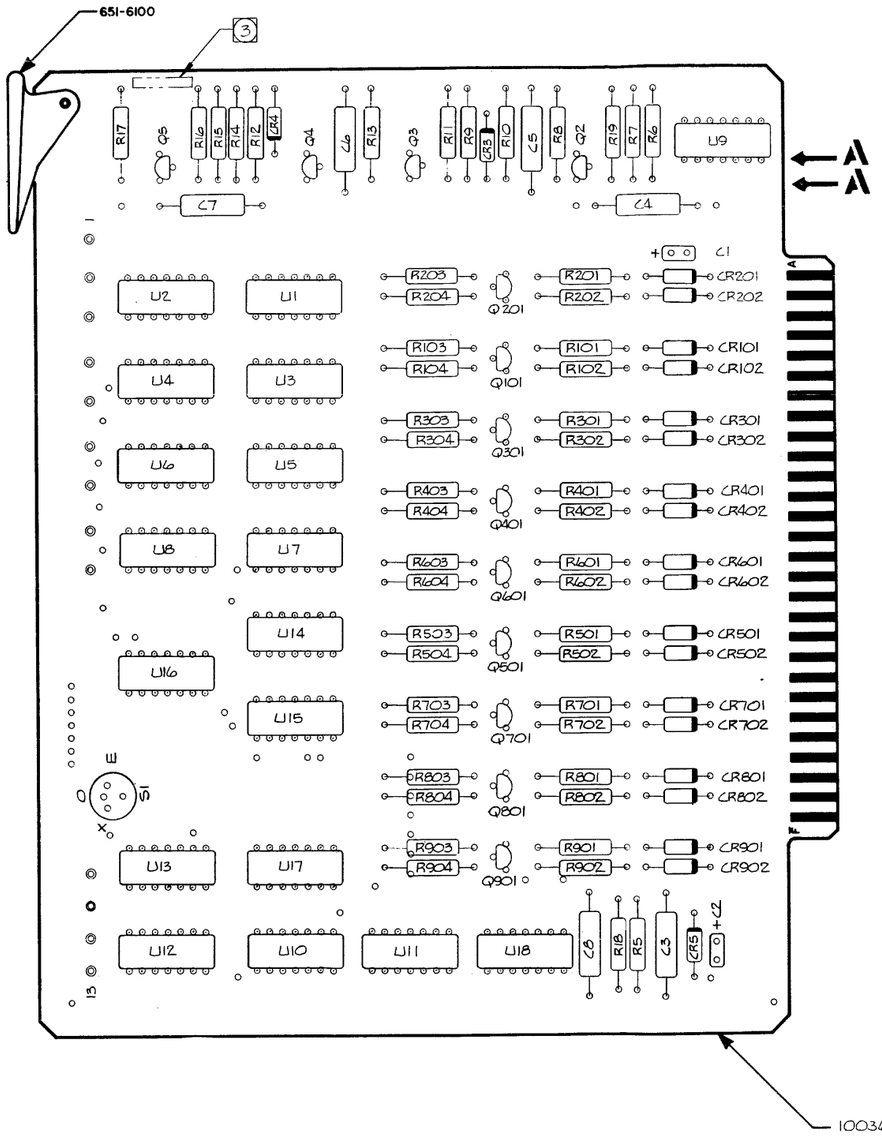
REFERENCE DESIGNATORS	
LAST USED	DELETED
R19	
C8	
CR5	
Q5	
U18	
TP13	

PERIPHERAL EQUIPMENT CORPORATION

SCHEMATIC - ECHO CHECK PARITY

SIZE B | 100363 | REV

DATE	BY	REVISION RECORD	AUTH.	APP.	CK.
8/2	A	ERN 1-EN	GWS		

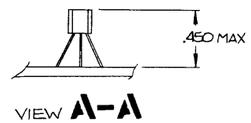


4 TABLE I

PART NO.	REF DESIGNATION
101-1515	R5,18
101-1025	R6,15,19
101-1825	R104-904
101-2225	R9
101-2725	R7,16
101-3325	R8,17,10
101-4725	R12,13
101-6825	R11,14
101-1035	R102-R902,R108-R903
101-1235	R101-R901
131-1020	C4,5,7
131-2220	C6
131-1530	C3,8
132-2752	C1,2
200-4123	Q101-Q901, Q2-Q5
300-4446	CR101-901,102-902,3,4,5
574-8711	S1
700-8360	U1,5,9,11,14,16
700-8460	U2-4,6-8,10,12,13,15,17,18

TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09



3 RUBBER STAMP PART NO., INCLUDING VERSION NO, AND LATEST ISSUE.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC - 100363
SPEC - 100367

NOTES: UNLESS OTHERWISE SPECIFIED

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSIONS, SEE TABLE I.

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE 2/1	DRAWN BY S. FICCEN
FRACTIONAL ±	TITLE PCBA ECHO CHECK PARITY		SHEET 1 OF 1
ANGULAR ±	DATE 7/11/68	DRAWING NUMBER 100364	ISSUE A

TRANSFORMER CONNECTION CHART

LINE VOLTAGE	INPUT LINE TERMINALS "A" TO	"B" TO	CONNECT TERMINALS
117 V	1	7	2 TO 6
200 V	1	6	3 TO 5
240 V	1	7	4 TO 6

J201 5 6 10 19 17 9 11 12 16 25 7 21 24 8 2 4 27 28 26 1 3 14 13 15

J202 14 3 1 26 27 4 12 11 13 28 E 9 F

Q201 Q202 Q203 Q204 Q205 Q206 Q207 Q208 Q209 Q210

R201 R202 R203

Q211 201-3228

TB201 1 5 6 2 3 4 7 8

K201 CR202 CR203 CR204

E202 E201 E203

J213 Y X W

R204 20

XF203 XF201 XF202

CR201 320-9622

C201 18000 C202 18000

T201 511-0206

(7) P102 & J102 IS SUPPLIED WITH 10-1/2 IN. REEL TRANSPORTS ONLY.

(6) MT301 IS SUPPLIED WITH INCREMENTAL TRANSPORTS ONLY UNIT WILL BE SHIPPED WITH PINS 1&2 OF TB301 CONNECTED TO EITHER PINS 6&7 OR 8&9 OF MT301

(5) SEE TRANSFORMER CONNECTION CHART, ZONE 12E

4. ALL DIODES ARE 300-4426

3. ALL TRANSISTORS ARE 200-3055

2. ALL CAPACITORS IN MICROFARADS, 20%, 25 V. UNLESS

1. ALL RESISTORS IN OHMS 2.0 WATT, 10 %

NOTES: UNLESS OTHERWISE SPECIFIED

DATE	SYM	REVISION RECORD	AUTH	DR	CH
2/18	A	ERN 1-AK	SM	JE	SM
3/19	B	ERN 020	SM	JE	SM
4/19	C	RELEASE & REDRAWN - ECN 116	SM	JE	WF

ELECTRONIC ASSY | TRANSPORT ASSY

J202 (14 3 1 26 27 4 12 11 13 28 E 9 F) (18 17 16 X J 6 7 F)

10 19 17 9 11 12 16 25 7 21 24 8 2 4 27 28 26 1 3 14 13 15

Q201 Q202 Q203 Q204 Q205 Q206 Q207 Q208 Q209 Q210

R201 R202 R203

Q211 201-3228

TB201 (1 5 6 2 3 4 7 8)

XF201 XF202

CR201 320-9622

C201 18000 C202 18000

J203 (I D F 10 B 24 J 18 E C)

J203 (16 S 25)

P102 | J102

BL BK BJ BH BF BE BD BX BV BZ CA BW BY BN BM BT BU BS BR BP CP CE CJ CH CC CN CM CR A B D C CK CF CD CB AA AE AF K L

CAPSTAN DRIVE ASSY (6)

B301 MT301 T301

TB301 (5 6 1 2 7 8)

TB101 (4 5 8 2 1 7 3 6)

BLACK RED B101

RED BLACK B102

R101 1K 1W R102 1K 1W

TB102 (7 8 3 2 1 4 5 6)

S101 .3(NC) 2(C) 1(NO)

-5V

ORANGE RED BROWN YELLOW

+5V 0V EOT BOT

PHOTO TAB DETECTOR

S102 POWER

S103 LOAD FWD

S104 FILE GAP/ FORWARD

S105 READY

S106 REWIND

WRITE LOCKOUT ASSY

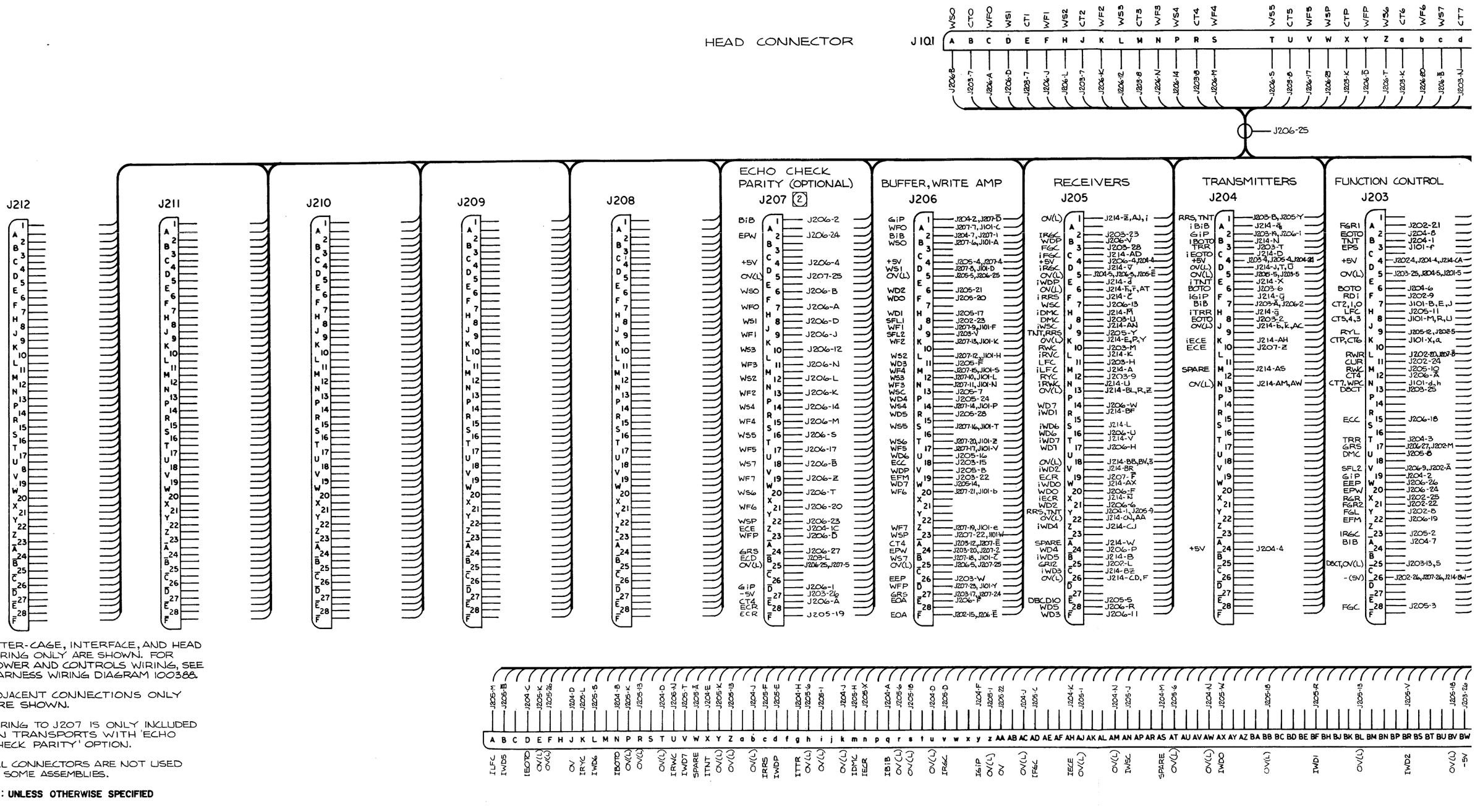
1(NC) 2(C) S401

3(NC) 1(NO) S402

2(C) 3 K Ω E402

CR401 E401 K401

TOLERANCES		DEB-BRIER EQUIPMENT CORPORATION	
		SCALE	DRAWN BY J.E. 14-FEB-68
			APPROVED BY W.F. 14-FEB-68
		TITLE SCHEMATIC - POWER AND HARNESS WIRING	
		DATE 12 FEB 68	DRAWING NUMBER 100388
			ISSUE


HEAD CONNECTOR
J101
WS0 CT0 WF0 WS1 CT1 WF1 WS2 CT2 WF2 WS3 CT3 WF3 WS4 CT4 WF4 WS5 CT5 WF5 WSP CTP WFP WS6 CT6 WF6 WS7 CT7
J206-25
J212
J211
J210
J209
J208
ECHO CHECK PARITY (OPTIONAL)
J207 2
BUFFER, WRITE AMP
J206
RECEIVERS
J205
TRANSMITTERS
J204
FUNCTION CONTROL
J203
+5V
J204-4
4. INTER-CAGE, INTERFACE, AND HEAD WIRING ONLY ARE SHOWN. FOR POWER AND CONTROLS WIRING, SEE HARNESS WIRING DIAGRAM 100388.
3. ADJACENT CONNECTIONS ONLY ARE SHOWN.
2 WIRING TO J207 IS ONLY INCLUDED ON TRANSPORTS WITH 'ECHO CHECK PARITY' OPTION.
1. ALL CONNECTORS ARE NOT USED IN SOME ASSEMBLIES.
NOTES: UNLESS OTHERWISE SPECIFIED

DATE	SYM	REVISION RECORD	AUTH	DR	CH
7-26	A	ERN 1-EA			

WS3 CT3 WF3 WS4 CT4 WF4 WS5 CT5 WF5 WSP CTP WFP WS6 CT6 WF6 WS7 CT7 WF7 EPS WPC

L M N P R S T U V W X Y Z a b c d e f h — HEAD FRAME

J206-12 J203-8 J206-N J206-14 J203-8 J206-M J206-5 J203-8 J206-17 J206-23 J203-K J206-15 J206-T J203-K J206-20 J206-15 J203-N J206-Z J205-3 J203-N J204-5

J206-25

ERS

- J214-Ē, AJ, i
- J203-23
- J206-V
- J203-28
- J214-AD
- J206-4, J204-4
- J214-V
- 14-5, J206-5, J205-Ē
- J214-d
- J214-h, F, AT
- J214-Z
- J206-13
- J214-FR
- J203-U
- J214-AN
- J205-Y
- J214-E, P, Y
- J203-M
- J214-K
- J203-H
- J214-A
- J203-9
- J214-U
- J214-BL, R, Z
- J206-W
- J214-BF
- J214-L
- J204-U
- J214-V
- J206-H
- J214-BB, BV, 3
- J214-BR
- J207-F
- J214-AX
- J206-F
- J214-N
- J206-6
- J204-1, J205-9
- J214-CN, AA
- J214-CJ
- J214-W
- J206-P
- J214-B
- J202-L
- J214-BZ
- J214-CD, F
- J205-5
- J206-R
- J206-11

TRANSMITTERS
J204

RRS, TNT	A	1	J203-B, J205-Y
iBiB		2	J214-ā
GiP		3	J203-N, J206-1
iBOTO	B		J214-N
TRR			J203-T
iEOTO	C	4	J214-D
+5V			J203-4, J205-4, J204-21
OV(L)	D	5	J214-J, T, U
OV(L)			J206-5, J203-5
iTNT	E	6	J214-X
BOTO			J203-6
iGiP	F	7	J214-g
BiB			J203-Ā, J206-2
iTRR	H	8	J214-ḡ
EOTO			J203-2
OV(L)	J	9	J214-b, k, AC
iECE	K	10	J214-AH
ECE			J207-Z
	L	11	
SPARE	M	12	J214-AS
OV(L)	N	13	J214-AM, AW
	P	14	
	R	15	
	S	16	
	T	17	
	U	18	
	V	19	
	W	20	
	X	21	
	Y	22	
	Z	23	
+5V	A	24	J204-4
	B	25	
	C	26	
	D	27	
	E	28	
	F		

FUNCTION CONTROL
J203

F&R1	A	1	J202-21
EOTO		2	J204-6
TNT	B	3	J204-1
EPS			J101-f
+5V	C	4	J202-4, J204-4, J214-CA
OV(L)	D	5	J203-25, J204-5, J201-5
BOTO	E	6	J204-6
RDi		7	J202-9
CT2, 1, 0	F		J101-B, E, J
LFC	H	8	J205-11
CT5, 4, 3			J101-M, R, U
RYL	J	9	J205-12, J202-5
CTP, CT6	K	10	J101-X, a
RWR	L	11	J202-20, J207-B
CLR			J202-24
RWC	M	12	J205-10
CT4			J206-Ā
CT7, WPC	N	13	J101-d, h
DECT			J203-25
	P	14	
ECC	R	15	J206-18
	S	16	
TRR	T	17	J204-3
GRS			J206-27, J202-M
DMC	U	18	J205-8
SFL2	V		J206-9, J202-Ā
GiP		19	J204-2
EEP	W		J206-26
EPW		20	J206-24
R&R	X	21	J202-25
F&R2			J202-22
F&L	Y	22	J202-8
EFM			J206-19
IR&C	Z	23	J205-2
BIB	A		J204-7
	B	24	
DECT, OV(L)		25	J203-13, 5
-(5V)	C	26	J202-26, J207-26, J214-BW
	D	27	
	E	28	
F&C	F		J205-3

CAPSTAN DRIVE
J202

+16V	A	1	J201-1
		2	
+10V	B	3	J201-3
+5V	C	4	J203-4, J201-4
RYC	D	5	J203-9
	E	6	
	F	7	
F&R1	H	8	J202-21
F&L			J203-Y
RDI	J	9	J203-F
RWR	K		J202-20
&R12	L	10	J205-25
&RS	M	11	J203-17
	N	12	
	P	13	
OV(S)	R	14	J201-14
EOA	S	15	J206-F
	T	16	
	U	17	
	V	18	
	W	19	
RWR	X	20	J205-L, J202-K
F&R1	Y	21	J205-A, J202-H
F&R2	Z	22	J203-21
	A	23	
SFL1	B	24	J206-8
SFL2	C		J203-V
CLR	D		J203-11
R&R	E	25	J203-X
-5V	F	26	J203-26, J204-26
-10V		27	J201-27

REEL SERVO
J201

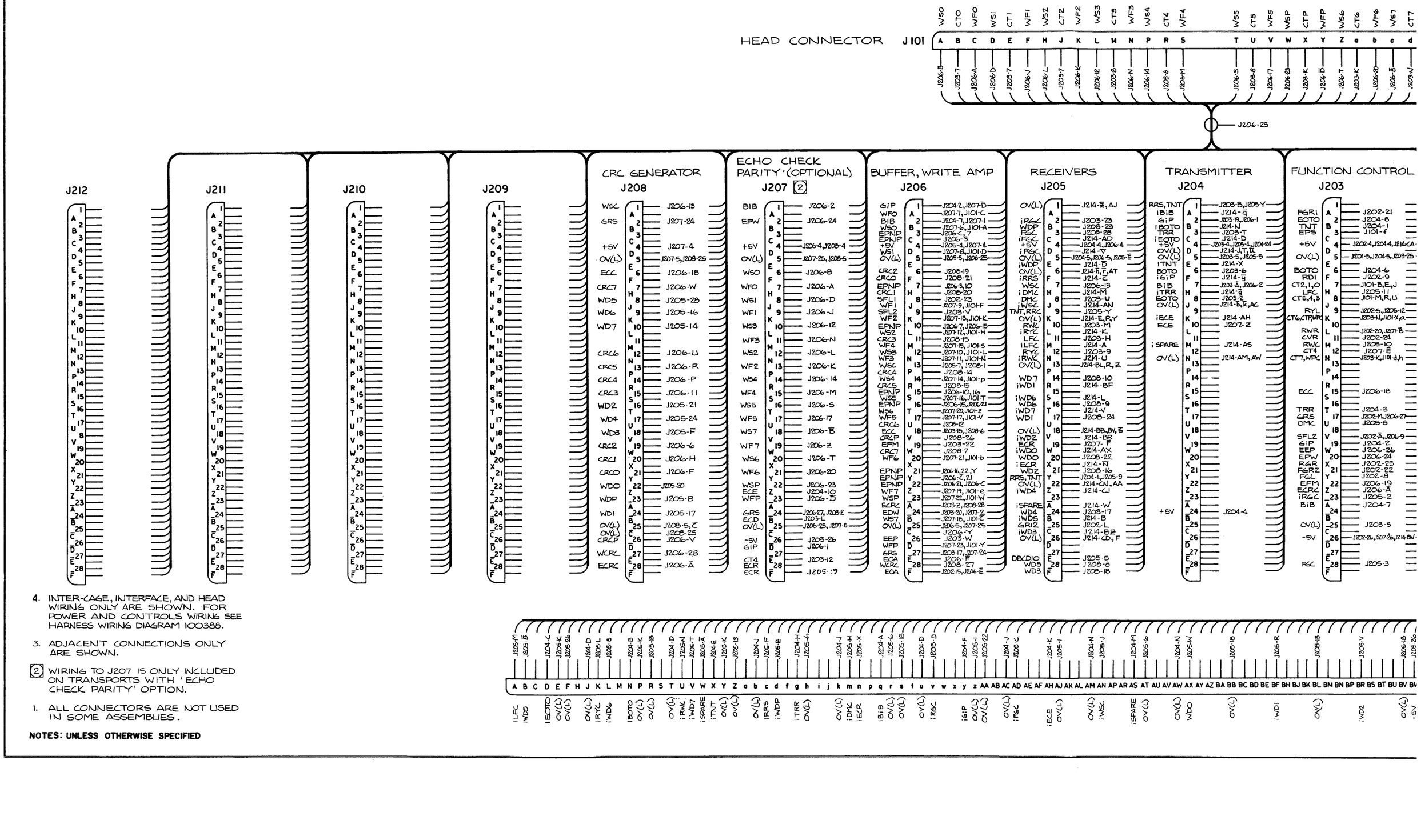
+16V	A	1	J202-1
	B	2	
+10V	C	3	J202-3, J214-CR
+5V	D	4	J202-4
OV(L)	E	5	J201-25, J208-5
	F	6	
	H	7	
	J	8	
	K	9	
	L	10	
	M	11	
	N	12	
	P	13	
OV(S)	R	14	J202-14
	S	15	
	T	16	
	U	17	
	V	18	
	W	19	
	X	20	
	Y	21	
	Z	22	
	A	23	
	B	24	
OV(L)	C	25	J201-5, J214-CE
-5V	D	26	J202-26
-10V	E	27	J202-27, J214-CL
	F	28	

J204-N J205-J J204-M J205-6 J204-N J205-W J205-16 J205-R J205-13 J205-V J205-18 J203-26 J205-2 J203-4 J205-26 J201-25 J205-21 J201-27 J205-22 E204 J201-3

L AM AN AP AR AS AT AU AV AW AX AY AZ BA BB BC BD BE BF BH BJ BK BL BM BN BP BR BS BT BU BV BW BX BY BZ CA CB CC CD CE CF CH CJ CK CL CM CN CP CR CS — J214 INTERFACE CONNECTOR

OV(L) INSC SPARE OV(L) OV(L) INDO OV(L) INDI OV(L) INWD2 OV(L) -5V INDO3 +5V OV(L) OV(L) INDO4 -10V OV(L) CHASSIS GRD +10V

TOLERANCES (EXCEPT AS STATED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE	DRAWN BY E. FICKEN
FRACTIONAL ±	TITLE WIRING DIAGRAM - INCREMENTAL WRITE, DTL INTERFACE, ECHO CHECK		APPROVED BY
ANGULAR ±	DATE 6/3/68	DRAWING NUMBER 100493	REV A



4. INTER-CAGE, INTERFACE, AND HEAD WIRING ONLY ARE SHOWN. FOR POWER AND CONTROLS WIRING SEE HARNESS WIRING DIAGRAM 100388.
3. ADJACENT CONNECTIONS ONLY ARE SHOWN.
(2) WIRING TO J207 IS ONLY INCLUDED ON TRANSPORTS WITH 'ECHO CHECK PARITY' OPTION.
1. ALL CONNECTORS ARE NOT USED IN SOME ASSEMBLIES.

NOTES: UNLESS OTHERWISE SPECIFIED

DATE	SYM	REVISION RECORD	AUTH	DR	CH
7-26	A	ERN 1-EA	SMV		JE

WF2 WS3 CT3 WF3 WS4 CT4 WF4 WS5 CT5 WF5 WSP CTP WFP WS6 CT6 WF6 WS7 CT7 WF8 EPS WPE

K L M N P R S T U V W X Y Z a b c d e f h — HEAD FRAME

J206-K J206-12 J203-8 J206-N J206-14 J203-8 J206-M J206-S J203-8 J206-17 J206-23 J203-K J206-D J206-T J203-K J206-20 J206-B J203-J J206-E J203-3 J203-N J204-S

J206-25

ERS

- J214-Z, AJ
- J203-Z3
- J208-28
- J214-AD
- J204-4, J206-4
- J214-Y
- 204-5, J206-5, J205-E
- J214-D
- J214-h, f, AT
- J214-C
- J206-13
- J214-M
- J203-U
- J214-AN
- J205-Y
- J214-E, P, Y
- J203-M
- J214-K
- J203-H
- J214-A
- J203-9
- J214-U
- J214-BL, R, Z
- J206-10
- J214-BF
- J214-L
- J206-9
- J214-V
- J208-24
- J214-BB, BV, 3
- J214-BR
- J207-F
- J214-AX
- J208-22
- J214-N
- J208-16
- J204-1, J205-9
- J214-CJ, AA
- J214-CJ
- J214-W
- J208-17
- J214-B
- J202-L
- J214-BZ
- J214-CD, F
- J205-5
- J208-6
- J208-18

TRANSMITTER
J204

RRS, TNT	1	A	J203-B, J205-Y
IBiB	2	B	J214-a
GiP	3	C	J203-19, J206-1
IBOTO	4	D	J214-N
TRR	5	E	J203-T
iEOTO	6	F	J214-D
+5V	7	H	J203-4, J205-4, J204-24
OV(L)	8	J	J214-J, T, U
OV(L)	9	K	J203-5, J205-5
ITNT	10	L	J214-X
BOTO	11	M	J203-6
iGiP	12	N	J214-g
BiB	13	P	J203-Ā, J206-Z
iTRR	14	R	J214-a
EOTO	15	S	J203-Z
OV(L)	16	T	J214-B, E, AC
iECE	17	U	J214-AH
ECE	18	V	J207-Z
iSPARE	19	W	J214-AS
OV(L)	20	X	J214-AM, AW
	21	Y	
	22	Z	
	23	A	
+5V	24	B	J204-4
	25	C	
	26	D	
	27	E	
	28	F	

FUNCTION CONTROL
J203

FGR1	1	A	J202-21
EOTO	2	B	J204-8
TNT	3	C	J204-1
EPS	4	D	J101-f
+5V	5	E	J202-4, J204-4, J214-CA
OV(L)	6	F	J201-5, J204-5, J203-25
BOTO	7	H	J204-6
RDI	8	J	J202-9
CT2, 1, 0	9	K	J101-B, E, J
LFC	10	L	J205-11
CT5, 4, 3	11	M	J101-M, R, U
RYL	12	N	J202-5, J205-12
CT6, LTP, WPE	13	P	J203-N, J101-X, a
RWR	14	R	J202-20, J207-B
CVR	15	S	J202-24
RWC	16	T	J205-10
CT4	17	U	J207-E
CT7, WPC	18	V	J203-K, J101-d, h
	19	W	
	20	X	
	21	Y	
	22	Z	
	23	A	
	24	B	
OV(L)	25	C	J203-5
-5V	26	D	J202-26, J207-26, J214-BV
	27	E	
FGL	28	F	J205-3
ECC	15	S	J206-18
TRR	17	U	J204-3
GRS	17	U	J202-M, J206-27
DMC	18	V	J205-8
SFL2	19	W	J202-Ā, J206-9
GiP	19	W	J204-2
EEP	20	W	J206-26
EPW	20	X	J206-24
RGR	21	X	J202-25
FGR2	21	Y	J202-22
FGL	22	Y	J202-8
EFM	22	Z	J206-19
ECRC	23	Z	J204-A
iRGC	23	A	J205-2
BiB	24	A	J204-7

CAPSTAN DRIVE
J202

+16V	1	A	J201-1
	2	B	
+10V	3	C	J201-3
+5V	4	D	J201-4, J203-4
RYL	5	E	J203-9
	6	F	
FGR1	7	H	J202-21
FGL	8	J	J203-Y
RDI	9	K	J203-F
RWR	10	L	J202-20
GR12	11	M	J205-25
GRS	12	N	J203-17
	13	P	
OV(S)	14	R	J201-14
EOA	15	S	J206-F
	16	T	
	17	U	
	18	V	
	19	W	
RWR	20	X	J202-K, J203-L
FGR1	21	Y	J202-H, J203-A
FGR2	22	Z	J203-21
SFL1	23	A	J206-8
SFL2	23	A	J203-V
CVR	24	B	J203-11
RGR	25	C	J203-X
-5V	26	D	J201-26, J208-26
-10V	27	E	J201-27

REEL SERVO
J201

+16V	1	A	J202-1
	2	B	
+10V	3	C	J202-3, J214-CR
+5V	4	D	J202-4
OV(L)	5	E	J201-25, J203-5
	6	F	
	7	H	
	8	J	
	9	K	
	10	L	
	11	M	
	12	N	
	13	P	
OV(S)	14	R	J202-14
	15	S	
	16	T	
	17	U	
	18	V	
	19	W	
	20	X	
	21	Y	
	22	Z	
	23	A	
	24	B	
OV(L)	25	C	J201-5, J214-CE
-5V	26	D	J202-26
-10V	27	E	J202-27, J214-CL
	28	F	

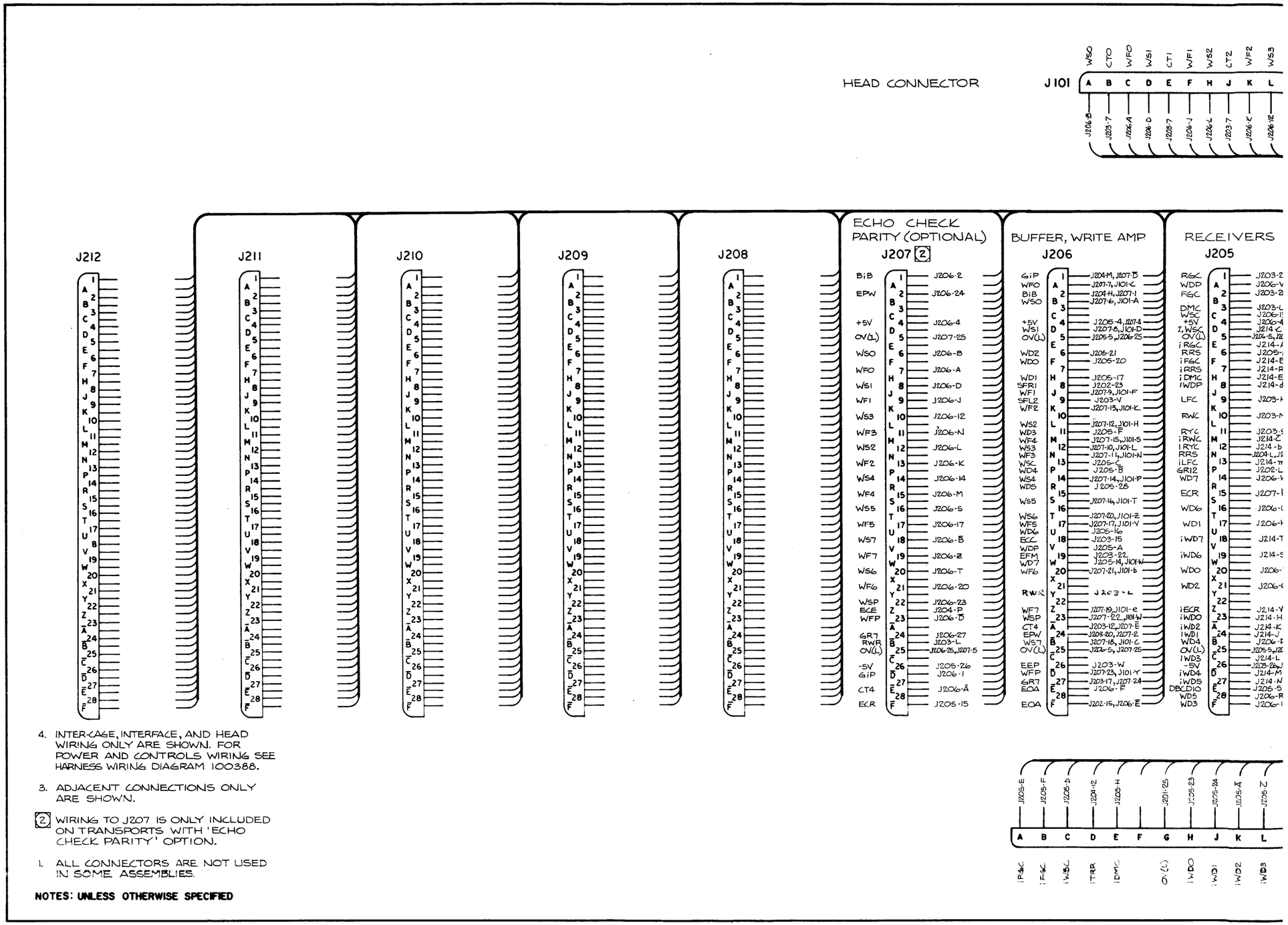
J204-N J205-J J204-M J205-6 J204-N J205-W J205-18 J205-R J205-13 J205-V J205-15 J208-26 J205-2 J203-4 J205-26 J201-5 J205-2 J201-27 J205-22 E204 J201-3

AL AM AN AP AR AS AT AU AV AW AX AY AZ BA BB BC BD BE BF BH BJ BK BL BM BN BP BR BS BT BU BV BW BX BY BZ CA CB CC CD CE CF CH CJ CK CL CM CN CP CR CS

OV(L) iWSC | iSPARE OV(L) | OV(L) WDO | OV(L) iWD1 | OV(L) iWD2 | OV(L) -5V | iWD5 +5V | OV(L) OV(L) | iWD4 -10V | OV(L) CHASSIS GRD +10V

J214 INTERFACE CONNECTOR

TOLERANCES (EXCEPT AS NOTED) DECIMAL ±	PERIPHERAL EQUIPMENT CORPORATION	SCALE	DRAWN BY G. FICKEN
FRACTIONAL ±	TITLE WIRING DIAGRAM - INCREMENTAL WRITE, DTL INTERFACE, ECHO CHECK, CRC		APPROVED
ANGULAR ±	DATE 5/3/66	DRAWING NUMBER 100494	REV A



4. INTER-CAGE, INTERFACE, AND HEAD WIRING ONLY ARE SHOWN. FOR POWER AND CONTROLS WIRING SEE HARNESS WIRING DIAGRAM 100388.

3. ADJACENT CONNECTIONS ONLY ARE SHOWN.

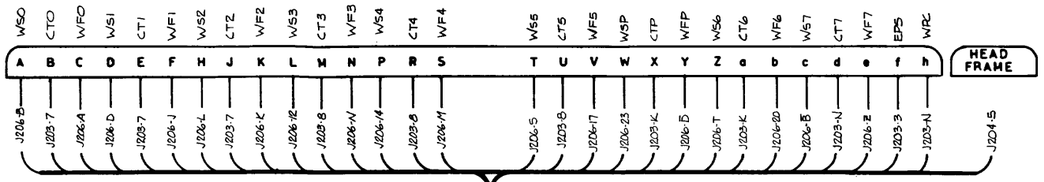
[2] WIRING TO J207 IS ONLY INCLUDED ON TRANSPORTS WITH 'ECHO CHECK PARITY' OPTION.

1. ALL CONNECTORS ARE NOT USED IN SOME ASSEMBLIES.

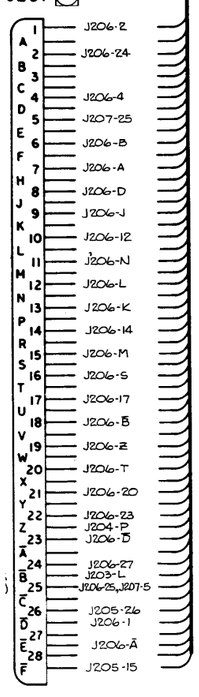
NOTES: UNLESS OTHERWISE SPECIFIED

DATE	SYM	REVISION RECORD	AUTH	DR	CH
7-26	A	ERN 1-5A	Sm		

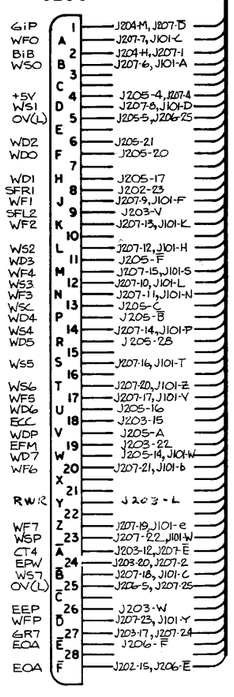
CONNECTOR J101



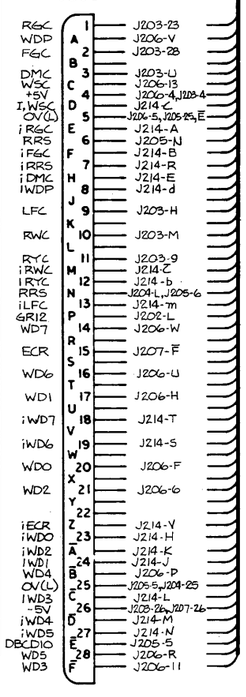
I/O CHECK TY (OPTIONAL) J207 [2]



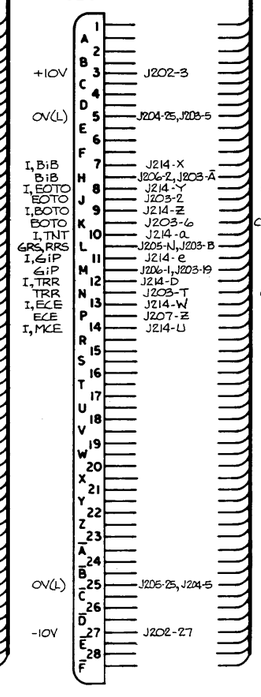
BUFFER, WRITE AMP J206



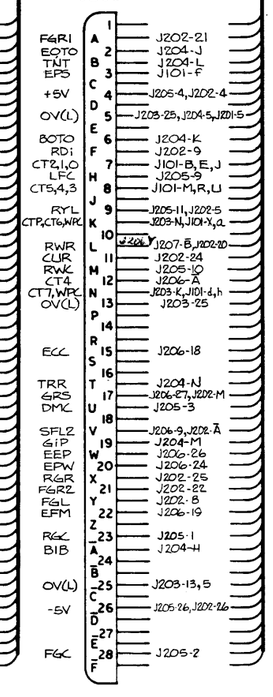
RECEIVERS J205



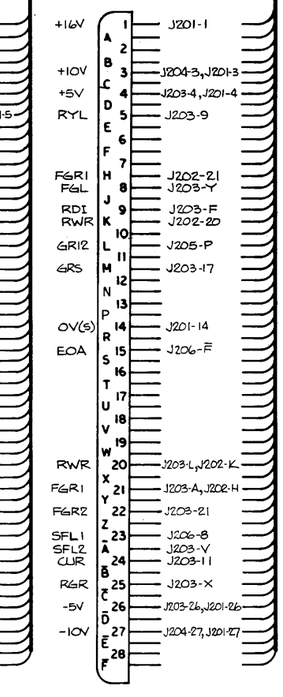
TRANSMITTERS J204



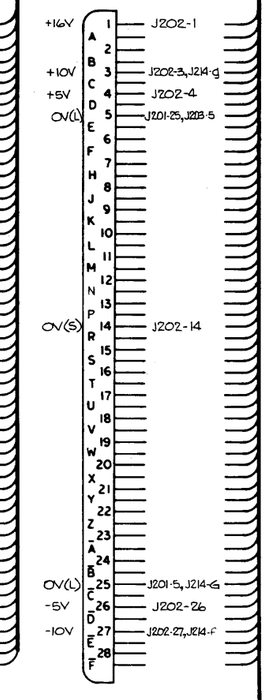
FUNCTION CONTROL J203



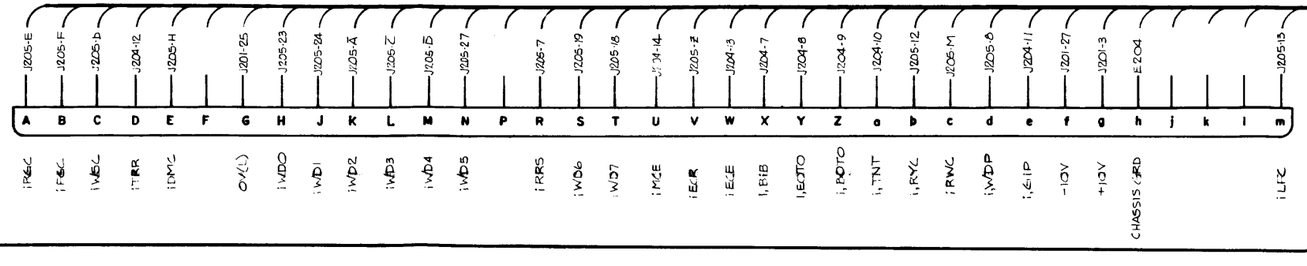
CAPSTAN DRIVE J202



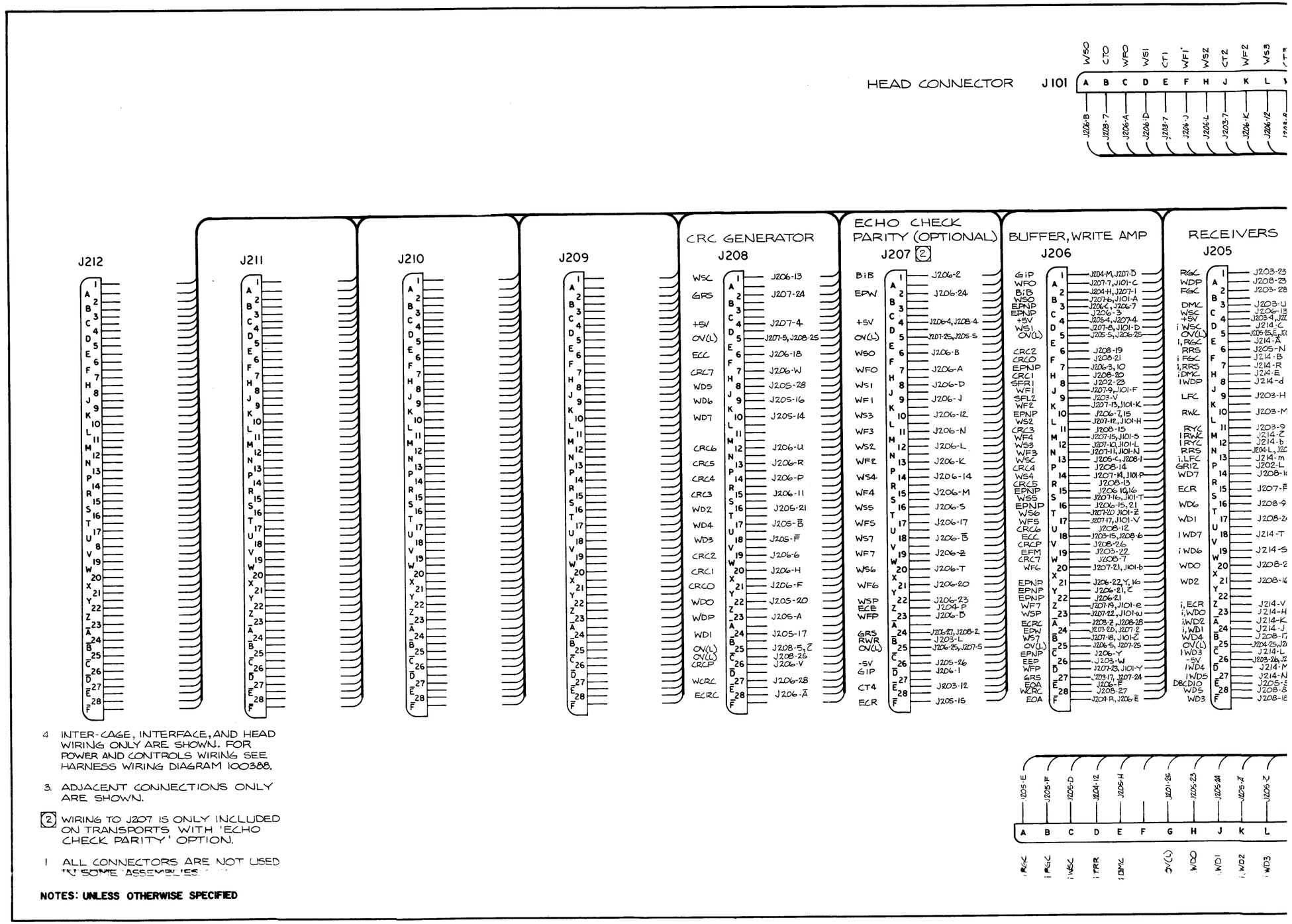
REEL SERVO J201



J214 INTERFACE CONNECTOR



TOLERANCES EXCEPT AS NOTED	PERIPHERAL EQUIPMENT CORPORATION	
DECIMAL ±	DRAWN	CHECKED G FICKEN
FRACTIONAL ±	APPROVED	
ANGULAR ±	TITLE WIRING DIAGRAM - INCREMENTAL WRITE, SLOW INTERFACE, ECHO CHECK	
	DATE 9/4/68	DRAWING NUMBER 100496 REV A



4 INTER-CAGE, INTERFACE, AND HEAD WIRING ONLY ARE SHOWN. FOR POWER AND CONTROLS WIRING SEE HARNESS WIRING DIAGRAM 100388.

3. ADJACENT CONNECTIONS ONLY ARE SHOWN.

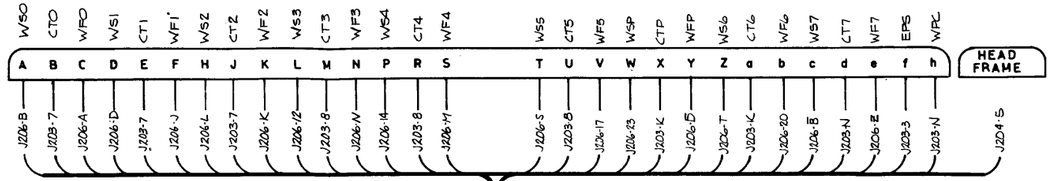
[2] WIRING TO J207 IS ONLY INCLUDED ON TRANSPORTS WITH 'ECHO CHECK PARITY' OPTION.

1 ALL CONNECTORS ARE NOT USED IN SOME ASSEMBLIES.

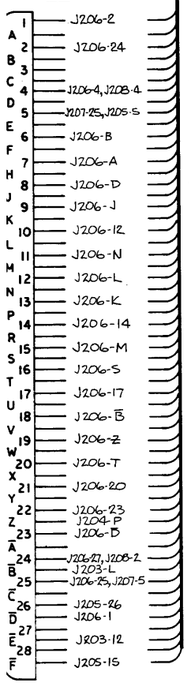
NOTES: UNLESS OTHERWISE SPECIFIED

DATE	SYM	REVISION RECORD	AUTH	DR	CH
7-26	A	ERN 1-EA	SW		JE

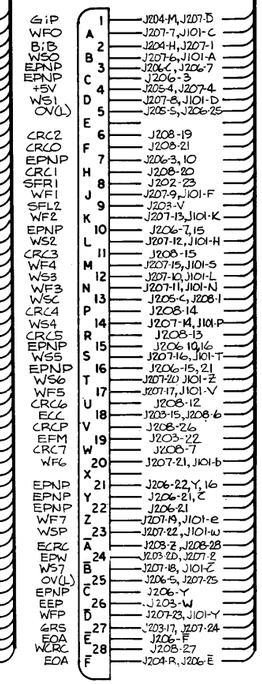
AD CONNECTOR J101



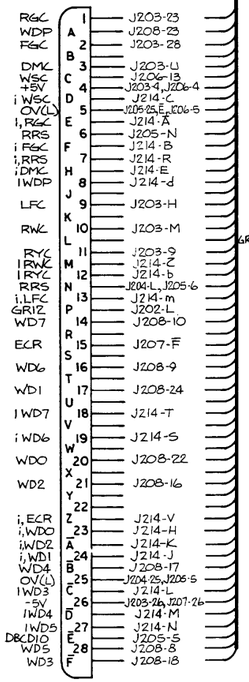
CHECK TY (OPTIONAL) 207 (2)



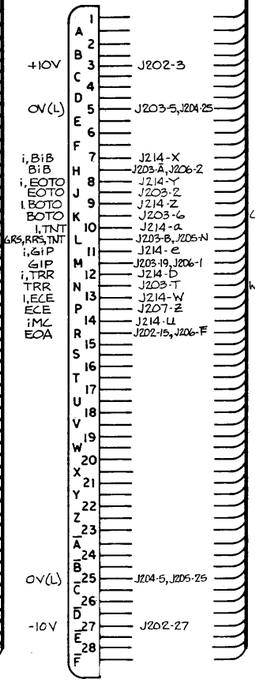
BUFFER, WRITE AMP J206



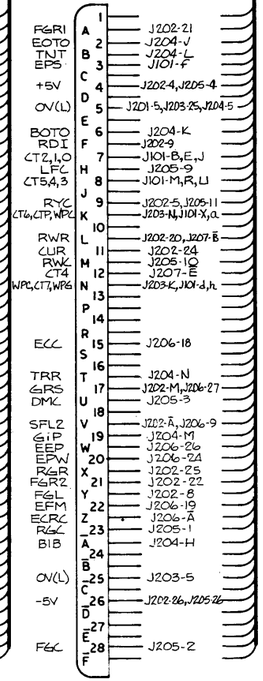
RECEIVERS J205



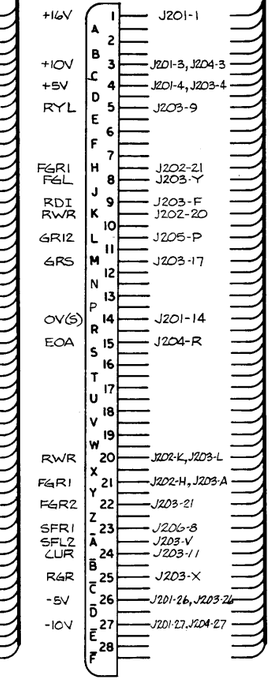
TRANSMITTERS J204



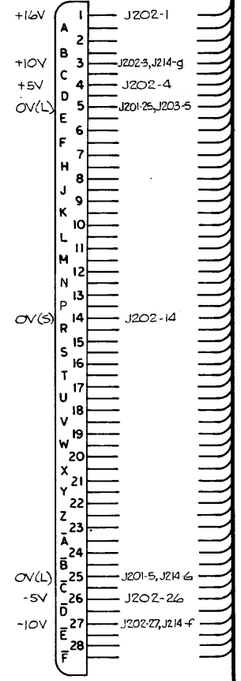
FUNCTION CONTROL J203

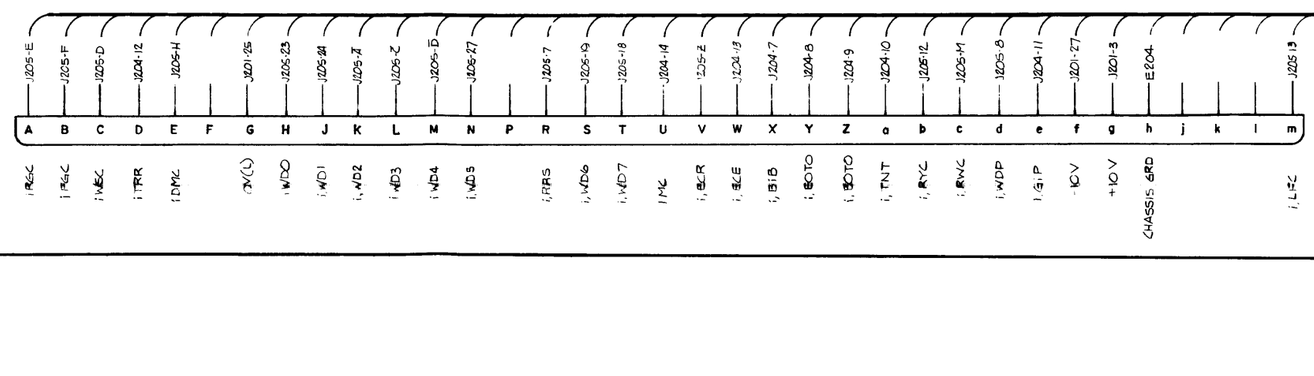


CAPSTAN DRIVE J202



REEL SERVO J201





J214 INTERFACE CONNECTOR

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE	DRAWN BY S.W. FICKEN
			APPROVED BY
FRACTIONAL ±	TITLE WIRING DIAGRAM - INCREMENTAL WRITE, SLOW INTERFACE, ECHO CHECK & CRC		
ANGULAR ±	DATE 6/4/68	DRAWING NUMBER 100497	REV A