5.20 LARGE CAPACITY DISK CONTROLLER (LCDC) THEORY

The large capacity disk controller (LCDC) will be described on two levels: (1) a functional description, and (2) a page by page logic description.

5.20.1 FUNCTIONAL DESCRIPTION

The Large Capacity Disk subsystem has three basic elements: the LCDC, the large capacity disk drive (LCD), and the interfacing cables. The LCDC provides an interface between the system and up to four LCDs. All control, status, and data signals are transferred between the system and the LCD via this interface.

The LCDC consists of two PCBAs, the Control Adaptor and the Data Adaptor. It is installed in the system card cage in place of the Rigid Disk Controller (RDC). It is assigned the same Universal Bus address as the RDC, 0FF10-0FF17. In this address range the LCDC will respond to the standard system bootstrap commands. The LCDC may also be assigned address 0FF18-0FF1F. In this range the LCDC will not respond to the bootstrap sequence. When two LCDCs are installed, one is set to each address range.

The LCD subsystem to system interface characteristics are consistant with the other XL device controllers, except the LCDC and drives appear to the system software as four individual controllers. The LCDC is timeshared between the system and the drives and is capable of supporting four concurrent tasks (if four drives are attached). Once a task is initiated, it is executed sequentially with the LCDC and Bus devoting whatever time and resources are necessary to support command, status, or data transfers. Due to the limitations imposed by shared LCDC hardware, true concurrency involves a large amount of device latency with short bursts of high speed data transfers. This mode of operation allows the LCDC to support a high level of subsystem activity with little or no interference between tasks.

The system software initiates a task by constructing a command list, or channel program, in memory and starting its execution. A channel program is in contiguous memory locations and consists of LCDC and LCD commands and buffer discriptors. The software initiates a channel by providing the LCDC with the starting address and the LCD device number assigned to the task.

The LCDC then accesses the channel program and executes the program. LCDC instructions are provided to output LCD commands, to input and buffer status information, to transfer data to and from DMA buffers in main memory, and to end the channel program when the task is complete. As each LCDC instruction is processed, the LCDC monitors current task status. If the task status is not consistent with the LCDC instruction (for example, finding an input transfer command during a write sequence) the task is terminated and an ABNORMAL END status is posted.

As each command is received, the LCDC interprets and executes it. For example, a read operation positions the drive read/write heads to the specified cylinder (seek), scans the sector headers to locate the specified sector, reads the data into the specified buffer, verifies the data, and posts final status. When the LCDC has initiated a device operation, it suspends processing that channel program and becomes available for another task. When the device operation is complete, channel program processing is resumed at the next opportunity.

Channel program execution continues in this manner until the task is complete. At this point, an LCDC instruction (End Channel Program) directs the LCD to post final device status and terminate the task. If the LCDC detects an error that cannot be handled by itself, the task if terminated in such a manner as to leave a certain amount of residual status in the LCDC to allow software diagnosis of the error and facilitate recovery.

Certain logic functions of the LCD interfaces are implemented by common hardware which must be shared. This sharing prohibits certain concurrent operations. This common hardware is required during read, write, and ECC processing. The LCDC cannot perform more than one of these operations at a time.

5.20.2 LCDC LOGIC DESCRIPTION

The following paragraphs describe the two PCBAs that make up the LCDC controller.

5.20.2.1 LCDC Control Adaptor PCBA Logic Description

Sheet 1

LCDC Block Diagram

This sheet contains a block diagram that depicts the inter-relationship between the Control Adaptor PCBA and the Data Adaptor PCBA which comprise the LCDC.

Sheet 2

Control Adaptor Block Diagram

This sheet contains a block diagram of the Control Adaptor PCBA.

Sheet 3

System Universal Interface

The System Universal Interface connects the Control Adaptor PCBA with the XL Universal Bus (UBUS). This interface includes power distribution lines as well as data, address and control lines.

Disk "A" Cable Interface

This interface connects the Control Adaptor PCBA with the "A" cable of the disk drive's SMD interface. The "A" cable carries commands from the Control Adaptor PCBA to the drive and status information from the drive to the PCBA. No user data is carried on the "A" cable.

Adaptor PCBA Interconnect

This cable allows the Control Adaptor and Data Adaptor PCBAs to share the data, address and control signals necessary to allow the two PCBAs to function as one peripheral controller.

Sheet 4

Z80 Microprocessor

The Z80 supervises the transfer of data between the XL system memory and the disk drive. If ZMEREQ is True, the Z80 believes it is accessing its own memory. All 16 address lines are used for this type of access. If ZIOREQ is True, the Z80 believes it is accessing an I/O device on its own bus. The eight LS address lines are used to access I/O devices. To allow the use of both I/O and memory Z80 commands, the hardware and status registers can be accessed in either the I/O or memory address ranges. Because the Z80 is always in control of the LCDC's data and address buses, the bus request and bus acknowledge pins are not used.

Control Buffer

This buffer amplifies the Z80's memory control signals for use on both PCBAs of the LCDC.

Interval Timer

The interval timer is a programmable Z80 Counter/Timer Circuit (CTC) used to manage interrupts intended for the Z80. The CTC has four input channels ranked by priority, TR0-3 (TR0 highest priority). Each of these inputs are programmed to drive the INT output. When an interrupt is generated a vector unique to that channel is placed on the CTC's data lines.

DMA Run (DRUN) connected to TR0, is the highest priority interrupt. This signal indicates the Z80 is ready to transfer to or from the FIFO and the UBUS. TR0 is negative edge triggered with a down count of one.

The Index Detected (INDET) signal, which indicates the drive has detected the index mark on the disk, is connected to TR1. TR1 is negative edge triggered and has a count of one.

TR2, also negative edge triggered with a count of one, interrupts the Z80 if the Run Timer one-shot is not restarted before its period has expired.

TR3 is used as an interval timer to interrupt the Z80 if certain operations exceed their worst-case time limit. WR6007, connected to TR3, is used for diagnostic purposes only.

Data Multiplexers

The LCDC has an internal data bus used by the Z80, ZDB 0-7. This bus is divided into three segments. 0ZDB interfaces with the Z80 and the Interval Timer. This segment connects with the 2ZDB segment via bus transceivers 17D and 18D. 2ZDB interfaces with the majority of the logic on both PCBAs of the LCDC and with 4ZDB through bus transceivers 22D and 23D. 4ZDB interfaces the Z80 with the Program PROM and Control RAM. Bus transceivers 23F and 23H allow 2ZDB to interface with the 4Kx8 Data RAM through the memory Data Bus, MDB0-7.

The direction of data flow in bus transceivers 18D and 17D is controlled by NAND gate 13A. When 2ZRD is true the transceiver's inputs (INA-D) are disabled and the outputs (OUTA-D) are enabled. This allows data from 2ZDB to be driven onto 0ZDB. During write operations (2ZRD = false) the inputs are enabled to allow data from 0ZDB to be driven onto 2ZDB. If the Z80 is reading the Interval Timer, the transceiver outputs remain disabled.

When the Z80 reads the Program PROM or Control RAM (PTRE and ZRD = true), data is allowed to pass from 4ZDB to 2ZDB through transceivers 2D and 23D. Data flows from 2ZDB to 4ZDB during writes to the RAM (PTRE = true, ZRD = false). This data flow is controlled by the NAND gates in package 21D. Data flow between MDB and 2ZDB is handled by transceivers 23F and 23H in the same manner.

Address Buffer

Buffers 16D and 15C buffer the Z80's address lines (ZAB0-15) and are always enabled.

Sheet 5

Strobe Generator

The Strobe Generator decodes the addresses output by the Z80 and generates signals to enable individual devices or blocks of devices. The address decoding is done in several ranges.

The first range that is decoded is 0000-3FFF, the Program PROM. The two most significant bits must be zero. ZAB14 and ZAB15 are tested at pins 8 and 9 of AND gate 13B. If they both are false, then pin 10 of 13B will be high and decoder 14B will be enabled. The LCDC is equipped with either 1Kx4 or 2Kx4 PROMs, for either 8K or 16K of program memory as required. Multiplexer 14C, controlled by jumper W5, allows the address range of either memory size to be selected.

Without the jumper, input B of 14C is selected. AB13 is then applied to one of the enabling pins on 14B, limiting the range of the decoder to 0000-1FFF. AB lines 10, 11, and 12 are used for the select inputs of the decoder. Pin 11 of 13B is driven high to keep A10/CS true, permanently enabling the PROMs. Because one less address line is used to address the 1K PROMs than the 2K PROMs, the address range is halved.

When jumper W5 is installed to select the 2K PROMs, the A inputs of the multiplexer are selected, routing AB lines 11, 12, and 13 to decoder 14B and permanently enabling it. AB line 10 is tied to pin 12 of 13B, high or low as required. A10/CS becomes the MS bit of the address at the PROM.

The next range of address, 4000-4FFF, accesses the 4K of Control RAM. Addresses in this range cause pin 10 of 13B to be low (false) and pin 12 of 13A to be low (true) (ZAB15 = 0, ZAB14 = 1). The low/true signal from 13A enables decoder 14A at pin 1. In this range ZAB13 and ZAB12 will be zero, and a low/true signal will be generated at pin 4 of the decoder. This signal enables the other decoder in package 14A (pin 15). This decoder is used to decode ZAB11 and ZAB10 to generate the select signals for 1K segments of the Control RAM.

Addresses 5000-5FFF are decoded at pin 5 of 14A. This range of addresses represents the 4K Data RAM. Addresses for this RAM are further developed in the RAM Address Generator on Sheet 11.

Addresses from 6000 to 6FFF are decoded at pin 6 of 14A. This range is limited by the discrete component decoder made up of AND gates 13C, 13B, and 12C. This decoder has two segments, one for decoding in the Z80's memory address range and one for decoding in the Z80's I/O address range. The memory decoder limits the range to 6000 to 603F, and the I/O decoder limits the range to 00 to 3F. Both of these ranges include the control and status registers. When the Z80 is making a memory access, pin 8 of 12C becomes low/true (ZMREQ = true). When the Z80 is accessing its

I/O registers, pin 6 of 12C becomes low/true (ZIOREQ = true). When either term is true, decoder 11A is enabled. This allows both I/O and memory related Z80 commands to access the status and control registers. Since the Z80 only uses the eight LS bits of its address bus (ZAB00-07) to access I/O devices, the only terms to determine the address range 00 to 3F are ZAB07 and ZAB06 at pins 2 and 3 of 13B.

Decoder 11A uses lines ZAB03-05 to further decode the address. The decoder divides the addresses into groups of eight. Pin 15 enables the devices which decode addresses 00 to 07, and pin 14 enables the devices which decode addresses 08 to 0F, etc.

Decoders 8D/9D and 10D/11D are enabled by accesses from 00 to 07 and 08 to 0F respectively. One of each pair decodes write terms (ZWR = true), and the other decodes read terms (ZRD = true). All four decoders decode address lines ZAB00-02, completing the decoding process and developing the individual strobes.

Sheet 6

Power Sequence Control

The Power Sequence Control logic allows the LCDC to power up and power down the disk drives remotely. To turn on a drive, the Z80 sets flip-flop 11K by writing to address 6005 with a one in bit seven of the associated data word. Setting 11K causes pin 11 of NAND gate 11L to become high. In turn, transistors Q5 and Q6 will pull Power Sequence Pick (PSP) and Power Sequence Hold (PSH) low. These two signals are applied to the drive. Both signals are required to power on a drive. To prevent the heavy current draw that would occur if four drives all powered up at once, PSP is daisy chained between drives and not passed to the next drive until the current drive has achieved ready status.

The drive powers off when PSH becomes high (false). The Z80 shuts down a drive by writing a zero in bit seven to address 6005. This resets the flip-flop and causes pin 11 of gate 11L to go low and both signals (PSP and PSH) to go high.

The Z80 may read the status of the flip-flop by reading address 6005, data bit seven.

Disk Receivers

These receivers are 8 line receivers contained in four packages 13K, 14H, 14K, and 14L. Each receiver monitors one bus line comprised of a pair of twisted wires. This dual wire arrangement allows the bus to be installed in a noisy environment. This is because the line receivers compare the difference in potential (differential) between the wires instead of measuring the potential independently. Because the two wires are close together, any noise will affect both equally and the difference between the voltages on the two of them will remain the same.

The line receivers receive status information from the selected drive. When the A input is high and the B input is low the output (Y) of the device will go high and vice versa. Both receivers in package 13K have high/true attached to the B inputs and low/true attached to the A inputs making the output low/true instead of high/true. It is important to note that all inputs to the receivers are not at TTL levels. In fact, all voltages on each pair of lines will be zero or negative with respect to ground. To obtain a high signal the line driver must pull the B input low until a differential of -25mV with respect to the other input (ground) is achieved. To achieve a low signal the line pulls the A input low. The line driver will only pull one line low at a time. All eight receivers are enabled whenever any drive is selected (DRSLD = true).

Status Buffer

This buffer is used for the drive status data presented by the Disk Receivers onto the Z80 data bus. The buffer flip-flops and their outputs are enabled by a Z80 read of address 6002.

Control Register

This register stores commands for the selected disk drive. These commands are stored in two eight-bit latches, 15F and 21K, then transmitted to the drive on the A cable bus. The bus has ten lines and can carry three different kinds of data: the 10-bit binary cylinder address, 5-bit binary head select, and one of ten control commands (one per line). The nature of the data on the bus is specified by three tags: Set Cylinder (SCYL), Set Head (SHD), or Set Control (SCT).

To allow command or selection data to stabilize on the bus before the tag is turned on, counter 19D does not enable tag decoder 18F for at least one ZCLK after latch 15F has been loaded. The decoder remains enabled for four ZCLKs before the counter is disabled.

The Z80 is prohibited from sending commands to the drive that control data transfers to and from the disk. This is done by disabling the drivers of bus lines 0, 1, and 5 (write gate, read gate, and address mark enable) when the Z80 is generating the Set Control tag and the Data PCBA is not controlling the operation (SECCMD = false). This condition is detected at AND gate 11H, pins 9-11.

Data Multiplexer

The Data Multiplexer allows the data control logic on the Data PCBA to set Read Enable (RDEN), Write Enable (WREN), and Address Mark Enable (AMEN) commands to the drive. When the signal Set Sector Command (SECCMD) is true, the B inputs of multiplexer 20K are selected allowing the signals to drive the appropriate bus lines. The Set Control tag is driven true at the same time.

Disk Transmitters

The Disk Transmitters are 16 line drivers contained in eight packages. Each driver is designed to drive a twisted pair of wires that comprise each bus line. The wire pairs function is described under the section on the Disk Receivers.

When all three inputs to a driver channel are high, the line driver will pull the Z output low until a differential of at least -25mV with respect to the Y output is achieved. If any of the three inputs is low the line driver will pull the Y output low. All bus lines are terminated with 56 ohm resistors.

Fourteen of the bus lines are set for high/true inputs. If their inputs are true the Z output will be pulled low. The Set Cylinder and Set Head tag lines are low/true. The drivers for these lines are in package 18H. A negative (low) true input to these drivers causes the Y output to be pulled low.

The Device Select lines (DEVS0 and DEVS1) are not paired. The Z outputs of their drivers (15H and 17K) are pulled low with a high/true input. Because these lines are not paired, their immunity to noise is reduced.

Sheet 7

Slave Control

The Slave Control logic manages the LCDC's response to accesses from the XL system UBUS. Addresses in the LCDC's range are detected by the decoder formed by gates 5F, 3K, and 2L. Since

an XL system can accommodate two LCDCs, the address range is selectable. This selection is accomplished by exclusive OR gate 1L. If Controller Address Select (CAS) is true, the controller's address range is FF10-FF17. If CAS is false, the range is FF18 to FF1F. Only a controller in the range FF10-FF17 will respond to bootstrap load commands.

When an address in the LCDC's range is detected, pin 9 of 2L will go low and flip-flop 2F will set causing pin 7 to become high. This removes the preset from pin 4 of flip-flop 1F. This flip-flop is part of the Memory Grant Logic which regulates the Z80's and UBUS' access of the 16x8 Interface Register RAM. If the Z80 is not already accessing the RAM (GTZ = false) flip-flop 1F is allowed to set, pulling pin 5 low and generating the Grant UBUS (GTU) signal. When pin 5 goes low flip-flop 2F in the Slave Control logic will set its pin 9 high on the next BCLK. If the UBUS drivers of the LCDC are enabled (OUTE = true), a MACK will be generated at pin 3 of gate 11L.

The GTU signal enables decoder 1D. This decoder decodes write strobes such as the one generated at pin 15. This strobe clocks Out Enable flip-flop 11F. Boot Strap flip-flop 11F is clocked by a strobe generated by decoder 1D.

When the UBUS is reading the LCDC, Slave Read is generated at pin 12 of gate 10H.

Memory Grant

This logic controls the access of the Interface Register (16x8) by the Z80 and the UBUS. For the Z80 to access the register (ZUBRF = true), flip-flop 1F sets and generates GTZ, unless the UBUS has already initiated an access. For the UBUS to access the register, flip-flop 1F sets and generates GTU, unless the Z80 has been granted priority. It is unlikely for both flip-flops to set simultaneously because the 16MHz CLK16 and 5MHz BCLK are not synchronized.

ADX3 Control

Flip-flop 8E stores the nineteenth address bit used during accesses of extended memory. The Z80 loads the flip-flop by writing to address 600D and reads the flip-flop's status at address 6005. The address bit is available to the UBUS when MASTER is true.

UBUS Status

The Out Enable flip-flop controls the LCDC's UBUS drivers. It is controlled by XL software writing to address FF10. A one in the LS bit of the data word sets the flip-flop and zero resets it. The flip-flop can also be set by the Z80 (FOUTE = true), however this is a development system feature.

A system write to FF12 with a one in the LS bit of the data word sets the Boot Strap flip-flop indicating that a boot strap load is required.

Address Transceivers

These four data transceivers interface the LCDC with the address portion of the UBUS. Receive is permanently enabled, transmit is enabled when the LCDC is bus master.

Sheet 8

Master Control

This logic consists of three flip-flops that request and receive UBUS master grants. The LCDC will request bus mastership any time it has data to transfer to system memory. This is done by the DMA

Request (DREQ) signal. If the LCDC is enabled (OUTE = true), and not already master, DREQ causes pin 9 of flip-flop 9K to go high resulting in Bus Request (BRQ2) to be generated at pin 6 of gate 11L.

When Grant In (GIN) is received, Master flip-flop 9K sets pin 6 low and pin 7 high. If Bus Hold (BHLD) or MCYC is true, GIN will be blocked at gate 10K. When Master flip-flop sets, line driver 9H is enabled. This allows the inverted MACK signal from the UBUS to be driven back onto the UBUS as Memory Cycle (MCYC) with Memory Write and the Address Extension bits.

The high signal at pin 7 of the Master flip-flop also causes flip-flop 11K to set pin 6 low on the BCLK after Master goes true. This blocks another DREQ from setting 9K before the end of the current memory cycle. Flip-flop 9K toggles off on the same BCLK. With 9K reset and MACK false, the inputs (pins 2 and 3) of the Master flip-flop will be in the no-change state.

When the bus slave activates MACK, MCYC will become false. The no-change is removed from the inputs of Master and it will reset on the next BCLK. With Master off, flip-flop 11K will reset and the Master Control logic will be re-enabled.

UBUS Control

The UBUS Control logic consists of several line drivers/receivers used to buffer control signals to and from the UBUS. The drivers in package 9H are enabled when the LCDC is bus master and the drivers in package 9L are permanently enabled.

UBUS Status

This logic allows the Z80 to sample the condition of several UBUS control latches. This is done by a Z80 read of address 600D, enabling line drivers 9H. One of the status bits is provided by counter 4D. This counter counts bus clocks when the LCDC is bus master. If the counter reaches six, it declares a UBUS Time-Out (UBTO). The two NAND gates in 9E form a latch that stores the true UBTO signal until Error Reset is pulsed true.

Data Transceiver

These four transceivers interface the LCDC to the data segment of the UBUS. Their transmit function is enabled when the LCDC is bus slave and a read is performed (SLRD = true). High speed transfers of data from the disk are handled by a set of data transceivers on the Disk Data Adapter PCBA. When the LCDC is bus slave (receive function) the 16 lines of the transceivers are divided into halves, an upper and lower byte. This allows a 16 bit data word to be multiplexed into an eight bit register.

Sheet 9

UBUS Address Generator

The UBUS Address Generator logic consists of five programmable four-bit counters cascaded to allow the address to be easily incremented. The address generator is primarily for high speed transfer of data from memory to disk and disk to memory. The process is started by a three part process of loading the address into the counters. The LS byte of the address is loaded by a Z80 write to address 600B. The MS byte is loaded by a Z80 write to 600C. Two address extension bits and two control terms are loaded into address 600D. ZCLK clocks the counters while they are being loaded. To prevent ZCLK from incrementing the counters at other times, the clock is ANDed with the write strobe.

After the address is loaded, it can be incremented by MASTER, SKCLK, or WR6008, which are ORed at gate 10H.

The MASTER signal is used to increment the address when the LCDC is transferring data to or from the disk. The Skip Clock (SKCLK) signal increments the address when data from the FIFO is being skipped. WR6008 is used only for diagnostic purposes.

UBUS Word Counter

The UBUS Word Counter is similar to the UBUS Address Generator, and incremented by the same signals. Its purpose is to count the words that have been transferred. In preparation for a DMA, the Z80 loads the counters with the two's complement of the number of words to be transferred. An X'8' is loaded into the MS nibble (counter 7C) to ensure the MS bit of the counter is one for the duration of the count. The MS bit is DMA Run (DRUN) which enables the DMA control logic on the Data Adaptor PCBA. The counter overflows after the correct number of words has been transferred and DRUN goes false.

UBUS Status

When a UBUS or data error is detected this flip-flop is set and clears the UBUS Word Counter ending any DMA in progress. The flip-flop is cleared by a Z80 write to address 600D with a one in the MS bit of the word, or by a Reset (RS).

Sheet 10

Interface Register

This register is a 16x8 RAM used as a mailbox for communications between the XL and LCDC. Because the data buses of the XL and the LCDC's Z80 are of different widths, some fairly extensive logic is necessary to make the RAM accessible by both processors. Because of this difference, the XL accesses the RAM as eight 16-bit registers, and the Z80 accesses it as 16 eight-bit registers. Access to the register is governed by the Memory Grant Logic (sheet 7).

When the XL is granted access to the register, both input and output must be multiplexed. This multiplexing is done by the logic associated with flip-flop 5E. Prior to system access to the RAM, the low/false GTU signal clears flip-flop 5E. This sets the flip-flop (pin 6 = high) for the MS byte of the 16-bit XL data word (ENUDH = low). 5E is clocked by ACLK, which is 180 degrees out of phase with BCLK. Since BCLK synchronizes system memory cycles, the flip-flop sets half way through a memory cycle. When pin 5 goes high the LS byte of the system data word is accommodated. This also activates the LS RAM address bit through selector 7D. The remainder of the address is supplied by the three LS bits of the UBUS address, UAB13-15.

The logic for addressing the register is the same for either a system read or write, however, the data paths are different. When the Slave Control logic (sheet 7) detects a write to address FF11 or FF12 (the mailbox and attention registers in the RAM) signal FF11W or FF12W become true, causing (when GTU is also true) the RAM write strobe to be generated by the logic in package 4F. The 1ACLK clock that generates the write strobe is inverted with respect to 2ACLK, which clocks flip-flop 5E. This allows the upper byte of data to be strobed into the RAM before the flip-flop sets. The strobe is not generated again until the lower byte has had time to stabilize at the RAM inputs (50 nsecs.)

ENUDH and ENUDL, generated during UBUS writes enable the receive functions for the UBUS data transceivers for the MS byte and the LS byte respectively.

When the system is reading the RAM, SLRD will be true, enabling octal latch 8K and octal buffer 5K. When 5E sets and increments the address, the enable term is removed from 8K and freezes the MS byte at its outputs. The LS byte then appears at the outputs of buffer 5K. The LCDC then generates MACK, indicating the data is valid.

When the system reads the operations status register, FF13, the data in bit positions 00 and 01 (the two MS bits of the MS byte) does not come from the RAM, but from the two flip-flops in package 6E. Pin eight of 6E is the mailbox busy flag and pin six is the interrupt system flag. An address of FF13 is decoded by NAND gate 7F. A low/true at pin six turns off the buffer from the RAM and turns on the buffer from 6E. The flip-flops are set or cleared by an LCDC Z80 write to 6006. Z80 Data Bus line seven controls the mailbox busy flag; line six controls the interrupt system flag.

The LCDC Z80 accesses the RAM in 16 eight-bit words in the address range 6030 to 603F. The Z80 may access the RAM when GTZ is true. GTZ causes multiplexer 7D to select the four LS bits of ZAB. For a write operation, GTZ enables octal buffer 8H to allow the Z80 to interface with the RAM. The write strobe is generated by ANDing GTZ and ZWR and is produced by the Z80 as part of its write cycle. Read operations are accompanied by signal ZRD, which is used to enable to RAM output buffers in package 5H. The mailbox busy and interrupt system flags are read at address 6036.

Sheet 11

RAM Address Generator

The LCDC contains a high speed 4Kx8 static RAM used for intermediate data storage. This RAM can be accessed directly by the Z80. It can also be accessed by the data transfer logic on the Data Adapter PCBA. For this type of access an address must be generated. This address generating logic is very similar to the UBUS Address Generator on sheet 9. It consists of three programmable binary counters. In preparation for the transfer of a block of data from disk to RAM, the Z80 loads the starting address for the RAM into the generator. The eight LS bits are loaded into counters 22E and 23E at address 6009. The two MS bits and the page number are stored into counter 17E at address 600A. A combination of ZCLK and the write signal strobe the data into the counters.

After the generator is initialized, the transfer logic requests access to the RAM from the Memory Grant logic. When the grant is received (GTMF = true) data is transferred from the FIFO buffer to the RAM. After each word is transferred, the address generator is incremented (RAMCK). Data transfer is halted if the address generator overflows, or RAMD goes false.

Memory Grant

This logic controls access of the 4Kx8 RAM by the Z80 and the transfer logic. The Z80 requests access by activating the RAMZ signal. If the transfer logic is not already accessing the RAM, flip-flop 3E sets with pin eight high and nine low (GTMZ = true). RAMZ must remain true until the Z80 is completed with the transfer.

The transfer logic requests access to the RAM by activating signal RAMD. If the Z80 is not already accessing the RAM, flip-flop 3E sets with pin six high and pin five low (GTMF = true). If an address overflow occurs, a new access by the transfer logic is blocked by the low/true signal from gate 3D, pin 12.

Address Overflow Control

The Address Overflow Control monitors the RAM Address Generator for an overflow condition. This is indicated by the carry enable signal generated by counter 17E. This low/true signal is applied to pin 13 of 17F causing pin 9 to go high. The overflow control may be disabled by a Z80 write to address 6005 with a zero on data line four (ZDB4). The status of the flip-flops can be read at address 6005.

Address Multiplexer

This multiplexer selects between the Z80 Address Bus and the RAM Address Generator. The Z80 Address Bus is selected when the Z80 has been granted access to the RAM (GTMZ = true).

This logic multiplexes the write strobe and incorporates a two to four line decoder (18F) that decodes the RAM page number at 1K boundaries from the two MS bits of the RAM address. The multiplexer is enabled when either the Z80 or transfer logic has been granted access to the RAM.

Sheet 12

Diagnostic Switches

These switches allow a technician to select optional firmware routines for the LCDC diagnostic selftest. The switches are located in switch pack 2A on the Control Adaptor PCBA. The LCDC reads the condition of the switches at address 6001. An open switch causes a high line level; a closed one a low line level. The processor complements the data received from reading the pack. The read signal enables the outputs and freezes the flip-flops of octal latch 3A.

Address and Capacity Switches

The switches located in dip pack 1A are used to select the address range of the controller and to limit the storage capacity of the disk drive. Switch 1 specifies the LCDC's UBUS address range. Switches 2 and 3 set the capacity. See Table 5.20-1 for the switch settings.

Table 5.20-1. LCDC Control Adapter PCBA Switch Settings

Switch Pack 1A				
Switch No.				
1	2	3	4	Status Selected
OFF				Select LCDC No. 1 Address OFF10-OFF17
ON				Select LCDC No. 2 Address OFF18-OFF1F
	ON	ON		25% of LCD Available for Use (11 MB)
	ON	OFF		50% of LCD Available for Use (26 MB)
	OFF	ON		75% of LCD Available for Use (41 MB)
	OFF	OFF		100% of LCD Available for Use (56 MB)
			NOT USED	S4 Normal Position is OFF

When switch four is on, the LCDC sets the limits to the full capacity of the highest LCD installed. If switch four is off, the position of switches two through four can be read in the Operations Status Register and may be used by the system software to limit the capacity of the disk system. The Address and Capacity Register may be read at address 6004. The latch is also used to display the contents of the Header Lock Status Register.

Diagnostic LEDs

These LEDs display error codes. The error codes are latched in two four-bit programmable counters. The count function is permanently disabled. The counters are both loaded and read at address 6000.

Header Lock Status

This register is used to store header lock data. The data is stored by writing to address 6004. The register is read through the Address and Capacity Switch Register also at address 6004.

Crystal Clock

The clock is a 16 MHz crystal oscillator (2B). This 16 MHz signal is used to generate two clocks used by the LCDC. The gates in package 3B amplify the signal for use in several places on the LCDC. The 16 MHz signal is divided by counter 4D to supply the 4 MHz clock needed by the Z80.

System LEDs

These LEDs,displays condition information. The data is not latched. The LEDs indicate if the LCDC is bus master, interrupting the system, selecting a drive, or busy.

Run Timer

The Run Timer (4C) is a one-shot started by the Z80 after self test. It is then continually restarted to indicate that the firmware is running as designed. If the Z80 does not restart the one-shot within its 450 msecs period, the RUN signal will go false and the busy LED will go out.

Master Protect and Reset

This logic generates the reset signals used to initialize the LCDC. If MPRT becomes low/true, Q4 generates 3MPRT to reset the logic associated with the UBUS and start one-shot 4C. The one-shot generates a 2.5 usecs pulse amplified by Q3 and Q4. The one-shot is required to provide the minimum pulse width (750 nsecs) needed to reset the Z80. System software can also initiate a reset by writing to address FF10.

Sheets 13 and 14

Program PROM

This firmware contains the program that controls the LCDC Z80. This eight bit wide memory has eight pages, which may be 1K or 2K depending on the PROMs used. The address range for the 8K memory (1K PROMs) is 0000 to 1FFF. For 16K memory (2K PROMs) the address range is 0000 to 3FFF. Addressing of the Program PROMs is on Sheet 5.

Sheet 15

Control RAM

This RAM is used by the Z80 as a scratch pad. The RAM is eight bits wide with an address range of 4000 to 4FFF. The 4K of memory is divided into 1K pages. Up to 2K of this area may use PROMS to allow 10K of Program PROM using 1K PROMS. A jumper is used if the entire area is used as RAM, and removed to allow the use of PROMs. The logic in package 23B either generates a write strobe for RAMs or an enabling signal for the PROMs.

Sheet 16

Data RAM

The Data RAM is a 4Kx8 memory divided into 1K pages. It can be accessed by either the disk drive or the Z80 and is used primarily as temporary storage for data being transferred to or from the disk drive. These RAMs are static and thus need no refresh.

5.20.2.2 LCDC Data Adaptor PCBA Logic Description

Sheet 1

This sheet contains a block diagram of the Data Adaptor PCBA.

Sheet 2

System Universal Interface

The System Universal Interface connects the Data Adaptor PCBA with the XL Universal Bus (UBUS). This interface includes data lines, but not address lines. The addresses for the data generated on this PCBA are provided by the Control Adaptor PCBA. This interface also supplies power to the Data Adaptor PCBA.

Disk "B" Cable

This interface connects the "B" cable of the disk drive's SMD interface with the Data Adaptor PCBA. Each of the two "B" cable interfaces (the other is on sheet 3) can serve two drives. The "B" cable carries data, data clocks, and limited status information to and from the drives.

Sheet 3

Disk "B" Cable

This interface is the same as the disk "B" cable on sheet 2. The two "B" cable interfaces allow the LCDC to control up to four drives.

Adapter Interconnect

This interface connects the Control Adapter PCBA and the Data Adapter PCBA to allow the two to function as a single peripheral controller.

Sheet 4

Strobe Decode

This logic decodes the addresses generated by the Control Adaptor PCBA into individual strobes for the registers or devices on the Data Adaptor PCBA. It is essentially an extension of the decode logic on the Control Adaptor PCBA, sheet 5 and is enabled by Register Decode (REGDC). REGDC is true for addresses in the range 6018 to 602F. The two-to-four-line decoder 17H breaks that range into three smaller ranges: 6018-601F, 6020-6027, and 6028-602F. When an address in the first range is detected, 17H, pin 9, will go low and if ZWR is true Command Load (CMDLD) is generated. An address in the second range will cause pin 12 to go low enabling decoders 12E and 11E. Decoder 12E is enabled if ZRD is true to decode read strobes. 11E is enabled if ZWR is true to decode write strobes. An address in the last range causes pin 11 to go low and enable decoders 9E (read) and 10E (write).

Sheet 5

Data Latch and Buffer

The Data Latch and Buffer acts as a switch board for data transfered between the LCDC and the disk drive.

Octal buffers 4H and 7H multiplex the 16-bit data words from the FIFO onto the eight-bit Data RAM bus under control of flip-flop 12H. When Grant Memory FIFO (GTMF) goes true the LS byte of the data word is driven onto the Data RAM bus. When the LS byte is clocked into the RAM, flip-flop 12H sets and the MS byte of the word is driven onto the RAM bus. GTMF then goes low to clear 12H to restart the cycle.

To transfer data from the disk to the RAM the 16-bit data word is clocked into octal latches 2H and 3H. When Drive to RAM OP (DTROP) goes true, GTMF causes the outputs of latch 2H to drive the LS byte onto the RAM bus. When the data has been clocked into the RAM, the flip-flop sets and the MS byte is driven onto the bus.

Data from the RAM is sent to the FIFO through buffers 4L and 4K. A single byte from the Data RAM is driven onto both the upper and lower halves of the bus feeding the FIFO input register. One byte is latched into the register, the RAM is incremented, and the second byte is latched into the other half of the FIFO input register.

Data Transceiver

These bus transceivers transfer data directly between the FIFO and system memory under the control of the DMA controller (Sheet 7). UBUS addresses are generated by the Address Generator (Control Adaptor PCBA, Sheet 9).

Sheet 6

First-In-First-Out Memory (FIFO)

The FIFO buffers data transfers between the disk and the UBUS or Data RAM, and transfers between the Data RAM and UBUS. This buffer is composed of four 4x64 word chips: 1K, 1L, 8K, and 8L. These components are arranged in parallel to create a 16- bit by 64 word serial memory.

To load data into the FIFO a data mux (3K, 3L, 7K, and 7L) selects between the UBUS and Data RAM (UDB) or the drive (RDB) and latches one 16-bit word of data at a time. When the FIFO is full, IR will go low and when a word is transferred out of the FIFO IR will go high to indicate the buffer is ready to accept more data.

When a word has gone through the FIFO and is at the internal output buffer, Output Ready (pin 14) becomes high/true. The OR terms generated by the individual portions of the FIFO are ANDed at gate 9L to generate the FIFO Output Ready (FOR) signal. The data is then clocked into the Output Latch (1H and 8H) and the FIFO Output Latch Flag (FOLF) is generated to indicate valid data present in the latch. When the data has been transferred the appropriate FIFO Output Latch Flag Clock (DFOLFC, RFOLFC, or UFOLFC) is generated to reset flip-flop 11L and allow the cycle to begin again.

Sheet 7

UBUS DMA Control

This logic sequences data transfers between the FIFO and the UBUS by producing the FIFO Input and Output Flags Clocks (UFILFC and UFOLFC) and a DMA request signal. The logic also produces Skip Clock to allow FIFO data to be ignored if necessary.

To initiate transfer of data from the UBUS to the FIFO, terms WRCYL, FILF, CSEN, and DRUN are ANDed at gate 23H causing the NOR gate at 18K produce signal DREQ. The LCDC then requests bus UBUS mastership. When bus mastership is granted and the data is valid, the signals MASTER and MACK will be true. This condition causes UFILFC to be generated by AND gate 22H and NAND gate 23K. UFILFC causes the data from the UBUS to be latched into the FIFO's input register to begin the FIFO input sequence.

To transfer data from the FIFO to system CSEN, DRUN, FOLF, and WRCYL are ANDed at gate 23H to generate DREQ. When the LCDC is granted bus mastership the word in the FIFO Output Latch is written into system memory. UFOLFC is also generated at pin 11 of 23K to reset and store the word in the FIFO output in the Output Latch.

The UBUS DMA logic can also skip or ignore the data in the FIFO. To skip the data the standard FIFO to UBUS transfer is initiated with Skip Control (SKPC) high. This prevents DREQ from being generated and activates the flip-flops in 19L. These divide the ACLK by four to produce Skip Clock (SKCLK) which takes the place of MASTER in the generation of UFOLFC and incrementing the UBUS Address Generator (Control Adaptor PCBA, sheet 9).

Drive DMA Control

The Drive DMA Control logic controls transfer of data to the drive from the FIFO and from the drive to either the FIFO or directly to the LCDC Data RAM. All drive data transfers are synchronized by Shift Register Clock (SRC) and Word Time (WDTM). SRC synchronizes each data bit from the drive. WDTM is true every 16 bits (one word). The counter that generates WDTM is reset when an index mark is detected.

For transfers from the FIFO to the disk the Mode Path Register (sheet 9) is loaded with the appropriate information. The path is drive to FIFO (PDF) and the object is write data onto disk (DWEN). A Start Sector Data (STSD, write) is loaded into the Disk Data Control Sequencer (sheet 10). Data will be available in the FIFO output latch (FOLP = true). A target is also loaded into the Target Register.

When the Disk Data Sequencer is incremented by the detection of the target (TLE, sheet 10 = true), DMAEN will be activated causing the Drive/FIFO Output Latch Flag Clock to be generated at pin 8 of NAND gate 11K synchronous with WDTM and SRC. This causes the word in the FIFO Output Latch to be loaded into the Transmit Shift Register (sheet 12) and reset FOLF to load a new word into the FIFO Output Latch. This operation is synchronized with WRCK; therefore, the new word is loaded into the Transmit Shift Register as the last bit of the previous word is shifted out.

While data is moved out of the FIFO, the Z80 loads a new target into the Target Register and a Stop Last Data (SPLD, write) command into the Disk Data Control Sequencer. When the target is reached, the Sequencer will terminate the write (DMAEN = false). If the Sequencer attempts to transfer data from the FIFO and the FIFO Output Latch is empty (FOLF = false), the Drive/FIFO Output Latch Error Clock (DFOLEC) is generated at pin 6 of gate 12K to set the FIFO Output Latch Error Flag.

Word Clock (WDCK) is generated at pin 8 of gate 6C, synchronized by 4SRC to give WDTM greater resolution.

A drive to RAM transfer is implemented by both the Drive and RAM DMA Control logic. The transfer is initiated by the Z80 setting the RAM Write Enable (RWEN) and Path Drive/RAM (PDR) bits in the Mode/Path Register, then loading a STSD read command into the Disk Data Control Sequencer. When the sync mark is detected, DMAEN becomes true, presetting flip-flop 12H via gate 12K pin 11. This allows DRILFC to be generated when WDTM and 4SRC are true. This occurs after one 16-bit word has been clocked into the Receive Shift Register.

DRILFC, generated at pin 12 of gate 11K, clocks the data word in the Receive Shift Register into the Data Latch (sheet 5) and sets RILF. RILF is one of the qualifying terms for the RAM DATA control logic.

Data transferred from the drive to the UBUS passes through the FIFO. The enabling terms are PDF and a false DWEN. When these terms are met DMAEN goes true presetting 12H. DRILFC is then generated at pin 6 of gate 11K, after a word of data has been shifted into the Receive Shift Register.

Both DRILFC and DFILFC are generated, synchronous with WDTM, as long as DMAEN remains true. When DMAEN goes false, flip-flop 12H is asynchronously cleared by gate 12F, pin 8.

To load the Error Correction Code (ECC) data that follows the data segment on the disk into the FIFO or RAM, the Z80 sets bit zero of the Diagnostic Control Register (Z80 address 602A) high. This signal and Error Correction Code Accumulate (ECCUM) prevent 12H from being cleared when DMAEN goes false. This allows DRILFC or DFILFC to continue to clock the ECC data into the RAM or FIFO. When ECCUM becomes false, 12H will clear.

In the loop-back mode (data is transferred directly from the Transmit Shift Register to the Receive Shift Register) several adjustments to the latch clock timing are made. The FIFO is loaded with the data to be looped back into the RAM. Because data is going out of the FIFO and back into the RAM simultaneously, PDF, PDR, and PLB are all set to true in the Mode/Path Register. The Disk Data Control Sequencer is actuated by a STSD write.

After the Disk Data Control Sequencer generates SYNCWR as required by the disk protocol, the sync mark is generated, and while it is shifted through the transmit shift register, DMAEN is generated. WDTM is generated as the last bit of the sync is shifted out of the Transmit Register, causing DFOLFC to be generated. DFOLFC then parallel loads the first word of the test data into the Transmit Shift Register.

After the sync mark bits have been looped back into the Receive Shift Register, the loop back data path causes them to be loaded into RAM. Because of the propagation delays in the multiplexers, the Receive Shift Register is one clock (bit time) behind the Transmit Shift Register. To account for this, flip-flop 16F delays WDTM by one SRC clock before DRILFC is generated. In the loop-back mode (PLB = true), data selector 11F selects the delayed WDTM for setting of flip-flop 12H and generating DRILFC.

Flip-flop 12H normally sets asynchronously when DMAEN becomes true. In the loop-back mode the bit settings in the Diagnostic Control prevent this by applying a low signal to pin 12 of gate 12K. With PLB true 12H will not reset asynchronously when DMAEN becomes false.

WDTM clocks the data word into the RAM Input Latch, delayed one bit time to compensate for the propagation delay.

To terminate the loop-back operation, the Z80 loads a Stop Last Data command (SPLD, write) into the Disk Data Sequencer and when the target comparator detects the end target DMAEN becomes false. The low DMAEN provides the input at 12H's D pin. When WDTM is true the word in the Receive Shift register is clocked into the RAM input latch. Flip-flop 12H then resets as WDTM becomes false.

To load the ECC data following the loop-back data into RAM the processor sets the third bit of the Diagnostic Control register to true. This, combined with ECCUM, keeps the D input of 12H high until ECCUM goes false to allow the ECC data to be loaded into the RAM.

RAM DMA Control

The RAM DMA Control logic regulates the flow of data to and from the Data RAM. This may be to or from the FIFO, or directly from the drive. Transfers directly from the drive are controlled in conjunction with the Drive DMA Control logic. The control signals for the RAM are sequenced by an eight-bit parallel-out serial shift register (18L).

The data path for the transfer is selected by the three AND gates in package 19E. Pin 6 selects a RAM to FIFO Operation (RTFOP); pin 8 selects a FIFO to RAM Operation (FTROP); pin 12 selects a Drive to RAM Operation (RTROP). When the conditions for any of these signals are met, RAM Demand (RAMD) is generated at pin 8 of NOR gate 18K. This signal requests access to the Data RAM from the Grant Logic on the Control Adaptor PCBA. When this access is granted, Grant Memory FIFO (GTMF) becomes true. The generation of GTMF begins the operation of the sequencer. Because the A and B outputs are looped back into its serial input the sequencer produces a staggered output.

Output C of the sequencer causes RAMACK to be generated, which causes FIFO Input Latch Hold, MS Byte (FILMH) to be generated. This high/true signal disables the serial input to the sequencer limiting the number of pulses per output to two.

If the transfer is from RAM to FIFO, the first RAMCK generated by the sequencer increments the Data RAM to set up the first word. FIFO Input Latch Clock, MS Byte (FILMC) then clocks the data into the MS byte of the FIFO Input Latch. The RAM address is then incremented and FIFO Input Latch Clock, LS Byte (FILLC) clocks the LS byte into the FIFO Input Latch. FILF then becomes low/true and RAMD goes false. GTMF will then go false to allow the cycle to start again.

To transfer data from the FIFO to the RAM (FTROP = true), the MS byte of the data word from the FIFO will be available to the RAM through the Data Buffer (sheet 5) when GTMF becomes true. When RAMCK occurs, the RAM address will be incremented. This clock will also disable the MS byte buffers and enable the LS byte buffers in the Data Buffers. A second RAMCK increments the address for the subsequent transfer of the LS byte. This clock is synchronous with RFOLF, which resets the FIFO Output Latch Flag, and RAMD becomes false. GTMF then goes false and clear the sequencer.

To transfer data directly from the drive to the RAM, RAM Input Latch Flag (RILF) will become true when the data word from the drive is available. This causes RAMD to go true, and when access to the RAM is granted (GTMF = true), the MS byte of the word is stored in the RAM. The sequencer then generates RAMCK to increment the RAM and enable the LS byte of the RAM Input Latch. The LS byte is then stored in RAM. A final RAMCK increments the RAM address for the next transfer and RAM Input Latch Flag Clock (RILFC) resets the Ram Input Latch Flag and RAMD goes false. GTMF will then become false and clear the sequencer.

Sheet 8

Status Read

The Status Read registers allow the Z80 to monitor the progress of various sequencers that are not under its direct control. There are eight individual Status Read registers consisting of four groups of two data selectors. The eight three-state outputs of each group interface directly with the 6ZDB bus. The outputs are enabled and data selected by the address decoders on sheet four.

Option Switches

The eight Option Switches allow the options provided by the LCDC firmware to be manually selected. During initialization, the Z80 reads the register and executes the microprogram accordingly.

Data Transceivers

These two quad data transceivers interface the Z80 data bus on the Control Adaptor PCBA with the data bus on the Data Adaptor PCBA.

The direction of data flow through the transceivers is controlled by the Z80's read term, ZRD. When it is high/true, the receivers are disabled and data is driven from the IN pins onto the Control Adaptor PCBA' 2ZDB bus. During writes, ZRD is low/false, disabling the transceivers' drivers (via inverter 22K), causing the data to be passed from the 2ZDB bus to the Data Adaptor PCBA's 6ZDB bus.

Sheet 9

Target Register

This register stores the target value generated by the Z80 for use during write operations. The target value is the data word associated with any of the Disk Data Control Sequencer commands (CMDLC = true).

Target Comparator

The Target Comparator compares the value in the Target Register with the product of the Disk Bit Reference Counter's (DBRC) chunk counter. This comparator consists of two cascaded, four-bit, magnitude comparators (1B and 1C). The output of this logic is used as an event marker by the Disk Data Control Sequencer (DDCS).

During normal read and write operations, the comparators are continuously enabled (FIND = true). When the chunk count equals the target, pin six of 1C becomes high, generating Target Slice (TS). To prevent the Target Leading Edge (TLE) signal from being generated prematurely, flip-flop 5C does not set and allow TS to propagate through gate 6C until the DDCS enables its own clock selector (SCE = true). The flip-flop is reset by Data Command (DATCMD) at the end of the DDCS sequence. During initialization Header Slice Time (HSTM) resets the flip-flop.

Sample Sync Error (SSER) is generated four bytes after the target is past. If the sync mark has not been detected, the Sync Error flip-flop will set (sheet 12).

The two flip-flops in package 14B enable and disable the comparators during disk initialization. During normal read and write operations the false Initialize (INIT) signal keeps First Index Detected (FIND) true to keep the flip-flops locked off. During an initialization the true INIT allows Start Header Bit (STHB) to clock the flip-flop on.

Status Read

This register allows the Z80 to sample several condition bits. The two flip-flops in package 19H latch signals Index Detected (INDET) and Address Mark Detected (AMDET). These stay latched until cleared by a Z80 write to address 602E. The state of the Initial flip-flop (Mode/Path Register) and Split Memory bit can also be sampled in this register.

Mode/Path Register

The Mode/Path Register is used by the Z80 to set parameters and select data paths for disk drive operations. It consists of two four-bit programmable binary counters with their count enable inputs permanently held false. The parameter bits are latched into the register by a Z80 write to address 6020. The data is available at the outputs (pins 2-6) by reading address 6020.

The counter representing the four LS bits is reset, via 14C, after an initialize track command has been executed. Flip-flop 13B is also cleared by this initialize operation. This flip-flop latches the Initialize (INIT) bit, and is set or reset by the LS bit of the data word in a Z80 write to address 6021.

Sheet 10

Disk Data Control Sequencer

The Disk Data Control Sequencer (DDCS) allows the LCDC to make use of the low access time and high bit-transfer rates of Winchester technology disk drives. The DDCS produces a unique sequence of control signals in response to each of the commands issued by the Z80. These control signals enable blocks of logic in an order defined by the disk access algorithms. These control sequences are stored in four PROMs.

The Z80 controls the DDCs by writing to addresses 6018 through 601C. The actual command generated by the Z80 is a four-bit number comprised of the three LS bits of the Z80 address bus and the DWEN signal latched in the Mode/Path register. If the DWEN bit is on (true) the function is a write operation; if off, it is a read.

CMLD, generated by the Z80 to load a command into the DDCS, is generated by the Strobe Decode logic on sheet four. This signal selects the three LS bits of the Z80 address bus and DWEN as the inputs to selector 12A. Because the DDCS command signals are byte-oriented, the loading of a command is synchronous with the drive related Byte Marker Clock (BMCK).

To accomplish this synchronization, flip-flop 11C is in its initial state when a command is loaded into the DDCS. This generates a false Command Sync (CSYN) signal at pin eight. This signal is ANDed with CMDLD (Strobe Decode logic, sheet 4) to generate ZWAIT and 1CMDLD. The true ZWAIT causes the Z80 to cease processing. The 1CMDLD presets flip-flop 12C, causing a high to be applied to pin 12 of flip-flop 11C. When BMCK clocks 11C, CSYN goes true. A true CYSN causes both 1CMDLD and ZWAIT to become false. The rising of 1CMDLD clocks the DDCS command into latch 11A. The Z80 resumes processing when ZWAIT goes false.

The output of 11A provides the four LS address bits for the Sequence ROM (10A) and Chunk ROM (9A). 11A also provides bits six through nine of the Byte ROM (5A and 6A) address. The MS address bit for all ROMs is stored in flip-flop 11C and is set to zero when a command is loaded. The Byte ROMs also use the output of the byte counter in the Disk Bit Reference Counter (DBRC) to reference their output to the byte number of the current chunk.

When CSYN goes true it clears 12C at pin one, and through OR gates 11D and 13C, presets the other half of 12C to generate a false Select Clock Enable (SCE). SCE false disables clock selector 8C, which is used to select the event marker for the DDCS. On the next BMCK the CSYN flip-flop is reset. This resets 12C, allowing SCE to go true when DBRC2 becomes true. DBRC2 becomes true four bits into every byte. SCE also enables selector 8C.

The four LS bits of the Sequence ROM are looped back through data selector 12A (CMDLD = false) to the inputs of latch 11A. The fifth output bit is looped back to flip-flop 11C. When the event marker selected by 8C becomes true, these five bits from the ROM are latched to form the address for the DDCS.

The event marker causes one of the flip-flops in 12C to set (pin five high), turning off the other flip-flop in 12C at pin 10. This disables selector 8C. With pin five of 12C high, the CSYN flip-flop sets on the next BMCK, forcing 12C off. This allows the CSYN flip-flop to reset on the next BMCK. This allows the SCE flip-flop to set when DBRC2 occurs. This enables the event marker selector (8C) and readies the DDCS for the next sequence. Because it controls the select inputs of 8C, the DDCS defines the next event marker.

The command signals generated during a control sequence are latched in octal flip-flops 7A and 8A, synchronous with Byte Marker Clock (BMCK).

The three control signals generated by the Sequence ROM are latched in quad flip-flop 11B. These signals: Command Load Bit (CLB), Start Header Bit (STHB), and Start Command Bit (STCB) are used to initialize certain blocks of logic at the start of a DDCS sequence. Because they are inputs to clock, preset, or clear pins of flip-flops they must be terminated as the sequence begins. This termination is done by blip-flop 5C clearing latch 11B one byte after Data Command (DATCMD) becomes true. DATCMD is generated by the DDCS to indicate that the control signals are valid.

The flip-flop preset by CLB (13B on sheet 10) generates Sector Command (SECCMD). This indicates a DDCS command sequence is in progress. SECCMD is reset at the end of a data command sequence by Command End (CEND) and at the end of a header initialize by Initialize Done (INDN).

When enabled by Split Data Command (SDCM), flip-flop 8D generates Split Memory (SPLTM) to keep Write Enable (WREN) high when a split data operation is required during a write. This also keeps the ECC generator from clearing when reading or writing is resumed after a split. Flip-flop 8D is cleared by Sync Operation (SYNCOP), indicating the Start Sector Data command has been issued to restart data after a split.

Sheet 11

Disk Receivers

The Disk Receiver logic is 16 line receivers in eight packages. The 16 receivers are divided into four groups, one for each of the drives that can be connected to the LCDC. Each group receives data, clocks, and status information from its drive. Each receiver monitors the twisted pair of wires of one bus line. The twisted pair allows relatively noise-free operation.

Disk Receiver Multiplexer

These multiplexers (15H and 16D) select between the four groups of drive receivers. The selected drive is determined by the two Device Select (DEVS0 and DEVS1) signals.

Disk Transmitters

This logic is eight line drivers contained in four packages. These eight drivers are divided into four groups, one for each of the drives that can be connected to the LCDC. The only two signals provided to the drives are Write Clock and Write Data. Each driver drives the twisted pair of one bus line. The twisted pair allows relatively noise-free operation.

Transmitter Multiplexer

This multiplexer selects between the four groups of Disk Transmitters. The selected drive is determined by the two Device Select (DEVS0 and DEVS1) signals.

Crystal Clock

The Crystal Clock is a 20 MHz oscillator and two flip-flops. The flip-flops divide the output of the oscillator to provide 10 MHz and 5 MHz clocks.

Sheet 12

Data In Multiplexer and Clock Multiplexer

The Data In Multiplexer selects either receive data from the disk drive or transmit data from the transmit shift register for loop back testing. The selector is controlled by two NOR gates in package 15E. If pin 4 and pin 10 are both low, data is selected from the transmit shift register. If pin 4 is low and pin 10 high, the selection is grounded for use during error correction. If pin 4 is high and pin 10 low, receive data from the disk drive is selected. If both pins are high, data is selected from the transmit shift register.

The Clock Multiplexer selects which of four clocks will be used for the Shift Register Clock (SRC). Because this multiplexer has the same select inputs as the Data In Multiplexer, the clocks are directly associated with the data inputs. The exception is Servo Clock (SCLK) which is used to synchronize transmit data. During transmit operations data routed through the Data In Multiplexer to the Receive Shift Register is ignored.

ECC Data Multiplexer

The ECC Data Multiplexer is two four-to-one data multiplexers with common select inputs located in package 16E. One (output pin 7) selects from three sources of serialized data for transmission to the drive or for loop-back testing. The other (output pin 9) selects data for the Error Correction Code logic.

The selection is controlled by two NOR gates in package 15E. If pin 1 is low and pin 13 is high, data from the transmit shift register is selected for loop-back testing. If pin 1 and pin 13 are both low, both outputs of the multiplexers are grounded for use during error correction. If pin 1 is high and pin 13 low, the serial product of the ECC generation logic is looped back into the generator and transmitted to disk simultaneously during an ECC write. If both pins are high, serial data from the transmit shift register is sent to the drive and the ECC logic.

Sync Generator

This generator produces the sync mark to synchronize read operations. The mark, a FF19, is written before header and data fields. This generator is an eight-bit shift register with both serial and parallel inputs. It is connected serially with the Transmit Shift Register.

During writes, the Sync Write (SYNCWR) signal is generated for a period equal to one byte of disk data, four bytes before the real data starts. The low/true SYNCWR signal, via negative OR gate 5F, shifts eight ones (FF) into the LS byte of the transmit shift register (5H). This signal also parallel loads the second byte of the sync mark (19) into 6F. At the end of the byte, SYNCWR goes false, and begins shifting data out of 6F. After 16 shift clocks from when SYNCWR originally went true, the entire sync mark will be present in the transmit shift register. The two byte lapse between the sync mark and start of data allows the mark to shifted out of the transmit register before the first data word is parallel loaded into the transmit register.

Sync Detect

This logic is several NAND and AND gates arranged to detect the hex value FF19 at the output of the Receive Shift Register.

If Sync Search (SSRCH) or Force Search (FSRCH) is true, pin 9 of NAND gate 1F becomes low, synchronous with SRC, when the sync mark appears at the output of the receive shift register. This low (Sync Detect, SYNCD) presents flip-flop 8D via NOR gate 1E. 8D generates Sync Found (SYNCFD) until cleared by a Start Command Bit (STCB) or a Drive Command Abort (DCA).

The signal Strobe Sync Error (SSER) is generated by the Target Comparator logic (sheet 9) as the drive head passes out of the target area. If the sync mark has not been detected (SYNCFD = false), flip-flop 10 D sets and Sync Error (SYNCER) will be generated.

Transmit Shift Register

This register is two eight-bit serial shift registers, with both serial and parallel inputs, connect serially to allow 16-bit words to be loaded parallely and shifted out serially.

The signal Drive/FIFO Output Latch Flag Clock (DFOLFC) is used to load the shift registers. When there is a valid data word in the output latch of the FIFO, and the proper data path is enabled, DFOLFC will become true synchronous with Word Time (WDTM) and remain true for one bit-time (SRC period). When DFOLFC is true the data word is loaded into the register by the rising edge of SRC. This process is repeated every WDTM until the transfer is completed.

Receive Shift Register

The Receive Shift Register is two eight-bit parallel output serial shift registers connected in series to allow for a 16-bit data word. This data word from the drive is sampled under control of the Drive DMA Control logic on sheet seven.

Shift Buffer

This buffer resynchronizes the data before it is transmitted to the drive. This is required because of propagation delays caused by routing the transmit data through selector 16E.

Sheet 13

Error Correcting Code Generator

The Error Correcting Code Generator detects and corrects data errors caused by small, marginally defective areas on the disk media.

The generator is a 32-bit shift register divided into five smaller shift registers. The first register has nine bits, the second two, the third ten, the fourth nine, and the fifth two. There are EXECLUSIVE OR gates between each of the sections to combine the output of the upstream section with the data bit currently being input. The final output, ECC Data Out (ECCDT), is looped back and EXCLUSIVE ORed with the input, ECC Data In (ECCDI).

The outputs of each stage of the first three registers are ANDed to produce Zero Found (ZF). ZF will be true if there are no ones in any of the stages. The outputs of all 32 stages are ANDed to produce Zero Pattern (ZP). A true ZP indicates there are no ones in any stage of the generator.

During write operations the data generated by the Transmit Shift Register is input into the ECC as it is transferred to disk. At the end of the transfer there will be a unique 32-bit pattern remaining in the ECC register. This code is written onto the disk immediately after the data it represents.

When data is read from the disk the data received by the Receive Shift Register is shifted into the ECC generator. At the end of the data field there will be a 32-bit code left in the generator. If there were no errors during the read, the code will be identical to the code generated when the data was written. The two codes are EXCLUSIVELY ORed, and if they are identical ZP will be true, if not, ZP goes false and error correction procedures are started.

Sheet 14

Disk Bit Reference Counter

The Disk Bit Reference Counter (DBRC) keeps track of the position of the drive head relative to the disk media. The DBRC uses the Shift Register Clock (SRC) to count bits, bytes, and chunks.

The counter is five programmable, four-bit binary counters. The first counter, 3C, counts eight SRCs (bits) before it overflows and reinitializes via NOR gate 2D. With each overflow, the byte counter (2A and 3A) is incremented by one. Only the LS bit of 3A is used. When the byte counter overflows, the chunk counter (2B and 2C) is incremented. All eight of the chunk counter outputs are used to allow a maximum chunk count of 256.

The DBRC generates several markers: Byte Marker Clock (BMCK), during the last bit of every byte; Word Time (WDTM), every 16-bits; and Slice Marker Time (SMTM), every 32 bytes. The BDRC also counts bits during ECC operations.

The flip-flops in 5D allow the DBRC to be single stepped as a diagnostic operation.

Selector 4A chooses the Address Mark Detect (AMDET) or Index Mark Detected (INDET) to reinitialize the DBRC. INDET is used during initial formatting, and AMDET is used during normal data operations. The flip-flops in 4D generate the resync pulse and the gate logic defines whether the bit and byte counters, the chunk counter, or both are reinitialized.

5.20.3 LARGE CAPACITY DISK CONTROLLER GLOSSARY

The following glossary defines all of the signals contained on the LCDC logic diagram. In the PCBA column 'C' indicates the Control Adaptor PCBA and 'D' indicates the Data Adaptor PCBA.

SIGNAL	PCBA	SHEET OF ORIGIN	DEFINITION
A10/CS	C	5	Address 10/Chip Select
ACLK	C	3	Alternate Clock
AD00-15	C	7	Address Bus
ADX1,2,3	C	9	Address Extension Bits
AMDET	C	6	Address Mark Detect

SIGNAL	PCBA	SHEET OF ORIGIN	DEFINITION
AMEN	D	10	Address Mark Enable
ASRCH	D	14	Address Mark Search
BCLK	C	3	Bus Clock
BHLD	C	3	Bus Hold
BMCK	D	14	Byte Marker Clock
BRQ2	C	8	Bus Request
BST	C	7	Boot Strap
BUS00-09	C	6	Disk Bus
BUSY	C	3	Busy
CAS	C	12	Controller Address Select
CEND	D	10	Command End
CLB	D	10	Command Load Bit
CLK10	D	11	10 MHz. Clock
CLK16	C	12	16 MHz. Clock
CLK5	D	11	5 MHz. Clock
CLKSL0-2	D	10	Clock Select
CMDLD	D	4	Command Load
CSEN	D	7	Clock Selector Enable
CSYN	D	10	Command Synchronize
CTC	C	5	Counter/Timer Circuit
D00-15	C	8	UBUS Data
DATCMD	D	10	Data Command
DBRC00-15	D	14	Disk Bit Reference Counter Bus
DCA	D	10	Drive Command Abort
DERR	C	3	Data Error
DEVS0-1	C	6	Device Select

SIGNAL	PCBA	SHEET OF ORIGIN	DEFINITION
DEVSE	C	6	Device Select Tag
DEVSLD	D	2	Device Selected
DFILFC	D	7	Drive FIFO Input Latch Flag Clock
DFOLEC	D	7	Drive FIFO Output Error Latch Clock
DFOLFC	D	7	Drive FIFO Output Latch Flag Clock
DMAEN	D	10	DMA Enable
DREQ	D	7	DMA Request
DRILFC	D	7	Drive RAM Input Latch Flag Clock
DRSLS	D	11	Drive Selected
DRUN	C	9	DMA Run
DTROP	D	7	Drive To RAM Operation
DWEN	D	9	Drive Write Enable
ECCDI	D	12	ECC Data Input
ECCDO	D	13	ECC Data Output
ECCLR	D	10	ECC Clear
ECCORF	D	14	ECC Correct Function
ECCOR	D	14	ECC Correction Shift
ECCUM	D	10	ECC Cummulate
ECCWR	D	10	ECC Write
ECFRS	D	12	ECC Function Reset
ENUDH	C	10	Enable UBUS Data High Byte
ENUDL	C	10	Enable UBUS Data Low Byte
ERRS	C	9	Error Reset
FDB00-15	D	6	FIFO Data Bus

SIGNAL	PCBA	SHEET OF ORIGIN	DEFINITION
FF10W	C	7	FF10 Write
FF11W	C	7	FF11 Write
FF12W	C	7	FF12 Write
FF13W	C	7	FF13 Write
FILE	D	6	FIFO Input Latch Error
FILF	D	6	FIFO Input Latch Flag
FILLC	D	7	FIFO Input Latch Clock, MS Byte
FILMC	D	7	FIFO Input Latch Clock, LS Byte
FILMH	D	5	FIFO Input Latch Hold
FIND	D	9	First Index Detected
FIR	D	6	FIFO Input Ready
FOLE	D	6	FIFO Output Latch Error
FOLF	D	6	FIFO Output Latch Flag
FOR	D	6	FIFO Output Ready
FOUTE	C	5	Force Out Enable
FSRCH	D	7	Force Sync Search
FTROP	D	7	FIFO To RAM Operation
FWR	D	7	FIFO Write
GIN2	C	3	Grant In 2
GOT2	C	8	Grant Out 2
GTMF	C	11	Grant Memory FIFO
GTMZ	C	11	Grant Memory Z80
GTU	C	7	Grant Bus
GTZ	C	7	Grant Z80
HL0-3	C	12	Header Lock

SIGNAL	PCBA	SHEET OF ORIGIN	DEFINITION
HSRE	D	10	Header Slice Reset Enable
HSTM	D	14	Header Slice Time
INDET	C	6	Index Detected
INDN	D	9	Initialize Track Done
INIT	D	9	Initialize Mode
INRD	C	10	Interrupt Level D
MAB0-9	C	11	Memory Address Bus
MACK	C	7	Memory Acknowledge
MASTER	C	8	Master
MCYC	C	8	Memory Cycle
MDB0-7	D	5	Memory Data Bus
MPRT	C	12	Master Protect
MWRT	C	8	Memory Write
ONCYL	C	3	On Cylinder
OUTE	C	7	Out Enable
PAD0-4	D	10	PROM Address
PDF	D	9	Path Drive To FIFO
PDFRD	D	7	Path Drive, FIFO Read
PDR	D	9	Path Drive To RAM
PLB	D	9	Path Loop Back
PPG0-7	C	5	PROM Page
PRF	D	9	Path RAM To FIFO
PRPG8-11	C	5	PROM or RAM Page
PSH	C	6	Power Sequence Hold
PSP	C	6	Power Sequence Pick

SIGNAL	PCBA	SHEET OF ORIGIN	DEFINITION
PT	D	9	Past Target
PTRE	C	5	PROM Transceiver Enable
RAMCK	D	7	RAM Clock
RAMD	D	7	RAM Demand
RAMW	C	11	RAM Write
RAMZ	C	5	RAM Z80
RCEN	D	10	Read Clock Enable
RCLK	D	2	Receive Clock
RD6000-600F	C	5	Read 6000-600F
RD6020-602D	D	4	Read 6020-602D
RDAT	D	2	Receive Data
RDB00-15	D	12	Receive Data Bus
RDEN	D	10	Read Enable
REGDC	C	5	Register Decode
RFOLFC	D	7	RAM FIFO Output Latch Flag Clock
RILF	D	5	RAM Input Latch Flag
RILFC	D	7	RAM Input Latch Flag Clock
RPG0-3	C	11	RAM Page
RS	C	12	Reset
RSYNCA	D	14	Resync A
RTFOP	D	7	RAM To FIFO Operation
RUN	C	12	Run
RWEN	D	9	RAM Write Enable
SACE	D	10	Slice Advance Clock Enable
SCLK	D	10	Servo Clock

SIGNAL	PCBA	SHEET OF ORIGIN	DEFINITION
SCTL	C	6	Set Control
SCYL	C	6	Set Cylinder
SDCM	D	10	Split Data Chain Memory
SECCMD	D	10	Sector Command Active
SEER	C	3	Seek Error
SHD	C	6	Set Head
SKCKL	D	7	Skip Clock
SKPC	C	9	Skip Control
SLRD	C	7	Slave Read
SMTM	D	14	Slice Marker Time
SPLTM	D	10	Split Memory
SRC	D	12	Shift Register Clock
SSER	D	9	Sample Sync Error
SSRCH	D	10	Sync Search
STCB	D	10	Start Command Bit
STHB	D	10	Start Header Command Bit
SYNCD	D	12	Sync Pattern Detected
SYNCER	D	12	Sync Error
SYNCFD	D	12	Sync Found
SYNCOP	D	10	Sync Operation
SYNCWR	D	10	Sync Write
TEI	D	9	Target End Interrupt
TLE	D	9	Target Leading Edge
TS	D	9	Target Splice
UAB00-15	C	7	Universal Address Bus
UBERR	C	9	UBUS Error

SIGNAL	PCBA	SHEET OF ORIGIN	DEFINITION
UBTO	C	8	UBUS Timeout
UDB00-15	C	8	Universal Data Bus
UFILFC	D	7	UBUS To FIFO Input Latch Flag Clock
UFOLFC	D	7	UBUS From FIFO Output Latch Flag Clock
UNS	C	3	Unsafe
URDY	C	3	Unit Ready
WCLK	D	11	Write Clock
WDAT	D	12	Write Data
WDAT	D	11	Write Data
WDCK	D	7	Word Clock
WDTM	D	14	Word Time
WPROT	C	3	Write Protected
WR6001-600F	C	5	Write 6001-600F
WR6020-602F	D	4	Write 6020-602F
WRCYL	C	9	Write Cycle
WREN	D	10	Write Enable
XCEN	D	9	XTAL Clock Enable
ZAB0-15	C	4	Z80 Address Bus
ZCLK	C	12	Z80 Clock
ZDB0-7	C	4	Z80 Data Bus
ZF	D	13	Zero Found
ZINT	C	4	Z80 Interrupt
ZIOREQ	C	4	Z80 I/O Request
ZMERQ	C	4	Z80 Memory Request
ZP	D	13	Zero Pattern

SIGNAL	PCBA	SHEET OF ORIGIN	DEFINITION
ZRD	C	4	Z80 Read
ZUBRF	C	5	Z80 UBUS Register Request
ZWAIT	D	4	Z80 Wait
ZWR	C	4	Z80 Write