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134-190243-0

A

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装置名

806-120258-0

TF1600 MAGNETIC TAPE FORMATTER
CIRCUIT DIAGRAM

REV	COMP	DESCRIPTION(SC)	APP
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1	0	1980.5.1	—
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NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
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大橋

今村



TF1600
MAGNETIC TAPE
FORMATTER
CIRCUIT DIAGRAM

134-190243-0

NEC

SHT 1/2

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6

7

TABLE OF CONTENTS

134-190243-0

A

B

C

D

E

装置名

REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	—
NEXT SPEC			
DRAFT	ENG	CHK	APP ISSUE
	大橋		今村
TF1600 MAGNETIC TAPE FORMATTER CIRCUIT DIAGRAM			
134-190243-0			
NEC			SHT 2/2

A

B

C

D

E

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134-190244-0

1. CONFIGURATION

TF1600 MAGNETIC TAPE FORMATTER CIRCUIT DIAGRAMS.
Consists of the following :

(1) INTRODUCTORY REMARKS OF TF1600 FORMATTER CIRCUIT

It describes the introduction of understanding the diagrams.

(2) TF1600 MAGNETIC TAPE FORMATTER LOGIC CIRCUIT DIAGRAMS.

It describes the logic circuit.

(3) MTA 160 FMT TESTER CIRCUIT DIAGRAM.


It consists of the logic circuit of FMT tester for maintenance.

(4) TF1600 MAGNETIC FORMATTER CABLE CONNECTION.

It illustrates the cable connection between the logic circuits, FMT tester and the outer cable, and between the other devices and them.

(5) TF1600 MAGNETIC TAPE FORMATTER POWER SUPPLY AND SUPPLYING DIAGRAM.

They illustrate the power supply circuit for TF1600 MAGNETIC TAPE FORMATTER, the connection of wiring for power supply and the supplying in the back panel.

REV/COMP	DESCRIPTION(SC)	APP
1 0	1980.5.1	—
NEXT SPEC		
DRAFT	ENG	CHK
	大橋	今村
ISSUE 57.6.16 		
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM		
134-190244-0		
NEC		SHT 1/23

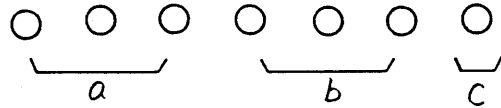
装置名

134-190244-0

2. POINT OF VIEW OF LOGIC CIRCUIT

2.1 NAMING OF LOGIC TAG

The logic tag is described by Seven characters of alphabet and numerals. illustrates the relation of the Connection between package.



- a: describes the functional block of Sending Signals or the interface between units.
- b: describes the function of signals
- c: describes the polarity of signals

Detailed Section a

FUNCTIONAL BLOCK INTERFACE	a
INTERFACE ADAPTER	IF1
FORMATTER CONTROL	FCT
DEVICE CONTROL	DCT
GCR WRITE CONTROL	GCW
PE CONTROL	PEG
NRZI CONTROL	NRG
READ LOGIC	RDL
ECC CONTROL	ECT
GCR READ FORMAT CONTROL	GRF
DESKEWING BUFFER	DSB
READ DISCRIMINATER	PLS
TESTER FOR MAINTENANCE	MNT
DAI INTERFACE	YA2
MTU INTERFACE	IFC

Detailed Section d

TRUE SIGNAL	1.3.5.7.9.B.D.F.H.J.L.N P.R.T.V.X.Z
COMPLEMENT SIGNAL	0.2.4.6.8.A.C.E.G.I.K.M O.Q.S.U.W.Y

2.2 NAMING OF SPECIAL SIGNAL

- XNU : Not used.
- X000 : is always "0"
- X100 : is always "1"
- XG00 : describes the ground.
- XP05 : describes +5V.
- XP12 : describes +12V
- XN12 : describes -12V

2.3 NAMING OF THE JUMPING TAGS

The Jumping tags illustrate the relation of the Connection in a particular package, and are described by four characters of alphabet and numerals.

REV/COMP	DESCRIPTION(SC)	APP			
1 0	1980.5.1	—			
NEXT SPEC					
DRAFT	ENG	CHK	APP	ISSUE	
	大橋		今村		
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM					
134-190244-0					
NEC				SHT	2/

装置名

134-190244-0

2.4 LOCATION OF PACKAGE

The mnemonic of packages shows the location of packages.

IF2		
IF1		
FCT	G9QWU PKG,	
DCT	G9QWT PKG, G9QWX PKG	
GCW	G9JAT PKG, G9MWU PKG	
PEG	G9JAS PKG,	
NRG	G9JAR PKG,	
RDL	G9JAB PKG, G9MWT PKG	
ECT	G9JAP PKG, G9MWS PKG	
GRF	G9QWS PKG,	
DSB	G9JAM PKG, G9MWW PKG	
PLS	G9JAK PKG, G9JAL PKG	G9NWJ PKG
PLS	G9JAK PKG, G9JAL PKG	G9NWJ PKG
PLS	G9JAK PKG, G9JAL PKG	G9NWJ PKG

REV	COMP	DESCRIPTION(SC)	APP
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NEXT SPEC			
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	大橋		今村
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM			
134-190244-0			
NEC			SHT 3/

装置名

2.5 TABLE OF INTEGRATED CIRCUIT

134-190244-0

TYPE	NAME	SYMBOL	FUNCTION
&	LS04 04 H04 S04		HEX INVERTER $\bar{Y} = A$
	06		HEX INVERTER BUFFER (0/c) $Y = \bar{A}$
	LS00 00 S00		QUAD 2-NAND GATE $\bar{Y} = A \cdot B$
	LS08 08 S08		QUAD 2-AND GATE $X = A \cdot B$
	LS10 10 S10		TRIPLE 3-NAND GATE $\bar{Y} = A \cdot B \cdot C$
	LS11 S11		TRIPLE 3-AND GATE $X = A \cdot B \cdot C$
	LS20		DUAL 4-NAND GATE $\bar{Y} = A \cdot B \cdot C \cdot D$
	LS21		DUAL 4-AND GATE $X = A \cdot B \cdot C \cdot D$
	LS30		SINGLE 8-NAND GATE $\bar{Y} = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$

TYPE	NAME	SYMBOL	FUNCTION																
&	38		QUAD 2-NAND BUFFER (0/c) $\bar{Y} = A \cdot B$																
	S133		13-INPUT NAND GATE $\bar{Y} = A \cdot B \cdot \dots \cdot M \cdot N$																
≥ 1	LS27		TRIPLE 3-NOR GATE $\bar{Y} = A + B + C$																
	LS32		QUAD 2-OR GATE $X = A + B$																
	S02		QUAD 2-NOR GATE $\bar{Y} = A + B$																
= 1	LS86 86		QUAD EXCLUSIVE OR GATE $X = A \oplus B$																
	LS266		QUAD 2-EXCLUSIVE NOR GATE $\bar{Y} = A \oplus B$																
AOR	LS51 51 S51		DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE OR $\bar{Y} = A \cdot B \cdot C + D \cdot E \cdot F$ $\bar{Y} = B \cdot C + E \cdot F$																
SEL	LS157 S157 LS257 LS158		<table border="1"> <tr> <td>S0</td> <td>E0</td> <td>Tn</td> <td>Fn</td> </tr> <tr> <td>0</td> <td>0</td> <td>nA</td> <td>nA</td> </tr> <tr> <td>1</td> <td>0</td> <td>nB</td> <td>nB</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>1</td> </tr> </table> <p>Fn : LS158 LS257 : 3-State output</p>	S0	E0	Tn	Fn	0	0	nA	nA	1	0	nB	nB	X	1	0	1
S0	E0	Tn	Fn																
0	0	nA	nA																
1	0	nB	nB																
X	1	0	1																

REV	COMP	DESCRIPTION(SC)	APP
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NEXT SPEC			
DRAFT	ENG	CHK	APP
	大橋		今村
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM			
134-190244-0			
NEC			SHT 4/

134-190244-0

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B

C

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装置名

REV/COMP DESCRIPTION(SC) APP

1 0 1980.5.1

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	

TF1600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

NEC SHT 5/

TYPE	NAME	SYMBOL	FUNCTION																																																												
SEL	LS153 153 S153 LS253		DUAL 4-INPUT MULTIPLEXER <table border="1"> <tr><th>S0</th><th>S1</th><th>E0</th><th>Tn</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>nA</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>nB</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>nC</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>nD</td></tr> <tr><td>x</td><td>x</td><td>1</td><td>0</td></tr> <tr><td colspan="4" style="text-align: right;">3-STATE</td></tr> </table> <p>LS253 : 3-STATE OUTPUT</p>	S0	S1	E0	Tn	0	0	0	nA	0	1	0	nB	1	0	0	nC	1	1	0	nD	x	x	1	0	3-STATE																																			
S0	S1	E0	Tn																																																												
0	0	0	nA																																																												
0	1	0	nB																																																												
1	0	0	nC																																																												
1	1	0	nD																																																												
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3-STATE																																																															
	LS151		8-INPUT MULTIPLEXER <table border="1"> <tr><th>S0</th><th>S1</th><th>S2</th><th>E0</th><th>T0</th><th>F0</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0A</td><td>0A</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0B</td><td>0B</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0C</td><td>0C</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0D</td><td>0D</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0E</td><td>0E</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0F</td><td>0F</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0G</td><td>0G</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0H</td><td>0H</td></tr> <tr><td>x</td><td>x</td><td>x</td><td>1</td><td>0</td><td>1</td></tr> </table>	S0	S1	S2	E0	T0	F0	0	0	0	0	0A	0A	0	0	1	0	0B	0B	0	1	0	0	0C	0C	0	1	1	0	0D	0D	1	0	0	0	0E	0E	1	0	1	0	0F	0F	1	1	0	0	0G	0G	1	1	1	0	0H	0H	x	x	x	1	0	1
S0	S1	S2	E0	T0	F0																																																										
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0	0	1	0	0B	0B																																																										
0	1	0	0	0C	0C																																																										
0	1	1	0	0D	0D																																																										
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DF	LS74 74 S74		DUAL D-TYPE FLIP-FLOP <table border="1"> <tr><th>0A</th><th>CP</th><th>MS</th><th>MR</th><th>T0</th><th>F0</th></tr> <tr><td>x</td><td>x</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>x</td><td>x</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>↑</td><td>1</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>x</td><td>0</td><td>1</td><td>1</td><td>HOLD</td><td>T0</td></tr> <tr><td>x</td><td>1</td><td>1</td><td>1</td><td>HOLD</td><td>T0</td></tr> <tr><td>x</td><td>x</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> </table>	0A	CP	MS	MR	T0	F0	x	x	1	0	0	1	x	x	0	1	1	0	0	↑	1	1	0	1	1	↑	1	1	1	0	x	0	1	1	HOLD	T0	x	1	1	1	HOLD	T0	x	x	0	0	1	1												
0A	CP	MS	MR	T0	F0																																																										
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	LS174 S174		HEX D-TYPE FLIP-FLOP <table border="1"> <tr><th>nA</th><th>CP</th><th>MR</th><th>Tn</th></tr> <tr><td>x</td><td>x</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>↑</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>↑</td><td>1</td><td>1</td></tr> <tr><td>x</td><td>0</td><td>1</td><td>HOLD</td></tr> <tr><td>x</td><td>1</td><td>1</td><td>HOLD</td></tr> </table>	nA	CP	MR	Tn	x	x	0	0	0	↑	1	0	1	↑	1	1	x	0	1	HOLD	x	1	1	HOLD																																				
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TYPE	NAME	SYMBOL	FUNCTION																																																															
DF	LS175 175 S175		QUAD D-TYPE FLIP-FLOP <table border="1"> <tr><th>nA</th><th>CP</th><th>MR</th><th>Tn</th><th>Fn</th></tr> <tr><td>x</td><td>x</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>↑</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>x</td><td>0</td><td>1</td><td>HOLD</td><td>HOLD</td></tr> <tr><td>x</td><td>1</td><td>1</td><td>HOLD</td><td>HOLD</td></tr> </table>	nA	CP	MR	Tn	Fn	x	x	0	0	1	0	↑	1	0	1	1	↑	1	1	0	x	0	1	HOLD	HOLD	x	1	1	HOLD	HOLD																																	
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x	1	1	HOLD	HOLD																																																														
	LS273 LS374		OCTAL D-TYPE FLIP-FLOP <table border="1"> <tr><th>0n</th><th>CP</th><th>MR(E0)</th><th>Tn</th></tr> <tr><td>x</td><td>x</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>↑</td><td>1</td><td>3-STATE</td></tr> <tr><td>1</td><td>↑</td><td>1</td><td>0</td></tr> <tr><td>x</td><td>0</td><td>1</td><td>HOLD</td></tr> <tr><td>x</td><td>1</td><td>1</td><td>HOLD</td></tr> </table> <p>LS374 : 3-STATE OUT (E0)</p>	0n	CP	MR(E0)	Tn	x	x	0	0	0	↑	1	3-STATE	1	↑	1	0	x	0	1	HOLD	x	1	1	HOLD																																							
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JK	S112		DUAL J-K EDGE TRIGGERED FLIP-FLOP <table border="1"> <tr><th>MS</th><th>MR</th><th>CP</th><th>J0</th><th>K0</th><th>T0</th><th>F0</th></tr> <tr><td>0</td><td>1</td><td>x</td><td>x</td><td>x</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>x</td><td>x</td><td>x</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>x</td><td>x</td><td>x</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>↓</td><td>0</td><td>0</td><td>Q0</td><td>Q0</td></tr> <tr><td>1</td><td>1</td><td>↓</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>↓</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>↓</td><td>1</td><td>1</td><td>TOG</td><td>GLE</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>x</td><td>x</td><td>Q0</td><td>Q0</td></tr> </table>	MS	MR	CP	J0	K0	T0	F0	0	1	x	x	x	1	0	1	0	x	x	x	0	1	0	0	x	x	x	1	1	1	1	↓	0	0	Q0	Q0	1	1	↓	1	0	1	0	1	1	↓	0	1	0	1	1	1	↓	1	1	TOG	GLE	1	1	1	x	x	Q0	Q0
MS	MR	CP	J0	K0	T0	F0																																																												
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1	1	1	x	x	Q0	Q0																																																												
LAT	LS279 279		QUAD S-R LATCH <table border="1"> <tr><th>S1-S2</th><th>R1</th><th>T0</th></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>HOLD</td></tr> </table>	S1-S2	R1	T0	0	0	1	0	1	1	1	0	0	1	1	HOLD																																																
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REV	COMP	DESCRIPTION(SC)	APP
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1	0	1980.5.1	
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TYPE	NAME	SYMBOL	FUNCTION
CNT	LS192		<p>UP/DOWN BCD COUNTER</p>
	LS193 193		<p>UP/DOWN BINARY COUNTER</p>

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D

E

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	

TF1600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

NEC SHT 6/

134-190244-0

A

B

C

D

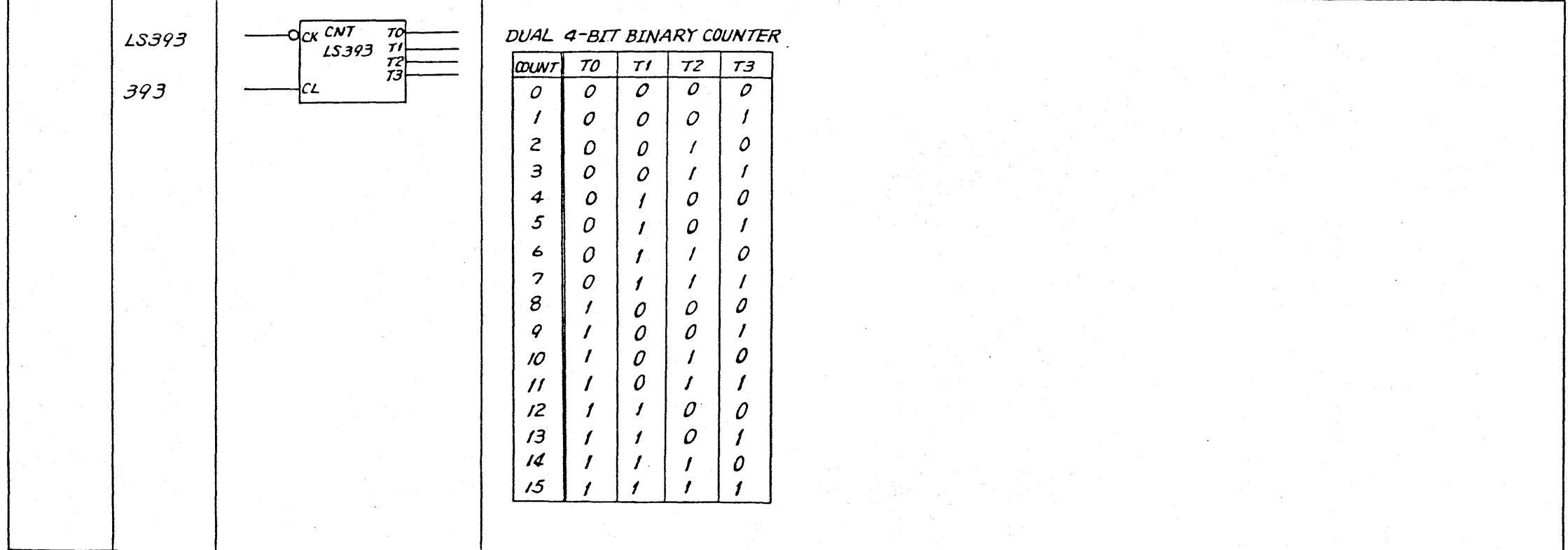
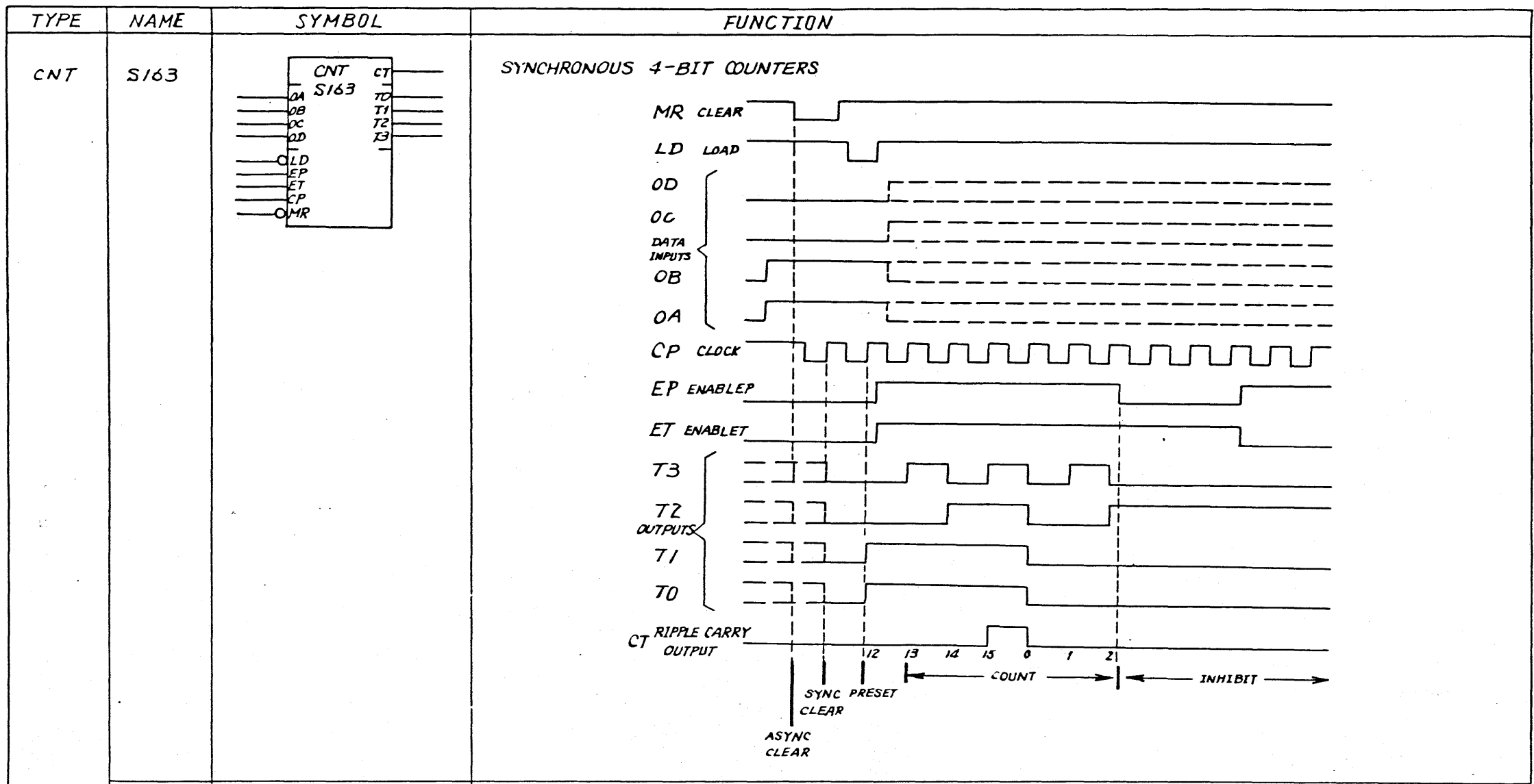
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REV	COMP	DESCRIPTION(SC)	APP
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1	0	1980.5.1	
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D

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	大橋		今村	

TF1600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

NEC SHT 7/

134-190244-0

REV/COMP	DESCRIPTION(SC)	APP
1 0	1980.5.1	—

TYPE	NAME	SYMBOL	FUNCTION																																																																																																																														
SFT	LS96		<p>5-BIT SHIFT REGISTER</p> <table border="1"> <tr><th>MR</th><th>EO</th><th>0A</th><th>1A</th><th>2A</th><th>3A</th><th>4A</th><th>CP</th><th>IS</th><th>T0</th><th>T1</th><th>T2</th><th>T3</th><th>T4</th></tr> <tr><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>X</td><td>X</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>L</td><td>X</td><td>0A₀</td><td>1A₀</td><td>2A₀</td><td>3A₀</td><td>4A₀</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>L</td><td>X</td><td>1</td><td>1A₀</td><td>1</td><td>3A₀</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>L</td><td>X</td><td>0A₀</td><td>1A₀</td><td>2A₀</td><td>3A₀</td><td>4A₀</td></tr> <tr><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>↑</td><td>1</td><td>1</td><td>0A_n</td><td>1A₀</td><td>2A_n</td><td>3A_n</td></tr> <tr><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>↑</td><td>0</td><td>0</td><td>0A_n</td><td>1A_n</td><td>2A_n</td><td>3A_n</td></tr> </table>	MR	EO	0A	1A	2A	3A	4A	CP	IS	T0	T1	T2	T3	T4	0	0	X	X	X	X	X	X	X	0	0	0	0	0	0	X	0	0	0	0	0	X	X	0	0	0	0	0	1	1	1	1	1	1	1	X	X	1	1	1	1	1	1	1	0	0	0	0	0	L	X	0A ₀	1A ₀	2A ₀	3A ₀	4A ₀	1	1	1	0	1	0	1	L	X	1	1A ₀	1	3A ₀	1	1	0	X	X	X	X	X	L	X	0A ₀	1A ₀	2A ₀	3A ₀	4A ₀	1	0	X	X	X	X	X	↑	1	1	0A _n	1A ₀	2A _n	3A _n	1	0	X	X	X	X	X	↑	0	0	0A _n	1A _n	2A _n	3A _n
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1	1	0	0	0	0	0	L	X	0A ₀	1A ₀	2A ₀	3A ₀	4A ₀																																																																																																																				
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1	0	X	X	X	X	X	↑	0	0	0A _n	1A _n	2A _n	3A _n																																																																																																																				
	LS164 164		<p>8-BIT SHIFT REGISTER SERIAL IN/PARALLEL OUT</p> <table border="1"> <tr><th>MR</th><th>CP</th><th>DO</th><th>DI</th><th>T0</th><th>T1</th><th>T2</th><th>T3</th><th>T4</th><th>T5</th><th>T6</th><th>T7</th></tr> <tr><td>0</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>X</td><td>X</td><td>T0₀</td><td>T1₀</td><td>T2₀</td><td>T3₀</td><td>T4₀</td><td>T5₀</td><td>T6₀</td><td>T7₀</td></tr> <tr><td>1</td><td>↑</td><td>1</td><td>1</td><td>1</td><td>T0_n</td><td>T1_n</td><td>T2_n</td><td>T3_n</td><td>T4_n</td><td>T5_n</td><td>T6_n</td></tr> <tr><td>1</td><td>↑</td><td>0</td><td>X</td><td>0</td><td>T0_n</td><td>T1_n</td><td>T2_n</td><td>T3_n</td><td>T4_n</td><td>T5_n</td><td>T6_n</td></tr> <tr><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>T0_n</td><td>T1_n</td><td>T2_n</td><td>T3_n</td><td>T4_n</td><td>T5_n</td><td>T6_n</td></tr> </table>	MR	CP	DO	DI	T0	T1	T2	T3	T4	T5	T6	T7	0	X	X	X	0	0	0	0	0	0	0	0	1	1	X	X	T0 ₀	T1 ₀	T2 ₀	T3 ₀	T4 ₀	T5 ₀	T6 ₀	T7 ₀	1	↑	1	1	1	T0 _n	T1 _n	T2 _n	T3 _n	T4 _n	T5 _n	T6 _n	1	↑	0	X	0	T0 _n	T1 _n	T2 _n	T3 _n	T4 _n	T5 _n	T6 _n	1	↑	X	0	0	T0 _n	T1 _n	T2 _n	T3 _n	T4 _n	T5 _n	T6 _n																																																						
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1	1	X	X	T0 ₀	T1 ₀	T2 ₀	T3 ₀	T4 ₀	T5 ₀	T6 ₀	T7 ₀																																																																																																																						
1	↑	1	1	1	T0 _n	T1 _n	T2 _n	T3 _n	T4 _n	T5 _n	T6 _n																																																																																																																						
1	↑	0	X	0	T0 _n	T1 _n	T2 _n	T3 _n	T4 _n	T5 _n	T6 _n																																																																																																																						
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	LS165		<p>PARALLEL LOAD 8 BIT SHIFT REGISTER</p> <table border="1"> <tr><th>MS</th><th>CH</th><th>CP</th><th>AO</th><th>0A-----0H</th><th>INTERNAL 0A</th><th>INTERNAL 0B</th><th>TO</th><th>FO</th></tr> <tr><td>0</td><td>X</td><td>X</td><td>X</td><td>a-----h</td><td>a</td><td>b</td><td>h</td><td>h</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>X</td><td>X</td><td>Q_{A0}</td><td>Q_{B0}</td><td>Q_{H0}</td><td>Q_{H0}</td></tr> <tr><td>1</td><td>0</td><td>↑</td><td>1</td><td>X</td><td>1</td><td>Q_{An}</td><td>Q_{Gn}</td><td>Q_{Gn}</td></tr> <tr><td>1</td><td>0</td><td>↑</td><td>0</td><td>X</td><td>0</td><td>Q_{An}</td><td>Q_{Gn}</td><td>Q_{Gn}</td></tr> <tr><td>1</td><td>1</td><td>X</td><td>X</td><td>X</td><td>Q_{A0}</td><td>Q_{B0}</td><td>Q_{H0}</td><td>Q_{Gn}</td></tr> </table>	MS	CH	CP	AO	0A-----0H	INTERNAL 0A	INTERNAL 0B	TO	FO	0	X	X	X	a-----h	a	b	h	h	1	0	0	X	X	Q _{A0}	Q _{B0}	Q _{H0}	Q _{H0}	1	0	↑	1	X	1	Q _{An}	Q _{Gn}	Q _{Gn}	1	0	↑	0	X	0	Q _{An}	Q _{Gn}	Q _{Gn}	1	1	X	X	X	Q _{A0}	Q _{B0}	Q _{H0}	Q _{Gn}																																																																								
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1	1	X	X	X	Q _{A0}	Q _{B0}	Q _{H0}	Q _{Gn}																																																																																																																									
	LS195		<p>4-BIT SHIFT REGISTER</p> <table border="1"> <tr><th>MR</th><th>EO</th><th>CP</th><th>JO</th><th>KO</th><th>0A</th><th>1A</th><th>2A</th><th>3A</th><th>T0</th><th>T1</th><th>T2</th><th>T3</th><th>F3</th></tr> <tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>↑</td><td>X</td><td>X</td><td>a</td><td>b</td><td>c</td><td>d</td><td>a</td><td>b</td><td>c</td><td>d</td><td>a</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>T0₀</td><td>T1₀</td><td>T2₀</td><td>T3₀</td><td>T3₀</td></tr> <tr><td>1</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>T0₀</td><td>T0₀</td><td>T1₀</td><td>T2₀</td><td>T2₀</td></tr> <tr><td>1</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>T0_n</td><td>T1_n</td><td>T2_n</td><td>T2_n</td></tr> <tr><td>1</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>T0_n</td><td>T1_n</td><td>T2_n</td><td>T2_n</td></tr> <tr><td>1</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>T0_n</td><td>T0_n</td><td>T1_n</td><td>T2_n</td><td>T2_n</td></tr> </table>	MR	EO	CP	JO	KO	0A	1A	2A	3A	T0	T1	T2	T3	F3	0	X	X	X	X	X	X	X	X	0	0	0	0	1	1	0	↑	X	X	a	b	c	d	a	b	c	d	a	1	1	0	X	X	X	X	X	X	T0 ₀	T1 ₀	T2 ₀	T3 ₀	T3 ₀	1	1	↑	0	1	X	X	X	X	T0 ₀	T0 ₀	T1 ₀	T2 ₀	T2 ₀	1	1	↑	0	0	X	X	X	X	0	T0 _n	T1 _n	T2 _n	T2 _n	1	1	↑	1	1	X	X	X	X	1	T0 _n	T1 _n	T2 _n	T2 _n	1	1	↑	1	0	X	X	X	X	T0 _n	T0 _n	T1 _n	T2 _n	T2 _n														
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NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	

TF1600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

NEC SHT 8/

134 - 190244 - 0

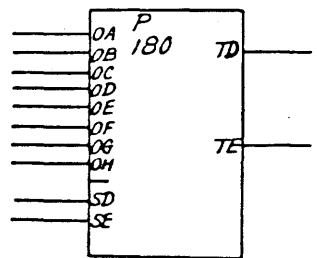
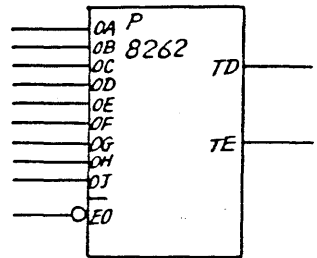
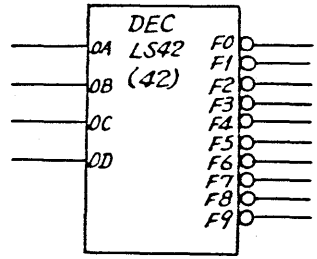
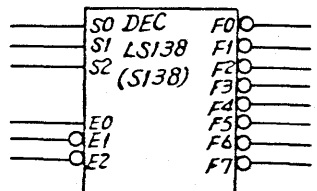
TYPE	NAME	SYMBOL	FUNCTION																				
FIFO	S225		<p><i>FIFO BUFFER MEMORY</i></p> <p><i>A FIFO is a memory storage device which allows data to be written into and/or read from its array at independent data.</i></p> <p><i>The data is processed in a parallel format, word by word.</i></p>																				
			<table border="1"> <thead> <tr> <th>Logic Pin No.</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0A ~ 4A</td> <td>Data Inputs</td> </tr> <tr> <td>CPI CP2</td> <td>Load Clock A Load Clock B</td> </tr> <tr> <td>CKIN</td> <td>Unload Clock Input</td> </tr> <tr> <td>EO</td> <td>Output Evable</td> </tr> <tr> <td>MR</td> <td>Clear</td> </tr> <tr> <td>T0 ~ T4</td> <td>Data Outputs</td> </tr> <tr> <td>IR</td> <td>Input Ready</td> </tr> <tr> <td>OR</td> <td>Output Ready</td> </tr> <tr> <td>CKD</td> <td>Unload Clock Output</td> </tr> </tbody> </table>	Logic Pin No.	Function	0A ~ 4A	Data Inputs	CPI CP2	Load Clock A Load Clock B	CKIN	Unload Clock Input	EO	Output Evable	MR	Clear	T0 ~ T4	Data Outputs	IR	Input Ready	OR	Output Ready	CKD	Unload Clock Output
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装置名

REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	—
NEXT SPEC			
DRAFT	ENG	CHK	APP ISSUE
	大橋		今村
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM			
134-190244-0			
NEC			SHT 9/

134-190244-0

REV/COMP	DESCRIPTION(SC)	APP
1 0	1980.5.1	—

TYPE	NAME	SYMBOL	FUNCTION																																																																																																																																																										
P	180		8-BIT PARITY GENERATOR/CHECKER <table border="1"> <tr> <th>Σ OF 1'S AT 0A-0H</th> <th>SE</th> <th>SD</th> <th>TE</th> <th>TD</th> </tr> <tr> <td>EVEN</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>ODD</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>EVEN</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>ODD</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> </table>	Σ OF 1'S AT 0A-0H	SE	SD	TE	TD	EVEN	1	0	1	0	ODD	1	0	0	1	EVEN	0	1	0	1	ODD	0	1	1	0	X	1	1	0	0	X	0	0	1	1																																																																																																																							
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NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	

TF1600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

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134-190244-0

TYPE	NAME	SYMBOL	FUNCTION																																																																																																																																																																																																																																																																																																																																																																																																																																																								
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ENC	LS148		<p>8-LINE TO 3-LINE OCTAL PRIORITY ENCODER</p> <table border="1"> <thead> <tr> <th>E0</th><th>0A</th><th>0B</th><th>0C</th><th>0D</th><th>0E</th><th>0F</th><th>0G</th><th>0H</th><th>F0</th><th>F1</th><th>F2</th><th>GS</th><th>CO</th> </tr> </thead> <tbody> <tr><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>X</td><td>X</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>X</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> </tbody> </table>	E0	0A	0B	0C	0D	0E	0F	0G	0H	F0	F1	F2	GS	CO	1	X	X	X	X	X	X	X	X	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	X	X	X	X	X	X	X	0	0	0	0	0	1	0	X	X	X	X	X	0	1	1	0	0	1	0	1	0	X	X	X	X	0	1	1	1	0	1	1	0	1	0	X	X	X	0	1	1	1	1	1	0	0	0	1	0	X	X	0	1	1	1	1	1	1	0	1	0	1	0	X	0	1	1	1	1	1	1	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1																																																																																																																																																																																																																																																																																																												
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TSB	LS240		<p>OCTAL BUFFERS/LINE DRIVERS/ LINE RECIVER (3-STATE)</p> <table border="1"> <thead> <tr> <th>X_n</th><th>E₀</th><th>Y_n</th> </tr> </thead> <tbody> <tr><td>Y_n</td><td>0</td><td>\bar{X}_n</td></tr> <tr><td>X</td><td>1</td><td>TRI-STATE</td></tr> </tbody> </table>	X _n	E ₀	Y _n	Y _n	0	\bar{X}_n	X	1	TRI-STATE																																																																																																																																																																																																																																																																																																																																																																																																																																															
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REV/COMP	DESCRIPTION(SC)	APP			
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NEXT SPEC					
DRAFT	ENG	CHK	APP	ISSUE	
	大橋		今村		
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM					
134-190244-0					
NEC				SHT	11/

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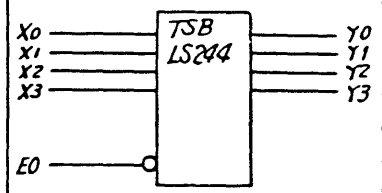
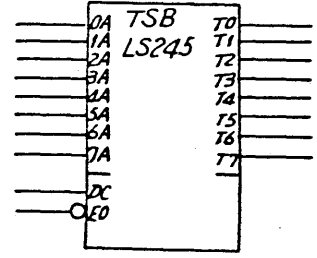
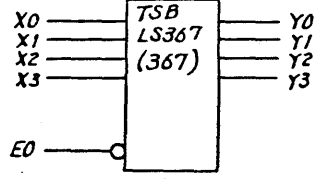
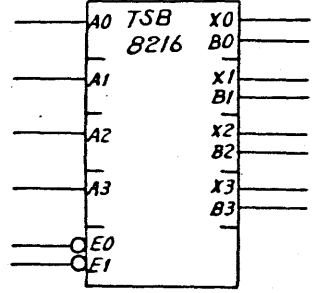
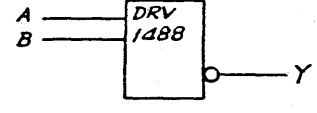
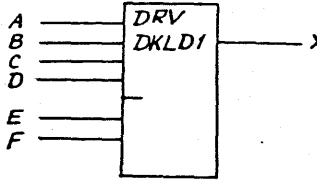
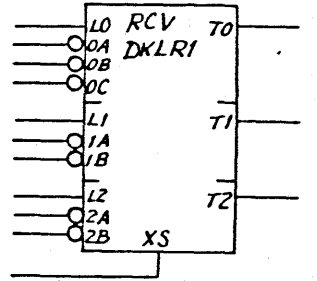
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134-190244-0

REV	COMP	DESCRIPTION(SC)	APP
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NEXT SPEC			
DRAFT	ENG	CHK	APP
	大橋		今村
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM			
134-190244-0			
NEC			SHT 12/

TYPE	NAME	SYMBOL	FUNCTION															
TSB	LS244		OCTAL BUFFERS/LINE DRIVER/LINE RECEIVER (3-STATE) <table border="1"> <tr><td>Xn</td><td>E0</td><td>Yn</td></tr> <tr><td>Xn</td><td>0</td><td>Xn</td></tr> <tr><td>X</td><td>1</td><td>3-STATE</td></tr> </table>	Xn	E0	Yn	Xn	0	Xn	X	1	3-STATE						
Xn	E0	Yn																
Xn	0	Xn																
X	1	3-STATE																
	LS245		OCTAL BUFFERS TRANCEIVERS (3-STATE) <table border="1"> <tr><td>E0</td><td>DC</td><td>OPERATION</td></tr> <tr><td>0</td><td>0</td><td>nA ← Tn</td></tr> <tr><td>0</td><td>1</td><td>nA → Tn</td></tr> <tr><td>1</td><td>X</td><td>3-STATE</td></tr> </table>	E0	DC	OPERATION	0	0	nA ← Tn	0	1	nA → Tn	1	X	3-STATE			
E0	DC	OPERATION																
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0	1	nA → Tn																
1	X	3-STATE																
	LS367 367		HEX BUFFERS 3-STATE 4 BITS & 2 BITS <table border="1"> <tr><td>Xn</td><td>E0</td><td>Yn</td></tr> <tr><td>Xn</td><td>0</td><td>Xn</td></tr> <tr><td>X</td><td>1</td><td>3-STATE</td></tr> </table>	Xn	E0	Yn	Xn	0	Xn	X	1	3-STATE						
Xn	E0	Yn																
Xn	0	Xn																
X	1	3-STATE																
	8216		4 BIT TRANCEIVER (3-STATE) <table border="1"> <tr><td>E0</td><td>E1</td><td>OPERATION</td></tr> <tr><td>0</td><td>0</td><td>A → X</td></tr> <tr><td>1</td><td>0</td><td>X → B</td></tr> <tr><td>0</td><td>1</td><td>3-STATE</td></tr> <tr><td>1</td><td>1</td><td>3-STATE</td></tr> </table>	E0	E1	OPERATION	0	0	A → X	1	0	X → B	0	1	3-STATE	1	1	3-STATE
E0	E1	OPERATION																
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1	0	X → B																
0	1	3-STATE																
1	1	3-STATE																
DRV	1488		QUAD LINE DRIVER $\bar{Y} = A \cdot B$															
	DKLD1 (B263)		DUAL LINE DRIVER $X = A \cdot B \cdot C \cdot D + E \cdot F$															
RCV	DKLR1 (B261)		TRIPLE LINE RECEIVER $T0 = XS (L0 \cdot 0A + 0B \cdot 0C)$															

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REV/COMP DESCRIPTION(SC) APP

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TYPE	NAME	SYMBOL	FUNCTION																																																																																																																																																																																																				
1 Ω	9602		DUAL RETRIGGERABLE ONE SHOT <table border="1"> <tr><th>OA</th><th>OB</th><th>MR</th><th>TO</th><th>FO</th></tr> <tr><td>0</td><td>↓</td><td>1</td><td>⌊</td><td>⌋</td></tr> <tr><td>↑</td><td>1</td><td>1</td><td>⌊</td><td>⌋</td></tr> <tr><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td></tr> </table>	OA	OB	MR	TO	FO	0	↓	1	⌊	⌋	↑	1	1	⌊	⌋	X	X	0	0	1																																																																																																																																																																																
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CMP	LS85 S85		4 BIT MAGNITUDE COMPARATOR <table border="1"> <tr><th>OA</th><th>OB</th><th>IA</th><th>IB</th><th>2A</th><th>2B</th><th>3A</th><th>3B</th><th>S0</th><th>S2</th><th>S1</th><th>TA</th><th>TC</th><th>TB</th></tr> <tr><td>OA > OB</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>OA < OB</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA > IB</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA < IB</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA = IB</td><td>2A > 2B</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA = IB</td><td>2A < 2B</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA = IB</td><td>2A = 2B</td><td>3A > 3B</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA = IB</td><td>2A = 2B</td><td>3A < 3B</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA = IB</td><td>2A = 2B</td><td>3A = 3B</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA = IB</td><td>2A = 2B</td><td>3A = 3B</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA = IB</td><td>2A = 2B</td><td>3A = 3B</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>OA = OB</td><td>IA = IB</td><td>2A = 2B</td><td>3A = 3B</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>OA = OB</td><td>IA = IB</td><td>2A = 2B</td><td>3A = 3B</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> </table>	OA	OB	IA	IB	2A	2B	3A	3B	S0	S2	S1	TA	TC	TB	OA > OB	X	X	X	X	X	X	X	X	X	X	1	0	0	OA < OB	X	X	X	X	X	X	X	X	X	X	0	1	0	OA = OB	IA > IB	X	X	X	X	X	X	X	X	X	1	0	0	OA = OB	IA < IB	X	X	X	X	X	X	X	X	X	0	1	0	OA = OB	IA = IB	2A > 2B	X	X	X	X	X	X	X	X	1	0	0	OA = OB	IA = IB	2A < 2B	X	X	X	X	X	X	X	X	0	1	0	OA = OB	IA = IB	2A = 2B	3A > 3B	X	X	X	X	X	X	X	1	0	0	OA = OB	IA = IB	2A = 2B	3A < 3B	X	X	X	X	X	X	X	0	1	0	OA = OB	IA = IB	2A = 2B	3A = 3B	1	0	0	1	0	0	0	1	0	0	OA = OB	IA = IB	2A = 2B	3A = 3B	0	1	0	0	1	0	0	0	1	0	OA = OB	IA = IB	2A = 2B	3A = 3B	0	0	1	0	0	1	0	0	0	1	OA = OB	IA = IB	2A = 2B	3A = 3B	1	1	0	0	0	0	0	0	0	0	OA = OB	IA = IB	2A = 2B	3A = 3B	0	0	0	1	1	0	0	1	1	0
OA	OB	IA	IB	2A	2B	3A	3B	S0	S2	S1	TA	TC	TB																																																																																																																																																																																										
OA > OB	X	X	X	X	X	X	X	X	X	X	1	0	0																																																																																																																																																																																										
OA < OB	X	X	X	X	X	X	X	X	X	X	0	1	0																																																																																																																																																																																										
OA = OB	IA > IB	X	X	X	X	X	X	X	X	X	1	0	0																																																																																																																																																																																										
OA = OB	IA < IB	X	X	X	X	X	X	X	X	X	0	1	0																																																																																																																																																																																										
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OA = OB	IA = IB	2A < 2B	X	X	X	X	X	X	X	X	0	1	0																																																																																																																																																																																										
OA = OB	IA = IB	2A = 2B	3A > 3B	X	X	X	X	X	X	X	1	0	0																																																																																																																																																																																										
OA = OB	IA = IB	2A = 2B	3A < 3B	X	X	X	X	X	X	X	0	1	0																																																																																																																																																																																										
OA = OB	IA = IB	2A = 2B	3A = 3B	1	0	0	1	0	0	0	1	0	0																																																																																																																																																																																										
OA = OB	IA = IB	2A = 2B	3A = 3B	0	1	0	0	1	0	0	0	1	0																																																																																																																																																																																										
OA = OB	IA = IB	2A = 2B	3A = 3B	0	0	1	0	0	1	0	0	0	1																																																																																																																																																																																										
OA = OB	IA = IB	2A = 2B	3A = 3B	1	1	0	0	0	0	0	0	0	0																																																																																																																																																																																										
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NEXT SPEC

DRAFT ENG CHK APP ISSUE

大橋 今村

TF1600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

NEC SHT 13/

134-190244-0

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B

REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	—

TYPE	NAME	SYMBOL	FUNCTION
PLA	82S100		<p>FIELD PROGRAMABLE LOGIC ARRAY.</p> <p>It is Bipolar Programmable Logic Arrays, containing 48 Product terms (AND terms), and 8 Sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-High (Fp), or True active-Low (Fp*). The true State of each output function is activated by any logical combination of 16 input variables, or their complements, up to 48 terms.</p>
CPU	D780C-1		<p>8-BIT CPU</p>

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NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	

TF1600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

NEC SHT 14/

134-190244-0

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REV	COMP	DESCRIPTION(SC)	APP
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1	0	1980.5.1	
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TYPE	NAME	SYMBOL	FUNCTION																																																																																
IOP	8212		<p>8-BIT I/O PORT</p> <table border="1"> <thead> <tr> <th>MR</th> <th>SB</th> <th>MO</th> <th>EO·EI</th> <th>T0 ~ T7</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>3-STATE</td> </tr> <tr> <td>1</td> <td>X</td> <td>1</td> <td>0</td> <td>Data Latch</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Data Latch</td> </tr> <tr> <td>0</td> <td>X</td> <td>1</td> <td>0</td> <td>RESET</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>RESET</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>1</td> <td>DATA IN</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>DATA IN</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>MR</th> <th>EO·EI</th> <th>SB</th> <th>*SR</th> <th>IT</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>X</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>X</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>X</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>HOLD</td> <td>HOLD</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>HOLD</td> <td>HOLD</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>*SR: INTERNAL SR FLIP FLOP (Q)</p>	MR	SB	MO	EO·EI	T0 ~ T7	X	X	0	0	3-STATE	1	X	1	0	Data Latch	1	0	0	1	Data Latch	0	X	1	0	RESET	0	0	0	1	RESET	X	1	0	1	DATA IN	X	X	1	1	DATA IN	MR	EO·EI	SB	*SR	IT	0	0	X	1	1	0	1	X	1	0	1	1	X	1	0	1	0	0	1	1	1	0	0	HOLD	HOLD	1	0	1	HOLD	HOLD	1	0	0	0	0
MR	SB	MO	EO·EI	T0 ~ T7																																																																															
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1	0	1	HOLD	HOLD																																																																															
1	0	0	0	0																																																																															

TYPE	NAME	SYMBOL	FUNCTION
TIM	8253		<p>PROGRAMMABLE INTERVAL TIMER</p>

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	

TF1600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

NEC SHT 15/

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134-190244-0

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REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	—
NEXT SPEC			
DRAFT	ENG	CHK	APP
	大橋		今村
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM			
134-190244-0			
NEC			SHT 16/

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TYPE	NAME	SYMBOL	FUNCTION																																																																																																
P10	8255	<table border="0"> <tr><td>P10</td><td>*D00</td><td>—</td></tr> <tr><td>8255</td><td>*D01</td><td>—</td></tr> <tr><td></td><td>*D02</td><td>—</td></tr> <tr><td></td><td>*D03</td><td>—</td></tr> <tr><td></td><td>*D04</td><td>—</td></tr> <tr><td></td><td>*D05</td><td>—</td></tr> <tr><td></td><td>*D06</td><td>—</td></tr> <tr><td></td><td>*D07</td><td>—</td></tr> <tr><td></td><td>*AP0</td><td>—</td></tr> <tr><td></td><td>*AP1</td><td>—</td></tr> <tr><td></td><td>*AP2</td><td>—</td></tr> <tr><td></td><td>*AP3</td><td>—</td></tr> <tr><td></td><td>*AP4</td><td>—</td></tr> <tr><td></td><td>*AP5</td><td>—</td></tr> <tr><td></td><td>*AP6</td><td>—</td></tr> <tr><td></td><td>*AP7</td><td>—</td></tr> <tr><td></td><td>*CP0</td><td>—</td></tr> <tr><td></td><td>*CP1</td><td>—</td></tr> <tr><td></td><td>*CP2</td><td>—</td></tr> <tr><td></td><td>*CP3</td><td>—</td></tr> <tr><td></td><td>*CP4</td><td>—</td></tr> <tr><td></td><td>*CP5</td><td>—</td></tr> <tr><td></td><td>*CP6</td><td>—</td></tr> <tr><td></td><td>*CP7</td><td>—</td></tr> <tr><td>—</td><td>A01</td><td>*BP0</td></tr> <tr><td>—</td><td>A11</td><td>*BP1</td></tr> <tr><td>○</td><td>R00</td><td>*BP2</td></tr> <tr><td>○</td><td>WR0</td><td>*BP3</td></tr> <tr><td>○</td><td>CS0</td><td>*BP4</td></tr> <tr><td>—</td><td>MR1</td><td>*BP5</td></tr> <tr><td></td><td></td><td>*BP6</td></tr> <tr><td></td><td></td><td>*BP7</td></tr> </table>	P10	*D00	—	8255	*D01	—		*D02	—		*D03	—		*D04	—		*D05	—		*D06	—		*D07	—		*AP0	—		*AP1	—		*AP2	—		*AP3	—		*AP4	—		*AP5	—		*AP6	—		*AP7	—		*CP0	—		*CP1	—		*CP2	—		*CP3	—		*CP4	—		*CP5	—		*CP6	—		*CP7	—	—	A01	*BP0	—	A11	*BP1	○	R00	*BP2	○	WR0	*BP3	○	CS0	*BP4	—	MR1	*BP5			*BP6			*BP7	PROGRAMMABLE I/O PORT
P10	*D00	—																																																																																																	
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—	MR1	*BP5																																																																																																	
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		*BP7																																																																																																	

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REV	COMP	DESCRIPTION(SC)	APP	
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NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM				
134-190244-0				
NEC			SHT 17/	

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TYPE	NAME	SYMBOL	FUNCTION
DMA	8257	<p>DMA *D00 —</p> <p>8257 *D01 —</p> <p>*D02 —</p> <p>*D03 —</p> <p>*D04 —</p> <p>*D05 —</p> <p>*D06 —</p> <p>*D07 —</p> <p>A00 —</p> <p>A01 —</p> <p>A02 —</p> <p>A03 —</p> <p>*A04 —</p> <p>*A05 —</p> <p>*A06 —</p> <p>*A07 —</p> <p>— DR0 DK0 ○ —</p> <p>— DR1 DK1 ○ —</p> <p>— DR2 DK2 ○ —</p> <p>— DR3 DK3 ○ —</p> <p>— HLD HRQ —</p> <p>— RDY AEN —</p> <p>ADC —</p> <p>TCI —</p> <p>HRK —</p> <p>MMR ○ —</p> <p>MMW ○ —</p> <p>*IOR ○ —</p> <p>*IOW ○ —</p> <p>○ CSO —</p> <p>— CLK —</p> <p>— RST —</p>	PROGRAMMABLE DMA CONTROLLER

134-190244-0

B

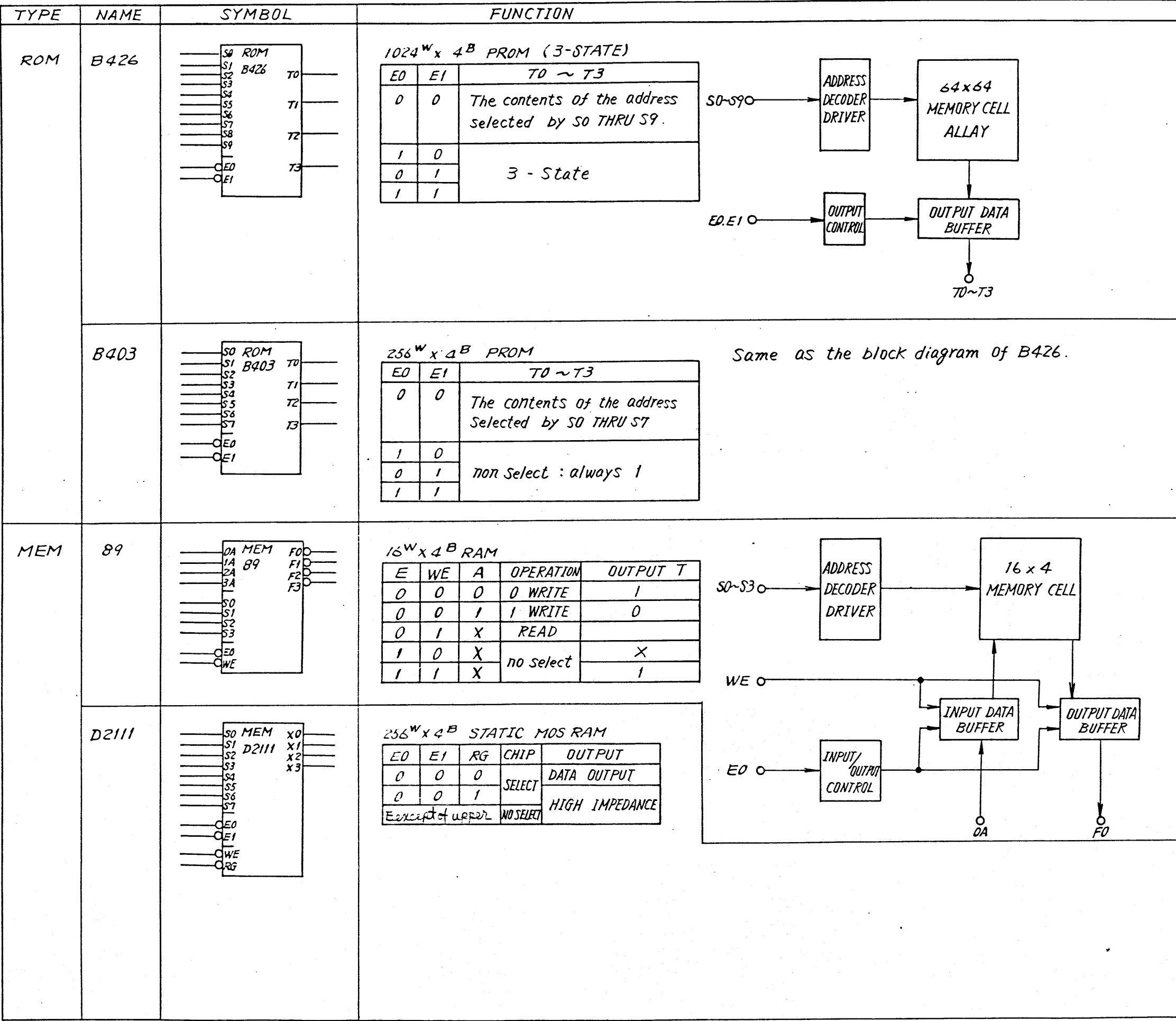
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REV	COMP	DESCRIPTION(SC)	APP
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NEXT SPEC			
DRAFT	ENG	CHK	APP
	大橋		今村
ISSUE			
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM			
134-190244-0			
NEC			SHT 18/



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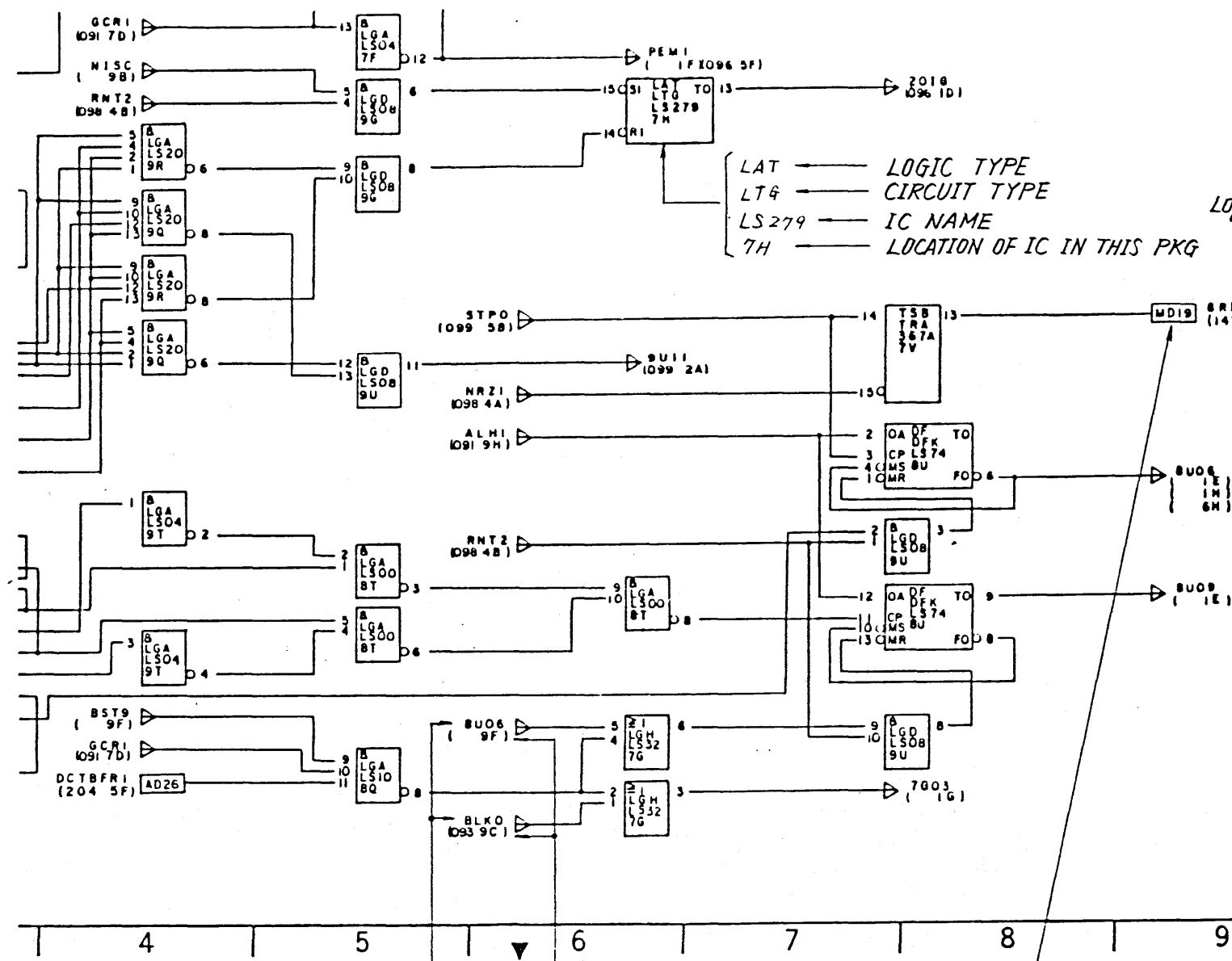
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134-190244-0

2.6 INTRODUCTORY REMARKS OF LOGIC CIRCUIT DRAWING



LAT — LOGIC TYPE
 LT4 — CIRCUIT TYPE
 LS279 — IC NAME
 7H — LOCATION OF IC IN THIS PKG

Logic Tag
 Shows PKG
 Page of the logic circuit drawing

Jumping Tag

Shows where this signals comes from
 ex. 093 9C
 There is source of this signal at the location 9C in the 093 page

PKG PIN NUMBER

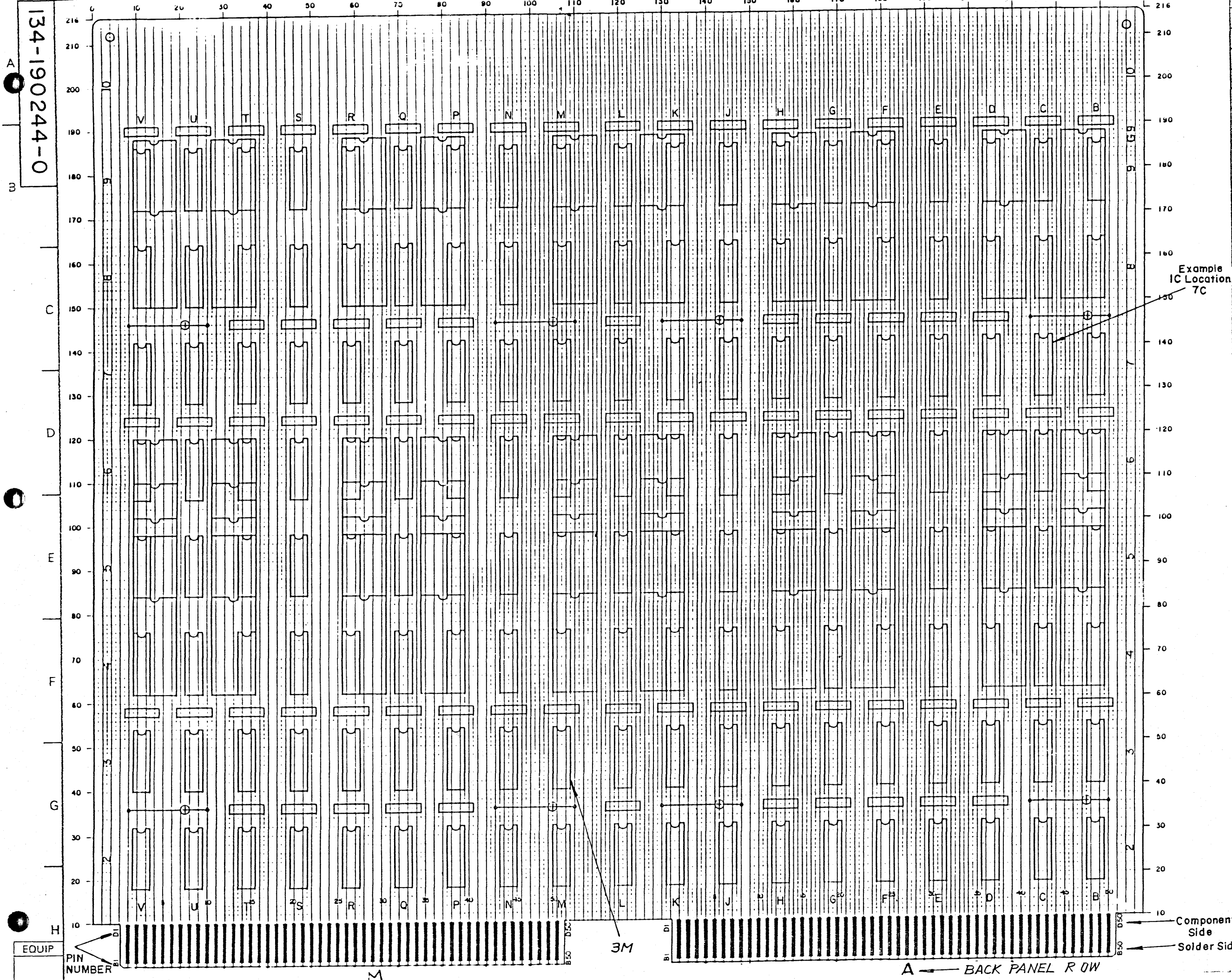
Shows where this signal goes to.
 ex 149 8D
 It shows that this signal is connected with the pin named the same logic tag at the location 8D in the 149 page.

図面略号	GRF
PKG実装位置	
PKG名	G9JAN
092	
設計者	
設計監	羽 友
技術指導	
実装	
承認	今 村
発行	
MTA16X FORMATTER GCR FORMAT CONTROL IN READ 2/9	
134-110229-009	
NEC	SHT 2/

日本電気株式会社

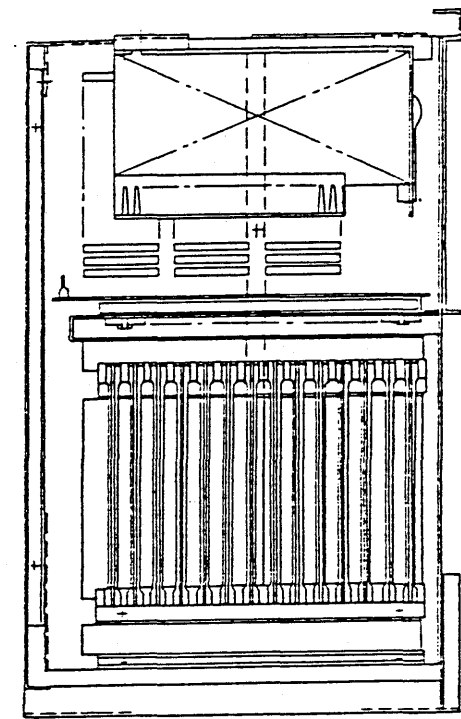
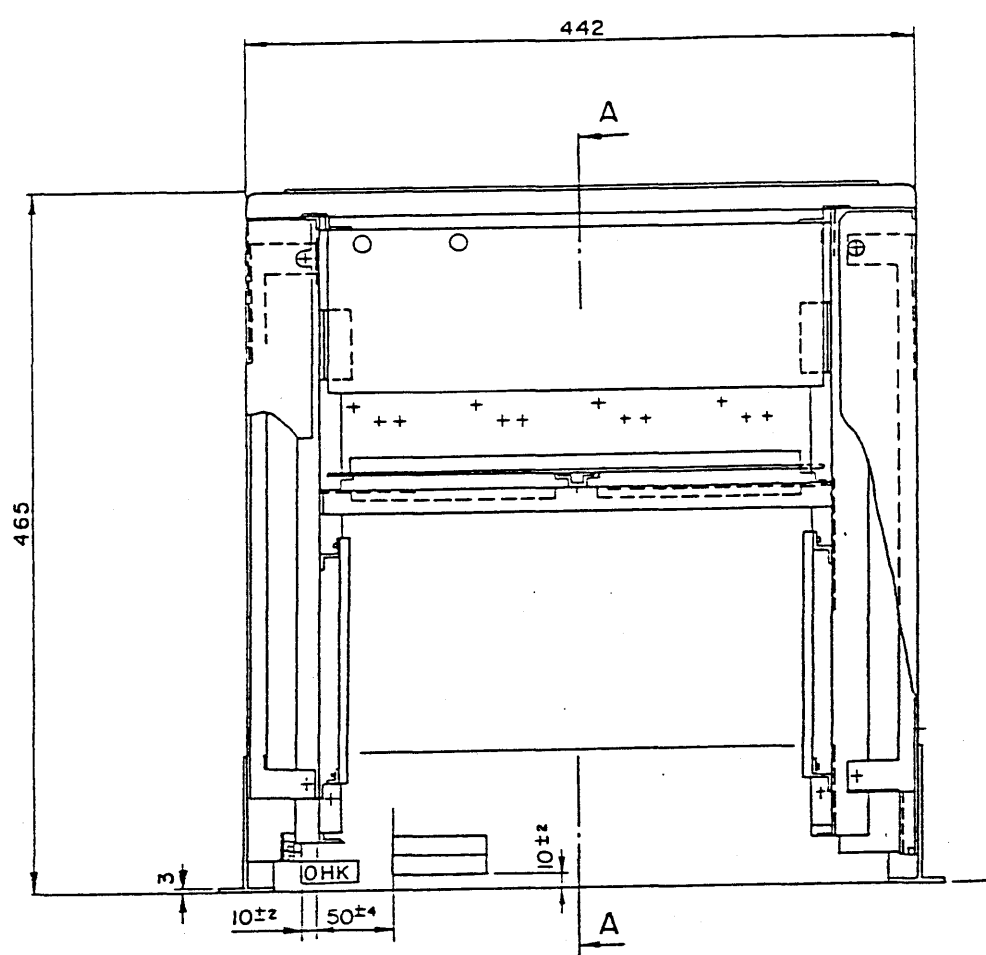
REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	
NEXT SPEC			
DRAFT	ENG	CHK	APP
	大 橋		今 村
TF1600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM			
134-190244-0			
NEC		SHT	19/

134-190244-0

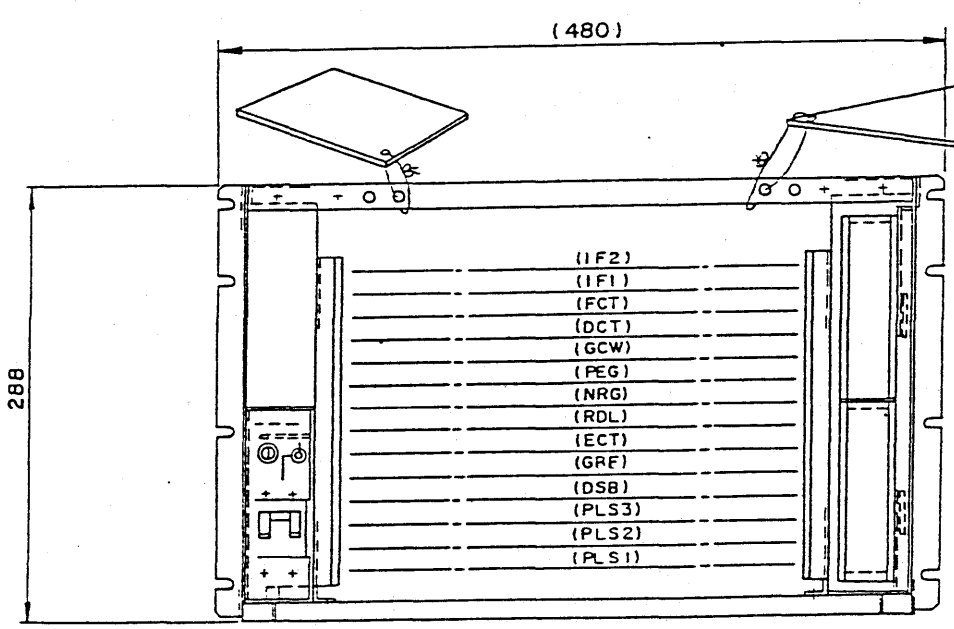


REV	COMP	DESCRIPTION (SC)	APP																																	
1	0	1980.5.1																																		
<table border="1"> <tr> <td>DWG ABBR</td> <td></td> </tr> <tr> <td>PKG LOCATION</td> <td></td> </tr> <tr> <td>PKG NAME</td> <td></td> </tr> <tr> <td>NEXT SPEC</td> <td></td> </tr> <tr> <td>DRAFT</td> <td>ENG</td> <td>CHK</td> <td>APP</td> <td>ISSUE</td> </tr> <tr> <td></td> <td>大橋</td> <td></td> <td>今村</td> <td></td> </tr> <tr> <td colspan="5"> TFI600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM </td> </tr> <tr> <td colspan="4">134-190244-0</td> <td></td> </tr> <tr> <td colspan="4">NEC</td> <td>20/</td> </tr> </table>				DWG ABBR		PKG LOCATION		PKG NAME		NEXT SPEC		DRAFT	ENG	CHK	APP	ISSUE		大橋		今村		TFI600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM					134-190244-0					NEC				20/
DWG ABBR																																				
PKG LOCATION																																				
PKG NAME																																				
NEXT SPEC																																				
DRAFT	ENG	CHK	APP	ISSUE																																
	大橋		今村																																	
TFI600 FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM																																				
134-190244-0																																				
NEC				20/																																

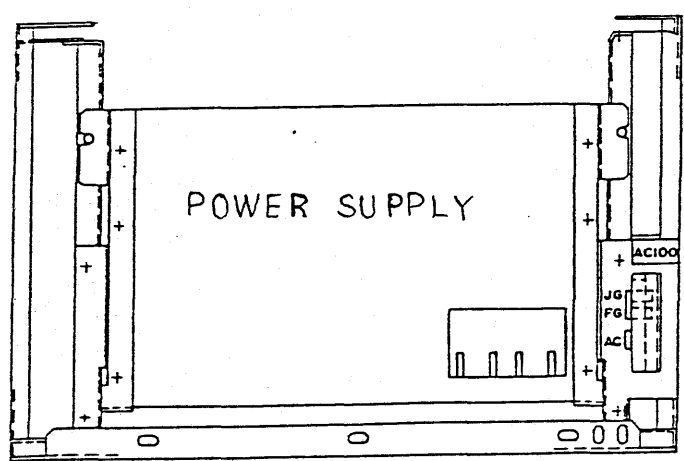
134-190244-0



SECTION A - A



CONSTRUCTION DIAGRAM



BACK

REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	

TF1600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

NEC SHT 21/

134-190244-0

PACKAGE CHECK PIN AND CONNECTOR ASSIGNMENT

The diagram shows a central component with various pins and connectors. The pins are labeled as follows:

- PLS1, PLS2, PLS3
- DSB
- GRF: TP01 3RY1, TP02 RDY1, TP03 DRB1, TP04 RYP1, TP05 RY71, TP06 RY61, TP07 RY51, TP08 RY41, TP09 RY31, TP10 RY21, TP11 RY11, TP12 RY01
- ECT: TP1 DEPO, TP2 DE70, TP3 DE60, TP4 DE50, TP5 DE40, TP6 DE30, TP7 DE20, TP8 DE10, TP9 DE00
- RDL
- NRG: TP1 WSB0, TP2 RWDD, TP3 STB0, TP4 BOF1, TP5 DPE1, TP6 CRE1, TP7 LRE1, TP8 DFM5, TP9 SKE1, TP10 TMD1, TP11 TMD3
- PEG: TP1 WSRO, TP2 WSRO, TP3 WSRO, TP4 WSRO, TP5 WSRO, TP6 WSRO, TP7 WSRO, TP8 WSRO, TP9 CWS0
- GCW: TP1 MG41, TP2 RSYC, TP3 REDC, TP4 CRCC, TP5 ACRC, TP6 PADC, TP7 ENDA, TP8 ENDO, TP9 LES9, TP10 DRO1, TP11 GDW1, TP12 5WP3, TP13 5W73, TP14 5W63, TP15 5W53, TP16 5W43, TP17 5W33, TP18 5W23, TP19 5W13, TP20 5W03
- DCT: TP1 FOP1, TP2 RSB1, TP3 BSR2, TP4 BSA0, TP5 IRDO, TP6 HLTO, TP7 MRDO, TP8 FBY1, TP9 IWTO, TP10 MWTO, TP11 DBY1, TP12 WSB1, TP19 5W13, TP20 5W03
- FCT: P6 MAINTENANCE CONNECTOR (LED1, LED2, LED3, LED4), P4 MT INTERFACE CONNECTOR (DATA), P3 MT INTERFACE CONNECTOR (CMD)
- IF1: P1 DAI INTERFACE CONNECTOR (14S) (DATA), P2 DAI INTERFACE CONNECTOR (CONTROL)
- IF2: P2 ADAPTER INTERFACE CONNECTOR (DATA), P5 ADAPTER INTERFACE CONNECTOR (STATUS), P1 ADAPTER INTERFACE CONNECTOR (CMD)

Sample for Adapter

REVCOMP	DESCRIPTION(SC)	APP
1 0	1980.5.1	

NEXT SPEC			
DRAFT	ENG	CHK	APP
	大橋		今村

TFI600 FORMATTER
INTRODUCTORY
REMARKS
OF CIRCUIT DIAGRAM

134-190244-0

NEC SHT 22/

Nippon Electric Co. Ltd

DC-405E
JIS A3 (297x420)

2

3

4

5

6

1

2

3

4

5

6

7

1 2 3 4 ▲ 5 6 7

134-190244-0

B

C

D

D

E

機名

REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	
NEXT SPEC			
DRAFT	ENG	CHK	APP
	大橋		今村
TF1600A FORMATTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM			
134-190244-0			
NEC			SHT 23/23

A

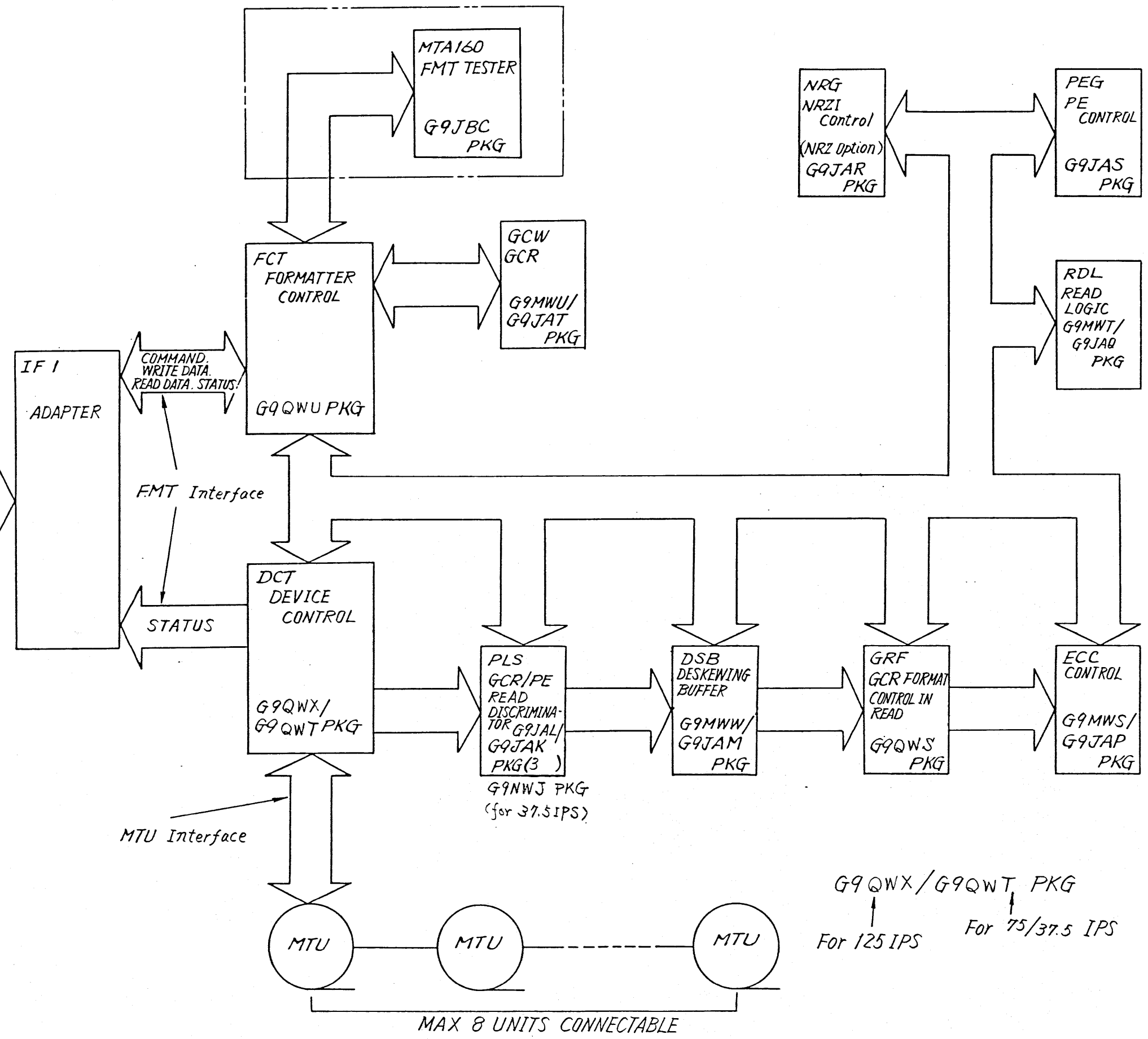
B

C

D

D

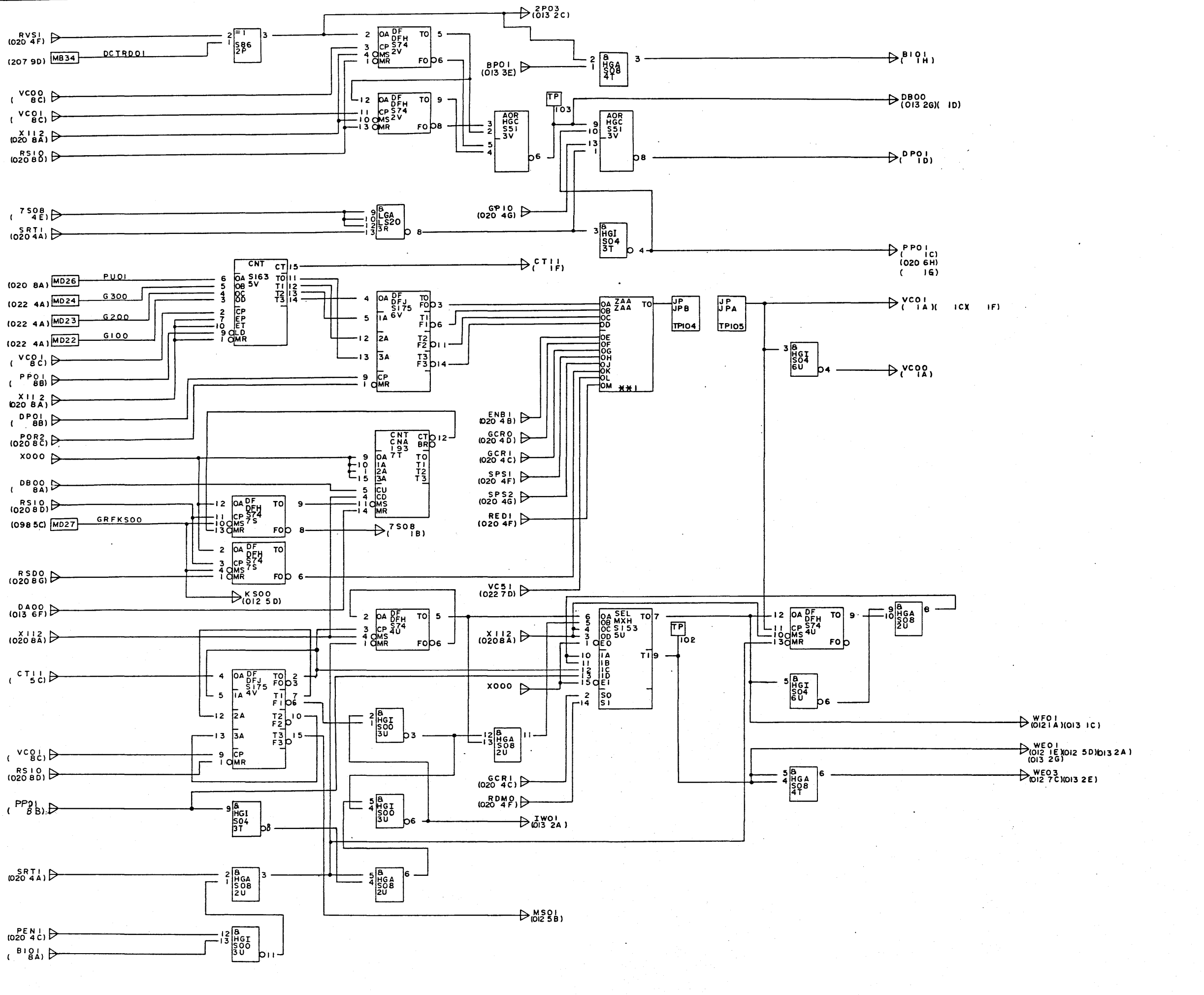
E



TF1600A FORMATTER BLOCK DIAGRAM

134-110229-013-0

A
B
C
D
E
F
G
H



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	
2	0	1981.2.25 SC-41236 山口	大橋
3	0	1981.11.20 SC-413606 山口 英文化による 全面書換	大橋
4	0	1983.3.10 SC-414198 誤記訂正 山口	大橋

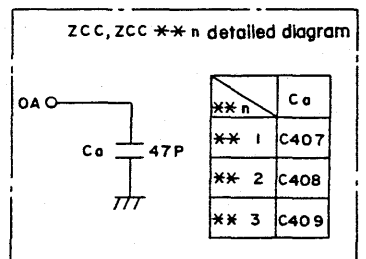
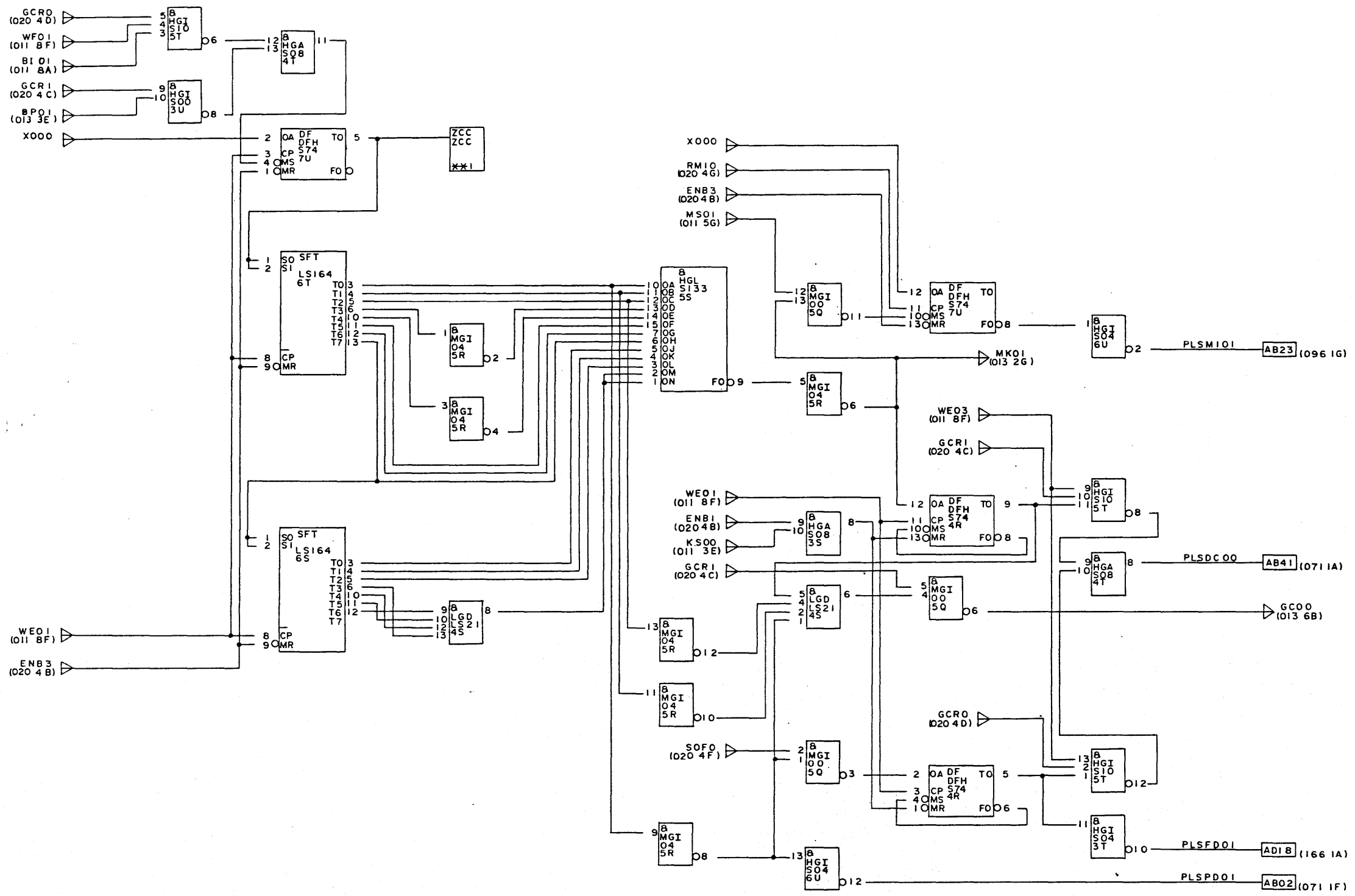
DWG ABBR	PLS I			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
O I I				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	出口		今村	

MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR 1/12
CIRCUIT DIAGRAM
(0,1,2 CH)

134-110229-013-0

NEC SHT 1/12

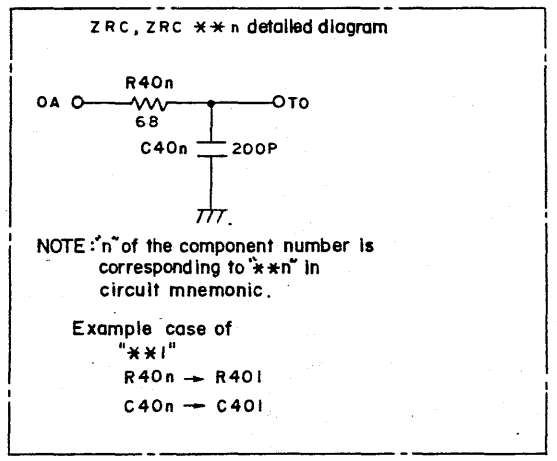
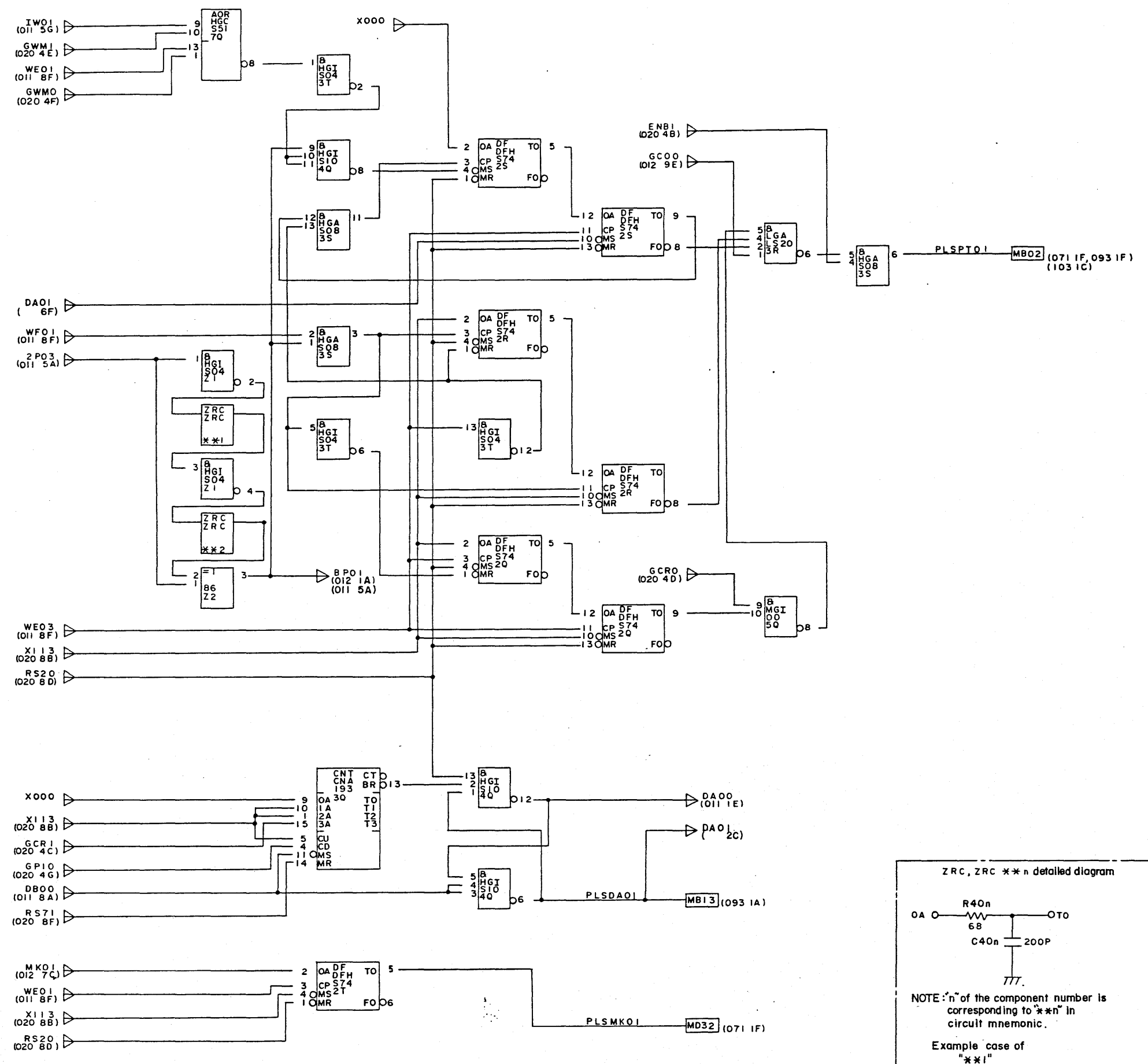
134-110229-013-



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS1			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
012				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR 2/12 CIRCUIT DIAGRAM (0,1,2 CH)				
134-110229-013-				
NEC				SHT 2/

134-110229-013-0



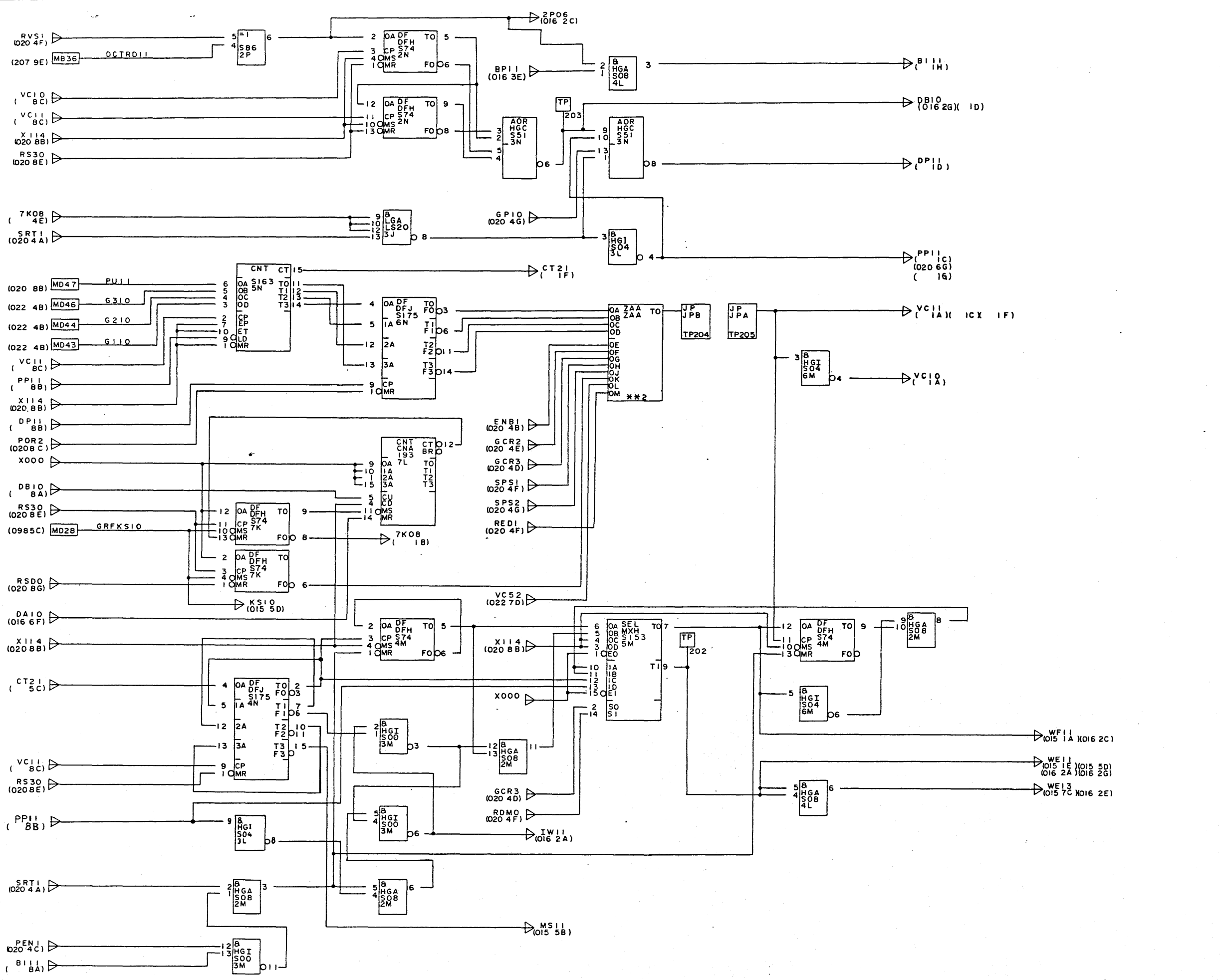
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS I			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
013				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	

MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR 3/12
CIRCUIT DIAGRAM
(0,1,2 CH)

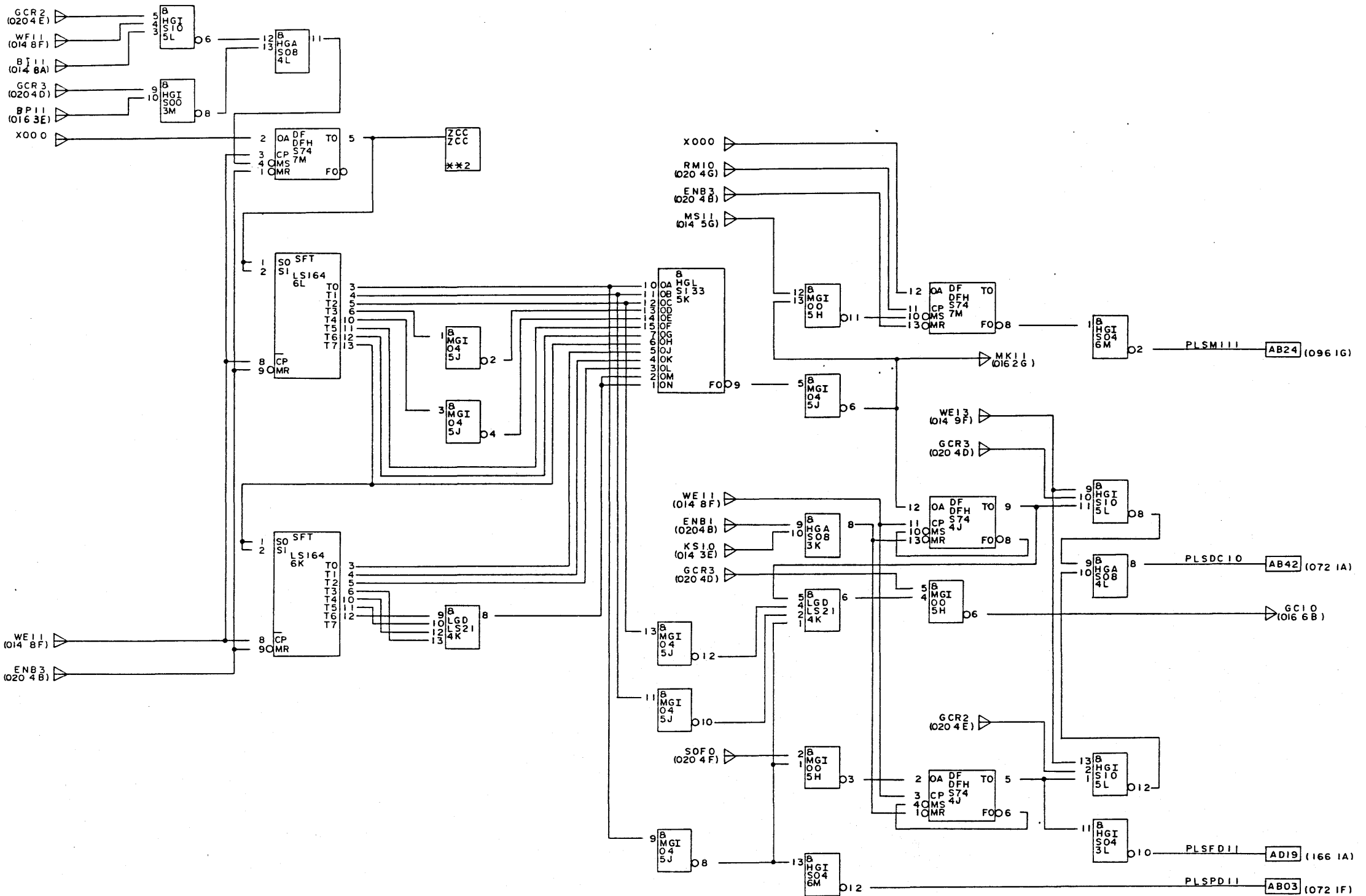
134-110229-013-0
NEC SH 3/

134-110229-013



装置名

134-110229-013



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

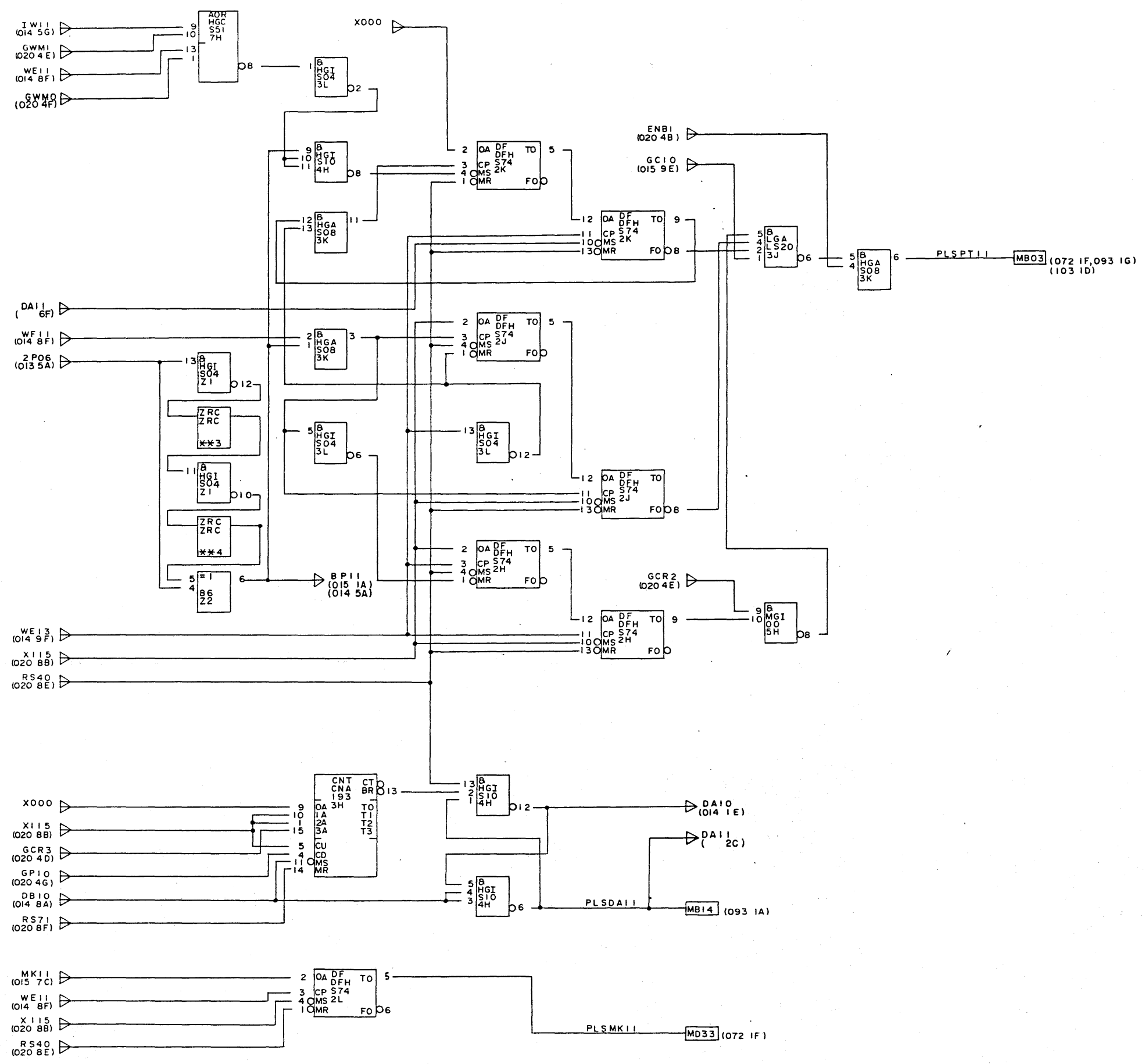
DWG ABBR	PLS I			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
015				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA6X FORMATTER
GCR/PE READ
DISCRIMINATOR 5/12
CIRCUIT DIAGRAM
(0,1,2 CH)

134-110229-013-
NEC SHT 5/

装置名

134-110229-013-0



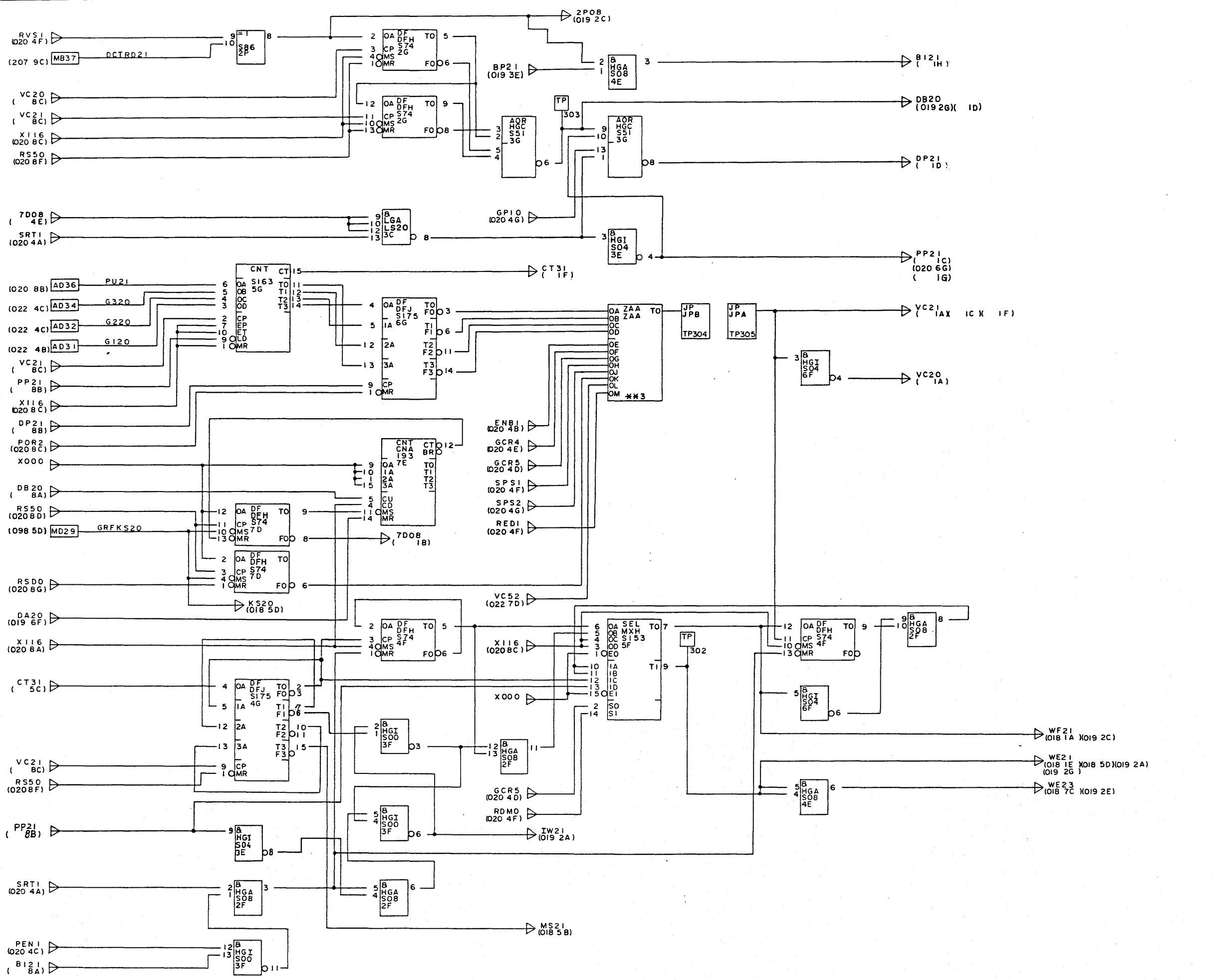
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS I			
PKG LOCATION				
PKG NAME	G9JAK,G9JAL			
016				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER GCR/PE READ DISCRIMINATOR 6/12 CIRCUIT DIAGRAM (0,1,2 CH)				
134-110229-013-0				
NEC				SHT 6/

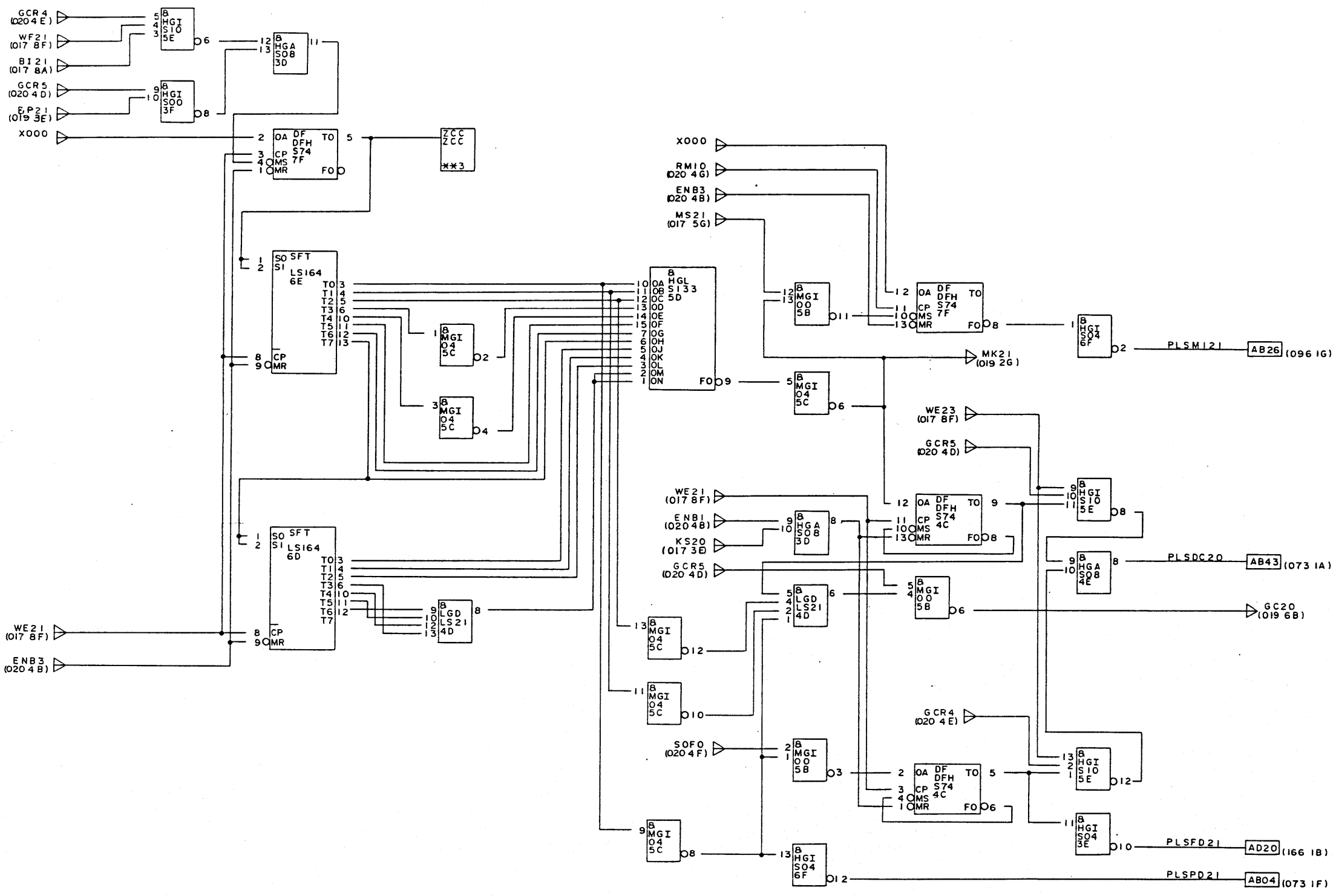
装置名

134-110229-013



装置名

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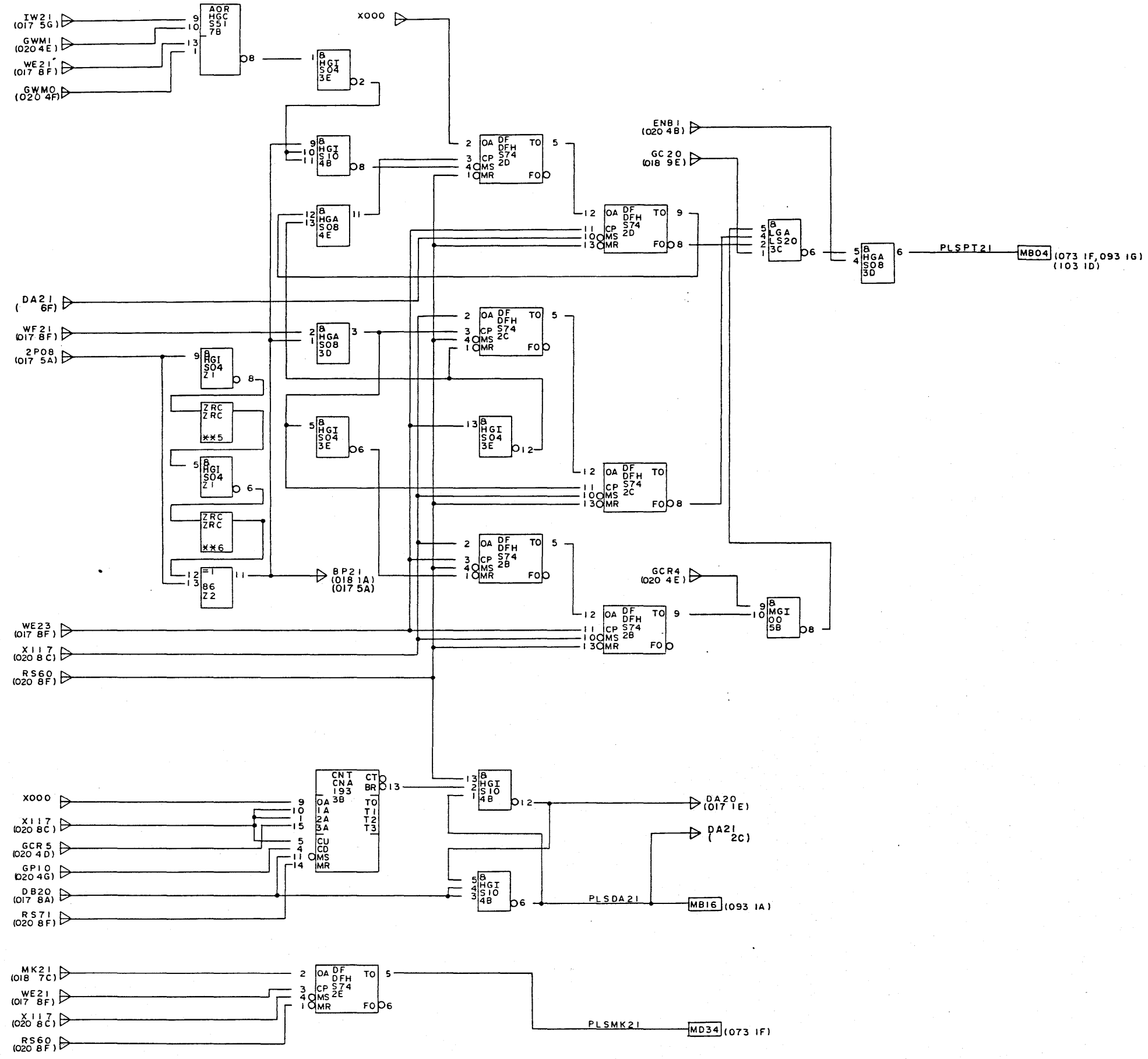


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS I			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
018				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR 8/12 CIRCUIT DIAGRAM (0,1,2 CH)				
134-110229-013-0				
NEC				SHT 8/

装置名

134-110229-013



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS I
PKG LOCATION	
PKG NAME	G9JAK,G9JAL

019

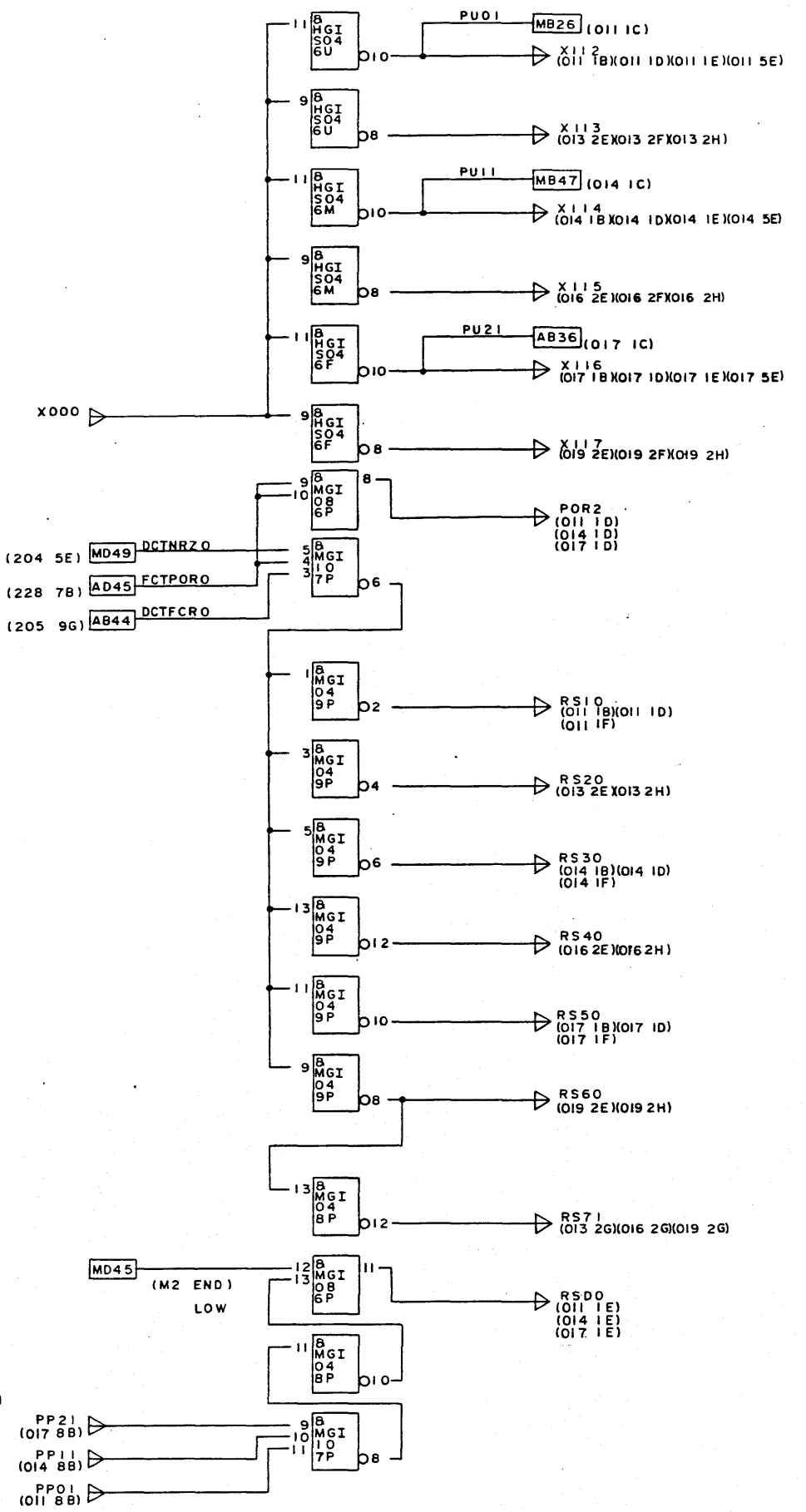
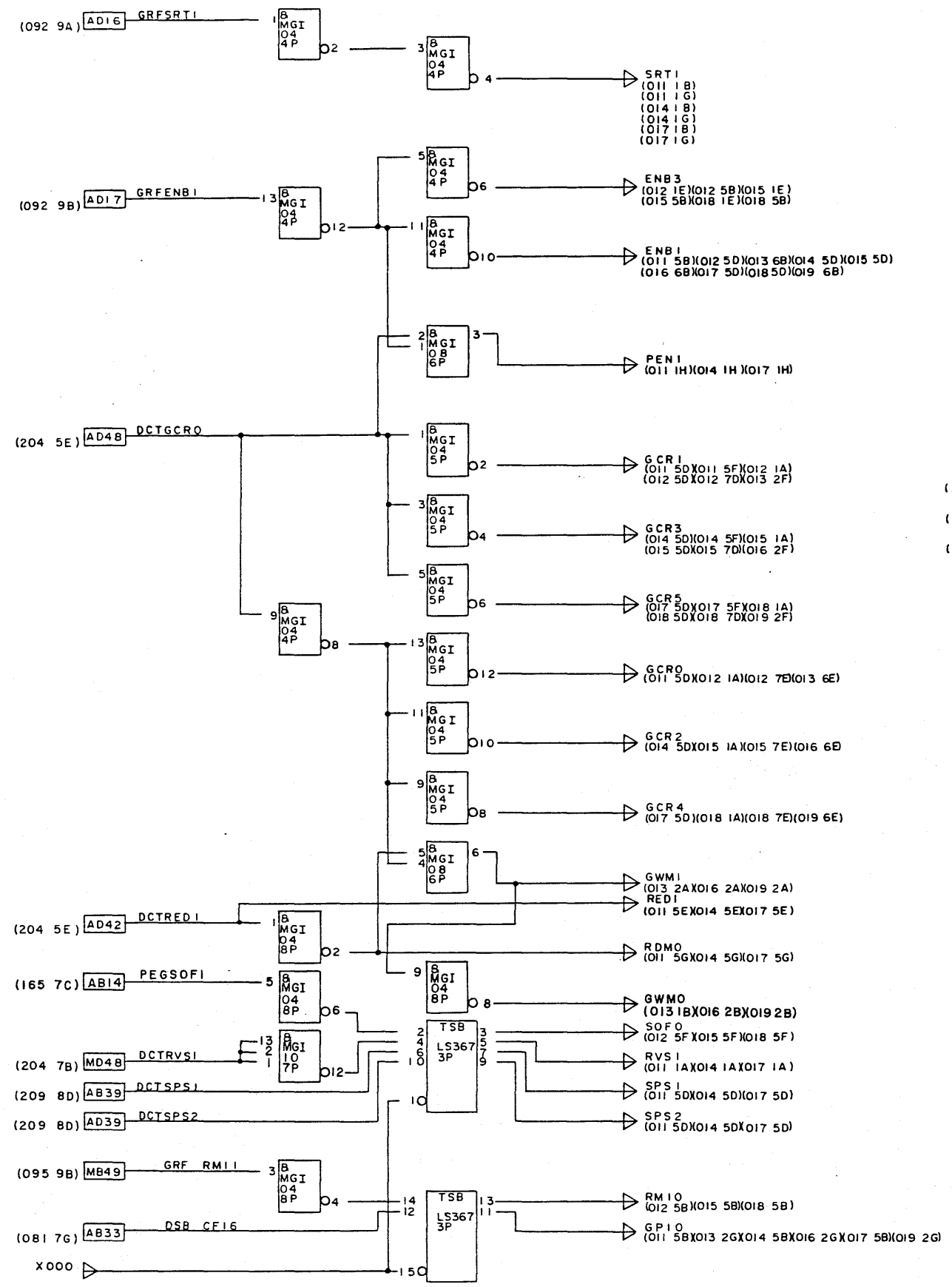
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	

MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR 9/12
CIRCUIT DIAGRAM
(0,1,2 CH)

134-110229-013

NEC SHT 9/

134-110229-013



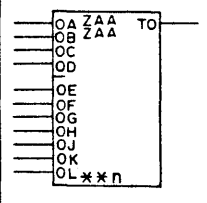
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLSI			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
020				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今村	
	口		村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR ¹⁰ / ₁₂ CIRCUIT DIAGRAM (0,1,2 CH)				
134-110229-013 - 0				
NEC				SHT 10/

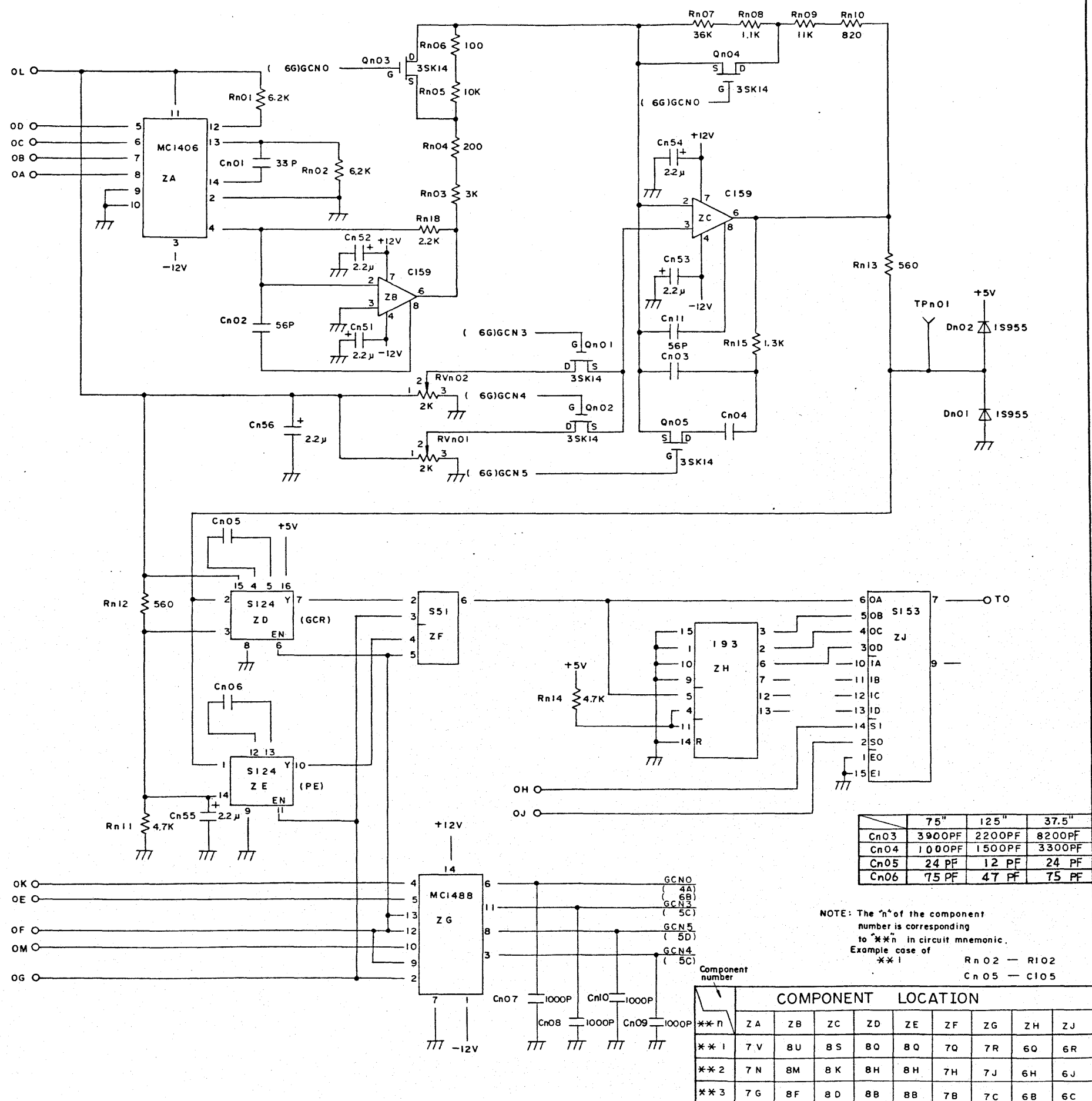
装置名

134-110229-013-0

SYMBOL



DETAILED DIAGRAM



	75"	125"	37.5"
Cn03	3900PF	2200PF	8200PF
Cn04	1000PF	1500PF	3300PF
Cn05	24 PF	12 PF	24 PF
Cn06	75 PF	47 PF	75 PF

NOTE: The "n" of the component number is corresponding to "*"n in circuit mnemonic. Example case of **1 Rn02 - R102 Cn05 - C105

Component number	COMPONENT LOCATION									
**n	ZA	ZB	ZC	ZD	ZE	ZF	ZG	ZH	ZJ	
**1	7V	8U	8S	80	8Q	7Q	7R	6Q	6R	
**2	7N	8M	8K	8H	8H	7H	7J	6H	6J	
**3	7G	8F	8D	8B	8B	7B	7C	6B	6C	

REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	PLS I
PKG LOCATION	
PKG NAME	G9JAK, G9JAL

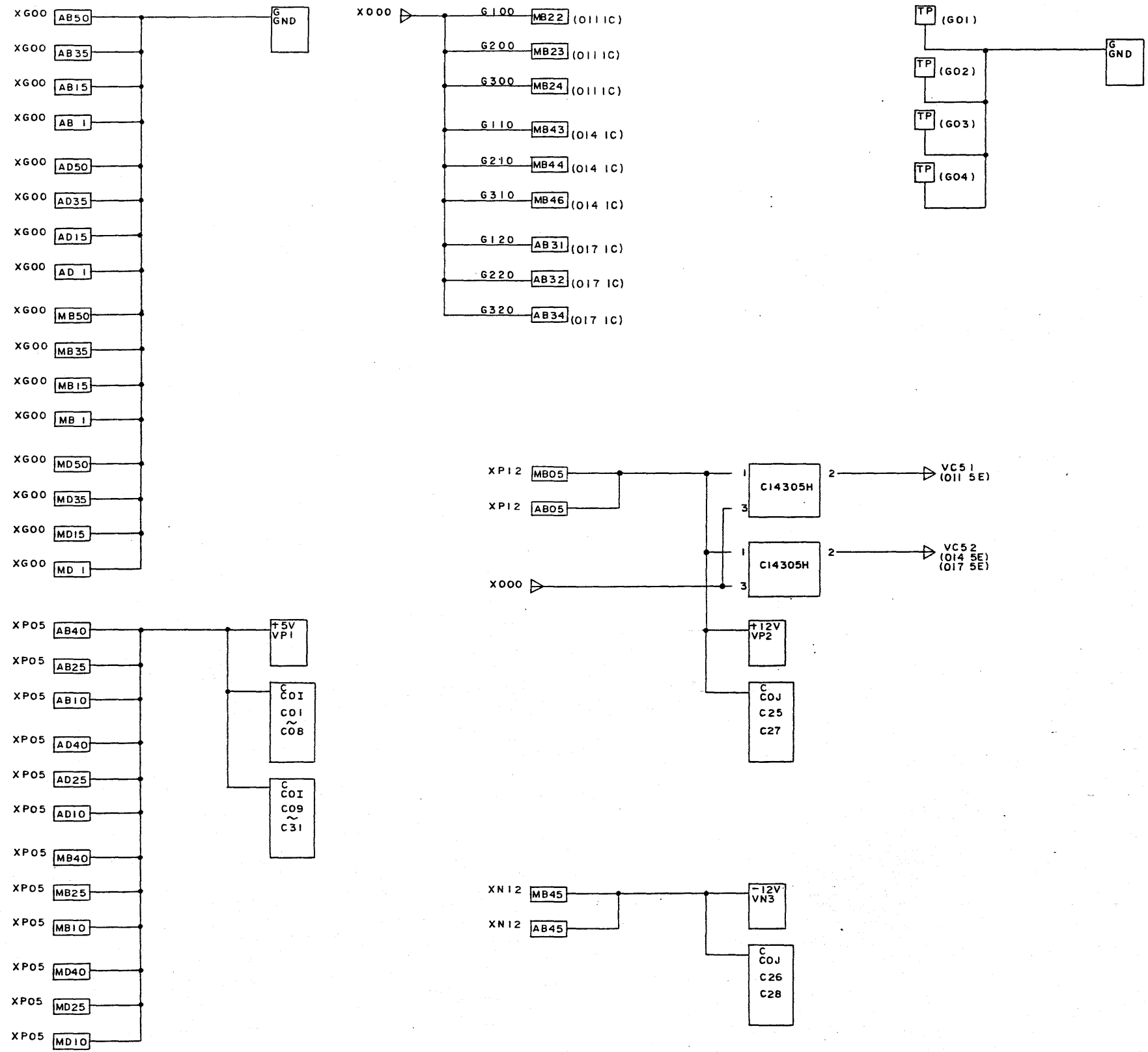
021				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR 1/12
CIRCUIT DIAGRAM
(0,1,2 CH)

134-110229-013-0

NEC SHI II

134-110229-013-0

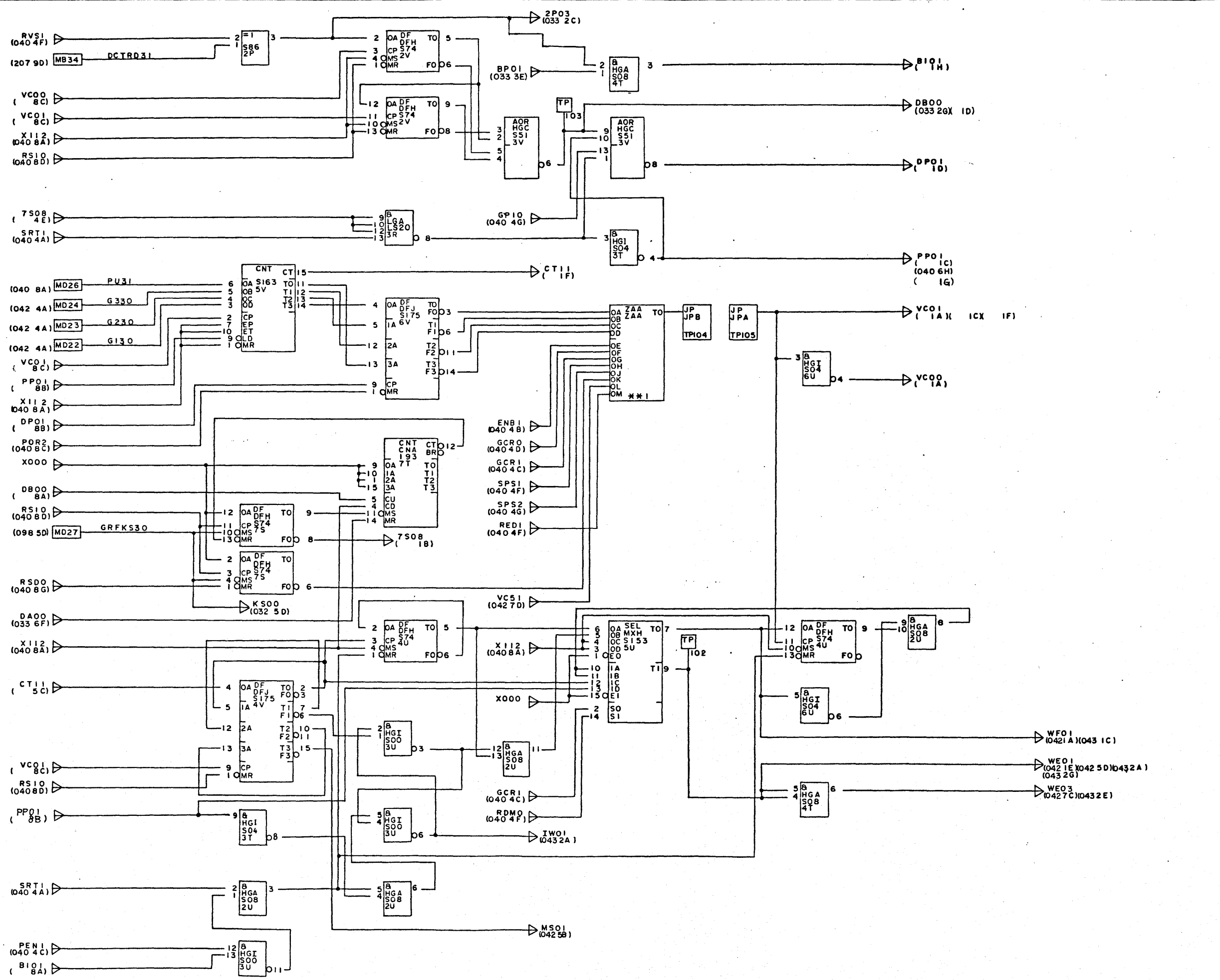


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR		PLS 1		
PKG LOCATION				
PKG NAME		G9JAK, G9JAL		
022				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR 12/12 CIRCUIT DIAGRAM (0, 1, 2 CH)				
134-110229-013-0				
NEC				SHT 12/12

装置名

134-110229-012-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
2	0	1981.2.25 SC-413236 山口	大橋
3	0	1981.11.20 SC-413606 山口 英文化による 全面書換	大橋
4	0	1983.3.10 SC-414196 山口 誤記訂正	大橋

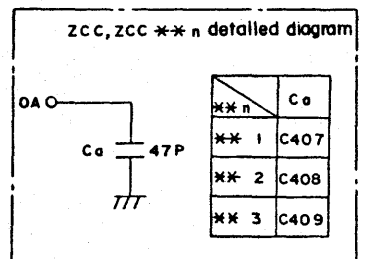
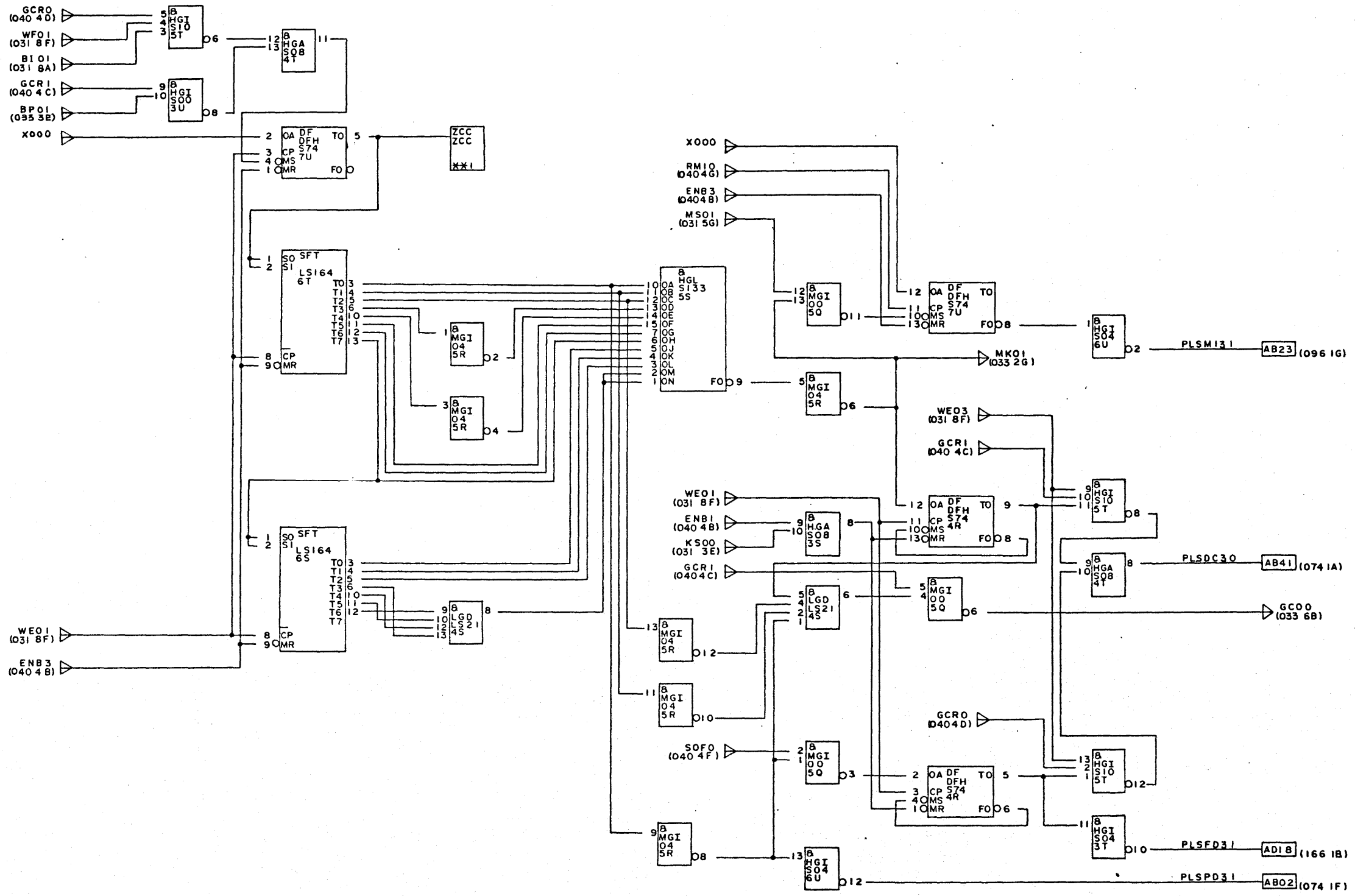
DWG ABBR	PLS 2
PKG LOCATION	
PKG NAME	G9JAK,G9JAL
031	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR
CIRCUIT DIAGRAM 1/12
(3,4,5 CH)

134-110229-012-0
NEC SHT 1/12

134-110229-012-0

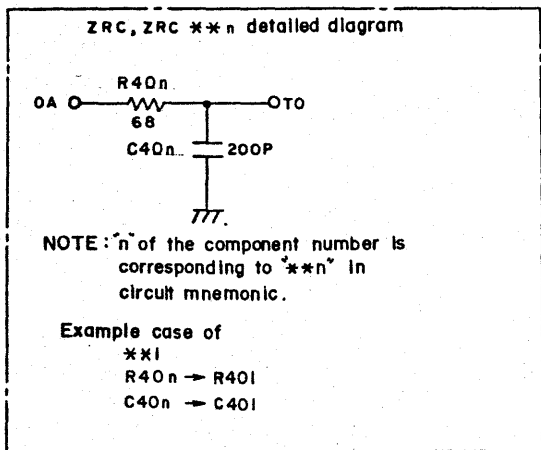
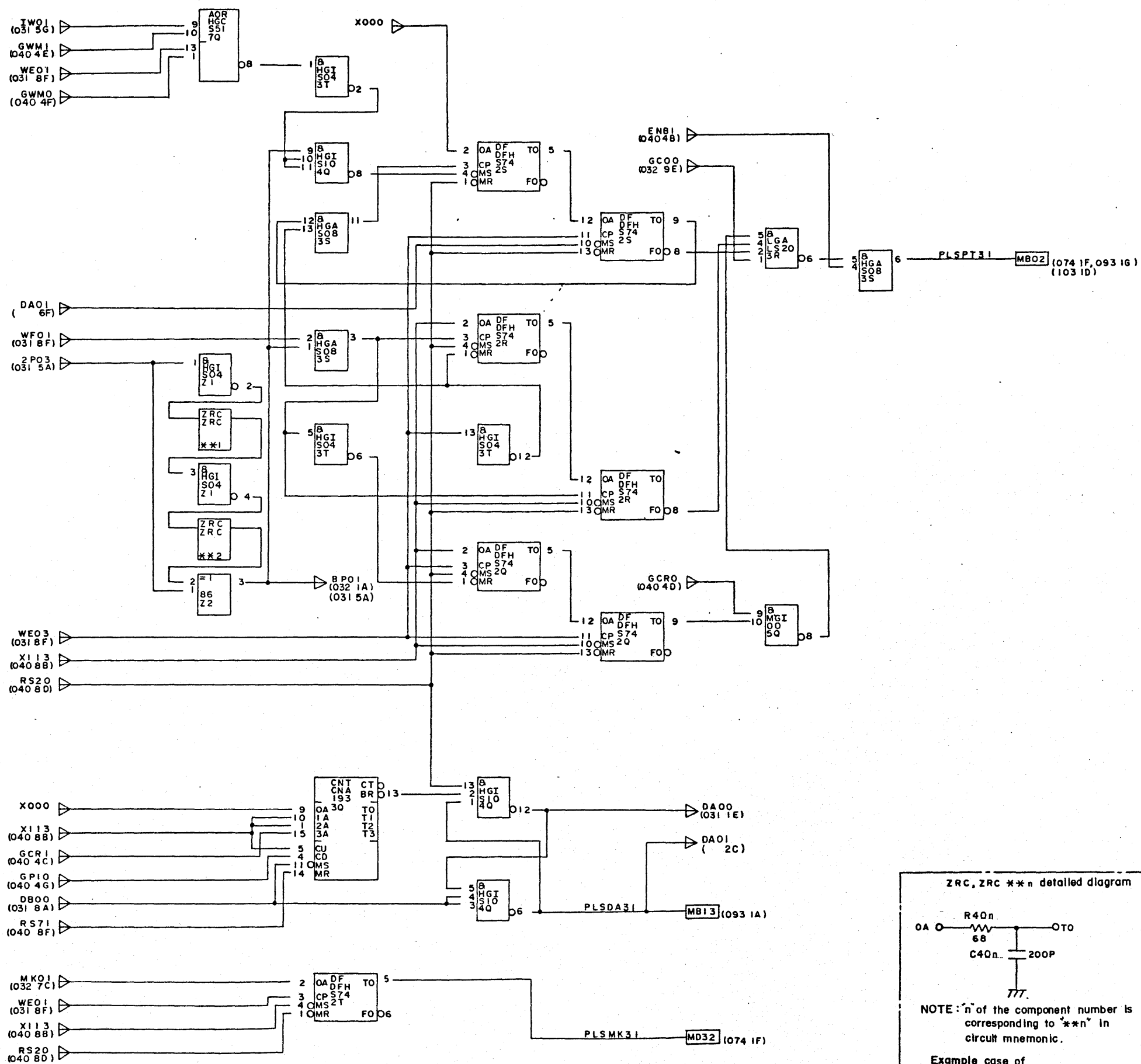


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 2			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
032				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 2/12 (3, 4, 5 CH)				
134-110229-012-0				
NEC				SHT 2/

装置名

134-110229-012-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

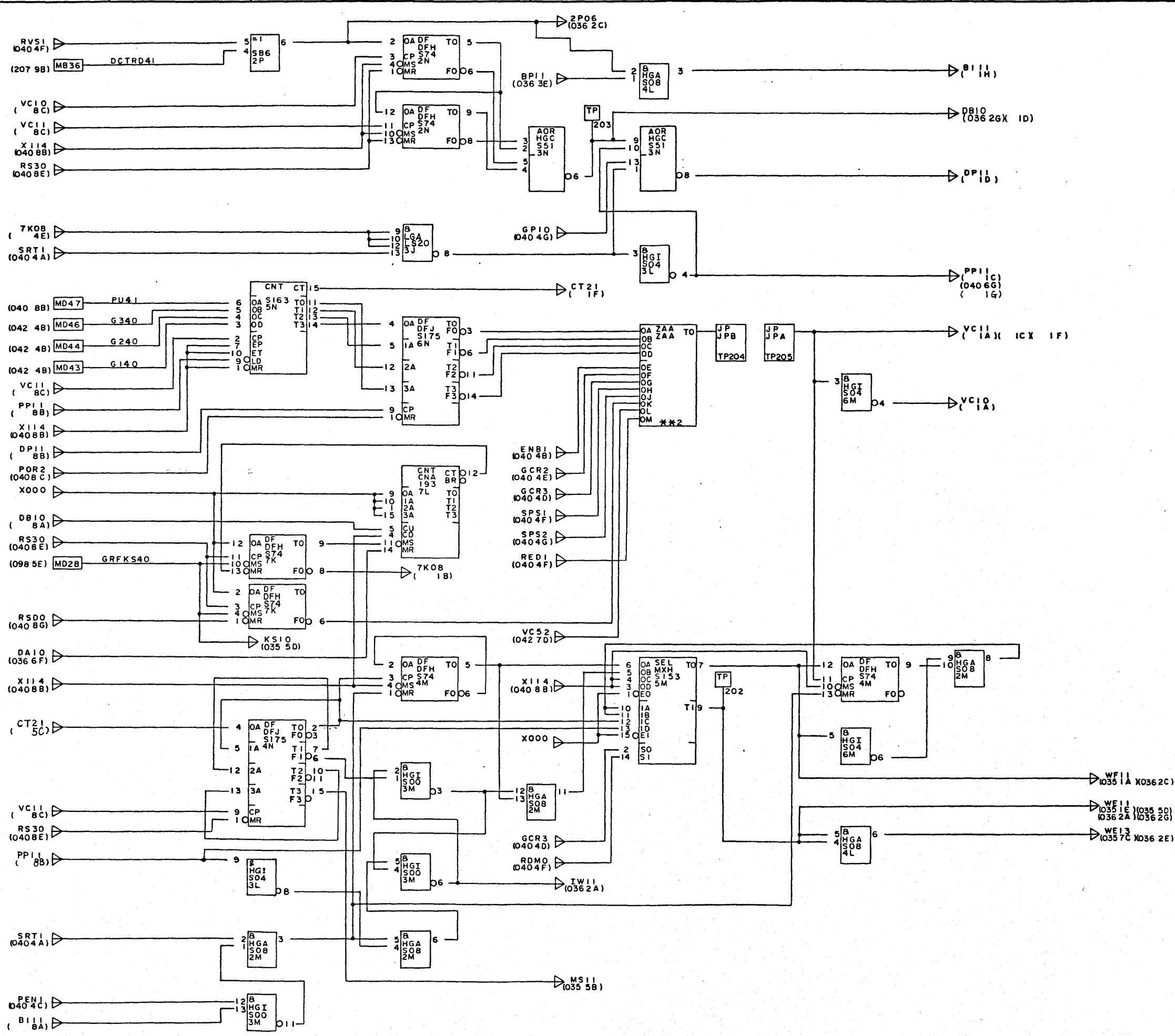
DWG ABBR	PLS 2			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
033				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	

MTA16X FORMATTER
 GCR/PE READ
 DISCRIMINATOR
 CIRCUIT DIAGRAM^{3/12}
 (3,4,5 CH)

134-110229-012-0

NEC SHT 3/

134-110229-012-0



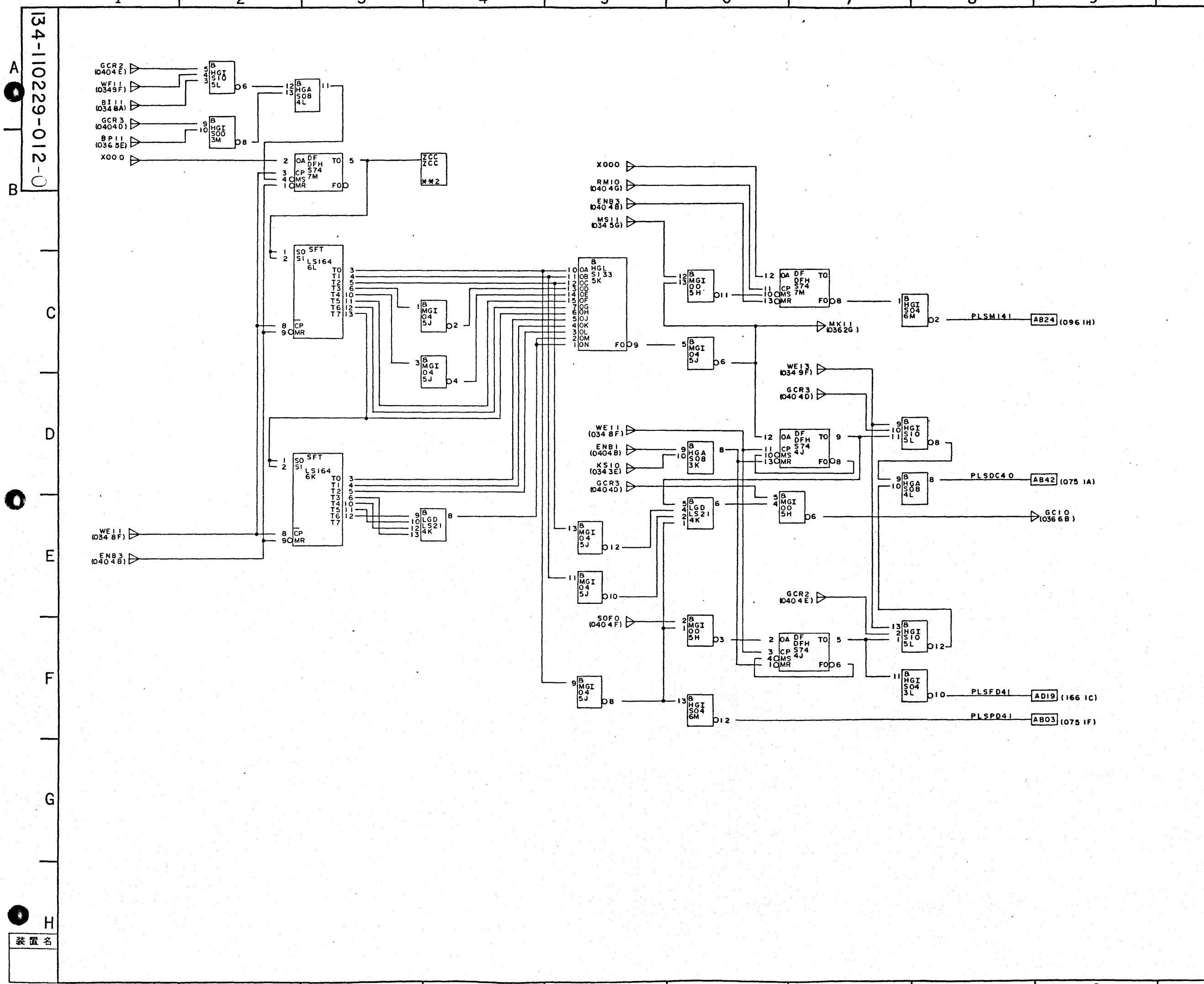
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 2			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
034				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	

**MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR
CIRCUIT DIAGRAM 4¹/₂
(3, 4, 5 CH)**

134-110229-012-0
NEC SHT 4/

装置名

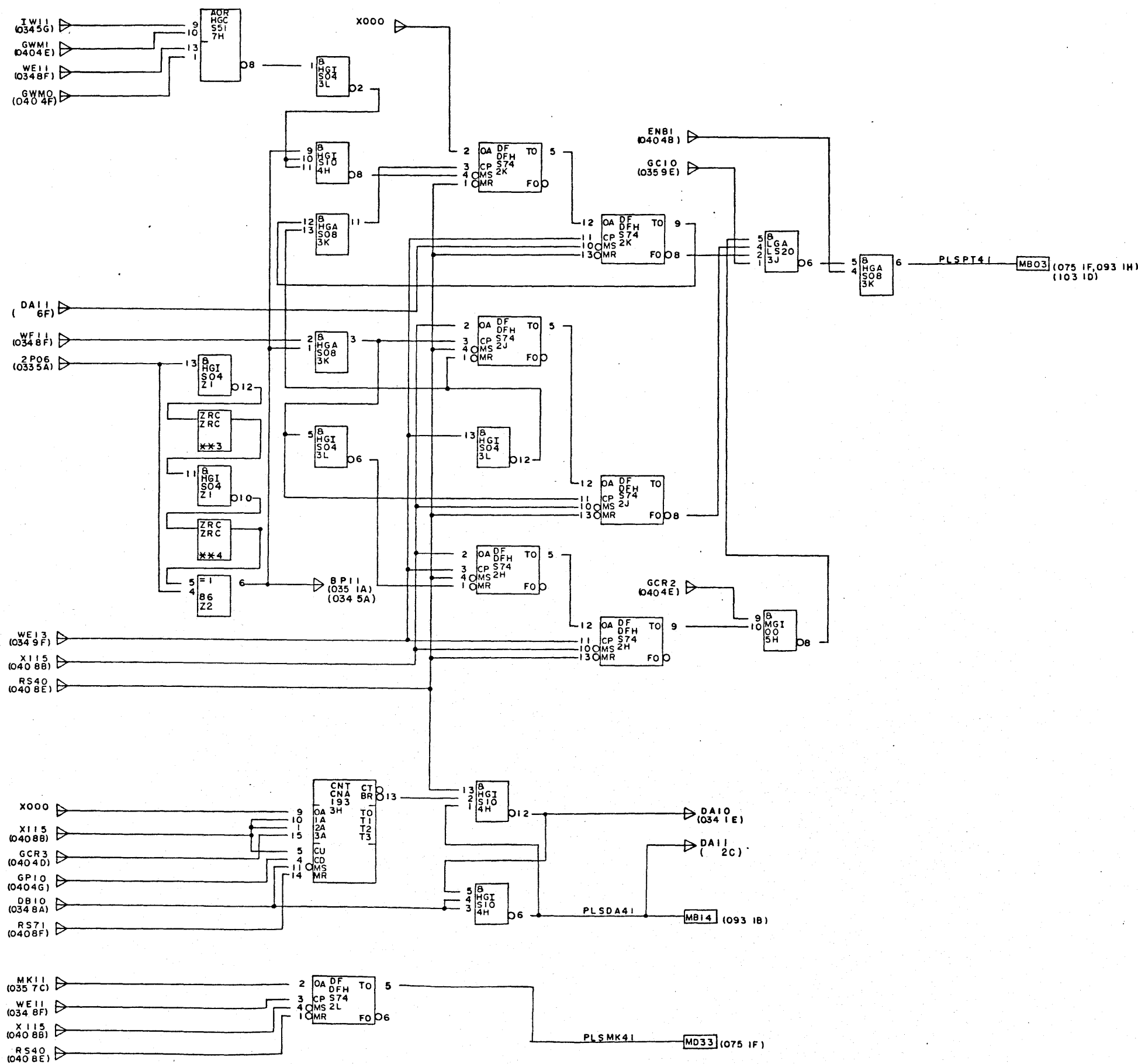


134-110229-012-0

A
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C
D
E
F
G
H

REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	
DWG ABBR		PLS2	
PKG LOCATION			
PKG NAME		G9JAK,G9JAL	
035			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 5/12 (3,4,5 CH)			
134-110229-012-0			
NEC		SHT	5/

134-110229-012-0



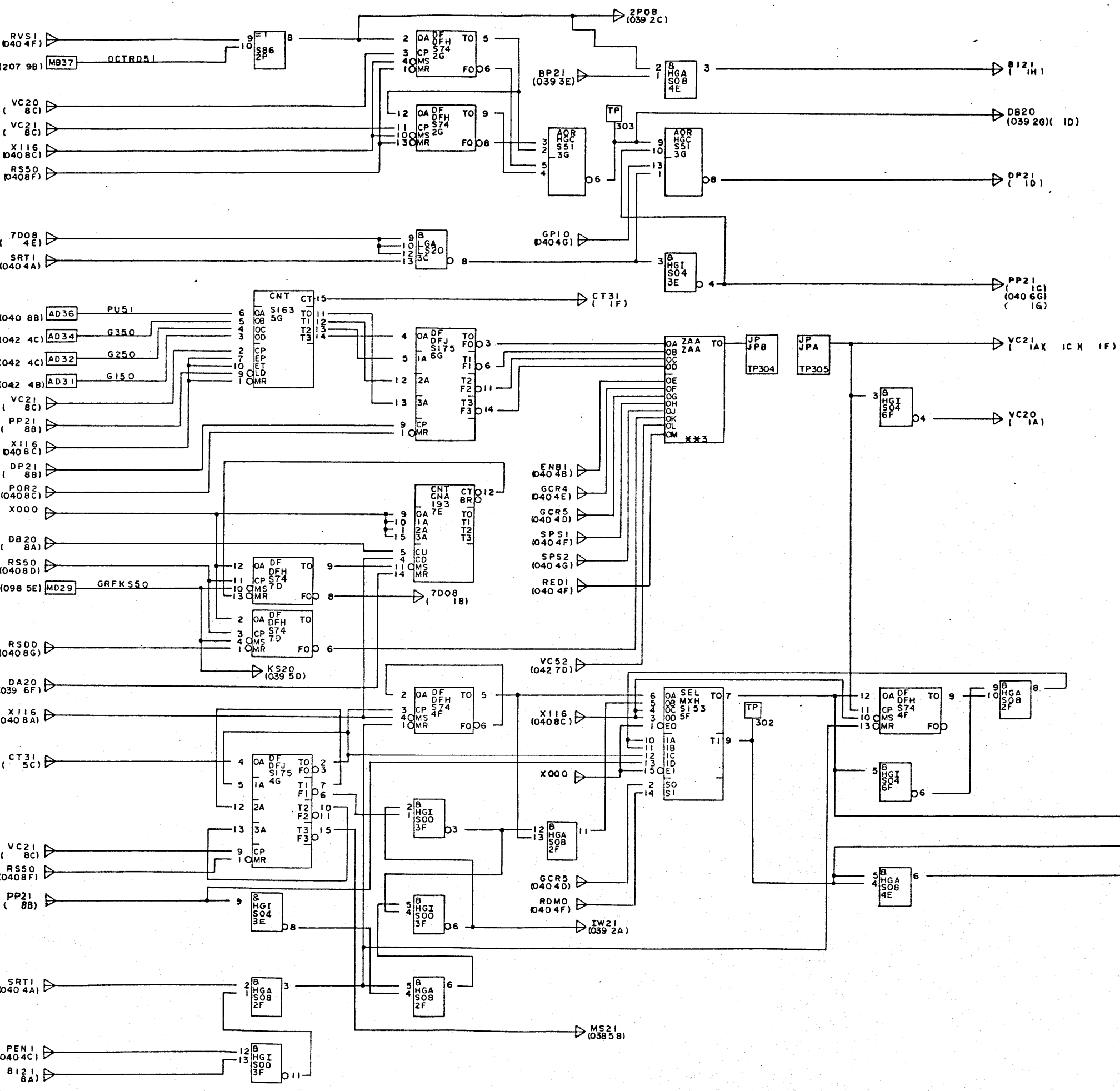
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 2		
PKG LOCATION			
PKG NAME	G9JAK, G9JAL		
036			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
<p style="text-align: center;">MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM^{6/12} (3, 4, 5 CH)</p>			
134-110229-012-0			
NEC			SHT 6/

装置名

134-110229-012-0

A
B
C
D
E
F
G
H



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 2
PKG LOCATION	
PKG NAME	G9JAK,G9JAL

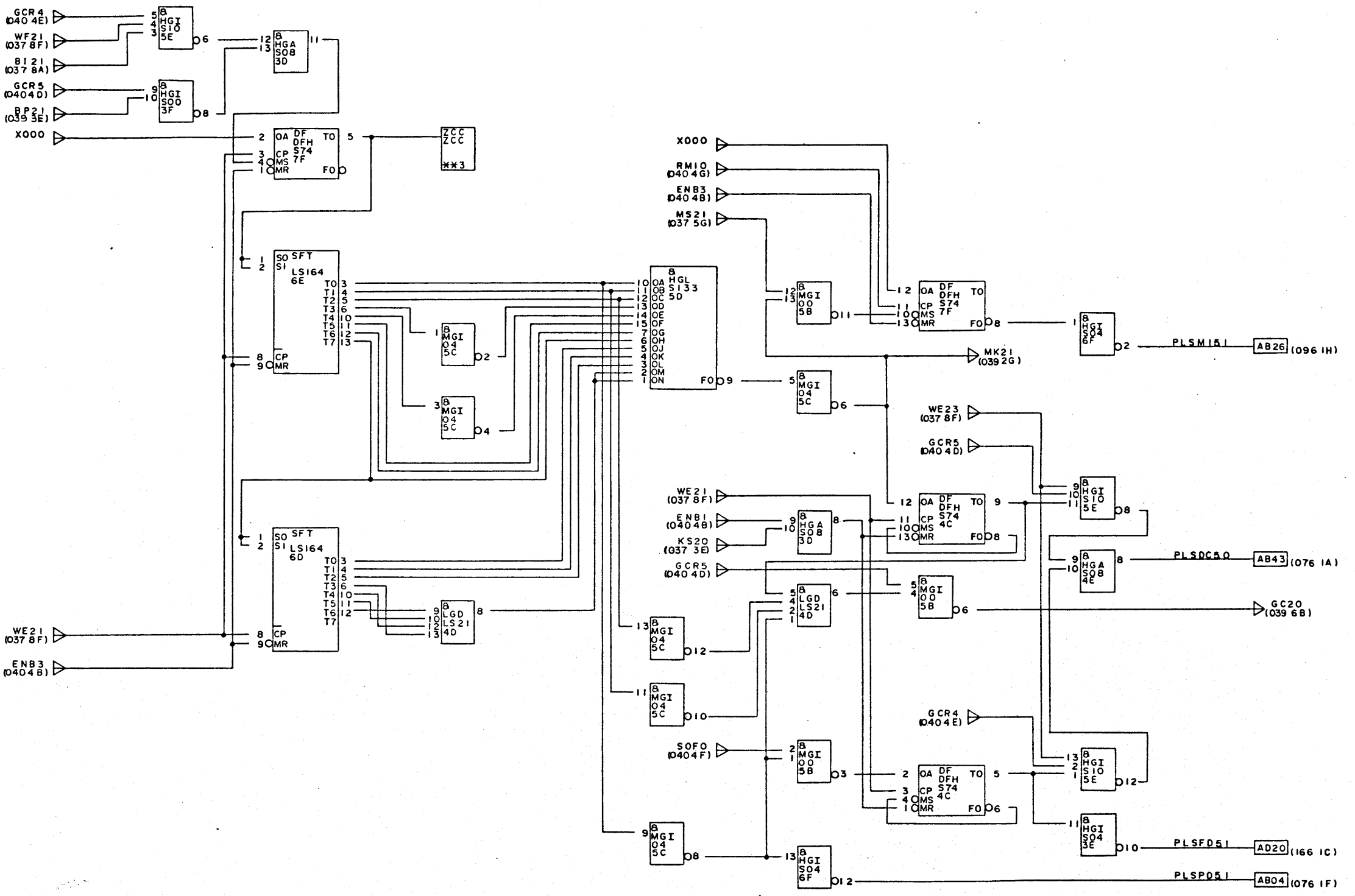
037

NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	

MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR
CIRCUIT DIAGRAM⁷/₁₂
(3,4,5 CH)

134-110229-012-0
NEC SHT 7/

134-110229-012 - C



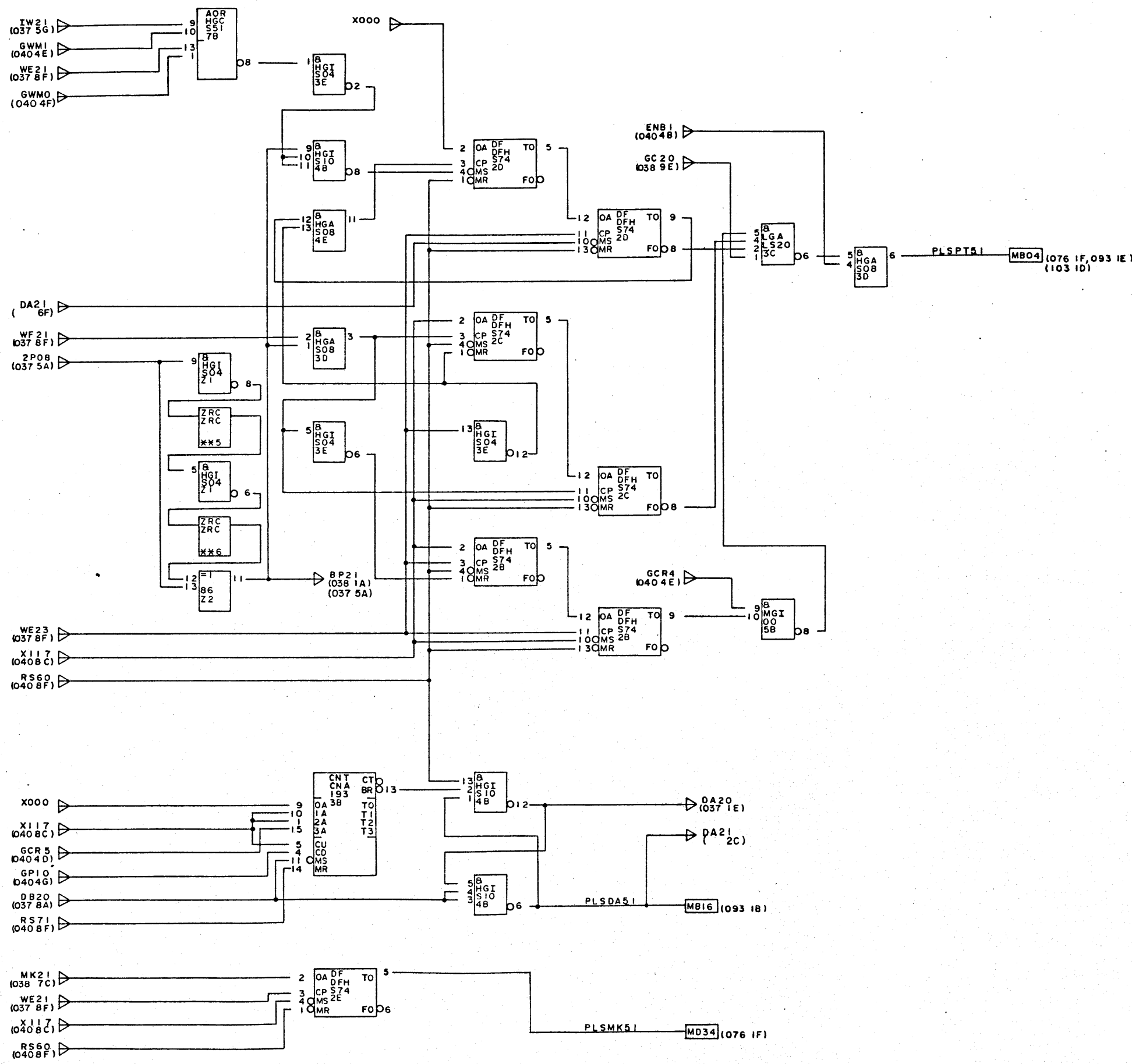
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 2			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
038				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM ⁸ / ₁₂ (3, 4, 5 CH)				
134-110229-012 - C				
NEC				SHT 8/

2515

装置名

134-110229-012-0

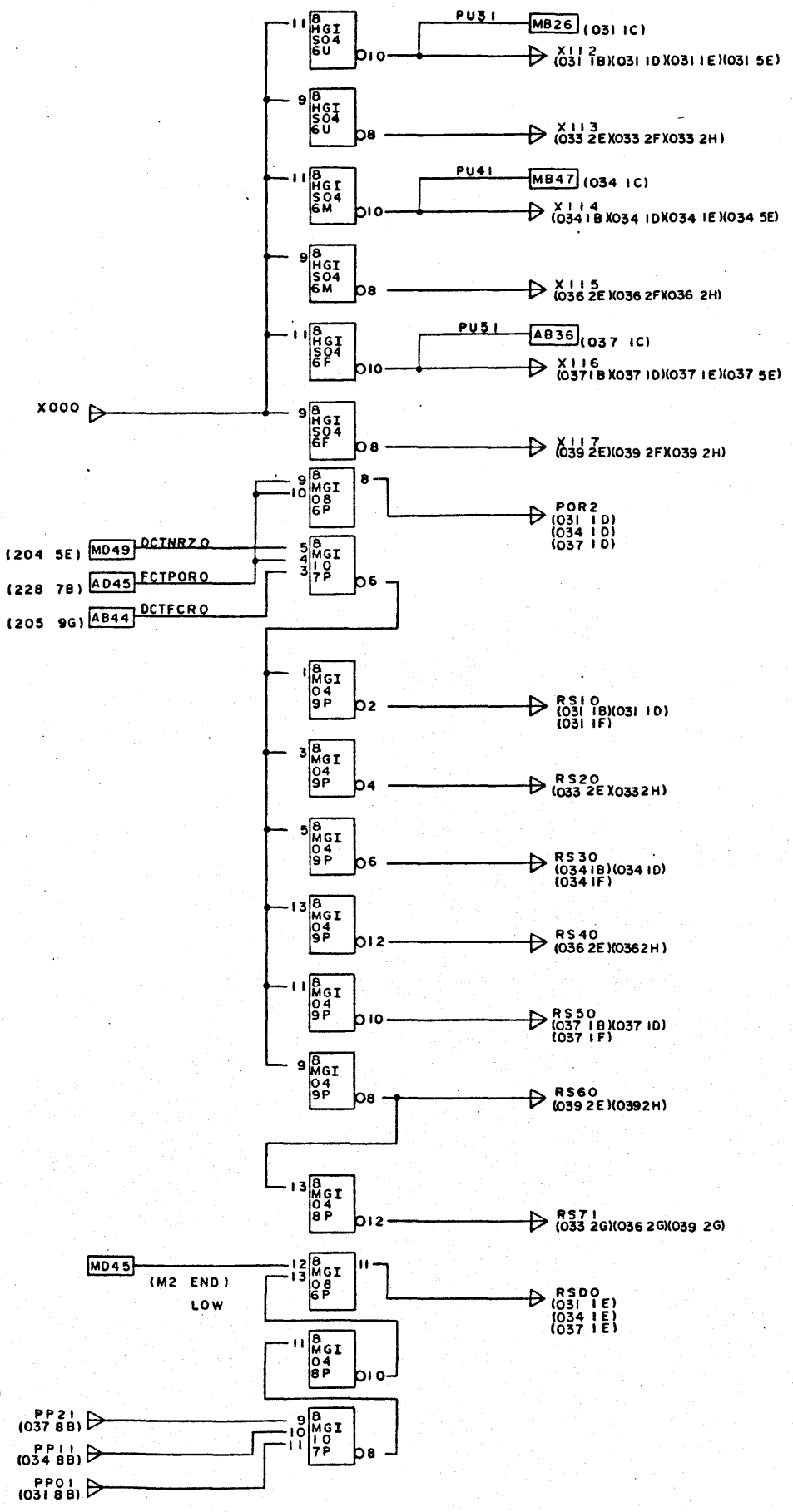
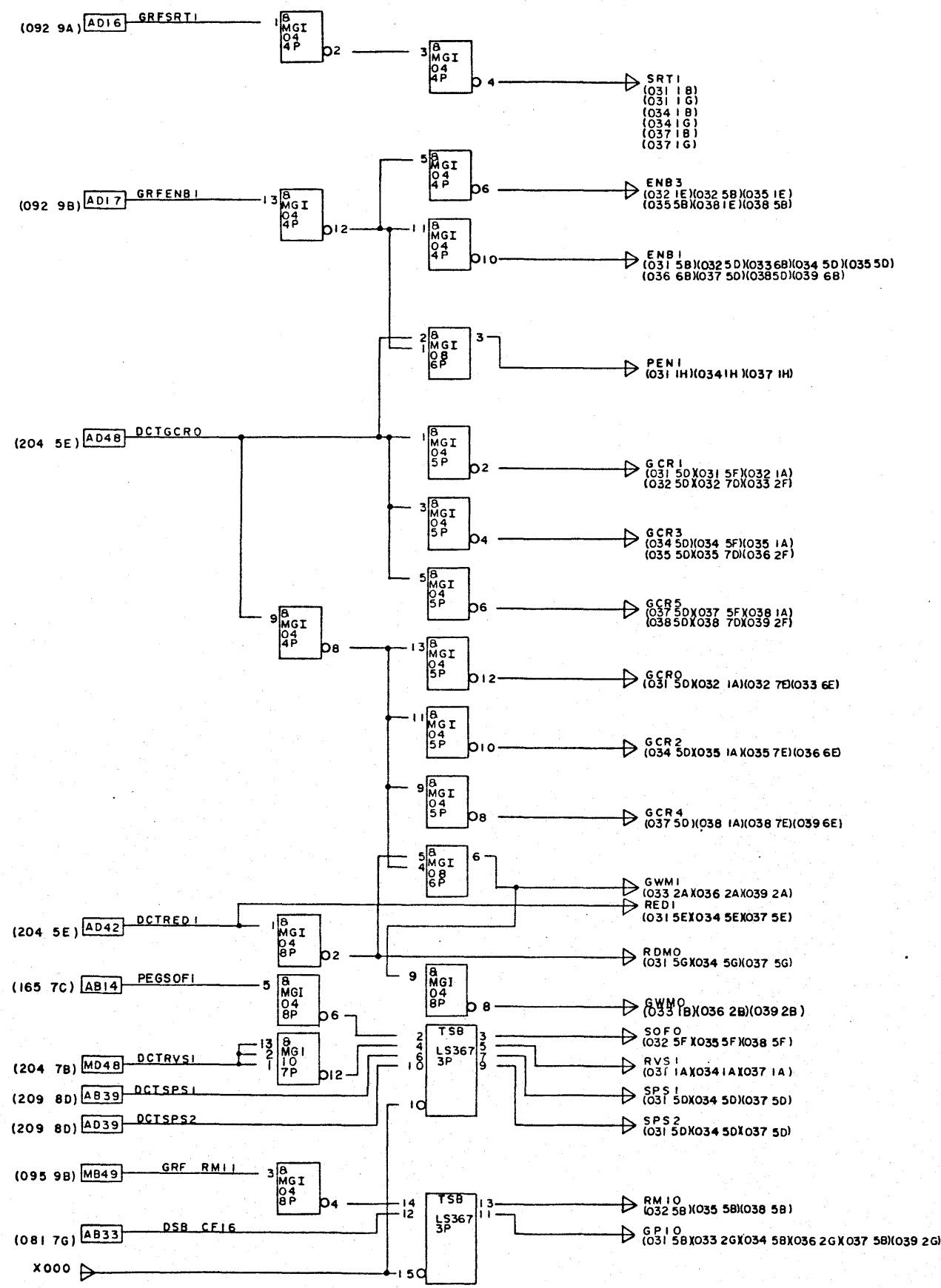


REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 2		
PKG LOCATION			
PKG NAME	G9JAK, G9JAL		
0.39			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM^{9/12} (3, 4, 5 CH)			
134-110229-012-0			
NEC			SHT 9/

装置名

134-110229-012-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

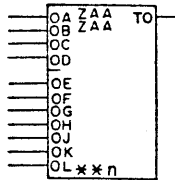
DWG ABBR	PLS 2			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
040				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	川		村	

MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM^{10,12} (3, 4, 5 CH)	
134-110229-012-0	
NEC	SHT 10/

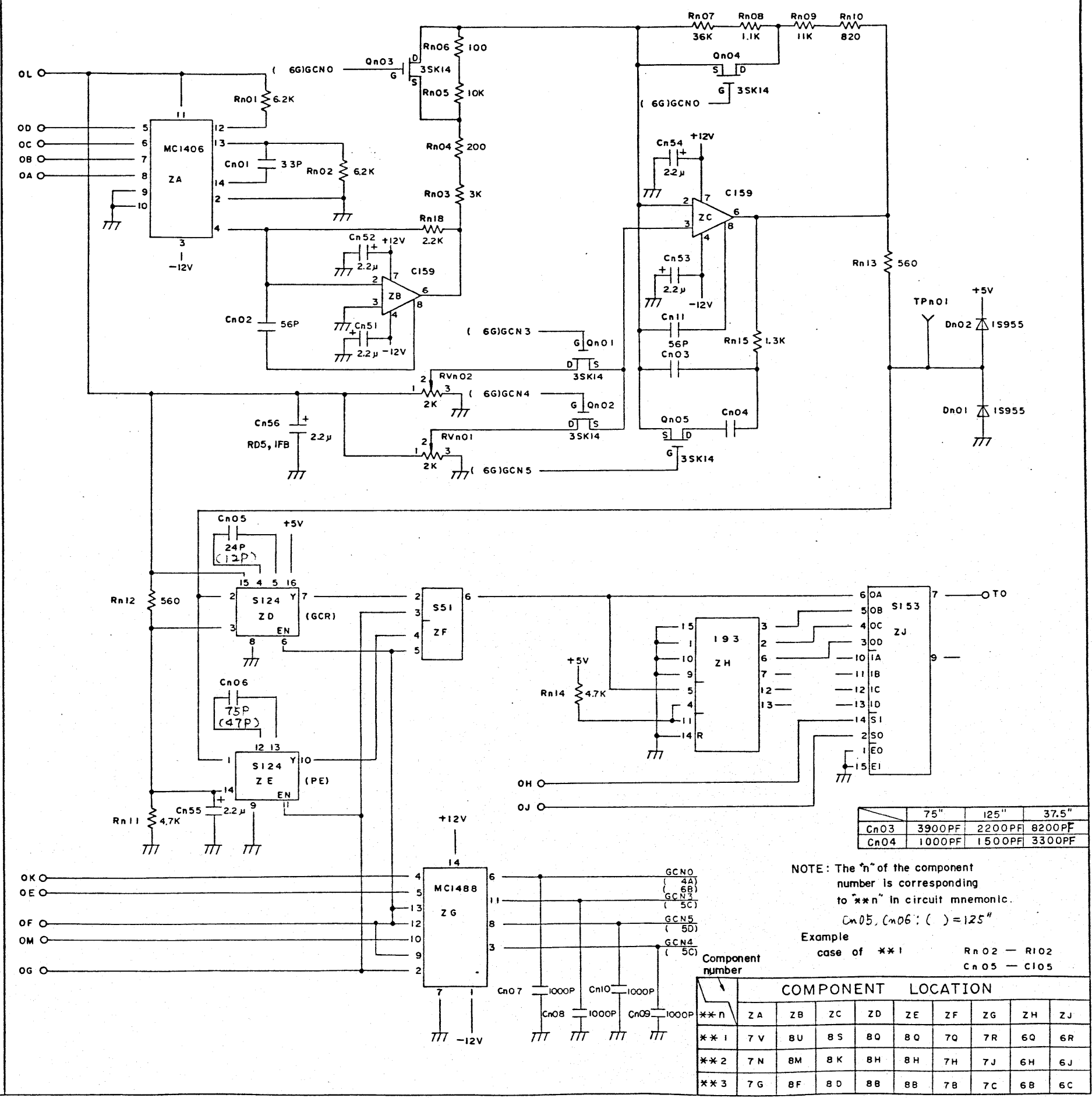
H
装置名

134-110229-012-0

SYMBOL



DETAILED DIAGRAM



	75"	125"	37.5"
Cn03	3900PF	2200PF	8200PF
Cn04	1000PF	1500PF	3300PF

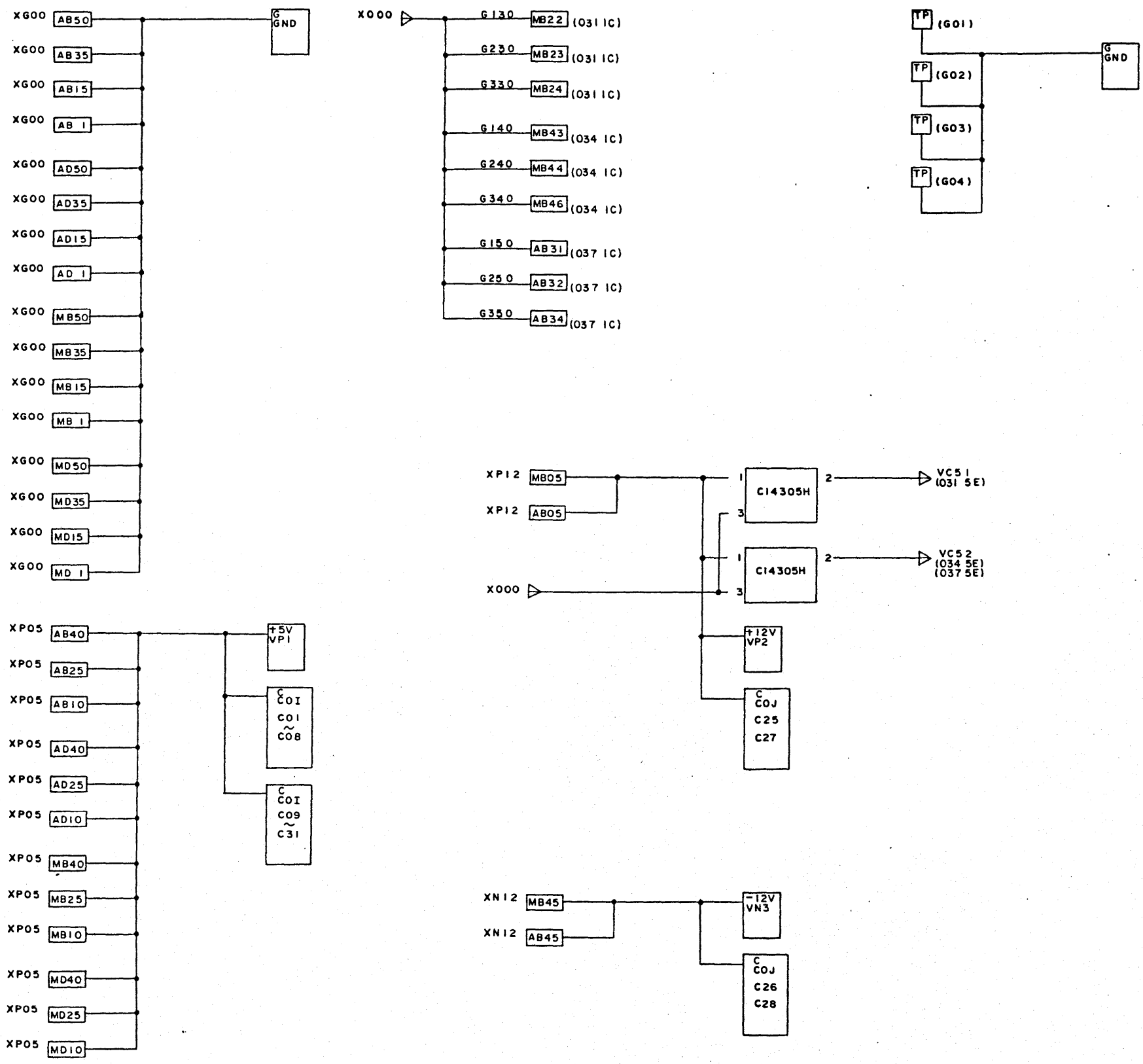
NOTE: The "n" of the component number is corresponding to "**n" in circuit mnemonic.
 Cn05, Cn06: () = 125"
 Example case of **1 Rn02 - R102
 Cn05 - C105

Component number	COMPONENT LOCATION								
**n	ZA	ZB	ZC	ZD	ZE	ZF	ZG	ZH	ZJ
**1	7V	8U	8S	8Q	8Q	7Q	7R	6Q	6R
**2	7N	8M	8K	8H	8H	7H	7J	6H	6J
**3	7G	8F	8D	8B	8B	7B	7C	6B	6C

REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 2			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
041				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	日		村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM ^{11,12} (3, 4, 5 CH)				
134-110229-012-0				
NEC				SHT 11/

134-110229-012-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 2
PKG LOCATION	
PKG NAME	G9JAK, G9JAL

042

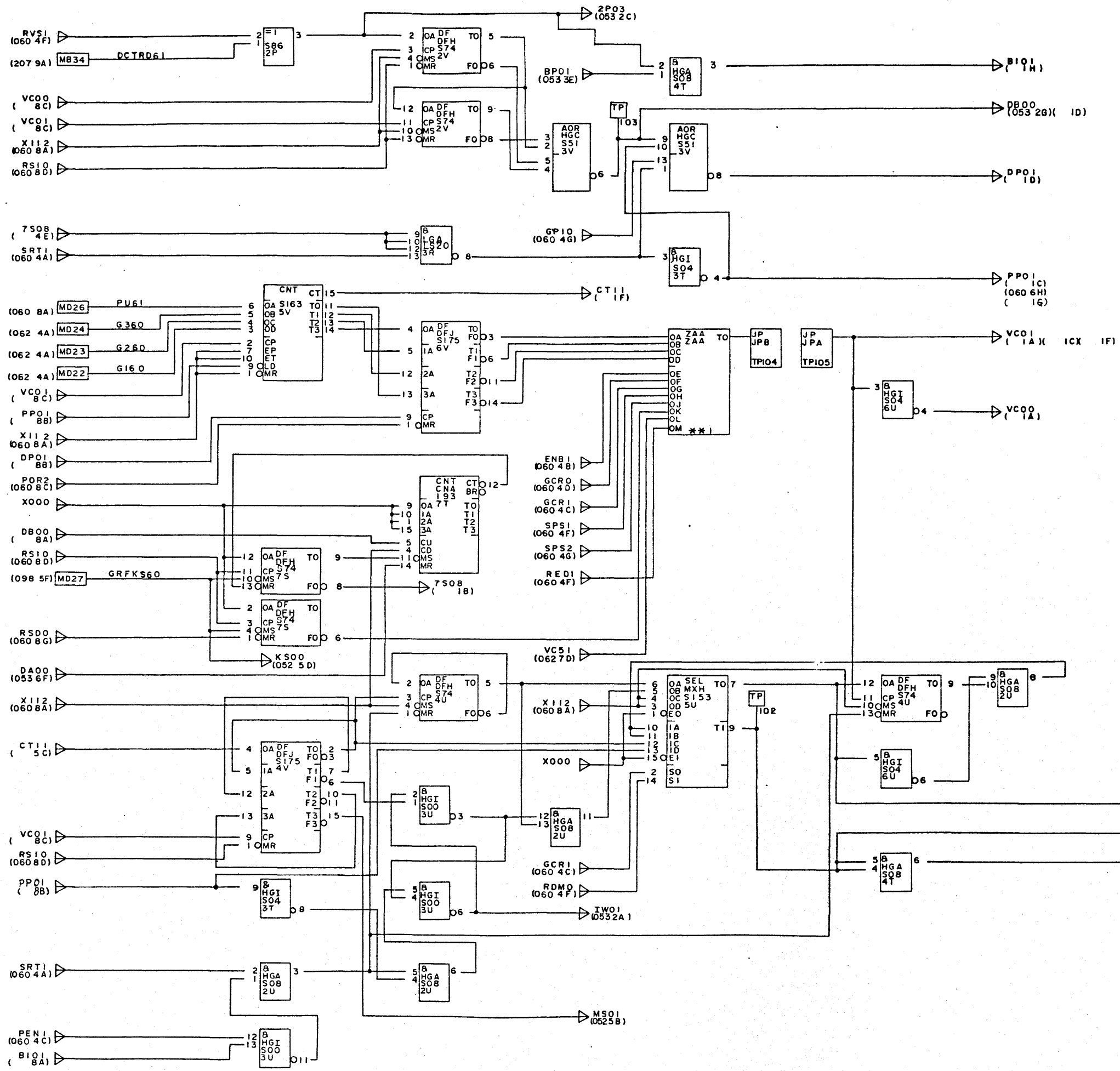
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	

MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR
CIRCUIT DIAGRAM^{12/12}
(3, 4, 5 CH)

134-110229-012-0

NEC ^{SHT} 12/12

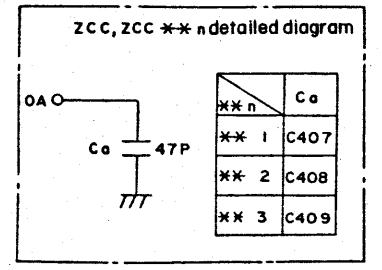
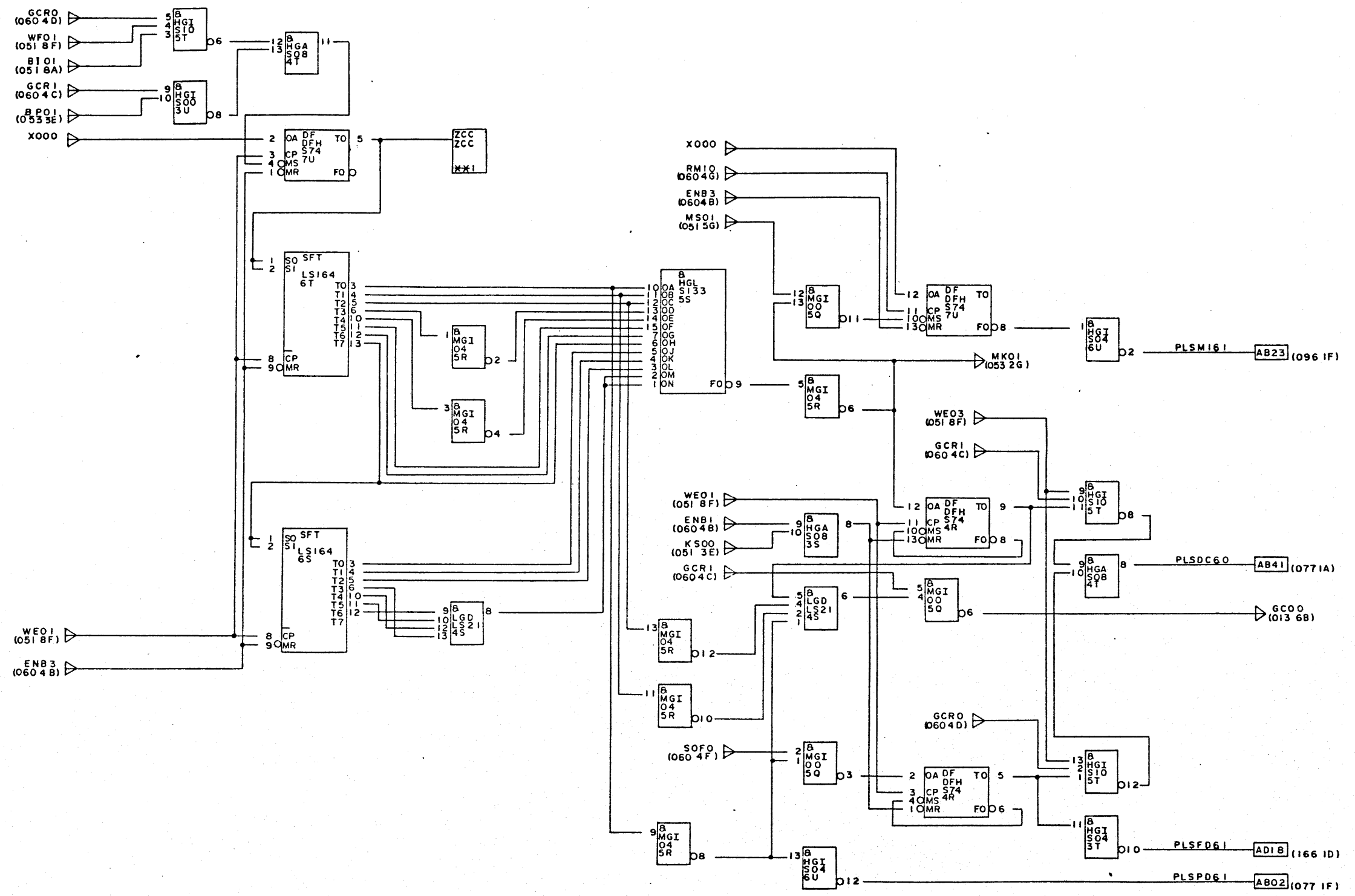
134-110229-011-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	
2	0	1981.2.25 SC-413236 山口	大橋
3	0	1981.11.20 SC-413606 山口 英文化協会 企画書撰	大橋
4	0	1983.3.10 SC-414196 山口 誤記訂正	大橋
DWG ABBR		PLS 3	
PKG LOCATION			
PKG NAME		G9JAK,G9JAL	
051			
NEXT SPEC			
DRAFT	ENG	CHK	APP ISSUE
	山口		今村
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 1/12 (6,7,P CH)			
134-110229-011-0			
NEC			SHT 1/12

装置名

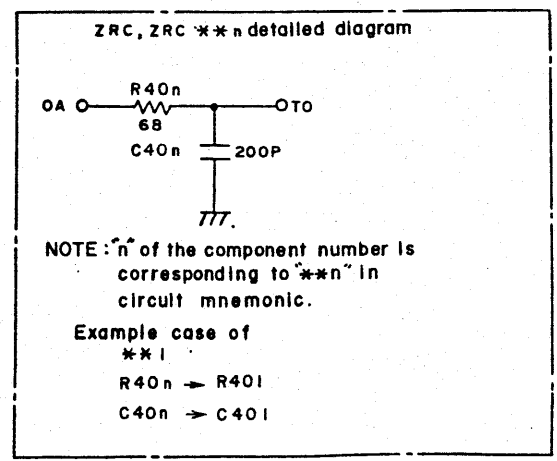
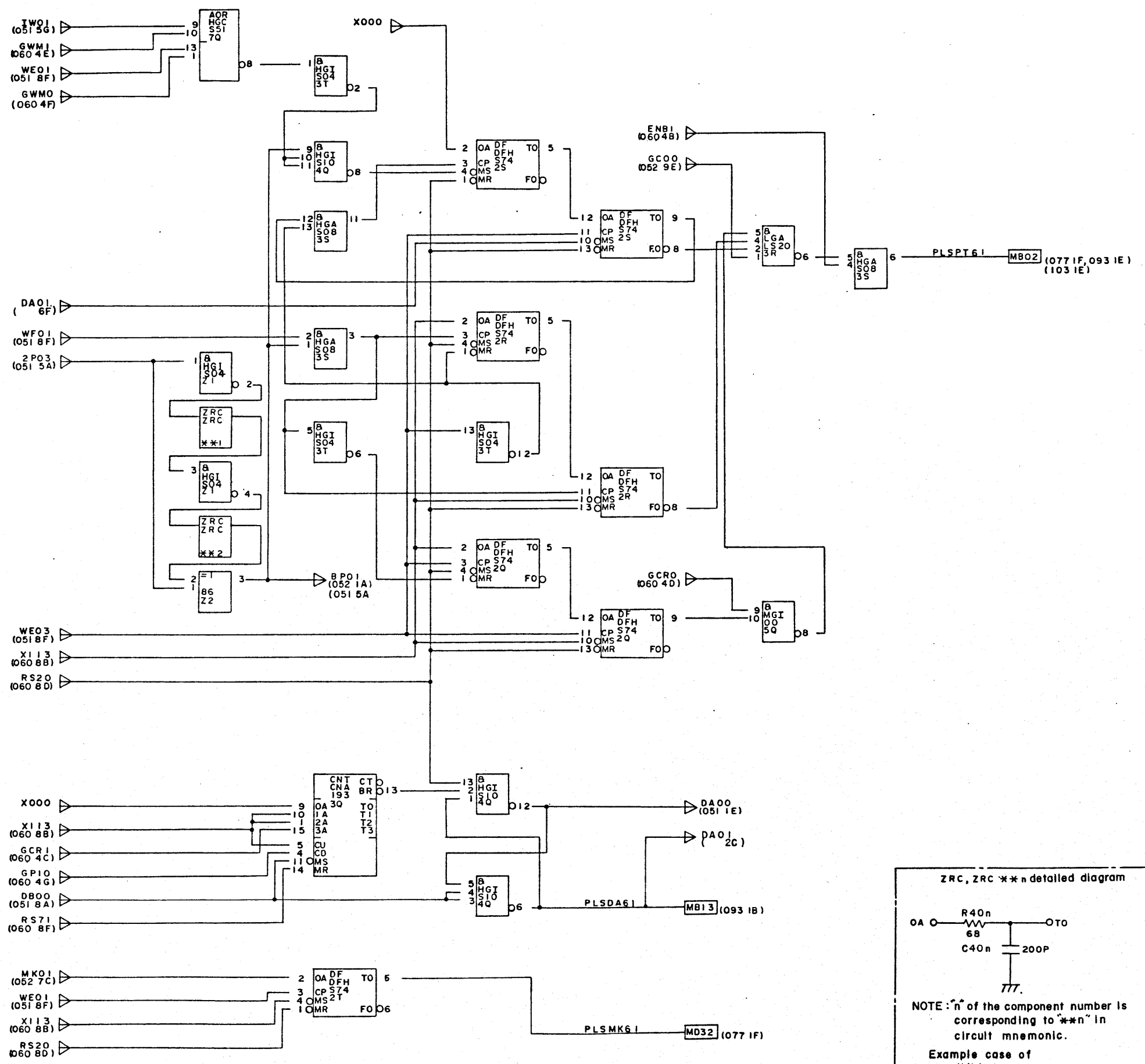
134-110229-011-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 3			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
052				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 2/12 (6,7, P CH)				
134-110229-011-0				
NEC				SHT 2 /

134-110229-011-

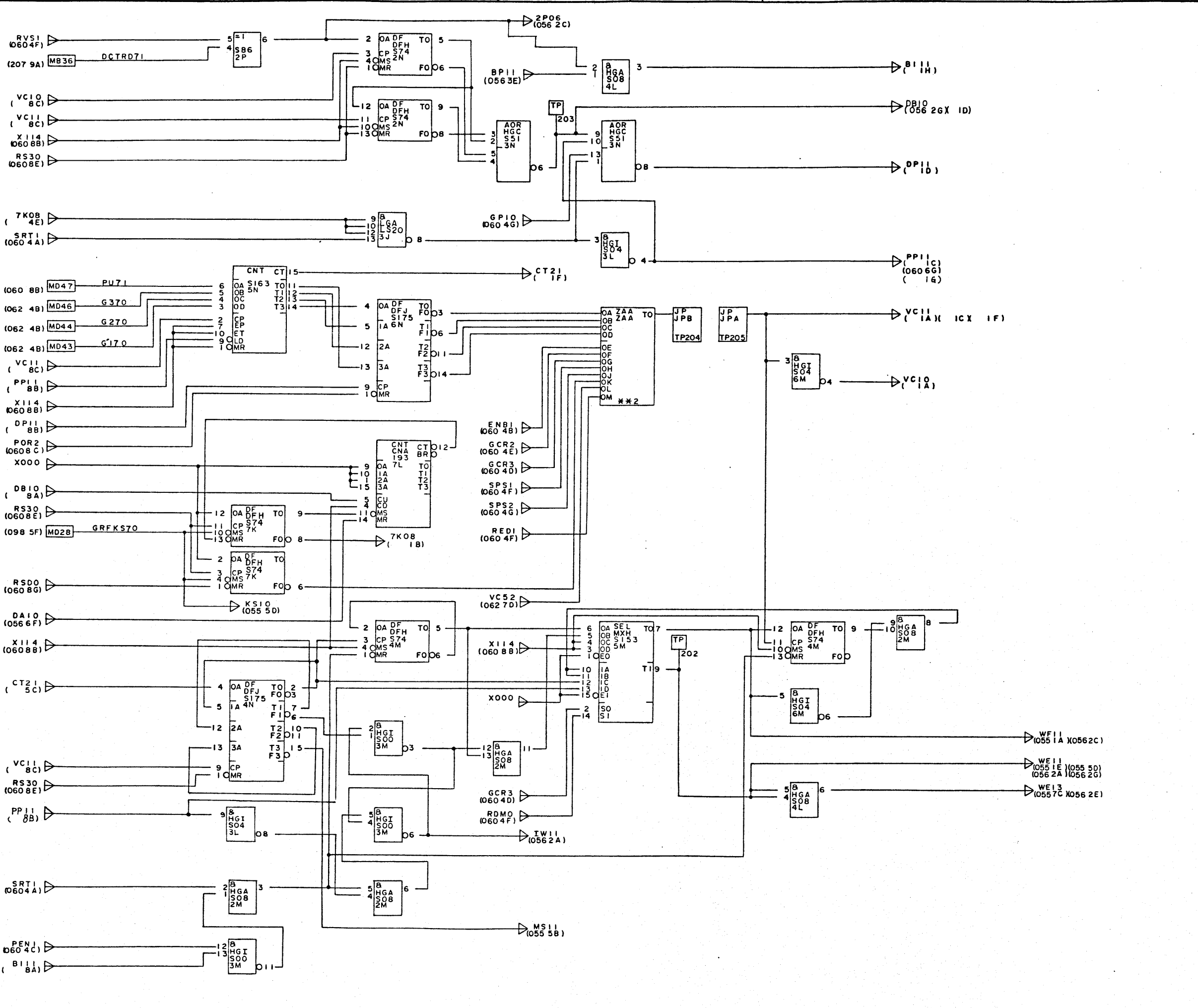


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 3			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
053				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 3/12 (6, 7, P CH)				
134-110229-011-				
NEC				SHT 3/

134-110229-011-0

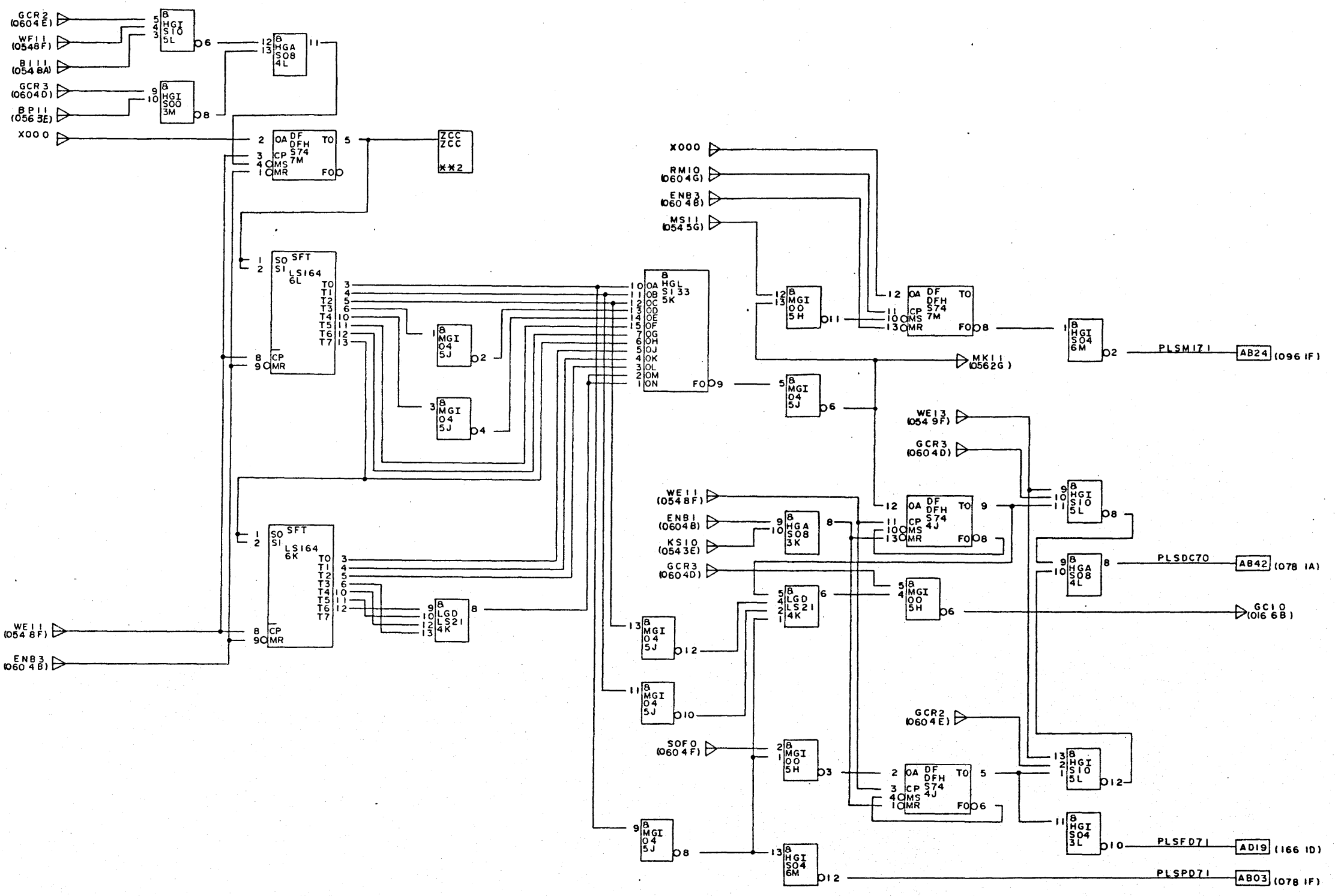
A
B
C
D
E
F
G
H



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 3			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
054				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 4/12 (6, 7, P CH)				
134-110229-011-0				
NEC				SHT 4/

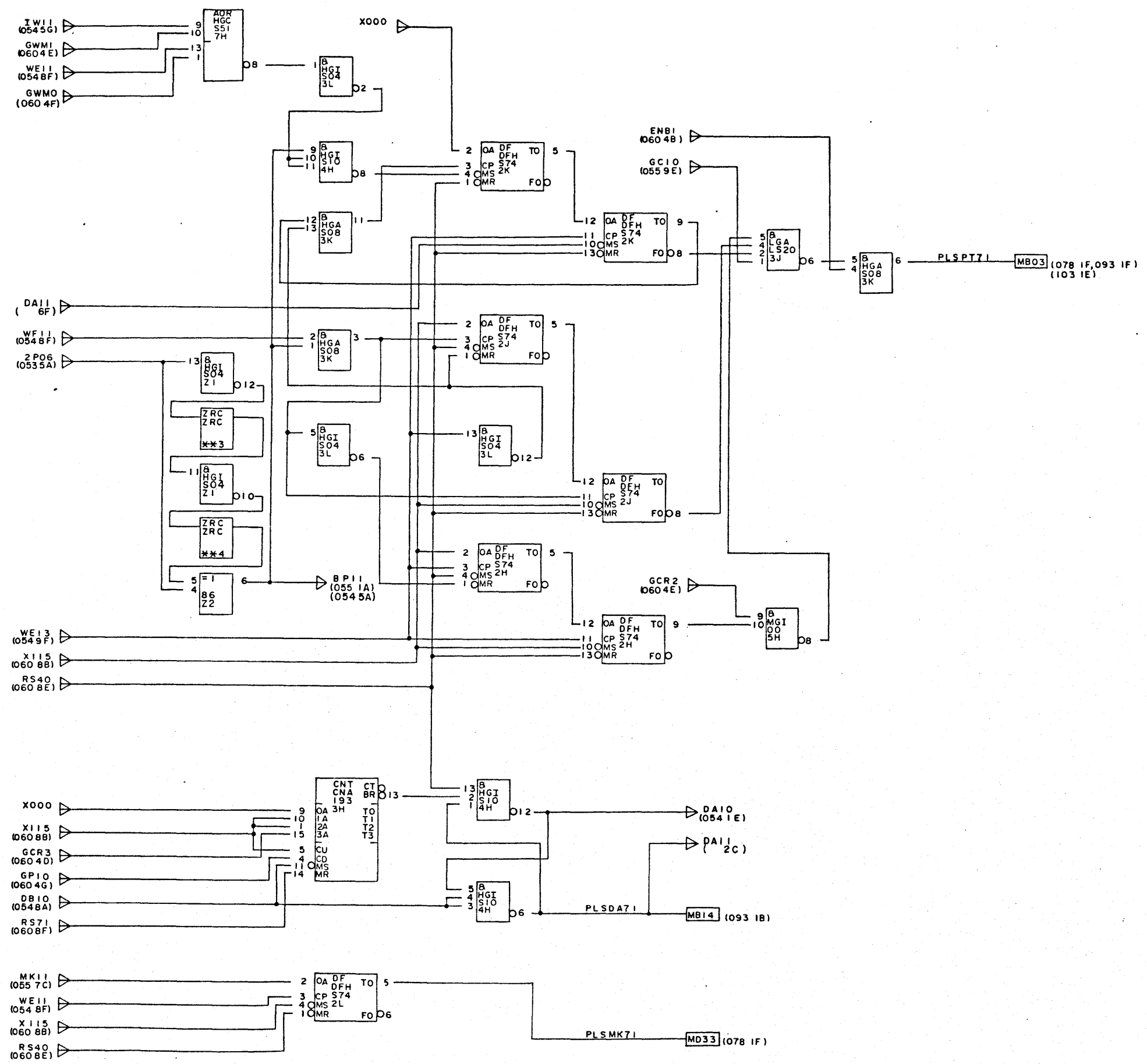
134-110229-011-0



REV	COMP	DESCRIPTION (SC)	APP																														
1	0	55.5.5																															
<table border="1"> <tr> <td>DWG ABBR</td> <td colspan="3">PLS 3</td> </tr> <tr> <td>PKG LOCATION</td> <td colspan="3"></td> </tr> <tr> <td>PKG NAME</td> <td colspan="3">G9JAK,G9JAL</td> </tr> <tr> <td colspan="4" style="text-align: center; font-size: 2em;">055</td> </tr> <tr> <td>NEXT SPEC</td> <td colspan="3"></td> </tr> <tr> <td>DRAFT</td> <td>ENG</td> <td>CHK</td> <td>APP</td> <td>ISSUE</td> </tr> <tr> <td></td> <td>山口</td> <td></td> <td>今村</td> <td></td> </tr> </table>				DWG ABBR	PLS 3			PKG LOCATION				PKG NAME	G9JAK,G9JAL			055				NEXT SPEC				DRAFT	ENG	CHK	APP	ISSUE		山口		今村	
DWG ABBR	PLS 3																																
PKG LOCATION																																	
PKG NAME	G9JAK,G9JAL																																
055																																	
NEXT SPEC																																	
DRAFT	ENG	CHK	APP	ISSUE																													
	山口		今村																														
<p>MTAI6X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM ⁵/₁₂ (6, 7, P CH)</p>																																	
134-110229-011-0																																	
NEC			SHT 5/																														

装置名

134-110229-011

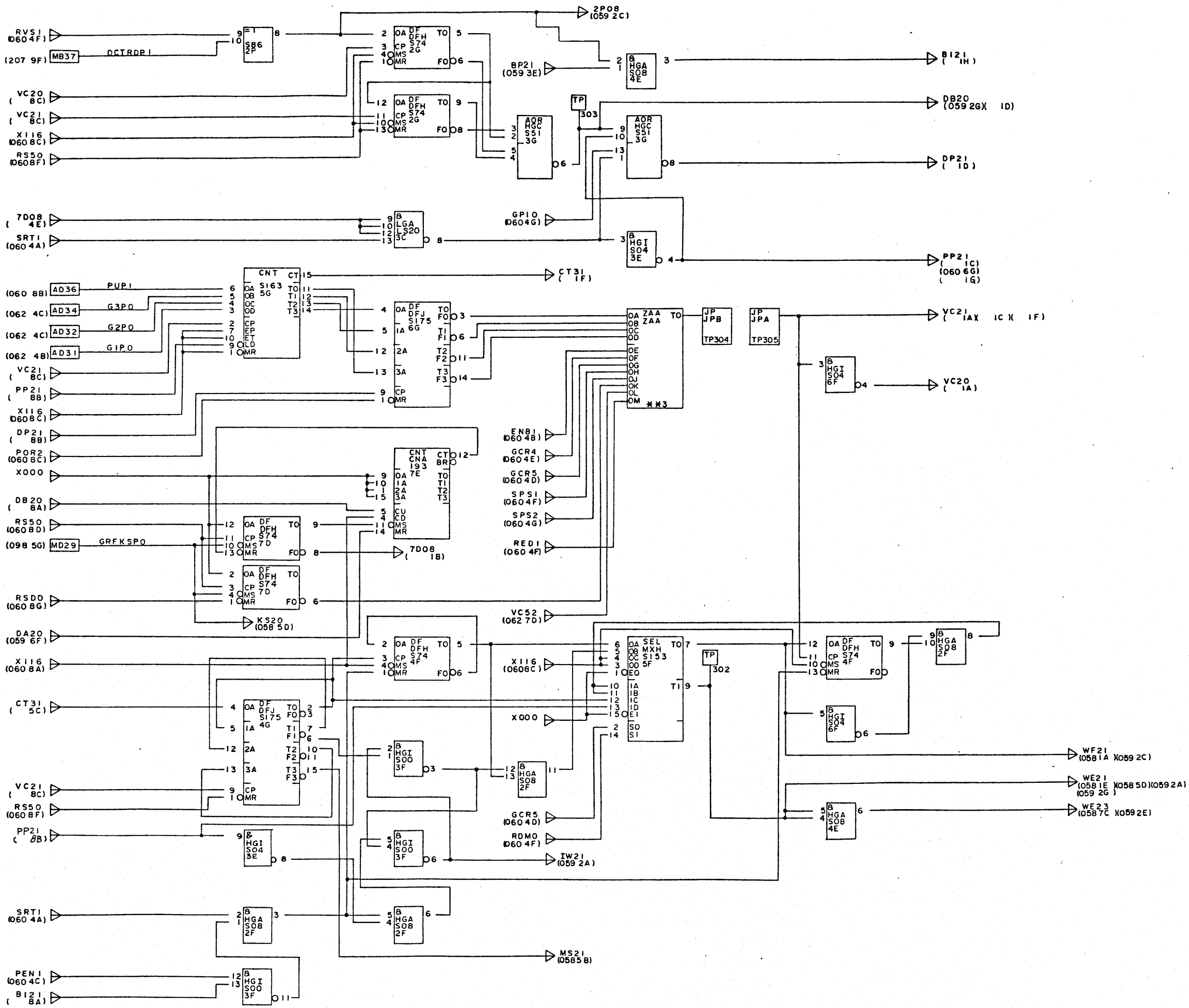


REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 3			
PKG LOCATION				
PKG NAME	G9JAK,G9JAL			
056				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	川		今	
	川		村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 6/12 (6, 7, P CH)				
134-110229-011				
NEC				SHT 6/

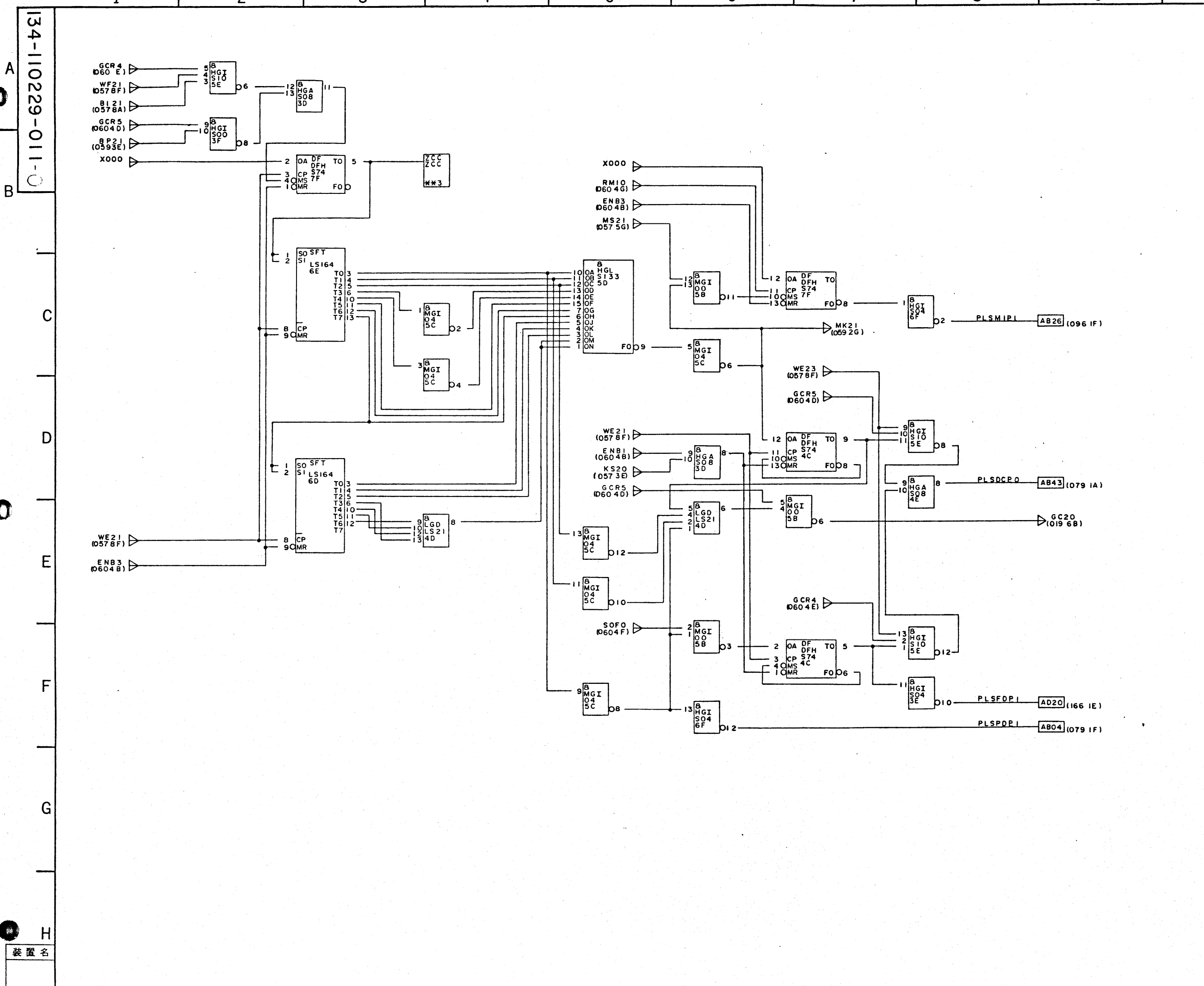
装置名

134-110229-011-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

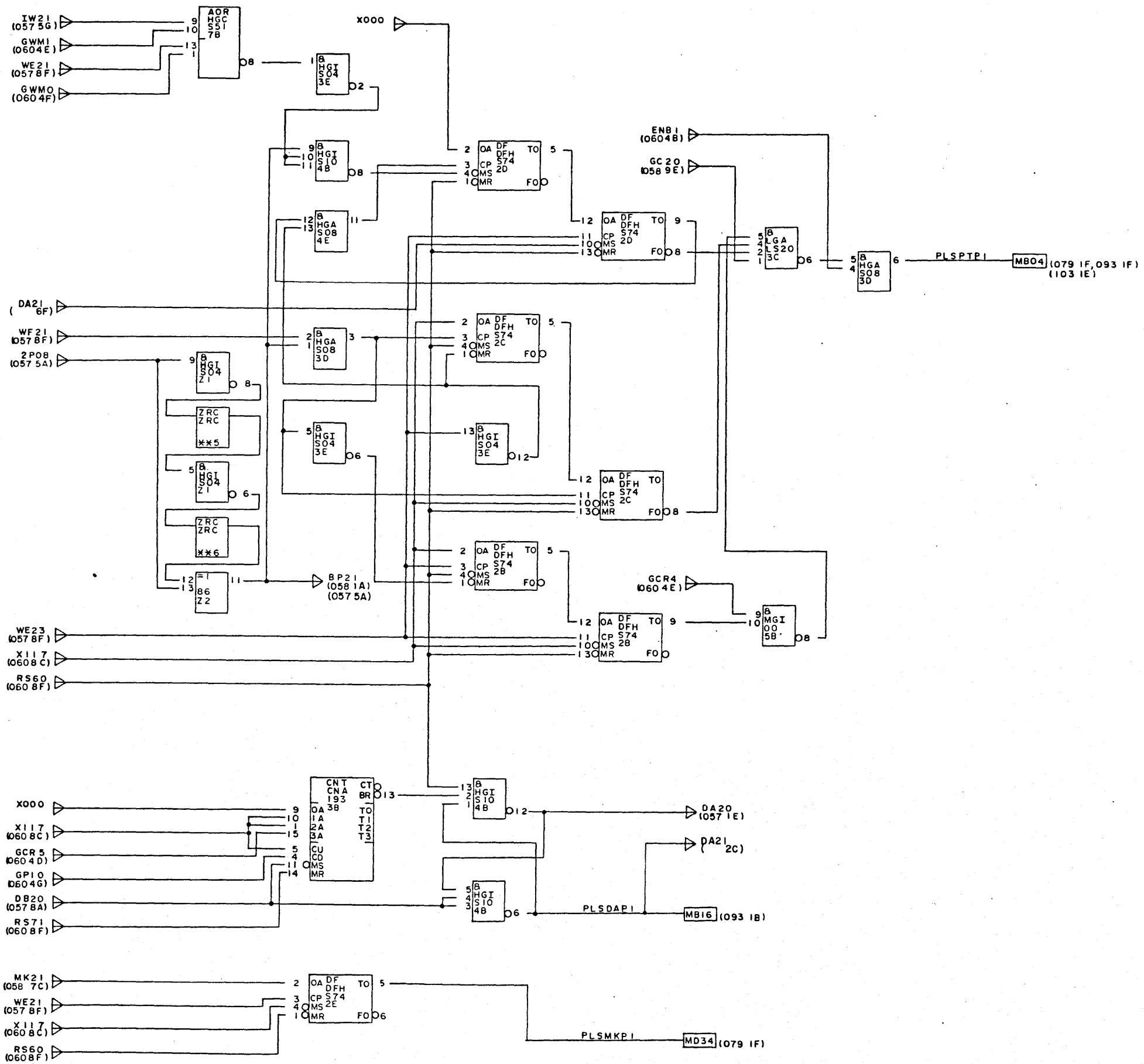
DWG ABBR	PLS 3			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
057				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	
MTAI6X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 7/12 (6, 7, P CH)				
134-110229-011-0				
NEC				SHT 7/



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS3			
PKG LOCATION				
PKG NAME	G9JAK,G9JAL			
058				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 8/12 (6,7, P CH)				
134-110229-011-0				
NEC				SHT 8/

134-110229-011-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 3			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
059				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	

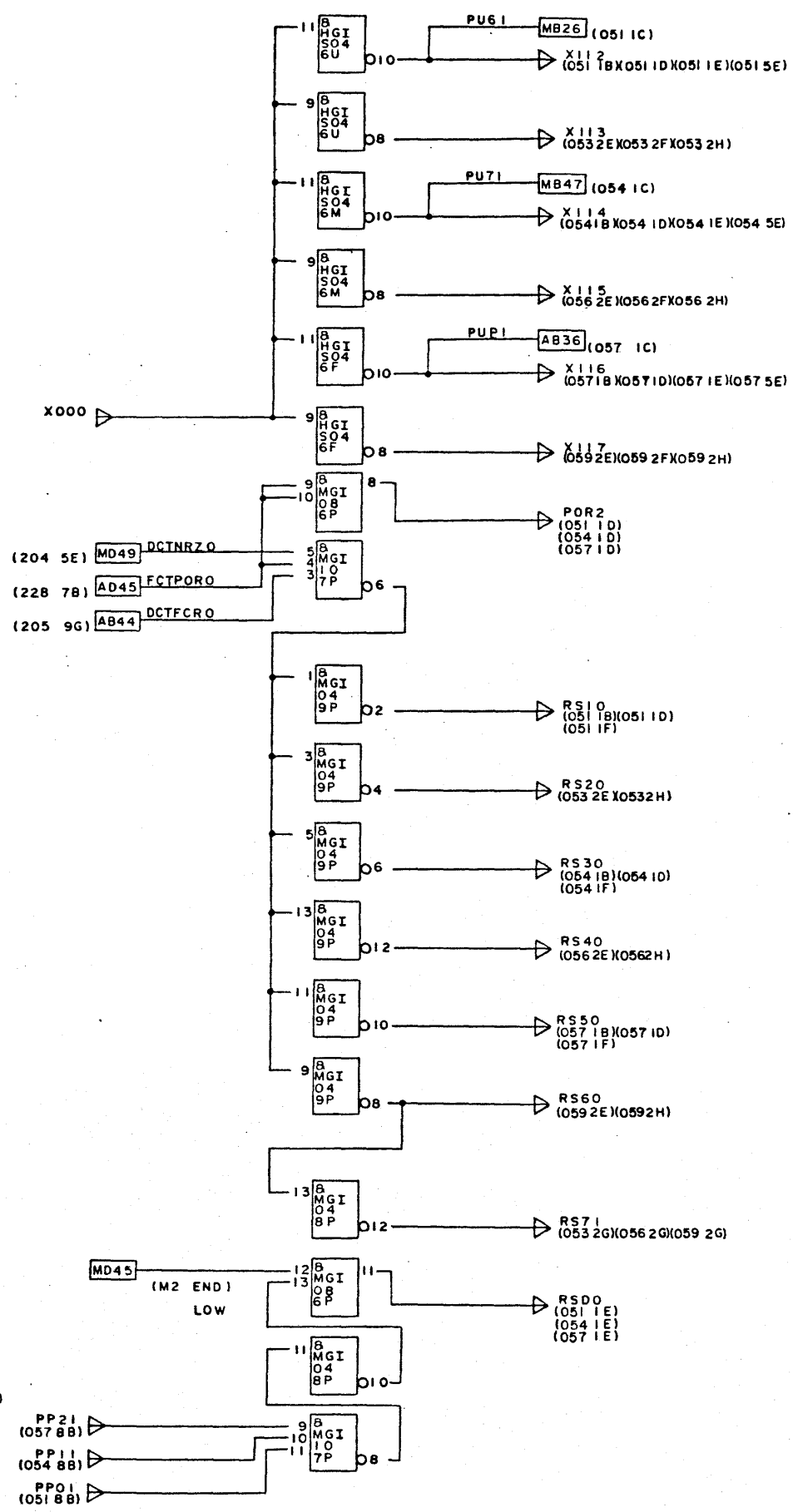
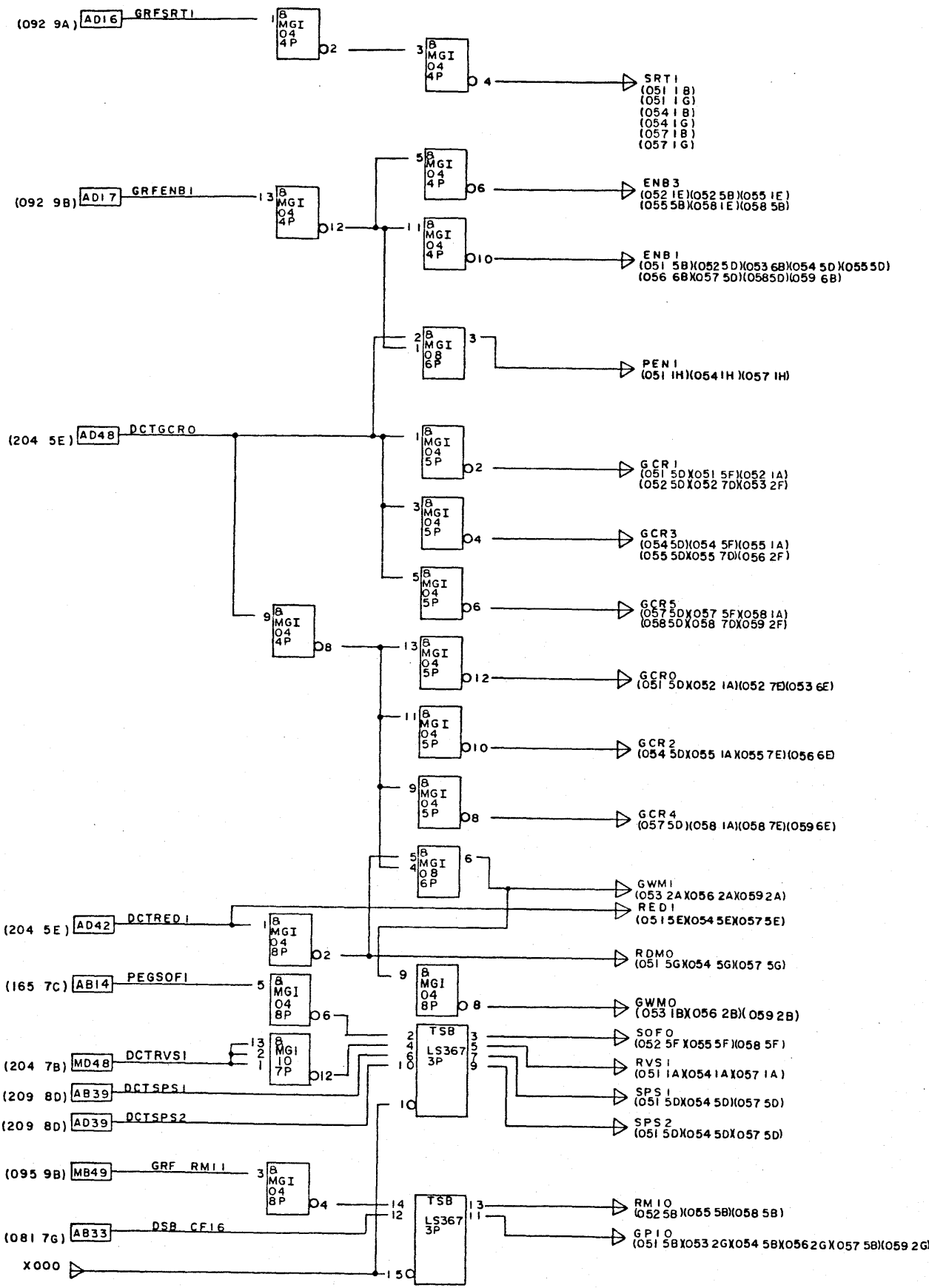
MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR
CIRCUIT DIAGRAM 9/12
(6,7, P CH)

134-110229-011-0

NEC SHT 9/

装置名

134-110229-011-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 3			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
060				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

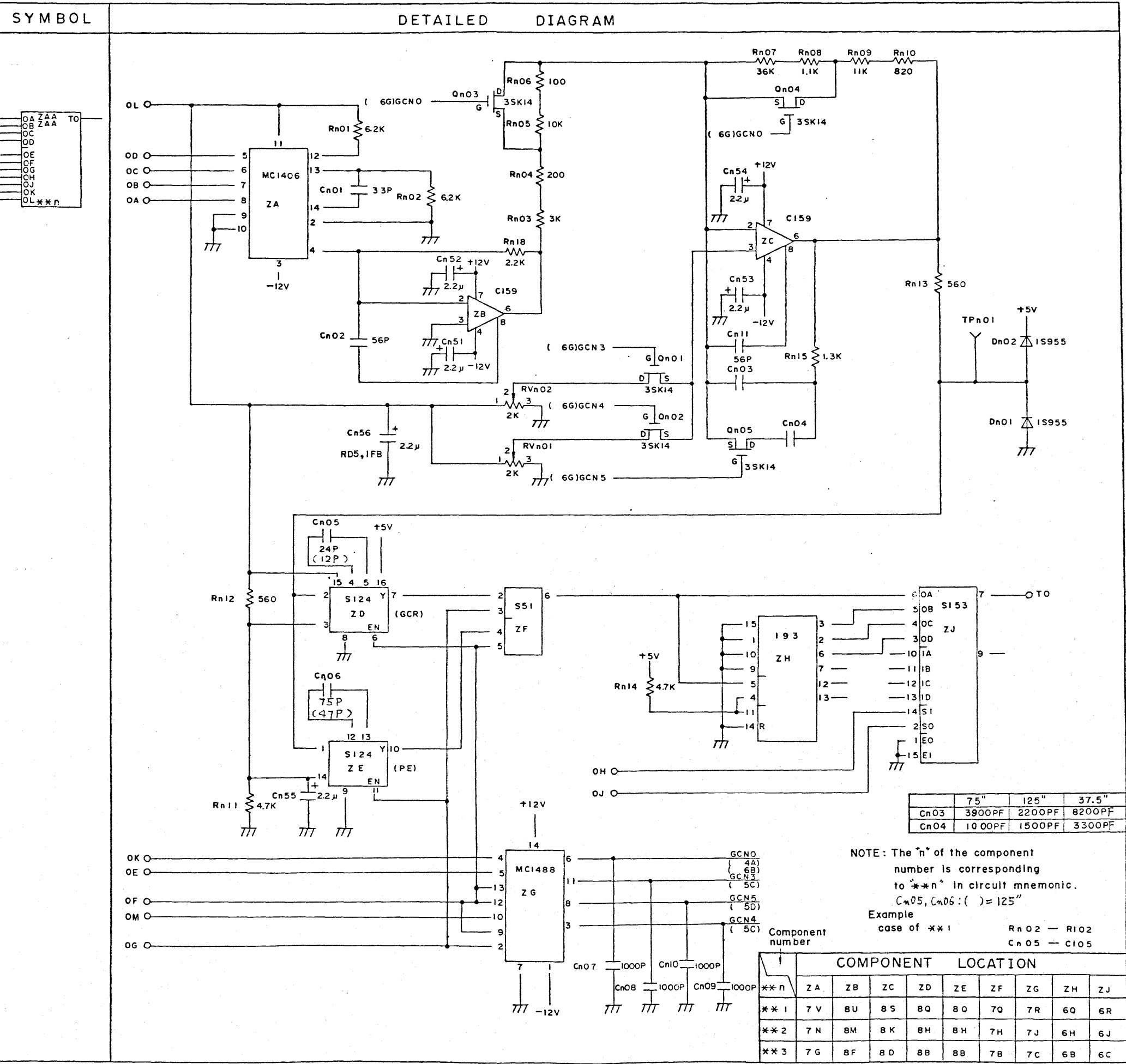
MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR
CIRCUIT DIAGRAM^{10/12}
(6, 7, P CH)

134-110229-011-0

NEC SHT 10/

装置名

134-110229-011-



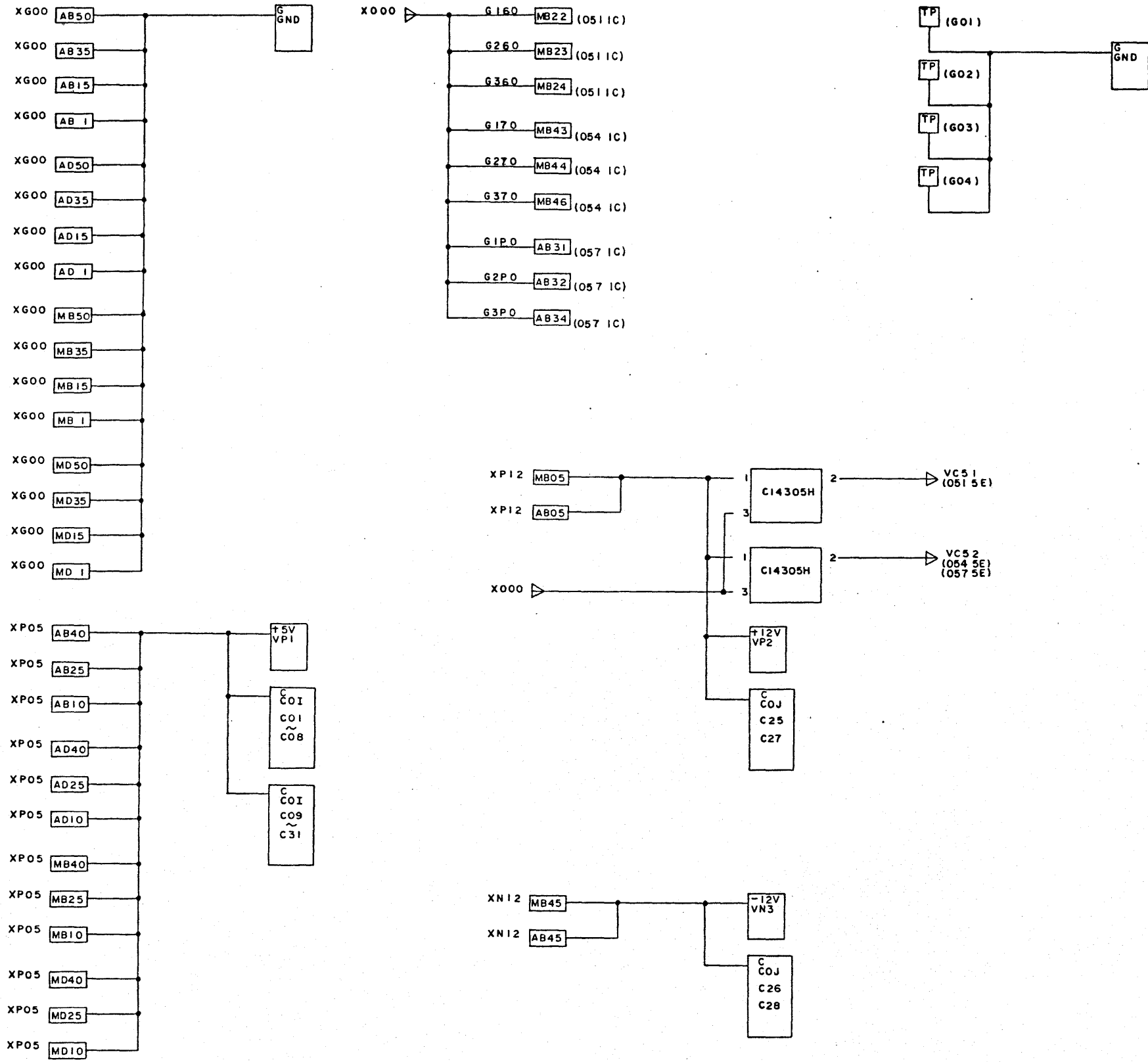
NOTE: The "n" of the component number is corresponding to "*"n" in circuit mnemonic.
 Cn05, Cn06: () = 125"
 Example case of **1 Rn02 - R102
 Cn05 - C105

Component number	COMPONENT LOCATION								
	Z A	Z B	Z C	Z D	Z E	Z F	Z G	Z H	Z J
**1	7V	8U	8S	8Q	8Q	7O	7R	6Q	6R
**2	7N	8M	8K	8H	8H	7H	7J	6H	6J
**3	7G	8F	8D	8B	8B	7B	7C	6B	6C

REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS3			
PKG LOCATION				
PKG NAME	G9JAK,G9JAL			
061				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	
MTA16X FORMATTER GCR/PE READ DISCRIMINATOR CIRCUIT DIAGRAM 1/12 (6,7,P CH)				
134-110229-011-				
NEC				SHT 11/

134-110229-011



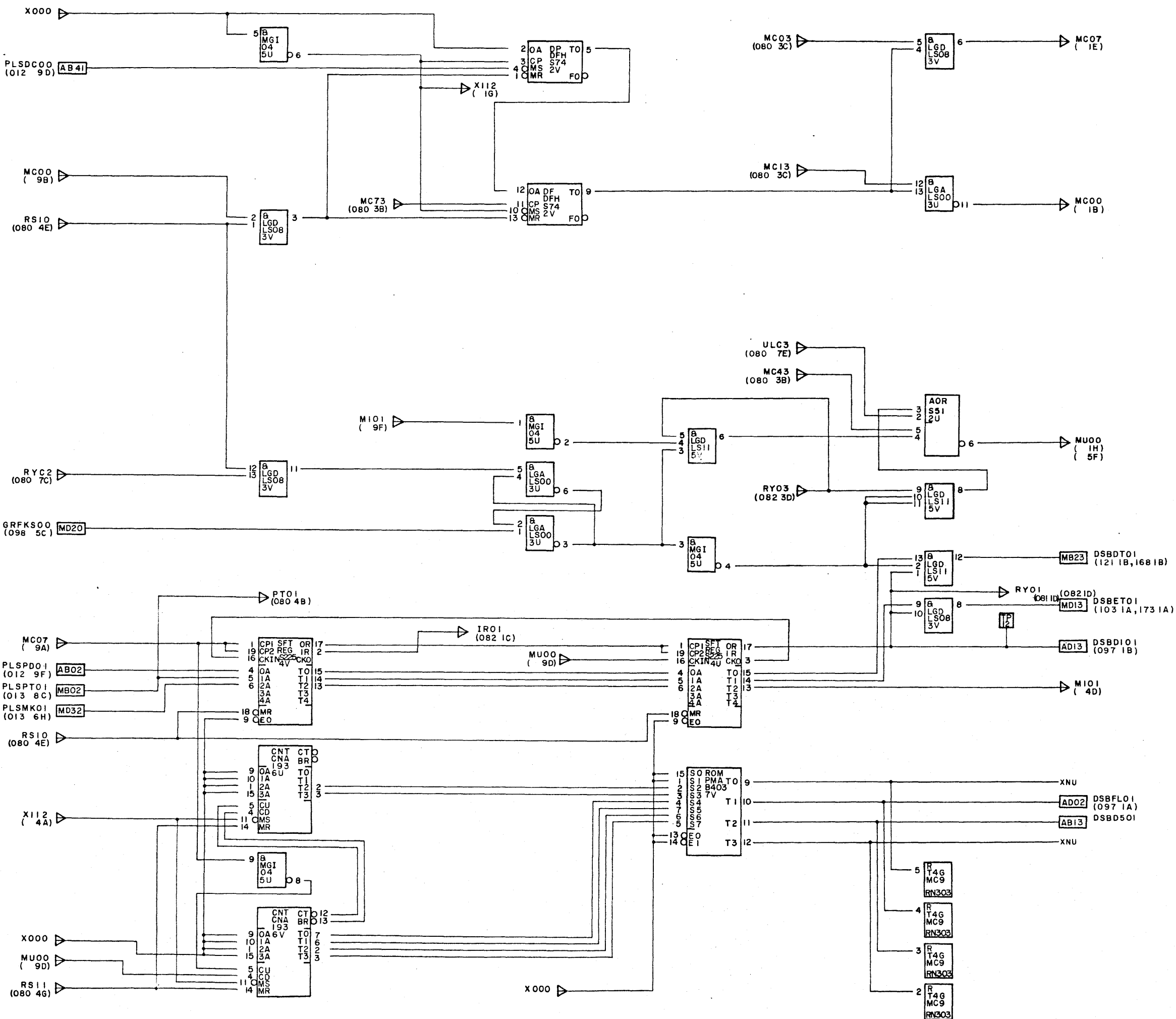
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PLS 3			
PKG LOCATION				
PKG NAME	G9JAK, G9JAL			
062				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
GCR/PE READ
DISCRIMINATOR
CIRCUIT DIAGRAM 1/12
(6,7, P CH)

134-110229-011 - 0
NEC SHIT 12/12

134-110229-010-0

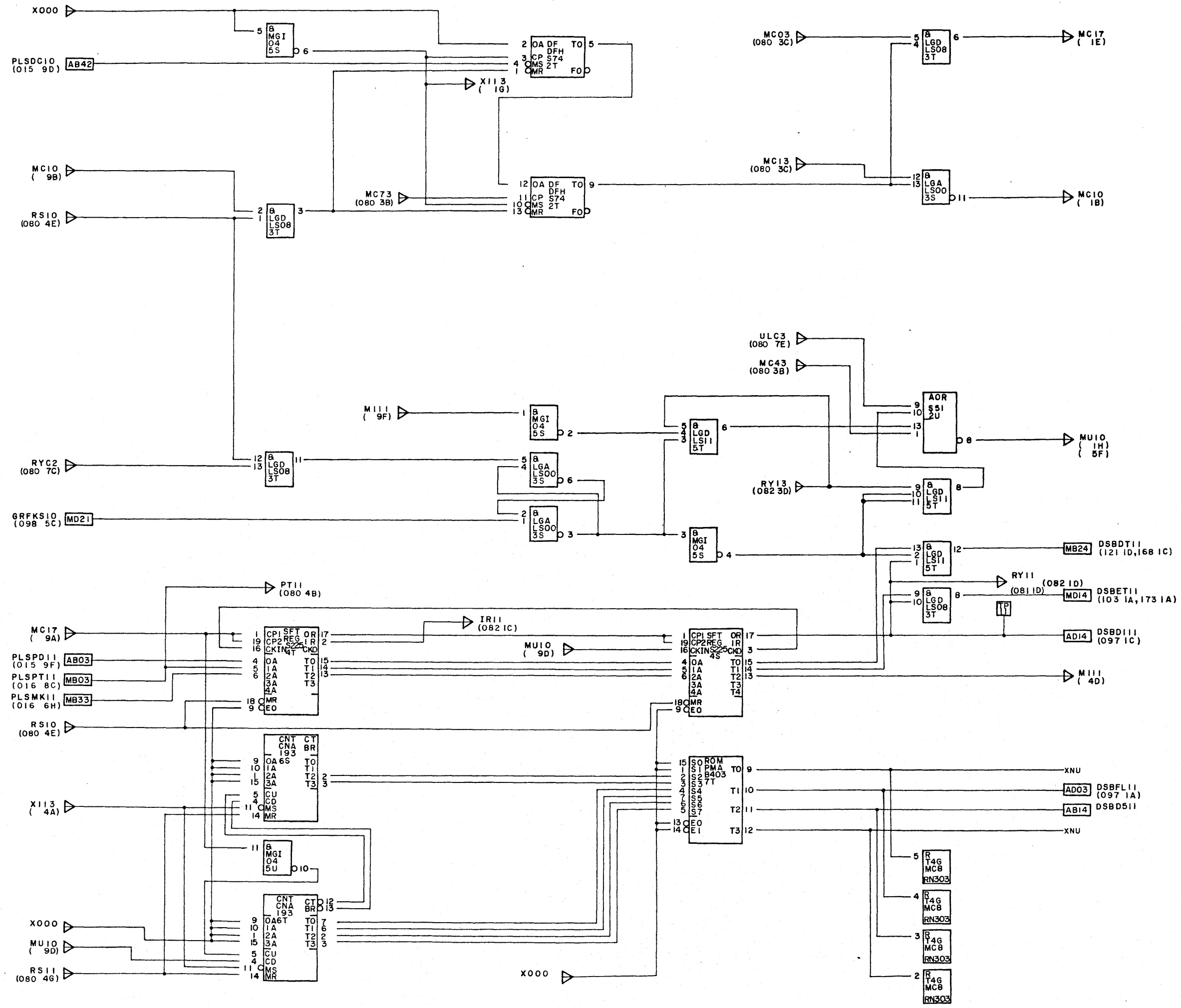


DWG ABBR	D S B		
PKG LOCATION			
PKG NAME	G9JAM, G9MWW		
071			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山		今
	口		村

MTA16X FORMATTER
 DESKEWING BUFFER
 CIRCUIT DIAGRAM
 1/12
 134-110229-010-0
 NEC

装置名

134-110229-010-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	D S B		
PKG LOCATION			
PKG NAME	G9JAM, G9MWW		
072			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山		今村
	川		

MTA16X FORMATTER
DESKEWING BUFFER
CIRCUIT DIAGRAM
2/12

134-110229-010-0

NEC SHT 2/

134-110229-010-0

REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

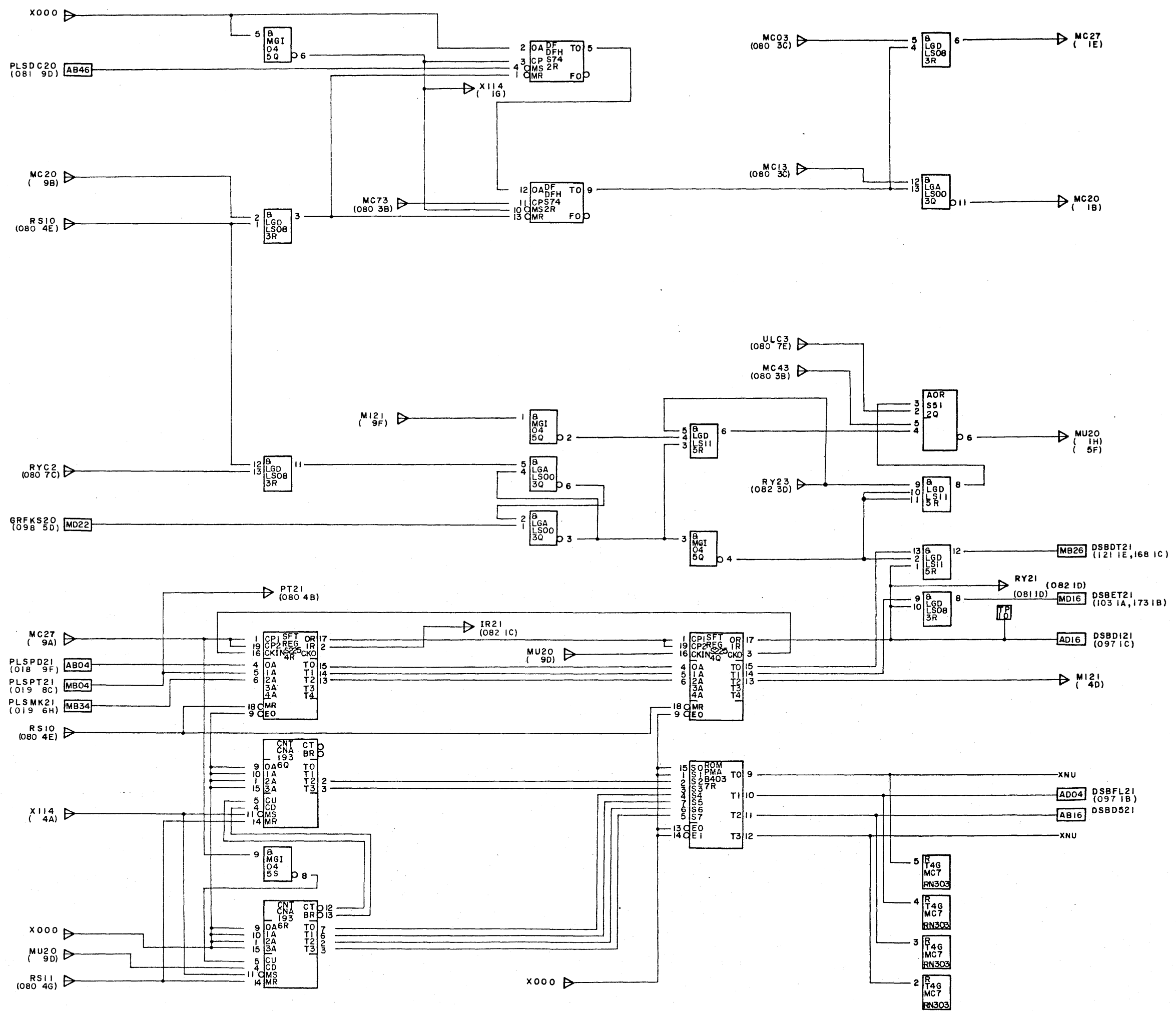
DWG ABBR	D S B
PKG LOCATION	
PKG NAME	G9JAM,G9MWW
073	

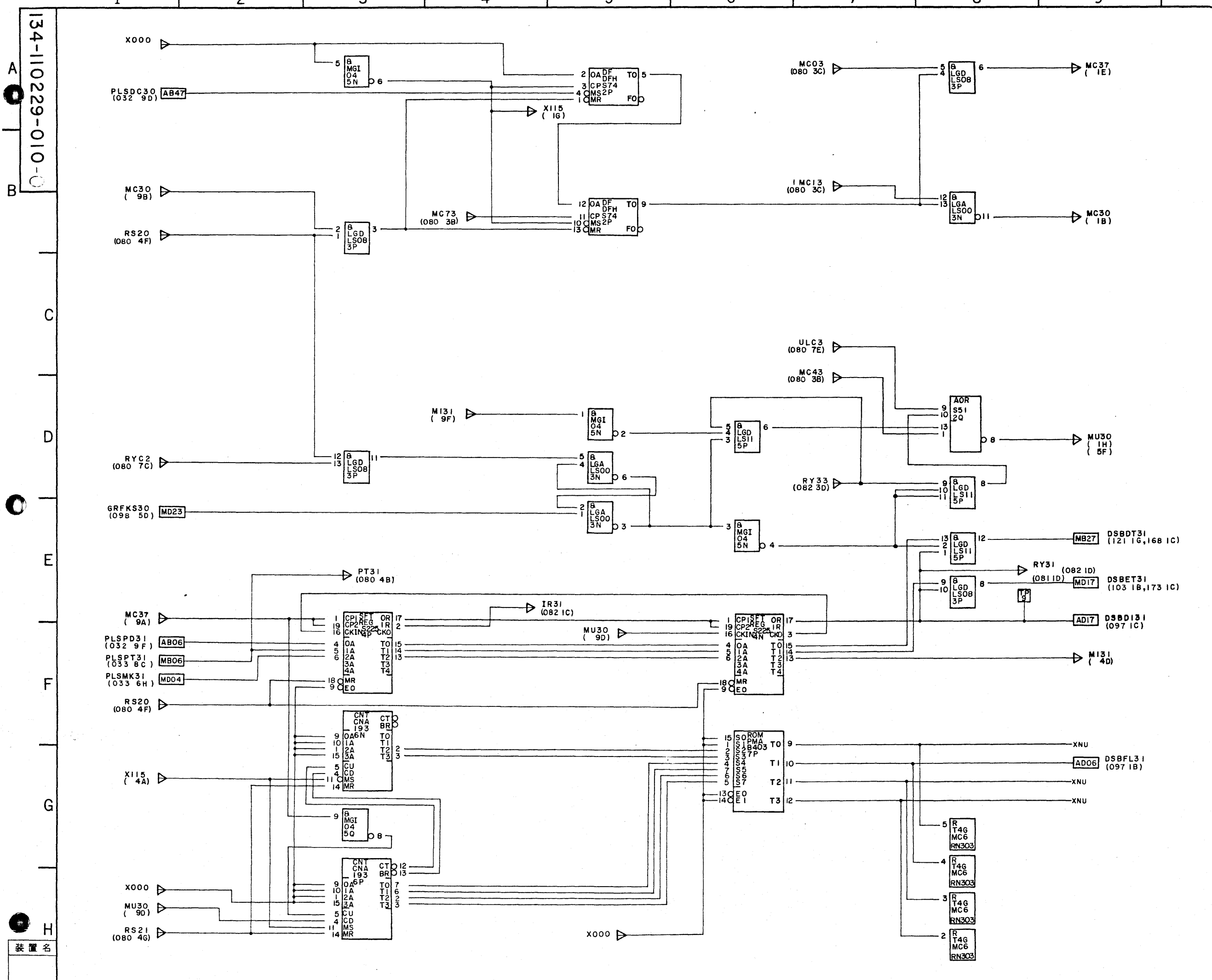
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
DESKEWING BUFFER
CIRCUIT DIAGRAM
3/12

134-110229-010-0

NEC SHT 3/





REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

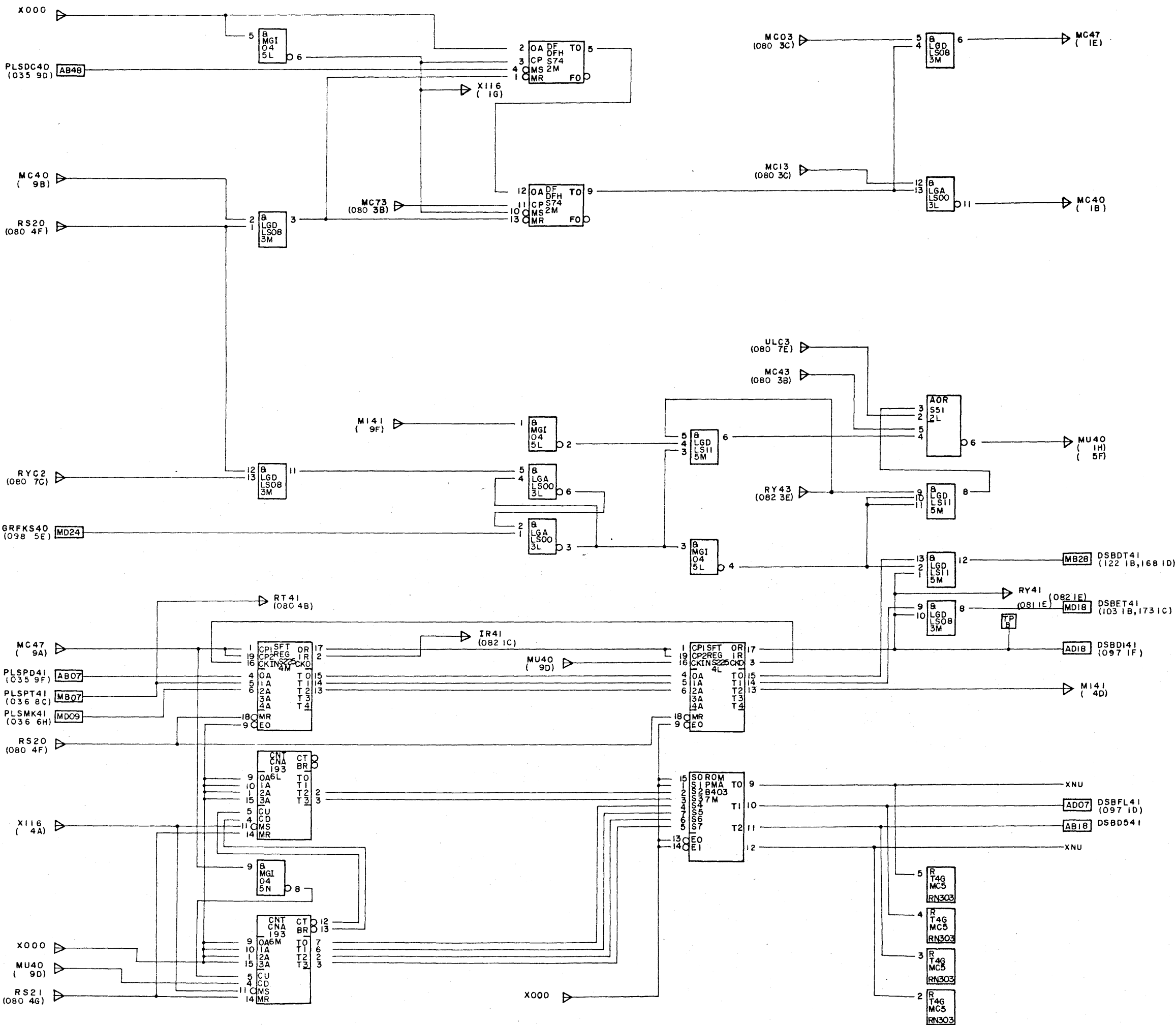
DWG ABBR	D S B			
PKG LOCATION				
PKG NAME	G9JAM,G9MWW			
074				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

**MTA16X FORMATTER
 DESKEWING BUFFER
 CIRCUIT DIAGRAM**
 4/12
 134-110229-010-0
NEC SHT 4/

134-110229-010-0
 A
 B
 C
 D
 E
 F
 G
 H
 装置名

X
 Y
 A
 B
 C
 D
 E
 F
 G
 H

134-110229-010



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	DSB			
PKG LOCATION				
PKG NAME	G9JAM,G9MWW			
075				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	山		村	

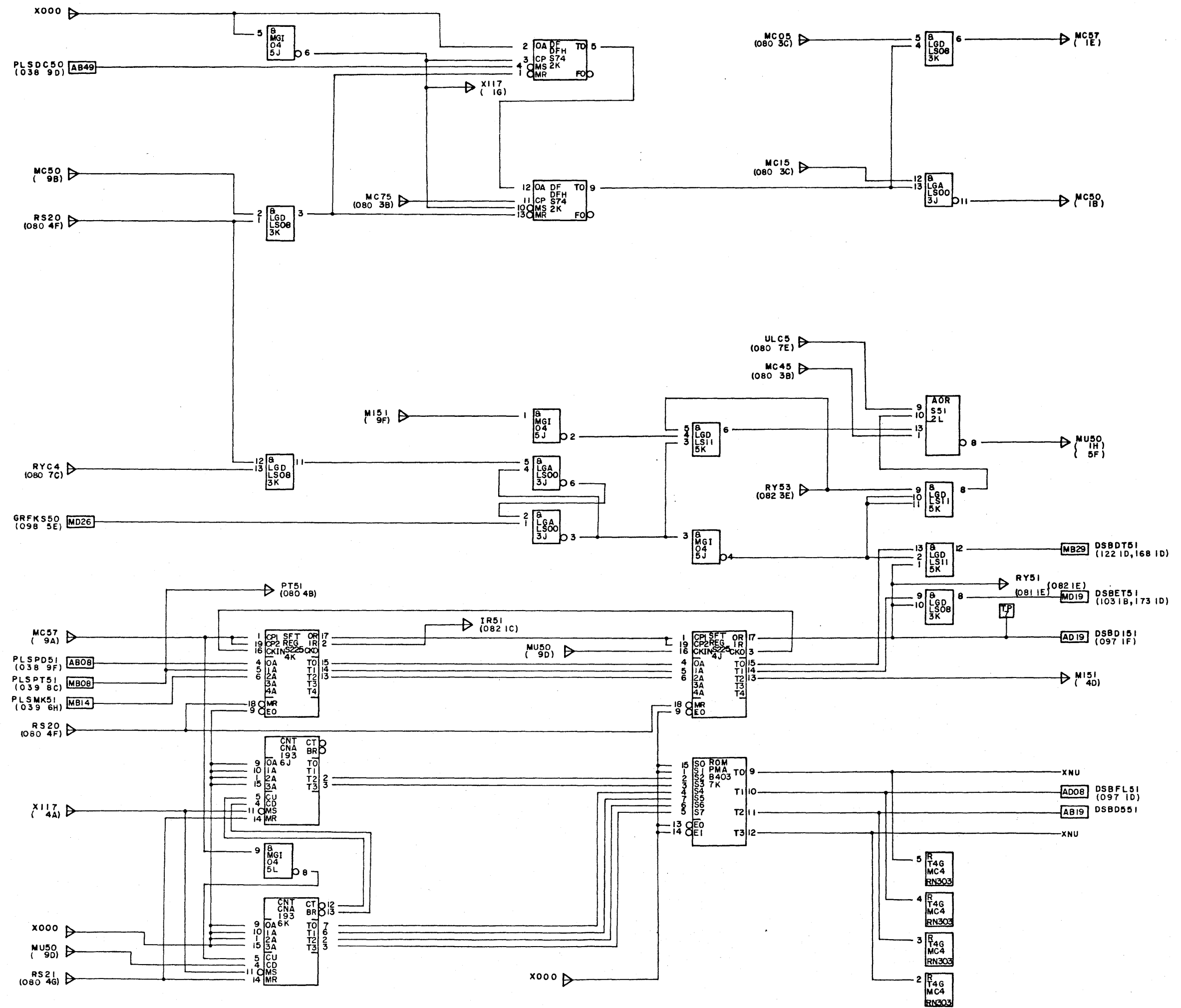
MTA16X FORMATTER DESKEWING BUFFER CIRCUIT DIAGRAM				
5/12				
134-110229-010				
NEC				SHT 5/

装置名

134-110229-010-0

REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	D S B		
PKG LOCATION			
PKG NAME	G9JAM,G9MWW		
076			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER DESKEWING BUFFER CIRCUIT DIAGRAM 6/12			
134-110229-010-0			
NEC			SHT 6/

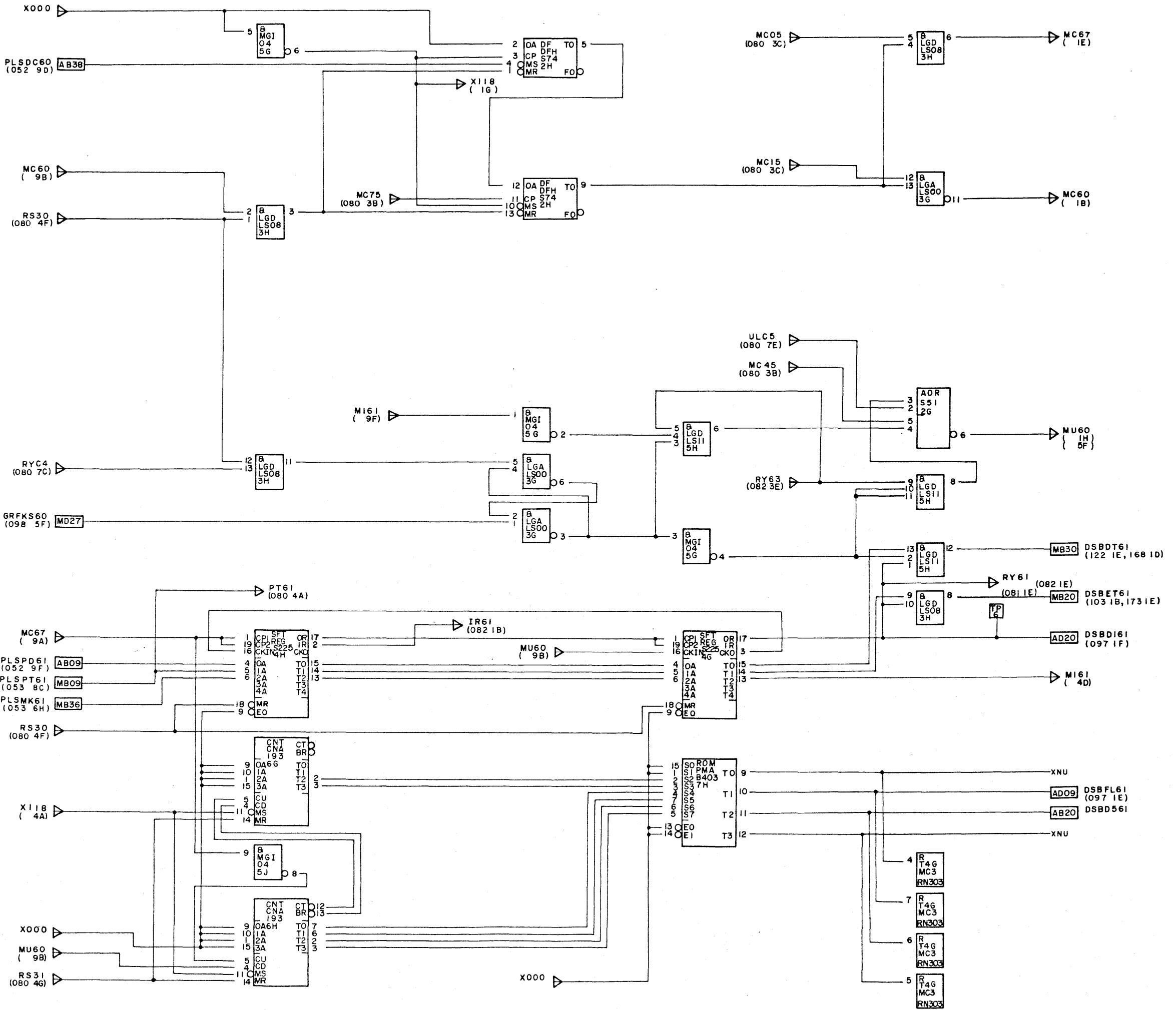


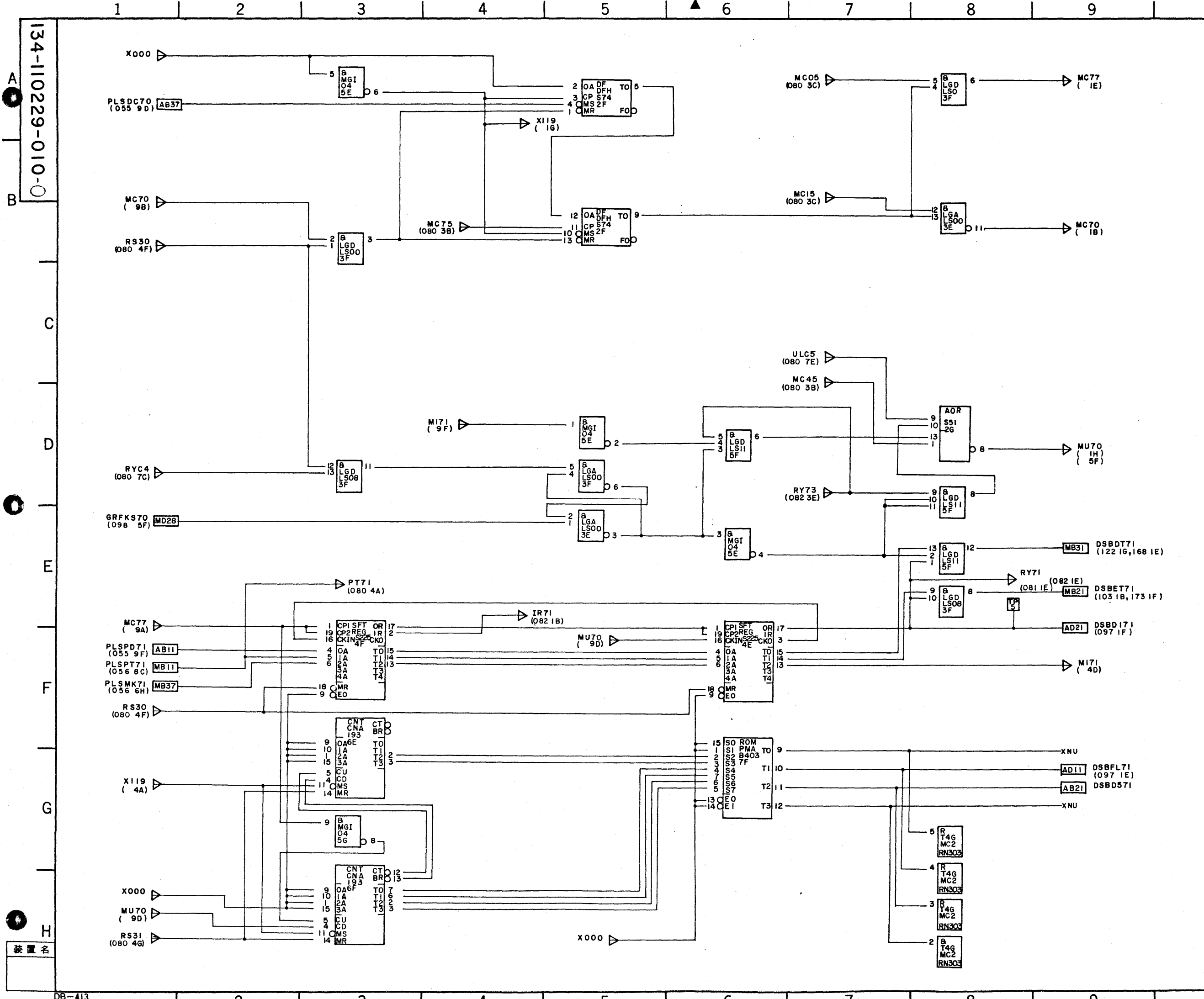
A
B
C
D
E
F
G
H

A
B
C
D
E
F
G
H

装置名

134-110229-010-0



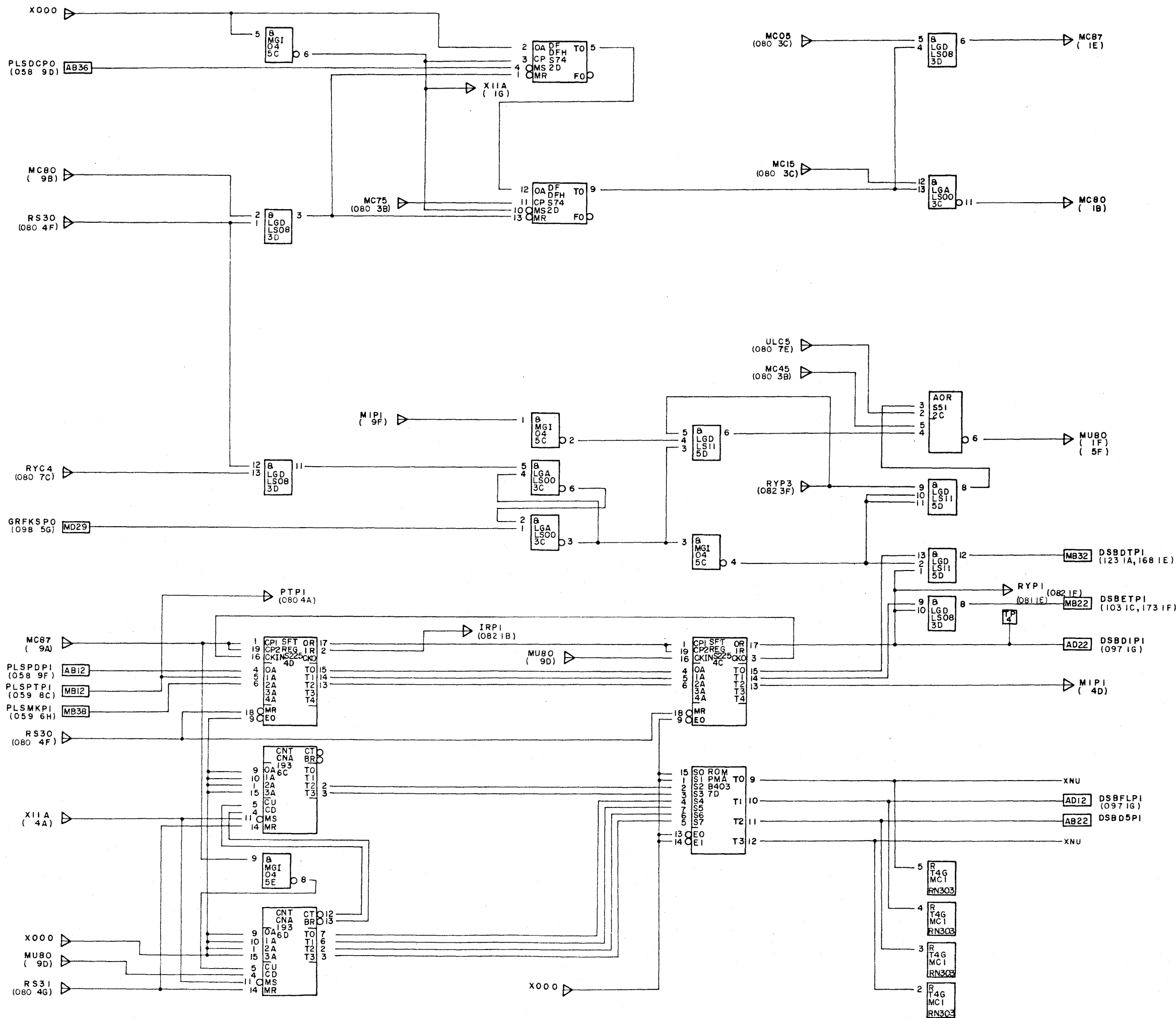


REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	
DWG ABBR		D S B	
PKG LOCATION			
PKG NAME		G9JAM, G9MWW	
078			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER DESKEWING BUFFER CIRCUIT DIAGRAM 8/12			
134-110229-010-0			
NEC			SHT 8 /

装置名
DB-413
MC 10 (100V)

134-110229-010-C

1 2 3 4 5 6 7 8 9 X Y



DWG ABBR	D S B
PKG LOCATION	
PKG NAME	G9JAM,G9MWW
079	

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	III		今村	
	II		村	

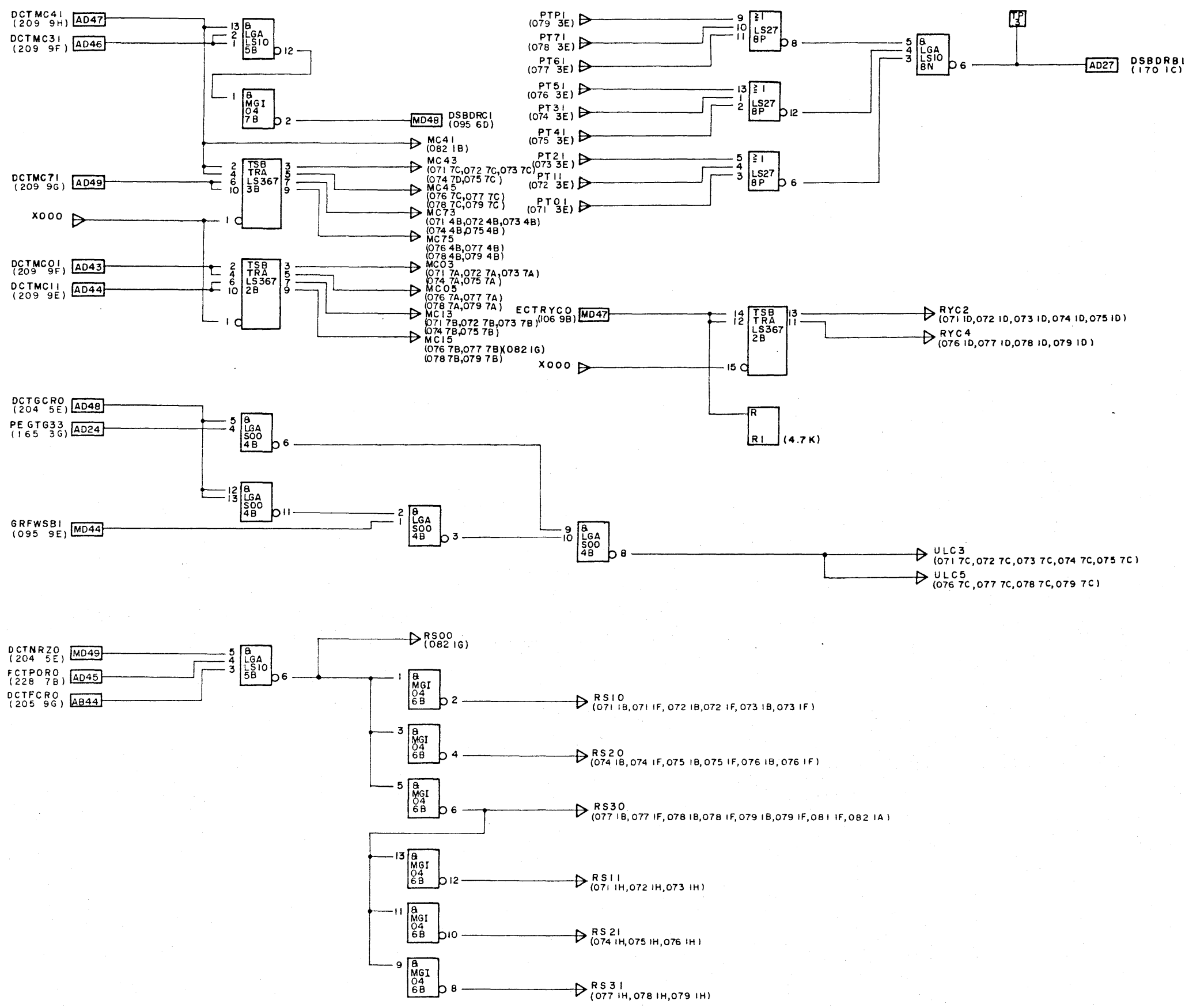
MTA16X FORMATTER
DESKEWING BUFFER
CIRCUIT DIAGRAM
9/12

134-110229-010-C

NEC SHT 9/

装置名

134-110229-010

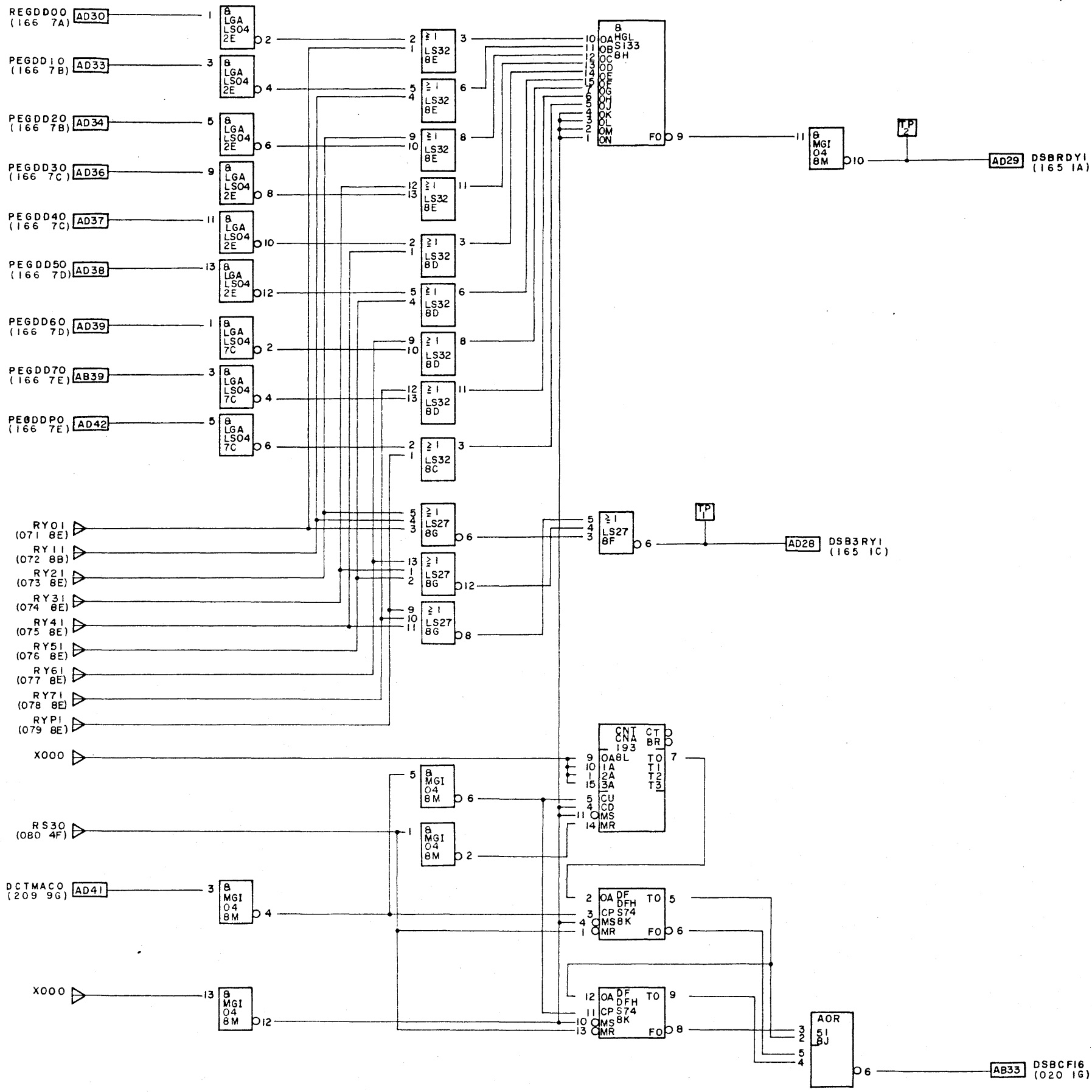


REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	D S B			
PKG LOCATION				
PKG NAME	G9JAM, G9MWW			
080				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今村	
MTA16X FORMATTER DESKEWING BUFFER CIRCUIT DIAGRAM 10/12				
134-110229-010-0				
NEC				SHT 10/

装置名

134-110229-010

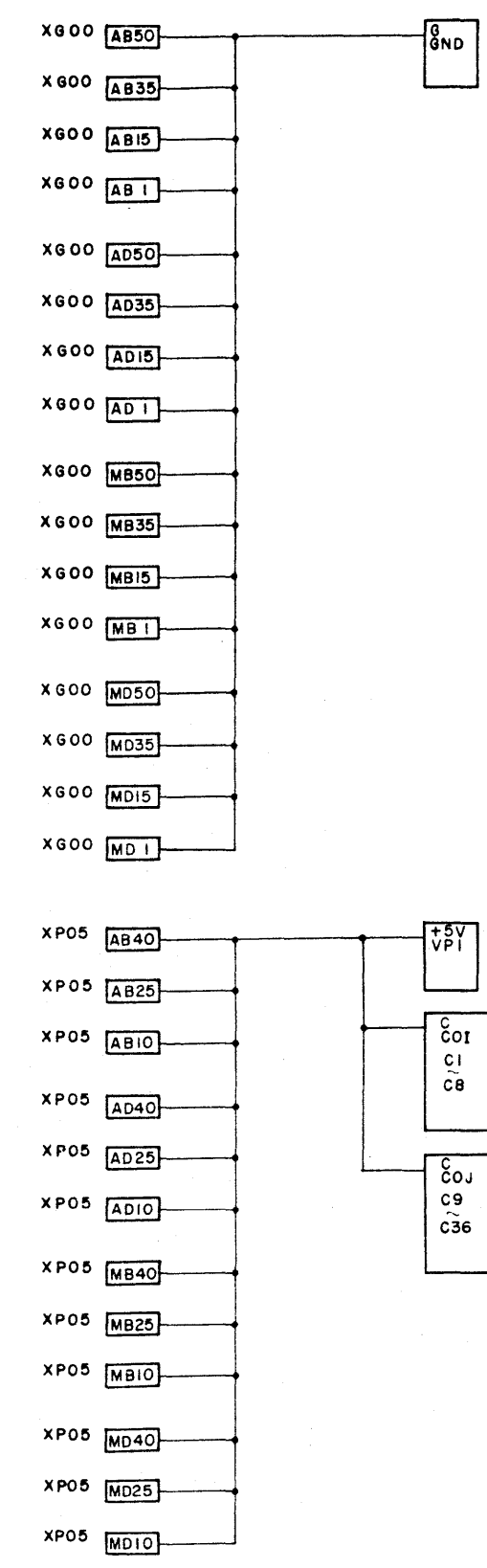
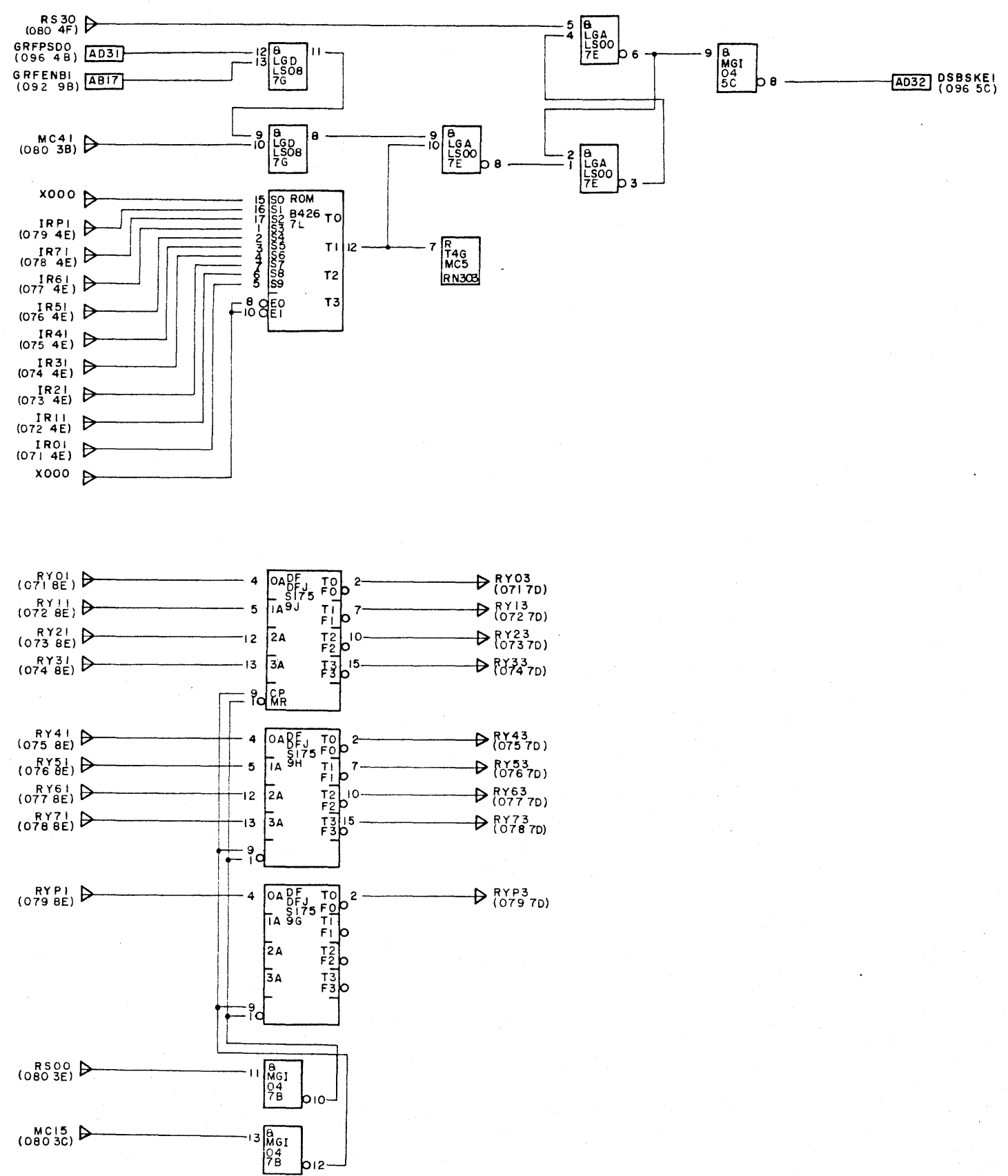


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	D S B		
PKG LOCATION			
PKG NAME	G9JAM, G9MWW		
081			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER DESKEWING BUFFER CIRCUIT DIAGRAM 11/12			
134-110229-010-			
NEC			SHT 11/

装置名

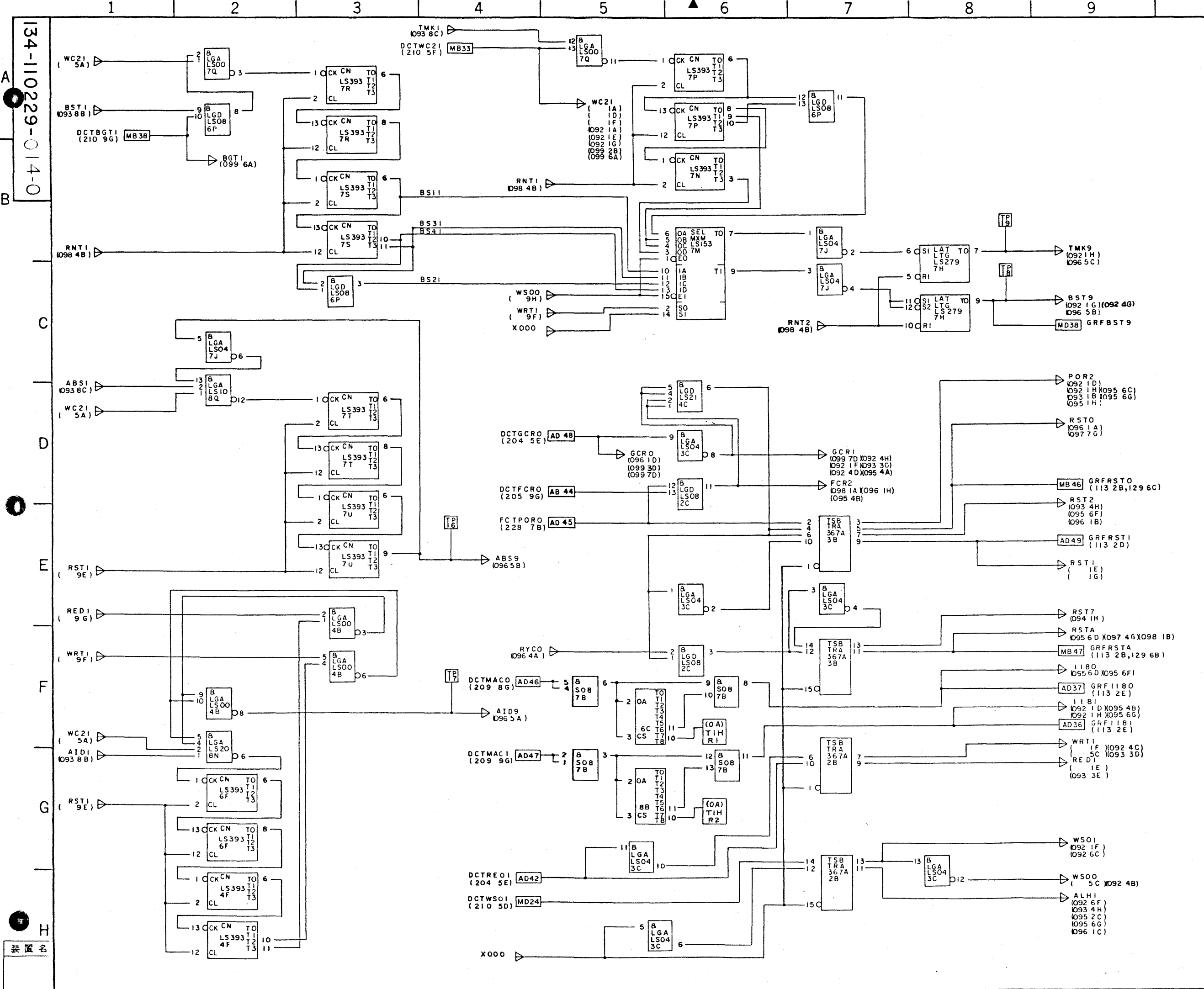
134-110229-010



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	D S B		
PKG LOCATION			
PKG NAME	G9JAM, G9MWW		
082			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山		今村
	口		村
MTA16X FORMATTER DESKEWING BUFFER CIRCUIT DIAGRAM 12/12			
134-110229-010			SHT 12/12
NEC			

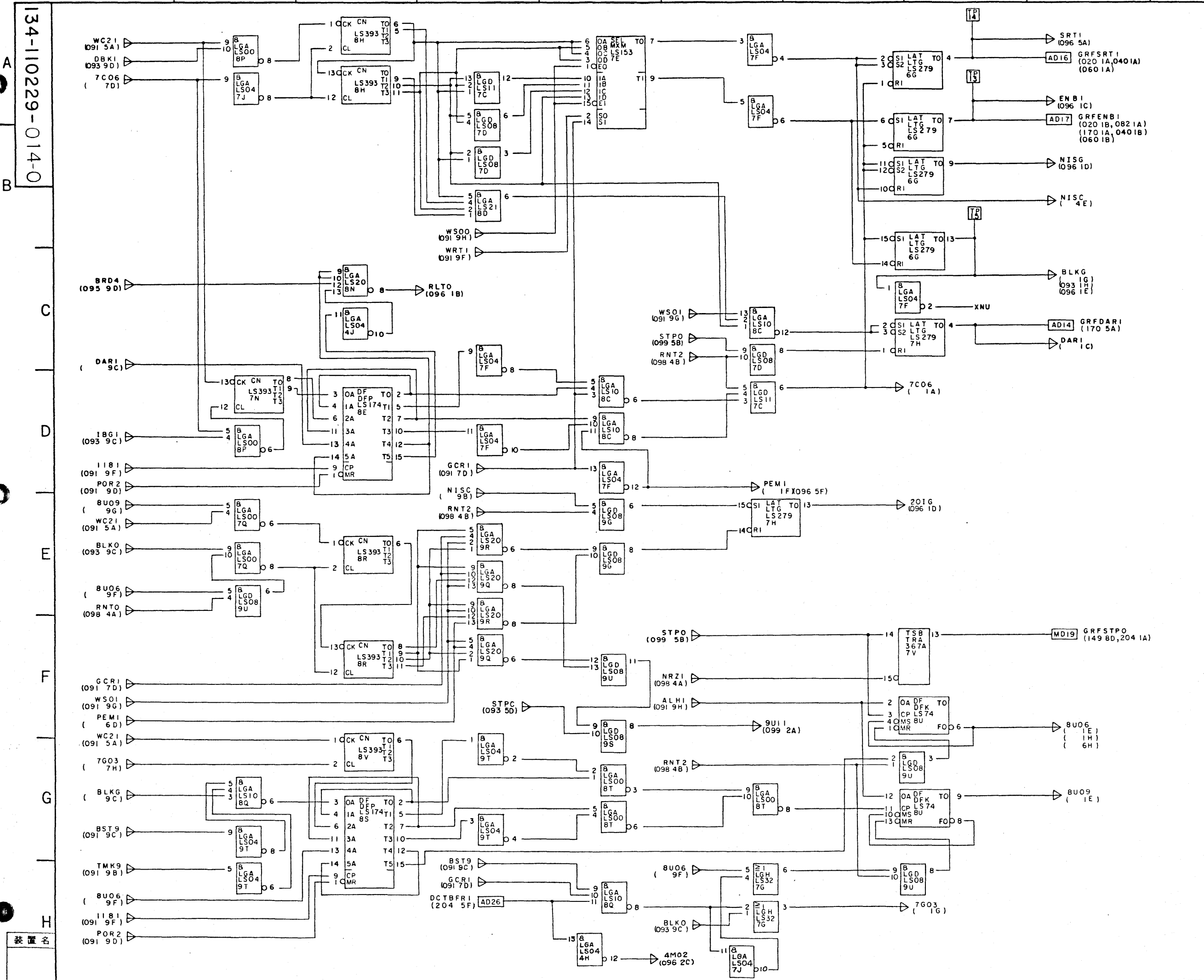
装置名



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

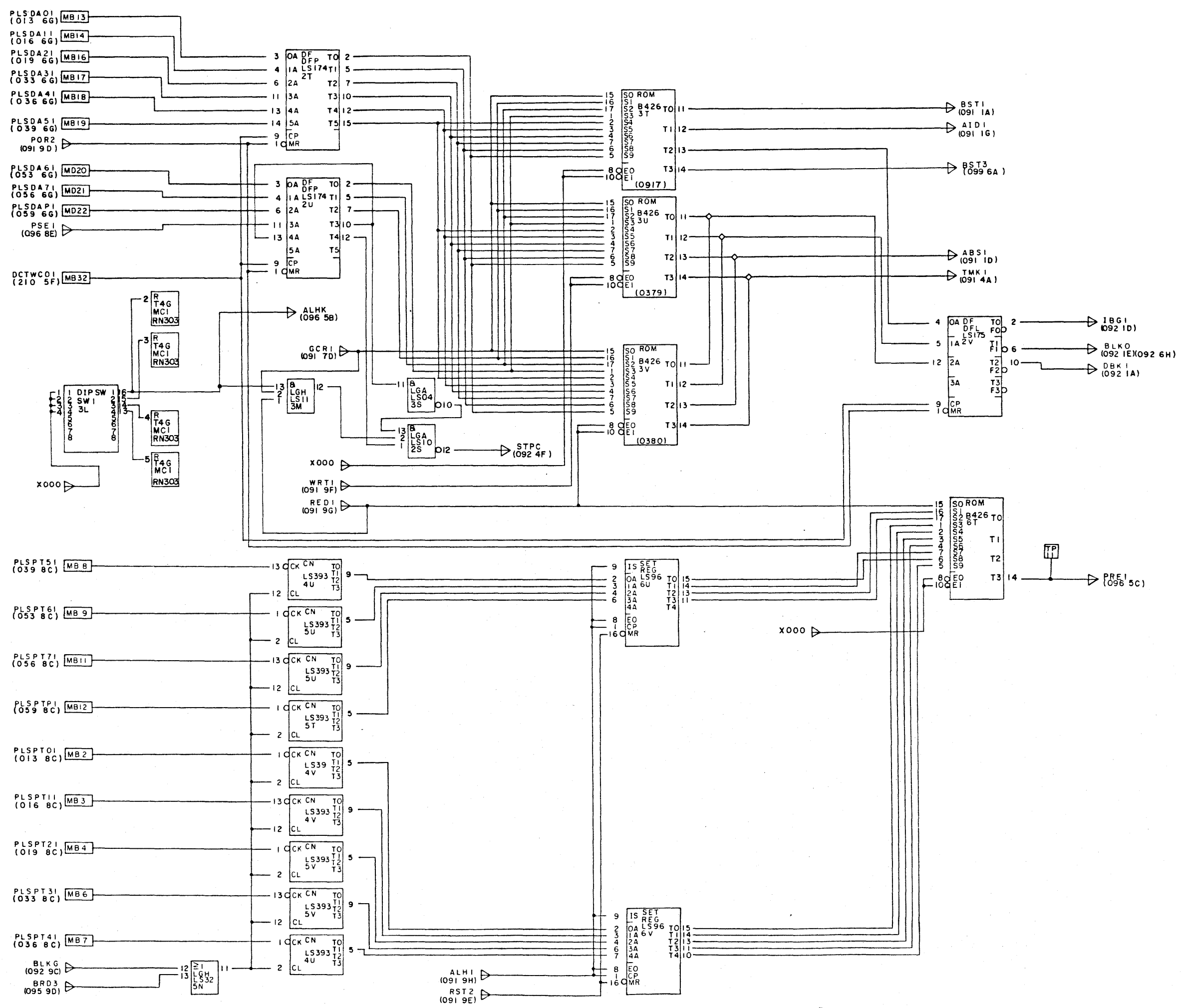
DWG ABBR	G R F			
PKG LOCATION				
PKG NAME	G9QWS			
091				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	村
MTA16X FORMATTER GCR FORMAT CONTROL IN READ CIRCUIT DIAGRAM 1/9				
134-110229-014-0				SHT 1/9
NEC				

134-110229-014-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
DWG ABBR		G R F	
PKG LOCATION			
PKG NAME		G9QWS	
092			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽		今
	賀		村
MTA16X FORMATTER GCR FORMAT CONTROL IN READ CIRCUIT DIAGRAM 2/9			
134-110229-014-0			
NEC			SHT 2/

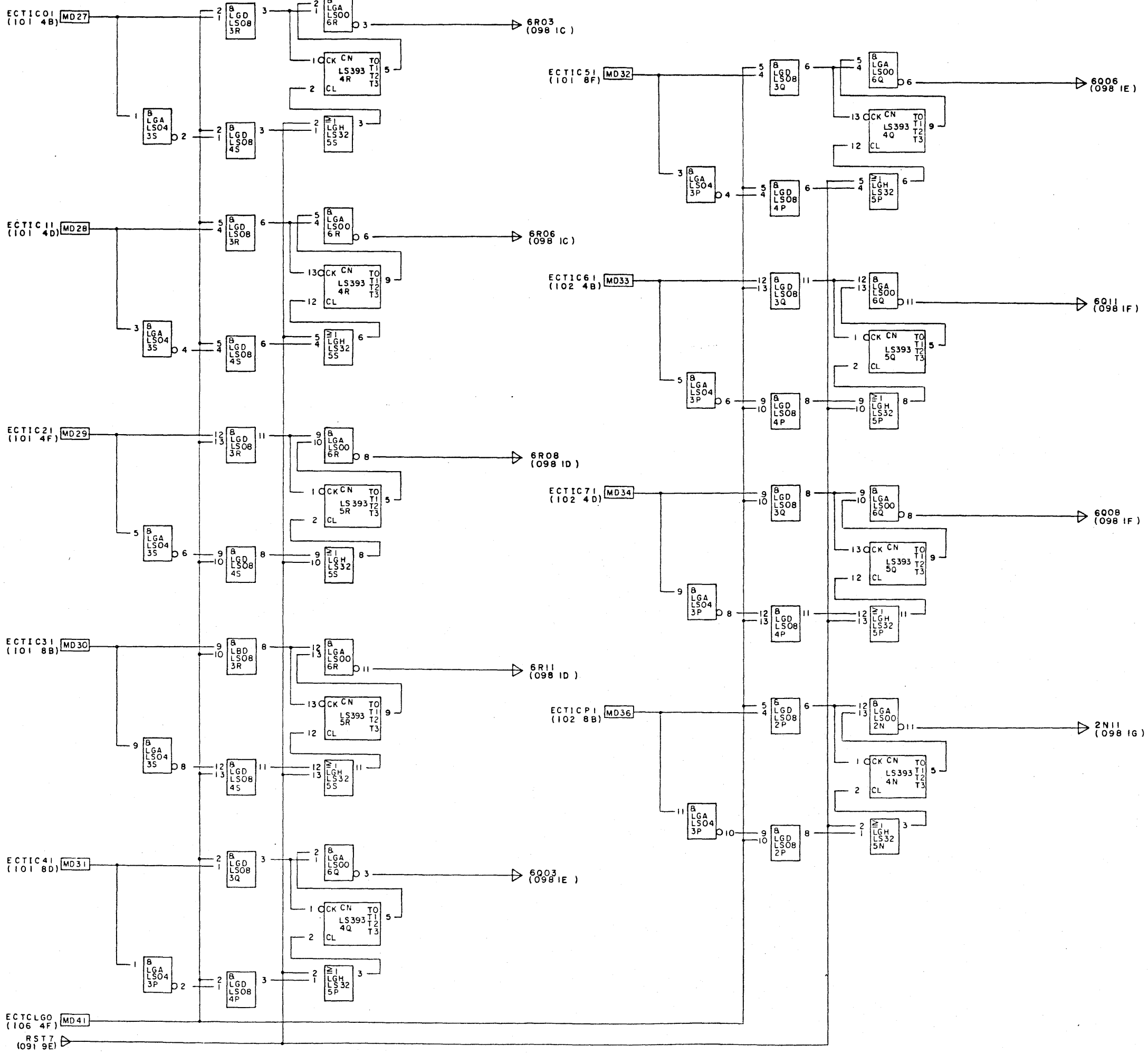
134-110229-014-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

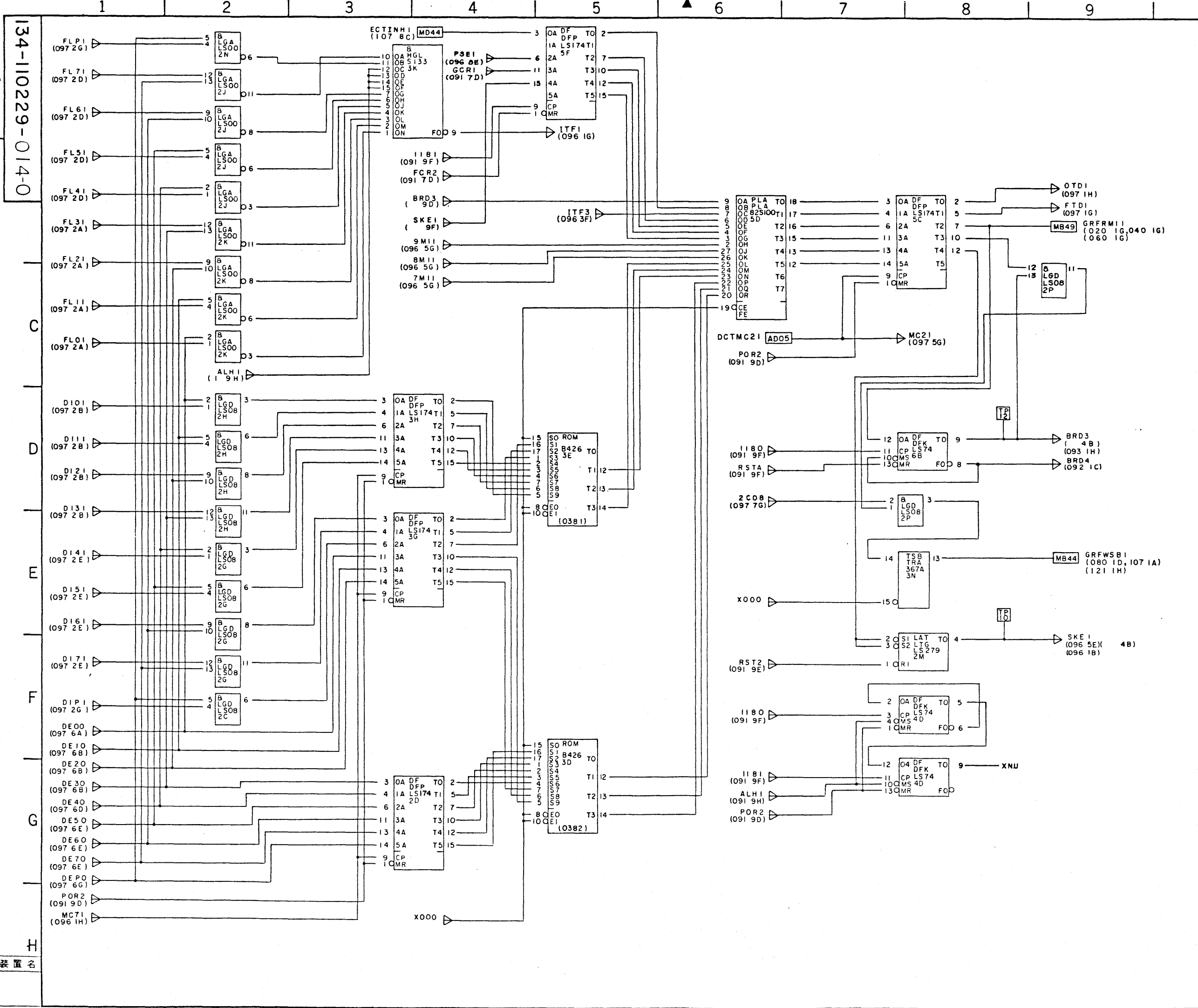
DWG ABBR	G R F				
PKG LOCATION					
PKG NAME	G9QWS				
093					
NEXT SPEC					
DRAFT	ENG	CHK	APP	ISSUE	
	羽		今		
	賀		村		
MTA16X FORMATTER GCR FORMAT CONTROL IN READ CIRCUIT DIAGRAM 3/9					
134-110229-014-0				SHT	3/
NEC					

134-110229-014-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G R F			
PKG LOCATION				
PKG NAME	G9QWS			
094				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	
MTA16X FORMATTER GCR FORMAT CONTROL IN READ CIRCUIT DIAGRAM 4/9				
134-110229-014-0				
NEC				SHT 4/

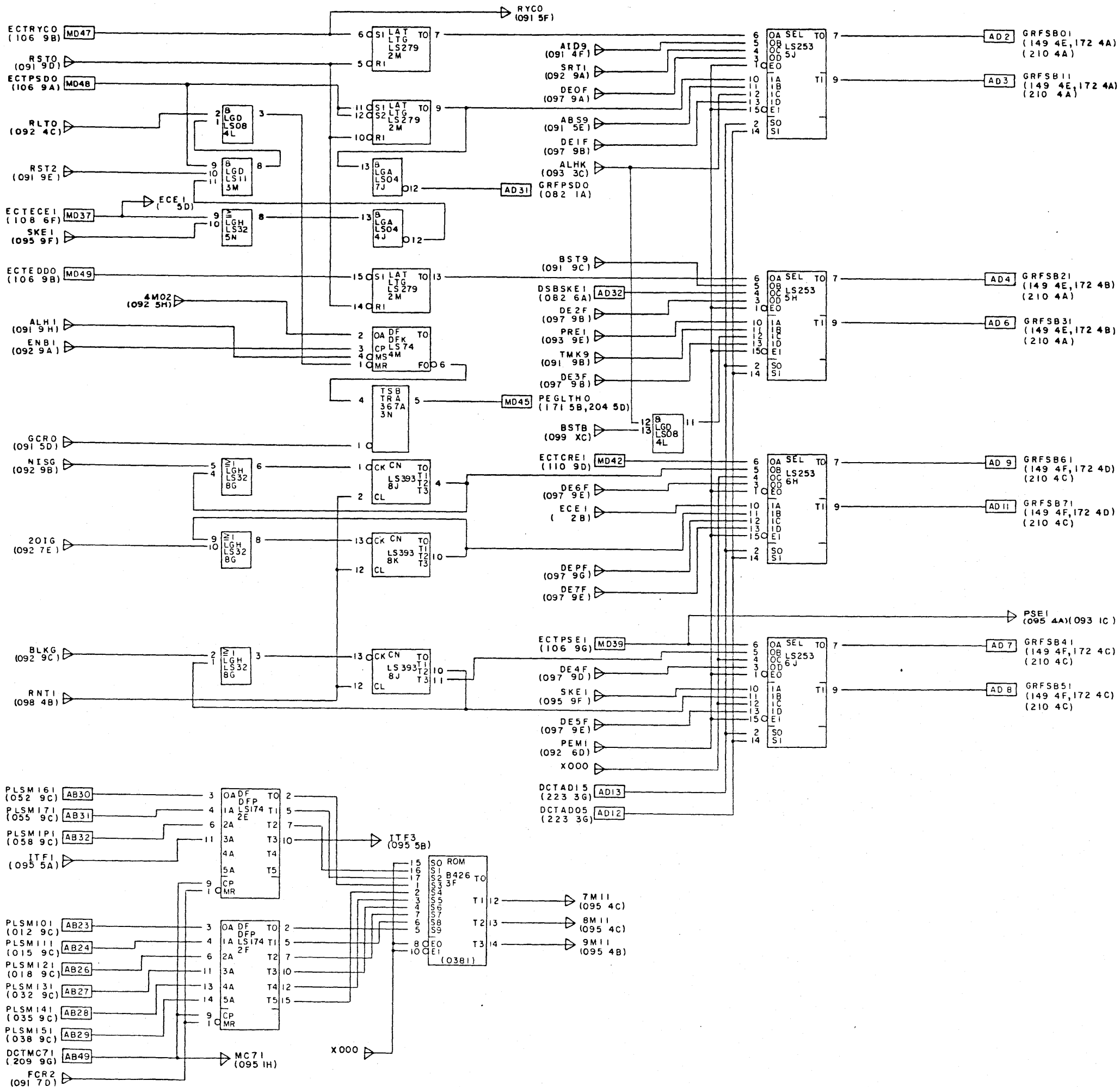


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G R F			
PKG LOCATION				
PKG NAME	G9QWS			
095				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	
MTA16X FORMATTER GCR FORMAT CONTROL IN READ CIRCUIT DIAGRAM 5/9				
134-110229-014-0				
NEC				SHT 5/

134-110229-014-0

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REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

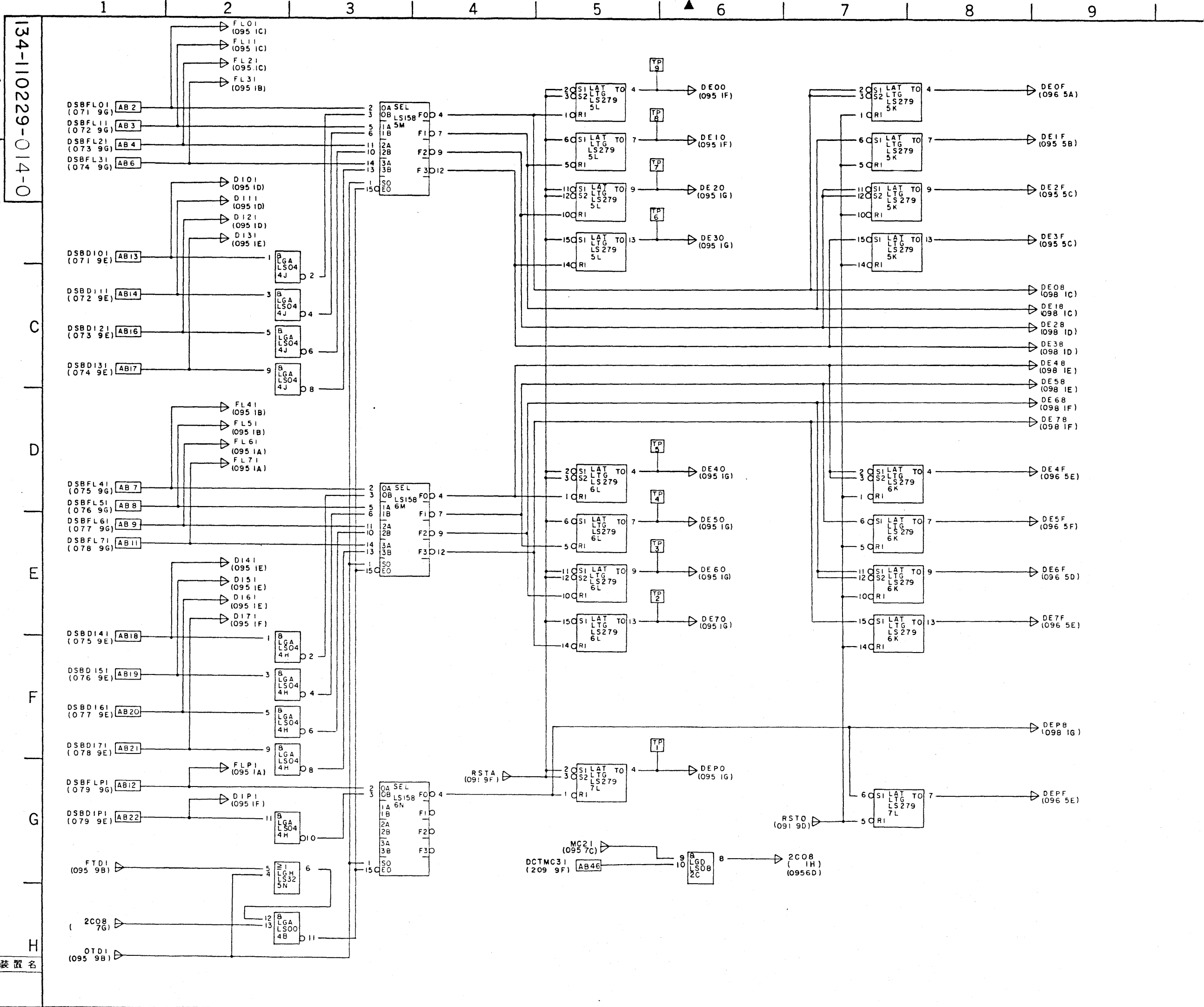
DWG ABBR	GRF
PKG LOCATION	
PKG NAME	G9QWS
096	

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	

MTA16X FORMATTER
GCR FORMAT CONTROL
IN READ
CIRCUIT DIAGRAM
6/9

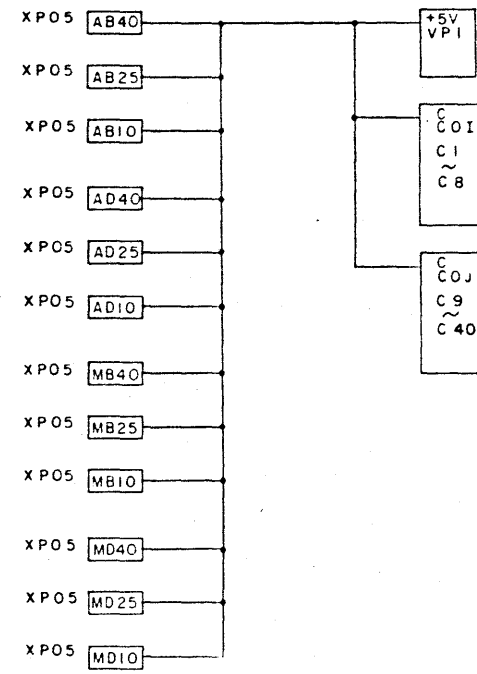
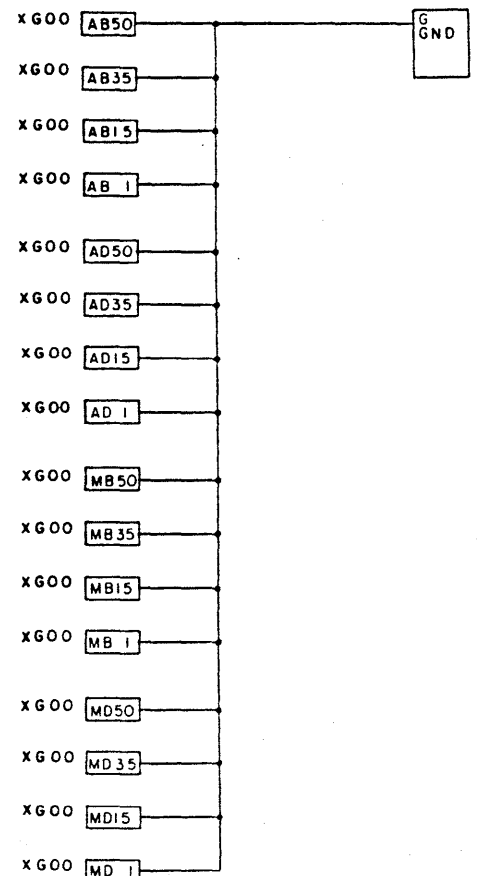
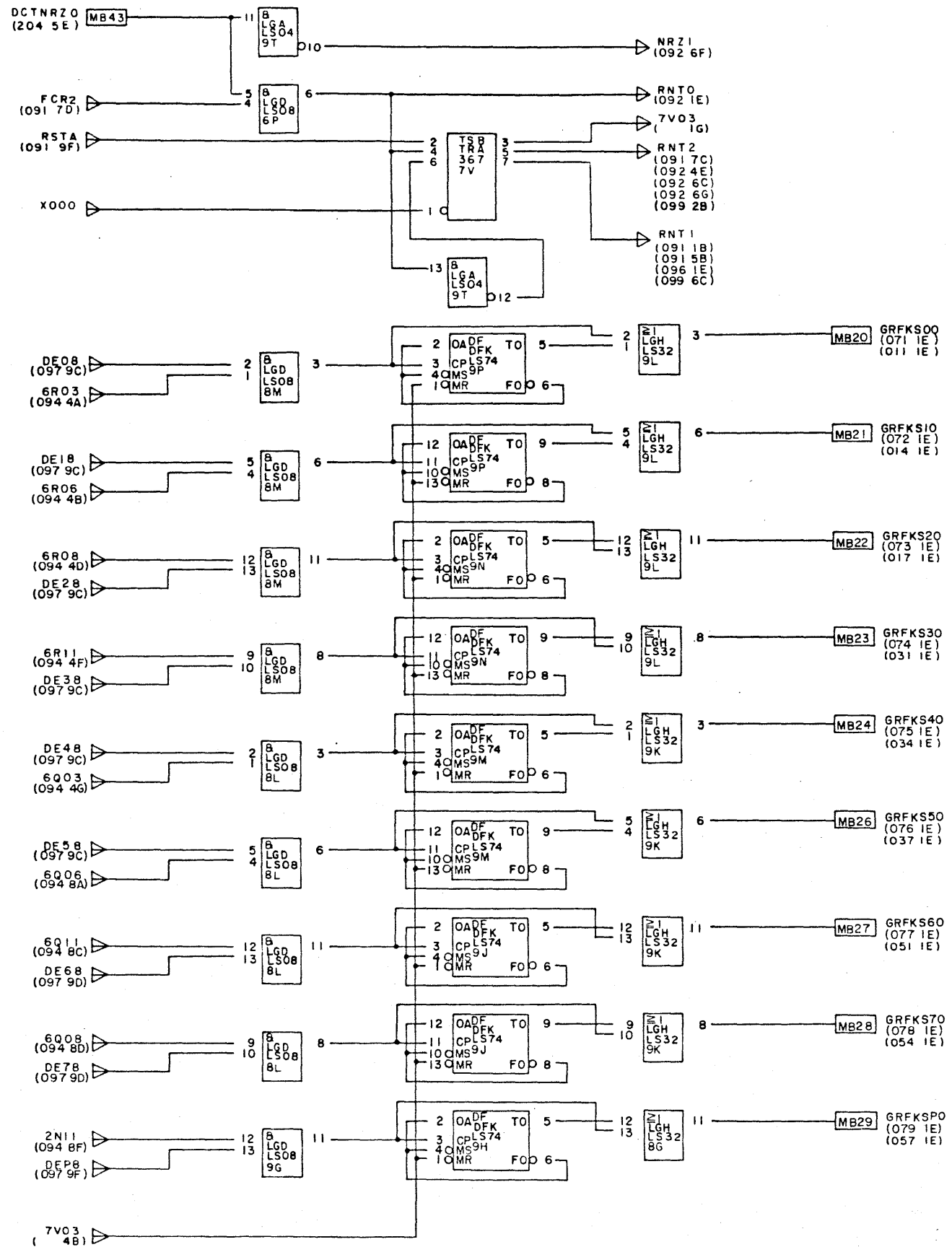
134-110229-014-0

NEC SHT 6/



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	
DWG ABBR		G R F	
PKG LOCATION			
PKG NAME		G9QWS	
097			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTA16X FORMATTER GCR FORMAT CONTROL IN READ CIRCUIT DIAGRAM 7/9			
134-110229-014-0			
NEC			SHT 7/

134-110229-014-0

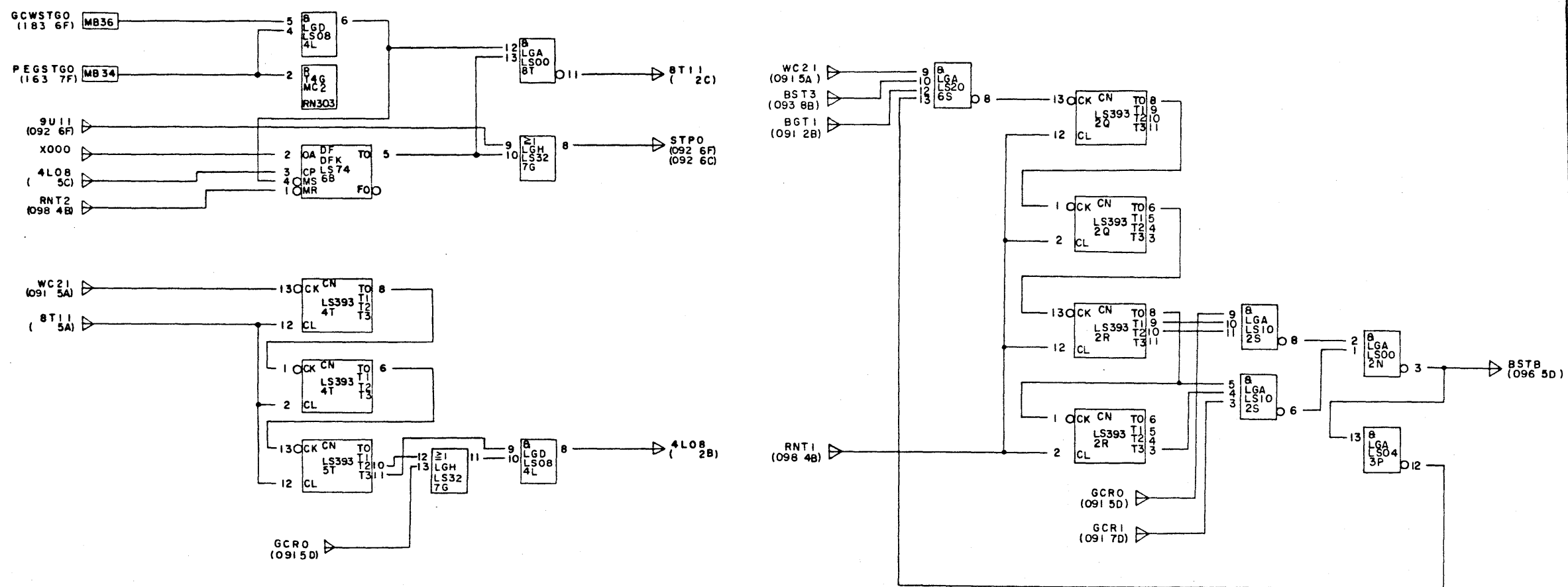


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G R F				
PKG LOCATION					
PKG NAME	G9QWS				
098					
NEXT SPEC					
DRAFT	ENG	CHK	APP	ISSUE	
	羽		今		
	賀		村		
MTA16X FORMATTER GCR FORMAT CONTROL IN READ CIRCUIT DIAGRAM 8/9					
134-110229-014-0					
NEC				SHT	8/

装置名

134-110229-014-0



REV	COMP	DESCRIPTION (SC)	APP
-----	------	------------------	-----

1	0	55.5.5	
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DWG ABBR	G R F
PKG LOCATION	
PKG NAME	G9QWS

099

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

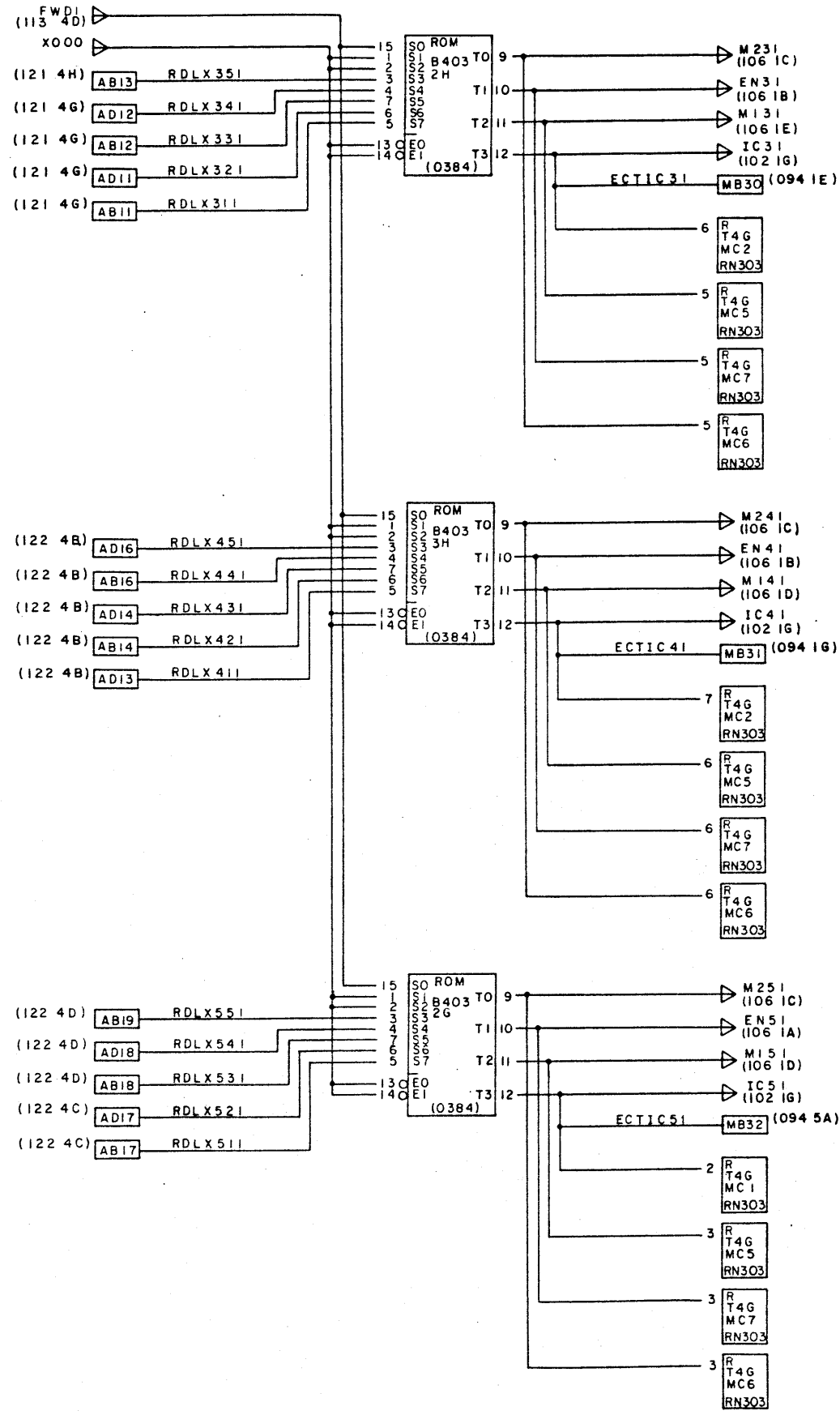
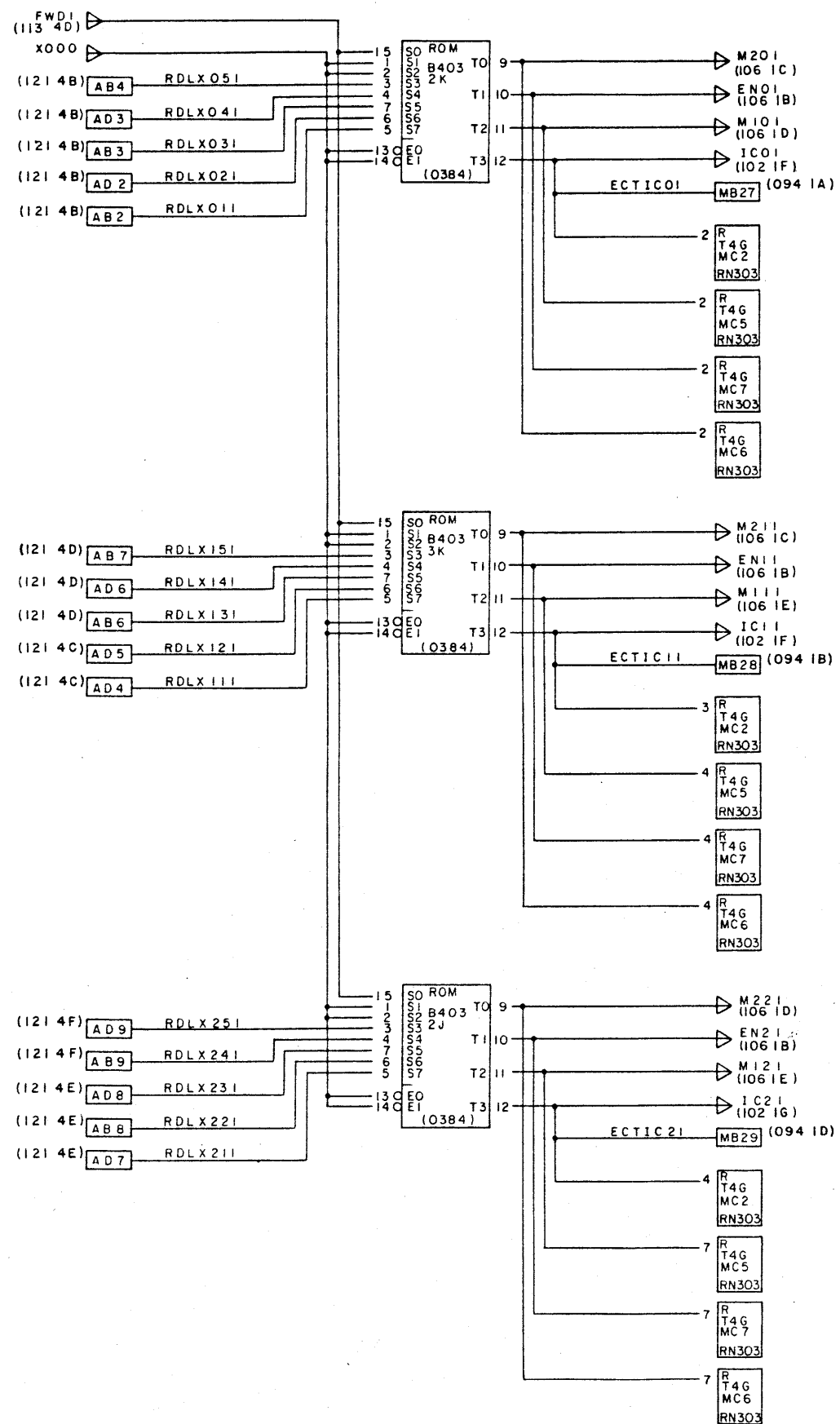
MTA16X FORMATTER
GCR FORMAT CONTROL
IN READ
CIRCUIT DIAGRAM
9/9

134-110229-014-0

NEC SHT 9/9

装置名

134-110229-008-0

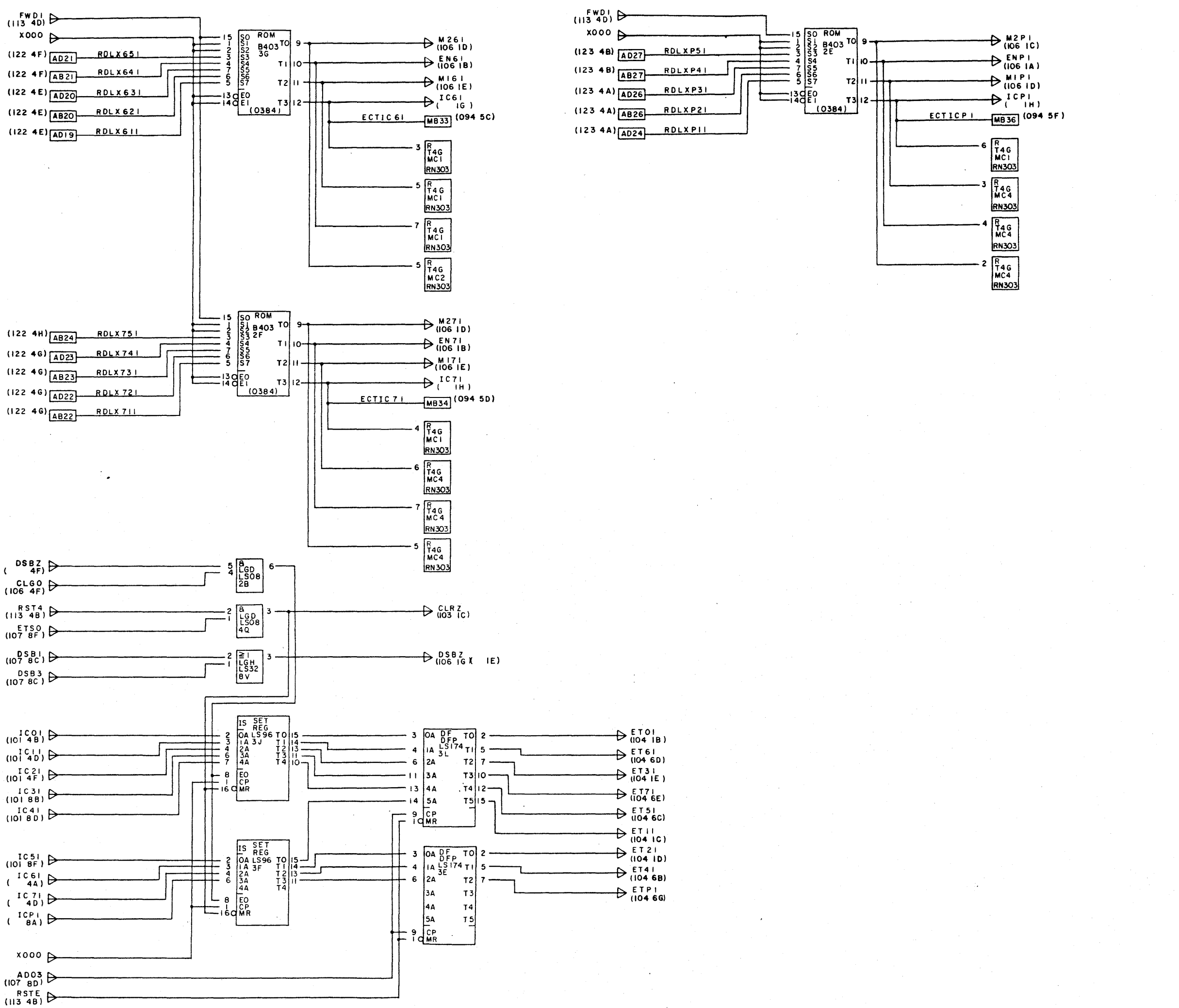


REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	
2	0		大橋

DWG ABBR	E C T			
PKG LOCATION				
PKG NAME	G9JAP,G9MWS			
101				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER E C C CONTROL CIRCUIT DIAGRAM 1/14				
134-110229-008-0				
NEC				SHT 1/14

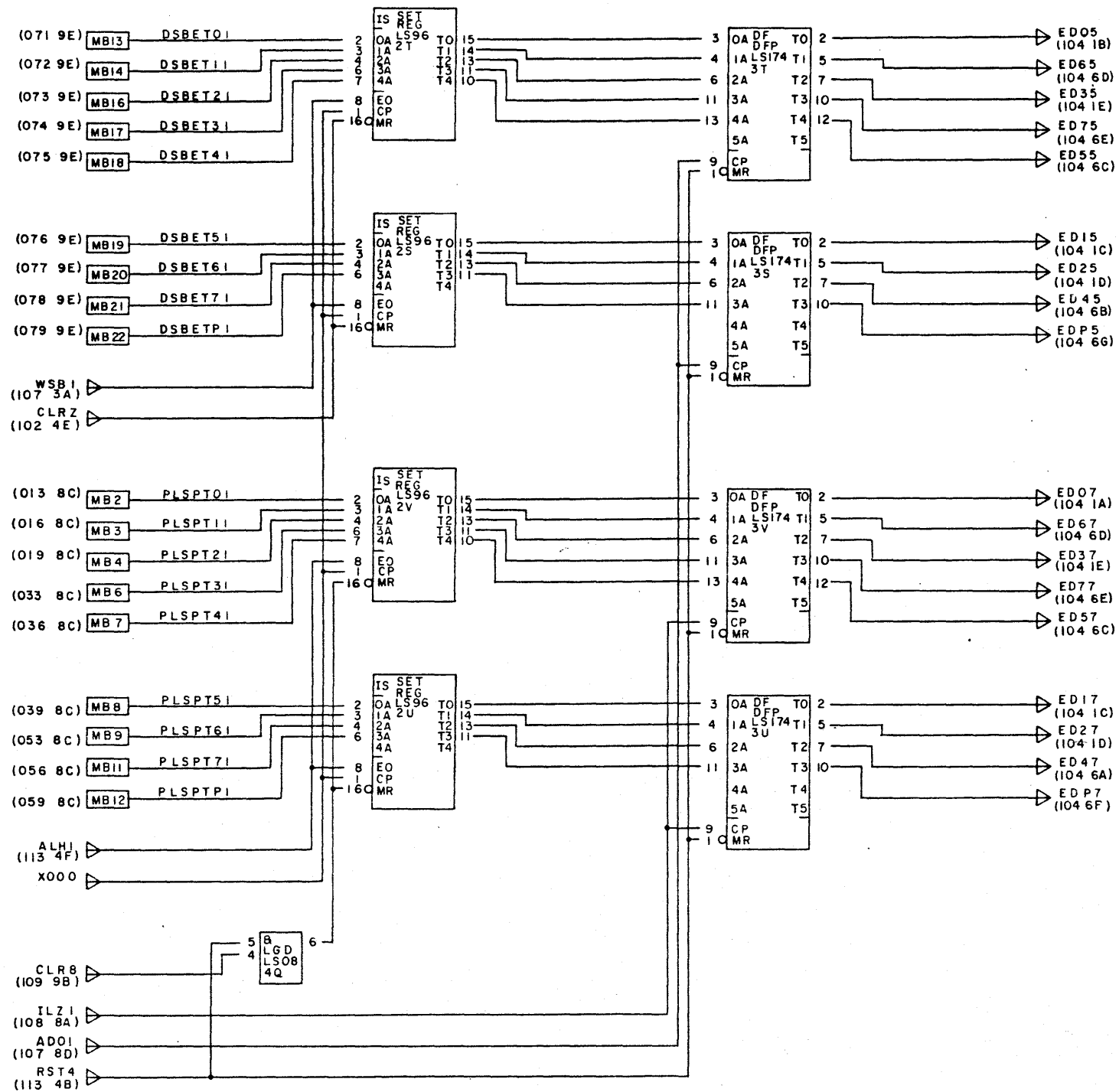
134-110229-008-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	E C T			
PKG LOCATION				
PKG NAME	G9JAP, G9MWS			
102				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	
MTA16X FORMATTER ECC CONTROL CIRCUIT DIAGRAM 2/14				
134-110229-008-0				
NEC				SHT 2/

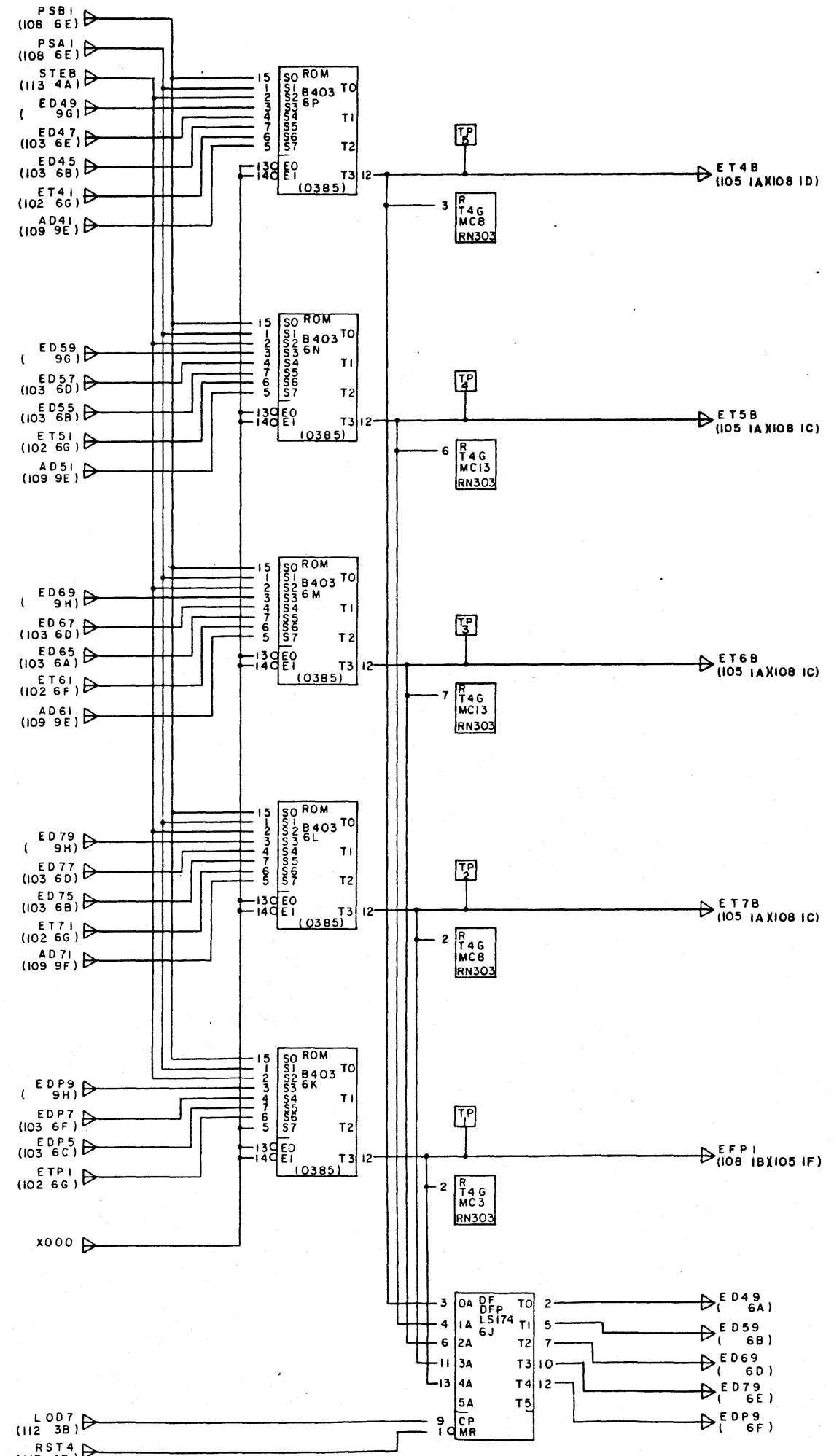
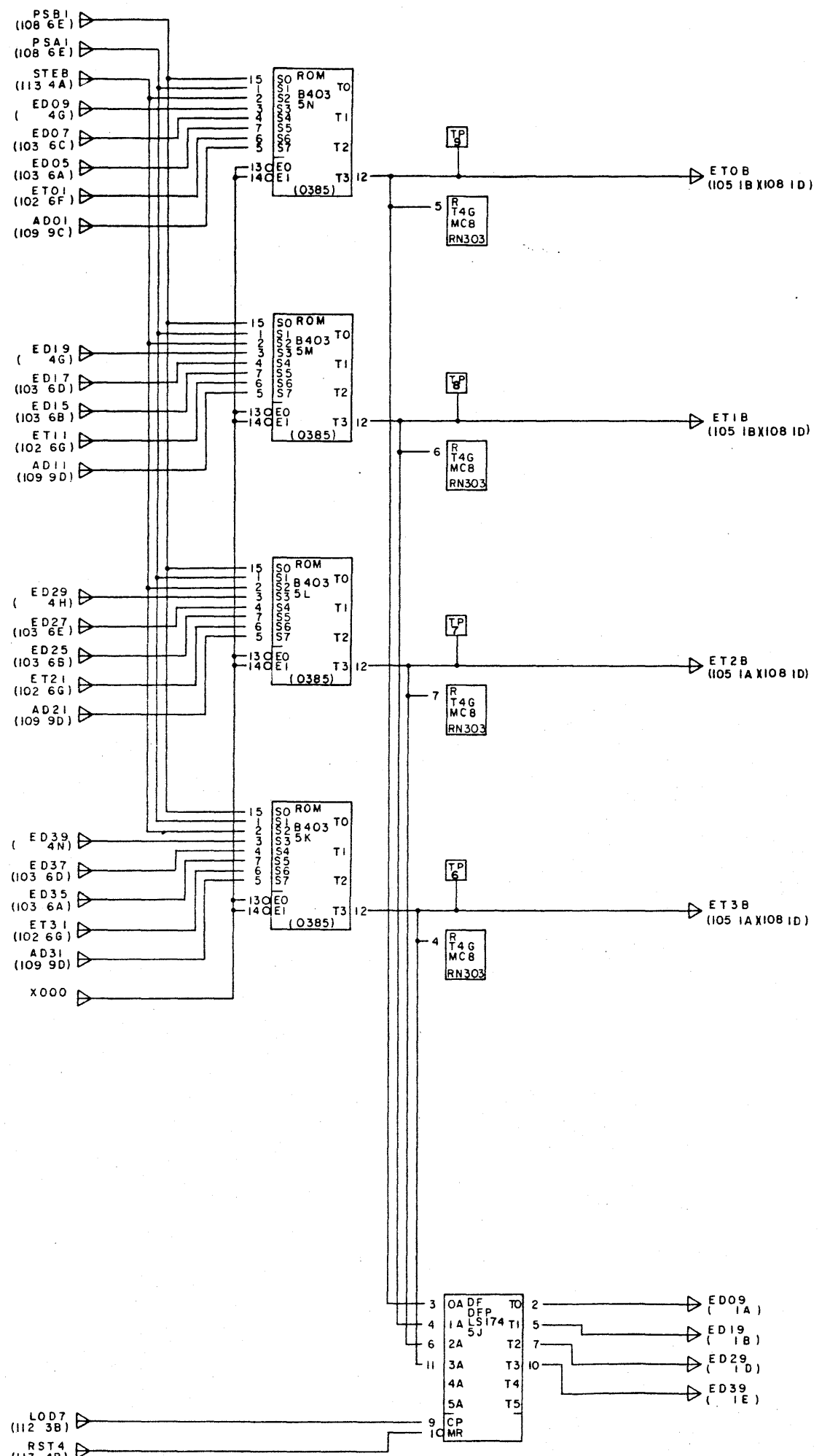
134-110229-008-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

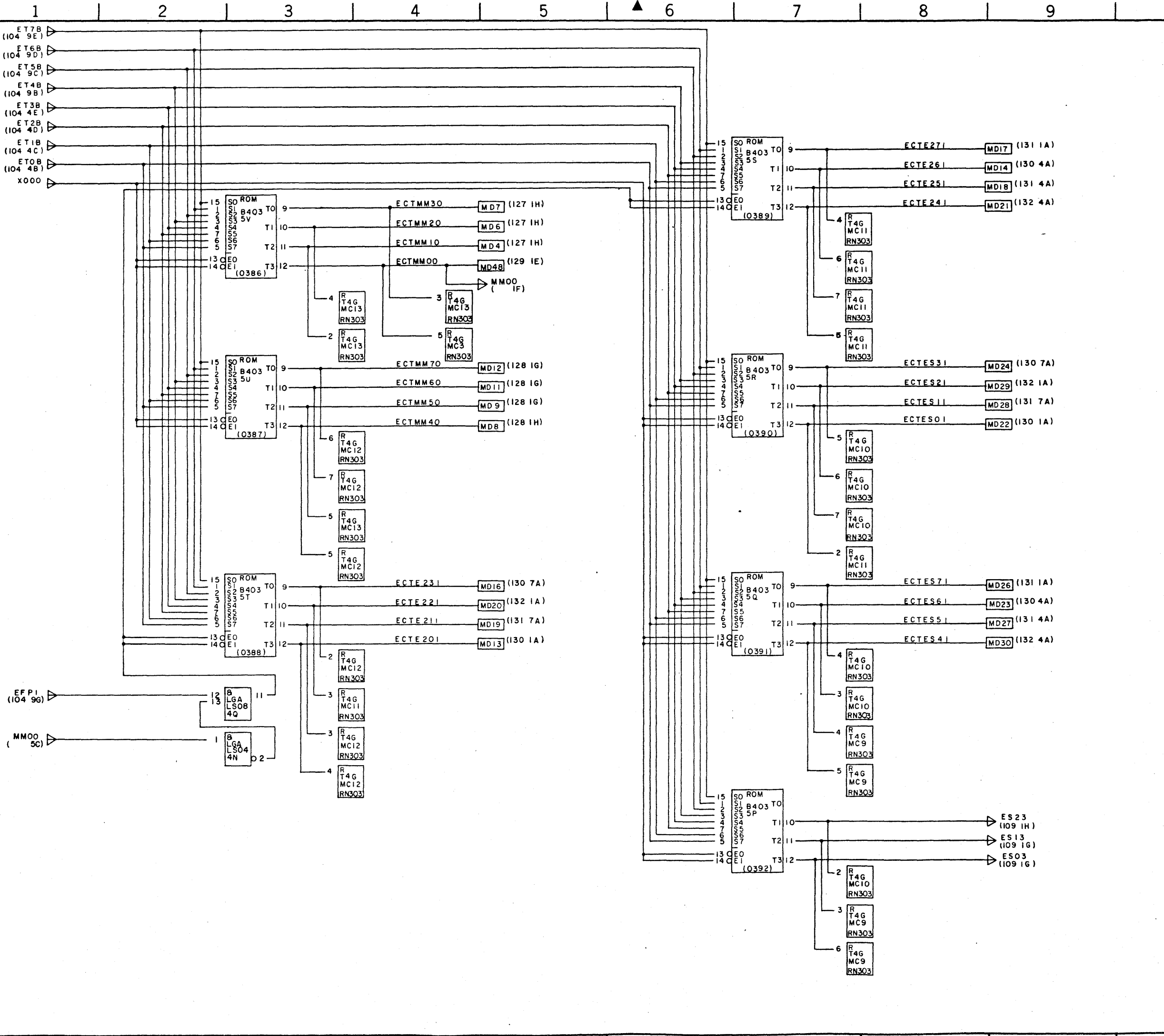
DWG ABBR	E C T		
PKG LOCATION			
PKG NAME	G9JAP,G9MWS		
103			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽		今
	賀		村
MTA16X FORMATTER ECC CONTROL CIRCUIT DIAGRAM 3/14			
134-110229-008-0			
NEC			SHT 3/

134-110229-008-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
DWG ABBR		E C T	
PKG LOCATION			
PKG NAME		G9JAP, G9MWS	
104			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTA16X FORMATTER ECC CONTROL CIRCUIT DIAGRAM 4/14			
134-110229-008-0			
NEC			SHT 4/

134-110229-008-0

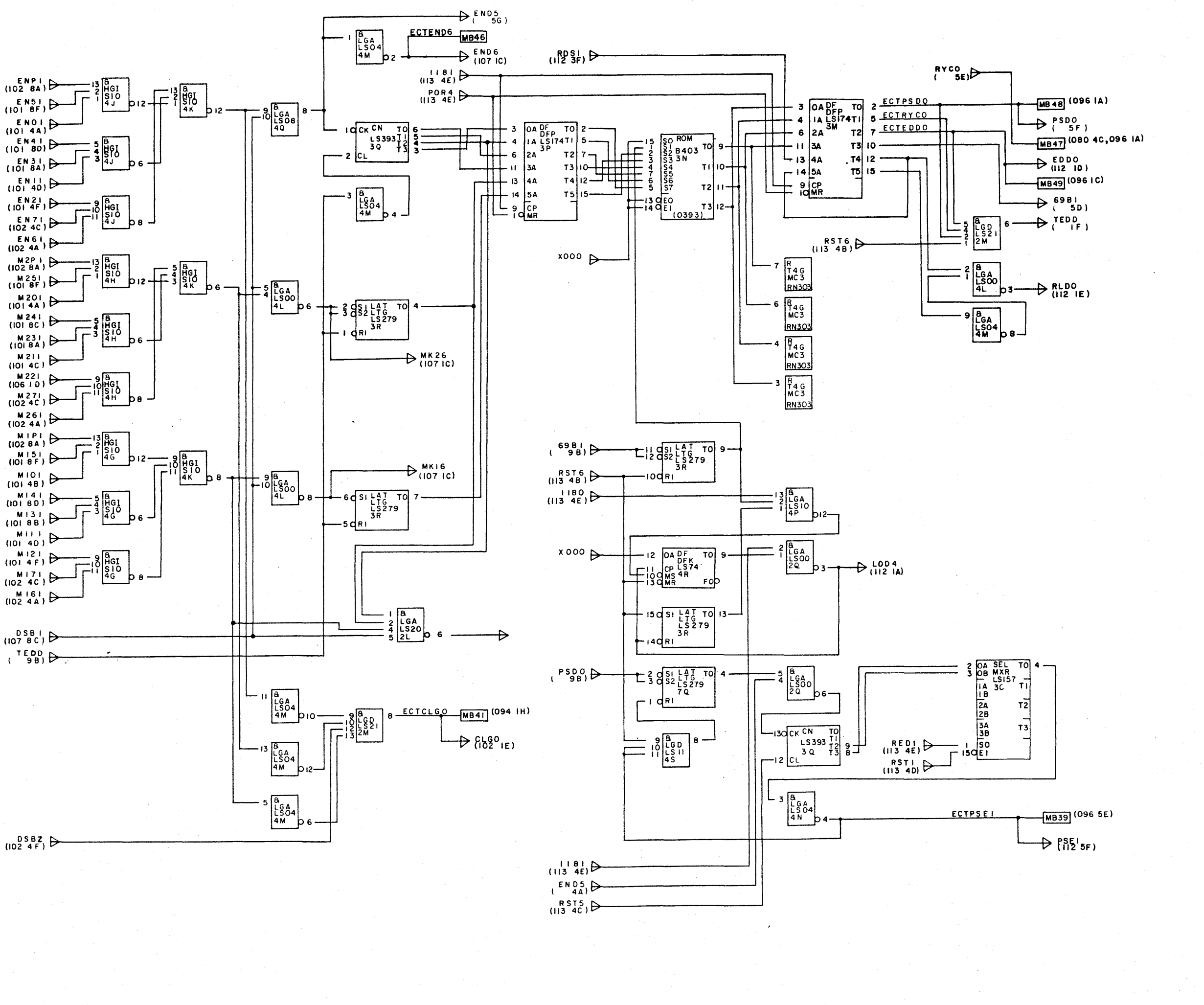


REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	E C T		
PKG LOCATION			
PKG NAME	G9JAP,G9MWS		
105			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽		今
	賀		村
MTA16X FORMATTER ECC CONTROL CIRCUIT DIAGRAM 5/14			
134-110229-008-0			
NEC			SHT 5/

装置名

134-110229-008-0

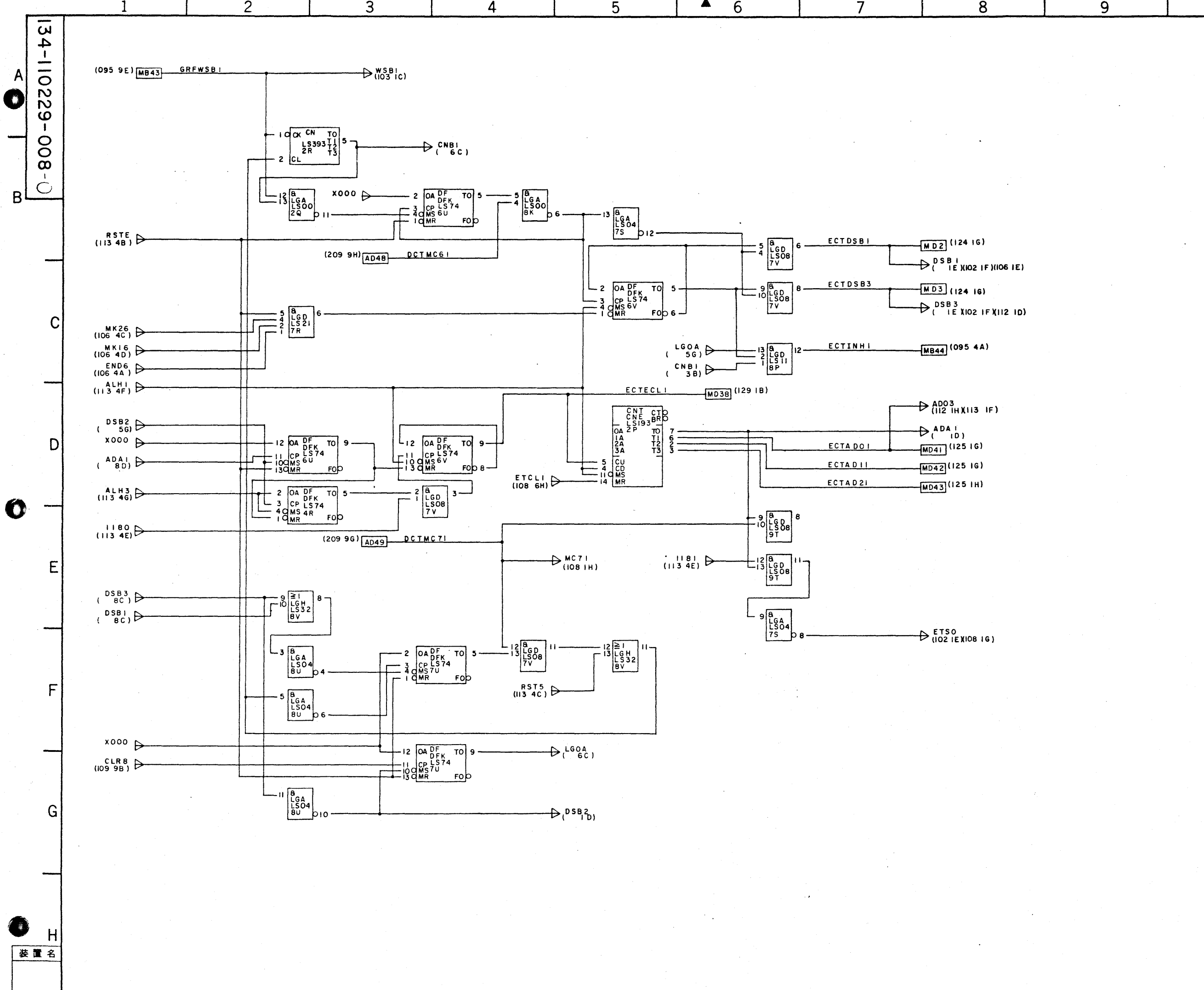


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	ECT			
PKG LOCATION				
PKG NAME	G9JAP, G9MWS			
106				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER ECC CONTROL CIRCUIT DIAGRAM 6/14				
134-110229-008-0				
NEC				SHT 6/

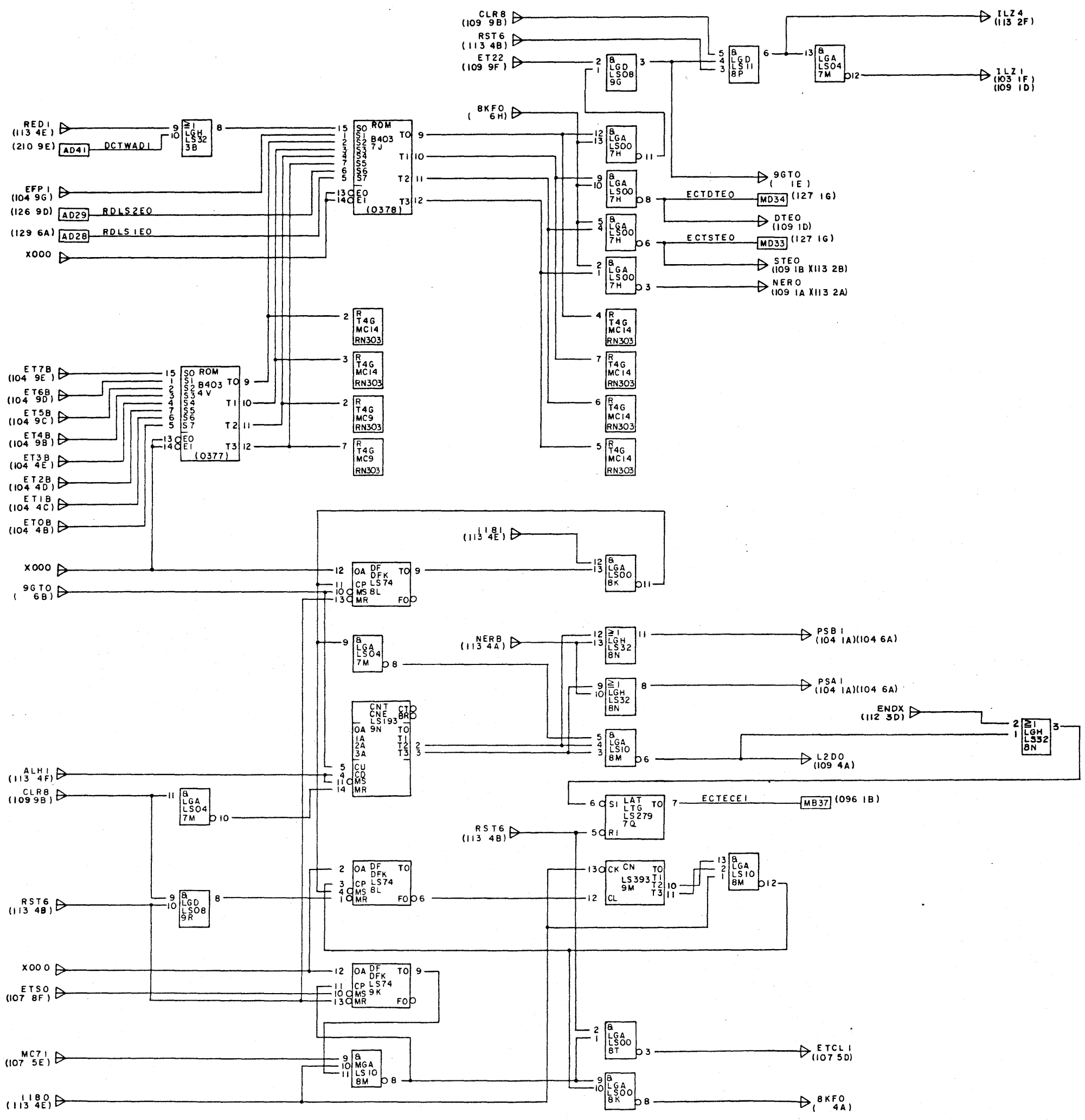
装置名



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	E C T			
PKG LOCATION				
PKG NAME	G9JAP, G9MW S			
107				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽 賀		今 村	
MTA16X FORMATTER E C C CONTROL CIRCUIT DIAGRAM 7/14				
134-110229-008-0				
NEC				SHT 7/

134-110229-008-0

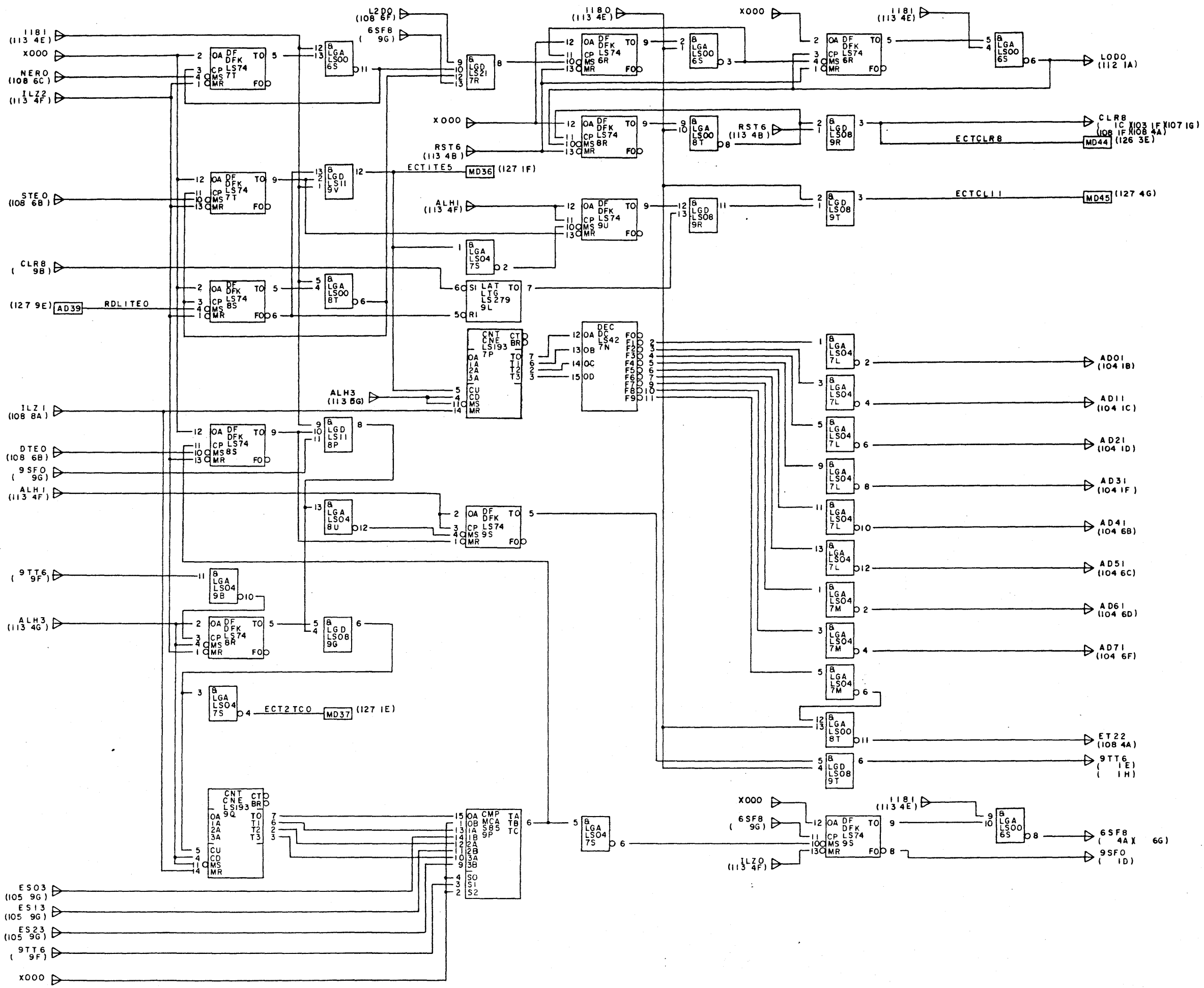


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	E C T		
PKG LOCATION			
PKG NAME	G9JAP, G9MWS		
108			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTA16X FORMATTER E C C CONTROL CIRCUIT DIAGRAM 8/14			
134-110229-008-0			
NEC			SHT 8/

装置名

134-110229-008

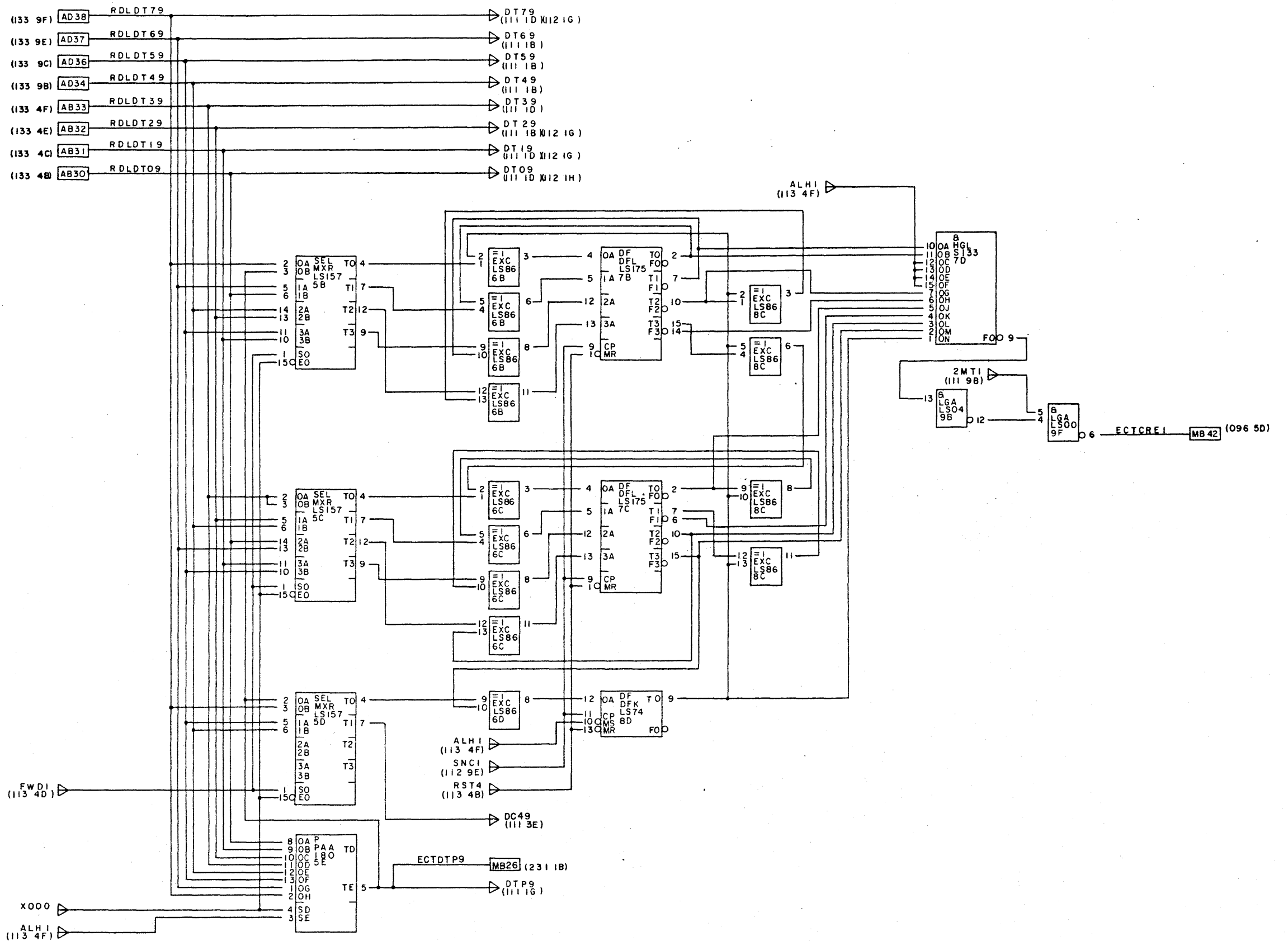


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	E C T		
PKG LOCATION			
PKG NAME	G9JAP, G9MWS		
109			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽		今
	賀		村
MTA16X FORMATTER E C C CONTROL CIRCUIT DIAGRAM 9/14			
134-110229-008-0			
NEC			SHT 9/

装置名

134-110229-008-0



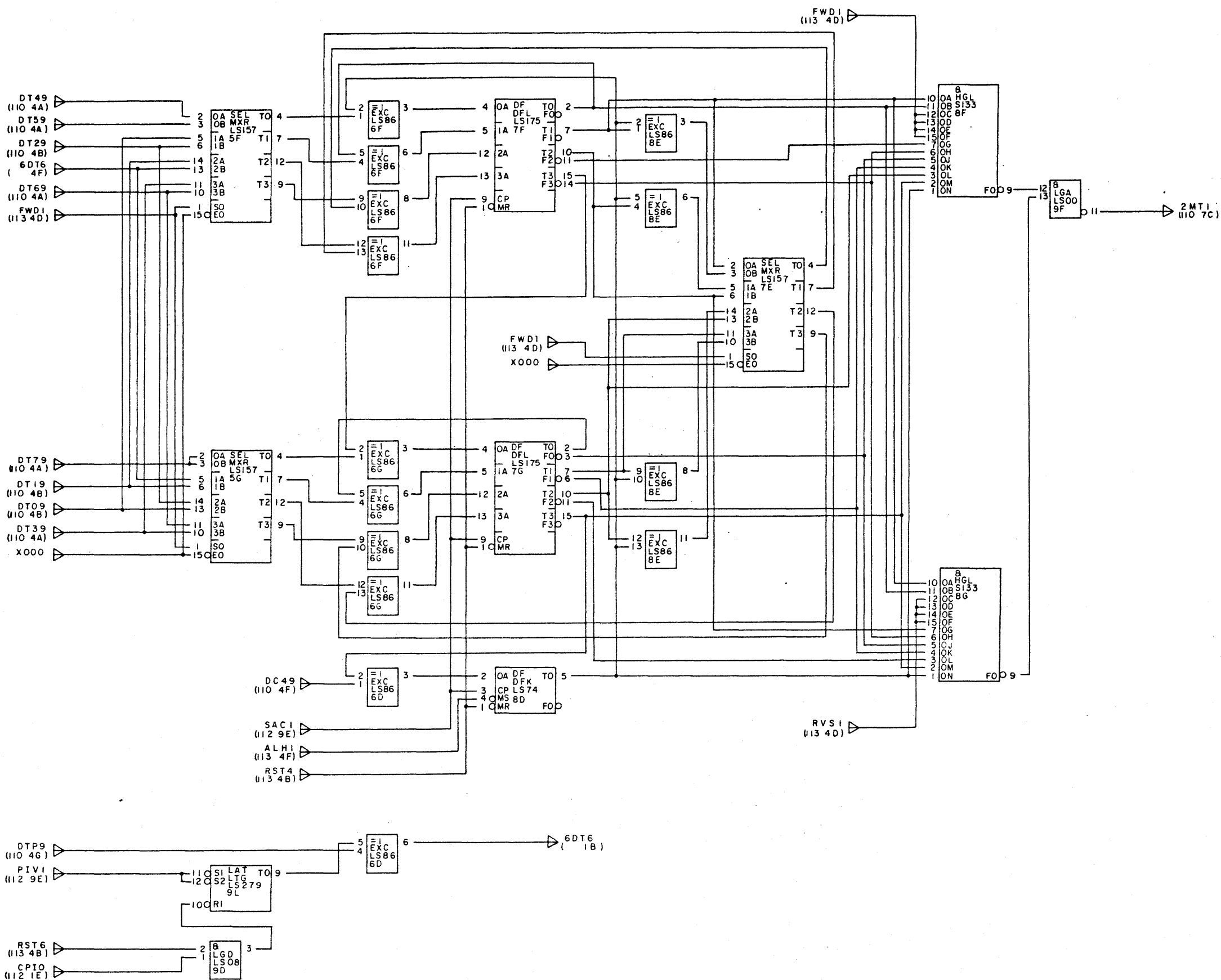
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	E C T		
PKG LOCATION			
PKG NAME	G9JAP,G9MWS		
110			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTA16X FORMATTER ECC CONTROL CIRCUIT DIAGRAM 10/14			
134-110229-008-0			
NEC			SHT 10/

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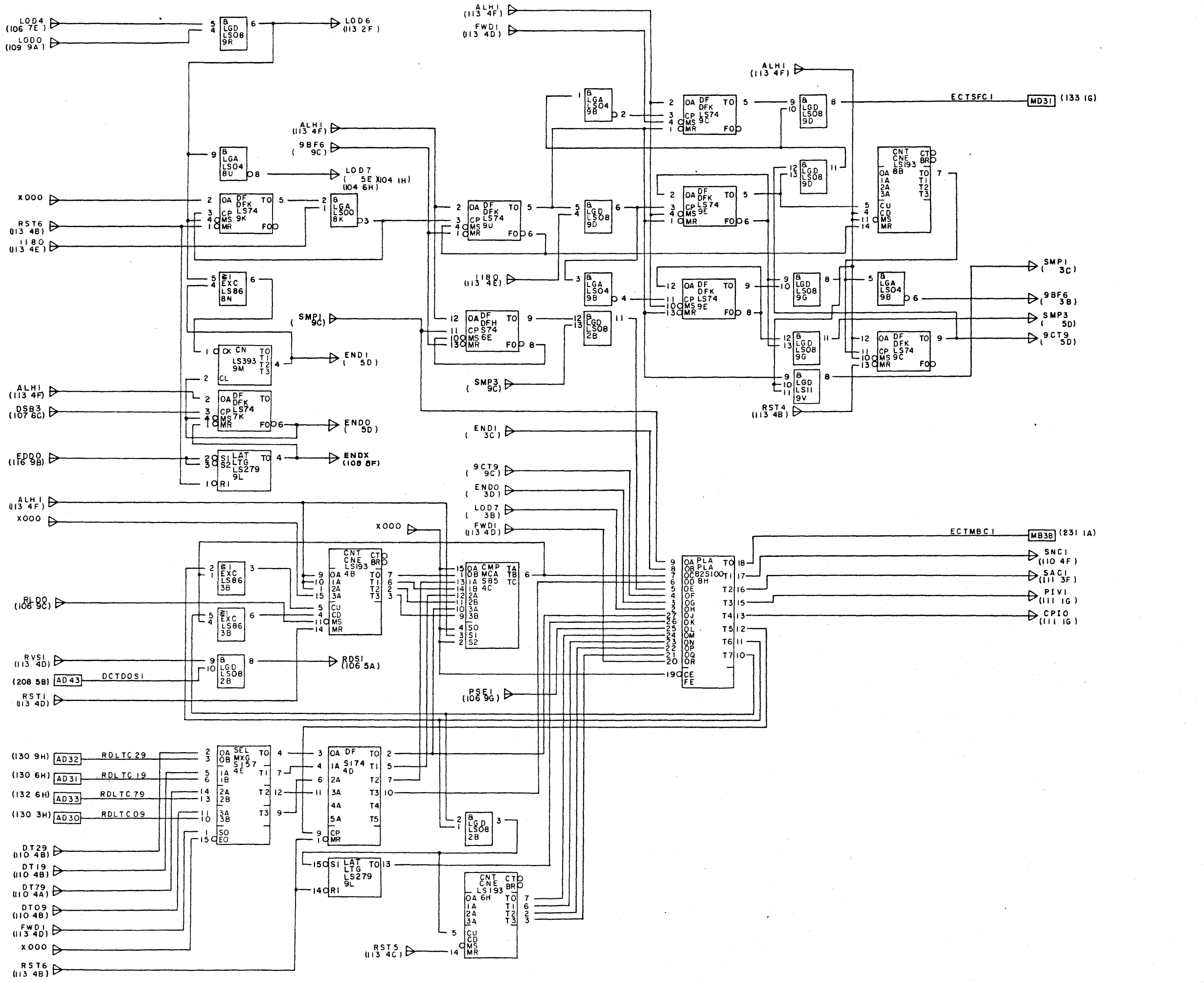
134-110229-008-0



DWG ABBR	E C T			
PKG LOCATION				
PKG NAME	G9JAP,G9MWS			
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
 ECC CONTROL
 CIRCUIT DIAGRAM
 11/14
 134-110229-008-0
 NEC SHT 11/

134-110229-008-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

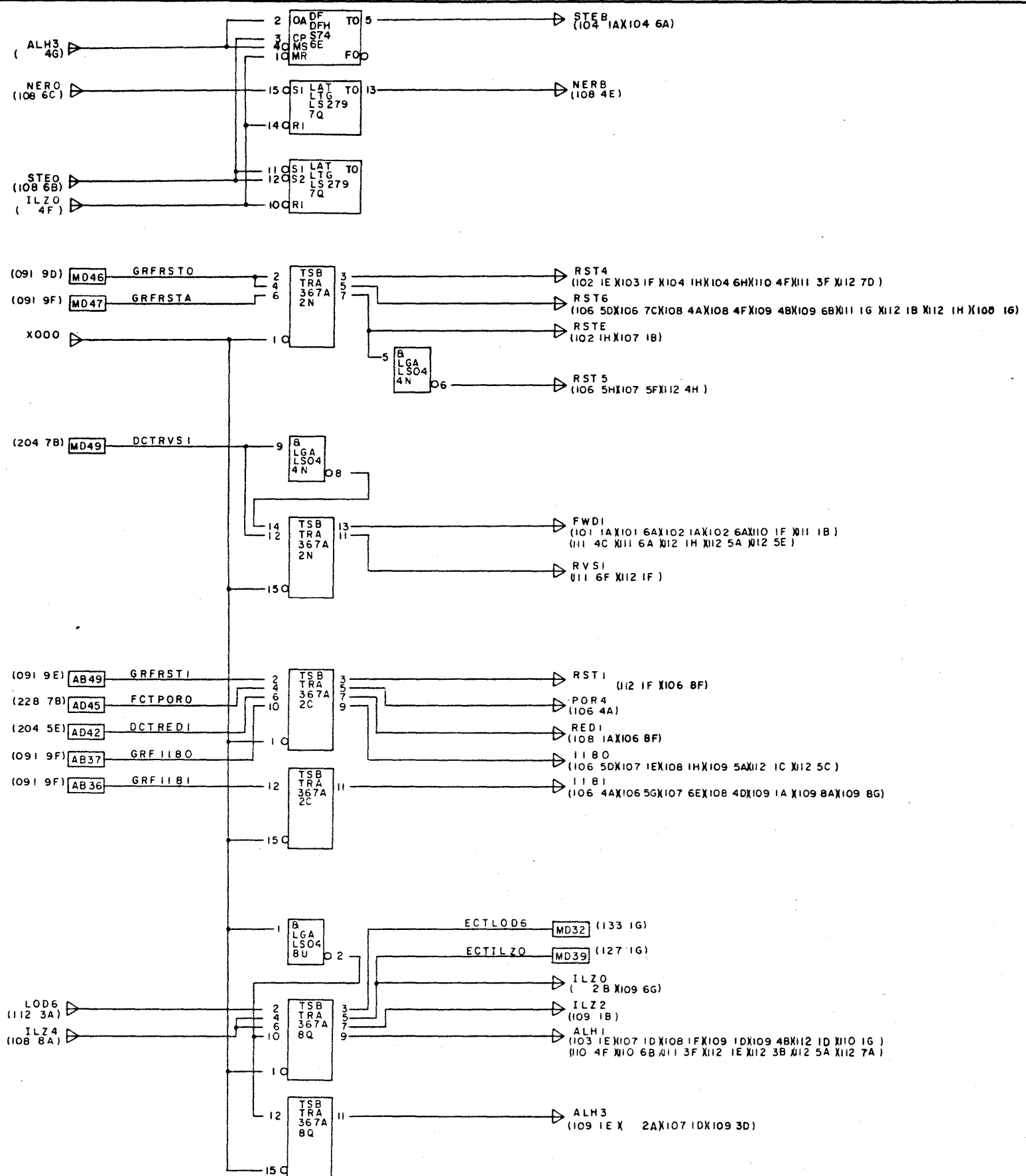
DWG ABBR	ECT
PKG LOCATION	
PKG NAME	G9JAP, G9MWS
112	

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	

MTA16X FORMATTER
ECC CONTROL
CIRCUIT DIAGRAM
 12/14

134-110229-008-0	
NEC	SHT 12/

134-110229-008-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

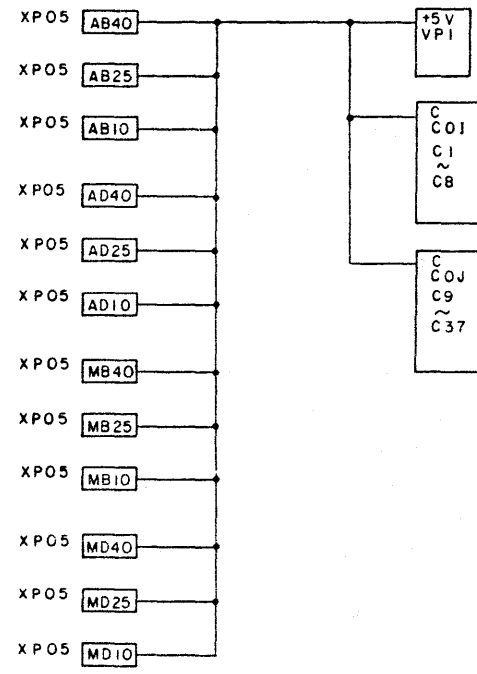
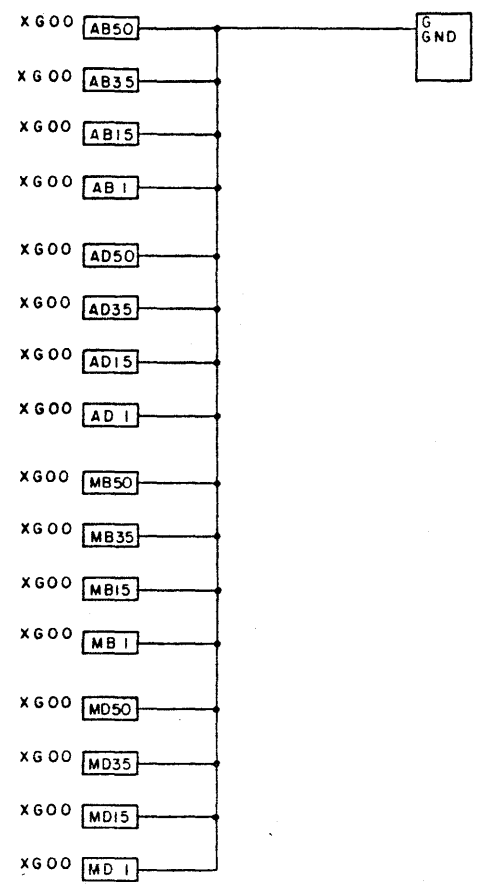
DWG ABBR	ECT
PKG LOCATION	
PKG NAME	G9JAP,G9MWS
113	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
ECC CONTROL
CIRCUIT DIAGRAM
13/14

134-110229-008-0
NEC
SHT 13/

134-110229-008-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	ECT
PKG LOCATION	
PKG NAME	G9JAP,G9MWS
114	
NEXT SPEC	

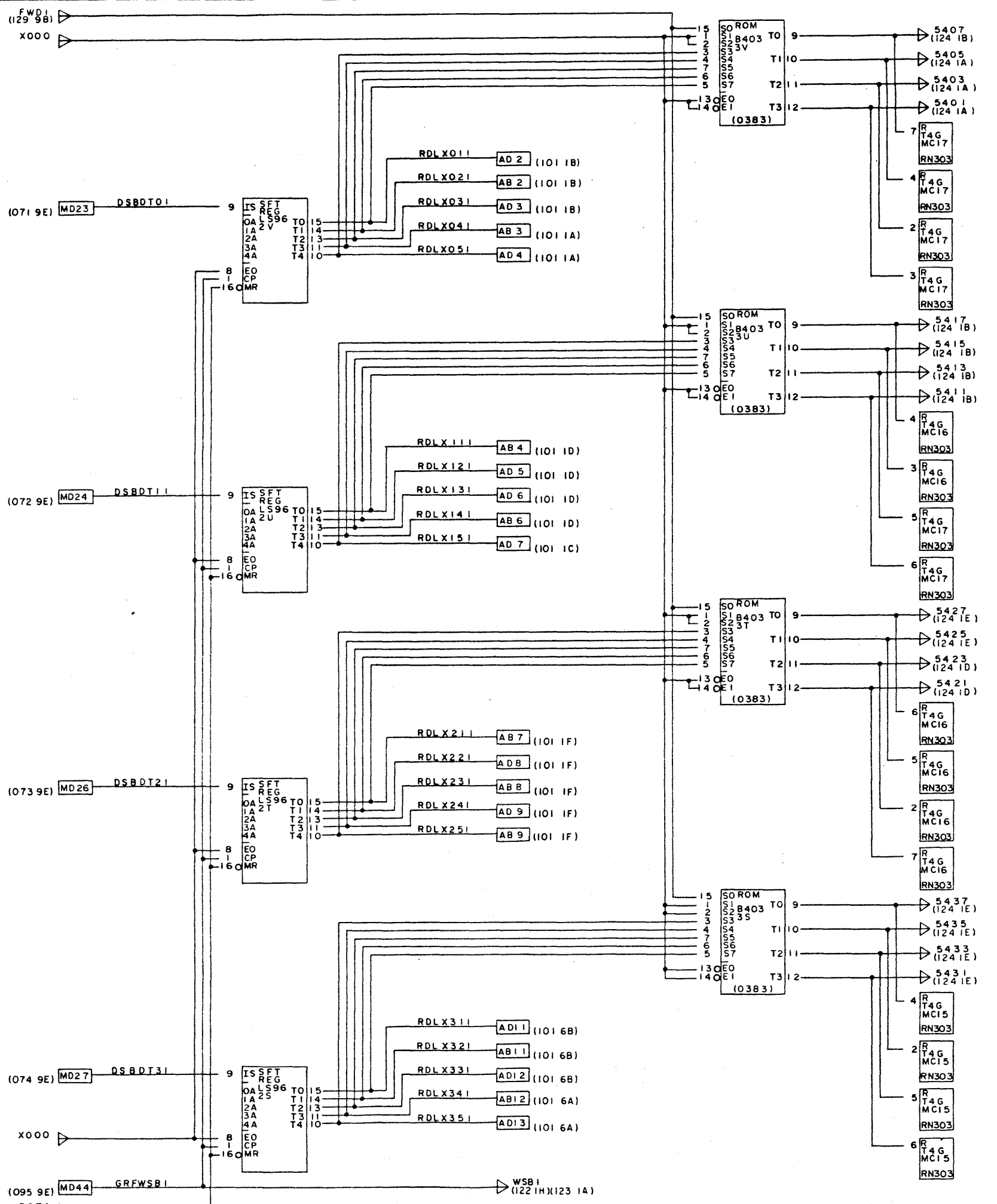
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
ECC CONTROL
CIRCUIT DIAGRAM
14/14

134-110229-008-0

NEC SHT 14/14

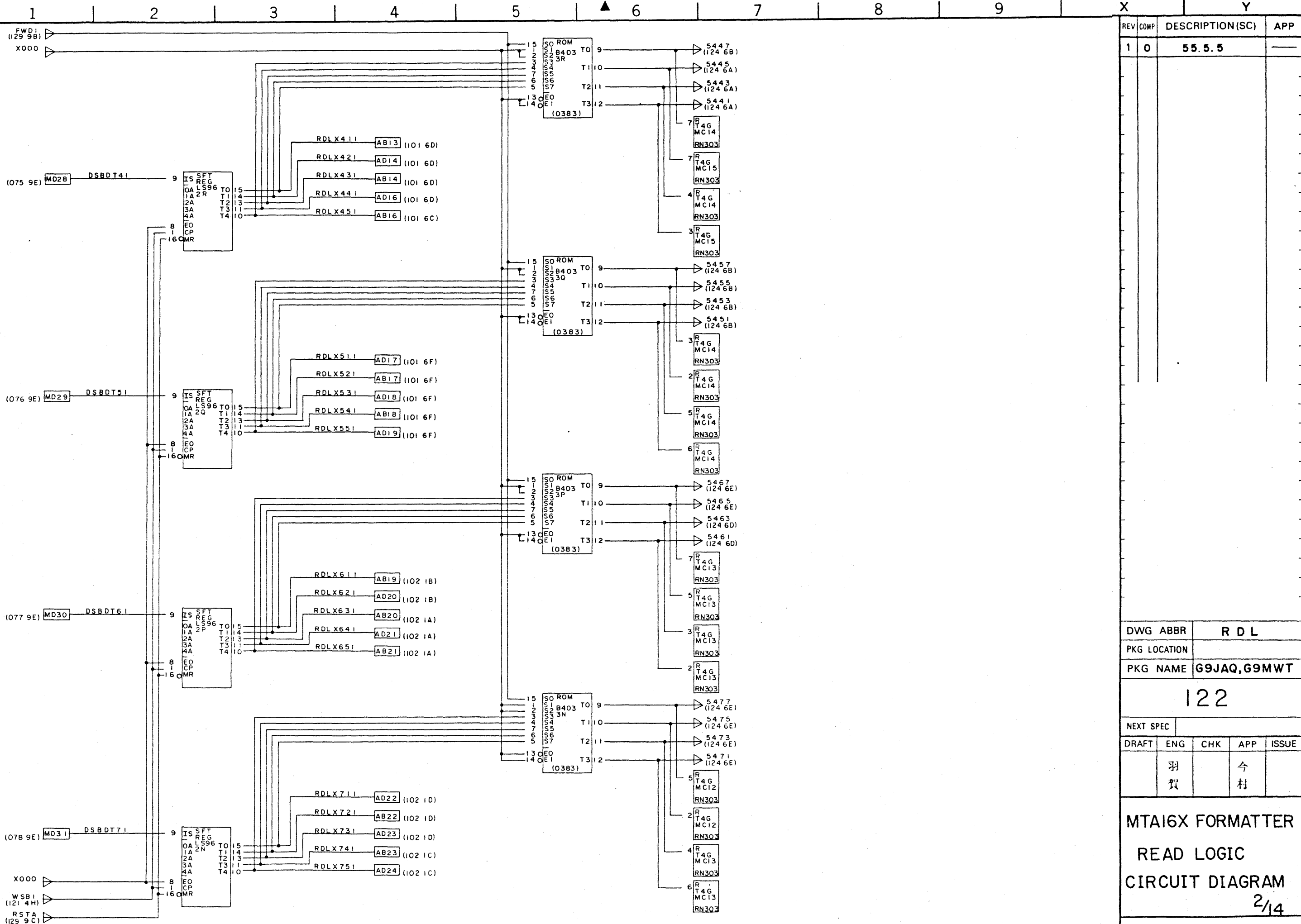
134-110229-007-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
2	0		大橋 羽賀

DWG ABBR	R D L			
PKG LOCATION				
PKG NAME	G9JQA,G9MWT			
121				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	
MTA16X FORMATTER READ LOGIC CIRCUIT DIAGRAM 1/14				
134-110229-007-0				
NEC				SHT 1/14

134-110229-007

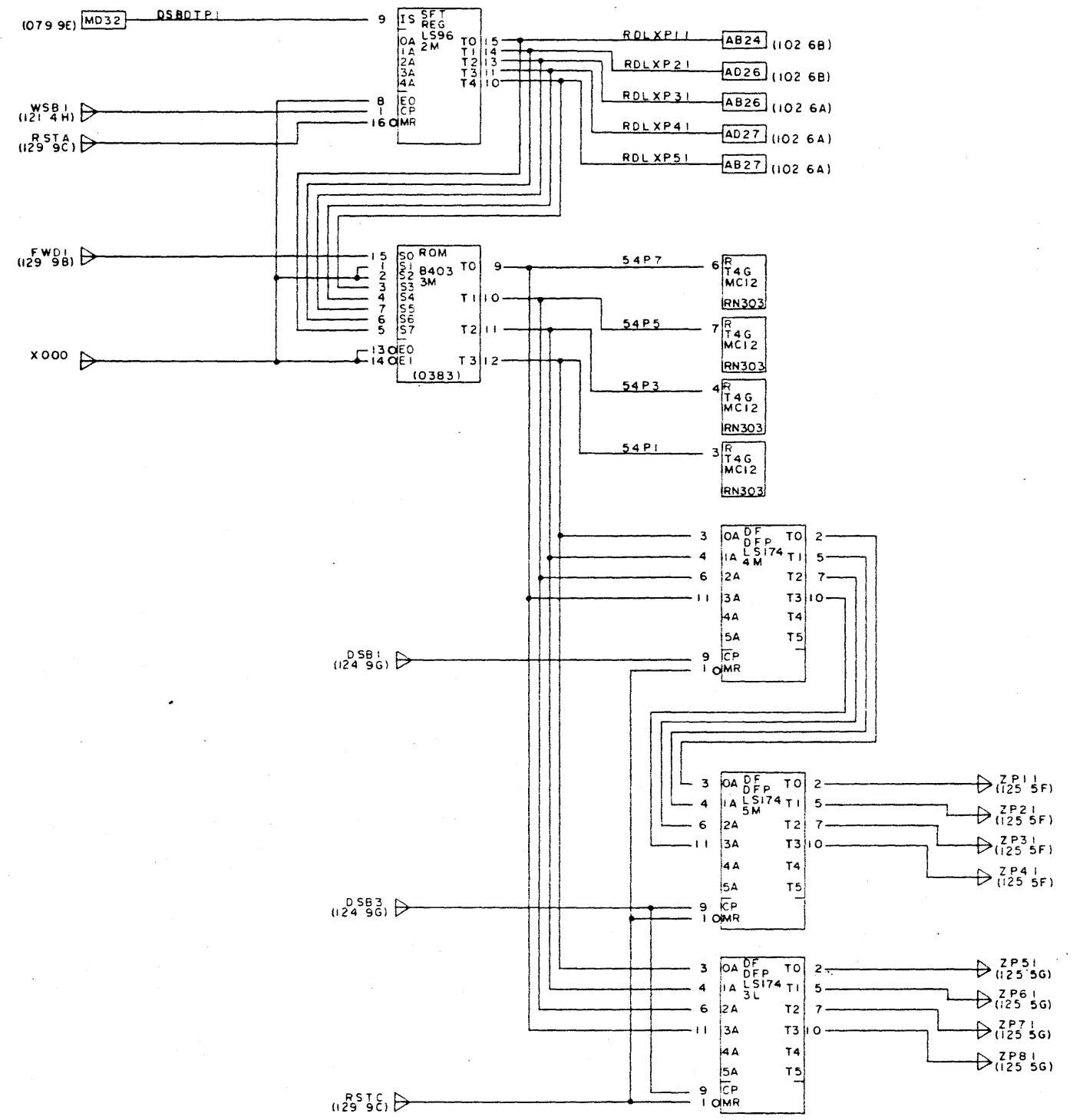


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	RDL		
PKG LOCATION			
PKG NAME	G9JAQ, G9MWT		
122			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTAI6X FORMATTER READ LOGIC CIRCUIT DIAGRAM 2/14			
134-110229-007			
NEC			SHT 2/

装置名

134-110229-007-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	R D L
PKG LOCATION	
PKG NAME	G9JAG, G9MWT
123	

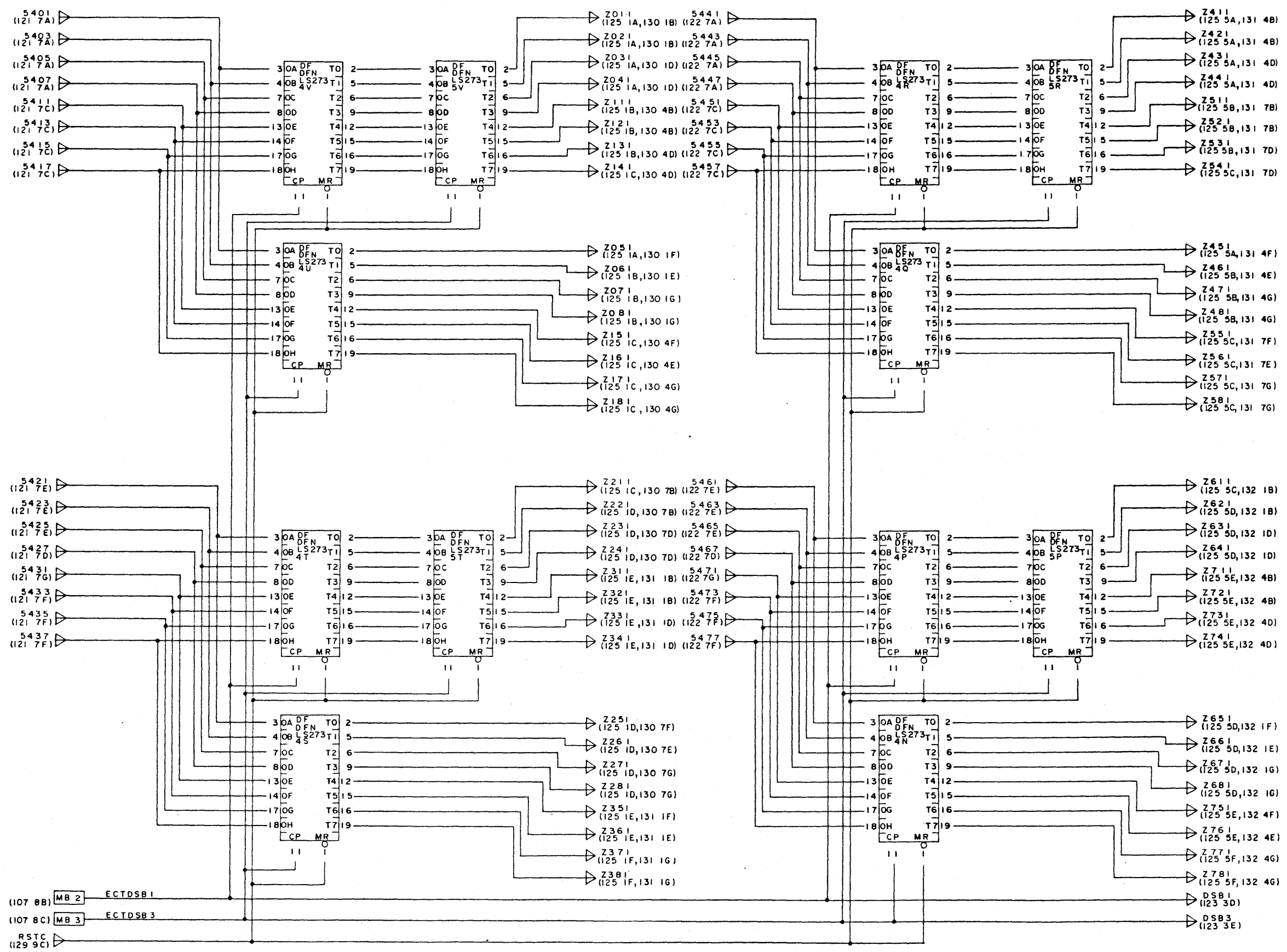
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
 READ LOGIC
 CIRCUIT DIAGRAM
 3/14

134-110229-007-0

NEC SHT 3/

134-110229-007

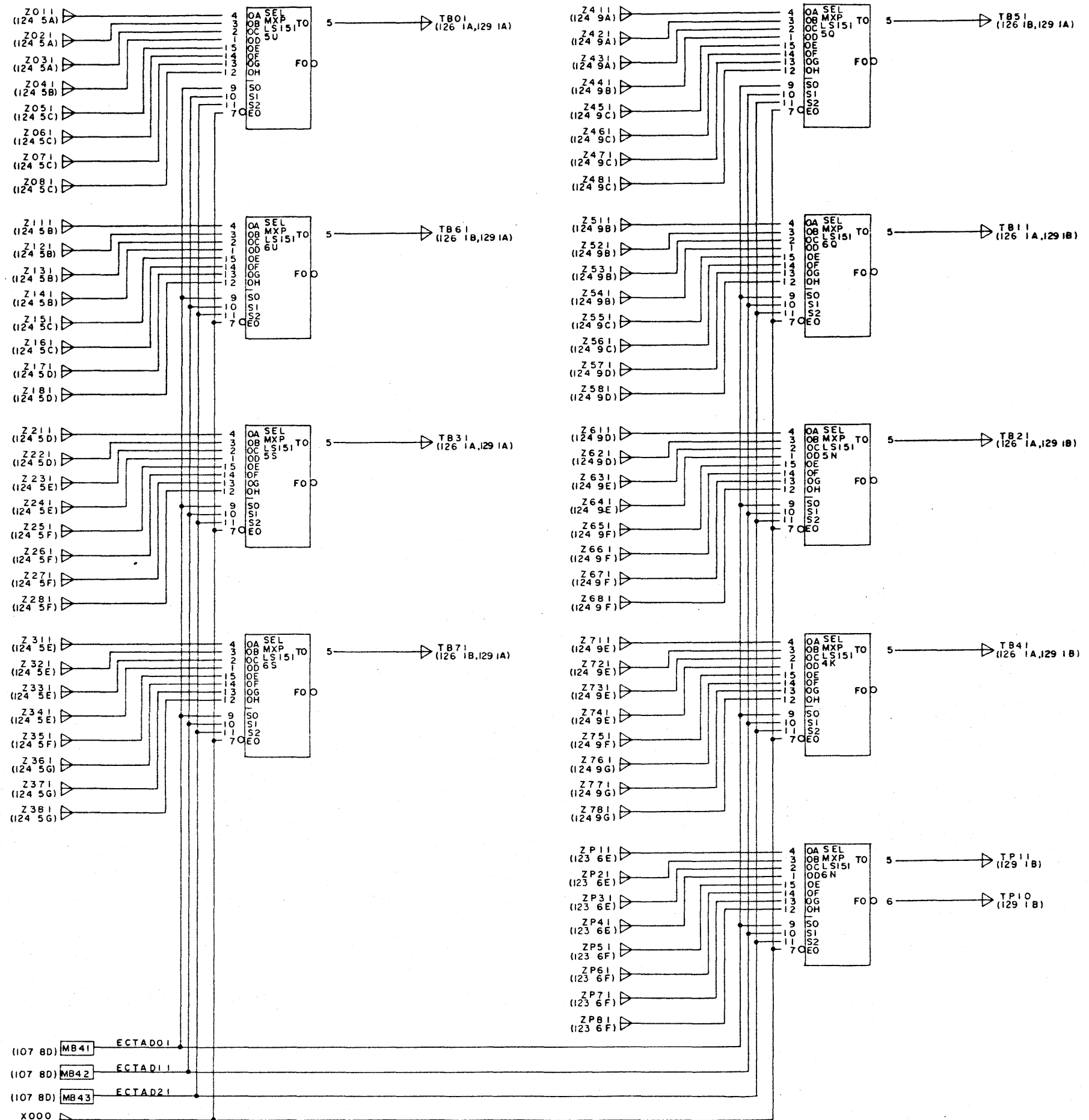


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	RDL			
PKG LOCATION				
PKG NAME	G9JQA, G9MWT			
124				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	
MTA16X FORMATTER READ LOGIC CIRCUIT DIAGRAM 4/14				
134-110229-007-0				
NEC				SHT 4/

装置名

134-110229-007-0

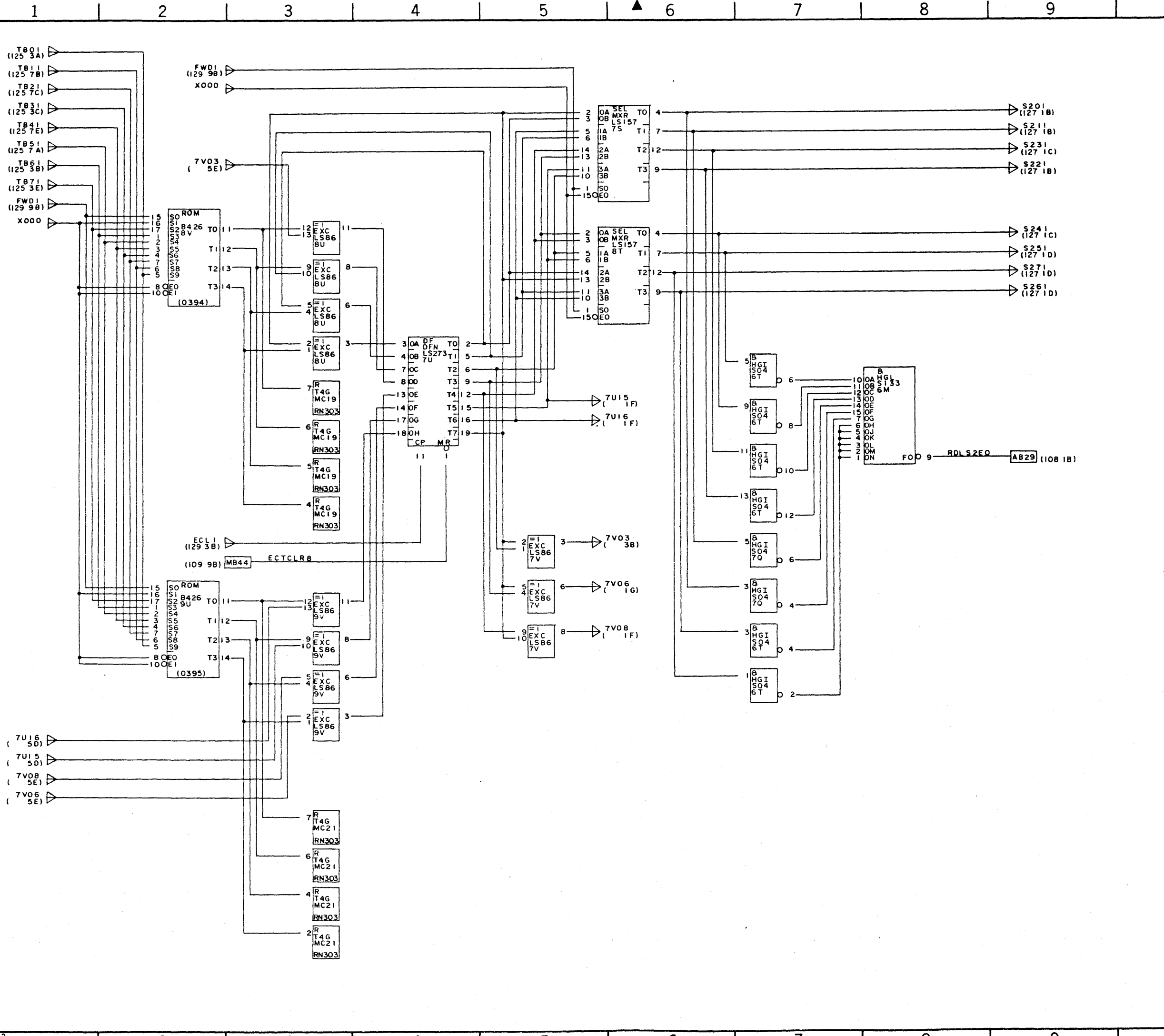


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
DWG ABBR		R D L	
PKG LOCATION			
PKG NAME		G9J AQ, G9M WT	
NEXT SPEC		135	
DRAFT	ENG	CHK	APP
	羽賀		今村
ISSUE			
MTA16X FORMATTER			
READ LOGIC			
CIRCUIT DIAGRAM			
5/14			
134-110229-007-0			
NEC		SHT	5/

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134-110229-007-0

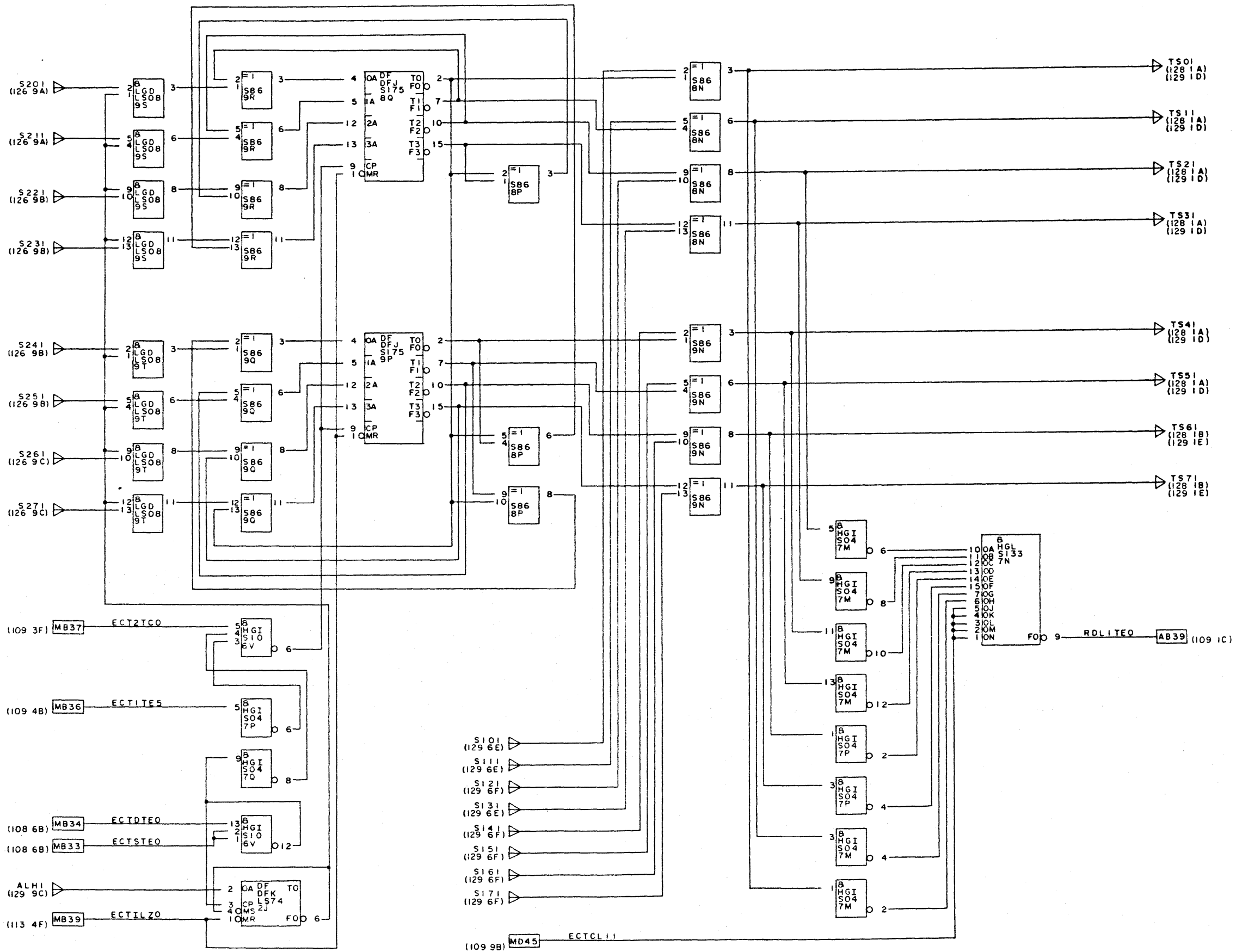


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	R D L			
PKG LOCATION				
PKG NAME	G9JAQ, G9MWT			
126				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	
MTA16X FORMATTER READ LOGIC CIRCUIT DIAGRAM 6/14				
134-110229-007-0				
NEC				SHT 6/

装置名

134-110229-007-0

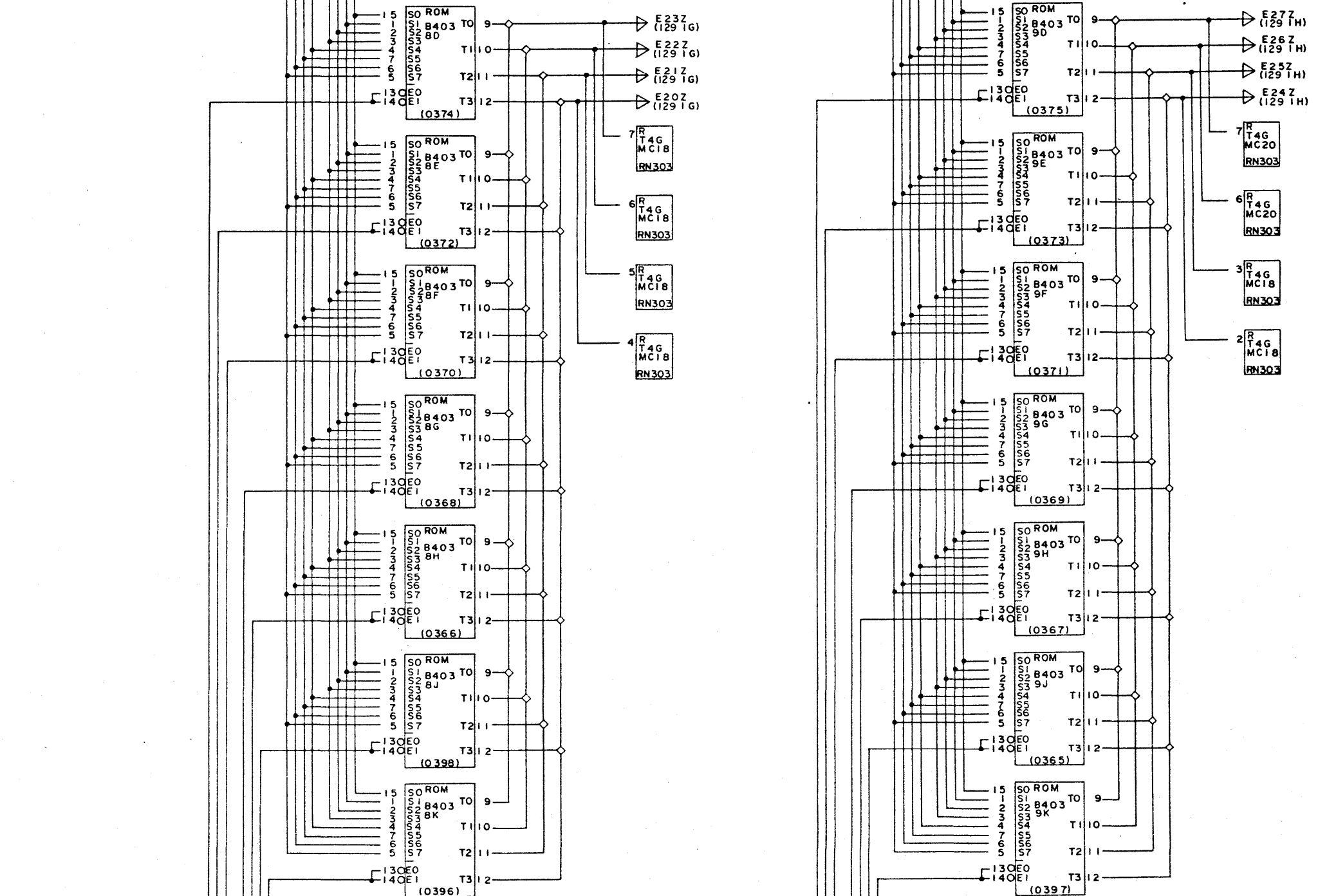


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	R D L			
PKG LOCATION				
PKG NAME	G9JQA,G9MWT			
127				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	
MTA16X FORMATTER READ LOGIC CIRCUIT DIAGRAM 7/14				
134-110229-007-0				
NEC				SHT 7/

134-110229-007-0

- TS01 (127 9A)
- TS11 (127 9B)
- TS21 (127 9B)
- TS31 (127 9B)
- TS41 (127 9C)
- TS51 (127 9D)
- TS61 (127 9D)
- TS71 (127 9D)

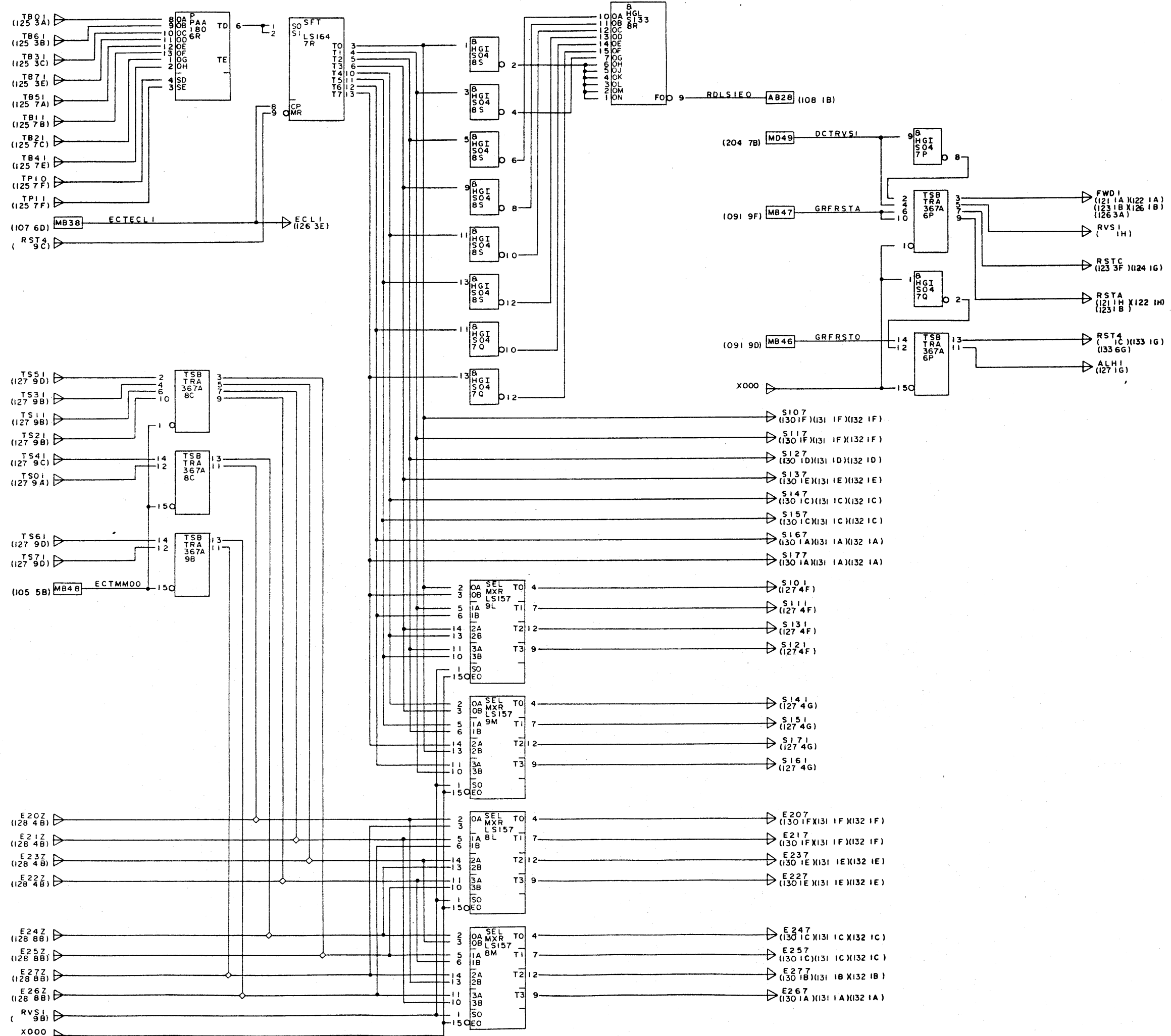


- (105 5C) MB12 ECTMM70
- (105 5C) MB11 ECTMM60
- (105 5D) MB9 ECTMM50
- (105 5D) MB8 ECTMM40
- (105 5B) MB7 ECTMM30
- (105 5B) MB6 ECTMM20
- (105 5B) MB4 ECTMM10

装置名

REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	
DWG ABBR		RDL	
PKG LOCATION			
PKG NAME		G9JAQ,G9MWT	
128			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTA16X FORMATTER READ LOGIC CIRCUIT DIAGRAM 8/14			
134-110229-007-0			
NEC			SHT 8/

134-110229-007-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	R D L
PKG LOCATION	
PKG NAME	G9JQA, G9MWT
129	
NEXT SPEC	

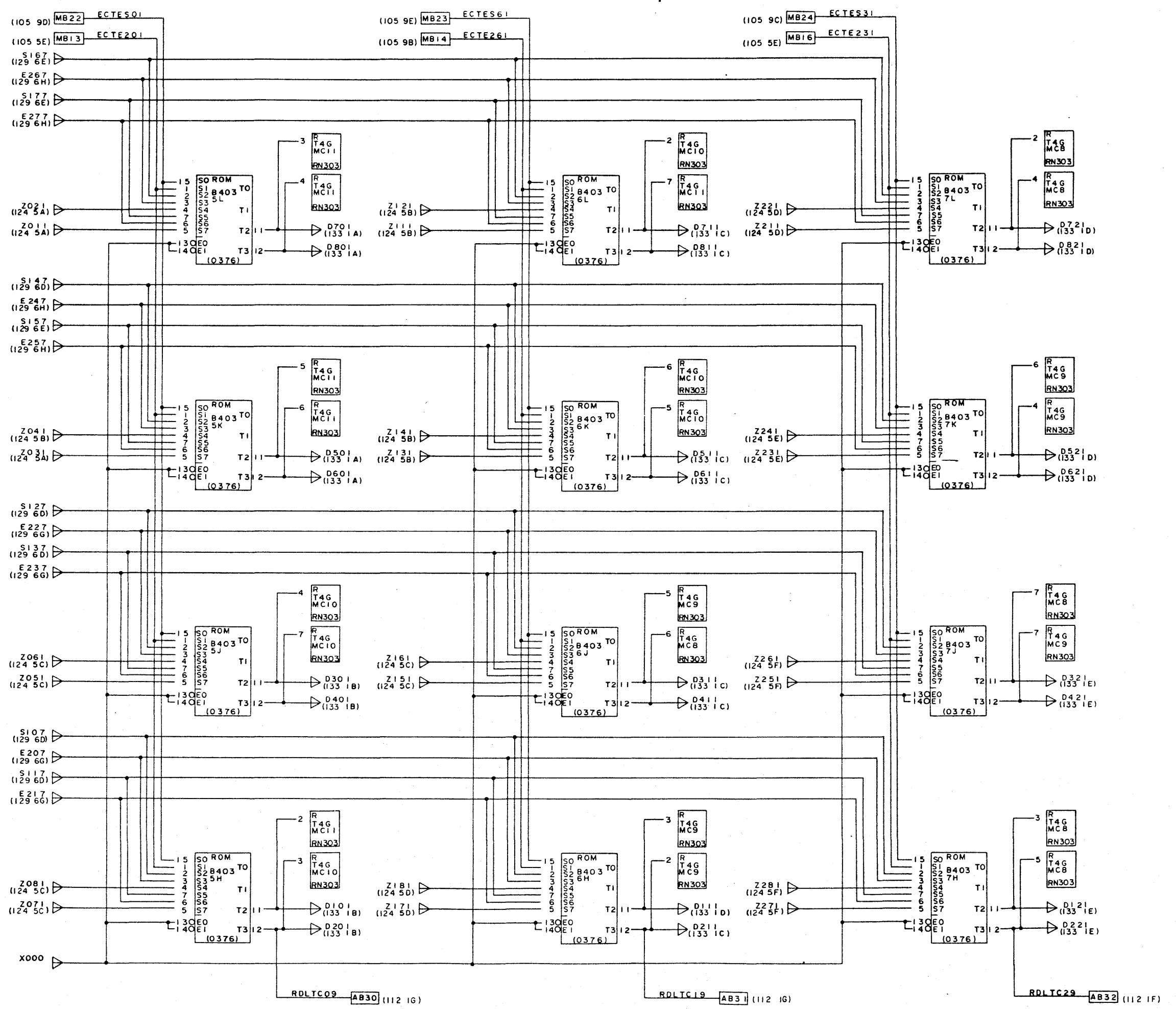
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
 READ LOGIC
 CIRCUIT DIAGRAM
 9/14

134-110229-007-0

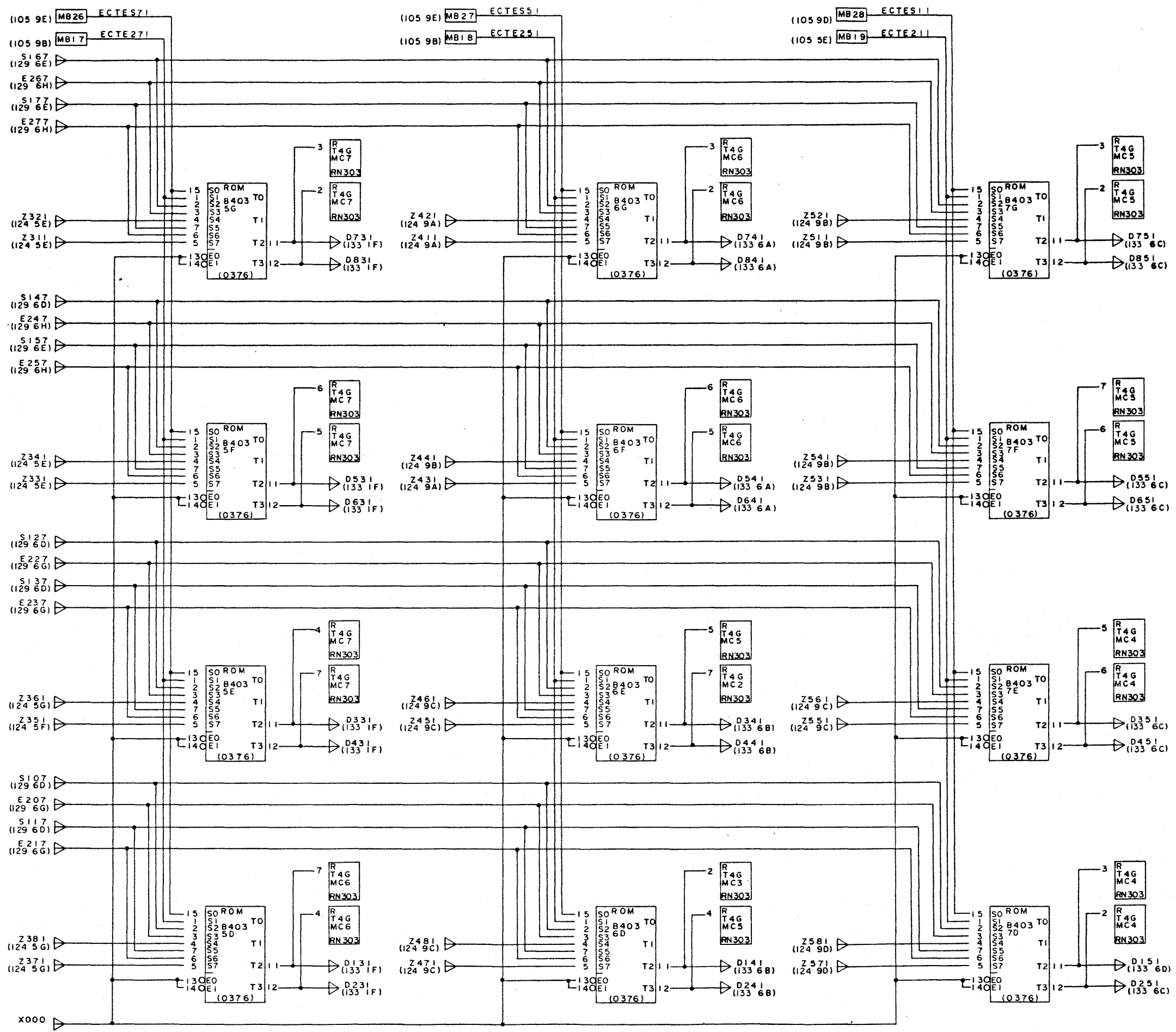
NEC SHT 9/

134-110229-007-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	
DWG ABBR		R D L	
PKG LOCATION			
PKG NAME		G9JQA,G9MWT	
		130	
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽		今
	賀		村
MTA16X FORMATTER READ LOGIC CIRCUIT DIAGRAM 10/14			
134-110229-007-0			
NEC		SHT 10/	

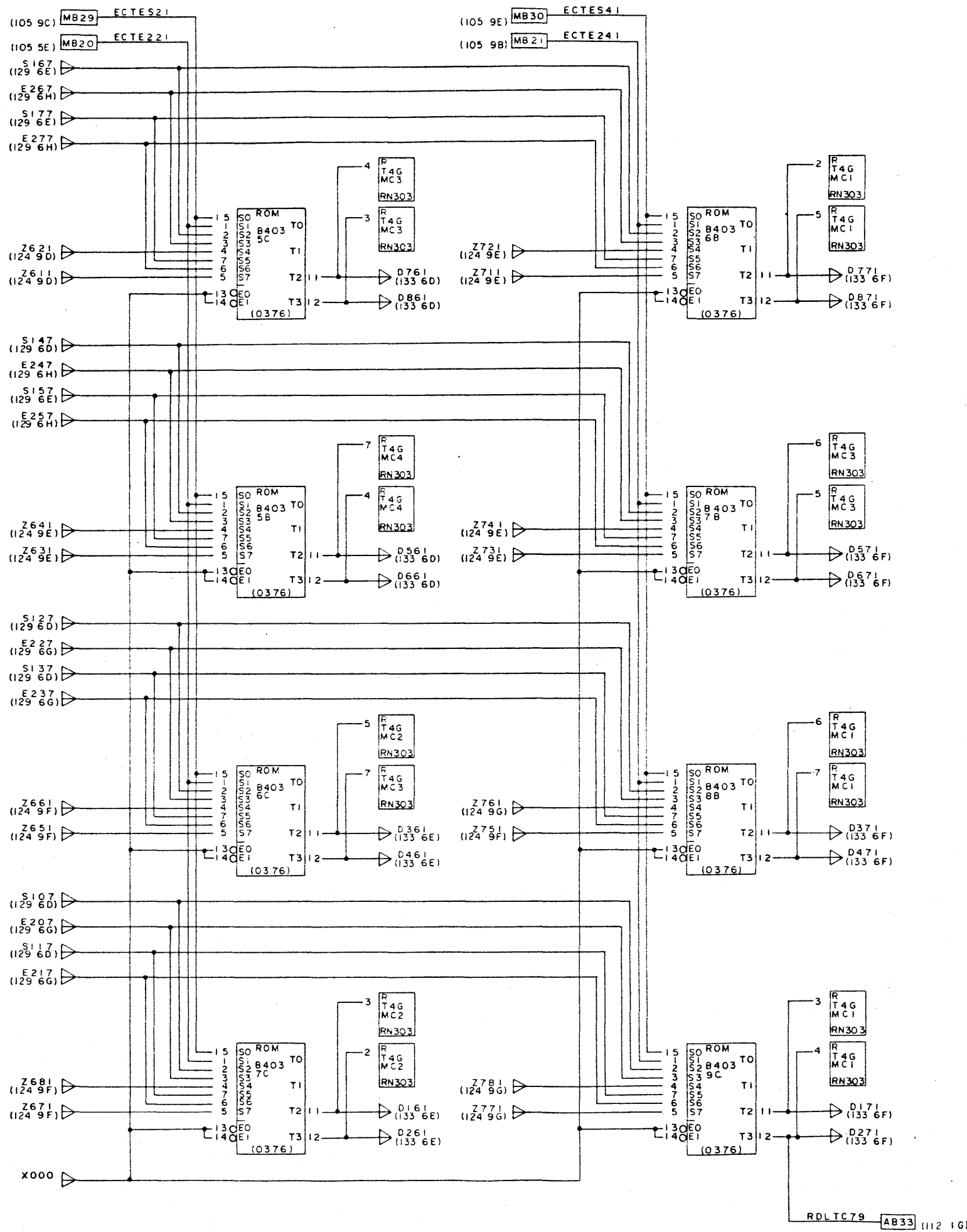
134-110229-007-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
DWG ABBR		RDL	
PKG LOCATION			
PKG NAME		G9JAJ, G9MWT	
131			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽		今村
MTA16X FORMATTER READ LOGIC CIRCUIT DIAGRAM 11/14			
134-110229-007-0			
NEC			SHT 11/

装置名

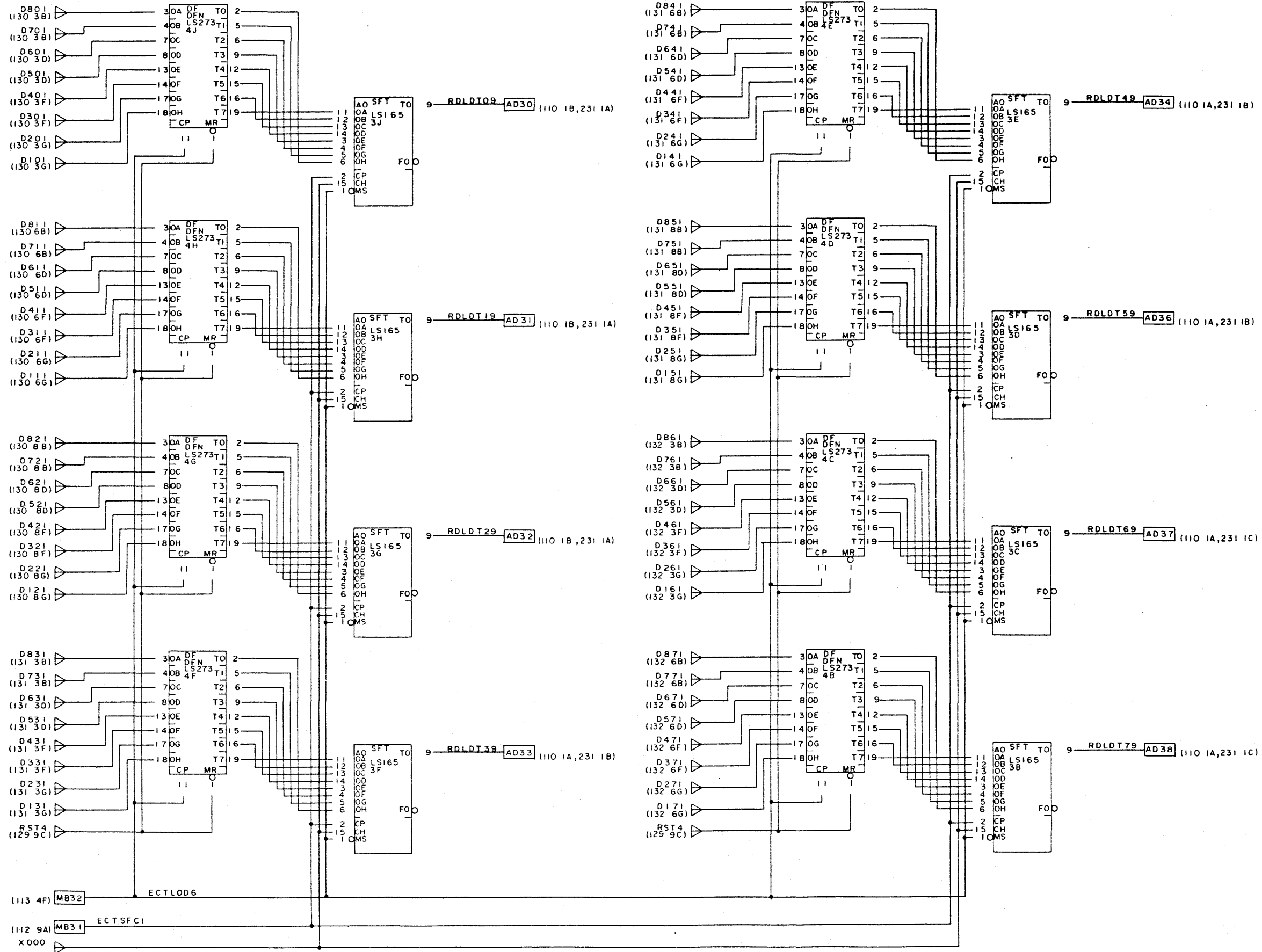
134-110229-007-0



REV	COMP	DESCRIPTION (SC)	APP																																												
1	0	55.5.5																																													
<table border="1"> <tr> <td>DWG ABBR</td> <td colspan="3">RDL</td> </tr> <tr> <td>PKG LOCATION</td> <td colspan="3"></td> </tr> <tr> <td>PKG NAME</td> <td colspan="3">G9JAG,G9MWT</td> </tr> <tr> <td colspan="4" style="text-align: center;">132</td> </tr> <tr> <td>NEXT SPEC</td> <td colspan="3"></td> </tr> <tr> <td>DRAFT</td> <td>ENG</td> <td>CHK</td> <td>APP</td> </tr> <tr> <td></td> <td>羽</td> <td></td> <td>今</td> </tr> <tr> <td></td> <td>賀</td> <td></td> <td>村</td> </tr> <tr> <td colspan="4" style="text-align: center;">MTAI6X FORMATTER READ LOGIC CIRCUIT DIAGRAM 12/14</td> </tr> <tr> <td colspan="4">134-110229-007-0</td> </tr> <tr> <td colspan="3">NEC</td> <td>SHT 12/</td> </tr> </table>				DWG ABBR	RDL			PKG LOCATION				PKG NAME	G9JAG,G9MWT			132				NEXT SPEC				DRAFT	ENG	CHK	APP		羽		今		賀		村	MTAI6X FORMATTER READ LOGIC CIRCUIT DIAGRAM 12/14				134-110229-007-0				NEC			SHT 12/
DWG ABBR	RDL																																														
PKG LOCATION																																															
PKG NAME	G9JAG,G9MWT																																														
132																																															
NEXT SPEC																																															
DRAFT	ENG	CHK	APP																																												
	羽		今																																												
	賀		村																																												
MTAI6X FORMATTER READ LOGIC CIRCUIT DIAGRAM 12/14																																															
134-110229-007-0																																															
NEC			SHT 12/																																												

装置名

134-110229-007-0



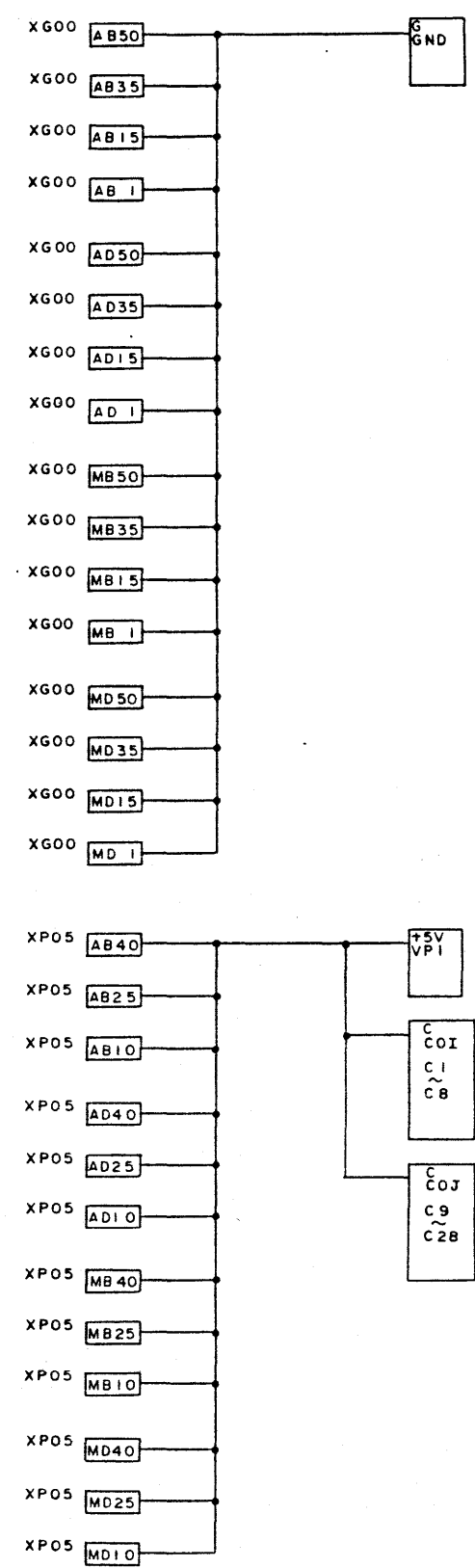
REV	COMP	DESCRIPTION (SC)	APP
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DWG ABBR		RDL	
PKG LOCATION			
PKG NAME		G9JAG, G9MWT	
		133	
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTA16X FORMATTER READ LOGIC CIRCUIT DIAGRAM 13/14			
134-110229-007-0			
NEC			SHT 13/

装置名

134-110229-007-0

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装置名

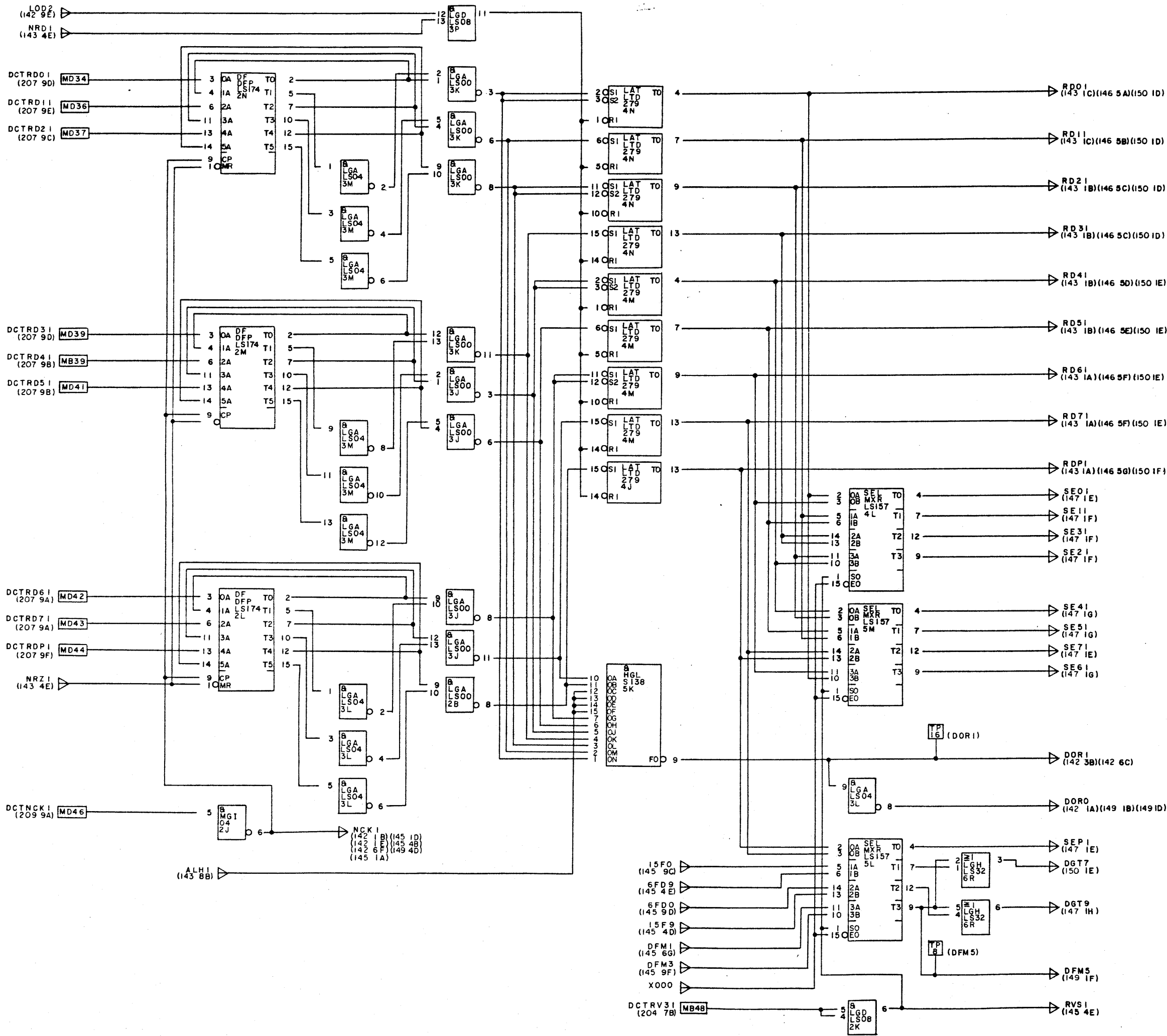


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	R D L			
PKG LOCATION				
PKG NAME	G9JAQ, G9MWT			
134				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽 賀		今 村	

MTA16X FORMATTER
 READ LOGIC
 CIRCUIT DIAGRAM
 14/14
 134-110229-007-0
 NEC SHT 14/14

134-110229-006-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	
2	0	11.5.26 羽賀 大橋	大橋

DWG ABBR	NRG			
PKG LOCATION				
PKG NAME	G9JAR			
141				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

**MTA16X FORMATTER
NRZI CONTROL
CIRCUIT DIAGRAM**

1/12

134-110229-006-0

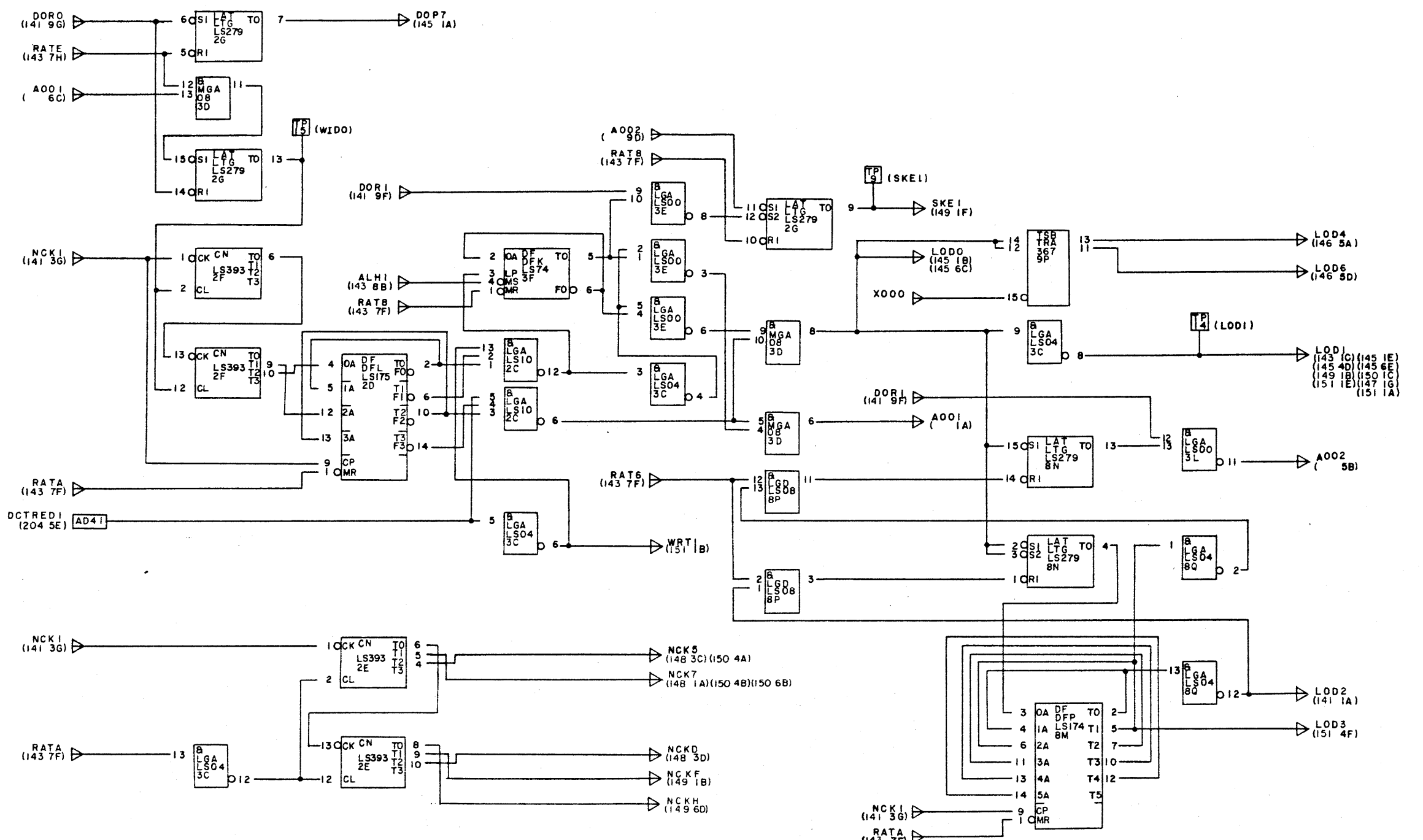
NEC SHT 1/12

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A
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装置名
DB-413
JIS A2 (420x594)

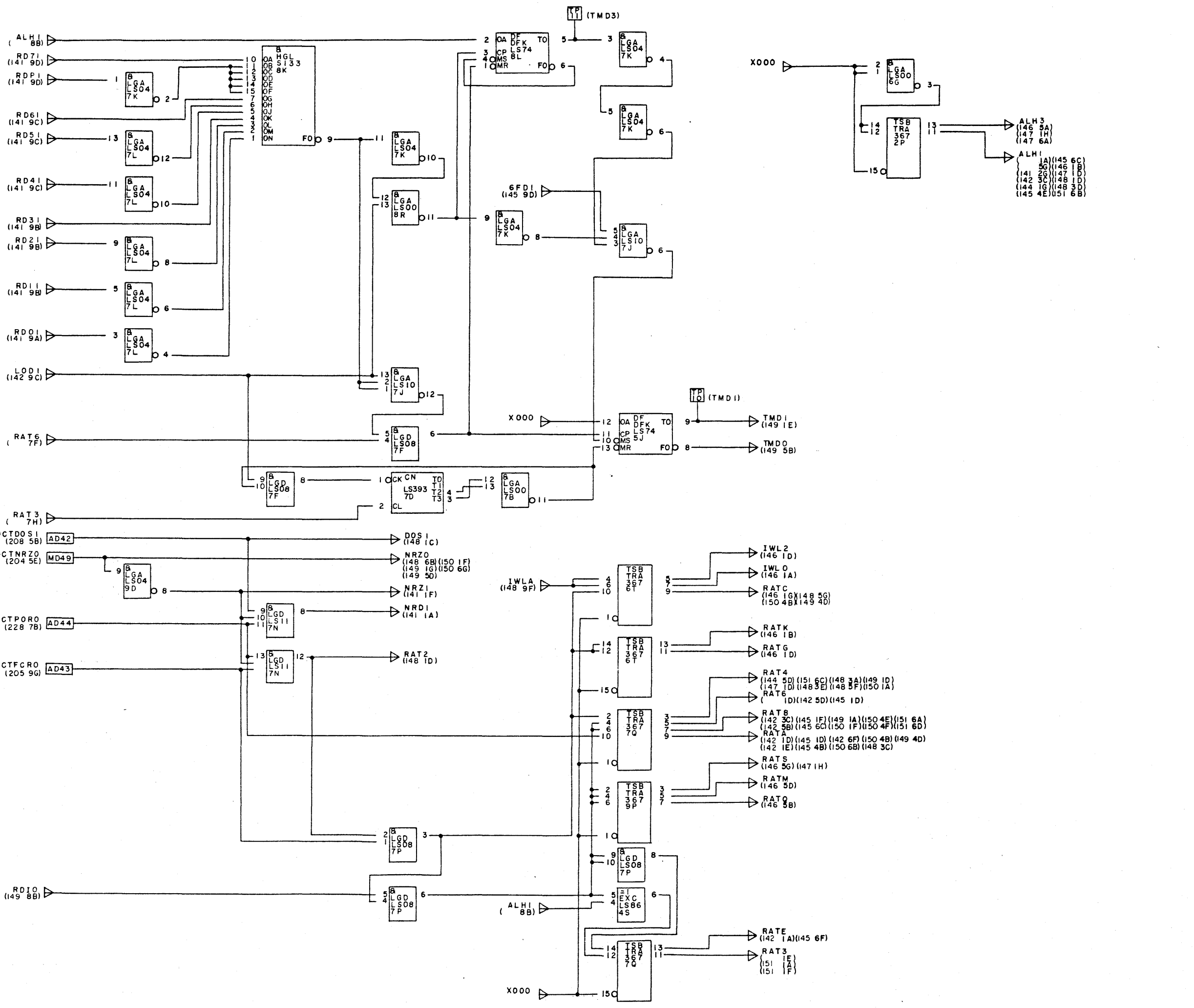
134-110229-006-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	N R G			
PKG LOCATION				
PKG NAME	G 9 J A R			
142				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽 賀		今 村	
MTAI6X FORMATTER NRZI CONTROL CIRCUIT DIAGRAM 2/12				
134-110229-006-0				
NEC				SHT 2 /

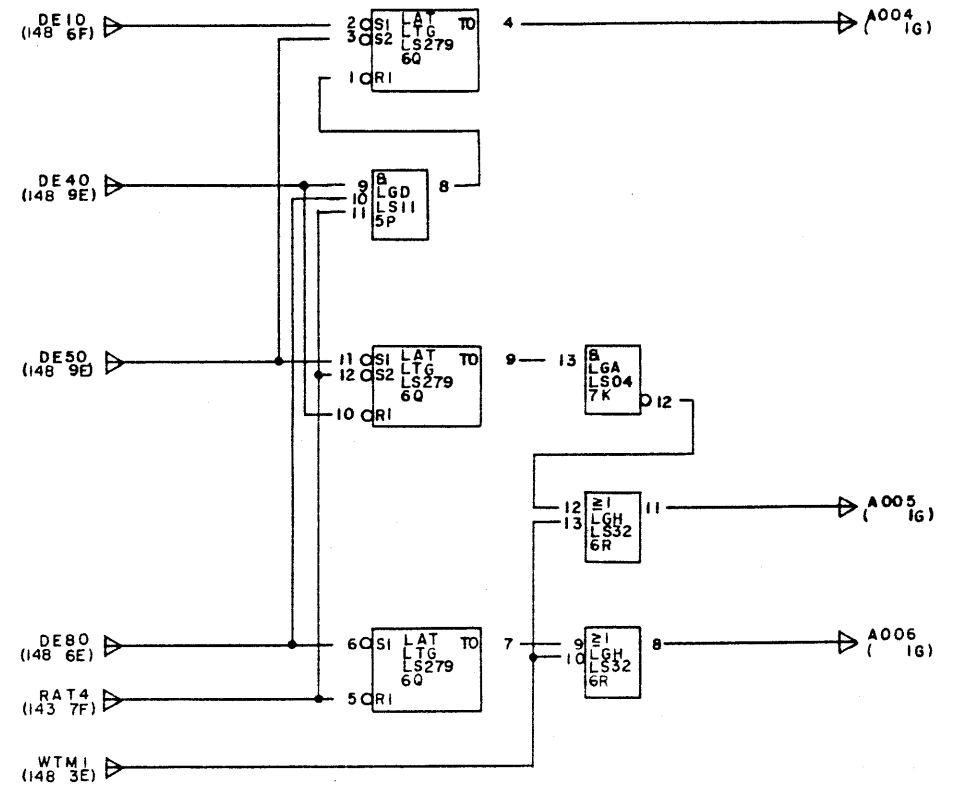
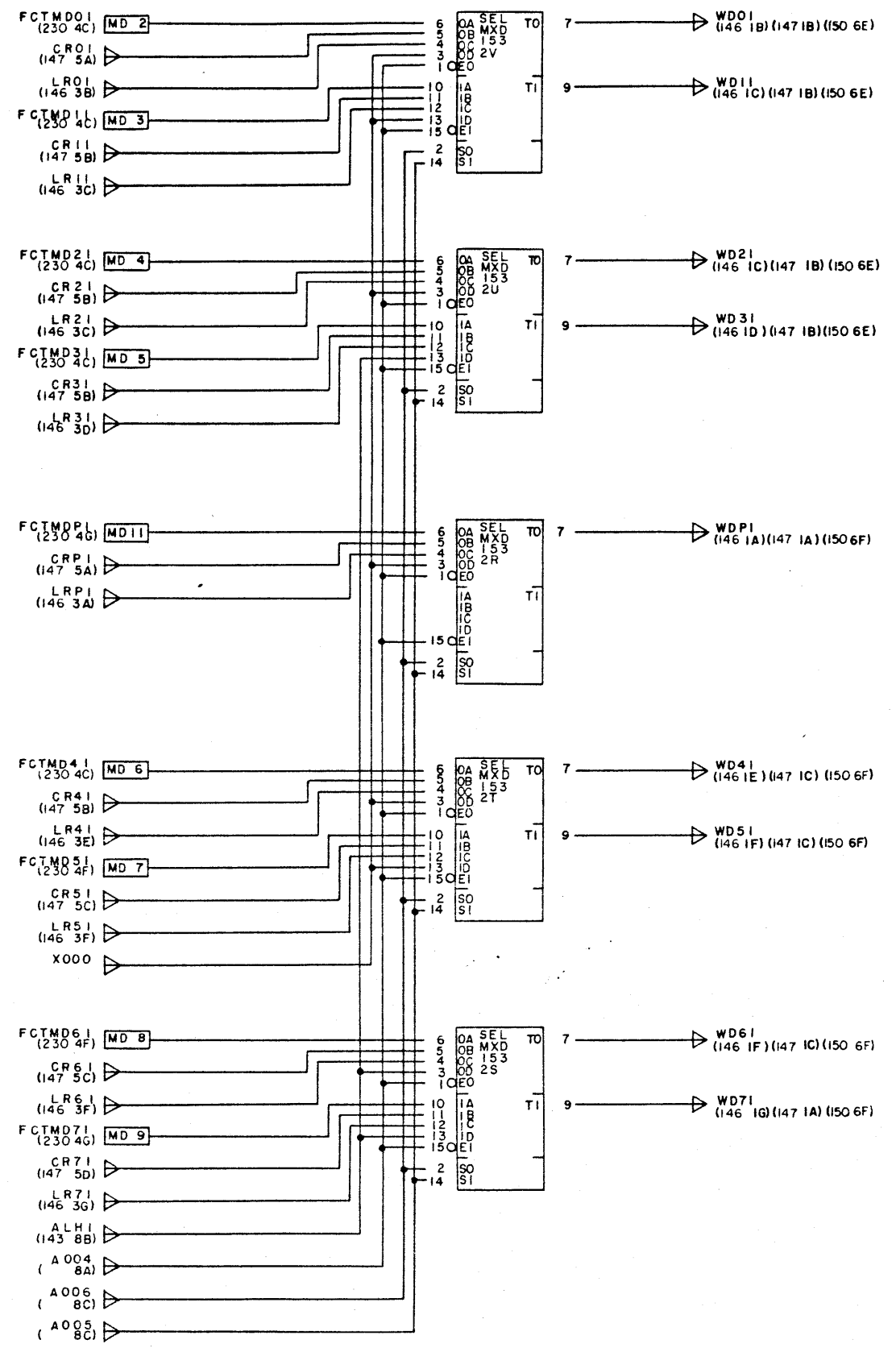
134-110229-006-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	N R G			
PKG LOCATION				
PKG NAME	G 9 J A R			
143				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	
MTA16X FORMATTER NRZI CONTROL CIRCUIT DIAGRAM 3/12				
134-110229-006-				
NEC				SHT 3/

134-110229-006-0



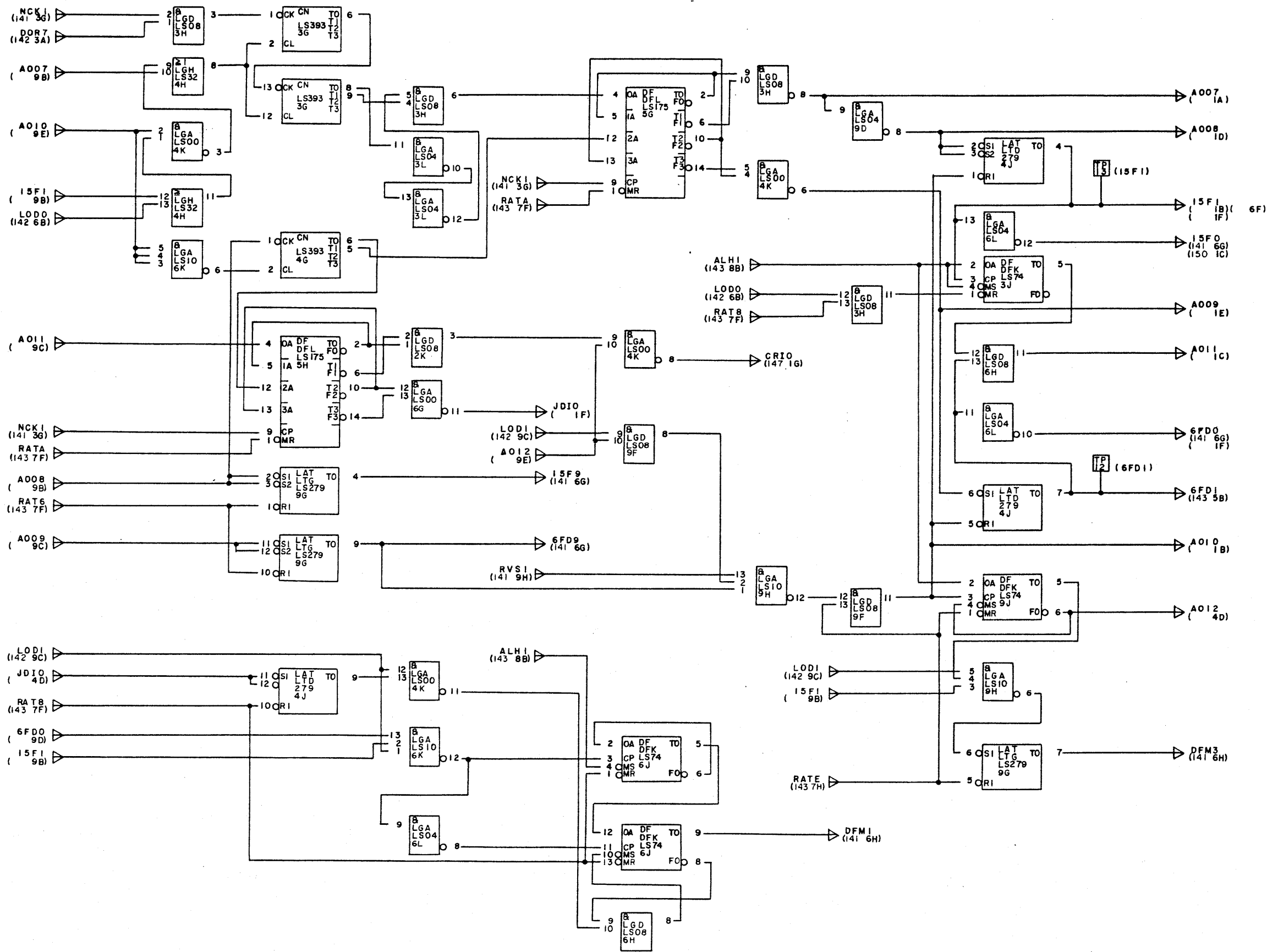
REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	N R G			
PKG LOCATION				
PKG NAME	G 9 J A R			
144				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
NRZI CONTROL
CIRCUIT DIAGRAM
4/12

134-110229-006-0
NEC SHT 4/

134-110229-006-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	N R G
PKG LOCATION	
PKG NAME	G 9 J A R
145	

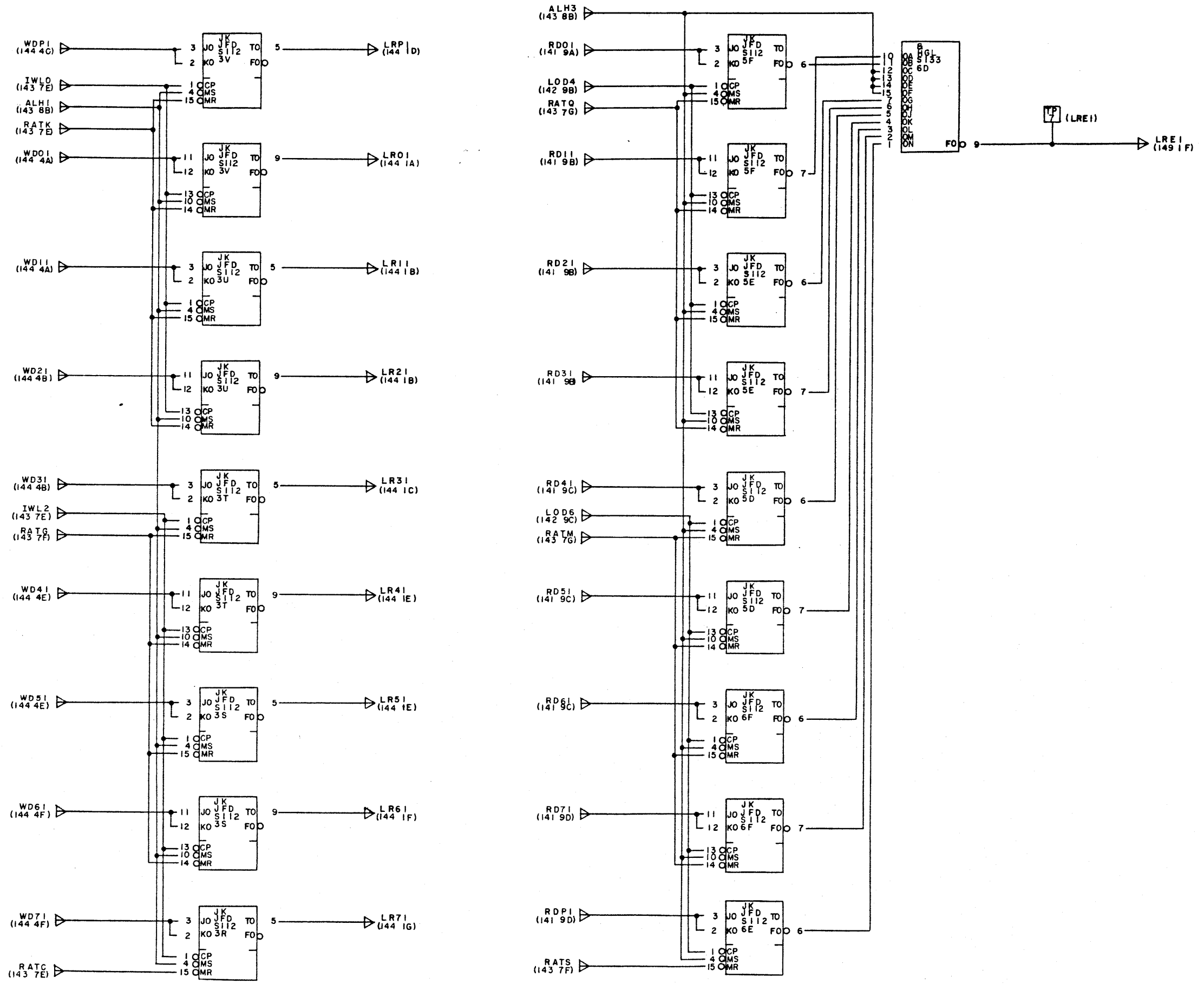
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	

MTA16X FORMATTER
NRZI CONTROL
CIRCUIT DIAGRAM
 5/12

134-110229-006-0

NEC SHT 5/

134-110229-006-0

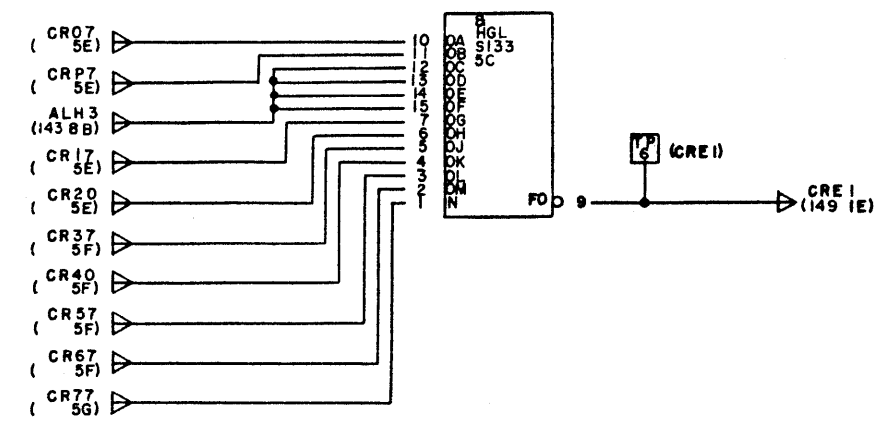
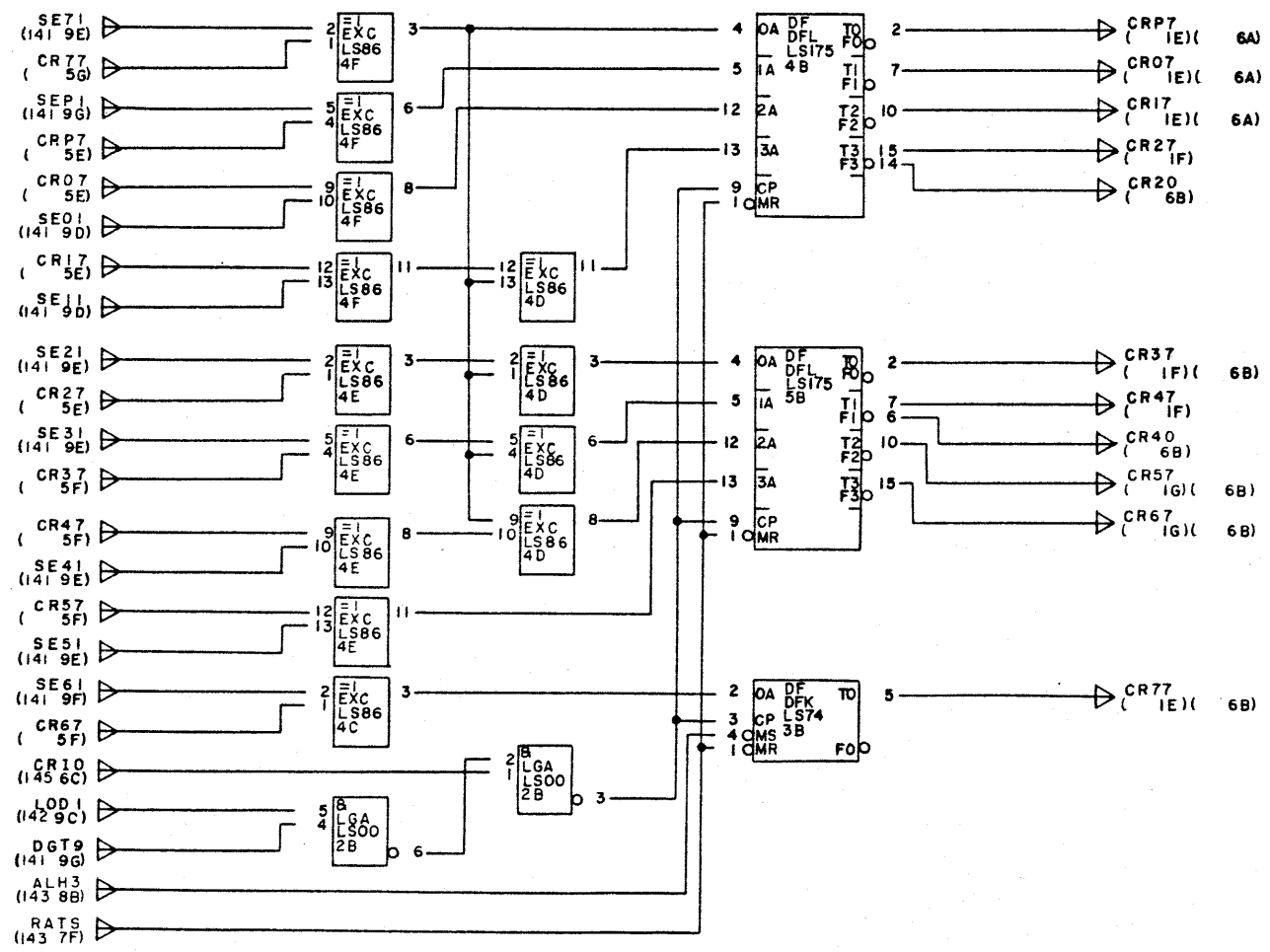
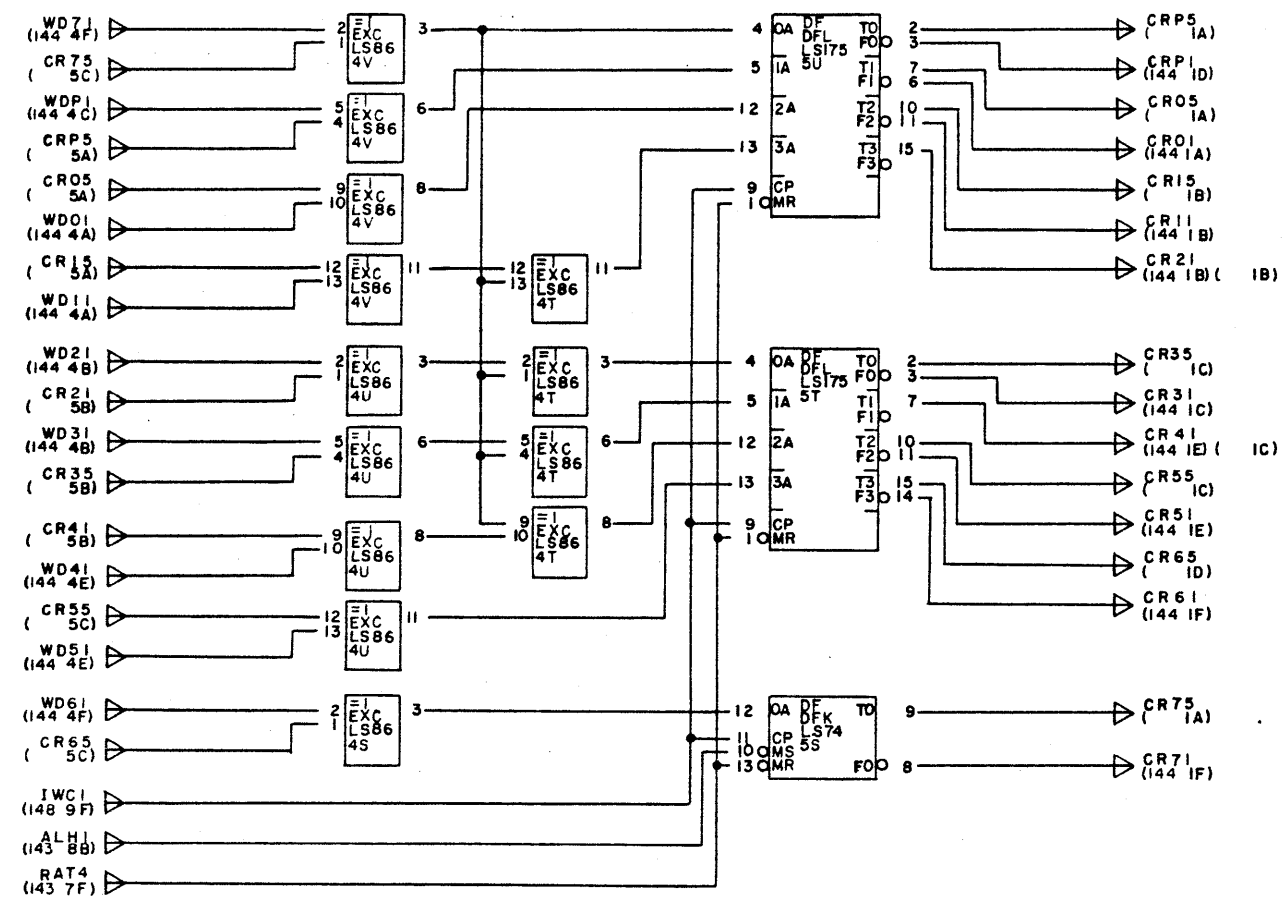


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	NRG		
PKG LOCATION			
PKG NAME	G9JAR		
146			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTA16X FORMATTER NRZI CONTROL CIRCUIT DIAGRAM 6/12			
134-110229-006-0			
NEC			SHT 6/

装置名

134-110229-006-0



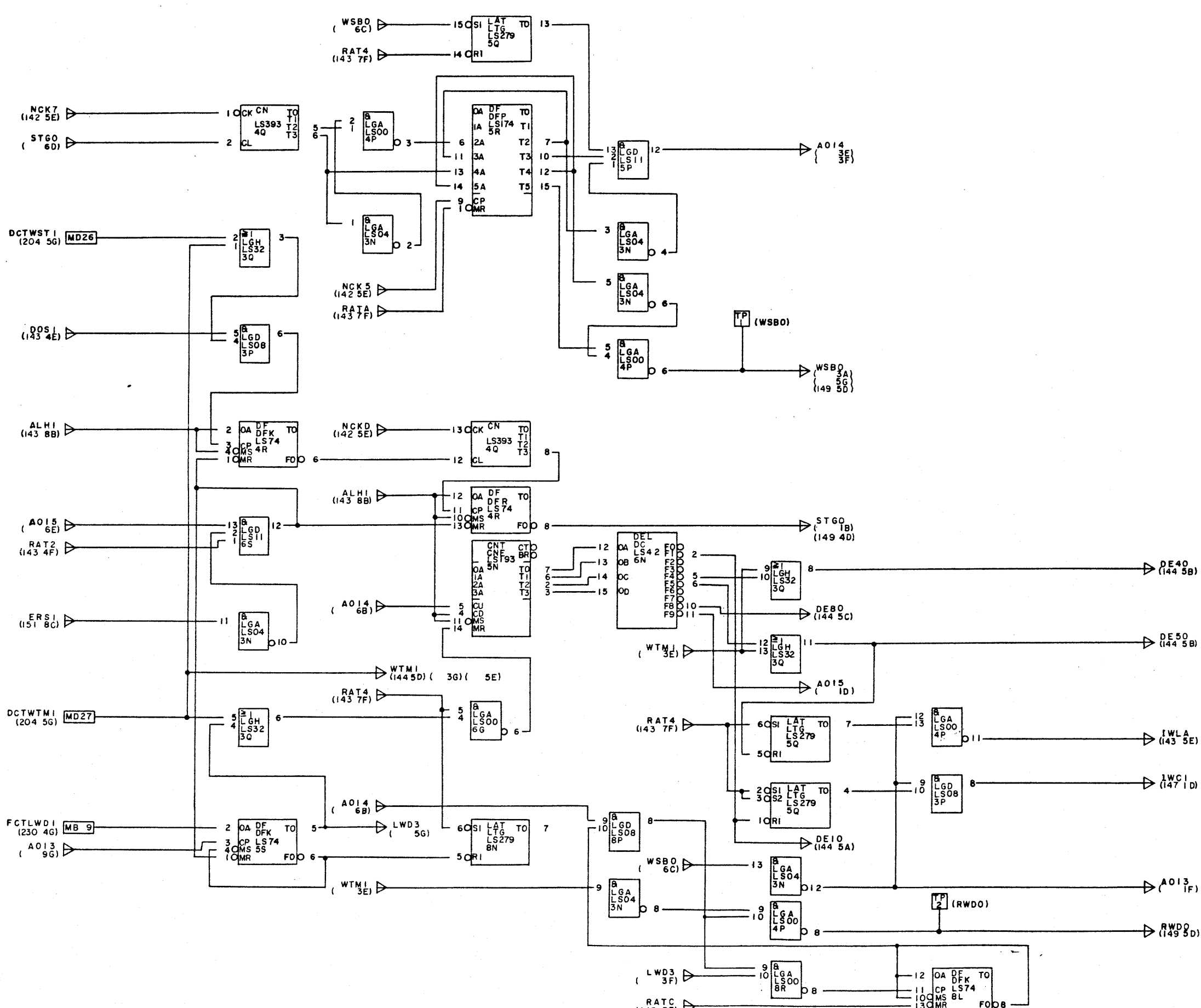
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	NRG			
PKG LOCATION				
PKG NAME	G9JAR			
147				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER NRZI CONTROL CIRCUIT DIAGRAM 7/12				
134-110229-006-0				
NEC				SHT 7/

装置名

134-110229-006-0

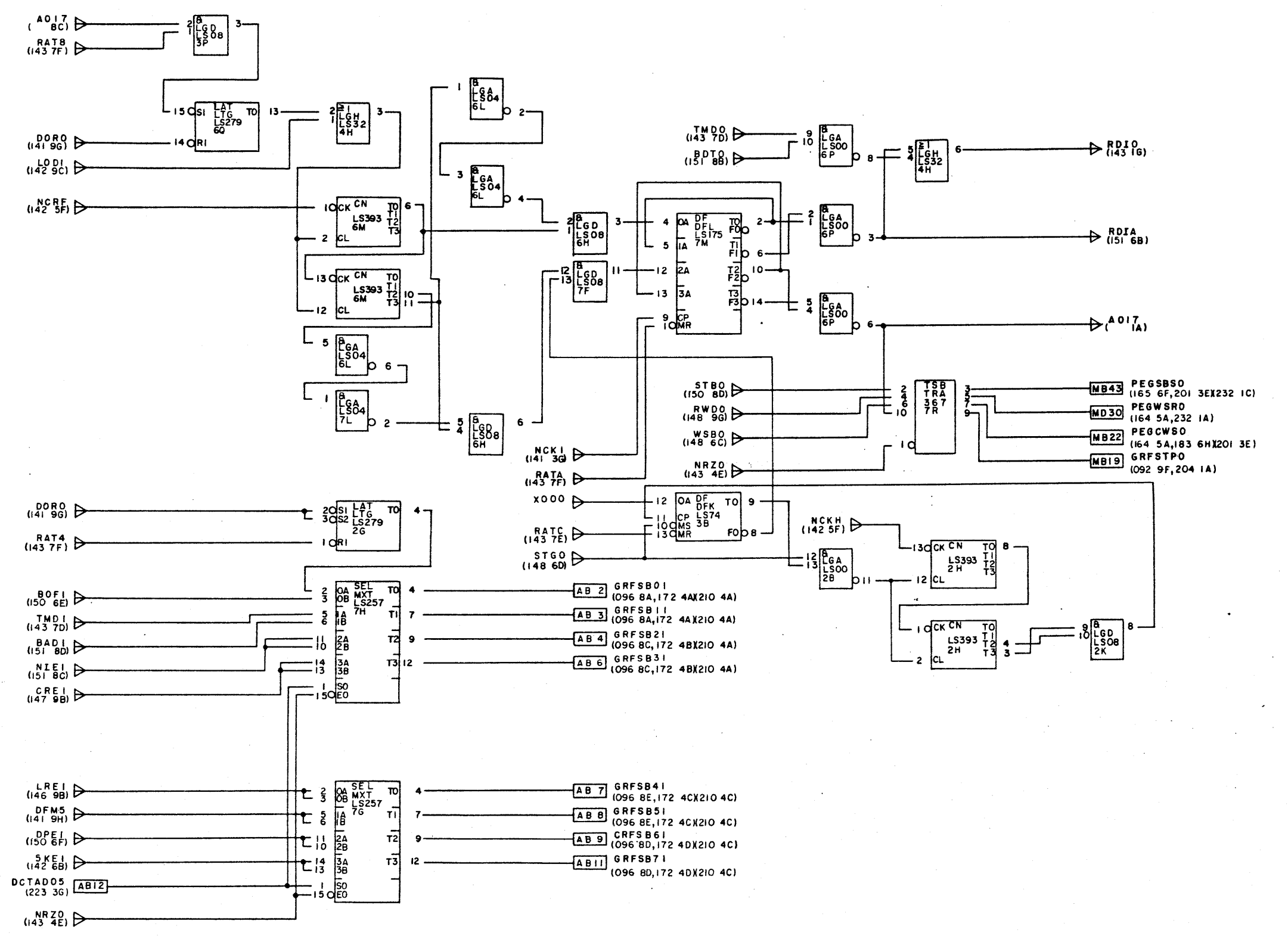


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	NRG			
PKG LOCATION				
PKG NAME	G9JAR			
148				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
NRZI CONTROL
CIRCUIT DIAGRAM
8/12
134-110229-006-0
NEC SHT 8/

134-110229-006-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

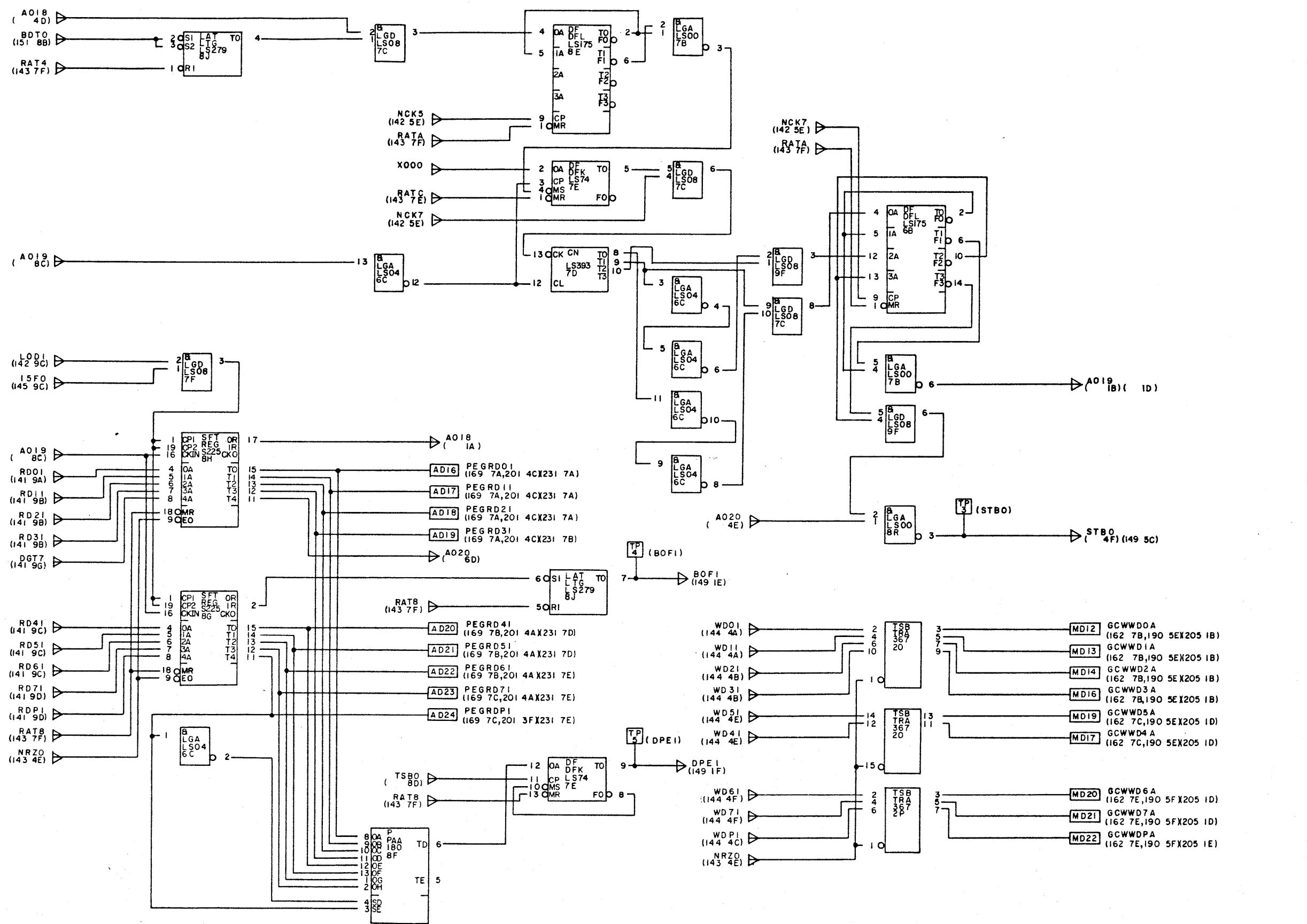
DWG ABBR	NRG			
PKG LOCATION				
PKG NAME	G9JAR			
149				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
NRZI CONTROL
CIRCUIT DIAGRAM
9/12

134-110229-006-0

NEC SHT 9/

134-110229-006-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	N R G			
PKG LOCATION				
PKG NAME	G 9 J A R			
150				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	

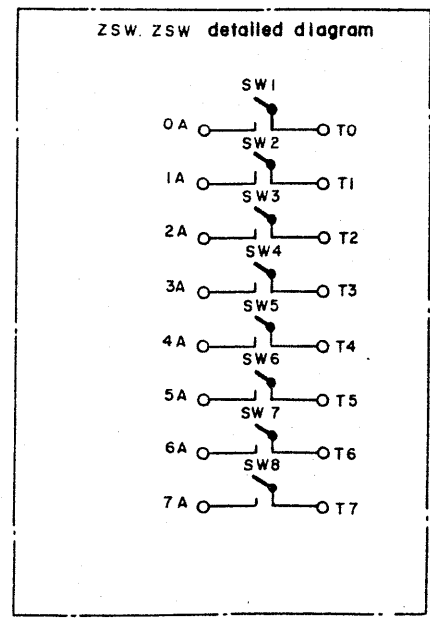
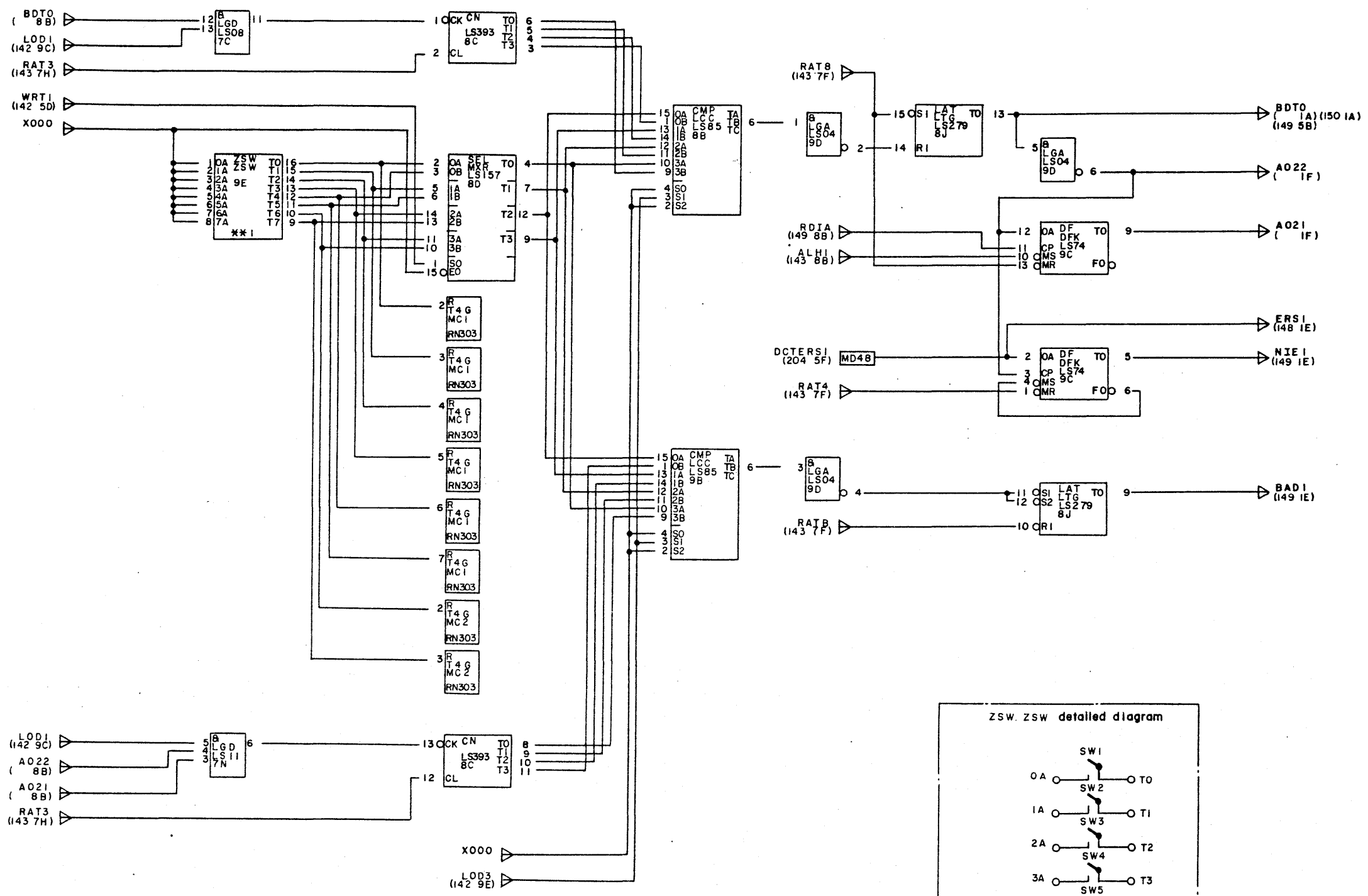
**MTA16X FORMATTER
NRZI CONTROL
CIRCUIT DIAGRAM**
10/12

134-110229-006-0

NEC SHT 10/

H
装置名

134-110229-006

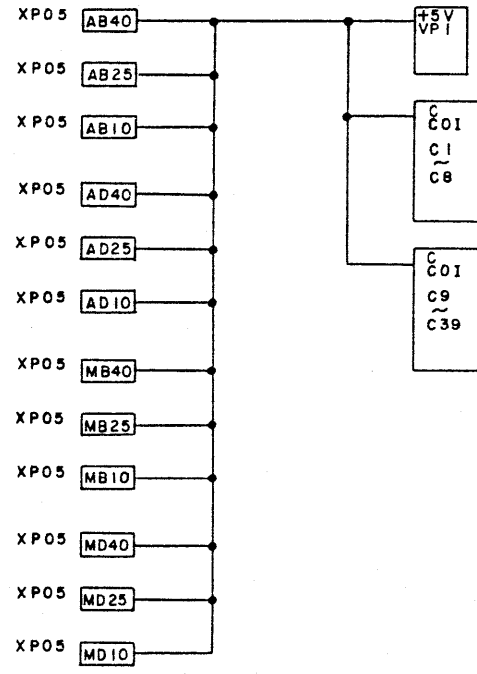
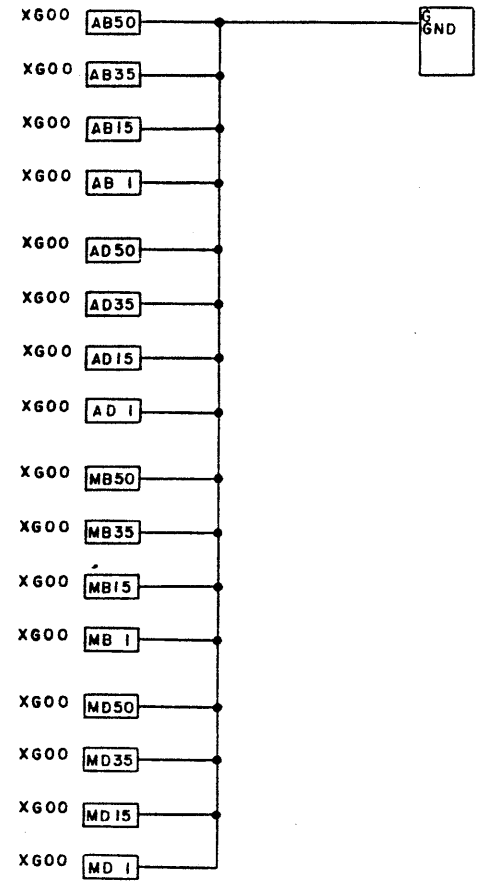


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	NRG			
PKG LOCATION				
PKG NAME	G9JAR			
151				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	
MTAIGX FORMATTER NRZI CONTROL CIRCUIT DIAGRAM 11/12				
134-110229-006-0				
NEC				SHT 11/

装置名

134-110229-006-0



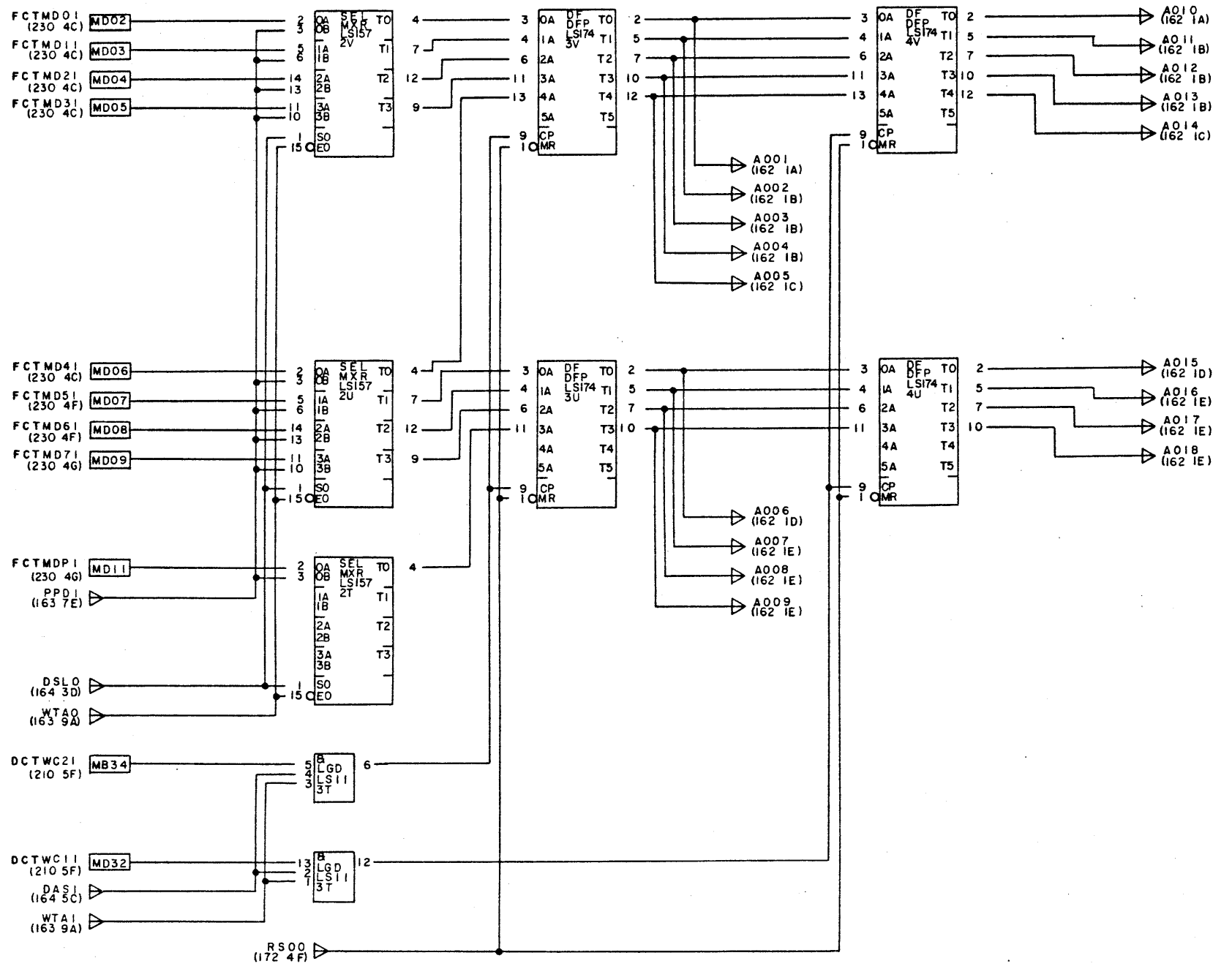
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	—

DWG ABBR	N R G			
PKG LOCATION				
PKG NAME	G 9 J A R			
152				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽 賀		今 村	

MTA16X FORMATTER
NRZI CONTROL
CIRCUIT DIAGRAM
12/12

134-110229-006-0
NEC SHT 12/12

134-110229-005-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
2	0		大橋

DWG ABBR	PEG
PKG LOCATION	
PKG NAME	G9JAS
161	
NEXT SPEC	

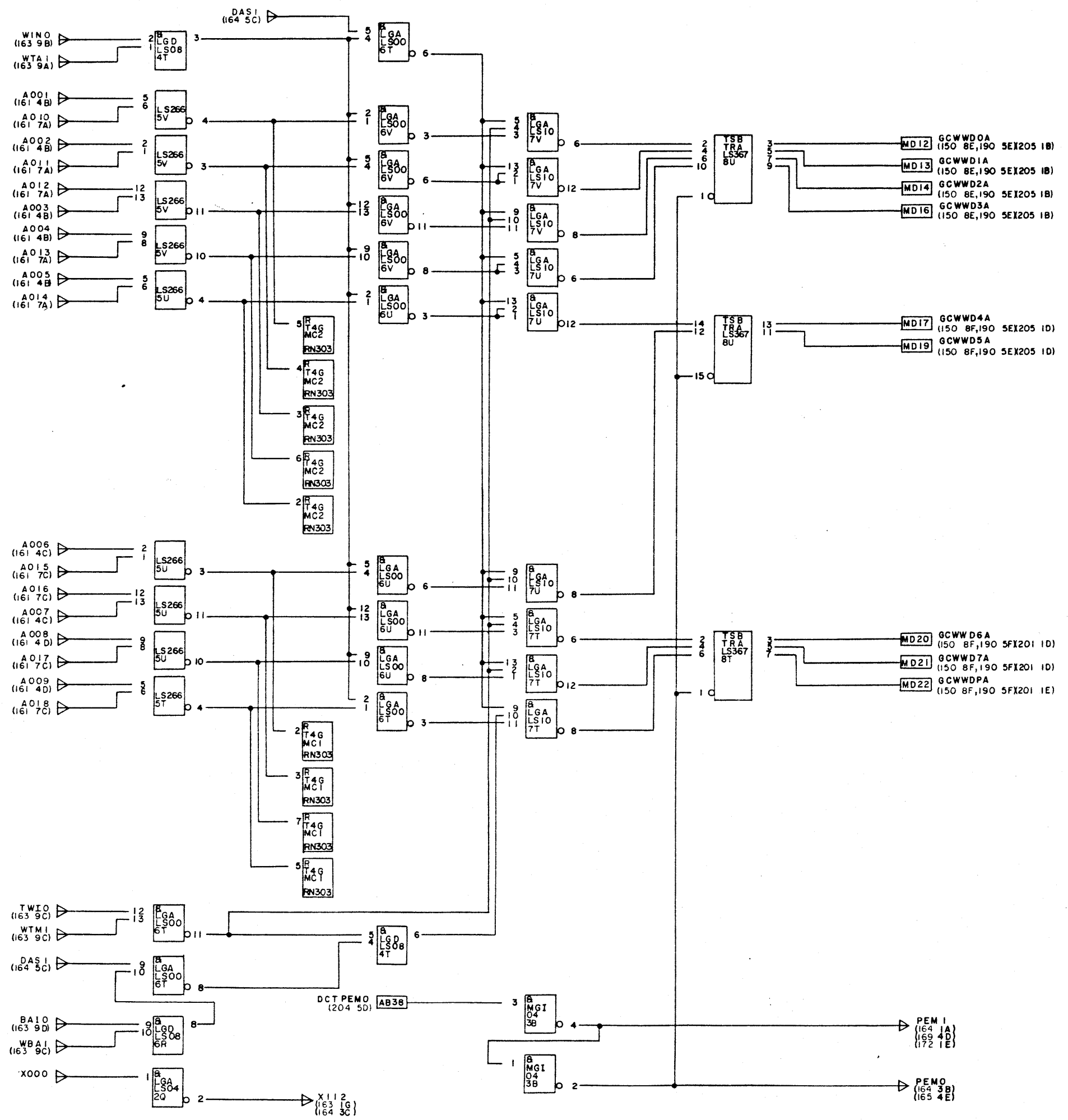
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
1/14

134-110229-005-0

NEC SHT 1/14

134-110229-005-0



REV	COMP	DESCRIPTION (SC)	APP
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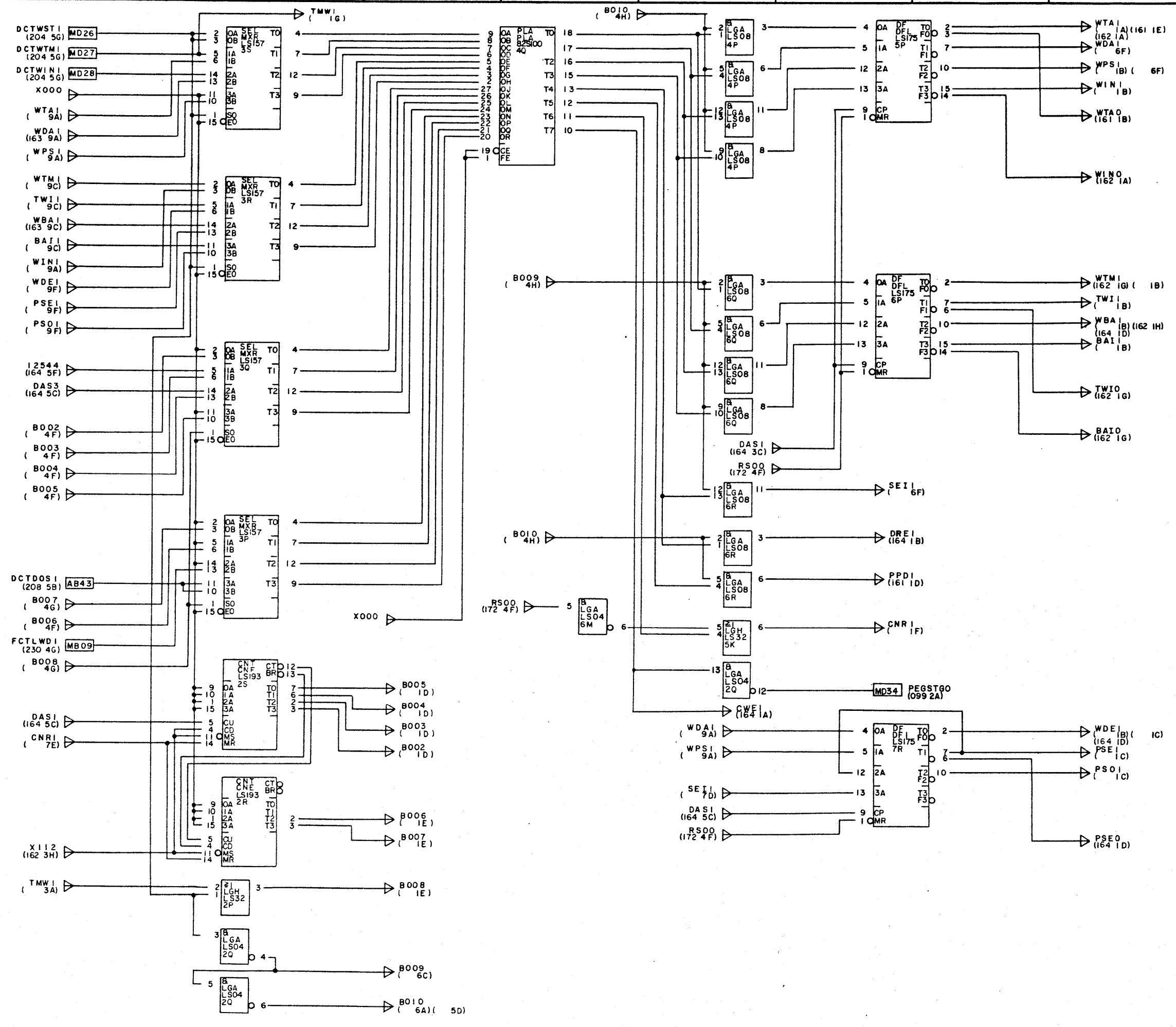
DWG ABBR	PEG			
PKG LOCATION				
PKG NAME	G9JAS			
162				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	山		村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
2/14

134-110229-005-0

NEC SHT 2/

134-110229-005-0



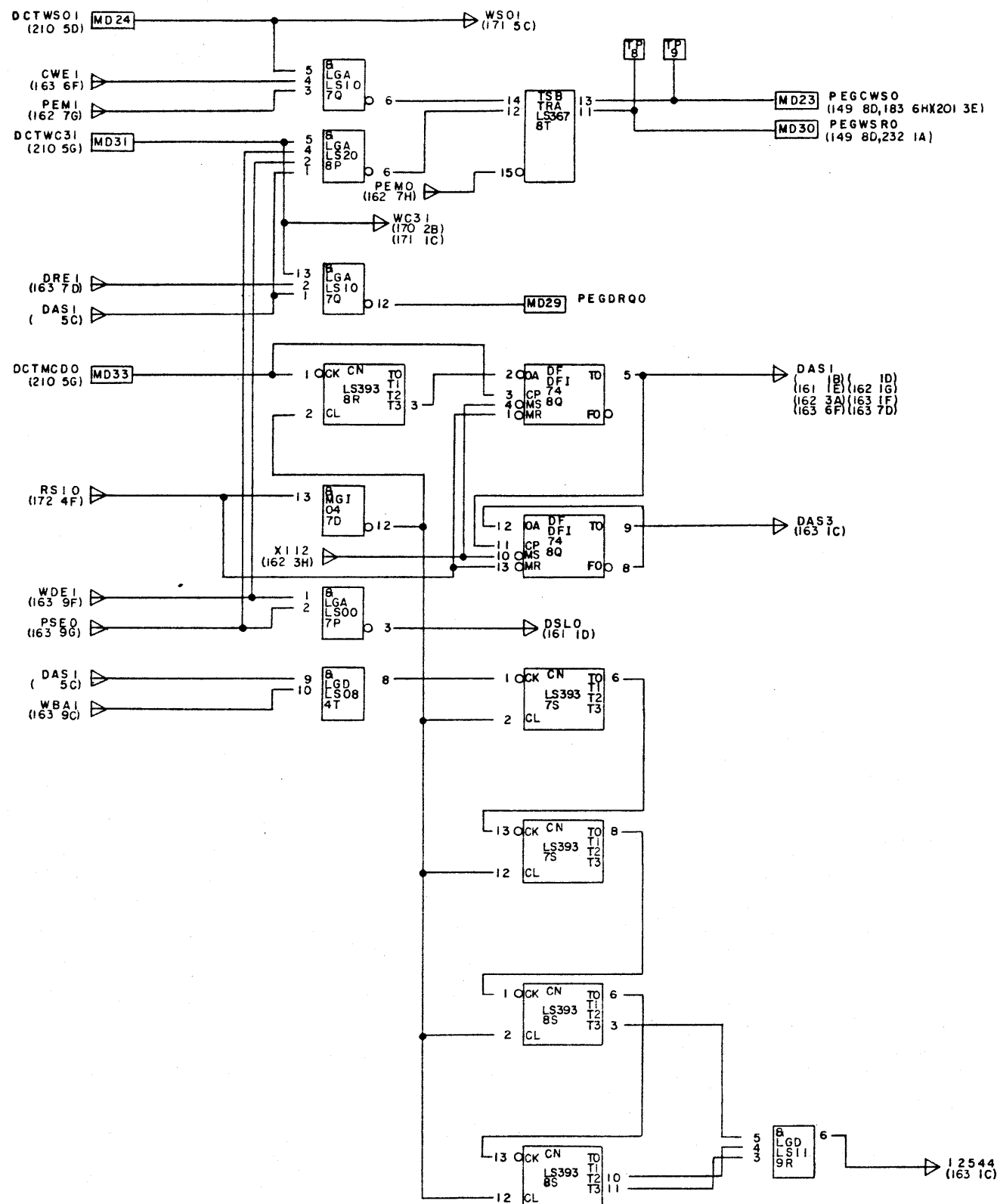
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PEG			
PKG LOCATION				
PKG NAME	G9JAS			
163				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER PE CONTROL CIRCUIT DIAGRAM 3/14				
134-110229-005-0				
NEC				SHR 3/

装置名

DB-413
JIS A2 (420x594)

134-110229-005-0



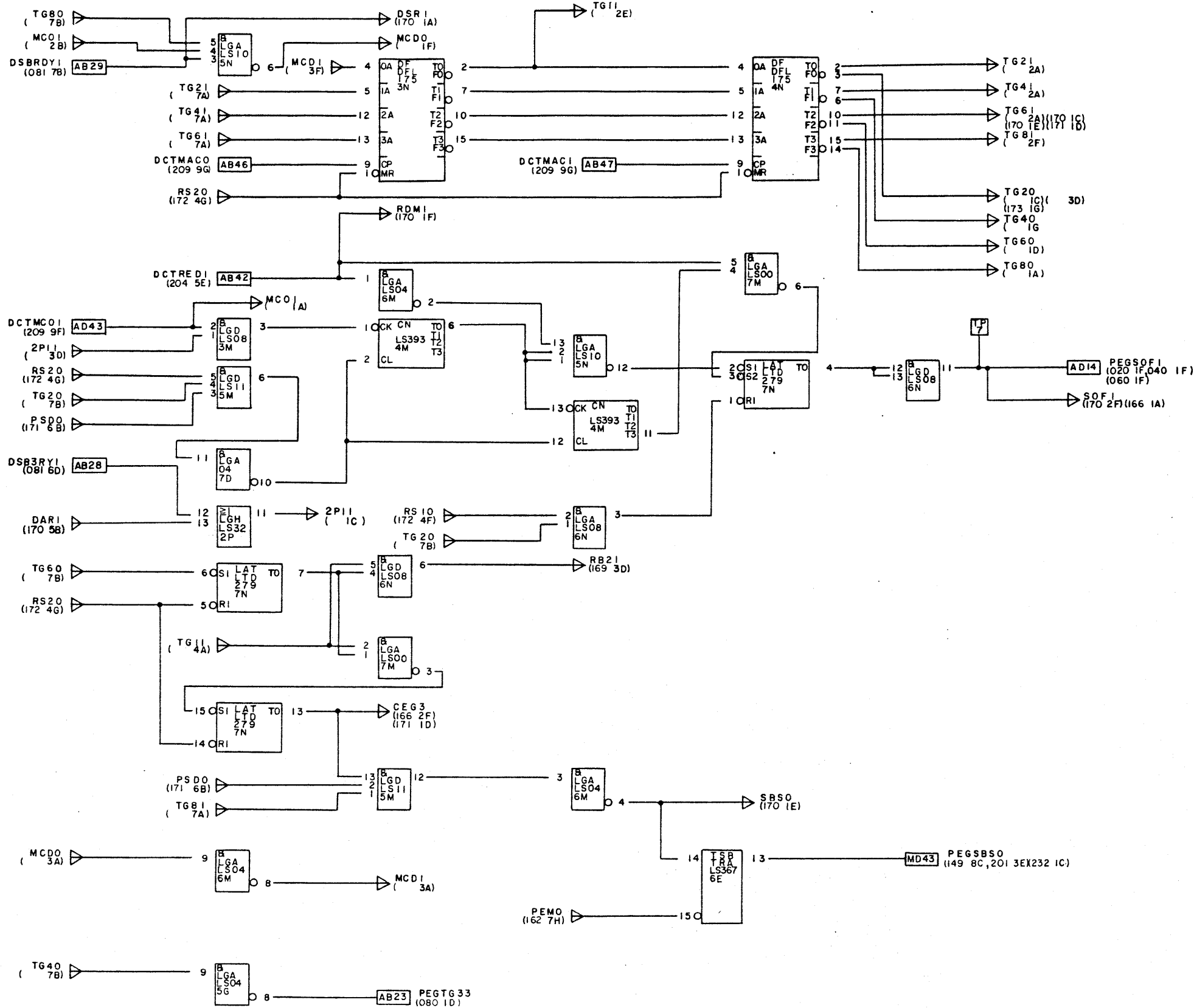
REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	PEG			
PKG LOCATION				
PKG NAME	G9JAS			
164				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
4/14

134-110229-005-0
NEC SHT 4/

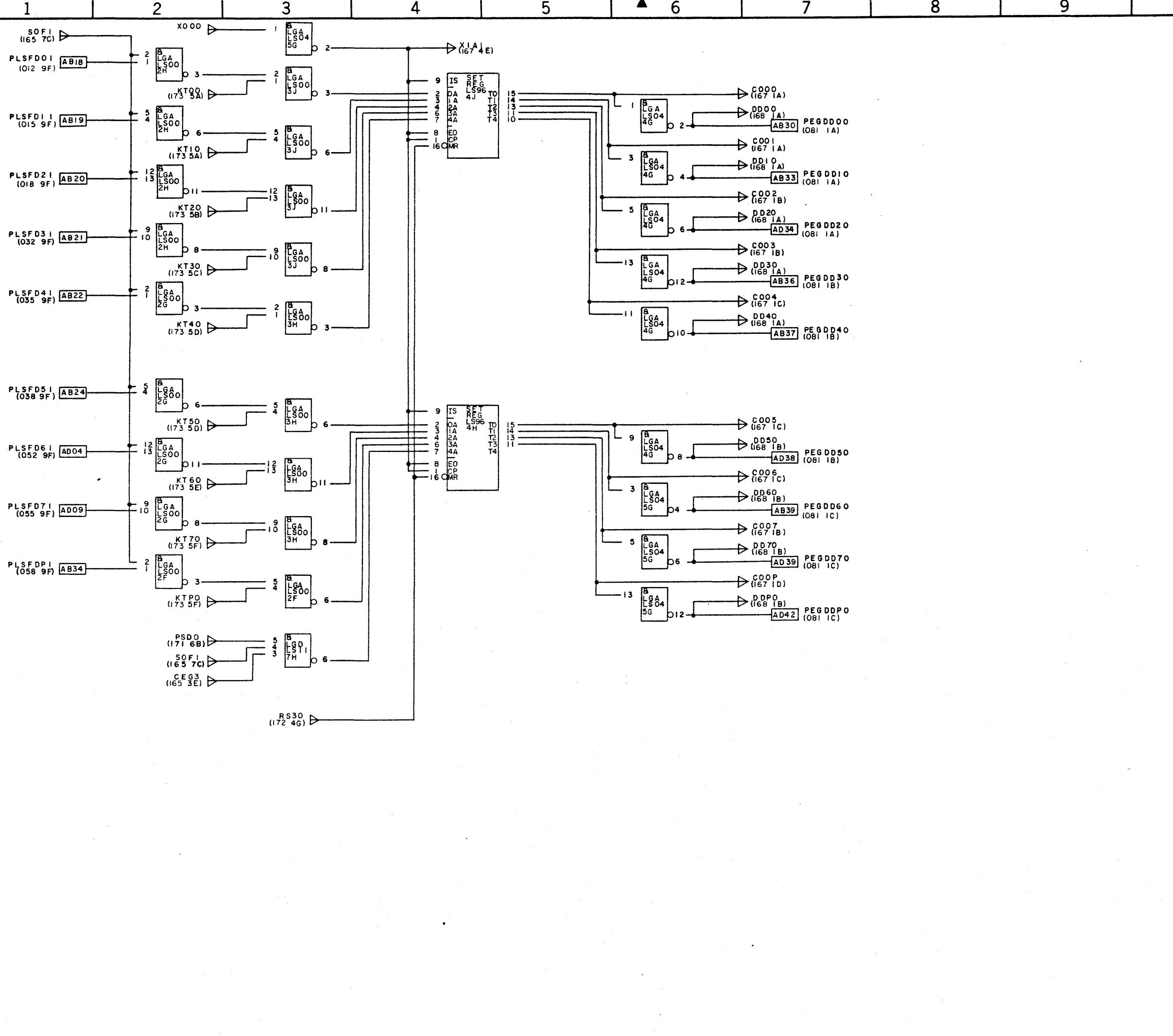
134-110229-005-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	PEG		
PKG LOCATION			
PKG NAME	G9JAS		
165			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER PE CONTROL CIRCUIT DIAGRAM 5/14			
134-110229-005-0			
NEC			SHT 5/

134-110229-005-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

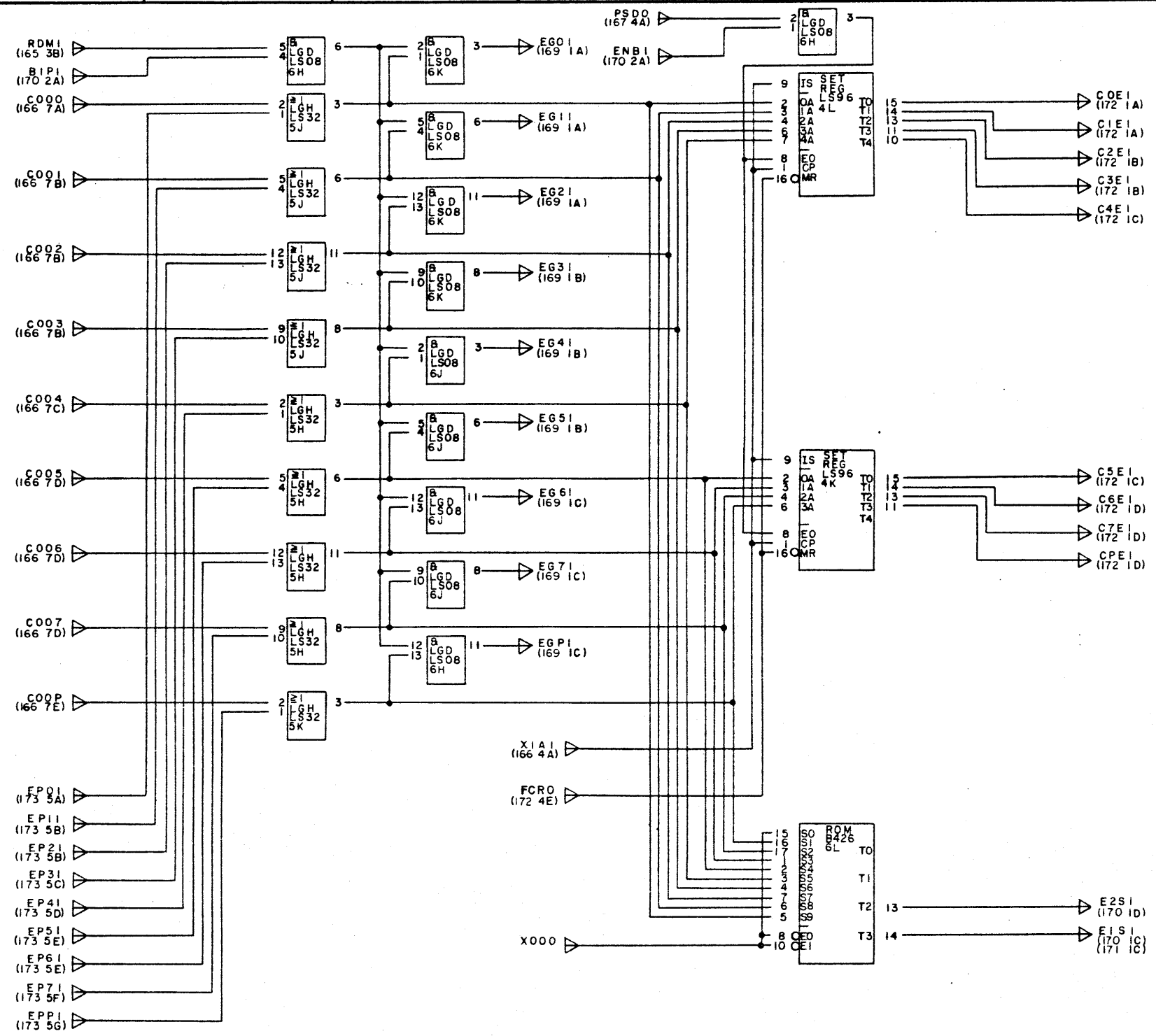
DWG ABBR	PEG			
PKG LOCATION				
PKG NAME	G9JAS			
166				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
6/14

134-110229-005-0

NEC SHT 6/

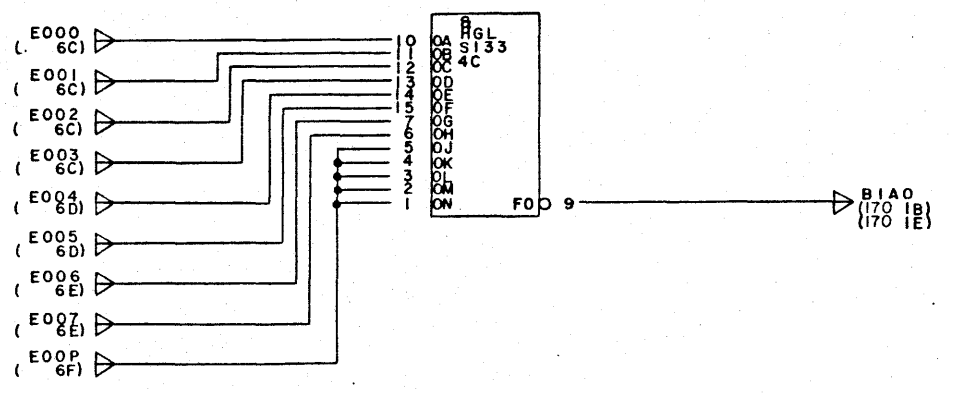
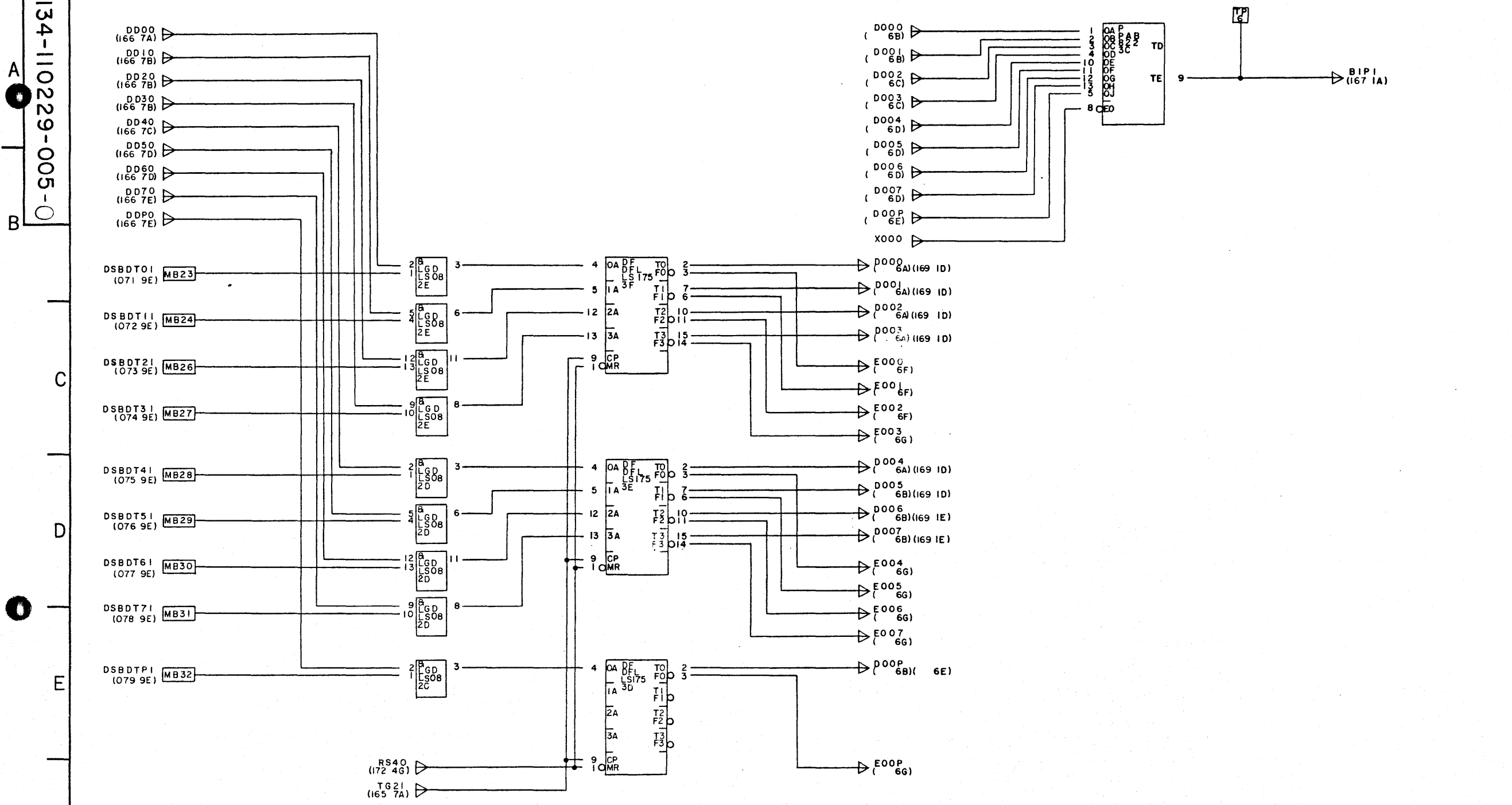
134-110229-005-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	P E G		
PKG LOCATION			
PKG NAME	G9JAS		
167			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER PE CONTROL CIRCUIT DIAGRAM 7/14			
134-110229-005-0			
NEC			SHT 7/

134-110229-005-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	P E G			
PKG LOCATION				
PKG NAME	G 9 J A S			
168				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山 口		今 村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
8/14

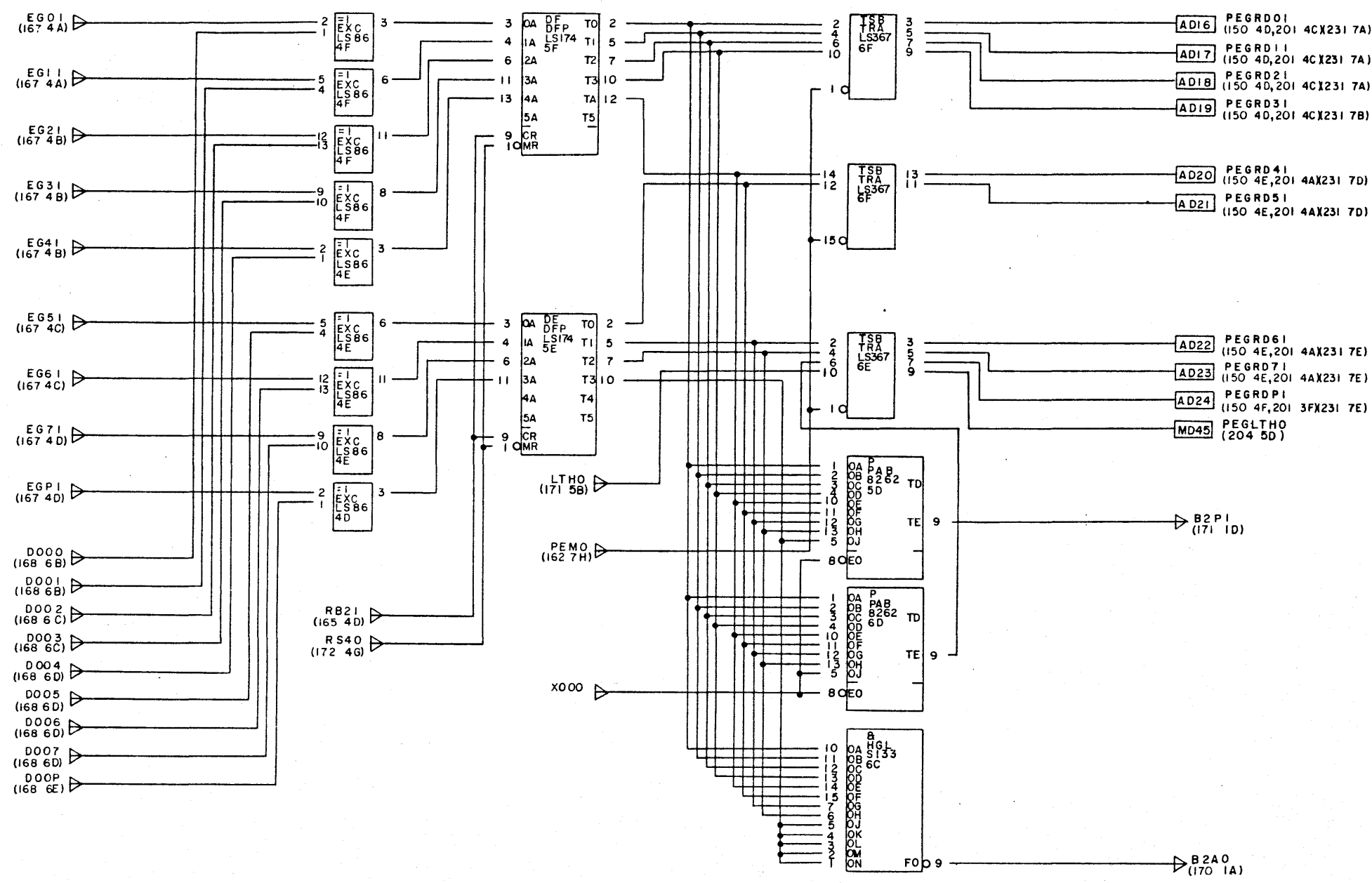
134-110229-005-0

NEC SHT 8/

装置名

134-110229-005-0

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REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

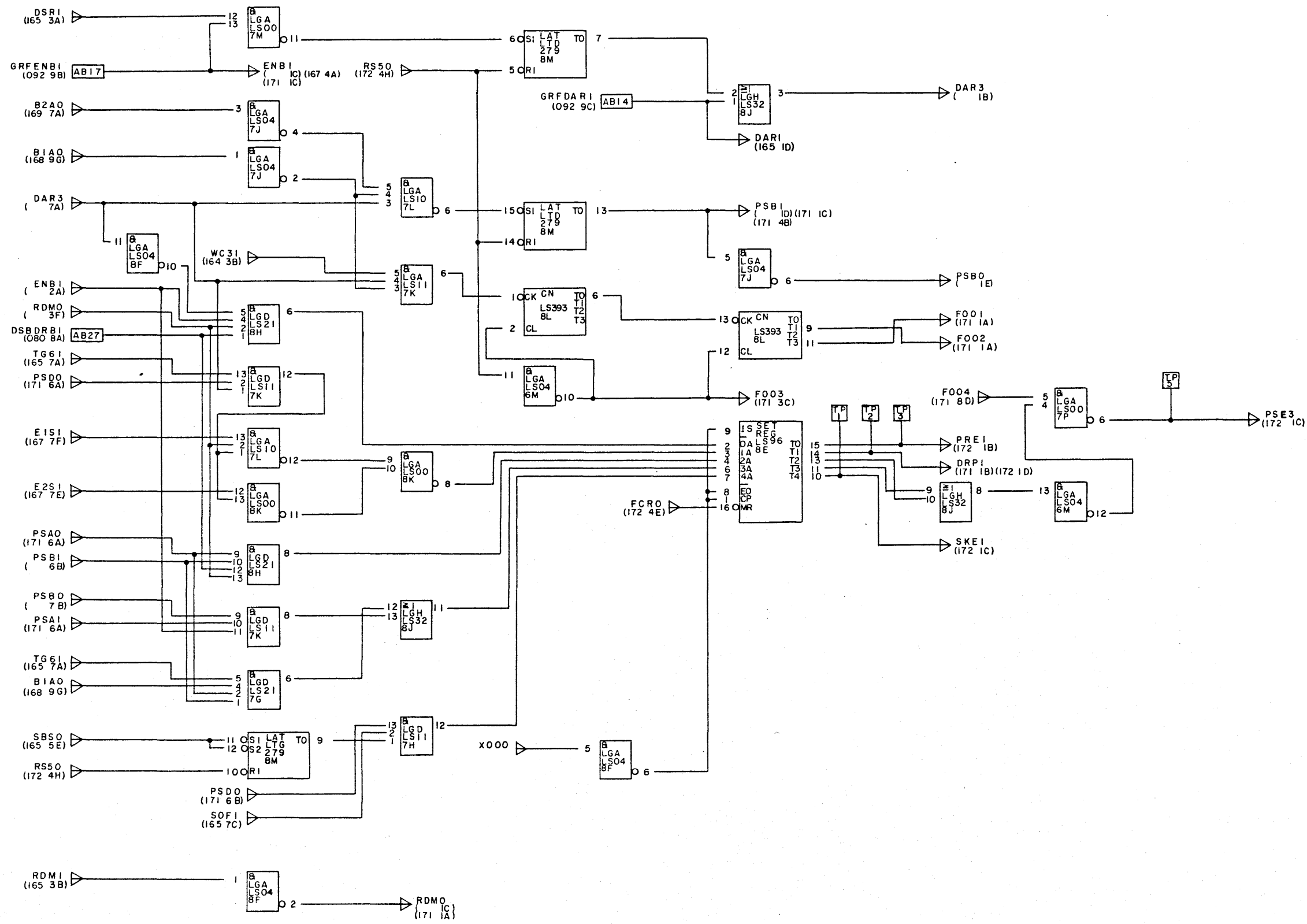
DWG ABBR	PEG			
PKG LOCATION				
PKG NAME	G9JAS			
169				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
9/14

134-110229-005-0

NEC SHT 9/

134-110229-005-0



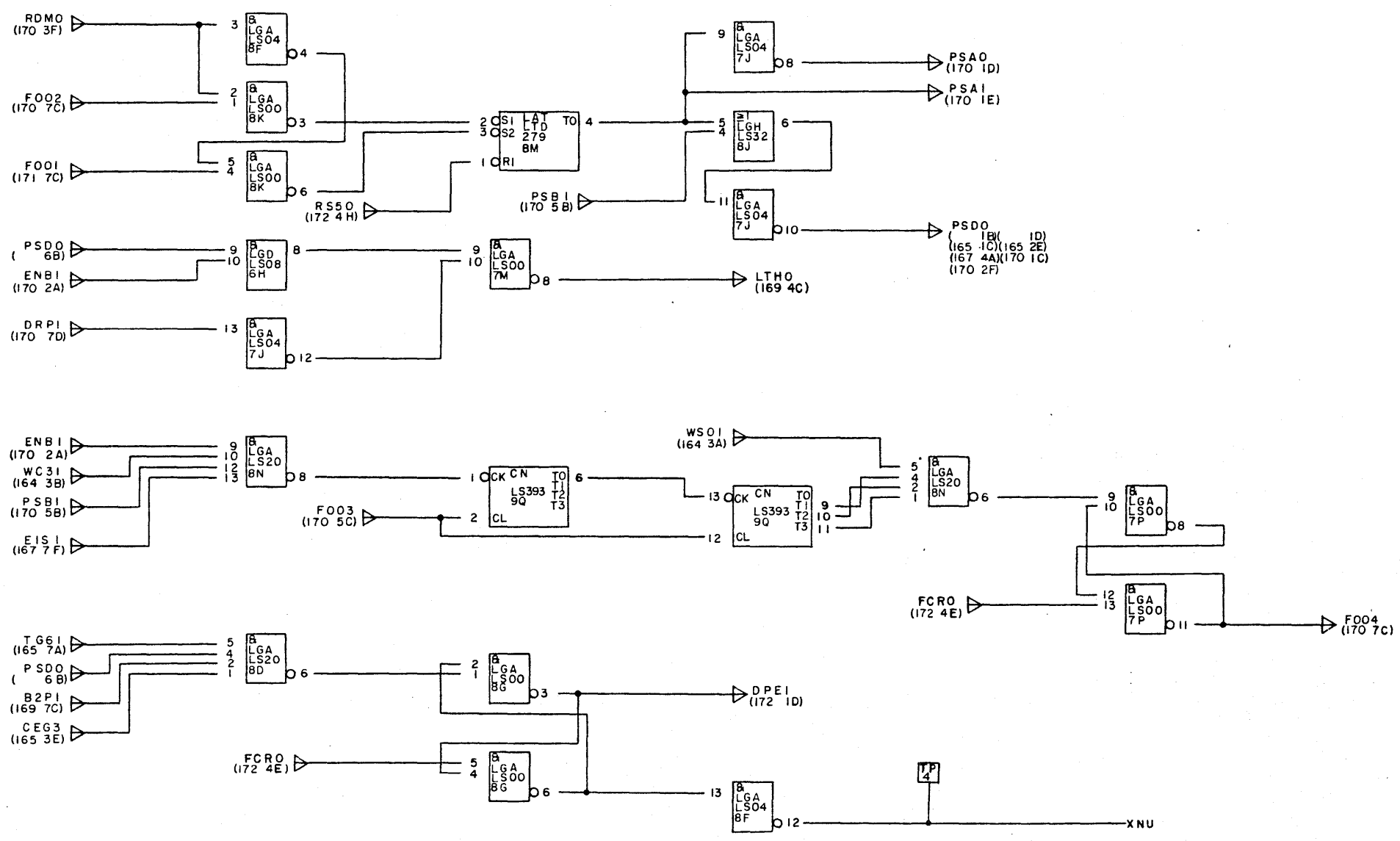
DWG ABBR	P E G			
PKG LOCATION				
PKG NAME	G 9 J A S			
170				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
10/14

134-110229-005-

NEC SHT 10/

134-110229-005-



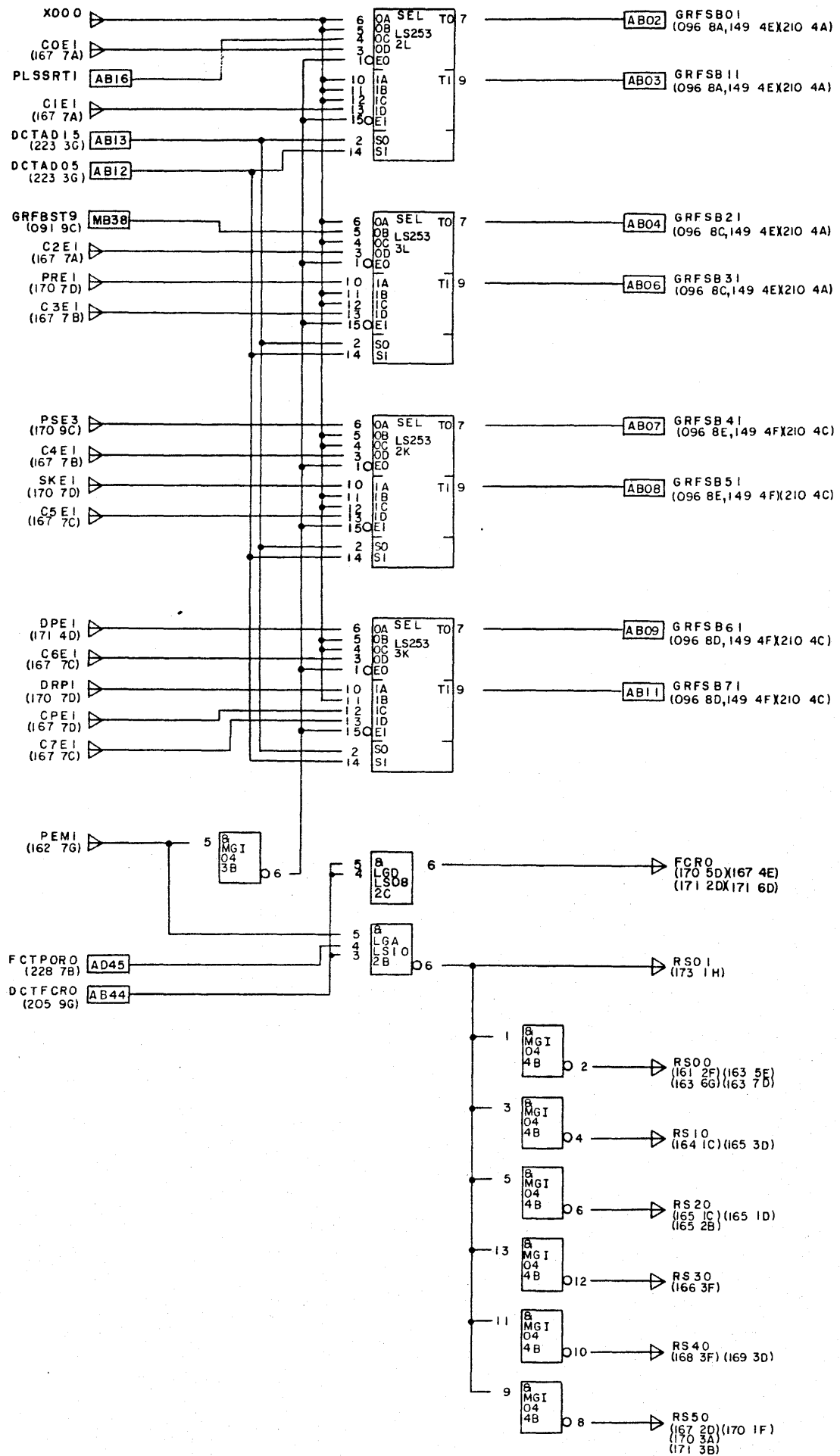
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	P E G			
PKG LOCATION				
PKG NAME	G 9 J A S			
171				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
11/14

134-110229-005-
NEC SHT 11/

134-110229-005-



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PEG
PKG LOCATION	
PKG NAME	G9JAS
172	

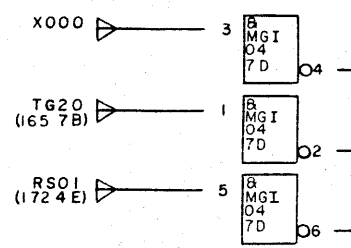
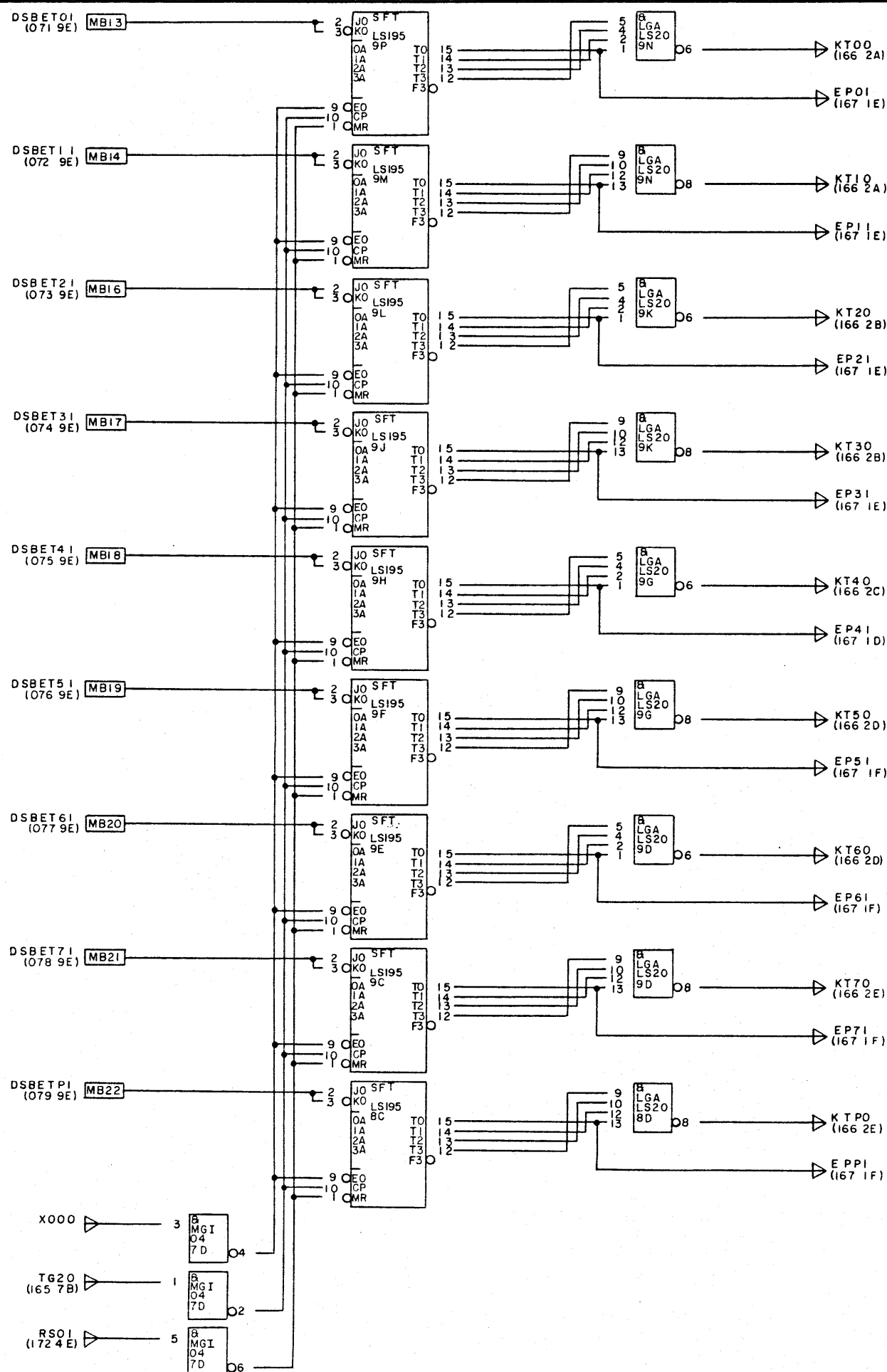
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
12/14

134-110229-005-

NEC SHT 12/

134-110229-005-0

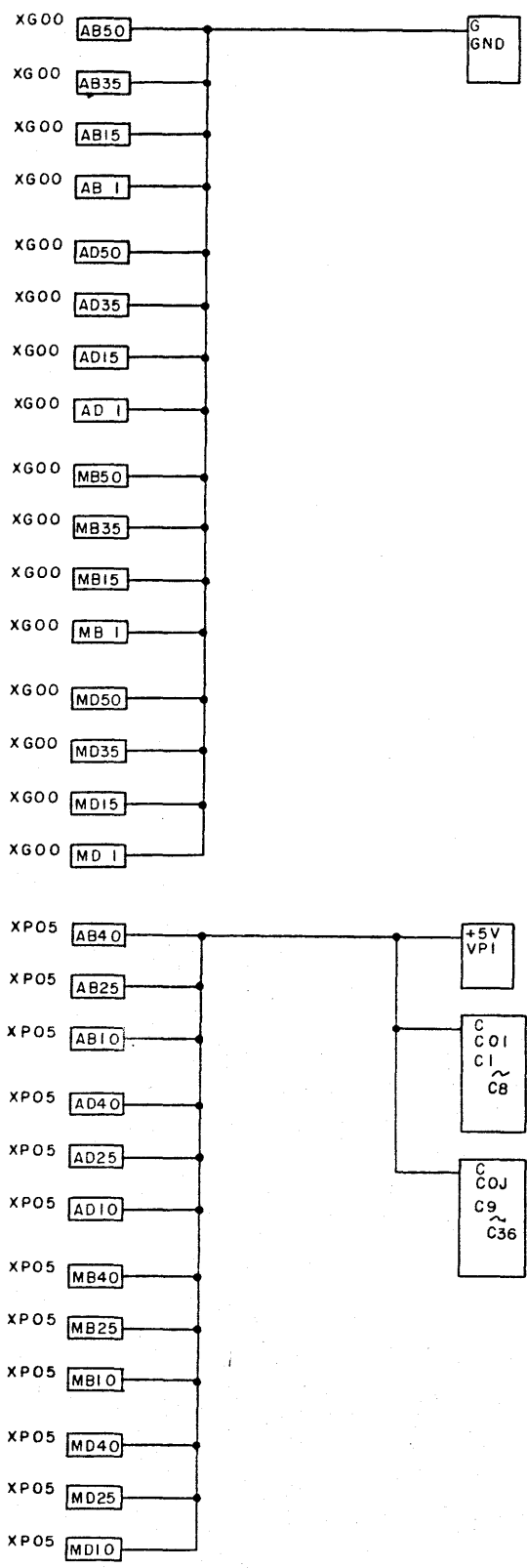


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	PEG			
PKG LOCATION				
PKG NAME	G9JAS			
173				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER PE CONTROL CIRCUIT DIAGRAM 13/14				
134-110229-005-0				
NEC				SHT 13/

134-110229-005-0



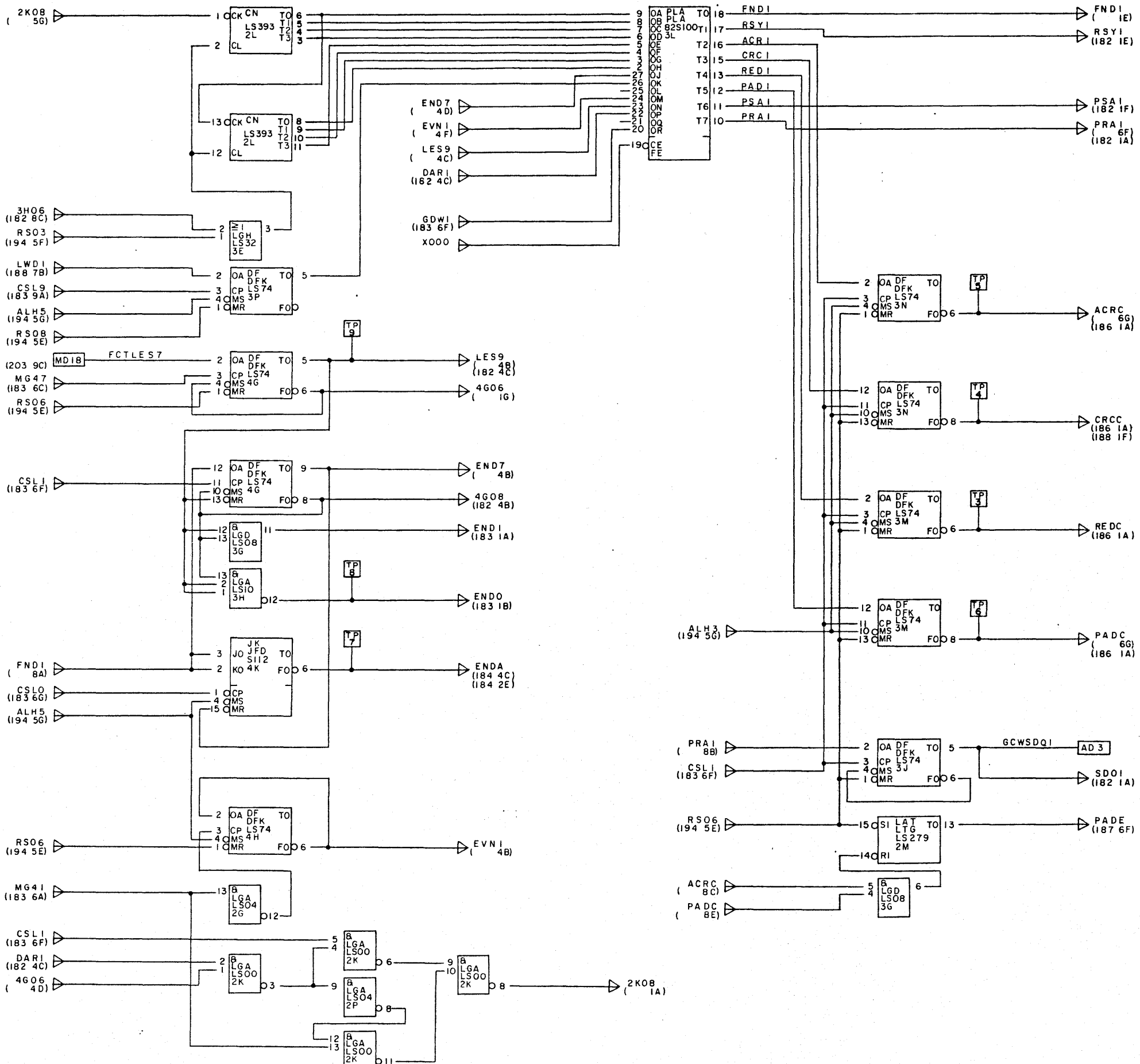
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	P E G			
PKG LOCATION				
PKG NAME	G 9 J A S			
174				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山 口		今 村	

MTA16X FORMATTER
PE CONTROL
CIRCUIT DIAGRAM
14/14

134-110229-005-0
NEC SHT 14/14

134-110229-004-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
2	0	1982.8.15	大橋 羽賀

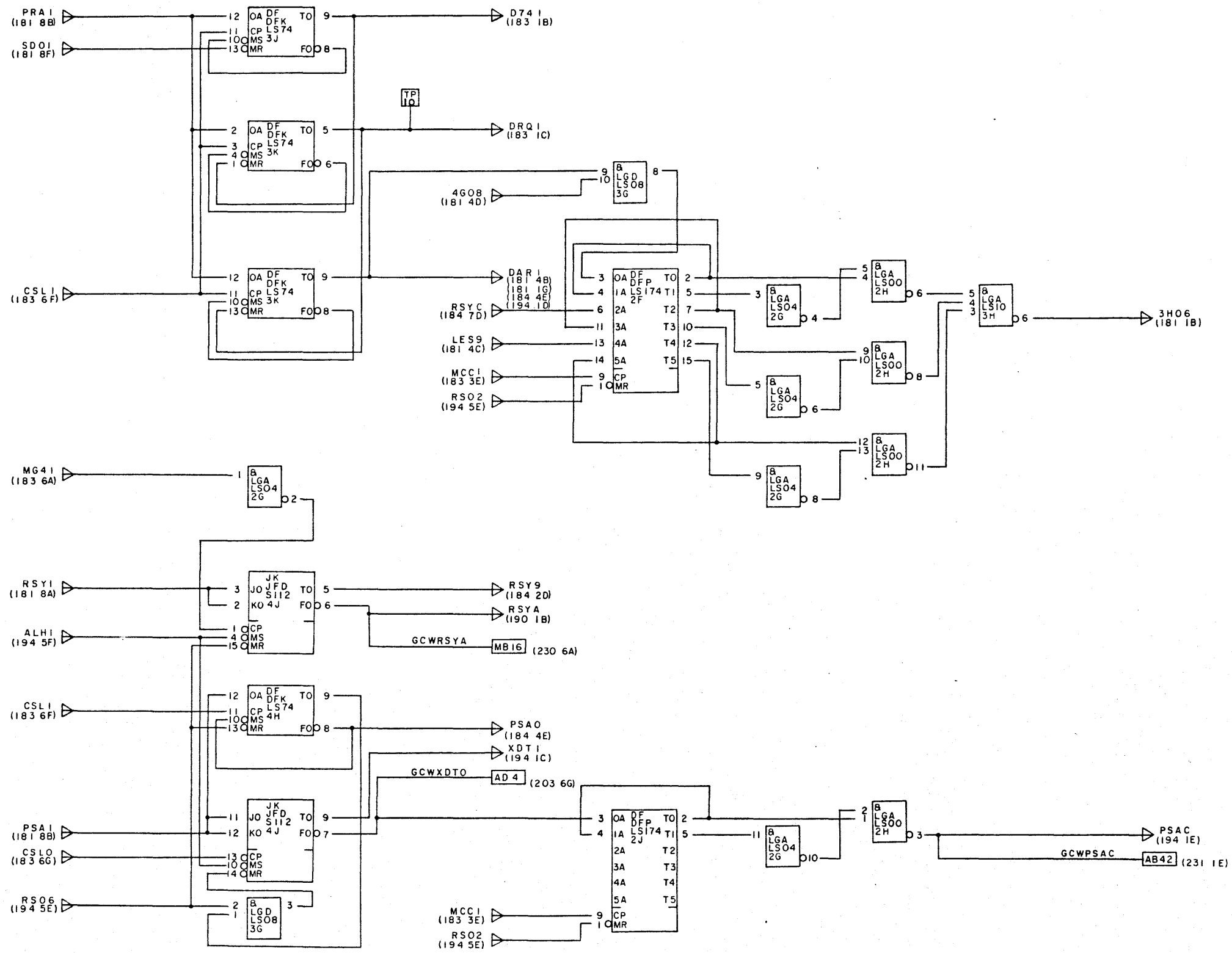
DWG ABBR	G C W			
PKG LOCATION				
PKG NAME	G9JAT,G9MWU			
181				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山羽		今村	
MTA16X FORMATTER GCR CONTROL IN WRITE CIRCUIT DIAGRAM 1/15				
134-110229-004-0				
NEC				SHT 1/15

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装置名

134-110229-004-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	G C W
PKG LOCATION	
PKG NAME	G9JAT,G9MWU
182	

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	

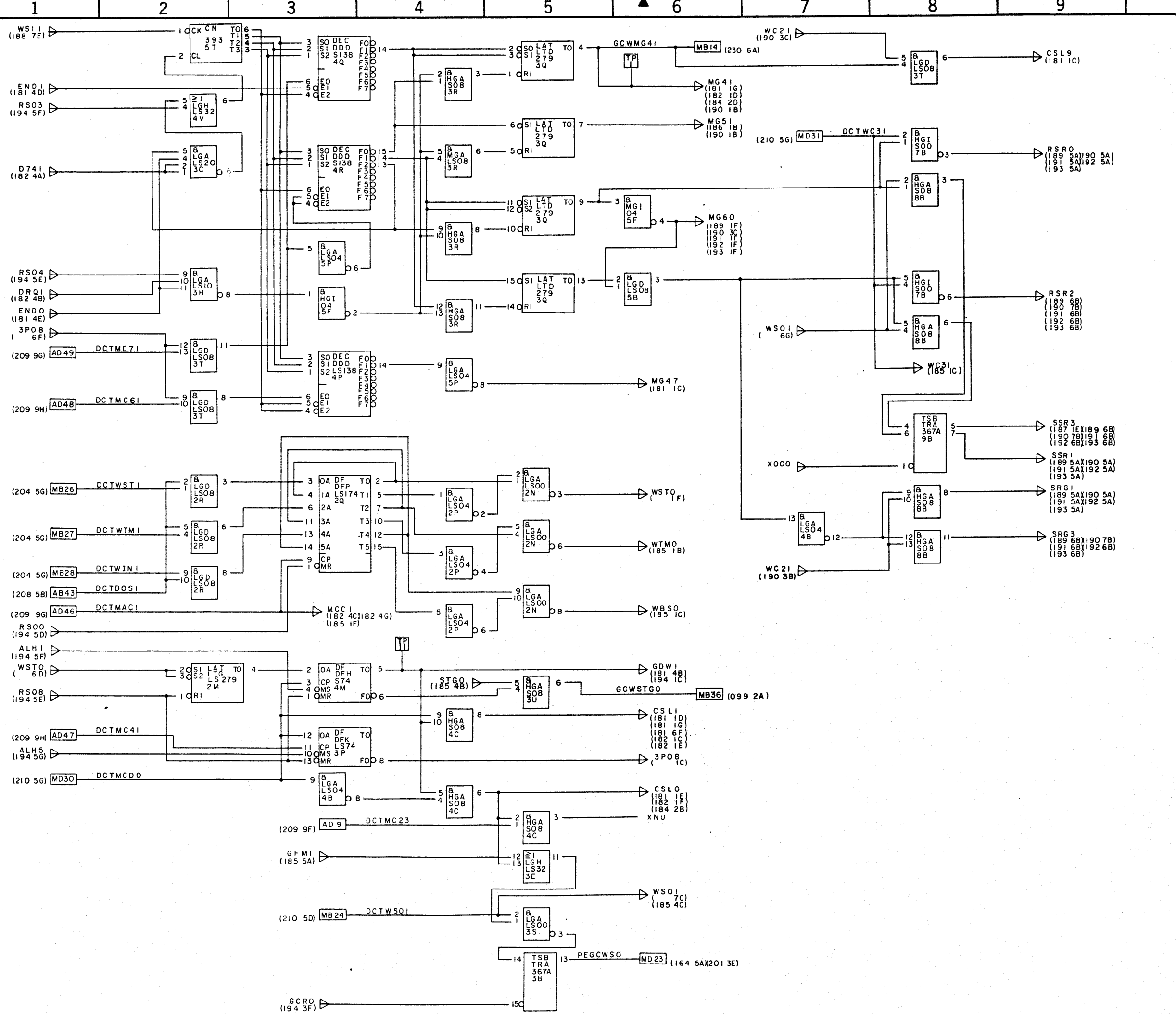
MTA16X FORMATTER
GCR CONTROL
IN WRITE
CIRCUIT DIAGRAM
2/15

134-110229-004-0
NEC SHT 2/

A
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134-110229-004-0

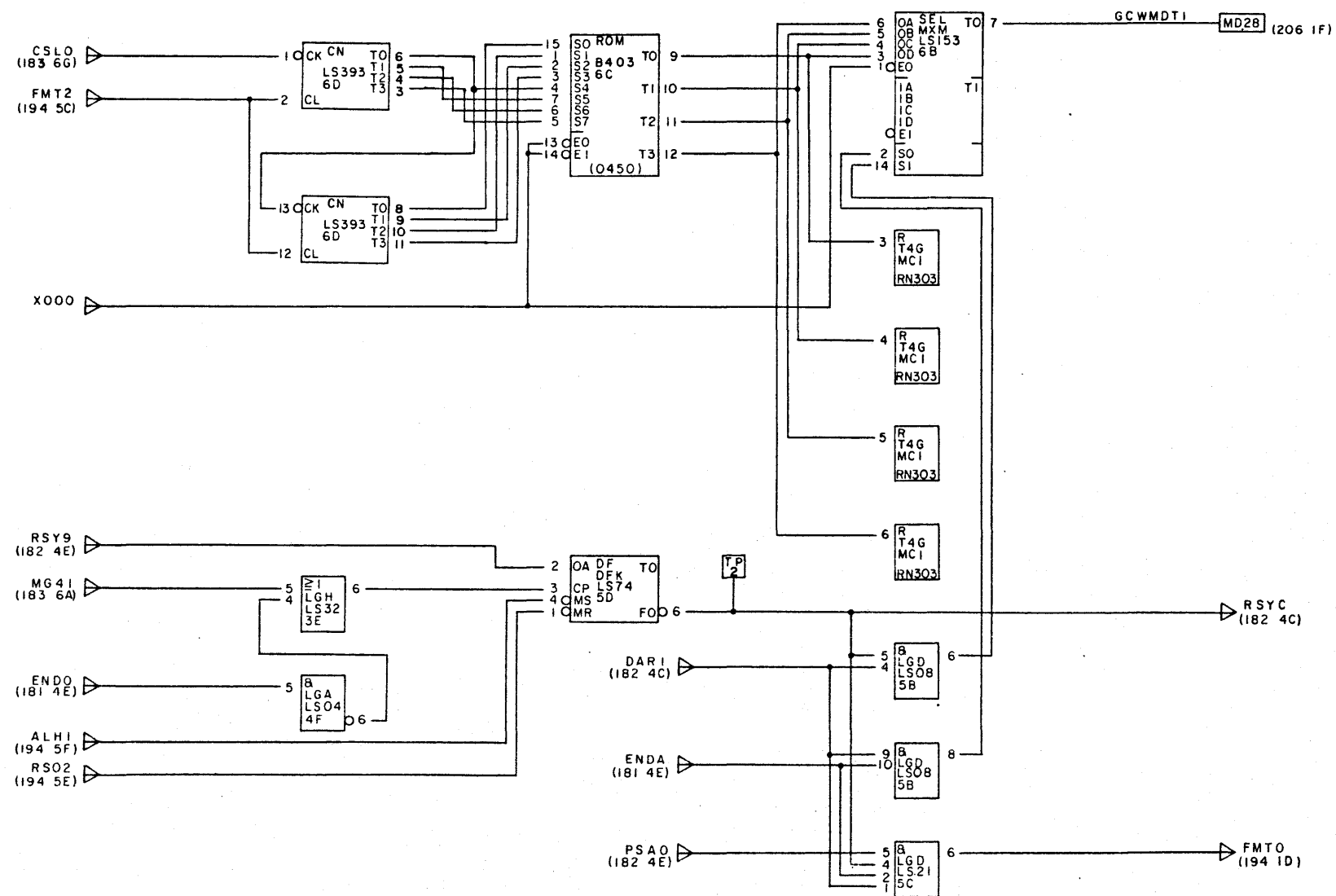


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G C W			
PKG LOCATION				
PKG NAME	G9JAT,G9MWU			
183				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽 賀		今 村	
MTAIX FORMATTER GCR CONTROL IN WRITE CIRCUIT DIAGRAM 3/15				
134-110229-004-0				
NEC				SHT 3/

装置名

134-110229-004



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G C W
PKG LOCATION	
PKG NAME	G9JAT, G9MWU

184

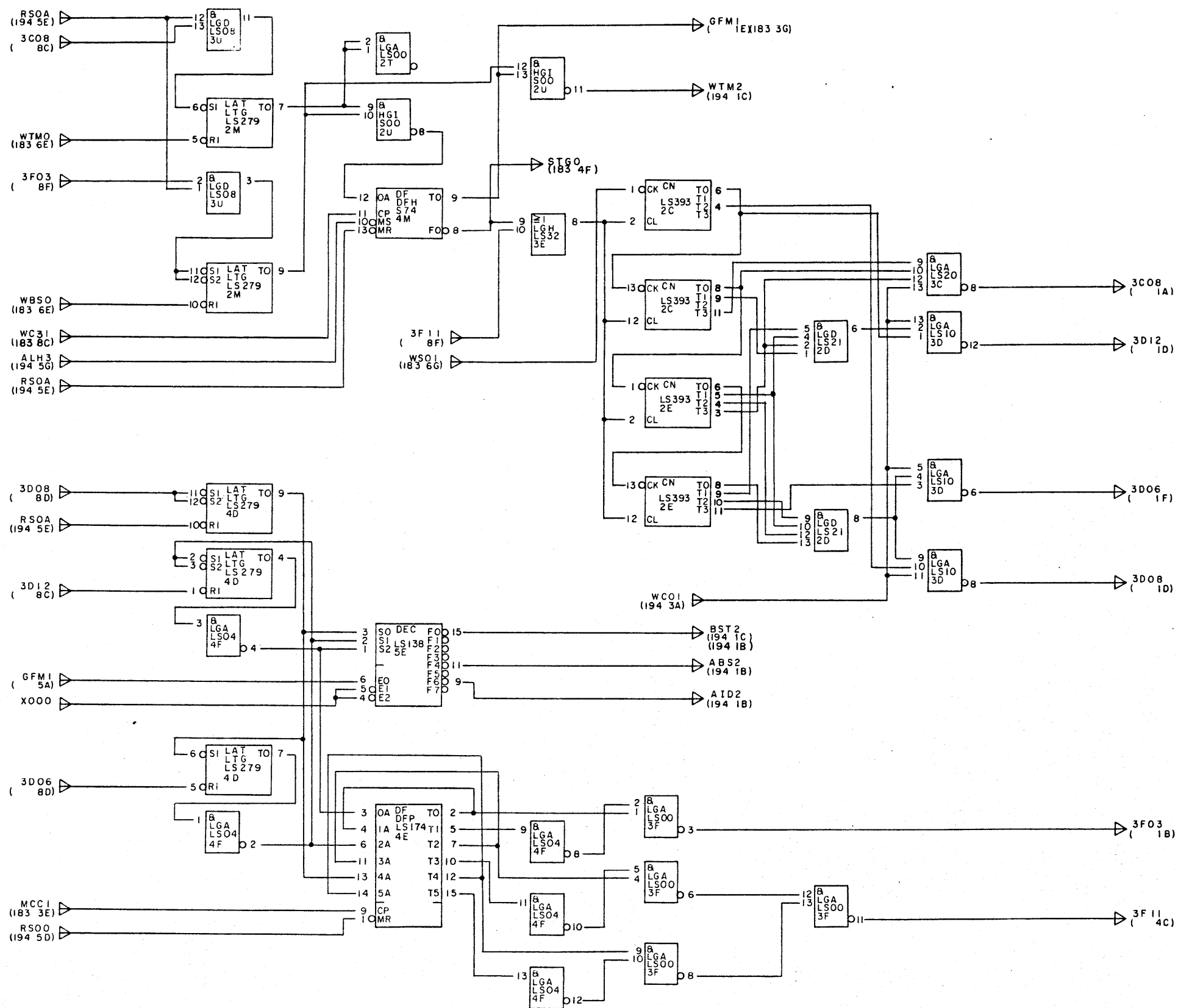
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
GCR CONTROL
IN WRITE
CIRCUIT DIAGRAM
4/15

134-110229-004

NEC SHT 4/

134-110229-004-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

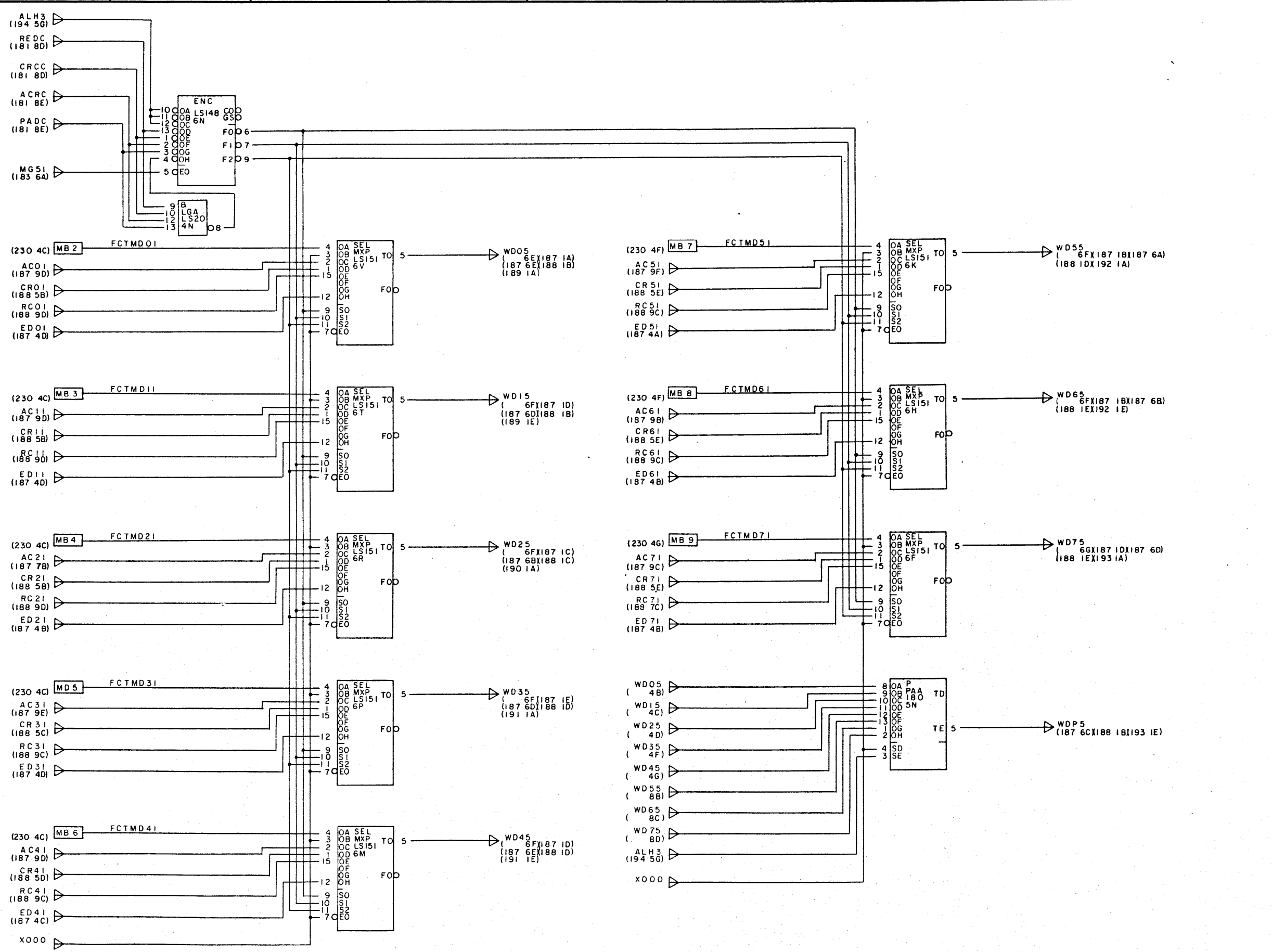
DWG ABBR	G C W			
PKG LOCATION				
PKG NAME	G9JAT,G9MWU			
185				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	

MTA16X FORMATTER
GCR CONTROL
IN WRITE
CIRCUIT DIAGRAM
5/15

134-110229-004-0

NEC SH 5/

134-110229-004



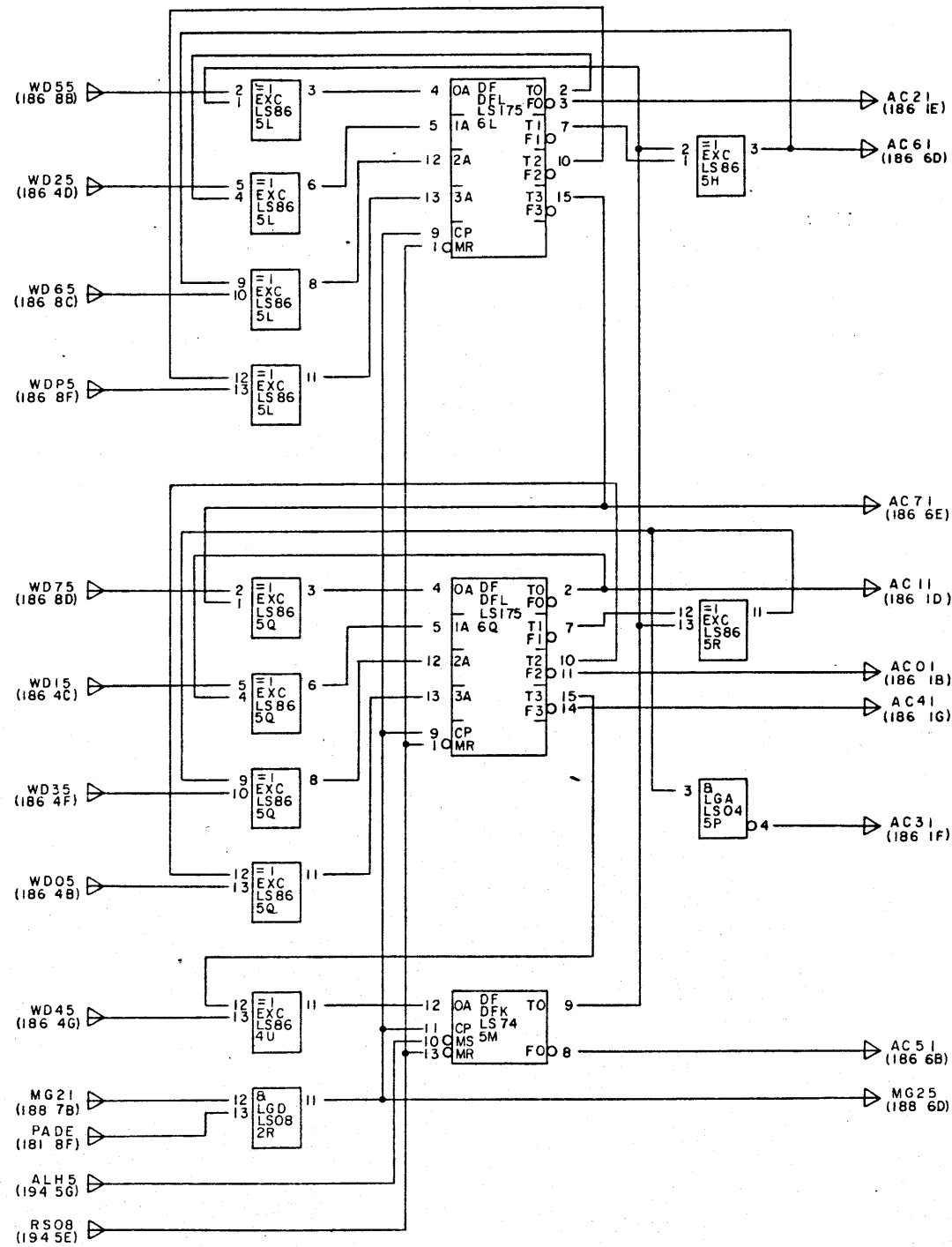
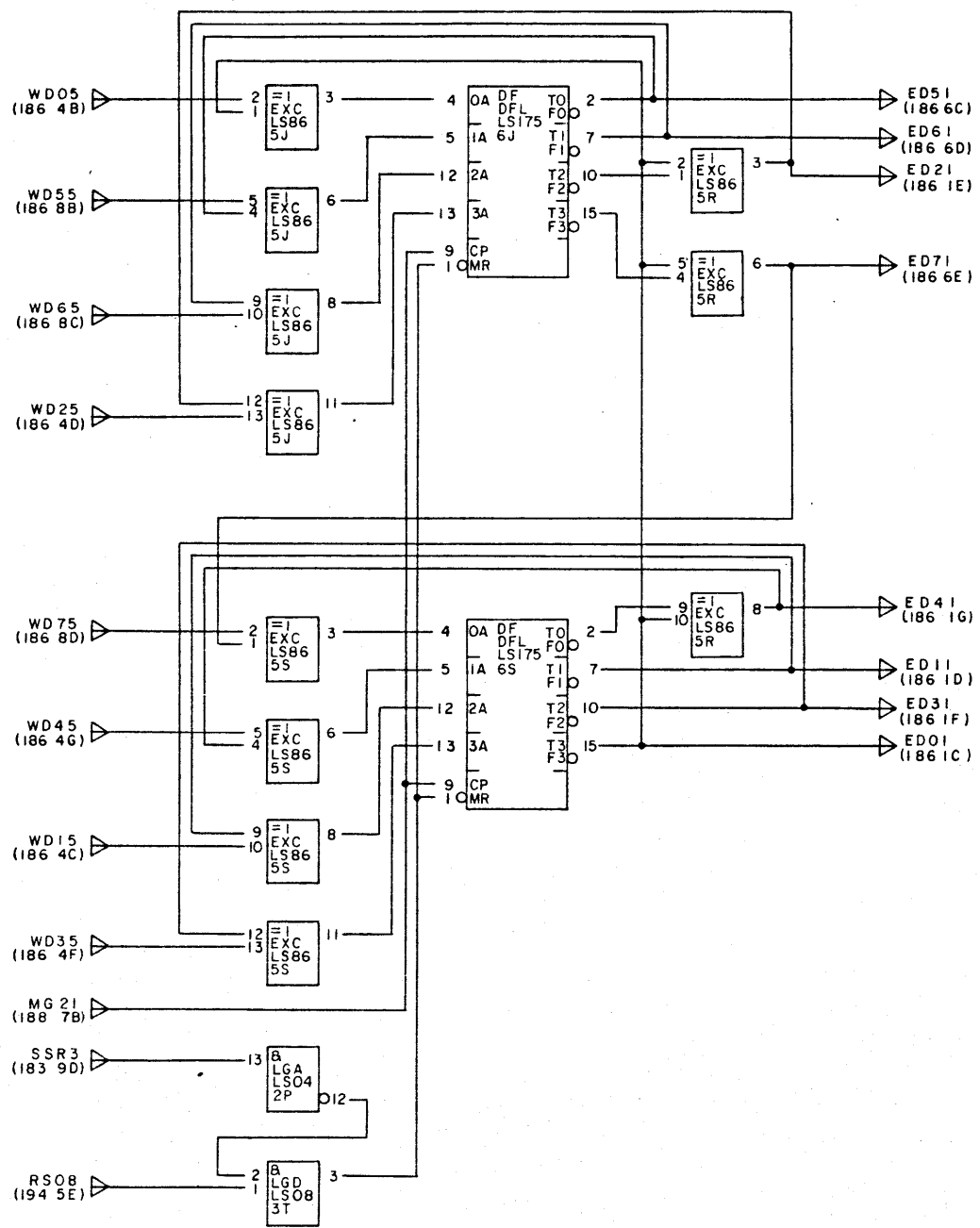
REV	COMP	DESCRIPTION (SC)	APP
1	0	55, 5.5	

DWG ABBR	G C W		
PKG LOCATION			
PKG NAME	G9JAT,G9MWU		
186			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽		今
	賀		村
MTAIX FORMATTER GCR CONTROL IN WRITE CIRCUIT DIAGRAM 6/15			
134-110229-004			
NEC			SHT 6/

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134-110229-004-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G C W
PKG LOCATION	
PKG NAME	G9JAT,G9MWU
187	

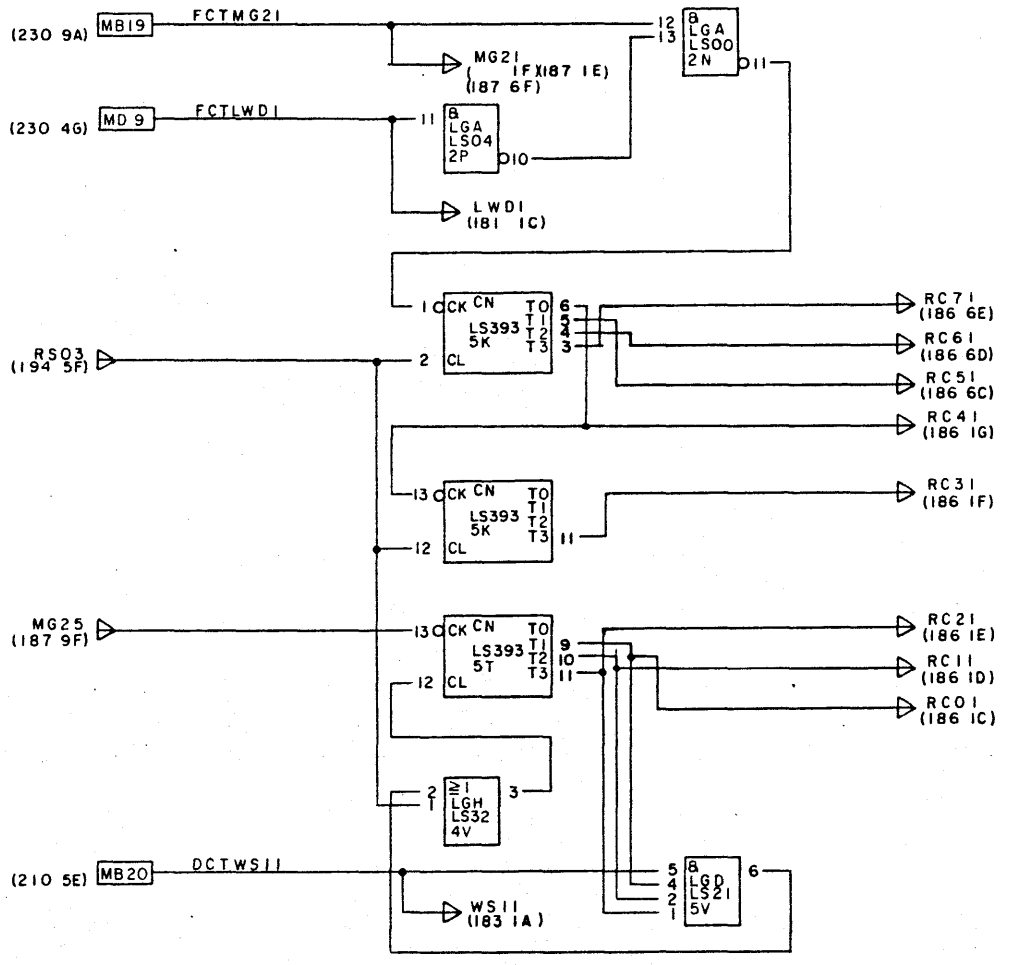
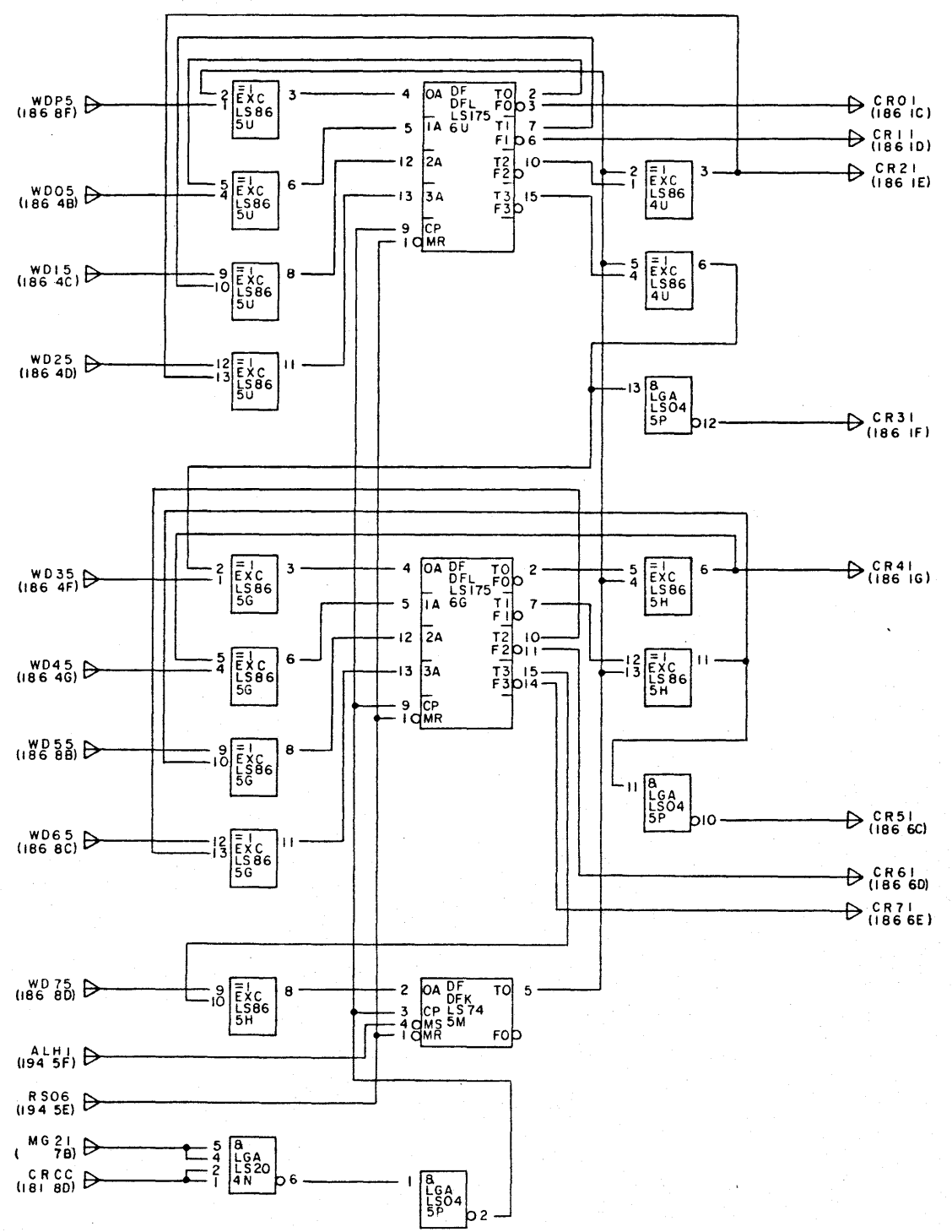
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	

MTA16X FORMATTER
GCR CONTROL
IN WRITE
CIRCUIT DIAGRAM
7/15

134-110229-004-0

NEC SHT 7/

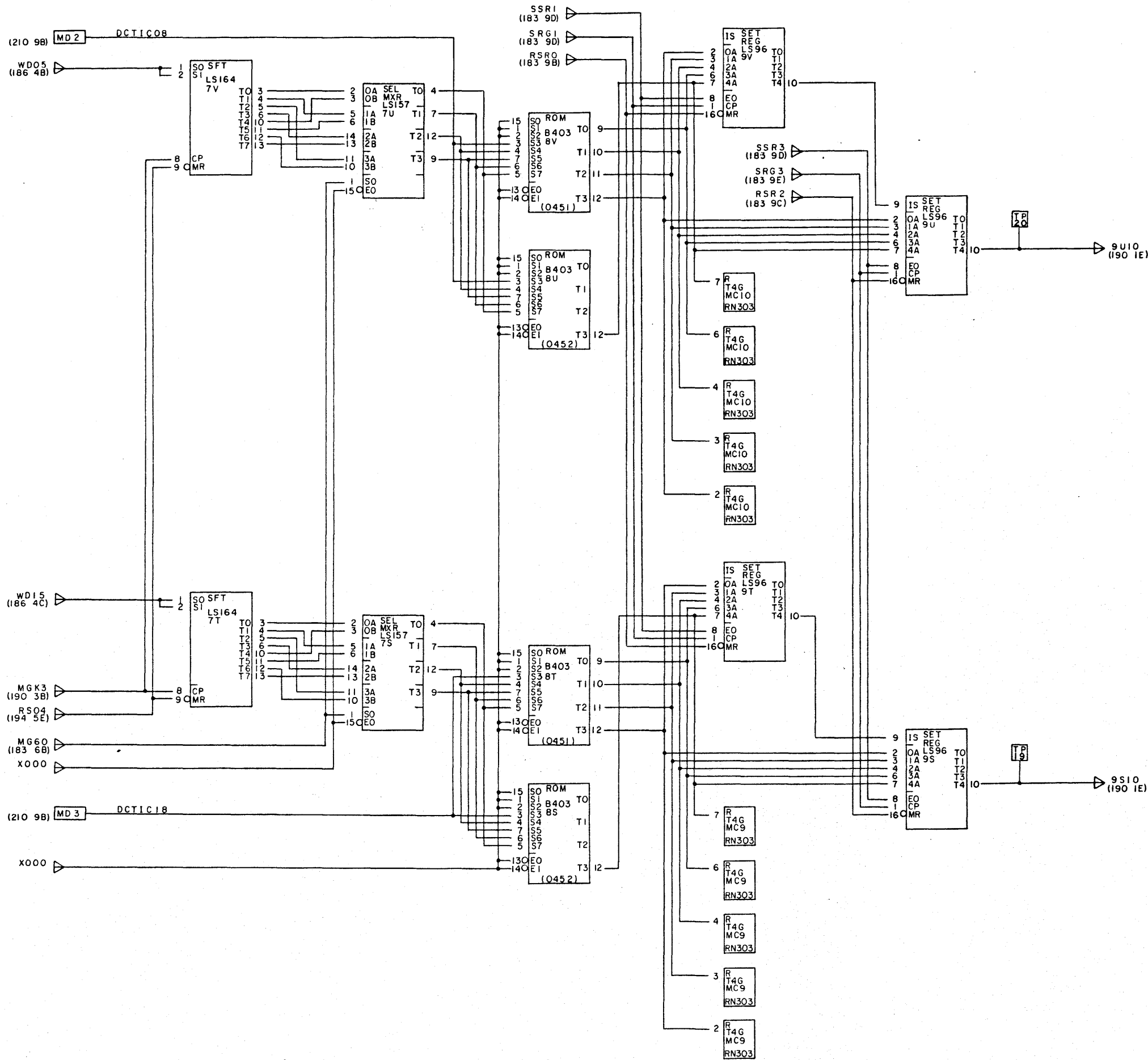
134-110229-004-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR		G C W		
PKG LOCATION				
PKG NAME G9JAT, G9MWU				
188				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	
MTA16X FORMATTER GCR CONTROL IN WRITE CIRCUIT DIAGRAM 8/15				
134-110229-004-0				
NEC				SHT 8/

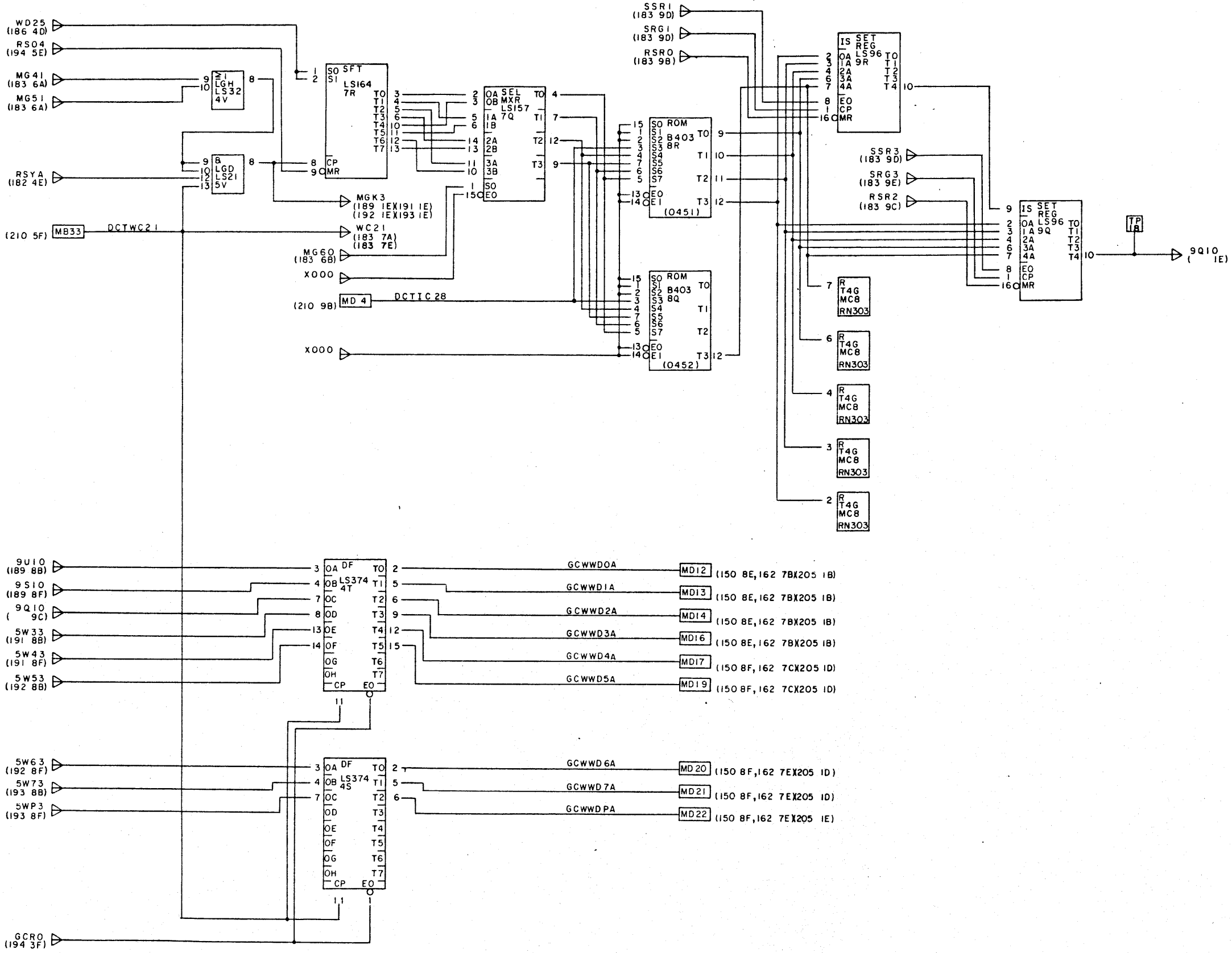
134-110229-004-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55, 5.5	

DWG ABBR	G C W			
PKG LOCATION				
PKG NAME	G9JAT, G9MWU			
189				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	
MTA16X FORMATTER GCR CONTROL IN WRITE CIRCUIT DIAGRAM 9/15				
134-110229-004-0				
NEC				SHT 9/

134-110229-004-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G C W
PKG LOCATION	
PKG NAME	G9JAT,G9MWU
190	
NEXT SPEC	

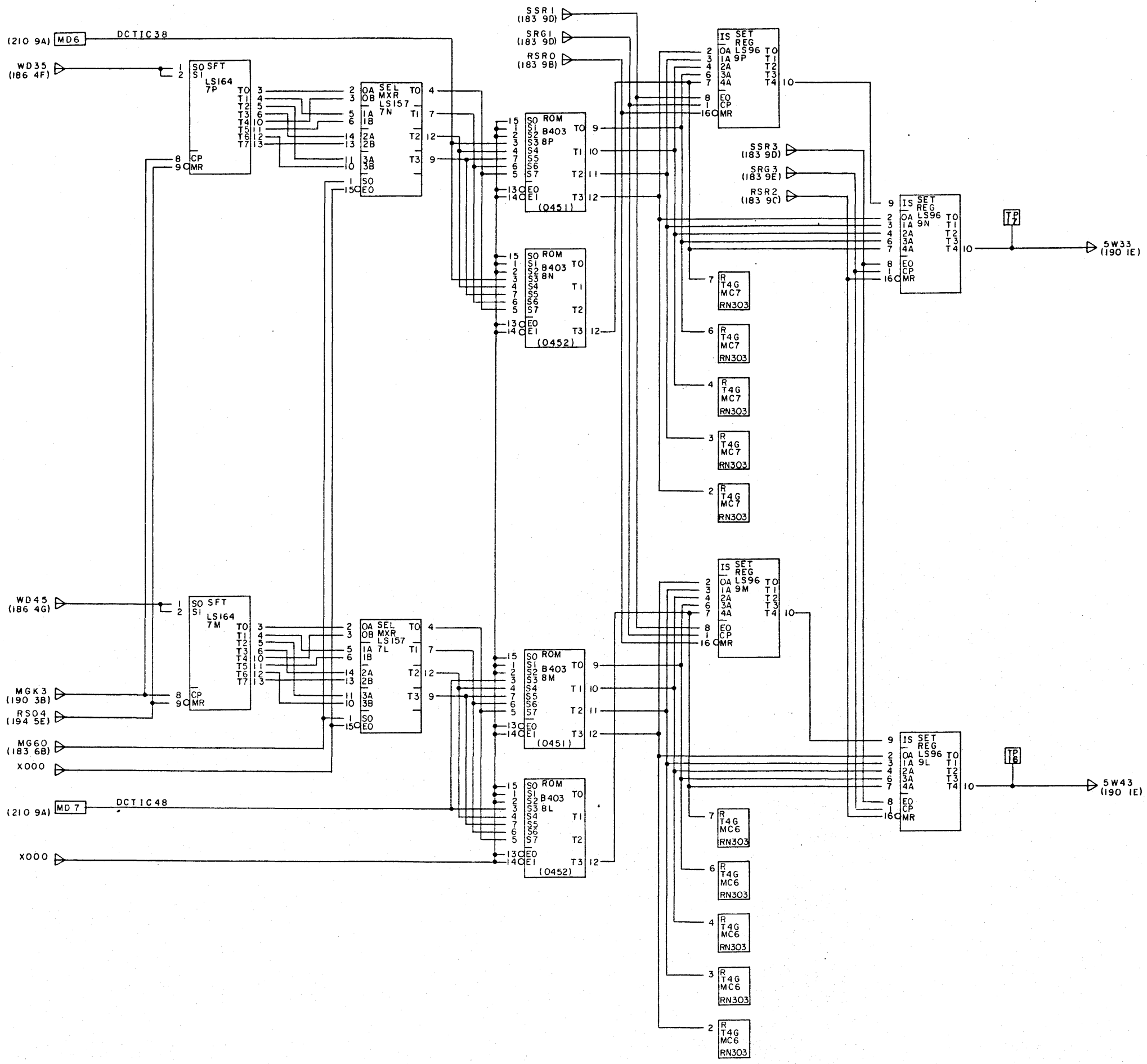
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	

MTA16X FORMATTER
GCR CONTROL
IN WRITE
CIRCUIT DIAGRAM
10/15

134-110229-004-0

NEC SH 10/

134-110229-004-0

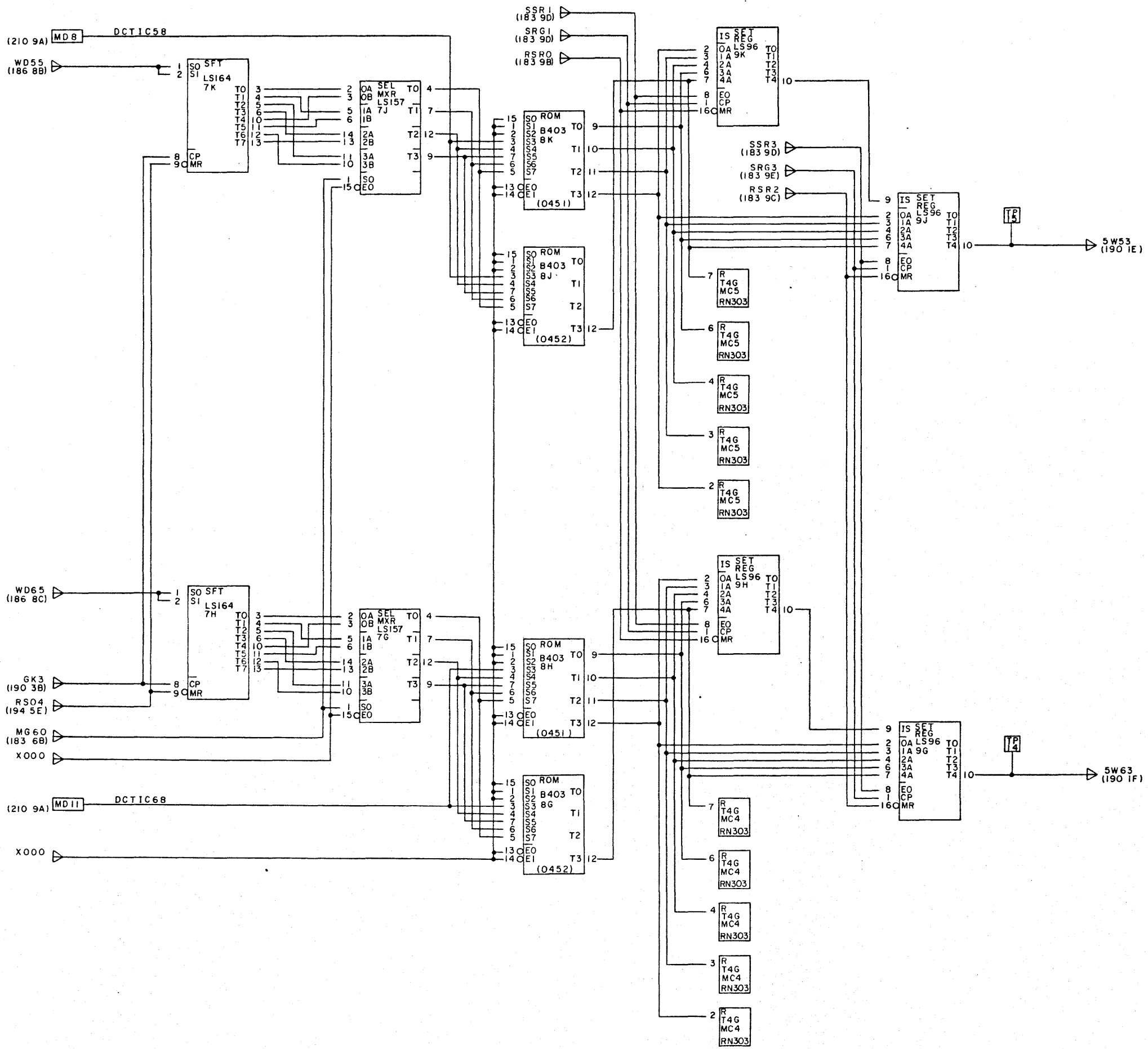


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G C W		
PKG LOCATION			
PKG NAME	G9JAT,G9MWU		
191			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTA16X FORMATTER GCR CONTROL IN WRITE CIRCUIT DIAGRAM 11/15			
134-110229-004-0			
NEC			SHT 11/

装置名

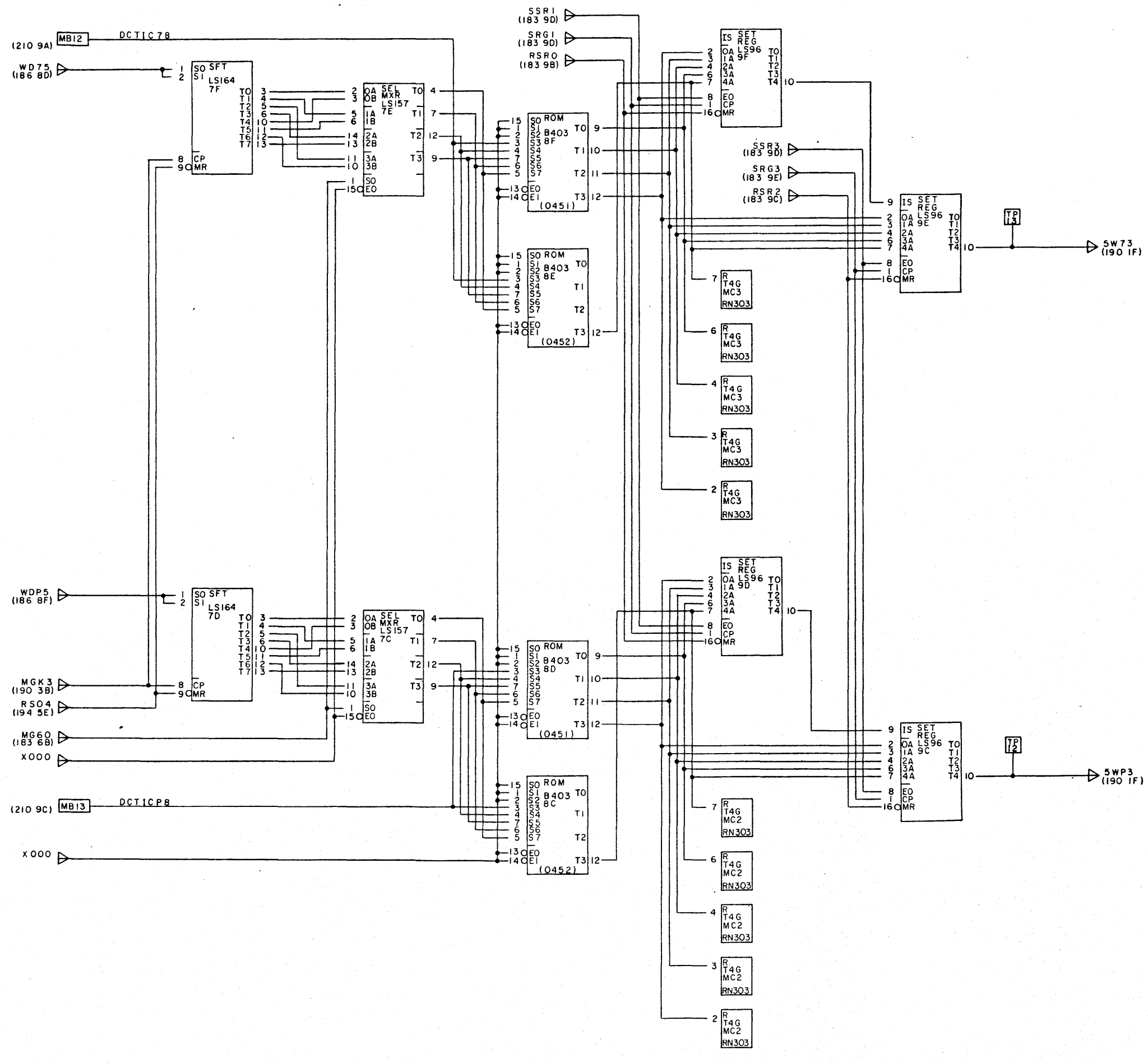
134-110229-004



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G C W		
PKG LOCATION			
PKG NAME	G9JAT,G9MWU		
192			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽		今
	賀		村
MTA16X FORMATTER GCR CONTROL IN WRITE CIRCUIT DIAGRAM 12/15			
134-110229-004			
NEC			SHT 12/

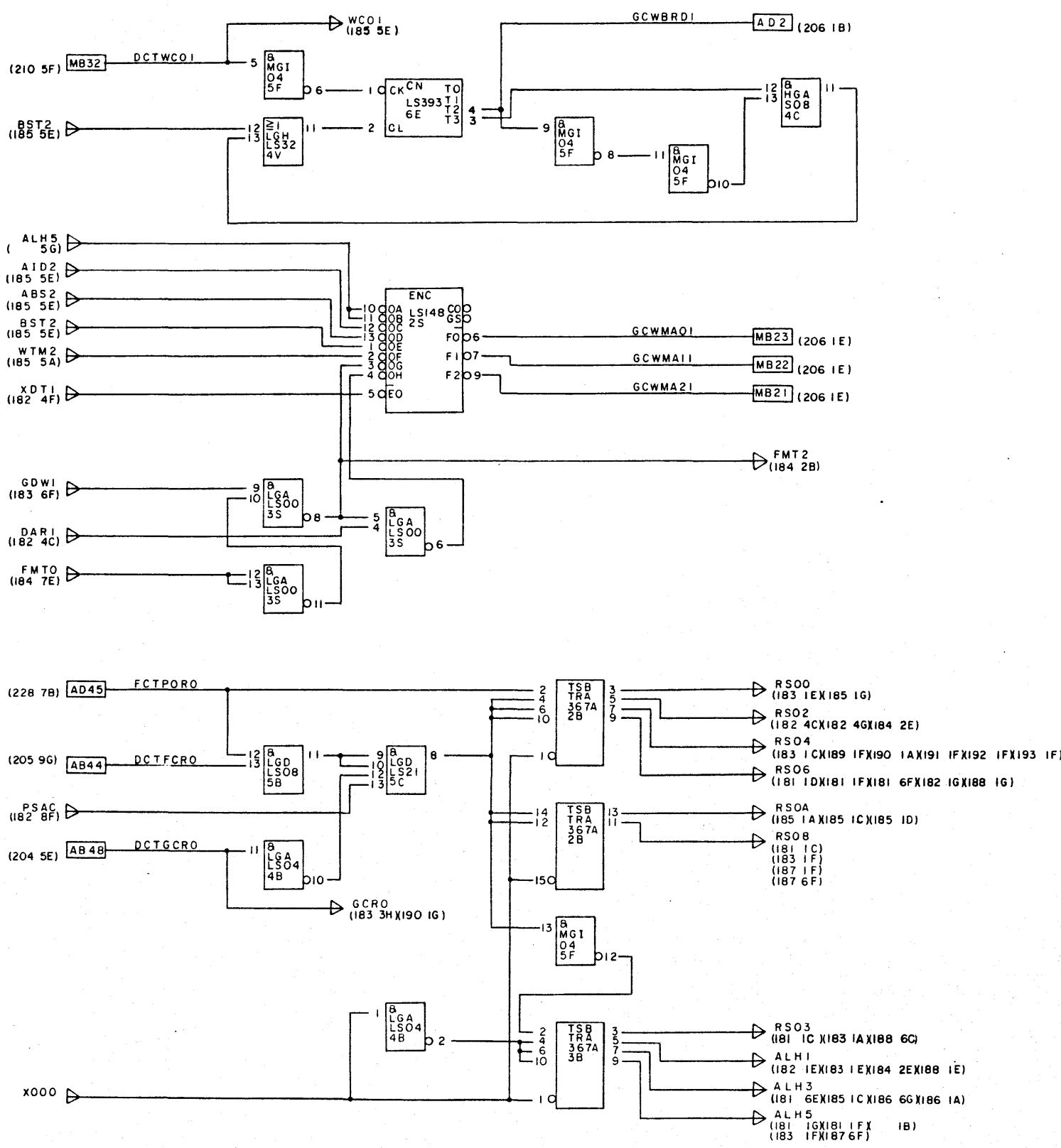
134-110229-004-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G C W		
PKG LOCATION			
PKG NAME	G9JAT, G9MWU		
193			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
MTA16X FORMATTER GCR CONTROL IN WRITE CIRCUIT DIAGRAM 13/15			
134-110229-004-0			
NEC			SHT 13/

134-110229-004-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	G C W
PKG LOCATION	
PKG NAME	G9JAT,G9MWU
194	
NEXT SPEC	

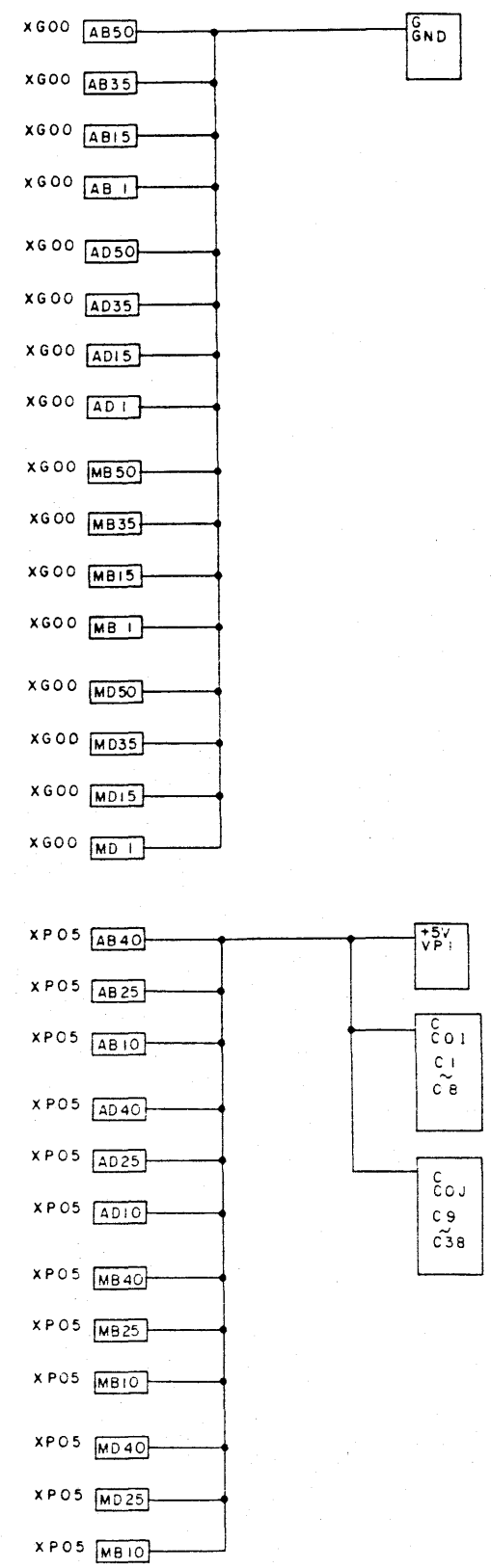
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	

MTA16X FORMATTER
GCR CONTROL
IN WRITE
CIRCUIT DIAGRAM
14/

134-110229-004-0
NEC SHT 14/

装置名

134-110229-004



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	G C W
PKG LOCATION	
PKG NAME	G9JAT,G9MWU
195	
NEXT SPEC	

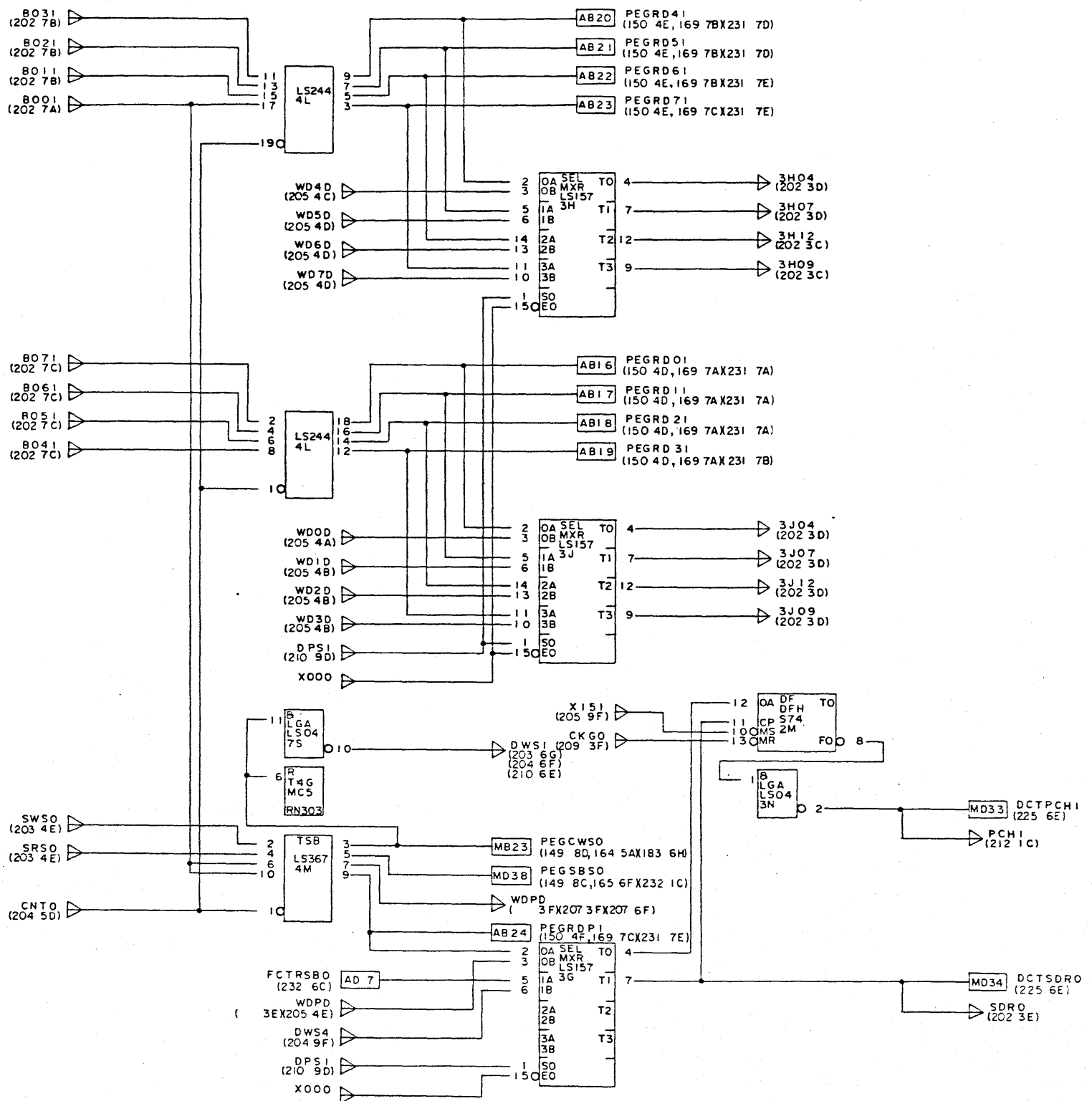
DRAFT	ENG	CHK	APP	ISSUE
	羽 賀		今 村	

MTA16X FORMATTER
GCR CONTROL
IN WRITE
CIRCUIT DIAGRAM
15/15

134-110229-004

NEC SHT 15/15

134-110229-015-0



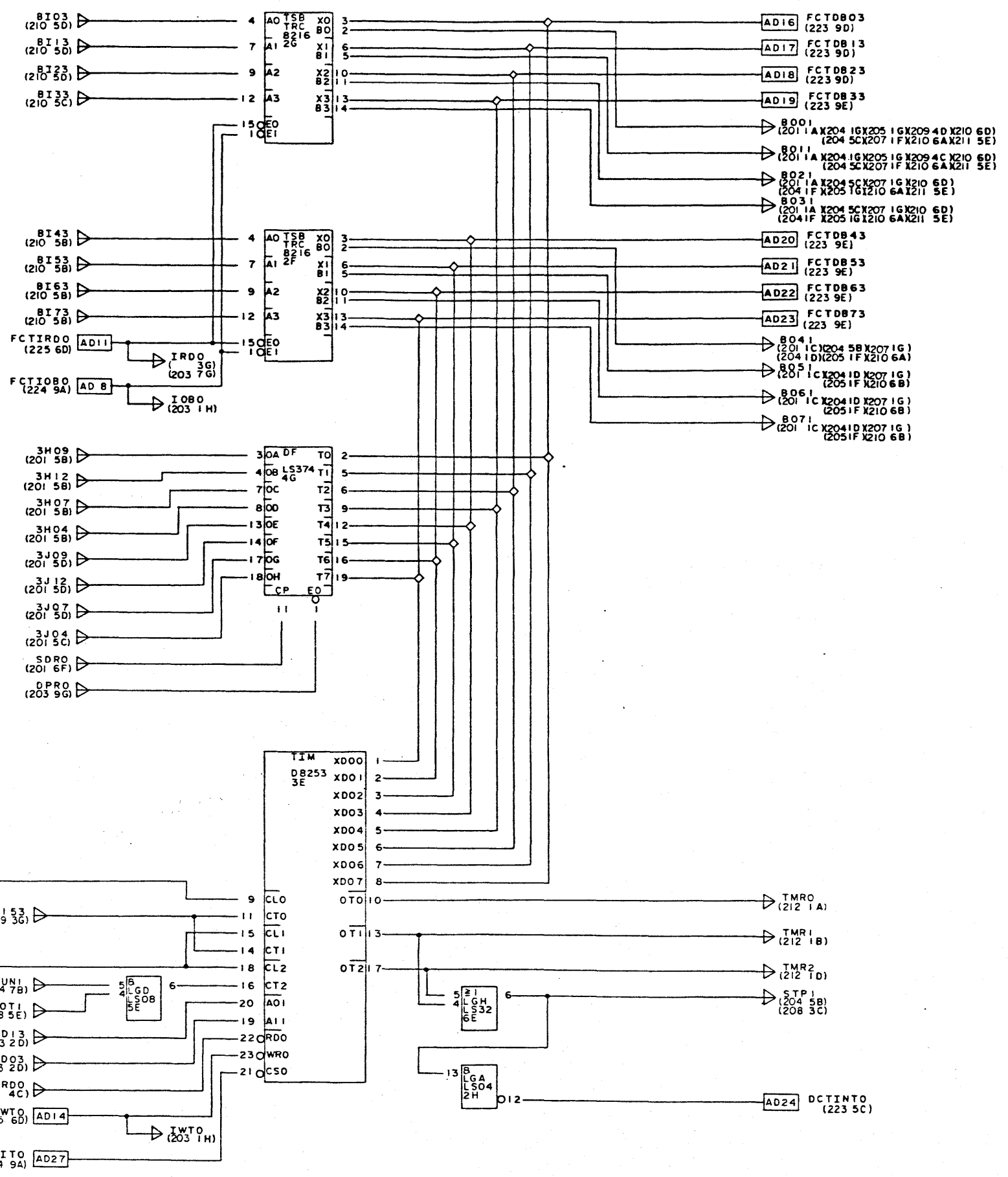
REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.2	
2	0	1983.2 SC-41431 大橋	大橋

DWG ABBR	D C T			
PKG LOCATION				
PKG NAME	G9QWT, G9QWX			
201				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
	賀		村	

MTA16X FORMATTER
DEVICE CONTROL
CIRCUIT DIAGRAM
1/14

134-110229-015-0
NEC SHT 1/14

134-110229-015-0



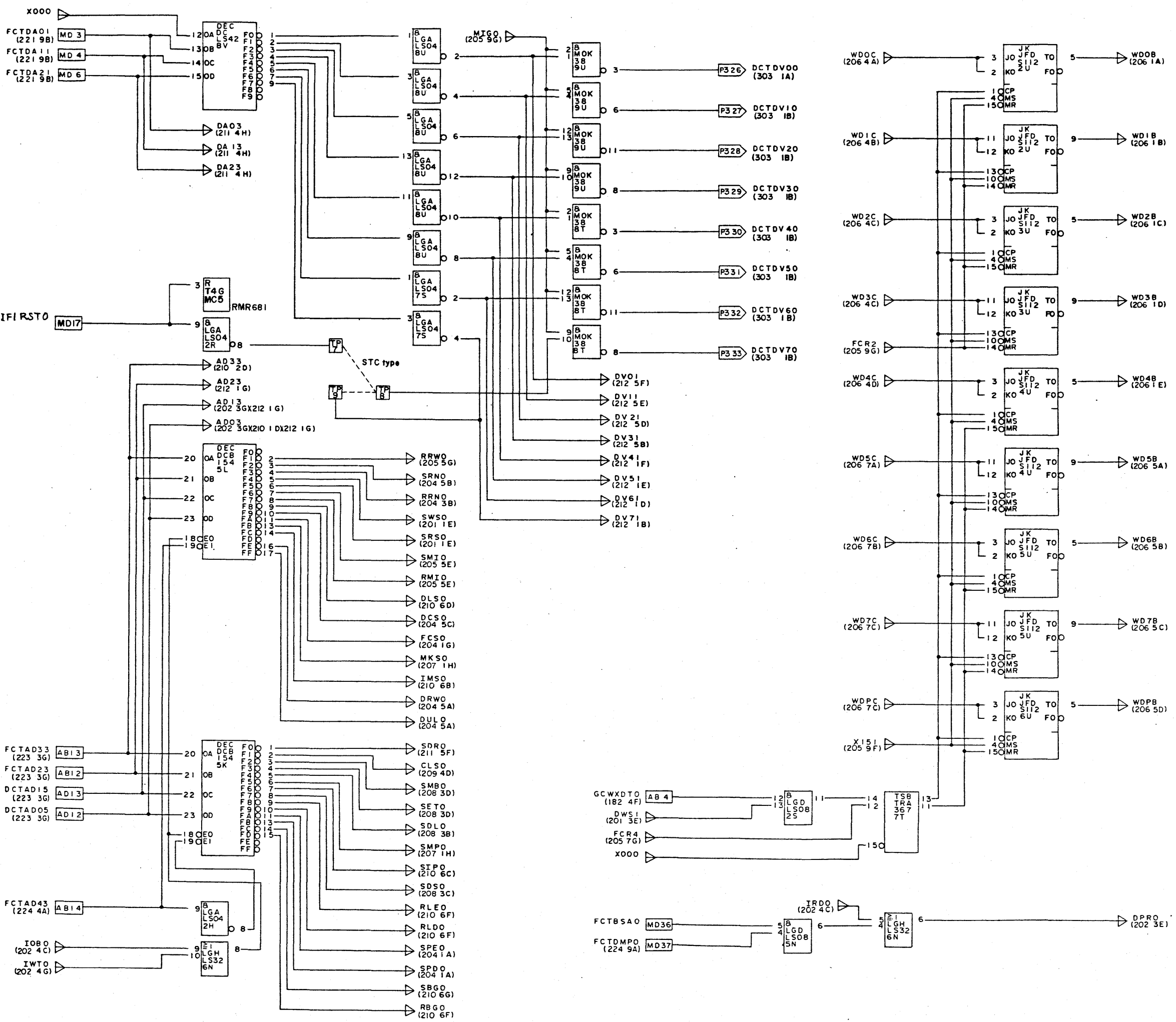
REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.2	

DWG ABBR	DCT			
PKG LOCATION				
PKG NAME	G9QWT, G9QWX			
202				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
 DEVICE CONTROL
 CIRCUIT DIAGRAM
 2/14
 134-110229-015-0
 NEC SHT 2/

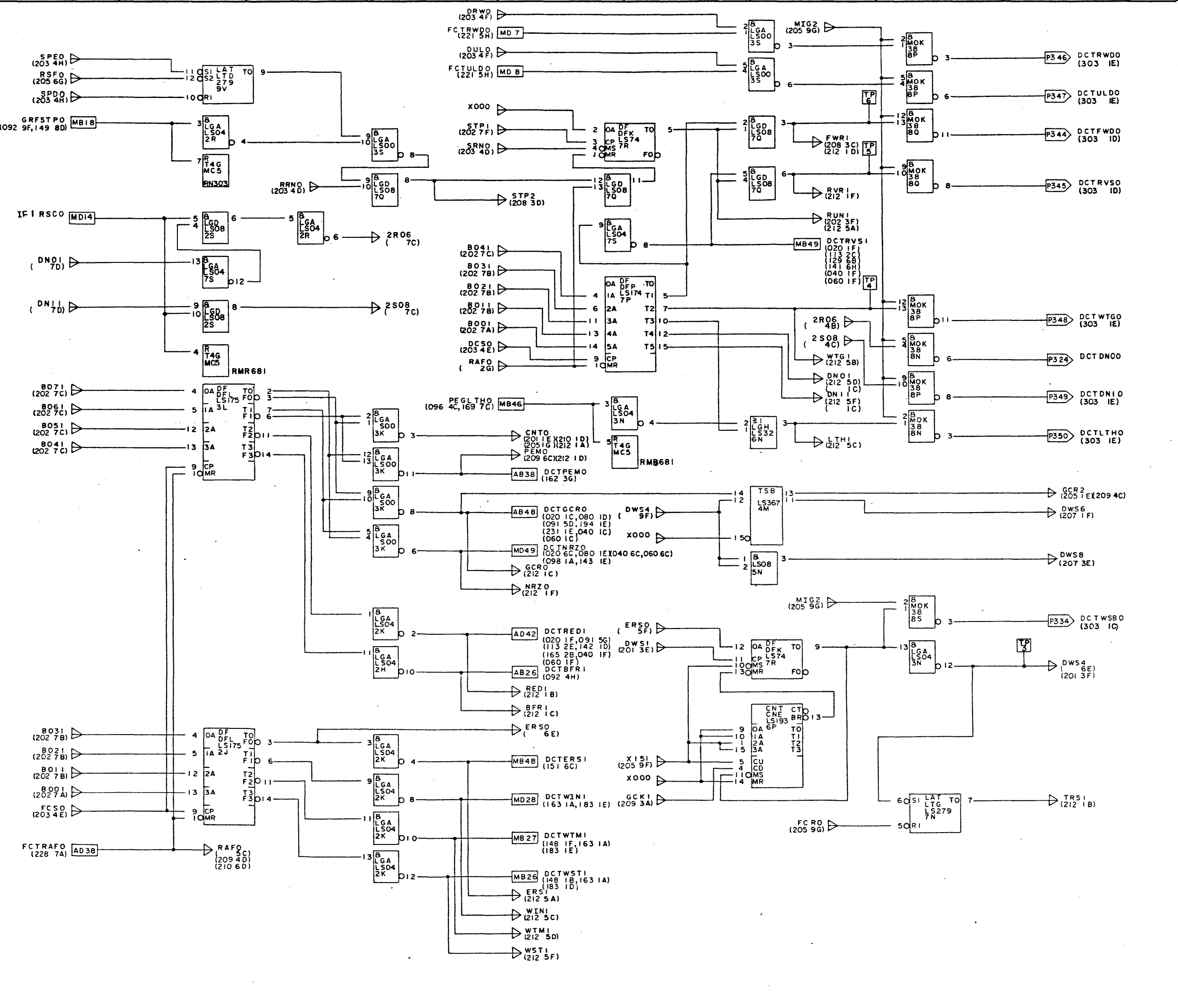
134-110229-015-0

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REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.2	
DWG ABBR		DCT	
PKG LOCATION			
PKG NAME		G9QWT, G9QWX	
NEXT SPEC		203	
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER DEVICE CONTROL CIRCUIT DIAGRAM 3/14			
134-110229-015-0			
NEC			SHT 3/

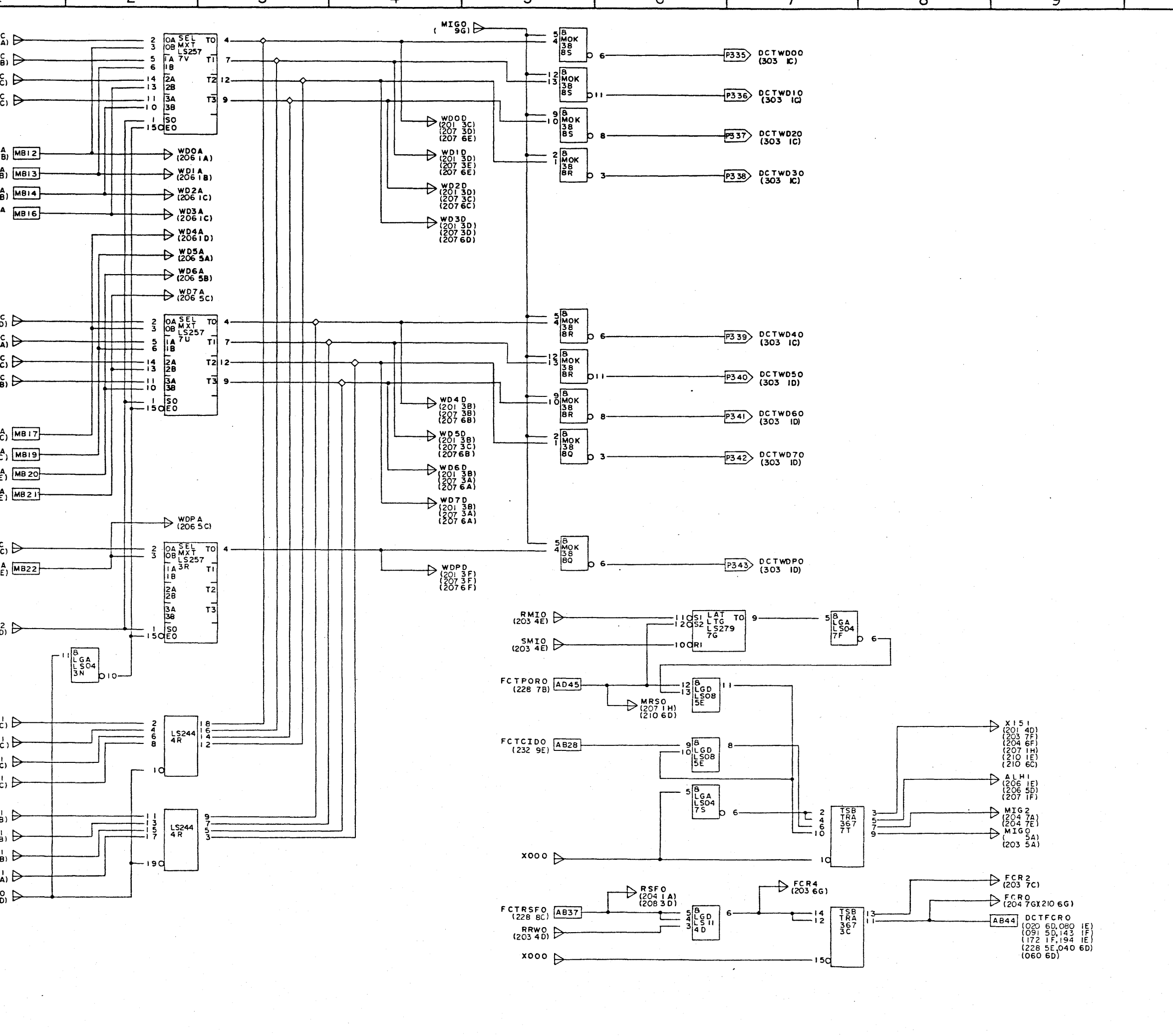
134-110229-015-0



REV	COMP	DESCRIPTION (SC)	APP
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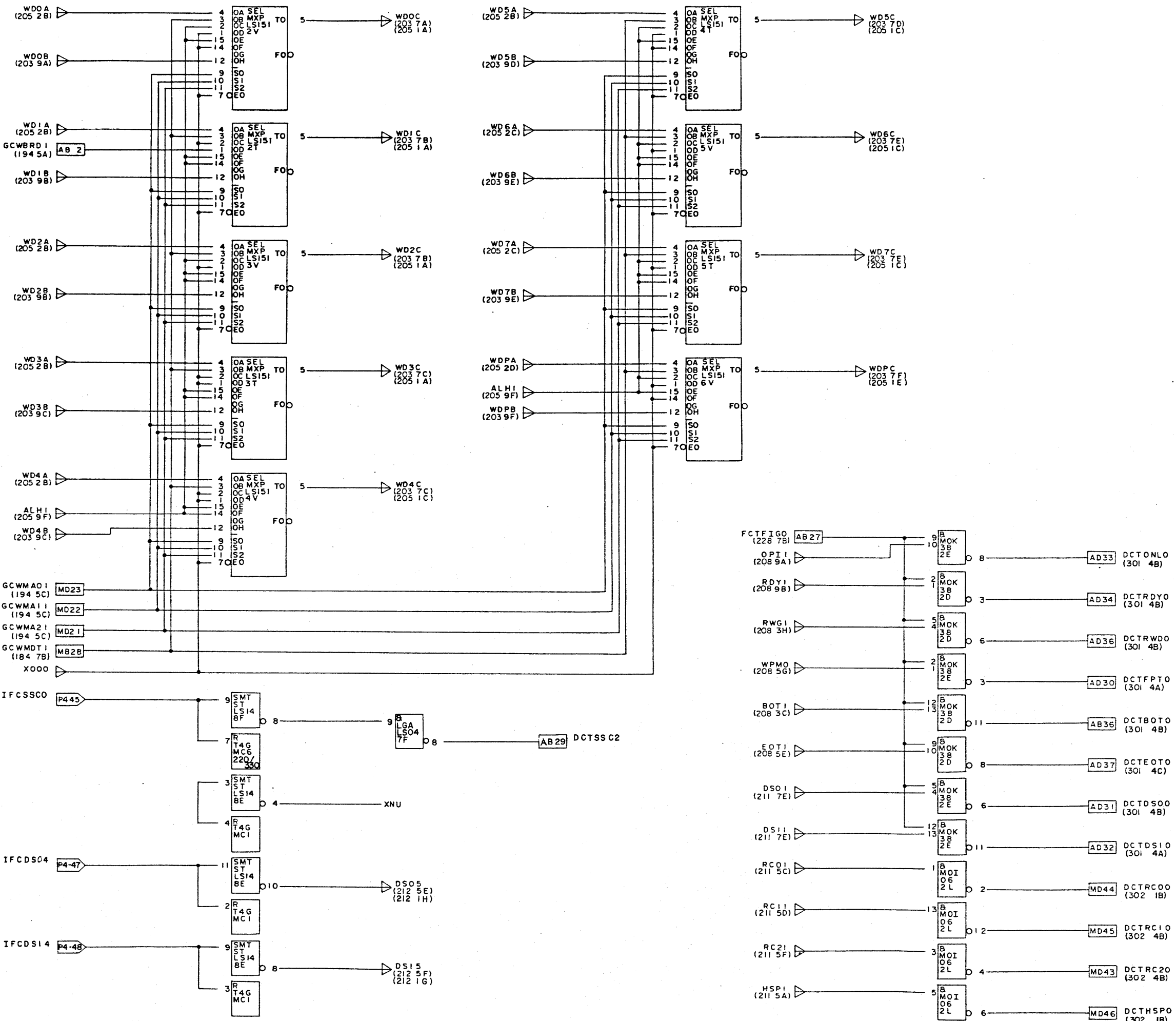
DWG ABBR	DCT			
PKG LOCATION				
PKG NAME	G9QWT, G9QWX			
204				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER DEVICE CONTROL CIRCUIT DIAGRAM 4/14				
134-110229-015-0				
NEC				SHT 4/

134-110229-015-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.2	
DWG ABBR		D C T	
PKG LOCATION			
PKG NAME		G9QWT,G9QWX	
205			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER DEVICE CONTROL CIRCUIT DIAGRAM 5/14			
134-110229-015-0			
NEC		SHT 5/	

134-110229-015-0

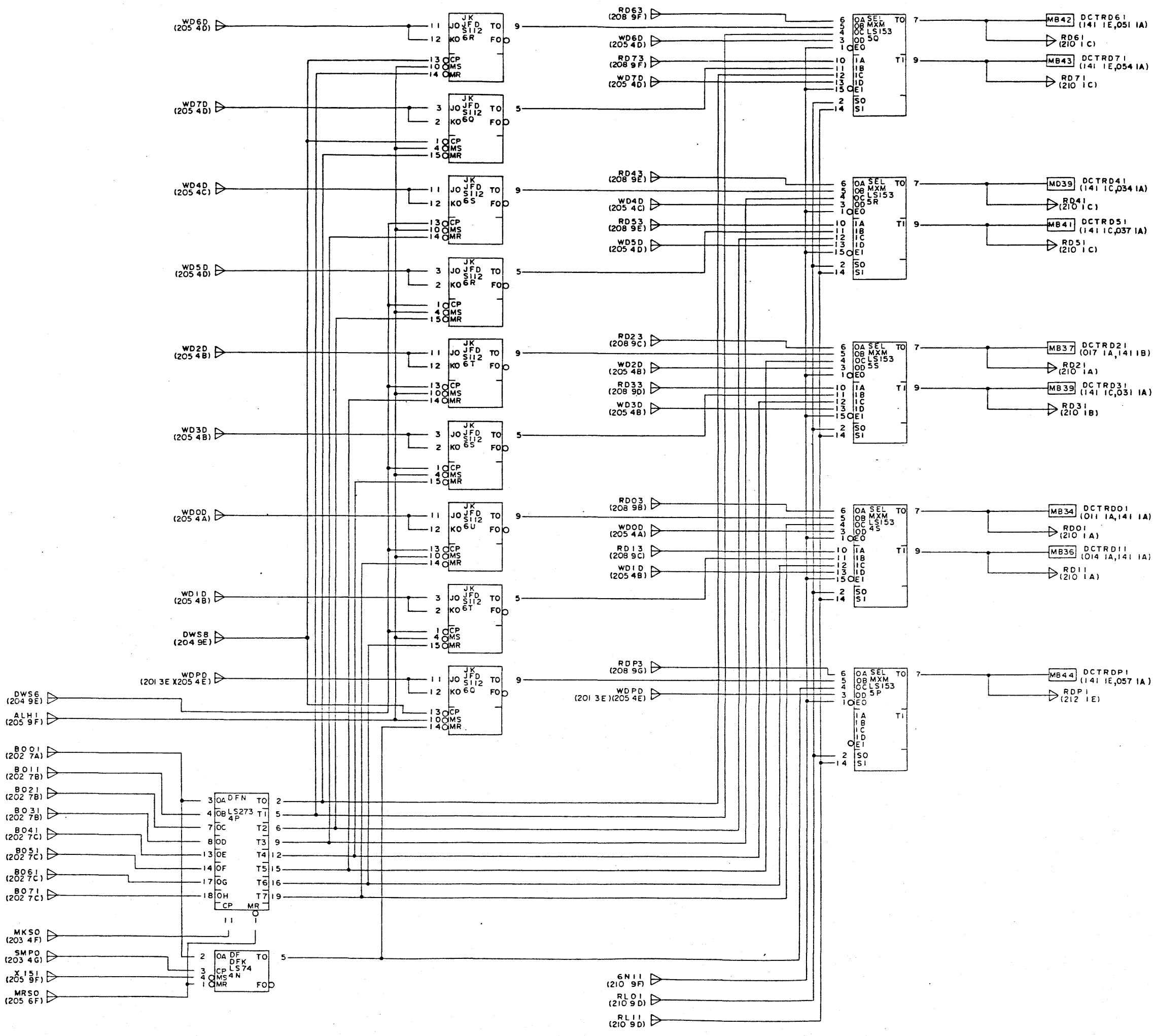


REV	COMP	DESCRIPTION(SC)	APP																												
1	0	1982.2																													
<table border="1"> <tr> <td>DWG ABBR</td> <td colspan="3">DCT</td> </tr> <tr> <td>PKG LOCATION</td> <td colspan="3"></td> </tr> <tr> <td>PKG NAME</td> <td colspan="3">G9QWT,G9QWX</td> </tr> <tr> <td colspan="4" style="text-align: center; font-size: 2em;">206</td> </tr> <tr> <td>NEXT SPEC</td> <td colspan="3"></td> </tr> <tr> <td>DRAFT</td> <td>ENG</td> <td>CHK</td> <td>APP</td> </tr> <tr> <td></td> <td>山口</td> <td></td> <td>今村</td> </tr> </table>				DWG ABBR	DCT			PKG LOCATION				PKG NAME	G9QWT,G9QWX			206				NEXT SPEC				DRAFT	ENG	CHK	APP		山口		今村
DWG ABBR	DCT																														
PKG LOCATION																															
PKG NAME	G9QWT,G9QWX																														
206																															
NEXT SPEC																															
DRAFT	ENG	CHK	APP																												
	山口		今村																												
<p>MTA16X FORMATTER DEVICE CONTROL CIRCUIT DIAGRAM</p> <p style="text-align: right; font-size: 1.5em;">6/14</p>																															
<p>134-110229-015-0</p>																															
<p>NEC</p>			<p>SHT 6/</p>																												

134-110229-015-0

1 2 3 4 5 6 7 8 9 X Y

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2	



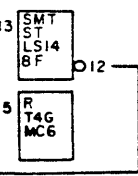
DWG ABBR	DCT			
PKG LOCATION				
PKG NAME	G9QWT,G9QWX			
207				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
 DEVICE CONTROL
 CIRCUIT DIAGRAM
 7/14
 134-110229-015-0
 NEC SHT 7/

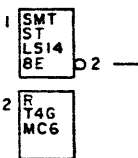
装置名

134-110229-015-0

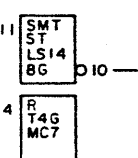
IFCDLEO (303 6D) P443



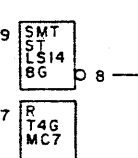
IFCDOSO (303 6D) P440



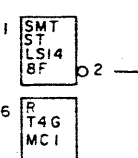
IFCBOTO (303 6C) P438



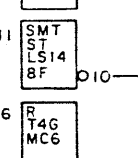
IFCEOTO (303 6C) P439



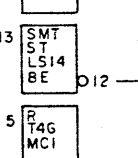
IFCALMO (303 6E) P446



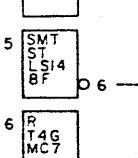
IFCLCWO (303 6D) P444



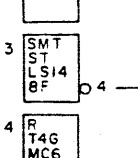
IFCLDDO (303 6E) P450



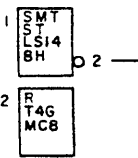
IFCWPMO (303 6D) P442



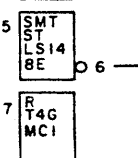
IFCRWGO (303 6D) P441



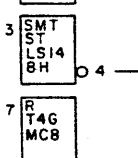
IFCOPIO (303 6A) P426



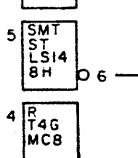
IFCRDYO (303 6E) P449



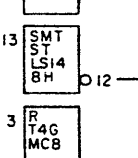
IFCRDOO (303 6B) P428



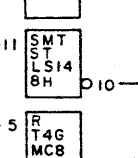
IFCRDIO (303 6B) P429



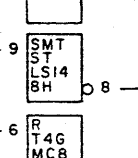
IFCRD2O (303 6B) P430



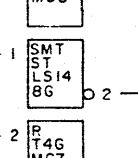
IFCRD3O (303 6B) P431



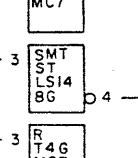
IFCRD4O (303 6B) P432



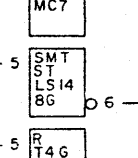
IFCRD5O (303 6B) P433



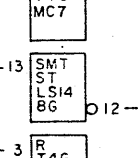
IFCRD6O (303 6C) P434



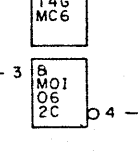
IFCRD7O (303 6C) P435



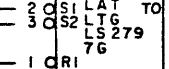
IFCRDPO (303 6C) P436



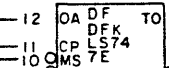
MBTI (202 3G) (206 7F) (212 5D)



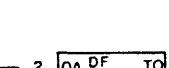
SDLO (203 4G)



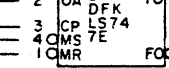
X000 (202 7F)



STP1 (202 7F)



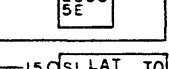
SDSO (203 4G)



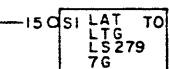
RSFO (205 6G)



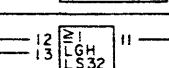
STP2 (204 5B)



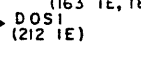
SETO (203 4G)



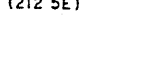
EOTI (202 3G) (206 7F) (212 1D)



AB43 DCTDOS1 (112 1E, 143 1E) (163 1E, 183 1E) (225 6F)



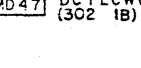
MD27 DCTALMI (226 6E)



MD42 DCTALMO (302 4B)



MD47 DCTLCWO (302 1B)



MD48 DCTLDDO (302 1A)

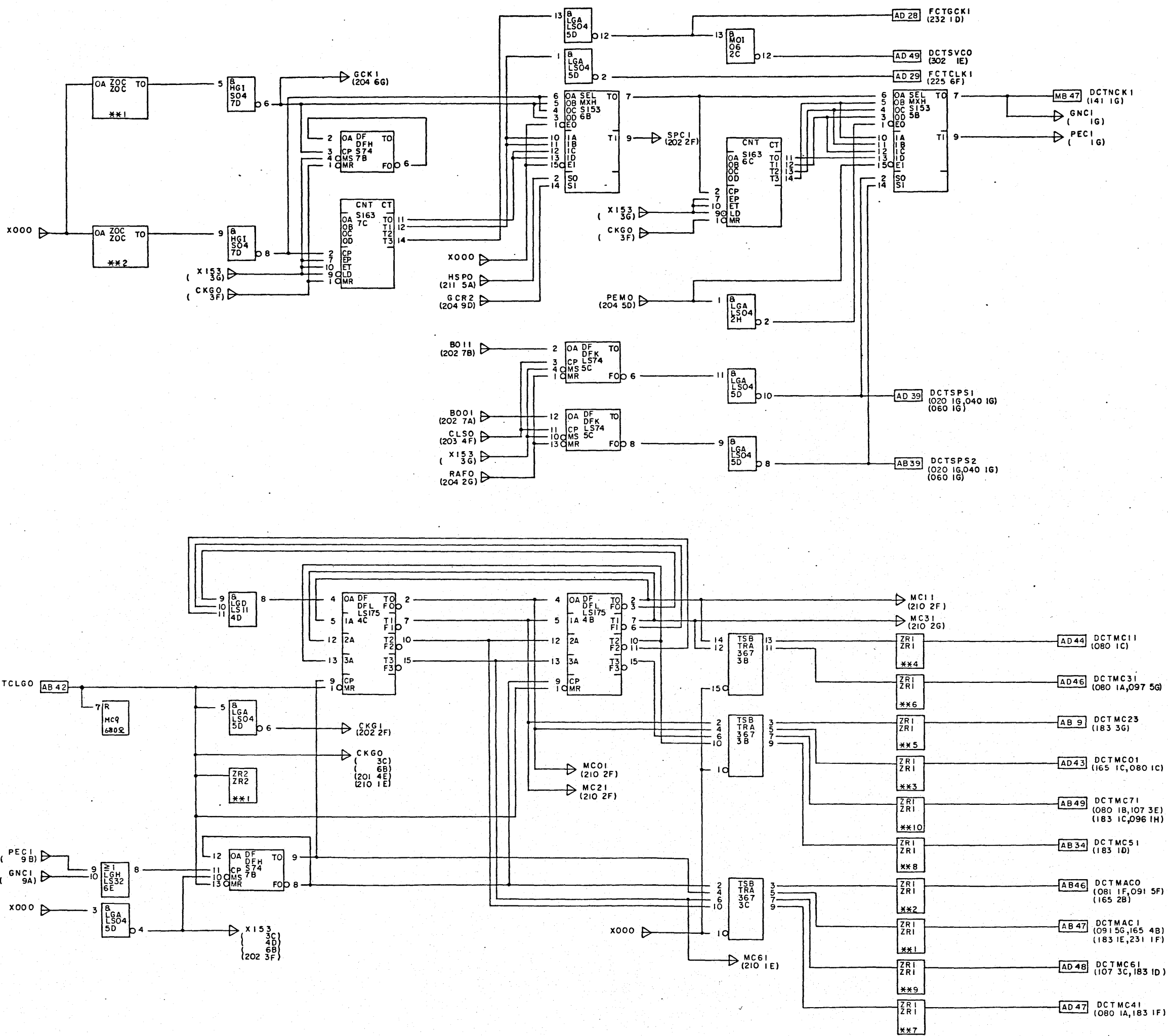


MD41 DCTMBTO (302 4C)



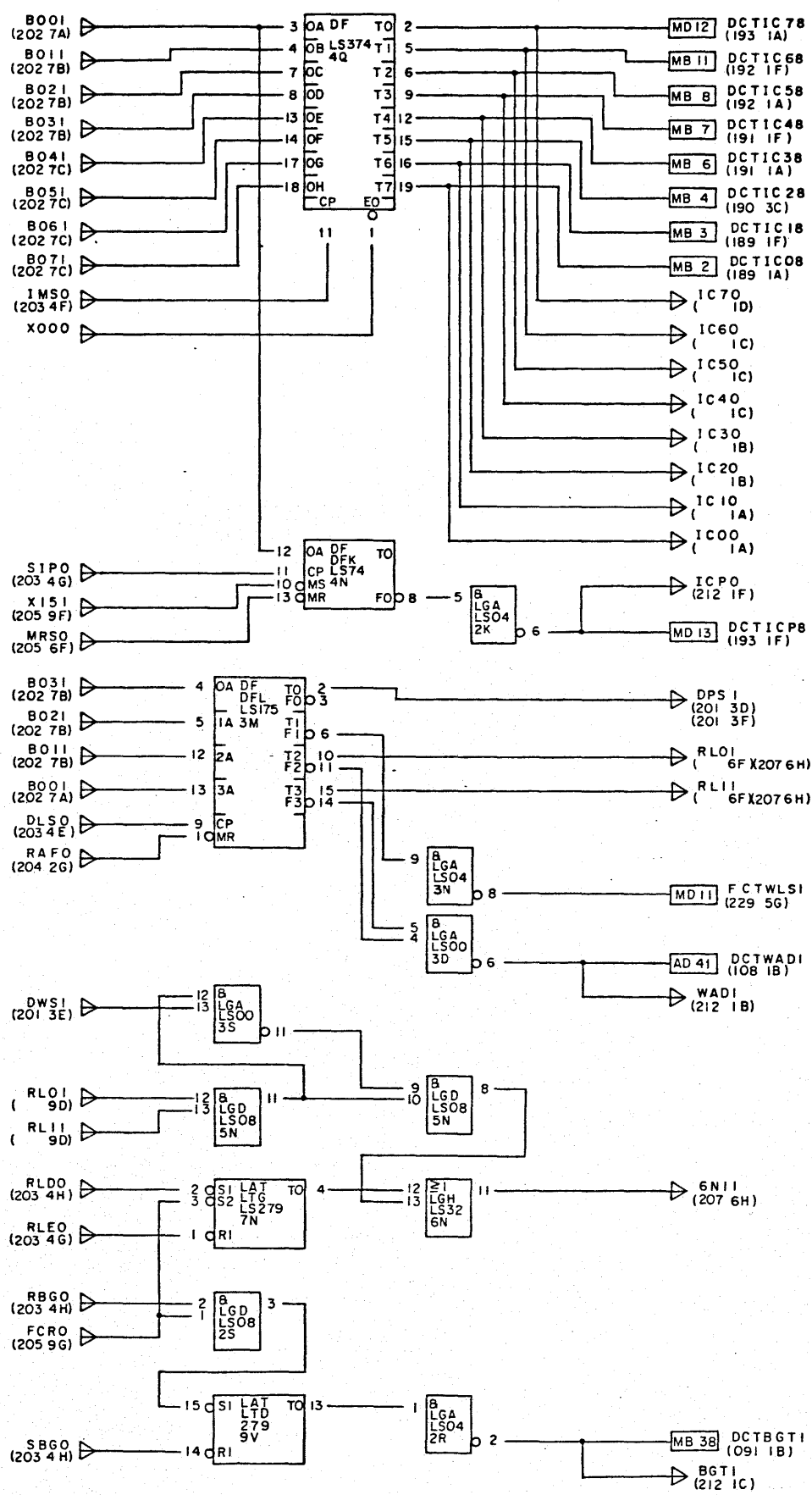
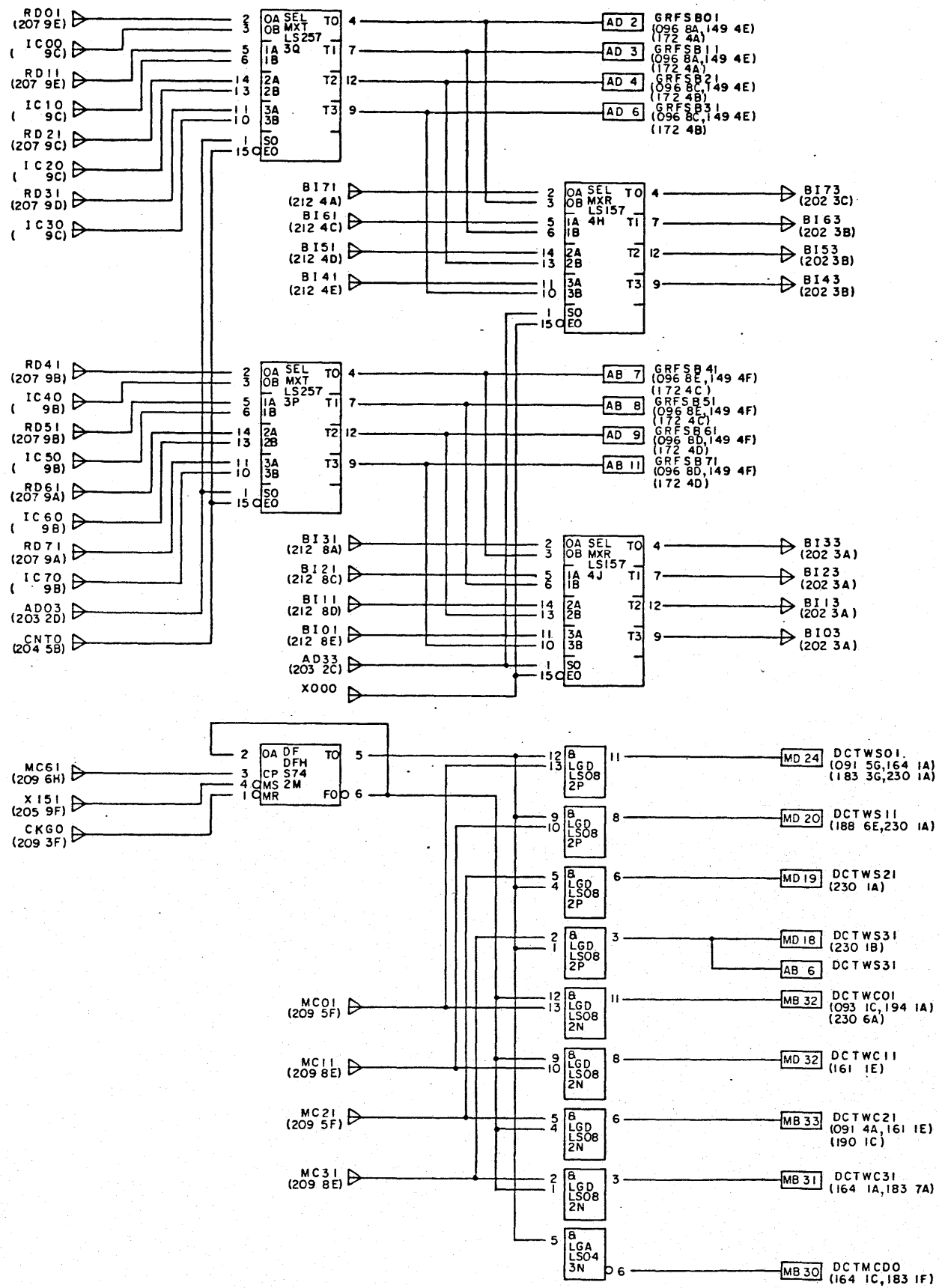
REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2	
DWG ABBR		D C T	
PKG LOCATION			
PKG NAME		G9QWT,G9QWX	
208			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER DEVICE CONTROL CIRCUIT DIAGRAM 8/14			
134-110229-015-0			
NEC			SHT 8/

134-110229-015-0



装置名

134-110229-015-0

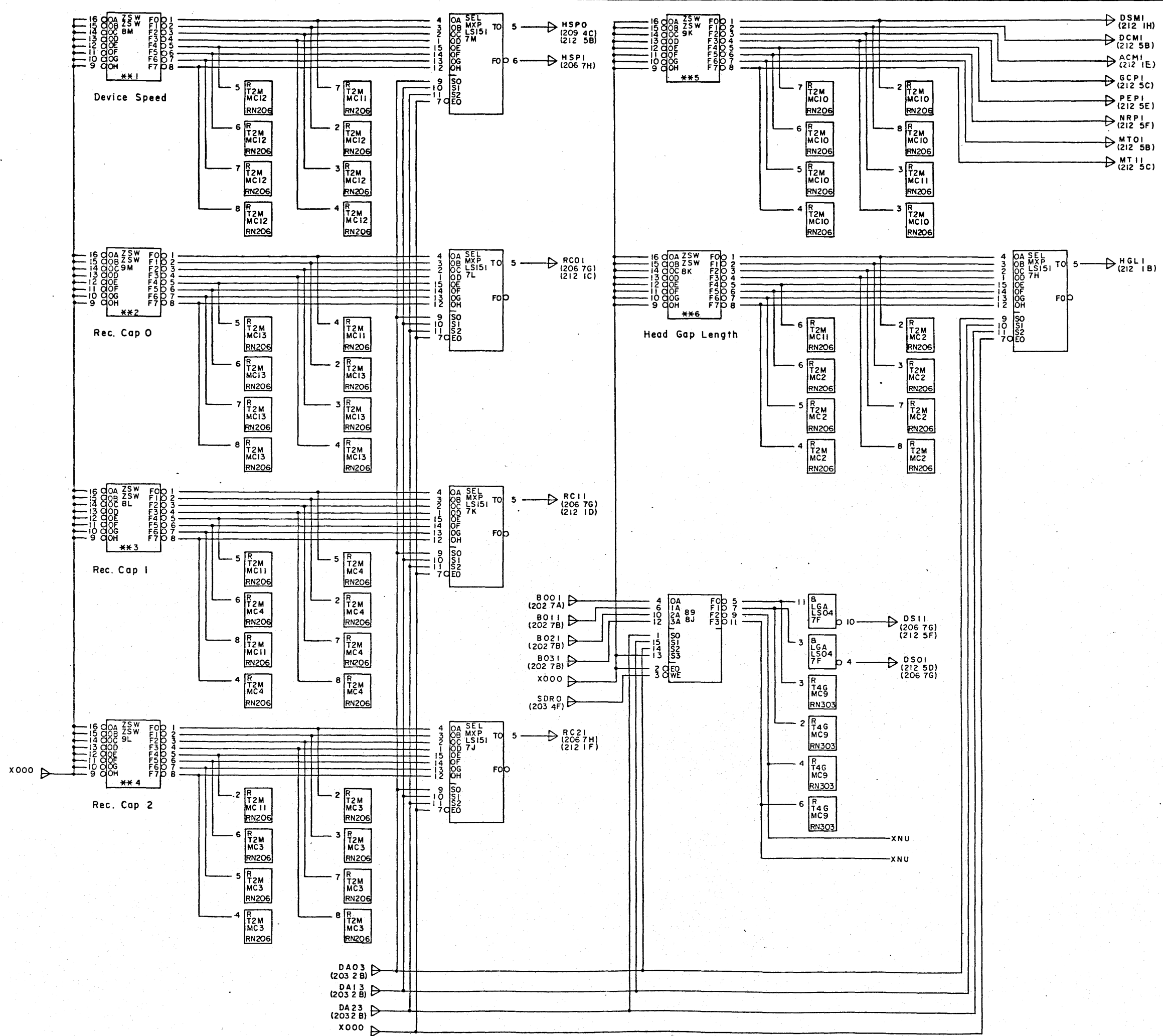


REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.2	

DWG ABBR	DCT			
PKG LOCATION				
PKG NAME	G9QWT, G9QWX			
210				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
 DEVICE CONTROL
 CIRCUIT DIAGRAM
 10/14
 134-110229-015-0
 NEC SHT 10/

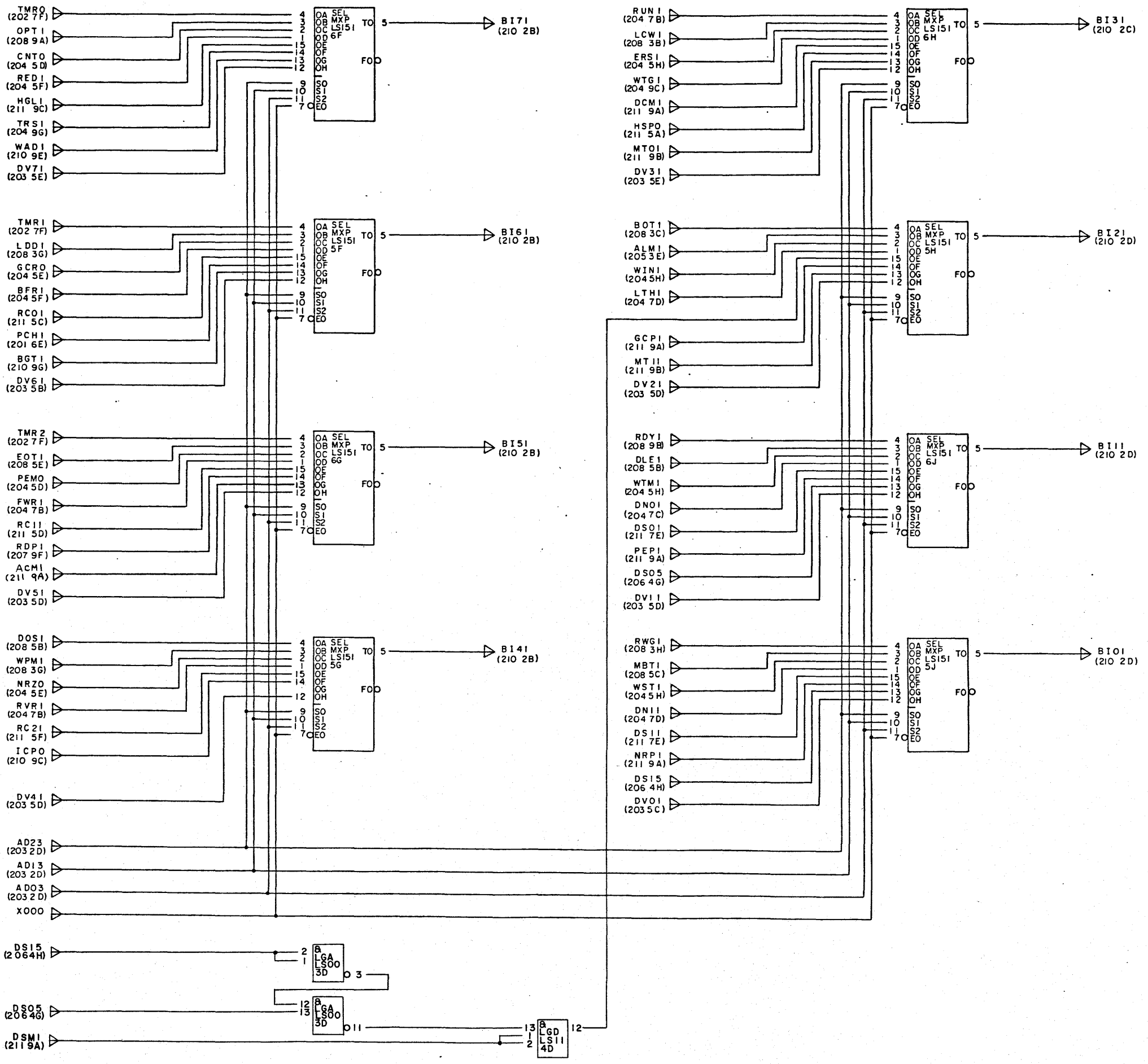
134-110229-015-0



REV	COMP	DESCRIPTION(SC)	APP																												
1	0	1982.2																													
<table border="1"> <tr> <td>DWG ABBR</td> <td colspan="3">D C T</td> </tr> <tr> <td>PKG LOCATION</td> <td colspan="3"></td> </tr> <tr> <td>PKG NAME</td> <td colspan="3">G9QWT,G9QWX</td> </tr> <tr> <td colspan="4" style="text-align: center;">211</td> </tr> <tr> <td>NEXT SPEC</td> <td colspan="3"></td> </tr> <tr> <td>DRAFT</td> <td>ENG</td> <td>CHK</td> <td>APP</td> </tr> <tr> <td></td> <td>山口</td> <td></td> <td>今村</td> </tr> </table>				DWG ABBR	D C T			PKG LOCATION				PKG NAME	G9QWT,G9QWX			211				NEXT SPEC				DRAFT	ENG	CHK	APP		山口		今村
DWG ABBR	D C T																														
PKG LOCATION																															
PKG NAME	G9QWT,G9QWX																														
211																															
NEXT SPEC																															
DRAFT	ENG	CHK	APP																												
	山口		今村																												
MTA16X FORMATTER DEVICE CONTROL CIRCUIT DIAGRAM 11/14																															
134-110229-015-0																															
NEC			SHT 11/																												

装置名

134-110229-015-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.2	

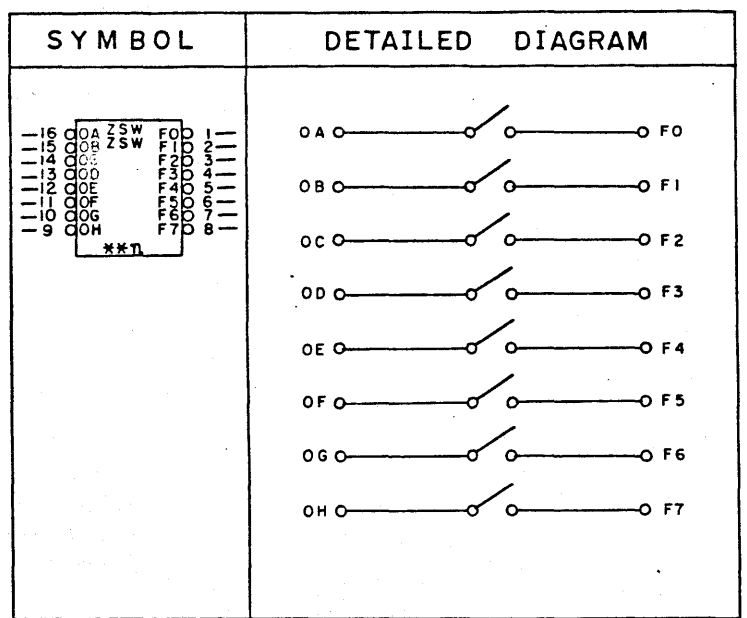
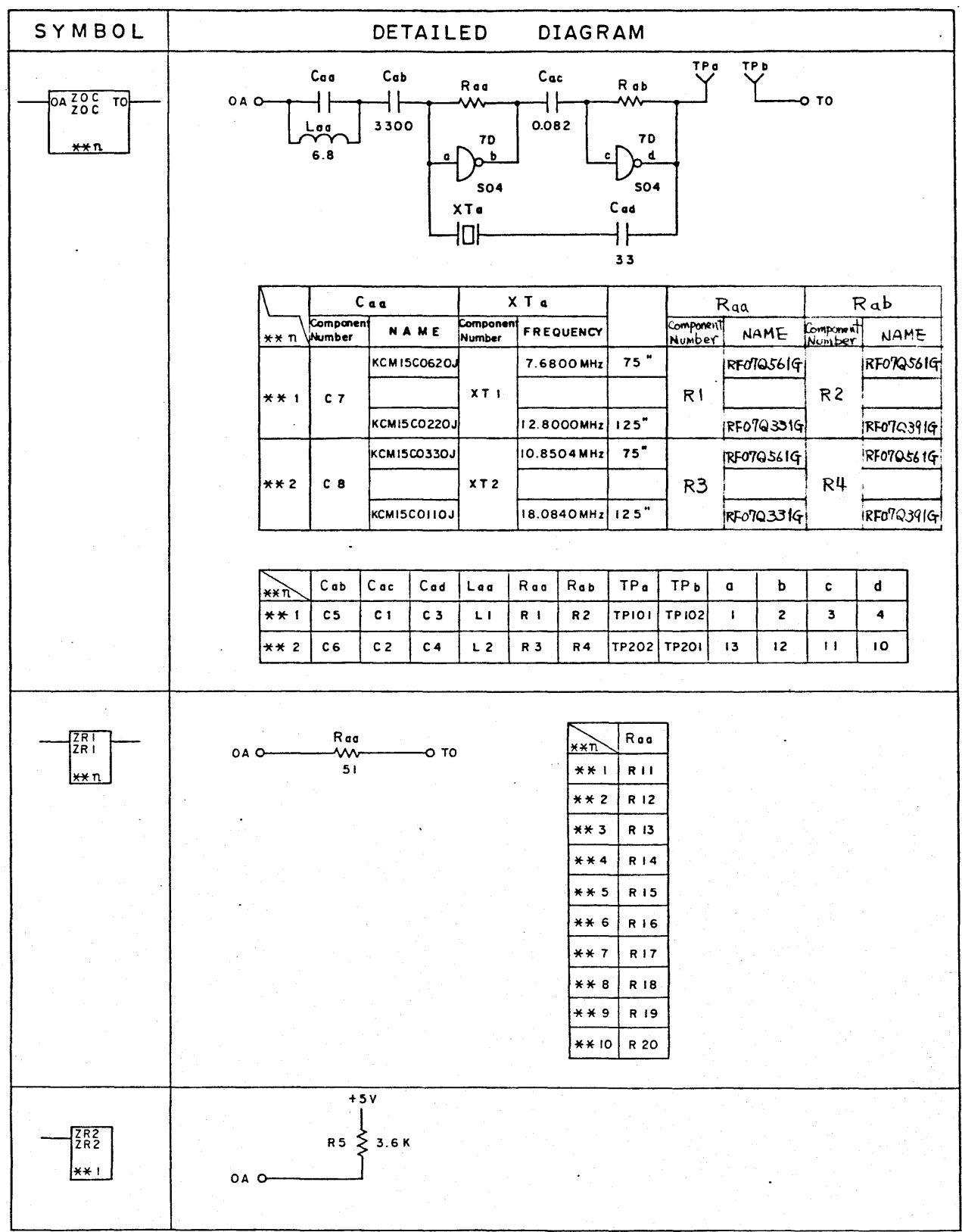
DWG ABBR	D C T		
PKG LOCATION			
PKG NAME	G9QWT,G9QWX		
212			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村

MTA16X FORMATTER
 DEVICE CONTROL
 CIRCUIT DIAGRAM
 12/14

134-110229-015-0

NEC SHT 12/

134-110229-015-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.2	

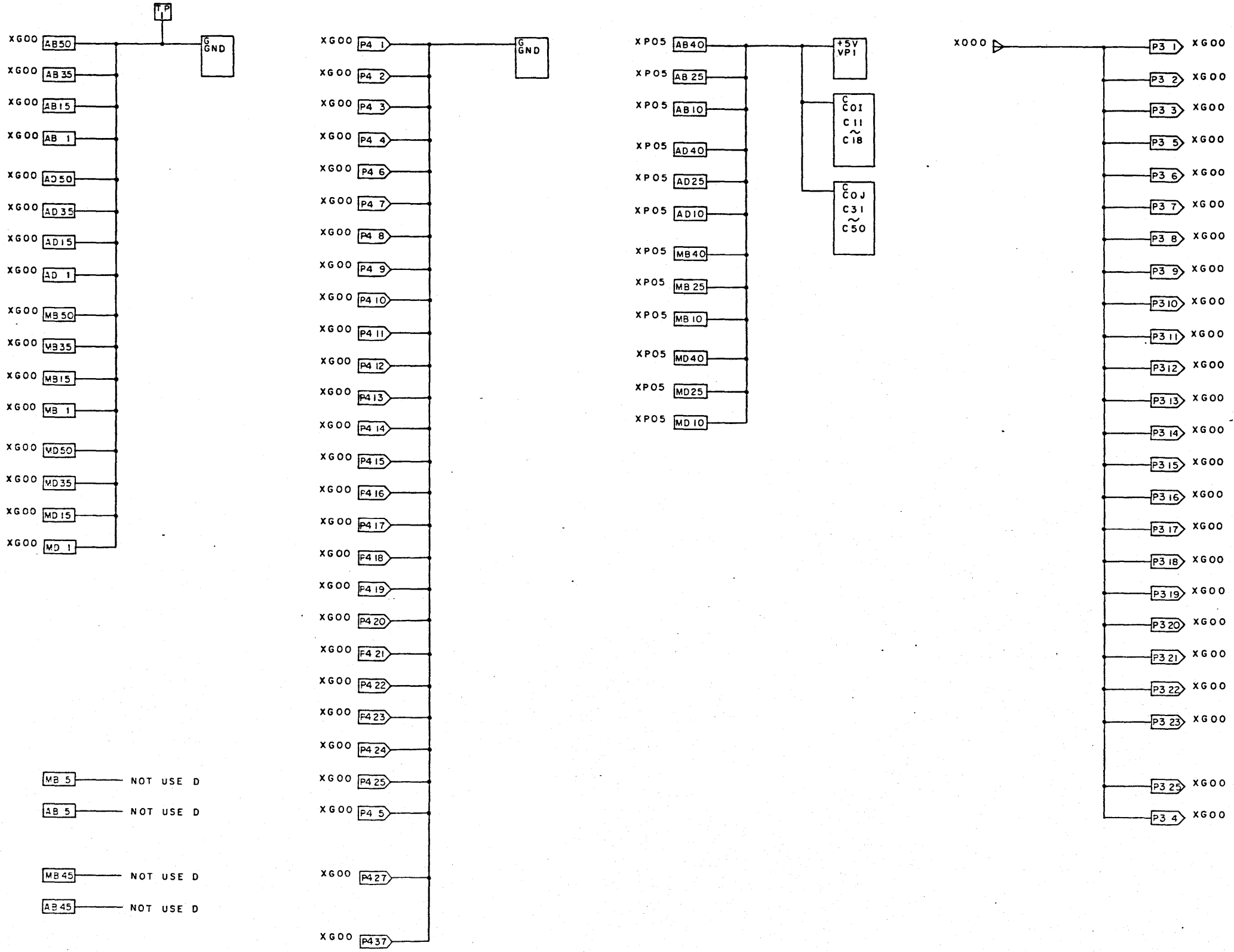
DWG ABBR	DCT			
PKG LOCATION				
PKG NAME	G9QWT, G9QWX			
213				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
 DEVICE CONTROL
 CIRCUIT DIAGRAM
 13/14

134-110229-015-0

NEC SHT 13/

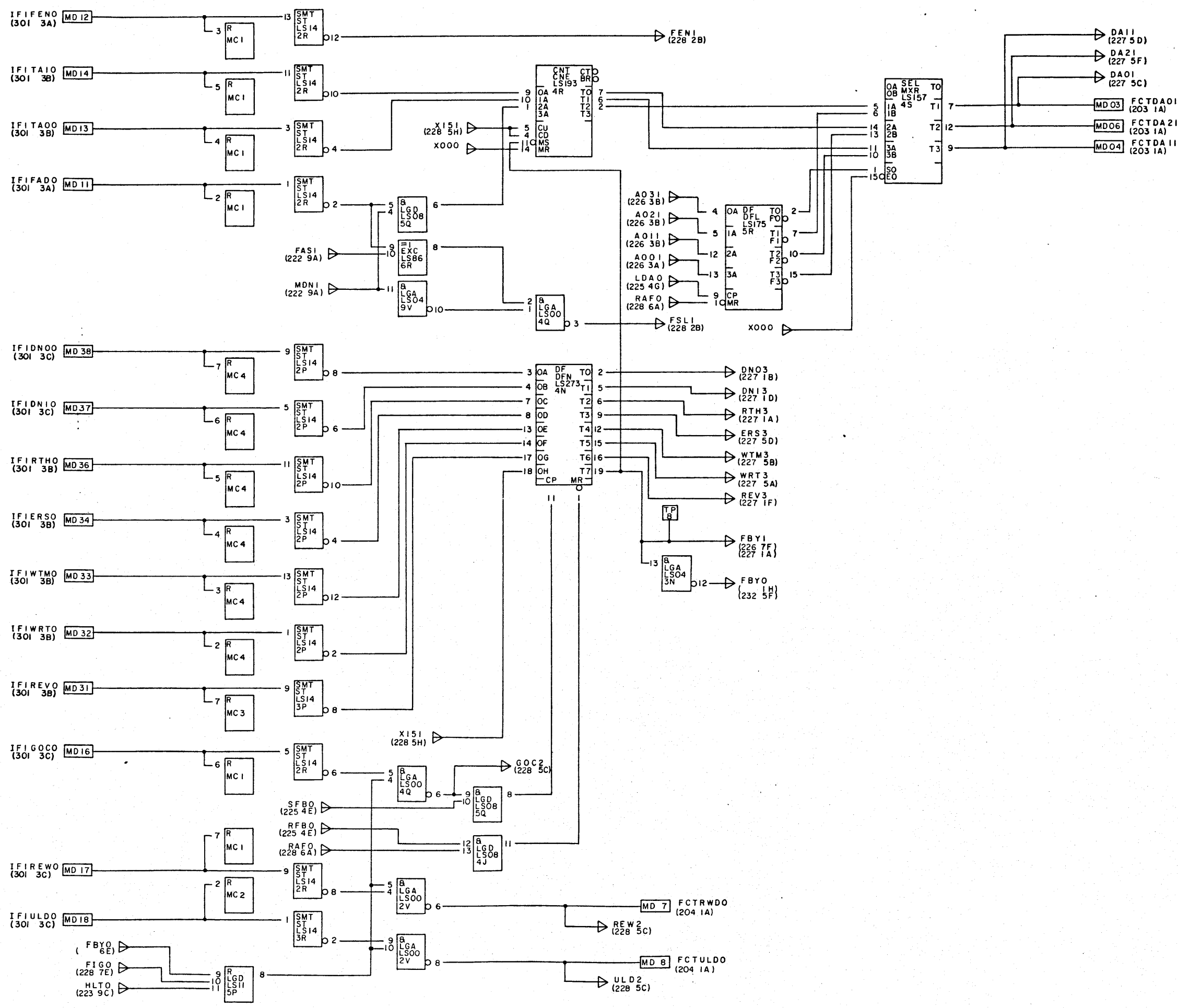
134-110229-015-0



MB 5 — NOT USE D
 AB 5 — NOT USE D
 MB 45 — NOT USE D
 AB 45 — NOT USE D

REV	COMP	DESCRIPTION (SC)	APP
1	o	1982.2	—
DWG ABBR		D C T	
PKG LOCATION			
PKG NAME		G9QWT,G9QWX	
214			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER DEVICE CONTROL CIRCUIT DIAGRAM 14/14			
134-110229-015-0			
NEC			SHT 14/14

134-110229-001-0



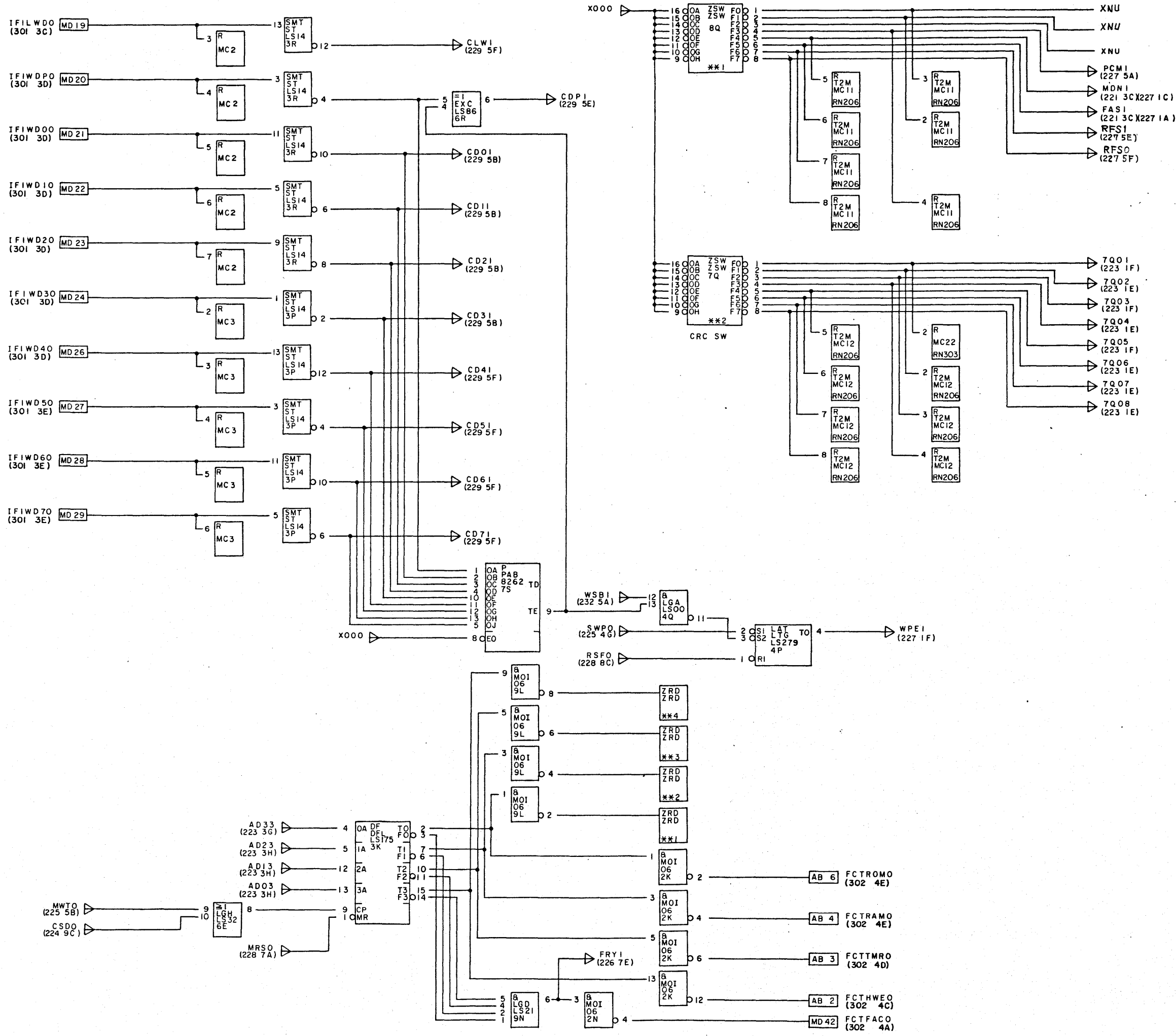
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
2	0	110.11.11 SC-4	大橋
3	0	1981.11.20 SC-5	大橋

DWG ABBR	FCT			
PKG LOCATION				
PKG NAME	99JAW.MWV.QWU			
221				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	6.30

MTA16X FORMATTER
FORMATTER CONTROL
CIRCUIT DIAGRAM
1/14
134-110229-001-0
NEC SHT 1/14

134-110229-001-0

A
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REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

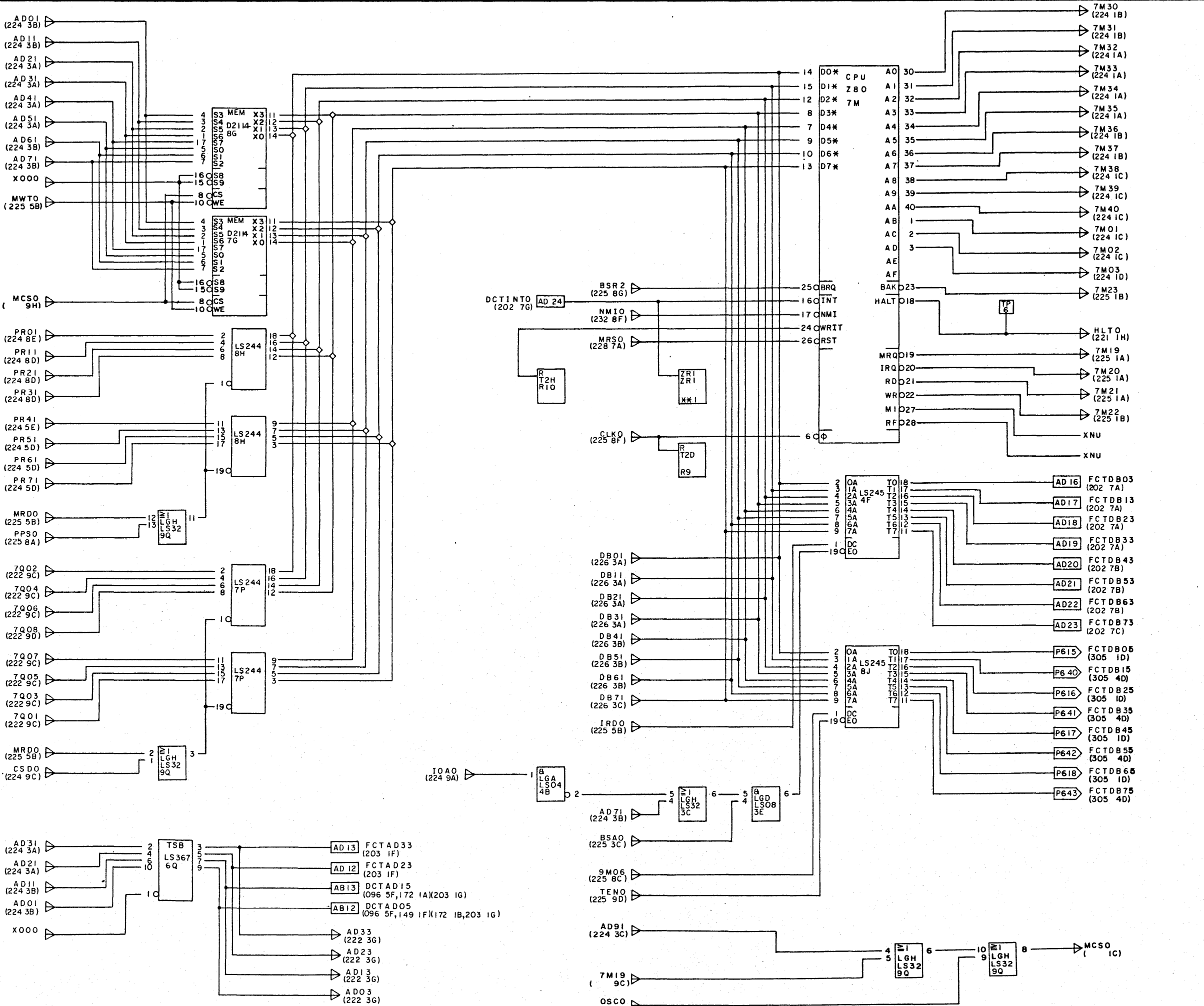
DWG ABBR	F C T			
PKG LOCATION				
PKG NAME	G9JAW, MWV, QWU			
222				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER FORMATTER CONTROL CIRCUIT DIAGRAM 2/14				
134-110229-001-0				
NEC				SHT 2/

A
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F
G
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装置名

134-110229-001-0

A B C D E F G H



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	F C T
PKG LOCATION	
PKG NAME	G9JAW, MWV, DWU
223	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山		今	
	口		村	

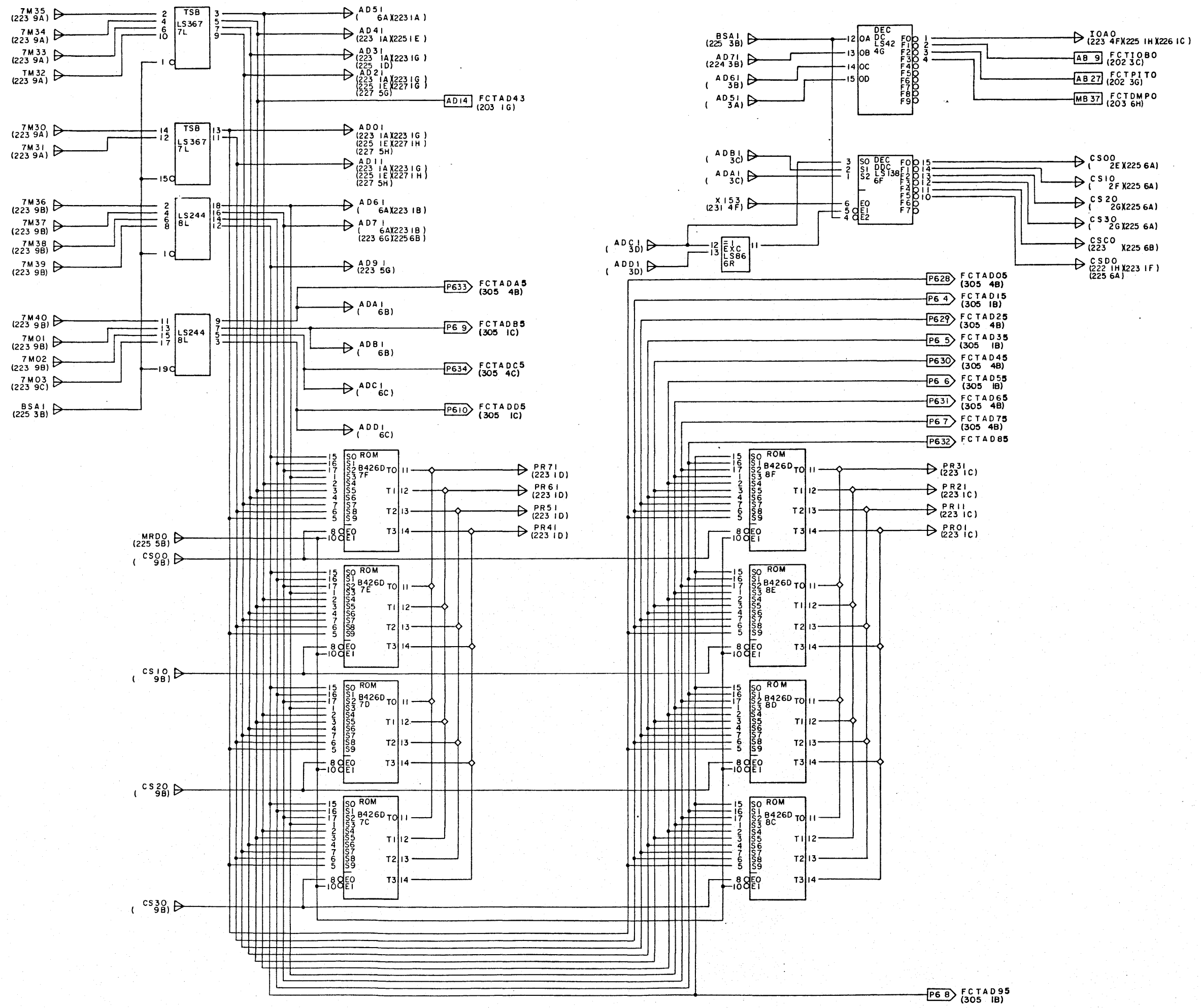
**MTA6X FORMATTER
FORMATTER CONTROL
CIRCUIT DIAGRAM**

3/14

134-110229-001-0

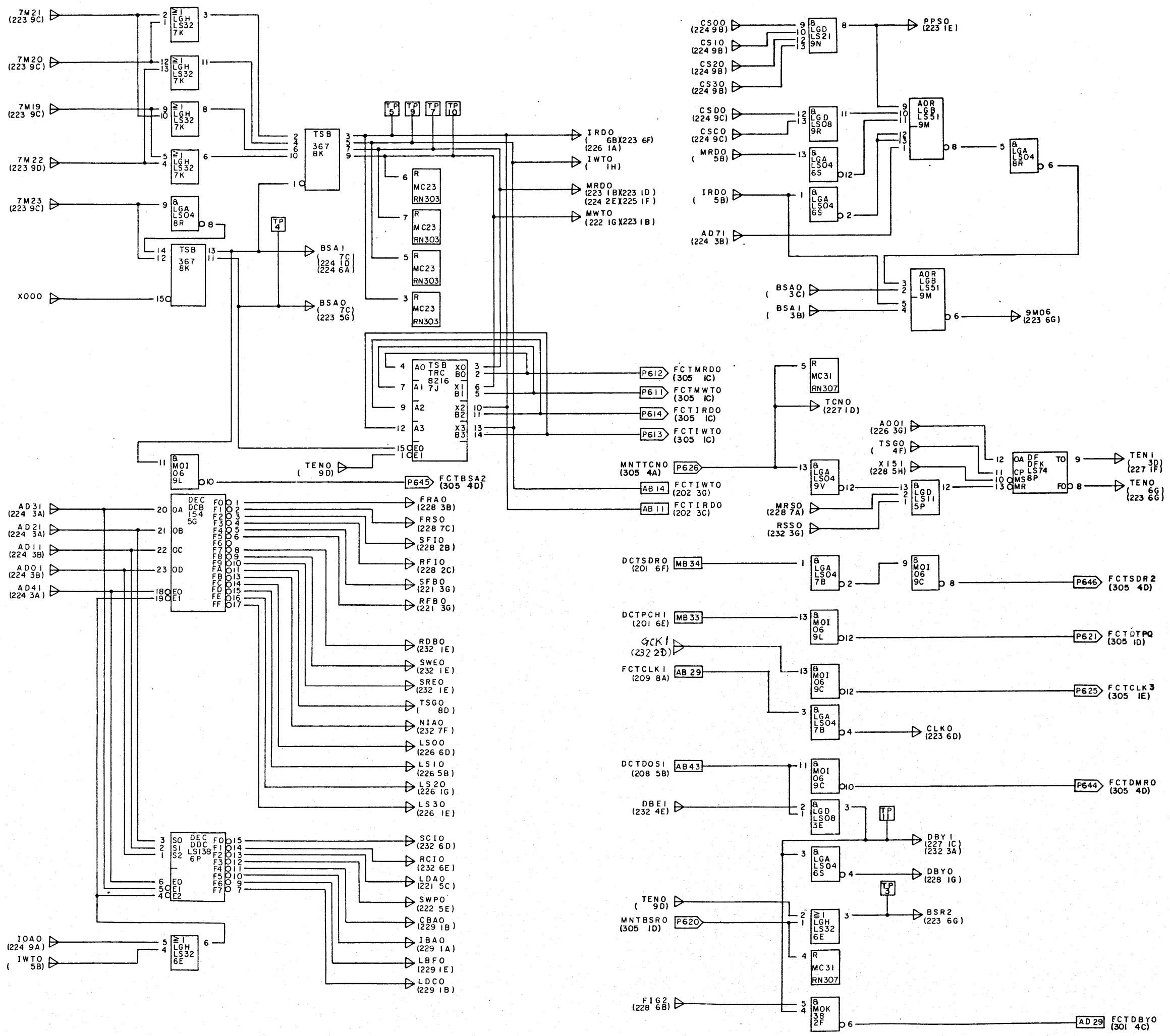
NEC SHT 3/

134-110229-001-



装置名

134-110229-001-0

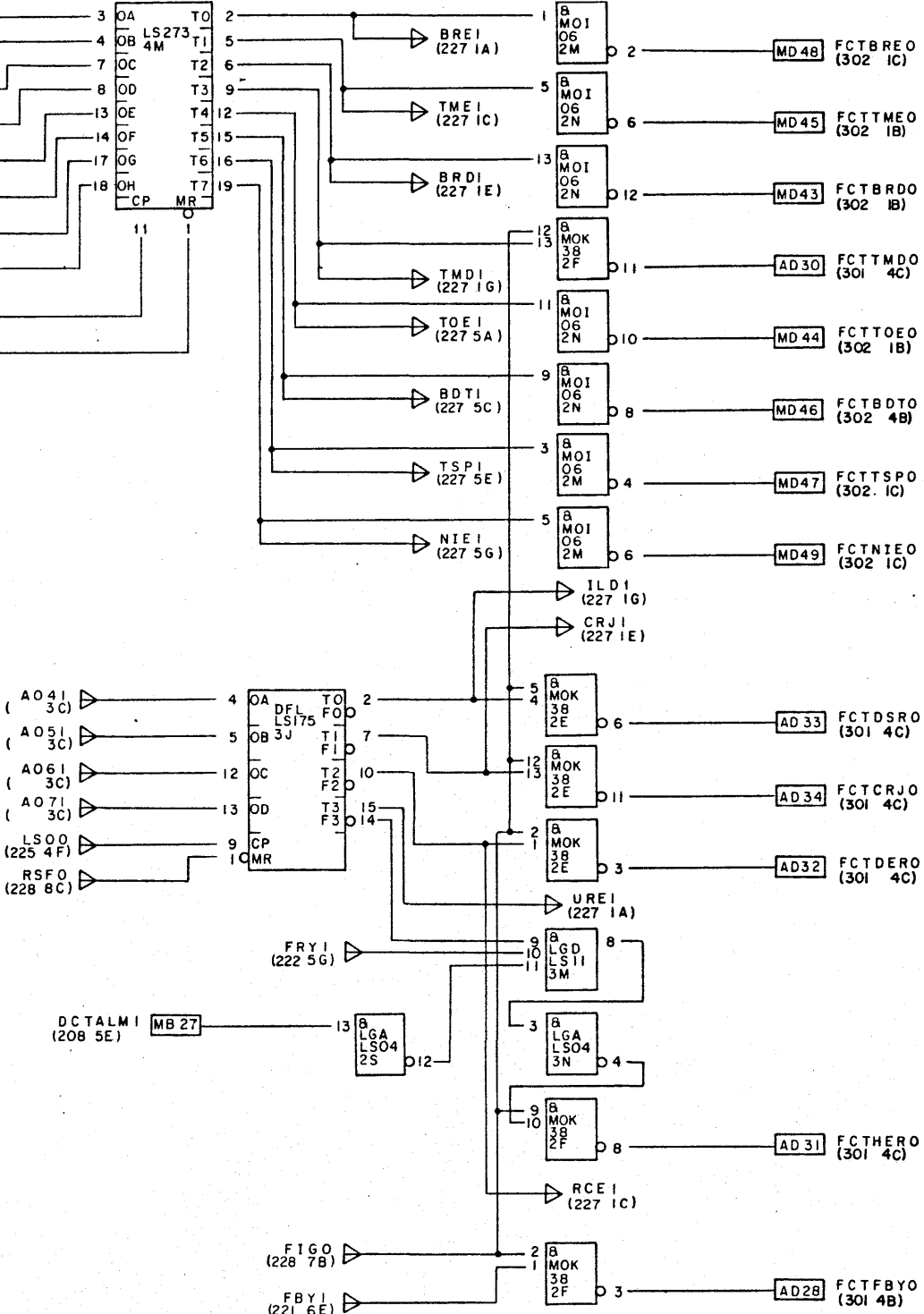
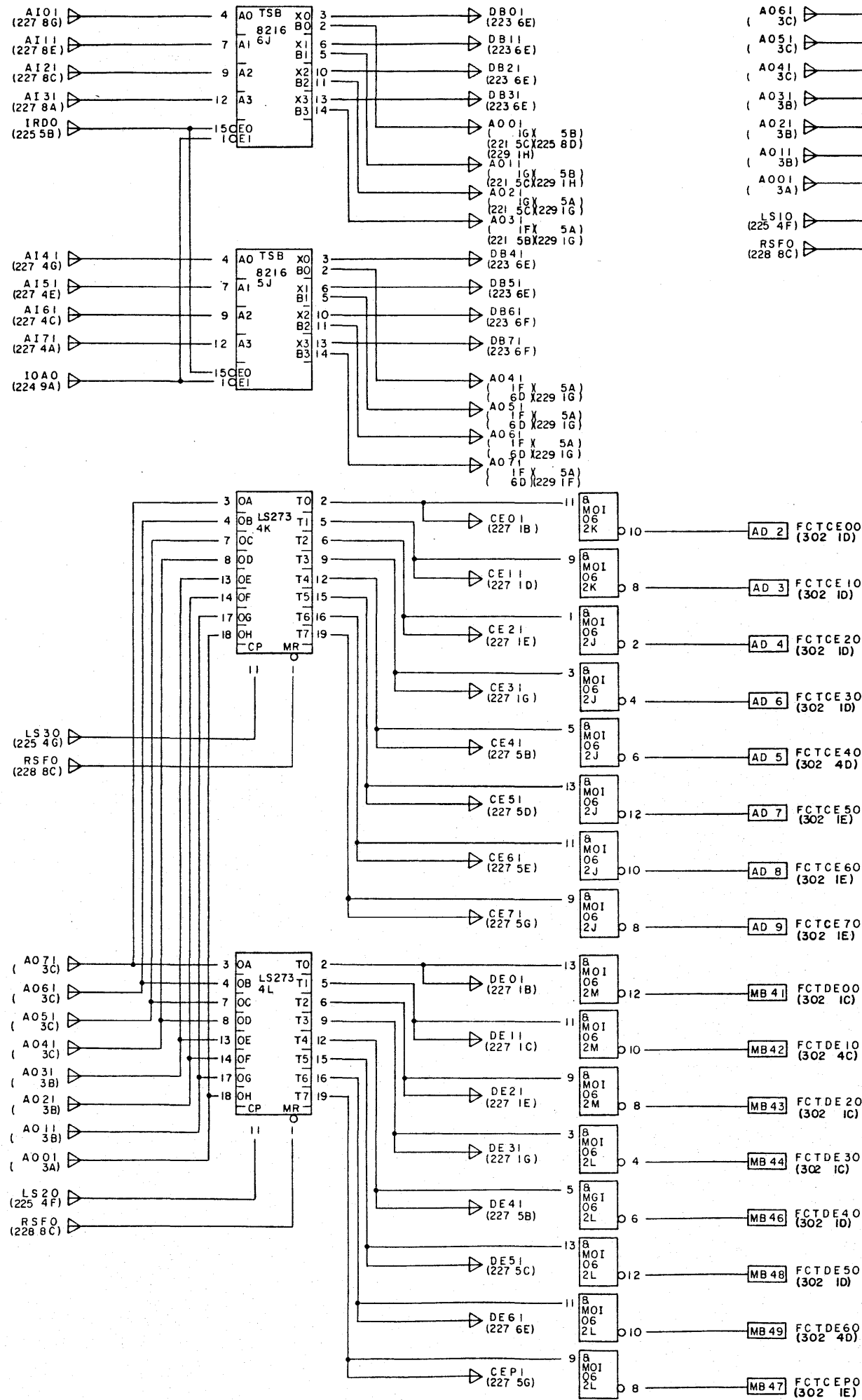


REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	FCT			
PKG LOCATION				
PKG NAME	GRTAW.MWV.QWU			
225				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
 FORMATTER CONTROL
 CIRCUIT DIAGRAM
 5/14
 134-110229-001-0
 NEC SHT 5/

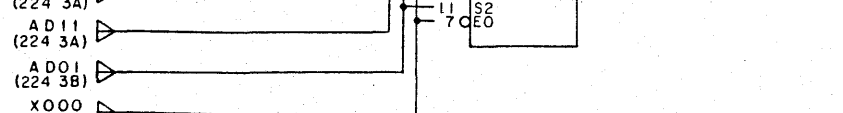
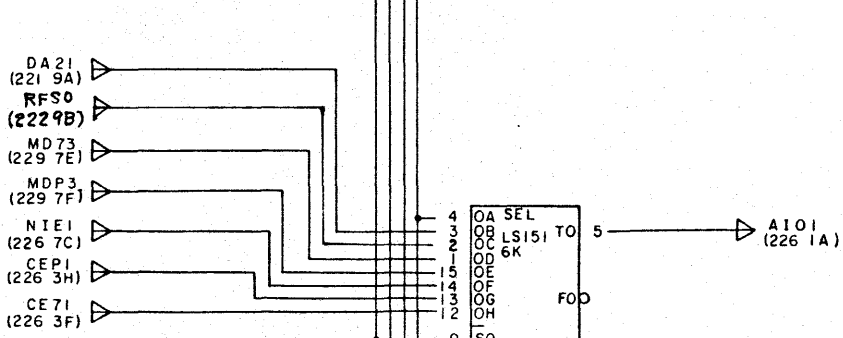
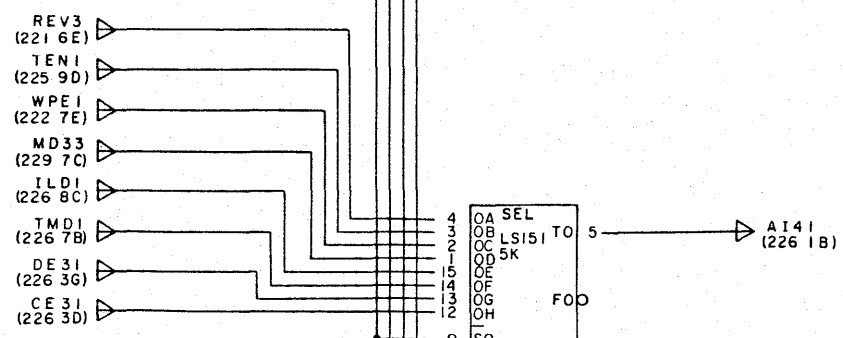
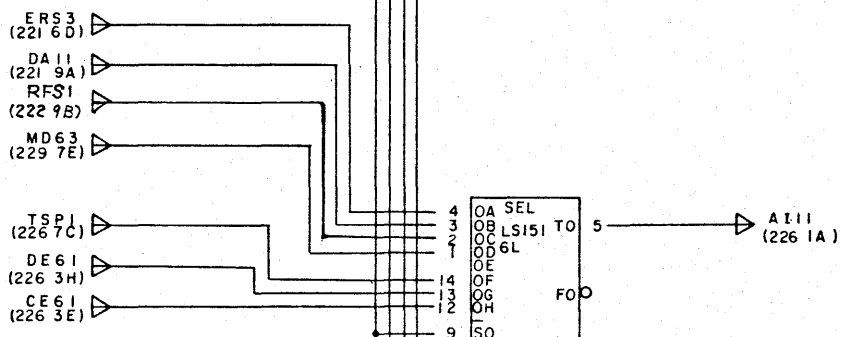
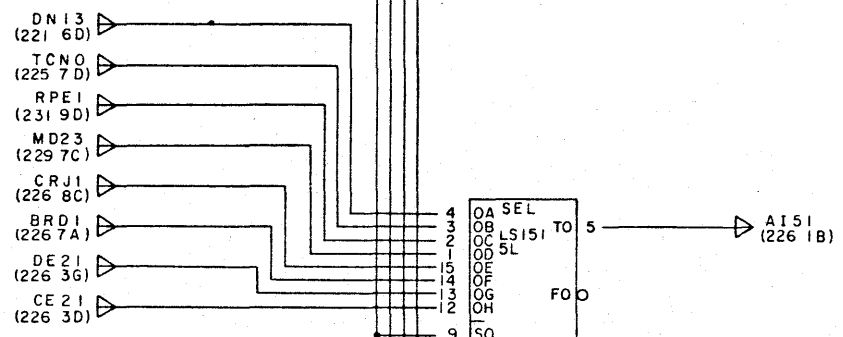
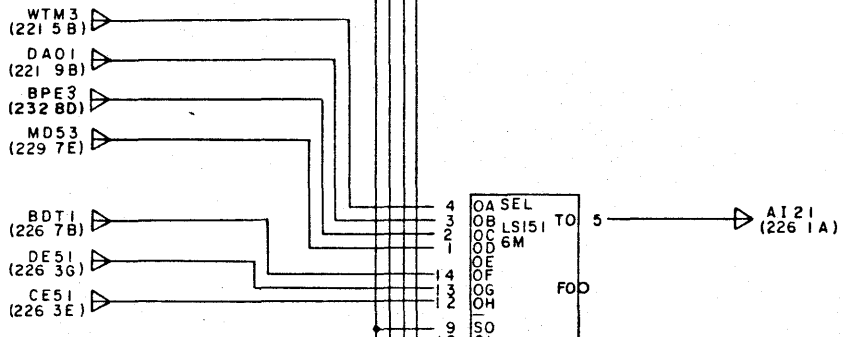
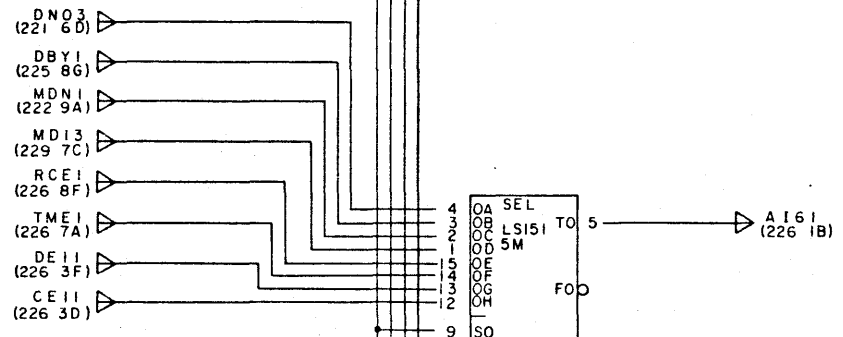
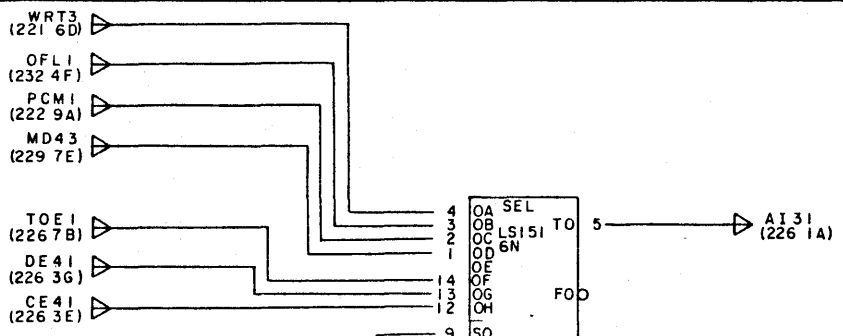
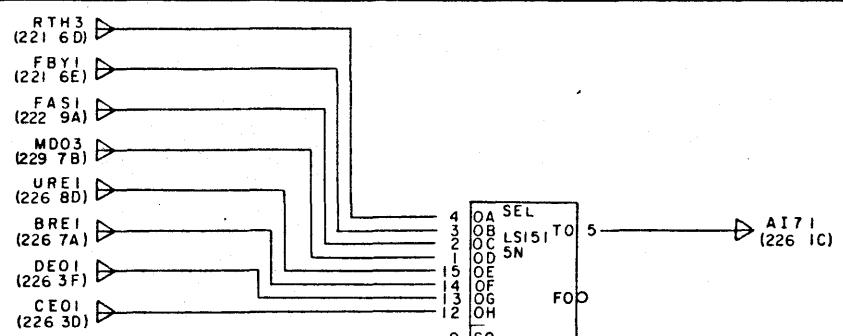
134-110229-001-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
226			
DWG ABBR		FCT	
PKG LOCATION			
PKG NAME		G1JAW,MWV,QWU	
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER FORMATTER CONTROL CIRCUIT DIAGRAM 6/14			
134-110229-001-0			
NEC			SHT 6/

装置名

134-110229-001-0



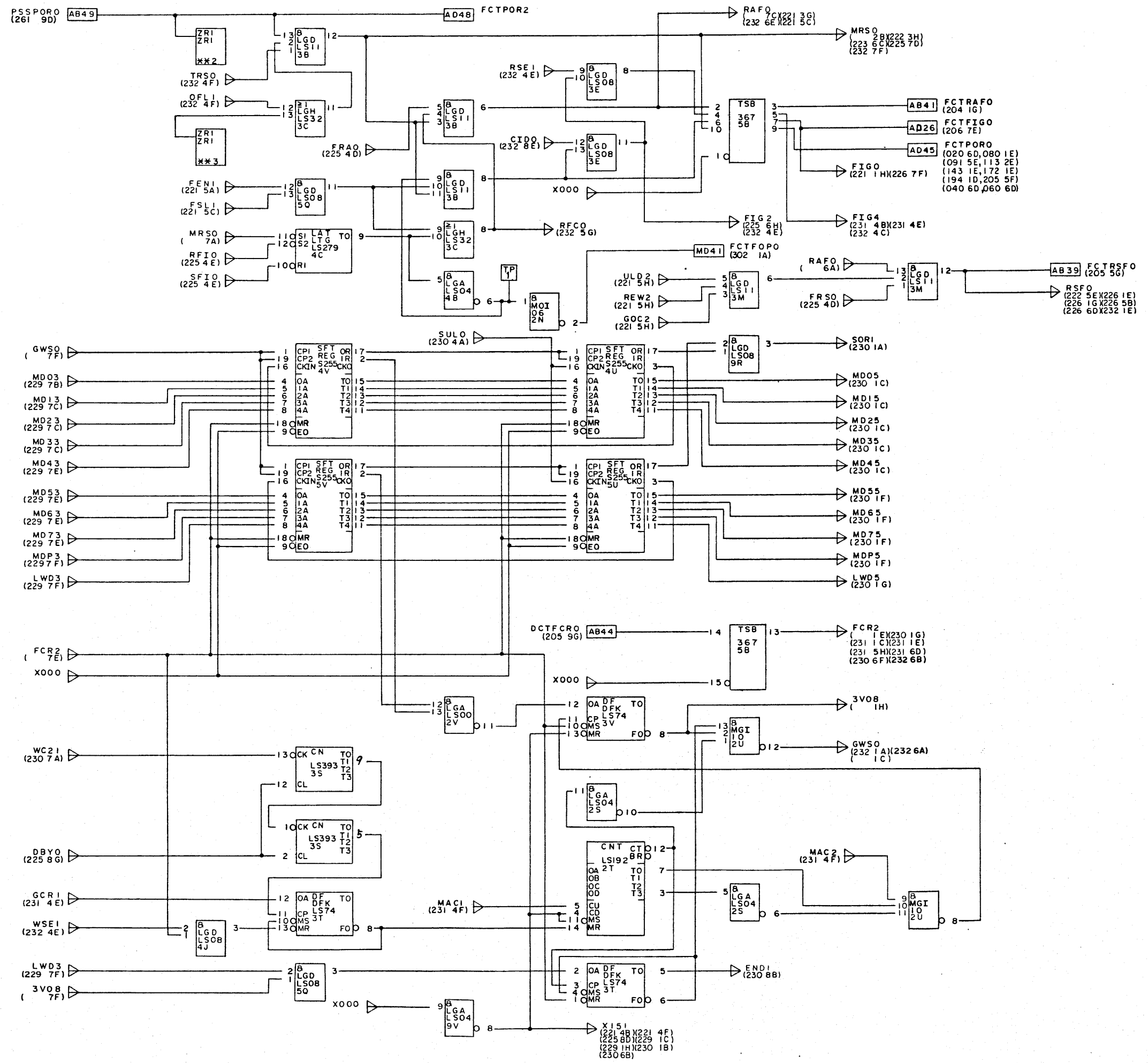
REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	F C T			
PKG LOCATION				
PKG NAME	69JAW, MWV, QWU			
227				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
 FORMATTER CONTROL
 CIRCUIT DIAGRAM
 7/14
 134-110229-001-0
 NEC SHT 7/

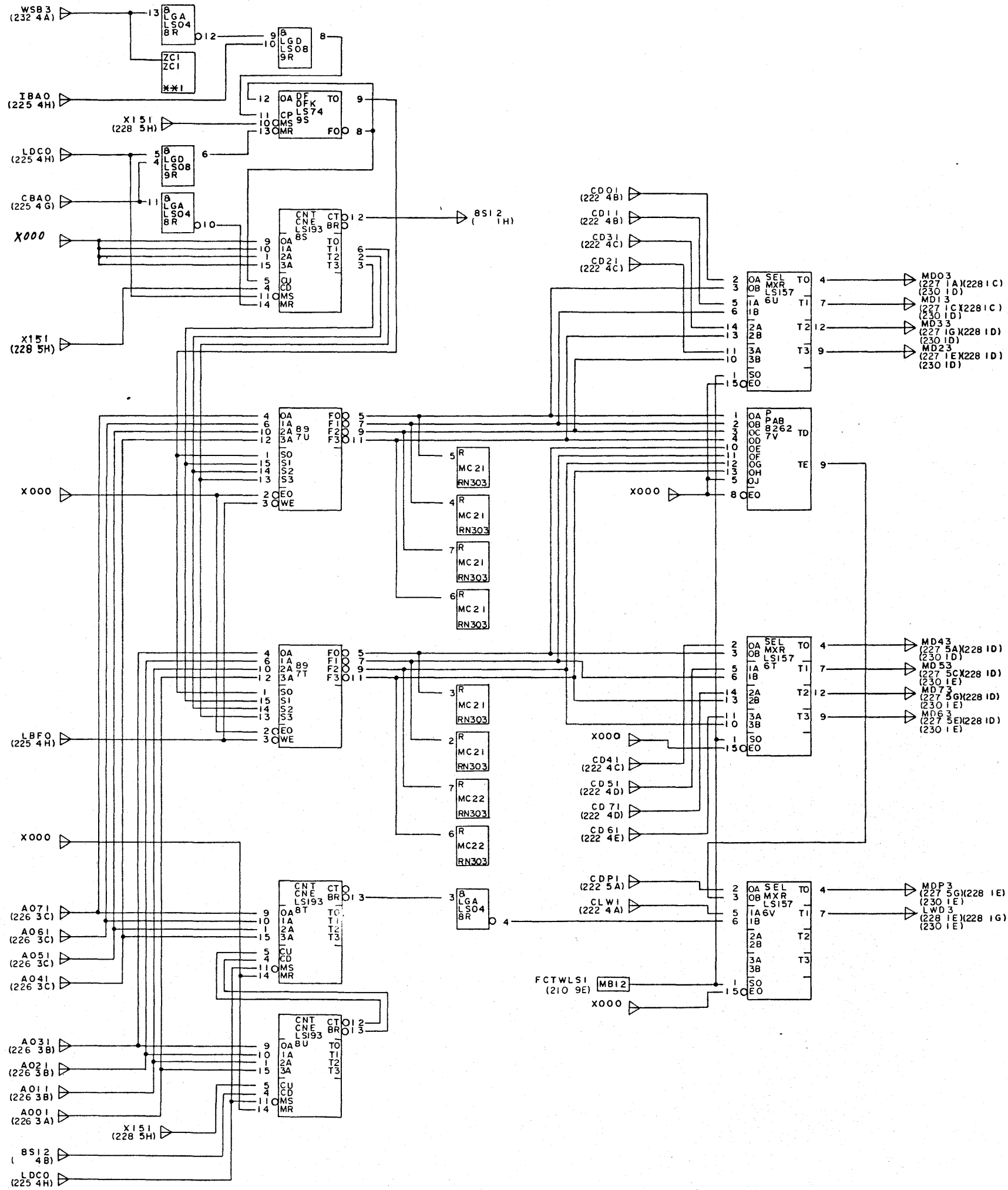
装置名

134-110229-001-0



DWG ABBR	F C T			
PKG LOCATION				
PKG NAME	G7JAW.MWV.QWU			
228				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER FORMATTER CONTROL CIRCUIT DIAGRAM 8/14				
134-110229-001-0				
NEC				SHT 8/

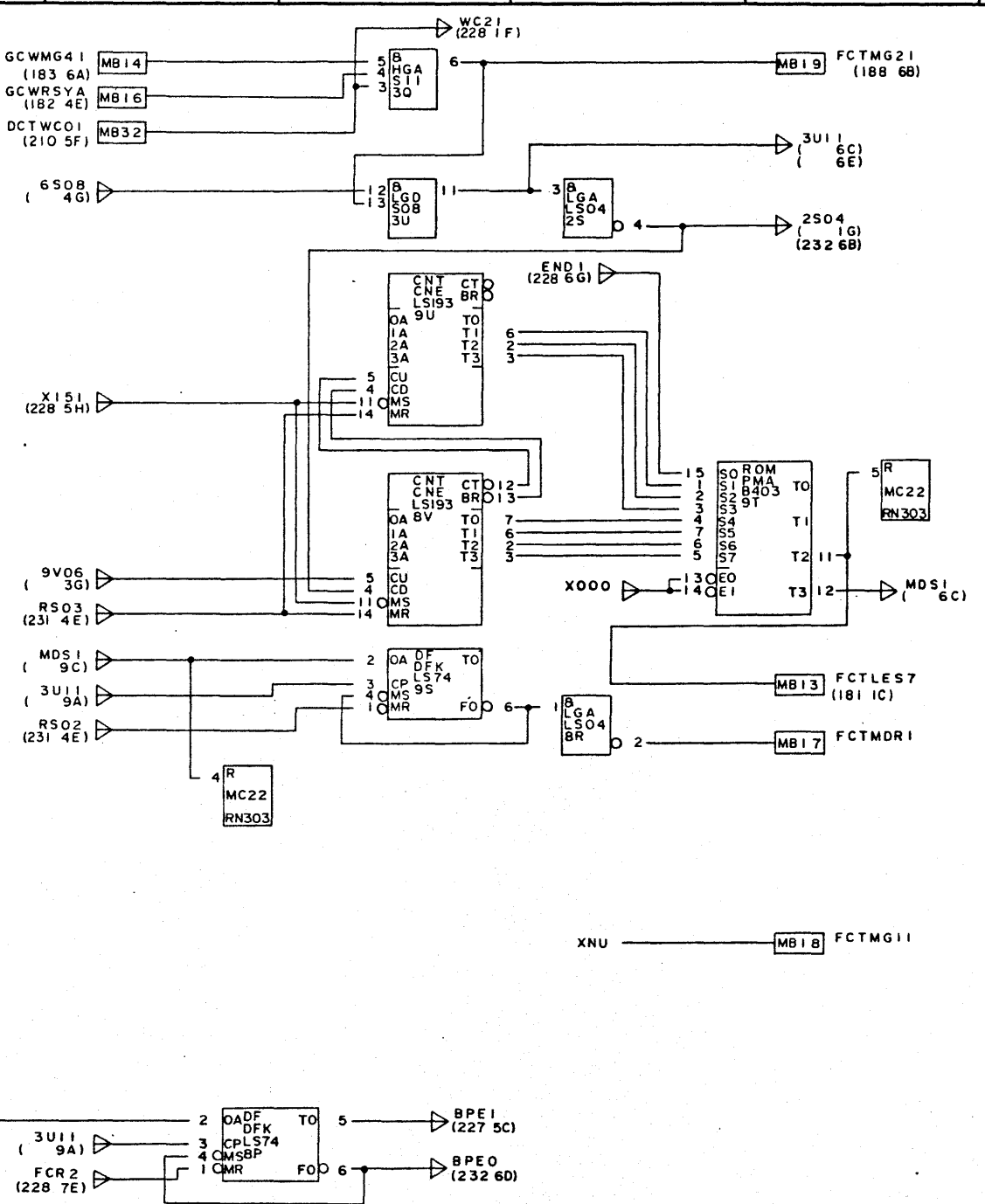
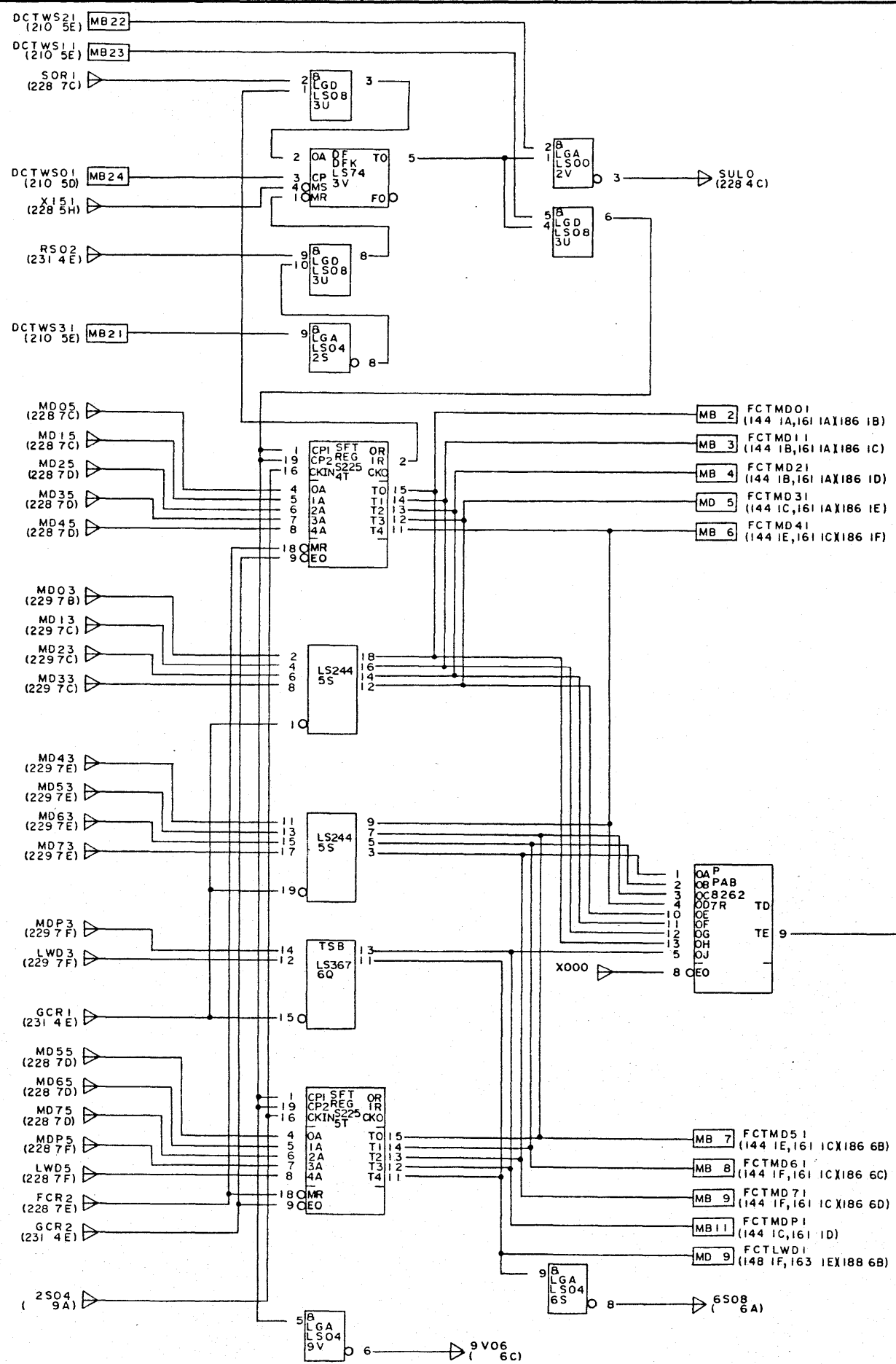
134-110229-001-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
DWG ABBR		FCT	
PKG LOCATION			
PKG NAME		G9JAW.MWV.QWJ	
229			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	山口		今村
MTA16X FORMATTER FORMATTER CONTROL CIRCUIT DIAGRAM 9/14			
134-110229-001-0			
NEC			SHT 9/

装置名
DB-413
JIS A2 (420×594)

134-110229-001-0



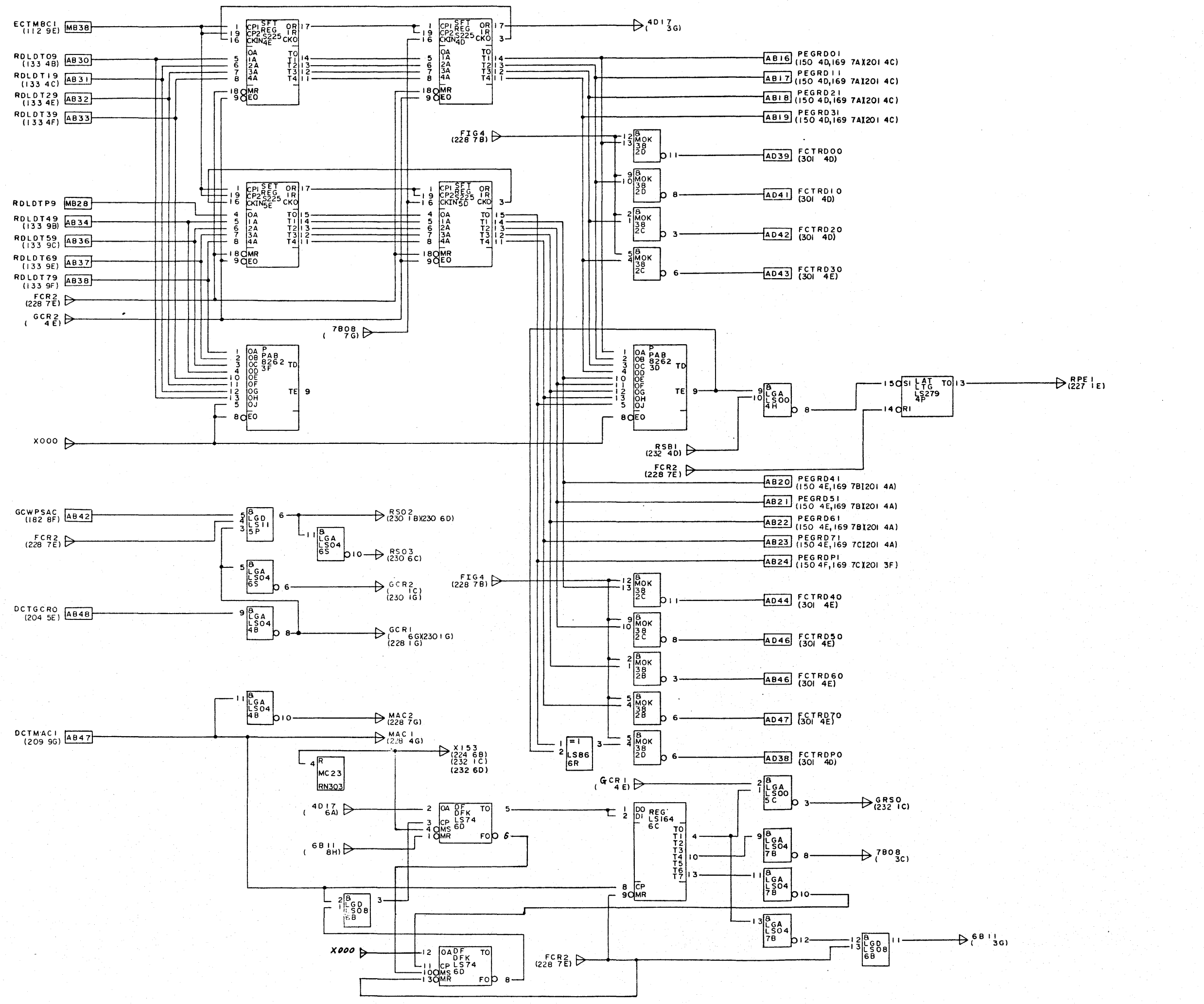
REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	FCT			
PKG LOCATION				
PKG NAME	G9JAW.MWV.QWU			
230				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	
MTA16X FORMATTER FORMATTER CONTROL CIRCUIT DIAGRAM 10/14				
134-110229-001				
NEC				SHT 10/

装置名

134-110229-001-0

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REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

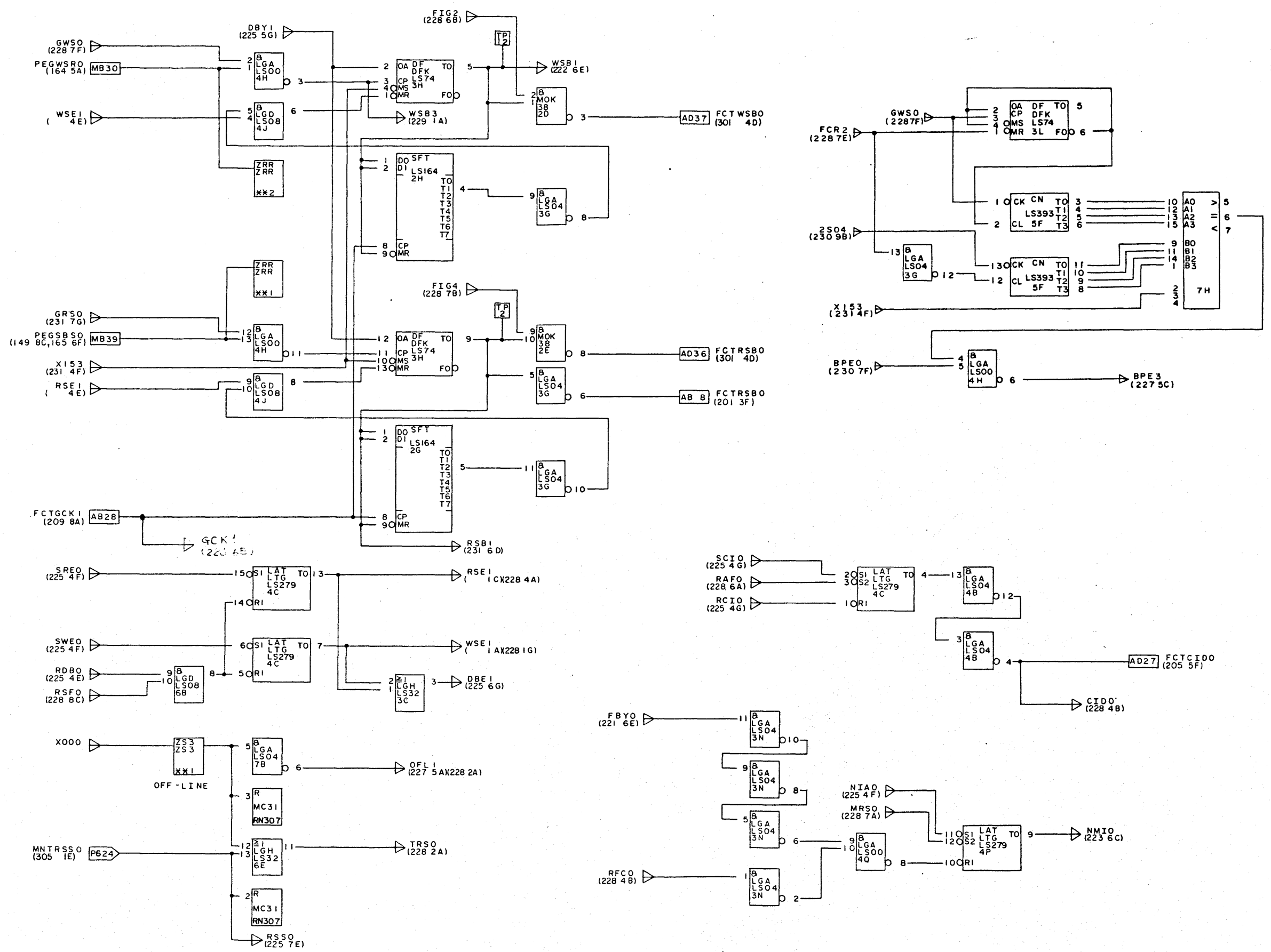
DWG ABBR	FCT			
PKG LOCATION				
PKG NAME	G9JAW.MWV.QWU			
231				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
FORMATTER CONTROL
CIRCUIT DIAGRAM
11/14

134-110229-001-0
NEC SHT 11/

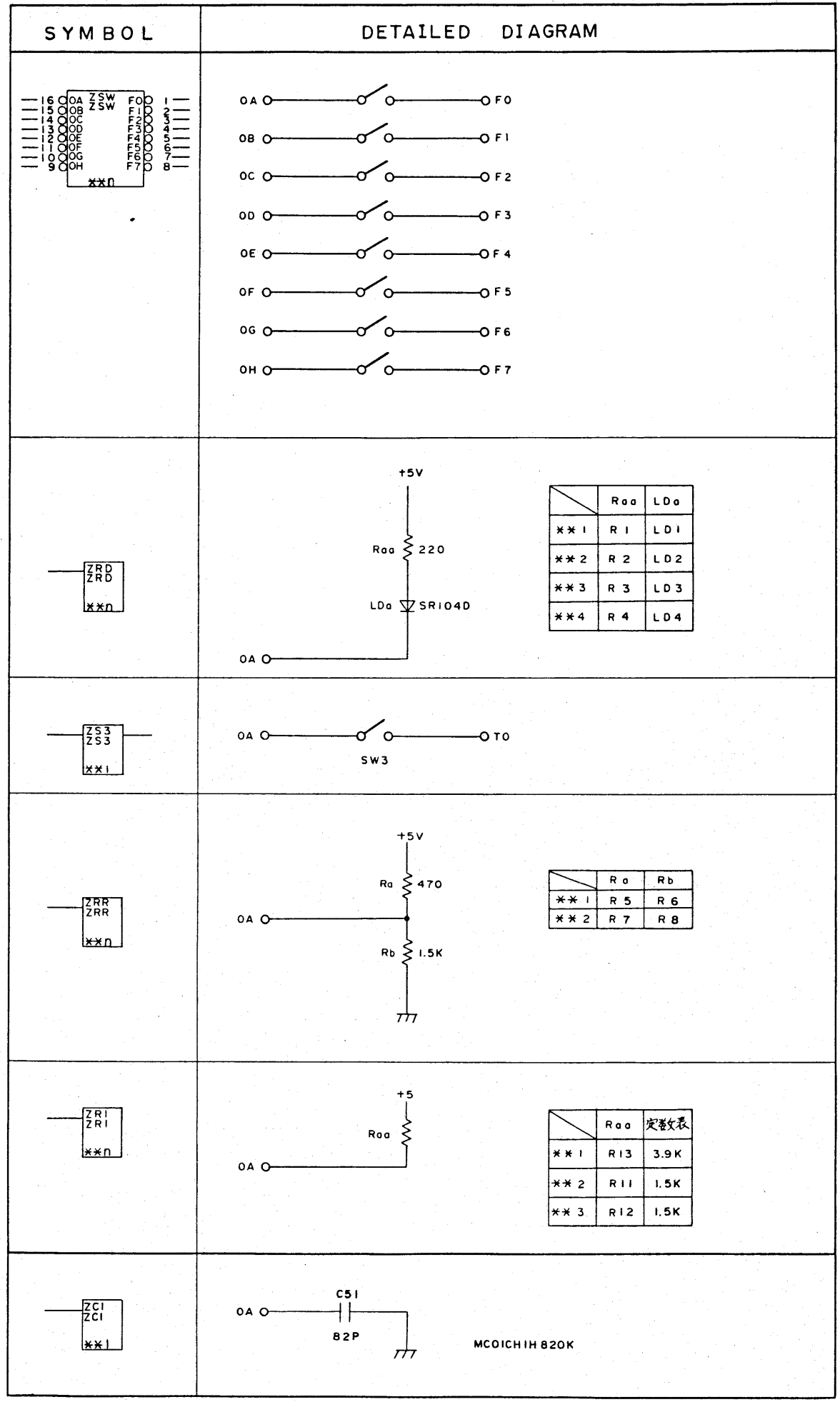
134-110229-001-0

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REV	COMP	DESCRIPTION(SC)	APP																				
1	0	55.5.5																					
<table border="1"> <tr> <td>DWG ABBR</td> <td>FCT</td> </tr> <tr> <td>PKG LOCATION</td> <td></td> </tr> <tr> <td>PKG NAME</td> <td>G9JAW.MWV.QWU</td> </tr> <tr> <td colspan="2" style="text-align: center;">232</td> </tr> <tr> <td>NEXT SPEC</td> <td></td> </tr> <tr> <td>DRAFT</td> <td>ENG</td> <td>CHK</td> <td>APP</td> <td>ISSUE</td> </tr> <tr> <td></td> <td>山口</td> <td></td> <td>今村</td> <td></td> </tr> </table>				DWG ABBR	FCT	PKG LOCATION		PKG NAME	G9JAW.MWV.QWU	232		NEXT SPEC		DRAFT	ENG	CHK	APP	ISSUE		山口		今村	
DWG ABBR	FCT																						
PKG LOCATION																							
PKG NAME	G9JAW.MWV.QWU																						
232																							
NEXT SPEC																							
DRAFT	ENG	CHK	APP	ISSUE																			
	山口		今村																				
MTA16X FORMATTER FORMATTER CONTROL CIRCUIT DIAGRAM 12/14																							
134-110229-001-0																							
NEC			SHT 12/																				

134-110229-001-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

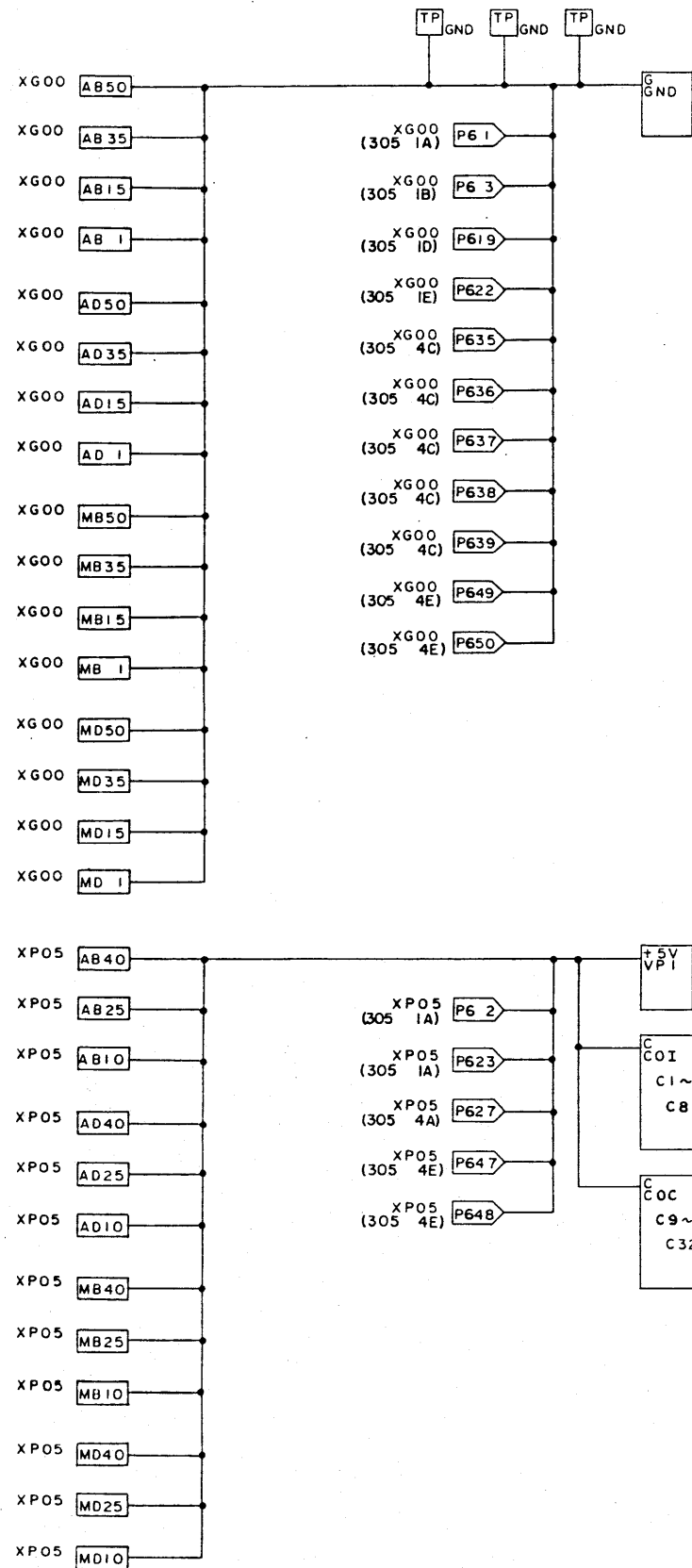
DWG ABBR	F C T			
PKG LOCATION				
PKG NAME	G?JAW.MWV.QWU			
233				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
 FORMATTER CONTROL
 CIRCUIT DIAGRAM
 13/14

134-110229-001-0

NEC SH 13/

134-110229-001-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	F C T			
PKG LOCATION				
PKG NAME	G9JAW, MWV, QWU			
234				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
 FORMATTER CONTROL
 CIRCUIT DIAGRAM
 14/14

134-110229-001-0
 NEC SHT 14/14

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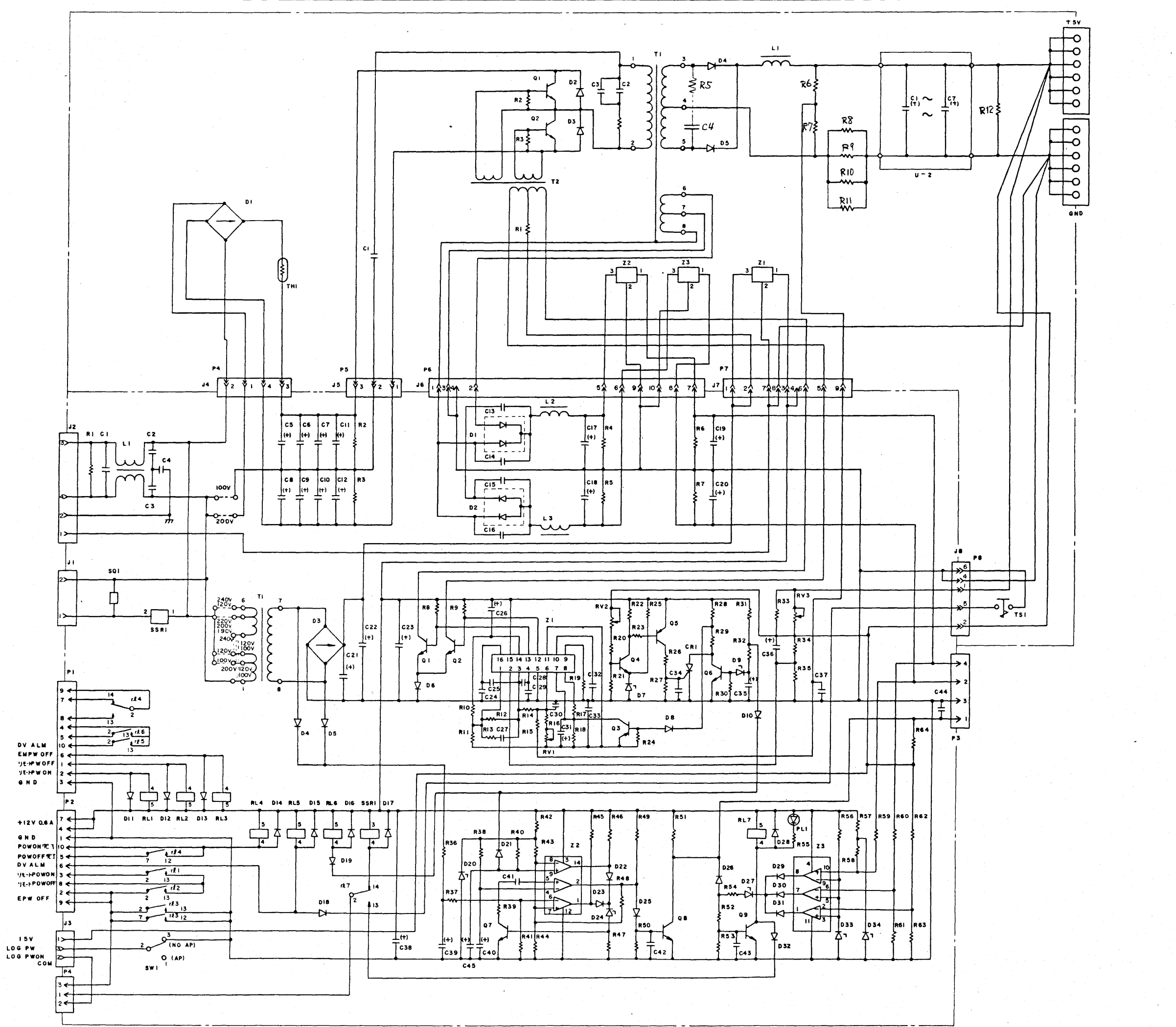
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装置名

134-190317-0

57.6.17

1 2 3 4 5 6 7 8 9 X Y



REV	COMP	DESCRIPTION (SC)	APP
1	0	1981.8	

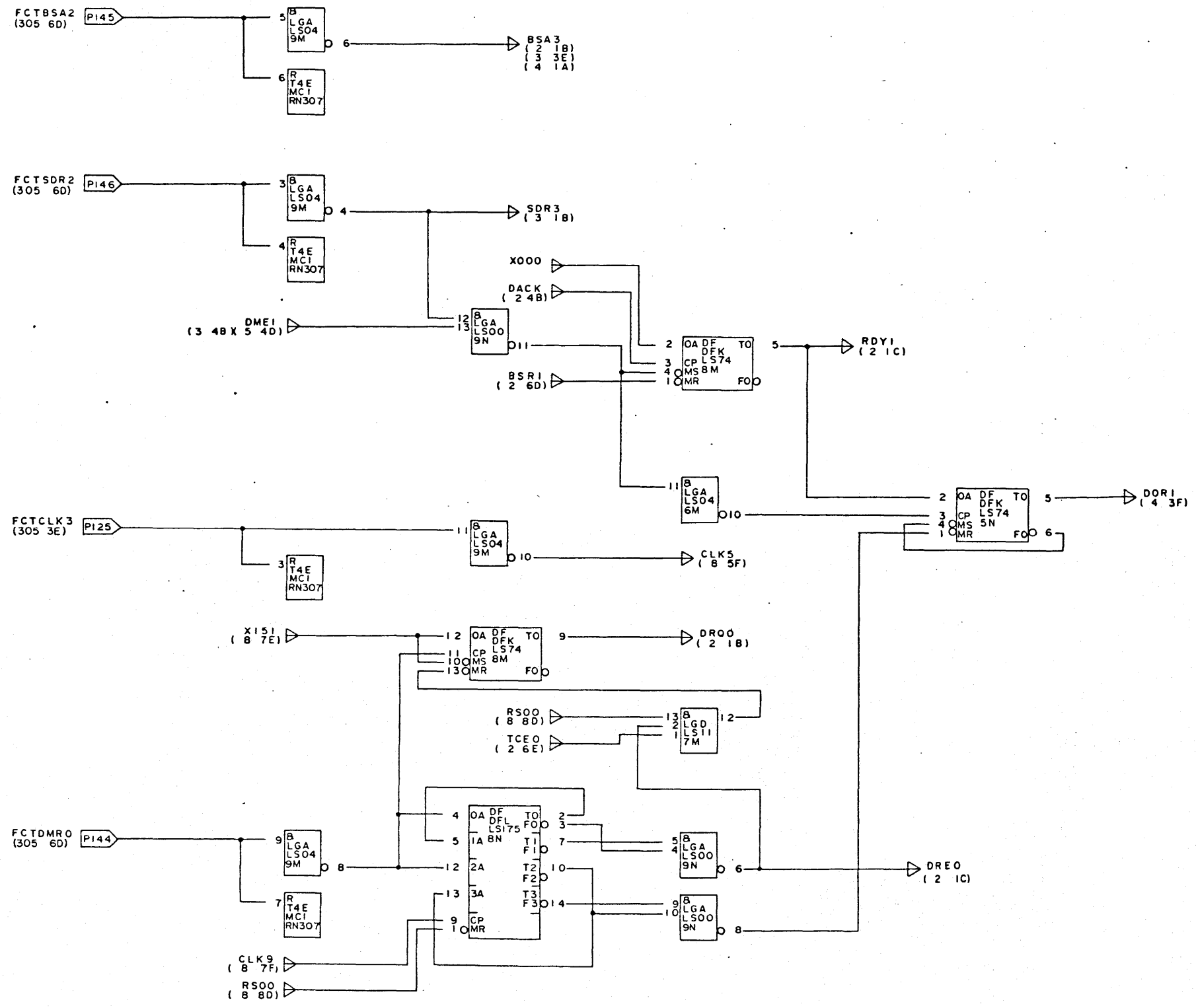
DWG ABBR	GFMTPS			
PKG LOCATION				
PKG NAME				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	51.6.17

MTA160
POWER
SUPPLY
CIRCUIT DIAGRAM

134-190317-0

NEC SHT 1/1

134-110238-001-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
2	1		大橋
			羽賀

DWG ABBR	MNT
PKG LOCATION	
PKG NAME	G9JBC
271	
NEXT SPEC	

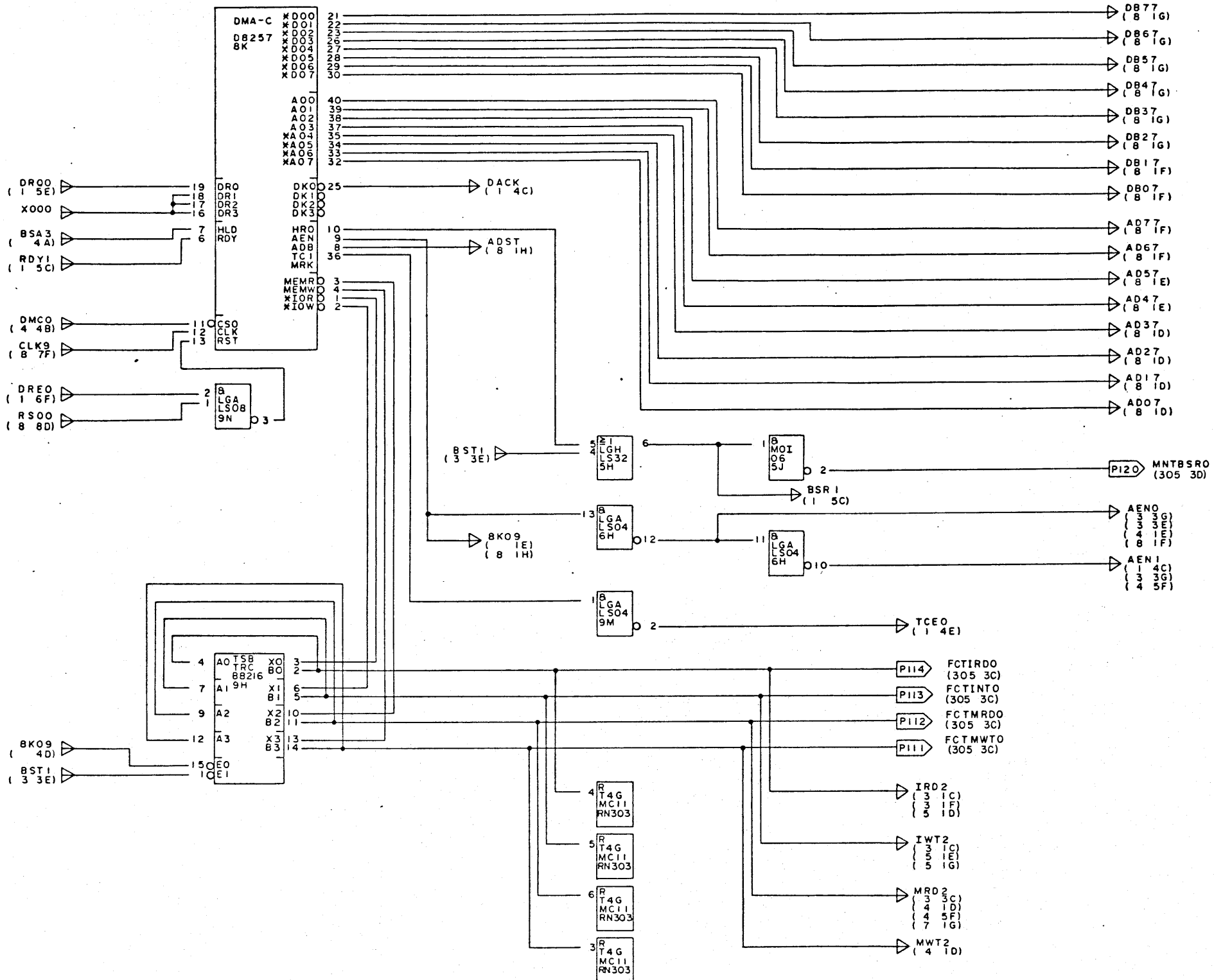
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	4/10

MTA 160
FMT TESTER
CIRCUIT DIAGRAM
1/10

134-110238-001-0
NEC
SHT 1/10

装置名

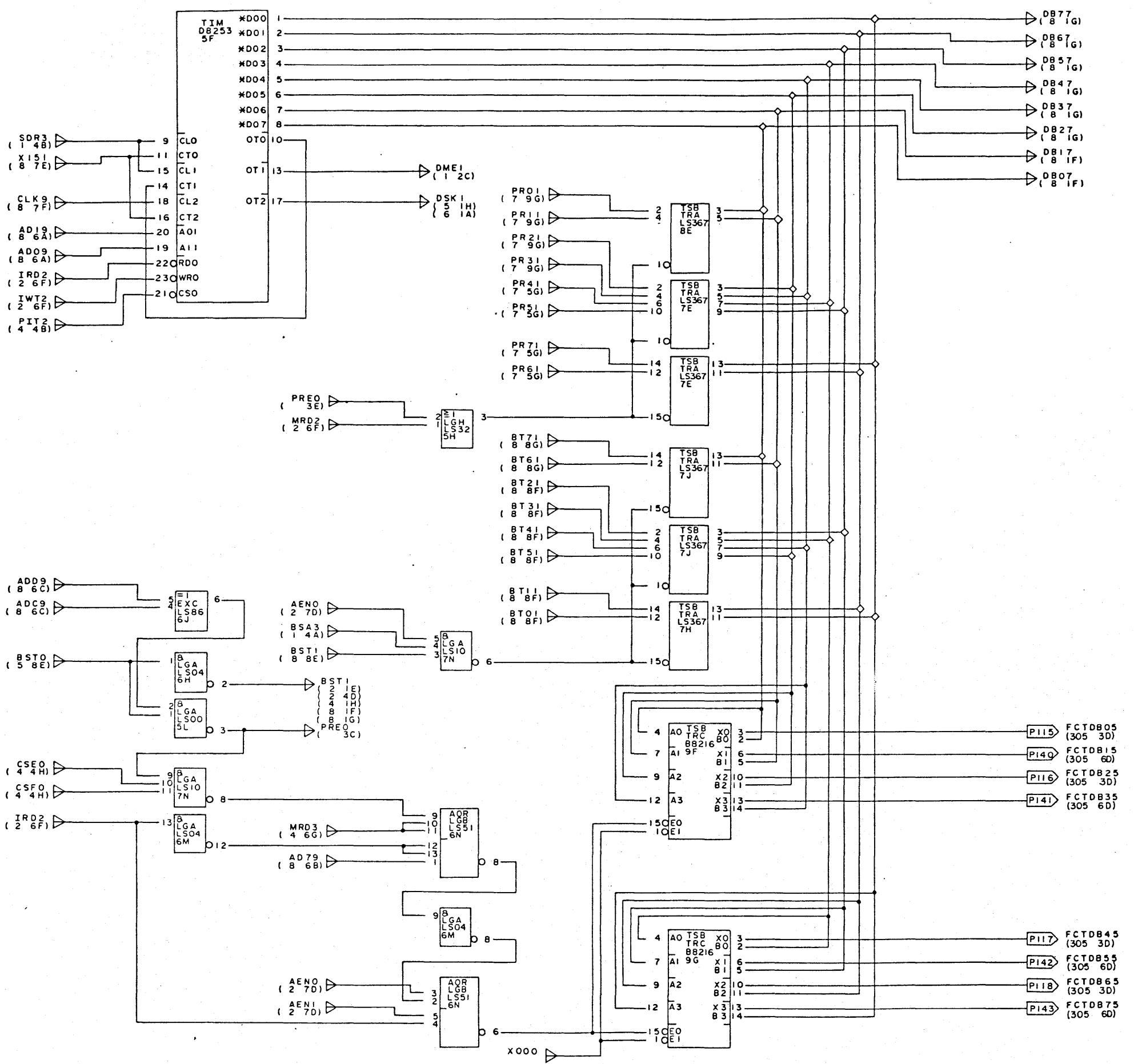
134-110238-001-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5-5	

DWG ABBR	MNT			
PKG LOCATION				
PKG NAME	G9JBC			
272				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
MTA160 FMT TESTER CIRCUIT DIAGRAM 2/10				
134-110238-001-0				
NEC				SHT 2/

134-110238-001-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	55.5.5	

DWG ABBR	MNT
PKG LOCATION	
PKG NAME	G9JBC

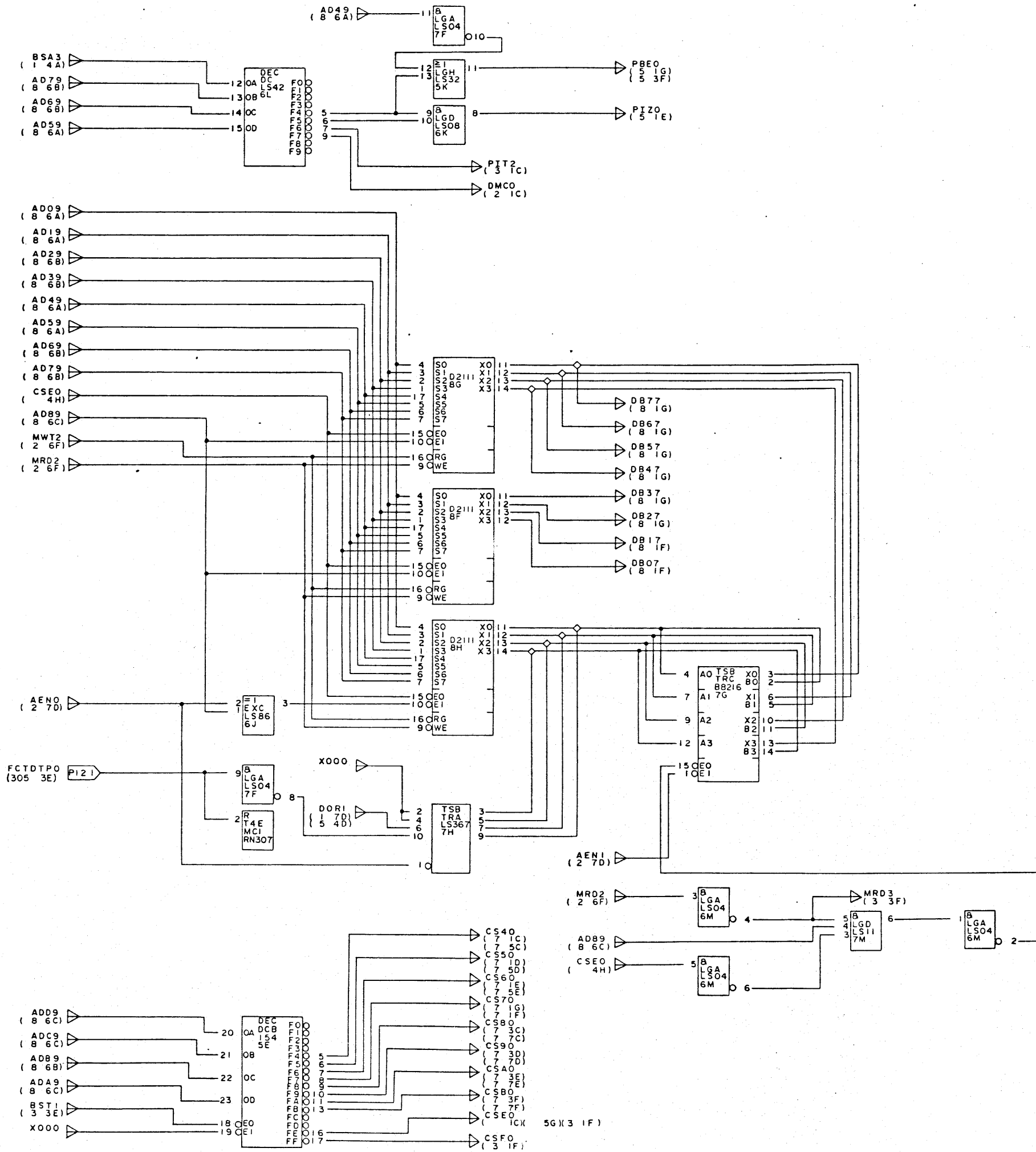
273				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

	羽		今	
	賀		村	

MTA 160
FMT TESTER
CIRCUIT DIAGRAM
3/10

134-110238-001-0	
NEC	SHT 3/

134-110238-001-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

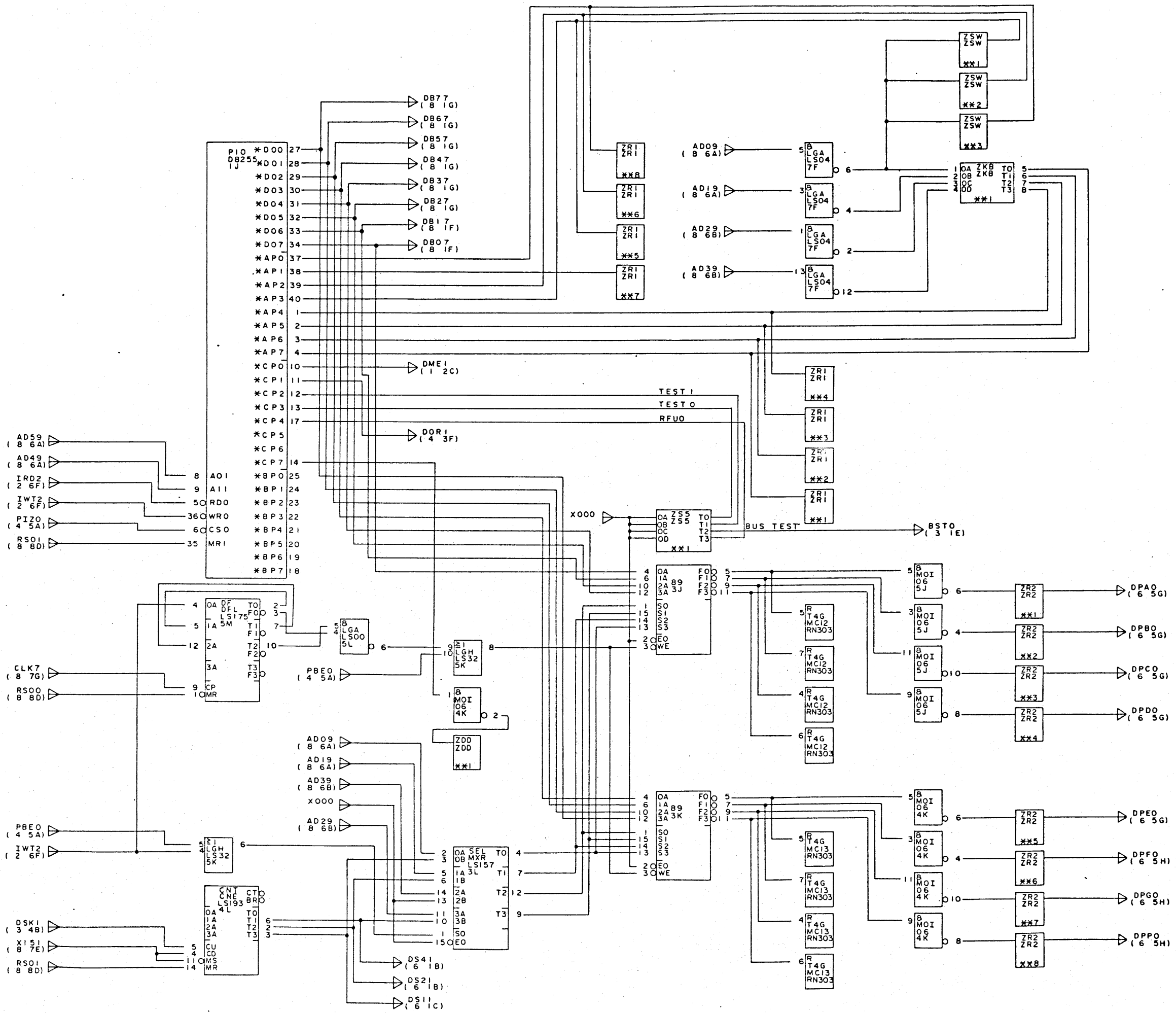
DWG ABBR	MNT			
PKG LOCATION				
PKG NAME	G9JBC			
274				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	

MTA 160
FMT TESTER
CIRCUIT DIAGRAM
4/10

134-110238-001-0

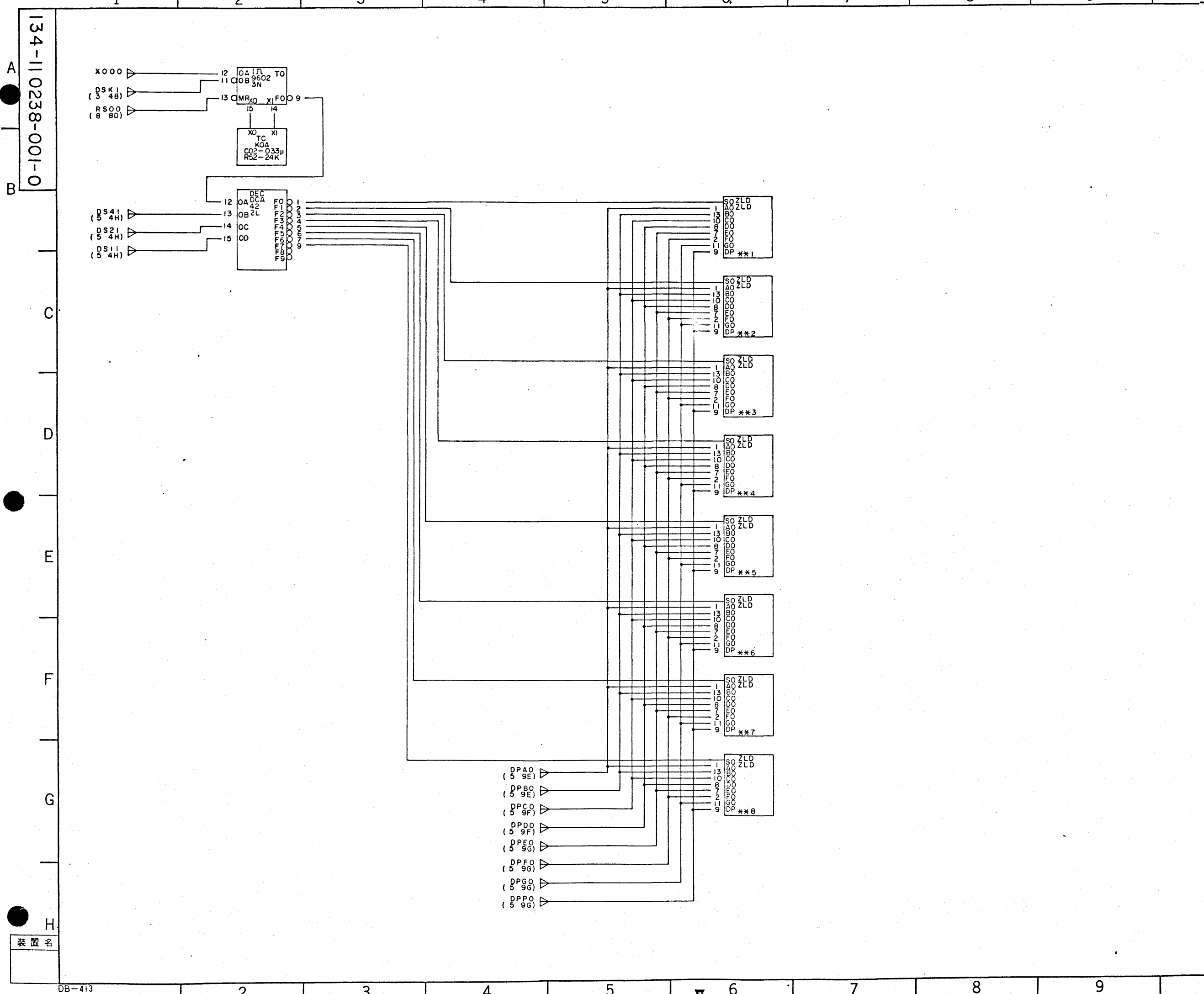
NEC SHT 4/

134-110238-001-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	MNT			
PKG LOCATION				
PKG NAME	G9JBC			
275				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	
MTA 160 FMT TESTER CIRCUIT DIAGRAM 5/10				
134-110238-001-0				
NEC				SHT 5/



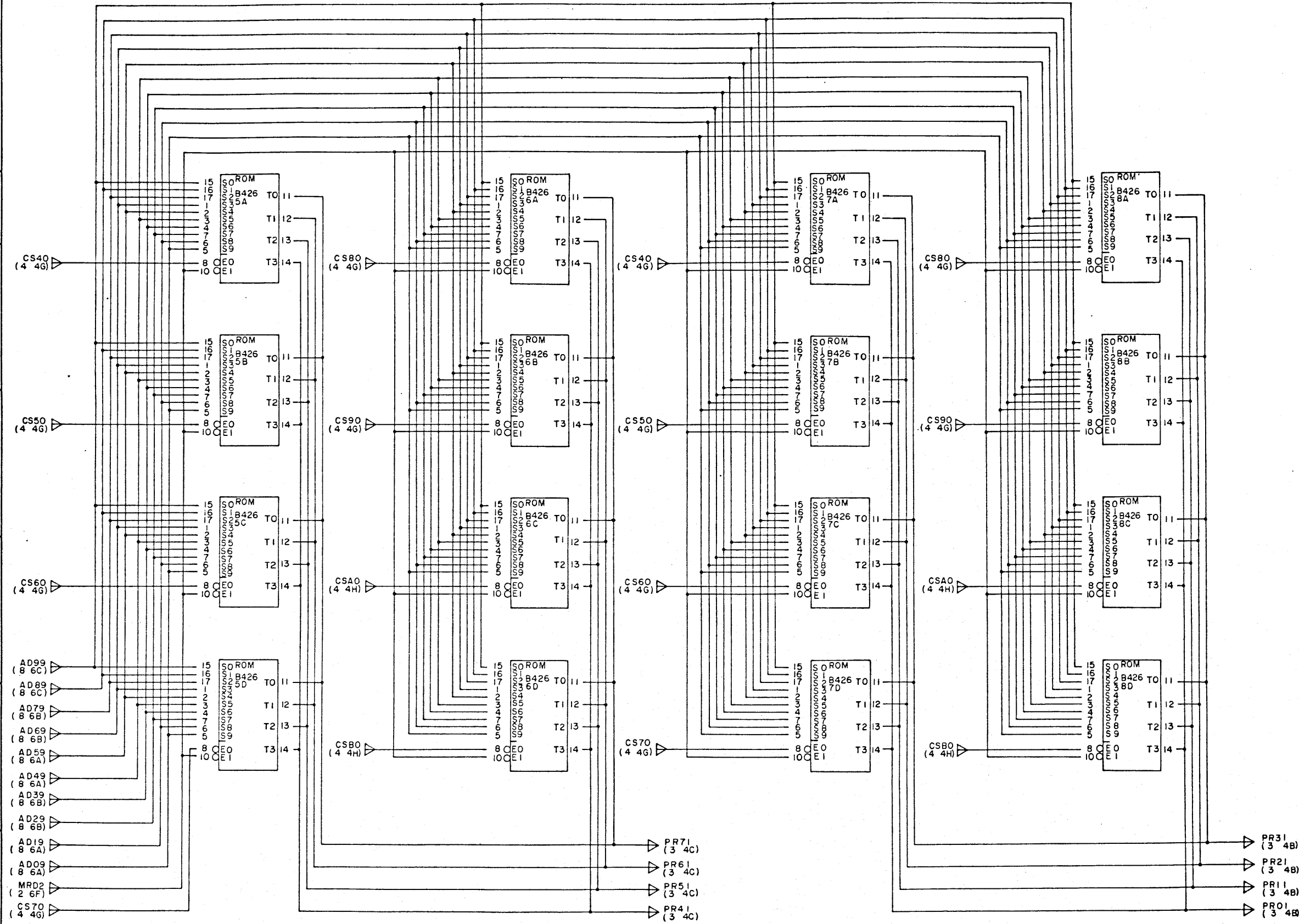
134-110238-001-0

装置名

REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	MNT			
PKG LOCATION				
PKG NAME	G9JBC			
276				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
MTA 160 FMT TESTER CIRCUIT DIAGRAM 6/10				
134-110238-001-0				
NEC				SHT 6/

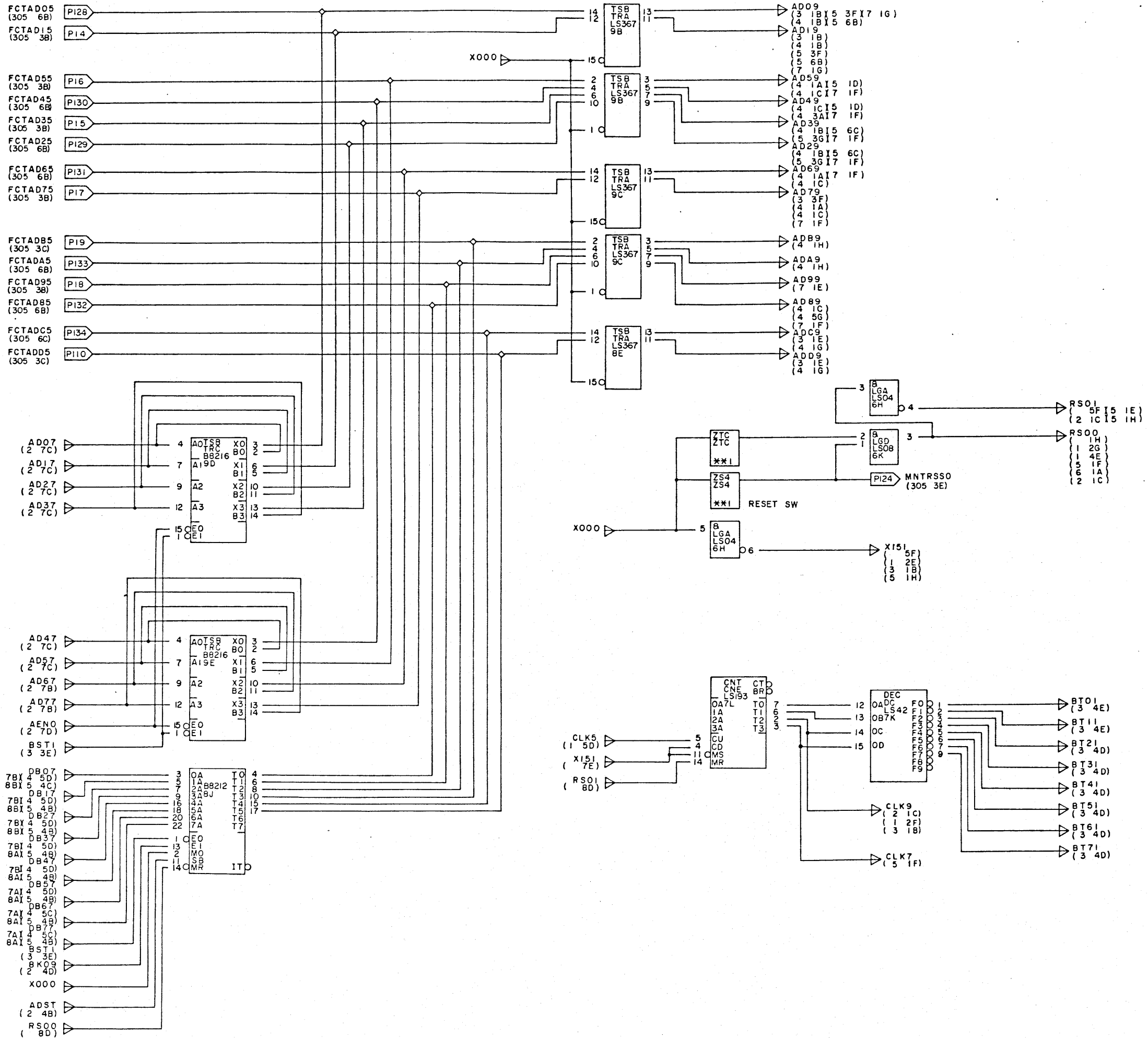
134-110238-001-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	M N T			
PKG LOCATION				
PKG NAME	G 9 J B C			
2 7 7				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽		今	
	賀		村	
MTA 160 FMT TESTER CIRCUIT DIAGRAM 7/10				
134-110238-001-0				
NEC				SHT 7/

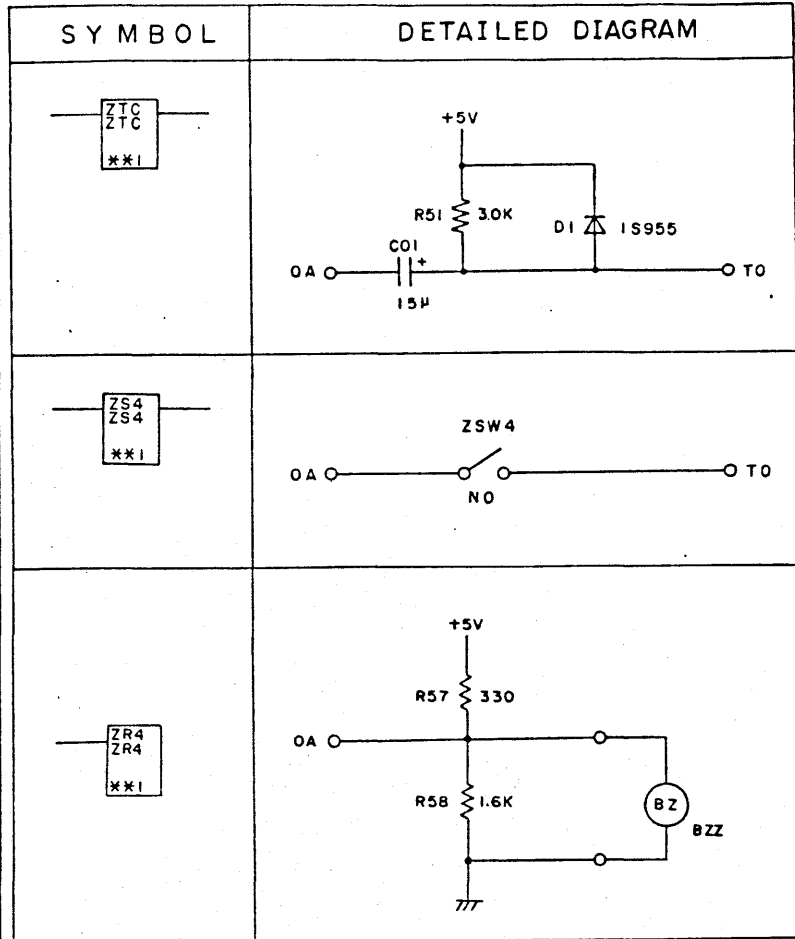
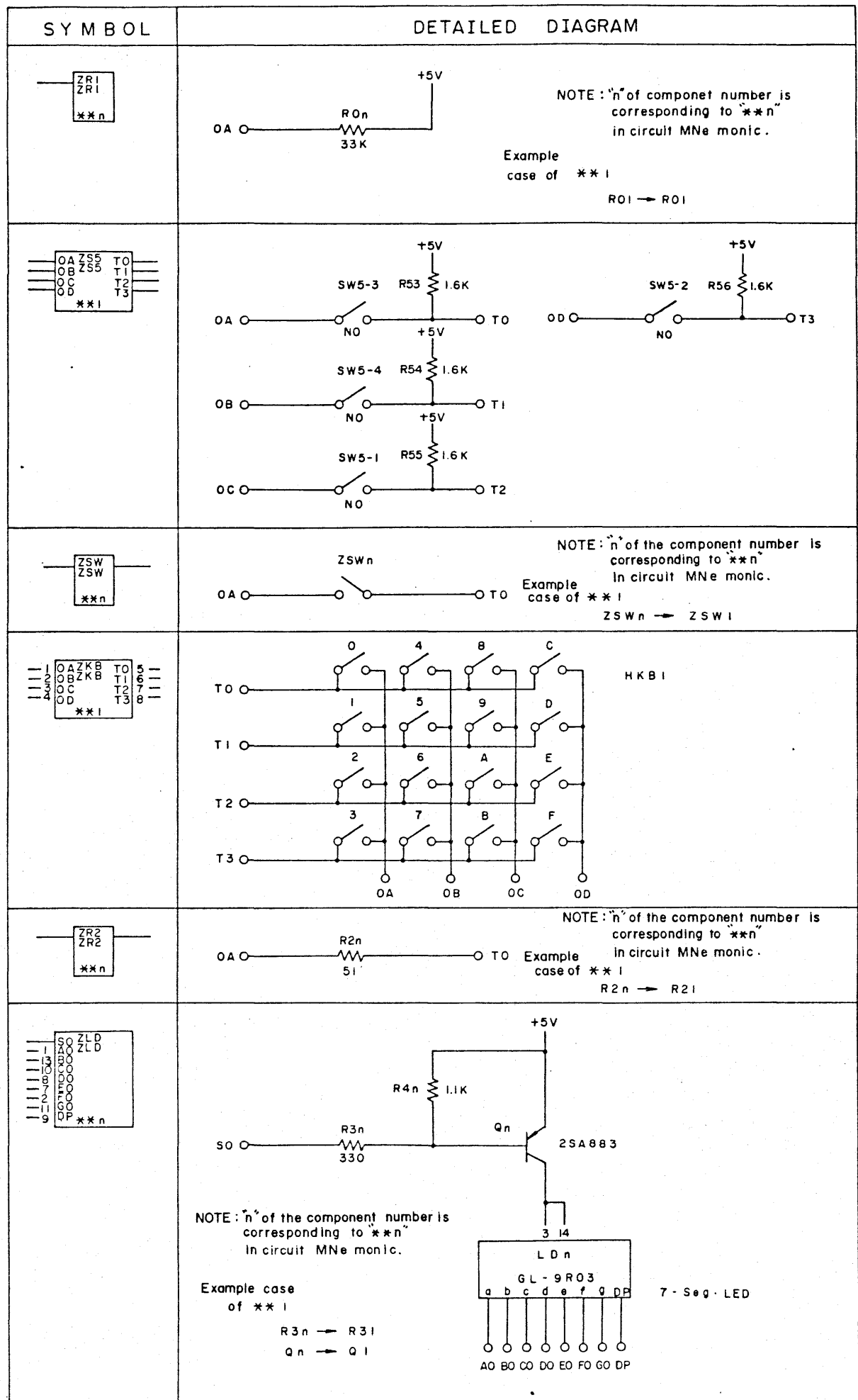
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REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

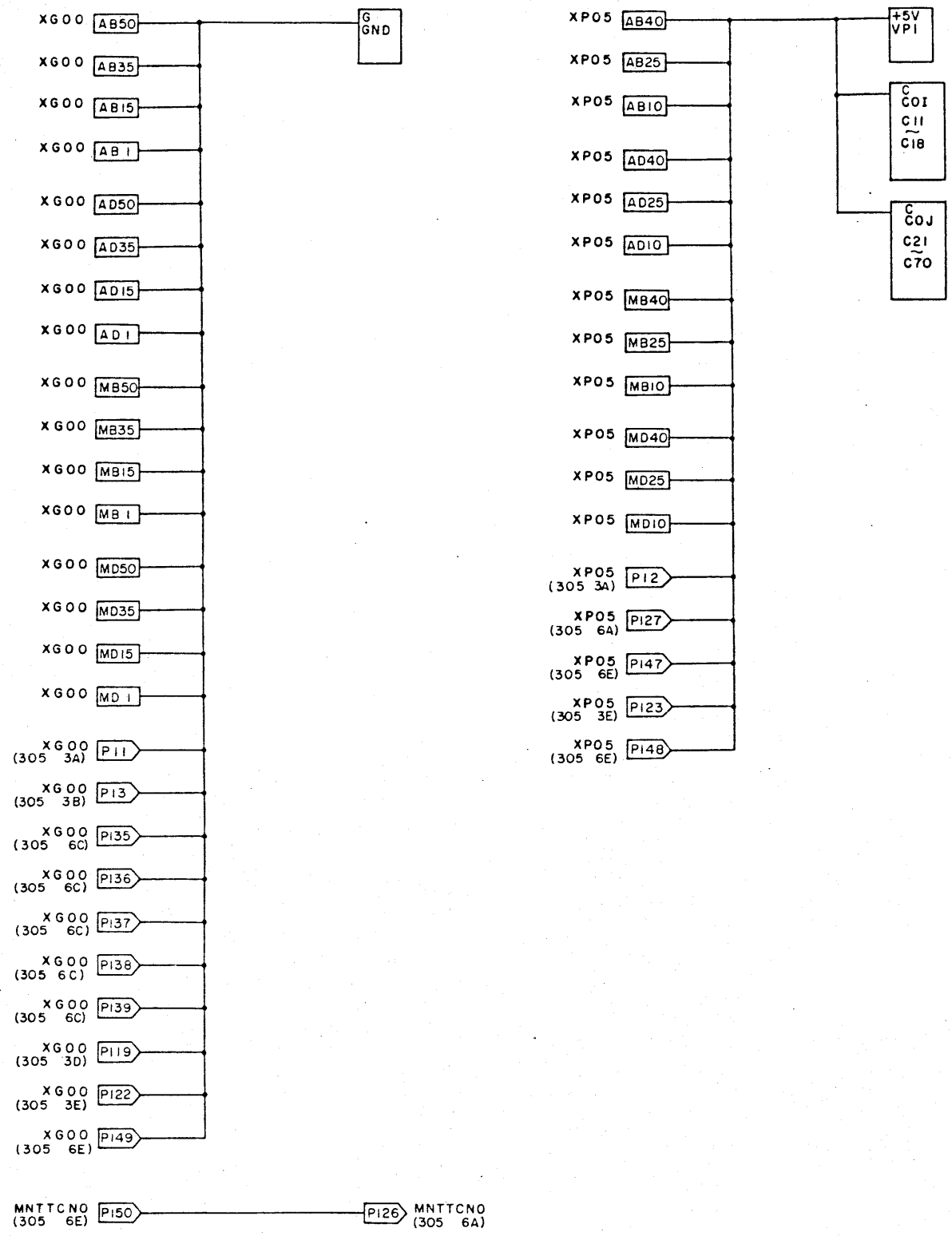
DWG ABBR	MNT			
PKG LOCATION				
PKG NAME	G9JBC			
278				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
			今村	
MTA 160 FMT TESTER CIRCUIT DIAGRAM 8/10				
134-110238-001-0				
NEC				SHT 8/

134-110238-001-0



REV	CGMP	DESCRIPTION (SC)	APP
1	0	55.5.5	
DWG ABBR		MNT	
PKG LOCATION			
PKG NAME		G9JBC	
		279	
NEXT SPEC			
DRAFT	ENG	CHK	APP
	羽賀		今村
ISSUE			
		MTA160 FMT TESTER CIRCUIT DIAGRAM	
			9/10
		134-110238-001-0	
NEC		SHT	9/

134-110238-001-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	55.5.5	

DWG ABBR	MNT			
PKG LOCATION				
PKG NAME	G9JBC			
280				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	羽賀		今村	
MTA160 FMT TESTER CIRCUIT DIAGRAM 10/10				
134-110238-001-0				
NEC				SHT 10/10

装置名

134-190248-0

	CHK-P1	CHK-IF1	CHK-FCT
FORMATTER ADDR	1	MB6	MD11
FORMATTER ENABLE	2	MB7	MD12
MTU ADDRESS 0	3	MB8	MD13
MTU ADDRESS 1	4	MB9	MD14
REVERSE/FORWARD	5	MB11	MD31
WRITE/READ	6	MB12	MD32
WRITE TAPE MARK	7	MB13	MD33
ERASE	8	MB14	MD34
READ THRESHOLD	9	MD14	MD36
DENSITYSELECT 1	10	MB16	MD37
DENSITYSELECT 0	11	MD16	MD38
COMMAND STROBE	12	MD17	MD16
REWIND	13	MB17	MD17
UNLOAD	14	MB18	MD18
LAST DATA	15	MB19	MD19
WRITE DATA P	16	MB20	MD20
WRITE DATA 0	17	MB21	MD21
WRITE DATA 1	18	MB22	MD22
WRITE DATA 2	19	MB23	MD23
WRITE DATA 3	20	MB24	MD24
WRITE DATA 4	21	MD26	MD26
WRITE DATA 5	22	MB26	MD27
WRITE DATA 6	23	MB27	MD28
WRITE DATA 7	24	MB28	MD29
XNU	25	MB29	
GND	26-50		

IFIFADD (2211B)
IFIFEND (2211A)
IFITADD (2211B)
IFITAID (2211A)
IFIRETD (2211F)
IFIWRTO (2211F)
IFIWTHD (2211E)
IFIERSD (2211E)
IFIRTHD (2211D)
IFIDNID (2211D)
IFIDNOD (2211D)
IFIGOOD (2211F)
IFIREWD (2211G)
IFIULDD (2211H)
IFILWDD (2211A)
IFIWDPO (2221A)
IFIWDDO (2221B)
IFIWDID (2221B)
IFIWD20 (2221B)
IFIWD30 (2221C)
IFIWD40 (2221C)
IFIWD50 (2221D)
IFIWD60 (2221D)
IFIWD70 (2221D)
XNU
XGDD

DCTFPTO (2069F)
DCTDSID (2069A)
DCTONLO (2069E)
DCTRDYD (2069E)
DCTRWDD (2069E)
DCTBOTO (2069F)
DCTEOTO (2069F)
FCTFBYD (2269F)
FCTDBYD (2269H)
FCTTMDO (2269B)
FCTHERD (2269E)
FCTDERD (2269B)
FCTDSRD (2269D)
FCTCRJO (2269D)
FCTRSBD (2326C)
FCTWSBD (2326B)
FCTRDPD (2317A)
FCTRDOD (2317B)
FCTRDID (2317B)
FCTRD20 (2317B)
FCTRD30 (2317C)
FCTRD40 (2317E)
FCTRD50 (2317F)
FCTRD60 (2317F)
FCTRD70 (2317F)
DCTDSDD (2069A)
XGDD

	CHK	CHK-IF1	CHK-P2
DCT AD30	AD30	AD30	1
AD32	AD32	AD32	2
AD33	AD33	AD33	3
AD34	AD34	AD34	4
AD36	AD36	AD36	5
AB36	AD37	AD37	6
AD37	AD38	AD38	7
FCT AD28	AB28	AB28	8
AD29	AB29	AB29	9
AD30	AB30	AB30	10
AD31	AB31	AB31	11
AD32	AB32	AB32	12
AD33	AB33	AB33	13
AD34	AB34	AB34	14
AD36	AB36	AB36	15
AD37	AB37	AB37	16
AD38	AB38	AB38	17
AD39	AB39	AB39	18
AD41	AB41	AB41	19
AD42	AB42	AB42	20
AD43	AB43	AB43	21
AD44	AB44	AB44	22
AD46	AB45	AB45	23
AB46	AB46	AB46	24
AD47	AB47	AB47	25
DCT AD31	AD31	AD31	26
			27-50

FILE PROTECT
DENSITY STATUS 1
ONLINE
READY
REWINDING
BEGINNING OF TAPE
END OF TAPE
FORMATTER BUSY
DATA BUSY
TAPE MARK DETECT
HARD ERROR
DATA ERROR
DENSITY ERROR
COMMAND REJECT
READ STROBE
WRITE STROBE
READ DATA P
READ DATA 0
READ DATA 1
READ DATA 2
READ DATA 3
READ DATA 4
READ DATA 5
READ DATA 6
READ DATA 7
DENSITY STATUS 0
GND

REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	

301

DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	51.6.16

MTA162 FORMATTER
CABLE CONNECTION
DIAGRAM

134-190248-0

NEC	SHT 1/3
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134-190248-0

CHK	CHK-IF1	CHK-P5
FCT MD41	MD41	1
DCT MD48	MB31	2
MD47	MB32	3
MD46	MB33	4
MD44	MB36	5
FCT MD43	MD43	6
MD44	MD44	7
MD45	MD45	8
MD47	MD47	9
MD48	MD48	10
MD49	MD49	11
MB41	MB41	12
MB43	MB43	13
MB44	MB44	14
MB46	MB46	15
MB48	MB48	16
AD2	AB2	17
AD3	AB3	18
AD4	AB4	19
AD6	AB6	20
AD7	AB7	21
AD8	AB8	22
AD9	AB9	23
MB47	MB47	24
DCT AD49	AD49	25

FORMATTER OPERATIONAL IN. XNU
 LOADED
 LAST COMMAND WRITE
 HIGH SPEED
 RECORDING CAPABILITY
 BURST DETECT
 TIME OUT
 TAPE MARK ERROR
 TAPE SLIP
 BURST ERROR
 NOISE IN ERASE
 DATA ERROR 0
 DATA ERROR 2
 DATA ERROR 3
 DATA ERROR 4
 DATA ERROR 5
 0-CHANNEL ERROR
 1-CHANNEL ERROR
 2-CHANNEL ERROR
 3-CHANNEL ERROR
 5-CHANNEL ERROR
 6-CHANNEL ERROR
 7-CHANNEL ERROR
 P-CHANNEL ERROR
 SERVICE CLOCK

FCT FAD (222 7H)
 XG00
 DCT RC10 (206 9H)
 DCT RC20 (206 9H)
 XG00
 DCT ALMO (208 6E)
 FCT BDT (226 9B)
 XG00
 DCT MBTO (208 9H)
 XG00
 FCT DE10 (226 5F)
 XG00
 FCT NWE (222 7H)
 XG00
 FCT DE60 (226 5H)
 XG00
 FCT THRO (222 7H)
 XG00
 FCT CE40 (226 5E)
 XG00
 FCT RAMD (222 7F)
 FCT ROMD (222 7F)
 XNU
 XG00

CHK-IF1	CHK-P5
MD42	26
MD42	27
	28
DCT MD45	29
MD43	30
	31
MD42	32
FCT MD46	33
	34
DCT MD41	35
	36
FCT MD42	37
	38
FCT AB2	39
	40
MB49	41
	42
AB3	43
	44
AD5	45
	46
AB4	47
AB6	48
	49
	50

GCR FORMATTER CONNECT
 FORMATTER ACTIVE
 GND
 RECORDING CAPABILITY 1
 RECORDING CAPABILITY 2
 GND
 DEVICE FAULT
 BAD TAPE
 GND
 MULTIPLE BDT
 GND
 DATA ERROR 1
 GND
 CONTROL %W ERROR
 GND
 DATA ERROR 6
 GND
 TIMER ERROR
 GND
 4-CHANNEL ERROR
 GND
 RAM ERROR
 ROM ERROR
 XNU
 GND

REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	
302			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	大橋		今村
MTA162 FORMATTER CABLE CONNECTION DIAGRAM			
134-190248-0			
NEC			SHT 2/

134-190248-0

CHK DCT P3	MTU IFC P1		MTU IFC P2	CHK DCT P4
XGDD	1~25	GND	1~25	XGDD
DCTWD70 (205 7D)	26	WRITE DATA 7	26	IFCRDYD (208 6A)
DCTWD60 (205 7D)	27	WRITE DATA 6	27	IFCDLED (208 1A)
DCTWD50 (205 7C)	28	WRITE DATA 5	28	XNU
DCTWD40 (205 7C)	29	WRITE DATA 4	29	XNU
DCTWD30 (205 7B)	30	WRITE DATA 3	30	IFCOPID (208 6A)
DCTWD20 (205 7A)	31	WRITE DATA 2	31	IFCRWGD (208 1H)
DCTWD10 (205 7A)	32	WRITE DATA 1	32	IFCEOTO (208 1B)
DCTWDD0 (205 7A)	33	WRITE DATA 0	33	IFCBOTO (208 1C)
DCTWDPO (205 7E)	34	WRITE DATA P	34	IFCWPMO (208 1G)
XP05 (214 6C)	35	+5V	35	IFCDDSD (208 1B)
XP05 (214 6C)	36	+5V	36	IFCLCWD (208 1F)
	37	XNU	37	XNU
DCTDY00 (203 6A)	38	DEVICE SELECT 0	38	IFCLDDO (208 1F)
DCTDV10 (203 6A)	39	DEVICE SELECT 1	39	IFCRD70 (208 6F)
DCTDY20 (203 6B)	40	DEVICE SELECT 2	40	IFCRD60 (208 6F)
DCTDV30 (203 6B)	41	DEVICE SELECT 3	41	IFCRD50 (208 6E)
DCTFWDD (204 4B)	42	FORWARD RUN	42	IFCRD40 (208 6E)
DCTRVS0 (204 9B)	43	REVERSE RUN	43	IFCRD30 (208 6D)
DCTRWDD (204 9A)	44	REWIND	44	IFCRD20 (208 6C)
DCTULDO (204 9A)	45	UNLOAD	45	IFCRD10 (208 6C)
DCTWTGD (204 9C)	46	WRITE GATE	46	IFCRD00 (208 6B)
DCTLTHD (204 9D)	47	LOW THRESHOLD	47	IFCRDPO (208 6G)
DCTLDND (204 9D)	48	LOW DENSITY	48	IFCDSWD (206 1H)
	49	XNU	49	IFCDNRO (206 1F)
DCTWSBD (204 9E)	50	WRITE STROBE	50	XNU

REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	
303			
NEXT SPEC			
DRAFT	ENG	CHK	APP
	大橋		今村
MTA162 FORMATTER CABLE CONNECTION DIAGRAM			
134-190248-0			
NEC			SHT 3/3

1 2 3 4 ▲ 5 6 7

134-190247-0

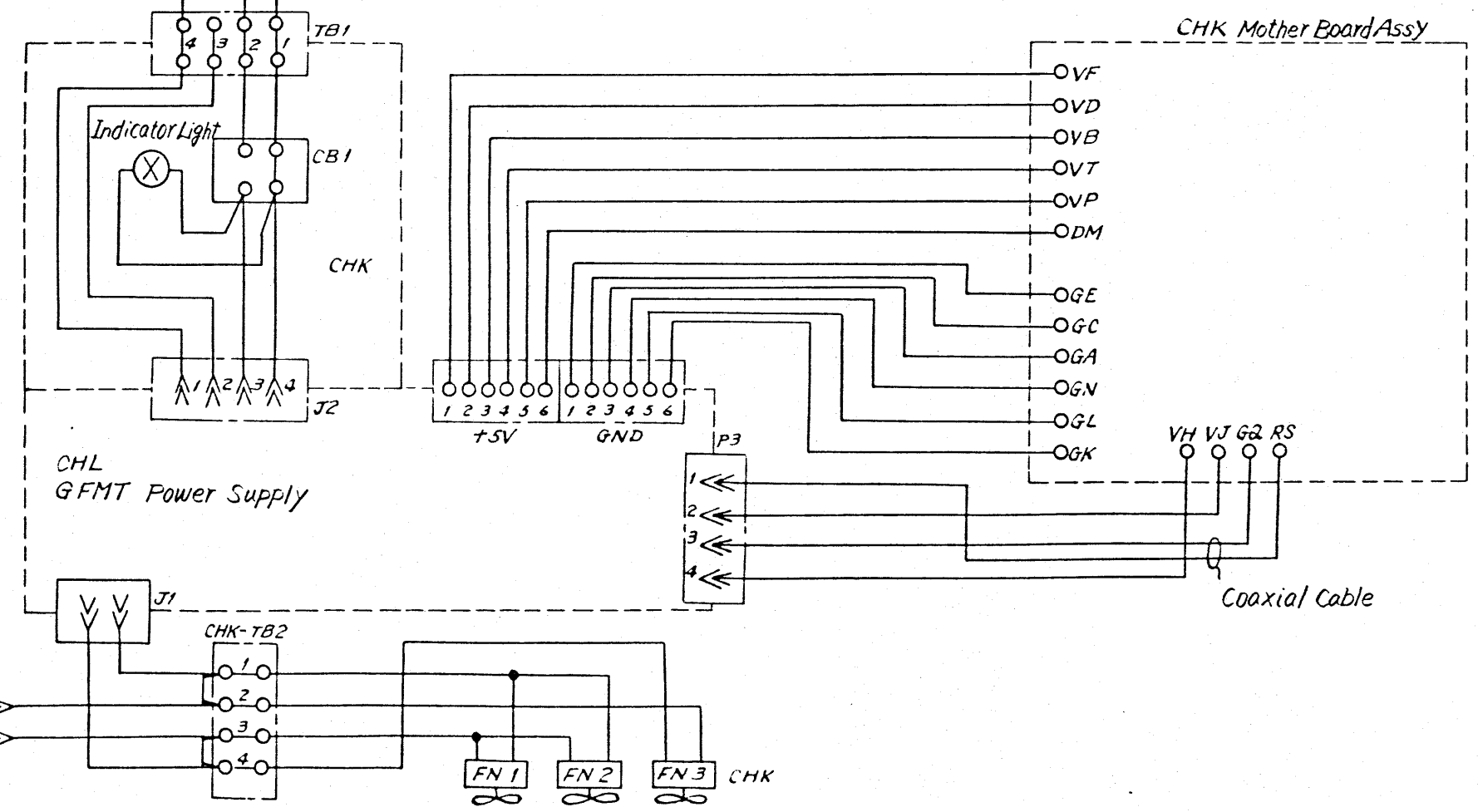
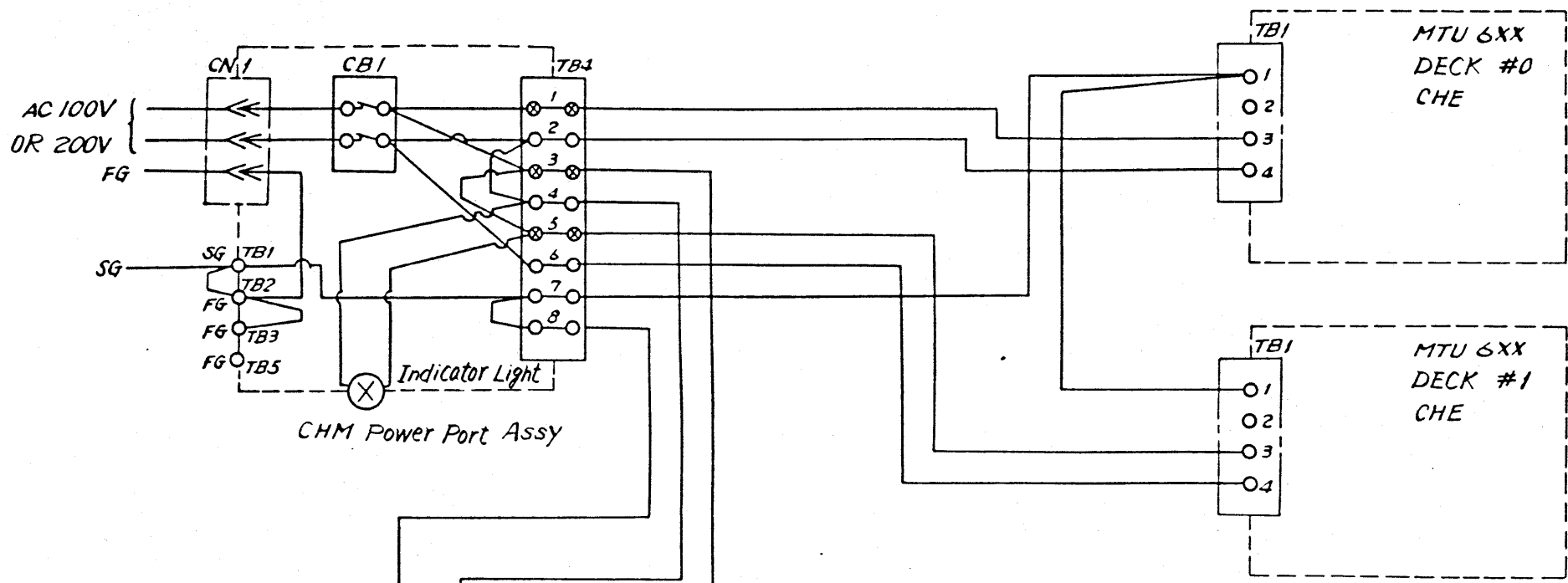
B

C

D

E

置名



REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	大橋		今村	57 8 15

MTA162 FORMATTER
CABLE CONNECTION OF
POWER SUPPLY

134-190247-0

NEC SHT 1/2

A

B

C

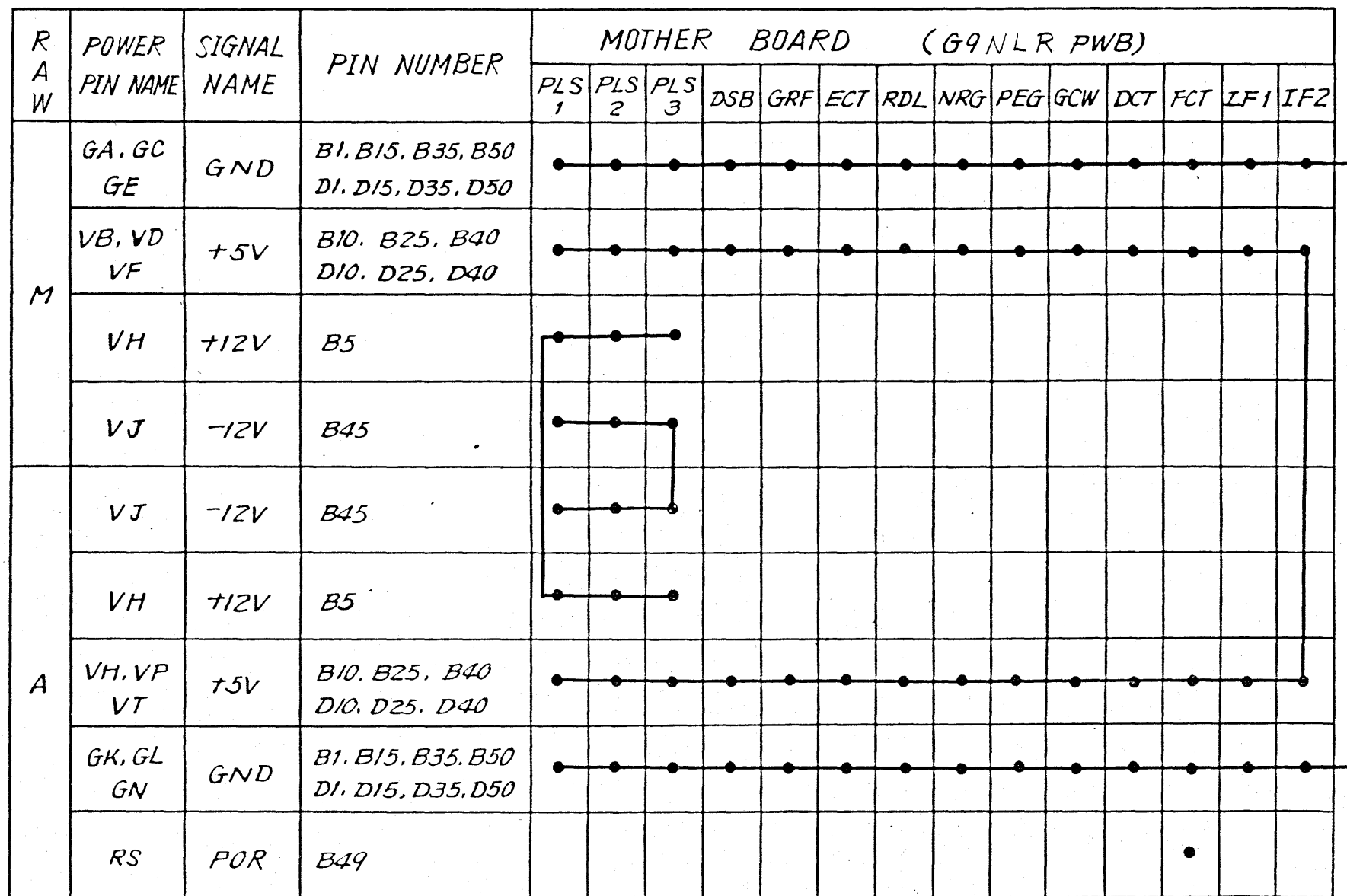
A

D

E

2 3 4 ▼ 5 6

134-190247-0



Detailed diagram of supplying the power to the mother board.

REV	COMP	DESCRIPTION(SC)	APP
1	0	1980.5.1	—
NEXT SPEC			
DRAFT	ENG	CHK	APP
	大橋		今村
MTA162 FORMATTER CABLE CONNECTION			
134-190247-0			
NEC			SHT 2/2