INTELLIGENT PERIPHERAL DEVICES (IPD) DATA BOOK

NEC

NEC Electronics Inc.

NEC

Intelligent Peripheral Devices [IPD]

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SELECTION GUIDES

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Section 1
Selection Guides

Part Numbering System

μPD72001L	Typical microdevice part number
μP	NEC monolithic silicon integrated circuit
D	Device type (D = digital MOS)
72001	Device identifier (alphanumeric)
L	Package type (L = PLCC)

A part number may include an alphanumeric suffix that identifies special device characteristics; for example, μPD72001L-11 has an 11-MHz data clock rating.

4-Bit, Single-Chip CMOS Microcomputers

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X4)	I/O	# Package	Pins
7502	LCD controller/driver	0.4	2.5 to 6.0	2K	128	23	Miniflat	64
7503	LCD controller/driver	0.4	2.5 to 6.0	4K	224	23	Miniflat	64
7507	General-purpose	0.4	2.7 to 6.0	2K	128	32	DIP SDIP Miniflat	40 40 52
7508	General-purpose	0.4	2.7 to 6.0	4K	224	32	DIP SDIP Miniflat	40 40 52
75CG08	Piggyback EPROM	0.4	4.5 to 5.5	2K or 4K	224	32	Ceramic DIP	40
7514	LCD controller/driver	0.5	2.7 to 6.0	4K	256	31	Miniflat	80
7527A	FIP controller/driver	0.6	2.7 to 6.0	2K	128	35	DIP SDIP	42 42
7528A	FIP controller/driver	0.6	2.7 to 6.0	4K	160	35	DIP SDIP	42 42
75CG28	Piggyback EPROM; FIP controller/driver	0.5	4.5 to 5.5	4K	160	35	Ceramic DIP	42
7533	A/D converter	0.5	2.7 to 6.0	4K	160	30	DIP SDIP Miniflat	42 42 44
75CG33	Piggyback EPROM; A/D converter	0.5	4.5 to 5.5	4K	160	30	Ceramic DIP	42
7537A	FIP controller/driver	0.6	2.7 to 6.0	2K	128	35	DIP SDIP	42 42
7538A	FIP controller/driver	0.6	2.7 to 6.0	4K	160	35	DIP SDIP	42 42
75CG38	Piggyback EPROM; FIP controller/driver	0.5	4.5 to 5.5	4K	160	35	Ceramic DIP	42
7554	Serial I/O; external clock or RC oscillator	0.7	2.7 to 6.0	1K	64	16	SDIP SOP	20 20
75P54	Serial I/O; external clock or RC oscillator	0.7	4.5 to 6.0	1K OTPROM	64	16	SDIP SOP	20 20
7564	Serial I/O; ceramic oscillator	0.7	2.7 to 6.0	1K	64	16	SDIP SOP	20 20
75P64	Serial I/O; ceramic oscillator	0.7	4.5 to 6.0	1K OTPROM	64	16	SDIP SOP	20 20
7556	Comparator; external clock or RC oscillator	0.7	2.7 to 6.0	1K	64	20	SDIP SOP	24 24
75P56	Comparator; external clock or RC oscillator	0.7	4.5 to 6.0	1K OTPROM	64	20	SDIP SOP	24 24
7566	Comparator; ceramic oscillator	0.7	2.7 to 6.0	1K	64	19	SDIP SOP	24 24
75P66	Comparator; ceramic oscillator	0.7	4.5 to 6.0	1K OTPROM	64	19	SDIP SOP	24 24
75004	General-purpose	4.19	2.7 to 6.0	4K	512	34	SDIP Miniflat	42 44

Plastic unless ceramic (or cerdip) is specified.
* Under development; consult Microcontroller Marketing for availability.

4-Bit, Single-Chip CMOS Microcomputers (cont)

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X4)	I/O	# Package	Pins
75006	General-purpose	4.19	2.7 to 6.0	6K	512	34	SDIP Miniflat	42 44
75008	General-purpose	4.19	2.7 to 6.0	8K	512	34	SDIP Miniflat	42 44
75P008	General-purpose	4.19	4.5 to 5.5	8K OTPROM	512	34	SDIP Miniflat	42 44
75028 *	A/D converter	4.19	2.7 to 6.0	8K	512	40	SDIP Miniflat	64 64
75P028 *	A/D converter	4.19	4.5 to 6.0	8K	512	40	SDIP Miniflat	64 64
75048 *	A/D converter; 0.5K EEPROM	4.19	2.7 to 6.0	8K	512	40	SDIP Miniflat	64 64
75104	High-end with 8-bit instruction	4.19	2.7 to 6.0	4096	320	58	SDIP Miniflat	64 64
75106	High-end with 8-bit instruction	4.19	2.7 to 6.0	6016	320	58	SDIP Miniflat	64 64
75108	High-end with 8-bit instruction	4.19	2.7 to 6.0	8064	512	58	SDIP Miniflat	64 64
75P108	High-end with 8-bit instruction; on-chip OTPROM or UVEPROM	4.19	4.5 to 5.5	8064	512	58	DIP Miniflat Shrink cerdip	64 64 64
75112	High-end with 8-bit instruction	4.19	2.7 to 6.0	12,032	512	58	SDIP Miniflat	64 64
75116	High-end with 8-bit instruction	4.19	2.7 to 6.0	16,128	512	58	SDIP Miniflat	64 64
75P116	High-end with 8-bit instruction	4.19	4.5 to 5.5	16,128 OTPROM	512	58	DIP Miniflat	64 64
75206	FIP controller/driver	4.19	2.7 to 6.0	6016	369	32	SDIP Miniflat	64 64
75208	FIP controller/driver	4.19	2.7 to 6.0	8064	497	32	SDIP Miniflat	64 64
75CG208	FIP controller/driver; piggyback EPROM	4.19	4.5 to 5.5	8064	512	32	Ceramic SDIP Ceramic flatpack	64 64
75212A	FIP controller/driver	4.19	2.7 to 6.0	12,160	512	32	SDIP Miniflat	64 64
75216A	FIP controller/driver	4.19	2.7 to 6.0	16,256	512	32	SDIP Miniflat	64 64
75CG216A	FIP controller/driver; piggyback EPROM	4.19	4.5 to 5.5	16,256	512	32	Ceramic SDIP Ceramic miniflat	64 64
75P216A *	FIP controller/driver	4.19	4.5 to 5.5	16,256 OTPROM	512	32	SDIP	64
75268 *	FIP controller/driver	4.19	2.7 to 6.0	8064	512	20	SDIP Flatpack	64 64
75304	LCD controller/driver	4.19	2.7 to 6.0	4K	512	68	Miniflat	80
75306	LCD controller/driver	4.19	2.7 to 6.0	6K	512	68	Miniflat	80
75308	LCD controller/driver	4.19	2.7 to 6.0	8K	512	68	Miniflat	80
75P308	LCD controller/driver; on-chip OTPROM or UVEPROM	4.19	4.5 to 5.5	8K	512	68	Miniflat Ceramic LCC	80 80
75312	LCD controller/driver	4.19	2.7 to 6.0	12K	512	68	Miniflat	80

4-Bit, Single-Chip CMOS Microcomputers (cont)

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X4)	I/O	# Package	Pins
75316	LCD controller/driver	4.19	2.7 to 6.0	16K	512	68	Miniflat	80
75P316A *	LCD controller/driver; on-chip OTPROM or UVEPROM	4.19	2.7 to 6.0	16K	512	68	Miniflat Ceramic LCC	80 80
75328	LCD controller/driver; A/D converter	4.19	2.7 to 6.0	8064	512	24	Miniflat	80
75P328	LCD controller/driver; A/D converter	4.19	4.5 to 5.5	8064 OTPROM	512	24	Miniflat	80
75402	Low-end	4.19	2.7 to 6.0	1920	64	22	DIP SDIP Miniflat	28 28 44
75P402	Low-end	4.19	4.5 to 5.5	1920 OTPROM	64	22	DIP SDIP Miniflat	28 28 44
75516	High-end; A/D converter	4.19	2.7 to 6.0	16K	512	68	Miniflat	80
75P516	High-end; A/D converter	4.19	4.5 to 5.5	16K OTPROM	512	68	Miniflat LCC	80 80

8-Bit, Single-Chip NMOS/CMOS Microcomputers

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	# Package	Pins
7810H	NMOS; A/D converter	15	4.5 to 5.5	External	256	32	SDIP QUIP	64 64
7811H	NMOS; A/D converter	15	4.5 to 5.5	4K	256	44	SDIP QUIP	64 64
78PG11H	NMOS; A/D converter piggyback EPROM	15	4.5 to 5.5	4K	256	44	Ceramic QUIP	64
78C10/78C10A	CMOS; A/D converter	15	4.5 to 5.5	External	256	32	QUIP SDIP Miniflat PLCC	64 64 64 68
78C11/78C11A	CMOS; A/D converter	15	4.5 to 5.5	4K	256	44	QUIP SDIP Miniflat PLCC	64 64 64 68
78C12A	CMOS; A/D converter	15	4.5 to 5.5	8K	256	44	QUIP SDIP Miniflat PLCC	64 64 64 68
78C14	CMOS; A/D converter	15	4.5 to 5.5	16K	256	44	QUIP SDIP Miniflat PLCC	64 64 64 68
78CP14	CMOS; A/D converter	15	4.5 to 5.5	16K OTPROM	256	44	QUIP SDIP Miniflat PLCC	64 64 64 68
				16K UVEPROM	256	44	Ceramic QUIP Shrink cerdip	64 64

8-Bit, Single-Chip NMOS/CMOS Microcomputers (cont)

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	# Package	Pins
78213	CMOS; A/D converter; advanced peripherals	12	4.5 to 5.5	External	512	54	SDIP	64
							QUIP	64
							Miniflat	74
							PLCC	68
78214	CMOS; A/D converter; advanced peripherals	12	4.5 to 5.5	16K	512	54	SDIP	64
							QUIP	64
							Miniflat	74
							PLCC	68
78P214	CMOS; A/D converter; advanced peripherals	12	4.5 to 5.5	16K OTPROM	512	54	SDIP	64
							QUIP	64
							Miniflat	74
							PLCC	68
				16K UVEPROM	512	54	Shrink cerdip	64
							Ceramic QUIP	64
78220	CMOS; analog comparator; large I/O	12	4.5 to 5.5	External	640	71	PLCC	84
							Miniflat	94
78224	CMOS; analog comparator; large I/O	12	4.5 to 5.5	16K	640	71	PLCC	84
							Miniflat	94
78P224	CMOS; analog comparator; large I/O	12	4.5 to 5.5	16K OTPROM	640	71	PLCC	84
							Miniflat	94
78233 *	CMOS; real-time outputs; A/D and D/A converters	12	4.5 to 5.5	External	640	54	Miniflat	80
							Miniflat	94
							PLCC	84
78234 *	CMOS; real-time outputs; A/D and D/A converters	12	4.5 to 5.5	16K	640	54	Miniflat	80
							Miniflat	94
							PLCC	84
78P234 *	CMOS; real-time outputs; A/D and D/A converters	12	4.5 to 5.5	16K OTPROM	640	54	Miniflat	80
							Miniflat	94
							PLCC	84

16-Bit, Single-Chip CMOS Microcomputers

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	# Package	Pins
78310A	Real-time motor control	12	4.5 to 5.5	External	256	48	SDIP	64
							QUIP	64
							Miniflat	64
							PLCC	68
78312A	Real-time motor control	12	4.5 to 5.5	8K	256	48	SDIP	64
							QUIP	64
							Miniflat	64
							PLCC	68
78P312A	Real-time motor control	12	4.5 to 5.5	8K UVEPROM	256	48	Shrink cerdip	64
							Ceramic QUIP	64
				8K OTPROM	256	48	SDIP	64
							QUIP	64
							PLCC	68
78320	High-end; advanced analog and digital peripherals	16	4.5 to 5.5	External	640	55	Miniflat	64
							PLCC	68
78322	High-end; advanced analog and digital peripherals	16	4.5 to 5.5	16K	640	55	Miniflat	64
							PLCC	68

16-Bit, Single-Chip CMOS Microcomputers (cont)

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	# Package	Pins
78P322	High-end; advanced analog and digital peripherals	16	4.5 to 5.5	16K OTPROM	640	55	PLCC	68
71P301	Port and memory extender used with 7832X microcomputer family; UVEPROM or OTPROM	–	4.5 to 5.5	16K	1K	16	PLCC Miniflat Ceramic QUIP	44 64 64

8-Bit, Single-Chip Microcomputers

Device, μPD	Features	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	# Package	Pins
8035HL	HMOS	6	4.5 to 5.5	External	64	27	DIP	40
8039HL	HMOS	11	4.5 to 5.5	External	128	27	DIP	40
80C39H	CMOS	12	2.5 to 6.0	External	128	27	DIP Miniflat	40 44
80C40H	CMOS	12	2.5 to 6.0	External	256	27	DIP	40
8041AH	NMOS; universal PPI	11	4.5 to 5.5	1K	64	18	DIP	40
80C42	CMOS; universal PPI	12	4.5 to 5.5	2K	128	18	DIP Miniflat	40 44
8048H	HMOS	6	4.5 to 5.5	1K	64	27	DIP	40
8049H	HMOS	11	4.5 to 5.5	2K	128	27	DIP	40
80C49H	CMOS	12	2.5 to 6.0	2K	128	27	DIP	40
49H	CMOS	12	2.5 to 6.0	2K	128	27	Miniflat	44
80C50H	CMOS	12	2.5 to 6.0	4K	256	27	DIP	40
50H	CMOS	12	2.5 to 6.0	4K	256	27	Miniflat	44
8741A	NMOS; universal PPI; UVEPROM	6	4.5 to 5.5	1K	64	18	Cerdip	40
8748H	NMOS; OTPROM or UVEPROM	11	4.5 to 5.5	1K	64	27	DIP Cerdip	40 40
8749H	HMOS; OTPROM or UVEPROM	11	4.5 to 5.5	2K	128	27	DIP Cerdip	40 40

CMOS Microprocessors

Device, μPD	Features	Data Bits	Clock (MHz)	# Package	Pins
70008A	*Z80 microprocessor	8	8	DIP	40
				Miniflat	44
				PLCC	44
70108 (V20)	8088 compatible; enhanced	8/16	8 or 10	DIP	40
				Ceramic DIP	40
				Miniflat	52
				PLCC	44
70116 (V30)	8086 compatible; enhanced	16	8 or 10	DIP	40
				Ceramic DIP	40
				Miniflat	52
				PLCC	44
70208 (V40)	MS-DOS, V20 compatible CPU with peripherals	8/16	8 or 10	Ceramic PGA	68
				PLCC	68
				Miniflat	80
70216 (V50)	MS-DOS, V30 compatible CPU with peripherals	16/16	8 or 10	PGA	68
				PLCC	68
				Miniflat	80
70616 (V60)	32-bit; high-speed	16/32	16	PGA	68
70632 (V70)	32-bit; high-speed	32/32	20/25	PGA	132
70832 (V80)	32-bit; high-speed	32/32	25	Ceramic PGA	208
70136 (V33)	Hardwired, enhanced V30	16	12 or 16	PGA	68
				PLCC	68
70236 (V53)	V33 core-based; high-integration; DMA, serial I/O, interrupt controller, etc.	16	–	Ceramic PGA	132
70320 (V25)	MS-DOS compatible; high-integration; DMA, serial I/O, interrupt controller, etc.	8/16	5 or 8	PLCC	84
				Miniflat	94
70330 (V35)	MS-DOS compatible; high-integration; DMA, serial I/O, interrupt controller, etc.	16	8	PLCC	84
				Miniflat	94
70325 (V25+)	MS-DOS compatible; high-integration; high-speed DMA	8/16	8 or 10	PLCC	84
				Miniflat	94
70335 (V35+)	MS-DOS compatible; high-integration; high-speed DMA	16	8 or 10	PLCC	84
				Miniflat	94
70327 (V25 Software Guard)	MS-DOS compatible; high-integration; software protection	8/16	8	PLCC	84
				Miniflat	94
70337 (V35 Software Guard)	MS-DOS compatible; high-integration; software protection	16	8	PLCC	84
				Miniflat	94
79011 (V25 RTOS)	MS-DOS compatible; high-integration; real-time operating system	8/16	8	PLCC	84
				Miniflat	94
79021 (V35 RTOS)	MS-DOS compatible; high-integration; real-time operating system	16	8	PLCC	84
				Miniflat	94
70322 (V25 ROM)	MS-DOS compatible; high-integration; 16K-byte ROM	8/16	8	PLCC	84

Plastic unless ceramic (or cerdip) is specified.
* For additional information, refer to 1987 Microcomputer Data Book.

CMOS Microprocessors (cont)

Device, μPD	Features	Data Bits	Clock (MHz)	# Package	Pins
70P322	MS-DOS compatible; high-integration; 16K-byte UVEPROM; V25 or V35 mode	8/16	8	Ceramic LCC	84
70332 (V35 ROM)	MS-DOS compatible; high-integration; 16K-byte ROM	16	8	PLCC	84

NMOS and HMOS Microprocessors

Device, μPD	Features	Data Bits	Clock (MHz)	# Package	Pins
8085A	*8-bit microprocessor; NMOS or HMOS	8	5	DIP	40
8086	*16-bit microprocessor; HMOS	16	8	Cerdip	40
8088	*8-bit microprocessor; HMOS	8	8	Ceramic DIP	40

CMOS System Support Products

Device, μPD	Name	Data Bits	Clock (MHz)	# Package	Pins
71011	Clock Pulse Generator/Driver	–	20	DIP	18
				SOP	20
71037	Programmable DMA Controller	8	10	DIP	40
				Miniflat	40
				PLCC	44
71051	Serial Control Unit	8	8/10	DIP	28
				Miniflat	44
				PLCC	28
71054	Programmable Timer/Controller	8	8/10	DIP	24
				Miniflat	44
				PLCC	28
71055	Parallel Interface Unit	8	8/10	DIP	40
				Miniflat	44
				PLCC	44
71059	Interrupt Control Unit	8	8/10	DIP	28
				Miniflat	44
				PLCC	28
71071	DMA Controller	8/16	8/10	DIP	48
				Ceramic DIP	48
				Miniflat	52
				PLCC	52
71082	Transparent Latch	8	8	DIP	20
				SOP	20
71083	Transparent Latch	8	8	DIP	20
				SOP	20
71084	Clock Pulse Generator/Driver	–	25	DIP	18
				SOP	20
71086	Bus Buffer/Driver	8	8	DIP	18
				SOP	20
71087	Bus Buffer/Driver	8	8	DIP	20
				SOP	20

CMOS System Support Products (cont)

Device, μPD	Name	Data Bits	Clock (MHz)	# Package	Pins
71088	System Bus Controller	–	8/10	DIP	20
				SOP	20
82C43	*Input/Output Expander	–	5	DIP	24
				Skinny DIP	24

NMOS System Support Products

Device, μPD	Name	Data Bits	Clock (MHz)	# Package	Pins
8155H	*256 x 8 RAM; I/O ports and timer	8	3 or 5	DIP	40
8156H	*256 x 8 RAM; I/O ports and timer	8	3 or 5	DIP	40
8237A	*Programmable DMA Controller	8	5	DIP	40
8243	*Input/Output Expander	–	5	DIP	24
8251A	*Programmable Communications Interface	8	3/5	DIP	28
8253	*Programmable Internal Timer	8	5	DIP	24
8255A	*Programmable Peripheral Interface	8	5	DIP	40
8257	*Programmable DMA Controller	8	5	DIP	40
8259A	*Programmable Interrupt Controller	8	5	DIP	28
8279	*Programmable Keyboard/Display Interface	–	5	DIP	40

Communications Controllers

Device, μPD	Name	Description	Data Rate	# Package	Pins
7201A	Multiprotocol Serial Communications Controller	Dual full-duplex serial channels; four DMA channels; programmable interrupt vectors; asychronous COP and BOP support; NMOS	1 Mb/s	DIP Ceramic DIP	40 40
72001	CMOS, Advanced Multiprotocol Serial Communications Controller	Functional superset of 8530; 8086/V30 interface; two full-duplex serial channels; two digital phase-locked loops; two baud-rate generators per channel; loopback test mode; short frame and mark idle detection	2.2 Mb/s	DIP Miniflat PLCC	40 52 52
72002	CMOS, Advanced Multiprotocol Serial Communications Controller	Low-cost, single-channel version of 72001; software compatible; direct interface to 8237 DMA. Not included in 1989-1990 IPD Data Book; refer to 72002 data sheet.	2.2 Mb/s	DIP Miniflat PLCC	40 44 44
72101	CMOS, HDLC Controller	Single full-duplex serial channel; on-chip DMA Controller. Not included in 1989-1990 IPD Data Book; refer to 72101 data sheet	4 Mb/s	DIP PLCC	64 68

Graphics Controllers

Device, μPD	Name	Description	Drawing Rate	# Package	Pins
7220A	High-Performance Graphics Display Controller	General-purpose, high-integration controller; hardwired support for lines, arc/circles, rectangles, and graphics characters; 1024x1024 pixel display with four planes	500 ns/dot	Ceramic DIP	40
72020	Graphics Display Controller	CMOS 7220A with 2M video memory; dual-port RAM control; write-masking on any bit; enhanced external synch	500 ns/dot	DIP Miniflat	40 52
72022	Intelligent Display Processor	Display and image processing for text and sprites; three display modes; four-way horizontal split-screen display; CMOS	500 ns/dot	PLCC Miniflat	68 80
72120	Advanced Graphics Display Controller	High-speed graphics operations including paint, area fill, slant, arbitrary angle rotate, up to 16x enlargement and reduction; dual-port RAM control; CMOS	500 ns/dot	PLCC Miniflat	84 94
72123	Advanced Graphics Display Controller II	Enhanced 72120; expanded command set; improved painting performance; laser printer interface controls; CMOS	400 ns/dot	PLCC Miniflat	84 94

Advanced Compression/Expansion Engine

Device, μPD	Name	Description	# Package	Pins
72185	Advanced Compression/ Expansion Engine	High-speed CCITT Group 3/4 bit-map image compression/expansion (A4 test chart, 400 PPI x 400 LPI in under 1 second); 32K-pixel line length; 32-megabyte image memory; on-chip DMA and refresh timing generator; CMOS	SDIP PLCC	64 68

Plastic unless ceramic (or cerdip) is specified.

Floppy-Disk Controllers

Device, μPD	Name	Description	Transfer Rate	# Package	Pins
765A/B	Floppy-Disk Controller	Industry-standard controller supporting IBM 3740 and IBM System 34 double-density format; enhanced 765B supports multitasking applications	500 kb/s	DIP	40
71065/66	Floppy-Disk Interface	Compatible with 765-family controllers and others; supports multiple data rates from 125 to 500 kb/s	500 kb/s	SOP SDIP	28 30
72065/65B	CMOS Floppy-Disk Controller	100% 765A/B microcode compatible; compatible with 808x microprocessor families	1 Mb/s	DIP PLCC Miniflat	40 44 52
72067	Floppy-Disk Controller	CMOS; 765A/B microcode compatible; clock generation/ switching circuitry; selectable write precompensation; digital phase-locked loop	500 kb/s	DIP Miniflat PLCC	48 52 52
72068	Floppy-Disk Controller	All features of the 72067 plus IBM-PC, PC/XT, PC/AT, or PS/2 style registers; 24-ma high-current drivers	500 kb/s	Miniflat PLCC	80 84
72069	Floppy-Disk Controller	All features of the 72067/68 with substitution of high-performance analog phase-locked loop for digital PLL	1 Mb/s	PLCC Miniflat	84 100

Hard-Disk Controllers

Device, μPD	Name	Description	Read/Write Clock	# Package	Pins
7261A/B	Hard-Disk Controller	Supports eight drives in SMD mode, four drives in ST506 mode; error correction and detection	23 MHz	Ceramic DIP	40
7262	Enhanced Small-Disk Interface (ESDI) Controller	Serial-mode ESDI compatible; controls up to seven drives; supports up to 80 heads; hard and soft-sector interfacing	18 MHz	Ceramic DIP	40
72061	CMOS Hard-Disk Controller	Supports SMD/SMD-E and ST506/412 type drives	24 MHz	DIP Miniflat PLCC	40 52 52
72111	Small Computer System Interface (SCSI) Controller	Selectable 8/16 data bus width; 16 high-level commands for reduced CPU load; single-command automatic execution; 4-Mb sync/async; CMOS	16 MHz	SDIP Miniflat PLCC	64 74 68

Digital Signal Processors

Device, μPD	Description	Instruction Cycle (ns)	Instruction ROM (Bits)	Data ROM (Bits)	Data RAM (Bits)	# Package	Pins
7720A	16-bit, fixed-point DSP; NMOS	244	512 x 23	510 x 13	128 x 16	DIP PLCC	28 44
77C20A	16-bit, fixed-point DSP; CMOS	244	512 x 23	510 x 13	128 x 16	DIP PLCC PLCC	28 28 44
77P20	16-bit, fixed-point DSP; CMOS	244	512 x 23 UVEPROM	510 x 13 UVEPROM	128 x 16	Cerdip	28
77C25	16-bit, fixed-point DSP; CMOS	122	2048 x 24	1024 x 16	256 x 16	DIP PLCC	28 44
77P25	16-bit, fixed-point DSP; CMOS	122	2048 x 24 OTPROM	1024 x 16 OTPROM	256 x 16	DIP PLCC	28 44
			2048 x 24 UVEPROM	1024 x 16 UVEPROM	256 x 16	Cerdip	28
77220	24-bit, fixed-point DSP; CMOS	122	2048 x 32	1024 x 24	512 x 24	Ceramic PGA PLCC	68 68
77230AR	32-bit, floating-point DSP; CMOS	150	2048 x 32	1024 x 32	1024 x 32	Ceramic PGA	68
77230AR-003	32-bit, floating-point DSP; CMOS; standard library software	150	n/a	n/a	n/a	Ceramic PGA	68
77P230R	32-bit, floating-point DSP; CMOS	150	2048 x 32 UVEPROM	1024 x 32 UVEPROM	1024 x 32	Ceramic PGA	68
77810	16-bit fixed-point modem DSP; CMOS	181	2048 x 24	1024 x 16	256 x 16	Ceramic PGA PLCC	68 68
7281	Image pipelined processor; NMOS	5-MHz clock	n/a	n/a	512 x 18	Ceramic DIP	40
9305	Support device for μPD7281 processors; CMOS	10-MHz clock	n/a	n/a	n/a	Ceramic PGA	132

Speech Processors

Device, μPD	Name	Technology	Clock (MHz)	Data ROM (Bits)	# Package	Pins
7730	ADPCM Speech Encoder/Decoder	NMOS	8	–	DIP	28
77C30	ADPCM Speech Encoder/Decoder	NMOS	8	–	DIP PLCC	28 44
7755	ADPCM Speech Synthesizer	CMOS	0.7	96K	DIP SOP	18 24
7756	ADPCM Speech Synthesizer	CMOS	0.7	256K	DIP SOP	18 24
77P56	ADPCM Speech Synthesizer	CMOS	0.7	256K OTPROM	DIP SOP	20 24
7757	ADPCM Speech Synthesizer	CMOS	0.7	512K	DIP SOP	18 24
7759	ADPCM Speech Synthesizer	CMOS	0.7	1024K external	DIP Miniflat	40 52

Plastic unless ceramic (or cerdip) is specified.

V-Series Development Tools Selection Guide

Part Number (Note 1)	Full Emulator	Full Emulator Probe	Mini-IE Emulator	Mini-IE Probe	Evaluation Boards	EPROM/OTP Device	Relocatable Assembler (Note 13)	C Compiler (Note 14)
μPD70136GJ-12	IE-70136-A016	EP-70136L-A (Note 2)	IE-70136-PC	EP-70136L-PC (Note 2)	DDK-70136	–	RA70136	CC70136
μPD70136GJ-16	IE-70136-A016	EP-70136L-A (Note 2)	IE-70136-PC	EP-70136L-PC (Note 2)	DDK-70136	–	RA70136	CC70136
μPD70136L-16	IE-70136-A016	EP-70136L-A	IE-70136-PC	EP-70136L-PC	DDK-70136	–	RA70136	CC70136
μPD70136L-12	IE-70136-A016	EP-70136L-A	IE-70136-PC	EP-70136L-PC	DDK-70136	–	RA70136	CC70136
μPD70136R-12	IE-70136-A016	EP-70136L-A (Note 3)	IE-70136-PC	EP-70136L-PC (Note 3)	DDK-70136	–	RA70136	CC70136
μPD70136R-16	IE-70136-A016	EP-70136L-A (Note 3)	IE-70136-PC	EP-70136L-PC (Note 3)	DDK-70136	–	RA70136	CC70136
μPD70208GF-8	IE-70208-A010	(Note 12)	EB-V40MINI-IE	–	EB-70208	–	RA70116	CC70116
μPD70208GF-10	IE-70208-A010	(Note 12)	EB-V40MINI-IE	–	EB-70208	–	RA70116	CC70116
μPD70208L-8	IE-70208-A010	IE-70000-2958	EB-V40MINI-IE	ADAPT68PGA 68PLCC (Note 4)	EB-70208	–	RA70116	CC70116
μPD70208L-10	IE-70208-A010	IE-70000-2958	EB-V40MINI-IE	ADAPT68PGA 68PLCC (Note 4)	EB-70208	–	RA70116	CC70116
μPD70208R-8	IE-70208-A010	IE-70000-2959	EB-V40MINI-IE	(Note 4)	EB-70208	–	RA70116	CC70116
μPD70208R-10	IE-70208-A010	IE-70000-2959	EB-V40MINI-IE	(Note 4)	EB-70208	–	RA70116	CC70116
μPD70216GF-8	IE-70216-A010	(Note 12)	EB-V50MINI-IE	–	EB70216	–	RA70116	CC70116
μPD70216GF-10	IE-70216-A010	(Note 12)	EB-V50MINI-IE	–	EB70216	–	RA70116	CC70116
μPD70216L-8	IE-70216-A010	IE-70000-2958	EB-V50MINI-IE	ADAPT68PGA 68PLCC (Note 4)	EB70216	–	RA70116	CC70116
μPD70216L-10	IE-70216-A010	IE-70000-2958	EB-V50MINI-IE	ADAPT68PGA 68PLCC (Note 4)	EB70216	–	RA70116	CC70116
μPD70216R-8	IE-70216-A010	IE-70000-2959	EB-V50MINI-IE	(Note 4)	EB70216	–	RA70116	CC70116
μPD70216R-10	IE-70216-A010	IE-70000-2959	EB-V50MINI-IE	(Note 4)	EB70216	–	RA70116	CC70116
μPD70320GJ	IE-70320-A008	EP-70320GJ (Note 5)	EB-V25MINI-IE-P	EP-70320GJ (Note 6)	DDK-70320	–	RA70320	CC70116
μPD70320GJ-8	IE-70320-A008	EP-70320GJ (Note 5)	EB-V25MINI-IE-P	EP-70320GJ (Note 6)	DDK-70320	–	RA70320	CC70116
μPD70320L	IE-70320-A008	EP-70320L	EB-V25MINI-IE-P	(Note 7)	DDK-70320	–	RA70320	CC70116
μPD70320L-8	IE-70320-A008	EP-70320L	EB-V25MINI-IE-P	(Note 7)	DDK-70320	–	RA70320	CC70116
μPD70322GJ	IE-70320-A008	EP-70320GJ (Note 5)	EB-V25MINI-IE-P	EP-70320GJ (Note 6)	DDK-70320	–	RA70320	CC70116
μPD70322GJ-8	IE-70320-A008	EP-70320GJ (Note 5)	EB-V25MINI-IE-P	EP-70320GJ (Note 6)	DDK-70320	–	RA70320	CC70116
μPD70322L	IE-70320-A008	EP-70320L	EB-V25MINI-IE-P	(Note 7)	DDK-70320	70P322K (Note 10)	RA70320	CC70116

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V-Series Development Tools Selection Guide (cont)

Part Number (Note 1)	Full Emulator	Full Emulator Probe	Mini-IE Emulator	Mini-IE Probe	Evaluation Boards	EPROM/OTP Device	Relocatable Assembler (Note 13)	C Compiler (Note 14)
μPD70322L-8	IE-70320-A008	EP-70320L	EB-V25MINI-IE-P	(Note 7)	DDK70320	70P322K (Note 10)	RA70320	CC70116
μPD70325GJ-8	IE-70325-A008	EP-70320GJ (Note 5)	(Note 12)	(Note 12)	DDK-70325	–	RA70320	CC70116
μPD70325GJ-10	IE-70325-A008 (Note 8)	EP-70320GJ (Note 5)	(Note 12)	(Note 12)	DDK-70325	–	RA70320	CC70116
μPD70325L-8	IE-70325-A008	EP-70320L	(Note 12)	(Note 12)	DDK-70325	–	RA70320	CC70116
μPD70325L-10	IE-70325-A008 (Note 8)	EP-70320L	(Note 12)	(Note 12)	DDK-70325	–	RA70320	CC70116
μPD70327GJ-8 (Note 9)	IE-70320-A008	EP-70320GJ (Note 5)	EB-V25MINI-IE-P	EP-70320GJ (Note 6)	–	–	RA70320	CC70116
μPD70327L-8 (Note 9)	IE-70320-A008	EP-70320L	EB-V25MINI-IE-P	(Note 7)	–	–	RA70320	CC70116
μPD70330GJ-8	IE-70330-A008	EP-70320GJ (Note 5)	EB-V35MINI-IE-P	EP-70320GJ (Note 6)	DDK-70330	–	RA70320	CC70116
μPD70330L-8	IE-70330-A008	EP-70320L	EB-V35MINI-IE-P	(Note 7)	DDK-70330	–	RA70320	CC70116
μPD70332GJ-8	IE-70330-A008	EP-70320GJ (Note 5)	EB-V35MINI-IE-P	EP-70320GJ (Note 6)	DDK-70330	–	RA70320	CC70116
μPD70332L-8	IE-70330-A008	EP-70320L	EB-V35MINI-IE-P	(Note 7)	DDK-70330	70P322K (Note 10)	RA70320	CC70116
μPD70335GJ-8	IE-70335-A008	EP-70320GJ (Note 5)	(Note 12)	(Note 12)	DDK-70330	–	RA70320	CC70116
μPD70335GJ-10	IE-70335-A008 (Note 8)	EP-70320GJ (Note 5)	(Note 12)	(Note 12)	DDK-70330	–	RA70320	CC70116
μPD70335L-8	IE-70335-A008	EP-70320L	(Note 12)	(Note 12)	DDK-70330	–	RA70320	CC70116
μPD70335L-10	IE-70335-A008 (Note 8)	EP-70320L	(Note 12)	(Note 12)	DDK-70330	–	RA70320	CC70116
μPD70337GJ-8 (Note 9)	IE-70330-A008	EP-70320GJ (Note 5)	EB-V35MINI-IE-P	EP-70320GJ (Note 6)	–	–	RA70320	CC70116
μPD70337L-8 (Note 9)	IE-70330-A008	EP-70320L	EB-V35MINI-IE-P	(Note 7)	–	–	RA70320	CC70116
μPD79011GJ-8 (Note 11)	IE-70320-A008	EP-70320GJ (Note 5)	(Note 12)	(Note 12)	–	–	RA70320	CC70116
μPD79011L-8 (Note 11)	+IE-70320-RTOS	EP-70320L	(Note 12)	(Note 12)	–	–	RA70320	CC70116
μPD79021L-8 (Note 11)	IE-70330-A008 +IE-70330-RTOS	EP-70320L	(Note 12)	(Note 12)	–	–	RA70320	CC70116

Notes:

(1) Packages:

Package	Description
GF	80-pin plastic miniflat
GJ	74-pin or 94-pin plastic miniflat
K	84-pin ceramic LCC with window
L	68-pin or 84-pin plastic LCC
R	68-pin PGA

(2) The EP-70136GL-A and EP-70136L-PC contain both a 68-pin PLCC probe and an adapter which converts the 68-pin PLCC probes to a 74-pin miniflat footprint.

(3) 68-pin PGA parts are supported by using the EP-70136L-A PLCC probe or EP-70136L-PC PLCC probe, plus a PLCC socket with a PGA-pinout. A PLCC socket of this type is supplied with the EP-70136L-A.

(4) The EB-V40 MINI-IE and EB-V50 MINI-IE support PGA packages directly; the ADAPT68PGA68PLCC adaptor converts the PGA-pinout on the MINI-IE to a PLCC footprint. This adaptor is supplied with the MINI-IE.

(5) The EP-70320GJ is an adaptor to the EP-70320L, which converts 84-pin PLCC probes to a 94-pin miniflat footprint. For GJ parts, both the PLCC probe and the adaptor are needed.

(6) The EP-70320GJ adaptor can be used to convert the supplied 84-pin PLCC cable of the EB-V25 MINI-IE-P or EB-V35 MINI-IE-P to a 94-pin miniflat.

(7) The EB-V25 MINI-IE-P and EB-V35 MINI-IE-P are supplied with an 84-pin PLCC cable.

(8) At the current time, the emulators for the μPD70325 and μPD70335 are specified to 8 MHz. Contact your local NEC Sales Office for the latest information on 10 MHz emulation.

(9) Development for the μPD70327 or μPD70337 can be done using the appropriate μPD70320 or μPD70330 tools; however, debugging of programs in the Software Guard mode is not supported at this time.

(10) The μPD70P322K EPROM device can be used for both μPD70322 and μPD70332 emulation. The μPD70P322K EPROM device can be programmed by using the PA-70P322L Programming Adapter and the PG-1500 EPROM Programmer.

(11) For emulation of μPD79011 or μPD79021, the base emulator (IE-70320 or IE-70330) plus Real-Time Operating System software IE-70320-RTOS or IE-70330-RTOS) is required.

(12) This emulation option is not currently supported, but may be available in the future. Contact your local NEC Sales Office for further information.

(13) The following relocatable assemblers are available:

RA70116-D52	For V20®/V30®/	(VS-DOS®)
RA70116-VVT1	V40™/V50™	(VAX/VMS™)
RA70116-VXT1		(VAX/UNIX™ 4.2 BSD or Ultrix™)
RA70136-D52	For V33™	(MS-DOS)
RA70136-VVT1		(VAX/VMS)
RA70136-VXT1		(VAX/UNIX 4.2 BSD or Ultrix)
RA70320-D52	For V25™ and V35™	(MS-DOS)
RA70320-VVT1		(VAX/VMS)
RA70320-VXT1		(VAX/UNIX 4.2 BSD or Ultrix)

(14) The following C compilers are available:

CC70116-D52	For V20/V30/	(MS-DOS)
CC70116-VVT1	V40/V50 and	(VAX/VMS)
CC70116-VXT1	V25/V35	(VAX/UNIX 4.2 BSD or Ultrix)
CC70136-D52	For V33	(MS-DOS)
CC70136-VVT1		(VAX/VMS)
CC70136-VXT1		(VAX/UNIX 4.2 BSD or Ultrix)
CC70320-D52	For V25 and V35	(MS-DOS)
CC70320-VVT1		(VAX/VMS)
CC70320-VXT1		(VAX/UNIX 4.2 BSD or Ultrix)

μPD75XX Series Development Tools Selection Guide

Part Number (Note 1)	Emulator*	Add-on Board*	System Evaluation Board	EPROM/OTP Device	PG-1500 Adapter (Note 2)	Absolute Assembler (Note 3)
μPD7501G-12	EVAKIT-7500B	EV7514	SE-7514A	–	–	ASM75
μPD7502G-12	EVAKIT-7500B	EV7514	SE-7514A	–	–	ASM75
μPD7503G-12	EVAKIT-7500B	EV7514	SE-7514A	–	–	ASM75
μPD7506C	EVAKIT-7500B	–	SE-7508	–	–	ASM75
μPD7506CT	EVAKIT-7500B	–	–	–	–	ASM75
μPD7506G-00	EVAKIT-7500B	–	–	–	–	ASM75
μPD7507C	EVAKIT-7500B	–	–	μPD78CG08E	–	ASM75
μPD7507CU	EVAKIT-7500B	–	–	–	–	ASM75
μPD7507G-00	EVAKIT-7500B	–	–	–	–	ASM75
μPD7507HC	EVAKIT-7500B	EV7508H	–	μPD75CG08HE	–	ASM75
μPD7507HCU	EVAKIT-7500B	EV7508H	–	–	–	ASM75
μPD7507HG-22	EVAKIT-7500B	EV7508H	–	–	–	ASM75
μPD7507SC	EVAKIT-7500B	–	SE-7508	–	–	ASM75
μPD7507SCT	EVAKIT-7500B	–	–	–	–	ASM75
μPD7508C	EVAKIT-7500B	–	–	μPD78CG08E	–	ASM75
μPD7508CU	EVAKIT-7500B	–	–	–	–	ASM75
μPD7508G-00	EVAKIT-7500B	–	–	–	–	ASM75
μPD75CG08E	EVAKIT-7500B	–	–	–	–	ASM75
μPD7508AC	EVAKIT-7500B	–	SE-7508	–	–	ASM75
μPD7508HC	EVAKIT-7500B	EV7508H	–	μPD75CG08HE	–	ASM75
μPD7508HCU	EVAKIT-7500B	EV7508H	–	–	–	ASM75
μPD7508HG-22	EVAKIT-7500B	EV7508H	–	–	–	ASM75
μPD75CG08HE	EVAKIT-7500B	EV7508H	–	–	–	ASM75
μPD7514G-12	EVAKIT-7500B	EV7514	SE-7514A	–	–	ASM75
μPD7516HCW	EVAKIT-7500B	EV7500FIP	–	–	–	ASM75
μPD7516HG-12	EVAKIT-7500B	EV7500FIP	–	–	–	ASM75
μPD7516HG-36	EVAKIT-7500B	EV7500FIP	–	μPD75CG16HE	–	ASM75
μPD75CG16HE	EVAKIT-7500B	EV7500FIP	–	–	–	ASM75
μPD7519HCW	EVAKIT-7500B	EV7500FIP	–	–	–	ASM75
μPD7519HG-12	EVAKIT-7500B	EV7500FIP	–	–	–	ASM75
μPD7519HG-36	EVAKIT-7500B	EV7500FIP	–	μPD75CG19HE	–	ASM75
μPD75CG19HE	EVAKIT-7500B	EV7500FIP	–	–	–	ASM75
μPD7527AC	EVAKIT-7500B	EV7528	–	μPD75CG28E	–	ASM75
μPD7527ACU	EVAKIT-7500B	EV7528	–	–	–	ASM75
μPD7528AC	EVAKIT-7500B	EV7528	–	μPD75CG28E	–	ASM75
μPD7528ACU	EVAKIT-7500B	EV7528	–	–	–	ASM75

* Required Tools

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μPD75XX Series Development Tools Selection Guide (cont)

Part Number (Note 1)	Emulator*	Add-on Board*	System Evaluation Board	EPROM/OTP Device	PG-1500 Adapter (Note 2)	Absolute Assembler (Note 3)
μPD75CG28E	EVAKIT-7500B	EV7528	–	–	–	ASM75
μPD7533C	EVAKIT-7500B	EV7533	–	μPD75CG33E	–	ASM75
μPD7533CU	EVAKIT-7500B	EV7533	–	–	–	ASM75
μPD7533G-22	EVAKIT-7500B	EV7533	–	–	–	ASM75
μPD75CG33E	EVAKIT-7500B	EV7533	–	–	–	ASM75
μPD7537AC	EVAKIT-7500B	EV7528	–	μPD75CG38E	–	ASM75
μPD7537ACU	EVAKIT-7500B	EV7528	–	–	–	ASM75
μPD7538AC	EVAKIT-7500B	EV7528	–	μPD75CG38E	–	ASM75
μPD7538ACU	EVAKIT-7500B	EV7528	–	–	–	ASM75
μPD75CG38E	EVAKIT-7500B	EV7528	–	–	–	ASM75
μPD7554CS	EVAKIT-7500B	EV7554A	SE-7554A	μPD75P54CS	PA-75P54CS	ASM75
μPD7554G	EVAKIT-7500B	EV7554A	SE-7554A	μPD75P54G	PA-75P54CS	ASM75
μPD75P54CS	EVAKIT-7500B	EV7554A	–	–	–	ASM75
μPD75P54G	EVAKIT-7500B	EV7554A	–	–	–	ASM75
μPD7556CS	EVAKIT-7500B	EV7554A	SE-7554A	μPD75P56CS	PA-75P56CS	ASM75
μPD7556G	EVAKIT-7500B	EV7554A	SE-7554A	μPD75P56G	PA-75P56CS	ASM75
μPD75P56CS	EVAKIT-7500B	EV7554A	–	–	–	ASM75
μPD75P56G	EVAKIT-7500B	EV7554A	–	–	–	ASM75
μPD7564CS	EVAKIT-7500B	EV7554A	SE-7554A	μPD75P64CS	PA-75P54CS	ASM75
μPD7564G	EVAKIT-7500B	EV7554A	SE-7554A	μPD75P64G	PA-75P54CS	ASM75
μPD75P64CS	EVAKIT-7500B	EV7554A	–	–	–	ASM75
μPD75P64G	EVAKIT-7500B	EV7554A	–	–	–	ASM75
μPD7566CS	EVAKIT-7500B	EV7554A	SE-7554A	μPD75P66CS	PA-75P56CS	ASM75
μPD7566G	EVAKIT-7500B	EV7554A	SE-7554A	μPD75P66G	PA-75P56CS	ASM75
μPD75P66CS	EVAKIT-7500B	EV7554A	–	–	–	ASM75
μPD75P66G	EVAKIT-7500B	EV7554A	–	–	–	ASM75

* Required tools

Notes:

(1) Packages:

Package	Description
C	28-pin plastic DIP (μPD7506/07S)
	40-pin plastic DIP (μPD7507/07H/08/08A/08H)
	42-pin plastic DIP (μPD7527A/28A/33/37A/38A)
CS	20-pin plastic shrink DIP (μPD7554/P54/64/P64)
	24-pin plastic shrink DIP (μPD7556/P56/66/P66)
CT	28-pin plastic shrink DIP
CU	40-pin plastic shrink DIP (μPD7507/07H/08/08H)
	42-pin plastic shrink DIP (μPD7527A/28A/33/37/37A/38A)
CW	64-pin plastic shrink DIP
E	40-pin ceramic piggy-back DIP (μPD75CG08/08H)
	42-pin ceramic piggy-back DIP (μPD75CG28/33/38)
	64-pin ceramic piggy-back QUIP (μPD75CG16H/19H)
G	20-pin plastic SO (μPD7554/P54/64/P64)
	24-pin plastic SO (μPD7556/P56/66/P66)
G-00	52-pin plastic miniflat
G-12	64-pin plastic miniflat (μPD7501/02/03/16H/19H)
	80-pin plastic miniflat (μPD7514)
G-22	44-pin plastic miniflat
G-36	64-pin plastic QUIP

(2) By using the specified adapter, the PG-1500 EPROM programmer can be used to program the OTP device.

(3) The ASM75 Absolute Assembler is provided to run under the MOS-DOS® operating system. (ASM75-D52).

MS-DOS is registered trademark of Microsoft Corporation.

μPD75XXX Series Development Tools Selection Guide

Part Number (Note 7)	Main Board Emulator*	Add-on Board*	Emulation Probe*	Optional Socket Adapter (Note 1)	EPROM/OTP Device (Note 2)	Relocatable Assembler (Note 5)	Structured Assembler (Note 6)
μPD75004CU	EVAKIT-75X	EV-75008	(Note 3)	–	μPD75P008CU/DU	RA75X	ST75X
μPD75006GB	EVAKIT-75X	EV-75008	EP-75008GB	EV-9200G-44	μPD75P008GB	RA75X	ST75X
μPD75006CU	EVAKIT-75X	EV-75008	(Note 3)	–	μPD75P008CU/DU	RA75X	ST75X
μPD75006GB	EVAKIT-75X	EV-75008	EP-75008GB	EV-9200G-44	μPD75P008GB	RA75X	ST75X
μPD75008CU	EVAKIT-75X	EV-75008	(Note 3)	–	μPD75P008CU/DU	RA75X	ST75X
μPD75008GB	EVAKIT-75X	EV-75008	EP-75008GB	EV-9200G-44	μPD75P008GB	RA75X	ST75X
μPD75P008CU	EVAKIT-75X	EV-75008	(Note 3)	–	–	RA75X	ST75X
μPD75P008DU	EVAKIT-75X	EV-75008	(Note 3)	–	–	RA75X	ST75X
μPD75P008GB	EVAKIT-75X	EV-75008	EP-75008GB	EV-9200G-44	–	RA75X	ST75X
μPD75028CW	EVAKIT-75X	EV-75048	(Note 4)	(Note 4)	μPD75P028CW	RA75X	ST75X
μPD75028GC	EVAKIT-75X	EV-75048	(Note 4)	(Note 4)	μPD75P028GC	RA75X	ST75X
μPD75P028CW	EVAKIT-75X	EV-75048	(Note 4)	(Note 4)	–	RA75X	ST75X
μPD75P028GC	EVAKIT-75X	EV-75048	(Note 4)	(Note 4)	–	RA75X	ST75X
μPD75048CW	EVAKIT-75X	EV-75048	(Note 4)	(Note 4)	–	RA75X	ST75X
μPD75048GC	EVAKIT-75X	EV-75048	(Note 4)	(Note 4)	–	RA75X	ST75X
μPD75104CW	EVAKIT-75X	EV-75108	(Note 3)	–	μPD75P108CW/DW	RA75X	ST75X
μPD75104G	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	μPD75P108G/GF μPD75P116GF	RA75X	ST75X
μPD75104GF	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	μPD75P108G/GF μPD75P116GF	RA75X	ST75X
μPD75104AGC	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	–	RA75X	ST75X
μPD75106CW	EVAKIT-75X	EV-75108	(Note 3)	–	μPD75P108CW/DW	RA75X	ST75X
μPD75106G	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	μPD75P108G/GF μPD75P116GF	RA75X	ST75X
μPD75106GF	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	μPD75P108G/GF μPD75P116GF	RA75X	ST75X
μPD75108AG	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	–	RA75X	ST75X
μPD75108AGC	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	–	RA75X	ST75X
μPD75108CW	EVAKIT-75X	EV-75108	(Note 3)	–	μPD75P108CW/DW	RA75X	ST75X
μPD75108G	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	μPD75P108G/GF μPD75P116GF	RA75X	ST75X
μPD75108GF	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	μPD75P108G/GF μPD75P116GF	RA75X	ST75X
μPD75P108BCW	EVAKIT-75X	EV-75108	(Note 3)	–	–	RA75X	ST75X
μPD75P108CW	EVAKIT-75X	EV-75108	(Note 3)	–	–	RA75X	ST75X
μPD75P108DW	EVAKIT-75X	EV-75108	(Note 3)	–	–	RA75X	ST75X
μPD75P108G	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	–	RA75X	ST75X
μPD75112CW	EVAKIT-75X	EV-75108	(Note 3)	–	μPD75P116CW	RA75X	ST75X

* Required Tools

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μPD75XXX Series Development Tools Selection Guide (cont)

Part Number (Note 7)	Main Board Emulator*	Add-on Board*	Emulation Probe*	Optional Socket Adapter (Note 1)	EPROM/OTP Device (Note 2)	Relocatable Assembler (Note 5)	Structured Assembler (Note 6)
μPD75112GF	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	μPD75P116GF	RA75X	ST75X
μPD75116CW	EVAKIT-75X	EV-75108	(Note 3)	–	μPD75P116CW	RA75X	ST75X
μPD75116GF	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	μPD75P116GF	RA75X	ST75X
μPD75P116BGF	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	–	RA75X	ST75X
μPD75P116CW	EVAKIT-75X	EV-75108	(Note 3)	–	–	RA75X	ST75X
μPD75P116GF	EVAKIT-75X	EV-75108	EP-75108GF	EV-9200G-64	–	RA75X	ST75X
μPD75206CW	EVAKIT-75X	EV-75216A	(Note 3)	–	μPD75P216ACW	RA75X	ST75X
μPD75206G	EVAKIT-75X	EV-75216A	EP-75216AGF	EV-9200G-64	–	RA75X	ST75X
μPD75208CW	EVAKIT-75X	EV-75216A	(Note 3)	–	μPD75P216ACW	RA75X	ST75X
μPD75208G	EVAKIT-75X	EV-75216A	EP-75216AGF	EV-9200G-64	–	RA75X	ST75X
μPD75CG208AE	EVAKIT-75X	EV-75216A	(Note 3)	–	–	RA75X	ST75X
μPD75CG208AEA	EVAKIT-75X	EV-75216A	EP-75216AGF	EV-9200G-64	–	RA75X	ST75X
μPD75212ACW	EVAKIT-75X	EV-75216A	(Note 3)	–	μPD75P216ACW	RA75X	ST75X
μPD75212AGF	EVAKIT-75X	EV-75216A	EP-75216AGF	EV-9200G-64	–	RA75X	ST75X
μPD75216ACW	EVAKIT-75X	EV-75216A	(Note 3)	–	μPD75P216ACW	RA75X	ST75X
μPD75216AGF	EVAKIT-75X	EV-75216A	EP-75216AGF	EV-9200G-64	–	RA75X	ST75X
μPD75CG216AE	EVAKIT-75X	EV-75216A	(Note 3)	–	–	RA75X	ST75X
μPD75CG216AEA	EVAKIT-75X	EV-75216A	EP-75216AGF	EV-9200G-64	–	RA75X	ST75X
μPD75P216ACW	EVAKIT-75X	EV-75216A	(Note 3)	–	μPD75P216ACW	RA75X	ST75X
μPD75268CW	EVAKIT-75X	EV-75216A	(Note 3)	–	μPD75P216ACW	RA75X	ST75X
μPD75268GF	EVAKIT-75X	EV-75216A	EP-75216AGF	EV-9200G-64	–	RA75X	ST75X
μPD75304GF	EVAKIT-75X	EV-75308	(Note 3)	EV-9200G-80	μPD75P308GF/K	RA75X	ST75X
μPD75306GF	EVAKIT-75X	EV-75308	(Note 3)	EV-9200G-80	μPD75P308GF/K	RA75X	ST75X
μPD75308GF	EVAKIT-75X	EV-75308	(Note 3)	EV-9200G-80	μPD75P308GF/K	RA75X	ST75X
μPD75P308GF	EVAKIT-75X	EV-75308	(Note 3)	EV-9200G-80	–	RA75X	ST75X
μPD75P308K	EVAKIT-75X	EV-75308	(Note 3)	EV-9200G-80	–	RA75X	ST75X
μPD75312GF	EVAKIT-75X	EV-75308	(Note 3)	EV-9200G-80	μPD75P316GF	RA75X	ST75X
μPD75P316GF	EVAKIT-75X	EV-75308	(Note 3)	EV-9200G-80	–	RA75X	ST75X
μPD75328GC	EVAKIT-75X	EV-75328	(Note 3)	–	μPD75P328GC	RA75X	ST75X
μPD75P328GC	EVAKIT-75X	EV-75328	(Note 3)	–	–	RA75X	ST75X
μPD75402C	EVAKIT-75X	EV-75402	(Note 3)	–	μPD75P402C	RA75X	ST75X
μPD75402CT	EVAKIT-75X	EV-75402	(Note 3)	–	μPD75P402CT	RA75X	ST75X
μPD75402GB	EVAKIT-75X	EV-75402	EP-75402GB	EV-9200G-44	μPD75P402GB	RA75X	ST75X
μPD75P402C	EVAKIT-75X	EV-75402	(Note 3)	–	–	RA75X	ST75X
μPD75P402CT	EVAKIT-75X	EV-75402	(Note 3)	–	–	RA75X	ST75X
μPD75P402GB	EVAKIT-75X	EV-75402	EP-75402GB	EV-9200G-44	–	RA75X	ST75X
μPD75516GF	EVAKIT-75X	EV-75516	(Note 3)	–	μPD75P516GF/K	RA75X	ST75X
μPD75P516GF	EVAKIT-75X	EV-75516	(Note 3)	–	–	RA75X	ST75X
μPD75P516K	EVAKIT-75X	EV-75516	(Note 3)	–	–		

* Required Tools

Notes:

(1) The EV-9200G-XX is an LCC socket with the footprint of the flat package. One unit is supplied with the probe. Additional units are available as replacement parts in sets of five.

(2) All EPROM/OTP devices can be programmed using the NEC PG-1500. Refer to the PG-1500 Programming Socket Adapter Selection Guide for the appropriate socket adapter.

(3) The emulation probe is shipped with the add-on board.

(4) Preliminary information. Contact your NEC Sales Representative for further information and availability.

(5) The RA75X relocatable assembler package is provided for the following operating systems:
RA75X-D52 (MOS-DOS®)
RA75X-VVT1 (VAX/VMS™)

(6) The ST75X structures assembler preprocessor is provided with RA75X

(7) Packages:

Package	Description
C	28-pin plastic DIP
CT	28-pin plastic shrink DIP
CU	42-pin plastic shrink DIP
CW	64-pin plastic shrink DIP
DU	42-pin ceramic shrink DIP with window
DW	64-pin ceramic shrink DIP with window
E	64-pin ceramic piggy-back shrink DIP
EA	64-pin ceramic piggy-back miniflat
G	64-pin plastic miniflat
GB	44-pin plastic miniflat
GC	64 or 80-pin plastic miniflat
GF	64 or 80-pin plastic miniflat
K	80-pin plastic miniflat

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μPD78XX Series Development Tools Selection Guide**

Part Number (Note 1)	Emulator*	Emulation Probe*	EPROM/OTP Device	PG-1500 Adapter (Note 2)	Relocatable Assembler (Note 10)	C Compiler (Note 10)
μPD7810HCW	IE-7811H-M	EV-9001-64 (Note 3)	–	–	RA87	CC87
μPD7810HG-36	IE-7811H-M	(Note 4)	–	–	RA87	CC87
μPD7811HCW	IE-7811H-M	EV-9001-64 (Note 3)	–	–	RA87	CC87
μPD7811HG-36	IE-7811H-M	(Note 4)	μPD78PG11HE (Note 6)	–	RA87	CC87
μPD78PG11HE	IE-7811H-M	(Note 4)	–	–	RA87	CC87
μPD78C10CW	IE-78C11-M	EV-9001-64 (Note 3)	–	–	RA87	CC87
μPD78C10G-36	IE-78C11-M	(Note 4)	–	–	RA87	CC87
μPD78C10G-1B	IE-78C11-M	(Note 5)	–	–	RA87	CC87
μPD78C10GF-3BE	IE-78C11-M	(Note 5)	–	–	RA87	CC87
μPD78C10L	IE-78C11-M	(Note 5)	–	–	RA87	CC87
μPD78C10ACW	IE-78C11-M (Note 8)	EV-9001-64 (Note 3)	–	–	RA87	CC87
μPD78C10AGQ-36	IE-78C11-M (Note 8)	(Note 4)	–	–	RA87	CC87
μPD78C10AGF-3BE	IE-78C11-M (Note 8)	(Note 5)	–	–	RA87	CC87
μPD78C10AL	IE-78C11-M (Note 8)	(Note 5)	–	–	RA87	CC87
μPD78C11CW	IE-78C11-M	EV-9001-64 (Note 3)	μPD78CP14CW/DW	PA-78CP14CW	RA87	CC87
μPD78C11G-36	IE-78C11-M	(Note 4)	μPD78CP14GQ-36/R μPD78CG14E	PA-78CP14GQ	RA87	CC87
μPD78C11G-1B	IE-78C11-M	(Note 5)	μPD78CP14GF-3BE	PA-78CP14GF	RA87	CC87
μPD78C11GF-3BE	IE-78C11-M	(Note 5)	μPD78CP14GF-3BE	PA-78CP14GF	RA87	CC87
μPD78C11L	IE-78C11-M	(Note 5)	μPD78CP14L	PA-78CP14L	RA87	CC87
μPD78C11ACW	IE-78C11-M (Note 8)	EV-9001-64 (Note 3)	μPD78CP14CW/DW (Note 7)	PA-78CP14CW	RA87	CC87
μPD78C11AGQ-36	IE-78C11-M (Note 8)	(Note 4)	μPD78CP14GQ-36/R (Note 7)	PA-78CP14GQ	RA87	CC87
μPD78C11AGF-3BE	IE-78C11-M (Note 8)	(Note 5)	μPD78CP14GF-3BE (Note 7)	PA-78CP14GF	RA87	CC87
μPD78C11AL	IE-78C11-M (Note 8)	(Note 5)	μPD78CP14L (Note 7)	PA-78CP14L	RA87	CC87
μPD78C12ACW	IE-78C11-M (Note 8)	EV-9001-64 (Note 3)	μPD78CP14CW/DW (Note 7)	PA-78CP14CW	RA87	CC87
μPD78C12AGQ-36	IE-78C11-M (Note 8)	(Note 4)	μPD78CP14GQ-36/R (Note 7)	PA-78CP14GQ	RA87	CC87

* Required Tools

** For all μPD78C1X devices, you may use the DDK-78C10 for evaluation purposes.

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μPD78XX Series Development Tools Selection Guide** (cont)

Part Number (Note 1)	Emulator*	Emulation Probe*	EPROM/OTP Device	PG-1500 Adapter (Note 2)	Relocatable Assembler (Note 10)	C Compiler (Note 10)
μPD78C12AGF-3BE	IE-78C11-M (Note 8)	(Note 5)	μPD78CP14GF-3BE (Note 7)	PA-78CP14GF	RA87	CC87
μPD78C12AL	IE-78C11-M (Note 8)	(Note 5)	μPD78CP14L (Note 7)	PA-78CP14L	RA87	CC87
μPD78C14CW	IE-78C11-M	EV-9001-64 (Note 3)	μPD78CP14CW/DW	PA-78CP14CW	RA87	CC87
μPD78C14G-36	IE-78C11-M	(Note 4)	μPD78CP14GQ-36/R μPD78CG14E	PA-78CP14GQ	RA87	CC87
μPD78C14G-1B	IE-78C11-M	(Note 5)	μPD78CP14GF	PA-78CP14GF	RA87	CC87
μPD78C14GF-3BE	IE-78C11-M	(Note 5)	μPD78CP14GF	PA-78CP14GF	RA87	CC87
μPD78C14L	IE-78C11-M	(Note 5)	μPD78CP14L	PA-78CP14L	RA87	CC87
μPD78C14AG-AB8	IE-78C11-M (Note 8)	(Note 5)	–	–	RA87	CC87
μPD78CG14E (Note 9)	IE-78C11-M	(Note 4)	–	–	RA87	CC87
μPD78CP14CW	IE-78C11-M	EV-9001-64 (Note 3)	–	PA-78CP14CW	RA87	CC87
μPD78CP14DW	IE-78C11-M	EV-9001-64 (Note 3)	–	PA-78CP14CW	RA87	CC87
μPD78CP14GQ-36	IE-78C11-M	(Note 4)	–	PA-78CP14GQ	RA87	CC87
μPD78CP14GF-3BE	IE-78C11-M	(Note 5)	–	PA-78CP14GF	RA87	CC87
μPD78CP14L	IE-78C11-M	(Note 5)	–	PA-78CP14L	RA87	CC87
μPD78CP14R	IE-78C11-M	(Note 4)	–	PA-78CP14GQ	RA87	CC87

* Required Tools

Notes:

(1) Packages

Package	Description
CW	64-pin plastic shrink DIP
DW	64-pin ceramic shrink DIP with window
E	64-pin ceramic piggyback QUIP
GF-1B	64-pin plastic miniflat (Resin Thickness: 2.05mm)
G-36	64-pin plastic QUIP
G-AB8	64-pin plastic miniflat (Interpin Pitch: 0.8mm)
GF-3BE	64-pin plastic miniflat (Resin Thickness: 2.7mm)
GQ-36	64-pin plastic QUIP
L	68-pin PLCC
R	64-pin ceramic QUIP with window

(2) By using the specified adapter, the PG-1500 EPROM programmer can be used to program the EPROM/OTP device.

(3) 64-pin shrink DIP adapter which plugs into the EP-7811HGQ emulation probe supplied with each IE.

(4) The emulation probe for the 64-pin QUIP package (EP-7811HGQ) is supplied with the IE.

(5) No emulation probe available.

(6) The μPD78PG11HE is a piggy-back EPROM device in a ceramic QUIP package. It accepts 2764 EPROMs.

(7) The μPD78CP14 EPROM/OTP devices do not have pull-up resistors on ports A, B, and C.

(8) The IE-78C11-M can be used by replacing the μPD78C10G-36 with a μPD78C10AGQ-36. However, it will not be able to emulate the optional pull-up resistors on ports A, B, and C.

(9) The μPD78CG14E is a piggy-back EPROM device in a ceramic QUIP package. It accepts 27C256 and 27C256A EPROMS.

(10) The following relocatable assemblers and C Compilers are available:

RA87-D52 RA87-VVT1	(MS-DOS®) (VAX/VMS™)	Relocatable assemblers for 78XX series
CCMSD-I5DD-87 CCVMS-OT16-87 CCUNX-OT16-87	(MS-DOS) (VAX/VMS) (VAX/UNIX™) 4.2 BSD or Ultrix™)	C Compilers for 78XX Series

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UNIX is a trademark of AT&T Bell Laboratories.

μPD78XXX Series Development Tools Selection Guide

Part Number (Note 1)	Emulator*	Emulation Probe*	EPROM/OTP Device	PG-1500 Adapter (Note 2)	Relocatable Assembler (Notes 11)	Structured Assembler (Note 12)	C Compiler (Note 13)
μPD78213CW	IE-78210-R	EP-78210CW	–	–	RA78K2	ST78K2	CC782XX
μPD78213GC-3B8	IE-78210-R	EP-78210GC	–	–	RA78K2	ST78K2	CC782XX
μPD78213GJ-5BJ	IE-78210-R	EP-78210GJ (Note 3)	–	–	RA78K2	ST78K2	CC782XX
μPD78213GQ-36	IE-78210-R	EP-78210GQ	–	–	RA78K2	ST78K2	CC782XX
μPD78213L	IE-78210-R	EP-78210L	–	–	RA78K2	ST78K2	CC782XX
μPD78214CW	IE-78210-R	EP-78210CW	μPD78P214CW/DW	PA-78P214CW	RA78K2	ST78K2	CC782XX
μPD78214GC-3B8	IE-78210-R	EP-78210GC	μPD78P214GC	PA-78P214GC	RA78K2	ST78K2	CC782XX
μPD78214GJ-5BJ	IE-78210-R	EP-78210GJ (Note 3)	μPD78P214GJ	PA-78P214GJ	RA78K2	ST78K2	CC782XX
μPD78214GQ-36	IE-78210-R	EP-78210GQ	μPD78P214GQ	PA-78P214GQ	RA78K2	ST78K2	CC782XX
μPD78214L	IE-78210-R	EP-78210L	μPD78P214L	PA-78P214L	RA78K2	ST78K2	CC782XX
μPD78P214CW	IE-78210-R	EP-78210CW	–	PA-78P214CW	RA78K2	ST78K2	CC782XX
μPD78P214DW	IE-78210-R	EP-78210CW	–	PA-78P214CW	RA78K2	ST78K2	CC782XX
μPD78P214GC-3B8	IE-78210-R	EP-78210GC	–	PA-78P214GC	RA78K2	ST78K2	CC782XX
μPD78P214GJ-5BJ	IE-78210-R	EP-78210GJ (Note 3)	–	PA-78P214GJ	RA78K2	ST78K2	CC782XX
μPD78P214GQ-36	IE-78210-R	EP-78210GQ	–	PA-78P214GQ	RA78K2	ST78K2	CC782XX
μPD78P214L	IE-78210-R	EP-78210L	–	PA-78P214L	RA78K2	ST78K2	CC782XX
μPD78220GJ-5BG	IE-78220-R	EP-78220GJ (Note 4)	–	–	RA78K2	ST78K2	CC782XX
μPD78220L	IE-78220-R	EP-78220L	–	–	RA78K2	ST78K2	CC782XX
μPD78224GJ-5BG	IE-78220-R	EP-78220GJ (Note 4)	μPD78P224GJ	PA-78P224GJ	RA78K2	ST78K2	CC782XX
μPD78224L	IE-78220-R	EP-78220L	μPD78P224L	PA-78P224L	RA78K2	ST78K2	CC782XX
μPD78P224GJ-5BG	IE-78220-R	EP-78220GJ (Note 4)	–	PA-78P224GJ	RA78K2	ST78K2	CC782XX
μPD78P224L	IE-78220-R	EP-78220L	–	PA-78P224L	RA78K2	ST78K2	CC782XX
μPD78310ACW	IE-78310A-R	(Note 5)	μPD78P312ACW/DW	PA-78P312CW	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78310AGF-3BE	IE-78310A-R	EP-78310GF	μPD78P312AGF-3BE	PA-78P312GF	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78310AGQ	IE-78310A-R	(Note 6)	μPD78P312AGQ/RQ	PA-78P312GQ	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78310AL	IE-78310A-R	EP-78310L	μPD78P312AL	PA-78P312L	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78312ACW	IE-78310A-R	(Note 5)	μPD78P312ACW/DW	PA-78P312CW	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78312AGF-3BE	IE-78310A-R	EP-78310GF	μPD78P312AGF-3BE	PA-78P312GF	RA78K3	ST78K3	CC78K3 (Note 7)

* Required Tools

μPD78XXX Series Development Tools Selection Guide (cont)

Part Number (Note 1)	Emulator*	Emulation Probe*	EPROM/OTP Device	PG-1500 Adapter (Note 2)	Relocatable Assembler (Note 11)	Structured Assembler (Note 12)	C Compiler (Note 13)
μPD78312AGQ	IE-78310A-R	(Note 6)	μPD78P312AGQ/RQ	PA-78P312GQ	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78312AL	IE-78310A-R	EP-78310L	μPD78P312AL	PA-78P312L	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78P312ACW	IE-78310A-R	(Note 5)	–	PA-78P312CW	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78P312ADW	IE-78310A-R	(Note 5)	–	PA-78P312CW	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78P312AGF-3BE	IE-78310A-R	EP-78310GF	–	PA-78P312GF	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78P312AGQ	IE-78310A-R	(Note 6)	–	PA-78P312GQ	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78P312AL	IE-78310A-R	EP-78310L	–	PA-78P312L	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78P312AR	IE-78310A-R	(Note 6)	–	PA-78P312GQ	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78320GJ-5BJ	IE-78320-R	(Note 8)	(Note 8)	(Note 8)	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78320L	IE-78320-R	(Note 8)	(Note 8)	(Note 8)	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78322GJ-5BJ	IE-78320-R	(Note 8)	(Note 8)	(Note 8)	RA78K3	ST78K3	CC78K3 (Note 7)
μPD78322L	IE-78320-R	(Note 8)	(Note 8)	(Note 8)	RA78K3	ST78K3	CC78K3 (Note 7)
μPD71P301GF-3BE	–	–	–	PA-71P301GF	–	–	–
μPD71P301GQ-36	–	–	–	PA-71P301GQ	–	–	–
μPD71P301KA (Note 9)	–	–	–	PA-71P301KA	–	–	–
μPD71P301KB (Note 10)	–	–	–	PA-71P301KB	–	–	–
μPD71P301L	–	–	–	PA-71P301L	–	–	–

* Required Tools

Notes:

(1) Packages:

Package	Description
CW	64-pin plastic shrink DIP
DW	64-pin ceramic shrink DIP with window
GC-3B8	64-pin ceramic plastic miniflat (14mm x 14mm
GF-3BE	64-pin plastic miniflat (Resin Thickness: 2.7mm)
GJ-5BG	94-pin plastic miniflat
GJ-5BJ	74-pin plastic miniflat (20mm x 20mm)
GQ	64-pin plastic QUIP
GQ-36	64-pin plastic QUIP
KA	44-pin ceramic LCC with window
KB	64-pin ceramic LCC with window
L	44-pin PLCC (μPD71P301L) 68-pin PLCC (μPD78213/214/P214L, μPD78320/322L) 84 pin PLCC (μPD78220L, μPD78224L)
RQ	64-pin ceramic QUIP with window

(2) By using the specified adapter, the PG-1500 EPROM programmer can be used to program the EPROM/OTP device.

(3) The EP-78210GJ is a 68-pin PLCC to 74-pin miniflat package adapter for use with the EP-78210L emulation probe.

(4) The EP-78220GJ is a 84-pin PLCC to 94-pin miniflat package adapter for use with the EP-78220L emulation probe.

(5) The emulation probe for the 64-pin shrink DIP package (EP-78310CW) is supplied with the IE.

(6) The emulation probe for the 64-pin QUIP package (EP-78310GQ) is supplied with the IE.

(7) There are two C Compilers for the μPD783XX devices: CC78K3 from NEC Electronics and one from Lattice Corporation. A source code debugger is included with CC78K3 package.

(8) Please contact your NEC Sales Representative for further information.

(9) Sockets for the μPD71P301KA (44-pin LCC package) are available from Yamaichi (IC61-0444-030).

(10) Sockets for the μPD71P301KB (64-pin LCC package) are available from NEC Electronics (EV-9200G-64) in sets of five.

μPD78XXX Series Evaluation Boards Selection Guide

Part Number	Design/Development Boards	Evaluation Boards
μPD7821X	EB-78210-PC	DDK-78K2
μPD7822X	EB-78220-PC	DDK-78K2
μPD7831X	—	DDK-78310A
μPD7832X	EB-78320-PC	—

Notes:

(1) The following relocatable packages are available:

RA78K2-D52 RA78K2-VVT1	(MS-DOS®) (VAX/VMS™)	Relocatable assembler for 78XX series
RA78K3-D52 RA78K3-VVT1	(MS-DOS) (VAX/VMS)	Relocatable assembler for 78XX series

(2) The ST78K2 structured assembler processor is provided with RA78K2. The ST78K3 structured assembler preprocessor is provided with RA78K3 and CC78K3.

(3) The following C Compiler packages are available:

CCMSD-I5DD-782XX CC78K3-D52 CC78K3-VVT1	(MS-DOS) (MS-DOS) (VAX/VMS)	For μPD783XX series

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VAX and VMS are trademarks of Digital Equipment Corporation.

DSP and Speech Development Tools Selection Guide

Part Number (Note 7)	Emulator	Evaluation Board	Assembler (Note 1)	Simulator (Note 2)	EPROM/OTP Device	PG-1500 Adapter (Note 3)
μPD7720AC	EVAKIT-7720B	—	ASM77	SIM77	μPD77P20D	(Note 5)
μPD7720AL	EVAKIT-7720B (Note 4)	—	ASM77	SIM77	—	—
μPD77P20D	EVAKIT-7720B	—	ASM77	SIM77	—	—
μPD77C20AC	EVAKIT-7720B	—	ASM77	SIM77	μPD77P20D	(Note 5)
μPD77C20AL	EVAKIT-7720B (Note 4)	—	ASM77	SIM77	—	—
μPD77C20ALK	EVAKIT-7720B (Note 4)	—	ASM77	SIM77	—	—
μPD77220L	EVAKIT-77220	—	RA77230	SM77230	—	—
μPD77220R	EVAKIT-77220	—	RA77230	SM772230	μPD77P220R	PA-77P230R
μPD77P220R	EVAKIT-77220	—	RA77230	SM77230	—	PA-77P230R
μPD77230AR	EVAKIT-77230	DDK-77230	RA77230	SM77230	μPD77P230R	PA-77P230R
μPD77P230R	EVAKIT-77230	DDK-77230	RA77230	SM77230	—	PA-77P230R
μPD77C25C	EVAKIT-77C25	—	RA77C25	—	μPD77P25C/D	PA-77P25C
μPD77C25L	EVAKIT-77C25 (Note 4)	—	RA77C25	—	μPD77P25L	—
μPD77P25C	EVAKIT-77C25	—	RA77C25	—	—	PA-77P25C
μPD77P25D	EVAKIT-77C25	—	RA77C25	—	—	PA-77P25C
μPD77P25L	EVAKIT-77C25 (Note 4)	—	RA77C25	—	—	—
μPD7755C	NV-300 System	EB-7759	—	—	μPD77P56C	PA-77P56C
μPD7755G	NV-300 System	EB-7759 (Note 6)	—	—	μPD77P56G	PA-77P56C
μPD7756C	NV-300 System	EB-7759	—	—	μPD77P56C	PA-77P56C
μPD7756G	NV-300 System	EB-7759 (Note 6)	—	—	μPD77P56G	PA-77P56C
μPD77P56C	NV-300 System	EB-7759	—	—	—	PA-77P56C
μPD77P56G	NV-300 System	EB-7759 (Note 6)	—	—	—	PA-77P56C
μPD7757C	NV-300 System	EB-7759	—	—	—	—
μPD7757G	NV-300 System	EB-7759 (Note 6)	—	—	—	—
μPD7759C	NV-300 System	EB-7759	—	—	—	—
μPD7759GC	NV-300 System	EB-7759	—	—	—	—
μPD77810L	IE-77810	—	RA77810	—	—	—
μPD77810R	IE-77810	—	RA77810	—	—	—

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Notes:

(1) The following assemblers are available:

Part Number	Description
ASM77-D52	Assembler for 7720 (MS-DOS®)
RA77C25-D52	Assembler for 77C25 (MS-DOS)
RA77C25-VVT1	Assembler for 77C25 (VAX/VMS™)
RA77230-D52	Assembler for 77230 (MS-DOS)
RA77230-VVT1	Assembler for 77230 (VAX/VMS)
RA77230-VXT1	Assembler for 77230 (VAX/UNIX ™) 4.2 BSD or Ultrix™)

(2) The following simulators are available:

Part Number	Description
SIM77-D52	Simulator for 7720 (MS-DOS)
SM77230-VVT1	Simulator for 77230 (VAX/UNIX)
SM77230-VXT1	Simulator for 77230 (VAX/UNIX 4.2 BSD or Ultrix)

(3) By using the specified adapter, the NEC PG-1500 EPROM programmer can be used to program the EPROM/OTP device.

(4) Please check with your NEC Sales Representative on the availability of a PLCC emulation probe.

(5) The μPD77P20D can be programmed using the EVAKIT-7720B.

(6) The EB-7759 comes with an emulation probe for only the 18-pin DIP.

(7) Packages:

Package	Description
C	18, 28, or 40-pin plastic DIP
D	28-pin ceramic DIP
G	24-pin plastic SOP
GC	52-pin plastic miniflat
L	44-or 68-pin PLCC
LK	28-pin PLCC
R	68-pin ceramic PGA

Socket Adapters and Adapter Modules

Target Chip	Socket Adapter (Note 1)	Adapter Module (Note 2)
Standard 27XXX EPROM Devices		
μPD27256 (12.5 V)	–	027A Board
μPD27256 (21 V)	–	027A Board
μPD27C256	–	027A Board
μPD27C256A	–	027A Board
μPD27C512	–	027A Board
μPD27C1000	–	027A Board
μPD27C1001	–	027A Board
μPD27C1024	–	027A Board
μPD75XX Series Devices		
μPD75P54CS	PA-75P54CS	04A Board
μPD75P54G	PA-75P54CS	04A Board
μPD75P56CS	PA-75P56CS	04A Board
μPD75P56G	PA-75P56CS	04A Board
μPD75P64CS	PA-75P54CS	04A Board
μPD75P64G	PA-75P54CS	04A Board
μPD75P66CS	PA-75P56CS	04A Board
μPD75P66G	PA-75P56CS	04A Board
μPD75XXX Series Devices		
μPD75P008CU	PA-75P008CU	04A Board
μPD75P008DU	PA-75P008CU	04A Board
μPD75P008GB	PA-75P008CU	04A Board
μPD75P028CW	PA-75P028CW	04A Board
μPD75P028GC	PA-75P028GC	04A Board
μPD75P108BCW	PA-75P108CW	04A Board
μPD75P108CW	PA-75P108CW	04A Board
μPD75P108DW	PA-75P108CW	04A Board
μPD75P108BGF	PA-75P116GF	04A Board
μPD75P108G	PA-75P116GF	04A Board
μPD75P116CW	PA-75P108CW	04A Board
μPD75P116GF	PA-75P116GF	04A Board
μPD75P216ACW	PA-75P216ACW	04A Board
μPD75P308GF	PA-75P308GF	04A Board
μPD75P308K	PA-75P308K	04A Board

Target Chip	Socket Adapter (Note 1)	Adapter Module (Note 2)
μPD75XXX Series Devices (cont)		
μPD75P316GF	PA-75P308GF	04A Board
μPD75P328GC	PA-75P328GC	04A Board
μPD75P402C	(Note 3)	027A Board
μPD75P402CT	PA-75P402CT	027A Board
μPD75P402GB	PA-75P402GB	027A Board
μPD75P516GF	PA-75P516GF	04A Board
μPD75P516K	PA-75P516K	04A Board
μPD78XX Series Devices		
μPD78CP14CW	PA-78CP14CW	027A Board
μPD78CP14DW	PA-78CP14CW	027A Board
μPD78CP14GQ	PA-78CP14GQ	027A Board
μPD78CP14GF	PA-78CP14GF	027A Board
μPD78CP14L	PA-78CP14L	027A Board
μPD78CP14R	PA-78CP14GQ	027A Board
μPD78XXX Series Devices		
μPD71P301GF	PA-71P301GF	027A Board
μPD71P301GQ	PA-71P301GQ	027A Board
μPD71P301KA	PA-71P301KA	027A Board
μPD71P301KB	PA-71P301KB	027A Board
μPD71P301L	PA-71P301L	027A Board
μPD78P214CW	PA-78P214CW	027A Board
μPD78P214GC	PA-78P214GC	027A Board
μPD78P214GJ	PA-78P214GJ	027A Board
μPD78P214GQ	PA-78P214GQ	027A Board
μPD78P214L	PA-78P214L	027A Board
μPD78P224GJ	PA-78P224GJ	027A Board
μPD78P224L	PA-78P224L	027A Board
μPD78P312ACW	PA-78P312CW	027A Board
μPD78P312ADW	PA-78P312CW	027A Board
μPD78P312AGF	PA-78P312GF	027A Board
μPD78P312AGQ	PA-78P312GQ	027A Board
μPD78P312AL	PA-78P312L	027A Board
μPD78P312AR	PA-78P312GQ	027A Board

Socket Adapters and Adapter Modules (cont)

Target Chip	Socket Adapter (Note 1)	Adapter Module (Note 2)
V-Series Devices		
μPD70P322K	PA-70P322L	027A Board
Digital Signal Processors		
μPD77P56C	PA-77P56C	04A Board
μPD77P56G	PA-77P56C	04A Board
μPD77P25C	PA-77P25C	027A Board
μPD77P25D	PA-77P25C	027A Board
μPD77P230R	PA-77P230R	027A Board

Notes:

(1) All socket adapters must be purchased separately.

(2) The 27A and 04A Adapter Modules are shipped with the PG-1500.

(3) The μPD75P402C does not require a programming socket adapter. It can be plugged directly into the 027A Board.

NEC

COMMUNICATIONS CONTROLLERS

2

Section 2
Communications Controllers

μPD7201A
Multiprotocol, Serial Communications Controller

Description

The μPD7201A is a dual-channel, multiprotocol, serial communications controller (MPSCC) that satisfies a wide variety of serial data communication requirements in computer systems. Its basic function is as a serial-to-parallel, parallel-to-serial converter/controller, and it is software configurable for serial data communications applications.

The μPD7201A can handle asynchronous and synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. It also supports virtually any other serial protocol for applications other than data communications.

The μPD7201A can generate and check cyclic redundancy check (CRC) codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where modem controls are not needed, they can be used for general-purpose I/O.

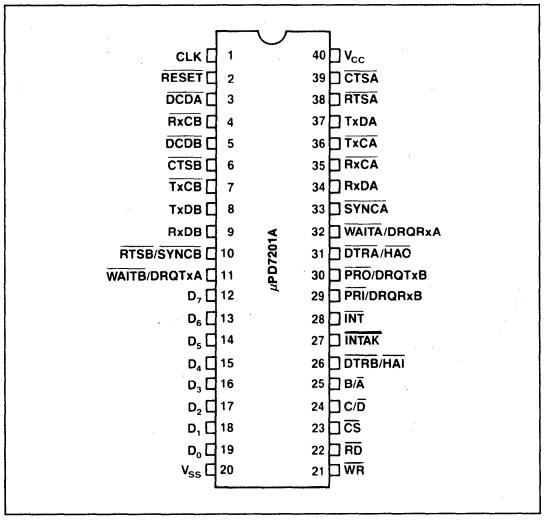
Features

- ☐ Two independent full-duplex serial channels
- ☐ Four independent DMA channels for send/receive data for both serial inputs/outputs
- ☐ Programmable interrupt vectors and interrupt priorities
- ☐ Modem control signals
- ☐ Variable software programmable data rate, up to 1 Mb/s at 5-MHz system clock
- ☐ Double-buffered transmitter data and quadruple-buffered receive data
- ☐ Selectable CRC algorithm
- ☐ Selection of interrupt, DMA, or polling mode of operation
- ☐ Asynchronous operation
  - — Character length: 5, 6, 7, or 8 bits
  - — Data clock frequency: 1x, 16x, 32x, or 64x data rate
  - — Parity: odd, even, or disable
  - — Break generation and detection
  - — Interrupt on parity, overrun, or framing errors
- ☐ Monosync, bisync, and external sync operations
  - — Software selectable sync characters
  - — Automatic sync insertion
  - — CRC generation and checking
- ☐ HDLC and SDLC operations
  - — Abort sequence generation and detection
  - — Automatic zero insertion and detection
  - — Address field recognition
  - — CRC generation and checking
  - — I-field residue handling
- ☐ N-channel MOS technology
- ☐ Single +5V power supply; interface to most microprocessors including 8080, 8085, 8086, and others.
- ☐ Single-phase TTL system clock: up to 5 MHz
- ☐ Plastic and ceramic dual-in-line packages

Ordering Information

Part Number	Package Type
μPD7201AC	40-pin plastic DIP
μPD7201AD	40-pin ceramic DIP

Pin Configuration



Pin Identification

No.	Symbol	Function
1	CLK	System clock input
2	$\overline{RESET}$	Reset input
3	$\overline{DCDA}$	Data carrier detect input A
4	$\overline{RxCB}$	Receiver clock input B
5	$\overline{DCDB}$	Data carrier detect input B
6	$\overline{CTSB}$	Clear to send input B
7	$\overline{TxCB}$	Transmitter clock input B
8	TxDB	Transmit data output B
9	RxDB	Receive data input B
10	$\overline{RTSB}/\overline{SYNCB}$	Request to send output B/Synchronization input/output B
11	$\overline{WAITB}$/DRQTxA	Wait output B/Transmit DMA request output A
12-19	D_7-D_0	Data Bus
20	V_{SS}	Ground
21	$\overline{WR}$	Write strobe input
22	$\overline{RD}$	Read strobe input
23	$\overline{CS}$	Chip select input
24	C/$\overline{D}$	Control/data input
25	B/$\overline{A}$	Channel select input
26	$\overline{DTRB}/\overline{HAI}$	Data terminal output B/Hold acknowledge input
27	$\overline{INTAK}$	Interrupt acknowledge input
28	$\overline{INT}$	Interrupt request output
29	$\overline{PRI}$/DRQRxB	Interrupt priority input/Receive DMA request output B
30	$\overline{PRO}$/DRQTxB	Interrupt priority output/Transmit DMA request output B
31	$\overline{DTRA}/\overline{HAO}$	Data terminal output A/Hold acknowledge output
32	$\overline{WAITA}$/DRQRxA	Wait output A/Receive DMA request output A
33	$\overline{SYNCA}$	Synchronization input/output A
34	RxDA	Receive data input A
35	$\overline{RxCA}$	Receiver clock input A
36	$\overline{TxCA}$	Transmitter clock input A
37	TxDA	Transmit data output A
38	$\overline{RTSA}$	Request to send output A
39	$\overline{CTSA}$	Clear to send input A
40	V_{CC}	+5 V

Pin Functions

CLK [System Clock]

A TTL-level clock signal is applied to the CLK input. The system clock frequency must be at least 4.5 times the data rate.

$\overline{RESET}$ [Reset]

A low on the $\overline{RESET}$ input (one complete CLK cycle minimum) initializes the MPSCC to the following conditions: receivers and transmitters disabled, TxDA and TxDB set to marking (high), and modem controls ($\overline{DTRA}$, $\overline{DTRB}$, $\overline{RTSA}$, $\overline{RTSB}$) set high.

In addition, all interrupts are disabled and all interrupt and DMA requests are cleared. All control registers must be rewritten after a reset before transmission or reception can be restarted.

$\overline{DCDA}$, $\overline{DCDB}$ [Data Carrier Detect]

The $\overline{DCDA}$ and $\overline{DCDB}$ inputs go low to indicate the presence of valid serial data at RxD. The MPSCC may be programmed so that the receiver is enabled only when $\overline{DCD}$ is low, and so that any change in state that lasts longer than the minium specified pulse width causes an interrupt and latches the $\overline{DCD}$ status bit to the new state.

$\overline{RxCA}$, $\overline{RxCB}$ [Receiver Clock]

The $\overline{RxCA}$ and $\overline{RxCB}$ inputs control sampling and shifting serial data at RxDA and RxDB. The MPSCC can be programmed so that the clock rate is 1, 16, 32, or 64 times the data rate. RxD is sampled on the rising edge of $\overline{RxC}$. $\overline{RxC}$ features a Schmitt-trigger input for relaxed rise and fall time requirements.

$\overline{TxCA}$, $\overline{TxCB}$ [Transmitter Clock]

The $\overline{TxCA}$ and $\overline{TxCB}$ inputs control the rate at which data is shifted out at TxDA and TxDB. The MPSCC can be programmed so that the clock rate is 1, 16, 32, or 64 times the data rate. Data changes on the falling edge of $\overline{TxC}$. $\overline{TxC}$ features a Schmitt-trigger input for relaxed rise and fall time requirements.

TxDA, TxDB [Transmit Data]

TxDA and TxDB output serial data from the MPSCC. (Marking high).

RxDA, RxDB [Receive Data]

RxDA and RxDB input serial data to the MPSCC. (Marking high.)

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$ [Clear to Send]

The $\overline{\text{CTSA}}$ and $\overline{\text{CTSB}}$ inputs go low to indicate that the receiving modem or peripheral is ready to receive data from the MPSCC. The MPSCC can be programmed so that the transmitter is enabled only when CTS is low. As with $\overline{\text{DCD}}$, the MPSCC can be programmed to cause an interrupt and latch the new state when $\overline{\text{CTS}}$ changes state for longer than the minimum specified pulse width.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$ [Request to Send]

When the MPSCC is in one of the synchronous modes, $\overline{\text{RTSA}}$ and $\overline{\text{RTSB}}$ are general-purpose outputs that can be set or reset with commands to the MPSCC. In asynchronous mode, $\overline{\text{RTS}}$ is active (low) as soon as it is programmed on. However, when programmed off, $\overline{\text{RTS}}$ remains active until the transmitter is completely empty. This feature simplifies the programming required to perform modem control.

$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$ [Synchronization]

The function of the $\overline{\text{SYNCA}}$ and $\overline{\text{SYNCB}}$ pins depends on the MPSCC operating mode. In asynchronous mode, $\overline{\text{SYNC}}$ is used as an input that the processor can read. It can be programmed to generate an interrupt in the same manner as $\overline{\text{DCD}}$ or $\overline{\text{CTS}}$.

In external sync mode, $\overline{\text{SYNC}}$ is an active-low input that notifies the MPSCC that synchronization has been achieved (see timing waveforms for details). Once synchronization is achieved, $\overline{\text{SYNC}}$ should be held low until synchronization is lost or a new message is about to start.

In internal synchronization modes (monosync, bisync, HDLC), $\overline{\text{SYNC}}$ is an output which is active (low) whenever a SYNC character match is made. There is no qualifying logic associated with this function. Regardless of character boundaries, $\overline{\text{SYNC}}$ is active on any match.

DRQTxA, DRQTxB, DRQRxA, DRQRxB [DMA Request]

When a DRQTxA, DRQTxB, DRQRxA, or DRQRxB output is active (high), it indicates to a DMA controller that a transmitter or receiver is requesting a DMA data transfer.

$\overline{\text{WAITA}}$, $\overline{\text{WAITB}}$ [Wait]

The $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ outputs synchronize the processor with the MPSCC when block transfer mode is used. It can be programmed to operate with either the receiver or transmitter, but not both simutaneously. $\overline{\text{WAIT}}$ is normally inactive (high). If the processor tries, for example, to perform an inappropriate data transfer such as a write to the transmitter when the transmitter buffer is full, the $\overline{\text{WAIT}}$ output for the channel will go active (low) until the MPSCC is ready to accept the data. The $\overline{\text{CS}}$, C/$\overline{\text{D}}$, B/$\overline{\text{A}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ inputs must remain stable while wait is active. (Open drain.)

D_0-D_7 [Data Bus]

The three-state data bus lines are connected to the system data bus. Data or status from the MPSCC is output on these lines when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are active (low). Data and commands are latched into the MPSCC on the rising edge of $\overline{\text{WR}}$ when $\overline{\text{CS}}$ is active.

$\overline{\text{WR}}$ [Write Strobe]

A low on the $\overline{\text{WR}}$ input (with either CS during the read cycle or HAI during a DMA cycle) notifies the MPSCC to write data or control information to the device.

$\overline{\text{RD}}$ [Read Strobe]

A low on the $\overline{\text{RD}}$ input (with either $\overline{\text{CS}}$ during a read cycle or $\overline{\text{HAI}}$ during a DMA cycle) notifies the MPSCC to read data or status from the device.

$\overline{\text{CS}}$ [Chip Select]

A low on the $\overline{\text{CS}}$ input allows the MPSCC to transfer data or commands during a read or write cycle.

C/$\overline{\text{D}}$ [Control/Data]

The C/$\overline{\text{D}}$ input, with $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$, and B/$\overline{\text{A}}$ selects the data register (C/D = 0) or the control and status registers (C/D = 1) for access over the data bus.

B/$\overline{\text{A}}$ [Channel Select]

B/$\overline{\text{A}}$ input low selects channel A and B/$\overline{\text{A}}$ high selects channel B for access during a read or write cycle.

$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$ [Data Terminal]

The $\overline{\text{DTRA}}$ and $\overline{\text{DTRB}}$ outputs are general-purpose, active-low outputs which may be set or reset with commands to the MPSCC.

$\overline{\text{INTAK}}$ [Interrupt Acknowledge]

The processor generates two or three $\overline{\text{INTAK}}$ low pulses (depending on the processor type) to signal all peripheral devices that an interrupt acknowledge sequence is taking place. During the interrupt acknowledge sequence, the MPSCC, if so programmed, places information on the data bus to vector the processor to the appropriate interrupt service location.

$\overline{\text{INT}}$ [Interrupt Request]

The $\overline{\text{INT}}$ output is pulled low when an internal interrupt request is accepted. (Open drain.)

$\overline{\text{PRI}}$ [Interrupt Priority In]

The $\overline{\text{PRI}}$ input informs the MPSCC that the highest priority device is requesting an interrupt. It is used with $\overline{\text{PRO}}$ to implement a priority-resolution daisychain when there is more than one interrupting device. The state of $\overline{\text{PRI}}$ and the programmed interrupt mode determine the MPSCC's response to an interrupt acknowledge sequence.

$\overline{\text{PRO}}$ [Interrupt Priority Out]

The $\overline{\text{PRO}}$ output is active (low) when $\overline{\text{PRI}}$ is active (low) and the MPSCC is not requesting an interrupt ($\overline{\text{INT}}$ is not active).

The active state informs the next lower priority device that there are no higher priority interrupt requests pending during an acknowledge sequence.

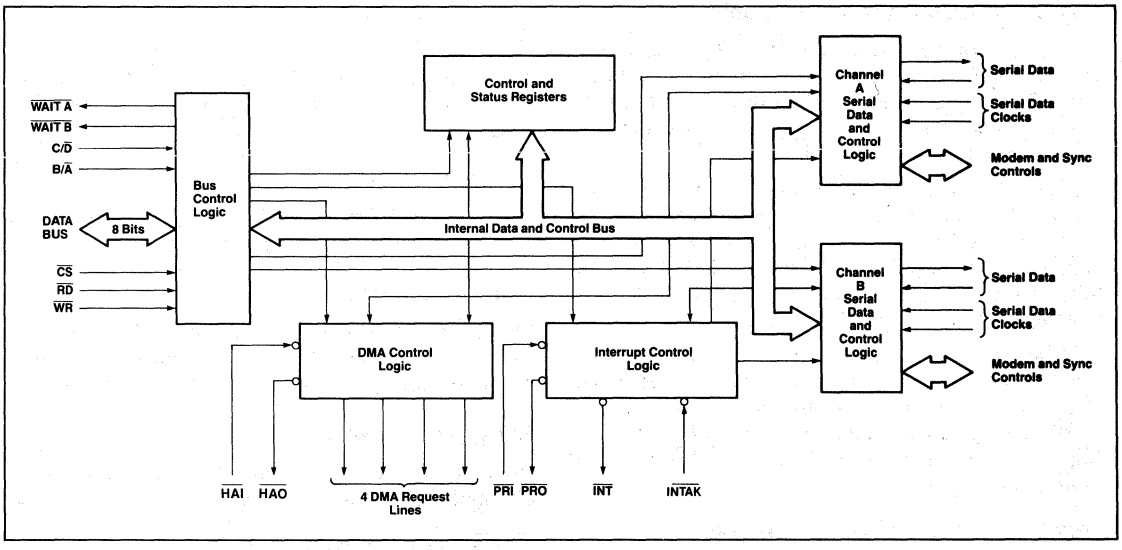
$\overline{\text{HAI}}$ [Hold Acknowledge In]

The $\overline{\text{HAI}}$ input goes low to notify the MPSCC that the host processor has acknowledged the DMA request and has placed itself in the hold state. The MPSCC then performs a DMA cycle for the highest priority outstanding DMA request, if any.

$\overline{\text{HAO}}$ [Hold Acknowledge Out]

The $\overline{\text{HAO}}$ output, with $\overline{\text{HAI}}$, implements a priority-resolution daisychain for multiple DMA devices. $\overline{\text{HAO}}$ is active (low) when $\overline{\text{HAI}}$ is active and there are no DMA requests pending in the MPSCC.

Block Diagram



Absolute Maximum Ratings

T_A = 25°C

Power Supply, V_{CC}	−0.5 to + 7.0 V
Input Voltage, V_I	−0.5 to + 7.0 V
Output Voltage, V_O	−0.5 to + 7.0 V
Operating temperature, T_{OPT}	0°C to + 70°C
Storage Temperature, T_{STG}	−65°C to + 150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C; V_{CC} = GND = OV

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Input Capacitance	C_{IN}		10	pF	fc = 1MHz
Output Capacitance	C_{OUT}		15	pF	Unmeasured pins
I/O Capacitance	$C_{I/O}$		20	pF	returned to GND.

DC Characteristics

T_A = 0°C to + 70°C; V_{CC} = +5 V ± 10%

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Input low voltage	V_{IL}	−0.5	+0.8	V	
Input high voltage	V_{IH}	+2.0	V_{CC}+0.5	V	
Output low voltage	V_{OL}		+0.45	V	I_{OL} = +2.0 mA
Output high Voltage	V_{OH}	+2.4		V	I_{OH} = 200μA
Input leakage current	I_{IL}		±10	μA	V_{IN}=V_{CC} to 0 V
Output leakage current	I_{OL}		±10	μA	V_{OUT}=V_{CC} to 0 V
V_{CC} supply current	I_{CC}		230	mA	

AC Characteristics

T_A = 0°C to + 70°C; V_{CC} = +5 V ± 10%

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Clock cycle	t_{CY}	200	4000	ns	
Clock high width	t_{CH}	70	2000	ns	
Clock low width	t_{CL}	70	2000	ns	

AC Characteristics (cont)

T_A = 0°C to + 70°C; V_{CC} = +5 V ± 10%

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Clock rise time	t_r	0	30	ns	
Clock fall time	t_f	0	30	ns	
Address setup to $\overline{RD}$	t_{AR}	0		ns	
Address hold from $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ pulse width	t_{RR}	200		ns	
Data output delay from address	t_{AD}		200	ns	
Data output delay from $\overline{RD}$	t_{RD}		200	ns	
Data float delay from $\overline{RD}$	t_{DF}	10	100	ns	
Address setup from $\overline{WR}$	t_{AW}	0		ns	
Address hold from $\overline{WR}$	t_{WA}	0		ns	
$\overline{WR}$ pulse width	t_{WW}	200		ns	
Data setup to $\overline{WR}$	t_{DW}	130		ns	
Data hold from $\overline{WR}$	t_{WD}	0		ns	
PRO delay from $\overline{PRI}$	t_{PIPO}		100	ns	
PRO delay from $\overline{INTAK}$	t_{IAPO}		200	ns	
PRI setup to $\overline{INTAK}$	t_{PHA}	0		ns	
PRI hold from $\overline{INTAK}$	t_{IAPI}	20		ns	
$\overline{INTAK}$ pulse width	t_{IAIA}	200		ns	
Data output delay from $\overline{INTAK}$	t_{IAD}		200	ns	
Data float delay from $\overline{INTAK}$	t_{DF}	10	100	ns	
Request hold from $\overline{RD}$/$\overline{WR}$	t_{CQ}		150	ns	
$\overline{HAI}$ setup to $\overline{RD}$/$\overline{WR}$	t_{HIC}	300		ns	
$\overline{HAI}$ hold from $\overline{RD}$/$\overline{WR}$	t_{CHI}	0		ns	
$\overline{HAO}$ delay from $\overline{HAI}$	t_{HIHO}		100	ns	
Data clock cycle	t_{DCY}	400		ns	RxC, TxC

AC Characteristics (cont)

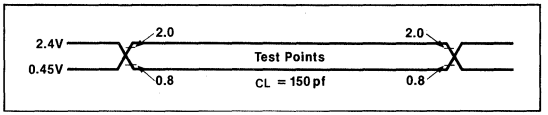
T_A = 0°C to + 70°C; V_{CC} = +5 V ± 10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Data clock high width	t_{DCH}	180		ns	RxC, TxC
Data clock low width	t_{DCL}	180		ns	RxC, TxC
Tx data delay from TxC	t_{TCTD}		300	ns	x1 Mode
			1000	ns	x16, x32, x64 Mode
Rx data setup to RxC	t_{RDRC}	0		ns	
Rx Data hold from RxC	t_{RCRD}	140		ns	
INT delay Time from Tx Data	t_{IDI}		4–6	t_{CY}	
INT delay Time from RxC	t_{RCI}		7–11	t_{CY}	
CTS, DCD, SYNC high pulse width	t_{MH}	200		ns	
CTS, DCD, SYNC low pulse width	t_{ML}	200		ns	
External INT from CTS, DCD, SYNC	t_{MF}		500	ns	
Recovery time between controls	t_{RV}	300		ns	
WAIT delay time from Address	t_{AWT}		120	ns	
SYNC setup to RxC	t_{RCS}		100	ns	

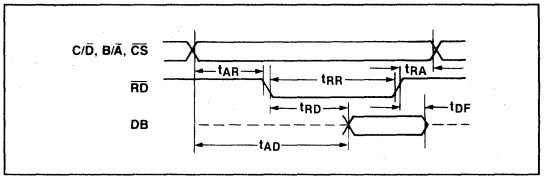
Note: 1. RESET must be active for a minimum of one complete CLK cycle.
2. In all modes system clock rate must be 4.5 times data rate.

Timing Waveforms

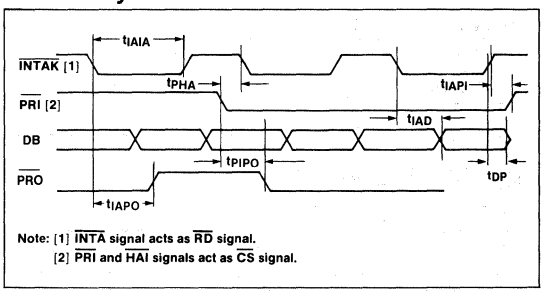
AC Waveform Measurement Points



Read Cycle

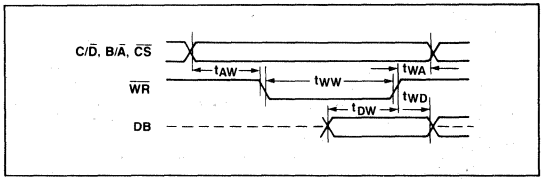


INTAK Cycle

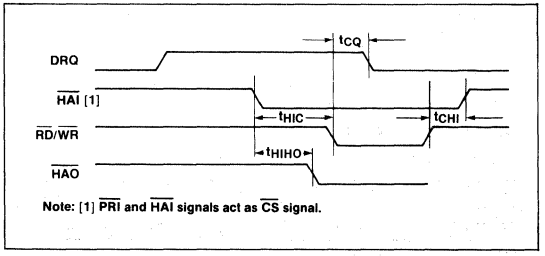


Note: [1] INTA signal acts as RD signal.
[2] PRI and HAI signals act as CS signal.

Write Cycle



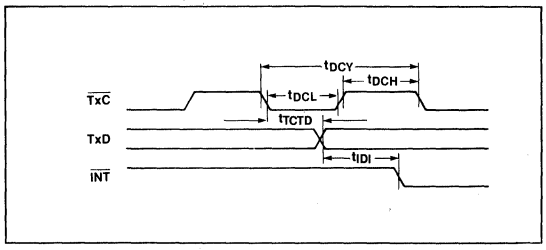
DMA Cycle



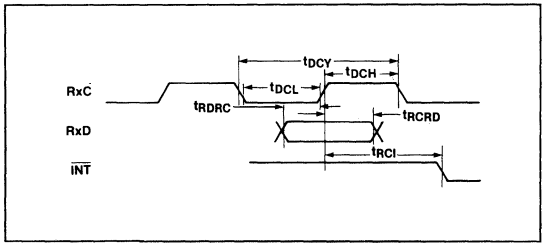
Note: [1] PRI and HAI signals act as CS signal.

Timing Waveforms (cont)

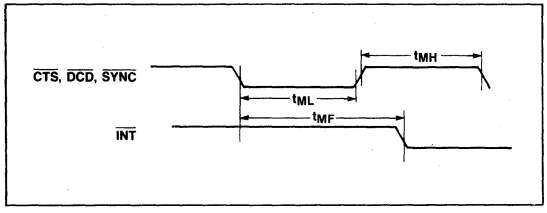
Transmit Data Cycle



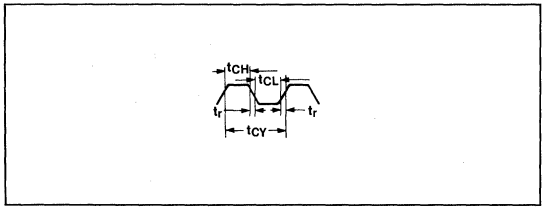
Receive Data Cycle



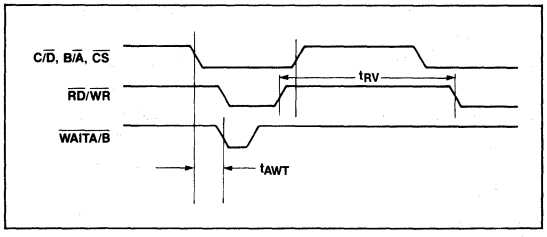
Other Timing



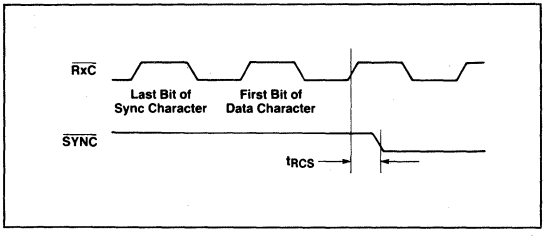
Clock



Read/Write Cycle (Software Block Transfer Mode)



Sync Pulse Generation (External Sync Mode)



Programming the MPSCC

Software operation of the MPSCC includes consistent register organization and high-level command structure to help minimize the number of operations required to implement complex protocol designs. The MPSCC also has extensive interrupt and status reporting capabilities to simplify programming.

The MPSCC Registers

The MPSCC interfaces to the system software with a number of control and status registers associated with each channel (see tables 1 and 2). Commonly used commands and status bits are accessed directly through control and status register 0. Other functions are accessed indirectly with a register pointer to minimize the address space that must be dedicated to the MPSCC.

All control and status registers except CR2 are separately maintained for each channel. Control and status register 2 are linked with the overall operation of the MPSCC and have different meanings when addressed through different channels.

Before intializing the MPSCC, first program control register 2A (2B if desired) to establish the MPSCC processor/bus interface mode. Each channel may then be programmed for separate use beginning with control register 4 to set the protocol mode for that channel. The remaining registers may then be programmed in any order.

Table 1. Control Registers

Control Register	Function
0	Frequently used commands and register pointer control
1	Interrupt control
2	Processor/bus interface control
3	Receiver control
4	Mode control
5	Transmitter control
6	Sync/address character
7	Sync character

Control Register 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CRC Control Command		Command			Register Pointer		

Register Pointer [D_0-D_2]

The register pointer specifies which register number is accessed at the next control register write or status register read. After a hardware or software reset, the register pointer is set to zero. Therefore, the first control byte goes to control register 0. When the register pointer is set to a value other than zero the next control or status ($C/\overline{D} = 1$) access is to the specified register. The pointer is then reset to 0 by setting the register pointer.

Commands [D_3-D_5]

Commands commonly used during the operation of the MPSCC are grouped in control register 0. They include the following:

Null [000]: This command has no effect and is used only to set the register pointer or issue a CRC command.

Send Abort [001]: When operating in the HDLC mode, this command causes the MPSCC to transmit the HDLC abort code by issuing 8 to 13 consecutive 1s. Any data currently in the transmitter or the transmitter buffer is destroyed. After sending the abort, the transmitter reverts to the idle phase (flags). When using the Tx byte count mode enable (D_6 of CR1), the send abort command is automatically issued when an underrun condition occurs.

Table 2. Status Registers

Status Register	Function
0	Buffer and "external/status" status
1	Received character error and special condition status
2 (Channel B only)	Interrupt Vector
3	Tx byte count register, low byte
4	Tx byte count register, high byte

Reset External Status Interrupt [010]: When the external/status change flag is set, the condition of bits D_3-D_7 of status register 0 are latched to capture the short pulses that may occur. The reset external/status interrupts command reenables the latches so that new interrupts may be sensed.

Channel Reset [011]: This command has the same effect on a single channel as an external reset at pin 2. A channel reset command to channel A rests the internal interrupt prioritization logic. This does not occur when a channel reset command is issued to channel B. All control registers associated with the channel to be reset must be reinitialized. After a channel reset, wait at least four system clock cycles before writing new commands or controls to that channel.

Enable Interrupt on Next Character [100]: Issue this command at any time when operating the MPSCC in an interrupt on first received character mode. This command must be issued at the end of a message to reenable the interrupt logic for the next received character (first character of the next message).

Reset Pending Transmitter Interrupt/DMA Request [101]: A pending transmitter buffer empty interrupt or DMA request can be reset without sending another character by issuing this command (typically at the end of a message). A new transmitter buffer empty interrupt or DMA request is not made until another character has been loaded and transferred to the transmitter shift register or when, if operating in synchronous mode, the first CRC character has been sent.

Error Reset [110]: This command resets a special receive condition interrupt. It also reenables the parity and overrun error latches that allow error checking at the end of a message.

End of Interrupt [111] [Channel A Only]: Once an interrupt request has been issued by the MPSCC, all lower priority internal and external interrupts in the daisy chain are held off to permit the current interrupt to be serviced while allowing higher priority interrupts to occur. At some point in the interrupt service routine (generally at the end), the end of the interrupt command must be issued to channel A to reenable the daisy chain and allow any pending lower priority internal interrupt requests to occur. The EOI command must be sent to channel A for interrupts that occured on either channel.

CRC Control Commands [D_6-D_7]

The following commands control the operation of the CRC generator/checker logic:

Null [00]: This command has no effect and is used when issuing other commands or setting the register pointer.

Reset Receiver CRC Checker [01]: This command resets the CRC checker to zero when the channel is in a synchronous mode. It resets to all 1s when in an HDLC mode.

Reset Transmitter CRC Generator [10]: This command resets the CRC generator to zero when the channel is in a synchronous mode. It resets to all 1s when in an HDLC mode.

Reset Idle/CRC Latch [11]: This command resets the idle/CRC latch so that when a transmitter underrun condition occurs (transmitter has no more characters to send), the transmitter enters the CRC phase of operation and begins to send the 16-bit CRC character calculated up to that point. The latch is then set so that if the underrun condition persists, idle characters are sent following the CRC. After a hardware or software reset, the latch is in the set state. This latch is automatically reset after the first character has been loaded into the Tx buffer in the HDLC mode.

Control Register 1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Wait Function Enable	Tx Byte Count Mode Enable	Wait on Receive Transmitter	Receiver Interrupt Mode		Condition Affects Vector	Transmitter Interrupt Enable	Ext/Status INT Enable

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Low Byte							

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
High Byte							

External/Status Interrupt Enable [D_0]

When this bit is set to one, the MPSCC issues an interrupt whenever any of the following conditions occur:
- Transition of the DCD, CTS or SYNC input pin
- Entering or leaving synchronous hunt phase, break detection or termination
- HDLC abort detection or termination
- Idle/CRC latch set (CRC being sent)
- After ending flag is sent in the HDLC mode

Transmitter Interrupt Enable [D_1]

When this bit is set to one, the MPSCC issues an interrupt when the following conditions occur:
- A character currently in the transmitter buffer is transferred to the shift register (transmitter buffer becomes empty), or
- The transmitter enters the idle phase and begins transmitting sync or flag characters.
- The Tx byte count mode enable bit is set (D_6 of CR1 = 1). The 7201A will automatically issue a Tx interrupt or DMA request when the transmitter becomes enabled (D_3 of CR5 = 1).

Condition Affects Vector [D_2]

When this bit is set to zero, the fixed vector programmed in CR2B during MPSCC initialization is returned in an interrupt acknowledge sequence. When this bit is set to one, the vector is modified to reflect the condition that caused the interrupt. (Programmed in channel B for both channels).

Receiver Interrupt Mode [D_3 - D_4]

This field controls how the MPSCC interrupt/DMA logic handles the character received condition.

Receiver Interrupts/DMA Request Disabled [00]: The MPSCC does not issue an interrupt or a DMA request when a character has been received.

Interrupt/DMA on First Received Character Only [01]: In this mode the MPSCC issues an interrupt only for the first character received after an enable interrupt/DMA on first character command (CR0) has been given. If the channel is in a DMA mode, a DMA request is issued for each character received, including the first. In general, use this mode whenever the MPSCC is in a DMA or block transfer mode. This will signal the processor that the beginning of an incoming message has been received.

Interrupt [and Issue a DMA Request] on All Received Characters [10]: In this mode an interrupt (and DMA request if the DMA mode is selected) is issued whenever there is a character present in the receiver buffer. A parity error is considered a special receive condition.

Interrupt [and Issue a DMA Request] on All Received Characters [11]: This mode is the same as the one above, except that a parity error is not considered a special receive condition. The following are considered special receive conditions:
— Receive overrun error
— Asynchronous framing error
— Parity error (if specified)
— HDLC end of message (final flag received)

Wait on Receiver/Transmitter [D_5]

If the wait function is enabled for block mode transfers, setting this bit to zero causes the MPSCC to issue a wait (WAIT output goes low) when the processor attempts to write a character to the transmitter while the transmitter buffer is full. Setting this bit to one causes the MPSCC to issue a wait when the processor attempts to read a character from the receiver while the receiver buffer is empty.

Tx Byte Count Enable [D_6]

Each channel has a 16-bit Tx byte count register used for automatic transmit termination. When this bit is set to one, the next two consecutive command cycle writes will be to the byte count register. The first byte is loaded into the lower 8 bits and the second to the upper 8 bits of the byte count register. The byte count register holds the number of transfers to be performed by the transmitter. A byte counter is incremented each time a transfer is performed until the value of the byte counter is equal to the value in the byte count register. When equal, interrupts or DMA requests will be stopped until the byte count enable bit is issued and a new byte count is loaded into the byte count register. If a transmit underrun occurs in the HDLC mode, and the byte count is not equal to the byte count register, an abort sequence will be sent automatically.

Also, when using the Tx byte count mode, a transmit interrupt or DMA request will automatically become active after issuing the TX enable command to CR5.

The Tx byte count mode can be cleared by either a channel reset command or a hardware reset.

Wait Function Enable [D_7]

Setting this bit to one enables the wait function selected by D_5 of CR1.

Control Register 2 (Channel A)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Pin 10 SYNCB/ RTSB	Rx INT Mask	Interrupt Vector			Priority	DMA Mode Select	

DMA Mode Select [D_0 - D_1]

Setting this field determines whether channel A or B is used in a DMA mode [data transfers are performed by a DMA controller], or in a non-DMA mode where transfers are performed by the processor in either a polled, interrupt, or block transfer mode. The functions of some MPSCC pins are also controlled by this field. See table 3.

Priority [D_2]

This bit selects the relative priorities of the various interrupt and DMA conditions according to the application requirements. See table 4.

Interrupt Vector Mode [D_3 - D_5]

This field determines how the MPSCC responds to an interrupt acknowledge sequence from the processor. See table 5.

Rx INT Mask [D_6]

This option is generally used in the DMA modes. Enabling this bit inhibits the interrupt from occuring when the interrupt/DMA request on first received character mode is selected. In other words, only a DMA request will be generated when the first character is received.

Table 3. DMA Mode Selection

		Channel		Pin Function					
D_1	D_0	A	B	11	26	29	30	31	32
0	0	Non-DMA	Non-DMA	WAITB	DTRB	PRI	PRO	DTRA	WAITA
0	1	DMA	Non-DMA	DRQTxA	HAI	PRI	PRO	HAO	DRQRxA
1	0	DMA	DMA	DRQTXA	HAI	DRQRxB	DRQTxB	HAO	DRQRxA
1	1	DMA	DMA	DRQTxA	DTRB	DRQRxB	DRQTxB	DTRA	DRQRxA

Table 4. DMA/Interrupt Priorities

D_2	Mode		DMA Priority Relation	Interrupt Priority Relation
	Channel A	Channel B		
0	INT	INT		SRxA, RxA > TxA > SRxB, RxB > TxB > ExTA > ExTB
1	INT	INT		SRxA, RxA > SRxB, RxB > TxA > TxB > ExTA > ExTB
0	DMA	INT	RxA > TxA	SRxA, RxA > SRxB, RxB > TxB > ExTA > ExTB
1	DMA	INT	RxA > TxA	SRxA, RxA > SRxB, RxB > TxB > ExTA > ExTB
0	DMA	DMA	RxA > TxA > RxB > TxB	SRxA, RxA > SRxB, RxB > TxB > ExTB
1	DMA	DMA	RxA > RxB > TxA > TxB	SRxA, RxA > SRxB, RxB > ExTA, ExTB

Table 5. Interrupt Acknowledge Sequence Response

D_5	D_4	D_3	Mode	Status Register 2B and Interrupt Vector Bits Affected When Condition Affects Vector is Enabled
0	0	0	Nonvectored	$D_4D_3D_2$
0	0	1	Nonvectored	$D_4D_3D_2$
0	1	0	Nonvectored	$D_2D_1D_0$
0	1	1	Illegal	
1	0	0	8085 Master	$D_4D_3D_2$
1	0	1	8085 Slave	$D_4D_3D_2$
1	1	0	8086	$D_2D_1D_0$
1	1	1	8085/8259A Slave	$D_4D_3D_2$

Pin 10 $\overline{\text{SYNCB}}/\overline{\text{RTSB}}$ Select [D_7]

Programming a zero into this bit selects RTSB as the function of pin 10. A one selects SYNCB as the function.

Control Register 2 (Channel B)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Interrupt Vector							

Interrupt Vector [D_0 - D_7]

When using the MPSCC in the vectored interrupt mode, the contents of this register are placed on the bus during the appropriate portion of the interrupt acknowledge sequence. Its value is modified if status affects vector is enabled. The value of SR2B can be read at anytime. This feature is useful in determining the cause of an interrupt when using the MPSCC in a nonvectored interrupt mode.

Control Register 3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Number of Received Bits per Character		Auto Enables	Enter Hunt Phase	Receiver CRC Enable	Address Search Mode	Sync Character Load Inhibit	Receiver Enable

Receiver Enable [D_0]

Setting this bit to one after the channel has been completely initialized allows the receiver to begin operation. This bit may be set to zero at any time to disable the receiver.

Sync Character Load Inhibit [D_1]

In the character synchronous modes, this bit inhibits the transfer of sync characters to the receiver buffer, thus performing a "sync-stripping" operation. When using the MPSCC's CRC checking ability, use this feature only to strip leading sync characters preceding a message, since the load inhibit does not exclude sync characters embedded in the message from the CRC calculation. Synchronous protocols using other types of block checking such as checksum or LRC are free to strip embedded sync characters.

Address Search Mode [D_2]

In the HDLC mode, setting this bit places the MPSCC in an address search mode. Character assembly does not begin until the 8-bit character (secondary address field) following the starting flag of a message matches either the address programmed into CR6 or the global address 11111111.

Receiver CRC Enable [D_3]

This bit enables and disables (1 = enable) the CRC checker in the character oriented protocol mode, allowing characters from the CRC calculation to be selectively included or excluded. The MPSCC has a one-character delay between the receiver shift register and the CRC checker so that the enabling or disabling takes affect with the last character transferred from the shift register to the receiver buffer. Therefore, there is one full character time in which to read the character and decide whether or not it should be included in the CRC calculation. In the HDLC mode, there is no 8-bit delay.

Enter Hunt Phase [D_4]

Although the MPSCC receiver automatically enters the sync hunt phase after a reset, there are other times when reentry is appropriate. This may occur when synchronization has been lost or, in an HDLC mode, to ignore the current incoming message. A one in this bit position at any time after initialization causes the MPSCC to reeneter the hunt phase.

Auto Enables [D_5]

Setting this bit to one causes the DCD and CTS inputs to act as enable inputs to the receiver and transmitter, respectively.

Number of Received Bits per Character [D_6 - D_7]

This field specifies the number of data bits assembled to make each character. The value may be changed while a character is being assembled and, if the change is made before the new number of bits has been reached, it affects that character. Otherwise, the new specifications take effect on the next character received. See table 6.

Control Register 4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Clock Rate		Sync Mode		Number of Stop Bits per Sync Mode		Parity Even/ Odd	Parity Enable

Parity Enable [D_0]

Setting this bit to one adds an extra data bit containing parity information to each transmitted character. Each received character is expected to contain this extra bit, and the receiver parity checker is enabled.

Table 6. Received Bits per Character

D_7	D_6	Bits per Character
0	0	5
0	1	7
1	0	6
1	1	8

Table 7. Stop Bits

D_3	D_2	Mode
0	0	Synchronous modes
0	1	Asynchronous 1 bit time (1 stop bit)
1	0	Asynchronous 1½ bit times (1½ stop bits)
1	1	Asynchronous 2 bit times (2 stop bits)

Parity Even/Odd [D_1]

Programming a zero into this bit when parity is enabled selects odd parity for the received character. Conversely, a one in this bit selects even parity generation and checking.

Number of Stop Bits or Sync Mode [D_2 - D_3]

This field specifies whether the channel is used in a synchronous or an asynchronous mode. In an asynchronous mode, this field also specifies the number of bit times used as the stop bit length by the transmitter. The receiver always checks for one stop bit. See table 7.

Sync Mode [D_4 - D_5]

When the stop bits/sync mode field is programmed for synchronous modes (D_2, D_3 = 00), this field specifies the particular synchronous format to be used. This field is ignored in an asynchronous mode. See table 8.

Clock Rate [D_6 - D_7]

This field specifies the relationship between the transmitter and receiver clock inputs (TxC, RxC) and the actual data rates at TxD and RxD. When operating in a synchronous mode, a 1x clock rate must be specified. In asynchronous modes, any of the rates may be specified. However, with a 1x clock rate, the receiver cannot determine the center of the start bit. In this mode, the sampling (rising) edge of RxC must be externally synchronized with the data. See table 9.

Table 8. Synchronous Formats

Sync Mode 1 D_5	Sync Mode 2 D_4	Mode
0	0	8-bit internal synchronization character (monosync)
0	1	16-bit internal synchronization character (bisync)
1	0	SDLC/HDLC
1	1	External synchronization (SYNC pin becomes an input)

Table 9. Clock Rates

Clock Rate 1 D_7	Clock Rate 2 D_6	Clock Rate
0	0	Clock Rate = 1x Data Rate
0	1	Clock Rate = 16x Data Rate
1	0	Clock Rate = 32x Data Rate
1	1	Clock Rate = 64x Data Rate

Control Register 5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DTR	Number of Transmitted Bits per Character		Send Break	Transmitter Enable	CRC Polynomial Select	RTS	Transmitter CRC Enable

Transmitter CRC Enable [D_0]

A one or a zero enables or disables (respectively) the CRC generator calculation. The enable or disable does not take effect until the next character is transferred from the transmitter buffer to the shift register, thus allowing specific characters to be included or excluded from the CRC calculation. By setting or resetting this bit just before loading the next character, it and subsequent characters are included or excluded from the calculation. If this bit is zero when the transmitter becomes empty, the MPSCC goes to the idle phase regardless of the state of the idle/CRC latch.

$\overline{RTS}$ [D_1]

In synchronous and HDLC modes, setting this bit to one causes the $\overline{RTS}$ pin to go low, while a zero causes it to go high. In an asynchronous mode, setting this bit to zero causes the $\overline{RTS}$ pin to go high when the transmitter is completely empty. This feature facilitates programming the MPSCC for use with asynchronous modems.

CRC Polynomial Select [D_2]

This bit selects the polynomial used by the transmitter and receiver for CRC generation and checking. A one selects the CRC-16 polynomial ($X^{16} + X^{15} + X^2 + 1$). A zero selects the CRC-CCITT polynomial ($X^{16} + X^{12} + X^5 + 1$). In an HDLC mode CRC-CCITT must be selected. Either polynomial may be used in other synchronous modes.

Transmitter Enable [D_3]

After a reset, the transmitted data output (TxD) is held high (marking) and the transmitter is disabled until this bit is set.

In an asynchronous mode TxD remains high until data is loaded for transmission.

When the transmitter is disabled in an asynchronous mode, any character currently being sent is completed before TxD returns to the marking state.

If the transmitter is disabled during the data phase in a synchronous mode, the current character is sent. TxD then goes high (marking). In an HDLC mode, the current character is sent, but the following marking line is zero-inserted. That is, the line goes low for one bit time out of every five.

Never disable the transmitter during the HDLC data phase unless a reset follows immediately. In either case, any character in the buffer register is held.

Disabling the transmitter during the CRC phase causes the remainder of the CRC character to be bit-substituted with the sync (or flag). The total number of bits transmitted is correct and TxD goes high after they are sent.

If the transmitter is disabled during the idle phase, the remainder of the sync (flag) character is sent. TxD then goes high.

Send Break [D_4]

Setting this bit to one immediately forces the transmitter output (TxD) low (spacing). This function overrides the normal transmitter output and destroys any data being transmitted, although the transmitter is still in operation. Resetting this bit releases the transmitter output.

Transmitted Bits per Character [D_5 - D_6]

This field controls the number of data bits transmitted in each character. The number of bits per character may be changed by rewriting this field just before the first character is loaded. See table 10.

Normally each character is sent to the MPSCC right-justified and the unused bits are ignored. However, when sending five bits or less, the data should be formatted as shown below to inform the MPSCC of the precise number of bits to be sent. See table 11.

Table 10. Transmitted Bits per Character

Transmitted Bits per Character 1 D_6	Transmitted Bits per Character D_5	Bits per Character
0	0	5 or less (see below)
0	1	7
1	0	6
1	1	8

Table 11. Transmitted Bits per Character for 5 Characters or Less

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Number of Bits per Charater
1	1	1	1	0	0	0	D_0	1
1	1	1	0	0	0	D_1	D_0	2
1	1	0	0	0	D_2	D_1	D_0	3
1	0	0	0	D_3	D_2	D_1	D_0	4
0	0	0	D_4	D_3	D_2	D_1	D_0	5

$\overline{DTR}$ [Data Terminal Ready] [D_7]

When this bit is one, the $\overline{DTR}$ output is low [active]. When this bit is zero, $\overline{DTR}$ is high.

Control Register 6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Sync Byte 1							

Sync Byte 1 [D_0 - D_7]

Sync byte 1 is used in the following modes:

Monosync	8-bit sync character transmitted during the idle phase
Bisync	Least significant (first) 8 bits of the 16-bit transmit and receive sync character
External Sync	Sync character transmitted during the idle phase
HDLC	Secondary address value matched to secondary address field of the HDLC frame when the MPSCC is in the address search mode

Control Register 7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Sync Byte 2							

Sync Byte 2 [D_0 - D_7]

Sync byte 2 is used in the following modes:

Monosync	8-bit sync character matched by the receiver
Bisync	Most significant (second) 8 bits of the 16-bit transmit and receive sync characters
HDLC	The flag character 01111110 must be programmed into control register 7 for flag matching by the MPSCC receiver

Status Register 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Break/ Abort	Idle/ CRC	CTS	Sync Status	DCD	Tx Buffer Empty	INT Pending	Rec'd Char Available

Received Character Available [D_0]

When this bit is set, it indicates that one or more characters in the receiver buffer are available for the processor to read. Once the processor has read all the available characters, the MPSCC resets this bit until a new character is received.

Interrupt Pending [D_1 - Channel A Only]

The interrupt pending bit is used with the interrupt vector register (status register 2) to make it easier to determine the MPSCC's interrupt status. This is useful in a nonvectored interrupt mode where the processor must poll each device to determine the interrupt source. In this mode, interrupt pending is set when status register 2B is read, the PRI input is active (low), and the MPSCC requests interrupt service.

It is not necessary to read the status registers of both channels to determine if an interrupt is pending. If the status affects vector is enabled and the interrupt pending is set, the vector read from SR2 contains valid condition information.

In a vectored interrupt mode, interrupt pending is set during the interrupt acknowledge cycle (on the leading edge of the second INTAK pulse) when the MPSCC is the highest priority device requesting interrupt service (PRI is active). In either mode, if there are no other pending interrupt requests, interrupt pending is reset when the end of the interrupt command is issued.

Transmitter Buffer Empty [D_2]

This bit is set whenever the transmitter buffer is empty — except during the transmission of CRC. The MPSCC uses the buffer to facilitate this function. After a reset, the buffer is considered empty and transmit buffer empty is set.

External/Status Flags [D_3 - D_7]

The following status bits reflect the state of the various conditions that cause an external/status interrupt. The MPSCC latches all external/status bits whenever a change occurs that would cause an external/status interrupt, regardless of whether this interrupt is enabled. This allows transient status changes on these lines to be saved.

When operating the MPSCC in an interrupt-driven mode for external/status interrupts, read status register 0 when this interrupt occurs and issue a reset external/status interrupt command to reenable the interrupt and the latches. To poll these bits without interrupts, issue the reset external/status interrupt command to first update the status to reflect the current values.

$\overline{DCD}$ [D_3]: This bit reflects the inverted state of the $\overline{DCD}$ input. When $\overline{DCD}$ is low the $\overline{DCD}$ status bit is high. Any transition on this bit causes an external/status interrupt request.

Sync Status [D_4]: The meaning of this bit depends on the operating mode of the MPSCC.

Asynchronous mode: Sync status reflects the inverted state of the $\overline{SYNC}$ input. When $\overline{SYNC}$ is low, sync status is high. Any transition on this bit causes an external/status interrupt request.

External synchronization mode: Sync status operates in the same manner as in asynchronous mode. The MPSCC's receiver synchronization logic is also tied to the sync status bit in an external synchronization mode. A low-to-high transition ($\overline{SYNC}$ input going low) informs the receiver that synchronization has started and character assembly begins.

A low-to-high transition on the $\overline{SYNC}$ input indicates that synchronization has been lost. The sync status becomes zero and an external/status is generated. The receiver remains in the receive data phase until the enter hunt phase bit in control register 3 is set.

Monosync, bisync, HDLC modes: In these modes, sync status indicates whether the MPSCC receiver is in the sync hunt or receive data phase of operation. A zero indicates that the MPSCC is in the receive data phase, and a one indicates that the MPSCC is in the sync hunt phase (as in after a reset or when the enter sync hunt bit sets to 1). As in the other modes, a transition on this bit causes an external/status interrupt. Note that entering a sync hunt phase (when programmed) or a reset causes an external/status interrupt request which may be cleared immediately with a reset external/status interrupt command.

$\overline{CTS}$ [D_5]: This bit reflects the inverted state of the $\overline{CTS}$ input. When $\overline{CTS}$ is low, the $\overline{CTS}$ status bit is high. Any transition on this bit causes an external/status interrupt request.

Idle/CRC [D_6] [Tx Underrun/EOM]: This bit indicates the state of the idle/CRC latch used in the synchronous mode. After a hardware reset, this bit is set to one, indicating that the transmitter is completely empty. When the MPSCC enters idle phase, it automatically transmits sync or flag characters.

In the HDLC mode, the MPSCC automatically resets this latch after the first byte of a frame is written to the Tx buffer.

When the transmitter is completely empty, the MPSCC sends the 16-bit CRC character and sets the latch again. An external/status interrupt is issued when the latch is set, indicating that CRC is being sent. No interrupt is issued when the latch is reset.

Break/Abort [D_7]: In the asynchronous mode, this bit indicates the detection of a break sequence (a null character plus framing error that occurs when the RxD input is held low, spacing, for more than one character time). Break/abort is reset when RxD returns high (marking).

In the HDLC mode, break/abort indicates the detection of an abort sequence when seven or more ones are received in sequence. It is reset when a zero is received.

Any transition of the break/abort bit causes an external/status interrupt.

Status Register 1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
End of SDLC Frame	CRC Framing Error	Over-run Error	Parity Error	SDLC Residue Code			All Sent

All Sent [D_0]

This bit is set when the transmitter is empty and reset when a character is present in the transmitter buffer or shift register. This feature simplifies the mode control software routines. In the bit synchronous mode, this bit sets when the ending flag pattern is sent.

Residue Code [D_1 - D_3]

Since the data portion of an HDLC message can consist of any number of bits and not necessarily an integral number of characters, the MPSCC has special logic to determine and report when the end of frame flag has been received (that is, the boundary between the data field and the CRC character in the last few data characters that were just read).

When the end of frame condition is indicated (D_7 of status register 1 = 1) and there is a special receive condition interrupt (if enabled), the last bits of the CRC character are in the receiver buffer. The residue code for the frame is valid in the status register 1 byte associated with that data character. (SR1 tracks the received data in its own buffer).

The meaning of the residue code depends upon the number of bits per character specified for the receiver. The previous character refers to the last character read before the end of frame, and so on. See table 12.

Table 12. Residue Codes

8 Bits per Character				
D_3	D_2	D_1	Previous Character	2nd Previous Character
1	0	0	C C C C C C C C	C C C C C D D D
0	1	0	C C C C C C C C	C C C C D D D D
1	1	0	C C C C C C C C	C C C D D D D D
0	0	1	C C C C C C C C	C C D D D D D D
1	0	1	C C C C C C C C	C D D D D D D D
0	1	1	C C C C C C C C*	D D D D D D D D*
1	1	1	C C C C C C C D	D D D D D D D D
0	0	0	C C C C C C D D	D D D D D D D D

7 Bits per Character				
D_3	D_2	D_1	Previous Character	2nd Previous Character
1	0	0	C C C C C C C	C C C C C D D
0	1	0	C C C C C C C	C C C C D D D
1	1	0	C C C C C C C	C C C D D D D
0	0	1	C C C C C C C	C C D D D D D
1	0	1	C C C C C C C	C D D D D D D
0	1	1	C C C C C C C*	D D D D D D D*
0	0	0	C C C C C C D	D D D D D D D

6 Bits per Character				
D_3	D_2	D_1	Previous Character	2nd Previous
1	0	0	C C C C C C	C C C C C D
0	1	0	C C C C C C	C C C C C D
1	1	0	C C C C C C	C C C D D D
0	0	1	C C C C C C	C C D D D D
1	0	1	C C C C C C	C D D D D D
0	0	0	C C C C C C	D D D D D D

5 Bits per Character				
D_3	D_2	D_1	Previous Character	2nd Previous
1	0	0	C C C C C*	D D D D D*
0	1	0	C C C C D	D D D D D
1	1	0	C C C D D	D D D D D
0	0	1	C C D D D	D D D D D
0	0	0	C D D D D	D D D D D

Notes: C = CRC bit
D = Valid data
* = No residue

Special Receive Condition Flags

The status bits described below—parity error (if parity as a special receive condition is enabled), receiver overrun error, CRC/framing error, and end of HDLC frame—all represent special receive conditions.

When any of these conditions occur and interrupts are enabled, the MPSCC issues an interrupt request. In addition, if a condition affect vector mode is enabled, the vector generated (and the contents of SR2B for nonvectored interrupts) is different from that of a received character available condition. Therefore, it is not necessary to analyze SR1 with each character to determine if an error has occurred.

Also, the parity error and receiver overrun error flags are latched. That is, once one of these errors occurs, the flag remains set for all subsequent characters until reset by the error reset command. Therefore read SR1 only at the end of a message to determine if either of these errors occurred anywhere in the message. The other flags are not latched and follow each character available in the receiver buffer.

Parity Error [D_4]: This bit is set and latched when parity is enabled and the received parity bit does not match the sense (odd or even) calculated from the data bits.

Receiver Overrun Error [D_5]: This error occurs and is latched when the receiver buffer already contains three characters and a fourth character is completely received, overwriting the last character in the buffer.

CRC/Framing Error [D_6]: In the asynchronous mode a framing error is flagged (but not latched) when no stop bit is detected at the end of a character (RxD is low one bit time after the center of the last data or parity bit). When this condition occurs, the MPSCC waits an additional one-half bit time before sampling again so that the framing error is not interpreted as a new start bit.

In the synchronous mode, this bit indicates the result of the comparison between the current CRC result and the appropriate check value. It is usually set to one, since a message rarely indicates a correct CRC result until correctly completed with the CRC check character. Note that a CRC error does not result in a special receive condition interrupt.

End of HDLC Frame [EOF] [D_7]: This status bit is used only in the bit synchronous mode to indicate that the end of frame flag has been received and that the CRC error flag and residue code are valid. This flag can be reset at any time by issuing an error reset command. The MPSCC also automatically resets this bit when the first character of the next message is sent.

Status Register 2B

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Interrupt Vector							

Interrupt Vector [D_0 - D_7 - Channel B Only]

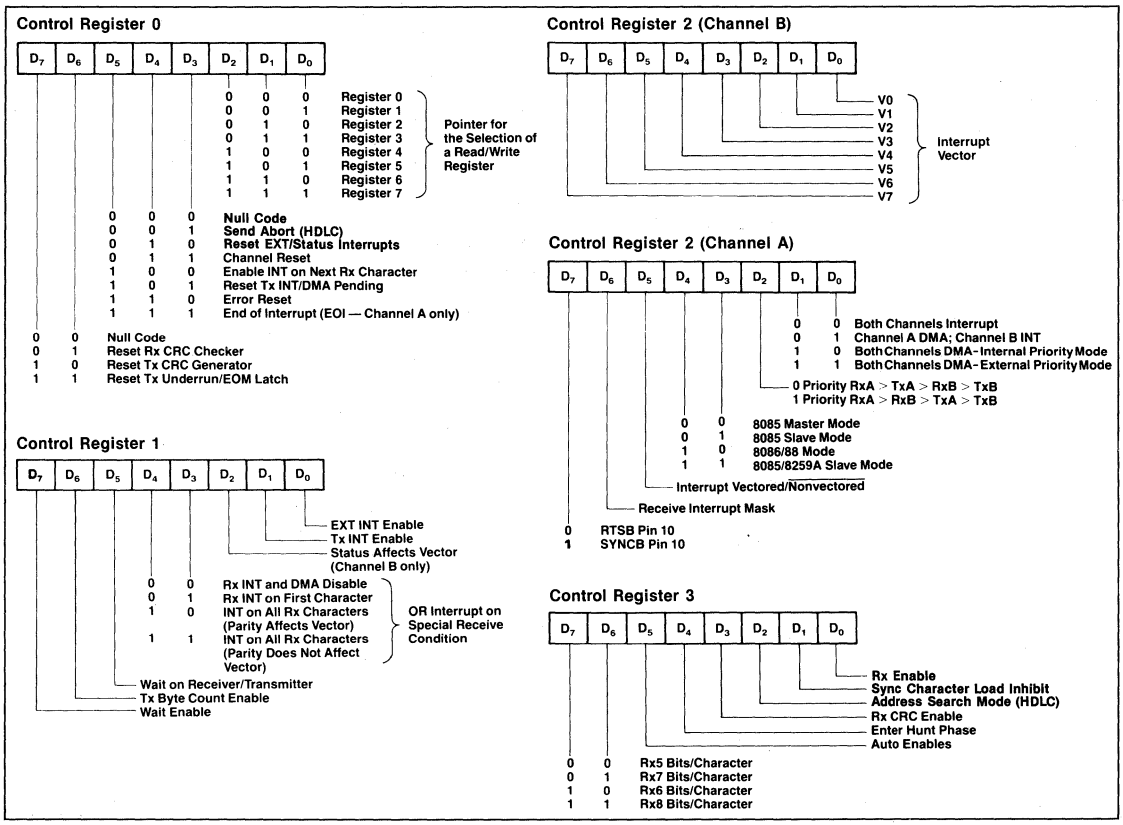
Reading status register 2B returns the interrupt vector that is programmed into control register 2B. If a condition affects vector mode is enabled, the value of the vector is modified as shown in table 13.

Code 111 can mean either channel A special receive condition or no interrupt pending. Examine the interrupt pending bit (D_1 of status register 0, channel A), to distinguish which it means. In a nonvectored interrupt mode, the vector register must be read first for the interrupt pending to be valid.

Table 13. Condition Affects Vector Modifications

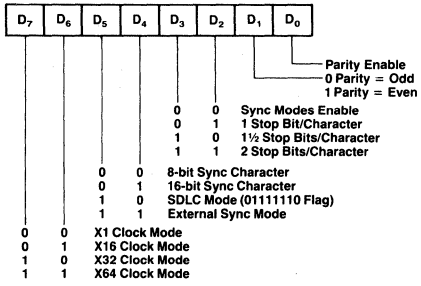
Interrupt Pending (SRO, D_1 Channel A)	8085 Modes / 8086 Modes	D_4 / D_2	D_3 / D_1	D_2 / D_0	Condition
0		1	1	1	No interrupt pending
1		0	0	0	Channel B transmitter buffer empty
1		0	0	1	Channel B external/status Change
1		0	1	0	Channel B received character available
1		0	1	1	Channel B special receive condition
1		1	0	0	Channel A transmitter buffer empty
1		1	0	1	Channel A external/status change
1		1	1	0	Channel A received Character available
1		1	1	1	Channel A special receive condition

Status Register Bit Functions (Sheet 1 of 2)

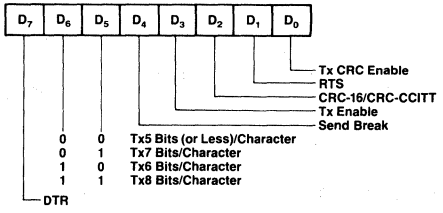


Status Register Bit Functions (Sheet 2 of 2)

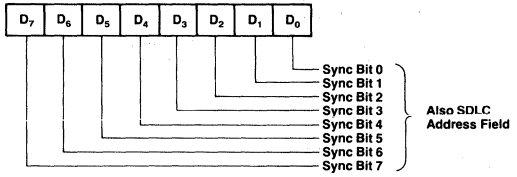
Control Register 4



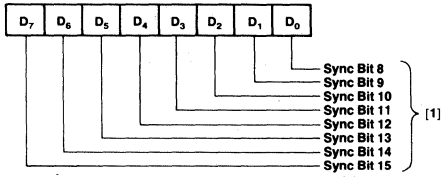
Control Register 5



Control Register 6



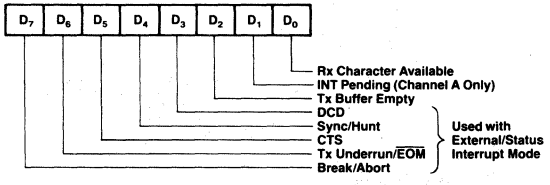
Control Register 7



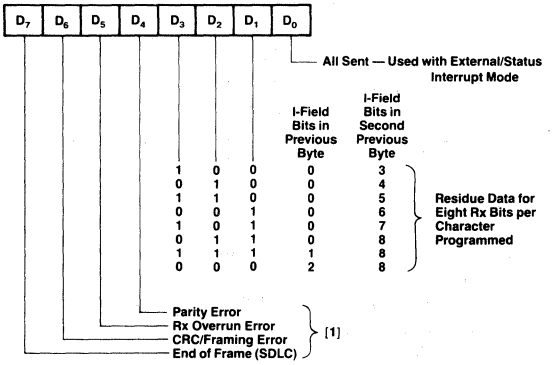
Note:

[1] For SDLC it must be programmed to 01111110 for flag recognition.

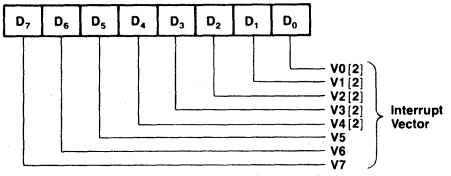
Status Register 0



Status Register 1



Status Register 2B

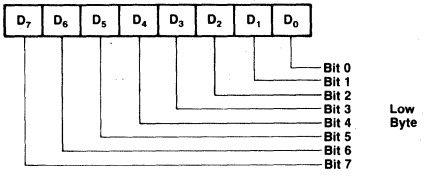


Note:

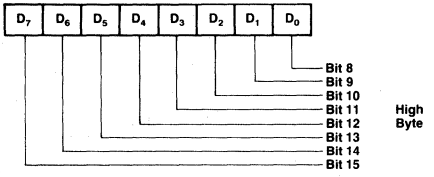
[1] Used with special receive condition mode.

[2] Variable if Status Affects Vector is programmed.

Status Register 3 (Tx Byte Count Register)



Status Register 4 (Tx Byte Count Register)



μPD72001
CMOS, Advanced Multiprotocol, Serial Communications Controller

Description

The μPD72001 advanced multiprotocol serial controller (AMPSC) is a high-performance, single-chip, serial communications controller designed to meet a wide variety of communications requirements. The AMPSC contains two independent full-duplex channels which can be configured to transmit and receive data in either asynchronous protocol or one of two synchronous protocols: character-oriented protocol (COP) or bit-oriented protocol (BOP). The COP and BOP synchronous protocols include cyclic redundancy check (CRC) generation and checking.

The AMPSC has several interrupt modes, including vectored and nonvectored. Separate direct memory access (DMA) requests are available for the transmitter and receiver on each channel, allowing high speed operation. The AMPSC is easily interfaced to most microprocessors with a minimum of logic.

The μPD72001 AMPSC is an upgraded CMOS version of the μPD7201A MPSCC with the following additions: four internal baud rate generator (BRG)/timers, two digital phase-locked loops (DPLL), two crystal oscillators, and the capability of synchronous data link control (SDLC) loop operation. The BRG's can be used as independent timers, when they are not being used as baud rate generators. Each timer generates its own zero count interrupt. These features simplify design requirements and at the same time enhance the flexible architecture of the μPD7201A.

Features

- ☐ Advanced version of the μPD7201A
- ☐ Functional superset of industry standard 8530
- ☐ CMOS technology
- ☐ Multiprotocol
  - — Asynchronous
  - — Synchronous
  - — Character-oriented (BISYNC/MONO-SYNC)
  - — Bit-oriented (SDLC/HDLC)
- ☐ Two independent full-duplex channels
- ☐ Versatile host-system interface
  - — Software polling
  - — Interrupt
  - — DMA
- ☐ Interface to a majority of microprocessors (V-Series, 8080, 8085, 80X86/88, and others)
- ☐ DC to 2.2-Mb/s data rate
- ☐ Modem control signals
- ☐ NRZ, NRZI, and FM encoding/decoding, Manchester decoding
- ☐ Digital phase-locked loop per channel
- ☐ Two baud rate generator/timers per channel (receive and transmit)
- ☐ Crystal oscillator per channel
- ☐ Loopback test mode
- ☐ SDLC loop mode
- ☐ Mark idle detection
- ☐ Short frame detection
- ☐ Single +5 V power supply
- ☐ Standby mode for reduced power consumption
- ☐ Two speed versions: 8 MHz and 11 MHz systems and input data clocks
- ☐ Available in DIP, PLCC, and quadflat packages

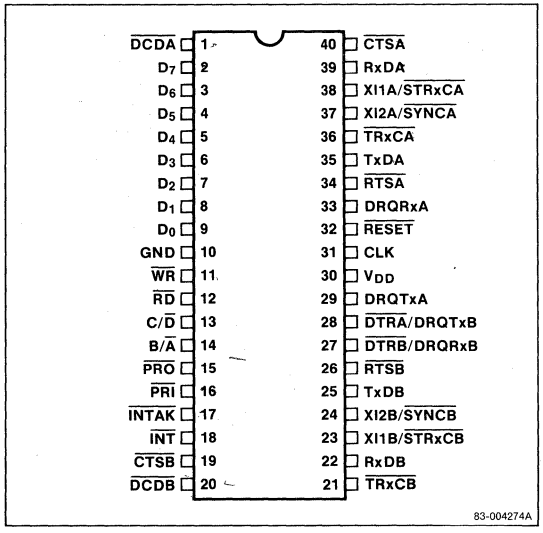
2

Ordering Information

Part No.	Package Type	Max Clock Speed
μPD72001C	40-pin plastic DIP	8 MHz
μPD72001C-11	40-pin plastic DIP	11 MHz
μPD72001GC-3B6	52-pin plastic miniflat	8 MHz
μPD72001GC-3B6-11	52-pin plastic	11 MHz
μPD72001L	52-pin plastic leaded chip carrier (PLCC)	8 MHz
μPD72001L-11	52-pin plastic leaded chip carrier (PLCC)	11 MHz

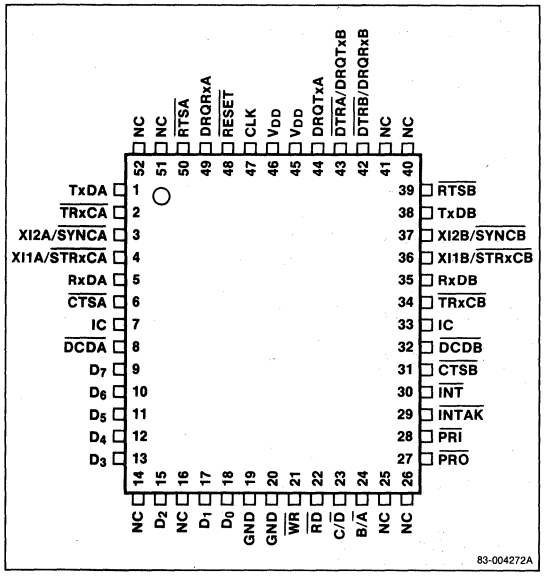
Pin Configurations

40-Pin Plastic DIP

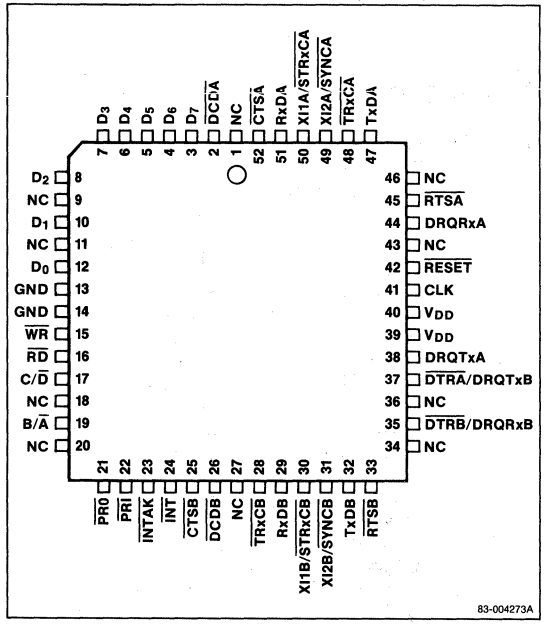


Pin Configurations (cont)

52-Pin Plastic Miniflat



52-Pin Plastic Leaded Chip Carrier (PLCC)



Pin Identification

Symbol	Function
B/$\overline{A}$	Channel B or channel A select input from host computer
C/$\overline{D}$	Control/data input select from host computer
CLK	System clock input from host computer
$\overline{CTSA}$	Clear-to-send input for channel A
$\overline{CTSB}$	Clear-to-send input for channel B
$\overline{DCDA}$	Data carrier detect input for channel A
$\overline{DCDB}$	Data carrier detect input for channel B
$\overline{DTRA}$/DRQTxB	Data terminal ready output for channel A or DMA request output for transmit channel B; determined by control register CR2A
$\overline{DTRB}$/DRQRxB	Data terminal ready output for channel B or DMA request output for receive channel B; determined by control register CR2A
DRQRxA	DMA request output for receive channel A
DRQTxA	DMA request output for transmit channel A
D_7-D_0	System data bus
$\overline{INT}$	Interrupt request output to host computer
$\overline{INTAK}$	Interrupt acknowledge input from host computer
$\overline{PRI}$	Priority input, interrupt daisy chain control
$\overline{PRO}$	Priority output, interrupt daisy chain control
$\overline{RD}$	Read control input from host computer
$\overline{RESET}$	System reset input from host computer
$\overline{RTSA}$	Request-to-send output for channel A
$\overline{RTSB}$	Request-to-send output for channel B
RxDA	Receive data input for channel A
RxDB	Receive data input for channel B
$\overline{TRxCA}$	Transmit-receive clock input for channel A
$\overline{TRxCB}$	Transmit-receive clock input for channel B
TxDA	Transmit data output for channel A
TxDB	Transmit data output for channnel B
$\overline{WR}$	Write control input from host computer
XI1A/$\overline{STRxCA}$	External crystal connection for channel A or transmit-receive clock source input for channel A
XI2A/$\overline{SYNCA}$	External crystal connection for channel A or synchronization input for channel A
XI1B/$\overline{STRxCB}$	External crystal connection for channel B or transmit-receive clock source input for channel B
XI2B/$\overline{SYNCB}$	External crystal connection for channel B or synchronization input for channel B
GND	System ground
V_{DD}	+5 V (typical)

Pin Functions

CPU Interface

B/$\overline{A}$ [Channel Select]. The input to this pin selects the channel to be accessed for a write or read operation. A low input selects channel A; a high input selects channel B.

C/$\overline{D}$ [Control/Data Select]. The input to this pin selects the type of data on the data bus during a write or read access. A low input selects data; a high input selects a control or status register.

CLK [System Clock]. This input supplies the clock for the internal operation of the device. It is separate from the data clocks. The system clock input must be more than five times the serial data transfer rate.

$\overline{INT}$ [Interrupt]. The interrupt request output signal at this pin goes low if an interrupt cause occurs within the AMPSC. The output is an open-drain transistor and requires a pull-up resistor.

$\overline{INTAK}$ [Interrupt Acknowledge]. An active-low input signal at this pin is used in response to an interrupt request. In the Vector mode (CR2A bit D7 = 1), it causes the interrupt vector to be placed on the data bus. The output vector mode determines the number of cycles of $\overline{INTAK}$ toggling that are required for each interrupt acknowledge cycle (see CR2A bits D3-D5). In the Nonvector mode (D7 = 0), this pin must be pulled high. If unused, this pin must also be pulled high.

$\overline{PRI}$ [Priority Input]. The $\overline{PRI}$ signal controls interrupt request generation and interrupt vector output. The pin is the input for the interrupt priority daisy chain that determines how interrupts from multiple devices are resolved. A high level prevents the AMPSC from presenting an interrupt vector during the INTAK sequence. A low level allows the vector to be presented. If unused, this pin must be tied low.

$\overline{PRO}$ [Priority Output]. This is an output to the interrupt priority daisy chain. It controls interrupt requests from lower-priority devices. It indicates the existence of a higher-priority interrupt, either within the AMPSC or, if no internal interrupt exists, the condition of the $\overline{PRI}$ input.

$\overline{RESET}$ [Reset]. Applying a low signal continuously for two or more clock cycles (t_{CYK}) to this pin resets the AMPSC (system reset) and places it in Standby mode. A system reset disables the transmitter, receiver, interrupt, and DMA functions and sets the TxD and general-purpose output pins to high. It also resets all bits of the control registers.

$\overline{RD}$ [Read]. The active-low $\overline{RD}$ input signal causes status or receive (Rx) data to be read out of the AMPSC. The data is presented on pins D_0-D_7. The values are dependent on the state of the B/$\overline{A}$ and C/$\overline{D}$ inputs and the internal state of the device.

$\overline{WR}$ [Write]. The active-low $\overline{WR}$ input signal causes control words or transmit (Tx) data to be written into the AMPSC. The data written is input on pins D0-D7 (data bus). The destination of the data is determined by the state of the B/$\overline{A}$ and C/$\overline{D}$ pins and the value of the internal register pointer.

D_7-D_0 [Data Bus]. These pins constitute a three-state, 8-bit, bidirectional data bus. The bus is connected to the host processor's data bus to transfer control words, status information, and send/receive data.

Channel Interface

RxDA, RxDB [Receive Data]. Receive data enters the AMPSC on these pins.

TxDA, TxDB [Transmit Data]. Transmit data exits the AMPSC on these pins.

DRQTxA, DRQTxB [DMA Transmit Requests]. These active-high outputs for channels A and B are DMA requests to the DMA controller. The pin is set to high when the Tx buffer is emptied. The conditions under which this occurs depend on the status of control register CR1 bit D2. (DRQTxB and $\overline{DTRA}$ are dual functions of the same pin.)

DRQRxA, DRQRxB [DMA Receive Requests]. These active-high outputs for channels A and B are DMA requests to the DMA controller. The pin is set to high when the receiver enters the Rx Character Available state. It is reset when received data is read out of the channel. (DRQRxB and $\overline{DTRB}$ are dual functions of the same pin.)

$\overline{TRxCA}$, $\overline{TRxCB}$ [Transmit/Receive Clock]. If bit D2 of control register CR15 is zero, these pins are transmit or receive clock inputs. Also, they are inputs if bits D5 and D6 or D3 and D4 are set to one and zero, respectively, overriding the state of bit D2.

If none of the conditions above are true, the pins function as outputs with the source selectable between the crystal oscillator, the BRG, the DPLL, and the transmit clock. Selection is made with bits D0 and D1 of CR15.

$\overline{STRxCA}$, $\overline{STRxCB}$ [Clock Source]. These pins are the transmit or receive clock source inputs for channels A and B, respectively. They can be routed internally to the transmitter, receiver, BRG's, or DPLL. An alternative function as an external crystal connection point (XI) is selected by control register CR15 bit D7.

XI1A, XI2A and XI1B, XI2B [Crystal Connections]. These two pin pairs may be connected to external crystals that control the internal oscillators for channels A and B, respectively. (See $\overline{\text{STRxCA}}$ and $\overline{\text{STRxCB}}$.)

Modem Control

RTSA, RTSB [Request to Send]. These are general-purpose outputs usable, as an example, for modem control. Pin status is set by CR5 bit 01 and Auto Enable bit status (CR3 bit D5).

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$ [Clear to Send]. These are general-purpose inputs usable, as an example, for modem control. A status change on $\overline{\text{CTSA}}$ or $\overline{\text{CTSB}}$ affects E/S bit latch operation. If E/S INT is enabled (CR1 bit D0 set to 1), an E/S interrupt occurs. If the Auto Enable mode is selected (CR3 bit D5 set to 1), $\overline{\text{CTSA}}$ and $\overline{\text{CTSB}}$ can be used with the Tx Enable bit (CR5 bit D3) to control transmitter operation.

$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$ [Data Carrier Detect]. These are general-purpose inputs usable, as an example, for modem control. A status change on $\overline{\text{DCDA}}$ or $\overline{\text{DCDB}}$ affects E/S bit latch operation. If E/S INT is enabled (CR1 bit D0 set to 1), an E/S interrupt occurs. If the Auto Enable mode is selected (CR3 bit D5 set to 1), $\overline{\text{DCDA}}$ and $\overline{\text{DCDB}}$ can be used with the Rx Enable bit (CR3 bit D0) to control receiver operation.

$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$ [Data Terminal Ready]. These are general-purpose active-low outputs controlled by control register CR5A bit D7. (DRQTxB and DRQRxB have dual pin functions with $\overline{\text{DTRA}}$ and $\overline{\text{DTRB}}$.)

$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$ [Sync Input or Output]. In accordance with the settings of control regsister CR4 bits D7-D2, and with CR15 bit D7 = 0, the three functions of these pins are as follows.

(1) Asynchronous mode: general-purpose input that functions like $\overline{\text{DCD}}$ and $\overline{\text{CTS}}$.

(2) External sync mode: active-low input indicates to the AMPSC that synchronization has occurred.

(3) Internal sync mode: active-low output indicates when synchronization is detected by the AMPSC.

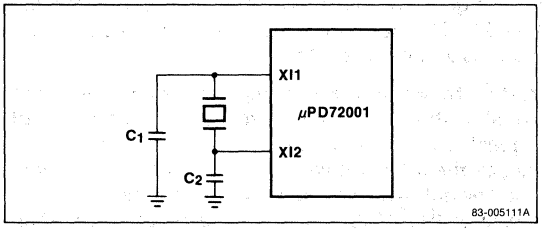
Crystal Recommendations

The crystals used with the μPD72001 internal crystal oscillators should be parallel resonant, fundamental mode, with an AT cut. For frequency stability, two capacitors can be added from the pins of the crystal to ground (figure 1). The value of the capacitors can be calculated by the following formula:

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_S$$

C_L is the load capacitance of the crystal and C_S is all stray capacitance in parallel with the crystal. The C_S value should include the input capacitance (C_{IO} and C_{IN}) of the μPD72001 and any wiring or socket capacitance.

Figure 1. Crystal Configuration Circuit



Absolute Maximum Ratings

$T_A = +25°C$

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_i	−0.5 to V_{DD} + 0.5 V
Output voltage, V_O	−0.5 to V_{DD} + 0.5 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

DC Characteristics

T_A = −10 to +70°C; V_{DD} = + 5 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	−0.5		+0.8	V	All pins except CLK
	V_{ILC}	−0.5		+0.6	V	CLK pin
Input high voltage	V_{IH}	+2.2		V_{DD} + 0.5	V	All pins except CLK
	V_{IHC}	+3.3		V_{DD} + 0.5	V	CLK pin
Output low voltage	V_{OL}			+0.45	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	0.7 V_{DD}			V	I_{OH} = −400 μA
Output leakage current, high	I_{LOH}			+10	μA	V_{OUT} = V_{DD}
Output leakage current, low	I_{LOL}			−10	μA	V_{OUT} = 0 V
Input leakage current, high	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input leakage current, low	I_{LIL}			−10	μA	V_{IN} = 0 V
V_{DD} supply current	I_{DD}		20	40	mA	All outputs at high level; t_{CY} = 0.125 μs
Standby current	I_{DDI}		1	20	μA	f_{RxC} = f_{TxC} = f_{CLK} = DC
			1	2	mA	Standby mode

Capacitance

T_A = 25°C; V_{DD} = 0 V

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Input capacitance	C_{IN}		10	pF	f_C = 1 MHz; unmeasured pins returned to 0 V.
I/O capacitance	C_{IO}		20	pF	

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Limits, 8 MHz Min	Max	Limits, 11 MHz Min	Max	Unit	Test Conditions
Clock							
Clock cycle (Note 1)	t_{CYK}	125	2000	91	2000	ns	
Clock high level width	t_{WKH}	50	1000	40	1000	ns	
Clock low-level width	t_{WKL}	50	1000	40	1000	ns	
Clock rise time	t_{KR}		10		10	ns	1.5 to 3.0 V
Clock fall time	t_{KF}		10		10	ns	3.0 to 1.5 V

Notes:

(1) In all modes, the system clock frequency must be more than five times the maximum data rate.

AC Characteristics (cont)

Parameter	Symbol	Limits, 8 MHz Min	Limits, 8 MHz Max	Limits, 11 MHz Min	Limits, 11 MHz Max	Unit	Test Conditions
Read Cycle							
Address setup time to $\overline{RD}\downarrow$	t_{SAR}	0		0		ns	
Address hold time from $\overline{RD}\uparrow$	t_{HRA}	0		0		ns	
$\overline{RD}$ pulse width	t_{WRL}	150		150		ns	
Data output delay time from address	t_{DAD}		120		120	ns	
Data output delay time from $\overline{RD}\downarrow$	t_{DRD}		120		120	ns	
Data float delay time from $\overline{RD}\uparrow$	t_{FRD}	10	85	10	85	ns	
Write Cycle							
Address setup time to $\overline{WR}\downarrow$	t_{SAW}	0		0		ns	
Address hold time from $\overline{WR}\uparrow$	t_{HWA}	0		0		ns	
$\overline{WR}$ pulse width	t_{WWL}	150		150		ns	
Data setup time to $\overline{WR}\uparrow$	t_{SDW}	120		120		ns	
Data hold time from $\overline{WR}\uparrow$	t_{HWD}	0		0		ns	
Read/Write Cycle							
$\overline{RD}/\overline{WR}$ recovery time (Note 2)	t_{RV}	160		160		ns	
Transmit or Receive Cycle							
Transmit/receive data cycle	t_{CYD}	5		5		t_{CYK}	
$\overline{STRxC}$, $\overline{TRxC}$ input clock cycle	t_{CYC}	125		91		ns	
$\overline{STRxC}$, $\overline{TRxC}$ input clock pulse							
High-level width	t_{WCH}	50		40		ns	
Low-level width	t_{WCL}	50		40		ns	
Transmit Cycle							
TxD delay time from $\overline{STRxC}\downarrow$, $\overline{TRxC}\downarrow$	t_{DTCTD1}		100		100	ns	x1 mode
	t_{DTCTD2}		300		300	ns	x16, x32, x64 mode
$\overline{INT}$ delay time from TxD	t_{DTDIQ}	4	6	4	6	t_{CYK}	Tx INT mode
DRQTx delay time from TxD	t_{DTDDQ}	4	6	4	6	t_{CYK}	Tx DMA mode

Notes [cont]:

(2) For all operations except Tx/Rx data transfer

AC Characteristics (cont)

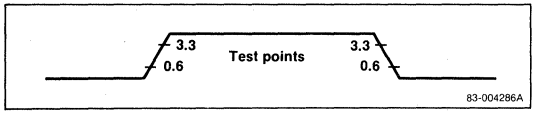
Parameter	Symbol	Limits, 8 MHz Min	Limits, 8 MHz Max	Limits, 11 MHz Min	Limits, 11 MHz Max	Unit	Test Conditions
Receive Cycle							
RxD setup time to $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑	t_{SRDRC}	0		0		ns	
RxD hold time from $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑	t_{HRCRD}	140		140		ns	
INT delay time from $\overline{RxC}$ ↑ (Note 3)	t_{DRCIQ}	7	11	7	11	t_{CYK}	Rx IN mode
DRQRx delay time from $\overline{RxC}$ ↑ (Note 3)	t_{DRCDQ}	7	11	7	11	t_{CYK}	Rx DMA mode
DMA Request Control							
DRQRx ↓ request delay time from $\overline{RD}$ ↓	t_{DRDQ}		120		120	ns	
DRQTx ↓ request delay time from $\overline{WR}$ ↓	t_{DWDQ}		120		120	ns	
Interrupt Control							
$\overline{INTAK}$ low-level width	t_{WIAL}	150		150		ns	
$\overline{PRO}$ delay time from $\overline{PRI}$	t_{DPIPO}		50		50	ns	
$\overline{PRI}$ setup time to $\overline{INTAK}$ ↓	t_{SPIIA}	0		0		ns	When vector output is selected.
PRI hold time from $\overline{INTAK}$ ↑	t_{HIAPI}	20		20		ns	
Data output delay time from $\overline{INTAK}$ ↓	t_{DIAD}		120		120	ns	
Data float delay time from $\overline{INTAK}$ ↑	t_{FIAD}	10	85	10	85	ns	
Modem Control							
$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse							
High-level width	t_{WMH}	2		2		t_{CYK}	
Low-level width	t_{WML}	2		2		t_{CYK}	
INT delay time from $\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$	t_{DMIQ}		2		2	t_{CYK}	
Sync Control							
$\overline{SYNC}$ delay $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑	t_{DTRCSY}	0	2	0	2	t_{CYK}	COP external synchronization
Crystal Oscillator							
XI1 input cycle time	t_{CYX}	125	1000	91	1000	ns	
Reset							
$\overline{RESET}$ pulse width	t_{WRSL}	2		2		t_{CYK}	

Notes [cont]:

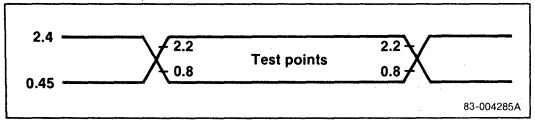
(3) $\overline{STRxC}$ or $\overline{TRxC}$, whichever is used for the receive clock

Timing Waveforms

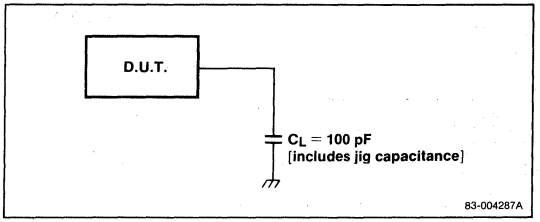
Clock Input Test Points



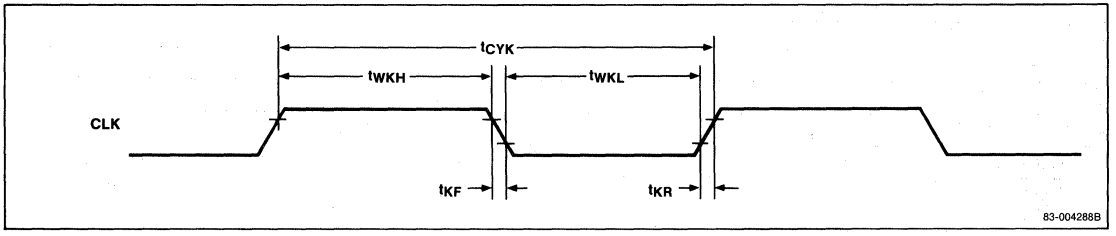
I/O Waveform Test Points



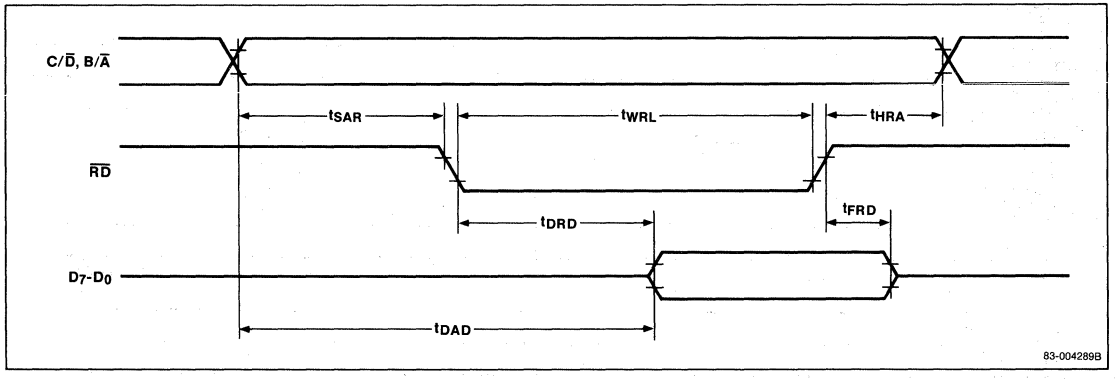
AC Test Load Circuit



Clock Timing

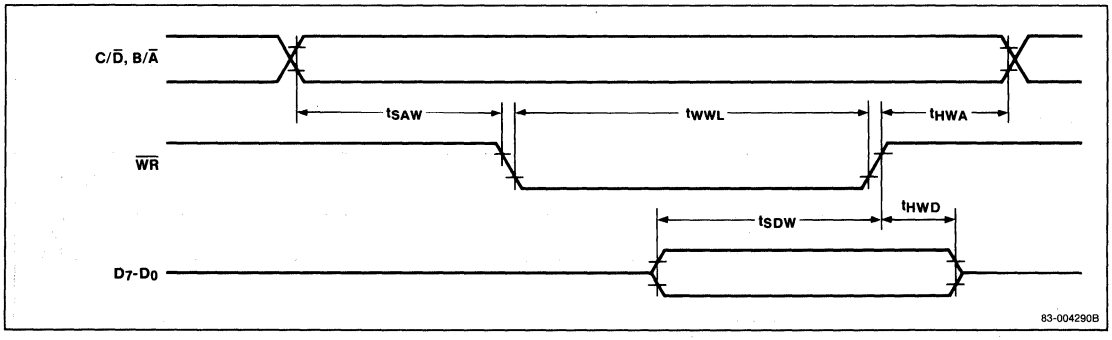


Read Cycle

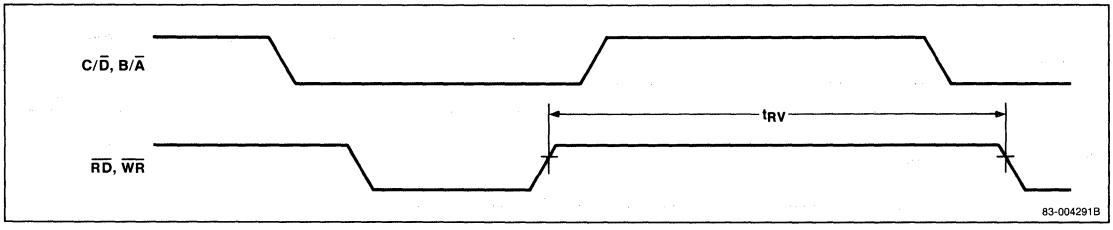


Timing Waveforms (cont)

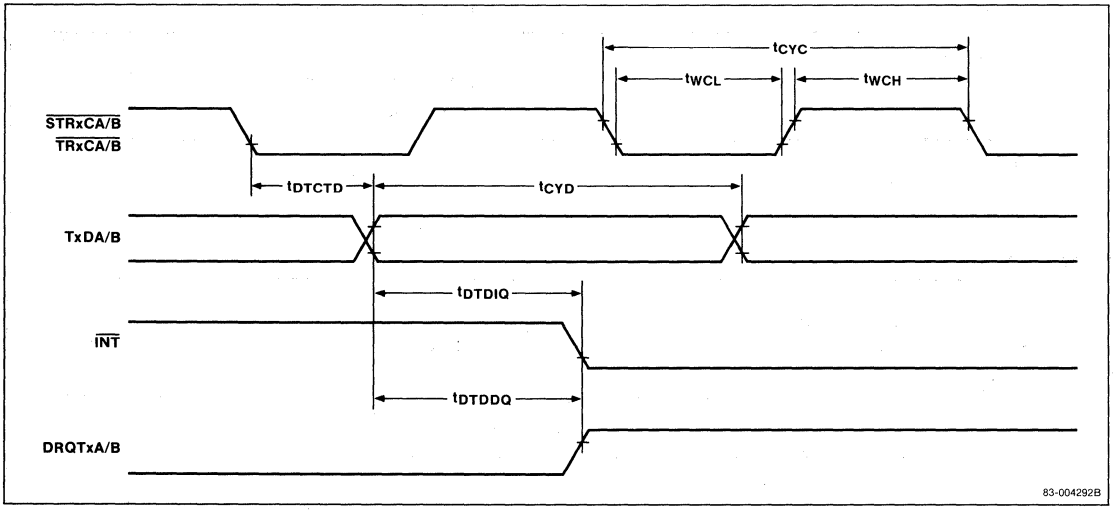
Write Cycle



Read/Write Cycle (for all operations except Tx/Rx data transfer)

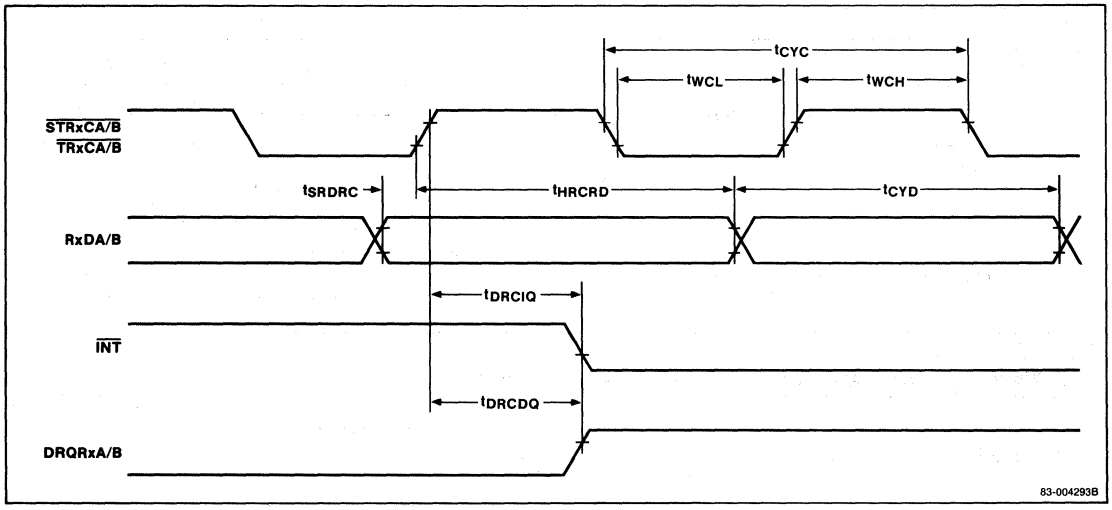


Transmit Cycle

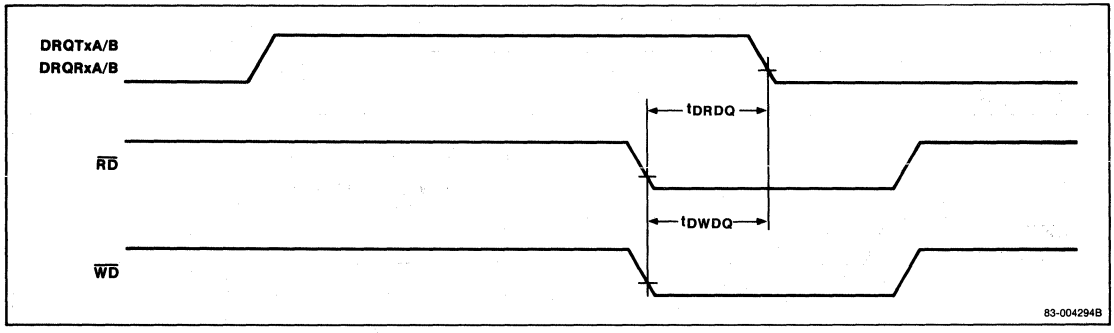


Timing Waveforms (cont)

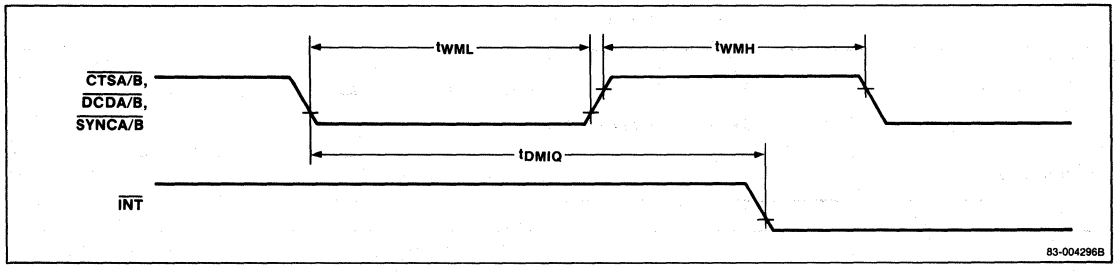
Receive Cycle



DMA Request Control

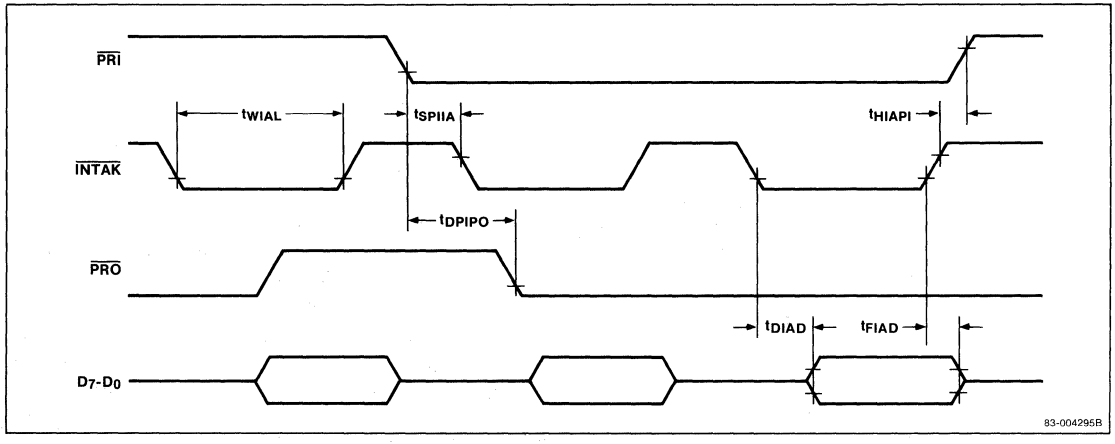


Modem Control

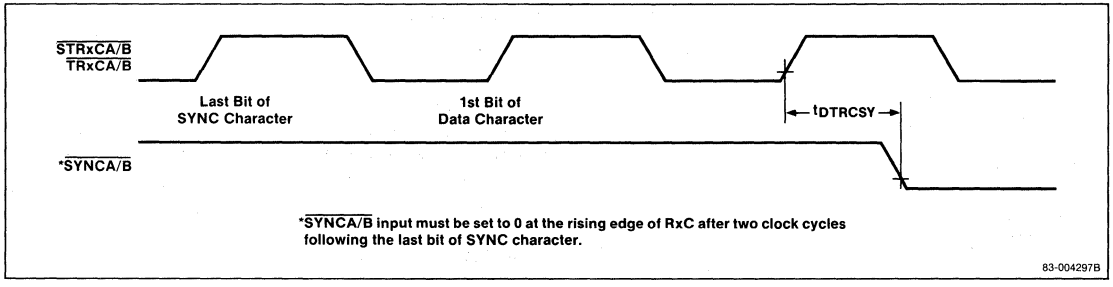


Timing Waveforms (cont)

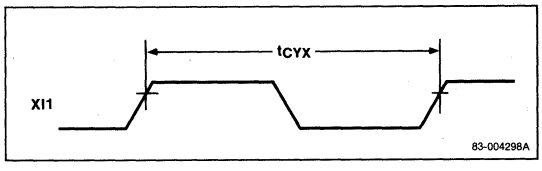
Interrupt Control



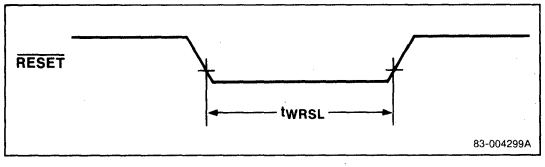
Sync Control



Crystal Oscillator



Reset



Functional Operation

Refer to the μPD72001 AMPSC block diagram (figure 2) for an overview of the four major functional blocks of logic listed below.

- System clock control
- Interface control
- Transmitter
- Receiver

System Clock Control

The system clock control logic receives and manages the system clock (CLK), which operates the internal circuitry of the μPD72001. The system clock and internal circuitry must be operating in order for the transmitters and receivers of the μPD72001 to function. In standby mode, the system clock is blocked by the clock control circuitry and the transmitters and receivers can not operate. In clocked operation, the system clock can be used as the source for the data clock, which is used by the transmitters and receivers.

The internal registers of the μPD72001 are static in nature and do not require the system clock to retain their contents.

Interface Control

The interface control logic contains the signals used to control the transfer of data and status information between the host CPU and the AMPSC. This logic block has four types of interface lines. The read/write and control lines ($\overline{RD}$, $\overline{WR}$, C/$\overline{D}$, B/$\overline{A}$) select what data is to be transferred and the direction of the transfer. The reset line ($\overline{RESET}$) which is part of this group, resets the internal state of the μPD72001 when held active. The interrupt control line ($\overline{INT}$) sends a signal to the host CPU when the AMPSC requires attention. The interrupt acknowledge line ($\overline{INTAK}$) signals the μPD72001 when the host CPU is ready to service its request for attention. The interrupt priority lines ($\overline{PRI}$, $\overline{PRO}$) are used to form the interrupt priority daisy chain, which arbitrates the interrupt service priority.

The DMA control lines (DRQRxA, DRQTxA, DRQRxB, DRQTxB), inform the DMA controller when a data transfer is ready. The data bus buffer provides temporary storage of the data (D7-D0) being transferred from the internal registers of the μPD72001 to the host CPU.

Transmitter

Each channel's transmitter accepts parallel byte data and sends it out serially. The data is sent out at a rate determined by the transmit data clock (TxCLK). The source of this clock is determined by the clock control multiplexer. Bytes are loaded into the transmit buffer. When the transmit shift register is empty, the contents of the transmit buffer are loaded into the transmit shift register.

The transmitter is also responsible for the transmit CRC calculation and sending flags and sync characters. The transmitter can be made to send breaks and aborts using commands from the host CPU.

The internal loopback feature connects the transmitter to the receiver and disconnects the receiver from the RxD pin.

The echo loop feature connects the receiver to the TxD pin and disconnects the transmitter.

The Baud Rate Generators (BRGs) divide down the selected clock source to produce data clocks that can be used for the transmitter and receiver. The clock multiplexer selects the clock sources for them. By selecting the correct value for the BRG count, the BRG can be used as a timer with a wide dynamic range. The clock source for the timer can be selected from the system clock, the data clock, an external source, or a crystal.

Receiver

The receivers in the AMPSC accept serial data into the receive shift register, which in turn assembles this serial data into parallel characters (byte). The assembled byte is transferred into the receive buffer (FIFO), which can contain up to three bytes. The receive status of each byte is transferred along with it through the receive buffer. In this way, the status reported by the μPD72001 is always current for the byte that is about to be removed from the FIFO.

The receive shift register also checks for flags and sync characters in the synchronous modes. Flags are automatically removed from the data stream, while sync characters have the option of being retained. This is determined by a CPU command.

The receiver in synchronous modes, calculates the received CRC and checks it against the CRC that is received with the data. A difference is reported to the host processor.

The digital phase-locked loop (DPLL) is used to separate the data from the clocking information in the NRZI, FM, and Manchester encoded received bit streams. It locks in on the received data and provides an accurate and stable clock for the receiver.

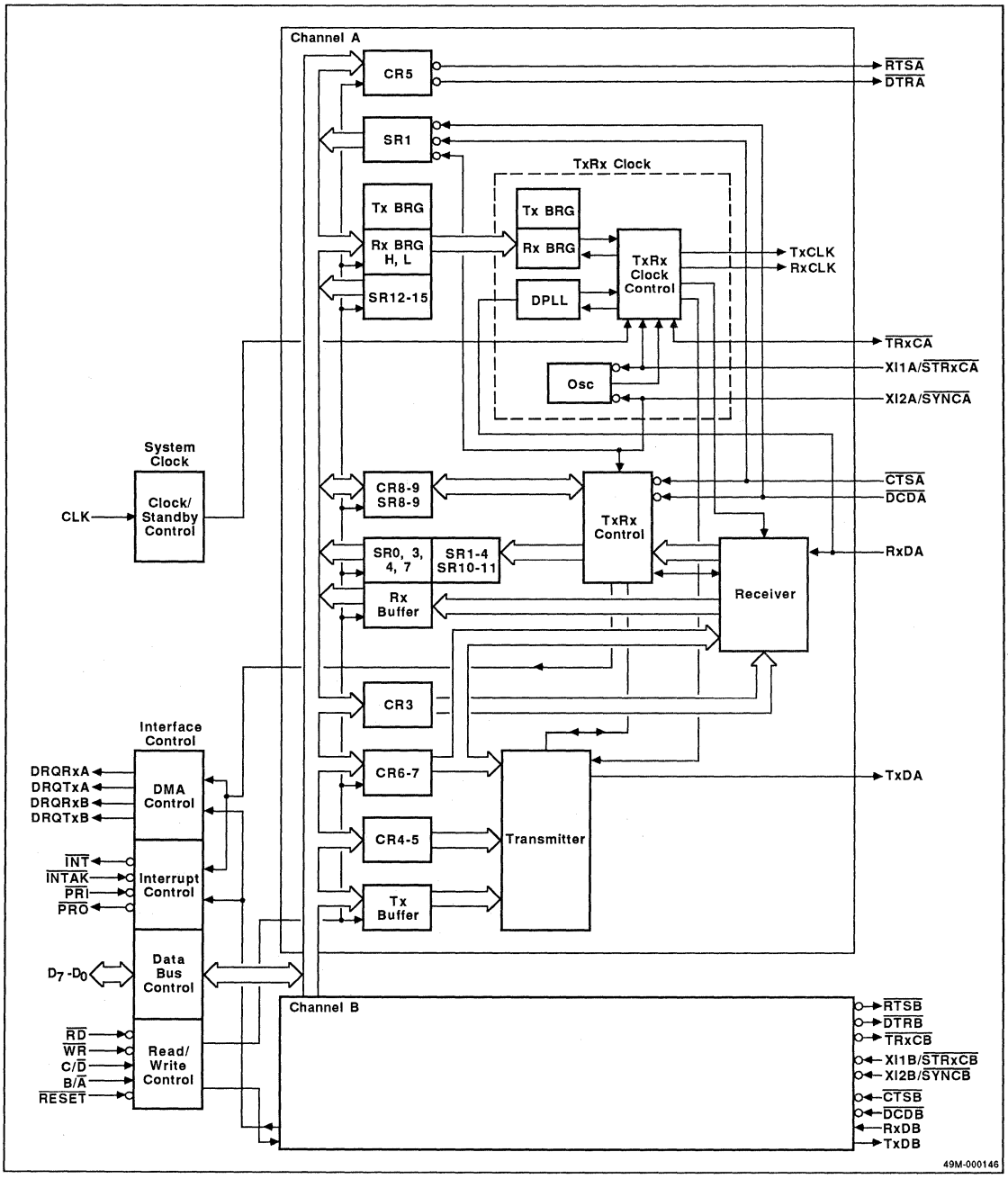
Standby Mode

The μPD72001 enters the standby mode after a hardware reset or by issuing the standby command (CR13 bit D0). In standby mode, the system and data clocks are blocked internally by the clock multiplexer. This shuts down the AMPSC and reduces power consumption greatly. System power requirements can be further reduced by externally stopping the input clock transitions.

In standby mode, the μPD72001 retains all register values, but no internal functions operate and read operations of the AMPSC will not transfer any data.

To release the standby mode, a write cycle must be performed to CR0. To resume normal operation without affecting the internal state of the device, a zero can be written to CR0.

Figure 2. μPD72001 AMPSC Block Diagram



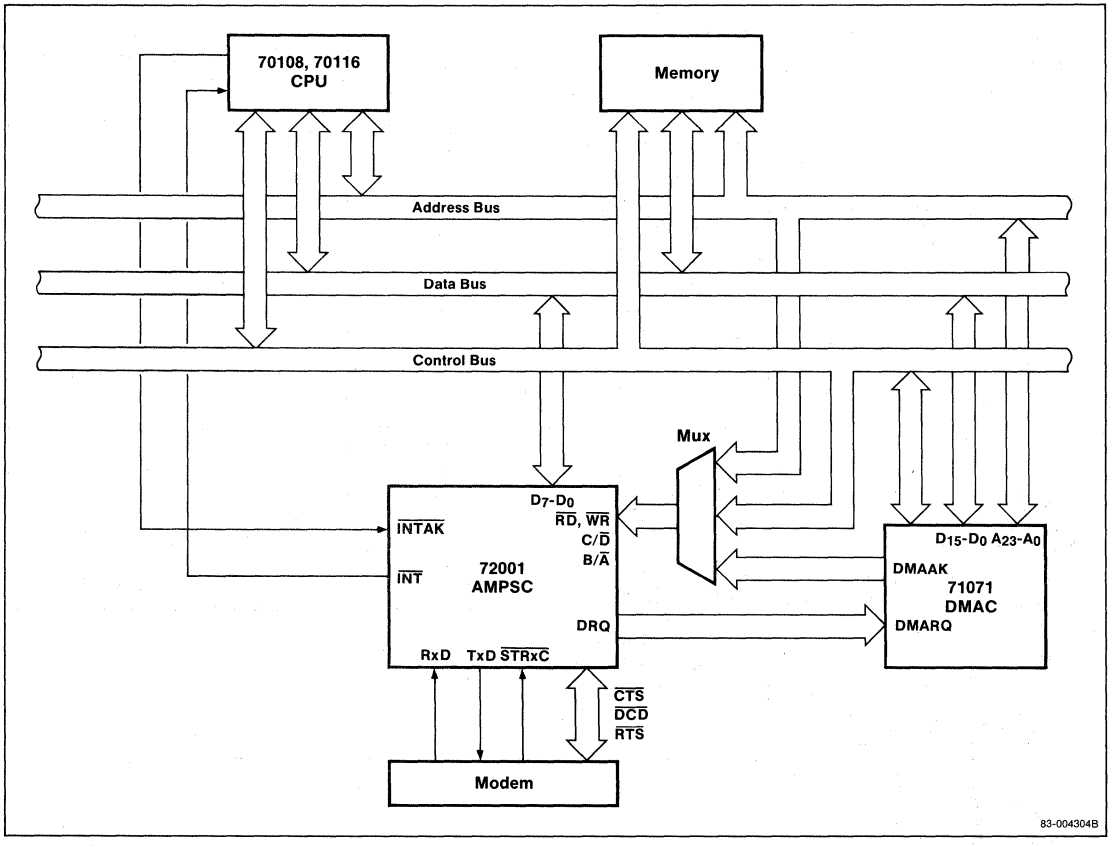
System Configuration Example

In the system configuration example (figure 3), the μPD72001 is used as a high-speed interface to a modem. It controls the modem interface and serial data flow. The AMPSC is used with a direct memory access controller (DMAC), such as the μPD71071 in order to speed the data transfer and reduce the host CPU overhead.The μPD72001 directly interfaces with the host CPU, without requiring an interrupt controller, such as the μPD71059. Extra hardware is not required, since the AMPSC can generate its own interrupt vectors.

The interface between the μPD72001 and the host CPU is not very complex. It requires only address decoding logic for I/O operations. A multiplexer can be used to decode DMA acknowledge signals. However, it is not necessary with DMA controllers, such as the μPD71071, which are able to do their own I/O addressing.

The AMPSC's flexible interface to a variety of host processors makes connection simple.

Figure 3. System Configuration Example



Programming the AMPSC

Software programming the AMPSC utilizes separate data and command/status paths. The data path uses an 8-bit register. The command/status path has a set of 8-bit registers structured for efficient and complete control with a minimum of interaction from the host processor.

The internal registers (table 1) are divided into control registers (CRs) and status registers (SRs). Also, unless otherwise noted in table 1, each channel has its own set of registers; for example, CR1A and CR1B are the CR1 control registers for channels A and B.

The control and status registers for a given channel are all accessed through the same I/O address. The different registers are selected by using the register pointer in CR0 (bits D0-D2). The register pointer is reset to zero after each register operation. For example, to write to CR2, a two is initially written to the control address (C/$\overline{D}$ pin set high). After this the value to be written into CR2 is also written to the control address. To read from SR2, a two is written to the control address, and then a read cycle at the control address reads the value in SR2. A zero is not required to be written before CR0 and SR0 are accessed.Control registers (figure 4) set up the device operation mode or control device operations. The host processor writes control words into these registers.

Status registers (figure 5) hold device status information. The host processor can sense the AMPSC device status by reading these registers.

Frequently used information is retained in control register CR0 and status register SR0. This information can be sent or received by writing or reading a single byte. In normal operation, CR0 is initially loaded with a command to reset the AMPSC. Next, CR2 is loaded to set the interface mode. This is followed by the remaining registers, beginning with CR4 to set the protocol type.

Table 1. AMPSC Internal Register Configuration

Control Registers	CR0	
	CR1	
	CR2	Functions differ for CR2A and CR2B
	CR3	
	CR4	
	CR5	
	CR6	
	CR7	
	CR8, CR9	Registers for each channel are used in pairs: CR8A/CR9A; CR8B/CR9B
	CR10	
	CR11	
	CR12	Tx/Rx BRG registers are loaded by setting bits 0 and 1 of CR12
	CR13	
	CR14	
	CR15	
Status Registers	SR0	
	SR1	
	SR2B	No register SR2A
	SR3	
	SR4A	No register SR4B
	SR5, SR6, SR7	No registers
	SR8	
	SR9	
	SR10	
	SR11	
	SR12, SR13	Registers for each channel are used in pairs: SR12A/SR13A; SR12B/SR13B
	SR14, SR15	Registers for each channel are used in pairs: SR14A/SR15A; SR14B/SR15B

2

Figure 4. Control Register Bit Functions

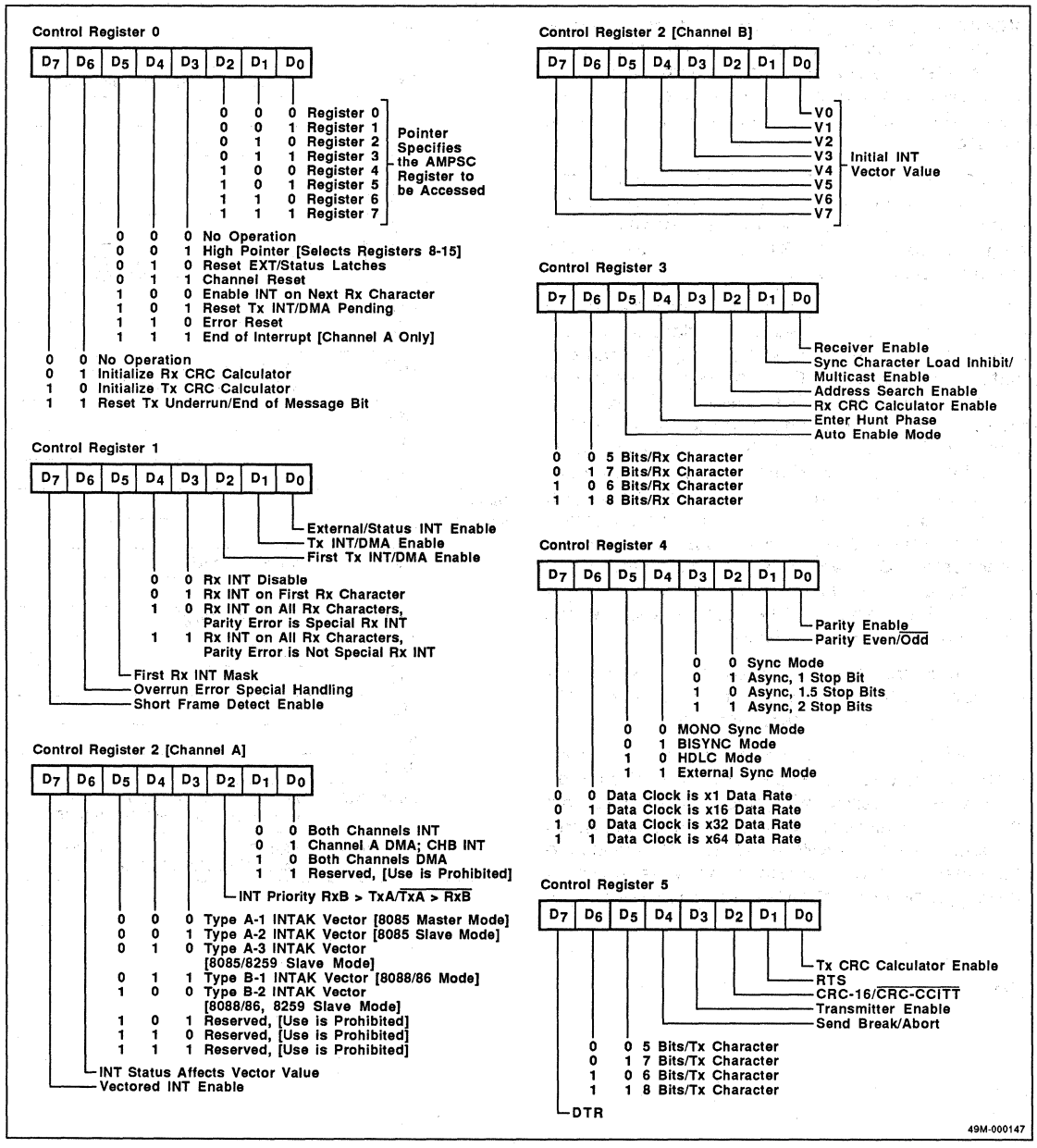


Figure 4. Control Register Bit Functions (cont)

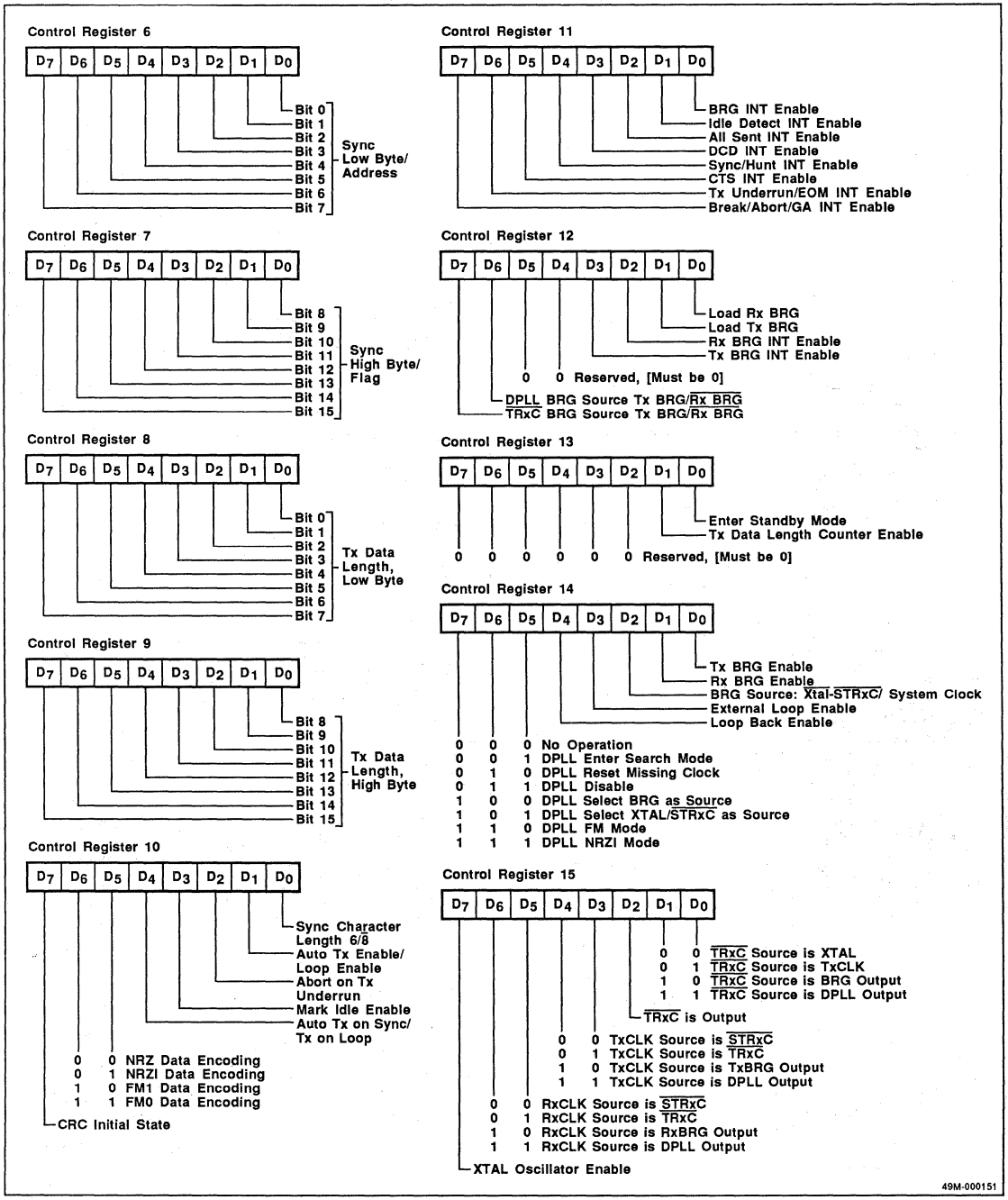


Figure 5. Status Register Bit Functions

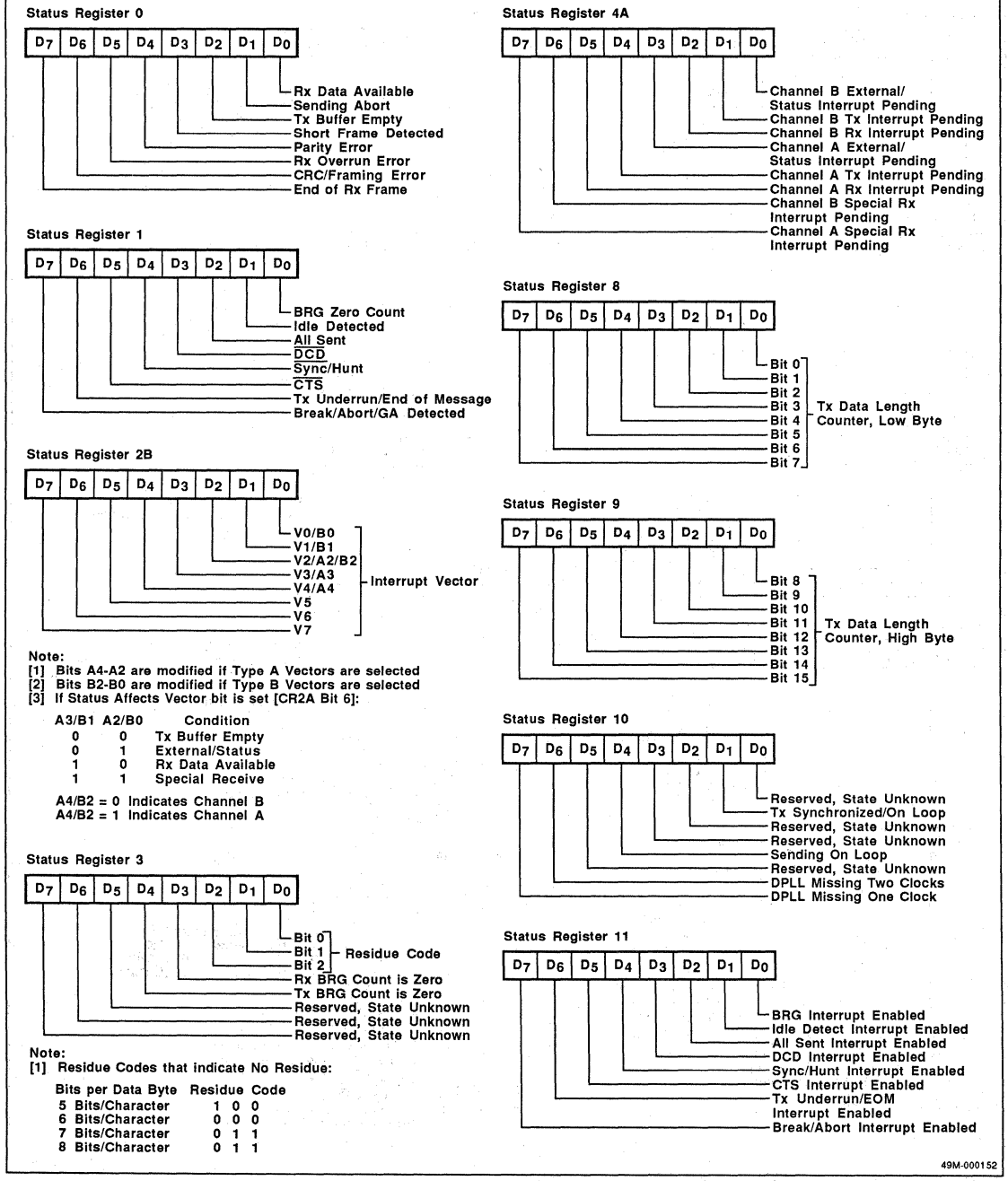
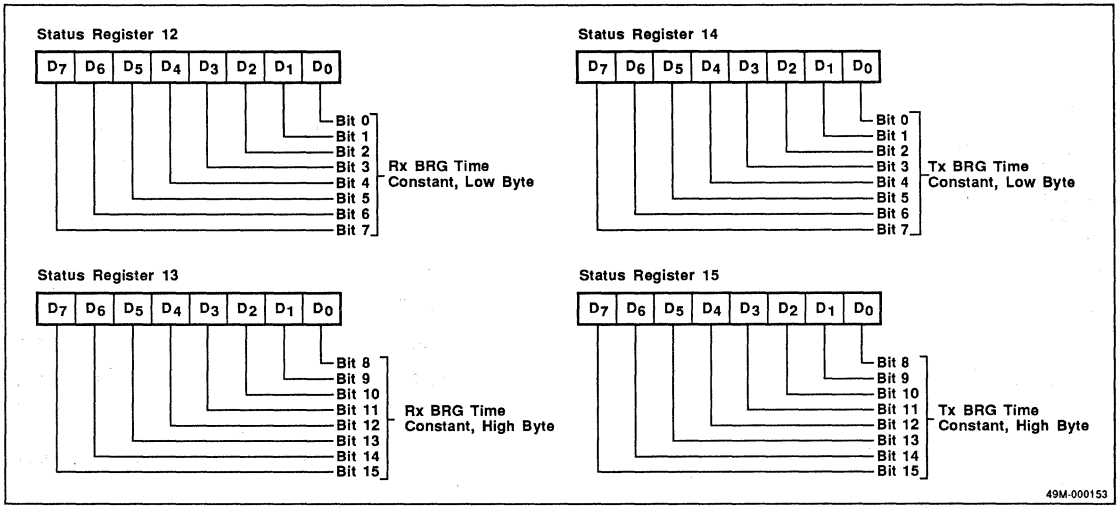


Figure 5. Status Register Bit Functions (cont)



Control Register CR0

CRC Control [D7-D6]

These bits are valid when the COP or BOP mode is selected. They are not used in the asynchronous mode.

No Operation [00]. This command has no effect.

Initialize Rx CRC Calculator [01]. This command initializes the receiver (Rx) CRC calculator. The command should be issued before data reception starts. However, before this command is issued, the initial value of the Rx CRC calculator must be set by the value of CR10 bit D7.

This command is not required in the BOP mode, since the CRC calculator is automatically initialized upon receipt of the flag value according to the value of CR10 bit D7.

Initialize Tx CRC Calculator [10]. This command initializes the transmit (TX) CRC calculator. It should be issued before data transmission is started. However, before the command is issued, the initial value of the Tx CRC calculator must be set by the value of CR10 bit D7.

In the BOP mode, if CR10 bit D7 is set to one, the Tx CRC calculator is automatically initialized to one, when a flag value is loaded into the transmit shift register within the AMPSC.

Reset Tx Underrun/EOM Bit [11]. This command resets SR1 bit D6 from one to zero (transmit underrun/end-of-message bit). If data is not loaded into the transmit buffer before the transmit shift register begins transmitting its last bit, the AMPSC enters the Tx Underrun/EOM state. At this point, the AMPSC checks to see if a CRC SYNC/Flag or abort is to be sent, which depends on the value of SR1 bit D6 and the operating mode. Therefore, SR1 bit D6 must be reset before transmission of the last byte starts. At the occurrence of Tx underrun, the CRC or the SYNC character/flag is sent when the SR1 bit D6 is a zero or one, respectively.SR1 bit D6 is set when the CRC or SYNC/Flag byte is written to the Tx register by the AMPSC.

In the BOP mode, bit D6 of SR1 is automatically set to zero when the first data byte of a frame is written into the AMPSC.

Command [D5-D3]

These bits control the state of the device.

No Operation [000]. This command has no effect.

High Pointer [001]. This command is used in conjunction with CR0 bits D2-D0 (Register Pointer) to access status registers 8 through 15. For example, to access SR11, bits D5-D0 of CR0 are set to 001011.

Reset E/S Bit Latches [010]. This Reset External/Status Bit Latch command is issued when an E/S bit (each bit of SR1) latch operation has occurred. It opens the E/S latches and prepares for the latching of a new E/S bit status change. If E/S interrupt is enabled, an E/S interrupt will occur and the latches will latch when an E/S bit's status changes. Not all state transitions will cause latching and an interrupt to occur. See the description of SR1 for details. New status will not be available in SR1 until this command is issued.

Channel Reset [011]. This command resets an AMPSC channel. It performs a function similar to the $\overline{\text{RESET}}$ pin. Executing the channel reset command halts channel operation. After a channel reset, three system clock periods (t_{CY}) should elapse before any further commands or data are sent to the channel.

Enable Next Rx Character Interrupt [100]. This command is valid only when the First Rx INT mode (CR1 bits D4-D3 = 01) is selected. It is issued at the end of a message to request an additional Rx interrupt for the first received byte of the next message. The additional Rx interrupt occurs when the next data byte is received after the command is issued.

This command has no effect when the First Rx INT mask is on (CR1 bit D5 = 1), even if the First Rx INT mode is selected.

Reset Tx Interrupt/DMA Pending [101]. This command is used to clear a pending Tx interrupt request or Tx DMA request while the Tx buffer is empty (SR0 bit D2 = 1). It is typically used to clear a Tx interrupt or Tx DMA request caused by the Tx buffer empty state that occurs after the last byte is written into the AMPSC.

Error Reset [110]. This command is used to reset the pertinent bits (SR0 bits D7-D3) if a Special Rx Condition has occurred. If it occurs when the First Rx INT mode is selected, any data that is subsequently received is not transferred to the last stage of the AMPSC internal Rx buffer, but will remain in the first and second stages until this command is issued.

End of Interrupt [111]. This command is used so that the AMPSC can recognize the end of interrupt service processing. It should be issued when interrupt service for the AMPSC is completed. Command execution resets the internal interrupt service latch and re-enables lower priority interrupt requests. This command is required when the start of interrupt service has been indicated by either conducting an $\overline{\text{INTAK}}$ cycle, or by reading SR2B.

Register Pointer [D2-D0]

These bits specify which AMPSC register number is to be accessed. The bits are reset to 000 when system reset is executed or when the AMPSC is accessed after a Register Pointer value is specified. For registers numbered 8 and above, the High Pointer command (D5-D3 = 001) is used inconjunction with the Register Pointer to access them.

Control Register CR1

Short Frame Detect [D7]

Valid only in BOP mode, this bit detects short HDLC frames (frames that are less than 32 bits long).

Short Frame Detect Disabled [0]. Short frame detection is disabled.

Short Frame Detect Enabled [1]. Short frame detection is enabled. If a short frame is received, SR0 bit D3 (Short Frame Detect) is set to 1, causing a Special Rx condition interrupt.

Overrun Error INT [D6]

This bit selects the timing of overrun error detection.

Normal Mode [0]. In this mode, an overrrun error is indicated when the received data that caused the overrun error is transferred to the last stage of the receive buffer. A Special Rx Condition interrupt occurs at this time.

Special Mode [1]. In this mode, the Rx Overrun Error bit immediately reflects an overrun error within the AMPSC. A Special Rx Condition interrupt also occurs at this time. The received data that caused the overrun error may not be the byte at the last stage of the RxFIFO.

Receive Interrupt on First Character Mask [D5]

This bit is enabled only if the First Rx INT mode (CR1 bits D4-D3 = 01) is selected. It is used to mask Rx interrupts caused by received data. Setting this bit to 1 causes all first receive interrupts to be masked. It does not mask Special Receive interrupts. It is used in data transfers when no interrupt service is desired or required, such as DMA only data transfer.

Receive Interrupt Mode [D4-D3]

These bits set the Rx INT mode. They specify the way received data is managed.

Disable Mode [00]. This Receive Interrupt Disable mode is used to accept received data using status polling, or to disable the receive interrupt request.

First Rx Character Mode [01]. In this mode, which is typically used with DMA data transfer, an Rx interrupt occurs only when the first byte is received. This occurs when Rx is enabled after initialization or after the Enable Next Received Character interrupt command is issued.

All Receive-1 Mode [10]. This mode causes a receive interrupt to be generated for each byte received. In this mode, a parity error causes a Special Rx Condition interrupt.

All Receive-2 Mode [11]. This mode is the same as All Receive-1, except that parity error does not cause a Special Rx Condition interrupt.

First Transmit Interrupt/DMA Enable [D2]

This bit determines whether a Tx INT/DMA request is generated immediately after the transmitter is enabled. It is valid when INT/DMA is enabled (CR1 bit D1 = 1).

A transmit interrupt or DMA request is issued if bit D2 is 1 when the transmitter is enabled, but not if the bit is 0. Regardless of the state of bit D2, an interrupt or DMA request is generated when the Tx buffer makes the full-to-empty transition.

Transmit Interrupt/DMA Enable [D1]

This bit enables the transmit interrupt or DMA request. Each time a transmit interrupt condition exists and provided bit D1 is set, an interrupt or DMA request is generated.

External/Status Interrupt Enable [D0]

If bit D0 is set, a change in state of the external/status bits causes an interrupt and the state of the bits is latched. The latches must be reset with the Reset External/Status Bit Latch command (CR0 bits D5-D3), before subsequent interrupts can occur.

Control Register CR2A

Vectored Interrupt Enable [D7]

This bit enables transmission of the interrupt vector. If the bit is set, the interrupt vector is placed on the data bus during the INTAK cycle. If the bit is reset, the vector is never placed on the bus; It can be read by the host processor. In this mode, the $\overline{INT}$ signal is released after the host processor reads SR2B or clears the interrupt condition.

Interrupt Status Affects Vector [D6]

This bit determines if the value of an interrupt vector is modified by the cause of interrupt. If the bit is set, the vector is modified as specified by bits D5-D3. If the bit is reset, the vector is not modified and the cause of interrupt must be determined by reading SR0 and SR1.

Interrupt Vector Mode [D5-D3]

These bits determine the interrupt vector operation. The bits also select which bits of an interrupt vector are to be changed when the Status Affects Vector is set by CR2A bit D6. For details of how the vector is modified, refer to the description of register SR2B. Table 4 shows the vector operation determined by bits D5-D3.

Interrupt Priority Select [D2]

This bit selects the priority of interrupt requests within the AMPSC. The priority does not apply to DMA transfer.

If bit D2 = 0, the priority from high-to-low is RxA, TxA, RxB, TxB, E/S A, E/S B.

If bit D2 = 1, the priority from high-to-low is RxA, RxB, TxA, TxB, E/S A, E/S B.

Interrupt/DMA Mode [D1-D0]

These bits select the data transfer mode for each channel. The E/S, Rx, and Special Rx Condition interrupts can be enabled in both modes. The Tx interrupts are disabled on any channel in DMA mode. The three modes are as follows:

Bits D1-D0	Mode
00	Both channels interrupt
01	DMA on channel A, interrupt on channel B
10	DMA on both channels

Control Register CR2B

Bits D7-D0 of CR2B set the initial value of an interrupt vector.

Table 4. Interrupt Vector Operation Throughout INTAK Sequence

CR2A						Data Bus Status (INTAK response of AMPSC)							
D5	D4	D3	Mode	PRI	INTAK Cycle	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	A1	*	1st.	1	1	0	0	1	1	0	1
				low	2nd.	V7	V6	V5	M4	M3	M2	V1	V0
				low	3rd.	0	0	0	0	0	0	0	0
				*	1st.	1	1	0	0	1	1	0	1
				high	2nd.	High Impedance							
				high	3rd.	High Impedance							
0	0	1	A2	*	1st.	High Impedance							
0	1	0	A3	low	2nd.	V7	V6	V5	M4	M3	M2	V1	V0
				low	3rd.	0	0	0	0	0	0	0	0
				*	1st.	High Impedance							
				high	2nd.	High Impedance							
				high	3rd.	High Impedance							
0	1	1	B1	*	1st.	High Impedance							
1	0	0	B2	low	2nd.	V7	V6	V5	V4	V3	M2	M1	M0
				*	1st.	High Impedance							
				high	2nd.	High Impedance							

Notes:

(1) * = Don't care.

(2) When Status Affects Vector (bit 6 of CR2A) is set, the M data bits are modified to indicate the interrupt source.

(3) Modes A3 and B2 ignore the state of PRI. They are slave modes for use with an interrupt controller such as the μPD71059.

Control Register CR3

Receive Character Bit Length [D7-D6]

These bits determine the number of bits per character in the received data.

Bits D7-D6	Bits/Character
00	5
01	7
10	6
11	8

Auto Enable Mode [D5]

Bit D5 enables and disables the auto enable mode. In this mode, the $\overline{CTS}$ and $\overline{DCD}$ pins control operation of the transmitter and receiver, respectively. If the input pin is high, the Tx or Rx is disabled. The $\overline{RTS}$ pin outputs the current transmitter status. The pin remains low during transmission and returns high only after all characters have been sent. The auto enable mode is enabled by setting bit D5 to one and disabled by resetting bit D5 to zero. With bit D5 = 0, $\overline{CTS}$, $\overline{DCD}$, and $\overline{RTS}$ function as normal inputs and outputs.

Enter Hunt Phase [D4]

Valid in COP or BOP mode, this bit forces the AMPSC to enter the Hunt Phase. In the Hunt Phase, the μPD72001 searches the received data stream for either a sync or flag before it begins loading data into the Rx FIFO.

Receive CRC Calculator Enable [D3]

Valid only in COP or BOP mode, bit D3 determines whether or not a CRC calculation is to be performed on the received data. The CRC is calculated 8 bit times after a byte is transferred into the receive FIFO. If bit D3 is reset before this time, the byte will not be included in the CRC calculation. The bit must be set again after the next byte is received to resume the CRC calculation.

Address Search Mode Enable [D2]

Valid only in BOP mode, bit D2 determines whether or not the address field value of a received frame is to be compared with the value set in CR6. If the bit is set to one, Address Search is enabled and the AMPSC checks the first byte of the frame. If the byte matches CR6 or the global address (FFH), the frame is received. If the byte does not match, the AMPSC enters the Hunt mode again, and the byte and the rest of the frame are blocked and not received. If Multicast mode is enabled (bit D1), only the four most significant bits (D7-D4) of the address byte are compared.

Sync Character Load Inhibit/Multicast Enable [D1]

Valid only in COP or BOP mode, bit D1 has a different meaning in each mode. In COP mode, setting bit D1 to one enables the Sync Character Load Inhibit function. This prevents any byte that matches the value in CR6 from being loaded into the receive FIFO and being included in the CRC calculation.

In BOP mode, bit D1 enables the Multicast function. In this mode, which is a modified form of the address search mode, only the most significant four bits of the received address are compared with the identical bits of CR6. Frame acceptance will function in the same way as in the address search mode.

Receiver Enable [D0]

This bit enables and disables the receiver. Setting bit D0 enables the receiver, resetting it disables the receiver.

Control Register CR4

Clock Rate [D7-D6]

Bits D7 and D6 select the clock rate divisor. They are ignored in the internal synchronous modes. In the external synchronous mode, only the x1 and x16 selections are valid.

In asynchronous mode, the following values apply:

Bits D7-D6	Divisor
00	x1
01	x16
10	x32
11	x64

The divisor value is the factor by which the supplied data clock is greater than the data rate for the transmitter and receiver. The data clock source is selected by the clock multiplexer. It can be set to any of the BRG, DPLL, or external clock sources. The divisor determines the number of times that the received data is sampled per bit time by the receiver. Also, it determines the composition of the transmitter output.

Protocol Mode [D5-D4]

Bits D5-D4 select the synchronous protocol, which are used when synchronous mode is selected with bits D3-D2.

Bits D5-D4	Mode
00	Mono-Sync, character synchronous
01	Bisync, character synchronous
11	External Sync, character synchronous
10	HDLC, bit synchronous

Tx Stop Bits/Sync Mode [D3-D2]

Bits D3-D2 select the number of stop bits sent after each byte in Asynchronous mode, or they select the Synchronous mode.

Bits D3-D2	Mode
00	Sync mode
01	Async mode, 1 stop bit
10	Async mode, 1.5 stop bits
11	Async mode, 2 stop bits

Parity Select [D1]

Valid in Asynchronous and COP modes, bit D1 selects the parity type: 0 = odd and 1 = even. It is used only when the Parity Enable bit D0 of CR4 is set to one.

Parity Enable [D0]

Bit D0 enables the parity bit calculation on transmitted data and parity checking on received data. Setting bit D0 enables parity; resetting bit D0 disables parity. If the length of the received character is 7 bits or less, the parity bit can be read in the received data byte. If parity is disabled, no parity bit is transmitted and none is expected on receipt.

Control Register CR5

$\overline{\text{DTR}}$ Control [D7]

This bit controls the $\overline{\text{DTR}}$ pin status: 0 = high and 1 = low. The $\overline{\text{DTR}}$ pin function is disabled if channel B is operating in the DMA mode (CR2A bits D1-D0 = 10)

Transmit Character Bit Length [D6-D5]

These bits specify the bit count per character in transmitted data.

Bits D6-D5	Bits/Character
00	5 or fewer
01	7
10	6
11	8

If the bit count per character is 6 or 7, only the low-order bits of the byte are valid and the most significant bit(s) are ignored. If the count is 5 bits or lower when writing into the transmit data register, refer to the data format that is shown in table 5.

Table 5. Parallel Data Format for One to Five Bits per Character

Bits	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	0	0	D0
2	1	1	1	0	0	0	D1	D0
3	1	1	0	0	0	D2	D1	D0
4	1	0	0	0	D3	D2	D1	D0
5	0	0	0	D4	D3	D2	D1	D0

Dn = Effective data bit

Send Break/Abort [D4]

Bit D4 controls the break or abort transmission according to the selected operation mode. In asynchronous mode, bit D4 controls sending the break signal (TxD set to spacing (0) condition). Setting bit D4 to one begins sending the break signal; resetting it to zero returns the transmitter to normal operation.

In COP mode with Tx on Loop selected (bits 4 and 1 in CR10), setting bit D4 causes the transmitter to be synchronized with the receiver. The bit is reset automatically when synchronization is achieved.

In BOP mode, setting bit D4 to one causes eight 1-bits (abort sequence) to be sent. After completion of the message, bit D4 is reset automatically and the transmitter returns to the idle state.

Transmit Enable [D3]

Disable. Setting bit D3 to the zero state disables the transmitter function. If the transmitter is currently sending a character, the AMPSC waits until the character is completed before setting TxD to the marking (1) state. If bit D3 is reset during transmission of a CRC character, a SYNC character or flag is sent in place of the CRC character.

If D3 is reset in the COP or BOP mode, the Tx Underrun/EOM bit (SR1 bit D6) is set.

If the AMPSC is in the SDLC Loop mode (refer to CR10) or Echo Loop Test (refer to CR14), the TxD pin is connected to RxD, and is not set to marking.

Enable. Setting bit D3 to the one state enables the transmitter to start transmission. If the Auto Enable mode is selected (CR3 bit D5 = 1), the signal applied to the CTS pin controls the transmitter operation.

CRC Polynomial [D2]

This bit selects the polynomial used for CRC calculation. It is valid only in COP or BOP mode. Only the CCITT polynomial is used in BOP mode. Bit 7 of CR10 sets the initial value of the CRC calculator.

D2 = 0 (CRC-CCITT): The generating polynomial expression is $X^{16} + X^{12} + X^5 + 1$.

D2 = 1 (CRC-16): The generating polynomial expression is $X^{16} + X^{12} + X^2 + 1$.

$\overline{RTS}$ Control [D1]

Bit D1 controls the $\overline{RTS}$ pin. Setting bit D1 to the zero state causes $\overline{RTS}$ to be high, setting it to the one state causes it to go low. If Auto Enable mode is selected in Asynchronous mode, $\overline{RTS}$ operates differently. If the bit remains at zero from the start of transmission through to the end, $\overline{RTS}$ will stay high. If it is set to one, it remains low. If it starts set to one and is then set to zero while transmitting, $\overline{RTS}$ will not go high until all data is transferred out of the Tx shift register.

Transmit CRC Calculator Enable [D0]

Valid only in the COP or BOP mode, bit D0 determines whether or not transmitted data is included in the CRC calculation. If bit D0 is set when the byte is transferred into the Tx shift register, the byte is included in the Tx CRC calculation. Bit D0 should be set or reset before loading a data byte into the AMPSC.

Control Register CR6

Valid only in the COP or BOP mode, this byte (bits D7-D0) specifies the SYNC character pattern or address value.

In Monosync or External Sync mode, D7-D0 holds the transmit Sync character. In Bisync mode, the low-order byte of the Sync pattern is set in D7-D0.

If the sync character is 6 bits (CR10 bit D0 = 1), bits D3-D0 should be set to one.

In mono or external sync bits D1 and D0 are repeated in positions D7 and D6.

In BOP mode, this byte is the secondary address.

Control Register CR7

Valid only in the COP or BOP mode, these bits specify the Sync character or flag.

In Monosync mode, D7-D0 holds the receive Sync character. In BISYNC mode, the high-order byte of the Sync character is set in D7-D0. These bits are not used in External Sync mode.

In BOP mode, the flag pattern (01111110) is set in bits D7-D0.

Control Register CR8

Valid only in the BOP mode, CR8 bits D7-D0 hold the low byte (bits 7-0) of the transmit data length. Register pair CR8 and CR9 must be set before the Tx Data Length Counter Enable bit (D1 of CR13) and Tx Enable bit (D3 of CR5) are set. The transmit data length register (TxDLR) is used to automate the sending of HDLC frames. See the description of CR13 for detail information.

Control Register CR9

Valid only in the BOP mode, CR9 bits D7-D0 hold the high byte (bits 15-8) of the transmit data length. Register CR9 is paired with CR8.

Control Register CR10

Initial CRC State [D7]

Valid only in the COP or BOP mode, bit D7 specifies the initial state of the CRC calculation circuit. Setting this bit to zero causes the CRC to be initialized to zero when the Initialize CRC command (CR0 bits 7-6) is performed. Setting this bit to one causes the CRC to be set to all ones.

Data Format [D6-D5]

These bits specify the serial data format and enable the corresponding encoder/decoder.

Bits D6-D5	Format
00	NRZ
01	NRZI
10	FM1
11	FM0

With NRZ format, it is possible to decode Manchester encoded data by setting the DPLL mode to FM (CR14 bits D7-D5 = 110).

Auto Tx on Sync/Tx on Loop [D4]

Bit D4 is valid only in the COP or BOP mode. In COP mode, it synchronizes the receiver with the transmitter. In BOP mode, it controls SDLC loop operation. The bit is valid only when the Loop Enable state (CR10 bit D1 = 1) is selected.

In COP mode, bit D4 provides the Auto Tx on Sync function to synchronize receiver and transmitter operation.

(1) D4 = 0. The Auto Tx on Sync function (CR10 bit D1 = 1) is disabled. Once synchronization is established after this bit is set to 1, resetting the bit to 0 does not affect synchronization.

(2) D4 = 1. If bit D1 (Loop Enable) is also set to one, the transmitter is disabled and the receiver enters the Hunt Phase. When the SYNC character is detected, character synchronization is established, the transmitter is enabled, and data transmission can begin. The state of character synchronization can be determined from the state of the Tx Sync/GA Detect bit (SR10 bit D1).

In BOP mode, bit D4 set to one enables or bit D4 set to zero disables the Tx on Loop function. It is used for data transmission during the SDLC loop operation.

(1) D4 = 0. Once the AMPSC forms a loop and starts transmission, bit D4 must be reset to zero. This allows the CRC and flag to be automatically transmitted if a Tx Underrun/EOM occurs and allows the AMPSC to be subsequently placed in Loop mode with a 1-bit delay. Bit D4 must be reset before the CRC transmission is completed.

(2) D4 = 1. When the Loop Enable bit (CR10 bit D1) is set to one, SDLC Loop Operation mode is selected, in which the RxD input is connected to the TxD output within the AMPSC to form a loop. The GA (Go Ahead) pattern detection is initiated. If the GA pattern (11111110 = FEH) is detected, a 1-bit delay is inserted between RxD and TxD and the GA pattern detection is continued. At this point, the transmitter remains disabled. The receiver can be enabled at this point. Subsequently, if the GA pattern is detected, the transmitter is enabled. At this point, the GA pattern is automatically transformed into a flag so that any data in the Tx buffer may be transmitted following the flag. Once transmission is started, bit D4 must be reset before the end of the frame.

Idle Condition [D3]

Valid only in BOP mode, bit D3 determines the type of information to be transmitted following a closing flag or completion of the Send Abort. If bit D3 is zero, flags will be sent; if it is a one, continuous marks (ones) will be sent.

Transmit Condition on Underrun [D2]

Valid only in the BOP mode, bit D2 determines transmitter action when a Tx Underrun condition occurs. If bit D2 is reset, Tx Underrun/EOM generates either the CRC followed by a flag or just a flag depending on the state of the Tx Underrun bit (SR1 bit D6) and the CRC enable bit (CR5 bit D0). If the CRC is disabled or the Tx underrun bit is a one, only flags are sent. Otherwise, the CRC is sent followed by flags. If bit D2 is set, the abort message is sent followed by flags.

Auto Tx/Loop Enable [D1]

Valid only in the COP or BOP mode, bit D1 enables the two types of loop operations that are set with bit D4. This bit should be set before the transmitter or receiver is enabled.

SYNC Character Length [D0]

Valid only in the COP mode, bit D0 determines the number of bits per SYNC character. Setting bit D0 to zero gives a character length of 8 bits in Mono-sync and 16 bits in Bisync. With bit D0 = 1, the character lengths are 6 and 12 bits, respectively.

Control Register CR11

Each bit of CR11 controls an E/S interrupt request generated by the AMPSC. An interrupt is set if the E/S interrupts are enabled (CR1 bit D0 = 1). For the causes of interrupts assigned to each, refer to the description of SR1. Setting each bit to one enables it as a source of interrupts.

Break/Abort/Go Ahead Interrupt Enable [D7]

In Asynchronous and COP modes, bit D7 enables interrupts at the beginning and end of each detected break condition (a null character plus a framing error).

In BOP mode, when not in SDLC loop, bit D7 enables interrupts at the beginning and end of each received abort condition (seven or more consecutive 1-bits). In SDLC loop mode, bit D7 also enables interrupts for detecting the GA pattern (11111110 = FEH).

Transmitter Underrun/End of Message Interrupt Enable [D6]

Valid only in the COP or BOP mode, bit D6 enables interrupts caused by transmitter underrun and Tx End of Message detection.

$\overline{\text{Clear to Send}}$ Interrupt Enable [D5]

Bit D5 enables interrupts caused by a change of state on the $\overline{\text{CTS}}$ pin.

$\overline{\text{SYNC}}$/Hunt Interrupt Enable [D4]

Bit D4 enables interrupts caused by a change in the $\overline{\text{SYNC}}$/Hunt state.

$\overline{\text{Data Carrier Detect}}$ Interrupt Enable [D3]

Bit D3 enables interrupts caused by a change of state on the $\overline{\text{DCD}}$ pin.

All Sent Interrupt Enable [D2]

Valid only in the Asynchronous or BOP mode, bit D2 enables interrupts generated by the All-Sent condition.

Idle Detect Interrupt Enable [D1]

Valid only in the BOP mode, bit D1 enables interrupts caused by a change in the Idle Detection condition.

BRG Interrupt Enable [D0]

Bit D0 enables interrupts caused by one of the baud rate generator/timers (BRG) counting down from one to zero. Also, each of the BRGs must be enabled in CR12 bits D3-D2.

Control Register CR12

BRG Select for TRxC [D7]

When BRG is selected as the source of the clock at the TRxC pin (CR15 bits D1-D0 = 10), and the TRxC pin is set to output (CR15 bit D2 = 1), bit D7 selects TxBRG (one state) or RxBRG (zero state).

BRG Select for DPLL [D6]

Bit D6 selects the source (TxBRG or RxBRG) for the DPLL. It is valid when the BRG is selected as the source for the DPLL circuit (CR14 bits D7-D5 = 100). Setting bit D6 to one selects TxBRG and setting it to zero selects RxBRG.

Transmit BRG Interrupt Enable [D3]

Bit D3 enables an E/S interrupt when the TxBRG counts down from 1 to 0. It is valid only when the BRG IE bit is set (CR11 bit D0 = 1).

Receive BRG Interrupt Enable [D2]

Bit D2 enables an E/S interrupt when the RxBRG counts down from 1 to 0. It is valid only when the BRG IE bit is set (CR11 bit D0 = 1).

Transmit BRG Register Set [D1]

Bit D1 is used to write the time constant value into the TxBRG register. When D1 is set to one, the next two bytes written to the AMPSC are assumed to be the time constant value. The lower byte is written in the first write cycle and the upper byte in the second write cycle. Bit D1 is automatically reset after the register is loaded.

The time constant value is calculated by using the following formula.

$$\text{Time constant} = \frac{\text{Source clock frequency (Hz)}}{2 \times \text{(Data clock rate (BPS))}} - 2$$

The data clock rate is the transmitted or received data rate multiplied by the clock factor specified in CR4 bits D7-D6.For example, if the system clock is selected as the BRG source (CR14 bit D2 = 1) at 8 MHz and the BRG is the transmitter source (CR15 bits D4-D3 = 10) with a clock factor of x16 (CR4 bits D7-D6 = 01) and data rate of 9600 bits per second, the calculation would be as follows.

$$\frac{8 \times 10^6}{2 \times (9600 \times 16)} - 2 = 24.04 = 0018 \text{ (hex)}$$

The loading sequence in hexadecimal for the TxBRG would be; 0C, 02, 18, and 00.

If data is being written while the BRG is running, the value will not be loaded into the BRG until it counts down to zero.

Receive BRG Register Set [D0]

Bit D0 is used to write the count value into the RxBRG register. It operates in the same manner as bit D1 for the TxBRG register.

Control Register CR13

Transmit Data Length Counter Enable [D1]

Bit D1 enables the transmit data length counter (TxDLC) that is used to determine the end of a transmitted frame and is only valid in BOP mode. When bit D1 is set to one, the TxDLC (SR8-SR9) is incremented each time a Tx interrupt or DMA request is generated, and the value is compared with the value in the transmit length register (TxLR) (CR8-CR9). If the two values are equal, Tx interrupts/DMA requests are masked.

The subsequent Tx buffer empty interrupt is masked and no interrupt or DMA request is made. This results in a transmitter underrun. The AMPSC then sends the CRC and a closing flag. After this the AMPSC issues an external status interrupt with the All Sent bit set.If the transmitter underruns and the transmit length values do not match, then the MPSC sends an abort and sets the Sending Abort bit (SR0 bit D1). An E/S interrupt for the All Sent is generated. The TxLC value (SR8-SR9) can also be compared with the frame length to determine if correct transmission occurred. After the abort is sent, the TxDLC enable bit must be set to one again in order to generate new Tx interrupts/DMA requests.

Standby Mode Set [D0]

Setting bit D0 to one places the AMPSC in the Standby mode. This mode consumes very little power but saves all internal register values. Greater power reduction is possible by not toggling any of the AMPSC inputs. In this mode, the system clock (CLK) and the data clocks are not circulated within the AMPSC.

The AMPSC enters the Standby mode automatically after RESET. Writing 00H to CR0 restores normal operation. Table 6 lists the status of the pins in standby mode.

During Standby mode, the $\overline{WR}$ and $\overline{RD}$ pins must be held high and the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins can not be toggled. Read cycles that are conducted will not result in data being driven onto the bus.

Table 6. Pin Status in Standby Mode

Pin Symbol	Input/Output	Pin Status
$\overline{WR}$	Input	Unchanged
$\overline{RD}$	Input	Unchanged
B/$\overline{A}$	Input	Unchanged
C/$\overline{D}$	Input	Unchanged
D_7-D_0	Input/Output	High impedance
$\overline{INT}$	Output	Retains the current state
$\overline{INTAK}$	Input	Unchanged
$\overline{PRI}$	Input	Unchanged
$\overline{PRO}$	Output	Depends on PRI
DRQTxA	Output	Retains the current state
DRQRxA	Output	Retains the current state
$\overline{DTRA}$/DRQTxB	Output	Retains the current state
$\overline{DTRB}$/DRQRxB	Output	Retains the current state
TxDA, TxDB	Output	Retains the current state
RxDA, RxDB	Input	Unchanged
$\overline{TRxCA}$, $\overline{TRxCB}$	Input/Output	High impedance
$\overline{STRxCA}$, XI1A	Input	Unchanged
$\overline{STRxCB}$, XI1B	Input	Unchanged
XI2A/$\overline{SYNCA}$	Input/Output	High impedance
XI2B/$\overline{SYNCB}$	Input/Output	High impedance
$\overline{RTSA}$, $\overline{RTSB}$	Output	Retains the current state
$\overline{CTSA}$, $\overline{CTSB}$	Input	Unchanged
$\overline{DCDA}$, $\overline{DCDB}$	Input	Unchanged

Control Register CR14

DPLL Command [D7-D5]

These bits control the digital phase-locked loop (DPLL). After reset, the DPLL is disabled, the $\overline{STRxC}$ pin is selected as the source clock, and the NRZ1 mode is selected. The DPLL commands corresponding to the eight states of bits D7-D5 are described below.

No Operation [000]. This command causes no operation.

Enter Search [001]. This command causes the DPLL to start the detection of edges in received data. Circuit operation depends on the data format.

Reset Missing Clock [010]. Valid when FM mode is selected, this command resets the Missing Clock bits (SR10 bits D7-D6).

Disable [011]. This command stops DPLL operation and resets the Missing Clock bits.

Source BRG Select [100]. This command selects one BRG as the clock source for the DPLL. Selection of TxBRG or RxBRG is determined by CR12 bit D6 (BRG Select for DPLL).

Source Xtal/$\overline{\text{STRxC}}$ Select [101]. This command is used when the crystal-controlled oscillator or a clock applied to the $\overline{\text{STRxC}}$ pin is to be the source clock for the DPLL. Selection between the crystal OSC and the $\overline{\text{STRxC}}$ input is specified by CR15 bit D7 (Xtal Select).

FM Mode [110]. This command is used when received data is to be treated as FM format. Setting the data format to NRZ (CR10 bits D6-D5 = 00) allows the μPD72001 to decode Manchester encoded data.

NRZI Mode [111]. This command is used when received serial data is to be treated as NRZI format.

Local Self Test [D4]

When bit D4 is set to one, the transmitter output is directly connected to the input of the receiver within the AMPSC. Signals applied to the RxD pin will be ignored. In this mode, Autoenable cannot be used to control the transmitter or receiver.

Echo Loop Test [D3]

When bit D3 is set to one, the RxD input pin is connected to the TxD output pin in the AMPSC, so that the received data is echoed back to the remote sender for line testing. The AMPSC transmitter is disabled.

BRG Source Select [D2]

Bit D2 selects the source clock for the BRGs. The selected source clock is shared by the TxBRG and the RxBRG. If D2 is set to one, the system clock is used as the source clock. If D2 is set to zero, the source clock can either be the crystal oscillator (CR15 bit D7 = 1) or the $\overline{\text{STRxC}}$ input (CR15 bit D7 = 0).

Receive BRG Enable [D1]

Setting bit D1 to one starts the RxBRG, which takes two clocks to begin operating.

Transmit BRG Enable [D0]

Setting bit D0 to one starts the TxBRG, which takes two clocks to begin operating.

Control Register CR15

Crystal Select [D7]

If bit D7 is set to one, the on-chip crystal oscillator is enabled and a crystal can be connected across pins XI1 and XI2. If bit D7 is zero, the oscillator is disabled and the pins become $\overline{\text{SYNC}}$ and $\overline{\text{STRxC}}$.

Receive Clock Select [D6-D5]

These bits select the source for the receive data clock.

Bits D6-D5	Receive Clock Source
00	Clock applied to $\overline{\text{STRxC}}$ pin
01	Clock applied to $\overline{\text{TRxC}}$ pin (CR15 bits D2-D0 are invalid)
10	RxBRG output
11	DPLL output

Transmit Clock Select [D4-D3]

These bits select the source for the transmit data clock.

Bits D4-D3	Transmit Clock Source
00	Clock applied to $\overline{\text{STRxC}}$ pin
01	Clock applied to $\overline{\text{TRxC}}$ pin (CR15 bits D2-D0 are invalid.)
10	TxBRG output
11	DPLL output

$\overline{\text{TRxC}}$ Input/Output [D2]

Bit D2 determines whether the $\overline{\text{TRxC}}$ pin will be an input or an output. It is an input if bit D2 = 0 or if the pin is specified as an input by bits D6-D5 or D4-D3.

$\overline{\text{TRxC}}$ Source Select [D1-D0]

When the $\overline{\text{TRxC}}$ pin is selected as an output, these bits determine the output source. Refer to the preceding descriptions for D6-D5, D4-D3, and D2 to determine when the $\overline{\text{TRxC}}$ pin is an output.

Bits D1-D0	Output at Pin $\overline{\text{TRxC}}$
00	On-chip crystal oscillator (if enabled)
01	Transmit data clock
10	TxBRG or RxBRG as selected by CR12 bit D7
11	DPLL output

Status Register SR0

End of Frame [D7]

Valid only in the BOP mode, bit D7 indicates if reception of a single frame is complete. When this bit is one, a complete frame has been received and the CRC Error bit (SR0 bit D6) and Residue Code (SR3 bits D2-D0) are valid. The EOF condition causes a Special Rx Condition interrupt. The Error Reset command resets this bit.

CRC/Framing Error [D6]

In the asynchronous mode, bit D6 indicates a framing error. It is set to one if a zero is detected at the stop bit position. It generates a Special Rx Condition interrupt. Bit D6 is reset by an Error Reset command or reception of a normal data byte.

In the COP or BOP mode, bit D6 set to one indicates a CRC error. Bit D6 set to zero indicates no CRC error.

In the COP mode, bit D6 is valid 20 bit times subsequent to the last bit of the second CRC byte that is input at the RxD pin, or 16 bit times after the second CRC byte is transferred to the Rx buffer.

In the BOP mode, bit D6 is valid when the End-of-Frame bit (SR0 bit D7) is set to one.

A CRC error does not generate a Special Rx Condition interrupt.

Receive Overrun Error [D5]

A one in bit D5 indicates an Rx Overrun error. This error occurs each time the AMPSC attempts to transfer an additional byte from the Rx shift register to the Rx FIFO and the FIFO is already full.

An Rx Overrun error causes a Special Rx Condition interrupt. The timing of the Rx Overrun Error and the resulting Special Rx Condition interrupt will differ depending on the setting of the Overrun Error INT bit (CR1 bit D6). For more details, refer to the description of control register CR1.

The Rx Overrun Error bit is reset by the Error Reset command.

Parity Error [D4]

Valid only in the Asynchronous or COP mode when parity is enabled (CR4 bit D0 = 1). A one in bit D4 indicates that a parity error occurred in a received byte. The Parity Error bit is reset by the Error Reset command.

In the All Receive INT-1 mode (CR1 bits D4-D3 = 10), a parity error causes a Special Rx Condition interrupt.

Short Frame Detect [D3]

Valid only in the BOP mode when Short Frame Detect Enable is selected (CR1 bit D7 = 1), bit D3 is set when a short frame is received and is reset by the Error Reset command. A short frame has less than 32 bits between two flags.

Detection of a short frame causes a Special Rx Condition interrupt.

Transmit Buffer Empty [D2]

A one in bit D2 indicates that the Tx buffer is empty and can be loaded with the next Tx byte. Bit D2 is zero when the Tx buffer contains a byte that has not been transferred to the Tx shift register. Bit D2 is also zero in the COP or BOP mode during CRC transmission.

Sending Abort [D1]

Valid only in the BOP mode, a one in bit D1 indicates that the AMPSC is sending an abort sequence.

Bit D1 is reset by the Error Reset command. Status changes in bit D1 do not cause an interrupt.

Receive Data Available [D0]

A one in bit D0 indicates the presence of valid received data in the Rx buffer of the AMPSC.

Status Register SR1

This register consists of external status bits that indicate the causes of E/S interrupts. If the E/S INT is enabled (CR1 bit D0 = 1) and an interrupt by an specific E/S bit is enabled, the changes in the pertinent E/S bit states are latched and cause an E/S interrupt. If the E/S interrupt is disabled, changes in the E/S bit status will not be latched.

Break/Abort/Go Ahead Detect [D7]

Bit D7 is valid only in the Asynchronous or BOP mode. In the Asynchronous mode, a one in bit D7 indicates that a Break (character in which the start, stop, and data bits are all zeros) has occurred. Data received during the Break (all zeros) are not loaded into the Rx FIFO.

In the BOP mode, bit D7 indicates the reception of an abort (seven or more consecutive ones). In SDLC Loop mode, bit D7 indicates reception of the Go Ahead message (11111110 = FEH).

Transmit Underrun/End of Message [D6]

Valid only in the COP or BOP mode, a one in bit D6 indicates that all transmit data has been transferred to the Tx shift register. CRC transmission, when the transmitter underruns, can be controlled by manipulating this bit.

If CRC transmission is desired when the transmitter underruns, bit D6 must be reset to zero by the Reset Tx Underrun/EOM command bit (CR0 bits D7-D6 = 11). Before this command is issued, the transmitter must be enabled and at least one byte must have been transferred to the Tx buffer.

In the BOP mode, bit D6 is automatically reset to zero when the first byte is transferred after transmission is enabled. A status change from one to zero in this bit does not cause an E/S interrupt.

Clear To Send [D5]

Bit D5 indicates the inverted state of the $\overline{CTS}$ pin. Any change causes an interrupt.

Sync/Hunt [D4]

In the Asynchronous or external sync COP mode, bit D4 indicates the inverted state of the SYNC pin.

In the internal sync COP or BOP mode, bit D4 indicates the AMPSC synchronization state. A zero in bit D4 indicates that synchronization is established. A one indicates that the AMPSC is in the Hunt Phase or that the receiver is disabled.

Any change in state generates an interrupt.

Data Carrier Detect [D3]

Bit D3 indicates the inverted state of the $\overline{DCD}$ pin. Any change generates an interrupt.

All Sent [D2]

Valid only in the Asynchronous or BOP mode. Bit D2 set to one indicates that all the transmit data within the AMPSC has left the Tx shift register. The one to zero state transition of this bit does not generate an interrupt.

Idle Detect [D1]

Bit D1 set to one indicates detection of the Idle state (15 or more consecutive 1's) in BOP mode. The one to zero state transition of this bit does not generate an interrupt.

BRG Zero Count [D0]

Bit D0 set to one indicates that one of the BRG's has counted down to zero. Bits D4-D3 of SR3 determine which BRG counted out. The one to zero state transition of this bit does not generate an interrupt.

Status Register SR2B

This register indicates the value of the interrupt vector. It can only be read from the B channel. The value depends on the state of CR2A bit D6 (Status Affects Vector bit). If bit D6 is zero, SR2B will always equal CR2B. If bit D6 is one, the value of SR2B is modified by the cause of the highest priority interrupt source within the μPD72001.

The bits of SR2B that are affected depend on the Output Vector Type setting. Bits V4-V2 are affected for Type A vectors, and bits V2-V0 for Type B vectors. All other bits remain unchanged. Table 7 gives the value returned for the various types of interrupts.

Table 7. Vector Values in SR2B

V4, V2	V3, V1	V2, V0	Channel	Condition
0	0	0	B	Tx buffer empty
0	0	1		External/status
0	1	0		Rx data available
0	1	1		Special Rx condition
1	0	0	A	Tx buffer empty
1	0	1		External/status
1	1	0		Rx data available
1	1	1		Special Rx condition

When interrupts are available in the non-vectored mode (CR2A bit D7 = 0), SR2B is read in order to indicate to the μPD72001 that interrupt service has started. This clears the interrupt request (INT) and prevents lower priority interrupts from being generated until the End of Interrupt command (CR0) is issued.

Status Register SR3

TxBRG Zero Count [D4]

Bit D4 is valid when TxBRG is enabled (CR14 bit D0 = 1). A one in bit D0 indicates that the TxBRG counted down to zero. This bit in conjunction with the SR1 bit D0, causes an external/status interrupt and is latched on a transition from zero to one. The transition from one to zero does not cause an interrupt.

RxBRG Zero Count [D3]

Bit D3 is valid when RxBRG is enabled (CR14 bit D1 = 1). A one in bit D3 indicates that the RxBRG counted down to zero. This bit functions in the same manner as bit D4.

Residue Code [D2-D0]

Valid only in the BOP mode, bits D2-D0 indicate the number of valid bits in the last data byte received in a frame. The meaning of these bits depends on the number of bits per data byte. The previous character refers to the last character read before the end of frame, and so on. See Table 8. Figure 6 is an example of a residue code of 000 and a character length of 8 bits. It indicates that bits zero and one in the last byte are valid.

Figure 6. Example of Valid Bits in the I-Field (Residue Code = 000)

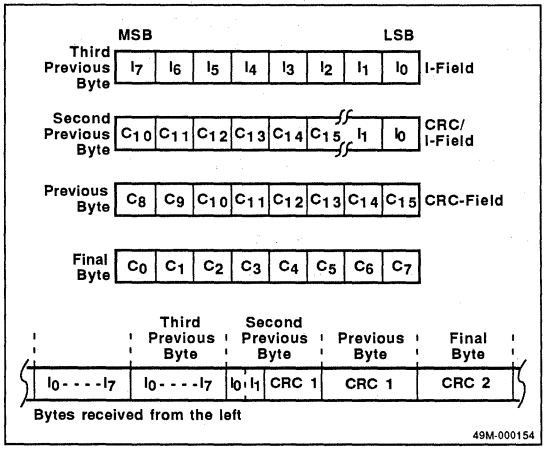


Table 8. Residue Codes

D2	D1	D0	Previous Character MSB							LSB	2nd Previous Character MSB							LSB
8 Bits per Character																		
0	0	0	C	C	C	C	C	C	C	C	C	C	C	C	C	C	D	D
0	0	1	C	C	C	C	C	C	C	C	C	C	D	D	D	D	D	D
0	1	0	C	C	C	C	C	C	C	C	C	C	C	C	D	D	D	D
0	1	1*	C	C	C	C	C	C	C	C	D	D	D	D	D	D	D	D
1	0	0	C	C	C	C	C	C	C	C	C	C	C	C	C	D	D	D
1	0	1	C	C	C	C	C	C	C	C	C	D	D	D	D	D	D	D
1	1	0	C	C	C	C	C	C	C	C	C	C	C	D	D	D	D	D
1	1	1	C	C	C	C	C	C	C	D	D	D	D	D	D	D	D	D
7 Bits per Character																		
0	0	0	X	C	C	C	C	C	C	D	X	D	D	D	D	D	D	D
0	0	1	X	C	C	C	C	C	C	C	X	C	C	D	D	D	D	D
0	1	0	X	C	C	C	C	C	C	C	X	C	C	C	C	D	D	D
0	1	1*	X	C	C	C	C	C	C	C	X	D	D	D	D	D	D	D
1	0	0	X	C	C	C	C	C	C	C	X	C	C	C	C	C	D	D
1	0	1	X	C	C	C	C	C	C	C	X	C	D	D	D	D	D	D
1	1	0	X	C	C	C	C	C	C	C	X	C	C	C	D	D	D	D
6 Bits per Character																		
0	0	0*	X	X	C	C	C	C	C	C	X	X	D	D	D	D	D	D
0	0	1	X	X	C	C	C	C	C	C	X	X	C	C	D	D	D	D
0	1	0	X	X	C	C	C	C	C	C	X	X	C	C	C	C	D	D
1	0	0	X	X	C	C	C	C	C	C	X	X	C	C	C	C	C	D
1	0	1	X	X	C	C	C	C	C	C	X	X	C	D	D	D	D	D
1	1	0	X	X	C	C	C	C	C	C	X	X	C	C	C	D	D	D
5 Bits per Character																		
0	0	0	X	X	X	C	C	C	C	C	X	X	X	C	D	D	D	D
0	0	1	X	X	X	C	C	C	C	C	X	X	X	C	C	D	D	D
0	1	0	X	X	X	C	C	C	C	C	X	X	X	C	C	C	C	D
1	0	0*	X	X	X	C	C	C	C	C	X	X	X	C	C	C	C	C
1	1	0	X	X	X	C	C	C	C	C	X	X	X	C	C	C	D	D

C = CRC bit
D = Valid data
X = Invalid
* = No residue (boundary of the last received data matches the boundary between one byte and the CRC).

Status Register SR4A

Each bit of this register indicates whether or not a corresponding cause of interrupt exists within the AMPSC. A bit is set to one when its matching interrupt is being serviced or if a lower-priority interrupt is pending during the servicing of a higher-priority interrupt. Otherwise, it is zero. Although this register can be read only on channel A, its function is shared by both channels.

Bit	Chan	Description
D7	A	Special Rx condition; INT pending
D6	B	Special Rx condition; INT pending
D5	A	Rx INT pending
D4	A	Tx INT pending
D3	A	E/S INT pending
D2	B	Rx INT pending
D1	B	Tx INT pending
D0	B	E/S INT pending

Status Register SR8

Valid only in the BOP mode, bits D7-D0 of SR8 are the low order byte of the Tx Data Length counter. Register SR8 is normally used to determine if frame transmission completed correctly. If the value of CR8/CR9 does not equal the value of SR8/SR9 when the transmitter underruns, the AMPSC automatically transmits an Abort. Registers SR8 and SR9 are cleared by a reset or when the TxDLC enable bit (CR13 bit D8) is set to one.

Status Register SR9

Valid only in the BOP mode, bits D7-D0 of SR9 are the high order byte of the Tx Data Length counter. Registers SR8 and SR9 are used in conjunction with each other.

Status Register SR10

One Clock Missing [D7]

This bit indicates if a transition has been detected in the received data. It is valid when the FM data format is selected and the DPLL is in operation. With FM data format, a transition (rising or falling) must occur within one bit time at a bit boundary or center. The DPLL uses this transition as a reference for clock generation.

If no transitions occur, the DPLL clock generation may not operate properly. The DPLL detects transitions every 2 bits.

A one in bit D7 indicates no transition was detected in the received data. This bit is latched, and is reset by the Reset Missing Clock command (CR14 bits D7-D5 = 010) or the Enter Search command (CR14 bits D7-D5 = 001).

Two Clocks Missing [D6]

Bit D6 indicates that two consecutive transitions in the received data were missed.

Sending on Loop [D4]

Bit D4 set to the one state indicates that the AMPSC is in the SDLC loop connection and is transmitting. It is valid only in the BOP mode when the SDLC Loop is selected (CR10 bits D4, D1 = 1,1).

Tx Sync/On Loop [D1]

Bit D1 is valid only in the COP or BOP mode. In the COP mode, a one in bit D1 indicates that the transmitter and receiver are synchronized (SYNC character detection on the receiver has been completed) after both the Auto Tx on Sync and the bit D4 Enable bits (CR10 bits D4,D1) were reset, and transmission is enabled for the device.

In the BOP mode, a one in bit D1 indicates that a GA pattern was detected and a 1-bit delay was inserted between the RxD input and the TxD output. Bit D1 remains a one during the time that the SDLC loop is formed. When D1 is zero, the TxD and RxD lines are connected without the delay in loop mode. Bit D1 is also zero when the AMPSC is not in the loop mode.

Status Register SR11

This register directly indicates the value set in CR11 for interrupt enables. The host processor can use SR11 to read the interrupt enable states for the various interrupt sources within the AMPSC.

Status Register SR12

This register indicates the lower 8 bits (bits 7-0) of the value set in the Rx BRG.

Status Register SR13

This register indicates the upper 8 bits (bits 15-8) of the value set in the Rx BRG.

Status Register SR14

This register indicates the lower 8 bits (bits 7-0) of the value set in the Tx BRG.

Status Register SR15

This register indicates the upper 8 bits (bits 15-8) of the value set in the Tx BRG.

GRAPHICS CONTROLLERS

Section 3
Graphics Controllers

μPD7220A High-Performance Graphics Display Controller

Description

The μPD7220A high-performance graphics display controller (HGDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the HGDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the HGDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the HGDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the HGDC is ideal for advanced computer graphics applications.

For a more detailed description of the HGDC's operation, please refer to the 7220/7220A design manuals.

System Considerations

The HGDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the HGDC's design, each of the system components is used to the maximum extent through a six-level hierarchy of simultaneous tasks. At the lowest level, the HGDC generates the basic video raster timing, including sync and blanking signals. Partitioning areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the HGDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the HGDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the HGDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

Features

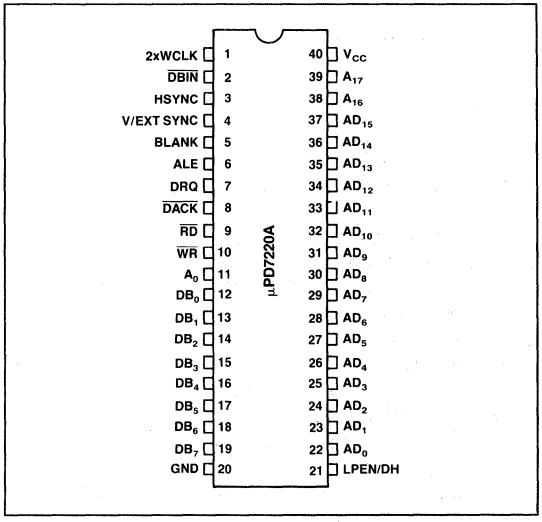
- ☐ Microprocessor interface
  - — DMA transfers with 8257- or 8237-type controllers
  - — FIFO command buffering
- ☐ Display memory interface
  - — Up to 256K words of 16-bits
  - — Read-modify-write (RMW) display memory cycles as fast as 500 ns
  - — Dynamic RAM refresh cycles for nonaccessed memory
- ☐ Light pen input
- ☐ Drawing hold input
- ☐ External video synchronization mode
- ☐ Graphic mode
  - — Four megabit, bit-mapped display memory
- ☐ Character mode
  - — 8K character code and attributes display memory
- ☐ Mixed graphics and character mode
  - — 64K if all characters
  - — 1 megapixel if all graphics
- ☐ Graphics capabilities
  - — Figure drawing of lines, arc/circles, rectangles, and graphics characters in 500 ns per pixel
  - — Display 1024-by-1024 pixels with 4 planes of color or grayscale
  - — Two independently scrollable areas
- ☐ Character capabilities
  - — Auto cursor advanced
  - — Four independently scrollable areas
  - — Programmable cursor height
  - — Characters per row: up to 256
  - — Character rows per screen: up to 100
- ☐ Video display format
  - — Zoom magnification factors of 1 to 16
  - — Panning
  - — Command-settable video raster parameters
- ☐ NMOS technology
- ☐ Single +5 V power supply
- ☐ DMA capability
  - — Bytes or word transfers
  - — 4 clock periods per byte transferred
- ☐ On-chip pull-up resistor for VSYNC/EXT, HSYNC and $\overline{\text{DACK}}$, and a pull-down resistor for LPEN/DH

3

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7220AD	40-pin ceramic DIP	6 MHz
μPD7220AD-1	40-pin ceramic DIP	7 MHz
μPD7220AD-2	40-pin ceramic DIP	8 MHz

Pin Configuration



Character Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Line counter bits 0 to 2 outputs
38	AD_{16}	Line counter bit 3 output
39	AD_{17}	Cursor output and line counter bit 4

Mixed Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Address and data bits 13 to 15
38	A_{16}	Attribute blink and clear line counter output
39	A_{17}	Cursor and bit-map area flag output

Pin Identification

Pin No.	Pin Symbol	Function
1	2xWCLK	Clock input
2	$\overline{DBIN}$	Display memory read input flag
3	HSYNC	Horizontal video sync output
4	V/EXT SYNC	Vertical video sync output or external VSYNC input
5	BLANK	CRT blanking output
6	ALE	Address latch enable output
7	DRQ	DMA request output
8	$\overline{DACK}$	DMA acknowledge input
9	$\overline{RD}$	Read strobe input for microprocessor interface
10	$\overline{WR}$	Write stobe input for microprocessor interface
11	A_0	Address select input for microprocessor interface
12-19	DB_0-DB_7	Bidirectional data bus to host microprocessor
20	GND	Ground
21	LPEN/DH	Light pen detect input drawing hold input
22-34	AD_0-AD_{12}	Address data lines to display memory
35-37	AD_{13}-AD_{15}	Utilization varies with mode of operation
38	A_{16}	Utilization varies with mode of operation
39	A_{17}	Utilization varies with mode of operation
40	V_{CC}	+5 V ±10% power supply

Graphics Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Address and data bits 13 to 15
38	A_{16}	Address bit 16 output
39	A_{17}	Address bit 17 output

Pin Functions

2xWCLK [Clock Input]

2xWCLK is the clock input.

$\overline{DBIN}$ [Data Bus Input Enable]

The $\overline{DBIN}$ output indicates the time the AGDC will accept data read from display RAM during read-modify-write (RMW) cycles.

HSYNC [Horizontal Sync]

The HSYNC output indicates the time the CRT's beam is to start its retrace back to the left side of the screen.

V/EXT SYNC [Vertical SYNC Output/External Sync Input]

The AGDC can be programmed to output a vertical sync signal at the start of the return of the CRT's beam from the lower right of the screen to the upper left during vertical retrace. The AGDC may also be programmed to accept an external sync input when used in slave mode.

BLANK [Blank]

BLANK is output during inactive display times (horizontal and vertical retrace) of the CRT and during a read-modify-write memory cycle when in flash mode.

ALE [Address Latch Enable]

The falling edge of ALE indicates the first clock cycle of a display memory cycle and the availability of the memory address on pins AD_0-AD_{17}. ALE and external logic can generate display memory control signals.

A_0 [Address Bit 0]

A_0 is the address select input for the microprocessor interface.

A_1 [Address Bit 1]

The A_1 input selects registers when reading or writing to the AGDC.

$\overline{DACK}$ [DMA Acknowledge]

$\overline{DACK}$ is the DMA acknowledge input handshake line that directly interfaces to the μPD8257 or μPD8237 DMA controller.

DRQ [DMA Request]

DRQ is the DMA request output handshake line that directly interfaces to the μPD8257 or μPD8237 DMA controller.

$\overline{RD}$ [Read Strobe]

The host CPU clears the $\overline{RD}$ input to 0 when reading the internal status and FIFO registers.

$\overline{WR}$ [Write Strobe]

The host CPU clears $\overline{WR}$ to 0 when writing to the internal command and parameter registers.

DB_0-DB_7 [Data Bus]

DB_0-DB_7, the 8-bit, three-state bidirectional data bus transfers data to and from the host CPU via the system bus.

LPEN/DH [Light Pen/Drawing Hold]

The LPEN/DH input can be programmed as either a light pen input or drawing hold input. The drawing hold input halts all read-modify-write operations.

AD_0-AD_{17} [Address and Data Lines]

AD_0-AD_{17} are address and data lines to display memory. AD_{13}-AD_{17} functions vary with the mode of operation of the ADGC. The μPD7220/7220A Graphics Display Controller User's Manual describes these functions and modes of operation.

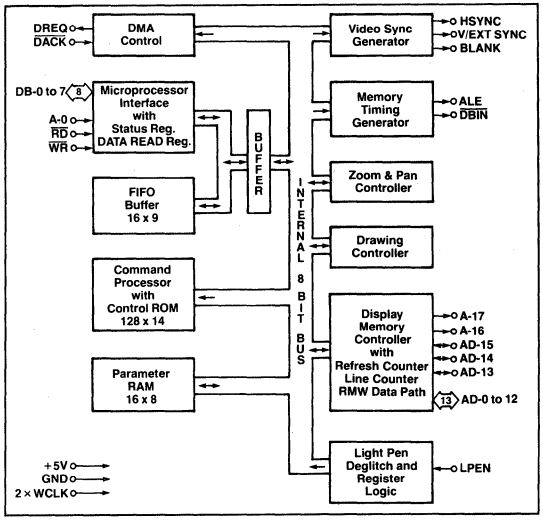
V_{CC} [Power Supply]

V_{CC} is the +5 V power supply input.

GND [Ground]

GND is ground potential.

Block Diagram



HGDC Components

Microprocessor Bus Interface

Control of the HGDC by the system microprocessor is achieved through an 8-bit bidirectional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal HGDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

Applications

NEC Electronics Inc. recently learned that application of the μPD7220 or μPD7220A Graphics Display Controller in conjunction with other non-NEC Electronics Inc. equipment to achieve panning and zooming capabilities may infringe U.S. Patents 4,197,590 and RE 31,200 held by CADTRAK CORPORATION of Sunnyvale, Ca. Neither the μPD7220 nor the μPD7220A Graphics Display Controllers by themselves infringe CADTRAK's patents. CUSTOMERS OF NEC ELECTRONICS INC. ARE HEREBY GIVEN NOTICE OF THE EXISTENCE OF THE CADTRAK PATENTS. USER'S ARE RESPONSIBLE FOR INSURING THAT THEIR SYSTEM DESIGN, MANUFACTURE AND RESULTING PRODUCT DO NOT VIOLATE ANY APPLICABLE PATENTS.

Command Processor

The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destinations within the HGDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

DMA Control

The DMA control circuitry in the HGDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a μPD8257 or μPD8237 DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

Parameter RAM

The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

Video Sync Generator

Based on the clock input, the sync logic generates the raster timing signals for almost interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple HGDCs.

Memory Timing Generator

The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle, which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the HGDC's ALE and $\overline{\text{DBIN}}$ outputs.

Zoom & Pan Controller

Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independently of the other display areas.

Drawing Controller

The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing controller needs no further assistance to complete the figure drawing.

Display Memory Controller

The display memory contoller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMs. The memory controller apportions the video field time between the various types of cycles.

Light Pen Deglitcher/Drawing Hold

Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address. If this input is held high for a period greater than four 2xWCLK cycles, drawing execution is halted when bit 7 of P5 of the SYNC command is set.

Programmer's View of HGDC

The HGDC occupies two addresses on the system microprocessor bus through which the HGDC's status register and FIFO are accessed. Commands and parameters are written into the HGDC's FIFO and are differentiated based on address bit A_0. The status register or the FIFO can be read as selected by the address line.

Commands to the HGDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacks the parameters, loads them into the appropriate registers within the HGDC, and initiates the required operations.

The commands available in the HGDC can be organized into five categories as described in the following section.

HGDC Microprocessor Bus Interface Registers

A0	READ	WRITE
0	Status Register	Parameter Into FIFO
1	FIFO Read	Command Into FIFO

HGDC Commands Summary

Video Control Commands

1. RESET1 — Resets the GDC to its idle state. Resychronizes video timing. Blanks the display.
2. RESET2 — Resets the HGDC to its idle state. Does not resynchronize video timing. Blanks the display.
3. RESET3 — Resets the HGDC to its idle state. Does not resynchronize video timing. Does not blank the display.
4. SYNC — Specifies the video display format.
5. VSYNC — Selects master or slave video synchronization mode.
6. CCHAR — Specifies the cursor and character row heights.

Display Control Commands

1. START — Ends idle mode and unblanks the display.
2. BLANK1 — Controls the blanking and unblanking of the display, along with video resynchronization.
3. BLANK2 — Controls the blanking and unblanking of the display. Does not blank the display.
4. ZOOM — Specifies zoom factors for the display and graphics characters writing.
5. CURS — Sets the position of the cursor in display memory.
6. PRAM — Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
7. PITCH — Specifies the width of the X dimension of display memory.

Drawing Control Commands

1. WDAT — Writes data words or bytes into display memory.
2. MASK — Sets the mask register contents.
3. FIGS — Specifies the parameters for the drawing controller.
4. FIGD — Draws the figure as specified above.
5. GCHRD — Draws the graphics character into display memory.

Data Read Commands

1. RDAT Reads data words or bytes from display memory.
2. CURD Reads the cursor position.
3. LPRD Reads the light pen address.

DMA Control Commands

1. DMAR Requests a DMA read transfer.
2. DMAW Requests a DMA write transfer.

Status Register Flags

SR-7: Light Pen Detect

When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

SR-6: Horizontal Blank Active/Vertical Blank Active

A 1 value for this flag signifies that horizontal retrace blanking or vertical retrace blanking is currently underway dependent on the status of the VH bit in SYNC or the RESETx parameter 6.

SR-5: Vertical Sync

Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

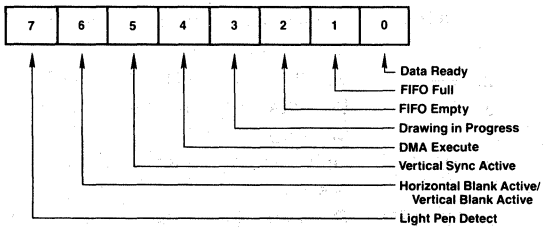
SR-4: DMA Execute

This bit is a 1 during DMA data tranfers.

SR-3: Drawing in Progress

While the HGDC is drawing a graphics figure, this status bit is a 1.

Status Register (SR)



SR-2: FIFO Empty

This bit and the FIFO-full flag coordinate system microprocessor accesses with the HGDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the HGDC have been interpreted.

SR-1: FIFO Full

A 1 at this flag indicates a full FIFO in the HGDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked before each write into the HGDC.

SR-0: Data Ready

When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

FIFO Operation & Command Protocol

The first-in, first-out buffer (FIFO) in the HGDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the HGDC's command set. The host microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the HGDC requires differentiation of the first byte of a command sequence from the succeeding bytes. The first byte contains the operation code and the remaining bytes carry parameters. Writing into the HGDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the HGDC tests this bit as it interprets the entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the HGDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the HGDC always put the FIFO into write mode if it was not in it already. If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require an HGDC response, such as RDAT, CURD and LPRD, put the FIFO into read mode after the command is interpreted by the HGDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

Read-Modify-Write Cycle

Data transfers between the HGDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four-clock period timing of the RMW cycle is used to 1. output the address, 2. read data rom the memory, 3. modify the data, and 4. write the modified data back into the initially selected memory address. This type of memory cycle is used for all interactions with display memory including DMA transfers, except for the two-clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the HGDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT parameters or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with ones in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a 4-bit dAD field to specify the dot address. The command processor converts this parameter into the 1-of-16 format used in the Mask register for figure drawing. A full 16-bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

The Logic unit combines the data read from display memory, the Pattern register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the Pattern register data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

Figure Drawing

The HGDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 8 MHz, this is equal to 500 ns. During the RMW cycle the HGDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the HGDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the HGDC's internal RMW logic.

During the drawing process, the HGDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The HGDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counter-clockwise.

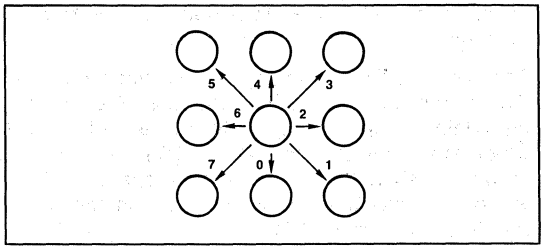
Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer to the right or left. The table below summarizes these operations for each direction.

Dir	Operations to Address the Next Pixel
000	EAD – P → EAD
001	EAD – P → EAD dAD (MSB) = 1:EAD – 1 → EAD dAD → LR
010	dAD (MSB) = 1:EAD – 1 → EAD dAD → LR
011	EAD – P → EAD dAD (MSB) = 1:EAD – 1 → EAD dAD → LR
100	EAD – P → EAD
101	EAD – P → EAD dAD (LSB) = 1:EAD – 1 → EAD dAD → RR
110	dAD (LSB) = 1:EAD – 1 → EAD dAD → RR
111	EAD – P → EAD dAD (LSB) = 1:EAD – 1 → EAD dAD → RR

Note:

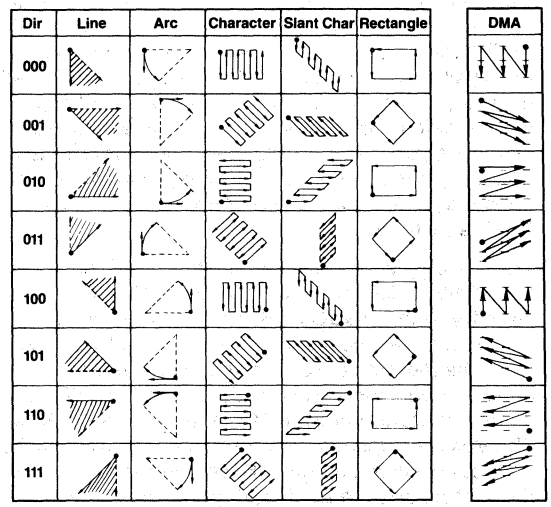
P = Pitch, LR = Left Rotate, RR = Right Rotate, EAD = Execute Word Address, and dAD = Dot Address stored in the Mask register.

Drawing Directions



Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to affect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:



Note that during line drawing, the angle of the line may be anywhere within the shaded octant defined by the DIR value. Arc drawing starts in the direction initially specified by the DIR value and veers into an arc as drawing proceeds. An arc may be up to 45° in length. DMA transfers are done on word boundaries only, and follow the arrows indicated in the table to find successive word addresses. The slanted paths for DMA transfers indicate the HGDC changing both the X and Y components of the word address when moving to the next word. It does not follow a 45° diagonal path by pixels.

Drawing Parameters

In preparation for graphics figure drawing, the HGDC's Drawing processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the HGDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The HGDC Drawing controller coordinates the RMW circuitry and address registers to draw the specified figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specific details about the figure to be drawn are reduced by the microprocessor to form conducive to high-speed address calculations within the HGDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

Drawing Type	DC	D	D2	D1	DM
Initial Value (1)	0	8	8	−1	−1
Line	$\lvert\Delta I\rvert$	$2\lvert\Delta D\rvert - \lvert\Delta I\rvert$	$2(\lvert\Delta D\rvert - \lvert\Delta I\rvert)$	$2\lvert\Delta D\rvert$	−
Arc (2)	$r\sin\phi$	r−1	2(r−1)	−1	$r\sin\theta\downarrow$
Rectangle	3	A−1	B−1	−1	A−1
Area fill	B−1	A	A	−	−
Graphic character (3)	B−1	A	A	−	−
Read & write data	W−1	−	−	−	−
DMAW	D−1	C−1	−	−	−
DMAR	D−1	C−1	(C−1)/2/†	−	−

Note:

All numbers are shown in base 10 for convenience. The HGDC accepts base 2 numbers (2's complement notation) where appropriate.

(1) Initial values for the various parameters remain as each drawing process ends.

(2) Circles are drawn with 8 arcs, each of which span 45°, so that $\sin\phi = 1/\sqrt{2}$ and $\sin\theta = 0$.

(3) Graphic characters are a special case of bit-map area filling in which B and $A \leq 8$. If $A = 8$ there is no need to load D and D2.

Symbol Definitions

−1 = All ONES value.
− = No parameter bytes sent to HGDC for this parameter.
ΔI = The larger at Δx or Δy.
ΔD = The smaller at Δx or Δy.
r = Radius of curvature, in pixels.
ϕ = Angle from major axis to end of the arc. $\phi \leq 45°$.
θ = Angle from major axis to start of the arc. $\theta \leq 45°$.
↑ = Round up to the next higher integer.
↓ = Round down to the next lower integer.
A = Number of pixels in the initially specified direction.
B = Number of pixels in the direction at right angles to the initially specified direction.
W = Number of words to be accessed.
C = Number of bytes to be transferred in the initially specified direction. (Two bytes per word if word transfer mode is selected.)
D = Number of words to be accessed in the direction at right angles to the initially specified direction.
DC = Drawing count parameter which is one less than the number of RMW cycles to be executed.
DM = Dots masked from drawing during arc drawing.
† = Needed only for word reads.

Graphics Character Drawing

Graphics characters can be drawn into display memory pixel by pixel. The up to 8-by-8 character display is loaded into the HGDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

Once the parameter RAM has been loaded with up to eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the ZOOM command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor.

The movement of these PRAM bytes to the display memory is controlled by the parameters of the FIGS command.

Based on the specified height and width of the area to be drawn, the parameter RAM is scanned to fill the required area.

For an 8-by-8 graphics character, the first pixel drawn uses the LSB of RA-15, the second pixel uses bit 1 of RA-15, and so on, until the MSB of RA-15 is reached.

The HGDC jumps to the corresponding bit in RA-14 to continue the drawing. The progression then advances toward the LSB of RA-14. This snaking sequence is continued for the other 6 PRAM bytes. This progression matches the sequence of display memory addresses calculated by the drawing processor as shown above. If the area is narrower than 8 pixels wide, the snaking will advance to the next PRAM byte before the MSB is reached. If the area is less than 8 lines high, fewer bytes in the parameter RAM will be scanned. If the area is larger than 8 by 8, the HGDC will repeat the contents of the parameter RAM in two dimensions, as required to fill the area with the 8-by-8 mosaic. (Fractions of the 8-by-8 pattern will be used to fill areas which are not multiples of 8 by 8.)

Parameter RAM Contents: RAM Address RA-0 to RA-15

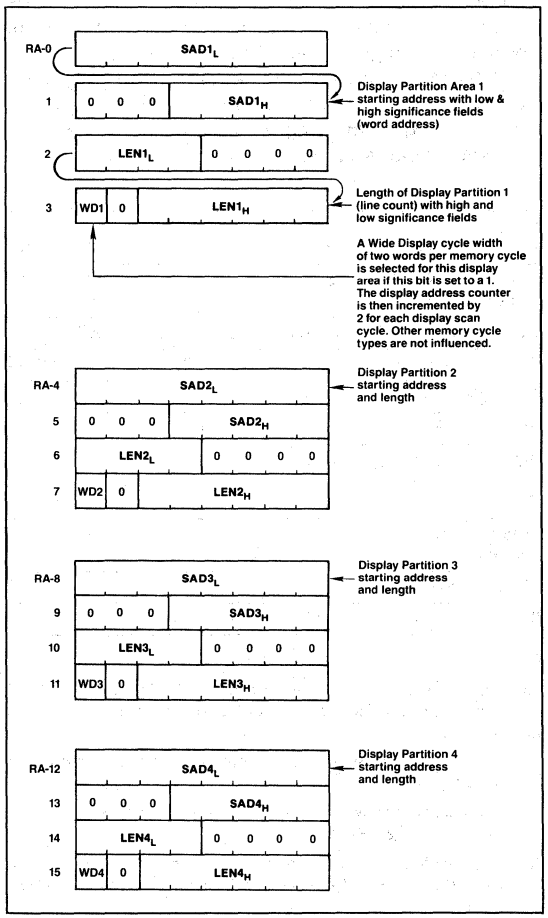
The parameters stored in the parameter RAM, PRAM, are available for the HGDC to refer to repeatedly during figure drawing and raster-scanning. In each mode of operation the values in the PRAM are interpreted by the HGDC in a predetermined fashion. The host microprocessor must load the appropriate parameters into the proper PRAM locations. PRAM loading command allows the host to write into any location of the PRAM and transfer as many bytes as desired. In this way any stored parameter byte or bytes may be changed without influencing the other bytes.

The PRAM stores two types of information. For specifying the details of the display area partitions, blocks of four bytes are used. The four parameters stored in each block include the starting address in display memory of each display area, and its length. In addition, there are two mode bits for each area which specify whether the area is a bit-mapped graphics area or a coded-character area, and whether a 16-bit or a 32-bit wide display cycle is to be used for that area.

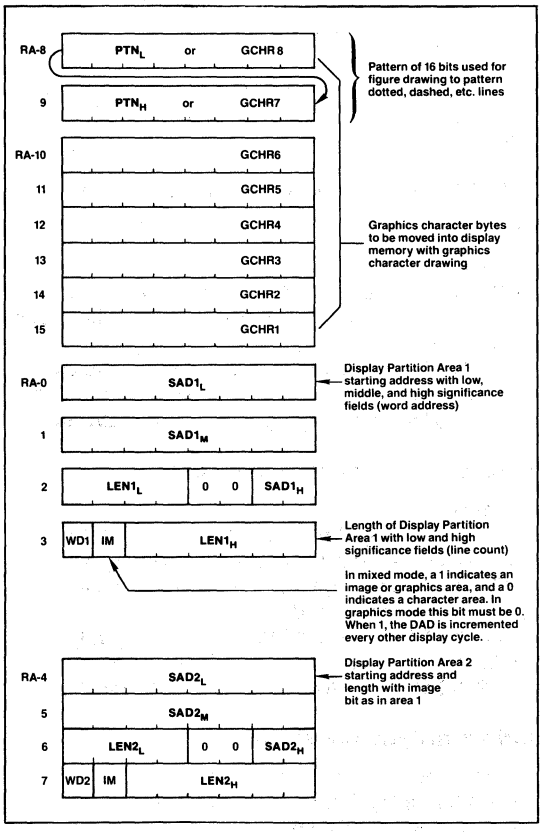
The other use for the PRAM contents is to supply the pattern for figure drawing when in a bit-mapped graphics area or mode. In these situations, PRAM bytes 8 through 16 are reserved for this patterning information. For line, arc, and rectangle drawing (linear figures) locations 8 and 9 are loaded into the Pattern register to allow the HGDC to draw dotted, dashed, etc. lines. For area filling and graphics bit-mapped character drawing, locations 8 through 15 are referenced for the pattern or character to be drawn.

Details of the bit assignments are shown for the various modes of operation.

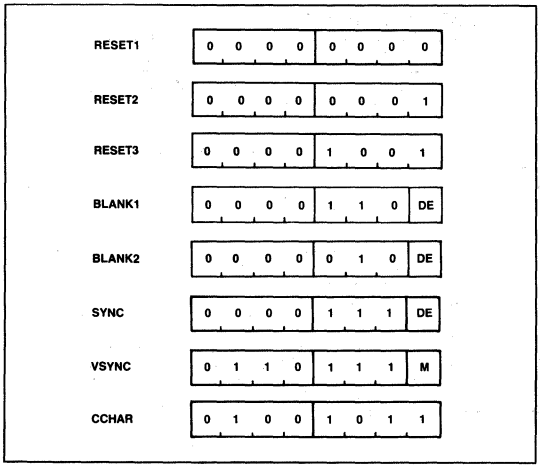
Character Mode



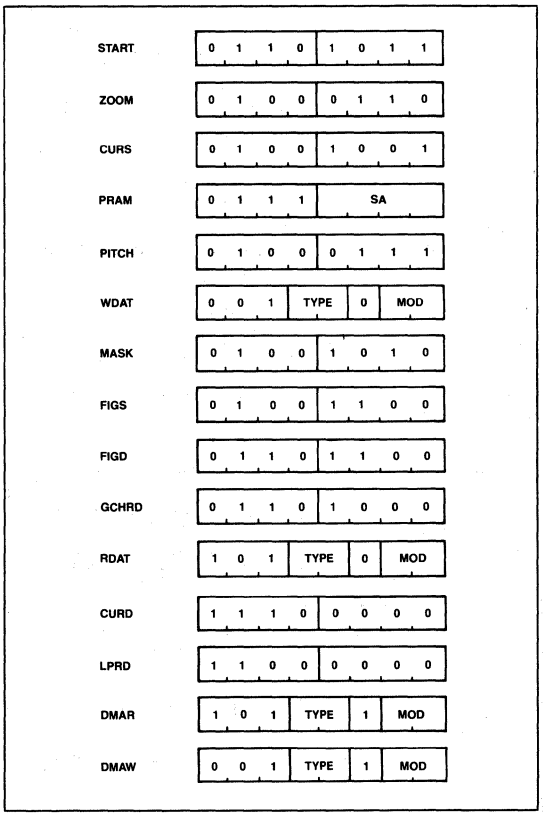
Graphics and Mixed Graphics and Character Modes



Command Bytes Summary

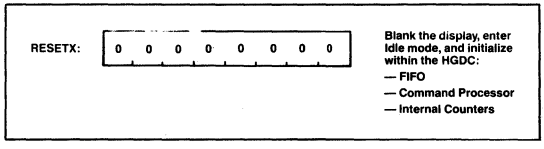


Command Bytes Summary



Video Control Commands

Reset



This command can be executed at any time and does not modify any of the parameters already loaded into the HGDC.

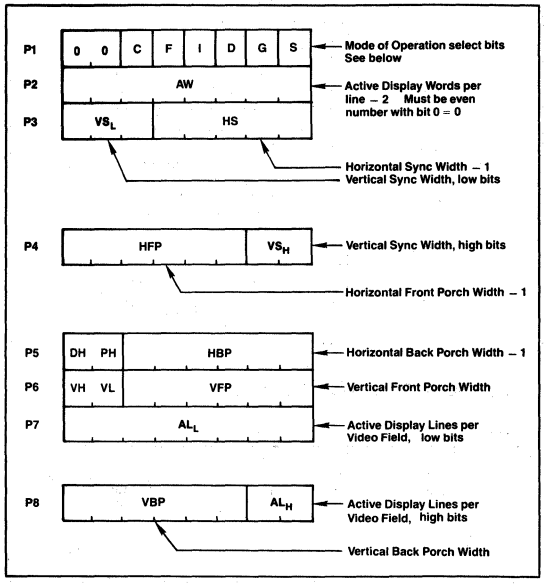
If followed by the parameter bytes, this command also sets the sync generator parameters as described below. Idle mode is exited with the START command.

RESET1: Resync video timing in slave mode.
RESET2: Blank the display and so not resync.
RESET3: Unblank the display and do not resync.

In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any. The number of active words per line must be an even number from 2 to 256. An all-zero parameter value selects a count equal to 2^n where n = number of bits in the parameter field for vertical parameters. All horizontal widths are counted in display words. All vertical invervals are counted in lines.

If the Drawing Hold (DH) is set to one, pin 21 (LPEN/DH) is used as the drawing hold control pin. When the input to LPEN/DH is held high for over four 2 x WCLK clocks, the drawing address output is temporarily held and the display address is output.

The HGDC allows an even or odd number of lines per frame. Selection is via the VL flag, the seventh bit of the sixth parameter byte following a RESET or SYNC command. When VL is 0, an odd number of display lines is generated.



VL	Number of lines in interfaced mode
0	Odd, as in 7220
1	Even

When VH = 0, status operation is as in μPD7220.

VH	Blank Status Bit Definition
0	Status register bit 6 indicates horizontal blank
1	Status register bit 6 indicates vertical blank

PH is the most significant bit (9) of the display pitch parameter. Use the PITCH command to set the lower eight bits.

SYNC Generator Period Constraints

Horizontal Back Porch Constraints

1. In general:
   HBP ≧ 3 Display Word Cycles (6 clock cycles).
2. If the Image bit or WD mode changes within one video field:
   HBP ≧ 5 Display Word Cycles (10 clock cycles).
3. If interlaced, mixed mode, or split screen is used:
   HBP ≧ 5 Display Word Cycles (10 clock cycles).

Horizontal Front Porch Constraints

1. In general:
   HFP ≧ 2 Display Word Cycles (4 clock cycles).
2. If the GDC is used in video sync Slave mode:
   HFP ≧ 4 Display Word Cycles (8 clock cycles).
3. If the Light Pen is used:
   HFP ≧ 6 Display Word Cycles (12 clock cycles).
4. If interlaced mode, DMA, or ZOOM is used:
   HFP ≧ 3 Display Word Cycles (6 clock cycles).

Horizontal Sync Constraints

1. If interlaced display mode is used:
   HS ≧ 5 Display Word Cycles (6 clock cycles).
2. If DRAM Refresh is enabled:
   HS ≧ 2 Display Word Cycles (4 clock cycles).

Modes of Operation Bits

C	G	Display Mode
0	0	Mixed graphics and character
0	1	Graphics mode
1	0	Character mode
1	1	Invalid

I	S	Video Framing
0	0	Non-interlaced
0	1	Invalid
1	0	Interlaced repeat field for character displays
1	1	Interlaced

Repeat Field Framing: 2 field sequence with 1/2 line offset between otherwise identical fields.
Interlaced Framing: 2 field sequence with 1/2 line offset. Each field displays alternate lines.
Non-Interlaced Framing: 1 field brings all the information to the screen.

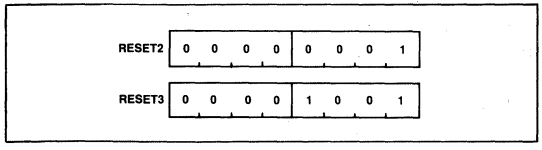
D	Dynamic RAM Refresh Cycles Enable
0	No refresh—static RAM
1	Refresh—dynamic RAM

Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

F	Drawing Time Window
0	Drawing during active display time and retrace blanking
1	Drawing only during retrace blanking

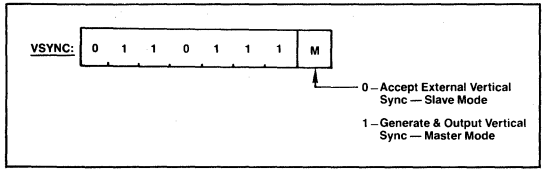
Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.

Both commands allow a reset while preventing re-initialization of the internal sync generator by an external sync source (slave mode).



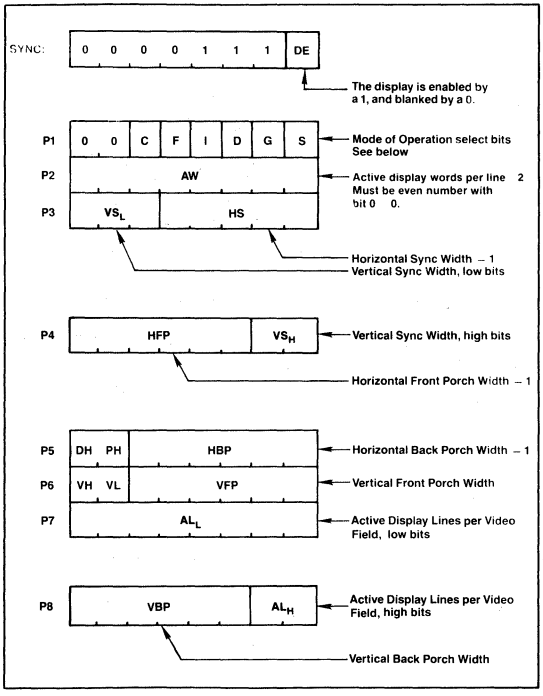
Vertical Sync Mode

When using two or more HGDCs to contribute to one image, one HGDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all HGDCs are connected together.



SYNC Format Specify

This command also loads parameters into the sync generator. The various parameter fields and bits are identical to those at the RESET command. The HDGC is not reset nor does it enter idle mode.



Slave Mode Operation

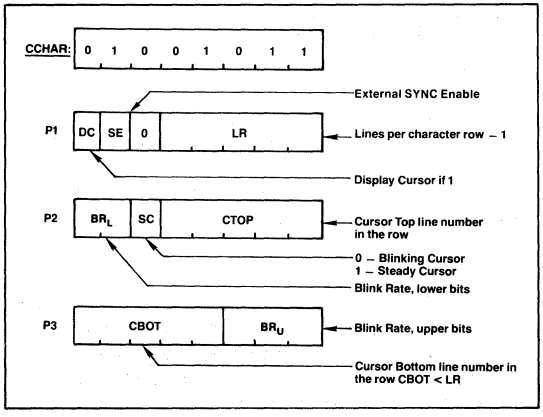
A few considerations should be observed when synchronizing two or more HGDCs to generate overlayed video via the V/EXT SYNC pin. As mentioned above, the Horizontal Front Porch (HFP) must be four or more display cycles wide. This is equivalent to eight or more clock cycles. This gives the slave HGDCs time to initialize their internal video sync generators to the proper point in the video field to match the incoming vertical sync pulse (VSYNC). This resetting of the generator occurs just after the end of the incoming VSYNC pulse, during the HFP interval. Enough time during HFP is required to allow the slave HGDC to complete the operation before the start of the HSYNC interval.

Once the HGDCs are initialized and set up as master and slaves, they must be given time to synchronize. It is a good idea to watch the VSYNC status bit of the master HGDC and wait until after one or more VSYNC pulses have been generated before the display progess is started. The START command will begin the active display of data and will end the video synchronization process, so be sure there has been at least one VSYNC pulse generated to which the slaves can synchronize.

Cursor and Character Characteristics

In graphics mode, LR should be set to 0. The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always one-half the cursor rate but with a 3/4-on-1/4-off duty cycle. **All three parameter bytes must be output for interlaced displays, regardless of mode.** For interlaced displays in graphics mode, the parameter $BR_L = 3$.

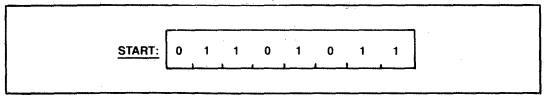
When SE = 0, the HGDC, in slave mode, detects the falling edge of EX. SYNC on the first frame. When SE = 1, the HGDC, in slave mode, detects the falling edge of EX. SYNC on every frame.



Display Control Commands

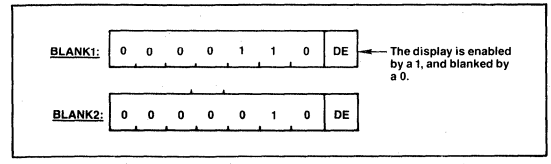
Start Display and End Idle Mode

The START command generates the video signals as specified by the RESETX or SYNC command.



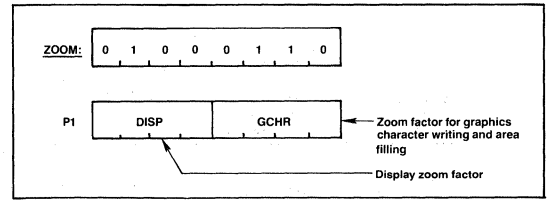
Display Blanking Control

BLANK2 does not cause the resyncing of an HGDC in slave mode. BLANK1 does cause the resyncing of an HGDC in slave mode.



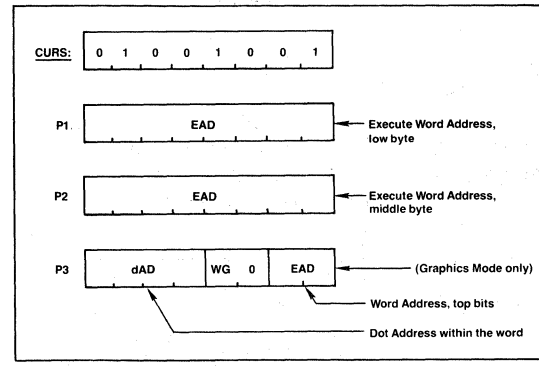
Zoom Factors Specify

Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.



Cursor Position Specify

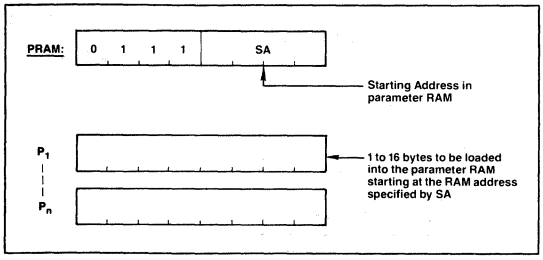
In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address. In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.



When the WG bit is set to one, any data following the WDAT command is written as is. When the WG bit is set to zero, the 7220A performs as the 7220 does: The pattern written is determined by the least significant bit of each parameter byte following the WDAT command. This bit is expanded into 16 identical bits which form the pattern.

Parameter RAM Load

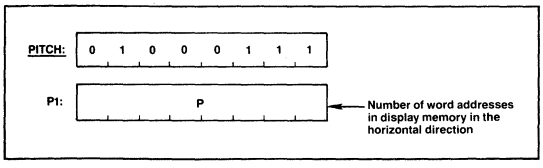
From the starting address, SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is determined by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.



Pitch Specification

This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

The Pitch parameter (width of display memory) is set by two different commands. In addition to the PITCH command, the RESET (or SYNC) command also sets the pitch value. The "active-words-per-line" parameter, which specifies the width of the raster-scan display, also sets the pitch of the display memory. Note that the AW value is two less than the display window width. The PITCH command must be used to set the proper memory width larger than the window width.



Drawing Control Commands

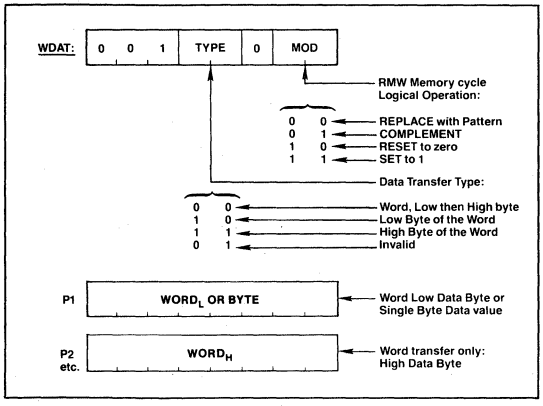
Write Data into Display Memory

Upon receiving a set of parameters (two bytes for a word transfer, one for a byte transfer), one RMW cycle into video memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.

For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

In graphics bit-map situations, only the LSB of the WDAT parameter bytes is used as the pattern in the RMW operations. Therefore it is possible to have only an all ones or all zeros pattern. If the WG bit of the third parameter of the CURS command is set to one, any byte following the WDAT command is written as is. In coded character applications all the bits of the WDAT parameters are used to establish the drawing pattern.

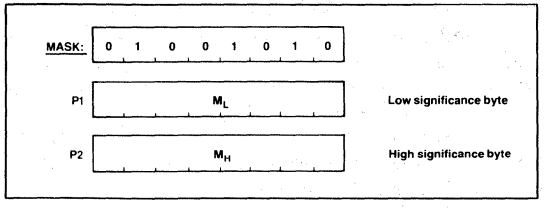
The WDAT command operates differently from the other commands which initiate RMW cycle activity. It requires parameters to set up the Pattern register while the other commands use the stored values in the parameter RAM. Like all of these commands, the WDAT command must be preceded by a FIGS command and its parameters. Only the first three parameters need be given following the FIGS opcode to set up the type of drawing, the DIR direction, and DC value. The DC parameter +1 will be the number of RMW cycles done by the HGDC with the first set of WDAT parameters. Additional sets of WDAT parameters will see a DC value of 0 which will cause only one RMW cycle to be executed per set of parameters.



Mask Register Load

This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

The Mask register is loaded both by the MASK command and the third parameter byte of the CURS command. The MASK command accepts two parameter bytes to load a 16-bit value into the Mask register. All 16-bits can be individually one or zero, under program control. The CURS command, on the other hand, puts a 1-of-16 pattern into the Mask register based on the value of the Dot Address value, dAD. If normal single-pixel-at-a-time graphics figure drawing is desired, there is no need to do a MASK command at all since the CURS command will set up the proper pattern to address the proper pixels as drawing progresses. For coded character DMA, and screen setting and clearing operations using the WDAT command, the MASK command should be used after the CURS command if its third parameter byte has been output. The Mask register should be set to all ones for any "word-at-a-time" operation.



Valid Figure Type Select Combinations

SL	R	A	GC	L	Operation
0	0	0	0	0	Character display mode drawing, individual dot drawing, DMA, WDAT, and RDAT
0	0	0	0	1	Straight line drawing
0	0	0	1	0	Graphics character drawing and area filling with graphics character pattern
0	0	1	0	0	Arc and circle drawing
0	1	0	0	0	Rectangle drawing
1	0	0	1	0	Slanted graphics character drawing and slanted area filling

Only these bit combinations assure correct drawing operation.

Figure Drawing Parameters Specify

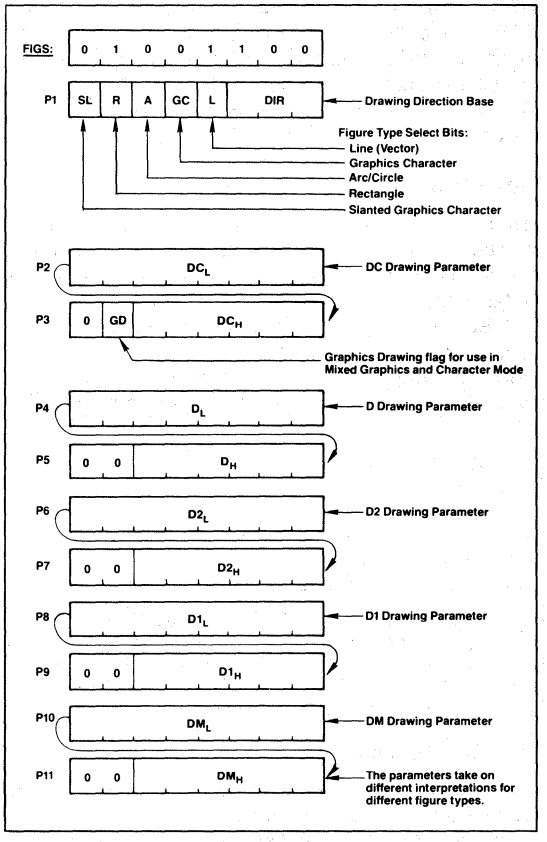
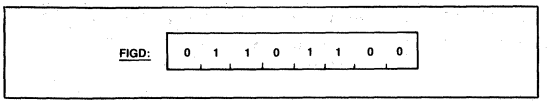


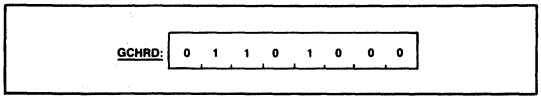
Figure Draw Start

On execution of this instruction, the HGDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.



Graphics Character Draw and Area Filling Start

Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

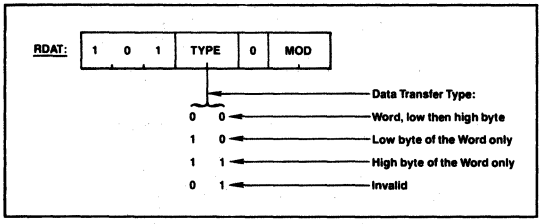


Data Read Commands

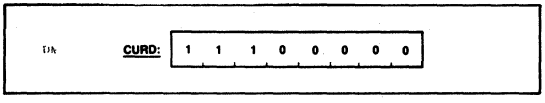
Read Data from Display Memory

Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes).

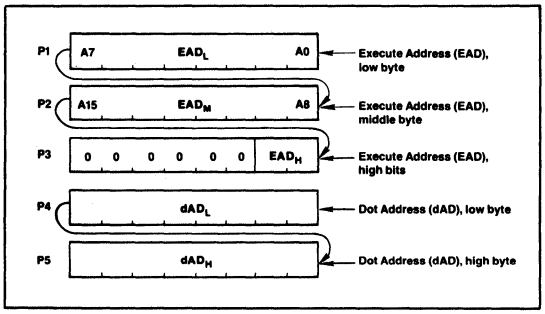
As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the HGDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost. MOD should be set to 00 if no modification to video buffer is desired.



Cursor Address Read



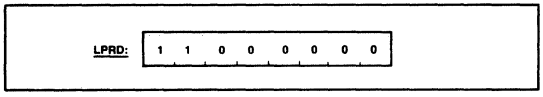
The following bytes are returned by the HGDC through the FIFO:



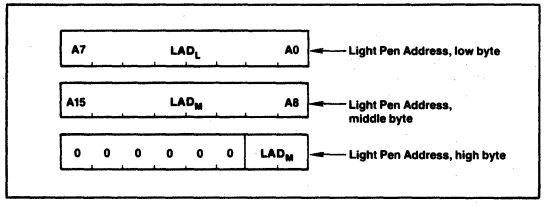
The execute address, EAD, points to the display memory word containing the pixel to be addressed.

The dot address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

Light Pen Address Read



The following bytes are returned by the HGDC through the FIFO:

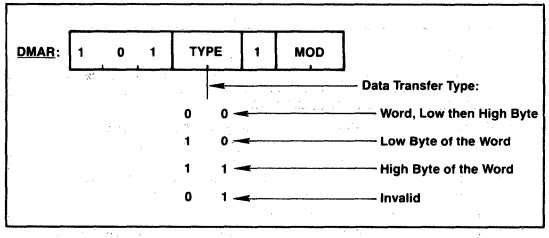


The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.

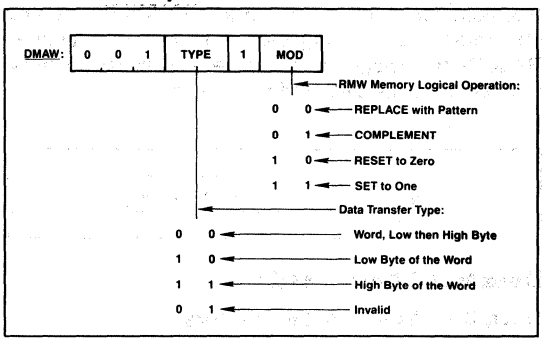
The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

DMA Control Commands

DMA Read Request



DMA Write Request



AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

		7220AD Limits		7220AD-1 Limits		7220AD-2 Limits			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Cycle (GDC ⟷ CPU)									
Address setup to $\overline{RD}\downarrow$	t_{AR}	0		0		0		ns	
Address hold from $\overline{RD}\uparrow$	t_{RA}	0		0		0		ns	
$\overline{RD}$ pulse width	t_{RH1}	$t_{RD1}+20$	$t_{RCY}-1/2\,t_{CLK}$	$t_{RD1}+20$	$t_{RCY}-1/2\,t_{CLK}$	$t_{RD1}+20$	$t_{RCY}-1/2\,t_{CLK}$	ns	
Data delay from $\overline{RD}\downarrow$	t_{RD1}		75		65		55	ns	C_L = 50 pF
Data floating from $\overline{RD}\uparrow$	t_{DF}	0	75	0	65	0	55	ns	
$\overline{RD}$ pulse cycle	t_{RCY}	4 t_{CLK}		4 t_{CLK}		4 t_{CLK}		ns	
Write Cycle (GDC ⟷ CPU)									
Address setup to $\overline{WR}\downarrow$	t_{AW}	0		0		0		ns	
Address hold from $\overline{WR}\uparrow$	t_{WA}	10		10		10		ns	
$\overline{WR}$ pulse width	t_{WW}	80	$t_{WCY}-t_{CLK}$	70	$t_{WCY}-t_{CLK}$	60	$t_{WCY}-t_{CLK}$	ns	
Data setup to $\overline{WR}\uparrow$	t_{DW}	65		55		45		ns	
Data hold from $\overline{WR}\uparrow$	t_{WD}	0		10		10		ns	
$\overline{WR}$ pulse cycle	t_{WCY}	4 t_{CLK}		4 t_{CLK}		4 t_{CLK}		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

Parameter	Symbol	7220AD Limits		7220AD-1 Limits		7220AD-2 Limits		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
DMA Read Cycle (GDC ⟷ CPU)									
$\overline{DACK}$ setup to $\overline{RD}\downarrow$	t_{KR}	0		0		0		ns	
$\overline{DACK}$ hold from $\overline{RD}\uparrow$	t_{RK}	0		0		0		ns	
$\overline{RD}$ pulse width	t_{RR2}	t_{RD2} + 20		t_{RD2} + 20		t_{RD2} + 20		ns	
Data delay from $\overline{RD}\downarrow$	t_{RD2}		1.5 t_{CLK} + 80		1.5 t_{CLK} + 70		1.5 t_{CLK} + 60	ns	C_L = 50 pF
DREQ delay from 2xWCLK↑	t_{REQ}		100		85		75	ns	C_L = 50 pF
DREQ setup to $\overline{DACK}\downarrow$	t_{QK}	0		0		0		ns	
$\overline{DACK}$ high-level width	t_{DK}	t_{CLK}		t_{CLK}		t_{CLK}		ns	
$\overline{DACK}$ pulse cycle	t_E	4 t_{CLK} (1)		4 t_{CLK} (1)		4 t_{CLK} (1)		ns	
DREQ↓ delay from $\overline{DACK}\downarrow$	$t_{KQ(R)}$		t_{CLK} + 100		t_{CLK} + 90		t_{CLK} + 80	ns	C_L = 50 pF
$\overline{DACK}$ low-level width	t_{LK}	2 t_{CLK}		2 t_{CLK}		2 t_{CLK}			
DMA Write Cycle (GDC ⟷ CPU)									
$\overline{DACK}$ setup to $\overline{WR}\downarrow$	t_{KW}	0		0		0		ns	
$\overline{DACK}$ hold from $\overline{WR}\uparrow$	t_{WK}	0		0		0		ns	
RMW Cycle (GDC ⟷ Display Memory)									
Address/data display from 2xWCLK↑	t_{AD}	20	105	20	90	15	80	ns	C_L = 50 pF
Address/data floating from 2xWCLK↑	t_{OFF}	20	105	20	90	15	80	ns	C_L = 50 pF
Input data setup to 2xWCLK↓	t_{DIS}	0		0		0		ns	
Input data hold from 2xWCLK↓	t_{DIH}	t_{DE}		t_{DE}		t_{DE}		ns	
$\overline{DBIN}$ delay from 2xWCLK↓	t_{DE}	20	80	20	70	15	60	ns	C_L = 50 pF
ALE↑ delay from 2xWCLK↑	t_{RR}	20	80	20	70	15	60	ns	C_L = 50 pF
ALE↓ delay from 2xWCLK↓	t_{RF}	20	65	20	55	15	50	ns	C_L = 50 pF
ALE high width	t_{RW}	1/3 t_{CLK}		1/3 t_{CLK}		1/3 t_{CLK}		ns	C_L = 50 pF
ALE low width	t_{RL}	1.5 t_{CLK} − 30		1.5 t_{CLK} − 30		1.5 t_{CLK} − 30		ns	
Address setup to ALE↓	t_{AA}	30		30		30			

Note:

(1) For high-byte and low-byte transfers: t_E = 5 t_{CLK}.

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

Parameter	Symbol	7220AD Limits Min	7220AD Limits Max	7220AD-1 Limits Min	7220AD-1 Limits Max	7220AD-2 Limits Min	7220AD-2 Limits Max	Unit	Test Conditions
Display Cycle (GDC ⟷ Display Memory)									
Video signal display from 2xWCLK↑	t_{VD}		90		80		70	ns	C_L = 50 pF
Input Cycle (GDC ⟷ Display Memory)									
Input signal setup to 2xWCLK↑	t_{PS}	10		10		10		ns	
Input signal width	t_{PW}	t_{CLK}		t_{CLK}		t_{CLK}		ns	
Clock (2xWCLK)									
Clock rise time	t_{CR}		15		15		15	ns	
Clock fall time	t_{CF}		15		15		15	ns	
Clock high pulse width	t_{CH}	70		61		52		ns	
Clock low pulse width	t_{CL}	70		61		52		ns	
Clock cycle	t_{CLK}	165	10000	145	10000	125	10000	ns	

Capacitance

T_A = 25°C; V_{CC} = GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			10	pF	f_C = 1 MHz
IO capacitance	C_{IO}			20	pF	V_I (unmeasured) = 0 V
Output capacitance	C_{OUT}			20	pF	
Clock input capacitance	$C\phi$			20	pF	

Absolute Maximum Ratings (Tentative)

Ambient temperature under bias	0 to +70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to +7 V
Power dissipation	1.5 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	−0.5		0.8	V	(Note 1)
Input high voltage	V_{IH}	2.2		V_{CC} + 0.5	V	(Notes 2, 3)
Output low voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output high voltage	V_{OH}	2.4			V	I_{OH} = −400 μA

DC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5 V ±10%; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low leak current (except VSYNC, $\overline{DACK}$)	I_{IL}			−10	μA	V_I = 0 V
Input low leak current (VSYNC, $\overline{DACK}$)	I_{IL}			−500	μA	V_I = 0 V
Input high leak current (except LPEN/DH)	I_{IH}			+10	μA	$V_I = V_{CC}$
Input high leak current (LPEN/DH)	I_{IH}			+500	μA	$V_I = V_{CC}$
Output low leak current	I_{OL}			−10	μA	V_O = 0 V
Output high leak current	I_{OH}			+10	μA	$V_O = V_{CC}$
Clock input low voltage	V_{CL}	−0.5		0.6	V	
Clock input high voltage	V_{CH}	3.5		V_{CC} + 1.0	V	
V_{CC} supply current	I_{CC}			270	mA	

Note:

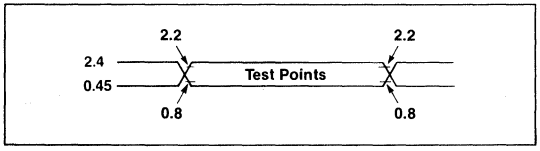
(1) For 2xWCLK, V_{IL} = −0.5 to +0.6 V.

(2) For 2xWCLK, V_{IH} = +3.9 V to V_{CC} +1.0 V.

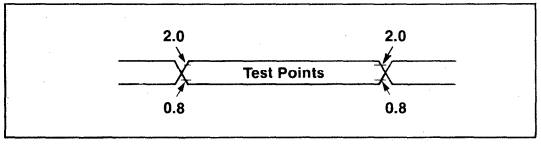
(3) For $\overline{WR}$, V_{IH} = 2.5 V to V_{CC} +0.5 V.

AC Testing Conditions

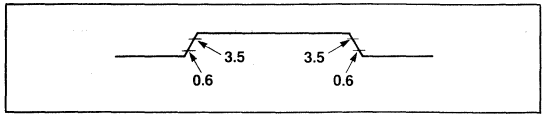
Input Waveform for AC Test (Except 2xCCLK)



Output Waveform for AC Test

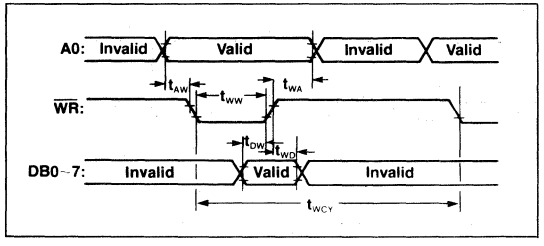


Clock Timing (2xCCLK)

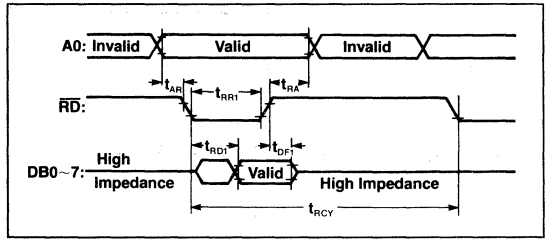


Timing Waveforms

Microprocessor Interface Write Timing

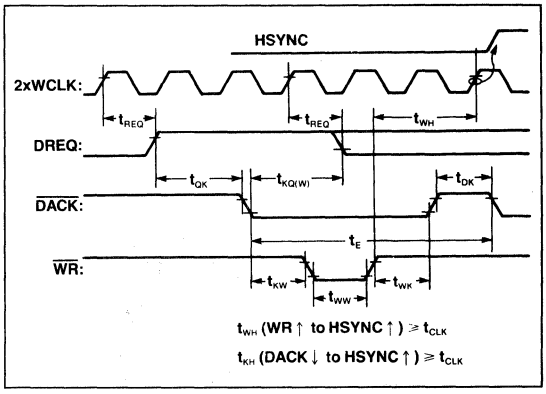


Microprocessor Interface Read Timing

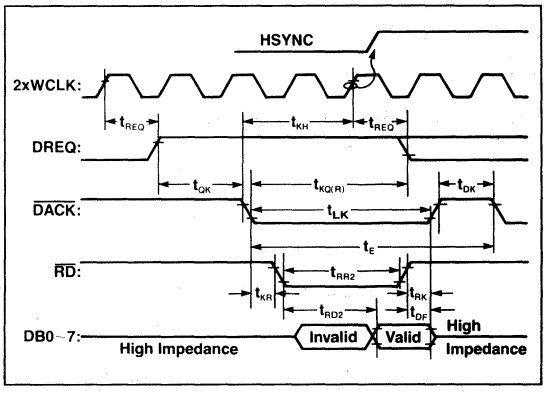


Timing Waveforms (cont)

Microprocessor Interface DMA Write Timing



Microprocessor Interface DMA Read Timing



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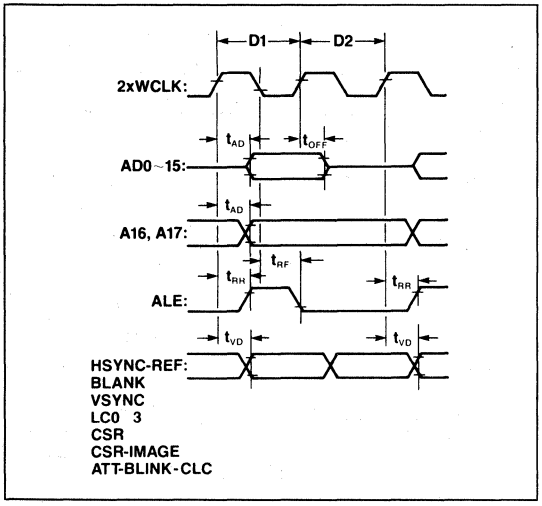
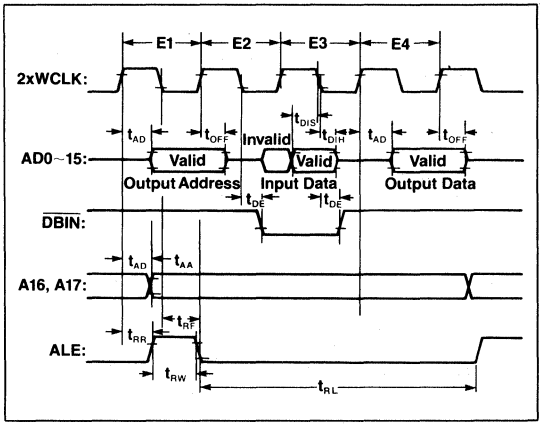
Timing Waveforms (cont)

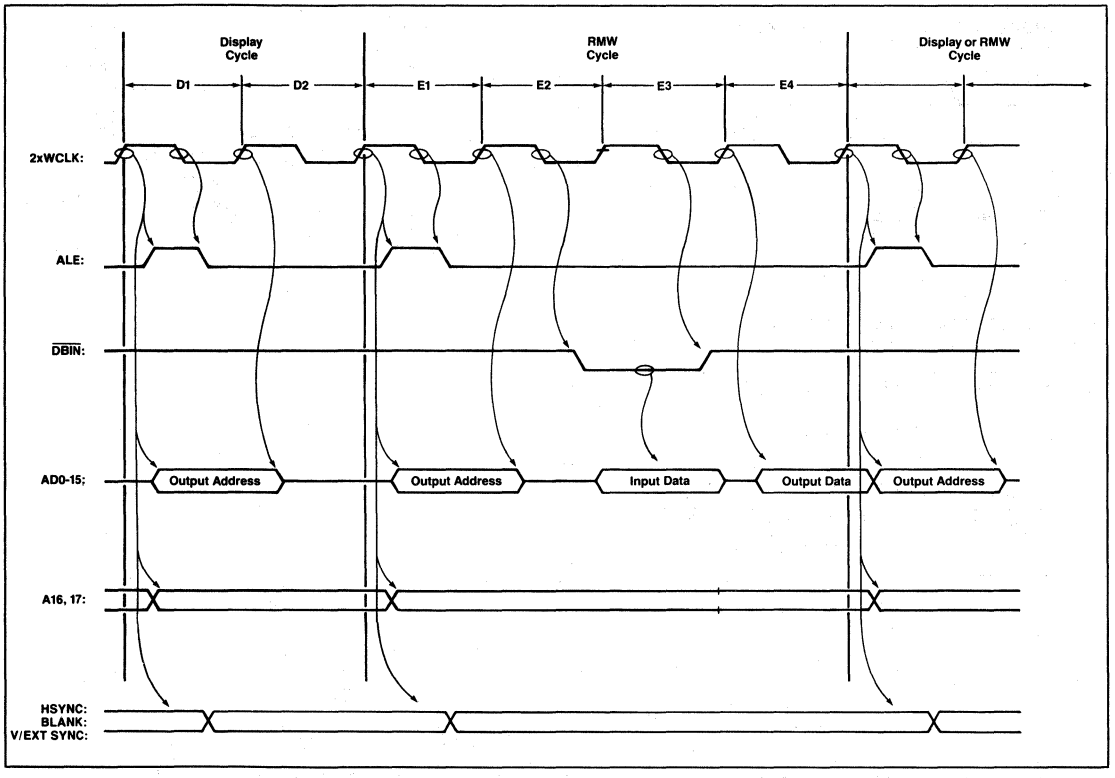
Display Memory Display Cycle Timing



Display Memory RMW Timing

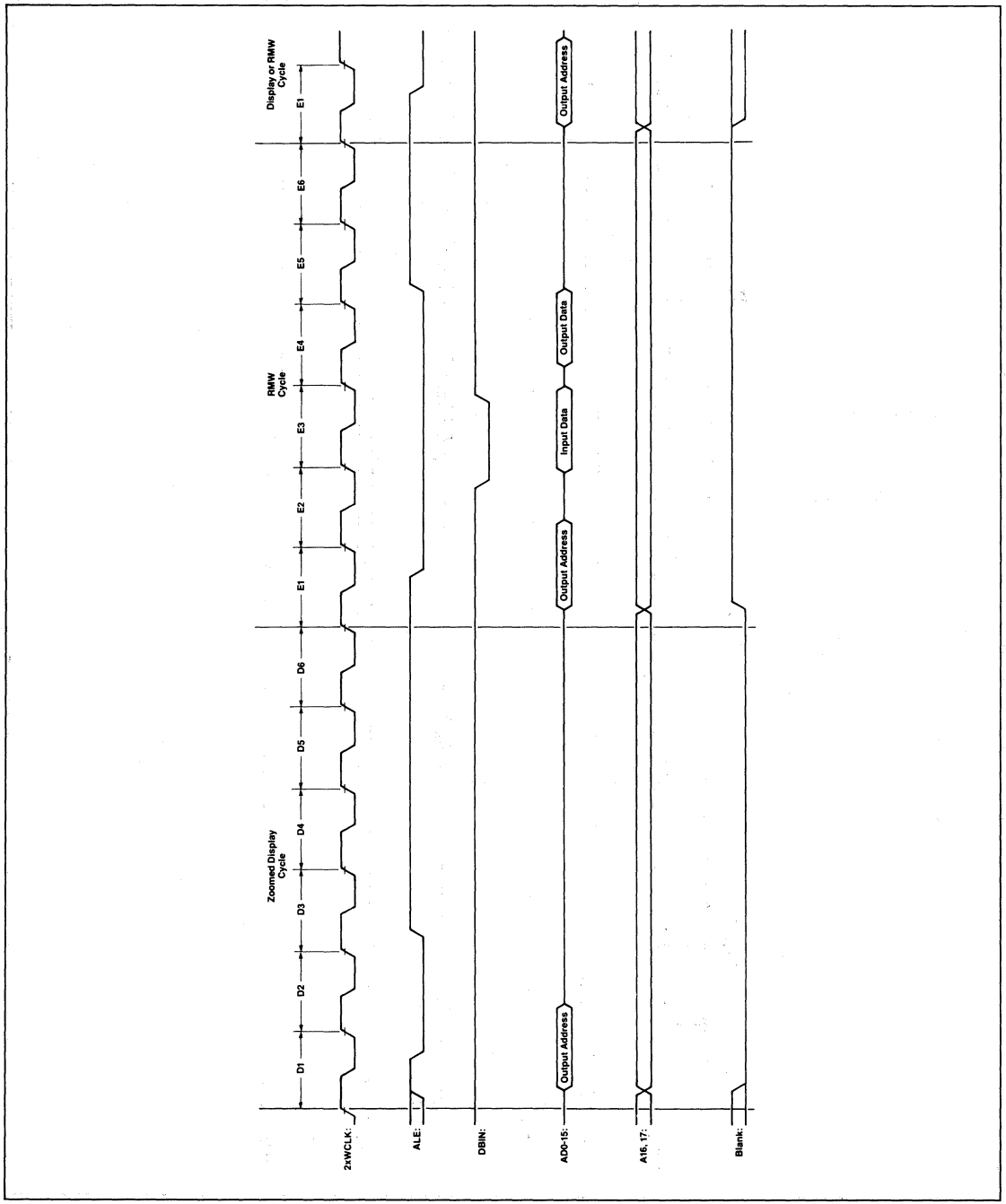


Display and RMW Cycles (1x Zoom)



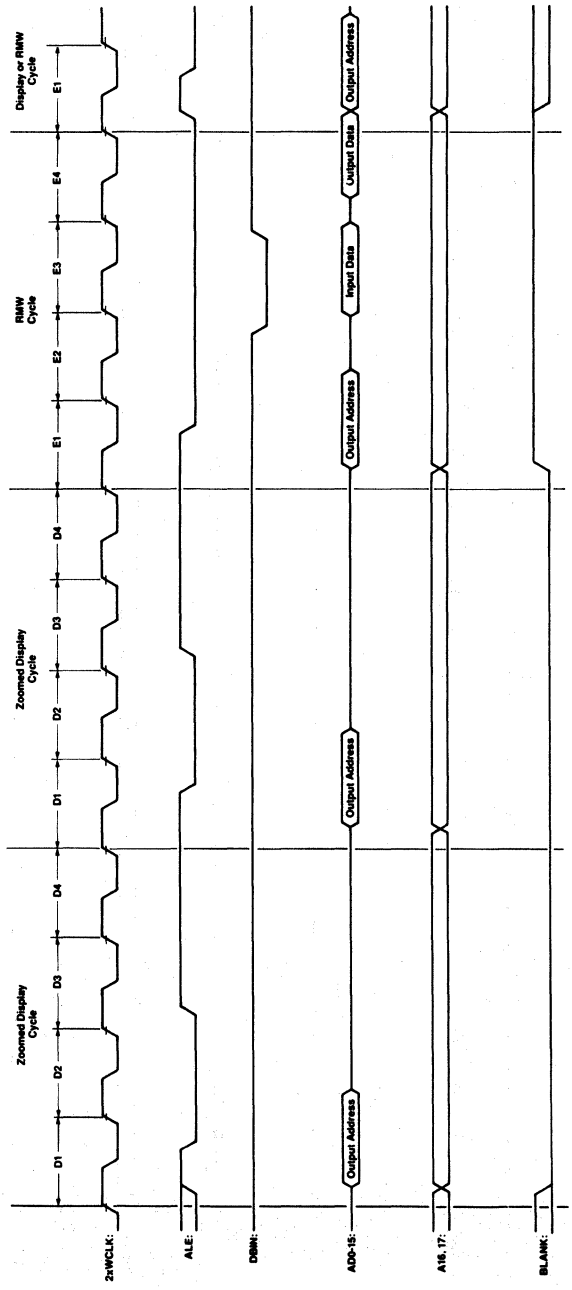
Timing Waveforms (cont)

Display and RMW Cycles (2x Zoom)



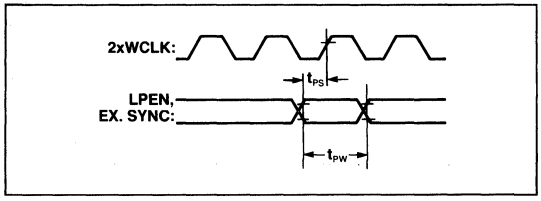
Timing Waveforms (cont)

Display and RMW Cycles (3x Zoom)

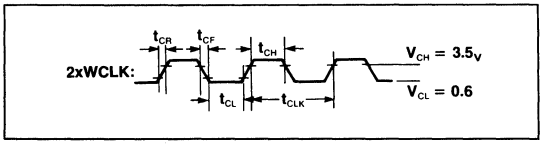


Timing Waveforms (cont)

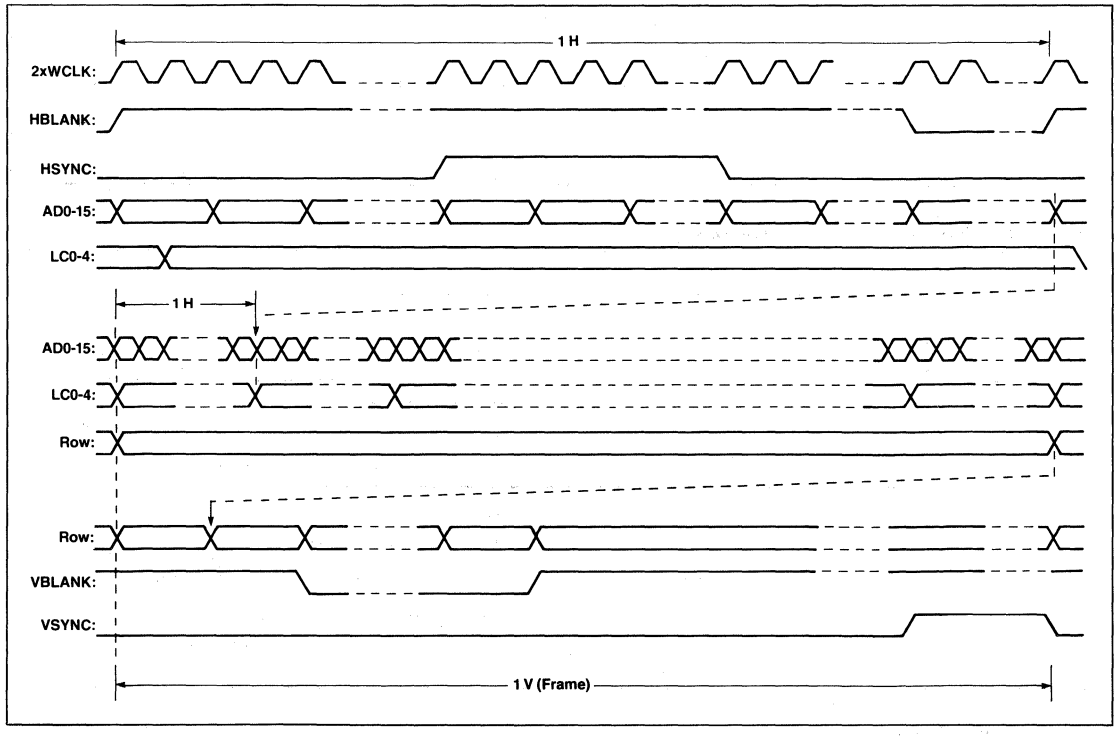
Light Pen and External Sync Input Timing



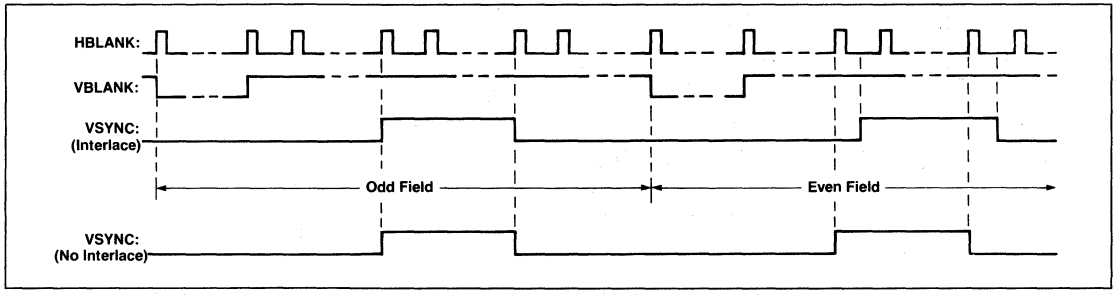
Clock Timing (2xWCLK)



Video Sync Signals Timing

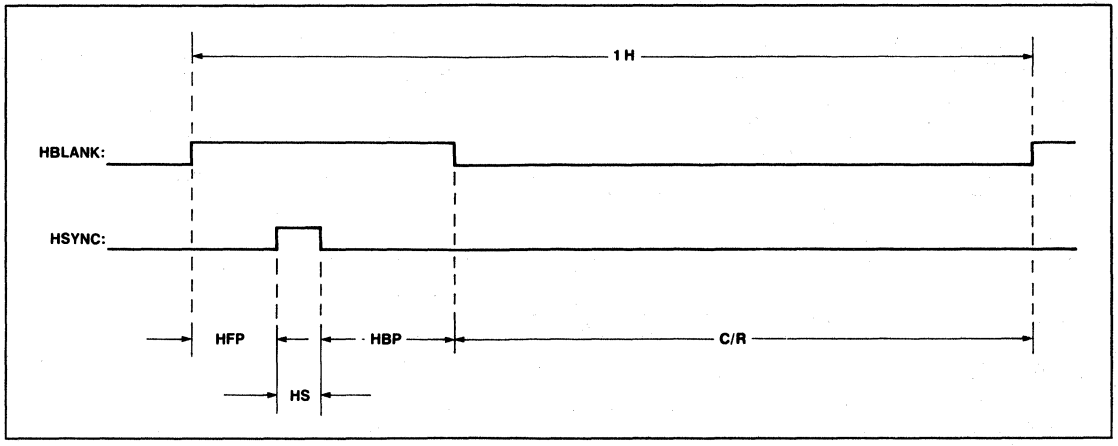


Interlaced Video Timing

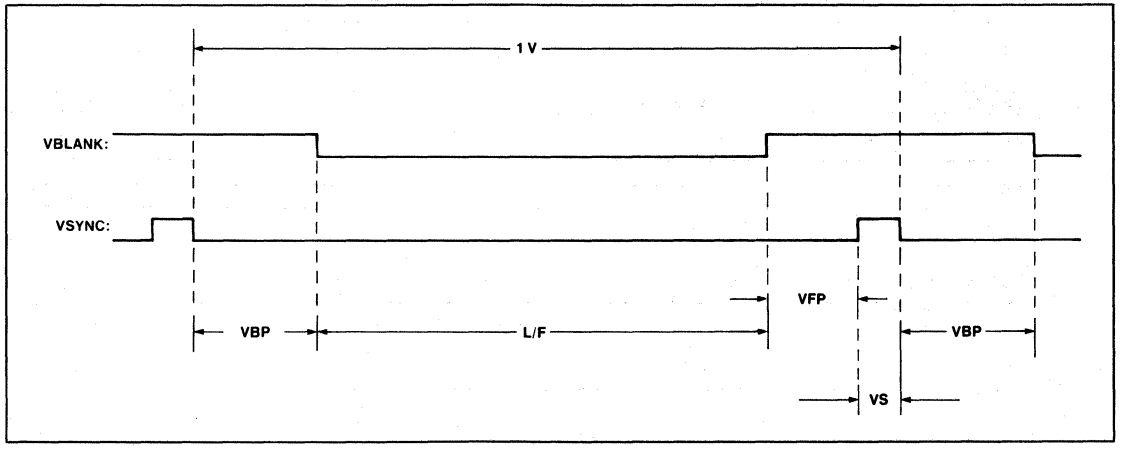


Timing Waveforms (cont)

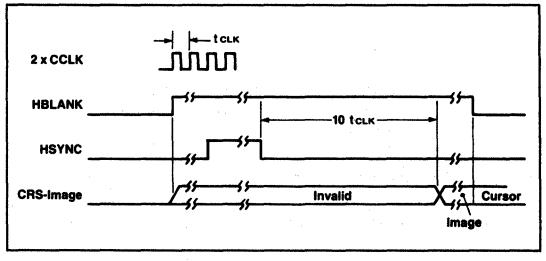
Video Horizontal Sync Generator Parameters



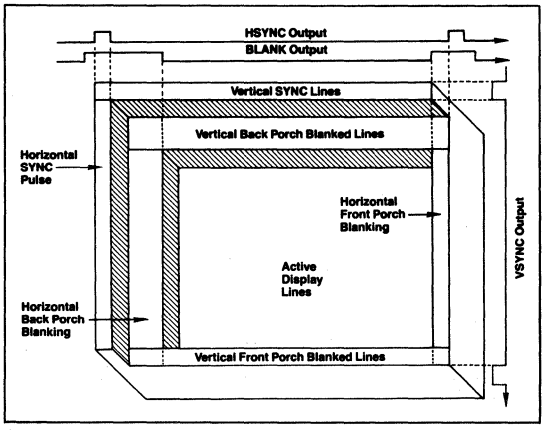
Video Vertical Sync Generator Parameters



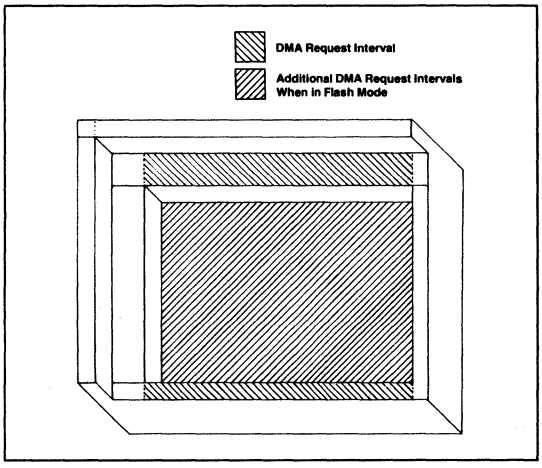
Cursor—Image Bit Flag



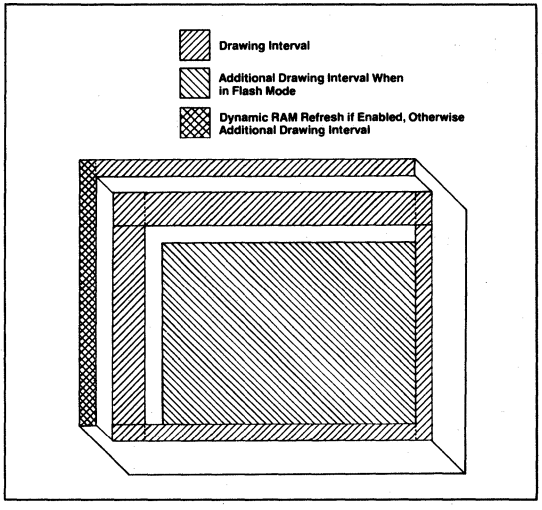
Video Field Timing



DMA Request Intervals



Drawing Intervals



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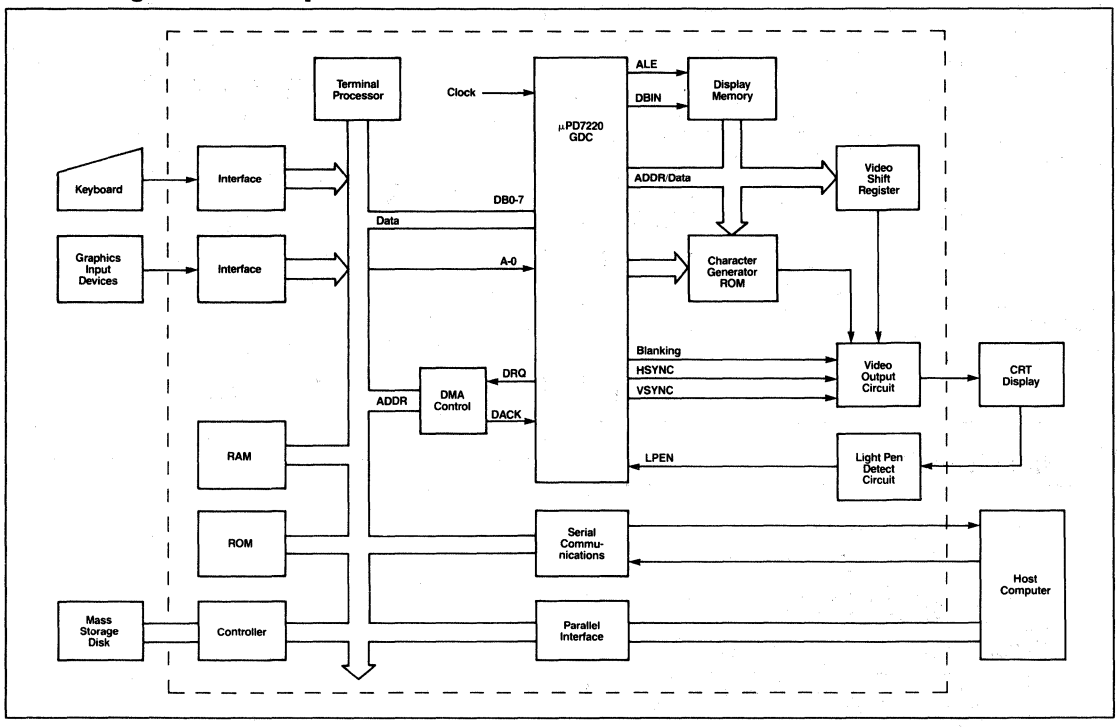
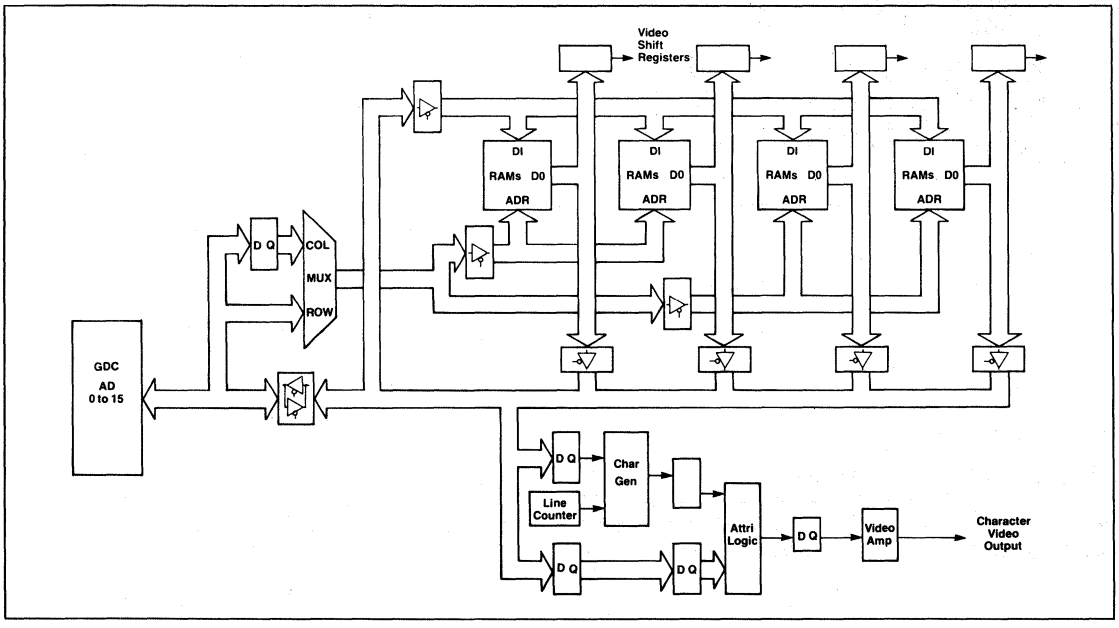
Block Diagram of a Graphics Terminal



Multiplane Display Memory Diagram



Description

The μPD72020 is an enhanced graphics display controller resulting from the implementation of CMOS technology on the μPD7220A.

In addition to the functions of the μPD7220A, the μPD72020 incorporates address space expansion, video RAM control, and write mask functions. It is suitable for a wide range of applications from simple display terminals to high-resolution graphics display devices.

This data sheet covers only functions additional to those of the μPD7220A. For further details of the μPD72020, refer to the μPD72020 User's Manual.

Features

- Enhanced functions compared with the μPD7220A
  - Video memory space: 2M bytes maximum (1M 16-bit words)
  - Control of dual-port RAM (video RAM)
  - Write-masking of any desired bit
  - Enhanced external synchronization function
  - CMOS technology
- μPD7220A-compatible functions
  - High-speed graphics drawing: 500 ns/dot (operating at 8 MHz)
  - Selection of drawing timing: flashless/flash mode
  - Drawing of straight lines, arcs, quadrilaterals, graphic characters
  - Any kind of line specifiable
  - Four different dot-correction modes
  - Enlarged drawing/enlarged display
  - Panning and scrolling
  - Automatic cursor shifting
  - Attributes assignable character by character
  - Interlaced/noninterlaced scanning
  - DRAM refreshing
  - Master/slave operation
  - Video memory control independent of main memory
  - 16 x 9-bit on-chip input/output FIFO
  - DMA control
  - Single +5-volt power supply

Applications

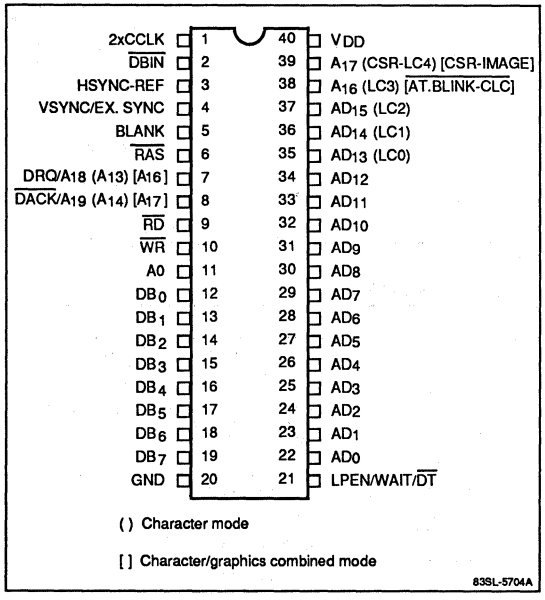
Some application functions implemented by use of this product in conjunction with other products may infringe on U.S. Patent No. 4,197,590 and Re. 31,200 etc. held by CADTRAK Corporation of the United States, and the corresponding patents in various countries. Problems may arise from such patents even when a different graphics display controller or discrete circuitry is used, and thus resolution on the basis of this product alone is not possible. Therefore, the user is requested to undertake as his or her own responsibility an investigation of measures to cope with this situation before designing an application system.

Ordering Information

Part No.	Package
μPD72020C-8	40-pin plastic DIP
μPD72020GC-8-3B6	52-pin plastic miniflat

Pin Configurations

40-Pin Plastic DIP



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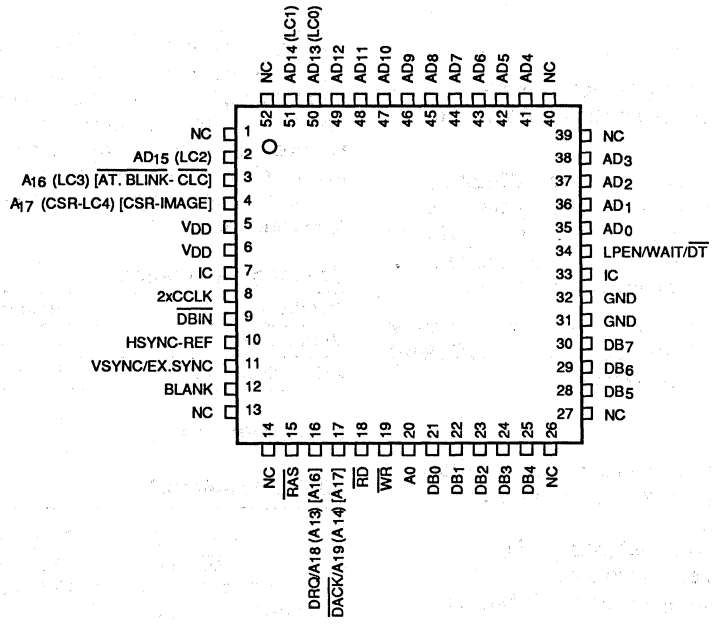
52-Pin Plastic Miniflat



Pin Identification

Symbol	Function
A0	Address select input for microprocessor interface
AD_0-AD_{12}	Address-data lines to display memory
AD_{13}/LC0, AD_{14}/LC1, AD_{15}/LC2	See text and table 3.
A_{16}/LC3/AT.BLINK-CLC, A_{17}/CSR-LC4/CSR-IMAGE	See text and table 3.
BLANK	CRT blanking output
$\overline{DACK}/A_{19}/A_{14}/A_{17}$	See text and table 1.
DB_0-DB_7	Bidirectional data bus to host microprocessor
$\overline{DBIN}$	Display memory read input flag
$DRQ/A_{18}/A_{13}/A_{16}$	See text and table 1.
HSYNC-REF	Horizontal video sync output

Symbol	Function
LPEN/WAIT/$\overline{DT}$	See text and table 2.
$\overline{RAS}$	Row address strobe
$\overline{RD}$	Read strobe input for microprocessor interface
VSYNC/EX.SYNC	Vertical video sync output or external VSYNC input
$\overline{WR}$	Write strobe input for microprocessor interface
2xCCLK	Clock input
GND	Ground
V_{DD}	+5-volt power supply
IC	Internal connection
NC	No connection

PIN FUNCTIONS

Pins on the μPD7220A and the μPD72020 have similar functions. Differences are described below.

Pins DRQ and $\overline{DACK}$

The functions of these pins depend on the setting of the PN bit by the WMASK command, which validates the address extension functions See table 1.

A_{13}, A_{14}, A_{16}-A_{19}. When the address extension function is selected by setting PN of the WMASK command, the upper 2 bits (of the extended address) are output in the video memory in each display/draw mode.

After the address extension function has been selected, the DMA-related functions cannot be used. Use the CHR and G bits of the SYNC command to set the display/draw mode (as with the μPD7220A).

DRQ (DMA Request). When the DMAR or DMAW command is executed, the DMA request signal is output. This signal is input to the DRQ pin of the DMA controller.

After the DMA-related functions have been selected, the address extension functions cannot be used.

$\overline{DACK}$ (DMA Acknowledge). A signal indicating DMA transfer is input. This signal is output from the $\overline{DACK}$ pin of the DMA controller.

Pin LPEN/WAIT/$\overline{DT}$

The functions of this pin depend on the setting of the DTE bit by the WMASK command, which validates the DT signal generation function. See table 2.

$\overline{DT}$ (Data Transfer). When the $\overline{DT}$ signal generation function is selected by setting DTE of the WMASK command, the $\overline{DT}$ signal is output to indicate the display address supply timings for the μPD41264-type video RAMs (VRAMs).

After the $\overline{DT}$ signal generation function has been selected, the LPEN and WAIT functions cannot be used.

LPEN (Light Pen Strobe). When the light pen detects a light input, the H-level signal is input.

After the LPEN function has been selected, the $\overline{DT}$ signal generation function cannot be used.

WAIT (Drawing Wait). When a signal that remains at the H-level for a period of at least four clocks is input in the drawing stop mode, the μPD72020 will stop drawing temporarily if it is executing drawing and output a display address.

After the WAIT function has been selected, the $\overline{DT}$ signal generation function cannot be used.

Pins AD_{13}-AD_{15}, A_{16}, and A_{17}

The functions of some other pins depend on the operating mode: character, graphics, or character/graphics combined. See table 3.

Table 1. Pin Functions Available Through Address Extension

Pin Symbol	PN Bit (WMASK Command)	Action	Mode	I/O	Pin Function
DRQ/A_{18}/A_{13}/A_{16}	0	Action similar to μPD7220A		Output	DRQ
	1	Address extension	Graphics	Output	A_{18}
			Character	Output	A_{13}
			Combined	Output	A_{16}
$\overline{DACK}$/A_{19}/A_{14}/A_{17}	0	Action similar to μPD7220A		Input	$\overline{DACK}$
	1	Address extension	Graphics	Output	A_{19}
			Character	Output	A_{14}
			Combined	Output	A_{17}

Table 2. Pin Functions Available Through $\overline{DT}$ Signal Generation

Pin Symbol	DTE Bit (WMASK Command)	Action	I/O	Pin Function
LPEN/WAIT/ $\overline{DT}$	0	Action similar to μPD7220A	Input	LPEN/WAIT
	1	$\overline{DT}$ signal generation	Output	$\overline{DT}$

Table 3. Multifunction Pins AD_{13}-AD_{15}, A_{16}, and A_{17}

Pin Symbol	Mode	I/O	Function
AD_{13}-AD_{15}	Graphics; combined	I/O	Address-data lines 13-15 to display memory
LC0-LC2	Character	Output	Line counter bits 0-2
A_{16}	Graphics	Output	Address bit 16
LC3	Character	Output	Line counter bit 3
$\overline{AT.BLINK\text{-}CLC}$	Combined	Output	Attribute blink and clear line counter
A_{17}	Graphics	Output	Address bit 17
CSR-LC4	Character	Output	Cursor and line counter bit 4
CSR-IMAGE	Combined	Output	Cursor and bit-map area flag

ADDED BLOCK FUNCTIONS

Refer to the μPD72020 Block Diagram and the System Configuration Diagram.

Video RAM Control

Additional blocks generate the $\overline{DT}$ signal, which indicates the display-address supply timings for the video RAMs. Data within the RAMs can be transferred to the serial register.

Pin Extension Control

The video memory address is extended 2 bits (with the address space extended fourfold) in each of the character, character/graphics combined, and graphics modes.

These bits are used for both $\overline{DACK}$ pin and DRQ pin in each mode: A_{14} and A_{13}; A_{17} and A_{16}; A_{19} and A_{18}.

WMASK Register

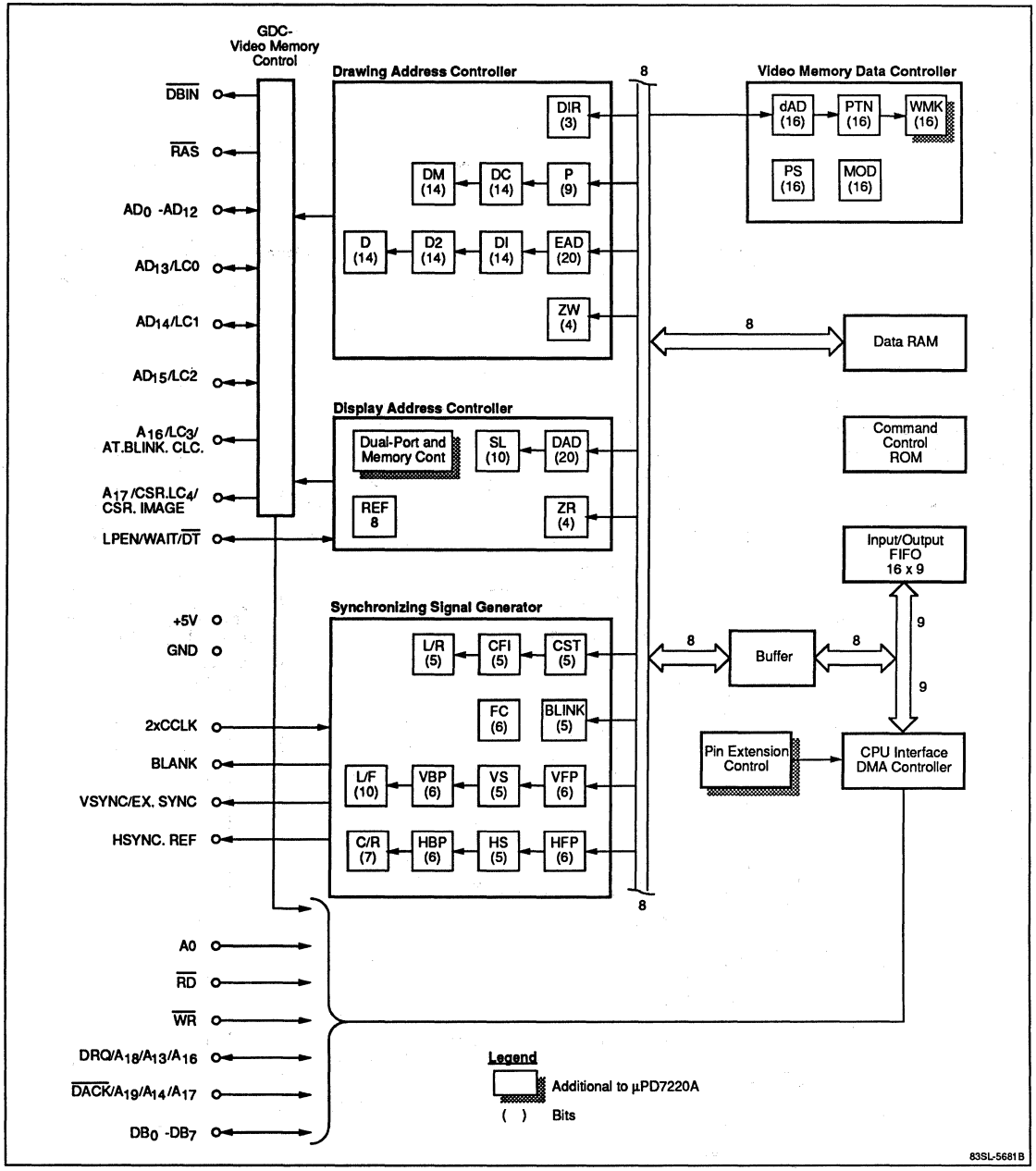
This 16-bit register is used to mask the data for multicolor synchronous drawing with one word in 8/4/2/1-bit configuration.

IMPROVED FUNCTIONS

The μPD72020 functions have been improved while maintaining compatibility with the μPD7220A in both hardware and software. Table 4 compares functions of the μPD72020 and the μPD7220A.

The μPD72020 is initialized by reset input so that it can function similarly to the μPD7220A.

μPD72020 Block Diagram



System Configuration Diagram; μPD72020 With Video RAM Control Signal $\overline{DT}$

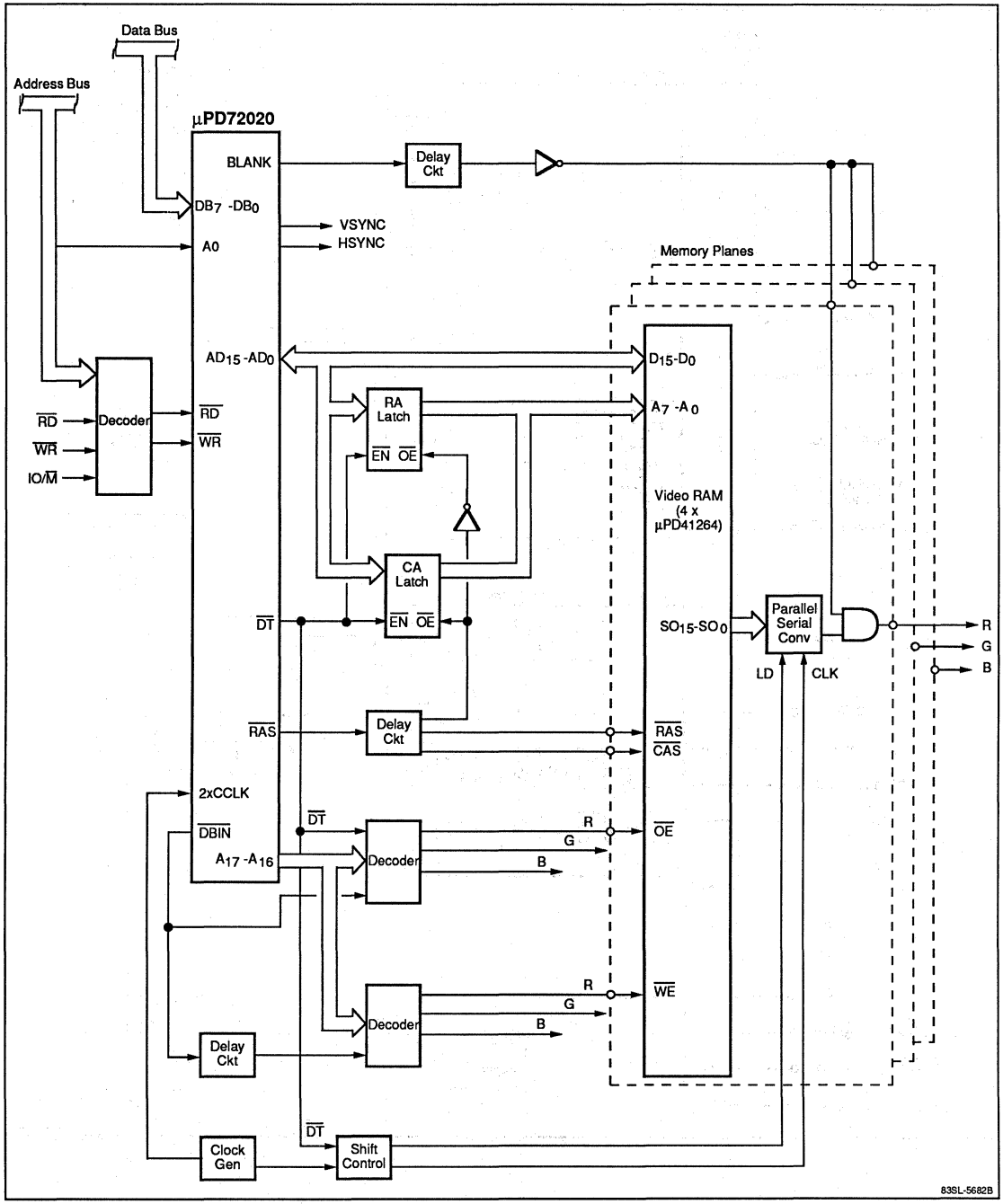


Table 4. Comparison of μPD72020 and μPD7220A Functions

μPD72020	μPD7220A
WMASK Command	
WMASK command is used to validate the new functions of the μPD72020.	WMASK command is not used.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	1	1	0	1	0
P1	WMKL							
P2	WMKH							
P3	PN	TM	DTE	CY1	CY0	0	0	0

WMK Sets the WMASK register value.

PN Sets the address extension function.

TM Changes the initializing timing of the horizontal synchronization counter in the slave mode for external synchronization, and sets the initializing function of the field counter.

DTE Sets the function of generating the $\overline{DT}$ signal.

CY Set the $\overline{DT}$ signal output mode and the BLANK signal mask.

LPEN Command	
Light pen address (LAD) is extended 2 bits by setting PN of the WMASK command.	Light pen address (LAD) extension function is not available.

PN 0 Same as μPD7220A

1 EAD is extended 2 bits.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	0	0	0	0	0	0
D1	LADL							
D2	LADM							
D3	X	X	X	X	LADH			

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	0	0	0	0	0	0
D1	LADL							
D2	LADH							
D3	X	X	X	X	X	X	LADH	

CSRW Command	
Draw execution address (EAD) is extended 2 bits by setting PN of the WMASK command.	Draw execution address (EAD) extension function is not available.

PN 0 Same as μPD7220A

1 EAD is extended 2 bits.

Character Mode

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	0	EADH						

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	0	0	0	EADH				

Table 4. Comparison of μPD72020 and μPD7220A Functions (cont)

μPD72020	μPD7220A

CSRW Command (cont)

Character/Graphics Combined Mode (Character Display)

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADM							
P3	0	0	0	0	0	0	EADH	

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADH							

Character/Graphics Combined Mode (Graphics Display/Drawing)

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADM							
P3	dAD				0	0	EADH	
P4	WG	0	0	0	0	0	0	0

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADH							
P3	dAD				WG	0	0	0

Graphics Mode

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADM							
P3	dAD				EADH			
P4	WG	0	0	0	0	0	0	0

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	0	1	0	0	1
P1	EADL							
P2	EADM							
P3	dAD				WG	0	EADH	

CSRR Command

Draw execution address (EAD) is extended 2 bits by setting PN of the WMASK command.

PN 0 Same as μPD7220A

1 EAD is extended 2 bits.

Draw execution address (EAD) extension function is not available.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	1	0	0	0	0	0
D1	EADL							
D2	EADM							
D3	X	X	X	X	EADH			
D4	dADL							
D5	dADH							

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	1	0	0	0	0	0
D1	EADL							
D2	EADM							
D3	X	X	X	X	X	X	EADH	
D4	dADL							
D5	dADH							

Table 4. Comparison of μPD72020 and μPD7220A Functions (cont)

μPD72020	μPD7220A
SCROLL Command	
Display start address (SAD) is extended 2 bits by setting PN of the WMASK command. PN 0 Same as μPD7220A 1 SAD is extended 2 bits.	Display start address (SAD) extension function is not available.

Character Mode

Built-In RAM Map

	MSB						LSB
RA	Contents or RAM						
0	SAD1L						
1	0	SAD1H					
2	SL1L			0	0	0	0
3	*	0	SL1H				
4	SAD2L						
5	0	SAD2H					
6	SL2L			0	0	0	0
7	*	0	SL2H				
8	SAD3L						
9	0	SAD3H					
A	SL3L			0	0	0	0
B	*	0	SL3H				
C	SAD4L						
D	0	SAD4H					
E	SL4L			0	0	0	0
F	*	0	SL4H				

* DAD+2

	MSB						LSB
RA	Contents or RAM						
0	SAD1L						
1	0	0	0	SAD1H			
2	SL1L			0	0	0	0
3	*	0	SL1H				
4	SAD2L						
5	0	0	0	SAD2H			
6	SL2L			0	0	0	0
7	*	0	SL2H				
8	SAD3L						
9	0	0	0	SAD3H			
A	SL3L			0	0	0	0
B	*	0	SL3H				
C	SAD4L						
D	0	0	0	SAD4H			
E	SL4L			0	0	0	0
F	*	0	SL4H				

* DAD+2

Table 4. Comparison of μPD72020 and μPD7220A Functions (cont)

μPD72020	μPD7220A
SCROLL Command (cont)	

Character/Graphics Combined Mode (Character Display)

Built-In RAM Map

	MSB							LSB
RA	Contents of RAM							
0	SAD1L							
1	SAD1M							
2	SL1L					0	0	SAD1H
3	*	0	SL1H					
4	SAD2L							
5	SAD2M							
6	SL2L					0	0	SAD2H
7	*	0	SL2H					
8	SAD3L							
9	SAD3M							
A	SL3L					0	0	SAD3H
B	*	0	SL3H					
C	SAD4L							
D	SAD4M							
E	SL4L					0	0	SAD4H
F	*	0	SL4H					

* DAD+2

	MSB							LSB
RA	Contents of RAM							
0	SAD1L							
1	SAD1H							
2	SL1L					0	0	0	0
3	*	0	SL1H					
4	SAD2L							
5	SAD2H							
6	SL2L					0	0	0	0
7	*	0	SL2H					
8	SAD3L							
9	SAD3H							
A	SL3L					0	0	0	0
B	*	0	SL3H					
C	SAD4L							
D	SAD4H							
E	SL4L					0	0	0	0
F	*	0	SL4H					

* DAD+2

Character/Graphics Combined Mode (Graphics Display/Drawing)

Built-In RAM Map

	MSB							LSB
RA	Contents of RAM							
0	SAD1L							
1	SAD1M							
2	SL1L					0	0	SAD1H
3	*	IM	SL1H					
4	SAD2L							
5	SAD2M							
6	SL2L					0	0	SAD2H
7	*	IM	SL2H					

* DAD+2

	MSB							LSB
RA	Contents of RAM							
0	SAD1L							
1	SAD1H							
2	SL1L					0	0	0	0
3	*	IM	SL1H					
4	SAD2L							
5	SAD2H							
6	SL2L					0	0	0	0
7	*	IM	SL2H					

* DAD+2

Table 4. Comparison of μPD72020 and μPD7220A Functions (cont)

μPD72020	μPD7220A
Scroll Command (cont)	

Graphics Mode

Built-In RAM Map

	MSB							LSB
RA	Contents or RAM							
0	SAD1L							
1	SAD1M							
2	SL1L						SAD1H	
3	*	IM	SL1H					
4	SAD2L							
5	SAD2M							
6	SL2L						SAD2H	
7	*	IM	SL2H					

* DAD+2

	MSB							LSB
RA	Contents or RAM							
0	SAD1L							
1	SAD1M							
2	SL1L						0	0	SAD1H
3	*	IM	SL1H					
4	SAD2L							
5	SAD2M							
6	SL2L						0	0	SAD2H
7	*	IM	SL2H					

* DAD+2

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COMMANDS

The μPD72020 supports all commands of the μPD7220A. Although command names are different, opcodes are the same. The μPD72020 can activate the software created for use with the μPD7220A.

The improved functions of the μPD72020 can be used by setting the new WMASK command. Once the RESET command is input, however, the WMASK command becomes inactive and the μPD72020 maintains the same functions as those of the μPD7220A.

This section describes the WMASK command as well as the SCROLL, LPEN, CSRW, and CSRR commands, which are affected by the setting of the WMASK command.

WMASK Command

This new command (figure 1) controls four new functions.

- WMASK register setting
- Address extension
- Selection of additional functions in the external slave mode
- $\overline{DT}$ signal generation

Figure 1. WMASK Command Format

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	0	1	1	0	1	0
P1	WMKL							
P2	WMKH							
P3	PN	TM	DTE	CY1	CY0	0	0	0

WMK Bit. The μPD72020 is equipped with the conventional MASK register and a 16-bit WMASK register. The WMK bit is used to set this WMASK register.

The 16-bit WMASK register is used for write mask of the multicolor, simultaneously-drawn data with one word set in 8-, 4-, 2- and 1-bit formats. Each bit of the WMASK register corresponds to each bit of the drawn data.

(1) When a WMASK register bit is set to 0 by the WMK, the drawn data bit corresponding to the WMASK register bit set to 0 is not affected by drawing.

(2) When a WMASK register bit is set to 1 by the WMK, operation is similar to the μPD7220A. Thus, the drawn data bit corresponding to the WMASK register bit set to 1 is affected by drawing.

When the RESET command is input, the μPD72020 is set to this mode.

PN Bit. PN is used to set the address extension function for the video memory.

(1) When PN = 0, operation is similar to the μPD7220A. Thus, the address extension function cannot be used.

When the RESET command is input, the μPD72020 is set to this mode.

(2) When PN = 1, the video memory address is extended 2 bits (with the address space expanded fourfold).

The DRQ/A_{18}/A_{13}/A_{16} pin and the $\overline{DACK}$/A_{19}/A_{14}/A_{17} pin output the upper 2 bits of the extended address. The DMA-related functions cannot be used.

The address to be output depends on the display and drawing modes. See table 1. The address space is shown in table 5.

Table 5. Address Space With Extended Address

	Character Mode	Character/Graphics Combined Mode	Graphics Mode
Address space	15 bits (32K words)	18 bits (256K words)	20 bits (1M words)

As the address space is expanded, the following command bits are also extended.

- LAD bit of LPEN command
- EAD bit of CSRW command
- EAD bit of CSRR command
- SAD bit of SCROLL command

Refer to the description of each command for details.

TM Bit. TM has been added to solve the following two problems with the μPD7220A.

- Because the vertical and horizontal counters are initialized at the start of VFP and HFP, respectively, when the external synchronizing signal is input to the μPD7220A, horizontal positioning cannot be readily done for synchronization with the μPD7220A by inputting a synchronizing signal from the external device.

- When the μPD7220A is operated in the interlace mode, input of the external synchronizing signal causes no effect on the field counter. Thus, if the synchronizing signal is unconditionally input from the external device when the μPD7220A is in the second field, the second and first fields are reversed in subsequent frames and the fields do not conform with the external device.

When the μPD72020 operates in the slave mode for external synchronization, the setting of the TM bit will cause the μPD72020 to operate differently from the μPD7220A in the following operations.

- The timing of initializing the horizontal synchronous counter is changed.
- The initializing function of the field counter is validated.

When TM = 0, the function similar to the external synchronizing function of the μPD7220A is carried out. When the RESET command is input, the μPD72020 is set to this mode.

When TM = 1, the following two operations differ from those of the μPD7220A.

(1) When the RESET command is executed or the EX.SYNC (external synchronizing signal) is input, the horizontal counter is reset at the rising edge of the HS. See figure 2.

(2) When the RESET command is executed in the interlace mode or the EX.SYNC signal is input, the field counter is unconditionally reset to the first field mode.

Thus, the VSYNC signal in the second field should be removed externally so that the synchronizing signal applied to the EX.SYNC pin serves as the VSYNC signal in the first field (in the interlace mode).

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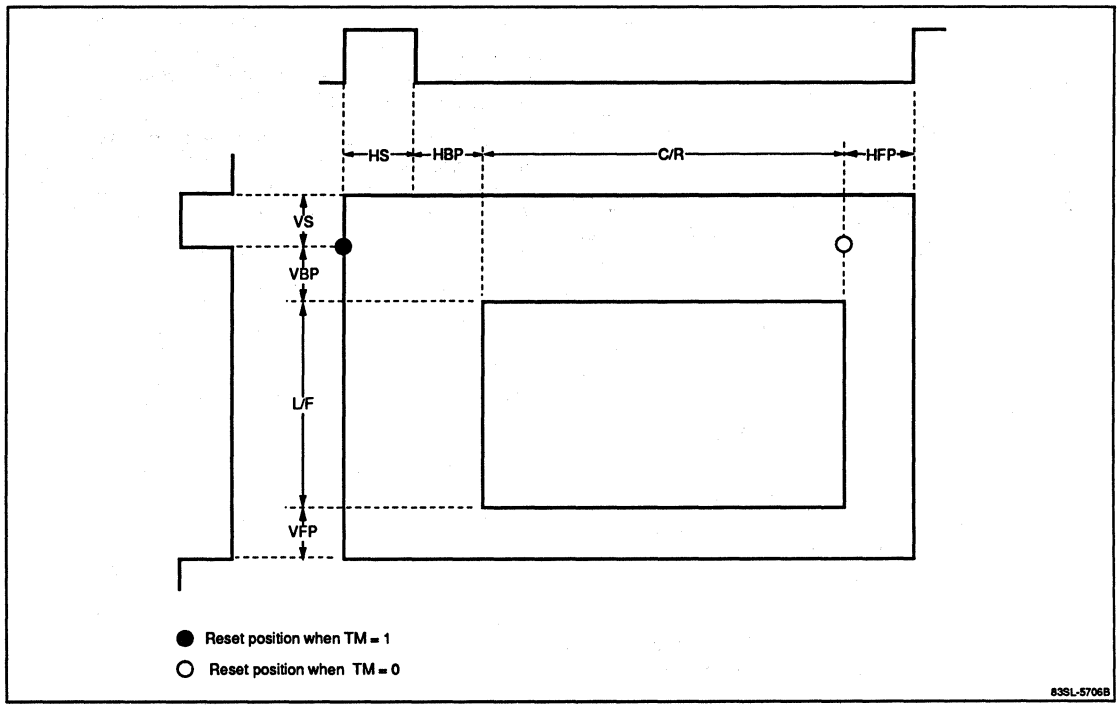
Figure 2. Horizontal Counter Reset Timing



DTE, CY1, CY0 Bits. To prevent the display screen from becoming blurred during drawing operations, the μPD7220A normally performed drawing in the flashless drawing mode. Thus, the drawing period was limited and it was difficult to improve the drawing efficiency.

To solve this problem, video RAMs can be used for the μPD72020. Through the use of VRAMs, both drawing and display can be carried out simultaneously in the flashless drawing mode with the result that the drawing efficiency can be improved. DTE, CY1, and CY0 are used to control the μPD41264-type VRAMs and the BLANK signal.

Table 6. $\overline{DT}$ Signal Output Modes

DTE	CY1	CY0	Function
0	0	0	GDC mode 0
0	0	1	GDC mode 1 (BLANK signal mask †)
0	1	0	Inhibited
0	1	1	Inhibited
1	0	0	$\overline{DT}$ signal output mode 0 (BLANK signal mask †)
1	0	1	Inhibited
1	1	0	$\overline{DT}$ signal output mode 1 (BLANK signal mask †)
1	1	1	$\overline{DT}$ signal output mode 2 (BLANK signal mask †)

† If the μPD72020 has started drawing operations in the display mode, the BLANK signal is not set to H.

DTE = 0. Operation is similar to the μPD7220A. The $\overline{DT}$ signal functions cannot be used. The LPEN/WAIT/$\overline{DT}$ pin performs the LPEN or WAIT functions.

The following two modes are available by setting CY1 or CY0 (table 6).

(1) GDC mode 0 operation is similar to the μPD7220A. When the RESET command is input, the μPD72020 is set to this mode.

(2) GDC mode 1 operation is similar to GDC mode 0 except if the μPD72020 starts drawing operations during the display period, the BLANK signal is not set to H even in the flash screen mode.

DTE = 1. The $\overline{DT}$ signal functions are enabled and the $\overline{DT}$ signal is output from the LPEN/WAIT/$\overline{DT}$ pin. The $\overline{DT}$ signal is used for display timing when the display memory consists of dual-port video RAMs. The VRAMs allow drawing during both drawing and display cycles.

When DTE is set to 1, the μPD72020 internally tracks the display address and outputs it and the $\overline{DT}$ signal under either of two conditions.

(1) At the start of every horizontal scan line (figure 3).

(2) When the lower 8 bits of the display address (DAD) internal counter are 0.

The starting display address should be set before setting DTE to 1. The μPD72020 will temporarily stop a drawing operation before issuance of the $\overline{DT}$ signal, as in the case of the μPD7220A WAIT function.

The $\overline{DT}$ signal output timing depends on the setting of the IM and DAD+2 bits of the SCROLL command. CY0 and CY1 determine which of the following three $\overline{DT}$ signal output modes is used.

Mode 0 With DTE = 1. In mode 0, the $\overline{DT}$ signal is output as shown in figure 4.

(1) At the start of every horizontal scan line.

(2) When the lower 8 bits of the DAD counter change from FEH or FFH to 00H.

Additionally, the $\overline{DT}$ signal active state in mode 0 has the following qualifications.

(1) $\overline{DT}$ may become active in succession; for example, when the DAD counter changes to 00H just after the start of a horizontal scan line as in figure 4C.

(2) When the lower 8 bits of the DAD counter become 00H in succession, $\overline{DT}$ becomes active during the first cycle only. See figure 4D.

(3) $\overline{DT}$ will not become active during HFP, HS, HBP, VFP, VS, or VBP periods.

Mode 1 With DTE = 1. In mode 1, the $\overline{DT}$ signal is ouput as shown in figure 5A.

(1) At the start of every horizontal scan line.

(2) When the lower 8 bits of the DAD counter change from FEH or FFH to 00H.

Additionally, the $\overline{DT}$ signal active state in mode 1 has the following qualifications.

(1) $\overline{DT}$ may become active in succession.

(2) When the lower 8 bits of the DAD counter change to 00H in succession, $\overline{DT}$ is active only during the first cycle.

(3) $\overline{DT}$ can become active during HFP, HS, HBP, VFP, VS, or VBP periods.

(4) $\overline{DT}$ will not become active while the DMA refresh operation is disabled (D-bit of SYNC command set to 1).

(5) $\overline{DT}$ becomes active every four cycles.

Mode 2 With DTE = 1. In mode 2, the $\overline{DT}$ signal output is the same as described for mode 1 except $\overline{DT}$ is active every eight cycles instead of every four cycles. See figure 5B.

3

Figure 3. $\overline{DT}$ Signal Output for Each Horizontal Line

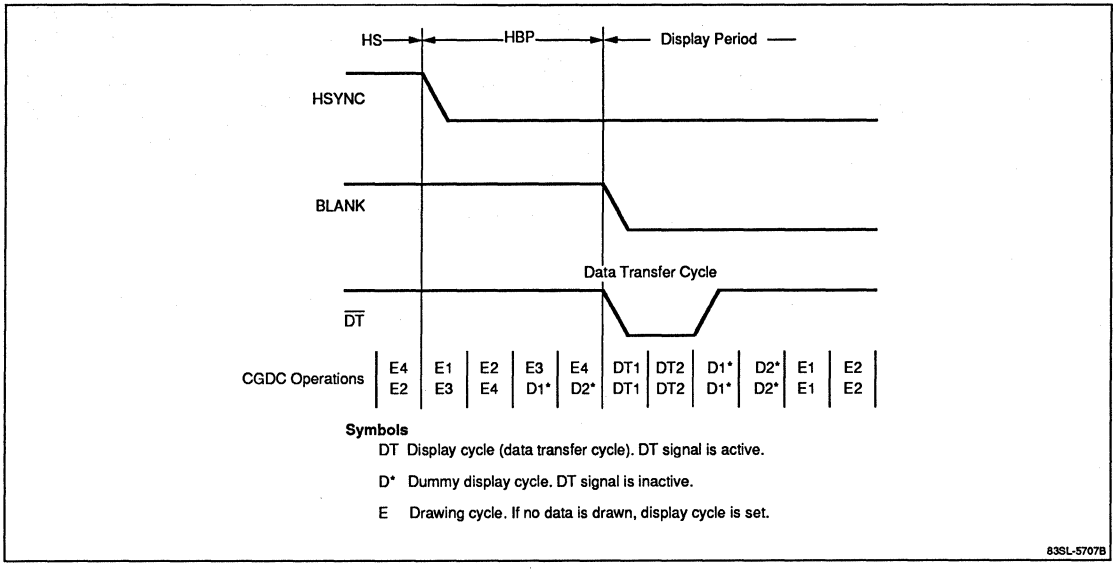
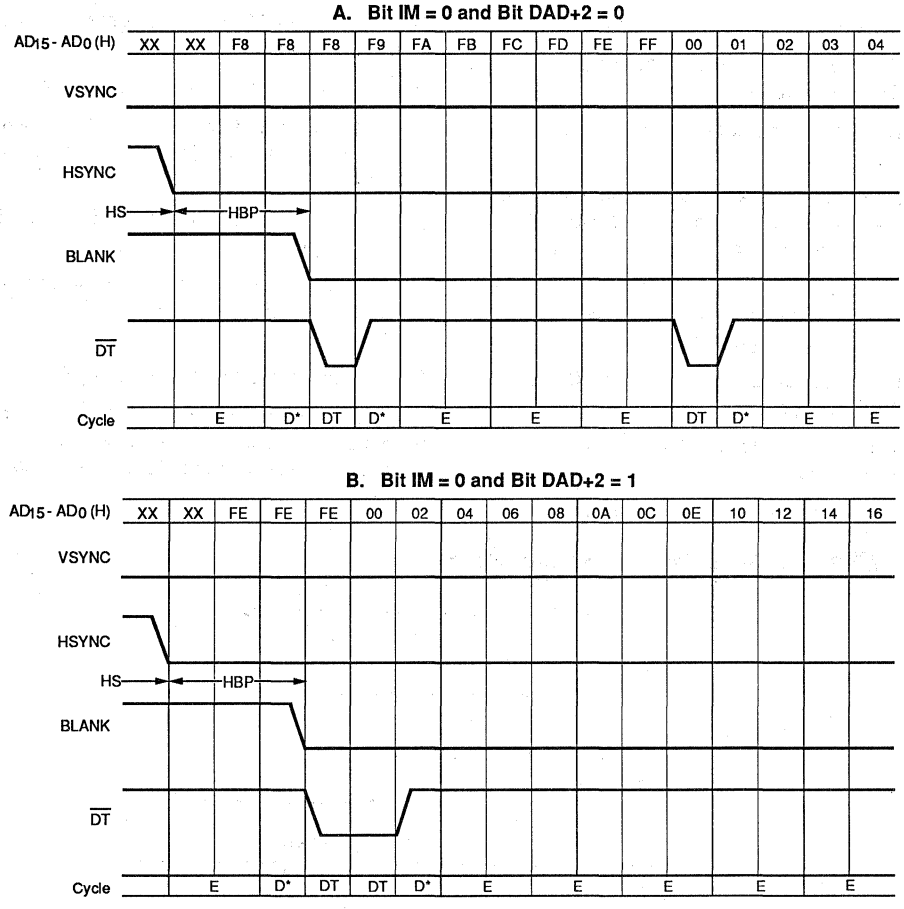


Figure 4. $\overline{DT}$ Signal Output, Mode 0 (Sheet 1 of 2)



Symbols

DT Display cycle (data transfer cycle). $\overline{DT}$ signal is active.

D* Dummy display cycle. $\overline{DT}$ signal is inactive.

E Drawing cycle. If no data is drawn, display cycle is set.

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Figure 4. $\overline{DT}$ Signal Output, Mode 0 (Sheet 2 of 2)

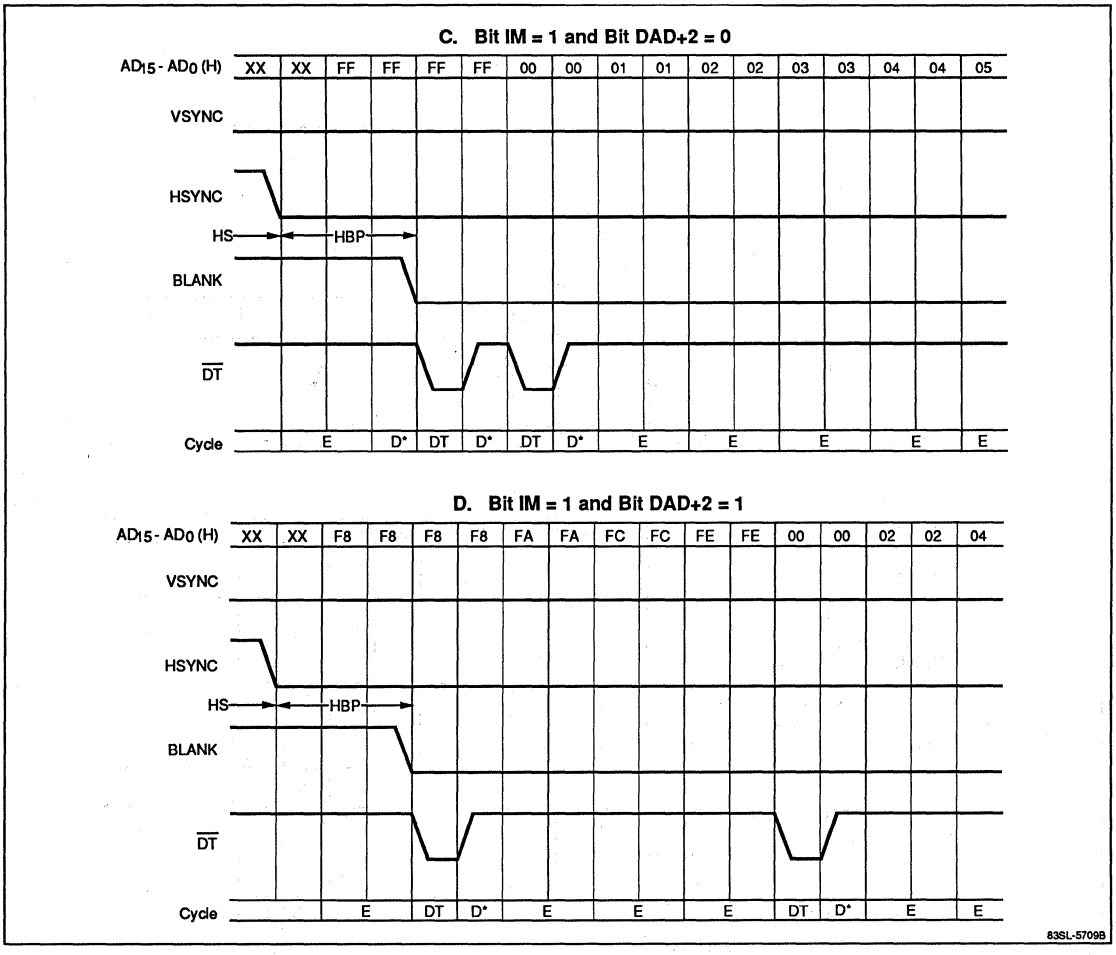
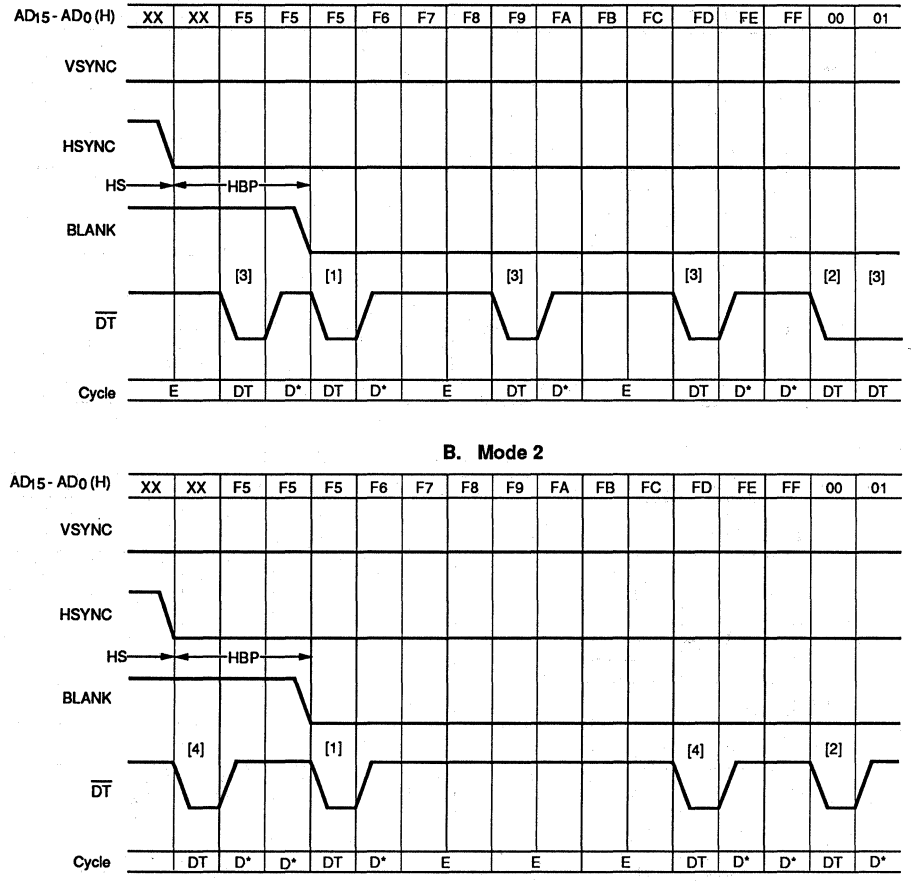


Figure 5. $\overline{DT}$ Signal Output, Mode 1 and Mode 2



Symbols

DT Display cycle (data transfer cycle). $\overline{DT}$ signal is active

D* Dummy display cycle. $\overline{DT}$ signal is inactive.

E Drawing cycle. If no data is drawn, display cycle is set.

[1] $\overline{DT}$ becomes active at display cycle start.

[2] $\overline{DT}$ becomes active when counting of the DAD lower 8 bits has terminated (FEH or FFH changes to 00H).

[3] $\overline{DT}$ becomes active every four cycles as controlled by counter that resets at diplay cycle start.

[4] $\overline{DT}$ becomes active every eight cycles.

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LPEN Command

When the address extension function is set by the WMASK command (with PN set to 1), the upper 2 bits of the light pen address (LAD) in the LPEN command are extended and a maximum of 20 bits can be used.

When PN = 0, the light pen address (LAD) is the same as with the μPD7220A.

The LPEN command format with the extended LAD is shown in figure 6.

Figure 6. LPEN Command Format

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	0	0	0	0	0	0
D1	LADL							
D2	LADM							
D3	X	X	X	X	LADH			

CSRW Command

When the address extension function is set by the WMASK command (with PN set to 1), the upper 2 bits of the drawing execution address (EAD) in the LPEN command are extended.

When PN = 0, the drawing execution address (EAD) is the same as with the μPD7220A.

Address extension causes the WG bits to be positioned differently in the character/graphics combined mode (character display/drawing) or the graphics mode.

The CSRW command formats are included in table 4.

CSRR Command

When the address extension function is set by the WMASK command (with PN set to 1), the upper 2 bits of the drawing execution address (EAD) in the LPEN command are extended and a maximum of 20 bits can be used.

When PN = 0, the drawing execution address (EAD) is the same as with the μPD7220A.

The CSRR command format with the extended EAD is shown in figure 7.

Figure 7. CSRR Command Format

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	1	1	1	0	0	0	0	0
D1	EADL							
D2	EADM							
D3	X	X	X	X	EADH			
D4	dADL							
D5	dADH							

SCROLL Command

When the address extension function is set by the WMASK command (with PN set to 1), the upper 2 bits of the display start address (SAD) in the SCROLL command are extended.

When PN = 0, the display start address (SAD) is the same as with the μPD7220A.

The SCROLL command format is shown in figure 8. The built-in RAM map with the extended SAD is included in table 4.

Figure 8. SCROLL Command Format

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CMD	0	1	1	1	RA			

3

Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.3 V
Output voltage, V_O	−0.5 to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL}	−0.5	0.8	V	Except 2xCCLK
		−0.5	0.6	V	2xCCLK
High-level input voltage	V_{IH}	2.2	V_{CC} + 0.5	V	Except 2xCCLK, $\overline{WR}$
		3.5	V_{CC} + 0.5	V	2xCCLK
		2.5	V_{CC} + 0.5	V	$\overline{WR}$
Low-level output voltage	V_{OL}		0.45	V	I_{OL} = 2.2 mA
High-level output voltage	V_{OH}	0.7 V_{DD}		V	I_{OH} = −400 μA
Low-level input leakage current	I_{LIL}		−10	μA	V_I = 0 V; except VSYNC, $\overline{DACK}$
			−500	μA	V_I = 0 V; VSYNC, $\overline{DACK}$
High-level input leakage current	I_{LIH}		10	μA	V_I = V_{DD}; except LPEN/WAIT/$\overline{DT}$
			500	μA	V_I = V_{DD}; LPEN/WAIT/$\overline{DT}$
Low-level output leakage current	I_{LOL}		−10	μA	V_O = 0 V
High-level output leakage current	I_{LOH}		10	μA	V_O = V_{DD}
Supply current	I_{CC}		70	mA	

Capacitance

T_A = +25°C; V_{DD} = GND = 0 V

Item	Symbol	Min	Max	Unit	Condition
Input	C_I		15	pF	f = 1 MHz; 0 V except for tested pin
Output	C_O		20	pF	
Input/output	$C_{I/O}$		20	pF	
Clock input	C_C		20	pF	

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Item	Symbol	Min	Max	Unit	Conditions
Clock 2xCCLK					
Clock cycle	t_{CY}	125	10,000	ns	
High-level clock width	t_{CH}	52		ns	
Low-level clock width	t_{CL}	52		ns	
Clock rise time	t_{CR}		15	ns	
Clock fall time	t_{CF}		15	ns	
Read Cycle					
Address setup time to $\overline{RD}$ ↓	t_{AR}	0		ns	
Address hold time from $\overline{RD}$ ↑	t_{RA}	0		ns	
$\overline{RD}$ pulse width	t_{RR1}	t_{RD1} +20		ns	
Data output delay time from $\overline{RD}$ ↓	t_{RD1}		55	ns	C_L = 50 pF
Data float delay time from $\overline{RD}$ ↑	t_{DF}	0	55	ns	
$\overline{RD}$ pulse cycle	t_{RCY}	4.5 t_{CY}		ns	DE = 0
		12 t_{CY}		ns	DE = 1
$\overline{RD}$ recovery time	t_{RV}	2 t_{CY}		ns	Also valid in DMA cycle
Write Cycle					
Address setup time to $\overline{WR}$ ↓	t_{AW}	0		ns	
Address hold time from $\overline{WR}$ ↑	t_{WA}	10		ns	
$\overline{WR}$ pulse width	t_{WW}	60		ns	
Data setup time to $\overline{WR}$ ↑	t_{DW}	45		ns	
Data hold time from $\overline{WR}$ ↑	t_{WD}	10		ns	
$\overline{WR}$ pulse cycle	t_{WCY}	4.5 t_{CY}		ns	
$\overline{WR}$ recovery time	t_{RV}	2 t_{CY}		ns	Also valid in DMA cycle
DMA Read Cycle					
$\overline{DACK}$ setup time to $\overline{RD}$ ↓	t_{AKR}	0		ns	
$\overline{DACK}$ hold time from $\overline{RD}$ ↑	t_{RAK}	0		ns	
$\overline{RD}$ pulse width	t_{RR2}	t_{RD2} +20		ns	
Data output delay time from $\overline{RD}$ ↓	t_{RD2}		2 t_{CY} +60	ns	C_L = 50 pF

AC Characteristics (cont)

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Item	Symbol	Min	Max	Unit	Conditions
DMA Read Cycle(cont)					
DREQ output delay time from 2xCCLK ↑	t_{CRQ}		75	ns	C_L = 50 pF
DREQ setup time to $\overline{DACK}$ ↓	t_{RQAK}	0		ns	
DREQ ↓ delay time from $\overline{DACK}$ ↓	t_{AKRQ}		1.5 t_{CY} + 80	ns	C_L = 50 pF
$\overline{DACK}$ pulse cycle	t_{AKCY}	4.5 t_{CY}		ns	See Note.
High-level $\overline{DACK}$ width	t_{AKH}	t_{CY}		ns	
Low-level $\overline{DACK}$ width	t_{AKL}	2.5 t_{CY}		ns	
DMA Write Cycle					
$\overline{DACK}$ setup time to $\overline{WR}$ ↓	t_{AKW}	0		ns	
$\overline{DACK}$ hold time from $\overline{WR}$ ↑	t_{WAK}	0		ns	
Read/Modify/Write Cycle					
Address/data delay time from 2xCCLK ↑	t_{CA}	15	80	ns	C_L = 50 pF
Address/data float delay time from 2xCCLK ↑	t_{CAF}	15	80	ns	C_L = 50 pF
Data setup time to 2xCCLK ↓	t_{DC}	0		ns	
Data hold time from 2xCCLK ↓	t_{CDF}	t_{CBI}		ns	
$\overline{DBIN}$ delay time from 2xCCLK ↓	t_{CBI}	15	60	ns	C_L = 50 pF
$\overline{RAS}$ ↑ delay time from 2xCCLK	t_{CRSH}	15	60	ns	C_L = 50 pF
$\overline{RAS}$ ↑ delay time from 2xCCLK ↓	t_{CRSL}	15	50	ns	C_L = 50 pF
High-level $\overline{RAS}$ width	t_{RSH}	1/3 t_{CY}		ns	
Low-level $\overline{RAS}$ width	t_{RSL}	1.5 t_{CY} − 30		ns	
Address setup time to $\overline{ARSL}$ ↓	t_{ARSL}	30		ns	
Display Cycle					
Output signal delay time from 2xCCLK ↑	t_{CO}		70	ns	C_L = 50 pF

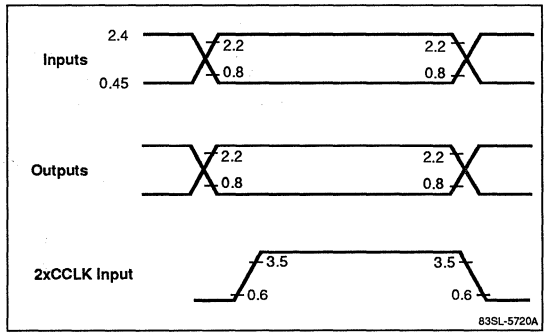
AC Characteristics (cont)

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Item	Symbol	Min	Max	Unit	Conditions
Input Cycle					
Input signal setup time to 2xCCLK ↑	t_{PC}	10		ns	
Input signal pulse width	t_{PP}	t_{CY}		ns	

Note: Performs two-dimensional rectangular area assignment whereby the dc parameter is set to other than 0. When byte-by-byte transfer is specified, the value is 5.5 t_{CY}.

Voltage Thresholds for Timing Measurements



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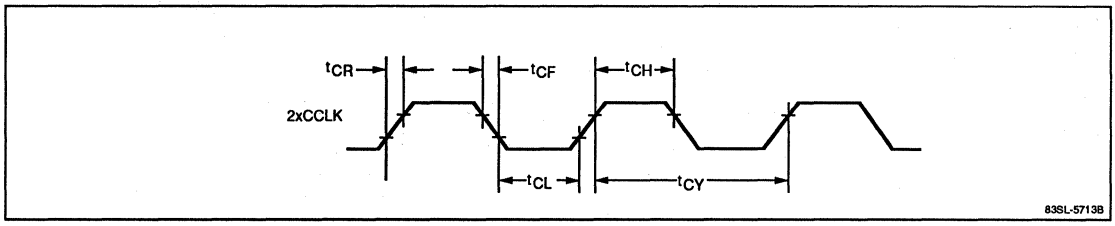
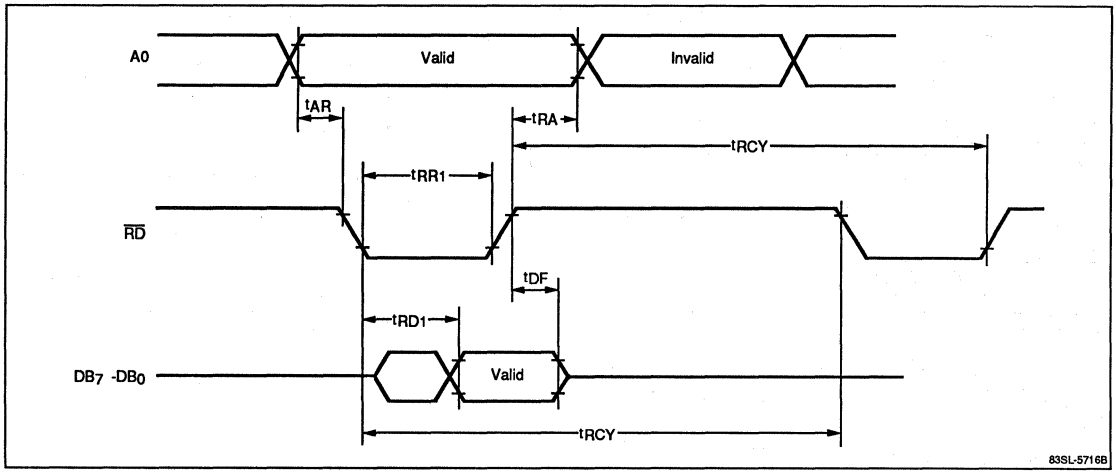
Timing Waveforms

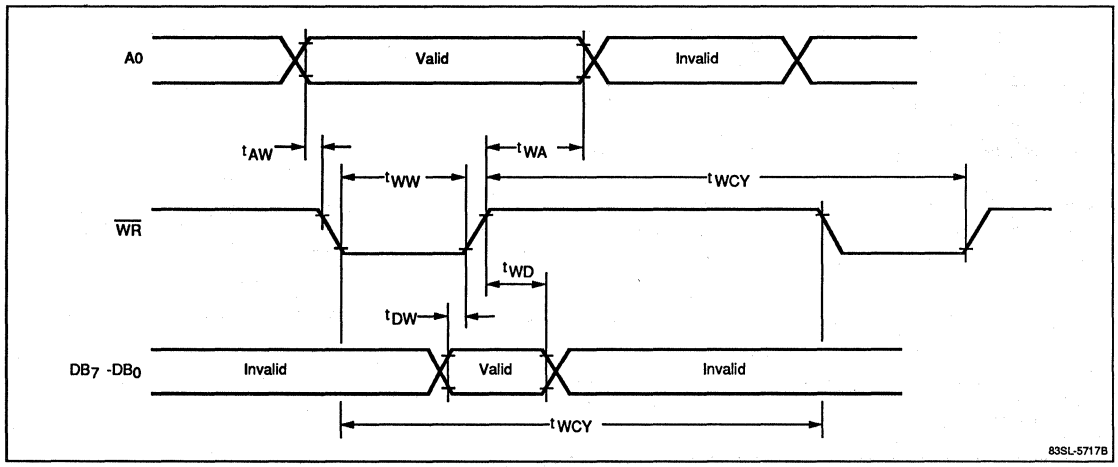
Clock 2xCCLK



Read Cycle

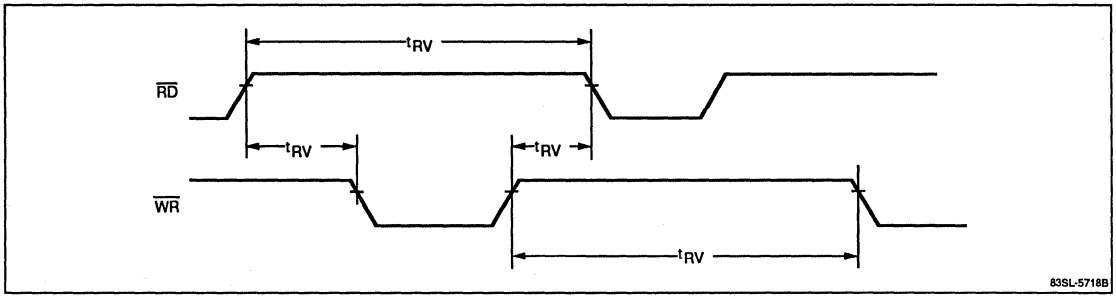


Write Cycle

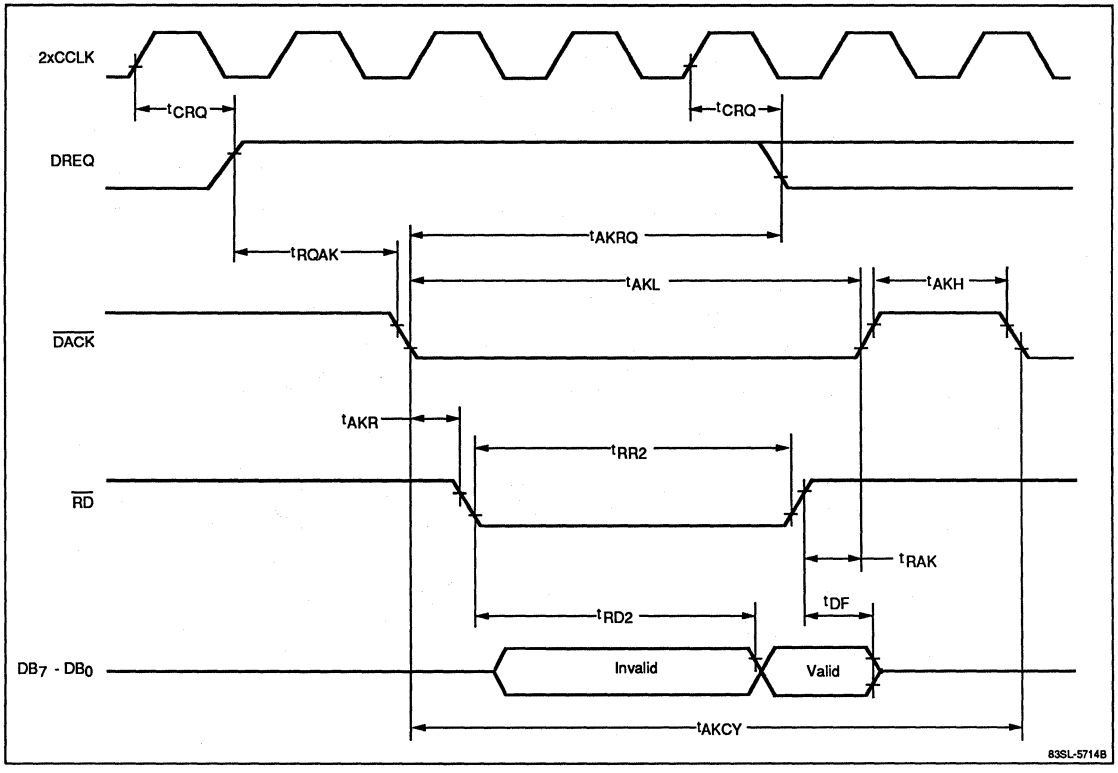


Timing Waveforms (cont)

Read/Write Recovery

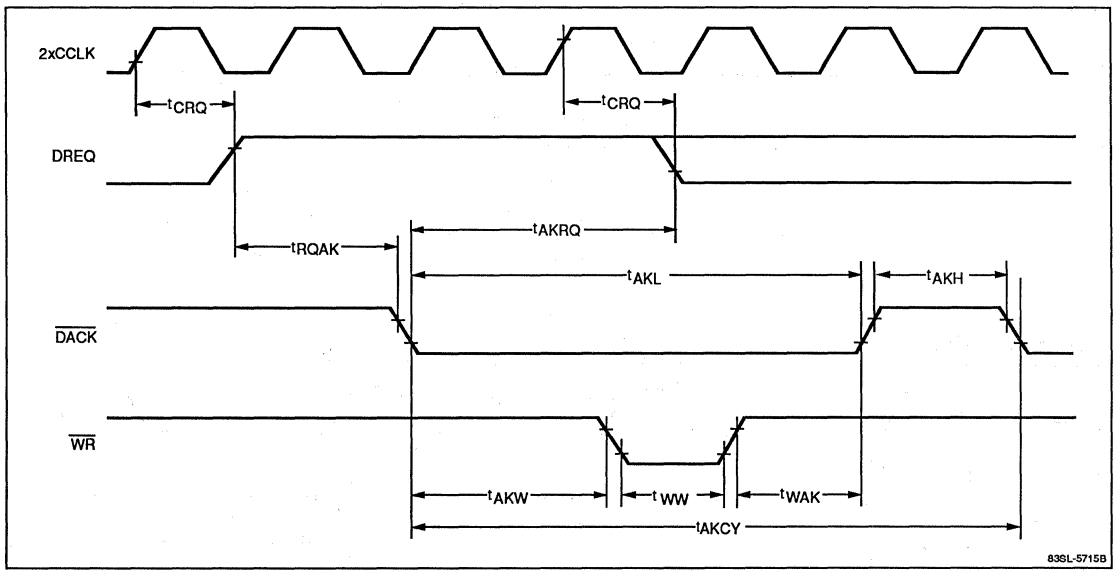


DMA Read Cycle

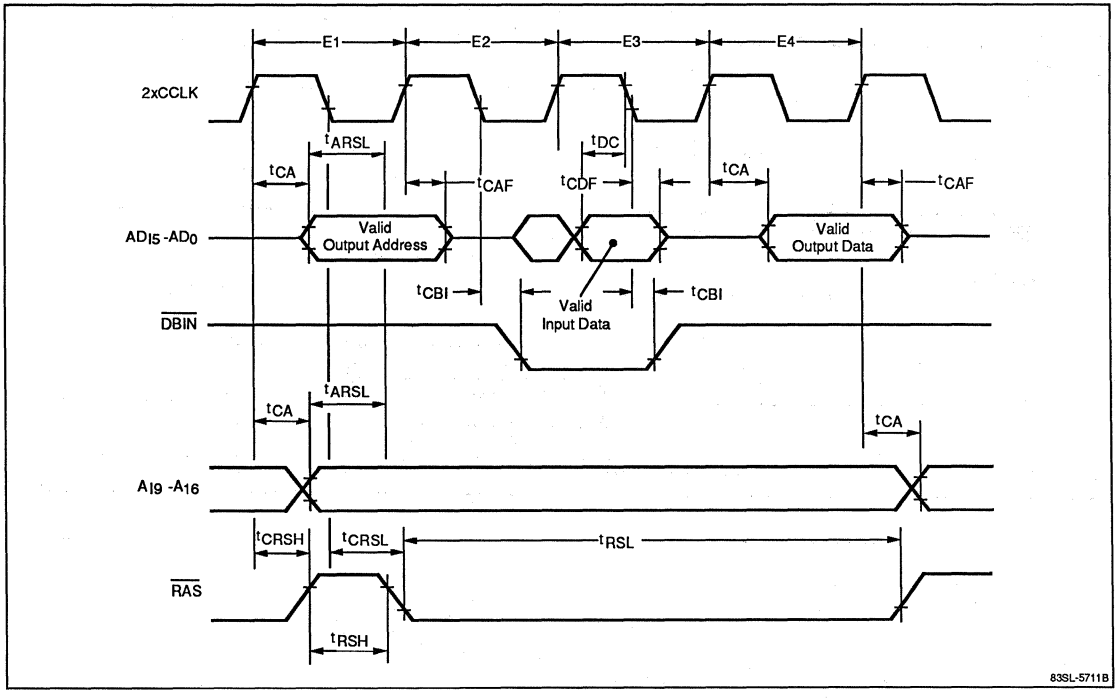


Timing Waveforms (cont)

DMA Write Cycle

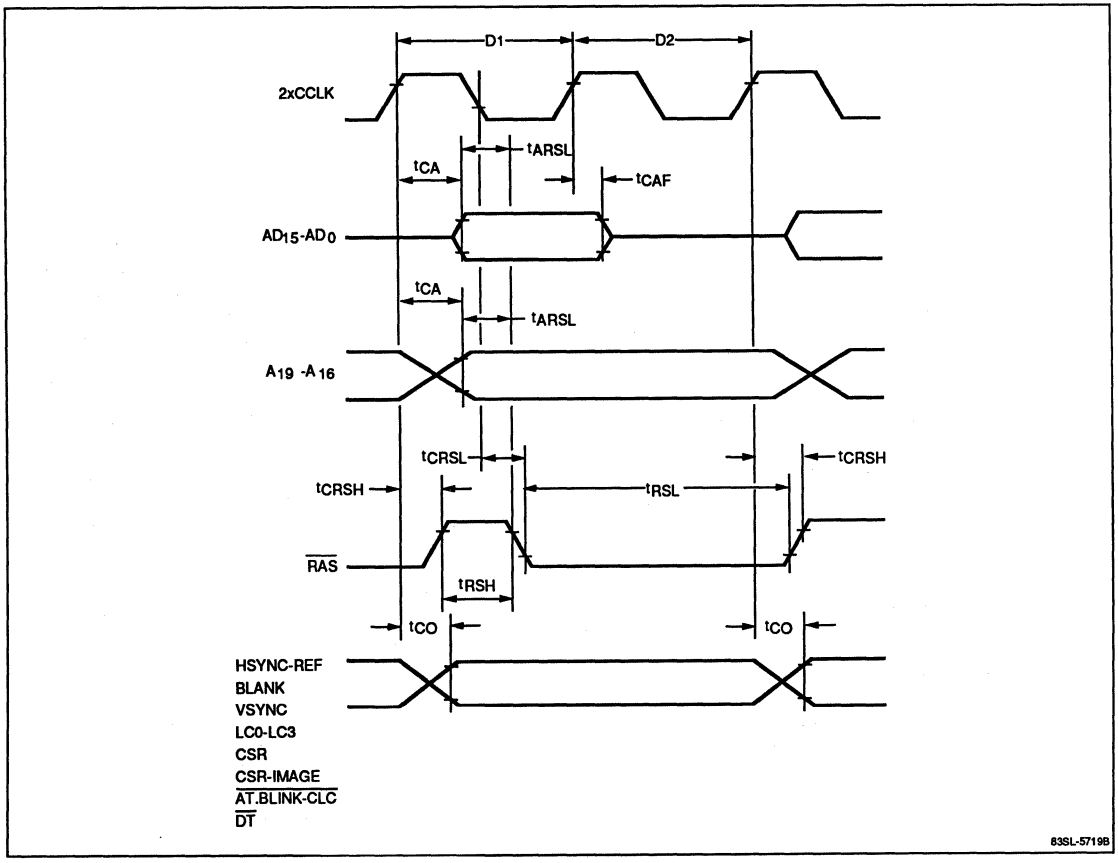


Read/Modify/Write Cycle

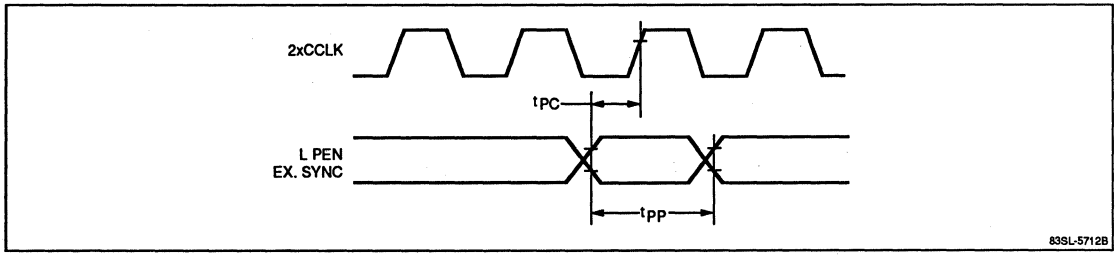


Timing Waveforms (cont)

Display Cycle



Input Cycle



μPD72022
Intelligent Display Processor

Description

The μPD72022 Intelligent Display Processor (IDP) performs CRT display control and image display data processing for text, static pictures, and sprites.

Features

- Three display modes: text, semigraphics, graphics
- Four-way horizontal split-screen display
- Smooth-scroll control (vertical, horizontal)
- Sprite image display
- 16-color display
- Attribute addition (7 max)
- Interlaced display through external synchronization
- Up to 256K x 16-bit word video memory addressing
- DRAM refresh
- Optional dual-port RAM
- Bus arbitration control
- CRT control signal programmable variables
  - Horizontal display time, retrace time (left and right), sync pulse width
  - Vertical display time, retrace time, sync pulse width
  - Rasters/line
  - Blinking time
- Variable display resolution
  - Horizontal: 640 dots max (22-MHz max dot rate)
  - Vertical: 512 dots max
  - Display signal (4 bits/dot) serial output
- Horizontal and vertical external synchronization
- 22 screen-control/drawing commands
- CMOS
- Single +5-volt power supply

Ordering Information

Part Number	Package
μPD72022GF-3B9	80-pin plastic miniflat
μPD72022L	68-pin PLCC

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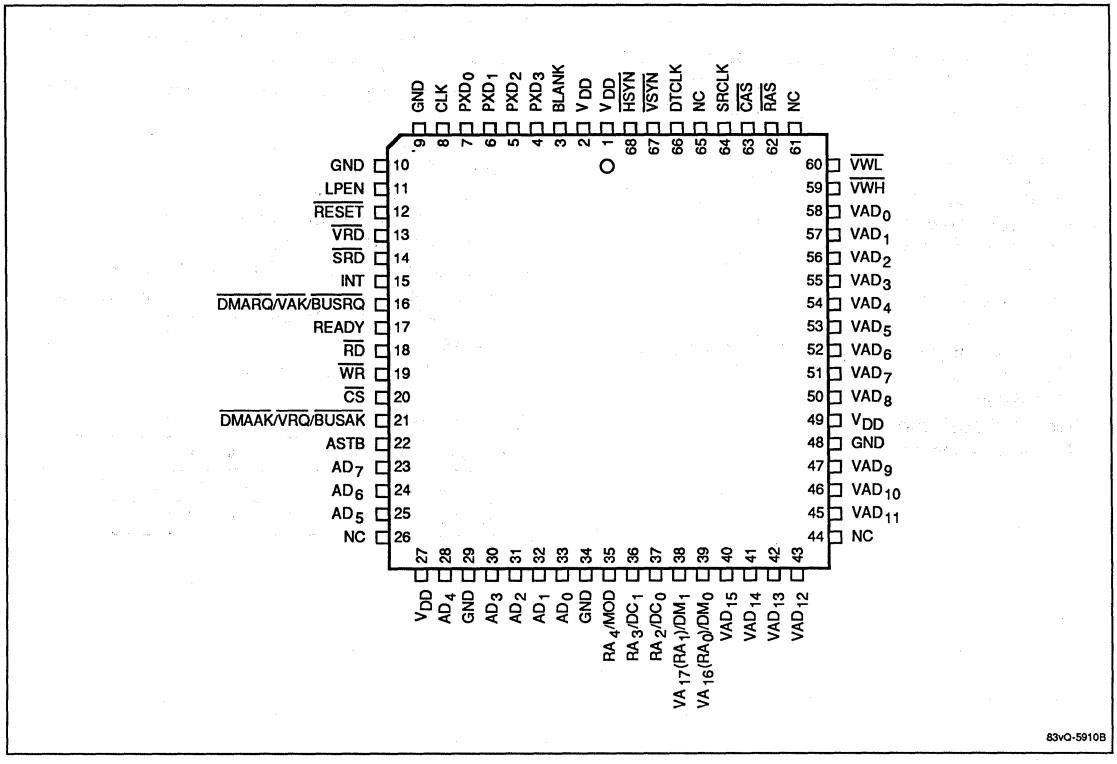
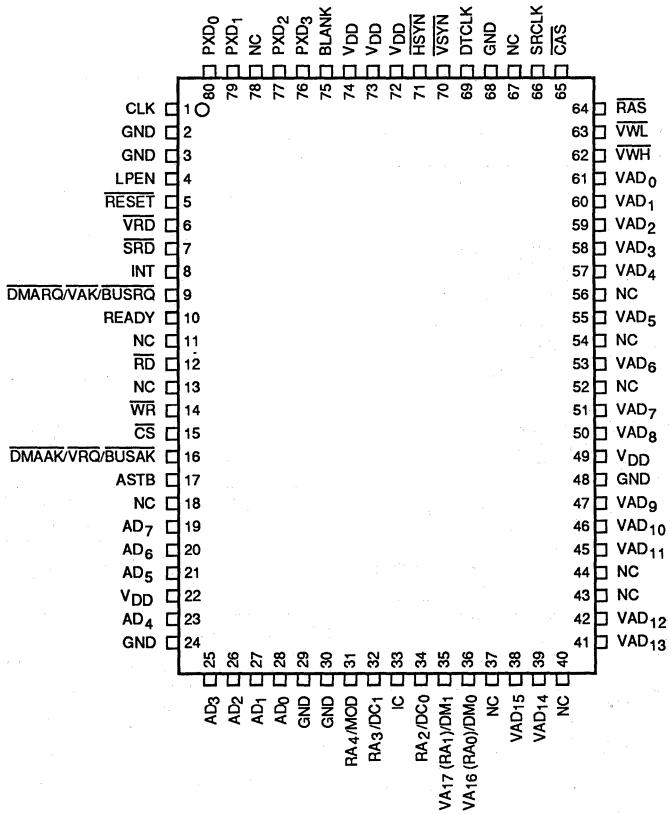
50071

Pin Configurations

68-Pin PLCC



80-Pin Plastic Miniflat



83vQ-5909B

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Pin Identification

Symbol	I/O	Signal Function
Host System Interface		
AD_0-AD_7	I/O	Three-state, bidirectional address/data bus. See table 1.
ASTB	In	Address Strobe. Read address information from AD_0-AD_7.
$\overline{BUSAK}$	In	Bus Acknowledge. While this signal is active, μPD72022 controls the system bus.
$\overline{BUSRQ}$	Out	Bus Request. Request for system bus control.
CLK	In	System clock.
$\overline{CS}$	In	Chip Select. Enables $\overline{RD}$ and $\overline{WR}$ signals.
$\overline{DMAAK}$	In	DMA Acknowledge. Enables DMA cycle.
$\overline{DMARQ}$	Out	DMA Request.
INT	Out	Interrupt request to host processor.
$\overline{RD}$	In	Control signal for reading data or status flag from μPD72022.
READY	Out	Indicates μPD72022 may be accessed for memory read/write cycle or I/O read/write cycle.
$\overline{RESET}$	In	Initializes μPD72022.
$\overline{VAK}$	Out	Video Memory Acknowledge. Indicates host processor has direct control of video memory.
$\overline{VRQ}$	In	Video Memory Request. Host processor requests direct control of video memory.
$\overline{WR}$	In	Control signal for writing data, commands, or parameters into μPD72022.
Video Memory Interface		
$\overline{CAS}$	Out	Column Address Strobe.
MOD	In	Mode change signal. See RA_4.
RA_0-RA_1	Out	Raster Address 0-1. RA_0 and RA_1 are also used for DM_0 and DM_1, respectively. See Display Data Control in this table.
RA_2-RA_3	Out	Raster Address 2-3. RA_2 and RA_3 are also used for DC_0 and DC_1, respectively. See Display Data Control in this table.
RA_4	Out	Raster Address 4. RA_4 is also used for MOD input.
$\overline{RAS}$	Out	Row Address Strobe.
SRCLK	Out	Serial Read Clock. Used with optional dual-port RAM.
$\overline{SRD}$	Out	Serial Read. Active while data is read from serial port with optional dual-port RAM.
VAD_0-VAD_{15}	I/O	Video Memory Address 0-15 output; DRAM refresh addresss output; data input/output.
VA_{16}-VA_{17}	Out	Video Memory Address 16-17. Also used for RA_0, RA_1

Symbol	I/O	Signal Function
$\overline{VRD}$	Out	Video Memory Read. Strobe signal to read data from video memory.
$\overline{VWH}$, $\overline{VWL}$	Out	Video Memory Write, High and Low. Strobe signals to write data into video memory.
CRT Interface		
BLANK	Out	Blanking display signal.
DTCLK	I/O	Dot Clock. During internal DTCLK mode, timing pulses derived by dividing CLK are output. During external DTCLK mode, the internal scanning subsystem derives a reference clock from the DTCLK input.
$\overline{HSYN}$	I/O	Horizontal Sync. Signal output when internal sync is specified; signal input when external sync is specifiifed.
LPEN	In	Light Pen Strobe. The DTCLK mode is specified by the LPEN level when the $\overline{RESET}$ signal level rises. LPEN — DTCLK Mode High — Internal DTCLK output Low — External DTCLK input
PXD_0-PXD_3	Out	Pixel Data 0-3. Display signal (four bits/dot) in sync with DTCLK.
$\overline{VSYN}$	I/O	Vertical Sync. Signal output when internal sync is specified; signal input when external sync is specified.
Display Data Control		
DC_0, DC_1	Out	Display Cycle. Specifies display processing cycle when μPD72022 is accessing video memory. DC_1 DC_0 Display Cycle 0 0 Other than indicated below 0 1 Static picture display cycle 1 0 Sprite display cycle 1 1 Screen start cycle See Video Memory Interface, RA_2 and RA_3.
DM_0, DM_1	Out	Display Mode. Specifies the static picture display mode. DM_1 DM_0 Display Mode 0 x Text mode 1 0 Semigraphics mode 1 1 Graphics mode See Video Memory Interface, RA_0 and RA_1.
Other Pins		
GND		Ground
V_{DD}		+5-volt power supply
NC		No Connection

μPD72022 Block Diagram

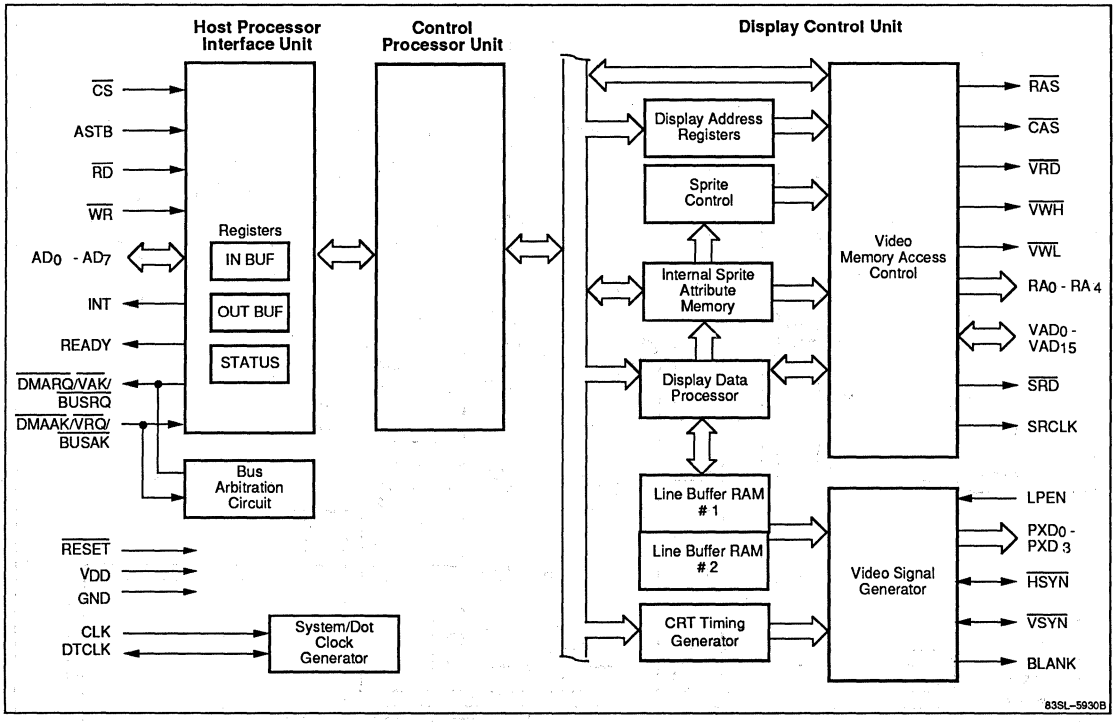
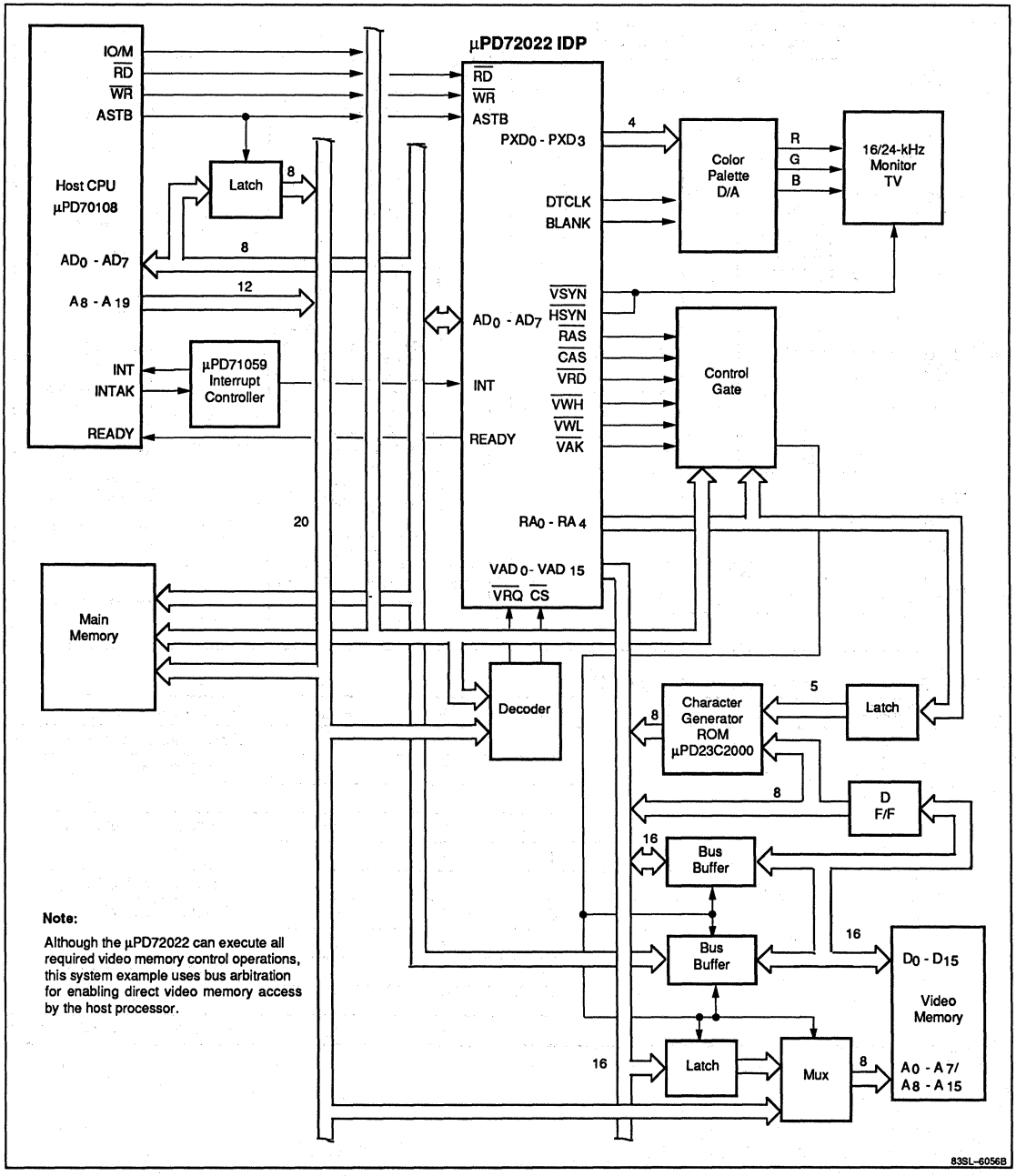


Table 1. Functions of Address/Data Bus AD_0-AD_7

$\overline{CS}$	$\overline{DMAAK}$	$\overline{WR}$	$\overline{RD}$	AD_2	AD_1	AD_0	Bus Function
1	1	x	x	x	x	x	Floating (high impedance)
0	1	0	1	0	1	0	μPD72022 command input
				1	1	1	
				0	1	1	μPD72022 parameter input
				1	1	0	
1	0	0	1	x	x	x	Write operation via DMA transfer
0	1	1	0	0	1	0	μPD72022 status output
				1	1	1	
				0	1	1	μPD72022 parameter output
				1	1	0	
1	0	1	0	x	x	x	Read operation via DMA transfer

x = Don't care

μPD72022 in a Video Display System



Absolute Maximum Ratings

T_A = +25°C

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to +7.0 V
Output voltage, V_O	−0.5 to +7.0 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Capacitance

T_A = +25°C; V_{DD} = GND = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Input capacitance	C_I		10	pF	Unmeasured pins returned to 0 V
Output capacitance	C_O		20	pF	
Input/output capacitance	C_{IO}		20	pF	
Clock input capacitance	C_C		20	pF	

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Input low voltage	V_{IL}	−0.5	0.8	V	Note 1
		−0.5	0.6	V	Note 2
Input high voltage	V_{IH}	2.2	V_{DD} + 0.5	V	Note 1
		3.5	V_{DD} + 1.0	V	Note 2
Output low voltage	V_{OL}		0.45	V	I_{OL} = 2.2 mA
Output high voltage	V_{OH}	0.7 V_{DD}		V	I_{OH} = −400 μA
Input low leakage current	I_{LIL}		−10	μA	V_I = 0 V
Input high leakage current	I_{LIH}		10	μA	V_I = V_{DD}
Output low leakage current	I_{LOL}		−10	μA	V_I = 0 V
Output high leakage current	I_{LOH}		10	μA	V_I = V_{DD}
Power supply current	I_{DD}		150	mA	

Notes:

(1) Except CLK, DTCLK, and $\overline{\text{RESET}}$

(2) CLK, DTCLK, and $\overline{\text{RESET}}$

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
Clock						
System clock cycle	2	t_{CY}	45	50	ns	
System clock width, high	2	t_{KKH}	18		ns	
System clock width, low	2	t_{KKL}	18		ns	
Dot clock cycle	2	t_{CYDK}	45	4 t_{CY}	ns	Input; C_L = 30 pF
			67.5	4 t_{CY}	ns	Output; C_L = 30 pF
Dot clock width, high	2	t_{DKDKH}	18		ns	Input; C_L = 30 pF
			t_{KKH}		ns	Output; C_L = 30 pF
Dot clock width, low	2	t_{DKDKL}	18		ns	
Reset						
$\overline{\text{RESET}}$ pulse width	3	t_{RSRSL}	8 t_{CY} + 6 t_{CYDK}		ns	
LPEN setup time to $\overline{\text{RESET}}$ ↑	3	t_{SLPRS}	16 t_{CY}			
LPEN hold time from $\overline{\text{RESET}}$ ↑	3	t_{HRSLP}	0			
CPU Read/Write Cycle						
ASTB pulse width	4, 5	t_{STSTH}	45		ns	
Address setup time to ASTB ↓	4, 5	t_{SAST}	25		ns	
Address hold time from ASTB ↓	4, 5	t_{HAST}	10		ns	
$\overline{\text{CS}}$ setup time to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ ↓	4, 5	t_{SCSRW}	0		ns	

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AC Characteristics (cont)

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
CPU Read/Write Cycle (cont)						
$\overline{CS}$ hold time from $\overline{RD}$ or $\overline{WR}$ ↑	4, 5	t_{HRWCS}	0		ns	
$\overline{RD}$ pulse width	4, 15	t_{RRL}	170		ns	
Data delay time from $\overline{RD}$ ↓	4, 15	t_{DRD}	120		ns	
Data hold time from $\overline{RD}$ ↑	4, 15	t_{HRD}	0		ns	
Data float time from $\overline{RD}$ ↑	4, 15	t_{FRD}		55	ns	
$\overline{WR}$ pulse width	5, 16	t_{WWL}	180		ns	
Data setup time to $\overline{WR}$ ↑	5, 16	t_{SDW}	100		ns	
Data hold time from $\overline{WR}$ ↑	5, 16	t_{HWD}	10		ns	
READY delay time from $\overline{RD}$ or $\overline{WR}$ ↓	4, 5, 16	t_{DRWRDY}		55	ns	
READY delay time from $\overline{VRQ}$ ↓	9	t_{DVQRDY}		60	ns	
$\overline{RD}$ recovery time	4	t_{RVR}	150		ns	
$\overline{WR}$ recovery time	5	t_{RVW}	150		ns	
Read access cycle	4	t_{CYR}	$t_{RRL} + 10\,t_{CY}$		ns	
Write access cycle	5	t_{CYW}	$t_{WWL} + 10\,t_{CY}$		ns	
VRAM Read/Write Cycle						
Random read/write cycle	6-8, 11-13	t_{CYRAS}	270		ns	Note 1; also refresh cycle
			360		ns	Note 2; also data transfer cycle
$\overline{RAS}$ width high	6-8, 11-13	$t_{RASRASH}$	95		ns	
$\overline{RAS}$ width low	6-8, 11-13	$t_{RASRASL}$	130		ns	Note 1; also refresh cycle
			210		ns	Note 2; also data transfer cycle
$\overline{CAS}$ width high	6-7, 11-13	$t_{CASCASH}$	110		ns	
$\overline{CAS}$ width low	6-7, 11-13	$t_{CASCASL}$	105		ns	Note 1
			185		ns	Note 2; also data transfer cycle
$\overline{RAS}$ ↓ delay time from $\overline{CAS}$ ↑	6-8, 11-13	$t_{DCASRASL}$	30		ns	
$\overline{CAS}$ ↓ delay time from $\overline{RAS}$ ↓	6-7, 11-13	$t_{DRASCASL}$	40		ns	
$\overline{RAS}$ ↑ delay time from $\overline{CAS}$ ↓	6-7, 11-13	$t_{DCASRASH}$	60		ns	Note 1
			150		ns	Note 2; also data transfer cycle
Address setup time to $\overline{RAS}$ ↓	6-8, 11-13	t_{SVARAS}	35		ns	
Address hold time from $\overline{RAS}$ ↓	6-8, 11-13	t_{HRASVA}	10		ns	
Mode setup time to $\overline{CAS}$ ↓	6-7, 11-13	t_{SMDCAS}	10		ns	
Mode hold time from $\overline{CAS}$ ↓	6-7, 11-13	t_{HCASMD}	110		ns	Note 1
			185		ns	Note 2

AC Characteristics (cont)

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
VRAM Read/Write Cycle (cont)						
$\overline{VRD}$ ↑ delay time from $\overline{CAS}$ ↓	6, 12-13	t_{DCASVR}	70		ns	Note 1
			150		ns	Note 2
$\overline{CAS}$ ↑ delay time from $\overline{VRD}$ ↑	6, 11-13	t_{DVRCAS}	0		ns	
$\overline{VRD}$ pulse width	6, 12-13	t_{VRVRL}	70		ns	Note 1
			150		ns	Note 2
$\overline{CAS}$ ↓ delay time from $\overline{VW}$ ↑	6	$t_{DVWHCAS}$	70		ns	
$\overline{VW}$ ↓ delay time from $\overline{RAS}$ ↑	6	$t_{DRASHVW}$	35		ns	
$\overline{VW}$ ↓ delay time from $\overline{CAS}$ ↑	6	$t_{DCASVWL}$	15		ns	
Input data setup time to $\overline{VRD}$ ↑	6	t_{SDVR}	40		ns	
Input data hold time from $\overline{VRD}$ ↑	6	t_{HVRD}	0	30	ns	
$\overline{VRD}$ ↑ delay time from $\overline{RAS}$ ↓	6, 12-13	$t_{DRASVRH}$	130		ns	Note 1
			210		ns	Note 2
$\overline{RAS}$ ↓ setup time from $\overline{VRD}$ ↑	6, 12-13	t_{SVRRAS}	15		ns	
$\overline{VRD}$ ↓ hold time from $\overline{RAS}$ ↓	6, 12-13	t_{HRASVR}	25		ns	
VRAM Write Cycle						
$\overline{RAS}$ ↓ delay time from $\overline{VRD}$ ↑	7	t_{DVRRAS}	15		ns	
$\overline{VRD}$ ↓ delay time from $\overline{RAS}$ ↓	7	$t_{DRASVRL}$	130		ns	
$\overline{RAS}$ ↓ delay time from $\overline{VW}$ ↑	7	t_{DVWRAS}	35		ns	
$\overline{VW}$ ↑ delay time from $\overline{RAS}$ ↓	7	$t_{DRASLVW}$	−10		ns	
$\overline{CAS}$ ↓ delay time from $\overline{VW}$ ↓	7	$t_{DVWLCAS}$	10		ns	
$\overline{VW}$ ↑ delay time from $\overline{CAS}$ ↓	7	$t_{DCASVWH}$	155		ns	
$\overline{VW}$ pulse width	7	t_{VWVWL}	165		ns	
Data setup time to $\overline{CAS}$ ↓	7	t_{SDCAS}	10		ns	
Data hold time from $\overline{CAS}$ ↓	7	t_{HCASD}	155		ns	
VRAM Refresh Cycle						
$\overline{CAS}$ ↓ delay time from $\overline{RAS}$ ↑	8	$t_{DRASHCAS}$	20		ns	
VRAM Request						
$\overline{VAK}$ setup time to $\overline{CAS}$ ↑	9	t_{SVACAS}	20		ns	Interleave mode
$\overline{VAK}$ hold time from $\overline{CAS}$ ↓	9	t_{HCASVA}	10		ns	
VRQ recovery time	9	t_{RVVQ}	10 t_{CY}		ns	
READY delay time from $\overline{VRQ}$ ↓	9	t_{DVQRDY}		60	ns	
$\overline{VRQ}$ hold time from READY ↑	9	t_{HRDYVQ}	0		ns	
VAD float delay time from $\overline{CAS}$ ↑	9,10	$t_{FCASVAD}$		30	ns	
VAD delay time from $\overline{CAS}$ ↑	9, 10	$t_{DCASVAD}$		50	ns	

3

AC Characteristics (cont)

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
VRAM Request (cont)						
$\overline{BURSQ}$ ↓ delay time from $\overline{BUSAK}$ ↑	10	t_{DBABQ}	0		ns	Dual-port mode
$\overline{BUSAK}$ hold time from $\overline{BUSRQ}$ ↑	10	t_{HBQHBA}	10		ns	
$\overline{BUSAK}$ hold time from $\overline{BUSRQ}$ ↓	10	t_{HBQLBA}	0	2000	ns	
Data Transfer Cycle						
$\overline{VRD}$ ↑ delay time from SRCLK ↑	11	t_{DSKVR}	100		ns	
SRCLK hold time from $\overline{VRD}$ ↑	11	t_{HVRSK}	100		ns	
$\overline{RAS}$ ↓ delay time from $\overline{VRD}$ ↓	11	$t_{DVRRASL}$	30		ns	
$\overline{VRD}$ hold time from $\overline{RAS}$ ↓	11	$t_{HRASLVR}$	60		ns	
$\overline{VRD}$ hold time from $\overline{CAS}$ ↓	11	t_{HCASVR}	10		ns	
$\overline{RAS}$ ↑ delay time from $\overline{VRD}$ ↓	11	$t_{DVRRASH}$	100		ns	
$\overline{CAS}$ ↑ delay time from $\overline{VRD}$ ↑	11	t_{DVRCAS}	120		ns	
$\overline{VRD}$ hold time from $\overline{RAS}$ ↑	11	$t_{HRASHVR}$	10		ns	
VRAM Serial Read Cycle						
$\overline{SRD}$ width high	12, 13	t_{SRSRH}	200		ns	
$\overline{SRD}$ width low	12, 13	t_{SRSRL}	200		ns	
SRCLK ↓ delay time from $\overline{SRD}$ ↓	12, 13	t_{DSRSK}	15		ns	
SRCLK width high	12, 13	t_{SKSKH}	25		ns	
SRCLK width low	12, 13	t_{SKSKL}	25		ns	
Serial read cycle	12, 13	t_{CYSK}	90		ns	
Data setup time to SRCLK ↑	12	t_{SDSK}	25		ns	Graphics display cycle
Data hold time from SRCLK ↑	12	t_{HSKD}	10		ns	
Data setup time to $\overline{VRD}$ ↑	13	t_{SDVR}	40		ns	Text display cycle
Data hold time from $\overline{VRD}$ ↑	13	t_{HVRD}	0	30	ns	Semigraphics display cycle
Display Timing						
Output display time from DTCLK ↑	14	t_{DDKDSP}	5	38	ns	Note 3; C_L = 50 pF
Input setup time to DTCLK ↑	14	t_{SIDK}	25		ns	Note 4
Input hold time from DTCLK ↑	14	t_{HDKI}	5		ns	
Input pulse width	14	t_{II}	6 t_{CYDK}		ns	
DMA Cycle						
$\overline{DMARQ}$ ↑ delay time from $\overline{DMAAK}$ ↓	15, 16	t_{DDADQH}		50	ns	
$\overline{DMARQ}$ ↓ delay time from $\overline{DMAAK}$ ↑	15, 16	t_{DDADQL}	0		ns	
$\overline{DMAAK}$ hold time to $\overline{DMARK}$ ↓	15, 16	t_{HDQDA}	0		ns	
$\overline{DMAAK}$ setup time to RD ↓	15	t_{SDAR}	0		ns	
$\overline{DMAAK}$ hold time to RD ↑	15	t_{HRDA}	20		ns	
$\overline{DMAAK}$ setup time to WR ↓	16	t_{SDAW}	0		ns	
$\overline{DMAAK}$ hold time to WR ↑	16	t_{HWDA}	20		ns	

AC Characteristics (cont)

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
Interrupt						
INT rising time	17	t_{INTR}		30	ns	
INT falling time	17	t_{INTF}		30	ns	

Notes:

(1) Cycles: Text display; Semigraphics display; Display start

(2) Cycles: Graphics display; Sprite display; Command processing

(3) $\overline{HSYN}$, $\overline{VSYN}$, BLANK, PXD0-PXD3

(4) $\overline{HSYN}$, $\overline{VSYN}$, LPEN

Figure 1. Voltage Thresholds for Timing Measurements

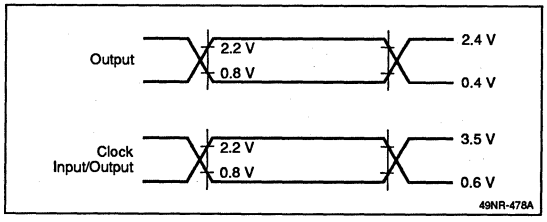

Figure 2. Clock Waveform

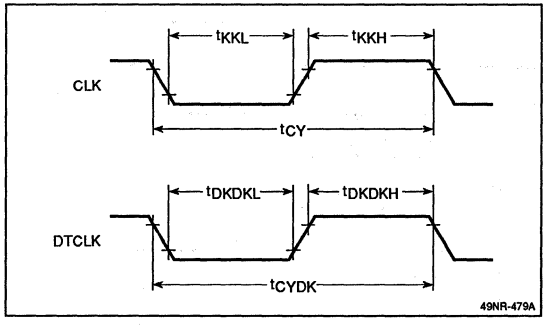

Figure 3. Reset Waveform

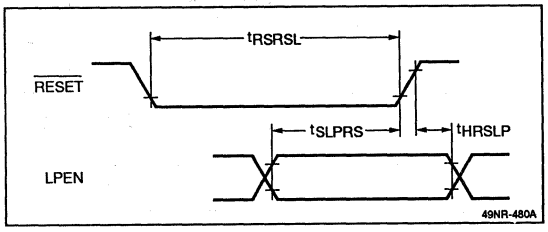

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Figure 4. CPU Read Cycle

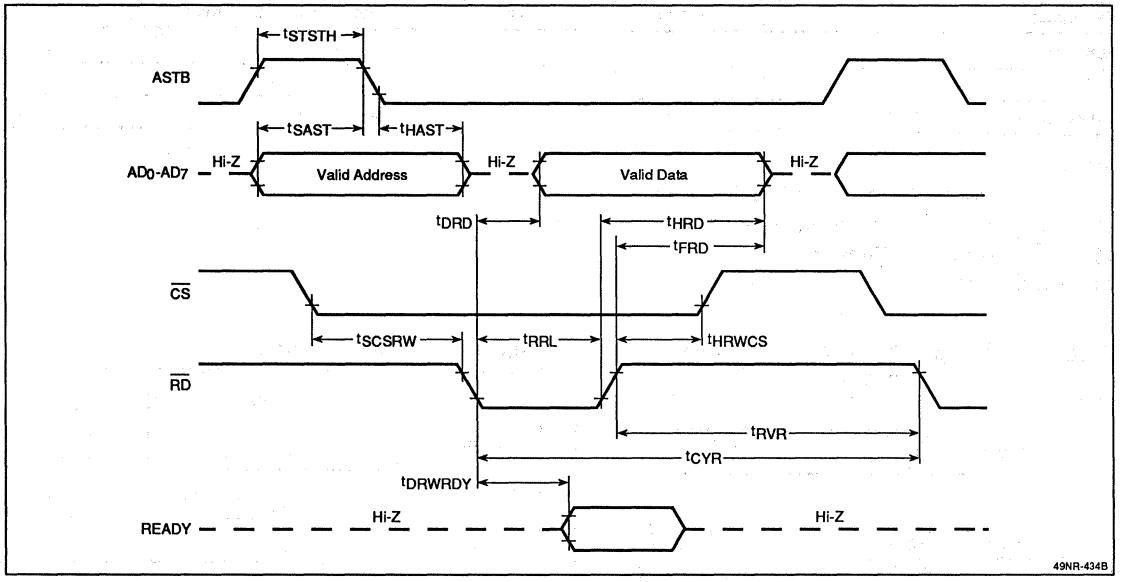


Figure 5. CPU Write Cycle

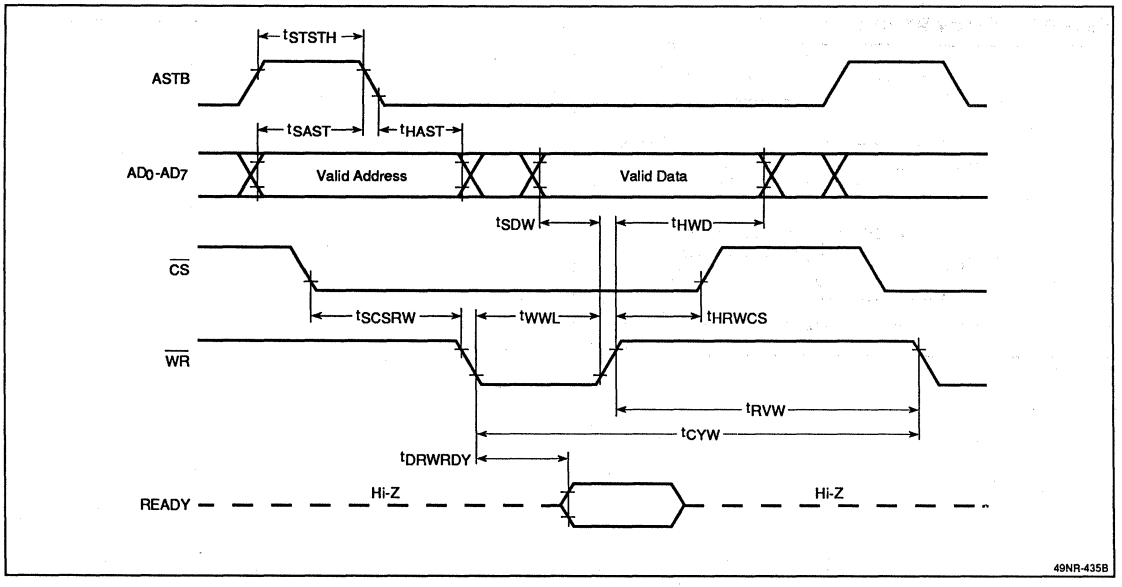


Figure 6. VRAM Read Cycle

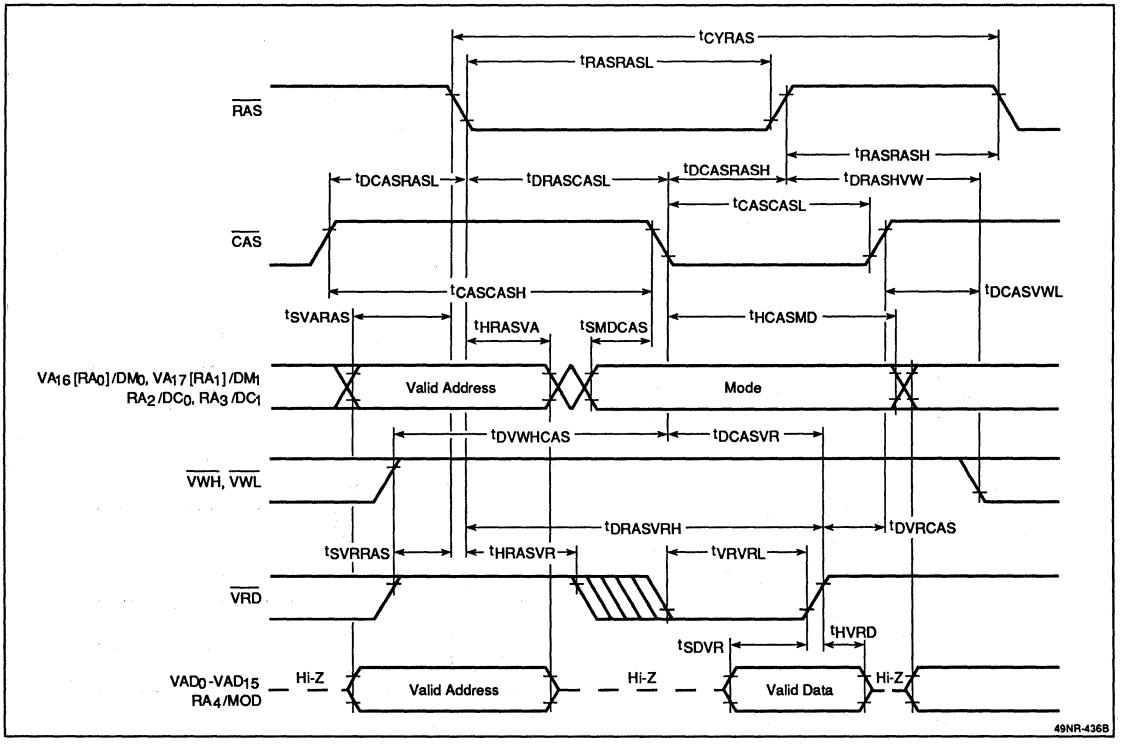


Figure 7. VRAM Write Cycle

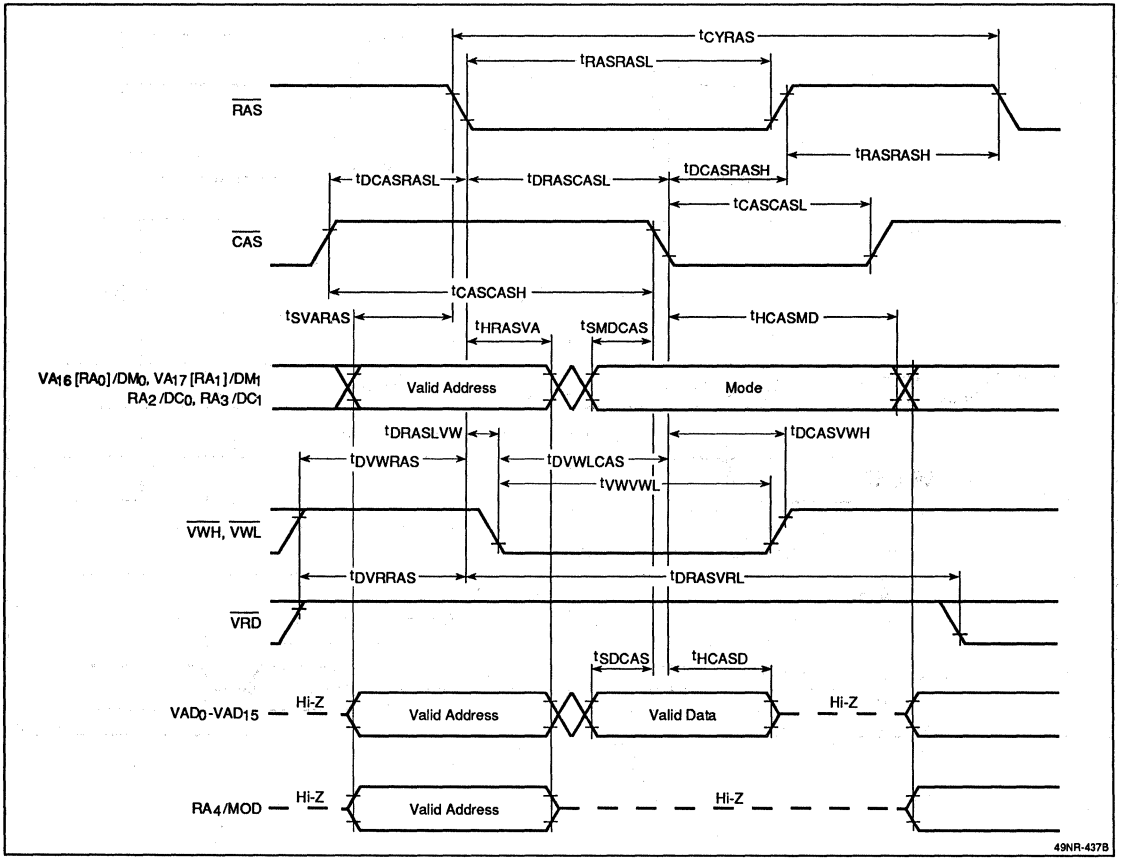


Figure 8. VRAM Refresh Cycle

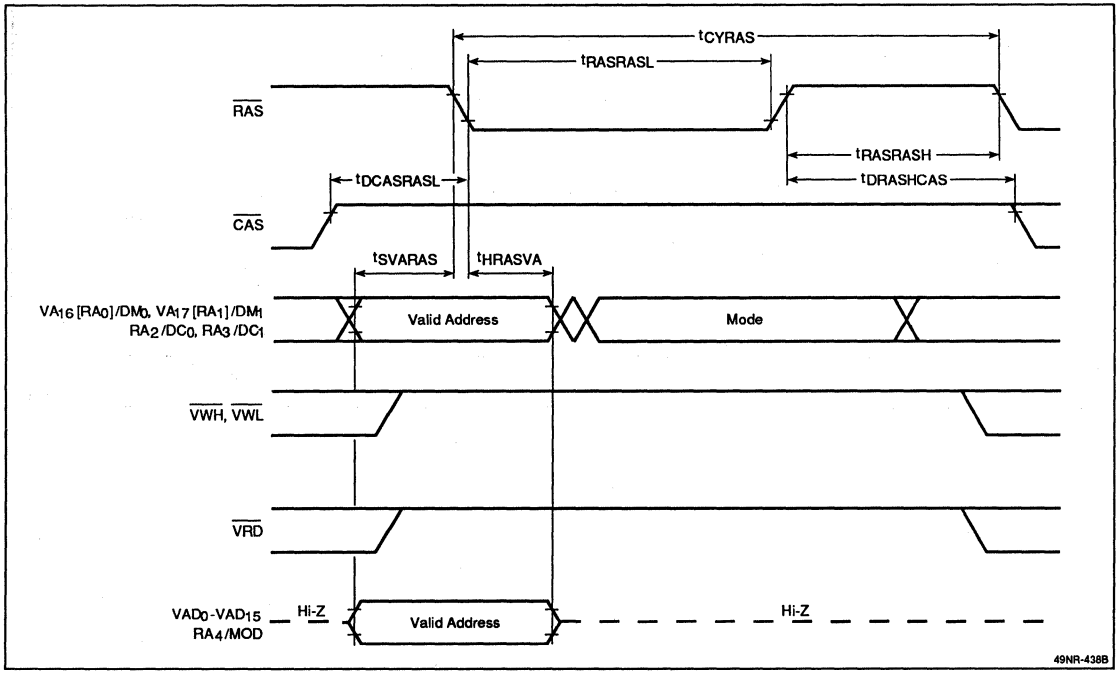


Figure 9. VRAM Request; Interleave Mode

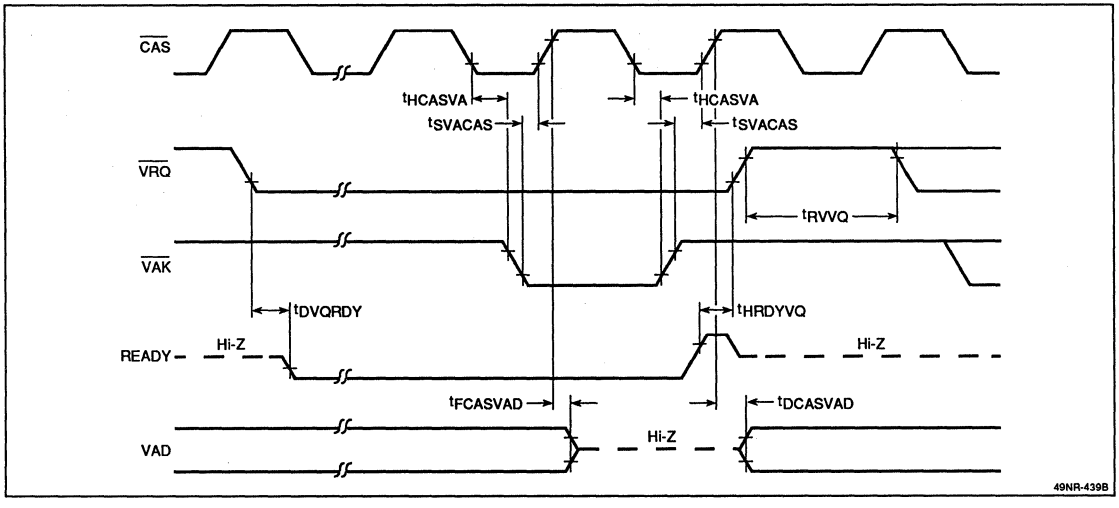


Figure 10. VRAM Request; Dual-Port Mode

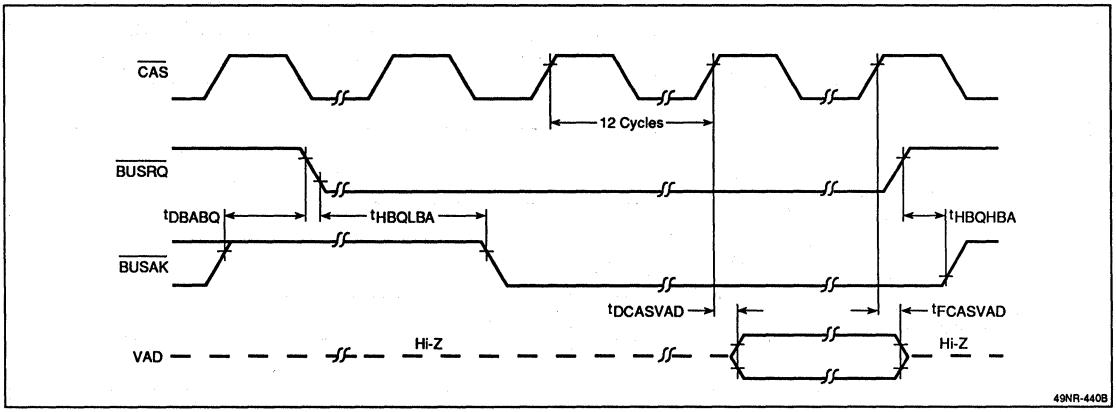


Figure 11. Data Transfer Cycle

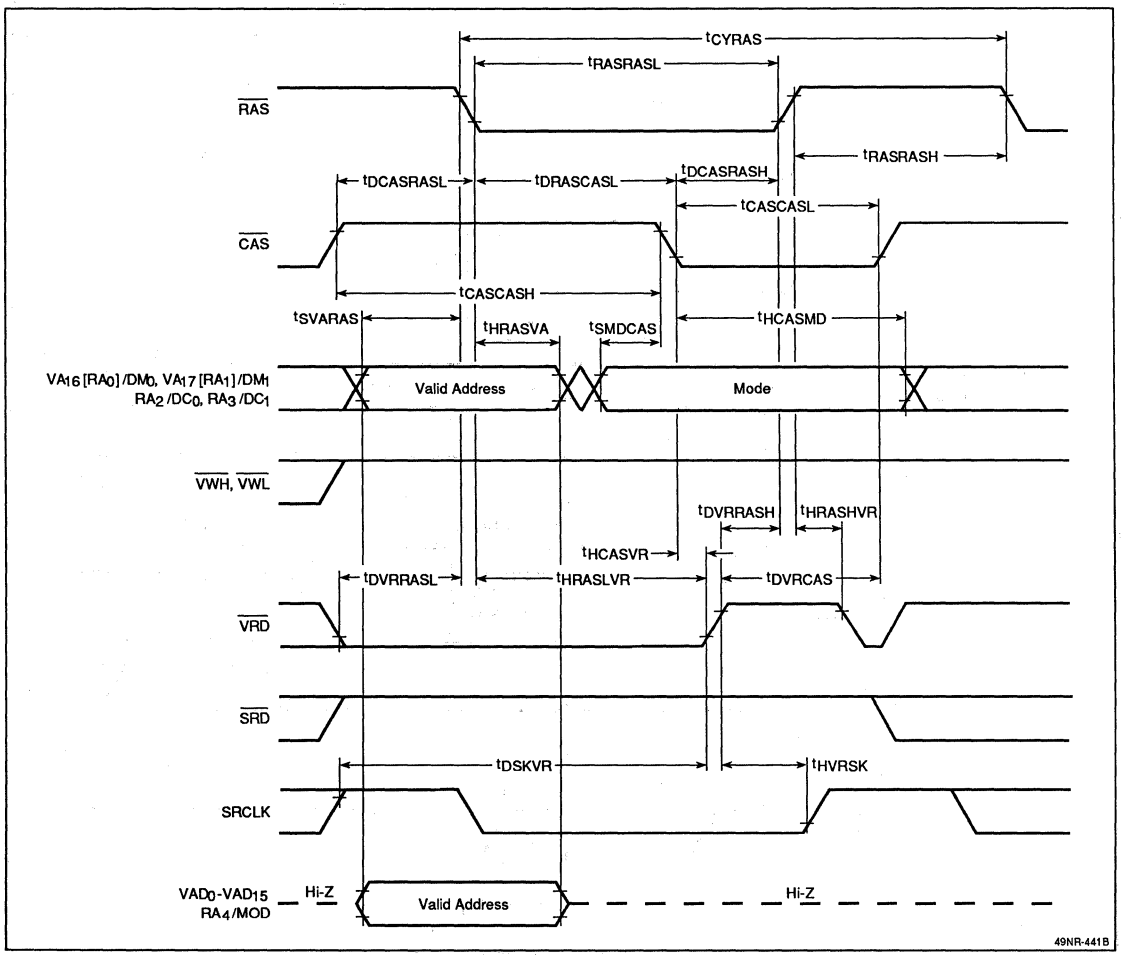


Figure 12. VRAM Serial Read Cycle; Graphics Display

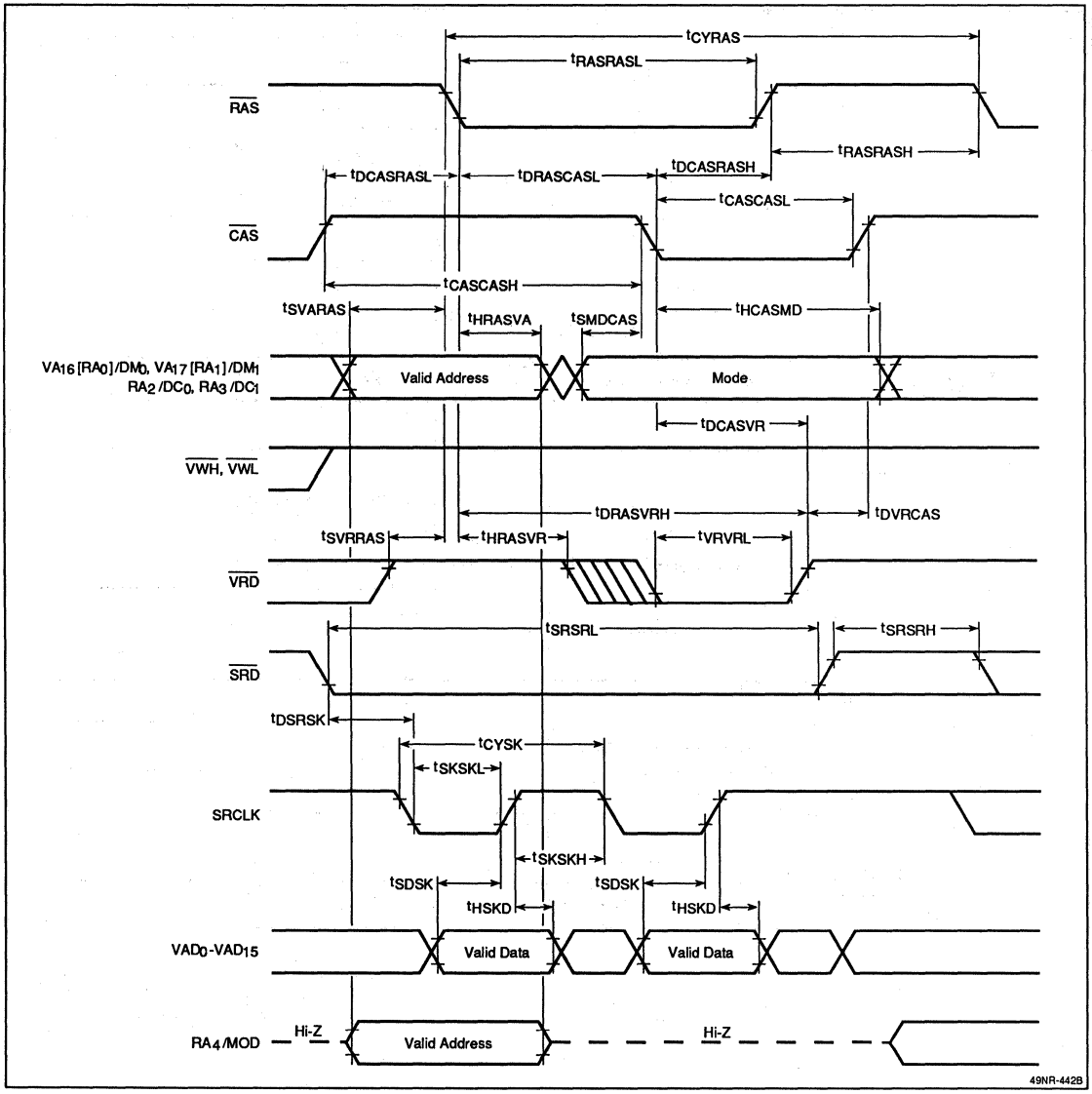


Figure 13. VRAM Serial Read Cycle; Text or Semigraphics Display

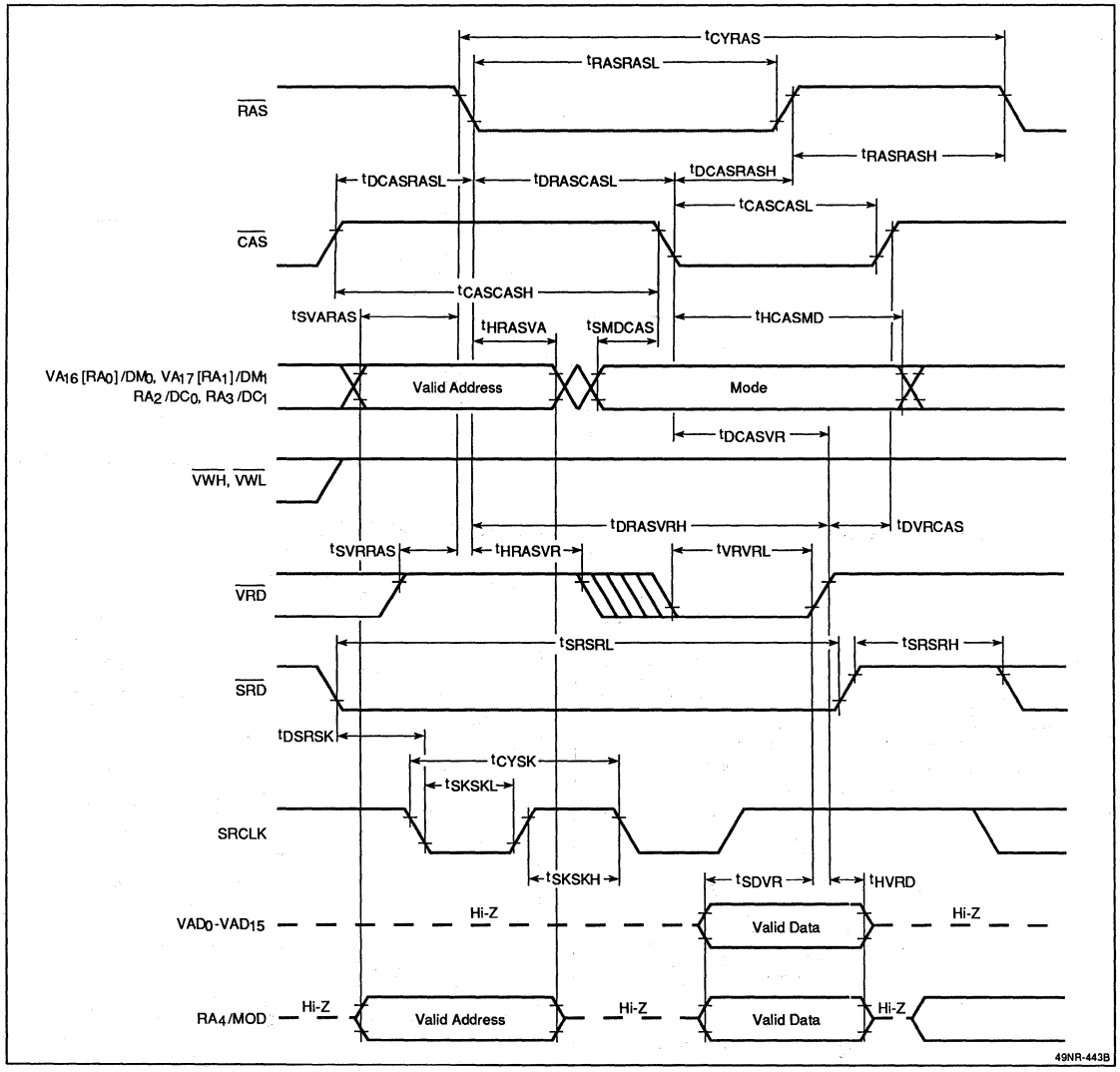


Figure 14. Display Timing

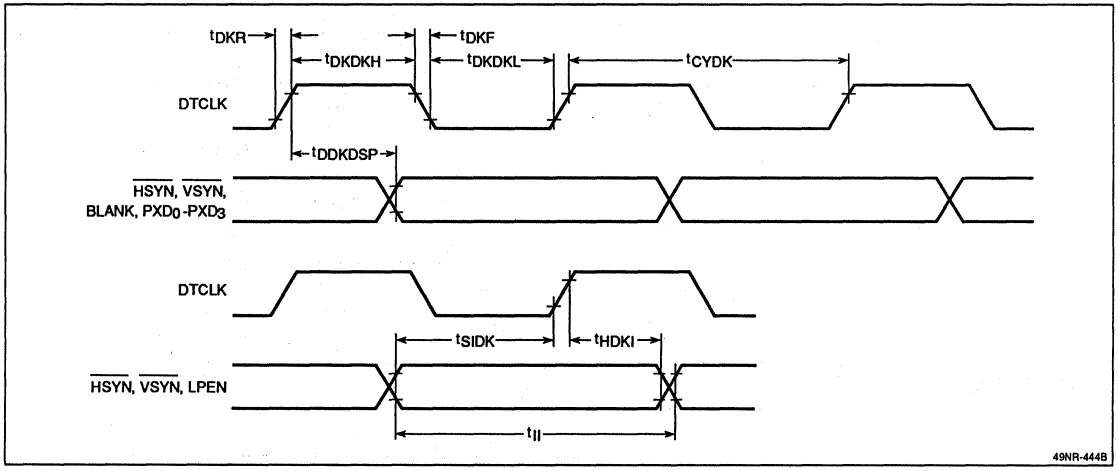


Figure 15. DMA Read Cycle

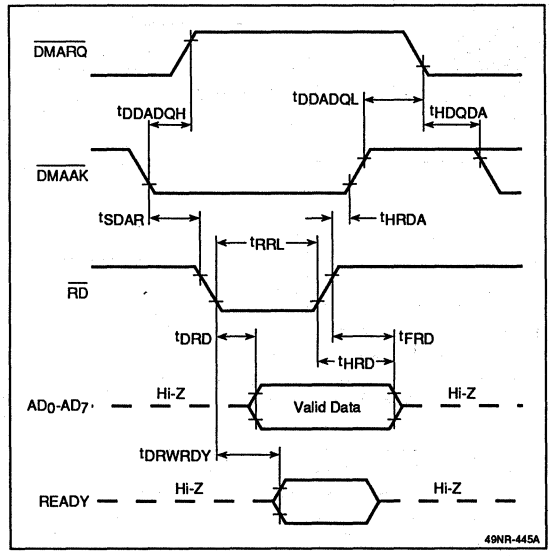


Figure 16. DMA Write Cycle

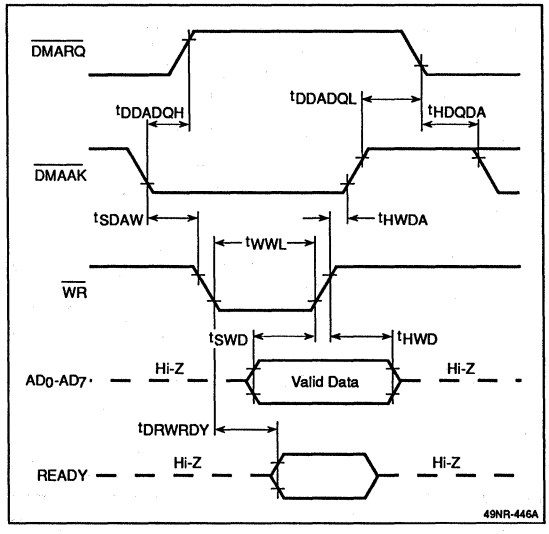
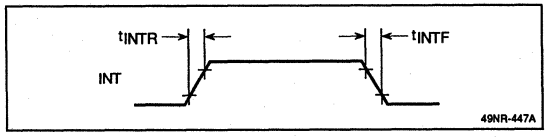


Figure 17. Interrupt Waveform



INTERNAL STRUCTURE

The μPD72022 IDP consists of three units: host processor interface unit, control processor unit, and display control unit. Refer to the μPD72022 Block Diagram.

Host Processor Interface Unit

The host processor interface unit transfers commands, parameters, and such status information as the μPD72022 internal processing state, to and from the host processor.

Control functions include asynchronous bus interface control, DMA control, and interrupt control.

Control Processor Unit

The control processor unit reads and executes commands and parameters from the host processor via the host processor interface unit.

Display data processing in video memory, display address control, screen control, etc., in the display control unit are implemented.

Display Control Unit

The display control unit generates and outputs video memory display addresses, display signals, and CRT control signals. It generates various timing signals required in the μPD72022.

COMMANDS

The μPD72022 has 22 commands for implementing initialization, display control, and sprite control operations. See table 2.

Table 2. List of Commands

Name	Function
Initialization	
SYNC	Selects display operation mode and specifies scan timing.
Display Control	
DSPOF	Generates screen control table base address and border color; enables display controller; starts display.
DSPOP	Disables display controller and terminates display.
DSPDEF	Defines display screen layout and display format.
CURDEF	Defines cursor display format.
ACTSCR	Selects active screen area.
CURS	Moves cursor to specified cursor display position.
LPNR	Determines light pen position.

Table 2. List of Commands (cont)

Name	Function
Video Memory Control	
DPLD	Specifies video memory operation address or address offset.
DPRD	Determines video memory operation address.
MASK	Sets bit mask for data storage in video memory.
RDAT	Reads contents of video memory and sends data to host processor.
WDAT	Stores transfer data in video memory.
BLKTOT	Reads the video memory contents and transfers the data via DMA operation.
BLKTIN	Stores the data transferred via DMA operation into the video memory.
EXIT	Terminates video memory operation command processing.
Sprite Control	
SPRON	Enables the sprite controller and initiates sprite image display.
SPROF	Disables the sprite controller and terminates sprite image display.
SPRSW	Toggles the sprite display on or off for each sprite operation.
SPRRD	Reads the sprite attribute table data.
SPRWR	Writes data into the sprite attribute table.
SPROV	Determines the sprite controller operation status.

3

INITIALIZATION COMMANDS

SYNC Command

Command Code 10H

0	0	0	1	0	0	0	0

Parameters

RM		EL	EV	VM	0	DPM	ILM
0	RF	EC	ES	RV	RS		
0	0	LBL					
0	0	LBR					
HAD							
0	0	RBR					
0	0	RBL					
0	0	HS					
0	0	TBL					
0	0	TBR					
VAD (L)							
0	VAD (H)	BBR					
0	0	BBL					
0	0	VS					

The SYNC command terminates display controller operation and defines operation mode and horizontal/vertical scan timing with the following parameters.

- **ILM, DPM** (Interleave Mode, Dual Port Mode)

  The format of the interblock interface between the host system, IDP, and video memory is specified. Dual-port mode can only be specified for the VRAM serial access (VM = 1).

DPM	ILM	Operation
0	0	Standalone mode
0	1	Interleave mode
1	0	Dual-port mode
1	1	Disabled

- **EV** (Enable Vertical Blank Interrupt)

  Parameter EV determines whether the occurrence of a vertical blanking signal causes an interrupt signal to be generated on the INT pin.

EV	Interrupt
0	Vertical blank interrupt disabled
1	Vertical blank interrupt enabled

- **EL** (Enable Light Pen Interrupt)

  Parameter EL specifies whether the occurrence of a light-pen signal causes an interrupt signal to be generated on the INT line.

EL	Interrupt
0	Light pen interrupt disabled
1	Light pen interrupt enabled

- **VM** (VRAM Access Mode)

  Parameter VM specifies the video memory access mode for static picture display data generation.

VM	Video Memory
0	Random access mode
1	Serial access mode

- **RM** (Raster Mode)

  Parameter RM specifies CRT scanning mode and display signal generation mode.

RM	CRT Scanning Mode
00	Noninterlace (640 x 400, 24K CRT)
01	Interlace (640 x 400, 15K CRT)
10	Vertical magnify (640 x 200, 24K CRT)
11	Normal (640 x 200, 15K CRT)

- **RS** (Resolution Select)

  Parameter RS specifies the divide ratio for generation of the display signal dot time. This ratio can be combined with horizontal and vertical scan timing to vary display resolution. Table 3 is an example based on a 20-MHz source clock.

Table 3. Display Resolution Example (20-MHz Clock)

RS	Divide Ratio	Corresponding Resolution	HAD Setup Value	VAD Setup Value	Recommended CRT
000	Divide by 4	256 x 192	256 (63)	192	Horizontal scan frequency 15.75 kHz
001	Divide by 3	320 x 200	320 (79)	200	
010	Divide by 2	512 x 192	512 (127)	192	
011	Divide by 1.5	640 x 200	640 (159)	200	
100	Divide by 1	640 x 400	640 (159)	400	24.83 kHz
Others			Disabled (dot clock is not output)		

- **RV** (Reverse Screen)

  Parameter RV specifies reverse display of the entire screen. When RV is cleared to 0, normal display is enabled; when RV is set to 1, text foreground and background colors in the text display are reversed.

- **ES** (External Sync)

  Parameter ES specifies use of the $\overline{\text{HSYN}}$ and $\overline{\text{VSYN}}$ pins and external synchronization. When ES is set to 1, horizontal and vertical synchronizing signals are output on the $\overline{\text{HSYN}}$ and $\overline{\text{VSYN}}$ pins.

  When ES is cleared to 0, the pins are placed in a high-impedance state, and display timing is synchronized with an input reference signal.

- **EC** (External Clock)

  Parameter EC specifies DTCLK pin operation and determines display timing signals. When EC is set to 1, a signal generated from the internal divider is output on the DTCLK pin as dot clock.

  When EC is cleared to 0, the DTCLK pin is placed in a high-impedance state, and display timing is based on an input clock reference signal.

  EC an be set in external dot clock input mode (LPEN signal is low at reset time).

- **RF** (Refresh Control)

  Parameter RF controls video memory refresh operations. When RF is cleared to 0, no refresh operation is performed; when set to 1, refresh operations are initiated.

- **LBL** (Left Blanking) See figure 18.
  LBR (Left Border)
  HAD (Horizontal Active Display)
  RBR (Right Border)
  RBL (Right Blanking)
  HS (Horizontal Sync)

  Horizontal scan timing is specified in four-dot time (TCK) units. Each timing is generated at the time of (specified value + 1) x TCK.

  The horizontal scan parameters have the following restrictions.

  HS ≥ 04H
  LBL ≥ 03H
  HAD = odd number (bit 0 = 1)

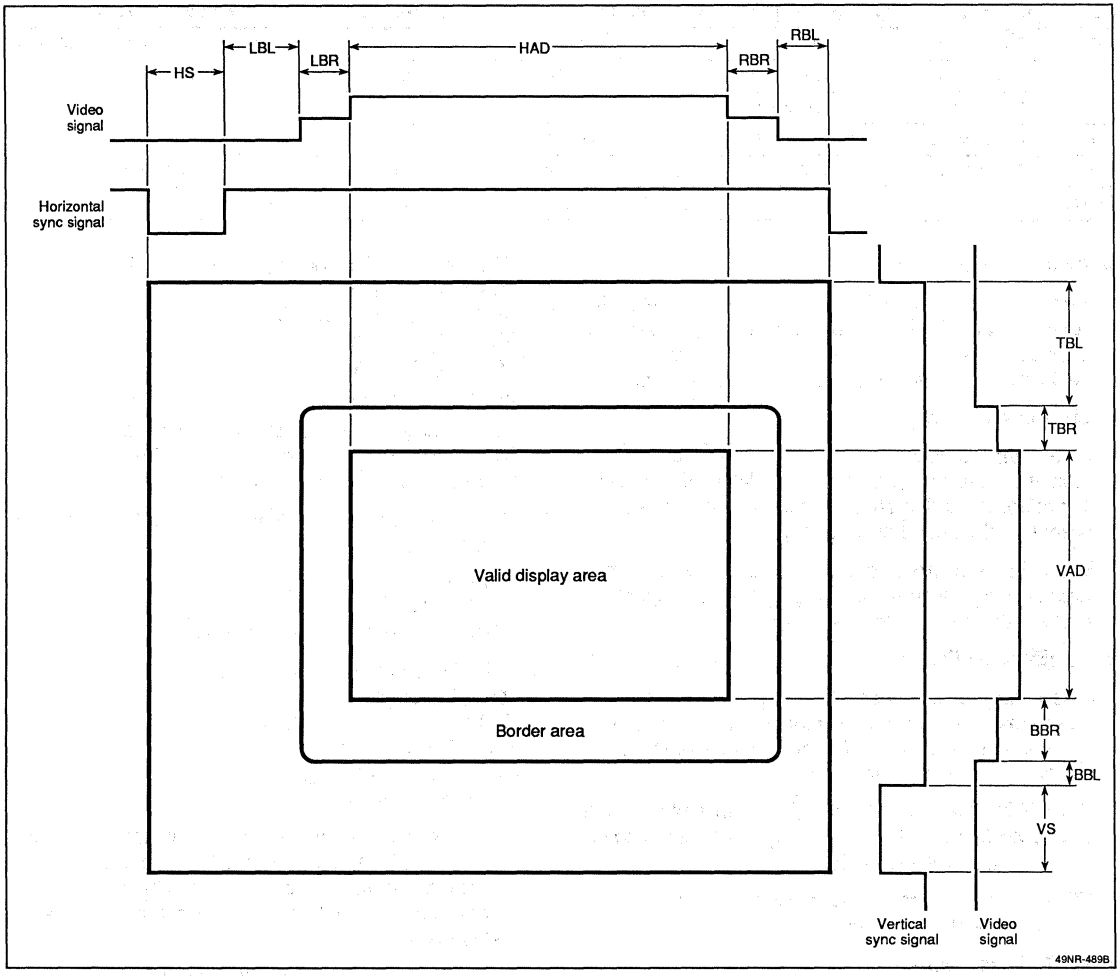
- **TBL** (Top Blanking) See figure 18
  TBR (Top Border)
  VAD (Vertical Active Display)
  BBR (Bottom Border)
  BBL (Bottom Blanking)
  VS (Vertical Sync)

  The number of rasters (vertical scan lines) is specified to control vertical scan timing. An integer multiple of 2 is set in the valid display time (VAD). The vertical border time (TBR, BBR) can be omitted if the specified value is 0.

  The vertical scan parameters have the following restrictions.

  VS ≥ 04H
  TBL + TBR ≥ 10H (for non-sprite display)
  TBL + TBR ≥ 20H (for sprite display)
  VAD ≥ 04H
  BBR + BBL ≥ 02H

Figure 18. Horizontal and Vertical Scan Parameters



DISPLAY CONTROL COMMANDS

DSPON Command

Command Code 12H

0	0	0	1	0	0	1	0

Parameters

Base address					(lower)
0	0	0	0	0	(upper)
0	0	0	0	BC	

The DSPON command enables the display controller and generates the display signal.

In display access after the screen control table base address is specified in byte units, the address provided by multiplying the setup value by 256 is referenced as the screen control table start address.

- **BC** (Back Drop Color)

  Parameter BC specifies the background color of the transparent color specification portion of the valid display time and the horizontal/vertical border area.

DSPOF Command

Command Code 13H

0	0	0	1	0	0	1	1

The DSPOF command disables the display controller and sprite controller and terminates display. The horizontal/vertical retrace time is output on the display signal output pin.

DSPDEF Command

Command Code 14H

0	0	0	1	0	1	0	0

Parameters

ATROFF (L)							
ATROFF (M)							
0	PITCH			0	(H)		
0	0	0	MRA				
0	0	0	HRA				
BR				0	0	0	

The DSPDEF command defines display screen layout and display format. The following parameters are specified.

- **ATROFF** (Attribute Offset)

  The character code and attribute code store address offset are specified in byte units. If the offset is a negative value, input the complement.

ATROFF	Offset
0H	Disabled
1H	1 byte
2H	2 bytes
:	:
3FFFFH	262,143 bytes
40000H	−262,144 bytes
:	:
7FFFFH	−1 byte

- **PITCH** (Character Pitch)

  The character code pitch is specified.

PITCH	Pitch
0H	Disabled
1H	1 byte
:	:
7H	7 bytes

- **MRA** (Maximum Raster Address)

  The character vertical display size is specified in number of rasters. This position is used as the underline display position.

MRA	No. of Rasters
0 to 6H	Disabled
7H	8 rasters
:	:
1FH	32 rasters

- **HRA** (Horizontal Raster Address)

  The horizontal line display position is specified as a raster position.

HRA	Display Position
0H	First raster
1H	Second raster
:	:
1FH	32nd raster

- **BR** (Blinking Rate)

  The blink attribute character display and cursor blink are specified. Each character specified with the blink attribute is turned on (bright) in the time of the setup value x 24 fields and off (dark) in the time of the setup value x 8 fields.

  The cursor blinks in the time of the setup value x 8 fields.

  The number of bright and dark fields for attribute and cursor blink are shown below.

	Attribute		Cursor	
BR	Bright	Dark	Bright	Dark
0H	768	256	256	256
1H	24	8	8	8
2H	48	16	16	16
:	:	:	:	:
1FH	744	248	248	248

CURDEF Command

Command Code 15H

0	0	0	1	0	1	0	1

Parameters

CURN			0	CE	BE

The CURDEF command defines the cursor display mode. Parameter CURN specifies cursor sprite, and the CURS command specifies the cursor position, which also updates the display position of the sprite specified in CURN.

- **BE** (Blinking Enable)

  Parameter BE specifies whether cursor blinking is enabled. To suppress cursor blinking, clear BE to 0.

- **CE** (Cursor Enable)

  Parameter CE specifies whether cursor display is enabled. To turn off the cursor, clear CE to 0.

  Since the sprite function is used for cursor display, specify sprite display accordingly at the same time.

ACTSCR Command

Command Code 16H

0	0	0	1	0	1	1	0

Parameters

0	SCRN		0	0	0	0	0

The active screen area where cursor position control and light pen position control are valid is specified.

SCRN	Active Screen Area
0	First split screen
1	Second split screen
2	Third split screen
3	Fourth split screen

CURS Command

Command Code 1EH

0	0	0	1	1	1	1	0

Parameters

Vertical position (lower)					
0	0	0	0	0	(upper)
Horizontal position (lower)					
0	0	0	0	0	0	(upper)

The cursor is moved to the position specified by the parameters.

Screen position is specified by virtual screen coordinates, first designating a Y (line) position value, then an X (column) position value. If a specified position exceeds the lower or right edge of the virtual screen, the cursor is positioned at the respective edge of the virtual screen.

The internal variable data pointer (DPTR0) is updated to the video memory address value corresponding to the coordinates of the cursor position.

LPNR Command

Command Code 1AH

0	0	0	1	1	0	1	0

Output Data

Vertical position (lower)						
0	0	0	0	0	(upper)	
Horizontal position (lower)						
0	0	0	0	0	0	(upper)

The light pen detection coordinates are determined and the light pen detection status is reset to 0.

Virtual screen coordinates are specified by first designating the Y (line) position and then the X (column) position.

The internal variable data pointer (DPTR0) is updated to the video memory address value corresponding to the light pen detection coordinates.

VIDEO MEMORY OPERATION COMMANDS

DPLD Command

Command Code 8E/8FH

1	0	0	0	1	1	1	N

Parameters

VRAM address (lower)					
(intermediate)					
0	0	0	0	0	(upper)

The address data entered by using the parameter is stored in the specified internal variable data pointer (DPTR0 or DPTR1)

N	Data Pointer
0	Store in DPTR0
1	Store in DPTR1

The data pointer value is used for address specification or update in later VRAM access.

The 19-bit address parameter can be used to access 512K-byte video memory space. If the DPTR1 value is negative, input the complement.

In the commands listed in table 4, the address update mode is specified in the command code MOD field, and the data pointer value can be updated each time a VRAM access is made.

If the coordinates on the virtual screen can be obtained by cursor position specification and light pen input position detection, the data pointer (DPTR0) is updated to the corresponding video memory address value.

Table 4. Data Pointer Update

MOD	Data Pointer Update	RDAT, WDAT	BLKTOT, BLKTIN
00	Data pointer is not changed.	Enabled	Disabled
01	ATROFF value is added; then the data pointer is updated.	Enabled	Enabled
10	PITCH value is added; then the data pointer is updated.	Enabled	Enabled
11	DPTR1 value is added; then the data pointer is updated.	Enabled	Enabled

DPRD Command

Command Code 8AH

1	0	0	0	1	0	1	0

Output Data

VRAM address (lower)					
(intermediate)					
0	0	0	0	0	(upper)

The data pointer (DPTR0) value is determined.

MASK Command

Command Code 89H

1	0	0	0	1	0	0	1

Parameters

Mask data

The mask data entered via the parameter is stored in the internal variable mask register (MSKR).

The mask register value is used for write data mask processing in later VRAM access. When the mask bit value is 0, the VRAM contents are held; when 1, write data is stored.

In mask processing, the mask register value is determined before a VRAM write operation is initiated.

The video memory contents at the transfer destination address are read and ANDed with the inverted mask data value, and a mask is set. In addition, the write data to be stored in video memory and the mask data value are ANDed together, and a mask is set. The results are ORed together, and then written into video memory.

RDAT Command

Command Code 90/91/92/93H

1	0	0	1	0	0	MOD

Output Data

Read data
•
•
•
Read data

The video memory contents are read from the address specified in the data pointer (DPTR0), and the data is transferred to the host processor.

If the host processor receives the memory data, the data pointer (DPTR0) contents are updated according to MOD specification (table 4), and the video memory contents at the next address are read and transferred.

The memory contents are read until another command is entered.

WDAT Command

Command Code 94/95/96/97H

1	0	0	1	0	1	MOD

Input Data

Write data
•
•
•
Write data

With the WDAT (Write VRAM Data) command, mask processing is performed for data input by the host processor according to the mask register value. Then, the data is written into video memory at the address specified by the data pointer (DPTR0).

After the data is written, the data pointer (DPTR0) contents are updated according to MOD specification (table 4) to the next video memory address.

If the host processor inputs data consecutively, the data write into video memory and data pointer update are repeated until another command is entered.

BLKTOT Command

Command Code 99/9A/9BH

1	0	0	1	1	0	MOD

DMA Transfer Output Data

Read data
•
•
•
Read data

The video memory contents are read from the address specified in the data pointer (DPTR0) and stored in the output data buffer. A DMA transfer request signal ($\overline{\text{DMARQ}}$) is then generated to prompt the DMA controller to receive the read data. The DMA acknowledge signal ($\overline{\text{DMAAK}}$, $\overline{\text{RD}}$) is used to output the data buffer contents to the data bus. If the DMA controller receives the data and the buffer is not empty, the DMA transfer request generation is continued.

If the buffer is empty, the data pointer (DPTR0) value is updated according to MOD specification (table 4), and the video memory contents at the next address are read and stored in the output data buffer. Therefore, the address of the data read by the DMA controller does not correspond to the data pointer value.

If the output data buffer is empty, the memory read and the data pointer update are repeated until the host processor inputs another command based on the DMA controller terminal count.

BLKTIN Command

Command Code 9D/9E/9FH

1	0	0	1	1	1	MOD

DMA Transfer Input Data

Write data
•
•
•
Write data

DMA transfer request signal ($\overline{DMARQ}$) is generated to prompt the DMA controller to transfer write data. Data input together with the DMA acknowledge signal ($\overline{DMAAK}$, $\overline{WR}$) is written into video memory.

Mask processing is performed for data input by executing the DMA transfer according to the mask register value; then the data is written into video memory at the address specified in the data pointer (DPTR0).

After the data is written, the data pointer (DPTR0) contents are updated according to MOD specification (table 4) to the next video memory address.

If the DMA controller inputs data consecutively, the data write into video memory and the update of the data pointer are repeated until the host processor inputs another command based on the DMA controller terminal count.

EXIT Command

Command Code 88H

1	0	0	0	1	0	0	0

Command processing during parameter acceptance is stopped and a command wait state is initiated.

Video memory operation command processing during data transfer is stopped and a command wait state is initiated.

If parameter acceptance is terminated and processing is started, data or any command other than the video memory operation commands cannot be terminated by issuing the EXIT command.

SPRITE CONTROL COMMANDS

SPRON Command

Command Code 82H

1	0	0	0	0	0	1	0

Parameters

SAB (lower)							
0	0	0	0	0	(upper)		
HSPN					ESP	SPMG	SPGR

If the display controller has been enabled by the DSPON command, sprite display is initiated.

The sprite status (SC) in the status data is reset and interrupt signal generation from the sprite controller is enabled or disabled according to ESP specification.

The sprite attribute table and sprite pattern area base address (SAB), sprite magnification (SPMG), and sprite grouping function (SPGR) are set in the sprite controller.

If the command is input during sprite display, the sprite controller operation parameter is changed.

- **HSPN** (Horizontal Sprite Number)

  This parameter specifies the maximum number of sprite images that can be displayed on a single horizontal line.

- **SPMG** (Sprite Magnify)

  Sprite magnification display is specified. When SPMG is set to 1, sprite display data is magnified two-fold in the vertical direction display.

- **SPGR** (Sprite Grouping)

  The grouping function in sprite detection is specified. When SPGR is set to 1, collision detection between different groups is enabled.

- **ESP** (Enable Sprite Interrupt)

  INT signal from the sprite controller is specified. When ESP is set to 1, an INT signal is generated at the INT pin when sprite collision is detected or the maximum number of sprite images is exceeded.

SPROF Command

Command Code 83H

1	0	0	0	0	0	1	1

Sprite controller operation is disabled and sprite display is terminated.

SPRRD Command

Command Code 80H

1	0	0	0	0	0	0	0

Parameters

SPN	ATN

Output Data

Read data 1
•
•
•
Read data n

The sprite attribute table contents are read from the address corresponding to the SPN (sprite number) and ATN (attribute number) parameters, and the data is transferred to the host processor.

ATN	Attribute
0	YP lower
1	YSIZE, SPSW, YP upper
2	XP lower
3	XSIZE, SPDM, XP upper
4	SPDA lower
5	SPDA upper
6	SCF (color)
7	Not used

If the host processor receives the attribute data, the attribute number is incremented and the next attribute data is read and transferred. When attribute number 7 is read, the sprite number is also updated so that the next sprite vertical position (YP lower) can be read.

The attribute data read and the attribute and sprite number update are repeated until another command is input.

SPWR Command

Command Code 84H

1	0	0	0	0	1	0	0

Parameters

SPN	ATN

Input Data

Store data 1
•
•
•
Store data n

Data input by using the parameters is stored in the sprite attribute table.

ATN	Attribute
0	YP lower
1	YSIZE, SPSW, YP upper
2	XP lower
3	XSIZE, SPDM, XP upper
4	SPDA lower
5	SPDA upper
6	SCF (color)
7	Not used

The input data following the second parameter is written into video memory from the address corresponding to the first parameter SPN (sprite number) and ATN (attribute number).

Each time one byte of data is stored, the attribute number is incremented so that the next attribute number can be specified. When attribute number 7 is stored, the sprite number is also updated so that the next sprite vertical position (YP lower) can be specified.

If the host processor inputs data consecutively, the attribute number is incremented from 0 through 7 for each sprite number, which advances in increments of 1.

SPRSW Command

Command Code 85H

1	0	0	0	0	1	0	1

Parameters

SPN	0	SPSW	0

This command specifies the sprite display on or off by setting the sprite attribute SPSW bit.

The sprite number is specified in the SPN parameter. If the SPSW parameter is set to 1, sprite display is turned on; if cleared to 0, sprite display is turned off. Thus, display on or off for each sprite can be specified as desired.

SPROV Command

Command Code 81H

1	0	0	0	0	0	0	1

Output Parameters

0	SO	C	OVS

The sprite controller operation status is determined and the sprite status bit in the status data (SC) is reset to 0.

The sprite controlled status is defined by parameters SO, OVS, and C.

(1) SO indicates whether the maximum number of sprite images that can be displayed on a single horizontal line (HSPN specification) has been exceeded.

(2) OVS specifies the first excessive sprite number.

(3) C indicates the detection of sprite collision.

STATUS

The μPD72022 sends the display hardware operation status and command processing status information to the host processor via the status output port.

The status data format and the bit contents viewed from the host are explained below.

7	6	5	4	3	2	1	0
LP	VB	SC	ER	—	BUSY	OBF	IBF

Input Buffer Full

IBF (bit 0) indicates that data is stored in the internal input data buffer during command/parameter input from the host processor. It is set on the rising edge of the $\overline{WR}$ strobe signal when the host processor writes commands/parameters. It is reset when the input data buffer contents are read by μPD72022 internal processing.

The host processor should check that the flag is reset before inputting the next command/parameter. If a command/parameter is input when the flag is set, the μPD72022 drives the READY signal low, forcing the host to wait.

Output Buffer Full

OBF (bit 1) indicates that the μPD72022 has data stored in the output data buffer. It is set when a write is made to the output data buffer during internal processing. It is reset on the rising edge of the $\overline{RD}$ strobe signal when the host reads the output data buffer contents through the parameter output port.

The host processor should check that the flag is set before reading data from the parameter output port. If data is read when the flag is set, the μPD72022 drives the READY signal low, forcing the host to wait. The flag is reset when a command is input.

Busy

The BUSY flag (bit 2) indicates that the μPD72022 is performing command processing. It is set under the same conditions as IBF and reset when the execution of all commands stored in the internal FIFO buffer has been completed.

In command processing of SPRRD, SPRWR, BLKTIN, BLKTOT, WDAT, or RDAT, however, BUSY is reset when the FIFO buffer is empty after the completion of processing of successive input commands. Therefore, BUSY is always set when any of these six commands is being executed.

Error

ER (bit 4) indicates that an error occurred during command processing. It is set when an abnormal state is encountered; for example, when parameters required for command execution are not entered, or the value of an entered parameter is not proper.

When an error occurs, μPD72022 stops command processing. To recover, issue the EXIT command, followed by the desired command. ER is reset when the EXIT command is executed.

Specific error causes are as follows.

(1) Parameter is entered when command code is not entered.

(2) Command/parameter is entered from any port other than the command or parameter input port.

(3) Any code other than a command code is entered from the command port.

(4) The number of parameters is too large. Up to a given number of parameters are assumed to be valid and processed. When excessive parameters are entered, ER is set and the excessive parameters are not processed.

(5) The number of parameters is too small. All the entered parameters are assumed to be valid and processed.

  (a) When a command (except EXIT) is entered following the parameters, ER is set and command processing starts

  (b) When an EXIT command is entered following the parameters, it is assumed that termination of the immediately preceding command entered is specified. ER is not set and command entry is awaited.

  (c) When other than a command or parameter entry follows the parameters, an error results. ER is set and command entry is awaited.

(6) LPNR command is made on any area other than the active screen area specified by the ACTSCR command.

Sprite Control

The SC flag (bit 5) indicates occurrence of sprite over or sprite collision state during sprite display operation. It is updated each time one screen display is terminated (vertical blank).

(1) Sprite Over. The SC flag is set when the number of sprite images existing on a single horizontal line exceeds the HSPN setup value. The first sprite number exceeding the setup value can be read by command (SPROV) specification.

(2) Sprite Collision. The SC flag is set when dot overlap of two or more sprite images occurs.

Vertical Blank

VB (bit 6) indicates vertical blanking time (BBR, BBL, or VS time). It can be used for the host processor to synchronize with display operations.

Light Pen Detect

LP (bit 7) indicates that an address is detected by using the light pen signal. It is set when the address is detected and reset when the LPNR command is issued.

CONTROL

After initialization (figure 19), the μPD72022 executes control according to the sequence shown in figure 20.

In figure 20, a check is made to ensure that IBF (bit 0) of the μPD72022 status data format is cleared to 0; then the command/parameter is written.

If the command is a data read or write command, then data is read or written.

The sequence to check that the IBF bit is cleared to 0 can be omitted by using the READY signals; however, this does not apply to read commands (RDAT, BLKTOT, SPRRD, DPRD, LPNR, SPROV).

Figure 19. μPD72022 Initialization

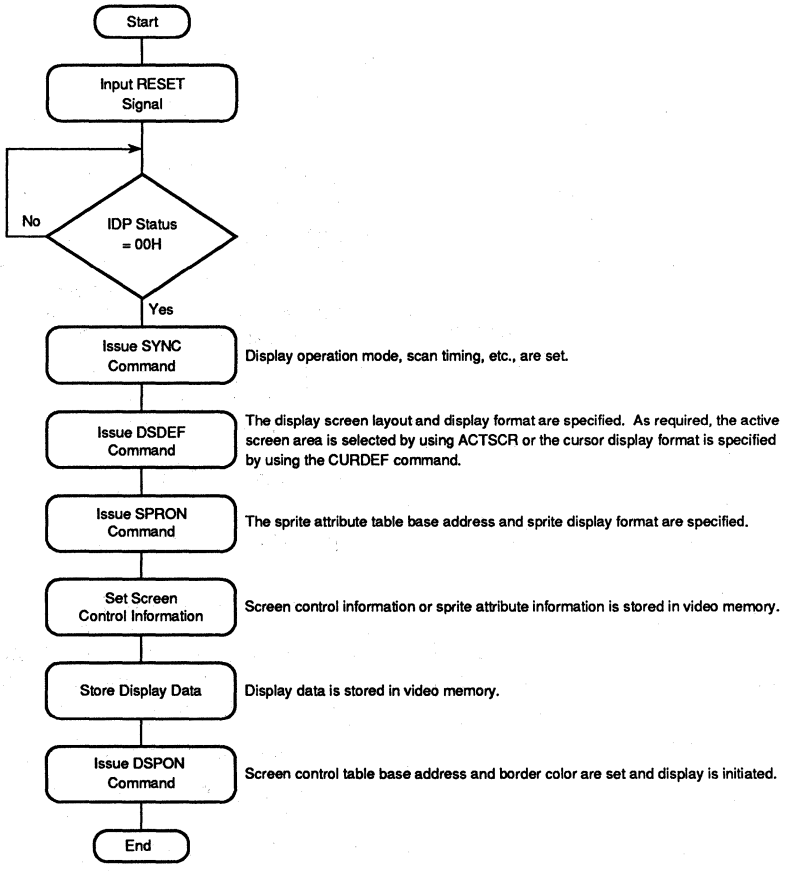
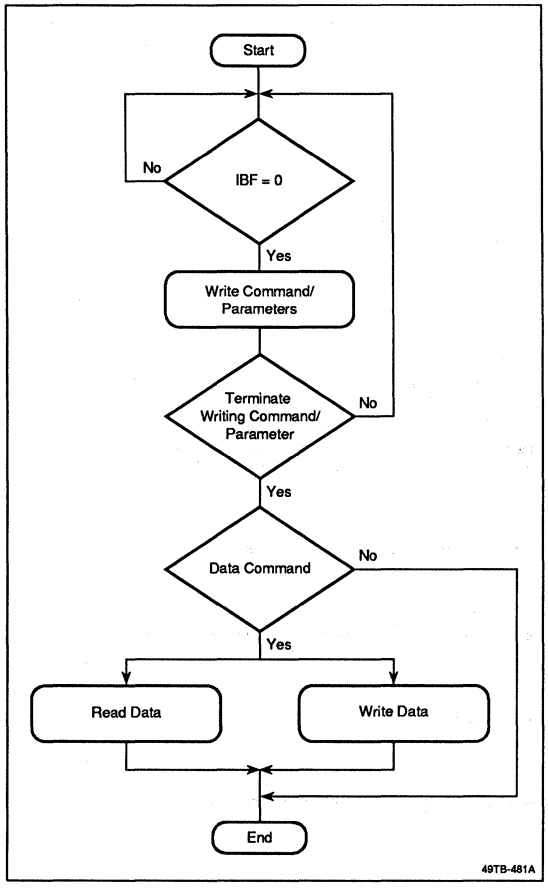


Figure 20 μPD72022 Basic Control Flow



DISPLAY

Static Picture Display

The μPD72022 IDP has three static picture display modes: text, semigraphics, and graphics.

Text Mode. Video memory data is recognized as character code and attribute data. Character patterns from the character generator specified by character code are displayed. Color or format qualification is specified by attribute data paired with character code. See figure 21.

Semigraphics Mode. Video memory data is recognized as pattern code. Pattern data (format and color) in the pattern data area specified by pattern code is displayed. Two modes are available according to how pattern data is stored. See figures 22 and 23.

Graphics Mode. Video memory data is recognized and displayed as color patterns corresponding directly to the display screen. See figure 24.

Sprite Image Display

The μPD72022 IDP can control a maximum of 32 sprite images. Collision between sprite images can be detected.

Any desired color pattern (sprite) is displayed at any desired position of the screen based on information in the video memory sprite attribute table. Sprite control commands can change the sprite size, color, display address, display position, etc. See figure 25.

Screen Split Display

The μPD72022 IPD can split the display screen into rectangular windows and display any area extracted from video memory. Each display area is independently controlled by the μPD72022. See figure 26.

Figure 21. Data Flow in Text Mode

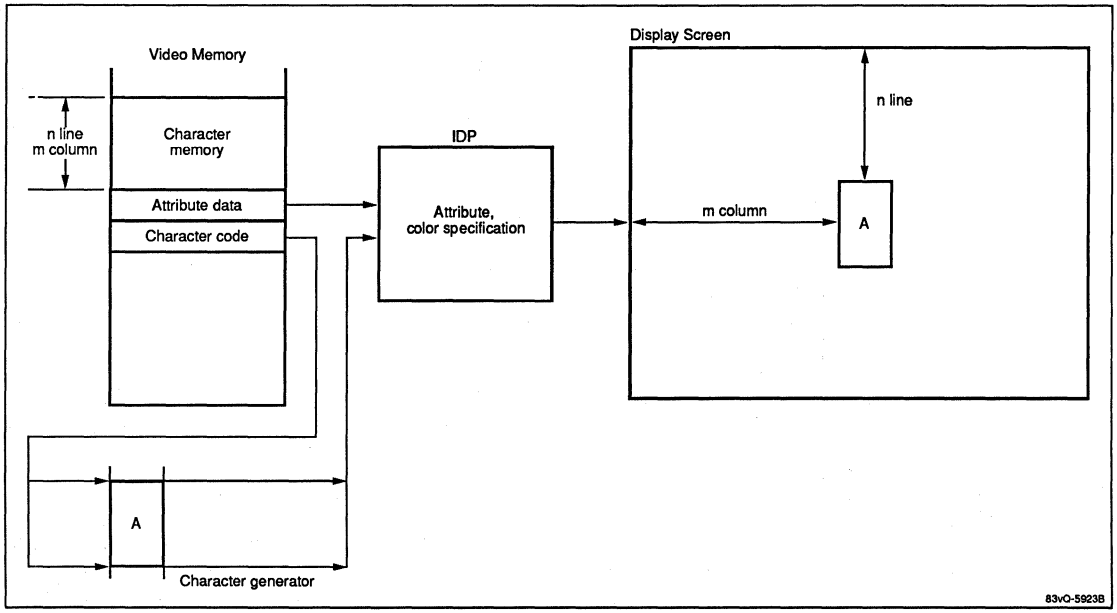


Figure 22. Data Flow in Semigraphics Mode 0

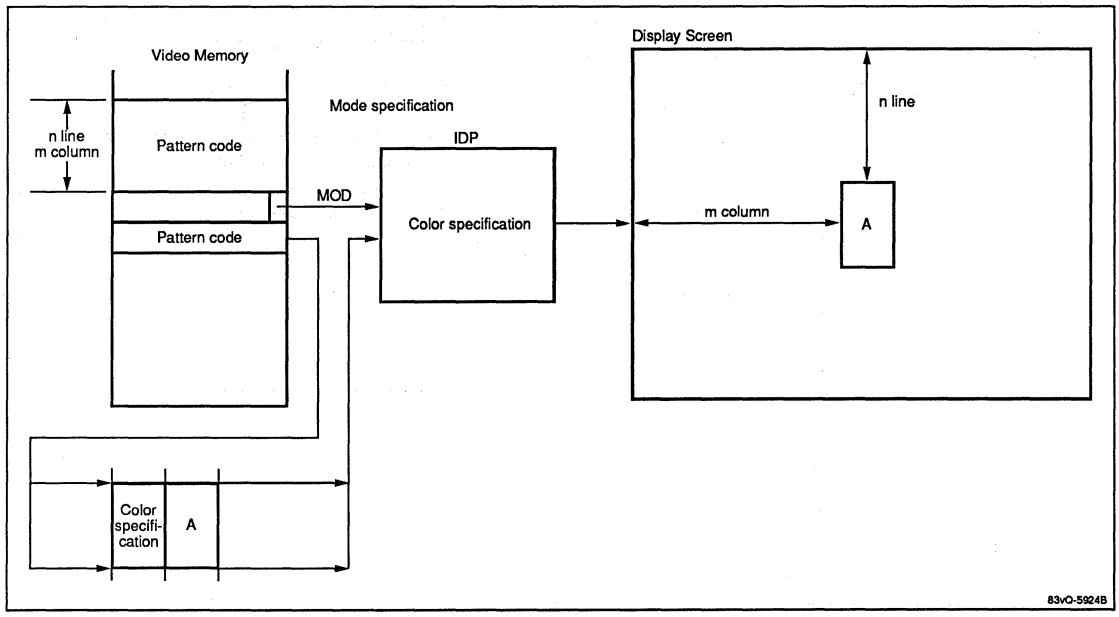


Figure 23. Data Flow in Semigraphics Mode 1

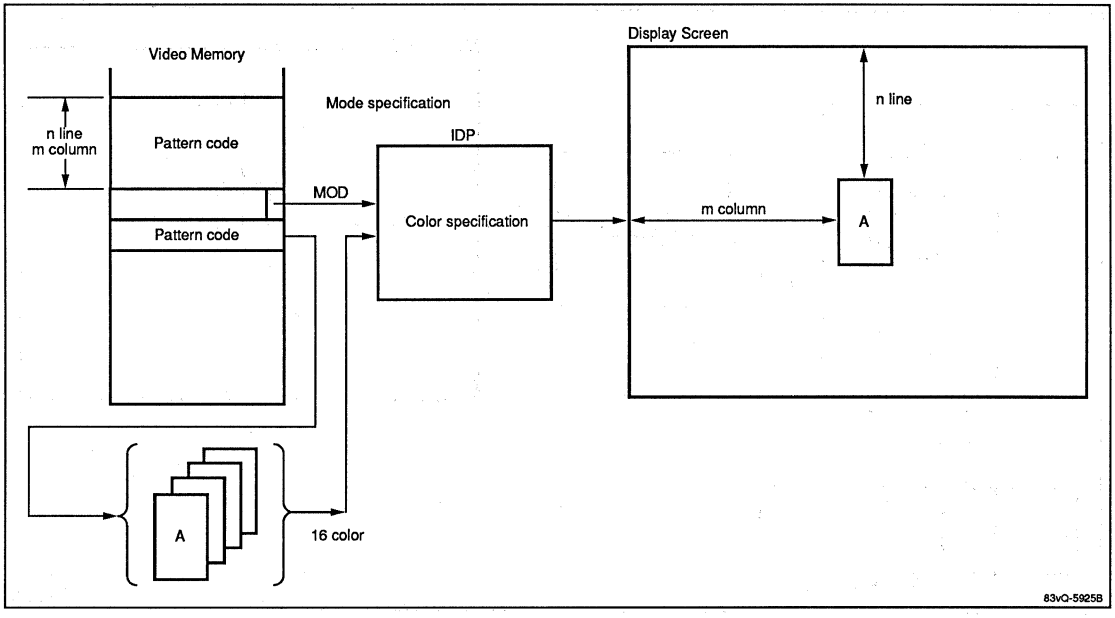


Figure 24. Data Flow in Graphics Mode

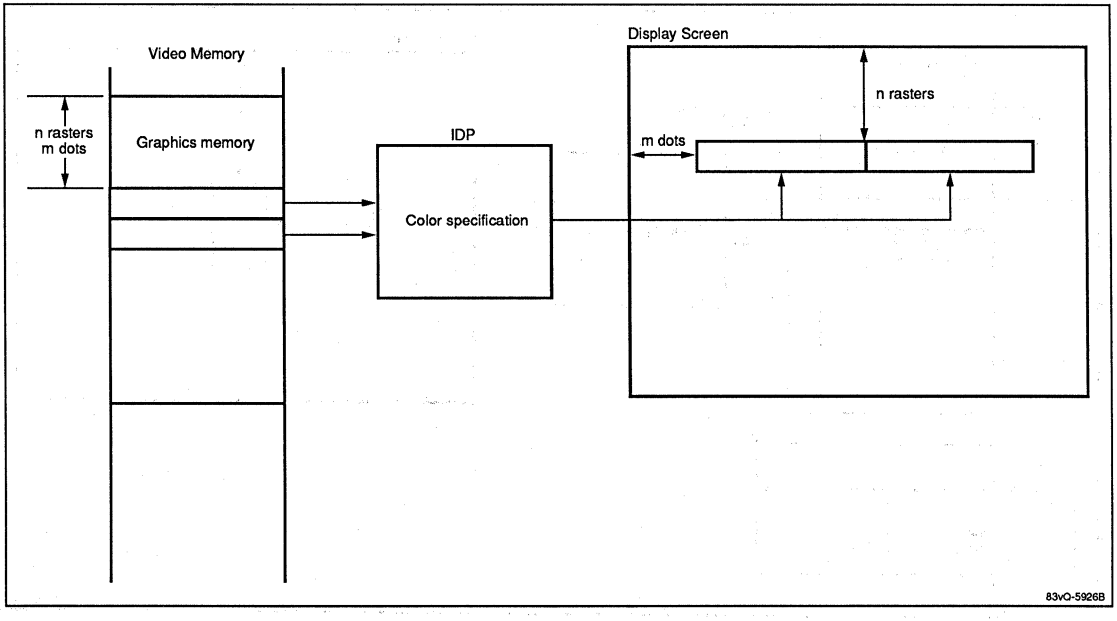


Figure 25. Data Flow During Sprite Image Display

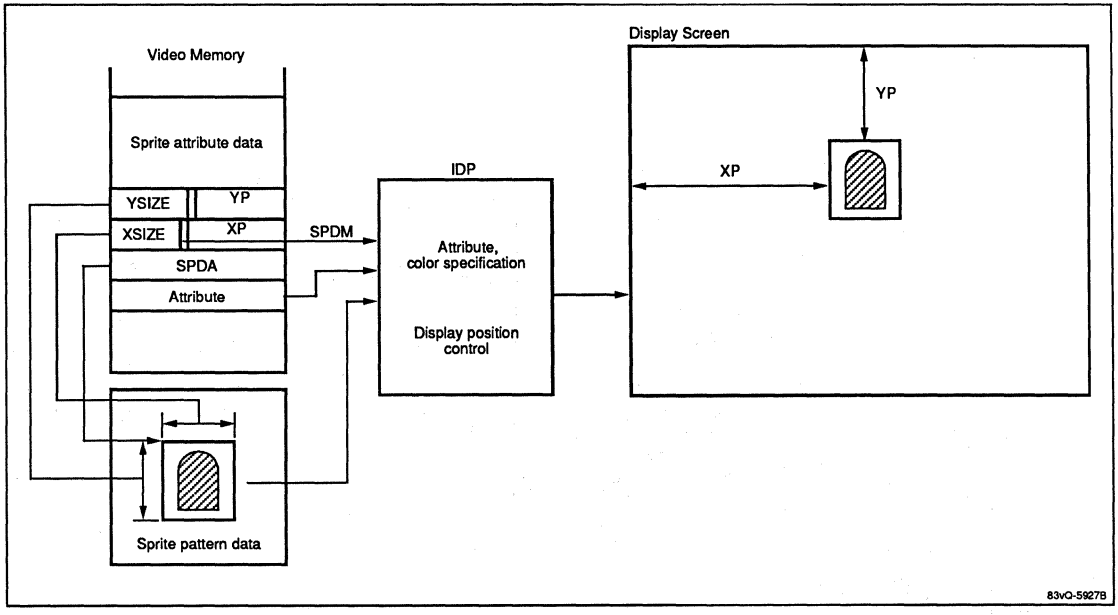
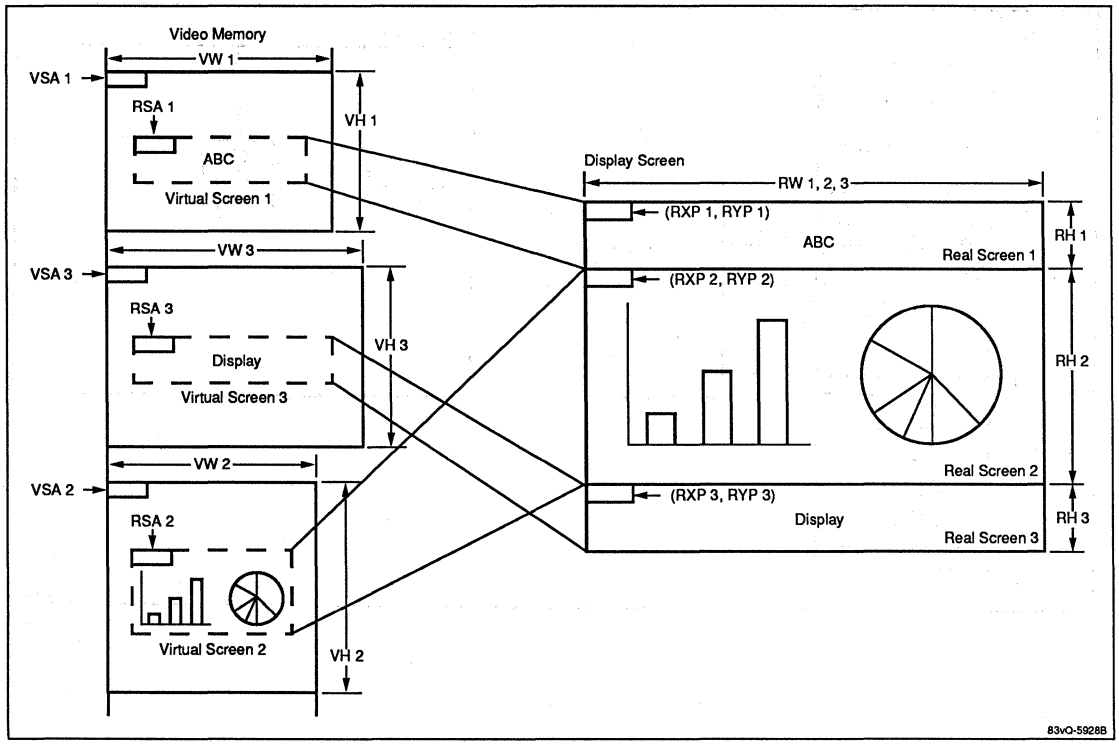


Figure 26. Example of Screen Split Display



Scan Mode Specification

The μPD72022 IDP enables specification of four scan modes by using SYNC command parameter RM before video signal generation. See figure 27.

Noninterlace Mode. The raster address is incremented for each horizontal scan. The display data address is updated every specified number of rasters.

In graphics mode, the display data address is updated each horizontal scan.

Interlace Mode. Odd and even fields are displayed alternately. In the odd field, the raster address starts at 0; in the even field, it starts at 1. The raster address is incremented by two for each horizontal scan.

In graphics mode, the display address is updated so that display data in the opposite field is skipped.

In interlace mode, the MRA value must be specified so that the numbeer of rasters is even.

To use the interlace mode, a value appropriate for the 16-kHz monitor must be set in the raster parameter and the interlace synchronizing signal must be input from an external source.

Vertical Magnification Mode. The raster address is incremented every two horizontal scans. The display data address is updated every specified number of rasters.

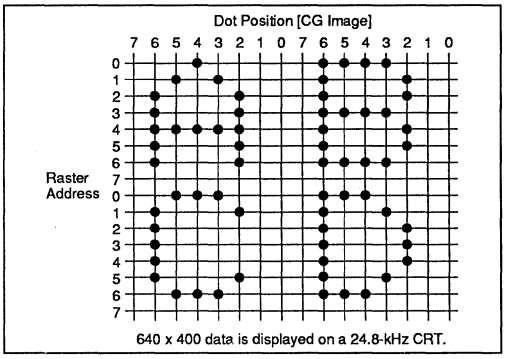
In graphics mode, the display data address is updated every two horizontal scans.

Normal Mode. The raster address is incremented each horizontal scan. The display data address is updated every specified number of rasters.

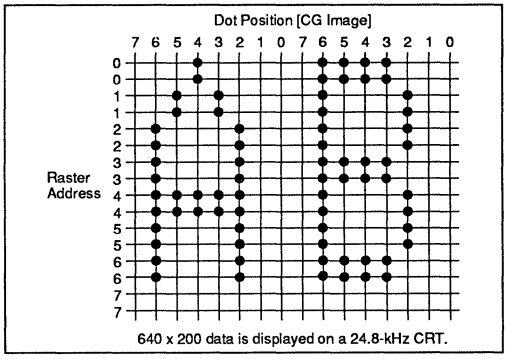
In graphics mode, the display data address is updated each horizontal scan.

Figure 27. Scan Modes

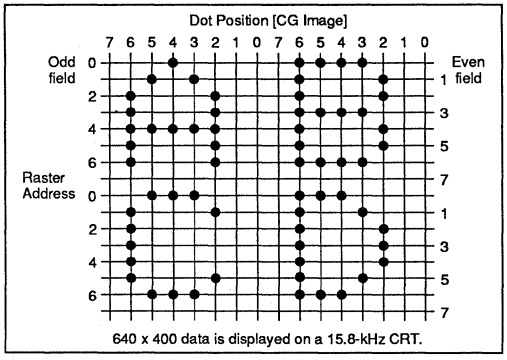
A. Noninterlace Mode



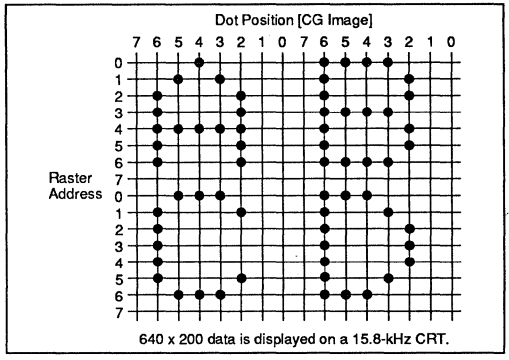
C. Vertical Magnification Mode



B. Interlace Mode



D. Normal Mode



49NR-475B

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μPD72120
Advanced Graphics Display Controller

Description

The μPD72120 Advanced Graphics Display Controller (AGDC) displays characters and graphics on a raster scan device from commands and parameters received from a host processor or CPU. Features of the AGDC include high-speed graphics drawing capabilities, video timing signal generation, large capacity display memory control (including video RAMs), and a versatile CPU interface. These features allow the AGDC to control graphics drawing and display of bit-mapped systems.

Features

- High-speed graphics drawing functions
  - Graphics drawing: dot, straight line, rectangle, circle, arc, sector, segment, ellipse, ellipse arc, ellipse sector, and ellipse segment
  - Maximum drawing speed
    500 ns/pixel (8 MHz, pixel mode)
    500 ns/dot (8 MHz, plane mode)
  - Area filling (high-speed processing in word units): triangle, trapezoid, circle, ellipse, and rectangle
  - Painting: filling of any arbitrary enclosed area (bit boundary retrieval)
  - Data transfers in display memory: multiplane transfers; data transformation (90°/180°/270° rotation and reversal); multiwindow transfers; maximum transfer speed of 500 ns/word
  - Image processing: slant, arbitrary angle rotation, 16/N enlargement, and N/16 shrinkage (N any integer from 1 to16)
  - Position specification by X-Y coordinates
  - Logical operations between planes
- Video timing signal generation
  - High-speed processing by two system clocks: display (for video sync signal generation) and graphics drawing clocks
  - External synchronization capability
- Large-capacity display memory
  - Display memory bus interface: 24-bit address and 16-bit data bus for addressing up to 16M words, 16 bits/word
  - Video RAM (VRAM) control
  - Display memory bus arbitration
- Host processor (CPU) interface
  - System bus interface: 20-bit address bus, 8- or 16-bit data bus
  - Data transfer with external DMA controller: from system memory to display memory (PUT); from display memory to system memory (GET)
  - High-speed pipeline processing with preprocessor before drawing processor
  - CPU memory or I/O mapping of internal registers and display memory for efficient system interface
- 8-MHz system clock
- CMOS technology
- Single +5-volt power supply
- Packages: 84-pin PLCC, 94-pin plastic miniflat

Ordering Information

Part No	Package
μPD72120L	84-pin PLCC
μPD72120GJ-5BG	94-pin plastic miniflat

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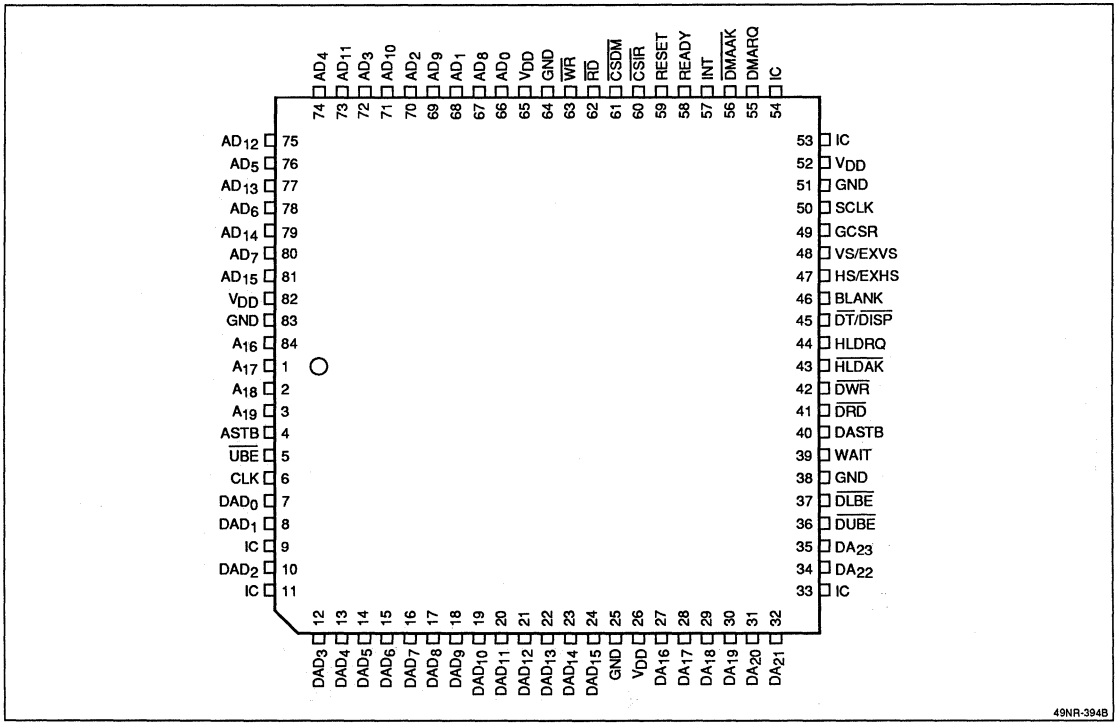
50068

Pin Identification

Symbol	I/O	Signal Function
Clock Pins		
CLK	In	Clock supplied to circuits other than the sync signal generator and display processor. The drawing processor and preprocessor speed depend on this clock frequency.
SCLK	In	Clock supplied to the sync signal generator and the display processor. This clock frequency is determined by the CRT timing requirements: horizontal sync frequency, number of dots per line, etc.
System Bus Control Pins		
AD_0-AD_{15}	I/O	I/O bus to the CPU consisting of multiplexed 16-bit address and a bidirectional data bus.
A_{16}-A_{19}	In	Upper four address bits of the 20-bit address.
ASTB	In	Latches the address on A_{16}-A_{19} and AD_0-AD_{15} on the falling edge.
$\overline{UBE}$	In	Together with AD_0, defines the data access format as shown below. $\overline{UBE}$ should be tied high when connected to an 8-bit CPU. AD_0 $\overline{UBE}$ Data Access Format 0 0 Even-address word 0 1 Even-address byte 1 0 Odd-address byte 1 1 Odd-address byte
$\overline{RD}$	In	Performs a read of data from the AGDC by the host CPU.
$\overline{WR}$	In	Performs a write of data to the AGDC from the host CPU.
$\overline{CSIR}$	In	Enables reading/writing of the AGDC internal registers by the host CPU. The register is selected by the address input on AD_0-AD_7.
$\overline{CSDM}$	In	Enables reading/writing of display memory through the AGDC by the host CPU. The display memory address is generated by the address input on A_{16}-A_{19} and AD_0-AD_{15} and by the bank register.
READY	Out	Activated by the data access request ($\overline{RD}$/$\overline{WR}$) for the AGDC. During the access, the signal may be low. RESET will set the READY line high.
INT	Out	Signals an interrupt from the AGDC.
DMARQ	Out	Indicates a request for data transfer (PUT/GET) to an external DMA controller. DMARQ will be low after RESET.
$\overline{DMAAK}$	In	Acknowledgment of DMA request to the AGDC by the DMA controller.
RESET	In	Initializes operation of the AGDC. The internal parameter register is not cleared by RESET (it is initialized by setting data).
Display Memory Control Pins		
DAD_0-DAD_{15}	I/O	I/O pins for display memory; 16-bit address multiplexed with data.
DA_{16}-DA_{23}	Out	Upper 8 bits of display memory address (the lower 16 bits of the 24-bit address are output on DAD_0-DAD_{15}).
DASTB	Out	Indicates that a display memory address is present on the falling edge.
$\overline{DUBE}$, $\overline{DLBE}$	Out	Defines the data format for accessing the display. RESET sets both pins low. $\overline{DUBE}$ $\overline{DLBE}$ Data Access Format AGDC 0 0 Word 16-bit CPU 0 0 Word 8/16-bit CPU 0 1 High (odd) byte 8/16-bit CPU 1 0 Low (even) byte 8-bit CPU 1 1 High (odd) byte
$\overline{DRD}$	Out	Controls reading of the display memory by the AGDC. Set high by RESET.
$\overline{DWR}$	Out	Controls writing to the display memory by the AGDC. Set high by RESET.
HLDRQ	In	Requests control of the display memory bus by an external device to transfer display data.
$\overline{HLDAK}$	Out	Indicates that the AGDC memory bus (DAD_0-DAD_{15} and DA_{16}-DA_{23} is in high-impedance state so that an external device can have access to the display memory bus. Set high by RESET.
Video Timing Signal Related Pins		
VS/EXVS	I/O	When the AGDC operates as the master, VS is the vertical sync signal output. When the AGDC operates as a slave, the EXVS input initializes the internal vertical sync signal on the rising edge.
HS/EXHS	I/O	When the AGDC operates as the master, HS is the horizontal sync signal output. When the AGDC operates as a slave, EXHS initializes the internal horizontal sync signal on the rising edge.
Display Signal Related Pins		
BLANK	Out	Used to blank the display.
$\overline{DT/DISP}$	Out	Set to DT in the DT mode (when using VRAMs) and specifies the data transfer. In the cycle steal mode (VRAMs not used), indicates the display cycle.
GCSR	Out	Specifies the display of the graphics cursor
GWAIT	Out	Graphics wait signal
Other Pins		
V_{DD}		+5-volt power supply
GND		Ground
IC		Internally connected; leave unconnected

Pin Configurations

84-Pin PLCC



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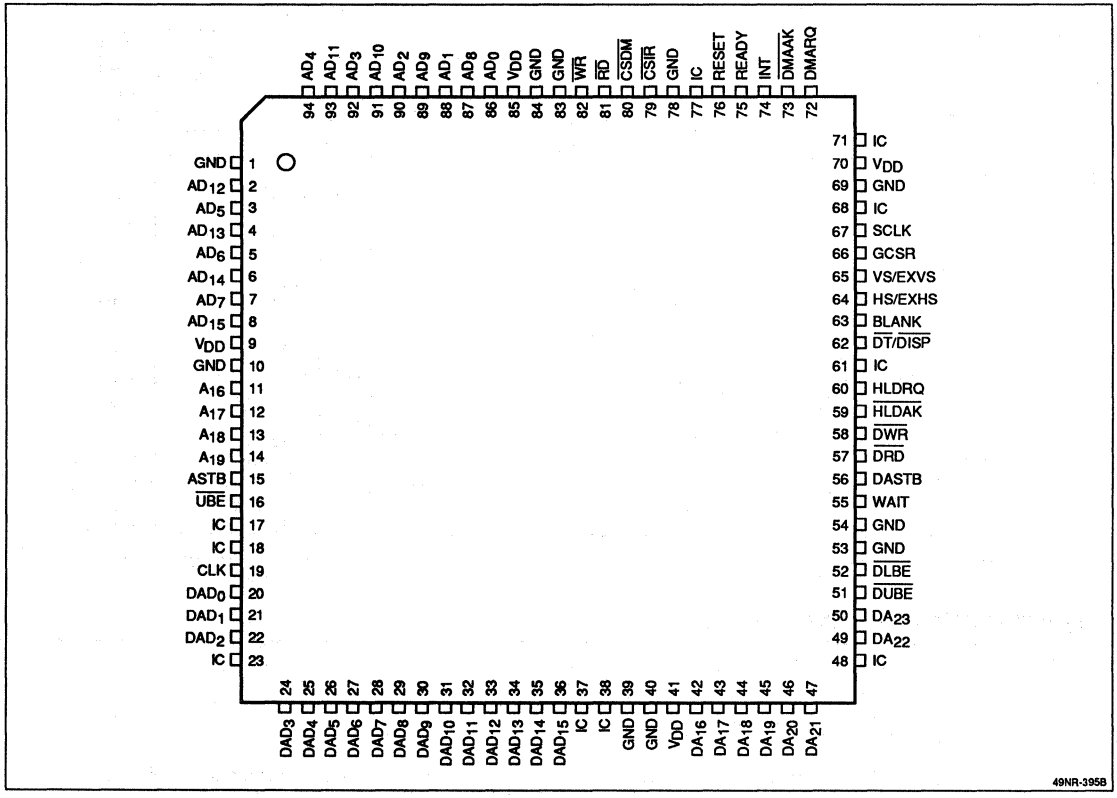
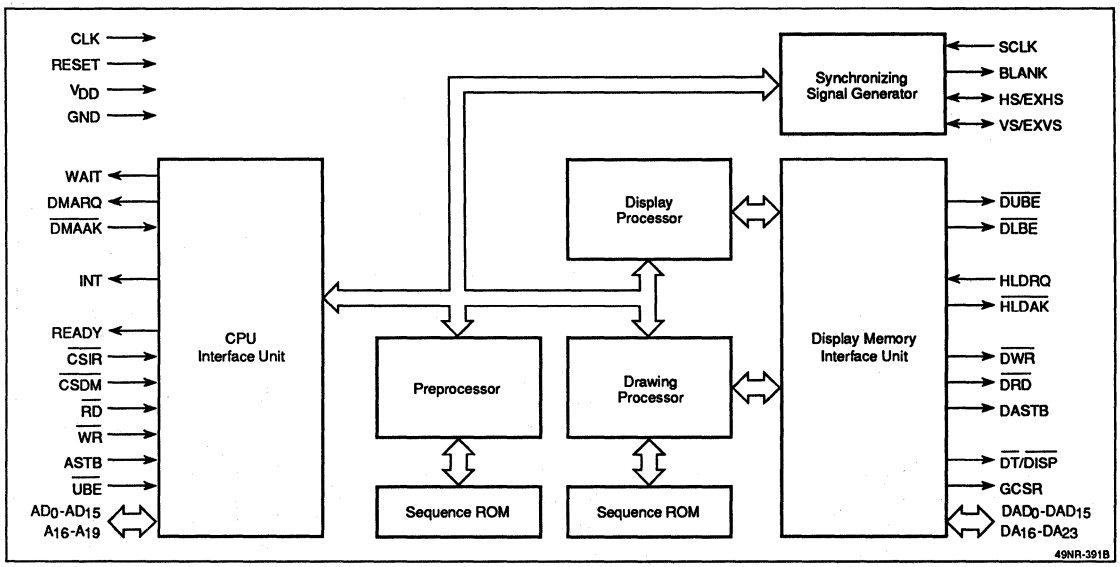
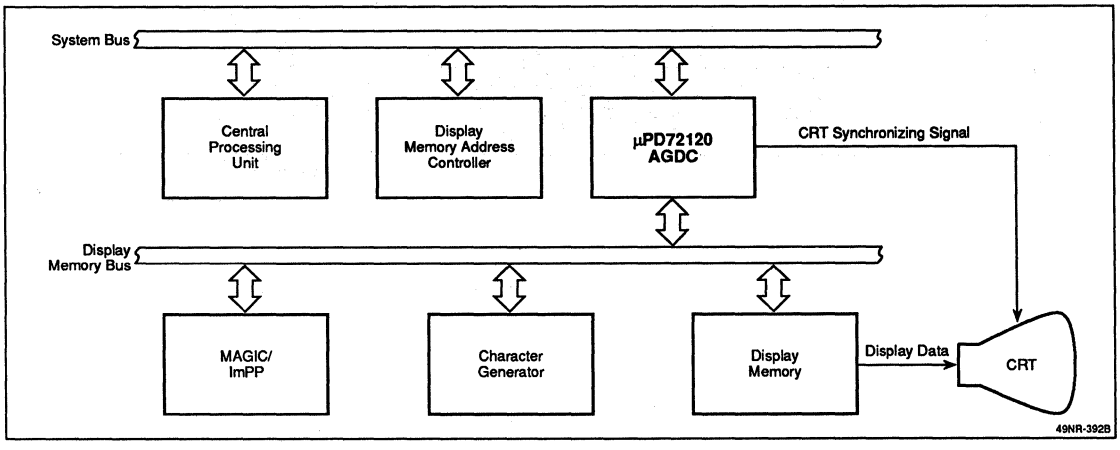
94-Pin Plastic QFP



μPD72120 Block Diagram



System Configuration Example



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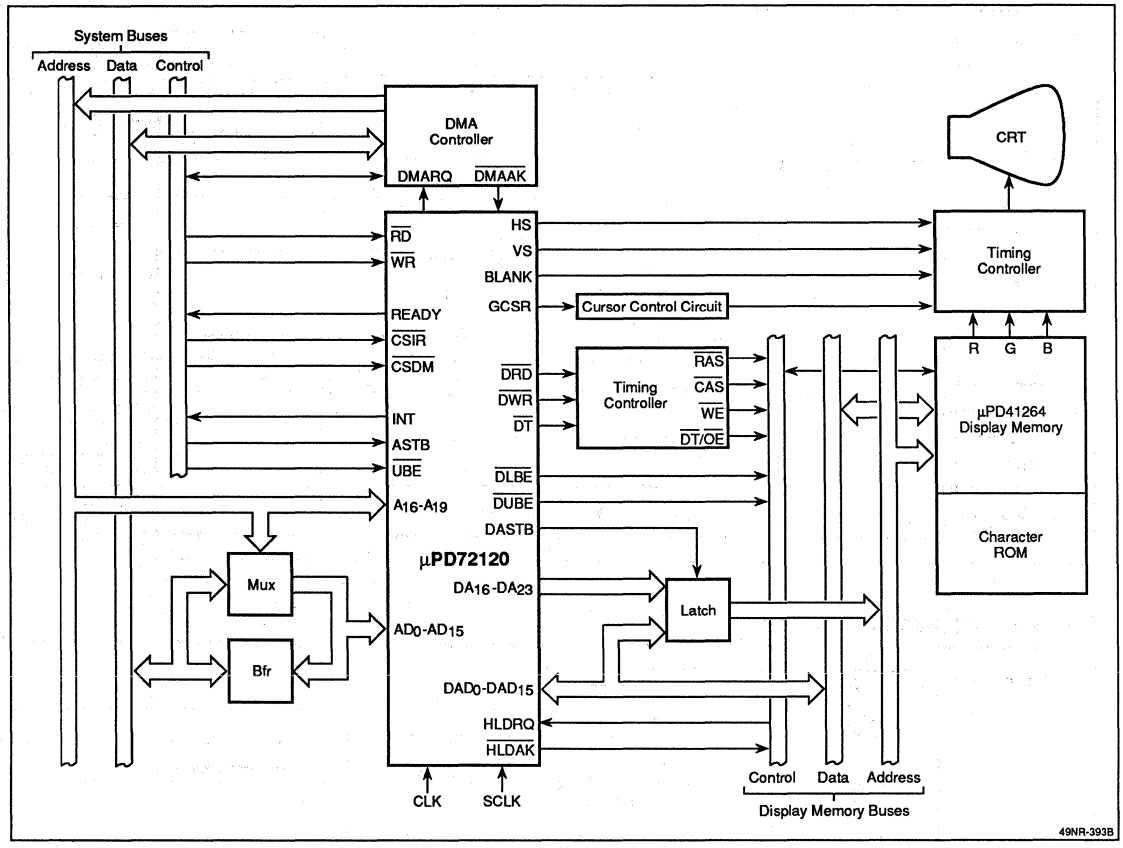
General Application Diagram



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to +7.0 V
Output voltage, V_O	−0.5 to +7.0 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Power dissipation, P_D	1.1 W

Capacitance

T_A = +25°C; V_{DD} = GND = 0 V

Parameter	Symbol	Min	Max	Unit	Condition
Input	C_I		10	pF	f = 1 MHz; unmeasured pins returned to 0 V
Output	C_O		20	pF	
Input/ output	$C_{I/O}$		20	pF	
Clock input	C_C		20	pF	

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Condition
Low-level input voltage	V_{IL}	−0.5	0.8	V	Except CLK or SCLK
		−0.5	0.6	V	CLK, SCLK
High-level input voltage	V_{IH}	2.2	V_{DD} + 0.5	V	Except CLK or SCLK
		3.5	V_{DD} + 1.0	V	CLK, SCLK
Low-level output voltage	V_{OL}		0.45	V	I_{OL} = 2.2 mA
High-level output voltage	V_{OH}	2.4		V	I_{OH} = −400 μA
Low-level input leakage current	I_{LIL}		−10	μA	V_I = 0 V
High-level input leakage cur ent	I_{LIH}		10	μA	V_I = V_{DD}
Low-level output leakage current	I_{LOL}		−10	μA	V_O = 0 V
High-level output leakage current	I_{LOH}		10	μA	V_O = V_{DD}
Supply current	I_{DD}		200	mA	

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AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%; see figure 1

Parameter		Figure	Symbol	Min	Max	Unit	Condition
Clock (CLK, SCLK)							
Clock period	CLK	2	t_{CYK}	125	600	ns	
	SCLK	2	t_{CYSK}	125	600	ns	$t_{CYK} \leq t_{CYSK}$
High-level clock width	CLK	2	t_{WKH}	52		ns	
	SCLK	2	t_{WSKH}	52		ns	
Low-level clock width	CLK	2	t_{WKL}	52		ns	
	SCLK	2	t_{WSKL}	52		ns	
Clock rise time	CLK	2	t_{KR}		15	ns	
	SCLK	2	t_{SKR}		15	ns	
Clock fall time	CLK	2	t_{KF}		15	ns	
	SCLK	2	t_{SKF}		15	ns	
Reset, Interrupt							
Reset pulse width		3	t_{RST}	5		t_{CYSK}	
CLK ↑ to INT ↑ delay time		3	t_{DKI}		50	ns	C_L = 50 pF
$\overline{RD}$ ↓ to INT↓ delay time		3	t_{DRI}		3 t_{CYK} + 50	ns	STATUS read
HLDRQ, $\overline{HLDAK}$							
CLK ↑ to $\overline{HLDAK}$ delay time		4	t_{DKHA}		50	ns	C_L = 50 pF
HLDRQ setup time to CLK ↑		4	t_{SKHQ}	20		ns	
HLDRQ hold time from CLK ↑		4	t_{HKHQ}	20		ns	
DMA Read/Write Cycle							
CLK ↑ to DMARQ output delay time		5,6	t_{DKMQ}		50	ns	C_L = 50 pF
DMARQ setup time to $\overline{DMAAK}$ ↓		5,6	t_{SMAMQ}	0		ns	
$\overline{DMAAK}$ setup time to $\overline{RD}$ ↓		5	t_{SRMA}	0		ns	
$\overline{DMAAK}$ hold time from $\overline{RD}$ ↑		5	t_{HRMA}	0		ns	
$\overline{DMAAK}$ setup time to $\overline{WR}$ ↓		6	t_{SWMA}	0		ns	
$\overline{DMAAK}$ hold time from $\overline{WR}$ ↑		6	t_{HWMA}	0		ns	
Display Memory Bus Read Cycle							
CLK ↑ to address or data output delay time		4,7,8	t_{DKA}		30	ns	C_L = 50 pF
Input data setup time to CLK ↑		7	t_{SKD}	20		ns	
Input data hold time from CLK ↑		7	t_{HKD}	0		ns	
CLK ↑ to DASTB ↑ delay time		7,8	t_{DKDSH}		30	ns	C_L = 50 pF
CLK ↓ to DASTB ↓ delay time		7,8	t_{DKDSL}		30	ns	
CLK ↑ to $\overline{DRD}$ delay time		7	t_{DKDR}		30	ns	
CLK ↑ to $\overline{DWR}$ delay time		8	t_{DKDW}		30	ns	
System Bus Read Cycle							
$\overline{CS}$ setup time to $\overline{RD}$ ↓		9	t_{SRC}	0		ns	
$\overline{CS}$ hold time from $\overline{RD}$ ↑		9	t_{HRC}	0		ns	
$\overline{RD}$ width, high		5,9	t_{WRH}	50		ns	
ASTB pulse width		5,6,9,10	t_{WAS}	30		ns	

AC Characteristics (cont)

Parameter	Figure	Symbol	Min	Max	Unit	Condition
ASTB setup time to $\overline{RD}$ ↓	5,9	t_{SRAS}	0		ns	
Address setup time to ASTB ↓	5,6,9,10	t_{SASA}	20		ns	
Address hold time from ASTB ↓	5,9	t_{HASA}	0		ns	
Data setup time to READY ↑	5,9	t_{SRYD}	0		ns	
Data float delay time from $\overline{RD}$ ↑	5,9	t_{FRD}	0	40	ns	
$\overline{RD}$ ↓ to READY ↓ delay time	5,9	t_{DRRY}		30	ns	C_L = 50 pF
$\overline{RD}$ hold time from READY ↑	5,9	t_{HRYR}	0		ns	
CLK ↑ to READY ↑ delay time	5,9	t_{DKRY}		40	ns	C_L = 50 pF
$\overline{RD}$ ↑ to ASTB ↑ delay time	5,9	t_{DRAS}	0		ns	
System Bus Write Cycle						
$\overline{CS}$ setup time to $\overline{WR}$ ↓	10	t_{SWC}	0		ns	
$\overline{CS}$ hold time from $\overline{WR}$ ↑	10	t_{HWC}	0		ns	
$\overline{WR}$ width, low	6,10	t_{WWL}	50		ns	
$\overline{WR}$ width, high	6,10	t_{WWH}	50		ns	
Data setup time to $\overline{WR}$ ↑	6,10	t_{SWD}	50		ns	
Data hold time from $\overline{WR}$ ↑	6,10	t_{HWD}	0		ns	
$\overline{WR}$ ↓ to READY ↓ delay time	6,10	t_{DWRY}		30	ns	C_L = 50 pF
$\overline{WR}$ hold time from READY ↑	6,10	t_{HRYW}	50		ns	
CLK ↑ to READY ↑ delay time	6,10	t_{DKRY}		40	ns	C_L = 50 pF
ASTB setup time to $\overline{WR}$ ↓	6,10	t_{SWAS}	0		ns	
$\overline{WR}$ ↑ to ASTB ↑ delay time	6,10	t_{DWAS}	0		ns	
Display Cycle						
SCLK ↑ to DASTB ↑ delay time	11,12,13	$t_{DSKDASH}$		30	ns	C_L = 50 pF
SCLK ↓ to DASTB ↓ delay time	11,12,13	$t_{DSKDASL}$		30	ns	
SCLK ↑ to $\overline{DT/DISP}$ delay time	11,12,13	t_{DSKDT}		30	ns	
SCLK ↑ to address delay time	11,12,13	t_{DSKA}		30	ns	
SCLK ↑ to output signal delay time (HS, VS, BLANK, or GCSR)	11,12, 13	t_{DSKO}		50	ns	
SCLK ↑ to WAIT delay time	11,12	t_{DSKWT}		70	ns	
WAIT pulse width	11	t_{WWT}	$4t_{CYSK} - 70$		ns	
EXVS setup time to SCLK ↑	11	t_{SSKEV}	20		ns	
EXHS setup time to SCLK ↑	11	t_{SSKEH}	20		ns	
EXVS hold time from SCLK ↑	11	t_{HSKEV}	20		ns	
EXHS hold time from SCLK ↑	11	t_{HSKEH}	20		ns	

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Figure 1. Voltage Thresholds for Timing Measurements

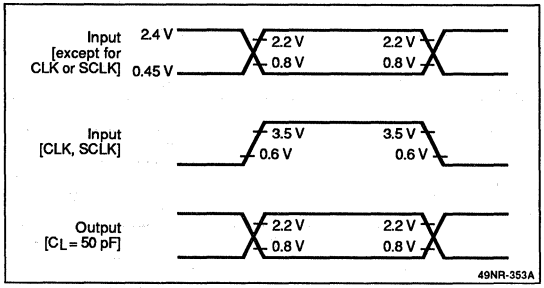

Figure 2. Clock Waveforms

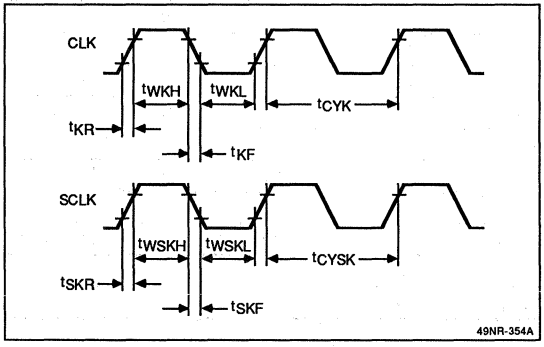

Figure 3. Reset and Interrupt Waveforms

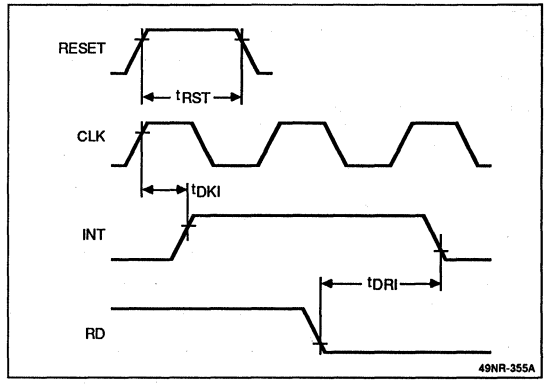

Figure 4. HLDRQ and $\overline{\text{HLDAK}}$ Waveforms

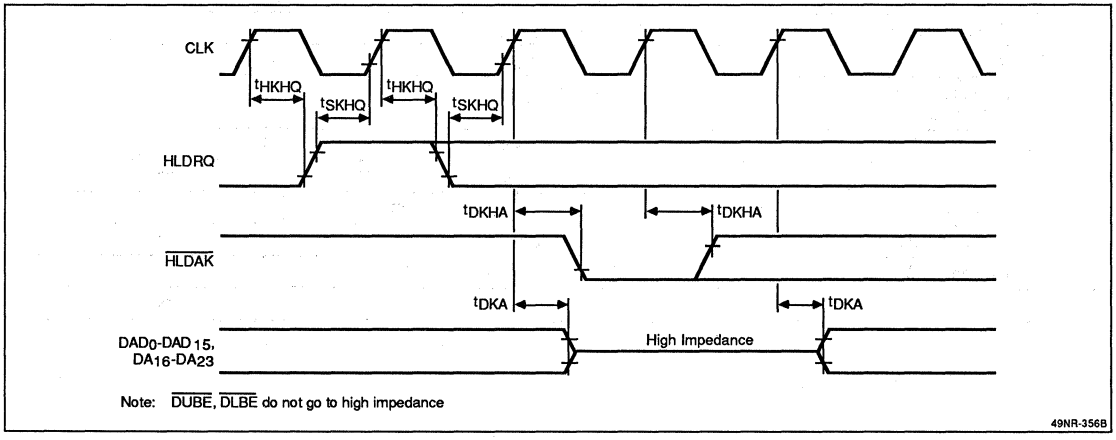

Figure 5. DMA Read Cycle

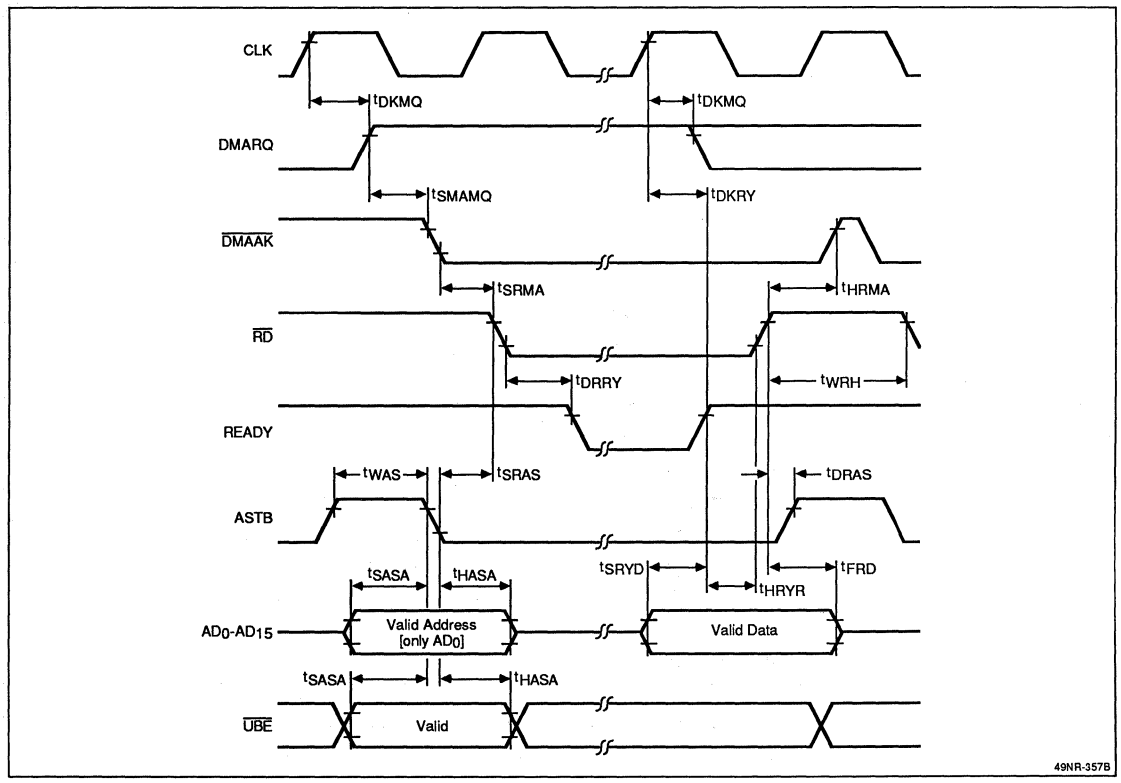

Figure 6. DMA Write Cycle

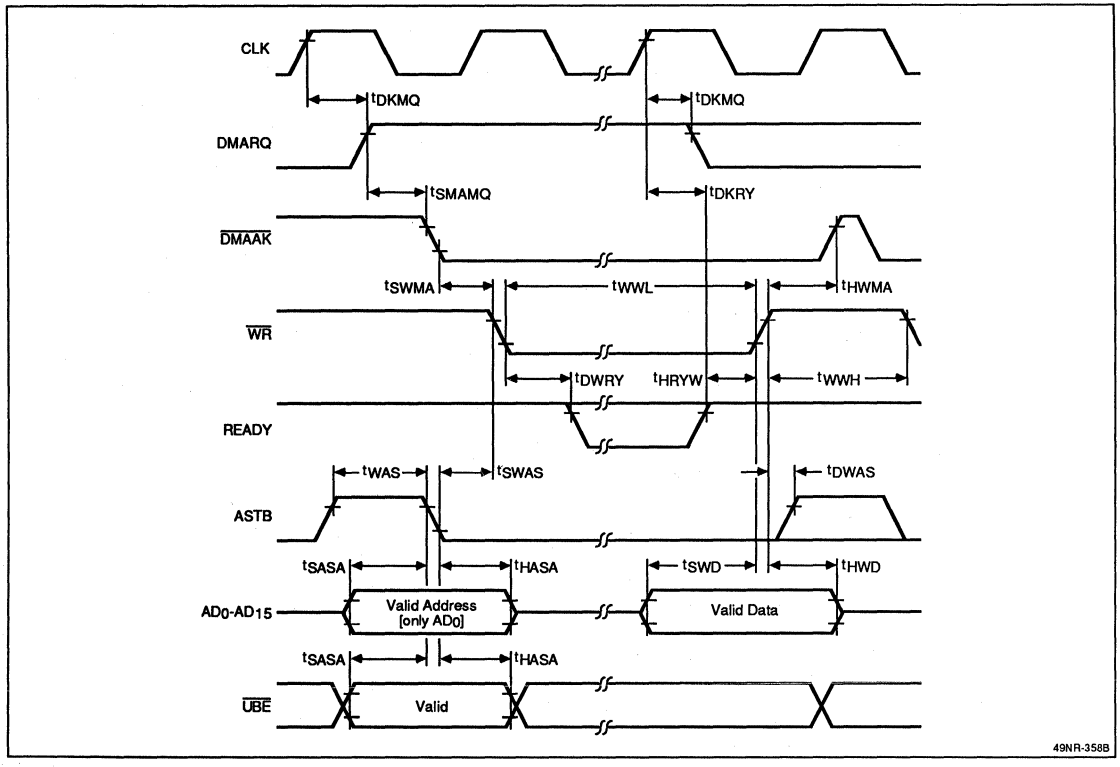

Figure 7. Display Memory Bus Read Cycle

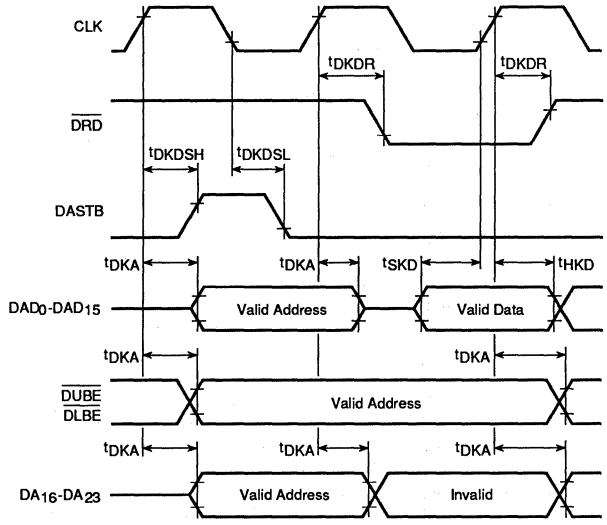

Figure 8. Display Memory Bus Write Cycle

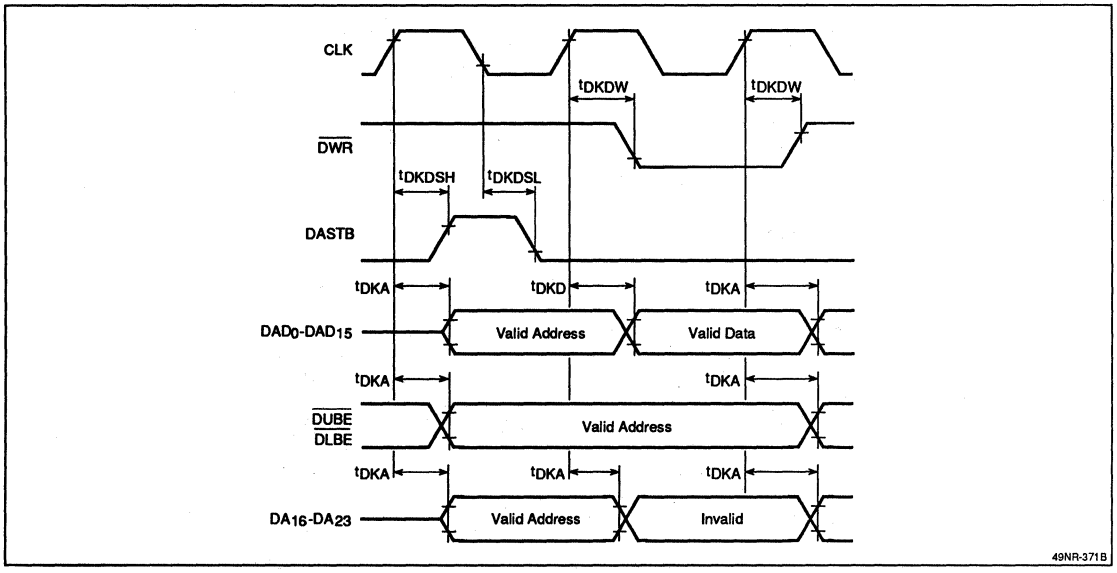

Figure 9. System Bus Read Cycle

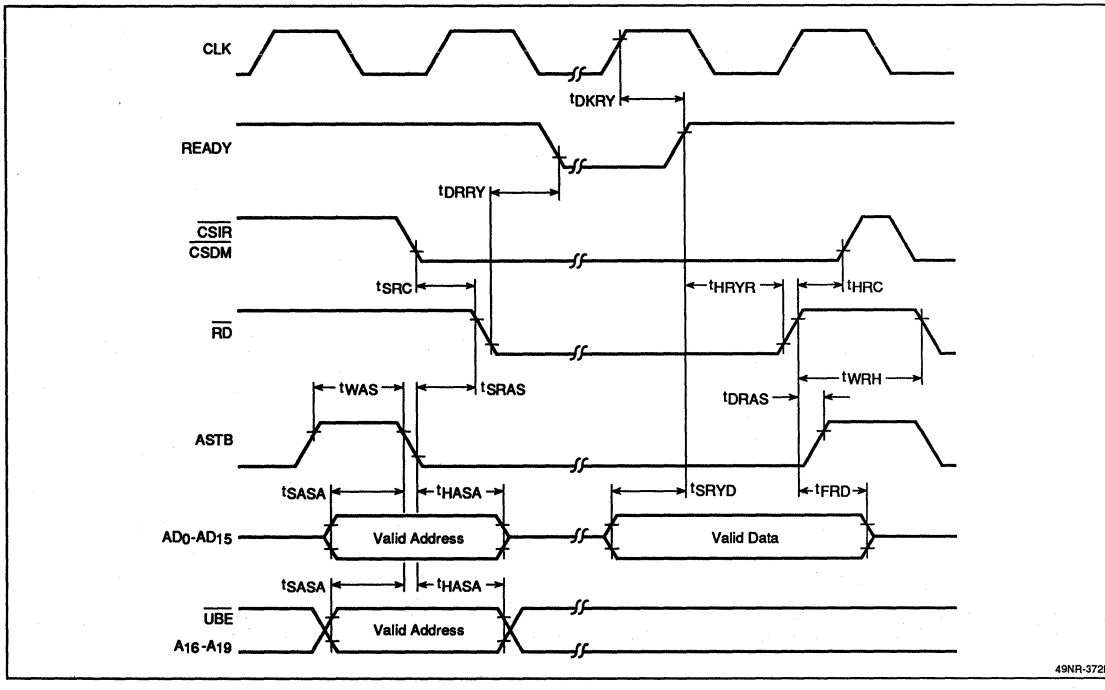

Figure 10. System Bus Write Cycle

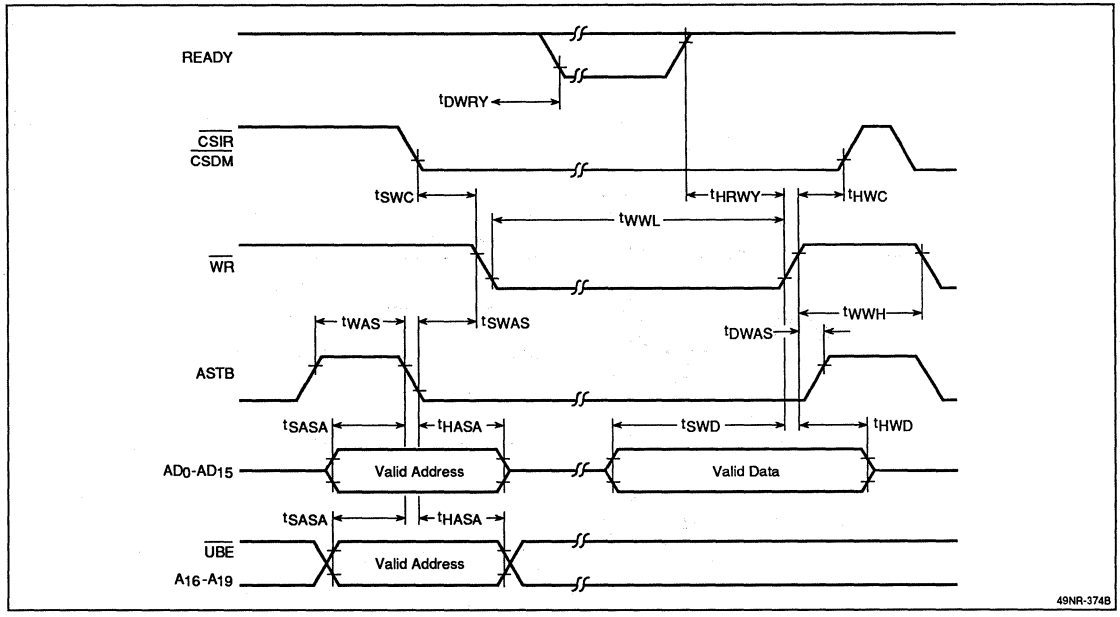

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Figure 11. Display Cycle

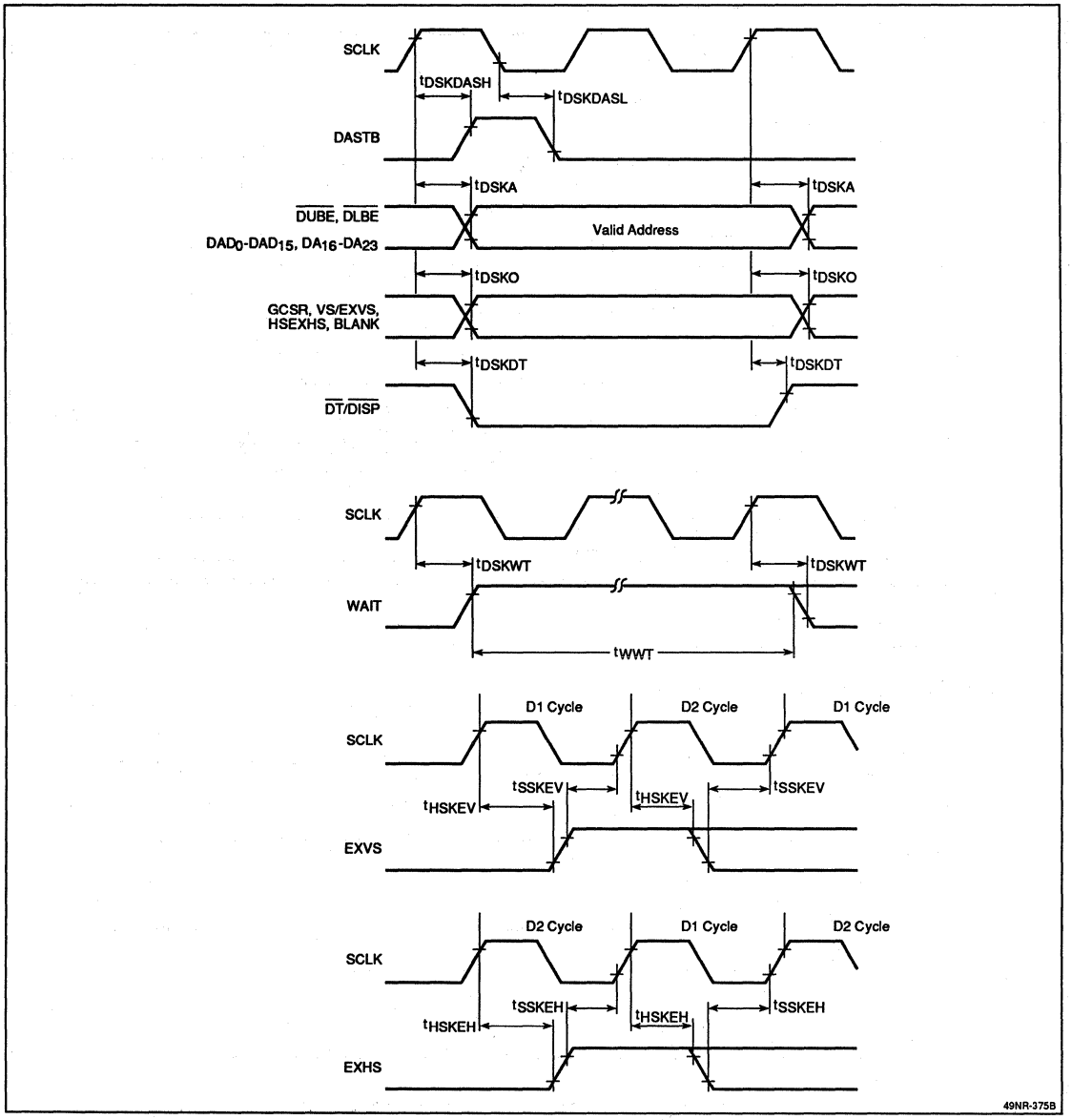


Figure 12. Display Refresh Cycle (DT Mode)

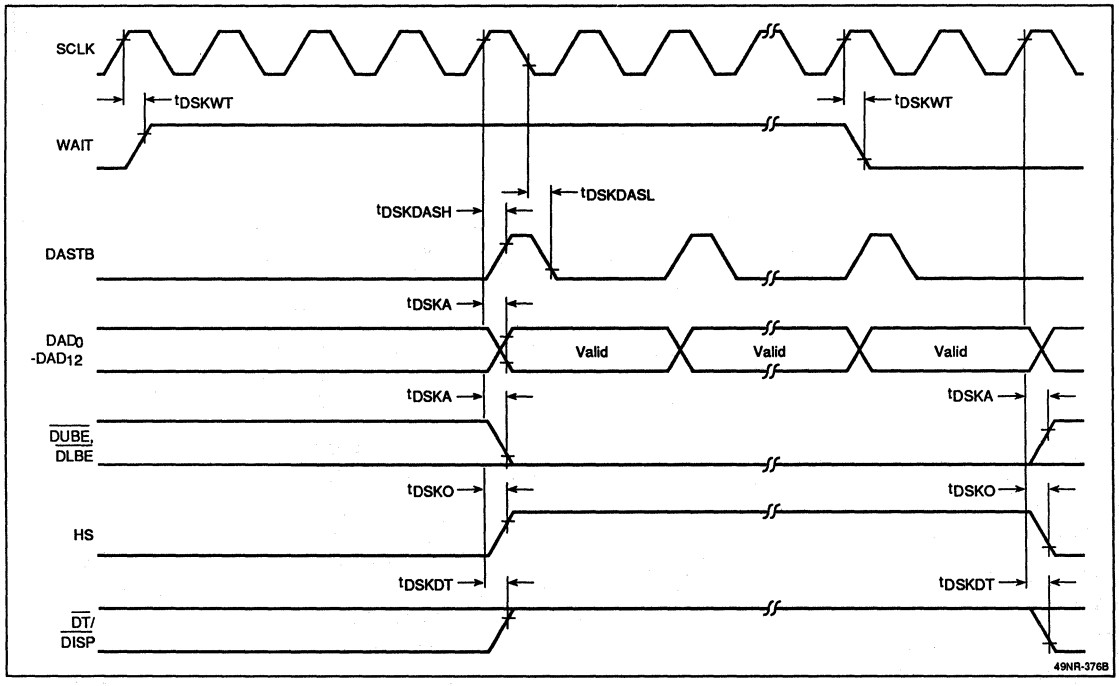
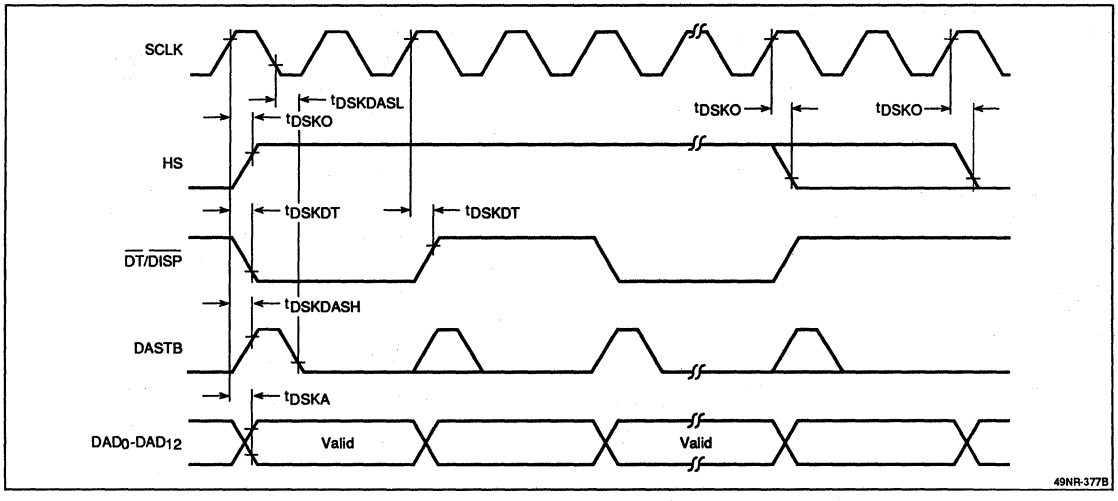


Figure 13. Display Refresh Cycle (CS Mode)



FUNCTIONAL DESCRIPTION

Preprocessor

The preprocessor includes a 56-word parameter RAM, an arithmetic logic unit, and a general-purpose register. It carries out the following drawing preprocessing by microprogram control.

- Conversion between coordinate and physical addresses
- Command interpretation
- Drawing parameter generation
- Calculation of tiling pattern position
- Sorting of vertex coordinates for triangular fill command
- Error checking on user-defined parameters
- Data passing with drawing processor
- Drawing processor initiation

Along with the drawing processor, the preprocessor forms part of a three-stage pipeline to improve throughput.

Drawing Processor

The drawing processor carries out the drawing operations on the display memory with the commands and parameters generated by the preprocessor. The drawing processor includes various arithmetic units, a general-purpose register, an arithmetic logic unit, and mask generating circuitry. In addition, it contains a 32-bit barrel shifter for high-speed bit-boundary processing operations and a 90-degree rotation data buffer. These components are controlled by a horizontal-type microprogram that can execute five types of instructions simultaneously in a single step.

Display Processor

An external dot-shifter for parallel-to-serial conversion is generally necessary to create scan line information for display on a CRT. The display processor generates display addresses to supply the image data to the dot shifter. This processor includes a DRAM refresh controller to generate refresh addresses during the horizontal sync active period. The display controller also controls the generation of refresh and display addresses for dual-port DRAMs (video RAMs), DRAMs, and SRAMs.

Sync Signal Generator

The sync signal generator produces horizontal and vertical sync signals and blank signals according to the parameters set by the user. This circuitry also generates the graphics cursor signal that can be used (with external circuitry) to generate a screen cursor.

CPU Interface Unit

The CPU interface unit includes a DMA interface (DMARQ, $\overline{\text{DMAAK}}$) and an interrupt (INT) control circuit. The unit controls timing for system bus communications.

Display Memory Interface Unit

This interface unit controls the drawing, display, and refresh address outputs. It also controls the display memory bus arbitration for direct access to the display memory by other processors.

REGISTERS

Table 1 lists the registers according to four classifications: control, display, drawing, and data port. Figure 14 shows the register configurations in numerical order by register address from 00H to 7FH.

Also in numerical order by address are the register descriptions in table 2. Figures listed below supplement the descriptions.

Figure	Title
15	Raster Operations; Replace and XOR
16	Raster Operations; AND and OR
17	Status Register Configuration
18	Display Memory Address Generation
19	Control Register Configuration
20	Definition of Clipping Rectangle
21	Display Control Register Configuration
22	Cursor Position Registers
23	Horizontal and Vertical Sync Timing Diagram

DRAWING OPERATIONS

The DRAW command is written to the COMMAND register at address 6EH-6FH. The opcode in register 6FH determines the type of drawing. Various combinations of the command are selected by flags in register 6EH.

Table 3 lists the commands in five categories: data read, graphics drawing, fill, copy, and PUT/GET. Table 4 describes the commands and shows the register configuration.

Figures listed below give examples of DRAW commands.

Figure	Title
24	Graphics Drawing Commands
25	Fill and Paint Commands
26	Copy Commands; Copy, Rotate, Slant
27	Copy Commands; Enlarge/Shrink, Rotate

Table 5 summarizes the DRAW commands. Table 6 describes the 20 operation flags that can be set in register 6EH.

Table 1. Register Classifications

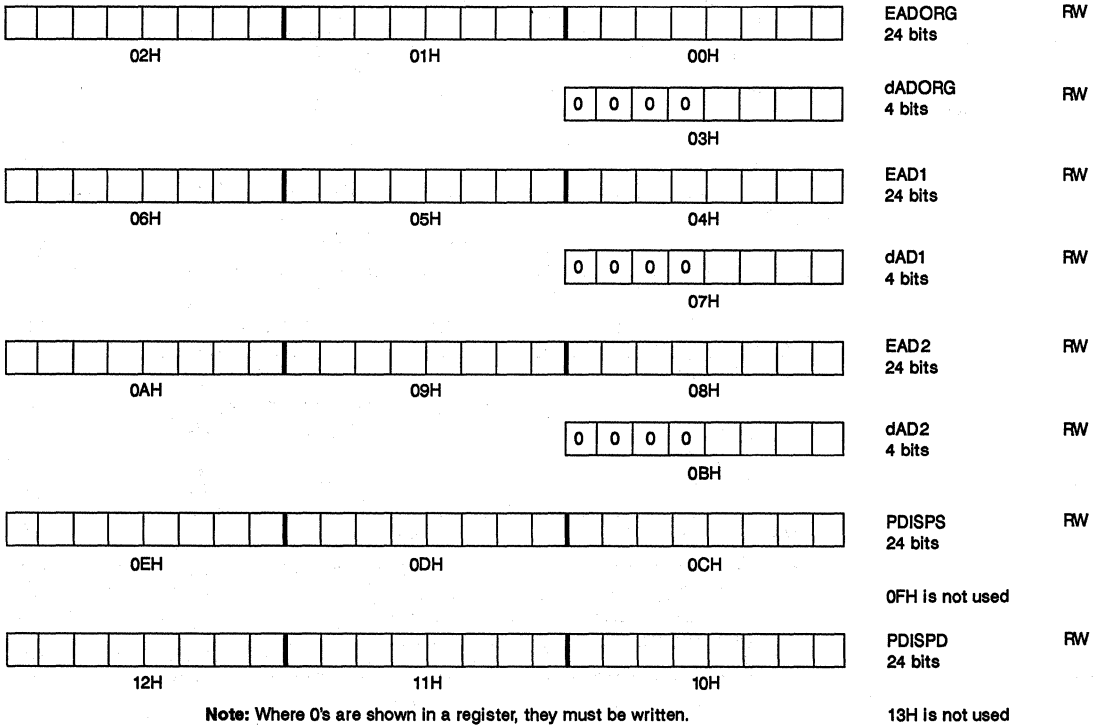
Classification	Application	Register Name	Address (Hex)	Bits
μPD72120 AGDC control registers	Status	STATUS	3C-3D	9
	Control	CTRL	3D	8
	Higher 8 bits of address in display memory direct access	BANK	3C	8
Display-related registers	Display status setting	DISPLAY CTRL	70-71	16
	Display area setting	DISPLAY PITCH	72-73	12
		AC	73	3
		DAD	74-76	24
		WC(L)	77	8
		WC(H)	7D	4
	Cursor setting	CRS	79	1
		CE	79	1
		GCSRX	78-79	12
		GCSRYS	7A-7B	12
		GCSRYE	7C-7D	12
	Horizontal sync signal setting	HS, HBP HH, HD, HFP	7E-7F	12
	Vertical sync signal setting	VS, VBP, L/F, VFP	7E-7F	12
Drawing-related registers	Logical address zero point setting	EADORG	00-02	24
		dADORG	03	4
	Logical address setting	PITCHS	58-59	16
		PITCHD	5A-5B	16
	Plane setting	PDISPS	0C-0E	24
		PDISPD	10-12	24
		PMAX	14-15	16
	Interplane logical operation setting	MOD0	16	4
		MOD1	16	4
		PLANES	5E-5F	16
	Clipping setting	XCLMIN	62-63	16
		YCLMIN	64-65	16
		XCLMAX	66-67	16
		YCLMAX	68-69	16
		CLIP	6D	2
	Enlarge/shrink coefficient setting	MAGH	6C	4
		MAGV	6C	4
	Painting pattern setting	PTNP	18-1A	24
		PTNCNT	60-61	16
	AGDC work area setting	STACK	1C-1E	24
		STMAX	5C-5D	16
	Physical address (word address) value setting	EAD1	04-06	24
		EAD2	08-0A	24

Table 1. Register Classifications (cont)

Classification	Application	Register Name	Address (Hex)	Bits
Drawing related-registers (cont)	Physical address (dot address) value setting	dAD1	07	4
		dAD2	0B	4
	Logical address (X coordinate) value setting	X	40-41	16
		DX*	44-45	16
		XS	48-49	16
		XE	4C-4D	16
		XC	50-51	16
		DH	54-55	16
	Logical address (Y coordinate) value setting	Y	42-43	16
		DY	46-47	16
		YS	4A-4B	16
		YE	4E-4F	16
		YC	52-53	16
		DV	56-57	16
	Command	COMMAND	6E-6F	16
Data port registers	Data port during execution of PUT/GET	PGPORT	3E-3F	16
	Data port during execution of READ DP/READ COL	DX*	44-45	16

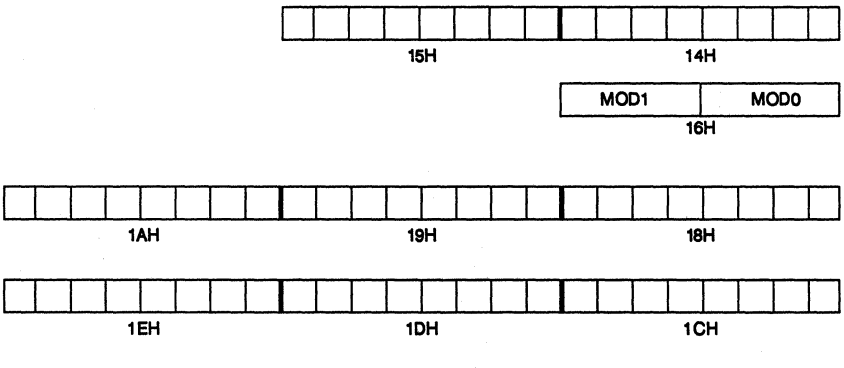
* The DX register is used as the logical address (X coordinate) value setting register and at the same time as the data port during the execution of a READ DP or READ COL command.

Figure 14. Register Configurations



Note: Where 0's are shown in a register, they must be written.

Figure 14. Register Configurations (cont)



PMAX 16 bits RW

MOD1/MOD0 4 bits each RW

17H is not used

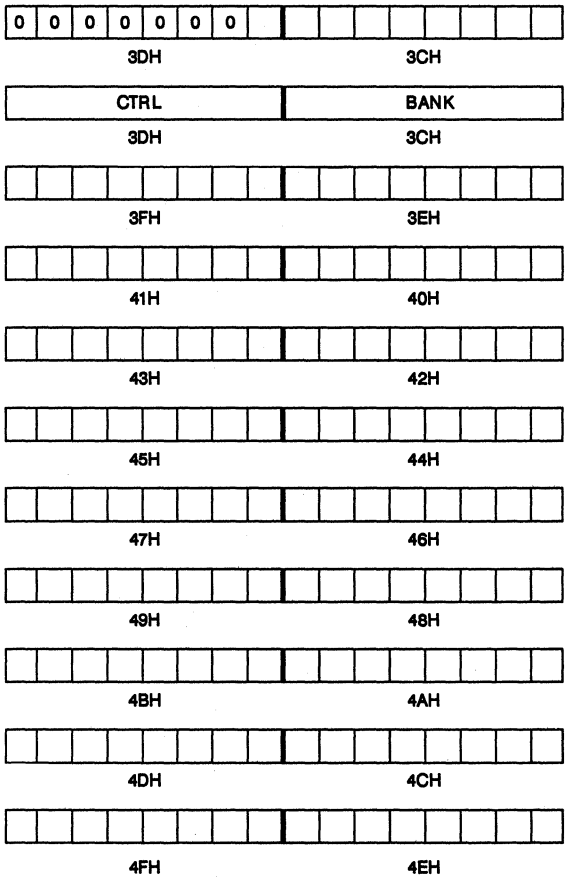
PTNP 24 bits RW

1BH is not used

STACK 24 bits RW

1FH is not used

Addresses 20H-3BH are used as internal working registers. These addresses are not available to the user.



STATUS 9 bits R

CTRL/BANK 8 bits each W

PGPORT 16 bits RW

X 16 bits RW

Y 16 bits RW

DX 16 bits RW

DY 16 bits RW

XS 16 bits RW

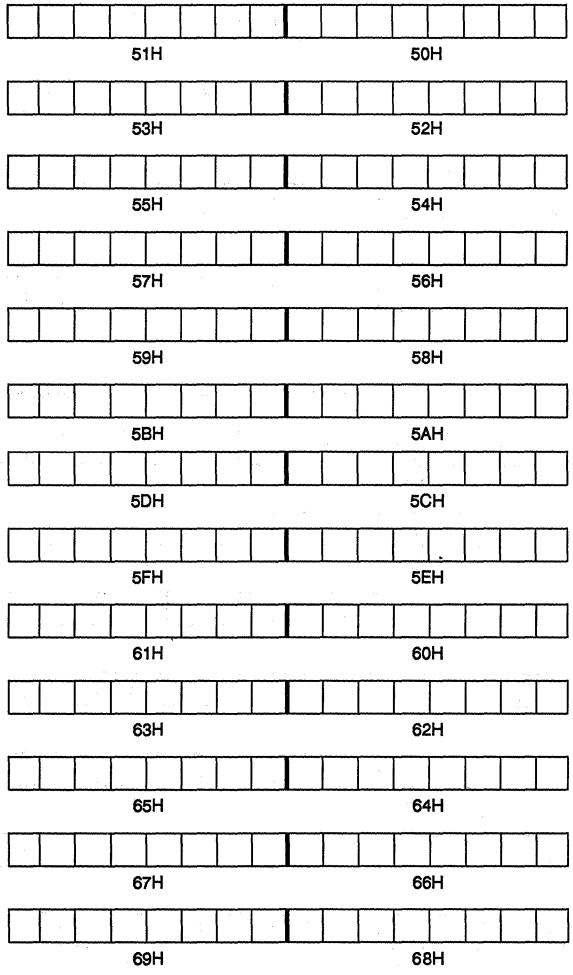
YS 16 bits RW

XE 16 bits RW

YE 16 bits RW

3

Figure 14. Register Configurations (cont)



Addresses 6AH-6BH are used as internal working registers. They are not available to the user.

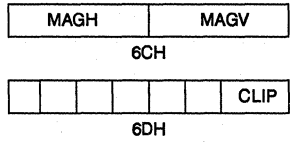


Figure 14. Register Configuration (cont)

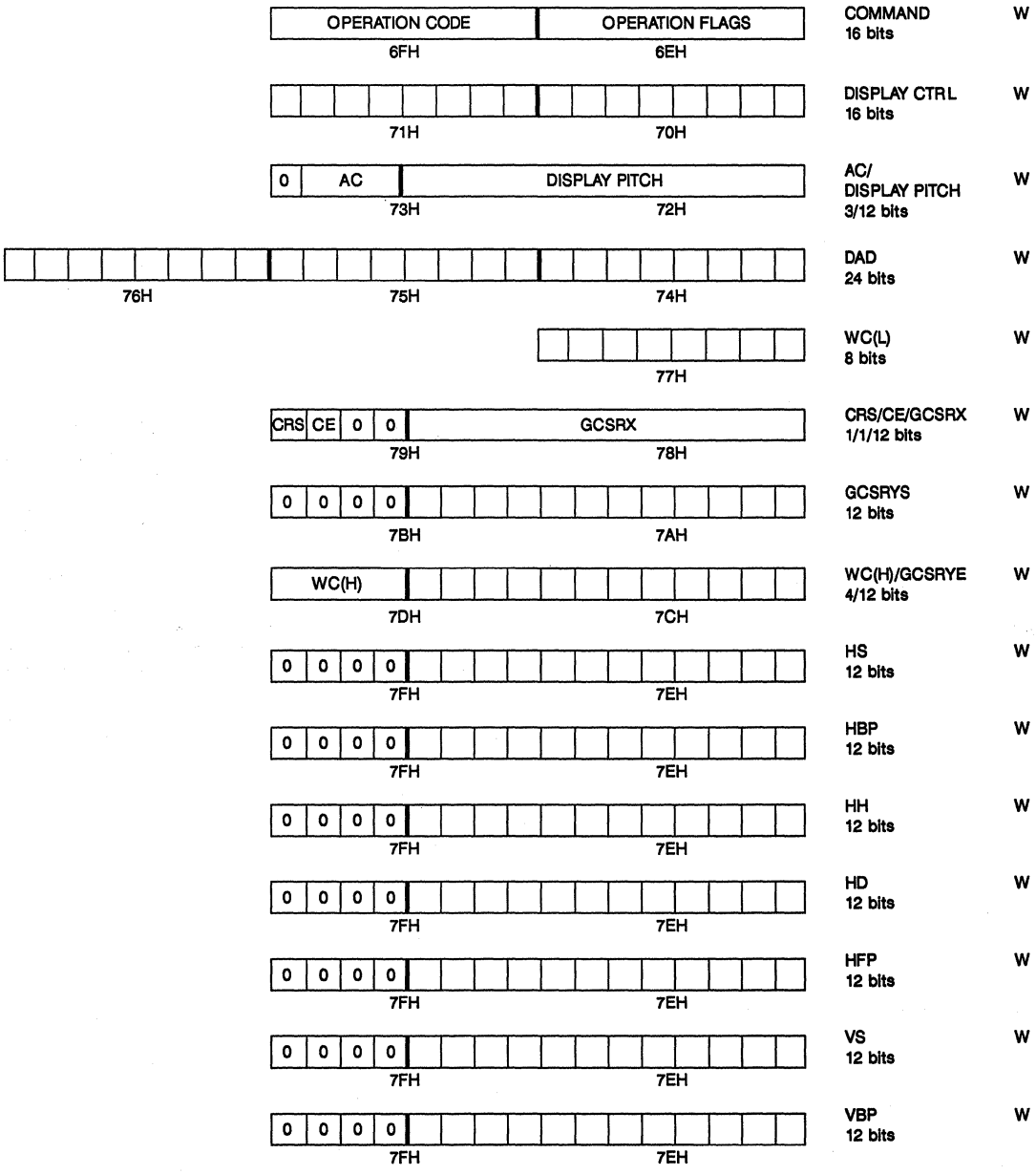
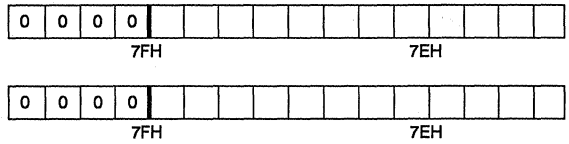


Figure 14. Register Configurations (cont)



HS, HBP, HH, HD, HFP, VS, VBP, L/F and VFP are all at address 7EH-7FH and must be written in the order listed.

Table 2. Register Descriptions

Address (Hex)	Bits	Name	Description
00H-02H	24	EADORG Execution Address Origin	Sets the physical address (effective address) in the display memory corresponding to the origin (0,0) on the logical plane (the X-Y coordinate plane).
03H	4	dADORG Dot Address Origin	Sets the dot position in the physical address (effective address) in the display memory corresponding to the origin (0,0) on the logical plane (the X-Y coordinate plane).
04H-06H	24	EAD1 Execution Address 1	Sets the drawing start physical address value in the drawing processor when the drawing start position is given by the physical address.
07H	4	dAD1 Dot Address 1	Sets the dot position in the display memory when the drawing start position is given by the physical address
08H-0AH	24	EAD2 Execution Address 2	Sets the drawing start physical address value in the drawing processor when the drawing start position is given by the physical address.
0BH	4	dAD2 Dot Address 2	Sets the dot position in the display memory when the drawing start position is given by the physical address.
0CH-0EH	24	PDISPS Plane Displacement Source	Sets the number of words that occupy one memory plane when the memory is configured with two or more planes. In the case of a COPY command, sets the number of words per source plane. In the case of a PAINT command, sets the number of words per plane containing the tiling pattern.
10H-12H	24	PDISPD Plane Displacement Destination	Sets the number of words that occupy one memory plane when the memory is configured with two or more planes. In the case of a COPY command, sets the number of words per destination plane. In the case of a PAINT command, sets the number of words per painting plane.
14H-15H	16	PMAX Plane Maximum	Sets the number of planes (up to 16) in the display memory to be drawn, as shown in the following table: PMAX — Planes 0000 0000 0000 0001 — 1 0000 0000 0000 0010 — 1-2 0000 0000 0000 0100 — 1-3 0010 0000 0000 0000 — 1-14 0100 0000 0000 0000 — 1-15 1000 0000 0000 0000 — 1-16
16H	4	MOD0 Drawing Mode 0	Defines the type of logical operation to be performed during drawing or copying. When the bit in the PLANES register corresponding to the memory plane is 0, the logical operation defined by MOD0 is performed. See figures 15 and 16.
16H	4	MOD1 Drawing Mode 1	Defines the type of logical operation to be performed during drawing or copying. When the bit in the PLANES registers corresponding to the memory plane is 1, the logical operation defined by MOD1 is performed. See figures 15 and 16.
18H-1AH	24	PTNP Pattern Pointer	Sets the first physical address in the display memory area containing the tiling (painting or filling) pattern.

Table 2. Register Descriptions (cont)

Address (Hex)	Bits	Name	Description
1CH-1EH	24	STACK Stack Pointer	Sets the first physical address in the display memory area to save data such as coordinates, etc., during retrieval of the boundary points during the PAINT command (arbitrary area fill). It may be considered as the working area of the AGDC during execution of the PAINT command.
3CH-3DH	9	STATUS Status	Contains the internal status of the AGDC. The format is shown in figure 17.
3CH	8	BANK Bank	The AGDC interface to the CPU accommodates up to a 20-bit address. The AGDC can address 16M words (32M bytes) of display memory (24-bit addressing). When the CPU addresses display memory directly (through the AGDC), the lower 16 or 20 bits provided by the CPU are combined with the 8 bits from the BANK register to form the 24-bit display memory address. The address combination is shown in figure 18,
3DH	8	CTRL Control	Controls internal AGDC processing. See figure 19.
3EH-3FH	16	PGPORT Put/Get Port	During a PUT operation, data is written to this register by the host CPU or system DMA controller. The AGDC then places the data into display memory. During a GET operation, the host CPU or DMA controller reads the data from this register that was retrieved from the display memory by the AGDC.
40H-57H	16 each	X, Y, DX, DY, XS, YS, XE, YE, XC, YC,.DH, DV	Set the coordinate parameters for various drawing operations. The DX register is also used for reading the data during the READ COL command. The DH register is also used for storing half the line pattern when a 32-bit line pattern is used.
58H-59H	16	PITCHS Pitch Source	Sets the number of words in the horizontal direction of the source display memory area to be transferred.
5AH-5BH	16	PITCHD Pitch Destination	Sets the number of words in the horizontal direction of the display memory for drawing or as the destination of display memory transfer.
5CH-5DH	16	STMAX Stack Maximum	Sets the size of the display memory area in words for the STACK (used during the arbitrary area fill PAINT command). Each boundary point found during the PAINT command requires six words of memory in the STACK area.
5EH-5FH	16	PLANES Plane Select	Selects the type of logical operation to be performed on each plane during drawing or copying. Each bit in this register corresponds to a display memory plane.The least significant bit (bit 0) corresponds to the first plane, the most significant bit (bit 15) to the 16th plane. A 0 in the bit position for a plane indicates that the logical operation specified by MOD0 is to be performed and a 1, the operation specified by MOD1.
60H-61H	16	PTNCNT Pattern Count	Sets the line pattern for drawing straight and curved lines. During filling or painting operations, the function of this register depends on the TL bit as follows. TL = 1 PTNCNT specifies the length (in words) of the tiling pattern in display memory. The starting address is contained in the PTNP register. TL = 0 PTNCNT contains the actual 16-bit pattern to be used as the tiling pattern.
62H-69H	16 each	XCLMIN, YCLMIN, XCLMAX, YCLMAX X and Y Clipping, Minimum/Maximum Values	Defines the rectangular clipping region. An example is shown in figure 20.
6CH	4	MAGH Horizontal Magnification	Sets the horizontal enlarge/shrink factor.
6CH	4	MAGV Vertical Magnification	Sets the vertical enlarge/shrink factor.

Table 2. Register Descriptions (cont)

Address (Hex)	Bits	Name	Description
6DH	2	CLIP Clipping Mode	Sets the clipping mode to select one of the following operations. CLIP — Function 00 — Draws within the clipping rectangle. Must be in this mode for PAINT. 01 — No clipping operation 10 — Draws outside the clipping rectangle 11 — Prohibited
6EH-6FH	16	COMMAND	Commands to be executed by the AGDC are written to this register. The lower byte (bits 0-7) consists of operation flags and the upper byte (bits 8-15), an operation code. Processing begins when an operation code is written to the COMMAND register.
70H-71H	16	DISPLAY CTRL Display Control	Sets the operation of the display processor and sync signal generation. The format and function are shown in figure 21.
72H-73H	12	DISPLAY PITCH	Sets the total number of words in the horizontal direction (width) of a plane. Display Pitch — Number of addresses (words) 0000 0000 0000 — 4096 0000 0000 0001 — 1 0000 0000 0010 — 2 0000 0000 0011 — 3 : — : 1111 1111 1110 — 4094 1111 1111 1111 — 4095
73H	3	AC Address Control	Defines which address bus signal lines should be used to output the refresh address. AC — Refresh address output pins — Conditions for setting DT active 000 — DAD_0-DAD_{12} — DAD_0-DAD_7 = 0 001 — Disabled — Disabled 010 — Disabled — Disabled 011 — Disabled — Disabled 100 — DAD_1-DAD_{12} — DAD_1-DAD_8 = 0 101 — DAD_2-DAD_{12} — DAD_2-DAD_9 = 0 110 — DAD_3-DAD_{12} — DAD_3-DAD_{10} = 0 111 — DAD_4-DAD_{12} — DAD_4-DAD_{11} = 0
74H-76H	24	DAD Display Address	Sets the display starting address for the screen
77H (Lower 8 bits), 7DH (Upper 4 bits)	12	WC Word Count	Sets the number of displayed words during a horizontal scan line (while BLANK low or inactive) WC — Number of displayed words 0000 0000 0000 — 1 0000 0000 0001 — 2 : — : 1111 1111 1110 — 4095 1111 1111 1111 — 4096
78H-79H	12	GCSRX Graphics Cursor X Coordinate	Sets the X (horizontal) coordinate start for the graphics cursor output pin. It is given as the number of dispaly cycles from the start of each horizontal scan line GCSRX — Starting position on each horizontal line 0000 0000 0000 — Disabled 0000 0000 0001 — 1st display cycle 0000 0000 0010 — 2nd display cycle : — : 1111 1111 1110 — 4094th display cycle 1111 1111 1111 — 4095th display cycle

Table 2. Register Descriptions (cont)

Address (Hex)	Bits	Name	Description
79H	1	CRS Cursor Configure Select	Determines whether the horizontal and vertical cursor position registers are ANDed or ORed together. See figure 22. CRS — Function 0 — AND 1 — OR
79H	1	CE Cursor Display Enable	Enables the graphics cursor signal to be output on the GCSR pin. CE — Function 0 — Disabled 1 — Enabled
7AH-7BH	12	GCSRYS Graphics Cursor Y Coordinate Start	Determines the starting Y (vertical) coordinate of the graphics cursor, counting display lines from the top down. GCSRYS — Vertical starting line 0000 0000 0000 — invalid 0000 0000 0001 — 1st display line 0000 0000 0010 — 2nd display line : — : 1111 1111 1110 — 4094th display line 1111 1111 1111 — 4095th display line
7CH-7DH	12	GCSRYE Graphics Cursor Y Coordinate End	Determines the ending Y (vertical) coordinate of the graphics cursor, counting display lines from the top down. GCSRYE — Vertical ending line 0000 0000 0000 — invalid 0000 0000 0001 — 1st display line 0000 0000 0010 — 2nd display line : — : 1111 1111 1110 — 4094th display line 1111 1111 1111 — 4095th display line
7EH-7FH	12	HS (Horizontal Sync), HBP (Horizontal Back Porch), HH (HBP to Midpoint Between Consecutive HSs), HD (Horizontal Drawing Period), HFP (Horizontal Front Porch)	Sets the horizontal video sync (timing) parameters. See figure 23. HS Horizontal sync high-level period (horizontal retrace) HBP Horizontal back porch (non-displayed portion on left side of screen) HH Rising/falling timing for even field synchronization during interlaced display HD Horizontal display period (active display time) HFP Horizontal front porch (non-displayed portion on right side of screen) HS, HBP, HH, HD, HFP — * SCLK periods 0000 0000 0000 — 2 clocks 0000 0000 0001 — 4 clocks : — : 1111 1111 1110 — 8190 clocks 1111 1111 1111 — 8192 clocks *One display cycle is equal to two SCLK periods Setting requirements For display control by AGDC: HS, HBP, HH, HD, HBP ≥ 4 SCLK periods For interlace display: HBP ≥ 6 SCLK periods For AGDC in slave mode: HS ≥ 10 SCLK periods

3

Table 2. Register Descriptions (cont)

Address (Hex)	Bits	Name	Description
7EH-7FH	12 each	VS (Vertical Sync), VBP (Vertical Back Porch), L/F (Lines per Field), VFP (Vertical Front Porch)	Sets the vertical sync (timing) parameters. See figure 23. VS Vertical sync (retrace) high-level period VBP Vertical back porch (non-displayed portion on upper part of screen) L/F Lines per field (number of horizontal scan lines displayed) VFP Vertical front porch (non-displayed portion on lower part of screen) VS, VBP, L/F, VFP — *Horizontal scan lines 0000 0000 0000 — 4096 0000 0000 0001 — 1 0000 0000 0010 — 2 : — : 1111 1111 1110 — 4094 1111 1111 1111 — 4095 * Vertical timing parameters are set as multiples of the horizontal scan line period.

Figure 15. Raster Operations: Replace and XOR (MOD0/MOD1)

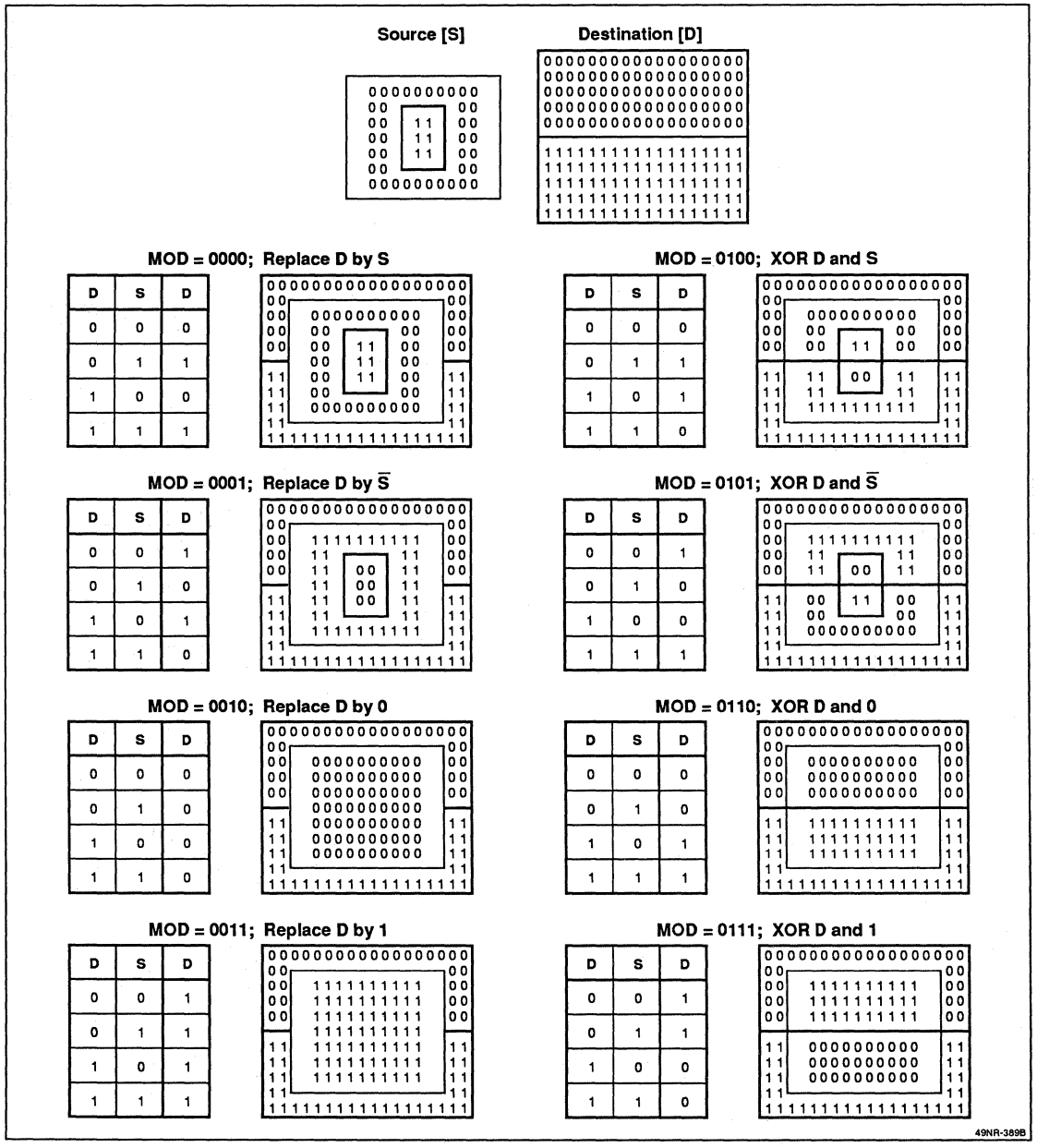


Figure 16. Raster Operations; AND and OR (MOD0/MOD1)

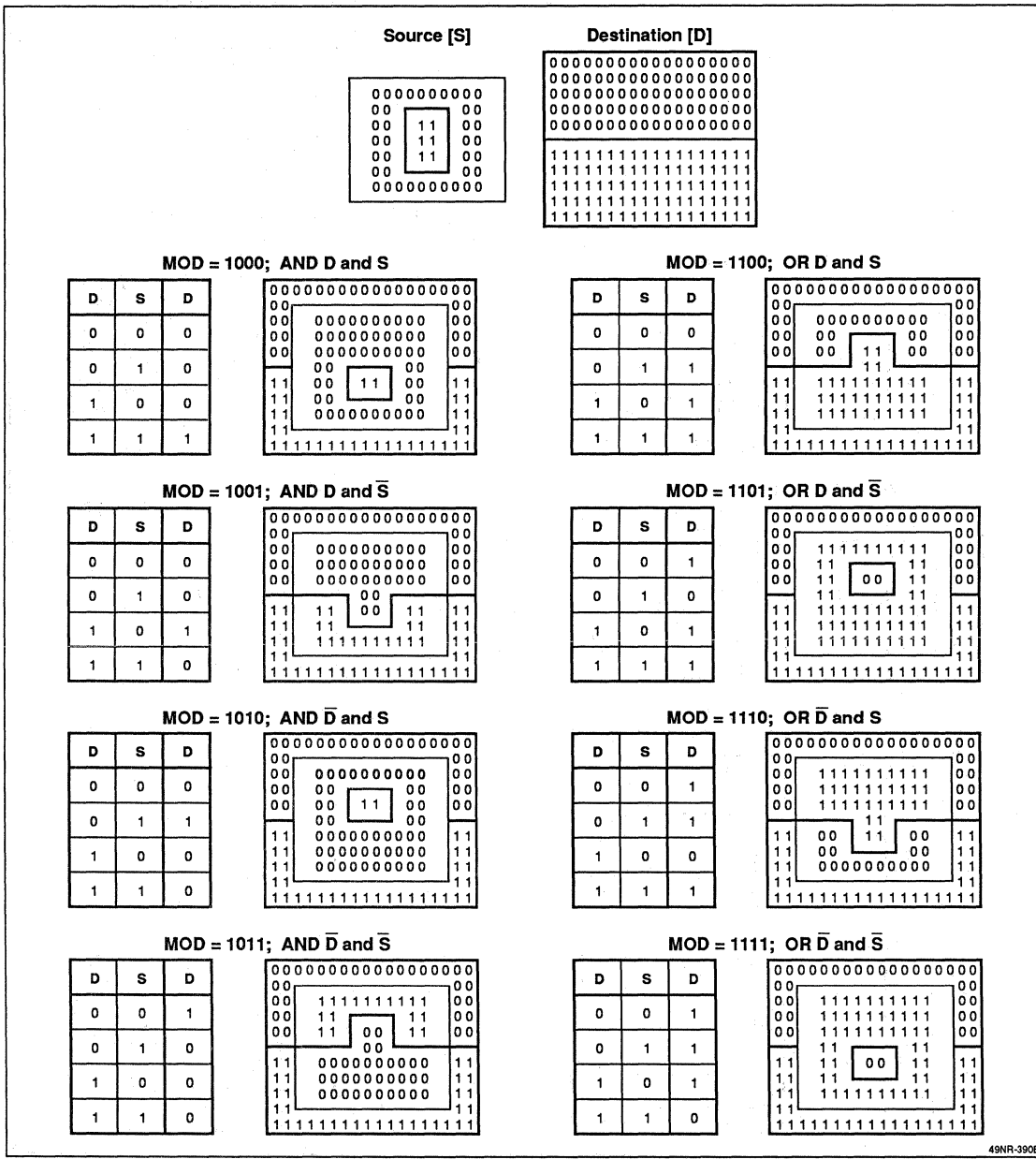
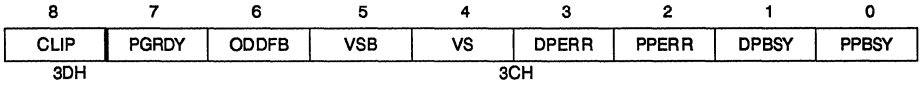


Figure 17. Status Register Format



Bit	Flag Name	Abbreviation	Meaning When Bit = 1
0	Preprocessor Busy	PPBSY	The preprocessor is executing a command.
1	Drawing Processor Busy	DPBSY	The drawing processor is executing a command.
2	Preprocessor Error	PPERR	An error was detected during the execution of a command by the preprocessor.
3	Drawing Processor Error	DPERR	An error was detected during execution of a command by the drawing processor.
4	Vertical Sync Period	VS	Indicates vertical sync period.
5	Vertical Blanking Period	VSB	Indicates vertical blanking period.
6	Odd Field	ODDFD	Indicates odd field during interlaced operation.
7	Put/Get Ready	PGRDY	Indicates that data can be transferred during a PUT or GET command.
8	Clipping	CLIP	Picking or object detected.

Figure 18. Display Memory Addressing

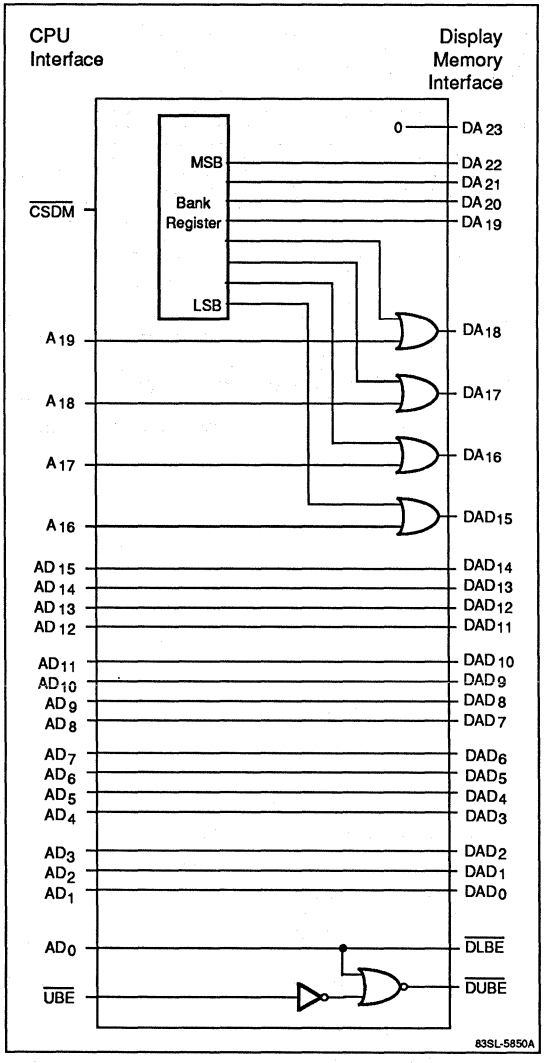


Figure 19. Register Format

7	6	5	4	3	2	1	0
DBIE	PBIE	CIE	0	0	0	ABORT	RESET

Bit	Flag Name	Abbreviation	Meaning When Bit = 1
0	Software Reset	RESET	Initializes μPD72120.
1	Processor Abort	ABORT	Stops any processing being performed and clears the processor BUSY status.
2	Not used		Must be set to 0.
3	Not used		
4	Not used		
5	Clipping Interrupt Enable	CIE	Enables the INT signal when picking (drawing in the clipped region).
6	Preprocessor Busy Interrupt Enable	PBIE	Enables the INT signal when the preprocessor status changes from BUSY to NOT BUSY.
7	Drawing Processor Busy Interrupt Enable	DBIE	Enables the INT signal when the drawing processor status changes from BUSY to NOT BUSY.

Figure 20. Rectangular Clipping Region

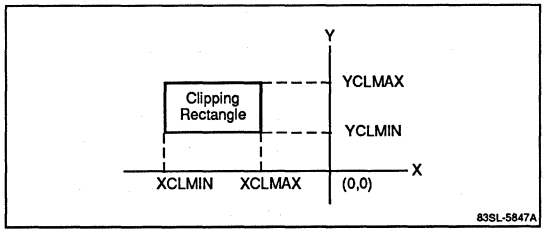


Figure 21. Display Control Register

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB
DTM	DTT	DAD+			IN	RE	SC	FCCL	TCCL	MASK	M/S	SD	LFI	SPST	SVS

Bit	Flag Name	Abbreviation	Function
0	Slave Sync	SVS	When the AGDC is in the slave mode, SVS determines the initialization of the internal horizontal and vertical counters. SVS is ignored in the master mode. SVS 0 Initializes the vertical and horizontal counters at the rising edge of EXVS and EXHS, respectively. 1 Initializes the vertical and horizontal counters at the rising edge of EXVS.
1	Sync Parameter Setting	SPST	Enables the writing of the sync timing parameters (HS, HBP, HH, HD, HFP, VS, VBP, L/F and VFP) to address 7EH-7FH. The writing should take place after SPST is set to 0, then to 1. SPST 0 Disables writing of sync parameters 1 Enables writing of sync parameters
2	Display Lines per Frame in Interlace Mode	LFI	Defines whether there is an even or odd number of lines per frame in interlaced mode. LFI is ignored in non-interlaced mode. LFI 0 Even total number of lines for the sum of even and odd fields (one frame). 1 Odd total number of lines for sum of even and odd fields.

Figure 21. Display Control Register (cont)

Bit	Flag Name	Abbreviation	Function
3	Stop Display	SD	Defines the state of the BLANK output signal. SD is set to 1 by a high level on the RESET pin. SD 0 BLANK signal active (high) only for the non-display period defined by the video sync signals. 1 BLANK signal active for display and non-display periods (on continuously),
4	Master/Slave	M/S	Defines whether the AGDC is a master or a slave in terms of video sync signal generation. M/S 0 Sets the AGDC to slave mode (video sync signals input through EXVS and EXHS). 1 Sets the AGDC to master mode (generates video sync signals and outputs them through VS and HS).
5	Mask	MASK	Defines the VS signal output timing in the master mode. In the slave mode, defines the validity of the EXHS and EXVS sync timing input. MS MASK 0 0 Accepts EXHS and EXVS sync timing input. 0 1 Ignores EXHS and EXVS sync timing input. 1 0 Only the VS signal of the even field in interlace mode is output. 1 1 The VS signal is output normally.
6	Timing Counter Clear	TCCL	Defines the timing for initializing the internal display cycle counter when the AGDC is in slave mode. TCCL is ignored when the AGDC is in master mode. TCCL 0 Does not initialize the display cycle counter on the rising edge of EXVS. 1 Initializes the display cycle counter on the rising edge of EXVS (sets the counter to the D1 cycle).
7	Field Counter Clear	FCCL	Defines the timing for initializing the internal field counter when using interlaced display in the slave mode. When the AGDC is in master mode or non-interlaced display, FCCL is ignored. FCCL 0 Does not initialize the field counter on the rising edge of EXVS. 1 Initializes the field counter on the rising edge of EXVS, setting the counter to the even field.
8	Steal Control	SC	Defines the relationship between the CLK and SCLK signals when the AGDC is in the DT mode (using video RAMs). If the AGDC is in cycle steal mode, SC is ignored. SC 0 CLK does not equal SCLK. 1 CLK and SCLK are the same
9	Refresh Enable	RE	Defines whether the AGDC is to generate DRAM refresh addresses. RE 0 The AGDC does not generate DRAM refresh addresses 1 The AGDC generates DRAM refresh address while HS is active (high)
10	Interlace	IN	Defines whether interlaced or non-interlaced display mode is to be used. IN 0 Non-interlaced display 1 Interlaced display

Figure 21. Display Control Register (cont)

Bit	Flag Name	Abbreviation	Function
11, 12, 13	Display Address Proceedings	DAD+	Defines how the AGDC's 24-bit display address register is to be incremented during each display cycle. The register is not incremented while BLANK is active. It is incremented ast each display cycle (two SCLK periods) in the DT (VRAM) mode or each time a display cycle is started in the CS (cycle steal) mode. DAD+ — Increment 000 DAD+1 — DAD → DAD+1 → DAD+2 → DAD+3 → DAD+4 . . . 001 DAD+2 — DAD → DAD+2 → DAD+4 → DAD+6 → DAD+8 . . . 010 DAD+4 — DAD → DAD+4 → DAD+8 → DAD+12 → DAD+16 . . . 011 DAD+8 — DAD → DAD+8 → DAD+16 → DAD+24 → DAD+32 . . . 100 DAD+16 — DAD → DAD+16 → DAD+32 → DAD+48 → DAD+64 . . . 101 DAD+32 — DAD → DAD+32 → DAD+64 → DAD+96 → DAD+128 . . . 110 DAD+1/4 — DAD → DAD → DAD → DAD → DAD+1 → DAD+1 →. . . 111 DAD+1/2 — DAD → DAD → DAD+1 → DAD+1 → DAD+2 → DAD+2 . .
14	Data Transfer Timing	DTT	Defines the output timing for the DT (data transfer) signal when using VRAMs. DTT is ignored in the cycle steal mode. DTT 0 DT is generated (active low) when any of the following conditions is true. (a) At the start of the screen display (at the first rising edge of the BLANK signal in a frame) (b) At the start of each horizontal scan line (at the falling edge of BLANK) (c) When all 8 AC register-defined bits of the 24-bit display address are 0 (when the lower 8 bits are 00H). 1 DT is generated when any of the following conditions is true. (a) At the start of the screen display (at the first rising edge of the BLANK signal in a frame) (b) When all 8 AC register-defined bits of the 24-bit display address are 0.
15	Data Transfer Mode	DTM	Defines the display cycle generation timing. Data transfer mode is normally used with video RAMs and cycle steal mode with other types of memories. DTM 0 Sets the cycle steal (SC) mode. The DT/DISP pin outputs the DISP signal (active low). Display and drawing cycles alternate in this mode. 1 Sets the data transfer (DT) mode. The DT/DISP pin outputs the DT signal (active low).

Figure 22. Cursor Position Select

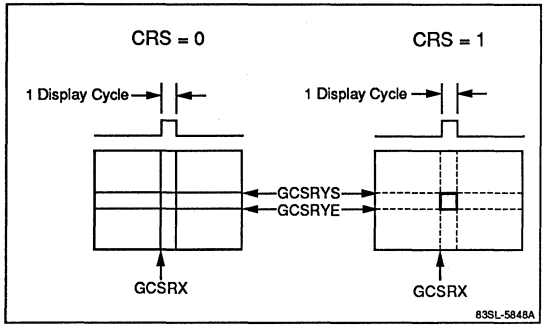


Figure 23. Horizontal and Vertical Timing Parameters

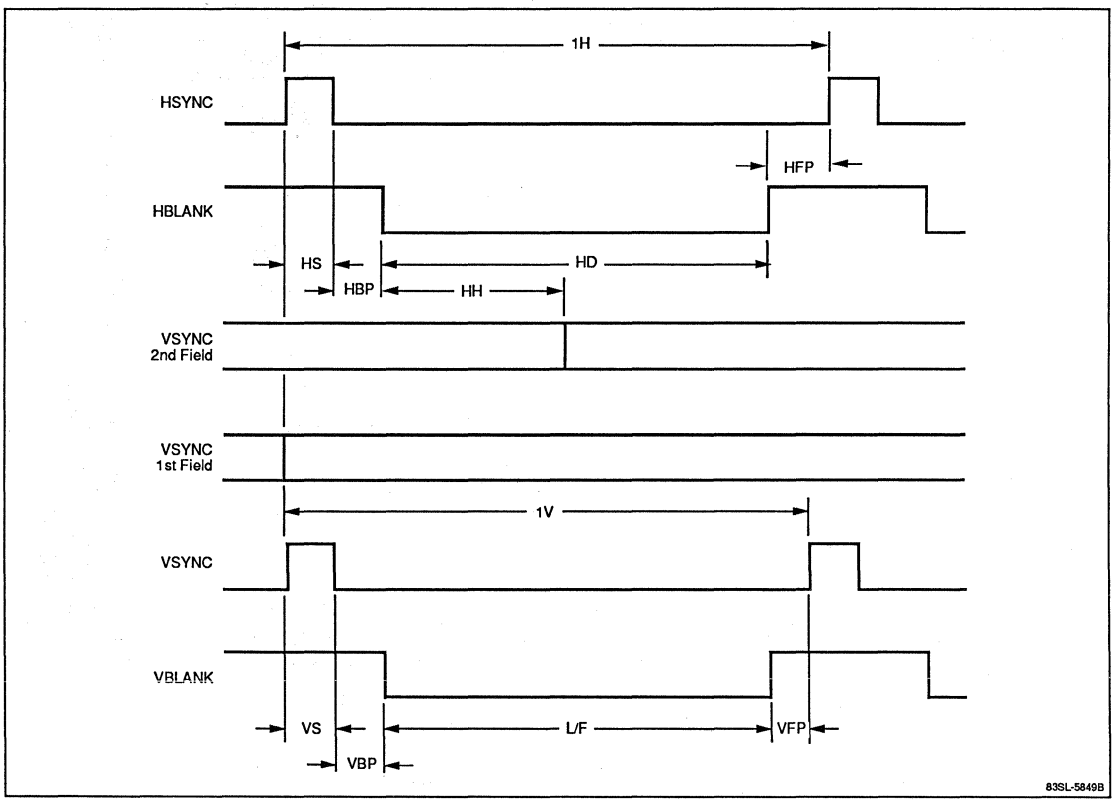


Table 3. List of DRAW Commands

Commands		Absolute Coordinates	Relative Coordinates
Data Read Commands	Coordinate value read	READ_DP	
	Color information read	READ_COL	
Graphics Drawing Commands	Dot	DOT_D	
		A_DOT_M	R_DOT_M
	Straight line	A_LINE_M0	R_LINE_M0
		A_LINE_M1	R_LINE_M1
		A_LINE_M2	R_LINE_M2
		A_LINE_D0	R_LINE_D0
		A_LINE_D1	R_LINE_D1
		A_LINE_D2	R_LINE_D2
		A_LINE_D3	
	Rectangle	A_REC	R_REC
	Circle	CRL	
	Arc	CARC	
	Circle sector	CSEC	
	Circle segment (bow)	CSEG	
	Ellipse	ELPS	
	Ellipse arc	EARC	
	Ellipse sector	ESEC	
	Ellipse segment (bow)	ESEG	
Fill Commands	Arbitrary area fill	PAINT	
	Triangle fill	A_TRI_FILL	
	Trapezoid fill	A_TRA_FILL	
	Rectangle fill	A_REC_FILL_C	
		A_REC_FILL_A	R_REC_FILL
	Circle fill	CRL_FILL	
	Ellipse fill	ELPS_FILL	
Copy Commands	Physical address to physical address	A_COPY_AA	
	Coordinate to physical address	A_COPY_CA	
	Physical address to coordinate	A_COPY_AC	
	Coordinate to coordinate	A_COPY_CC	
	Copy function extensions	90°_COPY	
		SL_COPY	
		FR_ES_COPY	
		ES_COPY	
PUT/GET Commands	System memory to display memory	PUT_A	
		PUT_C	
	Display memory to system memory	GET_A	
		GET_C	
	GET function extensions	90°_GET	

Table 4. DRAW Command Descriptions

Commands	Name	Description
Data Read Commands	READ_DP Read Drawing Pointer	The current drawing pointer coordinates (X#, Y#) are output to the X and Y registers to be read by the host CPU.

6FH								6EH							
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

READ_COL Read Color	The color information in each memory plane corresponding to the coordinates (X, Y) pointed to by the X and Y registers is placed in the DX register to be read by the host CPU. The least significant bit corresponds to the first plane, the most significant bit to the 16th plane.

6FH								6EH							
1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0

Graphics Drawing Commands	DOT_D Dot Direct	A dot is drawn at the current drawing pointer coordinates (X#, Y#). The drawing pointer (X#, Y#) remains unchanged. The bit pointer of the PNTCNT register shifts from the LSB by 1 bit toward the MSB .

6FH								6EH							
0	0	0	0	1	0	0	0	0	IP	0	PXEN	BPPX		0	0

A_DOT_M Absolute Dot with Move	A dot is drawn at the (X, Y) coordinates pointed to by the X and Y registers, respectively. The drawing pointer (X#, Y#) changes to (X, Y). The bit pointer of the PNTCNT register shifts from the LSB by 1 bit toward the MSB .

6FH								6EH							
0	0	0	0	1	1	0	0	0	IP	0	PXEN	BPPX		0	0

R_DOT_M Relative Dot with Move	A dot is drawn at the (X+DX, Y+DY) defined by the X, DX, Y, and DY registers, respectively. The drawing pointer (X#, Y#) changes to (X+DX, Y+DY). The bit pointer of the PNTCNT register shifts from the LSB by 1 bit toward the MSB .

6FH								6EH							
0	0	0	1	0	0	0	0	0	IP	0	PXEN	BPPX		0	0

Absolute Line with Move 0, 1, 2	A straight line is drawn from coordinates (X, Y) pointed to by the X and Y registers to (XE, YE) pointed to by the XE and YE registers. WEP determines whether the end point (XE, YE) is drawn. The drawing pointer (X#, Y#) changes to (XE, YE). The commands differ as follows.
A_LINE_M0	The X and Y registers change to the values in the XE and YE registers. The XE, YE, XS, and YS registers do not change value.

6FH								6EH							
0	0	0	1	0	1	0	0	ED	IP	ES	PXEN	BPPX (PL)		ESH	WEP

Table 4. DRAW Command Descriptions (cont)

Commands	Name	Description
Graphics Drawing Commands (cont)	A_LINE_M1	The X, Y, XE, YE, XS, and YS registers do not change value.

6FH

0	0	0	1	1	0	0	0

6EH

ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

A_LINE_M2				The XS and YS registers change to the values in the X and Y registers. The X and Y registers change to the values in the XE and YE registers. The XE and YE registers do not change value.	

6FH

0	0	0	1	1	1	0	0

6EH

ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

Absolute Line Direct 0, 1, 2, 3				A straight line is drawn from the current drawing pointer (X#, Y#) to the coordinates (XE, YE) pointed to by the XE and YE registers, respectively. The values in the X and Y registers should be equal to the drawing pointer (X#, Y#) in order to execute these commands. The drawing of the end point (XE, YE) is determined by WEP. The commands differ as follows.	
A_LINE_D0				The drawing pointer (X#, Y#) and X and Y register values change to XE and YE. The values in the XE, YE, XS, and YS registers do not change.	

6FH

0	0	1	0	0	0	0	0

6EH

ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

A_LINE_D1				The values in the X, Y, XE, YE, XS, and YS registers do not change. The drawing pointer (X#, Y#) changes to (XE, YE).	

6FH

0	0	1	0	0	1	0	0

6EH

ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

A_LINE_D2				The values in the XS and YS registers change to those in the X and Y registers. The X and Y register values change to those in the XE and YE registers. The XE and YE register values do not change. The drawing pointer (X#, Y#) changes to (XE, YE).	

6FH

0	0	1	0	1	0	0	0

6EH

ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

Table 4. DRAW Command Descriptions (cont)

Commands	Name	Description
Graphics Drawing Commands (cont)	A_LINE_D3	The values in the XS and YS registers are used for the end point of the line. The drawing pointer changes to (XS, YS). The values in the X and Y registers change to those in the XS and YS registers. The XE, YE, XS, and YS register values do not change.

	6FH							6EH						
0	0	1	0	1	1	0	0	ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

Relative Line with Move 0, 1, 2	A straight line is drawn from coordinates (X, Y) pointed to by the X and Y registers to the point (X+DX, Y+DY) with DX and DY contained in their respective registers. Drawing of the end point is determined by the WEP bit.
R_LINE_M0	The drawing pointer (X#, Y#) changes to (X+DX, Y+DY). The X and Y registers change to (X+DX, Y+DY). The DX, DY, XS, and YS register values do not change.

	6FH							6EH						
0	0	1	1	0	0	0	0	ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

R_LINE_M1	The drawing pointer (X#, Y#) changes to (X+DX, Y+DY). The X, Y, DX, DY, XS, and YS register values do not change.

	6FH							6EH						
0	0	1	1	0	1	0	0	ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

R_LINE_M2	The drawing pointer (X#, Y#) changes to (X+DX, Y+DY). The XS, and YS registers change to (X, Y). The X and Y registers change to (X+DX, Y+DY). The DX and DY register values do not change.

	6FH							6EH						
0	0	1	1	1	0	0	0	ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

R Line Direct 0, 1, 2	A straight line is drawn from the drawing pointer (X#, Y#) to the coordinates (X+DX, Y+DY) pointed to by the DX and DY registers. The drawing of the end point is determined by the WEP bit. The drawing pointer changes to (X+DX, Y+DY).
R_LINE_D0	The X and Y registers change to (X+DX, Y+DY). The DX, DY, XS, and YS register values do not change.

	6FH							6EH						
0	0	1	1	1	1	0	0	ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

Table 4. Drawing Command Descriptions (cont)

Commands	Name	Description
Graphics Drawing Commands (cont)	R_LINE_D1	The X Y, DX, DY, XS, and YS register values do not change .

6FH								6EH						
0	1	0	0	0	0	0	0	ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

R_LINE_D2	The XS and YS registers change to (X, Y). The X and Y registers change to (X+DX, Y+DY). The DX and DY register values do not change.

6FH								6EH						
0	1	0	0	0	1	0	0	ED	IP	ES	PXEN	BPPX (PL)	ESH	WEP

A_REC Absolute Rectangle	A rectangle with horizontal and vertical sides parallel to the X and Y axes is drawn with the diagonal vertices at coordinates (X, Y) and (XS, YS) pointed to by the X, Y, XS, and YS registers, respectively. The drawing pointer (X#, Y#) changes to (X, Y).

6FH								6EH						
0	1	0	0	1	0	0	0	0	IP	ES	PXEN	BPPX	ESH	0

R_REC Relative Rectangle	A rectangle with horizontal and vertical sides parallel to the X and Y axes is drawn with the diagonal vertices at coordinates (X, Y) and (X+DX, Y+DY). The drawing pointer (X#, Y#) changes to (X, Y).

6FH								6EH						
0	1	0	0	1	1	0	0	0	IP	ES	PXEN	BPPX	ESH	0

CRL Circle	A circle is drawn counterclockwise with the center at (XC, YC) pointed to by the XC and YC registers and with radius DX defined by the DX register. The drawing pointer (X#, Y#) changes to (XC, YC+DX). The circle is started from (XC, YC+DX). DX must be > 0.

6FH								6EH						
0	1	0	1	0	0	0	0	0	IP	0	PXEN	BPPX	0	0

CARC Circle Arc	A circular arc is drawn from coordinates (XS, YS) to (XE, YE) with the center of the circle at (XC, YC) and radius DX. These are pointed to by the XS, YS, XE, YE, XC, YC, and DX registers, respectively. The drawing pointer changes to (XE, YE). DX must be > 0.

6FH								6EH						
0	1	0	1	0	1	0	0	CF	IP	0	PXEN	BPPX	0	WEP

CSEC Circle Sector	A circular sector is drawn with the center at (XC, YC), DX the radius, (XS, YS) the starting point, and (XE, YE) the ending point. The drawing pointer changes to (XS, YS). DX must be > 0.

6FH								6EH						
0	1	0	1	1	0	0	0	CF	IP	0	PXEN	BPPX	0	0

3

Table 4. DRAW Command Descriptions (cont)

Commands	Name	Description
Graphics Drawing Commands (cont)	CSEG Circle Segment	A circle segment is drawn with the arc starting at (XS, YS), ending at (XE, YE), the circle center at (XC, YC), and with radius DX. A line segment connects the arc starting and ending point to complete the segment. The drawing pointer (X#, Y#) changes to (XS, YS). The radius DX must be > 0.

	6FH										6EH			
0	1	0	1	1	0	1	0	CF	IP	0	PXEN	BPPX	0	0

ELPS Ellipse	An ellipse with major and minor axes parallel to the coordinate axes is drawn counterclockwise with the center at (XC, YC), the Y-direction radius DY, and the ratio of the squares of the X-axis and Y-axis radii in DH and DV such that $DX^2/DY^2 = DH/DV$. The drawing pointer (X#, Y#) changes to (XC, YC+DY). The radius DY must be > 0.

	6FH										6EH			
0	1	0	1	1	1	0	0	0	IP	0	PXEN	BPPX	0	0

EARC Ellipse Arc	An elliptical arc with major and minor axes parallel to the coordinate axes is drawn from (XS, YS) to (XE, YE) with the ellipse center at (XC, YC), Y-direction radius DY, and the ratio of the squares of the X- and Y-direction radii $DX^2/DY^2 = DH/DV$. The drawing pointer (X#, Y#) changes to (XE, YE). The radius DY must be > 0.

	6FH										6EH			
0	1	1	0	0	0	0	0	CF	IP	0	PXEN	BPPX	0	WEP

ESEC Ellipse Sector	An elliptical sector with major and minor axes parallel to the coordinate axes is drawn from (XS, YS) to (XE, YE) with the ellipse center at (XC, YC), Y-direction radius DY, and the ratio of the squares of the X- and Y-direction radii $DX^2/DY^2 = DH/DV$. The drawing pointer (X#, Y#) changes to XS, YS). The radius DY must be > 0.

	6FH										6EH			
0	1	1	0	0	1	0	0	CF	IP	0	PXEN	BPPX	0	0

ESEG Ellipse Segment	An elliptical segment with major and minor axes parallel to the coordinate axes is drawn from (XS, YS) to (XE, YE) with the ellipse center at (XC, YC), Y-direction radius DY, and the ratio of the squares of the X- and Y-direction radii $DX^2/DY^2 = DH/DV$. The drawing pointer (X#, Y#) changes to (XS, YS).

	6FH										6EH			
0	1	1	0	0	1	0	1	CF	IP	0	PXEN	BPPX	0	0

Table 4. DRAW Command Descriptions (cont)

Commands	Name	Description
Fill and Paint Commands	PAINT	A boundary-point search is carried out starting from coordinates (X, Y) and the resulting enclosed area is filled with a solid or tiling pattern. When PMOD = 0, the boundary colors are set into the DX register. The area to be painted must be enclosed within the clipping rectangle and the CLIP register must be set to 00.

6FH								6EH							
0	1	1	0	1	0	0	0	TL	0	1	SS	0	PMOD	0	0

A_TRI_FILL Absolute Triangle Fill	A triangular region with vertices at (X, Y), (XS, YS), and (XC, YC) is filled with the tiling pattern. Y, YS, and YC must not be equal to each other.

6FH								6EH							
0	1	1	0	1	1	0	0	TL	0	1	SS	WL	WR	0	0

A_TRA_FILL Absolute Trapezoid Fill	A trapezoidal area with its parallel sides (upper and lower) defined by line segments connecting (X, Y) to (XS, Y) and (YS, YE) to (XE, YE), where YS is an X-axis value, is filled with the tiling pattern.

6FH								6EH							
0	1	1	1	0	0	0	0	TL	0	1	SS	WL	WR	0	0

R_TRA_FILL Relative Trapezoid Fill	A trapezoidal area with its upper parallel side defined by the line segment connecting (X, Y) to (XS, Y), a height of DV+1 dots above the lower side line segment connecting X+DX and XS+XC, is filled with the tiing pattern.

6FH								6EH							
0	1	1	1	0	1	0	0	TL	0	1	SS	WL	WR	0	0

A_REC _ FILL_ C Absolute Rectangle Fill by Coordinates	A rectangle with vertical and horizontal sides parallel to the coordinate axes is filled with the tiling pattern. The diagonal vertices of the rectangle are (X, Y) and (XS, YS).

6FH								6EH							
1	0	0	0	1	1	0	0	TL	0	1	SS	WL	WR	FAST	0

A_REC_FILL_A Absolute Rectangle Fill by Address	A rectangle with vertical and horizontal sides parallel to the coordinate axes is filled with the tiling pattern. The rectangle is defined by the number of dots in the horizontal direction DH+1, the number of dots in the vertical direction DV+1, the starting address (physical address) EAD1, and the bit position in the starting address dAD1.

6FH								6EH							
1	0	0	0	1	1	1	0	0	0	1	1	1	1	1	0

3

Table 4. DRAW Command Descriptions (cont)

Commands	Name	Description
Fill and Paint Commands (cont)	R_REC_FILL Relative Rectangle Fill by Coordinates	A rectangle with vertical and horizontal sides parallel to the coordinate axes is filled with the tiling pattern. The rectangle is defined by the starting point (X, Y), the horizontal width DX, and the vertical height DY. The diagonal vertices are at (X, Y) and (X+DX, Y+DY).

	6FH								6EH							
1	0	0	1	0	0	0	0	TL	0	1	SS	WL	WR	FAST	0

Name	Description
CRL_FILL Circle Fill	A circle with its center at (XC, YC) and a radius of DX is filled with the tiling pattern. Points on the circumference are filled. The filling starts from the top of the circle and proceeds downward.

	6FH								6EH							
0	1	0	1	0	0	0	0	TL	0	1	SS	1	1	0	0

Name	Description
ELPS_FILL Ellipse Fill	An ellipse with its major and minor axes parallel to the coordinate axes, center at (XC, YC), Y-direction radius DY, and ratio of the squares of the X- and Y-direction radii DX^2/DY^2 = DH/DV is filled with the tiling pattern. The filling starts from the the top of the ellipse and proceeds downward.

	6FH								6EH							
0	1	0	1	1	1	0	0	TL	0	1	SS	1	1	0	0

	Name	Description
Copy Commands	A_COPY_AA Absolute Copy Address to Address	A rectangular area of memory starting from physical location EAD2 and bit position dAD2, with horizontal size DH+1 dots and vertical size DV+1 dots, is transferred to the rectangular area of memory starting from EAD1 and bit position dAD1.

	6FH								6EH							
0	1	1	1	1	0	0	0	ESE	REV	ROT	0	SD_SEL		FAST	0

Name	Description
A_COPY_CA Absolute Copy Coordinate to Address	A rectangular area of display memory starting from (XS, YS), with horizontal size DH+1 dots and vertical size DV+1 dots, is transferred to the rectangular area of memory starting from physical address EAD1 and bit position dAD1.

	6FH								6EH							
0	1	1	1	1	1	0	0	ESE	REV	ROT	0	SD_SEL		FAST	0

Name	Description
A_COPY_AC Absolute Copy Address to Coordinate	A rectangular area of display memory starting from physical address EAD2 and bit position dAD2, with horizontal size DH+1 dots and vertical size DV+1 dots, is transferred to the rectangular area of memory starting from (X, Y).

	6FH								6EH							
1	0	0	0	0	0	0	0	ESE	REV	ROT	0	SD_SEL		FAST	0

Table 4. DRAW Command Descriptions (cont)

Commands	Name	Description
Copy Commands (cont)	A_COPY_CC Absolute Copy Coordinate to Coordinate	A rectangular area of display memory starting from (XS, YS), with horizontal size DH+1 dots and vertical size DV+1 dots, is transferred to the rectangular area of memory starting at (X, Y).

6FH								6EH						
1	0	0	0	0	1	0	0	ESE	REV	ROT	0	SD_SEL	FAST	0

Copy Function Extensions		The function of each COPY command can be extended by changing the lower 2 bits of the command code. This extension is defined in the lower byte (6EH) of the command register.
	90°_COPY 90° Rotation Copy	The transferred memory area is rotated 90° counterclockwise.

6EH						
ESE	REV	ROT	1	SD_SEL	0	0

	SL_COPY Slant Copy	The data in a rectangular area of display memory is slanted by DX in the X-direction to the change in the Y-direction

6EH						
ESE	REV	ROT	0	SD_SEL	0	1

	FR_ES_COPY Free Angle Rotation, Enlarge/Shrink Copy	The rectangular data from the source area is transferred to a parallelogram at the destination area in display memory. DY and DX determine the angle for the horizontal side, XE and YE for the vertical side. MAGH and MAGV determine the horizontal and vertical enlargement or shrink factors.

6EH						
ESH	ESV	FS	1	SD_SEL	1	0

	ES_COPY Enlarge/Shrink Copy	The rectangular data from the source area is transferred to a rectangular area at the destination in display memory and enlarged or shrunk in the horizontal and/or vertical direction. MAGH and MAGV determine the horizontal and vertical scale factors.

6EH						
ESH	REV	ROT	ESV	SD_SEL	1	1

3

Table 4. DRAW Command Descriptions (cont)

Commands	Name	Description
PUT/GET Commands	PUT_A Put Data to Address Field	Transfers data from the PGPORT register to a rectangular area of display memory starting from word address EAD1 and bit position dAD1 with horizontal width DH+1 dots and vertical height DV+1 dots.

	6FH								6EH					
1	0	0	1	0	1	0	0	0	REV	ROT	0	SD_SEL	1	1

	PUT_C Put Data to Coordinate Field	Transfers data from the PGPORT register to a rectangular area of display memory starting from (X, Y) with horizontal width DH+1 dots and vertical height DV+1 dots.

	6FH								6EH					
1	0	0	1	1	0	0	0	0	REV	ROT	0	SD_SEL	1	1

	GET_A Get Data from Address Field	Transfers data to the PGPORT register from a rectangular area of display memory starting from word address EAD1 and bit position dAD1 with horizontal width DH+1 dots and vertical height DV+1 dots.

	6FH								6EH					
1	0	0	1	0	1	1	0	0	0	0	0	SD_SEL	1	0

	GET_C Get Data from Coordinate Field	Transfers data to the PGPORT register from a rectangular area of display memory starting from (X, Y) with horizontal width DH+1 dots and vertical height DV+1 dots.

	6FH								6EH					
1	0	0	1	1	0	1	0	0	0	0	0	SD_SEL	1	1

	Get Function Extensions 90°_COPY	Data in the rectangular area of display memory is rotated through 90° and transferred to the PGPORT register.

	6EH						
0	REV	ROT	1	SD_SEL	1	0

Figure 24. Graphics Drawing Commands

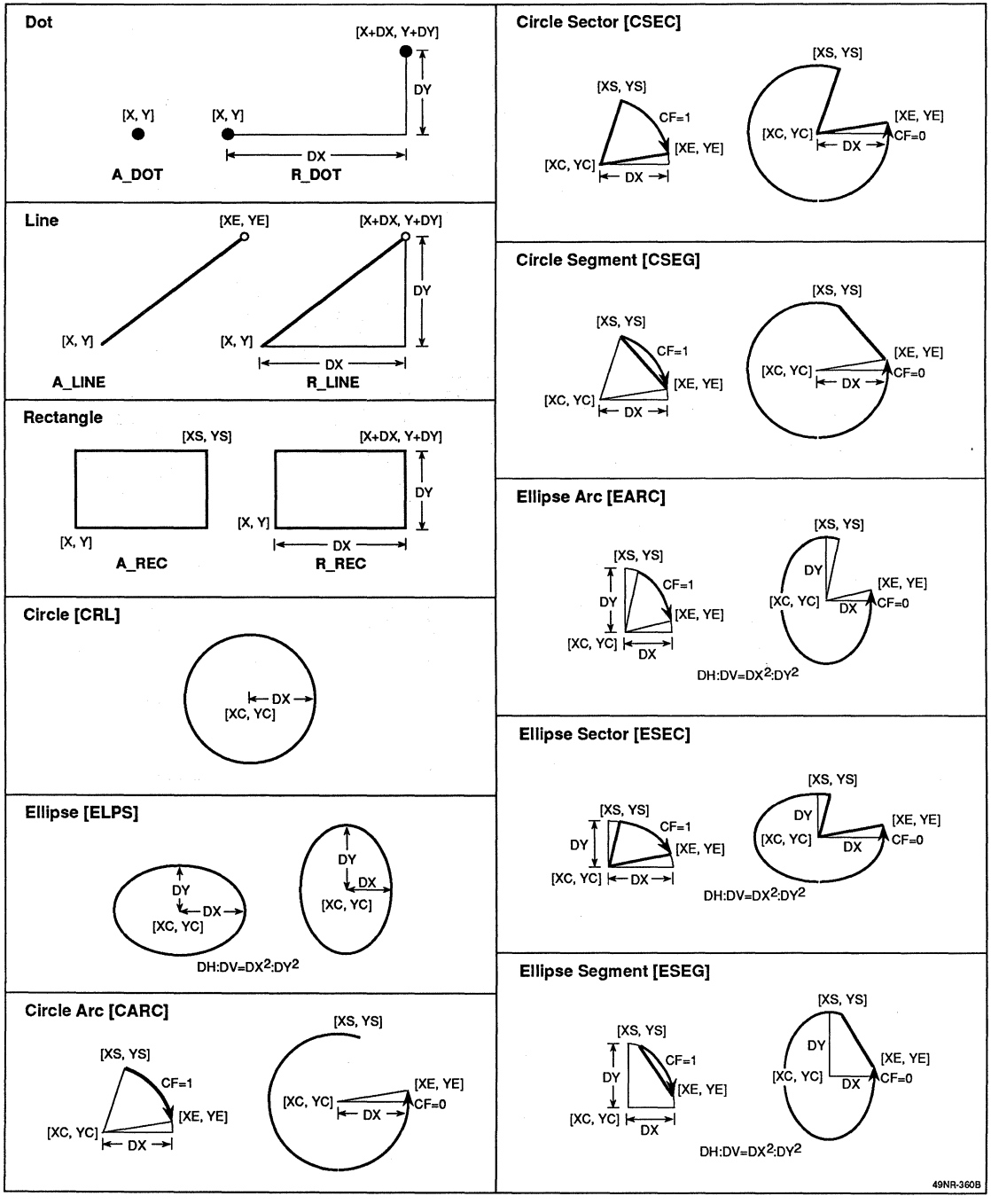
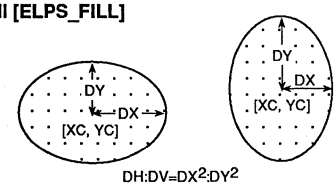


Figure 25. Fill and Paint Commands

Paint

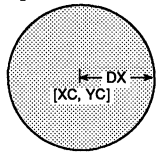
DX: Boundary Color

Ellipse Fill [ELPS_FILL]

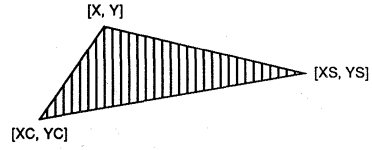


DH:DV=DX²:DY²

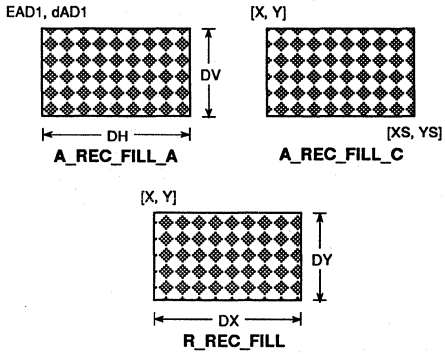
Circle Fill [CRL_FILL]



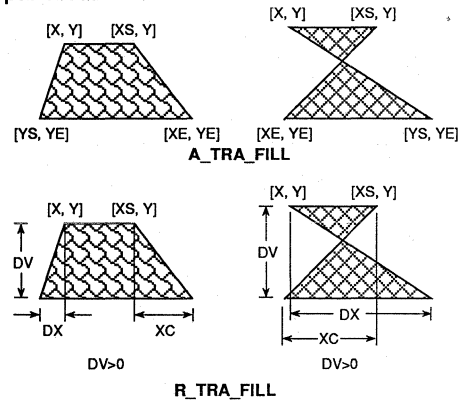
Triangle Fill [A_TRI_FILL]



Rectangle Fill



Trapezoid Fill



49NR-361B

Figure 26. Copy Commands; Copy, Rotate, Slant

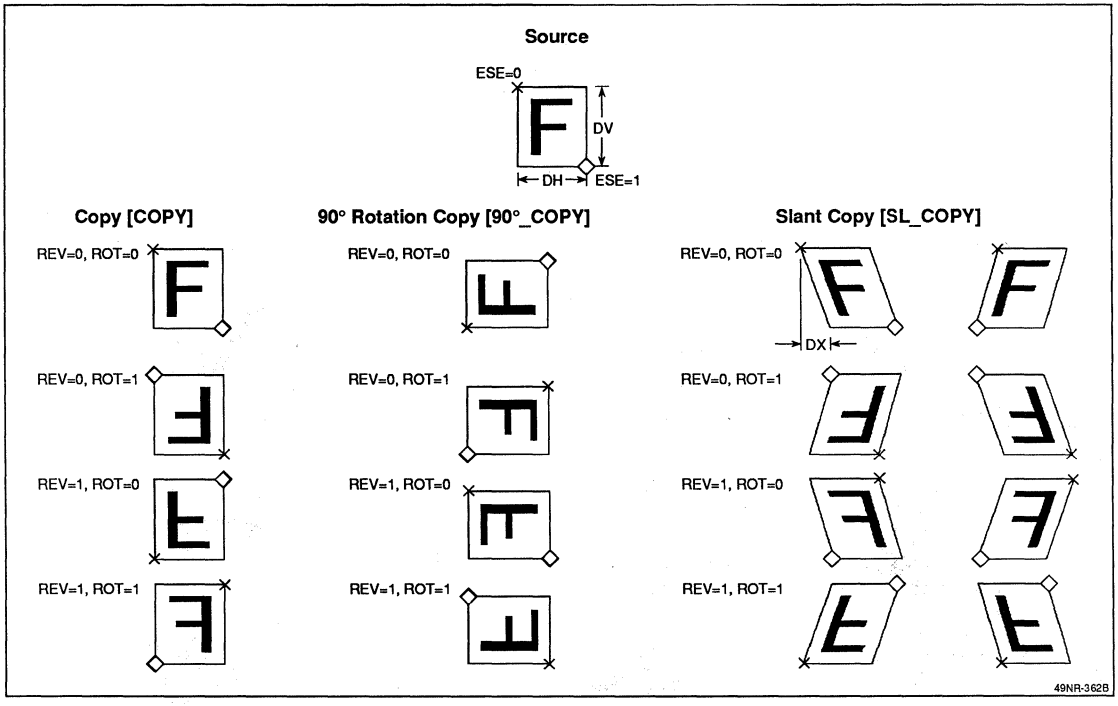


Figure 27. Copy Commands; Enlarge/Shrink, Rotate

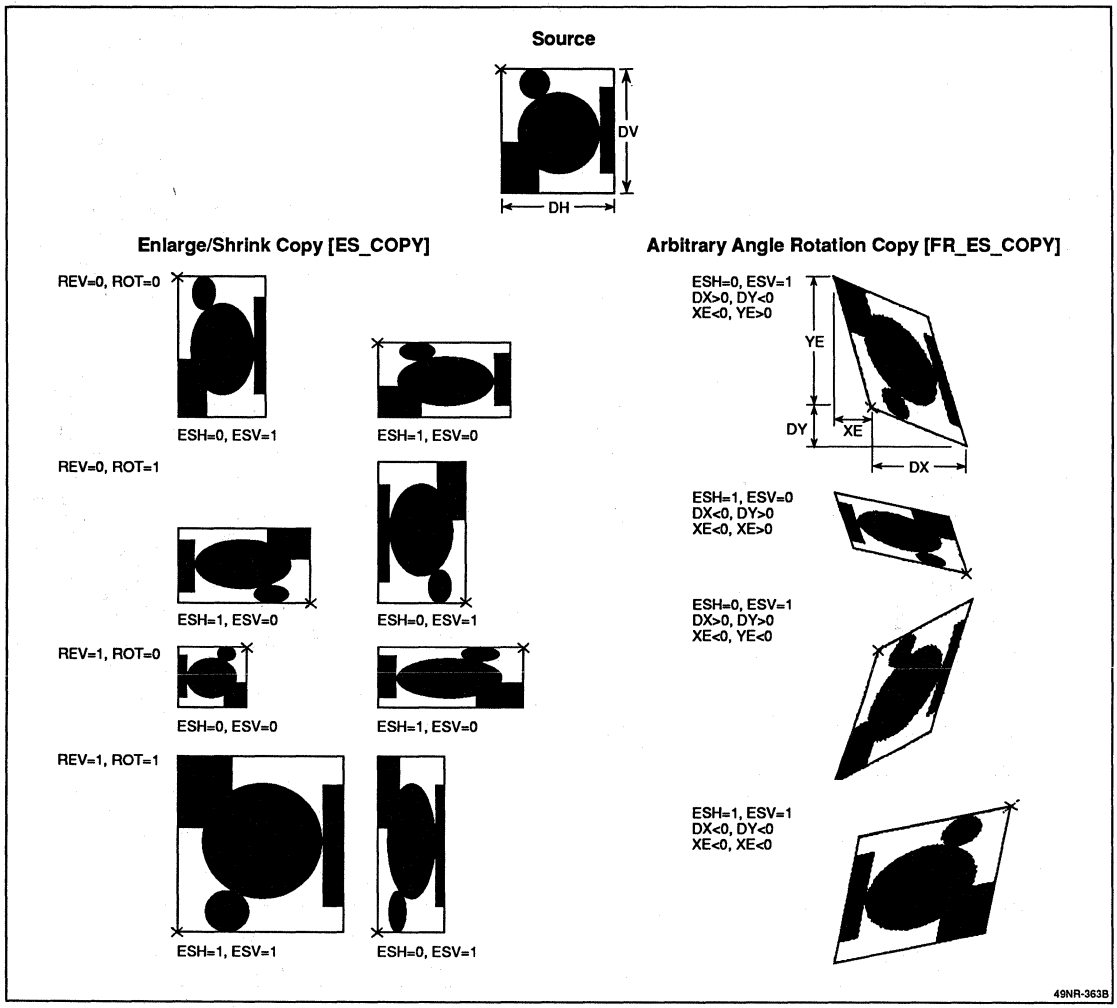


Table 5. DRAW Command Summary

Command	Opcode (Hex)	Parameters
READ_DP	04	None
READ_COL	9C	X, Y

B7			Operation Flags				B0	
0	0	0	0	0	0	0	0	6EH

Command	Opcode (Hex)	Parameters
DOT_D	08	None
A_DOT_M	0C	X,Y
R_DOT_M	10	DX, DY

B7			Operation Flags			B0	
0	IP	0	PXEN	BPPX	0	0	6EH

Command	Opcode (Hex)	Parameters
A_LINE_M0	14	X, Y, XE, YE
_M1	18	
_M2	1C	
A_LINE_D0	20	XE, YE
_D1	24	
_D2	28	
_D3	2C	
R_LINE_M0	30	X, Y, DX, DY
_M1	34	
_M2	38	
R_LINE_D0	3C	DX, DY
_D1	40	
_D2	44	

B7			Operation Flags			B0	
ED	IP	ES	PXEN	BPPX	ESH	WEP	6EH
				(PL)			

Command	Opcode (Hex)	Parameters
A_REC	48	X, Y, XS, YS
R_REC	4C	X, Y, DX, DY

B7			Operation Flags			B0	
0	IP	ES	PXEN	BPPX	ESH	0	6EH

Command	Opcode (Hex)	Parameters
CRL	50	XC, YC, DX

B7			Operation Flags			B0	
0	IP	0	PXEN	BPPX	0	0	6EH

Command	Opcode (Hex)	Parameters
CARC	54	XC, YC, DX, XS, YS, XE, YE

B7			Operation Flags			B0	
CF	IP	0	PXEN	BPPX	0	WEP	6EH

Command	Opcode (Hex)	Parameters
CSEC	58	XC, YC, DX, XS, YS, XE, YE
CSEG	5A	

B7			Operation Flags			B0	
CF	IP	0	PXEN	BPPX	0	0	6EH

Command	Opcode (Hex)	Parameters
ELPS	5C	XC, YC, DY, DH, DV

B7			Operation Flags			B0	
0	IP	0	PXEN	BPPX	0	0	6EH

Command	Opcode (Hex)	Parameters
EARC	60	XC, YC, DY, DH, DV, DX, XS, YS, XE, YE

B7			Operation Flags			B0	
CF	IP	0	PXEN	BPPX	0	WEP	6EH

Command	Opcode (Hex)	Parameters
ESEC	64	XC, YC, DY, DH, DV, DX, XS, YS, XE, YE
ESEG	65	

B7			Operation Flags			B0	
CF	IP	0	PXEN	BPPX	0	0	6EH

Command	Opcode (Hex)	Parameters
PAINT	68	X, Y, (DX)

B7			Operation Flags				B0	
TL	0	1	SS	0	PMOD	0	0	6EH

Command	Opcode (Hex)	Parameters
A_TRI_FILL	6C	X, Y, XS, YS, XC, YC
A_TRA_FILL	70	X, Y, XS, YS, XE, YE
R_TRA_FILL	74	X, Y, XS, DX, XC, DV

B7			Operation Flags				B0	
TL	0	1	SS	WL	WR	0	0	6EH

Command	Opcode (Hex)	Parameters
A_REC_FILL_C	8C	X, Y, XS, YS

B7			Operation Flags				B0	
TL	0	1	SS	WL	WR	FAST	0	6EH

Command	Opcode (Hex)	Parameters
A_REC_FILL_A	8E	EAD1, dAD1, DH, DV

B7			Operation Flags				B0	
0	0	1	1	1	1	1	0	6EH

Command	Opcode (Hex)	Parameters
R_REC_FILL	90	X, Y, DX, DY

B7			Operation Flags				B0	
TL	0	1	SS	WL	WR	FAST	0	6EH

3

Table 5. DRAW Command Summary (cont)

Command	Opcode (Hex)	Parameters
CRL_FILL	50	XC, YC, DX
ELPS_FILL	5C	XC, YC, DY, DH, DV

Operation Flags

B7							B0	
TL	0	1	SS	1	1	0	0	6EH

Command	Opcode (Hex)	Parameters
A_COPY_AA	78	EAD1, dAD1, EAD2, dAD2, DH, DV
_CA	7C	XS, YS, EAD1, dAD1, DH, DV
_AC	80	EAD2, dAD2, DH, DV, X, Y
_CC	84	XS, YS, X, Y, DH, DV

Operation Flags

B7						B0	
ESE	REV	ROT	0	SD_SEL	FAST	0	6EH

Command	Opcode (Hex)	Parameters
A_90°_COPY_AA	78	EAD1, dAD1, EAD2, dAD2, DH, DV
_CA	7C	XS, YS, EAD2, dAD2, DH, DV
_AC	80	EAD2, dAD2, X, Y, DH, DV
_CC	84	XS, YS, X, Y, DH, DV

Operation Flags

B7						B0	
ESE	REV	ROT	1	SD_SEL	0	0	6EH

Command	Opcode (Hex)	Parameters
A_SL_COPY_AA	78	EAD1, dAD1, EAD2, dAD2, DH, DV, DX
_CA	7C	XS, YS, EAD1, dAD1, DH, DV, DX
_AC	80	EAD2, dAD2, X, Y, DH, DV, DX
_CC	84	XS, YS, X, Y, DH, DV, DX

Operation Flags

B7						B0	
ESE	REV	ROT	0	SD_SEL	0	1	6EH

Command	Opcode (Hex)	Parameters
A_FR_ES_COPY _AA	78	EAD1, dAD1, EAD2, dAD2, DH, DV, DX, DY, XE, YE
_CA	7C	XS, YS, EAD1, dAD1, DH, DV, DX, DY, XE, YE
_AC	80	EAD2, dAD2, X, Y, DH, DV, DX, DY, XE, YE
_CC	84	XS, YS, X, Y, DH, DV, DX, DY, XE, YE

Operation Flags

B7						B0	
ESH	ESV	FS	1	SD_SEL	1	0	6EH

Command	Opcode (Hex)	Parameters
A_ES_COPY_AC	80	EAD2, dAD2, X, Y, DH, DV
_CC	84	XS, YS, X, Y, DH, DV

Operation Flags

B7						B0	
ESH	REV	ROT	ESV	SD_SEL	1	1	6EH

Command	Opcode (Hex)	Parameters
PUT_A	94	EAD1, dAD1, DH, DV
_C	98	X, Y, DH, DV

Operation Flags

B7						B0	
0	REV	ROT	0	SD_SEL	1	1	6EH

Command	Opcode (Hex)	Parameters
GET_A	96	EAD1, dAD1, DH, DV
_C	9A	X, Y, DH, DV

Operation Flags

B7						B0	
0	0	0	0	SD_SEL	1	0	6EH

Command	Opcode (Hex)	Parameters
90°_GET_A	96	EAD1, dAD1, DH, DV
_C	9A	X, Y, DH, DV

Operation Flags

B7						B0	
0	REV	ROT	1	SD_SEL	1	0	6EH

Table 6. Operation Flag Descriptions

PXEN (Pixel Drawing Enable)
BPPX (Bits per Pixel)

The plane or packed pixel display memory configuration is selected by PXEN and the number of bits in one pixel is defined by BPPX. The μPD72120 display memory data width is 16 bits. For plane configuration, PXEN = 0.

BPPX	PXEN	Bits/Pixel
xx	0	1
00	1	2
01	1	4
10	1	8
11	1	16

ES (Enlarge/Shrink)
ESH (Enlarge/Shrink Horizontally)
ESV (Enlarge/Shrink Vertically)

Select the enlarge and shrink options.

ES	ESH	ESV	Copy Operation	Drawing Operation
0	X	X	No enlarge/shrink	No enlarge/shrink
1	0	X	Horizontal shrink	Horizontal pattern shrink
1	1	X	Horizontal enlarge	Horizontal pattern enlarge
1	X	0	Vertical shrink	—
1	X	1	Vertical enlarge	—

Enlargement/Shrinkage factors.

MAGH/MAGV	ESH/ESV = 0	ESH/ESV = 1
0	1/16	16/1
1	2/16	16/2
2	3/16	16/3
3	4/16	16/4
4	5/16	16/5
5	6/16	16/6
6	7/16	16/7
7	8/16	16/8
8	9/16	16/9
9	10/16	16/10
10	11/16	16/11
11	12/16	16/12
12	13/16	16/13
13	14/16	16/14
14	15/16	16/15
15	16/16	16/16

ED (Enlargement Direction)

Defines the direction of enlargement for line drawing.

ED	Enlargement Direction
0	To the right of the line in the direction of drawing.
1	To the left of the line in the direction of drawing.

IP (Initialize Pattern Pointer)

Initializes the line pattern pointer to the first bit of the pattern register.

IP	Function
0	Pointer not initialized
1	Pointer initialized

CF (Clockwise Flag)

Defines the drawing direction for circular and elliptical arcs, sectors, and segments.

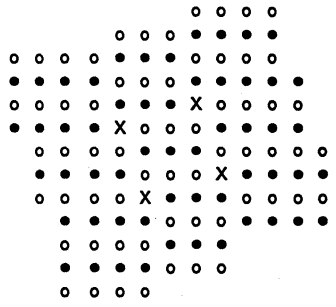
CF	Function
0	Counterclockwise
1	Clockwise

3

Table 6. Operation Flag Descriptions (cont)

Name	Description
TL (Tiling Pattern) SS (Single Source Pattern)	Defines the use of a tiling pattern in filling. TL / SS / Function 0 / 0 / Not used 0 / 1 / The pattern in the PTNCNT register is used for all planes 1 / 0 / The patterns stored in display memory are used for each plane. 1 / 1 / The same pattern stored in display memory is used for all planes. To quickly clear all planes to zero, set TL = 0 and SS = 1. When it is necessary to paint with a different color for each bit, set TL = 1 and SS = 0.
PMOD (Paint Mode)	Selects the arbitrary boundary area for the PAINT command. PMOD / Function 0 / Boundary colors are defined by the DX register. 1 / Boundaries are all the points with colors different than the starting point (X, Y).
WL (Write Left) WR (Write Right)	Defines whether the boundary points are drawn during a FILL command. WL / Function: 0 Points on left boundary are not drawn; 1 Points on left boundary are drawn WR / Function: 0 Points on right boundary are not drawn; 1 Points on right boundary are drawn
FAST (Fast)	Specifies the normal or fast mode for drawing. FAST / Function 0 / Normal speed 1 / Fast speed However, FAST mode cannot be used for all drawing operations. REC_FILL: The FAST mode cannot be used if clipping or painting with a tiling pattern. It can only be used for replacing data. COPY: The FAST mode can be used only for ordinary COPY with replace, it cannot be used with other COPY operation or with multiple sources.
ESE (Exchange Start With End)	Defines the reading order of the source data during COPY. ESE / Reading Order 0 / Upper left to lower right (left to right on each row) 1 / Lower right to upper left (right to left on each row)
REV (Reverse)	Defines the reverse drawing direction during COPY REV / Drawing Direction 0 / Left to right, top to bottom 1 / Right to left, top to bottom
ROT (Rotation)	Defines 180° rotation drawing during COPY. ROT / Function 0 / Normal 1 / 180° rotation drawing
SD_SEL (Source Destination Mode Select)	Selects the transfer mode between planes. SD SEL / Transfer Mode / Logical Operation By 00 / Multiple sources and single destination / MOD1 during read of the sources; MOD0 during write to the destination 01 / Multiple sources and single destination / MOD0 or MOD1 during read of the sources; REPLACE during write to the destination 10 / Single source and multiple desinations / MOD0 or MOD1 during write to each of the destinations. 11 / Multiple sources and multiple destinations / MOD0 or MOD1 during write to each of the destinations.

Table 6. Operation Flag Descriptions (cont)

Name	Description
FS (Fill Shortage)	When the coordinate conversion is made during the arbitrary angle rotate copy, some points may not be drawn. FS specifies whether to draw these points. FS Function 0 X Points drawn 1 X Points not drawn 
PL (Pattern Line Length)	Specifies whether a 16-bit or 32-bit pattern is to be used for line drawing. PL Pattern Length Pattern 0 16 bits PNTCNT contains the 16-bit pattern. 1 32 bits PNTCNT contains the first 16 bits of the pattern; DH contains the next 16 bits. The pattern cannot be initialized by setting IP = 0.

μPD72123
Advanced Graphics Display Controller II

Description

The μPD72123 Advanced Graphics Display Controller II (AGDC II) is an enhanced version of the μPD72120 AGDC. It executes bit map graphics processing at high speed as a peripheral to a host CPU, reducing the host's workload and improving processing efficiency.

Features

- Compatible with μPD72120 AGDC
- Higher speed drawing
  - 10-MHz drawing clock
- Large command set
  - Line drawing with graphics pen
  - Painting arbitrary or defined areas with tiling patterns
  - Enlarge, shrink, and arbitrary-angle rotate copy commands
  - Data transfer between system and display memory
- Flexible system configurations
  - Drawing can be performed on display or system memory space
  - Data bus can be used with most microprocessors
  - Independent drawing and display clocks
  - VRAM control
  - Laser printer interface controls
- Versatile drawing environment
  - Pipelined processing
  - Two X-Y coordinate systems can be defined
  - Conversion between one-dimensional and two-dimensional data arrays
  - Clipping/picking
- Improved painting performance
- Bit search command
- Vertical blank interrupt
- Bit reversal
- Drawing wait/retry timing
- CMOS technology
- Single +5-volt power supply

Ordering Information

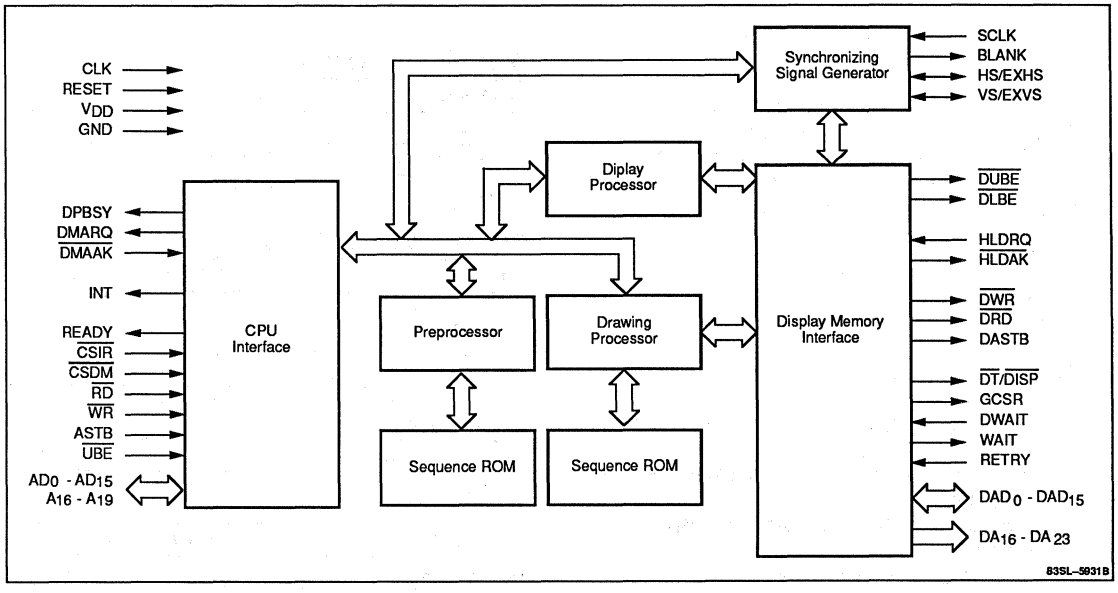
Part Number	Package
μPD72123R	132-pin ceramic PGA
μPD72123GJ-5BG	94-pin plastic miniflat
μPD72123L	84-pin PLCC

Comparison of μPD72123 and μPD72120

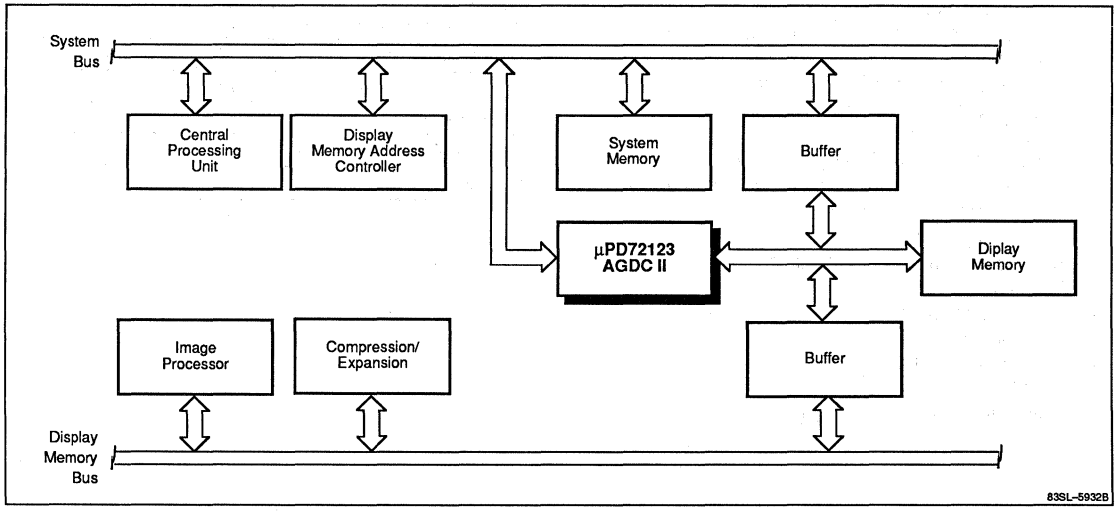
Item	μPD72123	μPD72120
Clock frequency	10 MHz	8 MHz
X-Y coordinate systems	Two	One
Line pattern	32 bits	16 bits
Raster operations (no. of operands)	Three	Two
Tiling pattern (horizontal)	32 bits	16 bits
Trapezoid fill (lower line select)	✓	—
Paint speed	Increased	—
Paint stack area	Decreased	—
Graphics pen	✓	—
Bit search	✓	—
Vertical blank interrupt	✓	—
Laser printer control	✓	—
Drawing busy output signal	✓	—
Wait drawing cycle	✓	—
Retry drawing cycle	✓	—
Bit reversal	✓	—

3

μPD72123 Block Diagram



System Configuration Example



ADVANCED COMPRESSION/EXPANSION ENGINE

Section 4
Advanced Compression/Expansion Engine

μPD72185
Advanced Compression/ Expansion Engine

Description

The μPD72185 Advanced Compression/Expansion Engine (ACEE) is a dedicated high-speed processor that performs binary image data compression and expansion using CCITT Group 3 and Group 4 algorithms. The μPD72185 supports all the coding methods specified in the CCITT T.4 and T.6 recommendations.

The μPD72185 ACEE operates on 8- or 16-bit-wide data residing in memory. It can compress image data into reduced codes and also expand reduced codes into an image. Compressed codes can be transferred to or from a separate processor or parallel peripheral through an I/O port.

The μPD72185 has a high-performance, four-stage pipelined architecture. It has separate host CPU and image data buses for maximum data throughput. The on-chip DMA controller manages all data transfer on the image bus.

The μPD72185 is designed for high-performance image compression applications, such as facsimile machines, PC FAX boards, scanners, printers, image workstations, electronic document storage systems, and magnetic and optical disk based electronic filing systems.

Features

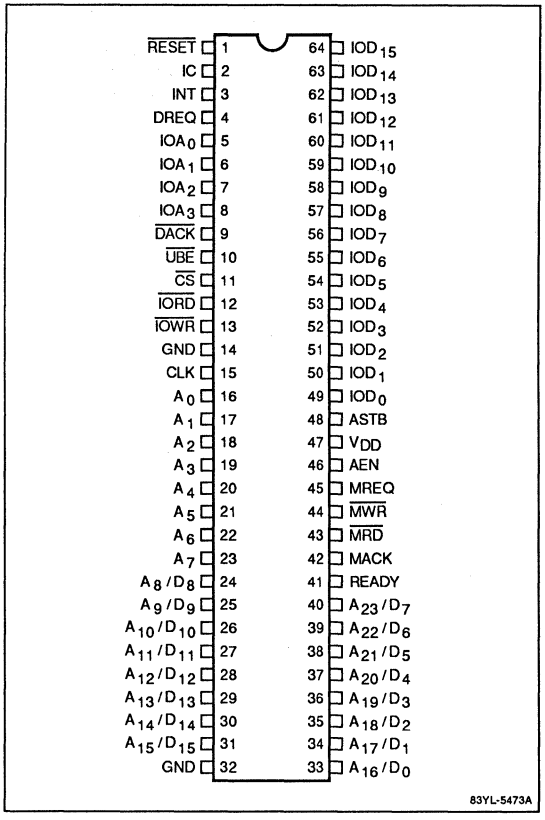
- High-speed processing
  - Compression/expansion of CCITT standard test chart (A4 size, 400 PPI x 400 LPI) in under 1 second
    Internal four-stage pipelined CPU
- Handles a variety of encoding/decoding methods: CCITT standard MH, MR, and MMR
- 32K pixels maximum per line
- Supports 32-megabyte image memory
- Image data enlargement/reduction
  - Horizontally
    x2 enlargement (on decoding)
    x1/2 reduction (on encoding)
  - Vertically
    x2 and x4 enlargement (on decoding)
    x1/2 and x1/4 reduction (on encoding)
- Bit boundary processing
- Automatic error handling on decoding
- Multitasking capability
- Dual bus system
  - Image memory side (24-bit address bus, 8/16-bit data bus)
    Host CPU side (8/16-bit data bus)
- High integration
  - On-chip DMA controller
  - On-chip refresh timing generation circuit
- CMOS process
  - Single +5-volt power supply
  - System clock: 8 MHz maximum

Ordering Information

Part No.	Package
μPD72185CW	64-pin plastic shrink DIP (750 mil)
μPD72185L	68-pin PLCC (plastic leaded chip carrier)

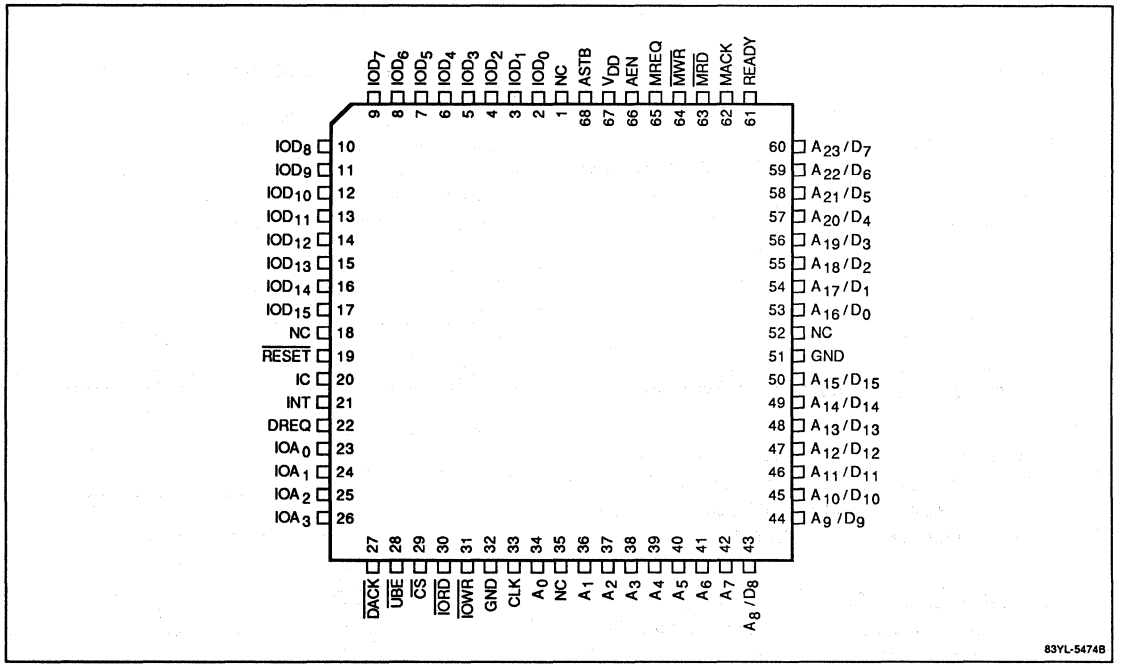
Pin Configurations

64-Pin Plastic Shrink DIP



4

68-Pin PLCC (Plastic Leaded Chip Carrier)



Pin Identification

Symbol	Function
Host Interface	
$\overline{CS}$ (Chip Select)	Active-low input signal enables I/O access to μPD72185 from host bus.
$\overline{DACK}$ (DMA Acknowledge)	Input signal from external DMA controller. Must be inactive (high) when host CPU performs I/O access to μPD72185.
DREQ (DMA Request)	Output signal to external DMA controller. Becomes active low when there is readable data or space that can be written to in the μPD72185.
INT (Interrupt Request)	Output signal to host CPU.
IOA_0-IOA_3 I/O Address)	4-bit address input selects register or register pair when host CPU performs I/O access to μPD72185.
IOD_0-IOD_{15} (I/O Data Bus)	16-bit, two-way data bus
$\overline{IORD}$ (I/O Read)	Low-level input signal when host CPU reads from μPD72185 by I/O access.
$\overline{IOWR}$ (I/O Write)	Low-level input signal when host CPU writes to μPD72185 by I/O access.
$\overline{UBE}$ (Upper Byte Enable)	When host CPU writes to μPD72185 by I/O access, byte or word transfer is specified by $\overline{UBE}$ input signal in combination with IOA_0 input.
Image Memory Interface	
A_0-A_7 (Address Bus)	Lower 8-bit address of image memory bus.
A_8-A_{15}/D_8-D_{15}, A_{16}-A_{23}/D_0-D_7 (Address/Data Bus)	Upper 16-bit address of image memory bus multiplexed with the 16-bit data bus.
AEN (Address Enable)	Output signal becomes active when μPD72185 is Bus Master on the image bus.
ASTB (Address Strobe)	High-level output signal used to latch address output from μPD72185.
MACK (Memory Acknowledge)	Active-high input signal grants μPD72185 use of image memory bus in response to MREQ signal.
$\overline{MRD}$ (Memory Read)	High-level output when μPD72185 is Bus Master on the image bus. Becomes low level when data is read from image memory. Set to high impedance when μPD72185 is Bus Slave.
MREQ (Memory Request)	High-level output signal requests use of image memory bus when μPD72185 is Bus Slave on the image bus. Becomes active for a DMA transfer between μPD72185 and image memory.

Pin Identification (cont)

Symbol	Function
$\overline{MWR}$ (Memory Write)	High-level output when μPD72185 is Bus Master on the image bus. Becomes low level when data is written to image memory. Set to high impedance when μPD72185 is Bus Slave.
READY (Ready)	Low-level input signal extends $\overline{MRD}$ and $\overline{MWR}$ cycle by adding wait states.. Signal must not be altered within setup/hold time period.
Other Pins	
CLK (Clock)	External clock input.
$\overline{RESET}$ (Reset)	System reset input. Must be held low for at least seven system clock cycles. After reset, μPD72185 becomes Bus Slave on the image bus.
IC (Internal Connection)	This pin must always be pulled up.
NC (No Connection)	No internal connections are made to this pin.
V_{DD}	Positive power supply pin.
GND (Ground)	Both ground pins must be connected.

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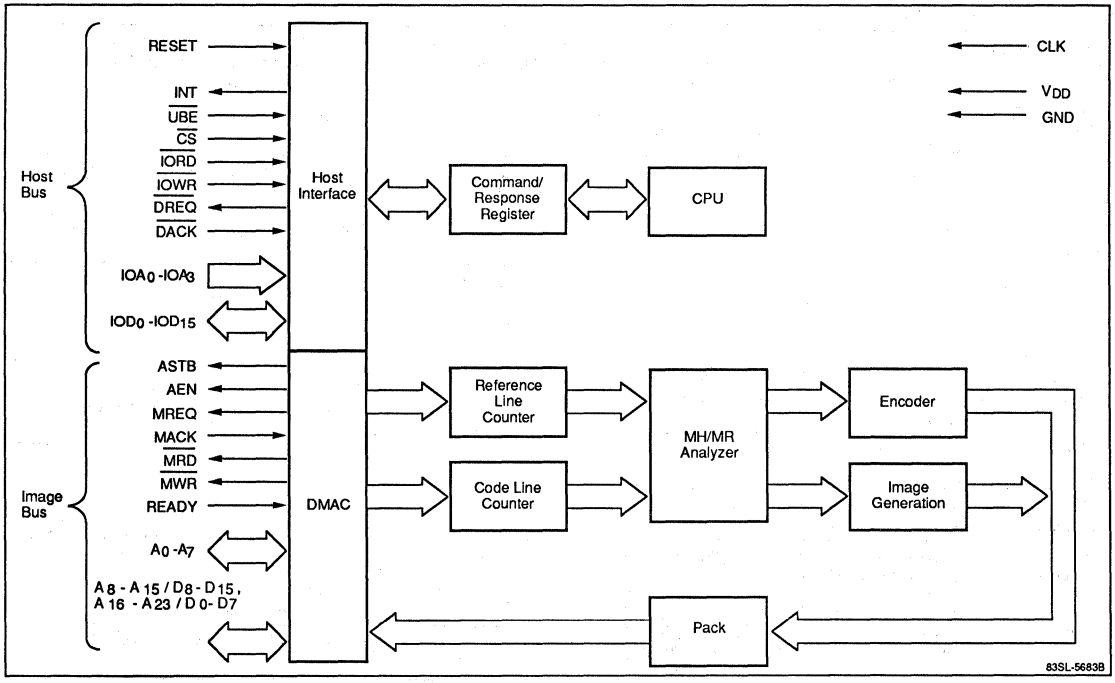
μPD72185 Block Diagram



Absolute Maximum Ratings

T_A = +25°C

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.3 V
Output voltage, V_O	−0.5 to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−40 to +125°C

DC Characteristics

T_A = −40 to +85°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input voltage, low-level	V_{ILC}	−0.5		+0.8	V	CLK pin
	V_{IL}	−0.5		+0.8	V	Other pins
Input voltage, high-level	V_{IHC}	+3.3		V_{DD} + 0.3	V	CLK, $\overline{RESET}$ pins
	V_{IH}	+2.2		V_{DD} + 0.3	V	Other pins
Output voltage, low-level	V_{OL}			+0.4	V	I_{OL} = 2.5 mA
Output voltage, high-level	V_{OH}	0.7 V_{DD}			V	I_{OH} = −400 μA
Input leakage current	I_{LI}			±10	μA	V_{IN} = 0 to V_{DD}
Output leakage current	I_{LO}			±10	μA	V_{OUT} = 0 to V_{DD}
Supply current	I_{DD}		50	100	mA	While operating

AC Characteristics

T_A = −40 to +85°C; V_{DD} = 5 V ±10%

Parameter	Figure	Symbol	Min	Max	Unit	Condition
Clock						
CLK cycle	2	t_{CYK}	125	1000	ns	
CLK low-level width	2	t_{KKL}	50		ns	
CLK high-level width	2	t_{KKH}	50		ns	
CLK rise time	2	t_{KR}		10	ns	1.5 → 3.0 V
CLK fall time	2	t_{KF}				3.0 → 1.5 V
Image Memory Interface						
MREQ ↑ delay time from CLK ↑	3	t_{DMQH}		100	ns	
MREQ ↓ delay time from CLK ↑	3	t_{DMQH}		100	ns	
MACK ↑ setup time to CLK ↑	3	t_{SMA}	35		ns	
MACK ↓ hold time from CLK ↑	3	t_{HMA}	20		ns	
AEN ↑ delay time from CLK ↑	3	t_{DAEH}		100	ns	
AEN ↓ delay time from CLK ↑	3	t_{DAEL}		100	ns	
ASTB ↑ delay time from CLK ↓	3	t_{DSTH}		70	ns	
ASTB high-level width	3	t_{STST}	t_{KKH} − 15		ns	
ASTB ↓ delay time from CLK ↑	3	t_{DSTL}		100	ns	
Address/data/$\overline{MRD}$/$\overline{MWR}$ delay time from CLK ↓	3	t_{DA}		100	ns	
Address/data/$\overline{MRD}$/$\overline{MWR}$ float time from CLK ↓	3	t_{FA}	25	70	ns	
Address setup time to ASTB ↓	3	t_{SAST}	t_{KKH} − 35		ns	
Address hold time from ASTB ↓	3	t_{HSTA}	t_{KKL} − 20		ns	
$\overline{MRD}$ ↓ delay time from Address float	3	t_{DAR}	0		ns	
$\overline{MRD}$ ↓ delay time from CLK ↓	3	t_{DRL}		70	ns	
$\overline{MRD}$ low-level width	3	t_{RRL2}	$2t_{CYK}$ − 50		ns	WAIT = 0
$\overline{MRD}$↑ delay time from CLK ↑	3	t_{DRH}		70	ns	
Input data setup time to $\overline{MRD}$ ↑	3	t_{SDR}	70		ns	
Input data hold time from MRD ↑	3	t_{HRD}	0		ns	
$\overline{MWR}$↓ delay time from CLK ↓	3	t_{DWL}		70	ns	
$\overline{MWR}$ low-level width	3	t_{WWL2}	$2t_{CYK}$ − 50		ns	WAIT = 0
$\overline{MWR}$↑ delay time from CLK ↑	3	t_{DWH}		70	ns	
READY setup time to CLK ↑	3	t_{SRY}	35		ns	
READY hold time from CLK ↑	3	t_{HRY}	20		ns	
Host Interface						
$\overline{DACK}$/$\overline{CS}$ recovery time	4, 5	t_{RDC}	200		ns	
$\overline{IORD}$ low-level width	4, 7	t_{RRL}	150		ns	
Address/$\overline{CS}$ ↓ setup time to $\overline{IORD}$ ↓	4	t_{SAR}	35		ns	
Address/$\overline{CS}$ ↓ hold time from $\overline{IORD}$ ↑	4	t_{HRA}	0		ns	
Output data delay time from $\overline{IORD}$ ↓	4	t_{DRD}		120	ns	
Output data float time from $\overline{IORD}$ ↑	4	t_{FRD}	10	70	ns	
$\overline{IOWR}$ low-level width	5	t_{WWL}	100		ns	
$\overline{CS}$ ↓ hold time from $\overline{IOWR}$ ↑	5	t_{WWCS}	0		ns	

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AC Characteristics (cont)

$T_A = -40$ to $+85°C$; $V_{DD} = 5\ V \pm 10\%$

Parameter	Figure	Symbol	Min	Max	Unit	Condition
Address/$\overline{UBE}$/$\overline{CS}$ ↓ setup time to $\overline{IOWR}$ ↓	5	t_{SAW}	0		ns	
Address/$\overline{UBE}$ hold time from $\overline{IOWR}$ ↑	5	t_{HWA}	0		ns	
Input data setup time to $\overline{IOWR}$ ↑	5	t_{SDW}	100		ns	
Input data hold time from $\overline{IOWR}$ ↑	5	t_{HWD}	0		ns	
$\overline{RESET}$ low-level width	6	t_{RSTL}	$7t_{CYK}$		ns	
V_{DD} setup time to $\overline{RESET}$ ↑	6	t_{SVDD}	1000		ns	
$\overline{IOWR}$/$\overline{IORD}$ wait time from $\overline{RESET}$ ↑	6	t_{SYWR}	$2t_{CYK}$		ns	
$\overline{IOWR}$/$\overline{IORD}$ recovery time	7	t_{RVWR}	200		ns	
DREQ ↓ delay time from $\overline{IORD}$ ↓	7	t_{DRDQ}		140	ns	
DREQ ↓ delay time from $\overline{IOWR}$ ↓	7	t_{DWDQ}		140	ns	

Figure 1. Voltage Thresholds for Timing Measurements

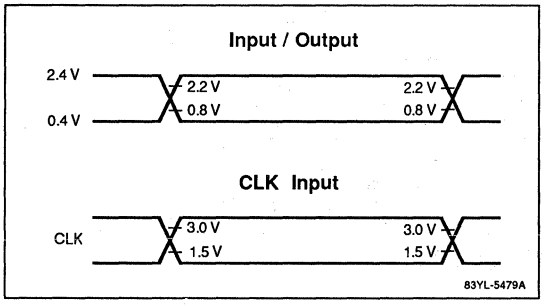


Figure 2. Clock Timing

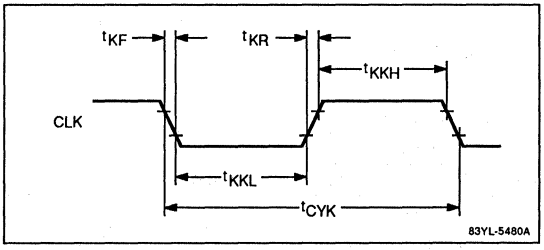
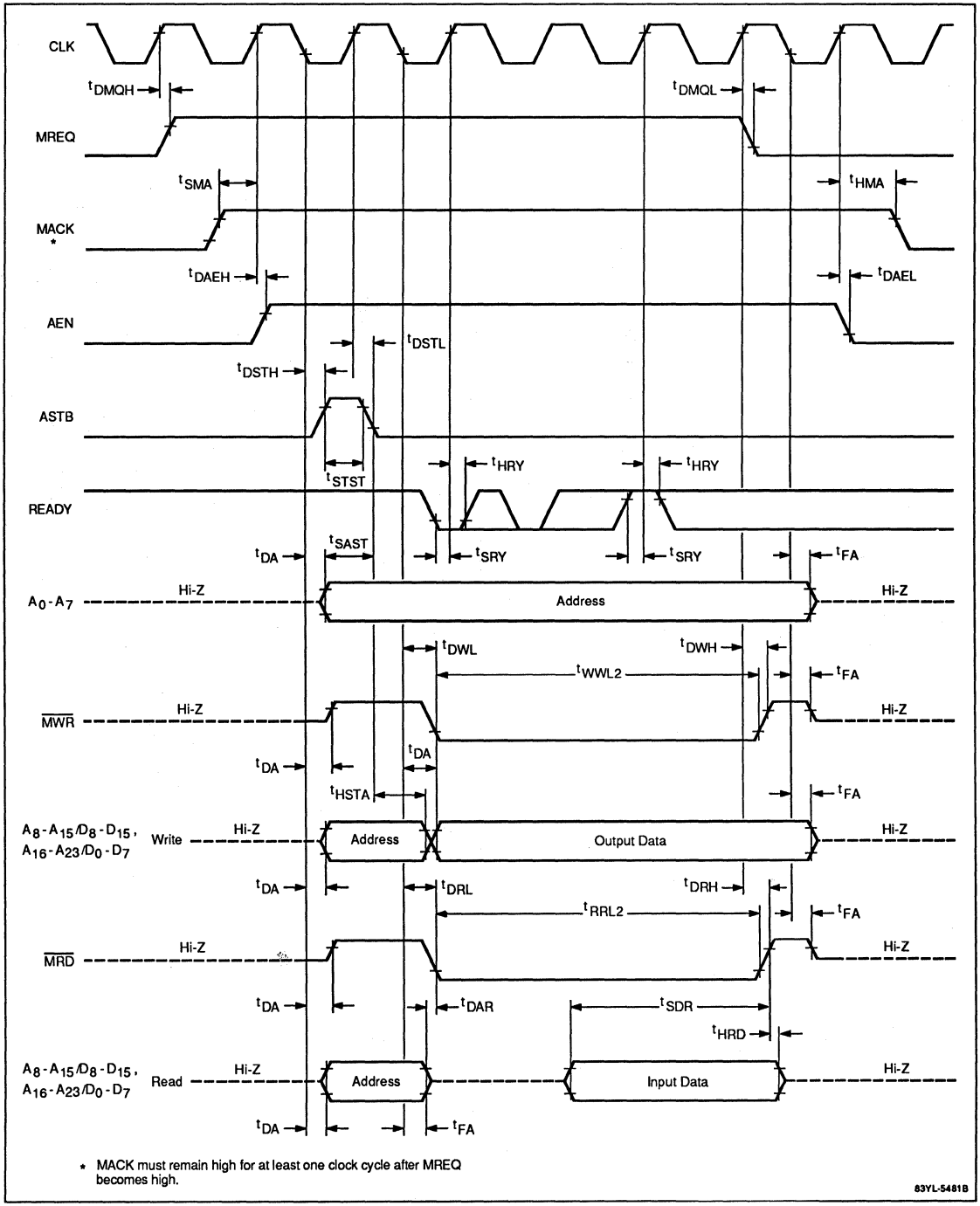


Figure 3. DMA Transfer Timing on Image Bus



* MACK must remain high for at least one clock cycle after MREQ becomes high.

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Figure 4. Timing for Read from μPD72185 on Host Bus

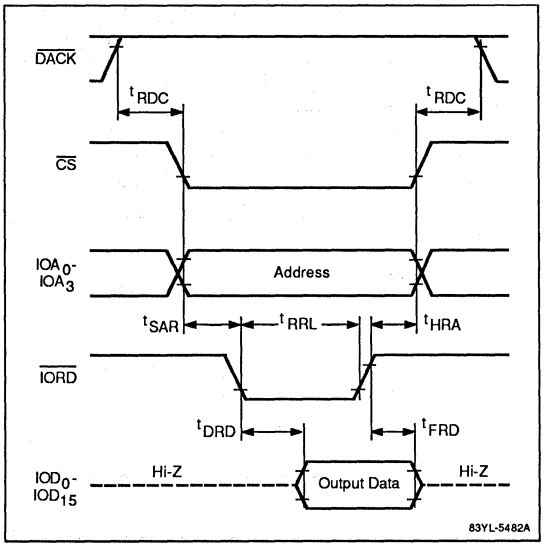


Figure 5. Timing for Write to μPD72185 on Host Bus

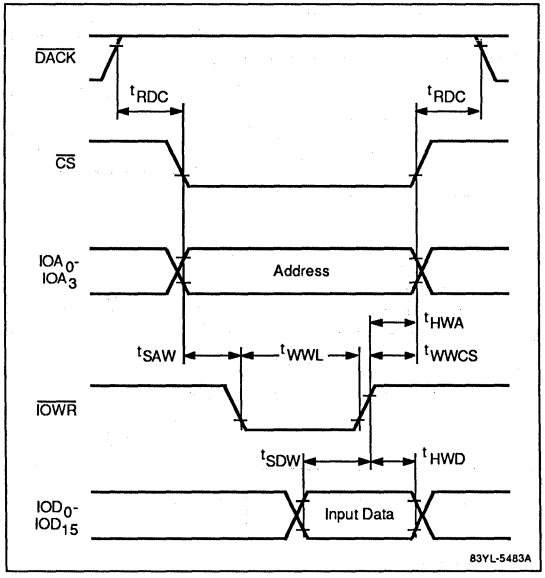


Figure 6. Reset Timing

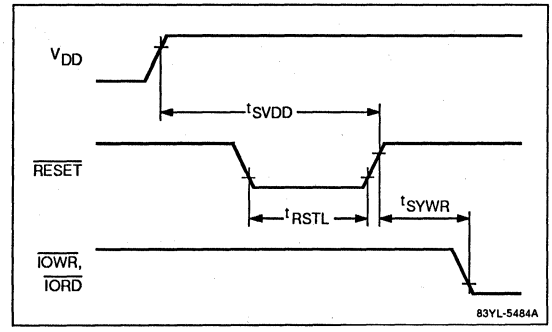
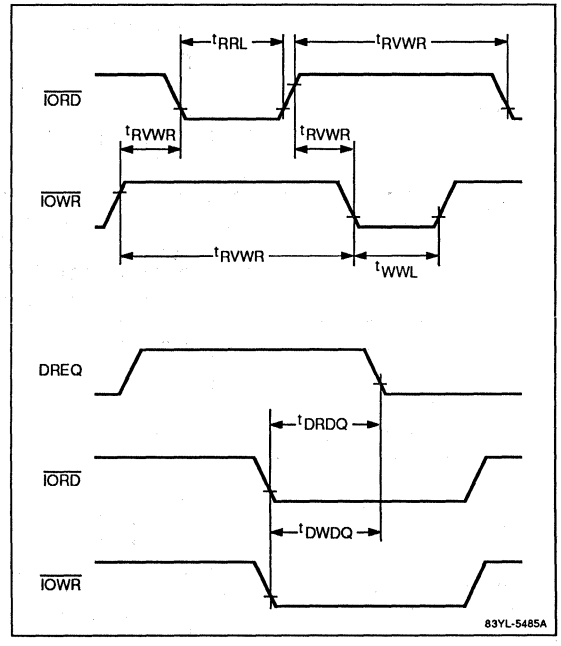


Figure 7. Read/Write Cycle Timing



OVERVIEW

The μPD72185 encodes and decodes binary image data in accordance with the standard system prescribed by the CCITT (International Telegraph and Telephone Consultative Committee). See table 1.

Table 1. CCITT Standard Systems

System	CCITT Recommendation
MW	T.4 (G3 Facsimile)
MR	T.4 (G3 Facsimile)
MMR	T.6 (G4 Facsimile)

The μPD72185 has two bus interfaces with which it connects to the system.One interface is with the host CPU and the other is with image memory. Data exchange with the host CPU is by ordinary I/O accesses; data exchange with image memory is by DMA transfers using the on-chip DMA controller.

In this document, the bus on the host CPU side is called the host bus, and the the bus on the image memory side is called the image memory bus.

In addition to encoding/decoding, the μPD72185 can perform data transfers between the image memory and the host CPU. Also, it can perform image enlargement and reduction on expansion and compression and logical operations (AND, OR, XOR,) while transferring data. Table 2 and figure 8 show the processing patterns.

Table 2. μPD72185 Processing Patterns

Type	Processing	Data Flow, Bus-to-Bus		
A	Encoding	Image memory	→	Image memory
B	Decoding	Image memory	→	Image memory
C	Encoding	Image memory	→	Host
D	Decoding	Host	→	Image memory
E	Data transfer	Image memory	→	Host
F	Data transfer	Host	→	Image memory
G	Data transfer	Image memory	→	Image memory

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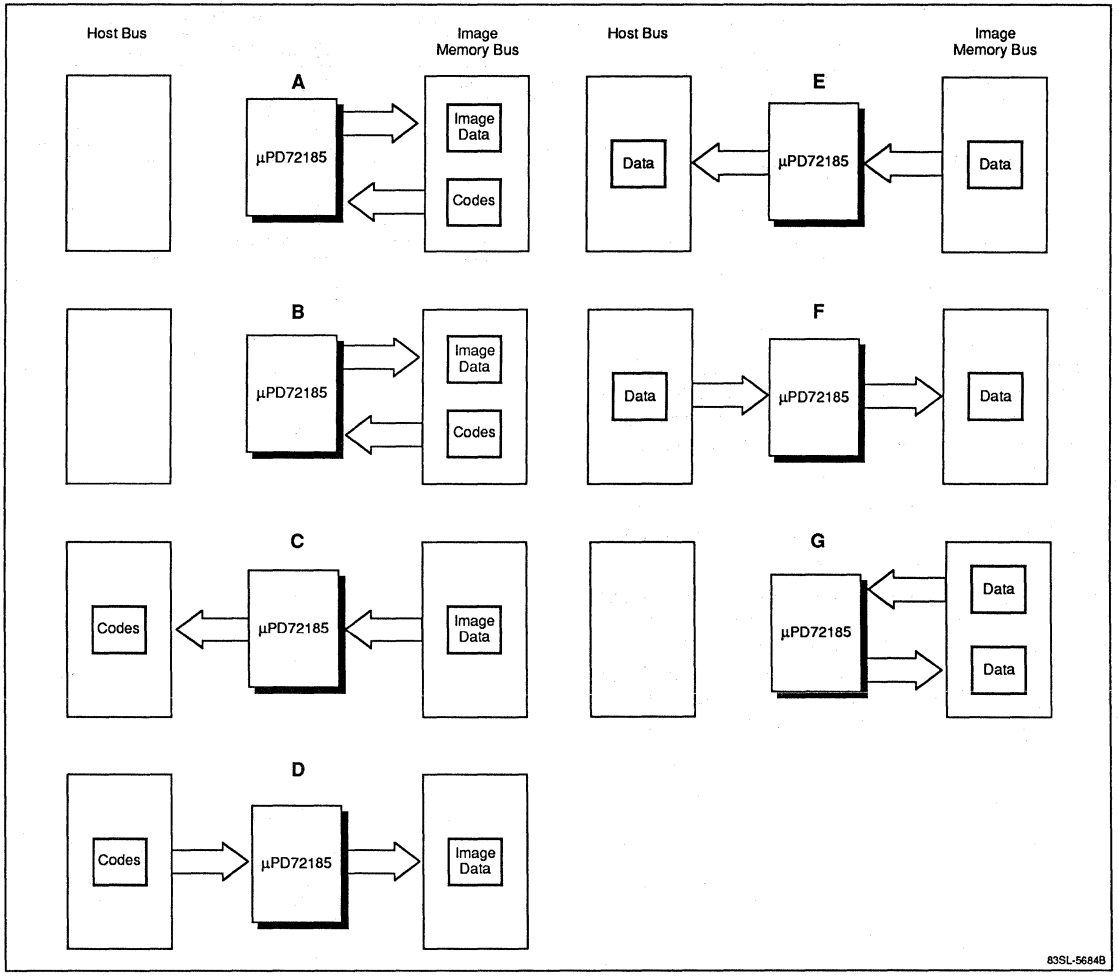
Figure 8. μPD72185 Processing Patterns



PROCESSING

Modes

The two processing modes of the μPD72185—block and line—are selected by commands from the host CPU. In block mode, which is more commonly used, one command controls processing of multiple lines. In line mode, one command is required for each line. Line mode allows encoding/decoding methods other those prescribed by the CCITT.

Line Processing

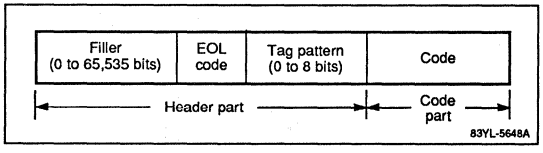
A compressed line consists of a header and code as shown in figure 9. In the header, commands from the host CPU specify the number of filler bits (0 to 65,535), the presence/absence of the EOL code, and the number of bits in the tag pattern (0 to 8).

The code that follows the header consists of encoded binary image data. The encoding method can be specified per line by commands from the host CPU.

At the time of encoding, a line is generated in this order: filler + EOL code + tag pattern + code. This filler is appended to the immediately preceding line.

Decoding is performed one line at a time in this order: code + filler + EOL code + tag pattern. If a page starts with an EOL code, the μPD72185 detects the EOL code and the following tag pattern and processes them before starting line-by-line decoding.

Figure 9. Line Composition (Line Mode)



EXTERNAL INTERFACE

The μPD72185 exchanges data with image memory by DMA transfers via the on-chip DMA controller. When the μPD72185 needs to access image memory, it requests use of the image memory bus by activating MREQ. Data is exchanged with a host CPU (including an external DMA controller) by normal I/O accesses. The host CPU reads and writes data through the μPD72185 I/O addresses.

MULTITASKING

Multitasking means using the μPD72185 to process multiple image areas in parallel by time division.

The μPD72185 processes an image area specified by the host CPU as a unit. On completion of processing, the μPD72185 sends back to the host CPU in the form of a response: memory manage ment information, processing information, counter information, etc.

As an example, consider a case in which image data encoded by one method is to be recoded by another method. When the recoded data extends over multiple image areas, the following two methods can be employed.

(1) All encoded data in the multiple image areas is decoded. This image data is then reencoded all at once.

(2) Encoded data in multiple image areas is decoded in small blocks. This image data is then recoded a block at a time, processing only a section of each image each time..

Depending on the system design, pipelining with method 2 may improve processing efficiency. This method can be implemented through the host CPU's management of responses sent back by the μPD72185.

ENLARGEMENT/REDUCTION

The μPD72185 can reduce an image when encoding and enlarge image data when decoding. Reduction is performed by a simple thinning-out operation, and enlargement by repeating the same data. Enlargement/reduction types are shown in table 3.

Table 3. Enlargement/Reduction Types

	Enlargement and (Reduction) Factors	
Type	Horizontal	Vertical
A	1 (1)	1 (1)
B	1 (1)	2 (1/2)
C	2 (1/2)	2 (1/2)
D	2 (1/2)	4 (1/4)

WHITE MASK

The μPD72185 can perform white mask processing on the right edge and left edge of image data. The amount of white masking is specified separately for each edge in word units (0 to 255 words)

The μPD72185 automatically white masks data on encoding image data. It is not able to perform decoding and white mask processing at the same time. Hence, white mask processing is performed once decoding is completed

BIT BOUNDARY

Some image areas consist of lines not terminated in either byte or word units but with an odd number of bits. The μPD72185 handles image areas of this kind with bit boundary processing.

Lines with an odd number of bits are processed by specifying void bits up to the byte or word boundary. See figure 10.

Figure 10. Bit Boundary Processing (Word Units)

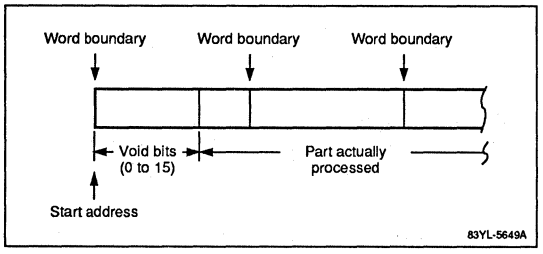


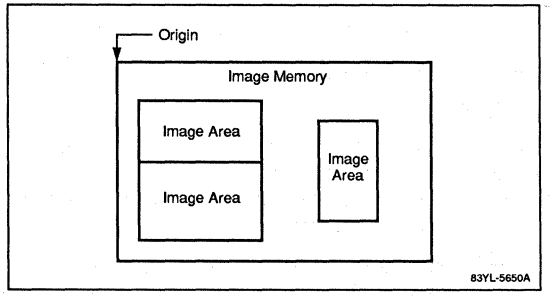
IMAGE MEMORY

Image Area

Image memory means the whole area of memory accessible by the μPD72185. An image area, on the other hand, is a rectangular area within image memory (figure 11), the size and location of which is specified by commands from the host CPU. The unit of processing is an image area.

The μPD72185 can append and also detect the code indicating the end of a page using commands from the host CPU. Page management, however, is performed by the host CPU.

Figure 11. Image Area Examples



Memory Organization

Under control of the host CPU, image memory can be either byte-organized (8-bit units) or word-organized (16-bit units). One μPD72185 address corresponds to one byte or one word in memory. In both cases the μPD72185 does its internal processing and writes to image memory in 16-bit units. Thus, when image memory is byte-organized, two accesses are required, one to an odd-numbered address and one to an even-numbered address.

The 24-line address bus allows access to a large amount of image memory. Table 4 shows image memory capacity for byte and word organization.

Table 4. Image Memory Capacity

Organization	Size	*Capacity
Byte	16M bytes	64 A4 sheets
Word	32M bytes	128 A4 sheets

*A4 sheet = 210 mm wide by 297 mm long
Horizontal: 8 dots/mm
Vertical: 4 dots/mm

Data Storage

Image memory can store code and other general data as well as binary image data. Binary image data is converted to white/black levels shown in table 5 and stored as follows.

(1) The first bits scanned are packed in sequence starting from the LSB of a byte/word.

(2) The first data byte/word scanned is packed in sequence in byte/word units starting from the lower address side.

Code transferred serially is stored as follows.

(1) The first bits transmitted are packed in sequence starting from the LSB of a byte/word.

(2) The first data byte/word transmitted is packed in sequence starting from the lower address side.

Table 5. Binary Image Data Levels

Level	Binary Notation
White	0
Black	1

ENCODING/DECODING SYSTEMS

Table 6 lists the encoding/decoding systems the μPD72185 can handle, including CCITT standard systems. Figure 12 shows coded data formats for MH, MR, and MMR systems.

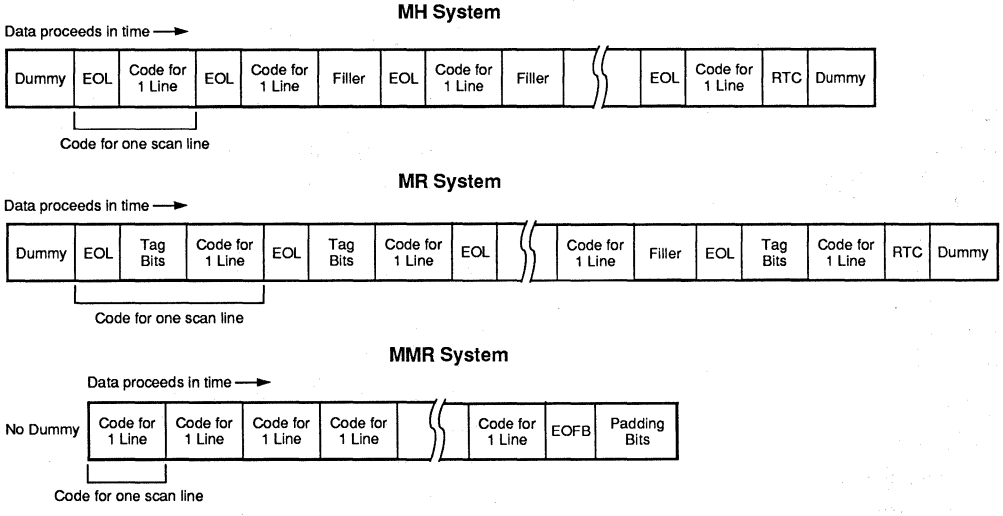
Table 6. Encoding/Decoding Systems

System	Summary
MH	One-dimensional encoding/decoding system, G3 facsimile, CCITT standard.
MR	Two-dimensional encoding/decoding system, G3 facsimile, CCITT standard.
MMR	Two-dimensional encoding/decoding system, G4 facsimile, CCITT standard.
Other	Systems other than CCITT standards that can be implemented by selecting line mode

Picture Elements

Image data that exceeds 2623 picture elements (pixels) per scan line is processed using the run-length code table expansion method stipulated in CCITT Recommendation T.6.

Figure 12. Code Data Formats in MH, MR, and MMR Systems



Item	MH System	MR System	MMR System
Start of each scan line	EOL	EOL	No EOL
Filler	Insertable	Insertable	None
RTC	Normally EOL x 6	(EOL + 1) x 6	EOL x 2
K-parameter	Undefined	Present	None
Tag bits	None	Normally 1 bit	None
EOL for head of page	None	None	None
≥ 2624 run length code	Make-up code x n + termination code		

Symbols

EOFB	End of facsimile block
EOL	End of line
RTC	Return to control
Dummy	Variable-length string of zeros

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K-Parameter

In the MR system, the K-parameter determines the coding technique and the transmission error recovery procedures. The value of the K-parameter can be specified as a number from 1 to 255 or as infinity (∞).

Whether the code for a particular line uses one-dimensional encoding or two-dimensional encoding is indicated by the value of the tag bit inserted after EOL. See table 7.

Table 7. Relation Between Encoding System and Tag Bit

Encoding System	Tag Bit Value	Method of Representation
One-dimensional	1	EOL + 1 (tag bit)
Two-dimensional	0	EOL + 0 (tag bit)

Filler Bits

When encoding, the μPD72185 can adjust the length of the coded data by adding filler bits. The two methods of adding filler bits are as follows.

(1) Specify minimum number of bits transmitted with the BLO command

(2) Specify number of added filler bits with the LNO command.

When decoding, the μPD72185 ignores the added filler bits.

Error Detection

When decoding, the μPD72185 can detect errors in the code and carry out appropriate processing. Table 8 lists the types of error detection.

Table 8. Types of Error Detection

Error Detection	Applicable Encoding Systems
Illegal code	MH, MR, MMR
Logically inconsistent code	MR, MMR
Decoded line longer than specified line length	MH, MR, MMR
Decoded line shorter than specified line length	
Abnormal page end	

Line Number Count

When decoding, the μPD72185 performs three kinds of line counting.

(1) The number of normally-decoded lines (normally-processed line count).

(2) The number of lines in error (error line count).

(3) The maximum number of consecutive lines in which errors occurred (consecutive error line count).

The start of error line counting and successive error line counting can be specified in either of two ways as shown below. The selection and setting of the initial value of each line count is done by command.

(1) Start count from occurrence of first error.

(2) Start count from normal decoding of one line.

HOST INTERFACE

Exchanges between the μPD72185 and the host CPU (or an external DMA controller) are performed by I/O accesses over the host interface. In general, writes from the host CPU to the μPD72185 are in the form of commands and reads from the μPD72185 are in the form of responses.

The host bus width is 16 data bits but can be accessed 8 bits at a time by manipulation of the logic level on pins IOA_0 and $\overline{UBE}$. See table 9.

Table 9. Host Bus Width

IOA_0	$\overline{UBE}$	Bus Width	Pins
0	0	16 bits	IOD_0-IOD_{15}
X	1	8 bits	IOD_0-IOD_7
1	0	8 bits	IOD_8-IOD_{15}

To get the μPD72185 to start processing, the following operations are necessary.

(1) Write the command into the command registers.

(2) Write 1 into the CRQ bit of the control register.

When the CRQ bit is set, the μPD72185 begins processing as directed by the command received. Once processing has begun, the host CPU cannot write 1 to the CRQ bit again for the next processing operation until it confirms that processing has been completed or interrupted.

Basic Timing

Figure 13 is a timing diagram applicable to reads from the μPD72185 and writes by the host CPU. Figure 14 shows the timing for an external DMA controller in the word mode and byte mode.

REGISTERS

Exchanges between the μPD72185 and the host CPU, including commands and responses, utilize the registers and the data FIFO area illustrated in figure 15. The register I/O addresses are 0H through DH; EH and FH are not allowed. Note that the I/O addresses are shared by corresponding registers in the read and write configurations of figure 15.

Figure 13. Read/Write Timing

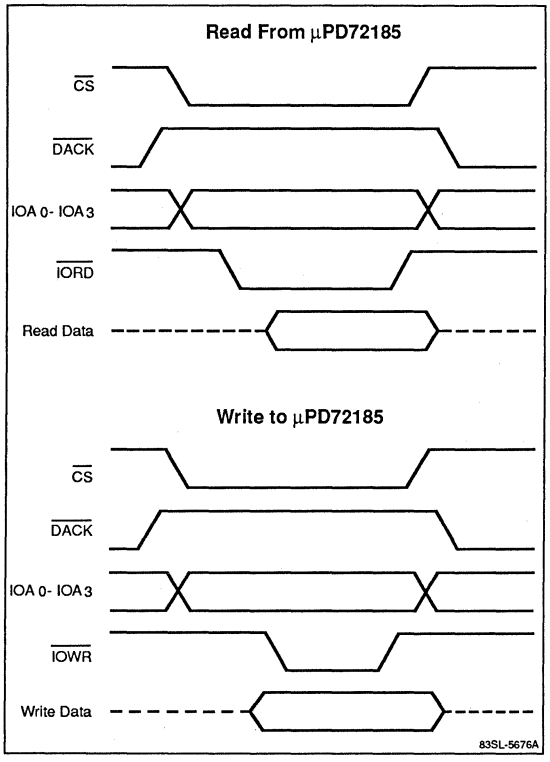

Figure 14. Read/Write Timing With External DMA Controller

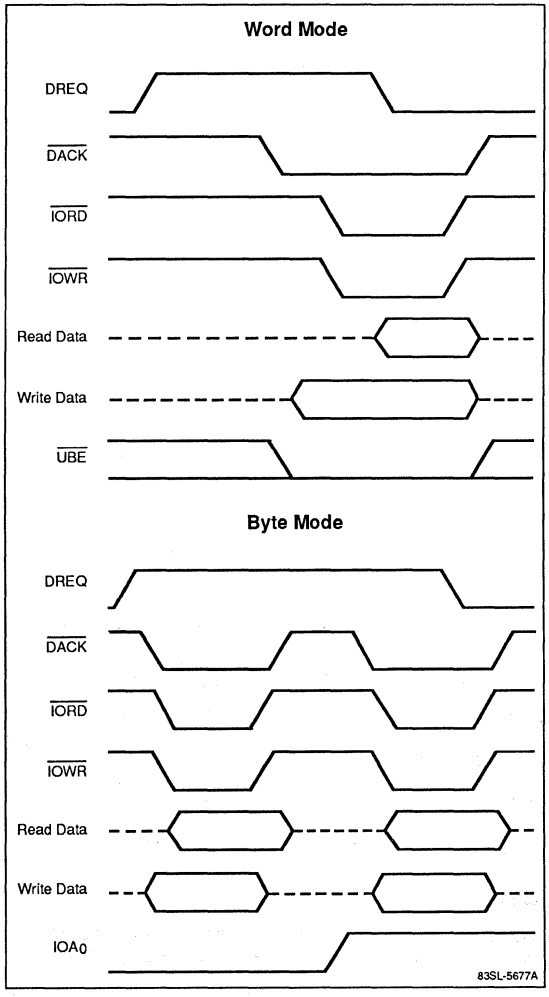

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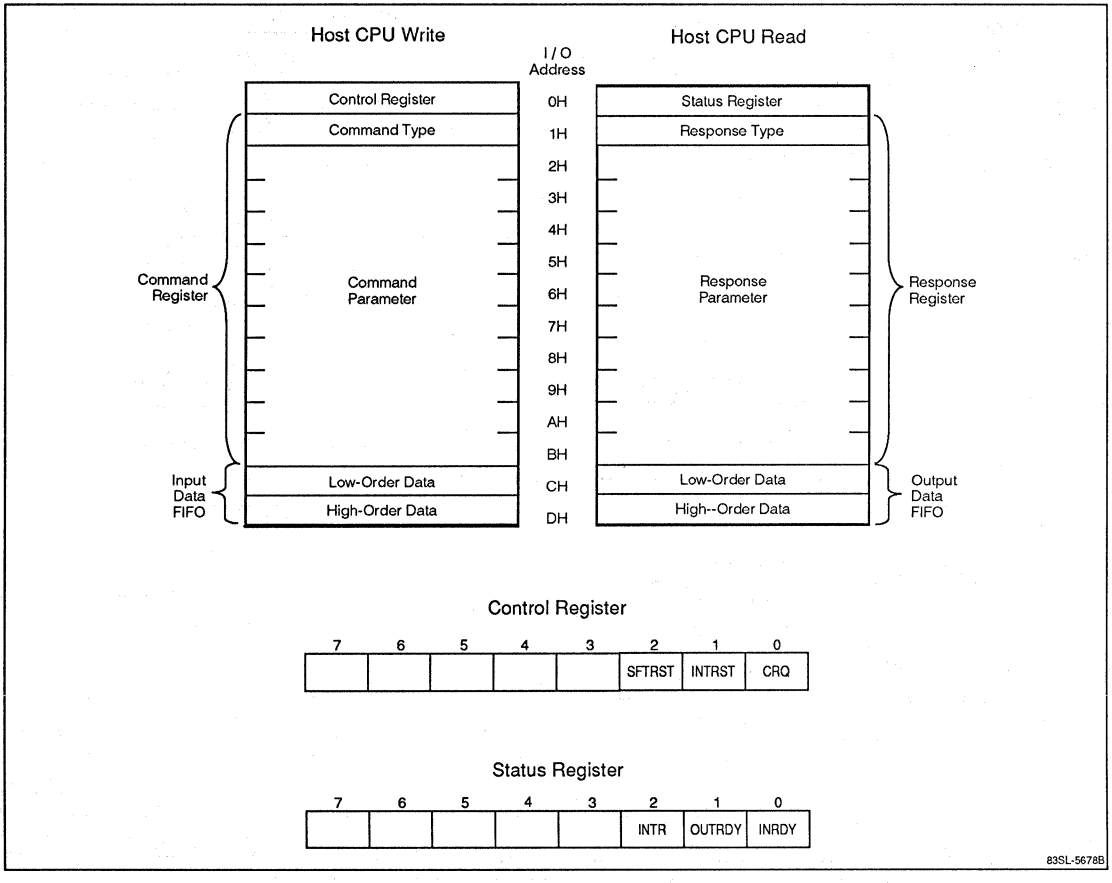
Figure 15. Register Organization



Control Register

The control register is used in writes from the host CPU. The functions of bits 0, 1, and 2 are explained below.

Command Request (CRQ). When 1 is written to the CRQ bit after the host CPU has written a command, the μPD72185 begins processing according to the command. The CRQ bit is automatically reset after completion of processing.

Interrupt Reset (INTRST). When the host CPU writes a 1 to the INTRST bit, the INT pin output and the INTR bit are reset. After being set, the INTRST bit will be reset automatically.

Software Reset (SFTRST). Software reset by setting SFTRST to 1 is functionally identical to hardware reset at the $\overline{\text{RESET}}$ pin.

Status Register

The status register is used in reads from the host CPU. The functions of bits 0, 1, and 2 are explained below.

Input Ready (INRDY). A 1 in the INRDY bit indicates the input data FIFO is ready to receive data from the host CPU.

Interrupt Request (INTR). The INTR bit shows the same logic level as the INT pin. The μPD72185 sets this bit to notify the host CPU that processing has been completed or interrupted.

Command Register

The command register is used in writes from the host CPU. It has two parts: command type and command parameter.

Response Register

The response register is used in reads from the host CPU. It has two parts: response type and response parameter.

Input/Output Data FIFO

The μPD72185 exchanges image data, code, etc., with the host CPU via the data FIFOs. The input data FIFO and the output data FIFO are each two bytes wide.

IMAGE MEMORY INTERFACE

The image memory interface is between the μPD72185 and the image memory, which stores image data and code. Accesses to image memory from the μPD72185 are performed by DMA operations using the on-chip DMA controller. Via the image memory interface, the μPD72185 directly controls image memory.

When the μPD72185 completes command processing, it reports completion or interruption to the host CPU by setting the output of the INT pin to high and at the same time setting the INTR bit in the status register. See figure 15.

The host CPU, meanwhile, confirms completion or interruption of processing either by sampling the INT signal level or by software polling the INTR bit.

DMA Transfer Timing

The basic bus cycle in a DMA transfer takes three system clock pulses: S1, S2, and S3. In this bus cycle, the μPD72185 reads or writes 1 byte or 1 word. See figure 16.

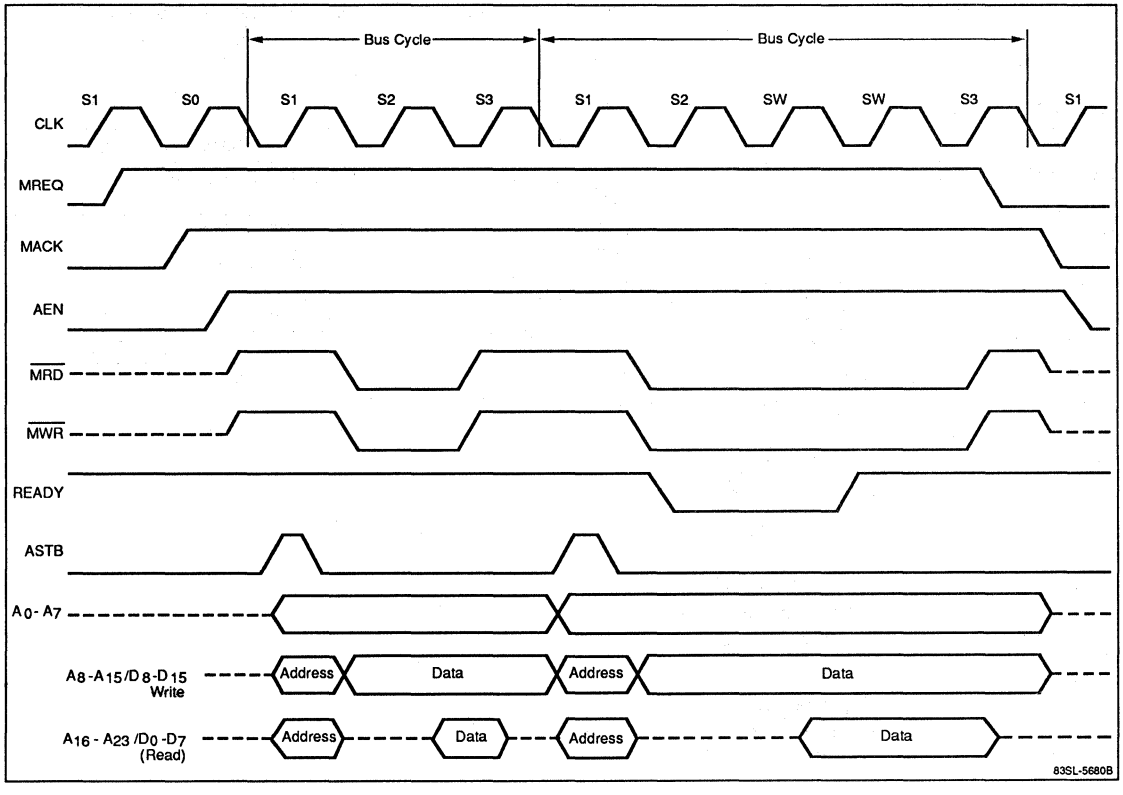
If the access time to an image memory element is long, and a read/write is not possible within the basic bus cycle, then the μPD72185 can insert wait states (SW) between S2 and S3, extending the read/write pulse width.

The two methods of inserting a wait state are:

(1) Using the READY pin.

(2) Programming wait states with a command

Figure 16. DMA Transfer Timing



Bus Cycle Modes

The μPD72185 has three modes in which it operates on the image memory bus as a Bus Master. A command selects the bus cycle mode.

Total Bus Monopolization Mode. The μPD72185 completely monopolizes the bus. The MREQ and MACK signals are not used.

Demand Mode. The μPD72185 holds on to the bus by keeping the MREQ signal high. The length of time held depends on the data being processed. The μPD72185 will always surrender the bus on completing the processing of a line.

Eight Bus Cycle Monopolization Mode. The μPD72185 monopolizes the bus for a maximum of eight bus cycles, after which it releases the bus by dropping MREQ to low. It waits at least three clock intervals before raising MREQ high again .

DMA Break

When the μPD72185 is monopolizing the image memory bus (MREQ = 1), MACK is normally kept high. If MACK falls to low while MREQ is high, the μPD72185 immediately discontinues the DMA transfer. However, because the MACK signal level is sampled at the rising edge of S3, there is a maximum delay of 1 bus cycle + 1/2 clock interval from the fall of MACK until the μPD72185 actually releases the bus.

In the total bus monopolization mode, DMA break does not operate.

Refresh

The μPD72185 is able to output refresh timing to image memory, thus facilitating the connection of pseudo-SRAM. However, the μPD72185 does not output the refresh address itself. Consequently, when DRAM is used in image memory, a refresh address generation circuit must be connected externally or a CAS-before-RAS cycle must be generated.

The refresh function is enabled with a command and performed with a read cycle to address 80000H. Pin A_{23}/D_7 used as the refresh timing output pin decreases the bus width to 23 bits..

COMMANDS

The μPD72185 has five types of commands: assignment, operation, statistical, CLB switch, and special. Table 11 describes the command types; table 12 describes the commands

Table 11. Command Types

Type	Function	Command
Assignment	Specifies system configuration, storage locations of data processed or to be processed, and processing mode.	MOD, SCDB, SIMB, SPRS, SYS
Operation	Gives directions to μPD72185 for start of encoding/decoding, data transfer (composition), and similar processing.	ABT, BLO, CNT, EOL, LNO, MSK, RTAG, RTC, TRO
Statistical	Requests information on processing executed by μPD72185.	RCLB. RPRS
CLB switch	Specifies use/non-use of compressed line buffer.*	CLB-ON, CLB-OFF
Special	Reads firmware version of the μPD72185.	RVER

* The compressed line buffer handles compressed storage of the code for one line according to the coding mode.

Table 12. List of Commands

Name	Function
ABT (Abort)	When a CFE interrupt* is generated, the μPD72185 resumes processing with the ABT command. However, this is done only for the line being processed when the interrupt was generated. When this line is completed, the μPD72185 interrupts processing again. If the ABT command is issued when an interrupt has not been generated, the μPD72185 cancels the continuous processing mode.
BLO (Block operation)	For block mode, specifies minimum number of bits transferred, word length of a line, number of void bits at left/right side, word length of white mask at left/ right side, etc. Normally, encoding/decoding by the μPD72185 is performed through this command.
CLB-ON/OFF (Compression line buffer on/off)	User specifies use of compression line buffer by CLB-ON or CLB-OFF command. Valid only in line mode.
CNT (Continue)	When the CNT command is issued, the μPD72185 processes the next consecutive image area equal in size to the area previously processed using the same processing mode and encoding/decoding system. By means of the CNT command, the μPD72185 can resume processing even when a CFE interrupt has been generated.
EOL (End of line)	During encoding, adds EOL code to coded data; during decoding, detects added EOL code. If the detected EOL code is judged to be part of the RTC code, the μPD72185 starts RTC search.
FILL (Fill	During encoding, adds fill bits to coded data.
LNO (Line operation)	For line mode, specifies number of fill bits to be added, word length of a line, number of void bits at left/right side, tag bit, etc.
MOD (Mode)	Assigns processing mode, encoding/ decoding format (transfer mode in case of a transfer), K-parameter, RTC, enlargement/ reduction, etc.
MSK (White mask)	For line-to-receive mask processing, specifies word length, word length of left/right side white mask, number of void bits on left/ right, etc. Also performs white mask processing on image buffer.
RCLB (Read compression line buffer)	When the RCLB command is received, the μPD72185 reads the contents of the compression line buffer. Provides user with pixel distribution data for a line.

Table 12. List of Commands (cont)

Name	Function
RPRS (Read process status)	Requests statistical information from μPD72185 on number of normally-processed lines, number of error lines, etc., resulting from processing.
RTAG (Read tag pattern)	During decoding, reads tag pattern attached to start of a line. In line mode, interpretation of the tag pattern by the host CPU allows an individual non-CCITT standard encoding/decoding system to be implemented.
RTC (Return to control)	During encoding, adds RTC code to coded data; during decoding, detects added RTC code.
RVER (Read version number)	Reads firmware versions built into μPD72185
SCDB (Set code buffer)	Specifies start address, size, and start bit position of image area (code buffer) that stores code. When the coded data is coming from the host CPU side, the start address should be set to 0.
SIMB (Set image buffer)	Specifies start address of reference line in image memory, and start address and size of image area (image buffer) that stores image data. When a transfer is performed, specifies transfer source/destination address and size of transfer.
SPRS (Set process status)	Specifies initialization values for normal processing line count, maximum error line count, etc., and abort if error line count exceeds maximum.
SYS (System)	Assigns specific system parameters such as image memory organization, bus cycle mode, word length of a line, etc. Also initializes internal μPD72185 parameter table.
TRO (Transfer operation)	Performs data transfer/composition for image buffer specified by IMB command.

* CFE interrupt is generated if a CEMPT or CFULL response is returned.

RESPONSES

The μPD72185 has four types of responses: confirmation, error, statistical, and special. Table 13 describes the response types; table 14 describes the responses.

Table 13. Response Types

Type	Function	Response
Confirmation	Reports normal completion of processing requested by a command	BCDOK, BDCOK,ECDOK, EDCOK, FILLOK, LCDOK, LDCOK, MODOK, MSKOK, POK, RCDOK, RDCOK, SCDBOK, SIMBOK, SOK, SYSOK, TAGPAT, TRNOK, VEROK
Error	Returned when an error occurs during processing requested by a command.	BLABT, CMDERR, DBLCRQ LNABT
Statistical	Returns statistical information in response to a command.	PRSTBL
Special	Other than above.	CEMPT, CFULL, CLBTBL

Table 14. List of Responses

Name	Function
BCDOK (Block code okay)	Indicates normal termination of encoding by BLO command. Sends back to host CPU: number of lines processed; start address of image data buffer following processed image data buffer; start address and start bit position of code buffer following processed code buffer.
BDCOK (Block decode okay)	Indicates normal termination of decoding by BLO command. Sends back to host CPU: number of lines processed; start address of image data buffer following processed image data buffer; start address and start bit position of code buffer following processed code buffer.
BLABT (Block abort)	Indicates that during decoding by BLO command, processing was aborted because error line count exceeded maximum value set by SPRS command. Sends back to host CPU: number of lines processed; start address of image buffer following processed image buffer; start address and start bit position of code buffer following processed code buffer.
CEMPT (CDB empty)	Indicates specified code buffer has become empty during decoding. At this point, the μPD72185 enters the CFE interrupt state and subsequently accepts only SYS, SCDB, CNT, ABT, RPRS, and RCLB commands. If other commands are issued, a CFEERR response is returned.
CFEERR (CDB full/empty error)	In the CFE interrupt state, indicates a command other than SYS, SCDB, CNT, ABT, RPRS, or RCLB has been issued.

Table 14. List of Responses (cont)

Name	Function
CFULL (CDB full)	Indicates specified code buffer has become full during encoding. At this point, the μPD72185 enters the CFE interrupt state and subsequently accepts only SYS, SCDB, CNT, ABT, RPRS, and RCLB commands. If other commands are issued, a CFEERR response is returned.
CLBTBL (CLBTBL table)	Reports compression line buffer contents in response to RCLB command.
CMDERR (Command error)	Indicates that there is no command corresponding to input command code.
DBLCRQ (Double CRQ error)	Indicates receipt of duplicate command requests during processing, and notifies host CPU that processing being executed is invalidated.
ECDOK (EOL code okay)	Indicates EOL code has been added and output to code buffer by EOL command. Sends back to host CPU: start address and start bit position of code buffer following processed code buffer.
EDCOK (EOL decode okay)	Indicates detection of EOL code in code buffer by EOL command. Sends back to host CPU: address and position of bit following detected EOL code.
FILLOK (FILL okay)	Indicates that the number of fill bits specified by a FILL command have been output. Sends back to host CPU: start address and bit position of buffer code following fill bits.
LCDOK (Line code okay)	Indicates normal termination of encoding by LNO command. Sends back to host CPU: number of lines remaining in image buffer; start address of image buffer following processed image buffer; start address and start bit position of code buffer following processed code buffer.
LDCOK (Line decode okay)	Indicates normal termination of decoding by LNO command. Sends back to host CPU: number of lines remaining in image buffer; start address of image buffer following processed image buffer; start address and start bit position of code buffer following processed code buffer.
LNABT (Line abort)	Indicates that during execution of decoding by LNO command, processing was aborted because error line count exceeded maximum value set by SPRS command. Sends back to host CPU: number of lines remaining in image buffer; start address of image buffer following processed image buffer; start address and start bit position of code buffer following processed code buffer.

Table 14. List of Responses (cont)

Name	Function
MODOK (MOD okay)	Indicates normal termination of MOD command processing.
MSKOK (Mask okay)	Indicates normal termination of processing by MSK command. Sends back to host CPU: start address of next image buffer to be processed.
POK (Process okay)	When the μPD72185 is in continuous processing mode, and the object of execution by an ABT command is BLO, LNO, RTAG, EOL, or RTC, then POK indicates continuous processing mode has been discontinued. Sends back to host CPU: start address and start bit position of code buffer following processed code buffer.
PRSTBL (Process status table)	Reports contents of statistical information table before it is initialized by SPRS command. Also reports current contents of table in response to RPRS command.
RCDOK (RTC code okay)	Indicates RTC code has been added and output to code buffer by RTC command. Sends back to host CPU: start address and start bit position of code buffer following processed code buffer.
RDCOK (RTC decode okay)	Indicates detection of RTC code in code buffer by RTC command. Sends back to host CPU: address and position of bit following detected RTC code.
SCDBOK (SCDB okay)	Indicates normal termination of SCDB command processing.
SIMBOK (SIMB okay)	Indicates normal termination of SIMB command processing.
SOK (Set okay)	Indicates that when a CNT or ABT command has been issued and the command to be executed does not exist, the μPD72185 has terminated processing.
SYSOK (SYS okay)	Indicates normal termination of SYS command processing.
TAGPAT (Tag pattern)	Indicates tag pattern specified by an RTAG command has been read. Sends back to host CPU: start address of code buffer following read tag pattern and start bit position of that code buffer.
TRNOK (Transfer okay)	Indicates normal termination of data transfer/composition processing by TRO command. Sends back to host CPU: next transfer source/destination address.
VEROK (RVER okay)	Returns firmware version to the host CPU.

SYSTEM CONFIGURATION

Figure 17 is a diagram of low-end and high-end system configurations.

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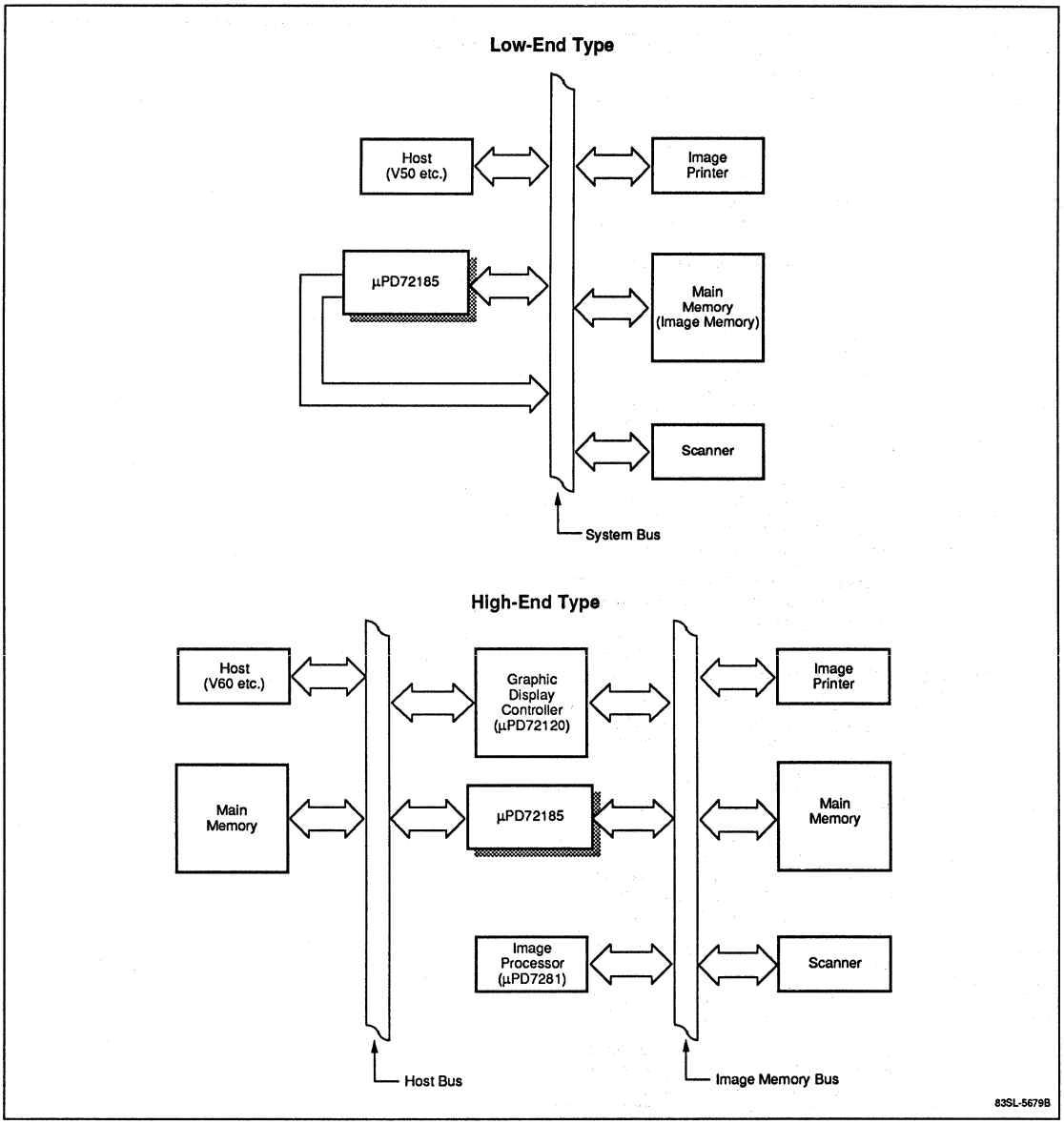
Figure 17. System Configurations



NEC

FLOPPY-DISK CONTROLLERS

5

Section 5
Floppy-Disk Controllers

NEC

NEC Electronics Inc.

μPD765A/μPD765B Single/Double Density Floppy-Disk Controller

Description

The μPD765A/B is an LSI floppy disk controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double-sided recording. The μPD765A/B provides control signals which simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk interface.

Hand-shaking signals are provided in the μPD765A/B which make DMA operation easy to incorporate with the aid of an external DMA controller chip, such as the μPD8257. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

There are 16 commands which the μPD765A/μPD765B will execute. Most of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available.

Read Data	Read Deleted Data
Read ID	Write Data
Specify	Write ID (Format Write)
Read Diagnostic	Write Deleted Data
Scan Equal	Seek
Scan High or Equal	Recalibrate
Scan Low or Equal	Sense Interrupt Status
Version	Sense Drive Status.

Ordering Information

Device Number	Package Type	Max Freq. of Operation
μPD765AC2	40-pin plastic DIP	8 MHz
μPD765B	40-pin plastic DIP	8 MHz

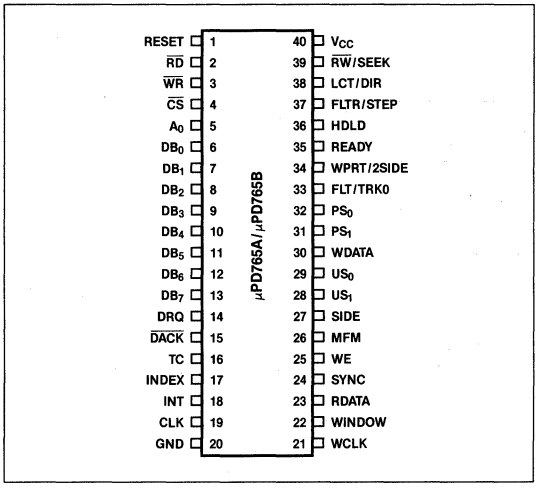
Features

Address mark detection circuitry is internal to the FDC which simplifies the phase-locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The μPD765A/μPD765B offers additional features such as multi-track and multi-side read and write commands and single and double density capabilities.

- ☐ FM, MFM Control
- ☐ Variable recording length: 128, 256, . . . 8192 bytes/sector
- ☐ IBM-compatible format (single- and double-sided, single- and double-density)
- ☐ Multi-sector and multi-track transfer capability
- ☐ Drive up to 4 floppy or micro floppydisk drives
- ☐ Data scan capability — will scan a single sector or an entire cylinder comparing byte-for-byte host memory and disk data
- ☐ Data transfers in DMA or non-DMA mode
- ☐ Parallel seek operations on up to four drives
- ☐ Compatible with μPD8080/85, μPD8086/88, V-series and μPD780 (Z80®) microprocessors
- ☐ Single-phase clock: 8 MHz maximum
- ☐ +5 V only

® Z80 is a registered trademark of the Zilog Corporation.

Pin Configuration



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Pin Identification

No.	Symbol	Function
1	RESET	Reset input
2	$\overline{RD}$	Read control input
3	$\overline{WR}$	Write control input
4	$\overline{CS}$	Chip select input
5	A_0	Data or status select input
6–13	DB_0–DB_7	Bidirectional data bus
14	DRQ	DMA request output
15	$\overline{DACK}$	DMA acknowledge input
16	TC	Terminal count input
17	INDEX	Index input
18	INT	Interrupt request output
19	CLK	Clock input
20	GND	Ground
21	WCLK	Write clock input
22	WINDOW	Read data window input
23	RDATA	Read data input
24	SYNC	VCO sync output
25	WE	Write enable output
26	MFM	MFM output
27	SIDE	Head select output
28, 29	US_0, US_1	FDD unit select output
30	WDATA	Write data output
31, 32	PS_0, PS_1	Preshift output
33	FLT / TRK0	Fault / track zero input
34	WPRT / 2SIDE	Write protect / two side input
35	READY	Ready input
36	HDLD	Head load output
37	FLTR / STEP	Fault reset / step output
38	LCT / DIR	Low current direction output
39	$\overline{RW}$ / SEEK	Read / write / seek output
40	V_{CC}	DC power (+5 V)

Pin Functions

RESET (Reset)

The RESET input places the FDC in the idle state. It resets the output lines to the FDD to 0 (low), except PS0, 1 and WDATA (undefined), INT and DRQ also go low; DB0-7 goes to an input state. It does not affect SRT, HUT, or HLT in the Specify command. If the RDY input is held high during reset, the FDC will generate an interrupt within 1.024 ms. To clear this interrupt, use the Sense Interrupt Status command.

$\overline{RD}$ (Read Strobe)

The RD input allows the transfer of data from the FDC to the data bus when low and either $\overline{CS}$ or $\overline{DACK}$ is asserted.

$\overline{WR}$ (Write Strobe)

The $\overline{WR}$ input allows the transfer of data to the FDC from the data bus when low. Disabled when $\overline{CS}$ is high.

A_0 (Data/Status Select)

The A_0 input selects the data register ($A_0 = 1$) or status register ($A_0 = 0$) contents to be accessed through the data bus.

$\overline{CS}$ (Chip Select)

The FDC is selected when $\overline{CS}$ is low, enabling $\overline{RD}$ and $\overline{WR}$.

DB_0–DB_7 (Data Bus)

DB_0–DB_7 are a bidirectional 8-bit data bus. Disabled when $\overline{CS}$ is high.

DRQ (DMA Request)

The FDC asserts the DRQ output high to request a DMA transfer.

$\overline{DACK}$ (DMA Acknowledge)

When the $\overline{DACK}$ input is low, a DMA cycle is active and the controller is performing a DMA transfer.

TC (Terminal Count)

When the TC input is high, it indicates the termination of a DMA transfer. It terminates data transfer during Read/Write/Scan commands in DMA or interrupt mode.

INDEX (Index)

The INDEX input goes high at the beginning of a disk track.

INT (Interrupt)

The INT output is FDC's interrupt request. In Non-DMA mode, the signal is output for each byte. In DMA mode, it is output at the termination of a command operation.

CLK (Clock)

CLK is the input for the FDC's single-phase, TTL-level squarewave clock: 8 MHz or 4 MHz. (Requires a pull-up resistor.)

WCLK (Write Clock)

The WCLK input sets the data write rate to the FDD. It is 500 kHz for FM, 1 MHz for MFM drives, for 8 MHz operation of the FDC; 250 kHz FM or 500 kHz MFM for 4 MHz FDC operation.

This signal must be input for read and write cycles. WCLK's rising edge must be synchronized with CLK's rising edge, except for the μPD765B.

WINDOW (Read Data Window)

The WINDOW input is generated by the phase-locked loop (PLL). It is used to sample data from the FDD and in distinguishing between clock and data bits in the FDC.

RDATA (Read Data)

The RDATA input is the read data from the FDD, containing clock and data bits. To avoid a deadlock situation, input RDATA and WINDOW together.

WDATA (Write Data)

WDATA is the serial clock and data output to the FDD.

WE (Write Enable)

The WE output enables write data into the FDD.

SYNC (VCO Sync)

The SYNC output inhibits the VCO in the PLL when low, enables it when high.

MFM (MFM Mode)

The MFM output shows the VCO's operation mode. It is high for MFM, low for FM.

SIDE (Head Select)

Head 1 is selected when the SIDE output is 1 (high), head 0 is selected when SIDE is 0 (low).

US_0, US_1 (Unit Select 0, 1)

The US_0 and US_1 outputs select up to 4 floppy disk drive units using an external decoder.

PS_0, PS_1 (Preshift 0, 1)

The PS_0 and PS_1 outputs are the write precompensation request signals for MFM mode. They determine early, late, and normal times for WDATA shifting.

PS0	PS1	Shift (MFM WDATA)
0	0	Normal
0	1	Late
1	0	Early
1	1	—

READY (Ready)

The READY input indicates that the FDD is ready to receive data.

HDLD (Head Load)

The HDLD output is the command which causes the read/write head in the FDD to contact the diskette.

FLT/TRK0 (Fault/Track 0)

In the read/write mode, the FLT input detects FDD fault conditions. In the seek mode, TRK0 indicates track 0 head position.

WPRT/2SIDE (Write Protect/Two Side)

In the read/write mode, the WPRT input senses write protected status (at the drive or media.) In the seek mode, 2SIDE senses two-sided media.

FLTR/STEP (Fault Reset/Step)

In the read/write mode, the FLTR output resets the fault flip-flop in the FDD. In the seek mode, STEP outputs step pulses to move the head to another cylinder. A fault reset pulse is issued at the beginning or each Read or Write command prior to the HDLD signal.

LCT/DIR (Low Current/Direction)

In the read/write mode, the LCT output indicates that the R/W head is positioned at cylinder 42 or greater. In the seek mode, the DIR output determines the direction the head will move in when it receives a step pulse. If DIR is 0, seeks are performed in the outward direction; DIR is 1, seeks are performed in the inward direction.

$\overline{RW}$/SEEK (Read/Write/Seek)

The $\overline{RW}$/SEEK output specifies the read/write mode when low, and the seek mode when high.

GND (Ground)

Ground.

V_{CC} (+5 V)

+5 V power supply.

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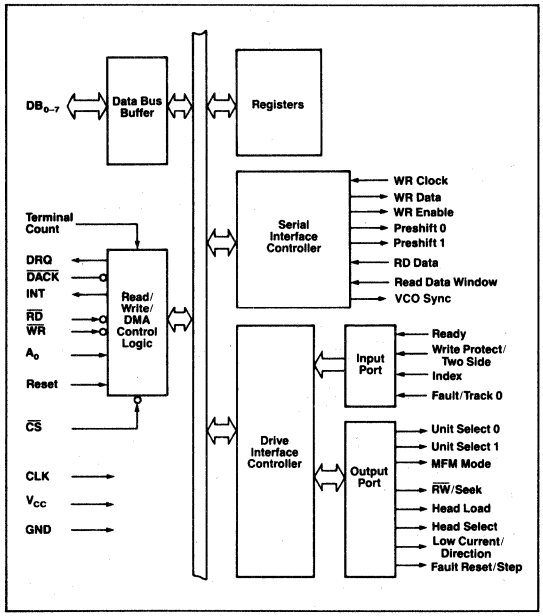
Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{CC}	−0.5 to +7 V
Input voltage, V_I	−0.5 to +7 V
Output voltage, V_O	−0.5 to +7 V
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in the Absolute Maximum Ratings could cause permanent damage. The device should not be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.5		+0.8	V	
Input voltage high	V_{IH}	2.0		V_{CC}+0.5	V	
Output voltage low	V_{OL}			0.45	V	$I_{OL} = 2.0\,mA$
Output voltage high	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -200\,\mu A$
Input voltage low (CLK + WCLK)	$V_{IL}(\Phi)$	−0.5		0.65	V	
Input voltage high (CLK + WCLK)	$V_{IH}(\Phi)$	2.4		V_{CC}+0.5	V	
Supply current (V_{CC})	I_{CC}			150 140	mA mA	μPD765AC2 μPD765B
Input load current high	I_{LIH}			10	μA	$V_{IN} = V_{CC}$
Input load current low	I_{LIL}			−10	μA	$V_{IN} = 0\,V$
Output leakage current high	I_{LOH}			10	μA	$V_{OUT} = V_{CC}$
Output leakage current low	I_{LOL}			−10	μA	$V_{OUT} = +0.45\,V$

Capacitance

$T_A = 25°C$, $f_C = 1\,MHz$, $V_{CC} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input clock capacitance	$C_{IN}(\Phi)$			20	pF	(Note 1)
Input capacitance	C_{IN}			10	pF	(Note 1)
Output capacitance	C_{OUT}			20	pF	(Note 1)

Note:
(1) All pins except pin under test tied to AC ground.

DIFFERENCES BETWEEN μPD765A AND μPD765B

The μPD765B is a functionally enhanced version of the μPD765A. Differences are explained below.

Overrun Bit [OR]

In μPD765A, when executing a read- or write-type command (except READ ID and SCAN types), the result status OR bit is not set if there is an overrun on the final byte of a sector. An improvement in the μPD765B allows it to set the OR bit in any situation.

DRQ Reset

When an overrun occurs, the μPD765A needs $\overline{\text{DACK}}$ input to reset DRQ. If $\overline{\text{DACK}}$ is not available, an external DMA controller continues to operate even after the FDC enters the R-Phase (Result Phase), and stored result status may be transferred accidentally as ordinary data.

On the other hand, the μPD765B resets DRQ automatically just before the R-Phase entry and independent of the $\overline{\text{DACK}}$ input. See AC Characteristics for DRQ reset timing.

Clock Synchronization

The μPD765B does not require synchronization between the CLK and WCLK inputs.

Version Command

The Version command distinguishes the μPD765B from other devices. The ST0 response to the Version command is:

Part No.	ST0 Value
μPD765A	80H
μPD765B	90H

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AC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5$ V ±10%

Parameter	Symbol	Min	Typ (1)	Max	Unit	Conditions
Clock period	ϕ_{CY}	120	125	500	ns	8-MHz CLK
		240	250	500	ns	4-MHz CLK
Clock active (high, low)	ϕ_0	40			ns	
Clock rise time	ϕ_R			20	ns	
Clock fall time	ϕ_F			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to RD ↓	t_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}$ ↑	t_{RA}	0			ns	
$\overline{RD}$ width	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	t_{RD}			140	ns	$C_L = 100$ pF
DB to float delay time from $\overline{RD}$ ↑	t_{DF}	10		85	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to WR ↓	t_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time to $\overline{WR}$ ↑	t_{WA}	0			ns	
$\overline{WR}$ width	t_{WW}	200			ns	
Data setup time to $\overline{WR}$ ↑	t_{DW}	100			ns	
Data hold time from $\overline{WR}$ ↑	t_{WD}	0			ns	
$\overline{INT}$ delay time from $\overline{RD}$ ↑	t_{RI}			$2\phi_{CY} + \phi_0 + 135$	ns	Non-DMA mode
$\overline{INT}$ delay time from $\overline{WR}$ ↑	t_{WI}			$2\phi_{CY} + \phi_0 + 135$	ns	
DRQ cycle time	t_{MCY}	13			μs	$\phi_{CY} = 125$ ns (Note 4)
$\overline{DACK}$ ↓ → DRQ ↓ delay	t_{AM}			140	ns	
DRQ ↑ → $\overline{DACK}$ ↓ delay	t_{MA}	200			ns	$\phi_{CY} = 125$ ns (Note 4)
$\overline{DACK}$ width	t_{AA}	$2\phi_{CY} + 15$			ns	
TC width	t_{TC}	1			ϕ_{CY}	
Reset width	t_{RST}	14			ϕ_{CY}	
DRQ ↓ → INT response time	t_{MI}	60		77	ϕ_{CY}	μPD765B only
INT → $\overline{DACK}$ ineffective	t_{IA}			1	ϕ_{CY}	

Parameter	Symbol	Min	Typ (1)	Max	Unit	Conditions
WCLK cycle time	t_{CY}		16		ϕ_{CY}	MFM = 0
			8		ϕ_{CY}	MFM = 1
WCLK active time (high)	t_0	80	250	350	ns	Note 4
CLK ↑ → WCLK ↓ delay	t_{CWL}	0		ϕ_0	ns	μPD765AC2 only
WCLK, RDATA and WINDOW rise time	t_R			20	ns	
WCLK, RDATA and WINDOW fall time	t_F			20	ns	
Preshift delay time from WCLK ↑	t_{CP}	20		100	ns	
WCLK ↑ → WE ↑ delay	t_{CWE}	20		100	ns	
WDATA delay time from WCLK ↑	t_{CD}	20		100	ns	
RDATA active time (high)	t_{RDD}	40			ns	
Window cycle time	t_{WCY}		2		μs	MFM = 0
			1		μs	MFM = 1
Window hold time from RDATA	t_{RDW}	15			ns	
Window setup time to RDATA	t_{WRD}	15			ns	
$US_{0,1}$ setup time to SEEK ↑	t_{US}	12			μs	8-MHz CLK Notes 4, 5
SEEK setup time to DIR	t_{SD}	7			μs	
Direction setup time to step ↑	t_{DST}	1.0			μs	
$US_{0,1}$ hold time from step ↑	t_{STU}	5.0			μs	
Step active time (high)	t_{STP}	6	7	8	μs	Notes 4, 5
Step cycle time	t_{SC}	33	Note 2	Note 2	μs	
Fault reset active time (high)	t_{FR}	8.0		10	μs	
Write data width	t_{WDD}	$t_0 - 50$			ns	
$US_{0,1}$ hold time after seek	t_{SU}	15			μs	8-MHz CLK Notes 3, 4, 5
SEEK hold time from DIR	t_{DS}	30			μs	8-MHz CLK Notes 4, 5
DIR hold time after step	t_{STD}	24			μs	
Index pulse width	t_{IDX}	4			ϕ_{CY}	

AC Characteristics (cont)

Parameter	Symbol	Min	Typ (1)	Max	Unit	Conditions
$\overline{RD}$ ↓ delay from DRQ	t_{MR}	800			ns	8-MHz CLK Note 4
$\overline{WR}$ ↓ delay from DRQ	t_{MW}	250			ns	
$\overline{WR}$ ↑ or $\overline{RD}$ ↑ response time from DRQ ↑	t_{MRW}			12	μs	

Notes:

(1) Typical values for $T_A = 25°C$ and nominal supply voltage.

(2) Under software control. The range is from 1 ms to 16 ms at 8-MHz clock period, and 2 ms to 32 ms at 4-MHz clock period.

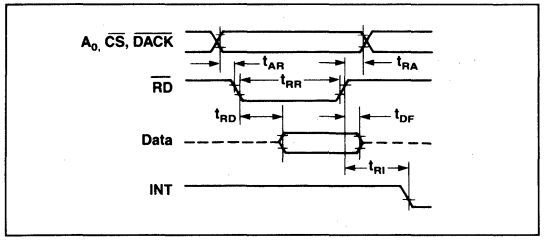
(3) When one device is executing a SEEK operation, SENSE DRIVE STATUS is executed on another device.

(4) Double these values for a 4-MHz clock period.

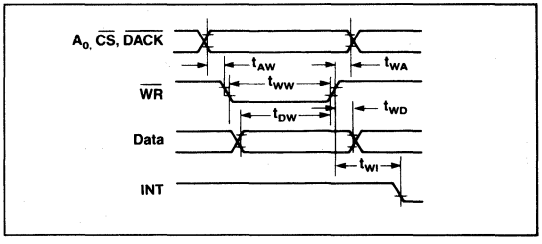
(5) The drive side rating has a variance of −50 ns from the minimum value.

Timing Waveforms

Processor Read Operation



Processor Write Operation



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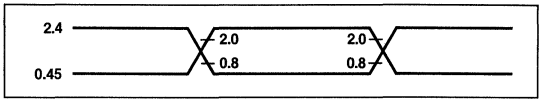
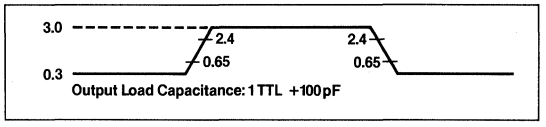
Timing Waveforms (Cont)

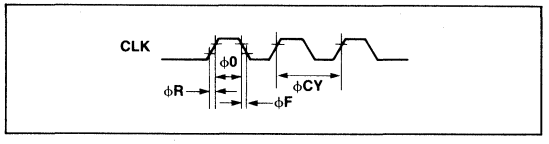
Data Input Waveform for AC Test (Except CLK, WCLK)



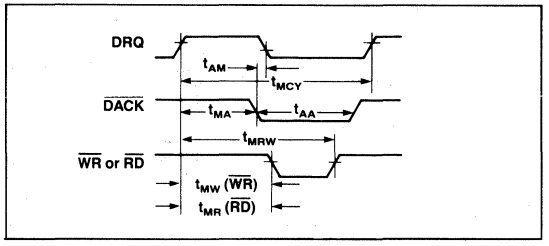
Clock (WCLK, CLK) Input Waveform for AC Test



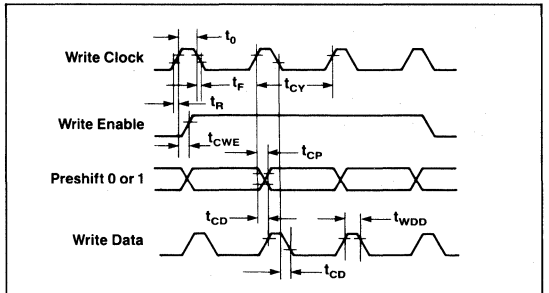
Clock



DMA Operation

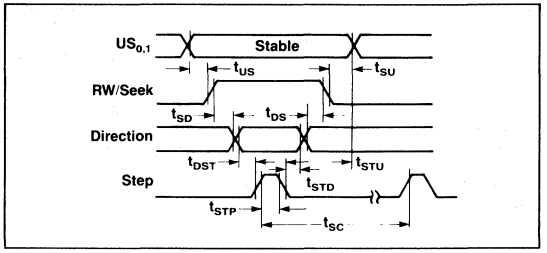


FDD Write Operation

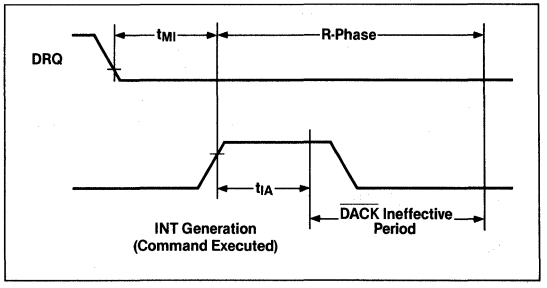


	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

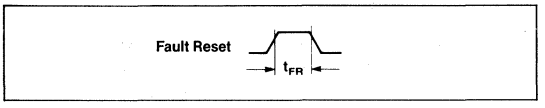
Seek Operation



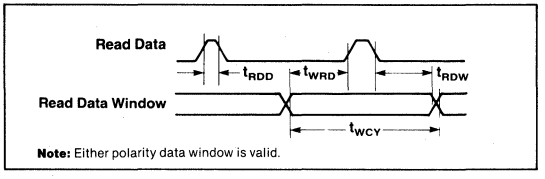
Overrun Operation (μPD765B Only)



FLT Reset

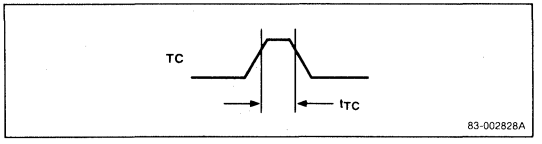


FDD Read Operation

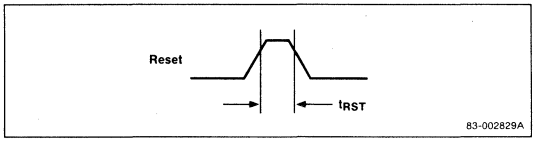


Note: Either polarity data window is valid.

Terminal Count

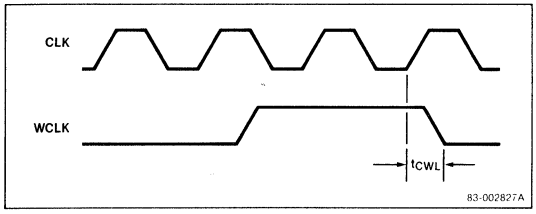


Reset

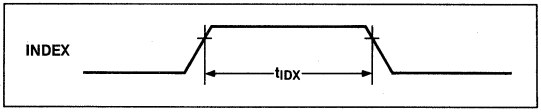


Timing Waveforms (Cont)

Write Clock



Index



Internal Registers

The μPD765A/μPD765B contains two registers which may be accessed by the main system processor: a status register and a data register. The 8-bit main status register contains the status information of the FDC, and may be accessed at any time. The 8-bit data register (which actually consists of four registers, ST0-ST3, in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the data register in order to program or obtain the results after a particular command (table 3). Only the status register may be read and used to facilitate the transfer of data between the processor and μPD765A/μPD765B.

The relationship between the status/data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in table 1.

Table 1. Status/Data Register Addressing

A_0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read main status register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from data register
1	1	0	Write into data register

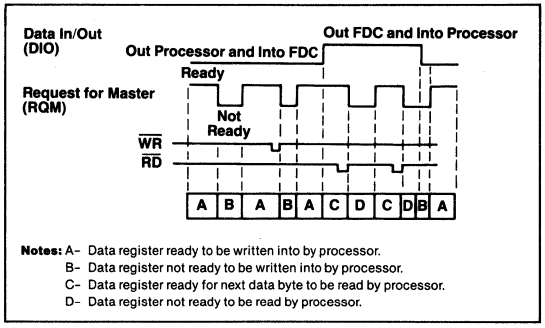
The bits in the main status register are defined in table 2.

Table 2. Main Status Register

Pin No.	Pin Name	Function
DB_0	D_0B (FDD 0 Busy)	FDD number 0 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_1	D_1B (FDD 1 Busy)	FDD number 1 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_2	D_2B (FDD 2 Busy)	FDD number 2 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_3	D_3B (FDD 3 Busy)	FDD number 3 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_4	CB (FDC Busy)	A Read or Write command is in process. FDC will not accept any other command.
DB_5	EXM (Execution Mode)	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
DB_6	DIO (Data Input / Output)	Indicates direction of data transfer between FDC and data register. If DIO=1, then transfer is from data register to the processor. If DIO=0, then transfer is from the processor to data register.
DB_7	RQM (Request for Master)	Indicates data register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the status register indicate when data is ready and in which direction data will be transferred on the data bus. See figure 1.

Figure 1. DIO and RQM



Notes: A- Data register ready to be written into by processor.
B- Data register not ready to be written into by processor.
C- Data register ready for next data byte to be read by processor.
D- Data register not ready to be read by processor.

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Table 3. Status Register Identification

Pin No.	Pin Name	Function
Status Register 0		
D_7, D_6	IC (Interrupt Code)	$D_7=0$ and $D_6=0$ Normal termination of command, (NT). Command was completed and properly executed.
		$D_7=0$ and $D_6=1$ Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
		$D_7=1$ and $D_6=0$ Invalid command issue, (IC). Command which was issued was never started.
		$D_7=1$ and $D_6=1$ Abnormal termination because during command execution the ready signal from FDD changed state.
D_5	SE (Seek End)	When the FDC completes the Seek command, this flag is set to 1 (high).
D_4	EC (Equipment Check)	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	NR (Not Ready)	When the FDD is in the not-ready state and a Read or Write command is issued, this flag is set. If a Read or Write command is issued to side 1 of a single-sided drive, then this flag is set.
D_2	HD (Head Address)	This flag is used to indicate the state of the head at interrupt.
D_1	US_1 (Unit Select 1)	This flag is used to indicate a drive unit number at interrupt.
D_0	US_0 (Unit Select 0)	This flag is used to indicate a drive unit number at interrupt.
Status Register 1		
D_7	EN (End of Cylinder)	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6		Not used. This bit is always 0 (low).
D_5	DE (Data Error)	When the FDC detects a CRC(1) error in either the ID field or the data field, this flag is set.
D_4	OR (Overrun)	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3		Not used. This bit is always 0 (low).

Table 3. Status Register Identification (cont)

Pin No.	Pin Name	Function
Status Register 1 (cont)		
D_2	ND (No Data)	During execution of Read Data, Read Deleted Data, Write Data, Write Deleted Data or Scan command, if the FDC cannot find the sector specified in the IDR(2) Register, this flag is set.
		During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set.
		During execution of the Read Diagnostic command, if the starting sector cannot be found, then this flag is set.
D_1	NW (Not Writable)	During execution of Write Data, Write Deleted Data or Write ID command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	MA (Missing Address Mark)	This bit is set if the FDC does not detect the IDAM before 2 index pulses. It is also set if the FDC cannot find the DAM or DDAM after the IDAM is found, MD bit of ST2 is also set at this time.
Status Register 2		
D_7		Not used. This bit is always 0 (low).
D_6	CM (Control Mark)	During execution of the Read Data or Scan command, if the FDC encounters a sector which contains a deleted data address mark, this flag is set. Also set if DAM is found during Read Deleted Data.
D_5	DD (Data Error in Data Field)	If the FDC detects a CRC error in the data field then this flag is set.
D_4	WC (Wrong Cylinder)	This bit is related to the ND bit, and when the contents of C(3) on the medium is different from that stored in the IDR, this flag is set.
D_3	SH (Scan Equal Hit)	During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set.
D_2	SN (Scan Not Satisfied)	During execution of the Scan command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	BC (Bad Cylinder)	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FFH, then this flag is set.
D_0	MD (Missing Address Mark in Data Field)	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set.

Table 3. Status Register Identification (cont)

Pin No.	Name	Function
Status Register 3		
D_7	FT (Fault)	This bit is used to indicate the status of the fault signal from the FDD.
D_6	WP (Write Protected)	This bit is used to indicate the status of the write protected signal from the FDD.
D_5	RY (Ready)	This bit is used to indicate the status of the ready signal from the FDD.
D_4	T0 (Track 0)	This bit is used to indicate the status of the track 0 signal from the FDD.
D_3	TS (Two-Side)	This bit is used to indicate the status of the two-side signal from the FDD.
D_2	HD (Head Address)	This bit is used to indicate the status of the side select signal to the FDD.
D_1	US_1 (Unit Select 1)	This bit is used to indicate the status of the unit select 1 signal to the FDD.
D_0	US_0 (Unit Select 0)	This bit is used to indicate the status of the unit select 0 signal to the FDD.

Note:
(1) CRC = Cyclic Redundancy Check
(2) IDR = Internal Data Register
(3) Cylinder (C) is described more fully in the Command Symbol Description.

Command Sequence

The μPD765A/μPD765B is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the μPD765A/μPD765B and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

Table 4 shows the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written, and an "R" indicates a result byte. The definitions of other abbriviations used in table are given in the Command Symbol Description table.

Command Symbol Description

Name	Function
A_0 (Address Line 0)	A_0 controls selection of main status register ($A_0=0$) or data register ($A_0=1$).
C (Cylinder Number)	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
D (Data)	D stands for the data pattern which is going to be written into a sector during WRITE ID operation.
D_7–D_0 (Data Bus)	8-bit data bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL (Data Length)	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT (End of Track)	EOT stands for the final sector number on a cylinder. During read or write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL (Gap Length)	GPL stands for the length of gap 3. During Read/Write commands this value determines the number of bytes that VCO sync will stay low after two CRC bytes. During Format command it determines the size of gap 3.
H (Head Address)	H stands for the logical head number 0 or 1, as specified in ID field.
HD (Head)	HD stands for a the physical head number 0 or 1 and controls the polarity of pin 27. (H=HD in all command words.)
HLT (Head Load Time)	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT (Head Unload Time)	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF (FM or MFM Mode)	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT (Multitrack)	IF MT is high, a multitrack operation is performed. If MT=1 after finishing read/write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N (Number)	N stands for the number of data bytes written in a sector.
NCN (New Cylinder Number)	NCN stands for a new cylinder number which is going to be reached as a result of the seek operation; desired position of head.
ND (Non-DMA Mode)	ND stands for operation in the non-DMA mode.
PCN (Present Cylinder Number)	PCN stands for the cylinder number at the completion of Sense Interrupt Status command, position of head at present time.
R (Record)	R stands for the sector number which will be read or written.
R/W (Read/Write)	R/W stands for either Read (R) or Write (W) signal.
SC (Sector)	SC indicates the number of sectors per cylinder.
SK (Skip)	SK stands for skip deleted data address mark.

Command Symbol Description (cont)

Name	Function
SRT (Step Rate Time)	SRT stands for the stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (FH = 1 ms, EH = 2 ms, etc.).
ST0–ST3 (Status 0–3)	ST0–ST3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST0–ST3 may be read only after a command has been executed and contains information relevant to that particular command.

Command Symbol Description (cont)

Name	Function
STP	During a scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US_0, US_1 (Unit Select)	US stands for a selected drive number 0 or 3.

Table 4. Instruction Set (Notes 1, 2)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	(Note 3)
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

Note:
(1) Symbols used in this table are described at the end of this section.
(2) A_0 should equal 1 for all operations.
(3) X = Don't care, usually made to equal 0.

Table 4. Instruction Set (Notes 1, 2) (cont)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the main system and FDD
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Read Diagnostic										
Command	W	0	MF	SK	0	0	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

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Table 4. Instruction Set (Notes 1, 2) (cont)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in data register.
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information read during execution phase from floppy disk.
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Write ID [Format Write]										
Command	W	0	MF	0	0	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				N			→	Bytes / sector
	W	←				SC			→	Sectors / track
	W	←				GPL			→	Gap 3
	W	←				D			→	Filler byte
Execution										FDC formats an entire track.
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	In this case, the ID information has no meaning
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				STP			→	
Execution										Data compared between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

Note:
(1) Symbols used in this table are described at the end of this section.
(2) A_0 should equal 1 for all operations.
(3) X = Don't care, usually made to equal 0.

Table 4. Instruction Set (Notes 1, 2) (cont)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				STP			→	
Execution										Data compared between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				STP			→	
Execution										Data compared between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to track 0
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command codes
Result	R	←				ST0			→	Status information about the FDC at the end of seek operation
	R	←				PCN			→	
Specify										
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	←		SRT		→	←		HUT	→
	W	←			HLT			→		ND
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Result	R	←				ST3			→	Status information about FDD

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Table 4. Instruction Set (Notes 1, 2) (cont)

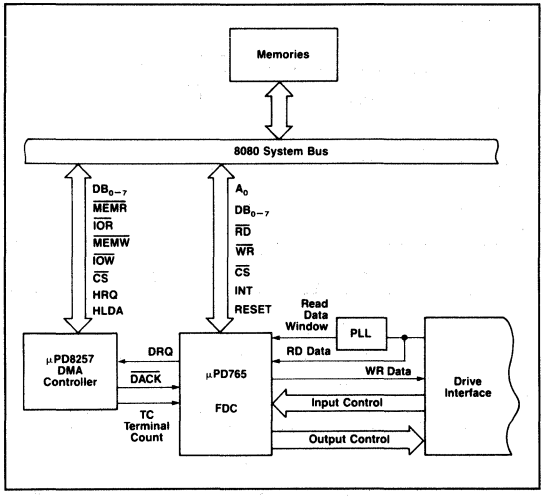
Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Version										
Command	W	X	X	X	1	0	0	0	0	Command codes
Result	R	←			ST0				→	90H indicates 765B 80H indicates 765A / A-2
Seek										
Command	W	0	0	0	0	1	1	1	1	Command code
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			NCN				→	
Execution										Head is positioned over proper cylinder on diskette
Invalid										
Command	W	←			Invalid Codes				→	Invalid Command codes (No op — FDC goes into state)
Result	R	←			ST0				→	ST0 = 80H

Note:
(1) Symbols used in this table are described at the end of this section.
(2) A_0 should equal 1 for all operations.
(3) X = Don't care, usually made to equal 0.

System Configuration

Figure 2 shows an example of a system using a μPD765A/B.

Figure 2. System Configuration



Data Format

Figure 3 shows the data transfer format for the μPD765A and μPD765B in FM and MFM modes. Figure 4 shows VCO Sync timing.

Figure 3. Data Format

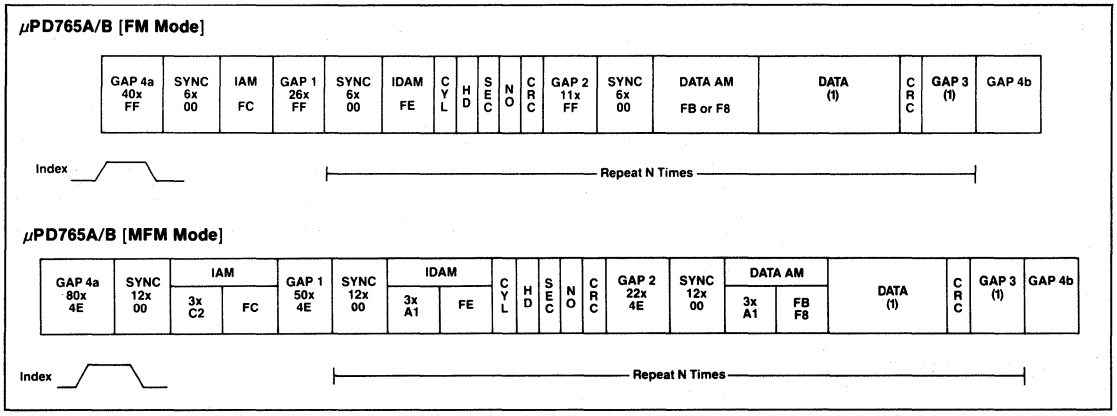
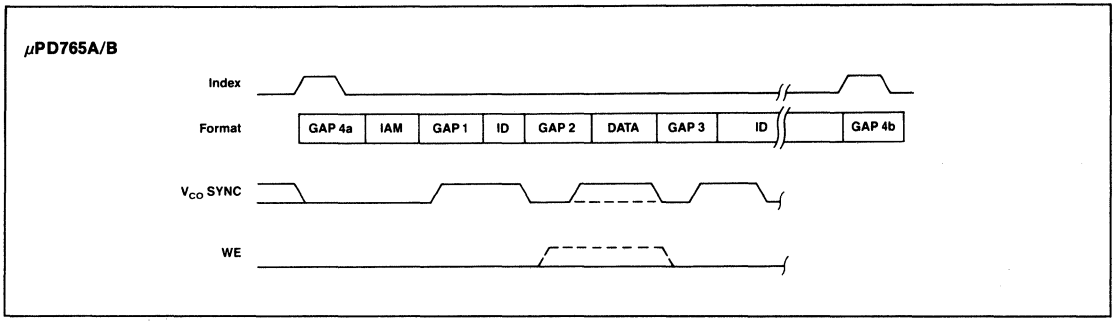


Figure 4. VCO Sync Timing



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Description

The μPD71065 and μPD71066 are CMOS devices that interface a floppy-disk drive (FDD) with a floppy-disk controller (FDC). The controller can be μPD765A/B, μPD7265, μPD72065/B, μPD72066, μPD7260, or one of the FD179X series.

The floppy-disk interface can operate at various data rates, including the 300-kb/s rate that results from using high-density 5-inch drives with media formatted at the standard 250-kb/s rate. Also, the μPD71065/66 generates the write clock needed by the selected controller and provides synchronous switching when changing data rates.

Features

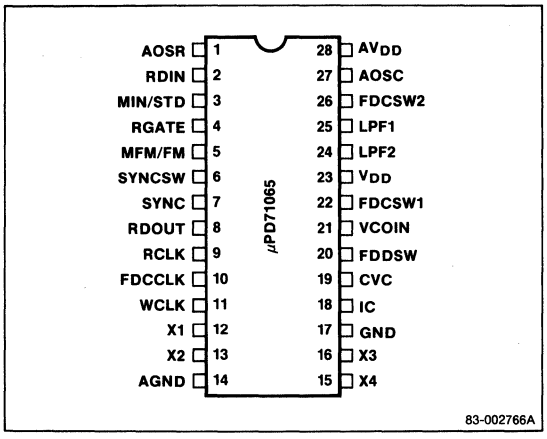
- ☐ Compatible with all industry-standard controllers
- ☐ Multiple data rates: 500/300/250/150/125 kb/s
- ☐ Internal or external sync field detection logic
- ☐ Head-loading timer for FD179X-series controllers
- ☐ No analog adjustments required
- ☐ CMOS, low power consumption
- ☐ 5-volt power supply

Ordering Information

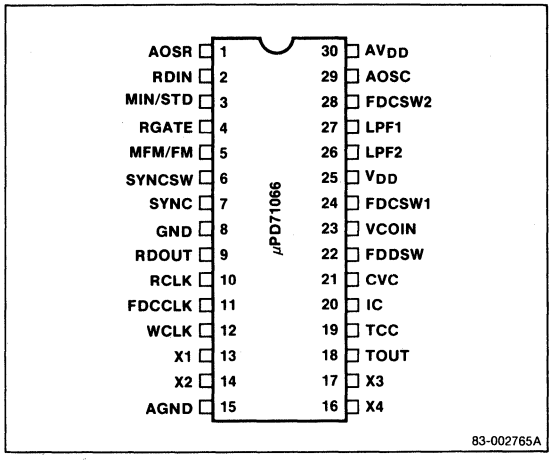
Part Number	Package	Internal Timer
μPD71065G	28-pin plastic SO	Not included
μPD71066CT	30-pin plastic shrink DIP	Implemented to FD179X-series controllers as head-loading timer.

Pin Configurations

28-Pin Plastic SO



30-Pin Plastic Shrink DIP



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Pin Identification

Symbol	Input/Output	Function
ACOS		Capacitor connection pin for analog one-shot
AGND		Ground for analog circuits
AOSR		Resistor connection pin for analog one-shot
AV_{DD}		Power supply for analog circuits
CVC		Capacitor connection pin for VCO
FDCCLK	Output	Clock to FDC
FDCSW1	Input*	FDC selection pin or timer trigger input
FDCSW2	Input*	FDC selection pin
FDDSW	Input*	Data transfer rate selection pin
GND		Ground
IC		Internally connected; should be left open
LPF1, LPF2	Output	Connection pins to external lowpass filter
MFM/FM	Input*	Recording density selection pin
MIN/STD	Input*	5- or 8-inch FDD selection pin
RCLK	Output	Read data sampling clock
RDOUT	Output	Read data to FDC
RGATE	Input*	Read enable/disable
RDIN	Input*	Read data from FDD
SYNC	Input*	External PLL gain selection
SYNCSW	Input*	Determines whether gain selection is internal or external
TCC		External RC time constant connection to internal timer (μPD71066)
TOUT	Output	Timer signal (μPD71066)
VCOIN	Input	External lowpass filter output to internal VCO
V_{DD}		+5-volt power supply
WCLK	Output	Write clock to FDC
X1, X2		Connection pins for 16-MHz crystal (X1, X2) or external clock input (X1)
X3, X4		Connection pins for 19.2-MHz crystal (X3, X4) or external clock input (X3)

*Input pin has an on-chip pull-up resistor

Pin Functions

The following paragraphs supplement the brief descriptions of certain pins in the preceding table. Pin symbols are in alphabetical order.

FDCSW1 and FDCSW2. The μPD71065/66 is configured for the applicable FDC by applying logic levels L and H (or open) to these pins.

FDCSW1	FDCSW2	Floppy-Disk Controller
Open or H	Open or H	μPD765A/7265
L	Open or H	μPD7260
*	L	FD179X series

* FDCSW1 is the trigger input to the timer circuit when FDCSW2 is low.

FDDSW. The logic level applied to this pin selects the data transfer rate of the FDD.

FDDSW	Data Transfer Rate
Open or H	500/250/125 kb/s
L	500/250/300/150 kb/s

MFM/FM Pin. The logic level applied to this pin and the FDCSW2 pin selects the modulation type. Double-density and single-density recording use MFM (modified FM) and FM modulation, respectively.

FDCSW2	MFM/FM	Modulation
H	H	MFM
H	L	FM
L	H	FM
L	L	MFM

MIN/STD. Logic level L on this pin selects a 5-inch FDD. An open or H selects an 8-inch FDD.

RDIN. This is a composite read data and clock signal input from the FDD.

RDOUT. The read data output from this pin is synchronized with the read clock (RCLK) derived from the RDIN composite signal.

RGATE. In conjuction with FDCSW2, RGATE enables or disables the read operation that is sent from the FDC.

FDCSW2	RGATE	Read Operation
H	H	Enable
H	L	Disable
L	H	Disable
L	L	Enable

SYNC and SYNCSW. The PLL gain is determined by the intput signal at the SYNC pin and the logic levels at the FDCSW1 and SYNCSW pins.

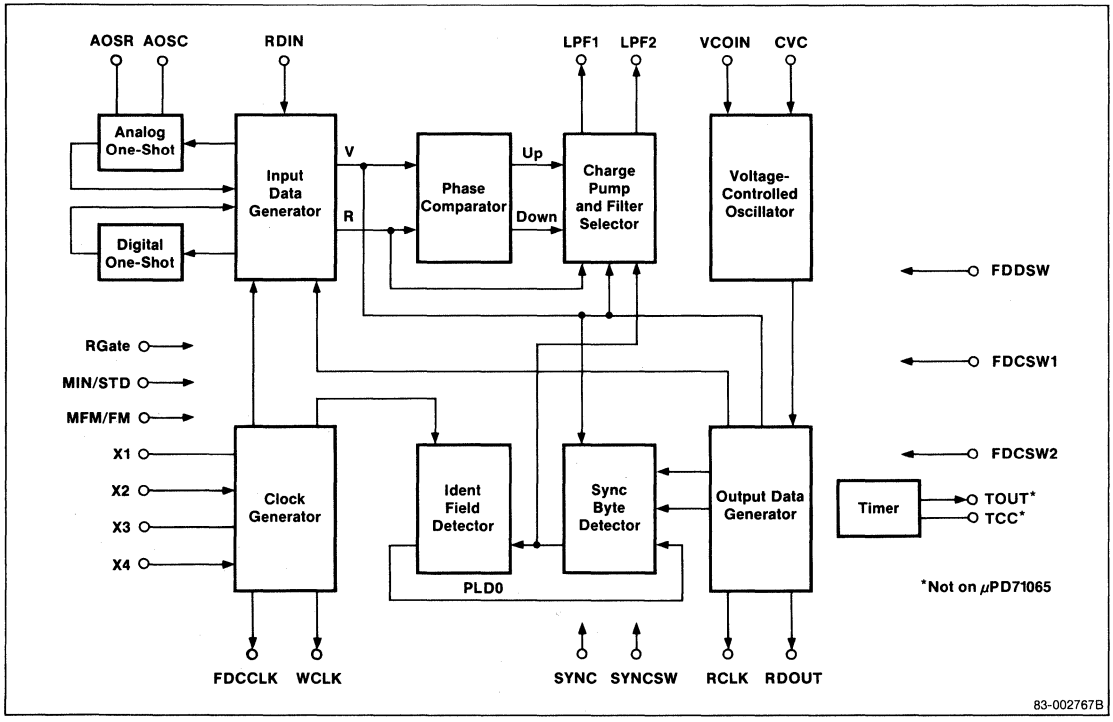
FDCSW1	SYNCSW	SYNC	PLL Gain
Open or H	Open or H	H (1)	Low
		L (1)	High
	L	H (2)	Low
		L (2)	High

Note:

(1) Input signal at SYNC is the PLL gain selection signal between the ID and DATA fields.

(2) Input signal at SYNC Is the SYNC field detection signal from the FDC.

Block Diagram



Functions of the block diagram components are explained below.

Clock Generator. Using both 16-MHz and 19.2-MHz oscillators, outputs clock signals corresponding to the mode used to the FDCCLK and WCLK pins.

Input Data Generator. According to the input data, generates the R and V signals to be input to the phase comparator. In addition to this, the input data generator determines whether the analog one-shot circuit or the digital one-shot circuit is used.

Charge Pump and Filter Selector. According to the PLL (phase-locked loop) gain selection signal, enables or disables the LPF2 side charge pump to control the PLL gain.

Output Data Generator. Generates the window signal (RCLK) and read data signal (RDOUT) depending on the mode and FDC to be used.

Sync Byte Detector. Detects the sync field within 16 to 20 pulses regardless of FM or MFM mode.

Ident Field Detector. Determines whether the sync field detected by the sync byte detector is ID or DATA field and sets the PLL gain.

Basic External Circuit

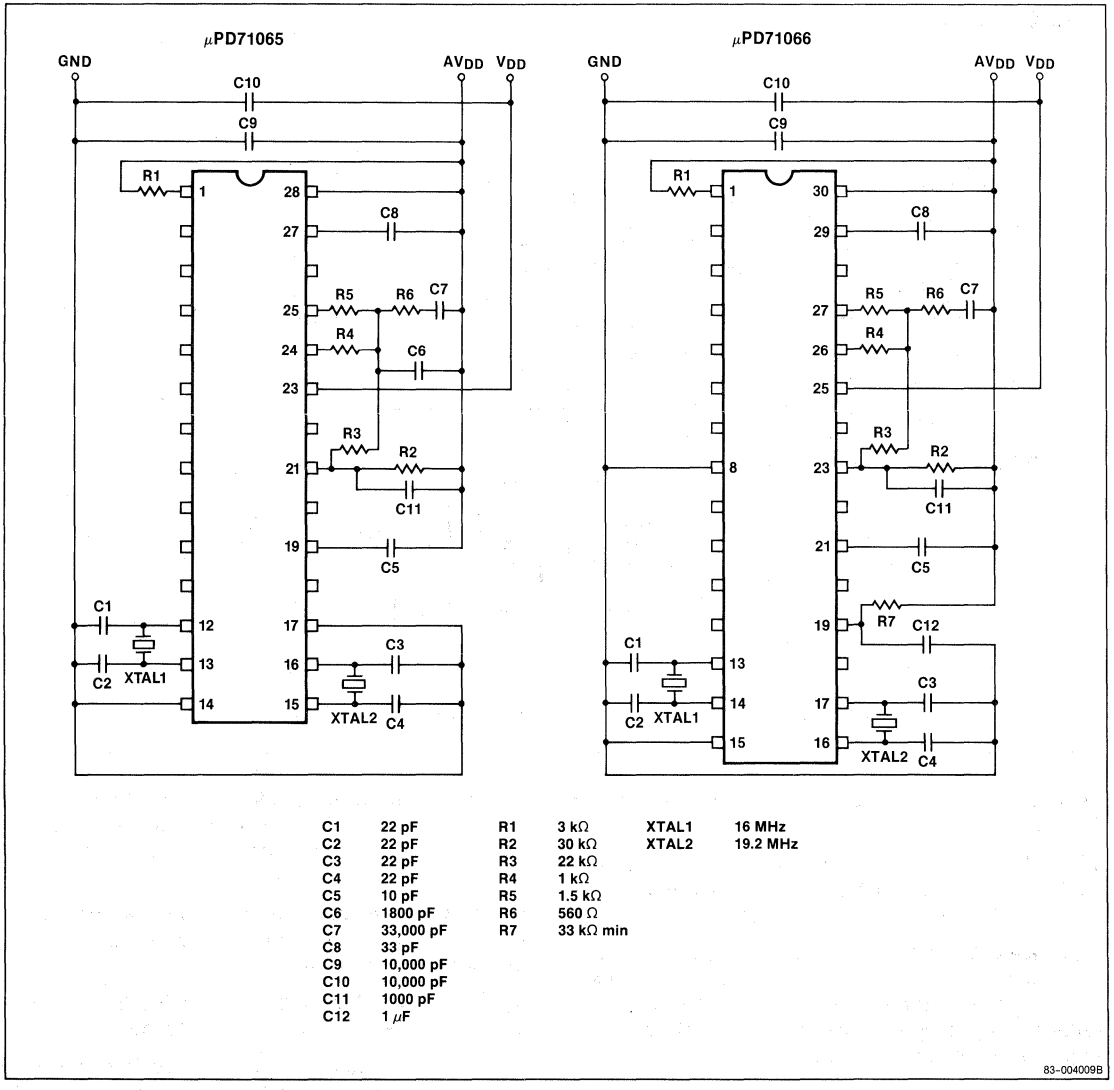
Figure 1 shows the basic external circuit including the lowpass filter and crystals. The data transfer rate is selected by strapping pins FDDSW, MIN/STD, and MFM/FM to L (low) or open (high). See table 1.

The VCO frequency and the phase delay between RDIN and RDOUT can be optimized by adjusting resistors R2 and R1, respectively.

VCO Frequency

For this procedure, the data transfer rate is undefined. Strap RGATE to H and RDIN to L. Adjust resistor R2 to set the VCO frequency at the RCLK pin to the same numerical value as the data transfer rate; for example, 500 kHz and 500 kb/s.

Figure 1. Basic External Circuit



C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	30 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	22 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	1.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	33,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	1000 pF				
C12	1 μF				

Data Read Phase Delay

For this procedure, set the data transfer rate to 500 kb/s, set the RDIN signal to a 2-μs cycle time, and strap RGATE to H. Adjust resistor R1 to set the value of t_{STW} (figure 2) to 950 ns.

Figure 2. Read Data Timing Diagram

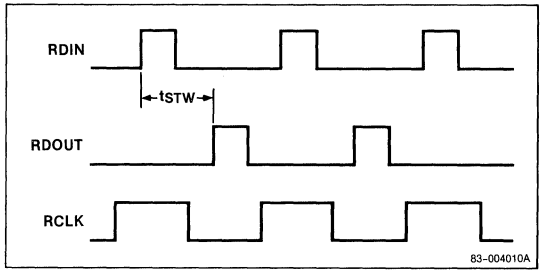


Table 1. Data Transfer Rate Selection

Floppy-Disk Controllers	Data Transfer Rate (kb/s)	Clock Output Frequencies from μPD71065/71066			Selection Pins (Note 1)		
		FDCCLK (MHz)	RCLK (kHz)	WCLK (kHz)	FDDSW	MIN/STD	MFM/FM
μPD765A, μPD7265, μPD72065, μPD72066 (Note 2)	250	4	250	500	Open	Open	Open
	125	4	125	250	Open	Open	L
	500	8	500	1 MHz	Open	L	Open
	250	8	250	500	Open	L	L
	300	4.8	300	600	L	Open	Open
	150	4.8	150	300	L	Open	L
	500	8	500	1 MHz	L	L	Open
	250	8	250	500	L	L	L
μPD7260 (Note 3)	250	4	500	500	Open	Open	Open
	125	4	250	250	Open	Open	L
	500	8	1 MHz	1 MHz	Open	L	Open
	250	8	500	500	Open	L	L
	300	4.8	600	600	L	Open	Open
	150	4.8	300	300	L	Open	L
	500	8	1 MHz	1 MHz	L	L	Open
	250	8	500	500	L	L	L
FD179X Series (Note 4)	250	1	250	500	Open	Open	L
	125	1	125	250	Open	Open	Open
	500	2	500	1 MHz	Open	L	L
	250	2	250	500	Open	L	Open
	300	1.2	300	600	L	Open	L
	150	1.2	150	300	L	Open	Open
	500	2	500	1 MHz	L	L	L
	250	2	250	500	L	L	Open

Note:

(1) Selection pin states: L = low; Open = open or H (high)

(2) μPD765A/7265/72065/72066:
FDCSW1 and FDCSW2 = Open

(3) μPD7260:
FDCSW1 = L and FDCSW2 = Open.
FDCLK clock is not used

(4) FD179X Series:
FDCSW1 = Don't care and FDCSW2 = L.
WCLK clock is not used.

Electrical Characteristics

Figures 3 through 8 are test circuits for verifying certain parameters in the dc and ac characteristics tables.

Absolute Maximum Ratings

$T_A = +25°C$

Power supply voltage, V_{DD}	−0.3 to +6 V
Input voltage, V_I	−0.3 to V_{DD} + 0.3 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
Operation temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−40 to +125°C

DC Characteristics

$T_A = -10$ to $+70°C$; $V_{DD} = +5$ V ±10%

		Limits					
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	Test Circuit
Input voltage, low	V_{IL}	−0.3		0.8	V		
Input voltage, high	V_{IH}	2.2		V_{DD} + 0.3	V		
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2 mA	
Output voltage, high	V_{OH}	0.7 V_{DD}		V_{DD}	V	I_{OH} = − 200 μA	
Clock input level	V_{KP-P}	1		V_{DD}	V		Figure 5
Input leakage current, low	I_{LIL}	−150		−50	μA	V_I = 0 V	
Input leakage current, high	I_{LIH}	−10		+10	μA	$V_I = V_{DD}$	
Output leakage current, low	I_{LOL}	−10			μA	V_O = 0.45 V	
Output leakage current, high	I_{LOH}			+10	μA	$V_O = V_{DD}$	
Power supply current	I_{DD}			25	mA	XTAL: 16 MHz, 19.2 MHz	Figure 3
				20	mA	XTAL: 16 MHz	Figure 4

AC Characteristics

$T_A = -10$ to $+70°C$; $V_{DD} = +5$ V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	Test Circuit
Rise time	t_R	0		20	ns		
Fall time	t_F	0		20	ns		
RDOUT setup time to RCLK ↑	t_{SRR}	40			ns	For μPD7260	Figure 6
CLK high/low level width	t_{KK}	20			ns		
VCO oscillation frequency	f_o			8	MHz	$V_F = V_{DD}$	Figure 7
VCO free-run frequency	f_i	3.6	4	4.4	MHz	FDDSW = H, V_F = open	
		2.1	2.4	2.7	MHz	FDDSW = L, V_F = open	
VCO control voltage sensitivity	K_V	2.5	3.5	4.6	MHz/V	$\lvert(V_{DD}/2) - V_F\rvert \leq 0.5$ V	
K_V voltage coefficient	$\Delta K_V/V_{DD}$	−1	−19	−22	%/V		
f_i power supply voltage coefficient	$\Delta f_i/V_{DD}$	0		5	%/V		
f_i temperature coefficient	$\Delta f_i/T_A$	0	−500	−1000	ppm/°C		
Phase detect sensitivity	K_P	0.7	0.8	0.9	V/rad		
RCLK jitter	t_j	0	30	50	ns	500-kb/s mode	Figure 8
RDIN ↑ to RDOUT ↑ delay time	t_{DRR}	900	950	1000	ns		
Capture range (Note 1)	f_{CAP}	537		427	kHz	500-kb/s mode	
		286		213	kHz	250-kb/s mode	
		143		107	kHz	125-kb/s mode	
		343		256	kHz	300-kb/s mode	
		172		128	kHz	150-kb/s mode	
FDCCLK ↑ to WCLK ↑ delay time (Note 2)	t_{DFWR}			30	ns	$C_L = 15$ pF	Figure 1
FDCCLK ↑ to WCLK ↓ delay time (Note 2)	t_{DFWF}			30	ns	$C_L = 15$ pF	

Note:

(1) The frequencies in the Max and Min columns are the lower and upper limits, respectively, of the capture range. For example, in the 500-kb/s mode, the capture range is from 427 kHz (or lower) to 537 kHz (or higher).

(2) Clock outputs to FDC.

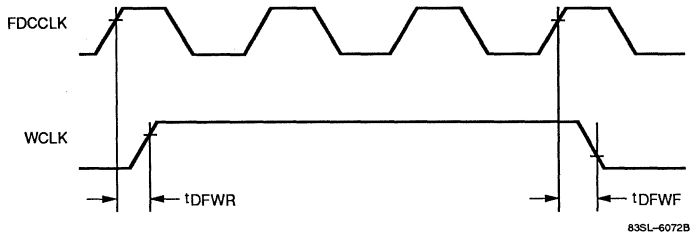
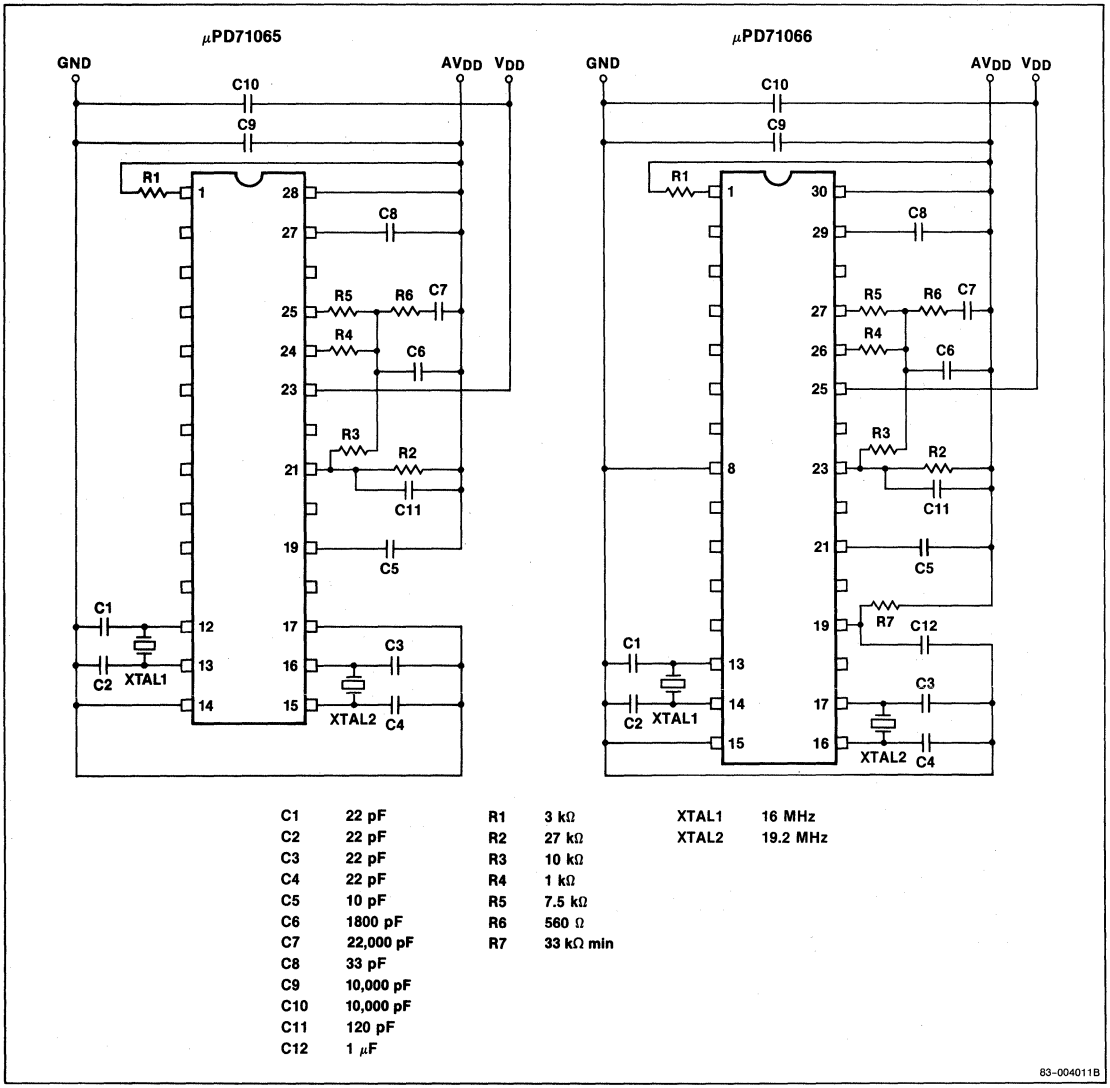


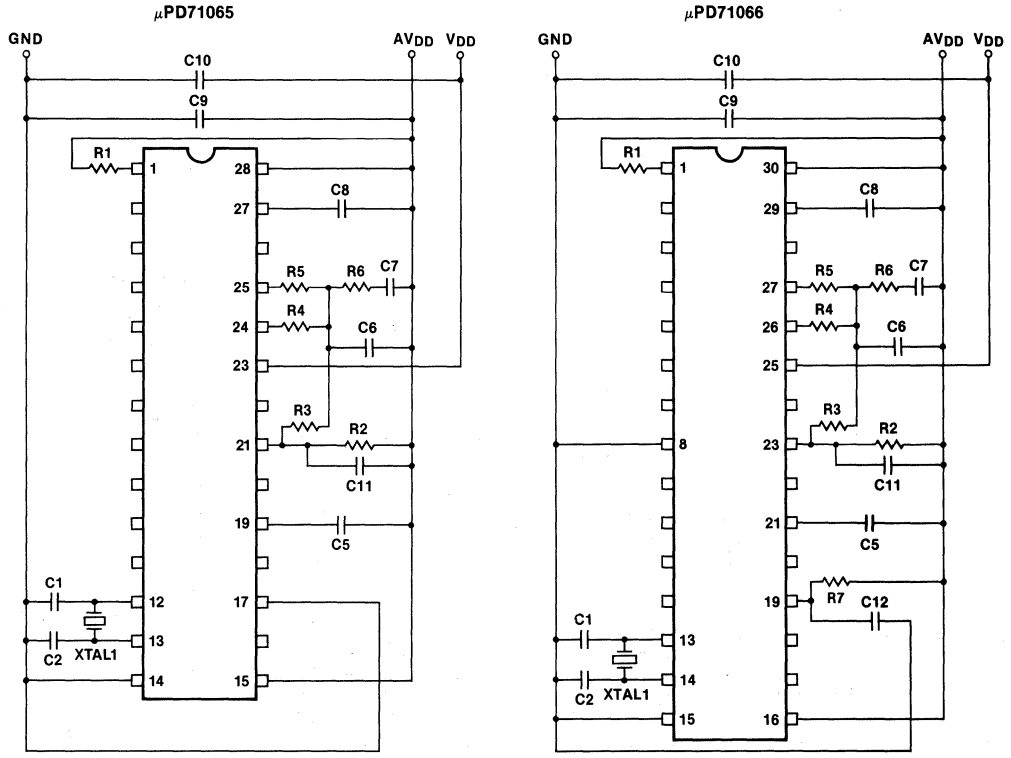
Figure 3. Test Circuit 1



C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	27 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	10 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	7.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	22,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

83-004011B

Figure 4. Test Circuit 2



C1	22 pF	R1	3 kΩ	XTAL	16 MHz
C2	22 pF	R2	27 kΩ		
C5	10 pF	R3	10 kΩ		
C6	1800 pF	R4	1 kΩ		
C7	22,000 pF	R5	7.5 kΩ		
C8	33 pF	R6	560 Ω		
C9	10,000 pF	R7	33 kΩ min		
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

83-004012B

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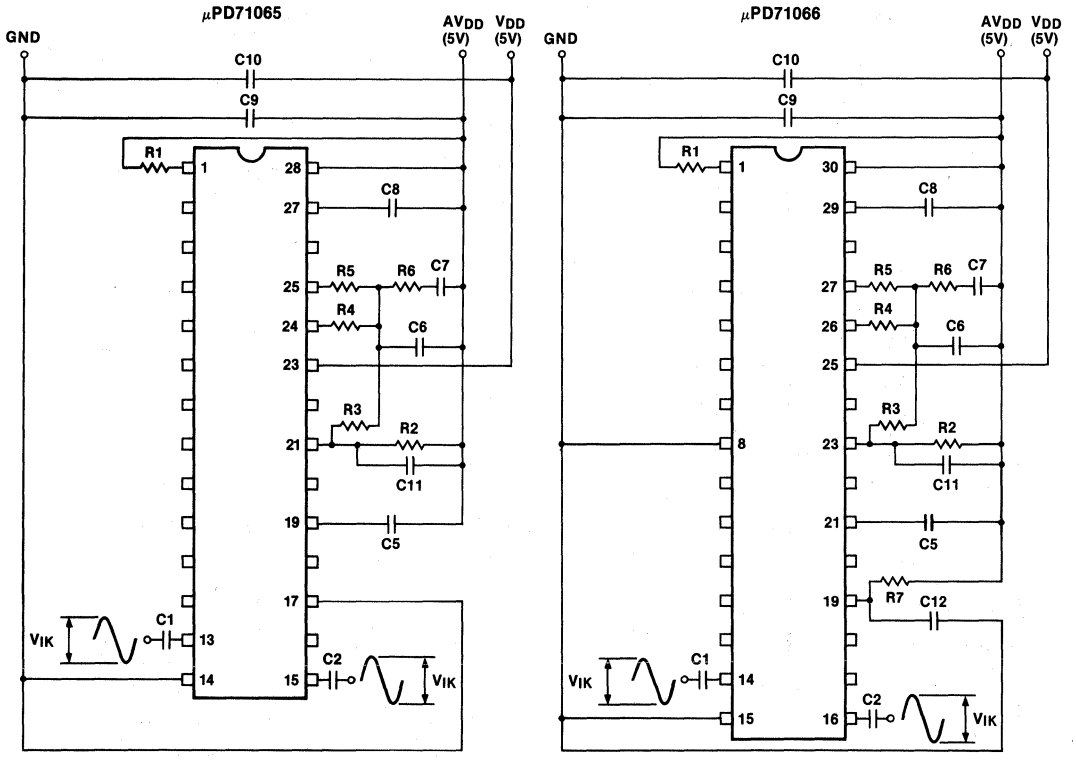
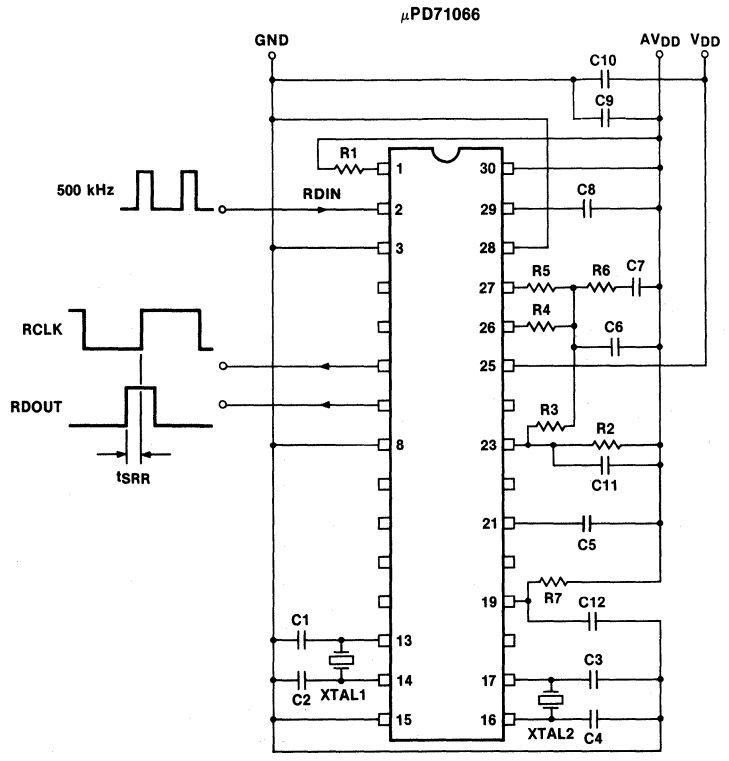
Figure 5. Test Circuit 3



C1	22 pF	R1	3 kΩ
C2	22 pF	R2	27 kΩ
C5	10 pF	R3	10 kΩ
C6	1800 pF	R4	1 kΩ
C7	22,000 pF	R5	7.5 kΩ
C8	33 pF	R6	560 Ω
C9	10,000 pF	R7	33 kΩ min
C10	10,000 pF		
C11	120 pF		
C12	1 μF		

83-004013B

Figure 6. Test Circuit 4



C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	27 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	10 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	7.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	22,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

83-004015B

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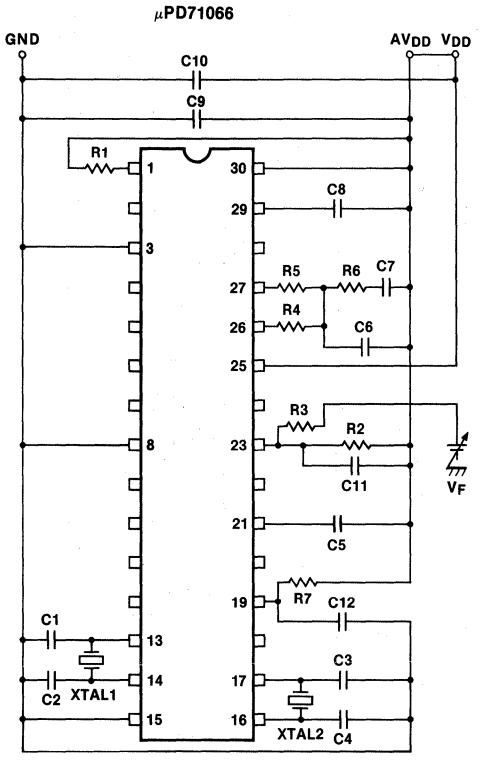
Figure 7. Test Circuit 5

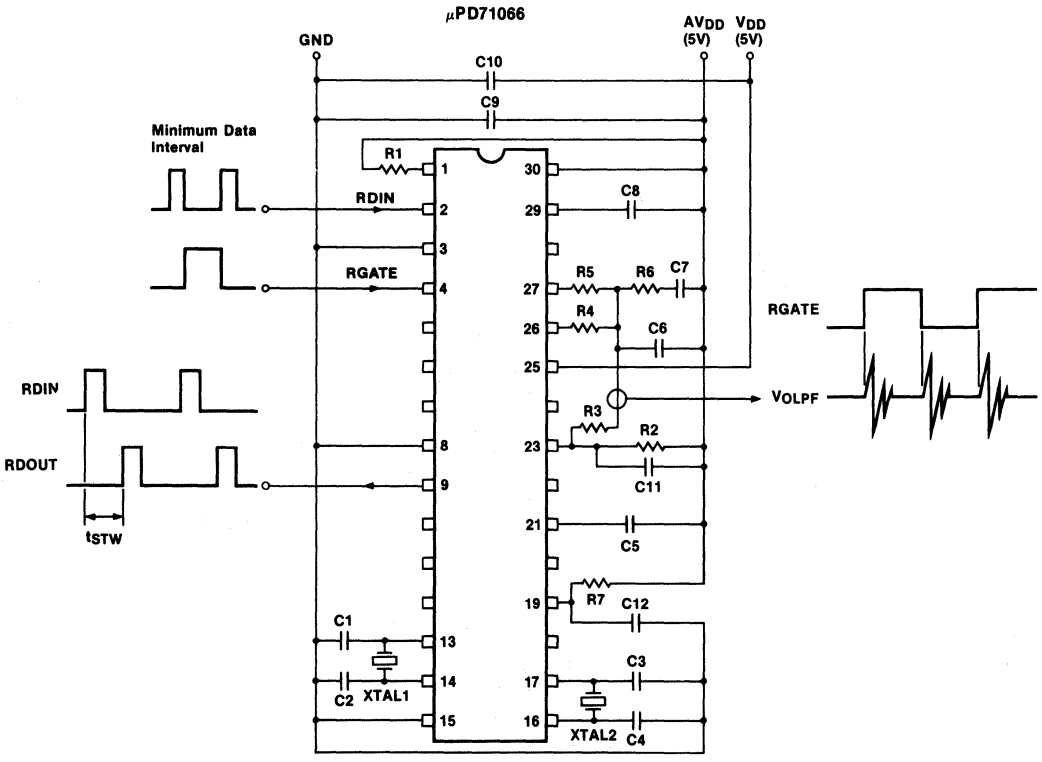


$f_X = 8f_{RCLK}$

C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	27 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	10 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	7.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	22,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

83-004014B

Figure 8. Test Circuit 6



$$f = \frac{1}{400 \times (\text{Min Data Interval})}$$

Duty = 50%

C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	27 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	10 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	7.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	22,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

83-004016B

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System Configurations

Figures 9 through 23 are system configuration examples of the μPD71065 and μPD71066 with various floppy-disk controllers and data transfer rates. See table 2.

For additional details and the values of resistors and capacitors, see figure 1.

Table 2. System Configuration Examples

Floppy-Disk Interface	Floppy-Disk Controllers	Data Transfer Rates (kb/s)	Figure
μPD71065	μPD765A, μPD7265, μPD72065, μPD72066	500/250/125	9
		300/150	10
		500/250/125 and 300/150	11
	μPD7260	500/250/125	12
		300/150	13
		500/250/125 and 300/150	14
μPD71066	μPD765A, μPD7265, μPD72065, μPD72066	500/250/125	15
		300/150	16
		500/250/125 and 300/150	17
	μPD7260	500/250/125	18
		300/150	19
		500/250/125 and 300/150	20
	FD179X	500/250/125	21
		300/150	22
		500/250/125 and 300/150	23

Figure 9. System Example 1: μPD71065 FDI and μPD765A FDC

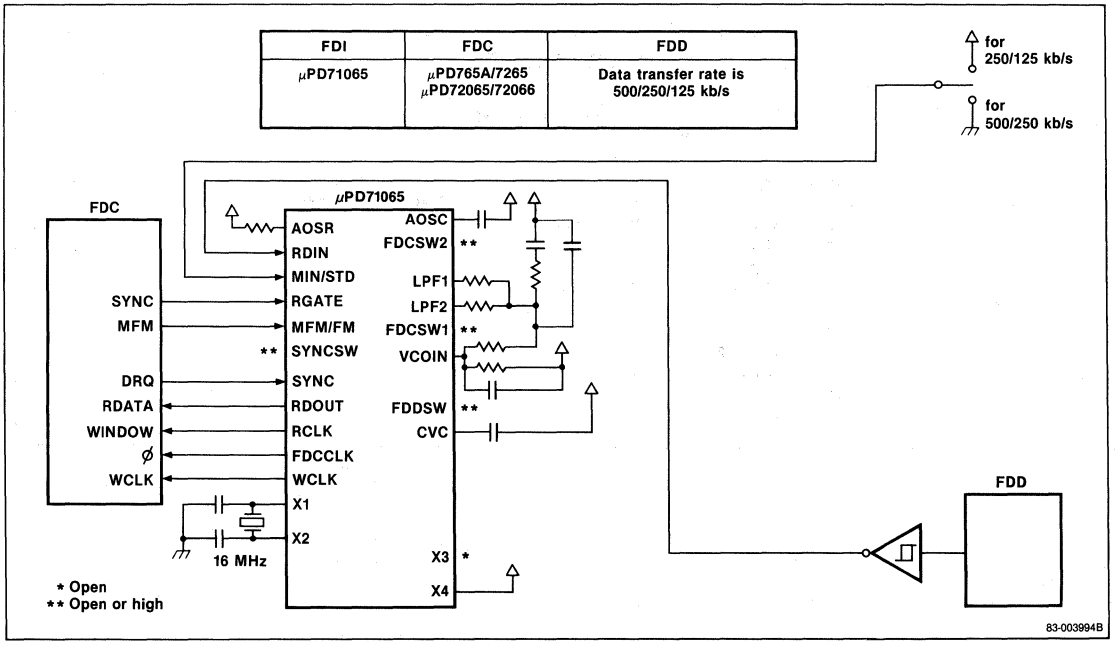

Figure 10. System Example 2: μPD71065 FDI and μPD765A FDC

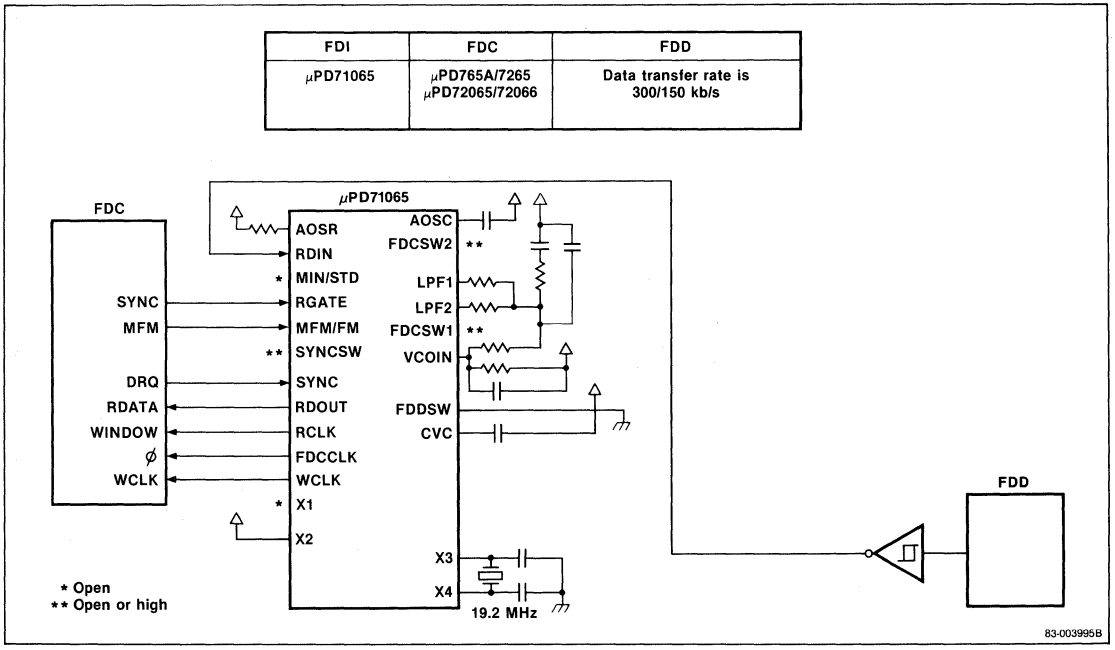

Figure 11. System Example 3: μPD71065 FDI and μPD765A FDC

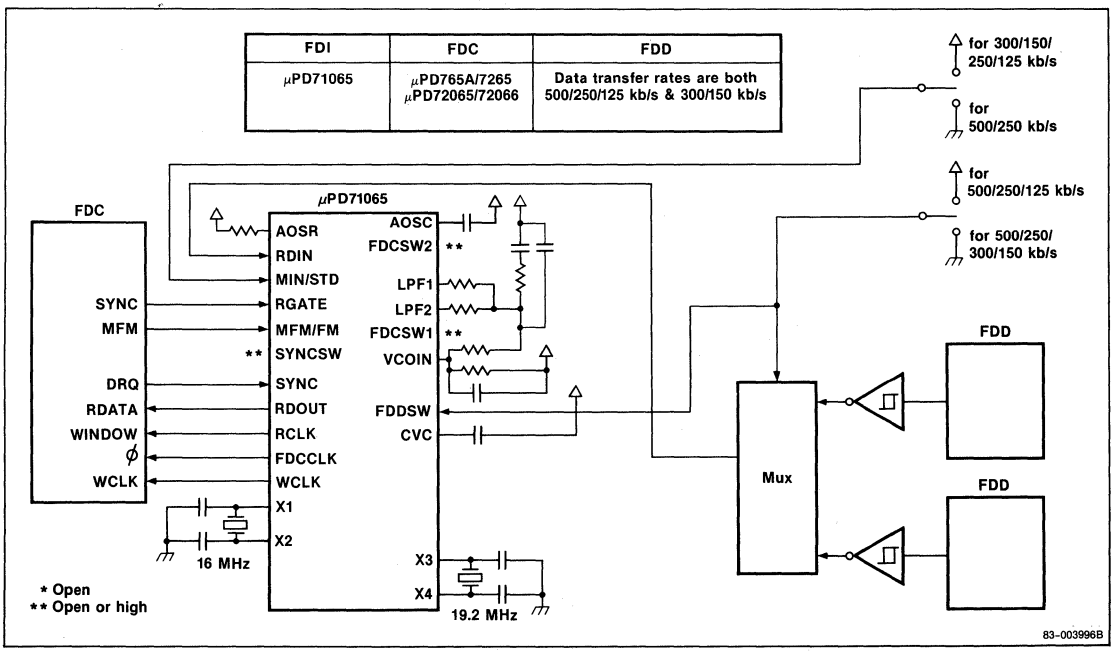

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Figure 12. System Example 4: μPD71065 FDI and μPD7260 FDC

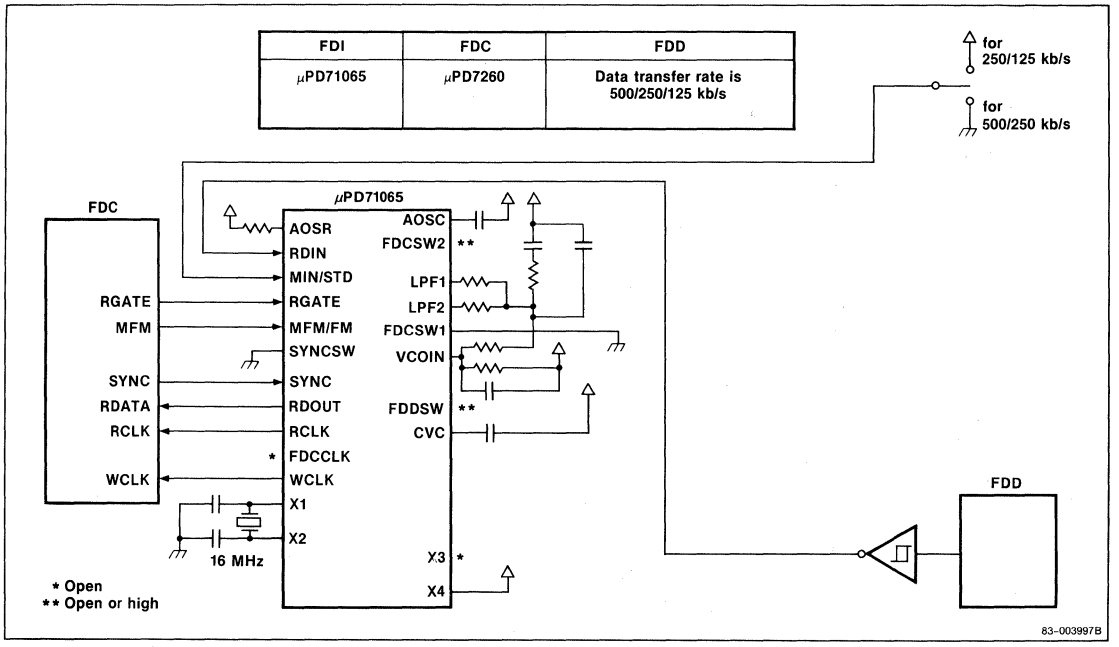

Figure 13. System Example 5: μPD71065 FDI and μPD7260 FDC

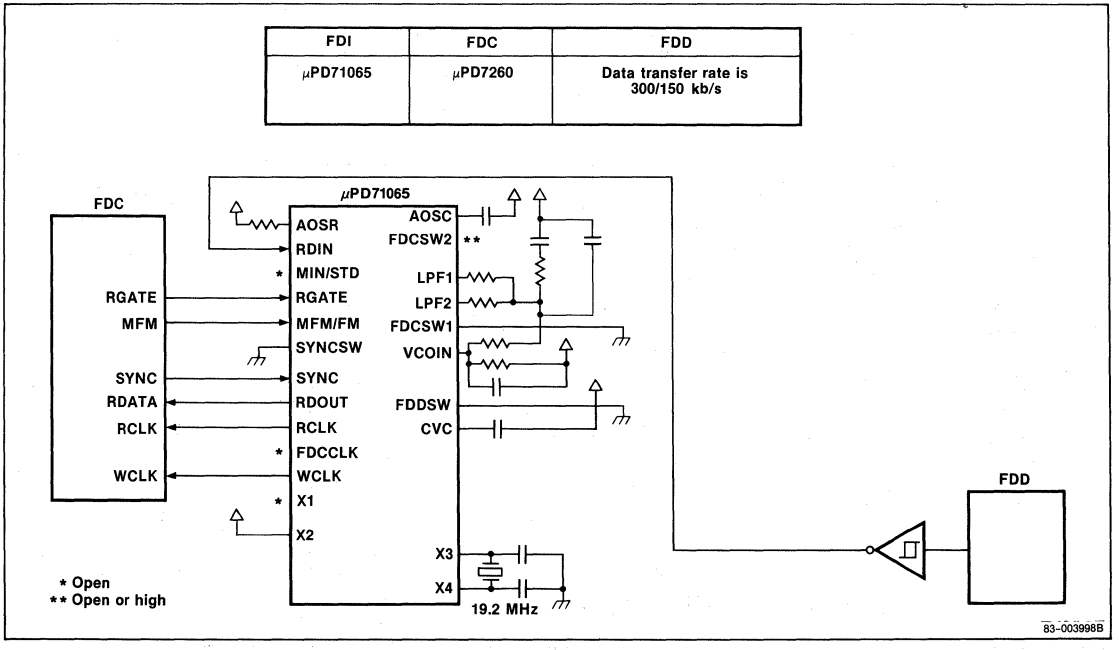

Figure 14. System Example 6: μPD71065 FDI and μPD7260 FDC

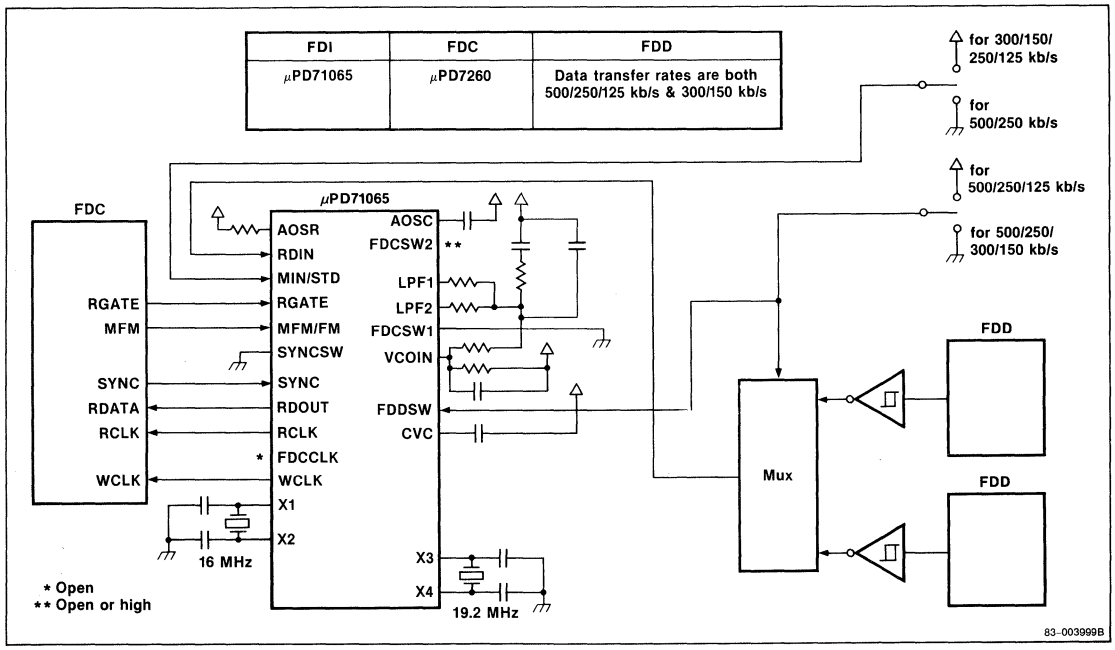

Figure 15. System Example 7: μPD71066 FDI and μPD765A FDC

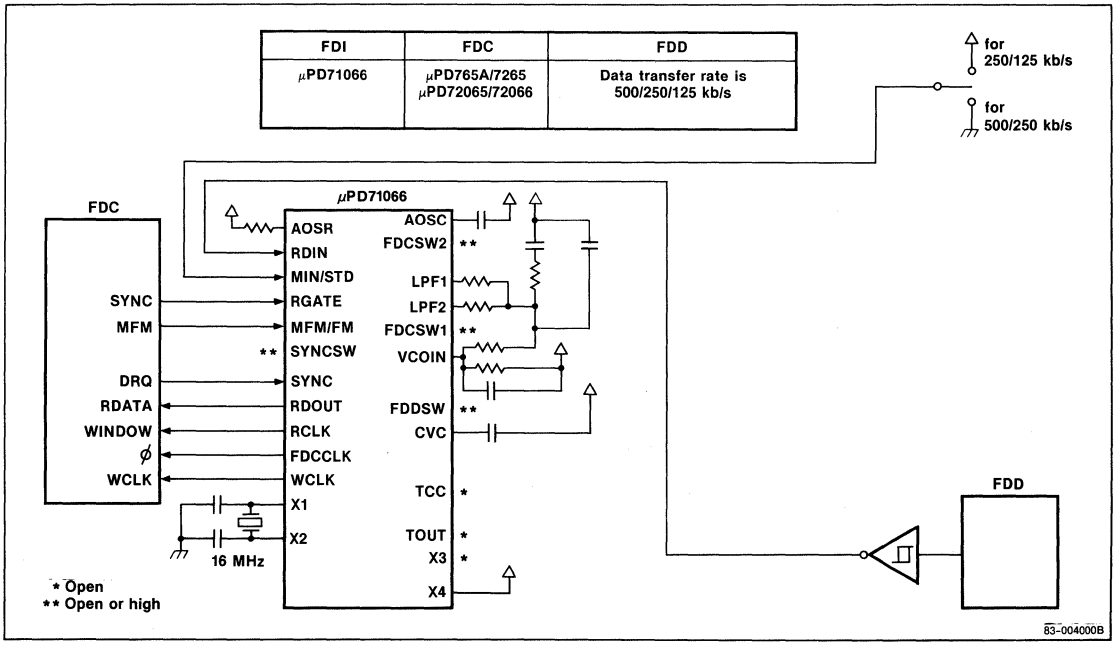

Figure 16. System Example 8: μPD71066 FDI and μPD765A FDC

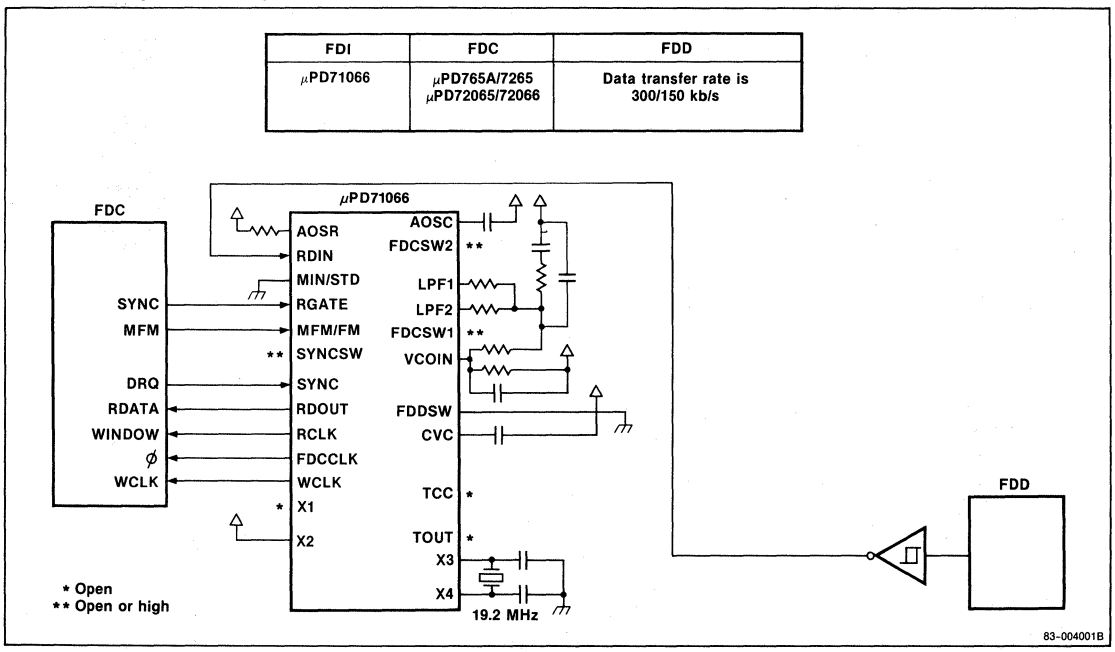

Figure 17. System Example 9: μPD71066 FDI and μPD765A FDC

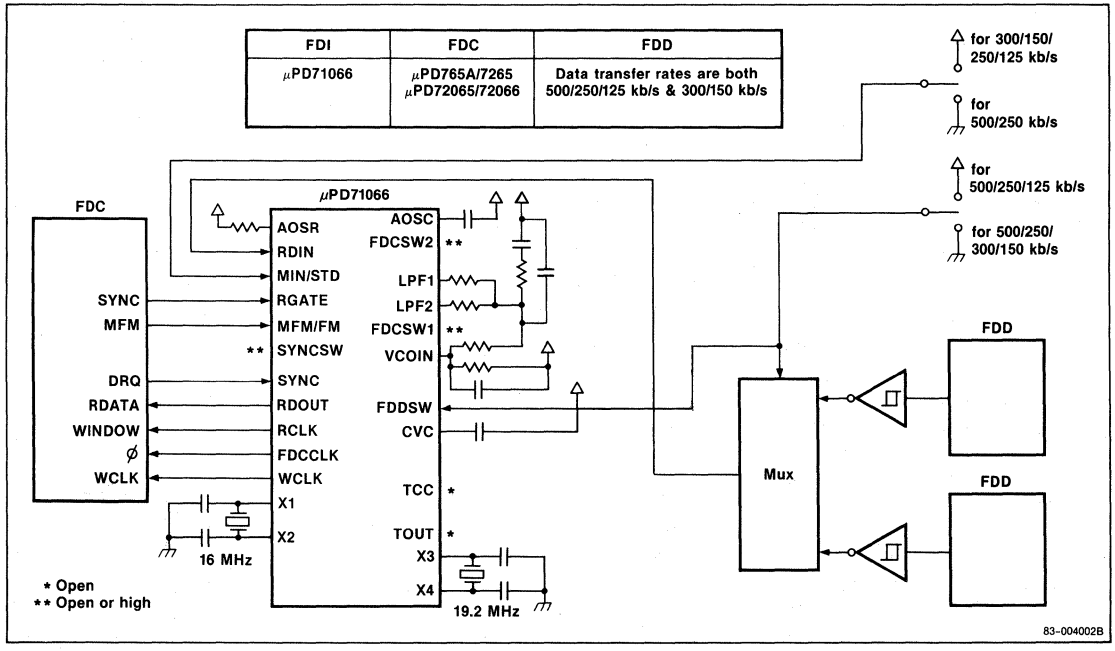

Figure 18. System Example 10: μPD71066 FDI and μPD7260 FDC

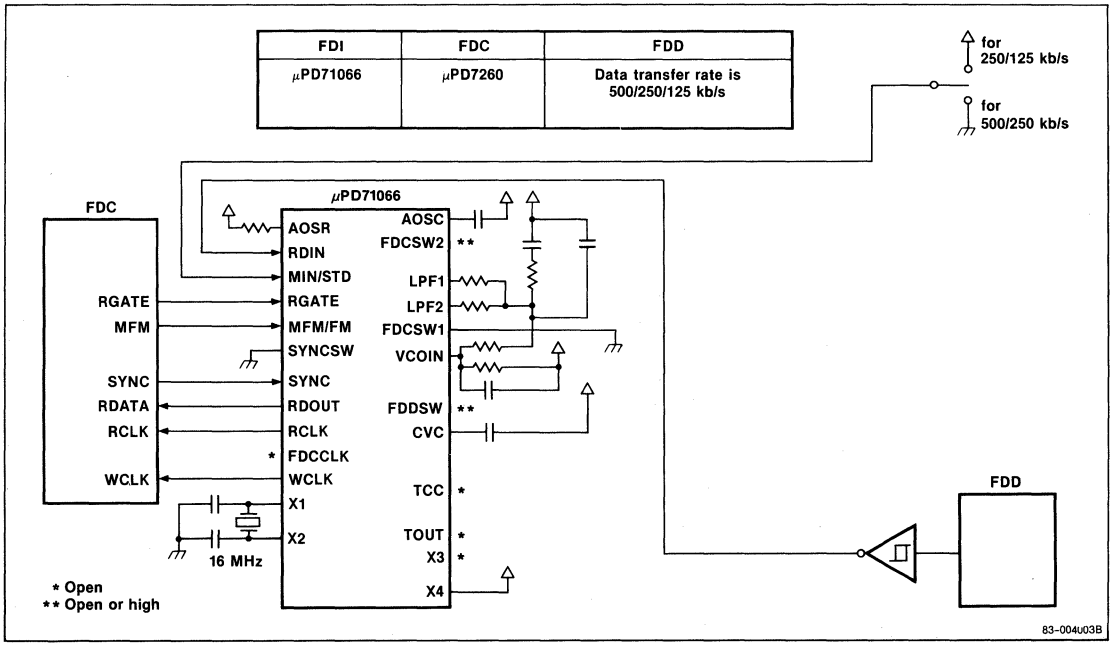

Figure 19. System Example 11: μPD71066 FDI and μPD7260 FDC

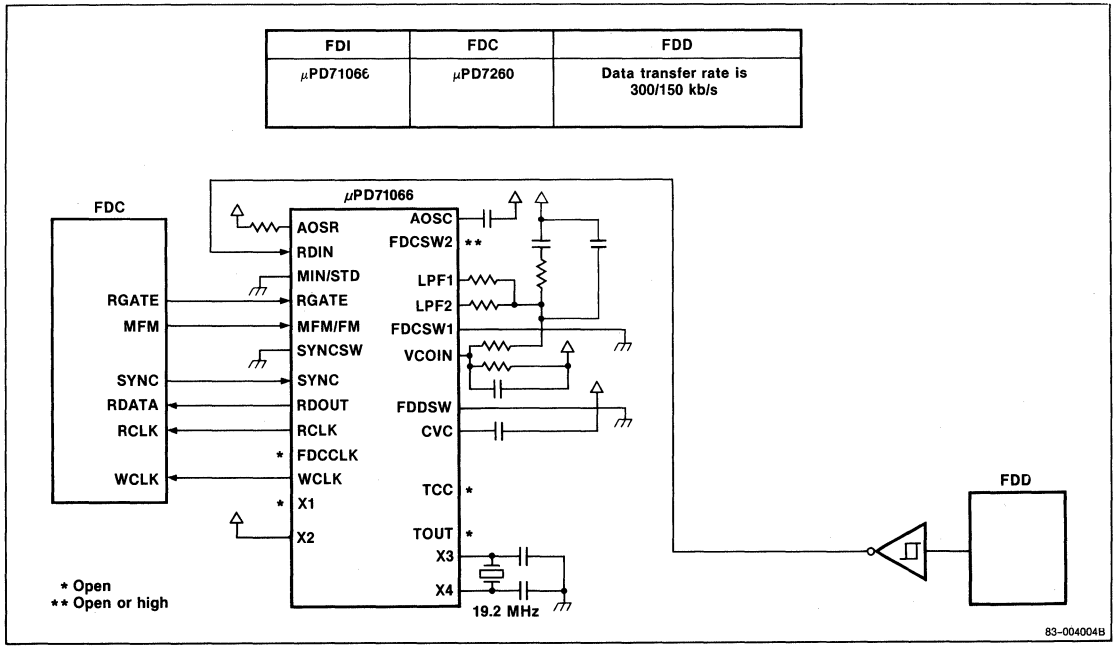

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Figure 20. System Example 12: μPD71066 FDI and μPD7260 FDC

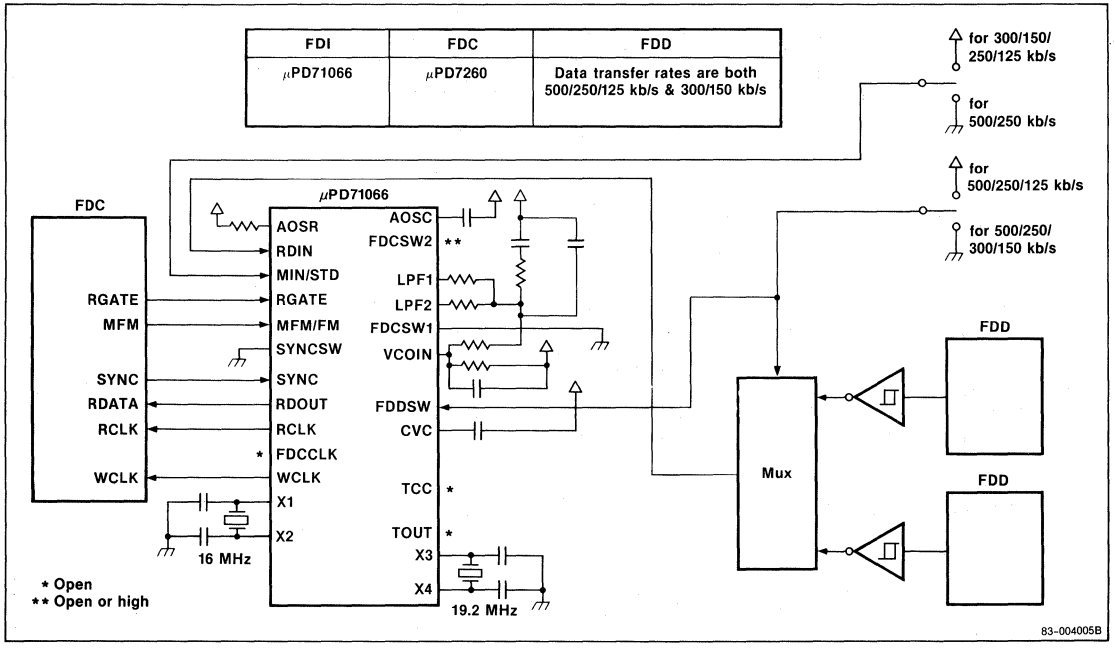


Figure 21. System Example 13: μPD71066 FDI and FD179X FDC

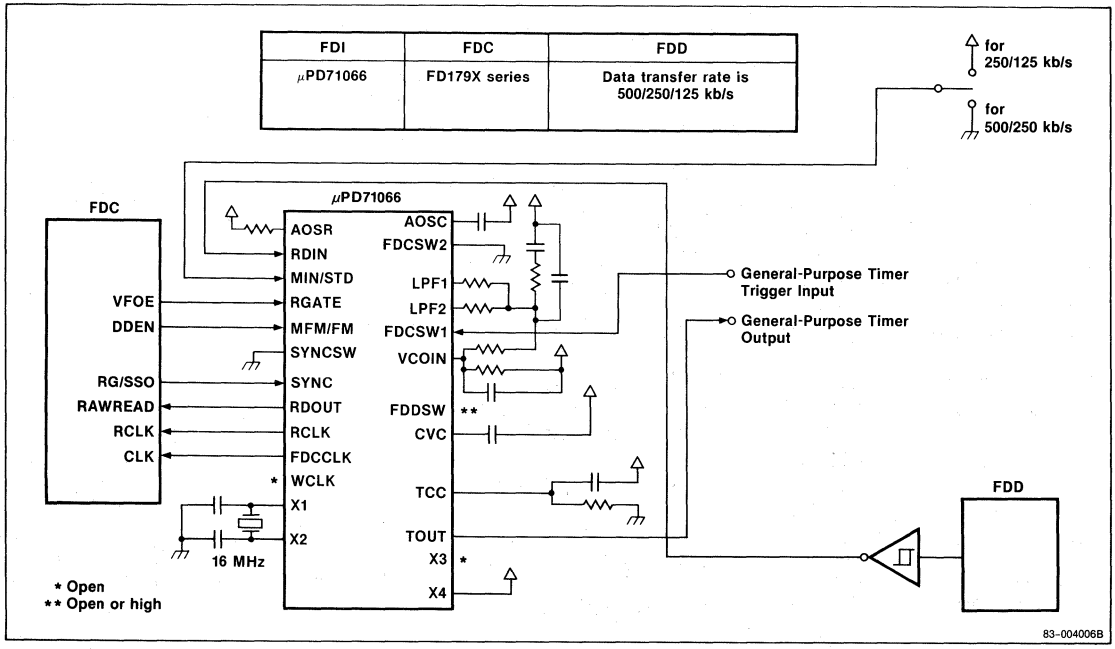


Figure 22. System Example 14: μPD71066 FDI and FD179X FDC

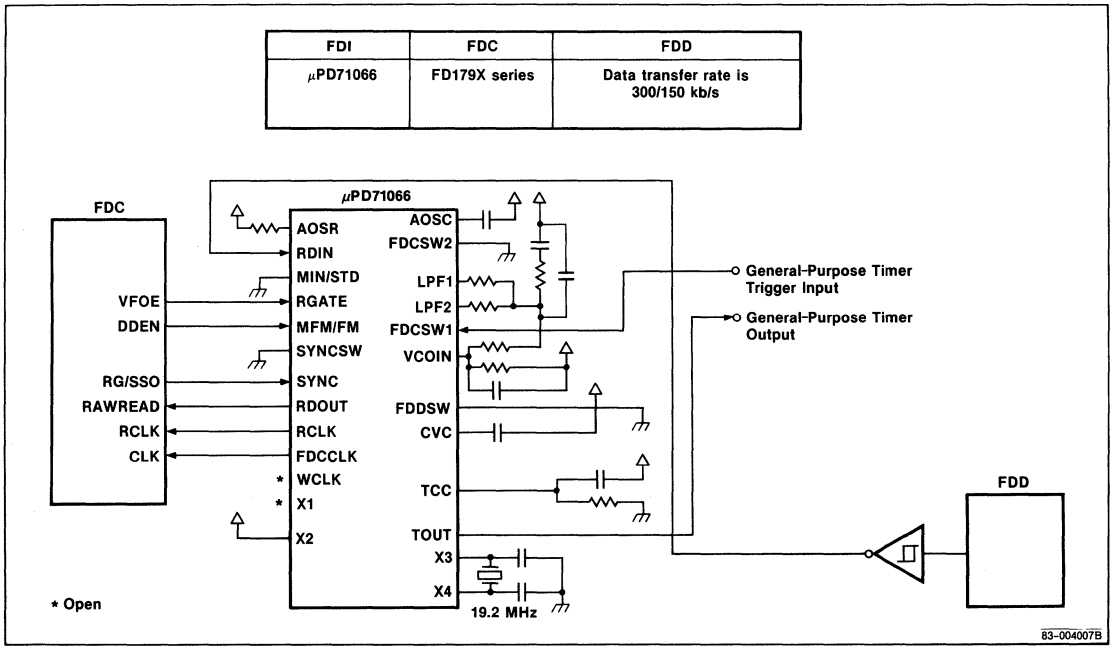
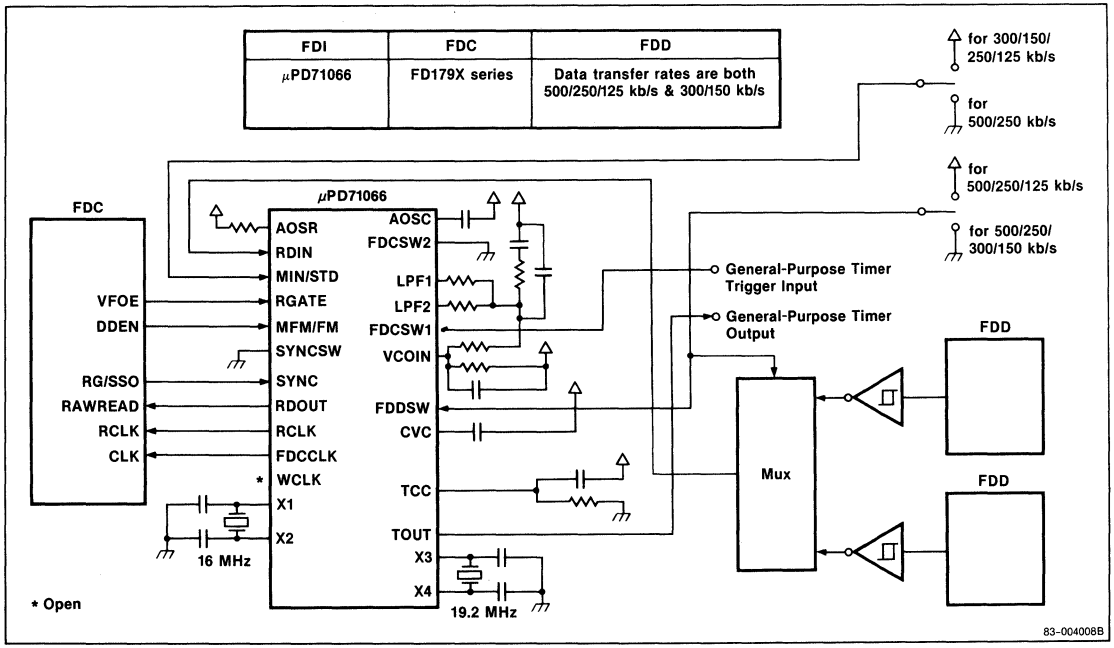


Figure 23. System Example 15: μPD71066 FDI and FD179X FDC



5

μPD72065/65B
CMOS Floppy-Disk Controller

Description

The μPD72065/65B CMOS Floppy-Disk Controller (FDC) is NEC's follow-on to the μPD765A/B. (μPD72065B is a functionally enhanced version of μPD72065.) The FDC is an LSI chip containing the circuitry and control functions for interfacing a processor to four floppy-disk drives (FDDs). It is capable of either IBM 3740 single-density format (FM) or IBM system 34 double-density format (MFM), including double-sided recording.

Control signals of the FDC simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy-disk interface.

Handshaking signals of the FDC make DMA operation easy to incorporate with the aid of an external DMA controller chip, such as the μPD8257. In DMA mode, the processor need only load the command into the FDC; all data transfers occur under control of the FDC and DMA controllers. In non-DMA mode, the FDC generates interrupts to the processor every time a data byte is to be transferred.

The FDC will execute the 19 commands listed below. Most of the commands require multiple 8-bit bytes to fully specify the operation that the processor wants the FDC to perform.

- Read Data
- Read ID
- Specify
- Read Diagnostics
- Scan Equal
- Scan High or Equal
- Scan Low or Equal
- Sense Drive Status
- Reset Standby
- Version
- Read Deleted Data
- Write Data
- Write ID
- Write Deleted Data
- Seek
- Recalibrate
- Sense Interrupt Status
- Set Standby
- Software Reset

Features

Internal address mark detection circuitry of the FDC simplifies the phase-locked loop and read electronics. Track stepping, head load time, and head unload time are user-programmable. Additional features are multitrack and multiside read and write commands plus single- and double-density capabilities.

- 100% 765A/B microcode compatibility
- Sony (ECMA) compatible recording format
- IBM-compatible format (single- and double-density)
- Multisector and multitrack transfer capability
- Interface processor with up to four floppy-disk or microfloppy-disk drives
- Data scan capability: single sector or entire cylinder, comparing host memory and disk data byte-by-byte
- Data transfers in DMA and non-DMA modes
- Parallel seek operations on up to four disk drives
- Compatible with μPD8080/85, μPD8086/88, and μPD780 (Z80®) microprocessors
- Single-phase clock (8 MHz maximum)
- +5-volt power supply
- CMOS technology

Ordering Information

Part Number	Package	Note
μPD72065C	40-pin plastic DIP (600 mil)	
65G	52-pin plastic miniflat (3.5-mm leads)	3
65GC	52-pin plastic miniflat (1.8-mm leads)	3
65L	44-pin PLCC	
μPD72065BC	40-pin plastic DIP (600 mil)	2
65BGC-3B6	52-pin plastic miniflat (1.8-mm leads)	2, 3
65BL	44-pin PLCC	2

Notes:

(1) The basic part numbers are μPD72065 and μPD72065B. Suffix codes are added to identify particular packages.

(2) The part is under development.

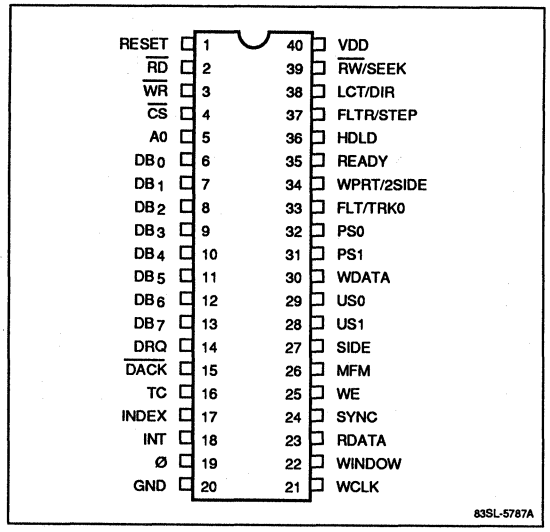
(3) Surface-mount conditions differ among the miniflat packages, as in reflow soldering. The NEC sales staff can provide details.

Z80 is a registered trademark of Zilog Corp.

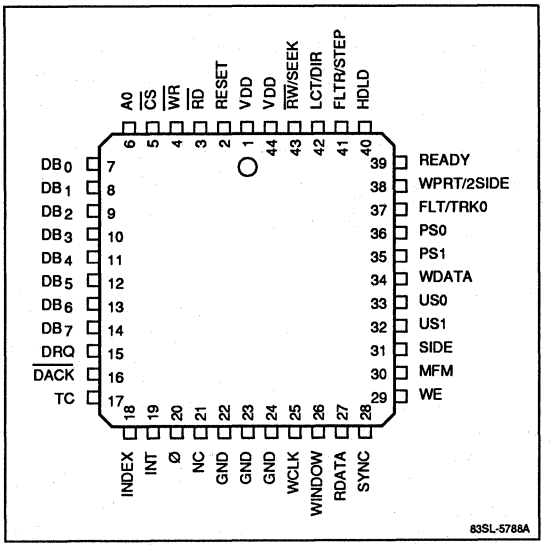
50073

Pin Configurations

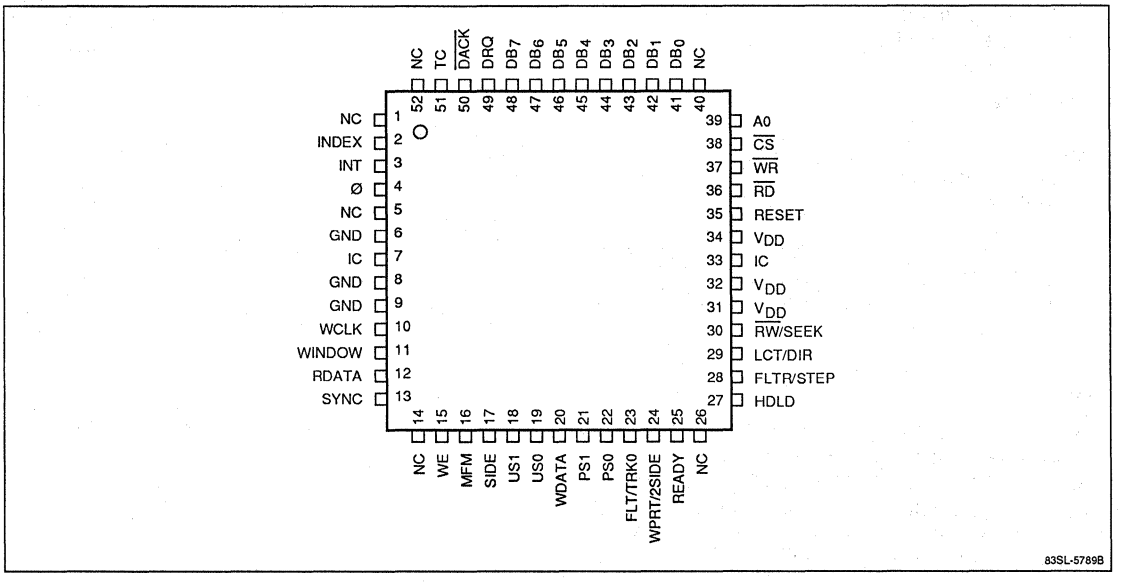
40-Pin Plastic DIP



44-Pin PLCC (Plastic Leaded Chip Carrier)



52-Pin Plastic Miniflat



Pin Identification

Symbol	I/O	Function
A0	In	Via the address bus, selects internal status register (0) or data register (1)
$\overline{CS}$	In	Chip select. Enables RD and WR signals.
$\overline{DACK}$	In	DMA acknowledge.
DB_0-DB_7	I/O	Bidirectional three-state data bus. At reset, bus goes to input mode.
DRQ	Out	DMA request. Request for data transfer in DMA mode.
FLT/TRK0	In	FLT (Fault). In read/write operation (RW/SEEK pin = 0), indicates whether FDD is in fault state. TRK0 (Track 0). In seek operation (RW/SEEK pin = 1), indicates whether FDD read/write head is positioned at cylinder 0.
FLTR/STEP	Out	FLTR (Fault read). In read/write operation (RW/SEEK pin = 0), releases FDD fault state. STEP. In seek operation (RW/SEEK pin = 1), outputs seek pulses.
HDLD	Out	Head load. Sets FDD read/write head to load state.
INDEX	In	Indicates that FDD read/write head is on the physical starting point of the track.
INT	Out	Interrupt request. Requests main system to deal with transfer of data or result of execution.
LCT/DIR	Out	LCT (Low current). In read/write operation (RW/SEEK pin = 0), indicates FDD read/write head is selecting a cylinder beyond the 42nd. DIR. In seek operation (RW/SEEK pin = 1), specifies direction, toward the outside (0) or the inside (1).
MFM	Out	Specifies function mode of VFO circuits: 0 = FM; 1 = MFM.
PS0, PS1	Out	Preshift signal requesting WDATA bit to shift in the opposite direction of expected peak shift to cancel out peak shift created when writing in MFM mode. PS0 PS1 FM MFM 0 0 No No shift 0 1 shift Delays WDATA bit 1 0 Advances WDATA bit 1 1
$\overline{RD}$	In	Control signal used by main system to read out data from FDC to data bus.
RDATA	In	Data (clock and data bits) read out from FDD. Unless both WINDOW and RDATA are input at read operation, FDC will enter deadlock state.
READY	In	Indicates FDD is in ready state.
RESET	In	Sets FDC to idle state as follows. Drive interface outputs except PS0, PS1, and WDATA (undefined) are set to low. In the main system, INT and DRQ are set to low and DB_0-DB_7 are set to input mode.
$\overline{RW}$/SEEK	Out	Selects read/write operation (0) or seek operation (1).
SIDE	Out	Selects head 0 (SIDE = 0) or head 1 (SIDE = 1) in a double-sided FDD.
SYNC	Out	VFO synchronize. Indicates FDC functional mode: read operation (1) or read operation inhibited (0).
TC	In	Terminal count. Request for data transfer termination.
US0, US1	Out	Unit select. One of four FDDs is selected by decoding US0 and US1.
WCLK	In	Write clock. Timing signal for data transfer in write operation; should also be input in read operation. Rising edges of WCLK and ϕ must be synchronized for μPD72065 but not for μPD72065B. WCLK = 16 ϕ cycles in FM mode and 8 ϕ cycles in MFM mode.
WDATA	Out	Write data (clock and data bits) to FDD.
WE	Out	Write enable. Requests write operation to FDD.
WINDOW	In	Data window signal generated by VFO circuit and used for sampling the clock and data bits of RDATA. Discrimination between clock and data bits is done in the FDC.
WPRT/2SIDE	In	WPRT (Write protected). In read/write operation (RW/SEEK pin = 0), indicates whether media is in write inhibit state. 2SIDE. In seek operation (RW/SEEK pin = 1), indicates whether a double-sided floppy disk is inserted.

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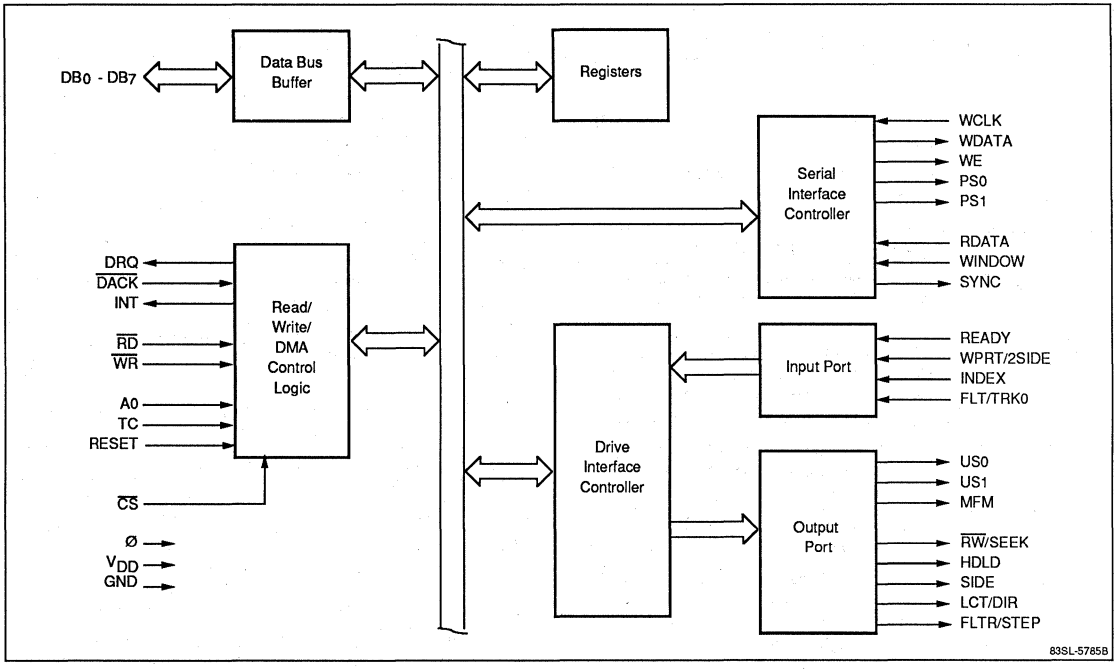
Pin Identification (cont)

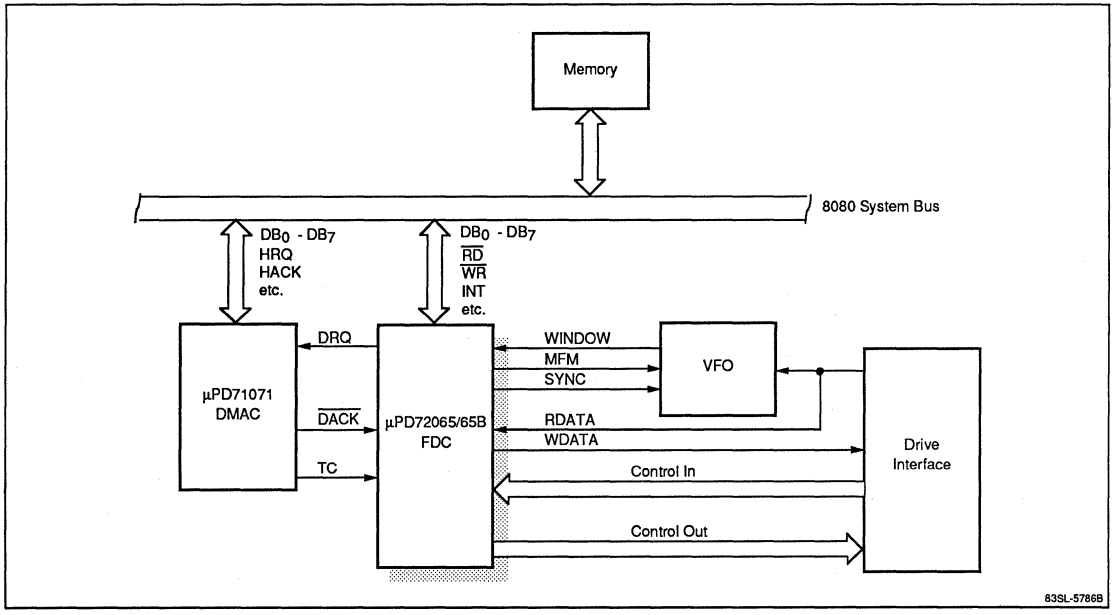
Symbol	I/O	Function
$\overline{WR}$	In	Control signal used by main system to write data on data bus to FDC.
ϕ	In	Single-phase clock: standard floppy, 8 MHz; minifloppy, 4 MHz.
GND		Ground
V_{DD}	In	+5-volt power supply
IC		Internal connection; must be left open.
NC		No connection.

Note: At reset, all output pins go to the low state except for pins PS0 and PS1, whose state is undefined.

μPD72065/65B Block Diagram



System Configuration



Absolute Maximum Ratings

T_A = +25°C

Voltage on any pin	−0.5 to +7 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Capacitance

T_A = +25°C; V_{DD} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Clock capacitance	C_ϕ		20	pF	Unmeasured pins returned to 0 V.
Input capacitance	C_{IN}		10	pF	
Output capacitance	C_{OUT}		20	pF	

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DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Input voltage, low	VI_{IL}	−0.5	0.8	V	
Input voltage, high	VI_{IH}	2.2	V_{DD} + 0.5	V	
Input voltage, low (φ, WCLK)	V_{IL}	−0.5	0.65	V	
Input voltage, high (φ, WCLK)	V_{IH}	2.2	V_{DD} + 0.5	V	
Output voltage, low	V_{OL}		0.45	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4	V_{DD}	V	I_{OH} = −200 μA
Input leakage current, low	I_{LIL}		−10	μA	V_{IN} = 0 V
Input leakage current, high	I_{LIH}		+10	μA	V_{IN} = V_{DD}
Output leakage current, low	I_{LOL}		−10	μA	V_{OUT} = +0.45 V
Output leakage current, high	I_{LOH}		+10	μA	V_{OUT} = V_{DD}
V_{DD} supply current	I_{DD}		10	mA	ϕ_{CY} = 125 ns
	I_{DD1}		500	μA	ϕ_{CY} = 125 ns
			250	μA	ϕ_{CY} = 250 ns
			100	μA	Clock stopped

AC Characteristics; Main System Side

T_A = −10 to +70°C; V_{DD} = +5 V ±10%; MFM data transfer = 500 kb/s (8 MHz), 250 kb/s (4 MHz)

			8-MHz Operation			4-MHz Operation				
Parameter	**Figure**	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Clock cycle	2	ϕ_{CY}	120	125	500	240	250	500	ns	
Clock width, high/low	2	ϕ_{θ}	40			40			ns	
Clock rise time	2	ϕ_R			20			20	ns	
Clock fall time	2	ϕ_F			20			20	ns	
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}$	3	t_{AR}	0			0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}$	3	t_{RA}	0			0			ns	
$\overline{RD}$ pulse width	3	t_{RR}	200			200			ns	
Data access time from $\overline{RD}$ ↓	3	t_{RD}			140			140	ns	
Data float delay time from $\overline{RD}$ ↑	3	t_{DF}	10		85	10		85	ns	
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}$	4	t_{AW}	0			0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time to $\overline{WR}$	4	t_{WA}	0			0			ns	
$\overline{WR}$ pulse width	4	t_{WW}	200			200			ns	
Data setup time to $\overline{WR}$	4	t_{DW}	100			100			ns	
Data hold time from $\overline{WR}$	4	t_{WD}	0			0			ns	
INT delay time from $\overline{RD}$ ↑	3	t_{RI}			400			400	ns	Data transfer in non-DMA mode
INT delay time from $\overline{WR}$ ↑	4	t_{WI}			400			400	ns	
DRQ cycle time	5	t_{MCY}	13			26			μs	8-MHz: ϕ_{CY} = 125 ns 4-MHz: ϕ_{CY} = 250 ns
$\overline{DACK}$ ↓ response time from DRQ ↑	5	t_{MA}	200			400			ns	
$\overline{RD}$ ↓ response time from DRQ ↑	5	t_{MR}	125			250			ns	
$\overline{WR}$ ↓ response time from DRQ ↑	5	t_{MW}	250			500			ns	
DRQ delay time from $\overline{DACK}$ ↓	5	t_{AM}			140			140	ns	
$\overline{DACK}$ pulse width	5	t_{AA}	2			2			ϕ_{CY}	
$\overline{WR}$/$\overline{RD}$ response time from DRQ ↑	5	t_{MRW}			12			12	μs	
TC pulse width	5	t_{TC}	60			60			ns	
RESET pulse width	6	t_{RST}	14			14			ϕ_{CY}	
Clock hold time at standby	7	t_{WC}	32			32			ϕ_{CY}	
Clock setup time at standby release	7	t_{CW}	16			16			ϕ_{CY}	
INT response time from DRQ ↓	8	t_{MI}	60		77	60		77	ϕ_{CY}	μPD72065B only
INT ↑ to $\overline{DACK}$ ineffective	8	t_{IA}			1			1	ϕ_{CY}	

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AC Characteristics; Drive Side

T_A = −10 to +70°C; V_{DD} = +5 V ±10%; MFM data transfer = 500 kb/s (8 MHz), 250 kb/s (4 MHz)

			8-MHz Operation			4-MHz Operation				
Parameter	**Figure**	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
WCLK cycle time	9	t_{CY}		16			16		ϕ_{CY}	MFM = 0
				8			8		ϕ_{CY}	MFM = 1
WCLK width, high	9	t_ϕ	80	250	350	160	500	700	ns	8-MHz: ϕ_{CY} = 125 ns 4-MHz: ϕ_{CY} = 250 ns
WCLK, RDATA, WINDOW rise time	9	t_R			20			20	ns	
WCLK, RDATA, WINDOW fall time	9	t_F			20			20	ns	
PS0, PS1 delay time from WCLK	9	t_{CP}	10		80	10			ns	
WDATA delay time from WCLK	9	t_{CD}	10		80	10			ns	
WE delay time from WCLK	9	t_{CWE}	10		80	10			ns	
WDATA width	9	t_{WDD}	t_ϕ − 50			t_ϕ − 50			ns	
RDATA active time high	10	t_{RDD}	40			40			ns	
WINDOW cycle time	10	t_{WCY}		2			4		μs	MFM = 0
				1			2		μs	MFM = 1
WINDOW setup time to RDATA	10	t_{WRD}	15			15			ns	
WINDOW hold time from RDATA	10	t_{RDW}	15			15			ns	
US0, US1 setup time to SEEK	11	t_{US}	12			24			μs	8-MHz: ϕ_{CY} = 125 ns 4-MHz: ϕ_{CY} = 250 ns (Note 1)
SEEK setup time to DIR	11	t_{SD}	7			14			μs	
DIR setup time to STEP	11	t_{DST}	1			2			μs	
US0, US1 hold time from STEP	11	t_{STU}	5			10			μs	
STEP active time high	11	t_{STP}	6	7	8	12	14	16	μs	
US0, US1 hold time after SEEK	11	t_{SU}	15			30			μs	
SEEK hold time from DIR	11	t_{DS}	30			60			μs	
DIR hold time after STEP	11	t_{STD}	24			48			μs	
STEP cycle time	11	t_{SC}	33			66			μs	
FLTR active time high	11	t_{FR}	8		10	16		20	μs	
INDEX level high	12	t_{IDK}	4			4			ϕ_{CY}	

Notes:

(1) For the parameters on figures 11 and 12, the minimum values are 50 ns less than the values (μs) specified in the table. For example, 10 μs is actually 9.950 μs.

(2) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

Figure 1. Voltage Thresholds for Timing Measurements

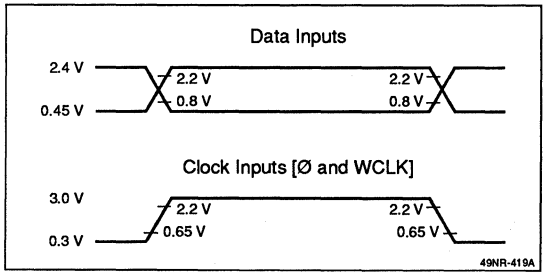

Figure 2. Clock Waveform

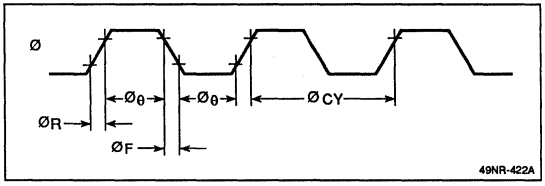

Figure 3. Read Operation

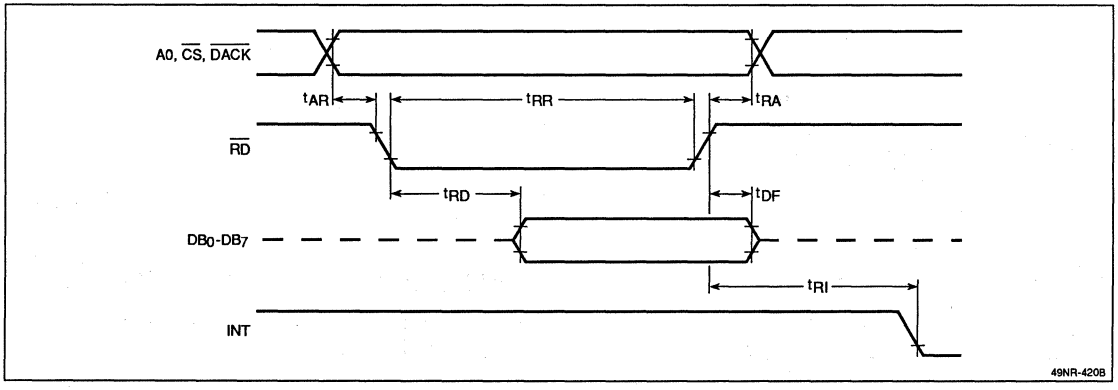

Figure 4. Write Operation

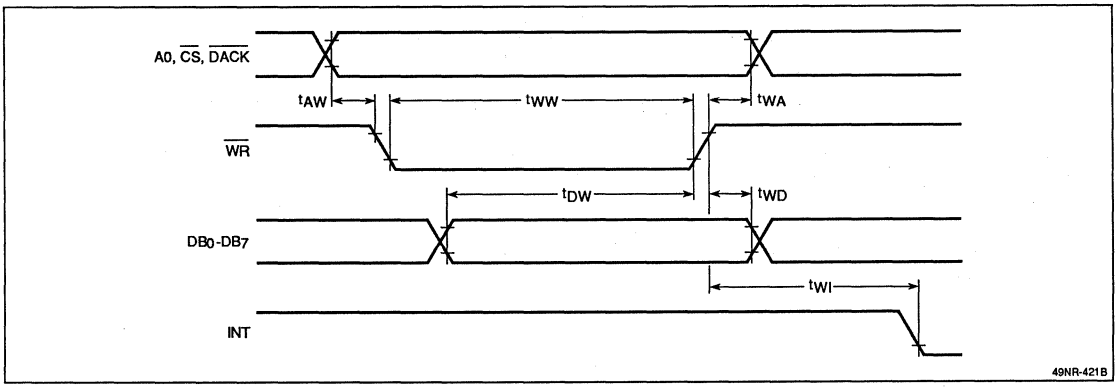

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Figure 5. DMA Operation

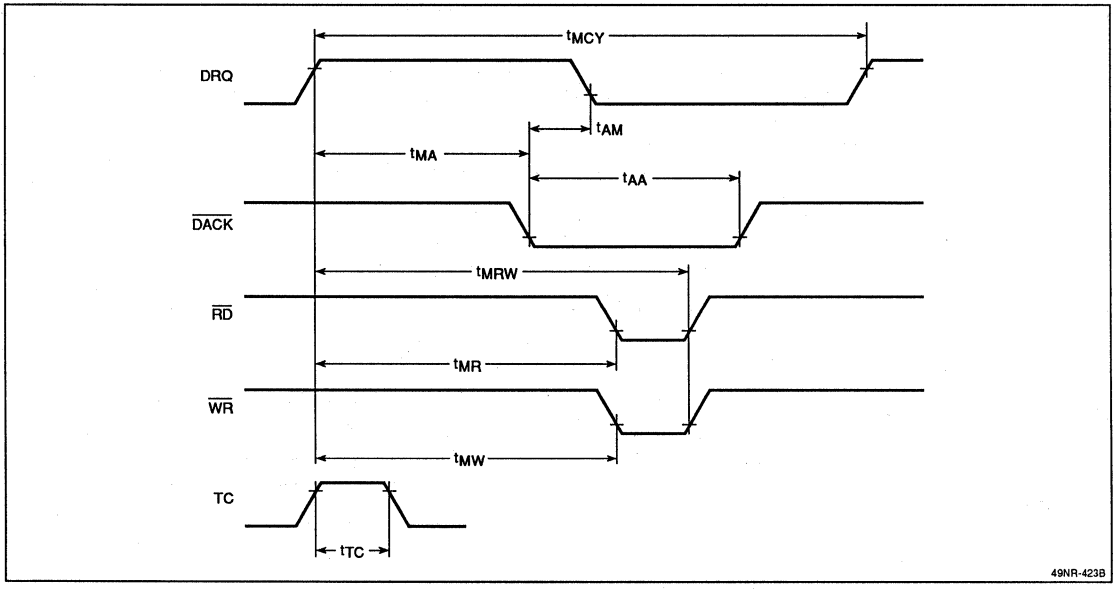

Figure 6. RESET Waveform

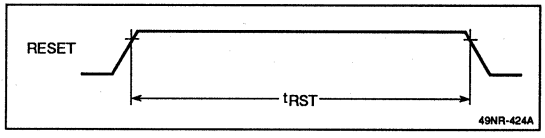

Figure 7. Standby Operation

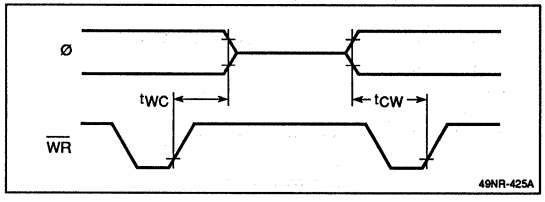

Figure 8. Overrun Operation (μPD72065B)

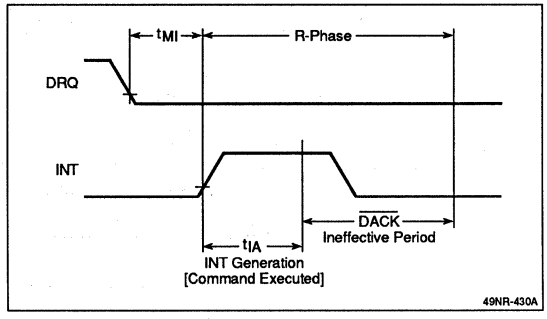

Figure 9. FDD Write Operation

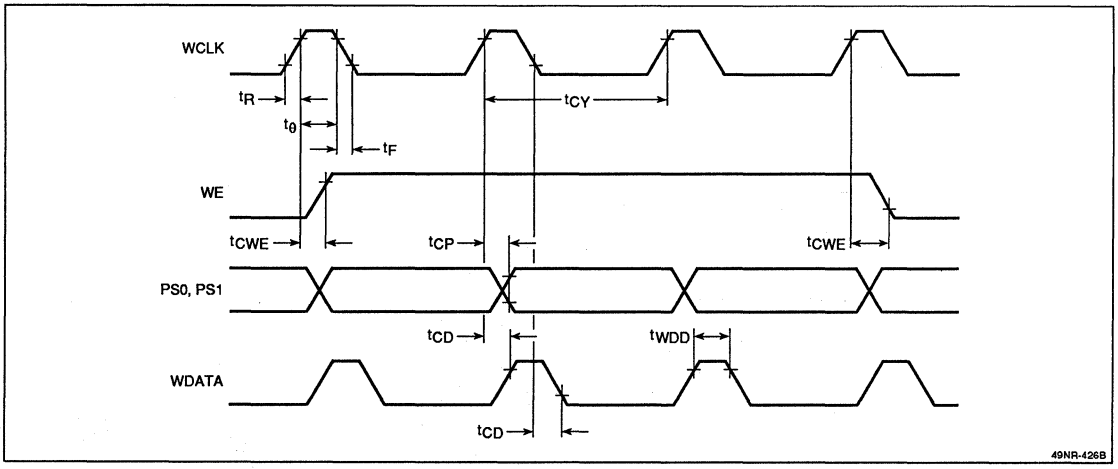

Figure 10. FDD Read Operation

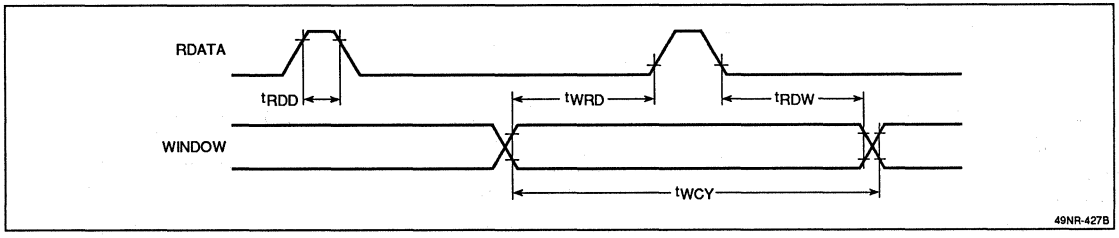

Figure 11. Seek Operation

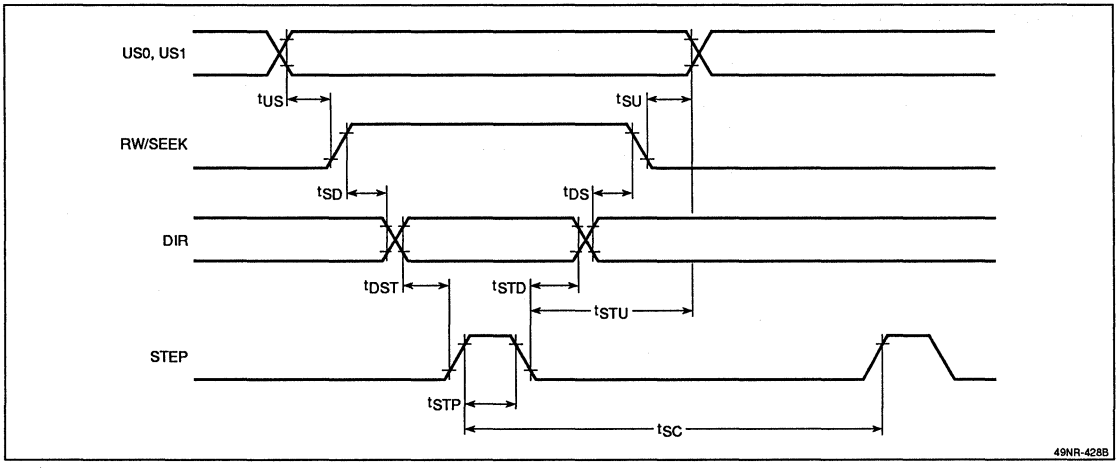

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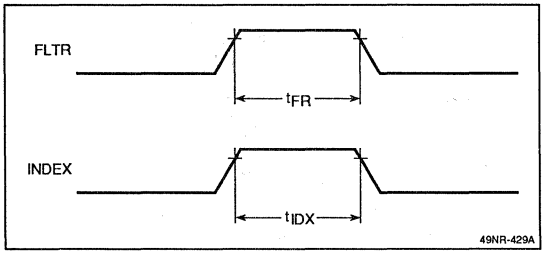
Figure 12. FLTR and INDEX Waveforms



COMPARISON, μPD72065 VS μPD72065B

The μPD72065B is a functionally enhanced version of the μPD72065. Differences are explained below.

Overrun Bit (OR)

In the μPD72065, when executing a read- or write-type command (except READ ID and SCAN types), the result status OR bit is not set if there is an overrun on the final byte of a sector. An improvement in the μPD72065B allows it to set the OR bit in any situation.

DRQ Reset

When an overrun occurs, the μPD72065 needs the $\overline{DACK}$ input to reset DRQ. If $\overline{DACK}$ is not available, an external DMA controller continues operating even after the FDC enters the R-phase, and stored result status may be transferred accidentally as ordinary data.

On the other hand, the μPD72065B resets DRQ automatically just before the R-phase entry and independent of the $\overline{DACK}$ input. See AC Characteristics for DRQ reset timing.

Clock Synchronization

The μPD72065 does not require synchronization between the ϕ clock and WCLK inputs.

VERSION Command

The VERSION command distinguishes the μPD72065B from other devices. The ST0 response to the command is:

Part No.	ST0 Value
μPD72065	80H
μPD72065B	90H

COMPARISON, μPD72065/65B VS μPD765A/B

Table 1 shows differences in the parameters and features of the FDCs.

Table 1. μPD72065/65B and μPD765A/B

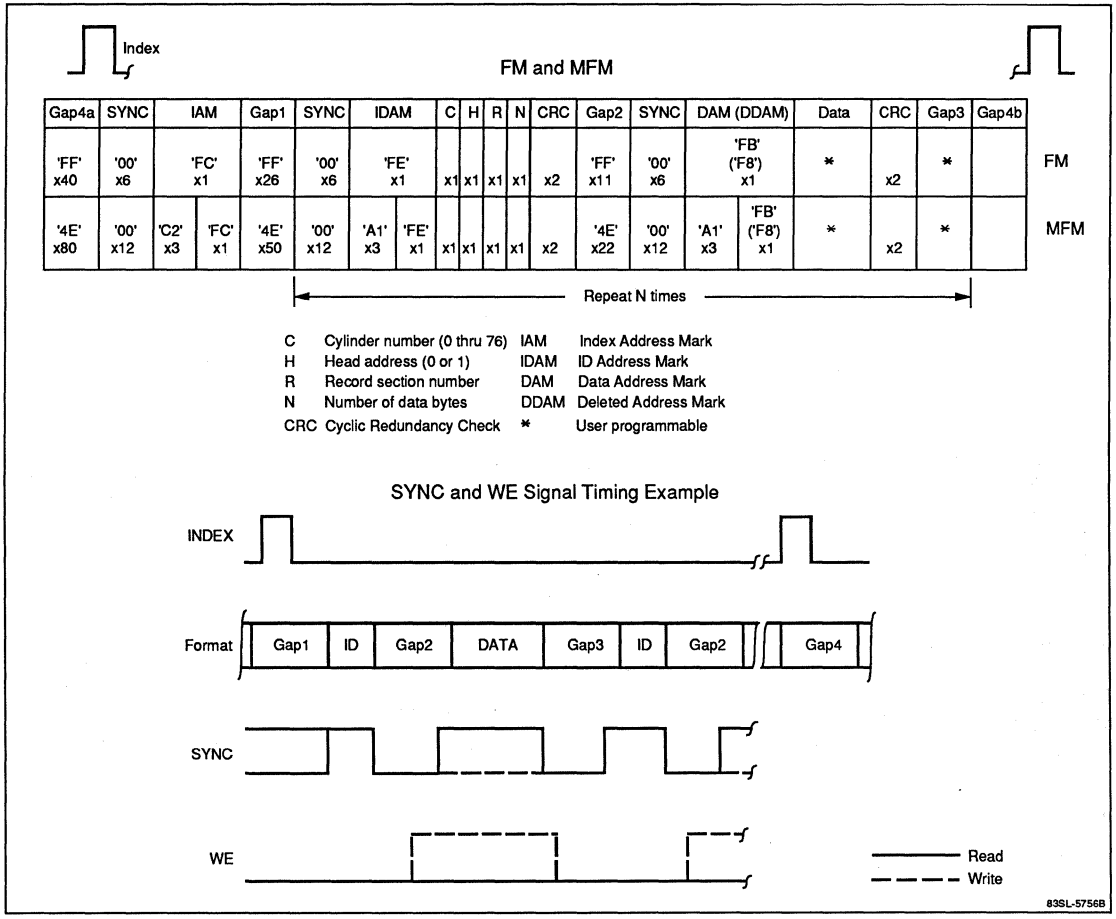
Parameter	μPD72065/65B	μPD765A/B
Track format	IBM	IBM
Tracks to be recalibrated	255	77
Skipping time after Index pulse detection	0.2 ms (4 MHz)	1.2 ms (4 MHz)
DRQ ↑ to RD ↓ response time		
ϕ_{CY} = 125 ns	1 x ϕ_{CY}	0.8 μs
ϕ_{CY} = 250 ns	1 x ϕ_{CY}	1.6 μs
FDD response latency after Unit select signal		
ϕ_{CY} = 125 ns	2.5 μs	0.5 μs
ϕ_{CY} = 250 ns	5.0 μs	1.0 μs
Multitrack write by tunnel erase head	Yes	No
Standby function (Standby command)	Yes	No
SOFTWARE RESET command	Yes	No

ϕ_{CY} = clock cycle time

DATA FORMAT

Figure 13 shows the data format for FM and MFM modes

Figure 13. Data Format and Timing.



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Description

The μPD72067 Floppy-Disk Controller (FDC) is a CMOS device that integrates onto a single chip the peripheral logic necessary for todays's high-performance, low-power designs. It maintains complete microcode compatibility with the NEC μPD765 and μPD72065 devices, long established as the industry standard for floppy-disk control.

The μPD72067 incorporates on-chip clock generation/switching, selectable write precompensation, and all the circuitry required for directly interfacing four floppy- disk drives.

An internal high-performance digital phase-locked loop (DPLL) enables reliable data separation at data transfer rates up to 500 kb/s.

Features

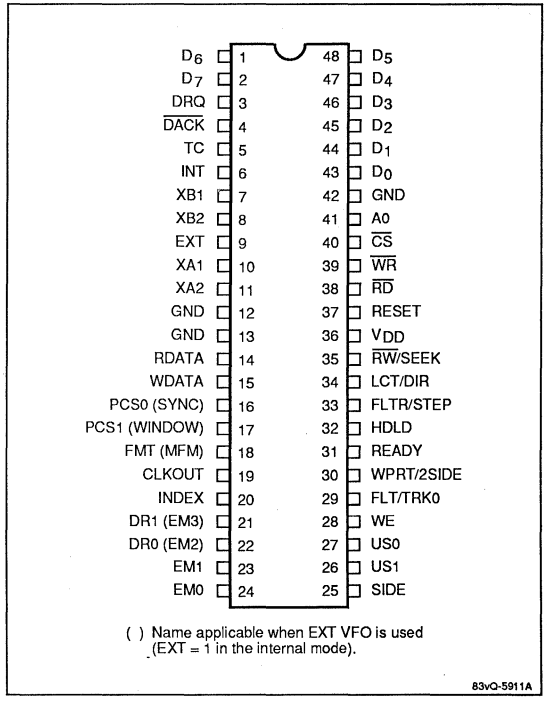
- Command compatible with μPD765A, 765A-2, 765B, 7265, 72065, 72065B, 72066
- IBM diskette compatible
  - — Single-sided, 128/256/512 bytes/sector
  - — Double-sided, 256 bytes/sector
  - — Double-sided, double-density, 256/1024 bytes/sector
- ECMA/ISO minifloppy-disk format compatible
  - — ECMA66 (ISO/TC 97/SC11 N419), single-sided, single-density, 256 bytes/sector
  - — ECMA70 (ISO/TC 97/SC11 N475), double-sided, double-density, 256 bytes/sector
- Data transfer rates: 125, 150, 250, 300, 500 kb/s
- Standby function
- On-chip peripheral circuits
  - — VFO (DPLL) for window signal generation
  - — Write precompensation
  - — System clock generator
  - — Write clock generator
- External VFO (such as μPD71065/71066) can be connected
- Spindle motor control
- FM, MFM control (specified in each command)
- Variable record length: 128, 256, 512, 1024, 2048, 4096, or 8192 bytes/sector
- Multisector and multitrack functions
- Controls up to four FDDs
- Mixed floppy-disks: single- and double-sided, single- and double-density
- Simultaneous seek operation on four FDDs
- Intermediate or incomplete sector read/write can be specified (FM, 128 bytes/sector)
- Internal CRC generation and check ($x^{16} + x^{12} + x^5 + 1$)
- Stepping speed programmable
- Head load and unlead times programmable
- Data scan function: detection of sector satisfying equal-to, greater-than, or less-than condition with main memory data)
- DMA or non-DMA (interrupt) data transfer
- CMOS
- Single +5-volt power supply

Ordering Information

Part Number	Package
μPD72067C	48-pin plastic DIP (600 mil)
μPD72067GC-3B6	52-pin plastic miniflat
μPD72067L	52-pin PLCC (plastic leaded chip carrier)

Pin Configurations

48-Pin Plastic DIP (600 mil)



( ) Name applicable when EXT VFO is used (EXT = 1 in the internal mode).

83vQ-5911A

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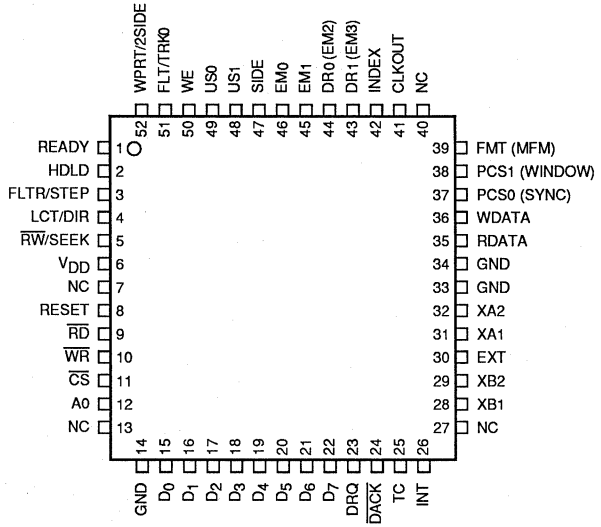
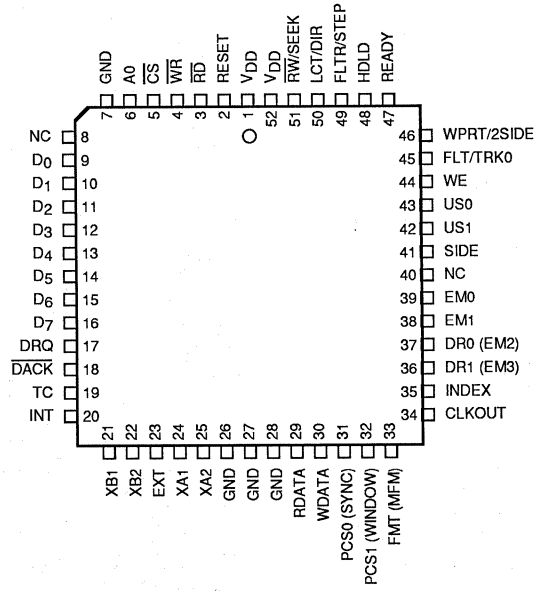
52-Pin Plastic Miniflat



( ) Name applicable when EXT VFO is used
(EXT = 1 in the internal mode)

83vQ-5918B

52-Pin PLCC



( ) Name applicable when EXT VFO is used
(EXT = 1 in the internal mode)

83vQ-5917B

Pin Identification

Symbol	I/O	Signal Function
A0	In	Address 0. Selects μPD72067 registers via address bus. A0 Registers 0 Status or auxiliary command 1 Data
CLKOUT	Out	When EXT = 1, supplies clock required by a μPD71065/71066 used as an external VFO. DR1 CLKOUT 0 16 MHz 1 19.2 MHz Note: CLKOUT goes low when EXT = 0.
$\overline{CS}$	In	Chip Select. Validates $\overline{RD}$ and $\overline{WR}$ signals.
D_0-D_7	I/O	Bidirectional, three-state data bus.
$\overline{DACK}$	In	DMA Acknowledge. Enables DMA cycle.
DR0, DR1	In	Data Rate. Sets data transfer rate in external mode.
(EM2, EM3)	Out	Enable Motor. Controls spindle motor in internal mode.
DRQ	Out	DMA Request. Requests data transfer in DMA mode.
EM0, EM1	Out	Enable Motor. Controls spindle motor.
EXT	In	External VFO. Selects VFO in internal mode. EXT VFO 0 Internal 1 External In external mode, the input to EXT is not significant.
FLTR/STEP	Out	FLTR (Fault Reset). When $\overline{RW}$/SEEK is set to 0, FLTR releases the drive fault state. STEP. When $\overline{RW}$/SEEK is set to 1, STEP generates seek pulses
FLT/TRK0	In	FLT (Fault). When $\overline{RW}$/SEEK is set to 0, FLT indicates whether the drive is in fault state or not. RK0 (Track 0). When $\overline{RW}$/SEEK is set to 1, TRK0 indicates whether the read/write head is positioned at cylinder 0 or not.
FMT	In	Format. Selects format in external mode. FMT Format 0 IBM 1 ECMA
(MFM)	Out	MFM Mode. In internal mode, format is specified by the SELECT FORMAT command. The MFM output signal specifies the VFO circuit operation mode. MFM Mode 0 FM 1 MFM
HDLD	Out	Head Load. Causes read/write head to contact the diskette.
INDEX	In	Indicates read/write head is positioned at the physical starting point of the track on the medium.
INT	Out	Interrupt Request. Requests main system to process the transfer data and execution results.
LCT/DIR	Out	LCT (Low Current). When $\overline{RW}$/SEEK signal is set to 0, LCT indicates the read/write head selects the 43rd or later cylinder. DIR (Direction). When $\overline{RW}$/SEEK signal is set to 1, DIR specifies the seek direction. DIR Direction 0 Outer 1 Inner
PCS0	In	Precompensation. In external mode, PCS0 determines the amount of precompensation.
(SYNC)	Out	VFO Synchronize. In internal mode, SYNC indicates the μPD72067 operation mode. SYNC Mode 0 Read operation is inhibited 1 Read operation is being performed This pin should be pulled high or low by resistors if external mode is not used.
PCS1	In	Precompensation. In external mode, PCS1 (with PCS0) determines the amount of precompensation.
(WINDOW)	In	Data Window. In internal mode, the WINDOW signal generated by the VFO circuit samples the $\overline{RDATA}$ bits. The μPD72067 determines whether a bit is clock or data. This pin should be tied directly high or low if external mode is not used.
$\overline{RD}$	In	Read. Causes the main system to read data from the μPD72067 to the data bus.
RDATA	In	Read data (consisting of clock and data bits) from the drive. If both WINDOW and RDATA are not input at the read state, a deadlock state is entered.
READY	In	Indicates the drive is in a ready state.
RESET	In	Places μPD72067 in idle state. • Outputs are low except WDATA is undefined. • In main system, INT and DRQ are low. • D_0-D_7 are in the input state.
$\overline{RW}$/SEEK	Out	Specifies whether certain FDD interface signals are used for read/write or seek. RW/SEEK Signal function 0 Read/write 1 Seek
SIDE	Out	Selects head 0 or head 1 of screen-type drive. SIDE Selected 0 Head 0 1 Head 1
TC	In	Terminal Count. Indicates data transfer termination.

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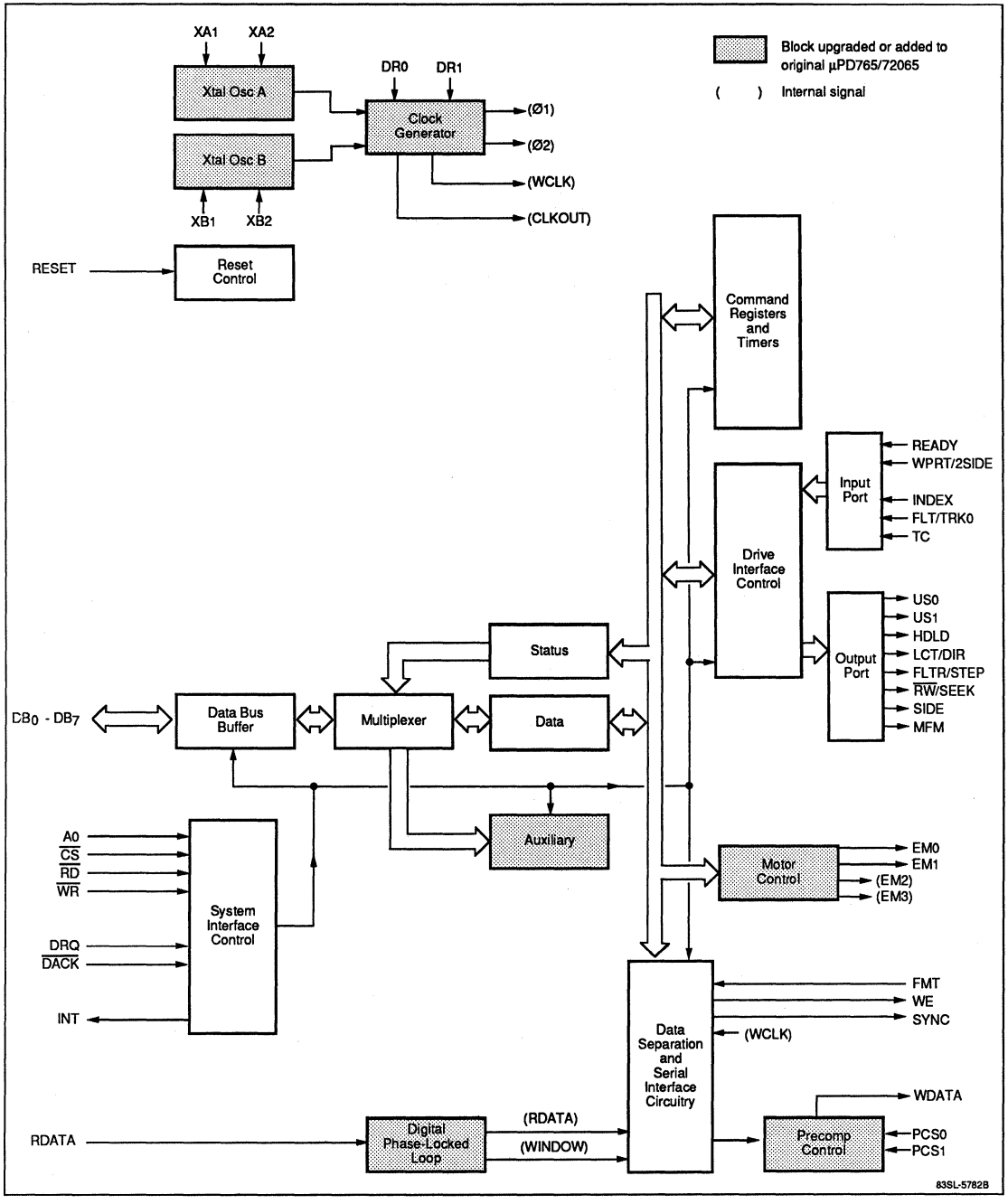
Pin Identification (cont)

Symbol	I/O	Signal Function
US0, US1	Out	Unit Select. One of four FDDs is selected by decoding US0 and US1.
WDATA	Out	Write data (clock and data bits) to FDD.
WE	Out	Write Enable. Requests FDD to write data.
WPRT/2SIDE	In	WPRT (Write Protected). When $\overline{RW}$/SEEK is set to 0, WPRT indicates whether the medium is write-protected. 2SIDE (Two Side). When $\overline{RW}$/SEEK is set to 1, 2SIDE indicates whether the medium is double-sided.
$\overline{WR}$	In	Write. Control signal that allows the main system to read data from the μPD72067 to the data bus.
XA1, XA2	In	Crystal A. To use internal VFO (EXT = 0), connect a 32-MHz quartz crystal resonator to XA1 and XA2. As an alternative, connect a 32-MHz external clock to XA1 and leave XA2 open. To use external VFO (EXT = 1), connect a 16-MHz quartz crystal resonator to XA1 and XA2. As an alternative, connect a 16-MHz external clock to XA1 and leave XA2 open.
XB1, XB2	In	Crystal B. To use the 300-kb/s data transfer rate, connect a 19.2-MHz quartz crystal resonator to XB1 and XB2. As an alternative, connect a 19.2-MHz external clock to XB1 and leave XB2 open.
NC		No Connection
GND		Ground
V_{DD}	In	+5-volt power supply

Note:

The pin symbol in parentheses applies when external VFO is used.

μPD72067 Block Diagram



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Absolute Maximum Ratings

T_A = +25°C

Voltage on any pin	−0.5 to +7 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to 150°C

Capacitance

T_A = +25°C; V_{DD} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Clock capacitance	C_ϕ		20	pF	Unmeasured pins returned to 0 V.
Input capacitance	C_{IN}		10	pF	
Output capacitance	C_{OUT}		20	pF	

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL}	−0.5	0.8	V	
High-level input voltage	V_{IH}	2.2	V_{DD} + 0.5	V	
Low-level output voltage	V_{OL}		0.45	V	I_{OL} = 2.0 mA
High-level output voltage	V_{OH}	0.7 V_{DD}	V_{DD}	V	I_{OH} = −200 μA
Low-level input leakage current	I_{LIL}		−10	μA	V_{IN} = 0 V
High-level input leakage current	I_{LIH}		+10	μA	V_{IN} = V_{DD}
Low-level output leakage current	I_{LOL}		−10	μA	V_{OUT} = +0.45 V
High-level output leakage current	I_{LOH}		+10	μA	V_{OUT} = V_{DD}
V_{DD} supply current	I_{DD}		60	mA	Note 1
Standby current	I_{DD1}		100	μA	
Oscillator stabilization time	t_{KS}		10	ms	

Notes:

(1) When a 32-MHz crystal is connected to XA1-XA2 or a 19.2-MHz crystal is connected to XB1-XB2.

AC Characteristics 1; Standard Floppy-Disk Control

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 500 kb/s

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	Note 1
DRQ cycle time	4	t_{MCY}	13			μs	DR1 = 0, DR0 = 1
$\overline{DACK}$ ↓ response time from DRQ ↑	4	t_{MA}	200			ns	
DRQ delay time from $\overline{DACK}$ ↓	4	t_{AM}			140	ns	
$\overline{DACK}$ pulse width	4	t_{AA}	8			ϕ_{CY}	Note 5
$\overline{RD}$ ↓ response time from DRQ ↑	4	t_{MR}	125			ns	DR1 = 0, DR0 = 1
$\overline{WR}$ ↓ response time from DRQ ↑	4	t_{MW}	250			ns	
$\overline{WR}$/$\overline{RD}$ response time from DRQ ↑	4	t_{MRW}			12	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	60			ϕ_{CY}	Note 5

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AC Characteristics 1; Standard Floppy-Disk Control (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	6	t_{RDD}	40			ns	
WINDOW cycle time (Note 2)	6	t_{WCY}		2		μs	MFM = 0
				1		μs	MFM = 1
WINDOW setup time to RDATA (Note 2)	6	t_{WRD}	15			ns	
WINDOW hold time from RDATA (Note 2)	6	t_{RDW}	15			ns	
US0, US1 setup time to SEEK	7	t_{US}	12			μs	Note 3
SEEK setup time to DIR	7	t_{SD}	7			μs	
DIR setup time to STEP	7	t_{DST}	1			μs	
US0, US1 hold time from STEP	7	t_{STU}	5			μs	
STEP high-level width	7	t_{STP}	6	7	8	μs	
US0, US1 hold time from SEEK (Note 4)	7	t_{SU}	15			μs	
SEEK hold time from DIR	7	t_{DS}	30			μs	
DIR hold time from STEP	7	t_{STD}	24			μs	
STEP cycle time	7	t_{SC}	33			μs	
FLTR high-level width	8	t_{FR}	8		10	μs	
INDEX high-level width	8	t_{IDX}	16			ϕ_{CY}	Note 5

Notes:

(1) For data transfer in non-DMA mode.

(2) When external VFO is used.

(3) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(4) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(5) The time ϕ_{CY} is a multiple of the period of a quartz crystal resonator connected to pins XA1-XA2 or an external clock connected to pin XA1. The multiple is four (EXT = 0) or two (EXT = 1).

(6) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 2; Minifloppy-Disk Control

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 250 kb/s

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	Note 1
DRQ cycle time	4	t_{MCY}	26			μs	DR1 = 0, DR0 = 0
$\overline{DACK}$ ↓ response time from DRQ ↑	4	t_{MA}	400			ns	
DRQ delay time from $\overline{DACK}$ ↓	4	t_{AM}			140	ns	
$\overline{DACK}$ pulse width	4	t_{AA}	8			ϕ_{CY}	Note 5
$\overline{RD}$ ↓ response time from DRQ ↑	4	t_{MR}	250			ns	DR1 = 0, DR0 = 0
$\overline{WR}$ ↓ response time from DRQ ↑	4	t_{MW}	500			ns	
$\overline{WR}$/$\overline{RD}$ response time from DRQ ↑	4	t_{MRW}			24	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	60			ϕ_{CY}	Note 5

5

AC Characteristics 2; Minifloppy-Disk Control (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	6	t_{RDD}	40			ns	
WINDOW cycle time (Note 2)	6	t_{WCY}		4		μs	MFM = 0
				2		μs	MFM = 1
WINDOW setup time to RDATA (Note 2)	6	t_{WRD}	15			ns	
WINDOW hold time from RDATA (Note 2)	6	t_{RDW}	15			ns	
US0, US1 setup time to SEEK	7	t_{US}	24			μs	Note 3
SEEK setup time to DIR	7	t_{SD}	14			μs	
DIR setup time to STEP	7	t_{DST}	2			μs	
US0, US1 hold time from STEP	7	t_{STU}	10			μs	
STEP high-level width	7	t_{STP}	12	14	16	μs	
US0, US1 hold time from SEEK (Note 4)	7	t_{SU}	30			μs	
DIR hold time from STEP	7	t_{STD}	48			μs	
SEEK hold time from DIR	7	t_{DS}	60			μs	
STEP cycle time	7	t_{SC}	66			μs	
FLTR high-level width	8	t_{FR}	16		20	μs	
INDEX high-level width	8	t_{IDX}	16			ϕ_{CY}	Note 5

Notes:

(1) For data transfer in non-DMA mode.

(2) When external VFO is used.

(3) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(4) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(5) ϕ_{CY} is a multiple of the period of a quartz crystal resonator connected to pins XA1-XA2 or an external clock connected to pin XA1. The multiple is eight (EXT = 0) or four (EXT = 1).

(6) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 3; High-Speed Floppy-Disk Control

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 300 kb/s

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	Note 1
DRQ cycle time	4	t_{MCY}	21.7			μs	DR1 = 1, DR0 = 1
$\overline{DACK}$ ↓ response time from DRQ ↑	4	t_{MA}	333.3			ns	
DRQ delay time from $\overline{DACK}$ ↓	4	t_{AM}			140	ns	
$\overline{DACK}$ pulse width	4	t_{AA}	8			ϕ_{CY}	Note 5
$\overline{RD}$ ↓ response time from DRQ ↑	4	t_{MR}	208.3			ns	DR1 = 1, DR0 = 1
$\overline{WR}$ ↓ response time from DRQ ↑	4	t_{MW}	416.7			ns	
$\overline{WR}$/$\overline{RD}$ response time from DRQ ↑	4	t_{MRW}			12	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	60			ϕ_{CY}	Note 5

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AC Characteristics 3; High-Speed Floppy-Disk Control (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	6	t_{RDD}	40			ns	
WINDOW cycle time (Note 2)	6	t_{WCY}		3.33		μs	MFM = 0
				1.67		μs	MFM = 1
WINDOW setup time to RDATA (Note 2)	6	t_{WRD}	15			ns	
WINDOW hold time from RDATA (Note 2)	6	t_{RDW}	15			ns	
US0, US1 setup time to SEEK	7	t_{US}	20			μs	Note 3
SEEK setup time to DIR	7	t_{SD}	11.7			μs	
DIR setup time to STEP	7	t_{DST}	1.7			μs	
US0, US1 hold time from STEP	7	t_{STU}	8.3			μs	
STEP high-level width	7	t_{STP}	10	11.7	13.3	μs	
US0, US1 hold time from SEEK (Note 4)	7	t_{SU}	25			μs	
DIR hold time from STEP	7	t_{STD}	40			μs	
SEEK hold time from DIR	7	t_{DS}	50			μs	
STEP cycle time	7	t_{SC}	55			μs	
FLTR high-level width	8	t_{FR}	13.3		16.7	μs	
INDEX high-level width	8	t_{IDX}	16			ϕ_{CY}	Note 5

Notes:

(1) For data transfer in non-DMA mode.

(2) When external VFO is used.

(3) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(4) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(5) ϕ_{CY} is a multiple of the period of a quartz crystal resonator connected to pins XB1-XB2 or an external clock connected to pin XB1. The multiple is four (EXT = 0) or two (EXT = 1).

(6) See figure 1 for timing measurement voltage thresholds.

Figure 1. Voltage Thresholds for Timing Measurements

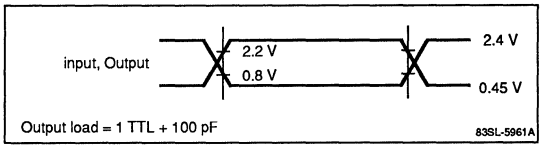

Figure 2. Read Operation

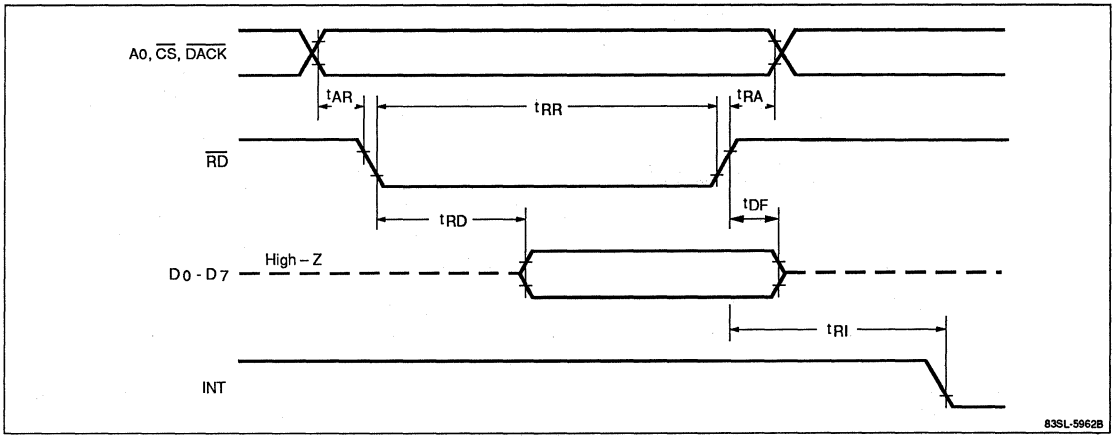

Figure 3. Write Operation

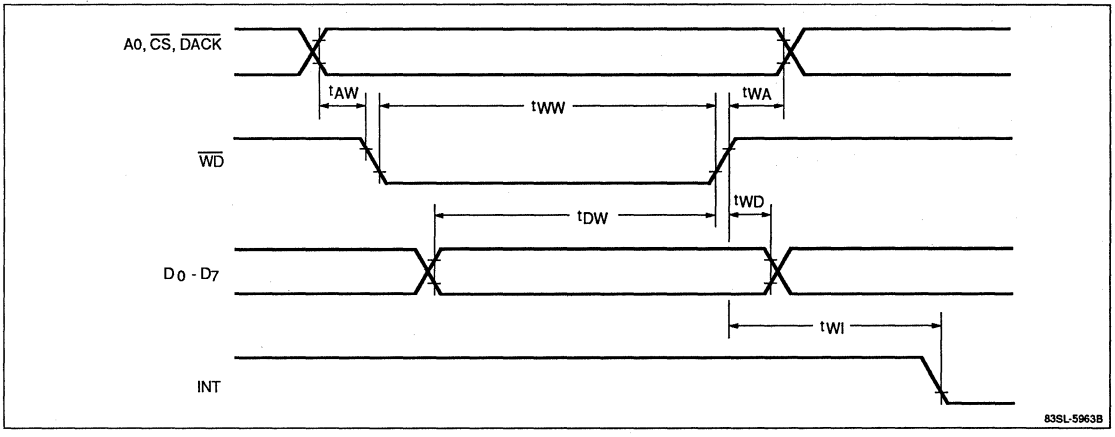

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Figure 4. DMA Operation

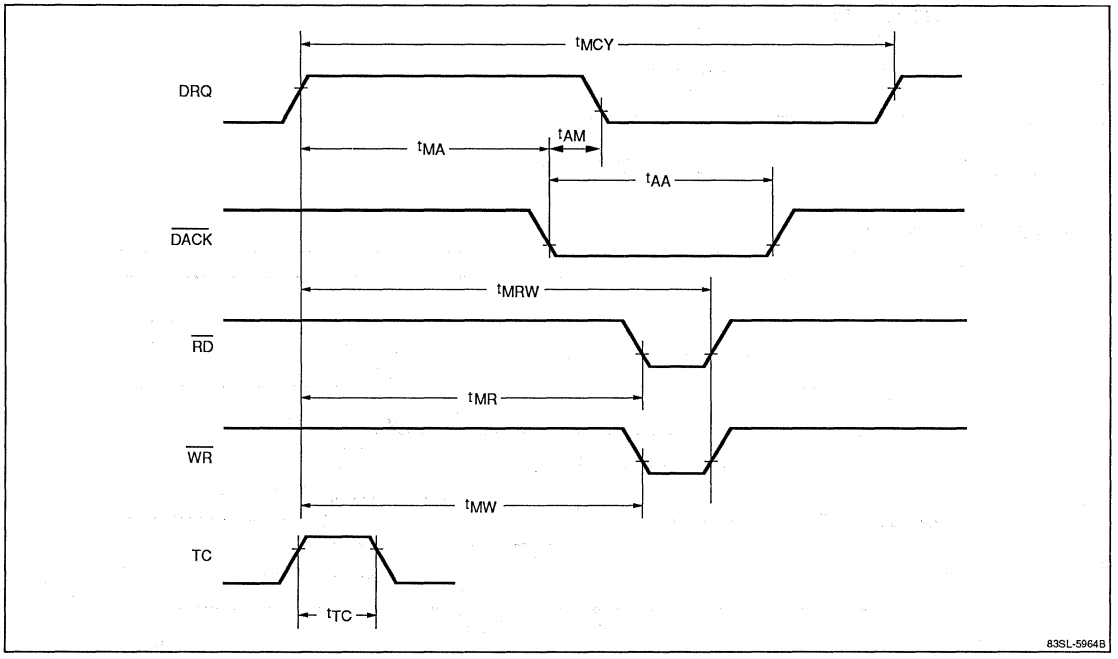


Figure 5. RESET Waveform

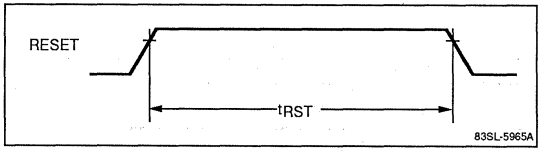


Figure 6. Device Read Operation

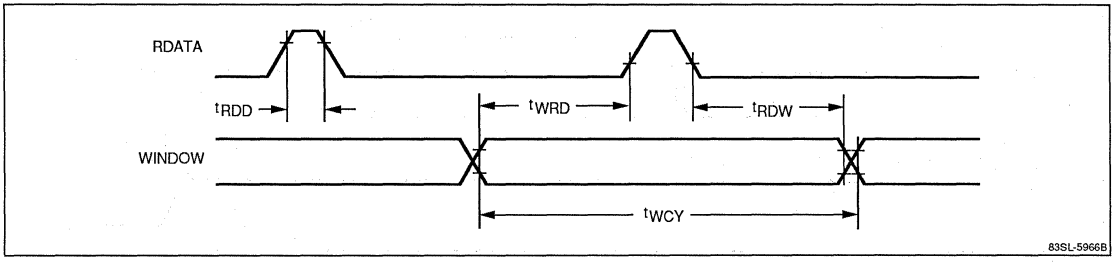


Figure 7. Seek Operation

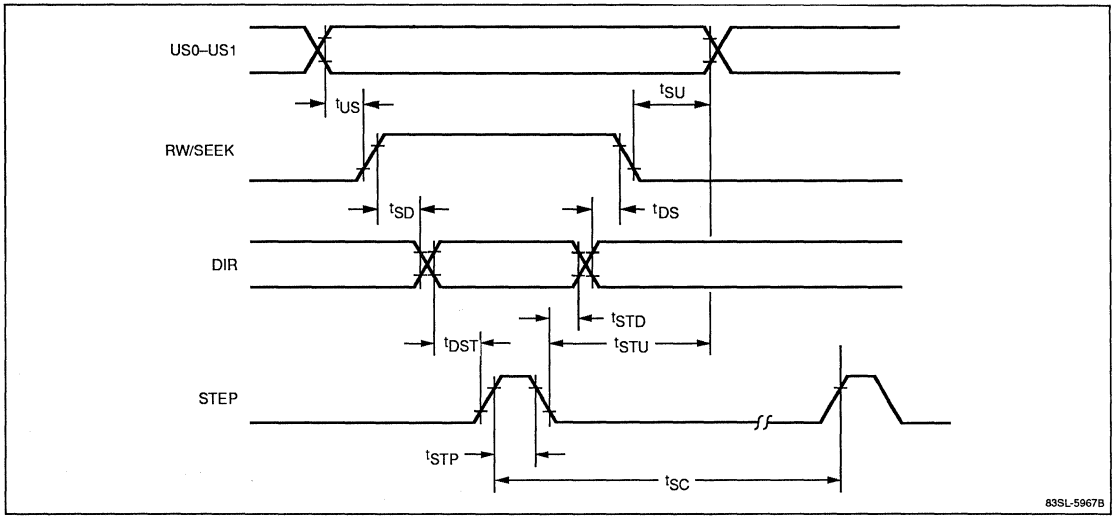
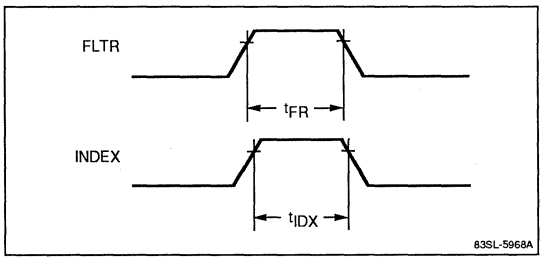


Figure 8. FLTR and INDEX Waveforms



Registers

The μPD72067 contains three 8-bit registers for interfacing the main system—data, status, and auxiliary command. Control signals $\overline{CS}$, A0, $\overline{RD}$, and $\overline{WR}$ select a particular register operation as shown in table 1.

(1) The data register temporarily stores information (command, parameter, data, or result status) transferred between the μPD72067 and the main system.

(2) The status register (table 2) indicates the state of the μPD72067. The main system can read the status register contents at any time.

(3) The auxiliary command register temporarily stores auxiliary commands given the μPD72067.

Table 1. Register Selection

$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	Operation
0	0	0	1	Read status register
0	0	1	0	Write auxiliary command register
0	1	0	1	Read data register
0	1	1	0	Write data register
1	x	x	x	Not defined

x = Don't care

Notes:

(1) When the DACK input is active low, data register selection is independent of $\overline{CS}$ and A0.

(2) When both $\overline{CS}$ and A0 are set to 0, a write of code other than auxiliary command code ($\overline{WR}$ = 0) is inhibited.

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Table 2. Status Register Contents

Bit	Name	Symbol	Description
D7	Request for master	RQM	Indicates μPD72067 is ready to transfer data to and from the main system. Operation depends on the DIO bit D6. When DIO = 0, the main system sends data to μPD72067. When the main system writes data into μPD72067, RQM is set to 0; when μPD72067 reads the data, RQM is set to 1. • C-phase, wait for command • Non-DMA write E-phase • SEEK type E-phase When DIO = 1, μPD72067 sends data to the main system. When μPD72067 places data in the data register, RQM is set to 1; when the main system reads the data, RQM is set to 0. • R-phase • Non-DMA read E-phase (except for READ ID)
D6	Data input/output	DIO	Indicates the data transfer direction between the main system and μPD72067. DIO Direction 0 Main system to μPD72067 1 μPD72067 to main system
D5	Non-DMA mode	NDM	Indicates data is being transferred in non-DMA mode (E-phase). In C- or R-phase, bit D5 is cleared.
D4	μPD72067 busy	CB	Indicates μPD72067 is in C-phase, R-phase, or read/write command E-phase. (In SEEK type E- phase, the CB bit D4 is not set to 1.) When bit D4 is set to 1, the next command is not acknowledged.
D3	FD3 busy	D3B	Indicates that device 3 performs seek operation or that a seek operation termination interrupt is pending (E-phase). When bit D3 is set to 1, a read/write type command must not be written.
D2	FD2 busy	D2B	Same as bit D3 for device 2.
D1	FD1 busy	D1B	Same as bit D3 for device 1.
D0	FD0 busy	D0B	Same as bit D3 for device 0.

Digital Phase-Locked Loop (DPLL)

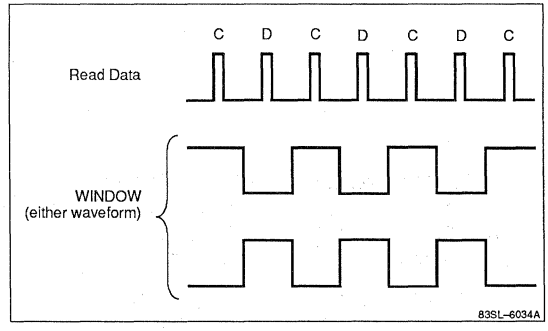
From the external 32-MHz system clock, the DPLL generates a WINDOW signal and synchronizes it with the phase and frequency of read data from a disk drive.

The frequency correction range and peak shift margin of the DPLL are affected by the data transfer rate (pin DR1).

DR1	Range	Margin
0	±25%	81.5
1	±25%	88.6

As shown in figure 9, read data is separated into data bits and clock bits by sampling with the WINDOW signal. The bits are centered in the window. If WINDOW is low for data bits, it is high for clock bits, and vice versa.

Figure 9. WINDOW Signal Waveform



Data Shift Register

In the read mode, the data shift register converts serial data into parallel form and outputs it to the 8-bit internal bus. In the write mode, the process is reversed and serial data is output to the CRC generator/checker and output mixer.

Clock Shift Register

In the read mode, the clock shift register converts serial clock bits into parallel form and outputs them to the 8-bit internal bus. In the write mode, the clock shift register converts parallel clock bits from the internal bus into a serial stream and sends it to the output mixer.

Cyclic Redundancy Check (CRC)

The CRC generator/checker operates with the polynomial $x^{16} + x^{12} + x^5 + 1$. In the read mode, the CRC of read data is calculated and compared with the CRC byte added following sector ID information and data. A mismatch produces an error indication.

In the write mode, CRC is calculated and two CRC bytes are added following ID information and data.

Precompensation

Because of the magnetic chracteristics of the media, read data is shifted from data write timing. Because the shift can be predicted according to the data pattern, it can be compensated by preshifting write data in the opposite direction.

Preshifting is used only for MFM mode, which has a data window half the width of the window in FM mode. The precompensation value (shift) is determined in the external mode by the input signals to pins PCS0 and PCS1, or in the internal mode by bits PS0 and PS1 of the CONTROL INTERNAL MODE command. See table 3.

Table 3. Precompensation Values

DR1	PCS1	PCS0	Shift
0	0	0	0.0
0	0	1	125.0
0	1	0	187.0
0	1	1	250.0
1	0	0	0.0
1	0	1	208.3
1	1	0	312.5
1	1	1	416.7

System Clocks

The system clock frequencies depend on the type of VFO and the type of floppy-disk. See table 4.

Table 4. System Clocks

VFO	Floppy-Disk	Clock XA	Clock XB
Internal	Standard or mini	32 MHz	
	High-density	32 MHz	19.2 MHz
External	Standard or mini	16 MHz	
	High-density	16 MHz	19.2 MHz

If a 32- or 16-MHz system clock is required, connect a quartz crystal resonator to pins XA1 and XA2, or connect an external clock signal to pin XA1 and leave XA2 open.

If a 19.2-MHz system clock is required, connect a quartz crystal resonator to pins XB1 and XB2, or connect an external clock signal to pin XB1 and leave XB2 open.

Internal Clocks

From the system clock, the μPD72067 generates the five internal clocks listed below.

(1) Internal system clock: controls internal operations and determines the data transfer rate.

(2) Write clock: frequency is twice the data transfer rate.

(3) DPLL clock: based on the 32-MHz system clock; source of the WINDOW signal.

(4) Precompensation clock

(5) 71065/66 clock: required if μPD71065 or μPD71066 is the external VFO.

Clock Selection

The system clock—32 or 16 MHz at the XA input or 19.2 MHz at the XB input—is selected by the state of the DR1 pin in external mode or the DR1 bit of the CONTROL INTERNAL MODE command in the internal mode.

For the selected system clock, the generated internal clock frequencies (table 5) are specified according to mode as follows.

(1) External mode: state of DR0 pin and command MFM bit.

(2) Internal mode: state of DR0 bit of CONTROL INTERNAL MODE command and MFM command bit.

When μPD71065 or μPD71066 is used as external VFO, the clock selected by the DR1 pin is output from the CLKOUT pin as the 71065/66 operation clock.

Table 5. Control Signals and Internal Clocks

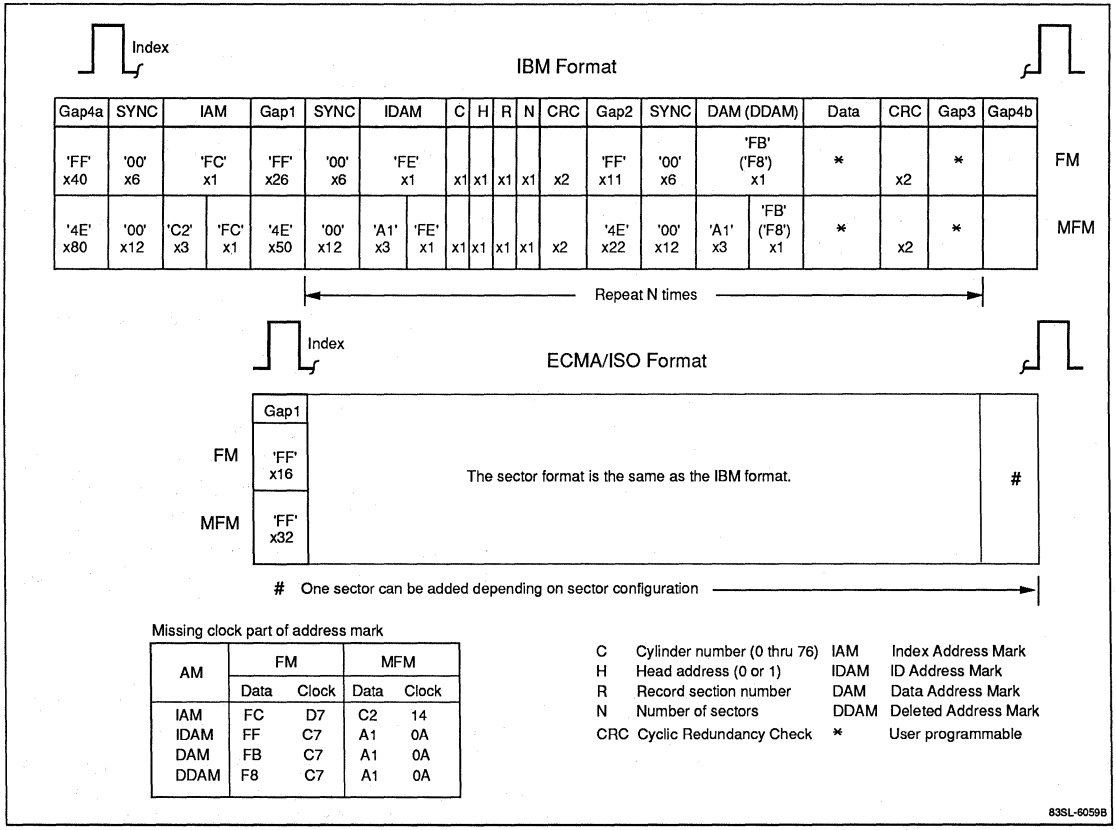
System Clock	DR1	DR0	MFM Bit	Data Transfer Rate (kb/s)	Internal Clocks: System (MHz)	Write (kHz)	DPLL (MHz)	Precomp	71065/66
32 MHz (Note 1) or 16 MHz (Note 2)	0	0	0	125	4	250	8	16 MHz	16 MHz
	0	0	1	250	4	500	16		
	0	1	0	250	8	500	16		
	0	1	1	500	8	1 MHz	32		
19.2 MHz	1	0	0	75	2.4	150	4.8	9.6 MHz	19.2 MHz
	1	0	1	150	2.4	300	9.6		
	1	1	0	150	4.8	300	9.6		
	1	1	1	300	4.8	600	19.2		

Notes:

(1) Internal VFO; internal mode with EXT = 0, or external mode.

(2) External VFO; internal mode with EXT = 1.

Figure 10. Track Formats



Format

The track format (IBM or ECMA/ISO) is specified by the FMT bit of the SELECT FORMAT command in internal mode or by the input signal to the FMT pin in external mode. See figure 10.

Commands

Table 6 describes the 15 commands and 8 auxiliary commands of the μPD72067.

System Bus Interface

Figure 11 is a reference circuit diagram of the interface between the μPD72067 and a system bus for data transfer in the DMA mode. The DMA controller is μPD71071. To prevent I/O port misselection during the DMA cycle, the Address Enable (AEN) output of μPD71071 inhibits other I/O ports.

Floppy-Disk Drive Interface

Figure 12 is a reference circuit diagram of the interface between a floppy-disk drive and the μPD72067 when the VFO is internal.

Figure 13 is a reference circuit diagram of the interface between a floppy-disk drive and the μPD72067 when the external VFO is μPD71065 or μPD71066. Special signal functions for this application are described below.

MFM	Recording system change signal
SYNC	Read enable/inhibit
CLKOUT	System clock to operate μPD71065/66
DRQ	Lock internal VFO (DPLL)
USO, US1	Drive select decoded by 74139
RW/SEEK	Select signal for demultiplexer (NAND gates) and multiplexer(LS157)

Table 6. List of Commands

Command Name	Function
Read Commands	
READ DATA	Specifies a sector and transfers its data to the host.
READ DELETED DATA	
READ ID	Reads a sector ID.
READ DIAGNOSTIC	Checks the track format.
SCAN EQUAL	Compares each sector data with host data and detects a sector that satisfies the set condition.
SCAN LOW OR EQUAL	
SCAN HIGH OR EQUAL	
Write Commands	
WRITE DATA	Specifies a sector and transfers its data to the host.
WRITE DELETED DATA	
WRITE ID	Writes the format of a track.
Seek Commands	
RECALIBRATE	Moves the read/write head to the outermost track (track 0).
SEEK	Moves the read/write head to the specified cylinder.
Sense Commands	
SENSE INTERRUPT STATUS	Reads the interrupt factor (seek end/state change) in the μPD72067.
SENSE DEVICE STATUS	Reads the FDD status.
Initialize Command	
SPECIFY	Defines a μPD72067 operation mode.
Auxiliary Commands	
SET STANDBY	Drives the μPD72067 in the standby status.
RESET STANDBY	Releases the μPD72067 from the standby status.
SOFTWARE RESET	Initializes the μPD72067.
ENABLE EXTERNAL MODE	Sets the μPD72067 in External Mode.
CONTROL INTERNAL MODE	Sets the μPD72067 in Internal Mode and sets both data transmission rate and precompensation value.
ENABLE MOTORS	Controls On/Off of the spindle motor.
SELECT FORMAT	Selects either IBM or ECMA/ISO format.
START CLOCK	Starts the clock generator operation.

Figure 11. μPD72067 to System Bus Interface

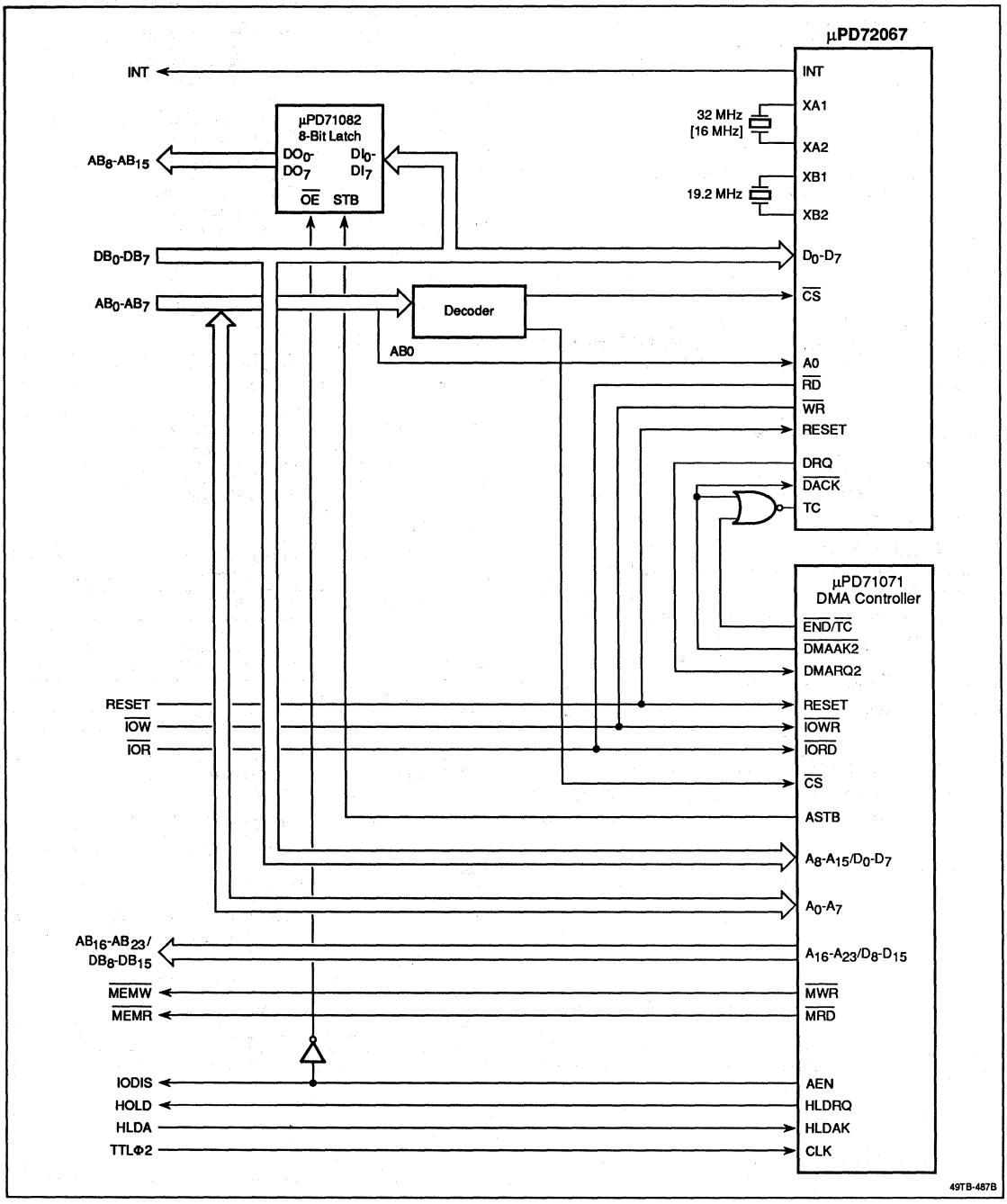


Figure 12. μPD72067 to FDD Interface 1

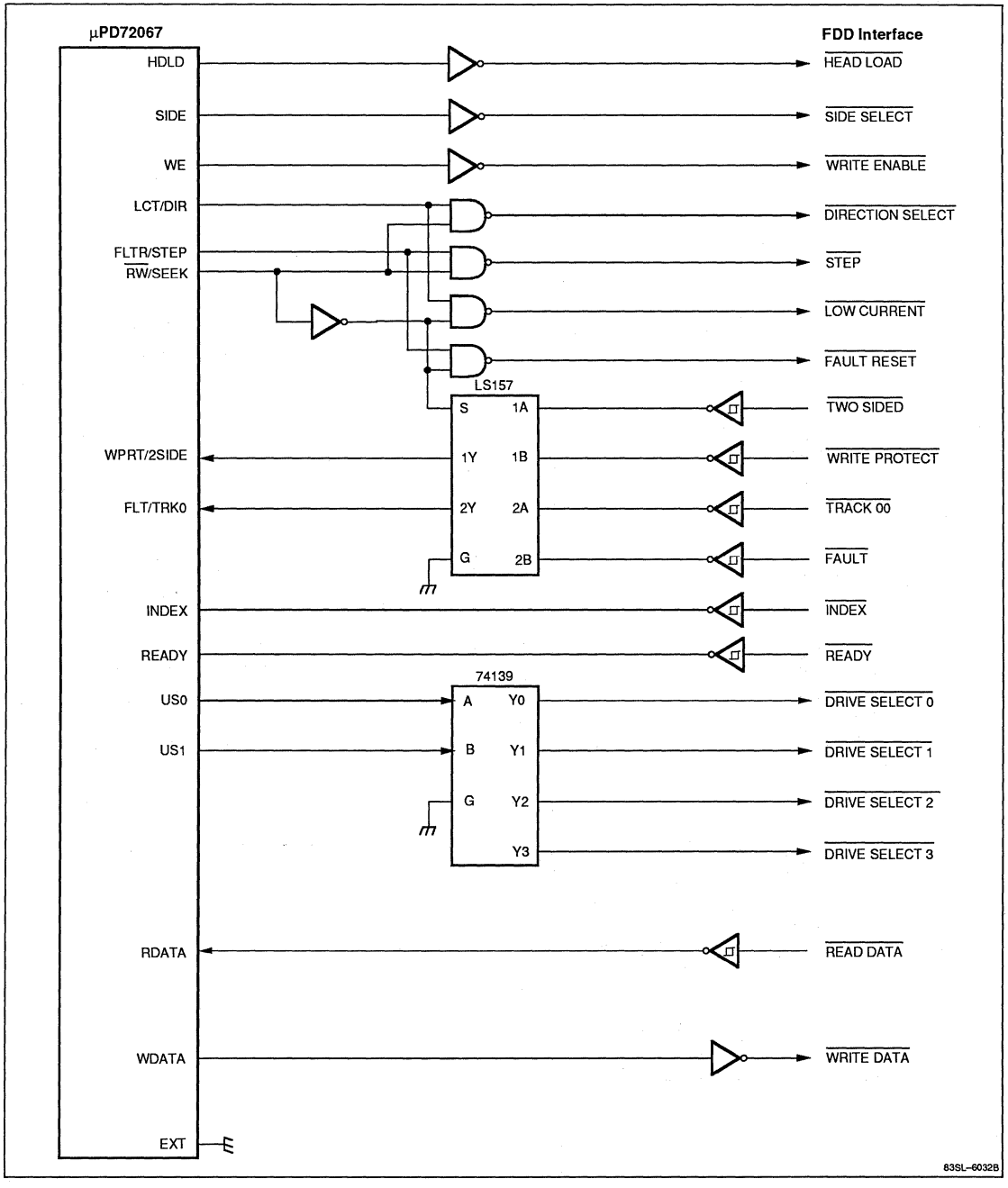
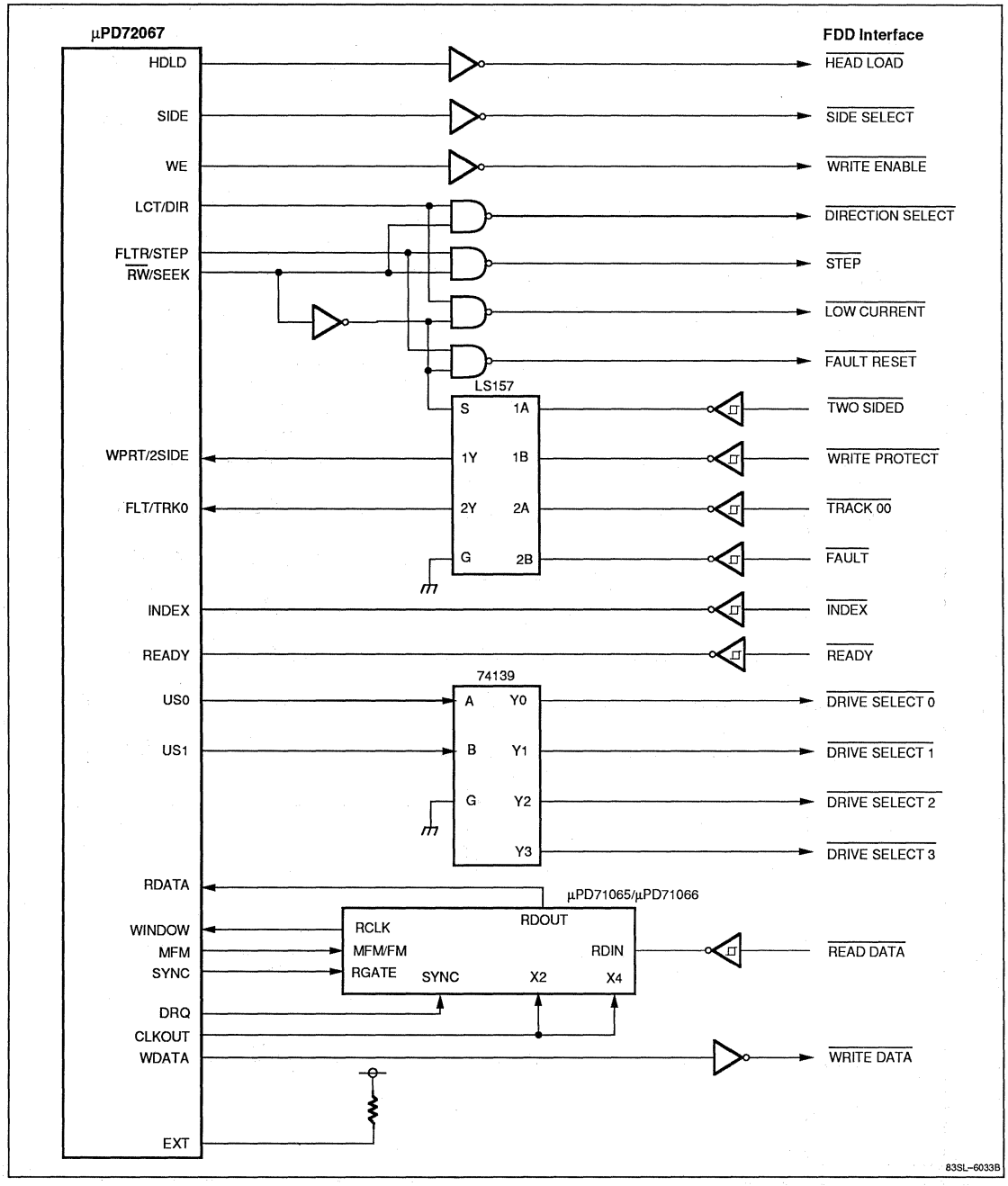


Figure 13. μPD72067 to FDD Interface 2



NEC Electronics Inc.

μPD72068
Floppy-Disk Controller

PRELIMINARY

Description

The μPD72068 FDC is one of NEC's integrated solutions for today's floppy-disk controller designs. An outgrowth of the μPD765A—long established as the industry standard for floppy-disk contol—the μPD72068 maintains complete microcode compatibility and contains the latest enhancements required for multitasking applications. Additionally, the μPD72068 integrates the standard host-interface registers used in IBM PC, PC/XT, PC/AT, and PS/2® designs.

The μPD72068 incorporates a high-performance digital PLL that is impervious to harmonic lock-on, a characteristic of analog counterparts. Being digital, the PLL requires no adjustments and supports all standard data rates as well as 600 kb/s.

The μPD72068 has on-chip clock generation, selectable write precompensation, and all the circuitry necessary for interfacing directly to four floppy-disk drives.

IBM PC, PC/XT, PC/AT, and PS/2 are registered trademarks of International Business Machines Corp.

Features

- Software compatible with μPD765A/765B, μPD7265, μPD72065/65B, μPD72066, and μPD72067
- Compatible with V-Series data/control bus and other standard 8/16-bit CPUs
- IBM and ECMA/ISO formats
- Data transfer rate: 600, 500, 300, 250, 150 kb/s
- High-performance, on-chip digital PLL
- Two system clock generators
- Programmable stepping speed
- Write-compensate circuit (programmable preshift)
- FDD interface
  - — High-current drivers (24-mA sink)
  - — Schmitt receivers
- Direct control of four FDDs
  - — Spindle motor control
  - — Unit select control
- Three selectable modes support:
  - — PC, PC/XT, PC/AT, PS/2 registers
  - — Internal operating mode selection
  - — External operating mode selection

Ordering Information

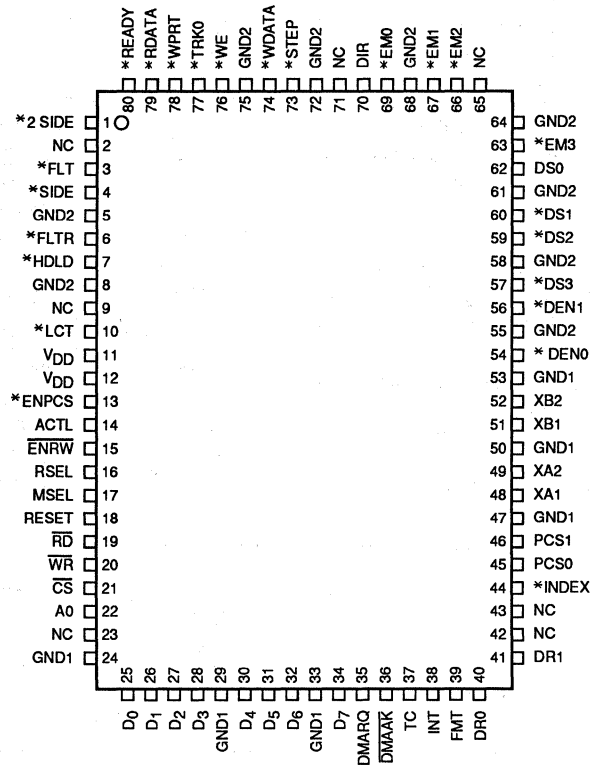
Part Number	Package
μPD72068GF-3B9	80-pin plastic miniflat
μPD72068L	84-pin PLCC (plastic leaded chip carrier)

5

50076

Pin Configurations

80-Pin Plastic Miniflat

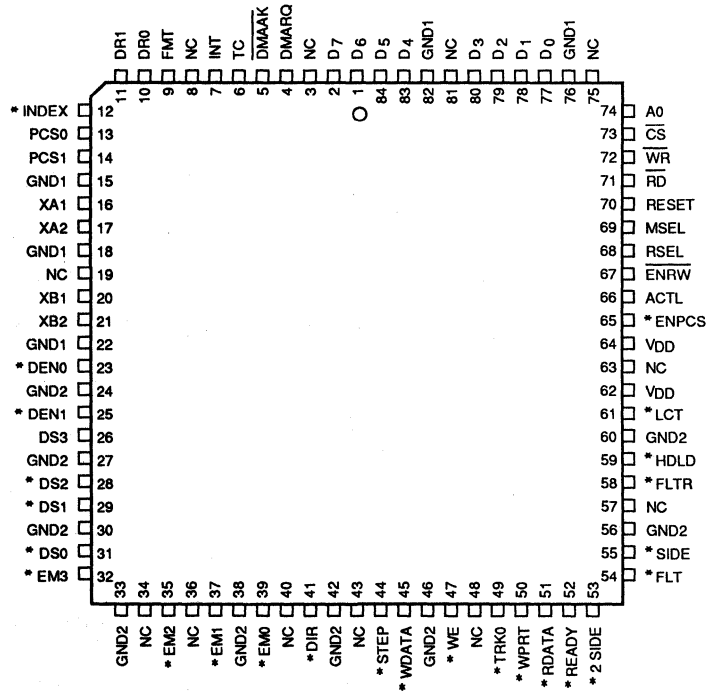


* Active level is variable.

Connect GND1 and GND2 to ground with the shortest possible wiring.

83vQ-5914B

84-Pin PLCC



* Active level is variable.

Connect GND1 and GND2 to ground with the shortest possible wiring.

83vO-5919B

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Pin Identification

Symbol	I/O	Signal Function
A0	In	Address 0. Selects μPD72068 registers. A0 Registers 0 Status, auxiliary command, digital out 1 Data, control
ACTL	In	Active Level. Sets active level of drive interface signal. ACTL Active Level 0 High 1 Low
$\overline{CS}$	In	Chip Select. Validates $\overline{RD}$ and $\overline{WR}$ signals when MSEL = 0. In Register mode (MSEL = 1), $\overline{CS}$ may be used as address line 1 in a typical PC system.
D_0-D_7	I/O	Data Bus. Bidirectional, three-state data bus.
DEN0, DEN1 (*)	Out	Density. Specifies preset data transfer rate; can be used for FDD data transfer rate control. See table 1.
DIR (*)	Out	Direction. Specifies the seek direction. DIR Seek Direction 0 Centrifugal 1 Centripetal
$\overline{DMAAK}$	In	DMA Acknowledge. Enables DMA cycle.
DMARQ	Out	DMA Request. Requests data transfer in DMA mode.
DR0, DR1	In	Data Rate. Sets data transfer rate in external mode. For internal mode, pull these pins low with high-value resistors.
DS0-DS3 (*)	Out	Drive Select. Selects up to four FDDs.
EM0-EM3 (*)	Out	Enable Motor. Controls spindle motor on/off; also can be used as a general-purpose output port.
ENPCS (*)	In	Enable Precompensation. ACTL ENPCS Preshift Value 0 0 0 ns 0 1 Assigned by mode 1 0 Assigned by mode 1 1 0 ns If the preshift amount is to be varied according to the number of cylinders, the appropriate control signal is input on ENPCS. When applying preshifting to cylinders 43 and above, variable control can be performed automatically by connecting the ENPCS and LCT pins.
$\overline{ENRW}$	In	Enable Read Write. Validate $\overline{RD}$ and $\overline{WR}$ signals when MSEL = 1. When MSEL = 0, this signal is meaningless.
FLT (*)	In	Fault. Indicates FDD is faulty.
FLTR (*)	Out	Fault Reset. Releases FDD from fault state.
FMT	In	Format. Selects format in external mode. FMT Format 0 IBM 1 ECMA For internal mode, pull this pin low with a high-value resistor.

Symbol	I/O	Signal Function
HDLD (*)	Out	Head Load. Causes the drive head to contact the diskette.
INDEX (*)	In	Indicates drive head is positioned at physical start point of track on the medium.
INT	Out	Interrupt Request. Requests main system to process transferred data and execution results.
LCT (*)	Out	Low Current. Indicates drive head has selected a cylinder after the 43rd.
MSEL	In	Mode Select. Validates IBM-PC register and on-chip peripheral circuits.
PCS0, PCS1	In	Precompensation. Selects the preshift amount in external or register mode. For internal mode, pull these pins low with high-value resistors.
$\overline{RD}$	In	Read. This control signal causes the main system to read data from the μPD72068 to the data bus.
RDATA (*)	In	Read data (consists of clock and data bits) from FDD.
READY (*)	In	Indicates FDD is ready.
RESET	In	Sets μPD72068 to idle state. FDD interface outputs except for WDATA (undefined) are: ACTL Output 0 All low 1 All high For the main system, INT and DMARQ are set to low and D_0-D_7 are set for input. When MSEL = 0, μPD72068 enters external mode directly after a reset.
RSEL	In	Register Select. When MSEL = 1, used with $\overline{CS}$ and A0 to select registers for IBM-PC (digital out register and control register). Invalid when MSEL = 0
SIDE (*)	Out	Side Select. Selects double-sided drive head. ACTL SIDE Drive Head 0 (Active high) 0 Head 0 0 1 Head 1 1 (Active low) 0 Head 1 1 1 Head 0
STEP (*)	Out	Generates seek pulses.
TC	In	Terminal Count. Terminates data transfer.
TRK0 (*)	In	Indicates drive head is positioned at cylinder 0.
WDATA (*)	Out	Write data (clock and data bits) to FDD.
WE (*)	Out	Requests FDD to write data.
WPRT (*)	In	Indicates medium is write-protected.
$\overline{WR}$	In	Write. Control signal that allows the main system to write data bus data into μPD72068.

Pin Identification (cont)

Symbol	I/O	Signal Function
XA1, XA2	In	Crystal A. For internal oscillator frequency control, a crystal resonator is connected to XA1 and XA2. For external clock input at XA1, XA2 is open. Frequency = 32 MHz To support only 500/250 kb/s data rates, crystal B is not necessary; connect XA2 to XB1.
XB1, XB2	In	Crystal B. For internal oscillator frequency control, a crystal resonator is connected to XB1 and XB2. For external clock input at XB1, XB2 is open. Frequency: 38.4 MHz; Data Rate: 600 kb/s Frequency: 19.2 MHz; Data Rate: All other rates To support only 500/250 kb/s data rates, crystal B is not necessary; connect XA2 to XB1.
2SIDE (*)	In	Indicates a medium with two usable sides has been loaded into the FDD.
NC	—	No Connection.
GND1	—	Digital system ground.
GND2	—	Buffer system ground.
V_{DD}	In	+5-volt power supply

(*) Active high when ACTL = 0; active low when ACTL = 1.

Pin Reset Status

Pin	Reset Status
D_0-D_7	Input
DMARQ, INT	Low
WDATA	Undefined
DIR, DS0-DS3, EM0-EM3, FLTR, HDLD, LCT, SIDE, STEP, WE	Low when ACTL =0; high when ACTL= 1.
DEN0, DEN1	Output depends on the preset data transfer rates. Value set when ACTL = 0 is inverted when ACTL = 1, and vice versa.
Other pins	

Table 1. Data Transfer Rate Settings

Mode	Input Pins DR1	DR0	D1	D0	MFM Data Transfer Rate (kb/s)	Output Pins DEN1	DEN0
Internal/ external (Note 1)	0	0	—	—	250	1	0
	0	1	—	—	500	1	1
	1	0	—	—	150 (300)	1	0
	1	1	—	—	300 (600)	0	0
Register (Note 2)	0	x	0	0	500	1	1
	0	x	0	1	250	1	0
	0	x	1	0	250	1	0
	0	x	1	1	150 (300)	1	0
	1	x	0	0	500	1	1
	1	x	0	1	300 (600)	0	0
	1	x	1	0	250	1	0
	1	x	1	1	150 (300)	1	0

Notes:

(1) In internal mode, DR1 and DR0 are bits of the CONTROL INTERNAL MODE command. In external mode, DR1 and DR0 are input pins.

(2) In register mode, DR0 input pin status is "Don't Care" (x).

(3) Data transfer rates in parentheses are with a 38.4-MHz crystal resonator connected to pins XB1 and XB2 or a 38.4-MHz clock connected to pin XB1.

(4) Data transfer rates are for MFM mode. In FM mode, these rates are halved.

(5) DEN1 and DN0 values are when ACTL = 1 (active low). When ACTL = 0 (active high), values are inverted.

Operation Modes

Since μPD72068 has been developed from μPD72067, the external and internal modes available for μPD72067 are also available for μPD72068 (exept the external VFO mode). In addition, the register mode is available for μPD72068. The register mode is used to operate the IBM-PC registers and special-purpose circuits of μPD72068. Procedures for setting the data transfer rate, precompensation amount, etc., vary depending on the modes. The differences in the procedures are shown in table 2.

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Table 2. Operation Modes

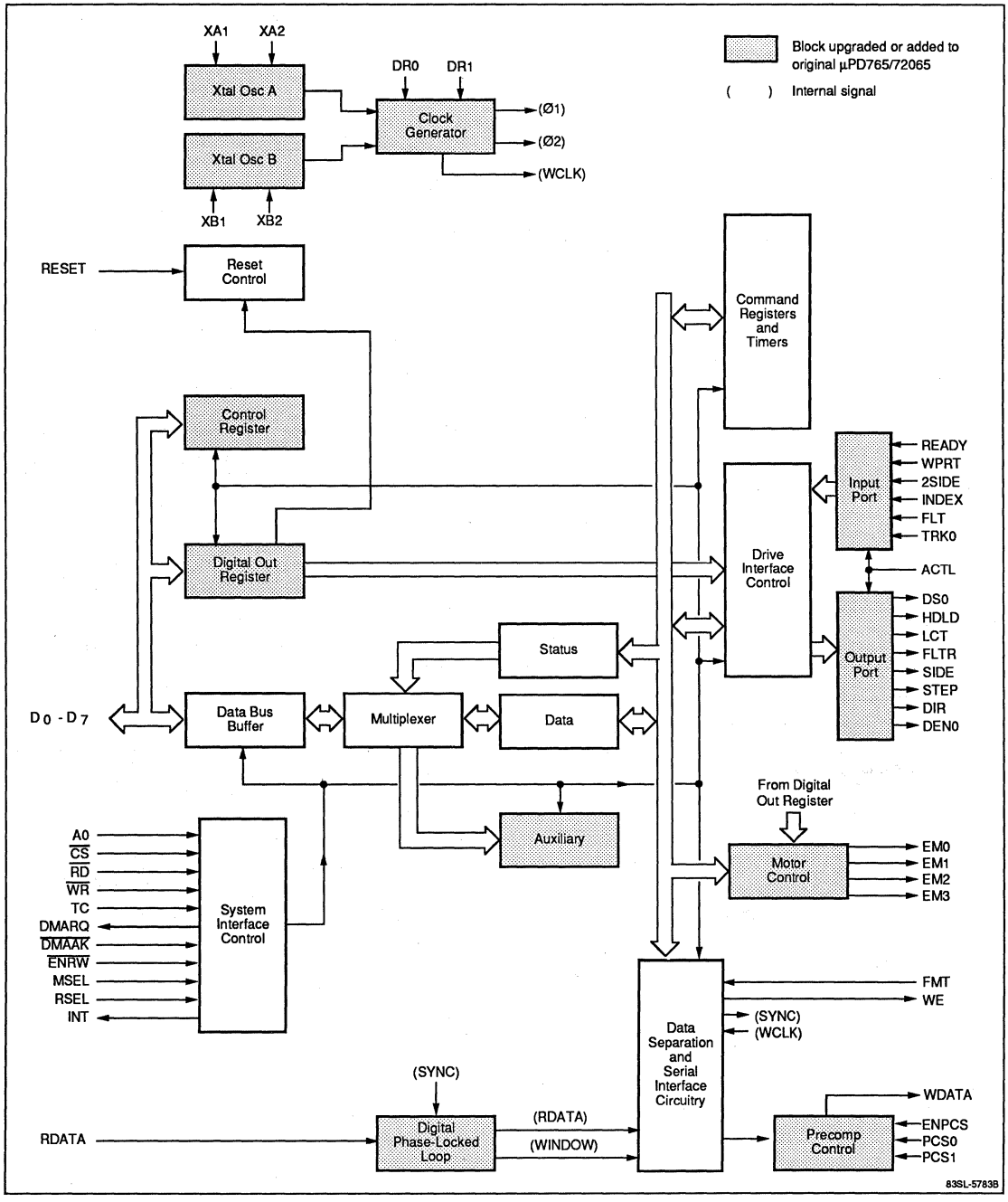
Mode	MSEL Pin	Command	Data Transfer Rate Setting	Drive Select	Precompensation Amount Setting	Format Change	Motor On/Off Control
Register mode	1	None	D0 and D1 bits and DR1 pin of control register	Digital out register	PCS0, PCS1, and DR1 pins	FMT pin	Digital out register
Internal mode	0	Note 1	CONTROL INTERNAL MODE command	US1 and US0 bits in the command	CONTROL INTERNAL MODE command	SELECT FORMAT command	ENABLE MOTORS command
External mode	0	Note 2	DR1 and DR0 pins		PCS1, PCS0, and DR1 pins	FMT pin	

Notes:

(1) CONTROL INTERNAL MODE command

(2) ENABLE EXTERNAL MODE command

μPD72068 Block Diagram



Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Voltage on any pin (except V_{DD})	−0.5 to +7 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to 150°C

Capacitance

T_A = +25°C; V_{DD} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Clock capacitance	C_ϕ		20	pF	Unmeasured pins returned to 0 V.
Input capacitance	C_{IN}		20	pF	
Output capacitance	C_{OUT}		20	pF	

Oscillator Specifications

T_A = −10 to +70°C; V_{DD} = +5 V ±10%; see figures 1, 2, and 3.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal Resonator Source						
Oscillator stabilization time (Note 1)	t_{KS}			10	ms	
External Clock, Direct Input						
Low-level input voltage	V_{IL}	−0.5		0.2 V_{DD}	V	Pins XA1, XB1
High-level input voltage	V_{IH}	0.8 V_{DD}		V_{DD} + 0.5	V	
Clock cycle	t_{CYA}		31.25		ns	Pin XA1
	t_{CYB}		52.08		ns	19.2-MHz clock input to pin XB1
			26.04		ns	38.4-MHz clock input to pin XB1
Permissible clock cycle error from typical value (Note 2)				±0.5	%	Pins XA1, XB1
Clock high-level width	t_{KKH}	7.0			ns	Pin XA1
		15.0			ns	Pin XB1; t_{CYB} = 52.08 ns
		6.0			ns	Pin XB1; t_{CYB} = 26.04 ns
Clock low-level width	t_{KKL}	7.0			ns	Pin XA1
		15.0			ns	Pin XB1; t_{CYB} = 52.08 ns
		6.0			ns	Pin XB1; t_{CYB} = 26.04 ns
Clock rise time	t_{KR}			5.0	ns	
Clock fall time	t_{KF}			5.0	ns	
External Clock, Capacitor-Coupled Input						
Clock input amplitude	V_{KP-P}	2.0		V_{DD}	V	Pins XA1, XB1
Clock cycle	t_{CYA}		31.25		ns	Pin XA1
	t_{CYB}		52.08		ns	19.2-MHz clock input to pin XB1
			26.04		ns	38.4-MHz clock input to pin XB1
Permissible clock cycle error from typical value (Note 2)				±0.5	%	Pins XA1, XB1
Duty cycle, high-level		40		60	%	

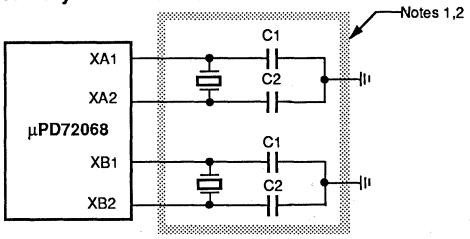
Notes:

(1) Oscillator stabilization time should also be taken as the wait time between the issuance of START CLOCK and RESET STANDBY commands.

(2) Clock cycle error affects DPLL performance.

Figure 1. Recommended External Clock Circuits

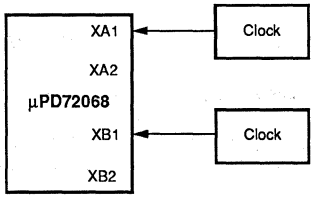
A. Crystal Resonator Source



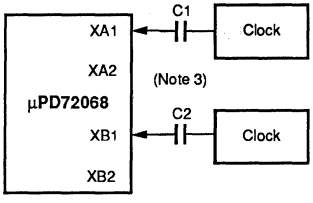
Frequency	*Part No.	C1, C2
32 MHz (pins XA1, XA2)	32 MHz EFD Type	15 pF ±20%
	TQC–254A–6R	10 pF ±20%
	TQC–254A–8R	
19.2 MHz (pins XB1, XB2)	TQC–253A–6R	16 pF ±20%
	TQC–253A–8R	

* Toyo Communication Equipment Co., Ltd.

B. External Clock, Direct Input



C. External Clock, Capacitor–Coupled



Notes:

(1) Oscillator circuit should be as close as possible to pins XA1, XA2, XB1, and XB2.

(2) No other signal lines should pass through shaded box.

(3) C1 and C2 = 110 to 10,000 pf.

83SL-5757A

Figure 2. External Clock Waveform

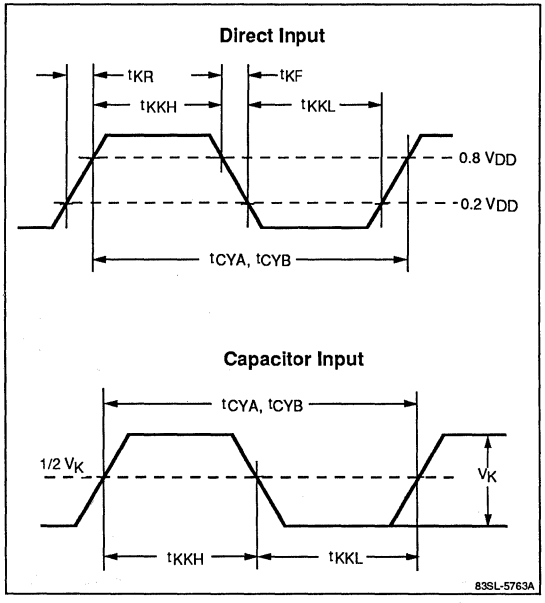
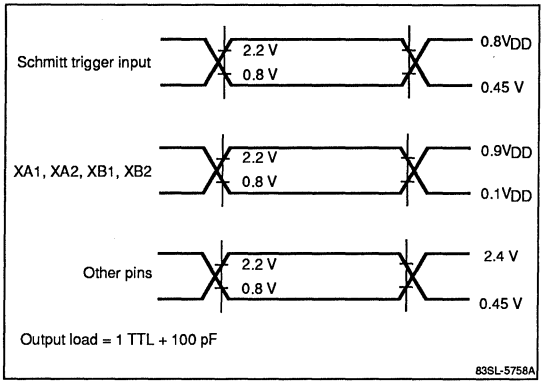


Figure 3. Voltage Thresholds for Timing Measurements



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DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Pin Groups	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL}	2	−0.5	0.8	V	
	V_{IL1}	1	−0.5	0.2 V_{DD}	V	
High-level input voltage	V_{IH}	2	2.2	V_{DD} + 0.5	V	
	V_{IH1}	1	0.8 V_{DD}	V_{DD} + 0.5	V	
Low-level output voltage	V_{OL}	4, 5		0.45	V	I_{OL} = 2.0 mA
	V_{OL1}	3		0.45	V	I_{OL} = 24.0 mA
High-level output voltage	V_{OH}	4, 5	0.7 V_{DD}	V_{DD}	V	I_{OH} = −200 μA
Low-level input leakage current	I_{LIL}	1, 2		−10	μA	V_{IN} = 0 V
High-level input leakage current	I_{LIH}	1, 2		+10	μA	V_{IN} = V_{DD}
Low-level output leakage current	I_{LOL}	4, 5		−10	μA	V_{OUT} = +0.45 V
	I_{LOL1}	3		−100	μA	
High-level output leakage current	I_{LOH}	4, 5		+10	μA	V_{OUT} = V_{DD}
	I_{LOH1}	3		+100	μA	
V_{DD} supply current	I_{DD}			60	mA	Note 1
Standby current	I_{DD1}			100	μA	Note 2

Notes:

(1) When a 32-MHz crystal is connected to XA1-XA2 and a 19.2-MHz crystal is connected to XB1-XB2.

(2) When an external clock is supplied, the clock should be fixed low during standby.

Pin Groups:

(1) Schmitt-trigger inputs: ENPCS, FLT, INDEX, RDATA, READY, TRK0, WPRT, 2SIDE.

(2) Non-Schmitt-trigger inputs and D_0-D_7; excludes XA1, XA2, XB1, XB2.

(3) Drive-side outputs when ACTL = 1 (active-low mode): DEN0-DEN1, DIR, DS0-DS3, EM0-EM3, FLTR, HDLD, LCT, SIDE, STEP, WDATA, WE.

(4) Drive-side outputs when ACTL = 0 (active-high mode): Same pins as group 3.

(5) Other than drive-side outputs; also D_0-D_7.

AC Characteristics 1; 500 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 500 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	13			μs	t_{CYA} = 31.25 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	200			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	8.5			t_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	125			ns	t_{CYA} = 31.25 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	250			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			12	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	128			t_{CYA}	When external clock is input to XA1 pin
Clock setup time after standby release	8	t_{CW}	64			t_{CYA}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	64			t_{CYA}	
INT response time from DMARQ ↓	9	t_{MI}	240		308	t_{CYA}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			4	t_{CYA}	

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AC Characteristics 1; 500 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		250		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	12			μs	t_{CYA} = 31.25 ns; Note 2
DIR setup time to STEP	11	t_{DST}	1			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	5			μs	
STEP high-level width	11	t_{STP}	6	7	8	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	15			μs	
DIR hold time from STEP	11	t_{STD}	24			μs	
STEP cycle time	11	t_{SC}	33			μs	
FLTR high-level width	12	t_{FR}	8		10	μs	
INDEX high-level width	12	t_{IDX}	16			t_{CYA}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 2; 250 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 250 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	26			μs	t_{CYA} = 31.25 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	400			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	16.5			t_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	250			ns	t_{CYA} = 31.25 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	500			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			24	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	256			t_{CYA}	When external clock is input to XA1 pin
Clock setup time after standby release	8	t_{CW}	128			t_{CYA}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	128			t_{CYA}	
INT response time from DMARQ ↓	9	t_{MI}	480		616	t_{CYA}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			8	t_{CYA}	

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AC Characteristics 2; 250 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		500		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	24			μs	t_{CYA} = 31.25 ns; Note 2
DIR setup time to STEP	11	t_{DST}	2			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	10			μs	
STEP high-level width	11	t_{STP}	12	14	16	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	30			μs	
DIR hold time from STEP	11	t_{STD}	48			μs	
STEP cycle time	11	t_{SC}	66			μs	
FLTR high-level width	12	t_{FR}	16		20	μs	
INDEX high-level width	12	t_{IDX}	32			t_{CYA}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 24 μs is actually 23.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 3; 300 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 300 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin); t_{CYB} = 52.08 ns (19.2 MHz at XB1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	21.7			μs	t_{CYB} = 52.08 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	333.3			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	8.3			t_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	208.3			ns	t_{CYB} = 52.08 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	416.7			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			20	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	128			t_{CYB}	When external clock is input to XB1 pin
Clock setup time after standby release	8	t_{CW}	64			t_{CYB}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	64			t_{CYB}	
INT response time from DMARQ ↓	9	t_{MI}	240		308	t_{CYB}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			4	t_{CYB}	

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AC Characteristics 3; 300 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		416.7		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	20			μs	t_{CYB} = 52.08 ns; Note 2
DIR setup time to STEP	11	t_{DST}	1.7			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	8.3			μs	
STEP high-level width	11	t_{STP}	10	11.7	13.3	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	25			μs	
DIR hold time from STEP	11	t_{STD}	40			μs	
STEP cycle time	11	t_{SC}	55			μs	
FLTR high-level width	12	t_{FR}	13.3		16.7	μs	
INDEX high-level width	12	t_{IDX}	16			t_{CYB}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 20 μs is actually 19.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 4; 150 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 150 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin); t_{CYB} = 52.08 ns (19.2 MHz at XB1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	43.4			μs	t_{CYB} = 52.08 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	666.6			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	16.3			t_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	416.7			ns	t_{CYB} = 52.08 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	833.4			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			40	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	256			t_{CYB}	When external clock is input to XB1 pin
Clock setup time after standby release	8	t_{CW}	128			t_{CYB}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	128			t_{CYB}	
INT response time from DMARQ ↓	9	t_{MI}	480		616	t_{CYB}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			8	t_{CYB}	

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AC Characteristics 4; 150 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		833.4		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	40			μs	t_{CYB} = 52.08 ns; Note 2
DIR setup time to STEP	11	t_{DST}	3.4			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	16.6			μs	
STEP high-level width	11	t_{STP}	20	23.4	26.6	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	50			μs	
DIR hold time from STEP	11	t_{STD}	80			μs	
STEP cycle time	11	t_{SC}	110			μs	
FLTR high-level width	12	t_{FR}	26.6		33.4	μs	
INDEX high-level width	12	t_{IDX}	32			t_{CYB}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 40 μs is actually 39.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 5; 600 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 600 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin); t_{CYB} = 26.04 ns (38.4 MHz at XB1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	10.8			μs	t_{CYB} = 26.04 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	166.7			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	8.6			t_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	104.2			ns	t_{CYB} = 26.04 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	208.3			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			12	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	128			t_{CYB}	When external clock is input to XB1 pin
Clock setup time after standby release	8	t_{CW}	64			t_{CYB}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	64			t_{CYB}	
INT response time from DMARQ ↓	9	t_{MI}	240		308	t_{CYB}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			4	t_{CYB}	

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AC Characteristics 5; 600 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		208.3		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	10			μs	t_{CYB} = 26.04 ns; Note 2
DIR setup time to STEP	11	t_{DST}	0.8			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	4.2			μs	
STEP high-level width	11	t_{STP}	5.0	5.8	6.7	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	12.5			μs	
DIR hold time from STEP	11	t_{STD}	20			μs	
STEP cycle time	11	t_{SC}	27.5			μs	
FLTR high-level width	12	t_{FR}	6.7		8.3	μs	
INDEX high-level width	12	t_{IDX}	16			t_{CYB}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 10 μs is actually 9.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 6; 300 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 300 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin); t_{CYB} = 26.04 ns (38.4 MHz at XB1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	21.7			μs	t_{CYB} = 26.04 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	333.3			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	16.6			t_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	208.3			ns	t_{CYB} = 26.04 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	416.7			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			24	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	256			t_{CYB}	When external clock is input to XB1 pin
Clock setup time after standby release	8	t_{CW}	128			t_{CYB}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	128			t_{CYB}	
INT response time from DMARQ ↓	9	t_{MI}	480		616	t_{CYB}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			8	t_{CYB}	

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AC Characteristics 6; 300 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		416.7		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	20			μs	t_{CYB} = 26.04 ns; Note 2
DIR setup time to STEP	11	t_{DST}	1.7			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	8.3			μs	
STEP high-level width	11	t_{STP}	10	11.7	13.3	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	25			μs	
DIR hold time from STEP	11	t_{STD}	40			μs	
STEP cycle time	11	t_{SC}	55			μs	
FLTR high-level width	12	t_{FR}	13.3		16.7	μs	
INDEX high-level width	12	t_{IDX}	32			t_{CYB}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 20 μs is actually 19.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

Figure 4. Read Operation

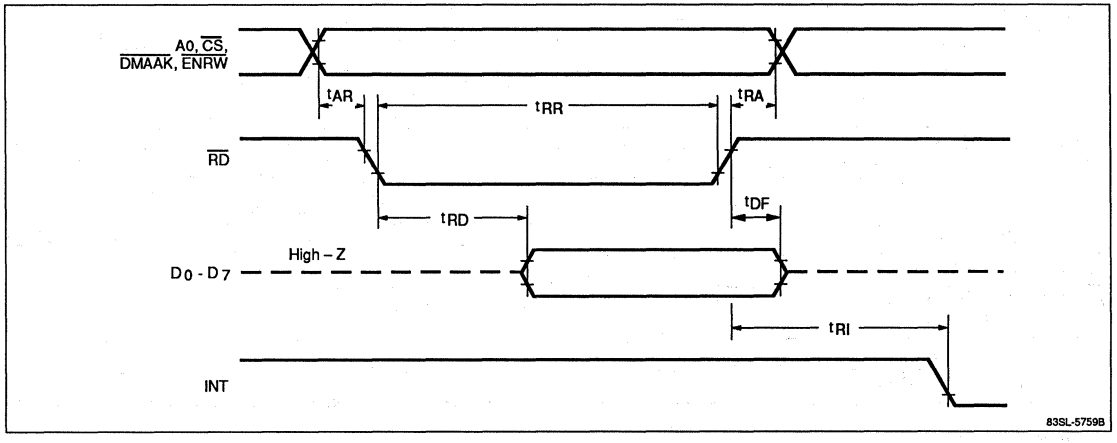

Figure 5. Write Operation

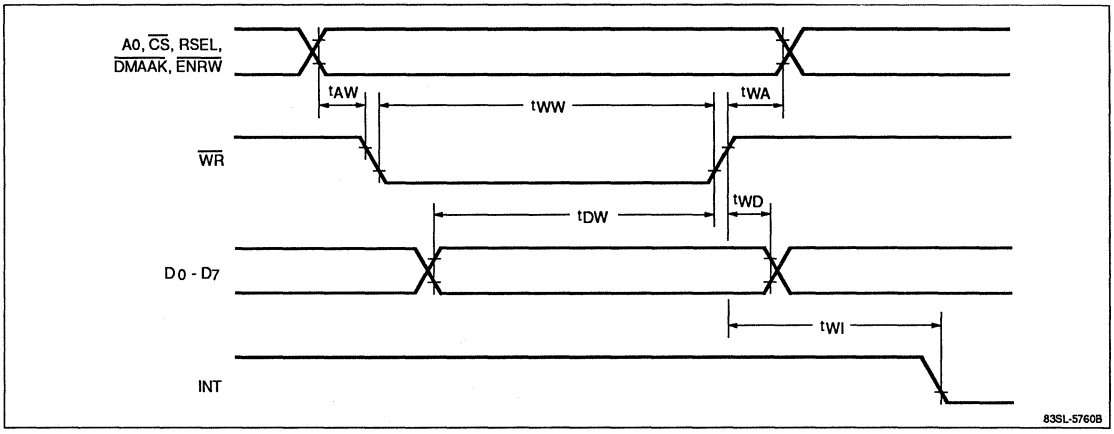

Figure. 6 DMA Operation

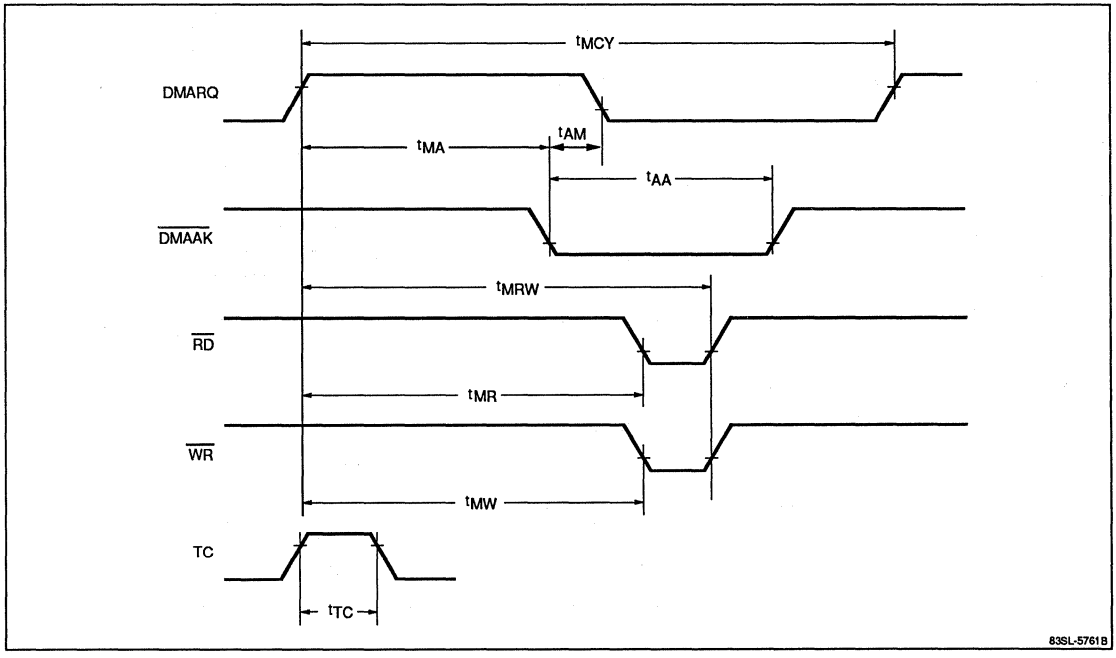

Figure 7. RESET Waveform

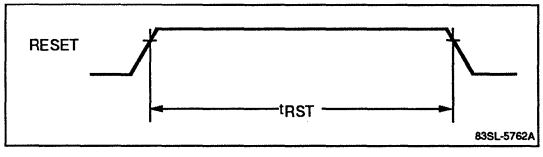

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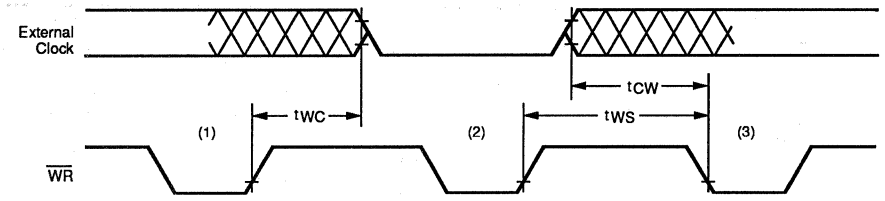
Figure 8. Standby Operation (With External Clock Input)



Notes:

(1) SET STANDBY command write.

(2) START CLOCK command write.

(3) RESET STANDBY command write.

(4) When in standby mode the external clock should be fixed low. The standby current specifications cannot be met unless this is done.

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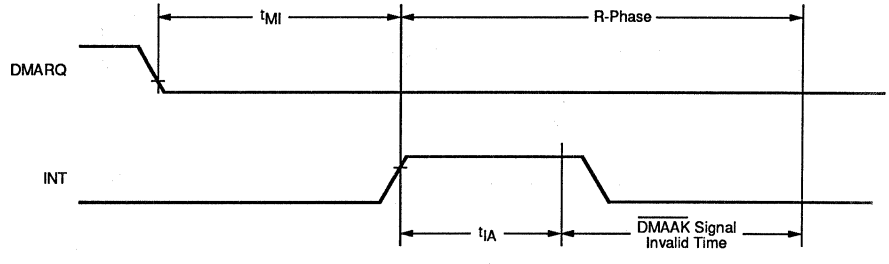
Figure. 9 Operation in Case of Overrun



INT generation on completion of command

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Figure 10. RDATA and WDATA Waveforms

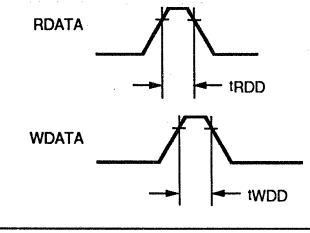

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Figure 11. Seek Operattion

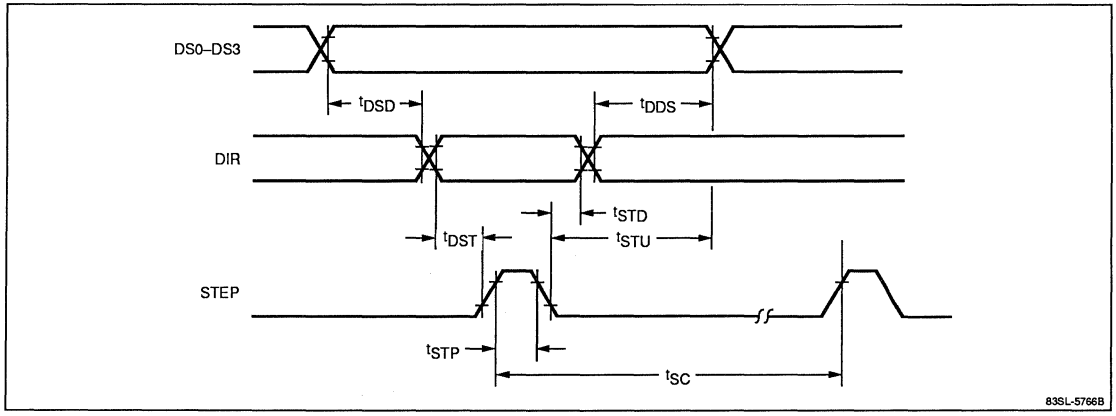
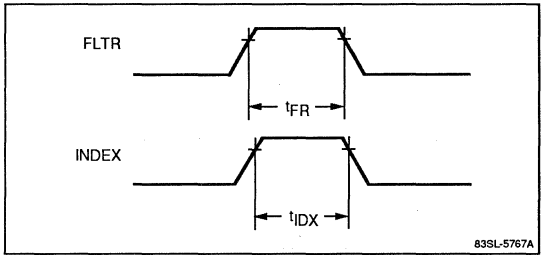


Figure 12. FLTR and INDEX Waveforms



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Description

The μPD72069 Floppy-Disk Controller (FDC) is one of NEC's integrated solutions for today's floppy-disk controller designs. An outgrowth of the μPD765A—long established as the industry standard for floppy-disk contol—the μPD72069 maintains complete microcode compatibility and contains the latest enhancements required for multitasking applications. Additionally, the μPD72069 integrates the standard host-interface registers used in IBM PC, PC/XT, PC/AT, and PS/2® designs.

The μPD72069 incorporates a high-performance analog PLL that requires no adjustments and supports all standard data rates as well as 600 kb/s and 1 Mb/s for the latest advances in tape and disk technology.

The μPD72069 has on-chip clock generation, selectable write precompensation, and all the circuitry necessary for interfacing directly to four floppy-disk drives.

Features

- 100% μPD765A/765B software and hardware compatible
- IBM and ECMA (Sony) formats
- Analog PLL (no adjustment required)
- Data transfer rate: 1 Mb/s; 600, 500, 300, 250, 150 kb/s
- Two system clock generators
- Write precompensation (programmable shift values)
- Programmable stepping speed
- Direct control of four FDDs
  - — Spindle motor control
  - — Unit select control
  - — High-current driver outputs (open drain)
- Three selectable modes support:
  - — PC, PC/XT, PC/AT registers
  - — Internal operating mode selection
  - — External operating mode selection

Ordering Information

Part Number	Package
μPD72069GF-3BA	100-pin plastic miniflat
μPD72069L	84-pin PLCC (plastic leaded chip carrier)

IBM PC, PC/XT, PC/AT, and PS/2 are registered trademarks of International Business Machines Corp.

Pin Identification

Symbol	I/O	Signal Function
A0	In	Address 0. Selects a register in μPD72069.
ACTL	In	Active Level. Sets active level of drive interface signal. ACTL — Active Level 0 — High 1 — Low
CGP1, CGP2	Out	Charge Pump. Phase difference of sub PLL devices.
$\overline{CS}$	In	Chip Select. Validates $\overline{RD}$ and $\overline{WR}$ signals.
D_0-D_7	I/O	Data Bus. Bidirectional, three-state data bus.
DEN0, DEN1 (*)	Out	Density. Specifies the density of a drive that can support more than one density. The output is a value corresponding to the selected data transmision rate. DEN0: When DR1 = 0 and DR0 = 1, the DEN0 output is 1. Otherwise it is 0. DEN1: When DR1 = 1 and DR0 = 1, the DEN1 output is 0. Otherwise it is 1. The values specified above are applicable when ACTL = 1. The values are reversed when ACTL = 0.
DIR (*)	Out	Direction. Specifies the seek direction. ACTL — DIR — Direction 0 — 0 — Outward 0 — 1 — Inward 1 — 0 — Inward 1 — 1 — Outward
$\overline{DMAAK}$	In	DMA Acknowledge. Enables DMA cycle.
DMARQ	Out	DMA Request. Requests data transfer in DMA mode.
DR0-DR2	In	Data Rate. Sets data transfer rate in external mode.
DS0-DS3 (*)	Out	Drive Select. Selects up to four FDDs.
EM0-EM4 (*)	Out	Enable Motor. Controls FDD spindle motor on/off; also can be used as a general-purpose output port.
ENIDX (*)	In	Enable Index. Validates INDEX and RDATA signals from FDD.
ENPCS (*)	In	Enable Precompensation. This pin is usually connected to the LCT pin
$\overline{ENRW}$	In	Enable Read Write. Validate $\overline{RD}$ and $\overline{WR}$ signals when MSEL = 1. When MSEL = 0, this signal is meaningless.
FLT (*)	In	Fault. Indicates FDD is faulty.
FLTR (*)	Out	Fault Reset. Releases FDD from fault state.

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Pin Identification (cont)

Symbol	I/O	Signal Function
FMT	In	Format. Selects format in external mode. FMT Format 0 IBM 1 ECMA/ISO
HDLD (*)	Out	Head Load. Sets drive head in the load state.
INDEX (*)	In	Indicates drive head is positioned at physical start point of track on the medium.
INT	Out	Interrupt Request. Requests main system to process transferred data and execution results.
LCT (*)	Out	Low Current. Indicates drive head has selected a cylinder on or after the 43rd.
LPF1, LPF2	Out	Lowpass Filter. Phase difference of main PLL devices.
MSEL	In	Mode Select. Validates IBM-PC register and on-chip peripheral circuit.
PCS0, PCS1	In	Precompensation. Sets precompensation value in external or register mode.
$\overline{RD}$	In	Read. This control signal causes the main system to read data from the μPD72069 to the data bus.
RDATA (*)	In	Read data (consists of clock and data bits) from FDD.
READY (*)	In	Indicates FDD is ready.
RESET	In	Sets μPD72069 to idle state. FDD interface outputs except for WDATA (undefined) are: ACTL Output 0 All low 1 All high For the main system, INT and DMARQ are set to low and D_0-D_7 are set for input.
RSEL	In	Register Select. When MSEL = 1, used with $\overline{CS}$ and A0 to select register for IBM-PC (digital out register or control register). Invalid when MSEL = 0
SIDE (*)	Out	Side Select. Selects double-sided drive head. ACTL SIDE Drive Head 0 0 Head 0 0 1 Head 1 1 0 Head 1 1 1 Head 0
STEP (*)	Out	Generates seek pulses.
TC	In	Terminal Count. Terminates data transfer.
TRK0 (*)	In	Indicates drive head is positioned at cylinder 0.
WDATA (*)	Out	Write data (clock and data bits) to FDD.
WE (*)	Out	Requests FDD to write data.
WPRT (*)	In	Indicates medium is write-protected.
$\overline{WR}$	In	Write. Control signal that allows the main system to write data bus data into μPD72069.

Pin Identification (cont)

Symbol	I/O	Signal Function
XA1, XA2	In	Crystal A. For internal oscillator frequency control, a crystal resonator is connected to XA1 and XA2. For external clock input at XA1, XA2 is open. Frequency = 16 MHz
XB1, XB2	In	Crystal B. For internal oscillator frequency control, a crystal resonator is connected to XB1 and XB2. For external clock input at XB1, XB2 is open. Frequency = 19.2 MHz
2SIDE (*)	In	Indicates a medium with two usable sides has been loaded into the FDD.
IC	—	Internal Connection. Connect to GND1
NC	—	No Connection.
GND1	—	Ground for digital devices.
GND2	—	Ground for analog devices.
GND3	—	Ground for buffers.
V_{DD1}	In	+5-volt power supply for digital devices.
V_{DD2}	In	+5-volt power supply for analog devices.

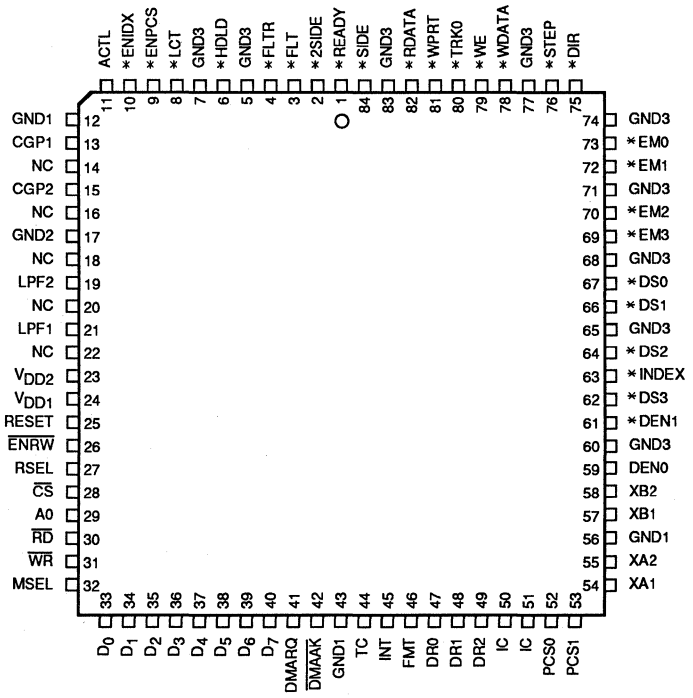
(*) Active high when ACTL = 0; active low when ACTL = 1.

Output Pin Reset Status

Pin	Reset Status
D_0-D_7	Input
DMARQ, INT	Low
CGP1, CGP2, LPF1, LPF2, WDATA	Undefined
DIR, DS0-DS3, EM0-EM3, FLTR, HDLD, LCT, SIDE, STEP, WE	Low when ACTL =0; high when ACTL= 1.
DEN0, DEN1	Output depends on the preset data transfer rates. Value set when ACTL = 0 is inverted when ACTL = 1, and vice versa.

Pin Configurations

84-Pin PLCC



* Active level is variable

IC Connect to GND1

Connect GND1, GND2, and GND3 to main ground with the shortest possible wiring

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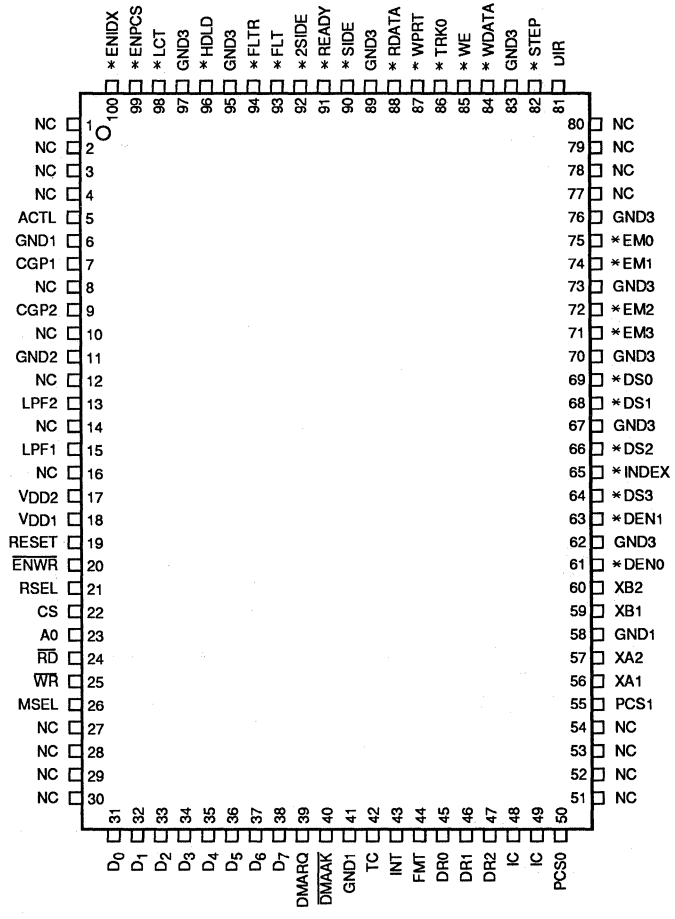
100-Pin Plastic Miniflat



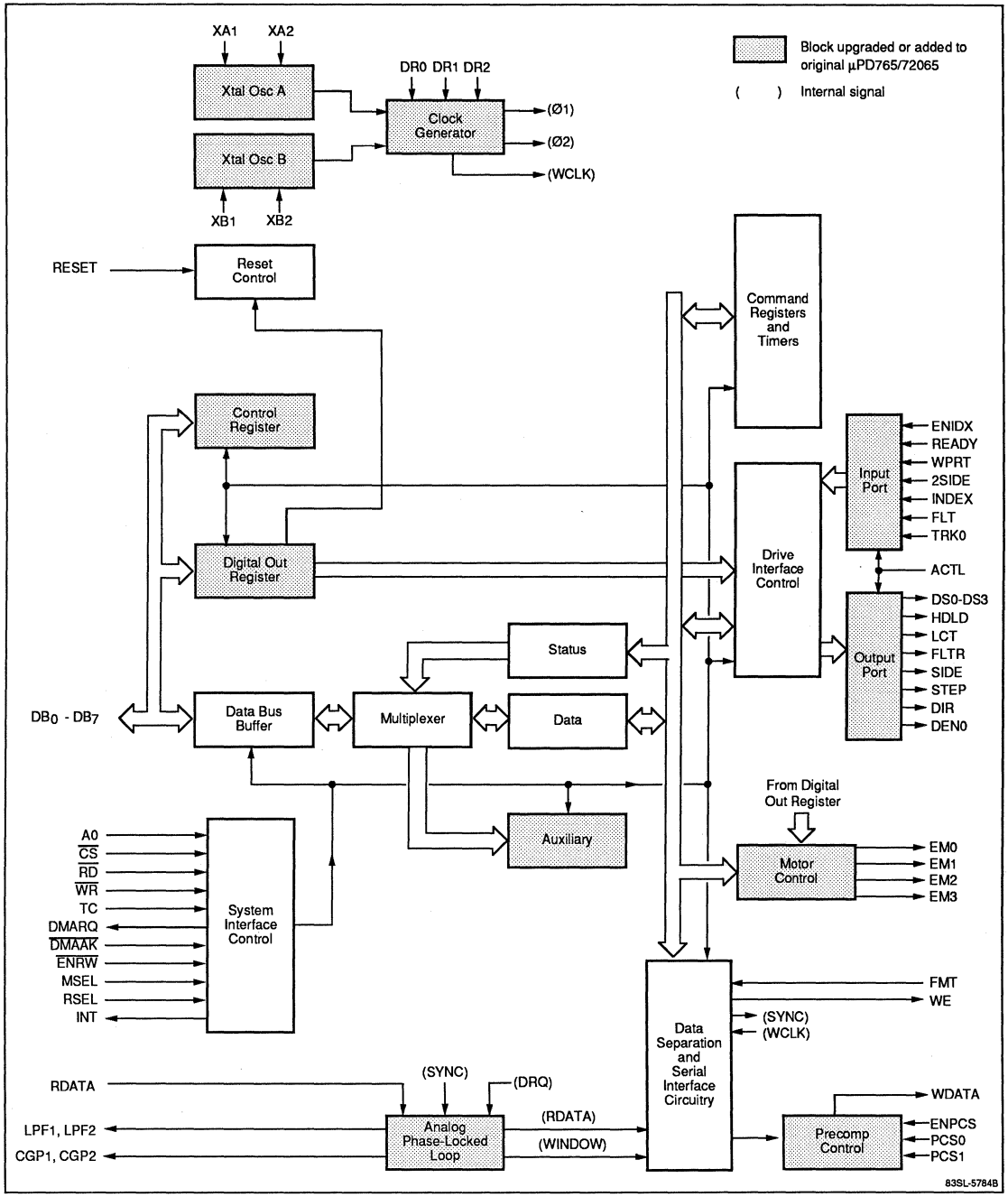
* Active level is variable

IC Connect to GND1

Connect GND1, GND2, and GND3 to main ground with the shortest possible wiring

83vO-5921B

μPD72069 Block Diagram



Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Voltage on any pin (except V_{DD})	−0.5 to +7 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to 150°C

Oscillator Specifications

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Low-level input voltage	V_{IL}	−0.5		0.2 V_{DD}	V	Pins XA1, XB1
High-level input voltage	V_{IH}	0.8 V_{DD}		V_{DD} + 0.5	V	
Clock cycle	ϕ_{CYA}	62.2	62.5	63.8	ns	Pins XA1, XA2
	ϕ_{CYB}	51.8	52.08	52.3	ns	Pins XB1, XB2
Clock width, high/low	ϕ_ℓ	0.35		0.65	ϕ_{CYA}, ϕ_{CYB}	
Clock rise time	ϕ_R			0.15	ϕ_{CYA}, ϕ_{CYB}	
Clock fall time	ϕ_F			0.15	ϕ_{CYA}, ϕ_{CYB}	

Analog PLL Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
VCO free-run frequency	f_T	9.9	10.0	10.1	MHz
f_T power supply voltage coefficient	f_{TUDD}	−0.1	0	+0.1	%/V
f_T temperature coefficient	f_{TTA}	−10	0	+10	ppm/°C
Capture range	f_{CTB}	±7.5			%
Lock range	f_{CTA}	±10			%
Capture range power supply voltage coefficient	f_{CTUD}	−5	0	+5	%/V
Capture range temperature coefficient	f_{CTTA}	−5	0	+5	ppm/°C
VCO jitter	t_{JIT}	0		2	ns
Peak shift margin	t_{PFTM}	80			%
Pull-in time	t_{PLIN}			20	bit

AC Characteristics 1; 1 Mb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;

MFM data transfer rate = 1 Mb/s; ϕ_{CYA} = 62.5 ns (16 MHz at XA1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	6.5			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	100			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	2			ϕ_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	62.5			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	125			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			6	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	32			ϕ_{CYA}	When external clock is input to XA1 pin.
Clock setup time at standby release	6	t_{CW}	16			ϕ_{CYA}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	16			ϕ_{CYA}	
INT response time from DMARQ ↓	7	t_{MI}	60		77	ϕ_{CYA}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			1	ϕ_{CYA}	

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AC Characteristics 1; 1 Mb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ active-low time	8	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ active-low time	8	t_{WDD}		125		ns	
DS0-DS3 setup time to $\overline{\text{DIR}}$	9	t_{DSD}	9.5			μs	Note 2
DIR setup time to $\overline{\text{STEP}}$	9	t_{DST}	0.5			μs	
DS0-DS3 hold time after $\overline{\text{STEP}}$	9	t_{STU}	2.5			μs	
$\overline{\text{STEP}}$ active-low time	9	t_{STP}	3	3.5	4	μs	
DS0-DS3 hold time after $\overline{\text{DIR}}$ (Note 1)	9	t_{DDS}	22.5			μs	
DIR hold time after $\overline{\text{STEP}}$	9	t_{STD}	12			μs	
$\overline{\text{STEP}}$ cycle time	9	t_{SC}	16.5			μs	
$\overline{\text{FLTR}}$ active-low time	10	t_{FR}	4		5	μs	
$\overline{\text{INDEX}}$ low time	10	t_{IDX}	4			ϕ_{CYA}	

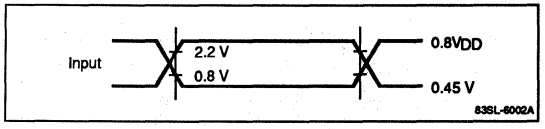
Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 9.5 μs is actually 9.450 μs.

(3) See figure 1 for timing measurement voltage thresholds.

Figure 1. Voltage Threshold for Timing Measurements



AC Characteristics 2; 500 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 500 kb/s; ϕ_{CYA} = 62.5 ns (16 MHz at XA1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	13			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	200			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	4			ϕ_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	125			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	250			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			12	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	64			ϕ_{CYA}	When external clock is input to XA1 pin.
Clock setup time at standby release	6	t_{CW}	32			ϕ_{CYA}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	32			ϕ_{CYA}	
INT response time from DMARQ ↓	7	t_{MI}	120		154	ϕ_{CYA}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			2	ϕ_{CYA}	

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AC Characteristics 2; 500 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ active-low time	8	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ active-low time	8	t_{WDD}		250		ns	
DS0-DS3 setup time to $\overline{\text{DIR}}$	9	t_{DSD}	19			μs	Note 2
DIR setup time to $\overline{\text{STEP}}$	9	t_{DST}	1			μs	
DS0-DS3 hold time after $\overline{\text{STEP}}$	9	t_{STU}	5			μs	
$\overline{\text{STEP}}$ active-low time	9	t_{STP}	6	7	8	μs	
DS0-DS3 hold time after $\overline{\text{DIR}}$ (Note 1)	9	t_{DDS}	45			μs	
DIR hold time after $\overline{\text{STEP}}$	9	t_{STD}	24			μs	
$\overline{\text{STEP}}$ cycle time	9	t_{SC}	33			μs	
$\overline{\text{FLTR}}$ active-low time	10	t_{FR}	8		10	μs	
$\overline{\text{INDEX}}$ low time	10	t_{IDX}	8			ϕ_{CYA}	

Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 19 μs is actually 18.950 μs.

(3) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 3; 250 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;

MFM data transfer rate = 250 kb/s; ϕ_{CYA} = 62.5 ns (16 MHz at XA1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	26			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	400			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	8			ϕ_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	250			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	500			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			6	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	128			ϕ_{CYA}	When external clock is input to XA1 pin.
Clock setup time at standby release	6	t_{CW}	64			ϕ_{CYA}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	64			ϕ_{CYA}	
INT response time from DMARQ ↓	7	t_{MI}	240		308	ϕ_{CYA}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			4	ϕ_{CYA}	

5

AC Characteristics 3; 250 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ active-low time	8	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ active-low time	8	t_{WDD}		500		ns	
DS0-DS3 setup time to $\overline{\text{DIR}}$	9	t_{DSD}	38			μs	Note 2
DIR setup time to $\overline{\text{STEP}}$	9	t_{DST}	2			μs	
DS0-DS3 hold time after $\overline{\text{STEP}}$	9	t_{STU}	10			μs	
$\overline{\text{STEP}}$ active-low time	9	t_{STP}	12	14	16	μs	
DS0-DS3 hold time after $\overline{\text{DIR}}$ (Note 1)	9	t_{DDS}	90			μs	
DIR hold time after $\overline{\text{STEP}}$	9	t_{STD}	48			μs	
$\overline{\text{STEP}}$ cycle time	9	t_{SC}	66			μs	
$\overline{\text{FLTR}}$ active-low time	10	t_{FR}	16		20	μs	
$\overline{\text{INDEX}}$ low time	10	t_{IDX}	16			ϕ_{CYA}	

Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 38 μs is actually 37.950 μs.

(3) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 4; 600 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;

MFM data transfer rate = 600 kb/s; ϕ_{CYA} = 62.5 ns, ϕ_{CYB} = 52.08 ns (19.2 MHz at XB1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	10.8			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	166.7			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	4			ϕ_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	104.2			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	208.3			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			10	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	64			ϕ_{CYB}	When external clock is input to XB1 pin.
Clock setup time at standby release	6	t_{CW}	32			ϕ_{CYB}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	32			ϕ_{CYB}	
INT response time from DMARQ ↓	7	t_{MI}	120		154	ϕ_{CYB}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			2	ϕ_{CYB}	

5

AC Characteristics 4; 600 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ active-low time	8	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ active-low time	8	t_{WDD}		208.3		ns	
DS0-DS3 setup time to $\overline{\text{DIR}}$	9	t_{DSD}	9.5			μs	Note 2
DIR setup time to $\overline{\text{STEP}}$	9	t_{DST}	0.5			μs	
DS0-DS3 hold time after $\overline{\text{STEP}}$	9	t_{STU}	2.5			μs	
$\overline{\text{STEP}}$ active-low time	9	t_{STP}	3	3.5	4	μs	
DS0-DS3 hold time after $\overline{\text{DIR}}$ (Note 1)	9	t_{DDS}	12			μs	
DIR hold time after $\overline{\text{STEP}}$	9	t_{STD}	22.5			μs	
$\overline{\text{STEP}}$ cycle time	9	t_{SC}	16.5			μs	
$\overline{\text{FLTR}}$ active-low time	10	t_{FR}	4		5	μs	
$\overline{\text{INDEX}}$ low time	10	t_{IDX}	8			ϕ_{CYB}	

Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 9.5 μs is actually 9.450 μs.

(3) See figure 1 for timing measurement voltage thresholds.

AC Characteristics 5; 300 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;

MFM data transfer rate = 300 kb/s; ϕ_{CYA} = 62.5 ns, ϕ_{CYB} = 52.08 ns (19.2 MHz at XB1)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	2	t_{AR}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	2	t_{RA}	0			ns	
$\overline{RD}$ pulse width	2	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↑	2	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	2	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	2	t_{RI}			400	ns	For data transfer in non-DMA mode
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	3	t_{AW}	0			ns	
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	3	t_{WA}	0			ns	
$\overline{WR}$ pulse width	3	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	3	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	3	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	3	t_{WI}			400	ns	For data transfer in non-DMA mode
DMARQ cycle time	4	t_{MCY}	21.7			μs	
$\overline{DMAAK}$ ↓ response time from DMARQ ↓	4	t_{MA}	333.3			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	4	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	4	t_{AA}	8			ϕ_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	4	t_{MR}	208.3			ns	
$\overline{WR}$ ↓ response time from DMARQ ↑	4	t_{MW}	416.7			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	4	t_{MRW}			20	μs	
TC pulse width	4	t_{TC}	60			ns	
RESET pulse width	5	t_{RST}	30			ϕ_{CYA}	
Clock hold time at standby	6	t_{WC}	128			ϕ_{CYB}	When external clock is input to XB1 pin.
Clock setup time at standby release	6	t_{CW}	64			ϕ_{CYB}	
START CLOCK command setup time to RESET STANDBY command	6	t_{WS}	64			ϕ_{CYB}	
INT response time from DMARQ ↓	7	t_{MI}	240		308	ϕ_{CYB}	
Time from INT to invalidate $\overline{DMAAK}$	7	t_{IA}			4	ϕ_{CYB}	

5

AC Characteristics 5; 300 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
$\overline{\text{RDATA}}$ active-low time	8	t_{RDD}	40			ns	
$\overline{\text{WDATA}}$ active-low time	8	t_{WDD}		416.7		ns	
DS0-DS3 setup time to $\overline{\text{DIR}}$	9	t_{DSD}	19			μs	Note 2
DIR setup time to $\overline{\text{STEP}}$	9	t_{DST}	1			μs	
DS0-DS3 hold time after $\overline{\text{STEP}}$	9	t_{STU}	5			μs	
$\overline{\text{STEP}}$ active-low time	9	t_{STP}	6	7	8	μs	
DS0-DS3 hold time after $\overline{\text{DIR}}$ (Note 1)	9	t_{DDS}	24			μs	
DIR hold time after $\overline{\text{STEP}}$	9	t_{STD}	45			μs	
$\overline{\text{STEP}}$ cycle time	9	t_{SC}	33			μs	
$\overline{\text{FLTR}}$ active-low time	10	t_{FR}	8		10	μs	
$\overline{\text{INDEX}}$ low time	10	t_{IDX}	16			ϕ_{CYB}	

Notes:

(1) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 19 μs is actually 18.950 μs.

(3) See figure 1 for timing measurement voltage thresholds.

Figure 2. Read Operation

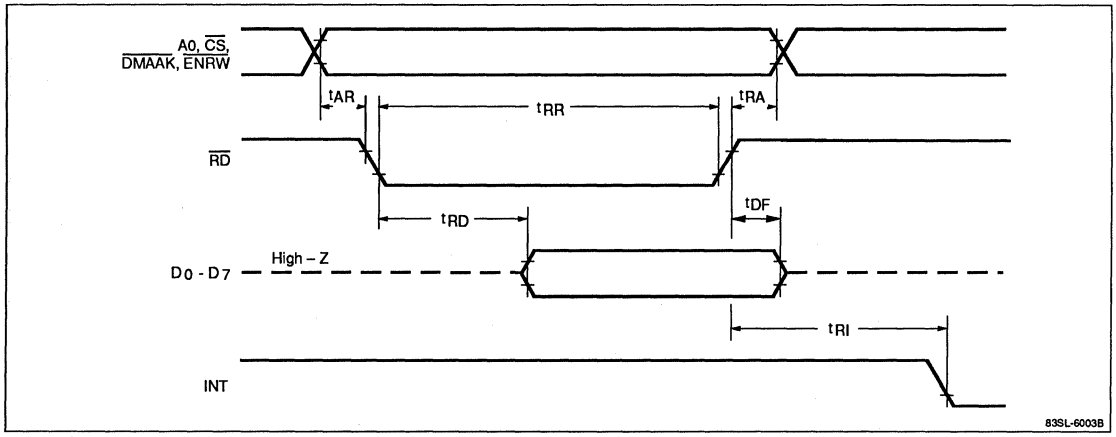

Figure 3. Write Operation

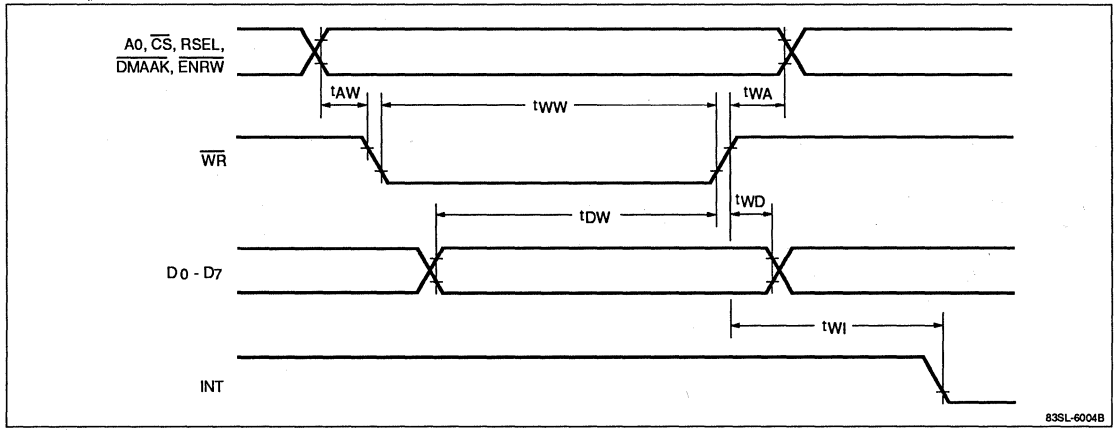

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Figure 4. DMA Operation

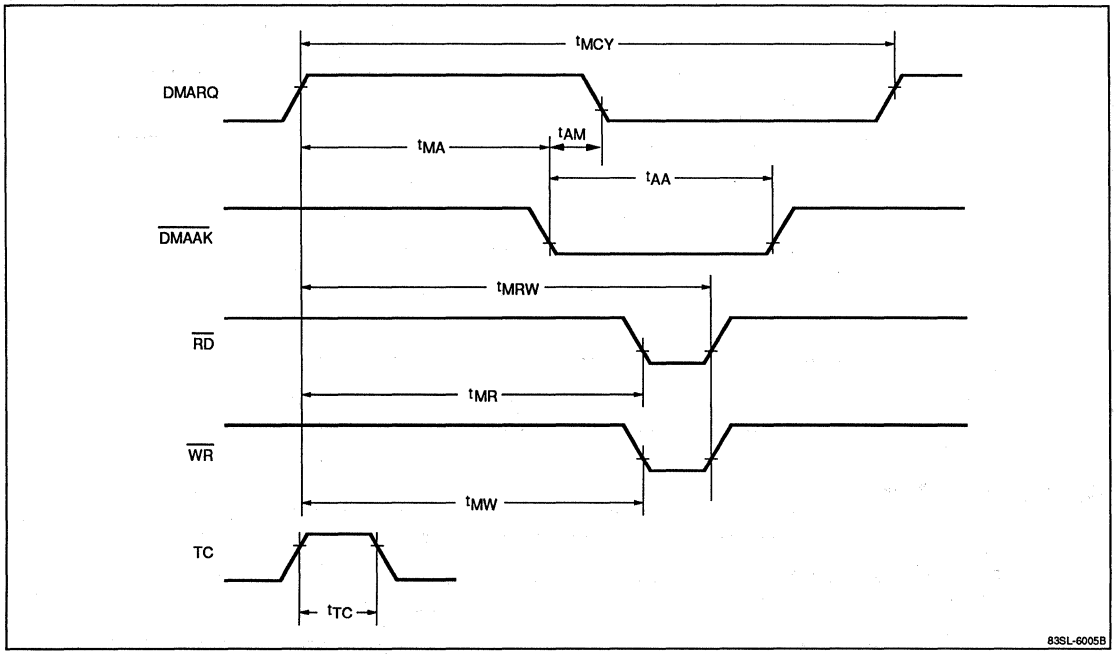


Figure 5. Reset Operattion

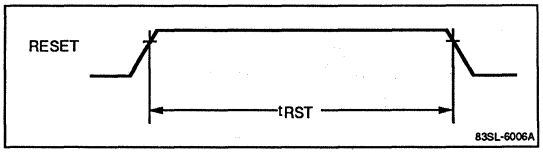
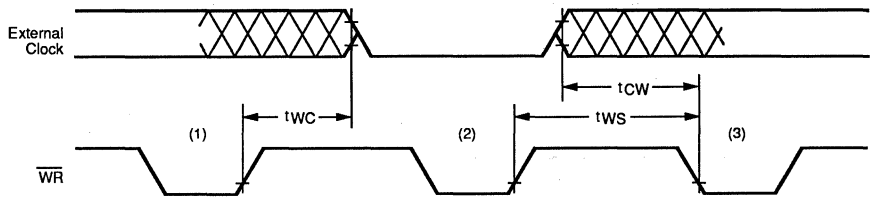


Figure. 6 Standby Operation



Notes:

(1) SET STANDBY command write.

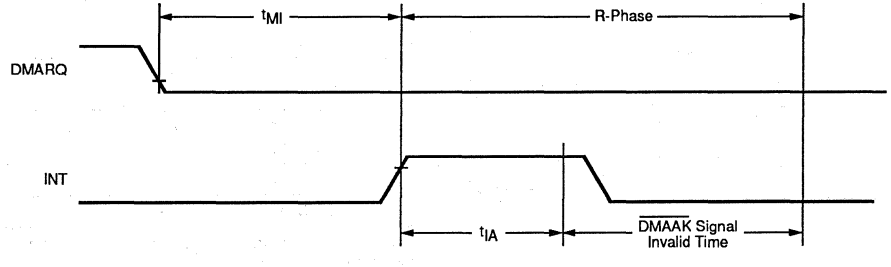
(2) START CLOCK command write.

(3) RESET STANDBY command write.

(4) When in standby mode the external clock should be fixed low. The standby current specifications cannot be met unless this is done.

83SL-6008B

Figure 7. Overrun Operation



INT generation on completion of command

83SL-6007B

Figure 8. RDATA and WDATA Waveforms

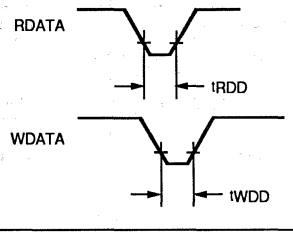


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Figure 9. Seek Operation

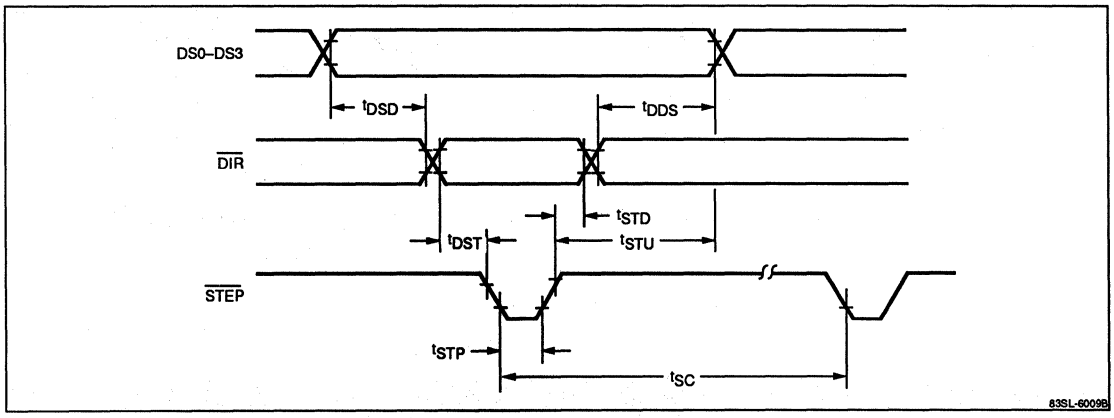
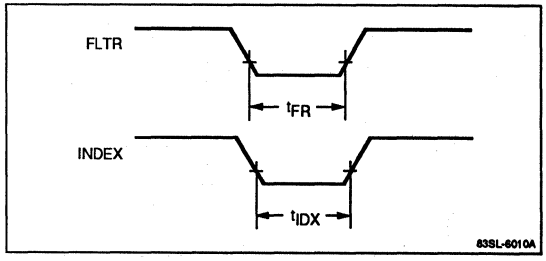


Figure 10. FLTR and INDEX Waveforms



μPD72067/68/69

Table 1 compares features of μPD72067, μPD72068, and μPDPD72069

Operation Modes

Table 2 describes the external, internal, and register modes of the μPD72069

Commands

Table 3 describes the 15 commands and 10 subcommands of the μPD72069.

Table 1. Feature Comparison, μPD72067/68/69

		μPD72067	μPD72068	μPD72069
FDD side external circuits built-in	Data sampling VFO	Digital PLL	Digital PLL	Analog PLL
	Write compensation	✓	✓	✓
	Motor control	✓	✓	✓
	Decoder	—	✓	✓
	Driver	—	✓	✓
Correspondence to high-speed data transmission		500 kb/s	500 kb/s	1.0 Mb/s
☆ CPU side external circuits built-in		—	✓	✓

☆ Circuits corresponding to IBM-PC (Address, DMARQ, and INT)

Table 2. Operation Modes

Mode	Function	Remarks
External	Sets the following parameters at the corresponding pins. • Data transmission speed • Write compensation value • Format (IBM/ECMA) • Motor control	Part of the programs of μPD765, 7265, 72065, and 72066 should be modified
Internal	Sets the following parameters using the corresponding commands (software). • Data transmission speed • Write compensation value • Format (IBM/ECMA) • Motor control	Part of the programs of μPD765, 7265, 72065, and 72066 should be modified.

Table 2. Operation Modes (cont)

Mode	Function	Remarks
Register	Corresponds to IBM-PC.	A dedicated CPU side interface is built-in An FDD select (DS0-DS3) stop function is built-in.

Table 3. Commands and Subcommands

Command Name	Function
Read Commands	
READ DATA	Specifies a sector and transfers its data to the host.
READ DELETED DATA	
READ ID	Reads a sector ID.
READ DIAGNOSTIC	Checks the track format.
SCAN EQUAL	Compares each sector data with host data and detects a sector that satisfies the set condition.
SCAN LOW OR EQUAL	
SCAN HIGH OR EQUAL	
Write Commands	
WRITE DATA	Specifies a sector and transfers its data to the host.
WRITE DELETED DATA	
WRITE ID	Writes the format of a track.
Seek Commands	
RECALIBRATE	Moves the read/write head to the outermost track (track 0).
SEEK	Moves the read/write head to the specified cylinder.
Sense Commands	
SENSE INTERRUPT STATUS	Reads the interrupt factor (seek end/state change) in the μPD72069.
SENSE DEVICE STATUS	Reads the FDD status.
Initialize Command	
SPECIFY	Defines a μPD72069 operation mode.
Subcommands	
SET STANDBY	Drives the μPD72069 in the standby status.
RESET STANDBY	Releases the μPD72069 from the standby status.
SOFTWARE RESET	Initializes the μPD72069.

Table 3. Commands and Subcommands (cont)

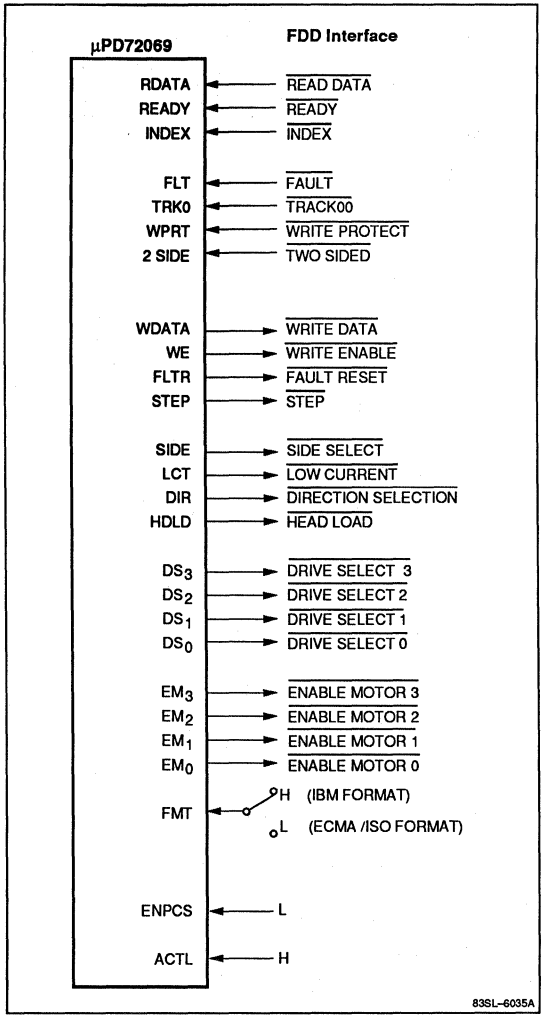
Command Name	Function
ENABLE EXTERNAL MODE	Sets the μPD72069 in External Mode.
CONTROL INTERNAL MODE	Sets the μPD72069 in Internal Mode and sets both data transmission rate and precompensation value.
ENABLE MOTORS	Control On/Off of the spindle motor.
SELECT FORMAT	Selects either IBM or ECMA/ISO format.
START CLOCK	Starts the clock generator operation.
DATA TRANSFER RATE	Sets a data transmission rate.
PRECOMPENSATION	Sets a precompensation value.

5

Interface With FDD

Figure 11 is a reference circuit diagram of the direct connections between the μPD72069 and a floppy-disk drive.

Figure 11. μPD72069 to FDD Interface



System Bus

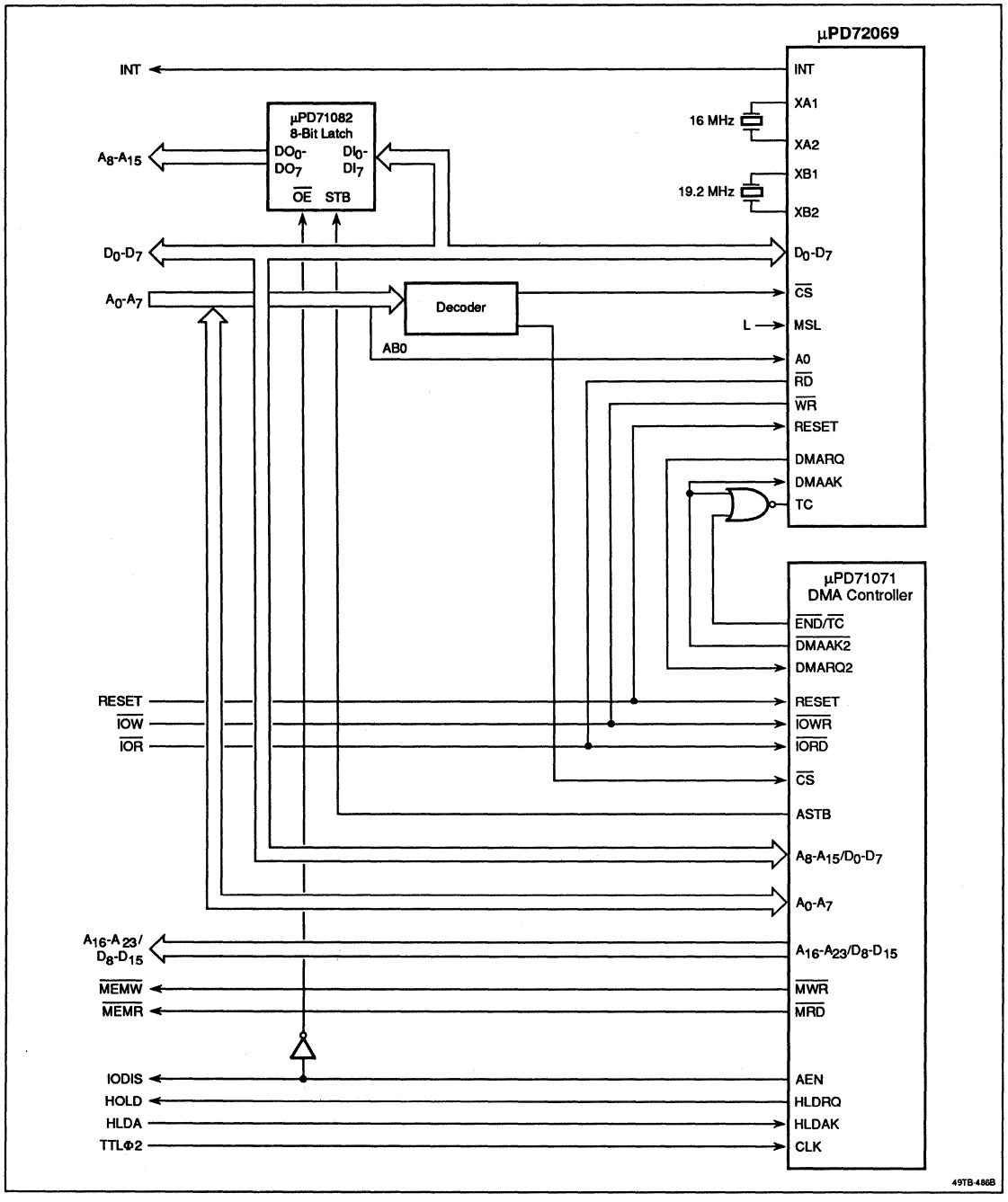
Table 4 lists the system clock XA or XB crystal appropriate for the selected floppy-disk drive

Figure 12 is a reference circuit diagram of the interface between the μPD72069 and a system bus for data transmission in Internal or External mode. To prevent misselection of I/O ports during DMA cycles, the Address Enable (AEN) output of μPD71071 inhibits other I/O ports.

Table 4. System Clock Frequencies

DR2-DR0	Mod Type	Data Rate (kb/s)	XA 16 MHZ	XB 19.2 MHz
000	FM	125	✓	—
	MFM	250	✓	—
001	FM	250	✓	—
	MFM	500	✓	—
010	FM	300	—	✓
	MFM	600	—	✓
011	FM	300	—	✓
	MFM	600	—	✓
100	FM	250	✓	—
	MFM	500	✓	—
101	FM	500	✓	—
	MFM	1 Mb/s	✓	—
110	FM	600	—	✓
111	FM	300	—	✓
	MFM	600	—	✓

Figure 12. μPD72069 to Host System Interface



HARD-DISK CONTROLLERS

Section 6
Hard-Disk Controllers

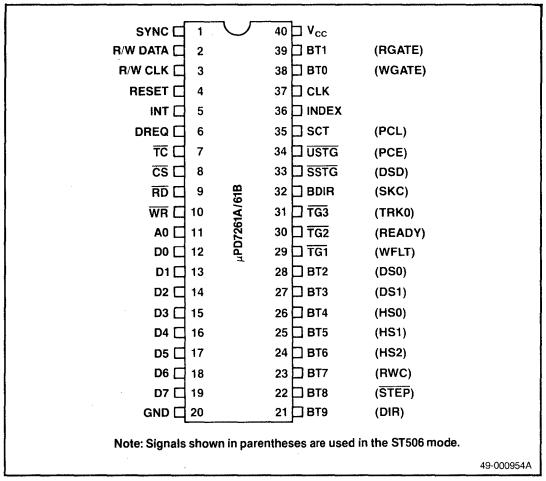
Description

The μPD7261A and μPD7261B hard-disk controllers are intelligent microprocessor peripherals designed to control a number of different types of disk drives. They are capable of supporting either hard-sector or soft-sector disks and provide all control signals that interface the controller with either SMD disk interfaces or ST506-type drives. The sophisticated instruction set minimizes the software overhead for the host microprocessor. By using the DMA controller, the microprocessor needs only to load a few command bytes into the μPD7261A/7261B and all the data transfers associated with read, write, or format operations are done by the μPD7261A/7261B and the DMA controller. Extensive error reporting, verify commands, ECC, and CRC data error checking assure reliable controller operation. The μPD7261A/7261B provides internal address mark detection, ID verification, and CRC or ECC checking and verification. An eight-byte FIFO is used for loading command parameters and obtaining command results. This makes the structuring of software drivers a simple task. The FIFO is also used for buffering data during DMA read/write operations.

Features

- ☐ Flexible interface to various types of hard disk drives
- ☐ Programmable track format
- ☐ Controls up to 8 drives in SMD mode; up to 4 drives in ST506-type mode
- ☐ Parallel seek operation capability
- ☐ Multi-sector and multi-track transfer capability
- ☐ Data scan and data verify capability
- ☐ High-level commands, including:
  Read Data, Read ID, Write Data, Format, Scan Data, Verify Data, Verify ID, Check, Seek (normal or buffered), Recalibrate (normal or buffered), Read Diagnostic (SMD only), Specify, Sense Interrupt Status, Sense Unit Status, and Detect Error
- ☐ NRZ or MFM data format
- ☐ Maximum R/W CLK frequency:
  — 12 MHz (7261A)
  — 18 MHz (7261B-18)
  — 23 MHz (7261B-23)
- ☐ Error detection and correction capability
- ☐ Simple I/O structure: compatible with most microprocessors
- ☐ All inputs and outputs except clock pins are TTL-compatible (clock pins require pullup)
- ☐ Data transfers under DMA control
- ☐ NMOS
- ☐ Single +5-volt power supply
- ☐ 40-pin ceramic DIP

Pin Configuration



Note: Signals shown in parentheses are used in the ST506 mode.

49-000954A

Ordering Information

Device Number	Package Type	Max Freq. of Operation
μPD7261AD	40-pin ceramic DIP	12 MHz
μPD7261BD-18	40-pin ceramic DIP	18 MHz
μPD7261BD-23	40-pin ceramic DIP	23 MHz

Pin Identification

No.	Symbol	Function
Host Interface		
4	RESET	Reset input
5	INT	Interrupt request output
6	DREQ	DMA request output
7	$\overline{TC}$	Terminal count input
8	$\overline{CS}$	Chip select input
9	$\overline{RD}$	Read strobe input
10	$\overline{WR}$	Write strobe input
11	A_0	Register select input
12–19	D_0–D_7	Data I/O bus
20	GND	Ground
37	CLOCK	External clock input
40	V_{CC}	+5 V power supply
SMD Interface		
1	SYNC	PLL synchronization output
2	R/W DATA	Read/write data I/O
3	R/W CLK	Read/write clock input

6

Pin Identification (cont)

No.	Symbol	Function
SMD Interface (cont)		
21-28, 38, 39	BT9-BT0	Bit 9-0 outputs / Status inputs
29-31	$\overline{TG1}$-$\overline{TG3}$	Tag 1-3 output
32	BDIR	Bit direction output
33	$\overline{SSTG}$	SR select tag output
34	$\overline{USTG}$	Unit select tag output
35	SCT	Sector input
36	INDEX	Sector zero input
ST506-Type Interface		
1	SYNC	PLL lock / Read clock enable output
2	R/W DATA	Read / write data I / O
3	R/W CLK	Read / write clock input
21	DIR	Direction in output
22	$\overline{STEP}$	Step pulse output
23	RWC	Reduced write current output
24-26	HS2-HS0	Head select outputs 2-0
27, 28	DS1, DS0	Drive select outputs 1, 0
29	WFLT	Write fault input
30	READY	Ready input
31	TRK0	Track zero input
32	SKC	Seek complete input
33	DSD	Drive selected input
34	PCE	Precomp early output
35	PCL	Precomp late output
36	INDEX	Index input
38	WGATE	Write gate output
39	RGATE	Read gate output

Pin Functions—Host Interface

RESET (Reset)

When the RESET input is pulled high, it forces the device into an idle state. The device remains idle until a command is issued to the system.

INT (Interrupt Request)

The μPD7261A/7261B pulls the INT output high to request an interrupt.

DREQ (DMA Request)

The μPD7261A/7261B pulls the DREQ output high to request a DMA transfer between the disk controller and the memory.

$\overline{TC}$ (Terminal Count)

The $\overline{TC}$ input goes low to signal the final DMA transfer.

$\overline{CS}$ (Chip Select)

When the $\overline{CS}$ input is low, it enables reading from or writing to the register selected by A_0.

$\overline{RD}$ (Read Strobe)

When the $\overline{RD}$ strobe is low, data is read from the selected register.

$\overline{WR}$ (Write Strobe)

When the $\overline{WR}$ input is low, data is written to the selected register.

A_0 (Register Select)

The A_0 input is connected to a non-multiplexed address bus line. When A_0 is high, it selects the command or status register. When it is low, it selects the data buffer.

D_0-D_7 (Data Bus)

D_0-D_7 are connected to the system data bus.

CLOCK (Clock)

The CLOCK input is the timing clock for the on-chip processor.

Pin Functions—SMD Interface

SYNC (PLL Synchronization)

This output goes high after the read gate signal (BT1 when $\overline{TG3} = 0$) is high and a given number of bytes (GPL2-2) has elapsed.

R/W DATA (Read/Write Data)

The R/W DATA pin outputs the write data to the drive, and inputs the read data from the drive.

R/W CLK (Read/Write Clock)

R/W CLK is the input for the read and write clocks.

BT9-BT0 (Bit 9-0)

BT9-BT0 output the bit signals, bit 9-0. The bit 9-0 outputs send cylinder and unit addresses to the drives. BT9-BT2 also act as inputs for status signals from the drives as shown in table 1.

Table 1. Bit and Control Information

No.	Bit	Control
21	BT9	Unit Selected
22	BT8	Seek End
23	BT7	Write Protected
24	BT6	
25	BT5	Unit Ready
26	BT4	On Cylinder
27	BT3	Seek Error
28	BT2	Fault

BT7-BT2 also read the device status 2 (SR7-SR2) and device type (DT7-DT2). The index and SCT pins read SR0, SR1 and DT0, DT1.

BDIR (Bit Direction)

The BDIR output determines whether pins 28-21 will output BT2-BT9 or input drive status signals.

$\overline{TG3}$-$\overline{TG1}$ (Tag 3-1)

The $\overline{TG}$ outputs define the use of the BT pins. When $\overline{TG1}$ is low, BT9-BT0 output the cylinder address. When $\overline{TG2}$ is low, BT7-BT0 select a head address. When $\overline{TG3}$ is low, BT9-BT0 output control signals for the disk drive.

$\overline{SSTG}$ (SR Select Tag)

When the $\overline{SSTG}$ output is low, BT7-BT2, INDEX and SCT will be inputting SR7-SR0 or DT7-DT0.

$\overline{USTG}$ (Unit Select Tag)

When the $\overline{USTG}$ output is low, BT4-BT2 will be outputting a unit address.

INDEX (Index)

The INDEX input goes high when the drive detects an index mark. INDEX also acts as the SR0 and DT0 input pin.

SCT (Sector)

The SCT input goes high when the drive detects a sector mark. SCT also acts as the SR1 and DT1 input pin.

Pin Functions — ST506-Type Interface

SYNC (Read Clock Enable)

SYNC indicates that a sync pattern has been detected and that synchronization has been achieved.

R/W DATA (Read/Write Data)

The R/W DATA pin outputs the write data to the drive, and inputs the read data from the drive.

R/W CLK (Read/Write Clock)

R/W CLK is the input for the read and write clocks.

DIR (Direction In)

The DIR output determines the direction the read/write head will move in when it receives a step pulse. DIR high will cause the head to move inward, DIR low will move the head outward.

$\overline{STEP}$ (Step Pulse)

$\overline{STEP}$ outputs the head step pulses.

RWC (Reduced Write Current)

The RWC output signals that the read/write head of the disk drive has selected a cylinder address larger than that specified in the SPECIFY command. This signal is used to reduce the write current.

HS2-HS0 (Head Select 2-0)

The HS2-HS0 outputs select the head. Up to 8 read/write heads can be selected per drive.

DS1, DS0 (Drive Select 1,0)

The DS1 and DS0 outputs select one of up to 4 drives.

WFLT (Write Fault)

The WFLT input detects write faults.

READY (Ready)

The READY input detects the drive's ready state.

TRK0 (Track 0)

The TRK0 input signals that the head is at track 0.

SKC (Seek Complete)

The SKC input signals that a seek is complete.

DSD (Drive Selected)

The DSD input signals that the drive is selected.

PCE (Precomp Early)

When the PCE output is high, early write precompensation is required.

PCL (Precomp Late)

When the PCL output is high, late write precompensation is required.

INDEX (Index)

The INDEX input goes high when the drive detects the index mark.

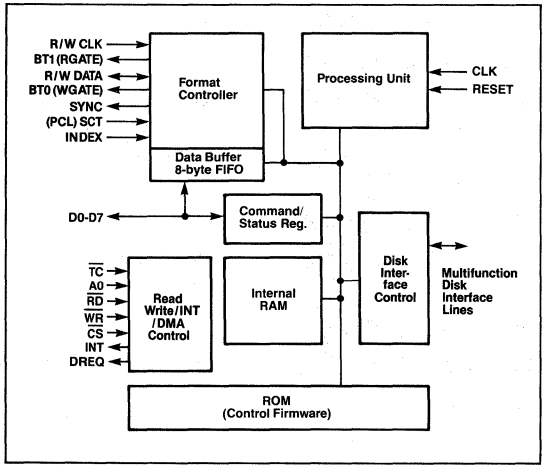
WGATE (Write Gate)

WGATE output goes high when the μPD7261A/7261B is writing data.

RGATE (Read Gate)

The RGATE output goes high when the μPD7261A/7261B is reading from the disk.

Block Diagram



Absolute Maximum Ratings

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin with respect to ground, V_{CC}	−0.5 to +7.0 V*
Input voltage, V_I	−0.5 to +7.0 V*
Output voltage, V_O	−0.5 to +7.0 V*

Comment: Exposing the device to stresses above those listed in the Absolute Maximum Ratings could cause permanent damage. The device should not be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_A = 25°C

DC Characteristics

*μPD7261B specifications are preliminary

T_A = 0 to +70°C, V_{CC} = +5.0 V ± 10% unless otherwise specified

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL1}	−0.5		+0.8	V	All except CLK, R/W CLK
Input voltage low	V_{IL2}	−0.5		+0.6	V	CLK, R/W CLK
Input voltage high	V_{IH1}	+2.0		V_{CC} +0.5	V	All except CLK, R/W CLK
Input voltage high	V_{IH2}	+3.3		V_{CC} +0.5	V	CLK, R/W CLK
Output voltage low	V_{OL}			+0.45	V	I_{OL} = +2.0 mA
Output voltage high	V_{OH1}	+2.4			V	I_{OH} = −100 μA, all except pins 21–34
Output voltage high	V_{OH2}	+2.4			V	I_{OH} = −50 μA, pins 21–34
Input leakage current	I_{LI1}			±10	μA	V_{IN} = V_{CC} to 0.45 V, all except pins 21–34
Input leakage current	I_{LI2}			−500 (7261A)	μA	V_{IN} = V_{CC} to 0.45 V; pins 21–34
				−700 (7261B)	μA	
Output leakage current	I_{LO}			±10	μA	V_{OUT} = V_{CC} to 0.45 V
Supply current	I_{CC}		250	320	mA	

Capacitance

T_A = 25°C, V_{CC} = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			15	pF	(Note 1)
Output capacitance	C_{OUT}			15	pF	(Note 1)
Input / Output capacitance	$C_{I/O}$			20	pF	(Note 1)

Note:

(1) f = 1 MHz, All unmeasured pins tied to GND.

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; $C_L = 100$ pF (50 pF for 7261B-23)

Parameter	Symbol	Limits 7261A Min	7261A Max	7261B-18 Min	7261B-18 Max	7261B-23 Min	7261B-23 Max	Unit	Test Conditions
Processor Interface									
Clock cycle	t_{CY}	83		55		43		ns	
Clock time, low	t_{CL}	30		20		15		ns	
Clock time, high	t_{CH}	30		20		17		ns	
Clock rise time	t_{CR}		10		10		10	ns	
Clock fall time	t_{CF}		10		10		10	ns	
A_0, $\overline{CS}$ setup to $\overline{RD}$	t_{AR}	0		0		0		ns	
A_0, $\overline{CS}$ hold from $\overline{RD}$	t_{RA}	0		0		0		ns	
$\overline{RD}$ pulse width	t_{RR}	200		100		100		ns	
Data delay from $\overline{RD}$	t_{RD}		150		85		85	ns	
Output float delay	t_{RDF}	0	100	0	75	0	75	ns	
Data delay from A_0, $\overline{CS}$	t_{AD}		150		85		85	ns	
A_0, $\overline{CS}$ setup to $\overline{WR}$	t_{AW}	0		0		0		ns	
A_0, $\overline{CS}$ hold from $\overline{WR}$	t_{WA}	0		0		0		ns	
$\overline{WR}$ pulse width	t_{WW}	200		100		100		ns	
Data setup to $\overline{WR}$	t_{DW}	100		55		55		ns	
Data hold from $\overline{WR}$	t_{WD}	5		5		5		ns	
Recovery time from $\overline{RD}$, $\overline{WR}$	t_{RV}	200		70		70		ns	
Reset pulse width	t_{RES}	100		100		100		t_{CY}	
$\overline{TC}$ pulse width	t_{TC}	100		100		80		ns	
INT delay from $\overline{WR}$ ↑	t_{WI}		200		200		200	ns	
DREQ delay from $\overline{WR}$ ↑	t_{WRQ}		250		125		125	ns	
DREQ delay from $\overline{RD}$ ↑	t_{RRQ1}		250		160		160	ns	During disk read operation
DREQ delay from $\overline{RD}$ ↓	t_{RRQ2}		150		130		100	ns	After disk read operation
ST506-Type Interface									
R/W CLK cycle period	t_{RWCY}	83		83		83		ns	
R/W CLK time, low	t_{RWCL}	30		30		30		ns	
R/W CLK time, high	t_{RWCH}	30		30		30		ns	
R/W CLK rise time	t_{RWCR}		10		10		10	ns	
R/W CLK fall time	t_{RWCF}		10		10		10	ns	
R/W DATA setup to R/W CLK	t_{RDRC}	40		35		35		ns	
R/W DATA hold from R/W CLK	t_{RCRD}	5		5		5		ns	
R/W DATA delay from R/W CLK	t_{WCWD}	35	90	10	60	10	60	ns	
RGATE delay from R/W CLK	t_{RCRG}		300		300		300	ns	
WGATE delay from R/W CLK	t_{WCWG}		150		150		150	ns	
PCE / PCL delay from R/W CLK	t_{RWCPC}	35	110	10	80	10	80	ns	
SYNC delay from R/W CLK	t_{RWCSY}		150		150		150	ns	

6

AC Characteristics (cont)

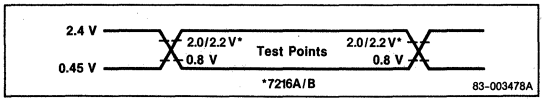
Parameter	Symbol	Limits 7261A Min	7261A Max	7261B-18 Min	7261B-18 Max	7261B-23 Min	7261B-23 Max	Unit	Test Conditions
ST506-Type Interface (cont)									
DS0, DS1 setup to $\overline{STEP}$	t_{DSST}	250		250		250		t_{CY}	Normal seek mode
DIR setup to $\overline{STEP}$	t_{DIST}	200		200		200		t_{CY}	
$\overline{STEP}$ pulse width	t_{STEP}	69	85	69	85	69	85	t_{CY}	
DS0, DS1 hold from $\overline{STEP}$	t_{STDS}	750		750		750		t_{CY}	Normal seek mode; polling mode
DIR hold from $\overline{STEP}$	t_{STDI}	750		750		750		t_{CY}	
DS0, DS1 hold from SKC	t_{SKDS}	100		100		100		t_{CY}	Normal seek mode; nonpolling
DIR hold from SKC	t_{SKDI}	100		100		100		t_{CY}	
DS0, DS1 setup to $\overline{STEP}$	t_{DSSTB}	250		250		250		t_{CY}	Buffered seek mode
DIR setup to $\overline{STEP}$	t_{DISTB}	200		200		200		t_{CY}	
$\overline{STEP}$ pulse width	t_{STEPB}	69	85	69	85	69	85	t_{CY}	
$\overline{STEP}$ cycle period	t_{STCY}	500	660	500	660	500	660	t_{CY}	
DS0, DS1 hold from $\overline{STEP}$	t_{STDSB}	200		200		200		t_{CY}	Buffered seek mode; polling mode
DIR hold from $\overline{STEP}$	t_{STDIB}	200		200		200		t_{CY}	
DS0, DS1 hold from SKC	t_{SKDSB}	100		100		100		t_{CY}	Buffered seek mode; nonpolling
DIR hold from SKC	t_{SKDIB}	100		100		100		t_{CY}	
Index pulse width	t_{IDXF}	8		8		8		t_{RWCY}	
SMD Interface									
R/W CLK cycle period	t_{RWCY}	83		55		43		ns	
R/W CLK time, low	t_{RWCL}	30		20		15		ns	
R/W CLK time, high	t_{RWCH}	30		20		17		ns	
R/W CLK rise time	t_{RWCR}		10		10		10	ns	
R/W CLK fall time	t_{RWCF}		10		10		10	ns	
R/W DATA setup to R/W CLK	t_{RDRC}	40		35		35	ns		
R/W DATA hold from R/W CLK	t_{RCRD}	5		5		5		ns	
R/W DATA delay from R/W CLK	t_{WCWD}	35	90	10	60	10	50	ns	
BT1 delay from R/W CLK	t_{RCRG}		300		300		300	ns	
BT0 delay from R/W CLK	t_{WCWG}		150		150		150	ns	
SYNC delay from R/W CLK	t_{RWCSY}		150		150		150	ns	
BDIR setup to $\overline{USTG}$	t_{BDUT}	60		60		60		t_{CY}	Unit select operation
BDIR hold from $\overline{USTG}$	t_{UTBD}	15		15		15		t_{CY}	
Unit ADR setup to $\overline{USTG}$	t_{UAUT}	38	52	38	52	38	52	t_{CY}	
Unit ADR hold from $\overline{USTG}$	t_{UTUA}	15		15		15		t_{CY}	
BDIR setup to $\overline{TG1}$	t_{BDT1}	27	48	27	48	27	48	t_{CY}	Cylinder select operation
BDIR hold from $\overline{TG1}$	t_{T1BD}	60		60		60		t_{CY}	

AC Characteristics (cont)

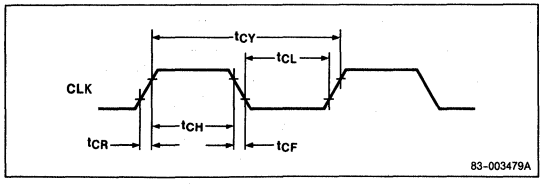
Parameter	Symbol	Limits						Unit	Test Conditions
		7261A		7261B-18		7261B-23			
		Min	Max	Min	Max	Min	Max		
SMD Interface (cont)									
CYL. ADR setup to $\overline{TG1}$	t_{CAT1}	27	48	27	48	27	48	t_{CY}	Cylinder select operation
CYL. ADR hold from $\overline{TG1}$	t_{T1CA}	24		24		24		t_{CY}	
$\overline{TG1}$ pulse width	t_{TG1}	24	36	24	36	24	36	t_{CY}	
BDIR setup to $\overline{TG2}$	t_{BDT2}	15		15		15		t_{CY}	Head select operation
BDIR hold from $\overline{TG2}$	t_{T2BD}	70		70		70		t_{CY}	
HEAD ADR setup $\overline{TG2}$	t_{HAT2}	15	70	15	70	15	70	t_{CY}	
HEAD ADR hold from $\overline{TG2}$	t_{T2HA}	24		24		24		t_{CY}	
$\overline{TG2}$, pulse width	t_{TG2}	24	36	24	36	24	36	t_{CY}	
BDIR setup to $\overline{TG3}$	t_{BDT3}	24		24		24		t_{CY}	RT2, FAULT CLR, SERVO, DATA STB control timing
BDIR hold from $\overline{TG3}$	t_{T3BD}	24	36	24	36	24	36	t_{CY}	
$\overline{TG3}$, pulse width	t_{TG3}	56	100	56	100	56	100	t_{CY}	
$\overline{BT2}$, 3, 4, 6, 7, 8 setup to $\overline{TG3}$	t_{BTT3}		56		56		56	t_{CY}	
BT4, 6 hold from $\overline{TG3}$	t_{T3BT1}	24		24		24		t_{CY}	
BT2, 3, 7, 8 hold from $\overline{TG3}$	t_{T3BT2}	75		75		75		t_{CY}	
BDIR delay from $\overline{SSTG}$	t_{STBD}	24		24		24		t_{CY}	Sense unit status timing
BDIR high time	t_{BDIR}	54	66	54	66	54	66	t_{CY}	
BT9 setup to BDIR	t_{BTBD}	38	52	38	52	38	52	t_{CY}	
BT9 hold from BDIR	t_{BDBT}	24	33	24	33	24	33	t_{CY}	
$\overline{SSTG}$ pulse width	t_{SSTG}		370		370		370	t_{CY}	
Index pulse width	t_{IDXH}	8		8		8			
SCT pulse width	t_{SCT}	8		8		8			

Timing Waveforms—Host System Interface

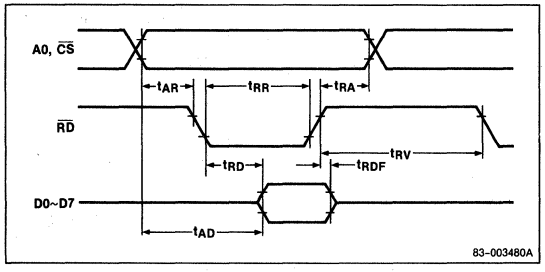
AC Test Points (Except R/W CLK, CLK)



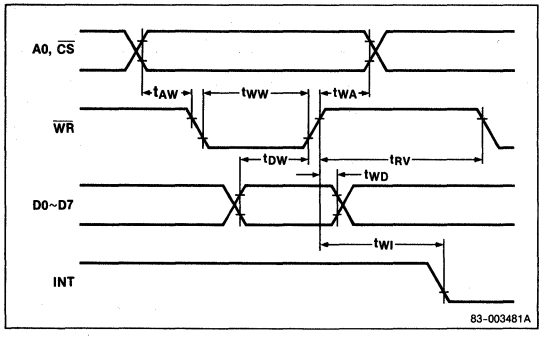
CLK Waveform



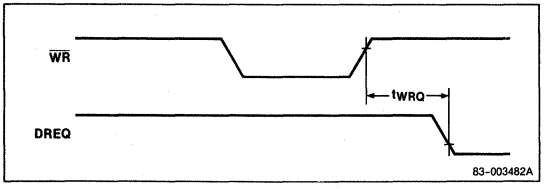
Read Timing



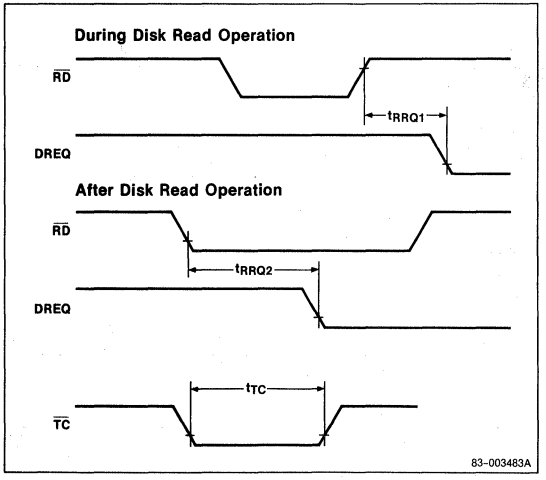
Write Timing



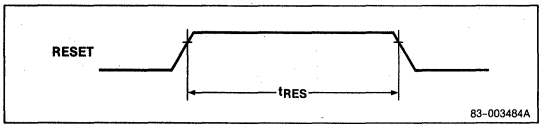
DMA Write Timing



DMA Read Timing

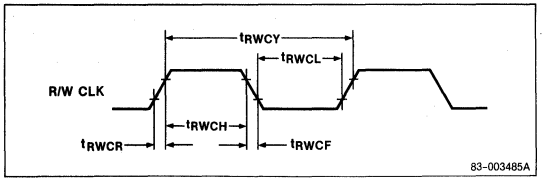


Reset Waveform

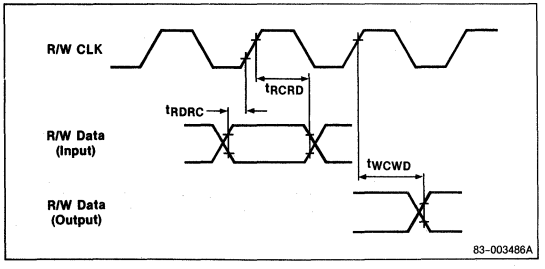


Timing Waveforms—SMD Interface

R/W CLK Waveform

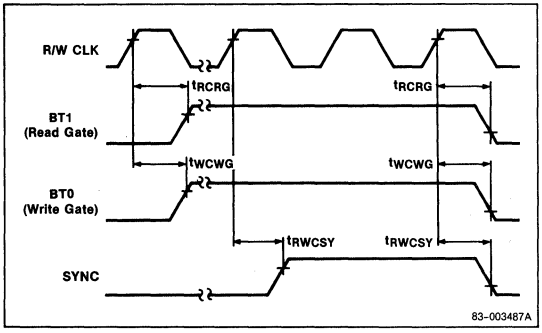


Data Read/Write Timing

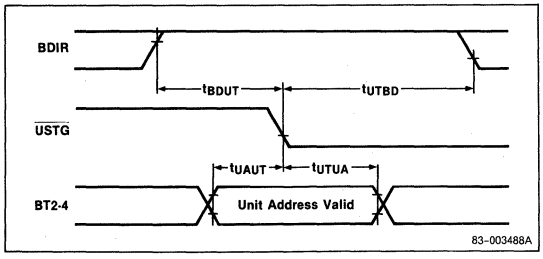


Timing Waveforms—SMD Interface (cont)

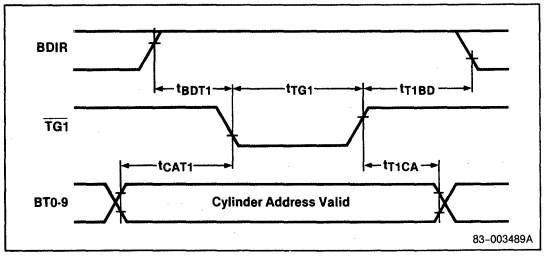
Read/Write Timing



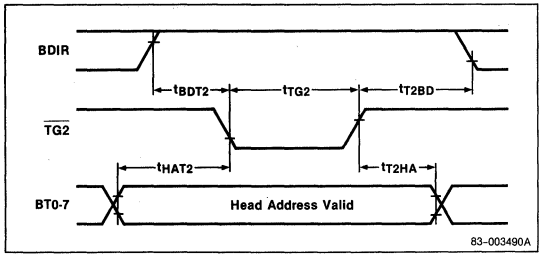
Unit Select Timing



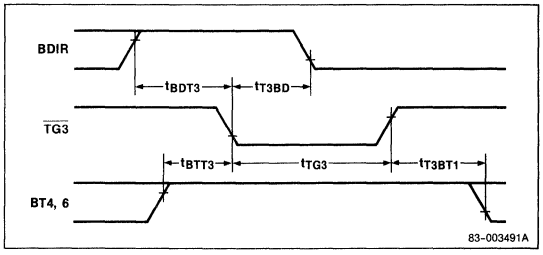
Seek Timing



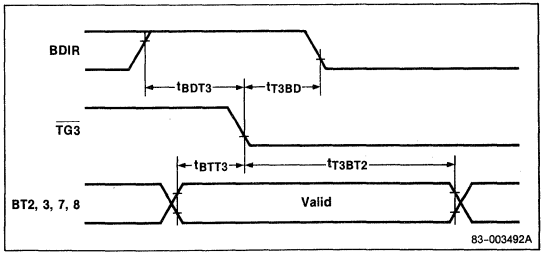
Head Select Timing



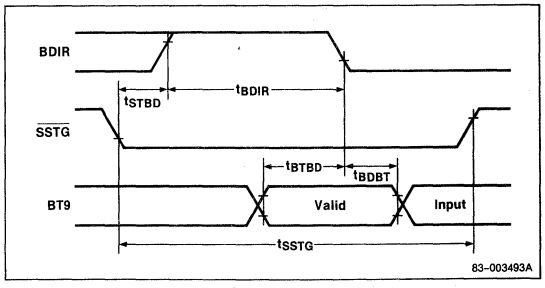
Bit Bus Timing, Fault Clear/Return-to-Zero



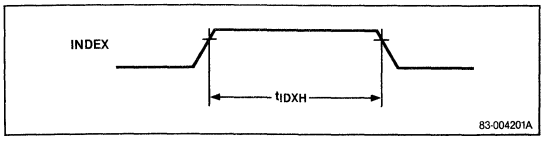
Bit Bus Timing, Servo Offset/Data Strobe



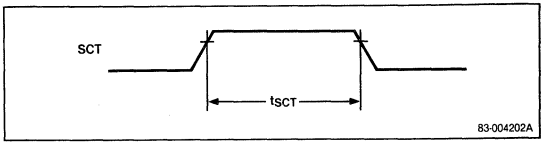
Bit Bus 9 Timing



Index Waveform



Sector Waveform



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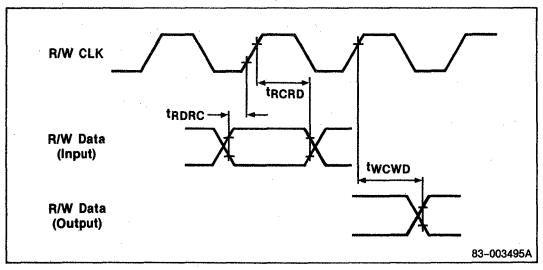
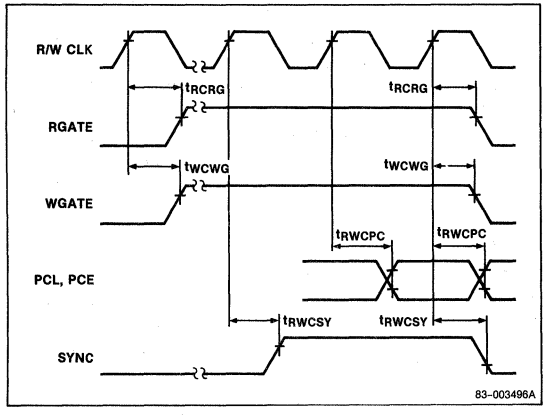
Timing Waveforms—ST506-Type Interface

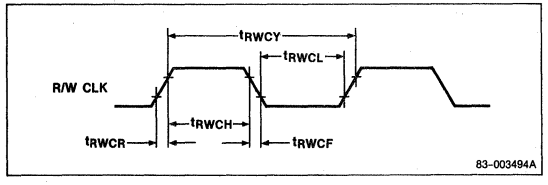
Data Read/Write Operation



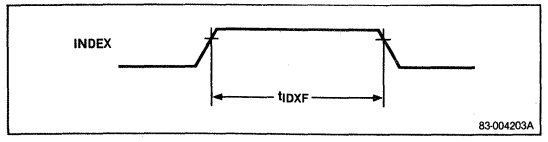
Read/Write Operation



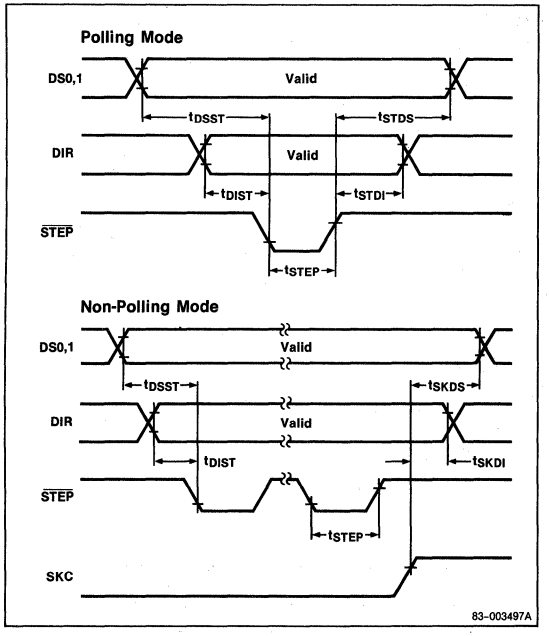
R/W CLK Waveform



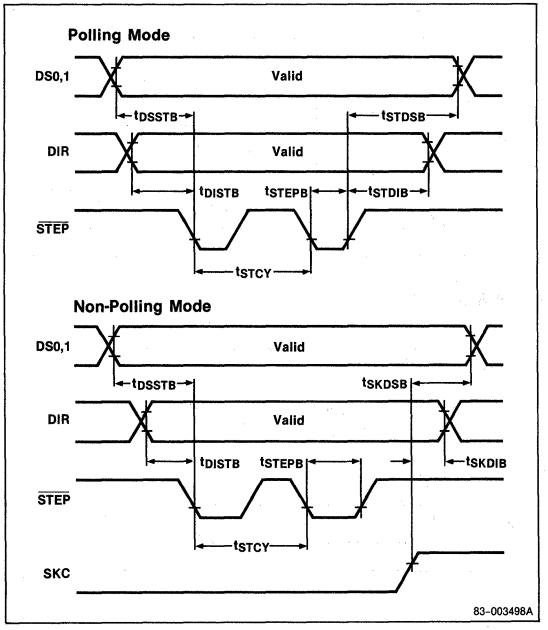
Index Waveform



Normal Seek Operation

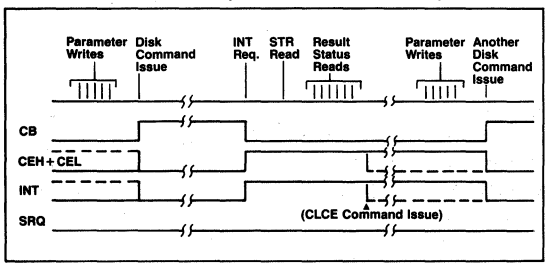


Buffered Seek Operation

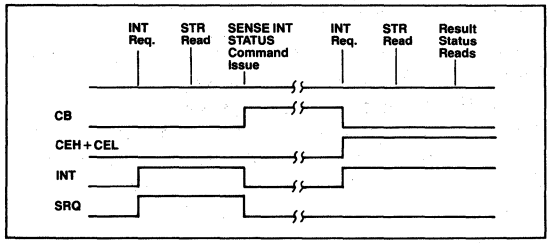


Timing Waveforms—ST506-Type Interface (cont)

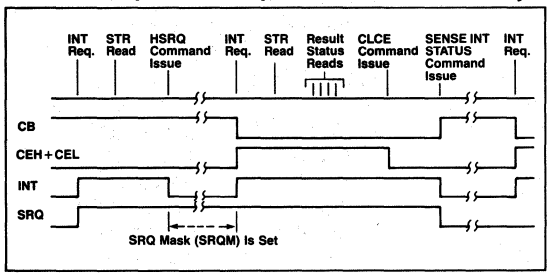
Read/Write Sequence (Disk Command Issue)



Sense Interrupt Status Request When Controller Not Busy



Sense Interrupt Status Request When Controller Busy



High-Level Commands

Specify

Allows user to select SMD or ST506-type mode data block length, ending track number, end sector number, gap length, track at which write current is reduced, ECC or CRC function, choice of polynomial, and polling mode enable.

Sense Interrupt Status

When a change of disk status occurs, the HDC will interrupt the host CPU. This command will reveal the cause of interrupt, such as seek end, disk ready change, seek error, or equipment check. The disk unit address is also supplied.

Sense Unit Status

The host CPU specifies the drive numbers and the HDC will return information such as write fault, ready, track 000, seek complete and drive selected, or for SMD units fault, seek error, on cylinder, unit ready, AM found, write protected, seek end, and unit selected.

Detect Error

Used after a read operation where ECC has been employed. The detect error command supplies the information needed to allow the host CPU to execute an error correction routine. (Only allowed when an actual correctable error is detected by the HDC.)

Recalibrate

Returns the disk drive heads to the home position or track 000 position. Has four modes of operation: SMD, normal, buffered, or nonpolling.

Seek

Moves the disk drive heads to the specified cylinder. As in recalibrate, seek has four modes of operation.

Format

This command is used to initialize the medium with the desired format which includes various gap lengths, data patterns, and CRC codes. This command is used in conjunction with the specify command.

Verify ID

Used to verify the ID bytes with data from memory. Performs the operation over a specified number of sectors.

Read ID

Used to verify the position of the read/write heads.

Read Diagnostic

Used in SMD mode only, the command allows the programmer to read a sector of data even if the ID portion of the sector is defective. Only one sector at a time can be read.

Read Data

Reads and transfers to the system memory the number of sectors specified. The HDC can read multiple sectors and multiple tracks with one instruction.

Scan

Compares a specified block of memory with specified sectors on the disk. The 7261A/7261B continues until a sector with matching data is found, until the sector count reaches zero, or the end of the cylinder is reached.

Verify Data

Makes a sector-by-sector comparison of data in the system memory by DMA transfer. As in read operation, multiple sectors and tracks may be verified with this commmand.

Write Data

Data from the system memory, transferred by DMA, is written onto the specified disk unit. As in the read command, data may be written onto successive sectors and tracks.

Auxiliary Command

Allows four additional functions to be executed: software reset, clear data buffer, mask interrupt request bit (masks interrupts caused by change of status of drives), and reset interrupt caused by command termination (used when no further disk commands will be issued, which would normally reset the interrupt).

Command Operation

There are three phases for most of the instructions that the μPD7261A/7261B can execute: command phase, execution phase, and result phase. During the command phase the host CPU loads preset parameters into the μPD7261A/7261B FIFO via the data bus and by successive write pulses to the part with A_0 and CS true low. Once the required parameter bytes are loaded the appropriate command is initiated by issuing a write pulse with A_0 high and CS low and the command code on the data bus.

The μPD7261A/7261B is now in the execution phase. This can be verified by examining the status register bit 7 (the controller busy bit). The execution phase is ended when a normal termination or an abnormal termination occurs. An abnormal termination can occur due to a read or write error, or a change of status in the addressed disk drive. A normal termination occurs when the command given is correctly completed. (This is indicated by bits in the status register.) The result phase is then entered. The host CPU may read various result parameters from the FIFO. These result parameters may be useful in determining the cause of an interrupt, or the location of a sector causing a read error, for example.

The chart shown in table 2 illustrates the preset parameters and result parameters that are associated with each command. The abbreviations are defined at the end of table 2.

Table 2. Preset Parameters and Result Status Byte

Disk Command	Command Code	Preset Parameters/Result Status 1st	2nd	3rd	4th	5th	6th	7th	8th
Detect error	0100X								
		EADH	EADL	EPT1	EPT2	EPT3			
Recalibrate	0101[B]								
		IST*							
Seek	0110[B]	PCNH	PCNL						
		IST*							
Format	0111(S)	PHN	(PSN)	SCNT	DPAT	GPL1	[GPL3]		
		EST	SCNT						
Verify ID	1000(S)	PHN	(PSN)	SCNT					
		EST	SCNT						
Read ID	1001(S)	PHN	(PSN)	SCNT					
		EST	SCNT						
(Read diagnostic)	1010X	PHN	PSN						
		EST							
Read data	1011X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Check	1100X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Scan	1101X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Verify data	1110X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Write data	1111X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Sense interrupt status	0001X	IST							
Specify	0010X	MODE	DTLH	DTLL	ETN	ESN	GPL2	(MGPL1) [RWCH]	[RWCL]
Sense unit status	0011X								
		UST							

Note:
( ): These are omitted for soft-sector disks.
[ ]: These are omitted for hard-sector disks.
*: IST available as a result byte only when in nonpolling mode.
B: Indicates buffered mode when set.
S: Indicates Skewed mode (SMD only) when set.
X: Indicates don't care.

Mnemonic Definitions

EADH Error address, high byte
EADL Error address, low byte
EPT1 Error pattern, byte one
EPT2 Error pattern, byte two
EPT3 Error pattern, byte three
PCNH Physical cylinder number, high byte

Mnemonic Definitions (cont)

PCNL Physical cylinder number, low byte
PHN Physical head number
PSN Physical sector number
SCNT Sector count
DPAT Data pattern
GPL1 Gap length one
GPL3 Gap length three
EST Error status byte
FLAG Flag byte
LCNH Logical cylinder number, high byte

Mnemonic Definitions (cont)

LCNL	Logical cylinder number, low byte
LHN	Logical head number
LSN	Logical sector number
IST	Interrupt status byte
MODE	Mode
DTLH	Data length, high byte
DTLL	Data length, low byte
ETN	Ending track number
ESN	Ending sector number
GPL2	Gap length two
RWCL	Write current cylinder, low byte
RWCH	Write current cylinder, high byte
UST	Unit status byte
MGPL1	Modified gap length 1

Status Register

This register is a read only register and may be read by asserting $\overline{RD}$ and $\overline{CS}$ with A_0 high. The status register may be read at any time. It is used to determine controller status and partial result status. See table 3.

Table 3. Status Register Bits

Pin No.	Pin Name	Function
D_7	CB (Controller busy)	Set by a disk command issue. Cleared when the command is completed. (This bit is also set by an external reset signal or an RST command, but will be cleared at the completion of the reset function.) When this bit is set, a new disk command will not be accepted.
D_6, D_5	CEH, CEL (Command end)	CEH = 0 and CEL = 0 A disk command is in process, or no disk command is issued after the last reset signal or the last CLCE auxiliary command. Both the CEH and CEL bits are cleared by a disk command, a CLCE auxiliary command, or a reset signal.
		CEH = 0 and CEL = 1 Abnormal termination of a disk command. Execution of a disk command was started, but was not successfully completed.
		CEH = 1 and CEL = 0 Normal termination of a disk command. The execution of a disk command was completed and properly executed.
		CEH = 1 and CEL = 1 Invalid command issue.

Table 3. Status Register Bits (cont)

Pin No.	Pin Name	Function
D_4	SRQ (Sense interrupt status request)	When a seek end, an equipment check condition, or a ready signal state change is detected, this bit is set requesting a sense interrupt status command be issued to take the detailed information. This bit is cleared by an issue of that command or by a reset signal.
D_3	RRQ (Reset request)	Set when controller has lost control of the format controller (missing address mark, for example). An auxiliary RST command or RESET signal will clear this bit.
D_2	IER (ID error)	Set when a CRC error is detected in the ID field. An auxiliary RST or another disk command will reset this bit.
D_1	NCI (Not coincident)	Set if the controller cannot find a sector on the cylinder which meets the comparison condition during the execution of a scan command. This bit is also set if data from the disk does not coincide with the data from the system during a verify ID or a verify data command. This bit is cleared by a disk command or a reset signal.
D_0	DRQ (Data request)	During execution of write ID, verify ID, scan, verify data, or a write data command, this bit is set to request that data be written into the data buffer. During execution of read ID, read diagnostic, or read data command, this bit is set to request that data be read from the data buffer.

Error Status Byte

This byte is available to the host at the termination of a read, write, or data verification command and provides additional error information to the host CPU. If the status register indicates a normal command termination, it can be assumed that the command was executed without error and it is not necessary to read this byte. When it is necessary to determine the cause of an error this byte may be read by issuing an $\overline{RD}$ pulse with $\overline{CS}$ and A_0 low. The remaining result bytes associated with a particular command may be read by issuing additional $\overline{RD}$ pulses. Data transfer from or to the FIFO is asynchronous and may occur at rates up to 2.5 Mbytes per second. See table 4.

Table 4. Error Status Bits

Pin No.	Pin Name	Function
D_7	ENC (End of cylinder)	Set when the controller tries to access a sector beyond the final sector of a cylinder. Cleared by a disk command or an auxiliary RST command.
D_6	OVR (Overrun)	When set, indicates that the FIFO became full during a read operation, or empty during a write operation.
D_5	DER (Data error)	A CRC or an ECC error was detected in the data field.
D_4	EQC (Equipment check)	A fault signal from the drive has been detected or a track 0 signal has not been returned within a certain time interval after the recalibrate command was issued.
D_3	NR (Not ready)	The drive is not in ready state.
D_2	ND (No data)	The sector specified by ID parameters was not found on the track.
D_1	NWR (Not writable)	Set if write protect signal is detected when the controller tries to write on the disk. It is cleared by a disk command or by an auxiliary RST command.
D_0	MAM (Missing address mark)	This bit is set if during execution of read data, check, scan, or verify data commands, no address mark was found in the data field or if during execution of a read ID or verify ID command, no address mark was detected in the ID field.

Interrupt Status Byte

This byte is made available to the host CPU by executing the Sense Interrupt Status command. This command should be issued only when the μPD7261A/7261B requests it, as indicated by bit D_4 of the status register. This byte reveals changes in disk drive status that have occurred. See table 5.

Table 5. Interrupt Status Bits

Pin No.	Pin Name	Function
D_7	SEN (Seek end)	A seek end or seek complete signal has been returned after a seek or a recalibrate command was issued.
D_6	RC (Ready change)	The state of the ready signal from the drives has changed. The state itself is indicated by the NR bit.
D_5	SER (Seek error)	Seek error has been detected on seek end.
D_4	EQC (Equipment check)	Identical to bit 4 of the error status byte.
D_3	NR (Not ready)	Identical to bit 3 of the error status byte.
D_2–D_0	UA_2–UA_0 (Unit address)	The unit address of the drive which caused an interrupt request on any of the above conditions.

Drive Interface

The μPD7261A/7261B has been designed to implement two of the more popular types of interfaces: the SMD (Storage Module Drive) and the floppy-like Winchester drive which has come to be known as the ST506 interface. The desired interface mode is selected by the Specify command.

ST506-Type Interface

In the ST506 mode the μPD7261A/7261B performs MFM encoding and decoding at data rates to 6 MHz and provides all necessary drive interface signals. Included internally is circuitry for address mark detection, sync area recognition, serial-to-parallel-to-serial conversion, an 8-byte FIFO for data buffering, and circuitry for logical addressing of the drives. External circuitry required consists of control signal buffering, a delay network for precompensation, a phase-lock loop, a write clock oscillator and a differential transceiver for drive data. The floppy-like interface can be implemented with as few as 7 IC's using NEC's hard-disk interface chip, the μPD9306A, or with 12 to 14 SSI ICs. See figure 1.

Figure 1. μPD7261A/7261B ST506-Type Interface

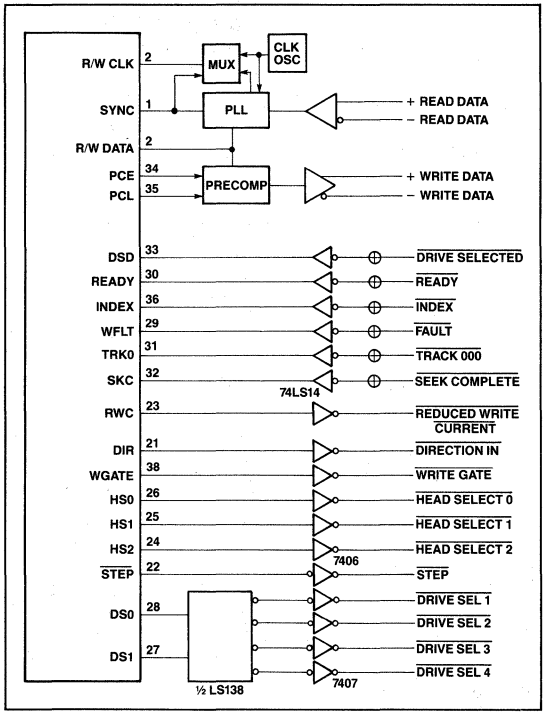
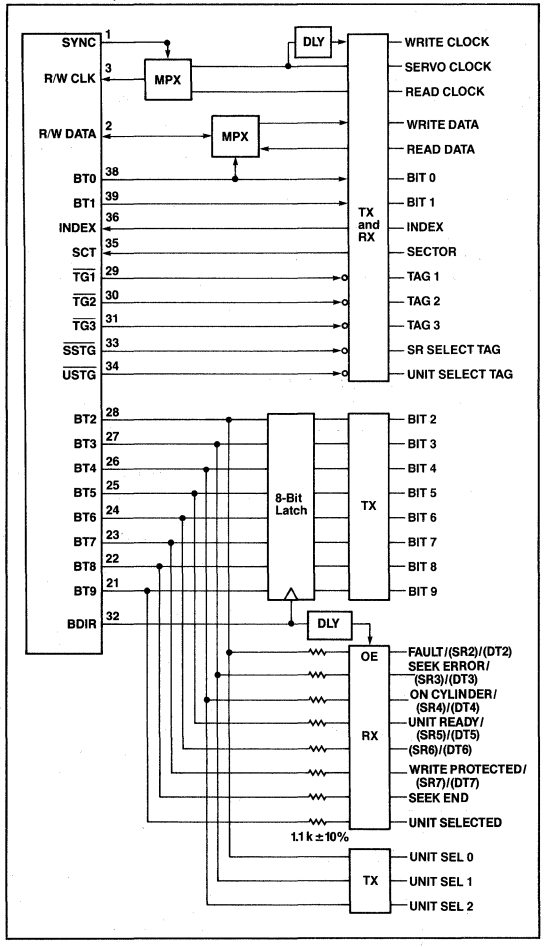


Figure 2. μPD7261A/7261B SMD Interface



SMD Interface

In the SMD mode the μPD7261A/7261B will support data rates to 10 MHz/15 MHz in the NRZ format. All control functions necessary for an SMD interface are implemented on-chip with de-multiplexing of 8 data lines performed externally by a single 8-bit latch. A small amount of logic is required to multiplex the data and clock lines, and differential drivers and receivers are required to implement the actual interface. Depending on individual logic design and the number of drives used, the SMD interface may be implemented with as few as 12 ICs. See figure 2.

Note:

CLK (pin 37) frequency must be a minimum of 1.1 × NRZ data rate.

Internal Architecture

The μPD7261A/7261B can be divided into three major internal logic blocks: command processor; format controller; microprocessor interface.

Command Processor

The command processor is an 8-bit microprocessor with its own instruction set, program ROM, scratchpad RAM, ALU, and I/O interface. Its major functions are:

- ☐ To decode the commands from the host microcomputer that are received through the 8-bit data bus
- ☐ To execute seek and recalibrate commands
- ☐ To interface to the drives and read the drive status lines
- ☐ To load the format controller with the appropriate microcode, enabling it to execute the various read/write data commands.

The command processor microprocessor is idle until it receives the command from the host microcomputer. It then reads the parameter bytes from the FIFO, and loads them into its RAM. The command byte is decoded and, depending on its opcode, the appropriate subroutine from the 2.6K internal ROM is selected and executed. Some of these commands are executed by the command processor without involvement of the format

controller. When data transfers to and from the disk are made, the command processor loads the appropriate microcode into the format controller, then relinquishes control. When the data transfer is complete, the command processor again takes control. One other important function that the command processor performs is managing the interface to the disk drives. The command processor contains an I/O port structure similar to many single-chip microcomputers in that the ports may be configured as input or output pins. Depending on the mode of operation selected by the Specify command, the command processor will use the bidirectional I/O lines for different functions.

Command Register

This register is a write only register. It is selected when the A_0 input is high and the $\overline{CS}$ input is low. There are two kinds of commands: disk commands and auxiliary commands. Each command format is shown in figure 3.

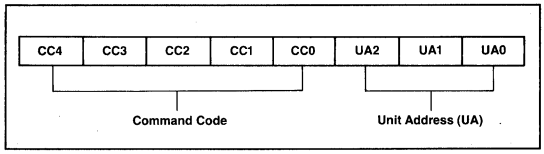
An auxiliary command is accepted at any time and is immediately executed, while a disk command is ignored if the on-chip processor is busy processing another disk command. A valid disk command causes the processor to begin execution using the parameters previously loaded into the data buffer. Disk commands and the parameters needed are described in the Microprocessor Interface section.

Command Codes

CC4	CC3	CC2	CC1	CC0	
0	0	0	0	X	(Auxiliary Command)
0	0	0	1	X	Sense int. status (Note 1)
0	0	1	0	X	Specify (Note 1)
0	0	1	1	X	Sense unit status
0	1	0	0	X	Detect error (Note 1)
0	1	0	1	[B]	Recalibrate
0	1	1	0	[B]	Seek
0	1	1	1	[S]	Format
1	0	0	0	[S]	Verify ID
1	0	0	1	[S]	Read ID
1	0	1	0	X	Read diagnostic
1	0	1	1	X	Read data
1	1	0	0	X	Check
1	1	0	1	X	Scan
1	1	1	0	X	Verify data
1	1	1	1	X	Write data

Note:
(1) The UA field is 000.
[B] Indicates buffered mode when set.
[S] Indicates skewed mode when set.

Figure 3. Disk Command Byte



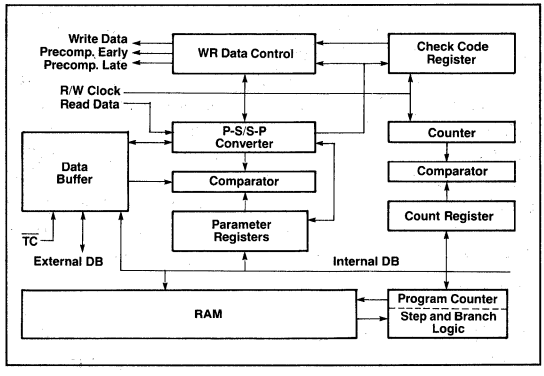
Format Controller

The format controller is built with logic that enables it to execute instructions at very high speed: one instruction per single clock cycle. The major functions it performs are:

- ☐ Serial-to-parallel and parallel-to-serial data conversion
- ☐ CRC and ECC generation and checking
- ☐ MFM data decoding and encoding
- ☐ Write precompensation
- ☐ Address mark detection and generation
- ☐ ID field search in soft-sector format
- ☐ DMA data transfer control during read/write operations.

The major blocks in the format controller are the sequencer and the serial/parallel data handler. The sequencer consists of a writable control store (32 words by 16 bits), a program counter, branch logic, and the parameter register. The serial/parallel logic consists of a parallel-to-serial converter for disk write operations, a serial-to-parallel converter for disk read operations, precompensation logic for writing MFM data, comparator logic that locates sync fields, address marks, and ID fields. There is also comparator logic that is used during Verify Data commands. See figure 4.

Figure 4. Block Diagram of the Format Controller



6

Microprocessor Interface

Read/Write Control. The internal registers are selected as shown in truth table 6.

Table 6. Register Selection Table

$\overline{CS}$	A_0	$\overline{RD}$	$\overline{WR}$	Selection
0	0	0	1	Data buffer register (Note 1)
0	0	1	0	Data buffer register (Note 1)
0	1	0	1	Status register
0	1	1	0	Command register
0	X	1	1	Don't care
1	X	X	X	Don't care
0	X	0	0	Inhibited

Note:
(1) Preset parameters and result status information are written and read from the result status register in the HDC through this data buffer register.

Interrupt. The interrupt request line is activated or inactivated according to the following equation:

$$INT = CEH + CEL + SRQ \bullet \overline{SRQM}$$

This means that if either of the command end bits is set or if the sense interrupt status request bit is set (and the SRQM mask is not set), then an interrupt will be generated. The command end bits, CEH and CEL, are set by command termination.

The SRQ bit is set when an equipment check condition or a state change of the ready signal from the disk drives is detected. It is also set when a seek operation is completed. Under these conditions the INT line is activated unless the SRQM mask is set.

Both of the CEH and CEL bits are cleared by a disk command, but both bits may be cleared before the next disk command by issuing a CLCE auxiliary command.

The interrupt caused by the SRQ bit indicates that a sense interrupt status command should be issued by the host microprocessor so that it can determine the exact cause of the interrupt. However, the μPD7261A/7261B may be processing a disk command when the interrupt occurs. Since it is not possible to issue a disk command while the μPD7261A/7261B is busy, an HSRQ auxiliary command can be issued to set the SRQM (sense interrupt request mask) and mask the interrupt. The SRQM is reset upon completion of the disk command in progress.

DMA Control. When true, the DREQ pin and the DRQ (data request) bit of the status register indicate a request for data transfer between the disk controller and external memory. These are activated during execution of the following disk commands:

HDC ← memory: Format, Verify ID, Scan, Verify Data, Write Data

HDC → memory: Read ID, Read Diagnostic, Read Data

Data being read from a disk or external memory is temporarily stored in the data buffer (8 bytes maximum), and is transferred to external memory or a disk, respectively.

Data transfers are terminated externally by a reset signal or by a read or a write data operation coinciding with an active terminal count ($\overline{TC}$) signal. They are also terminated internally when an abnormal condition is detected or all the data specified by the sector count parameter (SCNT) has been transferred.

Data transfers are accomplished by $\overline{RD}$ or $\overline{WR}$ signals to the μPD7261A/7261B when DREQ is active. During read operations, DREQ goes active when the FIFO contains three or more bytes. If the FIFO contains three bytes and an $\overline{RD}$ pulse is issued, DREQ goes low within t_{RRQ1}. DREQ will stay active on the final sector until the final byte is extracted. In this case, DREQ goes low within t_{RRQ2}. During write operations DREQ is asserted as soon as a Write Data command is accepted. DREQ remains high until the FIFO contains six bytes, at which time it goes low within t_{WAI}. DREQ corresponds to FIFO almost-full and FIFO almost-empty as implemented in the μPD7261A/7261B. This has been done so that a fast DMA controller may actually overrun the FIFO by one or two bytes without harm.

Commands

Recalibrate

0101B	
	IST*

The read/write heads of the specified drive are retracted to the cylinder 0 position. IST is available as a result byte only if polling mode is disabled. See Specify.

Hard-Sector. An RTZ (Return to Zero) signal is asserted on the bit-6 line with the TAG-3 bit being set. Then the CEH bit of the status register is set indicating a normal termination of the command.

After this command is given, the HDC checks the seek end, unit ready, and fault lines of the drive continually until an active signal is detected on these lines. Then the SRQ bit of the status register is set indicating that a sense interrupt status command should be performed. Each bit of the IST (interrupt status) byte is set according to the result, in anticipation of the sense interrupt status command.

Soft-Sector. There are four different ways to implement the Recalibrate command when the ST506 interface mode has been specified. Both polling and nonpolling modes of operation are provided, with both normal or buffered Recalibrate commands available in either mode.

Normal Mode with Polling. The CEH bit of EST is set to 1 immediately after the Recalibrate command is issued (a Recalibrate command may now be issued to another drive). The HDC now begins generating step pulses at the specified rate. The PCN for the drive is cleared and the TRK0 signal is checked while stepping pulses are sent to one or more drives. When TRK0 is asserted, the SEN (seek end) bit of the IST (interrupt status) byte is set and the SRQ bit of the status register is set. This causes an interrupt and requests that a sense interrupt status command be issued. If 1023 pulses have been sent and TRK0 is not asserted, then the SRQ bit is again set, but with the SER (seek error) and EQC (equipment check) bits of the IST byte set. The ready signal of each drive is checked before each step pulse is sent, and the Recalibrate command is terminated if the drive enters a not-ready state, whereby the NR bit of the IST byte is set to 1.

Normal Mode with Polling Disabled. Operation is similar to that in "Normal Mode with Polling", but the CEH and CEL bits of the status register are not set until either the SEN (seek end) or the SER (seek error) condition occurs. The SRQ bit is not set when polling is disabled, and the IST byte is now available as a result byte when the Recalibrate command is terminated (see "Preset Parameters and Result Status Bytes"). It is not possible to overlap Recalibrate operations in this mode.

Buffered Mode with Polling. This mode operates in a manner similar to that described as "Normal Mode with Polling", but with the following differences:

(1) 1023 step pulses are sent at a high rate of speed (approximately 50 μs between pulses)

(2) After the required number of pulses are sent, the CEH bit is set, and then additional Recalibrate or Seek commands will be accepted for other drives

(3) The SRQ bit is set when the drive asserts SKC, which causes the SEN bit of the IST byte to be set

(4) If SEN is not set within the time it takes to send 1023 "normal" pulses (i.e., when in normal stepping mode), then SER and EQC of the IST byte are set.

Buffered Mode with Polling Disabled. 1023 stepping pulses are immediately sent after the Recalibrate command is issued. CEH and/or CEL is set when SEN or SER occurs. SEN is set when TRK0 from the addressed drive is asserted. SER is set if TRK0 is not asserted within the time required to send 1023 "normal" pulses. The Recalibrate command will be terminated abnormally if a not-ready condition occurs prior to SEN being set. The SRQ bit of the status register is not set. The IST byte (interrupt status) is available as a result byte when either CEH or CEL is set.

Seek

0110B	PCNH	PCNL
	IST*	

PCNH = Physical Cylinder Number, High Byte
PCNL = Physical Cylinder Number, Low Byte

The read/write heads of the specified drive are moved to the cylinder specified by PCNH and PCNL. IST is available as a result byte only if polling mode is disabled. See Specify.

Hard-Sector. The contents of PCNH and PCNL are asserted on the BIT0 through BIT9 output lines of the SMD interface with the TAG1 control line being set. (The most significant six bits of PCNH are not used.) The CEH bit of the status register is then set, and the command is terminated normally.

The HDC then checks the seek end, unit ready and fault lines of the drive continually until an active signal is detected on these lines. The SRQ bit of the status register is then set requesting that a Sense Interrupt Status command be performed. Each bit of the IST (interrupt status) byte is set appropriately in anticipation of the Sense Interrupt Status command.

Soft-Sector (Normal Stepping, Polling Enabled). In this mode, the CEH bit of the status register is set to 1 as soon as the Seek command is issued. This allows a Seek or Recalibrate command to be issued to another drive. The HDC now sends stepping pulses at the specified rate and monitors the ready signal. Should the drive enter a not-ready state, the SER bit of the IST byte is set and the SRQ bit of the status register is set, causing an interrupt and requesting a Sense Interrupt Status command. When the drive asserts the seek complete (SKC) signal, the SEN bit of the IST byte is set and the SRQ bit of the status register is set, again requesting service.

Soft-Sector (Normal Stepping, Polling Disabled). Stepping pulses to the drive begin as soon as the Seek command is accepted. The ready signal is checked prior to each step pulse. If the drive enters a not-ready state the seek command is terminated abnormally (CEL = 1), and SER of the IST byte is set. If the seek operation is successful, the seek command will be terminated normally (CEH = 1) when the drive asserts SKC (seek complete). The SEN (seek end) bit of the IST byte is set and the IST (interrupt status) byte is available as a result byte. The Sense Interrupt Status command is not allowed (SRQ is not set), nor can seek operations be overlapped in this mode.

Soft-Sector (Buffered Stepping, Polling Enabled). As soon as the Seek command is accepted by the HDC, high-speed stepping pulses are generated. As soon as the required number of pulses are sent, CEH is set to 1, indicating a normal termination. Another Seek command in the same mode may now be issued. The drive is now controlling its own head positioner and asserts SKC when the target cyclinder is reached.) If the drive has not asserted SKC (seek complete) within the time it takes to send the required number of pulses in normal stepping mode, or if the drive enters a not-ready state, then the SER bit of the IST byte and the SRQ bit of the status register are set. Otherwise, the SEN bit of the IST byte is set, along with SRQ of the status register.

Soft-Sector (Buffered Stepping, Polling Disabled). In this mode, the appropriate number of high-speed stepping pulses are sent as soon as the Seek command is issued. If the drive enters a not-ready state, or if SKC (seek complete) is not asserted within the time it takes to send the required number of pulses in normal stepping mode, then the Seek command is terminated normally (generating an interrupt). The IST byte is available as a result byte and the appropriate bit is set; i.e., SER and EQC or NR (not ready). If the seek operation is successful, the Seek command is terminated normally (CEH = 1) and the SEN bit of the IST byte is set. The IST byte is available as a result byte. The Sense Interrupt Status command is not allowed (SRQ is not set), nor can seek operations be overlapped in this mode.

Format

0111S	PHN	(PSN)	SCNT	DPAT	GPL1	(GPL3)	
	EST	SCNT					

PHN = Physical Head Number
PSN = Physical Sector Number
SCNT = Sector Count
DPAT = Data Pattern
GPL1 = Gap Length 1
GPL3 = Gap Length 3
EST = Error Status

This command is used to write the desired ID and data format on the disk.

(1) When using hard-sector drives, this command will begin format-writing at the sector specified by PHN and PSN, which are loaded during command phase.

When soft-sector drives are specified, this command will begin format-writing at the sector immediately following the index pulse on the track specified by PHN.

In either case, data transmitted from the local memory by DMA operation is written into the ID field, and the data field is filled with the data constant specified by DPAT until DTL (data length) is zero. DTL is established during the specify command with DTLH and DTTL. The sector count, SCNT, is decremented by one at the end of the Format operation on each sector. The following bytes are required by the HDC for each sector: (FLAG), LCNH, LCNL, LHN, and LSN. FLAG is omitted on soft-sector drives. These bytes are transferred by DMA.

The format operation produces the various gaps with length as specified by GPL1, GPL2 (See Specify), and GPL3 (For soft-sector only.)

Note:
GPL3 may not exceed decimal value of 44.

(2) The above operation is repeated until SCNT is equal to zero. The execution of the command is terminated normally, when the content of SCNT is equal to zero and the second index pulse has occurred.

(3) When using a hard-sector drive, it is possible to write the ID field displaced from the normal position by 64 bytes by setting the skew bit of the command byte ((S) = 1). This is useful when defective media prevent writing in the normal area of the sector.

(4) Items 4, 5, and 8 of the Read Data and item 4 of the Write Data command are identical for this command. Refer to these items (which appear later in this section) for remaining format operation details.

Verify ID

1000S	PHN	(PSN)	SCNT	
	EST	SCNT		

PHN = Physical Head Number
PSN = Physical Sector Number
SCNT = Sector Count
EST = Error Status

ID bytes of specified sectors are read and compared with the data that are accessed from local memory via DMA control. The first sector that is verified is specified by PHN and PSN when a hard-sector disk is used. For soft-sector disks, only PHN is given and the Verify ID command begins comparisons with the first physical sector on the track.

Byte comparisons continue as long as successful or until the sector count is zero or a CRC error is found.

When using a hard-sector drive, it is possible to have the HDC verify a skewed ID field by setting the skew bit of the command byte. Refer to the Format section, given earlier, for details.

Read ID

1001S	PHN	PSN	SCNT	
	EST	SCNT		

PHN = Physical Head Number
PSN = Physical Sector Number
SCNT = Sector Count
EST = Error Status

ID bytes of specified sectors are read and transferred to local memory by DMA.

Hard-sector disks: Beginning with the sector specified by PHN and PSN, the ID bytes of each sector (FLAG, LCNH, LCNL, LHN, LSN) are read until an error is found or the SCNT has reached zero.

It is also possible to perform the above operation with skewed ID fields by setting the skew bit of the command byte. This will allow reading ID fields that have been shifted by 64 bytes by the Skewed Format command.

Soft-sector disks: This command will begin checking ID fields immediately following the index pulse and will continue until one valid ID field is read, or until the second index pulse is detected or SCNT = 0, whichever occurs first. Four bytes per soft sector are read: LCNH, LCNL, LHN, and LSN.

Read Diagnostic

1010X	PHN	PSN	
	EST		

PHN = Physical Head Number
PSN = Physical Sector Number
EST = Error Status

This command is implemented only for hard-sector disks. The desired physical sector is specified, and the data field will be read even if the ID bytes of that sector contain a CRC error. Only one sector at a time may be read by this command.

Read Data

1011X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

This command is used to read and transfer data via DMA from the disk to the local memory.

(1) The HDC reads data from the specified sector which is determined by the following preset parameters: FLAG (for hard-sector only), LCNH, LCNL, LHN, and LSN. The drive is selected by UA (unit address) in the command byte. The HDC then transfers the read data to the local memory via DMA operation.

(2) After reading each sector, the HDC updates the SCNT and LSN to point to the next sector, and repeats the above described operation until SCNT is equal to zero. During the above read operations, if LSN is equal to ESN, the HDC updates LSN, and continues the read operations after relocating the head (track) specified by LHN.

(3) The HDC abnormally terminates the execution of this command if SCNT is not equal to zero when the HDC reads out the data from the last sector (LSN = ESN and LHN = ETN). The ENC (end of cylinder) bit of EST (error status) is set to one in this situation.

(4) The HDC will terminate this command if a fault signal is detected while reading data. The HDC will set the EQC (equipment check) of the EST (error status) byte when this occurs.

(5) The HDC will terminate this command abnormally if the ready signal from the drive is not active or becomes not active while a Read Data command is being performed. The NR (not ready) bit of the EST (error status) register will be set to one in this case.

(6) The HDC will end this command abnormally if it cannot find an AM (address mark) (soft-sector mode) or a SYNC byte (hard-sector mode) of the ID field before four index pulses occur. Under these conditions, the RRQ (reset request) bit of the STR (status register) will be set. In order to perform further disk commands the HDC will have to be reset because the format controller is hung up looking for an AM or SYNC byte.

(7) ECC mode: If the HDC detects an ECC error during a read operation, it will execute the following operations: First, the HDC decides whether or not the error is correctable by checking the syndrome of the error pattern. If the error is correctable, the HDC terminates the command in the normal mode after setting the DER (data error) bit of EST register to one. The host system can input the error address and the error pattern information by issuing the Detect Error command. If it is not a correctable error, the HDC will terminate the command in the abnormal mode after setting the DER bit of the EST register to one.

CRC mode: If the HDC detects a CRC error on a sector during the read operation, the HDC will terminate the command in the abnormal mode after setting the DER bit of the EST register to one.

(8) If the HDC detects an overrun condition during a Read Data operation, the OVR (overrun) bit of the EST register is set. (An overrun condition occurs when the internal data FIFO is full, another data byte has been received from the disk drive, and a DMA service does not occur.) The command is then terminated in the abnormal mode.

(9) If the HDC cannot find the desired sector within the occurrence of three index pulses, the ND (no data) bit of the EST register is set to one and the command is terminated in the abnormal mode.

(10) If TC (terminal count) occurs during a Read Data command the DMA transfers to the local memory will stop. However, the HDC does continue the read operation until the end of the sector, if SCNT = 1.

If SCNT is 2 or more, DMA transfers restart when SCNT is updated to the next sector, and will continue until SCNT is zero.

(11) If the Read Data command has been successfully completed, the result status will be set indicating such, and the result status bytes will be updated according to the number of sectors that have been read. The logical disk parameters — LSN, LHN, and LCN — are incremented as follows:

LSN is incremented at the end of each sector until the value of ESN is reached. LSN is then set to 0 and LHN is incremented. If LHN reaches the value of ETN, then LHN is cleared and LCN is incremented.

In other words, if a Read or Write operation is terminated normally, the various parameters will point to the next logical sector.

If the command is terminated in the abnormal mode, the result status bytes will indicate on which sector, cylinder, and head the error occurred.

(12) If the HDC cannot detect the address mark (soft-sector) or SYNC bytes (hard-sector) immediately following the VFO sync in the data field, the HDC will set the MAM (missing address mark) bit of the EST register to one, and will terminate the command in the abnormal mode.

Check

1100X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

This command is used to confirm that the data previously written to the medium by the Write Data command contains the correct CRC or ECC.

(1) The HDC reads the data in the sector specified by FLAG (hard-sector only), LCNH, LCNL, LHN, and LSN. The Check command differs from the Read Data command in that no DMA transfers occur.

With the exception of the ECC mode, the Check command is the same as the Read Data command. Please refer to items 2, 3, 4, 5, 6, 7, 8, 11, and 12 of Read Data command for details.

(2) If in the ECC mode, the HDC detects only ECC errors and does not execute any error correction operation even if the ECC errors are correctable. No data transfers have been made, and there is no data to correct.

Scan

1101X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

(1) In executing the Scan command, the HDC reads the data from the sector specified by the preset parameters of the command phase. The HDC then compares this data with the data transmitted from the local memory. (The purpose of this command is to locate a sector that contains the same data as the local memory.)

This command will terminate successfully if the data from the disk and the data from the local memory are the same. If they are not, the HDC updates SCNT and LSN, and executes the abovementioned operation again.

If the HDC cannot locate a sector that satisfies the scan conditions, the NCI bit of the STR will be set. The HDC tries to compare data until the end of the cylinder has been reached, or until SCNT is zero.

(2) If the value of the LSN (logical sector number) is equal to that of ESN (ending sector number) after updating LSN, the HDC updates the contents of LHN (increasing by 1) and that of LSN (LSN = 0), and repeats the operation described in item 1 after selecting the next head.

(3) After comparing the data transferred from the host CPU with the data in the specified sectors, the result bytes (FLAG, which is only for hard-sector disks, LCNH, LCNL, LHN, and LSN) will be set equal to the sector location that satisfies the Scan command.

(4) The descriptions in 4, 5, 6, 8, and 9 of Read Data command, and items 3 and 4 of Verify Data command are identical for this command. Refer to these descriptions for additional details.

Verify Data

1110X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

This command is used to verify data on the disk.

(1) The HDC reads the data from the specified sector, and compares the data transmitted from the local memory via DMA with the data from the disk.

The sector is specified by FLAG (hard-sector only), LCNH, LCNL, LHN, and LSN, and the drive is selected by UA. If the data transmitted from the local memory is the same as that read from the sector, the HDC updates the contents of LSN and SCNT, and continues the abovementioned operation. After updating SCNT, if the value of SCNT is equal to zero, the HDC ends the execution of the command in the normal mode. If the value of LSN is equal to that of ESN after updating LSN, the HDC updates the contents of LHN and LSN, and the HDC continues the verify data operation after selecting the head (track) specified by LHN.

If the data transmitted from the local memory is not the same as that read from the sector, the HDC ends the execution of the command in the abnormal mode after setting the NCI (not coincident) bit of STR to one.

(2) If, after verifying the data on the last sector, the contents of SCNT are not equal to zero, the HDC terminates execution of the command abnormally after setting the ENC (end of cylinder) bit of the EST register to one.

(3) After verifying the data read from a sector, the HDC checks the CRC bytes (CRC mode) or the ECC bytes (ECC mode).

If the HDC detects a CRC or an ECC error on a sector, the HDC terminates execution of the command abnormally after setting the DER bit of the EST register to a one.

(4) After detecting an active $\overline{TC}$ signal ($\overline{TC} = 0$), the HDC executes the above operation by comparing the read data from the disk drive with the data 00 instead of the data from the main system until the end of the sector.

In the case of SCNT greater than one, when SCNT is updated, DMA transfers restart and disk data is compared against host data until SCNT is zero.

(5) After verification of the data on all the sectors, FLAG (hard-sector only), LCNH, LCNL, LHN, and LSN are set to the values of FLAG, LCNH, LCNL, LHN, and LSN of the last verified sector.

(6) The descriptions in items 4, 5, 6, 8, 9, and 12 of the Read Data command are valid in this command. Please refer to these items for additional detail.

Write Data

1111X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

(1) This command is used to write data into the data field of the sectors specifed by FLAG (hard disks only), LCNH, LCNL, LHN, and LSN, and to write CRC bytes or ECC bytes according to each internally specified mode (CRC or ECC). The data is written to the disk via DMA transfer from the local memory.

(2) After writing data on a sector, the HDC updates the contents of SCNT and LSN, and repeats the above described Write Data operation until SCNT is equal to zero.

During the above Write Data operations, if LSN is equal to ESN, the HDC updates LHN and LSN, and continues the Write Data operations after selecting the new head (track) specified by LHN.

As described above, the HDC has the capability of multi-sector and multi-track write operations.

(3) The HDC abnormally terminates the execution of this command if the SCNT is not equal to zero when the HDC writes the data to the last sector (LSN = ESN and LHN = ETN). The ENC (end of cylinder) bit of EST (error status) register is set to one in this situation.

(4) If the write protected signal is active (high) at the beginning of the execution of this command, the HDC ends the execution of this command in the abnormal mode after setting the NWR (not writable) bit of the EST register to one.

(5) After detecting an active $\overline{TC}$ signal ($\overline{TC} = 0$), the HDC writes the data 00 to the sector, instead of the data from the host system.

In the case of SCNT of two or more, when SCNT is updated, the DMA transfers will restart and writing of host data will continue until SCNT = 0.

(6) In the ST506-type mode, the HDC will set the reduced write current output bit to a one when the cylinder number becomes greater than that specified by RWCH and RWCL. These parameters are loaded during execution of the Specify command.

The descriptions in items 4, 5, 6, 8, 9, and 11 of the Read Data command are applicable here also. Refer to these items for further detail.

Sense Interrupt Status

0001X	
	IST

IST = Interrupt Status

(1) The HDC transfers the new disk status to the host CPU at the end of a Seek or Recalibrate operation or the new disk status resulting from a change of state of the ready signal, which may occur at any time.

(2) If the Seek or Recalibrate command in progress is completed when this command is issued or if there has been no change of state of the ready signal from the drive, this command will be terminated abnormally.

Specify

0010X	MODE	DTLH	DTLL	ETN	ESN	GPL2	(MGPL1) [RWCH]	[RWCL]

MODE = Mode Byte; Selects Operation Mode
DTLH = Data Length, High Byte
DTLL = Data Length, Low Byte
ETN = Ending Track Number
ESN = Ending Sector Number
GPL2 = Gap Length 2
MGPL1 = Gap Length 1 (used in SMD mode only); Controls Read Gate Timing
RWCH = Reduced Write Current (Cylinder No.), High Byte
RWCL = Reduced Write Current (Cylinder No.), Low Byte

The Specify command is used to set the operational mode of the HDC by presetting various parameters. Parameters such as MODE (figure 5, table 7), DTLH (figure 6), DTLL, ETN, ESN, GPL2, MGPL1/RWCH, and RWCL may be programmed into the HDC. This allows for a high degree of versatility. Data record length is programmable from 128 to 4095 bytes in soft-sector mode and 256 to 4095 bytes in hard-sector mode.

Figure 5. Mode Byte

0	ECC	CRCS	SSEC	DSL/ STP3	DSE/ STP2	SOM/ STP1	SOP/ STP0

Figure 6. DTLH Byte

1	CRC·	PAD	POL	DTL11	DTL10	DTL9	DTL8

CRC· = Initial Value of Polynomial Counter, Either All Zeros or All Ones
PAD = Selects ID/Data pad of 00H if 0
= Selects ID/Data pad of 4EH if 1
POL = Polling Mode if 0
= Nonpolling Mode if 1

Table 7. Mode Byte Bits

Bit Name	Specified Mode
ECC	1 ECC is appended in data field: $(x^{21}+1)(x^{11}+x^2+1)$
	0 CRC is appended in data field
CRCS	1 Generator polynomial: $(x^{16}+1)$
	0 Generator polynomial: $(x^{16}+x^{12}+x^5+1)$
SSEC	1 Soft-sector disk (floppy-like interface), MFM data
	0 Hard-sector disk (SMD interface), NRZ data

	SSEC = 0		SSEC = 1
DSL	Data strobe late	STP3	(Note 1)
DSE	Data strobe early	STP2	(Note 1)
SOM	Servo offset minus	STP1	(Note 1)
SOP	Servo offset plus	STP0	(Note 1)

Note:
(1) Stepping rate for ST506 mode = (16-STP) × 2110 × t_{CY}
Assuming a 10 MHz processor clock: F_H = 2.11 ms...O_H = 33.76 ms

Sense Unit Status

Soft-Sector Mode

0011X	
	UST

SMD Mode

0011X	1	2	5
	UST	DS	DT

The Sense Unit Status (SUS) command is used to transfer the Unit Status (UST) to the host. In the case of SMD mode the SUS command may also be used to transfer the Detail Status (DS) and Device Type (DT) by using the appropriate preset parameter value as shown above. No preset parameters are used in the soft-sector mode, although one is required in the SMD mode. Values other than 1, 2, or 5 do not produce valid results.

After result bytes are placed in FIFO, HDC generates a FAULT CLEAR when in SMD mode.

The DS and DT bytes are defined by the type of drives used. The UST is shown in table 8.

Table 8. Unit Status Byte

Bit No.	Interface Type: SMD	Interface Type: ST506
D_7	Unit selected	0
D_6	Seek end	0
D_5	Write protected	0
D_4	0	Drive selected
D_3	Unit ready	Seek complete
D_2	On cylinder	Track 000
D_1	Seek error	Ready
D_0	Fault	Write fault

Detect Error

0100X	
	EADH EADL EPT1 EPT2 EPT3

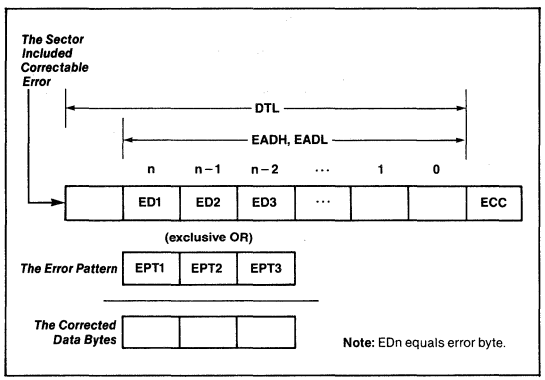
EADH = Error Address, High Byte
EADL = Error Address, Low Byte
EPT1 = Error Pattern, Byte 1
EPT2 = Error Pattern, Byte 2
EPT3 = Error Pattern, Byte 3

This command is used to transfer the error pattern and the error address to the host CPU, when correctable errors have occurred during the execution of a Read Data command with the ECC mode enabled.

The error address (EADH and EADL) is calculated from the last data byte of the sector that contained a correctable error which was indicated by the status bit of the previous Read Data command with the ECC mode enabled. The error pattern is used for correcting the error data at the location where the error occurred. After receiving the error address and the error pattern, the host CPU can correct the error data by performing an exclusive-OR of the error pattern and the error data. See figure 7.

The result bytes are available to the host CPU within 100μs.

Figure 7. Error Correction



Auxiliary Command

0000AAAA	

There are no preset parameters or result bytes associated with this command. The definitions of the 4 LSBs (AAAA) are given in figure 8 and table 9. The auxiliary command is accepted at any time and is immediately executed. The auxiliary command may be used to recover from certain types of error conditions, or to mask and clear interrupts.

Figure 8. Auxiliary Command

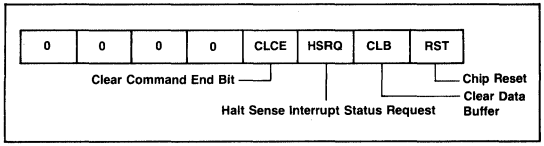


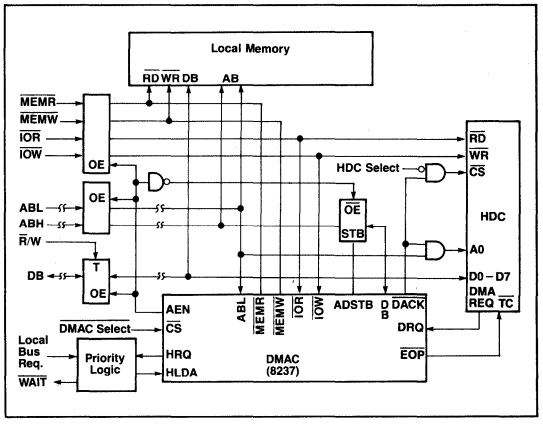
Table 9. Auxiliary Command Bits

Bit Name	Operation
CLCE	Clears the CE bits of the status register, inactivating the interrupt request output caused by Command End condition. This is used when no disk commands are going to be issued and it is desired to clear the interrupt.
HSRQ	Deactivates the interrupt request output caused by Sense Interrupt Status Request condition until a Command End occurs. However, this command has no effect on the SRQ bit of the status register.
CLB	Clears the data buffer.
RST	This has the same effect as a reset signal on the Reset input. This function is used whenever the RRQ bit in the status register is set (indicating the format controller is hung up), or when a software reset is needed.

System Example

Figure 9 shows an example of a local bus system.

Figure 9. Local Bus System



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Track Format

Figure 10 shows track format for hard- and soft-sectored disks.

System Example Timing Diagrams

Figures 11 through 22 show the interface timing (soft-sector and hard-sector) required to interface the hard disk drive.

Figure 10. Track Format

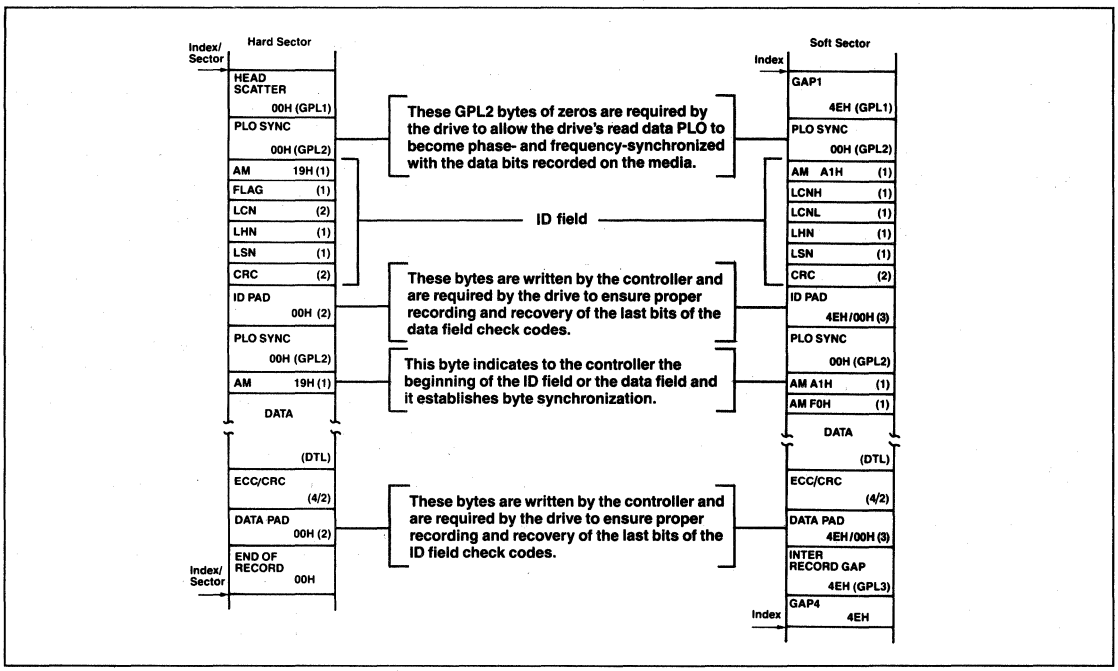

Figure 11. "Unit Selection" and "State Sense" Timing (Hard Sector)

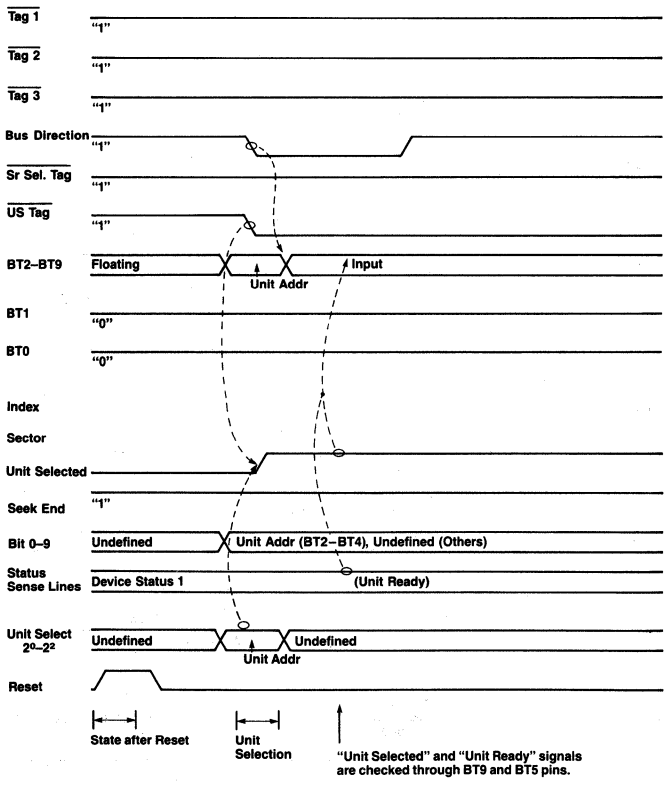

Figure 12. Return to Zero Timing (Hard Sector)

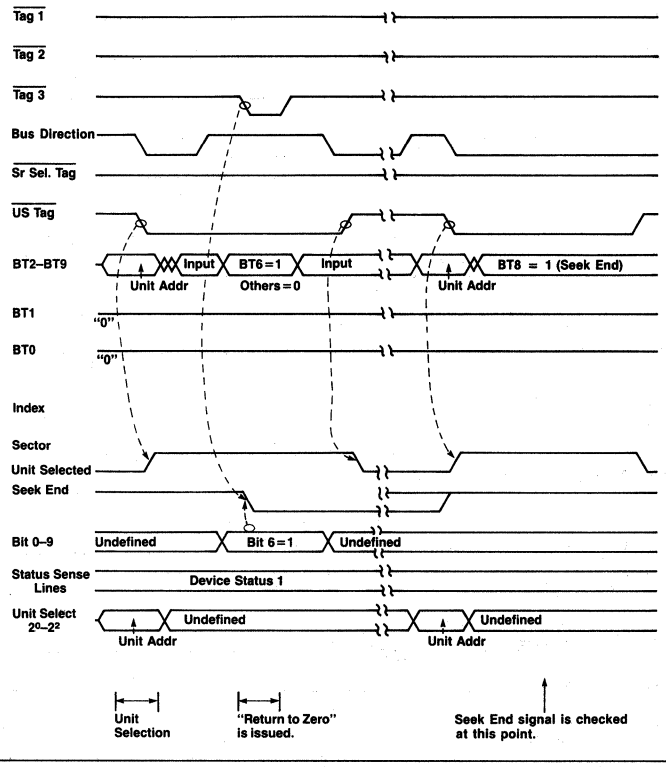

Figure 13. "Seek" Timing (Hard Sector)

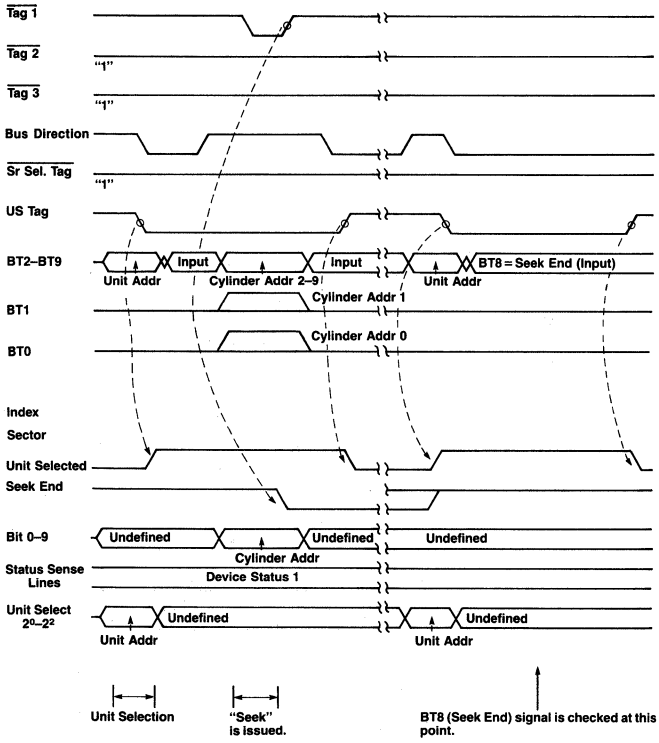

Figure 14. "Head Select" Timing (Hard Sector)

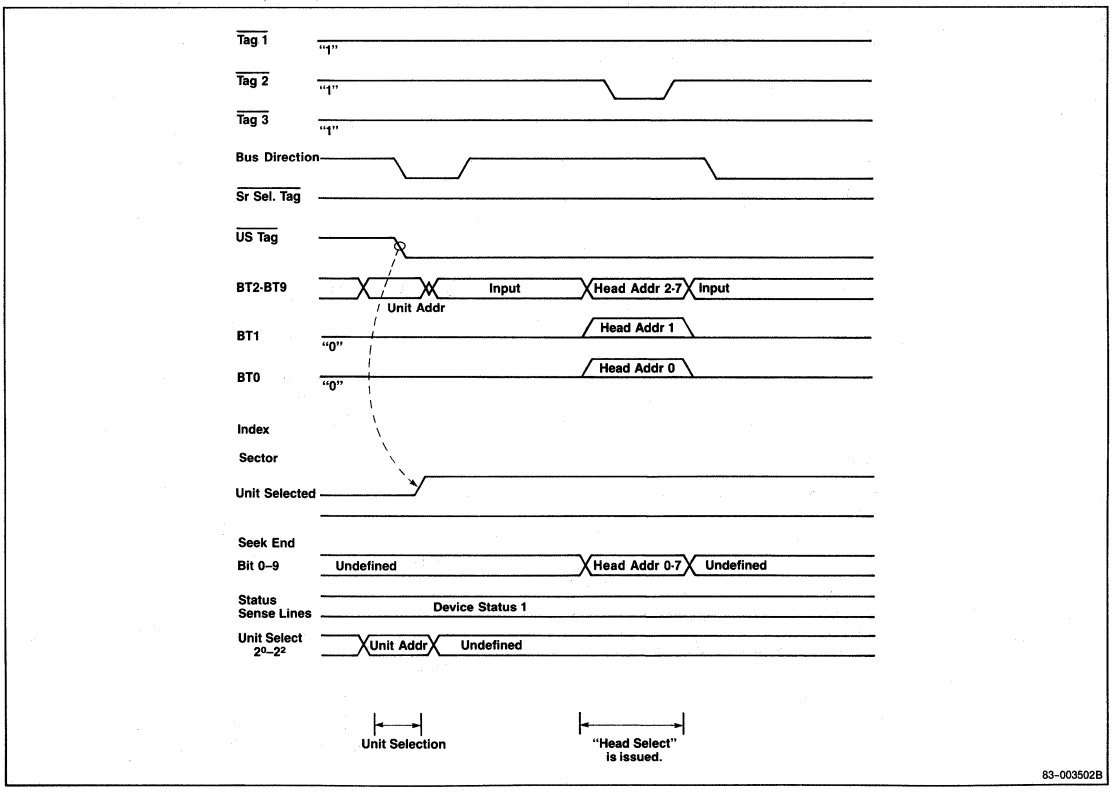

Figure 15. "Unit Status Sense' Timing (Hard Sector)

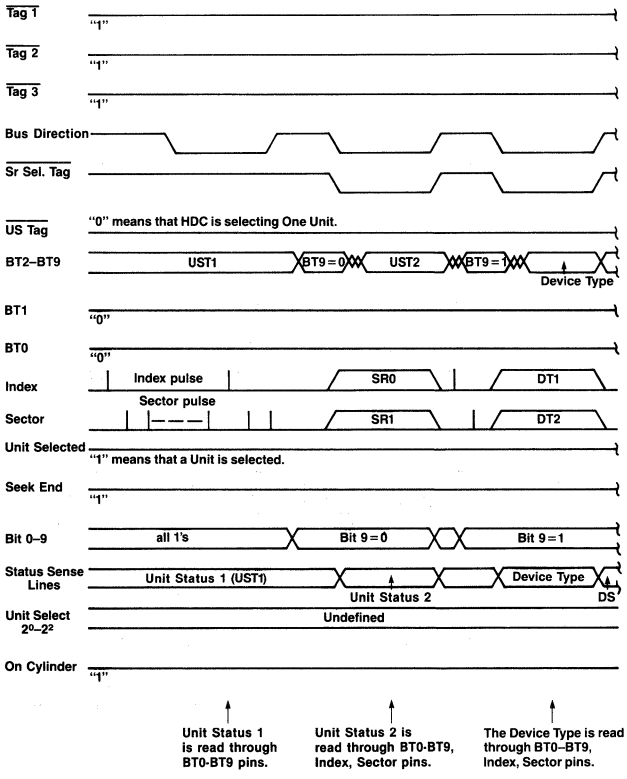

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Figure 16. "Data Read" Timing (Hard Sector)

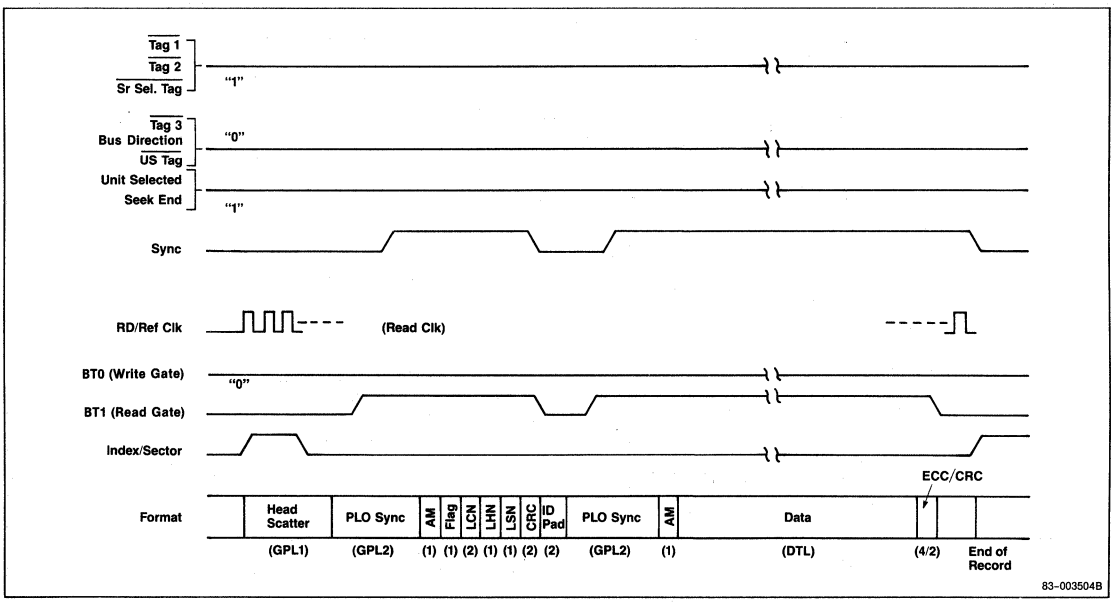

Figure 17. "Data Write" Timing (Hard Sector)

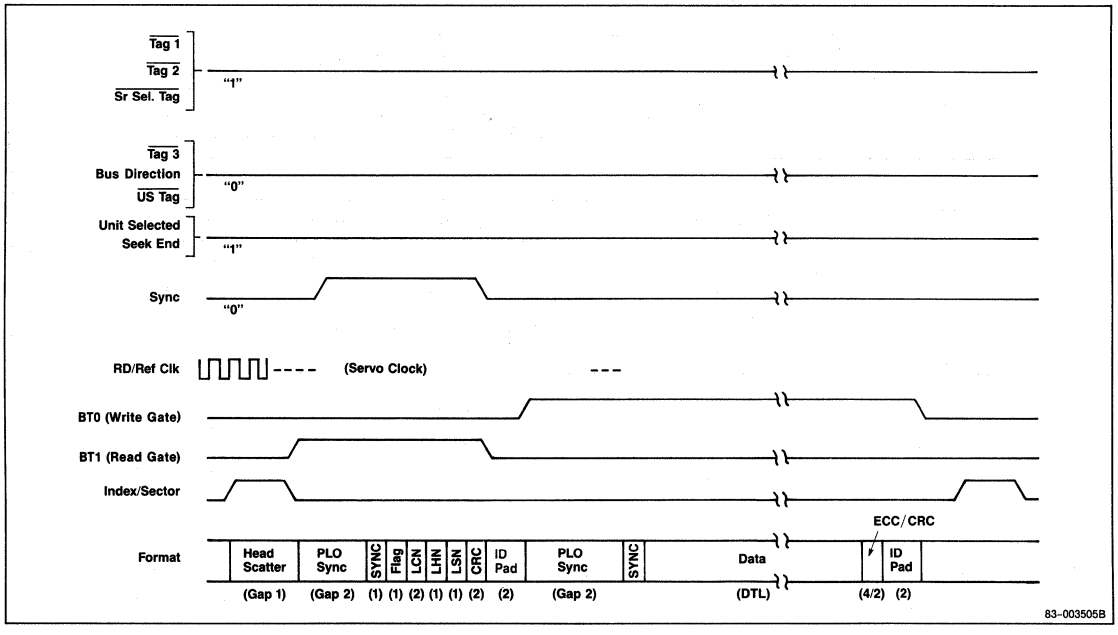

Figure 18. "Drive Select" and "Unit Status Sense" Timing (Soft Sector)

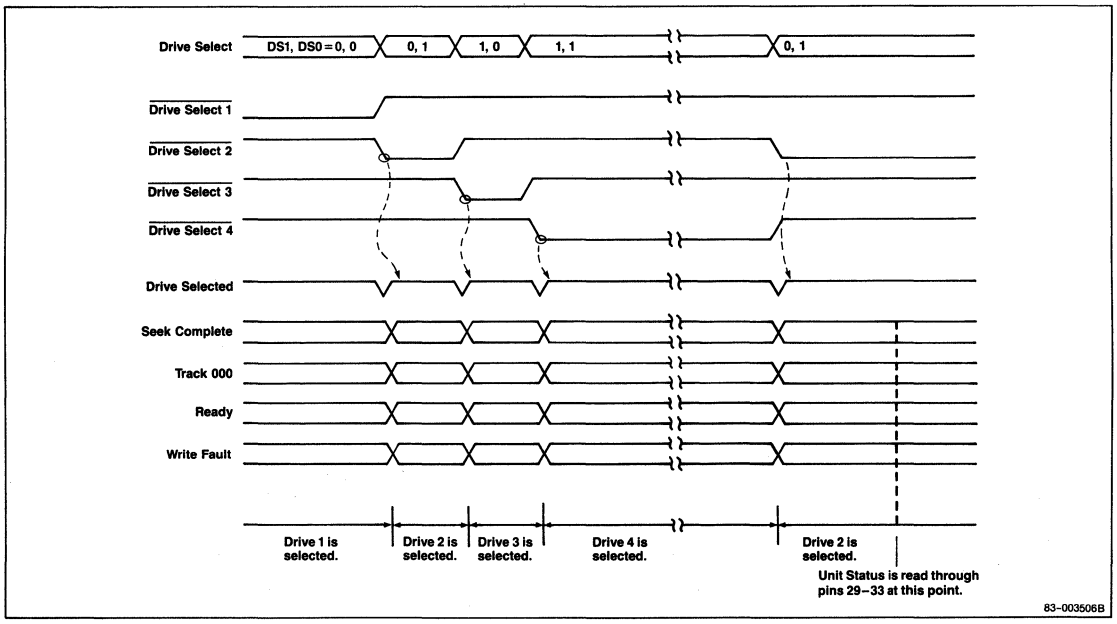

Figure 19. "Normal Seek" Timing (Soft Sector)

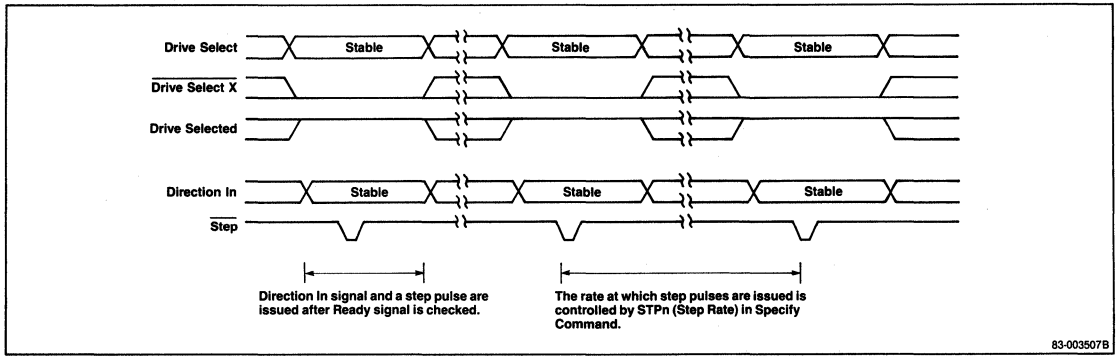

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Figure 20. "Buffered Seek" Timing (Soft Sector)

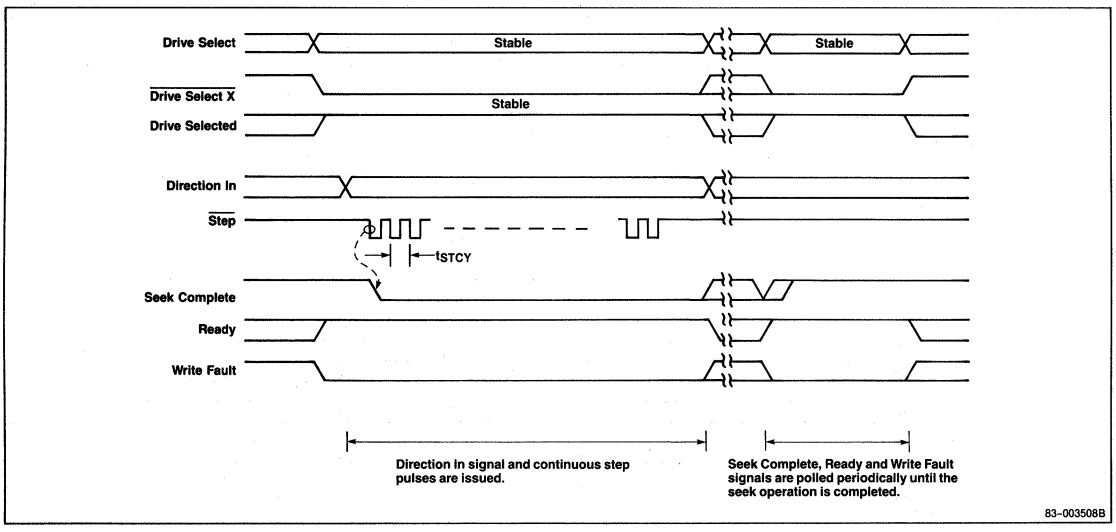


Figure 21. "Data Read" Timing (Soft Sector)

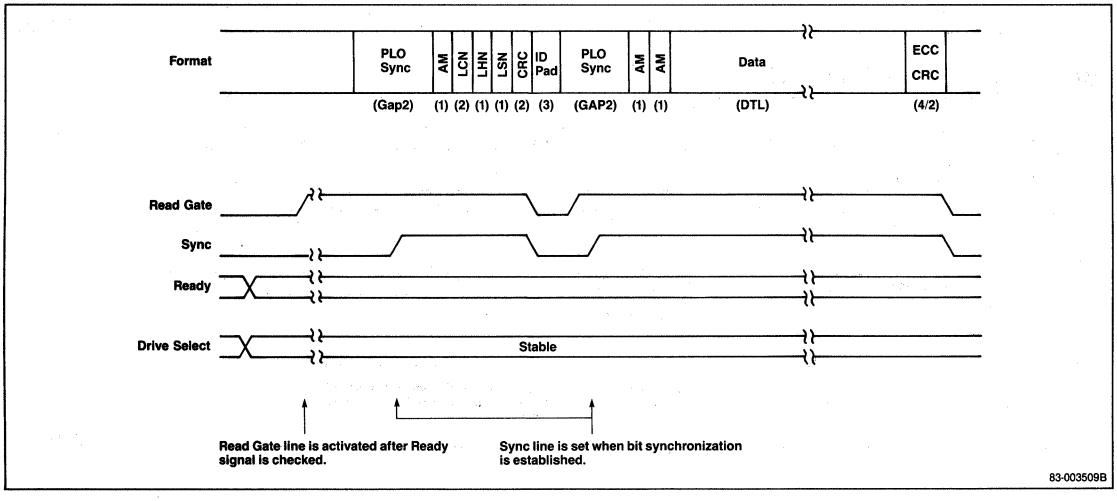
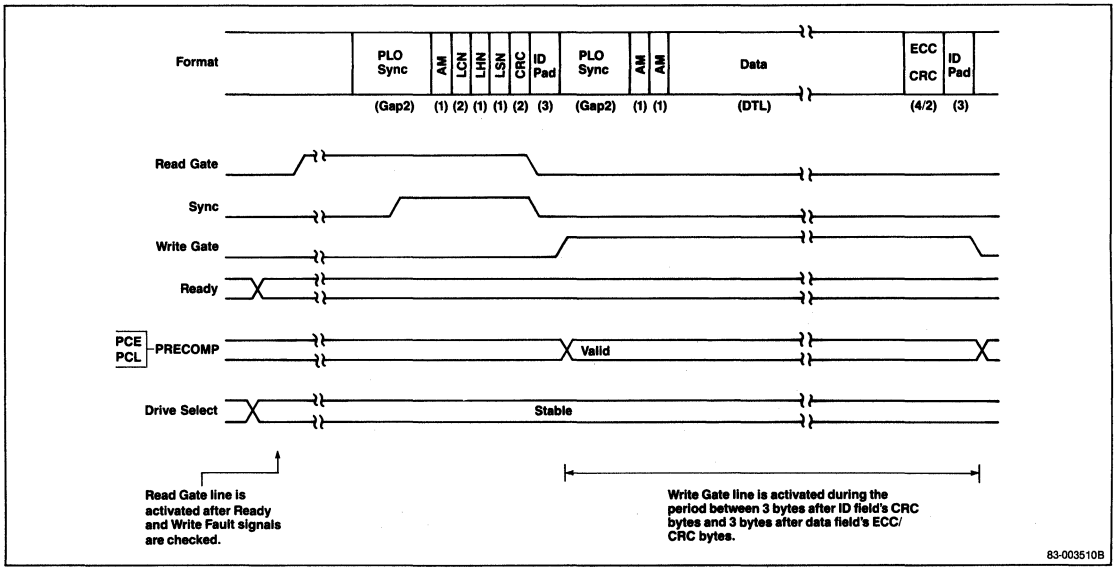


Figure 22. "Data Write" Timing (Soft Sector)



6

μPD7262
Enhanced Small-Disk Interface Controller

Description

The μPD7262 enhanced small-disk interface controller (ESDIC) is a hard-disk drive (HDD) controller capable of supporting up to seven HDDs. It is a single-chip solution to ESDI controller design and conforms to ANSI Specification X3T9.3/1987, revision F.

Note: A control sequence that changes the state of the write gate (WGATE) signal to function as the write start signal for the ID field's phase-locked oscillator (PLO) area for hard-sector formatting is covered in the ANSI specification, but it is not supported by the μPD7262.

The μPD7262 can be controlled by a general bus like the one provided by the V-Series family. It has 27 powerful commands and its control interface significantly reduces host processor overhead for HDDs for both software and hardware. This simplifies interfacing.

The μPD7262 uses the group drive concept to control up to seven HDDs divided into a maximum of three groups. Each group may be designated arbitrarily according to common control parameters such as data length per sector, number of sectors per track, and error correction/detection.

Features

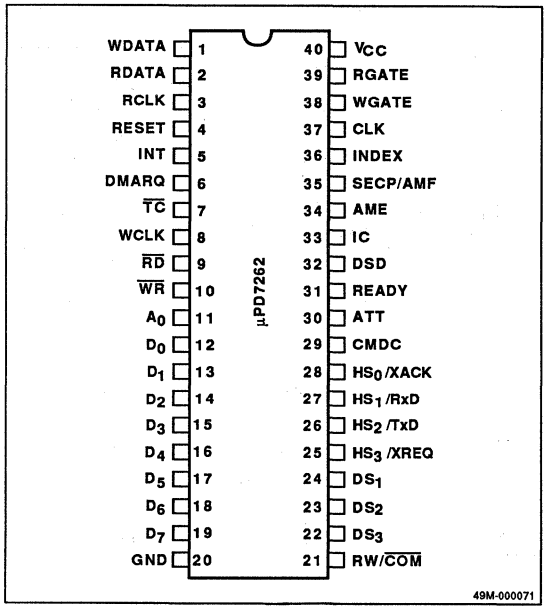
- Serial mode ESDI-compatible
- Capable of controlling up to seven disk drives
- Supports up to 80 heads (5 groups of 16) for each disk drive
- Hard- and soft-sector interfacing
- Programmable track format
  - — Variable byte synchronization patterns: ABSP and DBSP
  - — Variable data length: 128 to 65,536 bytes/sector
  - — Variable gap length
    - Intersector gap
    - PLO sync field
    - Format speed tolerance gap
- Selectable sector start signal: sector pulse/address mark found
- Maximum clock frequency
  - — 18 MHz (7262-18)
  - — 12 MHz (7262-12)
- 22 disk commands available
- Parallel seek operation capability
- Multisector, multitrack, and multicylinder functions
- Implied seek function
- Data scan/verify function
- Data read function from sectors with errors
- Skew function
- CRC/ECC selection
- NMOS technology
- Single +5 V power supply
- 40-pin ceramic DIP

Ordering Information

Part Number	Max Frequency	Package
μPD7262D18	18 MHz	40-pin ceramic DIP
μPD7262D12	12 MHz	

Pin Configuration

40-Pin Ceramic Dip



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Pin Identification

Symbol	I/O	Function
Host System Interface		
A_0	In	Address 0 (register select); selects a register or the data FIFO.
D_0-D_7	I/O	Three-state bidirectional data bus.
DMARQ	Out	DMA request
INT	Out	Interrupt request; indicates completion of command execution by the μPD7262 or completion of a seek operation by a disk drive.
$\overline{RD}$	In	Controls reading data or status from the μPD7262: active low.
$\overline{TC}$	In	Terminal count; indicates completion of data transfer; active low.
$\overline{WR}$	In	Controls writing data or commands to the μPD7262; active low.
Disk Drive Interface		
AME	Out	Address mark enable; causes the disk drive to write or to search for an address mark.
AMF	In	Address mark found; indicates the beginning of a sector in a soft-sector type of disk drive.
ATT	In	Attention; requests receipt of the standard status byte issued by the disk drive.
CMDC	In	Command complete; indicates that the disk drive has completed the execution of a serial command and is able to receive the next command.
DS_3-DS_1	Out	Drive select 3, 2, 1; binary encoded outputs that select a disk drive.
DSD	In	Drive selected; indicates that the disk drive specified with DS_3-DS_1 is selected.
HS_3-HS_0	Out	Head select 3, 2, 1, 0; binary encoded outputs that select a read/write head; see RW/$\overline{COM}$ below.
INDEX	In	Indicates detection of the index mark in the drive.
RCLK	In	Read clock that samples RDATA during read operations; also the reference clock that determines the WCLK frequency during write operations.
RDATA	In	Read data (NRZ) from the disk drive.
READY	In	Indicates the disk drive's ready state.
RGATE	Out	Read gate; signals the disk drive to read data.
RW/$\overline{COM}$	Out	Read-write/communicate; determines the function of pins 25-28.

	RW/$\overline{COM}$	
Pin	1	0
25	HS_3	XREQ
26	HS_2	TxD
27	HS_1	RxD
28	HS_0	XACK

Pin Identification (cont)

Symbol	I/O	Function
RxD	In	Receive data; receives configuration/status from the disk drive; see RW/$\overline{COM}$ above
SECP	In	Sector pulse; indicates the beginning of a sector in a hard-sector type of disk drive.
TxD	Out	Transmit data; transmits a serial command to the disk drive; see R/W/$\overline{COM}$ above.
WCLK	Out	Write clock synchronized with WDATA.
WDATA	Out	Writes data (NRZ) to the disk drive.
WGATE	Out	Write gate; signals the disk drive to write data.
XACK	In	Transfer acknowledge; acknowledgment by the disk drive to a request for command or configuration/status transfer; see RW/$\overline{COM}$ above.
XREQ	Out	Transfer request; requests a command or configuration/status transfer by the disk drive; see RW/$\overline{COM}$ above.
Circuit Control		
CLK	In	Single-phase system clock; the frequency must be between 0.7 and 1.8 times the RCLK frequency and the clock signal must be input continuously.
RESET	In	Clears the internal circuits of the μPD7262.
TM	In	Test mode; this pin should be grounded for normal operation; the ground is removed for test mode operation.
GND	In	Ground.
V_{CC}	In	+5-volt power supply.

Standard Signal Names

Tables 1 and 2 show the conversion between the μPD7262 pin symbols and the ESDI standard signal names.

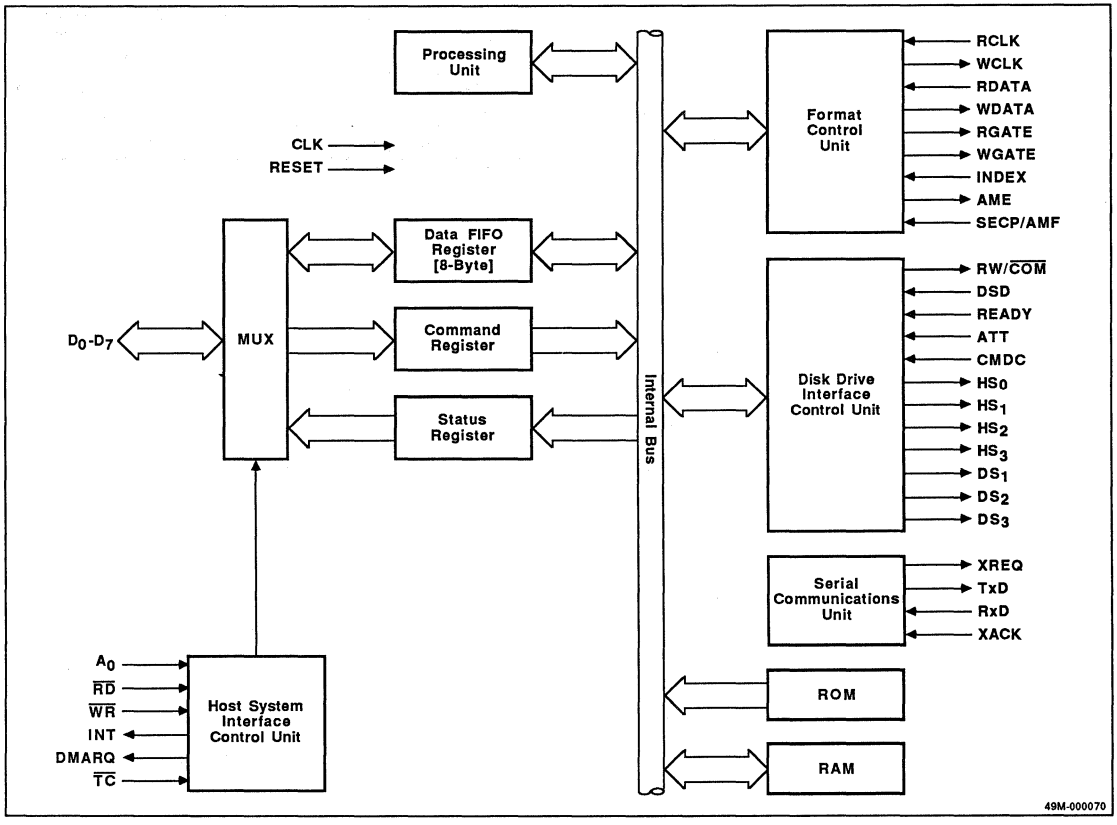
Table 1. Control Cable Connections With μPD7262

Symbol	ESDI Signal Name
DS_1-DS_3	Drive select 1-3
HS_0-HS_3	Head select 2(0)-2(3)
XREQ	Transfer request
XACK	Transfer acknowledge
TxD	Command data
RxD	Configuration/status data
READY	Ready
WGATE	Write gate
RGATE	Read gate

Table 2. Data Cable Connections With μPD7262

Pin Symbol	ESDI Signal Name
WDATA	± NRZ write data
RDATA	± NRZ read data
RCLK	± Read/reference clock
WCLK	± Write clock
CMDC	Command complete
DSD	Drive selected
AME	Address mark enable
SECP	Sector pulse
AMF	Address mark found
INDEX	Index

μPD7262 Block Diagram



Absolute Maximum Ratings

T_A = +25°C

Operating temperature, T_{OPT}	−10.0 to +70°C
Storage temperature, T_{STG}	−65.0 to +150°C
Output voltage, V_O	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to +7.0 V
Supply voltage, V_{CC}	−0.5 to +7.0 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Capacitance

T_A = +25°C; V_{CC} = GND = 0 V

Parameter	Symbol	Typ	Max	Unit	Conditions
Input capacitance	C_I		15	pF	f = 1 MHz; unmeasured pins tied to GND.
Output capacitance	C_O		15	pF	
Input/output capacitance	C_{IO}		20	pF	

DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input voltage, low 1	V_{IL1}	−0.5		+0.8	V	All except CLK, RCLK
Input voltage, low 2	V_{IL2}	−0.5		+0.6	V	CLK, RCLK
Input voltage, high 1	V_{IH1}	+2.2		V_{CC} + 0.5	V	All except CLK, RCLK
Input voltage, high 2	V_{IH2}	+3.3		V_{CC} + 0.5	V	CLK, RCLK
Output voltage, low	V_{OL}			+0.4	V	I_{OL} = +2.0 mA
Output voltage, high 1	V_{OH1}	+2.4			V	I_{OH} = −100 μA; all except pins 21-33
Output voltage, high 2	V_{OH2}	+2.4			V	I_{OH} = −50 μA; pins 21-33
Input leakage current 1	I_{LI1}			±10	μA	V_I = 0.45 V to V_{CC}; all except pins 21-33
Input leakage current 2	I_{LI2}			−700	μA	V_I = 0.45 V to V_{CC}; pins 21-33
Output leakage, current	I_{LO}			±30	μA	V_O = 0.45 V to V_{CC}
Supply current	I_{CC}		250	350	mA	

AC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5$ V ±10%; see figure 1 for timing measurement thresholds.

Parameter	Figure	Symbol	7262-18 Min	7262-18 Max	7262-12 Min	7262-12 Max	Unit	Conditions
Host System Interface								
CLK cycle	2	t_{CY}	55	10,000	83	10,000	ns	
CLK width, high	2	t_{CH}	20		30		ns	
CLK width, low	2	t_{CL}	20		30		ns	
CLK rise time	2	t_{CR}		10		10	ns	
CLK fall time	2	t_{CF}		10		10	ns	
A_0 setup to $\overline{RD}\downarrow$	5	t_{AR}	0		0		ns	
A_0 hold from $\overline{RD}\uparrow$	5	t_{RA}	0		0		ns	
$\overline{RD}$ pulse width	5	t_{RR}	100		100		ns	
Data delay from A_0	5	t_{AD}		85		85	ns	
Data delay from $\overline{RD}\downarrow$	5	t_{RD}		85		85	ns	
Data float delay from $\overline{RD}\uparrow$	5	t_{RDF}	0	75	0	75	ns	
A_0 setup to $\overline{WR}\downarrow$	6	t_{AW}	0		0		ns	
A_0 hold from $\overline{WR}\uparrow$	6	t_{WA}	0		0		ns	
$\overline{WR}$ pulse width	6	t_{WW}	100		100		ns	
Data setup to $\overline{WR}\uparrow$	6	t_{DW}	55		55		ns	
Data hold from $\overline{WR}\uparrow$	6	t_{WD}	5		5		ns	
Recovery time from $\overline{RD}\uparrow$ or $\overline{WR}\uparrow$	5, 6	t_{RV}	70		70		ns	
INT delay from $\overline{WR}\uparrow$	6	t_{WI}		200		200	ns	
DMARQ delay from $\overline{WR}\uparrow$	8	t_{WRQ}		125		125	ns	
DMARQ delay from $\overline{RD}\uparrow$	7	t_{RRQ1}		160		160	ns	During disk read operation
DMARQ delay from $\overline{RD}\downarrow$	7	t_{RRQ2}		100		120	ns	After disk read operation
$\overline{TC}$ pulse width	4	t_{TT}	80		80		ns	
$\overline{TC}$ delay from $\overline{RD}\downarrow$ or $\overline{WR}\downarrow$	4	t_{RWT}	80		80		ns	
$\overline{RD}\uparrow$ or $\overline{WR}\uparrow$ delay from $\overline{TC}\downarrow$	4	t_{TRW}	80		80		ns	
RESET pulse width	3	t_{RES}	100		100		t_{CY}	
Disk Drive Interface								
RCLK cycle	9	t_{RCY}	55	10,000	83	10,000	ns	
RCLK width, high	9	t_{RCH}	0.40		0.40		t_{RCY}	
RCLK width, low	9	t_{RCL}	0.40		0.40		t_{RCY}	
RCLK rise time	9	t_{RCR}		8		8	ns	
RCLK fall time	9	t_{RCF}		8		8	ns	
Data setup to RCLK↑	9	t_{RDRC}	15		15		ns	
Data hold from RCLK↑	9	t_{RCRD}	15		15		ns	
WCLK cycle	10	t_{WCY}	0.95	1.05	0.95	1.05	t_{RCY}	
WCLK width, high	10	t_{WCH}	0.25	0.75	0.25	0.75	t_{RCY}	
WCLK width, low	10	t_{WCL}	0.25	0.75	0.25	0.75	t_{RCY}	

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AC Characteristics (cont)

Parameter	Figure	Symbol	7262-18 Min	7262-18 Max	7262-12 Min	7262-12 Max	Unit	Conditions
Disk Drive Interface (cont)								
WCLK rise time	10	t_{WCR}		10		10	ns	
WCLK fall time	10	t_{WCF}		10		10	ns	
Data setup to WCLK↑	10	t_{WDWC}	0.20		0.20		t_{RCY}	
Data hold from WCLK↑	10	t_{WCWD}	0.20		0.20		t_{RCY}	
RGATE↑ delay from AMF↑	13	t_{AFRG}		300		300	ns	
AME↓ delay from AMF↓	13	t_{AFAE}	0		0		ns	
SECP pulse width	12	t_{SEPF}	400		400		ns	
INDEX pulse width	11	t_{IDXF}	400		400		ns	
WGATE setup to AME↑	16	t_{WGAE}	440		440		ns	
WGATE hold from AME↓	16	t_{AEWG}	440		440		ns	
WGATE mask time	16	t_{WGM}	8		8		t_{RCY}	Immediately after ADR PAD field
Communication setup RW/$\overline{COM}$↓	17	t_{CC}	830		830		ns	
HS_1-HS_0 float delay from RW/$\overline{COM}$↓	17	t_{CHF}		50		50	ns	
HS_3-HS_0 output delay from RW/$\overline{COM}$↑	17	t_{RWH}		50		50	ns	
TxD setup to XREQ	14	t_{TDXR}	50		50		ns	1-bit transmit
TxD hold from XREQ	14	t_{XRTD}	0	2 t_{CY} + 400	0	2 t_{CY} + 400	ns	
XACK delay from XREQ	14	t_{XRXAT}	0		0		ns	
XREQ delay from XACK	14	t_{XAXRT}	50	19 t_{CY} + 300	50	19 t_{CY} + 300	ns	
RxD setup to XACK	15	t_{RDXA}	50		50		ns	1-bit receive
RxD hold from XACK	15	t_{XARD}	0		0		ns	
XACK delay from XREQ	15	t_{XRXAR}	0		0		ns	
XREQ delay from XACK	15	t_{XAXRR}	50	19 t_{CY} + 300	50	19 t_{CY} + 300	ns	

Figure 1. AC Test Points

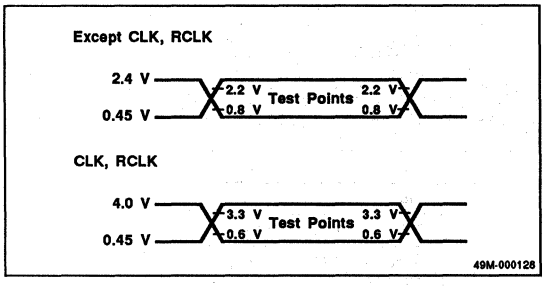

Figure 2. CLK Pulse Timing

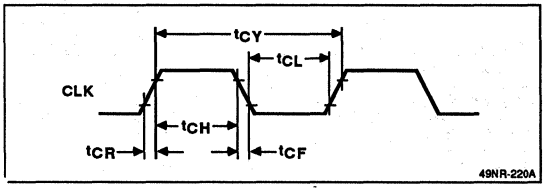

Figure 3. Reset Pulse Timing

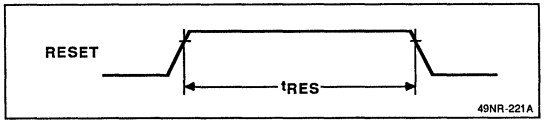

Figure 4. TC Pulse Timing

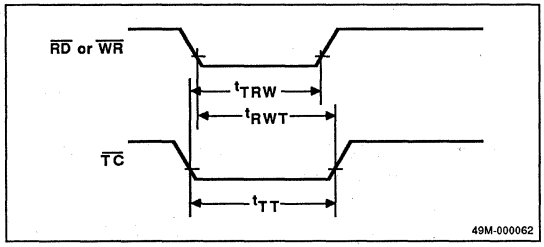

Figure 5. Read Timing

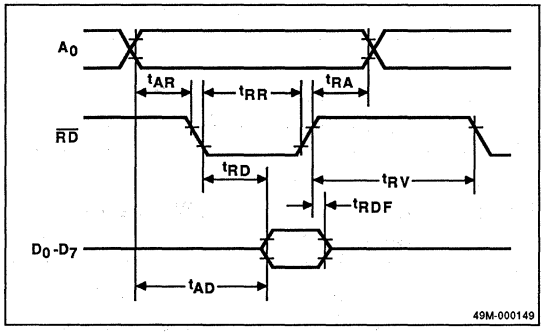

Figure 6. Write Timing

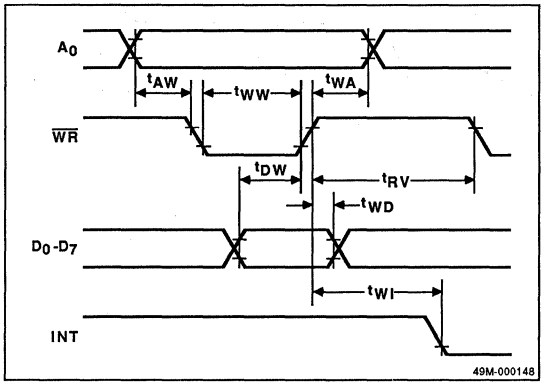

Figure 7. DMA Read Timing

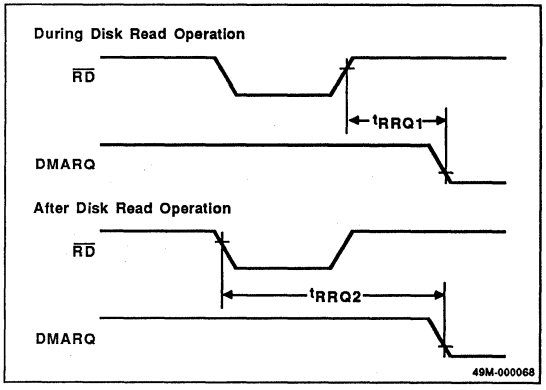

Figure 8. DMA Write Timing

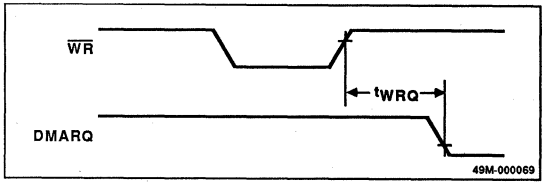

Figure 9. Data Read Timing

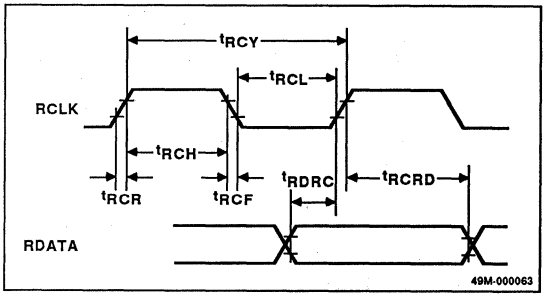

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Figure 10. Data Write Timing

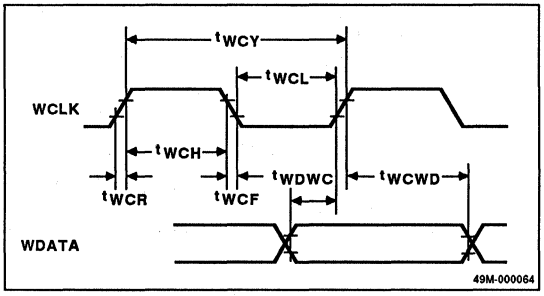


Figure 11. Index Timing

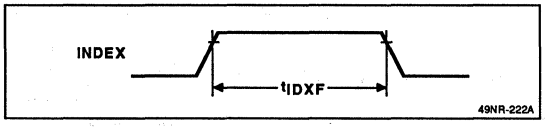


Figure 12. Sector Timing

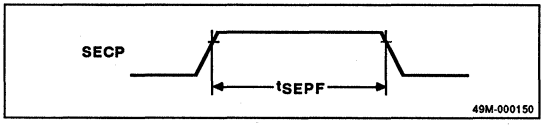


Figure 13. Address Mark Found/Read Gate Timing

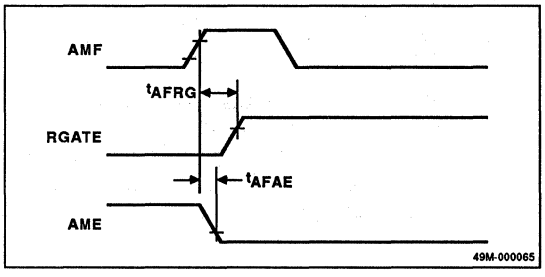


Figure 14. One-Bit Transfer Timing (to Drive)

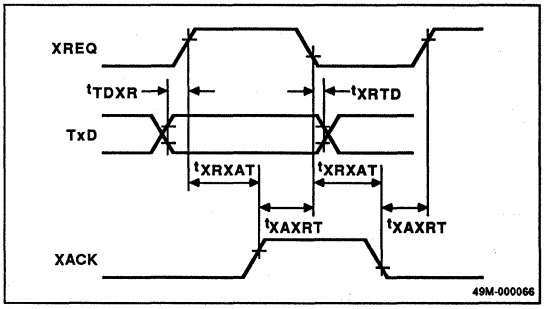


Figure 15. One-Bit Transfer Timing (from Drive)

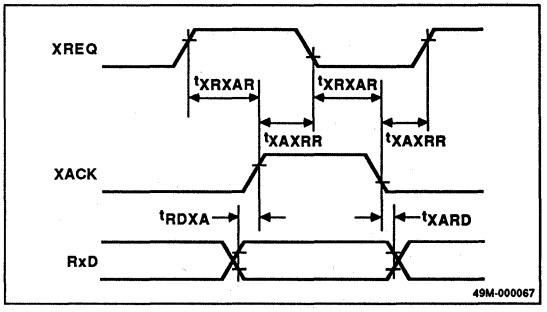


Figure 16. Address Mark Enable/Write Gate Timing

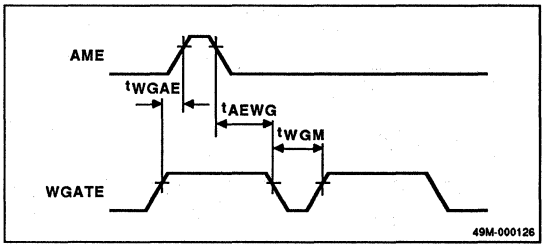
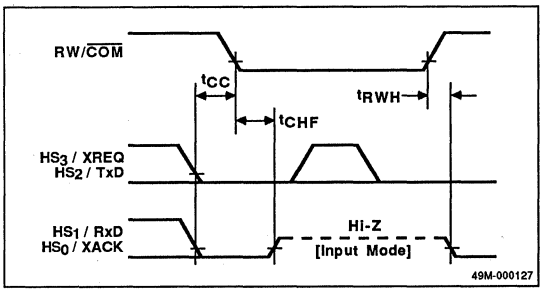


Figure 17. Communications Timing



ARCHITECTURE

Refer to the block diagram of the μPD7262.

Processing Unit

The processing unit decodes commands sent from the host system to control internal units, such as the format control unit, and then generates the result status.

Read Only Memory (ROM)

The ROM contains the firmware necessary for executing commands sent from the host system.

Random Access Memory (RAM)

The RAM is used to temporarily store parameters required by the firmware for command execution.

Command Register

The host system sends disk commands and subcommands via the data bus to the command register. The command register is selected by signal A_0 going high and signal $\overline{WR}$ going low. The contents of the data bus can then be transferred into the command register. The host system cannot read data in the command register. It is a write-only register.

Status Register (STR)

The status register reports the internal status of the μPD7262 to the host system. Data from the host system cannot be transferred into the read-only status register. Status register selection is performed when signal A_0 goes high and signal $\overline{RD}$ goes low, enabling the register contents to be output onto the data bus. The host system can select and read the contents of the status register any time. The status register can be cleared to 00H by the CHIP RESET subcommand or by the RESET signal. Status register bits D7-D0 are described in Table 3.

Table 3. Status Register (STR) Bit Definitions

Bit	Status Name	Function
D7	Controller Busy (CB)	Indicates that the μPD7262 is executing a disk command. The CB bit is set upon disk command execution and cleared when execution is completed. While the CB bit is set, the host system cannot send a new disk command.
D6, D5	Command End (CEH, CEL)	Indicates that the disk command execution is completed. Both CEH and CEL bits can be cleared by a reset signal, by sending the next disk command or clear command end bit, or by a chip reset subcommand from the host system. Combinations of the different states of bits D6,D5 are listed below. (0,0) indicates no disk command has been sent from the host system during disk command execution or after a reset signal input or clear command end bit or chip reset subcommand. (0,1) indicates disk command execution was aborted. (1,0) indicates disk command execution was successful. (1,1) indicates the disk command sent from the host system is invalid for any of the following reasons. • The group assign command is not sent after reset. • G1,G0 = 0,0 is specified by the specify 2 command. • A command word high (CWH) or command word low (CWL) not supported by the send command is specified. • An internal information selection (IIS) not specified by the get internal information command is specified.
D4	Sense Seek Request (SRQ)	When a disk drive seek operation is completed, bit D4 is set to request a sense seek status command from the host system. This bit is not reset by a mask SRQ interrupt subcommand.
D3	Reset Request (RRQ)	When set, bit D3 requests an immediate reset of the μPD7262.

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Table 3. Status Register (STR) Bit Definitions (cont)

Bit	Status Name	Function
D2	ID/Data Error (IDE)	Bit D2 is set when a CRC error is detected in the ID field during execution of an ID field read command (read ID, verify ID). Bit D2 is also set when a CRC/ECC error is detected in the data field during execution of a data field read command (read data, check, scan, verify data, read diagnostic).
D1	Not Coincident (NCI)	Bit D1 is set if the ID or data transferred from the host system does not match that on the sector during execution of the verify ID or verify data command, or if sector data that matches the data transferred from the host system cannot be detected during execution of the scan command.
D0	Interface Fault (IFLT)	Bit D0 indicates that a transfer of 17 bits of serial communications data from the falling edge of XREQ to the rising edge of the 17th XACK has not occurred within a specified time period 480 x TIME x COMT, or indicates a timeout of the CMDC signal.

Data FIFO Register

The data FIFO (first-in, first-out) 8 x 8-bit register is used to store temporarily—asynchrouous with the system clock—commands, parameters, read/write data, and the result status transferred between the μPD7262 and the host system.

When executing a disk command, the μPD7262 first loads the parameters, then clears the data FIFO register before executing the command. The data FIFO register can store only eight bytes of data; the ninth and successive bytes are not accepted if the FIFO is full.

Host System Interface Control Unit

This unit controls the interface between the host system and the μPD7262.

Read/Write Control. The read/write control circuit selects the command/status register or data FIFO register by decoding the read ($\overline{RD}$), write ($\overline{WR}$), and address (A_0) signals, which are output from the host system. The internal registers are selected as shown in table 4.

Table 4. Register Selection

A_0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read data FIFO register
0	1	0	Write data FIFO register
1	0	1	Read status register
1	1	0	Write command register
x	1	1	Non-select

Interrupt Request Control. The interrupt request control circuit outputs the interrupt request (INT) to the host system.

When disk command execution terminates, or when the SRQ bit in the status register is set, this control circuit sets the INT signal to active (high) level. The INT signal returns to inactive (low) level when the host system writes a clear command end bit subcommand to the μPD7262.

Note that the INT signal caused by SRQ cannot be reset with the clear command end bit subcommand; the sense interrupt status command should be used to reset INT.

DMA Request Control. The DMA request control circuit processes DMA requests (DMARQ) to the host system.

During disk command execution, when a DMA transfer is required between the memory and the μPD7262, or between the memory and the disk drive via the μPD7262, this control circuit sets the DMARQ signal to active (high) level. The conditions under which this control circuit sets the DMARQ signal active are defined as follows according to the number of bytes of data stored in the data FIFO register.

(1) μPD7262 → memory data transfer: Read ID, read diagnostic, and read data commands. When data is being sent to the memory after it is read from the data FIFO register, the DMARQ signal is set active. The DMARQ signal is also set active when a single byte remains in the data FIFO register immediately before normal termination of a command; that is, directly before an interrupt is generated.

(2) Memory → μPD7262 data transfer: Write format, verify ID, scan, verify data, and write data commands. When data is sent to the data FIFO register after being read from memory, if the data FIFO register contains 6 or fewer bytes of data, the DMARQ signal is set active.

The DMARQ will not become active when one of the following conditions occurs.

(1) Disk command execution is aborted (abnormal termination).

(2) Data in all sectors specified by the sector count parameter (SCNT) has been transferred by a successful command execution (normal termination).

(3) Terminal count signal ($\overline{TC}$) from the host system is set active.

TC Control. The terminal count control circuit halts operation of the host system control unit in accordance with the terminal count input ($\overline{TC}$) from the host system.

Disk Drive Interface Control Unit

Under control of the processing unit, the disk drive interface control unit outputs head and unit addresses as well as control signals.

Signals indicating the status of the disk drive are directly input to this unit.

Serial Communications Unit

Under control of the processing unit, the serial communications unit performs data transfers to or from a disk drive in handshaking mode. Also, the serial communications unit generates and checks parity.

Format Control Unit

Under control of the processing unit, the format control unit writes data to the disk drive or reads data from the disk drive according to the specified track format. The unit provides the following functions:

- Encoding/decoding of FM and MFM data
- Phase-shift compensation during read operation
- Serial-to-parallel or parallel-to-serial conversion
- Address mark writing and detection
- Data transfer control
- Check code generation, error detection, and correction

RESET

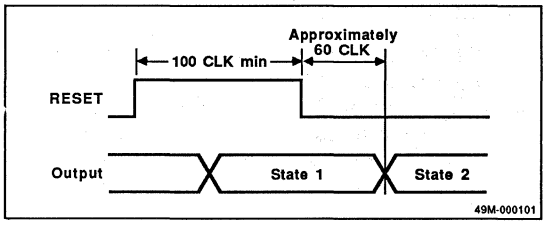
If 100 or more CLK cycles are continuously input to the CLK and RCLK pins while the RESET pin is high, the μPD7262 clears all its internal registers and enters the idle state.

Table 5 indicates the status of the input/output pins during the reset state and 60 CLK cycles after the reset has been released. See figure 18.

Table 5. Effect of Reset on I/O Pin Status

Pin Symbol	Reset, State 1	After Reset, State 2
WDATA	High impedance	High impedance
INT	Low	Low
DMARQ	Low	Low
WCLK	CLK output	CLK output
D_7-D_0	High impedance	High Impedance
RW	High	High
DS_3-DS_1	High	High
HS_3/XREQ	High	Low
HS_2/TxD	High	Low
HS_1/RxD	High	Low
HS_0/XACK	High	Low
AME	Low	Low
WGATE	Low	Low
RGATE	Low	Low

Figure 18. Reset State Timing



ERROR DETECTION AND CORRECTION

The μPD7262 has a cyclic redundancy check (CRC) function and two error correction code (ECC) functions as shown in table 6.

Table 6. CRC and ECC Error Detection

Function		Polynomial Generator Formula	Bytes/ Sector
CRC		$X^{16} + X^{12} + X^5 + 1$	2
ECC	32 bits	$(X^{21} + 1)(X^{11} + X^2 + 1)$	4
	56 bits	$(X^{22} + 1)(X^{11} + X^7 + X^6 + X + 1)$ $(X^{11} + X^9 + X^7 + X^6 + X^5 + X + 1)$ $(X^{12} + X^{11} + X^{10} + X^9 + X^8 +$ $X^7 + X^6 + X^5 + X^4 + X^3 + X^2 + X + 1)$	7

Each ECC function has its own error correction function, the performance of which is shown in table 7. In cases where the error burst length exceeds the 11-bit maximum, the detection performance of the 56-bit ECC is better than that of the 32-bit ECC by a factor of 10^7.

Table 7. ECC Error Correction Performance

ECC	Maximum Single Error Burst Length	Maximum Sector Data Length
32-bit	11 bits	5369 bytes
56-bit	11 bits	64K bytes

SKEW FUNCTION

When the skew (SK) function is specified in the disk command parameter during access of a hard-sector disk, the μPD7262 shifts the address area. This area, located after the address byte sync pattern (ABSP), is delayed 64 bytes, thus stretching the Gap 1 Length (GP1L).

This function is effective when a media defect exists in the address area of a disk. However, the sector length is decreased by 64 bytes. A sector formatted in this manner must be accessed in the skew access mode.

COMMANDS

The μPD7262 has 22 disk commands for data read/write, seek, serial communications operations, etc., Four subcommands are used for controlling the internal status of the μPD7262. The controller is always ready to accept a subcommand. However, if the μPD7262 executes a disk command while already busy (CB = 1), it disables other disk commands.

Disk subcommands must be executed individually, not as a group.

Disk Command Operation Phases

The μPD7262 executes disk commands sent from the host system in three distinct phases.

Command Phase (C-Phase). When the μPD7262 is in the idle state (CB = 0), the host system sends command parameters to the data FIFO register in the order specified for each command. It then writes the command code to the command register. The following disk commands have no command parameters: detect error, sense unit status, sense seek status, and recalibrate.

Execution Phase (E-Phase). The μPD7262 executes the disk commands specified by the command parameters.

Result Phase (R-Phase). The μPD7262 places the result information into the data FIFO register. After reading the contents of the status register, the host system reads the number of result bytes specified for the disk command, as required by the user, from the data FIFO register.

For certain disk command operations—such as read, write, and scan—a value that was updated during command execution will be set into an R-phase parameter with the same name as the parameter in the C-phase so that it may be used by subsequent commands. The following commands have no result parameters: specify 0, 1, and 2.

Disk Command Set

The 22 commands and four subcommands are described in the following tables.

Table	Description
8	Disk command groups
9	Disk command operations
10	Disk command parameters
11	Disk subcommands

Table 8. Disk Command Groups

Group	Command	Description
Initialize	Group assign	Assigns group numbers to each of seven drives
	Specify 0	Sets the timer constants.
	Specify 1, Specify 2	Sets operation parameters for the drive group.
	Get internal information	Reads set parameters specified by group assign and specify 0-2 commands.
Send	Send	Sends serial commands to the specified drive.
	Send extended	Sends serial commands to the specified drive (used when ESDI command is expanded).
Sense	Sense seek status	Reads the completion status of seek operations at drives.
	Sense unit status	Reads the drive status.

Table 8. Disk Command Groups (cont)

Group	Command	Description
Seek	Recalibrate	Positions the read/write head to track 0.
	Physical seek	Positions the read/write head to a specified physical cylinder.
	Logical seek	Positions the read/write head to a specified logical cylinder.
Write	Write track format	Writes track format for each track to a maximum of 65,536 tracks.
	Write sector format	Specifies a starting sector and writes format on each sector to a maximum of one track.
	Write data	Specifies a sector and transfers the host processor's data for that sector.

Table 8. Disk Command Groups (cont)

Group	Command	Description
Read	Read ID	Transfers the sector ID to the host processor.
	Read data	Specifies a sector and transfers the sector data to the host processor.
	Read diagnostic	Transfers data to the host processor without reading ID.
	Verify ID	Verifies ID on the track with the host processor's data.
	Check	Specifies a sector to check for sector data error.
	Scan	Compares data sector-by-sector with host processor's data to detect the matching sector.
Error handling	Detect error	Generates error correction code (ECC) information.

Table 9. Disk Command Operations

				Parameters								
Command	Phase	A_0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Group assign	Command	0	W				GN1					
		0	W				GN2					
		0	W				GN3					
		0	W				GN4					
		0	W				GN5					
		0	W				GN6					
		0	W				GN7					
		1	W	0	0	1	0	0	1	0	0	
	Result	1	R				STR					
		0	R				EST					
Specify 0	Command	0	W				TIME					
		0	W				COMT					
		0	W				CETH					
		0	W				CETL					
		1	W	0	0	1	0	1	0	0	0	
	Result	1	R				STR					
Specify 1	Command	0	W				MODE					See figure 19.
		0	W				DTLH					
		0	W				DTLL					
		0	W				ESN					
		0	W				COH					
		0	W				COL					
		1	W	0	0	1	0	1	0	G1	G0	
	Result	1	R				STR					

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Table 9. Disk Command Operations (cont)

Command	Phase	A_0	R/W	Parameters D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Specify 2	Command	0	W				ABSP					
		0	W				DBSP					
		0	W				GPIL					
		0	W				PLOL					
		0	W				GP2L					
		0	W				EHN					EHN byte can be omitted.
		1	W	0	0	1	0	1	1	G1	G0	
	Result	1	R				STR					
Get internal information	Command	0	W				IIS					See figure 20.
		1	W	0	0	1	0	0	0	0	0	
	Result	1	R				STR					IIS determines the number of bytes
		0	R				IIF1					
		0	R				IIF2					
		0	R				IIF3					
		0	R				IIF4					
		0	R				IIF5					
		0	R				IIF6					
		0	R				IIF7					
Send	Command	0	W				CWH					See figure 21.
		0	W				CWL					
		1	W	0	0	1	1	1	DS3	DS2	DS1	
	Result	1	R				STR					
		0	R				EST					
		0	R				RDTH					Specified depending on CWH.
		0	R				RDTL					
Send extended	Command	0	W				TMOD					See figure 22.
		0	W				CWH					
		0	W				CWL					
		1	W	0	1	0	0	1	DS3	DS2	DS1	
	Result	1	R				STR					
		0	R				EST					
		0	R				RDTH					Specified depending on TMOD.
		0	R				RDTL					
Sense seek status	Command	1	W	0	0	0	1	0	0	0	0	
	Result	1	R				STR					
		0	R				SCST					
		0	R				SEST					
		0	R				SBST					

Table 9. Disk Command Operations (cont)

Command	Phase	A_0	R/W	Parameters D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Sense unit status	Command	1	W	0	0	1	1	0	DS3	DS2	DS1	
	Result	1	R				STR					
		0	R				EST					
		0	R				DST					See figure 23.
		0	R				SSTH					
		0	R				SSTL					
Recalibrate	Command	1	W	0	1	0	1	0	DS3	DS2	DS1	
	Result	1	R				STR					
		0	R				EST					
Physical seek	Command	0	W	0	0	0	0		PCNH			
		0	W				PCNL					
		1	W	0	1	1	0	0	DS3	DS2	DS1	
	Result	1	R				STR					
		0	R				EST					
Logical seek	Command	0	W				LCNH					
		0	W				LCNL					
		0	W				TCOH					TCOH and TCOL can be omitted
		0	W				TCOL					
		1	W	0	1	1	0	1	DS3	DS2	DS1	
	Execution											Seek operation
	Result	1	R				STR					
		0	R				EST					
Write track format	Command	0	W				PHN					
		0	W				TCTH					
		0	W				TCTL					
		0	W				DPAT					
		1	W	0	1	1	1	0	DS3	DS2	DS1	
	Execution	0	W									Transfers IDs of the sectors on the track.
	Result	1	R				STR					
		0	R				EST					
		0	R				PHN					
		0	R				TCTH					
		0	R				TCTL					
		0	R				DPAT					

Table 9. Disk Command Operations (cont)

Command	Phase	A_0	R/W	Parameters D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Write sector format	Command	0	W	0	0	0	0	0	1	FA	SK	
		0	W	PHN								
		0	W	PSN								
		0	W	DPAT								
		0	W	SCT								
		1	W	0	1	1	1	0	DS3	DS2	DS1	
	Execution	0	W									Transfers IDs of the specified sectors.
	Result	1	R	STR								
		0	R	EST								
		0	R	PHN								
		0	R	PSN								
		0	R	DPAT								
		0	R	SCT								
Verify ID	Command	0	W	PHN								
		0	W	PSN								
		0	W	SCTH								
		0	W	SCTL								
		1	W	1	0	0	0	SK	DS3	DS2	DS1	
	Execution	0	W									Compares ID
	Result	1	R	STR								
		0	R	EST								
		0	R	PHN								
		0	R	PSN								
		0	R	SCTH								
		0	R	SCTL								
Read ID	Command	0	W	PHN								
		0	W	PSN								
		0	W	SCTH								
		0	W	SCTL								
		1	W	1	0	0	1	SK	DS3	DS2	DS1	
	Execution	0	R									Transfers ID
	Result	1	R	STR								
		0	R	EST								
		0	R	PHN								
		0	R	PSN								
		0	R	SCTH								
		0	R	SCTL								

Table 9. Disk Command Operations (cont)

Command	Phase	A_0	R/W	Parameters D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Read data	Command	0	W				LCNH					
		0	W				LCNL					
		0	W				LHN					
		0	W				LSN					
		0	W				FLAG					
		0	W				SCTH					
		0	W				SCTL					
		0	W				PHN					PHN byte can be omitted,
		1	W	1	0	1	1	EC	DS3	DS2	DS1	
	Execution	0	R									Transfers data
	Result	1	R				STR					
		0	R				EST					
		0	R				LCNH					If sector execution is successfull, the logical parameters point to the next sector. If sector execution is not successful, the logical parameters point to the aborted sector.
		0	R				LCNL					
		0	R				LHN					
		0	R				LSN					
		0	R				FLAG					
		0	R				SCTH					
		0	R				SCTL					
Detect error	Command	1	W	0	1	0	0	0	0	0	0	
	Result	1	R				STR					
		0	R				EAOH					See figure 24.
		0	R				EAOL					
		0	R				EPT1					See figure 25.
		0	R				EPT2					
		0	R				EPT3					
Verify data	Command	0	W				LCNH					
		0	W				LCNL					
		0	W				LHN					
		0	W				LSN					
		0	W				FLAG					
		0	W				SCTH					
		0	W				SCTL					
		0	W				PHN					PHN byte can be omitted
		1	W	1	1	1	0	0	DS3	DS2	DS1	
	Execution	0	W									Compares data

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Table 9. Disk Command Operations (cont)

Command	Phase	A_0	R/W	Parameters D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Verify data (cont)	Result	1	R				STR					
		0	R				EST					
		0	R				LCNH					
		0	R				LCNL					
		0	R				LHN					
		0	R				LSN					
		0	R				FLAG					
		0	R				SCTH					
		0	R				SCTL					
Check	Command	0	W				LCNH					
		0	W				LCNL					
		0	W				LHN					
		0	W				LSN					
		0	W				FLAG					
		0	W				SCTH					
		0	W				SCTL					
		0	W				PHN					PHN byte can be omitted.
		1	W	1	1	0	0	0	DS3	DS2	DS1	
	Execution											Data check
	Result	1	R				STR					
		0	R				EST					
		0	R				LCNH					
		0	R				LCNL					
		0	R				LHN					
		0	R				LSN					
		0	R				FLAG					
		0	R				SCTH					
		0	R				SCTL					
Scan	Command	0	W				LCNH					
		0	W				LCNL					
		0	W				LHN					
		0	W				LSN					
		0	W				FLAG					
		0	W				SCTH					
		0	W				SCTL					
		0	W				PHN					PHN byte can be omitted
		1	W	1	1	0	1	0	DS3	DS2	DS1	
	Execution	0	W									Compares data

Table 9. Disk Command Operations (cont)

Command	Phase	A_0	R/W	Parameters D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Scan (cont)	Result	1	R				STR					Last sector to be compared. In the case of NCI, the next to the last sector is to be compared.
		0	R				EST					
		0	R				LCNH					
		0	R				LCNL					
		0	R				LHN					
		0	R				LSN					
		0	R				FLAG					
		0	R				SCTH					
		0	R				SCTL					
Read diagnostic	Command	0	W				PHN					
		0	W				PSN					
		0	W				SCTH					
		0	W				SCTL					
		1	W	1	0	1	0	SK	DS3	DS2	DS1	
	Execution	0	R									Transfers data
	Result	1	R				STR					
		0	R				EST					
		0	R				PHN					
		0	R				PSN					
		0	R				SCTH					
		0	R				SCTL					
Write data	Command	0	W				LCNH					
		0	W				LCNL					
		0	W				LHN					
		0	W				LSN					
		0	W				FLAG					
		0	W				SCTH					
		0	W				SCTL					
		0	W				PHN					PHN byte can be omitted
		1	W	1	1	1	1	0	DS3	DS2	DS1	
	Execution	0	W									Transfers data
	Result	1	R				STR					
		0	R				EST					
		0	R				LCNH					
		0	R				LCNL					
		0	R				LHN					
		0	R				LSN					
		0	R				FLAG					
		0	R				SCTH					
		0	R				SCTL					

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Figure 19. Specify 1 Command

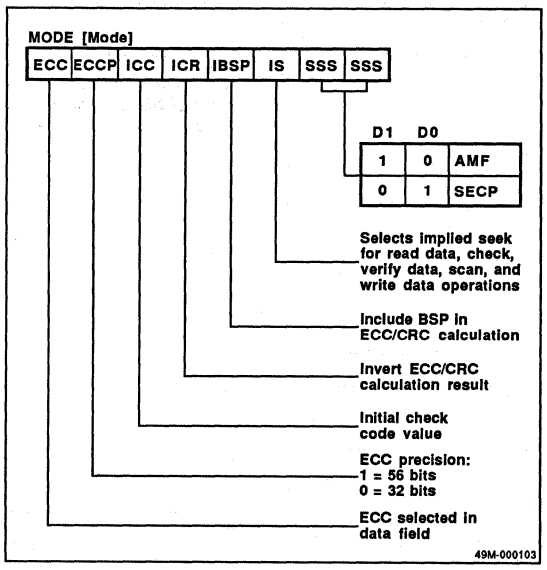

Figure 20. Get Internal Information Command

IIS								IIF	
D7	D6	D5	D4	D3	D2	D1	D0	Contents	# of Bytes
0	0	0	0	X	X	X	X	Group Assign Parameters	7
0	0	0	1	X	X	0	0	Specify 0 Parameters	4
0	0	0	1	X	X	G1	G0	Specify 1 Parameters	6
0	0	1	0	X	X	G1	G0	Specify 2 Parameters	6

49M-000104

Figure 21. Send Command Word High, Low (CWH, CWL)

CWH								CWL							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Command function				Command modifier				0	0	0	0	0	0	0	0
Command function								Command parameter							

49M-000105

Figure 22. Send Extended Command

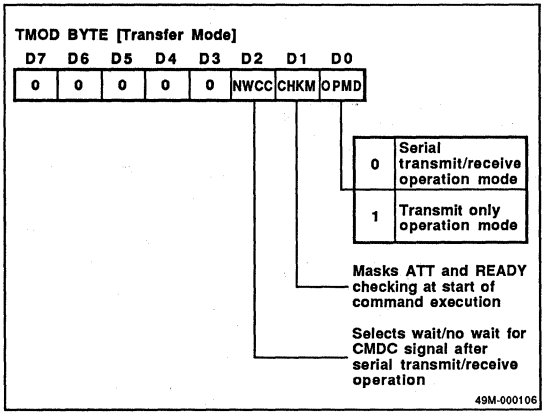

Figure 23. Sense Unit Status Command

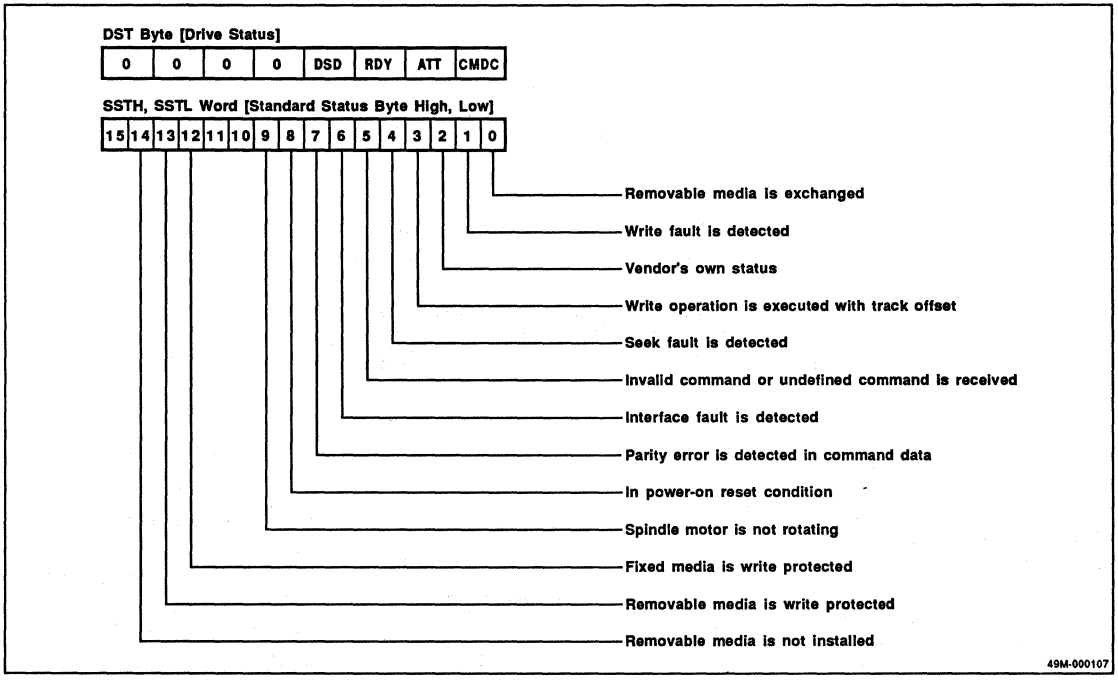

Figure 24. Detect Error Command; Error Address Offset (EAO)

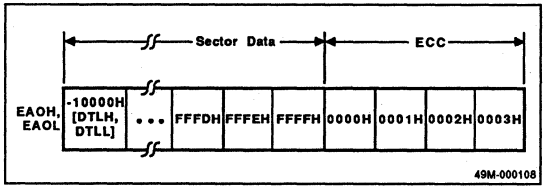

Figure 25. Detect Error Command; Error Pattern (EPT)

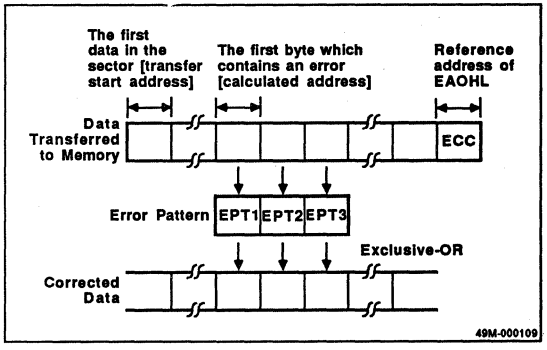

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Table 10. Disk Command Parameters

Parameter	Function
ABSP (Address byte sync pattern)	Specifies the pattern to be synchronized with bytes in an address area.
CETH/CETL (Command end timer high or low)	Specifies the maximum time to wait for the CMDC signal after a serial command is sent to a disk drive. Timer: ts x (CETH, CETL). (If CETH, CETL = 0000, timer = ts x 65,536.)
COH/COL (Cylinder offset high or low)	Specifies the offset value to determine the cylinder to be seeked in an implied or logical seek operator. (COH, COL): 0000 — FFFF.
COMT (Communications timer)	Specifies the maximum time for checking a protocol error during serial communications. Time = ts x COMT (If COMT = 00, time = ts x 256).
CWH/CWL (Command word high or low)	Specifies a μPD7262 serial command code which is sent to a disk drive when executing the send or send extended command.
DBSP (Data byte sync pattern)	Specifies the pattern to sychronize with the bytes in a data area.
DPAT (Data pattern)	Specifies the data pattern to be written to the data field when formatting a sector.
DST (Drive status byte)	Indicates the status of the disk drive status signal.
DS1, DS2, DS3 (Drive select 1, 2, 3)	Specifies a disk drive number.
DTLH/DTLL (Data length high or low)	Specifies the length of a data field. (DTLH, DTLL): 0080 — FFFF (If DTLH, L = 0000, number of bytes = 65,536).
EAOH/EAOL (Error address offset high or low)	Indicates the location of a correctable ECC error by using an offset value from the first ECC byte to the first byte of the ECC error.
EC (Error correction)	Specifies whether or not to generate the ECC error correction pattern when the read data command is executed. When EC = 1, correction pattern is generated.
EHN (End head number)	Specifies the number of the last read/write head to be selected. EHN: 00 — 4F.
EPT1, EPT2, EPT3 (Error pattern 1, 2, 3)	Three-byte data pattern used to correct an ECC error byte.
ESN (End sector number)	Specifies the last sector number within a track. ESN: 0 — FF.
EST (Error status byte)	Indicates the status of the completion of a disk command execution.
FA (Format Address Area)	Specifies formatting to be performed only in the address areas. For hard sector: from leading edge of sector pulse to end of address pad. For soft sector: from beginning of ISG to end of address area.
FLAG (Flag)	Specifies the FLAG pattern within the IDs.
G0, G1 (Group 0, 1)	Specifies a group to set parameters for specify 1 or specify 2 command execution. (Binary encoded.)
GN1-7 (Group number)	Each byte specifies a group number 1, 2, or 3 corresponding to drive 1 through 7, respectively. An FF value indicates that the drive is not connected.
GP1L (Gap 1 length)	Specifies the length of Gap 1 (portion that follows leading edge of index pulse in LSG).
GP2L (Gap 2 length)	Specifies the length of Gap 2 FSTG + (portion that precedes leading edge of index pulse in ISG).
IIF1-7 (Internal information 1-7)	Indicates parameters for operations set in the μPD7262.
IIS (Internal information selection)	Specifies parameters for operations to be read from the μPD7262.

Table 10. Disk Command Parameters (cont)

Parameter	Function
LCNH/LCNL (Logical cyclinder number high or low)	Indicates a logical cylinder number on the media.
LHN (Logical head number)	Indicates a logical head number on the media.
LSN (Logical sector number)	Indicates a logical sector number on the media.
MODE (Mode)	Specifies the operation mode of the μPD7262.
PCNH/PCNL (Physical cylinder number high or low)	Specifies the seek destination cylinder of a physical seek operation. These parameters are retained in the μPD7262 after execution of a command.
PHN (Physical head number)	Specifies the physical head number (PHN ≤ EHN).
PLOL (PLO length)	Specifies the PLO SYNC length.
PSN (Physical sector number)	Indicates a physical sector number.
RDTH/RDTL (Returned data high or low)	Indicates the result status that a drive sends back to the μPD7262 in response to a serial command.
SBST (Seek busy status byte)	Indicates a drive that is in a seek operation. Bits 1-7 correspond to drives 1-7, respectively.
SCST (Seek complete status byte)	Indicates a drive that has completed a seek operation. Bits 1-7 correspond to drives 1-7, respectively.
SCT/SCTH/SCTL (Sector count/sector count high or low)	Indicates the number of sectors to be processed. If SCT = 00, number of sectors = 256. If SCTH, SCTL = 0000, number of sectors = 65,536.
SEST (Seek error status byte)	Indicates a drive in which a seek error has occurred. Bits 1-7 correspond to drives 1-7, respectively.
SK (Skew)	Specifies a skew access operation for hard sector only; see "SKEW FUNCTION" section.
SSTH/SSTL (Standard status byte high or low)	Indicates the standard status of a drive.
STR (Status register)	Indicates the internal status of the μPD7262.
TCTH, TCTL (Temporary count high or low)	Indicates the number of tracks to be formatted. If TCTH, TCTL = 0000, then number of tracks = 65,536.
TCOH/TCOL (Temporary cylinder offset high or low)	Indicates a temporary offset for a logical cylinder number to determine the cylinder to be seeked.
TIME (Time)	Sets the internal reference time (ts) for ESDIC operation. ts = 480 CLK x time. (If time = 0, ts = 480 CLK x 256).
TMOD (Transfer mode)	Specifies the serial communications transmit/receive mode.

Table 11. Disk Subcommands

Subcommand	Description	D7	D6	D5	D4	D3	D2	D1	D0
Chip reset	Resets the μPD7262.	0	0	0	0	0	0	0	1
Clear data FIFO	Clears the FIFO data.	0	0	0	0	0	0	1	0
Mask SRQ interrupt	Masks SRQ interrupt.	0	0	0	0	0	1	0	0
Clear command end bit	Clears a disk command execution (completion condition).	0	0	0	0	1	0	0	0

Result Status

The result status provides information with which the μPD7262 informs the host system of the conditions following a disk command execution. The first result status byte is the error status byte (table 12), which indicates the condition of command termination.

Table 12. Error Status Byte (EST)

Bit No.	Name	Contents
D7	MS/C (Missing seek/ correctable error)	MS is selected when the IDE bit of STR is set to 0, and C is selected when the IDE is 1. When IDE = 0 0 Indicates that an error has occurred in implied seek or multicylinder operation. 1 Indicates that there is no implied seek or multicylinder operation, or that they were executed normally. When IDE = 1 0 A noncorrectable error has occurred. 1 A correctable error has occurred.
D6	OVR (Overrun)	Indicates that the data FIFO has overflowed or underflowed during data transfer operation.
D5	DBY (Drive busy)	Indicates an attempt to transmit a serial command to a disk drive that is executing a serial command.
D4	ATN (Attention)	Indicates detection of an ATT signal from a disk drive.
D3	NR (Not ready)	Indicates that the disk drive is not in the ready state.
D2	ND (Not data)	Indicates that the specified sector is not found.
D1	PE (Parity error)	Indicates that a parity error was detected during serial communications.
D0	MBSP (Missing BSP)	Indicates that the specified BSP is not found.

APPLICATIONS

Interfacing With the System Bus

Figure 26 shows an example of how the μPD7262 interfaces with the system bus. The following types of devices are used.

μPD71071	DMA controller
μPD71082	8-bit latch
μPD71086	8-bit bus transceiver

To prevent access by an external bus during the DMA cycle, the AEN signal of the μPD71071 is used to disable the bus transceivers.

Interfacing With the Disk Drive

Figure 27 shows an example of the interface between the μPD7262 and hard-disk drive. In the example, the external data selector and demultiplexer combination is used to:

- Separate the read/write head select signals
- Output data when executing a read/write disk command
- Control the different signals associated with the serial commands.

The demultiplexer and multiplexer combination provides signals that the disk drives can input or output independent of the drive select signals.

Figure 26. Example of the System Bus Interface

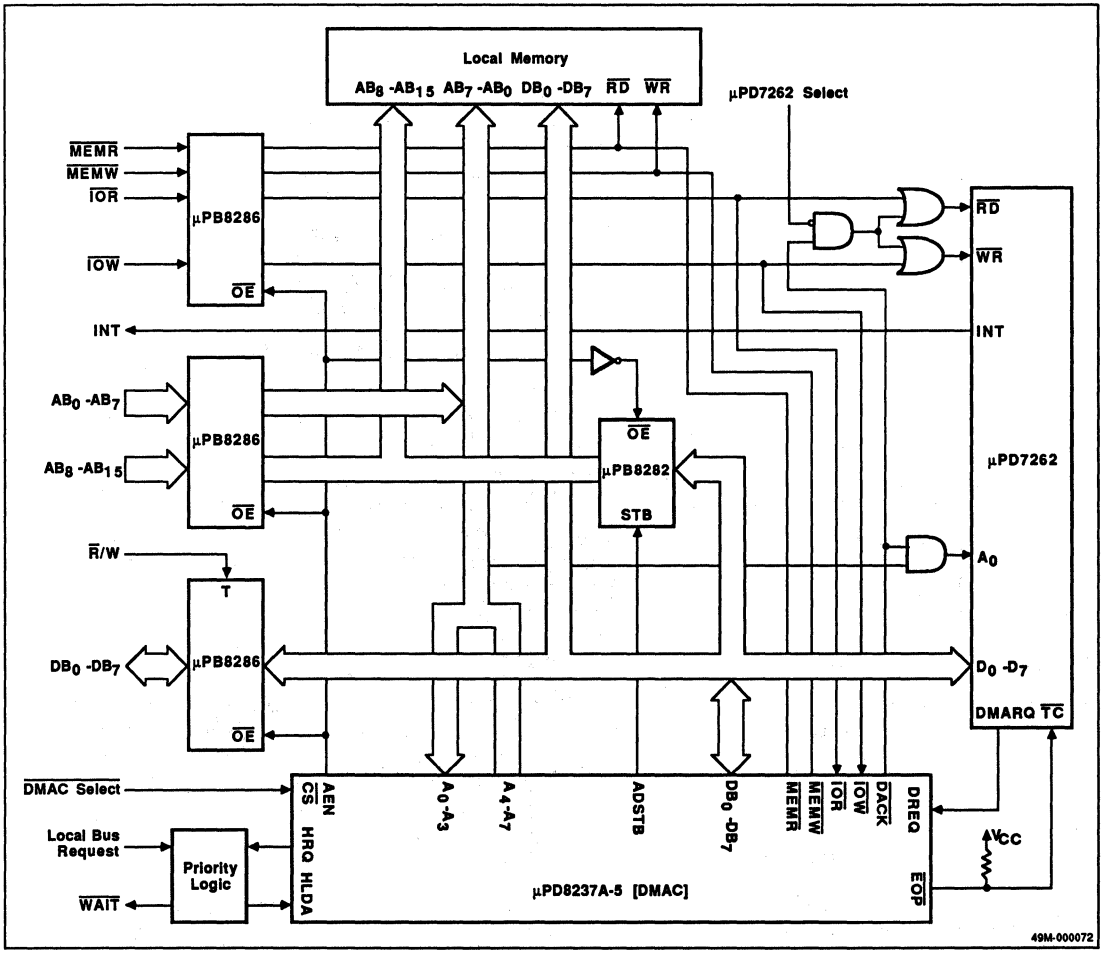

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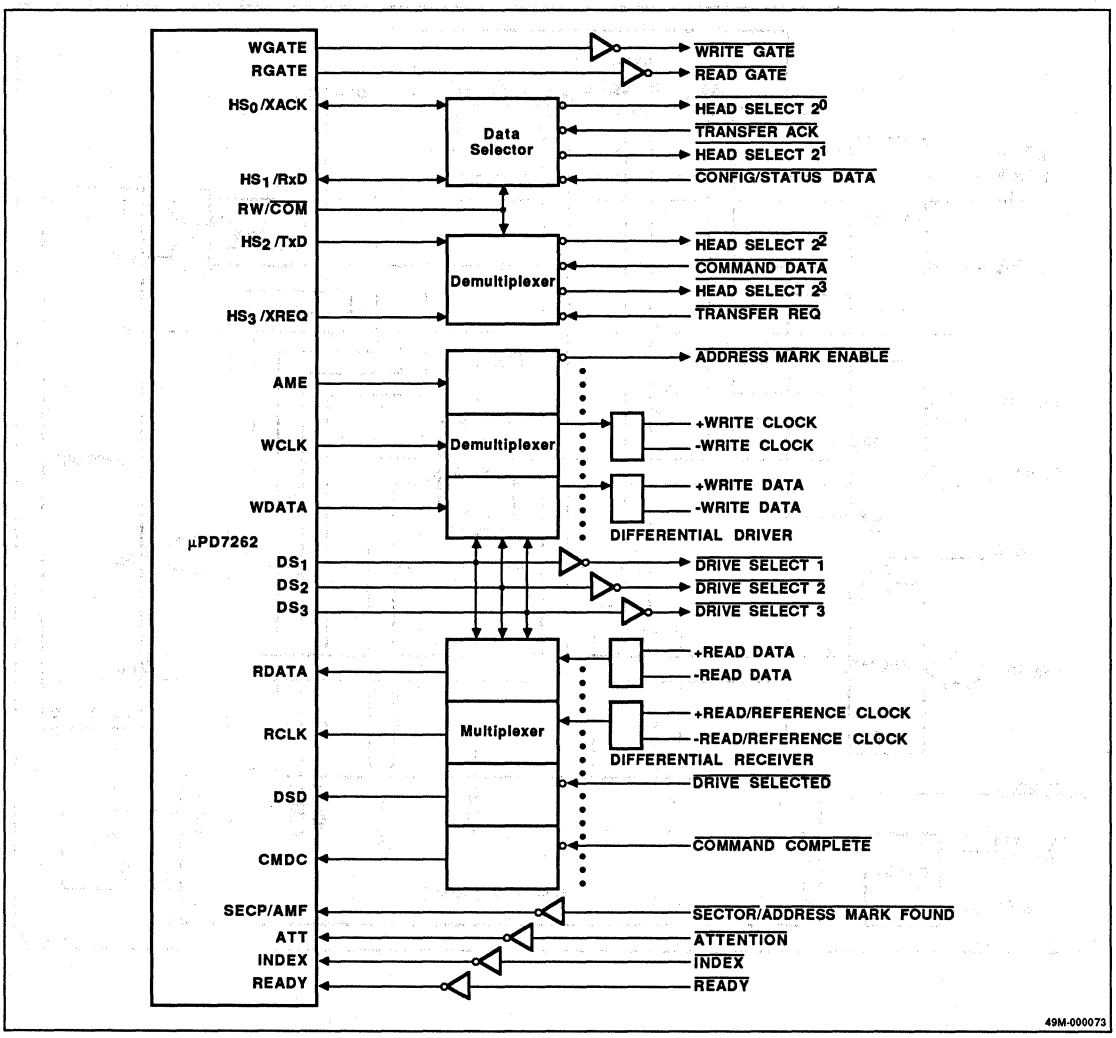
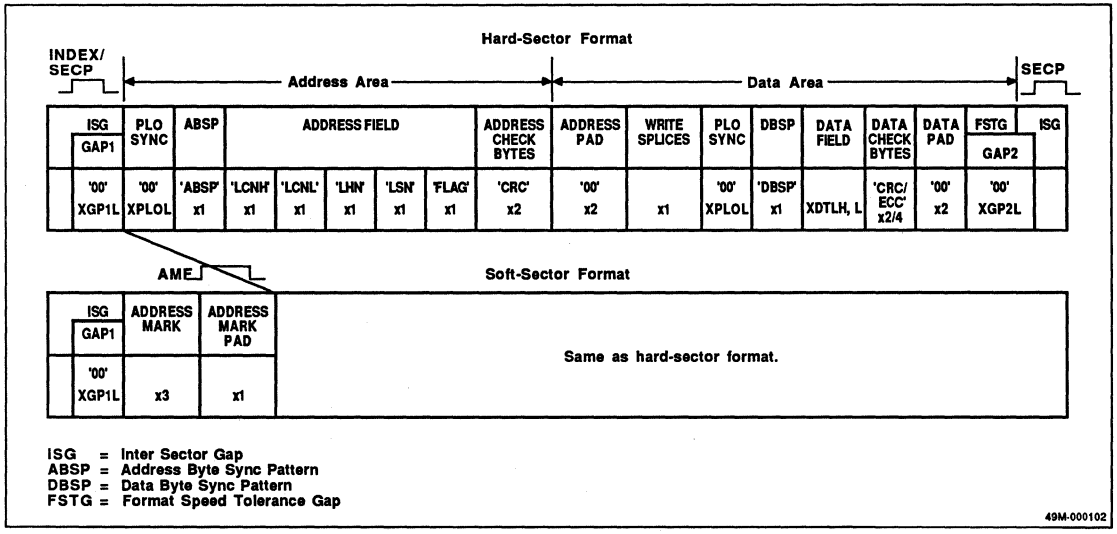
Figure 27. Example of the Interface Between the μPD7262 and a Hard-Disk Drive



SECTOR FORMATS

Figure 28 shows the hard-sector and soft-sector formats for a hard-disk drive.

Figure 28. Hard-Sector and Soft-Sector Formats



Description

The μPD72061 is a hard-disk controller featuring low power consumption and high-speed data transfers. Based on the μPD7261A/B, it provides control signals for interfacing SMD/SMD-E and ST506/412 type drives. The sophisticated instruction set minimizes the software overhead for the host microprocessor and gives the user flexibility in selecting operating parameters.

The DMA interface signals of the μPD72061 facilitate multisector and multitrack data transfers. Extensive error reporting, verify commands, and CRC/ECC data error checking assure reliable controller operation.

An 8-byte FIFO is used for loading command parameters and obtaining command results. This makes structuring of drivers a simple task. The FIFO also buffers data during DMA read/write operations.

Features

- Flexible interface supports SMD/SMD-E and ST506/412 type drives
- Programmable track format
- Controls up to eight drives in SMD-type mode, four drives in ST506-type mode
- Parallel seek operation
- Multisector and multitrack transfer
- Data scan and data verify
- High-level commands, including:
  - Read Data, Write Data, Scan Data, Verify Data
  - Read ID, Verify ID
  - Check, Seek (normal or buffered), Specify
  - Read Diagnostic (SMD only), Detect Error
  - Format
- NRZ or MFM format
- Read/write clock frequency: 24 MHz max
- Error detection and correction
- CMOS
- μPD7261A/B compatible
- Single +5-volt power supply
- 40-pin plastic DIP, 52-pin plastic miniflat, 52-pin PLCC

Ordering Information

Part Number	Package
μPD72061C	40-pin plastic DIP
μPD72061GC-3B6	52-pin plastic miniflat
μPD72061L	52-pin PLCC

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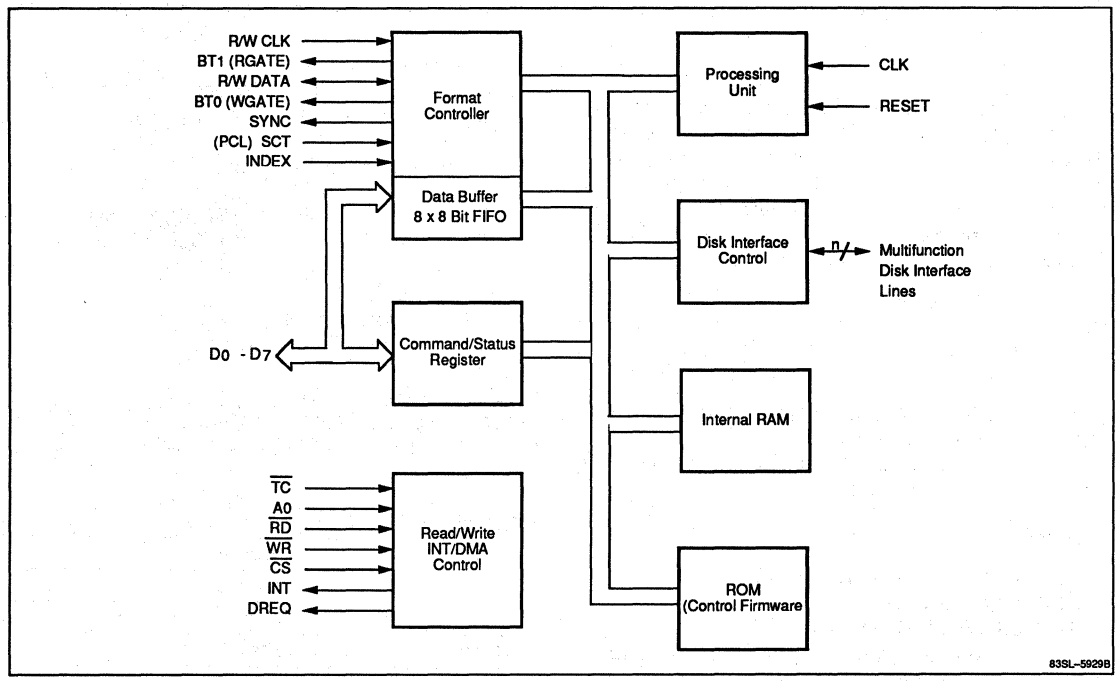
μPD72061 Block Diagram



μPD72111
Small Computer System Interface Controller

Description

The μPD72111 is a small computer system interface controller (SCSIC) conforming to ANSI X3T9.2/82-2 Rev.17B. The μPD72111 SCSI controller offers a true 16-bit CPU data bus but also can be interfaced to an 8-bit CPU data bus.

The μPD72111 contains functions for controlling the sequence between bus phases so that host processor overhead can be reduced. In addition, single-ended type bus drivers/receivers are internally provided on the SCSI bus side so that system size can be reduced.

The μPD72111 was developed utilizing NEC's 1.2-μm CMOS process technology for low power consumption. It operates from a single 5-volt supply and is available in plastic DIP, PLCC, and miniflat packages.

Features

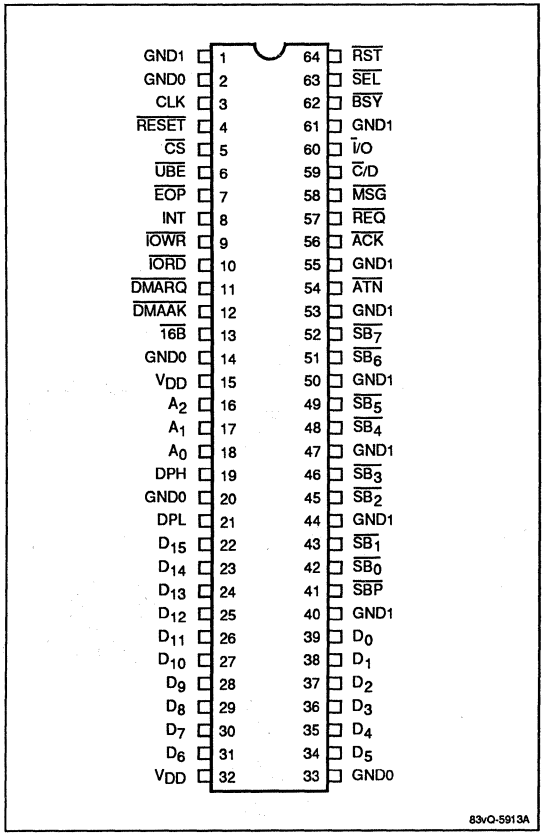
- Conforms to ANSI X3T9.2 Rev.17B
  - Arbitration function
  - Disconnection/reconnection function
  - Parity generation and check function
- Two different data transfer modes
  - Synchronous: 4.0 Mbytes/second max; offset value selectable from 1 to 8
  - Asynchronous: 4.0 Mbytes/second max target
- 16 commands reduce host CPU load; automatic execution of standard operation as SCSI controller can be performed by a single command
- Operates as initiator or target
- Internal single-ended type SCSI bus drivers (48-mA) and Schmitt-type receivers
- CPU data bus width selectable (16 bits or 8 bits)
- Programmed transfer or DMA transfer selectable
- Internal 24-bit transfer counter
- FIFO-type data buffers on SCSI bus side and CPU bus side

Ordering Information

Part No.	Package
μPD72111CW	64-pin plastic shrink DIP (750 mil)
μPD72111L	68-pin PLCC
μPD72111GJ-5BJ	74-pin plastic miniflat

Pin Configurations

64-Pin Plastic Shrink DIP (750 mil)



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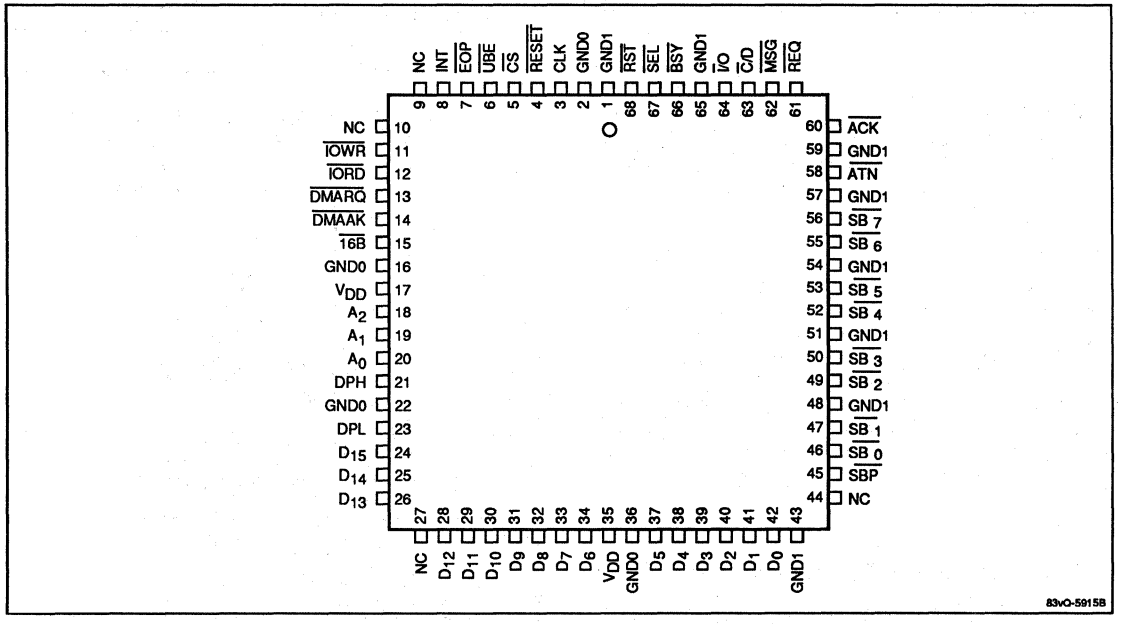
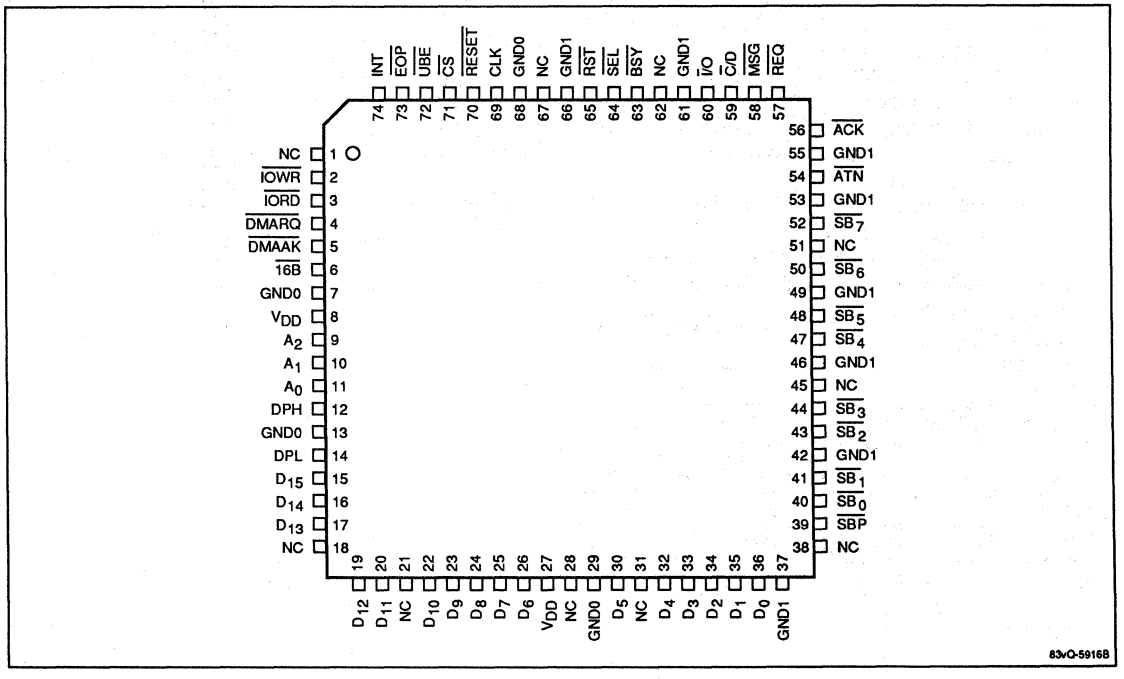
68-Pin PLCC



74-Pin Plastic Miniflat



Pin Identification

Symbol	I/O	Signal Function
CPU Interface Pins		
A_0-A_2	In	Address bus, bits 0-2. Specifies direct access register to be accessed.
$\overline{CS}$	In	Chip Select. Enables internal register accessing.
D_0-D_{15}	I/O	Data bus, bits 0-15. Function depends on bus mode. 16-Bit Bus Mode D_0-D_7 Lower 8 data bits D_8-D_{15} Upper 8 data bits. 8-Bit Bus Mode D_0-D_7 8 data bits D_8-D_{15} High-impedance state
$\overline{DMAAK}$	In	DMA Acknowledge. DMA service enable signal input.
$\overline{DMARQ}$	Out	DMA Request. DMA service signal output.
DPH	I/O	Data Parity High. In 16-bit bus mode, parity bit for data bits D_8-D_{15}. In 8-bit bus mode, this pin becomes high impedance.
DPL	I/O	Data Parity Low. Parity bit for data bits D_0-D_7.
$\overline{EOP}$	Out	End of Process. Open-drain output that terminates DMA service data transfer.
INT	Out	Interrupt Request. Open-drain output to CPU.
$\overline{IORD}$	In	I/O Read. Enables CPU to read contents of μPD72111 internal register.
$\overline{IOWR}$	In	I/O Write. Enables CPU to write data to μPD72111 internal register.
$\overline{UBE}$	In	Upper Byte Enable. In 16-bit bus mode, indicates that upper 8 bits of data bus are valid; $\overline{UBE}$ and address A_0 determine how internal register is accessed. A_0 / $\overline{UBE}$ / Register Access 0 / 0 / 16-bit units (D_0-D_{15}) 0 / 1 / 8-bit units (D_0-D_7) 1 / 0 / 8-bit units (D_8-D_{15}) 1 / 1 / Not allowed
$\overline{16B}$	In	16-Bit Bus. Selects bus mode: 0 = 16-bit; 1 = 8-bit.
SCSI Interface Pins		
$\overline{ACK}$	I/O	Acknowledge. Indicates that initiator has accepted the target information transfer request.
$\overline{ATN}$	I/O	Attention. Indicates that initiator is requesting the message-out phase.
$\overline{BSY}$	I/O	Busy. Indicates that another SCSI device is currently using the bus.
$\overline{C}/D$	I/O	Command/Data.
$\overline{I}/O$	I/O	Input/Output.
$\overline{MSG}$	I/O	Message. Combinations of these signals determine the SCSI bus phase. MSG / $\overline{C}/D$ / $\overline{I}/O$ / Bus Phase 1 / 1 / 1 / Data-out 1 / 1 / 0 / Data-in 1 / 0 / 1 / Command 1 / 0 / 0 / Status 0 / 0 / 1 / Message-out 0 / 0 / 0 / Message in
$\overline{REQ}$	I/O	Requests transfer of target information.
$\overline{RST}$	I/O	Reset. When $\overline{RST}$ signal is detected, μPD72111 immediately releases SCSI bus, sets INT pin active, and then enters idle state.
$\overline{SB_0}$-$\overline{SB_7}$	I/O	SCSI data bus, bits 0-7.
$\overline{SBP}$	I/O	Parity bit for SCSI data bus.
$\overline{SEL}$	I/O	Indicates that the select/reselect operation is being executed.
Other Pins		
CLK	In	External clock.
$\overline{RESET}$	In	System reset.
GND0	-	Ground (0 V).
GND1	-	Driver/receiver ground (0 V).
V_{DD}	In	+5-volt power supply.

Notes:

(1) Each SCSI interface pin has an open-drain driver and a Schmitt receiver so that the μPD72111 can be directly connected to a single-end SCSI bus.

(2) After reset, the status of each output pin and each I/O pin is high-impedance except:

$\overline{DMARQ}$	High level
$\overline{EOP}$	High level
INT	Low level

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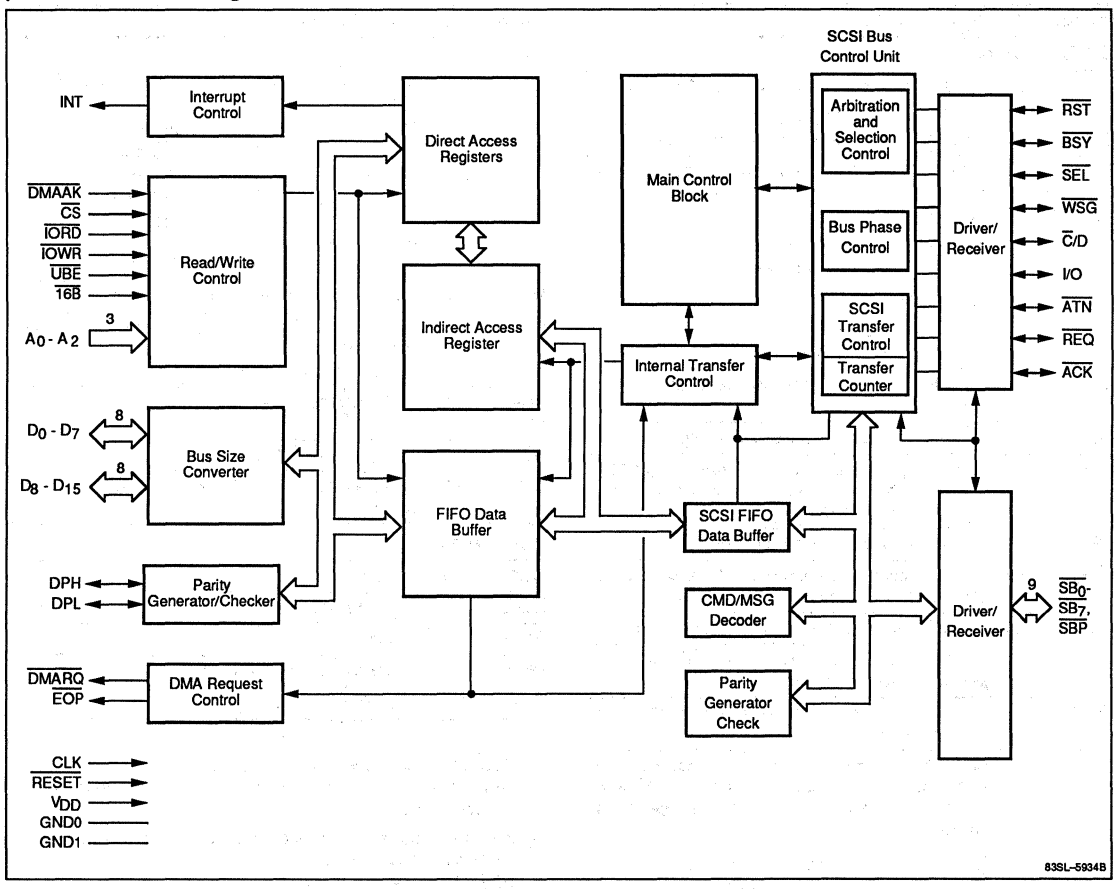
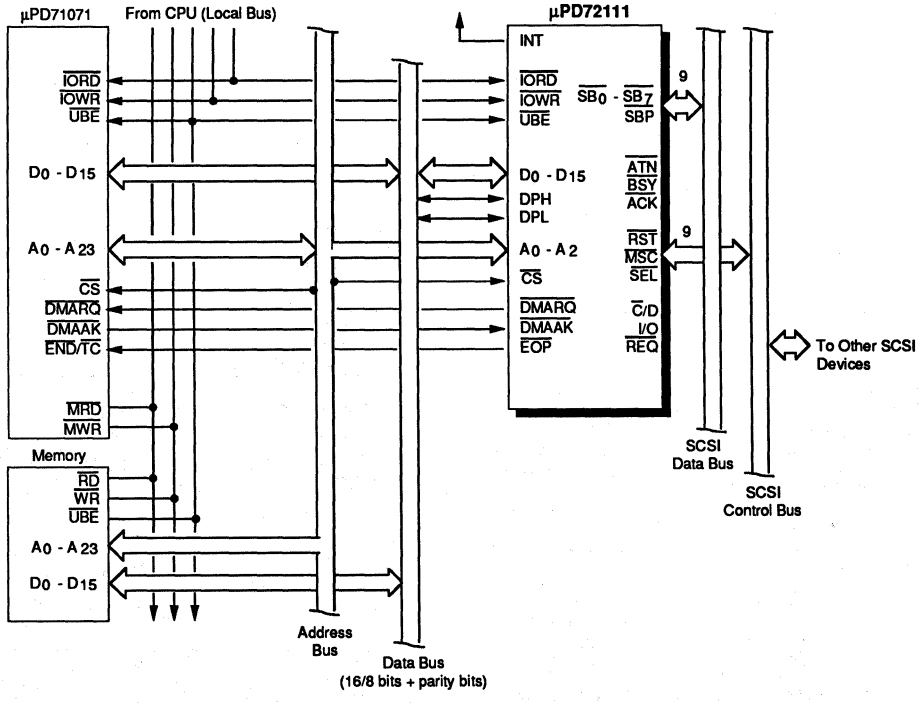
μPD72111 Block Diagram



Typical System Configuration



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Internal Blocks

Name	Description
SCSI bus driver/receiver	Open-drain driver for a single-end SCSI bus and a Schmitt-type receiver.
Arbitration/ selection control	Controls execution sequence of arbitration, selection, and reselection phases; consists of a timing generator and a sequencer.
Bus phase control	Outputs a signal that specifies bus phase type; also monitors bus phase to detect a transition.
SCSI transfer control	Controls data transfer operation on the SCSI bus in each data transfer phase: data-in, data-out, status, message-in, and message-out. Controls SCSI protocol according to $\overline{REQ}$ and $\overline{ACK}$ signals. Controls data transfer execution/termination according to SCSI FIFO status. Contains a 24-bit transfer counter that manages the amount of transfer data on the SCSI bus.
SCSI FIFO data buffer	Eight-bit, eight-stage asynchronous FIFO that adjusts difference between data transfer timing of internal and external SCSI buses; also used for queuing received data for synchronous data transfer.
Command/ message decoder	Decodes received command and message; generates decoded signal that specifies the next sequence.
SCSI parity generator/ checker	Generates parity that will be attached to data output to SCSI data bus; or checks parity attached to data read out from SCSI data bus.
Main control	Sequencer that controls microprogram, operation of each block, and control sequence.
Internal transfer control	Controls data transfer between SCSI FIFO and FIFO or between registers in the indirect access register block. Controls 8-bit/16-bit conversion when host CPU is set to 16-bit bus mode.
Direct access registers	Comprises registers that can be directly accessed from host CPU, such as command register, status register, etc.
Indirect access registers	Comprises registers that cannot be directly accessed from host CPU, but that can be accessed through the window in the direct access register.
FIFO data buffer	This 16-bit, eight-stage asynchronous FIFO increases usage rate of host bus. In 8-bit mode, only the lower 8 bits are used; in 16-bit mode, accessing in 8-bit units is not possible.
Interrupt control	Sets/resets interrupt request signal.
Read/write control	Controls read/write operation of various internal registers; also controls 8-bit accessing in 16-bit mode.
Bus-size converter	Converts bus size according to bus mode.
Host parity generator/ checker	Generates parity that will be attached to data output to CPU data bus; or checks parity attached to data read out from CPU data bus.
DMA request control	Generates DMA service request signal ($\overline{DMARQ}$) according to FIFO status; also controls termination of command operation by $\overline{EOP}$ signal.

Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.5 V
Output voltage, V_O	−0.5 to V_{DD} + 0.5 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL1}	0	0.8	V	Other than CLK
	V_{IL2}	0	0.6	V	CLK
High-level input voltage	V_{IH1}	2.2		V	CPU bus
	V_{IH2}	2.0		V	SCSI bus
	V_{IH3}	3.9		V	CLK
Input hysteresis	V_{HI}	0.2		V	SCSI bus
Low-level output voltage	V_{OL1}		0.4	V	I_{OL1} = 2.5 mA; CPU bus
	V_{OL2}		0.4	V	I_{OL2} = 48.0 mA; SCSI bus
High-level output voltage	V_{OH}	2.4		V	I_{OH} = −400 μA; CPU bus
Low-level input leakage current	I_{LIL1}		−10	μA	V_I = 0 V; CPU bus
	I_{LIL2}		−1.0	mA	V_I = 0 V; SCSI bus
High-level input leakage current	I_{LIH1}		10	μA	V_I = V_{DD}; CPU bus
	I_{LIH2}		0.1	mA	V_I = V_{DD}; SCSI bus
Low-level output leakage current	I_{LOL}		−10	μA	V_I = 0 V; CPU bus

DC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
High-level output leakage current	I_{LOH1}		10	μA	$V_O = V_{DD}$; CPU bus
	I_{LOH2}		0.25	mA	$V_O = V_{DD}$; SCSI bus
Supply current	I_{DD}		100	mA	At 16 MHz

Capacitance

T_A = +25°C; V_{DD} = 0 V; f = 1 Mhz

Item	Symbol	Min	Max	Unit	Conditions
Input capacitance	C_I		20	pF	CPU bus; unmeasured pins at 0 V.
Output capacitance	C_O		20	pF	
Input/output capacitance	C_{IO1}		20	pF	
	C_{IO2}		100	pF	SCSI bus; unmeasured pins at 0 V.

Figure 1. Voltage Thresholds for Timing Measurements

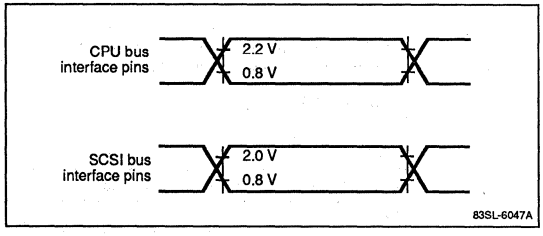


Figure 2. Clock Timing

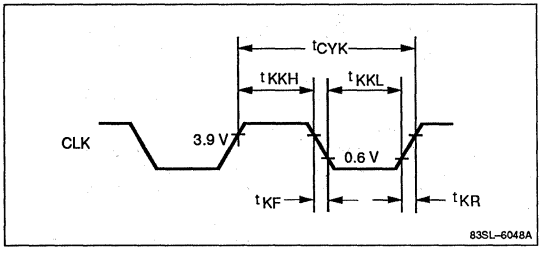
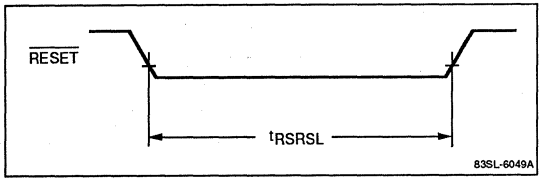


Figure 3 RESET Waveform



AC Characteristics; CPU Bus Interface

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%; see figure 1 for timing measurement voltage thresholds

Parameter	Symbol	Min	Max	Unit	Conditions
Clock (figure 2)					
CLK input cycle time	t_{CYK}	60		ns	
CLK input high-level width	t_{KKH}	25		ns	
CLK input low-level width	t_{KKL}	25		ns	
CLK input rise time	t_{KR}		10	ns	
CLK input fall time	t_{KF}		10	ns	
Reset (figure 3)					
$\overline{RESET}$ low-level width	t_{RSRSL}	16		t_{CYK}	
CPU Bus Read (figure 4)					
$\overline{CS}$ set time to $\overline{IORD}$ ↓	t_{SCSR}	20		ns	
$\overline{CS}$ hold time from $\overline{IORD}$ ↑	t_{HRCS}	0		ns	
Address set time to $\overline{IORD}$ ↓	t_{SAR}	20		ns	
Address hold time from $\overline{IORD}$ ↑	t_{HRA}	0		ns	
$\overline{DMAAK}$ set time to $\overline{IORD}$ ↓	t_{SDAR}	20		ns	
$\overline{DMAAK}$ hold time from $\overline{IORD}$ ↑	t_{HRDA}	0		ns	
$\overline{IORD}$ low-level width	t_{RRL}	80		ns	
$\overline{IORD}$ ↑ to data output delay time	t_{DRD}		50	ns	
$\overline{IORD}$ ↑ to data float time	t_{FRD}	0	50	ns	
$\overline{IORD}$ ↑ to $\overline{DMARQ}$ ↑ delay time	t_{DRDQ}		80	ns	
CPU Bus Write (figure 5)					
$\overline{CS}$ set time to $\overline{IOWR}$ ↓	t_{SCSW}	20		ns	
$\overline{CS}$ hold time from $\overline{IOWR}$ ↑	t_{HWCS}	0		ns	
Address set time to $\overline{IOWR}$ ↓	t_{SAW}	20		ns	
Address hold time from $\overline{IOWR}$ ↑	t_{HWA}	0		ns	
$\overline{DMAAK}$ set time to $\overline{IOWR}$ ↓	t_{SDAW}	20		ns	
$\overline{DMAAK}$ hold time from $\overline{IOWR}$ ↑	t_{HWDA}	0		ns	
$\overline{IOWR}$ low-level width	t_{WWL}	80		ns	
Data set time to $\overline{IOWR}$ ↑	t_{SDW}	20		ns	
Data hold time from $\overline{IOWR}$ ↑	t_{HWD}	0		ns	
$\overline{IOWR}$ ↑ to $\overline{DMARQ}$ ↑ delay time	t_{DWDQ}		80	ns	
Other CPU Bus (figure 6)					
$\overline{IOWR}$ ↑ to $\overline{IORD}$ ↓ or $\overline{IOWR}$ ↑ recovery time	t_{RVW}	80		ns	

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AC Characteristics; CPU Bus Interface (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
$\overline{IORD}$ ↑ to $\overline{IORD}$ ↓ or $\overline{IOWR}$ ↓ recovery time	t_{RVR}	80		ns	
$\overline{IORD}$ ↑ to $\overline{EOP}$ ↓ delay time	t_{DREP}		40	ns	
$\overline{IOWR}$ ↑ to $\overline{EOP}$ ↓ delay time	t_{DWEP}		40	ns	
$\overline{IORD}$ ↑ to INT ↓ delay time	t_{DRI}		40	ns	
$\overline{IOWR}$ ↑ to INT ↓ delay time	t_{DWI}		40	ns	
INT low-level width	t_{IIL}	2		t_{CYK}	

AC Characteristics; SCSI Bus Interface

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%; see figure 1 for timing measurement voltage thresholds

Parameter	Symbol	Min	Max	Unit	Conditions
Arbitration (figure 7)					
Bus free detection to $\overline{BSY}$ response time	t_{DBFBY}	14		t_{CYK}	
$\overline{BSY}$ ↓ to ID output delay time	t_{DBYID}	0		ns	
$\overline{BSY}$ ↓ to $\overline{SEL}$ ↓ delay time	t_{DBYSL}	36		t_{CYK}	
Selection as initiator (figure 8)					
$\overline{SEL}$ ↓ to ID output delay time	t_{DSLID1}	20		t_{CYK}	
$\overline{SEL}$ ↓ to $\overline{ACK}$, $\overline{ATN}$ output delay time	t_{DSLAK}	20		t_{CYK}	
$\overline{ACK}$, $\overline{ATN}$ output to $\overline{BSY}$ ↑ delay time	t_{DAKBY}	2		t_{CYK}	
$\overline{BSY}$ ↑ to $\overline{BSY}$ ↓ input valid delay time	t_{DBYBY1}	8		t_{CYK}	
$\overline{BSY}$ ↓ to $\overline{SEL}$ ↑ output delay time	t_{DBYSL1}	2		t_{CYK}	
Selection as target (figure 9)					
$\overline{BSY}$ hold time from $\overline{SEL}$ ↓	t_{HSLBY1}	0		ns	
ID set time from $\overline{BSY}$ ↑	t_{SIDBY}	0		ns	
$\overline{BSY}$ ↑ to $\overline{BSY}$ ↓ output delay time	t_{DBYBY2}	10		t_{CYK}	
ID hold time from $\overline{BSY}$ ↓	t_{HBYID1}	0		ns	
$\overline{SEL}$ hold time from $\overline{BSY}$ ↓	t_{HEYSL1}	0		ns	
$\overline{ATN}$ set time to $\overline{SEL}$ ↑	t_{SATSL}	0		ns	
$\overline{SEL}$ ↑ to target output delay time	t_{DSLTG}	2		t_{CYK}	
Reselection as initiator (figure 10)					
$\overline{BSY}$ hold time from $\overline{SEL}$ ↓	t_{HSLBY2}	0		ns	
ID set time to $\overline{BSY}$ ↑	t_{SIDBY}	0		ns	
I/O set time to $\overline{BSY}$ ↑	t_{SIOBY}	0		ns	
$\overline{SEL}$ ↑ to $\overline{ATN}$ output delay time	t_{DSLAT}	2		t_{CYK}	
$\overline{BSY}$ ↑ to $\overline{BSY}$ ↓ output delay time	t_{DBYBY3}	10		t_{CYK}	
ID hold time from $\overline{BSY}$ ↓	t_{HBYID2}	0		ns	
$\overline{SEL}$ hold time from $\overline{BSY}$ ↓	t_{HBYSL2}	0		ns	
$\overline{SEL}$ ↑ to $\overline{BSY}$ ↑ output delay time	t_{DSLBY}	2		t_{CYK}	
Reselection as target (figure 11)					
$\overline{SEL}$ ↑ to ID output delay time	t_{DSLID2}	20		t_{CYK}	
$\overline{SEL}$ ↓ to target output delay time	t_{DSLTG}	0		ns	
ID output to I/O output delay time	t_{DIDIO}	0		ns	
I/O input to $\overline{BSY}$ ↑ output delay time	t_{DIOBY}	2		t_{CYK}	
$\overline{BSY}$ ↑ to $\overline{BSY}$ ↓ input valid delay time	t_{DBYBY4}	8		t_{CYK}	
$\overline{BSY}$ ↓ to $\overline{SEL}$ ↑ output delay time	t_{DBYSL2}	2		t_{CYK}	
Reception as initiator in asynchronous mode; data-in, status, and message-in phases (figure 12)					
$\overline{SEL}$ ↑ to phase input valid delay time	t_{DSLPH1}	0		ns	
I/O ↓ to data float delay time	t_{FIOD1}	0		ns	
Phase set time to $\overline{REQ}$ ↓	t_{SPHRQ1}	400		ns	
Data set time to $\overline{REQ}$ ↓	t_{SDRQ1}	5		ns	
$\overline{REQ}$ ↓ to $\overline{ACK}$ ↓ output delay time	t_{DRQAK1}	0		ns	
Data hold time from $\overline{ACK}$ ↓	t_{HAKD1}	0		ns	
$\overline{REQ}$ hold time from $\overline{ACK}$ ↓	t_{HAKRQ1}	0		ns	
$\overline{REQ}$ ↑ to $\overline{ACK}$ ↑ output delay time	t_{DRQAK2}	1		t_{CYK}	
Phase hold time from $\overline{ACK}$ ↑	t_{HAKPH1}	0		ns	
Transfer as target in asynchronous mode; data-in, status, and message-in phases (figure 13)					
$\overline{SEL}$ ↑ to phase output delay time	t_{DSLPH2}	2		t_{CYK}	
I/O ↓ to data output delay time	t_{DIOD1}	0		ns	
Phase set time to $\overline{REQ}$ ↓	t_{SPHRQ2}	500		ns	
Data hold time to $\overline{REQ}$ ↓	t_{SDRQ2}	55		ns	
$\overline{REQ}$ ↓ to $\overline{ACK}$ ↓ input valid delay time	t_{DRQAK3}	0		ns	
$\overline{ACK}$ ↓ to $\overline{REQ}$ ↑ output delay time	t_{DAKRQ1}	1		t_{CYK}	
Data hold time from $\overline{ACK}$ ↓	t_{HAKD2}	0		ns	

AC Characteristics; SCSI Bus Interface (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
$\overline{ACK}$ hold time from $\overline{REQ}$ ↑	t_{HRQAK1}	0		ns	
$\overline{ACK}$ ↑ to $\overline{REQ}$ ↓ output delay time	t_{DAKRQ2}	1		t_{CYK}	
Phase hold time from $\overline{ACK}$ ↑	t_{HAKPH2}	1		t_{CYK}	
Transfer as initiator in asynchronous mode; data-out, command, and message-in phases (figure 14)					
$\overline{SEL}$ ↑ to phase input delay time	t_{DSLPH3}	0		ns	
I/O ↑ to data output delay time	t_{DIOD2}	0		ns	
Phase set time to $\overline{REQ}$ ↓	t_{SPHRQ3}	400		ns	
Data set time to $\overline{ACK}$ ↓	t_{SDAK1}	55		ns	
$\overline{REQ}$ ↓ to $\overline{ACK}$ ↓ output delay time	t_{DRQAK4}	1		t_{CYK}	
Data hold time from $\overline{REQ}$ ↑	t_{HRQD1}	0		ns	
$\overline{REQ}$ hold time from $\overline{ACK}$ ↓	t_{HAKRQ2}	0		ns	
$\overline{REQ}$ ↑ to $\overline{ACK}$ ↑ output delay time	t_{DRQAK5}	1		t_{CYK}	
Phase hold time from $\overline{ACK}$ ↑	t_{HAKPH3}	0		ns	
Reception as target in asynchronous mode; data-out, command, and message-out phases (figure 15)					
$\overline{SEL}$ ↑ to phase output delay time	t_{DSLPH4}	2		t_{CYK}	
I/O ↑ to data float delay time	t_{FIOD2}	0		ns	
Phase set time to $\overline{REQ}$ ↓	t_{SPHRQ4}	500		ns	
Data set time to $\overline{ACK}$ ↓	t_{SDAK2}	5		ns	
$\overline{REQ}$ ↓ to $\overline{ACK}$ ↓ input valid delay time	t_{DRQAK6}	0		ns	
$\overline{ACK}$ ↓ to $\overline{REQ}$ ↑ output delay time	t_{DAKRQ3}	1		t_{CYK}	
Data hold time from $\overline{REQ}$ ↑	t_{HRQD2}	0		ns	
$\overline{ACK}$ hold time from $\overline{REQ}$ ↑	t_{HRQAK2}	55		ns	
$\overline{ACK}$ hold time from $\overline{REQ}$ ↑	t_{HRQAK2}	55		ns	
$\overline{ACK}$ ↑ to $\overline{REQ}$ ↓ output delay time	t_{DAKRQ4}	1		t_{CYK}	
Phase hold time from $\overline{ACK}$ ↑	t_{HAKPH4}	1		t_{CYK}	
Reception as initiator in synchronous mode; data-in phase (figure 16)					
$\overline{SEL}$ ↑ to phase input delay time	t_{DSLPH5}	0		ns	
I/O ↓ to data float delay time	t_{FIOD3}	0		ns	
Phase set time to $\overline{REQ}$ ↓	t_{SPHRQ5}	400		ns	
Data set time to $\overline{REQ}$ ↓	t_{SDRQ3}	5		ns	
Data hold time from $\overline{REQ}$ ↓	t_{HRQD3}	5		ns	
$\overline{REQ}$ input low-level width	t_{RQRQL1}	50		ns	
$\overline{REQ}$ ↑ to $\overline{REQ}$ ↓ recovery time	t_{RVRQ1}	2		t_{CYK}	
$\overline{ACK}$ output low-level width	t_{AKAKL1}	2		t_{CYK}	

Parameter	Symbol	Min	Max	Unit	Conditions
Phase hold time from $\overline{ACK}$ ↑	t_{HAKPH5}	0		ns	
Transfer as target in synchronous mode; data-in phase (figure 17)					
$\overline{SEL}$ ↑ to phase output delay time	t_{DSLPH6}	2		t_{CYK}	
I/O ↓ to data output delay time	t_{DIOD3}	0		ns	
Phase set time to $\overline{REQ}$ ↓	t_{SPHRQ6}	500		ns	
Data set time to $\overline{REQ}$ ↓	t_{SDRQ4}	55		ns	
Data hold time from $\overline{REQ}$ ↓	t_{HRQD4}	125		ns	
$\overline{REQ}$ output low-level width	t_{RQRQL2}	2		t_{CYK}	
$\overline{ACK}$ input low-level width	t_{AKAKL2}	50		ns	
$\overline{ACK}$ ↑ to $\overline{ACK}$ ↓ recovery time	t_{RVAK1}	2		t_{CYK}	
Phase hold time from $\overline{ACK}$ ↑	t_{HAKPH6}	1		t_{CYK}	
Transfer as initiator in synchronous mode; data-out phase (figure 18)					
$\overline{SEL}$ ↑ to phase input valid delay time	t_{DSLPH7}	0		ns	
I/O ↓ to data output delay time	t_{DIOD4}	0		ns	
Phase set time to $\overline{REQ}$ ↓	t_{SPHRQ7}	400		ns	
Data set time to $\overline{ACK}$ ↓	t_{SDAK3}	55		ns	
Data hold time from $\overline{ACK}$ ↓	t_{HAKD3}	125		ns	
$\overline{REQ}$ input low-level width	t_{RQRQL3}	50		ns	
$\overline{REQ}$ ↑ to $\overline{REQ}$ ↓ recovery time	t_{RVRQ2}	2		t_{CYK}	
$\overline{ACK}$ output low-level width	t_{AKAKL3}	2		t_{CYK}	
Phase hold time from $\overline{ACK}$ ↑	t_{HAKPH7}	0		ns	
Reception as target in synchronous mode; data-out phase (figure 19)					
$\overline{SEL}$ ↑ to phase output delay time	t_{DSLPH8}	2		t_{CYK}	
I/O ↓ to data float delay time	t_{FIOD4}	0		ns	
Phase set time to $\overline{REQ}$ ↓	t_{SPHRQ8}	500		ns	
Data set time to $\overline{ACK}$ ↓	t_{SDAK4}	5		ns	
Data hold time from $\overline{DAK}$ ↓	t_{HAKD4}	5		ns	
$\overline{REQ}$ output low-level width	t_{RQRQL4}	2		t_{CYK}	
$\overline{ACK}$ input low-level width	t_{AKAKL4}	50		ns	
$\overline{ACK}$ ↑ to $\overline{ACK}$ ↓ recovery time	t_{RVAK2}	125		ns	
Phase hold time from $\overline{ACK}$ ↑	t_{HAKPH8}	1		t_{CYK}	
Arbitration; bus free (figure 20)					
$\overline{SEL}$ ↓ to ID float delay time	t_{FSLID}		$4t_{CYK}+50$	ns	
Selection/reselection; bus free (figure 21)					
ID float to $\overline{SEL}$ ↑ delay time	t_{DIDSL}	3200		t_{CYK}	
$\overline{SEL}$ ↑ to control float delay time	t_{FSLCTL}	0		ns	

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Figure 4. CPU Bus Read

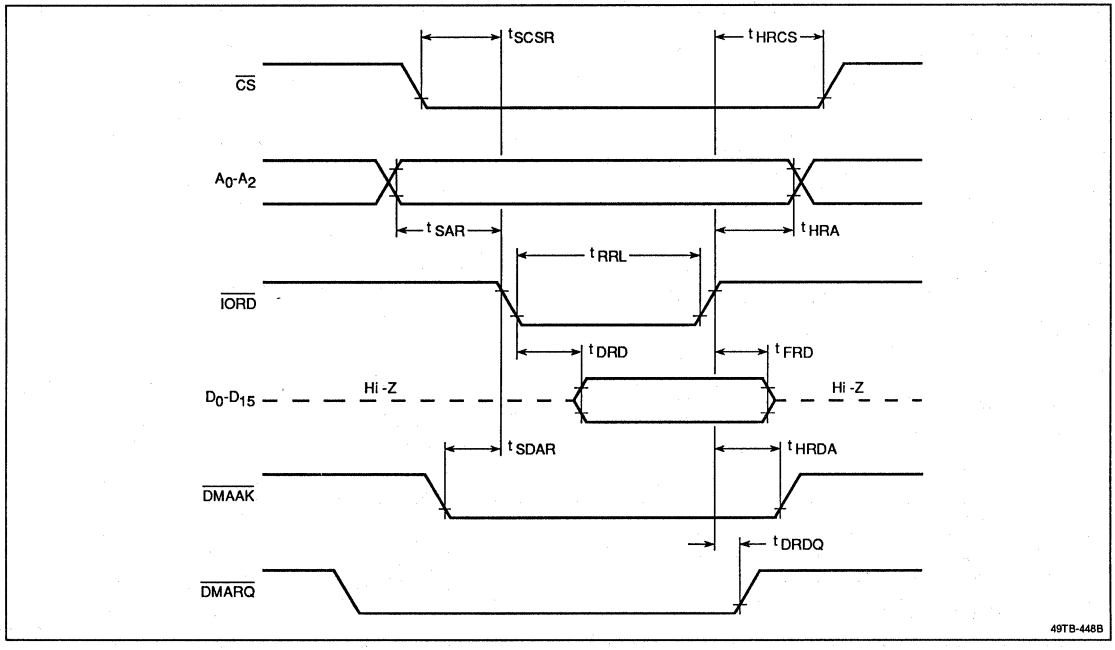

Figure 5. CPU Bus Write

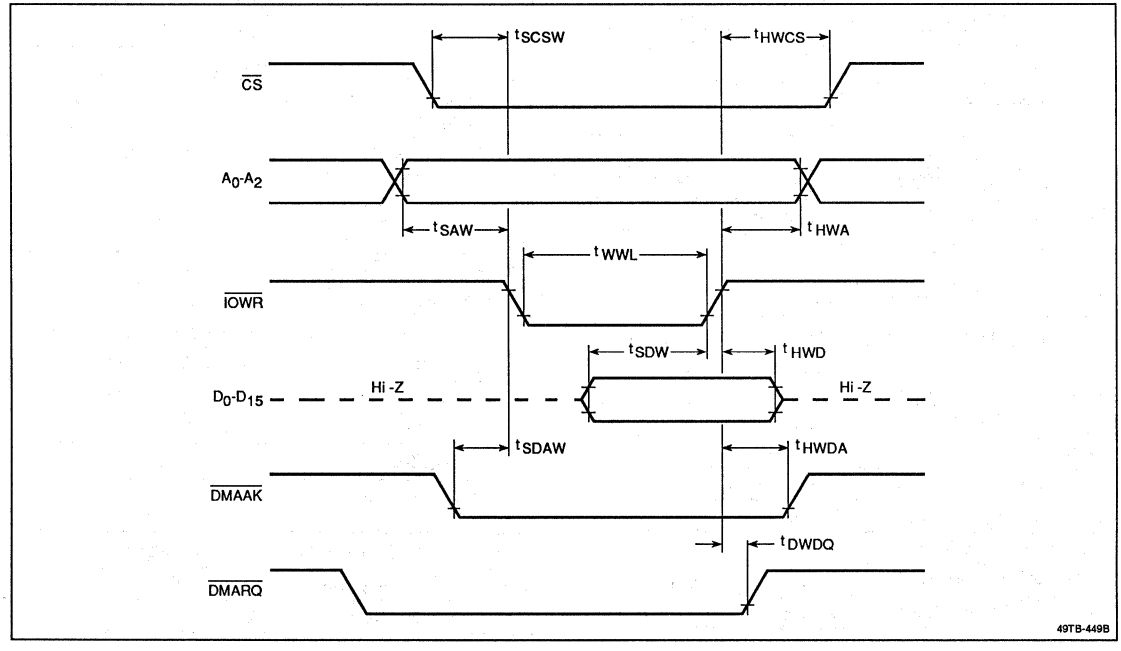

Figure 6. Other CPU Bus Timing

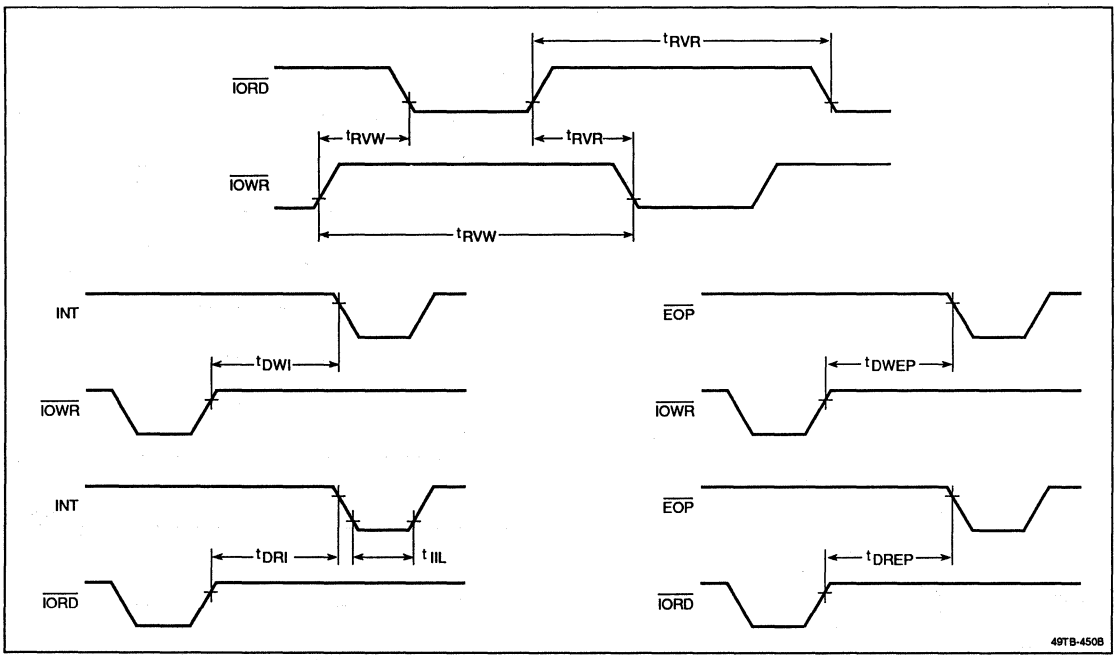

Figure 7. SCSI Bus; Arbitration

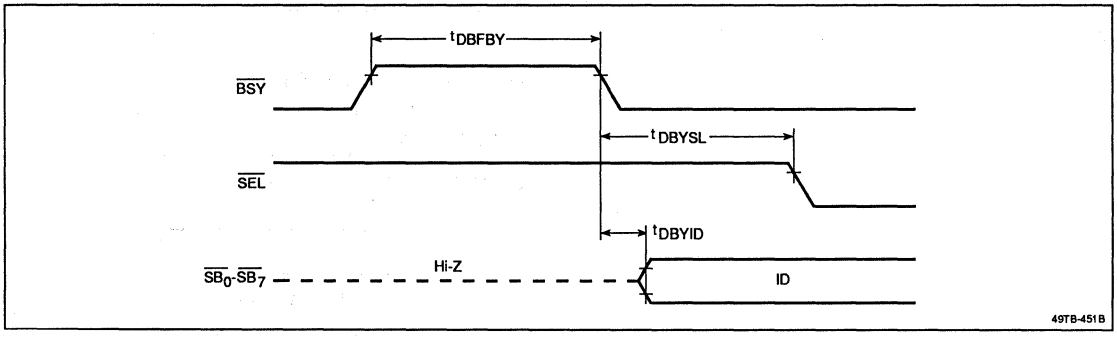

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Figure 8. SCSI Bus; Selection as Initiator

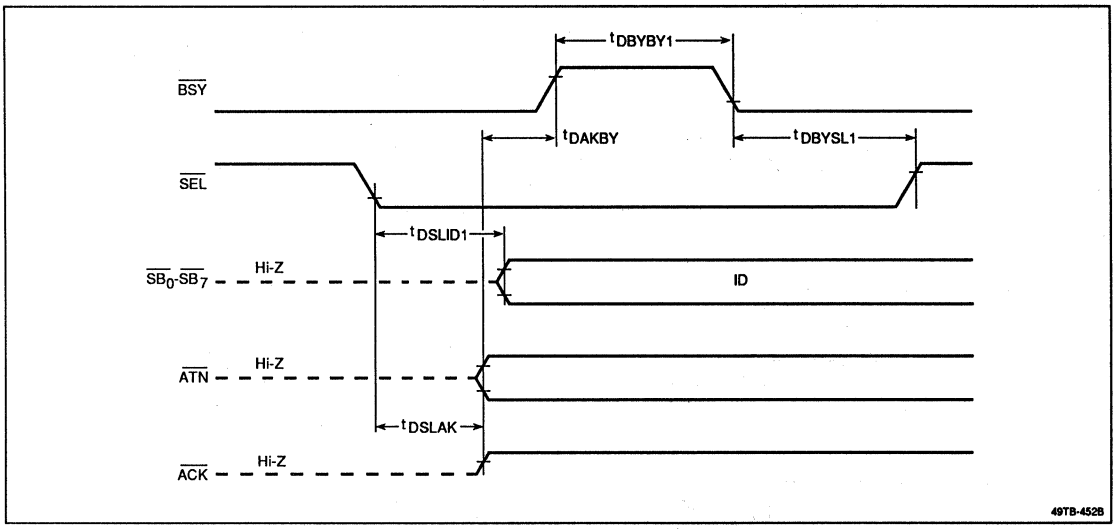

Figure 9. SCSI Bus; Selection as Target

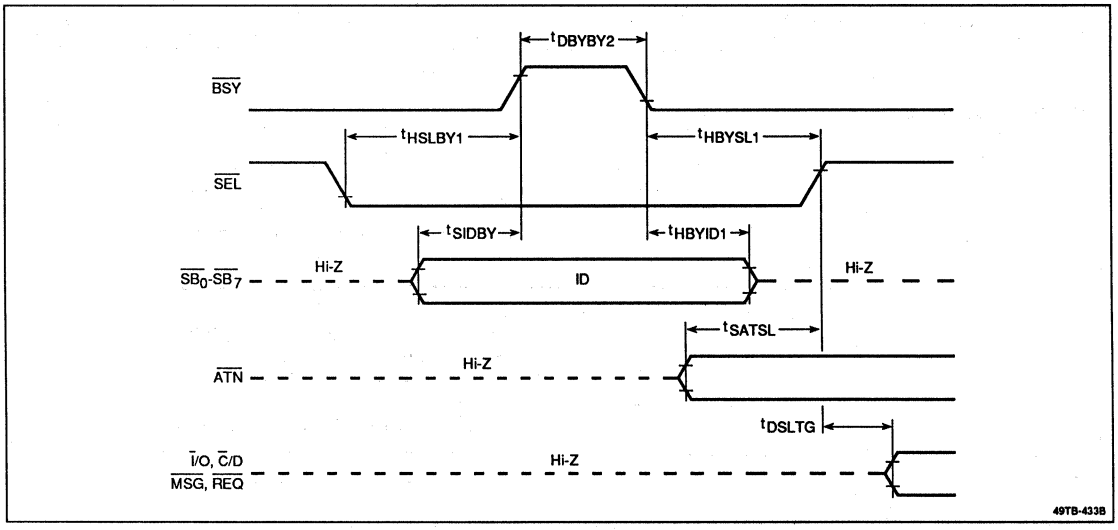

Figure 10. SCSI Bus; Reselection as Initiator

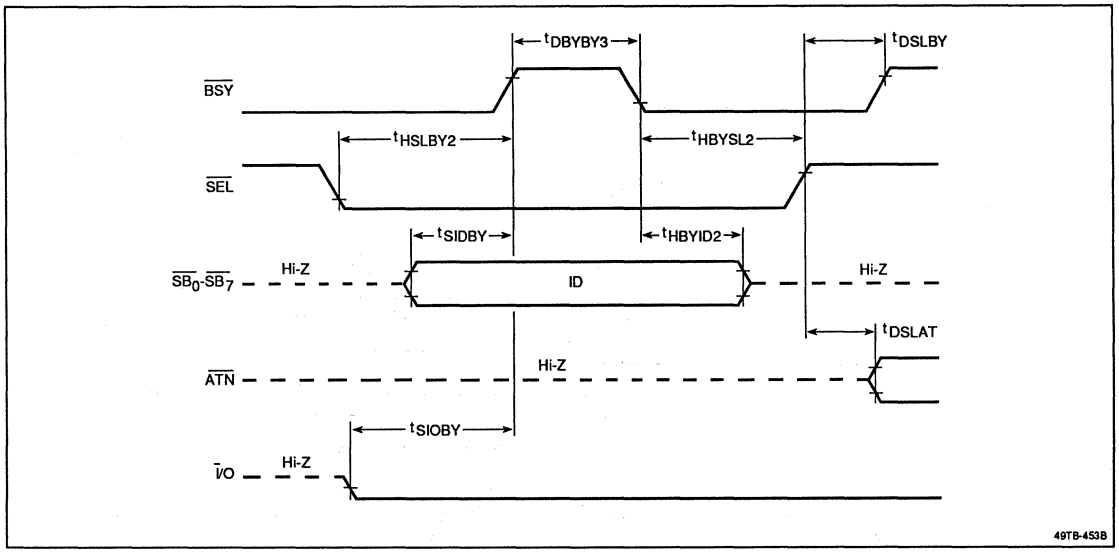

Figure 11. SCSI Bus; Reselection as Target

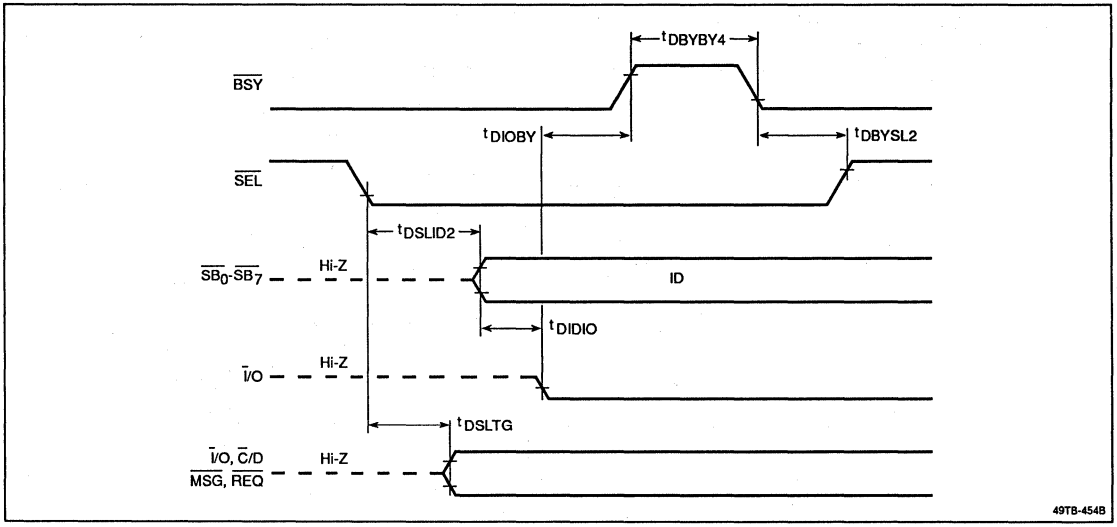

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Figure 12. SCSI Bus; Reception as Initiator

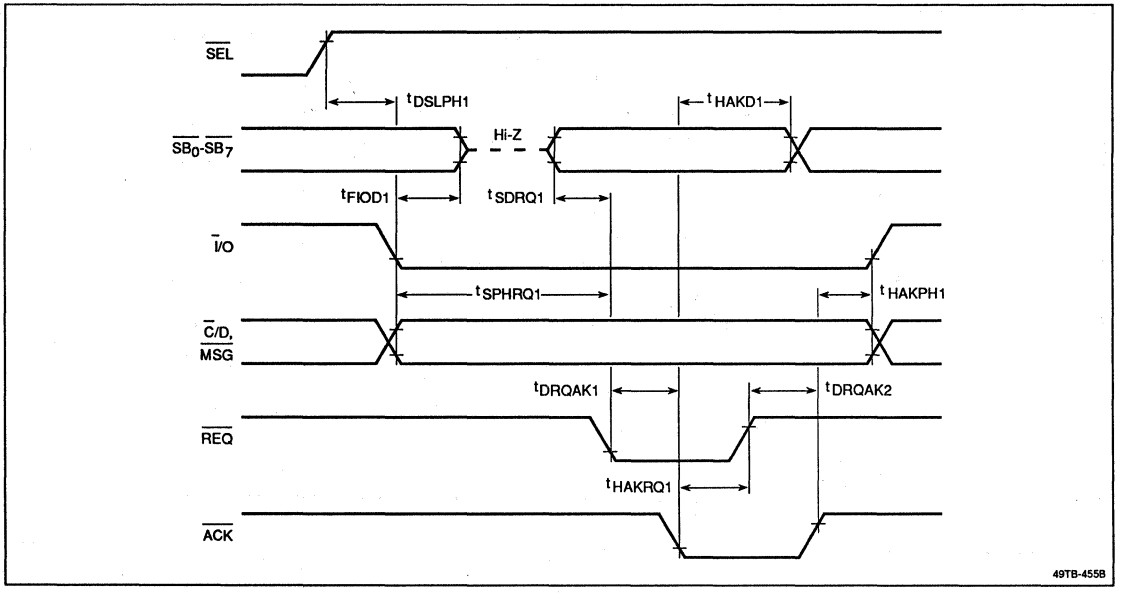

Figure 13. SCSI Bus; Transfer as Target

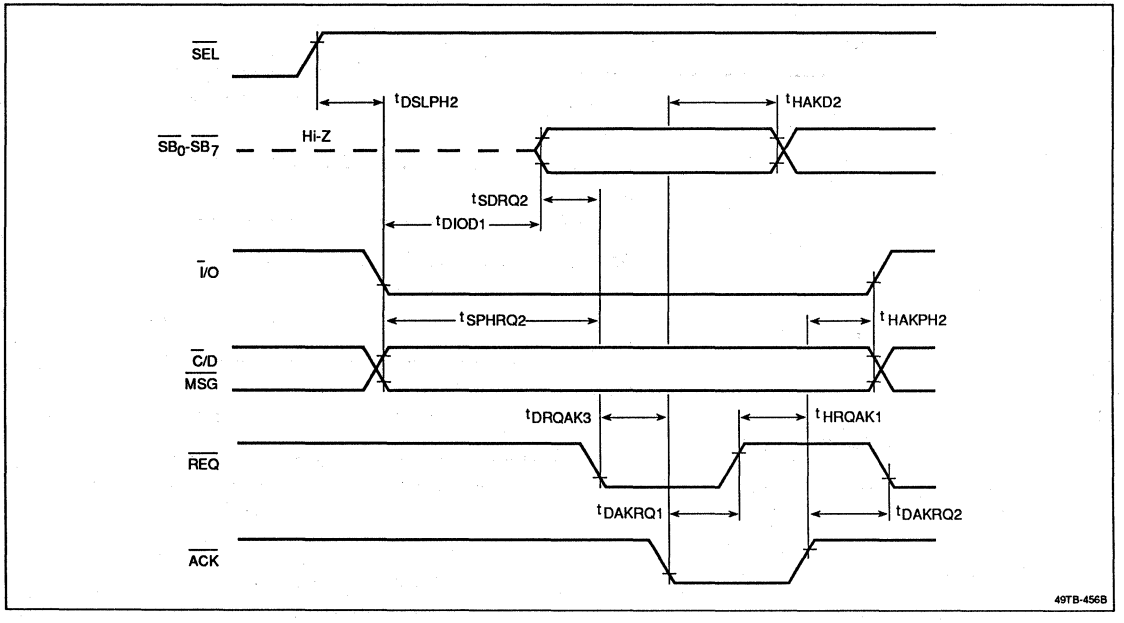

Figure 14. SCSI Bus; Transfer as Initiator in Async Mode

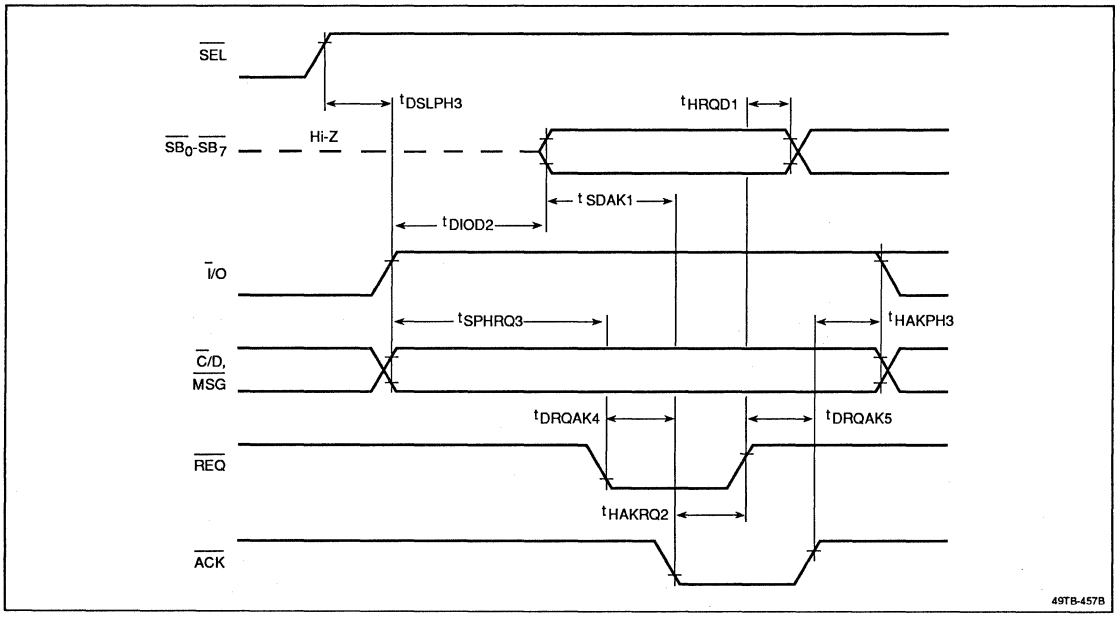

Figure 15. SCSI Bus; Reception as Target in Async Mode

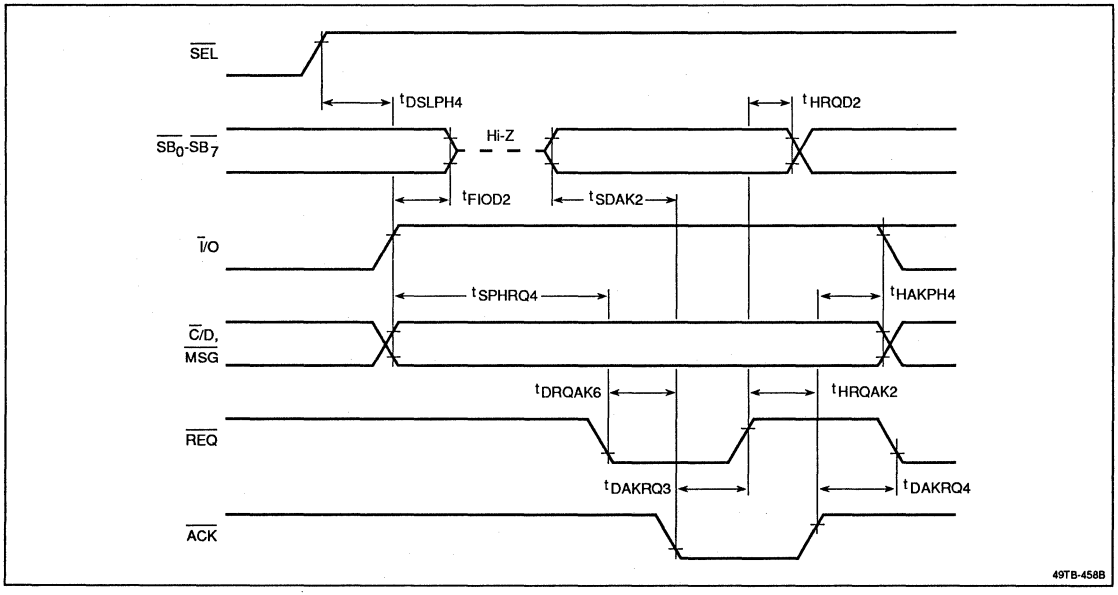

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Figure 16. SCSI Bus; Reception as Initiator in Sync Mode

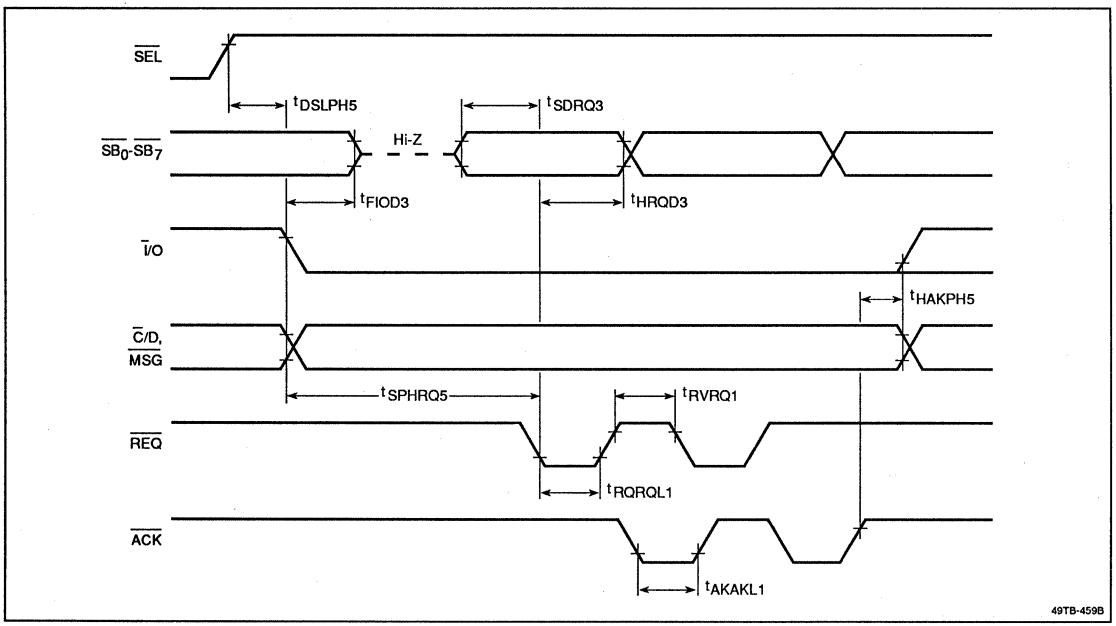

Figure 17. SCSI Bus; Transfer as Target in Sync Mode

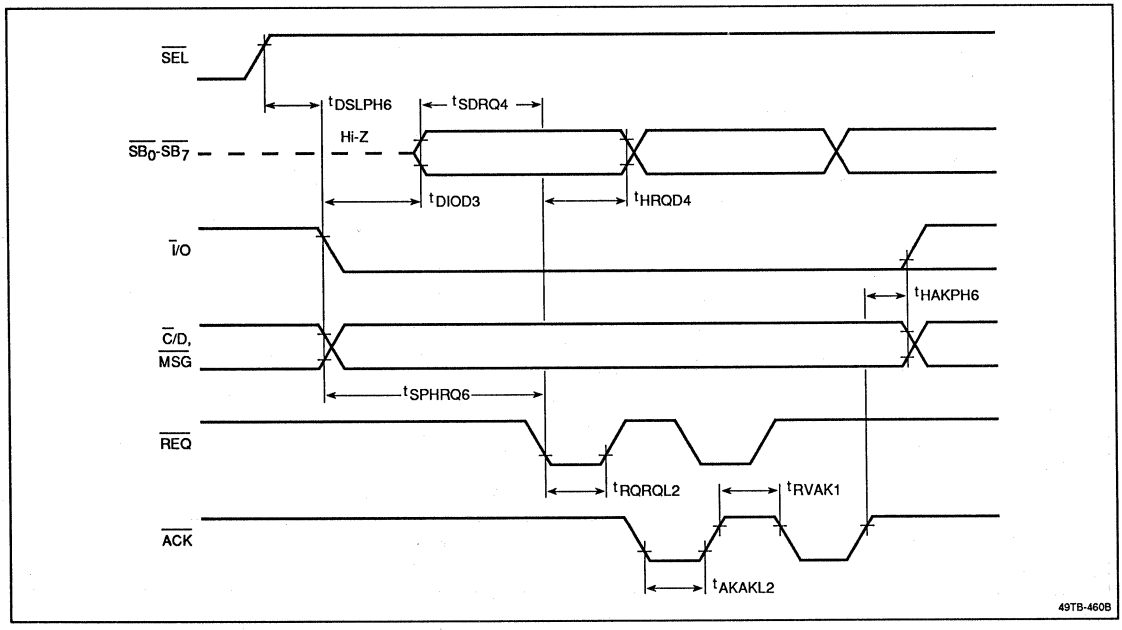

Figure 18. SCSI Bus; Transfer as Initiator in Sync Mode

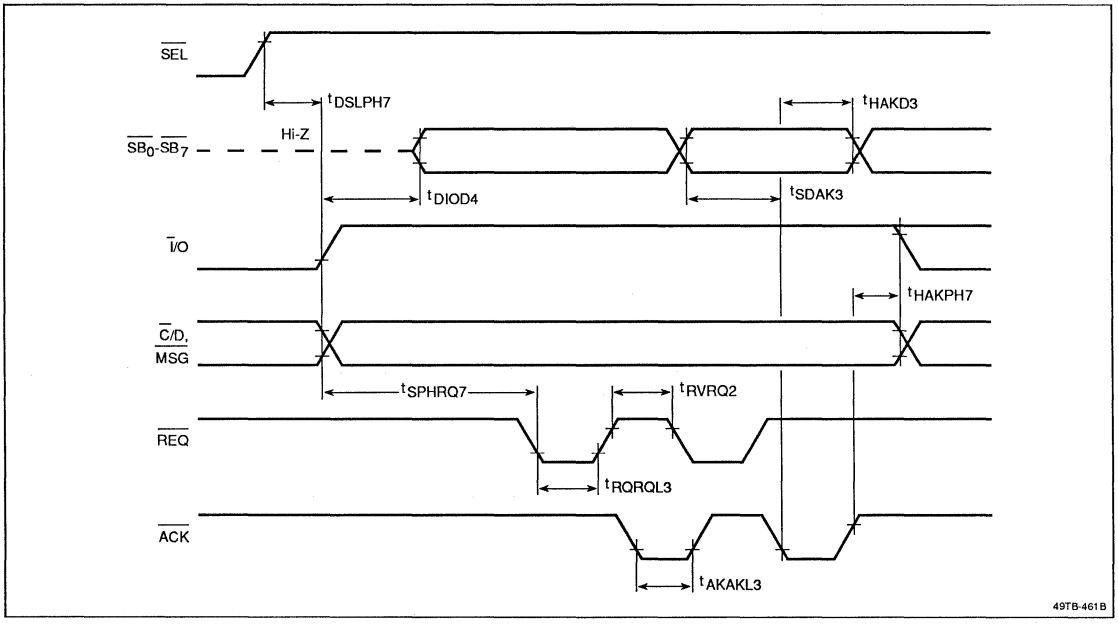

Figure 19. SCSI Bus; Reception as Target in Sync Mode

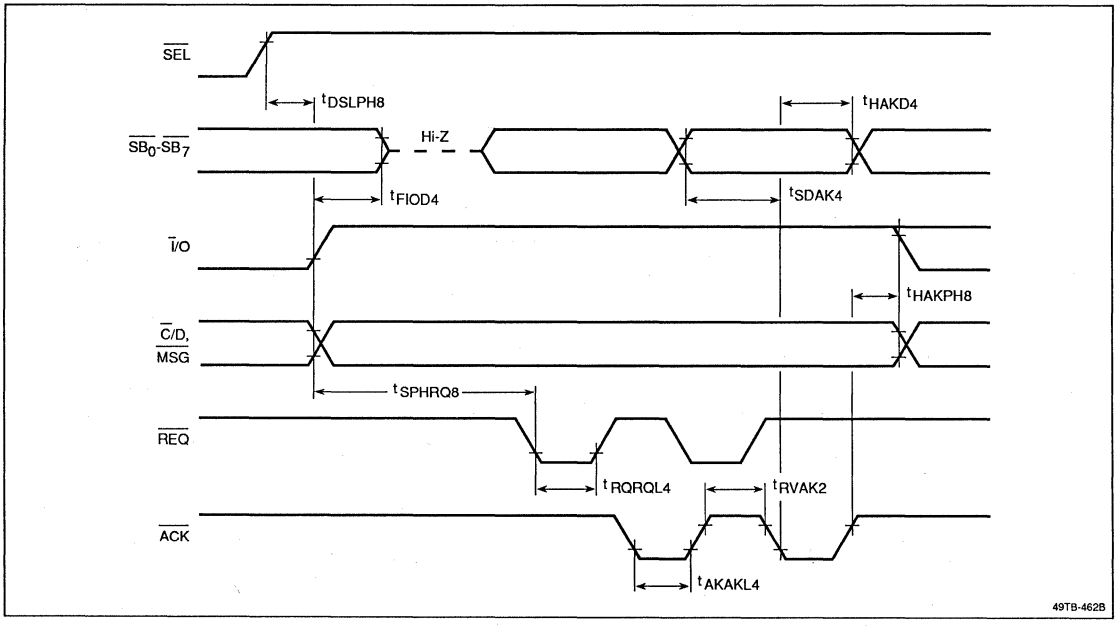

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Figure 20. SCSI Bus; Arbitration, Bus Free

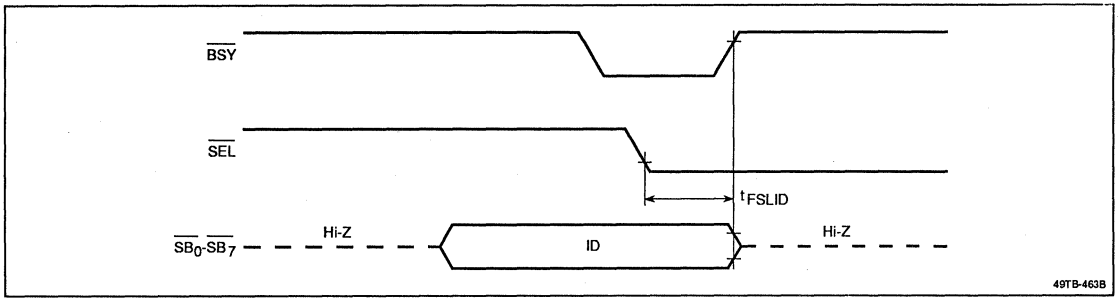
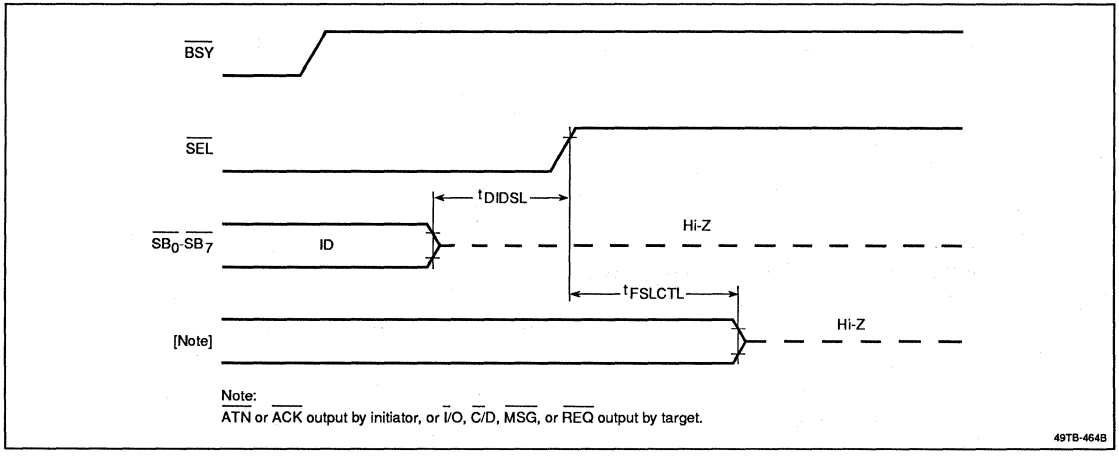


Figure 21. SCSI Bus; Selection/Reselection, Bus Free



DIRECT ACCESS REGISTERS

Table 1 lists the 10 internal registers that can be directly accessed from the host CPU. The register address is specified by pins A_2-A_0.

Table 1. Direct Access Registers

Address A_2-A_0	R/W	Symbol	Register Name
000	R/W	DFL	Data FIFO
001	R/W	DFH	
010	R	CST	Controller status
011	R/W	ADR	Address
100	R/W	WIN1	Window
101	R/W	WIN2	
110	R	TP	Terminated phase
	W	DID	Destination ID
111	R	IST	Interrupt status
	W	CMD	Command

Data FIFO Register

The 16-bit data FIFO register (figure 22) is used to write or read data (including command, status, and message data) accessed through the SCSI bus.

In the 8-bit mode, only the lower 8-bit DFL register at address 0H is used. The contents of the upper 8-bit DFH register at address 1H are fixed to 00H.

In the 16-bit mode, the register is accessed to/from address 0H with signals $A_0 = 0$ and $\overline{UBE} = 0$. When data is sent to the SCSI data bus, the DFL contents are output

first, followed by the DFH contents. When data is sent, the first byte fills DFL and the second byte fills DFH.

The data FIFO register empties when a $\overline{\text{RESET}}$ signal is input, the CHIP RESET command is executed, or the CLEAR FIFO command is executed.

Figure 22. DFL and DFH Registers

16-Bit Mode

	DFH							
0H	DI5	D14	D13	D12	D11	D10	D9	D8
	DFL							
	D7	D6	D5	D4	D3	D2	D1	D0

8-Bit Mode

	DFL							
0H	D7	D6	D5	D4	D3	D2	D1	D0

Controller Status Register

The 8-bit CST register (figure 23) indicates the operating condition of the μPD72111. This is a read-only register; data written to CST becomes invalid.

The value of the CST register becomes 82H when a $\overline{\text{RESET}}$ signal is input or the CHIP RESET command is executed.

Address Register

When accessing an indirect access register, the address should be set to the 8-bit ADR register and the window register (WIN1, WIN2) accessed. Bit 7 of ADR (figure 24) specifies the mode and bits 5-0 specify the address of the indirect access register.

In the auto-increment mode, each access automatically increments the contents of the lower 6 bits of ADR (+1 for the 8-bit bus mode, +2 for the 16-bit bus mode).

The ADR register is reset to 00H by a $\overline{\text{RESET}}$ signal or by execution of the CHIP RESET command.

Figure 23. CST Register

	7	DFH						0
2H	CBSY	INTRQ	CST1	CST0	ATNC	FFUL	FEMP	DRQ

CBSY	μPD72111 Command Execution Status
0	Idle (waiting for a command or executing a type A command
1	Busy (executing type B or C command)

INTRQ	CPU Interrupt Request
0	Not generated
1	Generated

CST1, CST0		μPD72111 Operating Condition
0	0	Disconnected state
0	1	Initiator state
1	0	Target state

ATNC	$\overline{\text{ATN}}$ Pin Status
0	Inactive(high level)
1	Active (low level)

FFUL, FEMP		FIFO State
0	0	Neither full nor empty
0	1	Empty
1	0	Full

DRQ	DFL/DFH Register
0	Accessing DFL/DFH is disabled
1	Writing to or reading from DFL/DFH is requested

Figure 24. ADR Register

	7	Read/Write						0
3H	AINC	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

AINC	Mode for Accessing an Indirect Access Register
0	Normal mode (address in not automatically updated
1	Auto-increment mode (address is automatically updated)

ADR5-ADR0	Indirect Access Register Address
000000	00H
:	:
111111	3FH

Window Register

The window register (figure 25) comprises two 8-bit registers used as a window for accessing the indirect access registers. With the μPD72111 in the 8-bit mode, WIN1 and WIN2 are accessed to/from addresses 4H and 5H, respectively.

In the 16-bit mode, WIN1 and WIN2 function as one 16-bit register accessed to/from address 4H. WIN1 and WIN2 hold the least- and most-significant bytes of the word, respectively. According to the settings of signals A_0 and $\overline{UBE}$, either or both registers can be accessed.

A_0	$\overline{UBE}$	Address	Register Accessed
0	0	4H	WIN1, WIN2
0	1	4H	WIN1
1	0	5H	WIN2

Figure 25. WIN1 and WIN2 Registers

16-Bit Mode

	WIN2							
4H	DI5	D14	D13	D12	D11	D10	D9	D8
	WIN1							
	D7	D6	D5	D4	D3	D2	D1	D0

8-Bit Mode

	WIN1							
4H	D7	D6	D5	D4	D3	D2	D1	D0
	WIN2							
5H	D7	D6	D5	D4	D3	D2	D1	D0

Terminated Phase Register

The 8-bit TP register (figure 26) indicates the phase executed when a command execution is terminated.

The TP register is reset to 00H by a $\overline{RESET}$ signal or by execution of the CHIP RESET command.

Destination ID Register

Bits 2-0 of the DID register (figure 27) set the ID of the target to be selected or the initiator to be reselected. Bit 7 of DID can be set to mask the interrupt request signal (INT). The INTRQ bit of the CST register (figure 23) indicates whether the INT signal was generated or not.

Zeros must be written to bits 6-3 of the DID register.

Figure 26. TP Register

	7			Read Only				0
6H	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0

TP7-TP0	Command	Execution Phase
0000 0001	SCSI RESET	SCSI reset
0001 0001	SELECT	Arbitration
0001 0010		Target selection
0010 0001	TRANSFER	Information transfer
0011 0001	AUTO INITIATOR	Arbitration
0011 0010		Target selection
0011 0011		Identify message transmit
0011 0100		Command transmit
0011 0101		Data transmit/receive
0011 0110		Status receive
0011 0111		Command complete message receive
0100 0001	RESELECT	Arbitration
0100 0010		Initiator reselection
0101 0001	RECEIVE	Information receive
0110 0001	SEND	Information transmit
0111 0001	AUTO TARGET	Selected waiting
0111 0010		Identify message receive
0111 0011		Command receive
1000 0001	RE-RECEIVE	Arbitration
1000 0010		Initiator reselection
1000 0011		Identify message transmit
1000 0100		Data receive
1001 0001	RE-SEND	Arbitration
1001 0010		Initiator reselection
1001 0011		Identify message transmit
1001 0100		Data transmit

Figure 27. DID Register

	7			Write Only				0
6H	INTM	0	0	0	0	DID2	DID1	DID0

INTM	Interrupt Request Signal Mask Function
0	Does not mask interrupt request (INT signal is output when interrupt is generated
1	Masks interrupt request (INT signal is not output even if interrupt request is generated

DID2-DID0	Setting ID of SCSI Device To Be Selected
000	0
:	:
111	7

Interrupt Status Register

The read-only IST register (figure 28) indicates the cause of the interrupt request. If the current contents of IST are not read out, they are retained and IST is not updated for new interrupt generation.

Similarly, if the previous contents were not read out, IST would not have been dated for the current interrupt; however, the current interrupt data would be retained elsewhere internally.

Bit 7 of the IST register indicates the group of the interrupt request generation source. The contents of bits 6-0 depend on the value of bit 7.

The IST register is reset to 00H by a $\overline{\text{RESET}}$ signal or by execution of the CHIP RESET command.

Command Register

The 8-bit CMD register (figure 29) is used by the CPU to write commands to the μPD72111. Commands are described later in table 3.

INDIRECT ACCESS REGISTERS

The 27 registers listed in table 2 can be directly accessed by the CPU through a window in a direct access register. The register address is specified by the lower 6 bits of the ADR register (figure 24).

Table 2. Indirect Access Registers

Address	R/W	Symbol	Register Name
00H	R	TST	Target status
01H	R	SBST	SCSI bus status
02H	R	SID	Source ID
03H	R/W	MSG	Message
04H thru 0FH	R/W	CDB00 thru CDB11	Command descriptor block
10H	R/W	TMOD	Transfer mode
11H	R	CTCL	Current counter (lower 8 bits)
	W	BTCL	Base counter (lower 8 bits)
12H	R	CTCM	Current counter (middle 8 bits)
	W	BTCM	Base counter (middle 8 bits)
13H	R	CTCH	Current counter (upper 8 bits)
	W	BTCH	Base counter (upper 8 bits)
14H thru 1FH			Reserved
20H	R/W	BFTOUT	Bus free timeout
21H	R/W	SRTOUT	Selection/reselection timeout
22H	R/W	RATOUT	$\overline{\text{REQ}}/\overline{\text{ACK}}$ handshake timeout
23H	R/W	CDBL	Command descriptor block length
24H	R/W	MOD	Mode
25H	R/W	PID	Physical ID
26H thru 3FH			Reserved

R = Read only; W = Write only; R/W = Read/Write

6

Figure 28. IST Register

	7			Write Only				0
7H	SRI	IST6	IST5	IST4	IST3	IST2	IST1	IST0

SRI	Interrupt Request Type
0	Interrupt request caused by command termination (normal termination or abort)
1	Interrupt request caused by service request issued to CPU

SRI	IST6-IST0			Interrupt Request Generation Source
0	000	AT	000	Command normal termination
0	000	AT	001	Command break
0	001	AT	000	Invalid command
0	010	AT	000	FIFO overrun/underrun
0	010	AT	001	Synchronous offset error
0	010	AT	010	SCSI bus parity error
0	010	AT	011	CPU bus parity error
0	010	AT	100	Bus free time-out error
0	010	AT	101	Selection/reselection timeout error
0	010	AT	110	$\overline{\text{REQ}}$/$\overline{\text{ACK}}$ timeout error
0	011	0	000	Data-out phase error
0	011	0	001	Data-in phase error
0	011	0	010	Command phase error
0	011	0	011	Status phase error
0	011	0	110	Message-out phase error
0	011	0	111	Message-in phase error
0	100	AT	000	Unsupported SCSI command group
1	000	0	000	Reset
1	000	0	001	SCSI reset condition occurred
1	001	0	000	Disconnected
1	001	0	001	Reselected
1	001	AT	010	Selected
1	010	0	000	Data-out phase started
1	010	0	001	Data-in phase started
1	010	0	010	Command phase started
1	010	0	011	Status phase started
1	010	0	110	Message-out phase started
1	010	0	111	Message-in phase started
1	100	AT	000	Message received

AT bit is valid in target mode only. It shows whether attention condition has occurred (AT = 1) or not (AT = 0).

Figure 29. CMD Register

	7			Write Only				0
7H	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

Target Status Register

The TST register (figure 30) stores the status byte of the target received in the status phase during execution of the AUTO INITIATOR command.

Figure 30. TST Register

	7	Read Only	0
00H	TST		

SCSI Bus Status Register

The SBST register (figure 31) indicates the status of each signal on the SCSI control bus.

Figure 31. SBST Register

	7			Read Only				0
01H	BSY	SEL	REQ	ACK	ATN	MSG	C/D	I/O

Status of Each Pin	
0	Inactive (high level)
1	Active(low level)

Source ID Register

The read-only SID register (figure 32) stores the ID of the last SCSI device that selected the μPD72111. Bits 6-3 are always read out as zeros.

Figure 32. SID Register

	7			Read Only				0
02H	S/R	0	0	0	0	SID2	SID1	SID0

S/R	μPD72111 Select/Reselect Operation
0	Has neither been selected nor reselected (contents of SID2-SID0 are invalid)
1	Has been selected or reselected (contents of SID2-SID0 are valid)

SID2-SID0	ID No. of Last SCDI Device That Selected μPD72111
000	0
:	:
111	7

Message Register

The MSG register (figure 33) sets transmit messages or stores receive messages when the μPD72111 is transmitting or receiving.

Figure 33. MSG Register

	7	Read/Write	0
03H	MSG		

Command Descriptor Block

The 12 CDB registers (figure 34) set/store the command descriptor blocks of SCSI commands.

Figure 34. CDB Registers

	7	Read/Write	0
04H	CDB00		
05H	CDB01		
06H	CDB02		
07H	CDB03		
08H	CDB03		
09H	CDB04		
0AH	CDB06		
0BH	CDB07		
0CH	CDB08		
0DH	CDB09		
0EH	CDB10		
0FH	CDB11		

Transfer Mode Register

The TMOD register (figure 35) sets the mode for data transfer. Zero must be written to bit 3.

Current Counter

The 24-bit CTC register (figure 36) counts the number of data bytes transferred in the information transfer phase. This is a read-only register; data cannot be written to it.

During execution of an information transfer command, the CTC counter is loaded with the values in the BTC base counter. The values loaded from BTC to CTC are controlled by count select bits C1 and C0 of the command code (table 5).

Figure 35. TMOD Register

	7			Read/Write				0
10H	SYNC	TPD2	TPD1	TPD0	0	TOF2	TOF1	TOF0

SYNC	Data Transfer Mode
0	Asynchronous mode
1	Synchronous mode

TPD2-TPD0	Cycles for Sync Mode	Transfer Rate (at 16 MHz)
000	16 clock cycles	1.00 Mbytes/s
001		
010	4 clock cycles	4.00 Mbytes/s
011	6 clock cycles	2.67 Mbytes/s
100	8 clock cycles	2.00 Mbytes/s
101	10 clock cycles	1.60 Mbytes/s
110	12 clock cycles	1.33 Mbytes/s
111	14 clock cycles	1.14 Mbytes/s

TOF2-TOF0	$\overline{REQ}$, $\overline{ACK}$ Pulse Offset Value for Sync Mode
000	1
:	:
111	8

Figure 36. CTC Register

	7	Read Only	0
11H	CTCL		
12H	CTCM		
13H	CTCH		

Base Counter

The 24-bit BTC register (figure 37) sets the number of data transfer bytes to be loaded into the CTC current counter. This is a write-only register; the contents cannot be read out. The count values written to BTC are controlled by count select bits C1 and C0 of the command code. (table 5).

Bus Free Timeout Register

The BFTOUT register (figure 38) sets the bus free timeout. If 00H is written to this register, the timeout detection function will not operate.

6

Figure 37. BTC Register

	7	Write Only	0
11H		BTCL	
12H		BTCM	
13H		BTCH	

BTCH	BTCM	BTCL	Number of Data Transfer Bytes
00H	00H	00H	0
:	:	:	:
00H	00H	FFH	255
00H	01H	00H	256
:	:	:	:
00H	FFH	FFH	65,535
01H	00H	00H	65,536
:	:	:	:
FFH	FFH	FFH	16,777,215

Figure 38. BFTOUT Register

	7	Read/Write	0
20H		BFTOUT	

BFTOUT	Bus Free Timeout (at 16 MHz)
00H	No timeout detection is performed
01H	8.192 ms
:	:
FFH	2088.928 ms

Selection/Reselection Timeout Register

The SRTOUT register (figure 39) sets the timeout for the selection or reselection operation. If 00H is written to this register, the timeout detection function will not operate.

Figure 39. SRTOUT Register

	7	Read/Write	0
21H		SRTOUT	

SRTOUT	Selection/Reselection Timeout (at 16 MHz)
00H	No timeout detection is performed
01H	8.192 ns
:	:
FFH	2088.928 ms

$\overline{\text{REQ}}/\overline{\text{ACK}}$ Handshake Timeout Register

The RATOUT register (figure 40) sets the timeout for handshake operation of $\overline{\text{REQ}}$ and $\overline{\text{ACK}}$ signals during information transfer. If 00H is written to this register, the timeout detection function will not operate.

Figure 40. RATOUT Register

	7	Read/Write	0
22H		RATOUT	

RATOUT	$\overline{\text{REQ}}/\overline{\text{ACK}}$ Timeout (at 16 MHz)
00H	No timeout detection is performed
01H	128 μs
:	:
FFH	32,640 μs

Command Descriptor Block Length Register

The CDBL register (figure 41) sets parameters for the group 6 and group 7 SCSI commands (vendor unique) of the SCSI specifications by using the AUTOINITIATOR command and the AUTO TARGET command.

Figure 41. CDBL Register

	7			Read/Write				0
23H	CL73	CL72	CL71	CL70	CL63	CL62	CL61	CL60

CL73-CL70	Group 7 SCSI Command; CDB Length
0001	1 byte
:	:
1100	12 bytes
1101	Does not support group 7 SCSI commands (generates unsupported group command error)
:	
1111	
0000	
CL63-CL60	**Group 6 SCSI Command; CDB Length**
0001	1 byte
:	:
1100	12 bytes
1101	Does not support group 6 SCSI commands (generates unsupported group command error)
:	
1111	
0000	

Mode Register

The MOD register (figure 42) sets the μPD72111 operation mode.

Figure 42. MOD Register

	7			Read/Write				0
24H	DMA	HPS	DHP	DSP	NAM	SIM	RAEN	SAEN

DMA	**Data Transfer Mode (in data-in/data-out phase)**	
0	Program I/O mode	
1	DMA mode	
HPS	**DHP**	**CPU Bus Parity**
0	0	Odd parity
1	0	Even parity
x	1	Disable parity
DSP	**SCSI Bus Parity**	
0	Enable (even parity only)	
1	Disable parity	
NAM	**SIM**	**Bus Arbitration Execution**
0	x	Arbitration mode
1	0	Non-arbitration mode (non-single-initiator mode)
1	1	Non-arbitration mode (single-initiator mode)
RAEN	**Response (when reselected as initiator by target)**	
0	Does not respond	
1	Responds	
SAEN	**Response (when reselected as target by initiator)**	
0	Does not respond	
1	Responds	

Physical ID Register

The PID register (figure 43) sets the μPD72111's own physical ID on the SCSI system. Zeros must be written to bits 6-3.

Figure 43. PID Register

	7			Read/Write				0
25H	FEN	0	0	0	0	PID2	PID1	PID0

FEN	**Controller Operation**
0	Does not operate as initiator
1	Operates as initiator
PID2-PID0	**μPD72111's Own ID Number**
000	0
:	:
111	7

COMMANDS

Descriptions

The CPU controls the μPD72111 with the 16 commands described in table 3. Commands are listed in groups according to mode—initiator/target, initiator, and target.

Command Code

Table 4 gives the command code, status, and type for each command.

Command Bits. Symbols for command bits in table 4 are explained below.

Symbol	Function
C1, C0	Count select bits
AT	$\overline{ATN}$ signal status selection bit. (1 means the initiator is requesting the message-out phase.)
MG, CD	Transfer information specification bits

The function of count select bits C1 and C0 is to specify the value loaded to the current transfer counter. This can reduce the overhead of modifying the transfer counter. See table 5.

Status. Table 4 specifies the status in effect when the command is issued. Symbols are explained below.

Symbol	Status
D	Disconnect
I	Initiator
T	Target

Type. Table 4 classifies commands as type A, B, or C according to the execution status defined under "μPD72111 Processing" below.

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Table 3. Command Functions

Mode	Command Name	Mnemonic	Function
Initiator or Target	CHIP RESET	CRST	Resets μPD72111 using software.
	BREAK	BRK	Discontinues command execution.
	DISCONNECT	DIS	Releases SCSI bus.
	CLEAR FIFO	CLRF	Clears FIFO
	SCSI RESET	SRST	Resets SCSI bus.
Initiator	SET ATN	SETAT	Sets $\overline{ATN}$ signal.
	RESET ACK	RSTAK	Resets $\overline{ACK}$ signal.
	SELECT	SEL	Selects a target.
	TRANSFER	TFR	Sends/receives data (in initiator mode).
	AUTO INITIATOR	AIN	Automatically executes initiator standard operation.
Target	RESELECT	RSEL	Reselects initiator
	RECEIVE	REC	Receives data (in target mode).
	SEND	SND	Sends data (in target mode).
	AUTO TARGET	ATG	Automatically executes target standard operation.
	RE-RECEIVE	RREC	Reselects → Continuous execution of data-receive operation (in target mode)
	RE-SEND	RSND	Reselects → Continuous execution of data-send operation (in target mode)

Table 4. Command Codes

Command Name	Command Code								Status	Type
CHIP RESET	0	0	0	0	0	0	0	0	D, I, T	A
BREAK	0	0	0	0	0	0	0	1	D, I, T	A
DISCONNECT	0	0	0	0	0	0	1	0	D, I, T	A
CLEAR FIFO	0	0	0	0	0	1	0	1	D, I, T	A
SCSI RESET	0	0	0	0	1	0	0	0	D, I, T	B
SET ATN	0	0	0	0	0	0	1	1	I	A
RESET ACK	0	0	0	0	0	1	0	0	I	A
SELECT	0	0	0	1	AT	0	0	0	D	B
TRANSFER	C1	C0	0	1	0	0	1	0	I	B
AUTO INITIATOR	C1	C0	0	1	AT	1	0	0	D	C
RESELECT	0	0	1	0	0	0	0	0	D	B
RECEIVE	C1	C0	1	0	1	MG	CD	0	T	B
SEND	C1	C0	1	0	1	MG	CD	1	T	B
AUTO TARGET	0	0	1	1	0	0	0	0	D	C
RE-RECEIVE	C1	C0	1	1	1	0	0	0	D	C
RE-SEND	C1	C0	1	1	1	0	0	1	D	C

Table 5. Loading the Current Transfer Counter

C1	C0	Load Operation		Counting Range
0	0	CTCH/M/L	← BTCH/M/L	0 to 16,776,960 bytes in 1-byte units
0	1	CTCH/M CTCL	← BTCH/M ← 00H	0 to 16,776,960 bytes in 256-byte units

Table 5. Loading the Current Transfer Counter

C1	C0	Load Operation		Counting Range
1	0	CTCH/M CTCL	← 0000H ← BTCL	0 to 256 bytes in 1-byte units
1	1	CTCH/M/L	← 000001H	Single-byte only

μPD72111 PROCESSING

Processing by the μPD72111 is in either of two categories:

- Command processing initiated by a command from the CPU
- Response processing executed by the SCSI bus status transition

Command Processing

Command processing operations differ depending on the command executed.

Type A Command. Except for CHIP RESET, the command is immediately executed. Then, a new command is awaited.

CHIP RESET Command. The μPD72111 is immediately reset, after which an interrupt request is generated.

Type B and C Commands. The issued command is synchronized with the system clock and executed. After the command is executed, an interrupt is generated.

Response Processing

When selected or reselected by another device, response processing for the device is executed. If the bus status changes during information transfer, the bus phase after the transition is detected and reported. The μPD72111 generates an interrupt upon completing the response processing.

HOST CPU PROCESSING

Processing by the host CPU for the μPD72111 is in either of two categories.

- Command issuance processing by request from the CPU side. See figure 44.
- Interrupt processing generated when the operation specified by the command is completed, or the SCSI bus status changes. See figure 45.

Figure 44. Command Issuance Processing Flow

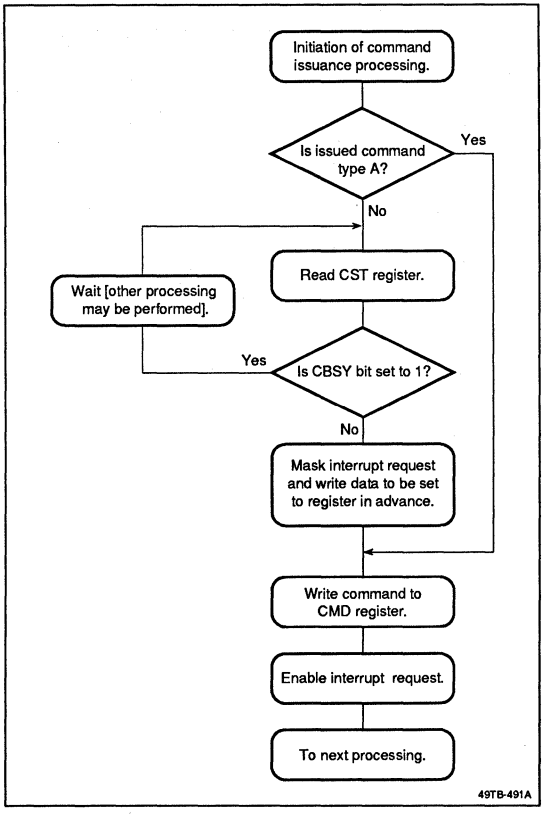
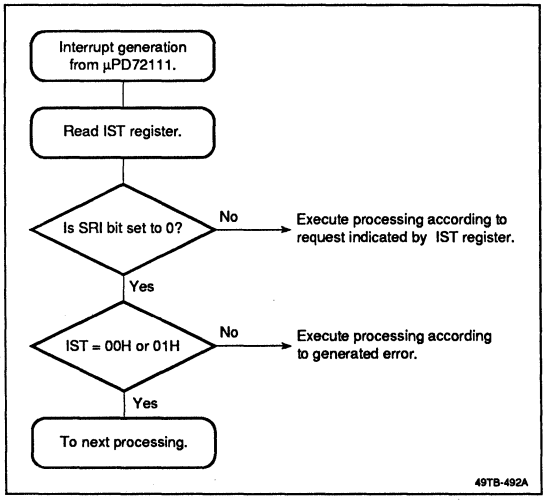


Figure 45. Interrupt Processing Flow



6

LCD CONTROLLERS

7

Section 7
LCD Controllers

μPD7225
CMOS, Intelligent, Alphanumeric LCD Controller/Driver

Description

The μPD7225 is an intelligent peripheral device designed to interface most microprocessors with a wide variety of alphanumeric LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 32 segments and is easily cascaded for larger LCD applications. The μPD7225 communicates with a host microprocessor through an 8-bit serial interface. It includes a 7-segment numeric and a 14-segment alphanumeric segment decoder to reduce system software requirements. The μPD7225 is manufactured with a low power consumption CMOS process allowing use of a single power supply between 2.7 V and 5.5 V. It is available in a space-saving 52-pin plastic flat package.

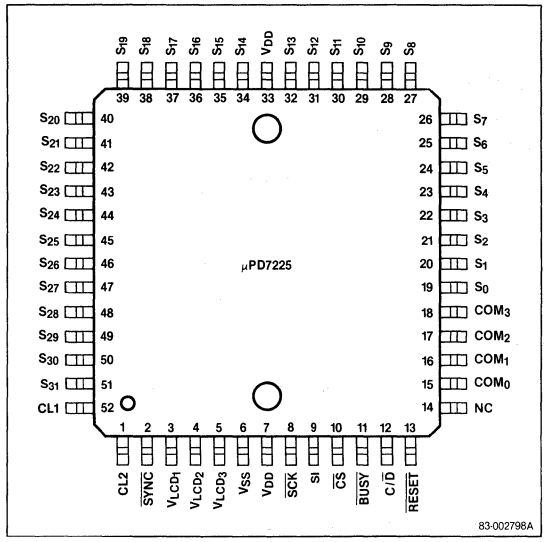
Features

- ☐ Single chip LCD controller with direct LCD drive
- ☐ Low cost serial interface to most microprocessors
- ☐ Compatible with
  - — 7-segment numeric LCD configurations up to 16 digits
  - — 14-segment alphanumeric LCD configurations up to 8 characters
- ☐ Selectable LCD drive configuration:
  - — Static, biplexed, triplexed, or quadruplexed
- ☐ 32-segment drivers
- ☐ Cascadable for larger LCD applications
- ☐ Selectable LCD bias voltage configuration:
  - — Static, 1/2 or 1/3
- ☐ Hardware logic blocks reduce system software requirements
  - — 8-bit serial interface
  - — Two 32 × 4-bit static RAMs for display data and blinking data storage
  - — Programmable segment decoding capability:
    - 16-character, 7-segment numeric decoder
    - 64-character, 14-segment USASCII alphanumeric decoder
  - — Programmable segment blinking capability
  - — Automatic synchronization of segment drivers with sequentially multiplexed backplane drivers
- ☐ Single power supply, variable from 2.7 V to 5.5 V
- ☐ Low power consumption CMOS technology
- ☐ Extended −40°C to +85°C temperature range available

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7225G-00	52-pin plastic miniflat	1 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	CL2	System clock output
2	$\overline{SYNC}$	Synchronization port
3–5	V_{LCD1}–V_{LCD3}	LCD bias voltage supply inputs
6	V_{SS}	Ground
7, 33	V_{DD}	Power
8	$\overline{SCK}$	Serial clock input
9	SI	Serial input
10	$\overline{CS}$	Chip select
11	$\overline{BUSY}$	Busy output
12	$C/\overline{D}$	Command or data select input
13	$\overline{RESET}$	Reset input
14	NC	No connection
15–18	COM_0–COM_3	LCD backplane driver outputs
19–32, 34–51	S_0–S_{31}	LCD segment driver outputs
52	CL1	System clock input

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Pin Functions

COM_0-COM_3

LCD backplane driver outputs.

S_0-S_{31}

LCD segment driver outputs.

V_{LCD1}-V_{LCD3}

LCD bias voltage supply inputs to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.

SI

Serial input from the microprocessor.

$\overline{SCK}$

Serial clock input. Synchronizes 8-bit serial data transfer from the microprocessor to the μPD7225.

$\overline{BUSY}$

Handshake output indicates the μPD7225 is ready to receive the next data byte.

C/$\overline{D}$

Command/data select input. Distinguishes serially input data byte as a command or as display data.

$\overline{CS}$

Chip select input. Enables the μPD7225 for data input from the microprocessor. When $\overline{CS}$ is deselected, the display can be updated.

$\overline{SYNC}$

Synchronization port. For multichip operation, tie all $\overline{SYNC}$ lines together.

CL1

System clock input. Connect CL1 either to CL2 with a 180 kΩ resistor, or to an external clock source.

CL2

System clock output. Connect CL2 to CL1 with a 180 kΩ resistor, or leave open.

$\overline{RESET}$

Reset input. R/C circuit or pulse initializes the μPD7225 after power-up.

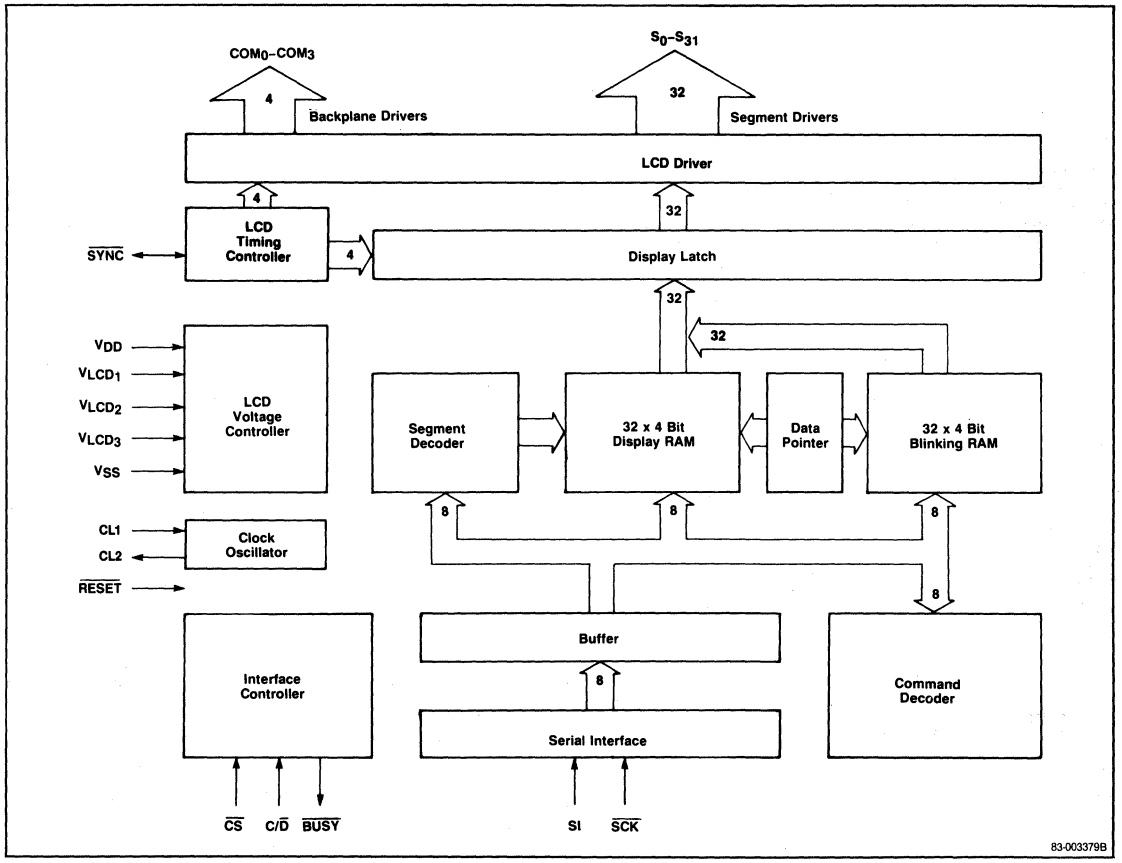
V_{DD}

Power supply positive. Apply single voltage ranging from 2.7 to 5.5 V for proper operation.

V_{SS}

Ground.

Block Diagram



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Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	−0.3 V to V_{DD} +0.3 V
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = -10°C$ to +70°C, $V_{DD} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	0		0.3 V_{DD}	V	
Input voltage high	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Output voltage low	V_{OL1}			0.5	V	$\overline{BUSY}$, $I_{OL} = 100\,\mu A$
	V_{OL2}			1.0	V	$I_{OL} = 900\,\mu A$, $\overline{SYNC}$
Output voltage high	V_{OH}	V_{DD} −0.5			V	$\overline{BUSY}$, $\overline{SYNC}$, $I_{OH} = -10\,\mu A$
Input leakage current low	I_{LIL}			−2	μA	$V_{IL} = 0\,V$
Input leakage current high	I_{LIH}			2	μA	$V_{IH} = V_{DD}$
Output leakage current	I_{LOL}			−2	μA	$V_{OL} = 0\,V$
	I_{LOH}			2	μA	$V_{OH} = V_{DD}$
Output short circuit current	I_{OS}			−300	μA	$\overline{SYNC}$, $V_{OS} = 1.0\,V$
Backplane driver output impedance	R_{COM}		5	7	kΩ	COM_0–COM_3, $V_{DD} \geq V_{LCD}$ (Note 1)
Segment driver output impedance	R_{SEG}		7	14	kΩ	S_0–S_{31}, $V_{DD} \geq V_{LCD}$ (Note 1)
Supply current	I_{DD}		100	250	μA	CL1 external clock, $f_\phi = 200$ kHz

Note:
(1) Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes.

DC Characteristics (cont)

$T_A = -0°C$ to +70°C, $V_{DD} = +2.7\,V$ to 5.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL1}	0		0.3 V_{DD}	V	Except $\overline{SCK}$
	V_{IL2}	0		0.2 V_{DD}	V	$\overline{SCK}$
Input voltage high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except $\overline{SCK}$
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{SCK}$
Output voltage low	V_{OL1}			0.5	V	$\overline{BUSY}$, $I_{OL} = 100\,\mu A$
	V_{OL2}			0.5	V	$I_{OL} = 400\,\mu A$, $\overline{SYNC}$
Output voltage high	V_{OH}	V_{DD} −0.75			V	$\overline{BUSY}$, $\overline{SYNC}$, $I_{OH} = -7\,\mu A$
Input leakage current low	I_{LIL}			−2	μA	$V_{IL} = 0\,V$
Input leakage current high	I_{LIH}			2	μA	$V_{IH} = V_{DD}$
Output leakage current	I_{LOL}			−2	μA	$V_{OL} = 0\,V$
	I_{LOH}			2	μA	$V_{OH} = V_{DD}$
Output short circuit current	I_{OS}			−200	μA	$\overline{SYNC}$, $V_{OS} = 0.5\,V$
Backplane driver output impedance	R_{COM}		6		kΩ	COM_0–COM_3, $V_{DD} \geq V_{LCD}$ (Note 1)
Segment driver output impedance	R_{SEG}		12		kΩ	S_0–S_{31}, $V_{DD} \geq V_{LCD}$ (Note 1)
Supply current	I_{DD}		30	100	μA	CL1 external clock, $V_{DD} = 3.0\,V \pm 10\%$, $f_\phi = 140$ kHz

Note:
(1) Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes.

Capacitance

$T_A = 25°C$, $f_\phi = 1$ MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions(1)
Input capacitance	C_I			10	pF	
Output capacitance	C_{O1}			20	pF	Except $\overline{BUSY}$
	C_{O2}			15	pF	$\overline{BUSY}$
I/O capacitance	C_{IO}			15	pF	$\overline{SYNC}$
Clock capacitance	C_ϕ			30	pF	CL1 input

Note:
(1) All unmeasured pins returned to 0 V.

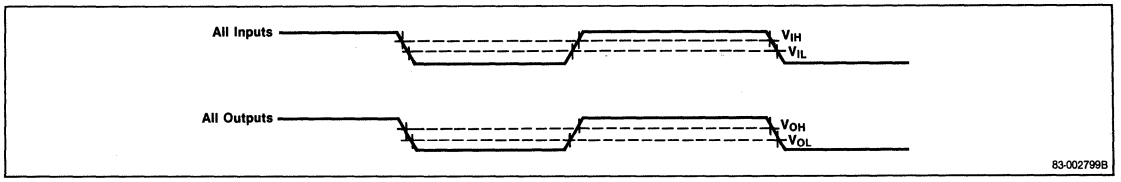
AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock frequency	f_ϕ	50		200	kHz	
	f_{OSC}	85	130	175	kHz	R = 180 kΩ ±5%
Clock pulse width low	$t_{\phi WL}$	2		16	μs	CL1, external clock
Clock pulse width high	$t_{\phi WH}$	2		16	μs	CL1, external clock
$\overline{SCK}$ cycle	t_{CYK}	900			ns	
$\overline{SCK}$ pulse width low	t_{KWL}	400			ns	
$\overline{SCK}$ pulse width high	t_{KWH}	400			ns	
$\overline{BUSY}$ ↑ to $\overline{SCK}$ ↓ hold time	t_{BHK}	0			ns	
SI setup time to $\overline{SCK}$ ↑	t_{ISK}	100			ns	
SI hold time after $\overline{SCK}$ ↑	t_{IHK}	200			ns	
8th $\overline{SCK}$ ↑ to $\overline{BUSY}$ ↓ delay time	t_{KDB}			3	μs	$C_L = 50$ pF
$\overline{CS}$ ↓ to $\overline{BUSY}$ ↓ delay time	t_{CDB}			1.5	μs	$C_L = 50$ pF
C / $\overline{D}$ setup time to 8th $\overline{SCK}$ ↑	t_{DSK}	9			μs	
C / $\overline{D}$ hold time after 8th $\overline{SCK}$ ↑	t_{DHK}	1			μs	
$\overline{CS}$ hold time after 8th $\overline{SCK}$ ↑	t_{CHK}	1			μs	
$\overline{CS}$ pulse width low	t_{CWL}	$8/f_\phi$			μs	
$\overline{CS}$ pulse width high	t_{CWH}	$8/f_\phi$			μs	

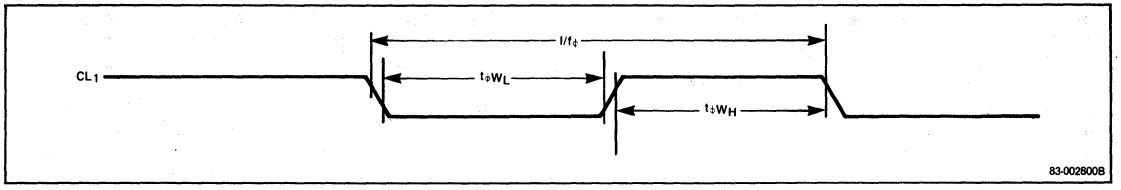
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock frequency	f_ϕ	50		140	kHz	
	f_{OSC}	50	100	140	kHz	R = 180 kΩ ±5%, $V_{DD} = 3.0V \pm 10\%$
Clock pulse width low	$t_{\phi WL}$	3		16	μs	CL1, external clock
Clock pulse width high	$t_{\phi WH}$	3		16	μs	CL1, external clock
$\overline{SCK}$ cycle	t_{CYK}	4			μs	
$\overline{SCK}$ pulse width low	t_{KWL}	1.8			μs	
$\overline{SCK}$ pulse width high	t_{KWH}	1.8			μs	
$\overline{BUSY}$ ↑ to $\overline{SCK}$ ↓ hold time	t_{BHK}	0			ns	
SI setup time to $\overline{SCK}$ ↑	t_{ISK}	1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{IHK}	1			μs	
8th $\overline{SCK}$ ↑ to $\overline{BUSY}$ ↓ delay time	t_{KDB}			5	μs	$C_L = 50$ pF
$\overline{CS}$ ↓ to $\overline{BUSY}$ ↓ delay time	t_{CDB}			5	μs	$C_L = 50$ pF
C / $\overline{D}$ setup time to 8th $\overline{SCK}$ ↑	t_{DSK}	18			μs	
C / $\overline{D}$ hold time after 8th $\overline{SCK}$ ↑	t_{DHK}	1			μs	
$\overline{CS}$ hold time after 8th $\overline{SCK}$ ↑	t_{CHK}	1			μs	
$\overline{CS}$ pulse width low	t_{CWL}	$8/f_\phi$			μs	
$\overline{CS}$ pulse width high	t_{CWH}	$8/f_\phi$			μs	
$\overline{SYNC}$ load capacitance	C_L			50	pF	$f_\phi = 200$ kHz

AC Timing Characteristics

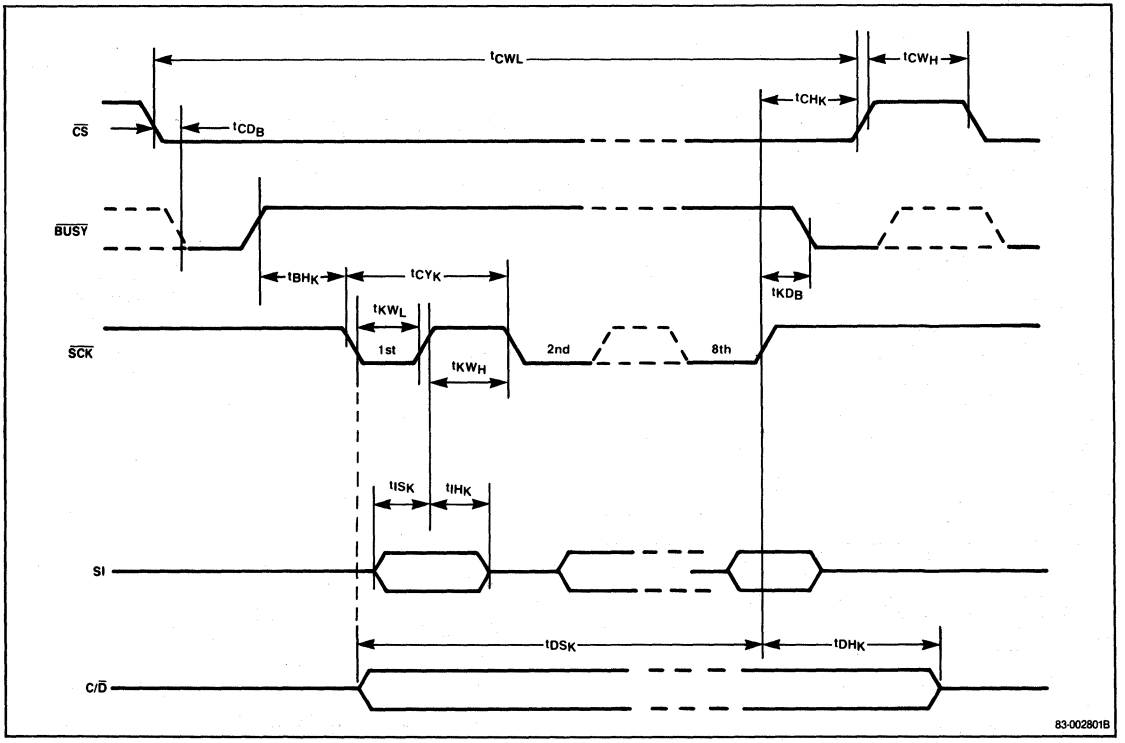


Timing Waveforms

Clock



Serial Interface



Instruction Set (Note 1)

Command	Description	Hex Code	Operation Code							
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Mode Set	Initialize the μPD7225, including selection of: 1) LCD drive configuration 2) LCD bias voltage configuration 3) LCD frame frequency	40–5F	0	1	0	d_4	d_3	d_2	d_1	d_0
Unsynchronous Data Transfer	Synchronize display RAM data transfer to display latch with $\overline{CS}$	30	0	0	1	1	0	0	0	0
Synchronous Data Transfer	Synchronize display RAM data transfer to display latch with LCD drive cycle	31	0	0	1	1	0	0	0	1
Interrupt Data Transfer	Interrupt display RAM data transfer to display latch	38	0	0	1	1	1	0	0	0
Load Data Pointer	Load data pointer with 5 bits of immediate data	E0–FF	1	1	1	d_4	d_3	d_2	d_1	d_0
Clear Display RAM	Clear the display RAM and reset the data pointer	20	0	0	1	0	0	0	0	0
Write Display RAM	Write 4 bits of immediate data to the display RAM location addressed by the data pointer; increment data pointer	D0–DF	1	1	0	1	d_3	d_2	d_1	d_0
AND Display RAM	Perform a logical AND between the display RAM data addressed by the data pointer and 4 bits of immediate data; write result to same display RAM location. Increment data pointer	90–9F	1	0	0	1	d_3	d_2	d_1	d_0
OR Display RAM	Perform a logical OR between the display RAM data addressed by the data pointer and 4 bits of immediate data; write result to same display RAM location; increment data pointer	B0–BF	1	0	1	1	d_3	d_2	d_1	d_0
Enable Segment Decoder	Start use of the segment decoder	15	0	0	0	1	0	1	0	1
Disable Segment Decoder	Stop use of the segment decoder	14	0	0	0	1	0	1	0	0
Enable Display	Turn on the LCD	11	0	0	0	1	0	0	0	1
Disable Display	Turn off the LCD	10	0	0	0	1	0	0	0	0
Clear Blinking RAM	Clear the blinking RAM and reset the data pointer	00	0	0	0	0	0	0	0	0
Write Blinking RAM	Write 4 bits of immediate data to the blinking RAM location addressed by the data pointer; increment data pointer	C0–CF	1	1	0	0	d_3	d_2	d_1	d_0
AND Blinking RAM	Perform a logical AND between blinking RAM data addressed by the data pointer and 4 bits of immediate data; write result to same blinking location; increment data pointer	80–8F	1	0	0	0	d_3	d_2	d_1	d_0
OR Blinking RAM	Perform a logical OR between blinking RAM data addressed by the data pointer and 4 bits of immediate data; write result to same blinking location; increment data pointer	A0–AF	1	0	1	0	d_3	d_2	d_1	d_0
Enable Blinking	Start segment blinking at the frequency specified by 1 bit of immediate data	1A–1B	0	0	0	1	1	0	1	d_0
Disable Blinking	Stop segment blinking	18	0	0	0	1	1	0	0	0

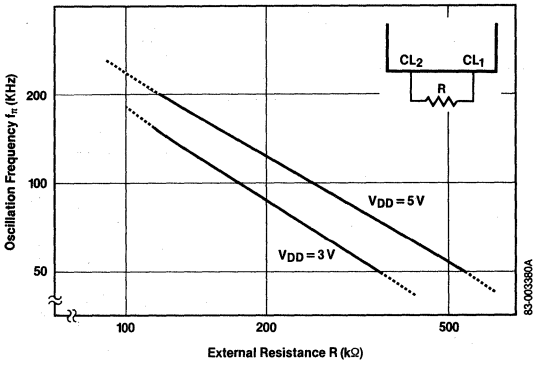
Note:
(1) Details of operation and application examples can be found in the μPD7225 Intelligent Alphanumeric LCD Controller/Driver Technical Manual.

7

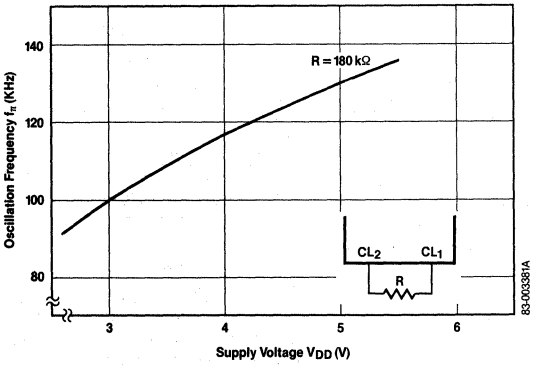
Operating Characteristics

$T_A = 25°C$

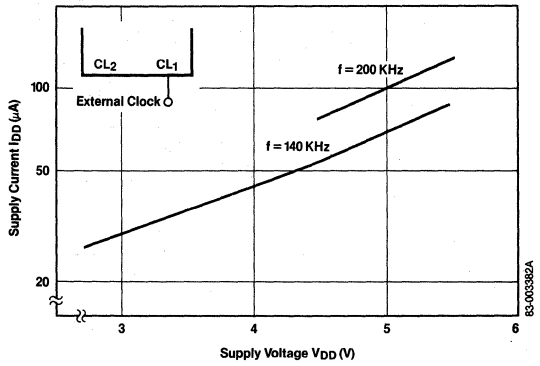
External Resistance vs Oscillation Frequency



Supply Voltage vs Oscillation Frequency



Supply Voltage vs Supply Current



7-Segment Numeric Data Decoder Character Set

Display Byte (HEX)	Character	Decoded Display RAM Data				
		Triplexed			Quadruplexed	
		Display RAM Address			Display RAM Address	
		n+2	n+1	n	n+1	n
00		3	5	3	D	7
01		0	0	3	0	6
02		2	7	1	E	3
03		0	7	3	A	7
04		1	2	3	3	6
05		1	7	2	B	5
06		3	7	2	F	5
07		0	1	3	0	7
08		3	7	3	F	7
09		1	7	3	B	7
0A		3	2	0	2	0
0B		3	7	0	F	1
0C		3	5	0	D	1
0D		0	6	0	A	0
0E		2	6	2	E	4
0F		0	0	0	0	0

14-Segment Alphanumeric Data Decoder Character Set

Display Byte (HEX)	Char.	Display RAM Address n+3	n+2	n+1	n	Display Byte (HEX)	Char.	Display RAM Address n+3	n+2	n+1	n	Display Byte (HEX)	Char.	Display RAM Address n+3	n+2	n+1	n	Display Byte (HEX)	Char.	Display RAM Address n+3	n+2	n+1	n
A0		0	0	0	0	B0		4	7	E	2	C0		A	7	C	0	D0		2	3	6	4
A1			Invalid			B1		0	6	0	0	C1		2	7	6	4	D1		0	7	E	8
A2			Invalid			B2		2	3	C	4	C2		8	7	8	5	D2		2	3	6	C
A3			Invalid			B3		2	7	8	4	C3		0	1	E	0	D3		1	5	8	4
A4			Invalid			B4		2	6	2	4	C4		8	7	8	1	D4		8	1	0	1
A5			Invalid			B5		2	5	A	4	C5		2	1	E	4	D5		0	6	E	0
A6			Invalid			B6		2	5	E	4	C6		2	1	6	4	D6		4	0	6	2
A7		0	0	0	2	B7		0	7	0	0	C7		0	5	E	4	D7		4	6	6	8
A8		0	0	0	A	B8		2	7	E	4	C8		2	6	6	4	D8		5	0	0	A
A9		5	0	0	0	B9		2	7	A	4	C9		8	1	8	1	D9		9	0	0	2
AA		F	0	0	F	BA			Invalid			CA		0	6	C	0	DA		4	1	8	2
AB		A	0	0	5	BB			Invalid			CB		2	0	6	A	DB			Invalid		
AC			Invalid			BC		4	0	8	2	CC		0	0	E	0	DC		1	0	0	8
AD		2	0	0	4	BD		2	0	8	4	CD		1	6	6	2	DD				Invalid	
AE			Invalid			BE		1	0	8	8	CE		1	6	6	8	DE			Invalid		
AF		4	0	0	2	BF			Invalid			CF		0	7	E	0	DF			Invalid		

μPD7227
CMOS, Intelligent, Dot-Matrix LCD Controller/Driver

Description

The μPD7227 intelligent dot-matrix LCD controller/driver is a peripheral device designed to interface most microprocessors with a wide variety of dot matrix LCDs. It can directly drive any multiplexed LCD organized as 8 rows by 40 columns, and is easily cascaded up to 16 rows and 280 columns. The μPD7227 is equipped with several hardware logic blocks, such as an 8-bit serial interface, ASCII character generator, 40 x 16 static RAM with full read/write capability, and an LCD timing controller; all of which reduce microprocessor system software requirements. The μPD7227 is manufactured with a single 5 V CMOS process, and is available in a space-saving 64-pin plastic flat package.

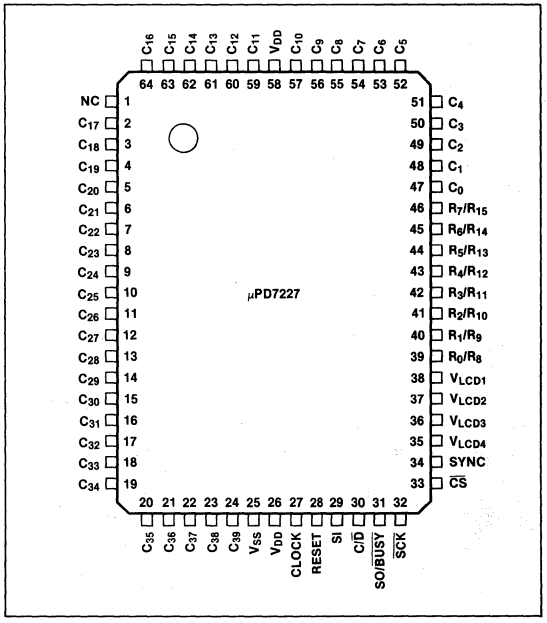
Features

- ☐ Single-chip LCD controller with direct LCD drive
- ☐ Compatible with most microprocessors
- ☐ Eight row drives
  - — Designed for dot-matrix LCD configurations up to 280 dots
  - — Designed for 5 x 7 dot-matrix character LCD configuration up to 8 characters
  - — Cascadable to 16 row drives
- ☐ 40 column drives
  - — Cascadable to 280 column drives
- ☐ Hardware logic blocks reduce system software requirements
  - — 8-bit serial interface for communication
  - — ASCII 5 x 7 dot-matrix character generator with 64-character vocabulary
  - — 40 x 16-bit static RAM for data storage, retrieval, and complete back-up memory capability.
  - — Voltage controller generates LCD bias voltages
  - — Timing controller synchronizes column drives with sequentially-multiplexed row drives
- ☐ Single +5 V power supply
- ☐ CMOS technology

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7227G-12	64-pin plastic miniflat	1000 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	NC	No connection
2-24, 47-57, 59-64	C_0-C_{39}	LCD column driver outputs
25	V_{SS}	Ground
26, 58	V_{DD}	Power
27	CLOCK	System clock input
28	RESET	Reset input
29	SI	Serial input
30	C/$\overline{D}$	Command or data select input
31	SO/$\overline{BUSY}$	Serial output or busy output
32	$\overline{SCK}$	Serial clock input
33	CS	Chip select input
34	SYNC	Synchronization port
35-38	V_{LCD1}-V_{LCD4}	LCD bias voltage supply inputs
39-46	R_0/R_8-R_7/R_{15}	LCD row driver outputs

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Pin Functions

C_0-C_{39}

LCD column driver outputs.

R0/8-R7/15

LCD row driver outputs.

V_{LCD1}-V_{LCD4}

LCD bias voltage supply inputs to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across VDD.

SI

Serial input from the microprocessor.

SO/$\overline{BUSY}$

Serial output from the μPD7227 to the microprocessor when in read mode and C/$\overline{D}$ is low. When $\overline{BUSY}$ (active low), handshake output indicates the μPD7227 is ready to receive/send the next data byte.

$\overline{SCK}$

Serial clock input. Synchronizes 8-bit serial data transfer between the microprocessor and μPD7227.

C/$\overline{D}$

Command/data select input. Distinguishes serially input data byte as a command or as display data.

$\overline{CS}$

Chip select input. Enables the μPD7227 for communication with the microprocessor.

SYNC

Synchronization port. For multichip operation, tie all SYNC lines together and configure with the MODE SET command.

CLOCK

System clock input. Connect to external clock source.

RESET

Reset input. RC circuit or pulse initializes the μPD7227 after power-up.

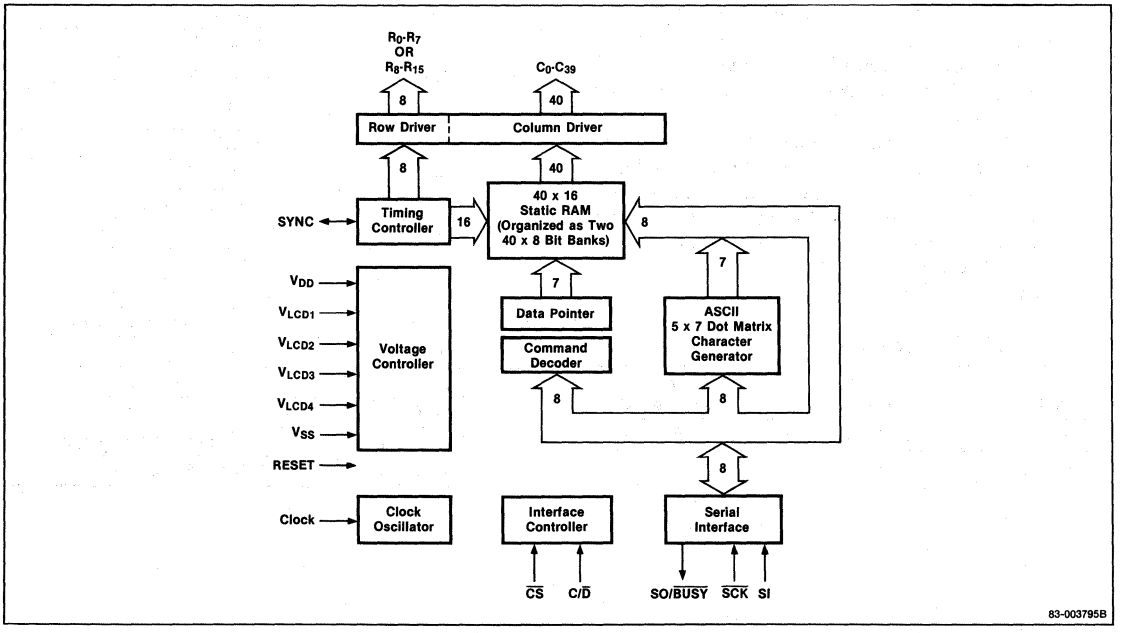
V_{DD}

Power supply positive. Apply single voltage 5 V ± 10% for proper operation.

V_{SS}

Ground.

Block Diagram



Absolute Maximum Ratings

T_A = 25°C

Power supply, V_{DD}	−0.3 V to +7.0 V
All inputs and outputs with respect to V_{CC}	−0.3 V to V_{DD} +0.3 V
Storage temperature, T_{STG}	−65°C to +150°C
Operating temperature, T_{OPT}	−10°C to +70°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input capacitance	C_I		10	pF	fϕ = 1 MHz
Output capacitance	C_O		25	pF	Unmeasured pins returned to ground.
Input/output capacitance	C_{IO}		15	pF SYNC	

DC Characteristics

T_A = −10°C to +70°C, V_{DD} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Input voltage, low	V_{IL}	0		0.3 V_{DD}	V	
Input leakage current, high	I_{LIH}			+10	μA	V_{IH} = V_{DD}
Input leakage current, low	I_{LIL}			−10	μA	V_{IH} = 0V
Output voltage, high	V_{OH1}	V_{DD}-0.5			V	SO/BUSY, I_{OH} = −400 μA
	V_{OH2}	V_{DD}-0.5			V	SYNC, I_{OH} = −100 μA
Output voltage, low	V_{OL1}			0.45	V	SO/BUSY, I_{OL} = +1.7 mA
				0.45	V	SYNC, I_{OL} = +100 μA
Output leakage current, high	I_{LOH}			+10	μA	V_{OH} = V_{DD}
Output leakage current, low	I_{LOL}			−10	μA	V_{OL} = 0V
LCD operating voltage	V_{LCD}	3.0		V_{DD}	V	8-row multiplexed LCD drive configuration
			V_{DD}		V	16-row multiplexed LCD drive configuration
Row drive output impedance	R_{ROW}		4	8	kΩ	
Column drive output impedance	R_{COLUMN}		10	15	kΩ	
Supply current	I_{DD}		200	400	μA	f0 = 400 KHz

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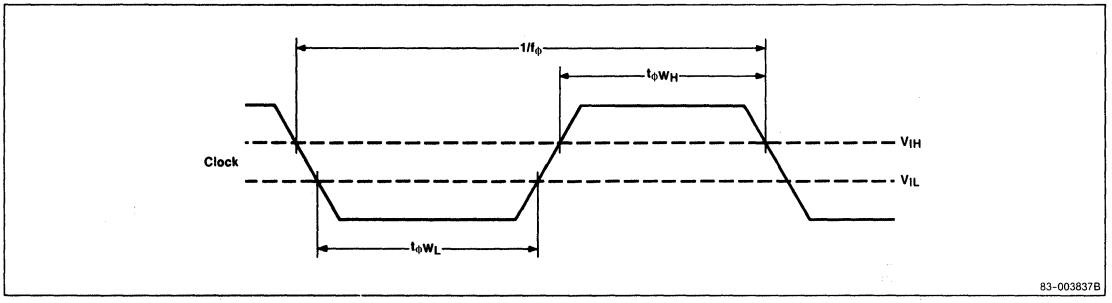
AC Characteristics

T_A = −10°C to +70°C, V_{DD} = +5.0V ± 10%

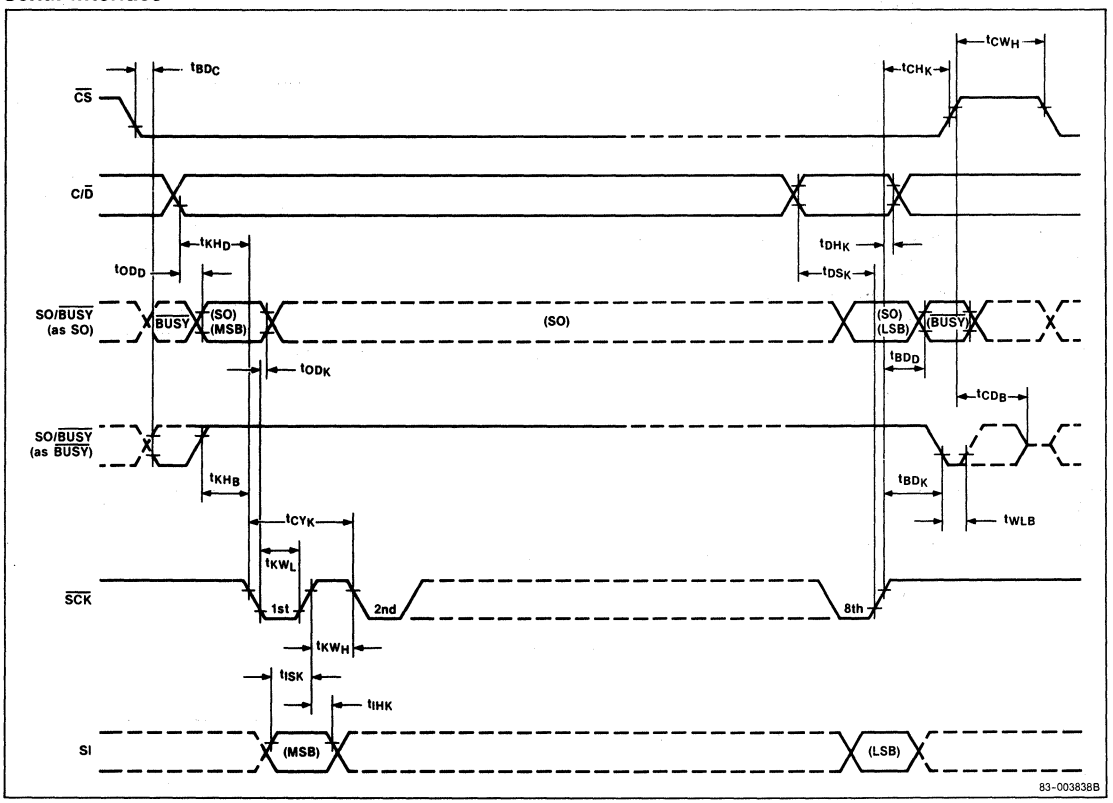
Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Clock frequency	f_ϕ	100	1000	KHz	
Clock pulse width high	$t_{\phi WH}$	400		ns	
Clock pulse width low	$t_{\phi WL}$	400		ns	
$\overline{SCK}$ cycle	t_{CYK}	0.9		μs	
$\overline{SCK}$ pulse width high	t_{KWH}	400		ns	
$\overline{SCK}$ pulse width low	t_{KWL}	400		ns	
$\overline{SCK}$ hold time after $\overline{BUSY}$↑	t_{KHB}	0		ns	
SI setup time to $\overline{SCK}$↑	t_{ISK}	100		ns	
SI hold time after $\overline{SCK}$↑	t_{IHK}	250		ns	
SO delay time after $\overline{SCK}$↓	t_{ODK}		320	ns	C_{LOAD} = 50 pF
SO delay time after C/$\overline{D}$↓	t_{ODD}		2	μs	
$\overline{SCK}$ hold time after C/$\overline{D}$↓	t_{KHD}	2		μs	
$\overline{BUSY}$ delay time after 8th $\overline{SCK}$↑	t_{BDK}		3	μs	C_{LOAD} = 50 pF
$\overline{BUSY}$ delay time after C/$\overline{D}$↑	t_{BDD}		2	μs	
$\overline{BUSY}$ delay time after $\overline{CS}$↓	t_{BDC}		2	μs	
C/$\overline{D}$ setup time to 8th $\overline{SCK}$↑	t_{DSK}	2		μs	
C/$\overline{D}$ hold time after 8th $\overline{SCK}$↑	t_{DHK}	2		μs	
$\overline{CS}$ hold time after 8th $\overline{SCK}$↑	t_{CHK}	2		μs	
$\overline{CS}$ pulse width high	t_{CWH}	2/f_ϕ		μs	
$\overline{CS}$↑ delay time to $\overline{BUSY}$ floating	t_{CDB}	2		μs	C_{LOAD} = 50 pF
SYNC load capacitance	C_{LOADS}		100	pF	
$\overline{BUSY}$ low level width	t_{WLB}	18	64	1/f_ϕ	C_{LOAD} = 50 pF

Timing Waveforms

Clock Waveform



Serial Interface



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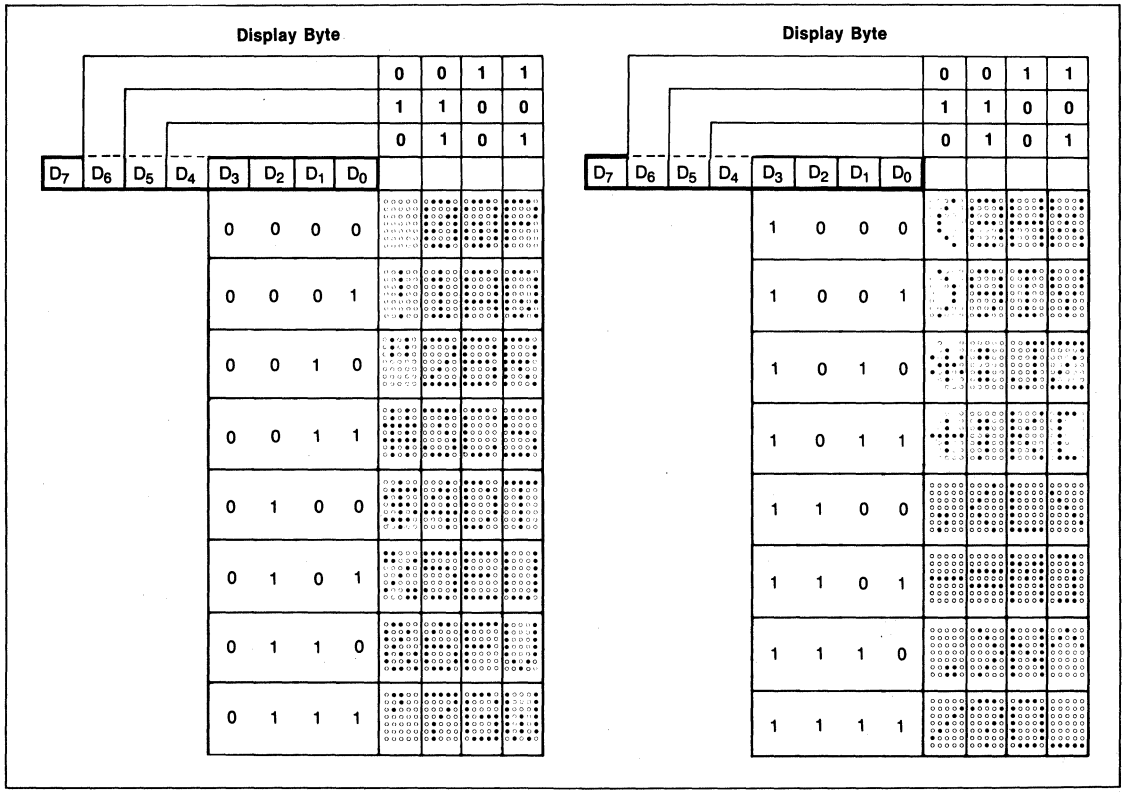
Command Summary

Command	Description	Instruction Code Binary D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
Mode Set	Initialize the μPD7227, including selection of 1. LCD drive configuration 2. Row driver port function 3. RAM bank 4. SYNC port function	0	0	0	1	1	D_2	D_1	D_0	18-1F
Frame Frequency Set	Set LCD frame frequency	0	0	0	1	0	D_2	D_1	D_0	10-14
Load Data Pointer	Load data pointer with 7 bits of immediate data	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0	80-E7
Write Mode	Write display byte in serial register to RAM location addressed by data pointer; modify data pointer	0	1	1	0	0	1	D_1	D_0	64-67
Read Mode	Load RAM contents addressed by data pointer into serial register for output; modify data pointer	0	1	1	0	0	0	D_1	D_0	60-63
AND Mode	Perform a logical AND between the display byte in the serial register and the RAM contents addressed by data pointer; write result to same RAM location; modify data pointer	0	1	1	0	1	1	D_1	D_0	6C-6F
OR Mode	Perform a logical OR between the display byte in the serial register and the RAM contents addressed by data pointer; write result to same RAM location; modify data pointer	0	1	1	0	1	0	D_1	D_0	68-6B
Character Mode	Decode display byte in serial register into 5 x 7 character with character generator; write character to RAM location addressed by data pointer; increment data pointer by 5	0	1	1	1	0	0	1	0	72
Set Bit	Set single bit of RAM location addressed by data pointer; modify data pointer	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
Reset Bit	Reset single bit of RAM location addressed by data pointer; modify data pointer	0	0	1	D_4	D_3	D_2	D_1	D_0	20-3F
Enable Display	Turn on the LCD	0	0	0	0	1	0	0	1	09
Disable Display	Turn off the ICD	0	0	0	0	1	0	0	0	08

Further details of operation can be found in the μPD7227 intelligent dot-matrix LCD controller/driver technical manual.

5×7 Character Set as Generated in μPD7227



μPD7228/28A
CMOS, Intelligent Dot-Matrix LCD Controller/Driver

Description

The μPD72228/28A controller/driver is a peripheral CMOS device designed to interface most microprocessors with a wide variety of dot-matrix LCDs. It can directly drive any multiplexed LCD organized as 8 rows by 50 columns or 16 rows by 42 columns.

The μPD7228/28A has a standby function to conserve power. It is equipped with an 8-bit serial interface, a 4-bit parallel interface, character generators, a 50 x 16 static RAM with full read/write capability, and an LCD timing controller, all of which reduce microprocessor system software requirements.

The μPD7228/28A operates with a single +5-volt power supply and is available in a space-saving 80-pin plastic miniflat package.

Features

- LCD direct drive
- 8-or 16-line multiplexing drive possible with single-chip
  - 8-line multiplexing: 400 (50 x 8) dots
  - 16-line multiplexing: 672 (42 x 16) dots
- 8-line or 16-line multiplexing drive with n chip configuration
  - 8-line multiplexing: n x 400 (n x 50 x 8) dots
  - 16-line multiplexing: n x 800 (n x 50 x 16) dots
- RAM: 2 x 50 x 8 bits for display data storage
- Programmer designated dot (graphics) display
- 5 x 7 dot-matrix display by on-chip character generator
  - ASCII (alphanumerics, others): 96 characters
  - JIS (Japan Industrial Standard), Katakana and others: 64 characters.
- Cursor operating command
- 8-bit serial interface compatible with μPD7500, μCOM-87/87LC
- 4-bit parallel interface compatible with μPD7500, μCOM-84/84C
- Standby function
- CMOS technology
- Single +5-volt power supply
- Extended −40 to +85°C temperature range (μPD7228A)

Ordering Information

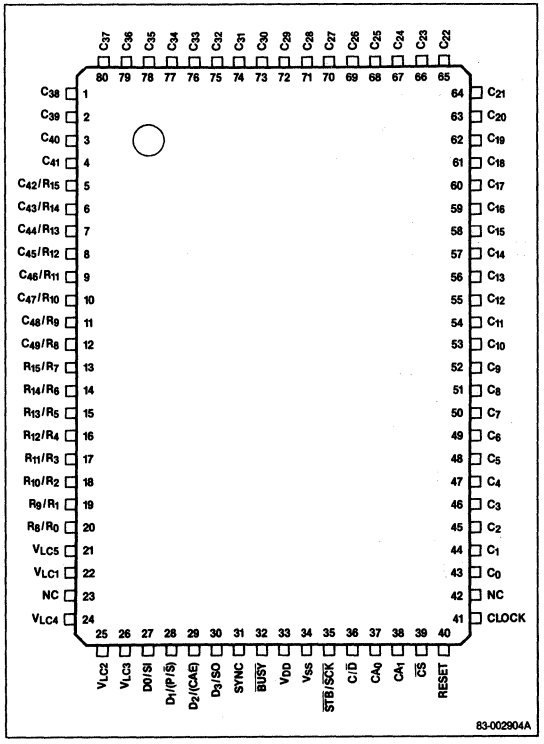
Part No.	Package
μPD7228G-12	80-pin plastic miniflat
μPD7228AG-12 (Note 1)	80-pin plastic miniflat

Notes:

(1) μPD7228A version has extended temperature range and LCD voltage range.

Pin Configuration

80-Pin Plastic Miniflat



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Pin Identification

Symbol	Function
C_0-C_{41}	LCD column drive outputs
C_{42}-C_{49}/R_{15}-R_8	LCD column/row drive outputs
R_{15}-R_8/R_7-R_8	LCD row drive outputs
V_{LC1}-V_{LC5}	LCD power supply
NC	No connection
D_0/S_I	Data bus 0/Serial input
D_1(P/$\overline{S}$)	Data bus 1 (Parallel/serial select)
D_2(CAE)	Data bus 2 (Chip address enable)
D_3/SO	Data bus 3/Serial output
SYNC	Synchronization signal input/output
$\overline{BUSY}$	Busy signal output
V_{DD}	Power supply
V_{SS}	Ground
$\overline{STB}/\overline{SCK}$	Strobe/Serial clock input
C/$\overline{D}$	Command/data select input
CA_0, CA_1	Chip address select inputs
$\overline{CS}$	Chip select input
RESET	Reset signal input
CLOCK	System clock input

PIN FUNCTIONS

D_0-D_3 (Data Bus)

In parallel interface mode, D_0-D_3 are input/output pins for 4-bit parallel data. Data on these lines is read at the rising edge of $\overline{STB}$. The 4 bits read on the first $\overline{STB}$ are loaded into the highest 4 bits of the serial/parallel register. The 4 bits read on the second $\overline{STB}$ are loaded into the lowest 4 bits of the register.

The contents of the serial/parallel register are output to these pins on the falling edge of $\overline{STB}$. As in the above case, the high-order 4 bits correspond to the first $\overline{STB}$, and the low-order 4 bits to the second $\overline{STB}$.

In serial interface mode, D_0 is a serial data input pin and D_3 is a serial data output pin. D_1 selects serial or parallel interface mode (P/$\overline{S}$), and D_2 is the chip address enable pin (CAE).

SI Serial Data-In (Input Common to D_0)

In serial interface mode, SI inputs serial data. Data on SI is loaded into the serial/parallel register at the rising edge of $\overline{SCK}$. The first data loaded is the most significant bit. To eliminate noise errors, SI uses the Schmitt-trigger input.

SO Serial Data-Out (Output Common to D_3)

In serial interface mode, SO is an output pin for serial data. The contents of the serial/parallel register are output to the SO pin, beginning with the most significant bit, on the falling edge of $\overline{SCK}$.

P/S Parallel/Serial Select (Input Common to D_1)

This pin sets parallel interface mode if it is high at the falling edge of RESET (at reset release). If it is low at the falling edge of RESET, it selects serial interface mode. The Schmitt-trigger prevents noise errors.

CAE Chip Address Enable (Input Common to D_2)

This pin is used only during serial interface mode; that is, when P/$\overline{S}$ is low at the falling edge of RESET. To enable chip addressing, the CAE line must be high at the falling edge of RESET. In parallel interface mode (when P/$\overline{S}$ is high at the falling edge of RESET), the chip addressing function is enabled regardless of the logic state of CAE at the falling edge of RESET. The Schmitt-trigger input prevents noise errors.

CA_0-CA_1 (Chip Address)

These input pins allow you to address the μPD7228/28A in a multichip configuration used for driving logic displays. During parallel interface mode, CA_0 and CA_1 are compared to chip address data sent from the CPU regardless of CAE status during a reset.

However, during serial interface mode, CA_0 and CA_1 are compared with chip address data from the CPU only when CAE enables chip addressing.

In multichip configurations, the device is selected if $\overline{CS}$ = 0 and CA_0 and CA_1 match the chip address generated by the CPU. This address is the low 2 bits of the first 8-bit data input after $\overline{CS}$ = 0.

In serial interface mode, if chip address selection is not used, connect CA_0 and CA_1 to ground.

$\overline{CS}$ (Chip Select)

$\overline{CS}$ is an active-low chip select input pin. When you are not using the chip address selection function, the STB/$\overline{SCK}$ and C/$\overline{D}$ inputs are enabled if a low input is sent to $\overline{CS}$.

When you are using the chip address select function, if $\overline{CS}$ is brought low and the chip address data matches CA_0-CA_1, then $\overline{STB}/\overline{SCK}$ and C/$\overline{D}$ are enabled.

When $\overline{CS}$ is made high, D_0-D_3 and $\overline{BUSY}$ are placed in a high-impedance state. The Schmitt-trigger input prevents noise errors.

$\overline{STB}$/$\overline{SCK}$ (Strobe/Serial Clock)

In parallel interface mode, this is the strobe signal input pin ($\overline{STB}$) for 4-bit parallel input and output data, In serial interface mode, this is the serial clock input pin ($\overline{SCK}$) for serial input and output data.

C/$\overline{D}$ (Command/Data)

This pin specifies whether the parallel or serial input is a command or data. Bring C/$\overline{D}$ high to input a command, and low to input data.

In parallel interface mode, the contents of C/$\overline{D}$ are latched at the rising edge of the second $\overline{STB}$. Perform any changes to the C/$\overline{D}$ input before the falling edge of the first $\overline{STB}$. When outputting data, hold C/$\overline{D}$ low, whether serial or parallel.

In serial interface mode, the contents of C/$\overline{D}$ are latched at the rising edge of the eighth $\overline{SCK}$.

The Schmitt-trigger input prevents noise errors.

$\overline{BUSY}$ (Busy)

This pin outputs a busy signal to the CPU to warn that the μPD7228/28A is internally busy. When this signal is low, the CPU cannot read/write the μPD7228/28A.

In the parallel interface mode, $\overline{BUSY}$ is forced low at the rising edge of the second $\overline{STB}$. In the serial interface mode, $\overline{BUSY}$ is forced low at the rising edge of the eighth $\overline{SCK}$.

If a chip is deselected ($\overline{CS}$ = high or chip address data does not match), the $\overline{BUSY}$ pin is placed in the high-impedance state.

SYNC (Synchronous)

In a multichip configuration, the SYNC signal synchronizes the phases of the LCD drive ac signals (row/column signal) among all the μPD7228/28A's within the frame period. It uses the row drive signal as a common signal.

If one chip is designated master, its SYNC pin is in output mode and the remaining chips are made slaves. Their SYNC pins are put in input mode. The SMM command selects input or output mode. The master chip outputs a SYNC pulse in the last cycle of each frame. The slave chip reads the SYNC pulse from its own SYNC input for synchronization with the master chip.

In a single-chip configuration, set the SYNC pin in the input or output mode. If you choose input mode, connect the SYNC pin to V_{SS}; conversely, if you choose output mode, the SYNC pin must be open.

Figures 1 and 2 show the output timing for the SYNC pulse in 8- and 16-line multiplexing.

Figure 1. SYNC Signal in 8-Line Multiplexing

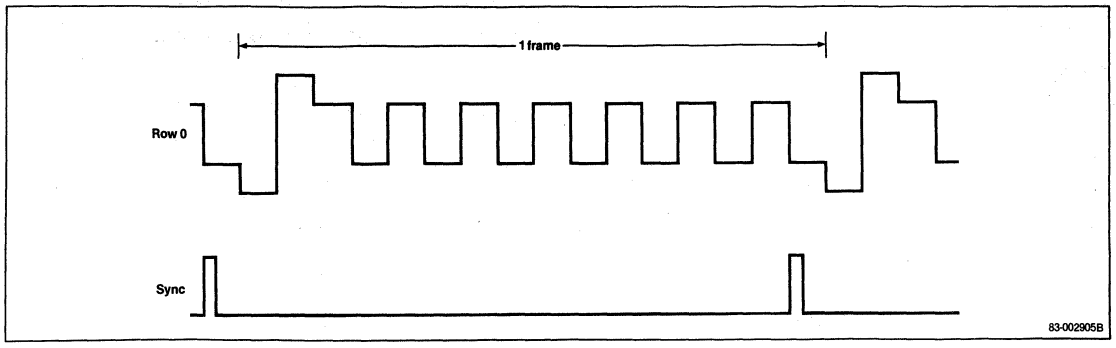

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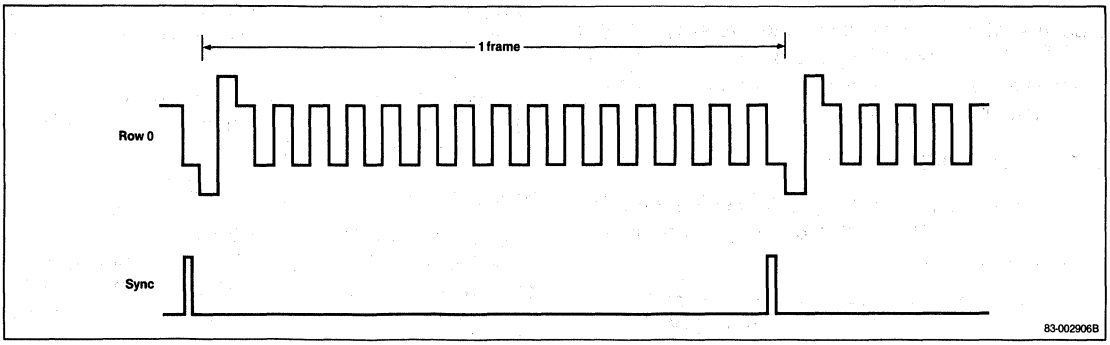
Figure 2. SYNC Signal in 16-Line Multiplexing



C_0-C_{41} (Column)

These pins output the column drive signals for the LCD.

C_{42}-C_{49}/R_{15}-R_8 (Column/Row)

These pins are column drive outputs (C_{42}-C_{49}, 50 x 8 mode) or row drive outputs (R_{15}-R_8, 42 x 16 mode), according to the SMM command.

R_{15}-R_8/R_7-R_0 (Row)

These pins are row drive outputs for rows R_{15}-R_8 or R_7-R_0, according to the SMM command.

V_{LC1}-V_{LC5} (LCD Drive Voltage Supply)

These are reference voltage input pins for determining the voltage level of the LCD column/row drive signals.

CLOCK (Clock)

This is the external clock input pin.

RESET (Reset)

This is the active-high reset signal input pin. It has priority over all operations. You can also use it to release standby mode and begin low power data retention.

V_{DD} (Power Supply)

This is a positive power supply pin.

V_{SS} (Ground)

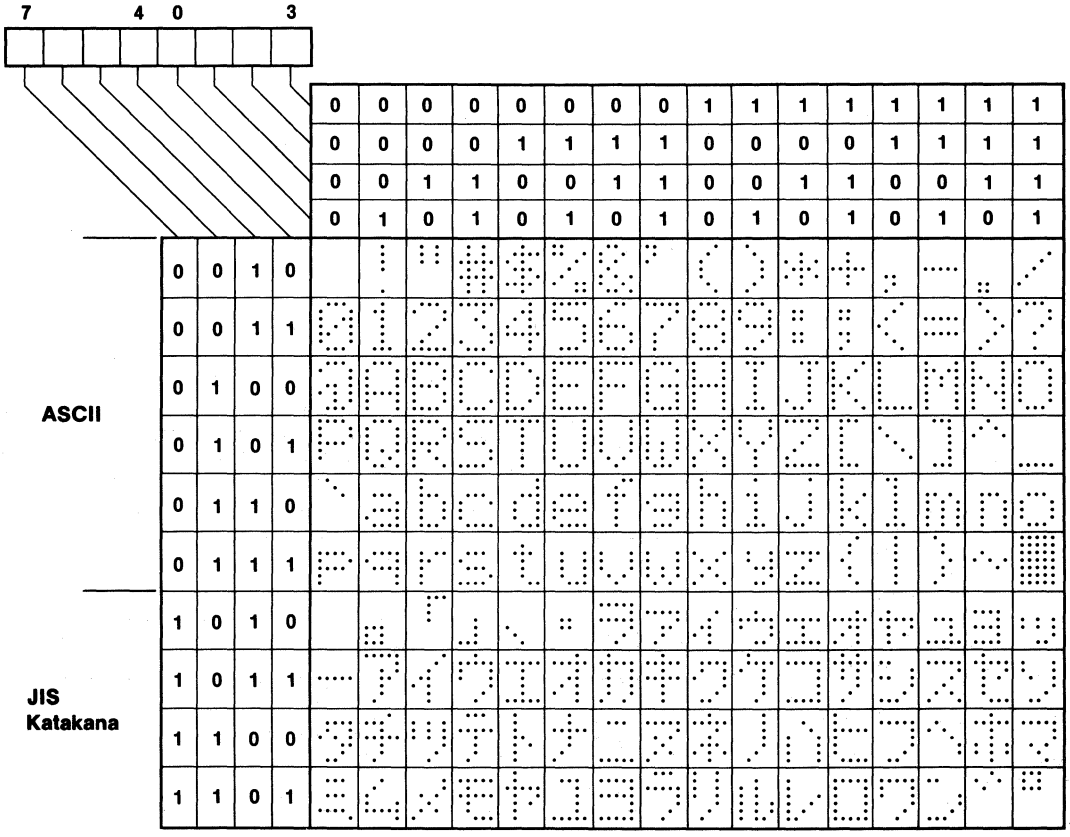
This is ground (GND).

COMMANDS FOR μPD7228/28A

The μPD7228/28A has 16 types of commands, each command consisting of one byte (8 bits).

Figure 3 shows the character codes and display patterns.

Figure 3. Character Codes and Display Patterns



Notes:

(1) The character generator transfers 7-bit dot patterns five times to the five contiguous addresses of data memory.

(2) ASCII Characters, 96 (20H-7FH)

Upper case	26
Lower case	26
Numbers	10
Symbols	34

(3) JIS Characters, 64 (A0H-DFH)

Katakana	55
Symbols	9

(4) Because the character generator does not use bit 7 of data memory, dot R7 in 8 time-division mode and dots R7 and R15 in 16 time-division mode, corresponding to the most significant bits, can be used as cursor independent of the character generator. Use the cursor manipulation commands WRCURS and CLCURS.

83-002913B

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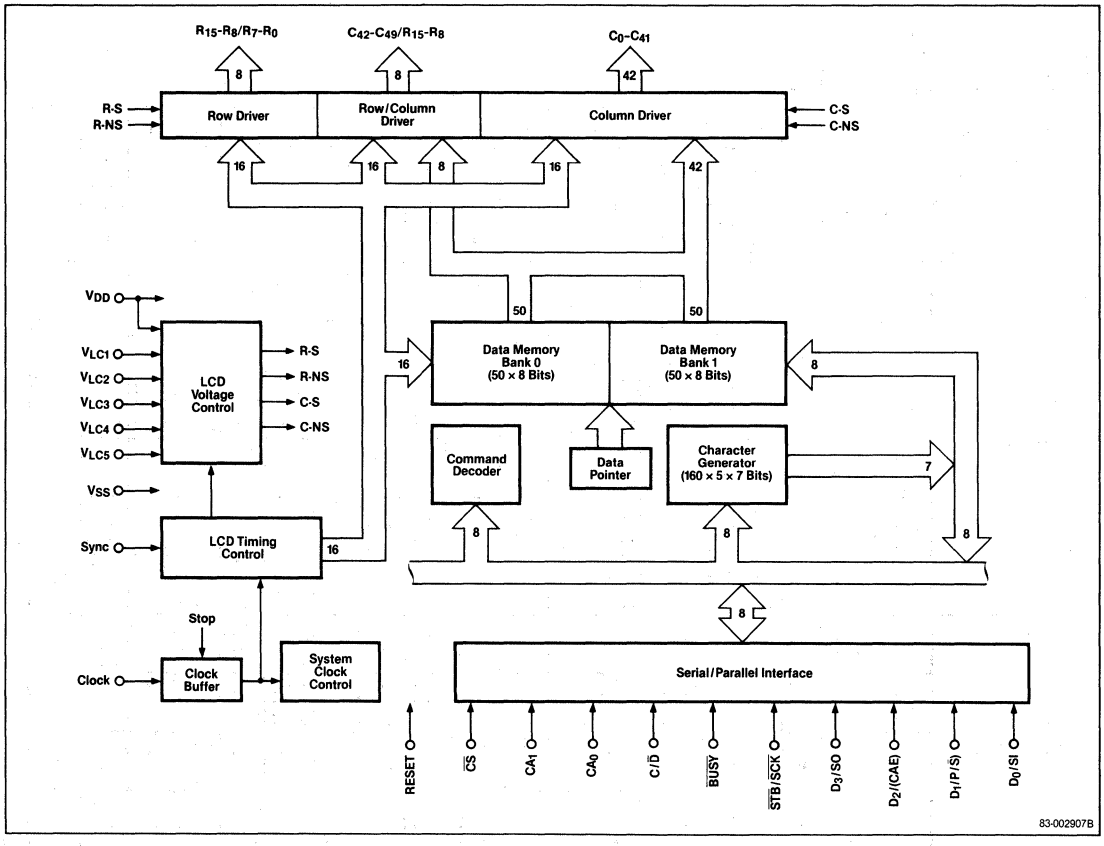
Block Diagram



Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	−0.3 V to V_{DD} +0.3 V
LCD operating voltage, V_{LCD} (7228A)	4.5 to 12.5 V
Operating temperature, T_{OPT}	
7228	−10 to +70°C
7228A	−40 to +85°C

Capacitance

T_A = 25°C; V_{DD} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_I			10	pF	Return unmeasured pins to 0 V.
Output capacitance	C_O			25	pF	
I/O capacitance	C_{IO}			15	pF	

DC Characteristics

T_A = −10 to +70°C V_{DD} = +5 V ±10%

Parameter	Symbol	μPD7228 Min	μPD7228 Typ	μPD7228 Max	μPD7228A Min	μPD7228A Typ	μPD7228A Max	Unit	Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	0.7 V_{DD}		V_{DD}	V	Except $\overline{SCK}$
	V_{IH2}	0.8 V_{DD}		V_{DD}	0.8 V_{DD}		V_{DD}	V	$\overline{SCK}$
Input voltage, low	V_{IL}	0		0.3 V_{DD}	0		0.3 V_{DD}	V	
Output voltage, high	V_{OH1}	V_{DD} − 0.5			V_{DD} − 0.5			V	$\overline{BUSY}$, D_0-D_3; I_{OH} = −400 μA
	V_{OH2}	V_{DD} − 0.5			V_{DD} − 0.5			V	SYNC; I_{OH} = −100 μA
Output voltage, low	V_{OL1}			0.45			0.5	V	$\overline{BUSY}$, D_0-D_3; I_{OL} = 1.7 mA
	V_{OL2}			0.45			0.5	V	SYNC; I_{OL} = 100 μA
Input leakage current, high	I_{LIH}			10			10	μA	V_I = V_{DD}
Input leakage current, low	I_{LIL}			−10			−10	μA	V_I = 0 V
Output leakage current, high	I_{LOH}			10			10	μA	V_O = V_{DD}
Output leakage current, low	I_{LOL}			−10			−10	μA	V_I = 0 V
LCD operating voltage	V_{LCD}	3.0		V_{DD}	4.5		12.5	V	
Row output impedance	R_{ROW}		4	8		8	16	kΩ	
Row/column output impedance	$R_{ROW/COL}$		5	10		7.5	20	kΩ	
Column output impedance	R_{COL}		10	15		15	30	kΩ	
Supply current	I_{DD1}		200	400		250	600	μA	Operating mode; f_C = 400 kHz
	I_{DD2}			20			25	μA	Stop mode; CLK = 0 V

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	μPD7228 Min	μPD7228 Typ	μPD7228 Max	μPD7228A Min	μPD7228A Typ	μPD7228A Max	Unit	Conditions
Common Operation									
Clock frequency	f_C	100		1100	100		1100	kHz	
Clock pulse width, high	t_{WHC}	350			350			ns	
Clock pulse width, low	t_{WLC}	350			350			ns	
$\overline{RESET}$ pulse width, high	t_{HRS}	4			4			μs	
$\overline{BUSY}$ delay time from $\overline{CS}$ ↓	t_{DCSB}			2			3	μs	C_L = 50 pF
$\overline{CS}$ ↑ delay time to $\overline{BUSY}$ floating	t_{DCSBF}			4			5	μs	C_L = 50 pF
$\overline{CS}$ high-level time	t_{WHCS}	4			4			μs	
SYNC load capacitance	C_{LSY}			100			100	pF	
Data setup time to RESET ↓	t_{SDR}	0			0			μs	
Data hold time from RESET ↓	t_{HRD}	4			5			μs	
Serial Interface Operation									
$\overline{SCK}$ cycle	t_{CYK}	0.9			0.9			μs	
$\overline{SCK}$ pulse width, high	t_{WHK}	400			400			ns	
$\overline{SCK}$ pulse width, low	t_{WLK}	400			400			ns	
$\overline{SCK}$ hold time from $\overline{BUSY}$ ↑	t_{HBK}	0			0			ns	
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	100			120			ns	
SI hold time from $\overline{SCK}$ ↑	t_{HKI}	250			270			ns	

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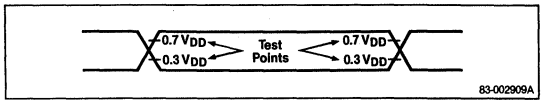
AC Characteristics (cont)

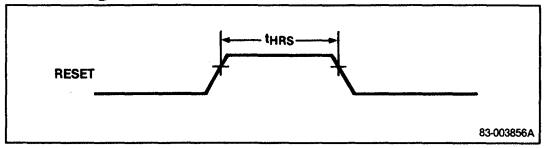
Parameter	Symbol	μPD7228			μPD7228A			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max		
SO delay time from $\overline{SCK}$ ↓	t_{DKO}			320			350	ns	C_L = 50 pF
$\overline{BUSY}$ delay time from eighth $\overline{SCK}$ ↑	t_{DKB}			3			4	μs	
$\overline{BUSY}$ low-level time	t_{WLB}	18		64	18		64	$1/f_C$	
C/$\overline{D}$ setup time to first $\overline{SCK}$ ↓	t_{SDK}	0			0			μs	
C/$\overline{D}$ hold time from eighth $\overline{SCK}$ ↑	t_{HKD}	2			3			μs	
$\overline{CS}$ hold time from eighth $\overline{SCK}$ ↑	t_{HKCS}	2			5			μs	
Parallel Interface Operation									
Input command setup time to $\overline{STB}$ ↓	t_A	100			120			ns	C_L = 80 pF
Input command hold time from $\overline{STB}$ ↓	t_B	90			110			ns	C_L = 20 pF
Input data setup time to $\overline{STB}$ ↑	t_C	230			250			ns	C_L = 80 pF
Input data hold time from $\overline{STB}$ ↑	t_D	50			70			ns	C_L = 20 pF
Output data delay time	t_{ACC}	90		650	90		750	ns	C_L = 80 pF
Output data hold time	t_H	0		150	0		150	ns	C_L = 20 pF
$\overline{STB}$ pulse width low	t_{SL}	700			700			ns	
$\overline{STB}$ high-level time	t_{SH}	1			1			μs	
$\overline{STB}$ hold time from $\overline{BUSY}$ ↑	t_{HBS}	0			0			μs	
$\overline{BUSY}$ delay time from second $\overline{STB}$ ↑	t_{DSB}			3			4	μs	
C/$\overline{D}$ setup time to first $\overline{STB}$ ↓	t_{SDS}	0			0			μs	
C/$\overline{D}$ hold time from second $\overline{STB}$ ↑	t_{HSD}	2			3			μs	
$\overline{CS}$ hold time from second $\overline{STB}$ ↑	t_{HSCS}	2			3			μs	

Timing Waveforms

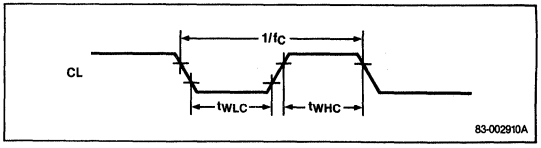
AC Timing Test Points



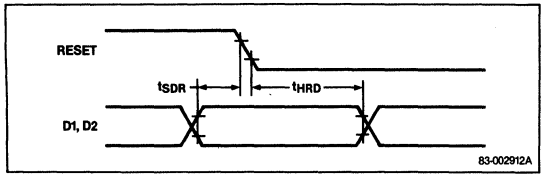
Reset Signal



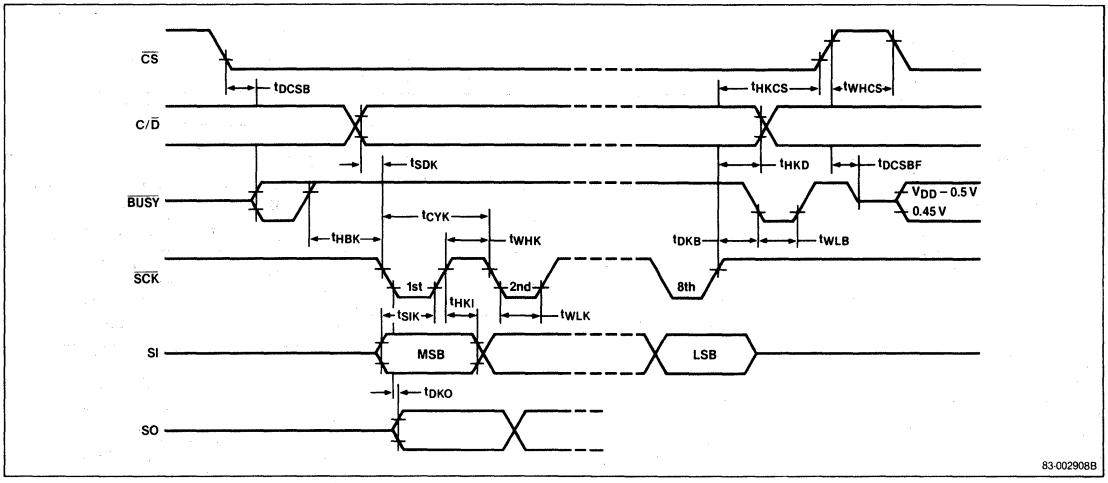
Clock Waveform



Interface



Serial Interface



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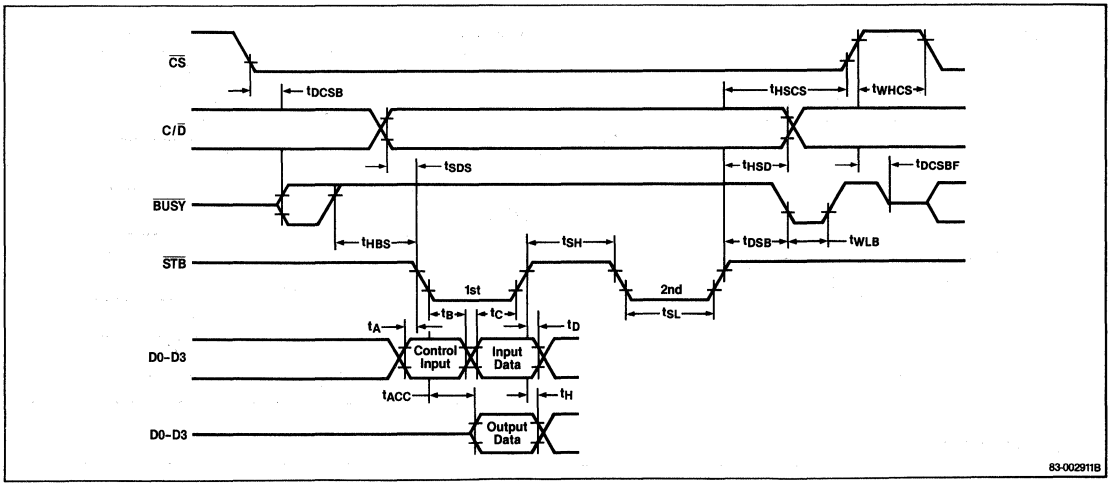
Parallel Interface



Command Summary

Mnemonic	Operation	Instruction Code								Hex Code
SFF	Set frame frequency	0	0	0	1	0	F_2	F_1	F_0	10H-14H
SMM	Set multiplexing mode	0	0	0	1	1	M_2	M_1	M_0	18H-1FH
DISP OFF	Display off	0	0	0	0	1	0	0	0	08H
DISP ON	Display on	0	0	0	0	1	0	0	1	09H
LDPI	Load data pointer with immediate	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0	80H-B1H, C0H-F1H
SRM	Set read mode	0	1	1	0	0	0	I_1	I_0	60H-63H
SWM	Set write mode	0	1	1	0	0	1	I_1	I_0	64H-67H
SORM	Set OR mode	0	1	1	0	1	0	I_1	I_0	68H-6BH
SANDM	Set AND mode	0	1	1	0	1	1	I_1	I_0	6CH-6FH
SCML	Set character mode with left entry	0	1	1	1	0	0	0	1	71H
SCMR	Set character mode with right entry	0	1	1	1	0	0	1	0	72H
BRESET	Bit reset	0	0	1	B_2	B_1	B_0	J_1	J_0	20H-3FH
BSET	Bit set	0	1	0	B_2	B_1	B_0	J_1	J_0	40H-5FH
CLCURS	Clear cursor	0	1	1	1	1	1	0	0	7CH
WRCURS	Write cursor	0	1	1	1	1	1	0	1	7DH
STOP	Set stop mode	0	0	0	0	0	0	0	1	01H

B_2-B_0 Specifies a data memory bit

D_6-D_0 Immediate data

F_2-F_0 Specifies frame frequency as a submultiple of clock frequency

I_1-I_0 Specifies modification of data pointer contents after byte data is processed

J_1-J_0 Specifies modification of data pointer contents after bit is set or reset

M_2-M_0 Specifies data memory bank, number of rows, functions of row/column drivers, and SYNC pin mode

NEC

MEMORIES FOR GRAPHICS APPLICATIONS

8

Section 8
Memories for Graphics Applications

μPD41264/42273/42274
Dual-Port Graphics Buffers

Description

NEC's dual-port graphics buffers are equipped with a 4-bit random access port and a 4-bit serial read port. On each device, the random access port is used by the host CPU to read or write data addressed in any desired order. The serial read port is connected to an internal data register through a serial read output circuit.

The random access port also has a write-per-bit capability that allows each of the four data bits to be individually selected or masked for a write cycle. Furthermore, a flash write option with write-per-bit control on the μPD42274 is provided by the FWE pin and enables data in the color register to be written to a selected row in the random access port.

The devices feature fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port, however, continues to operate normally. Following the clock transition of a data transfer, the serial read output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL- compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

Features

- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page capabilities
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - Hidden refreshing by means of $\overline{CAS}$-controlled output
  - Write-per-bit capability regarding four I/O bits
  - Write bit selection multiplexed on IO_0-IO_3
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read operation specified by column address inputs
  - Transfer of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time or standby operation of serial port
- Fast serial read operation by means of serial control pins
  - Serial data output on SO_0-SO_3
  - Direct connection of multiple serial outputs for extension of data length

Ordering Information

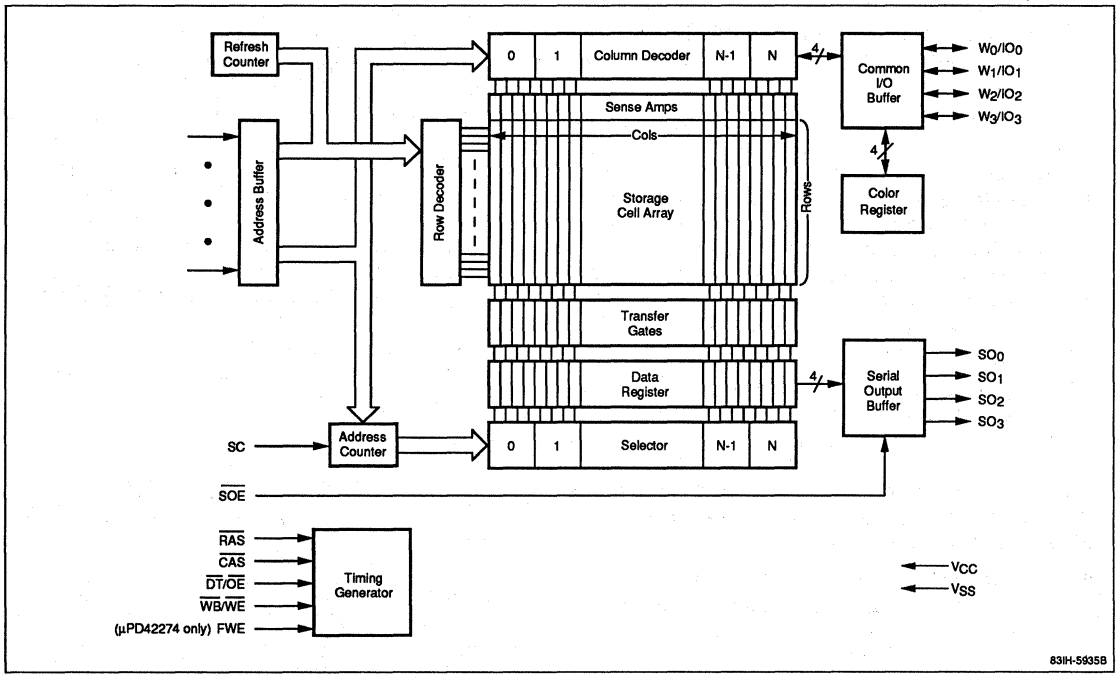
Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD41264C-12	120 ns	40 ns	24-pin plastic DIP
C-15	150 ns	60 ns	
μPD41264V-12	120 ns	40 ns	24-pin plastic ZIP
V-15	150 ns	60 ns	
μPD42273LE-10	100 ns	30 ns	28-pin plastic SOJ
LE-12	120 ns	40 ns	
μPD42273V-10	100 ns	30 ns	28-pin plastic ZIP
V-12	120 ns	40 ns	
μPD42274LE-10	100 ns	30 ns	28-pin plastic SOJ
LE-12	120 ns	40 ns	
μPD42274V-10	100 ns	30 ns	28-pin plastic ZIP
V-12	120 ns	40 ns	

Contact your NEC sales representative for copies of the complete data sheets.

Comparison of Dual-Port Graphics Buffers

Features	μPD41264	μPD42273	μPD42274
Density	256K	1 Meg	1 Meg
Organization	64K x 4	256K x 4	256K x 4
Serial data register	256 x 4	512 x 4	512 x 4
Refresh period	4 ms	8 ms	8 ms
Refresh addresses	256	512	512
Flash write	No	No	Yes
Process	NMOS	CMOS	CMOS
Pins	24	28	28

Block Diagram



Description

NEC's dual-port line buffers are fabricated with a silicon-gate CMOS process and can execute asynchronous read and write cycles at high speed. They also can be used as a time axis converter or a digital delay line of up to the length of the line buffer (at maximum frequency, the minimum delay line length is 10 bits).

Applications include NTSC and PAL digital television systems, image processing in facsimile machines, plain paper copiers, video systems, and other optical scanners; time base correction in video playback systems; and data communication buffering in multiprocessor systems and local area networks.

Features

- Dual-port operation
- Image processing and data communications systems applications
- Asynchronous and simultaneous read/write operation

Ordering Information

Device		Read Cycle Time (min)	Write Cycle Time (max)	Package
μPD42101	C-3	34 ns	34 ns	24-pin plastic DIP
	C-2	34 ns	69 ns	
	C-1	69 ns	69 ns	
μPD42101	G-3	34 ns	34 ns	24-pin plastic miniflat
	G-2	34 ns	69 ns	
	G-1	69 ns	69 ns	
μPD42102	C-3	28 ns	28 ns	24-pin plastic DIP
	C-2	28 ns	56 ns	
	C-1	56 ns	56 ns	
μPD42102	G-3	28 ns	28 ns	24-pin plastic miniflat
	G-2	28 ns	28 ns	
	G-1	56 ns	56 ns	
μPD42505	C-50	50 ns	50 ns	24-pin plastic DIP
	C-75	75 ns	75 ns	
	C-50H	50 ns	50 ns	
	C-75H	75 ns	75 ns	
μPD42505	V-50	50 ns	50 ns	28-pin plastic ZIP
	V-75	75 ns	75 ns	
	V-50H	50 ns	50 ns	
	V-75H	75 ns	75 ns	

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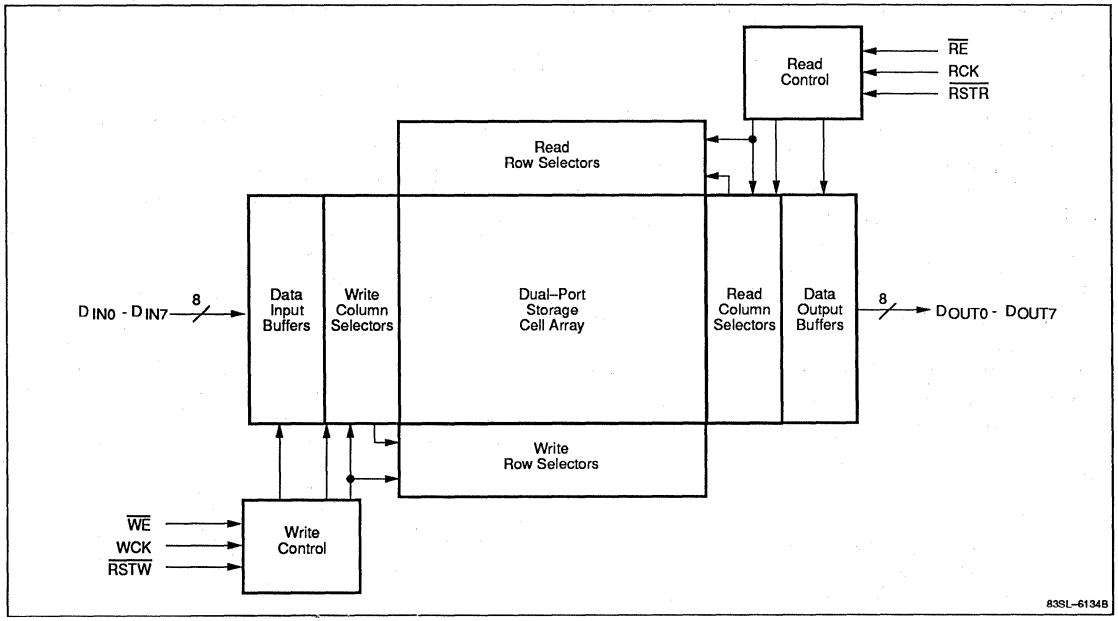
Contact your NEC sales representative for copies of the complete data sheets.

Block Diagram



Comparison of Dual-Port Line Buffers

Features	μPD42101	μPD42102	μPD42505
Organization	910 x 8	1135 x 8	5048 x 8
Speeds (ns)	34 or 69	28 or 56	50 or 75
$4f_{SC}$ digital television system	NTSC	PAL	
Maximum digital delay (clocks)	910	1135	5048

OPERATION

Reset Cycle

NEC's line buffers require the initialization of internal circuits using the $\overline{RSTW}/\overline{RSTR}$ reset signals before starting operation as a time axis converter or a digital delay line.

A reset cycle can be executed at anytime and does not depend on the state of $\overline{RE}$ or $\overline{WE}$. However, $\overline{RSTW}$ and $\overline{RSTR}$ must satisfy required setup and hold times as measured from the rising edges of WCK and RCK.

Write/Read Cycle

Write and read cycles are synchronized to their respective WCK/RCK inputs and executed individually when WCK or RCK is high and $\overline{WE}$ or $\overline{RE}$ is low. Write data must satisfy the setup and hold times as specified from the rising edge of WCK. New data written to a particular address is available for reading after 1/2 write cycle + 500 ns (maximum).

The access time of the read cycle is measured from the rising edge of RCK, either by t_{ACR} for an access during the first cycle directly after a reset begins, or by t_{AC} for an access under other conditions. Stored data is read nondestructively; data can be repeatedly read within a prescribed time of 5 ms maximum (20 ms maximum for H versions).

Time Axis Conversion

In order to use these line buffers as time axis converters, write and read cycles must be controlled independently. First, write/read ports are initialized separately using the reset signals. Then, write cycles are executed in synchronization with WCK and write data is stored sequentially from address 0 of the device. Afterward, when a read cycle is executed in synchronization with RCK, stored data can be read sequentially from address 0.

Since write and read cycles can be executed independently, data loaded at one arbitrary drive frequency can be read at another arbitrary drive frequency. In this sense, the line buffer functions as a time axis converter.

Digital Delay Line

NEC's line buffers can also easily be used as digital delay lines. After initializing the internal circuits using simultaneous $\overline{RSTW}/\overline{RSTR}$ signals, write/read cycles are executed simultaneously by supplying the same pulse to the write clock (WCK) and read clock (RCK). The write data is always read after the full line delay if neither write nor read operation has been inhibited. This is the essential delay line function.

If either $\overline{WE}$ or $\overline{RE}$ is set at a nonselected (high) level for several cycles while the other is maintained at a selected (low) level, the delay line length can differ from the line length.

For example, if only $\overline{WE}$ is set to a high level (write disable) for a small number of cycles, read cycles are executed continuously and the delay line length is large. Alternatively, if only $\overline{RE}$ is set to a high level (read disable) for a small number of cycles, write cycles are executed continuously and the delay line length is small. Note that the minimum delay line length is 10 bits (for maximum frequency operation) and the maximum is the length of the line buffer.

A data delay of less than the line length can also be obtained by applying the $\overline{RSTW}$ and $\overline{RSTR}$ signals at different times. For example, data is loaded for "m" cycles after $\overline{RSTW}$ and then this data is read after supplying $\overline{RSTR}$. In the case, since write data can be read from the beginning after a delay of "m" cycles, the device can be used as an "m-bit" digital delay line.

The $\overline{RSTW}/\overline{RSTR}$ reset signals can also be simultaneously loaded at every 1H (horizontal line) period. In this case, write data loaded in the previous line cycle is read out from the beginning as read data after the reset. Therefore, a delay line length can be obtained according to the length of the reset signals supplied.

NEC

NEC Electronics Inc.

μPD42270
NTSC Field Buffer

Preliminary Information

Description

The μPD42270 is a field buffer designed for NTSC TV applications and for other applications where serial data is needed. Equipped with four planes of 263-line by 910-bit storage, the μPD42270 can execute serial write and read cycles on any of the 263 lines. Within a line, four planes of 910 bits each may be written or read at the NTSC sampling rate of $4f_{SC}$.

Each of the four planes in the μPD42270 is equipped with two ports, one each for the write and read data registers. Each of the registers is split into two 455-bit segments, but functions as if it were organized as one scan line of 910 bits. Independent control of write and read operation makes it possible for the device to operate synchronously or asynchronously at a clock frequency of 14.3 MHz or higher.

The synchronous option simplifies interframe luminance (Y) and chrominance (C) separation and interfield noise reduction and makes it easy to obtain a one-field delay line for digital TV and VCR applications requiring NTSC $4f_{SC}$ sampling. To obtain a very long delay, field length can be configured from 260 to 263 lines and line length of the last line from 896 to 910 bits.

The asynchronous option is useful in applications such as frame synchronization and time base correction, where line jump, line hold, line reset and pointer clear functions are required to support special effects in TV field processing.

Regular refreshing of the device's dynamic storage cells is performed automatically by an internal arbitration circuit. All inputs and outputs, including clocks, are TTL-compatible. The μPD42270 is packaged in a 400-mil, 28-pin plastic DIP and is guaranteed for operation at −20 to +70°C.

Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42270C-60	40 ns	60 ns	28-pin plastic DIP

Features

- ☐ Three functional blocks
  - — Four 263-line x 910-bit storage planes
  - — 910-bit write register for each plane
  - — 910-bit read register for each plane
- ☐ Two data ports: serial write and serial read
- ☐ Asynchronous operation
  - — Dual-port accessibility
  - — Carry-out capability to indicate position of scan line
  - — Line jump, line hold, line reset, and pointer clear functions
- ☐ Synchronous operation
  - — Variable field length: 260 to 263 lines
  - — Variable last line length: 896 to 910 bits
- ☐ Automatic refreshing
- ☐ CMOS technology
- ☐ Fully TTL-compatible inputs, outputs, and clocks
- ☐ Three-state outputs
- ☐ Single +5-volt ±10% power supply
- ☐ On-chip substrate bias generator
- ☐ Standard 400-mil, 28-pin plastic DIP packaging

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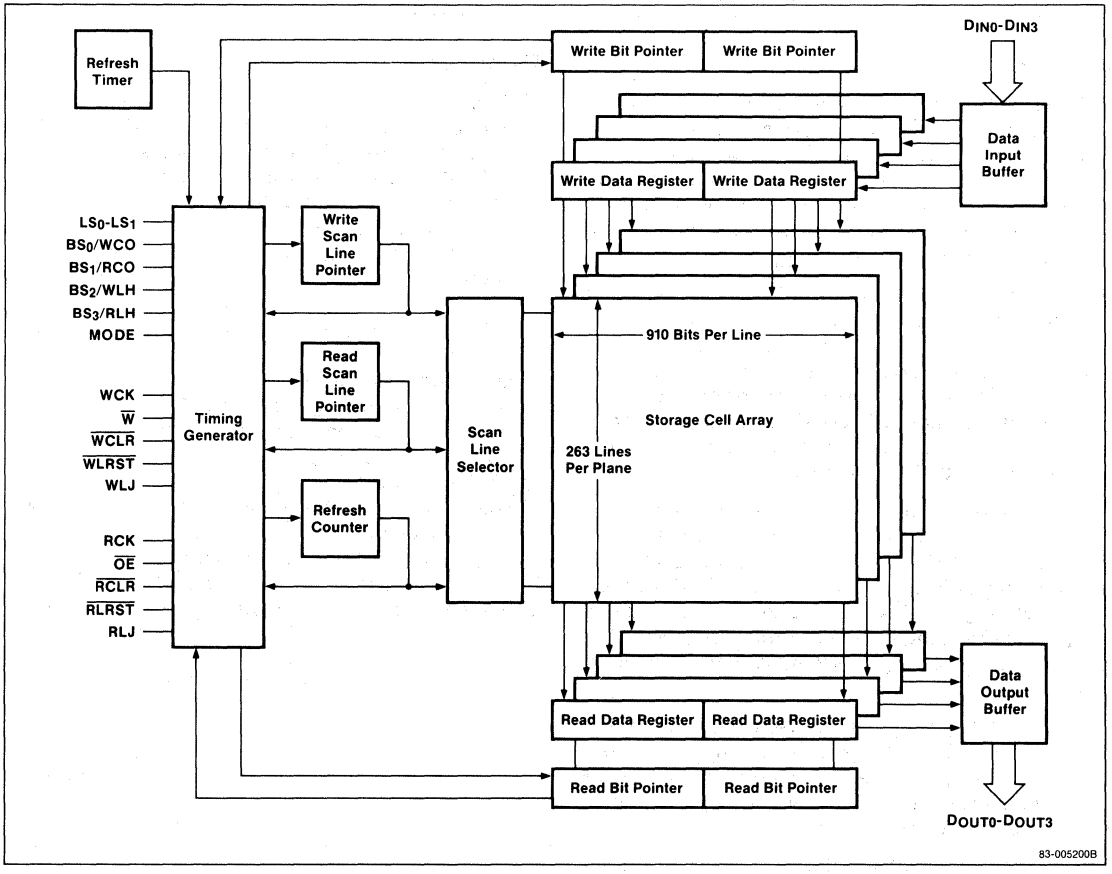
Contact your NEC sales representative for a copy of the complete data sheet.

Block Diagram



NEC

NEC Electronics Inc.

μPD43501
1,024-Channel
Time-Division Switch

Preliminary Information

Description

The μPD43501 is a time-switch device designed for use in a high-performance digital communications network. Features include a time-switch function by which up to 1,024 channels can be exchanged using a 16-bit data width, and a tone output function by which an 8-bit tone signal can be output to an arbitrary channel.

Two planes of 1-kword by 8-bit storage area and one plane of 1-kword by 10-bit control storage area for the time-switch function enable the μPD43501 to realize switching modes in which arbitrary 1,024 or 512 input channels can be connected to arbitrary 1,024 or 512 output channels. The configuration of the tone signal output section, one plane of 64-word by 8-bit tone storage area and one plane of 1-kword by 8-bit tone control storage area, allows the device to output up to 64 different tone signals to an arbitrary output channel as 8-bit voice/tone data.

Ordering Information

Part Number	Data Transfer Rate (max)	Package
μPD43501R	8.192 Mbps	132-pin ceramic pin grid array (PGA)

Features

- ☐ Separate switch storage and control storage to allow construction with one VLSI device of a non-blocking switching network having a maximum capacity of 1,024 channels
- ☐ Selectable operation
  - — 1,024 by 1,024 serial input and output
  - — 1,024 by 1,024 parallel input and output
    - • 16.384 MHz operating frequency
    - • 8.192 Mbps data transfer rate
  - — 512 by 512 parallel input and output
    - • 8.192 MHz operating frequency
    - • 4.096 Mbps data transfer rate
- ☐ Switching flexibility
  - — 8- or 16-bit data width
  - — n by 64 kbps connection
- ☐ Tone signal output function
- ☐ 8 by 8 space switch for an 8.192 Mbps, 128-channel multiplexed line
- ☐ CPU interfaces for the control storage and tone control storage
- ☐ Low power consumption: 1000 mW (typ)
- ☐ TTL-compatible inputs and outputs
- ☐ 132-pin ceramic pin grid array packaging

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Switching Functions

Mode 0

In this mode, the μPD43501 inputs eight 128-channel multiplexed lines from ports SI_{00} through SI_{07} (or from CI_{00} through CI_{07}) and outputs eight 128-channel multiplexed lines to ports SO_{00} through SO_{07} (or CO_{00} through CO_{07}). Refer to figure 1 for a functional pin diagram.

Serial input data from the input ports first is converted to parallel data by the serial-to-parallel converters in the receive section, and then multiplexed and sent to the input section of the switch storage area. Since the write address counter is synchronized with input data, the write address of the switch storage area corresponds to the time slot number of the input signal. Writing multiplexed data to the switch address specified by the write address counter causes input data in the time slot corresponding to the switch address always to be stored at that address (figure 2).

Conversely, a control storage address corresponds to an output-side time slot number, and the data in control storage indicates the switch storage address, i.e., the input-side time slot number is stored at the control storage address corresponding to the output-side time slot to which the input-side is transferred.

The address signal is sent from the read address counter to control storage in synchronization with each output-side time slot. Data read out by this operation is then sent to the switch storage area as the address signal, and the data in the specified address (input-side time slot) is then read out on the output side and switched. Switched data is sent to the parallel-to-serial converters in the transmission section, where it is converted to serial data and then output to the appropriate output ports.

With this switching function, the data in an arbitrary time slot on the input side can be output as data in an arbitrary time slot on the output side. Furthermore, in addition to the time division switch function, a space switch function enables switching time slots on any of the eight input ports to be output on any of the eight output ports. This means that a nonblocking 8 x 8 space switch for 128-channel multiplexed lines can be realized.

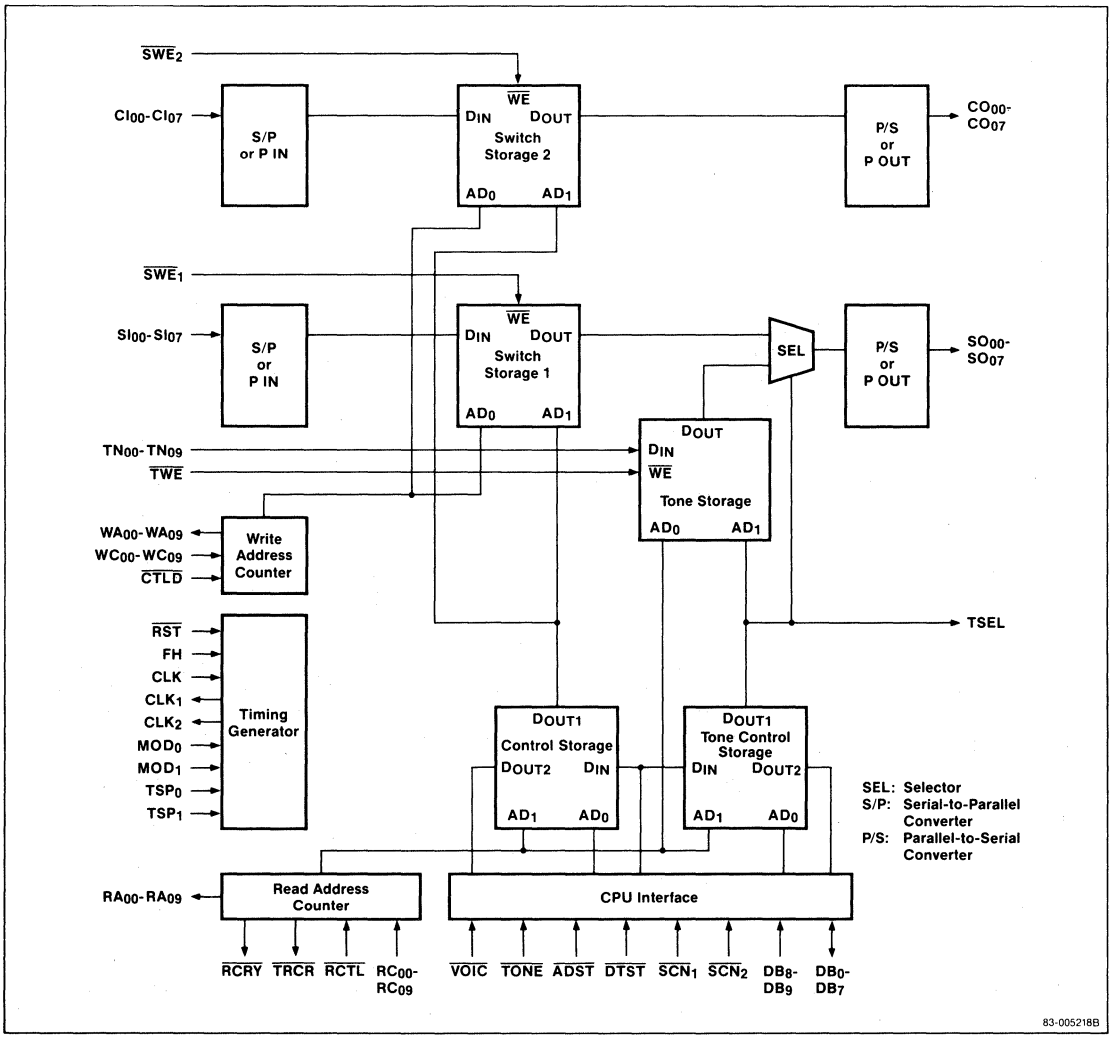
Mode 1

Mode 1 makes it possible for the μPD43501 to input 512-channel multiplexed lines (4.096 Mbps by 8 bits), 8 bits in parallel, and output 512-channel multiplexed lines, 8 bits in parallel. The input signals received on the input ports are sent to the switch storage area in parallel, after which the same switching functions described in Mode 0 are then performed.

Mode 2

In Mode 2, the μPD43501 inputs 1,024-channel multiplexed lines (8.192 Mbps by 8 bits), 8 bits in parallel, and outputs 1,024-channel multiplexed lines, 8 bits in parallel. The input signals received on the input ports are sent to the switch storage area in parallel, after which the same switching functions described in Mode 0 are performed.

Block Diagram



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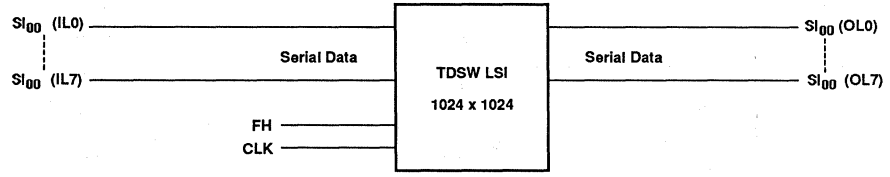
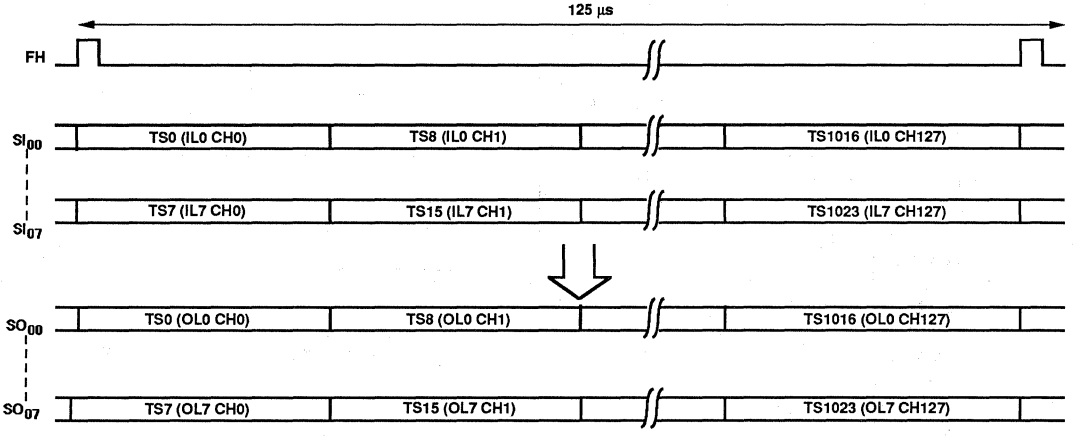
Time Slot Versus Frame Configuration

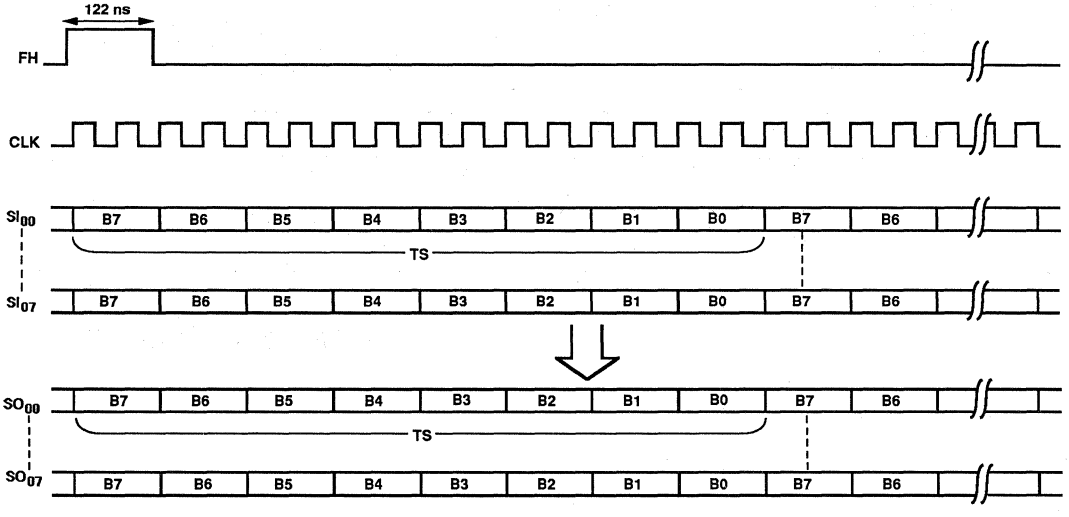
Mode 0



Frame Configuration



Time Slot Configuration



Notes:
[1] IL = input line
[2] OL = output line
[3] TS = time slot
[4] CH = channel

831H-5215B

PACKAGE DRAWINGS

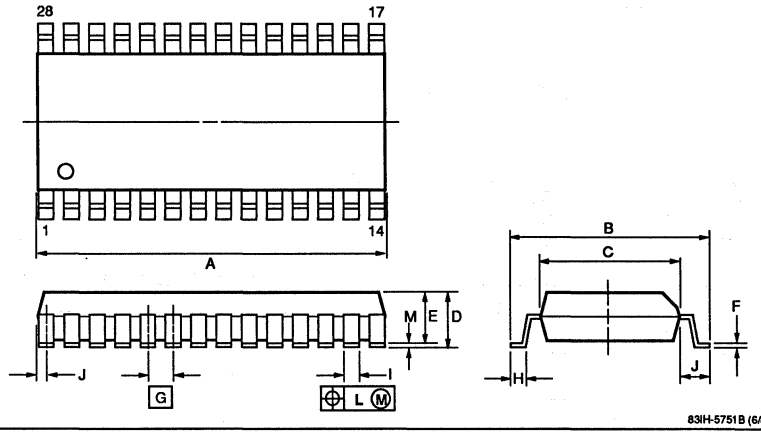
Section 9
Package Drawings

Package/Device Cross-Reference

Package	Device, μPD
28-Pin Plastic SOP (375 mil)	71065G
30-Pin Plastic Shrink DIP (400 mil)	71066CT
40-Pin Plastic DIP (600 mil)	765AC2 765B 7201AC 72001C 72001C-11 72020C-8 72061C 72065C 72065BC
40-Pin Ceramic DIP With Side-Brazed Leads (600 mil)	7201AD 7220AD 7220AD-1 7220AD-2 7261AD 7261BD-18 7261BD-23
40-Pin Cerdip (600 mil)	7262D12 7262D18
44-Pin PLCC	72065L 72065BL
48-Pin Plastic DIP (600 mil)	72067C
52-Pin Plastic Miniflat (3.5-mm leads)	7225G-00 72065G
52-Pin Plastic Miniflat (1.8-mm leads)	72001GC-3B6 72001GC-3B6-11 72020GC-8-3B6 72061GC-3B6 72065GC 72065BGC-3B6 72067GC-3B6
52-Pin PLCC	72001L 72001L-11 72061L 72067L
64-Pin Plastic Miniflat	7227G-12
64-Pin Plastic Shrink DIP (750 mil)	72111CW 72185CW
68-Pin PLCC	72022L 72111L 72185L
74-Pin Plastic Miniflat	72111GJ-5BJ
80-Pin Plastic Miniflat (2.35-mm leads)	7228G-12 7228AG-12
80-Pin Plastic Miniflat (1.8-mm leads)	72022GF-3B9 72068GF-3B9
84-Pin PLCC	72068L 72069L 72120L 72123L
94-Pin Plastic Miniflat	72120J-5BG 72123GJ-5BG
100-Pin Plastic Miniflat	72069GF-3BA
132-Pin Ceramic PGA	72123R

28-Pin Plastic SOP (375 mil)

Item	Millimeters	Inches
A	18.07 max	.711 max
B	10.3 ±0.3	.406 ±.012
C	7.2	.283
D	2.9 max	.114 max
E	2.50	.098
F	1.6	.063
G	1.27 [TP]	.050 [TP]
H	0.8 ±0.2	.031 ±.008
I	0.78 max	.031 max
J	$0.40^{+0.10}_{-0.05}$	$.016^{+.004}_{-.002}$
K	$0.15^{+0.10}_{-0.05}$	$.006^{+.004}_{-.002}$
L	0.12	.005
M	0.1 ±0.1	.004 ±.004

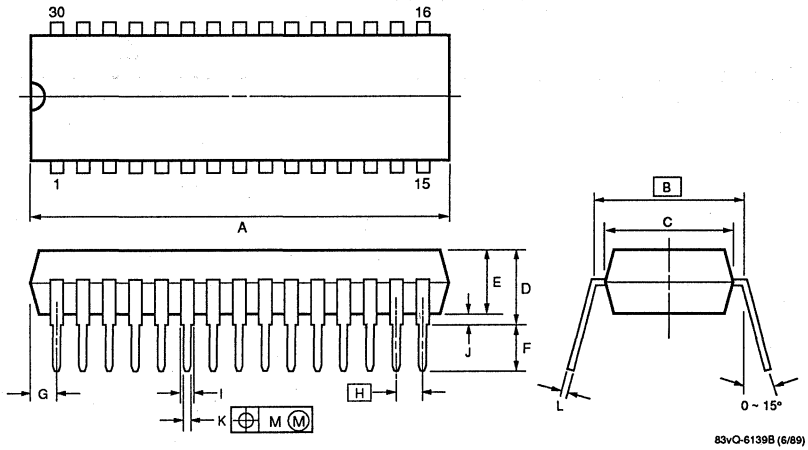


P28GM-50-375R

83IH-5751B (6/89)

30-Pin Plastic Shrink DIP (400 mil)

Item	Millimeters	Inches
A	28.46 max	1.120 max
B	10.16 [TP]	.400 [TP]
C	8.6	.339
D	5.08 max	.200 max
E	4.31 max	.170 max
F	3.2 ±0.30	.126 ±.012
G	1.78 max	.070 max
H	1.778 [TP]	.070 [TP]
I	0.85 min	.033 min
J	0.51 min	.020 min
K	0.50 ±0.10	0.20 ±.004
L	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.002}$
M	0.17	.007



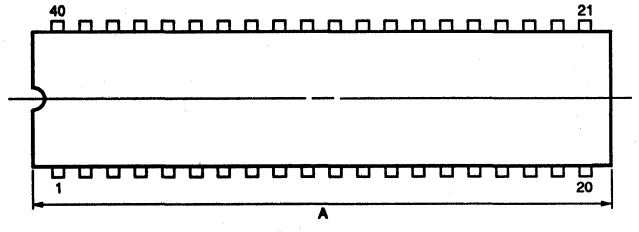
S30C-70-400B

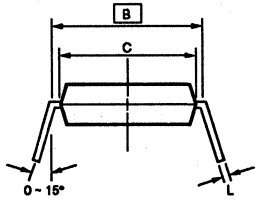
83vO-6139B (6/89)

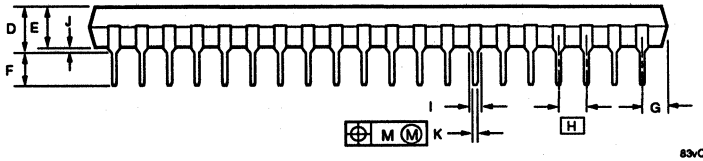
9

40-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	15.24 [TP]	.600 [TP]
C	13.2	.520
D	5.72 max	.225 max
E	4.31 max	.170 max
F	3.6 ±0.3	.142 ±.012
G	2.54 max	.100 max
H	2.54 [TP]	.100 [TP]
I	1.2 min	.047 min
J	0.51 min	.020 min
K	0.50 ±0.10	.020 ±.004
L	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.002}$
M	0.25	.010







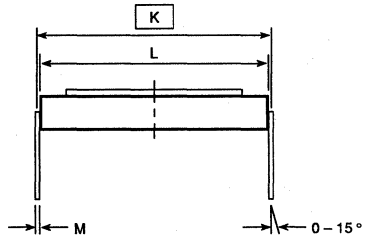
P40C-100-600A

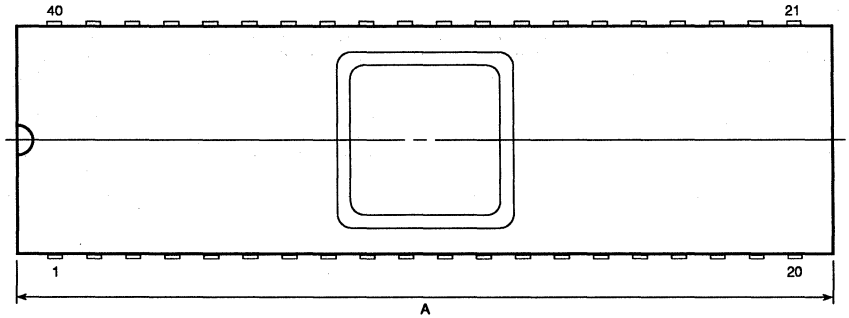
83vQ-5140B (6/89)

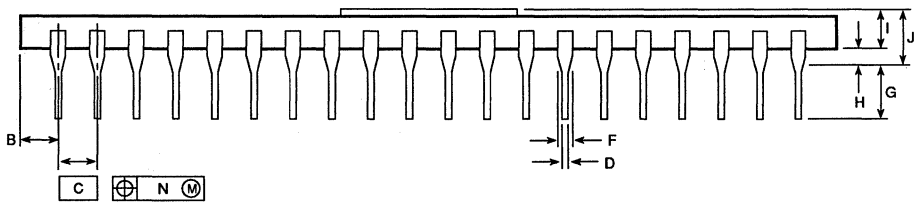
40-Pin Ceramic DIP With Side-Brazed Leads (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.46 ± 0.05	.018 ± .002
F	0.92 min	.036 min
G	3.5 ± 0.3	.138 ± .012
H	1.0 min	.039 min
I	2.64	.104
J	4.57 max	.180 max
K*	15.24 (TP)	.600 (TP)
L	14.93	.588
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.







P40D-100-600A

49NR-526B (5/89)

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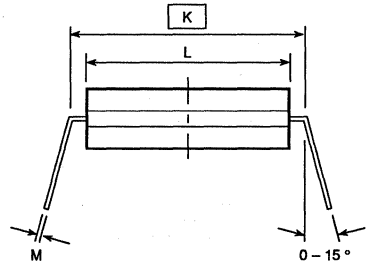
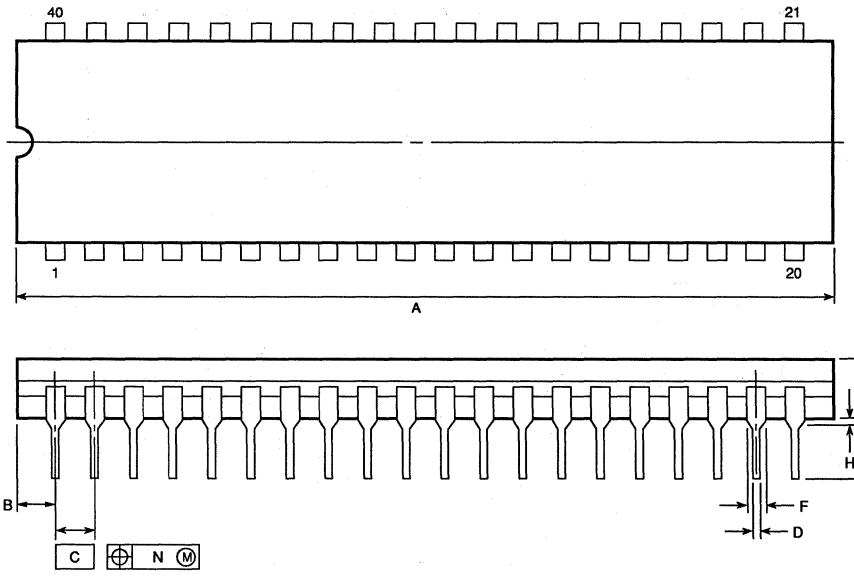
NEC

40-Pin Cerdip (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ±0.3	.138 ±.012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K*	15.24 (TP)	.600 (TP)
L	13.21	.520
M	0.25 ±0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.



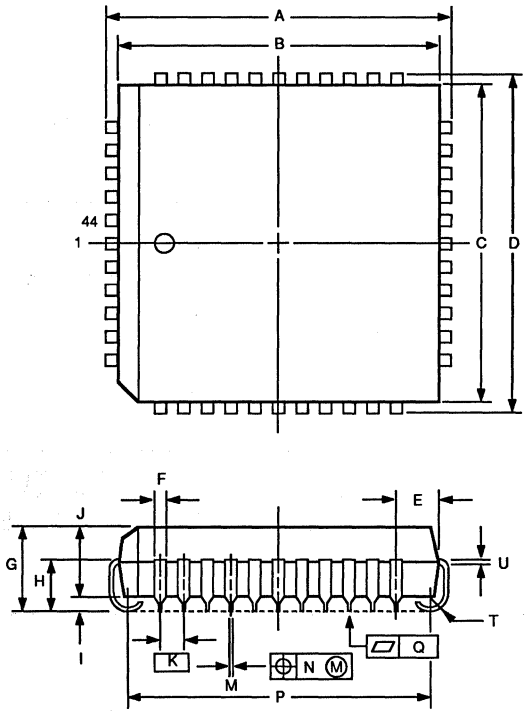


P40DH-100-600A

49NR-530B (6/89)

44-Pin PLCC

Item	Millimeters	Inches
A	17.5 ±0.2	.689 ±.008
B	16.58	.653
C	16.58	.653
D	17.5 ±0.2	.689 ±.008
E	1.94 ±0.15	.076 ±.006
F	0.6	.024
G	4.4 ±0.2	.173 ±.008
H	2.8 ±0.2	.110 ±.008
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 ±.004
N	0.12	.005
P	15.50 ±0.20	.610 ±.008
Q	0.15	.006
T	0.8 radius	.031 radius
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

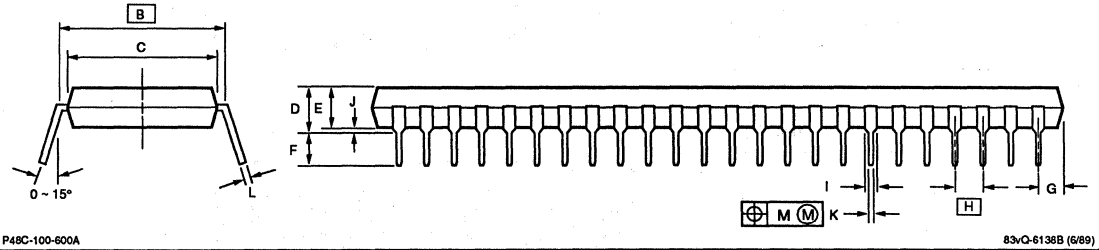


P44L-50A1

6/89 83YL-5804B

48-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	63.50 max	2.500 max
B	15.24 [TP]	.600 [TP]
C	13.8	.543
D	5.72 max	.225 max
E	4.31 max	.170 max
F	3.6 ±0.3	.142 ±.012
G	2.54 max	.100 max
H	2.54 [TP]	.100 [TP]
I	1.1 min	.043 min
J	0.51 min	.020 min
K	0.50 ±0.10	.020 ±.004
L	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.002}$
M	0.25	.010

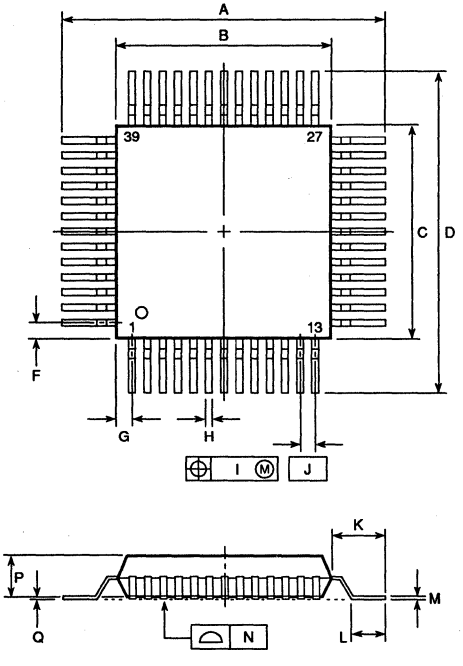


P48C-100-600A

83vQ-6138B (6/89)

52-Pin Plastic Miniflat (3.5-mm leads)

Item	Millimeters	Inches
A	21.0 ±0.4	.827 ±.016
B	14.0 ±0.2	.551 $^{+.009}_{-.008}$
C	14.0 ±0.2	.551 $^{+.009}_{-.008}$
D	21.0 ±0.4	.827 ±.016
F	1.0	.039
G	1.0	.039
H	0.40 ±0.10	.016 $^{+.004}_{-.005}$
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	3.5 ±0.2	.138 $^{+.008}_{-.009}$
L	2.2 ±0.2	.087 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.15	.006
P	2.6 $^{+0.2}_{-0.1}$	.102 $^{+.009}_{-.004}$
Q	0.1 ±0.1	.004 ±.004



P52G-100-00

49NR-536B (6/89)

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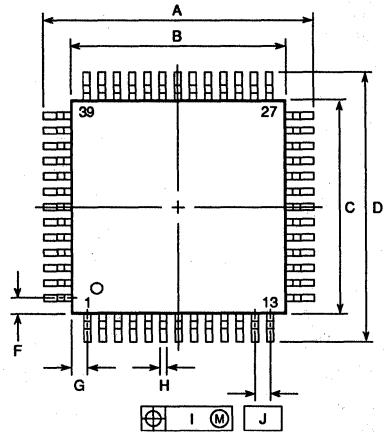
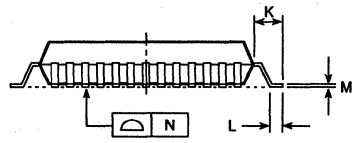
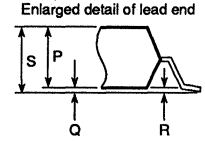
52-Pin Plastic Miniflat (1.8-mm leads)

Item	Millimeters	Inches
A	17.6 ±0.4	.693 ±.016
B	14.0 ±0.2	.551 $^{+.009}_{-.008}$
C	14.0 ±0.2	.551 $^{+.009}_{-.008}$
D	17.6 ±0.4	.693 ±.016
F	1.0	.039
G	1.0	.039
H	0.40 ±0.10	.016 $^{+.004}_{-.005}$
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	1.8 ±0.2	.071 $^{+.008}_{-.009}$
L	0.8 ±0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.15	.006
P	2.7	.106
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	3.0 max	.119 max





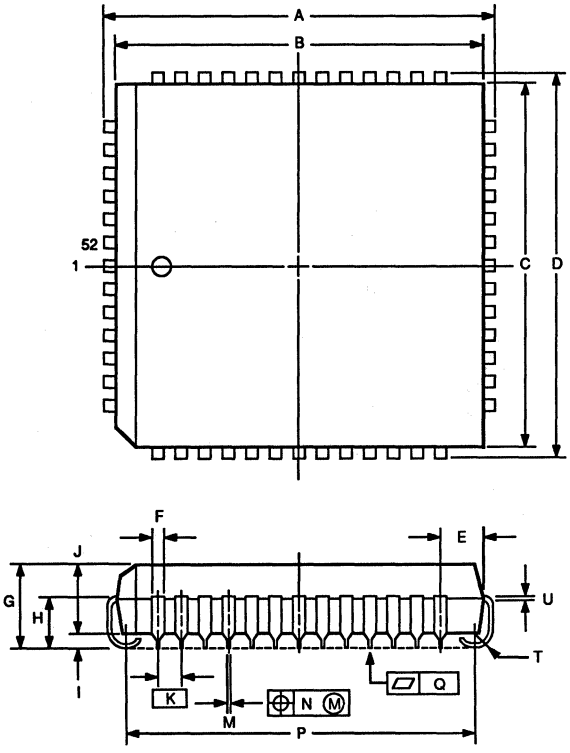


P52GC-100-3B6

49NR-493B (5/89)

52-Pin PLCC

Item	Millimeters	Inches
A	20.1 ±0.2	.791 ±.008
B	19.12	.753
C	19.12	.753
D	20.1 ±0.2	.791 ±.008
E	1.94 ±0.15	.076 ±.006
F	0.6	.024
G	4.4 ±0.2	.173 ±.008
H	2.8 ±0.2	.110 ±.008
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 ±.004
N	0.12	.005
P	18.04 ±0.20	.710 ±.008
Q	0.15	.006
T	0.8 radius	.031 radius
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$



P52L-50A1

83YL-5805B

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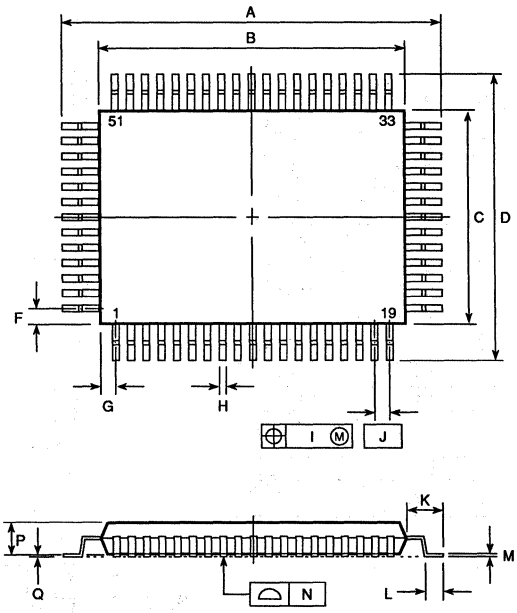
64-Pin Plastic Miniflat

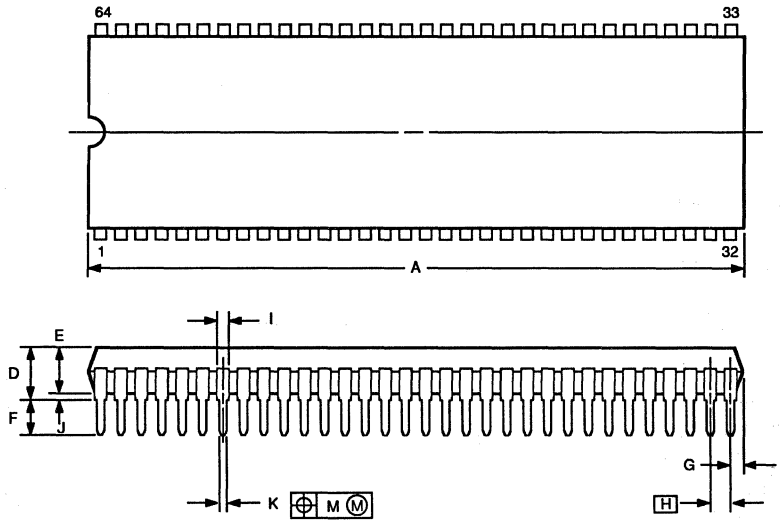
Item	Millimeters	Inches
A	24.7 ±0.4	.972 $^{+.017}_{-.016}$
B	20.0 ±0.2	.795 $^{+.009}_{-.008}$
C	14.0 ±0.2	.551 $^{+.009}_{-.008}$
D	18.7 ±0.4	.736 ±.016
F	1.0	.039
G	1.0	.039
H	0.40 ±0.10	.016 $^{+.004}_{-.005}$
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	2.35 ±0.2	.093 $^{+.008}_{-.009}$
L	1.2 ±0.2	.047 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.15	.006
P	2.05 $^{+0.2}_{-0.1}$	.081 $^{+.008}_{-.005}$
Q	0.1 ±0.1	.004 ±.004



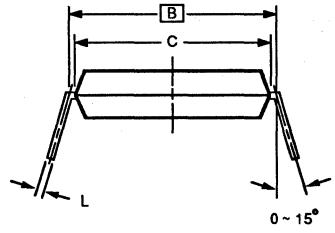
P64G-100-12_1B

49NR-543B (6/89)

64-Pin Plastic Shrink DIP (750 mil)



Item	Millimeters	Inches
A	58.68 max	2.310 max
B	19.05 (TP)	.750 (TP)
C	17.0	.669
D	5.08 max	.200 max
E	4.31 max	.170 max
F	3.2 ±0.3	.126 ±.012
G	1.78 max	.070 max
H	1.778 (TP)	.070 (TP)
I	0.9 min	.035 min
J	0.51 min	.020 min
K	0.50 ±0.10	.020 ±.004
L	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.002}$
M	0.17	.007



P64C-70-750A, C

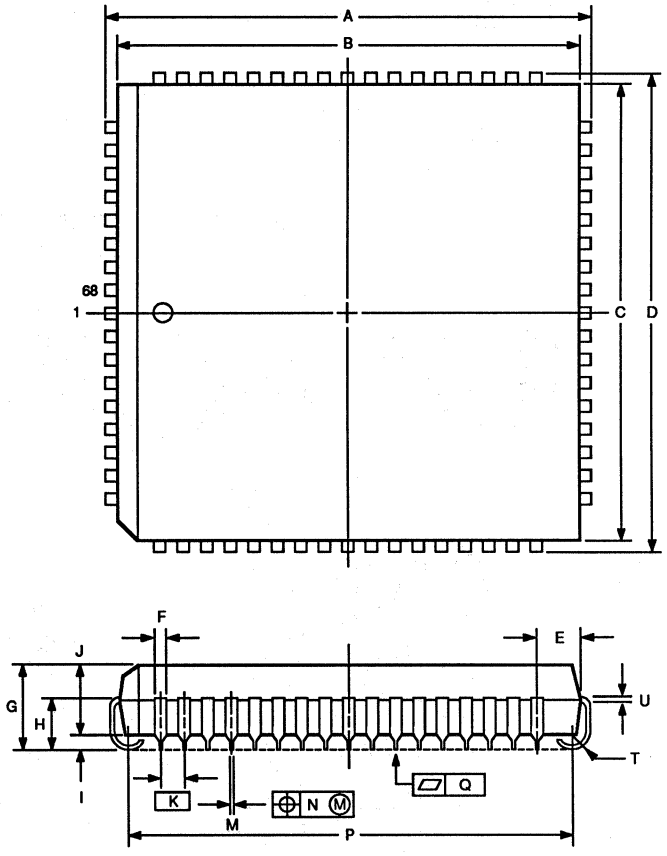
5/89

83YL-5560B

9

68-Pin PLCC

Item	Millimeters	Inches
A	25.2 ±0.2	.992 ±.008
B	24.20	.953
C	24.20	.953
D	25.2 ±0.2	.992 ±.008
E	1.94 ±0.15	$.076^{+.007}_{-.006}$
F	0.6	.024
G	4.4 ±0.2	$.173^{+.009}_{-.008}$
H	2.8 ±0.2	$.110^{+.009}_{-.008}$
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	$.016^{+.004}_{-.005}$
N	0.12	.005
P	23.12 ±0.20	$.910^{+.009}_{-.008}$
Q	0.15	.006
T	0.8 radius	.031 radius
U	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$

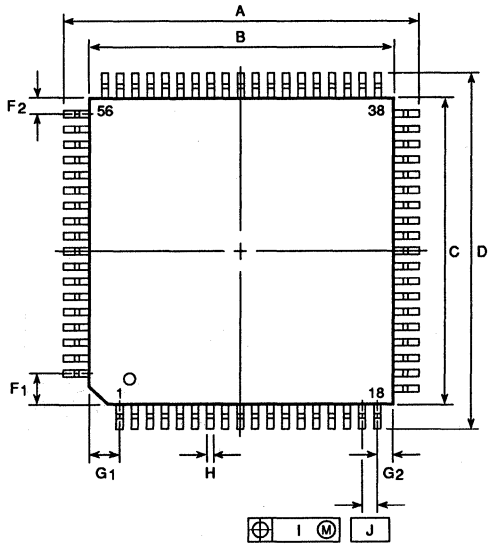


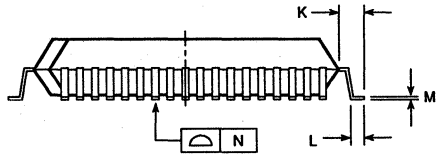
SSD-20615-1 (10-13-86)
P68L-50A1

5/89
83YL-5561B

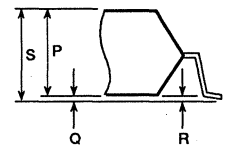
74-Pin Plastic Miniflat

Item	Millimeters	Inches
A	23.2 ±0.4	.913 $^{+.017}_{-.016}$
B	20.0 ±0.2	.787 $^{+.009}_{-.008}$
C	20.0 ±0.2	.787 $^{+.009}_{-.008}$
D	23.2 ±0.4	.913 $^{+.017}_{-.016}$
F_1	2.0	.079
F_2	1.0	.039
G_1	2.0	.079
G_2	1.0	.039
H	0.40 ±0.10	.016 $^{+.004}_{-.005}$
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	1.6 ±0.2	.063 ±.002
L	0.8 ±0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.005}$
N	0.15	.006
P	3.7	.146
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	4.0 max	.158 max





Enlarged detail of lead end



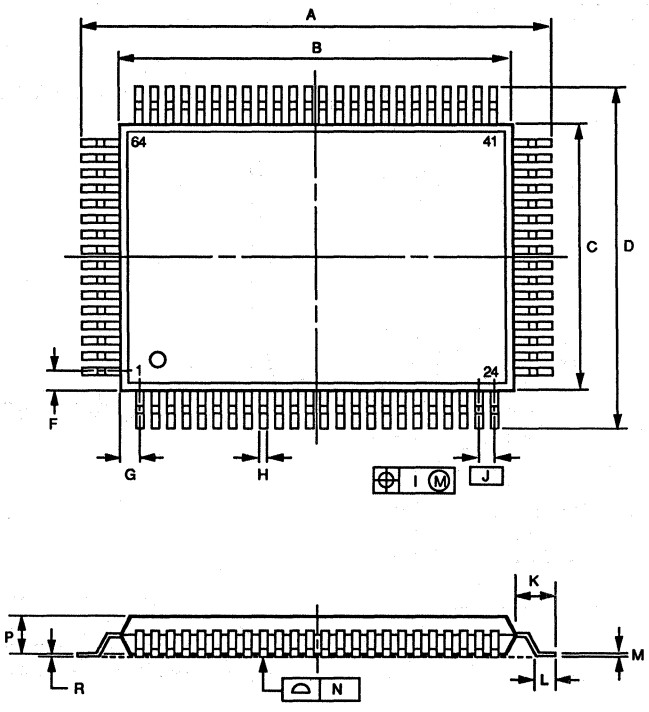
S74GJ-100-5BJ

49NR-347B
(6/89)

9

80-Pin Plastic Miniflat (2.35-mm leads)

Item	Millimeters	Inches
A	24.7 ±0.4	.972 ±.016
B	20.0 ±0.2	.787 $^{+.009}_{-.008}$
C	14.0 ±0.2	.551 $^{+.009}_{-.008}$
D	18.7 ±0.4	.736 ±.016
F	1.0	.039
G	0.8	.031
H	0.35 ±0.10	.014 $^{+.004}_{-.005}$
I	0.15	.006
J	0.8 (TP)	.031 (TP)
K	2.35 ±0.2	.093 $^{+.009}_{-.008}$
L	1.2 ±0.2	.047 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
N	0.15	.006
P	2.05 $^{+0.2}_{-0.1}$	.081 $^{+.008}_{-.004}$
R	0.1 ±0.1	.004 ±.004

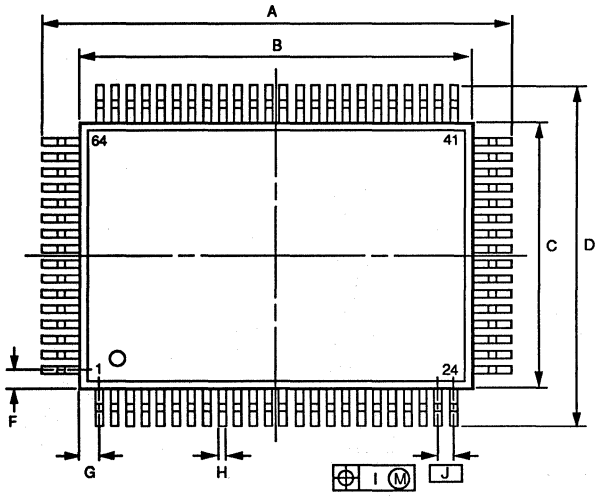


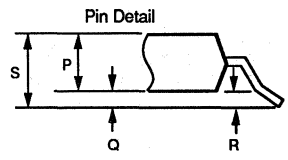
P80G-80-12

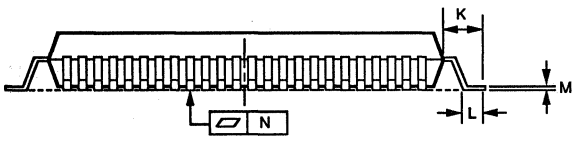
83SL-6222B (6/89)

80-Pin Plastic Miniflat (1.8-mm leads)

Item	Millimeters	Inches
A	23.6 ±0.4	.929 ±.016
B	20.0 ±0.2	.787 $^{+.009}_{-.008}$
C	14.0 ±0.2	.551 $^{+.009}_{-.008}$
D	17.6 ±0.4	.693 ±.016
F	1.0	.039
G	0.8	.031
H	0.35 ±0.10	.014 $^{+.004}_{-.005}$
I	0.15	.006
J	0.8 (TP)	.031 (TP)
K	1.8 ±0.2	.071 $^{+.009}_{-.008}$
L	0.8 ±0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
N	0.15	.006
P	2.7	.106
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	3.0 max	.118 max







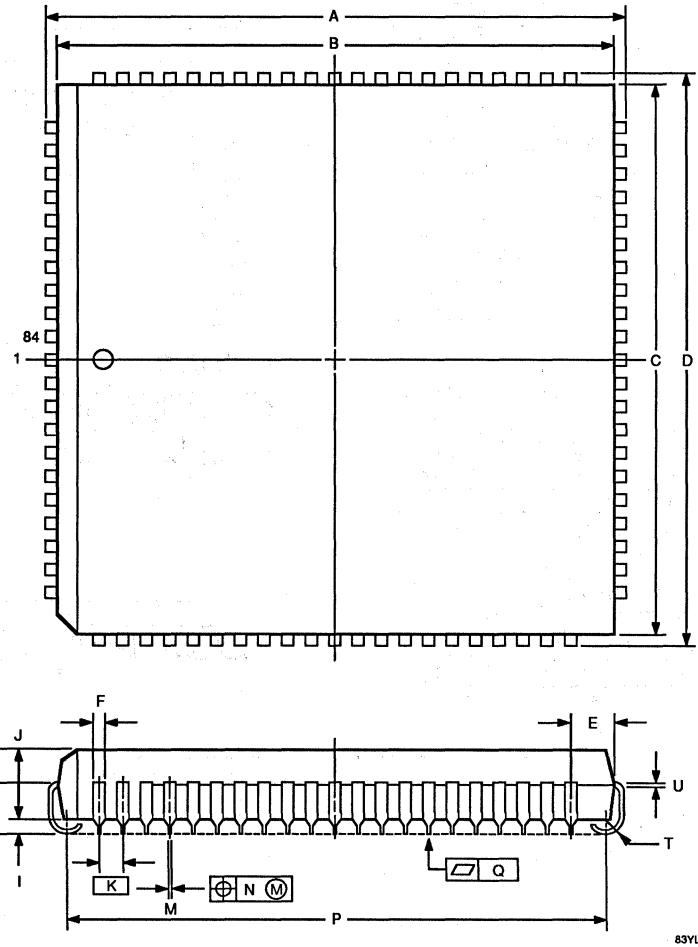
P80GF-80-3B9

83IH-5543B (6/89)

9

84-Pin PLCC

Item	Millimeters	Inches
A	30.2 ±0.2	1.189 ±.008
B	29.28	1.153
C	29.28	1.153
D	30.2 ±0.2	1.189 ±.008
E	1.94 ±0.15	.076 ±.006
F	0.6	.024
G	4.4 ±0.2	.173 ±.008
H	2.8 ±0.2	.110 ±.008
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 ±.004
N	0.12	.005
P	28.20 ±0.20	1.110 ±.008
Q	0.15	.006
T	0.8 radius	.031 radius
U	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$

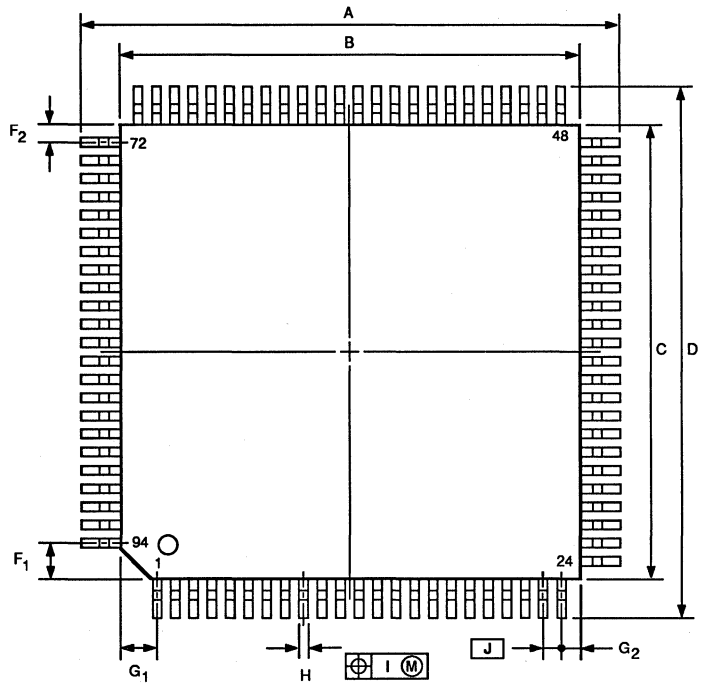


P84L-50A3

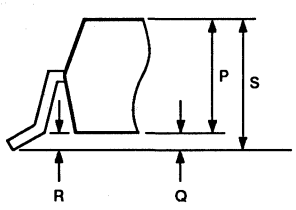
83YL-5806B
(6/89)

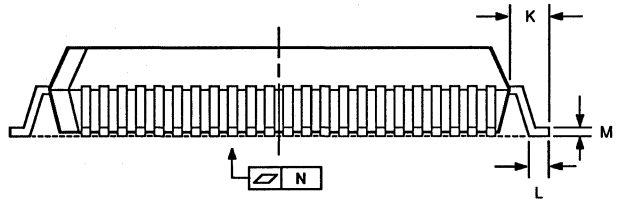
94-Pin Plastic Miniflat

Item	Millimeters	Inches
A	23.2 ±0.4	.913 +.017 −.016
B	20.0 ±0.2	.787 +.009 −.008
C	20.0 ±0.2	.787 +.009 −.008
D	23.2 ±0.4	.913 +.017 −.016
F_1	1.6	.063
F_2	0.8	.031
G_1	1.6	.063
G_2	0.8	.031
H	0.35 ±0.10	.014 +.004 −.005
I	0.15	.006
J	0.8 (TP)	.031 (TP)
K	1.6 ±0.2	.063 ±.008
L	0.8 ±0.2	.031 +.009 −.008
M	0.15 +0.10 −0.05	.006 +.004 −.003
N	0.15	.006
P	3.7	.146
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	4.0 max	.158 max



Detail of lead end





S94GJ-80-5BG

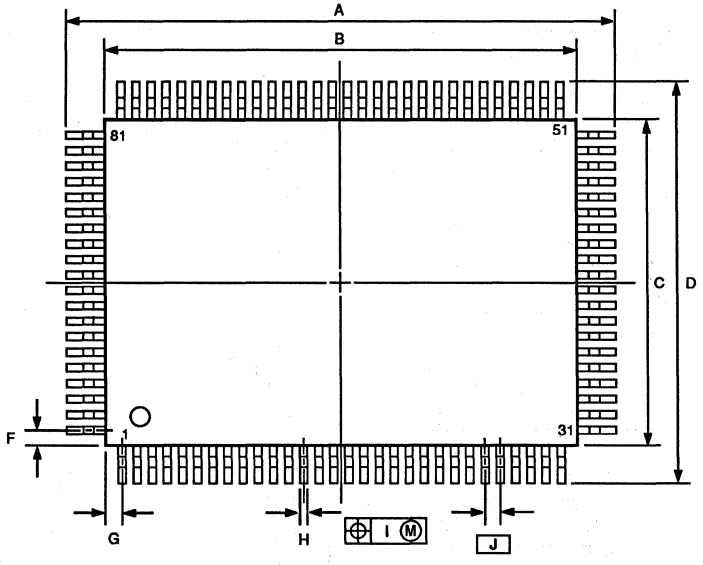
6/89
83YL-5810B

9

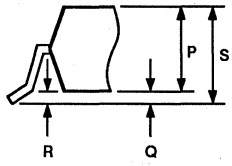
NEC

100-Pin Plastic Miniflat

Item	Millimeters	Inches
A	23.6 ±0.4	.929 ±.016
B	20.0 ±0.2	.787 $^{+.009}_{-.008}$
C	14.0 ±0.2	.551 $^{+.009}_{-.008}$
D	17.6 ±0.4	.693 ±.016
F	0.8	.039
G	0.6	.031
H	0.30 ±0.10	.014 $^{+.004}_{-.005}$
I	0.15	.006
J	0.65 (TP)	.031 (TP)
K	1.8 ±0.2	.071 $^{+.009}_{-.008}$
L	0.8 ±0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
N	0.15	.006
P	2.7	.106
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	3.0 max	.118 max



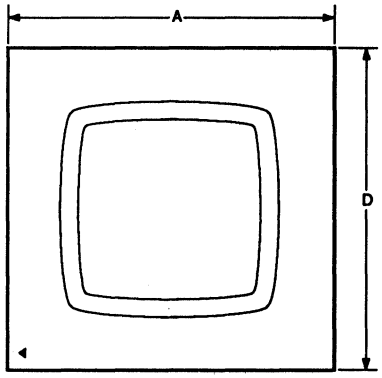
Detail of lead end

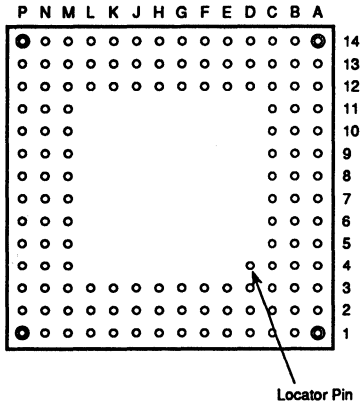


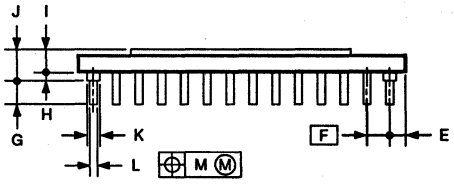
P100GF-65-3BA

6/89 83YL-5811B

132-Pin Ceramic PGA







Item	Millimeters	Inches
A	35.56 ±0.4	$1.400^{+.016}_{-.015}$
D	35.56 ±0.4	$1.400^{+.016}_{-.015}$
E	1.27	.050
F	2.54 (TP)	.100 (TP)
G	2.8 ±0.3	$.110^{+.012}_{-.011}$
H	0.5 min	.019 min
I	2.9	.114
J	4.57 max	.180 max
K	ø1.2 ±0.2	$ø.047^{+.008}_{-.007}$
L	ø0.46 ±0.05	$ø.018^{+.002}_{-.001}$
M	0.5	.020

X132R-100A

6/89
83YL-5617B

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