National Semiconductor
Order No. IMP-16L/924B
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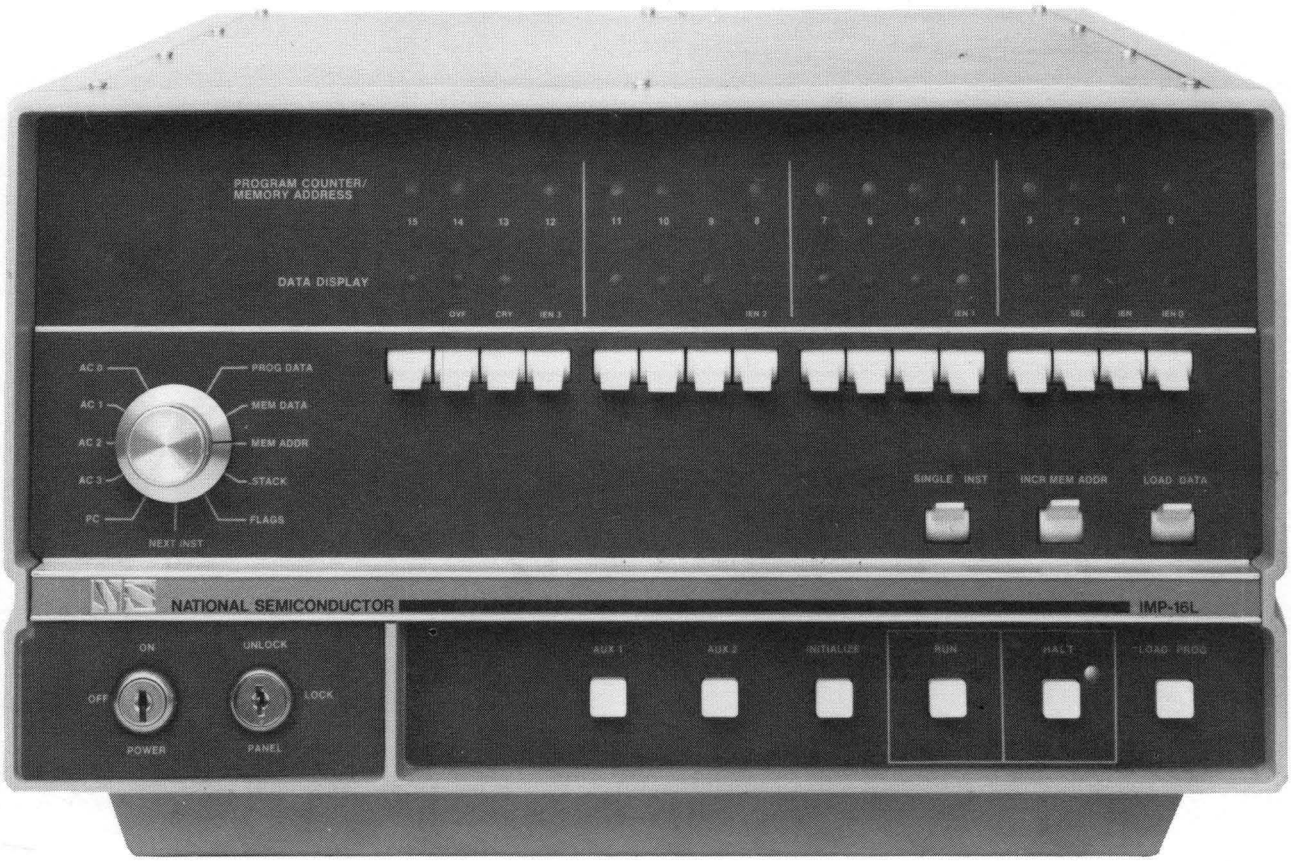
IMP-16L
Product Description



IMP-16L Microcomputer

1.0 INTRODUCTION

The IMP-16L is a general-purpose 16-bit microcomputer designed expressly for the OEM (original equipment manufacturer) user. A high-speed asynchronous bus affords direct memory access by peripheral devices and, along with the modular configuration of the equipment, gives the user maximum flexibility for configuration of his systems. The basic IMP-16L and the options for adding or even deleting certain modules provides an unusually versatile capability for developing a variety of OEM equipment, software, and full-scale processing systems. Both the memory and the microprocessor include LSI circuits that are advanced products of proven semiconductor technology, thus providing lower cost, higher reliability, smaller size, and lower power consumption.

The configuration that is most attractive to a given user depends upon a variety of factors. These factors may change over the life of the system manufacturer's product. An important advantage of the availability of these different configurations of the IMP-16L is the option of changing the configuration in response to changing conditions. For example, the system manufacturer may initially procure the IMP-16L as a stand-alone system in order to expedite software development and to permit rapid assembly of models for field trial. Later, it may be more economical to purchase subassemblies that are packaged in an enclosure customized for the application. When production quantities warrant, the system manufacturer may later decide to purchase at the semiconductor component level. Thus, the manufacturer may optimize both his development and production phases due to the versatility of the IMP-16L design and options.

Both cross and resident assembler programs are available as options to support the preparation of user's application programs. The cross assembler may be used on a large-scale computer system to assemble programs written in the IMP-16 language. Also, the cross assembler has been installed on the nationwide Tymshare computer utility. Another technique available for assembling application programs is the resident assembler program, which can be loaded into the IMP-16L memory and then used to assemble the user's application programs.

A number of IMP-16 loader programs and an IMP-16 debug program are also available to support development of user's application programs.

A programmers control panel is supplied with the IMP-16L to provide access to the CPU registers and memory. It includes an array of data switches, data and address indicators, and function switches. Using the programmers panel, the operator may address, load, and examine memory and CPU registers and control the operation of the microcomputer.

1.1 IMP-16L OPERATIONAL FEATURES

Word Length – 16 bits

Instruction Set – 60 general-purpose instructions (43 in basic set, 17 in expanded set)

Arithmetic – Parallel, binary, fixed point, twos complement

Memory – 4096 16-bit words of semiconductor memory, expandable in increments of 4096 words to a maximum of 65,536 words

Registers (Accumulators) – 4 general-purpose

Pushdown Stack – 16 16-bit words

Addressing Modes – Page size of 256 words. For direct and indirect modes:

- Direct – 256 words
- Relative to Program Counter – 256 words
- Relative to Accumulator 2 or 3* – 256 words
- Indirect – 65,536 words

Typical Instruction-Execution Speeds –

- Register-to-register addition – 4.9 microseconds
- Memory-to-register addition – 8.4 microseconds
- Register input/output – 10.5 microseconds
- Direct Memory Access (DMA) transfer – 1.05 microseconds

Operating Speed – 1.4-microsecond microcycle time

Input/Output and Control –

- Autonomous 16-bit data bus
- 1-MHz DMA transfer rate
- 4 interrupt levels
- Addressing for 256 peripheral devices

Input Power – 105 to 125 VAC at 60 Hz (220 VAC, 50 Hz optional)

Temperature –

- Operating – 0 to 50°C
- Storage – –20 to +70°C

Humidity – Maximum of 90% relative humidity without condensation

Dimensions – 12 inches high, 17 inches wide, and 24 inches long

1.2 APPLICATIONS

Among the numerous applications possible for the IMP-16L are the following examples:

- Peripheral Device Controllers
  - Card Readers
  - "Floppy" Discs
  - Cassette Tape Units
- Process Controllers
  - Machine Tools
  - Process Controls
  - Traffic Controls
- Terminal Systems
- Stand-alone Cash Registers
- Functional Device Testers
- Evaluation System for National Semiconductor's GPC/P System Kit
- Data Communication Systems
- Small Business Machines
- Test System Controllers
- Point-of-Sale Systems

***Indexing gives maximum range of 65,536 words in page sizes of 256 words each.**

1.3 IMP-16L CONFIGURATION

The functional configuration of the major units comprising the basic IMP-16L is shown in the block diagram of figure 1–1. The Central Processing Unit (CPU), Memory, and Peripheral Devices communicate and exchange data with one another by way of the 16-bit asynchronous data bus. Both programmed data transfers and direct memory access (DMA) transfers take place between memory and peripheral devices over the 16-bit asynchronous bus independent of CPU operation. Also, this bus provides a means for IMP-16L multiprocessor configurations to share a common memory. The maximum bus transfer rate is one million 16-bit words per second.

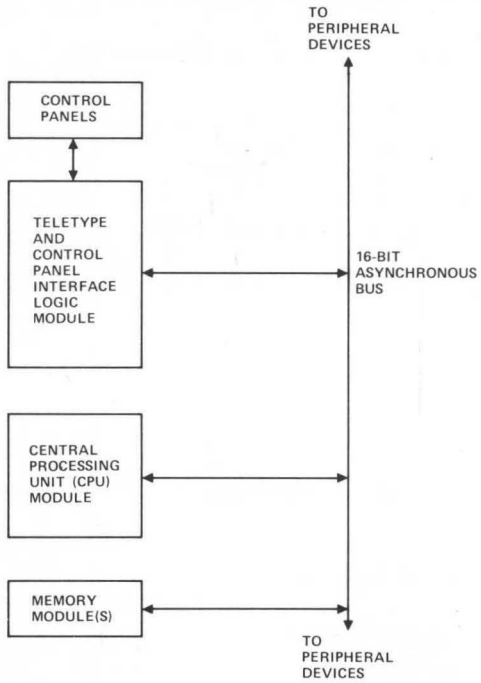


Figure 1–1. Block Diagram of Basic IMP-16L

1.4 PHYSICAL LAYOUT OF IMP-16L CHASSIS

Figure 1–2 shows the physical layout of the IMP-16L chassis.

1.4.1 Card Modules

A variety of functional modules is provided on 8½-by-11-inch printed wiring cards:

- CPU Module – One card comprising the central processing unit, bus controller, and bus interface logic.
- Memory Module – One card comprising 4096 words of read/write memory (RAM), 512 words of read-only memory (ROM) with bus interface, and memory control circuits.
- Interface Modules – Several peripheral device interface modules are available, including Teletypewriter (standard) and card reader (option).

1.4.2 Card Cage

One 12-connector card cage is supplied with the basic IMP-16L microprocessor. It is prewired to hold the CPU, two 4K memory cards, a front panel interface, and a card reader controller. One additional 6-connector card cage may be installed for expansion. If still more expansion is required, the power supplies may be removed and remotely installed, thus providing space for an additional pair of 6-connector card cages.

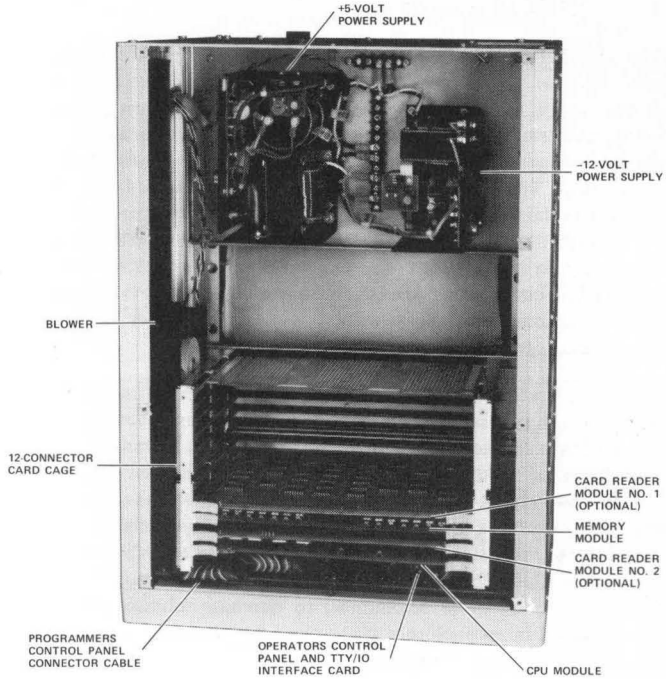


Figure 1–2. Top Internal View of IMP-16L Microcomputer

NOTE

The IMP-16L is available with one or more 4K RAM memory modules, as IMP-16L/3xx. "xx" is the number of 4K modules included with the system. Thus, an 8K system would be designated IMP-16L/308.

1.4.3 Chassis

The chassis accommodates card cages in any combination to a maximum of 30 card slots. The chassis may be a stand-alone unit or may be adapted for rack mounting.

1.4.4 Control Panels

The operators and programmers control panels are attached to the front of the chassis and are shown facing page 1.

1.4.5 Power Supplies

The IMP-16L is supplied with a power supply having the following specification:

+5 volts, 12 amperes
–12 volts, 3 amperes

1.5 BASIC IMP-16L AND SUPPORT OPTIONS

An assortment of hardware, firmware, and software items are available as part of and for the support of the basic IMP-16L. These are listed in table 1–1.

Table 1–1. Major IMP-16L Units and Options

Item	Unit, Contents, Options	Order Number
1	IMP-16L Microprocessor system (with DMA bus) Hardware (IMP16L HARD): • Chassis (wired for the following: 8K memory; and a card reader controller, composed of two logic cards and one I/O card) • Power supply assembly • Teletypewriter/control panel interface logic card • Teletypewriter I/O cable connector • 12-connector card cage • Operators control panel • Programmers control panel • CPU card (includes two CROMs for basic and extended instruction sets) • 4K memory card (includes two 256-by-8 PROM/ROMs programmed for paper tape loader, control panel service, TTY control, and two sockets for additional 256 words of PROM/ROM) Reference Manuals: • *IMP-16L Users Manual* (4200028) • *Tymshare Users Manual* (4200018) • *IMP-16L Utilities Reference Manual* (4200025) • *IMP-16 Assembler Manual* (4200002) Software Paper Tapes and Listings (16LBASSOFT): • IMP-16L CPU Diagnostic Routine (CPUXDI) • IMP-16L Memory Diagnostic Routine (MEMDIL) • IMP-16L Software Debug Routine (DEBUG) • IMP-16L Relocating Loader Routine (GENLDR) • Teletypewriter Software Package (STTYIO)	IMP-16L/304 *or* IMP-16L/308 (with second 4K RAM card)
2	IMP-16L Options Card Reader (Documation Model M300L – 300 cards per minute)	IMP-16/825
3	Card Reader Interface Package Hardware (16LCRHARD): • Card reader controller – two PC boards • One I/O cable assembly Software (16LCRSOFT): • IMP-16L CPU Diagnostic Routine (CPUXDI – uses absolute loader) • IMP-16L Memory Diagnostic Routine (MEMDIL – uses absolute loader) • IMP-16L Software Debug Routine (DEBUG – relocatable loader format) • Card Reader Bootstrap Loader Routine (CRBOOT – binary loader format) • Card Reader Absolute Loader (ABSCR – card reader bootstrap format) • IMP-16L Relocating Loader Format (GENLDR) • IMP-16L Teletypewriter Software Package (STTYIO – relocatable loader format)	IMP-16L/825W
4	IMP-16 Assembler (cross assembler written in FORTRAN) • Source deck • Listing • *IMP-16 Assembler Manual* (4200002) • *Program Description Manual* (4210003) • *Installation of IMP-16L Assembler on System 360/370 Operators Manual* (4200014) • Card decks with listings for card punch routines for CRBOOT format and RLM format	IMP-16S/900A
5	Teletypewriter (ASR Model 33 wired for cable for IMP-16L)	IMP-16/810
6	4K memory card with sockets for ROMs (firmware ROMs not included)	IMP-16L/004
7	64-socket blank circuit card for OEM prototyping	IMP-00H/891
8	90-socket blank circuit card for OEM prototyping	IMP-00H/892
9	Card extender	IMP-00H/890

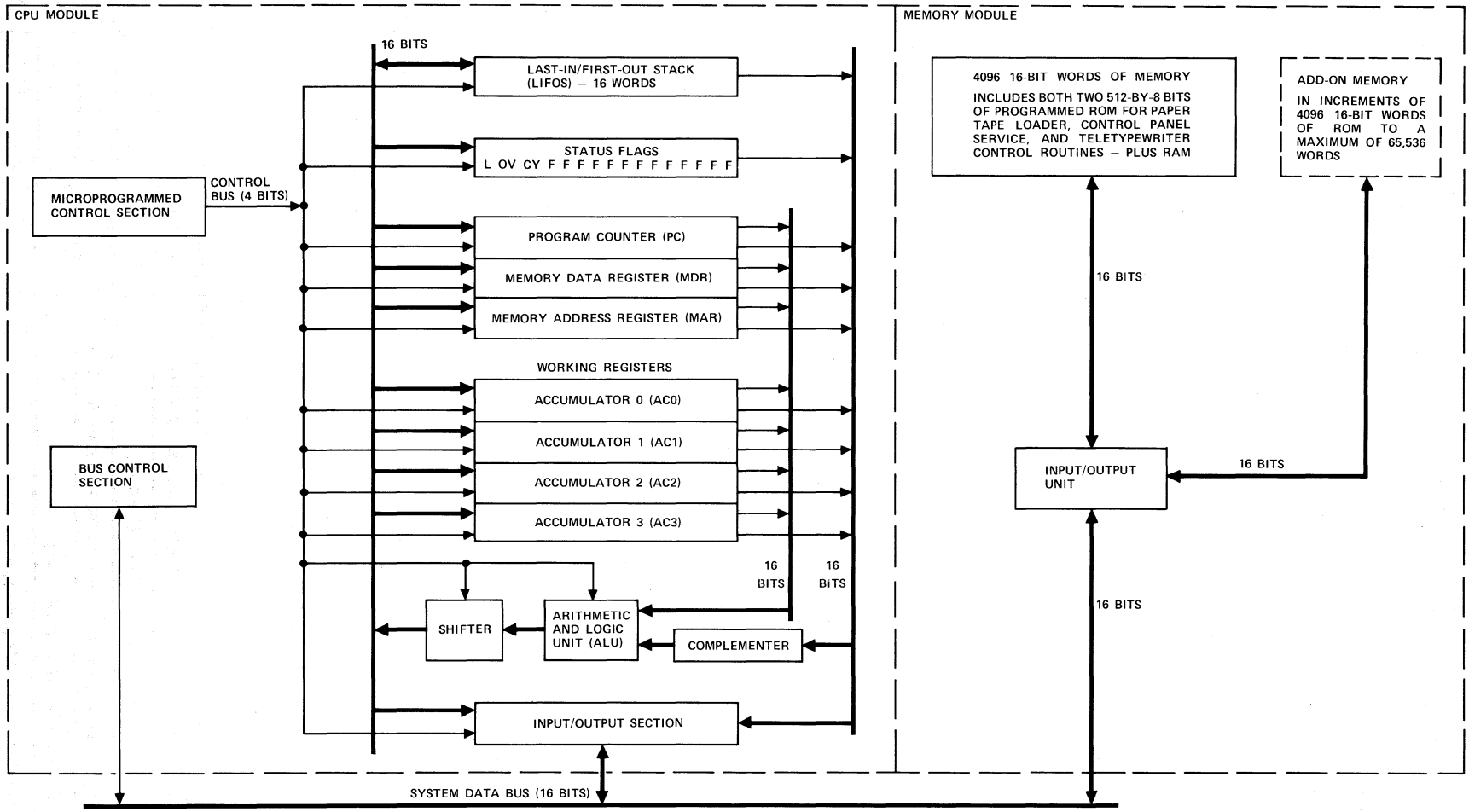


Figure 2–1. IMP-16L Simplified Functional Block Diagram

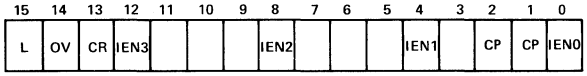
2.0 SYSTEM ORGANIZATION

Although an IMP-16L system may be configured in a variety of ways from the available modules, the central processor module and the memory module are basic to almost any configuration. Figure 2–1 shows the block diagram of a system composed of only these two types of modules. The Central Processing Unit (CPU) provides registers for data storage, the Arithmetic and Logic Unit (ALU) to process the stored data, and the microprogrammed control section to control the operation of the CPU. An Input/Output Section interfaces the registers with the System Data Bus so data may be transferred between the registers and memory or peripheral devices. The Register, ALU, and Input/Output Units are controlled by a Microprogrammed Control Section. The operation of the data bus is controlled by the Bus Control Section of the CPU module. Bus operation is asynchronous with respect to ALU and register operations, so data may be transferred between memory and a peripheral (or a second processor) independent of ALU operation. The Bus Control Section provides for bus timing and resolves the priority of devices requesting bus access.

2.1 REGISTER AND ARITHMETIC SECTION

The CPU module provides four 16-bit Accumulators (AC0, AC1, AC2, and AC3) for data storage (figure 2–1) Two of these (AC2 and AC3) may also be used as index registers.

Three additional registers are provided for use in instruction execution and are not directly available to the programmer. These registers serve the function of Program Counter (PC), Memory Address Register (MAR), and Memory Data Register (MDR). A 16-word pushdown Stack is provided for use with program interrupts and for subroutines. Sixteen Status Flags are also provided in the CPU and are implemented as a register. The flag assignments are shown in figure 2–2. Flags with no assigned function may be used by the programmer as desired.



L = LINK FLAG
OV = OVERFLOW FLAG
CR = CARRY FLAG
IEN0 = INTERRUPT ENABLE FLAG FOR LEVEL 0
IEN1 = INTERRUPT ENABLE FLAG FOR LEVEL 1
IEN2 = INTERRUPT ENABLE FLAG FOR LEVEL 2
IEN3 = INTERRUPT ENABLE FLAG FOR LEVEL 3
CP = RESERVED FOR USE BY CONTROL PANEL

Figure 2–2. CPU Status Flag Assignments

The ALU provides the capability for operating on data stored in any of the above elements. All arithmetic operations are performed using binary twos-complement arithmetic.

Communication between the registers and the rest of the system is provided by the Input/Output Unit. This unit has the capability to request bus access from the Bus Control Unit and to perform a transfer when access is granted.

2.2 MICROPROGRAMMED CONTROL SECTION

All actions of the CPU module are directed by the Microprogrammed Control Section. The Microprogrammed Control Section is similar to a small, low-level processor within a processor. The actions of the Microprogrammed Control Section are determined by a microprogram stored in a read-only memory (ROM). The instructions used for this program are very basic and control the actions of the CPU at a very detailed level. Moreover, they have a short execution time; this makes it practical to use a number of these microprogram-level instructions (microinstructions) to implement more-powerful instructions (macroinstructions) used by the programmer.

Microprogramming permits the IMP-16L to have a much more versatile and extensive instruction set than would otherwise be possible; it also affords the economical development of custom instructions for special applications.

2.3 INSTRUCTION SET

The standard IMP-16L instruction set consists of both a basic 43-instruction set and an expanded 17-instruction set. The basic instructions are implemented by one control read-only memory (CROM) and the expanded instruction by a second CROM. Because the basic instructions are common to all IMP-16 microprocessors, the IMP-16L may be used for program development for other IMP-16 systems.

2.3.1 Basic Instruction Set

The basic format for the memory reference instruction is shown in figure 2–3. Multiple addressing modes are possible, as specified by the value of xr. With the base page mode of addressing (when xr=0), the memory address is determined solely by the value of the displacement field, disp, taken as an unsigned number from 0 to 255. When xr = 1, the mode of addressing is relative: the memory address is formed by adding the Program Counter contents to the value of disp, interpreted as a signed number from –128 to +127. With the remaining two modes of addressing, two of the four working accumulators may be used as index registers: the value of disp taken as a signed number is added to the contents of the index register.

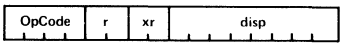


Figure 2–3. Format for Memory Reference Basic Instructions

The r field specifies one of the four working accumulators that is to be used in the instruction. The operation code for the instruction is specified by the OpCode.

Other classes of instructions use modifications of the format shown in figure 2–3. A "register-to-register" class of instructions uses the xr value to specify a second register. A "single register" class of instructions has the operation code field extended to six bits, with the xr value specifying the register. A list of the 43 basic instructions is provided in table 2–1.

2.3.2 Expanded Instruction Set

A group of 17 additional instructions is available with the IMP-16L. Six memory reference instructions are provided; these instructions use indexed addressing similar to the basic instruction set, except a double-word format (figure 2–4) is used (16-bit displacement field). The nonmemory reference instructions (of the expanded group) use a single-word format.

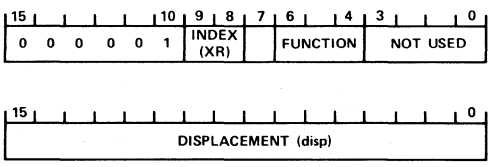


Figure 2–4. Modified Memory Reference Instruction Format

Table 2–1. Basic Instruction Set

Memory Reference Instructions		
Load	Jump Indirect	Skip If AND Is Zero*
Load Indirect	Branch on Condition	Increment and Skip If Zero
Store	Skip If Greater	Decrement and Skip If Zero
Store Indirect	Skip If Not Equal	Jump to Subroutine
Add	AND*	Jump to Subroutine Indirect
Subtract	OR*	Jump to Subroutine Implied
Jump		
Register Reference Instructions		
Push Stack	Exchange Register and Stack	Shift Left
Pull Stack	Exchange Registers	Shift Right
Add Immediate, Skip If Zero	Register Copy	Register ADD
Load Immediate	Rotate Left	Register XOR
Complement and Add Immediate	Rotate Right	Register AND
I/O and Miscellaneous Instructions		
Set Flag	Register In	Push Flags on Stack
Pulse Flag	Return from Interrupt	Pull Flags from Stack
Register Out	Return from Subroutine	Halt

Table 2–2. Expanded Instruction Set

Memory Reference Instructions		
Multiply	Double Precision Add	Load Byte
Divide	Double Precision Subtract	Store Byte
Nonmemory Reference Instructions		
Interrupt Scan	Set Bit	Complement Bit
Jump to Level 0 Interrupt, Indirect	Clear Bit	Jump to Subroutine through Pointer
Set Status Flag	Skip If Status Flag True	Jump through Pointer
Clear Status Flag	Skip If Bit True	

2.4 MEMORY MODULE

The memory module provides 4096 16-bit words of read/write, random access semiconductor memory (RAM) and an optional semiconductor read-only memory (ROM) of 512 16-bit words. The ROM is used to provide a number of commonly used routines in nonvolatile form. The RAM is used for program and data storage as determined by the user.

The RAM cycle time is the same as a normal system data bus cycle time. It responds to read memory or write memory bus transactions within its selected range of 4096 addresses. The address range of a memory module is selected by backplane wiring connection. Systems may be configured with memory add-on to a maximum of 65,536 words in increments of 4096 words.

The access time of the ROM is longer than a normal system data bus cycle; therefore, ROM accesses use an extended bus cycle. For a ROM access, the bus cycle time is increased from the normal 1.05 microseconds to 1.75 microseconds. Thus, programs stored in ROM take 700 nanoseconds longer to execute per instruction. Since a typical instruction execution time is about 8 microseconds, this is less than a 10% increase. Note that the ROM addresses run from $FF00_{16}$ to $FFFF_{16}$ and are not alterable.

***Only AC0 or AC1 is available with these instructions.**

2.5 SYSTEM DATA BUS

All communication between modules in an IMP-16L Integrated Microcomputer occurs over the System Data Bus. This bus is independent of the processor and handles communications between any two devices connected to the bus. In order to transfer information over the bus, a device first requests access through the Bus Priority Network of the Bus Control. If no higher priority request is present, control of the bus is granted and the device then becomes bus master for one bus cycle. During this cycle, the master may address any other bus-connected device (which becomes the slave) and may command a transfer of data to or from the slave.

The System Data Bus, as shown in figure 2–5, is composed of three signal buses. The data bus consists of 16 bidirectional data lines. The timing bus provides the basic system clocks as well as address and data strobes which indicate when data is valid on the bus. The control bus provides a priority system for bus access, signals to indicate whether the current transaction is a read or write from memory or a peripheral, an extended cycle signal, and a response line to indicate that a peripheral device has accepted an order sent over the system bus. See figure 2–6 as an example of the timing for a write memory operation.

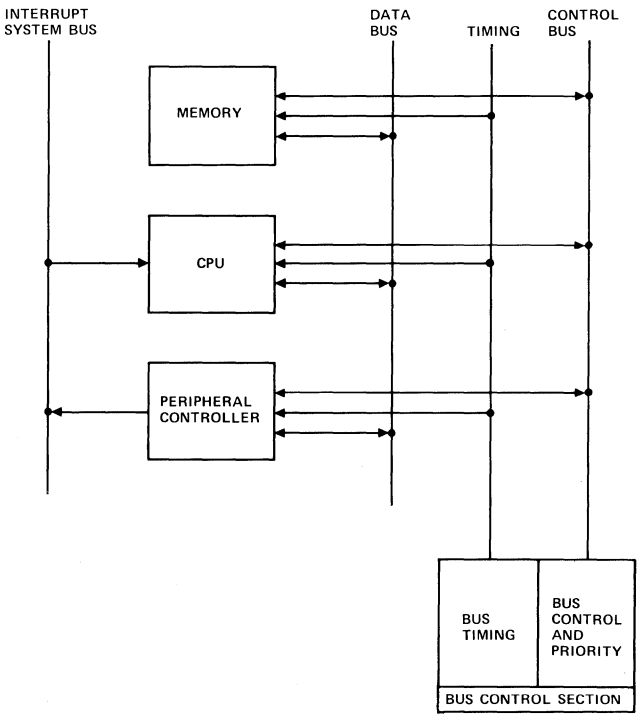


Figure 2–5. System Data Bus Structure

2.6 CONTROL PANEL

The programmers control panel offers access to the CPU registers and system memory and provides features useful in program debugging and system operation. The control panel logic module contains the interfacing circuits needed for the control panel.

2.7 PERIPHERAL UNITS

The peripheral controllers that are available with the IMP-16L are described below. For the OEM customer, the peripheral interface electronics (controller), as well as the peripheral device, can be supplied. Detailed information is available for designing custom interfaces between the IMP-16L bus and other peripheral devices.

2.7.1 Teletypewriter

The Teletypewriter Controller is incorporated on the same circuit board as the control panel logic module; thus, it is available at no additional expense. This "minimum cost" interface operates under program control by the CPU to allow full duplex communication with a single Teletypewriter.

2.7.2 Card Reader

The Card Reader Controller provides communication over the System Data Bus under direct memory access control. The central processor issues commands to the Card Reader Controller over the 16-bit data bus. The Card Reader Controller then responds to these commands by generating the appropriate timing and control signals to the card reader and monitoring the data and status outputs from the card reader. Data read from the card are then transferred directly to the system memory over the System Data Bus, and the Card Reader Controller generates an interrupt to the CPU to signal completion of the order or the occurrence of an error condition.

The Card Reader Controller has two modes of operation. In the bootstrap mode, a control panel switch causes one card to be read and deposited in packed format in the first 40 locations of system memory. In the normal mode, the Card Reader Controller also transfers data directly to memory, but does so in response to a command from the CPU. Data may be transferred in standard format, where each column of data on the card is stored right-justified in one 16-bit word of memory; or in packed format, where 8 bits from each column are stored in alternate halfwords of memory.

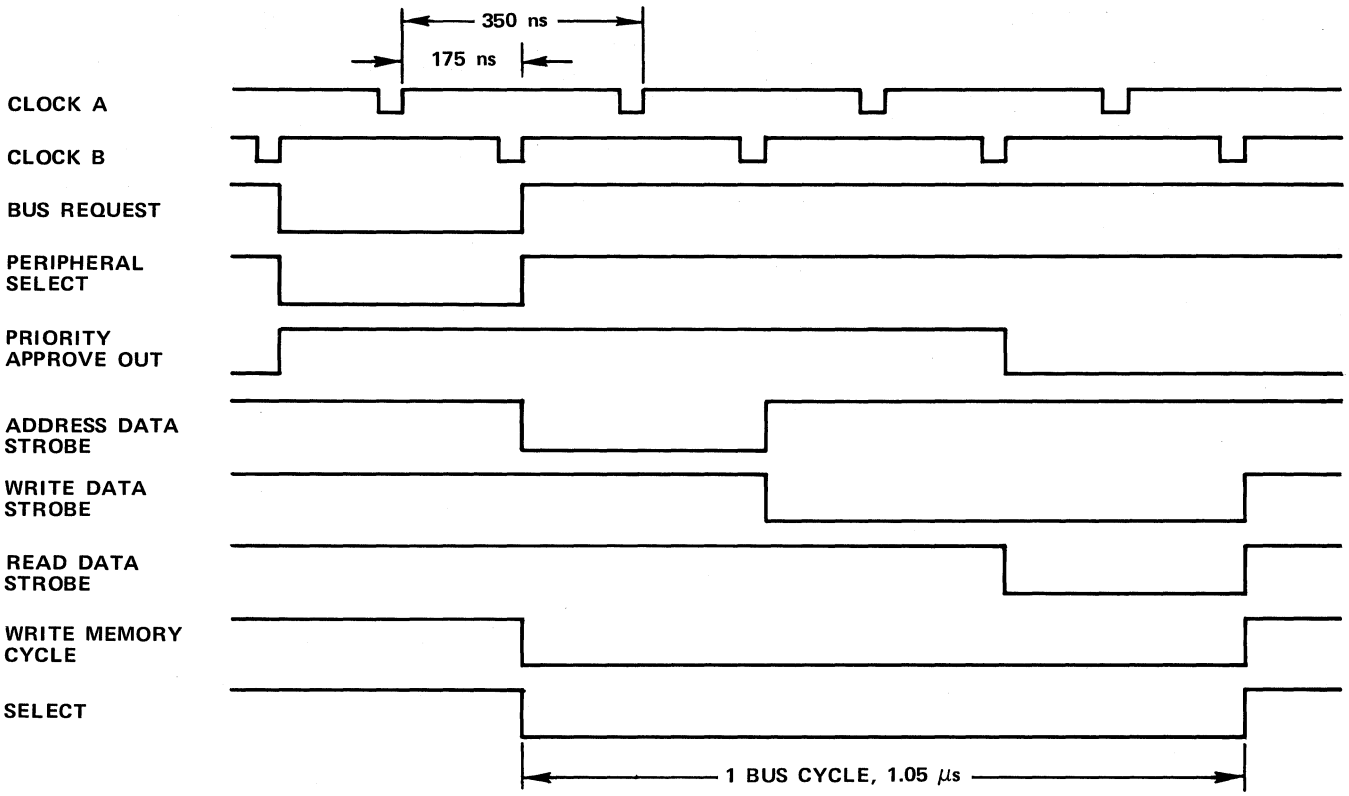


Figure 2–6. Bus Write Memory Timing Diagram

3.0 SOFTWARE

3.1 ASSEMBLER

An assembler written in ANSI FORTRAN is available. This allows maximum transferability to a wide variety of large computer systems and the advantage of file management and text editing capabilities of large general-purpose computer systems.

The assembler contains the following features:

- Relocatable- or absolute-load-module generation
- Conditional assembly features
- Global symbols for communication between independent assemblies
- Wide variety of assembly-time operators (+, –, *, /, AND, OR, NOT)
- Local symbols
- Error messages including error position in the source line

Utility programs written in ANSI FORTRAN are available for conversion of the assembler object output to various media (for example, punched cards and paper tape) and various formats (for example, the card reader bootstrap format).

The assembler with its supporting utility programs has been installed on a nationwide computer utility (timesharing) service and thus is readily available to a wide range of users.

3.2 DIAGNOSTIC PROGRAMS

Extensive diagnostic programs are available for testing and debugging both the central processing unit and the memory.

3.3 LOADERS

A variety of loaders is available for entering programs produced by the assembler into read/write memory. The input media may be either punched cards or paper tape. The format of the programs may be either absolute or relocatable modules.

The following loaders are available:

- A firmware paper tape loader, which can be activated by the LOAD PROG switch on the control panel and which loads an absolute program module via the paper tape reader
- A card reader bootstrap, which loads an absolute hexadecimal card deck into memory
- An absolute loader, which loads one or more absolute program modules via the card reader
- A relocating, linking loader, which loads one or more program modules via the card reader or paper tape, relocates them to any location in memory, and links them together via global symbols specified at assembly time

3.4 PROGRAM DEBUG AID

DEBUG is a relocatable object program that provides aids for the efficient development of user's programs. The program is designed to be used with a Teletypewriter to allow the operator to perform the following debugging functions:

- Printing the contents of registers or selected areas of memory
- Modifying the contents of registers or memory locations
- Providing instruction breakpoint halts or "snapshots" during the execution of a user's program
- Allowing the initiating of execution at any point in a program
- Searching memory

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
(408) 732-5000
TWX: 910-339-9240

National Semiconductor Electronics SDNBHD
Batu Berendam
Free Trade Zone
Malacca, Malaysia
Telephone: 5171
Telex: NSELECT 519 MALACCA (c/o Kuala Lumpur)

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D 808 Fuerstenfeldbruck
Industriestrasse 10
West Germany
Telephone: (08141) 1371
Telex: 27649

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Larkfield Industrial Estates
Greenock, Scotland
Telephone: (0475) 33251
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