National Semiconductor

400103

National SCAN Databook

IEEE 1149.1 Products
Design For Test With Boundary Scan

SCAN
DATABOOK

1996 Edition

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Super-Block™
SuperChip™
SuperScript™
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TeleGate™
The National Anthem®
TinyPak™
TLC™
Trapezoidal™
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National Semiconductor's SCAN Data Book offers Design for Test Solutions to improve R&D development cycle time, reduce test development and manufacturing cost and improve a customer's end system uptime. Designers, test engineers and engineering management using concurrent engineering practices will see life-cycle cost of ownership go down for systems designed with boundary scan.

The SCAN Family of IEEE 1149.1 (JTAG) compliant devices simplify integration of design and test.

SCAN Data Book

National Semiconductor

Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Alpha-Numeric Index

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SCAN Products Selection Guide

Function	Device	Bit-Width	Features
TRANSCEIVERS			
Non-Inverting	SCAN18245T	18-bit	• Dual Output Enable Control Signals • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP and HIGHZ Instructions • 9-Bit Data Busses for Parity Applications • TRI-STATE® Outputs for Bus-Oriented Applications • Reduced-Swing Outputs source 32 mA/sink 64 mA (Comm), and source 24 mA/sink 48 mA (Military) • Guaranteed to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V • TTL Compatible Inputs • 25 mil Pitch SSOP (Shrink Small Outline Package)
Non-Inverting	SCAN182245A	18-bit	• High performance BiCMOS technology (t_{PD} < 4 ns, typ) • 25Ω series resistors in outputs eliminate the need for external terminating resistors • Dual output enable control signals • TRI-STATE outputs for bus-oriented applications • 25 mil pitch SSOP (Shrink Small Outline Package) • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP, IDCODE and HIGHZ instructions
FLIP-FLOPS			
D	SCAN18374T	18-bit	• Buffered Positive Edge-Triggered Clock • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP and HIGHZ Instructions • 9-Bit Data Busses for Parity Applications • TRI-STATE Outputs for Bus-Oriented Applications • Reduced-Swing Outputs source 32 mA/sink 64 mA (Comm), and source 24 mA/sink 48 mA (Military) • Guaranteed to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V • TTL Compatible Inputs • 25 mil Pitch SSOP (Shrink Small Outline Package)
D	SCAN182374A	18-bit	• High performance BiCMOS technology (T_{PD} < 4 ns, typical) • 25Ω series resistor outputs eliminate need for external terminating resistors • Buffered positive edge-triggered clock • TRI-STATE outputs for bus-oriented applications • 25 mil pitch SSOP (Shrink Small Outline Package) • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP, IDCODE and HIGHZ instructions

Function	Device	Bit-Width	Features
LATCHES			
Transparent	SCAN18373T	18-bit	• Buffered Active-Low Latch Enable • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP and HIGHZ Instructions • 9-Bit Data Busses for Parity Applications • TRI-STATE Outputs for Bus-Oriented Applications • Reduced-Swing Outputs source 32 mA/sink 64 mA (Comm), and source 24 mA/sink 48 mA (Military) • Guaranteed to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V • TTL Compatible Inputs • 25 mil Pitch SSOP (Shrink Small Outline Package)
Transparent	SCAN182373A	18-bit	• High performance BiCMOS technology (T_{PD} < 4 ns, typical) • 25Ω series resistor outputs eliminate need for external terminating resistors • Buffered active-low latch enable • TRI-STATE outputs for bus-oriented applications • 25 mil pitch SSOP (Shrink Small Outline Package) • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP, IDCODE and HIGHZ instructions
LINE DRIVERS			
Inverting	SCAN18540T	18-bit	(Same Features of the SCAN18541T)
Non-Inverting	SCAN18541T	18-bit	• Dual output enable signals per byte • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP and HIGHZ Instructions • 9-Bit Data Busses for Parity Applications • TRI-STATE Outputs for Bus-Oriented Applications • Reduced-Swing Outputs source 32 mA/sink 64 mA (Comm), and source 24 mA/sink 48 mA (Military) • Guaranteed to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V • TTL Compatible Inputs • 25 mil Pitch SSOP (Shrink Small Outline Package)
Non-Inverting	SCAN182541A	18-bit	• High performance BiCMOS technology (T_{PD} < 4 ns, typical) • 25Ω series resistor outputs eliminate need for external terminating resistors • Dual output enable signals per byte • TRI-STATE outputs for bus-oriented applications • 25 mil pitch SSOP (Shrink Small Outline Package) • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP, IDCODE and HIGHZ instructions

Function	Device	Features
SYSTEM SUPPORT		
Embedded Boundary Scan Controller	SCANPSC100F	• Compatible with the IEEE Std. 1149.1 (JTAG) Test Access Port and Boundary Scan Architecture • Interfaces up to Two 1149.1 Scan Rings • Fabricated in FACT™ 1.5μ CMOS Process • Generic Parallel Interface Synchronizes Processor Signals with the SCANPSC100F Operation Clock, SCK • 16-Bit Serial Signature Compaction (SSC) at the Test Data in (TDI) Port • Automatically produces Pseudo-Random Patterns at the Test Data Out (TDO) Port • 25 MHz Operation • TTL Compatible Inputs, Outputs are Full-Swing CMOS with 24 mA Source/Sink Capability
Hierarchical and Multidrop Addressable JTAG Port	SCANPSC110F	• True IEEE1149.1 Hierarchical and Multidrop Addressable Capability • The 6 Slot Inputs Support Up to 59 Unique Addresses, a Broadcast Address, and 4 Multi-cast Group Addresses • 3 IEEE 1149.1-Compatible Configurable Local Scan Ports • Mode Register Allows Local TAPs to be Bypassed, Selected for Insertion into the Scan Chain Individually, or Serially in Groups of Two or Three • 32-bit TCK Counter • 16-bit LFSR Signature Compactor • Local TAPs Can Be TRI-STATE Via the $\overline{OE}$ Input to Allow an Alternate Test Master to Take Control of the Local TAPs
SCAN Embedded Application Software Enabler	SCAN EASE	• Processor independent—runs on big/little endian and memory- and I/O-mapped architectures • Compatible with Teradyne VICTORY™ ATPG and JTAG Technology BTPG™ tools (others supported upon request) • Provides automated translation, application and evaluation of ATPG-generated tests in an embedded system environment • Includes a Scan Function Library and National's Embedded Boundary Scan Controller SCANPSC100F device driver to support custom or non-ATPG generated vector applications • Supports embedded test data log for diagnostic processing • Includes Microsoft Windows GUI and serial communication tool for system administration and remote testing • Supports SCANPSC110F Hierarchical and Multidrop JTAG Addressable Port architecture

Section 1

Design for Test Solutions with Boundary Scan

Section 1 Contents

Design for Test Solutions with Boundary Scan

What is DFT?

Design for Test, or DFT, is being used by many companies to lower the overall cost of development, manufacturing, test and field service. Some companies call it "Concurrent Engineering" and it replaces the "Over-the-wall" method of product development. In each stage of the product life-cycle, a consideration for testing is made in the earliest stages of design.

National employs boundary scan technology to enable not just chip testing, but also board testing, system testing, and in-field service testing.

What is the standard? For most purposes the following terms are used interchangeably:

IEEE 1149.1

1149.1

JTAG

Dot 1

Boundary Scan

SCAN

IEEE 1149.1 is a set of standards for *board* test protocol. Newer standards are being developed by different IEEE working groups for *system* test and *analog* test protocol. IEEE 1149.1 is a 4-wire standard which allows compliant silicon to perform interconnect testing. It supports BIST (Built In Self-Test), and provides an alternative or supplement to Bed of Nails testing and functional testing.

Adding boundary scan to a board does add cost and time to the design cycle due to the increased cost of boundary scan compliant components and initial time investment required to understand the boundary scan architecture and tools. However, these costs are easily justified when viewing the benefits and cost savings boundary scan provides at every stage of a product's life cycle. What was originally developed as a manufacturing test tool offers benefits before, during and after manufacturing.

Board Development

A designer uses boundary scan to save time during the prototyping and design debug stage. With boundary scan, non design-related, structural faults can be detected and then eliminated at both the board level and component level. This allows designers to effectively locate and resolve design related problems. Additionally, designers use boundary scan to partition a board, load seed values for devices with BIST and/or load internal values into device registers (e.g. internal scan, LSSD, etc.) to isolate logic errors. With boundary scan, many of the vectors developed and used during the design phase can be passed on to manufacturing to provide an additional cost and time savings.

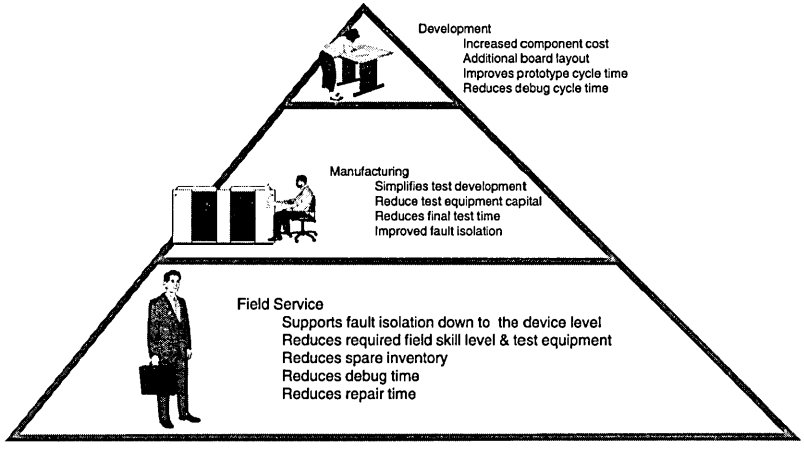

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FIGURE 1. Boundary Scan Benefits Entire Product Life Cycle

Board Manufacturing

The key benefits at the manufacturing phase are test development time savings; improved fault coverage and diagnosis; and improved test throughput through reduced test times. As with the design phase, boundary scan provides the additional advantage of applying many of the vectors used for manufacturing to be later applied during field debug and diagnosis.

Field Service

Field failures are often due to structural failures which surface due to the stress—temperature, humidity, vibration—that the boards are exposed to in the field environment. Using boundary scan, field technicians have the ability to quickly test for structural faults down to the component level without the burden of probing or returning the board to the factory. Eliminating these tasks allows for more efficient diagnosis and repair which reduces cost and system downtime.

The advantage of boundary scan become even more apparent when boundary scan is extended from the board level to the system level test.

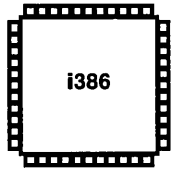
Often, the objection to the use of boundary scan include:

1. Performance (speed) decreases due to the extra delay added by the boundary scan multiplexer in the data path.
2. Cost increases due to additional silicon and TAP pins on the device package—as well as design time.
3. Delay to market due to additional circuit design time.

However, the manufacturing benefits as well as product development cycle time improvements easily outweigh the initial added efforts.

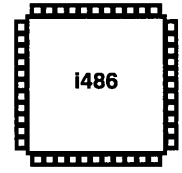
Using boundary scan on their 80486 design, Intel realized two orders of magnitude improvement in time to develop circuit test-patterns with significant cost reduction, too. See *Figure 2.*

Boundary scan provides cost savings over the life cycle of a system in the testing of boards, systems, and in field maintenance.



80386 Conventional ICT Patterns

Study Part	1 Weeks
Develop Test Patterns	4 Weeks
Verify on ATE	2 Weeks
Total Time	7 Weeks ($14,000)



80486 with VICTORY/1149.1 ICT Patterns

Generate/Verify BSDL	8 Hours
Generate Test Patterns	---
Verify Patterns	2 Hours
Total Time	10 Hours ($500)

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FIGURE 2. Intel Reduced Test Development Time and Test Cycle Time

The Economics of Design for Test

Many of the perceived costs of a DFT strategy fall upon the design organization, while many of the benefits reward the manufacturing and test organizations. This adversarial position can be eliminated by meeting the needs of all organizations involved in DFT.

EFFECT OF DFT BY DEPARTMENT

Design	Die Area	Increased Cost
	Design Cycle Time	Lowered Cost
	Performance Impact	Increased Cost
	EDA Tools	Increased Cost
Test	Fault Simulation	Lowered Cost
	Simplified Debug & Diagnostics	Lowered Cost
	Fewer Design Changes	Lowered Cost
	Lower ATE Cost	Lowered Cost

IMPACT OF DFT VARIABLES BY DEPARTMENT

Profit Factor	Department	Impact
Units Sold	Design	New product feature, faster design cycle time
	Marketing	Lower selling price through cost reduction
	Sales	Lower selling price
Selling Price	Design Marketing Sales	New product features of higher quality
Variable Cost	Marketing Sales Manufacturing Design	Higher cost of silicon, lower overall manufacturing costs
Fixed Cost	Manufacturing	Lower cost ATE, more productive ATE (higher throughput), improved fault coverage
	Field Service	Less field spare inventory, faster debug and diagnosis
Total Profit	Management	Overall investment strategy, capital utilization, ROA, cost calculation methods

Boundary scan also provides cost savings which can be measured directly in production and can reduce the time to market. This method fits within a concurrent engineering environment in various ways:

- Reduces test time and costs
- Reduces test preparation time and costs
- Increases the time available for test programs for production
- Allows simpler, less costly testers
- Shortens diagnostic times
- Provides a commonality of tester interface
- Allows the continued test of high density/poor-access boards

Where the Failures Are

PCB test failures can result from either structural faults (opens, stuck-ats, bridging, missing/wrong components, etc.), analog failures (faulty or incorrect passive components) or performance faults (timing problems or board/component design errors). However, structural faults account for the overwhelming majority of board failures during manufacturing test. In fact, data from Teradyne, a leader in the test industry, suggests that greater than 80% of the board level test manufacturing failures are structural in nature. See *Figure 3*.

Where the Failures Are (Continued)

A number of methods have been implemented to provide a means of detecting structural failures. These methods range from use of functional board testers (FBT) to in-circuit testers (ICT) and combinational (ICT and FBT) testers. Boundary scan was created to provide an improved technique for screening structural faults through reduced test programming time and improved fault coverage.

It should be noted that boundary scan is not a technique for detecting at-speed, dynamic performance faults. Performance fault testing requires the use of an at-speed functional board tester. With very thorough debug and simulation during board development and pre-assembly test of board components, the need for performance fault testing during manufacturing is up to the discretion of the board manufacturer and its customers. Even if at-speed functional testing is required, the use of structural testing prior to functional testing will help eliminate manufacturing defects and ease the diagnosis of performance or functional failures.

For the cases where access is possible, the access occurs at a price. Even if it is possible to add test pads, pads consume board area—contrary to the goal of saving board area—and can present performance degradation. Additionally, the cost increases substantially for test point fixtures, the fine tip probes or clam shell probes for double sided boards. See *Figure 4*.

For the case of MCMs (multi-chip modules) and inaccessible board nodes (nodes under a mezzanine card, blocked by a component or other hardware, etc.), access is not possible and the only option other than boundary scan is cluster testing: using bed of nails to apply stimulus on MCM or board cluster inputs and measure values at outputs of the MCM or board cluster. This creates the same burdens as when using a FBT, where creating test vectors requires knowledge of the entire MCM or board cluster functionality which increases test development, diagnostics and test time.

The existence of inaccessible nodes in manufacturing are passed on to the field service engineer attempting to use manual probing as a vital step in debugging a board failure. This leads to increased field service time and costs and, longer system down time for your customer.

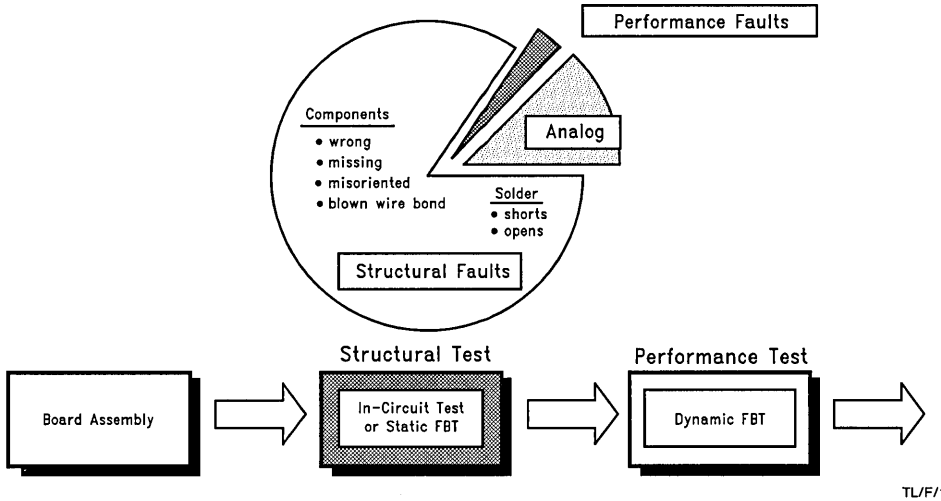

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FIGURE 3. The Majority of Printed Circuit Board (PCB) Manufacturing Failures Are a Result of Structural Faults

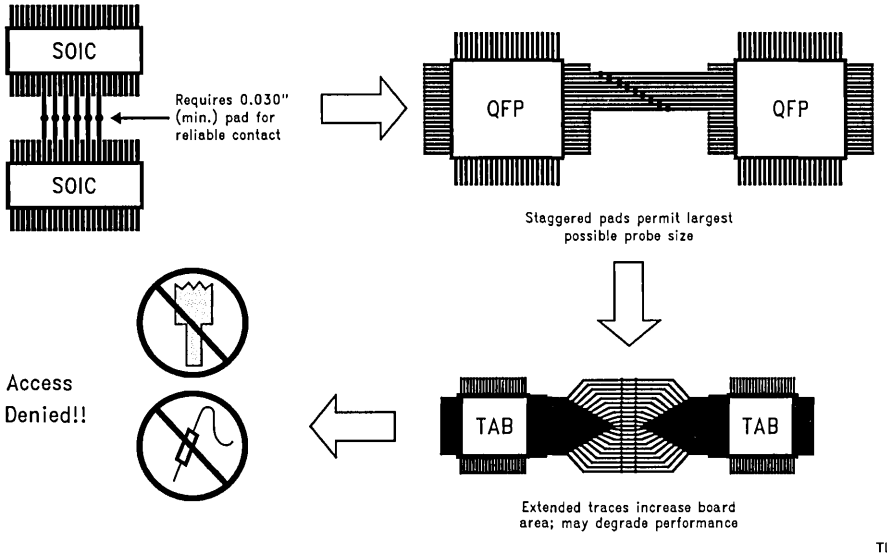

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FIGURE 4. Device Packaging Density Makes Physical Access Expensive, Unreliable, or Impossible

Boundary Scan Fundamentals

The IEEE 1149.1 standard defines a 4 pin TAP (Test Access Port) which allows electrical access around the "boundary" of compliant devices. The TAP pins are:

- TDI Test Data In
- TDO Test Data Out
- TMS Test Mode Select
- TCK Test Clock

It also defines a 16 state TAP Controller and several registers used to control the test data.

Boundary scan registers are placed at all I/O pins, and they are interconnected to form a serial chain around the core functionality of the device.

With the addition of the boundary scan registers at the I/O of a component, interconnect testing with boundary scan devices can be performed with no dependence on device functionality. IEEE 1149.1 compliant automatic test program generation (ATPG) tools are available from a number of vendors to automatically generate interconnect tests using a board netlist and BSDL files for each 1149.1 compliant device on the board as inputs. BSDL files provide a description of the specific implementation of boundary scan features within each compliant component.

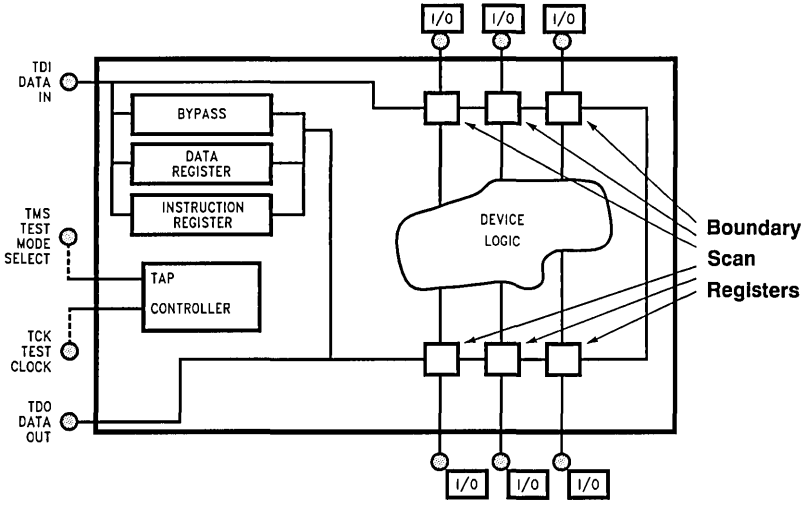

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FIGURE 5. 1149.1 Device Hardware

In like fashion as the chip, the boundary scan chain is extended to the board in a serial scan chain. Boards in systems can also be linked in a scan chain.

When placed on a printed circuit board, each 1149.1 component is connected together to form a chain of boundary scan devices. In *Figure 6*, note the scan chain connections:

TDI/TDO: The tester's serial test data out pin is connected to the first device's TDI. The test data is passed from the first device to the second device via the TDO pin which connects to the second device's TDI pin. This chain formation continues until the last device's TDO pin is connected back to the tester. Therefore, shifting data into a device's instruction or data registers requires that the data passes through every JTAG device which is connected ahead of the device in the scan chain. Additionally, as the data is shifted into the device, the data previously stored in the selected instruction or data register is shifted out of the chain. The tester software either reads and evaluates the returning data or masks it out. The Bypass register is included to shorten the chain when shifting data through devices which are not participating in a given scan operation.

TCK/TMS: All devices in the chain are connected in parallel to the TCK and TMS signals. This means that all the devices' TAP controllers are in the exact same state and transition simultaneously. The instruction register allows each device to include different data registers in the scan chain and perform different scan operations.

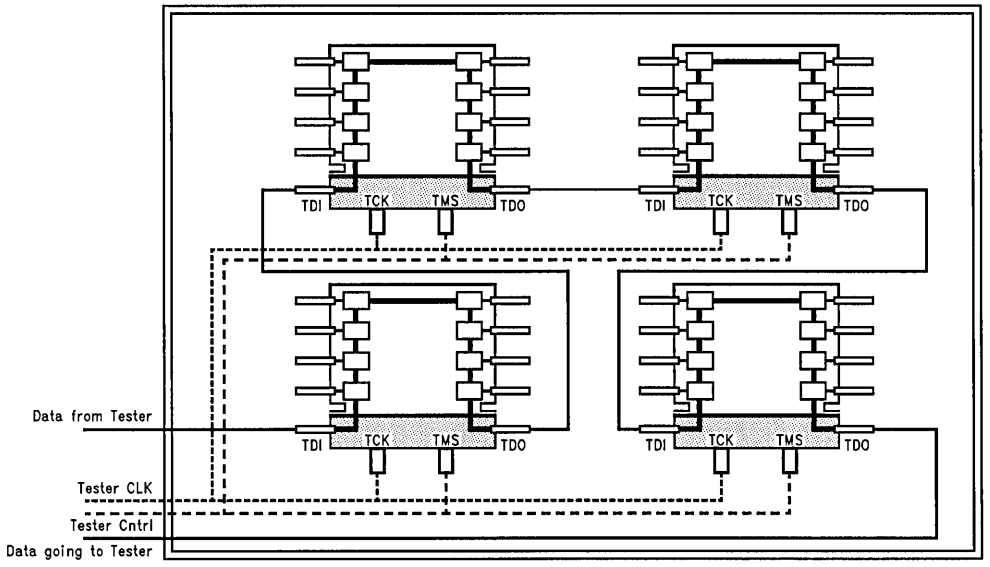

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FIGURE 6. 1149.1 Boundary Scan Chain

Implementing boundary scan on every component on the board provides the maximum benefit in terms of reduced tester cost, test development times and concurrent engineering. However, boundary scan can also complement an ICT in testing structural faults. See *Figure 7*. This was fully recognized by ICT tester companies when they developed their ICT systems and most ICT's now have a connector dedicated for boundary scan testing. Additionally, these tester companies included the option of mixing boundary scan and ICT in their ATPG tools by using ICT component libraries for non-scan products and BSDL for scan products. For example, vectors can be automatically generated to drive signals with boundary scan and compare results using physical test probes. Many companies have already invested millions of dollars in ICTs and may want to use boundary scan only where required for inaccessible nodes, non-library parts, etc. or as a means of cutting ICT fixture costs.

For smaller companies or companies in the process of purchasing new ICT equipment, implementing boundary scan may provide a way to reduce the required ICT features like number of channels providing a tremendous reduction in the tester cost where cost ranges from $200K up to $1M.

Figure 7 shows two examples of ICT and boundary scan working together. The lower of the two graphics shows cluster testing. Cluster testing is the testing of a group of devices by applying data to the inputs of the group or cluster and evaluating the results on the output of the group or cluster. Cluster testing can vary from testing the interconnects between the components in the cluster to testing the internal nodes of each component within the cluster.

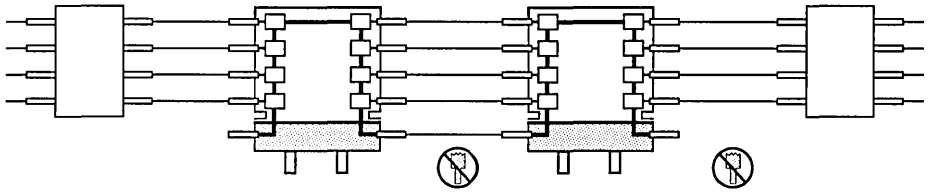
System Test

National supports the needs of the system design architect by:

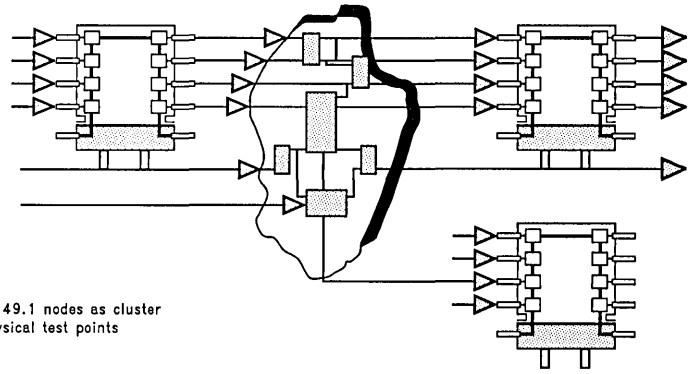
- Acknowledging the need for live insertion on the backplane
- Fully complying to IEEE 1149.1 (board test)
- Addressing the 1149.5 standard (system test)

While boundary scan diagnostics are particularly useful for telecommunications and workstations, their benefits also extend to board manufacturers that want to reduce the time-to-market of their products.

For small companies, we provide the option to expensive $1 million test equipment. With help from our software and hardware partners (such as Corelis and JTAG Technologies), National can support total system test solutions with PC-based boundary scan devices, software, and hardware solutions.



Boundary scan works with an ICT to provide access to inaccessible nodes and/or to reduce ICT physical test points



Treating non-IEEE 1149.1 nodes as cluster can eliminate ICT physical test points

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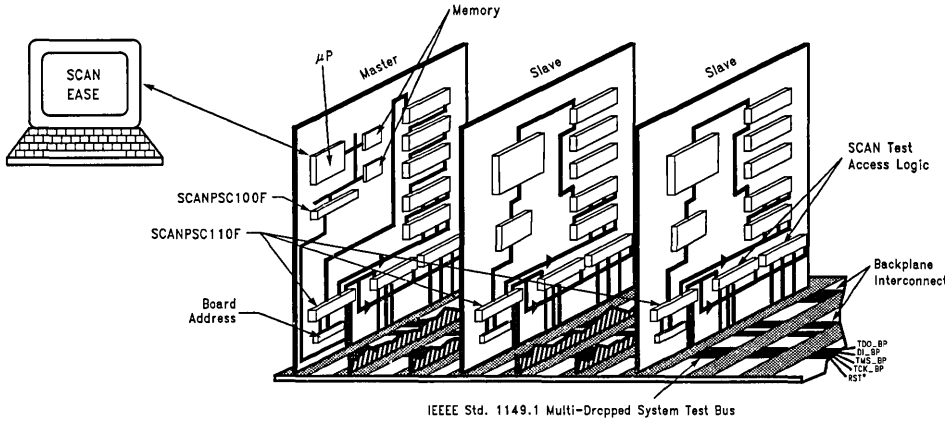
FIGURE 7. Boundary Scan and ICT Can Work Together

HOW IT WORKS

For system test and diagnostics, start with the Embedded Boundary Scan Controller, SCANPSC100F and your choice of microprocessor and memory to create an embedded test master, freeing up external test equipment.

Add the Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F Bridge to each board in the multidrop or hierarchical backplane to address any number of boards, selectively or in groups, for board test as well as backplane interconnect failures. If a board is off-line or removed, the scan chains remain unbroken.

But what if a board is removed while powered up? Then add SCAN ABT Test Access Logic along the back-plane card edge to provide fault-tolerant power-up and power-down live insertion. Now backplane interconnect checks can be performed and boards inserted/removed through controlled power-up/power-down sequences. The 25Ω series resistors on SCAN ABT outputs also eliminates the need for an external damping resistor.



- SCAN EASE Compatible with 1149.1 hardware and existing test board vectors
- SCANPSC100F creates embedded test master
- SCANPSC110F enables individual board addressing, multiple and hierarchical boards for testing "like" boards simultaneously
- SCAN ABT live insertion

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FIGURE 8. Creating Embedded System Test

System-Level Embedded Test

Developing hardware and software to implement embedded test capability can be significant in terms of both time and expense. To reduce our customers' in-house software development efforts, National offers SCAN EASE to apply, control, and evaluate tests within an 1149.1-compliant embedded system. For more examples refer to AN-1022, Boundary-Scan, An Enabling Technology for System Level Embedded Test.

SCAN EASE TOOLS

SCAN EASE (Embedded Applications Software Enabler) is a suite of software tools that enables ATPG (Automatic Test Program Generation) or custom-generated test vectors to be embedded within an IEEE 1149.1 compatible system. See *Figure 9*. SCAN EASE includes three groups of tools:

- EmbedPrep
- EmbedTest
- EmbedComm

TEST DEVELOPMENT PROCESS

The test development process for embedded system test begins with generating tests using an off-the-shelf ATPG tool. See *Figure 10*. Separate tests are created for each board type in the system during manufacturing test development. These tests can be re-used for embedded test. National's SCAN EASE includes tools to compile test vectors stored in Serial Vector Format (SVF) or Pattern Format (PAT) into Embedded Vector Format (EVF) for use with EmbedTest. EVF is a compact binary vector format suitable for embedded applications. Several of the board-level EVF files can be concatenated to create a system-level test. Partitioning tests enables EmbedTest to isolate and report pass/fail information to the partition level (board, module, etc.) without running diagnostic software. EVF test files can be located in ROM for power-up self test or down loaded to RAM.

EmbedTest provides a set of functions that enable communication between the embedded system and a serial interface to a system administrator or remote computer. EmbedTest commands—such as configuration, reporting test results, downloading new tests, and uploading data logs—are performed over this interface.

Note that SCAN EASE is also included in our SCAN Developer/Demo Kit. This kit demonstrates system board check, interconnect testing, and backplane testing (see *Figure 8*). Included are:

- Embedded Boundary Scan Controller—SCANPSC100F works with customer's choice of microprocessor
- Multidrop and Hierarchical Addressable JTAG Port SCANPSC100F SCAN Bridge for system test—addresses any number of boards in the backplane
- SCAN ABT Test Access Logic—provides live insertion capability for boards along the backplane

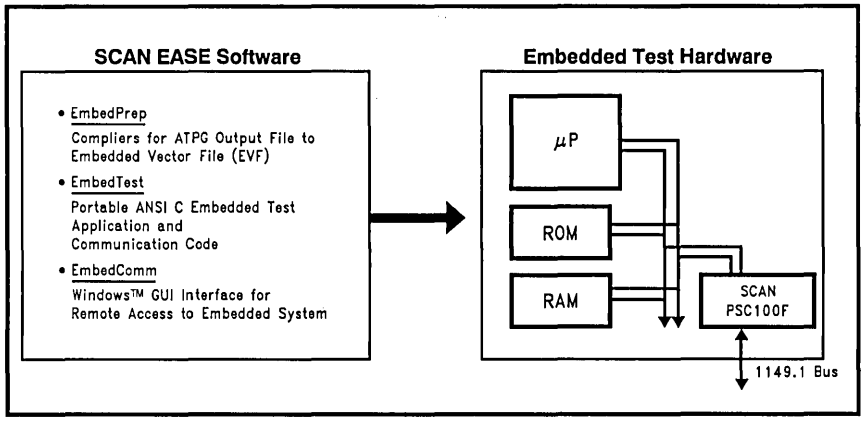

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FIGURE 9. SCAN EASE Enables ATPG Test Vectors to be Embedded

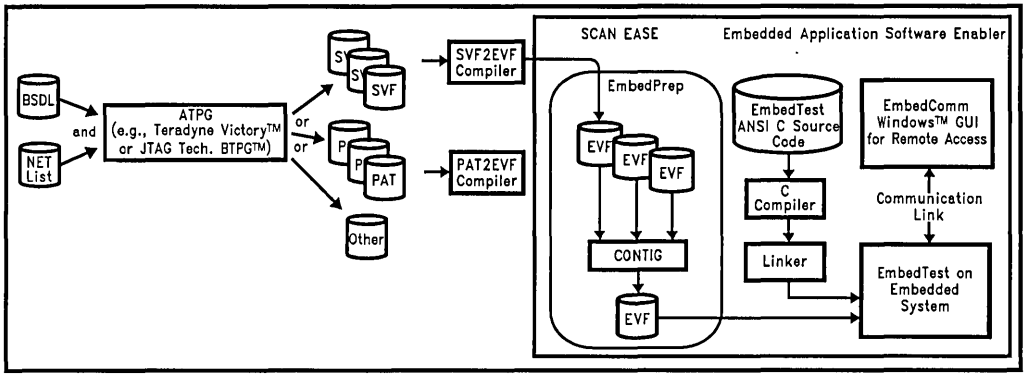

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FIGURE 10. SCAN EASE Reuses Existing Test Vectors, Compiles them for your Target Microprocessors and Compresses them for Storage in Memory

The Impact of PC and Communications Technology

The market is ripe for the valuable services provided by PC-based and in-system testing. Having a system perform its own self-test upon power-up frees up design engineers to add more features to an end system, as opposed to spending money on testing a system. With advances in PCs, the capability of remote testing now exists. It is possible to dial up a modem service, connect to a remote system in the field and perform maintenance, improving the end-system uptime. Once the target site is on-line, the system performs self-testing and reports back failures.

There are many factors associated with improving end-system uptime including systems that require high reliability, systems that perform services for large groups of people or customers that need to stay on-line all the time. Initially SCAN EASE will diagnose the problem for the purpose of repair. Since vectors are stored in ROM, it will be easy to download system upgrades and new system configurations in the near future.

Recent applications have arisen to extend the use of IEEE 1149.1 boundary scan all the way to system integration and field service. This new arena boasts additional leverage for the re-use of test vectors, improved time to break-even for products and increased value to end-users.

What products will result from this technology? A tester on a chip will go into simple machines that give people trouble like printers, copiers, facsimile machines, and give them the intelligence to do power-on self-test, diagnosis and repair. The machine will be able to call the home office through advanced communications capabilities, communicate with the home office, literally saying, "This is what is wrong with me." Remote verification of the diagnosis as well as repair can then take place.

On an even wider scale, telecommunications equipment buried in remote locations will be accessible. Board will be tested, brought off-line, and others brought on-line to replace them—electronically and remotely.

Section 2

Description of Boundary Scan

Section 2 Contents

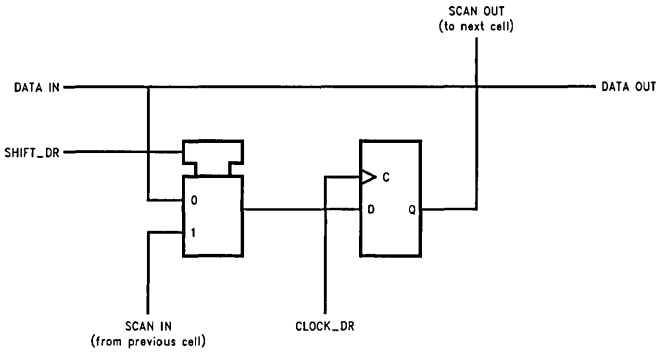
Description of Boundary-Scan

Boundary-Scan Circuitry

The scan cells used in the Boundary-Scan register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals see *Figure 1.* AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

Scan Cell TYPE1
Input Boundary-Scan Cell



TL/F/12132–3

Scan Cell TYPE2
Output Boundary-Scan Cell

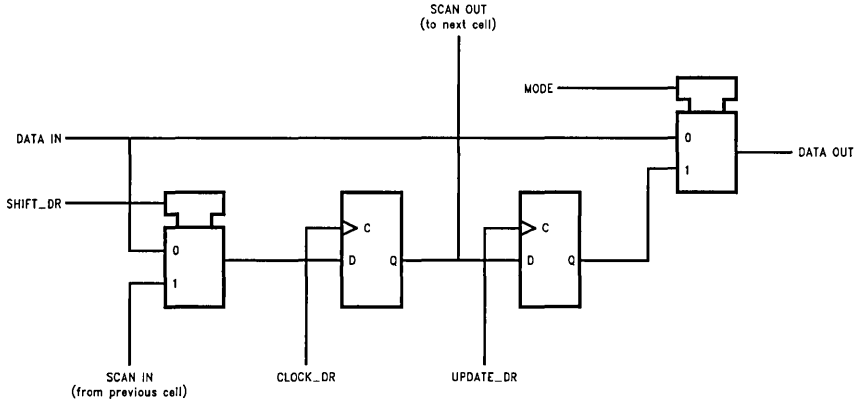


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FIGURE 1. Type 1 and Type 2 Scan Cells are Located at Input and Output Pin, Respectively

Boundary-Scan Registers

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

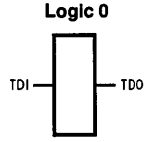


FIGURE 2. Bypass Register Scan Chain Definition

TABLE Ia. Scan ABT Product IDCODE (32-Bit Code per IEEE 1149.1)

Device	Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
SCAN182245A	0000	111111	0000000000	00000001111	1
SCAN182373A	0000	111111	0000001000	00000001111	1
SCAN182374A	0000	111111	0000000111	00000001111	1
SCAN182541A	0000	111111	0000001001	00000001111	1

MSB **LSB**

TABLE Ib. SCAN CMOS Device Identification (8-Bit Code Described in Device BSDL)

Device	8-Bit Code
SCAN18245T	00111101
SCAN18373T	00101101
SCAN18374T	00011101
SCAN18540T	01001101
SCAN18541T	10111101

Scan ABT devices include the 32-bit 1149.1-compliant IDCODE as shown in Table Ia. Scan CMOS devices do not include the IDCODE, however they do have an 8-bit device identification code which is described in its device BSDL model and shown in Table Ib.

Tables IIa, IIb and IV show which instructions are included for SCAN ABT and SCAN CMOS.

The INSTRUCTION register *Figure 3* is an 8-bit register which, for SCAN ABT, captures the default value of 10000001 (SAMPLE/PRELOAD, Table IIa) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is not required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction.

In the case of SCAN CMOS, the 8-bit INSTRUCTION register captures the device's 8-bit identification code in Table Ib. For more information refer to the section on instruction definitions.

TABLE IIa. SCAN ABT Instruction Registers

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

TABLE IIb. SCAN CMOS Instruction Register

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
All Others	BYPASS

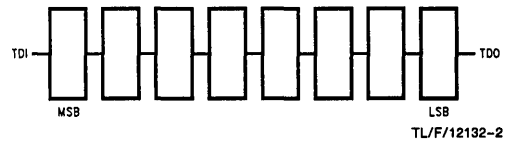


FIGURE 3. Instruction Register Scan Chain Definition

Boundary Scan Overview

This document is a supplement to the National Semiconductor SCAN Test Access Logic products datasheets. It provides an overview of the IEEE 1149.1 (boundary scan) circuit features included on the National's SCAN devices. The IEEE 1149.1 Std. document should be consulted for more detailed information about the IEEE 1149.1 standard requirements.

The IEEE 1149.1 boundary scan standard circuitry is comprised of 3 functional blocks—a test access port (TAP), a TAP controller and a set of registers.

I. TEST ACCESS PORT (TAP)

The Test Access Port (TAP) consists of four pins dedicated solely to the operation of the test logic. The four pins include TMS (Test Mode Select), TDI (Test Data In), TDO (Test Data Out), and TCK (Test Clock). These products contain a power-up reset function in lieu of adding the $\overline{\text{TRST}}$ pin. The motivation of this option is to save package size and hence customer board space, thus making the decision to implement 1149.1 less costly to the system designer.

TCK: This input provides the test clock for the test logic defined by the IEEE 1149.1 Standard. In accordance with the standard requirements, all test logic will retain its state indefinitely upon stopping TCK at a logic low, or 0. Additionally, the same retention may occur upon stopping TCK at a logic high, or 1, which is a permission granted by the standard. The motivation for TCK to be a dedicated test input is 1) to insure that it can be used independently of system clocks running at different frequencies, 2) that it permits shifting of test data without altering any system logic state when undertaking on-line system monitoring tasks, and 3) that it can be used to test all board interconnect even when that interconnect transfers clock signals from one device to another.

TMS: This input is the command signal to control system operation modes. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pull-up resistor to implement a logic high for an undriven input. The requirement that an unforced TMS input produce a logic high is to ensure that the normal operation of the design can continue without interference from the test logic by guaranteeing that an undriven TMS input can put the TAP Controller into the Test Logic Reset state.

TDI: This signal provides the serial data input of test instructions and data to the test logic. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pull-up resistor to implement a logic high for an undriven input. Test data will arrive at TDO without inversion after the appropriate number of clock cycles as determined by the length of the register currently connected between TDI and TDO. The requirement that an unforced TDI input produce a logic high is to assist in the determination of manufacturing defects in the test scan chain interconnect. A consistent field of 1's in shifting out the data registers can indicate where a break in the scan chain interconnect occurred.

TDO: This signal provides the serial data output of test instructions and data from the test logic. Changes in the logic state and drive activity for this output occur upon the falling edge of TCK. This is to avoid a race condition when TDO is connected to TDI of the next chip in the scan chain which is sampled on the rising edge. This output shall remain inactive except when the scanning of data is in progress. This is to permit the ability to multiplex scan chains on the board without causing signal contention between multiple TDO outputs connected together to form parallel scan chains.

II. TAP CONTROLLER

The TAP controller is a 16 state finite state machine which controls the insertion of the data and instruction registers (described later in this document) between TDI and TDO pins, and controls the flow of data through these registers.

Changes in the state of the TAP Controller (see *Figure 4*) are solely a response to the value of TMS upon the rising edge of TCK, or upon power-up (or the application of a logic low to the optional $\overline{\text{TRST}}$ input which is not included in the products referring to this document). In any given state actions of the test logic taken in that state occur on the falling or rising edge of TCK following the rising edge of TCK which caused the TAP Controller to enter the state initially.

Note: It may happen that actions to occur in one state happen on the same rising edge of TCK that cause the TAP Controller to enter the next state.

Test Logic Reset: In this state, the boundary scan test logic is disabled to allow the device to function normally. All boundary scan registers are reset to their default states. This state is entered by at most, five TCK cycles while holding TMS high or asynchronously by pulling TRST low (if TRST pin is included). The IEEE 1149.1 standard requires that an internal pull-up be included on the TMS pin to assure the TAP will return and remain in test logic reset if TMS is floating.

Run Test/Idle: This state provides a dual purpose depending on the active instruction. It is included to allow for optional or user defined tests, including BIST, to be performed. For the required IEEE 1149.1 instructions, all test data registers retain their current state (i.e., remain idle).

SELECT-DR Scan: This is a temporary state in which all test data registers retain their previous values.

Capture-DR: In this controller state data may be parallel loaded into the data register selected by the current instruction; otherwise, it retains its previous values.

SHIFT-DR: In this state the test data register selected between TDI and TDO by the current instruction will shift one stage at each rising edge of TCK. TDO is active during this state. Test data registers not selected by the current instruction maintain their previous values.

Exit1-DR: This is a temporary state in which all test data registers retain their previous values.

PAUSE-DR: This is a temporary state in which all data registers retain their previous values. This state is intended to temporarily halt the shifting of test data into the data register selected while retaining the ability to keep TCK running; TCK may be a free-running clock. This state is often used to load additional test vectors from external memory.

Exit2-DR: This is a temporary state in which all test data registers retain their previous values.

UPDATE-DR: The parallel output register of the selected test data register may be updated on the falling edge of TCK in this state, provided the test data register has such a parallel output register. The intent of the parallel output register is to provide the ability to apply the contents of the test data registers to the test logic simultaneously rather than applying it as it is being shifted in. All test data registers not selected by the current instruction retain their previous values.

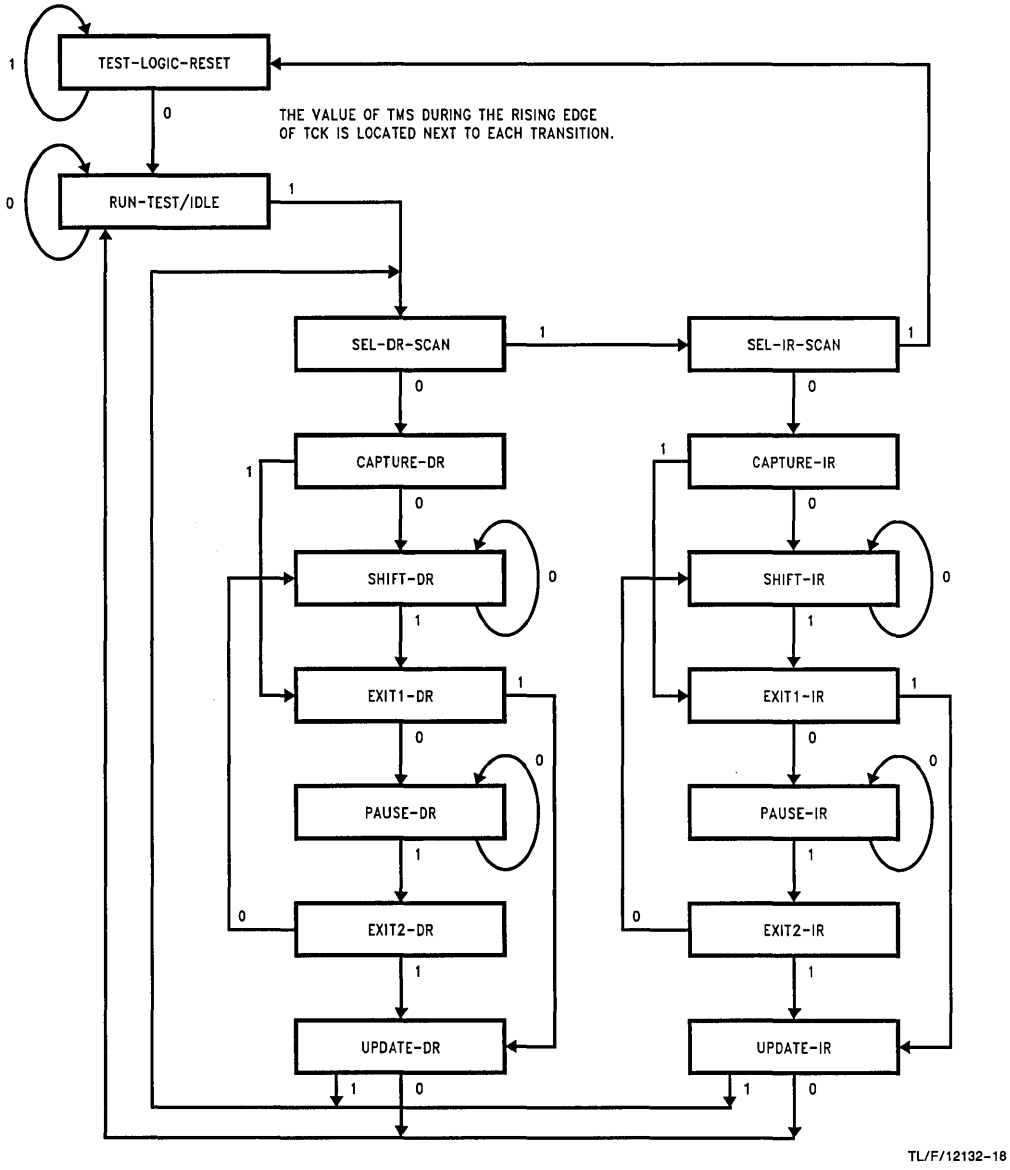


FIGURE 4. TAP Controller State Diagram

SELECT-IR Scan: This is a temporary state in which the INSTRUCTION register retains its previous value.

Capture-IR: In this controller state, a fixed value must be parallel loaded into the INSTRUCTION register. The only restriction on what that data may be is that its least significant bit must be a logic high, or 1, and its second least significant bit must be a logic low, or 0. These opposite state bits can be used to check the correct operation of the scan chain on the board by forcing a bit toggle when the instructions are shifted.

SHIFT-IR: In this state the INSTRUCTION register selected between TDI and TDO will shift one stage at each rising edge of TCK. TDO is active during this state.

Exit1-IR: This is a temporary state in which the INSTRUCTION register retains its previous value.

PAUSE-IR: This is a temporary state in which the INSTRUCTION register retains its previous value. This state is intended to temporarily halt the shifting of test data into the INSTRUCTION register while retaining the ability to keep TCK running. This state is often used to load additional test vectors from external memory.

Exit2-IR: This is a temporary state in which the INSTRUCTION register retains its previous value.

UPDATE-IR: The parallel output register of the INSTRUCTION register will be updated on the falling edge of TCK in this state. The intent of the parallel output register is to provide the ability to apply the contents of the INSTRUCTION register to the test logic simultaneously rather than applying it as it is being shifted in.

TDO OUTPUT ACTIVITY

Control of the TDO output buffer follows Table III.

TABLE III. TDO Output Buffer Control

Controller State	Register Selected between TDI and TDO	TDO Driver
Test Logic Reset	BYPASS	Inactive
Run Test/Idle	BYPASS	Inactive
SELECT-DR Scan	**	Inactive
SELECT-IR Scan	INSTRUCTION	Inactive
Capture-IR	INSTRUCTION	Inactive
SHIFT-IR	INSTRUCTION	ACTIVE
Exit1-IR	INSTRUCTION	Inactive
PAUSE-IR	INSTRUCTION	Inactive
Exit2-IR	INSTRUCTION	Inactive
UPDATE-IR	INSTRUCTION	Inactive
Capture-DR	**	Inactive
SHIFT-DR	TEST DATA	ACTIVE
Exit1-DR	**	Inactive
PAUSE-DR	**	Inactive
Exit2-DR	**	Inactive
UPDATE-DR	**	Inactive

Note: ** = Data register selected depends on currently active instruction.

FEATURES OF THE TAP CONTROLLER

The TAP Controller will not be initialized by the operation of any system pin such as a system reset. The TAP Controller will be initialized into the Test Logic Reset state upon power-up. This requirement is intended to avoid bus signal contention upon system power-up by disabling the test logic which allows the system logic to operate normally and hence be controlled to avoid any contention. (The TAP Controller will return to the Test Logic Reset state after, at most, five clock cycles of TCK with TMS high; but the time required to enact that operation may not be sufficient to avoid contention.)

Note that the TAP Controller has been defined such that six of the sixteen states have the ability to maintain their state provided that TMS remains at the same value it had when entering the state. Those states include Test Logic Reset to hold off the test logic during normal system operation, Run Test/Idle to undertake multi-cycle self tests, SHIFT-DR and SHIFT-IR to maintain the data shifting process for an extended period, and PAUSE-DR and PAUSE-IR to halt the shifting process while some other activity is performed such as retrieving test data from additional memory. This feature is available in any/all states where multiple clock cycles may be required to achieve the desired outcome or where activity is to be halted but still provide the ability to make TCK a free-running clock.

III. BOUNDARY SCAN REGISTERS

INSTRUCTION REGISTER

The INSTRUCTION register permits specific commands to be shifted into the design to select a particular test data register and/or a specific test function. Additionally, the capture sequence of the INSTRUCTION register permits design specific data to be examined.

The INSTRUCTION register must be at least two bits long, the specific INSTRUCTION register included into the devices which reference this document is eight bits long, and the two least significant bits must capture the value "01". The significance of the two bit minimum length is two fold. First it permits the ability to supply unique codes for at least each of the three mandatory instructions required by the standard. Secondly, the bit value "01" in the least significant locations can be used to check the connectivity of the scan chain by forcing a bit toggle at each instruction during a scan of the INSTRUCTION registers. This technique not only assists in determining the correct connectivity of the scan chain about the board, but also assists in pin-pointing the location of any break in the scan chain.

All of National's SCAN Test Access Logic devices utilize an 8-bit instruction register. For the SCAN CMOS Test Access Logic devices, the 6 most significant bits which are loaded into the instruction register during the CAPTURE-IR state are used to provide a "pseudo ID code". The different codes captured into the INSTRUCTION register is a means of distinguishing the products in order to supply a method of evaluating the correct board placement of the products when an interrogation is performed through the scan chain only.

The captured "pseudo ID code" value is provided in each of the SCAN CMOS Test Access logic datasheets.

The SCAN ABT Test Access Logic devices include the IEEE 1149.1 optional ID CODE register and each device captures the same fixed value. This fixed value is the opcode for the SAMPLE/PRELOAD instruction, 1000001.

The order of scan through the INSTRUCTION register must be least-to-most; that is, the least significant bit is closest to TDO for a loaded instruction. During the SHIFT-IR state the instruction shifts one bit between TDI and TDO upon each rising edge of TCK and appears without inversion at TDO following the appropriate number of TCK cycles depending

on the fixed length of the INSTRUCTION register. A latched parallel output register accompanies each bit of the INSTRUCTION register such that the instruction can be updated or applied to the test logic simultaneously, rather than during the shift sequence. This latched parallel output changes upon the falling edge of TCK in the Update-IR state as well as upon the falling edge of TCK during the Test Logic Reset state. (It changes asynchronously upon the low assertion of the $\overline{TRST}$ input or upon power-up.)

Each instruction will identify a particular test data register to be connected between TDI and TDO when in the Shift-DR state along with defining any particular test actions to occur to that test data register and/or any others.

INSTRUCTION DEFINITIONS

The required instructions (see Table IV) include the BYPASS, EXTEST, and SAMPLE/PRELOAD instructions with optional instructions of HIGH-Z and CLAMP; and, for SCAN ABT only, the IDCODE. The additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT have also been incorporated into the SCAN ABT devices. The optional INTEST instruction was not incorporated because it adds a delay penalty to the system logic from gating that logic in order to provide controllability as well as observability. In the following descriptions each instruction will identify the test data register to be connected between TDI and TDO during the SHIFT-DR state, any restrictions on the binary codes used to implement the instruction, and what test data registers are used in undertaking the actions of the instruction.

1. **EXTEST.** This instruction allows circuitry external to the component package, typically the board interconnect, to be tested. Boundary-Scan register cells at the output pins are used to apply test stimuli, while those at the input pins capture test results. When this instruction is selected, the states of all signals on the system input pins will be loaded into the Boundary-Scan register upon the rising edge of TCK in the Capture-DR state and the contents of the Boundary-Scan register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-DR state. This instruction is mandatory under the guidelines of IEEE Standard 1149.1. The 000. . .0 instruction binary code must invoke the EXTEST instruction. During this instruction the Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state. Additional binary codes for this instruction are permitted.
2. **SAMPLE/PRELOAD.** This instruction allows a "snapshot" of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the Boundary-Scan SHIFT register prior to selection of another Boundary-Scan test instruction. During this instruction the Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state. When this instruction is selected, the states of all signals on the system pins will be loaded into the Boundary-Scan register upon the rising edge of TCK in the CAPTURE-DR state and the contents of the Boundary-Scan register will be loaded into the parallel output register included with the Boundary-Scan register bits upon the falling edge of TCK in the UPDATE-DR state.

   Note that by interfacing these two actions through the Exit1-DR state, the current state of the system pins can be captured into the Boundary-Scan register and stored into its parallel output registers for later application back onto those same pins. When the SAMPLE/PRELOAD instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. This instruction is mandatory under the guidelines of IEEE Standard 1149.1, but the binary code may be device specific.
3. **BYPASS.** This instruction allows rapid movement of test data to and from other components on a board that are required to perform test operations by selecting the BYPASS register, a single-bit shift-register stage, between TDI and TDO in the SHIFT-DR state to provide a minimum-length serial scan path. This instruction is mandatory under the guidelines of IEEE Standard 1149.1. The 111. . .1 instruction binary code must invoke the BYPASS instruction. This specific opcode, along with the requirement that an undriven TDI input produce a logic high value, is intended to load the BYPASS instruction during an instruction-scan cycle if the scan chain is broken. In such a case all instructions following the break in the scan chain will be loaded with the BYPASS instruction and hence have no impact upon the system's normal functional operation. Additional binary codes for this instruction are permitted. When the BYPASS instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. When the optional IDCODE register is not included, this instruction is loaded into the INSTRUCTION register in the Test Logic Reset state.

TABLE IV. Required and Optional Instructions Included

IEEE 1149.1	SCAN ABT	SCAN CMOS
Required	BYPASS	BYPASS
Required	EXTEST	EXTEST
Required	SAMPLE/PRELOAD	SAMPLE/PRELOAD
Optional	HIGH-Z	HIGH-Z
Optional	CLAMP	CLAMP
Optional	IDCODE	
Optional	SAMPLE-IN	
Optional	SAMPLE-OUT	
Optional	EXTEST-OUT	

4. **CLAMP.** This instruction allows fixed guarding values to be placed on signals that control the operation of logic not involved in the test, but does not require that the Boundary-Scan register be part of the serial scan path as in the EXTEST instruction. The contents of the Boundary-Scan register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-IR state for this instruction. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.
5. **HIGH-Z.** This instruction allows all of a components system outputs to be placed in an inactive drive state to permit its outputs to be safely backdriven during testing of other integrated circuits on the printed circuit board. All outputs of the device will become inactive even if during their normal system function they are two-state outputs. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.
6. **IDCODE.** (SCAN ABT and PSC110F only.) This instruction allows a blind interrogation of an identification code that is unique to this device type. During this instruction the IDCODE Register is connected between TDI and TDO in the SHIFT-DR state.
7. **SAMPLE-IN.** (SCAN ABT only.) This instruction is analogous to SAMPLE/PRELOAD but shortens the SCAN chain to include only the input and control pin cells (see Input Boundary-Scan register definition diagram in each datasheet). During this instruction only the Input Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state.
8. **SAMPLE-OUT.** (SCAN ABT only.) This instruction is analogous to SAMPLE/PRELOAD but shortens the SCAN chain to include only the output and internal TRI-STATE control cells (see Output Boundary-Scan register definition diagram in each datasheet). During this instruction only the Output Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state.
9. **EXTEST-OUT.** (SCAN ABT only.) This instruction is analogous to EXTEST but shortens the SCAN chain to include only the output and internal TRI-STATE control cells (see Output Boundary-Scan register definition diagram in each datasheet). During this instruction only the Output Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state.

Each of the previously defined instructions fully indicates which data registers may operate or interact with the system logic while the instruction is current. Test data registers that are not selected by the current instruction must be controlled such that they do not interfere with the system logic or the operation of the test data registers currently selected. While a given instruction may lead to operation of more than one test data register, only one test data register may be connected between TDI and TDO during the SHIFT-DR state for the given instruction.

BOUNDARY-SCAN REGISTER

The Boundary-Scan register permits testing of printed circuit board interconnects such as opens and shorts while also providing access to the components inputs and outputs when testing or monitoring its system logic. This register, as with all test data registers included in a 1149.1-compliant device, must be of fixed length. Data applied at the TDI input must appear without inversion at TDO during the SHIFT-DR state following the appropriate number of TCK cycles determined by the specific fixed length. This test data register will shift one stage toward TDO at each rising edge of TCK in the SHIFT-DR state when selected by the current instruction. Data will be parallel loaded into the Boundary-Scan register upon a rising edge of TCK in the Capture-DR state and the parallel register stages of the Boundary-Scan register will be latched upon the falling edge of TCK in the UPDATE-DR state provided that it is selected by the current instruction; otherwise, no change to its contents shall occur.

The shift register stages used in the make-up of the Boundary-Scan register may or may not be required to incorporate a parallel output register as well as its shift register stage. This requirement depends on the function of the system logic pin with which it is associated as well as the operational requirements of that pin during certain instructions defined for the device. The Input and Output Boundary-Scan cells demonstrate the parallel register stage, or lack thereof. The first cell can be used on system input pins where only observability of its logic state is necessary while the second scan cell can be used at system outputs where observability and controllability are required. Note that in the input scan cell there is no multiplexer directly in the data path while one does exist in the output scan cell. It is the logic gating of the data path that results in the performance penalty of the data path when controlling test logic is added. It is for this reason that the optional INTEST instruction was not included as one of the available features on the products which specifically reference this document. It was deemed unnecessary to pay the performance cost in exchange for the limited functional extension of controlling inputs as well.

If INTEST capability is desired, the system logic of the products referencing this document can be considered an extension of the EXTEST capability. All 1149.1-compliant devices require that the input and output data path scan cells be placed at logically equivalent locations to the system pin. As a result of that action the input/output buffers and voltage level translators are already tested as an extension of interconnect tests. If these interconnect tests are combined with the triggering of a 374 flip-flop clock input, as an example, the internal logic of the device can be evaluated as an extension of the EXTEST capability. Because the National SCAN products currently offered have easily manipulated

system logic, the 1149.1 user can logically extend the internal system logic to the EXTEST function. This feature is available during the EXTEST instructions for these products because the state of the outputs is captured along with the state of the inputs during the rising edge of TCK in the CAPTURE-DR state. Note that this is contrary to a recommendation of capturing fixed values on the outputs during EXTEST, but it provides for a feature that would otherwise not exist.

While these cells are sufficient to observe the logic state of the signal in which they are placed, they have a limitation in observing the activity of such a signal as in the specific case of a three-stated output. To determine the activity as well as the logic state of such an output, two such scan cells are required. One in the data signal path and another in the output enable signal path. By observing at both locations the drive activity and/or logic value can be inferred. In the case of a single output enable signal controlling more than one output data path, the output enable signal may be observable and controllable at a single location rather than at each specific output without loss of functional intent provided that the specific location retain control over all the data outputs in unison. This provision is included to reduce the hardware overhead as in the case of a device where such output enable signals are organized byte-wide.

The order of the required scan cells in the Boundary-Scan register is undefined by the 1149.1 Standard and hence can be device specific even if the system function of that device be identical to another 1149.1-compliant device. In other words, even if two identical system function devices are 1149.1-compliant there is no guarantee that such devices will be identical in the structure of the Boundary-Scan register.

A description of the Boundary Scan Register for each device is included in its datasheet.

Input Boundary-Scan Register (SCAN ABT only)

The Input Boundary-Scan register operates in a manner analogous to the full length Boundary-Scan register.

Output Boundary-Scan register (SCAN ABT only)

The Output Boundary-Scan register operates in a manner analogous to the full length Boundary-Scan register.

Please refer to the device datasheet for a description of its input and output Boundary-Scan Registers.

BYPASS REGISTER

The BYPASS register is also a test data register and therefore must comply with the definitions surrounding test data register operation; but its advantage is in its size, not necessarily in its function. The BYPASS register consists of a single shift register stage in order to shorten the board-level serial scan chain by bypassing some devices while accessing others. This feature is intended to reduce the software overhead in applying and retrieving serial test data by permitting a shortcut between TDI and TDO of any given integrated circuit in order to expedite access to others.

The BYPASS register must capture a logic low value upon the rising edge of TCK in the SHIFT-DR state provided that it is selected by the current instruction. This feature is designed to accompany those devices which incorporate the 32-bit device identification register. (The BYPASS register is a test data register whose least significant bit is a fixed logic high.) Upon an initial scan of the data registers connected across the board, all devices will either connect the BYPASS register or the optional device IDENTIFICATION register in its test data register scan path between TDI and TDO while in the SHIFT-DR state. (This condition is a result of power-up or a logic low assertion to $\overline{\text{TRST}}$ to initialize each 1149.1 device on board.) By shifting the data registers the retrieval of each logic zero indicates a BYPASS register connection until the first logic high is read. The logic high will be the framing bit of a device IDENTIFICATION register which would then indicate that the following thirty-one bits are identifiers to the specific device at that location of the scan chain. The requirement that the BYPASS register capture a logic low value is intended to form the background for the device IDENTIFICATION register framing bit. Additionally, the logic low value is opposite the value to be produced in the case of an undriven TDI input pin.

Device Identification Register

The device identification register is a 32-bit, read only register compliant with IEEE Std. 1149.1. When the IDCODE instruction is active, the identification register is loaded with a fixed, unique value upon leaving the Capture-DR state. The ID code register contains information pertaining to the device manufacturer, part number and revision. It is used to ensure the correct device is properly placed in the correct location within a boundary scan chain.

An identification (ID) register is included within the National SCAN ABT Test Access Logic devices. The specific ID register value is provided in the associated device datasheets.

Section 3

Device Description and Characteristics

Section 3 Contents

Device Description and Characteristics

Family Comparison Chart

Depending on system architecture and purpose, devices are selected to optimize system performance. National offers CMOS and BiCMOS SCAN families, and the comparison chart is provided to assist you with your selection criteria.

Speed, power, noise drive, etc. may weight differently in importance depending on whether the end system requires computing speed, low standby power, low EMI to meet FCC regulations or must meet any one of many bus standards.

BiCMOS and CMOS Family Comparison

Criteria		Significance	BICMOS	CMOS
Guaranteed Speed—t_{PLH} ns (A → B)		Faster system performance	6.5	8.5
Static Power I_{CCL} (Outputs Low)		Lower quiescent supply current, less power consumption, and less cooling required	65 mA	0.8 mA
Guaranteed Dynamic Power I_{CCD} (mA/MHz)		Lower system power consumption under heavier loading conditions	0.2 (Note 3)	not specified
Ground Bounce V_{OLP} (5V, 25°C)		Less data disruption, especially when switching multiple outputs at one time	not specified	1.5
Dynamic Threshold (5V, 25°C)	V_{ILD}	Less data disruption, especially when connected to a bus	0.8	0.8
	V_{IHD}		2.0	2.0
Packaging		Compatible with 16-bit wide pinout	SSOP	SSOP
Capacitance	C_{IN} (pF)	Lower capacitance means less bus loading, notwithstanding frequency	5.9	4.0
	$C_{I/O}$ (pF)		13.7	20
Output Drive (mA)	I_{OL}		15	64
	I_{OH}		−32	−32
ESD (Note 4)		Easier handling	>2000V	>2000V

NG = Not Guaranteed; NA = Not Available; NS = Not Specified

Assumptions: Device is SCAN18245T CMOS and SCAN182245A BiCMOS

Note 1: V_{OLP} is measured on '244 function.

Note 2: Specified with 8 outputs switching and no load.

Note 3: I_{CCD} measured 1 bit toggling, 0V to 5V, 50% duty cycle, outputs loaded with 50 pF, no resistor.

Note 4: Typical values for HBM ESD.

SCAN ABT Test Access Logic

When these functions are added to the card edge going into the backplane, users gain these benefits:

— Live insertion

— Removal of boards without having to power down the system

This saves time and eliminates those unwelcome sparks!

Here are other SCAN ABT features:

— 25Ω series resistors on the outputs reduce ringing (noise) and eliminate the need for an external "damping" resistor. In the past, this was used to reduce noise on CMOS or FCT products.

— SCAN ABT will power up in TRI-STATE®. Beyond allowing live insertion and board removal, it enables system power partitioning by electronically switching them off-line to save on power. This is particularly beneficial in remote locations that experience power shortages.

— SCAN ABT has reduced power during power-up and power-down TRI-STATE. This reduces the loading on the bus to which it is attached, taking less time to charge up all of the capacitance on the circuit using SCAN ABT, and allowing the bus to run faster.

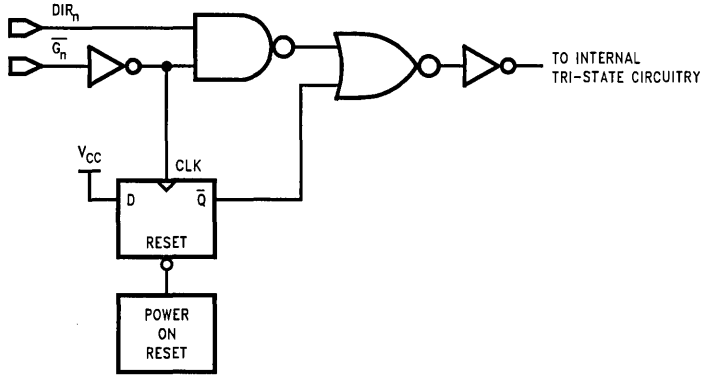
For more information on power-up and power-down characteristics refer to Application Note AN-881, *"Design Considerations for Fault Tolerant Backplanes,"* found in Section 7.

SCAN ABT Live Insertion and Power Cycling Characteristics

SCAN ABT is intended to serve in live insertion backplane applications. It provides 2nd Level Isolation[1] which indicates that while external circuitry to control the output enable pin is unnecessary, there may be a need to implement differential length backplane connector pins for V_{CC} and GND. As well, pre-bias circuitry for backplane pins may be necessary to avoid capacitive loading effects during live insertion.

SCAN ABT provides control of output enable pins during power cycling via the circuit in *Figure 1*. It essentially controls the $\overline{G_n}$ pin until V_{CC} reaches a known level.

During *power-up*, when V_{CC} ramps through the 0.0V to 0.7V range, all internal device circuitry is inactive, leaving output and I/O pins of the device in high impedance. From approximately 0.8V to 1.8V V_{CC}, the Power-On-Reset circuitry, (POR), in *Figure 1* becomes active and maintains device high impedance mode. The POR does this by providing a low from its output that resets the flip-flop The output, $\overline{Q}$, of the flip-flop then goes high and disables the NOR gate from an incidental low input on the $\overline{G_n}$ pin. After 1.8V V_{CC}, the POR circuitry becomes inactive and ceases to control the flip-flop. To bring the device out of high impedance, the $\overline{G_n}$ input must receive an inactive-to-active transition, a high-to-low transition on $\overline{G_n}$ in this case to change the state of the flip-flop. With a low on the $\overline{Q}$ output of the flip-flop, the NOR gate is free to allow propagation of a $\overline{G_n}$ signal.



TL/F/12133–2

FIGURE 1

[1]Section 7, *Design Considerations for Fault Tolerant Backplanes,* Application Note AN-881.

SCAN ABT Live Insertion and Power Cycling Characteristics (Continued)

During *power-down*, the Power-On-Reset circuitry will become active and reset the flip-flop at approximately 1.8V V_{CC}. Again, the $\overline{Q}$ output of the flip-flop returns to a high and disables the NOR gate from inputs from the $\overline{G_n}$ pin. The device will then remain in high impedance for the remaining ramp down from 1.8V to 0.0V V_{CC}.

Some suggestions to help the designer with live insertion issues:

- The $\overline{G_n}$ pin can float during power-up until the Power-On-Reset circuitry becomes inactive.
- The $\overline{G_n}$ pin can float on power-down only after the Power-On-Reset has become active.

The description of the functionality of the Power-On-Reset circuitry can best be described in the diagram of *Figure 2*.

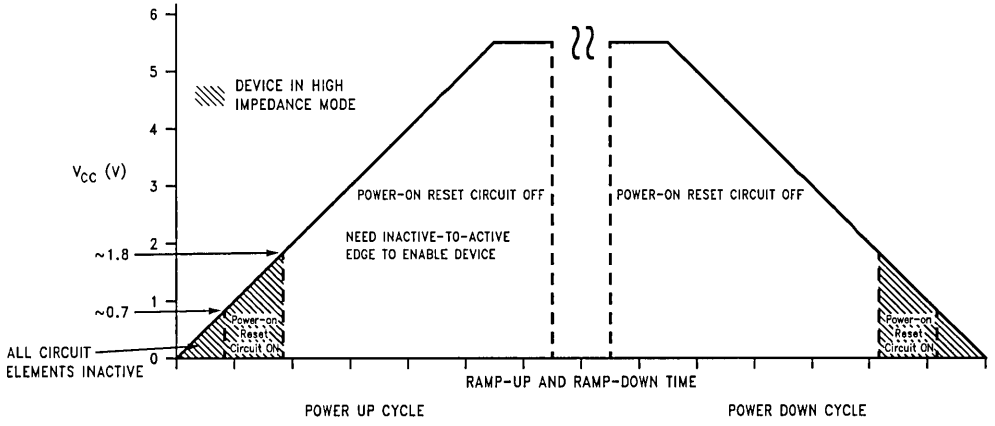


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FIGURE 2. SCAN ABT Includes Additional Power-On Reset Circuitry Not Otherwise Included in ABT Devices

ABT Circuit and Design Architecture

SCAN ABT performs as ABT devices, except as where noted.

The circuitry for an ABT non-inverting Buffer with TRI-STATE control logic is shown in *Figure 3*. Robust bipolar components form the dual rail ESD protection networks for both input and output structures. The Q6 and D6 ESD circuits provide protection to the V_{CC} rail and have a high enough breakdown voltage rating to remain high impedance (I_{ZZ} < 100 μA) during powered-down applications. The Schottky transistors Q5, Q7 and Q8 provide protection to the Ground rail and double functionally as highly conductive undershoot clamps.

The TRI-STATE output structure is formed with Bipolar components to produce high drive (I_{OL} = 64 mA; I_{OH} = −32 mA) and high speed TTL compatible logic swings. The pull-up stage utilizes cascaded emitter followers Q3 and Q4 to provide high source current drive for the charging of capacitive loads. The no-load TTL compatible V_{OH} level is one forward-biased V_{BE} (Q3) drop and one forward-biased V_{FD} Schottky diode (D4) drop below the V_{CC} rail yielding typical 3.8V V_{OH} at 5V V_{CC}, 25°C and 10 μA source current. The ON source impedance of this pull-up stage is typically less than 10Ω for source currents between −5 mA to −40 mA at 25°C. This initial low impedance turn-on characteristic allows the pull-up stage to easily provide a V_{OH} level of 2V minimum at I_{OH} source current of −32 mA over the operating V_{CC} and temperature ranges. At 25°C and source currents above −50 mA, the pull-up stage becomes limited by voltage drop across the R_{IOS} resistor and the effective source impedance becomes 25Ω typically. Schottky diodes D3, D4 and D5 also provide blocking to insure that the pull-up stage remains high impedance during power down applications.

When the output is enabled by a logic low on the $\overline{OE}$ input and a logic high is on the Data input, the base of Q3 is driven to the V_{CC} rail by the CMOS inverter in the data path. The open drain CMOS NAND gate is logic high-open (non-conducting) and allows the base of Q4 to be driven ON by Q3. The CMOS NOR gate goes low turning Q1 OFF and turning ON the CMOS AC/DC Miller Killer circuitry which grounds the base of Q2, quickly turning it OFF. This circuitry provides an active shunt for any charge coupled by the Miller Effect of the Q2 collector-base capacitance during the low to high output transition. Use of this active circuitry improves output rise time and serves to reduce simultaneous conduction of pull-up and pull-down stages during LH transitions. The AC/DC Miller Killer circuit is also active when the output goes to TRI-STATE to prevent Q2 base injection by the LH transitions of other outputs on a bus, therefore dynamic bus loading will be capacitive only.

Power Down Miller Killer circuitry at the base of Q2 is inactive when V_{CC} is applied. When V_{CC} is powered down, the Power Down Miller Killer circuitry provides an active shunt to transient energy coupled to the Q2 base by its collector base capacitance. This prevents momentary turn-on of Q2 during LH transitions in partial power down bus applications and maintains the powered off output as only a Hi-Z light capacitive load (I_{ZZ} < 100 μA) to the bus.

Note that Q1 drives only the Q2 pull-down stage and does not function as the Phase Splitter driver typical of TTL logic. The pull-up stage is controlled by CMOS logic independent of Q1. This feature allows the input threshold voltages for the CMOS logic driving the pull-up stage to be set independent of the logic driving the pull-down stage.

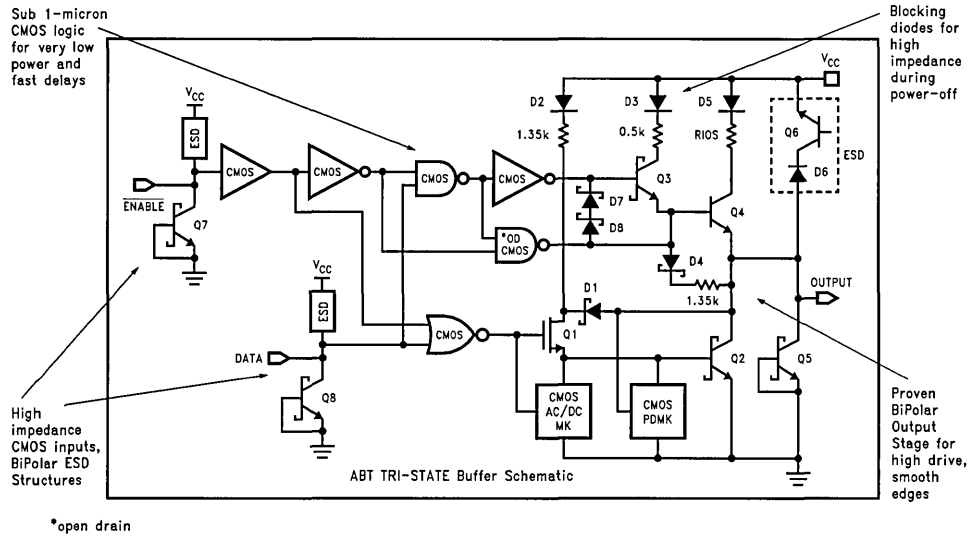

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FIGURE 3. Basic ABT TRI-STATE Buffer Schematic

ABT Circuit and Design Architecture (Continued)

The transfer function for the non-inverting ABT Buffer shown in *Figure 4* indicates that the data input switching threshold for the pull-down stage is approximately 200 mV lower than the pull-up stage. As the Data input is swept from logic LOW to logic HIGH, the output switches from active LOW to high impedance at an input threshold of about 1.3V at 25°C and a V_{CC} of 5.0V. When the input reaches about 1.5V, the output switches from high impedance to HIGH. This design feature serves to reduce simultaneous conduction of the stages during switching. Also, the 200 mV offset in Data input switching thresholds acts like hysteresis and causes the buffer to be very tolerant of slow data input edge rates, i.e., edge rates slower than 10 ns/V can easily be tolerated without output oscillation. The switching threshold is proportional to V_{CC} as indicated in *Figure 5* and is quite stable as a function of temperature as indicated by *Figure 6.*

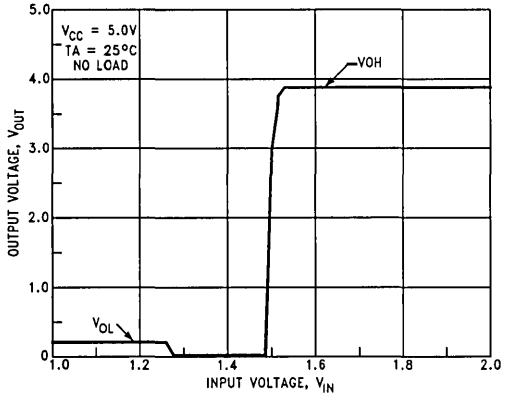

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FIGURE 4. Buffer Transfer Function @ Room Temperature V_{CC} = 5V, T_A = 25°C, No Load

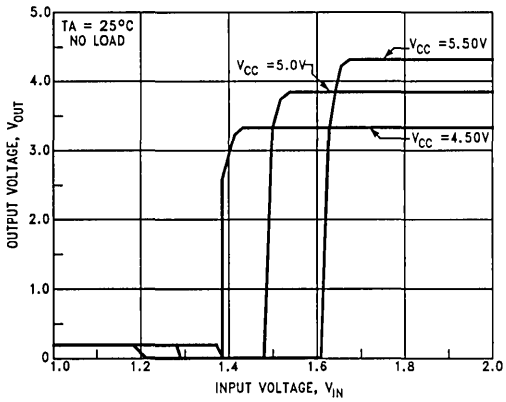

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FIGURE 5. Transfer Function vs V_{CC} T_A = 25°C, No Load

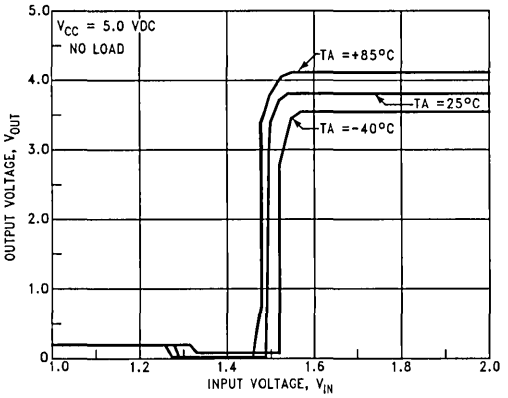

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FIGURE 6. Transfer Function vs Temperature V_{CC} = 5V DC, No Load

With the output enabled by a LOW on the $\overline{OE}$ input, a LOW on the Data input forces active LOWS on both the CMOS inverter and the open drain CMOS NAND gate outputs, which then simultaneously turn OFF Q3 and Q4. The CMOS NOR gate output goes HIGH, turning the AC/DC Miller Killer circuitry OFF and Q1 ON to drive Q2 ON. Q2 is designed to easily sink 64 mA I_{OL}, at V_{OL} < 0.55V. During HL output transitions, Schottky diode D1 assists the pull-down stage in providing a low impedance discharge path for the output load capacitance. As the stage turns on, part of the charge on the output load passes through D1 and Q1 to momentarily increase the base drive to Q2 and increase Q2's current sink capability. See output characteristics in *Figure 7*, I_{OL} vs V_{OL}.

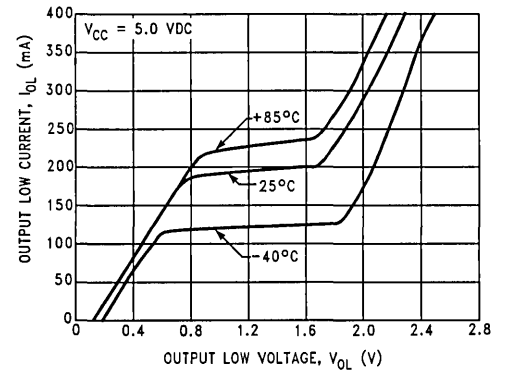

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FIGURE 7. Output Low Characteristics V_{CC} = 5V DC

ABT Circuit and Design Architecture (Continued)

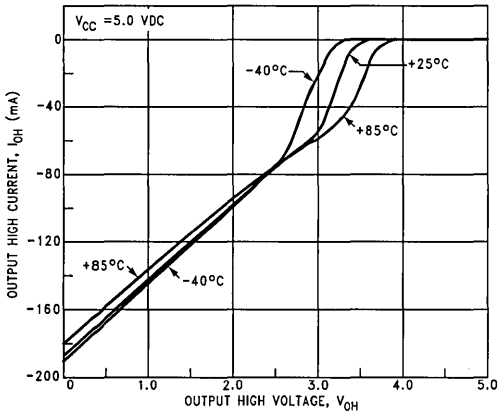

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FIGURE 8. Output High Characteristics
V_{CC} = 5V DC

When the output is disabled by a HIGH on the $\overline{OE}$ input, the enable CMOS logic quickly overrides the Data path logic and cuts off drive to whichever stage is ON. In the case of an LZ transition, the CMOS NOR gate is driven LOW turning OFF Q1 and turning ON the AC/DC Miller Killer circuitry to insure Q2 is quickly turned off. In the case of a HZ transition, the CMOS inverter goes hard LOW to turn off Q3 and quickly discharge the base of Q4 through Schottky diodes D7 and D8. The effect of disable time (t_{PLZ}, t_{PHZ}) being typically faster than enable time (t_{PZL}, t_{PZH}) inherently helps avoid bus contention.

Since the CMOS Enable logic remains active to V_{CC}'s well below 2V, high impedance control can be maintained to V_{CC} voltages below the turn-on V_{CC} thresholds of the Bipolar output stage. This insures the capability for glitch free power ON/OFF high impedance outputs with the provision that the $\overline{OE}$ input is maintained logic HIGH at or greater than the data sheet specified 2.0V minimum V_{IH} during the V_{CC} power ramp. However, since the CMOS logic switching threshold varies proportional to V_{CC}, a practical worst case $\overline{OE}$ logic high of 2.0V or 50% of V_{CC}, will maintain the power ON/OFF TRI-STATE condition during the V_{CC} transition.

ABT is designed to be tolerant of controlled live insertion at the PCB level. Controlled means that the insertion or removal methodology is accomplished in such a way that power to the PCB is applied in a preferred sequence and that control signals are provided to the PCB also in the preferred sequence such that output control is asserted to prevent contention of outputs attached to a bus during the power up or down sequence.

Tolerant means that ABT is designed and guaranteed to behave in a predictable manner during controlled PCB live insertion in systems requiring fault-tolerant or noninterruptable applications. Additionally, ABT has features which facilitate design of systems which must utilize power partitioning for redundant circuitry or for powering saving of inactive circuits.

All ABT input, output, and I/O pins are protected with robust Bipolar components with respect to both V_{CC} and Ground rails. This circuitry is designed to withstand 2000V (Human Body Model) and also to provide clamping action for voltage undershoot while preserving low capacitive loading of the pin. The clamping action by the undershoot clamp begins aggressively at voltages more negative than −0.5V relative to Ground, but this clamp remains non-conductive at voltages up to 7V. Relative to the V_{CC} rail, the ESD circuitry begins clamping only at voltages greater than 5.5V above V_{CC}. These ESD circuits remain high impedance and non-conductive for applied input or output voltages between −0.4V to 5.5V with V_{CC} = 0V to 5.5V.

ABT CMOS input stages are Hi-Z with or without V_{CC} applied. The I_{IL}, I_{IH}, and I_{BVI} datasheet specification guarantees high DC impedance for inputs with V_{CC} applied. The V_{ID} specification guarantees Hi-Z inputs with V_{CC} = 0V.

High impedance output and I/O pins are capable of maintaining Hi-Z status with V_{CC} = 0 and during the application or removal of V_{CC}. The ABT data sheet parameters I_{OZH} and I_{OZL} guarantee < 50 μA output leakage for applied V_{OUT} voltages of 2.7V or 0.5V at any V_{CC} between 5.5V and 0V with the output disabled and with the appropriate logic input voltage maintained on the $\overline{OE}$ input pin. An additional I_{ZZ} bus drainage specification guarantees < 100 μA output leakage at V_{OUT} = 5.5V with V_{CC} = 0V. Therefore, ABT outputs are guaranteed to remain glitch-free during the power cycle and at power down V_{CC} = 0V. Refer to Application Section for a more detailed discussion of live insertion and powerup/down TRI-STATE capabilities of ABT.

Threshold and Noise Margin

Figure 9 describes the input signal voltage levels for use with ABT products. The AC testing input levels follow industry convention which require 0.0V for a logic LOW and 3.0V level for a logic HIGH. DC input levels are typically 0.0V to V_{IL}, and high input levels are typically V_{IH} to V_{CC}. DC testing uses a combination of threshold and hard levels to assure datasheet guarantees. Input threshold levels are usually guaranteed through V_{OL} and V_{OH} tests.

High level noise immunity is the difference between V_{OH} and V_{IH} and low level noise immunity is the difference between V_{IL} and V_{OL}. Noise-free V_{IH} or V_{IL} levels should not induce a switch on the appropriate output of an ABT device. When testing in an automated environment, extreme caution should be taken to ensure that input levels plus noise do not go into the transition region.

Dynamic System Power Dissipation

One of several advantages to using BiCMOS logic is its low power when compared to bipolar technologies. As well, it has reduced dynamic output power because of the reduced output swing in comparison to CMOS devices. In the static or quiescent high state, SCAN ABT will consume power like a pure CMOS device, and in the quiescent low state all power goes to driving the bipolar output pull-down transistor.

Total power consumption under AC conditions comes from three sources; quiescent power, internal dynamic power, and output dynamic power.

In other words: $P_{TOTAL} = P_{DQ} + P_{DINT} + P_{DOUT}$

Where:

P_{TOTAL} = Total Power Dissipation
P_{DQ} = Quiescent Power Dissipation
P_{DINT} = Internal Dynamic Power Dissipation
P_{DOUT} = Output Power Dissipation

First the Quiescent power can be derived from the following equation.

$$P_{DQ} = \left[\frac{I_{CCL}}{N} * N_{QOL} * V_{CC}\right] + \left[D_{ICC} * N_{QIH} * V_{CC}\right] + \left[\frac{I_{CCH}}{N} * N_{QOH} * V_{CC}\right]$$

Where:

P_{DQ} = Quiescent Power Dissipation
I_{CCH} = Quiescent Power Supply Current with All Outputs High
I_{CCL} = Quiescent Power Supply Current with All Outputs Low
N_{QOL} = Number of Quiescent Outputs Low
N_{QOH} = Number of Quiescent Outputs High
N_{QIH} = Number of Quiescent Inputs High
N = Number of Active Outputs
DI_{CC} = Power Supply Current for Input with V_{IN} other than V_{CC}

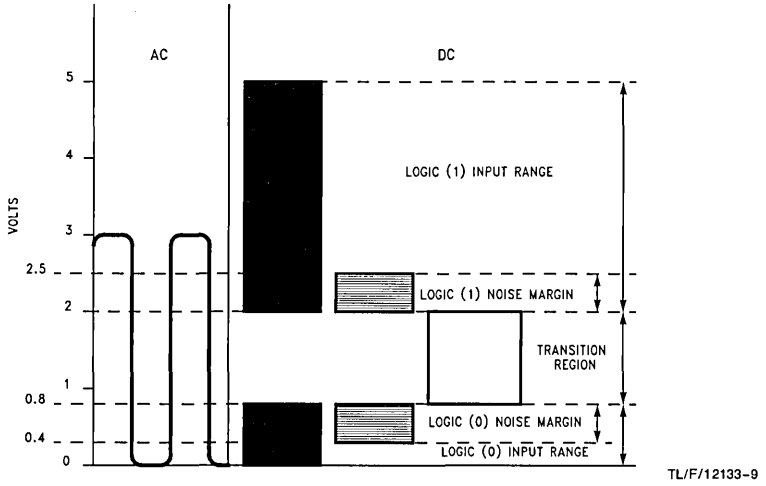

FIGURE 9

Dynamic System Power Dissipation (Continued)

Secondly, a SCAN ABT device will dissipate power internally by charging and discharging internal capacitiance. The following equation takes into account the duty cycle of inputs and outputs and current due to the internal switching of capacitances.

$$P_{DINT} = [(DI_{CC}*DH*NS)*V_{DD}] + \left[\left(\frac{I_{CCL}}{N}*NS*DL\right)*V_{CC}\right] + [(I_{CCD}*f*NS)*V_{CC}]$$

Where:

P_{DINT} = Internal Dynamic Power Dissipation

V_{CC} = Power Supply Voltage

DI_{CC} = Power Supply Current for Input with V_{IN} other than V_{CC} (For example, a typical TTL input voltage is considered to be 3.4V)

Note: The farther away an input (V_{IN}) is from threshold (1.5V), the less power supply current the IC will consume.

N = Number of Active Outputs

DH = Duty Cycle for Switching Inputs High

DL = Duty Cycle for Switching Outputs Low

I_{CCL} = Data book specification for power supply current with all outputs low

I_{CCD} = Power consumption coefficient (mA/MHz) for 1-bit toggling

f = Frequency of Outputs

NS = Number of Outputs Switching

Finally, at high frequencies a significant amount of current is consumed by a device to drive its output load. SCAN ABT has an advantage here because of its reduced output swing compared to CMOS devices. For a simple case, if we assume only capacitive components to the load, we can use the following equation.

$$P_{OUT} = [C_L * VS * f] * V_{CC}$$

Where:

P_{DOUT} = Output Power Dissipation

C_L = Load Capacitance

VS = Output Voltage Swing

f = Output Operating Frequency

V_{CC} = Power Supply Voltage

Take for an example a SCAN182244A with all 18 outputs switching at 16 MHz. How much power would be consumed by the IC in this case?

Assumptions:

1. V_{CC} = 5V
2. The data and control inputs are being driven with 0V and 3.4V voltages for logic levels.
3. Data input frequency = 16 MHz @ 50% duty cycle.
4. C_L = 50 pF
5. There are no DC loads on the outputs, i.e., outputs are either unterminated or terminated with an AC shunt termination.
6. Since the output high voltage is produced by a Darlington transistor pair, the output voltage swing will be assumed to be V_{CC} − 1.6V or 5.0 − 1.6V = 3.4V. Therefore VS = 3.4V with V_{CC} = 5.0V.

For quiescent current, all data inputs and outputs are switching leaving only the 2 $\overline{OE}$ inputs static low.

$$P_{DQ} = \left[\frac{I_{CCL}}{N}*N_{QOL}*V_{CC}\right] + [DI_{CC}*N_{QIH}*V_{CC}] + \left[\frac{I_{CCH}}{N}*N_{QOH}*V_{CC}\right]$$

$$= 0 + 0 + 0 = 0$$

Internal Dynamic Current

$$P_{DINT} = [(DI_{CC}*NS*DH)*V_{DD}] + [(\frac{I_{CCL}}{N}*NS*DL)*V_{CC}] + [(I_{CCD}*f*NS)*V_{CC}]$$

$$P_{DINT} = [(2.5e-3*18*0.5)*5.0] + [(\frac{30e-3}{18}*8*0.5)*5.0] + [(0.1*16*18)*5.0]$$

$$= 5.60 + 1.66 + 144$$

$$= 151.3 \text{ mW}$$

Finally the Output Current

$$P_{OUT} = [C_L * VS * f] * V_{CC}$$

$$P_{OUT} = [50.e-12*3.4V*16e6] * 5.0$$

$$= [2.72e-3]*5$$

$$= 13.5 \text{ mW}$$

$$P_{TOTAL} = P_{DQ} + P_{DINT} + P_{DOUT}$$

$$= 0 + 151.3 \text{ mW} + 13.5 \text{ mW}$$

$$P_{TOTAL} = 164.8 \text{ mW}$$

ABT Process Characteristics

PROCESS CHARACTERISTICS

National's 1.0 μm BCT process combines bipolar and CMOS transistors in a single process to achieve high speed, high drive characteristics while maintaining low tri-state power and the ability to control noise.

National's 1.0 μm BCT process provides a suitable platform for migration to higher performance levels with minor technology enhancements planned for the near future. In its present form, the technology supports Interface, Digital, Bus and Telecom products from National Semiconductor.

PROCESS FEATURES

- 18 masking layers using stepper lithography
- 100% ion implantation utilized for dopant placement
- Localized retrograde wells tailored for high performance
- Optimized recessed and field isolation sequence for CMOS/bipolar
- NMOS LDD (Lightly Doped Drain), PMOS Halo architecture
- 150Å gate oxide
- Self aligned bipolar contact set utilizing minimum geometries
- Localized retrograde sub-emitter collector
- Advanced planarization on all topographies
- PtSi Schottky diodes, all contacts use platinum for resistance reduction
- Barrier metal of TiW
- Dual layer metal of Al-Cu 0.3% for long term reliability
- Metal pitch of 3.5 microns

PROCESS FLOW

1.0	Buried Layer
2.0	P-Well
3.0	N-Well
4.0	Isolation
5.0	Sink
6.0	Active
7.0	Active Strip
8.0	Poly
9.0	Base
10.0	Bipolar Contact
11.0	Emitter
12.0	P+ Source/Drain
13.0	N+ Source/Drain
14.0	Contact
15.0	Metal 1
16.0	Via
17.0	Metal 2
18.0	Passivation

PROCESS PARAMETERS

- Bipolar Performance: 10 GHz Ft with gains greater than 100
- CMOS Performance: 0.5 μm min Leff
- Platinum Schottky diodes for TTL
- Typical ESD Performance: >2000V, Human Body Method
- Robust latch-up and punch-through protection with retrograde wells
- Advanced interconnect supports superior temperature cycle performance

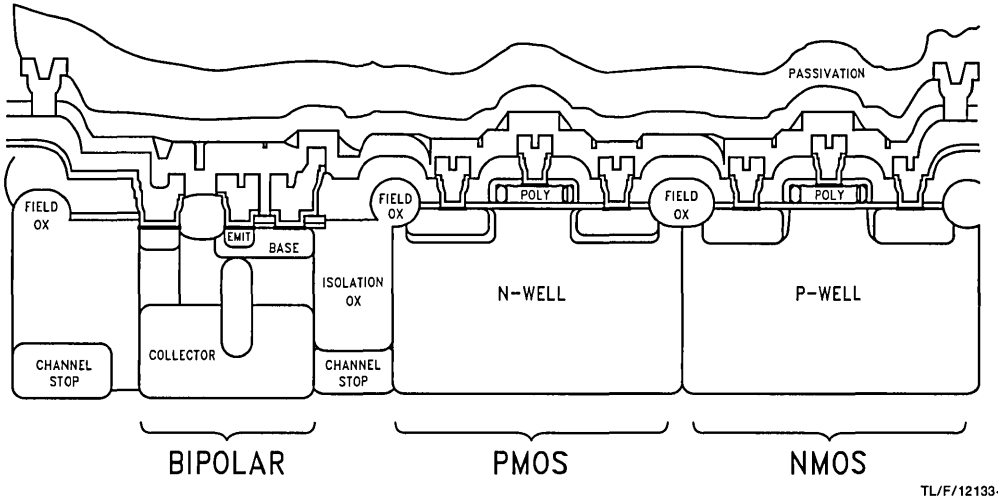

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FIGURE 10. 1.0 μm BCT Process Cross Section

SCAN CMOS Test Access Logic

SCAN CMOS features low power consumption. Products are used in board test by surrounding clusters of non-boundary scan devices to create a fully 1149.1 compliant board. SCAN CMOS provides adequate drive and buffering for microprocessors, too. For more information on Advanced CMOS devices, refer to the FACT Databook.

SCAN CMOS logic is manufactured on a 1.3 μm process and offers a good combination of high speed, low power dissipation, high noise immunity, wide fanout capability and high reliability.

Characteristics

Meets or Exceeds JEDEC Standards for 74ACXX

Family

High Performance Outputs
- — Common Output Structure
- — Output Sink/Source Current of −24/48 mA
- — Transmission Line Driving 50Ω (Commercial)/75Ω (Military) Guaranteed

Temperature Range

— Commercial	−40°C to +85°C
— Military	−55°C to +125°C

Improved ESD Protection Network

High Current Latch-Up Immunity

Patented Noise Suppression Circuitry

Noise Immunity

The DC noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The input threshold of a device and the output voltage, $|V_{IL} - V_{OL}|/|V_{IH} - V_{OH}|$ at 4.5V V_{DD}, for SCAN CMOS is 1.25V/1.25V.

Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of SCAN CMOS.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture or Equivalent
Tektronics Model 7854 Oscilloscope or Equivalent

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{DD} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3V HIGH. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.

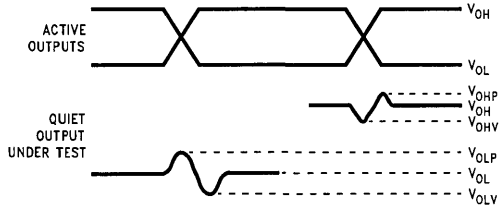

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FIGURE 11. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

- Measure V_{OLP} and V_{OLV} on the quiet output LOW during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output HIGH during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

Noise Characteristics (Continued)

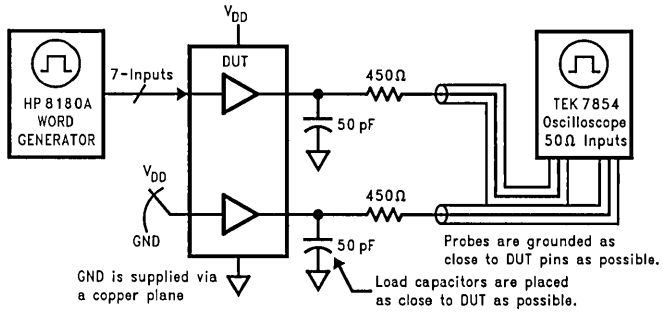

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FIGURE 12. Simultaneous Switching Test Circuit

Output Characteristics

All SCAN CMOS outputs are buffered to ensure consistent output voltage and current specifications. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All SCAN CMOS devices are guaranteed to source 48 mA and sink −24 mA. Commercial devices are capable of driving 50Ω transmission lines.

Circuit Characteristics

POWER DISSIPATION

One advantage to using CMOS logic is its extremely low power consumption. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Total power dissipation of SCAN CMOS device under AC conditions is a function of three basic sources, quiescent power, internal dynamic power, and output dynamic power dissipation.

Firstly, a SCAN CMOS device will dissipate power in the quiescent or static condition. This can be calculated by using the formula: (Note: In many datasheets I_{DD}, ΔI_{DD}, I_{DDT}, and V_{DD} are referred to as I_{CC}, ΔI_{CC}, I_{CCT}, and V_{CC}, respectively. There are no differences.)

Eq. 1 $PD_Q = I_{DD} \bullet V_{DD}$

PD_Q = Quiescent Power Dissipation
I_{DD} = Quiescent Power Supply Current Drain
V_{DD} = Power Supply Voltage

Secondly, a SCAN CMOS device will dissipate power dynamically by charging and discharging internal capacitance. This can be calculated by using the following formula:

Eq. 2.

$$PD_{INT} = [(I_{DDT} \bullet D_H \bullet N_T) \bullet V_{DD}] + [(C_{PD} \bullet V_S \bullet f) \bullet V_{DD}]$$

PD_{INT} = Internal Dynamic Power Dissipation
I_{DDT} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs HIGH
N_T = Number of TTL Inputs at D_H
V_{DD} = Power Supply Voltage
C_{PD} = Device Power Dissipation Capacitance
V_S = Output Voltage Swing
f = Internal Frequency of Operation

C_{PD} values are specified for each device and are measured per JEDEC standards as described in this section. On device data sheets, C_{PD} is a typical value and is given either for the package or for the individual stages with the device. V_S and V_{DD} are the same value and can be replaced by V_{DD}^2 in the formula.

Thirdly, a SCAN CMOS device will dissipate power dynamically by charging and discharging any load capacitance. This can be calculated by using the following formula:

Eq. 3 $PD_{OUT} = (C_L \bullet V_S \bullet f) \bullet V_{DD}$

PD_{OUT} = Output Power Dissipation
C_L = Load Capacitance
V_S = Output Voltage Swing
f = Output Operating Frequency
V_{DD} = Power Supply Voltage

Circuit Characteristics (Continued)

In many cases the output frequency is the same as the internal operation frequency. Also V_S is similar to V_{DD} and can be replaced by V_{DD}^2.

The total device power dissipation is the sum of the quiescent power and all of the dynamic power dissipation. This is best described as:

Eq. 4 $PD_{TOTAL} = PD_Q + PD_{DYNAMIC}$ or
$PD_{TOTAL} = PD_Q + PD_{INT} + PD_{OUT}$

The following is an exercise in calculating total dynamic I_{DD} for SCAN CMOS. The device used as an example is the SCAN18245T. Static I_{DD}, I_{DDT} and C_{PD} numbers can be found in the datasheet. I_{DD} numbers used will be worst-case commercial guarantees. Room temperature power will be less. These are approximate worst-case calculations.

The following assumptions have been made:

1. I_{DD} will be calculated per input/output (as per JEDEC C_{PD} calculations). The total for the SCAN18245T will be the calculated $I_{DD} \times 18$.
2. Worst case conditions and JEDEC would require that the data is being toggled at the clock frequency in order to change the outputs at the maximum rate (½ CP).
3. The data and clock input signals are derived from TTL level drivers (0V to 3.0V swing) at 50% duty cycle.
4. The clock frequency is 16 MHz.
5. I_{DD} will be calculated for $C_L = 50$ pF.
6. $V_{DD} = 5V$.
7. Total POWER dissipation can be obtained by multiplying total I_{DD} by V_{DD} (5.0V).
8. Quiescent I_{DD} will be neglected in the total I_{DD} calculation because it is 1000 times less than dynamic I_{DD}.
9. There is no DC load on the outputs, i.e. outputs are either unterminated or terminated with series or AC shunt termination.

The I_{DD} calculations are as follows:

I_{DD} Total = Input I_{DD} + Internal Switching I_{DD} + Output Switching (AC load) I_{DD}

Input I_{DD} = (I_{DDT}) × (number of TTL inputs) × (Duty Cycle)
= $(2 \times 10^{-3}) \times (1) \times (0.50)$
= 1.0 mA per input being toggled at TTL levels

Internal I_{DD} = $(V_{SWING}) \times (C_{PD}) \times$ (CP freq)
= $(5.0) \times (41 \times 10^{-12}) \times (16 \times 10^{+6})$
= 3.28 per mA per input being toggled by CP

Output I_{DD} = $(V_{SWING} \times (C_L) \times$ (Q freq)
C_L = 50 pF
= $(5.0) \times (50 \times 10^{-12}) \times (8 \times 10^{+6})$
= 2 mA per output toggled at ½ CP

Adding Input, Internal and Output I_{DD} together and multiplying by 18 I/O per SCAN18245T, the approximate worst-case I_{DD} calculations are as follows:

$C_L = 50$ pF I_{DD} total = 100.48 mA or 502.4 mW* at a CP of 16 MHz

(*Power is obtained by multiplying I_{DD} by V_{DD})

Section 4

Loading Specifications, Waveforms, Quality and Reliability

Section 4 Contents

Loading Specifications, Waveforms, Quality and Reliability

Definition of Terms

DC Characteristics

Currents: Positive current is defined as conventional current flow into a device. Negative current is defined as current flow out of a device. All current limits are specified as absolute values.

Voltages: All voltages are referenced to the ground pin. All voltage limits are specified as absolute values.

I_{BVI} Input HIGH Current (Breakdown Test). The current flowing into an input when a specified Absolute MAX HIGH voltage is applied to that input.

I_{BVIT} I/O Pin HIGH Current (Breakdown Test) The current flowing into a disabled (output is high impedance) I/O pin when a specified Absolute MAX HIGH voltage is applied to that I/O pin.

I_{CEX} Output HIGH Leakage Current. The current flowing into a HIGH output due to the application of a specified HIGH voltage to that output.

I_{CCH} The current flowing into the V_{CC} supply terminal when the outputs are in the HIGH state.

I_{CCL} The current flowing into the V_{CC} supply terminal when the outputs are in the LOW state.

I_{CCT} Additional I_{CC} due to TTL HIGH levels forced on CMOS inputs.

I_{CCZ} The current flowing into the V_{CC} supply terminal when the outputs are disabled (high impedance).

I_{IL} Input LOW Current. The current flowing out of an input when a specified LOW voltage is applied to that input.

I_{IH} Input HIGH Current. The current flowing into an input when a specified HIGH voltage is applied to that input.

I_{OH} Output HIGH Current. The current flowing out of an output which is in the HIGH state.

I_{OL} Output LOW Current. The current flowing into an output which is in the LOW state.

I_{OS} Output Short Circuit Current. The current flowing out of an output in the HIGH state when that output is shorted to ground (or other specified potential).

I_{OZL} Output OFF current (LOW). The current flowing out of a disabled TRI-STATE® output when a specified LOW voltage is applied to that output.

I_{OZH} Output OFF current (HIGH). The current flowing into a disabled TRI-STATE output when a specified HIGH voltage is applied to that output.

I_{ZZ} Bus Drainage. The current flowing into an output or I/O pin when a specified HIGH level is applied to the output or I/O pin of a power-down device.

V_{CC} Supply Voltage. The range of power supply voltages over which the device is guaranteed to operate.

V_{CD} Input Clamp Diode Voltage. The voltage on an input (−) when a specified current is pulled from that input.

V_{ID} Input Breakdown Voltage. The voltage on an input of a powered-down device when a specified current is forced into that input.

V_{IH} Input HIGH Voltage. The minimum input voltage that is recognized as a DC HIGH-level.

V_{IHD} Dynamic Input HIGH Voltage. The minimum input voltage that is recognized as a HIGH-level during a Multiple Output Switching (MOS) operation.

V_{IL} Input LOW Voltage. The maximum input voltage that is recognized as a DC LOW-level.

V_{ILD} Dynamic Input LOW Voltage. The maximum input voltage that is recognized as a LOW-level during Multiple Output Switching (MOS) operation.

V_{OH} Output HIGH Voltage. The voltage at an output conditioned HIGH with a specified output load and V_{CC} supply voltage.

V_{OHV} Minimum (valley) voltage induced on a static HIGH high output during switching of other outputs.

V_{OL} Output LOW Voltage. The voltage at an output conditioned LOW with a specified output load and V_{CC} supply voltage.

V_{OLP} Maximum (peak) voltage induced on a static LOW output during switching of other outputs.

V_{OLV} Minimum (valley) voltage induced on a static LOW output during switching of other outputs.

AC Characteristics

f_t Maximum Transistor Operating Frequency—The frequency at which the gain of the transistor has dropped by three decibels.

f_{max} Toggle Frequency/Operating Frequency—The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} Propagation Delay Time—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation Delay Time—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_w Pulse Width—The time between 1.5V amplitude points of the leading and trailing edges of a pulse.

t_h Hold Time—The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s Setup Time—The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} Output Disable Time (of a TRI-STATE Output) from HIGH Level—The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} Output Disable Time (of a TRI-STATE Output) from LOW Level—The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

t_{PZH} Output Enable Time (of a TRI-STATE Output) to a HIGH Level—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} Output Enable Time (of a TRI-STATE Output) to a LOW Level—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW levels.

t_{rec} Recovery Time—The time between the 1.5V level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

AC Loading and Waveforms

For Normal Operation *Figures 1* and *2* show waveforms for all propagation delay and pulse width measurements while *Figures 3* and *4* show waveforms for TRI-STATE enable and disable times. The waveforms shown in *Figure 5* describe setup, hold and recovery times. These diagrams define all input and output measure points used in testing devices in the Normal Operation Mode.

For SCAN Test Operation, *Figure 8* shows propagation delay waveforms; *Figures 9* and *10*, TRI-STATE enable and disable times waveforms; *Figure 11* Set up, hold, and recovery time waveforms and *Figure 12,* Pulse Width waveform.

Figure 6 shows the AC loading circuit used in characterizing and specifying propagation delays of all devices, unless otherwise specified in the data sheet of a specific device. The value of the capacitive load (C_L) is variable and is defined in the AC Electrical Characteristics.

The 500Ω resistor to ground in *Figure 6* is intended to slightly load the output and limit the quiescent HIGH-state voltage to about +3.5V. Also shown in *Figure 6* is a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with open-collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establishes a quiescent HIGH level of +3.5V, which correlates with the HIGH level discussed in the preceding paragraph.

Figures 7a and *7b* describe the input pulse requirements necessary when testing circuits.

Waveforms

Normal Operation

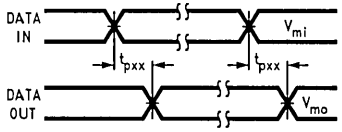

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FIGURE 1. Waveform for Inverting and Non-Inverting Functions

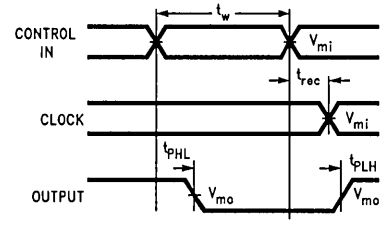

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FIGURE 2. Propagation Delay, Pulse Width and t_{rec} Waveforms

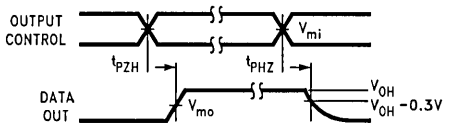

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FIGURE 3. TRI-STATE Output High Enable and Disable Times

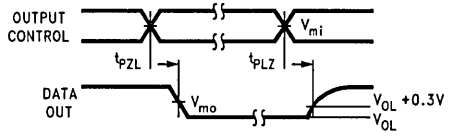

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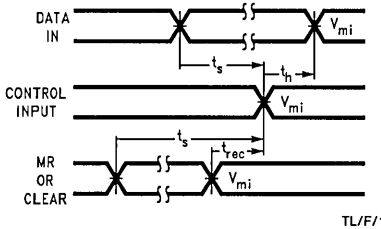
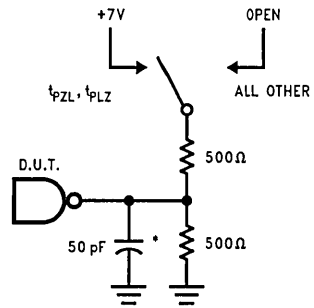
FIGURE 4. TRI-STATE Output Low Enable and Disable Times



TL/F/12134–5

V_{mi} = 1.5V
V_{mo} = 1.5V

FIGURE 5. Setup Time, Hold Time and Recovery Time



TL/F/12134–6

*Includes jig and probe capacitance

FIGURE 6. Standard AC Test Load

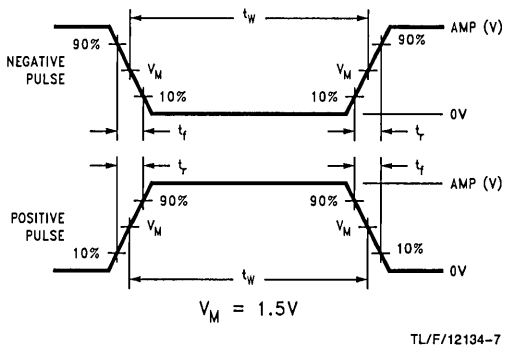


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FIGURE 7a. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 7b. Test Input Signal Requirements

4

Waveforms (Continued)

Scan Test Operation

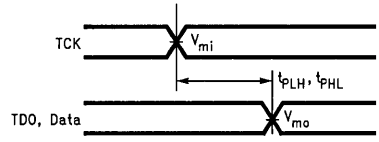

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FIGURE 8. Propagation Delay

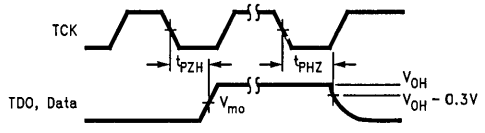

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FIGURE 9. TRI-STATE Output High Enable and Disable Times

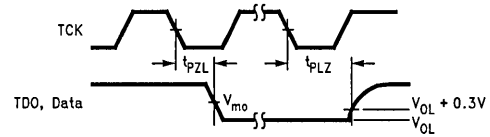

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FIGURE 10. TRI-STATE Output Low Enable and Disable Times

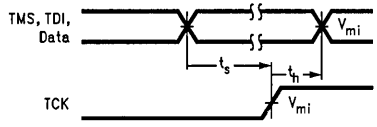

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FIGURE 11. Setup Time, Hold Time and Recovery Time

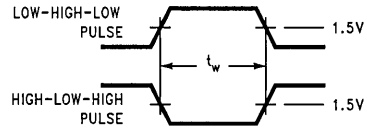

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FIGURE 12. Pulse Width

V_{mi} = 1.5V
V_{mo} = 1.5V

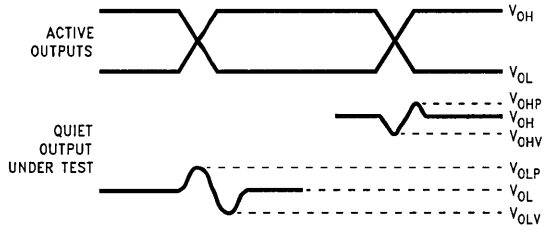

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FIGURE 13. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

Skew Definitions and Examples

Minimizing output skew is a key design criteria in today's high-speed clocking schemes, and National has incorporated skew specifications into the SCAN CMOS family of devices.

This section provides general definitions and examples of skew.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s). See *Figure 15.*

Example:

If signal appears at out #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device, duty cycle and device-to-device delay differences.

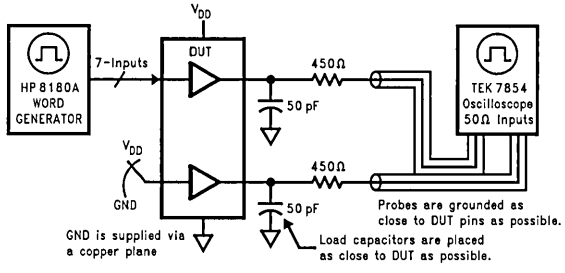

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FIGURE 14. Simultaneous Switching Test Circuit

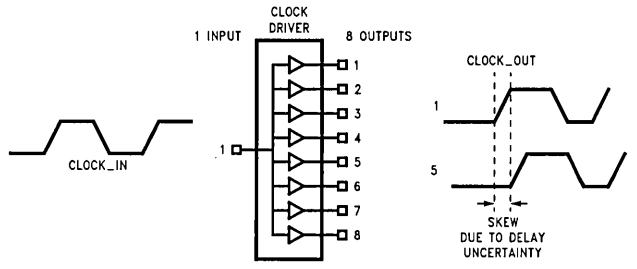

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FIGURE 15. Clock Output Skew

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

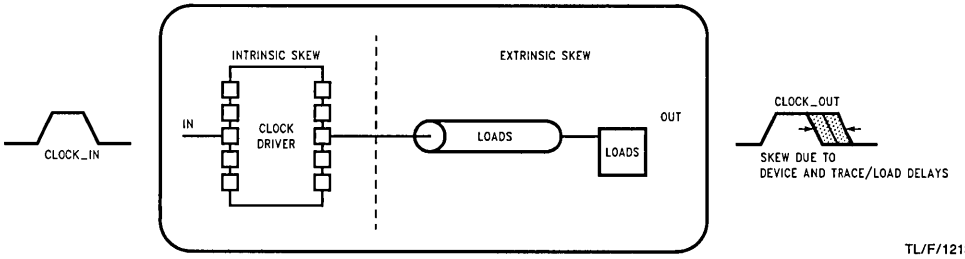

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FIGURE 16. Sources of Clock Skew

Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles

Total system skew budget = 10% of clock cycle = 2 ns* → 2 ns

If extrinsic skew = 1 ns → − 1 ns

Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design *Rule of thumb.*

Skew Definitions and Examples (Continued)

CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is *High* or *Low* in a given clock cycle.

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Duty Cycle = t/T * 100%

FIGURE 17. Duty Cycle Calculation

Clock Signal

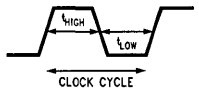

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FIGURE 18. Clock Cycle

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.

Clock + Skew

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FIGURE 19. Clock Skew

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE I

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle		
50 MHz	0 ns	10 ns	10 ns	50/50%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%		
50 MHz	1 ns	11 ns	9 ns	55/45%		
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

$t_{OSHL} = |t_{PHL_{MAX}} - t_{PHL_{MIN}}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLH_{MAX}} - t_{PLH_{MIN}}|$

Propagation delays are measured across the outputs of any given device.

Example

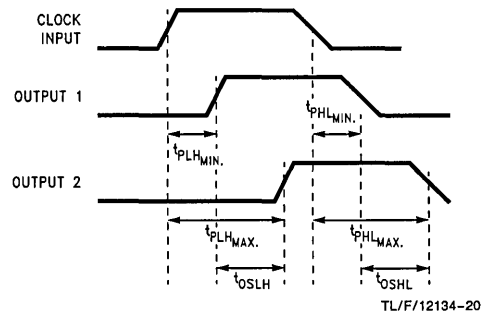

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FIGURE 20. t_{OSLH}, t_{OSHL}

Characterization and Test Specifications

Philosophy

During the product introduction process for National logic IC's, a new IC design will undergo a rigorous characterization to baseline its performance. This data is required to correlate with simulation models, determine product specifications, compare performance to other product, provide a feedback mechanism to the fabrication process, and for customer information. National's Logic IC characterizations are designed to get as much information as possible about the product and potential customer application performance.

National's logic IC characterization methodology uses past knowledge of design performance, simulation, and process parametrics to determine what electrical parameters to characterize. Characterization samples are selected so that they have key process parametrics (e.g., Drive, Beta, V_{tn}, V_{tp} L_{eff}, etc.) which have been shown to significantly affect device electrical parameters. Data is acquired and processed using statistical analysis software. Manufacturing test limits are then set using the knowledge of variations due to fabrication, package, tester, V_{CC}, temperature, and condition. This allows product to be shipped on demand without problems or delays.

The following are brief summaries of characterization tests performed.

AC Electrical Characteristics

Single Output Switching propagation delays
Testing includes measured propagation delays at 50 pF and 250 pF output load capacitances.

t_{PLH} t_{PHL}	Active Propagation Delays
t_{PZH} t_{PZL}	Enable Propagation Delays
t_{PLZ} t_{PHZ}	Disable Propagation Delays

Also included are input timing parameters

t_S	Setup Time
t_H	Hold Time

Multiple (Simultaneous) Output Switching Propagation Delays
These tests are used to ensure compliance to the extended databook specifications and include active propagation delays, disable and enable times at 50 pF and 250 pF output loads.

Multiple Output Switching Skew
Performance data from the Multiple Output Switching propagation delay testing is analyzed to obtain information regarding output skew of an IC.

FMAX (synchronous logic)
FMAX determines the minimum frequency at which the device is guaranteed to operate for a clocked IC. This test is package and test environment sensitive.

Pulse Width (synchronous logic)
Pulse Width testing is used to define the minimum pulse duration that a flip-flop or latch input will accept and still function properly. This test is package and test environment sensitive.

F-Toggle (asynchronous logic)
F-Toggle is the minimum frequency at which the IC is guaranteed to function under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

AC Dynamic (Noise) Characteristics

V_{OLP}, V_{OLV}—Ground Bounce (Quiet Output Switching)
Measured parameters with 50 pF loading relate the amount that a static conditioned output will change in voltage under multiple outputs switching condition with outputs operating in phase. They are heavily influenced by the magnitude that V_{CC} and Ground move internal to the IC.

V_{ILD}, V_{IHD}—Dynamic Threshold
Dynamic threshold measures the shift of an IC's input threshold due to noise generated while under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

Input Edge Rate
This test is performed to determine what minimum edge rate can be applied to an input and have the corresponding output transition with no abnormalities such as glitches or oscillations.

DC Electrical Characteristics

Automated Test Equipment (ATE) DC Tests
DC test data gathered show the performance of an IC to statically applied voltages and currents.

Functional Shmoo
The function shmoo shows the function operational window of an IC at a wide range of V_{CC}'s and temperatures.

Power Up & Power Down Output Shmoo
Similar to the function shmoo, the power up and power down output shmoo shows the DC operation of an output during power up and power down conditions.

Transfer Characteristic (V_{IN}/V_{OUT})

Input Traces (V_{IN}/I_{IN})
Output Traces (V_{OL}/I_{OL}, V_{OH}/I_{OH})

Power

Power-Up I_{CC} Traces
Shows how the supply current reacts to various input conditions during power up.

I_{CC} vs V_{IN} Traces
Traces of I_{CC} vs V_{IN} show how the supply current changes with input voltage.

Power (Continued)

I_{CCD} (Dynamic I_{CC})

Determines the amount of current an IC will consume at frequency.

Capacitance

Input/Output Capacitance (C_{IN}/C_{OUT})

Reliability Tests

Latch-up

Testing determines if an IC is susceptible to latch-up from over-current or over-voltage stresses per MIL-STD-883 JEDEC method 17.

HBM Electrostatic Discharge, Human Body Model

Per MIL-STD-883C method 3015.6.

Quality and Reliability

Introduction

Product qualification is a disciplined, team activity which focuses on demonstrating, through the acquisition and analysis of engineering data, that a device design, fab process, or package design meets or exceeds minimum standards of performance. In most cases, this involves running samples of product through a series of tests which expose the samples to operating stresses far in excess of those which would be encountered in even the most severe "real life" operating environment. These tests are called either accelerated stress tests or accelerated life tests. A properly designed qualification test sequence exposes, within a matter of days or weeks, those design, materials, or workmanship defects which would lead to device failure in the customer's application after months or even years of operation.

In order to be considered a "world class" supplier of semiconductor devices, NSC designs and manufactures products which are capable of meeting the reliability expectations of its most demanding customers. While customer requirements and expectations vary on the subject of reliability requirements for devices, virtually all large users have general procurement specifications which establish failure rate goals or objectives for the suppliers of the components used in their products.

Failure rate goals for infant mortality and long-term-failure-rate-in-service have been established for all NSC product lines. These goals are published internally at the beginning of each fiscal half-year (usually June and December). The actual performance of the product against these goals is measured monthly using life test data gathered from various sources including the Fast Reaction and Long Term Audit Program. Performance is reviewed every six (6) months by Reliability and Product Group management and adjusted as necessary to reflect customer expectations, competitive data, and/or historical performance trends.

Given that product reliability is an overriding corporate objective, and that any deficiency in design, materials, procedures, or workmanship, has a potential for adversely affecting the reliability of the product, Manufacturing and Engineering organizations within NSC, its subsidiaries, and its sub-contractors, involved in introducing a new device, process, or package, share a joint responsibility for demonstrating that the product does conform to NSC standards and to the standards and expectations of NSC's customers.

As a matter of policy, it is NSC's goal to design and manufacture product that is 100% defect-free and capable of surviving the qualification tests with zero failures. This policy is not interpreted as a directive to abandon a qualification program when failures occur or to delay new product releases until perfection has been achieved. Rather, the policy is intended to focus engineering resources on the identification and elimination of the design, process, or workmanship deficiencies that are the root causes of the failures and then to engineer a solution to correct those deficiencies.

Results from the initial qualification for the SCAN ABT Advanced Logic families are published in Self Qualification handbooks. Additional stress testing is performed regularly as a reliability monitor as part of the Fast Reaction Program and Long Term Audit Program. The Self Qualification handbook contains the data typically requested by customers as part of joint qualification programs in addition to detailed explanations of all tests performed. The Logic self qualification handbook may be obtained by contacting the Customer Response Center at 1-800-272-9959.

TABLE II. Qualification Requirements for Logic Integrated Circuits

Test	Test Method	Test/Stress Conditions	Sample Size Each Lot
Operating Life	SOP-5-049-RA Method 107	1000 Hours @T_A = 125°C	77
High Temperature Storage	SOP-5-049-RA Method 103	1000 Hours @150°C	45
Temperature Cycle	SOP-5-049-RA Method 105	1000 Cycles −65°C to +150°C	77
Temperature Cycle with Preconditioning	SOP-5-049-RA Method 105	1000 Cycles −65°C to +150°C	77
Temperature-Humidity-Bias	SOP-5-049-RA Method 104	1000 Hours 85°C @ 85%RH	77
Temperature-Humidity-Bias with Preconditioning	Method 112 Method 104	Precondition plus 100 hours 85°C to 85%RH	77
Autoclave	Method 101	500 hours 121°C @ 15 psig	45
Thermal Shock	Method 106	100 Cycles −65°C to +150°C	22
Salt Atmosphere	Method 209	25 Hours 35°C	22
Resistance to Solvents	Method 207	4 Solvents	3 Each Solvent
Lead Integrity	Method 205	Condition as Appropriate to Package	22 Leads
Solderability	Method 203	8 Hour Steam 5 secs @260°C	22
Solder Heat	Method 204	12 secs 260°C	22

Quality Information and Communication (QUIC) System

BACKGROUND

National's Quality Assurance Systems Development group (QASD) maintains a variety of data tracking systems such as: Electronic Reliability Data Management (ERDM), Failure Analysis (F/A), Burn-in Board Inventory, and a number of others.

QUIC users will find a user friendly, menu-driven, real-time system that gives them a simultaneous-user environment with timely data inputs from sites around the world. QUIC is programmed to recognize each individual user of the system at the point of logging on to the mainframe, and provides an appropriate list of menu options consistent with the user's level of access requirements.

National grants access to QUIC by customers that provides a sufficient level of security over the entire system, thus precluding the possibility of accidental access (or even damage) to various files.

HOW A CUSTOMER LINKS TO QUIC

1. Check to make sure you have the hardware components listed below. (An attached printer is desirable but not imperative.)

   IBM/PC compatible computer with at least 128k memory.

   Hayes compatible 1200 baud modem (or 2400, 4800 or 9600).

   Touch tone phone.
2. Request access to QUIC by contacting your National sales representative or Customer Service Center at 1-800-272-9959, who will coordinate all activities necessary to provide access for your company and arrange training (usually handled over the telephone).
3. Identify the person who will be your company's main contact and user of the QUIC system. This person will assume responsibility for the USERID assigned to your company and will receive training on how to access and use the QUIC system.
4. National will provide a USERID, password and account number with appropriate menus and a communications software package called EXECULINK, which allows the customer's PC to talk with NSC's host computer and also turns the PC into a virtual host terminal, with full-screen editing capability and full use of program function (PF) keys. EXECULINK also provides for file transferring between host and PC and spooling of print files to a PC-attached printer.

ONGOING IMPROVEMENTS

As we receive feedback from the users of QUIC, we (QASD) will continue to enhance the "User Friendliness" of the system and add new features which, we hope, will help promote a true sense of teamwork between us and our customers.

Wafer Level Reliability (WLR)

BACKGROUND

The conventional methods of reliability screening, that of short-term burn-in to eliminate infant mortalities and long-term life tests at high temperature, will soon become impractical for many devices. The reasons for this are tighter infant mortality ppm requirements, higher costs, and shortened lifetimes.

As device complexity increases, the testing sample size required to ensure infant mortality ppm levels in the 0–10 ppm range will quickly deplete reliability test capacity. While burn-in eliminates inferior devices, it can also substantially shorten the lifetimes of "good" devices to an unacceptable level, creating an expensive and somewhat risky procedure. New technology advances which minimize geometry, have moved our device lifetime distributions closer to our customer's expected system life. As device geometries shrink, resulting in higher current densities, electric fields, and chip temperatures, tighter fab process control and instant feedback become critical.

THE GOAL OF WAFER-LEVEL-RELIABILITY TESTING-PROCESS RELIABILITY

Wafer-level-reliability testing represents a proactive, correlation and control approach to ensuring device reliability. WLR is not meant to replace classical reliability testing. Instead it is used to supplement existing methods.

WLR testing is used to:

1. Identify shifts in On-Line Process Controls (fab monitors) which affect product reliability.
2. Reduce process qualification cycle time.
3. Improve process qualification success rate.
4. Assess reliability trends of production processes.
5. Quantify the reliability impact of process modifications.

WLR provides faster feedback for fab process control. The collection of WLR test data during and at the end of wafer fab processing provide a reliability baseline for each of our fab processes. Shifts in WLR test results, whether intentional (a process change or qualification) or unintentional (a process control problem), signal an increase or decrease in product reliability risk. WLR monitoring of production processes using Statistical Quality Control (SQC) techniques provides engineering with the information required to find and fix process control problems faster, and to determine the effectiveness of on-line process controls from a reliability standpoint. In this way, WLR testing is used to link on-line process controls to the traditional accelerated life testing methods.

NATIONAL'S WLR PROGRAM

National developed a corporate-wide WLR program which continues to implement powerful, new test techniques. WLR testing has been used effectively to help understand how process variability affects product reliability. It is also used to help build-in reliability at the design stage for new process technologies.

WLR tests and test structures have been designed to increase the likelihood and predict a rate of a reliability failure mechanism occurrence. In addition, National has developed a partnership with a leading parametric test system supplier. Working together, a WLR test system was designed and developed to meet the unique requirements of Wafer-Level-Reliability testing. These systems are capable of testing to the voltage, current, and temperature extremes required for inducing the desired failure mechanisms in a short period of time. Some examples of the reliability failure mechanisms that are monitored using WLR techniques include:

Interlayer Dielectric Integrity

Unique high voltage testing (to 1500V) is used to test for dielectric particles, metal hillocks or contamination, and poor dielectric stop coverage. Designed experiments

Wafer Level Reliability (WLR) (Continued)

have been successful in correlating the high voltage WLR test results to fab process monitors (such as deposition temperature and etch selectivity), and to accelerated life test results (Op-life, Temp Cycle, and Thermal Shock).

Metal Step Coverage

High current testing of large area metal serpentine structures is performed to detect restrictions in the conducting stripe. Designed experiments have been successful in correlating the high current WLR test results to fab process monitors such as metal thickness, critical dimensions, and via size.

Mobile Ions

A 200°C hot chuck is used with custom-built high temperature probe cards to accurately measure transistor threshold voltage shifts for a variety of oxide layers. Other methods for detecting mobile ion contamination include the use of self-heated polysilicon gate test structures and Triangular Voltage Sweep (TVS) test techniques.

Metal Stress Voids

High current resistance measurements are taken before and after wafers are processed through a series of heating and cooling cycles. This heat treatment is designed to mimic the high temperature processing incurred during device assembly (such as a seal-dip furnace), and it has been shown to accelerate metal void formation when the stress of the overlying film is high enough. Significant increases in the final resistance indicate the formation of metal stress voids.

Gate Oxide Integrity:

JEDEC J_{RAMP}, V_{RAMP} and Q_{BD} test techniques are used to monitor gate oxide quality. The WLR tester is also used to perform very sensitive leakage current measurements, using a specially designed picoammeter module, which allows us to detect subtle differences in gate oxide quality.

Passivation Integrity

A novel wafer-level-autoclave test technique has been developed which allows us to quantify the level of protection the passivation film provides when the wafer is subjected to a high temperature, high humidity environment.

Hot Electron Degradation

Two wafer level tests are performed to indicate device susceptibility to hot electron damage. First, the maximum substrate current is measured to indicate the level of impact ionization occurring at the drain edge. Second, gate current measurements are taken to gauge the magnitude of electron injection during device operation. Long-term DC stressing of transistors at peak substrate current conditions is also monitored.

Electromigration

A Standard Wafer Electromigration Accelerated Test (SWEAT) technique is used to measure the sensitivity of a metal line to electromigration failures. SWEAT is used as a relative test of the reliability of a line.

Contact Electromigration

Risk of failures due to contact spiking and solid phase epitaxial growth (SPEG) are monitored by forcing current through specially designed test structures, and monitoring increases in resistance and substrate leakage.

Electrostatic Discharge Sensitivity (ESD)

BICMOS LOGIC

National BiCMOS Logic has designed special dual-rail ESD protection circuitry to increase its level of ESD performance over non-protected inputs and outputs. This protection is standard on all BiCMOS Logic designs and was first used in National's family.

By design, this circuitry limits product vulnerability to both positive and negative Human Body Model (HBM) ESD and Electrical Overstress (EOS) voltages by protecting inputs and outputs connected to V_{CC} as well as ground. Protection to ground is provided through the transistor Q2 and diode D2, standard Schottky clamp. The path to V_{CC} is protected through the BVCEO breakdown mechanism of Q1. Diode D1 ensures isolation of the input or output from V_{CC} leakages.

The device design and layout ensures dependable turn-on characteristics as well as robustness.

ESD protection was achieved with no appreciable affect on speed or increase in capacitance.

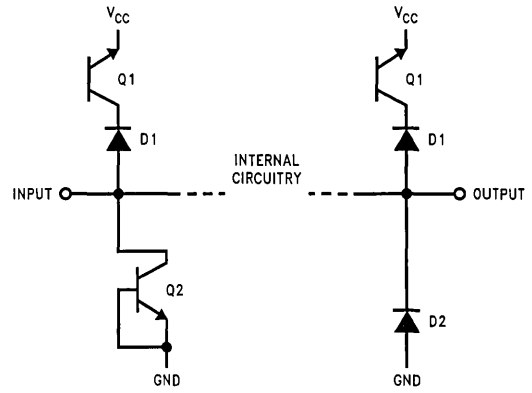

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Figure 21. ESD Protection Circuit

Electrostatic Discharge Sensitivity (ESD) (Continued)

ABT and SCAN ABT logic ESD sensitivity is guaranteed greater than 2000V, using the MIL-STD-883C, test method 3015 for Human Body Model (HBM) ESD.

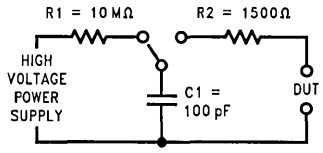

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Figure 22. HBM Test Circuit

Normal handling precautions should be observed as in the case of any semiconductor.

CMOS Logic

Circuits which show excellent resistance to ESD-type damage are classified as category "B" of MIL-STD-883C, test method 3015, and withstand in excess of 4000V typically. It is guaranteed to have 2000V ESD immunity on all inputs and outputs. Parts do not require any special handling procedures, however, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 23 shows the ESD test circuit used in the sensitivity analysis for this specification. *Figure 24* is the pulse waveform required to perform the sensitivity test.

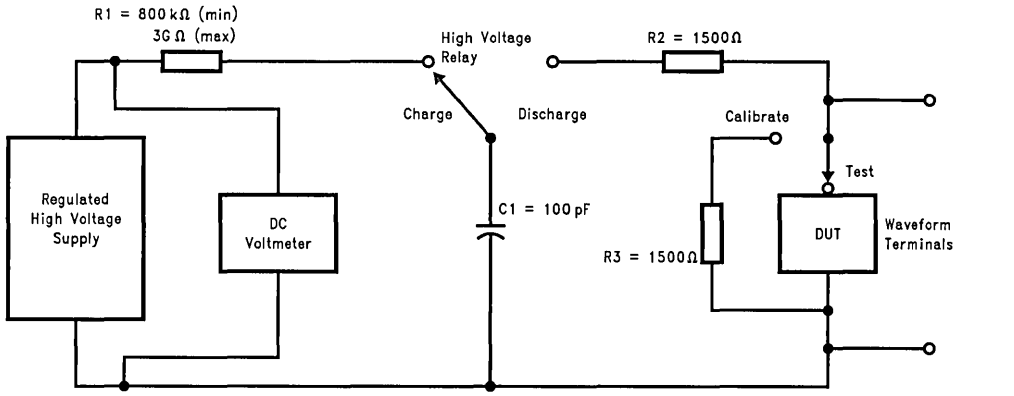

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FIGURE 23. ESD Test Circuit

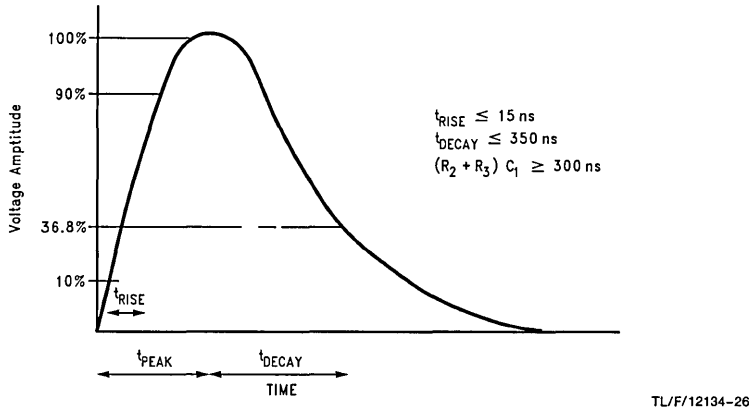

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FIGURE 24. ESD Pulse Waveform

Power Sensitivities for Minimum Geometry Products

The demand for high performance process technology capable of sub 4 ns speeds, minimal noise and lower operating voltages drives the microelectronics industry towards decreasing layout geometries. Advanced process technology minimizes gate widths, gate oxide thickness and junction depths to improve gate switching speeds. In contrast, the decreased geometries reduce the ability of the devices built on advanced processes to resist electrical overstresses. As geometries decrease, emphasis shifts towards the reduction of environmentally induced electrical overstresses to ensure system and component reliability.

Market trends continue to drive the need for smaller geometries with reduced power supply voltages. Current 5.0V technologies are migrating towards 3.0V technologies while 3.0V technologies have shown a greater sensitivity to electrical overstresses. Sensitivities to electrical overstresses have been observed in as large as 1.0 μm geometries.

Device damage from electrical overstresses vary and the categories include, but are not limited to: Electrical-Over-Stress (EOS) due to excessive current or voltage exposure and Electro-Static-Discharge (ESD) be it exposure by Human Body Model, Charged Device Model or Machine Model. Sources of electrically induced overstresses are difficult to determine; however, investigation of failures from small geometry devices may show that environmental hazards such as unregulated and unconditioned power supplies in the field exceed "Absolute Maximum Ratings" causing unrecoverable device damage.

Advanced processes such as BiCMOS include small dimension current density limited geometries that are sensitive to electrically induced overstresses. The combination of internal bipolar and CMOS gates provides current capabilities for maximum device performance. In an unconditioned supply environment, the bipolar section of a BiCMOS circuit can source excessive current through the CMOS section and cause damage due to the CMOS circuit's current density limited geometries.

In an effort to resolve device sensitivities to electrical overstresses, designers and engineers can reference device databooks. Databook specifications include "Absolute Maximum Ratings" and adherence to this specification is essential in ensuring component and system level reliability.

1. A. Amerasekera, A. Chatterjee, *"An Investigation of BiCMOS ESD Protection Circuit Elements and Applications in Submicron Technologies"*, EOS/ESD Symposium, p5B.6.1.

Latchup Testing

Latchup in CMOS and bipolar circuits can vary in severity from being a temporary condition of excessive I_{CC} current and functional failure, to total destruction requiring a new unit. The latchup condition is usually caused by applying a stimulus that is able to cause a regenerative condition in a PNP-NPN structure. For a more detailed description of definitions and causes of latchup, see National Semiconductor Application Note 600 (located in the "FACT Advanced CMOS Logic Data book" Lit. # 40019).

BiCMOS Logic

National has characterized its Advanced BiCMOS logic for robustness using the JEDEC 17 method and an IMCS 4600 Automated Latchup Test System. The automated test equipment approach to latchup provides a repeatable test setup and application of test conditions, reduces the amount of time for evaluation, and provides a more comprehensive set of vectors and stimuli over a shorter period of time.

The JEDEC 17 method is a standard measurement procedure for the characterization of CMOS integrated circuit latchup susceptability/immunity, measured under static conditions. The method allows for overcurrent/overvoltage stressing of inputs and outputs to detect latchup.

In short, the JEDEC 17 method follows a sequence of:

1. Apply power
2. Setup I/O conditions to place device in desired state
3. Apply trigger source for desired duration
4. Measure supply current
5. Remove power supply if $I_{CC} \geq$ test limit
6. Inspect for electrical damage

The time for each parameter as well as the temperature is critical for correlation of latchup. National characterizes latchup on the Advanced BiCMOS family at 125°C and with the critical timing parameters on Table III. Close correlation can only be accomplished by using the same trigger duration, V_{CC}, test temperature, and magnitude of trigger stimulus.

TABLE III. Critical Timing Parameters

Symbol	Parameter	Time
T_W	Trigger Duration	500 μs
t_{COOL}	Cool Down Time	10 ms

Latchup Testing (Continued)

For BiCMOS ABT products, logic states are checked for a susceptability to latchup with all outputs high, all outputs low and all outputs in TRI-STATE. If the device is a bidirectional device, then the logic states are tested in each direction. All inputs and outputs are tested for each logic state and direction.

Because the ABT and SCAN ABT family is designed for live insertion, a Positive Voltage Trigger (PVT) and a Negative Current Trigger (NIT) is applied to the inputs and outputs to check for latchup.

Forcing a current in the positive direction overstresses the inputs and outputs by causing a breakdown. Such breakdowns consume enough power in the breakdown area to cause the junction permanent damage. PVT stresses the inputs and output while keeping the input and output devices out of any breakdown region.

Finally all inputs and outputs have clamp diodes, requiring a negative current trigger as a stimulus for latchup. The clamp diodes are designed to allow current flow into ground without injecting carriers into the substrate that could cause a parasitic PNP-NPN. Supply and stimulus values used by National for latchup testing the ABT family are in Table IV.

TABLE IV. Supply and Stimulus Values

Stimulus	Parameter	V_{CC}	Stimulus
PVT	Positive Voltage Trigger	7.0V	V_{CC} + 3V (10V)
NIT	Negative Current Trigger	7.0V	−500 mA

Verification of any unusual observations is performed with a curve tracer manually. For example, when ABT outputs are brought below ground, the NMOS transistor feeding current to the bipolar output will turn on and current from V_{CC} will come out of the output pull-down device. This condition is unavoidable by design and is not latchup. Thus good analysis of observations will tell one whether latchup has occurred.

Due to the high trigger stresses, devices used for latchup testing should be discarded and not used for design, production, or other tests. Latchup testing is potentially destructive and may limit the life of a device.

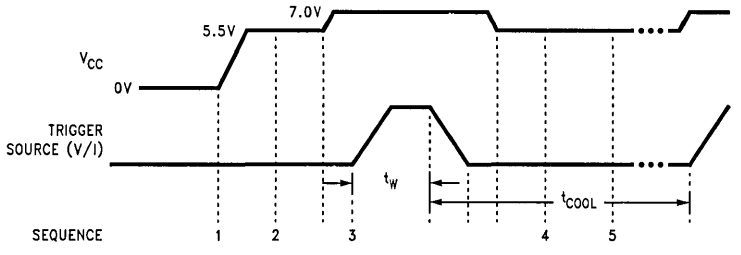

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FIGURE 25.

Latchup Testing (Continued)

CMOS Logic

In the past a major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. SCAN CMOS logic is guaranteed not to latch-up with dynamic currents of 300 mA forced into or out of the inputs or the outputs under worst case conditions (T_A = 125°C and V_{DD} = 5.5 V_{DC}). At room temperature the parts can typically withstand dynamic currents of close to 1A. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

SCAN CMOS devices have been specifically designed to reduce the possibility of latch-up occurring; National Semiconductor accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

The test procedure is as follows; five pulses, each of at least 2000V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883C, TM-3015. Devices that result in ESD immunity in the 2000V–3999V range are listed as ESD Class 2. Devices that result in ESD immunity in the 4000+V range are listed as ESD Class 3.

For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.

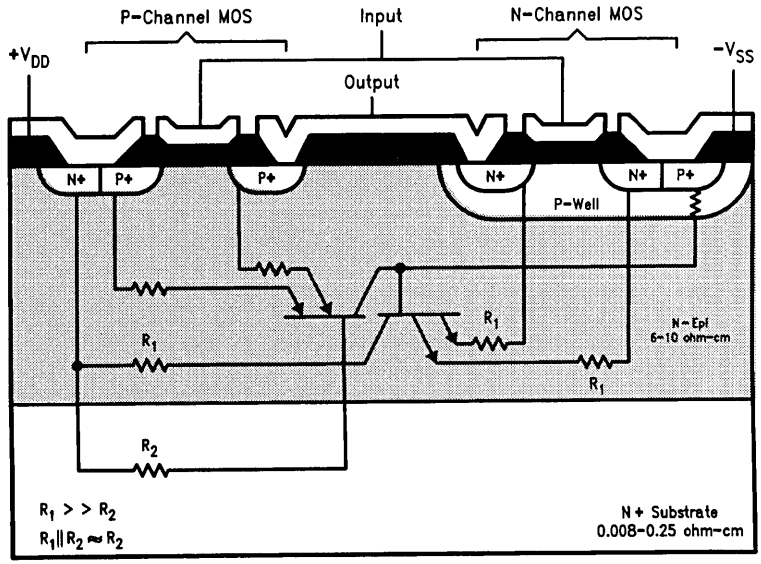

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FIGURE 26. Advanced CMOS EPI Process Cross Section with Latch-up Circuit Model

Section 5

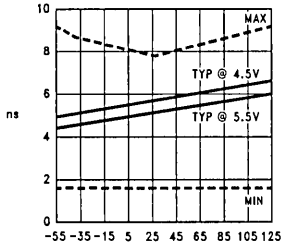
Characterization Data

Section 5 Contents

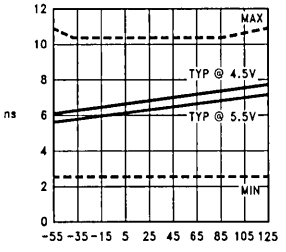
Propagation Delay vs Temperature Capacitive Loading and Switching Outputs

SCAN18245T

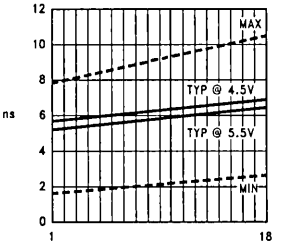
t_{PHL} (A to B/B to A) vs Temperature
C_L = 50 pF, 1 Output Switching



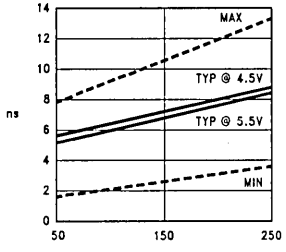
t_{PHL} (A to B/B to A) vs Temperature
C_L = 50 pF, 18 Outputs Switching



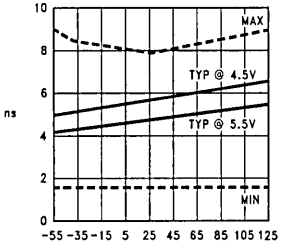
t_{PHL} (A to B/B to A) vs
Outputs Switching
C_L = 50 pF, T_A = +25°C



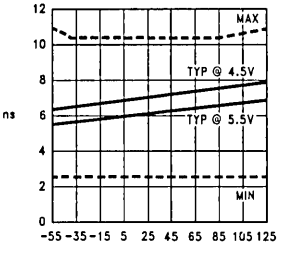
t_{PHL} (A to B/B to A) vs Load Capacitance
1 Output Switching, T_A = +25°C



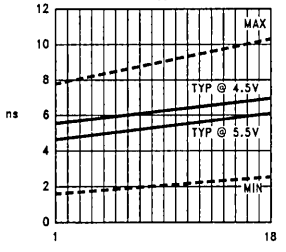
t_{PLH} (A to B/B to A) vs Temperature
C_L = 50 pF, 1 Output Switching



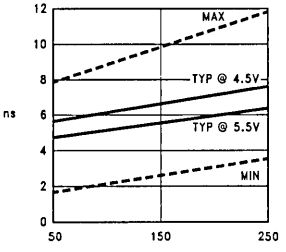
t_{PLH} (A to B/B to A) vs Temperature
C_L = 50 pF, 18 Outputs Switching



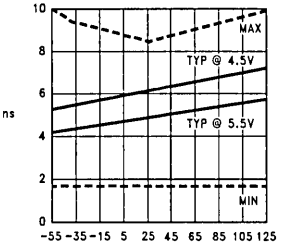
t_{PLH} (A to B/B to A) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



t_{PLH} (A to B/B to A) vs Load Capacitance
1 Output Switching, T_A = +25°C



t_{PZH} ($\overline{OE}$ to A_n/B_n) vs Temperature
C_L = 50 pF, 1 Output Switching



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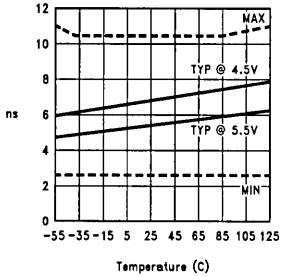
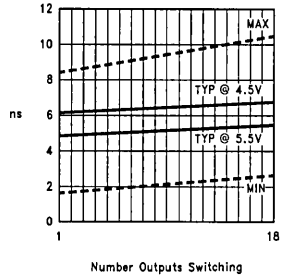
SCAN18245T (Continued)

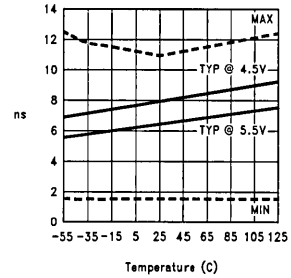
t_{PZH} ($\overline{OE}$ to A_n/B_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



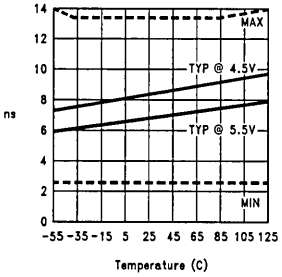
t_{PZH} ($\overline{OE}$ to A_n/B_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



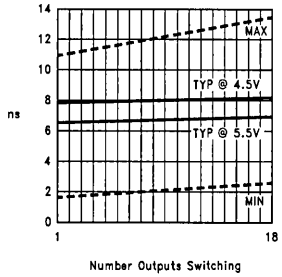
t_{PZL} ($\overline{OE}$ to A_n/B_n) vs Temperature
C_L = 50 pF, 1 Output Switching



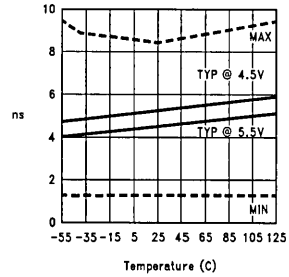
t_{PZL} ($\overline{OE}$ to A_n/B_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



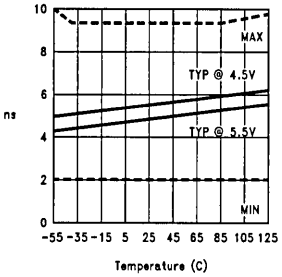
t_{PZL} ($\overline{OE}$ to A_n/B_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



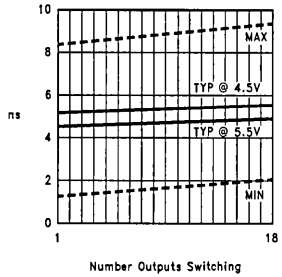
t_{PHZ} ($\overline{OE}$ to A_n/B_n) vs Temperature
C_L = 50 pF, 1 Output Switching



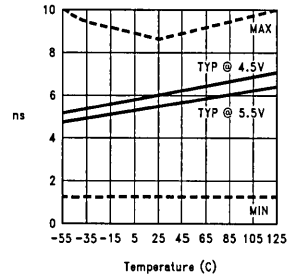
t_{PHZ} ($\overline{OE}$ to A_n/B_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



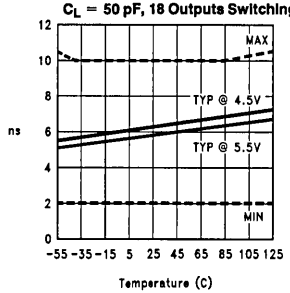
t_{PHZ} ($\overline{OE}$ to A_n/B_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



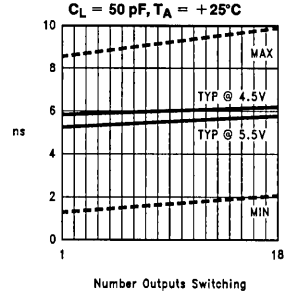
t_{PLZ} ($\overline{OE}$ to A_n/B_n) vs Temperature
C_L = 50 pF, 1 Output Switching



t_{PLZ} ($\overline{OE}$ to A_n/B_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



t_{PLZ} ($\overline{OE}$ to A_n/B_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



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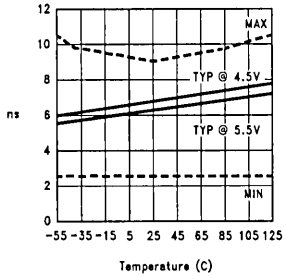
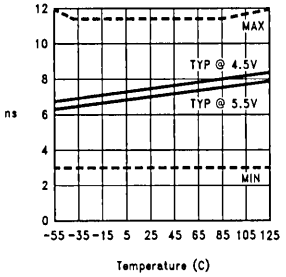
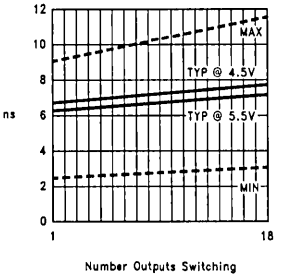
t_{PHL} (I_n to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



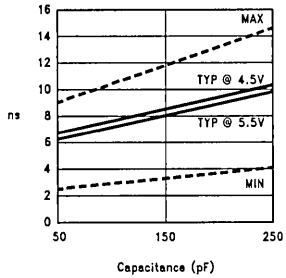
t_{PHL} (I_n to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



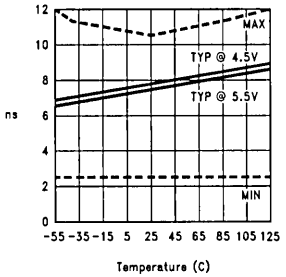
t_{PHL} (I_n to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



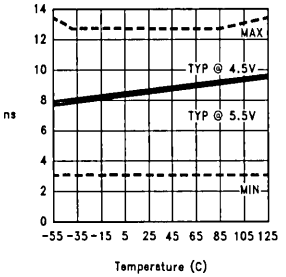
t_{PHL} (I_n to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



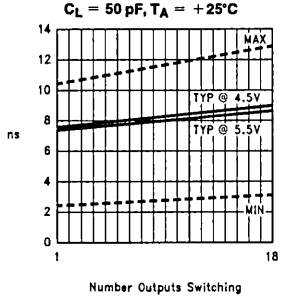
t_{PHL} (LE to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



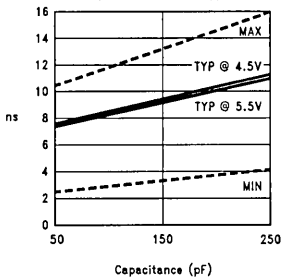
t_{PHL} (LE to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



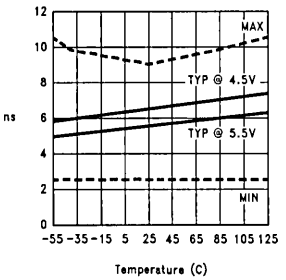
t_{PHL} (LE to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



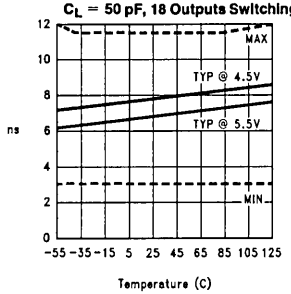
t_{PHL} (LE to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



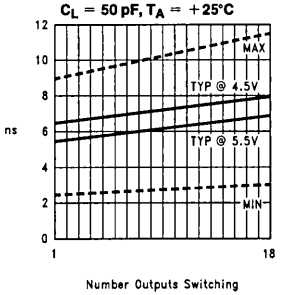
t_{PLH} (I_n to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



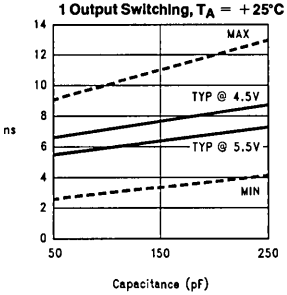
t_{PLH} (I_n to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



t_{PLH} (I_n to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



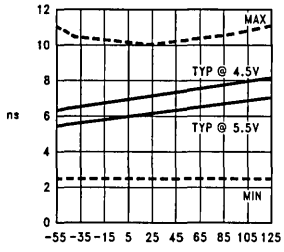
t_{PLH} (I_n to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



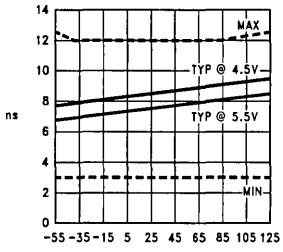
TL/F/11576-3

SCAN18373T (Continued)

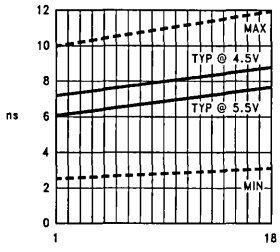
t_{PLH} (LE to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



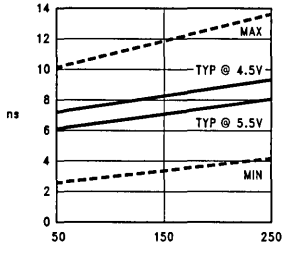
t_{PLH} (LE to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



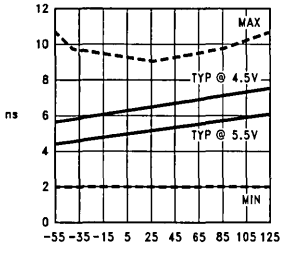
t_{PLH} (LE to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



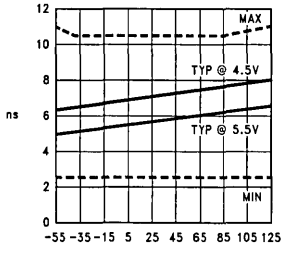
t_{PLH} (LE to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



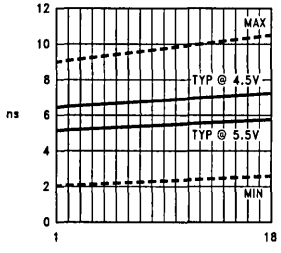
t_{PZH} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



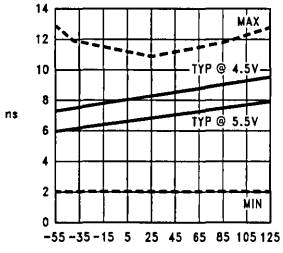
t_{PZH} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



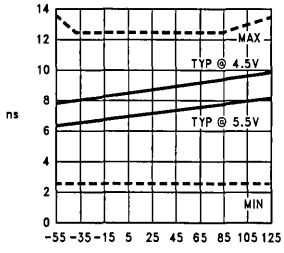
t_{PZH} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



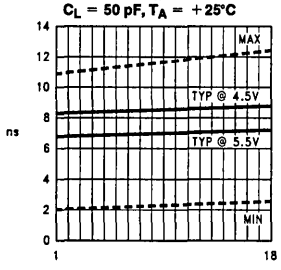
t_{PZL} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



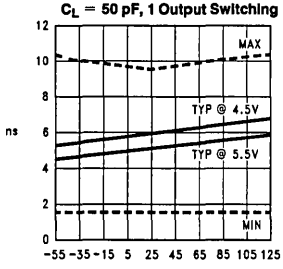
t_{PZL} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



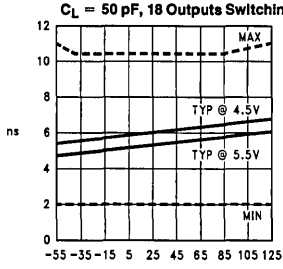
t_{PZL} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



t_{PHZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



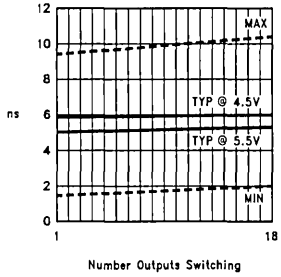
t_{PHZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



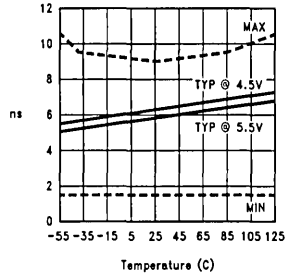
TL/F/11576–4

SCAN18373T (Continued)

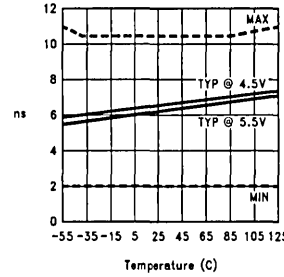
t_{PHZ} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



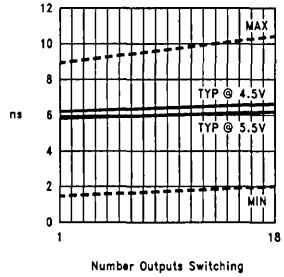
t_{PLZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



t_{PLZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



t_{PLZ} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



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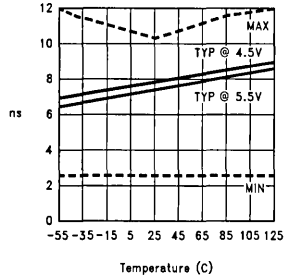
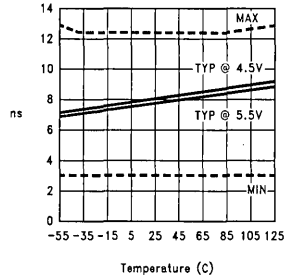
SCAN18374T

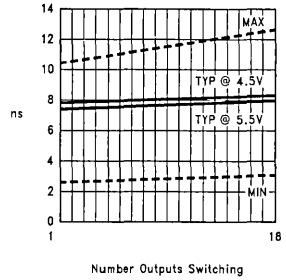
t_{PHL} (CP to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



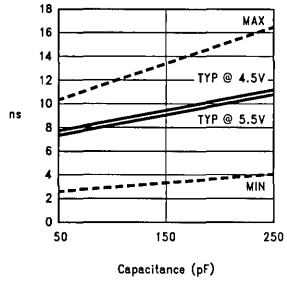
t_{PHL} (CP to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



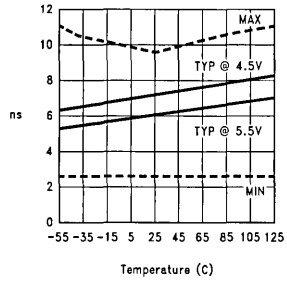
t_{PHL} (CP to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



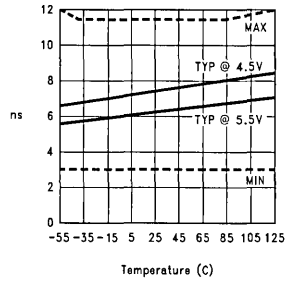
t_{PHL} (CP to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



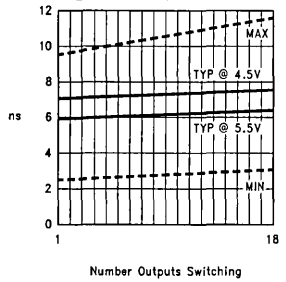
t_{PLH} (CP to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



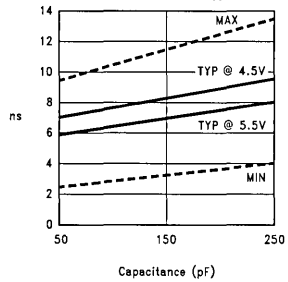
t_{PLH} (CP to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



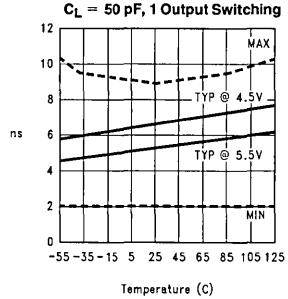
t_{PLH} (CP to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



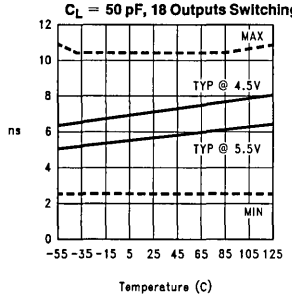
t_{PLH} (CP to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



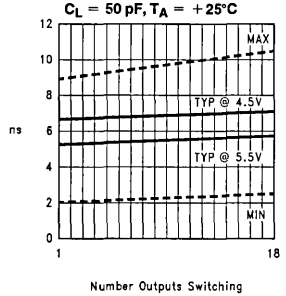
t_{PZH} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



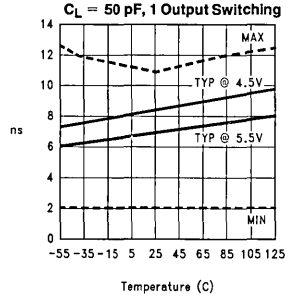
t_{PZH} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



t_{PZH} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



t_{PZL} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



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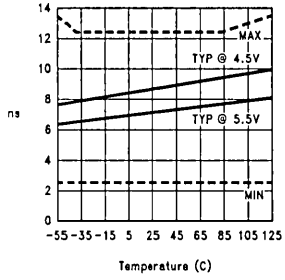
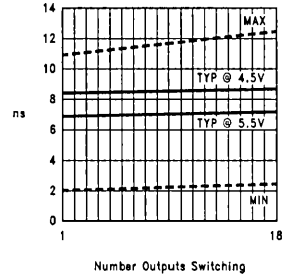
SCAN18374T (Continued)

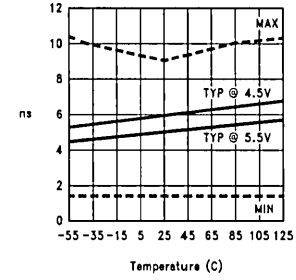
t_{PZL} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



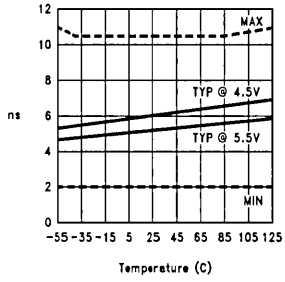
t_{PZL} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



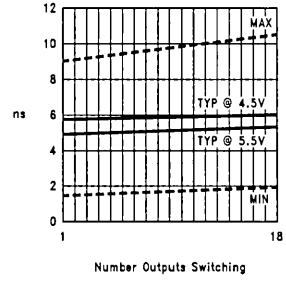
t_{PHZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



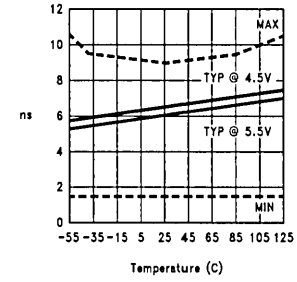
t_{PHZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



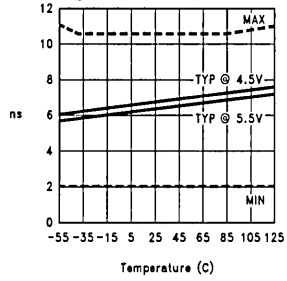
t_{PHZ} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



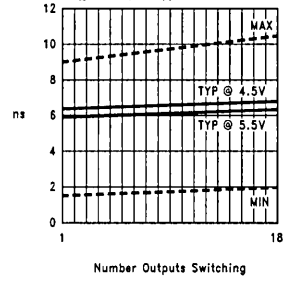
t_{PLZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



t_{PLZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



t_{PLZ} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



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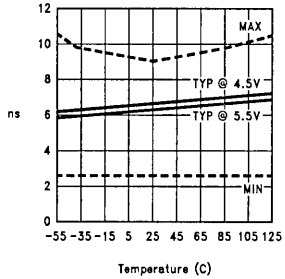
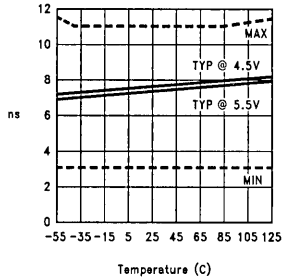
SCAN18540T

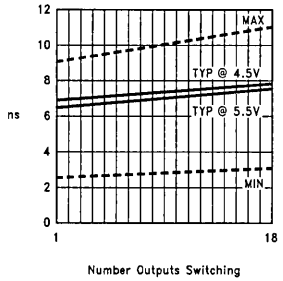
t_{PHL} (I_n to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



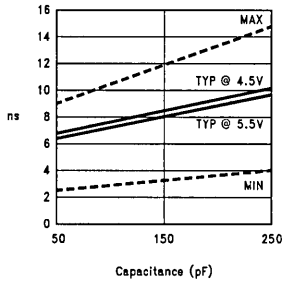
t_{PHL} (I_n to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



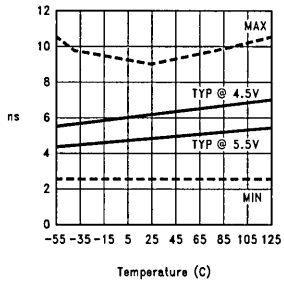
t_{PHL} (I_n to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



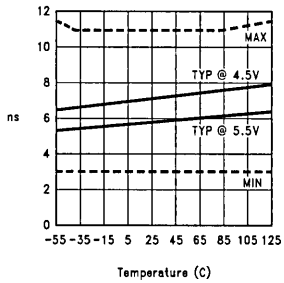
t_{PHL} (I_n to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



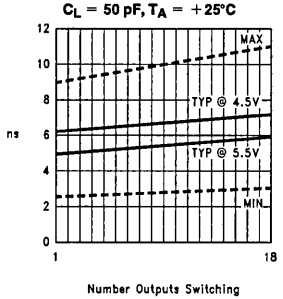
t_{PLH} (I_n to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



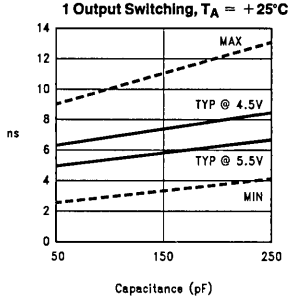
t_{PLH} (I_n to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



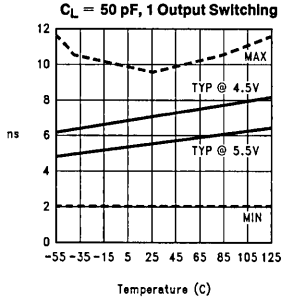
t_{PLH} (I_n to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



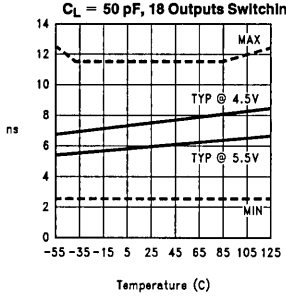
t_{PLH} (I_n to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



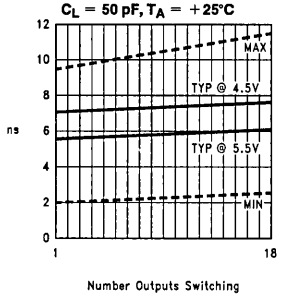
t_{PZH} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



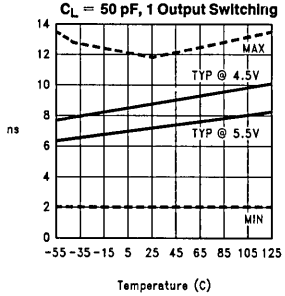
t_{PZH} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



t_{PZH} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



t_{PZL} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



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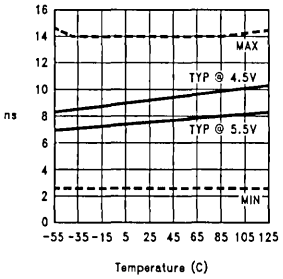
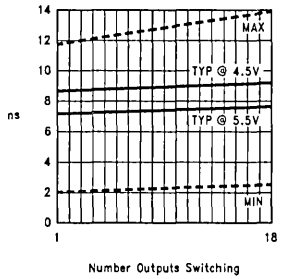
SCAN18540T (Continued)

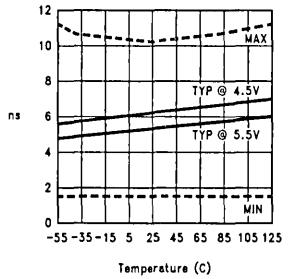
t_{PZL} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



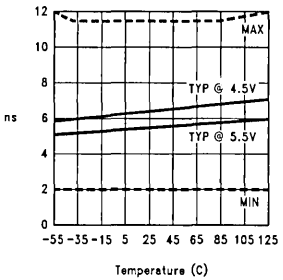
t_{PZL} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



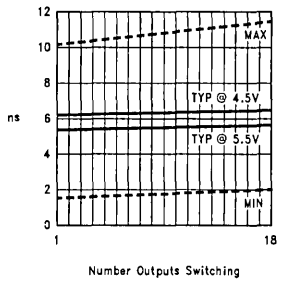
t_{PHZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



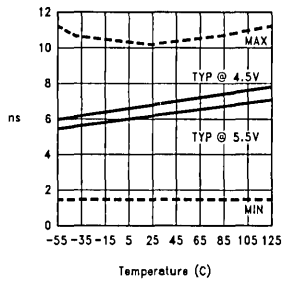
t_{PHZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



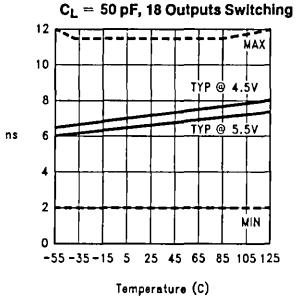
t_{PHZ} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



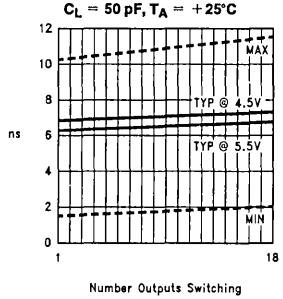
t_{PLZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



t_{PLZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



t_{PLZ} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



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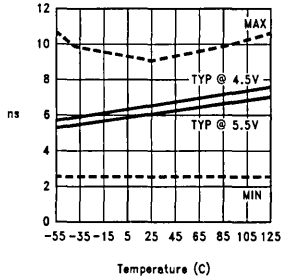
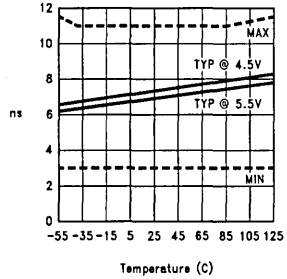
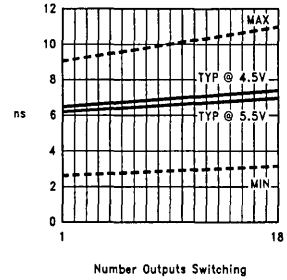
t_{PHL} (I_n to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



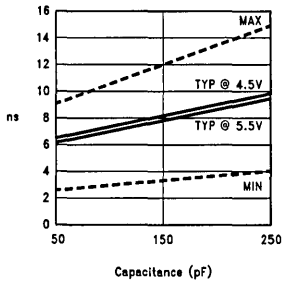
t_{PHL} (I_n to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



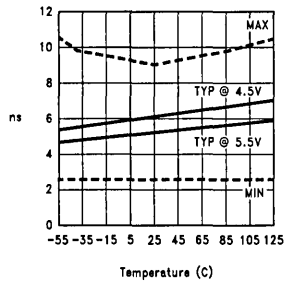
t_{PHL} (I_n to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



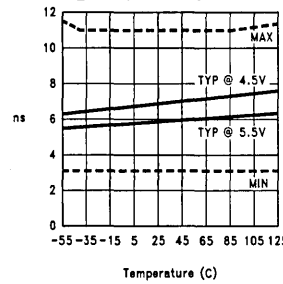
t_{PHL} (I_n to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



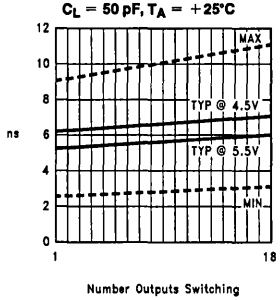
t_{PLH} (I_n to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



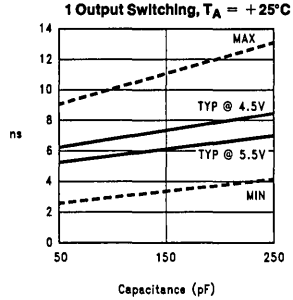
t_{PLH} (I_n to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



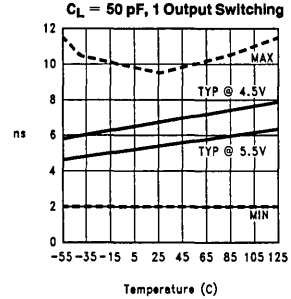
t_{PLH} (I_n to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



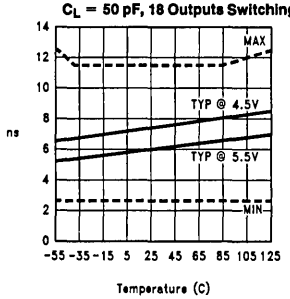
t_{PLH} (I_n to O_n) vs Load Capacitance
1 Output Switching, T_A = +25°C



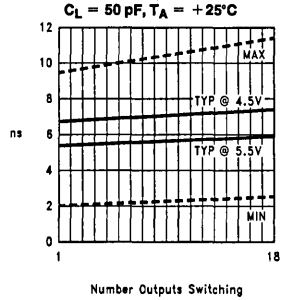
t_{PZH} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



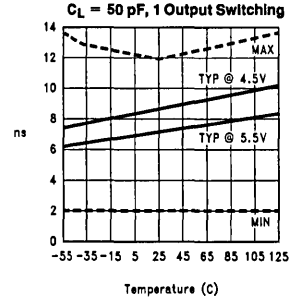
t_{PZH} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



t_{PZH} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



t_{PZL} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



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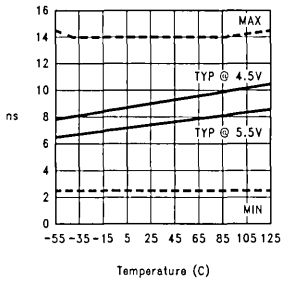
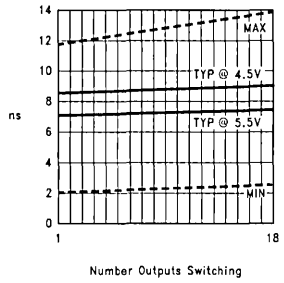
SCAN18541T (Continued)

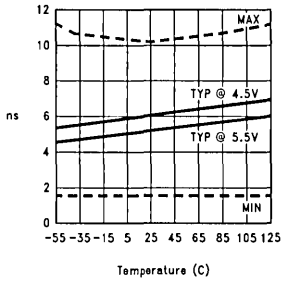
t_{PZL} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



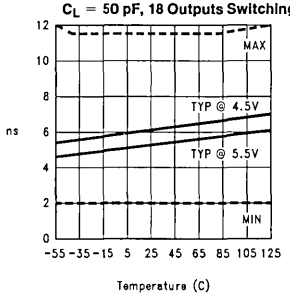
t_{PZL} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



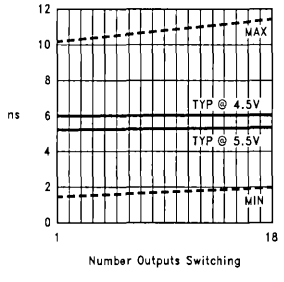
t_{PHZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



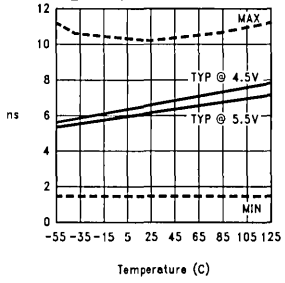
t_{PHZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



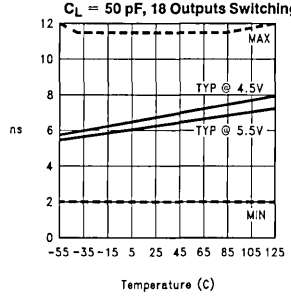
t_{PHZ} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



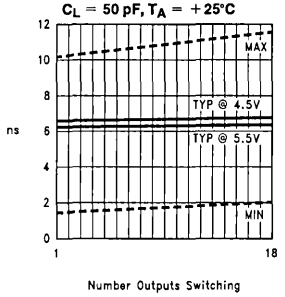
t_{PLZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 1 Output Switching



t_{PLZ} ($\overline{OE}$ to O_n) vs Temperature
C_L = 50 pF, 18 Outputs Switching



t_{PLZ} ($\overline{OE}$ to O_n) vs # Outputs Switching
C_L = 50 pF, T_A = +25°C



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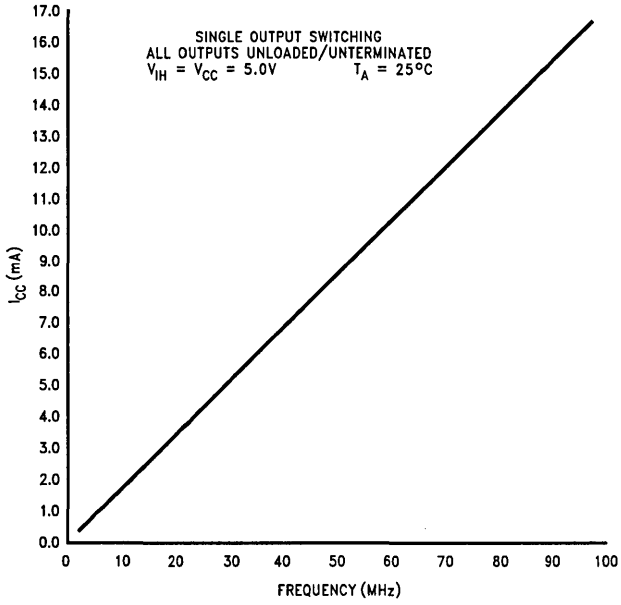
Typical I_{CC} vs Frequency

(SCAN18245T, SCAN18373T, SCAN18374T, SCAN18540T, and SCAN 18541T)



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Section 6

Boundary Scan Design Support

Section 6 Contents

Boundary Scan Design Support

Information on IEEE Standards

The IEEE Working Group developed the IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture. To purchase this book [$50], please call one of the following numbers and ask for SH13144:

In the USA: 1-800-678-IEEE

Outside the U.S. or Canada: 1-908-981-1392

Some Excellent Literature Written on Boundary Scan Includes:

1. *Boundary-Scan Test, A Practical Approach* by Harry Bleeker, Peter van den Eijnden, Frans de Jong, Kluwer Academic Publishers
2. *The Boundary-Scan Handbook* by Kenneth P. Parker, Kluwer Academic Publishers
3. *The Test Access Port and Boundary-Scan Architecture* by Colin M. Maunder and Rodham E. Tulloss, IEEE Computer Society Press (1-800-CS-BOOKS)
4. *IEEE 1149.1—1994 SCAN Tutorial Handbook* by National Semiconductor, call 1-800-272-9959, Customer Response Center.

CONFERENCES

An excellent platform for seeing the latest developments in boundary scan support is to attend conferences. One of the biggest is the International Test Conference (ITC) held annually in the fall.

In Europe, the European Test Conference (ETC) is held every other spring. For more information call the IEEE Computer Society in Brussels at: 32-2-7702242.

BSDL Models

The BSDL (Boundary Scan Description Language) is designed as a subset and standard practice of VHDL, a standard language for describing the testability features of our boundary scan devices.

National Semiconductor will supply the BSDL models on a floppy to you, free of charge.

National has BSDL models available today on the following devices:

18-bit CMOS Test Access Logic
SCAN18245T
SCAN18373T
SCAN18374T
SCAN18540T
SCAN18541T

18-bit BiCMOS Test Access Logic
SCAN182245A
SCAN182373A
SCAN182374A
SCAN182541A

SCANPSC110F Hierarchical and Multidrop Addressable JTAG Port

To obtain BSDL models, call **1-800-341-0392 x4500** and ask for the SCAN Applications group, or download from National's site on the World Wide Web: http://www.national.com.

Other Simulation Models

National recognizes that our end customers require simulation models of our devices.

The following companies offer various models for National products:

Synopsys/Logic Modeling, 503-690-6900, modelinfo@lmc.com
Zeelan Technology, 503-520-1000, zeelan@netcom.com
Quad Design/VIEWlogic, 805-988-8250, http://www.view.logic.com

Other Simulation Models (Continued)

Please contact *Logic Modeling* at the following locations:

U.S. HEADQUARTERS

19500 N.W. Gibbs Drive
P.O. Box 310
Beaverton, OR 97075
Tel: (503) 690-6900
Fax: (503) 690-6906
Tech. Product Support:
1-800-445-1888

LM Division

1520 McCandless Drive
Milpitas, CA 95035
Tel: (408) 957-5200
Fax: (408) 945-9181

VHDL Division

4500 East Pacific Coast Highway
Suite 210
Long Beach, CA 90804
Tel: (310) 494-4127
Fax: (310) 494-8106

European Headquarters

Doncastle House
Doncastle Road
Bracknell, Berks RG12 8PE
England
Tel: 44-344-300833
Fax: 44-344-300844

France

Immeuble Ampère
Rue Ampère
95300 Pontoise
Tel: 33-1-30-75-95-02
Fax: 33-1-30-38-45-70

Germany

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12607 Hidden Creek Way
Cerritos, CA 90701
310-926-6727

GenRad, Inc.

300 Baker Avenue
Concord, MA 01742-2174
1-800-4-GENRAD

Hamilton Hallmark

Technical Support Center
1-800-605-3296
http://www.tsc.hh.avnet.com

Hewlett Packard

815 S.W. 14th
Loveland, CO 80537
http://www.hp.com

JTAG Technologies

Eindhoven
The Netherlands
+31 40 7 82584

Synopsys Europe

Stefan-George-Ring 6
D-81929 Munich
Germany
011.49.89.99.59.12.30
http://www.synopsys.com

Synopsys N. America

700 East Middlefield Rd
Mountain View, CA 94043
1-800-445-1888
Logic Modeling Product Information
1-800-346-6353

Teradyne

321 Harrison Avenue
Boston, MA 02118
617-422-3567
http://www.teradyne/com

Test Economic Services

270 Hyde End Road
Spencers Wood
Reading
Berks. RG7 1DL

United Kingdom

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Boundary Scan Tools Available from National

- *Test Cost Spreadsheet Model for ASICs and Boards*—Floppy disk and documentation; helps calculate development costs; employs Excel spreadsheet and Macros.
- *SCAN Remote and Embedded System Test Demonstration and Developer Kit*—Hardware to borrow. Includes Test Master board with μP, RAM/ROM, and SCANPSC100 Embedded Boundary Scan Controller; backplane populated with slave cards containing SCANPSC110 JTAG Addressable Port (Bridge), SCAN CMOS Test Access Logic and SCAN ABT Test Access Logic. Demonstrates built-in self-test upon power up; backplane interconnect test; missing board test; board partitioning and test; download of new test vectors to RAM; live insertion of slave cards. LED displays included to allow boundary scan controller TAP states to be monitored during demonstration and development. Contact SCAN Applications Group at 1-800-341-0392 x4500.
- *1994 SCAN Tutorial Volume I*—Co-developed by Teradyne and National, it describes JTAG terminology, methods, applications for use.
- *The Economics of Design for Test*—Series of 3 articles, co-authored by Gary O'Donnell, National Semiconductor; Prof. Tony Ambler, Brunel University; R. G. Ben Bennetts, Synopsys; Harry Bleeker, JTAG Technologies. Identifies enabling technologies, barriers to adoption, clarifying the costs. Reprinted from *Evaluation Engineering Magazine* (9-11/94).
- *Live Insertion for SCAN and VME Gets Attention*—Article reprint from *Electronic Engineering* (12/94), on SCAN ABT Test Access Logic for live insertion applications.
- *IRIDIUM Satellite: A Large System Application of Design for Testability*—Article reprint from IEEE International Test Conference 1993. Discusses application of system-level boundary scan (based on the National SCANPSC110) in the Iridium satellite program.
- *Boundary-Scan-Based System Test: Comparing Two Approaches*—Article written by National that compare our SCANPSC110 Bridge with Texas Instruments' offerings. Published 3/94 in *Electronic Engineering*.
- *Six Good Reasons Why Boundary Scan Should be Designed into a Board*—Written by Alan Nelson, Marconi Instruments; advocates the benefits boundary scan provide at all steps of the product life cycle (design prototype through field repair). Presented at NEPCON 1994.
- For articles call 1-800-341-0392 x4500 and ask for SCAN Support.

Section 7

Application Notes

Section 7 Contents

Structural System Test via IEEE Std. 1149.1 with Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F

National Semiconductor
Application Note 1023
Mark Grabosky

INTRODUCTION

IEEE Std. 1149.1 (JTAG) defines a standard Test Access Port (TAP), protocol and set of commands for built in test at both the chip and board level. A board designed with boundary scan components typically consists of one scan chain which daisy-chain (TDO to TDI) all components on the board. While a single scan chain solution might be adequate for testing a board in production or a single-board system, it is not adequate when a multi-board system requires interconnects between boards be tested after system integration. A number of methods are available for accessing system level boundary scan nets. Traditional methods included using a multi-channel tester to physically access each board, using a single tester connection with each board's TDI and TDO traces daisy chained together or by multiplexing the TMS pins running to each board. An alternative approach is to implement an addressable test access controller such as the SCANPSC110. The SCANPSC110 eliminates the shortcomings of the traditional methods while also providing the capability to partition a single board level scan chain into smaller chains.

While it is possible to separate cables to each board during production test, it becomes unwieldy quickly as the number of boards increase. Furthermore a multiple port solution is not practical for use with embedded test.

Even though daisy chaining multiple boards together is simple, several drawbacks exist. For example, ATPG software for a multiple-board system views the system as if it were one board. As the system scales upward, the number of NETS become large as will the number and length of serial test vectors required. When a board is missing or empty on a backplane, or a fault occurs in the boundary scan infrastructure of any one of the boards, the entire system becomes untestable.

A multiplexed TMS scheme works well for partitioning a system and giving board test access through a single test port. But, it does not scale up well on a backplane, and there is no provision for backplane interconnect testing. Backplane interconnect testing required the ability to park a board in the Pause-DR/IR TAP states (See Section 2, *Figure 4* in the Scan Databook for explanation of TAP states) while accessing another board. It also requires a means for performing system wide updates of scan commands and data.

The PSC110F solution provides a simple means for tying independent scan chains from multi-board systems together and selectively accessing them. A six-bit addressing scheme allows for up to 59 bridges on a single backplane. Test vectors generated for testing the individual boards can be used for testing the boards after system integration as well as for embedded test in the field. The partitioning achieved by using the PSC110F will automatically isolate faults down to the board level with no diagnostics. The multiple local scan ports (LSP) allow for additional partitioning of scan chains within a board. Backplane interconnect testing is enabled through the PARKPAUSE command and broadcast addressing feature. ATPG software is easily implemented and is available through multiple venders.

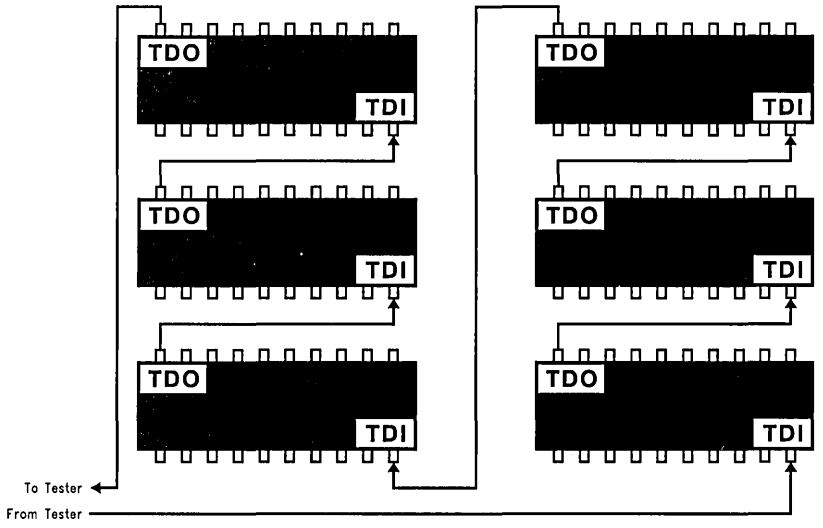

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FIGURE 1. Single Board Boundary Scan Implementation

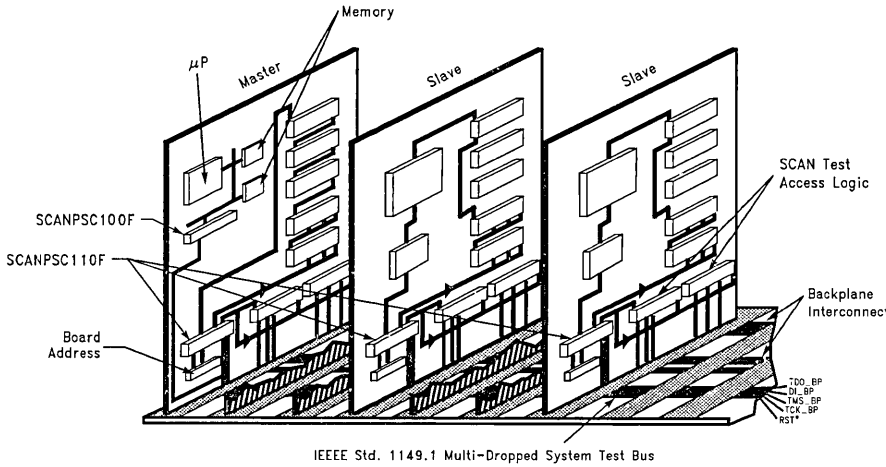

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FIGURE 2. SCANPSC110F Multidrop Configuration

SCANPSC110F APPLICATION EXAMPLE

For more information on this application example, refer to AN-1037 "Embedded IEEE 1149.1 Test Application Example."

Consider a system with a multidrop backplane. In general there are "N" slots. Some slots are populated with cards, others empty. There may be many different card types that may be used with this backplane, and there may be multiple cards of the same type used within this backplane for a given configuration.

The backplane architecture in this example is quite simple. Each of the N slots receive the same set of multidrop backplane signals. There are no active components on the backplane. However, there may be passive pull-up resistors to hold backplane signals high when tri-stated. The system test bus, (TDO_BP, TDI_BP, TMS_BP, TCK_BP, TRST_BP* (Asynchronous active low input)), is also connected to each slot in a multidrop configuration. Each card has a PSC110F connected to the system test bus, and a boundary scan interface (IEEE 1149.1 compliant drivers, latches, and transceivers such as SCAN18540T, SCAN18373T, SCAN182245T) connected to the system backplane.

SYSTEM WIDE INFRASTRUCTURE TEST

Infrastructure testing is always the first test that must be performed. At the system level, the infrastructure test consists of verification and determination of backplane configuration and then testing connectivity, identity and functionality of the components that make up the output scan chains which interface with the PSC110F LSP's.

VERIFICATION AND DETERMINATION OF BACKPLANE CONFIGURATION

This test sweeps the entire address range of the PSC110F and reads the captured value from the instruction register of a selected PSC110F. The PSC110F instruction register will capture the value "XXXXXX01", where "XXXXXX" represents the assigned address on the slot inputs. If the value scanned back matches the outgoing address, a PSC110F has been selected. A scanned back value of "11111111"would indicate that there is no PSC110F at the outgoing address, such as in the case of empty slot. These results can be used in one of two ways:

1. If the exact system configuration is known at test time, which is often the case in production, the results of the address range sweep can be compared to the known configuration. If a PSC110F is not found at an address where there should have been one, or if a PSC110F is found at an address where there should not have been one, the tester will report a failure.
2. If the system configuration is unknown at test time, the results from the address range sweep can be compared to a database containing all possible boards to determine what board types are present in the current configuration of the system. Later when interconnect testing of the cards and backplane is performed, this predetermined configuration is used to select the proper tests for the specific configuration.

LOCAL SCAN PORT INSTRUCTION TEST

After the system configuration is verified or determined, the test circuitry on each card must be tested. This is done by addressing each PSC110F unparking each of its LSP's, and scanning back the value captured by the Instruction Registers of each component in the local chains. A captured value of "01" in the least significant bits represents a functioning boundary scan component. In some cases the remaining bits of the Instruction Register capture are used to encode a pseudo ID code (e.g., components like National's SCAN18XXXT, SCAN18XXXA), and can be used to test for correct component placement. Optionally, the device identification register can be checked for each boundary scan component on the cards to check for correct component placement. The 18-bit SCAN ABT Test Access Logic SCAN18XXXA family includes the optional ID register, but some of the earlier boundary scan components were not equipped with the ID register.

BOARD LEVEL INTERCONNECT TESTING VIA SCANPSC110F

The individual boards or cards have already been tested during production. Re-testing after system integration is optional, but makes for a good QA check. In the case of embedded test that will be used for power on self test or periodic field testing, running go/no-go board level tests will enable built-in diagnostics down to the board level.

PSC110F Selection and Configuration

A. Select PSC110F by scanning an address into the PSC110F Instruction Register.

B. Configure the Mode Register for the appropriate local serial port network configuration for board test. If the board has only one scan chain connected to LSP1, the default configuration will be appropriate. If there are multiple chains connected to multiple LSPs on a board with interconnects running between the components of different chains, it is appropriate to unpark multiple LSPs to form what looks like one larger chain.

   The LSP network configuration is performed by:

   1. Scanning the MODESEL command into the selected PSC110F's Instruction Register.
   2. Scanning the appropriate value into the Mode register of the selected PSC110F.

C. Unpark the LSP by scanning the UNPARK command into the instruction register of the selected PSC110F.

Once the PSC110F is selected and its LSPs unparked, the connection is made between the tester and the target scan chains. The remainder of the board test consists of the same commands and test data that would be used for testing a board without the PSC110F with one exception:

The data for the PSC110F Instruction Register, Bypass data register, and PAD bits, must be added to the serial vectors.

The remaining steps for board test are:

D. Scan the SAMPLE/PRELOAD command into the target devices and the BYPASS command to the PSC110F.

E. Scan the first test vector into the boundary registers of the target devices.

F. Scan the EXTEST command into the target devices and the BYPASS command to the PSC110F.

G. Scan the next vector into the target devices; the captured results from the previous vector are shifted out as this vector is shifted in. This step is repeated until all test vectors for this board have been exercised.

H. Scan the GOTOWAIT command into the PSC110F instruction registers to return all PSC110F to the Wait-For-Address state where the next card can be addressed.

BACKPLANE INTERCONNECT TESTING

Testing the backplane is similar to testing NETS within a board with one exception. The nodes of the backplane NETS terminate at components that are connected to a different LSP on a PSC110F. (See *Figure 4*) For example in order to test the I/O lines of a multidrop backplane, say, with 3 cards, each card is connected to the test bus by its own PSC110F. The PSC110F provides the address information. One of the PSC110F's 3 LSPs (local scan ports) is connected to a backplane driver, such as National's SCAN ABT Test Access Logic, SCAN182245A. These drivers, in turn, are connected to the backplane itself, and thereby provide scan test operations for backplane interconnect testing.

Boundary scan ATPG software generates patterns with the assumption that the output cells of all of the components connected to a NET will be updated simultaneously. This assumption allows for one node to drive a NET during pattern i and another node to drive the same NET during pattern i + 1. If the update did not happen simultaneously at the two nodes, there could be significant periods of bus contention between the multiple outputs on a NET. Therefore, the Update-IR of the EXTEST command and all Update-DRs between patterns vectors (while EXTEST is the active command) must be performed simultaneously for all boards using the broadcast address on order to select all PSC110Fs on the backplane. In general, shifting operations must be done by addressing one PSC110F at a time.

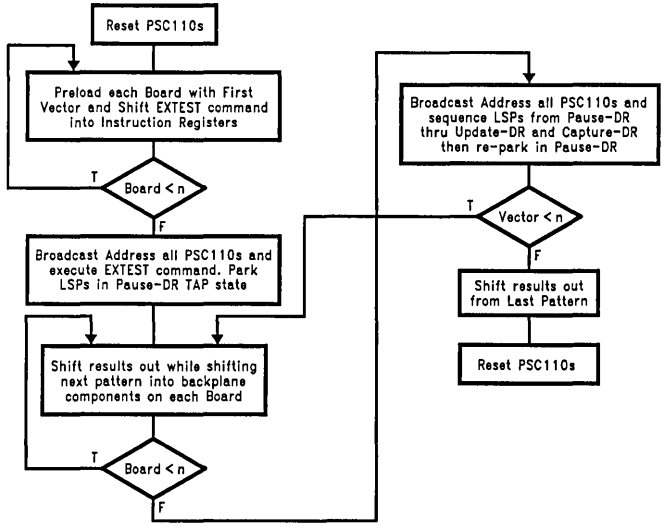

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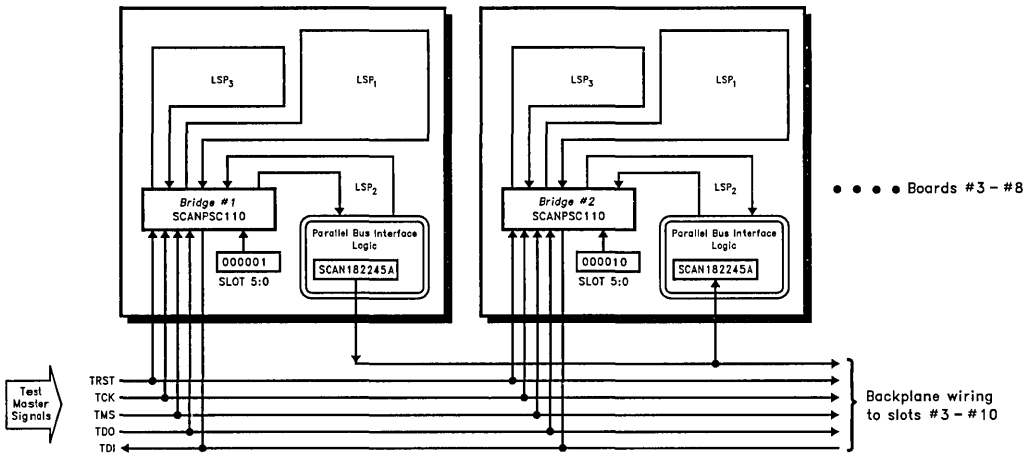
FIGURE 3. Backplane Interconnect Test Flow



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The PSC110F has 3 local scan ports. One port is connected to the backplane drivers. The other two partition the resident board.

FIGURE 4. Testing the Backplane Interconnects

A detailed description of the flow of the backplane interconnect test follows.

I. **Reset all PSC110F:** This can be performed by forcing TRST low or clocking TCK_BP five times while holding TMS_BP high.

II. **Configure/Preload:** Preload boundary scan registers of components connected to backplane signals on each card (i = 1 to n) with first test pattern, and shift EXTEST command into the Instruction Registers of all components that interface with the backplane signals.

A. Select PSC110F by scanning an address into the PSC110F Instruction Register.

B. Configure the Mode Register to unpark the LSP that interfaces to the backplane logic. This is not necessary if LSP1 is used (default configuration).

C. Unpark the LSP by scanning the UNPARK command into the Instruction Register of the selected PSC110F.

D. Scan the SAMPLE/PRELOAD command into the target devices and the PARKPAUSE command to the PSC110F.

E. Scan the first test vector into the boundary registers of the target devices. The TAP state sequence should go from Shift-DR to Exit1-DR through the Pause-DR state, after shifting the test vector, to avoid parking the LSP in the Pause-DR state (see PARKPAUSE command in the SCANPSC110F data sheet).

F. Shift the EXTEST command into the target devices and the GOTOWAIT command to the PSC110F. The TAP state sequence should go from Shift-IR to Exit1-IR to Update-IR, after shifting the commands, so that the active LSP will be parked in the Pause-IR state.

G. Repeat for each board involved with the backplane test.

III. **Execute EXTEST Command:** The EXTEST command is updated to all backplane components simultaneously to avoid significant periods of bus contention that would result from executing the EXTEST command one board at a time.

A. Select all PSC110F by scanning the broadcast address into the PSC110F Instruction Registers.

B. Scan the UNPARK command into the Instruction Register of the selected PSC110F. The LSP will not actually be unparked until the backplane TAP is sequenced back into the Pause-IR state, while the UNPARK command is active.

C. Scan the PARKPAUSE command into the PSC110F instruction register. The TAP state sequence should go from Shift-IR to Exit1-IR through the Pause-IR state, after shifting in the PARKPAUSE command. The LSP will unpark upon entering the Pause-IR state. The EXTEST command had previously been shifted into the Instruction Registers of the target devices and will become the active insruction once the LSP is unparked and sequenced through the Update-IR state.

D. Capture the logic values on the inputs of the target devices and park the LSP in the Pause-DR state by sequencing the backplane TAP's through Capture-DR to Exit1-DR to Update-DR.

E. Scan the GOTOWAIT command into the PSC110F Instruction Registers.

IV. Shift Test Data: Test results from the previous pattern are shifted out while the next pattern is shifted into the boundary registers of the components on each board in the system. Ater the data is shifted, the LSP is parked in the Pause-DR TAP state so that the boundary register contains the new data, but has not yet updated the value in its output cell.

A. Select a PSC110F by scanning an address into the PSC110F Instruction Register.

B. Scan the PARKPAUSE command into the Instruction Register of the selected PSC110F. (The PARKPAUSE command is used to unpark the LSP as well as to park the LSP).

C. Sequence the backplane TAPs into the Pause-DR state in order to unpark the LSP.

D. From the Pause-DR state, transition to Exit2-DR to Shift-IR, where the next test vector is shifted into the target devices, then to Exit1-DR to Update-DR. The LSP will be reparked in the PAUSE-DR state when transitioning from Exit1-DR to Update-DR, because the PARKPAUSE command is still active.

E. Scan the GOTOWAIT command into the PSC110F Instruction Registers.

F. Repeat for each board involved in the backplane test.

V. Drive/Capture: All PSC110F are selected and their LSPs that interface to the backplane components are unparked and sequenced through the Update-DR and Capture-DR states.

A. Select all PSC110F by scanning the broadcast address into the PSC110F Instruction Registers.

B. Scan the PARKPAUSE command into the Instruction Register of the selected PSC110F.

C. Sequence the backplane TAPs to the Pause-DR state in order to unpark the LSP.

D. Sequence from the Pause-DR state through Update-DR through Capture-DR to Exit1-DR to Update-DR. This will execute the next vector and repark the LSP in the Pause-DR state.

E. Scan the GOTOWAIT command into the PSC110F Instruction Registers.

VI. Shift Out Test Results from Last Vector: The test results from the last vector are shifted out while shifting in a safe dummy vector, one that tri-states the bus.

A. Select a PSC110F by scanning an address into the PSC110F Instruction Register.

B. Scan the PARKPAUSE command into the Instruction Register of the selected PSC110F. (The PARKPAUSE command is used to unpark the LSP as well as to park the LSP).

C. Sequence the backplane TAPs to the Pause-DR state in order to unpark the LSP.

D. From the Pause-DR state, transition to Exit2-DR to Shift-IR, where the results of the last test vector are shifted out, to Exit1-DR to Update-DR. The LSP will be reparked in the Pause-DR state when transitioning from Exit1-DR to Update-DR, because the PARKPAUSE command is still active.

E. Scan the GOTOWAIT command into the PSC110F Instruction Registers.

VII. Reset Test Logic: This can be performed by clocking TCK_BP eight (8) times while holding TMS_BP high. It takes three (3) clocks to reset the PSC110F from the Run-Test/Idle state and five (5) more to reset the target components from the Pause-DR state. In general, it takes five (5) TCK's for each level of test hierarchy.

Boundary-Scan, Silicon and Software Enable System Level Embedded Test

National Semiconductor
Application Note 1022
Mark Grabosky

ABSTRACT

Designing IC's, boards, and systems with a DFT strategy that utilizes boundary-scan, will make a quantum improvement in test development cycle-time, and fault coverage both in production and in the field. Tools are commercially available that automate design, test development, and ultimately embedded test for IEEE 1149.1 compatible systems. This paper is intended to familiarize designers and test engineers with the advantages of boundary-scan at the system level as well as present the architectural and implementation challenges of developing National's SCAN EASE software. For more information, refer to AN-1037, "Embedded IEEE 1149.1 Test Application Example."

INTRODUCTION

Boundary-Scan Fundamentals

The terms, 1149.1, 0.1, Boundary-Scan, and JTAG, are used synonymously in the industry and throughout this paper.

IEEE Std 1149.1 defines a standard architecture for designing Boundary-Scan test circuitry into digital integrated circuits for the purpose of testing the IC and the interconnections between IC's on a board or module. All 1149.1 compliant devices must have a Test Access Port (TAP) with 4 required pins: Test-Data-Input (TDI), Test-Data-Output (TDO), Test-Mode-Select (TMS), and Test-Clock (TCK). A fifth pin for Asynchronous Test Reset (TRST*) is optional (* means active low). See *Figure 1.*

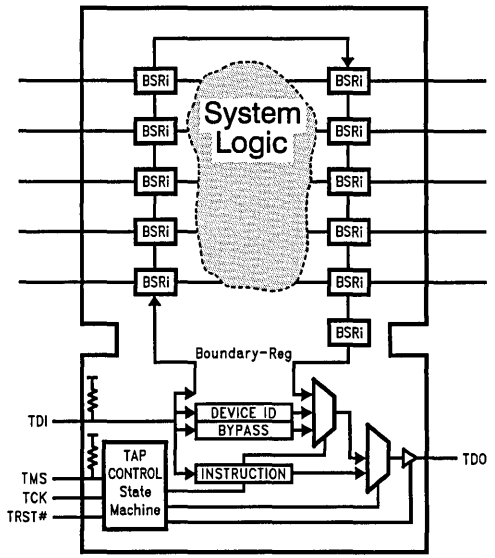

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FIGURE 1. Device Hardware

The boundary register is integrated into the input/output cells of the device. While in Interconnect Test Mode (Extest command is active) data shifted into the boundary registers' output cells is driven onto the outputs; and data driven onto the device's inputs is sampled by the input cells and shifted out for comparison to expected results. This simple process of shifting data, updating output cells, and sampling input cells, is the basic algorithm for board level interconnect fault testing.[1,2,3]

BOARD LEVEL BOUNDARY-SCAN TEST COVERAGE

At the board level, boundary-scan components are daisy chained (TDI to TDO) to form a single scan chain. See *Figure 2.* Boards comprised of 100% 1149.1 compliant components, can be tested with a vector set generated by ATPG (Automatic Pattern Generation) software to 100% fault coverage with a 4-wire JTAG tester, while achieving a quantum reduction in test development time and eliminating the need for expensive in-circuit testers. In addition, faults are automatically isolated to the NET, and in the case of opens, to the node (unit/pin).

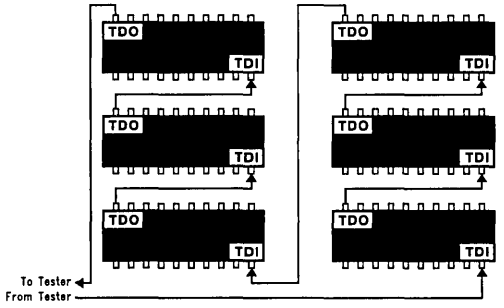

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FIGURE 2. Simple Board Boundary-Scan Implementation

Boards that do not have 100% boundary-scan components can greatly benefit from this methodology also. In fact, even a single chip with boundary-scan will simplify the test development effort, and may improve the testability of the board. Especially if the boundary-scan component is a complex sequential device. For this reason, boundary-scan has become a required feature of microprocessors, FPGAs and ASICs for many board manufacturers.

The boundary-scan cells are often called "virtual nails" or "silicon nails", since they provide the same capability as physical test points in a bed-of-nails fixture.[3] The task of generating board level fault tests for a device with boundary-scan is greatly simplified. Because each device pin can be sampled and/or forced by its boundary-cell, no knowledge of the on-chip system logic is required for fault testing the board. In an in-circuit test environment, assuming that the tester has bed-of-nails access to all of the NETs the

device is connected to, a stuck-at-one test is performed on all NETs with only one vector. To provide the stimulus, simply force all input NETs low via the physical nails and shift all lows into the devices output boundary-cells (via TDI) to drive the virtual nails low. To check the response, sample all output NETs via the physical nails and shift the data captured by the input boundary-cells (virtual nails) out on TDO.

If the response is all lows, the test passes, otherwise the test fails. Similarly, a stuck-at-low test requires just one vector. Bridging faults are isolated using a binary search algorithm. For Example, 3 vectors are required to test for bridging faults on a board with 8 NETs as shown in Table I:

TABLE I

Vector	N1	N2	N3	N4	N5	N6	N7	N8
1	0	0	0	0	1	1	1	1
2	0	0	1	1	0	0	1	1
3	0	1	0	1	0	1	0	1

The number of vectors to detect and isolate 100% of bridging faults is equal to:

$$Num\_Vectors(bridging) = \frac{\log NETS}{\log 2}$$

and

$$Num\_Vectors = \frac{\log NETS}{\log 2} + 2$$

Therefore, a chip with 64 system inputs/outputs each connected to a separate NET, 64 NETs, would require 6 vectors for bridging faults. Added to the 2 vectors required for stuck-at faults, a total of 8 vectors is required. Because of the exponential nature of the calculation, the simplicity is even more evident when a larger number of NETs are being tested. A board with 1,000 NETs requires 12 vectors; a board with 1 million NETs requires just 22 vectors.

Compare this to the number of vectors required to test a board with non-JTAG compliant IC's. If the device is simply combinatorial, it can be tested with 2^N Vectors (256 for 8 NETs). If the functionality is studied, the vector set may be greatly reduced, but this requires functional models and/or test development resources. The problem becomes even more complex when testing a sequential device. Several set-up vectors are typically required to condition a device to test an input, and several vectors may be required to propagate the fault to an output for observation.

The IEEE 1149.1 standard also defines a syntax, *Boundary-Scan Description Language* (BSDL), for describing the IC's pin-out, and the specific implementation of its test circuitry (e.g. boundary-register, optional registers, command set and opcodes).[4] BSDL files are provided by the manufacturer of 1149.1 compliant devices.

TEST DEVELOPMENT PROCESS

At the board level, generating tests for boundary-scan NETs is completely automated. ATPG requires only a NET list of the board, and BSDL models for each 1149.1 compliant device on the board. Additional information can be provided to the ATPG such as a NET information file to force a NET to always be driven high or low. For boards with less than 100% boundary-scan components, fault coverage can be increased by adding cluster tests to the vector set. Cluster tests are generated the same way as in-circuit tests for non-scan components. In the case of cluster testing, the stimulus is driven from, and the response is sampled by, the "virtual nails" of scan components that surround the cluster. Using this approach it is possible to achieve a high level of fault coverage even when several non-scan components are used. Of course, physical test points can be added to untestable NETs.

Further benefits are realized at system integration and field testing. Traditionally, functional testing was used here due to the complexity of obtaining physical access to test points with in-circuit testers. Functional test development requires a separate and complex effort. Intimate knowledge of the system functionality is required and fault isolation is typically poor. Using a boundary-scan approach, backplane interconnect tests and board tests are automated. Fault isolation is precise and the only tester access required is to the 4-wire scan chain.

SYSTEM LEVEL JTAG TESTING

Typically, boards are designed with only one scan chain. At system integration, the scan-chain of each board must be tied into the backplane architecture. The backplane could be designed so that the chains of each board would be daisy-chained to form a single system wide chain. This is undesirable for several reasons. Boards cannot be removed without breaking the chain; boards must be located in specific slots; a fault in the chain of one board would leave the entire system untestable. The preferred method for connecting the board level scan-chains to the backplane is a multi-drop backplane design with a JTAG addressable device on each board interfacing the backplane test bus to the board level scan-chains.

National's hierarchical and multidrop addressable JTAG Port, SCANPSC110F, provides this functionality.[2] See *Figure 3.*

Unlike other approaches, the PSC110F provides an addressing scheme using 1149.1 compatible protocol. A PSC110F is selected by shifting a 6-bit address into its instruction register that matches the value hardwired on its slot inputs, when in the Walt-for-Address state. Refer to the SCANPSC110F datasheet for detail.

The PSC110F also enables further partitioning of the board level scan-chains. Each PSC110F provides 3 Local Scan Ports (LSP) that can be configured to be connected individually to the test bus, or simultaneously in series to the test bus. This flexible LSP configuration helps partition hardware and simplifies the ATPG vectors. For example, LSP1 could be connected to all devices that interface to the backplane. LSP2 could be connected to all other on-board devices. LSP3 could connect to a mezzanine board. To test the mezzanine board, only LSP3 must be unparked. To test the interface between the board and the mezzanine board, LSP2 and LSP3 must be unparked. To test the board, LSP1 and LSP2 and to test the backplane interconnect, only LSP1 must be unparked. If NET lists are captured for each of these hierarchical views of the system, a separate test can be generated for each view resulting in a set of test partitions that can give an immediate indication as to which part of the system failed. This structured test methodology is particularly useful for embedded system test where diagnostic processing is limited. For more on backplane interconnect testing, refer to AN-1023, Structural System Test via IEEE Std. 1149.1 with SCANPSC110F.

EMBEDDED SYSTEM LEVEL JTAG TEST

Traditionally embedded or built-in self-test of non-boundary-scan designs, as in the case of system integration testing, was limited to functional testing. Here, a separate test development effort was required. However, the advantage of a boundary-scan design is that the test points are built into the system logic. In addition, all of these "virtual nails" are accessible via a 4-wire test-bus. In fact, with slight modification, the same board tests that were used in production test can be reused for embedded test.

Figure 4 shows the test development process from start to finish. Production tests are generated for each board in the system. One or more additional tests are generated for backplane interconnect testing. These tests are typically stored in tester specific formats such as SVF or PAT. These non-compact ASCII vector formats are fine for production testing, but the memory limitations of an embedded system make them undesirable for embedded test. Therefore, the tests are converted to Embedded Vector Format (EVF), a compact binary format defined by National, using SCAN EASE. Refer to the SCAN EASE datasheet.

Header information is stored along with each test so that when the test is executed, and fails, the failure can be isolated to the partition described in the header. The EVF partitions for several boards can be appended into one file and embedded on system PROM for power-up self-test, or they can be down-loaded to the system via a serial communication link.

EMBEDDED VECTOR FORMAT

EVF was defined under the constraints of being a compact binary format that is highly structured to be easily parsed by the embedded code, and independent of system architecture and memory organization such as little-endian, big-endian, 8-bit, 16-bit, 32-bit, 64-bit wide. To achieve the requirement of being memory organization independent, it was necessary to define EVF as a contiguous array of bytes. All architectures examined had one thing in common: a single byte of data can be addressed anywhere in memory and read into a byte-wide register, regardless of memory organizations. Larger data-types such as words or double-words, are in some cases required to be word or double-word aligned, respectively.[6] Also, reading a word stored in little-endian format on a big-endian machine would require the LSB and MSB to be swapped. A set of data structures were defined for each EVF record type.

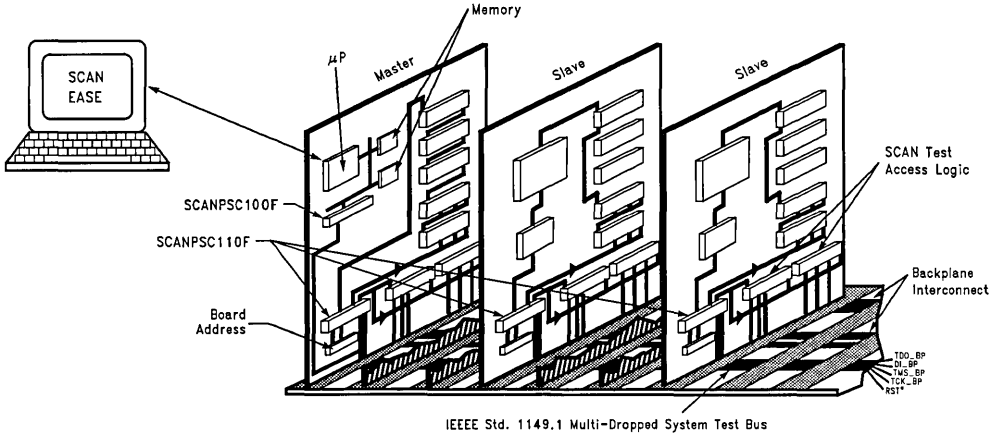

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FIGURE 3. Multidrop Configuration Using Boundary-Scan

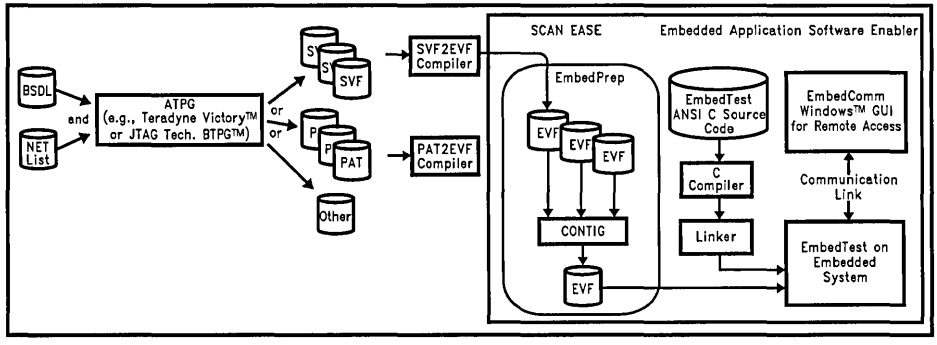

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FIGURE 4. Test Development Process

A typical data structure is:

```
/* evf_scan is used to parse SIR, SDR records */
struct evf_scan {
  unsigned char opcode;    /* EVF_SIR, EVF_SDR */
  unsigned char options;   /* Mask, TDO, TDI, Flag */
  LE_LONG num_bits_le;     /* Scan-Chain Length */
};
```

The actual test data immediately follows the data structure. Pointers to the outgoing TDI data, the expected TDO data, and the mask, are calculated from the options field and the scan-chain length. Note that the type LE_LONG must be used for reading/writing a 4-byte data type in order to make EVF, architecture independent.

```
typedef struct {
  unsigned char byte0;
  unsigned char byte1;
  unsigned char byte2;
  unsigned char byte3;
} LE_LONG;
```

EMBEDDED TEST APPLICATION CODE

The SCAN EASE application code was defined to be modular (see *Figure 5*), portable to most computer architectures and efficient, from both a code size and performance perspective. The code was written completely in ANSI C. The embedded test code was developed top-down in 5 modules. Additionally a communications module was developed to give a "truly" embedded system a means to communicate to a system administrator, or remote computer via modem.

The top layer of code is where hardware/software initialization is performed. Calls to the Pg_ctrl level are made to form test activity. A call to the Pg_ctrl function: InitTestTable(P_evf_bist) creates a linked list of table entries that contain a pointer to the EVF partition, whether it resides in RAM or ROM, a pointer to the datalog, and pass/fall information. A Table entry is added each time a new test is downloaded, AddTableEntry(), and updated each time a test is run, RunPartition(p_table_entry).

Calls to Evf_lib are made from RunPartition(). RunPartition() reads each EVF op-code and calls the appropriate evf_lib function to parse and execute that command. Evf_lib functions include: EvfScanDr(), EvfScanIr(), EvfState(), etc. EvfScanDr(p_evf_record), for example, determines if the record contains TDI, TDO, or MASK data by looking at bit-wise flags in the options field of the record, using the evf_scan data structure. If these flags are set, pointers to the data arrays are calculated and stored as statics. If the flags are not set, the function determines whether or not to use the previous vectors data. This enables vector compression and is typically useful for the mask data, whose value is usually constant from vector to vector for the duration of a board test. The options field is also used to determine whether or not to sample data returning from the scan-chain for comparison against an expected response.

Scanlib is where the 1149.1 intelligence resides. Scanlib functions include ScanDr(), ScanIr(), State(), etc. and are called from evf_lib. For example, ScanDr (p_outgoing_data, num_bits, p_incomming_data) determines the sequence of the TMS needed to progress the target TAPs from their present tap state to Shift-DR, and then from the Exit1-DR state to the End_IR state. Calls are made to the SCANPSC100F device driver (pscdrv) to actually sequence the target TAPS, SequenceTms(), and shift the data to and from the scan chains, Shift().

The SCANPSC110F driver, pscdrv, was written in direct support of National's Embedded Boundary-Scan Controller SCANPSC100F. Alternatively, a device driver written for a micro-controller parallel port, an I/O register, or other competitive devices, could be integrated into this software.

As previously mentioned, one constraint on this code is that it must be portable to most computer architectures. In some architectures, the SCANPSC100F may be memory-mapped, in others it may be mapped into I/O space. In the case of memory-mapped I/O devices, reads and writes to the device are made simply be equating a volatile variable located at the physical address space in which the device resides, (volatile)Tms = tms. If the device is I/O mapped, a function call is typically required, since C operands do not directly support I/O address space, WriteTms(tms).

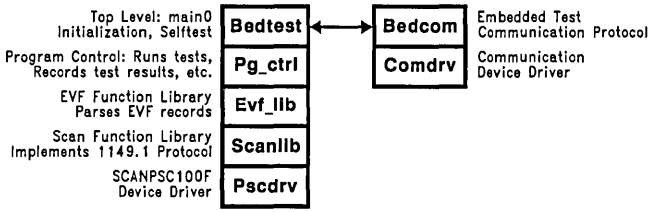

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FIGURE 5. SCAN EASE Code Is Modular

```
/* Macro's for Memory Mapped I/O */
#if BSM_TYPE == MEM_MAPPED
  #pragma sep_on segment psc100 class shadow
    volatile unsigned char Filler_byte;
    volatile unsigned char Psc_base;
  #pragma sep_off
  #define WRITE_PSC(PSC_REG_OFFSET, DATA)  * (unsigned char
    *) (&Psc_base + PSC_REG_OFFSET) = DATA
  #define READ_PSC(PSC_REG_OFFSET) *(unsigned char
    *) (&Psc_base + PSC_REG_OFFSET)
#endif

/* Macro's for I/O Port Mapped I/O */
#if BSM_TYPE == IO_MAPPED
  #define PSC_BASE 0x140
  #include <dos.h>
  #define WRITE_PSC (PSC_REG_OFFSET, DATA)
    outportb ((int) (PSC_BASE + PSC_REG_OFFSET), DATA)
  #define READ_PSC(PSC_REG_OFFSET) inportb((int) (PSC_BASE +
    PSC_REG_OFFSET))
#endif

/* If compiling for Corelis board, use Corelis low level
    driver for PSC100 */
#if BSM_TYPE == CORELIS_BOARD
  #include "cortest.h"
  #define PSC_BASE 0x140
  #define WRITE_PSC (PSC_REG_OFFSET, DATA) write_psc(0,
    PSC_REG_OFFSET, DATA)
  #define READ_PSC (PSC_REG_OFFSET) read_psc(0,
    PSC_REG_OFFSET)
#endif
```

These two cases are handled using a conditionally defined macro. This is the only conditional define in the code, and the only thing that may change when compiling for one architecture verses another.

Note that the above code also includes an option to define WRITE_PSC and READ_PSC to call functions for a Corelis ISA card, PC-1149.1/100F, High Speed PC-AT Bus Boundary-Scan controller. This option was extremely helpful in that it enabled the code development and debug to be performed on a PC, with a SCANPSC100F mounted on an ISA card, using a high level debugger. Once the code was debugged, it could be compiled for the target embedded system resulting in a great reduction in debug time of the embedded environment.

SUMMARY

A DFT strategy that utilizes boundary-scan components whenever available, will reduce test development cycle-time, increase fault coverage, reduce test time, and enable system level embedded test. Production tests can be reused for embedded (built-in) test and tools are available that automate this process. National provides components such as the Embedded Boundary-Scan Controller, SCANPSC100F, and the Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F Bridge, that enable system wide embedded scan testing. With the SCAN EASE software described in this paper, the task of implementing embedded scan test has become virtually an "off the shell" solution.

REFERENCES

[1] IEEE Std. 1149.1-1990, *"IEEE Standard Test Access Port and Boundary-Scan Architecture"*, IEEE Computer Society, 1990.

[2] NSC *"SCAN Databook"*, National Semiconductor, 1996.

[3] NSC, *"Scan Tutorial Handbook Volume I"*, National Semiconductor, 1994.

[4] IEEE Std. 1149.1-1990 Sup. B, *"Boundary-Scan Description Language"*, IEEE Computer Society, 1990.

[5] Eichelberger•Lindbloom•Waicukauski•Williams, *"Structured Logic Testing", Prentice Hall, 1991.*

[6] Motorola, *"M68000 Microprocessor User's Manual"*, Motorola 1990.

Embedded IEEE 1149.1 Test Application Example

National Semiconductor
Application Note 1037

This application example discusses the implementation of embedded, system level boundary scan test within an actual design, the National boundary scan demonstration system. Its intent is to describe the decisions, actions and results when applying boundary scan and National's SCAN EASE Software within a system. For more information see also AN-1022, "Boundary Scan Silicon and Software Enable System Level Embedded Test."

HARDWARE DESCRIPTION

The National boundary scan demonstration system is comprised of a multidrop backplane which interconnects a processor card to several system I/O cards. The backplane contains a 16-bit data bus, a 16-bit address bus and several control signals routed to six connectors. The processor card consists of a processor core which includes a Motorola 68302 μP, boot EPROM and working SRAM, a RS232 port for remote communication, a parallel backplane interface and an auxiliary parallel port. The I/O cards, each sharing an identical architecture, include a 16-bit LCD display, an on board EPROM which stores LCD messages, and a backplane interface. Each I/O card also contains logic which multiplexes data, from either the backplane or EPROM, to the display.

The number of I/O cards can vary within a given system. While five backplane I/O card connectors are available, only 2 of the 5 slots are typically populated with I/O cards. The multidrop (i.e. parallel) backplane architecture enables cards to populate any of the five connectors and allows connectors to remain empty. Board addressing is used to select cards for functional operation.

Functionally, the system is designed to display messages and system status information using the LCD display located on each I/O card. This message and status information is driven from the processor card, via the system backplane, or from EPROMs local to each I/O card. To demonstrate the features and functions of boundary scan, the system also contains LEDs which display the status of boundary scan activity.

TEST OBJECTIVES

The fundamental test objective for the National demonstration system was to utilize techniques which could be applied over the life of the product, including development, manufacturing and in-field operation. With effective prototyping to ensure functionality and timing performance, printed circuit board (PCB) structural faults, resulting from manufacturing errors or in-system board stress (e.g., temperature changes or mechanical stresses), were the primary focus. Boundary scan was seen as an effective means of detecting and diagnosing printed circuit board failures at all stages of the product's life cycle.

A specific area of concern during the development of the test strategy was system level test. Typically, limited tester access forces system test to rely on functional patterns to test for even simple interconnect failures. This leads to very complex test patterns, poor fault coverage and very difficult failure diagnostics. More importantly, the functional test routines depend on sound interconnects between components to be effective. Embedded, system-level boundary scan was perceived as a way to replace many of the functional tests with simple and easily diagnosable tests.

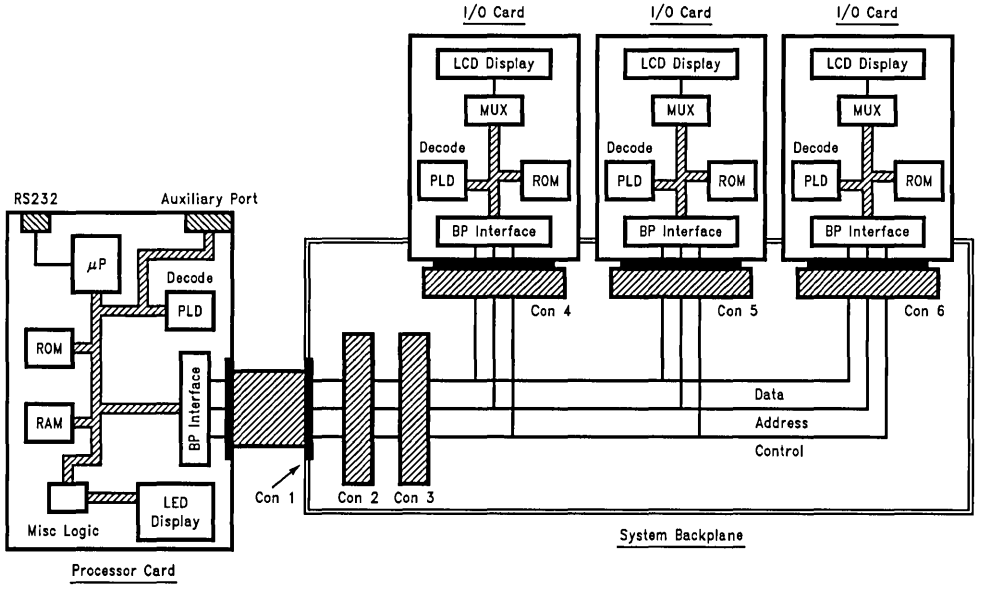

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FIGURE 1. Demonstration System Layout

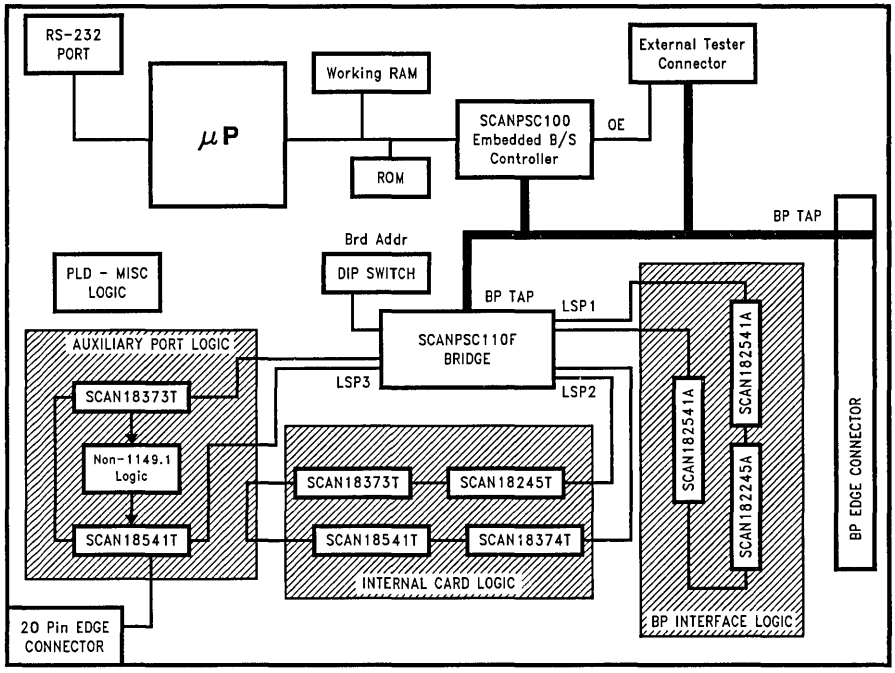

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FIGURE 2. Demonstration Processor Card

Boundary scan was viewed as only a part of the complete test solution. Functional test routines were still required to test system memory and confirm effective μP-to-system peripheral communication. Using the two techniques together maximized test effectiveness while reducing test development efforts.

IEEE 1149.1 COMPLIANT SYSTEM ARCHITECTURE

To accomplish the boundary scan test objectives, the 1149.1 test strategy covered three aspects of the system: board and backplane boundary scan test points, system level boundary scan access and embedded boundary scan control.

Board and Backplane Test Points

The first step in implementing boundary scan is to integrate 1149.1 compliant components into the functional design. Maximizing the percentage of nets covered by boundary scan reduces the cost of other techniques and equipment like in-circuit testers, while increasing the ability to apply the benefits of boundary scan at later phases of the product's life cycle. In the case of the National demo system, boundary scan was included on nearly every logic IC which populated the processor card and I/O cards.

To support backplane interconnect testing, National's 18-bit SCAN ABT Test Access Logic components were implemented at the backplane interface on both the processor card and I/O cards. Using 1149.1 compliant SCAN ABT logic (SCAN182245A) provided the required backplane test points while also creating a hot insertable[1] backplane interface. The hot insertable interface allowed failing processor or I/O cards to be removed or inserted without powering down the system.

To increase the structural fault coverage on nets connected to devices which are not available with boundary scan, a "cluster test" can be implemented. A cluster test relies on at least two boundary scan components and a functional knowledge of the cluster (i.e., cluster of devices) connected between them. Using one 1149.1 compliant component to drive test vectors to the cluster and the other to receive expected data from the cluster, the structural integrity of the cluster can be evaluated.

As the number and complexity of components increases, the development of test vectors becomes more difficult and diagnostic resolution increases. Within the demo system, a cluster test was implemented on the processor card's auxiliary port (see *Figure 2*).

On future demo design revisions, boundary scan will be expanded beyond the logic components to include an 1149.1 compliant microprocessor and programmable device (i.e., integrating the separate, non-1149.1 programmable devices into a single 1149.1 FPGA or CPLD). These additions will continue to drive the structural fault coverage towards 100% and also provide non-test capabilities, such as μP emulation and in-system FPGA programming via the JTAG port.

System Level Boundary Scan Access and Partitioning

With the 1149.1 components placed on the processor and I/O cards, the next objective is to interconnect the 1149.1 component TAP signals—TMS, TCK, TDI, TDO and TRST—at both the board and system levels. For the National demo design, this task was accomplished by adding a 5-bit bus to the backplane design and placing a National Hierarchical and Multidrop Addressable JTAG Port,

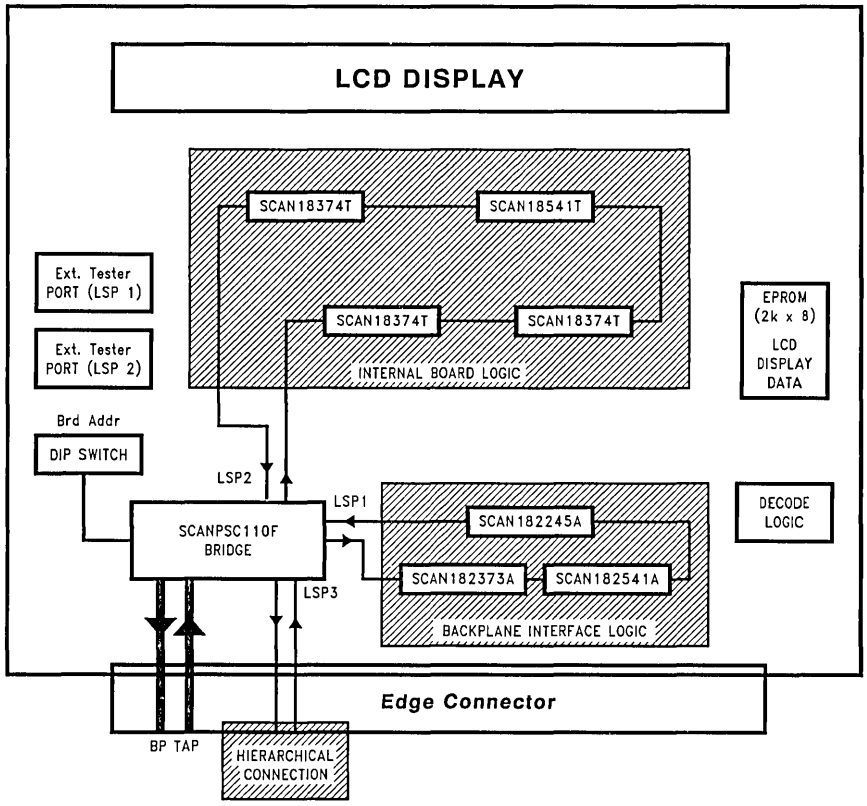

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FIGURE 3. Demonstration I/O Card

SCANPSC110F bridge, component at the backplane interface of the processor card and each I/O card. The SCANPSC110F bridge provides two key features to efficiently interconnect and partition a 1149.1 compliant system:

- **System Level Partitioning:** The SCANPSC110F bridge provides an addressable, multidrop interface to a single backplane TAP bus. This multidrop TAP interface is a perfect fit for this application because it preserves the ability for cards to be placed in any of the backplane connectors and for connectors to be left empty without requiring an entirely new set of boundary scan test vectors. Using a 1149.1 protocol, each SCANPSC110F bridge and, in turn, each board, can be addressed to participate in boundary scan test operations.
- **Board Level Partitioning:** Typically, board level boundary scan components are connected to form a single chain. The SCANPSC110F bridge provides three local scan ports (LSPs) which allows board level components to be partitioned into smaller, more manageable chains. Using the SCANPSC110F bridge's internal data registers, the LSPs can be configured to individually connect a single scan chain to the backplane TAP or to simultaneously connect up to three scan chains in series with the backplane TAP.

The ability to partition a board and system using the SCANPSC110F bridge simplifies test development, improves test efficiency and allows failures to be diagnosed to the partition level without using an off-line diagnostics tool. However, these benefits are only realized if the 1149.1 components are intelligently grouped and connected. The objective for testing the demo system was to test each board as a separate entity and to test the interconnects between the boards (i.e., the backplane). Enabling each board to be tested separately was easily accomplished when the SCANPSC110F bridge was placed at each card's backplane interface and connected to a system wide backplane TAP. With this interface, the tester TAP signals could be applied to each board separately.

With exclusive access to each board, the next critical task was to select which board components were grouped and connected to the SCANPSC110F bridge LSPs. Again, the test objectives were considered. To enable the development of an efficient, backplane specific boundary scan test, the 1149.1 compliant backplane interface components on each card were exclusively assigned to a single LSP. To group and assign the remaining 1149.1 compliant, board-level components to the other two SCANPSC110F bridge LSPs, each board type was viewed separately.

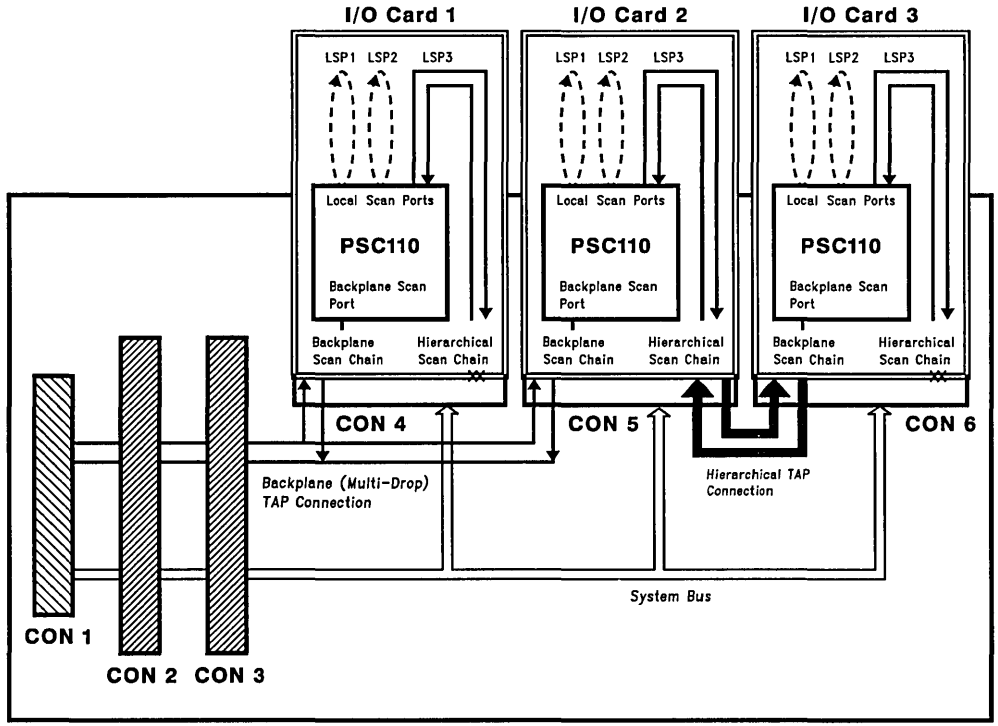

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FIGURE 4. Backplane—Hierarchical Connection

For the processor cards, the remaining compliant components were grouped an an internal logic chain and an auxiliary port logic chain. As with the backplane partition, these groups were selected to enable the development of group specific tests. The auxiliary port is intended to support a connection to a 1149.1 compliant sub-system. Assigning the port's compliant components to a unique LSP allows tests to be generated specifically for this port (and what is connected to it). The internal logic covers all other board level 1149.1 compliant components.

A similar component group was implemented for each I/O card. The internal card logic was grouped and assigned to one LSP while the other LSP was connected directly back to the backplane connector in order to provide a hierarchical connection. A hierarchical bridge connection is realized by connecting one SCANPSC110F bridge's LSP to a second SCANPSC110F bridge's backplane interface TAP. Hierarchical connections enable board scan chains to be split into more than the three chains supported by a single bridge. Hierarchical connections also enable a system to be partitioned into addressable sub-systems. In the case of the demonstration design, the hierarchical configuration was implemented to show the concept and addressing scheme required to address a bridge and its LSPs hierarchically. Since each I/O card shares an identical architecture, each I/O card's LSP3 connects directly to the backplane edge connector. The hierarchical connection is then realized using backplane routing between Con 5 and Con 6 (see *Figure 4*).

Embedded Boundary Scan Test Control

The final step of a boundary scan hardware design is to provide the means to apply and evaluate the boundary scan test vectors. For boards and systems which are tested using an external tester, the hardware implementation simply involves adding an applicable tester interface; e.g., additional pins on the edge connector, a special purpose connector/header or vias for ICT probes. For boards and systems which don't permit physical access, and/or require self-test or remote test capability, the test control must be embedded within the system.

For designs which require embedded test control, the optimal hardware implementation is one which enables both embedded and external tester access. This allows the design to benefit from the strengths of each method. The external tester offers the best means of developing tests for hardware debug and manufacturing. Using the ATPG and diagnostic tools provided with the external tester, tests can be easily developed and modified. Once the tests have been applied, failures can be diagnosed to the net or pin level automatically. With the tests finalized, and the boards/system tested, the tests and control are embedded to provide self-test and remote test access capability.

The National demo system hardware was designed to support both embedded and external test application. With the ability to address each demo card separately using the SCANPSC110F bridge, embedded and external access was only required on the processor card. The processor card then acted as the master to test each card and the backplane.

- **Embedded Test:** The embedded test capability for the demo system was implemented using the processor card's μP and the National SCANPSC100F Embedded Boundary Scan Controller. The SCANPSC100F provides an efficient, asynchronous interface between the μP's parallel data bus and the serial 1149.1 TAP, and is fully supported by the SCAN EASE software tools. The generic, asynchronous interface allows SCANPSC100F to interface with a wide range of processors and operate independent of the processor's operating frequency. The microprocessor views the SCANPSC100F as a standard I/O device.
  The processor card provided two options to initiate and evaluate embedded tests. For a power-on or post-reset self test, an LED display block was included with a separate LED for each card in the system. To initiate/evaluate tests remotely, the UART on the microprocessor was configured to provide an RS232 interface and an RS232 connector was added to the processor card. This remote interface also allows new tests to be downloaded and results to be uploaded.
- **External Test:** To provide system level access to an external tester, a connector was added to the processor card. In addition to the required tester signals, this connector included a sense line tied to the output enable pin on the SCANPSC100F. When the external tester was connected, the sense line was pulled high disabling the TAP pins on the SCANPSC100F. This, in turn, disabled the embedded tester and allowed the external tester, alone, to control the system TAP.

Figure 2 shows the high level connection between the μP, SCANPSC100F and external connector.

IEEE 1149.1 TEST EQUIPMENT

Hardware

A wide range of 1149.1 compliant testers are commercially available, ranging from in-circuit testers to PC-AT cards. For the demo system, the requirements for the tester hardware were low cost and portability. Based on these factors, two testers were selected: the JTAG Technologies PM3705 and the Corelis 1149.1/100F PC-AT card.

The PM3705 is a portable controller box which connects to a PC's parallel I/O port. It provides two 1149.1 TAPs and connects to the demo system via a 10-pin connector. Connectors are placed on each board (per PSC110F bridge LSP) to support board level test and on the processor card to support processor card and system level test. The PM3705 was used primarily for low volume board and system level manufacturing test, and for externally driven in-field test using a laptop computer.

The Corelis 1149.1/100F PC-AT card is based on National's SCANPSC100F which provides the ideal development platform for developing and debugging SCAN EASE functions. The SCAN EASE source code can be conditionally compiled to run directly on a 1149.1/100F PC-AT card. With a connection to the demo processor card's TAP connector, SCAN EASE was developed and debugged using a commerically available ANSI C debugger.

ATPG (Automatic Test Pattern Generation) Software Tool

Both the PM3705 and 1149.1/100F PC-AT card are supported by the JTAG Technologies ATPG tool, called VIP (Vector Interface Package). This tool automatically generates system level 1149.1 structural tests using four user-provided input files:

- **BSDL Selection File:** Boundary Scan Description Language files, which are provided by the component vendor or ASIC designer, define the specific implementation of 1149.1 features with an IC (see National SCAN Databook Section 6 Boundary Scan Design Support). With VIP, the user must create a BSDL selection file which provides the directory path to the BSDL file for each 1149.1 component included in a given test.
- **PCB Net List (In BNET Format):** A net list is automatically created by the PCB design and layout tool used to develop the PCB. The user must convert this net list format to a specific format which is read by VIP. This VIP format, called BNET, contains only the boundary scan nets. It also defines the connection of 1149.1 components in each boundary scan chain and associates a tester TAP with each chain.
- **Connection File:** This file defines the connection between each tester TAP (provided in the BNET file) and the SCANPSC110F bridges LSPs. It also defines how the SCANPSC110F bridges are connected to the backplane TAP and to each other (e.g., multidrop or hierarchical).
- **Pin Constraint File:** This file defines I/O pins in the net list which are pulled to fixed logic levels, I/O pins which must remain in the high-impedance state during a test to avoid bus contention, or system inputs which must maintain a specific logic level during a boundary scan test (e.g., a reset input pin).

SCAN EASE Software Tools

All three of the tools within SCAN EASE were utilized to develop and test the demonstration system:

- **EmbedPrep:** This tool was used to translate test vectors from the JTAG Technologies pattern format (PAT) to Embedded Vector Format (EVF). EVF is a compacted, ATPG-independent format that is used by the other SCAN EASE tools. EmbedPrep has no dependence on system hardware and is discussed further in the Embedding the Test Vectors section.
- **EmbedCom:** The EmbedCom tool is a Windows-based GUI which provides a user-friendly interface to the embedded test system. With this GUI, system self-test is initiated, new tests are downloaded to system RAM, pass fail information is displayed and datalogs can be uploaded. The GUI allows a user to test the system with no knowledge of 1149.1 or the embedded test code.
- **EmbedTest:** This tool, provided as ANSI C source code, contains functions which communicate with the system hardware and manage the application/evaluation of test data. Three aspects of the code must be considered when integrating EmbedTest into a specific design: integrating the EmbedTest functions with the application's operating system and system application code; mapping the SCANPSC100F addresses within the system; and implementing the drivers to support the μP specific UART (if serial communication with the EmbedTest code is required).

EmbedTest was written as multi-level modules. These levels range from the SCANPSC100F device drivers to a module called PG_CTRL which oversees the execution of tests and initialization of the test hardware. Integration with the system's operating system and application code is performed at the program control level. For the demo system, no operating system was implemented. A simple boot up routine was implemented to initialize the processor card

hardware and run EmbedTest. A self-test was run immediately after power up (or after a manual system reset button was pressed), then the system polled the RS232 port for further instruction.

EmbedTest includes three device driver options for mapping the SCANPSC100F. Two of the three drivers, the PSC100F in a memory mapped architecture and the PSC100 in an I/O mapped architecture, were included to ensure that the SCANPSC100F could be implemented with any commercially available microprocessor. For the demo, a Motorola 68K μP was used and, therefore, the memory mapped driver was selected. EmbedTest uses a conditionally defined macro to allow the user to easily specify the driver option.

The third SCANPSC100F driver option was written to support the application of EmbedTest using the SCANPSC100F-based Corelis 1149.1/100F PC-AT card. The demo system was used extensively in the development of the SCAN EASE tools. The Corelis 1149.1/100F PC-AT card enabled the majority of code development to occur on a PC using an ANSI-C debugger. Debugging modifications, prior to embedding the code within the system, minimized the time required to program a new EPROM each time a change to the code was made.

The final aspect of EmbedTest is the serial communication code. EmbedTest includes two modules which support serial communication. The highest level module interprets the commands entered using the EmbedCom GUI or generic emulator, and calls the appropriate EmbedTest application functions. The other, lower level, module is a UART specific device driver. For the demo, this device driver was specific to the Motorola 68K RS232 UART. The device driver configures and controls the UART hardware.

TEST DEVELOPMENT

Developing Test Vectors

In a previous section, the concept and benefit of system/board test partitioning was discussed. With the partitions defined in hardware, the next step is to develop tests corresponding to each partition. For the National demo application, separate tests were developed using the JTAG ATPG tool for each card and for the backplane. When applying embedded tests using SCAN EASE, each test is applied and evaluated separately. This enables SCAN EASE to provide pass/fail results for each test. For the demo, this level of resolution was enough to allow boards to be replaced and then fully diagnosed later using an external tester.

- **I/O Card:** Since all I/O cards share identical boundary scan configurations, generating tests to cover every I/O card required only one BNET file, one BSDL selection file and one constraint file. A unique Connection File was then created for each I/O card to provide the SCANPSC110F bridge address and LSP configuration. Samples of these files are shown in *Figures 5* through *8.*

  Internal Logic: The internal logic boundary scan test verifies the structural integrity of boundary scan nets within each I/O card. Some nets are shared between the internal logic chain (LSP2) and the backplane interface logic chain (LSP1). To access these shared nets, SCANPSC110F bridge is configured in the connection file to serially connect LSP1 and LSP2. The ATPG then views the LSP1 and LSP2 chains as a single chain and generates tests accordingly.

```
DESIGN S4A2_ABT

CHAIN               TAP1
  TCK               TCKL1
  TDI               TDIL1
  TDO               TDOL1
  TMS               TMSL1
  TRST              -
    IC_LIST
      U27           SCAN182245A
      U31           SCAN182541A
      U29           SCAN182373A
    END_IC_LIST
END_CHAIN

CHAIN               TAP2
  TCK               TCKL2
  TDI               TDIL2
  TDO               TDOL2
  TMS               TMSL2
  TRST              -
    IC_LIST
      U10           SCAN18541T
      U16           SCAN18374T
      U23           SCAN18374T
      U22           SCAN18374T
    END_IC_LIST
END_CHAIN

!PARRALLEL_CONNECTOR_LIST
!END_PARRALLEL_CONNECTOR_LIST

NETLIST
!NETname      ICname     PINnumber;
ADDIS0        U16        42
              U23         2
              U23        15;
ADDIS1        U16        41
              U23         4
              U23        16;
ADDIS2        U16        39
              U23         5
              U23        18;
ADDIS3        U16        38
              U23         7
              U23        19;
ADDIS4        U16        36
              U23         8
              U23        21;
ADDIS5        U16        35
              U23        10
              U23        22;
```

FIGURE 5. Sample BNET File

```
SYNTAX_VERSION 1.2
DESIGN IO_INT_2
REVISION UNKNOWN

TESTER_CHANNEL TAP1

! Board address is
! decimal 2 (00000010)
! The address is the only
! item that changes
! when creating internal
! net test for each I/O card
! TAP1 and TAP2 chains
! defined in BNET
! FROM TESTR (PART, ADDRESS, NAME OF LSPs
1-3) CASCADE1 (PSC110F, 2, TAP1, TAP2,
NONE)
END_CHANNEL
```

FIGURE 6. Sample Connection File

```
PRIMARY_IO  N;
! input tied to GND - set to sense low
OE1         S 0;
! input tied to VCC - set to sense high
DS1         S 1;
!Reset Pin - must remain high
! during test
RSTL        D 1;
```

FIGURE 7. Sample Constraint File

```
! path to BSDL files for
! devices involved in test
C:\bst\bstlib\ns182245.dsh
C:\bst\bstlib\ns182373.dsh
C:\bst\bstlib\ns18374.dsh
C:\bst\bstlib\ns18541.dsh
C:\bst\bstlib\ns182541.dsh
```

FIGURE 8. Sample BSDL Selection File

Hierarchical Board Test: (only applies to board populating Con 6): This test verifies the same nets covered in the internal test, but includes an extra SCANPSC110F bridge device in the path between the I/O card and the backplane TAP. The extra SCANPSC110F bridge is handled in the connection file and all other input files are unchanged. The connection file is shown in *Figure 9.*

```
SYNTAX_VERSION 1.2
DESIGN hierarc
REVISION UNKNOWN

TESTER_CHANNEL TAP 1

!FROM TESTR (PART, ADDRESS, NAME OF TAPS
1-3 FOR THIS BRIDGE)
  CASCADE1 (PSC110F, 3, NONE, NONE,
  CASCADE2)
  CASCADE2 (PSC110F, 4, TAP1, TAP2, NONE)
END_CHANNEL
```

FIGURE 9. Hierarchical Board Connection File

- **Processor Card:** The processor card includes boundary scan nets, but also serves as the test master for the remainder of the system. This dual role dictates that separate internal processor card tests must be created for applications with an external tester versus application with the embedded tester. When applying embedded tests, the 1149.1 components which access and evaluate the processor's local bus cannot be included in the boundary scan test. Controlling the local bus with boundary scan would prevent the processor from communicating with board resources required to apply the tests. When applying tests with an external tester, the processor communication is not required except with dynamic memory which must be refreshed. Therefore, the local bus boundary scan nets can be tested.

  Internal Logic (External Tester): The same process used to generate the internal logic tests for the I/O card was repeated to generate tests for the I/O card's internal logic nets. A BNET was created to include the boundary scan nets including the local bus nets; the selection file was created to point to the BSDL files; a constraint file was created to force or sense specific values; and a connection file was created, in this case, including all three LSPs in the chain.

  The processor card's auxiliary port logic (LSP3) contains a logic component connected between two boundary scan components. Therefore, testing the nets between these devices requires that signals pass through this component. A special list, called a cluster test, was generated to support this connection. To implement a cluster test, the user must provide a set of functional vectors for the cluster logic, in this case a single component. These functional vectors can range from a full functional vector set to only those vectors required to detect interconnect faults. For the JTAG Technologies ATPG tool, VIP, the functional patterns are passed into a post-process file called the APL file. The APL file is later compiled by the VIP tool to generate the test vectors.

  Internal Logic (Internal Tester): This test is a subset of the external tester version. For the embedded test version, boundary scan device outputs which interface the processor local bus were disabled throughout the test. Forcing the boundary scan outputs to a high impedance state was handled in the constraint file. A portion of the constraint file is shown in *Figure 10.*

```
PRIMARY_IO  N;
! input tied to GND - set to sense low
OE1         S 0;
! input tied to Vcc - set to sense high
DS1         S 1;
! Reset Pin - must remain high during test
RSTL        D 1;
! Local bus pin - forced to high impedance
CPUD0               Z;
CPUD1               Z;
CPUD2               Z;
CPUD3               Z;
CPUD4               Z;
CPUD5               Z;
CPUD6               Z;
.
.  continues....
.
```

FIGURE 10. Processor Card Internal Logic Constraint File

- **Backplane:** With tests generated for each board, the only remaining step is to develop tests to evaluate the interconnects between boards. For the JTAG Technologies VIP tool, a backplane test is viewed as just another board test. A BNET file for the boundary scan backplane nets and a connection file are created to indicate the SCANPSC110F bridges and LSPs containing components which interface these nets. In the case of the National demo, each card's backplane interface logic was connected to the SCANPSC110F bridges' LSP1. The backplane test connection file and BNET file are shown in *Figures 11* and *12.*

```
END_IC_LIST
END_CHAIN

! I/O Card 2
CHAIN               TAP3
  TCK               TCKL3
  TDI               TDIL3
  TDO               TDOL3
  TMS               TMSL3
  TRST              -
    IC_LIST
      U324          SCAN182245A
      U328          SCAN182541A
      U326          SCAN182373A
    END_IC_LIST
END_CHAIN
!PARRALLEL_CONNECTOR_LIST
!END_PARRALLEL_CONNECTOR_LIST
```

FIGURE 11. Backplane BNET File

```
NETLIST
!NETname      ICname     PINnumber;
BP_A0         U11        25
              U126       55
              U326       55;
BP_A1         U11        24
              U126       53
              U326       53;
BP_A2         U11        22
              U126       52
              U326       52;
BP_A3         U11        21
              U126       50
```

FIGURE 11. Backplane BNET File (Continued)

```
! Configuration file for backplane test.
!

SYNTAX_VERSION 1.2
DESIGN BCKPLN
REVISION UNKNOWN

TESTER_CHANNEL TAP1

!FROM TESTR (PART, ADDRESS, NAME OF TAPS 1-3
!FOR THIS BRIDGE)
 MULTIDROP1 (PSC110F, 1, TAP1, NONE, NONE)
!processor card
 MULTIDROP2 (PSC110F, 2, TAP2, NONE, NONE)
!I/O card 1
 MULTIDROP3 (PSC110F, 3, TAP3, NONE, NONE)
!I/O card 2

END_CHANNEL
```

FIGURE 12. Backplane Connection File

Embedding the Test Vectors

At this point, the hardware design is complete, the tests have been generated and the SCAN EASE code has been integrated into the system. The last step is to embed the test vectors into the system memory. This action requires two phases.

First, the vectors must be converted from the ATPG tool's output file format to EVF. The JTAG Technologies VIP tool generates test patterns in a unique file format, called the pattern format (PAT). To translate the PAT files into EVF files, the SCAN EASE EmbedPrep tool provides a PAT to EVF compiler. The compiler, called PAT2EVF, is an executable file which runs on a PC or workstation.

Each PAT file, representing a single test, is entered as an input to the compiler. PAT2EVF also prompts the user for information regarding the test name, test type and date. The test name, test type and date are included in the EVF's file header, which is later used by SCAN EASE to associate pass/fail status with the specific test.

With each PAT file converted to a corresponding EVF file, the next action required is to actually embed the vectors into memory. For the demo application, an EPROM programmer was used to embed each EVF file into the processor card's EPROM (the same PROM which contained the SCAN EASE EmbedTest code). EmbedTest uses a single locate statement to point to the embedded EVF vectors. Therefore, the separate EVF files must be appended together before programming the EPROM. EmbedTest uses the file header to determine where each separate EVF file starts and ends within this single, appended EVF file.

TEST APPLICATION AND FAILURE DIAGNOSTICS

At all stages of the demonstration system's life cycle, a combination of external and internal tests were performed. For PCB prototyping and board/system manufacturing test, an external test was applied, followed by an embedded test. For field level test, the opposite order was followed. The system was tested using the embedded tester and then, if necessary, tested using the external tester. The order of testing was dependent on the number of failures expected and the ability to diagnose failures with the embedded versus external test methods.

During prototyping and manufacturing, each PCB (cards and backplane) is tested for the first time. Therefore, these stages have the highest occurrence of PCB interconnect failures. For the demo application, external testing provided a quick test application and access to the JTAG Technologies diagnostic tool. With this tool, boundary scan failures were diagnosed automatically to the pin and/or net level. This extremely tight resolution facilitated board repairs. Once the failures were resolved, the embedded tests were applied to confirm correct operation of the embedded test routines and to enable execution of the non-boundary scan, functional test routines.

During field level test of the demo system, the objective was to quickly confirm that the interconnects were sound and that the system was functioning. Since the system was already thoroughly tested in manufacturing, the likelihood of a failure was very low. For this reason, the embedded self-test was an ideal method of testing the system.

For most field applications, the level of field test resolution is at the board or sub-system level. The goal in the field is to minimize system down time. If a failure is found, the board or sub-system is removed, replaced and retested. Depending on the cost, the board or sub-system is discarded or sent back to a repair depot. A similar goal was used for the demo system. With a separate test for each demo card and for the backplane, SCAN EASE was able to provide pass/fail diagnostics to the card/backplane level. If a failure was found, three options were available:

- **Card Removal:** The most simple option was to replace the card with a spare and diagnose the failure at the factory using an external tester.
- **Embedded Diagnostics:** SCAN EASE supports serial communication with the National demo system. With this link, new tests are downloaded to system RAM. These tests offer tighter diagnostic resolution than the card-level tests which are embedded in system ROM and applied during power on self-test. For example, the power on test simply shows that the card is failing. The downloaded tests may view a specific connection between devices on the card to determine which internal card connections are failing.
- **Off-line, Pin Level Diagnostics:** To provide pin level diagnostics for failing demo cards, an external tester and off-line diagnostics tool was utilized. The connection was made on the processor card to disable the embedded tester and provide access to the entire system. Since the embedded and external testers were connected at the same hardware location and since the embedded/external tests were identical, the embedded failures were repeatable on the external tester.
  For a system which does not provide external tester access, an alternative method of running off-line, pin level diagnostics is to use the datalogging option and serial communication capability provided with SCAN EASE to upload failing vectors to a file. This file is the converted to a format that is readable with an off-line tool.

BOUNDARY SCAN BENEFITS REALIZED WITH THE NATIONAL DEMO APPLICATION

Prototyping Boards and System

For the initial hardware debug, boundary scan proved to be a tremendous time saver. It eliminated the structural faults which are often very difficult and time consuming to debug using functional techniques. Once we were sure that the components were effectively placed on each PCB, we were able to focus our efforts on the primary objective of debugging functional and timing related problems.

Manufacturing Process Verification

Boundary scan provided a means of testing the interconnects for the entire system. With the use of the SCANPSC110F bridge on each card, tests were applied using a single, system wide tester connector, but partitioned for each card and the backplane. Boundary scan enabled efficient failure detection, diagnosis to the pin/net level and PCB repair.

Field Level System Test and Diagnostics

The National demonstration system is transported and presented all over the world. Therefore, the ability to test and resolve failures in the field was a key requirement of the test capability. With the ability to embed boundary scan test control within the system, the system interconnects were easily verified prior to each functional presentation. Additionally, remote access to the boundary scan vectors and test application code enabled test downloading and result evaluation to occur using a laptop computer.

Non-Contact Test Access for Surface Mount Technology IEEE 1149.1-1990

National Semiconductor
Application Note 891
John Andrews

ABSTRACT

Mechanical and chemical process challenges initially limited acceptance of surface mount technology (SMT). As those challenges have been overcome, another obstacle has become apparent: electronic test access. Through-hole components on a 100 mil grid allowed physical aceess. SMT which has provided new levels of packing density has also denied physical test access. To overcome this challenge, the Institute of Electrical and Electronics Engineers (IEEE) has sponsored a new standard, IEEE 1149.1-1990, the Standard Test Access Port and Boundary-Scan Architecture.

THE SMT ASSEMBLY CHALLENGE

The use of SMT has required the refinement of several technologies including: photolithographic improvements in printed circuit etching, computer aided layout to support routing the large number of interconnects, and soldering to allow devices to be attached to first one and then the reverse side of the printed wiring board (PWB) without through-hole mechanical capture.

Equipment to pick and place fragile SMT components with adequate alignment to the prepared pad area was needed to assure high yield assembly. Optical alignment systems replaced the open loop equipment used to assemble boards with dual-in-line packages. The technology has matured. SMT has gained wide acceptance.

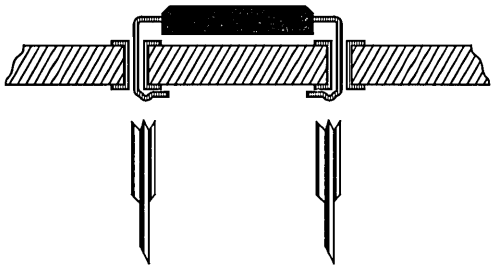
TRADITIONAL DEFECT DETECTION, DEFECT ISOLATION

A high yield assembly process, always a target, is important for SMT printed circuit cards because it can be difficult to isolate faults. There is risk of assembly damage during repair. If an incorrect diagnosis results in an unnecessary repair, not only are repair costs higher than necessary, but the risk of damage increases.

Bed-of-Nails test fixtures such as shown in *Figure 1* have provided test access for over twenty years. These fixtures have at least one test probe per IC pin to provide access for printed circuit continuity checking. Low voltage PWB interconnect continuity tests are usually run before applying full power to the PWB. Each connection point on each network is checked for continuity to all expected connections. In addition, by forcing a sequence of bits onto each output pin with the bed-of-nails and then reading the signal received on every other net, it is possible to detect nets that are shorted together and often to tell which two nets are shorted.

Once interconnection defects have been isolated and repaired, it has been common practice to use the bed-of-nails to drive each net of the fully powered board to test each integrated circuit on the assembly. For very simple ICs such test patterns were readily developed. A few microseconds were often adequate to determine that a simple IC was functioning correctly. During these functional tests, the electrical connection of the IC to the printed circuit board was checked as an integral side effect of the test.

Paper first published at Surface Mount International, 1992.

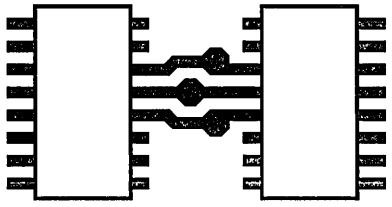


TL/F/11568–1

FIGURE 1. Traditional Bed-of-Nails PCB Test Access Method, Now Challenged by Shrinking Physical Contact Possibilities

Forcing a net with a bed-of-nails contact often required backdriving an IC's output. It might be necessary to force several hundred milliamperes into an IC's output to force a network to the opposite logic level. Backdriving IC outputs does not improve component lifetime. As IC complexity has grown, it has taken more test vectors and therefore required more time backdriving IC outputs.

As SMT allowed packing density to grow, printed circuit layout software began to appear with features that allowed physical access to continue with traditional bed-of-nails testing. *Figure 2* shows a portion of a layout that supports continued access. While supporting test access to allow defects to be detected, this defeated the advantage of SMT: higher packaging density. In addition, layout software became more complex as it was used to help overcome access problems.



TL/F/11568–2

FIGURE 2. Despite Shrinking Component Sizes, Some Users Have Kept Large Feature-Sized Etch to Continue to Support Physical Access

To support physical access some manufactures began using bed-of-nails fixtures that could contact both sides of a PWB. One user, in a personal communication, reported that these fixtures were so fragile that they might need to be repaired after testing as few as ten SMT printed circuit cards. And the time to develop such fixtures often extended beyond system development time and delayed the start of high volume production. Some users have reported that developing an SMT bed-of-nails fixture added 10% to their board development cost.

IEEE BOUNDARY-SCAN TEST ACCESS

IEEE 1149.1 was defined to replace the test access provided by a bed-of-nails test fixture. *Figure 3* shows an idealized concept of what was needed. As shown, a scan cell (SC) is located at each input and at each output pin. An output SC cell must be able, in test mode, to force the logic state of its output pin without regard to the state of the system logic. Similarly, each input SC must be able to monitor the signal on its input pin. IEEE 1149.1 was developed to provide this drive/sense capability using, not external test probes, but internal test circuits.

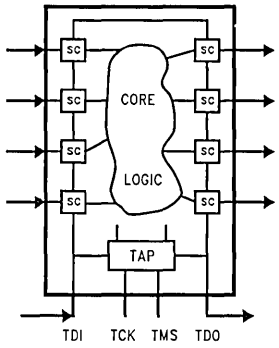


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FIGURE 3. Bed-of-Nails Test Access Has Been Replaced by Adding Embedded Test Probes to Each IC Input and by Providing Test Drivers at Each Output. Driving Outputs and Sampling Inputs is Called EXTEXT

As its name implies, boundary scan provides a scan path around the boundary of an IC as shown in *Figure 3*. Scan test access is a methodology that allows each IC to provide test access from within the IC itself, not from an external array of physical probes.

SILICON NAILS

Figure 4 shows an example of the kind of simple circuits needed to sample IC inputs and to replace the normal, mission mode drive values with test values. At each input we need a means for capturing the input signal and then shifting it out for external examation by automated test euuipment (ATE). This input circuit has shown in dashed lines some optional logic that will be discussed later.

The typical output boundary scan circuit is able, with limited external control signals, to become the source of the logic state that will drive the external interconnections. This is a solution to the simple problem of driving and sensing printed circuit board interconnections to detect process defects.

As shown in *Figure 3,* a test access port (TAP) controller is located in each IC to allow the ATE to control the boundary scan cells. The operation of the TAP controller and the implementation of its instructions have been described in detail in the IEEE standard.(1) The TAP has four dedicated test pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS). TDI and TDO are used to shift test data in and out of each 1149.1-compliant IC.

TCK shifts the data through each chip, while TMS controls a 16-state finite state machine in each IC. The state machine determines what each IC is doing. For example, an IC may be sampling its input, shifting data or driving outputs. In fact, the TMS input together with the TAP controller can shift TDI

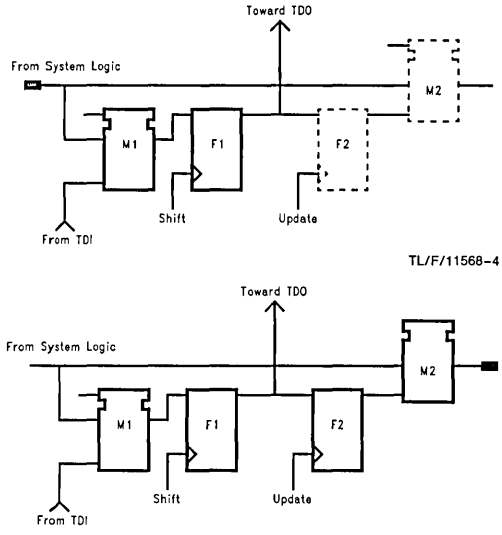
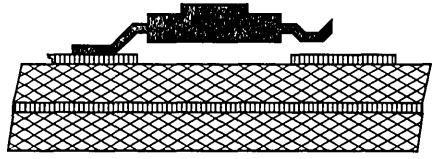


FIGURE 4. With IEEE 1149.1 I/O Pins May Capture the Data Arriving at a Pin and They May Be Used to Control Output Pins. Test Circuits Such as These May Also Test Internal System Logic. Circuits Such as These are Added to All System Pins

data into an instruction register. With the flexibility provided by an instruction register, IEEE 1149.1 is able to support an almost unlimited number of optional test features.

In 1149.1 the ability to drive test values onto output pins and to capture input logic states using the test logic is called EXTEST for external test. Most interconnect faults may be detected. For example, if a surface mount IC has a lead that is not attached to the printed circuit module as shown in *Figure 5,* the fault can be detected. Assume that this is an output, if the boundary-scan cell at that pin attempts to force the connected network, there will no response on the inputs that should be driven. The input boundary-scan cells of other ICs will detect a defect when they sample their input net.



TL/F/11568–6

FIGURE 5. Lifted IC Leads, Not Accessible with Bed-of-Nails by the Embedded Probes of the Driving and Receiving IC, If they Implement Boundary-Scan

Before 1149.1, to force the output driver in the IC with the lifted pin required that the automated test equipment generate a sequence of test vectors to force the inputs of the IC. This pattern would indirectly control the IC output. Controlling IC outputs from the inputs requires a complete functional understanding of the IC. This points out another advantage of IEEE 1149.1: PWB interconnect test programs can be developed without a detailed understanding of the function of each IC on the PWB. This simplification has resulted in test development time reductions that have compressed schedules from months to as little as one day.(2)

When bed-of-nails testers are used, it is necessary to control IC outputs by forcing the network to the desired test level even if the IC driving the net is attempting to force the net to the opposite level. This can result in forcing current levels well beyond manufacturer's specified maximum limits. The time spent backdriving an IC output must be limited to minimize reliability degradation. Using boundary-scan to test for interconnect faults removes the need to backdrive IC outputs.

REMOTE TEST ACCESS

Because direct physical access is not needed to detect faults, diagnostic tests may be run remotely. It is possible to test a digital system without even opening the system cabinet. Because physical access is not required, test engineers can run many PWB and system tests remotely using modem-connected testers without even leaving their office.

TESTING ICs AFTER PWB ASSEMBLY

IEEE 1149.1 can test more than the interconnections. It can also test ICS. Although bed-of-nails supported IC testing by forcing pins to required logic levels, boundary-scan registers allow test vectors to be shifted right into each IC. Once the vectors are in the IC commands such as INTEST for internal test can be used to deliver these test vectors to the inside of the IC. INTEST test results can be read using the scan cells at the IC output pins. INTEST uses the dashed line logic in *Figure 4* to connect the test stimulus to the IC's internal system logic. Using INTEST it is possible to deliver the same test vectors after PWB assembly as were used during component test at the IC foundry. The scan ring may be used to shift patterns to each IC allowing all ICs to be tested concurrently.

BUILT-IN-SELF-TEST (BIST) TECHNIQUES

IEEE 1149.1 can be used to support other test strategies. For example if an embedded deterministic pattern generator were built by reconfiguring a scan register, it might be possible to generate a new test vector with each clock pulse. This is a big time reduction compared to shifting in a new pattern with one clock pulses per bit in the PWB's scan path.

To test a multiplier, 1149.1 instructions could be used to reconfigure the test logic into a pattern generator and to connect the resulting patterns to the input ports of a multiplier. The reduce the time required to check each product at the multiplier output, other test logic can be used to compress the individual multiplier results into one composite test signature. If the test sequences are repeated in exactly the same way for unknown and for good multipliers, it is reasonable to conclude that multipliers that give the same result as a known good multiplier are probably defect free.

IEEE 1149.1 can be used to configure, to control and to observe BIST logic. For example, 1149.1 can be used to initialize the starting values for BIST pattern generators. It can be used to control test clocks. It can be used to shift out test results for examination by the ATE. BIST controlled by 1149.1 can reduce test time by orders of magnitude compared to the time required by shifting in vectors one at a time.

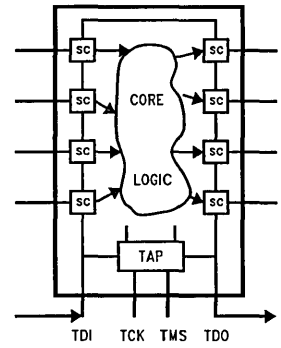


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FIGURE 6. Exploiting the Boundary-Scan Test Logic to Also Test the Interior of an IC. IEEE 1149.1 Defines a Standard Instruction Called INTEST

CHECKING FOR CORRECT COMPONENT SELECTION

IEEE 1149.1 can even be used to check for correct component selection. This feature was supported within the standard by defining an optional test feature called the IDCODE instruction. When the IDCODE command is included and executed, a 32-bit idcode will be the next pattern shifted out of the IC on the TDO pin.

The 32-bit code contains JEDEC-related manufacturer's identification, a part number as defined by the component manufacturer, and four bits that may be used to track design versions. Thus, without visual inspection, a printed circuit board may be inspected for correct component selection. The ability to electronically distinguish between different versions of an ASIC is intended to reduce errors caused by incorrect package labeling, and by accidental use of obsolete versions.

A system can be examined for the use of obsolete versions of an IC by reading each IDCODE. Remote access could be implemented. One day it may be possible to inspect systems that are in the field for known defective ICs. It is possible that the inspection could be completed without ever taking control of the system from a customer. With remote access, it may be possible to completely inspect a site without even visiting the facility.

EXAMPLE DESIGN

Some systems do not have spare backplane pins to allow 1149.1 to be added to the system. One solution to this test access problem is shown in *Figure 7.* Here a typical bus master, SCANPSC100[3,4,5], is connected to the system logic level backplane buses. The component converts the backplane bus to an 1149.1 test bus on the very PWB that needs the test bus.

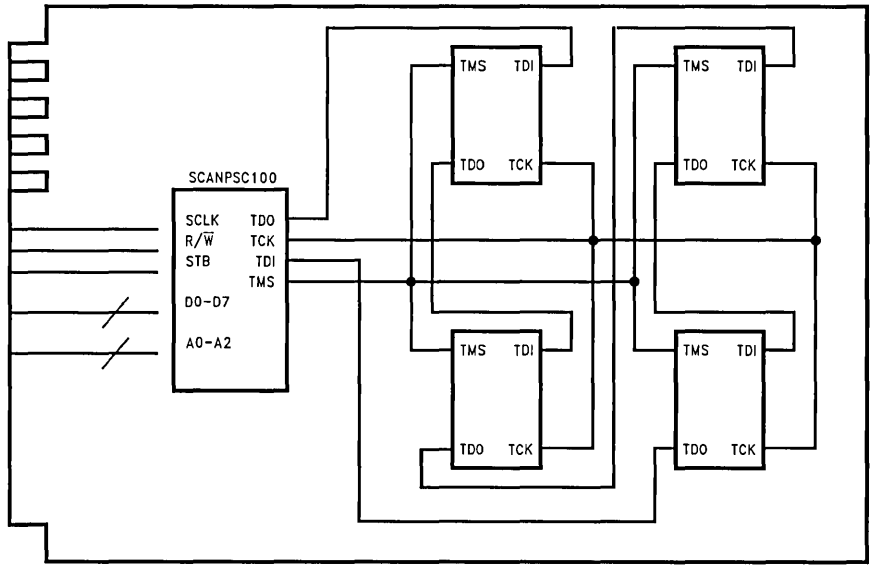

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FIGURE 7. An Example of 1149.1 Applied to the Test Access of a PWB with No Spare Backplane Pins to Provide Test Access. A Typical Bus Master, SCANPSC100, Develops the Needed Test Port on the Module

On the PWB are shown a few SCAN Widebus interface circuits whose 1149.1 test ports are connected to the bus master. These bus circuits and other 1149.1 compliant ASICs can be controlled by the four pin test bus. The diagnostic processor that stores and executes the 1149.1 tests could be the main system computer.

CONCLUSIONS

The IEEE has defined a boundary scan test access standard that supports test access that will allow packing density to continue to increase with regard to the need for direct physical test access. The standard offers features that allow not only interconnections to be tested, but for attached ICs as well.

DISCLAIMER

The opinions expressed herein are entirely personal and do not necessarily reflect those of either the IEEE or any of the 1149 Working Groups.

REFERENCES

1. IEEE Standard 1149.1-1990/ANSI, *"Standard Test Access Port and Boundary-Scan Architecture"*.
2. H. Kajitani, H. Sato, H Saito, and S. Oresjo, *"Practical Test Generation with IEEE 1149.1 Boundary-Scan"*, ATE and Instrumentation Conference 1992, pg 10.
3. J. Brown, *"Design of a Parallel-to-Serial Bus Converter"*, Electro 1991 Proceedings, pg. 534–539.
4. J. Brown & J. Marshall, *"A Second Generation Boundary-Scan Tester"*, Wescon 1991 Proceedings, Pg. 578–582.
5. National Semiconductor, *"PSC100, Parallel to Serial Converter"*, 1991.

ABT Design Considerations for Fault Tolerant Backplanes

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Application Note 881
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Application Engineer

INTRODUCTION

National Semiconductor's high speed Advanced BiCMOS Technology, ABT is a 1.0 μm process product introduced to provide a high speed fault tolerant solution for interface needs. Some of the targeted interface environments include computer servers, mainframes and central office switches.

Each of these interface environments suffer from glitching or level degradation on their backplane or bus, generated from either live insertion of a board or a power up and down cycle used when performing maintenance on a system. Board designers need to address live insertion and power cycling requirements when designing a fault tolerant system. Definitions and applications of live insertion and power cycling change based on the product that interfaces with a backplane environment.

Discussion of a fault tolerant benefits from a review of definitions and solutions for fault tolerant interfacing and a review of device specs and how they contribute to a fault tolerant environment.

DEFINITION OF TERMS

— Live Insertion

Boards like those seen in a telephone company's central office switch are often removed and inserted while the backplane remains active. Insertion and removal generates glitches and voltage level changes on the backplane. The level of isolation that a board mounted interface device provides the backplane can be broken down into three major groups.

— **1st Level of Isolation** is defined as the ability of the interface devices to allow insertion of the board to which it is mounted without having to power the system down. Requirements include a method of suspending the bus activity to prevent glitch or level corruption of bus data.

— **2nd Level of Isolation** is defined as the ability of the interface devices to allow insertion of the board without the need to power the system down or suspend bus activity. Requirements include a method by which the bus can check for, and correct, faults introduced on the backplane during board insertion or a method for providing proper biasing of the board interface devices with a staggered pin arrangement on the board-backplane connector. Precondition biasing circuitry for the interface device may also provide the required isolation.

— **3rd Level of Isolation** is defined as the ability of the interface devices to allow board insertion without any limitations, restrictions or requirements of other circuits on the preservation of bus data.

The level of isolation that an interface device mounted on a board provides for the backplane has a direct impact on system uptime. Increasing levels of isolation allow for increased serviceability without system interruption. Board isolation provided by an interface device gives more freedom to the designer for focusing on purpose built board functions, reducing board design complexity and ultimately, board cost. ABT products reward the board designer and the board user these benefits with a 2nd Level isolation solution.

— Fault Tolerance

Fault tolerance in a backplane environment is the ability of the bus to detect and/or correct errant signals from any source including glitches, level changes, etc., generated from the insertion or extraction of a board into a backplane. A system populated with ABT products minimizes the need for errant signal processing associated with the live insertion and extraction process when biased correctly.

— Power Up/Down TRI-STATE®

When the devices that interface with the backplane power up or down, their connection to the bus will ideally maintain a high impedance state. With respect to the ABT product family, the output enable circuitry has control of the output state of the interface device during power up and down so as to prevent intermittent low impedance loading or glitch generation commonly associated with conventional CMOS and Bipolar devices.

— Partial System Power Down

Partial system power down implies that a system comprised of a combination of hardware and firmware provides power switching control of a backplane slot to allow for insertion, or removal of a board. Partial system power down facilitates system serviceability. Board-mounted ABT interface products enhance serviceability for permitting backplane slot power cycling while maintaining high impedance, glitch free isolation with the board and its backplane.

SOLUTIONS FOR FAULT TOLERANT INTERFACING

The achievement of a fault tolerant system solution with live insertion capabilities begins with a review of some of the bus protection solutions available. Options available to the ABT product family include:

— Staggered Pin Arrangement

For a PC edge connector arrangement, the solution in *Figure 1* can be adopted to provide proper biasing of the output enable pin ($\overline{OE}$) to ensure high impedance on the backplane. It will satisfy both insert and removal requirements. While this configuration provides an ideal connector, constraints often limit the number of different pin lengths to two. By offsetting the $\overline{OE}$ pin, we want to ensure that it will either reach a high level of $\geq$2.0V, before V_{CC} is applied, or that $\overline{OE}$ will maintain a $\geq$50% V_{CC} level during the V_{CC} ramp.

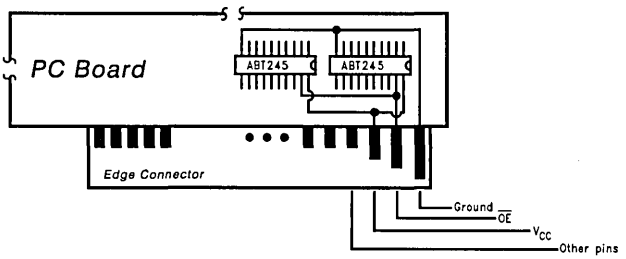


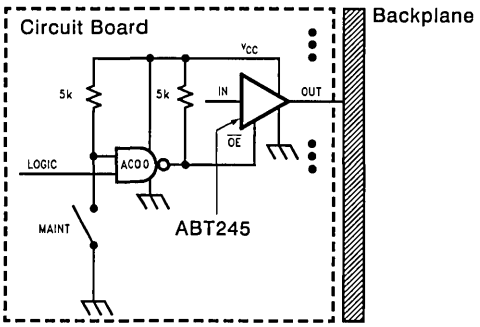
FIGURE 1

— Isolation Circuitry

Isolation circuitry provides another option for board and backplane isolation. Again, this solution will provide the necessary $\overline{OE}$ pin biasing to assure a level of 2.0V or to assure $\overline{OE}$ maintains ≥50% of V_{CC} as V_{CC} powers up or down for guaranteed high impedance interface to the backplane.

The design of Circuit-1 below provides >50% of V_{CC} for the $\overline{OE}$ pin throughout the V_{CC} ramp then switches to a voltage level of a logic high once the AC00 reaches its turn-on V_{CC}. After board insertion, the MAINT switch is opened and the LOGIC pin becomes the $\overline{OE}$ control. Live insertion or removal for this solution requires a technician to manually operate the maintenance switch (MAINT) to ensure proper biasing of $\overline{OE}$ and board-backplane isolation.

Circuit-1



SPECIFICATIONS AND THEIR CONTRIBUTION TO FAULT TOLERANT SYSTEMS

DC specifications and their characteristic input/output curves help map out the loading effects of an interface device on bus or backplane. The loading characteristics of typical ABT input and output pins are shown in *Figures 2–4.* National Semiconductor's ABT245 characteristic curves are used for this demonstration.

— Powered Down Backplane Isolation

The power down leakage characteristics of a bus interface device assist the interface board designer in understanding the effects of loading on his backplane. During live insertion, the board is not powered up and the instantaneous loading upon contact would look like the curves of VID and IZZ in *Figures 2* and *3.* Typically, loading leakages in the +200 μA range begin to affect the V_{OH}/V_{OL} levels in a backplane application. The VID and IZZ curves illustrate the loading effects on the backplane over a range of backplane voltages from 0.0V to 5.5V.

— VID

VID is a voltage that is measured on an input pin at a current loading of 1.9 μA in a power off condition such as when V_{CC} and the non-measurement pins are at 0.0V.

The curve of VID vs IID in *Figure 2* shows the current leakage of a typical ABT input pin. The ABT inputs limit loading leakage to <1.9 μA over an input voltage range from 0V to 5.5V.

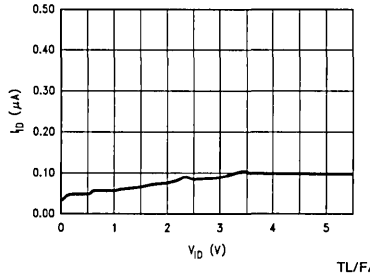


FIGURE 2

— IZZ

IZZ is a current that is measured on an output pin at a voltage of 5.5V during a power off condition such as when V_{CC} and the non-measurement pins are at 0.0V.

The curve of VZZ vs IZZ in *Figure 3* shows the current leakage of a typical ABT input/output (I/O) pin and how it loads a bus or backplane over a range of bus voltages from 0.0V to 5.5V. I/O pin configurations exhibit combined current characteristics from components of the input circuitry and output circuitry. ABT I/O pins specify loading leakage at 100 μA max. with a typical loading leakage at 3 μA at room temperature.

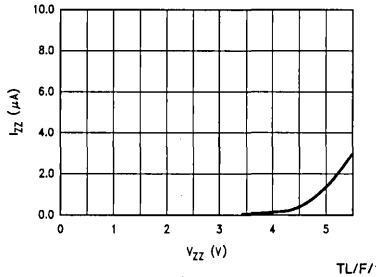


FIGURE 3

— Powered Up Backplane Isolation

During power up operation, the output enable pin, $\overline{OE}$, controls backplane isolation. The IOZH/IOZL parameters provide the interface board designer with the leakage characteristics of the interface device during a tri-stated condition.

— IOZL/IOZH

IOZL is a parameter that quantifies the output leakage current while the part is powered up and the output is conditioned low before it was tri-stated (disabled). IOZH is the same as IOZL except that the output was conditioned high before being tri-stated.

The IOZL/H curve in *Figure 4* shows an I/O pin leakage characteristic during TRI-STATE operation over a range of bus voltages from 0.0V to 5.5V. ABT devices specify IOZH/L at a maximum of 50 μA while typical leakage is in the vicinity of 12 μA at room temperature.

— Powering Cycling and Backplane Isolation

During the transition of a power up or power down cycle, an interface device output might act erratically by glitching or seeking a voltage level that is disruptive to the backplane. These transition characteristics degrade fault tolerant systems and would increase system down time.

The curves in *Figures 5* and *6* demonstrate the capability of the ABT245 to maintain isolation from an active bus and provide a glitch free output while being powered up and down. With the $\overline{OE}$ pin conditioned high, V_{CC} was cycled between 0.0V and 5.5V to monitor the output voltage levels as they would appear on a bus. Bus loads of 1 kΩ pull-up and pull-down were used. The bus voltage level disruption is in the micro-volts range attesting to the minimal impact ABT interface products would have on the backplane.

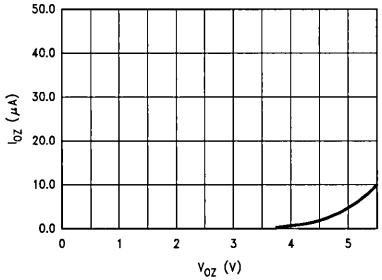


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FIGURE 4

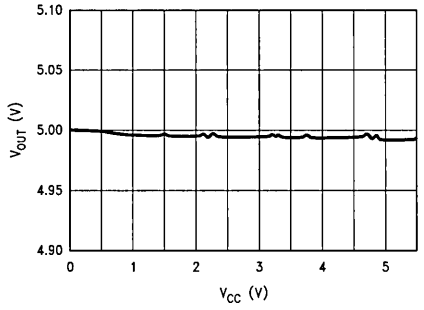

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FIGURE 5. Bus High Effects

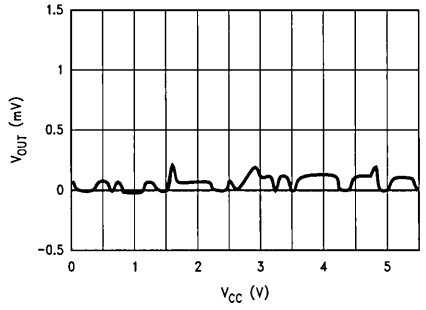

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FIGURE 6. Bus Low Effects

SUMMARY

ABT interface devices offer glitch free power cycling provided that the $\overline{OE}$ pin is held at the device specified V_{IH} (2.0V) level. In practice, $\overline{OE}$ will provide an output high impedance condition if $\overline{OE}$ maintains a level of $\geq$50% of V_{CC} through the 0V to 5.5V range. In fact, the $\overline{OE}$ pin circuitry gains control once V_{CC} is $\geq$1.0V. Interface device output characteristics for V_{CC} levels before 1.0V are controlled through the isolation circuitry discussed earlier.

ABT designs and specifications recognize the need for more fault tolerant interface devices. Live insertion guarantees such as VID/IZZ, IOZL/H and glitch free power cycling all promote better system uptime, especially for telecom switching environments. Together with extended AC specifications that reduce the need for complex performance evaluations, ABT live insertion guarantees allow designers to spend more time on total system performance features and not worry about the logic.

Design of a Parallel Bus-to-Scan Test Port Converter

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Application Note 889
Jay Brown

ABSTRACT

The IEEE Std. 1149.1 Standard Test Access Port and Boundary-Scan Architecture[1] as well as other scan path methodologies use a serial interface for transmitting data to and from the circuit under test. This serial communication presents an efficiency problem in transferring data between a processor and the scan ring. This paper describes the architecture and features of a device that interfaces a parallel host bus to a serial test bus. The parallel/serial converter, National's Embedded Boundary Scan Controller, SCANPSC100F, integrates several features to simplify board test and offers a way to make scan operations more efficient by managing shift operations directly in hardware.

INTRODUCTION

Scan path methodologies are the dominant technique in implementing Design-For Test in board and system designs. With the advent of high density board/packaging technologies, the need for scan is even more pronounced as physical access to multiple nodes on the board is no longer feasible. Boundary scan has become the generally accepted answer to this access problem. Wide acceptance of boundary scan is most readily evidenced with the creation of the IEEE Std. 1149.1 Standard Test Access Port and Boundary-Scan Architecture[1, 2]. Standardization of boundary scan through 1149.1 allows board designs to contain scannable components supplied by different manufacturers.

The use of 1149.1—or any other scan methodology—presents the problem of efficient data transference to and from the scan ring. Implementing scan operations with only a processor is software intensive, and consequently, very slow. The general solution to this efficiency problem is to manage shift operations in hardware.

The 'PSC100F was developed to offer a hardware solution to the scan problem. Simply put, the 'PSC100F facilitates the transfer of data between a parallel host bus and a serial test bus. The following sections first define objectives for developing the 'PSC100F. The architecture and basic operation are then described. Next, specific features are outlined along with the trade-off decisions that were made during implementation.

OBJECTIVES

The general objective of the 'PSC100F is to act together with a parallel bus host as a serial bus controller. A general concept of this application is shown in *Figure 1.*

Figure 1 shows the 'PSC100F interfaced to the 1149.1 bus. Because it is very likely that systems will contain other than 1149.1-type devices, one of the main design objectives is a 'PSC100F that is flexible enough to support many types of scan bus styles and standards. One can assume that systems will also contain several devices that employ some proprietary scan protocol. Also, there is another IEEE standard currently being developed that will provide an alternative to 1149.1[3]. To attain serial scan protocol independence, a means must be provided for the protocol to be determined by software.

Flexibility should also be designed into the parallel port to provide a variety of choices for a parallel bus host. A generic read/write protocol should be used. 'PSC100F status

Paper first published at Electro International, 1991.

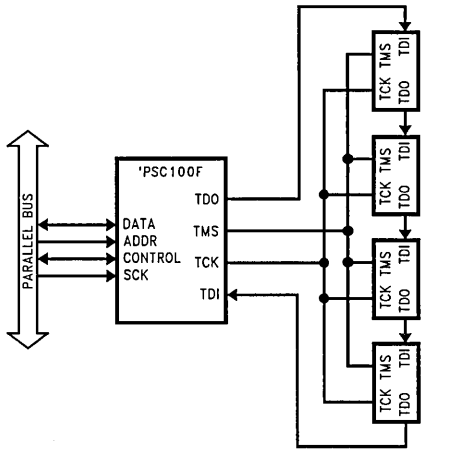

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FIGURE 1. Parallel/Serial Converter, National's Embedded Boundary Scan Controller, SCANPSC100F, General Application

should be supplied to the host with status registers or an interrupt pin. Synchronization between the 'PSC100F and the host should be reviewed as they may not always operate off of the same clock.

Several target applications must evaluated when designing a control mechanism for a serial test port. External instruments could use the 'PSC100F to serialize test vectors to be applied to some unit under test. For example, a 'PSC100F designed into a PC board could allow the PC to act as a simple and inexpensive automatic tester. Embedded in small systems, the 'PSC100F may access a single scan ring from a central control point. The host may be the system processor, a dedicated test processor, or a simple state machine for transferring test vectors between memory and the 'PSC100F. In larger systems, a single ring may cause unacceptable scan throughput. Partitioning the test architecture into many scan rings allows patterns to be scanned and applied to many blocks concurrently, improving throughput. The 'PSC100F should be able to support various combinations of these system test architectures.

In addition to providing a means of serializing data, the 'PSC100F should also provide features that simplify typical test operations. Pattern generation and compression features should be considered as well as a counter to count scanned bits and to count clocks during Built-In Self-Test (BIST) operations. Other features could be built in to simplify typical operations performed when using the 1149.1 standard, e.g., the SAMPLE operation.

When using the 'PSC100F, the assumption is made that testability is being designed into the system; therefore, to maintain a hierarchical test structure, the 'PSC100F must also be easily testable. Features must be implemented so that the 'PSC100F is fully testable from the parallel bus, or from a dedicated test port if size and cost allow. Also, some bypass mechanism should be implemented so that an external source (e.g., an ATE) may have access to the serial bus.

ARCHITECTURE AND BASIC OPERATION

The basic structure of the 'PSC100F is summarized by the block diagram in *Figure 2*. The conversion between parallel and serial data is basically managed by a bank of double-buffered, parallel-to-serial shift registers. Double buffering allows a parallel write or read to occur while data is shifting, thus improving throughput.

Three shifter/buffers are used for out-going data and one for in-coming. The pin names for the serial port follow the same convention as described in 1149.1. The Test Data Out (TDO) and Test Mode Select (TMS0:1) ports are used to output serial data, while data is shifted in at Test Data In (TDI). The Test Clock (TCK) is also generated and is derived directly from the 'PSC100F's clock, SCK. TDO and TDI are used to scan test data. If used in an 1149.1 application, TMS0:1 can be used to supply control to the Test Access Ports (TAP) of the 1149.1 board components. With two TMS lines, up to 2 scan chains can be controlled in parallel. However, as data appearing at the TMS0:1 outputs is completely user specific, other protocols can be implemented.

Read and write operations are performed with an 8-bit asynchronous parallel interface. For write operations, R/$\overline{W}$ and $\overline{CEB}$ lines are forced low. Data and address are then loaded with the STB signal. The write operation is synchronized to SCK before data is transferred to the addressed register. Read operations occur with R/$\overline{W}$ held high. When reading status bits for polling operations, a command must be issued to update status so data will not change while a read is taking place. Handshaking between the 'PSC100F and the host processor can be accomplished 3 ways: 1) By generating wait-states with the Ready ($\overline{RDY}$) signal, 2) By using any of 3 event-driven interrupts via the INT signal, or 3) by polling status bits in the Status Register.

Three mode bits are used to mask interrupt events which cause the INT pin to go high. Interrupts may be generated by expiration of the 32-bit counter, by the transmission of a byte of data from the TDO port, or by the reception of a byte by the TDI port.

The general problem of serial data flow is managed by controlling TCK, which is derived directly from SCK. If the host cannot keep up with the serial flow of data, TCK will be stopped in the low state. A 32-bit counter is included to control the number of bits being shifted. The number of bits to be scanned is first loaded into the counter by 4 consecutive writes to its address. Shifting may progress until the counter expires, causing TCK to stop. If the number of bits scanned is not a multiple of 8, software must align the last byte shifted and mask the unused bits.

The functionality of the 'PSC100F in any given application is dictated by the contents of the Mode Registers. Each shifter/buffer has a specific mode bit with which it can be enabled or disabled. If a shifter/buffer is not enabled, it has no impact on serial data flow and retains its last state. This is particularly useful when control data remains static during long shifts of test data. For example, during the Shift-DR state of the 1149.1 TAP Controller, TMS is held low for the duration of time that data is being scanned. Instead of shifting a long pattern of zeros from the TMS port, the TMS shifter/buffer can be turned off and the processor can spend all its time transferring data to and from the TDI and TDO ports.

The following sequence describes the actions that typically occur when using the 'PSC100F to apply test data through an 1149.1 boundary scan chain. The sequence begins with the TAP Controller *(Figure 3)* of each device on the board in the Run-Test Idle state. The objective in this example is to capture data in the Capture-DR state and shift 500 bits of new data into the scan path while shifting out 500 bits which resulted from the capture. The new data shifted in will be applied to the system logic in the Update-DR state. The TAP will then be returned to the Run-Test Idle state.

1. The host writes to the 'PSC100F, accessing one of the mode registers and enabling the 32-bit counter and one TMS port.
2. Three clock cycles are needed to get from Run-Test Idle to Shift-DR (see *Figure 3*). The pattern needed on TMS is 001 (LSB shifted first). First the counter is loaded with (00000003)h which will cause 3 clocks and 3 TMS bits to be issued. This is accomplished with 4 consecutive writes to the counter's address.
3. The pattern XXXXX001 is loaded into the TMS shifter/buffer by writing to its address. (The 5 most significant bits will not be used.)
4. TCK now runs for 3 clock cycles and stops. While transitioning from the Capture-DR state to the Shift-DR state, data was captured into the boundary scan register on the board.

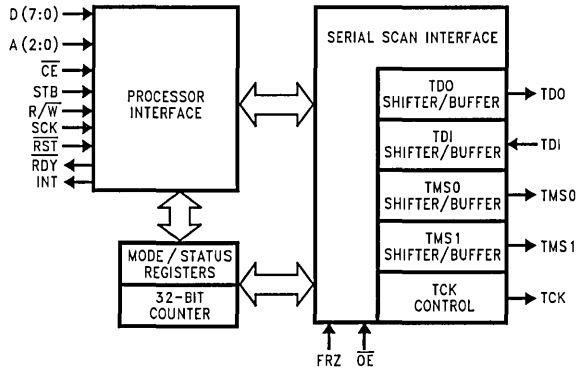

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FIGURE 2. Embedded Boundary Scan Controller, SCANPSC100F Architecture

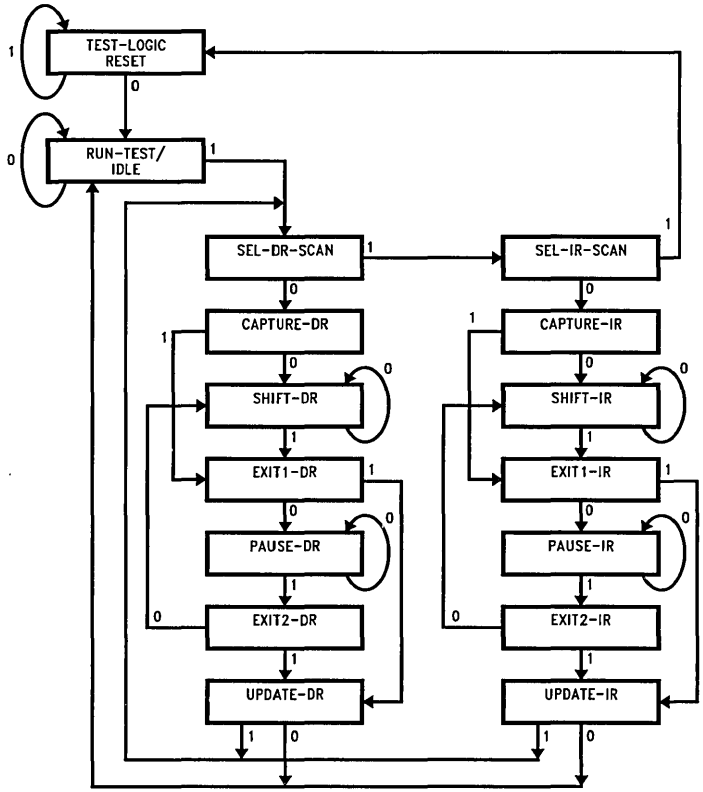

FIGURE 3. 1149.1 TAP Controller

5. With the TAP controller residing in the Shift-DR state, the next step is to configure the 'PSC100F to shift 500 bits of new data out of TDO while shifting the 500 captured bits into TDI. This action requires a write from the processor to the 'PSC100F Mode register 0 to disable TMS, to enable TDO and TDI, and set the Auto TMS High Enable Bit. With the TMS buffer disabled, the TMS pin retains the last logic level shifted out of the TMS buffer (i.e., the logic low which transitioned the TAP controller into the shift-DR state). This will hold all TAP controllers connected to the 'PSC100F in the shift-DR state.

   Setting the Auto TMS High Enable bit provides a key efficiency gain when shifting data to and from the 'PSC100F. With this bit set, TMS pin will automatially drive a high logic level, for one TCK cycle, when the counter reaches a count of 00000001. This high logic level transitions all TAP controllers to the EXIT1-DR state which shifts out/in the last bit and completes the shift operation.
6. TCK begins clocking when the first byte of data is written to TDO. The host exchanges 500 bits of data with the boundary scan chain by several consecutive write/read cycles. During this step, the processor may be unable to keep up with the serial flow of data, causing the TDO shifter/buffer to become empty or the TDI shifter/buffer to become full. If either of these conditions occurs before the counter expires, TCK will be stopped and restarted to prevent overflow and underflow conditions. When 499 clocks are issued, the counter expires causing TCK to stop.
7. To complete the example, the TAP Controller must be sequenced from Exit1-DR (where it is now), through Update-DR, and back to Run-Test Idle.
8. As TDO and TDI are no longer needed, their respective mode bits are cleared. The counter is loaded with (00000002)h which is how many clocks are needed to return to Run-Test Idle. The necessary TMS data is loaded: XXXXXX01.
9. Two TCK pulses are now issued and bring the TAP back to the Run-Test Idle state. Data that was shifted into the boundary scan chain in steps 7 and 8 has been updated during the Update-DR state.

FEATURES AND TRADEOFFS

This section describes many of the specific features included in the Embedded Boundary Scan Controller design. The reasoning for each feature is detailed.

Technology: The 'PSC100F is fabricated in a 1.5 μm CMOS process with the option of having either CMOS- or TTL-compatible input levels. CMOS is desirable for its "zero" static power consumption. When not in test mode, a system's power dissipation should not be impacted by dormant test circuitry.

Package: Pin count is kept to 28 for minimal impact on component cost and board area consumption. The 'PSC100F has been designed to fit both surface mount and through-hole type packages. Although surface mount packages will receive the most use, smaller companies that do not have

the luxury of surface mount manufacturing will use through-hole technology while still enjoying the low test costs of boundary scan.

Parallel Interface: A generic read/write protocol was chosen for the processor interface to ensure that compatibility will be preserved with all off-the-shelf processors. Three options are given for handshaking: interrupts, polling, and wait-state generation using the Ready ($\overline{RDY}$) signal. These options will give the user flexibility in transferring data. The data bus width was kept to 8 bits to minimize pin count and die size. Using a 16-bit bus would have meant going to the next highest standard package size: 44-pin. A significant increase in die area would also be seen. The improvement in scan throughput by using 16-bits did not outweigh cost.

Serial Port: Multiple ports were considered to maximize scan ring partitioning capabilities, but the package size constraint allows only one port. However, supplying two TMS pins allows up to two rings in parallel when using 1149.1.

Scan Protocol Support: An option was considered to include a "master" TAP Controller and control TMS directly in hardware. ICs have been presented that implement this kind of serial port controller[4, 5]. With this method, scan operations can be controlled by issuing a predefined set of commands. This option would allow a free-running TCK, with overflow and underflow prevented by using the Pause state of the 1149.1 TAP controller. Although this method of controlling scan would be less software intensive, there are several drawbacks. The controller would be restricted to using the 1149.1 protocol which may not be compatible with other proprietary scan methods. The command set would presuppose certain sequences through the TAP Controller, thus limiting flexibility. For these reasons, the "master TAP" method was not chosen. Instead, protocol and sequencing are completely controlled by software. Data overflow and undefflow is prevented by simply stopping TCK.

One drawback of this method is more software involvement and, consequently, a possible detriment to performance. In this application, however, performance is out-weighed by functionality and flexibility. Another possible drawback is that TCK must be gated. Gating TCK introduces a relatively large and unpredictable skew from part to part due to process variation. This skew will impact a high performance system if testing occurs while running at normal operating speed; however, it is anticipated that a majority of scan applications will occur while the system is in a slow "single step" mode. At low speeds, TCK skew will have no impact.

Clock Speed: The 'PSC100F is designed to run at up to 25 MHz over military and commercial temperature ranges.

Output Buffering: All outputs have 24 mA DC current drive and are capable of switching 50Ω transmission lines. The high drive capability of the parallel port reduces the need for buffering when communication occurs over the backplane. The serial port also gains from the high drive. For example, if using the 'PSC100F to serialize data for a PC tester, the strong drive of the outputs allows a lower number of buffer stages between the PC and the test head. On a typical board using 1149.1 components, TMS and TCK may see extremely high loads as these are connected to every scannable component The large outputs can handle these loads without external buffering. In addition to high drive, the output buffers contain noise suppression circuitry that will minimize ground bounce and undershoot.

External Tester Access: By forcing the $\overline{OE}$ pin high, all serial port pins will be TRI-STATEd. This allows an external test resource to access the serial port without contention with the 'PSC100F.

Pattern Generation and Compaction: The TDO shifter/buffer and 16 additional flip-flops may be reconfigured as a 32-bit linear feedback shift register (LFSR) for pseudo-random pattern generation (PRPG). The TDI shifter/buffer can be configured as a 16-bit LFSR for serial signature compaction.

Loopback Mode: By setting a mode bit, data appearing at TDI can be looped back through the TDO port. This simplifies read-only operations by leaving the scan path in its state prior to shifting.

Testability: The 'PSC100F is highly testable from the parallel port. All registers are directly or indirectly readable and writeable. A test loopback mode is provided so data appearing at TDO or TMS0:1 can be scanned back into the TDI shifter/buffer. The 32-bit counter can be placed in single step mode for easy testability. Adding a dedicated test port was considered, but again, package constraints prevented this.

SUMMARY

The presented device enhances transfer of data between a parallel processor bus and a serial test bus. The protocol for applying serial patterns is completely controlled by software for maximum flexibility. Data overflow and underflow are prevented by stopping the test clock, TCK. A 32-bit counter and other features have been integrated to help make the 'PSC100F a viable means for improving the efficiency of serial test data communication.

REFERENCES

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G.Host JTAG Interface for Graphics Host Reference Design

National Semiconductor
Application Note 1003
Hamilton Hallmark's
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INTRODUCTION

The Graphics Host Reference Design kit is produced by the staff at Hamilton Hallmark's Technical Support Center in partnership with suppliers. A *reference design* is a working design, with all of the necessary elements in place to serve as an example of how a project might be approached. Included are schematics, application notes, program code (where appropriate), and data sheets. Request a kit by calling 1-800-605-3296 xH147 or through the World Wide Web at http://www.tsc.hh.avnet.com.

The G.Host design (the G is for Graphics) was made possible with the active support of the following manufacturers:

- Advanced Micro Devices with the 29K™ family of RISC microcontrollers, the MACH®465 complex programmable logic device (CPLD), and the AMD® 5V-only Flash memory. These components form a powerful and feature-rich design core that is easy to use. Virtually no glue is needed to interface to a wide range of peripherals.
- National Semiconductor brings several boundary-scan (JTAG) hardware elements to this design. The high-integration components used in the reference design—and the correspondingly high pin count of fine-pitch devices—need reliable methods of programming, test, and verification. The MACH465 CPLD, in particular, is best programmed in the circuit after assembly. National's Multidrop and Hierarchical Addressable JTAG Port, SCANPSC110F bridge; the Embedded Boundary Scan Controller, SCANPSC100F; and the SCAN18245T JTAG-compatible bus transceivers make it possible to interface with the JTAG capability built into the MACH465 CPLD and the AM29200™ family microcontrollers with ease.
- Corelis contributes the software for the boundary-scan process to generate boundary-scan test files. Their boundary-scan emulator allows quick access to the capability of National's boundary-scan devices, the AM29200 family of boundary-scan-compliant microcontrollers, and the AMD MACH465 CPLD. These tools have been a real boon to the test and verification of this design.
- Wind River Systems supplies the operating system for the design. The 29K family RISC microcontrollers are powerful and easy to program in their own right, with an architecture that lends itself to C or C++-language programming, but Wind River's operating system allows the programmer to concentrate on the features of the individual product. The initializations, interrupt vectors, and housekeeping details are quickly dispatched with the OS. They no longer need to be software projects in their own right.

The AM29200 family of RISC microcontrollers is especially suited for dealing with multiple complex tasks like performing real-time handshaking for what is essentially a wireless network, decompressing the data and preprocessing it for the printer. That much work in real time demands a powerful and fast instruction set and a high degree of predictability in execution. Differences in execution time (inherent in CISC architectures) can create unpredictable latencies. When operating a fast real-time data operation, such as our RF link, latencies must be minimized. This is one of the benefits of a RISC architecture, such as that used in the AM29200 microcontroller family. Each instruction in the set is completed in one instruction cycle. (Exceptions are instructions that respond to, or return from, interrupts, external memory accesses, and some math instructions.) Because of this execution stability, it is possible to reliably determine the time it takes to respond to real-time events.

The MACH465 CPLD is an important complement to the AM29200 family microcontrollers in this design. Essentially a large programmable block, the MACH465 CPLD can be set to do virtually anything to complement the power of the microcontroller.

The 5V-only Flash memory is integral to the core design idea as well. It can be reprogrammed using the AM29200 family microcontroller by simply writing to it if that memory area is set as writable in the Flash memory and in the microcontroller. Boot and operating system code can be protected either by programming the boot-block sectors of the Flash memory as non-writeable, or by configuring the microcontroller to treat the Flash memory area as read only. In the G.Host design, the boot areas of the Flash memory are selected by the ROM Chip Select 0 ($\overline{\text{ROMCS0}}$) pin; the normal operating area is selected by the ROM Chip Select 1 ($\overline{\text{ROMCS1}}$) pin. Either method will protect critical code areas.

Having the ability to update the operational portion of the program allows for maintenance and updates from a remote location. Simply place the program update algorithms in a write-protected (read-only) code area, vector to it, and begin. One scenario would be to place the new program in DRAM as data, vector to the update routine, and write the Flash memory from DRAM.

Information will arrive at the G.Host through the bidirectional serial port. This port will be connected to an RF transceiver for bidirectional communication. The microcontroller will control the handshaking protocol, the decompression of the data received, and the compression of any data sent back to the remote PC. It will preprocess the data for the HP-LaserJet-II-compatible printer so the printer does not need to do any further conversion. Both graphics processing acceleration—making the print job less time consuming—and multiple PCs sharing the resources of a single printer are realized.

The implementation of JTAG interface testing was chosen for the G.Host design for several practical reasons. The design warranted test accessibility due to its short development and debug time allotment. Once the design progressed into a standalone working unit, it was desirable to have it exercise a built-in self test to diagnose and report any physical errors that might exist during power-up. For these reasons, the G.Host design utilized as many JTAG compliant components as possible.

To keep in context with the actual design and its implementation of boundary scan testing, it is assumed that the reader is familiar with general concepts of the IEEE 1149.1 standard. Additional information on JTAG and Boundary Scan may be found in the National Semiconductor SCAN Databook.

There were several factors that contributed to the actual implementation of JTAG on this design. First, it was necessary to decide how to interface the signals to the board for testing. Second, it was important to allow for self or embedded testing of the board once the design was functional. Third, a JTAG port would be required for programming the AMD Mach device on the board. And finally, a JTAG port was necessary to allow for emulation of the AM29200 device.

Although it is possible to simply connect an external boundary scan tester to the board directly via a cable carrying the 5 JTAG lines and daisy-chaining the TDO to TDI lines from one device to another, this was not the answer for the G.Host design. It was important to find a way of allowing the microprocessor to test the board utilizing boundary scan. This would entail two things:

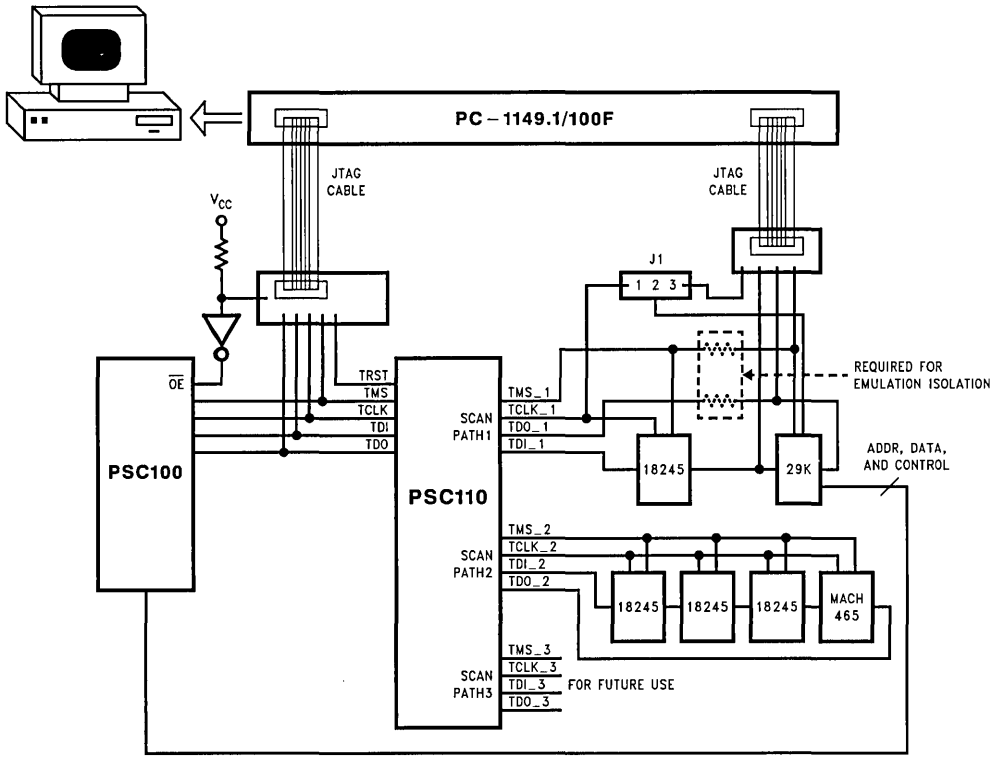
1. Finding a device that could accept a microprocessor interface on one side and a JTAG interface on the other.
2. Finding a device that could interface a single JTAG port into several separate chains in order to isolate the microprocessor and as few boundary scan components from the remaining JTAG devices possible.

National Semiconductor has two such components: the Embedded Boundary Scan Controller, SCANPSC100F and the Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F. The SCANPSC100F is an interface chip that connects an asynchronous parallel bus processor to a JTAG chain. Data can be written to the device via a μP/μC which is then serialized by the SCANPSC100F for boundary scan communications. Results on the boundary scan chain are sent back to the SCANPSC100F and are then readable on the μP/μC side. The SCANPSC110F is a SCAN bridge chip that supports up to 3 local scan paths which can be accessed individually from a single host JTAG port. Both of these devices were well suited for accomplishing our design goals.

The next task was determining if a suite of tools existed that would allow us to utilize these components successfully in the design. Corelis, a California based company specializing in boundary scan products, was the right choice. They have been working with both National Semiconductor and AMD for several years and have developed a powerful set of tools that will support testing a board containing the SCANPSC110F, JTAG programming a MACH device on board, and performing JTAG AM29000 emulation. The only interfacing required is several 10-pin headers placed on the G.Host board to connect a cable containing the 5 JTAG lines and 5 grounds from their hardware.

As stated earlier, the SCANPSC110 allows for multiple local scan paths. Choosing which devices to be placed on which particular chain was extremely important, based on the embedded self-testing goal. In order to boot-up the AM29000 device and execute test code, the only additional devices required on the G.Host design were a SCAN18245T transceiver, the flash memory, and a few minor discrete components. Of these devices, only the SCAN18245T includes boundary scan capability. Therefore, the AM29000 and SCAN18245T were placed on one chain while the remaining JTAG components were placed on the other. The final JTAG chain was to be reserved for the serial/RFD communications port, in case it included any boundary scan components.

As just stated, the first JTAG chain includes a AM29000 microcontroller and a National Semiconductor SCAN18245T. As seen in *Figure 1*, the boundary scan chain signals (TDO to TDI) are connected from the SCANPSC110, to the AM29000, then to SCAN18245T and back to the SCANPSC110. The TMS and TCLK lines are shown as being shared between the devices. This would be the standard configuration if JTAG emulation was not required. But, since the AM29000 needs to be isolated for emulation, 1 kΩ resistors were placed in the TMS and the TDI paths. Also, a jumper header is added to the TCLK path allowing either the SCANPSC110 or the alternate external port to drive the AM29000's TCLK line. (See *Figure 1.*)



TL/F/12119–14

FIGURE 1. G.Host JTAG Connectivity

As a side note, when external testing is performed on the board, the SCANPSC100's output enable must be disabled in order to avoid signal conflict on the boundary scan lines. This is accomplished by placing an inverter between one of the 5 header pins on the JTAG connector (normally open) and the active low output enable ($\overline{OE}$) signal of the SCANPSC100F. The input to the inverter contains a pull-up resistor, such that the $\overline{OE}$ signal is normally low. When the 10-pin JTAG cable is attached to the board, the input to the inverter is driven low from the ground connection on the cable and causing a high on the $\overline{OE}$ of the SCANPSC100F; thereby disabling the device.

The second boundary scan path contains four JTAG components: an AMD MACH465 and three SCAN18245T. The actual connections are shown in *Figure 1.* As in the previous path, isolation has been setup for the MACH465 in order to provide an alternate path for programming the device.

Actual testing of the G.Host design was extremely simple due to the suite of tools by Corelis. All that was required were two ASCII files: a connection (CON) file and boundary scan net (BNET) file. (Request electronic files from Hamilton Hallmark Technical Resource Center, 1-800-605-3294 or on the Internet at http://www.tsc.hh.avnet.com.) The CON file is a very simple file that is required when using a SCANPSC110F device on board. It specifies the names of the local scan paths that exist on the board which are referenced from the NET file. The NET file contains the backbone of the design. First an IC number must be associated with each JTAG device. Then each device is placed in order of location in each boundary scan chain (last placed first). Following this, is a list of the actual names and pin numbers of those connections that exist between these devices.

Also required, are the Boundary Scan Description files (BSD) of the JTAG devices used. These files are readily available from the manufacturer of the components themselves. (National BSD files for all SCAN parts may be obtained by calling 1-800-272-9959. Request Lit.# 580220-001; or on the World Wide Web at http://www.natsemi.com.) It is necessary to place these files into a specific directory that can be referenced by the software.

The Corelis tool used for testing was the PC-1149.1/100F/FULL. The hardware is a JTAG test board based on the National Semiconductor SCANPSC100F which contains 2 boundary scan interface ports. The software is a Windows based tool which includes Boundary Scan Automatic Test Pattern Generation (BTPG), and Enhanced Diagnostics. This package made the test development cycle extremely short and simplified due to its fully automated and admirably reported test results. The Corelis package is a powerful tool for JTAG testing.

CONTROLLERS

The AM29205 and the AM29200 microcontrollers were chosen as representative of the AMD 29K family of microprocessors and microcontrollers (see *Figures 4* and *5*). If the AM29205 microcontroller is adequate for a particular product or model, the footprint and interface for it is available. If the product or model needs more power, the bigger and faster AM29200 microcontroller may be used with no change in the rest of the design. Both devices have similar features and the same instruction set, with the AM29200 microcontroller being a superset of the AM29205 microcontroller.

The AM29205 microcontroller implements an external 16-bit instruction/data (ID) bus (still a full 32 bits internally). This presents some interesting complications when trying to use it interchangeably with the external 32-bit ID bus of the AM29200 microcontroller. Both microcontrollers have:

- A Harvard-style architecture, where program and data memory are separate
- DRAM interface drivers integrated in the microcontroller (including built-in CAS-before-RAS refresh)
- ROM drive (including support for writing to ROM space)
- Programmable peripheral-port pins.

The AM29200 microcontroller family is capable of DMA activity, and the ability to use it is built in the G.Host design as well. We are not using it in this iteration, however, because of the uncertainties involved in a DMA device possibly not releasing the bus back to the microcontroller in time to avoid data loss on the RF link. Hamilton Hallmark included it in the design to enhance the MACH465 CPLD FIFO when that is implemented. A designer wishing to use this feature could do so now, if no critical real-time operation could be jeopardized as our RF link could.

At power-on reset, both devices can be hardware-initialized to operate in a 16-bit format, and we have done that in this design. (Through the BOOTW signal, the AM29200 microcontroller may be configured to boot with 8-bit or 16-bit wide instruction fetching.) In this way, the boot code is the same for both microcontrollers, and the program can determine system configuration. The initialization code will check for microcontroller type (there is an internal processor revision level [PRL] field in the configuration register identifying each member of the family) re-initialize the appropriate registers to the proper values, then vector to the running portion of code as either a 16-bit or 32-bit external machine.

The 29K family microcontrollers are memory mapped with all features assigned to a memory address space of their own. This makes it easy to keep track of where peripherals and memory reside. Accessing a particular area of code memory, for example, is as simple as specifying the appropriate memory address range. The AM29200 and AM29205 microcontrollers will even take care of breaking the accesses into the appropriate number of wait states and bus widths as you have specified through internal control and configuration registers.

Since we have this powerful device available, we have used the MACH465 CPLD to implement a few other glue functions, such as translating levels for the parallel port, and providing the external latch functions needed by the microcontroller's parallel-port interface. The parallel port in the AM29200 family microcontrollers performs a mini bus-cycle within the larger parallel-port cycle. During a write, the microcontroller provides the appropriate control signals to place data in the parallel latch for the external system. It then completes the appropriate handshaking necessary to complete the transfer. During a read, the microcontroller uses the external parallel-port handshaking to determine when to read data from the external data latch. It then provides the necessary control signals to access the data.

Because the MACH465 CPLD is encased in a 208-pin package with a 25mm pin pitch, it could be difficult to program and then install the device on a printed circuit board (PCB) without damage due to excessive handling. Happily, AMD provided full boundary-scan (JTAG) capability in the MACH465 CPLD, which allows it to be programmed in the circuit. This is a tremendous advantage since the device only needs to be handled during assembly, and can be programmed according to need. Updates can be provided as well when desired. This is also useful in implementing different features in multiple products using the same hardware.

The MACH465 CPLD also features fixed, predictable, and deterministic delays throughout the part. This is important in this design to ensure reliable and synchronous data transmission throughout the multiplexing and demultiplexing stages of the design. Also, all macrocells in a logic block can be connected to an I/O cell through the output switch matrix. This matrix makes it possible to make significant design changes while minimizing the risk of a pinout change. All input and I/O pins have built-in pull-up resistors that help to minimize the external parts count.

Among the tasks delegated for the MACH465 CPLD are implementing a FIFO, using DRAM as the memory element and the CPLD as the control element. The CPLD will allow normal data accesses between the microcontroller and DRAM. In response to a signal from the microcontroller (not yet implemented) the MACH465 CPLD will begin to interleave FIFO data bound for the printer (which has been decompressed and preprocessed prior to being placed in the FIFO) with normal code and data-bus cycles. Once the word has been fetched from DRAM, it can be transferred to the printer a byte at a time.

The ability to expand this design is one of the goals we set in the beginning. The MACH465 CPLD has tremendous power and flexibility and has not yet been taxed in its abilities, except for pin count. We deliberately routed many of the control and bus signals through the CPLD, even though they were not being used, so that expansion would be mostly a matter of reprogramming the CPLD. This can be done in circuit.

In addition to the above, there are a few collateral duties for which the MACH465 CPLD is well suited. First among these is translating signals for the AM29205 microcontroller so that the memory interface can be 32 bits consistently. Inside the CPLD, we have programmed a multiplexer/demultiplexer designed to switch the lower order of data and instruction lines to and from the upper ones for the AM29205 microcontroller, based on both the signal that indicates which processor is installed (PIO5) and the A1 address line.

National Semiconductor's boundary-scan components are used to handle the hardware aspect of boundary scan. The Multidrop and Hierarchical Addressable JTAG Port, SCANPSC110F Bridge, provides an interface from one JTAG master port on a backplane or some other source, in this case the Corelis interface described earlier. In our design, we included the SCANPSC110F to allow multiple local test access ports (TAPs)—up to three per chip—to be created. Connecting the G.Host to a Corelis PC boundary-scan

interface, we can test each circuit individually and program the MACH465 CPLD in the circuit remotely, if we wish. The three ports allow for elements which may be missing at times (e.g., the RF link). The remaining paths can still be tested without changing the boundary-scan test routines for the others.

The Embedded Boundary Scan Controller, the SCANPSC100F is an 8-bit parallel-to-TAP bidirectional translator that allows us to implement the boundary-scan power-on self-test from the microcontroller. It is routed through the SCANPSC110F bridge.

Because of its position relative to the external boundary-scan test access port, the SCANPSC100F controller can enable the AM29200 family microcontroller to act as a test-bus master. The 8-bit parallel communications are translated into boundary-scan serial format and relayed to (and from) the rest of the system. To avoid confusion, insure that the external TAPs are set to an address different than the one used for the G.Host's SCANPSC100F bridge (U7).

Note: The IEEE Std 1149.1 boundary-scan specification requires only four serial signals. These are: Test Clock (TCK), Test Mode Select (TMS), Test Data Out (TDO), and Test Data In (TDI). The SCANPSC100F implements just these four required signals. There is a fifth, optional signal called Test Reset ($\overline{\text{TRST}}$) that is used by some devices. If your external path should make use of this signal, you will have to provide for it in additional circuitry. (One of the AM29200 family microcontroller I/O-port pins driving a simple buffer would work nicely.)

MEMORY

The ROM for this design uses two AMD 29F400 5V-only Flash memories, in a 256k x 32-bit wide arrangement (that's two 29F400 memory devices, each in a 256k x 16 setup). Except for the initialization sequence at power-on reset, the memory is accessed via a 32-bit interface, although 16-bit writes will be allowed in all but the boot-block area (see *Figure 8*). This allows the program, look-up tables, or identification bytes stored in the ROM to be updated in the circuit. The core routines to accomplish the update will reside in the boot-block area where they cannot be corrupted. Communications routines necessary to this process will also be protected.

During the initialization of the system, the microcontroller will boot in 16-bit mode. The MACH465 CPLD will be under self-test, so there is a need to have an alternate path for program execution. A National SCAN18245T transceiver provides this path during initialization in response to the ROM chip-select signal that is active during initialization (when the microcontroller is using the start-up memory area). A few control signals need to be synthesized during this time and, of course, the MACH465 CPLD will be under test, so it is not available to perform this function. We solved this dilemma by adding a PALCE22V10.

DRAM is organized as 4M x 32 bits wide, for 16 Mbyte of DRAM (see *Figure 9*). This is to accommodate page buffering for the printer and allow sufficient room to implement a FIFO controlled by the MACH465 CPLD. There is also enough room to store data tables or program updates, which can be installed by the microcontroller using an algorithm in its boot-block memory area.

A portion of the DRAM is to be used as the memory element of a FIFO, which will be controlled by the MACH465 CPLD. By adding this capability, we will not have to wait for the printer's response before returning to time-critical activities. Rather, we can store information in the DRAM FIFO area in 32-bit format, and retrieve it in 8-bit format for transfer to the printer. The printer transfer part of the operation is independent of the microcontroller.

Memory map and PIO control line assignments are shown in Tables I and II.

SUMMARY

The G.Host reference design is very straightforward and simple, designed for high performance while providing great flexibility. The schematics and data sheets included with the G.Host Reference Design Kit may be used as a springboard for other designs with only minor modifications required, or as it stands, if that meets your need. The components discussed here are easy to use, and they offer a great deal of power and performance—enough to tame the toughest embedded project.

RESOURCES

Hamilton Hallmark Technical Support Center
1-800-605-3296 ; http://www.tsc.hh.avnet.com

National Semiconductor Technical Resource Group
1-800-272-9959 ; http://www.natsemi.com

Advanced Micro Devices
1-800-222-9323 ; http://www.amd.com

Corelis
1-310-926-6727

MEMORY MAP

The G.Host maps functions to memory address in Table I.

TABLE I. Memory Map

Address Space (hexadecimal)	AM29200 Microcontroller Selection	G.Host Assignment	Maximum Size	
			AM29200	AM29205
0000 0000— 03FF FFFF All ROM Banks	ROM Bank 0 ROM Bank 1 ROM Bank 2	Boot Code Application Code Self-Test Port	64 Mbyte Bank Size User Set	12 Mbyte Bank Size User Set
4000 0000— 43FF FFFF All DRAM Banks	DRAM	Data Memory	64 Mbyte	12 Mbyte
5000 0000— 50FF FFFF All Mapped DRAM	Mapped DRAM	Not Used	16 Mbyte	16 Mbyte
6000 0000— 63FF FFFF	VDRAM Transfers	Not Used	64 Mbyte	
8000 0000— 8000 00FC	Internal Peripheral Registers	(See the following table for addresses)		
9000 0000— 90FF FFFF	PIA Area 0	Not Used	16 Mbyte	4 Mbyte
9100 0000— 91FF FFFF	PIA Area 1	Not Used	16 Mbyte	4 Mbyte
9200 0000— 92FF FFFF	PIA Area 2	Not Used	16 Mbyte	
9300 0000— 93FF FFFF	PIA Area 3	Not Used	16 Mbyte	
9400 0000— 94FF FFFF	PIA Area 4	Not Used	16 Mbyte	
9500 0000— 90FF FFFF	PIA Area 5	Not Used	16 Mbyte	
All Others	Reserved			

PIO CONTROL LINE ASSIGNMENTS

The G.Host assigns the peripheral input/output control lines of the AM29200 family microcontrollers as follows:

TABLE II. PIO Control Line Assignments

PIO Line	G.Host Function	Data Direction
PIO15	Serial Port CTS	Input
PIO14	Serial Port RTS	Output
PIO13–PIO8	Spares	(Not yet assigned)
PIO7–PIO0	(Not used)	

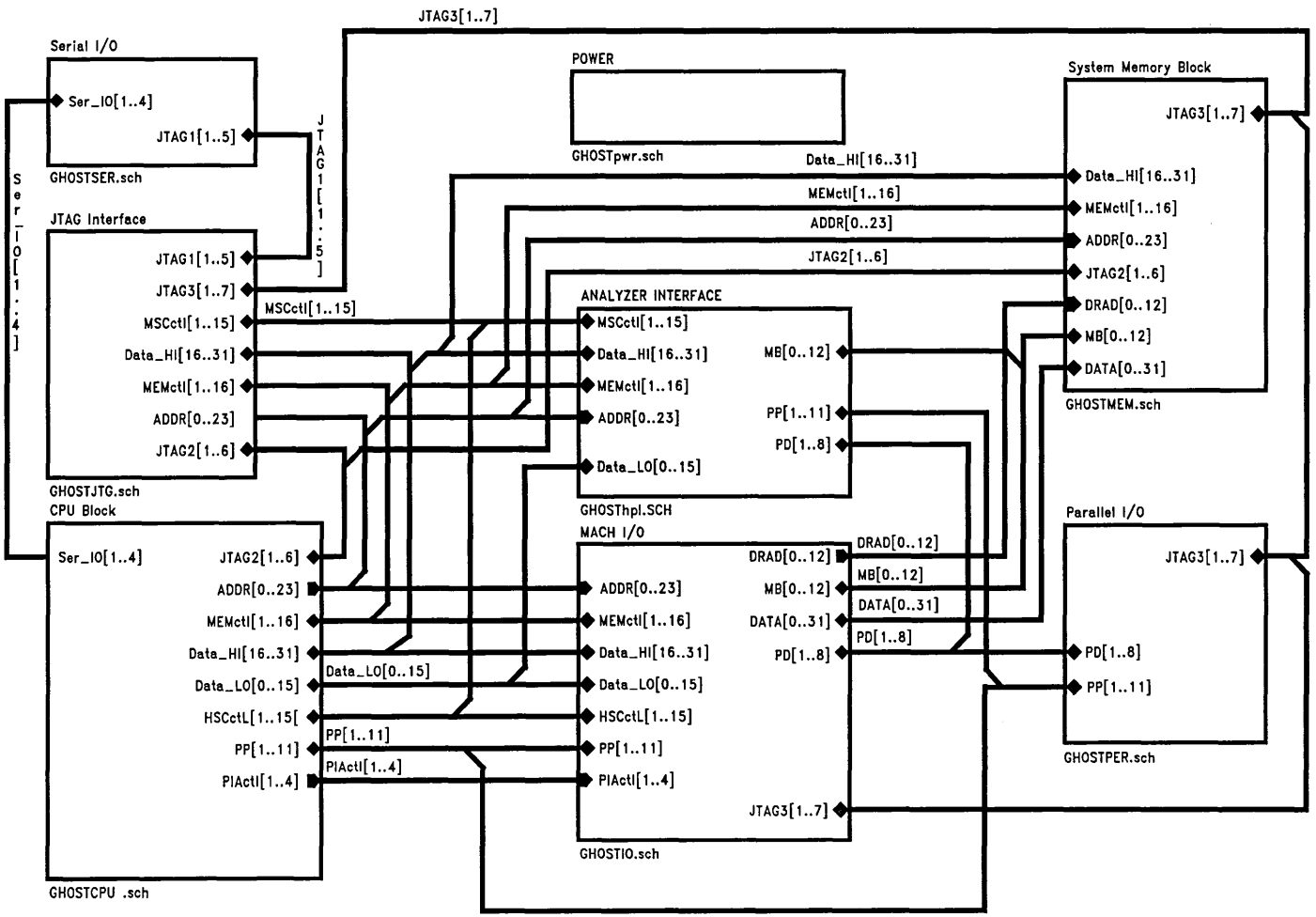


FIGURE 2. Top Level Block Diagram

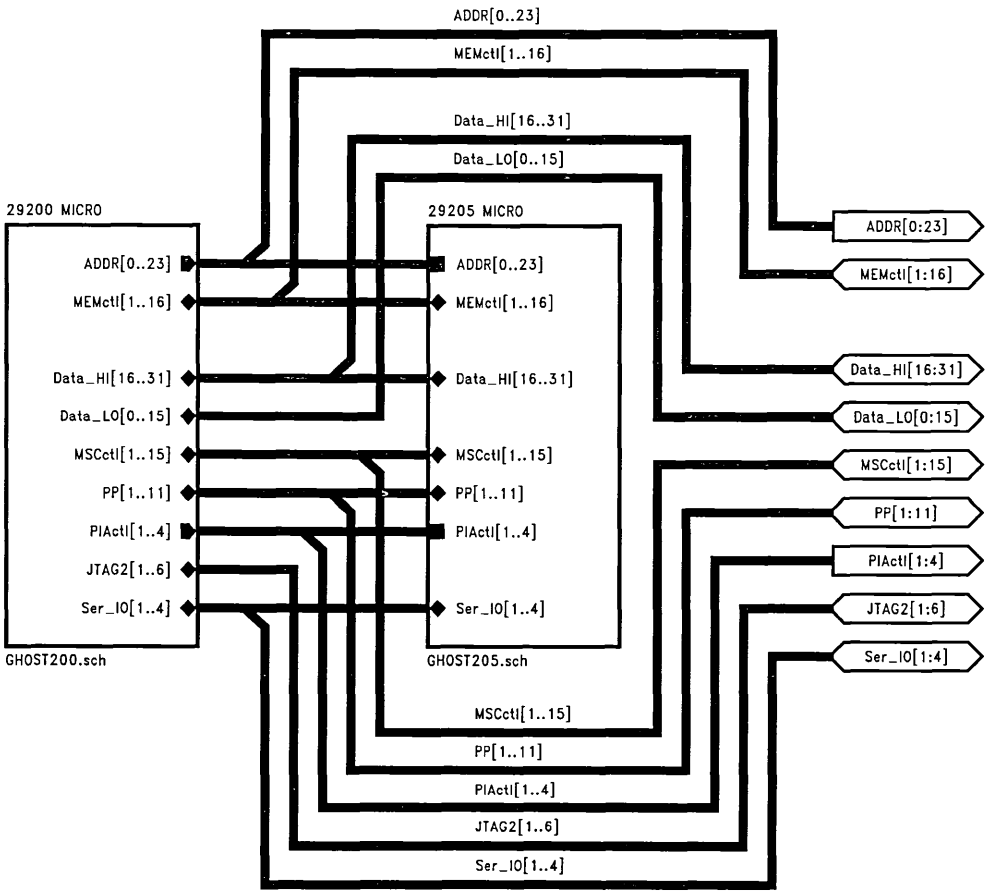


FIGURE 3. CPU Block

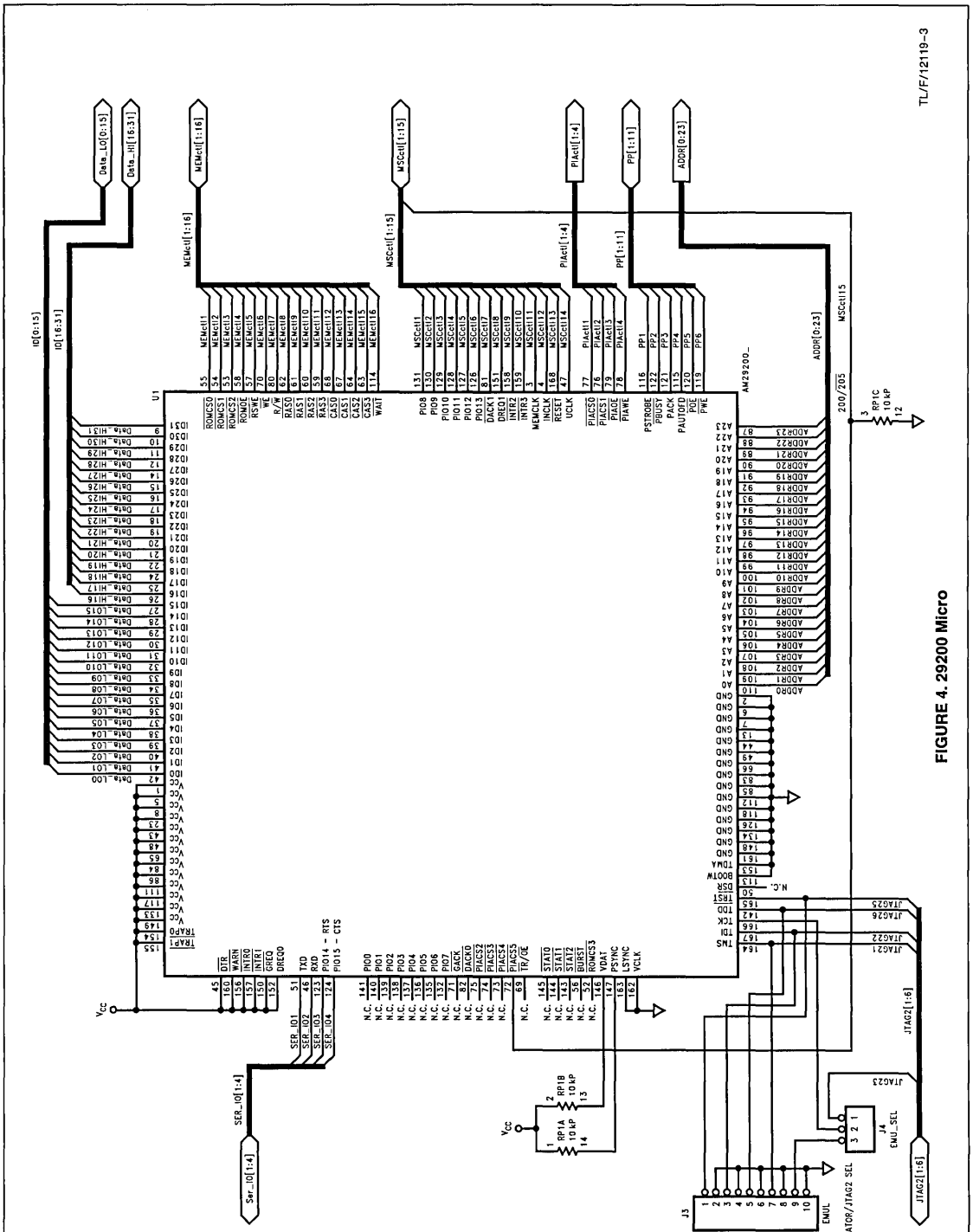


FIGURE 4. 29200 Micro

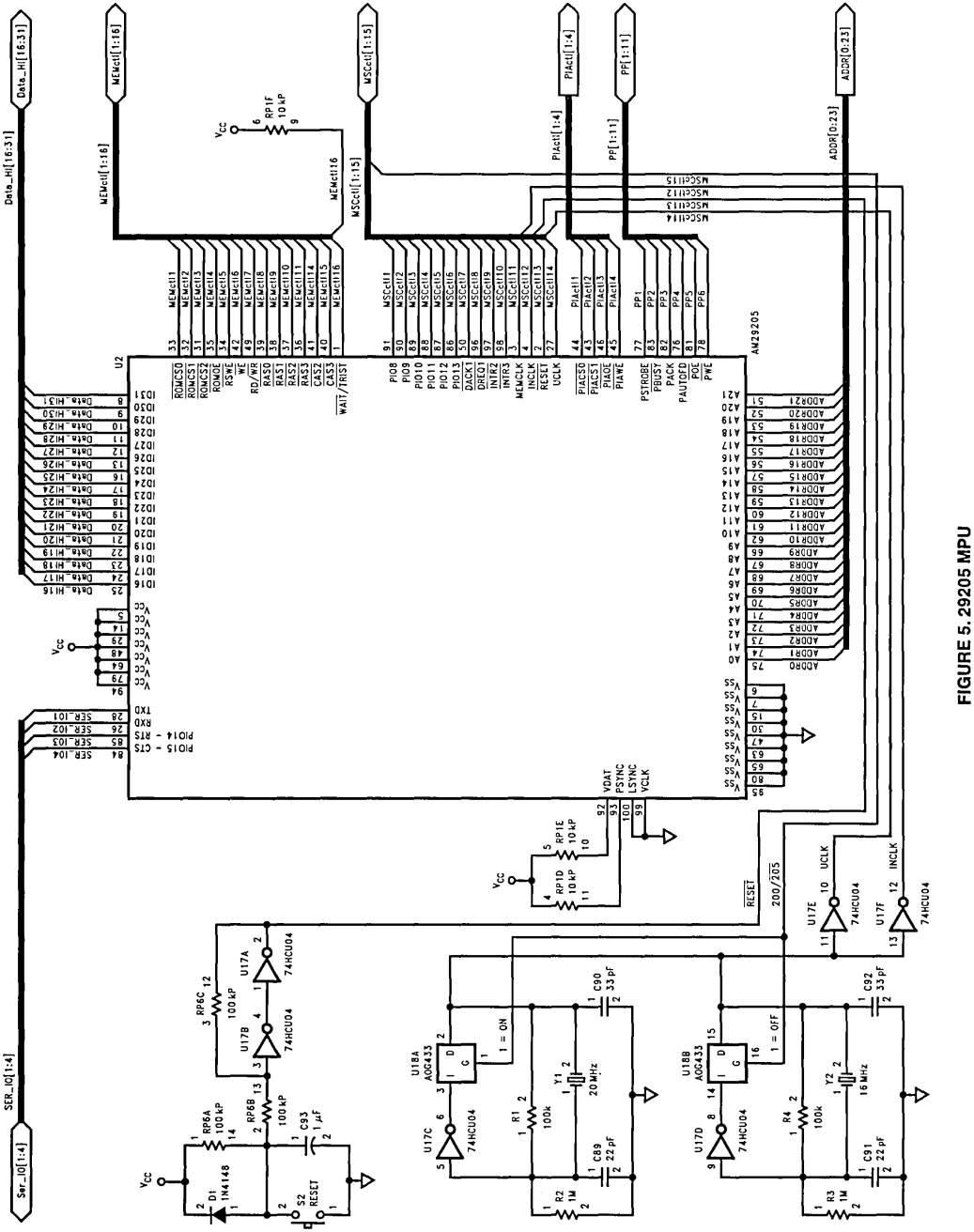


FIGURE 5. 29205 MPU

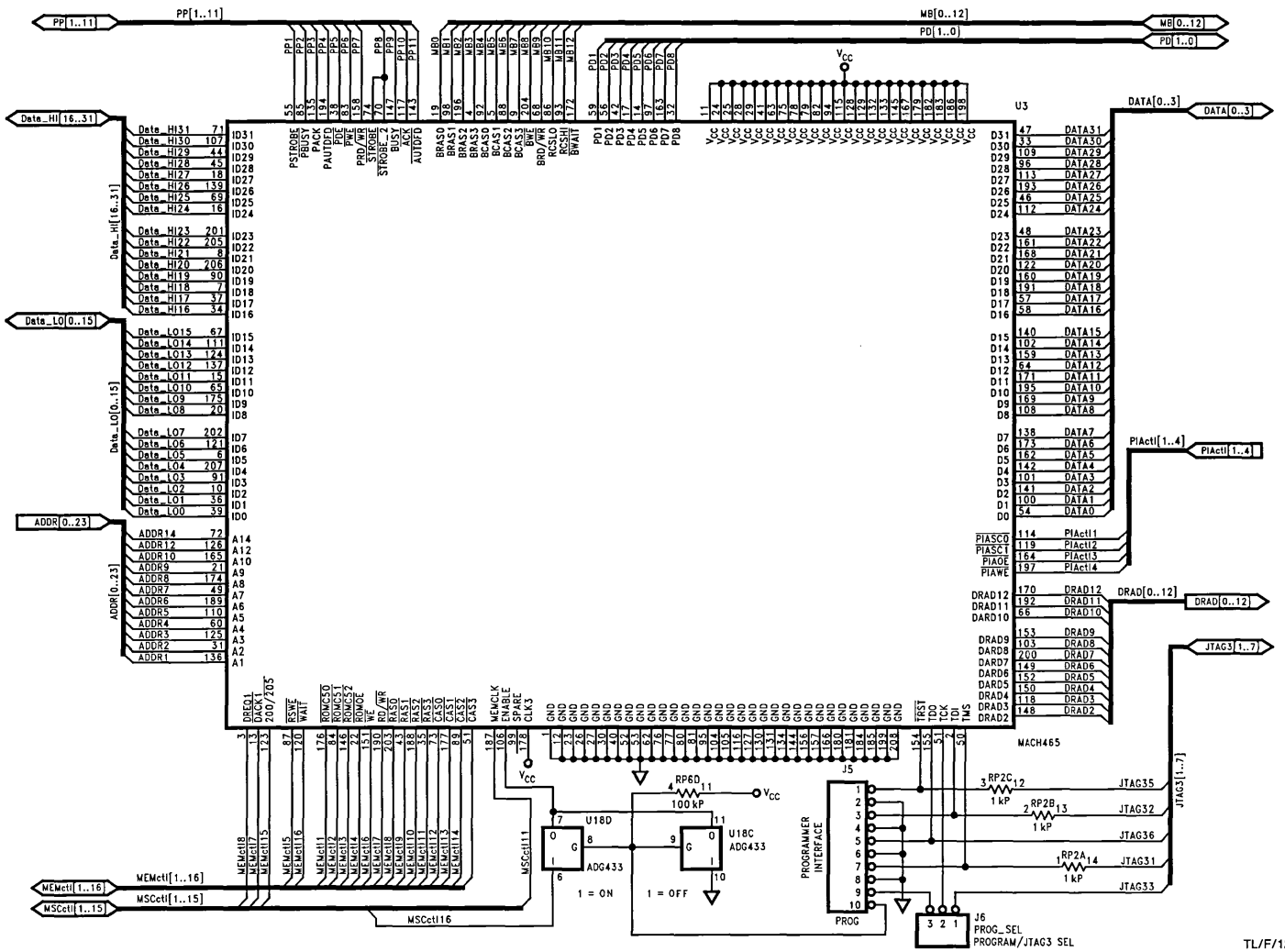
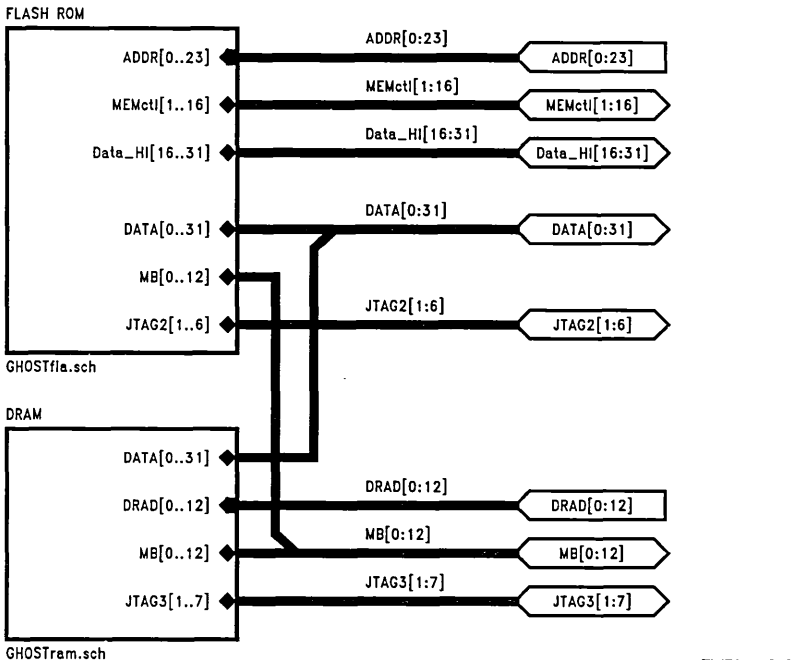
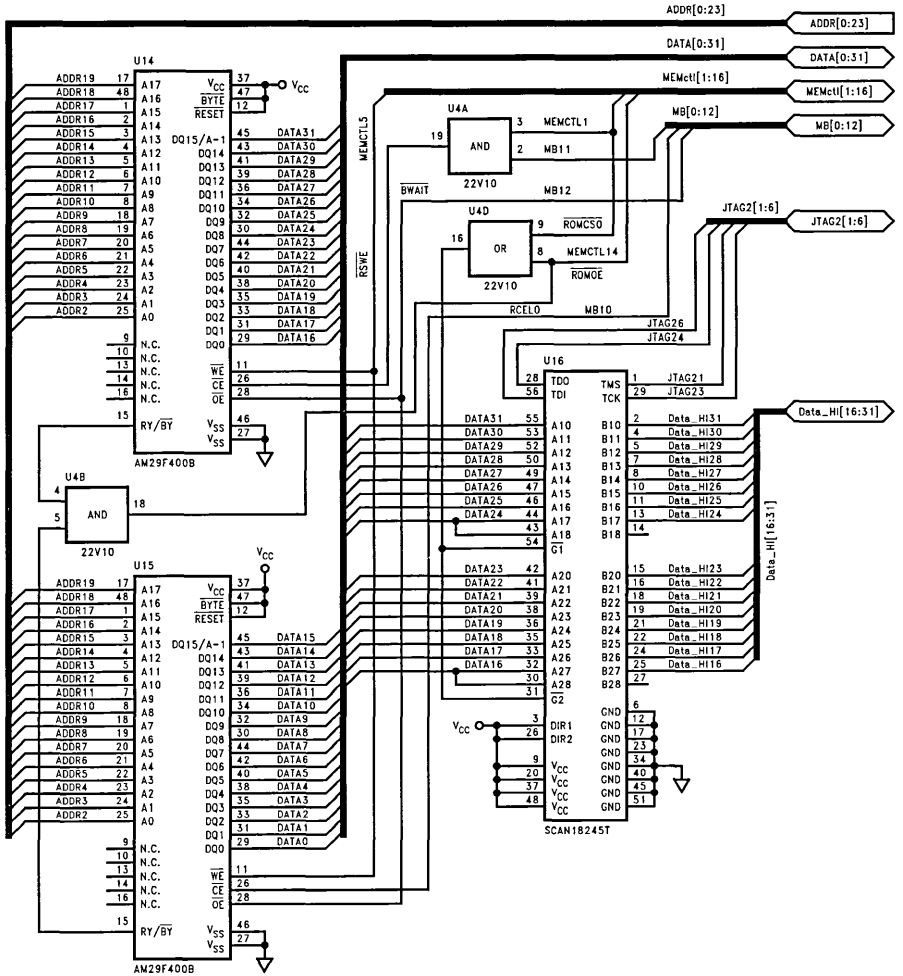


FIGURE 6. Mach465



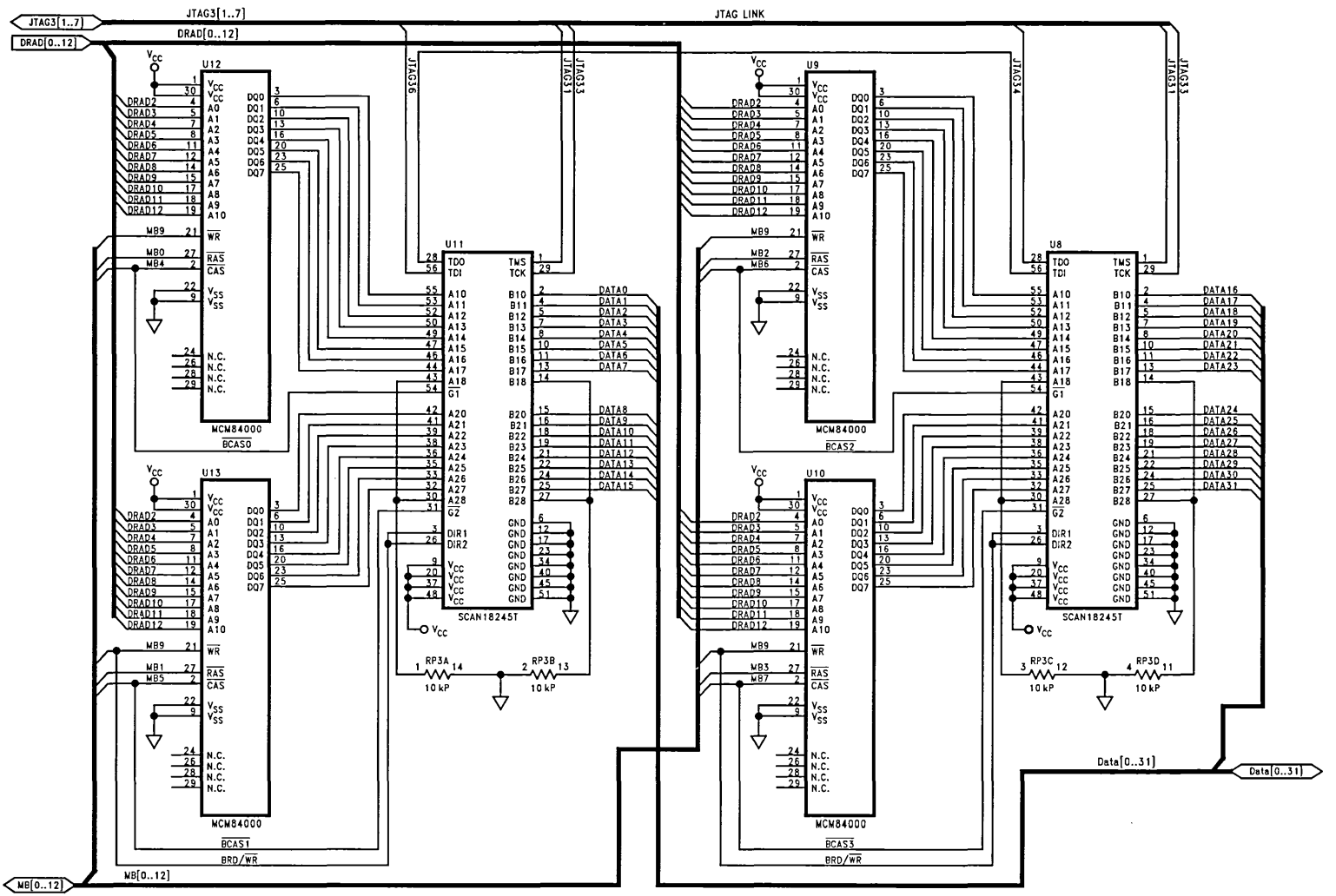
TL/F/12119–6

FIGURE 7. System Memory Block



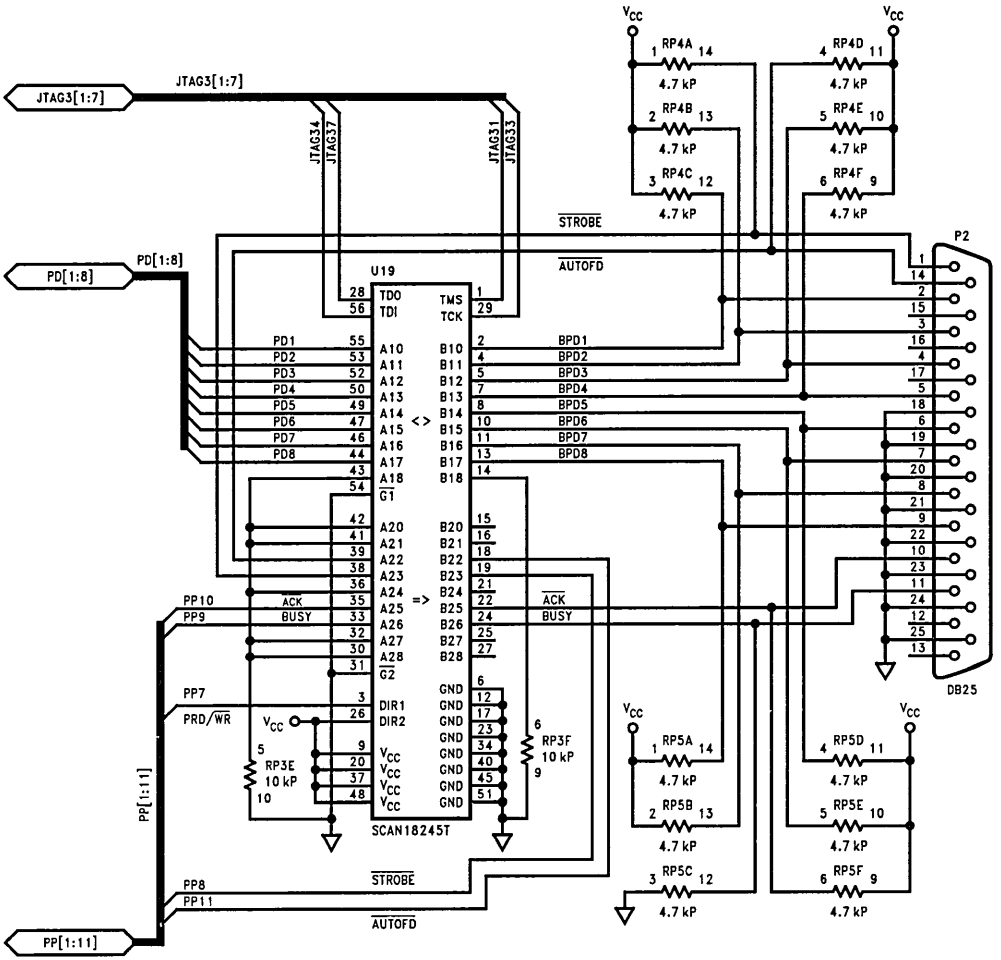
TL/F/12119–7

FIGURE 8. FLASH Memory



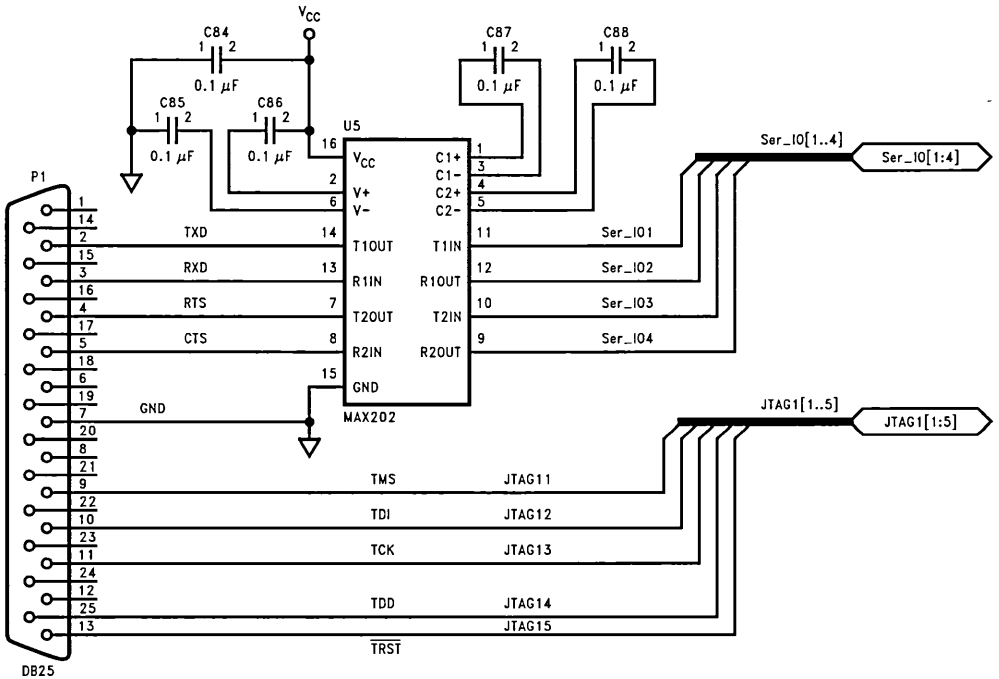
TL/F/12119-8

FIGURE 9. DRAM (Data) Memory



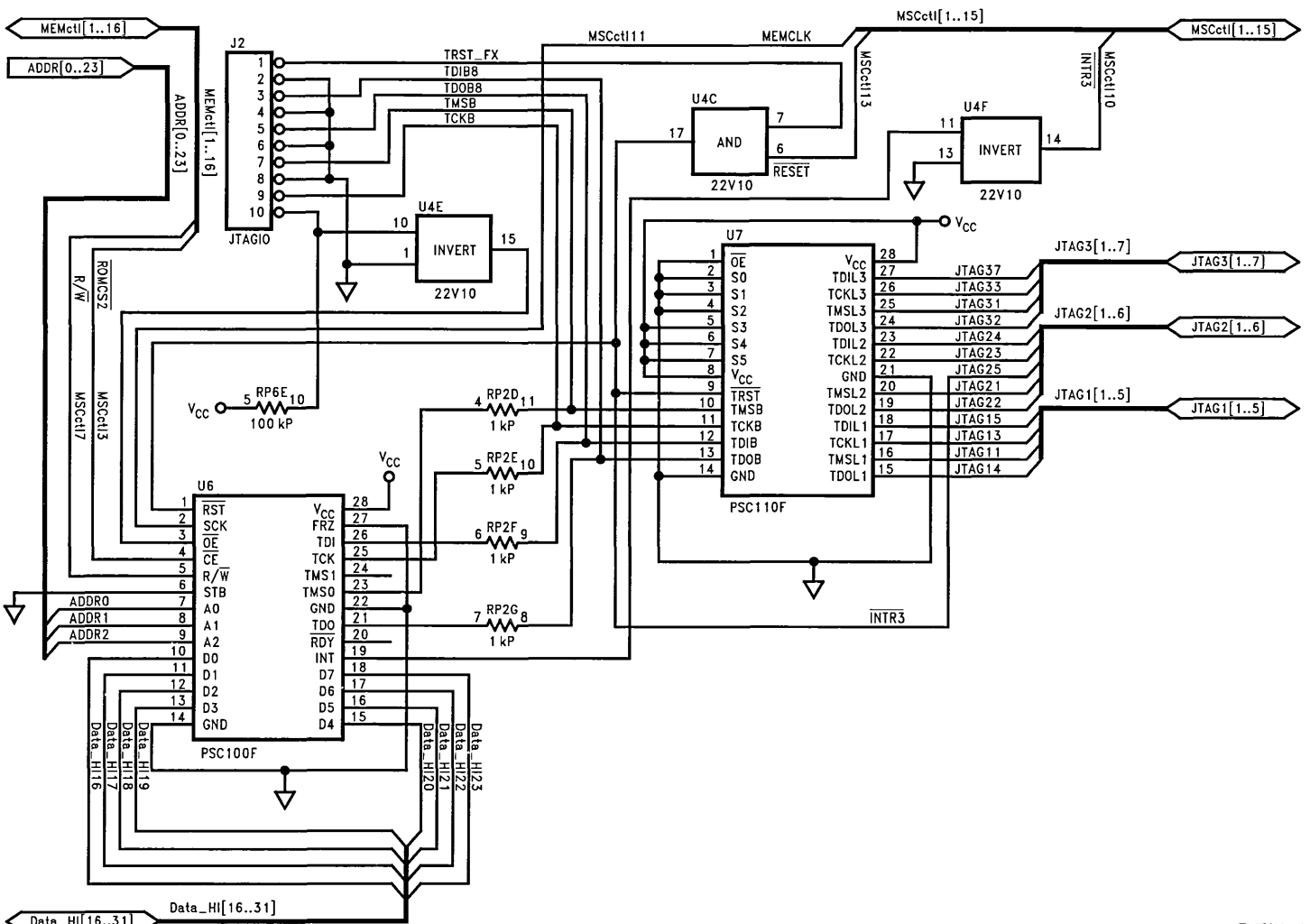
TL/F/12119–9

FIGURE 10. Parallel Interface



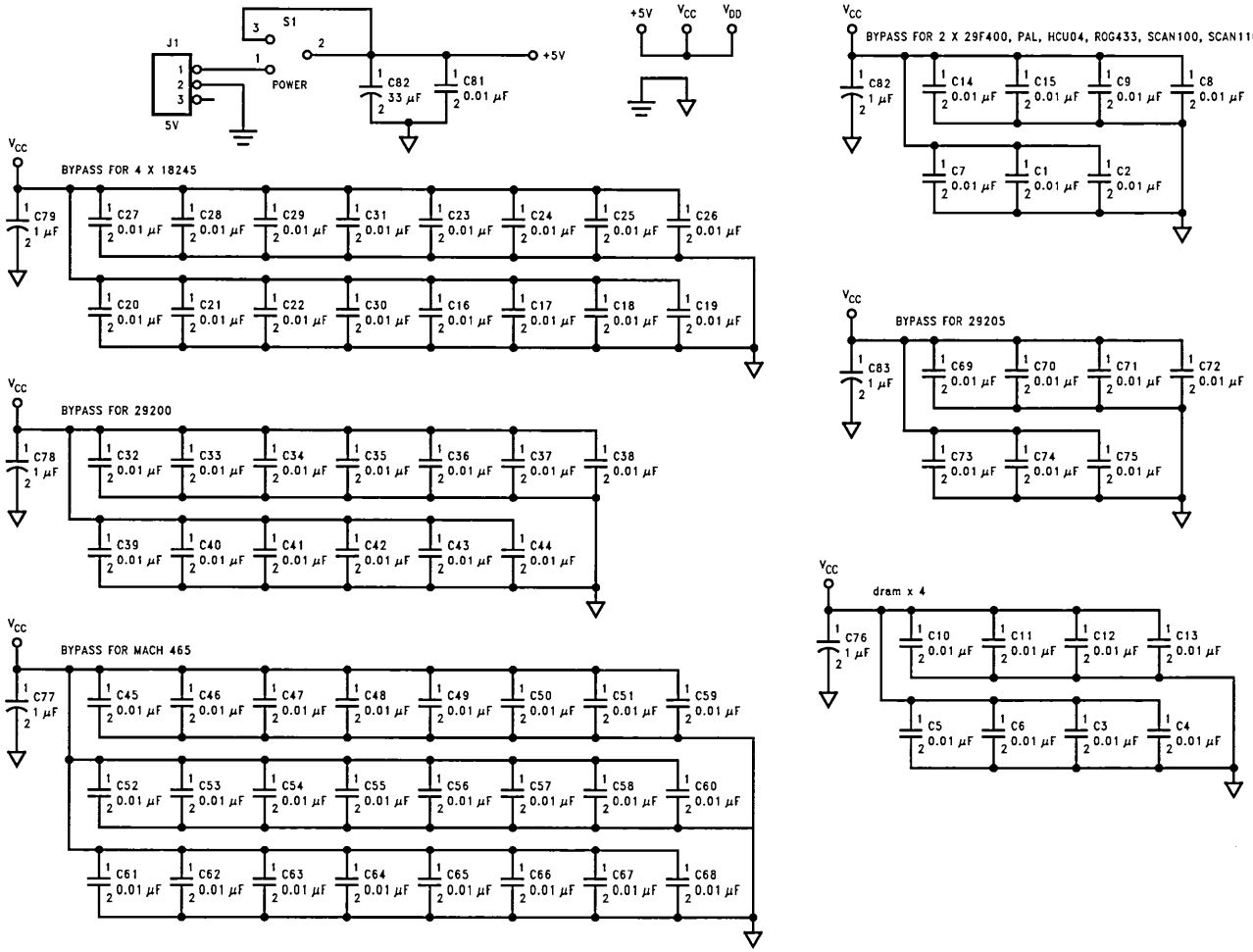
TL/F/12119–10

FIGURE 11. Serial Port



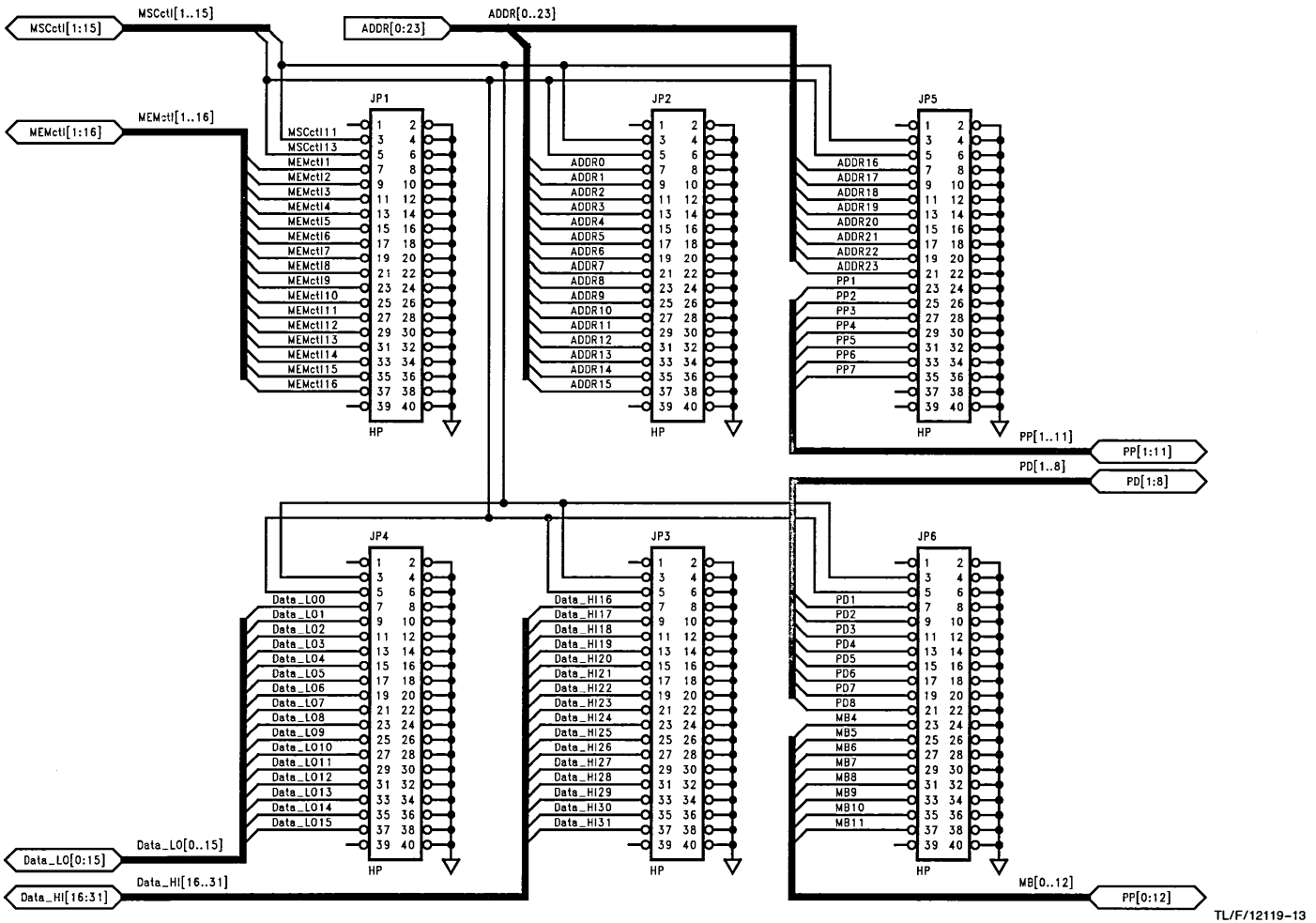
TL/F/12119–11

FIGURE 12. JTAG Interface



TL/F/12119–12

FIGURE 13. Power Supply



TL/F/12119–13

FIGURE 14. HP Logic Analyzer Interface

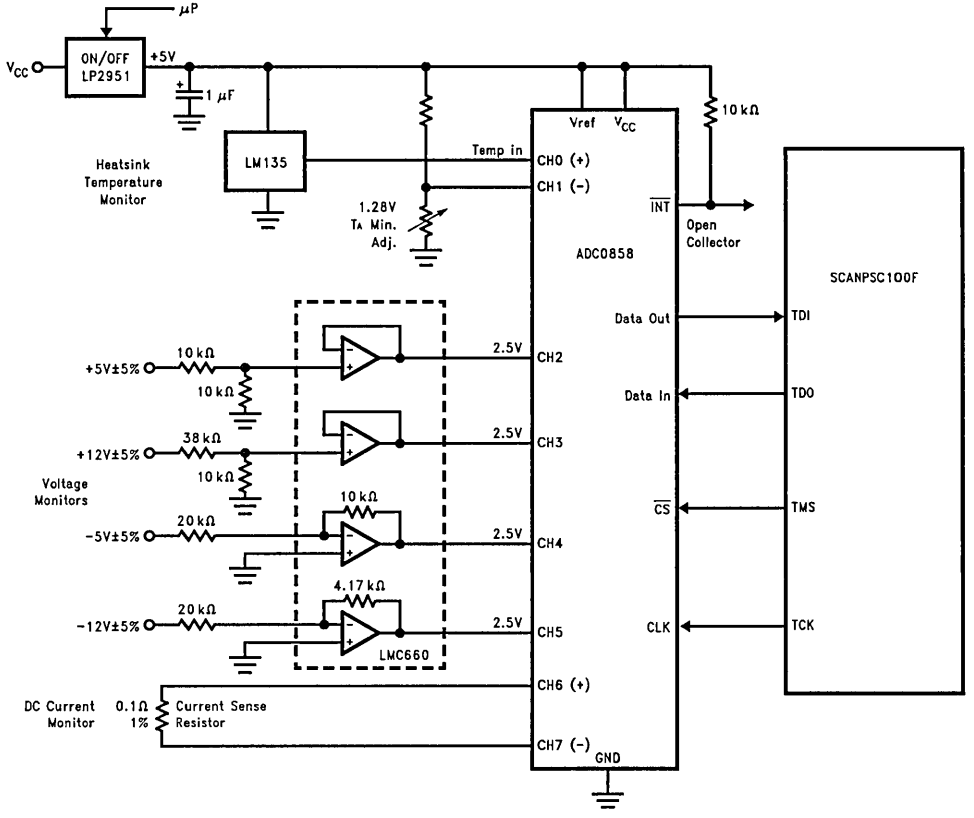
Integration of Analog Test

The IEEE 1149.1 standard is a strictly digital standard and makes no provision for analog test. The IEEE 1149.4 working group has been formed to address the challenging task of developing analog and mixed signal test standards compatible with the existing digital standard.

One solution available today is the ADC0858 Data Acquisition and Monitoring System. This device is an 8-bit programmable WATCHDOG™ that sequentially checks the voltage at each of its eight inputs, producing an interrupt when the voltage is outside a programmed window. Digital readings can be serially downloaded for evaluation. Device programming is accomplished through a serial data port. Since both device programming and data downloads are accomplished via their respective serial ports the device can be readily connected to an 1149.1 ring using either an Embedded Boundary Scan Controller, SCANPSC100F or SCAN Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F Bridge.

The application illustrated shows an ADC0858 monitoring system heat sink temperature, supply voltage and current limit, the tolerances for each being loaded into the onboard RAM. If an input exceeds its allowed range, an interrupt is triggered prompting the host microprocessor to adjust the tolerances, take other corrective action or simply datalog the failure.

In this application, an LP2951 low drop-out regulator supplies reference grade power and the conversion voltage reference for the ADC0858. The four low power Op amps of a CMOS LMC660 scale the inputs to 2.5V and provide a rail-to-output voltage swing that optimizes the ADC0858's full scale conversion. A ±0.5°C temperature accuracy is provided by an LM135 temperature sensor. The 0.1Ω resistor between CH6 and CH7 serves as a current monitor.



TL/F/11575–1

ADC0858CMJ/883 Monitors System Temperature, Voltage and Current

National Semiconductor

ADC0851 and ADC0858 8-Bit Analog Data Acquisition and Monitoring Systems

General Description

The ADC0851 and ADC0858 are 2 and 8 input analog data acquisition systems. They can function as conventional multiple input A/D converters, automatic scanning A/D converters or programmable analog "watchdog" systems. In "watchdog" mode they monitor analog inputs and determine whether these inputs are inside or outside user programmed window limits. This monitoring process takes place independent of the host processor. When any input falls outside of its programmed window limits, an interrupt is automatically generated which flags the processor; the chip can then be interrogated as to exactly which channels crossed which limits.

The advantage of this approach is that its frees the processor from having to frequently monitor analog variables. It can consequently save having to insert many A/D subroutine calls throughout real time application code. In control systems where many variables are continually being monitored this can significantly free up the processor, especially if the variables are DC or slow varying signals.

The Auto A/D conversion feature allows the device to scan through selected input channels, performing an A/D conversion on each channel without the need to select a new channel after each conversion.

Key Specifications

- Resolution — 8 Bits
- Total error — ±½ LSB or ± 1 LSB
- Low power — 50 mW
- Conversion time — 18 μs/Channel
- Limit comparison time — 2 μs/Limit

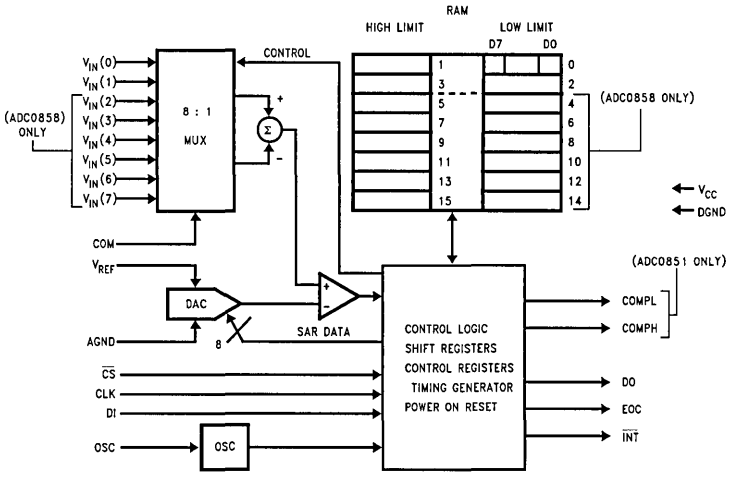
Features

- Watchdog operation signals processor when any channel is outside user programmed window limits
- Frees microprocessor from continually monitoring analog signals and simplifies applications software
- 2 (ADC0851) or 8 (ADC0858) analog input channels
- Single ended or differential input pairs
- COM input for DC offsetting of input voltage
- 4 (ADC0851) and 16 (ADC0858), 8-bit programmable limits
- NSC MICROWIRE™ interface
- Power fail detection
- Auto A/D conversion feature
- Single 5V supply
- Window limits are user programmable via serial interface

Applications

- Instrumentation monitoring and process control
- Digitizing automotive sensor signals
- Embedded diagnostics

Simplified Block Diagram

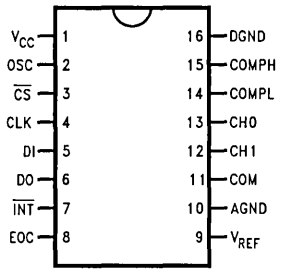


TL/H/11021–22

FIGURE 1

Connection Diagrams

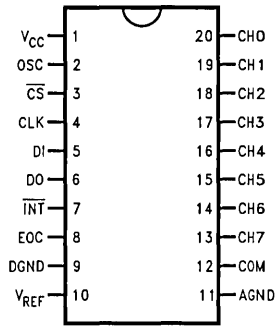
ADC0851
2-Channel MUX
Dual-In-Line Package



TL/H/11021–1

Top View

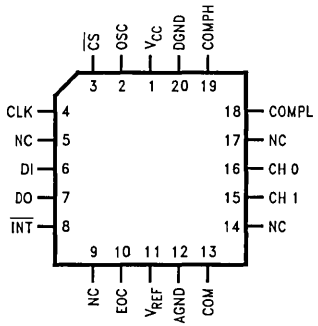
ADC0858
8-Channel MUX
Dual-In-Line Package



TL/H/11021–2

Top View

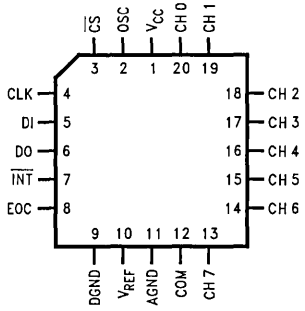
ADC0851 PLCC Package



TL/H/11021–3

Top View

ADC0858 PLCC Package



TL/H/11021–4

Top View

Ordering Information

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC0851BIN, ADC0851CIN	N16E, 16-Pin Plastic DIP
ADC0858BIN, ADC0858CIN	N20A, 20-Pin Plastic DIP
ADC0851BIV, ADC0851CIV	V20A, 20-Lead PLCC
ADC0858BIV, ADC0858CIV	V20A, 20-Lead PLCC

Military ($-55°C \leq T_A \leq +125°C$)	Package
ADC0851CMJ/883	J16A, 16-Pin Ceramic DIP
ADC0858CMJ/883	J20A, 20-Pin Ceramic DIP

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Section 8

SCAN CMOS Test Access Logic Datasheets

Section 8 Contents

National Semiconductor

SCAN18245T
Non-Inverting Transceiver with TRI-STATE® Outputs

General Description

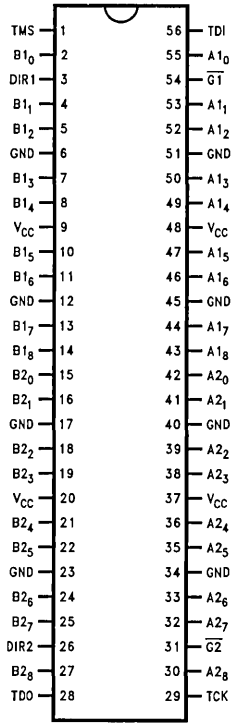
The SCAN18245T is a high speed, low-power bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Dual output enable control signals
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 32 mA/sink 64 mA (Comm), source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP and HIGHZ instructions
- Member of National's SCAN™ Products
- Available as Known Good Die

Ordering Code: See Section 11

Connection Diagram



TL/F/10961–1

Pin Names	Description
$A1_{(0-8)}$	Side A1 Inputs or TRI-STATE Outputs
$B1_{(0-8)}$	Side B1 Inputs or TRI-STATE Outputs
$A2_{(0-8)}$	Side A2 Inputs or TRI-STATE Outputs
$B2_{(0-8)}$	Side B2 Inputs or TRI-STATE Outputs
$\overline{G1}$, $\overline{G2}$	Output Enable Pins
DIR1, DIR2	Direction of Data Flow Pins

Order Number	Description
SCAN18245TSSC	SSOP in Tubes
SCAN18245TSSCX	SSOP in Tape and Reel
SCAN18245TFMQB	Flatpak Military
5962-9311501MXA	Military SMD#

Truth Tables

Inputs		A1 (0–8)		B1 (0–8)
$\overline{G1}$	DIR1			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

Inputs		A2 (0–8)		B2 (0–8)
$\overline{G2}$	DIR2			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

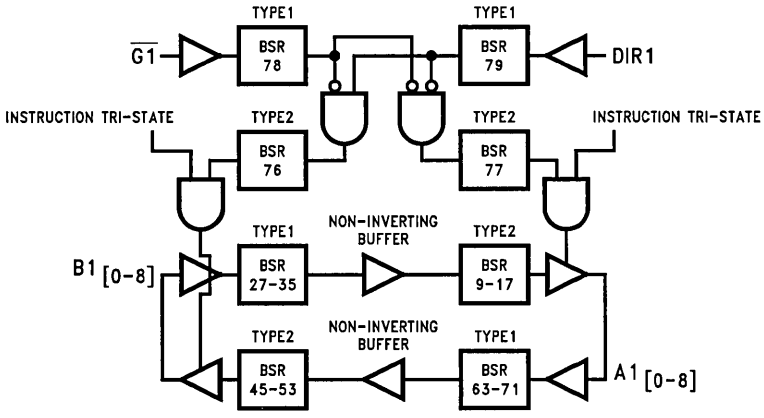
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Functional Description

The SCAN18245 consists of two sets of nine non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Direction pins (DIR1 and DIR2) LOW enables data from B ports to A ports, when HIGH enables data from A ports to B ports. The Output Enable pins ($\overline{G1}$ and $\overline{G2}$) when HIGH disables both A and B ports by placing them in a high impedance condition.

Block Diagrams

A1, B1, $\overline{G1}$ and DIR1

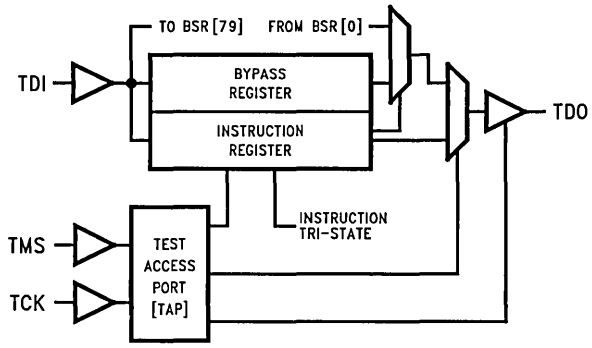


TL/F/10961–2

Note: BSR stands for Boundary Scan Register.

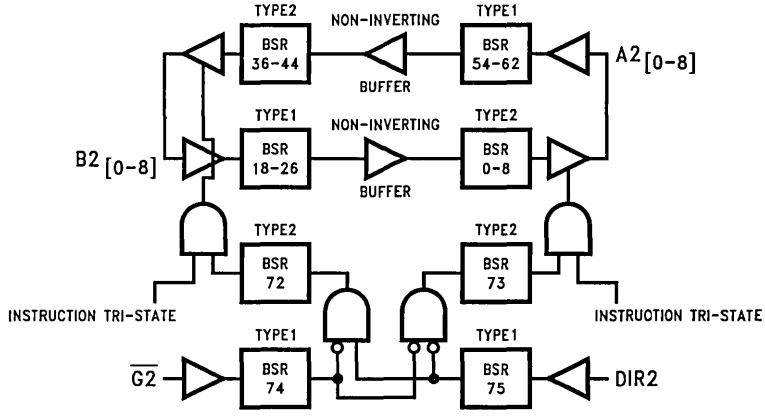
Block Diagrams (Continued)

Tap Controller



TL/F/10961–3

A2, B2, $\overline{G2}$ and DIR2



TL/F/10961–4

Note: BSR stands for Boundary Scan Register.

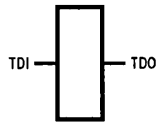
Description of Boundary-Scan Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0

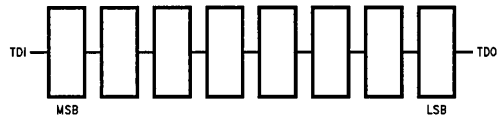


TL/F/10961–9

The INSTRUCTION register is an eight-bit register which captures the value 00111101.

The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18245T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

Instruction Register Scan Chain Definition

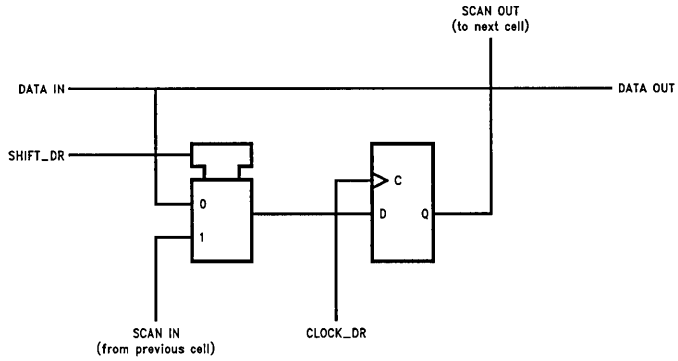


TL/F/10961–10

MSB → LSB

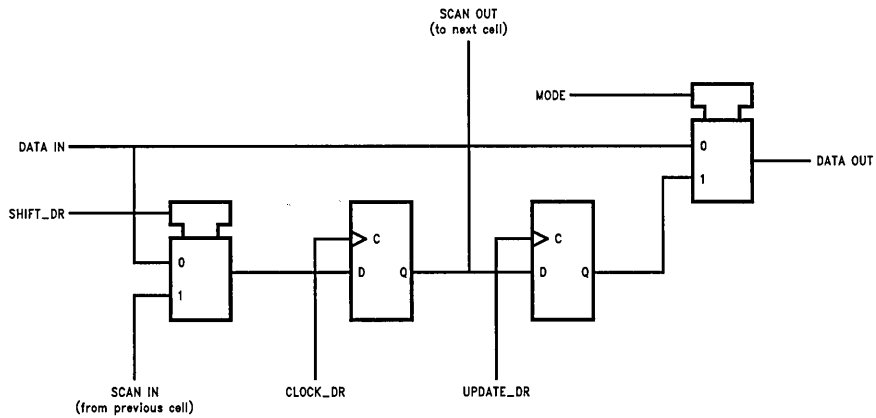
Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All Others	BYPASS

Scan Cell TYPE1



TL/F/10961–7

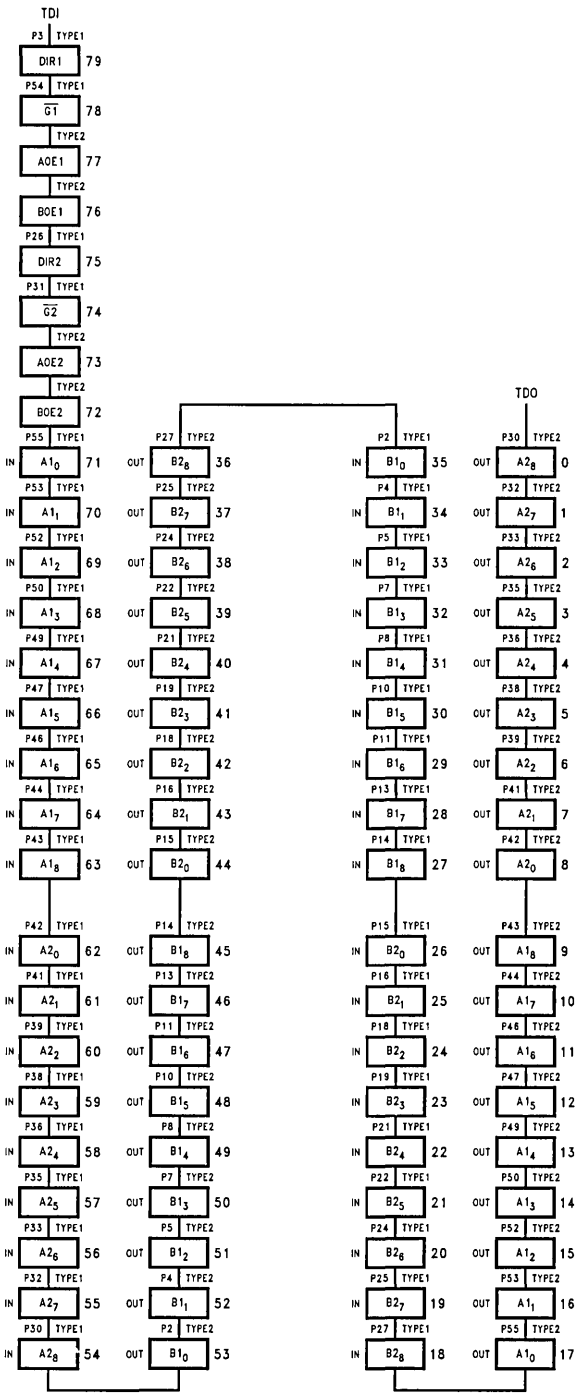
Scan Cell TYPE2



TL/F/10961–8

Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register
Scan Chain Definition (80 Bits In Length)



TL/F/10961–25

Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
79	DIR1	3	Input	TYPE1	
78	$\overline{G1}$	54	Input	TYPE1	
77	AOE_1		Internal	TYPE2	
76	BOE_1		Internal	TYPE2	Control
75	DIR2	26	Input	TYPE1	Signals
74	$\overline{G2}$	31	Input	TYPE1	
73	AOE_2		Internal	TYPE2	
72	BOE_2		Internal	TYPE2	
71	$A1_0$	55	Input	TYPE1	
70	$A1_1$	53	Input	TYPE1	
69	$A1_2$	52	Input	TYPE1	
68	$A1_3$	50	Input	TYPE1	
67	$A1_4$	49	Input	TYPE1	A1–in
66	$A1_5$	47	Input	TYPE1	
65	$A1_6$	46	Input	TYPE1	
64	$A1_7$	44	Input	TYPE1	
63	$A1_8$	43	Input	TYPE1	
62	$A2_0$	42	Input	TYPE1	
61	$A2_1$	41	Input	TYPE1	
60	$A2_2$	39	Input	TYPE1	
59	$A2_3$	38	Input	TYPE1	
58	$A2_4$	36	Input	TYPE1	A2–in
57	$A2_5$	35	Input	TYPE1	
56	$A2_6$	33	Input	TYPE1	
55	$A2_7$	32	Input	TYPE1	
54	$A2_8$	30	Input	TYPE1	
53	$B1_0$	2	Output	TYPE2	
52	$B1_1$	4	Output	TYPE2	
51	$B1_2$	5	Output	TYPE2	
50	$B1_3$	7	Output	TYPE2	
49	$B1_4$	8	Output	TYPE2	B1–out
48	$B1_5$	10	Output	TYPE2	
47	$B1_6$	11	Output	TYPE2	
46	$B1_7$	13	Output	TYPE2	
45	$B1_8$	14	Output	TYPE2	
44	$B2_0$	15	Output	TYPE2	
43	$B2_1$	16	Output	TYPE2	
42	$B2_2$	18	Output	TYPE2	
41	$B2_3$	19	Output	TYPE2	
40	$B2_4$	21	Output	TYPE2	B2–out
39	$B2_5$	22	Output	TYPE2	
38	$B2_6$	24	Output	TYPE2	
37	$B2_7$	25	Output	TYPE2	
36	$B2_8$	27	Output	TYPE2	
35	$B1_0$	2	Input	TYPE1	
34	$B1_1$	4	Input	TYPE1	
33	$B1_2$	5	Input	TYPE1	
32	$B1_3$	7	Input	TYPE1	
31	$B1_4$	8	Input	TYPE1	B1–in
30	$B1_5$	10	Input	TYPE1	
29	$B1_6$	11	Input	TYPE1	
28	$B1_7$	13	Input	TYPE1	
27	$B1_8$	14	Input	TYPE1	

Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index (Continued)

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
26	$B2_0$	15	Input	TYPE1	
25	$B2_1$	16	Input	TYPE1	
24	$B2_2$	18	Input	TYPE1	
23	$B2_3$	19	Input	TYPE1	
22	$B2_4$	21	Input	TYPE1	B2–in
21	$B2_5$	22	Input	TYPE1	
20	$B2_6$	24	Input	TYPE1	
19	$B2_7$	25	Input	TYPE1	
18	$B2_8$	27	Input	TYPE1	
17	$A1_0$	55	Output	TYPE2	
16	$A1_1$	53	Output	TYPE2	
15	$A1_2$	52	Output	TYPE2	
14	$A1_3$	50	Output	TYPE2	
13	$A1_4$	49	Output	TYPE2	A1–out
12	$A1_5$	47	Output	TYPE2	
11	$A1_6$	46	Output	TYPE2	
10	$A1_7$	44	Output	TYPE2	
9	$A1_8$	43	Output	TYPE2	
8	$A2_0$	42	Output	TYPE2	
7	$A2_1$	41	Output	TYPE2	
6	$A2_2$	39	Output	TYPE2	
5	$A2_3$	38	Output	TYPE2	
4	$A2_4$	36	Output	TYPE2	A2–out
3	$A2_5$	35	Output	TYPE2	
2	$A2_6$	33	Output	TYPE2	
1	$A2_7$	32	Output	TYPE2	
0	$A2_8$	30	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)	±70 mA
DC V_{CC} or Ground Current Per Output Pin	±70 mA
Junction Temperature SSOP	+140°C
Storage Temperature	−65°C to +150°C
ESD (Min)	2000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of SCAN circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
SCAN Products	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Commercial	−40°C to +85°C
Military	−55°C to +125°C
Minimum Input Edge Rate dV/dt	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial T_A = +25°C		Military T_A = −55°C to +125°C	Commercial T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Output Voltage	4.5		3.15	3.15	3.15	V	I_{OUT} = −50 μA
		5.5		4.15	4.15	4.15		
		4.5		2.4		2.4	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −32 mA
		5.5		2.4		2.4		
		4.5		2.4	2.4		V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA
		5.5		2.4	2.4			
V_{OL}	Maximum Low Output Voltage	4.5		0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5		0.1	0.1	0.1		
		4.5		0.55		0.55	V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 64 mA
		5.5		0.55		0.55		
		4.5		0.55	0.55		V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 48 mA
		5.5		0.55	0.55			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5		2.8	3.7	3.6	μA	V_I = V_{CC}
				−385	−385	−385	μA	V_I = GND
	Minimum Input Leakage	5.5		−160	−160	−160	μA	V_I = GND
I_{OLD}	†Minimum Dynamic Output Current	5.5		94	63	94	mA	V_{OLD} = 0.8V Max
I_{OHD}				−40	−27	−40	mA	V_{OHD} = 2.0V Min

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$	Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OS}	Output Short Circuit Current	5.5		−100	−100	−100	mA (min)	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5		16.0	168	88	μA	V_O = High TDI, TMS = V_{CC}
		5.5		750	930	820	μA	V_O = High TDI, TMS = GND
I_{CCt}	Maximum I_{CC} Per Input	5.5		2.0	2.0	2.0	mA	V_I = V_{CC}−2.1V
		5.5		2.15	2.15	2.15	mA	V_I = V_{CC}−2.1V TDI/TMS Pin, test one with the other floating

*All outputs loaded; thresholds associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$		Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Fig. No.
			Typ	Guaranteed Limits				
V_{OLP}	Maximum High Output Noise (Notes 2, 3)	5.0	1.0	1.5			V	4-13
V_{OLV}	Minimum Low Output Noise (Notes 2, 3)	5.0	−0.6	−1.2			V	4-13
V_{OHP}	Maximum Overshoot (Notes 1, 3)	5.0	V_{OH}+1.0	V_{OH}+1.5			V	4-13
V_{OHV}	Minimum V_{CC} Droop (Notes 1, 3)	5.0	V_{OH}−1.0	V_{OH}−1.8			V	4-13
V_{IHD}	Minimum High Dynamic Input (Notes 1, 4) Voltage Level	5.5	1.6	2.0	2.0	2.0	V	
V_{ILD}	Maximum Low Dynamic Input (Notes 1, 4) Voltage Level	5.5	1.4	0.8	0.8	0.8	V	

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay A to B, B to A	5.0	1.6 1.6		7.9 7.9	1.6 1.6	9.0 9.3	1.6 1.6	8.5 8.8	ns	4-1, 2
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.2 1.2		8.6 8.5	1.2 1.2	10.0 9.5	1.2 1.2	9.5 9.0	ns	4-3, 4
t_{PZL}, t_{PZH}	Enable Time	5.0	1.6 1.6		11.0 8.5	1.6 1.6	12.5 10.0	1.6 1.6	12.0 9.5	ns	4-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	2.8 2.8		13.2 13.2	2.8 2.8	15.8 15.8	2.8 2.8	14.5 14.5	ns	4-8
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.0 2.0		11.5 11.5	2.0 2.0	12.8 12.8	2.0 2.0	11.9 11.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	2.4 2.4		14.5 14.5	2.4 2.4	16.7 16.7	2.4 2.4	15.8 15.8	ns	4-9, 10
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0		18.0 18.0	4.0 4.0	21.7 21.7	4.0 4.0	19.8 19.8	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	4.0 4.0		18.6 18.6	4.0 4.0	21.2 21.2	4.0 4.0	20.2 20.2	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	4.4 4.4		19.9 19.9	4.4 4.4	23.0 23.0	4.4 4.4	21.5 21.5	ns	4-8
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	3.2 3.2		16.4 16.4	3.2 3.2	19.6 19.6	3.2 3.2	18.2 18.2	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	2.8 2.8		18.0 18.0	2.8 2.8	20.9 20.9	2.8 2.8	19.3 19.3	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	2.8 2.8		18.4 18.4	2.8 2.8	21.8 21.8	2.8 2.8	20.0 20.0	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0		18.9 18.9	4.0 4.0	22.6 22.6	4.0 4.0	20.9 20.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	3.2 3.2		19.9 19.9	3.2 3.2	23.7 23.7	3.2 3.2	21.7 21.7	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	3.6 3.6		21.3 21.3	3.6 3.6	24.9 24.9	3.6 3.6	23.3 23.3	ns	4-9, 10

*Voltage Range 5.0 is 5.0V ±0.5V.

All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF	Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum				
t_S	Setup Time, H or L Data to TCK (Note 1)	5.0	0.0	0.0	0.0	ns	4-11
t_H	Hold Time, H or L TCK to Data (Note 1)	5.0	6.5	7.5	6.5	ns	4-11
t_S	Setup Time, H or L $\overline{G1}$, $\overline{G2}$ to TCK (Note 2)	5.0	0.0	0.0	0.0	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{G1}$, $\overline{G2}$ (Note 2)	5.0	4.0	4.0	4.0	ns	4-11
t_S	Setup Time, H or L DIR1, DIR2 to TCK (Note 4)	5.0	0.0	0.0	0.0	ns	4-11
t_H	Hold Time, H or L TCK to DIR1, DIR2 (Note 4)	5.0	4.0	4.0	4.0	ns	4-11
t_S	Setup Time, H or L Internal AOE_n, BOE_n to TCK (Note 3)	5.0	1.0	1.0	1.0	ns	4-11
t_H	Hold Time, H or L TCK to Internal AOE_n, BOE_n (Note 3)	5.0	4.0	5.0	4.0	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0	7.0	7.0	7.0	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	2.0	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0	1.0	1.0	1.0	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0	3.5	4.5	3.5	ns	4-11
t_W	Pulse Width H L	5.0	15.0 5.0	15.0 5.0	15.0 5.0	ns	4-12
f_{max}	Maximum TCK Clock Frequency	5.0	25	25	25	MHz	
T_{PU}	Wait Time, Power Up to TCK	5.0	100	100	100	ns	
T_{DN}	Power Down Delay	0.0	100	100	100	ms	

*Voltage Range 5.0 is 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: Timing pertains to the TYPE1 BSR and TYPE2 BSR after the buffer (BSR 0–8, 9–17, 18–26, 27–35, 36–44, 45–53, 54–62, 63–71).

Note 2: Timing pertains to BSR 74 and 78 only.

Note 3: Timing pertains to BSR 72, 73, 76 and 77 only.

Note 4: Timing pertains to BSR 75 and 79 only.

Extended AC Electrical Characteristics

Symbol	Parameter	T_A = Comm V_{CC} = Comm C_L = 50 pF 18 Outputs Switching (Note 2)			T_A = Mil V_{CC} = Mil C_L = 50 pF 18 Outputs Switching (Note 2)		T_A = Comm V_{CC} = Comm C_L = 250 pF (Note 3)		T_A = Mil V_{CC} = Mil C_L = 250 pF (Note 3)		Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	2.5 2.5		10.5 10.5	2.5 2.5	11.0 11.0	3.5 3.5	12.0 13.5	3.5 3.5	13.0 14.5	ns
t_{PZH}, t_{PZL}	Output Enable Time	2.5 2.5		10.5 13.5	2.5 2.5	11.0 14.0	(Note 4)		(Note 4)		ns
t_{PHZ}, t_{PLZ}	Output Disable Time	2.0 2.0		9.5 10.0	2.0 2.0	10.0 10.5	(Note 5)		(Note 5)		ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		0.5	1.0				1.0			ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH data to Output		0.5	1.0				1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW.

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

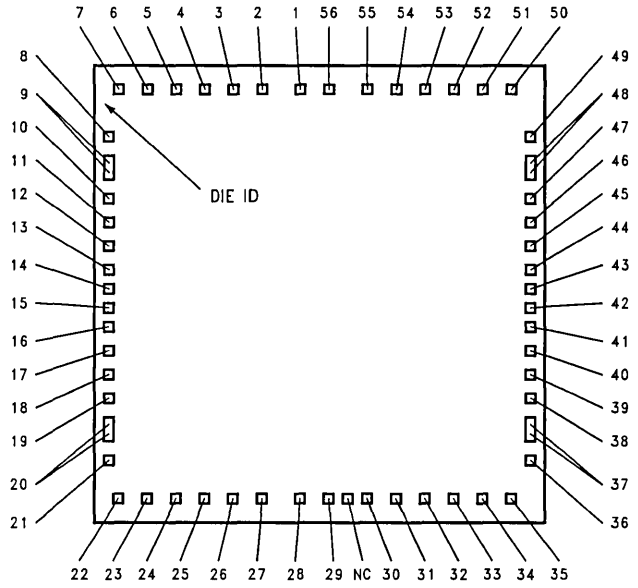
Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4	pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	20	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	41	pF	V_{CC} = 5.0V

Pad Diagram



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SCAN18245T Die Information

Die Revision	**Z**
Die ID	**Y8J245**
Die Size (X)	**4310 μm**
Die Size (Y)	**4310 μm**
Die Thickness	**14 mil**
Substrate Bias	**V_{CC} (optional)**
Backside Coating	**None**

Pad Locations

Signal Number	Signal Name	Pad Location*
1	TMS	−8.58, 77.81
2	$B1_0$	−19.94, 77.81
3	DIR1	−30.50, 77.81
4	$B1_1$	−40.98, 77.81
5	$B1_2$	−53.59, 77.81
6	GND	−63.73, 77.81
7	$B1_3$	−74.47, 77.81
8	$B1_4$	−79.73, 62.30
9	V_{CC}	−79.73, 51.55
		−79.73, 46.28
10	$B1_5$	−79.73, 36.05
11	$B1_6$	−79.73, 27.48
12	GND	−79.72, 19.46
13	$B1_7$	−79.73, 10.09
14	$B1_8$	−79.73, 3.46
15	$B2_0$	−79.73, −3.43
16	$B2_1$	−79.73, −10.06
17	GND	−79.72, −19.43
18	$B2_2$	−79.73, −27.45
19	$B2_3$	−79.73, −36.02
20	V_{CC}	−79.73, −46.24
		−79.73, −51.52
21	$B2_4$	−79.73, −62.27
22	$B2_5$	−74.47, −77.81
23	GND	−63.73, −77.81
24	$B2_6$	−53.59, −77.81
25	$B2_7$	−40.98, −77.81
26	DIR2	−30.50, −77.81
27	$B2_8$	−19.94, −77.81
28	TDO	−8.58, −77.81

Signal Number	Signal Name	Pad Location*
29	TCK	5.54, −77.81
30	$A2_8$	19.94, −77.81
31	$\overline{G2}$	30.50, −77.81
32	$A2_7$	40.98, −77.81
33	$A2_6$	53.59, −77.81
34	GND	63.73, −77.81
35	$A2_5$	74.47, −77.81
36	$A2_4$	79.73, −62.27
37	V_{CC}	79.73, −51.50
		79.73, −46.23
38	$A2_3$	79.73, −36.02
39	$A2_2$	79.73, −27.40
40	GND	79.73, −19.43
41	$A2_1$	79.73, −10.06
42	$A2_0$	79.73, −3.43
43	$A1_8$	79.73, 3.46
44	$A1_7$	79.73, 10.09
45	GND	79.72, 19.46
46	$A1_6$	79.73, 27.43
47	$A1_5$	79.73, 36.05
48	V_{CC}	79.73, 46.26
		79.73, 51.54
49	$A1_4$	79.73, 62.30
50	$A1_3$	74.47, 77.81
51	GND	63.73, 77.81
52	$A1_2$	53.59, 77.81
53	$A1_1$	40.98, 77.81
54	$\overline{G1}$	30.50, 77.81
55	$A1_0$	19.94, 77.81
56	TDI	5.54, 77.81

*X, Y coordinates measured in mils from center of die.

National Semiconductor

SCAN18373T
Transparent Latch with TRI-STATE® Outputs

General Description

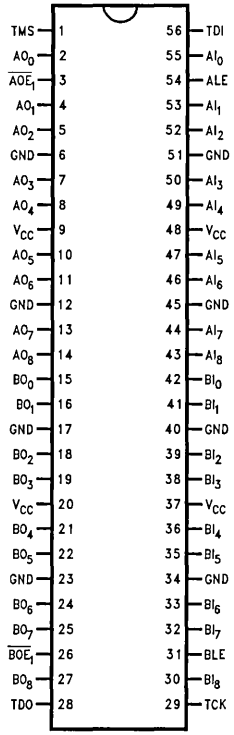
The SCAN18373T is a high speed, low-power transparent latch featuring separate data inputs organized into dual 9-bit bytes with byte-oriented latch enable and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Buffered active-low latch enable
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 32 mA/sink 64 mA (Comm), source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP and HIGHZ instructions
- Member of National's SCAN Products

Ordering Code: See Section 11

Connection Diagram



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Pin Names	Description
$AI_{(0-8)}$, $BI_{(0-8)}$	Data Inputs
ALE, BLE	Latch Enable Inputs
$\overline{AOE_1}$, $\overline{BOE_1}$	TRI-STATE Output Enable Inputs
$AO_{(0-8)}$, $BO_{(0-8)}$	TRI-STATE Latch Outputs

Order Number	Description
SCAN18373TSSC	SSOP in Tubes
SCAN18373TSSCX	SSOP in Tape and Reel
SCAN18373TFMQB	Flatpak Military
5962-9311801MXA	Military SMD #

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Truth Table

Inputs			AO (0–8)
ALE	$\overline{AOE_1}$	AI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	AO_0

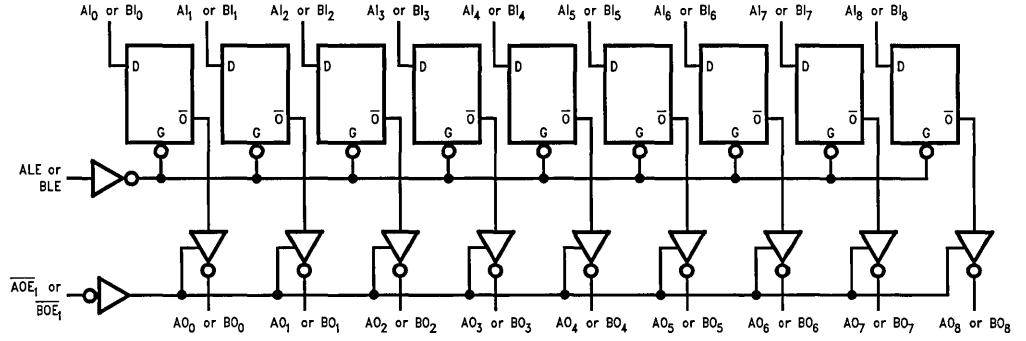
Inputs			BO (0–8)
BLE	$\overline{BOE_1}$	BI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	BO_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
AO_0 = Previous AO before H-to-L transition of ALE
BO_0 = Previous BO before H-to-L transition of BLE

Functional Description

The SCAN18373T consists of two sets of nine D-type latches with TRI-STATE standard outputs. When the Latch Enable (ALE or BLE) input is HIGH, data on the inputs ($AI_{(0-8)}$ or $BI_{(0-8)}$) enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its input changes. When Latch Enable is LOW, the latches store the information that was present on the inputs a set-up time preceding the HIGH-to-LOW transition of the Latch Enable. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{AOE_1}$ or $\overline{BOE_1}$) input. When Output Enable is LOW, the standard outputs are in the 2-state mode. When Output Enable is HIGH, the standard outputs are in the high impedance mode, but this does not interfere with entering new data into the latches.

Logic Diagram



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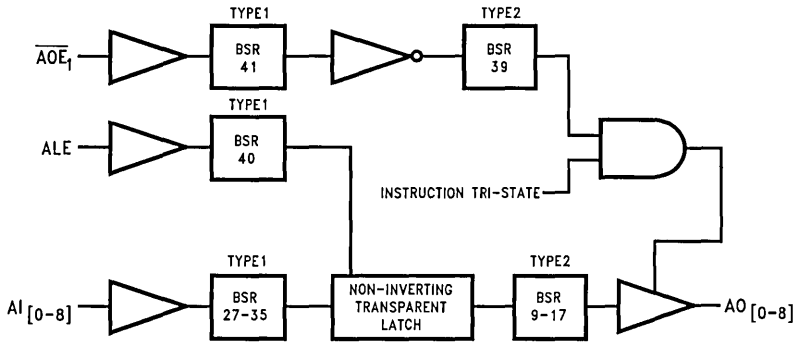
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Block Diagrams

Byte-A



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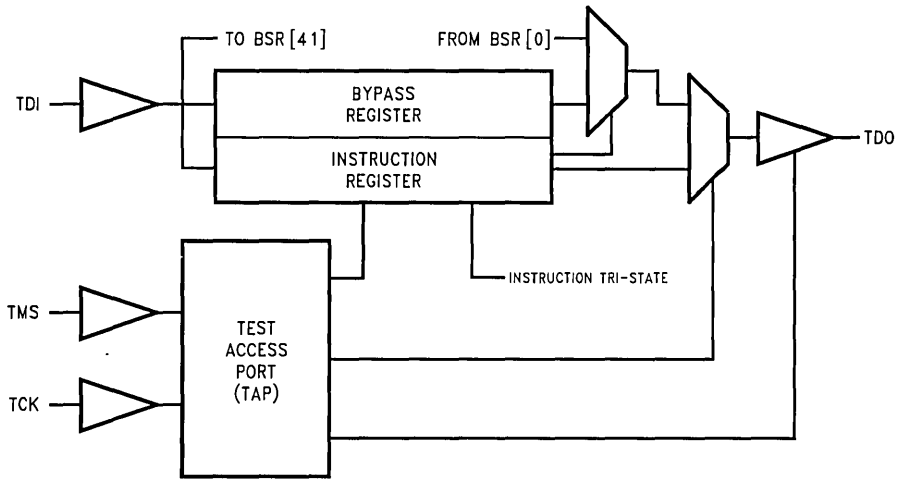
Tap Controller



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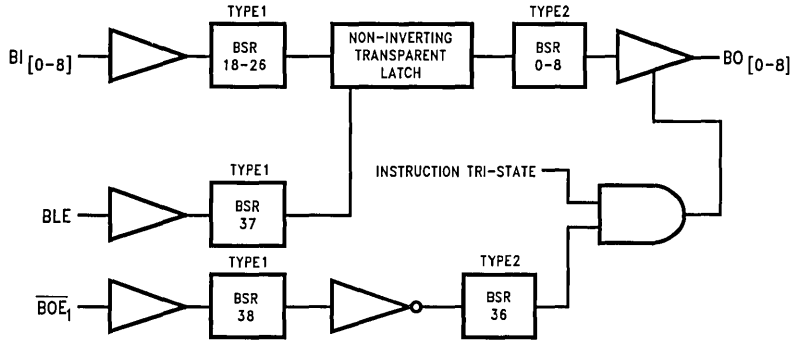
Byte-B



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Note: BSR stands for Boundary Scan Register.

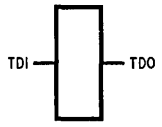
Description of Boundary-Scan Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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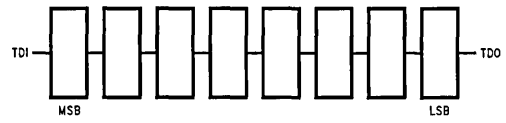
The INSTRUCTION register is an eight-bit register which captures the value 00111101.

The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18373T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

Instruction Register Scan Chain Definition



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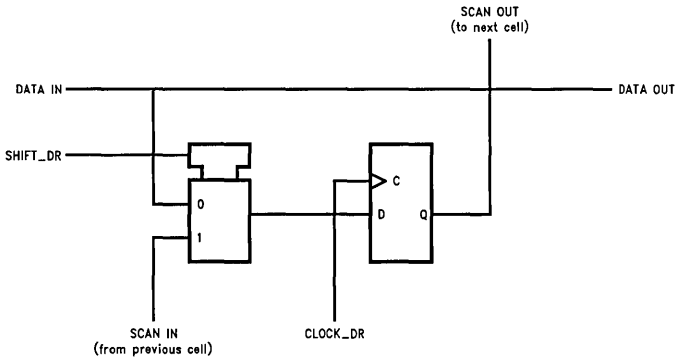
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All Others	BYPASS

Scan Cell TYPE1



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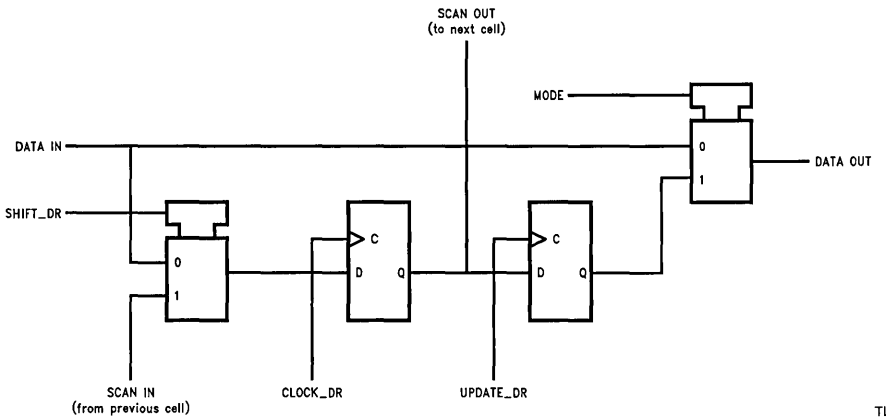
Scan Cell TYPE2



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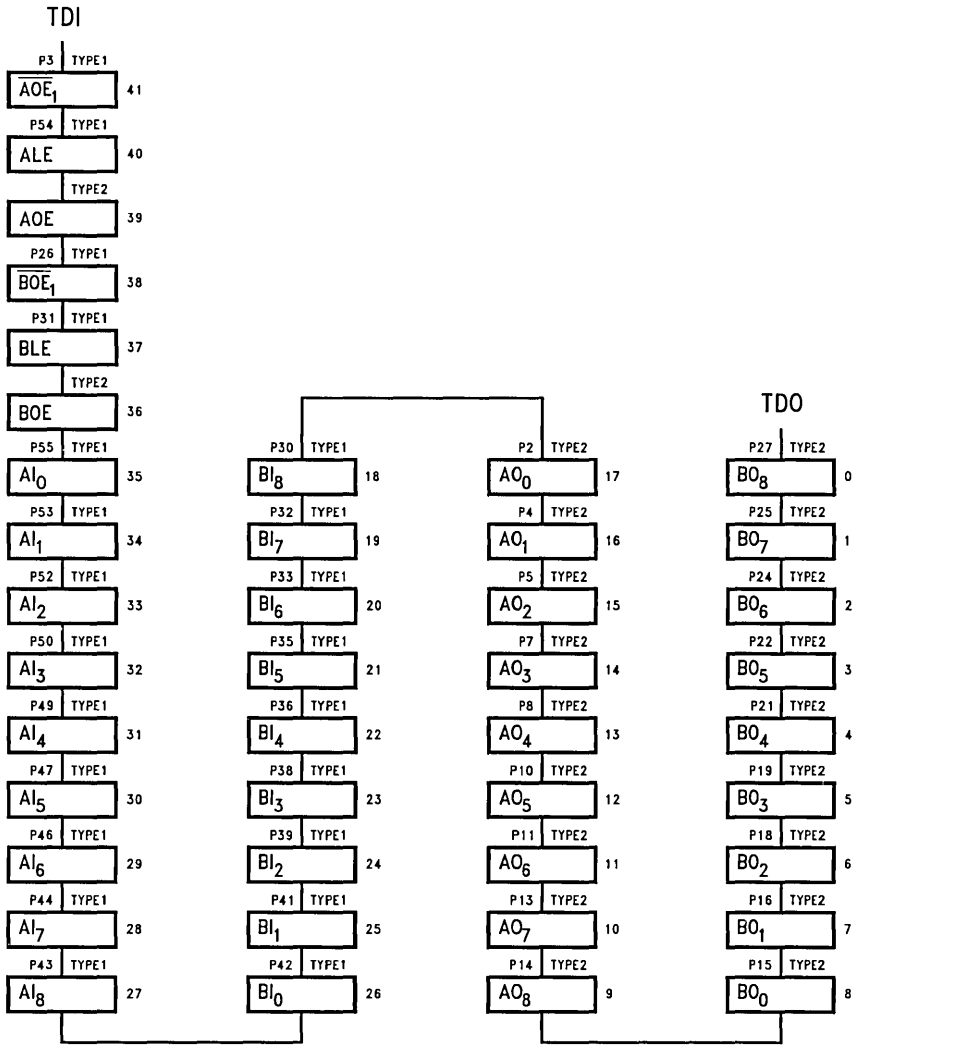
Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register
Scan Chain Definition (42 Bits in Length)



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Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	
40	ACP	54	Input	TYPE1	
39	AOE		Internal	TYPE2	Control
38	$\overline{BOE_1}$	26	Input	TYPE1	Signals
37	BCP	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	A-in
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	B-in
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	A-out
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	B-out
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±70 mA
DC V_{CC} or Ground Current Per Output Pin	±70 mA
Junction Temperature SSOP	+140°C
Storage Temperature	−65°C to +150°C
ESD (Min)	2000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of SCAN™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
SCAN Products	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Commercial	−40°C to +85°C
Military	−55°C to +125°C
Minimum Input Edge Rate dV/dt	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial T_A = +25°C		Military T_A = −55°C to +125°C	Commercial T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Output Voltage	4.5 5.5		3.15 4.15	3.15 4.15	3.15 4.15	V	I_{OUT} = −50 μA
		4.5 5.5		2.4 2.4		2.4 2.4	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −32 mA
		4.5 5.5		2.4 2.4	2.4 2.4		V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA
V_{OL}	Maximum Low Output Voltage	4.5 5.5		0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.55 0.55		0.55 0.55	V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 64 mA
		4.5 5.5		0.55 0.55	0.55 0.55		V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 48 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5		2.8	3.7	3.6	μA	V_I = V_{CC}
				−385	−385	−385	μA	V_I = GND
	Minimum Input Leakage	5.5		−160	−160	−160	μA	V_I = GND
I_{OLD}	†Minimum Dynamic Output Current	5.5		94	63	94	mA	V_{OLD} = 0.8V Max
I_{OHD}				−40	−27	−40	mA	V_{OHD} = 2.0V Min

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$		Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum Output Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH}
I_{OS}	Output Short Circuit Current	5.5		−100	−100	−100	mA Min	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5		16.0	168	88	μA	V_O = Open TDI, TMS = V_{CC}
		5.5		750	930	820	μA	V_O = Open TDI, TMS = GND
I_{CCt}	Maximum I_{CC} per Input	5.5		2.0	2.0	2.0	mA	$V_I = V_{CC} - 2.1V$
		5.5		2.15	2.15	2.15	mA	$V_I = V_{CC} - 2.1V$ TDI/TMS Pin, Test One with the Other Floating

*All outputs loaded; thresholds associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications: See Section 4

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$		Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Fig. No.
			Typ	Guaranteed Limits				
V_{OLP}	Maximum High Output Noise (Notes 2, 3)	5.0	1.0	1.5			V	4-13
V_{OLV}	Minimum Low Output Noise (Notes 2, 3)	5.0	−0.6	−1.2			V	4-13
V_{OHP}	Maximum Overshoot (Notes 1, 3)	5.0	V_{OH} + 1.0	V_{OH} + 1.5			V	4-13
V_{OHV}	Minimum V_{CC} Droop (Notes 1, 3)	5.0	V_{OH} − 1.0	V_{OH} − 1.8			V	4-13
V_{IHD}	Minimum High Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.6	2.0	2.0	2.0	V	
V_{ILD}	Maximum Low Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.4	0.8	0.8	0.8	V	

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n−1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n−1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n−1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay, D to Q	5.0	2.5 2.5		9.0 9.0	2.5 2.5	10.5 10.5	2.5 2.5	9.8 9.8	ns	4-1, 2
t_{PLH}, t_{PHL}	Propagation Delay, LE to Q	5.0	2.5 2.5		10.0 10.5	2.5 2.5	11.0 12.0	2.5 2.5	10.5 11.3	ns	4-1, 2
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.5 1.5		9.0 9.5	1.5 1.5	10.5 10.3	1.5 1.5	9.5 10.0	ns	4-3, 4
t_{PZL}, t_{PZH}	Enable Time	5.0	2.0 2.0		10.9 9.0	2.0 2.0	12.8 10.6	2.0 2.0	11.9 9.7	ns	4-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum				
t_S	Setup Time, H or L Data to LE	5.0	3.0	3.0	3.0	ns	4-5
t_H	Hold Time, H or L LE to Data	5.0	1.5	1.5	1.5	ns	4-5
t_W	LE Pulse Width	5.0	5.0	5.0	5.0	ns	4-2

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	3.5 3.5		13.2 13.2	3.5 3.5	15.8 15.8	3.5 3.5	14.5 14.5	ns	4-8
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.5 2.5		11.5 11.5	2.5 2.5	12.8 12.8	2.5 2.5	11.9 11.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	3.0 3.0		14.5 14.5	3.0 3.0	16.7 16.7	3.0 3.0	15.8 15.8	ns	4-9, 10
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0	5.0 5.0		18.0 18.0	5.0 5.0	21.7 21.7	5.0 5.0	19.8 19.8	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0	5.0 5.0		18.6 18.6	5.0 5.0	21.2 21.2	5.0 5.0	20.2 20.2	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	5.5 5.5		19.9 19.9	5.5 5.5	23.0 23.0	5.5 5.5	21.5 21.5	ns	4-8
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out during Update-DR State	5.0	4.0 4.0		16.4 16.4	4.0 4.0	19.6 19.6	4.0 4.0	18.2 18.2	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out during Update-IR State	5.0	5.0 5.0		19.5 19.5	5.0 5.0	22.4 22.4	5.0 5.0	20.8 20.8	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	5.0 5.0		19.9 19.9	5.0 5.0	23.3 23.3	5.0 5.0	21.5 21.5	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out during Update-DR State	5.0	5.0 5.0		18.9 18.9	5.0 5.0	22.6 22.6	5.0 5.0	20.9 20.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out during Update-IR State	5.0	6.5 6.5		22.4 22.4	6.5 6.5	26.2 26.2	6.5 6.5	24.2 24.2	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	7.0 7.0		23.8 23.8	7.0 7.0	27.4 27.4	7.0 7.0	25.7 25.7	ns	4-9, 10

*Voltage Range 5.0 is 5.0V ±0.5V.

All propagation delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF	Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum				
t_S	Setup Time, Data to TCK (Note 2)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, TCK to Data (Note 2)	5.0	4.5	4.5	4.5	ns	4-11
t_S	Setup Time, H or L $\overline{AOE}_1$, $\overline{BOE}_1$ to TCK (Note 4)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{AOE}_1$, $\overline{BOE}_1$ (Note 4)	5.0	4.5	5.0	4.5	ns	4-11
t_S	Setup Time, H or L Internal AOE, BOE, to TCK (Note 3)	5.0	3.0	3.0	3.0	ns	4–11
t_H	Hold Time, H or L TCK to Internal AOE, BOE (Note 3)	5.0	3.0	3.0	3.0	ns	4–11
t_S	Setup Time ALE, BLE (Note 1) to TCK	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time TCK to ALE, BLE (Note 1)	5.0	3.5	4.0	3.5	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0	8.0	8.0	8.0	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	2.0	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0	4.0	4.0	4.0	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0	4.5	4.5	4.5	ns	4-11
t_W	Pulse Width TCK H L	5.0	15.0 5.0	15.0 5.0	15.0 5.0	ns	4-12
f_{max}	Maximum TCK Clock Frequency	5.0	25	25	25	MHz	
T_{pu}	Wait Time, Power Up to TCK	5.0	100	100	100	ns	
T_{dn}	Power Down Delay	0.0	100	100	100	ms	

*Voltage Range 5.0 is 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: Timing pertains to BSR 37 and 40 only.

Note 2: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26 and 27-35.

Note 3: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

Note 4: Timing pertains to BSR 38 and 41 only.

Extended AC Electrical Characteristics: See Section 4

Symbol	Parameter	T_A = Com, V_{CC} = Com, C_L = 50 pF, 18 Outputs Switching (Note 2)			T_A = Mil, V_{CC} = Mil, C_L = 50 pF, 18 Outputs Switching (Note 2)		T_A = Com, V_{CC} = Com, C_L = 250 pF (Note 3)		T_A = Mil, V_{CC} = Mil, C_L = 250 pF (Note 3)		Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Latch Enable to Output	3.0 3.0		12.0 12.8	3.0 3.0	12.5 13.5	4.0 4.0	13.5 16.0	4.0 4.0	14.5 16.5	ns
t_{PLH} t_{PHL}	Propagation Delay Data to Output	3.0 3.0		11.5 11.5	3.0 3.0	12.0 12.0	4.0 4.0	13.0 14.5	4.0 4.0	14.0 15.5	ns
t_{PZH} t_{PZL}	Output Enable Time	2.5 2.5		10.5 12.5	2.5 2.5	11.0 13.5	(Note 4)		(Note 4)		ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0		10.5 10.5	2.0 2.0	11.0 11.0	(Note 5)		(Note 5)		ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		0.5	1.0				1.0			ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output		0.5	1.0				1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH.

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	13.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	34.0	pF	V_{CC} = 5.0V

National Semiconductor

SCAN18374T
D Flip-Flop with TRI-STATE® Outputs

General Description

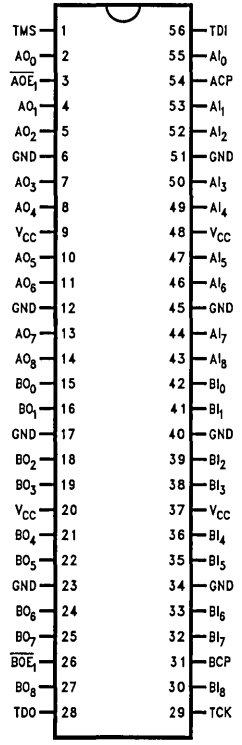
The SCAN18374T is a high speed, low-power D-type flip-flop featuring separate D-type inputs organized into dual 9-bit bytes with byte-oriented clock and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and BOUNDARY-SCAN Architecture with the incorporation of the defined BOUNDARY-SCAN test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 32 mA/sink 64 mA (Comm), source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP and HIGHZ instructions
- Member of National's SCAN Products

Ordering Code: See Section 11

Connection Diagram



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Pin Names	Description
$AI_{(0-8)}$, $BI_{(0-8)}$	Data Inputs
ACP, BCP	Clock Pulse Inputs
$\overline{AOE}_1$, $\overline{BOE}_1$	TRI-STATE Output Enable Inputs
$AO_{(0-8)}$, $BO_{(0-8)}$	TRI-STATE Outputs

Order Number	Description
SCAN18374TSSC	SSOP in Tubes
SCAN18374TSSCX	SSOP in Tape and Reel
SCAN18374TFMQB	Flatpak Military
5962-9320701MXA	Military SMD #

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Truth Tables

Inputs			$AO_{(0-8)}$
ACP	$\overline{AOE}_1$	$AI_{(0-8)}$	
X	H	X	Z
↗	L	L	L
↗	L	H	H

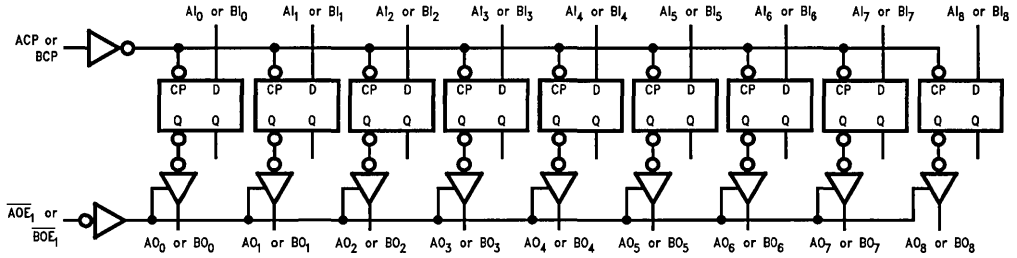
Inputs			$BO_{(0-8)}$
BCP	$\overline{BOE}_1$	$BI_{(0-8)}$	
X	H	X	Z
↗	L	L	L
↗	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = L-to-H Transition

Functional Description

The SCAN18374 consists of two sets of nine edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable pins are common to all flip-flops. Each set of the nine flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (ACP or BCP) transition. With the Output Enable ($\overline{AOE}_1$ or $\overline{BOE}_1$) LOW, the contents of the nine flip-flops are available at the outputs. When the Output Enable is HIGH, the outputs go to the high impedance state. Operation of the Output Enable input does not affect the state of the flip-flops.

Logic Diagram



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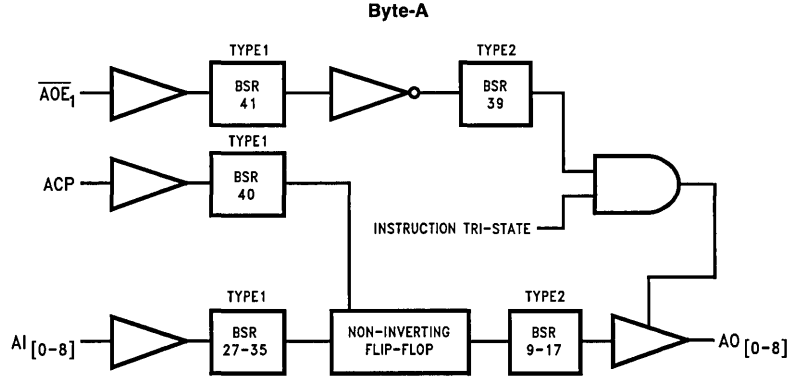
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Block Diagrams



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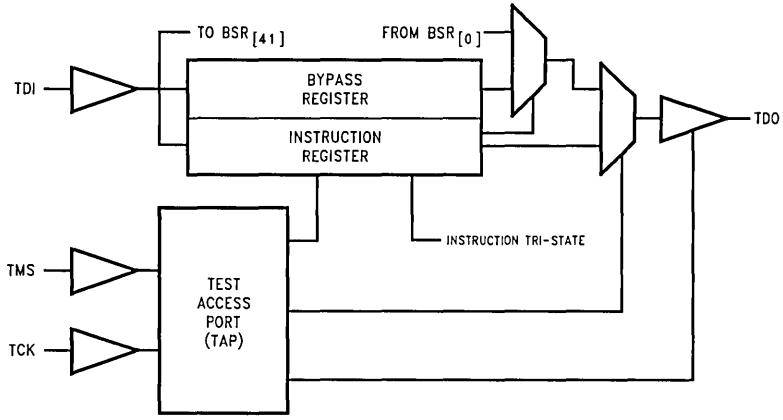
Note: BSR stands for Boundary Scan Register

Block Diagrams (Continued)

Tap Controller



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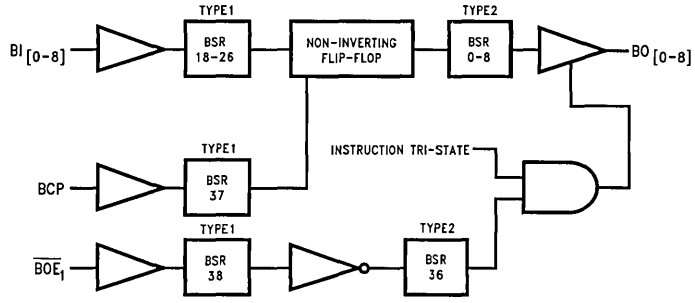
Byte-B



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Note: BSR stands for Boundary Scan Register

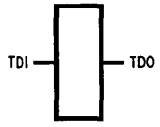
Description of Boundary-Scan Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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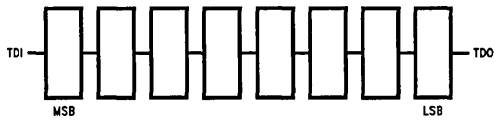
The INSTRUCTION register is an eight-bit register which captures the value 00111101.

The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18374T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

Instruction Register Scan Chain Definition



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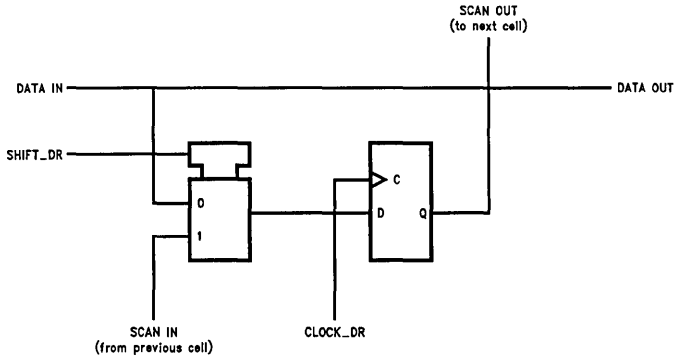
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All Others	BYPASS

Scan Cell TYPE1



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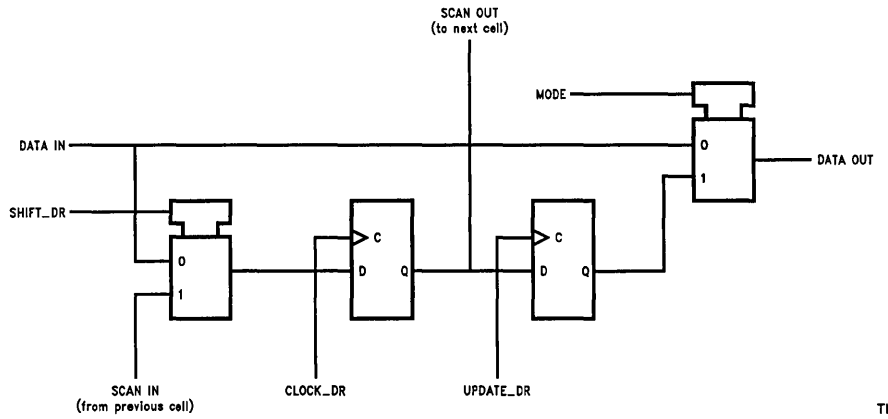
Scan Cell TYPE2



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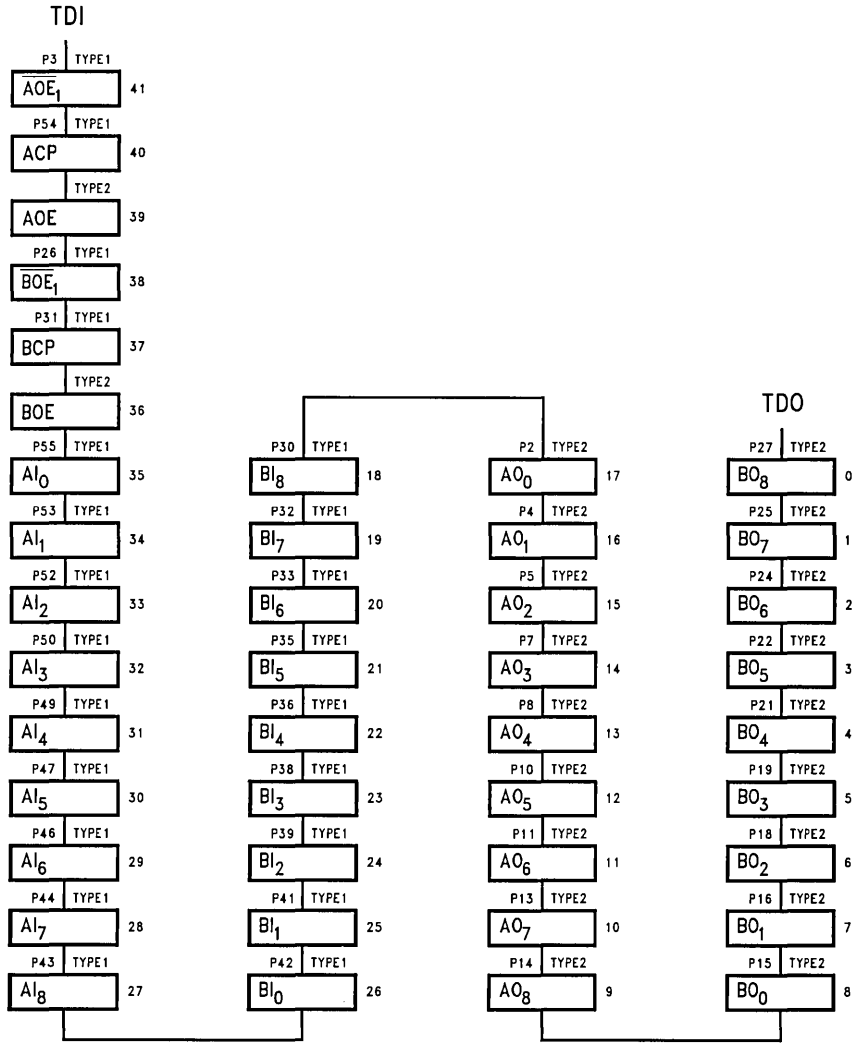
Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register
Scan Chain Definition (42 Bits In Length)



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Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	
40	ACP	54	Input	TYPE1	
39	AOE		Internal	TYPE2	Control
38	$\overline{BOE_1}$	26	Input	TYPE1	Signals
37	BCP	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	A-in
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	B-in
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	A-out
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	B-out
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)	±70 mA
DC V_{CC} or Ground Current Per Output Pin	±70 mA
Junction Temperature SSOP	+140°C
Storage Temperature	−65°C to +150°C
ESD (Min)	2000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of SCAN™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
SCAN Products	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Commercial	−40°C to +85°C
Military	−55°C to +125°C
Minimum Input Edge Rate dV/dt	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial		Military	Commercial	Units	Conditions
			T_A = +25°C		T_A = −55°C to +125°C	T_A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Output Voltage	4.5		3.15	3.15	3.15	V	I_{OUT} = −50 μA
		5.5		4.15	4.15	4.15		
		4.5		2.4		2.4	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −32 mA
		5.5		2.4		2.4		
		4.5		2.4	2.4		V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA
		5.5		2.4	2.4			
V_{OL}	Maximum Low Output Voltage	4.5		0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5		0.1	0.1	0.1		
		4.5		0.55		0.55	V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 64 mA
		5.5		0.55		0.55		
		4.5		0.55	0.55		V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 48 mA
		5.5		0.55	0.55			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5		2.8	3.7	3.6	μA	V_I = V_{CC}
				−385	−385	−385	μA	V_I = GND
	Minimum Input Leakage	5.5		−160	−160	−160	μA	V_I = GND
I_{OLD}	†Minimum Dynamic Output Current	5.5		94	63	94	mA	V_{OLD} = 0.8V Max
I_{OHD}				−40	−27	−40	mA	V_{OHD} = 2.0V Min

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$ Typ	Commercial $T_A = +25°C$ Guaranteed Limits	Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum Output Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH}
I_{OS}	Output Short Circuit Current	5.5		−100	−100	−100	mA (min)	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5		16.0	168	88	μA	V_O = Open TDI, TMS = V_{CC}
		5.5		750	930	820	μA	V_O = Open TDI, TMS = GND
I_{CCt}	Maximum I_{CC} Per Input	5.5		2.0	2.0	2.0	mA	$V_I = V_{CC} - 2.1V$
		5.5		2.15	2.15	2.15		$V_I = V_{CC} - 2.1V$ TDI/TMS Pin, Test One with the Other Floating

*All outputs loaded; thresholds associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications: See Section 4

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$ Typ	Commercial $T_A = +25°C$ Guaranteed Limits	Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Fig. No.
V_{OLP}	Maximum High Output Noise (Notes 2, 3)	5.0	1.0	1.5			V	4-13
V_{OLV}	Minimum Low Output Noise (Notes 2, 3)	5.0	−0.6	−1.2			V	4-13
V_{OHP}	Maximum Overshoot (Notes 1, 3)	5.0	V_{OH}+1.0	V_{OH}+1.5			V	4-13
V_{OHV}	Minimum V_{CC} Droop (Notes 1, 3)	5.0	V_{OH}−1.0	V_{OH}−1.8			V	4-13
V_{IHD}	Minimum High Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.6	2.0	2.0	2.0	V	
V_{ILD}	Maximum Low Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.4	0.8	0.8	0.8	V	

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n − 1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay CP to Q	5.0	2.5 2.5		9.5 10.3	2.5 2.5	11.0 12.0	2.5 2.5	10.5 11.5	ns	4-1, 2
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.5 1.5		9.0 9.0	1.5 1.5	10.5 10.3	1.5 1.5	9.5 10.0	ns	4-3, 4
t_{PZL}, t_{PZH}	Enable Time	5.0	2.0 2.0		10.9 8.9	2.0 2.0	12.6 10.3	2.0 2.0	12.0 9.5	ns	4-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum				
t_S	Setup Time, H or L Data to CP	5.0	3.0	3.0	3.0	ns	4-5
t_H	Hold Time, H or L CP to Data	5.0	1.5	1.5	1.5	ns	4-5
t_W	CP Pulse Width	5.0	5.0	5.0	5.0	ns	4-12
f_{max}	Maximum ACP/BCP Clock Frequency	5.0	100	70	90	MHz	

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	3.5 3.5		13.2 13.2	3.5 3.5	15.8 15.8	3.5 3.5	14.5 14.5	ns	4–8
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.5 2.5		11.5 11.5	2.5 2.5	12.8 12.8	2.5 2.5	11.9 11.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	3.0 3.0		14.5 14.5	3.0 3.0	16.7 16.7	3.0 3.0	15.8 15.8	ns	4-9, 10
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-DR State	5.0	5.0 5.0		18.0 18.0	5.0 5.0	21.7 21.7	5.0 5.0	19.8 19.8	ns	4–8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0		18.6 18.6	5.0 5.0	21.2 21.2	5.0 5.0	20.2 20.2	ns	4–8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.5 5.5		19.9 19.9	5.5 5.5	23.0 23.0	5.5 5.5	21.5 21.5	ns	4–8
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0		16.4 16.4	4.0 4.0	19.6 19.6	4.0 4.0	18.2 18.2	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0		19.5 19.5	5.0 5.0	22.4 22.4	5.0 5.0	20.8 20.8	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.0 5.0		19.9 19.9	5.0 5.0	23.3 23.3	5.0 5.0	21.5 21.5	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	5.0 5.0		18.9 18.9	5.0 5.0	22.6 22.6	5.0 5.0	20.9 20.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	6.5 6.5		22.4 22.4	6.5 6.5	26.2 26.2	6.5 6.5	24.2 24.2	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	7.0 7.0		23.8 23.8	7.0 7.0	27.4 27.4	7.0 7.0	25.7 25.7	ns	4-9, 10

*Voltage Range 5.0 is 5.0V ±0.5V.

All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF	Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum				
t_S	Setup Time, H or L Data to TCK (Note 1)	5.0	3.0	4.5	3.0	ns	4-11
t_H	Hold Time, H or L TCK to Data (Note 1)	5.0	4.5	5.5	4.5	ns	4-11
t_S	Setup Time, H or L $\overline{AOE_1}$, $\overline{BOE_1}$ to TCK (Note 3)	5.0	3.0	3.5	3.0	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{AOE_1}$, $\overline{BOE_1}$ (Note 3)	5.0	4.5	4.5	4.5	ns	4-11
t_S	Setup Time, H or L Internal AOE, BOE to TCK (Note 2)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to Internal AOE, BOE (Note 2)	5.0	3.0	3.0	3.0	ns	4-11
t_S	Setup Time ACP, BCP (Note 4) to TCK	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time TCK to ACP, BCP (Note 4)	5.0	3.5	3.5	3.5	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0	8.0	8.0	8.0	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	2.0	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0	4.0	4.0	4.0	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0	4.5	4.5	4.5	ns	4-11
t_W	Pulse Width TCK H L	5.0	 15.0 5.0	 15.0 5.0	 15.0 5.0	ns	4-12
f_{max}	Maximum TCK Clock Frequency	5.0	25	25	25	MHz	
T_{pu}	Wait Time, Power Up to TCK	5.0	100	100	100	ns	
T_{dn}	Power Down Delay	0.0	100	100	100	ms	

*Voltage Range 5.0 is 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: This delay represents the timing relationship between the data Input and TCK at the associated scan cells numbered 0–8, 9–17, 18–26 and 27–35.

Note 2: This delay represents the timing relationship between AOE, BOE and TCK at scan cells 36 and 39 only.

Note 3: Timing pertains to BSR 38 and 41 only.

Note 4: Timing pertains to BSR 37 and 40 only.

Extended AC Electrical Characteristics

Symbol	Parameter	T_A = Com, V_{CC} = Com, C_L = 50 pF, 18 Outputs Switching (Note 2)			T_A = Mil, V_{CC} = Mil, C_L = 50 pF, 18 Outputs Switching (Note 2)		T_A = COM, V_{CC} = Com, C_L = 250 pF (Note 3)		T_A = Mil, V_{CC} = Mil, C_L = 250 pF (Note 3)		Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	3.0 3.0		11.5 12.5	3.0 3.0	12.0 13.0	4.0 4.0	13.5 16.5	4.0 4.0	14.5 17.0	ns
t_{PZH}, t_{PZL}	Output Enable Time	2.5 2.5		10.5 12.5	2.5 2.5	11.0 13.5	(Note 4)		(Note 4)		ns
t_{PHZ}, t_{PLZ}	Output Disable Time	2.0 2.0		10.5 10.5	2.0 2.0	11.0 11.0	(Note 5)		(Note 5)		ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		0.5	1.0				1.0			ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output		0.5	1.0				1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW.

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	13.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	34.0	pF	V_{CC} = 5.0V

National Semiconductor

SCAN18540T
Inverting Line Driver with TRI-STATE® Outputs

General Description

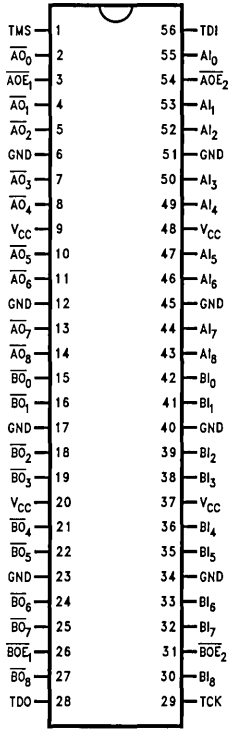
The SCAN18540T is a high speed, low-power line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented paired output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) compliant
- Dual output enable signals per byte
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 32 mA/sink 64 mA (Comm), source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP and HIGHZ instructions
- Member of National's SCAN products

Ordering Code: See Section 11

Connection Diagram



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Pin Names	Description
$AI_{(0-8)}$	Input pins, A side
$BI_{(0-8)}$	Input pins, B side
$\overline{AOE_1}$, $\overline{AOE_2}$	TRI-STATE Output Enable Input pins, A side
$\overline{BOE_1}$, $\overline{BOE_2}$	TRI-STATE Output Enable Input pins, B side
$\overline{AO}_{(0-8)}$	Output pins, A side
$\overline{BO}_{(0-8)}$	Output pins, B side

Truth Tables

Inputs			$\overline{AO}$ (0–8)
$\overline{AOE_1}$	$\overline{AOE_2}$	AI (0–8)	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

Inputs			$\overline{BO}$ (0–8)
$\overline{BOE_1}$	$\overline{BOE_2}$	BI (0–8)	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level L = LOW Voltage Level
X = Immaterial Z = High Impedance

Order Number	Description
SCAN18540TSSC	SSOP in Tubes
SCAN18540TSSCX	SSOP in Tape and Reel
SCAN18540TFMQB	Flatpak Military
5962-9312701MXA	Military SMD #

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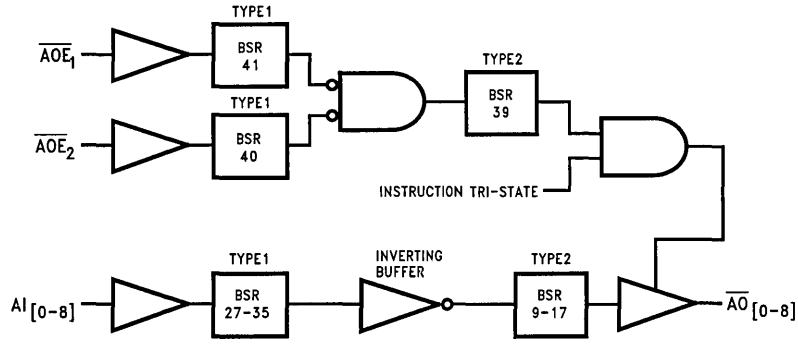
Block Diagrams

Byte-A



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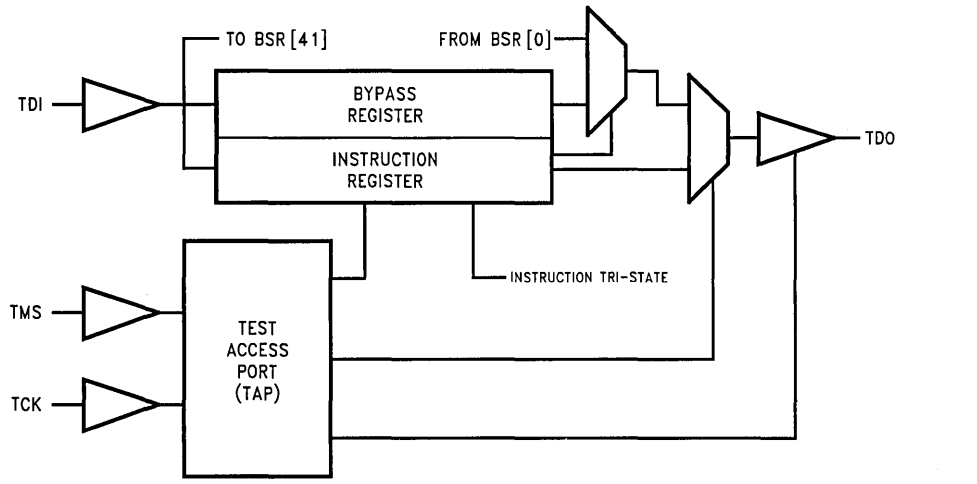
Tap Controller



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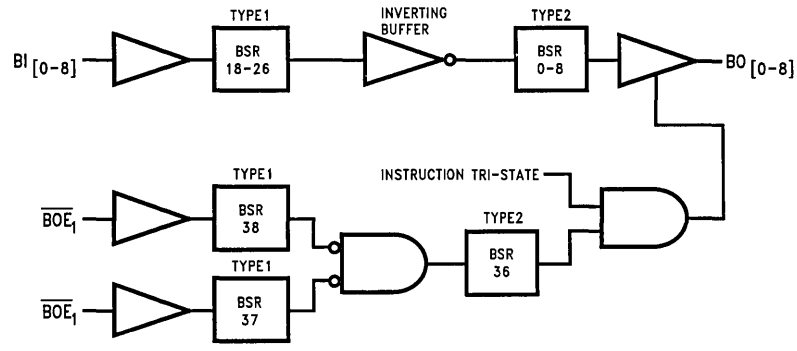
Byte-B



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Note: BSR stands for Boundary Scan Register

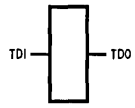
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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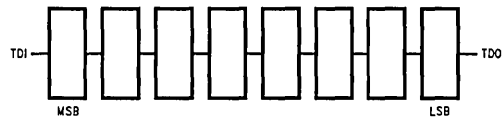
The INSTRUCTION register is an 8-bit register which captures the default value of 01001101. The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18540T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

Instruction Register Scan Chain Definition



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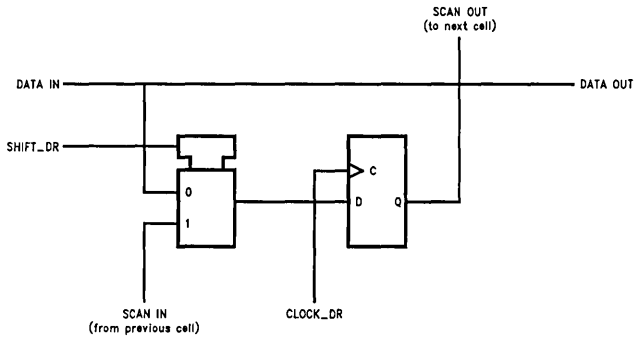
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
All Others	BYPASS

Scan Cell TYPE1



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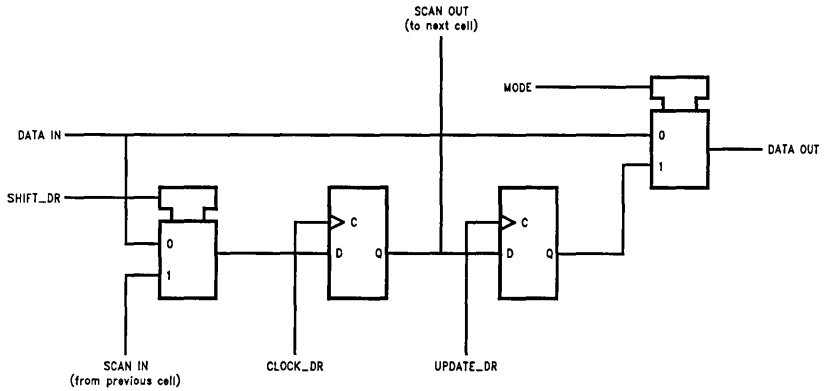
Scan Cell TYPE2



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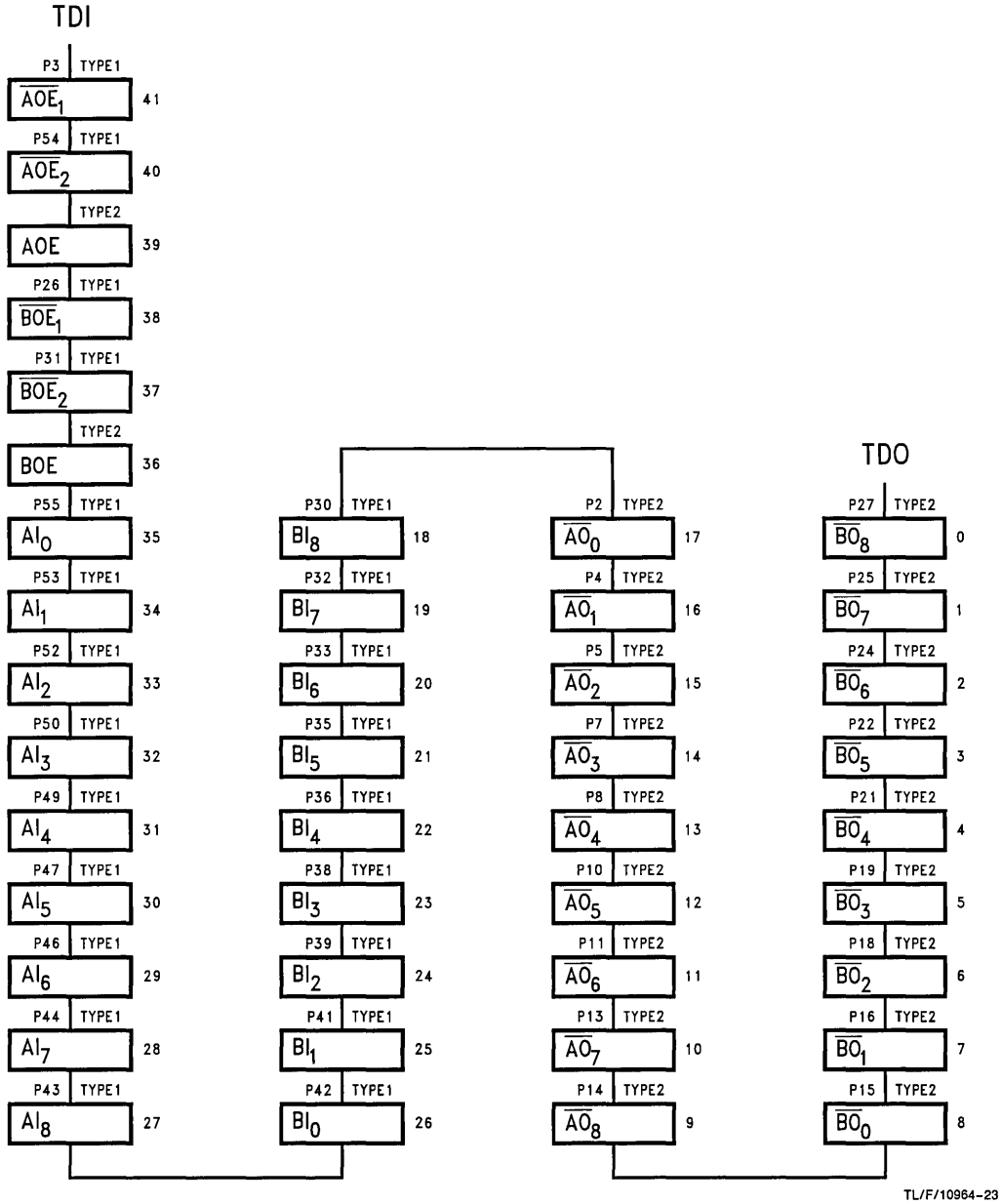
Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register

Scan Chain Definition (42 Bits in Length)



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Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	
40	$\overline{AOE_2}$	54	Input	TYPE1	
39	AOE		Internal	TYPE2	Control
38	$\overline{BOE_1}$	26	Input	TYPE1	Signals
37	$\overline{BOE_2}$	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	A-in
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	B-in
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	A-out
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	B-in
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source/Sink Current (I_O) ±70 mA

DC V_{CC} or Ground Current Per Output Pin ±70 mA

Junction Temperature
- SSOP +140°C

Storage Temperature −65°C to +150°C

ESD (Min) 2000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of SCAN circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- SCAN Products 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- Commercial −40°C to +85°C
- Military −55°C to +125°C

Minimum Input Edge Rate dV/dt 125 mV/ns
- V_{IN} from 0.8V to 2.0V
- V_{CC} @ 4.5V, 5.5V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$	Commercial $T_A = -55°C$ to $+125°C$	Military $T_A = -40°C$ to $+85°C$	Commercial	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Output Voltage	4.5		3.15	3.15	3.15	V	I_{OUT} = −50 μA
		5.5		4.15	4.15	4.15		
		4.5		2.4		2.4	V	$V_{IN} = V_{IL}$ or V_{IH}; I_{OH} = −32 mA
		5.5		2.4		2.4		
		4.5		2.4	2.4		V	$V_{IN} = V_{IL}$ or V_{IH}; I_{OH} = −24 mA
		5.5		2.4	2.4			
V_{OL}	Maximum Low Output Voltage	4.5		0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5		0.1	0.1	0.1		
		4.5		0.55		0.55	V	$V_{IN} = V_{IL}$ or V_{IH}; I_{OL} = 64 mA
		5.5		0.55		0.55		
		4.5		0.55	0.55			$V_{IN} = V_{IL}$ or V_{IH}; I_{OL} = 48 mA
		5.5		0.55	0.55			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5		2.8	3.7	3.6	μA	$V_I = V_{CC}$
				−385	−385	−385	μA	V_I = GND
	Minimum Input Leakage	5.5		−160	−160	−160	μA	V_I = GND
I_{OLD}	†Minimum Dynamic Output Current	5.5		94	63	94	mA	V_{OLD} = 0.8V Max
I_{OHD}				−40	−27	−40	mA	V_{OHD} = 2.0V Min

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$		Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum Output Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH}
I_{OS}	Output Short Circuit Current	5.5		−100	−100	−100	mA Min	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5		16.0	168	88	μA	V_O = Open TDI, TMS = V_{CC}
		5.5		750	930	820	μA	V_O = Open TDI, TMS = GND
I_{CCt}	Maximum I_{CC} Per Input	5.5		2.0	2.0	2.0	mA	V_I = V_{CC}−2.1V
		5.5		2.15	2.15	2.15	mA	V_I = V_{CC}−2.1V TDI/TMS Pin, Test One with the other Floating

*All outputs loaded; thresholds associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications: See Section 4

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$		Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Fig. No.
			Typ	Guaranteed Limits				
V_{OLP}	Maximum High Output Noise (Notes 2, 3)	5.0	1.0	1.5			V	4-13
V_{OLV}	Minimum Low Output Noise (Notes 2, 3)	5.0	−0.6	−1.2			V	4-13
V_{OHP}	Maximum Overshoot (Notes 1, 3)	5.0	V_{OH}+1.0	V_{OH}+1.5			V	4-13
V_{OHV}	Minimum V_{CC} Droop (Notes 1, 3)	5.0	V_{OH}−1.0	V_{OH}−1.8			V	4-13
V_{IHD}	Minimum High Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.6	2.0	2.0	2.0	V	
V_{ILD}	Maximum Low Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.4	0.8	0.8	0.8	V	

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Data to Q	5.0	2.5 2.5		9.0 9.0	2.5 2.5	10.5 10.5	2.5 2.5	9.8 9.8	ns	4-1, 2
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.5 1.5		10.2 10.2	1.5 1.5	11.2 11.2	1.5 1.5	10.7 10.7	ns	4-3, 4
t_{PZL}, t_{PZH}	Enable Time	5.0	2.0 2.0		11.8 9.5	2.0 2.0	13.5 11.5	2.0 2.0	12.8 10.5	ns	4-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	3.5 3.5		13.2 13.2	3.5 3.5	15.8 15.8	3.5 3.5	14.5 14.5	ns	4-8
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.5 2.5		11.5 11.5	2.5 2.5	12.8 12.8	2.5 2.5	11.9 11.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	3.0 3.0		14.5 14.5	3.0 3.0	16.7 16.7	3.0 3.0	15.8 15.8	ns	4-9, 10
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update--DR State	5.0	5.0 5.0		18.0 18.0	5.0 5.0	21.7 21.7	5.0 5.0	19.8 19.8	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0		18.6 18.6	5.0 5.0	21.2 21.2	5.0 5.0	20.2 20.2	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.5 5.5		19.9 19.9	5.5 5.5	23.0 23.0	5.5 5.5	21.5 21.5	ns	4-8
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0		16.4 16.4	4.0 4.0	19.6 19.6	4.0 4.0	18.2 18.2	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0		19.5 19.5	5.0 5.0	22.4 22.4	5.0 5.0	20.8 20.8	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.0 5.0		19.9 19.9	5.0 5.0	23.3 23.3	5.0 5.0	21.5 21.5	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	5.0 5.0		18.9 18.9	5.0 5.0	22.6 22.6	5.0 5.0	20.9 20.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	6.5 6.5		22.4 22.4	6.5 6.5	26.2 26.2	6.5 6.5	24.2 24.2	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	7.0 7.0		23.8 23.8	7.0 7.0	27.4 27.4	7.0 7.0	25.7 25.7	ns	4-9, 10

*Voltage Range 5.0 is 5.0V ±0.5V.

All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF	Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum				
t_S	Setup Time, H or L Data to TCK (Note 1)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to Data (Note 1)	5.0	4.5	5.5	4.5	ns	4-11
t_S	Setup Time, H or L $\overline{AOE}_n$, $\overline{BOE}_n$ to TCK (Note 3)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{AOE}_n$, $\overline{BOE}_n$ (Note 3)	5.0	4.5	4.5	4.5	ns	4-11
t_S	Setup Time, H or L Internal AOE, BOE, to TCK (Note 2)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to Internal AOE, BOE (Note 2)	5.0	3.0	3.0	3.0	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0	8.0	8.0	8.0	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	2.0	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0	4.0	4.0	4.0	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0	4.5	4.5	4.5	ns	4-11
t_W	Pulse Width TCK H TCK L	5.0	15.0 5.0	15.0 5.0	15.0 5.0	ns	4-12
f_{max}	Maximum TCK Clock Frequency	5.0	25	25	25	MHz	
T_{PU}	Wait Time, Power Up to TCK	5.0	100	100	100	ns	
T_{DN}	Power Down Delay	0.0	100	100	100	ms	

*Voltage Range 5.0 is 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26, and 27-35.

Note 2: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

Note 3: Timing pertains to BSR 37, 38, 40 and 41.

Extended AC Electrical Characteristics: See Section 4

Symbol	Parameter	T_A = Com, V_{CC} = Com, C_L = 50 pF, 18 Outputs Switching (Note 2)			T_A = Mil, V_{CC} = Mil, C_L = 50 pF, 18 Outputs Switching (Note 2)		T_A = Com, V_{CC} = Com, C_L = 250 pF (Note 3)		T_A = Mil, V_{CC} = Mil, C_L = 250 pF (Note 3)		Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	3.0 3.0		11.0 11.0	3.0 3.0	11.5 11.5	4.0 4.0	13.0 15.0	4.0 4.0	14.0 16.0	ns
t_{PZH}, t_{PZL}	Output Enable Time	2.5 2.5		11.5 14.0	2.5 2.5	12.5 14.5	(Note 4)		(Note 4)		ns
t_{PHZ}, t_{PLZ}	Ouput Disable Time	2.0 2.0		11.5 11.5	2.0 2.0	12.0 12.0	(Note 5)		(Note 5)		ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		0.5	1.0				1.0			ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output		0.5	1.0				1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination LOW to HIGH and/or HIGH to LOW.

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	13.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	34.0	pF	V_{CC} = 5.0V

National Semiconductor

SCAN18541T
Non-Inverting Line Driver with TRI-STATE® Outputs

General Description

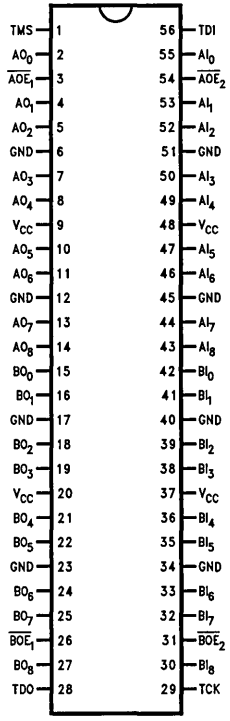
The SCAN18541T is a high speed, low-power line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented paired output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Dual output enable signals per byte
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 32 mA/sink 64 mA (Comm), source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP and HIGHZ instructions
- Member of National's SCAN Products

Ordering Code: See Section 11

Connection Diagram



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Pin Names

Pin Names	Description
$AI_{(0-8)}$	Input Pins, A Side
$BI_{(0-8)}$	Input Pins, B Side
$\overline{AOE_1}$, $\overline{AOE_2}$	TRI-STATE Output Enable Input Pins, A Side
$\overline{BOE_1}$, $\overline{BOE_2}$	TRI-STATE Output Enable Input Pins, B Side
$AO_{(0-8)}$	Output Pins, A Side
$AO_{(0-8)}$	Output Pins, B Side

Truth Tables

Inputs			AO (0–8)
$\overline{AOE_1}$	$\overline{AOE_2}$	AI (0–8)	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

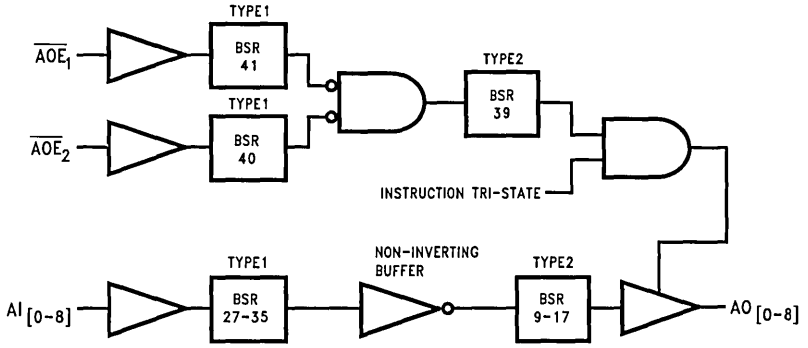
Inputs			BO (0–8)
$\overline{BOE_1}$	$\overline{BOE_2}$	BI (0–8)	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Order Number	Description
SCAN18541TSSC	SSOP in Tubes
SCAN18541TSSCX	SSOP in Tape and Reel
SCAN18541TFMQB	Flatpak Military
5962-9311601MXA	Military SMD#

Block Diagrams

Byte A



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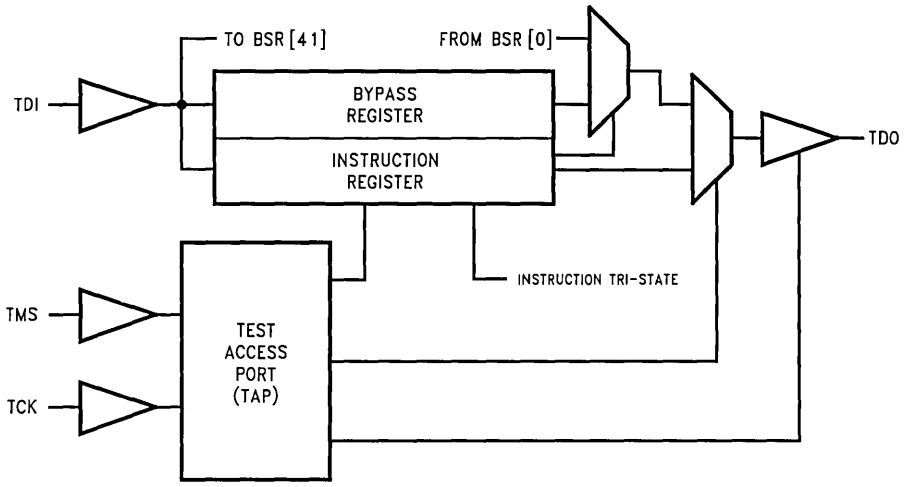
Tap Controller



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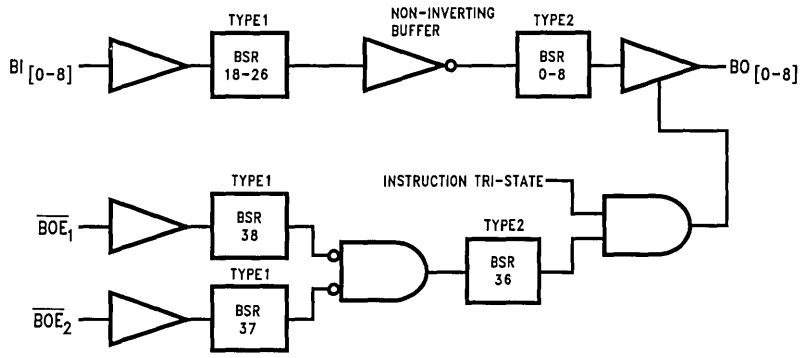
Byte B



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Note: BSR stands for Boundary Scan Register.

Description of Boundary-Scan Circuitry

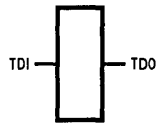
The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition

Logic 0



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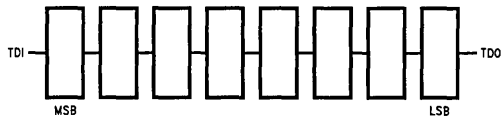
The INSTRUCTION register is an 8-bit register which captures the default value of 10000001. The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18541T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

Instruction Register Scan Chain Definition



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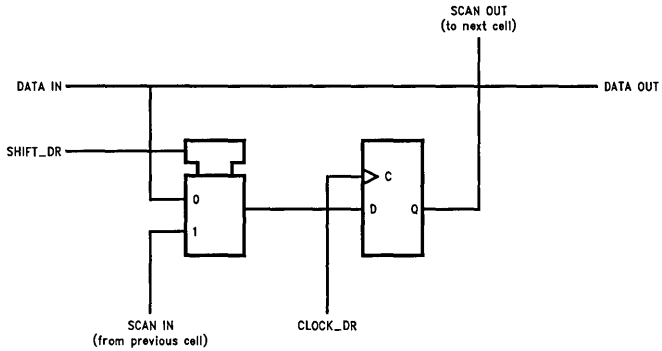
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
All Others	BYPASS

Scan Cell TYPE1



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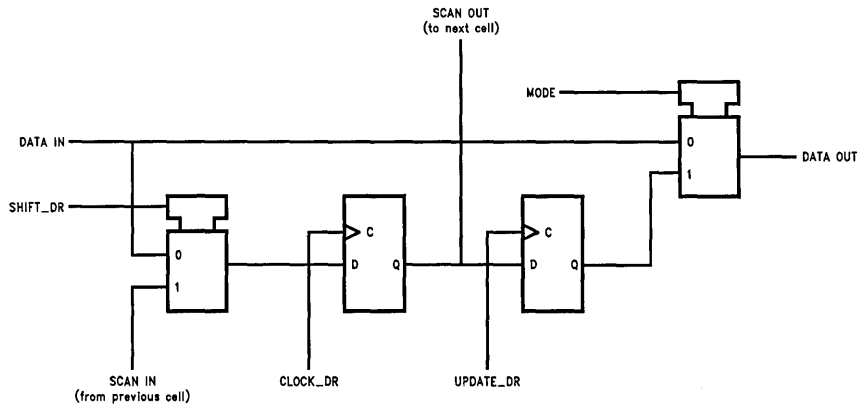
Scan Cell TYPE2



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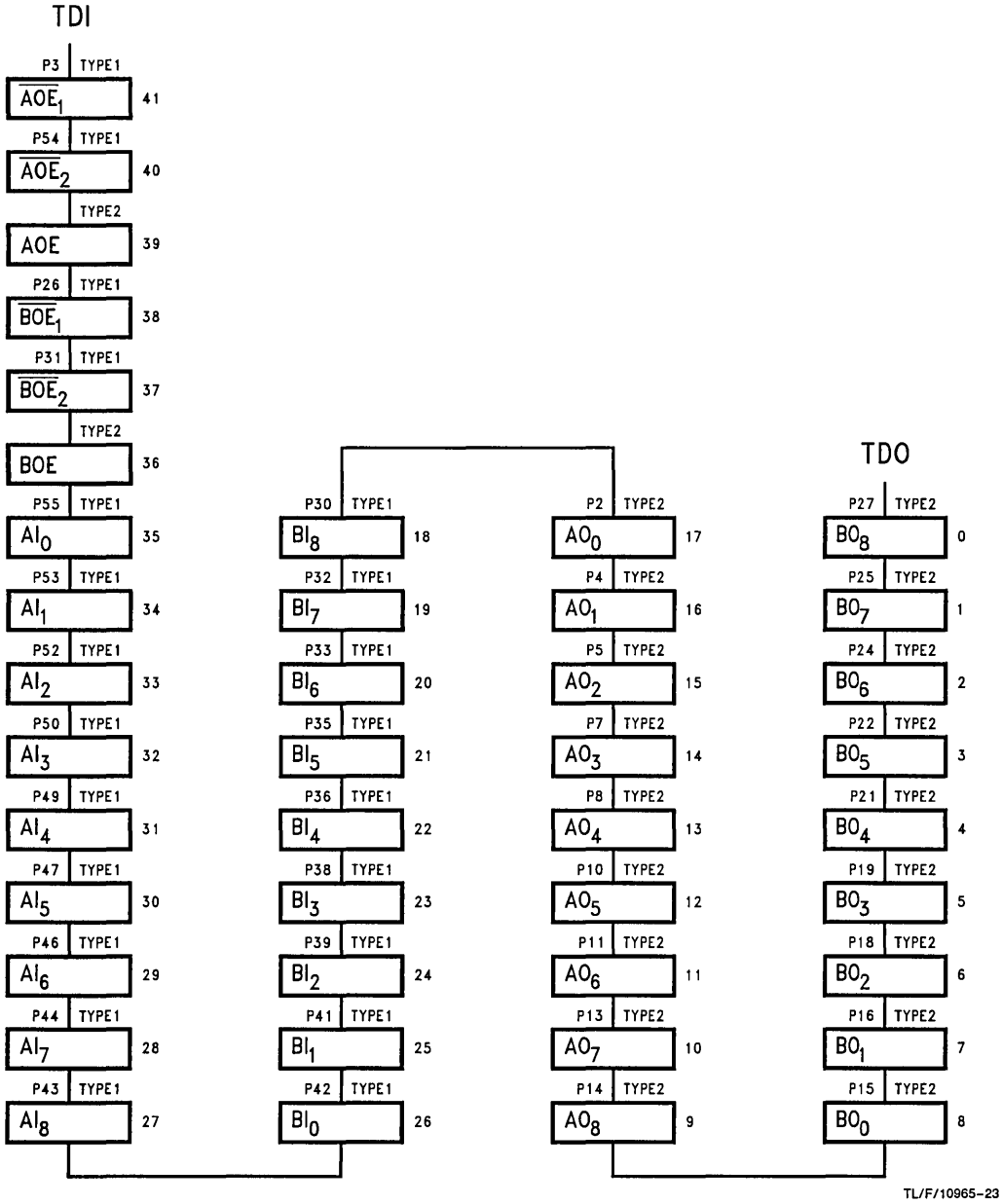
Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register

Scan Chain Definition (42 Bits in Length)



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Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	
40	$\overline{AOE_2}$	54	Input	TYPE1	
39	AOE		Internal	TYPE2	Control
38	$\overline{BOE_1}$	26	Input	TYPE1	Signals
37	$\overline{BOE_2}$	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	A-in
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	B-in
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	A-out
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	B-out
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)	±70 mA
DC V_{CC} or Ground Current Per Output Pin	±70 mA
Junction Temperature SSOP	+140°C
Storage Temperature	−65°C to +150°C
ESD (Min)	2000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of SCAN circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
SCAN Products	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Commercial	−40°C to +85°C
Military	−55°C to +125°C
Minimum Input Edge Rate dV/dt	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial		Military	Commercial	Units	Conditions
			T_A = +25°C		T_A = −55°C to +125°C	T_A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Output Voltage	4.5		3.15	3.15	3.15	V	I_{OUT} = −50 μA
		5.5		4.15	4.15	4.15		
		4.5		2.4		2.4	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −32 mA
		5.5		2.4		2.4		
		4.5		2.4	2.4		V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA
		5.5		2.4	2.4			
V_{OL}	Maximum Low Output Voltage	4.5		0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5		0.1	0.1	0.1		
		4.5		0.55		0.55	V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 64 mA
		5.5		0.55		0.55		
		4.5		0.55	0.55		V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 48 mA
		5.5		0.55	0.55			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5		2.8	3.7	3.6	μA	V_I = V_{CC}
				−385	−385	−385	μA	V_I = GND
	Minimum Input Leakage	5.5		−160	−160	−160	μA	V_I = GND
I_{OLD}	†Minimum Dynamic Output Current	5.5		94	63	94	mA	V_{OLD} = 0.8V Max
I_{OHD}				−40	−27	−40	mA	V_{OHD} = 2.0V Min

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$	Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OZ}	Maximum Output Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH}
I_{OS}	Output Short Circuit Current	5.5		−100	−100	−100	mA (min)	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5		16.0	168	88	μA	V_O = Open TDI, TMS = V_{CC}
		5.5		750	930	820	μA	V_O = Open TDI, TMS = GND
I_{CCt}	Maximum I_{CC} Per Input	5.5		2.0	2.0	2.0	mA	V_I = V_{CC}−2.1V
		5.5		2.15	2.15	2.15	mA	V_I = V_{CC}−2.1V TDI/TMS Pin, Test One with the Other Floating

*All outputs loaded; thresholds associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications: See Section 4

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$	Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Fig. No.
			Typ	Guaranteed Limits			
V_{OLP}	Maximum High Output Noise (Notes 2, 3)	5.0	1.0	1.5			V	4-13
V_{OLV}	Minimum Low Output Noise (Notes 2, 3)	5.0	−0.6	−1.2			V	4-13
V_{OHP}	Maximum Overshoot (Notes 1, 3)	5.0	V_{OH}+1.0	V_{OH}+1.5			V	4-13
V_{OHV}	Minimum V_{CC} Droop (Notes 1, 3)	5.0	V_{OH}−1.0	V_{OH}−1.8			V	4-13
V_{IHD}	Minimum High Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.6	2.0	2.0	2.0	V	
V_{ILD}	Maximum Low Dynamic Input Voltage Level (Notes 1, 4)	5.5	1.4	0.8	0.8	0.8	V	

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay Data to Q	5.0	2.5 2.5		9.0 9.0	2.5 2.5	10.5 10.5	2.5 2.5	9.8 9.8	ns	4-1, 2
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.5 1.5		10.2 10.2	1.5 1.5	11.2 11.2	1.5 1.5	10.7 10.7	ns	4-3, 4
t_{PZL}, t_{PZH}	Enable Time	5.0	2.0 2.0		11.8 9.5	2.0 2.0	13.5 11.5	2.0 2.0	12.8 10.5	ns	4-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$ $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	3.5 3.5		13.2 13.2	3.5 3.5	15.8 15.8	3.5 3.5	14.5 14.5	ns	4-8
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.5 2.5		11.5 11.5	2.5 2.5	12.8 12.8	2.5 2.5	11.9 11.9	ns	4-9, 10
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	3.0 3.0		14.5 14.5	3.0 3.0	16.7 16.7	3.0 3.0	15.8 15.8	ns	4-9, 10
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-DR State	5.0	5.0 5.0		18.0 18.0	5.0 5.0	21.7 21.7	5.0 5.0	19.8 19.8	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0		18.6 18.6	5.0 5.0	21.2 21.2	5.0 5.0	20.2 20.2	ns	4-8
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.5 5.5		19.9 19.9	5.5 5.5	23.0 23.0	5.5 5.5	21.5 21.5	ns	4-8
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0		16.4 16.4	4.0 4.0	19.6 19.6	4.0 4.0	18.2 18.2	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0		19.5 19.5	5.0 5.0	22.4 22.4	5.0 5.0	20.8 20.8	ns	4-9, 10
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.0 5.0		19.9 19.9	5.0 5.0	23.3 23.3	5.0 5.0	21.5 21.5	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	5.0 5.0		18.9 18.9	5.0 5.0	22.6 22.6	5.0 5.0	20.9 20.9	ns	4-9, 10

*Voltage Range 5.0 is 5.0V ±0.5V.

All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Electrical Characteristics Scan Test Operation: See Section 4 (Continued)

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	6.5 6.5		22.4 22.4	6.5 6.5	26.2 26.2	6.5 6.5	24.2 24.2	ns	4-9, 10
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	7.0 7.0		23.8 23.8	7.0 7.0	27.4 27.4	7.0 7.0	25.7 25.7	ns	4-9, 10

*Voltage Range 5.0 is 5.0V ±0.5V.

All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum				
t_S	Setup Time, H or L Data to TCK (Note 1)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to Data (Note 1)	5.0	4.5	5.0	4.5	ns	4-11
t_S	Setup Time, H or L $\overline{AOE}_n$, $\overline{BOE}_n$ to TCK (Note 3)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{AOE}_n$, $\overline{BOE}_n$ (Note 3)	5.0	4.5	4.5	4.5	ns	4-11
t_S	Setup Time, H or L Internal AOE, BOE, to TCK (Note 2)	5.0	3.0	3.0	3.0	ns	4-11
t_H	Hold Time, H or L TCK to Internal AOE, BOE (Note 2)	5.0	3.0	3.0	3.0	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0	8.0	8.0	8.0	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	2.0	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0	4.0	4.0	4.0	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0	4.5	4.5	4.5	ns	4-11
t_W	Pulse Width TCK H L	5.0	15.0 5.0	15.0 5.0	15.0 5.0	ns	4-12

AC Operating Requirements Scan Test Operation: See Section 4 (Continued)

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Guaranteed Minimum			
f_{max}	Maximum TCK Clock Frequency	5.0	25	25	25	MHz
T_{PU}	Wait Time, Power Up to TCK	5.0	100	100	100	ns
T_{DN}	Power Down Delay	0.0	100	100	100	ms

*Voltage Range 5.0 is 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26 and 27-35.

Note 2: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

Note 3: Timing pertains to BSR 37, 38, 40 and 41 only.

Extended AC Electrical Characteristics

Symbol	Parameter	$T_A = Com$, $V_{CC} = Com$, $C_L = 50$ pF, 18 Outputs Switching (Note 2)			$T_A = Mil$, $V_{CC} = Mil$, $C_L = 50$ pF, 18 Outputs Switching (Note 2)		$T_A = Com$, $V_{CC} = Com$, $C_L = 250$ pF (Note 3)		$T_A = Mil$, $V_{CC} = Mil$, $C_L = 250$ pF (Note 3)		Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	3.0 3.0		11.0 11.0	3.0 3.0	11.5 11.5	4.0 4.0	13.0 15.0	4.0 4.0	14.0 16.0	ns
t_{PZH}, t_{PZL}	Output Enable Time	2.5 2.5		11.5 14.0	2.5 2.5	12.5 14.5	(Note 4)		(Note 4)		ns
t_{PHZ}, t_{PLZ}	Output Disable Time	2.0 2.0		11.5 11.5	2.0 2.0	12.0 12.0	(Note 5)		(Note 5)		ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		0.5	1.0				1.0			ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output		0.5	1.0				1.0			ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW.

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	13.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	34.0	pF	$V_{CC} = 5.0V$

Section 9

SCAN ABT Test Access Logic Datasheets

Section 9 Contents

National Semiconductor

SCAN182245A
Non-Inverting Transceiver with 25Ω Series Resistor Outputs

General Description

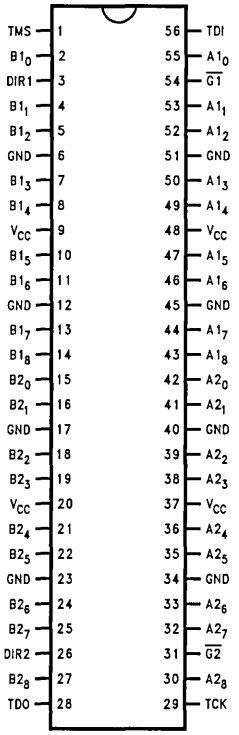
The SCAN182245A is a high performance BiCMOS bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- High performance BiCMOS technology
- 25Ω series resistors in outputs eliminate the need for external terminating resistors
- Dual output enable control signals
- TRI-STATE® outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- IEEE 1149.1 (JTAG) Compliant
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT
- Power Up TRI-STATE for hot insert
- Member of National's SCAN Products

Ordering Code: See Section 11

Connection Diagram



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Pin Names	Description
$A1_{(0-8)}$	Side A1 Inputs or TRI-STATE Outputs
$B1_{(0-8)}$	Side B1 Inputs or TRI-STATE Outputs
$A2_{(0-8)}$	Side A2 Inputs or TRI-STATE Outputs
$B2_{(0-8)}$	Side B2 Inputs or TRI-STATE Outputs
$\overline{G1}$, $\overline{G2}$	Output Enable Pins (Active Low)
DIR1, DIR2	Direction of Data Flow Pins

Order Number	Description
SCAN182245ASSC	SSOP in Tubes
SCAN182245ASSCX	SSOP Tape and Reel
SCAN182245AFMQB	Flatpak Military

Truth Tables

Inputs		$A1_{(0-8)}$		$B1_{(0-8)}$
†$\overline{G1}$	DIR1			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

Inputs		$A2_{(0-8)}$		$B2_{(0-8)}$
†$\overline{G2}$	DIR2			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

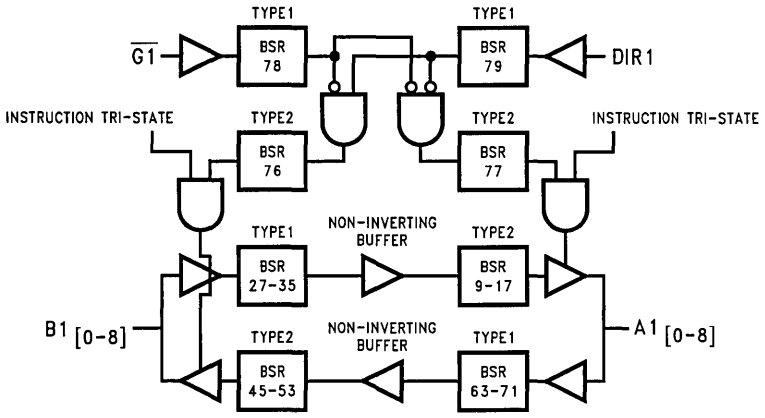
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
† = Inactive-to-Active transition must occur to enable outputs upon power-up.

Functional Description

The SCAN182245A consists of two sets of nine non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Direction pins (DIR1 and DIR2) LOW enables data from B ports to A ports, when HIGH enables data from A ports to B ports. The Output Enable pins ($\overline{G1}$ and $\overline{G2}$) when HIGH disables both A and B ports by placing them in a high impedance condition.

Block Diagrams

A1, B1, $\overline{G1}$ and DIR1



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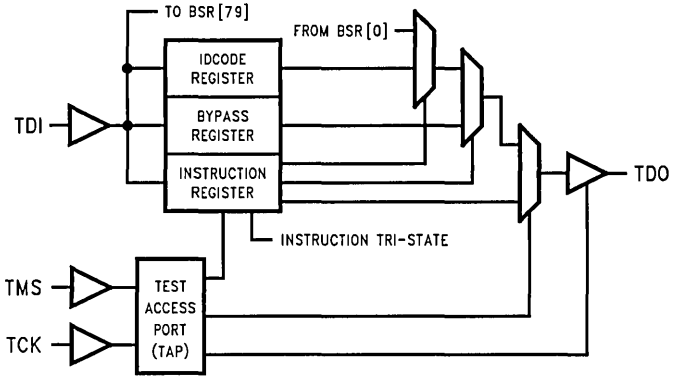
Note: BSR stands for Boundary Scan Register.

Block Diagrams (Continued)

Tap Controller



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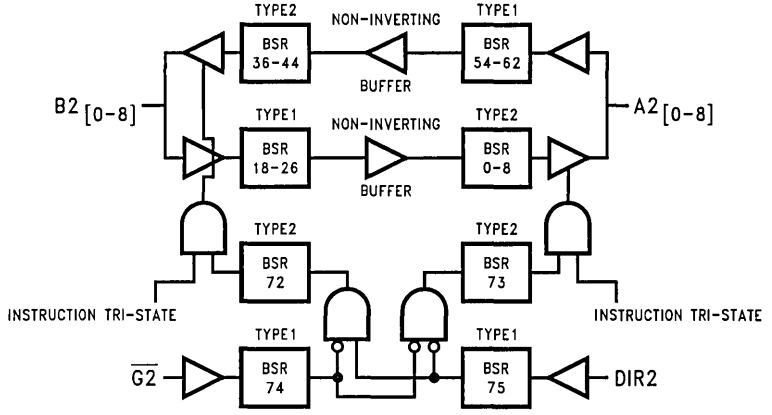
A2, B2, $\overline{G2}$ and DIR2



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Note: BSR stands for Boundary Scan Register.

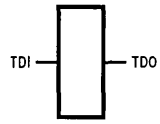
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10-11* for a further description of scan cell TYPE1 and *Figure 10-12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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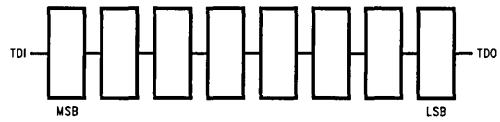
SCAN182245A Product IDCODE
(32-Bit Code per IEEE 1149.1)

Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
0000	111111	0000000000	00000001111	1

MSB **LSB**

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

Instruction Register Scan Chain Definition



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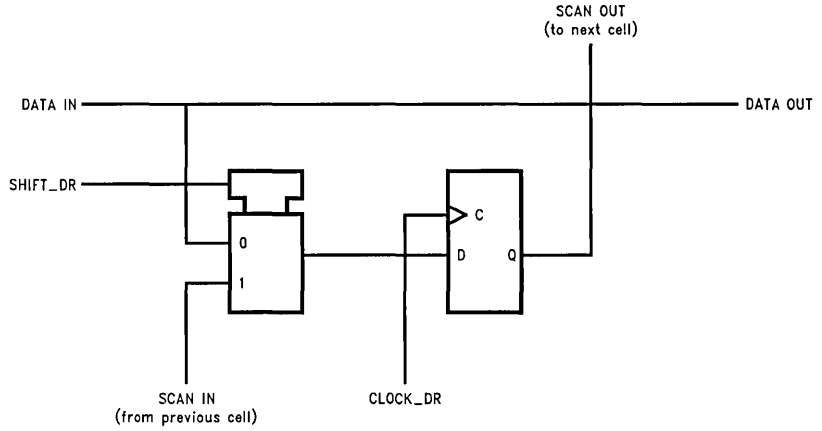
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

Description of BOUNDARY-SCAN Circuitry (Continued)

Scan Cell TYPE1



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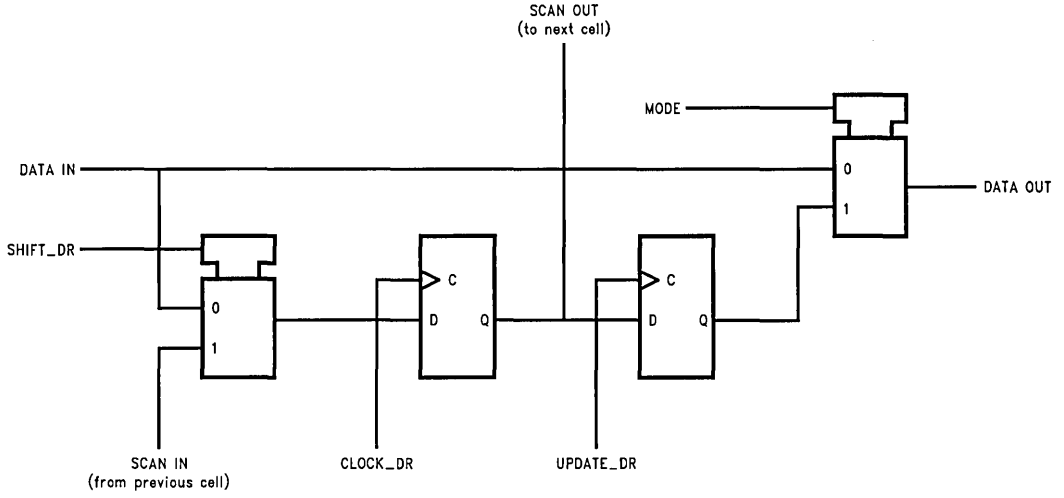
Scan Cell TYPE2



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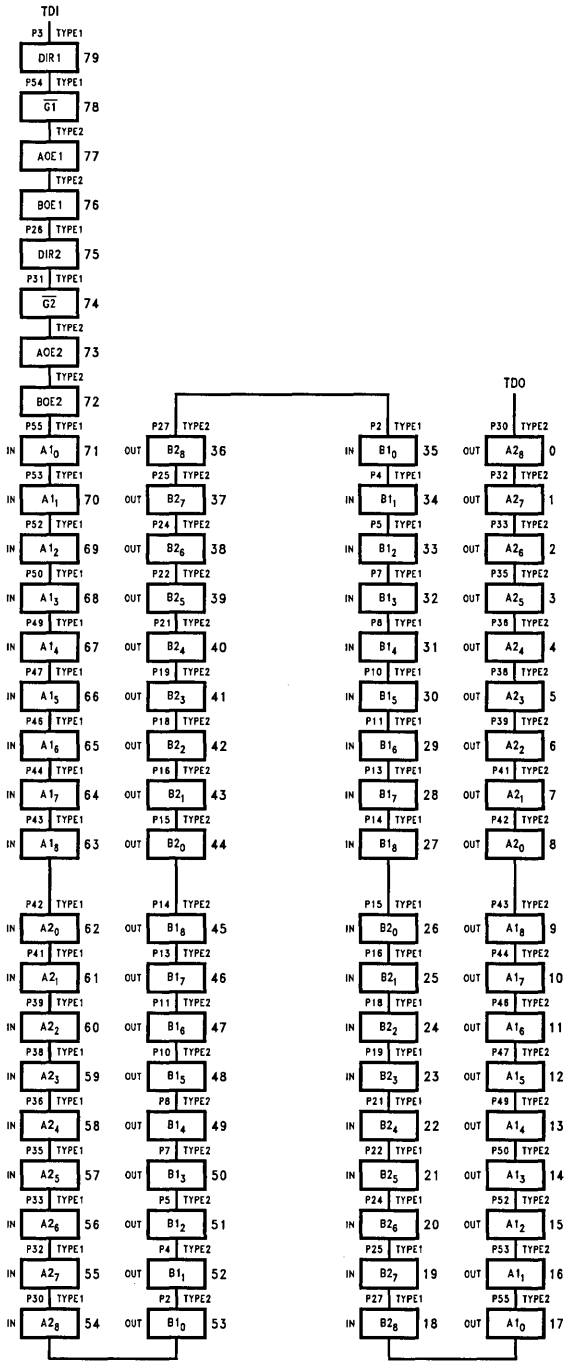
Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register

Scan Chain Definition (80 Bits In Length)



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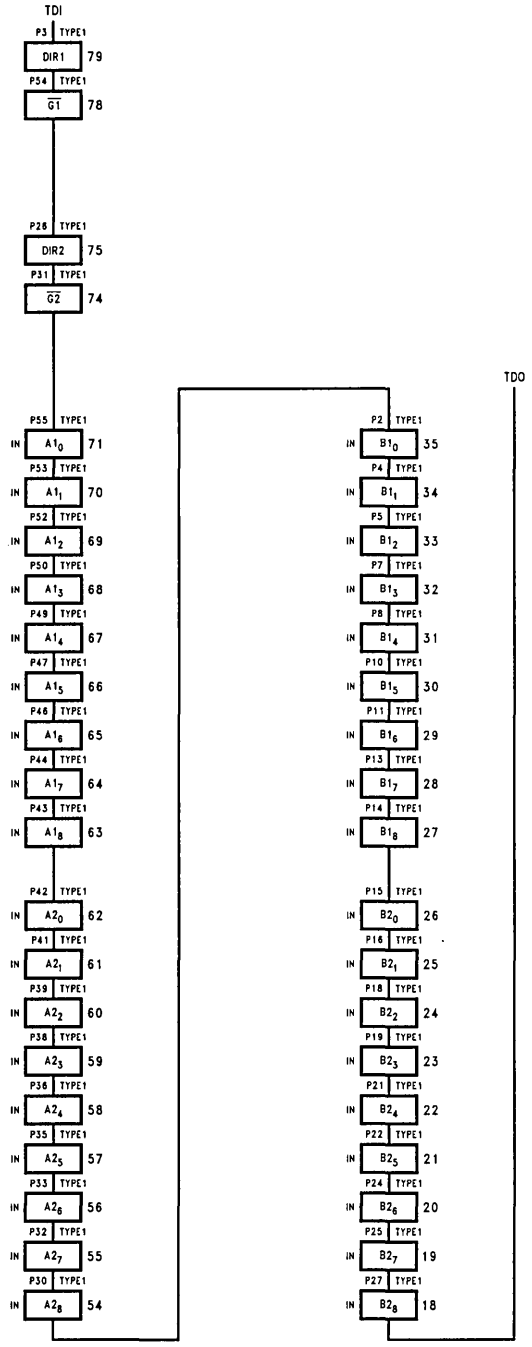
Description of BOUNDARY-SCAN Circuitry (Continued)

Input BOUNDARY-SCAN Register

Scan Chain Definition (40 Bits In Length)
When Sample In is Active



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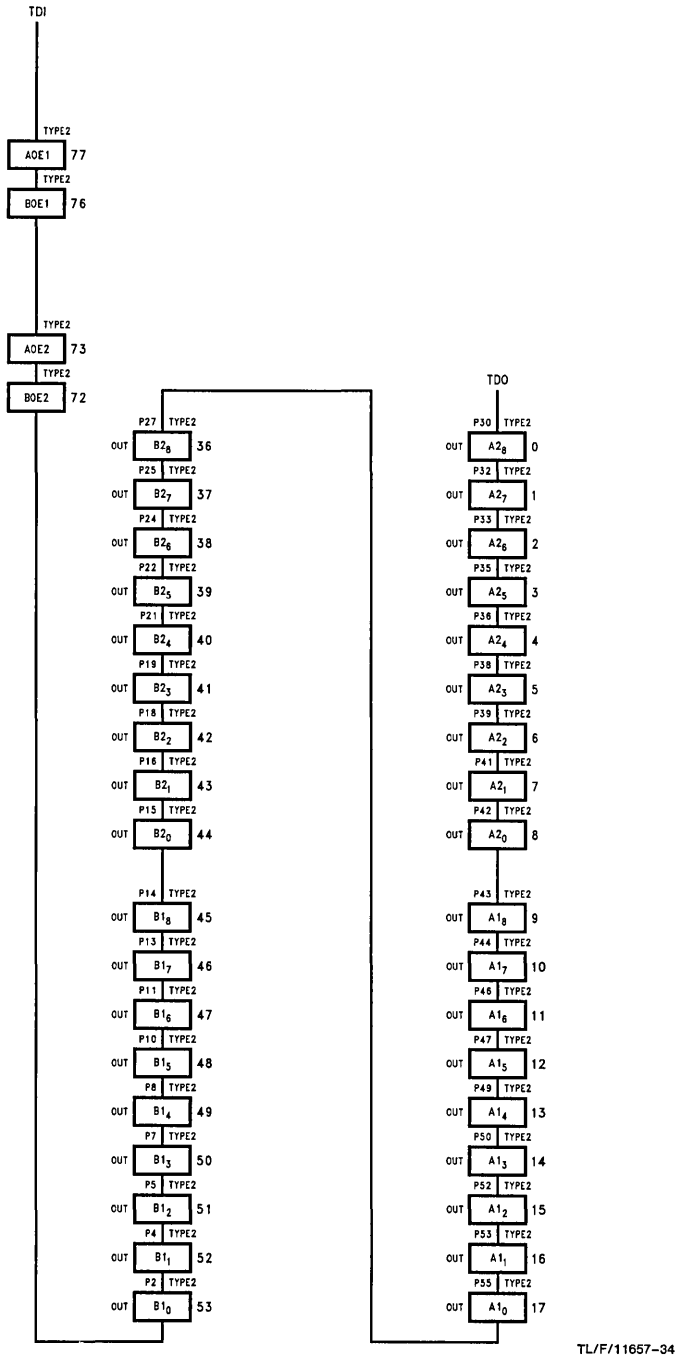
Description of BOUNDARY-SCAN Circuitry (Continued)

Output BOUNDARY-SCAN Register

Scan Chain Definition (40 Bits in Length)
When Sample Out and EXTEST-Out are Active



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Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
79	DIR1	3	Input	TYPE1	
78	$\overline{G1}$	54	Input	TYPE1	
77	AOE_1		Internal	TYPE2	
76	BOE_1		Internal	TYPE2	Control
75	DIR2	26	Input	TYPE1	Signals
74	$\overline{G2}$	31	Input	TYPE1	
73	AOE_2		Internal	TYPE2	
72	BOE_2		Internal	TYPE2	
71	$A1_0$	55	Input	TYPE1	
70	$A1_1$	53	Input	TYPE1	
69	$A1_2$	52	Input	TYPE1	
68	$A1_3$	50	Input	TYPE1	
67	$A1_4$	49	Input	TYPE1	A1–in
66	$A1_5$	47	Input	TYPE1	
65	$A1_6$	46	Input	TYPE1	
64	$A1_7$	44	Input	TYPE1	
63	$A1_8$	43	Input	TYPE1	
62	$A2_0$	42	Input	TYPE1	
61	$A2_1$	41	Input	TYPE1	
60	$A2_2$	39	Input	TYPE1	
59	$A2_3$	38	Input	TYPE1	
58	$A2_4$	36	Input	TYPE1	A2–in
57	$A2_5$	35	Input	TYPE1	
56	$A2_6$	33	Input	TYPE1	
55	$A2_7$	32	Input	TYPE1	
54	$A2_8$	30	Input	TYPE1	
53	$B1_0$	2	Output	TYPE2	
52	$B1_1$	4	Output	TYPE2	
51	$B1_2$	5	Output	TYPE2	
50	$B1_3$	7	Output	TYPE2	
49	$B1_4$	8	Output	TYPE2	B1–out
48	$B1_5$	10	Output	TYPE2	
47	$B1_6$	11	Output	TYPE2	
46	$B1_7$	13	Output	TYPE2	
45	$B1_8$	14	Output	TYPE2	
44	$B2_0$	15	Output	TYPE2	
43	$B2_1$	16	Output	TYPE2	
42	$B2_2$	18	Output	TYPE2	
41	$B2_3$	19	Output	TYPE2	
40	$B2_4$	21	Output	TYPE2	B2–out
39	$B2_5$	22	Output	TYPE2	
38	$B2_6$	24	Output	TYPE2	
37	$B2_7$	25	Output	TYPE2	
36	$B2_8$	27	Output	TYPE2	
35	$B1_0$	2	Input	TYPE1	
34	$B1_1$	4	Input	TYPE1	
33	$B1_2$	5	Input	TYPE1	
32	$B1_3$	7	Input	TYPE1	
31	$B1_4$	8	Input	TYPE1	B1–in
30	$B1_5$	10	Input	TYPE1	
29	$B1_6$	11	Input	TYPE1	
28	$B1_7$	13	Input	TYPE1	
27	$B1_8$	14	Input	TYPE1	

Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index (Continued)

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
26	$B2_0$	15	Input	TYPE1	
25	$B2_1$	16	Input	TYPE1	
24	$B2_2$	18	Input	TYPE1	
23	$B2_3$	19	Input	TYPE1	
22	$B2_4$	21	Input	TYPE1	B2–in
21	$B2_5$	22	Input	TYPE1	
20	$B2_6$	24	Input	TYPE1	
19	$B2_7$	25	Input	TYPE1	
18	$B2_8$	27	Input	TYPE1	
17	$A1_0$	55	Output	TYPE2	
16	$A1_1$	53	Output	TYPE2	
15	$A1_2$	52	Output	TYPE2	
14	$A1_3$	50	Output	TYPE2	
13	$A1_4$	49	Output	TYPE2	A1–out
12	$A1_5$	47	Output	TYPE2	
11	$A1_6$	46	Output	TYPE2	
10	$A1_7$	44	Output	TYPE2	
9	$A1_8$	43	Output	TYPE2	
8	$A2_0$	42	Output	TYPE2	
7	$A2_1$	41	Output	TYPE2	
6	$A2_2$	39	Output	TYPE2	
5	$A2_3$	38	Output	TYPE2	
4	$A2_4$	36	Output	TYPE2	A2–out
3	$A2_5$	35	Output	TYPE2	
2	$A2_6$	33	Output	TYPE2	
1	$A2_7$	32	Output	TYPE2	
0	$A2_8$	30	Output	TYPE2	

SCAN ABT Live Insertion and Power Cycling Characteristics

SCAN ABT is intended to serve in Live Insertion backplane applications. It provides 2nd Level Isolation[1] which indicates that while external circuitry to control the output enable pin is unnecessary, there may be a need to implement differential length backplane connector pins for V_{CC} and GND. As well, pre-bias circuitry for backplane pins may be necessary to avoid capacitive loading effects during live insertion.

SCAN ABT provides control of output enable pins during power cycling via the circuit in *Figure A*. It essentially controls the $\overline{G_n}$ pin until V_{CC} reaches a known level.

During *power-up*, when V_{CC} ramps through the 0.0V to 0.7V range, all internal device circuitry is inactive, leaving output and I/O pins of the device in high impedance. From approximately 0.8V to 1.8V V_{CC}, the Power-On-Reset circuitry, (POR), in *Figure A* becomes active and maintains device high impedance mode. The POR does this by providing a low from its output that resets the flip-flop The output, $\overline{Q}$, of the flip-flop then goes high and disables the NOR gate from an incidental low input on the $\overline{G_n}$ pin. After 1.8V V_{CC}, the POR circuitry becomes inactive and ceases to control the flip-flop. To bring the device out of high impedance, the $\overline{G_n}$ input must receive an inactive-to-active transition, a high-to-low transition on $\overline{G_n}$ in this case to change the state of the flip-flop. With a low on the $\overline{Q}$ output of the flip-flop, the NOR gate is free to allow propagation of a $\overline{G_n}$ signal.

During *power-down*, the Power-On-Reset circuitry will become active and reset the flip-flop at approximately 1.8V V_{CC}. Again, the $\overline{Q}$ output of the flip-flop returns to a high and disables the NOR gate from inputs from the $\overline{G_n}$ pin. The device will then remain in high impedance for the remaining ramp down from 1.8V to 0.0V V_{CC}.

Some suggestions to help the designer with live insertion issues:

- The $\overline{G_n}$ pin can float during power-up until the Power-On-Reset circuitry becomes inactive.
- The $\overline{G_n}$ pin can float on power-down only after the Power-On-Reset has become active.

The description of the functionality of the Power-On-Reset circuitry can best be described in the diagram of *Figure B*.

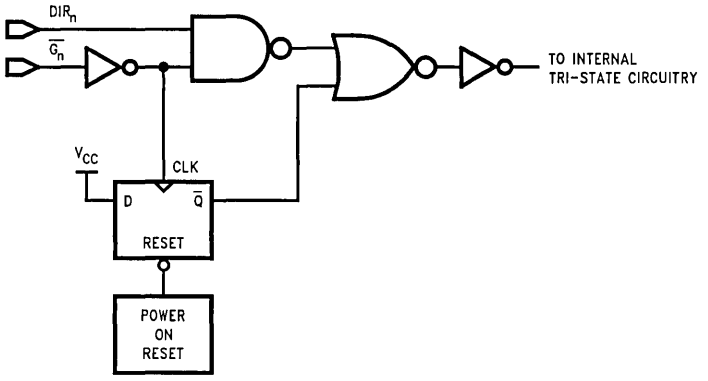

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FIGURE A

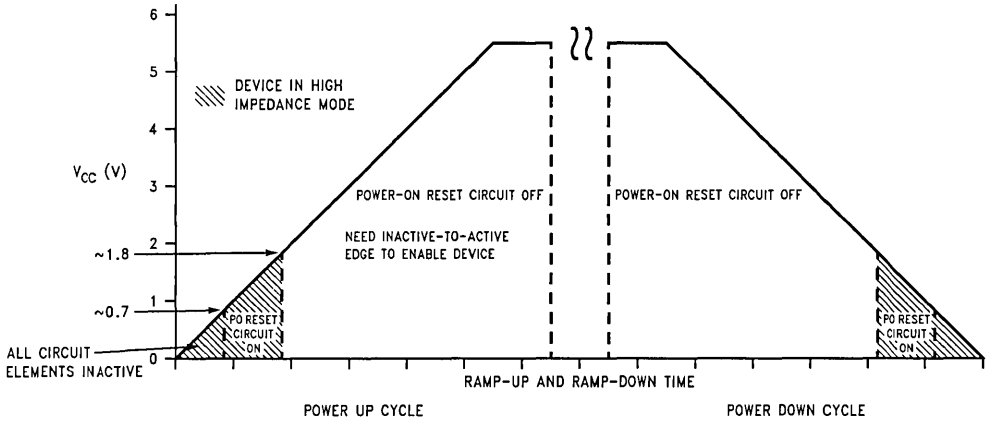

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FIGURE B

[1]Section 7, "Design Consideration for Fault Tolerant Backplanes", Application Note AN-881.

SCAN ABT includes additional power-on reset circuitry not otherwise included in ABT devices.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
DC Latchup Source Current	
Commercial	−500 mA
Military	−300 mA
Over Voltage Latchup (I/O)	10V
ESD (HBM) Min.	2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH Voltage			2.0			V	Recognized HIGH Signal
V_{IL}	Input LOW Voltage					0.8	V	Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage		Min			−1.2	V	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		Min	2.5			V	I_{OH} = −3 mA
		Mil	Min	2.0			V	I_{OH} = −24 mA
		Comm	Min	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage							
		Mil	Min			0.8	V	I_{OL} = 12 mA
		Comm	Min			0.8	V	I_{OL} = 15 mA
I_{IH}	Input HIGH Current	All Others	Max			5	μA	V_{IN} = 2.7V (Note 1)
			Max			5	μA	V_{IN} = V_{CC}
		TMS, TDI	Max			5	μA	V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test		Max			7	μA	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)		Max			100	μA	V_{IN} = 5.5V
I_{IL}	Input LOW Current	All Others	Max			−5	μA	V_{IN} = 0.5V (Note 1)
			Max			−5	μA	V_{IN} = 0.0V
		TMS, TDI	Max			−385	μA	V_{IN} = 0.0V
V_{ID}	Input Leakage Test		0.0	4.75			V	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
I_{IL} + I_{OZL}	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V
I_{OZH}	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V

Note 1: Guaranteed not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units	Conditions
I_{OS}	Output Short-Circuit Current	Max	−100		−275	mA	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current	Max			50	μA	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test	0.0			100	μA	V_{OUT} = 5.5V All Others GND
I_{CCH}	Power Supply Current	Max			250	μA	V_{OUT} = V_{CC}; TDI, TMS = V_{CC}
		Max			1.0	mA	V_{OUT} = V_{CC}; TDI, TMS = GND
I_{CCL}	Power Supply Current	Max			65	mA	V_{OUT} = LOW; TDI, TMS = V_{CC}
		Max			65.8	mA	V_{OUT} = LOW; TDI, TMS = GND
I_{CCZ}	Power Supply Current	Max			250	μA	TDI, TMS = V_{CC}
		Max			1.0	mA	TDI, TMS = GND
I_{CCT}	Additional I_{CC}/Input All Other Inputs	Max			2.9	mA	V_{IN} = V_{CC} − 2.1V
	TDI, TMS inputs	Max			3	mA	V_{IN} = V_{CC} − 2.1V
I_{CCD}	Dynamic I_{CC} No Load	Max			0.2	mA/ MHz	Outputs Open One Bit Toggling, 50% Duty Cycle

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military T_A = −55°C to +125°C C_L = 50 pF			Commercial T_A = −40°C to +85°C C_L = 50 pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	5.0				1.0 1.5	3.1 4.4	5.2 6.5	ns	4-1, 2
t_{PLZ} t_{PHZ}	Disable Time	5.0				1.5 1.5	4.8 5.2	8.6 8.9	ns	4-3, 4
t_{PZL} t_{PZH}	Enable Time	5.0				1.5 1.5	5.5 4.6	9.1 8.2	ns	4-3, 4

*Voltage Range 5.0V ±0.5V

AC Electrical Characteristics Scan Test Operation

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF			Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay TCK to TDO	5.0				2.9 4.2	6.1 7.7	10.2 12.1	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to TDO	5.0				2.1 3.3	5.9 7.4	10.7 12.5	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to TDO	5.0				4.6 2.8	8.7 6.8	13.7 11.5	ns	4-9, 10
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0				2.8 4.5	6.3 8.2	10.7 13.0	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0				3.3 5.0	7.2 9.3	12.2 14.8	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0				3.7 5.7	8.4 10.8	14.0 17.2	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-DR State	5.0				2.8 3.5	7.6 8.4	13.9 14.5	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-IR State	5.0				3.6 3.8	8.7 9.2	15.1 15.9	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Test Logic Reset State	5.0				4.0 4.2	9.8 9.9	17.1 16.6	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-DR State	5.0				4.4 3.0	9.3 7.5	15.5 13.3	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-IR State	5.0				5.2 3.9	10.7 9.0	17.4 15.4	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Test Logic Reset State	5.0				5.7 3.0	12.0 10.2	19.8 17.6	ns	4-9, 10

*Voltage Range 5.0V ±0.5V

All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements Scan Test Operation

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time Data to TCK (Note 1)	5.0		4.8	ns	4-11
t_H	Hold Time Data to TCK (Note 1)	5.0		2.5	ns	4-11
t_S	Setup Time, H or L $\overline{G1}$, $\overline{G2}$ to TCK (Note 2)	5.0		4.1	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{G1}$, $\overline{G2}$ (Note 2)	5.0		1.7	ns	4-11
t_S	Setup Time, H or L DIR1, DIR2 to TCK (Note 4)	5.0		4.2	ns	4-11
t_H	Hold Time, H or L TCK to DIR1, DIR2 (Note 4)	5.0		2.3	ns	4-11
t_S	Setup Time Internal OE to TCK (Note 3)	5.0		3.8	ns	4-11
t_H	Hold Time, H or L TCK to Internal OE (Note 3)	5.0		2.3	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0		8.7	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0		1.5	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0		6.7	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0		5.0	ns	4-11
t_W	Pulse Width TCK H L	5.0		10.2 8.5	ns	4-12
f_{max}	Maximum TCK Clock Frequency	5.0		50	MHz	
t_{PU}	Wait Time, Power Up to TCK	5.0		100	ns	
t_{DN}	Power Down Delay	0.0		100	ms	

*Voltage Range 5.0V ±0.5V

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: Timing pertains to the TYPE1 BSR and TYPE2 BSR after the buffer (BSR 0-8, 9-17, 18-26, 27-35, 36-44, 45-53, 54-62, 63-71).

Note 2: Timing pertains to BSR 74 and 78 only.

Note 3: Timing pertains to BSR 72, 73, 76 and 77 only.

Note 4: Timing pertains to BSR 75 and 79 only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.9	pF	$V_{CC} = 0.0V$ ($\overline{G}_n$, DIR_n)
$C_{I/O}$ (Note 1)	Output Capacitance	13.7	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

SCAN182373A
Transparent Latch with 25Ω Series Resistor Outputs

General Description

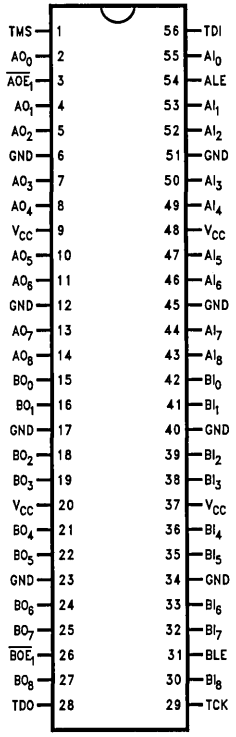
The SCAN182373A is a high performance BiCMOS transparent latch featuring separate data inputs organized into dual 9-bit bytes with byte-oriented latch enable and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- High performance BiCMOS technology
- 25Ω series resistor outputs eliminate need for external terminating resistors
- Buffered active-low latch enable
- TRI-STATE® outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT
- Power up TRI-STATE for hot insert
- Member of National's SCAN Products

Ordering Code: See Section 11

Connection Diagram



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Pin Names	Description
$AI_{(0-8)}$, $BI_{(0-8)}$	Data Inputs
ALE, BLE	Latch Enable Inputs
$\overline{AOE}_1$, $\overline{BOE}_1$	TRI-STATE Output Enable Inputs
$AO_{(0-8)}$, $BO_{(0-8)}$	TRI-STATE Latch Outputs

Order Number	Description
SCAN182373ASSC	SSOP in Tubes
SCAN182373ASSCX	SSOP in Tape and Reel
SCAN182373AFMQB	Military Flatpak

Truth Table

Inputs			AO (0–8)
ALE	†$\overline{AOE_1}$	AI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	AO_0

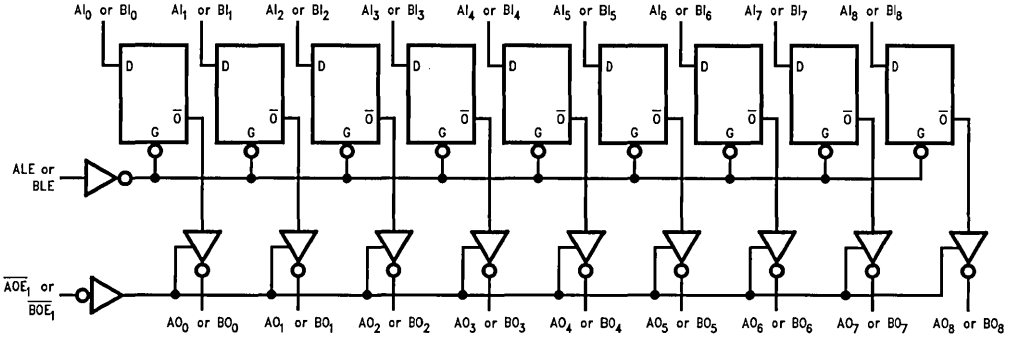
Inputs			BO (0–8)
BLE	†$\overline{BOE_1}$	BI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	BO_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
AO_0 = Previous AO before H-to-L transition of ALE
BO_0 = Previous BO before H-to-L transition of BLE
† = Inactive-to-active transition must occur to enable outputs upon power-up.

Functional Description

The SCAN182373A consists of two sets of nine D-type latches with TRI-STATE standard outputs. When the Latch Enable (ALE or BLE) input is HIGH, data on the inputs ($AI_{(0-8)}$ or $BI_{(0-8)}$) enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its input changes. When Latch Enable is LOW, the latches store the information that was present on the inputs a set-up time preceding the HIGH-to-LOW transition of the Latch Enable. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{AOE_1}$ or $\overline{BOE_1}$) input. When Output Enable is LOW, the standard outputs are in the 2-state mode. When Output Enable is HIGH, the standard outputs are in the high impedance mode, but this does not interfere with entering new data into the latches.

Logic Diagram



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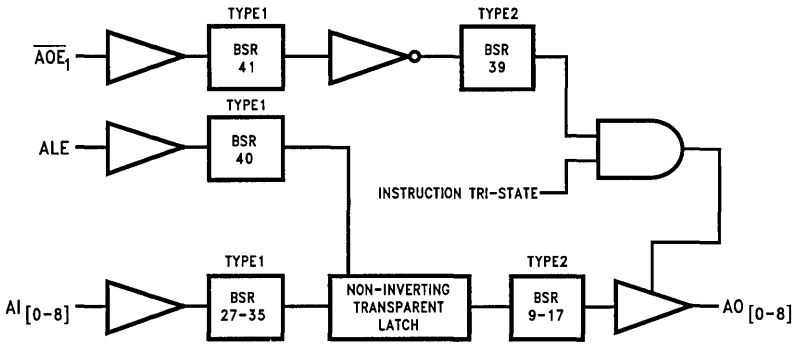
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Block Diagrams

Byte-A



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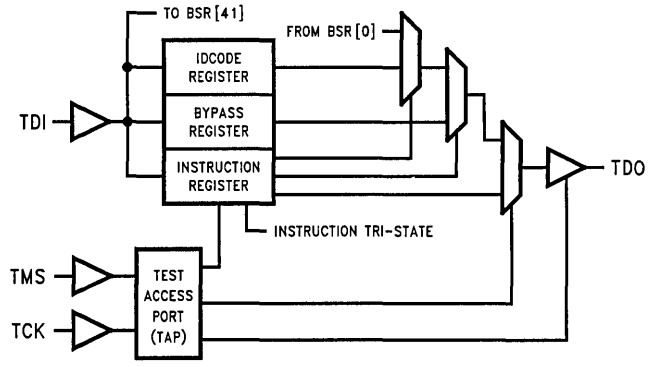
Tap Controller



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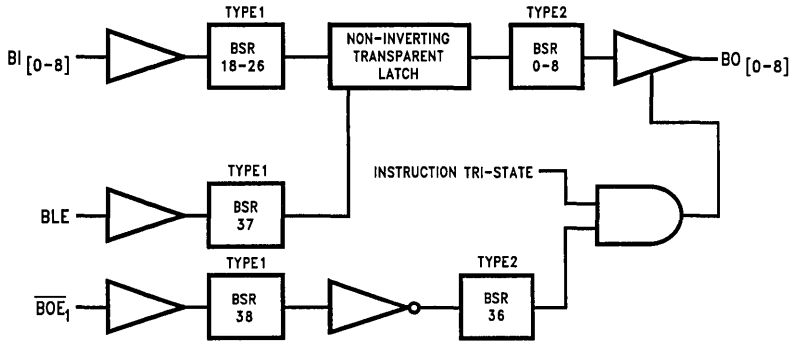
Byte-B



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Note: BSR stands for Boundary Scan Register.

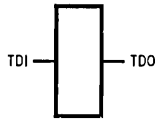
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10-11* for a further description of scan cell TYPE 1 and *Figure 10-12* for a further description of scan cell TYPE 2.)

Scan cell TYPE 1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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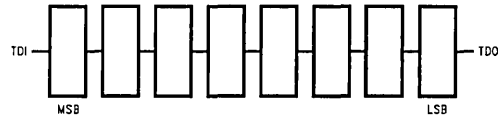
SCAN182373A Product IDCODE
(32-Bit Code per IEEE 1149.1)

Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
0000	111111	0000001000	00000001111	1

MSB **LSB**

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

Instruction Register Scan Chain Definition



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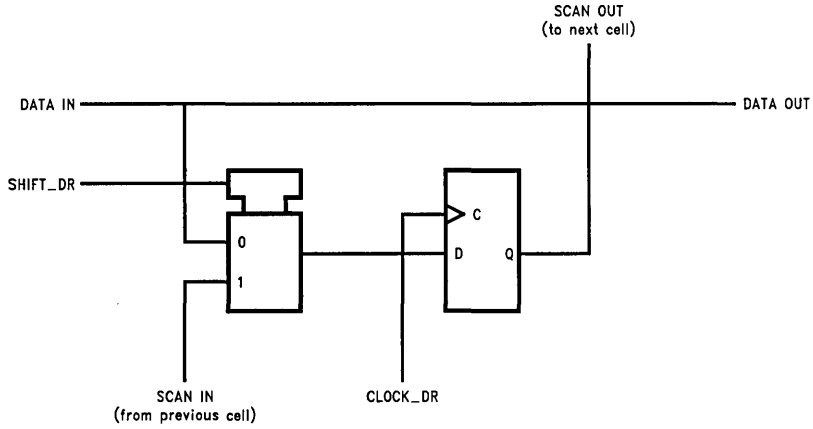
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

Description of BOUNDARY-SCAN Circuitry (Continued)

Scan Cell TYPE1



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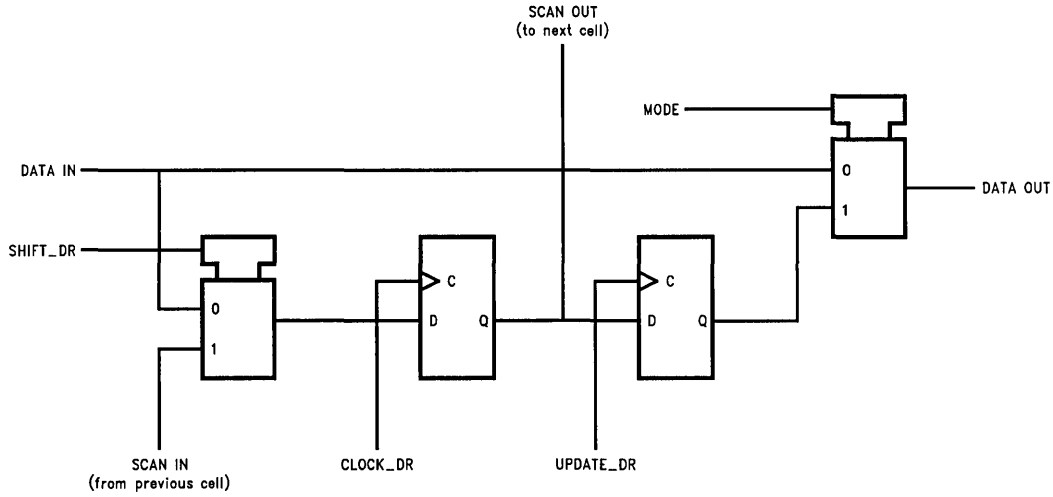
Scan Cell TYPE2



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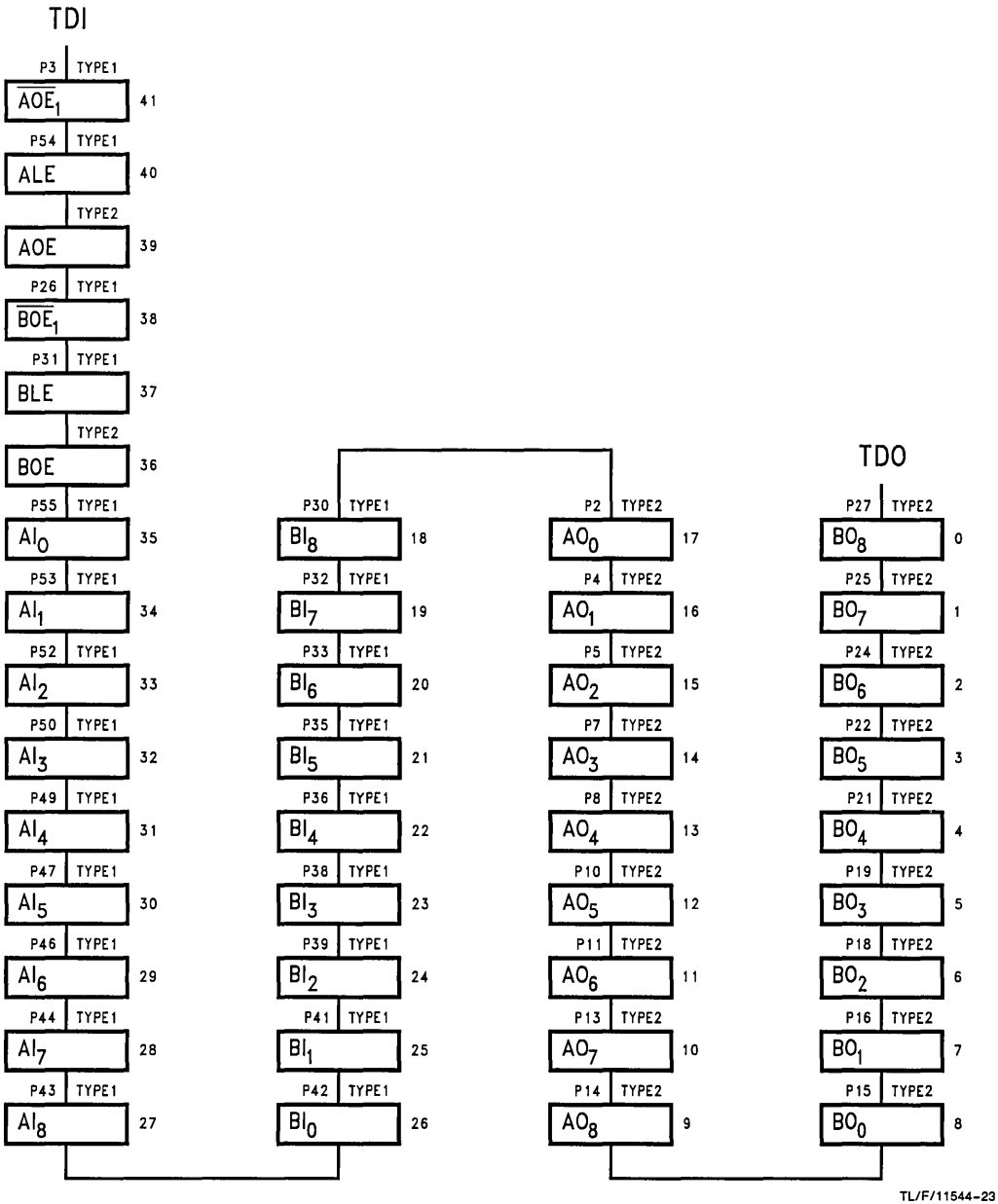
Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register

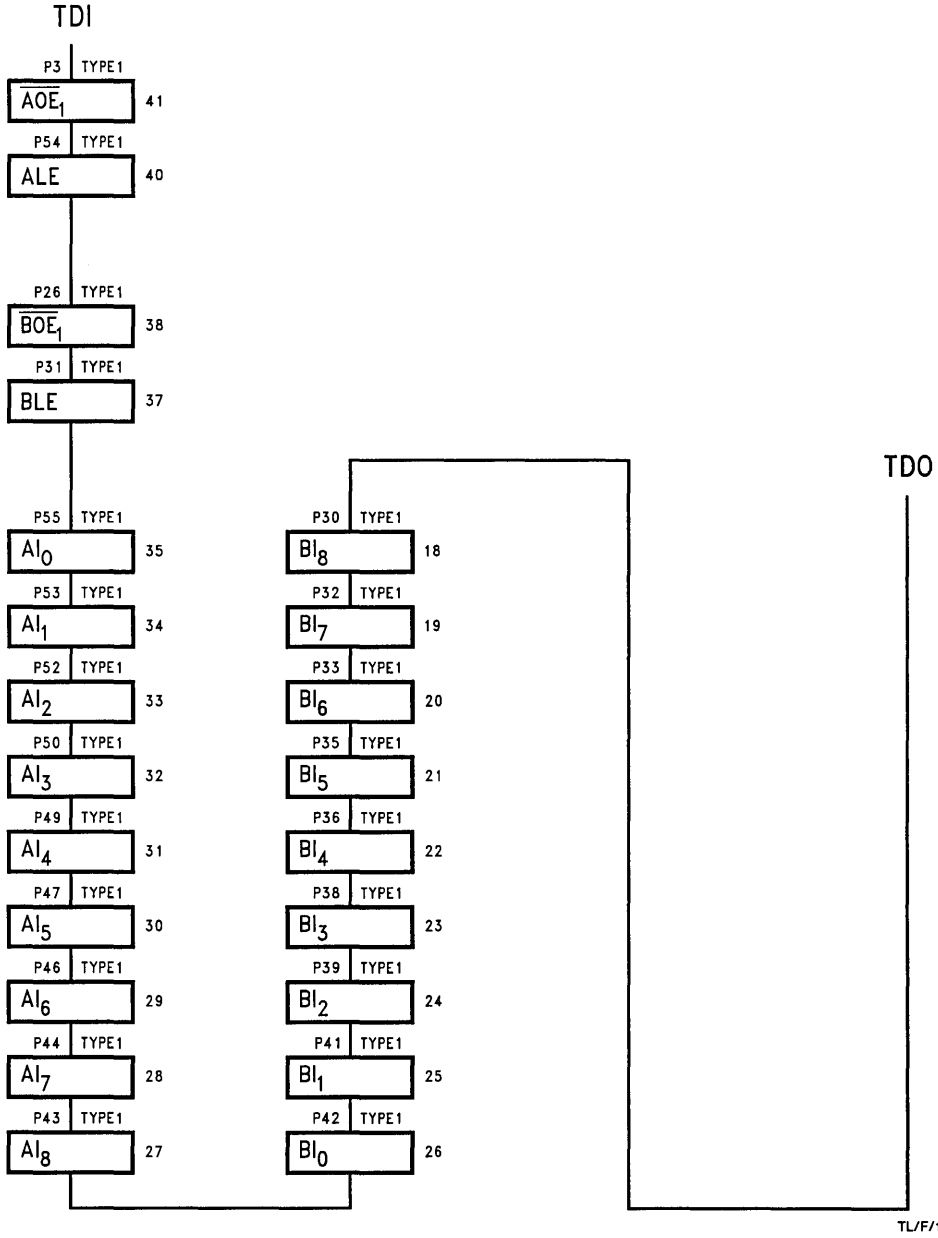
Scan Chain Definition (42 Bits in Length)



TL/F/11544–23

Description of BOUNDARY-SCAN Circuitry (Continued)

Input BOUNDARY-SCAN Register
Scan Chain Definition (22 Bits In Length)
When Sample In Is Active

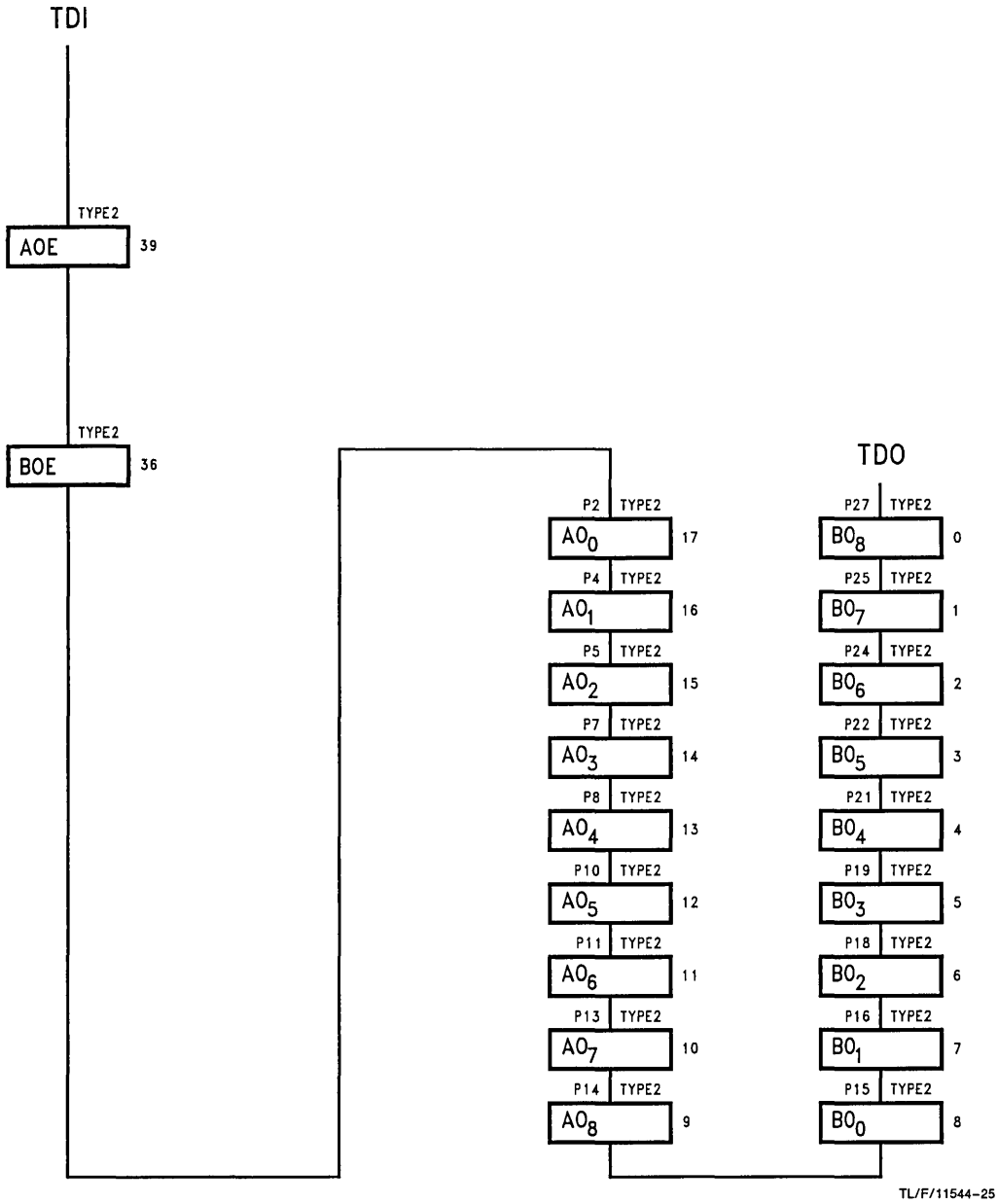


TL/F/11544–24

Description of BOUNDARY-SCAN Circuitry (Continued)

Output BOUNDARY-SCAN Register

Scan Chain Definition (20 Bits in Length)
When Sample Out and Extest Out are Active



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Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	
40	ALE	54	Input	TYPE1	
39	AOE		Internal	TYPE2	Control
38	$\overline{BOE_1}$	26	Input	TYPE1	Signals
37	BLE	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	A-in
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	B-in
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	A-out
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	B-out
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
DC Latchup Source Current	
Commercial	−500 mA
Military	−300 mA
Over Voltage Latchup (I/O)	10V
ESD (HBM) Min	2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit of current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH Voltage			2.0			V	Recognized HIGH Signal
V_{IL}	Input LOW Voltage					0.8	V	Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage		Min			−1.2	V	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		Min	2.5			V	I_{OH} = −3 mA
		Mil	Min	2.0			V	I_{OH} = −24 mA
		Comm	Min	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	Mil	Min			0.8	V	I_{OL} = 12 mA
		Comm	Min			0.8	V	I_{OL} = 15 mA
I_{IH}	Input HIGH Current	All Others	Max			5	μA	V_{IN} = 2.7V (Note 1)
			Max			5	μA	V_{IN} = V_{CC}
		TMS, TDI	Max			5	μA	V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test		Max			7	μA	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)		Max			100	μA	V_{IN} = 5.5V
I_{IL}	Input LOW Current	All Others	Max			−5	μA	V_{IN} = 0.5V (Note 1)
			Max			−5	μA	V_{IN} = 0.0V
		TMS, TDI	Max			−385	μA	V_{IN} = 0.0V
V_{ID}	Input Leakage Test		0.0	4.75			V	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
I_{IL} + I_{OZL}	Output Leakage Current		Max			−50		V_{OUT} = 0.5V
I_{OZH}	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		Max	−100		−275	mA	V_{OUT} = 0.0V

Note 1: Guaranteed not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
I_{CEX}	Output HIGH Leakage Current		Max			50	μA	$V_{OUT} = V_{CC}$
I_{ZZ}	Bus Drainage Test		0.0			100	μA	$V_{OUT} = 5.5V$ All Others Grounded
I_{CCH}	Power Supply Current		Max			250	μA	$V_{OUT} = V_{CC}$; TDI, TMS = V_{CC}
			Max			1.0	mA	$V_{OUT} = V_{CC}$; TDI, TMS = GND
I_{CCL}	Power Supply Current		Max			65	mA	V_{OUT} = LOW; TDI, TMS = V_{CC}
			Max			65.8	mA	V_{OUT} = LOW; TDI, TMS = GND
I_{CCZ}	Power Supply Current		Max			250	μA	TDI, TMS = V_{CC}
			Max			1.0	mA	TDI, TMS = GND
I_{CCT}	Additional I_{CC}/Input	All Other Inputs	Max			2.9	mA	$V_{IN} = V_{CC} - 2.1V$
		TDI, TMS Inputs	Max			3	mA	$V_{IN} = V_{CC} - 2.1V$
I_{CCD}	Dynamic I_{CC}	No Load	Max			0.2	mA/MHz	Outputs Open One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed not tested.

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF			Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay D to Q	5.0				1.2 2.0	3.7 4.5	6.5 7.4	ns	4-1, 2
t_{PLH} t_{PHL}	Propagation Delay LE to Q	5.0				1.3 1.8	4.1 4.5	7.4 7.3	ns	4-1, 2
t_{PLZ} t_{PHZ}	Disable Time	5.0				1.6 1.8	4.9 6.0	9.0 10.7	ns	4-3, 4
t_{PZL} t_{PZH}	Enable Time	5.0				1.6 1.0	6.0 5.0	9.5 9.3	ns	4-3, 4

*Voltage Range 5.0V ±0.5V

AC Operating Requirements Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time, H or L Data to LE	5.0		1.7	ns	4-5
t_H	Hold Time, H or L LE to Data	5.0		1.6	ns	4-5
t_W	LE Pulse Width	5.0		2.3	ns	4-2

*Voltage Range 5.0V ±0.5V

AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF			Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay TCK to TDO	5.0				3.6 4.8	5.8 7.4	8.6 10.6	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to TDO	5.0				2.7 4.0	5.6 7.1	9.0 10.9	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to TDO	5.0				5.2 3.6	8.6 6.6	12.5 10.1	ns	4-9, 10
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0				3.9 5.1	6.4 8.0	9.5 11.6	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0				4.7 5.7	7.7 9.1	11.3 13.1	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0				5.5 6.7	9.2 10.7	13.6 15.6	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-DR State	5.0				4.1 4.7	7.7 8.4	12.1 12.7	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-IR State	5.0				4.2 4.7	8.3 9.0	13.5 14.0	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Test Logic Reset State	5.0				5.5 6.3	10.1 10.8	15.6 16.2	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-DR State	5.0				5.8 4.3	9.6 7.7	14.2 11.7	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-IR State	5.0				6.1 4.7	11.0 9.0	16.0 13.7	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Test Logic Reset State	5.0				7.3 5.8	12.5 10.5	18.3 15.8	ns	4-9, 10

*Voltage Range 5.0V ±0.5V

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time, Data to TCK (Note 2)	5.0		2.7	ns	4-11
t_H	Hold Time, Data to TCK (Note 2)	5.0		2.4	ns	4-11
t_S	Setup Time, H or L $\overline{AOE}_1$, $\overline{BOE}_1$ to TCK (Note 1)	5.0		5.1	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{AOE}_1$, $\overline{BOE}_1$ (Note 1)	5.0		1.8	ns	4-11
t_S	Setup Time, H or L Internal AOE, BOE, to TCK (Note 3)	5.0		3.5	ns	4-11
t_H	Hold Time, H or L TCK to Internal AOE, BOE (Note 3)	5.0		1.8	ns	4-11
t_S	Setup Time ALE, BLE (Note 4) to TCK	5.0		5.1	ns	4-11
t_H	Hold Time TCK to ALE, BLE (Note 4)	5.0		1.8	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0		7.9	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0		1.8	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0		6.0	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0		3.0	ns	4-11
t_W	Pulse Width TCK H L	5.0		10.3 10.3	ns	4-12
f_{max}	Maximum TCK Clock Frequency	5.0		50	MHz	
t_{PU}	Wait Time, Power Up to TCK	5.0		100	ns	
t_{DN}	Power Down Delay	0.0		100	ms	

*Voltage Range 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: Timing pertains to BSR 38 and 41 only.

Note 2: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26 and 27-35.

Note 3: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

Note 4: Timing pertains to BSR 37 and 40 only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.8	pF	$V_{CC} = 0.0V$
C_{OUT} (Note 1)	Output Capacitance	13.8	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012

National Semiconductor

SCAN182374A
D Flip-Flop with 25Ω Series Resistor Outputs

General Description

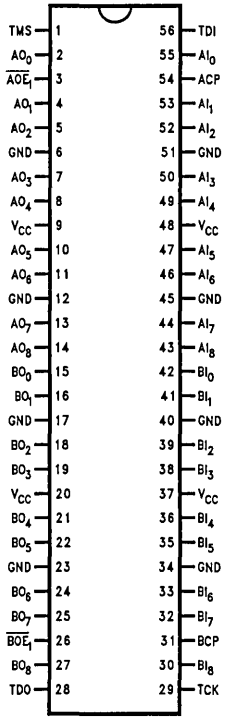
The SCAN182374A is a high performance BiCMOS D-type flip-flop featuring separate D-type inputs organized into dual 9-bit bytes with byte-oriented clock and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- High performance BiCMOS technology
- 25Ω series resistor outputs eliminate need for external terminating resistors
- Buffered positive edge-triggered clock
- TRI-STATE® outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT
- Power up TRI-STATE for hot insert
- Member of National's SCAN Products

Ordering Code: See Section 11

Connection Diagram



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Pin Names	Description
$AI_{(0-8)}$, $BI_{(0-8)}$	Data Inputs
ACP, BCP	Clock Pulse Inputs
$\overline{AOE}_1$, $\overline{BOE}_1$	TRI-STATE Output Enable Inputs
$AO_{(0-8)}$, $BO_{(0-8)}$	TRI-STATE Outputs

Order Number	Description
SCAN182374ASSC	SSOP in Tubes
SCAN182374ASSCX	SSOP in Tape and Reel
SCAN182374AFMQB	Flatpak Military

Truth Tables

Inputs			$AO_{(0-8)}$
ACP	†$\overline{AOE}_1$	$AI_{(0-8)}$	
X	H	X	Z
↗	L	L	L
↗	L	H	H

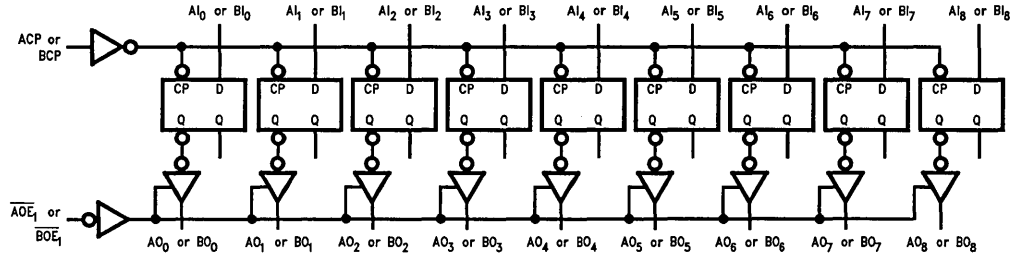
Inputs			$BO_{(0-8)}$
BCP	†$\overline{BOE}_1$	$BI_{(0-8)}$	
X	H	X	Z
↗	L	L	L
↗	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = L-to-H Transition
† = Inactive-to-active transition must occur to enable outputs upon power-up.

Functional Description

The SCAN182374A consists of two sets of nine edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable pins are common to all flip-flops. Each set of the nine flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (ACP or BCP) transition. With the Output Enable ($\overline{AOE}_1$ or $\overline{BOE}_1$) LOW, the contents of the nine flip-flops are available at the outputs. When the Output Enable is HIGH, the outputs go to the high impedance state. Operation of the Output Enable input does not affect the state of the flip-flops.

Logic Diagram



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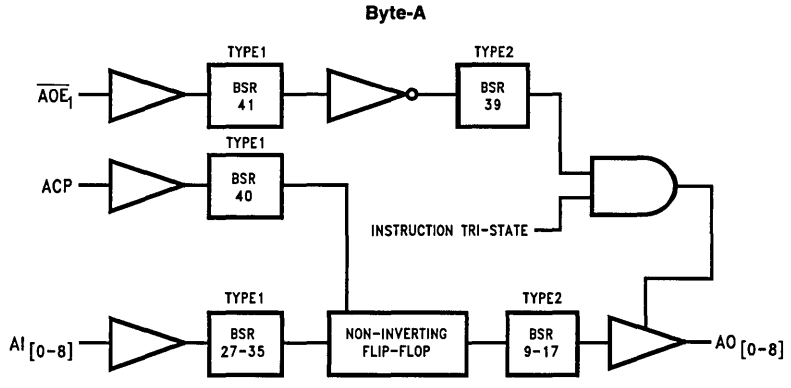
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Block Diagrams



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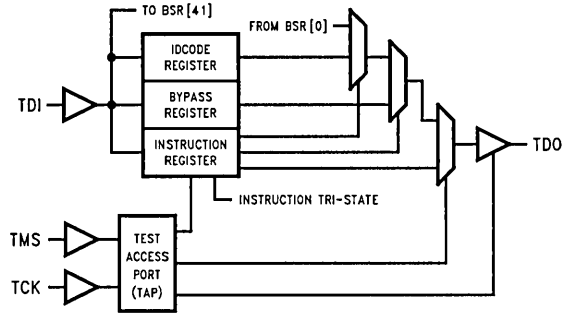
Note: BSR stands for Boundary Scan Register

Block Diagrams (Continued)

Tap Controller



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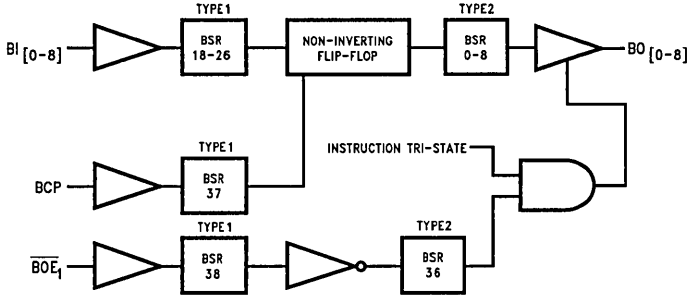
Byte-B



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Note: BSR stands for BOUNDARY-SCAN Register

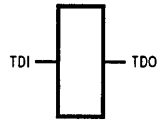
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10-11* for a further description of scan cell TYPE1 and *Figure 10-12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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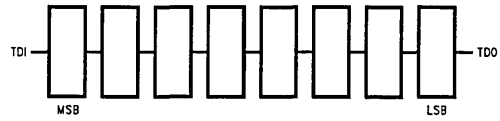
SCAN182374A Product IDCODE
(32-Bit Code per IEEE 1149.1)

Version	Entity	Per Number	Manufacturer ID	Required by 1149.1
0000	111111	0000000111	00000001111	1

MSB **LSB**

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

Instruction Register Sscan Chain Definition



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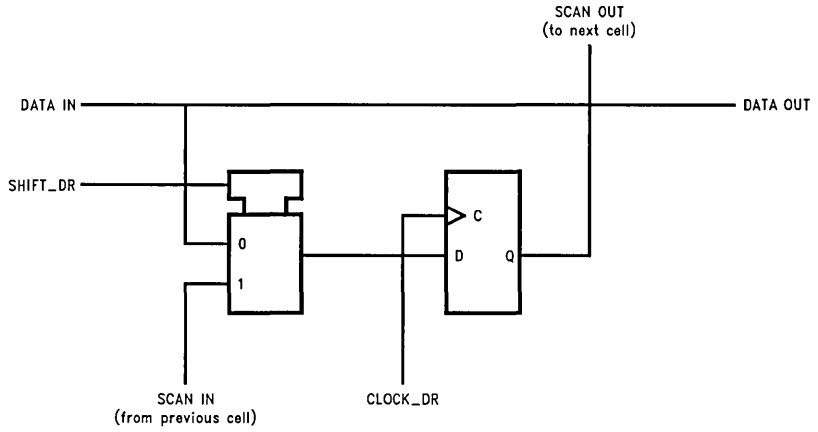
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Other	BYPASS

Description of BOUNDARY-SCAN Circuitry (Continued)

Scan Cell TYPE1



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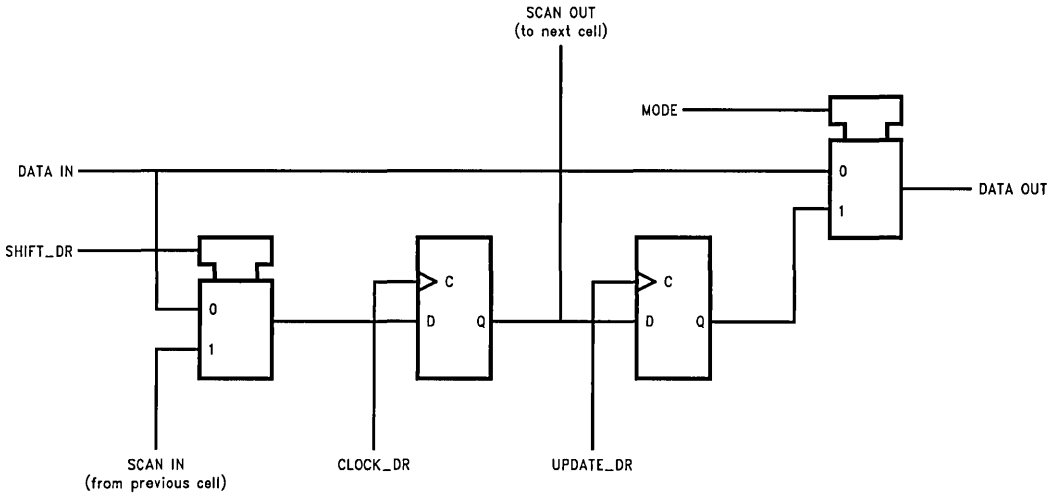
Scan Cell TYPE2

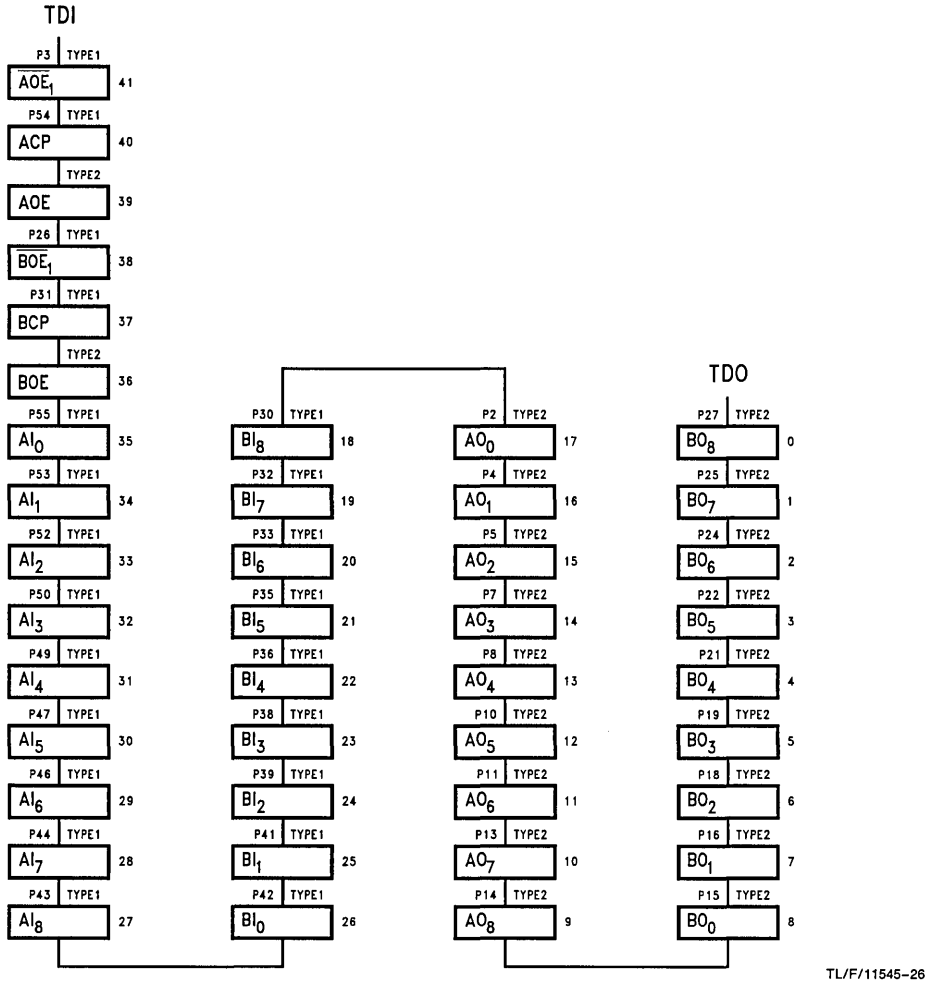


TL/F/11545–20

Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register

SCAN182374A Scan Chain Definition (42 Bits In Length)

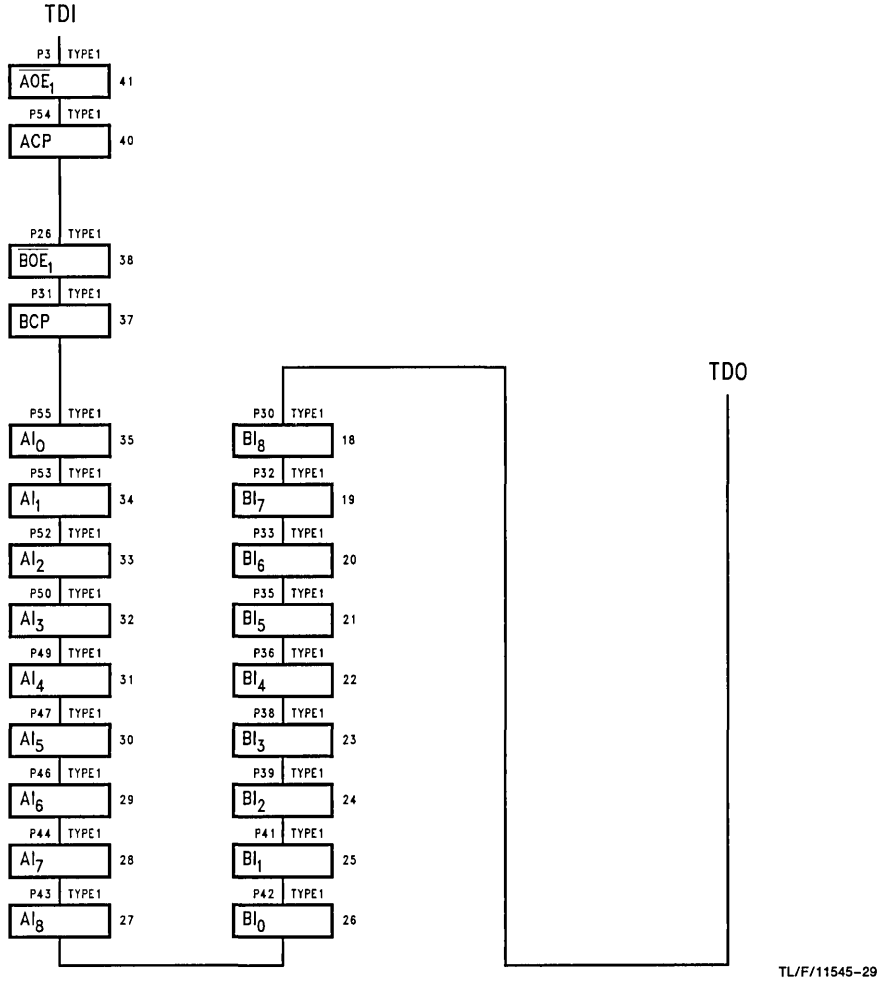


TL/F/11545–26

Description of BOUNDARY-SCAN Circuitry (Continued)

Input BOUNDARY-SCAN Register

Scan Chain Definition (22 Bits in Length)
When Sample In is Active



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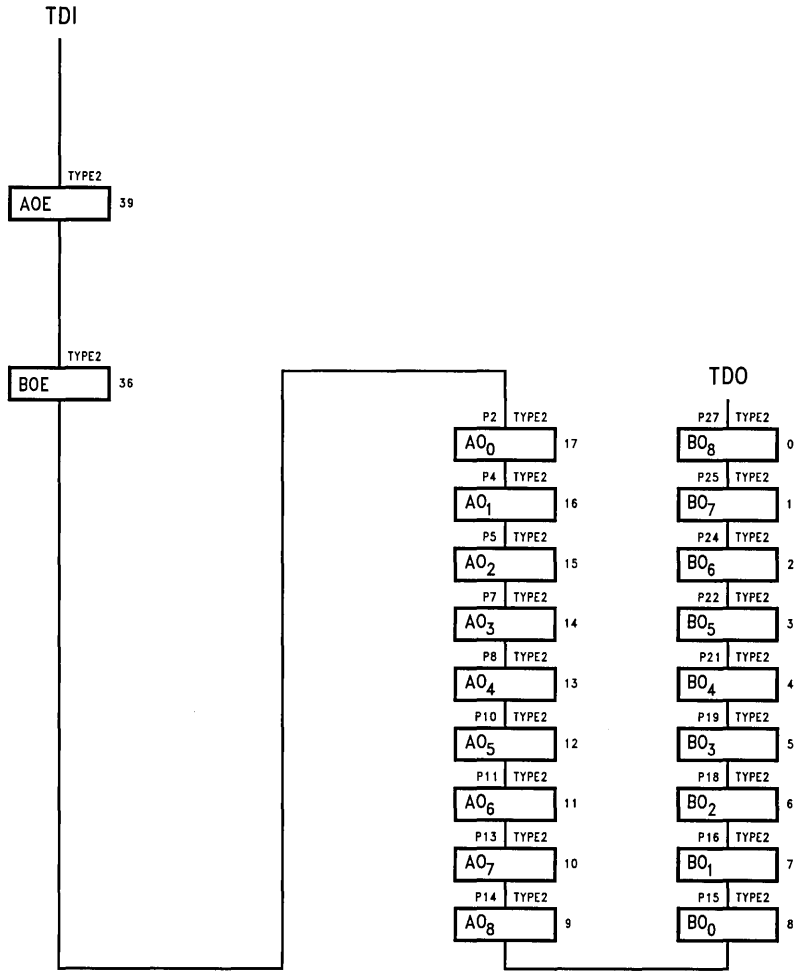
Description of BOUNDARY-SCAN Circuitry (Continued)

Output BOUNDARY-SCAN Register

Scan Chain Definition (20 Bits In Length)
When Sample Out and EXTEST Out are Active



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Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	
40	ACP	54	Input	TYPE1	
39	AOE		Internal	TYPE2	Control
38	$\overline{BOE_1}$	26	Input	TYPE1	Signals
37	BCP	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	A–in
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	B–in
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	A–out
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	B–out
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
DC Latchup Source Current	
Commercial	−500 mA
Military	−300 mA
Over Voltage Latchup (I/O)	10V
ESD (HBM) Min.	2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH Voltage			2.0			V	Recognized HIGH Signal
V_{IL}	Input LOW Voltage					0.8	V	Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage		Min			−1.2	V	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		Min	2.5			V	I_{OH} = −3 mA
		Mil	Min	2.0			V	I_{OH} = −24 mA
		Comm	Min	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage							
		Mil	Min			0.8	V	I_{OL} = 12 mA
		Comm	Min			0.8	V	I_{OL} = 15 mA
I_{IH}	Input HIGH Current	All Others	Max			5	μA	V_{IN} = 2.7V (Note 1)
			Max			5	μA	V_{IN} = V_{CC}
		TMS, TDI	Max			5	μA	V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test		Max			7	μA	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test(I/O)		Max			100	μA	V_{IN} = 5.5V
I_{IL}	Input LOW Current	All Others	Max			−5	μA	V_{IN} = 0.5V (Note 1)
			Max			−5	μA	V_{IN} = 0.0V
		TMS, TDI	Max			−385	μA	V_{IN} = 0.0V
V_{ID}	Input Leakage Test		0.0	4.75			V	I_{ID} = 1.9 μA All Other Pins Grounded
$I_{IH} + I_{OZH}$	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
$I_{IL} + I_{OZL}$	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V
I_{OZH}	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V

Note 1: Guaranteed not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
I_{OS}	Output Short-Circuit Current		Max	−100		−275	mA	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current		Max			50	μA	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test		0.0			100	μA	V_{OUT} = 5.5V All Others Grounded
I_{CCH}	Power Supply Current		Max			250	μA	V_{OUT} = V_{CC}; TDI, TMS = V_{CC}
			Max			1.0	mA	V_{OUT} = V_{CC}; TDI, TMS = GND
I_{CCL}	Power Supply Current		Max			65	mA	V_{OUT} = LOW; TDI, TMS = V_{CC}
			Max			65.8	mA	V_{OUT} = LOW; TDI, TMS = GND
I_{CCZ}	Power Supply Current		Max			250	μA	TDI, TMS = V_{CC}
			Max			1.0	mA	TDI, TMS = GND
I_{CCT}	Additional I_{CC}/Input	All Other Inputs	Max			2.9	mA	V_{IN} = V_{CC} − 2.1V
		TDI, TMS Inputs	Max			3	mA	V_{IN} = V_{CC} − 2.1V
I_{CCD}	Dynamic I_{CC}	No Load	Max			0.2	mA/ MHz	Outputs Open One Bit Toggling, 50% Duty Cycle

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military T_A = −55°C to +125°C C_L = 50 pF			Commercial T_A = −40°C to +85°C C_L = 50 pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to Q	5.0				1.4 2.1	4.6 4.9	6.1 6.8	ns	4-1, 2
t_{PLZ} t_{PHZ}	Disable Time	5.0				1.9 1.8	4.6 4.8	8.0 8.7	ns	4-3, 4
t_{PZL} t_{PZH}	Enable Time	5.0				2.0 1.4	6.7 6.0	9.4 8.2	ns	4-3, 4

*Voltage Range 5.0V ±0.5V

AC Operating Requirements Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military T_A = −55°C to +125°C C_L = 50 pF	Commercial T_A = −40°C to +85°C C_L = 50 pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time, H or L Data to CP	5.0		2.8	ns	4-5
t_H	Hold Time, H or L CP to Data	5.0		2.4	ns	4-5
t_W	CP Pulse Width	5.0		0.0	ns	4-2
f_{max}	Maximum ACP/BCP Clock Frequency	5.0		50	MHz	

*Voltage Range 5.0 is 5.0V ±0.5V.

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AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF			Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay TCK to TDO	5.0				2.9 4.0	5.8 7.3	9.5 11.5	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to TDO	5.0				1.9 3.0	5.6 7.1	10.0 12.1	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to TDO	5.0				4.4 2.7	8.4 6.4	13.2 10.9	ns	4-9, 10
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0				3.4 4.3	6.5 8.1	10.5 12.7	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0				3.9 4.7	7.8 9.1	12.8 14.5	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0				4.7 5.6	9.5 10.9	15.6 17.4	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-DR State	5.0				3.2 3.9	7.8 8.5	13.6 14.2	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-IR State	5.0				3.2 3.8	8.6 9.3	15.0 15.6	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Test Logic Reset State	5.0				4.2 5.0	10.2 11.0	18.0 18.5	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-DR State	5.0				5.0 3.7	9.6 7.7	15.3 13.0	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-IR State	5.0				5.3 4.0	10.8 9.0	17.4 15.1	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Test Logic Reset State	5.0				6.2 4.7	12.6 10.7	20.4 18.1	ns	4-9, 10

*Voltage Range 5.0V ±0.5V

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time Data to TCK (Note 2)	5.0		2.7	ns	4-11
t_H	Hold Time Data to TCK (Note 2)	5.0		3.1	ns	4-11
t_S	Setup Time, H or L $\overline{AOE_1}$, $\overline{BOE_1}$ to TCK (Note 1)	5.0		5.0	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{AOE_1}$, $\overline{BOE_1}$ (Note 1)	5.0		1.8	ns	4-11
t_S	Setup Time, H or L Internal AOE, BOE to TCK (Note 3)	5.0		3.6	ns	4-11
t_H	Hold Time, H or L TCK to Internal AOE, BOE (Note 3)	5.0		2.1	ns	4-11
t_S	Setup Time ACP, BCP (Note 4) to TCK	5.0		3.4	ns	4-11
t_H	Hold Time TCK to ACP, BCP (Note 4)	5.0		1.8	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0		8.7	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0		1.8	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0		6.4	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0		3.2	ns	4-11
t_W	Pulse Width TCK H L	5.0		8.2 11.2	ns	4-12
f_{max}	Maximum TCK Clock Frequency	5.0		50	MHz	
t_{PU}	Wait Time, Power Up to TCK	5.0		100	ns	
t_{DN}	Power Down Delay	0.0		100	ms	

*Voltage Range 5.0V ±0.5V

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: Timing pertains to BSR 38 and 41 only.

Note 2: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0–8, 9–17, 18–26 and 27–35.

Note 3: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

Note 4: Timing pertains to BSR 37 and 40 only.

Capacitance $T_A = 25°C$

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5.8	pF	$V_{CC} = 0.0V$
C_{OUT} (Note 1)	Output Capacitance	13.8	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

National Semiconductor

SCAN182541A
Non-Inverting Line Driver with 25Ω Series Resistor Outputs

General Description

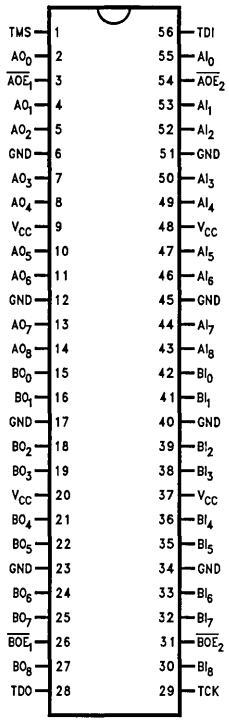
The SCAN182541A is a high performance BiCMOS line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented paired output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary-Scan architecture with the incorporation of the defined Boundary-Scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- High performance BiCMOS technology
- 25Ω series resistor outputs eliminate need for external terminating resistors
- Dual output enable signals per byte
- TRI-STATE® outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT
- Power up TRI-STATE for hot insert
- Member of National's SCAN Products

Ordering Code: See Section 11

Connection Diagram



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Pin Names	Description
$AI_{(0-8)}$	Input Pins, A Side
$BI_{(0-8)}$	Input Pins, B Side
$\overline{AOE}_1$, $\overline{AOE}_2$	TRI-STATE Output Enable Input Pins, A Side
$\overline{BOE}_1$, $\overline{BOE}_2$	TRI-STATE Output Enable Input Pins, B Side
$AO_{(0-8)}$	Output Pins, A Side
$BO_{(0-8)}$	Output Pins, B Side

Order Number	Description
SCAN182541ASSC	SSOP in Tubes
SCAN182541ASSCX	SSOP in Tape and Reel
SCAN182541AFMQB	Flatpak Military

Truth Tables

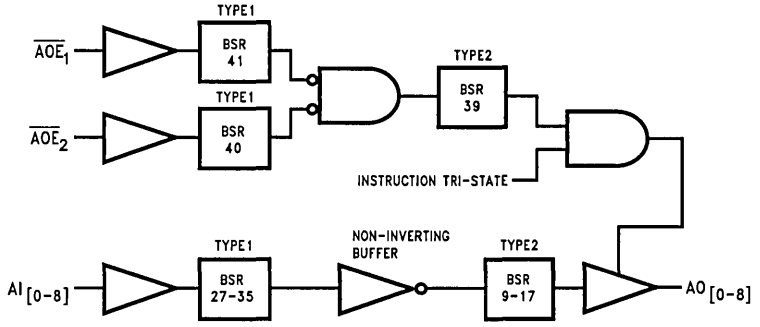
Inputs			$AO_{(0-8)}$
†$\overline{AOE}_1$	†$\overline{AOE}_2$	$AI_{(0-8)}$	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

Inputs			$BO_{(0-8)}$
†$\overline{BOE}_1$	†$\overline{BOE}_2$	$BI_{(0-8)}$	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
† = Inactive-to-active transition must occur to enable outputs upon power-up.

Block Diagrams

Byte A



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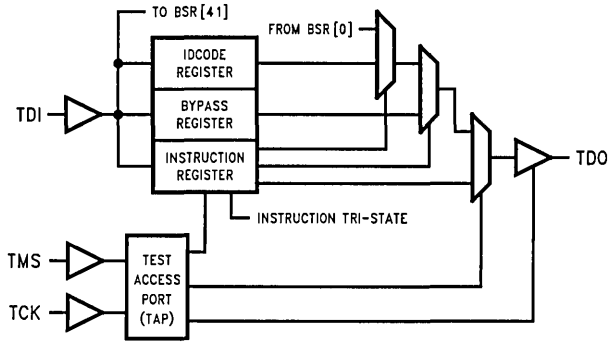
Tap Controller



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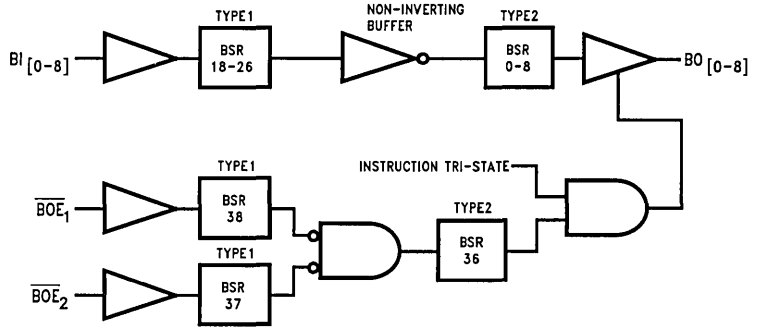
Byte B



TL/F/11543-4

Note: BSR stands for Boundary Scan Register.

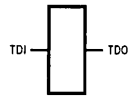
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



TL/F/11543–17

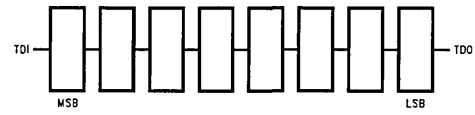
SCAN182541A Product IDCODE
(32-Bit Code per IEEE 1149.1)

Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
0000	111111	0000001001	00000001111	1

MSB **LSB**

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

Instruction Register Scan Chain Definition



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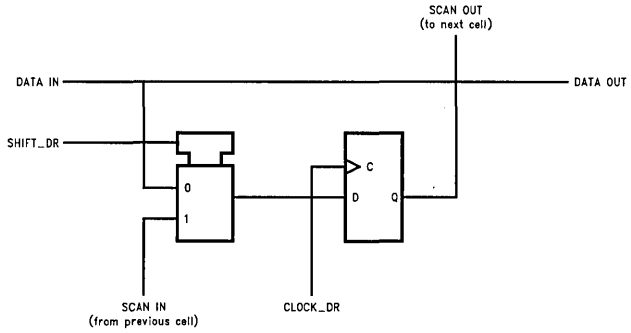
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

Scan Cell TYPE1



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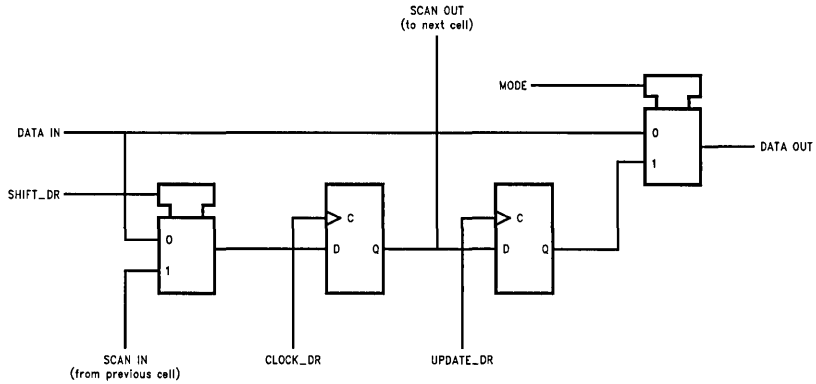
Scan Cell TYPE2



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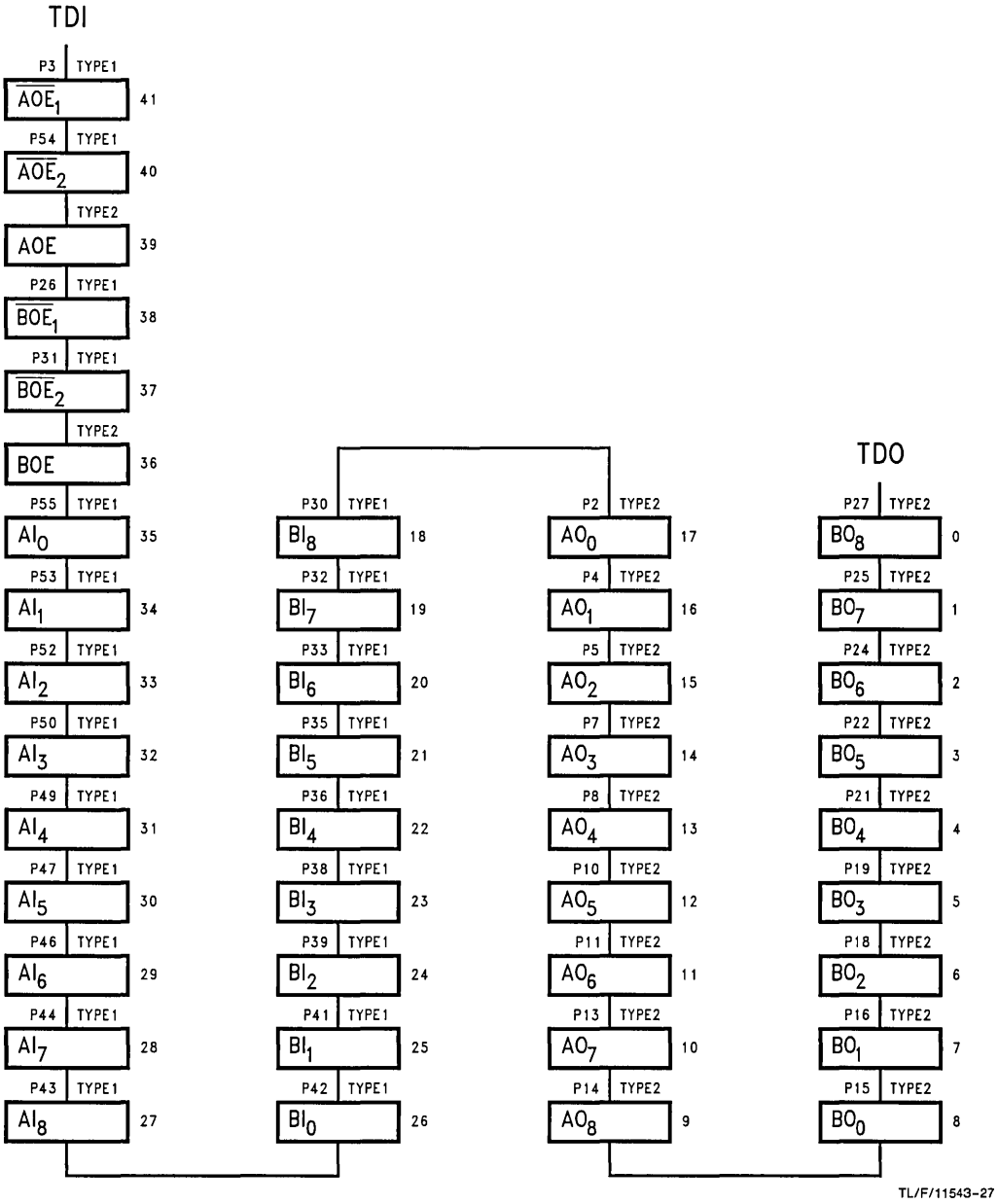
Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register

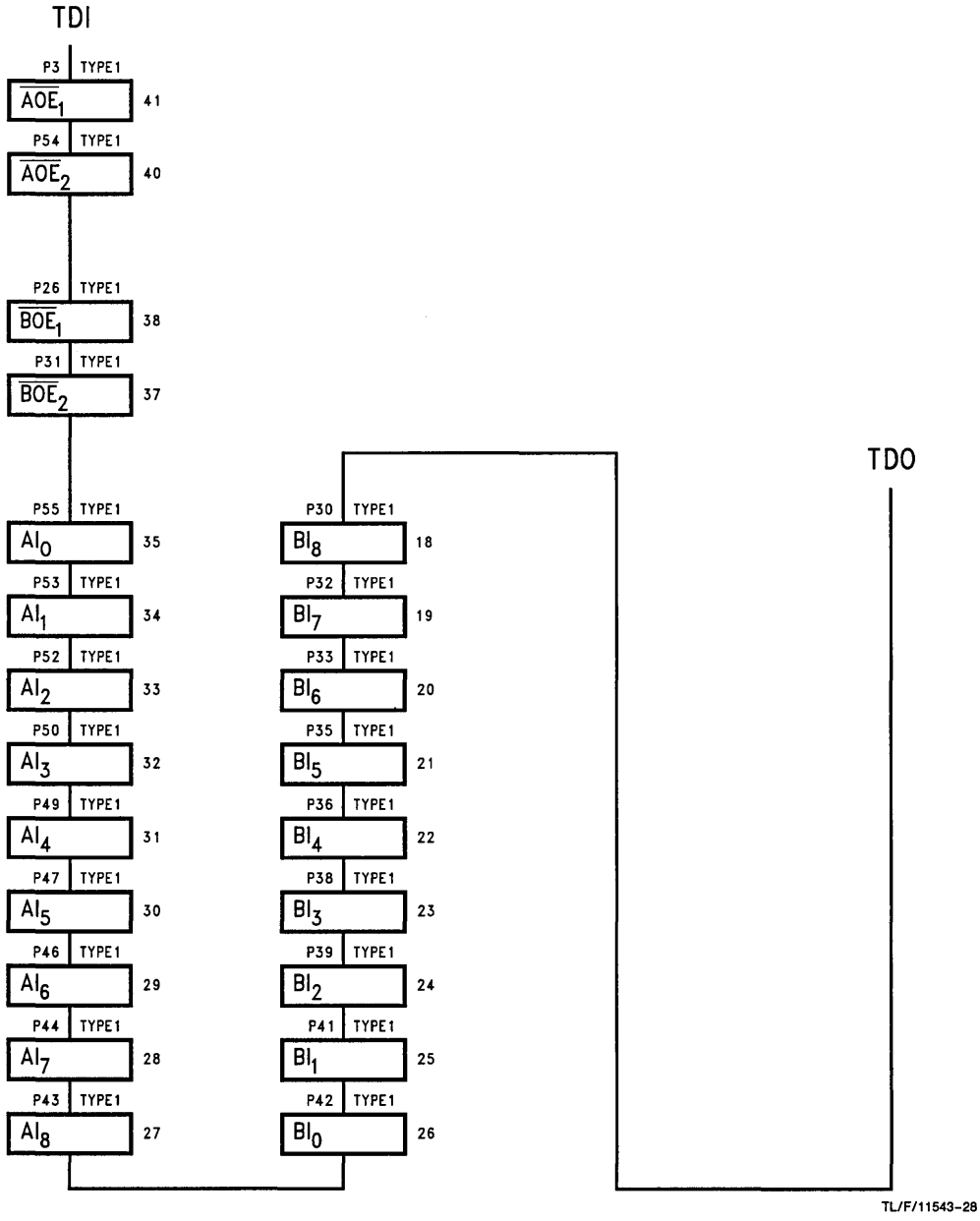
Scan Chain Definition (42 Bits In Length)



TL/F/11543–27

Description of BOUNDARY-SCAN Circuitry (Continued)

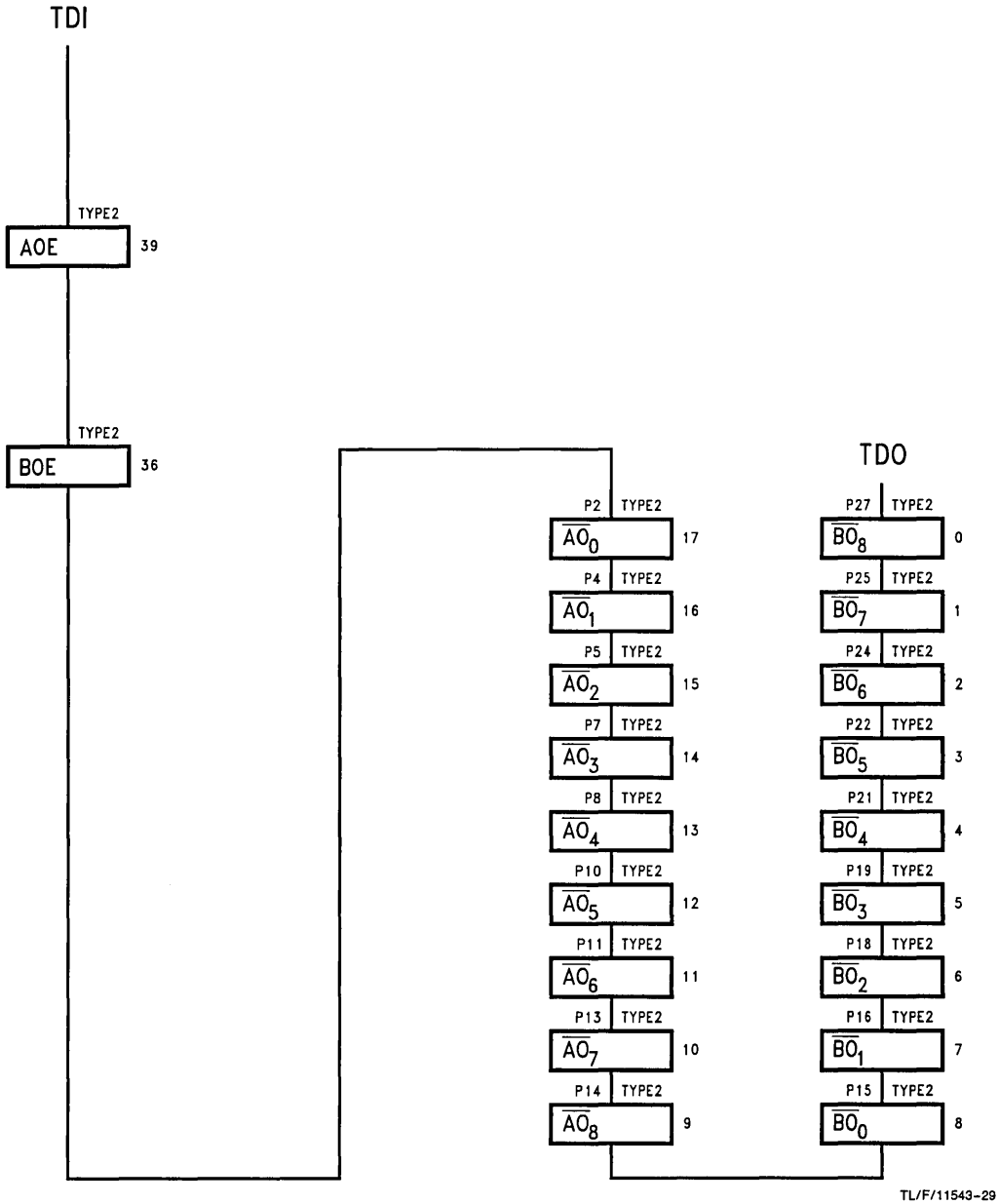
Input BOUNDARY-SCAN Register
Scan Chain Definition (22 Bits In Length)
When SAMPLE-IN Is Active



TL/F/11543–28

Description of BOUNDARY-SCAN Circuitry (Continued)

Output BOUNDARY-SCAN Register
Scan Chain Definition (20 Bits in Length)
When SAMPLE-OUT and EXTEXT Out are Active



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Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	
40	$\overline{AOE_2}$	54	Input	TYPE1	
39	AOE		Internal	TYPE2	Control
38	$\overline{BOE_1}$	26	Input	TYPE1	Signals
37	$\overline{BOE_2}$	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	A-in
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	B-in
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	A-out
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	B-out
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
DC Latchup Source Current	
Commercial	−500 mA
Military	−300 mA
Over Voltage Latchup (I/O)	10V
EDS (HBM) Min	2000V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH Voltage			2.0			V	Recognized HIGH Signal
V_{IL}	Input LOW Voltage					0.8	V	Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage		Min			−1.2	V	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		Min	2.5			V	I_{OH} = −3 mA
		Mil	Min	2.0			V	I_{OH} = −24 mA
		Comm	Min	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	Mil	Min			0.8	V	I_{OL} = 12 mA
		Comm	Min			0.8	V	I_{OL} = 15 mA
I_{IH}	Input HIGH Current	All Others	Max			5	μA	V_{IN} = 2.7V (Note 1)
			Max			5	μA	V_{IN} = V_{CC}
		TMS, TDI	Max			5	μA	V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test		Max			7	μA	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)		Max			100	μA	V_{IN} = 5.5V
I_{IL}	Input LOW Current	All Others	Max			−5	μA	V_{IN} = 0.5V (Note 1)
			Max			−5	μA	V_{IN} = 0.0V
		TMS, TDI	Max			−385	μA	V_{IN} = 0.0V
V_{ID}	Input Leakage Test		0.0	4.75			V	I_{ID} = 1.9 μA All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
I_{IL} + I_{OZL}	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V
I_{OZH}	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		Max	−100		−275	mA	V_{OUT} = 0.0V

Note 1: Guaranteed not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
I_{CEX}	Output HIGH Leakage Current		Max			50	μA	$V_{OUT} = V_{CC}$
I_{ZZ}	Bus Drainage Test		0.0			100	μA	$V_{OUT} = 5.5V$ All Others Grounded
I_{CCH}	Power Supply Current		Max			250	μA	$V_{OUT} = V_{CC}$; TDI, TMS = V_{CC}
			Max			1.0	mA	$V_{OUT} = V_{CC}$; TDI, TMS = GND
I_{CCL}	Power Supply Current		Max			65	mA	V_{OUT} = LOW; TDI, TMS = V_{CC}
			Max			65.8	mA	V_{OUT} = LOW; TDI, TMS = GND
I_{CCZ}	Power Supply Current		Max			250	μA	TDI, TMS = V_{CC}
			Max			1.0	mA	TDI, TMS = GND
I_{CCT}	Additional I_{CC}/Input	All Other Inputs	Max			2.9	mA	$V_{IN} = V_{CC} - 2.1V$
		TDI, TMS Inputs	Max			3	mA	$V_{IN} = V_{CC} - 2.1V$
I_{CCD}	Dynamic I_{CC}	No Load	Max			0.2	mA/MHz	Outputs Open One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed not tested.

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF			Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Q	5.0				1.0 1.9	3.4 4.1	5.2 6.5	ns	4-1
t_{PLZ} t_{PHZ}	Disable Time	5.0				2.0 1.9	5.2 5.6	8.7 9.2	ns	4-3, 4
t_{PZL} t_{PZH}	Enable Time	5.0				2.4 1.6	6.1 5.1	9.6 8.5	ns	4-3, 4

*Voltage Range 5.0V ±0.5V

AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF			Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay TCK to TDO	5.0				3.2 4.5	6.0 7.6	9.4 11.3	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to TDO	5.0				2.5 3.7	5.8 7.4	9.9 11.8	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to TDO	5.0				4.9 3.1	8.6 6.7	12.9 10.7	ns	4-9, 10
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0				3.7 4.9	6.7 8.3	10.3 12.4	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0				4.2 5.3	7.9 9.2	12.2 13.8	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0				5.0 6.2	9.4 10.9	14.6 16.4	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-DR State	5.0				3.7 4.3	7.9 8.7	13.0 13.7	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-IR State	5.0				3.7 4.3	8.5 9.4	14.2 14.8	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Test Logic Reset State	5.0				4.7 5.5	10.1 10.9	16.6 17.3	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-DR State	5.0				5.5 4.0	9.8 7.9	14.7 12.5	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-IR State	5.0				5.8 4.3	10.9 9.0	16.5 14.4	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Test Logic Reset State	5.0				6.6 4.9	12.5 10.5	19.1 16.9	ns	4-9, 10

*Voltage Range 5.0V ±0.5V

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time Data to TCK (Note 2)	5.0		2.2	ns	4-11
t_H	Hold Time Data to TCK (Note 2)	5.0		1.8	ns	4-11
t_S	Setup Time, H or L $\overline{AOE}_n$, $\overline{BOE}_n$ to TCK (Note 1)	5.0		3.7	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{AOE}_n$, $\overline{BOE}_n$ (Note 1)	5.0		1.8	ns	4-11
t_S	Setup Time, H or L Internal AOE_n, BOE_n, to TCK (Note 3)	5.0		2.7	ns	4-11
t_H	Hold Time, H or L TCK to Internal AOE_n, BOE_n (Note 3)	5.0		1.8	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0		7.5	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0		1.8	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0		5.0	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0		2.0	ns	4-11
t_W	Pulse Width TCK H L	5.0		10.0 10.8	ns	4-12
f_{max}	Maximum TCK Clock Frequency	5.0		50	MHz	
t_{PU}	Wait Time, Power Up to TCK	5.0		100	ns	
t_{DN}	Power Down Delay	0.0		100	ms	

*Voltage Range 5.0V ±0.5V

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: Timing pertains to BSR 38 and 41 or BSR 37 and 40.

Note 2: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26 and 27-35.

Note 3: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.8	pF	$V_{CC} = 0.0V$
C_{OUT} (Note 1)	Output Capacitance	13.8	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Section 10

System Test Support Datasheets

Section 10 Contents

National Semiconductor

SCANPSC100F
Embedded Boundary Scan Controller (IEEE 1149.1 Support)

General Description

The SCANPSC100F is designed to interface a generic parallel processor bus to a serial scan test bus. It is useful in improving scan throughput when applying serial vectors to system test circuitry and reduces the software overhead that is associated with applying serial patterns with a parallel processor. The 'PSC100F operates by serializing data from the parallel bus for shifting through the chain of 1149.1 compliant components (i.e., scan chain). Scan data returning from the scan chain is placed on the parallel port to be read by the host processor. Up to two scan chains can be directly controlled with the 'PSC100F via two independent TMS pins. Scan control is supplied with user specific patterns which makes the 'PSC100F protocol-independent. Overflow and underflow conditions are prevented by stopping the test clock. A 32-bit counter is used to program the number of TCK cycles required to complete a scan operation within the boundary scan chain or to complete a 'PSC100F Built-In Self Test (BIST) operation. SCANPSC100F device drivers and 1149.1 embedded test application code are available with National's SCAN Ease software tools.

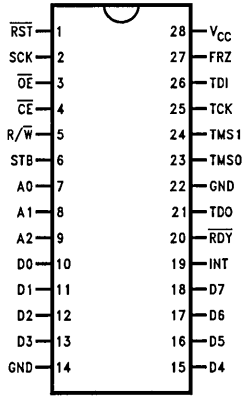
Features

- Compatible with IEEE Std. 1149.1 (JTAG) Test Access Port and Boundary Scan Architecture
- Supported by National's SCAN Ease (Embedded Application Software Enabler) Software
- Uses generic, asynchronous processor interface; compatible with a wide range of processors and PCLK frequencies
- Directly supports up to two 1149.1 scan chains
- 16-bit Serial Signature Compaction (SSC) at the Test Data In (TDI) port
- Automatically produces pseudo-random patterns at the Test Data Out (TDO) port
- Fabricated on FACT™ 1.5 μm CMOS process
- Supports 1149.1 test clock (TCK) frequencies up to 25 MHz
- TTL-compatible inputs; full-swing CMOS outputs with 24 mA source/sink capability

Ordering Code: See Section 11

Connection Diagrams

28-Pin SOIC, DIP and Flatpak



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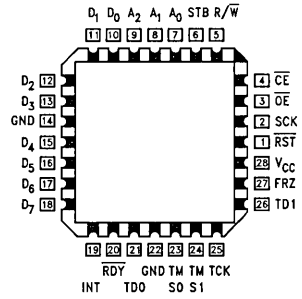
Pin Assignment for LCC



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Order Number	Description
SCANPSC100FSC	SOIC in Tubes
SCANPSC100FSCX	SOIC in Tape and Reel
SCANPSC100FFMQB	Military Flatpak
SCANPSC100FDMQB	Military Ceramic DIP
SCANPSC100FLMQB	Military Leadless Chip Carrier
5962-9475001QYA	Military SMD#, Flatpak
5962-9475001QXA	Military SMD#, CDIP
5962-9475001Q3A	Military SMD#, LCC

Chip Architecture

The 'PSC100 is designed to act together with a parallel bus host as a serial test bus master. Parallel data is written by the host to the 'PSC100, which serializes the data for application to a serial test bus. Serial data returning from the target scan chain(s) is placed on the processor port for parallel reads. Several features are included in the 'PSC100 which make scan test communication more convenient and efficient.

Figure 1 shows the major functional blocks of the 'PSC100 design. The Parallel Processor Interface (PPI) is an asynchronous, 8-bit parallel interface which is used by the host processor to write and read data. The PPI generates the necessary internal data, address, and control signals to complete internal write and read operations.

The Serial Scan Interface (SSI) consists of a bank of double-buffered parallel/serial shift registers (i.e., a 2 x 8 bit FIFO), or Shifter/Buffers. The double buffering improves efficiency by allowing parallel writes or reads to/from one of the two 8-bit FIFOs within the shifter/buffer while the other FIFO is shifting data to/from the scan chain. Three Shifter/Buffers are provided for outgoing serial data and one for incoming serial data. Test Data Out (TDO) is for scanning out test data while the two Test Mode Select signals (TMS0/1) are used to provide user specific control data. Test Data In (TDI) receives serial data from the scan chain. A local control block is associated with each Shifter/Buffer to provide shift and load control as well as providing full or empty status. The SSI also provides Test Clock (TCK) Control. TCK is stopped and started depending on the status of the Shifter/Buffers or the 32-bit Counter. By stopping and starting TCK, scan operations will proceed only when the enabled Shifter/Buffers are ready to send and/or receive serial data.

The 32-bit Counter (CNT32) is a count-down binary counter included to assist in controlling the SSI. The initial state of CNT32 is loaded from the parallel port with four consecutive writes to its address. When enabled, CNT32 is used to program the number of TCKs applied by the SSI to the boundary scan chain(s). The value of CNT32 can also be used to generate interrupts (i.e., when CNT32 reaches terminal count) and to trigger 'PSC100 features, such as, Auto TMS High (discussed later within this datasheet).

The Mode and Status Registers are used to control and observe the operation of the SSI and CNT32. Each of the Shifter/Buffers and CNT32 have an associated mode bit which enables it for participation in on-going operations. Status bits can be used for polling operations.

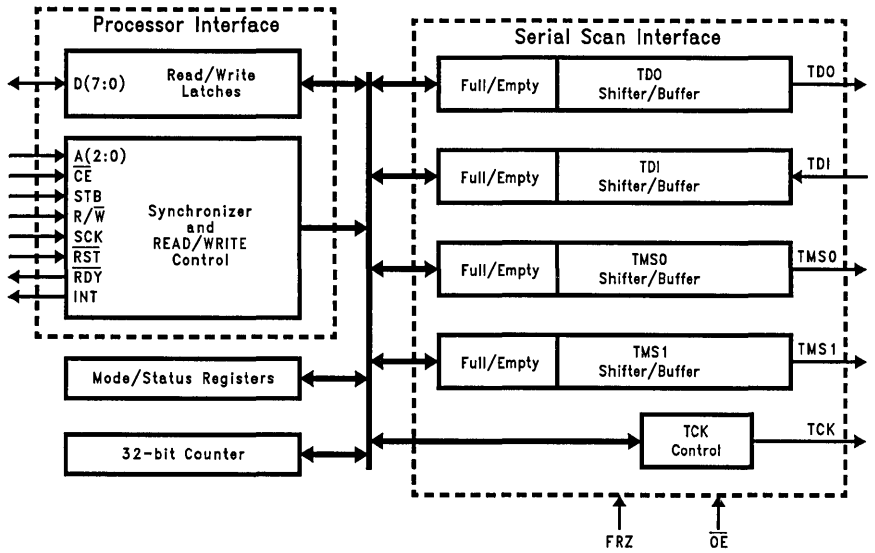

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FIGURE 1. 'PSC100 Block Diagram

Pin Descriptions

Pin Name	Description
$\overline{RST}$ (Input)	The Reset pin is an asynchronous input that, when low, initializes the 'PSC100. Mode bits, Shifter/Buffer and CNT32 control logic, TCK Control, and the PPI are all initialized to defined states. $\overline{RST}$ has hysteresis for improved noise immunity.
SCK (Input)	The System Clock drives all internal timing. The test clock, TCK, is a gated and buffered version of SCK. SCK has hysteresis for improved immunity.
$\overline{OE}$ (Input)	Output Enable TRI-STATEs all SSI outputs when high. A 20 kΩ pull-up resistor is connected to automatically TRI-STATE® these outputs when this signal is floating.
$\overline{CE}$ (Input)	Chip Enable, when low, enables the PPI for byte transfers. D(7:0) and $\overline{RDY}$ are TRI-STATEd if $\overline{CE}$ is high. $\overline{CE}$ has hysteresis for improved noise immunity.
R/$\overline{W}$ (Input)	Read/Write defines a PPI cycle—Read when high, Write when low. R/$\overline{W}$ has hysteresis for improved noise immunity.
STB (Input)	Strobe is used for timing all PPI byte transfers. D(7:0) are TRI-STATEd when STB is high. All other PPI inputs must meet specified setup and hold times with respect to this signal. STB has hysteresis for improved noise immunity.
A(2:0) (Input)	The Address pins are used to select the register to be written to or read from.
D(7:0) (I/O)	Bidirectional pins used to transfer parallel data to and from the 'PSC100.
INT (Output)	Interrupt is used to trigger a host interrupt for any of the defined interrupt events. INT is active high.
$\overline{RDY}$ (TRI-STATE Output)	Ready is used to synchronize asynchronous byte transfers between the host and the 'PSC100. When low, $\overline{RDY}$ signals that the addressed register is ready to be accessed $\overline{RDY}$ is enabled when $\overline{CE}$ is low.
TDO (TRI-STATE Output)	Test Data Out is the serial scan output from the 'PSC100. TDO is enabled when $\overline{OE}$ is low.
TMS(1:0) (TRI-STATE Output)	The Test Mode Select pins are serial outputs used to supply control logic to the UUT. TMS(1:0) are enabled when $\overline{OE}$ is low.
TCK (TRI-STATE Output)	The Test Clock output is a buffered version of SCK for distribution in the UUT. TCK Control logic starts and stops TCK to prevent overflow and underflow conditions. TCK is enabled when $\overline{OE}$ is low.
TDI (Input)	Test Data In is the serial scan input to the 'PSC100. A 20 kΩ pull-up resistor is connected to force TDI to a logic 1 when the TDO line from the UUT is floating.
FRZ (Input)	The Freeze pin is used to asynchronously generate a user-specific pulse on TCK. If the FRZ Enable Mode bit is set, TCK will be forced high if FRZ goes high. FRZ has hysteresis for improved noise immunity.

Mode and Status Registers

MODE REGISTER 0 (MODE0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDO Enable	TDI Enable	CNT32 Enable	TMS0 Enable	TMS1 Enable	Reserved	Auto TMS High Enable	Loop-Around Enable

This register is purely a mode register. All bits are writeable and readable. The value 00100000 is placed in this register upon $\overline{RST}$ low or a synchronous reset operation.

- Bit 7: This bit enables the TDO shifter/buffer for shift operations. If this bit is set, the TDO shifter/buffer will cause TCK to stop if it is empty.
- Bit 6: This bit enables the TDI shifter/buffer for shift operations. If this bit is set, the TDI shifter/buffer will cause TCK to stop if it is full.
- Bit 5: This bit enables the 32-bit counter. If this bit is set, the counter will cause TCK to stop if if has not been loaded or if it has reached terminal count.
- Bit 4: This bit enables the TMS0 shifter/buffer for shift operations. If this bit is set, the TMS0 shifter/buffer will cause TCK to stop if it is empty.
- Bit 3: This bit enables the TMS1 shifter/buffer for shift operations. If this bit is set, the TMS1 shifter/buffer will cause TCK to stop if it is empty.
- Bit 2: This bit is reserved and should remain as a logic 0 during all 'PSC100 operations.
- Bit 1: If this bit is set, TMS will be forced high when the 32-bit counter is at state (00000001)h.
- Bit 0: This bit causes TDI to be connected directly back through TDO for Loop-Around operations.

MODE REGISTER 1 (MODE1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDO Interrupt Enable	TDI Interrrupt Enable	CNT32 Interrupt Enable	PRPG Enable	SSC Enable	Freeze Pin Enable	Test Loop-Back	Test Loop-Back

This register is purely a mode register. All bits are writeable and readable. The value 00000000 is placed in this register upon $\overline{RST}$ low or a synchronous reset operation.

- Bit 7: If this bit is set and the TDO shifter/buffer is not full (i.e., one or both 8-bit TDO FIFOs are empty), the INT pin will go high.
- Bit 6: If this bit is set and the TDI shifter/buffer is not empty (i.e., one or both 8-bit TDI FIFOs are full), the INT pin will go high.
- Bit 5: If this bit is set, and the 32-bit counter is not loaded or has reached terminal count, the INT pin will go high.
- Bit 4: This bit signifies that the TD0 shifter/buffer is reconfigured as a 32-Bit Pseudo Random Pattern Generator. If set, and MODE0 Bit 7 is set, the TDO shifter/buffer will stop TCK until a seed value has been written to all four of the 8-bit LFSR segments.
- Bit 3: This bit signifies that the TD1 shifter/buffer is reconfigured as a 16-Bit Serial Signature Compactor. If set, and MODE0 Bit 6 is set, the TDI shifter/buffer will cause TCK to stop until a seed value has been written to the two TDI registers.
- Bit 2: If this bit is set, a high value on FRZ will force TCK high (see TCK Control Section).
- Bits 1 and 0: These bits are used to control Test Loop-Back operations according to the following table.

MODE1 Bit 1	MODE1 Bit 0	Function
0	0	Normal Operation
0	1	Loop-Back TDO to TDI
1	0	Loop-Back TMS0 to TDI
1	1	Loop Back TMS1 to TDI

Mode and Status Registers (Continued)

MODE REGISTER 2 (MODE2)

Write:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used	Not Used	Not Used	Not Used	Continuous Update	Update Status	Reset	Single Step CNT32

Read:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDO Status	TDI Status	CNT32 Status	TMS0 Status	TMS1 Status	Continuous Update	Reset	Single Step CNT32

This register contains both mode and status bits. Bits 4–7 are status bits only. Bit 3 is a status bit during read operations and a mode bit during write operations. Bits 0–2 are mode bits only. Upon $\overline{RST}$ low, or a synchronous reset, the value placed in MODE2 is 10111000 (Read mode). Latches used to update status bits 3–7 retain their last state upon $\overline{RST}$ and are in an "unknown" state after power-up. To initialize the latches to a known state, they need to be updated using the Update Status bit (bit 2) or continuous update bit (bit 3).

- Bit 7: Set high if the TDO shifter/buffer is not full, i.e., one or both 8-bit TDO FIFOs are ready to be written to.
- Bit 6: Set high if the TDI shifter/buffer is not empty, i.e., one or both 8-bit TDI FIFOs are ready to be read from.
- Bit 5: Set high if the 32-bit counter has not been loaded, or has reached terminal count.
- Bit 4: Set high if the TMS0 shifter/buffer is not full, i.e., one or both 8-bit TMS0 FIFOs are ready to be written to.
- Bit 3 (Read Cycle): Set high if the TMS1 shifter/buffer is not full, i.e., one or both 8-bit TMS1 FIFOs are ready to be written to.
- Bit 3 (Write Cycle): If set, will cause all status bits to be continuously updated.
- Bit 2 (Read Cycle): Shows the state of the Continuous Update bit during read operations (Bit 3 during writes).
- Bit 2 (Write Cycle): If set, will cause a pulse to be issued internally that will update all status bits. This bit will be reset upon completion of the pulse. The state of this bit is not readable. It is reset upon $\overline{RST}$ low.
- Bit 1: If set, will cause a synchronous reset of all functions except the parallel interface. The value of this bit will return to zero when the reset operation is complete.
- Bit 0: If set, will cause the 32-bit counter to count for one SCK cycle (no TCK cycle will be generated). The value of this bit will return to zero when the single step operation is complete.

PROGRAMMING RESTRICTIONS

Because certain mode bits enable shift operations for certain functions, these mode bits should *not* be changed when shift operations are in progress. The alignment of all registers during shift operations is controlled by a 3-bit counter in the TCK control block. Enabling or disabling a function in the middle of a shift operation may disrupt the logic necessary to keep all shifter/buffers byte-aligned.

For example, if the TDO shifter/buffer (already loaded) is enabled while the 3-bit counter value is 3, the shifter/buffer will only shift out only five bits of the first byte loaded.

The following bits should not be changed when shift operations are in progress, i.e., when TCK is enabled (see section on TCK Control).

- MODE0(7:3)
- MODE1(4:3)
- MODE2(0)

Parallel Processor Interface (PPI)

ADDRESS ASSIGNMENT

The following table defines which register is selected for access with the address lines, A(2:0).

A2	A1	A0	R/$\overline{W}$	Function
0	0	0	0	TDO Shifter/Buffer
0	0	0	1	Counter Register 1
0	0	1	0	TDI Shifter/Buffer
0	0	1	1	TDI Shifter/Buffer
0	1	0	0	TMS0 Shifter/Buffer
0	1	0	1	Counter Register 2
0	1	1	0	TMS1 Shifter/Buffer
0	1	1	1	Counter Register 3
1	0	0	0	32-Bit Counter
1	0	0	1	Counter Register 0
1	0	1	0	MODE0
1	0	1	1	MODE0
1	1	0	0	MODE1
1	1	0	1	MODE1
1	1	1	0	MODE2
1	1	1	1	MODE2

Parallel Processor Interface (PPI) (Continued)

TIMING WAVEFORMS

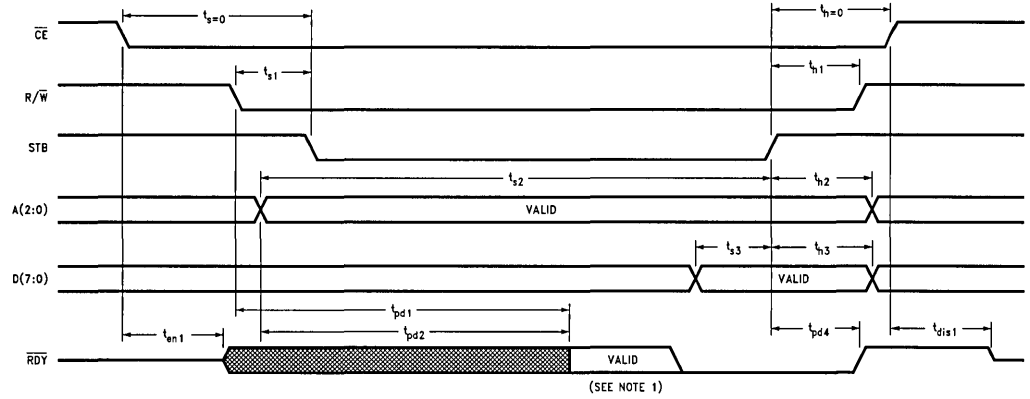

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FIGURE 2. Write Cycle

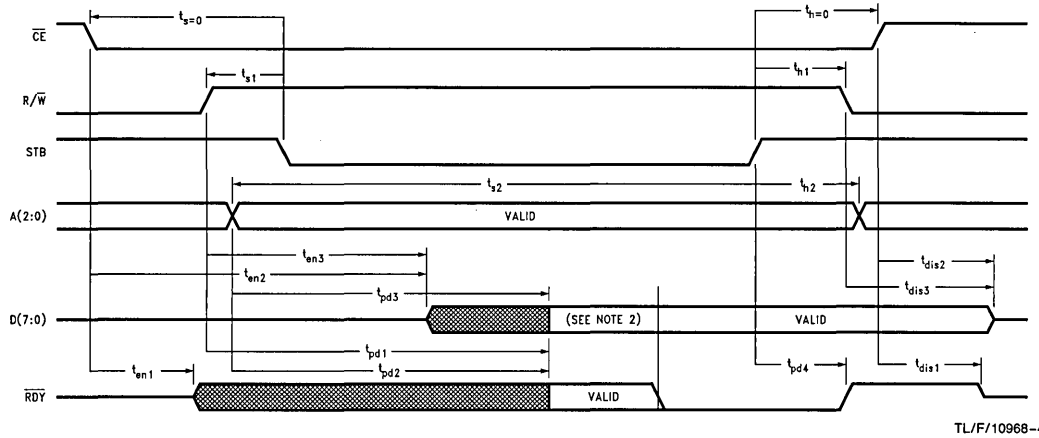

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FIGURE 3. Read Cycle

Note 1: Valid data is provided on the $\overline{RDY}$ line a t_{pd1} after R/$\overline{W}$ is asserted low or a t_{pd2} after valid data is decoded on A2:0. The $\overline{RDY}$ line will remain high until the addressed register is ready to participate in the write operation. This condition only applies when writing to a shifter/buffer and is eliminated (i.e., $\overline{RDY}$ will go low immediately once valid) when using shifter/buffer status polling (discussed later in this datasheet).

Note 2: Valid data will not appear on D7:0 (and $\overline{RDY}$ will remain high) until the addressed register is ready to participate in the read operation. When the addressed register becomes ready (i.e., a byte is available to be read), valid data will be placed on the D7:0 bus and the $\overline{RDY}$ pin will go low allowing the bus cycle to continue. This read cycle delay only applies when reading the TDI shifter/buffer and is eliminated when using shifter/buffer status poling.

Parallel Processor Interface (PPI) (Continued)

TIMING WAVEFORMS (Continued)

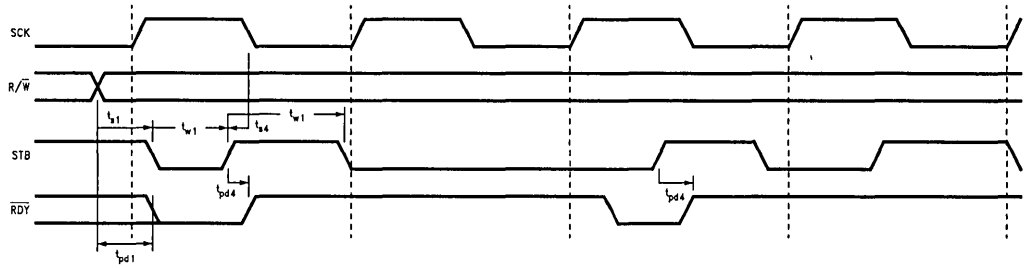

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FIGURE 4. Consecutive Read/Writes (best case timing)

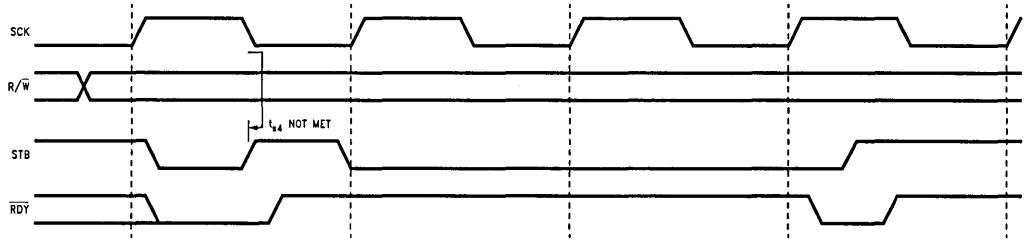

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FIGURE 5. Consecutive Read/Writes (worst case timing)

Figures 4/5: *Figure 4* shows the best case bus cycle timing for SCK and STB during consecutive read or write cycles. The rising edge of strobe occurs a setup time, t_{s4} or before the falling edge of SCK. This allows the cycle to be completed within 1.5 clock SCK clock cycles. *Figure 5* shows the worst case bus cycle timing for SCK and STB during consecutive read or write cycles. The rising edge of strobe does not meet the t_{s4} requirement between STB and SCK. Therefore, the propagation of the internal PSC100 control and reset signals is delayed until the next falling edge of SCK. The bus cycle is then completed 1.5 SCK cycles later creating a total bus cycle time of 2.5 SCK cycles. If worst case timing is considered for bus cycle timing, t_{s4} is not a mandatory timing specification.

Parallel Processor Interface (PPI) (Continued)

TIMING WAVEFORMS (Continued)

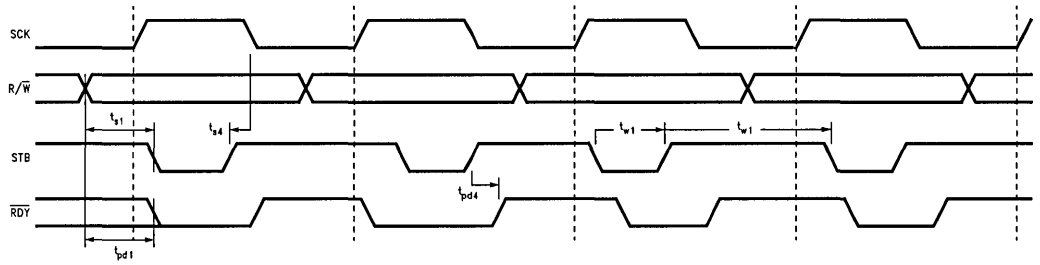

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FIGURE 6. Read/Write or Write/Read (best case timing)

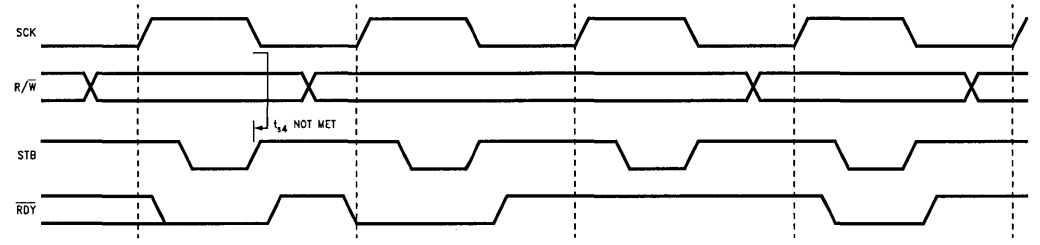

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FIGURE 7. Read/Write or Write/Read (worst case timing)

Note: *Figures 6/7*: This diagram shows the timing for a read followed by a write (or write followed by a read). Separate Read and Write data/address latches and control logic allow consecutive read/write or write/read operations to be overlapped (i.e., do not need to wait 2 or 3 SCK cycles between bus cycles). For the best case timing scenario (*Figure 6*: rising edge of STB to falling edge of SCK greater than t_{s4}), a new bus cycle can be performed each SCK cycle. For the worst timing scenario (*Figure 7*: rising edge of STB to falling edge of SCK is less than t_{s4}), a one SCK cycle delay must be included after each back to back read/write or write/read sequence.

Note: *Figures 4–7* assume that the PSC100 register participating in the bus cycle is ready to accept/provide data. For bus cycles involving a PSC100 shifter/buffer(s), the ready status of a shifter/buffer can be checked using the status bits in Mode Register 2 prior to the start of the bus cycle. Polling is required when the $\overline{RDY}$ pin is **not** used to provide a processor "handshake".

Parallel Processor Interface (PPI) (Continued)

READ AND WRITE CYCLES

A **Write cycle** (see *Figure 2*) is initiated by asserting $\overline{CE}$ and R/$\overline{W}$ low followed by a low on STB a set time later. $\overline{CE}$ and STB are gated within the PSC100F and may be asserted concurrently (i.e., zero setup and hold time). The address is then asserted on A2:0 to indicate which internal address within the PSC100F will be written to by the processor. An address decoder within the PSC100F monitors the address lines for a valid PSC100F register address. Once a valid address has been decoded, the $\overline{RDY}$ line becomes active (a propagation delay time later). The active $\overline{RDY}$ line will go low immediately if the addressed register is ready to accept data. If the addressed register is not ready, the $\overline{RDY}$ pin will remain high preventing the processor from completing the bus cycle. Once the register is ready to receive date (see Table II), the $\overline{RDY}$ pin will go low and processor can resume the write cycle. The processor then forces a high on STB (a wait time after $\overline{RDY}$ goes low) which latches the address (A2:0) and data (D7:0) completing the bus cycle. The $\overline{RDY}$ line is forced high a propagation delay later.

A **Read cycle** (see *Figure 3*) is initiated by asserting $\overline{CE}$ low and R/$\overline{W}$ high followed by a low on STB a set time later. $\overline{CE}$ and STB are gated within the PSC100F and may be asserted concurrently (i.e., zero setup and hold time). The address bits (A2:0) are then asserted to indicate which internal address within the PSC100F will be read by the processor. An address decoder within the PSC100F monitors the address lines for a valid PSC100F register address. Once a valid address has been decoded and if the addressed PSC100F register is ready to be read (see Table II), valid data is placed on the Data lines (D7:0) a propagation delay later and the ready line is asserted low. If the addressed register is not ready (e.g., the TDI shifter/buffer is empty), the ready line will remain high and hold the bus cycle until the register contains valid data. $\overline{RDY}$ will then go low allowing the read cycle to continue. With the high to low edge on $\overline{RDY}$ line, the processor can successfully read the valid data. However, the bus cycle is not completed within the PSC100F until the rising edge on STB which resets the PSC100F read logic (required prior to the start of the next read cycle).

Important note concerning the use of $\overline{RDY}$: The $\overline{RDY}$ signal provides a useful "handshake" between the PSC100F and the processor. However, care must be taken when using the PSC100F $\overline{RDY}$ signal to prevent a large (or indefinite) number of processor generated wait states. For example, if the TDO shifter/buffer is not enabled for shift operations and the processor writes to the TDO shifter/buffer address 3 times, the two registers which make up the TDO shifter/buffer will accept the first two bytes of data, but since the data is not shifting out, the 3rd byte will be held off by the $\overline{RDY}$ signal indefinitely. An equally severe problem could result with a finite number of wait states if the application uses dynamic memories. Holding the local bus with the PSC100F $\overline{RDY}$ line long enough to violate a DRAM refresh time will result in lost data within the dynamic memory.

Writing and Reading without the use of $\overline{RDY}$: With use of worst case PSC100F timing, Write and Read cycles can be successfully completed without the use of the $\overline{RDY}$ signal. All read and write cycles will complete within 2.5 SCK cycles (worst case). Therefore, by assuring at least 2.5 cycles occur after the rising edge of STB, bus cycles can be completed without using the $\overline{RDY}$ "handshake". The critical timing relationship within the PSC100F for write and read operation is between the rising edge of STB and the falling edge of SCK. The rising edge of strobe latches the address/data and also generates the internal signals required to complete read/write within the PSC100F (including a signal with resets the read/write logic and releases the RDY line). The propagation of these internal signals is initiated on the first falling edge of SCK after the STB pin is asserted high. If the rising edge on STB occurs an internal setup time (t_{S4}) or greater before the falling edge of SCK, the bus cycle can be completed within 1.5 SCK cycles (see *Figure 4*). However, if the internal setup time is not met, the propagation of internal control/reset signals is delayed until the next falling edge of SCK (1 SCK cycle later) which effectively completes the read/write operation and reset the logic for the next bus cycle within 2.5 cycles (see *Figure 5*). Synchronizing the rising edge of STB with the falling edge of SCK to assure that t_{S4} is met provides the maximum performance for a read/write operation. However, the asynchronous interface can be used effectively with software delays, hardware delays or programmed wait states (to assure 2.5 SCK cycles are completed) to avoid the need for synchronization.

Consecutive Reads and Writes: Separate control logic and data/address latches are used for a read and write operation within the PSC100F. This allows a write to occur after a read (or conversely, a read to occur after a write) prior to the 1.5/2.5 SCK clock cycle requirements described above. The timing for a read (or write) followed by a write (or read) is shown in *Figures 5* and *6*.

SYNCHRONIZATION

Writes and reads can be synchronized by using any of three methods: polling, interrupts, or wait state generation:

- Status bits may be polled to see if a register is ready to be written to or read from. To stabilize the status bits for read operations, the Update Status bit must be set in MODE2 to latch the status.

  Note: The status bits only provide the state of the shifter/buffers and do not indicate that an internal write or read is complete. Therefore, for applications not using the $\overline{RDY}$ signal to monitor the internal write/read status, timing must be controlled to assure that at least 2.5 SCK cycles are completed between consecutive read or consecutive write cycles.

- Any of three different events can be used to generate interrupts by forcing the INT pin high, see Table I.
- The $\overline{RDY}$ pin can be used to hold off the host until the addressed register is ready to be accessed. As described above, this pin can also be used to hold off additional reads/writes until the synchronizer has recovered from the previous read/write. $\overline{RDY}$ = 0 signifies that the 'PSC100F is ready to complete the current PPI cycle. The logic that determines the state of $\overline{RDY}$ is summarized in Table II.

Reading from CNT32 can be synchronized for testing by using the Single Step Counter mode bit.

Parallel Processor Interface (PPI) (Continued)

TABLE I. Interrupt Logic

MODE1(7) = 1 and TDO Shifter/Buffer Not Full	MODE1(6) = 1 and TDI Shifter/Buffer Not Empty	MODE1(5) = 1 and CNT32 Not Loaded, or at Terminal Count	INT
1	X	X	1
X	1	X	1
X	X	1	1
0	0	0	0

Note: Interrupts are generated using the INT pin. Three events trigger INT high. Each event has its own mode bit associated with it for masking or enabling these interrupts.

TABLE II. Ready State Logic

R/$\overline{W}$	Write Synchronizer Busy	TDO Shifter/Buffer Full and A(2:0) = 0	TMS0 Shifter/Buffer Full and A(2:0) = 2	TMS1 Shifter/Buffer Full and A(2:0) = 3	Read Synchronizer Busy	TDI Shifter/Buffer Empty and A(2:0) = 1	$\overline{RDY}$
0	1	X	X	X	X	X	1
0	X	1	X	X	X	X	1
0	X	X	1	X	X	X	1
0	X	X	X	1	X	X	1
0	0	0	0	0	X	X	0
1	X	X	X	X	1	X	1
1	X	X	X	X	X	1	1
1	X	X	X	X	0	0	0

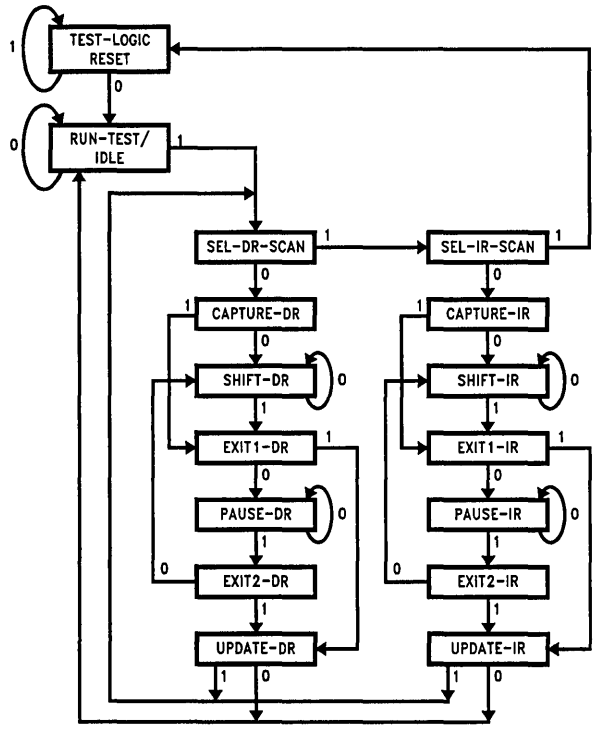

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FIGURE 8. 1149.1 (JTAG) TAP Controller State Diagram

Serial Scan Interface (SSI)

TCK CONTROL

TCK CONTROL is the central control block that enables or disables shift operations and provides byte alignment for the shifter/buffers. The state of all shifter/buffers and the 32-bit counter (CNT32) is evaluated here and TCK is stopped and started. A clock enable circuit allows the "TCK enable" signal to change only when SCK is low; therefore, TCK always stops low. TCK does not toggle (remains low) under the following conditions:

- TDO Shifter/Buffer is enabled and empty.
- TDO Shifter/Buffer is enabled in PRPG mode and is not fully loaded.
- TDI Shifter/Buffer is enabled and full.
- TDI Shifter/Buffer is enabled in SSC mode but is not fully loaded with an initial value.
- TMS0 Shifter/Buffer is enabled and empty.
- TMS1 Shifter/Buffer is enabled and empty.
- CNT32 is enabled but not loaded.
- CNT32 is enabled and has reached terminal count.

Also included within the TCK control block in CNT3, a 3-bit count up counter. CNT3 is included to maintain byte alignment within the shifter/buffers by providing a signal to toggle between the two 8-bit FIFOs which comprise the shifter/buffer. The toggling operation occurs, in an enabled shifter/buffer, each time CNT3 counts 8 TCK cycles or when CNT32 reaches terminal count. The CNT3 is reset to 0 when CNT32 reaches terminal count or after a PSC100 reset condition.

FREEZE MODE. This mode is included in the TCK control block to support the 1149.1 SAMPLE operation. The intent of the SAMPLE instruction is to allow device input and output levels to be observed during normal system operation. Data is latched (or "sampled") into the boundary scan registers when the TAP controller (see *Figure 8* on previous page) transitions from the Capture-DR state to the Shift-DR state (if SAMPLE/ PRELOAD is the active instruction). Synchronizing this "transition" (rising edge of TCK with TMS at logic low) with a known system state is imperative to an accurate pass/fail assessment. The Freeze Mode provides a means of asynchronously creating the TCK pulse via an external PSC100 pin. When the Freeze Pin Enable bit (bit 2 in Mode Register 1) is set, a logic high on the PSC100 FRZ input pin will cause TCK to go high. Once the transition is complete, the Freeze Mode can be removed (i.e. Freeze Pin Enable bit returned to logic 0 or Freeze pin forced low) and the sampled data can be shifted out/evaluated using the "standard" PSC100 protocol. *Figure 9* illustrates the logic implementation of the Freeze feature. It should be noted that Freeze mode is simply gated with the TCK output and does not disable shift operations within the shifter/buffers or disable CNT32. Therefore, no shifting or TCK counting using CNT32 should be performed when Freeze mode is enabled.

The "standard" mode of TCK control uses CNT32 in conjunction with the status registers to start and stop TCK. For this mode, CNT32 is enabled and loaded with the number of TCK cycles required to shift the desired bits to/from the scan chain. The shifter/buffer(s) participating in the shift operation is enabled and provides the necessary full/empty status to stop TCK for processor writes/reads. This mode of TCK control provides a systematic protocol for managing PSC100 operations (specifically, handling partial bytes). Another option for TCK control relies solely on the status of the shifter/buffers (i.e., CNT32 is disabled) to start and stop TCK. This option eliminates the time required to load CNT32, but makes management of partial bytes (see shifter/buffer description section) more cumbersome.

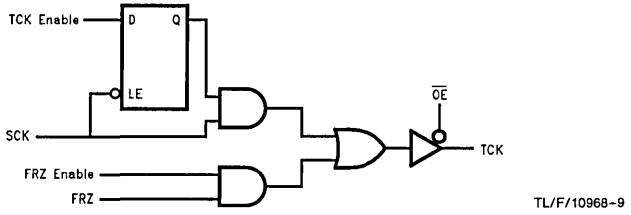

FIGURE 9. TCK Logic

Serial Scan Interface (SSI) (Continued)

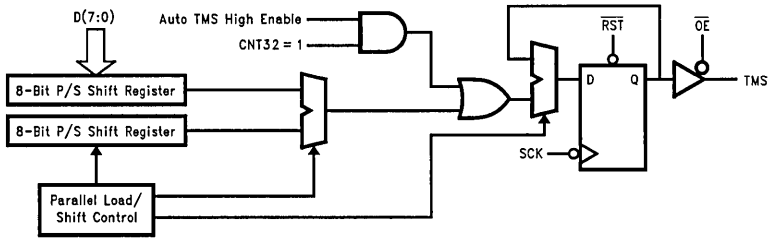

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FIGURE 10. TMS Shifter/Buffer Block Diagram

TMS(1:0) SHIFTER/BUFFERS

The TMS Shifter/Buffer block diagram is shown in *Figure 10*. These two blocks take parallel data and serialize it for shift operations through the serial port pins TMS0 and TMS1.

Double-buffering is achieved by configuring the shifter/buffer as a 2 x 8 FIFO. Write and shift operations are controlled by a local state machine that accepts stimulus from the PPI, Mode Registers, CNT32 and TCK Control section. The TMS outputs always change on the falling edge of SCK. The order of shifting is least significant bit first. TMS(1:0) are forced high upon $\overline{RST}$ low. TMS(1:0) are TRI-STATEd when $\overline{OE}$ is high.

Write operations are completed if the shifter/buffer is not full (independent of whether shifter/buffer is enabled or disabled). Otherwise they are ignored. Shifting occurs when the following conditions are all true:

- TMS is enabled with its respective mode bit.
- TMS shifter/buffer is not empty.
- TCK is enabled according to the logic in TCK Control.

When shift operations are not enabled, the TMS output retains its last state. During long shift sequences, the TMS shifter/buffer can be disabled and held static so that shift operations are concentrated only on TDI and TDO. The TMS output also retains its last state when Test Loop-Back operations are in progress.

Local select circuitry is used to toggle back and forth between the two registers of the "FIFO" when shifting. At any given time, one register is selected for shift operations. The other holds its previous state or can accept new parallel data. Shift register selection changes due to the following two events:

- CNT3 in TCK Control signals that 8 bits have been shifted. This event is used for basic toggling between each of the two shift registers.
- CNT32 enabled and at terminal count. This event is used to account for scan lengths which are not multiples of eight. When shift register selection changes due to this signal, any data remaining in the shift register is unused.

AUTO TMS HIGH MODE. This feature is included in the TMS shifter/buffer block to improve the efficiency of the PSC100 in supporting shift operations within the 1149.1 devices connected to the SSI. Shifting data and instructions into 1149.1 compliant devices requires that their TAP controllers be sequenced to the Shift-DR or Shift-IR states (see *Figure 8*). Once in this state, shifting occurs by holding TMS low and clocking TCK. The last bit is shifted when the TAP controller transitions to the EXIT1 state. This transition requires a logic 1 on TMS. The Auto TMS High feature, enabled by setting bit 1 of Mode Register 0, automatically creates a logic 1 on the TMS lines of the PSC100 when CNT32 = 1. Consequently, the last bit is shifted out without having to load specific TMS data into the shifter/buffer.

Note: Auto TMS High mode creates a logic 1 on both TMS lines (i.e., TMS0 and TMS1). Therefore, when using the Auto TMS High feature, all 1149.1 devices connected to the TMS line not participating in the current JTAG test operations should be placed in the Test-Logic-Reset TAP controller state to prevent inadvertent TAP controller transitions.

Serial Scan Interface (SSI) (Continued)

TDO SHIFTER/BUFFER

The TDO Shifter/Buffer block diagram is shown in *Figure 11*. This block takes parallel data and serializes it for shift operations through the serial port pin TDO. During normal shift modes, double-buffering is achieved by configuring the shifter/buffer as a 2 x 8 FIFO. This block can also be configured as a 32-bit Pseudo Random Pattern Generator (PRPG) with two additional 8-bit parallel-to-serial shift registers. Write and shift operations are controlled by a local state machine that accepts stimulus from the PPI, Mode Registers, CNT32, and the TCK Control section. The TDO output always changes on the falling edge of SCK. The order of shifting is least significant bit first. TDO is forced high upon $\overline{RST}$ low. TDO is TRI-STATEd when $\overline{OE}$ is high.

Write operations are completed if the shifter/buffer is not full (independent of whether shifter/buffer is enabled or disabled). Otherwise they are ignored.

Shifting occurs when the following conditions are all true:

- TDO is enabled with its respective mode bit.
- TDO shifter/buffer is not empty.
- TCK is enabled according to the logic in TCK Control.

When shift operations are not enabled, the TDO output retains its last state. The TDO output also retains its last state when Test Loop-Back operations are in progress.

Local select circuitry is used to toggle back and forth between the two registers of the "FIFO" when shifting. At any given time, one register is selected for shift operations. The other holds its previous state or can accept new parallel data. Shift register selection changes due to the following two events:

- CNT3 in TCK Control signals that 8 bits have been shifted. This event is used for basic toggling between each of the two shift registers.
- CNT32 enabled and at terminal count. This event is used to account for scan lengths which are not multiples of eight. When shift register selection changes due to this signal, any data remaining in the shift register is unused.

PRPG MODE. By setting MODE1(4), the TDO Shifter/Buffer is reconfigured as a 32-bit PRPG (Pseudo Random Pattern Generator) using the primitive polynomial:

$$F(X) = X^{32} + X^{22} + X^2 + X + 1$$

The PSC100 was developed to support both 1149.1 and non-1149.1 serial test methodologies. Since 1149.1 compliant devices include boundary scan registers on control pins (i.e. OE), which must remain fixed during boundary scan interconnect testing, generating pseudo-random patterns with PRPG mode provides limited usefulness for boundary scan test operations. PRPG mode may provide usefulness in other serial test or non-test related implementations which do not require fixed bits in the serial chain.

Figure 12 shows a block diagram of the Linear Feedback Shift Register hookup.

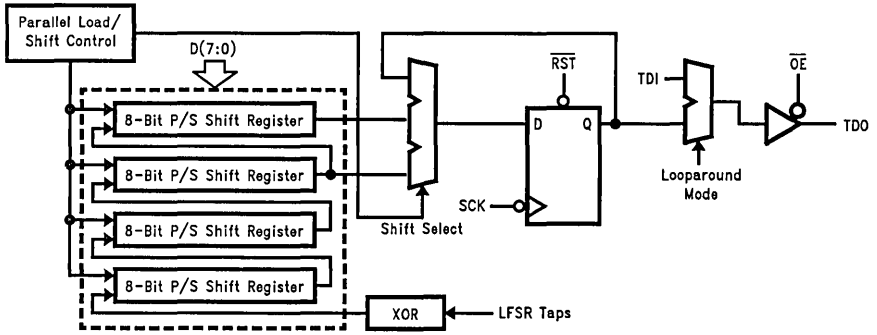

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FIGURE 11. TDO Shifter/Buffer Block Diagram Register Hookup

Serial Scan Interface (SSI) (Continued)

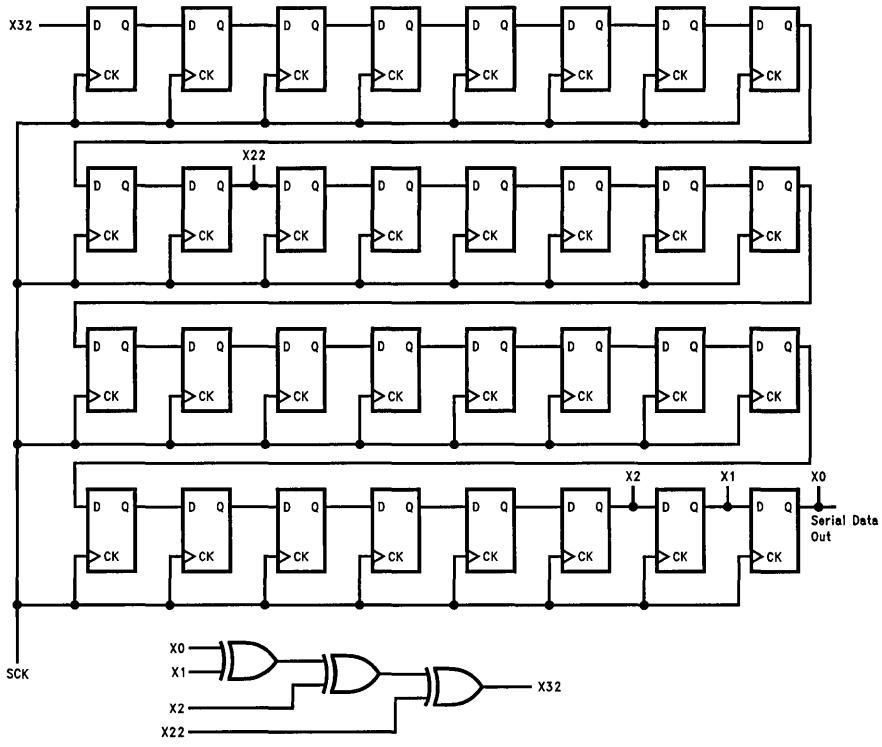

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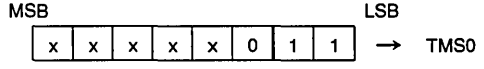
FIGURE 12. TDO PRPG Block Diagram

The PRPG is loaded by four PPI writes to the TDO address. When the PRPG enable bit is set, a pulse is issued internally that initializes the local parallel load logic such that the PRPG is loaded sequentially, least significant byte first, most significant byte last. When in PRPG mode, writes can be completed at any time; however, shift operations will be disabled until the PRPG is fully loaded.

LOOP AROUND MODE. This mode, enabled by setting bit 0 in Mode Register 0, will cause data appearing at the TDI input to be placed directly back on the TDO output. This feature can be used for read-only scan operations where data is shifted into TDI while returning the scan chain to its previous state when shifting is completed. It can also be used to bypass PSC100 devices connected within a boundary scan chain (i.e., a PSC100 located within a chain, but not providing the JTAG TAP data). Loop around has limited usefulness in most boundary scan applications since, typically, data in the scan chain is shifted out and evaluated as new data is shifted into the chain for the next test.

WRITING A PARTIAL BYTE TO THE TMS0, TMS1 OR TDO SHIFTER/BUFFER. Since the TMS0, TMS1 and TDO shifter/buffers shift out least significant bit first, the valid (meaningful) bits within a partial byte (i.e., byte containing <8 valid bits to be shifted to the scan chain) must be stored and written into the shifter/buffer as the least significant bits. This will assure that the desired bits will be accurately shifted to the boundary scan chain. For example, moving the TAP controllers within the boundary scan chain connected to TMS0 from the Pause-DR state to the Run-Test/Idle state requires a 3-bit (110) sequence on TMS0. To provide correct 3-bit sequence on TMS0, the partial byte would be written to the TMS0 shifter/buffer as:



A subsequent enable and load of CNT32 with decimal 3 and enable of the TMS0 shifter/buffer will initialize the shift operation. Terminal count on CNT32 will complete the shift operation. Since terminal count on CNT32 will cause the register selection to change within the shifter/buffer, the values labeled as "x" will not be used and are treated as "don't cares".

TDI SHIFTER/BUFFER

The TDI Shifter/Buffer block diagram is shown in *Figure 13*. This block shifts in serial data from the TDI port and puts it in parallel form for read operations at the PPI. During normal shift modes, double-buffering is achieved by configuring the shifter/buffer as a 2 x 8 FIFO. This block can also be configured as a 16-bit Serial Signature Compactor (SSC). Write, read, and shift operations are controlled by a local state

Serial Scan Interface (SSI) (Continued)

machine that accepts stimulus from the PPI, Mode Registers, CNT32 and the TCK Control section. The TDI input always shifts in data on the rising edge of SCK. The order of shifting is least significant bit first. The TDI input includes a pull-up resistor to force a logic 1 when the test data signal returning from the scan chain is floating.

Read operations are completed if the shifter/buffer is not empty and SSC mode is not enabled. Otherwise they are ignored. Write operations are only possible while in SSC mode. Otherwise they are ignored.

Shifting occurs when the following conditions are all true:

- TDI is enabled with its respective mode bit.
- TDI shifter/buffer is not full.
- TCK is enabled according to the logic in TCK Control.

Local select circuitry is used to toggle back and forth between the two registers of the "FIFO" when shifting. At any given time, one register is selected for shift operations. The other holds its previous state or can accept new serial data. Shift register selection changes due to the following two events:

- CNT3 in TCK Control signals that 8 bits have been shifted in. This event is used for basic toggling between each of the two shift registers.
- CNT32 enabled and at terminal count. This event is used to account for scan lengths which are not multiples of eight. When shift register selection changes due to this signal, a partial byte (i.e., byte with < eight valid data bits shifted from the scan chain) will exist in the corresponding shift register. The embedded test software functions written to support the evaluation of data read from the TDI shifter/buffer must consider bit placement when reading and evaluating a partial byte.

READING A PARTIAL BYTE FROM THE TDI SHIFTER/BUFFER. Data is shifted from the scan chain into each TDI register from most significant bit to least significant bit. Consequently, the valid (i.e., meaningful) bits in a partial byte shifted into a TDI register will reside in the upper significant bit locations. For example, if a scan operation involves shifting and evaluating 53 bits returning to TDI, TDI shifter/buffer must be read 7 times (i.e., 6 full bytes plus a partial byte containing 5 meaningful bits). If the last 5 bits shifted back to the TDI shifter/buffer are 11010, then upon completion of the shift operation (i.e., terminal count on CNT32), the shift register within the TDI shifter/buffer will contain the following partial byte:

	MSB							LSB
TDI →	0	1	0	1	1	x	x	x

Following a read of a partial byte, the embedded test software must adjust the position of the valid bits read from the TDI shifter/buffer or the position of the expected data to assure that an accurate comparison is made (and the non-meaningful bits are masked).

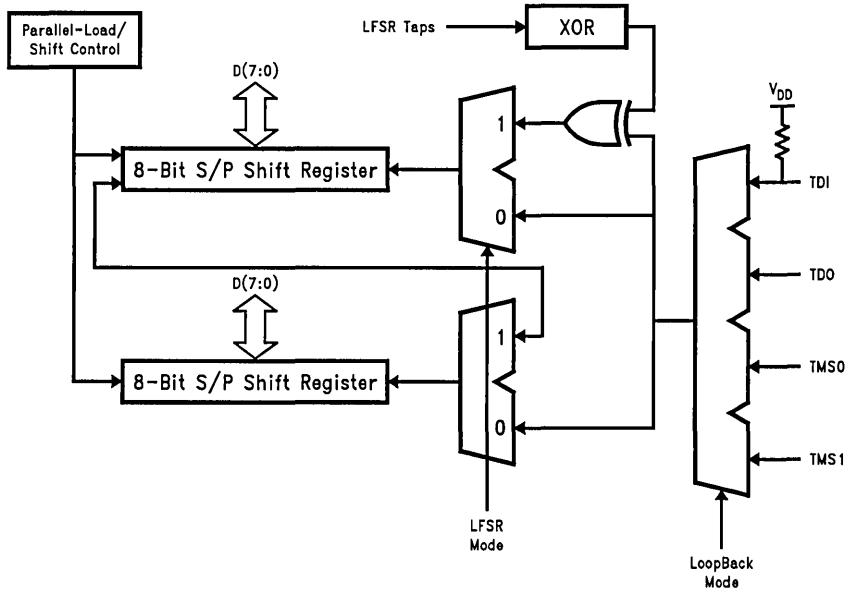


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FIGURE 13. TDI Shifter/Buffer Block Diagram

Serial Scan Interface (SSI) (Continued)

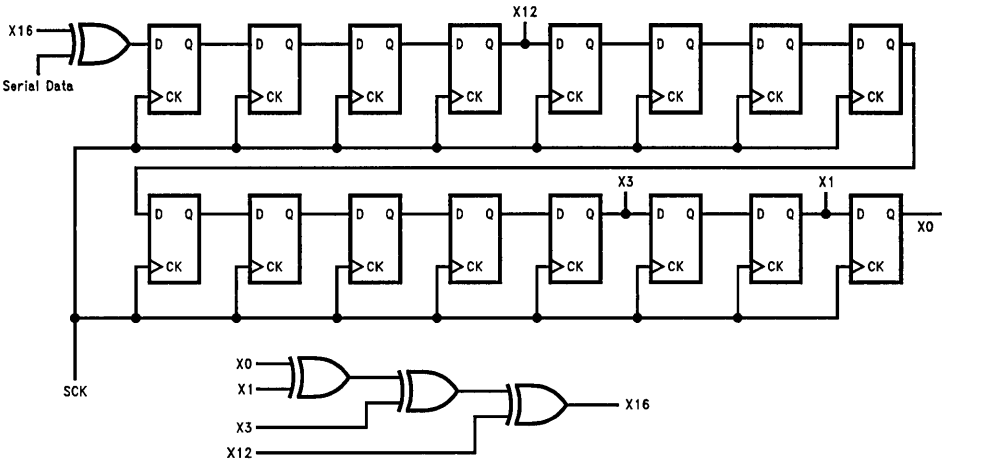

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FIGURE 14. TDI SSC Block Diagram

SSC MODE. By setting MODE1(3), the TDI Shifter/Buffer is reconfigured as a 16-bit SSC (Serial Signature Compactor) using the primitive polynomial:

$$F(X) = X^{16} + X^{12} + X^3 + X + 1$$

Within a chain of 1149.1 compliant devices, there are typically one or more input pins which are driven by uncontrolled signals (i.e., signals which are not driven to known logic levels during a boundary scan CAPTURE operation). These signals are masked during the evaluation of data returning from the scan chain. The SSC within the PSC100 does not provide masking capabilities and, therefore, provides limited usefulness for boundary scan test operations. SSC mode may provide usefulness in other serial test or non-test related implementations which contain predictable data returning into the TDI shifter/buffer.

Figure 14 shows a block diagram of the Linear Feedback Shift Register hookup.

The SSC is loaded by two PPI writes to the TDI address. When the SSC enable bit is set, a pulse is issued internally that initializes the local parallel load logic such that the SSC is loaded sequentially, most significant byte first, least significant byte last. When in SSC mode, writes can be completed at any time; however, shift operations will be disabled until the SSC is fully loaded. PPI reads from TDI are ignored while in SSC mode.

Upon leaving SSC mode an internal pulse causes the TDI shifter/buffer to be full. Also, local read select logic is initialized such that the signature is read most-significant byte first.

TEST LOOP-BACK MODES. This feature provides a means for testing 'PSC100 functionality by looping data appearing at the output of an outgoing shifter/buffer (i.e., TMS0, TMS1 or TDO) back to the input of the TDI shifter/buffer. The loop back function is accomplished with a simple multiplexer (see *Figure 13*) whose path selection is determined by setting the mode bits in MODE1(1:0). Loop back does not disable TCK or prevent shifting of data in the shifter/buffers to the scan chain(s) connected to the PSC100. Therefore, the state and operation of the TAP controllers within the scan chain(s) must be considered when developing Loop-Back test vectors to prevent undesired shifting of data or TAP controller transitions within the scan chain.

32-BIT COUNTER (CNT32)

CNT32 is a 32-bit, count-down binary counter arranged in four 8-bit segments. CNT32 can be loaded independent of its enable/disable status. Loading requires four consecutive writes to its address (least significant byte first). These four writes must *not* be interleaved with writes to any other address or the CNT32 write control logic will be re-initialized. This re-initialization will result in a partially filled counter with an undesired *value*. CNT32 is reset each time the counter hits terminal count or by asserting the $\overline{RST}$ pin. A synchronous reset condition (setting Mode2(1)) does not reset the counter and a new value must be written to CNT32 to provide the desired number of TCK cycles.

SINGLE STEP MODE: All four 8-bit registers are readable for testability; however, there are no update latches similar to the ones used for the status bits. To stabilize the counter for read operations during on-board test, the Single Step Mode has been added. This allows the user to place CNT32 in any state and then count for one SCK cycle (TCK will not toggle when in singled step mode). The result can then be read from the PPI. The counter can be tested by loading it with values at its boundary conditions, and then clocking for one cycle to see the results. For example, the counter could be loaded with the value:

00000001 00000000 00000000 00000000

The next step is to set the Single Step Mode bit so that the counter counts down to the next state and stops. The next value is:

00000000 11111111 11111111 11111111

Four read cycles using the PPI will reveal the results of the test.

Note: CNT32 will not wrap from terminal count (i.e., 00000000h decremented by 1 will remain unchanged and will not wrap to FFFFFFFFh). Therefore, CNT32 should be loaded with a non-zero value prior to a Single Step Mode Operation.

Serial Scan Interface (SSI) (Continued)

TIMING WAVEFORMS

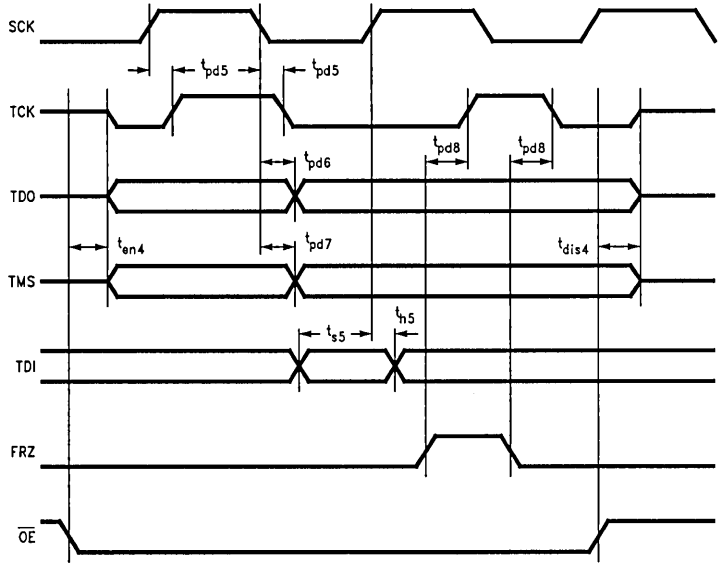

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FIGURE 15. Serial Scan Interface Timing

Embedded Test Software Support

A SCANPSC100 device driver is provided by National to supply functions for performing write, read and shift operations. National also offers a suite of software tools (called SCAN EASE) which enables ATPG or custom generated test vectors to be embedded, applied and evaluated within an IEEE 1149.1 compatible system. SCAN EASE is written to run on a wide range of processor and memory architectures. SCAN EASE includes the source code (ANSI C) and is modular to allow user modification based on application specific needs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
DC Latchup Source or Sink Current	±300 mA
Junction Temperature	
SOIC	+140°C
Storage Temperature	−65°C to +150°C
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of SCAN™ outside of recommended operation conditions.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'PSC100F	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Commercial	−40°C to +85°C
Military	−55°C to +125°C
Minimum Input Edge Rate dV/dt	
SCAN "F" Series Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial T_A = +25°C	Military T_A = −55°C to +125°C	Commercial T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Input Voltage	4.5 5.5		2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Input Voltage	4.5 5.5		0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Output Voltage	4.5 5.5		4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA All Outputs Loaded
V_{OL}	Maximum Low Output Voltage	4.5 5.5		0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = −50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 24 mA All Outputs Loaded
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_{IN} = V_{CC} for TDI, $\overline{OE}$ V_{IN} = V_{CC}, GND for All Others
I_{ILR}	Maximum Input Leakage Current	5.5		−385	−385	−385	μA	V_{IN} = GND for TDI, $\overline{OE}$ Only
I_{OLD}	Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max Maximum Test Duration = 2.0 ms, One Output Loaded at a Time

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$		Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OHD}	Minimum Dynamic Output Current	5.5			−50	−75	mA	V_{OHD} = 3.85V Min Maximum Test Duration = 2.0 ms, One Output Loaded at a Time
I_{OZ}	Maximum TRI-STATE Leakage Current			±0.5	±10.0	±5.0	µA	$V_{IN} = V_{CC}$, GND V_{IN} ($\overline{OE}$, R/$\overline{W}$, $\overline{CE}$, STB) = V_{IL}, V_{IH}
I_{OZT}	Maximum I/O Leakage Current			±0.6	±11.0	±6.0	µA	$V_{IN} = V_{CC}$, GND $V_O = V_{CC}$, GND V_{IN}(R/$\overline{W}$, $\overline{CE}$, STB) = V_{IL}, V_{IH}
I_{CC}	Maximum Quiescent Supply Current	5.5		8	160	80	µA	TDI, $\overline{OE}$ Float
I_{CCmax}	Maximum Quiescent Supply Current	5.5		768	920	840	µA	TDI, $\overline{OE}$ low
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.60	1.50	mA	$V_{IN} = V_{CC} - 2.1V$ Float: TDI, $\overline{OE}$
I_{CCTR}	Maximum I_{CC}/Input	5.5	0.65		1.65	1.65	mA	$V_{IN} = V_{CC} - 2.1V$ TDI and $\overline{OE}$ Only Float Untested Pin
I_{CCD}	Dynamic Power Supply Current (Note 1)	5.5	1.70	2.30	2.30	2.30	mA/ MHz	$V_{IH} = V_{CC}$, V_{IL} = 0, V_{CC} = Max, Outputs Open, F_{SCK} = 25 MHz

Note 1: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

AC Electrical Characteristics/Operating Requirements

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
PARALLEL PROCESSOR INTERFACE (PPI)											
t_{pd1}	Prop Delay R/$\overline{W}$ to $\overline{RDY}$	5.0	5.0	14.0	19.5	5.0	24.0	5.0	24.0	ns	2, 3, 4
t_{pd2}	Prop Delay A to $\overline{RDY}$	5.0	5.0	14.0	19.5	5.0	24.0	5.0	24.0	ns	2, 3
t_{pd3}	Prop Delay A to D	5.0	5.0	14.0	19.5	5.0	24.0	5.0	24.0	ns	3
t_{pd4}	Prop Delay STB to $\overline{RDY}$	5.0	8.0	14.5	19.0	7.0	24.0	8.0	20.5	ns	2–4, 6
t_{en1}	Enable Time $\overline{CE}$ to $\overline{RDY}$	5.0	2.0	7.0	10.0	2.0	13.0	2.0	11.0	ns	2, 3
t_{dis1}	Disable Time $\overline{CE}$ to $\overline{RDY}$	5.0	1.0	5.5	8.0	1.5	10.0	1.0	9.0	ns	2, 3
t_{en2}	Enable Time $\overline{CE}$ to D	5.0	3.0	9.5	13.5	1.5	16.5	3.0	14.5	ns	3
t_{dis2}	Disable Time $\overline{CE}$ to D	5.0	2.5	7.5	11.0	2.5	14.5	2.5	12.0	ns	3

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Electrical Characteristics/Operating Requirements (Continued)

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
PARALLEL PROCESSOR INTERFACE (PPI) (Continued)											
t_{en3}	Enable Time R/$\overline{W}$ to D	5.0	3.0	10.0	14.0	3.0	17.5	3.0	15.0	ns	3
t_{dis3}	Disable Time R/$\overline{W}$ to D	5.0	3.0	8.5	12.5	3.0	16.0	3.0	13.5	ns	3
t_{h1}	Hold Time, R/$\overline{W}$ to STB	5.0	0.5	0.0		0.5		0.5		ns	2–4, 6
t_{s1}	Setup Time R/$\overline{W}$ to STB	5.0	1.0	0.0		1.0		1.0		ns	2–4, 6
t_{h2}	Hold Time, A to STB ↑	5.0	4.0	2.5		4.5		4.0		ns	2, 3
t_{s2}	Setup Time, A to STB ↑	5.0	4.0	1.5		5.0		4.0		ns	2, 3
t_{h3}	Hold Time, D to STB ↑	5.0	4.0	2.5		4.5		4.0		ns	2
t_{s3}	Setup Time, D to STB ↑	5.0	0.0	−2.0		0.0		0.0		ns	2
t_{s4}	Setup Time, STB ↑ to SCK ↓	5.0	7.0	5.0		7.5		7.0		ns	4–7
t_W	Clock Pulse Width SCK (L)	5.0	19.5	12.0		20.0		19.5		ns	4, 6
	SCK (H)		18.5	14.0		20.0		18.5			
t_{W1}	Pulse Width STB (H or L)	5.0	5.5	2.0		6.0		5.5		ns	4, 6
f_{max}	Maximum Frequency Clock	5.0	25	35		25		25		MHz	

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Electrical Characteristics/Operating Requirements (Continued)

Symbol	Parameter	V_{CC}* (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF			Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
SERIAL SCAN INTERFACE (SSI)											
t_{pd5}	Prop Delay SCK to TCK	5.0	3.0	8.0	11.0	3.0	14.0	3.0	12.0	ns	15
t_{pd6}	Prop Delay SCK to TDO	5.0	5.5	12.0	16.0	5.5	19.5	5.5	17.5	ns	15
t_{pd7}	Prop Delay SCK to TMS	5.0	4.5	11.0	14.5	4.5	18.5	4.5	15.5	ns	15
t_{pd8}	Prop Delay FRZ to TCK	5.0	3.0	8.0	10.5	3.0	13.5	3.0	11.5	ns	15
t_{en4}	Enable Time $\overline{OE}$ to JTAG	5.0	2.0	7.0	10.0	2.0	13.0	2.0	11.0	ns	14
t_{dis4}	Disable Time $\overline{OE}$ to JTAG	5.0	1.0	6.0	9.0	2.0	11.0	1.0	10.0	ns	14
t_{h5}	Hold Time, H or L TDI to SCK (Note 1)	5.0	0.5	−1.5		0.5		0.5		ns	15
			0.0	−2.0		0.0		0.0			15
t_{s5}	Setup Time, H or L TDI to SCK (Note 1)	5.0	5.0	3.0		5.5		5.0		ns	15
			6.5	3.5		7.5		6.5			15
RST RELATED TIMING											
t_{pd}	Prop Delay $\overline{RST}$ to D	5.0	8.0	17.5	24.0	8.0	29.5	8.0	25.5	ns	
t_{pd}	Prop Delay $\overline{RST}$ to $\overline{RDY}$	5.0	8.0	19.5	25.5	8.0	31.0	8.0	28.0	ns	
t_{phl}	Prop Delay $\overline{RST}$ to INT	5.0	7.0	16.5	24.5	7.0	28.0	7.0	24.5	ns	
t_{plh}	Prop Delay $\overline{RST}$ to TDO	5.0	5.5	12.5	17.0	5.5	21.0	5.5	18.5	ns	
t_{plh}	Prop Delay $\overline{RST}$ to TMS	5.0	5.5	12.0	16.0	5.5	20.0	5.5	17.5	ns	
t_{WR}	Pulse Width $\overline{RST}$ (L)	5.0	6.0	4.0		6.5		6.0		ns	
t_{REC}	Recovery Time SCK from $\overline{RST}$	5.0	1.0	−0.5		1.0		1.0		ns	

Note 1: SSC Mode

*Voltage Range 5.0 is 5.0V ±0.5V.

Application Note

SCK MINIMUM PULSE WIDTH CALCULATION

The SCANPSC100 Parallel to Serial Converter is intended to act as the interface between a processor and an IEEE 1149.1 boundary scan chain. When used in this configuration, there is a critical timing situation that is not obvious. This timing involves the system clock rate at which data from the scan ring is being read into the 'PSC100's TDI pin (target TAP controllers in SHIFT-DR or SHIFT-IR states).

To fully understand the events which are taking place during this critical period, it is useful to view the waveforms of interest as they relate in time. See *Figure 16*. The TCK is derived internally to the 'PSC100 based on the system clock (SCK) and clock gating control. The result is that when TCK is running, it is at the same frequency as SCK but delayed in time by the SCK-TCK propagation delay.

The TCK signal from the 'PSC100 drives all of the IEEE 1149.1 target devices. On the rising edge of TCK, data present at each scan cell is clocked into it. On the falling edge, this data is presented at the output of the same scan cell for the next adjacent cell to read. With regards to the last cell in a particular target, the falling edge of TCK presents the data in the last scan cell to the TDO pin, a TCK-TDO propagation delay later.

At the 'PSC100, data shifted in through the TDI pin is clocked in on the rising edge of SCK, not TCK. The reason for this is that TCK is generated internal to the 'PSC100 and intended to control the boundary scan targets. The 'PSC100 is controlled by SCK, therefore the signal to be shifted into the TDI pin needs to be referenced to SCK not TCK. New TDI data must be present a TDI-SCK set-up time prior to the rising edge of SCK in order to guarantee validity. Although SCK is usually continuous, the TDI buffer is controlled by a SHIFT-ENABLE signal which is generated internal to the 'PSC100, based on the status of the TDI buffer and the Mode Registers.

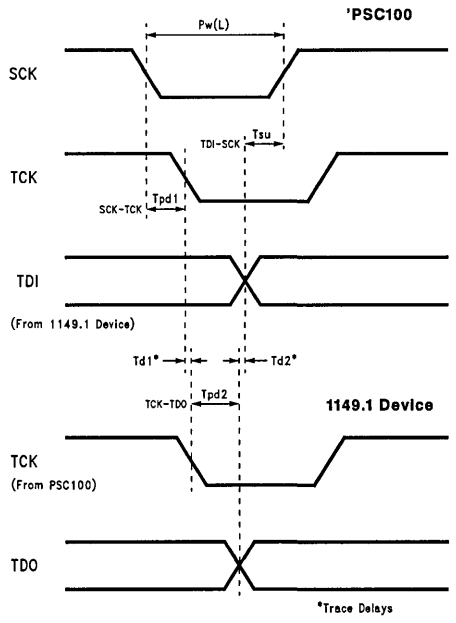
We now see the three major timing components which limit the duration of the SCK pulse width low. There are two minor additional delays which should be noted. The TCK signal from the 'PSC100 needs to arrive at the target device to be recognized, and this takes a finite amount of time depending on the signal trace length and impedance. Similarly, the TDO signal of the last target in the chain needs to reach the TDI pin of the 'PSC100, taking a finite amount of time as well. These two trace delays can be minimized by making the target device closest to the 'PSC100 the last device in the chain. See *Figure 17*.

PROGRAMMING RESTRICTIONS

Because certain mode bits enable shift operations for certain functions, these mode bits should not be changed when shift operations are in progress. The alignment of all registers during shift operations is controlled by a three bit counter in the TCK control block. Enabling or disabling a function in the middle of a shift operation may disrupt the logic necessary to keep all shifter/buffers byte-aligned. For example, if the TDO shifter/buffer (already loaded) is enabled while the three bit counter value is three, the shifter/buffer will only shift out 5 bits of the first byte loaded.

The following bits should not be changed when shift operations are in progress, i.e., when TCK is enabled (see TCK control section):

- MODE0(7:3)
- MODE1(4:3)
- MODE2(0)



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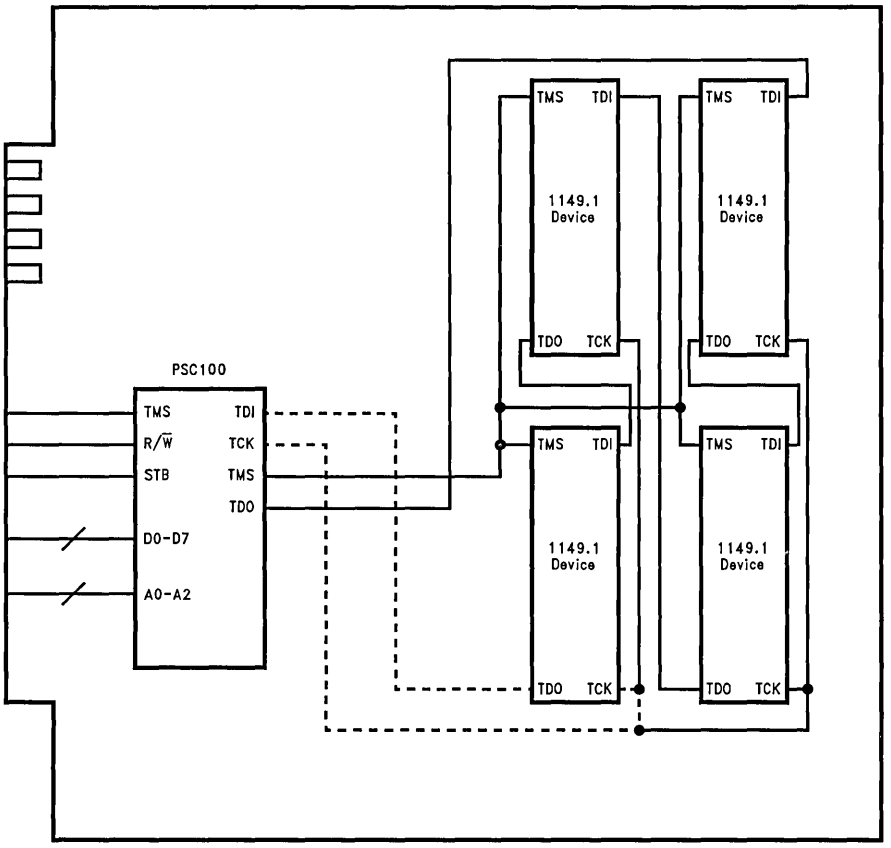
Pw(L) minimum = Tpd1 + Td1 + Tpd2 + Td2 + Tsu

FIGURE 16. System Clock Timing for Accurate TDI Data



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Note: – – – – – Minimize the lengths of these two traces.

FIGURE 17. SCANPSC100 Location Relative to Targets

National Semiconductor

SCANPSC110F SCAN Bridge Hierarchical and Multidrop Addressable JTAG Port (IEEE1149.1 System Test Support)

General Description

The SCANPSC110F Bridge extends the IEEE Std. 1149.1 test bus into a multidrop test bus environment. The advantage of a hierarchical approach over a single serial scan chain is improved test throughput and the ability to remove a board from the system and retain test access to the remaining modules. Each SCANPSC110F Bridge supports up to 3 local scan rings which can be accessed individually or combined serially. Addressing is accomplished by loading the instruction register with a value matching that of the Slot inputs. Backplane and inter-board testing can easily be accomplished by parking the local TAP Controllers in one of the stable TAP Controller states via a Park instruction. The 32-bit TCK counter enables built in self test operations to be performed on one port while other scan chains are simultaneously tested.

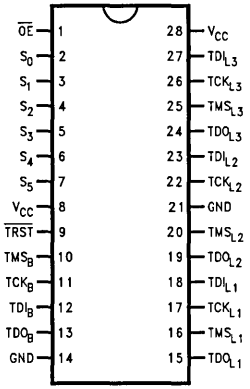
Features

- True IEEE1149.1 hierarchical and multidrop addressable capability
- The 6 slot inputs support up to 59 unique addresses, a Broadcast Address, and 4 Multi-cast Group Addresses
- 3 IEEE 1149.1-compatible configurable local scan ports
- Mode Register allows local TAPs to be bypassed, selected for insertion into the scan chain individually, or serially in groups of two or three
- 32-bit TCK counter
- 16-bit LFSR Signature Compactor
- Local TAPs can be tri-stated via the $\overline{OE}$ input to allow an alternate test master to take control of the local TAPs

Ordering Code: See Section 11

Connection Diagrams

28-Pin SOIC, CDIP and Flatpak



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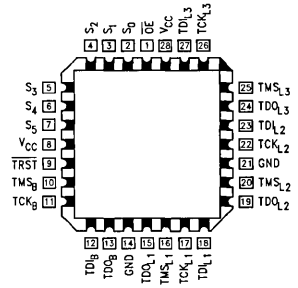
Order Number	Description
SCANPSC110FSC	SOIC in Tubes
SCANPSC110FSCX	SOIC in Table and Reel
SCANPSC110FFMQB	Military Flatpak
SCANPSC110FDMQB	Military DIP
SCANPSC110FLMQB	Military Leadless Chip Carrier

Pin Assignment for LCC



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Pin Names	Description
TCK_B	Backplane Test Clock Input
TMS_B	Backplane Test Mode Select Input
TDI_B	Backplane Test Data Input
TDO_B	Backplane Test Data Output
$\overline{TRST}$	Asynchronous Test Reset Input (Active low)
$S_{(0,5)}$	Address Select Port
$\overline{OE}$	Local Scan Port Output Enable (Active low)
$TCK_{L(1-3)}$	Local Port Test Clock Output
$TMS_{L(1-3)}$	Local Port Test Mode Select Output
$TDI_{L(1-3)}$	Local Port Test Data Input
$TDO_{L(1-3)}$	Local Port Test Data Output

Table of Contents

TABLE I. Glossary of Terms

LFSR	Linear Feedback Shift Register. When enabled, will generate a 16-bit signature of sampled serial test data.
LSP	Local Scan Port. A four signal port that drives a "local" (i.e. non-backplane) scan chain. (e.g., TCK_{L1}, TMS_{L1}, TDO_{L1}, TDI_{L1})
Local	Local is used to describe IEEE Std. 1149.1 compliant scan rings and the SCANPSC110F Bridge Test Access Port that drives them. The term "local" was adopted from the system test architecture that the 'PSC110F Bridge will most commonly be used in; namely, a system test backplane with a 'PSC110F Bridge on each card driving up to 3 "local" scan rings per card. (Each card can contain multiple 'PSC110Fs, with 3 local scan ports per 'PSC110F.)
Park/Unpark	Park, parked, unpark, and unparked, are used to describe the state of the LSP controller and the state of the local TAP controllers (the "local TAP controllers" refers to the TAP controllers of the scan components that make up a local scan ring). Park is also used to describe the action of parking a LSP (transitioning into one of the Parked LSP controller states). It is important to understand that when a LSP controller is in one of the parked states, TMS_L is held constant, thereby holding or "parking" the local TAP controllers in a given state.
TAP	Test Access Port as defined by IEEE Std. 1149.1
Selected/Unselected	Selected and Unselected refers to the state of the 'PSC110F Bridge Selection Controller. A selected 'PSC110F has been properly addressed and is ready to receive Level 2 protocol. Unselected 'PSC110Fs monitor the system test backplane, but do not accept Level 2 protocol (except for the *GOTOWAIT* instruction). The data registers and LSPs of unselected 'PSC110Fs are not accessible from the system test master.
Active Scan Chain	The Active Scan Chain refers to the scan chain configuration as seen by the test master at a given moment. When a 'PSC110F is selected with all of its LSPs parked, the active scan chain is the current scan bridge register only. When a LSP is unparked, the active scan chain becomes: TDI_B → the current 'PSC110F register → the local scan ring registers → a PAD bit → TDO_B. Refer to Table IV for Unparked configurations of the LSP network.
Level 1 Protocol	Level 1 is the protocol used to address a 'PSC110F.
Level 2 Protocol	Level 2 is the protocol that is used once a 'PSC110F is selected. Level 2 protocol is IEEE Std. 1149.1 compliant when an individual 'PSC110F is selected.
PAD	A one bit register that is placed at the end of each local scan port scan-chain. The PAD bit eliminates the prop delay that would be added by the 'PSC110F LSPN logic between TDI_{Ln} and $TDO_{L(n+1)}$ or TDO_B by buffering and synchronizing the TDI_L inputs to the falling edge of TCK_B, thus allowing data to be scanned at higher frequencies without violating set-up and hold times.
LSB	Least Significant Bit, the right-most position in a register (bit 0)
MSB	Most Significant Bit, the left-most position in a register

TABLE II. Detailed Pin Description Table

Name	I/O*	Pin # (SOIC & LCC)	Description
TMS_B	TTL Input w/Pull-Up Resistor	10	**BACKPLANE TEST MODE SELECT:** Controls sequencing through the TAP Controller of the SCANPSC110F Bridge. Also controls sequencing of the TAPs which are on the three (3) local scan chains.
TDI_B	TTL Input w/Pull-Up Resistor	12	**BACKPLANE TEST DATA INPUT:** All backplane scan data is supplied to the 'PSC110F through this input pin.
TDO_B	TRI-STATEable, 32 mA/64 mA Drive, Reduced-Swing, Output	13	**BACKPLANE TEST DATA OUTPUT:** This output drives test data from the 'PSC110F and the local TAPs, back toward the scan master controller.
TCK_B	TTL Schmitt Trigger Input	11	**TEST CLOCK INPUT FROM THE BACKPLANE:** This is the master clock signal that controls all scan operations of the 'PSC110F and of the three (3) local scan ports.
$\overline{TRST}$	TTL Input w/Pull-Up Resistor	9	**TEST RESET:** An asynchronous reset signal (active low) which initializes the 'PSC110F logic.
$S_{(0-5)}$	TTL Inputs	2, 3, 4, 5, 6, 7	**SLOT IDENTIFICATION:** The configuration of these six (6) pins is used to identify (assign a unique address to) each 'PSC110F on the system backplane.
$\overline{OE}$	TTL Input	1	**OUTPUT ENABLE for the Local Scan Ports, active low.** When high, this active-low control signal TRI-STATEs all three local scan ports on the 'PSC110F, to enable an alternate resource to access one or more of the three (3) local scan chains.
$TDO_{L(1-3)}$	TRI-STATEable, 24 mA/24 mA Drive Outputs	15,19, 24	**TEST DATA OUTPUTS:** Individual output for each of the three (3) local scan ports.
$TDI_{L(1-3)}$	TTL Inputs w/Pull-Up Resistors	18, 23, 27	**TEST DATA INPUTS:** Individual scan data input for each of the three (3) local scan ports.
$TMS_{L(1-3)}$	TRI-STATEable, 24 mA/24 mA Drive Outputs	16, 20, 25	**TEST MODE SELECT OUTPUTS:** Individual output for each of the three (3) local scan ports. TMS_L does **not** provide a pull-up resistor (which is assumed to be present on a connected TMS input, per the IEEE 1149.1 requirement)
$TCK_{L(1-3)}$	TRI-STATEable, 24 mA/24 mA Drive Output	17, 22, 26	**LOCAL TEST CLOCK OUTPUTS:** Individual output for each of the three (3) local scan ports. These are buffered versions of TCK_B.
V_{CC}	Power Supply Voltage	8, 28	**Power supply pins, 5.0V ± 10%.**
GND	Ground potential	14, 21	**Power supply pins 0V.**

*All pins are active HIGH unless otherwise noted.

Overview of SCANPSC110F Bridge Functions

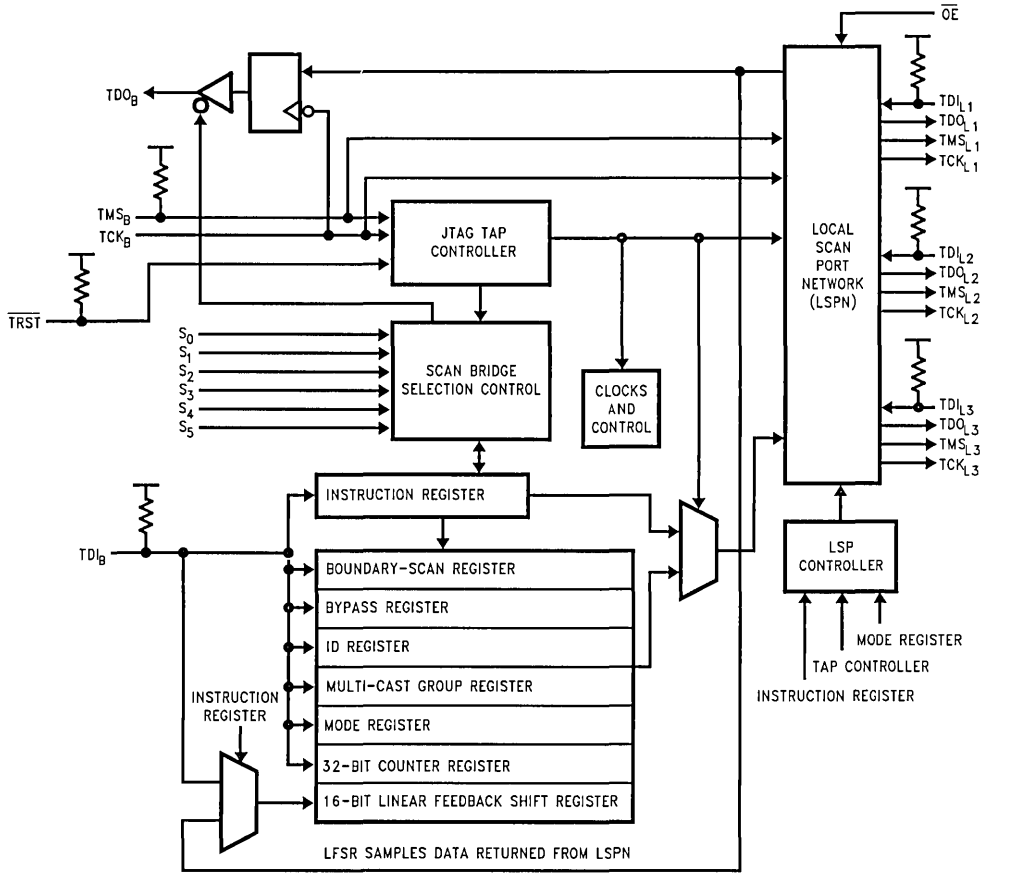

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FIGURE 1. SCANPSC110F Bridge Architecture

SCANPSC110F BRIDGE ARCHITECTURE

Figure 1 shows the basic architecture of the 'PSC110F. The device's major functional blocks are illustrated here. The TAP Controller, a 16-state state machine, is the central control for the device. The instruction register and various test data registers can be scanned to exercise the various functions of the 'PSC110F (these registers behave as defined in IEEE Std. 1149.1).

The 'PSC110F selection controller provides the functionality that allows the 1149.1 protocol to be used in a multi-drop environment. It primarily compares the address input to the slot identification and enables the 'PSC110F for subsequent scan operations.

The Local Scan Port Network (LSPN) contains multiplexing logic used to select different port configurations. The LSPN control block contains the Local Scan Port Controllers (LSPC) for each Local Scan Port (LSP_1, LSP_2, and LSP_3). This control block receives input from the 'PSC110F instruction register, mode register, and the TAP controller. Each local port contains all four (4) boundary scan signals needed to interface with the local TAPs.

SCANPSC110F BRIDGE STATE MACHINES

The 'PSC110F is IEEE 1149.1-compatible, in that it supports all required 1149.1 operations. In addition, it supports a higher level of protocol, (Level 1), that extends the IEEE 1149.1 Std. to a multi-drop environment.

In multi-drop scan systems, a scan tester can select individual 'PSC110Fs for participation in upcoming scan operations. 'PSC110F "selection" is accomplished by simultaneously scanning a device address out to multiple 'PSC110Fs. Through an on-chip address matching process, only those 'PSC110Fs whose statically-assigned address matches the scanned-out address become selected to receive further instructions from the scan tester. 'PSC110F selection is done using a "Level-1" protocol, while follow-on instructions are sent to selected 'PSC110Fs by using a "Level-2" protocol.

Overview of SCANPSC110F Bridge Functions (Continued)

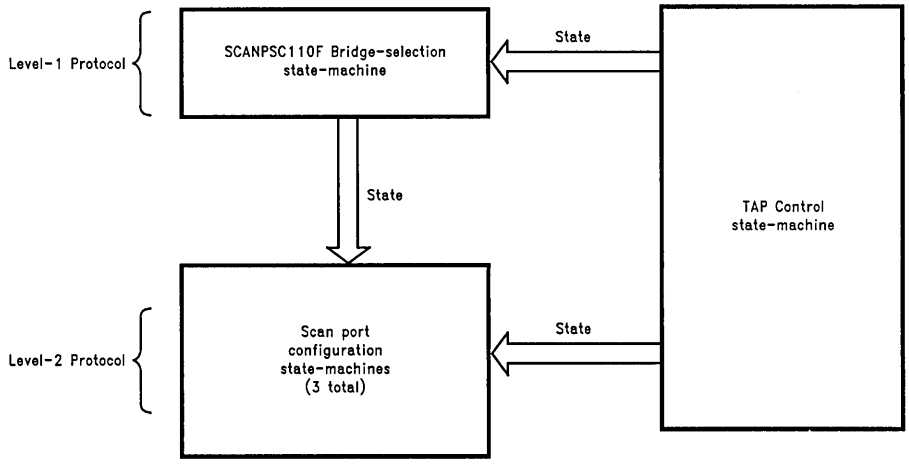

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FIGURE 2. SCANPSC110F Bridge State Machines

The 'PSC110F contains three distinct but coupled state-machines (see *Figure 2*). The first of these is the TAP-control state-machine, which is used to drive the 'PSC110Fs scan ports in conformance with the 1149.1 Standard (see *Figure 17* of appendix). The second is the 'PSC110F-selection state-machine *(Figure 3)*. The third state-machine actually consists of three identical but independent state-machines (see *Figure 4*), one per 'PSC110F local scan port. Each of these scan port-selection state-machines allows individual local ports to be inserted into and removed from the 'PSC110Fs overall scan chain.

The 'PSC110F selection state-machine performs the address matching which gives the 'PSC110F its multi-drop capability. That logic supports single-'PSC110F access, multicast, and broadcast. The 'PSC110F-selection state-machine implements the chip's Level-1 protocol.

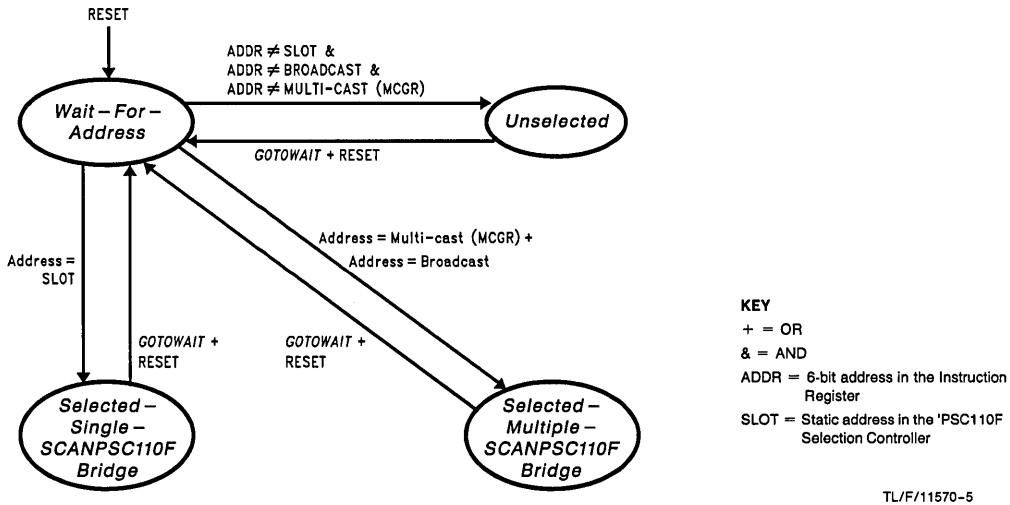

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FIGURE 3. State Machine for SCANPSC110F Bridge Selection Controller

Overview of SCANPSC110F Bridge Functions (Continued)

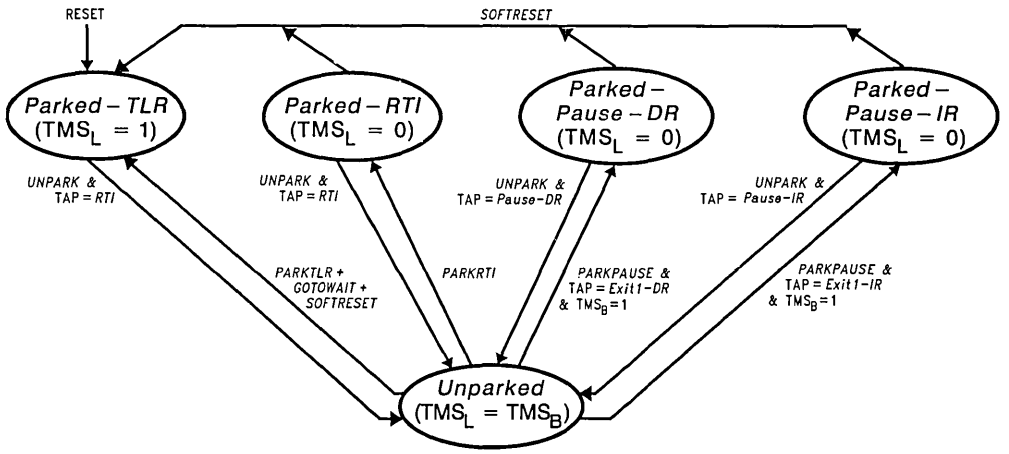

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FIGURE 4. Local SCANPSC110F Bridge Port Configuration State Machine

The 'PSC110F's scan port-configuration state-machine is used to control the insertion of local scan ports into the overall scan chain, or the isolation of local ports from the chain. From the perspective of a system's (single) scan controller, each 'PSC110F presents only one scan chain to the master. The 'PSC110F architecture allows one or more of the 'PSC110F's local ports to be included in the active scan chain.

Each local port can be "parked" in one of four stable states *(Parked-TLR, Parked-RTI, Parked-Pause-DR or Parked-Pause-IR)*, either individually or simultaneously with other local ports. Parking a chain removes that local chain from the active scan chain. Conversely, a parked chain can be "unparked", causing the corresponding local port to be inserted into the active scan chain.

As shown in *Figure 4*, the 'PSC110F's three scan port-configuration state-machines allow each of the part's local ports to occupy a different state at any given time. For example, some ports may be parked, perhaps in different states, while other ports participate in scan operations. The state-diagram shows that some state transitions depend on the current state of the TAP-control state-machine. As an example, a local port which is presently in the *Parked-RTI* state does not become unparked (i.e., enter the *Unparked* state) until the 'PSC110F receives an *UNPARK* instruction **and** the 'PSC110F's TAP state-machine enters the *Run-Test/Idle* state.

Similarly, certain transitions of the scan port-configuration state-machine can force the 'PSC110F's TAP-control state-machine into specific states. For example, when a local port is in the *Unparked* state and the 'PSC110F receives a *PARKRTI* instruction, the Local Port controller enters the *Parked-RTI* state in which TMS_{Ln} will be held low until the port is later unparked. While TMS_{Ln} is held low, all devices on that local scan chain remain in their current TAP State (the *RTI* TAP controller state in this example).

The 'PSC110F's scan port-configuration state-machine implements part of the 'PSC110F's Level-2 protocol. In addition, the 'PSC110F provides a number of Level-2 instructions for functions other than local scan port confguration. These instructions provide access to and control of various registers within the 'PSC110F. This set instructions includes:

BYPASS	*CNTRSEL*
EXTEST	*LFSRON*
SAMPLE/PRELOAD	*LFSROFF*
IDCODE	*CNTRON*
MODESEL	*CNTROFF*
MCGRSEL	*GOTOWAIT*
LFSRSEL	

Figure 5 illustrates how the 'PSC110F's state-machines interact. The 'PSC110F-selection state-machine enables or disables operation of the chip's three port-selection state-machines. In 'PSC110Fs which are selected via Level-1 protocol (either as individual 'PSC110Fs or as members of broadcast or multi-cast groups), Level-2 protocol commands can be used to park or unpark local scan ports. Note that most transitions of the port-configuration state-machines are gated by particular states of the 'PSC110F's TAP-control state-machine, as shown in *Figures 4* and *5*.

Overview of SCANPSC110F Bridge Functions (Continued)

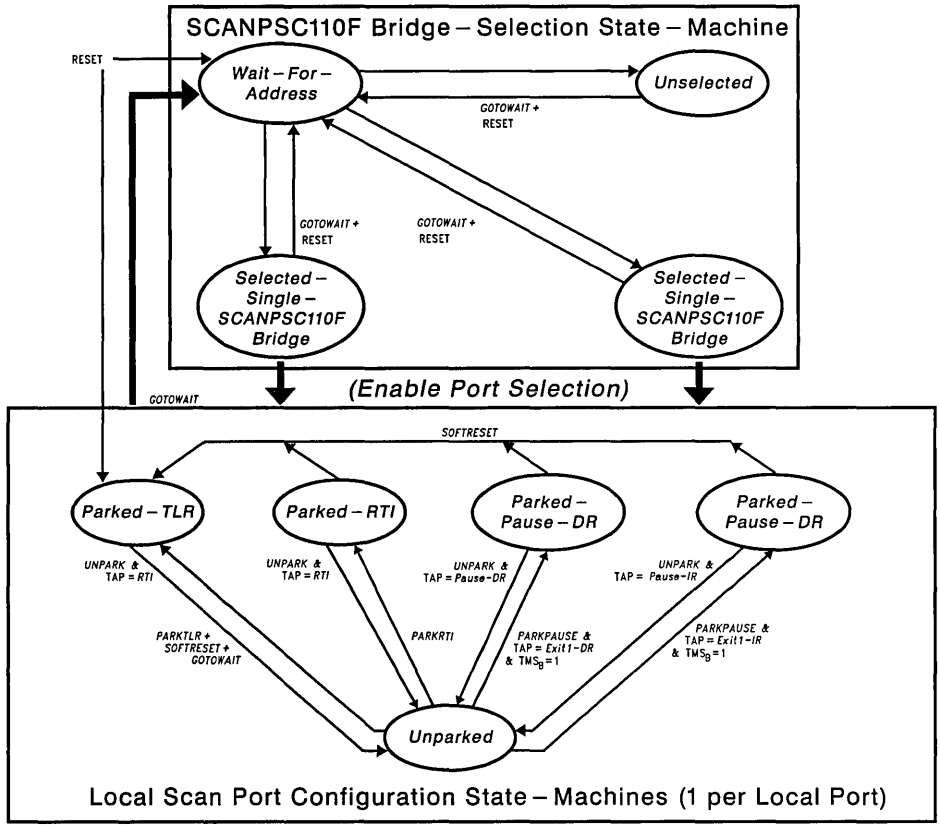

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FIGURE 5. Relationship Between SCANPSC110F Bridge State Machines

Following a hardware reset, the TAP controller state-machine is in the *Test-Logic-Reset (TLR)* state; the 'PSC110F-selection state-machine is in the *Wait-For-Address* state; and each of the three port-selection state-machines is in the *Parked-TLR* state. The 'PSC110F is then ready to receive Level-1 protocol, followed by Level-2 protocol.

Tester/SCANPSC110F Bridge Interface

An IEEE 1149.1 system tester sends instructions to a 'PSC110F via that 'PSC110F's backplane scan-port. Following test logic reset, the 'PSC110F's selection state-machine is in the *Wait-For-Address* state. When the 'PSC110F's TAP controller is sequenced to the Shift-IR state, data shifted in through the TDI_B input is shifted into the 'PSC110F's instruction register. Note that prior to successful selection of a 'PSC110F, data is not shifted out of the instruction register and out through the 'PSC110F's TDO_B output, as it is during normal scan operations. Instead, as each new bit enters the instruction register's most-significant bit, data shifted out from the least-significant bit is discarded.

When the instruction register is updated with the address data, the 'PSC110F's address-recognition logic compares the six least-significant bits of the instruction register with the 6-bit assigned address which is statically present on the $S_{(0-5)}$ inputs. Simultaneously, the scanned-in address is compared with the reserved Broadcast and Multi-cast addresses. If an address match is detected, the 'PSC110F-selection state-machine enters one of the two selected states. If the scanned address does not match a valid single-slot address or one of the reserved broadcast/multi-cast addresses, the 'PSC110F-selection state-machine enters the *Unselected* state.

Note that the SLOT inputs *should not be set* to a value corresponding to *a multi-cast group*, or to the *broadcast address*. Also note that the single-'PSC110F selection process must be performed for all 'PSC110Fs which are subsequently to be addressed in multi-cast mode. This is required because each such device's Multi-cast Group Register (MCGR) must be programmed with a multi-cast group number, and the MCGR is not accessible to the test controller until that 'PSC110F has first entered the *Selected-Single-'PSC110F* state.

Once a 'PSC110F has been selected, Level-2 protocol is used to issue commands and to access the chip's various registers.

Register Set

The SCANPSC110F Bridge includes a number of registers which are used for 'PSC110F selection and configuration, scan data manipulation, and scan-support operations. These registers can be grouped as shown in Table III.

The specific fields and functions of each of these registers are detailed in the section of this document titled "Data Register Descriptions".

Note that when any of these registers is selected for insertion into the 'PSC110F's scan-chain, scan data enters through that register's most-significant bit. Similarly, data that is shifted out of the register is fed to the scan input of the next-downstream device in the scan-chain.

TABLE III. Registers

Register Name	BSDL Name	Description
Instruction Register	INSTRUCTION	'PSC110F addressing and instruction-decode IEEE Std. 1149.1 required register
Boundary-Scan Register	BOUNDARY	IEEE Std. 1149.1 required register
Bypass Register	BYPASS	IEEE Std. 1149.1 required register
Device Identification Register	IDCODE	IEEE Std. 1149.1 optional register
Multi-Cast Group Register	MCGR	'PSC110F-group address assignment
Mode Register	MODE	'PSC110F local-port configuration and control bits
Linear-Feedback Shift Register	LFSR	'PSC110F scan-data compaction (signature generation)
TCK Counter Register	CNTR	Local-port TCK clock-gating (for BIST)

Addressing Scheme

The SCANPSC110F Bridge architecture extends the functionality of the IEEE 1149.1 Standard by supplementing that protocol with an addressing scheme which allows a test controller to communicate with specific 'PSC110Fs within a network of 'PSC110Fs. That network can include both multi-drop and hierarchical connectivity. In effect, the 'PSC110F architecture allows a test controller to dynamically select specific portions of such a network for participation in scan operations. This allows a complex system to be partitioned into smaller blocks for testing purposes.

The 'PSC110F provides two levels of test-network partitioning capability. First, a test controller can select entire individual 'PSC110Fs, specific sets of 'PSC110Fs (multi-cast groups), or all 'PSC110Fs (broadcast). This 'PSC110F-selection process is supported by a "Level-1" communication protocol. Second, within each selected 'PSC110F, a test controller can select one or more of the chip's three local scan-ports. That is, individual local ports can be selected for inclusion in the (single) scan-chain which a 'PSC110F presents to the test controller. This mechanism allows a controller to select specific terminal scan-chains within the overall scan network. The port-selection process is supported by a "Level-2" protocol.

Hierarchical Test Support

Multiple SCANPSC110F Bridges can be used to assemble a hierarchical boundary-scan tree. In such a configuration, the system tester can configure the local ports of a set of 'PSC110Fs so as to connect a specific set of local scan-chains to the active scan chain. Using this capability, the tester can selectively communicate with specific portions of a target system.

The tester's scan port is connected to the backplane scan port of a "root" layer of 'PSC110Fs, each of which can be selected using multi-drop addressing. A second tier of 'PSC110Fs can be connected to this root layer, by connecting a local port (LSP) of a root-layer 'PSC110F to the backplane port of a second-tier 'PSC110F. This process can be continued to construct a multi-level scan hierarchy.

'PSC110F local ports which are not cascaded into higher-level 'PSC110Fs can be thought of as the terminal "leaves" of a scan "tree". The test master can select one or more target leaves by selecting and configuring the local ports of an appropriate set of 'PSC110Fs in the test tree.

Level 1 Protocol

ADDRESSING MODES

The SCANPSC110F Bridge supports "single" and "multiple" modes of addressing a 'PSC110F. The "single" mode will select one 'PSC110F and is called Direct Addressing. More than one 'PSC110F device can be selected via the Broadcast and Multi-Cast Addressing modes.

TABLE IV. SCANPSC110F Bridge Address Modes

Address Types	Hex Address*	Binary Address**	TDO_B State
Direct Address	00 to 3A	XX000000 to XX111010	Normal IEEE Std. 1149.1
Broadcast Address	3B	XX111011	Always TRI-STATED
Multi-Cast Group 0	3C	XX111100	Always TRI-STATED
Multi-Cast Group 1	3D	XX111101	Always TRI-STATED
Multi-Cast Group 2	3E	XX111110	Always TRI-STATED
Multi-Cast Group 3	3F	XX111111	Always TRI-STATED

* Hex address '7X', 'BX', or 'FX' may be used instead of '3X'.

** Only the six (6) LSB's of the address is compared to the $S_{(0-5)}$ inputs. The two (2) MSB's are "don't cares".

DIRECT ADDRESSING

The 'PSC110F enters the *Wait-For-Address* state when:

1. its TAP Controller enters the *Test-Logic-Reset* state, or
2. its instruction register is updated with the *GOTOWAIT* instruction (while either selected or unselected).

Each 'PSC110F within a scan network must be statically configured with a unique address via its $S_{(0-5)}$ inputs. While the 'PSC110F controller is in the *Wait-For-Address* state, data shifted into bits 5 through 0 of the instruction register is compared with the address present on the $S_{(0-5)}$ inputs in the *Update-IR* state. If the six (6) LSBs of the instruction register match the address on the $S_{(0-5)}$ inputs, (see *Figure 6*) the 'PSC110F becomes selected, and is ready to receive Level 2 Protocol (i.e., further instructions). When the 'PSC110F is selected, its device identification register is inserted into the active scan chain.

All 'PSC110Fs whose $S_{(0-5)}$ address does not match the instruction register address become unselected. They will remain unselected until either their TAP Controller enters the *Test-Logic-Reset* state, or their instruction register is updated with the *GOTOWAIT* instruction.

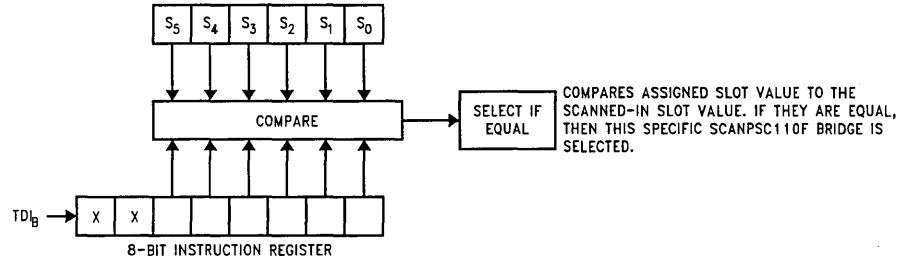

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FIGURE 6. Direct Addressing: Device Address Loaded Into Instruction Register

Level 1 Protocol (Continued)

BROADCAST ADDRESSING

The Broadcast Address allows a tester to simultaneously select all 'PSC110Fs in a test network. This mode is useful in testing systems which contain multiple identical boards. To avoid bus contention between scan-path output drivers on different boards, each 'PSC110F's TDO_B buffer is always tri-stated while in Broadcast mode. In this configuration, the on-chip Linear Feedback Shift Register (LFSR) can be used to accumulate a test result signature for each board that can be read back later by direct-addressing each board's 'PSC110F.

MULTI-CAST ADDRESSING

As a way to make the broadcast mechanism more selective, the 'PSC110F provides a "Multi-cast" addressing mode. A 'PSC110F's multi-cast group register (MCGR) can be programmed to assign that 'PSC110F to one of four (4) Multi-Cast groups. When 'PSC110Fs in the *Wait-For-Address* state are updated with a Multi-Cast address, all 'PSC110Fs whose MCGR matches the Multi-Cast group will become selected. As in Broadcast mode, TDO_B is always tri-stated while in Multi-cast mode.

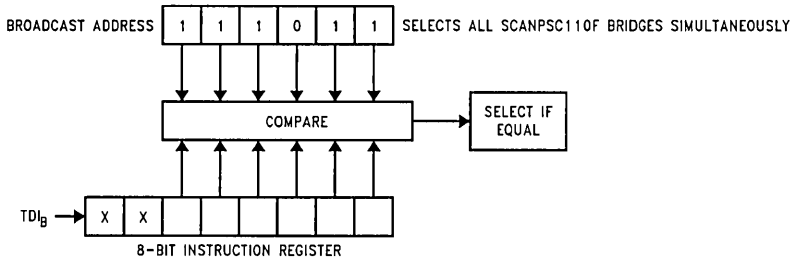

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FIGURE 7. Broadcast Addressing: Address Loaded into Instruction Register

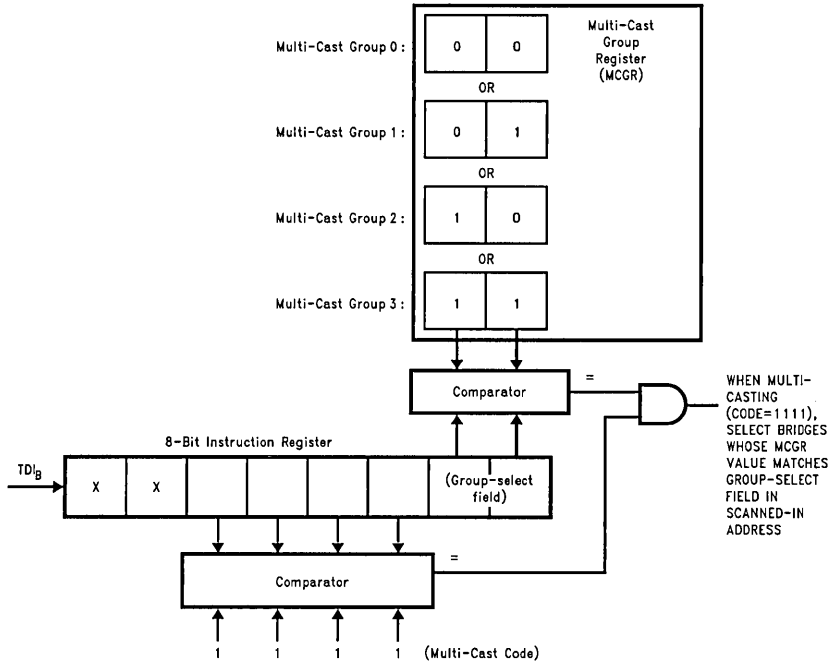

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FIGURE 8. Multi-Cast Addressing: Address Loaded into Instruction Register

Level 2 Protocol

Once the SCANPSC110F Bridge has been successfully addressed and selected, its internal registers may be accessed via Level-2 Protocol. Level-2 Protocol is compliant to IEEE Std. 1149.1 TAP protocol with one exception: if the 'PSC110F is selected via the Broadcast or Multi-Cast address, TDO_B will always be TRI-STATED. (The TDO_B buffer must be implemented this way to prevent bus contention.)

Upon being selected, (i.e., the 'PSC110F Selection controller transitions from the *Wait-For-Address* state to one of the *Selected* states), each of the local scan ports (LSP_1, LSP_2, LSP_3) remains parked in one of the following four TAP Controller states: *Test-Logic-Reset, Run-Test/Idle, Pause-DR*, or *Pause-IR* and the active scan chain will consist of: TDI_B through the instruction register (or the IDCODE register) and out through TDO_B.

$$TDI_B \longrightarrow \text{Instruction Register} \longrightarrow TDO_B$$

The *UNPARK* instruction (described later) is used to insert one or more local scan ports into the active scan chain. Table IV describes which local ports are inserted into the chain, and in what order.

LEVEL 2 INSTRUCTION TYPES

There are two types of instructions (reference Table V):

1. Instructions that insert a 'PSC110F register into the active scan chain so that the register can be captured or updated *(BYPASS, SAMPLE/PRELOAD, EXTEST, IDCODE, MODESEL, MCGRSEL, LFSRSEL, CNTRSEL).*
2. Instructions that configure local ports or control the operation of the linear feedback shift register and counter registers *(UNPARK, PARKTRL, PARKRTI, PARKPAUSE, GOTOWAIT, SOFTRESET, LFSRON, LFSROFF, CNTRON, CNTROFF).* These instructions, along with any other yet undefined Op-Codes, will cause the device identification register to be inserted into the active scan chain.

LEVEL 2 INSTRUCTION DESCRIPTIONS

BYPASS: The *BYPASS* instruction selects the bypass register for insertion into the active scan chain when the 'PSC110F is selected.

EXTEST: The *EXTEST* instruction selects the boundary-scan register for insertion into the active scan chain. The boundary-scan register consists of seven "sample only" shift cells connected to the $S_{(0-5)}$ and $\overline{OE}$ inputs. On the 'PSC110F, the *EXTEST* instruction performs the same function as the *SAMPLE/PRELOAD* instruction, since there aren't any scannable outputs on the device.

SAMPLE/PRELOAD: The *SAMPLE/PRELOAD* instruction selects the boundary-scan register for insertion into the active scan chain. The boundary-scan register consists of seven "sample only" shift cells connected to the $S_{(0-5)}$ and $\overline{OE}$ inputs.

IDCODE: The *IDCODE* instruction selects the device identification register for insertion into the active scan chain. When *IDCODE* is the current active instruction the device identification "0FC0E01F" Hex is captured upon exiting the *Capture-DR* state.

TABLE V. Level 2 Protocol and Op-Codes

Instructions	Hex Op-Code	Binary Op-Code	Data Register
BYPASS	FF	11111111	Bypass Register
EXTEST	00	00000000	Boundary-Scan Register
SAMPLE/PRELOAD	81	10000001	Boundary-Scan Register
IDCODE	AA	10101010	Device Identification Register
UNPARK	E7	11100111	Device Identification Register
PARKTLR	C5	11000101	Device Identification Register
PARKRTI	84	10000100	Device Identification Register
PARKPAUSE	C6	11000110	Device Identification Register
*GOTOWAIT**	C3	11000011	Device Identification Register
MODESEL	8E	10001110	Mode Register
MCGRSEL	03	00000011	Multi-Cast Group Register
SOFTRESET	88	10001000	Device Identification Register
LFSRSEL	C9	11001001	Linear Feedback Shift Register
LFSRON	0C	00001100	Device Identification Register
LFSROFF	8D	10001101	Device Identification Register
CNTRSEL	CE	11001110	32-Bit TCK Counter Register
CNTRON	0F	00001111	Device Identification Register
CNTROFF	90	10010000	Device Identification Register
Other Undefined	TBD	TBD	Device Identification Register

*The *GOTOWAIT* instruction returns both selected and unselected 'PSC110Fs to the *Wait-For-Address* state. All other instructions act on selected 'PSC110Fs only.

Level 2 Protocol (Continued)

UNPARK: This instruction unparks the Local Scan Port Network and inserts it into the active scan chain as configured by the Mode register (see Table IV). Unparked LSPs are sequenced synchronously with the 'PSC110F's TAP controller.

When a LSP has been parked in the *Test-Logic-Reset* or *Run-Test/Idle* state, it will not become unparked until the 'PSC110F's TAP Controller enters the *Run-Test/Idle* state following the *UNPARK* instruction. If an LSP has been parked in one of the stable pause states (*Pause-DR* or *Pause-IR*), it will not become unparked until the 'PSC110F's TAP Controller enters the respective pause state. (See *Figures 9, 10, 11,* and *12).*

PARKTLR: This instruction causes all unparked LSPs to be parked in the *Test-Logic-Reset* TAP controller state and removes the LSP network from the active scan chain. The LSP controllers keep the LSPs parked in the *Test-Logic-Reset* state by forcing their respective TMS_L output with a constant logic "1" while the LSP controller is in the *Parked-TLR* state (see *Figure 4*).

PARKRTI: This instruction causes all unparked LSPs to be parked in the *Run-Test/Idle* state. When a LSP_n is active (unparked), its TMS_L signals follow TMS_B and the LSP_n controller state transitions are synchronized with the TAP Controller state transitions of the 'PSC110F. When the instruction register is updated with the *PARKRTI* instruction, TMS_L will be forced to a constant logic "0", causing the unparked local TAP Controllers to be parked in the *Run-Test/Idle* state. When an LSP_n is parked, it is removed from the active scan chain.

PARKPAUSE: The *PARKPAUSE* instruction has dual functionality. It can be used to park unparked LSPs or to unpark parked LSPs. The instruction places all unparked LSPs in one of the TAP Controller pause states. A local port does not become parked until the 'PSC110F's TAP Controller is sequenced through *Exit1-DR/IR* into the *Update-DR/IR* state. When the 'PSC110F TAP Controller is in the *Exit1-DR* or *Exit1-IR* state and TMS_B is high, the LSP controller forces a constant logic '0" onto TMS_L thereby parking the port in the *Pause-DR* or *Pause-IR* state respectively (see *Figure 4*). Another instruction can then be loaded to reconfigure the local ports or to deselect the 'PSC110F (i.e., *MODESEL, GOTOWAIT,* etc.).

If the *PARKPAUSE* instruction is given to a bridge whose LSPs are parked in *Pause-IR* or *Pause-DR*, the parked LSPs will become unparked when the 'PSC110F's TAP controller is sequenced into the respective Pause state.

The *PARKPAUSE* instruction was implemented with this dual functionality to enable backplane testing (interconnect testing between boards) with simultaneous Updates and Captures.

Simultaneous Update and Capture of several boards can be performed by parking LSPs of the different boards in the *Pause-DR* TAP controller state, after shifting the data to be updated into the boundary registers of the components on each board. The broadcast address is used to select all 'PSC110Fs connected to the backplane. The *PARKPAUSE* instruction is scanned into the selected 'PSC110Fs and the 'PSC110F TAP controllers are sequenced to the *Pause-DR* state where the LSPs of all 'PSC110Fs become unparked. The local TAP controllers are then sequenced through the Update-DR, Select-DR, Capture-DR, Exit1-DR, and parked in the Pause-DR state, as the 'PSC110F TAP controller is sequenced into the Update-DR state. When a LSP is parked, it is removed from the active scan chain.

GOTOWAIT: This instruction is used to return all 'PSC110Fs to the *Wait-For-Address* state. All unparked LSPs will be parked in the *Test-Logic-Reset* TAP controller state (see *Figure 5*).

MODESEL: The *MODESEL* instruction inserts the mode register into the active scan chain. The mode register determines the LSPN configuration. Bit 7 of the mode register is a read-only counter status flag.

MCGRSEL: This instruction inserts the multi-cast group register (MCGR) into the active scan chain. The MCGR is used to group 'PSC110Fs into multi-cast groups for parallel TAP sequencing (i.e., to simultaneously perform identical scan operations).

SOFTRESET: This instruction causes all 3 Port configuration controllers (*Figure 4*) to enter the *Parked-TLR* state, which forces TMS_{Ln} high; this parks each local port in the *Test-Logic-Reset* state within 5 TCK_B cycles.

LFSRSEL: This instruction inserts the linear feedback shift register (LFSR) into the active scan chain, allowing a compacted signature to be shifted out of the LFSR during the *Shift-DR* state. (The signature is assumed to have been computed during earlier *LFSRON* shift operations.) This instruction disables the LFSR register's feedback circuitry, turning the LFSR into a standard 16-bit shift register. This allows a signature to be shifted out of the register, or a seed value to be shifted into it.

LFSRON: Once this instruction is executed, the linear feedback shift register samples data from the active scan path (including all unparked TDI_{Ln}) during the *Shift-DR* state. Data from the scan path is shifted into the linear feedback shift register and compacted. This allows a serial stream of data to be compressed into a 16-bit signature that can subsequently be shifted out using the *LFSRSEL* instruction. The linear feedback shift register is not placed in the scan chain during this mode. Instead, the register samples the active scan-chain data as it flows from the LSPN to TDO_B.

LFSROFF: This instruction terminates linear feedback shift register sampling. The LFSR retains its current state after receiving this instruction.

CNTRSEL: This instruction inserts the 32-bit TCK counter shift register into the active scan chain. This allows the user to program the number of "n" TCK cycles to send to the parked local ports once the *CNTRON* instruction is issued (e.g., for BIST operations). Note that to ensure completion of count-down, the 'PSC110F should receive at least "n" TCK_B pulses.

CNTRON: This instruction enables the TCK counter. The counter begins counting down on the first rising edge of TCK_B following the *Update-IR* TAP controller state and is decremented on each rising edge of TCK_B thereafter. When the TCK counter reaches terminal count, "00000000" Hex, TCK_L of all parked LSP's is held low. ***The CNTROFF instruction must be issued before unparking the LSPs of a 'PSC110F whose counter has reached terminal count.*** This function over-rides the mode register TCK control bit (bit-3).

CNTROFF: This instruction disables the TCK counter, and TCK_L control is returned to the mode register (bit-3).

Level 2 Protocol (Continued)

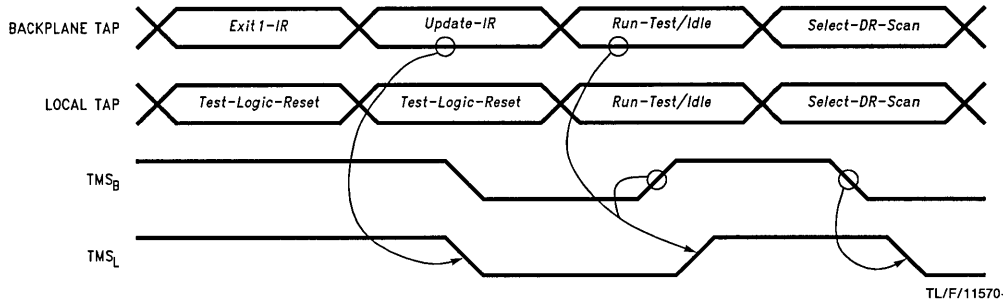

FIGURE 9. Local Scan Port Synchronization from *Parked-TLR* Instruction

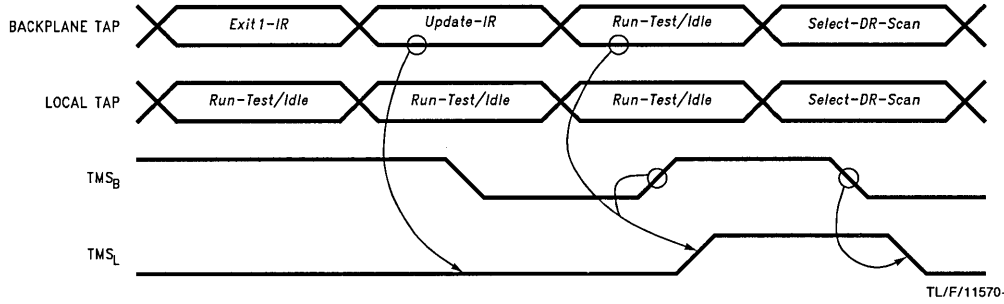

FIGURE 10. Local Scan Port Synchronization from *Parked-RTI* State

Register Descriptions

Instruction Register

The instruction shift register is an 8-bit register that is in series with the scan chain whenever the TAP Controller of the SCANPSC110F Bridge is in the *Shift-IR* state. Upon exiting the *Capture-IR* state, the value "XXXXXX01" is captured into the instruction register, where "XXXXXX" represents the value on the $S_{(0-5)}$ inputs.

When the 'PSC110F controller is in the *Wait-For-Address* state, the instruction register is used for 'PSC110F selection via address matching. In addressing individual 'PSC110Fs, the chip's addressing logic performs a comparison between a statically-configured (hard-wired) value on that 'PSC110F's slot inputs, and an address which is scanned into the chip"s instruction register. Binary address codes "000000" through "111010" ("00" through "3A" Hex) are reserved for addressing individual 'PSC110Fs. Address "3B" Hex is for Broadcast mode.

In doing multi-cast (group) addressing, a scanned-in address is compared against the (previously scanned-in) contents of a 'PSC110F's Multi-Cast Group register. Binary address codes "111110" through "111111" ("3A" through "3F" Hex) are reserved for multi-cast addressing, and should not be assigned as 'PSC110F slot-input values.

Boundary-Scan Register

The boundary-scan register is a "sample only" shift register containing cells from the $S_{(0-5)}$ and $\overline{OE}$ inputs. The register allows testing of circuitry external to the 'PSC110F. It permits the signals flowing between the system pins to be sampled and examined without interfering with the operation of the on-chip system logic.

The scan chain is arranged as follows:

$$TDI_B \rightarrow \overline{OE} \rightarrow S_5 \rightarrow S_4 \rightarrow S_3 \rightarrow S_2 \rightarrow S_1 \rightarrow S_0 \rightarrow LSPN \rightarrow TDO_B$$

Bypass Register

The bypass register is a 1-bit register that operates as specified in IEEE Std. 1149.1 once the 'PSC110F has been selected. The register provides a minimum length serial path for the movement of test data between TDI_B and the LSPN. This path can be selected when no other test data register needs to be accessed during a board-level test operation. Use of the bypass register shortens the serial access-path to test data registers located in other components on a board-level test data path.

Register Description (Continued)

Multi-Cast Group Register

"Multi-cast" is a method of simultaneously communicating with more than one selected 'PSC110F.

The multi-cast group register (MCGR) is a 2-bit register used to determine which multi-cast group a particular 'PSC110F is assigned to. Four addresses are reserved for multi-cast addressing. When a 'PSC110F is in the *Wait-For-Address* state and receives a multi-cast address, and if that 'PSC110F's MCGR contains a matching value for that multi-cast address, the 'PSC110F becomes selected and is ready to receive Level 2 Protocol (i.e., further instructions).

The MCGR is initialized to "00" upon entering the *Test-Logic-Reset* state.

The following actions are used to perform multi-cast addressing:

1. Assign all target 'PSC110Fs to a multi-cast group by writing each individual target 'PSC110F's MCGR with the same multi-cast group code (see Table VI). This configuration step must be done by individually addressing each target 'PSC110F, using that chip's assigned slot value.
2. Scan out the multi-cast group address through the TDI_B input of *all* 'PSC110Fs. Note that this occurs in parallel, resulting in the selection of only those 'PSC110Fs whose MCGR was previously programmed with the matching multi-cast group code.

TABLE VI. Multi-Cast Group Register Addressing

MCGR Bits 1, 0	Hex Address	Binary Address
00	3C	XX111100
01	3D	XX111101
10	3E	XX111110
11	3F	XX111111

TABLE VII. Mode Register Control of LSPN

Mode Register	Scan Chain Configuration (If unparked)
XXX0X000	$TDI_B \rightarrow$ Register $\rightarrow TDO_B$
XXX0X001	$TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow TDO_B$
XXX0X010	$TDI_B \rightarrow$ Register $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$
XXX0X011	$TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow TDO_B$
XXX0X100	$TDI_B \rightarrow$ Register $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$
XXX0X101	$TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$
XXX0X110	$TDI_B \rightarrow$ Register $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$
XXX0X111	$TDI_B \rightarrow$ Register $\rightarrow LSP_1 \rightarrow$ PAD $\rightarrow LSP_2 \rightarrow$ PAD $\rightarrow LSP_3 \rightarrow$ PAD $\rightarrow TDO_B$
XXX1XXXX	$TDI_B \rightarrow$ Register $\rightarrow TDO_B$ (Loopback)

X = don't care

Register = 'PSC110F instruction register or any of the 'PSC110F test data registers

PAD = insertion of a 1-bit register for synchronization

Mode Register

The mode register is an 8-bit data register used primarily to configure the Local Scan Port Network. The mode register is initialized to "00000001" binary upon entering the *Test-Logic-Reset* state.

Bits 0, 1, 2, and 4 are used for scan chain configuration as described in Table VII. When the *UNPARK* instruction is executed, the scan chain configuration will be as shown in Table VII above. When all LSPs are parked, the scan chain configuration will be $TDI_B \rightarrow$ 'PSC110F-register $\rightarrow TDO_B$. Bit 3 is used for TCK_{Ln} configuration, see Table VIII.

TABLE VIII. Test Clock Configuration

Bit 3	LSP_n	TCK_{Ln}
1	Parked	Stop
0	Parked	Run
1	Unparked	Run
0	Unparked	Run

Bit 3 is normally set to logic "0" so that TCK_L is free-running when the local scan ports are parked. When the local ports are parked, bit 3 can be programmed with logic "1", forcing all of the LSP TCK_L's to stop. This feature can be used in power sensitive applications to reduce the power consumed by the test circuitry in parts of the system that are not under test. ***Bit 3 of the mode register must be reset to logic "0" before the UNPARK instruction is executed.***

Bit 7 is a status bit for the TCK counter. When the counter is on and has reached terminal count (Zero) Bit 7 of the mode register will be high (logic "1"). Bit 7 is read-only and will be low in all other conditions.

Bits 5 and 6 are reserved for future use.

Device Identification Register

The device identification register (IDREG) is a 32-bit register compliant with IEEE Std. 1149.1. When the *IDCODE* instruction is active, the identification register is loaded with the value "0FC0E01F" Hex upon leaving the *Capture-DR* state (on the rising edge of the TCK_B).

Register Descriptions (Continued)

TABLE IX. Detailed Device Identification (Binary)

Bits 31–28	Bits 27–12	Bits 11–1	Bit 0
Version	Part Number	Manufacturer Identity	1
0000	1111 1100 0000 1110	0000 0001 111	1

Linear Feedback Shift Register

The 'PSC110F contains a "signature compactor" which supports test result evaluation in a multi-chain environment. The signature compactor consists of a 16-bit linear-feedback shift register (LFSR) which can monitor local-port scan data as it is shifted "upstream" from the 'PSC110F's local-port network. Once the LFSR is enabled, the LFSR's state changes in a reproducible way as each local-port data bit is shifted in from the local-port network. When all local-port data has been scanned in, the LFSR contains a 16-bit signature value which can be compared against a signature computed for the expected results vector.

The LFSR uses the following feedback polynomial:

$$F(x) = X^{16} + X^{12} + X^3 + X + 1$$

This signature compactor is used to compress serial data shifted in from the local scan chain, into a 16-bit signature. This signature can then be shifted out for comparison with an expected value. This allows users to test long scan chains in parallel, via Broadcast or Multi-Cast addressing modes, and check only the 16-bit signatures from each module.

The LFSR is initialized with a value of "0000" Hex upon reset.

32-Bit TCK Counter Register:

The 32-bit TCK counter register enables BIST testing that requires "n" TCK cycles, to be run on a parked LSP while another 'PSC110F port is being tested. The *CNTRSEL* instruction can be used to load a count-down value into the counter register via the active scan chain. When the counter is enabled (via the *CNTRON* instruction), and the LSP is parked, the local TCKs will stop and be held low when terminal count is reached.

The TCK counter is initialized with a value of "00000000" Hex upon reset.

Special Features

BIST SUPPORT

The sequence of instructions to run BIST testing on a parked SCANPSC110F Bridge port is as follows:

1. Pre-load the Boundary register of the device under test if needed.
2. Initialize the TCK counter to 00000000 Hex. Note that the TCK counter is initialized to 00000000 Hex upon *Test-Logic-Reset*, so this step may not be necessary.
3. Issue the *CNTRON* instruction to the 'PSC110F, to enable the TCK counter.
4. Shift the *PARKRTI* instruction into the 'PSC110F instruction register and *BIST* instruction into the instruction register of the device under test.
5. Issue the *CNTRSEL* instruction to the 'PSC110F.
6. Load the TCK counter (Shift the 32-bit value representing the number of TCK_L cycles needed to execute the BIST operation into the TCK counter register).
7. Bit 7 of the Mode register can be scanned to check the status of the TCK counter, (*MODESEL* instruction followed by a *Shift-DR*). Bit 7 logic "0" means the counter has not reached terminal count, logic "1" means that the counter has reached terminal count and the BIST operation has completed.
8. Execute the *CNTROFF* instruction.
9. Unpark the LSP and scan out the result of the BIST operation (the *CNTROFF* instruction must be executed before unparking the LSP).

The Self test will begin on the rising edge of TCK_B following the *Update-DR* TAP controller state.

RESET

Reset operations can be performed at three levels. The highest level resets all 'PSC110F registers and all of the local scan chains of selected and unselected 'PSC110Fs. This "Level 1" reset is performed whenever the 'PSC110F TAP Controller enters the *Test-Logic-Reset* state. *Test-Logic-Reset* can be entered synchronously by forcing TMS_B high for at least five (5) TCK_B pulses, or asynchronously by asserting the $\overline{TRST}$ pin. A "Level 1" reset forces all 'PSC110Fs into the *Wait-For-Address* state, parks all local scan chains in the *Test-Logic-Reset* state, and initializes all 'PSC110F registers.

TABLE X. Reset Configurations for Registers

Register	Bit Width	Initial Hex Value
MCGR	2	0
Instruction	8	AA (*IDCODE* Instruction)
Mode	8	01
LFSR	16	0000
32-Bit Counter	32	00000000

The *SOFTRESET* instruction is provided to perform a "Level 2" reset of all LSP's of selected 'PSC110Fs. *SOFTRESET* forces all TMS_L signals high, placing the corresponding local TAP Controllers in the *Test-Logic-Reset* state within five (5) TCK_B cycles.

The third level of reset is the resetting of individual local ports. An individual LSP can be reset by parking the port in the *Test-Logic-Reset* state via the *PARKTLR* instruction. To reset an individual LSP that is parked in one of the other parked states, the LSP must first be unparked via the *UNPARK* instruction.

PORT SYNCHRONIZATION

When a LSP is not being accessed, it is placed in one of the four TAP Controller states: *Test-Logic-Reset, Run-Test/Idle, Pause-DR,* or *Pause-IR.* The 'PSC110F is able to park a local chain by controlling the local Test Mode Select outputs ($TMS_{L(1-3)}$) (see *Figure 4*). TMS_{Ln} is forced high for parking in the *Test-Logic-Reset* state, and forced low for parking in *Run-Test/Idle, Pause-IR,* or *Pause-DR* states. Local chain access is achieved by issuing the *UNPARK* instruction. The LSPs do not become unparked until the 'PSC110F TAP Controller is sequenced through a specified synchronization state. Synchronization occurs in the *Run-Test/Idle* state for LSPs parked in *Test-Logic-Reset* or *Run-Test/Idle;* and in the *Pause-DR* or *Pause-IR* state for ports parked in *Pause-DR* or *Pause-IR,* respectively.

Figures 11 and *12* show the waveforms for synchronization of a local chain that was parked in the *Test-Logic-Reset* state. Once the *UNPARK* instruction is received in the instruction register, the LSPC forces TMS_L low on the falling edge of TCK_B.

Special Features (Continued)

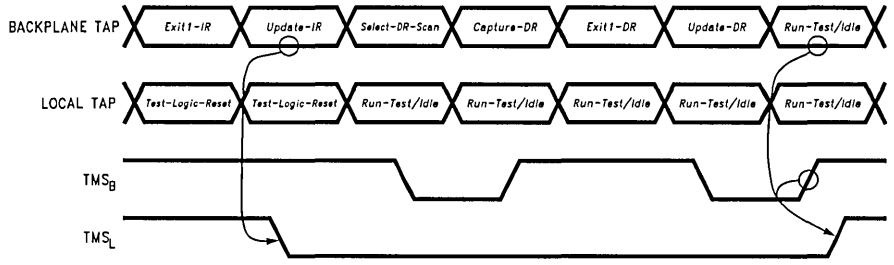

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FIGURE 11. Local Scan Port Synchronization on Second Pass

This moves the local chain TAP Controllers to the synchronization state *(Run-Test/Idle)*, where they stay until synchronization occurs. If the next state of the 'PSC110F TAP Controller is *Run-Test/Idle*, TMS_L is connected to TMS_B and the local TAP Controllers are synchronized to the 'PSC110F TAP Controller as shown in *Figure 12*. If the next state after *Update-IR* were *Select-DR*, TMS_L would remain low and synchronization would not occur until the 'PSC110F TAP Controller entered the *Run-Test/Idle* state, as shown in *Figure 11*.

Each local port has its own Local Scan Port Controller. This is necessary because the LSPN can be configured in any one of eight (8) possible combinations. Either one, some, or all of the local ports can be accessed simultaneously. Configuring the LSPN is accomplished with the mode register, in conjunction with the *UNPARK* instruction.

The LSPN can be unparked in one of seven different configurations, as specified by bits 0-2 of the mode register. Using multiple ports presents not only the task of synchronizing the 'PSC110F TAP Controller with the TAP Controllers of an individual local port, but also of synchronizing the individual local ports to one another.

When multiple local ports are selected for access, it is possible that two ports are parked in different states. This could occur when previous operations accessed the two ports separately and parked them in the two different states. The LSP Controllers handle this situation gracefully. *Figure 12* shows the *UNPARK* instruction being used to access LSP_1, LSP_2, and LSP_3 in series (mode register = "XXX0X111" binary). LSP_1 and LSP_2 become active as the 'PSC110F controller is sequenced through the *Run-Test/Idle* state. LSP_3 remains parked in the *Pause-DR* state until the 'PSC110F TAP Controller is sequenced through the *Pause-DR* state. At that point, all three local ports are synchronized for access via the active scan chain.

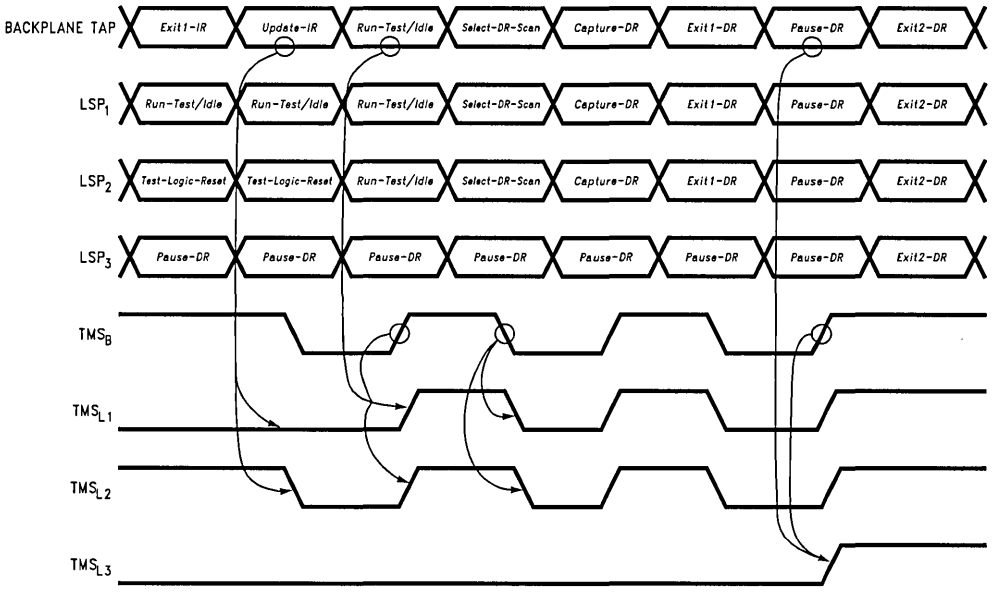

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FIGURE 12. Synchronization of the Three Local Scan Ports (LSP_1, LSP_2, and LSP_3)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IL})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
DC Latchup Source or Sink Current	±300 mA
Junction Temperature	
SOIC	+140°C
Storage Temperature	−65°C to +150°C
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply temperature, and output/input loading variables. National does not recommended operation of SCAN outside of recommended operation conditions.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
SCANPSC110F	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Commercial	−40°C to +85°C
Military	−55°C to +125°C
Minimum Input Edge Rate dV/dt	
SCAN "F" Series Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial T_A = 25°C		Military T_A = −55°C to +125°C	Commercial T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH} (TCK_{Ln}, TMS_{Ln}, TDO_{Ln})	Minimum High Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA V_{IN} (TDI_B, TMS_B, TCK_B) = V_{IH}
V_{OH} (TCK_{Ln}, TMS_{Ln}, TDO_{Ln})	Minimum High Output Voltage	4.5 5.5		3.86 4.86	3.7 4.7	3.76 4.76	V	I_{OUT} = −24 mA V_{IN} on $S_{(0-5)}$ and $TDI_{(1-3)}$ = V_{IH}, V_{IL} All Outputs Loaded
V_{OH} (TDO_B)	Minimum High Output Voltage	4.5 5.5		3.15 4.15	3.15 4.15	3.15 4.15	V	I_{OUT} = −50 μA
V_{OH} (TDO_B)	Minimum High Output Voltage	4.5 5.5		2.4 2.4		2.4 2.4	V	I_{OUT} = −32 mA All Outputs Loaded
V_{OH} (TDO_B)	Minimum High Output Voltage	4.5 5.5		2.4 2.4	2.4 2.4		V	I_{OUT} = −24 mA All Outputs Loaded
V_{OL} (TCK_{Ln},TMS_{Ln}, TDO_{Ln})	Maximum Low Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = +50 μA V_{IN} (TDI_B, TMS_B, TCK_B) = V_{IL}

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial T_A = 25°C		Military T_A = −55°C to +125°C	Commercial T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{OL} (TCK_{Ln}, TMS_{Ln}, TDO_{Ln})	Maximum Low Output Voltage	4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	I_{OUT} = +24 mA V_{IN} on $S_{(0-5)}$ and $TDI_{(1-3)}$ = V_{IH}, V_{IL} All Outputs Loaded
V_{OL} (TDO_B)	Maximum Low Output Voltage	4.5 5.5		0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = +50 μA
V_{OL} (TDO_B)	Maximum Low Output Voltage	4.5 5.5		0.55 0.55	0.55 0.55		V	I_{OUT} = +48 mA All Outputs Loaded
V_{OL} (TDO_B)	Maximum Low Ouput Voltage	4.5 5.5		0.55 0.55		0.55 0.55	V	I_{OUT} = +64 mA All Outputs Loaded
I_{IN} ($\overline{OE}$, TCK_B, $S_{(0-5)}$)	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_{IN} = V_{CC} or V_{IN} = GND
$I_{IN, MAX}$ ($\overline{TRST}$, TDI_{Ln}, TDI_B, TMS_B)	Maximum Input Leakage Current	5.5		2.8	3.7	3.6	μA	V_{IN} = V_{CC}
$I_{IN, MAX}$ ($\overline{TRST}$, TDI_{Ln}, TDI_B, TMS_B)	Maximum Input Leakage Current	5.5		−385	−385	−385	μA	V_{IN} = GND
$I_{IN, MIN}$ (TDI_B, TMS_B, $\overline{TRST}$, TDI_{Ln})	Minimum Input Leakage Current	5.5		−160	−160	−160	μA	V_{IN} = GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_{IN} = V_{CC} −2.1V
I_{CCT} (TDI_B, TMS_B, $\overline{TRST}$, TDI_L)	Maximum I_{CC}/Input	5.5	0.6		1.75	1.65	mA	V_{IN} = V_{CC} −2.1V Test one at a time with others floating
I_{CC}	Maximum Quiescent Supply Current	5.5		16	168	88	μA	TDI_B, TMS_B, $\overline{TRST}$, TDI_L = V_{CC}
$I_{CC, MAX}$	Maximum Quiescent Supply Current	5.5		2.35	2.5	2.4	mA	TDI_B, TMS_B, $\overline{TRST}$, TDI_L = GND
I_{OLD} (TCK_{Ln}, TMS_{Ln}, TDO_{Ln})	Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V max V_{IN} ($\overline{OE}$) = V_{IL} (Note 2)
I_{OLD} (TDO_B)	Minimum Dynamic Output Current	5.5		94	63	94	mA	V_{OLD} = 0.8V V_{IN} ($\overline{TRST}$) = V_{IH} (Note 2)

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial		Military	Commercial	Units	Conditions
			T_A = 25°C		T_A = −55°C to +125°C	T_A = −40°C to +85°C		
			Typ	Guaranteed Limits				
I_{OHD} (TCK_{Ln}, TMS_{Ln}, TDO_{Ln})	Minimum Dynamic Output Current	5.5			−50	−75	mA	V_{OHD} = 3.85V max (Note 2)
I_{OHD} (TDO_B)	Minimum Dynamic Output Current	5.5		−40	−27	−40	mA	V_{OHD} = 2.0V max (Note 2)
I_{OZ}	Maximum TRI-STATE® Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_{IN} ($\overline{OE}$) = V_{IH} V_{IN} ($\overline{TRST}$) = V_{IL} V_O = V_{CC}, GND
I_{OS} (TDO_B)	Output Short Circuit Current	5.5		−100	−100	−100	mA min	V_O = 0.0V (Note 3)

Note 2: Maximum test duration of 2 ms. One output loaded at a time.

Note 3: Maximum test duration not to exceed 1 second.

Noise Specifications

Symbol	Parameter	V_{CC} (V)	Commercial		Military	Commerical	Units	Conditions
			T_A = +25°C		T_A = −55°C to +125°C	T_A = −40°C to +85°C		
			Type	Guaranteed Limits				
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.3	0.6			V	*Figure 14* (Note 4)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	0.3	−0.6			V	*Figure 14* (Note 4)
V_{OHP}	Quiet Output Maximum Dynamic V_{OH}	5.0	V_{OH} + 0.5	V_{OH} + 1.0			V	*Figure 14* (Note 5)
V_{OHV}	Quiet Output Minimum Dynamic V_{OH}	5.0	V_{OH} − 0.7	V_{OH} − 1.2			V	*Figure 14* (Note 5)
V_{IHD}	Minimum High Dynamic Input Voltage Level	5.5	1.9	2.2	2.2	2.2	V	(Note 6)
V_{ILD}	Maximum Low Dynamic Input Voltage Level	5.5	1.4	0.8	0.8	0.8	V	(Note 6)

Note 4: Maximum number of outputs that can switch simultaneously is n. (n−1) outputs are switched LOW and one output held LOW.

Note 5: Maximum number of outputs that can switch simultaneously is n. (n−1) outputs are switched HIGH and one output held HIGH.

Note 6: Maximum number of data inputs (n) switching. (n−1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$, $C_L = 50$ pF			Military (Preliminary) $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay $TCK_B \downarrow$ to TCK_{Ln}	5.0	3.0	8.5	12.5	3.0	15.0	3.0	13.5	ns	13
	$TCK_B \uparrow$ to TCK_{Ln}		2.5	8.5	12.5	2.5	15.0	2.5	13.5		
t_{PHL}, t_{PLH}	Propagation Delay $TCK_B \downarrow$ to TDO_{Ln}	5.0	3.0	10.0	14.0	3.0	16.5	3.0	15.0	ns	13
	$TCK_B \downarrow$ to TDO_{Ln}		3.0	10.0	14.5	3.0	17.0	3.0	15.5		
t_{PHL}, t_{PLH}	Propagation Delay $TCK_B \downarrow$ to TMS_{Ln}	5.0	3.5	15.0	23.0	3.5	26.5	3.5	25.0	ns	13
	$TCK_B \downarrow$ to TMS_{Ln}		4.5	14.5	21.5	4.5	24.5	4.5	23.0		
t_{PHL}, t_{PLH}	Propagation Delay $TCK_B \downarrow$ to TDO_B	5.0	3.0	9.5	14.5	3.0	17.0	3.0	15.5	ns	13
	$TCK_B \downarrow$ to TDO_B		2.5	9.0	13.5	2.5	16.5	2.5	15.0		
t_{PHL}, t_{PLH}	Propagation Delay TMS_B to TMS_{Ln}	5.0	2.5	8.0	12.0	2.5	14.5	2.5	13.0	ns	13
			1.5	7.5	12.0	1.5	14.5	1.5	13.0		
t_{PLH}	Propagation Delay $\overline{TRST}$ to TMS_{Ln}	5.0	4.5	19.0	26.5	4.5	30.0	4.5	28.5	ns	15
t_{PZL}, t_{PZH}	Enable Time $TCK_B \downarrow$ to TDO_{Ln}	5.0	4.0	12.5	18.5	4.0	22.5	4.0	20.5	ns	
	$TCK_B \downarrow$ to TDO_{Ln}		3.0	11.0	15.5	3.0	19.0	3.0	17.0		
t_{PLZ}, t_{PHZ}	Disable Time $TCK_B \downarrow$ to TDO_{Ln}	5.0	1.5	7.5	12.0	1.5	15.5	1.5	13.5	ns	
	$TCK_B \downarrow$ to TDO_{Ln}		2.0	8.5	14.0	2.0	17.0	2.0	15.0		
t_{PZL}, t_{PZH}	Enable Time $TCK_B \downarrow$ to TDO_B	5.0	4.0	12.0	17.0	4.0	20.5	4.0	18.5	ns	
	$TCK_B \downarrow$ to TDO_B		2.5	9.0	13.5	2.5	16.5	2.5	14.5		
t_{PLZ}, t_{PHZ}	Disable Time $TCK_B \downarrow$ to TDO_B	5.0	2.0	9.0	13.0	2.0	16.5	2.0	14.5	ns	
	$TCK_B \downarrow$ to TDO_B		2.0	9.5	14.0	2.0	17.5	2.0	15.5		
t_{PZL}, t_{PZH}	Enable Time $\overline{OE}$ to TDO_{Ln}	5.0	3.0	10.0	15.0	3.0	19.5	3.0	17.5	ns	16
			3.0	10.0	14.0	3.0	17.0	3.0	15.0		
t_{PLZ}, t_{PHZ}	Disable Time $\overline{OE}$ to TDO_{Ln}	5.0	1.0	7.0	11.0	1.0	14.0	1.0	12.0	ns	16
			1.0	8.0	13.0	1.0	15.5	1.0	13.5		
t_{PZL}, t_{PZH}	Enable Time $\overline{OE}$ to TMS_{Ln}	5.0	2.0	8.0	11.5	2.0	14.5	2.0	12.5	ns	16
			1.5	6.5	10.0	1.5	13.0	1.5	11.0		
t_{PLZ}, t_{PHZ}	Disable Time $\overline{OE}$ to TMS_{Ln}	5.0	1.0	5.0	9.0	1.0	12.0	1.0	10.0	ns	16
			1.0	6.0	10.0	1.0	12.5	1.0	10.5		
t_{PZL}, t_{PZH}	Enable Time $\overline{OE}$ to TCK_{Ln}	5.0	2.0	8.0	11.5	2.0	14.5	2.0	12.5	ns	16
			1.5	6.5	10.0	1.5	13.0	1.5	11.0		
t_{PLZ}, t_{PHZ}	Disable Time $\overline{OE}$ to TCK_{Ln}	5.0	1.0	5.0	9.0	1.0	12.0	1.0	10.0	ns	16
			1.0	6.0	10.0	1.0	12.5	1.0	10.5		
t_{PLZ}, t_{PHZ}	Disable Time $\overline{TRST}$ to TDO_B	5.0	2.5	11.0	16.5	2.5	20.0	2.5	18.0	ns	15
			3.0	12.0	16.5	3.0	20.0	3.0	18.0		
t_{PLZ}, t_{PHZ}	Disable Time $\overline{TRST}$ to TDO_{Ln}	5.0	2.5	11.5	17.5	2.5	21.0	2.5	19.0	ns	15
			1.5	11.5	17.5	1.5	21.0	1.5	19.0		

AC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial		Military (Preliminary)	Commercial	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_S	Setup Time TMS_B to $TCK_B \uparrow$	5.0	3.5	8.0	8.0	8.0	ns	13
t_H	Hold Time TMS_B to $TCK_B \uparrow$	5.0	−0.5	4.0	4.0	4.0	ns	13
t_S	Setup Time TDI_B to $TCK_B \uparrow$	5.0	1.5	6.0	6.0	6.0	ns	13
t_H	Hold Time TdI_B to $TCK_B \uparrow$	5.0	1.0	4.0	4.0	4.0	ns	13
t_S	Setup Time S_n to $TCK_B \downarrow$ (in *Update-DR* state)	5.0	7.5	12.5	12.5	12.5	ns	
t_H	Hold Time S_n to $TCK_B \downarrow$ (in *Update-DR* state)	5.0	−3.0	0.0	0.0	0.0	ns	
t_S	Setup Time S_n to $TCK_B \uparrow$ (in *Capture-DR* or *Capture-IR* state)	5.0	0.0	4.0	4.0	4.0	ns	
t_H	Hold Time S_n to $TCK_B \uparrow$ (in *Capture-DR* or *Capture-IR* state)	5.0	1.5	6.0	6.0	6.0	ns	
t_S	Setup Time TDI_{Ln} to $TCK_B \uparrow$	5.0	−1.5	2.0	2.0	2.0	ns	13
t_H	Hold Time TDI_{Ln} to $TCK_B \uparrow$	5.0	2.0	6.0	6.0	6.0	ns	13
t_S	Setup Time $\overline{OE}$ to $TCK_B \uparrow$ (in *Capture-DR* state)	5.0	0.0	4.0	4.0	4.0	ns	
t_H	Hold Time $\overline{OE}$ to $TCK_B \uparrow$ (in *Capture-DR* State)	5.0	0.0	4.0	4.0	4.0	ns	
t_W	Clock Pulse Width TCK_B (H or L)	5.0	16.0	20.0	24.0	24.0	ns	13
t_{WL}	Clock Pulse Width $\overline{TRST}$ (L)	5.0	6.0	10.0	10.0	10.0	ns	15

AC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	Commercial		Military (Preliminary)	Commercial	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_{REC}	Recover Time $TCK_B \uparrow$ from $\overline{TRST}$	5.0	−2.0	2.0	2.0	2.0	ns	15
t_{OSHL}, t_{OSLH}	Output-to-Output Skew TCK_{Ln}	5.0		1.0	1.0	1.0	ns	(Note 7)
t_{OSHL}, t_{OSLH}	Output-to-Output Skew TMS_{Ln} (unparked)	5.0		2.0	2.0	2.0	ns	(Note 7)
F_{MAX}	Maximum Clock Frequency	5.0		25			MHz	

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}). The specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	5.0	pF	V_{CC} is Open
C_{OUT}	Output Pin Capacitance	6.5	pF	V_{CC} is Open
C_{PD}	Power Dissipation Capacitance	50	pF	$V_{CC} = 5.0V$

AC Waveforms

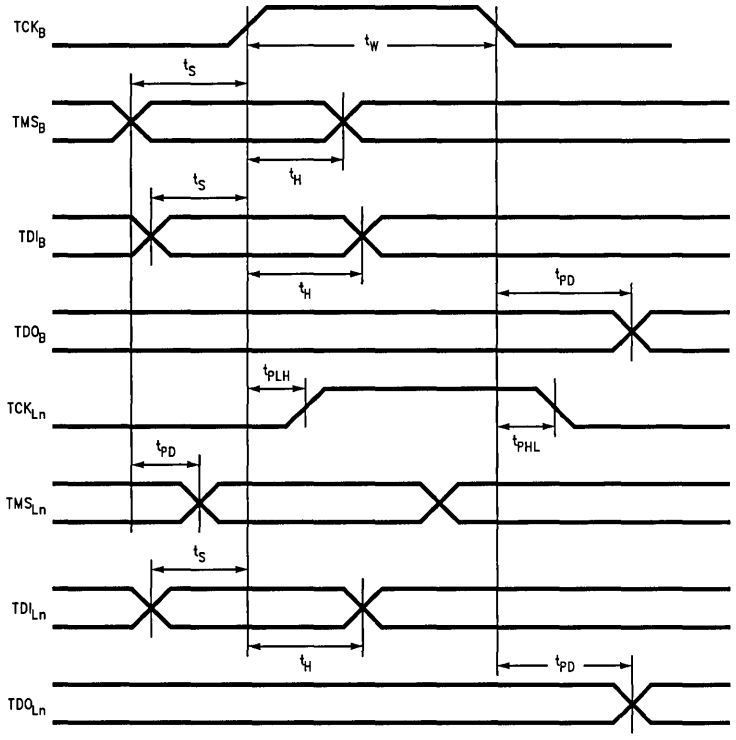

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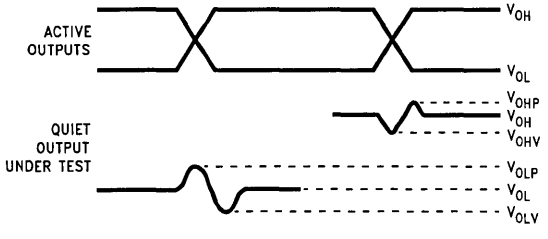
FIGURE 13. Waveforms for an Unparked SCANPSC110F Bridge in the SHIFT-DR (IR) TAP Controller State



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Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew ≤ 150 ps.

FIGURE 14. Quiet Output Noise Voltage Waveform

AC Waveforms (Continued)

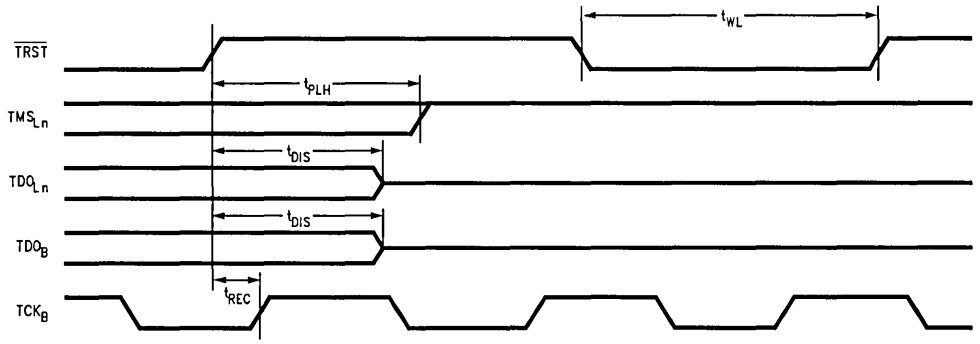

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FIGURE 15. Reset Waveforms

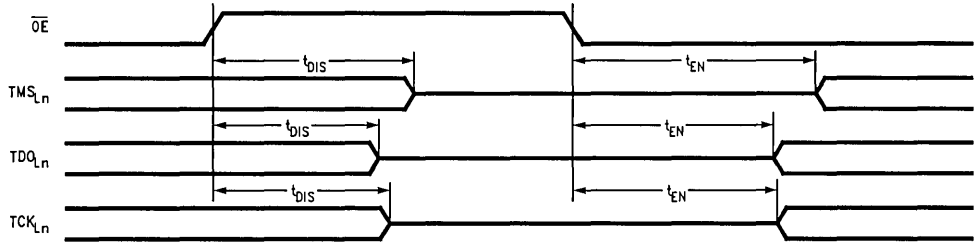

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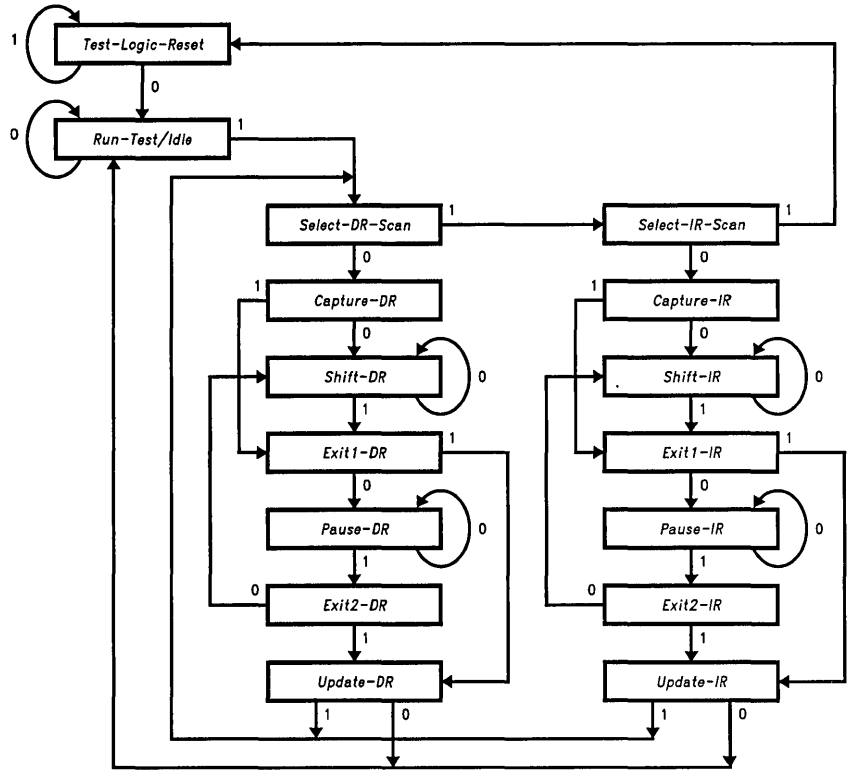
FIGURE 16. Output Enable Waveforms

Appendix



Note: The value of the TMS during the rising edge of TCK is located next to each transition.

FIGURE 17. IEEE 1149.1 TAP Controller State Diagram

Applications Example

The following sequence gives an example of how one might use the SCANPSC110F Bridge to perform 1149.1 operations via a multi-drop scan backplane. The system involved has 10 card slots, 8 of which are filled with modules, and 2 slots are empty. (See *Figure 18*).

More Information can be found in Application Notes:

AN-1023 Structural System Test via IEEE Std. 1149.1 with SCANPSC110F Hierarchical and Multidrop Addressable JTAG Port

AN-1022 Boundary Scan, An Enabling Technology for System Level Embedded Test

1. After the system is powered up a level-1 reset is performed via the $\overline{TRST}$ input. All TAP Controllers (both 'PSC110F and local) are asynchronously forced into the *Test-Logic-Reset* state. All LSP Controllers are in the parked *Test-Logic-Reset* state; this forces the TMS_L outputs of each port to a logic "1", keeping all board TAPs in the *Test-Logic-Reset* state.

2. The first task of the tester is to find out which slots are occupied on the backplane. This is accomplished by performing a serial poll of each slot address in the system, as assigned by the S_{0-5} value of each 'PSC110F in the system.

   Each target slot address is addressed by first sequencing all 'PSC110Fs on the backplane to the *Shift-IR* state, and then by shifting in the address of the target slot. The 'PSC110F TAP controller is then sequenced through the Update-IR state. If a 'PSC110F with the matching slot identification is present, it is selected. All other 'PSC110Fs are unselected. To determine whether that slot contains a selected 'PSC110F, the tester must read back the 'PSC110Fs S_{0-5} value (if present).

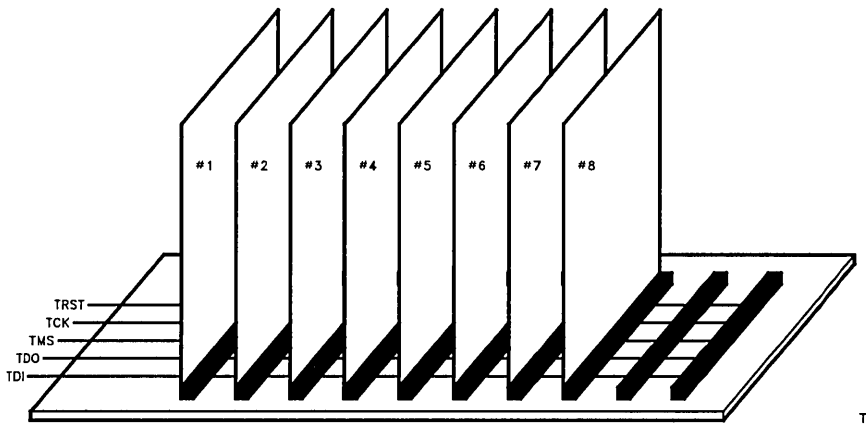
   The tester moves the selected 'PSC110F from the *Update-IR* state back to the *Shift-IR* state, and the instruction register is then scanned while loading the next instruction *(GOTOWAIT)*. During the *Capture-IR* state of the TAP Controller, a "01" pattern is loaded into the two least significant bits of the 'PSC110F's instruction register, and the most significant six bits capture the value on the S_{0-5} pins. The captured data is shifted out while the *GOTOWAIT* command is shifted in. If an "all ones" pattern is returned, a board does not exist at that location. (The "all ones" pattern is caused by the pull-up resistor on the TDI input of the controller, as required for 1149.1 compliance.)

   At the end of instruction register scan, the *GOTOWAIT* command is issued and all 'PSC110F selection controllers enter the *Wait-For-Address* state. This allows the next 'PSC110F in the polling sequence to be addressed. The polling process is repeated for every possible board address in the system. In this example, the tester finds that boards #1 through #8 are present, and boards #9 and #10 are missing. Therefore, it will report back its findings and will not attempt to test the missing boards.

3. Infrastructure testing of the populated boards may now proceed. The tester addresses the 'PSC110F on Board #1 for test operations. 'PSC110F #1 is now selected, while all others are unselected.

   Board #1 is wired such that all LSP_n's are connected to individual scan chains. The first objective is to test the scan chain integrity of the board. For this task, it is more efficient to configure the LSPN such that all three chains are placed in series. To accomplish this, the *MODESEL* instruction is issued to place the mode register into the active scan chain, and the binary value "00000111" is shifted into the mode register. The *UNPARK* instruction is then issued to access all three local chains.

   Once the *UNPARK* instruction has been updated and the 'PSC110F TAP controller is synchronized with the local TAP's, the scan chain integrity test can be performed on the local scan chains. This test is done by performing a *Capture-IR* and then shifting the scan chain checking the 2 least significant bits of each components instruction register for "01". If the LSB's of any component in the scan chain are not "01", the test fails. Diagnostic software can be used to narrow down the cause of the failure. Next the device identification of each component in the scan chain is checked. This is done by issuing the *IDCODE* instruction to each component in the scan chain. Components that do not support *IDCODE* will insert their bypass register into the active scan chain.



TL/F/11570–20

FIGURE 18. Boundary Scan Backplane with 10 Card Slots, 8 Slots Are Filled with Boards

Applications Example (Continued)

After the IDCODE register scan, the *GOTOWAIT* instruction is issued to reset the local scan ports and return the 'PSC110F Selection controller to the Wait-For-Address state. A sequence similar to step 3 is repeated for each board in the system.

4. Next, the tester addresses Board #1 to perform interconnect testing. For this task, it is efficient to configure the LSPN such that all three chains are placed in series. Therefore, the Mode register should be programmed with the binary value "00000111" (this was done in step 3 above and need not be repeated unless a *Test-Logic-Reset* was performed since then). The *UNPARK* instruction is issued to access all three local chains.

   Once the *UNPARK* instruction has been loaded and the 'PSC110F is synchronized with the local TAPs, normal 1149.1 scan operations may commence. To test the interconnect on Board #1, an instruction register scan sequence is performed and the *SAMPLE/PRELOAD* instruction is loaded into the instruction register of all target devices. The *BYPASS* instruction is loaded into the instruction register of 'PSC110F #1. A data register scan is now performed to preload the first test vector to be applied to the interconnect.

5. After the preload operation is performed, an instruction register scan is used to load the *EXTEST* instruction into all TAPs (*BYPASS* loaded into 'PSC110F #1). The appropriate sequencing is now performed to apply patterns in order to test the interconnect on Board #1.

6. Upon completion of the interconnect test on Board #1, the local chains must be parked. The *PARKTLR* command is loaded into the instruction register, and the TMS_{Ln} outputs of the three local chains are forced high, sending the three local TAPs into the *Test-Logic-Reset* state.

7. Now that the Board #1 interconnect has been tested, the interconnect on the other boards in the system must be checked. All 'PSC110F are returned to the *Wait-For-Address* state by issuing the *GOTOWAIT* instruction. Board #2 is addressed next, followed by the rest of the boards in the system. A sequence similar to steps 4 through 6 is used for each board.

8. Assume that boards #6, #7 and #8 are identical, so that it is possible to test them simultaneously. The tester first addresses Board #6. Next the *MCGRSEL* instruction is issued to place the Multi-Cast Group register into the active scan chain, and the binary value "01" is shifted into the MCGR. The *GOTOWAIT* instruction is then issued returning all 'PSC110F's to the *Wait-For-Address* state. The MCGR for 'PSC110F #7 and 'PSC110F #8 are programmed the same as Board #6. Next the Multi-Cast address "00111101" is issued by the tester, which causes the 'PSC110F Selection controller of 'PSC110F #6–#8 to enter the *Selected-Multi-Cast* state. The *LFSRON* instruction is then issued to enable the signature compaction circuitry on the selected 'PSC110Fs. The *SAMPLE/PRELOAD* and *EXTEST* instructions are then used to test the interconnects, similar to steps 4 and 5 above. When the test sequence is complete, the *GOTOWAIT* instruction is issued returning all 'PSC110Fs to the *Wait-For-Address state.* 'PSC110Fs #6, #7, and #8 are then addressed one at a time to read back the test signature from the LFSR (the LFSR is read by selecting it with the *LFSRSEL* instruction, then scanning out its contents.

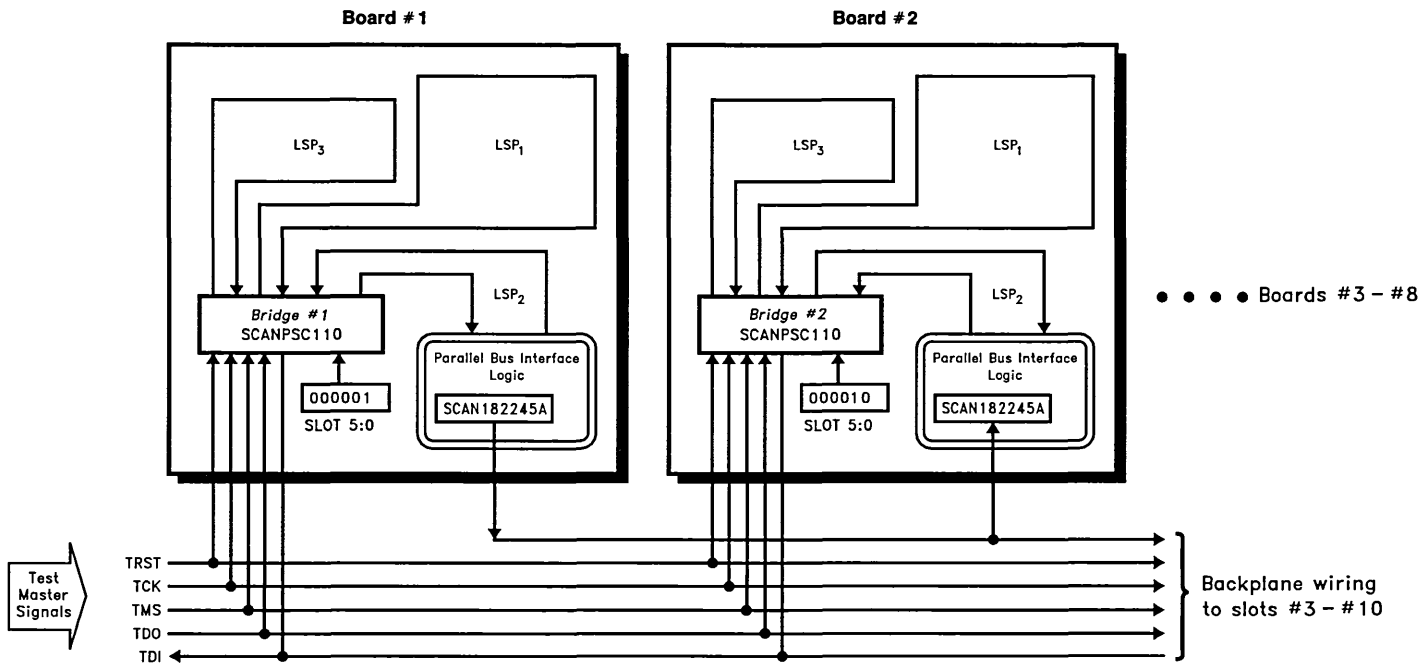
9. After testing the interconnect on the individual boards, the next step is to test the backplane interconnect. This is a pair-wise test between Board #1 and each of the other boards. Board #1 drives test patterns onto th backplane wiring, and the currently addressed slave board senses the written data via its backplane scan interface. In this example, the interconnect between Board #1 and Board #2 is tested first. To test this interconnect, the 1149.1-compliant backplane transceivers, SCAN182245A, SCAN ABT Test Access Logic, on each board must be accessed for scan operations (see *Figure 19*). For more information on SCAN ABT live insertion capabilities, refer to the SCAN182245A datasheet.

   First, the system master (Board #1) is addressed and selected. The 1149.1-compliant SCAN ABT transceivers reside on the chain connected to LSP_2 on Board #1. The mode register is re-configured so that only port LSP_2 is in the chain, and the *UNPARK* instruction is then used to access this chain. The appropriate instruction register and data register scan sequencing is then performed to apply a pattern to the backplane using the SCAN ABT bus transceiver.

10. To test the backplane interconnect, LSP_2 of Board #1 must be parked in the *Run-Test/Idle* TAP controller state, so that the EXTEST command will stay active when Board #1 is de-selected (the *PARKRTI* instruction is issued). The *GOTOWAIT* instruction is then issued to return all boards to the *Wait-For-Address* state. Each one of the slave boards is then addressed, one at a time, to sample the backplane signals being driven by Board #1. For example, Board #2 is addressed. The mode register is reconfigured, (if needed), to select the scan chain (LSP_2) that includes the SCAN ABT backplane transceivers for Board #2. The *UNPARK* instruction is issued to unpark LSP_n and insert it into the active scan chain. The *SAMPLE/PRELOAD* instruction is issued to the SCAN ABT backplane transceivers, (*BYPASS* to other components in the scan chain). The backplane is sampled by sequencing the TAP controller through the *Capture-DR* state and the data is shifted out and checked by the tester. The *PARKRTI* instruction is then given to park LSP_n of Board #2 in the *Run-Test/Idle* state, and the *GOTOWAIT* instruction is issued to return all 'PSC110Fs to the *Wait-For-Address* state so that the next board, (Board #3), can be sampled. This procedure is repeated for boards #3–#8, then Board #1 is selected again, a new pattern is shifted out and driven by the *EXTEST* command, and the slave boards are again sampled.

11. Step 10 is repeated until the backplane interconnect has been sufficiently tested.

12. When testing is complete, the controller sends out the *SOFTRESET* instruction to all 'PSC110Fs. This is accomplished by first using the broadcast address, "3B" Hex, to select all 'PSC110Fs. The *SOFTRESET* command is then loaded, causing $TMS_{L(1-3)}$ signals to go high; this drives all local TAPs into the *Test-Logic-Reset* state within five TCK cycles.



TL/F/11570–21

FIGURE 19. Testing the Backplane Interconnections

National Semiconductor

SCAN EASE
SCAN Embedded Application Software Enabler

General Description

National Semiconductor SCAN EASE, a suite of software tools, enables ATPG or custom generated test vectors to be embedded within an IEEE 1149.1 compatible system, administers test control and provides remote access.

EmbedPrep—Embedded Test Preparation includes embedded test development tools that convert ATPG output files, like SVF or PAT, into Embedded Vector Format (EVF) for use with EmbedTest.

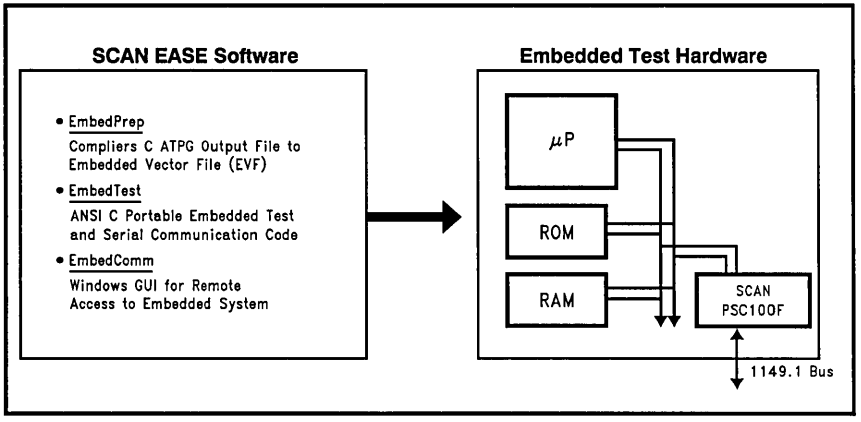
EmbedTest—Embedded Test application code includes high level code that controls the test flow and communications between the embedded system and a remote system test administrator. It includes function libraries for controlling IEEE 1149.1 compliant boundary scan chains (SCANLIB), and reading test vectors stored in EVF (EVFLIB). EmbedTest compiles to run on any microprocessor supporting ANSI-C.

EmbedComm—Embedded Test Communication provides a Windows® GUI for remote access to EmbedTest running on an embedded system.

Features

- Processor independent—runs on big/little endian and memory- and I/O-mapped architectures
- Compatible with Teradyne VICTORY™ ATPG and JTAG Technology BTPG™ tools (others supported upon request)
- Provides automated translation, application and evaluation of ATPG-generated tests in an embedded system environment
- Includes a Scan Function Library and National's Embedded Boundary Scan Controller SCANPSC100F device driver to support custom or non-ATPG generated vector applications
- Supports embedded test data log for diagnostic processing
- Includes Microsoft Windows GUI and serial communication code for system administration and remote testing
- Supports SCANPSC110F Hierarchical and Multidrop JTAG Addressable Port architecture

Order Number	Description
SCANEASEV100BSW	Basic Software License
SCANEASEV100CSW	Corporate License
SCANEASEV100MSW	Maintenance Contract



TL/F/12120–1

FIGURE 1. SCAN EASE Enables ATPG Test Vectors to be Embedded

Functional Description

SCAN EASE does much of the programming work required by programmers to convert a tester manufacturer's test vectors into embedded test vectors; manages and executes the test; and provides communications code to download and initiate tests remotely. SCAN EASE has a user-friendly Windows GUI interface to simplify test administration.

The test development process for embedded system test begins with generating tests using an off-the-shelf ATPG tool. A separate set of tests for each board type in the system is created during manufacturing test development. These tests can be reused for embedded test, too. National's SCAN EASE tools compile test vectors stored in Serial Vector Format (SVF) or Pattern Format (PAT) into EVF, a compact binary format appropriate for embedded applications.

Several of the board level EVF files can be concatenated to create a system level test. Partitioning tests enables EmbedTest to isolate and report pass/fail information to the partitioned level—board, module, etc.—without running diagnostic software. EVF test files can be placed in ROM for power-up self test or down loaded to RAM.

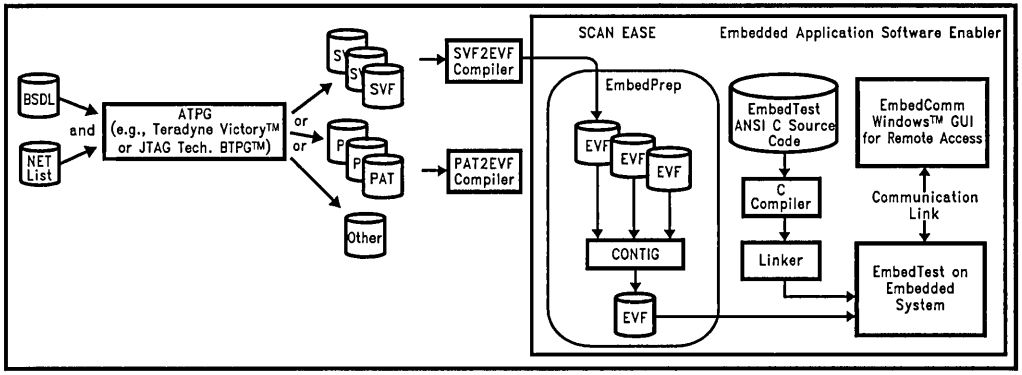
EmbedTest also provides a set of functions that enable communication between the embedded system and a serial interface for a system administrator or remote computer. EmbedTest commands, such as configuration, reporting test results, downloading new tests and uploading data logs, are performed over this serial interface.

Supporting Hardware

The SCANPSC100F Embedded Boundary Scan Controller is a 28-lead IC designed to provide a simple, efficient interface between a microprocessor and the 1149.1 Test Access Port (TAP) signals. Its 8-bit asynchronous interface connects directly to the local bus of many popular processors and allows the test clock (TCK) to run at a different clock speed than the local bus. The SCANPSC100F supports TCK frequencies up to 25 MHz.

Compatibility

Designed for portability and flexibility, both EmbedTest and EVF run on both big endian and little endian memory architectures; the SCANPSC100F can be either I/O-mapped or memory-mapped. This flexibility allows same code and test vectors to run on various machines simply by recompiling with a C-compiler for the target machine.



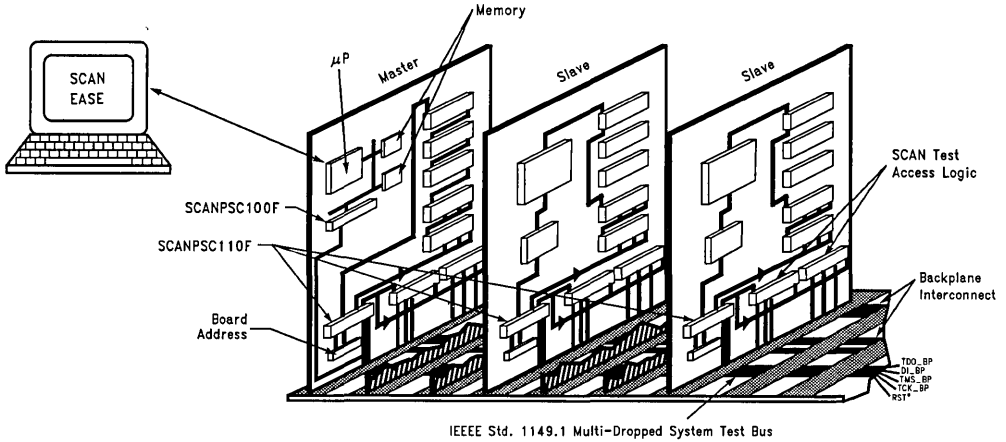
TL/F/12120–2

FIGURE 2. SCAN EASE Works with Existing Board Test Vectors

System Level Test Support

Partitioning tests is important to achieve built-in fault isolation. A natural place to partition tests is at the board or module interface. Design boards with a 100% scannable interface to the system back plane by buffering all back plane signals with boundary scan compliant components like National's 18-bit wide SCAN Test Access Logic CMOS and ABT devices. A 100% scannable interface enables ATPG to generate 100% fault coverage on the back plane. The SCAN ABT Test Access Logic interface with power-up TRI-STATE® for live insertion allows board level tests to be performed without disturbing back plane signals, too.

The Hierarchical and Multidrop JTAG Addressable Port SCANPSC110F provides an interface from a single IEEE 1149.1 TAP to "local TAPs" on boards or modules that reside within a system. This enables boards to be pulled or added to the system without breaking the serial scan chain, and makes it possible to perform an interrogating infrastructure test to determine the system configuration before applying board-level tests. The SCANPSC110F facilitates partitioning of boards and modules within the system for improved fault isolation.



TL/F/12120–3

FIGURE 3. Embedding SCAN EASE for System Level Test

More Detailed Information about SCAN EASE

An application note is available on National's Web Site (http://www.nsc.com), and through the National Technical Support Center (1-800-272-9959) to provide more detailed information on the SCAN EASE architecture and API (applications programming interface). The SCAN EASE product includes a reference manual to detail the EVF format, embedded code architecture and functions which comprise the SCAN EASE tool set.

Section 11

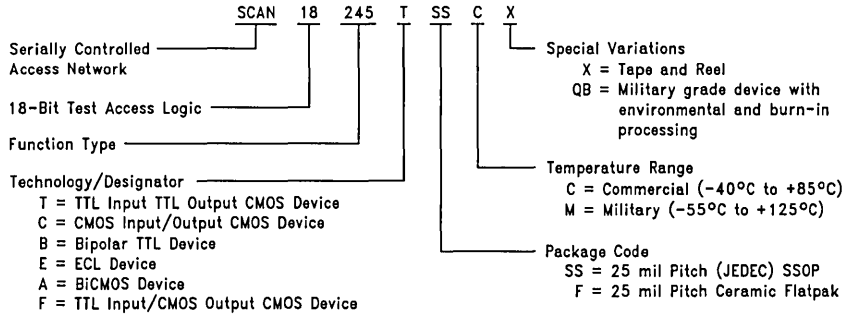
Ordering Information and Physical Dimensions

Section 11 Contents

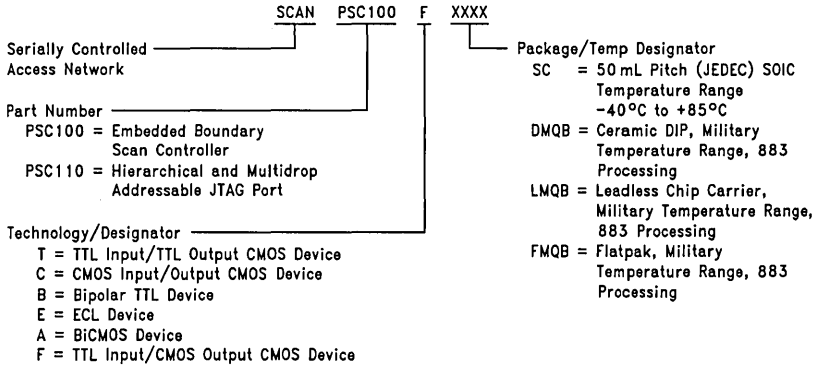
National Semiconductor

Ordering Information and Physical Dimensions

Ordering Information



TL/F/11596-9



TL/F/11596-10

SSOP Package Thermal Information

THERMAL RESISTANCE FOR SSOP PACKAGES

Package	Paddle Dimensions (mils)	θ_{JA} 0 LFPM (°C/W)	θ_{JA} 225 LFPM (°C/W)	θ_{JA} 500 LFPM (°C/W)	θ_{JA} 900 LFPM (°C/W)	θ_{JC}
20LD SSOP	110 x 144	127.0	99.4	90.1	78.5	N/A
24LD SSOP	98 x 106	117.0	91.4	82.7	73.5	N/A
24LD SSOP	120 x 150	100.8	81.3	72.1	65.7	25.7
48LD SSOP	190 x 190	75.5	58.0	51.5	44.0	21.5
56LD SSOP	190 x 190	67.8	53.0	47.4	42.1	18.5

THERMAL RESISTANCES FOR THE MILITARY FLATPAK PACKAGES

Package	Cavity Dimensions (mils)	θ_{JA} 0 LFPM (°C/W)	θ_{JA} 225 LFPM (°C/W)	θ_{JA} 500 LFPM (°C/W)	θ_{JA} 900 LFPM (°C/W)	θ_{JC}
48LD	250 x 250	74.4	58.1	50.0	43.9	6.6
56LD	250 x 250	59.8	47.9	39.0	35.1	3.4

Dry Pack

Dry Pack is moisture proof packing that is used to store SSOP devices to reduce the susceptibility of the "popcorn effect". Humidity collects inside the package by seeping through the plastic. If moisture is inside the device when the unit goes through a solder machine, the heat quickly changes the moisture to steam, and the pressurized steam pops open the package . . . thus the popcorn effect.

The Dry Pack bag is hermetically sealed and contains a small bag of desiccant which further helps to reduce moisture. All of the SCAN 56-pin SSOP devices will be shipped in Dry Pack bags. Included with the devices will be the following warning label and instructions for rebake:

Dry Pack Warning Label for Surface Mount Packages

National Semiconductor

ELECTROSTATIC
SENSITIVE DEVICES
Require Proper
Handling Procedures

CAUTION
This Bag Contains
MOISTURE SENSITIVE DEVICES

1. Shelf life in sealed bag: 24 months at <40°C and <90% Relative Humidity (RH).
2. Upon opening this bag, devices to be subjected to I.R., V.P.R. or equivalent process must be:
   a. Mounted within 48 hours at factory conditions of <30°C/60% RH, or
   b. Stored at <10% RH.
3. Devices require baking, before mounting, if:
   a. Humidity Indicator Card is >20% when read at 23°C ±5°C.
   b. 2a or 2b are not met.
4. If baking is required, devices may be baked for:
   a. 19 hours at 40°C +5°C/−0°C and <5% RH for low temperature device containers, or
   b. 8 hours at 125°C ±5°C for high temperature device containers.

Dry-Pack Seal Date: _____
(IF BLANK, SEE BAR CODE LABEL)

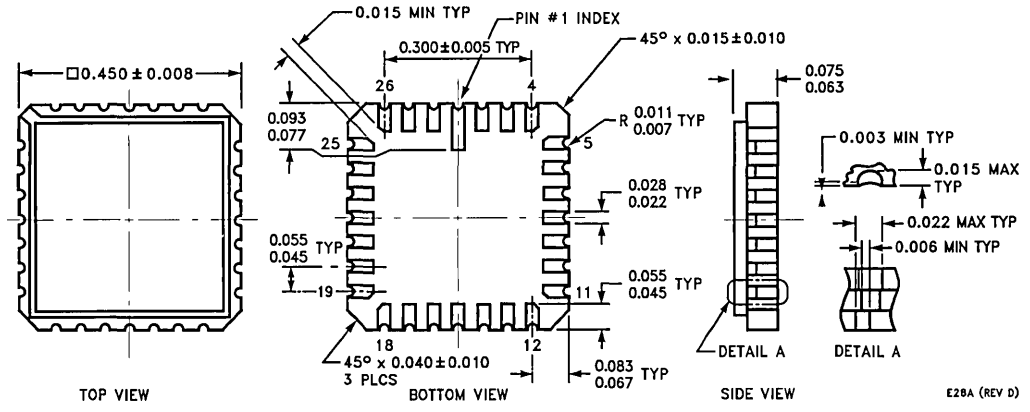
BAG SN 045317 MFR LOT No. C32729

Please follow these instructions carefully to avoid the popcorn effect.

National Semiconductor

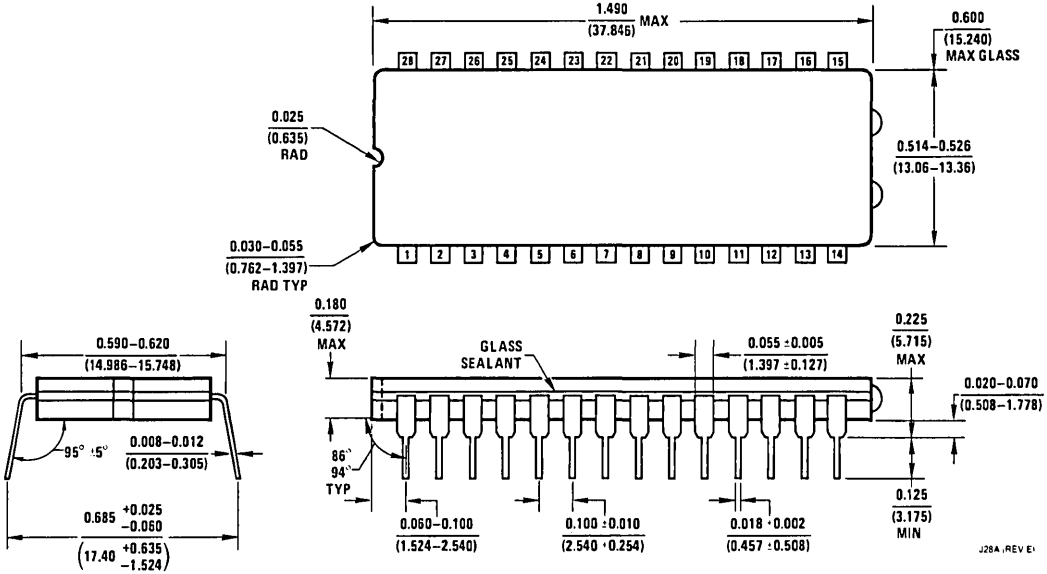
28 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E28A

All dimensions are in inches



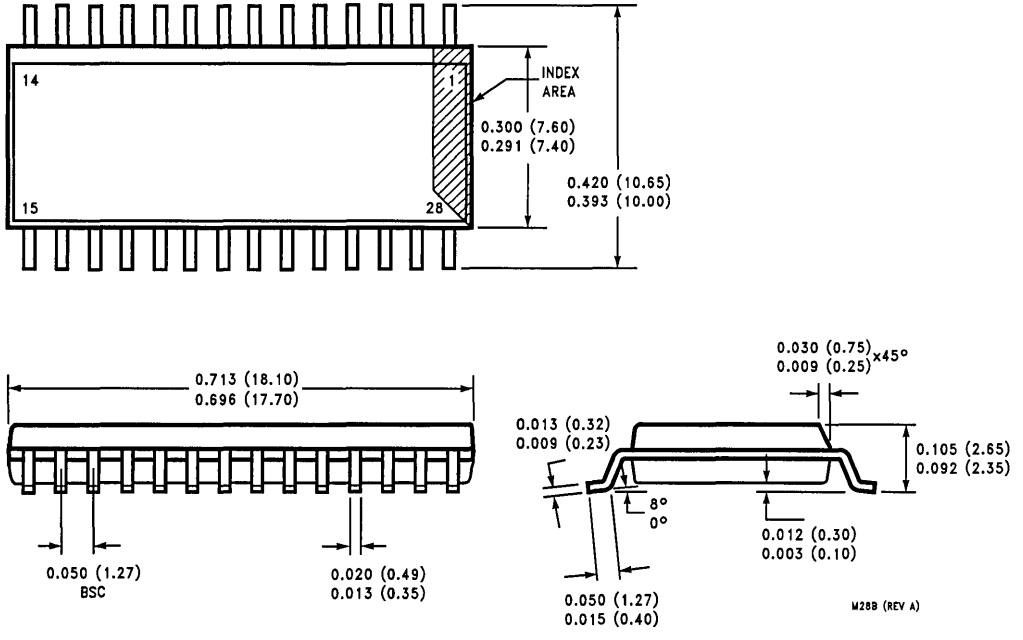
28 Lead Ceramic Dual-in-Line Package
NS Package Number J28A

All dimensions are in inches (millimeters)



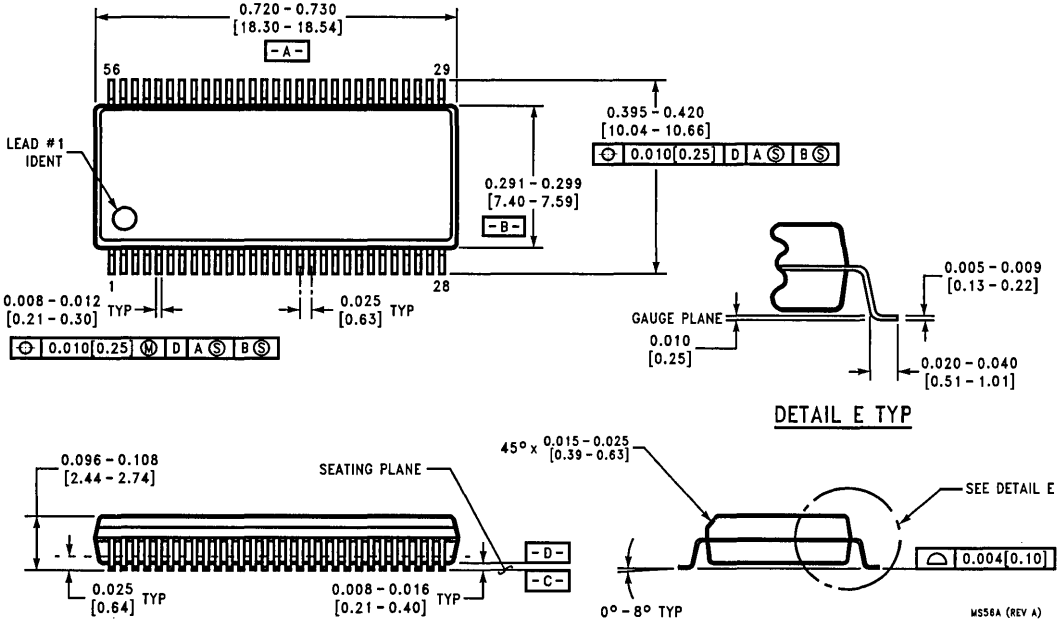
28 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M28B

All dimensions are in inches (millimeters)



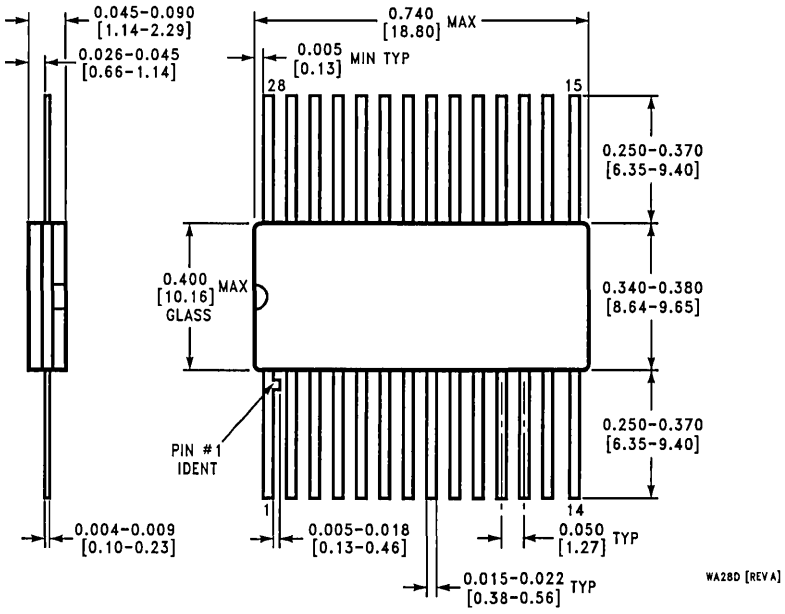
56 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS56A

All dimensions are in inches [millimeters]



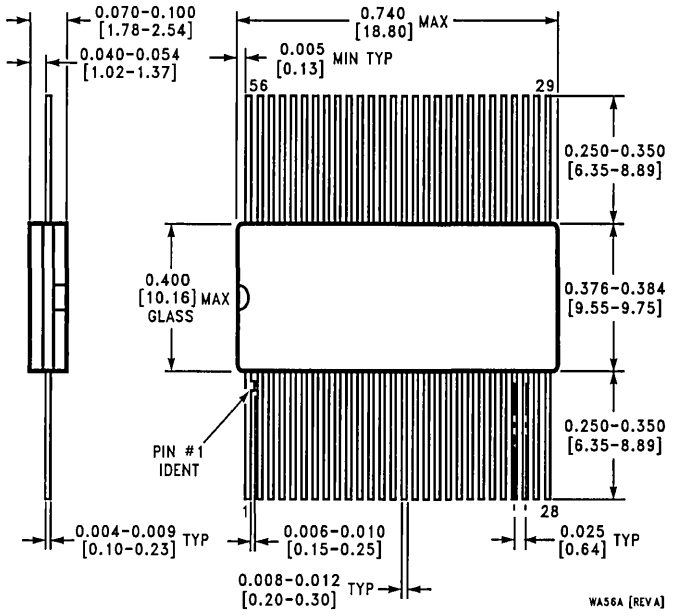
28 Lead Cerpack
NS Package Number WA28D

All dimensions are in inches [millimeters]



56 Lead Cerpack
NS Package Number WA56A

All dimensions are in inches [millimeters]



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National Semiconductor

Bookshelf of Technical Support Information

National Semiconductor Corporation recognizes the need to keep you informed about the availability of current technical literature.

This bookshelf is a compilation of books that are currently available. The listing that follows shows the publication year and section contents for each book.

For datasheets on new products and devices still in production but not found in a databook, please contact the National Semiconductor Customer Support Center at 1-800-272-9959.

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Please send them to:

Technical Communications Dept. M/S 16-300
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090

ADVANCED BiCMOS LOGIC (ABT, BiCMOS SCAN, LOW VOLTAGE BiCMOS, EXTENDED TTL TECHNOLOGY) DATABOOK—1996

ABT Description and Family Characteristics • ABT Ratings, Specifications and Waveforms
ABT Applications and Design Considerations • Quality and Reliability
SCAN18xxxA BiCMOS 5V Logic with Boundary Scan • 74LVT Low Voltage BiCMOS Logic
VME Extended TTL Technology for Backplanes • Advanced BiCMOS Clock Generation and Support

ADVANCED BIPOLAR LOGIC FAST®, FASTr™, ALS, AS DATABOOK—1995

Introduction to Advanced Bipolar Logic Families • FAST/FASTr/ALS/AS • Family Characteristics
Ratings, Specifications and Waveforms • Design Considerations • Datasheets • Ordering and Packaging Information

APPLICATION SPECIFIC ANALOG PRODUCTS DATABOOK—1995

Audio Circuits • Video Circuits • Automotive • Special Functions • Surface Mount

ASIC DESIGN MANUAL/GATE ARRAYS & STANDARD CELLS—1987

SSI/MSI Functions • Peripheral Functions • LSI/VLSI Functions • Design Guidelines • Packaging

CLOCK GENERATION AND SUPPORT (CGS) DESIGN DATABOOK—1995

Low Skew Clock Buffers/Drivers • Video Clock Generators • Low Skew PLL Clock Generators
Crystal Clock Oscillators

COP8™ DATABOOK—1994

COP8 Family • COP8 Applications • MICROWIRE/PLUS Peripherals • COP8 Development Support

CROSSVOLT™ LOW VOLTAGE LOGIC SERIES DATABOOK AND DESIGN GUIDE—1996

LCX Family • LVX Translator Family • LVX Bus Switch Family • LVX Family • LVQ Family • LVT Family
ALCX Family • GTL Family

DATA ACQUISITION DATABOOK—1995

Data Acquisition Systems • Analog-to-Digital Converters • Digital-to-Analog Converters • Voltage References
Temperature Sensors • Active Filters • Analog Switches/Multiplexers • Surface Mount

DATA ACQUISITION DATABOOK SUPPLEMENT—1992

New devices released since the printing of the 1989 Data Acquisition Linear Devices Databook.

DISCRETE SEMICONDUCTOR PRODUCTS DATABOOK—1989

Selection Guide and Cross Reference Guides • Diodes • Bipolar NPN Transistors
Bipolar PNP Transistors • JFET Transistors • Surface Mount Products • Pro-Electron Series
Consumer Series • Power Components • Transistor Datasheets • Process Characteristics

DRAM MANAGEMENT HANDBOOK—1993

Dynamic Memory Control • CPU Specific System Solutions • Error Detection and Correction
Microprocessor Applications

EMBEDDED CONTROLLERS DATABOOK—1992

COP400 Family • COP800 Family • COPS Applications • HPC Family • HPC Applications
MICROWIRE and MICROWIRE/PLUS Peripherals • Microcontroller Development Tools

ETHERNET DATABOOK—1996

Integrated Network Interface Controller Products • 10 Mb/s Physical Layer Transceivers and ENDECs
10 Mb/s Repeater Interface Controller Products • 100 Mb/s Fast Ethernet Protocol Products
Glossary and Acronyms

FDDI DATABOOK—1994

Datasheets • Application Notes

F100K ECL LOGIC DATABOOK & DESIGN GUIDE—1992

Family Overview • 300 Series (Low-Power) Datasheets • 100 Series Datasheets • 11C Datasheets
Design Guide • Circuit Basics • Logic Design • Transmission Line Concepts • System Considerations
Power Distribution and Thermal Considerations • Testing Techniques • 300 Series Package Qualification
Quality Assurance and Reliability • Application Notes

FACT™ ADVANCED CMOS LOGIC DATABOOK—1993

Description and Family Characteristics • Ratings, Specifications and Waveforms
Design Considerations • 54AC/74ACXXX • 54ACT/74ACTXXX • Quiet Series: 54ACQ/74ACQXXX
Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA/B

FAST® APPLICATIONS HANDBOOK—1990

Reprint of 1987 Fairchild FAST Applications Handbook
Contains application information on the FAST family: Introduction • Multiplexers • Decoders • Encoders
Operators • FIFOs • Counters • TTL Small Scale Integration • Line Driving and System Design
FAST Characteristics and Testing • Packaging Characteristics

HIGH-PERFORMANCE BUS INTERFACE DATABOOK—1994

QuickRing • Futurebus+/BTL Devices • BTL Transceiver Application Notes • Futurebus+ Application Notes
High Performance TTL Bus Drivers • PI-Bus • Futurebus+/BTL Reference

IBM DATA COMMUNICATIONS HANDBOOK—1992

IBM Data Communications • Application Notes

INTERFACE DATABOOK—1996

LVDS Circuits, Bus Circuits, Data Transmission Circuits, System Design Guide

LINEAR APPLICATIONS HANDBOOK—1994

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

LOW VOLTAGE DATABOOK—1992

This databook contains information on National's expanding portfolio of low and extended voltage products. Product datasheets included for: Low Voltage Logic (LVQ), Linear, EPROM, EEPROM, SRAM, Interface, ASIC, Embedded Controllers, Real Time Clocks, and Clock Generation and Support (CGS).

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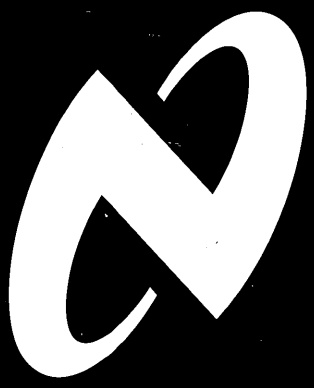

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