TTL DATA BOOK

National

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FEB 1976

National

National Semiconductor

TTL DATA BOOK

Section 1 - 54/74 SSI DEVICES
Connection Diagrams • Electrical Tables

Section 2 - 54/74 MSI DEVICES

Section 3 - National Semiconductor PROPRIETARY DEVICES

Section 4 - National Semiconductor ADDITIONAL DEVICES

NATIONAL

Alpha-Numerical Index

Note: When there are two sets of page numbers, the first designates the connection diagram page; the second indicates electrical tables.

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TTL Data Book — Alpha-Numerical Index

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54/74 SSI—SECTION 1

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54/74 MSI—SECTION 2

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PROPRIETARY–SECTION 3

ADDITIONAL DEVICES—SECTION 4

PARAMETER(1)			DM54/74 00 MIN	DM54/74 00 TYP	DM54/74 00 MAX	DM54H/74H H00 MIN	DM54H/74H H00 TYP	DM54H/74H H00 MAX	DM54L/74L L00 MIN	DM54L/74L L00 TYP	DM54L/74L L00 MAX	DM54LS/74LS LS00 MIN	DM54LS/74LS LS00 TYP	DM54LS/74LS LS00 MAX	DM54S/74S S00 MIN	DM54S/74S S00 TYP	DM54S/74S S00 MAX	UNITS
I_{OH}	High Level Output Current				−400			−500			−200			−400			−1000	μA
V_{OH}	High Level Output Voltage	DM54	2.4 @ 400μA			2.4 @ 500μA			2.4 @ 200μA			2.5 @ 400μA			2.5 @ 1000μA			V
		DM74	2.4 @ 400μA			2.4 @ 500μA			2.4 @ 200μA			2.7 @ 400μA			2.7 @ 1000μA			V
I_{OL}	Low Level Output Current	DM54			16			20			2			4			20	mA
		DM74			16			20			3.6			8			20	mA
V_{OL}	Low Level Output Voltage	DM54			0.4 @ 16 mA			0.4 @ 20 mA			0.3 @ 2 mA			0.4 @ 4 mA			0.5 @ 20 mA	V
		DM74			0.4 @ 16 mA			0.4 @ 20 mA			0.4 @ 3.6 mA			0.5 @ 8 mA			0.5 @ 20 mA	V
I_{IH}	High Level Input Current				40 @ 2.4V			50 @ 2.4V			10 @ 2.4V			20 @ 2.7V			50 @ 2.7V	μA
I_{IL}	Low Level Input Current				−1.6 @ 0.4V			−2.0 @ 0.4V			−0.18 @ 0.3V			−0.36 @ 0.4V			−2.0 @ 0.5V	mA
I_{OS}	Short Circuit Output Current		−20		−55	−40		−100	−3		−15	−30		−130	−40		−100	mA
I_{CCH}	Supply Current (Average per Gate)			1.0			2.5			0.11			0.2			2.5		mA
t_{PHL}	Turn "ON" Time			7	15		6.2	10		31	60		10	15		3	5	ns
t_{PLH}	Turn "OFF" Time			11	22		5.9	10		35	60		9	15		3	4.5	ns

Notes

(1) The 00 gate parameters were used in all cases.

(2) The product families below will drive the indicated number of loads of each of the above products.

FANOUT CAPABILITIES(2)	DM54/74 00 MIN	DM54H/74H H00 MIN	DM54L/74L L00 MIN	DM54LS/74LS LS00 MIN	DM54S/74S S00 MIN
Series DM54/74	10	8	40	20	8
Series DM54H/74H	12	10	50	25	10
Series DM54L/74L	2	1	20	10	1
Series DM54LS/74LS	5	4	40	20	4
Series DM54S/74S	12	10	100	50	10

This list is intended to give National replacements for competitors' parts not using the 54/74 numbering system.

Only the basic circuit numbers are cross referenced. As the pin-out sometimes varies between a flat package part and the equivalent DIP part, it is recommended that the manufacturer's specifications be consulted prior to specifying a direct replacement. Other than parts offered only in a flat package, the dual-in-line pin-outs were used as a guide in preparing the following cross references.

Direct Replacements were selected as pin-for-pin equivalent circuits based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in any particular application is not necessarily guaranteed. Before using a substitute, the user should compare the specifications of the substitute device with the detailed specifications of the original device.

National Semiconductor makes no warranty as to the information furnished, and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

DEVICE TYPE	NATIONAL DIRECT REPLACEMENT
AMD	
AM2502	DM2502/2502C
AM25L02	DM2502/2502C
AM2503	DM2503/2503C
AM25L03	DM2503/2503C
AM2504	DM2504/2504C
AM25L04	DM2504/2504C
AM25LS138	DM54LS138/74LS138
AM25LS139	DM54LS139/74LS139
AM25LS151	DM54LS151/74LS151
AM25LS153	DM54LS153/74LS153
AM25LS157	DM54LS157/74LS157
AM25LS158	DM54LS158/74LS158
AM25LS160	DM54LS160/74LS160
AM25LS161	DM54LS161/74LS161
AM25LS162	DM54LS162/74LS162
AM25LS163	DM54LS163/74LS163
AM25LS164	DM54LS164/74LS164
AM25LS174	DM54LS174/74LS174
AM25LS175	DM54LS175/74LS175
AM25LS181	DM54181/74181
AM25LS190	DM54LS190/74LS190
AM25LS191	DM54LS191/74LS191
AM25LS192	DM54LS192/74LS192
AM25LS193	DM54LS193/74LS193
AM25LS194A	DM54LS194A/74LS194A
AM25LS195A	DM54LS195A/74LS195A
AM25LS251	DM54LS251/74LS251
AM25LS253	DM54LS253/74LS253
AM25LS257	DM54LS257/74LS257
AM25LS258	DM54LS258/74LS258
AM2602	DM9602/8602
AM26L02	DM9602/8602
AM26S02	DM9602/8602
AM26123	DM54123/74123
AM26L123	DM54L123A/74L123A
AM93L60	DM75L60/85L60
AM93L66	DM75L63/85L63
Fairchild	
930	DM930
932	DM932
Fairchild (con't)	
933	DM933
935	DM935
936	DM936
937	DM937
944	DM944
945	DM945
946	DM946
948	DM948
949	DM949
961	DM961
962	DM962
963	DM963
9002	DM9002C
9003	DM9003C
9004	DM9004C
9005	DM9005C
9006	DM9006C
9008	DM9008C
9009	DM9009C
9012	DM9012C
9016	DM9016C
9024	DM9024/8024
9093	DM9093
9094	DM9094
9097	DM9097
9099	DM9099
9135	DM935
9157	DM957
9158	DM958
9300	DM9300/8300
9301	DM9301/8301
9307	DM5448/7448
9309	DM9309/8309
9310	DM9310/8310
9311	DM9311/8311
9312	DM9312/8312
9315	DM5441A/7441A
9316	DM9316/8316

DEVICE TYPE	NATIONAL DIRECT REPLACEMENT
Fairchild (con't)	
9317B	DM5447A/7447A
9317C	DM5446A/7446A
9318	DM9318/8318
9321	DM54LS139/74LS139
9322	DM9322/8322
9325	DM54141/74141
9341	DM54181/74181
9342	DM54182/74182
9345	DM5445/7445
9352	DM5442/7442
9357A	DM5446A/7446A
9357B	DM5447A/7447A
9358	DM5448/7448
9360	DM54192/74192
9366	DM54193/74193
9375	DM5475/7475
9377	DM54LS77/74LS77
9383	DM5483/7483
9385	DM5485/7485
9390	DM5490/7490
9391	DM5491A/7491A
9392	DM5492/7492
9393	DM5493/7493
9395	DM5495/7495
9396	DM5496/7496
9601	DM9601/8601
9602	DM9602/8602
9603	DM54121/74121
93141	DM54141/74141
93145	DM54145/74145
93150	DM54150/74150
93151	DM54151A/74151A
93153	DM54153/74153
93155	DM54155/74155
93156	DM54156/74156
93157	DM54157/74157
93160	DM54160A/74160A
93161	DM54161A/74161A
93162	DM54162A/74162A
93163	DM54163A/74163A
93164	DM54164/74164
93165	DM54165/74165
93166	DM54166/74166
93170	DM74170
93174	DM54174/74174
93175	DM54175/74175
93176	DM54176/74176
93177	DM54177/74177
93180	DM54180/74180
93190	DM54190/74190
93191	DM54191/74191
93194	DM54194/74194
93195	DM54195/74195
93196	DM54196/74196

DEVICE TYPE	NATIONAL DIRECT REPLACEMENT
Fairchild (con't)	
93197	DM54197/74197
93198	DM54198/74198
93199	DM54199/74199
9H00	DM54H00/74H00
9H01	DM54H01/74H01
9H04	DM54H04/74H04
9H05	DM54H05/74H05
9H08	DM54H08/74H08
9H10	DM54H10/74H10
9H11	DM54H11/74H11
9H20	DM54H20/74H20
9H21	DM54H21/74H21
9H22	DM54H22/74H22
9H30	DM54H30/74H30
9H40	DM54H40/74H40
9H50	DM54H50/74H50
9H51	DM54H51/74H51
9H52	DM54H52/74H52
9H53	DM54H53/74H53
9H54	DM54H54/74H54
9H55	DM54H55/74H55
9H60	DM54H60/74H60
9H61	DM54H61/74H61
9H62	DM54H62/74H62
9H71	DM54H71/74H71
9H72	DM54H72/74H72
9H73	DM54H73/74H73
9H74	DM54H74/74H74
9H76	DM54H76/74H76
9H78	DM54H78/74H78
9H103	DM54H103/74H103
9H106	DM54H106/74H106
9H108	DM54H108/74H108
93H00	DM54LS195A/74LS195A
9L00*	DM54L00/74L00
9L04*	DM54L04/74L04
9L24*	DM9024/8024
9L54*	DM54L54/74L54
9L86*	DM5486/7486
93L00*	DM54LS195A/74LS195A
93L01*	DM9301/8301
93L09*	DM9309/8309
93L10*	DM76L75/86L75
93L11*	DM54L154A/74L154A
93L12*	DM9312/8312
93L16*	DM76L76/86L76
93L18*	DM9318/8318
93L22*	DM54L157A/74L157A
93L34*	DM9334/8334
93L41*	DM54181/74181
96L02*	DM9602/8602

*The National Low Power circuits are "True Tenth Power," whereas the Fairchild circuits are not.

DEVICE TYPE	NATIONAL DIRECT REPLACEMENT
Fairchild (con't)	
9LS00	DM54LS00/74LS00
9LS02	DM54LS02/74LS02
9LS03	DM54LS03/74LS03
9LS04	DM54LS04/74LS04
9LS05	DM54LS05/74LS05
9LS08	DM54LS08/74LS08
9LS09	DM54LS09/74LS09
9LS10	DM54LS10/74LS10
9LS11	DM54LS11/74LS11
9LS14	DM54LS14/74LS14
9LS15	DM54LS15/74LS15
9LS20	DM54LS20/74LS20
9LS21	DM54LS21/74LS21
9LS22	DM54LS22/74LS22
9LS27	DM54LS27/74LS27
9LS30	DM54LS30/74LS30
9LS32	DM54LS32/74LS32
9LS37	DM54LS37/74LS37
9LS38	DM54LS38/74LS38
9LS40	DM54LS40/74LS40
9LS42	DM54LS42/74LS42
9LS51	DM54LS51/74LS51
9LS54	DM54LS54/74LS54
9LS55	DM54LS55/74LS55
9LS73	DM54LS73/74LS73
9LS74	DM54LS74/74LS74
9LS83	DM54LS83A/74LS83A
9LS86	DM54LS86/74LS86
9LS90	DM54LS90/74LS90
9LS92	DM54LS92/74LS92
9LS93	DM54LS93/74LS93
9LS95	DM54LS95B/74LS95B
9LS109	DM54LS109/74LS109
9LS112	DM54LS112/74LS112
9LS113	DM54LS113/74LS113
9LS114	DM54LS114/74LS114
9LS125	DM54LS125/74LS125
9LS126	DM54LS126/74LS126
9LS132	DM54LS132/74LS132
9LS133	DM74S133
9LS136	DM54LS136/74LS136
9LS138	DM54LS138/74LS138
9LS139	DM54LS139/74LS139
9LS151	DM54LS151/74LS151
9LS153	DM54LS153/74LS153
9LS155	DM54LS155/74LS155
9LS156	DM54LS156/74LS156
9LS157	DM54LS157/74LS157
9LS158	DM54LS158/74LS158
9LS160	DM54LS160/74LS160
9LS161	DM54LS161/74LS161
9LS162	DM54LS162/74LS162
9LS163	DM54LS163/74LS163
9LS164	DM54LS164/74LS164
9LS170	DM54LS170/74LS170
9LS174	DM54LS174/74LS174
Fairchild (con't)	
9LS175	DM54LS175/74LS175
9LS181	DM54181/74181
9LS190	DM54LS190/74LS190
9LS191	DM54LS191/74LS191
9LS192	DM54LS192/74LS192
9LS193	DM54LS193/74LS193
9LS194	DM54LS194A/74LS194A
9LS195	DM54LS195A/74LS195A
9LS196	DM54LS196/74LS196
9LS197	DM54LS197/74LS197
9LS251	DM54LS251/74LS251
9LS253	DM54LS253/74LS253
9LS257	DM54LS257/74LS257
9LS258	DM54LS258/74LS258
9LS259	DM9334/8334
9LS266	DM54LS266/74LS266
9LS279	DM54LS279/74LS279
9LS283	DM54LS283/74LS283
9LS295	DM54LS295A/74LS295A
9LS298	DM54LS298/74LS298
9LS365	DM54LS365/74LS365
9LS366	DM54LS366/74LS366
9LS367	DM54LS367/74LS367
9LS368	DM54LS368/74LS368
9LS670	DM54LS670/74LS670
9N00	DM5400/7400
9N01	DM5401/7401
9N02	DM5402/7402
9N03	DM5403/7403
9N04	DM5404/7404
9N05	DM5405/7405
9N06	DM5406/7406
9N07	DM5407/7407
9N08	DM5408/7408
9N09	DM5409/7409
9N10	DM5410/7410
9N11	DM5411/7411
9N12	DM54LS12/74LS12
9N13	DM5413/7413
9N14	DM5414/7414
9N16	DM5416/7416
9N17	DM5417/7417
9N20	DM5420/7420
9N21	DM54LS21/74LS21
9N23	DM5423/7423
9N25	DM5425/7425
9N26	DM5426/7426
9N27	DM5427/7427
9N30	DM5430/7430
9N32	DM5432/7432
9N37	DM5437/7437
9N38	DM5438/7438
9N39	DM5401/7401
9N40	DM5440/7440
9N50	DM5450/7450

*The National Low Power circuits are "True Tenth Power," whereas the Fairchild circuits are not.

DEVICE TYPE	NATIONAL DIRECT REPLACEMENT
Fairchild (con't)	
9N51	DM5451/7451
9N53	DM5453/7453
9N54	DM5454/7454
9N60	DM5460/7460
9N70	DM5470/7470
9N72	DM5472/7472
9N73	DM5473/7473
9N74	DM5474/7474
9N76	DM5476/7476
9N86	DM5486/7486
9N107	DM54107/74107
9N122	DM54LS122/74LS122
9N123	DM54123/74123
9N132	DM54132/74132
9N279	DM54LS279/74LS279
9S00	DM74S00
9S02	DM74S02
9S03	DM74S03
9S04A	DM74S04
9S05A	DM74S05
9S08	DM74LS08
9S09	DM74LS09
9S10	DM74S10
9S11	DM74S11
9S15	DM74S15
9S20	DM74S20
9S22	DM74S22
9S30	DM74S30
9S32	DM74LS32
9S40	DM74S40
9S51	DM74S51
9S64	DM74S64
9S65	DM74S65
9S74	DM74S74
9S86	DM74S86
9S109	DM74LS109
9S112	DM74S112
9S113	DM74S113
9S114	DM74S114
9S132	DM54LS132/74LS132
9S133	DM74S133
9S134	DM74S134
9S135	DM74S135
9S140	DM74S140
93S00	DM74S195
93S10	DM54LS160/74LS160
93S12	DM9312/8312
93S16	DM54LS161/74LS161
93S21	DM74S139
93S22	DM74S157
93S41	DM54181/74181
93S42	DM74S182
93S46	DM7160/8160
93S47	DM7160/8160

DEVICE TYPE	NATIONAL DIRECT REPLACEMENT
Fairchild (con't)	
93S138	DM74S138
93S139	DM74S139
93S151	DM74S151
93S153	DM74S153
93S157	DM74S157
93S158	DM74S158
93S174	DM74S174
93S175	DM74S175
93S194	DM74S194
93S251	DM74S251
93S253	DM74S253
93S257	DM74S257
93S258	DM74S258
96S02	DM9602/8602
Motorola	
MC830	DM930
MC832	DM932
MC833	DM933
MC836	DM936
MC837	DM937
MC840	DM935
MC844	DM944
MC845	DM945
MC846	DM946
MC848	DM948
MC849	DM949
MC852	DM9099
MC853	DM9093
MC855	DM9097
MC856	DM9094
MC857	DM957
MC858	DM958
MC861	DM961
MC862	DM962
MC863	DM963
MC1800	DM1800
MC1801	DM1801
Signetics	
8230	DM9312/8312
82S30	DM9312/8312
8241	DM54LS386/74LS386
82S41	DM54LS386/74LS386
8252	DM9301/8301
82S52	DM9301/8301
8269	DM7200/8200
8280	DM7280/8280
82S80	DM54LS196/74LS196
8281	DM7281/8281
82S81	DM54LS197/74LS197
8290	DM7290/8290
82S90	DM54LS196/74LS196
8291	DM7291/8291

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DEVICE TYPE	NATIONAL DIRECT REPLACEMENT
Signetics (con't)	
82S91	DM54LS197/74LS197
8292	DM54LS196/74LS196
8293	DM54LS197/74LS197
82147	DM54147/74147
82148	DM54148/74148
8415	DM1800
8455	DM5440/7440
8470	DM5410/7410
8471	DM54LS12/74LS12
8480	DM5400/7400
8481	DM5403/7403
8490	DM5404/7404
8806	DM5460/7460
8808	DM5430/7430
8815	DM5425/7425
8828	DM5474/7474
8840	DM5451/7451
8848	DM54LS54/74LS54
8859	DM5440/7440
8875	DM5427/7427
8881	DM5401/7401
8890	DM5404/7404
8891	DM5405/7405
8H16	DM54H20/74H20
8H70	DM54H10/74H10
8H80	DM54H00/74H00
8H90	DM54H04/74H04
8T10	DM7551/8551
8T22	DM9601/8601
8T54	DM5448/7448
8T95	DM7095/8095
8T96	DM7096/8096
8T97	DM7097/8097
8T98	DM7098/8098
TI	
SN15830	DM930
SN15832	DM932
SN15833	DM933
SN15835	DM935
SN15836	DM936
SN15837	DM937
SN15844	DM944
SN15845	DM945
SN15846	DM946

DEVICE TYPE	NATIONAL DIRECT REPLACEMENT
TI (con't)	
SN15848	DM948
SN15849	DM949
SN15857	DM957
SN15858	DM958
SN15861	DM961
SN15862	DM962
SN15863	DM963
SN151800	DM1800
SN151801	DM1801
SN158093	DM9093
SN158094	DM9094
SN158097	DM9097
SN158099	DM9099
SN29002	DM9002C
SN29003	DM9003C
SN29004	DM9004C
SN29005	DM9005C
SN29006	DM9006C
SN29008	DM9008C
SN29009	DM9009C
SN29012	DM9012C
SN29016	DM9016C
SN29024	DM8024
SN29300	DM8300
SN29301	DM8301
SN29309	DM8309
SN29310	DM8310
SN29311	DM8311
SN29312	DM8312
SN29316	DM8316
SN29318	DM8318
SN29322	DM8322
SN29334	DM8334
SN29601	DM8601
SN29602	DM8602
SN39024	DM9024
SN39300	DM9300
SN39301	DM9301
SN39309	DM9309
SN39310	DM9310
SN39311	DM9311
SN39312	DM9312
SN39316	DM9316
SN39318	DM9318
SN39322	DM9322
SN39334	DM9334
SN39601	DM9601
SN39602	DM9602

The following pages contain functional indexes and selection guides designed to simplify the choice of a particular function to fit a specific application. Essential characteristics of similar or like functions are grouped for comparative analysis, and the electrical specifications are referenced by page number. The following categories of functions are covered:

SSI FUNCTIONS

MSI FUNCTIONS

AND GATES WITH TOTEM-POLE OUTPUTS

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Dual 4-Input AND Gates	8.2 ns	40 mW	54H21	J,N	74H21	J,N	1-7	1-44
	12 ns	4.25 mW	54LS21	J,N,W	74LS21	J,N	1-7	1-44
Triple 3-Input AND Gates	4.75 ns	31 mW			74S11	N	1-5	1-44
	8.2 ns	40 mW	54H11	J,N	74H11	J,N	1-5	1-44
	12 ns	4.25 mW	54LS11	J,N,W	74LS11	J,N	1-5	1-44
Quad 2-Input AND Gates	12 ns	4.25 mW	54LS08	J,N,W	74LS08	J,N	1-4	1-44
	15 ns	19 mW	5408	J,N,W	7408	J,N	1-4	1-44

AND GATES WITH OPEN-COLLECTOR OUTPUTS

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Triple 3-Input AND Gates	6 ns	28 mW			74S15	N	1-6	1-46
	20 ns	4.25 mW	54LS15	J,N,W	74LS15	J,N	1-6	1-46
Quad 2-Input AND Gates	18.5 ns	19.4 mW	5409	J,N,W	7409	J,N	1-4	1-46
	20 ns	4.25 mW	54LS09	J,N,W	74LS09	J,N	1-4	1-46

AND-OR-INVERT GATES WITH TOTEM-POLE OUTPUTS

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
2-Wide 4-Input	12.5 ns	2.75 mW	54LS55	J,N,W	74LS55	J,N	1-15	1-56
	43 ns	1.5 mW	54L55	J,N,W	74L55	J,N	1-15	1-56
Dual 2-Wide 2-Input	3.5 ns	28 mW			74S51	N	1-12	1-56
	6.5 ns	29 mW	54H51	J,N	74H51	J,N	1-12	1-56
	10.5 ns	14 mW	5451	J,N,W	7451	J,N	1-12	1-56
	12.5 ns	2.75 mW	54LS51	J,N,W	74LS51	J,N	1-12	1-56
	43 ns	1.5 mW	54L51	J,N,W	74L51	J,N	1-12	1-56
4-Wide 4-2-3-2-Input	3.5 ns	29 mW			74S64	N	1-16	1-56
4-Wide 2-2-3-2-Input	6.6 ns	41 mW	54H54	J,N	74H54	J,N	1-14	1-56
4-Wide 2-Input	10.5 ns	23 mW	5454	J,N,W	7454	J,N	1-14	1-56
4-Wide 2-3-3-2-Input	12.5 ns	4.5 mW	54LS54	J,N,W	74LS54	J,N	1-14	1-56
4-Wide 2-3-3-2-Input	43 ns	1.5 mW	54L54	J,N,W	74L54	J,N	1-14	1-56

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package: Mil.		Coml.		Connection Diagram Page No.	Electrical Tables Page No.
4-Wide 4-2-3-2-Input	5.5 ns	36 mW			74S65	N	1-17	1-61

BUFFERS/CLOCK DRIVERS WITH TOTEM-POLE OUTPUTS (ALSO SEE CLOCK GENERATOR CIRCUITS)

Description	Low-Level Output Current	High-Level Output Current	Typ. Delay Time	Typ. Power Per Gate	Device Type and Package: Mil.		Coml.		Connection Diagram Page No.	Electrical Tables Page No.
Dual 4-Input NAND Buffers	60 mA	−3 mA	4 ns	44 mW			74S40	N	1-11	1-54
	60 mA	−1.5 mA	7.5 ns	44 mW	54H40	J,N	74H40	J,N	1-11	1-54
	48 mA	−1.2 mA	10.5 ns	26 mW	5440	J,N,W	7440	J,N	1-11	1-54
	24 mA	−1.2 mA	12 ns	4.3 mW			74LS40	J,N	1-11	1-54
	12 mA	−1.2 mA	12 ns	4.3 mW	54LS40	J,N,W			1-11	1-54
Quad 2-Input NAND Buffers	48 mA	−1.2 mA	10 ns	25 mW	7091	J,N,W	8091	J,N	3-3	3-4
	48 mA	−1.2 mA	10.5 ns	27 mW	5437	J,N,W	7437	J,N	1-10	1-54
	24 mA	−1.2 mA	12 ns	4.3 mW			74LS37	J,N	1-10	1-54
	12 mA	−1.2 mA	12 ns	4.3 mW	54LS37	J,N,W			1-10	1-54

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

Description	High-Level Output Voltage	Low-Level Output Current	Typ. Delay Time	Typ. Power Per Gate	Device Type and Package: Mil.		Coml.		Connection Diagram Page No.	Electrical Tables Page No.
Quad 2-Input NAND Buffers	15V	16 mA	13.5 ns	10 mW	5426	J,N	7426	J,N	1-9	1-42
	15V	8 mA	16 ns	2 mW			74LS26	J,N	1-9	1-42
	15V	4 mA	16 ns	2 mW	54LS26	J,N,W			1-9	1-42
	5.5V	48 mA	12.5 ns	24.4 mW	5438	J,N,W	7438	J,N	1-10	1-42
	5.5V	24 mA	19 ns	4.3 mW			74LS38	J,N	1-10	1-42
	5.5V	12 mA	19 ns	4.3 mW	54LS38	J,N,W			1-10	1-42
Hex Buffers/Drivers	30V	40 mA	13 ns	21 mW			7407	J,N	1-3	1-42
	30V	30 mA	13 ns	21 mW	5407	J,N,W			1-3	1-42
	15V	40 mA	13 ns	21 mW			7417	J,N	1-7	1-42
	15V	30 mA	13 ns	21 mW	5417	J,N,W			1-7	1-42
Hex Inverter Buffers/ Drivers	30V	40 mA	12.5 ns	26 mW			7406	J,N	1-3	1-42
	30V	30 mA	12.5 ns	26 mW	5406	J,N,W			1-3	1-42
	15V	40 mA	12.5 ns	26 mW			7416	J,N	1-6	1-42
	15V	30 mA	12.5 ns	26 mW	5416	J,N,W			1-6	1-42

BUS INTERFACE GATES WITH TRI-STATE TOTEM-POLE OUTPUTS

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Quad Bus Buffers	10 ns	40 mW	54125	J,N,W	74125	J,N	1-27	1-80
	10 ns	45 mW	54126	J,N,W	74126	J,N	1-27	1-80
	10 ns	40 mW	7093	J,N,W	8093	J,N	3-5	3-6
	10 ns	45 mW	7094	J,N,W	8094	J,N	3-5	3-6
	9 ns	30 mW	7099	J,N,W	8099	J,N	3-9	3-10
Hex Bus Drivers	12 ns	54 mW	54365	J,W	74365	J,N	1-32	1-86
	12 ns	54 mW	54367	J,W	74367	J,N	1-32	1-86
	12 ns	54 mW	7095	J,W	8095	J,N	3-7	3-8
	12 ns	54 mW	7097	J,W	8097	J,N	3-7	3 8
	33 ns	3.3 mW	70L95	J,N,W	80L95	J,N	3-7	3-8
	33 ns	3.3 mW	70L97	J,N,W	80L97	J,N	3-7	3-8
Hex Inverter Bus Drivers	11 ns	49 mW	54366	J,W	74366	J,N	1-32	1-86
	11 ns	49 mW	54368	J,W	74368	J,N	1-33	1-86
	11 ns	49 mW	7096	J,W	8096	J,N	3-7	3-8
	11 ns	49 mW	7098	J,W	8098	J,N	3-7	3-8
	30 ns	2.5 mW	70L96	J,N,W	80L96	J,N	3-7	3-8
	30 ns	2.5 mW	70L98	J,N,W	80L98	J,N	3-7	3-8
Octal Drivers	13 ns	10 mW	71LS95	N	81LS95	N	3-21	3-22
	13 ns	10 mW	71LS97	N	81LS97	N	3-21	3-22
Octal Inverter Drivers	9.5 ns	8 mW	71LS96	N	81LS96	N	3-21	3-22
	9.5 ns	8 mW	71LS98	N	81LS98	N	3-21	3-22
12-Input NAND Gates	4.5 ns	45 mW			74S134	N	1-28	1-80

CLOCK GENERATORS

Description	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
		Mil.		Coml.			
Dual Voltage-Controlled Oscillators	90 mW	54LS124	J,N,W	74LS124	J,N	2-44	2-45

EXPANDABLE GATES

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
2-Wide AND-OR-INVERT Gates	6.8 ns	30 mW	54H55	J,N	74H55	J,N	1-15	1-50
Dual 2-Wide AND-OR-INVERT Gates	6.5 ns	29 mW	54H50	J,N	74H50	J,N	1-11	1-50
	10.5 ns	14 mW	5450	J,N,W	7450	J,N	1-11	1-50
4-Wide AND-OR Gates	9.9 ns	88 mW	54H52	J,N	74H52	J,N	1-13	1-50
4-Wide AND-OR-INVERT Gates	6.6 ns	41 mW	54H53	J,N	74H53	J,N	1-13	1-50
	10.5 ns	23 mW	5453	J,N,W	7453	J,N	1-13	1-50
Dual 4-Input NOR Gates With Strobe	10.5 ns	23 mW	5423	J,N,W	7423	J,N	1-8	1-50

EXPANDERS

Description	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
		Mil.		Coml.			
Dual 4-Input Expanders	4 mW	5460	J,N,W	7460	J,N	1-15	1-58
	6 mW	54H60	J,N	74H60	J,N	1-15	1-59
3-2-2-3-Input AND-OR Expanders	25 mW	54H62	J,N	74H62	J,N	1-16	1-59
Triple 3-Input Expanders	13 mW	54H61	J,N	74H61	J,N	1-16	1-60

FLIP-FLOPS, GATED

Typ. Characteristics		Data Times		Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
f_{MAX} (MHz)	Pwr/F-F (mW)	Setup (ns)	Hold (ns)	Mil.		Coml.			
45	105	15	0	7511	J,N,W	8511	J,N	3-40	3-41
30	73	24	0	7613	J,N,W	8613	J,N	3-40	3-41
28	110	15	0	7512	J,N,W	8512	J,N	3-40	3-41
10	8.0	110	0	75L12	J,N,W	85L12	J,N	3-40	3-41
9	9.3	80	0	75L11	J,N,W	85L11	J,N	3-40	3-41
7	7.3	100	0	76L13	J,N,W	86L13	J,N	3-40	3-41

FLIP-FLOPS, SINGLE AND DUAL J-K EDGE TRIGGERED

Dwg. Ref.	Typ. Characteristics		Data Times		Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
	f_{MAX} (MHz)	Pwr/F-F (mW)	Setup (ns)	Hold (ns)	Mil.		Coml.			
A	125	75	6↓	0↓			74S112	N	1-24	1-70
	50	100	13↓	0↓	54H106	J,N	74H106	J,N	1-23	1 74
	45	10	20↓	0↓	54LS76	J,N,W	74LS76	N	1-21	1-68
	45	10	20↓	0↓	54LS112	J,N,W	74LS112	J,N	1-24	1-68
B	125	75	6↓	0↓			74S114	N	1-25	1-70
	50	100	13↓	0↓	54H108	J,N	74H108	J,N	1-24	1-74
	45	10	20↓	0↓	54LS78	J,N,W	74LS78	J,N	1-21	1-68
	45	10	20↓	0↓	54LS114	J,N,W	74LS114	J,N	1-25	1-68
C	125	75	6↓	0↓			74S113	N	1-25	1-70
	45	10	20↓	0↓	54LS113	J,N,W	74LS113	J,N	1-25	1-68
D	50	100	13↓	0↓	54H103	J,N	74H103	J,N	1-23	1-74
	45	10	20↓	0↓	54LS73	J,N,W	74LS73	J,N	1-20	1-68
	45	10	20↓	0↓	54LS107	J,N	74LS107	J,N	1-23	1-68
E	40	45	15↑	10↑	9024	J,N,W	8024	J,N	4-17	4-17
	33	10	20↑	5↑	54LS109	J,N,W	74LS109	J,N	1-24	1-68
	33	45	10↑	6↑	54109	J,N,W	74109	J,N	1-24	1-62
F	35	65	20↑	5↑	5470	J,N,W	7470	J,N	1-18	1-62

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

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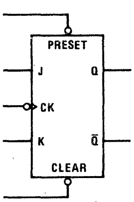

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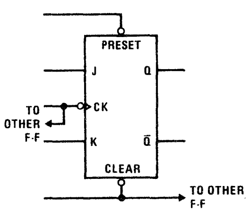

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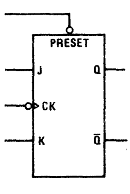

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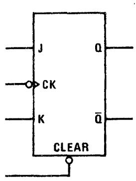

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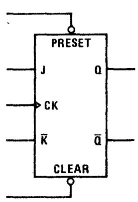

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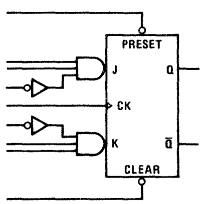

FLIP-FLOPS, DUAL D-TYPE

Dwg. Ref.	Typ. Characteristics		Data Times		Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
	f_{MAX} (MHz)	Pwr/F-F (mW)	Setup (ns)	Hold (ns)	Mil.		Coml.			
G	110	75	3↑	2↑			74S74	N	1-20	1-70
	43	75	15↑	5↑	54H74	J,N	74H74	J,N	1-20	1-64
	33	10	25↑	5↑	54LS74	J,N,W	74LS74	J,N	1-20	1-68
	25	43	20↑	5↑	5474	J,N,W	7474	J,N	1-20	1-62
	6	4	50↑	15↑	54L74	J,N,W	74L74	J,N	1-20	1-66

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

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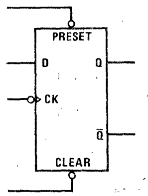

FLIP-FLOPS, SINGLE AND DUAL PULSE-TRIGGERED

Dwg. Ref.	Typ. Characteristics		Data Times		Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
	f_{MAX} (MHz)	Pwr/F-F (mW)	Setup (ns)	Hold (ns)	Mil.		Coml.			
H	30	80	0↑	0↓	54H73	J,N	74H73	J N	1-20	1-64
	20	50	0↑	0↓	5473	J,N,W	7473	J,N	1-20	1-62
	20	50	0↑	0↓	54107	J,N	74107	J,N	1-23	1-62
	6	3.8	0↑	0↓	54L73	J,N,W	74L73	J,N	1-20	1-66
I	30	80	0↑	0↓	54H76	J,N	74H76	J,N	1-21	1-64
	20	50	0↑	0↓	5476	J,N,W	7476	J,N	1-21	1-62
J	30	80	0↑	0↓	54H78	J,N	74H78	J,N	1-21	1-64
	6	3.8	0↑	0↓	54L78	J,N,W	74L78	J,N	1-21	1-66
K	30	80	0↑	0↓	54H71	J,N	74H71	J,N	1-18	1-64
L	30	80	0↑	0↓	54H72	J,N	74H72	J,N	1-19	1-64
	20	50	0↑	0↓	5472	J,N,W	7472	J,N	1-19	1-62
	6	3.8	0↑	0↓	54L72	J,N,W	74L72	J,N	1-19	1-66
M	6	3.8	0↑	0↓	54L71	J,N,W	74L71	J,N	1-19	1-66

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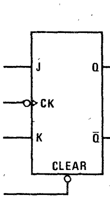

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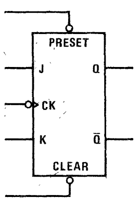

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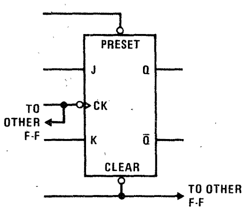

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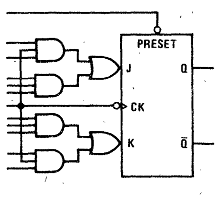

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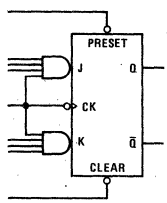

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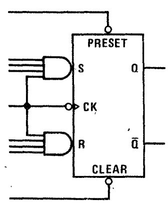


LATCHES, $\overline{S}$-$\overline{R}$

Description	Typ. Propagation Delay Time	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Quad $\overline{S}$-$\overline{R}$ Latches	12 ns	19 mW	54LS279	J,N,W	74LS279	J,N	2-168	2-169

LINE DRIVERS, 50-OHM/75-OHM

Description	Low-Level Output Current	High-Level Output Current	Typ. Delay Time	Typ. Power Per Gate	Device Type and Package			Connection Diagram Page No.	Electrical Tables Page No.
					Mil.	Coml.			
Dual 4-Input NAND Line Drivers	60 mA	–40 mA	4 ns	44 mW		74S140	N	1-29	1-54

NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Dual 4-Input NAND Gates	5 ns	17.5 mW			74S22	N	1-8	1-38
	8 ns	22 mW	54H22	J,N	74H22	J,N	1-8	1-38
	16 ns	2 mW	54LS22	J,N,W	74LS22	J,N	1-8	1-38
Triple 3-Input NAND Gates	16 ns	2 mW	54LS12	J,N,W	74LS12	J,N	1-5	1-38
Quad 2-Input NAND Gates	5 ns	17.5 mW			74S03	N	1-2	1-38
	8 ns	22 mW	54H01	J,N	74H01	J,N	1-1	1-38
	16 ns	2 mW	54LS01	J,N,W	74LS01	J,N	1-1	1-38
	16 ns	2 mW	54LS03	J,N,W	74LS03	J,N	1-2	1-38
	22 ns	10 mW	5401	J,N,W	7401	J,N	1-1	1-38
	22 ns	10 mW	5403	J,N	7403	J,N	1-2	1-38
	41 ns	1 mW	54L01	W	74L01	W	1-1	1-38
	41 ns	1 mW	54L03	J,N	74L03	J,N	1-2	1-38
	115 ns	1.8 mW			80L06	N	3-1	3-2
Hex Inverters	5 ns	17.5 mW			74S05	N	1-3	1-38
	8 ns	22 mW	54H05	J,N	74H05	J,N	1-3	1-38
	16 ns	2 mW	54LS05	J,N,W	74LS05	J,N	1-3	1-38
	22 ns	10 mW	5405	J,N,W	7405	J,N	1-3	1-38

NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Dual 4-Input NAND Gates	3 ns	19 mW			74S20	J,N	1-7	1-36
	6 ns	22 mW	54H20	J,N	74H20	J,N	1-7	1-36
	9.5 ns	2 mW	54LS20	J,N,W	74LS20	J,N	1-7	1-36
	10 ns	10 mW	5420	J,N,W	7420	J,N	1-7	1-36
	33 ns	1 mW	54L20	J,N,W	74L20	J,N	1-7	1-36
Dual 5-Input NAND Gates	10 ns	20 mW	7092	J,N,W	8092	J,N	3-3	3-4
Triple 3-Input NAND Gates	3 ns	19 mW			74S10	J,N	1-4	1-36
	6 ns	22 mW	54H10	J,N	74H10	J,N	1-4	1-36
	9.5 ns	2 mW	54LS10	J,N,W	74LS10	J,N	1-4	1-36
	10 ns	10 mW	5410	J,N,W	7410	J,N	1-4	1-36
	33 ns	1 mW	54L10	J,N,W	74L10	J,N	1-4	1-36
Quad 2-Input NAND Gates	3 ns	19 mW			74S00	N	1-1	1-36
	6 ns	22 mW	54H00	J,N	74H00	J,N	1-1	1-36
	9.5 ns	2 mW	54LS00	J,N,W	74LS00	J,N	1-1	1-36
	10 ns	10 mW	5400	J,N,W	7400	J,N	1-1	1-36
	33 ns	1 mW	54L00	J,N,W	74L00	J,N	1-1	1-36
Hex Inverters	3 ns	19 mW			74S04	N	1-2	1-36
	6 ns	22 mW	54H04	J,N	74H04	J,N	1-2	1-36
	9.5 ns	2 mW	54LS04	J,N,W	74LS04	J,N	1-2	1-36
	10 ns	10 mW	5404	J,N,W	7404	J,N	1-2	1-36
	11 ns	18 mW	7090	J,N,W	8090	J,N	3-3	3-4
	33 ns	1 mW	54L04	J,N,W	74L04	J,N	1-2	1-36
8-Input NAND Gates	3 ns	19 mW			74S30	J,N	1-9	1-36
	6 ns	22 mW	54H30	J,N	74H30	J,N	1-9	1-36
	10 ns	10 mW	5430	J,N,W	7430	J,N	1-9	1-36
	17 ns	2.4 mW	54LS30	J,N,W	74LS30	J,N	1-9	1-36
	33 ns	1 mW	54L30	J,N,W	74L30	J,N	1-9	1-36
13-Input NAND Gates	3 ns	19 mW			74S133	N	1-28	1-36

NOR GATES WITH TOTEM-POLE OUTPUTS

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Dual 4-Input NOR Gates With Strobe	10.5 ns	23 mW	5425	J,N,W	7425	J,N	1-8	1-40
Dual 5-Input NOR Gates	4 ns	54 mW			74S260	N	1-31	1-40
Triple 3-Input NOR Gates	8.5 ns	22 mW	5427	J,N,W	7427	J,N	1-9	1-40
	10 ns	4.5 mW	54LS27	J,N,W	74LS27	J,N	1-9	1-40
Quad 2-Input NOR Gates	3.5 ns	29 mW			74S02	N	1-2	1-40
	10 ns	2.75 mW	54LS02	J,N,W	74LS02	J,N	1-2	1-40
	10 ns	14 mW	5402	J,N,W	7402	J,N	1-2	1-40
	33 ns	1.5 mW	54L02	J,N,W	74L02	J,N	1-2	1-40

ONE SHOTS, RETRIGGERABLE

Description	No. of Inputs		Direct Clear	Output Pulse Range	Typ. Total Power	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
	Positive	Negative				Mil.		Coml.			
Single	2	2	Yes	45 ns—∞	30 mW	54LS122	J,N,W	74LS122	J,N	1-26	1-78
	2	2	Yes	50 ns—∞	90 mW	9601	J,N,W	8601	J,N	4-43	4-44
Dual	1	1	Yes	45 ns—∞	230 mW	54123	J,N,W	74123	J,N	1-26	1-78
	1	1	Yes	90 ns—∞	25 mW	54L123A	J,N,W	74L123A	J,N	1-26	1-78
	1	1	Yes	45 ns—∞	60 mW	54LS123	J,N,W	74LS123	J,N	1-26	1-78
	1	1	Yes	72 ns—∞	195 mW	9602	J,N,W	8602	J,N	4-46	4-47
	2	2	Yes	72 ns—∞	275 mW	7853	J,N,W	8853	J,N	3-151	3-152

ONE SHOTS WITH SCHMITT-TRIGGER INPUTS

Description	No. of Inputs		Output Pulse Range	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
	Positive	Negative			Mil.		Coml.			
Single	1	2	40 ns—28 s	90 mW	54121	J,N,W	74121	J,N	1-26	1-76
Dual	1	1	20 ns—70 s	23 mW			74LS221	J,N	1-30	1-76
	1	1	20 ns—49 s	23 mW	54LS221	J,N,W			1-30	1-76

OR GATES WITH TOTEM-POLE OUTPUTS

Description	Typ. Propagation Delay Time	Typ. Power Dissipation Per Gate	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Quad 2-Input OR Gates	12 ns	24 mW	5432	J,N,W	7432	J,N	1-10	1-52
	12 ns	5 mW	54LS32	J,N,W	74LS32	J,N	1-10	1-52

SCHMITT-TRIGGERS WITH TOTEM-POLE OUTPUTS

Description	Typ. Hysteresis	Typ. Delay Time	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Dual 4-Input NAND	0.8V	16.5 ns	5413	J,N,W	7413	J,N	1-5	1-48
Schmitt Triggers	0.8V	16.5 ns	54LS13	J,N,W	74LS13	J,N	1-5	1-48
Quad 2-Input NAND	0.8V	15 ns	54132	J,N,W	74132	J,N	1-27	1-48
Schmitt Triggers	0.8V	15 ns	54LS132	J,N,W	74LS132	J,N	1-27	1-48
Hex Schmitt Trigger Inverters	0.8V	15 ns	5414	J,N,W	7414	J,N	1-6	1-48
	0.8V	15 ns	54LS14	J,N,W	74LS14	J,N	1-6	1-48

ADDERS

Description	Typ. Carry Time	Typ. Add Time	Typ. Power Dissipation Per Bit	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
				Mil.		Coml.			
Single 4-Bit Full Adders	10 ns	15 ns	24 mW	54LS83A	J,N,W	74LS83A	J,N	2-17	2-18
	10 ns	15 ns	24 mW	54LS283	J,N,W	74LS283	J,N	2-17	2-18
	10 ns	16 ns	76 mW	5483	J,W	7483	J,N	2-17	2-18

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

Description	Typ. Carry Time	Typ. Add Time	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
				Mil.		Coml.			
4-Bit Arithmetic Logic Units/ Function Generators	12.5 ns	24 ns	455 mW	54181	J	74181	J,N	2-107	2-109
4-Bit Parallel Binary Accumulators	10 ns	20 ns	720 mW			74S281	N	2-173	2-174
Look-Ahead Carry Generators	7 ns		260 mW			74S182	N	2-113	2-114
	13 ns		180 mW	54182	J	74182	J,N	2-113	2-114

ARITHMETIC OPERATORS

Description	Typ. Delay Time	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Quad 2-Input EXCLUSIVE-NOR Gates	18 ns	40 mW	54LS266	J,N,W	74LS266	J,N	1-31	1-84
Quad 2-Input EXCLUSIVE-OR Gates With Open Collector Outputs	18 ns	30 mW	54LS136	J,N,W	74LS136	J,N	1-29	1-84
Quad 2-Input EXCLUSIVE-OR Gates with Totem-Pole Outputs	7 ns	250 mW			74S86	N	1-22	1-72
	10 ns	30 mW	54LS86	J,N,W	74LS86	J,N	1-22	1-72
	10 ns	30 mW	54LS386	J,N,W	74LS386	J,N	1-34	1-72
	14 ns	150 mW	5486	J,N,W	7486	J,N	1-22	1-72
	29 ns	15 mW	54L86	J,N,W	74L86	J,N	1-22	1-72
Quad EXCLUSIVE-OR/NOR Gates	8 ns	325 mW			74S135	N	1-28	1-82

CODE CONVERTERS

Description	Typ. Delay Time Per Package Level	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
6-Bit Binary to 6-Bit BCD Converters	25 ns	280 mW	54185A	J,W	74185A	J,N	2-116	2-117
	31 ns	350 mW			8899	N	3-156	3-157
6-Line BCD to 6-Line Binary, or 4-Line to 4-Line BCD 9's/BCD 10's Converters	25 ns	280 mW	54184	J,W	74184	J,N	2-116	2-117
	31 ns	350 mW			8898	N	3-156	3-157

COMPARATORS

Description	Typ. Compare Time	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
4-Bit Magnitude Comparators	20 ns	175 mW	7200	J,N,W	8200	J,N	3-23	3-24
	21 ns	275 mW	5485	J,W	7485	J,N	2-21	2-22
	70 ns	20 mW	54L85	J,N,W	74L85	J,N	2-21	2-22
	70 ns	75 mW	76L24	J,N,W	86L24	J,N	3-131	3-132
6-Bit Magnitude Comparators	20 ns	250 mW	7131	J,W	8131	J,N	3-19	3-20
	20 ns	250 mW	7136	J,W	8136	J,N	3-19	3-20
	21 ns	205 mW	7160	J,W	8160	J,N	3-17	3-18
10-Bit Magnitude Comparators	21 ns	240 mW	7130	J,F	8130	J,N	3-17	3-18

COUNTERS, ASYNCHRONOUS (RIPPLE CLOCK) – NEGATIVE-EDGE TRIGGERED

Description	Count Freq.	Parallel Load	Clear	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
					Mil.		Coml.			
4-Bit Binary	50 MHz	Yes	Low	240 mW	54197	J,N	74197	J,N	2-101	2-102
	40 MHz	Yes	Low	150 mW	7291	J,N,W	8291	J,N	4-11	4-12
	35 MHz	Yes	Low	150 mW	54177	J	74177	J,N	2-101	2-102
	35 MHz	Yes	Low	150 mW	7281	J,W	8281	J,N	4-11	4-12
	32 MHz	None	High	39 mW	54LS93	J,N,W	74LS93	J,N	2-30	2-31
	32 MHz	None	High	160 mW	5493A	J,W	7493A	J,N	2-30	2-31
	30 MHz	Yes	Low	60 mW	54LS197	J,N,W	74LS197	J,N	2-101	2-102
	6 MHz	None	High	20 mW	54L93	J,N,W	74L93	J,N	2-30	2-31
	6 MHz	None	High	20 mW	76L93	J,N,W	86L93	J,N	3-142	3-143
Decade	50 MHz	Yes	Low	240 mW	54196	J,N	74196	J,N	2-101	2-102
	40 MHz	Yes	Low	150 mW	7290	J,N,W	8290	J,N	4-11	4-12
	35 MHz	Yes	Low	150 mW	54176	J	74176	J,N	2-101	2-102
	35 MHz	Yes	Low	150 mW	7280	J,W	8280	J,N	4-11	4-12
	32 MHz	Set-to-9	High	40 mW	54LS90	J,N,W	74LS90	J,N	2-30	2-31
	32 MHz	Set-to-9	High	160 mW	5490A	J,W	7490A	J,N	2-30	2-31
	30 MHz	Yes	Low	60 mW	54LS196	J,N,W	74LS196	J,N	2-101	2-102
	6 MHz	Set-to-9	High	20 mW	54L90	J,N,W	74L90	J,N	2-30	2-31
Divide by 12	35 MHz	Yes	Low	150 mW	7288	J,W	8288	J,N	4-11	4-12
	32 MHz	None	High	39 mW	54LS92	J,N,W	74LS92	J,N	2-30	2-31
	32 MHz	None	High	160 mW	5492A	J,W	7492A	J,N	2-30	2-31

COUNTERS, SYNCHRONOUS—POSITIVE-EDGE TRIGGERED

Description	Count Freq.	Parallel Load	Clear	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
					Mil.		Coml.			
4-Bit Binary	25 MHz	Sync	Sync-L	93 mW	54LS163	J,N,W	74LS163	J,N	2-70	2-71
	25 MHz	Sync	Async-L	93 mW	54LS161	J,N,W	74LS161	J,N	2-70	2-71
	25 MHz	Sync	Sync-L	305 mW	54163A	J,W	74163A	J,N	2-70	2-71
	25 MHz	Sync	Async-L	305 mW	54161A	J,W	74161A	J,N	2-70	2-71
	25 MHz	Sync	Async-L	305 mW	9316	J,W	8316	J,N	4-27	4-28
	25 MHz	Sync	Sync-L	375 mW	7556	J,W	8556	J,N	3-72	3-73
	6 MHz	Sync	Async-L	33 mW	76L76	J,N,W	86L76	J,N	3-137	3-138
4-Bit Binary Up/Down	25 MHz	Sync	None	100 mW	54LS169	J,N,W	74LS169	J,N	2-85	2-86
	25 MHz	Async	Async-H	85 mW	54LS193	J,N,W	74LS193	J,N	2-133	2-134
	20 MHz	Async	Async-H	325 mW	54193	J,W	74193	J,N	2-133	2-134
	20 MHz	Async	Async-H	325 mW	7563	J,W	8563	J,N	3-76	3-77
	20 MHz	Async	None	90 mW	54LS191	J,N,W	74LS191	J,N	2-128	2-129
	20 MHz	Async	None	325 mW	54191	J,N,W	74191	J,N	2-128	2-129
	6 MHz	Async	Async-H	40 mW	54L193	J,N,W	74L193	J,N	2-133	2-134
	6 MHz	Async	Async-H	40 mW	75L63	J,N,W	85L63	J,N	3-76	3-77
Decade	25 MHz	Sync	Sync-L	93 mW	54LS162	J,N,W	74LS162	J,N	2-70	2-71
	25 MHz	Sync	Async-L	93 mW	54LS160	J,N,W	74LS160	J,N	2-70	2-71
	25 MHz	Sync	Sync-L	305 mW	54162A	J,W	74162A	J,N	2-70	2-71
	25 MHz	Sync	Async-L	305 mW	54160A	J,W	74160A	J,N	2-70	2-71
	25 MHz	Sync	Async-L	305 mW	9310	J,W	8310	J,N	4-27	4-28
	25 MHz	Sync	Sync-L	400 mW	7555	J,W	8555	J,W	3-72	3-73
	6 MHz	Sync	Async-L	33 mW	76L75	J,N,W	86L75	J,N	3-137	3-138
Decade Up/Down	25 MHz	Sync	None	100 mW	54LS168	J,N,W	74LS168	J,N	2-85	2-86
	25 MHz	Async	Async-H	85 mW	54LS192	J,N,W	74LS192	J,N	2-133	2-134
	20 MHz	Async	Async-H	325 mW	54192	J,W	74192	J,N	2-133	2-134
	20 MHz	Async	None	100 mW	54LS190	J,N,W	74LS190	J,N	2-128	2-129
	20 MHz	Async	None	325 mW	54190	J,N,W	74190	J,N	2-128	2-129
	20 MHz	Async	Async-H	325 mW	7560	J,W	8560	J,N	3-76	3-77
	6 MHz	Async	Async-H	40 mW	54L192	J,N,W	74L192	J,N	2-133	2-134
	6 MHz	Async	Async-H	40 mW	75L60	J,N,W	85L60	J,N	3-76	3-77
Modulo-N Divider	15 MHz	Sync	None	250 mW	7520	J,W	8520	J,N	3-44	3-47

DATA SELECTORS/MULTIPLEXERS

Description	Type of Output	Typ. Delay Times: Data to Inv. Output	Typ. Delay Times: Data to Non-Inv. Output	Typ. Delay Times: From Enable	Typ. Total Power Dissipation	Device Type and Package: Mil.		Device Type and Package: Coml.		Connection Diagram Page No.	Electrical Tables Page No.
Quad 2-Line to 1-Line	TRI-STATE	4 ns		14 ns	280 mW			74S258	N	2-165	2-166
	TRI-STATE		5 ns	14 ns	320 mW			74S257	N	2-165	2-166
	Standard	4 ns		7 ns	195 mW			74S158	N	2-66	2-67
	Standard		5 ns	8 ns	250 mW			74S157	N	2-66	2-67
	TRI-STATE	12 ns		20 ns	35 mW	54LS258	J,N,W	74LS258	J,N	2-165	2-166
	TRI-STATE		12 ns	20 ns	50 mW	54LS257	J,N,W	74LS257	J,N	2-165	2-166
	Standard	7 ns		12 ns	24 mW	54LS158	J,N,W	74LS158	J,N	2-66	2-67
	Standard		9 ns	14 ns	49 mW	54LS157	J,N,W	74LS157	J,N	2-66	2-67
	Standard		9 ns	14 ns	150 mW	54157	J,W	74157	J,N	2-66	2-67
	Standard		40 ns	60 ns	15 mW	54L157A	J,N,W	74L157A	J,N	2-66	2-67
	Standard		9 ns	14 ns	150 mW	9322	J,W	8322	J,N	4-38	4-39
	Standard		40 ns	60 ns	15 mW	71L22	J,N,W	81L22	J,N	3-13	3-14
	TRI-STATE		9.5 ns	N/A	200 mW	7123	J,W	8123	J,N	3-13	3-14
	TRI-STATE		40 ns	N/A	20 mW	71L23	J,N,W	81L23	J,N	3-13	3-14
Quad 2-Line to 1-Line With Storage	Standard		20 ns from clock		65 mW	54LS298	J,N,W	74LS298	J,N	2-184	2-185
Dual 4-Line to 1-Line	TRI-STATE		12 ns	16 ns	35 mW	54LS253	J,N,W	74LS253	J,N	2-163	2-164
	Standard		6 ns	9.5 ns	225 mW			74S153	N	2-57	2-58
	Standard		14 ns	17 ns	180 mW	54153	J,W	74153	J,N	2-57	2-58
	Standard		14 ns	17 ns	31 mW	54LS153	J,N,W	74LS153	J,N	2-57	2-58
	Standard	12 ns	20 ns	20 ns	135 mW	9309	J,W	8309	J,N	4-24	4-25
	TRI-STATE		13.5 ns	20 ns	170 mW	7214	J,W	8214	J,N	3-28	3-29
8-Line to 1-Line	TRI-STATE	4.5 ns	8 ns	14 ns	275 mW			74S251	N	2-160	2-161
	TRI-STATE	11 ns	18 ns	17 ns	155 mW	54251	J,W	74251	J,N	2-160	2-161
	TRI-STATE	17 ns	21 ns	21 ns	35 mW	54LS251	J,N,W	74LS251	J,N	2-160	2-161
	Standard	4.5 ns	8 ns	9 ns	225 mW			74S151	N	2-53	2-54
	Standard	8 ns	16 ns	22 ns	145 mW	54151A	J,W	74151A	J,N	2-53	2-54
	Standard	11 ns	18 ns	27 ns	30 mW	54LS151	J,N,W	74LS151	J,N	2-53	2-54
	Standard	9 ns	16 ns	17 ns	135 mW	9312	J,W	8312	J,N	4-24	4-25
	Standard	11 ns	18 ns	17 ns	155 mW	7121	J,W	8121	J,N	3-11	3-12
	Standard	22 ns		N/A	100 mW	7210	J,W	8210	J,N	3-25	3-26
	Standard	22 ns		20 ns	100 mW	7211	J,W	8211	J,N	3-25	3-26
16-Line to 1-Line	Standard	11 ns		18 ns	200 mW	54150	J,F	74150	J,N	2-53	2-54
	TRI-STATE	11 ns		21 ns	225 mW	7219	J,F	8219	J,N	3-28	3-29

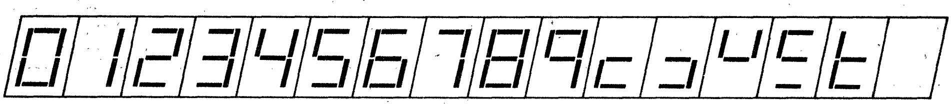
DECODERS/DEMULTIPLEXERS

Description	Type of Output	Typ. Select Time	Typ. Enable Time	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
					Mil.		Coml.			
Dual 2-Line to 4-Line	Totem-Pole	7.5 ns	6 ns	300 mW			74S139	N	2-46	2-47
	Totem-Pole	18 ns	15 ns	30 mW	54LS155	J,N,W	74LS155	J,N	2-63	2-64
	TRI-STATE	20 ns	15 ns	240 mW	7230	J,W	8230	J,N	3-37	3-38
	Totem-Pole	21 ns	16 ns	250 mW	54155	J,W	74155	J,N	2-63	2-64
	Totem-Pole	22 ns	19 ns	34 mW	54LS139	J,N,W	74LS139	J,N	2-46	2-47
	Open-Collector	23 ns	18 ns	250 mW	54156	J,W	74156	J,N	2-63	2-64
	Open-Collector	33 ns	26 ns	31 mW	54LS156	J,N,W	74LS156	J,N	2-63	2-64
3-Line to 8-Line	Totem-Pole	8 ns	7 ns	225 mW			74S138	N	2-46	2-47
	Totem-Pole	22 ns	21 ns	31 mW	54LS138	J,N,W	74LS138	J,N	2-46	2-47
	Totem-Pole	25 ns		140 mW	7223	J	8223	J,N	3-35	3-36
4-Line to 10-Line, BCD to Decimal	Totem-Pole	17 ns		35 mW	54LS42	J,N,W	74LS42	J,N	2-3	2-4
	Totem-Pole	17 ns		140 mW	5442	J,W	7442	J,N	2-3	2-4
	Totem-Pole	20 ns		125 mW	9301	J,W	8301	J,N	4-22	4-23
	Totem-Pole	67 ns		15 mW	54L42A	J,N,W	74L42A	J,N	2-3	2-4
4-Line to 16-Line	Totem-Pole	19.5 ns	17.5 ns	170 mW	54154	J,F	74154	J,N	2-60	2-61
	Totem-Pole	19.5 ns	17.5 ns	170 mW	9311	J,F	8311	J,N	4-33	4-34
	Totem-Pole	23 ns	19 ns	45 mW	54LS154	J,N,W	74LS154	J,N	2-60	2-61
	Totem-Pole	55 ns	45 ns	24 mW	54L154A	F,J,N	74L154A	J,N	2-60	2-61

DISPLAY DECODERS/DRIVERS, OPEN-COLLECTOR

Description	Output Sink Current	Off-State Output Voltage	Typ. Total Power Dissipation	Blanking	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
					Mil.		Coml.			
BCD to 7-Segment Decoders/Drivers	40 mA	30V	320 mW	Ripple	5446A	J,N,W	7446A	J,N	2-8	2-9
	40 mA	15V	320 mW	Ripple	5447A	J,N,W	7447A	J,N	2-8	2-9
	24 mA	15V	35 mW	Ripple			74LS47	J,N	2-8	2-9
	12 mA	15V	35 mW	Ripple	54LS47	J,N,W			2-8	2-9
	6.4 mA	5.5V	265 mW	Ripple	5448	J,N,W	7448	J,N	2-8	2-9
	6 mA	5.5V	125 mW	Ripple			74LS48	J,N	2-8	2-9
	4 mA	5.5V	40 mW	Direct	54LS49	J,N,W	74LS49	J,N	2-8	2-9
	2 mA	5.5V	125 mW	Ripple	54LS48	J,N,W			2-8	2-9
BCD to Decimal Decoders/Drivers	80 mA	30V	215 mW	Invalid Codes	5445	J,W	7445	J,N	2-6	2-7
	80 mA	15V	215 mW	Invalid Codes	54145	J,W	74145	J,N	2-6	2-7
	7 mA	60V	80 mW	Invalid Codes	54141	J,W	74141	J,N	2-1	2-2
7-Segment to BCD Decoders/Drivers	3.6 mA	2.4V	75 mW	Direct	76L25	J,N,W	86L25	J,N	3-134	3-135

RESULTANT DISPLAYS USING 46A, 47A, 48, LS47, LS48, LS49



0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

LATCHES

Description	No. of Bits	Clear	Outputs	Typ. Delay Time	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
						Mil.		Coml.			
Addressable Latches	8	Low	Q	21 ns	280 mW	9334	J,W	8334	J,N	4-40	4-41
DG (Clocked) Latches	4	None	Q, Q	11 ns	32 mW	54LS75	J,N,W	74LS75	J,N	2-14	2-15
	4	None	Q	10 ns	35 mW	54LS77	W			2-14	2-15
	4	None	Q, $\overline{Q}$	15 ns	160 mW	5475	J,N,W	7475	J,N	2-14	2-15
	4	None	Q, $\overline{Q}$	52 ns	17.5 mW	54L75A	J,N,W	74L75A	J,N	2-14	2-15
$\overline{S}$-$\overline{R}$ Latches	4	None	Q	12 ns	19 mW	54LS279	J,N,W	74LS279	J,N	2-168	2-169
	4	None	Q	19 ns	180 mW	7544	J,N,W	8544	J,N	3-54	3-55
TRI-STATE Counters/Latches	4	High	Q	28 ns	330 mW	7552	J,W	8552	J,N	3-64	3-65
	4	High	Q	95 ns	38 mW	75L52	J,N,W	85L52	J,N	3-64	3-65
	4	High	Q	28 ns	330 mW	7554	J,W	8554	J,N	3-64	3-65
	4	High	Q	95 ns	38 mW	75L54	J,N,W	85L54	J,N	3-64	3-65
	8	High	Q	21 ns	330 mW	7553	J,W	8553	J,N	3-70	3-71

MULTIPLIERS

Description	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
	Mil.		Coml.			
4-Bit by 4-Bit Parallel Binary Multipliers	7875A	J	8875A	J,N	3-154	3-155
	7875B	J	8875B	J,N	3-154	3-155

PARITY GENERATORS/CHECKERS

Description	Typ. Delay Time	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
8-Bit Odd/Even Parity Generators/Checkers	35 ns	170 mW	54180	J,W	74180	J,N	2-105	2-106
9-Bit Odd/Even Parity Generators/Checkers	13 ns	335 mW			74S280	N	2-170	2-171
	34 ns	130 mW	7220	J,N,W	8220	J,N	3-32	3-33

PRIORITY ENCODERS

Description	Typ. Propagation Delay Time	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
			Mil.		Coml.			
Cascadable Octal Priority Encoders	12 ns	190 mW	54148	J,W	74148	J,N	2-49	2-50
	12 ns	190 mW	9318	J,W	8318	J,N	4-36	4-37
Full BCD Priority Encoders	10 ns	225 mW	54147	J,W	74147	J,N	2-49	2-50

REGISTER FILES

Description	Typ. Address Time	Typ. Read Enable Time	Data Input Rate	Typ. Total Power Dissipation	Device Type and Package				Connection Diagram Page No.	Electrical Tables Page No.
					Mil.		Coml.			
4 Words of 4-Bits	27 ns	15 ns	20 MHz	125 mW	54LS170	J,N,W	74LS170	J,N	2-91	2-92
	30 ns	15 ns	20 MHz	635 mW			74170	J,N	2-91	2-92
4 Words of 4-Bits (TRI-STATE Outputs)	24 ns	19 ns	20 MHz	135 mW	54LS670	J,N,W	74LS670	J,N	2-191	2-192
	24 ns	19 ns	30 MHz	400 mW	7542	J,W	8542	J,N	3-52	3-53

REGISTERS, OTHER

Description	Freq.	Async. Clear	Typ. Total Power Dissipation	Device Type and Package: Mil.		Coml.		Connection Diagram Page No.	Electrical Tables Page No.
Quad Bus-Buffer Registers	25 MHz	High	250 mW	54173	J,W	74173	J,N	2-96	2-97
	25 MHz	High	250 mW	7551	J,W	8551	J,N	3-62	3-63
	6 MHz	High	28 mW	75L51	J,N,W	85L51	J,N	3-62	3-63
Quad D-Type Registers	75 MHz	Low	300 mW			74S175	N	2-98	2-99
	30 MHz	Low	55 mW	54LS175	J,N,W	74LS175	J,N	2-98	2-99
	25 MHz	Low	150 mW	54175	J,W	74175	J,N	2-98	2-99
Quad Multiplexers With Storage	25 MHz	None	65 mW	54LS298	J,N,W	74LS298	J,N	2-184	2-185
Hex D-Type Registers	75 MHz	Low	450 mW			74S174	N	2-98	2-99
	30 MHz	Low	80 mW	54LS174	J,N,W	74LS174	J,N	2-98	2-99
	25 MHz	Low	225 mW	54174	J,W	74174	J,N	2-98	2-99
8-Bit Universal Shift/Storage Registers	15 MHz	None	400 mW	7546	J,W	8546	J,N	3-56	3-57
Octal D-Type Registers	25 MHz	None	175 mW	54LS374	J,N,W	74LS374	J,N	2-187	2-188

REGISTERS, SHIFT

Description	No. of Bits	Shift Freq.	Serial Data Input	Async. Clear	Modes: S-R*	S-L*	Load	Hold	Typ. Total Power Dissipation	Device Type and Package: Mil.		Coml.		Connection Diagram Page No.	Electrical Tables Page No.
Parallel-In, Parallel-Out (Bidirectional)	8	25 MHz	D	Low	X	X	X	X	360 mW	54198	J	74198	J,N	2-148	2-149
	4	70 MHz	D	Low	X	X	X	X	450 mW			74S194	N	2-140	2-141
	4	25 MHz	D	Low	X	X	X	X	75 mW	54LS194A	J,N,W	74LS194A	J,N	2-140	2-141
	4	25 MHz	D	Low	X	X	X	X	195 mW	54194	J,W	74194	J,N	2-140	2-141
Parallel-In, Parallel-Out	8	25 MHz	J-$\overline{K}$	Low	X		X	X	360 mW	54199	J	74199	J,N	2-148	2-149
	5	10 MHz	D	Low	X		X		60 mW	54LS96	J,N,W	74LS96	J,N	2-39	2-40
	5	10 MHz	D	Low	X		X		240 mW	5496	J,W	7496	J,N	2-39	2-40
	4	70 MHz	J-$\overline{K}$	Low	X		X		375 mW			74S195	N	2-144	2-145
	4	30 MHz	J-$\overline{K}$	Low	X		X		195 mW	54195	J,W	74195	J,N	2-144	2-145
	4	30 MHz	J-$\overline{K}$	Low	X		X		300 mW	9300	J,N,W	8300	J,N	4-19	4-20
	4	30 MHz	J-$\overline{K}$	Low	X		X		70 mW	54LS195A	J,N,W	74LS195A	J,N	2-144	2-145
	4	25 MHz	D	Low	X		X		75 mW	54LS395	J,N,W	74LS395	J,N	2-189	2-190
	4	25 MHz	D	None	X		X		195 mW	5495	J,W	7495	J,N	2-36	2-37
	4	25 MHz	D	None	X		X		65 mW	54LS95B	J,N,W	74LS95B	J,N	2-36	2-37
	4	6 MHz	D	None	X		X		24 mW	54L95	J,N,W	74L95	J,N	2-36	2-37
Serial-In, Parallel-Out	8	25 MHz	Gated D	Low	X				80 mW	54LS164	J,N,W	74LS164	J,N	2-76	2-77
	8	25 MHz	Gated D	Low	X				175 mW	54164	J,W	74164	J,N	2-76	2-77
	8	25 MHz	Gated D	Low	X				175 mW	7570	J,W	8570	J,N	3-86	3-87
	8	6 MHz	Gated D	Low	X				30 mW	54L164A	J,N,W	74L164A	J,N	2-76	2-77
	8	6 MHz	Gated D	Low	X				30 mW	76L70	J,N,W	86L70	J,N	3-86	3-87
Parallel-In, Serial-Out	8	25 MHz	D	None	X		X	X	200 mW	54165	J,W	74165	J,N	2-79	2-80
	8	20 MHz	D	Low	X		X	X	360 mW	54166	J	74166	J,N	2-82	2-83
	8	14 MHz	D	None	X		X	X	200 mW	7590	J,W	8590	J,N	3-110	3-111
	8	6 MHz	D	None	X		X	X	30 mW	76L90	J,N,W	86L90	J,N	3-110	3-111
Serial-In, Serial-Out	8	10 MHz	Gated D	None	X				175 mW	5491A	J,W	7491A	J,N	2-34	2-35
	8	4 MHz	Gated D	None	X				17.5 mW	54L91	J,N,W	74L91	J,N	2-34	2-35

* S-R ≡ shift right, S-L ≡ shift left.

DUAL-IN-LINE PACKAGES

(N) All devices ordered with the "N" suffix are supplied in either the 14-pin, 16-pin, 20-pin, or 24-pin molded dual-in-line package. Molding material is EPOXY B, a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is Alloy 42 with a hot solder dipped surface to allow for ease of solderability.

(J) All devices ordered with the "J" suffix are supplied in either the 14-pin, 16-pin, or 24-pin ceramic dual-in-line package. The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

FLAT PACKAGES

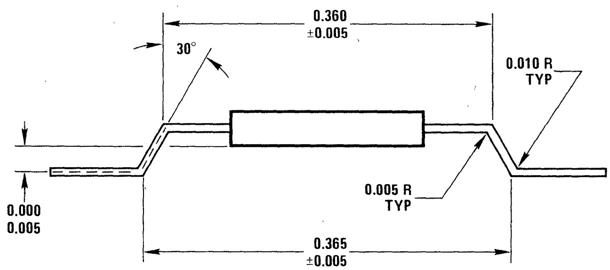
(W) All devices ordered with the "W" suffix are supplied in either the 14-pin or 16-pin ceramic flat package. The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

(F) All devices ordered with the "F" suffix are supplied in the 24-pin glass/metal flat package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.

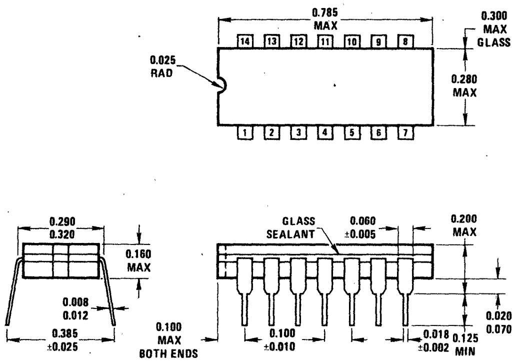
Four combinations of bottom insulator and formed leads are supplied for the W or F packages. Suffix coding is as follows:

Suffix	Bottom Insulator	Formed Leads
–00 (Ex: DM54L00W-00)	No	No
–01	Yes	Yes
–06	Yes	No
–07	No	Yes

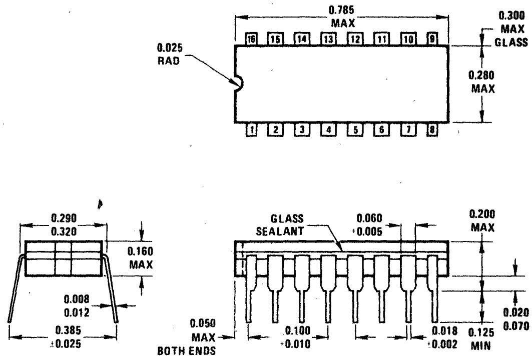
If no suffix is added, parts will be supplied as if the –00 suffix had been ordered.



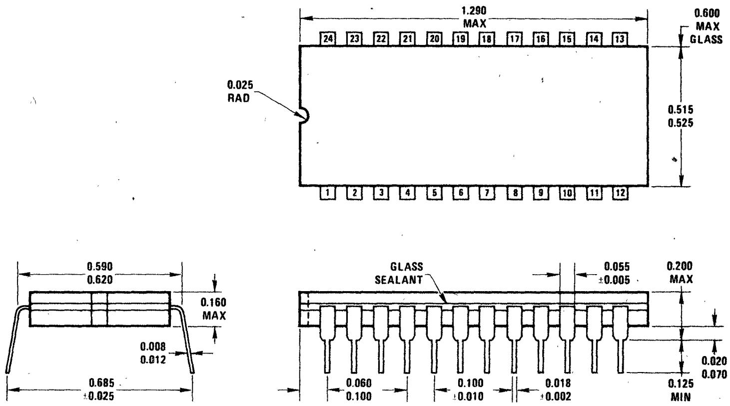
Standard Flat Pack Lead Form



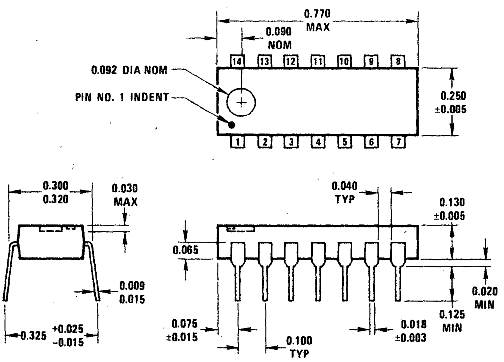
14-Pin Ceramic Dual-In-Line Package (J)



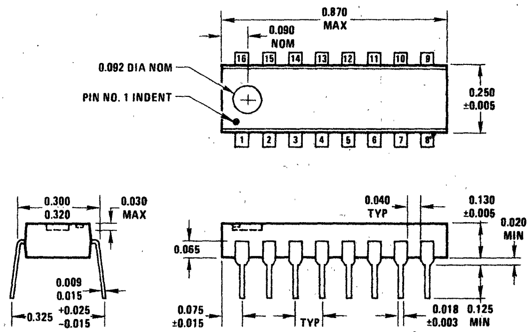
16-Pin Ceramic Dual-In-Line Package (J)



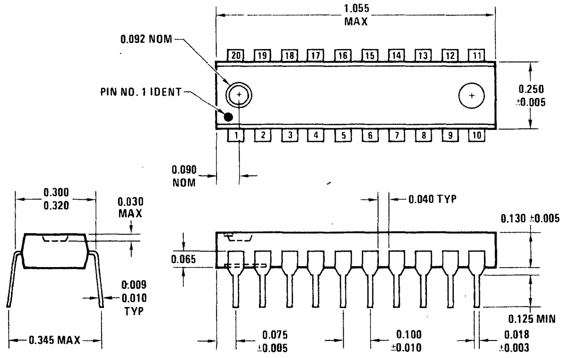
24-Pin Ceramic Dual-In-Line Package (J)



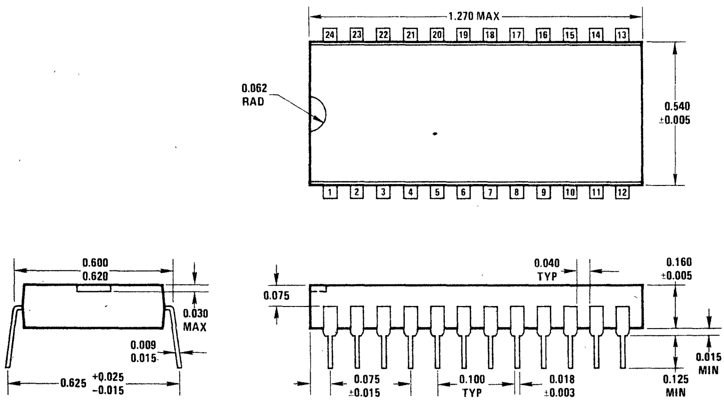
14-Pin Molded Dual-In-Line Package (N)



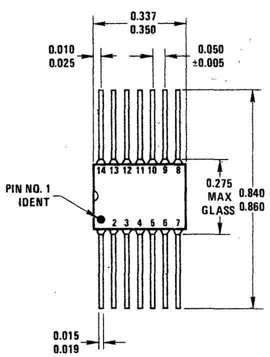
16-Pin Molded Dual-In-Line Package (N)



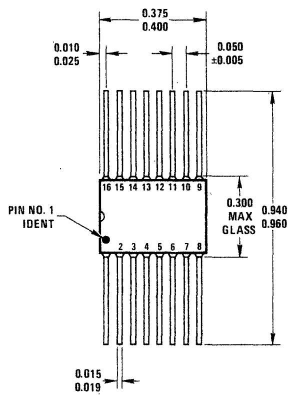
20-Pin Molded Dual-In-Line Package (N)



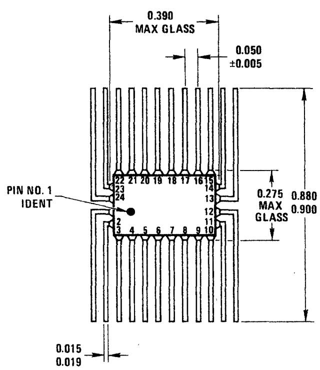
24-Pin Molded Dual-In-Line Package (N)



14-Pin Flat Package (W)



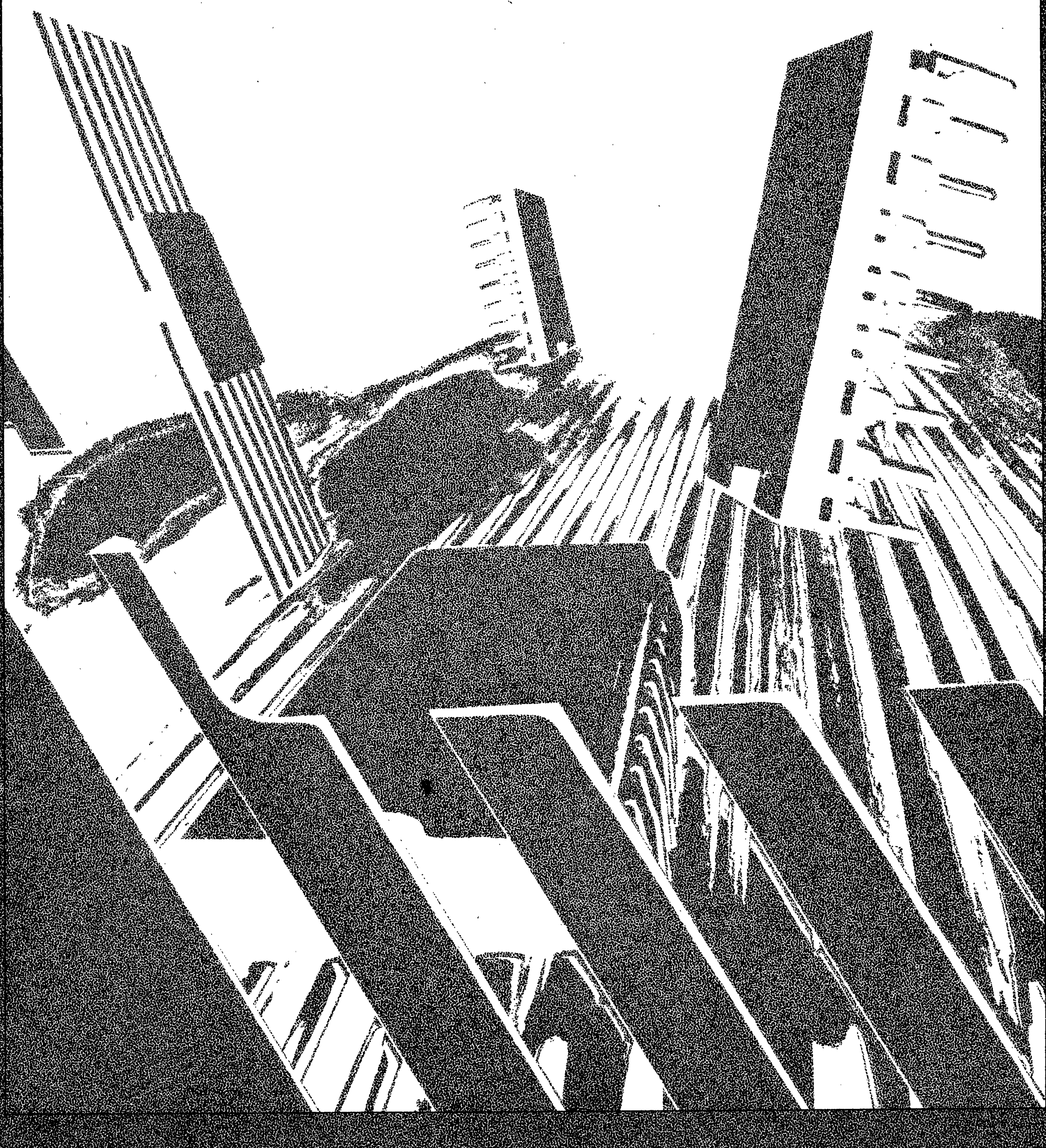
16-Pin Flat Package (W)



24-Pin Flat Package (F)

INCHES TO MILLIMETERS CONVERSION TABLE					
INCHES	MM	INCHES	MM	INCHES	MM
0.001	0.0254	0.010	0.254	0.100	2.54
0.002	0.0508	0.020	0.508	0.200	5.08
0.003	0.0762	0.030	0.762	0.300	7.62
0.004	0.1016	0.040	1.016	0.400	10.16
0.005	0.1270	0.050	1.270	0.500	12.70
0.006	0.1524	0.060	1.524	0.600	15.24
0.007	0.1778	0.070	1.778	0.700	17.78
0.008	0.2032	0.080	2.032	0.800	20.32
0.009	0.2286	0.090	2.286	0.900	22.86

National Semiconductor
54/74 SSI DEVICES
Section 1



54/74 SSI — Table of Contents

54/74 SSI Table of Contents

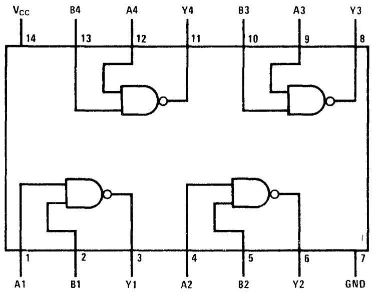
Table of Contents

54/74 SSI Table of Contents

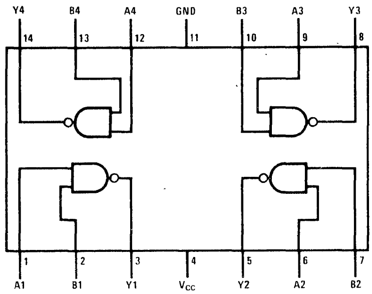
National Semiconductor
54/74 SSI DEVICES
Connection Diagrams
Section 1

00 Quad 2-Input NAND Gates

$Y = \overline{AB}$



5400/7400(J), (N); 54H00/74H00(J), (N);
54L00/74L00(J), (N); 54LS00/74LS00(J),(N),(W);
74S00(N)

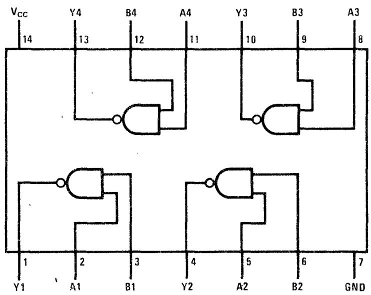


5400/7400(W); 54L00/74L00(W)

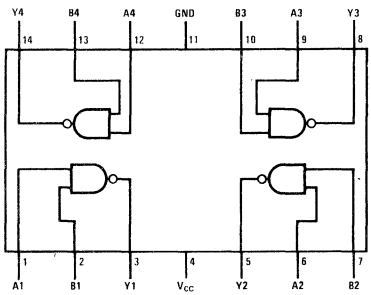
See page 1-36 for electrical tables.

01 Quad 2-Input NAND Gates with Open-Collector Outputs

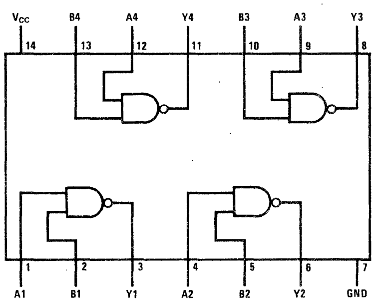
$Y = \overline{AB}$



5401/7401(J), (N); 54LS01/74LS01(J), (N), (W)



5401/7401(W); 54L01/74L01(W)

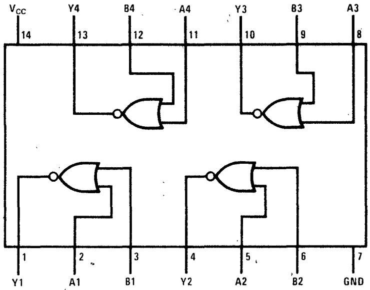


54H01/74H01(J), (N)

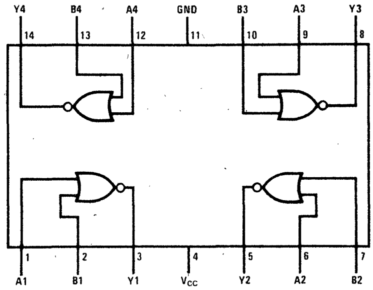
See page 1-38 for electrical tables.

02 Quad 2-Input NOR Gates

$Y = \overline{A+B}$



5402/7402(J), (N); 54L02/74L02(J), (N);
54LS02/74LS02(J), (N), (W); 74S02(N)

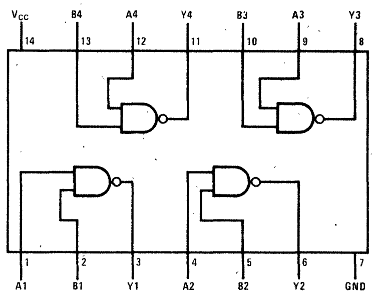


5402/7402(W); 54L02/74L02(W)

See page 1-40 for electrical tables.

03 Quad 2-Input NAND Gates with Open-Collector Outputs

$Y = \overline{AB}$

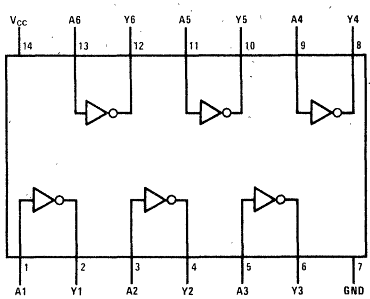


5403/7403(J), (N); 54L03/74L03(J), (N);
54LS03/74LS03(J), (N), (W); 74S03(N)

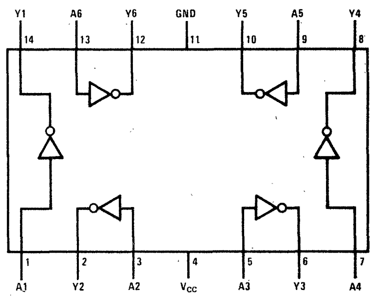
See page 1-38 for electrical tables.

04 Hex Inverters

$Y = \overline{A}$



5404/7404(J), (N); 54H04/74H04(J), (N);
54L04/74L04(J), (N); 54LS04/74LS04(J),(N),(W);
74S04(N)

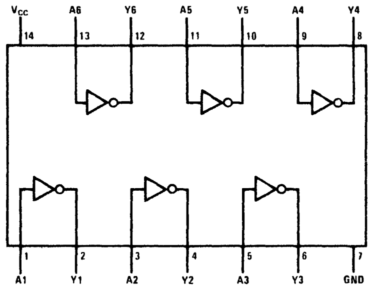


5404/7404(W); 54L04/74L04(W)

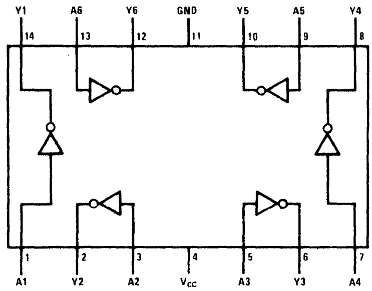
See page 1-36 for electrical tables.

05 Hex Inverters with Open-Collector Outputs

Y = $\overline{A}$



5405/7405(J), (N); 54H05/74H05(J), (N); 54L05/74L05(J), (N); 54LS05/74LS05(J), (N), (W); 74S05(N)

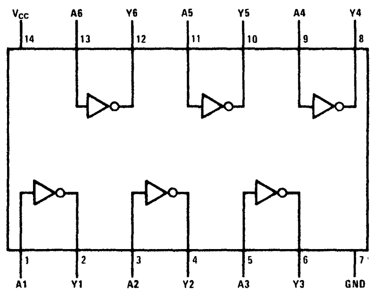


5405/7405(W); 54L05/74L05(W)

See page 1-38 for electrical tables.

06 Hex Buffers with Open-Collector High-Voltage Outputs

Y = $\overline{A}$

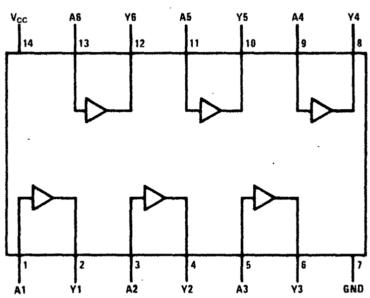


5406/7406(J), (N), (W)

See page 1-42 for electrical tables.

07 Hex Buffers with Open-Collector High-Voltage Outputs

Y = A

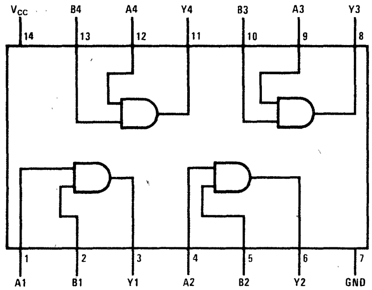


5407/7407(J), (N), (W)

See page 1-42 for electrical tables.

08 Quad 2-Input AND Gates

Y = AB

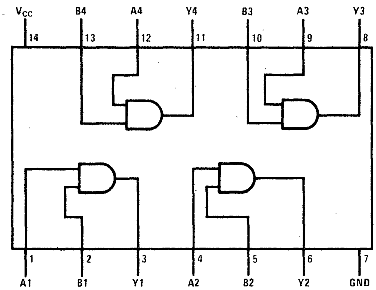


5408/7408(J), (N), (W); 54H08/74H08(J), (N); 54L08/74L08(J), (N), (W); 54LS08/74LS08(J), (N), (W)

See page 1-44 for electrical tables.

09 Quad 2-Input AND Gates with Open-Collector Outputs

Y = AB

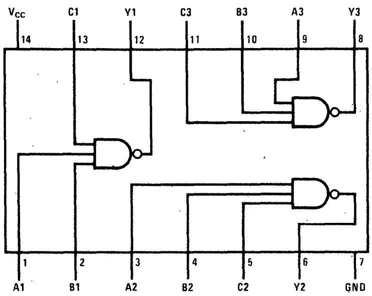


5409/7409(J), (N), (W); 54L09/74L09(J), (N), (W); 54LS09/74LS09(J), (N), (W)

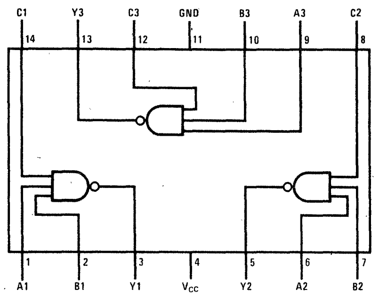
See page 1-46 for electrical tables.

10 Triple 3-Input NAND Gates

$Y = \overline{ABC}$



5410/7410(J), (N); 54H10/74H10(J), (N); 54L10/74L10(J), (N); 54LS10/74LS10(J), (N), (W); 74S10(N)

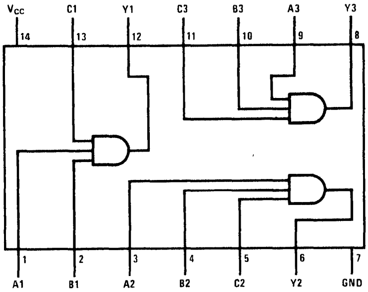


5410/7410(W); 54L10/74L10(W)

See page 1-36 for electrical tables.

11 Triple 3-Input AND Gates

$Y = ABC$

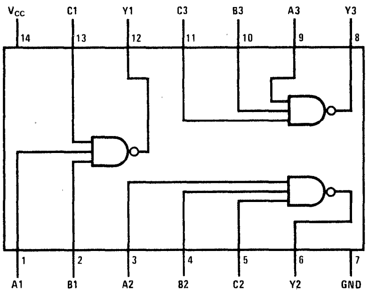


5411/7411(J), (N); 54H11/74H11(J), (N); 54L11/74L11(J), (N), (W); 54LS11/74LS11(J), (N), (W); 74S11(N)

See page 1-44 for electrical tables.

12 Triple 3-Input NAND Gates with Open-Collector Outputs

$Y = \overline{ABC}$

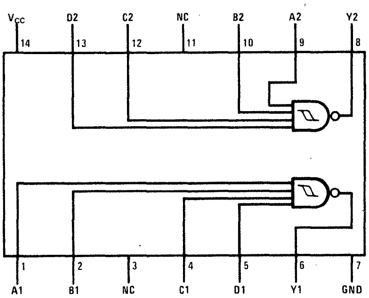


54LS12/74LS12(J), (N), (W)

See page 1-38 for electrical tables.

13 Dual 4-Input NAND Schmitt Triggers

$Y = \overline{ABCD}$

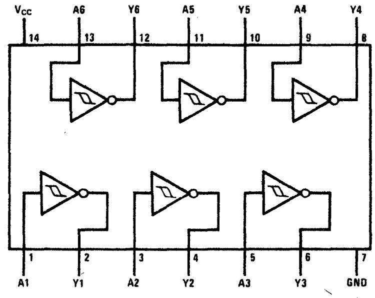


5413/7413(J),(N),(W); 54LS13/74LS13(J),(N),(W)

See page 1-48 for electrical tables.

14 Hex Schmitt Triggers

Y = $\overline{A}$

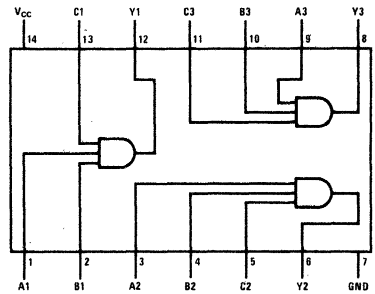


5414/7414(J),(N),(W); 54LS14/74LS14(J),(N),(W)

See page 1-48 for electrical tables.

15 Triple 3-Input AND Gates with Open-Collector Outputs

Y = ABC

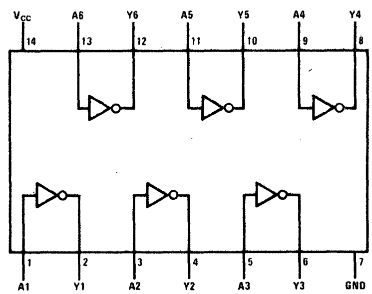


54LS15/74LS15(J),(N),(W); 74S15(N)

See page 1-46 for electrical tables.

16 Hex Buffers with Open-Collector High-Voltage Outputs

Y = $\overline{A}$

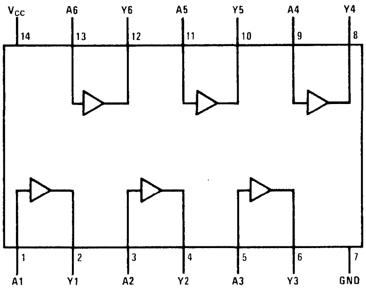


5416/7416(J),(N),(W)

See page 1-42 for electrical tables.

17 Hex Buffers with Open-Collector High-Voltage Outputs

Y = A

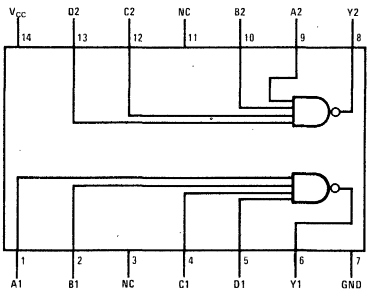


5417/7417(J),(N),(W)

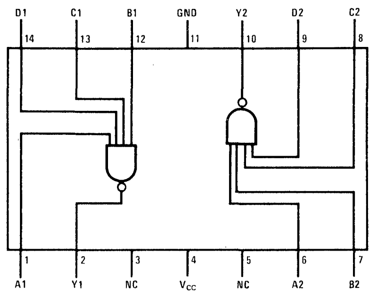
See page 1-42 for electrical tables.

20 Dual 4-Input NAND Gates

Y = $\overline{ABCD}$



5420/7420(J),(N); 54H20/74H20(J),(N); 54L20/74L20(J),(N); 54LS20/74LS20(J),(N),(W); 74S20(N)

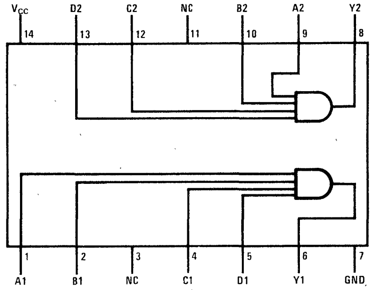


5420/7420(W); 54L20/74L20(W)

See page 1-36 for electrical tables.

21 Dual 4-Input AND Gates

Y = ABCD

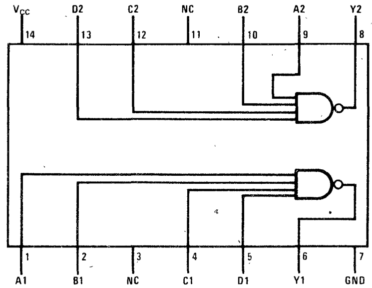


54H21/74H21(J),(N);54LS21/74LS21(J),(N),(W)

See page 1-44 for electrical tables.

22 Dual 4-Input NAND Gates with Open Collector Outputs

$Y = \overline{ABCD}$



54H22/74H22(J),(N); 54LS22/74LS22(J),(N),(W); 74S22(N)

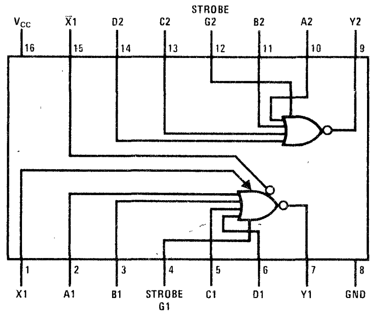
See page 1-38 for electrical tables.

23 Expandable Dual 4-Input NOR Gates with Strobe

$Y1 = \overline{G1\ (A1+B1+C1+D1)+X}$

$Y2 = \overline{G2\ (A2+B2+C2+D2)}$

X = output of 5460/7460

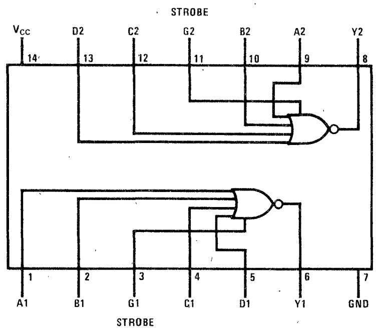


5423/7423(J),(N),(W)

See page 1-50 for electrical tables.

25 Dual 4-Input NOR Gates with Strobe

$Y = \overline{G(A+B+C+D)}$

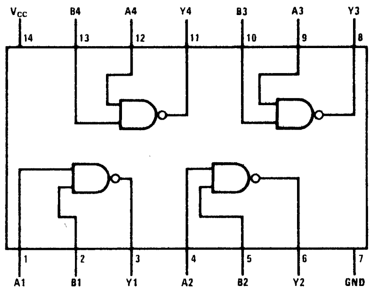


5425/7425(J),(N),(W)

See page 1-40 for electrical tables.

26 Quad 2-Input High-Voltage NAND Gates

$Y = \overline{AB}$

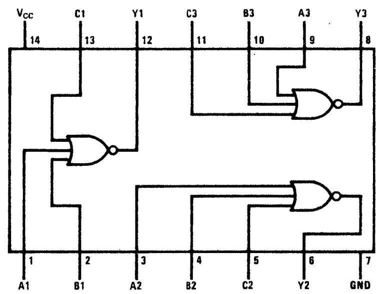


5426/7426(J),(N);54L26/74L26(J),(N);
54LS26/74LS26(J),(N),(W)

See page 1-42 for electrical tables.

27 Triple 3-Input NOR Gates

$Y = \overline{A+B+C}$

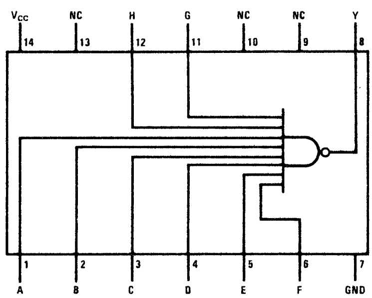


5427/7427(J),(N),(W); 54LS27/74LS27(J),(N),(W)

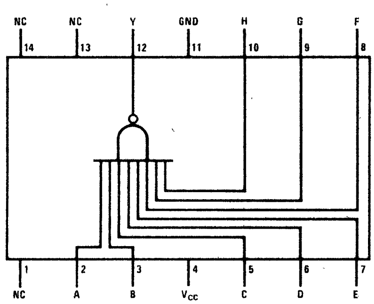
See page 1-40 for electrical tables.

30 8-Input NAND Gates

$Y = \overline{ABCDEFGH}$



5430/7430(J),(N);54H30/74H30(J),(N);
54L30/74L30(J),(N);54LS30/74LS30(J),(N),(W)
74S30(N)

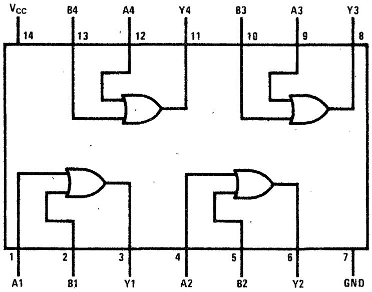


5430/7430(W); 54L30/74L30(W)

See page 1-36 for electrical tables.

32 Quad 2-Input OR Gates

Y = A + B

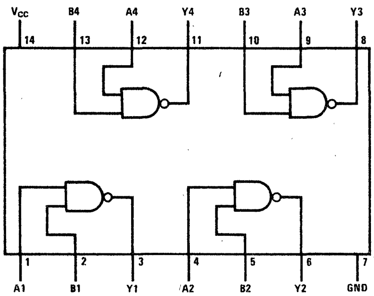


5432/7432(J),(N),(W);54L32/74L32(J),(N),(W);
54LS32/74LS32(J),(N),(W)

See page 1-52 for electrical tables.

37 Quad 2-Input NAND Buffers

$Y = \overline{AB}$

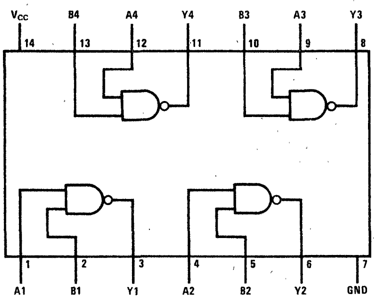


5437/7437(J),(N),(W);54LS37/74LS37(J),(N),(W)

See page 1-54 for electrical tables.

38 Quad 2-Input NAND Buffers with Open-Collector Outputs

$Y = \overline{AB}$

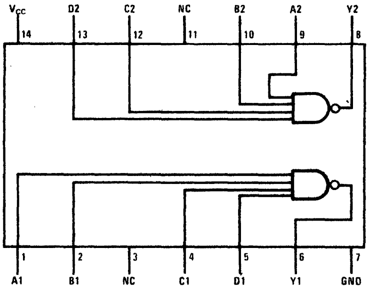


5438/7438(J),(N),(W);54LS38/74LS38(J),(N),(W)

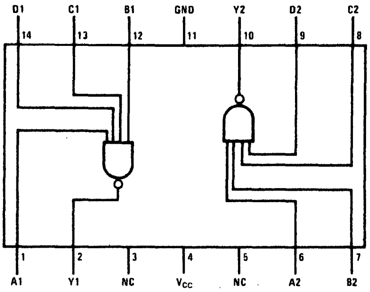
See page 1-42 for electrical tables.

40 Dual 4-Input NAND Buffers

$Y = \overline{ABCD}$



5440/7440(J), (N); 54H40/74H40(J), (N);
54LS40/74LS40(J), (N), (W); 74S40(N)



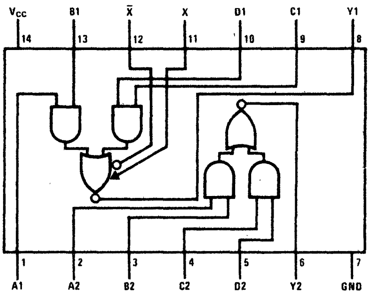
5440/7440(W)

See page 1-54 for electrical tables.

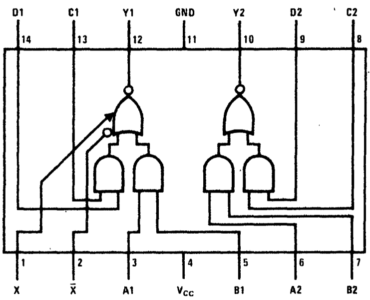
50 Dual 2-Wide, 2-Input, AND-OR-INVERT Gates

$Y = \overline{AB+CD+X}$

50: X = output of 5460/7460
H50: X = output of 54H60/74H60 or 54H62/74H62



5450/7450(J), (N); 54H50/74H50(J), (N)



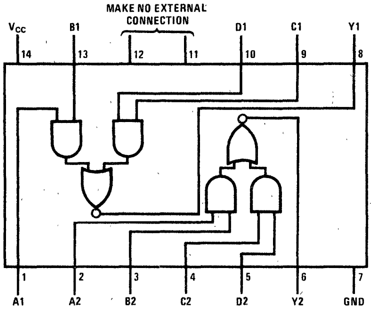
5450/7450(W)

See page 1-50 for electrical tables.

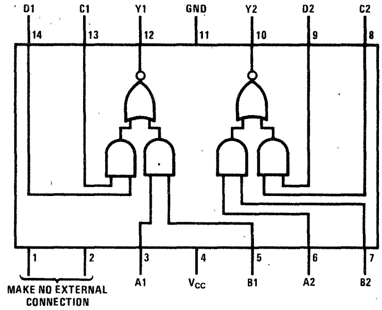
51 Dual 2-Wide, 2-Input AND-OR-INVERT Gates

51, H51, S51

$Y = \overline{AB+CD}$



5451/7451(J), (N); 54H51/74H51(J), (N); 74S51(N)

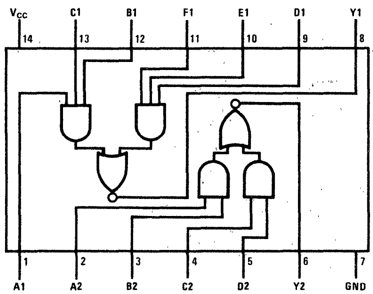


5451/7451(W)

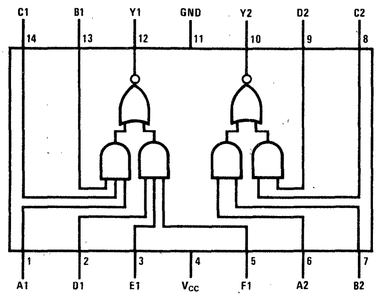
L51, LS51

$Y1 = \overline{(A1 \cdot B1 \cdot C1) + (D1 \cdot E1 \cdot F1)}$

$Y2 = \overline{(A2 \cdot B2) + (C2 \cdot D2)}$



54L51/74L51(J),(N); 54LS51/74LS51(J),(N),(W)

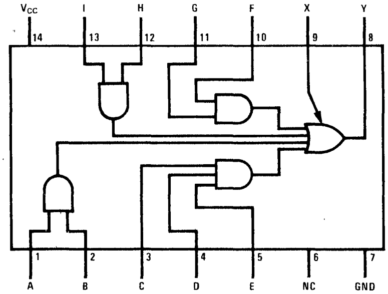


54L51/74L51(W)

See page 1-56 for electrical tables.

52 Expandable 4-Wide AND-OR Gates

Y = AB+CDE+FG+HI+X
X = output of 54H61/74H61

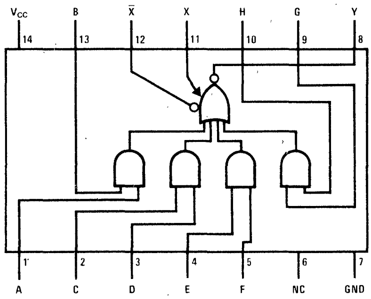


54H52/74H52(J), (N)

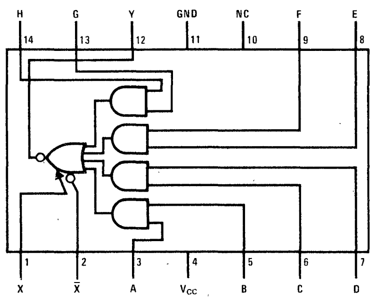
See page 1-50 for electrical tables.

53 Expandable 4-Wide AND-OR-INVERT Gates

53
$Y = \overline{AB+CD+EF+GH+X}$
X = output of 5460/7460

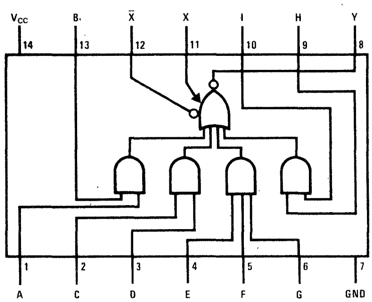


5453/7453(J), (N)



5453/7453(W)

H53
$Y = \overline{AB+CD+EFG+HI+X}$
X = output of 54H60/74H60
or 54H62/74H62

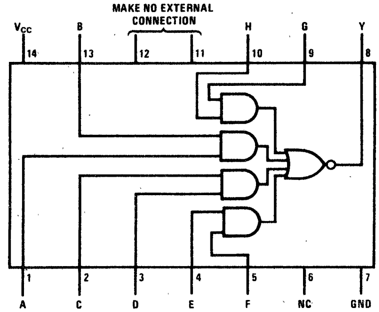


54H53/74H53(J), (N)

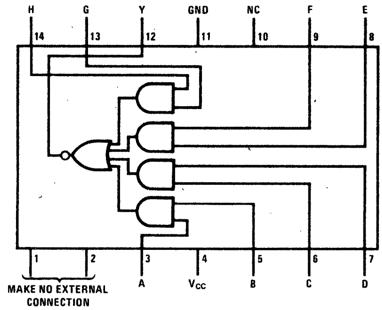
See page 1-50 for electrical tables.

54 4-Wide AND-OR-INVERT Gates

54
$Y = \overline{AB+CD+EF+GH}$



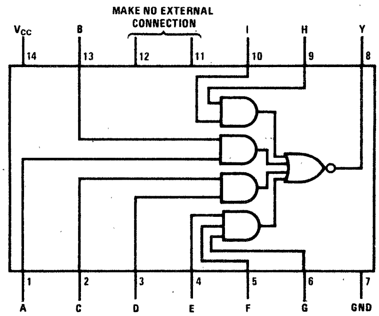
5454/7454(J), (N)



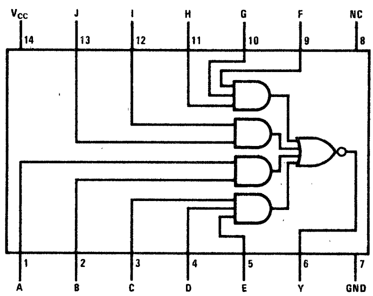
5454/7454(W)

H54
$Y = \overline{AB+CD+EFG+HI}$

L54(J, N), LS54
$Y = \overline{AB+CDE+FGH+IJ}$

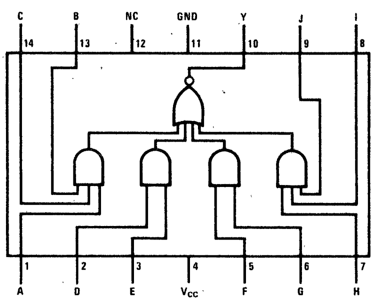


54H54/74H54(J), (N)



54L54/74L54(J),(N); 54LS54/74LS54(J),(N),(W)

L54(W)
$Y = \overline{ABC+DE+FG+HIJ}$



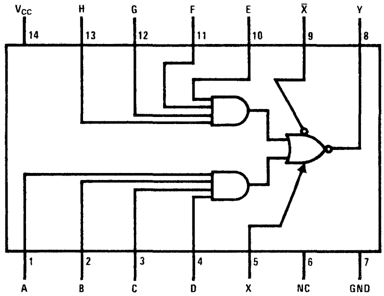
54L54/74L54(W)

See page 1-56 for electrical tables.

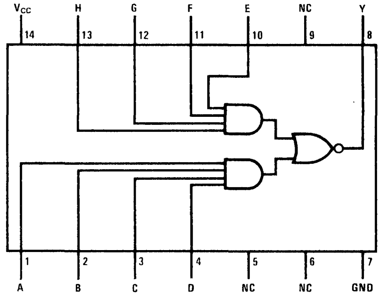
55 2-Wide, 4-Input AND-OR-INVERT Gates

H55 (EXPANDABLE)
Y = $\overline{ABCD+EFGH+X}$
X = output of 54H60/74H60 or 54H62/74H62

L55(J, N), LS55
Y = $\overline{ABCD+EFGH}$

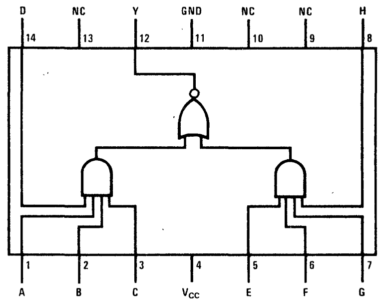


54H55/74H55(J),(N)



54L55/74L55(J),(N); 54LS55/74LS55(J),(N),(W)

L55(W)
Y = $\overline{ABCD+EFGH}$



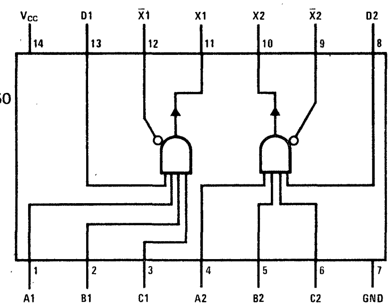
54L55/74L55(W)

See page 1-50 (H55), 1-56 (L55 and LS55) for electrical tables.

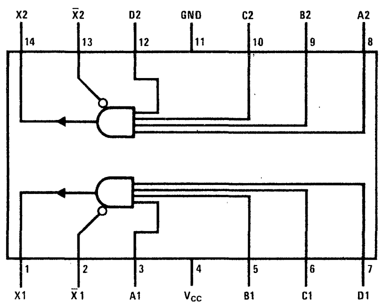
60 Dual 4-Input Expanders

60
X = ABCD when connected to X and $\overline{X}$ inputs of 5423/7423, 5450/7450 or 5453/7453

H60
X = ABCD when connnected to X and $\overline{X}$ inputs of 54H50/74H50, 54H53/74H53, or 54H55/74H55



5460/7460(J),(N); 54H60/74H60(J),(N)

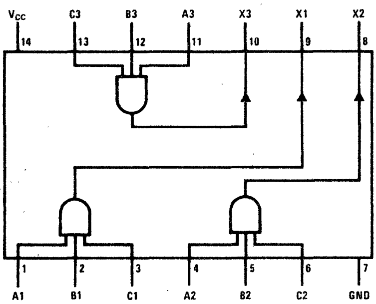


5460/7460(W)

See page 1-58 (60), 1-59 (H60) for electrical tables.

61 Triple 3-Input Expanders

X = ABC when connected to X input of 54H52/74H52

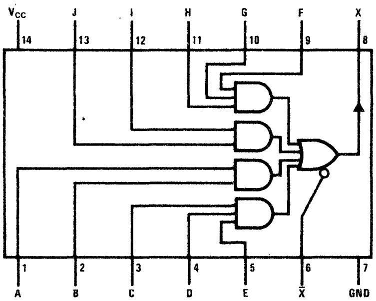


54H61/74H61(J),(N)

See page 1-60 for electrical tables.

62 4-Wide AND-OR Expander

X = AB + CDE + FGH + IJ when connected to X and $\overline{X}$ inputs of 54H50/74H50, 54H53/74H53 or 54H55/74H55

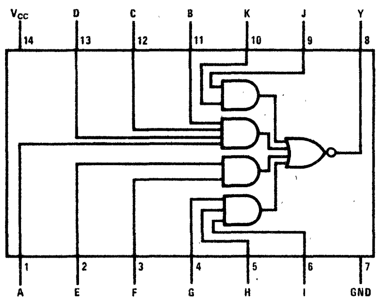


54H62/74H62(J),(N)

See page 1-59 for electrical tables.

64 4 Wide AND-OR-INVERT Gates

$Y = \overline{ABCD + EF + GHI + JK}$

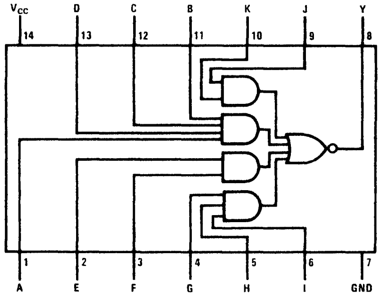


74S64(N)

See page 1-56 for electrical tables.

65 4 Wide AND-OR-INVERT Gates with Open-Collector Outputs

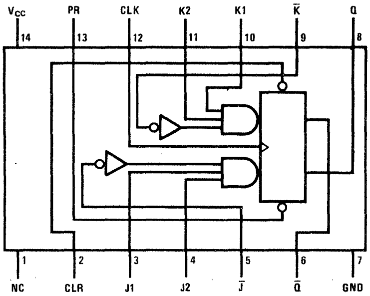
$Y = \overline{ABCD + EF + GHI + JK}$



74S65(N)

See page 1-61 for electrical tables.

70 AND-Gated J-K Positive-Edge-Triggered Flip-Flops with Preset and Clear

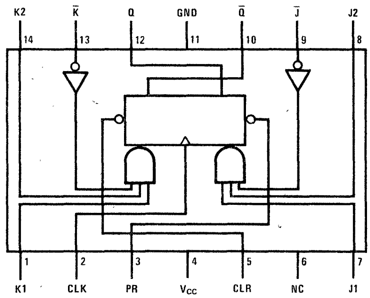


5470/7470(J),(N)

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	Q0	$\bar{Q}$0
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q0	$\bar{Q}$0

$J = J1 \cdot J2 \cdot \bar{J}$
$K = K1 \cdot K2 \cdot \bar{K}$
If inputs $\bar{J}$ and $\bar{K}$ are not used, they must be grounded.
Preset or Clear function can occur only when clock input is low.



5470/7470(W)

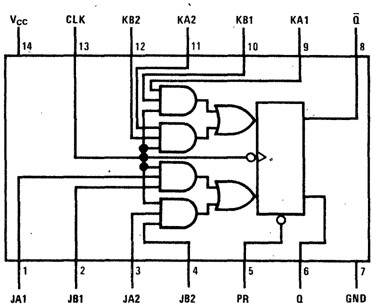
See page 1-62 for electrical tables.

H71 AND-OR-Gated J-K Master-Slave Flip-Flops with Preset

TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	⎍	L	L	Q0	$\bar{Q}$0
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

J = (J1A · J1B) + (J2A · J2B)
K = (K1A · K1B) + (K2A · K2B)

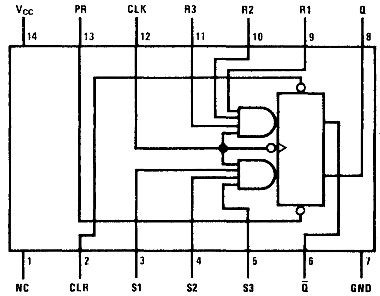


54H71/74H71(J),(N)

See page 1-64 for electrical tables.

Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

L71 AND-Gated R-S Master-Slave Flip-Flops with Preset and Clear

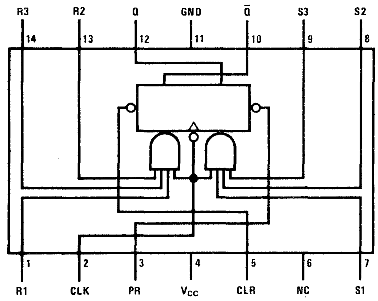


54L71/74L71(J),(N)

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	S	R	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q0	Q̄0
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	INDETERMINATE	

R = R1 · R2 · R3
S = S1 · S2 · S3



54L71/74L71(W)

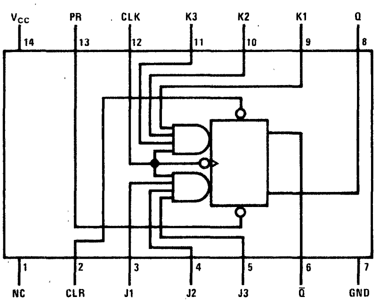
See page 1-66 for electrical tables.

72 AND-Gated J-K Master-Slave Flip-Flops with Preset and Clear

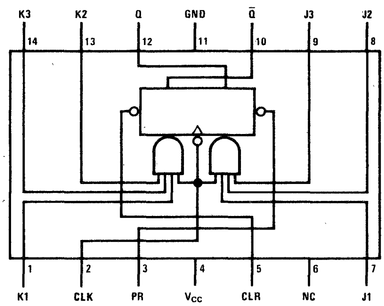
TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q0	Q̄0
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

J = J1·J2·J3
K = K1·K2·K3



5472/7472(J),(N);54H72/74H72(J),(N);
54L72/74L72(J),(N)



5472/7472(W);54L72/74L72(W)

See page 1-62 (72), 1-64 (H72), 1-66 (L72) for electrical tables.

Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

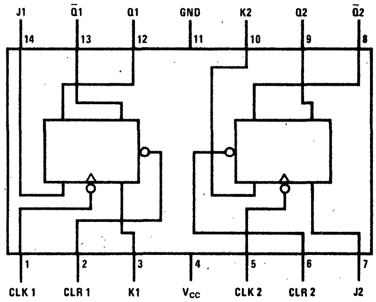
73 Dual J-K Flip-Flops with Clear

TRUTH TABLE
73, H73, L73

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q0	$\overline{Q}0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

TRUTH TABLE
LS73

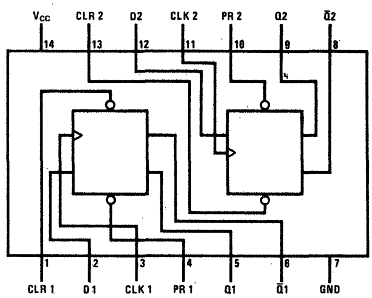
INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}0$



5473/7473(J), (N), (W); 54H73/74H73(J), (N); 54L73/74L73 (J), (N), (W); 54LS73/74LS73(J), (N), (W)

See page 1-62 (73), 1-64 (H73), 1-66 (L73), 1-68 (LS73) for electrical tables.

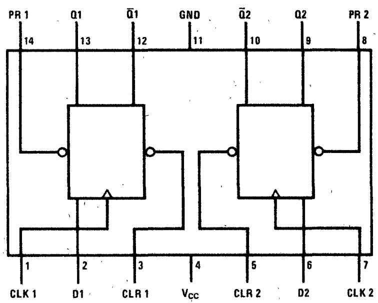
74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear



TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}0$

5474/7474(J),(N); 54H74/74H74(J),(N); 54L74/74L74(J),(N); 54LS74/74LS74(J),(N),(W); 74S74(N)



5474/7474(W); 54L74/74L74(W)

See page 1-62 (74), 1-64 (H74), 1-66 (L74), 1-68 (LS74), 1-70 (S74) for electrical tables.

Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

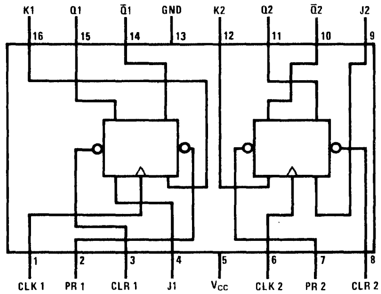
76 Dual J-K Flip-Flops with Preset and Clear

TRUTH TABLE
76, H76

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q0	Q̄0
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

TRUTH TABLE
LS76

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	Q̄0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	Q̄0



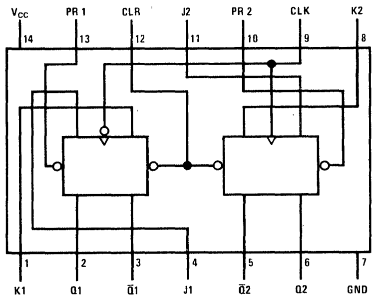
5476/7476(J), (N), (W); 54H76/74H76(J), (N); 54LS76/74LS76(J), (N), (W)

See page 1-62 (76), 1-64 (H76), 1-68 (LS76) for electrical tables.

78 Dual J-K Flip-Flops with Preset, Common Clear, and Common Clock

TRUTH TABLE
H78, L78

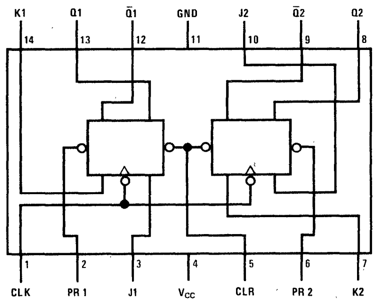
INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q0	Q̄0
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	



54H78/74H78(J),(N)

TRUTH TABLE
LS78

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	Q̄0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	Q̄0



54L78/74L78(J), (N), (W); 54LS78/74LS78(J), (N), (W)

See page 1-64 (H78), 1-66 (L78), 1-68 (LS78) for electrical tables.

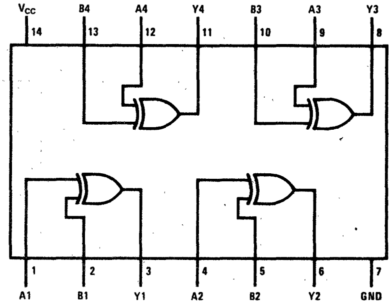
Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

86 Quad 2-Input EXCLUSIVE-OR Gates

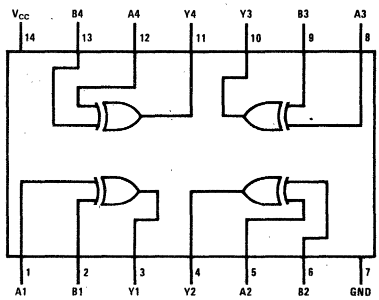


5486/7486(J), (N), (W);
54LS86/74LS86(J), (N), (W); 74S86(N)

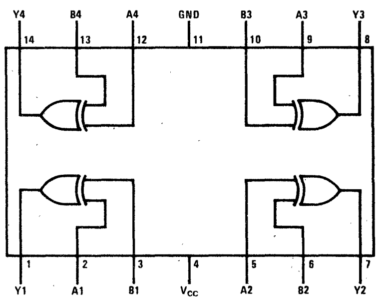
TRUTH TABLE
(86, L86, LS86, S86)

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$



54L86/74L86(J),(N)



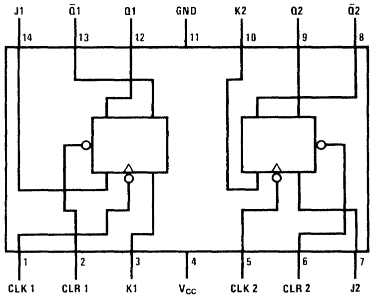
54L86/74L86(W)

See page 1-72 for electrical tables.

103 Dual J-K Negative-Edge-Triggered Flip-Flops with Clear

TRUTH TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}0$



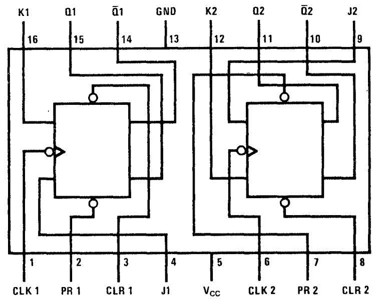
54H103/74H103(J),(N)

See page 1-74 for electrical tables.

106 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}0$



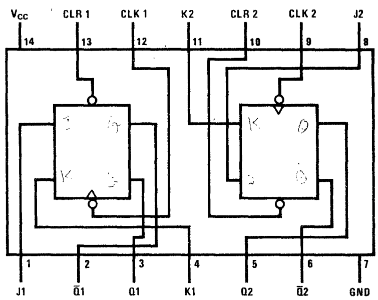
54H106/74H106(J), (N)

See page 1-74 for electrical tables.

107 Dual J-K Master-Slave Flip-Flops with Clear

TRUTH TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q0	$\overline{Q}0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	



54107/74107(J),(N); 54LS107/74LS107(J), (N), (W)

See page 1-62 (107), 1-68 (LS107) for electrical tables.

Notes: ⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q0 = the level of Q before the indicated input conditions were established.

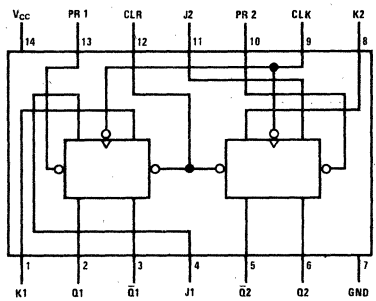
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

108 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear, and Common Clock

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\bar{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\bar{Q}$0



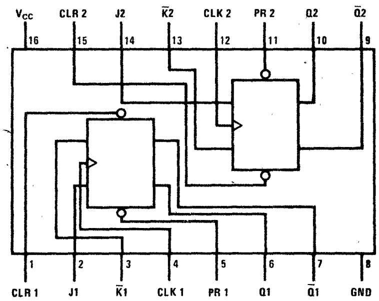
54H108/74H108(J), (N)

See page 1-74 for electrical tables.

109 Dual J-$\bar{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\bar{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\bar{Q}$0



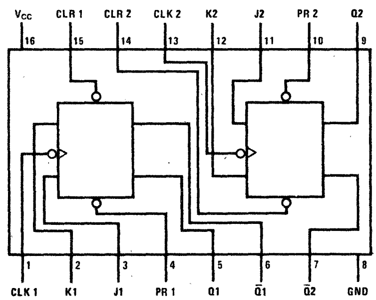
54109/74109(J), (N), (W);
54LS109/74LS109(J), (N), (W)

See page 1-62 (109), 1-68 (LS109) for electrical tables.

112 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\bar{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\bar{Q}$0



54LS112/74LS112(J), (N), (W); 74S112(N)

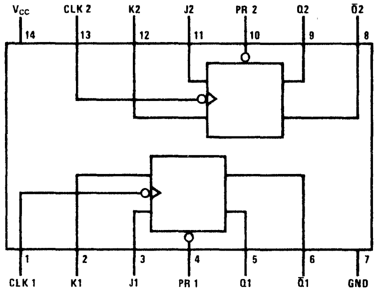
See page 1-68 (LS112), 1-70 (S112) for electrical tables.

Notes: Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

113 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0



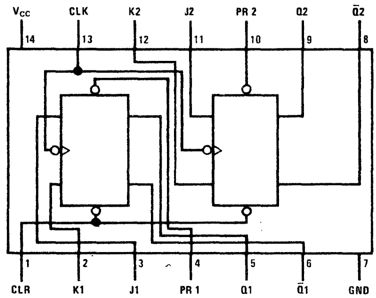
54LS113/74LS113(J), (N), (W); 74S113(N)

See page 1-68 (LS113), 1-70 (S113) for electrical tables.

114 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear, and Common Clock

TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

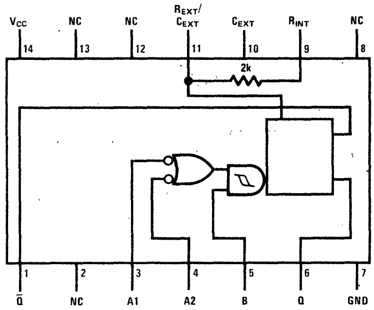


54LS114/74LS114(J), (N), (W); 74S114(N)

See page 1-68 (LS114), 1-70 (S114) for electrical tables.

Notes: Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

121 One Shots



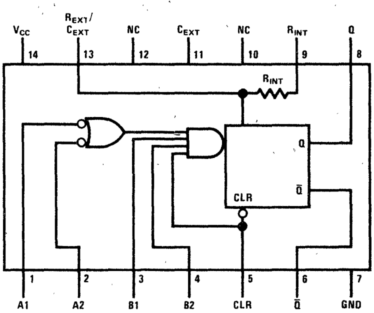
54121/74121(J), (N), (W)

TRUTH TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	Q̄
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⊓	⊔
↓	H	H	⊓	⊔
↓	↓	H	⊓	⊔
L	X	↑	⊓	⊔
X	L	↑	⊓	⊔

See page 1-76 for electrical tables.

122 Retriggerable One Shots with Clear



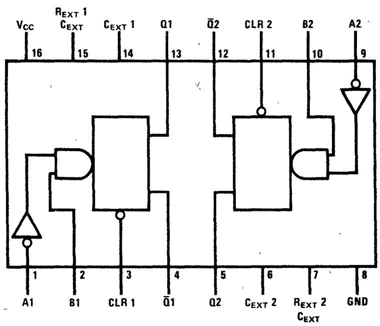
54LS122(J), (W); 74LS122(J), (N)

TRUTH TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	Q̄
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⊓	⊔
H	L	X	H	↑	⊓	⊔
H	X	L	H	H	L	H
H	X	L	↑	H	⊓	⊔
H	X	L	H	↑	⊓	⊔
H	H	↓	H	H	⊓	⊔
H	↓	↓	H	H	⊓	⊔
H	↓	H	H	H	⊓	⊔
↑	L	X	H	H	⊓	⊔
↑	X	L	H	H	⊓	⊔

See page 1-78 for electrical tables.

123,123A Dual Retriggerable One Shots with Clear



54123/74123(J), (N), (W);
54L123A/74L123A(J), (N), (W);
54LS123/74LS123(J), (N), (W)

TRUTH TABLE

INPUTS			OUTPUTS	
A	B	CLR	Q	Q̄
H	X	H	L	H
X	L	H	L	H
L	↑	H	⊓	⊔
↓	H	H	⊓	⊔
X	X	L	L	H

See page 1-78 for electrical tables.

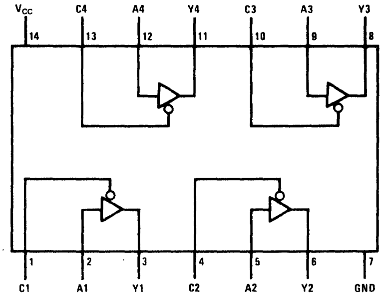
Notes: ⊓ = one high-level pulse, ⊔ = one low-level pulse.
To use the internal timing resistor of 54121/74121, connect R_{INT} to V_{CC}.
An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC} with R_{INT} open-circuited.
To obtain variable pulse widths, connect external variable resistance between R_{INT} or R_{EXT}/C_{EXT} and V_{CC}.

125 TRI-STATE Quad Buffers

TRUTH TABLE

INPUTS		OUTPUT
A	C	Y
H	L	H
L	L	L
X	H	Hi-Z

Y = A



54125/74125(J), (N), (W);
54LS125/74LS125(J), (N), (W)

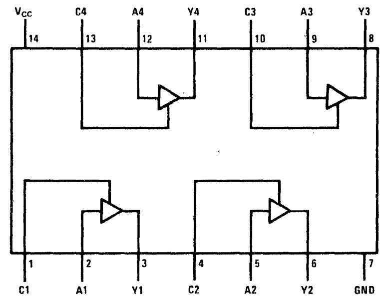
See page 1-80 for electrical tables.

126 TRI-STATE Quad Buffers

TRUTH TABLE

INPUTS		OUTPUT
A	C	Y
H	H	H
L	H	L
X	L	Hi-Z

Y = A

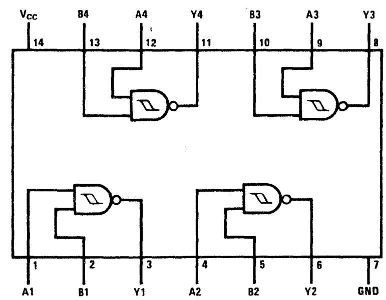


54126/74126(J), (N), (W);
54LS126/74LS126(J), (N), (W)

See page 1-80 for electrical tables.

132 Quad 2-Input NAND Schmitt Triggers

$Y = \overline{AB}$

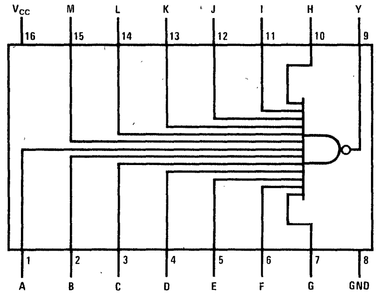


54132/74132(J), (N), (W);
54LS132/74LS132(J), (N), (W)

See page 1-48 for electrical tables.

133 13-Input NAND Gates

$Y = \overline{ABCDEFGHIJKLM}$



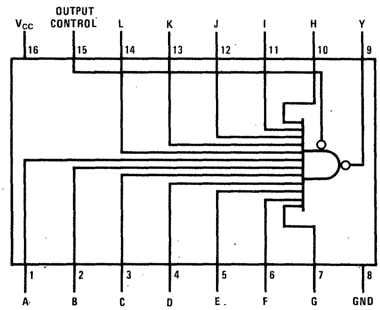
74S133(N)

See page 1-36 for electrical tables.

134 TRI-STATE 12-Input NAND Gates

$Y = \overline{ABCDEFGHIJKL}$

Output is off (disabled) when output control is high.



74S134(N)

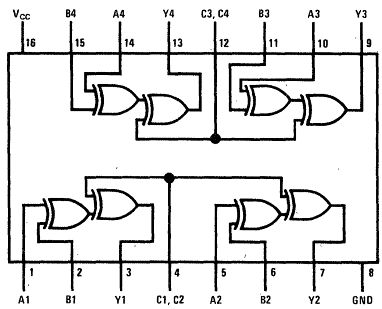
See page 1-80 for electrical tables.

135 Quad EXCLUSIVE-OR/NOR Gates

TRUTH TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

$Y = (A \oplus B) \oplus C =$
$A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$



74S135(N)

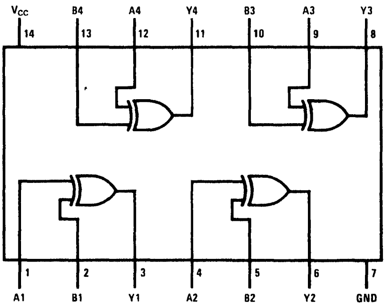
See page 1-82 for electrical tables.

136 Quad EXCLUSIVE-OR Gates with Open-Collector Outputs

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

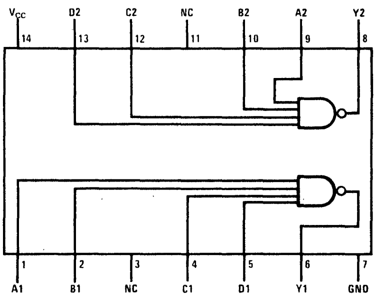


54LS136/74LS136(J), (N), (W)
74S136(N)

See page 1-84 for electrical tables.

140 Dual 50-Ohm Line Drivers

$Y = \overline{ABCD}$



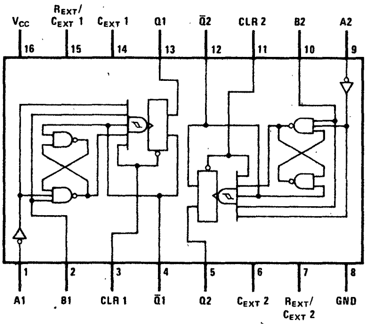
74S140(N)

See page 1-54 for electrical tables.

221 Dual One Shots with Schmitt-Trigger Inputs

TRUTH TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔



54LS221/74LS221(J), (N), (W)

See page 1-76 for electrical tables.

Notes: ⎍ = one high-level pulse, ⊔ = one low-level pulse.

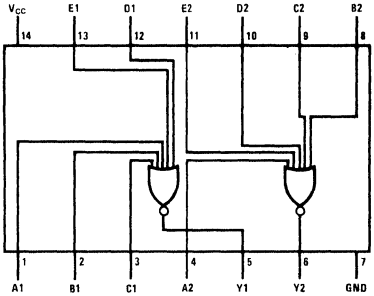
An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).

For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC}.

To obtain variable pulse widths, connect external variable resistance between R_{EXT}/C_{EXT} and V_{CC}.

260 Dual 5-Input NOR Gates

$Y = \overline{A+B+C+D+E}$



74S260(N)

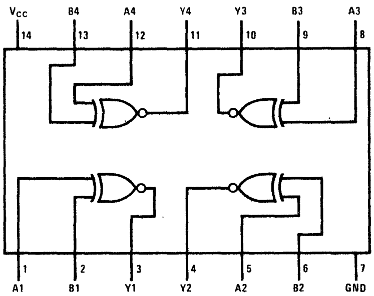
See page 1-40 for electrical tables.

266 Quad EXCLUSIVE-NOR Gates with Open-Collector Outputs

TRUTH TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	L
H	L	L
H	H	H

$Y = \overline{A \oplus B} = AB + \overline{A}\overline{B}$



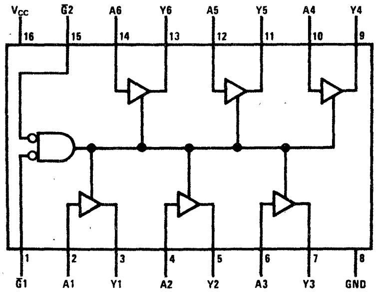
54LS266/74LS266(J), (N), (W)

See page 1-84 for electrical tables.

365 TRI-STATE Hex Buffers

TRUTH TABLE

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L



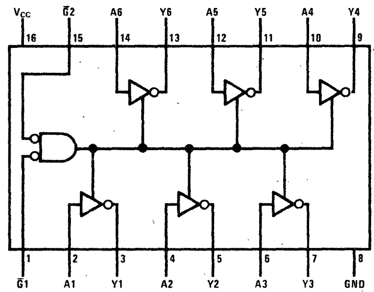
54365(J), (W)/74365(J), (N), (W); 54LS365/74LS365(J), (N), (W)

See page 1-86 for electrical tables.

366 TRI-STATE Hex Buffers

TRUTH TABLE

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H



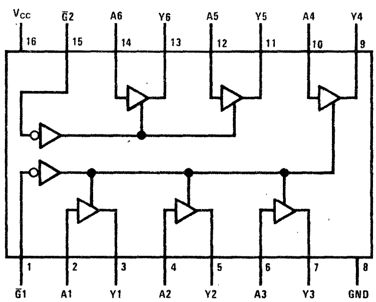
54366(J), (W)/74366(J), (N), (W); 54LS366/74LS366(J), (N), (W)

See page 1-86 for electrical tables.

367 TRI-STATE Hex Buffers

TRUTH TABLE

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L



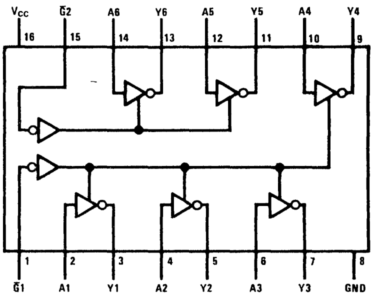
54367(J), (W)/74367(J), (N), (W); 54LS367/74LS367(J), (N), (W)

See page 1-86 for electrical tables.

368 TRI-STATE Hex Buffers

TRUTH TABLE

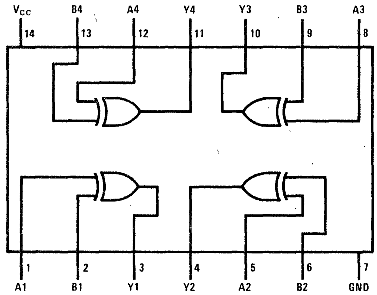
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H



54368(J), (W)/74368(J), (N), (W); 54LS368/74LS368(J), (N), (W)

See page 1-86 for electrical tables.

386 Quad EXCLUSIVE-OR Gates



54LS386/74LS386(J), (N), (W)

TRUTH TABLE

INPUTS		OUTPUT
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

See page 1-72 for electrical tables.

National Semiconductor 54/74 SSI DEVICES Electrical Tables Section 1

Max Ratings/Operating Conditions

RATINGS		54/74 SERIES	54H/74H SERIES	54L/74L SERIES	54LS/74LS SERIES DIODE INPUTS	54LS/74LS SERIES EMITTER INPUTS	54S/74S SERIES	UNITS
Maximum Allowable Supply Voltage		7	7	8	7	7	7	V
Guaranteed Operating Supply Voltage Range	54	4.50 to 5.50						V
	74	4.75 to 5.25						
Maximum Input Voltage		5.5	5.5	5.5	7	5.5	5.5	V
Maximum Voltage to Open-Collector Outputs*		7	7	8	7	7	7	V
Operating Free-Air Temperature Range	54	−55 to +125						°C
	74	0 to +70						
Storage Temperature Range		−65 to +150						°C

***Except for selected high voltage types, as specified in electrical tables.**

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		CONDITIONS			DM54/74 00, 04 10, 20, 30			DM54H/74H H00, H04 H10, H20, H30			DM54L/74L L00, L04 L10, L20, L30			DM54LS/74LS LS00 LS04, LS10 LS20, LS30			DM74S S00, S04 S10, S20 S30, S133			UNITS
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage				2			2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7			0.7			N/A	V
				DM74			0.8			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −8 mA							−1.5			N/A							V
			I_I = −12 mA				−1.5						N/A							
			I_I = −18 mA										N/A			−1.5			−1.2	
I_{OH}	High Level Output Current						−400			−500			−200			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		N/A			V
				DM74	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			20			2			4			N/A	mA
				DM74			16			20			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			N/A	V
				DM74		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74												0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			1			0.1						1	mA
			V_I = 7V													0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			50			10							μA
			V_I = 2.7V													20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V										−0.18							mA
			V_I = 0.4V	LS30												−0.4				
				Others			−1.6			−2						−0.36				
			V_I = 0.5V																−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−55	−40		−100	−3		−15	−30		−130			N/A	mA
				DM74	−18		−55	−40		−100	−3		−15	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			See Table															

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54H/DM74H, DM54LS/DM74LS and DM74S, duration of short circuit should not exceed one second.

(3) National Semiconductor temporarily reserves the right to ship DM54/DM74LS00, LS04, LS10, LS20, LS30 devices which have a minimum I_{OS} = 5.0 mA.

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
00	4	8	12	22
04	6	12	18	33
10	3	6	9	16.5
20	2	4	6	11
30	1	2	3	6
H00	10	16.8	26	40
H04	16	26	40	58
H10	7.5	12.6	19.5	30
H20	5	8.4	13	20
H30	2.5	4.2	6.5	10
L00	0.44	0.8	1.16	2.04
L04	0.66	1.2	1.74	3.06
L10	0.33	0.6	0.87	1.53
L20	0.22	0.4	0.58	1.02
L30	0.11	0.2	0.29	0.51
LS00	0.8	1.6	2.4	4.4
LS04	1.2	2.4	3.6	6.6
LS10	0.6	1.2	1.8	3.3
LS20	0.4	0.8	1.2	2.2
LS30	0.35	0.5	0.6	1.1
S00	10	16	20	36
S04	15	24	30	54
S10	7.5	12	15	27
S20	5	8	10	18
S30	3	5	5.5	10
S133	3	5	5.5	10

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
00, 10	$C_L = 15$ pF, $R_L = 400\Omega$		11	22		7	15
04, 20			12	22		8	15
30			13	22		8	15
H00	$C_L = 25$ pF, $R_L = 280\Omega$		5.9	10		6.2	10
H04			6	10		6.5	10
H10			5.9	10		6.3	10
H20			6	10		7	10
H30			6.8	10		8.9	12
L00, L04 L10, L20	$C_L = 50$ pF, $R_L = 4$ kΩ		35	60		31	60
L30			35	60		70	100
LS00, LS04 LS10, LS20	$C_L = 15$ pF, $R_L = 2$ kΩ		9	15		10	15
LS30			9	15		15	20
S00, S04	$C_L = 15$ pF, $R_L = 280\Omega$	2	3	4.5	2	3	5
S10, S20	$C_L = 50$ pF, $R_L = 280\Omega$		4.5	7		5	8
S30, S133	$C_L = 15$ pF, $R_L = 280\Omega$	2	4	6	2	4.5	7
	$C_L = 50$ pF, $R_L = 280\Omega$		5.5	8		6.5	10

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		CONDITIONS			DM54/74 01, 03 05 MIN	TYP(1)	MAX	DM54H/74H H01 H05, H22 MIN	TYP(1)	MAX	DM54L/74L L01, L03 L05 MIN	TYP(1)	MAX	DM54LS/74LS LS01, LS03 LS05, LS12, LS22 MIN	TYP(1)	MAX	DM74S S03 S05, S22 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.6			0.7			N/A	V
				DM74			0.8			0.8			0.6			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −8 mA							−1.5			N/A							V
			I_I = −12 mA				−1.5						N/A							
			I_I = −18 mA										N/A			−1.5			−1.2	
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IL} = Max V_{OH} = 5.5V					250			250			50			100			250	µA
V_{OH}	High Level Output Voltage						5.5			5.5			5.5			5.5			5.5	V
I_{OL}	Low Level Output Current			DM54			16			20			2			4			N/A	mA
				DM74			16			20			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IH} = 2V	I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			N/A	V
				DM74		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74												0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			1			0.1						1	mA
			V_I = 7V													0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			50			10							µA
			V_I = 2.7V													20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V										−0.18							mA
			V_I = 0.4V				−1.6			−2						−0.36				
			V_I = 0.5V																−2	
I_{CC}	Supply Current	V_{CC} = Max			See Table															

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
01	4	8	12	22
03	4	8	12	22
05	6	12	18	33
H01	6.8	10	26	40
H05	16	26	40	58
H22	3.4	5	13	20
L01	0.44	0.8	1.16	2.04
L03	0.44	0.8	1.16	2.04
L05	0.66	1.20	1.74	3.06
LS01	0.8	1.6	2.4	4.4
LS03	0.8	1.6	2.4	4.4
LS05	1.2	2.4	3.6	6.6
LS12	0.7	1.4	1.8	3.3
LS22	0.4	0.8	1.2	2.2
S03	6	13.2	20	36
S05	9	19.8	30	54
S22	3	6.6	10	18

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
01, 03	C_L = 15 pF R_L = 4 kΩ for t_{PLH} R_L = 400Ω for t_{PHL}		35	45		8	15
05			40	55		8	15
H01, H05 H22	C_L = 25 pF R_L = 280Ω		10	15		7.5	12
L01, L03 L05	C_L = 50 pF R_L = 4 kΩ		60	90		33	60
LS01, LS03 LS05, LS12 LS22	C_L = 15 pF R_L = 2 kΩ		17	32		15	28
S03, S05 S22	C_L = 15 pF R_L = 280Ω	2	5	7.5	2	4.5	7
	C_L = 50 pF R_L = 280Ω		7.5	11		7	11

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	Parameter	Conditions		DM54/74 02, 25, 27 MIN	TYP(1)	MAX	DM54L/74L L02 MIN	TYP(1)	MAX	DM54LS/74LS LS02, LS27 MIN	TYP(1)	MAX	DM74S S02, S260 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7			0.7			N/A	V
			DM74			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA			−1.5			N/A							V
		V_{CC} = Min	I_I = −18 mA						N/A			−1.5			−1.2	
I_{OH}	High Level Output Current		25, 27			−800										µA
			Others			−400			−200			−400			−1000	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max	LS27							2.4						V
			Others DM54	2.4	3.4		2.4	3.3		2.5	3.4		N/A			
			Others DM74	2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current		DM54			16			2			4			N/A	mA
			DM74			16			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OL} = Max, DM54		0.2	0.4		0.15	0.3		0.25	0.4			N/A	V
			I_{OL} = Max, DM74		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA, DM74									0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V			1			0.1						1	mA
		V_{CC} = Max	V_I = 7V									0.1				
I_{IH}	High Level Input Current: Data Inputs	V_{CC} = Max	V_I = 2.4V			40			10							µA
	High Level Input Current: Strobe of 25	V_{CC} = Max	V_I = 2.4V			160			N/A							
	High Level Input Current: All Inputs	V_{CC} = Max	V_I = 2.7V									20			50	
I_{IL}	Low Level Input Current: All Inputs	V_{CC} = Max	V_I = 0.3V						−0.18							mA
	Low Level Input Current: Data Inputs	V_{CC} = Max	V_I = 0.4V			−1.6						−0.36				
	Low Level Input Current: Strobe of 25	V_{CC} = Max	V_I = 0.4V			−6.4						N/A				
	Low Level Input Current: All Inputs	V_{CC} = Max	V_I = 0.5V												−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)	DM54	−20		−55	−3		−15	−30		−130			N/A	mA
			DM74	−18		−55	−3		−15	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max		See Table												

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/DM74LS and DM74S, duration of short circuit should not exceed one second.

(3) National Semiconductor temporarily reserves the right to ship DM54/DM74LS02, LS27 devices which have a minimum I_{OS} = 5.0 mA.

74S260 To Be Announced In 1976

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
02	8	16	14	27
25	8	16	10	19
27	10	16	16	26
L02	0.8	1.6	1.4	2.6
LS02	1.6	3.2	2.8	5.4
LS27	2.0	4	3.4	6.8
S02	17	29	26	45
S260	17	29	26	45

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
02	$C_L = 15$ pF, $R_L = 400\Omega$		12	22		8	15
25	$C_L = 15$ pF, $R_L = 400\Omega$		13	22		8	15
27	$C_L = 15$ pF, $R_L = 400\Omega$		7	11		10	15
L02	$C_L = 50$ pF, $R_L = 4$ kΩ		31	60		35	60
LS02, LS27	$C_L = 15$ pF, $R_L = 2$ kΩ		10	15		10	15
S02	$C_L = 15$ pF, $R_L = 280\Omega$		3.5	5.5		3.5	5.5
	$C_L = 50$ pF, $R_L = 280\Omega$		5	7.5		5	7.5
S260	$C_L = 15$ pF, $R_L = 280\Omega$		4	5.5		4	6

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER	CONDITIONS			DM54/74									DM54L/74L			DM54LS/74LS						UNITS
				06, 07, 16, 17			26			38			L26			LS26			LS38			
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH} High Level Input Voltage				2			2			2			2			2			2			V
V_{IL} Low Level Input Voltage			DM54			0.8			0.8			0.8			0.7			0.7			0.7	V
			DM74			0.8			0.8			0.8			0.7			0.8			0.8	
V_I Input Clamp Voltage	V_{CC} = Min	$I_I = -12$ mA				−1.5			−1.5			−1.5			N/A			N/A				V
		$I_I = -18$ mA													N/A			−1.5			−1.5	
I_{OH} High Level Output Current	V_{CC} = Min, V_I = (2)	V_{OH} = 12V							50						200			50				μA
		V_{OH} = Max				250			1000			250						1000			250	
V_{OH} High Level Output Voltage			06, 07			30																V
			16, 17			15																
			Others						15			5.5			15			15			5.5	
I_{OL} Low Level Output Current			DM54			30			16			48			2			4			12	mA
			DM74			40			16			48			3.6			8			24	
V_{OL} Low Level Output Voltage	V_{CC} = Min, V_I = (2)	I_{OL} = Max	DM54			0.7			0.4			0.4		0.15	0.3		0.25	0.4			0.4	V
		I_{OL} = Max	DM74			0.7			0.4			0.4			0.4		0.35	0.5			0.5	
		I_{OL} = 4 mA	DM74														0.25	0.4				
		I_{OL} = 12 mA	DM74																		0.4	
		I_{OL} = 16 mA				0.4																
I_I Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			1			1			0.1							mA
		V_I = 7V																0.1			0.1	
I_{IH} High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			40			40			10							μA
		V_I = 2.7V																20			20	
I_{IL} Low Level Input Current	V_{CC} = Max	V_I = 0.3V													−0.18							mA
		V_I = 0.4V				−1.6			−1.6			−1.6						−0.36			−0.36	
I_{CC} Supply Current	V_{CC} = Max			See Table																		

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) The input voltage is V_{IH} = 2V or V_{IL} = max, as appropriate.

LS38 To Be Announced In 1976

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
06, 16	30	42	27	38
07, 17	29	41	21	30
26	4	8	12	22
38	5	8.5	34	54
L26	0.48	0.8	1.32	2.04
LS26	0.8	1.6	2.4	4.4
LS38	0.9	2	6	12

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
06, 16	C_L = 15 pF		10	15		15	23
07, 17	R_L = 110Ω		6	10		20	30
26	C_L = 15 pF, R_L = 1 kΩ		16	24		11	17
38	C_L = 45 pF, R_L = 133Ω		14	22		11	18
L26	C_L = 15 pF, R_L = 4 kΩ		40	90		25	60
LS26	C_L = 15 pF, R_L = 2 kΩ		17	32		15	28
LS38	C_L = 45 pF, R_L = 667Ω		20	32		18	28

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS			DM54/74 08, 11 MIN	TYP(1)	MAX	DM54H/74H H08, H11, H21 MIN	TYP(1)	MAX	DM54L/74L L08, L11 MIN	TYP(1)	MAX	DM54LS/74LS LS08, LS11, LS21 MIN	TYP(1)	MAX	DM74S S11 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7			0.7			N/A	V
				DM74			0.8			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −8 mA							−1.5			N/A							V
			I_I = −12 mA				−1.5						N/A							
			I_I = −18 mA										N/A			−1.5			−1.2	
I_{OH}	High Level Output Current						−800			−500			−200			−400			−1000	µA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OH} = Max		DM54	2.4	3.4		2.4	3.4		2.4	3.3		2.5	3.4		N/A			V
				DM74	2.4	3.4		2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			20			2			4			N/A	mA
				DM74			16			20			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			N/A	V
				DM74		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74												0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			1			0.1						1	mA
			V_I = 7V													0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			50			10							µA
			V_I = 2.7V													20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V										−0.18							mA
			V_I = 0.4V				−1.6			−2						−0.36				
			V_I = 0.5V																−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−55	−40		−100	−3		−15	−30		−130			N/A	mA
				DM74	−18		−55	−40		−100	−3		−15	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			See Table															

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54H/DM74H, DM54LS/DM74LS and DM74S, duration of short circuit should not exceed one second.

LS11, LS21 To Be Announced In 1976

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
08	11	21	20	33
11	8	15	14	22
H08	28	40	42	64
H11	18	30	30	48
H21	12	20	20	32
L08	1.1	2.1	2.0	3.3
L11	1.0	1.5	1.6	2.2
LS08	2.4	4.8	4.4	8.8
LS11	1.8	3.6	3.3	6.6
LS21	1.2	2.4	2.2	4.4
S11	13.5	24	24	42

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
08, 11	C_L = 15 pF, R_L = 400Ω		17.5	27		12	19
H08, H11, H21	C_L = 25 pF, R_L = 280Ω		7.6	12		8.8	12
L08	C_L = 50 pF, R_L = 4 kΩ		45	90		45	90
L11			40	80		45	90
LS08, LS11, LS21	C_L = 15 pF, R_L = 2 kΩ		10	15		12	20
S11	C_L = 15 pF, R_L = 280Ω	2.5	4.5	7	2.5	5	7.5
	C_L = 50 pF, R_L = 280Ω		6	9		7.5	11

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS			DM54/74 09 MIN	DM54/74 09 TYP(1)	DM54/74 09 MAX	DM54L/DM74L L09 MIN	DM54L/DM74L L09 TYP(1)	DM54L/DM74L L09 MAX	DM54LS/DM74LS LS09, LS15 MIN	DM54LS/DM74LS LS09, LS15 TYP(1)	DM54LS/DM74LS LS09, LS15 MAX	DM74S S15 MIN	DM74S S15 TYP(1)	DM74S S15 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			0.7			N/A	V
				DM74			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5			N/A							V
			I_I = −18 mA							N/A			−1.5			−1.2	
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V, V_{OH} = 5.5V					250			50			100			250	μA
V_{OH}	High Level Output Voltage						5.5			5.5			5.5			5.5	V
I_{OL}	Low Level Output Current			DM54			16			2			4			N/A	mA
				DM74			16			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.15	0.3		0.25	0.4			N/A	V
				DM74		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74									0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			0.1						1	mA
			V_I = 7V										0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			10							μA
			V_I = 2.7V										20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V							−0.18							mA
			V_I = 0.4V				−1.6						−0.36				
			V_I = 0.5V													−2	
I_{CC}	Supply Current	V_{CC} = Max			See Table												

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

LS15 To Be Announced In 1976

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
09	11	21	20	33
L09	1.1	2.1	2	3.3
LS09	2.4	4.8	4.4	8.8
LS15	1.8	3.6	3.3	6.6
S15	10.5	19.5	24	42

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
09	C_L = 15 pF, R_L = 400Ω		21	32		16	24
L09	C_L = 15 pF, R_L = 4 kΩ		50	110		50	110
LS09, LS15	C_L = 15 pF, R_L = 2 kΩ		20	35		20	35
S15	C_L = 15 pF, R_L = 280Ω	2.5	5.5	8.5	2.5	6	9
	C_L = 50 pF, R_L = 280Ω		8.5	13		8	12

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS	DM54/74 13 MIN	DM54/74 13 TYP(1)	DM54/74 13 MAX	DM54/74 14 MIN	DM54/74 14 TYP(1)	DM54/74 14 MAX	DM54/74 132 MIN	DM54/74 132 TYP(1)	DM54/74 132 MAX	DM54LS/74LS LS13, LS14, LS132 MIN	DM54LS/74LS LS13, LS14, LS132 TYP(1)	DM54LS/74LS LS13, LS14, LS132 MAX	UNITS
V_{T+}	Positive-Going Threshold Voltage	V_{CC} = 5V	1.5	1.7	2	1.5	1.7	2	1.5	1.7	2	1.4	1.6	1.9	V
V_{T-}	Negative-Going Threshold Voltage	V_{CC} = 5V	0.6	0.9	1.1	0.6	0.9	1.1	0.6	0.9	1.1	0.5	0.8	1.0	V
V_{T+} − V_{T-}	Hysteresis	V_{CC} = 5V	0.4	0.8		0.4	0.8		0.4	0.8		0.4	0.8		V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5			−1.5			−1.5				V
		V_{CC} = Min, I_I = −18 mA												−1.5	V
I_{OH}	High Level Output Current				−800			−800			−800			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_I = V_{T-} Min, I_{OH} = Max, DM54	2.4	3.4		2.4	3.4		2.4	3.4		2.5	3.4		V
		V_{CC} = Min, V_I = V_{T-} Min, I_{OH} = Max, DM74	2.4	3.4		2.4	3.4		2.4	3.4		2.7	3.4		V
I_{OL}	Low Level Output Current	DM54			16			16			16			4	mA
		DM74			16			16			16			8	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_I = V_{T+}Max, I_{OL} = 4 mA											0.25	0.4	V
		V_{CC} = Min, V_I = V_{T+}Max, I_{OL} = 8 mA, DM74											0.35	0.5	V
		V_{CC} = Min, V_I = V_{T+}Max, I_{OL} = 16 mA		0.2	0.4		0.2	0.4		0.2	0.4				V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}		−0.65			−0.43			−0.43			−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}		−0.85			−0.56			−0.56			−0.18		mA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1			1				mA
		V_{CC} = Max, V_I = 7.0V												0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40			40			40				μA
		V_{CC} = Max, V_I = 2.7V												20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V		−1.0	−1.6		−0.8	−1.2		−0.8	−1.2			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)	−18		−55	−18		−55	−18		−55	−30		−130	mA
I_{CC}	Supply Current, Total Output High	V_{CC} = Max, V_I = 0V, LS13											2.9	6	mA
		V_{CC} = Max, V_I = 0V, LS14											8.6	16	mA
		V_{CC} = Max, V_I = 0V, LS132											5.9	11	mA
		V_{CC} = Max, V_I = 0V, Others		14	23		22	36		15	24				mA
	Supply Current, Total Output Low	V_{CC} = Max, V_I = 4.5V, LS13											4.1	7	mA
		V_{CC} = Max, V_I = 4.5V, LS14											12	21	mA
		V_{CC} = Max, V_I = 4.5V, LS132											8.2	14	mA
		V_{CC} = Max, V_I = 4.5V, Others		20	32		39	60		26	40				mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/DM74LS, duration of short circuit should not exceed one second.

LS13, LS14, LS132 To Be Announced In 1976

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output		t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output	
		TYP	MAX	TYP	MAX
13	C_L = 15 pF, R_L = 400Ω	18	27	15	22
14, 132		15	22	15	22
LS13	C_L = 15 pF, R_L = 2 kΩ	15	22	18	27
LS14, LS132		15	22	15	22

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER		CONDITIONS		DM54/74 23 MIN	DM54/74 23 TYP(1)	DM54/74 23 MAX	DM54/74 50, 53 MIN	DM54/74 50, 53 TYP(1)	DM54/74 50, 53 MAX	DM54H/74H H50, H52 H53, H55 MIN	DM54H/74H H50, H52 H53, H55 TYP(1)	DM54H/74H H50, H52 H53, H55 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min	$I_I = -8$ mA									−1.5	V
				$I_I = -12$ mA			−1.5			−1.5				
I_{OH}	High Level Output Current						−800			−400			−500	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_I = (2), I_{OH} = Max		2.4	3.4		2.4	3.4		2.4	3.4		V
I_{OL}	Low Level Output Current						16			16			20	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_I = (2), I_{OL} = Max			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V				1			1			1	mA
I_{IH}	High Level Input Current	Data Inputs	V_{CC} = Max, V_I = 2.4V				40			40			50	μA
		Strobe of 23					160			N/A			N/A	
I_{IL}	Low Level Input Current	Data Inputs	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6			−2	mA
		Strobe of 23					−6.4			N/A			N/A	
I_{OS}	Short Circuit Output Current		V_{CC} = Max (3)	DM54	−20		−55	−20		−55	−40		−100	mA
				DM74	−18		−55	−18		−55	−40		−100	
I_{CC}	Supply Current		V_{CC} = Max		See Table									

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) The input voltage is V_{IH} = 2V or V_{IL} = V_{IL} max, as appropriate.

(3) Not more than one output should be shorted at a time, and for the DM54H/DM74H, duration of short circuit should not exceed one second.

Electrical Characteristics using expander inputs, V_{CC} = Min, T_A = Min (unless otherwise noted) (4), (5), (6)

DEVICE	$I_{\bar{X}}$ (mA) (I_X for H52) Expander Current				$V_{BE(Q)}$ (V) Base-Emitter Voltage of Output Transistor Q				V_{OH} (V) High Level Output Voltage				V_{OL} (V) Low Level Output Voltage			
	CONDITIONS	MIN	TYP(1)	MAX	CONDITIONS	MIN	TYP(1)	MAX	CONDITIONS	MIN	TYP(1)	MAX	CONDITIONS	MIN	TYP(1)	MAX
DM5423 DM5450 DM5453	$V_{\bar{X}X}$ = 0.4V I_{OL} = 16 mA			−3.5 −2.9 −2.9	$I_X + I_{\bar{X}}$ = 410μA $R_{\bar{X}X}$ = 0 I_{OL} = 16 mA			1.1	I_X = 150μA $I_{\bar{X}}$ = −150μA I_{OH} = −400μA	2.4	3.4		$I_X + I_{\bar{X}}$ = 300μA $R_{\bar{X}X}$ = 138Ω I_{OL} = 16 mA		0.2	0.4
DM7423 DM7450 DM7453	$V_{\bar{X}X}$ = 0.4V I_{OL} = 16 mA			−3.5 −3.1 −3.1	$I_X + I_{\bar{X}}$ = 620μA $R_{\bar{X}X}$ = 0 I_{OL} = 16 mA			1.0	I_X = 270μA $I_{\bar{X}}$ = −270μA I_{OH} = −400μA	2.4	3.4		$I_X + I_{\bar{X}}$ = 430μA $R_{\bar{X}X}$ = 130Ω I_{OL} = 16 mA		0.2	0.4
DM54H50 DM54H53 DM54H55	$V_{\bar{X}}$ = 1.4V I_X = 0 I_{OL} = 0			−5.85	$I_X + I_{\bar{X}}$ = 700μA $R_{\bar{X}X}$ = 0 I_{OL} = 20 mA			1.1	I_X = 320μA $I_{\bar{X}}$ = −320μA I_{OH} = −500μA	2.4	3.4		$I_X + I_{\bar{X}}$ = 470μA $R_{\bar{X}X}$ = 68Ω I_{OL} = 20 mA		0.2	0.4
DM74H50 DM74H53 DM74H55	$V_{\bar{X}}$ = 1.4V I_X = 0 I_{OL} = 0			−6.3	$I_X + I_{\bar{X}}$ = 1.1 mA $R_{\bar{X}X}$ = 0 I_{OL} = 20 mA			1.0	I_X = 570μA I_X = −570μA I_{OH} = −500μA	2.4	3.4		$I_X + I_{\bar{X}}$ = 600μA $R_{\bar{X}X}$ = 63Ω I_{OL} = 20 mA		0.2	0.4
DM54H52 DM74H52	V_X = 1V I_{OH} = −500μA	−2.7		−4.5					V_X = 1V I_{OH} = −500μA	2.4	3.4		I_X = −300μA I_{OL} = 20 mA T_A = Max		0.2	0.4

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(4) The 23, 50, and 53 are designed for use with up to four 60 expanders.

(5) The H50, H53, and H55 are designed for use with up to four H60 expanders or one H62 expander.

(6) The H52 is designed for use with up to six H61 expanders.

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
23	8	16	10	19
50	4	8	7.4	14
53	4	8	5.1	9.5
H50	8.2	12.8	15.2	24
H52	20	31	15.2	24
H53	7.1	11	9.4	14
H55	4.5	6.4	7.5	12

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output		t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output	
		TYP	MAX	TYP	MAX
23, 50, 53	C_L = 15 pF, R_L = 400Ω Expander Pins Open	13	22	8	15
50	C_L = 15 pF, R_L = 400Ω From Input of 60 Expander	15	30	10	20
H50	C_L = 25 pF, R_L = 280Ω Expander Pins Open	6.8	11	6.2	11
H52		10.6	15	9.2	15
H53		7	11	6.2	11
H55		7	11	6.5	11
H50	C_L = 25 pF, R_L = 280Ω C = 15 pF, (GND to $\bar{X}$ of H50, H53, or H55; or to X of H52)	11		7.4	
H52		14.8		9.8	
H53		11.4		7.4	
H55		11.4		7.7	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS			DM54/74 32 MIN	DM54/74 32 TYP(1)	DM54/74 32 MAX	DM54L/74L L32 MIN	DM54L/74L L32 TYP(1)	DM54L/74L L32 MAX	DM54LS/74LS LS32 MIN	DM54LS/74LS LS32 TYP(1)	DM54LS/74LS LS32 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			0.7	V
				DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	$I_I = -12$ mA				−1.5			N/A				V
			$I_I = -18$ mA							N/A			−1.5	
I_{OH}	High Level Output Current						−800			−200			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OH} = Max		DM54	2.4	3.4		2.4	2.8		2.5	3.4		V
				DM74	2.4	3.4		2.4	2.8		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			2			4	mA
				DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.15	0.3		0.25	0.4	V
				DM74		0.2	0.4			0.4		0.35	0.5	
			I_{OL} = 4 mA	DM74									0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			0.1				mA
			V_I = 7V										0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			10				μA
			V_I = 2.7V										20	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V						−0.12	−0.18				mA
			V_I = 0.4V				−1.6						−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−20		−55	−3	−9	−15	−30		−130	mA
				DM74	−18		−55	−3	−9	−15	−30		−130	
I_{CC}	Supply Current: Total, Outputs High	V_{CC} = Max				15	22		1.5	2.2		3.1	6.2	mA
	Supply Current: Total, Outputs Low					23	38		2.3	3.8		4.9	9.8	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/DM74LS, duration of short circuit should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
32	$C_L = 15$ pF, $R_L = 400\Omega$		10	15		14	22
L32	$C_L = 50$ pF, $R_L = 4$ kΩ		40	80		50	100
LS32	$C_L = 15$ pF, $R_L = 2$ kΩ		14	22		14	22

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS			DM54/74 37, 40 MIN	TYP(1)	MAX	DM54H/74H H40 MIN	TYP(1)	MAX	DM54LS/74LS LS37, LS40 MIN	TYP(1)	MAX	DM74S S40, S140 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7			N/A	V
				DM74			0.8			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −8 mA							−1.5							V
			I_I = −12 mA				−1.5										
			I_I = −18 mA										−1.5			−1.2	
I_{OH}	High Level Output Current			Others			−1.2			−1.5			−1.2			−3	mA
				S140												−40	
V_{OH}	High Level Output Voltage	V_{CC} = Min	V_{IL} = Max	I_{OH} = Max	2.4	3.3		2.4	3.4		2.7	3.4					V
				I_{OH} = −3 mA										2.7	3.4		
			V_{IL} = 0.5V, R_O = 50Ω to GND, S140 Only											2			
I_{OL}	Low Level Output Current			DM54			48			60			12			N/A	mA
				DM74			48			60			24			60	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.25	0.4			N/A	V
				DM74		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 12 mA	DM74									0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			1						1	mA
			V_I = 7V										0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			100							μA
			V_I = 2.7V										20			100	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−1.6			−4			−0.36				mA
			V_I = 0.5V													−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−20		−70	−40		−125	−30		−130			N/A	mA
				DM74	−18		−70	−40		−125	−30		−130	−50		−225	
I_{CC}	Supply Current	V_{CC} = Max			See Table												

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second for 37, LS37, 40, H40 or LS40; or 100 milliseconds for S40 and S140.

LS37, LS40 To Be Announced In 1976

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
37	9	15.5	34	54
40	4	8	17	27
H40	10.4	16	25	40
LS37	0.9	2	6	12
LS40	0.45	1	3	6
S40	10	18	25	44
S140	10	18	25	44

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
37	C_L = 45 pF, R_L = 133Ω		13	22		8	15
40	C_L = 15 pF, R_L = 133Ω		13	22		8	15
H40	C_L = 25 pF, R_L = 93Ω		8.5	12		6.5	12
LS37 LS40	C_L = 45 pF, R_L = 667Ω		12	24		12	24
S40	C_L = 50 pF, R_L = 93Ω	2	4	6.5	2	4	6.5
S140	C_L = 150 pF, R_L = 93Ω		6	9		6	9

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS(1)			DM54/74 51, 54 MIN	TYP(1)	MAX	DM54H/74H H51, H54 MIN	TYP(1)	MAX	DM54L/74L L51, L54 L55 MIN	TYP(1)	MAX	DM54LS/74LS LS51, LS54 LS55 MIN	TYP(1)	MAX	DM74S S51, S64 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7			0.7			N/A	V
				DM74			0.8			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −8 mA							−1.5			N/A							V
			I_I = −12 mA				−1.5						N/A							
			I_I = −18 mA										N/A			−1.5			−1.2	
I_{OH}	High Level Output Current						−400			−500			−200			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min V_{IL} = Max I_{OH} = Max	LS54											2.4						V
			Others	DM54	2.4	3.4		2.4	3.4		2.4	3.3		2.5	3.4		N/A			
				DM74	2.4	3.4		2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			20			2			4			N/A	mA
				DM74			16			20			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IH} = 2V	I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			N/A	V
				DM74		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74												0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			1			0.1						1	mA
			V_I = 7V													0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			50			10							μA
			V_I = 2.7V													20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V										−0.18							mA
			V_I = 0.4V				−1.6			−2						−0.36				
			V_I = 0.5V																−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−20		−55	−40		−100	−3		−15	−30		−130			N/A	mA
				DM74	−18		−55	−40		−100	−3		−15	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			See Table															

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54H/DM74H, DM54LS/DM74LS and DM74S, duration of the short circuit should not exceed one second.

(3) National Semiconductor temporarily reserves the right to ship DM54/DM74LS51, LS54, LS55 devices which have a minimum I_{OS} = 5.0 mA.

74S51 To Be Announced In 1976

Supply Currents

DEVICE	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	TYP	MAX	TYP	MAX
51	4	8	7.4	14
54	4	8	5.1	9.5
H51	8.2	12.8	15.2	24
H54	7.1	11	9.4	14
L51	0.44	0.8	0.76	1.3
L54	0.39	0.8	0.60	0.99
L55	0.22	0.4	0.38	0.65
LS51	0.8	1.6	1.4	2.8
LS54	0.8	1.6	1.0	2
LS55	0.4	0.8	0.7	1.3
S51	8.2	17.8	13.6	22
S64	7	12.5	8.5	16

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		MIN	TYP	MAX	MIN	TYP	MAX
51, 54	C_L = 15 pF, R_L = 400Ω		13	22		8	15
H51	C_L = 25 pF, R_L = 280Ω		6.8	11		6.2	11
H54	C_L = 25 pF, R_L = 280Ω		7	11		6.2	11
L51, L54 L55	C_L = 50 pF, R_L = 4 kΩ		50	90		35	60
LS51, LS55	C_L = 15 pF, R_L = 2 kΩ		12	20		12.5	20
LS54	C_L = 15 pF, R_L = 2 kΩ		16	20		12.5	20
S51, S64	C_L = 15 pF, R_L = 280Ω	2	3.5	5.5	2	3.5	5.5
	C_L = 50 pF, R_L = 280Ω		5	8		5.5	8

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		DM54 60 CONDITIONS	MIN	TYP(1)	MAX	DM74 60 CONDITIONS	MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage		2				2			V
V_{IL}	Low Level Input Voltage				0.8				0.8	V
$V_{\overline{X}X(ON)}$	On-State Voltage Between Expander Outputs	V_{CC} = 4.5V, V_{IH} = 2V V_X = 1.1V, $I_{\overline{X}}$ = 3.5 mA T_A = −55°C			0.4	V_{CC} = 4.75V, V_{IH} = 2V V_X = 1V, $I_{\overline{X}}$ = 3.5 mA T_A = 0°C			0.4	V
$I_{X(ON)}$	On-State Expander Current	V_{CC} = 4.5V, V_{IH} = 2V V_X = 1.1V, $I_{\overline{X}}$ = 0 T_A = −55°C	−0.3			V_{CC} = 4.75V, V_{IH} = 2V V_X = 1V, $I_{\overline{X}}$ = 0 T_A = 0°C	−0.43			mA
$I_{\overline{X}(OFF)}$	Off-State Expander Current	V_{CC} = 4.5V, V_{IL} = 0.8V $V_{\overline{X}}$ = 4.5V, R_X = 1.2 kΩ T_A = −55°C			150	V_{CC} = 4.75V, V_{IL} = 0.8V $V_{\overline{X}}$ = 4.5V, R_X = 1.2 kΩ T_A = 0°C			270	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 5.5V			1	V_{CC} = 5.25V, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.4V			40	V_{CC} = 5.25V, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−1.6	V_{CC} = 5.25V, V_I = 0.4V			−1.6	mA
$I_{CC(ON)}$	Supply Current, Expander On	V_{CC} = 5.5V, V_I = 4.5V V_X = 0.85V, $I_{\overline{X}}$ = 0		1.2	2.5	V_{CC} = 5.25V, V_I = 4.5V V_X = 0.85V, $I_{\overline{X}}$ = 0		1.2	2.5	mA
$I_{CC(OFF)}$	Supply Current, Expander Off	V_{CC} = 5.5V, V_I = 0 V_X = 0.85V, $I_{\overline{X}}$ = 0		2	4	V_{CC} = 5.25V, V_I = 0 V_X = 0.85V, $I_{\overline{X}}$ = 0		2	4	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			DM54H H60, H62 CONDITIONS	MIN	TYP(1)	MAX	DM74H H60, H62 CONDITIONS	MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2				2			V
V_{IL}	Low Level Input Voltage					0.8				0.8	V
$V_{\bar{X}X(ON)}$	On-State Voltage Between Expander Outputs		V_{CC} = 4.5V, V_{IH} = 2V V_X = 1V, $I_{\bar{X}}$ = 5.85 mA T_A = −55°C			0.4	V_{CC} = 4.75V, V_{IH} = 2V V_X = 1V, $I_{\bar{X}}$ = 6.3 mA T_A = 0°C			0.4	V
			V_{CC} = 5.5V, V_{IH} = 2V V_X = 1V, $I_{\bar{X}}$ = 7.85 mA T_A = 125°C			0.4	V_{CC} = 5.25V, V_{IH} = 2V V_X = 1V, $I_{\bar{X}}$ = 7.4 mA T_A = 70°C			0.4	
$I_{X(ON)}$	On-State Expander Current		V_{CC} = 4.5V, V_{IH} = 2V V_X = 1V, $I_{\bar{X}}$ = 0 T_A = −55°C	−470			V_{CC} = 4.75V, V_{IH} = 2V V_X = 1V, $I_{\bar{X}}$ = 0 T_A = 0°C	−600			μA
$I_{\bar{X}(OFF)}$	Off-State Expander Current		V_{CC} = 4.5V, V_{IL} = 0.8V $V_{\bar{X}}$ = 4.5V, R_X = 575Ω T_A = −55°C			320	V_{CC} = 4.75V, V_{IL} = 0.8V $V_{\bar{X}}$ = 4.5V, R_X = 575Ω T_A = 0°C			570	μA
I_I	Input Current at Maximum Input Voltage		V_{CC} = 5.5V, V_I = 5.5V			1	V_{CC} = 5.25V, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current		V_{CC} = 5.5V, V_I = 2.4V			50	V_{CC} = 5.25V, V_I = 2.4V			50	μA
I_{IL}	Low Level Input Current		V_{CC} = 5.5V, V_I = 0.4V			−2	V_{CC} = 5.25V, V_I = 0.4V			−2	mA
$I_{CC(ON)}$	Supply Current, Expander On	H60	V_{CC} = 5.5V, V_I = 4.5V		1.9	3.5	V_{CC} = 5.25V, V_I = 4.5V		1.9	3.5	mA
		H62	V_X = 0.85V, $I_{\bar{X}}$ = 0		3.8	7	V_X = 0.85V, $I_{\bar{X}}$ = 0		3.8	7	
$I_{CC(OFF)}$	Supply Current, Expander Off	H60	V_{CC} = 5.5V, V_I = 0		3	4.5	V_{CC} = 5.25V, V_I = 0		3	4.5	mA
		H62	V_X = 0.85V, $I_{\bar{X}}$ = 0		6	9	V_X = 0.85, $I_{\bar{X}}$ = 0		6	9	
$C_{\bar{X}}$	Expander Output Capacitance	H60	V_{CC}, Inputs, and X		5.4		V_{CC}, Inputs, and X		5.4		pF
		H62	Open; f = 1 MHz		6.0		Open; f = 1 MHz		6.0		

Notes

(1) All typical values are at V_{CC} = 5V (except $C_{\bar{X}}$), T_A = 25°C.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		DM54H/74H H61 CONDITIONS	MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
$V_{X(ON)}$	On-State Expander Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_X = 4.5 mA for DM54H61 5.35 mA for DM74H61, T_A = Min			1	V
$I_{X(OFF)}$	Off-State Expander Current	V_{CC} = Min, V_{IL} = 0.8V, V_X = 2.2V, T_A = Max			50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.4V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−2	mA
$I_{CC(ON)}$	Supply Current, Expander On	V_{CC} = 5.5V, V_I = 4.5V		11	16	mA
$I_{CC(OFF)}$	Supply Current, Expander Off	V_{CC} = 5.5V, V_I = 0		5	7	mA
C_X	Expander Output Capacitance	V_{CC} and Inputs Open, f = 1 MHz		5.4		pF

Notes

(1) All typical values are at V_{CC} = 5V (except C_X), T_A = 25°C.

(2) The H52 is designed for use with up to six H61 expanders.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		CONDITIONS	DM74S S65 MIN	DM74S S65 TYP(1)	DM74S S65 MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IL} = 0.8V V_{OH} = 5.5V			250	μA
V_{OH}	High Level Output Voltage				5.5	V
I_{OL}	Low Level Output Current				20	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 20 mA			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current, Output High	V_{CC} = Max		6	11	mA
I_{CCL}	Supply Current, Output Low	V_{CC} = Max		8.5	16	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM74S S65 MIN	DM74S S65 TYP	DM74S S65 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF, R_L = 280Ω	2	5	7.5	ns
		C_L = 50 pF, R_L = 280Ω		8	12	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF, R_L = 280Ω	2	5.5	8.5	ns
		C_L = 50 pF, R_L = 280Ω		6.5	10	ns

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER		CONDITIONS		DM54/74												UNITS
					70			72, 73, 76, 107			74			109			
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage				2			2			2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8			0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5			−1.5			−1.5			−1.5	V
I_{OH}	High Level Output Current						−400			−400			−400			−1200	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4	3.4		2.4	3.4		2.4	3.4		2.4			V
I_{OL}	Low Level Output Current						16			16			16			16	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V				1			1			1			1	mA
I_{IH}	High Level Input Current	D, J, K, or $\overline{K}$	V_{CC} = Max, V_I = 2.4V				40			40			40			40	μA
		Clear					80			80			120			160	
		Preset					80			80			40			80	
		Clock					40			80			80			80	
I_{IL}	Low Level Input Current	D, J, K, or $\overline{K}$	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6			−1.6			−1.6	mA
		Clear					−3.2			−3.2			−3.2			−4.8	
		Preset					−3.2			−3.2			−1.6			−3.2	
		Clock					−1.6			−3.2			−3.2			−3.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	DM54	−20		−57	−20		−55	−20		−55	−30	−55	−85	mA
				DM74	−18		−57	−18		−55	−18		−55	−30	−55	−85	
I_{CC}	Supply Current (Average per Flip-Flop)		V_{CC} = Max(3)			13	26		9	17		8.5	15		10	15	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5V for the 70, and is grounded for all the others.

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74 70 MIN	70 TYP	70 MAX	72, 73, 76, 107 MIN	72, 73, 76, 107 TYP	72, 73, 76, 107 MAX	74 MIN	74 TYP	74 MAX	109 MIN	109 TYP	109 MAX	UNITS
f_{MAX}	Maximum Clock Frequency				$C_L = 15$ pF, $R_L = 400\Omega$	20	35		15	20		20	25		30	40		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Preset (as applicable)	Q				50		16	25			25		9	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Preset (as applicable)	$\overline{Q}$				50		25	40			40		18	29	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clear (as applicable)	$\overline{Q}$				50		16	25			25		9	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear (as applicable)	Q				50		25	40			40		17	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Q or $\overline{Q}$			27	50		16	25		14	25		12	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Q or $\overline{Q}$			18	50		25	40		20	40		19	28	ns
t_W	Pulse Width	Clock High				20			20			30			20			ns
		Clock Low				30			47			37			20			ns
		Preset or Clear Low				25			25			30			20			ns
t_{SETUP}	Input Setup Time(4)					20↑			0↑			20↑			15↑			ns
t_{HOLD}	Input Hold Time(4)					5↑			0↓			5↑			10↑			ns

Notes

(4) ↑ ↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER		CONDITIONS	DM54H/74H												UNITS
				H71			H72, H73, H76			H74			H78			
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage			2			2			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8			0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −8 mA			−1.5			−1.5			−1.5			−1.5	V
I_{OH}	High Level Output Current					−500			−500			−1000			−500	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
I_{OL}	Low Level Output Current					20			20			20			20	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 20 mA		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V			1			1			1			1	mA
I_{IH}	High Level Input Current	D, J, or K	V_{CC} = Max, V_I = 2.4V			50			50			50			50	μA
		Clear				N/A			100			150			200	
		Preset				150			100			100			100	
		Clock				100			50			100			100	
I_{IL}	Low Level Input Current	D, J, or K	V_{CC} = Max, V_I = 0.4V			−2			−2			−2			−2	mA
		Clear				N/A			−4			−4			−8	
		Preset				−6			−4			−2			−4	
		Clock				−4			−2			−4			−4	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply Current (Average per Flip-Flop)		V_{CC} = Max(3), DM54		19	30		16	25		15	21		16	25	mA
			V_{CC} = Max(3), DM74		19	30		16	25		15	25		16	25	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

(3) With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER			FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54H/74H H71, H72 H73, H76, H78 MIN	TYP	MAX	H74 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				$C_L = 25$ pF, $R_L = 280\Omega$	25	30		35	43		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Preset (as applicable)	Q			6	13			20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Preset (as applicable)	$\overline{Q}$			12	24			30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clear (as applicable)	$\overline{Q}$			6	13			20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear (as applicable)	Q			12	24			30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Q or $\overline{Q}$			14	21		8.5	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Q or $\overline{Q}$			22	27		13	20	ns
t_w	Pulse Width	Clock High				12			15			ns
		Clock Low				28			13.5			ns
		Clear or Preset Low				16			25			ns
t_{SETUP}	Setup Time(4)	High Level Data				0↑			10↑			ns
		Low Level Data				0↑			15↑			ns
t_{HOLD}	Hold Time(4)					0↓			5↑			ns

Notes

(4) ↓ ↑ The arrow indicates the edge of the clock pulse used for reference; ↑ for the rising edge, ↓ for the falling edge.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER		CONDITIONS		DM54L/74L L71, L72 MIN	L71, L72 TYP(1)	L71, L72 MAX	L73 MIN	L73 TYP(1)	L73 MAX	L74 MIN	L74 TYP(1)	L74 MAX	L78 MIN	L78 TYP(1)	L78 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			2			V
V_{IL}	Low Level Input Voltage	Clock Input					0.6			0.6			0.7			0.6	V
		All Other Inputs					0.7			0.7			0.7			0.7	
I_{OH}	High Level Output Current						−200			−200			−200			−200	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V	DM54L	2.4	3.3		2.4	3.3		2.4	3.3		2.4	3.3		V
			V_{IL} = Max, I_{OH} = Max	DM74L	2.4	3.2		2.4	3.2		2.4	3.2		2.4	3.2		
I_{OL}	Low Level Output Current			DM54			2			2			2			2	mA
				DM74			3.6			3.6			3.6			3.6	
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V	DM54L		0.15	0.3		0.15	0.3		0.15	0.3		0.15	0.3	V
			V_{IL} = Max, I_{OL} = Max	DM74L		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	
I_I	Input Current at Maximum Input Voltage	R, S, J, K, or D	V_{CC} = Max, V_I = 5.5V				100			100			100			100	μA
		Clear					200			200			300			400	
		Preset					200			200			200			200	
		Clock					200			200			200			400	
I_{IH}	High Level Input Current	R, S, J, K, or D	V_{CC} = Max, V_I = 2.4V				10			10			10			10	μA
		Clear					20			20			30			40	
		Preset					20			20			20			20	
		Clock					−200			−200			20			−400	
I_{IL}	Low Level Input Current	R, S, J, K, or D	V_{CC} = Max, V_I = 0.3V				−0.18			−0.18			−0.18			−0.18	mA
		Clear					−0.36			−0.36			−0.36			−0.72	
		Preset					−0.36			−0.36			−0.18			−0.36	
		Clock					−0.36			−0.36			−0.36			−0.72	
I_{OS}	Short Circuit Output Current		V_{CC} = Max		−3	−9	−15	−3	−9	−15	−3	−9	−15	−3	−9	−15	mA
I_{CC}	Supply Current		V_{CC} = Max(2)			0.76	1.44		1.52	2.88		1.6	3.0		1.52	2.88	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54L/74L L71, L72, L73, L78 MIN	TYP	MAX	L74 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency			$C_L = 50$ pF, $R_L = 4$ kΩ	6	11		6	11		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Preset or Clear	Q or $\overline{Q}$			35	75		40	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Preset or Clear (Clock High)	$\overline{Q}$ or Q			60	150		60	120	ns
		Preset or Clear (Clock Low)					150		60	120	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Q or $\overline{Q}$		10	35	75	10	50	90	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				10	60	150	10	60	120	
t_W	Pulse Width: Clock High				100			75			ns
	Pulse Width: Clock Low				100			75			
	Pulse Width: Clear or Preset Low				100			75			
t_{SETUP}	Setup Time(3)				0↑			50↑			ns
t_{HOLD}	Hold Time(3)				0↓			15↑			ns

Notes

(3) ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge ↓ for the falling edge.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER		CONDITIONS			DM54LS/74LS												UNITS
						LS73, LS76, LS107 LS112, LS113			LS74			LS78, LS114			LS109			
						MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage					2			2			2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.7			0.7			0.7			0.7	V
					DM74			0.8			0.8			0.8			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −18 mA					−1.5			−1.5			−1.5			−1.5	V
I_{OH}	High Level Output Current							−400			−400			−400			−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V		DM54	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
			V_{IL} = Max, I_{OH} = −400μA		DM74	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current				DM54			4			4			4			4	mA
					DM74			8			8			8			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min	I_{OL} = Max	DM54		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4	V
			V_{IH} = 2V		DM74		0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5	
			V_{IL} = Max	I_{OL} = 4 mA	DM74			0.4			0.4			0.4			0.4	
I_I	Input Current at Maximum Input Voltage	D, J, K, or $\overline{K}$	V_{CC} = Max	V_I = 5.5V							0.1						0.1	mA
				V_I = 7V				0.1						0.1				
		Clear		V_I = 5.5V							0.3						0.4	
				V_I = 7V				0.3						0.6				
		Preset		V_I = 5.5V							0.2						0.2	
				V_I = 7V				0.3						0.3				
		Clock		V_I = 5.5V							0.2						0.2	
				V_I = 7V				0.4						0.8				
I_{IH}	High Level Input Current	D,J,K or $\overline{K}$	V_{CC} = Max, V_I = 2.7V					20			20			20			20	μA
		Clear						60			60			120			80	
		Preset						60			40			60			40	
		Clock						80			40			160			40	
I_{IL}	Low Level Input Current	D,J,K or $\overline{K}$	V_{CC} = Max, V_I = 0.4V					−0.36			−0.4			−0.36			−0.4	mA
		Clear						−0.8			−1.2			−1.6			−1.6	
		Preset						−0.8			−0.8			−0.8			−0.8	
		Clock						−0.72			−0.8			−1.44			−0.8	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)			−30		−130	−30		−130	−30		−130	−30		−130	mA
I_{CC}	Supply Current		V_{CC} = Max(3)				4	8		4	8		4	8		4	8	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

(3) With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

(4) National Semiconductor temporarily reserves the right to ship DM54/DM74LS73, LS74, LS76, LS78, LS107, LS109, LS112, LS113, LS114 devices which have a minimum I_{OS} = 5.0 mA.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

PARAMETER			FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54LS/74LS LS73, LS76, LS78, LS107 LS112, LS113, LS114			LS74			LS109			UNITS
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 2 kΩ	30	45		25	33		25	33		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clear, Preset, or Clock (as appropriate)	Q or $\overline{Q}$			11	20		13	25		13	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						15	30		25	40		25	40	ns
t_W	Pulse Width	Clock High				20			25			25			ns
		Preset or Clear Low				25			25			25			
t_{SETUP}	Setup Time(5)	High Level Data				20↓			25↑			20↑			ns
		Low Level Data				20↓			20↑			20↑			
t_{HOLD}	Hold Time(5)					0↓			5↑			5↑			ns

Notes

(5) ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			CONDITIONS	DM74S S74 MIN	S74 TYP(1)	S74 MAX	S112 MIN	S112 TYP(1)	S112 MAX	S113 MIN	S113 TYP(1)	S113 MAX	S114 MIN	S114 TYP(1)	S114 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8			0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −18 mA			−1.2			−1.2			−1.2			−1.2	V
I_{OH}	High Level Output Current					−1			−1			−1			−1	mA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −1 mA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		V
I_{OL}	Low Level Output Current					20			20			20			20	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 20 mA			0.5			0.5			0.5			0.5	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V			1			1			1			1	mA
I_{IH}	High Level Input Current	J, K, or D	V_{CC} = Max, V_I = 2.7V			50			50			50			50	μA
		Clear				150			100			N/A			200	
		Preset				100			100			100			100	
		Clock				100			100			100			200	
I_{IL}	Low Level Input Current	J, K, or D	V_{CC} = Max, V_I = 0.5V			−2			−1.6			−1.6			−1.6	mA
		Clear				−6			−7			N/A			−14	
		Preset				−4			−7			−7			−7	
		Clock				−4			−4			−4			−8	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply Current		V_{CC} = Max(3)		30	50		30	50		30	50		30	50	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM74S S74 MIN	DM74S S74 TYP	DM74S S74 MAX	DM74S S112, S113, S114 MIN	DM74S S112, S113, S114 TYP	DM74S S112, S113, S114 MAX	UNITS
f_{MAX}	Maximum Clock Frequency			C_L = 15 pF, R_L = 280Ω	75	110		80	125		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Preset or Clear	Q or $\overline{Q}$			4	6	2	4	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Preset or Clear (Clock High)	$\overline{Q}$ or Q			9	13.5	2	5	7	ns
		Preset or Clear (Clock Low)				5	8	2	5	7	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Q or $\overline{Q}$			6	9	2	4	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock	Q or $\overline{Q}$			6	9	2	5	7	ns
t_W	Pulse Width — Clock High				6			6			ns
	Pulse Width — Clock Low				7.3			6.5			ns
	Pulse Width — Clear or Preset Low				7			8			ns
t_{SETUP}	Input Setup Time(4) — High Level Data				3↑			3↓			ns
	Input Setup Time(4) — Low Level Data				3↑			3↓			ns
t_{HOLD}	Input Hold Time(4)				2↑			0↓			ns

Notes

(4) ↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS		DM54/74 86 MIN	DM54/74 86 TYP(1)	DM54/74 86 MAX	DM54L/74L L86 MIN	DM54L/74L L86 TYP(1)	DM54L/74L L86 MAX	DM54LS/74LS LS86, LS386 MIN	DM54LS/74LS LS86, LS386 TYP(1)	DM54LS/74LS LS86, LS386 MAX	DM74S S86 MIN	DM74S S86 TYP(1)	DM74S S86 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7			0.7			N/A	V
			DM74			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −8 mA				−1.5		N/A								V
		V_{CC} = Min, I_I = −18 mA						N/A				−1.5			−1.2	
I_{OH}	High Level Output Current					−800			−200			−400			1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	DM54	2.4	3.4		2.4	3.3		2.5	3.4			N/A		V
			DM74	2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current		DM54			16			2			4			N/A	mA
			DM74			16			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM54		0.2	0.4		0.15	0.3		0.25	0.4			N/A	V
			DM74		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
		I_{OL} = 4 mA	DM74									0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			0.2						1	mA
		V_{CC} = Max, V_I = 7V										0.2				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			20							μA
		V_{CC} = Max, V_I = 2.7V										40			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V							−0.36							mA
		V_{CC} = Max, V_I = 0.4V				−1.6						−0.6				
		V_{CC} = Max, V_I = 0.5V													−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM54	−20		−55	−3		−15	−30		−130		N/A		mA
			DM74	−18		−55	−3		−15	−30		−130	−40		−100	
I_{CCH}	Supply Current, All Outputs High	V_{CC} = Max(3)	DM54		30	43		2.2	4.4		6.1	10		N/A		mA
			DM74		30	50		2.2	4.4		6.1	10		50	75	
I_{CCL}	Supply Current, All Outputs Low	V_{CC} = Max(4)			36	57		3.8	6.68							mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/DM74LS and DM74S, duration of short circuit should not exceed one second.

(3) I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

(4) I_{CCL} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

DEVICE	CONDITIONS (FROM INPUT A OR B)		t_{PLH} (ns) Propagation Delay Time, Low-to-High Level Output		t_{PHL} (ns) Propagation Delay Time, High-to-Low Level Output	
			TYP	MAX	TYP	MAX
86	C_L = 15 pF	Other Input Low	15	23	11	17
	R_L = 400Ω	Other Input High	18	30	13	22
L86	C_L = 50 pF	Other Input Low	37	60	21	60
	R_L = 4kΩ	Other Input High	25	60	35	60
LS86	C_L = 15 pF	Other Input Low	12	23	10	17
	R_L = 2kΩ	Other Input High	18	30	13	22
LS386	C_L = 15 pF	Other Input Low	12	23	10	17
	R_L = 2kΩ	Other Input High	18	30	13	22
S86	C_L = 15 pF	Other Input Low	7	10.5	6.5	10
	R_L = 280Ω	Other Input High	7	10.5	6.5	10

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER		CONDITIONS	DM54H/74H									UNITS
				H103			H106			H108			
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −8 mA			−1.5			−1.5			−1.5	V
I_{OH}	High Level Output Current					−500			−500			−500	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −500μA	2.4	3.4		2.4	3.4		2.4	3.4		V
I_{OL}	Low Level Output Current					20			20			20	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 20 mA		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V			1			1			1	mA
I_{IH}	High Level Input Current	Any J or K	V_{CC} = Max, V_I = 2.4V			50			50			50	μA
		Clear				100			100			200	μA
		Preset				N/A			100			100	μA
		Clock		0		−1	0		−1	0		−1	mA
I_{IL}	Low Level Input Current	Any J or K	V_{CC} = Max, V_I = 0.4V		−1	−2		−1	−2		−1	−2	mA
		Clear			−1	−2		−1	−2		−2	−4	mA
		Preset				N/A		−1	−2		−1	−2	mA
		Clock			−3	−4.8		−3	−4.8		−6	−9.6	mA
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply Current		V_{CC} = Max, (3)		40	76		40	76		40	76	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency			C_L = 25 pF, R_L = 280Ω	40	50		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Preset or Clear	Q or $\overline{Q}$			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Preset or Clear, Clock High	$\overline{Q}$ or Q			15	20	ns
		Preset or Clear, Clock Low				23	35	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Q or $\overline{Q}$			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					16	20	
t_W	Pulse Width, Clock High				10			ns
	Pulse Width, Clock Low				15			
	Pulse Width, Clear or Preset Low				16			
t_{SETUP}	Setup Time(4), High Level Data				10↓			ns
	Setup Time(4), Low Level Data				13↓			
t_{HOLD}	Hold Time(4)				0↓			ns

Notes

(4) ↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS			DM54/74 121 MIN	DM54/74 121 TYP(1)	DM54/74 121 MAX	DM54LS/74LS LS221 MIN	DM54LS/74LS LS221 TYP(1)	DM54LS/74LS LS221 MAX	UNITS
V_{T+}	Positive-Going Threshold Voltage at A Input	V_{CC} = Min				1.4	2		1.0	2	V
V_{T-}	Negative-Going Threshold Voltage at A Input	V_{CC} = Min		DM54	0.8	1.4		0.7	1.0		V
				DM74	0.8	1.4		0.8	1.0		
V_{T+}	Positive-Going Threshold Voltage at B Input	V_{CC} = Min				1.55	2		1.0	2	V
V_{T-}	Negative-Going Threshold Voltage at B Input	V_{CC} = Min		DM54	0.8	1.35		0.7	0.9		V
				DM74	0.8	1.35		0.8	0.9		
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5				V
			I_I = −18 mA							−1.5	
I_{OH}	High Level Output Current						−400			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −400μA		DM54	2.4	3.4		2.5	3.5		V
				DM74	2.4	3.4		2.7	3.5		
I_{OL}	Low Level Output Current			DM54			16			4	mA
				DM74			16			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 4 mA						0.25	0.4	V
			I_{OL} = 8 mA	DM74					0.35	0.5	
			I_{OL} = 16 mA			0.2	0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1				mA
			V_I = 7V							0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V	A1 or A2			40				μA
				B			80				
			V_I = 2.7V	All						20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V		A1 or A2			−1.6			−0.36	mA
				B			−3.2			−0.44	
				Clear			N/A			−0.54	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−55	−30		−150	mA
				DM74	−18		−55	−30		−150	
I_{CC}	Supply Current	V_{CC} = Max		Quiescent		13	25		4.7	11	mA
				Triggered		23	40		19	27	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS221/DM74LS221, duration of short circuit should not exceed one second.

LS221 To Be Announced In 1976

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25^\circ C$

Symbol	Parameter	From (Input)	To (Output)	DM54/74 121 Conditions		Min	Typ	Max	DM54LS/74LS LS221 Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A1 or A2	Q	$C_L = 15$ pF, $R_L = 400\Omega$	$C_T = 80$ pF, R_{INT} to V_{CC}		45	70	$C_L = 15$ pF, $R_L = 2$ kΩ	$C_T = 80$ pF, $R_T = 2$ kΩ		45	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	B	Q				35	55				35	55	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clear	$\overline{Q}$					N/A					65	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A1 or A2	$\overline{Q}$				50	80				50	80	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	B	$\overline{Q}$				40	65				40	65	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Q					N/A					55	ns
$t_{W(OUT)}$	Output Pulse Width: Internal Timing Resistor	A1, A2 or B	Q or $\overline{Q}$		$C_T = 80$ pF, R_{INT} to V_{CC}	70	110	150		$C_{EXT} = 80$ pF, $R_{EXT} = 2$ kΩ	70	120	150	ns
	Output Pulse Width: Zero-Timing Capacitance				$C_T = 0$, R_{INT} to V_{CC}		30	50		$C_{EXT} = 0$, $R_{EXT} = 2$ kΩ	20	47	70	ns
	Output Pulse Width: External Timing Resistor				$C_T = 100$ pF, $R_T = 10$ kΩ	600	700	800		$C_T = 100$ pF, $R_T = 10$ kΩ	600	670	750	ns
					$C_T = 1\mu F$, $R_T = 10$ kΩ	6	7	8		$C_T = 1\mu F$, $R_T = 10$ kΩ	6	6.7	7.5	ms
$t_{W(IN)}$	Input Pulse Width					50					40			ns
$t_{W(CLEAR)}$	Clear Pulse Width					N/A					40			ns
dv/dt	Rate of Rise or Fall of Input Pulse: Schmitt Input, B					1					1			V/s
	Rate of Rise or Fall of Input Pulse: Logic Input, A					1					1			V/µs
R_{EXT}	External Timing Resistance				DM54	1.4		30		DM54	1.4		70	kΩ
					DM74	1.4		40		DM74	1.4		100	kΩ
C_{EXT}	External Timing Capacitance					0		1000			0		1000	µF
t_{SETUP}	Clear-Inactive State Setup Time						N/A				15			ns
	Duty Cycle				$R_T = 2$ kΩ			67		$R_T = 2$ kΩ			67	%
					$R_T = $ Max R_{EXT}			90		$R_T = $ Max R_T			90	%

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS	DM54/74 123 MIN	DM54/74 123 TYP(1)	DM54/74 123 MAX	DM54L/74L L123A MIN	DM54L/74L L123A TYP(1)	DM54L/74L L123A MAX	DM54LS/74LS LS122, LS123 MIN	DM54LS/74LS LS122, LS123 TYP(1)	DM54LS/74LS LS122, LS123 MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			2			V
V_{IL}	Low Level Input Voltage	DM54			0.8			0.7			0.7	V
		DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5			−N/A				V
		V_{CC} = Min, I_I = −18 mA									−1.5	
I_{OH}	High Level Output Current				−800			−200			−400	µA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max(3), DM54	2.4	3.4		2.4	3.4		2.5	3.5		V
		V_{CC} = Min, I_{OH} = Max(3), DM74	2.4	3.4		2.4	3.4		2.7	3.5		
I_{OL}	Low Level Output Current	DM54			16			2.0			4	mA
		DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min (3), I_{OL} = Max, DM54		0.2	0.4		0.22	0.3		0.25	0.4	V
		V_{CC} = Min (3), I_{OL} = Max, DM74		0.2	0.4			0.4		0.35	0.5	
		V_{CC} = Min (3), I_{OL} = 4 mA, DM74								0.25	0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			0.1				mA
		V_{CC} = Max, V_I = 7V									0.1	
I_{IH}	High Level Input Current, Data Inputs	V_{CC} = Max, V_I = 2.4V			40			10				µA
		V_{CC} = Max, V_I = 2.7V									20	
	High Level Input Current, Clear Input	V_{CC} = Max, V_I = 2.4V			80			10				
		V_{CC} = Max, V_I = 2.7V									20	
I_{IL}	Low Level Input Current, Data Inputs	V_{CC} = Max, V_I = 0.4V			−1.6			−0.18			−0.4	mA
	Low Level Input Current, Clear Input	V_{CC} = Max, V_I = 0.4V			−1.6			−0.18			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)(3)	−10		−40	−2.5		−12	−30		−150	mA
I_{CC}	Supply Current (Quiescent or Triggered)	V_{CC} = Max(4)(5)(6), LS122								6	11	mA
		V_{CC} = Max(4)(5)(6), Others		46	66		5	7.5		12	20	

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

Parameter		From (Input)	To (Output)	DM54/74 123 Conditions	Min	Typ	Max	DM54L/74L L123A Conditions	Min	Typ	Max	DM54LS/74LS LS122, LS123 Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A	Q	$C_{EXT} = 0$, $R_{EXT} = 5\ k\Omega$, $C_L = 15\ pF$, $R_L = 400\Omega$		22	33	$C_{EXT} = 0$, $R_{EXT} = 32\ k\Omega$, $C_L = 50\ pF$, $R_L = 4\ k\Omega$		120	175	$C_{EXT} = 0$, $R_{EXT} = 5\ k\Omega$, $C_L = 15\ pF$, $R_L = 2\ k\Omega$		22	33	ns
		B	Q			19	28			86	135			29	44	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A	$\overline{Q}$			30	40			120	180			30	45	ns
		B	$\overline{Q}$			27	36			86	135			37	56	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Q			18	27			45	65			18	27	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clear	$\overline{Q}$			30	40			95	140			30	45	ns
$t_{WQ(MIN)}$	Minimum Width of Pulse at Output Q	A or B	Q			45	65			220	330			116	200	ns
t_{WQ}	Width of Pulse at Output Q	A or B	Q	$C_{EXT} = 1000\ pF$, $R_{EXT} = 10\ k\Omega$, $C_L = 15\ pF$, $R_L = 400\Omega$	2.76	3.03	3.37	$C_{EXT} = 1000\ pF$, $R_{EXT} = 100\ k\Omega$, $C_L = 50\ pF$, $R_L = 4\ k\Omega$	30.6	34.0	37.4	$C_{EXT} = 1000\ pF$, $R_{EXT} = 10\ k\Omega$, $C_L = 15\ pF$, $R_L = 2\ k\Omega$	4	4.5	5	ns
t_W	Pulse Width	A or B Inputs High			40				130				40			ns
		A or B Inputs Low			40				130				40			ns
		Clear Low			40				130				40			ns
R_{EXT}	External Timing Resistance	DM54			5		25		5		200		5		225	kΩ
		DM74			5		50		5		400		5		360	kΩ
C_{EXT}	External Capacitance				No Restriction				No Restriction				No Restriction			
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal	DM54					50				40				50	pF
		DM74					50				50				50	pF

Notes

(1) All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) Ground C_{EXT} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{EXT} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.

(4) Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_{EXT} = 0.02\mu F$, and $R_{EXT} = 25\ k\Omega$.

(5) I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs. A inputs grounded, all outputs open, $C_{EXT} = 0.02\mu F$, and $R_{EXT} = 25\ k\Omega$.

(6) With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock. (LS122, LS123)

LS122, LS123 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		CONDITIONS			DM54/74 125, 126 MIN	TYP(1)	MAX	DM54LS/74LS LS125, LS126 MIN	TYP(1)	MAX	DM74S S134 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			N/A	V
				DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5							V
			I_I = −18 mA							−1.5			−1.2	
I_{OH}	High Level Output Current			DM54			−2.0			−1.0			N/A	mA
				DM74			−5.2			−2.6			−6.5	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.3		2.4	3.4			N/A		V
				DM74	2.4	3.1		2.4	3.1		2.4	3.2		
I_{OL}	Low Level Output Current			DM54			16			8			N/A	mA
				DM74			16			16			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = Max	DM54			0.4			0.4			N/A	V
				DM74			0.4			0.5			0.5	
			I_{OL} = 4 mA	DM74						0.4				
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V	V_{IL} = 0.7V	V_O = 0.4V						−20				μA
				V_O = 2.7V						20				
			V_{IL} = 0.8V	V_O = 0.4V			−40							
				V_O = 0.5V									−50	
				V_O = 2.4V			40						50	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1						1	mA
			V_I = 7.0V							0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−1.6			−0.4				mA
			V_I = 0.5V										−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−30		−70	−30		−130		N/A		mA
				DM74	−28		−70	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			See Table									

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/DM74LS and DM74S, duration of short circuit should not exceed one second.

(3) Data for DM54LS/74LS125, 126 is preliminary.

LS125, LS126 To Be Announced In 1976

Supply Currents

DEVICE	CONDITIONS		I_{CC} (mA)		
	DATA INPUTS	OUTPUT CONTROLS	MIN	TYP(1)	MAX
125	0V	4.5V		32	54
126	0V	0V		36	62
LS125	0V	4.5V		11	18
LS126	0V	0V		12	21
S134	0V	0V		7	13
	5V	0V		9	16
	5V	5V		14	25

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM54/74 125 MIN	125 TYP	125 MAX	DM54/74 126 MIN	126 TYP	126 MAX	DM54LS/74LS LS125 MIN	LS125 TYP	LS125 MAX	DM54LS/74LS LS126 MIN	LS126 TYP	LS126 MAX	DM74S CONDITIONS	DM74S S134 MIN	S134 TYP	S134 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 400Ω, R_L = 2 kΩ (LS)		10	15		10	15		10	15		10	15	C_L = 15 pF, R_L = 280Ω		4	6	ns
															C_L = 50 pF, R_L = 280Ω		5.5	9	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	18		12	18		12	18		12	18	C_L = 15 pF, R_L = 280Ω		5	7.5	ns
															C_L = 50 pF, R_L = 280Ω		7	11	
t_{ZH}	Output Enable Time to High Level			12	18		13	19		12	18		13	19	C_L = 50 pF, R_L = 280Ω		13	19.5	ns
t_{ZL}	Output Enable Time to Low Level			16	25		16	25		16	25		16	25			14	21	ns
t_{HZ}	Output Disable Time From High Level	C_L = 5 pF, R_L = 400Ω, R_L = 2 kΩ (LS)		5	8		10	16		5	8		10	16	C_L = 5 pF, R_L = 280Ω		5.5	8.5	ns
t_{LZ}	Output Disable Time From Low Level			9	14		14	20		9	14		14	20			9	14	ns

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		CONDITIONS	DM74S S135 MIN	DM74S S135 TYP(1)	DM74S S135 MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{OH}	High Level Output Current				−1	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1 mA	2.7	3.4		V
I_{OL}	Low Level Output Current				20	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20 mA			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max(3)		65	99	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

(3) I_{CC} is measured with the inputs grounded and the outputs open.

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER(4)		FROM (INPUT)	CONDITIONS		DM74S S135 MIN	DM74S S135 TYP	DM74S S135 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A or B	B or A = L, C = L	C_L = 15 pF, R_L = 280Ω		8.5	13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					11	15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A or B	B or A = H, C = L			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					9	13.5	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A or B	B or A = L, C = H			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					6.5	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A or B	B or A = H, C = H			8.5	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7	11	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C	A = B			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					9.5	14.5	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C	A ≠ B			7.5	11.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					8	12	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS			DM54LS/74LS LS136, LS266 MIN	DM54LS/74LS LS136, LS266 TYP(1)	DM54LS/74LS LS136, LS266 MAX	DM74S S136 MIN	DM74S S136 TYP(1)	DM74S S136 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.7			N/A	V
				DM74			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5			−1.2	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, V_{OH} = 5.5V					100			250	μA
V_{OH}	High Level Output Voltage						5.5			5.5	V
I_{OL}	Low Level Output Current			DM54			4			N/A	mA
				DM74			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IH} = 2V V_{IL} = Max	I_{OL} = Max	DM54		0.25	0.4			N/A	V
				DM74		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74			0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V							1	mA
			V_I = 7V				0.2				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					40			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−0.6				mA
			V_I = 0.5V							−2	
I_{CC}	Supply Current	V_{CC} = Max(2)		LS136		6.1	10				mA
				Others		8	13		50	75	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	CONDITIONS		DM54LS/74LS LS136, LS266			DM74S S136			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A or B	Other Input Low	C_L = 15 pF, R_L = 2 kΩ (54LS/74LS), R_L = 280Ω (74S)		18	30		8	12.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A or B	Other Input Low			18	30		7.5	12	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A or B	Other Input High			18	30		8	12.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A or B	Other Input High			18	30		7.5	12	ns

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS		DM54/74 365, 366, 367, 368 MIN	DM54/74 365, 366, 367, 368 TYP(1)	DM54/74 365, 366, 367, 368 MAX	DM54LS/74LS LS365, LS366 LS367, LS368 MIN	DM54LS/74LS LS365, LS366 LS367, LS368 TYP(1)	DM54LS/74LS LS365, LS366 LS367, LS368 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7	V
			DM74			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA			−1.5				V
			I_I = −18 mA						−1.5	
I_{OH}	High Level Output Current		DM54			−2.0			−1.0	mA
			DM74			−5.2			−2.6	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	DM54	2.4	3.1		2.4	3.4		V
			DM74	2.4	3.1		2.4	3.1		
I_{OL}	Low Level Output Current		DM54			32			8	mA
			DM74			32			16	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = 8 mA						0.4	V
			I_{OL} = 16 mA, DM74						0.5	
			I_{OL} = 32 mA			0.4				
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V	V_O = 0.4V			−40			−20	µA
			V_O = 2.4V			40				
			V_O = 2.7V						20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V			1				mA
			V_I = 7.0V						0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V			40				µA
			V_I = 2.7V						20	
I_{IL}	Low Level Input Current — A Input	V_{CC} = Max	V_I = 0.5V, Both $\overline{G}$ Inputs at 2V			−40			−20	µA
			V_I = 0.4V, Both $\overline{G}$ Inputs at 0.4V			−1.6			−0.4	mA
	Low Level Input Current — $\overline{G}$ Input		V_I = 0.4V			−1.6			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−40		−115	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max	365, LS365, 367, LS367		65	85		22	28	mA
			366, LS366, 368, LS368		59	77		20	26	

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		DM54/74 CONDITIONS	DM54/74 365, 367 TYP	DM54/74 365, 367 MAX	DM54/74 366, 368 TYP	DM54/74 366, 368 MAX	DM54LS/74LS CONDITIONS	LS365, LS367 TYP	LS365, LS367 MAX	LS366, LS368 TYP	LS366, LS368 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L = 50$ pF, $R_L = 400\Omega$	10	16	11	17	$C_L = 15$ pF, $R_L = 2$ kΩ		16		17	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		14	22	10	16			22		16	ns
t_{ZH}	Output Enable Time to High Level		21	35	21	35			35		35	ns
t_{ZL}	Output Enable Time to Low Level		24	37	24	37			37		37	ns
t_{HZ}	Output Disable Time From High Level	$C_L = 5$ pF, $R_L = 400\Omega$	6	11	6	11	$C_L = 5$ pF, $R_L = 2$ kΩ		11		11	ns
t_{LZ}	Output Disable Time From Low Level		16	27	16	27			27		27	ns

Notes

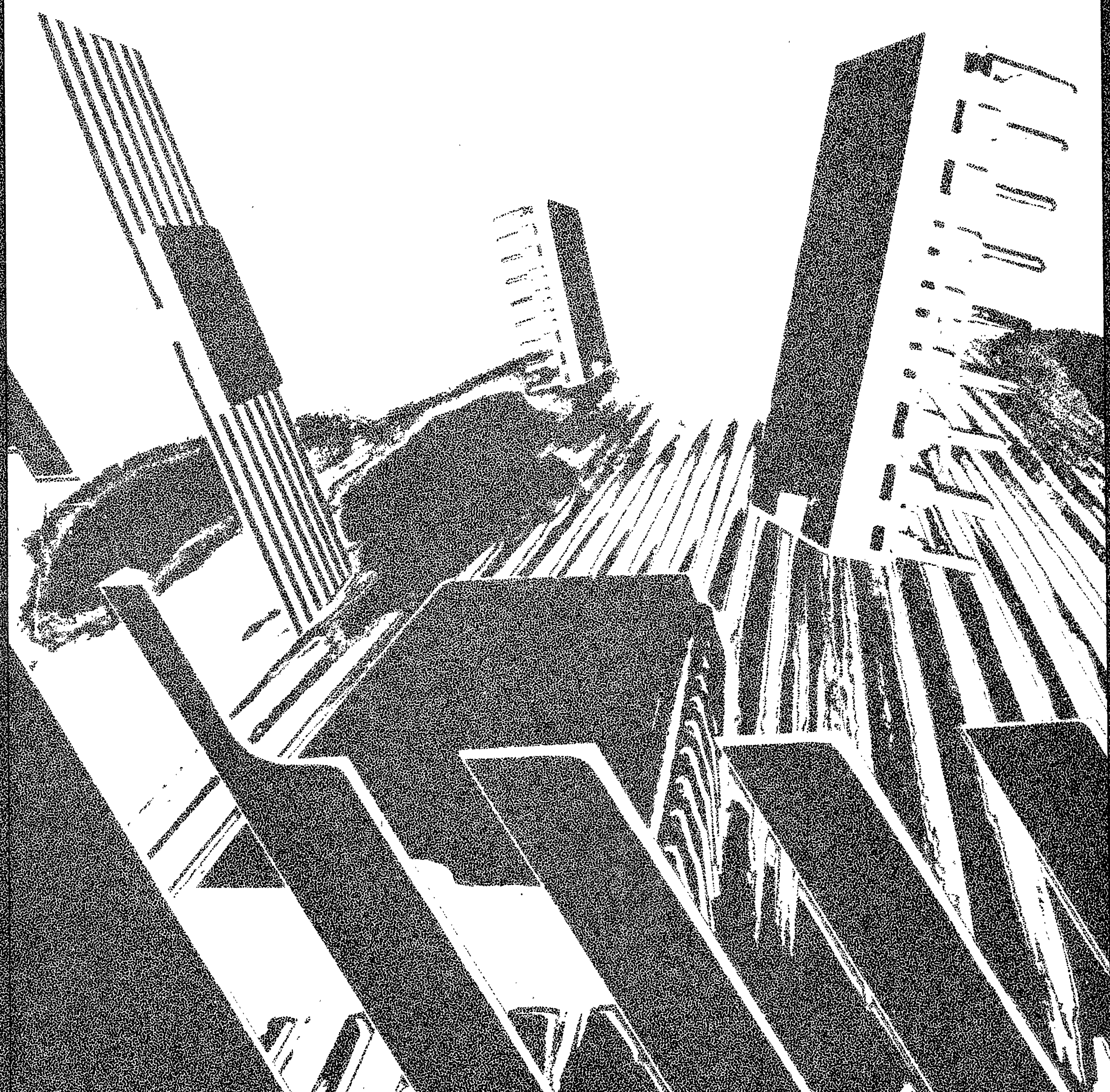
(1) All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) Data for DM54LS/74LS is preliminary.

LS365, LS366, LS367, LS368 To Be Announced In 1976

National Semiconductor
54/74 MSI DEVICES
Section 2



RATINGS		54/74 SERIES	54H/74H SERIES	54L/74L SERIES	54LS/74LS SERIES DIODE INPUTS	54LS/74LS SERIES EMITTER INPUTS	54S/74S SERIES	UNITS
Maximum Allowable Supply Voltage		7	7	8	7	7	7	V
Guaranteed Operating Supply Voltage Range	54	4.50 to 5.50						V
	74	4.75 to 5.25						
Maximum Input Voltage		5.5	5.5	5.5	7	5.5	5.5	V
Maximum Voltage to Open-Collector Outputs*		7	7	8	7	7	7	V
Operating Free-Air Temperature Range	54	−55 to +125						°C
	74	0 to +70						
Storage Temperature Range		−65 to +150						°C

***Except for selected high voltage types, as specified in electrical tables.**

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BCD/Decimal Decoders/Drivers

General Description

The DM5441A/DM7441A is a BCD-to-decimal decoder designed to drive gas-filled NIXIE tubes. The device is also capable of driving other types of low-current lamps and relays.

An over-range decoding feature provides that if binary numbers between 10 and 15 are applied to the input, the least significant bit (0-5) will be decoded on the output.

The DM54141/DM74141 is a BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes.

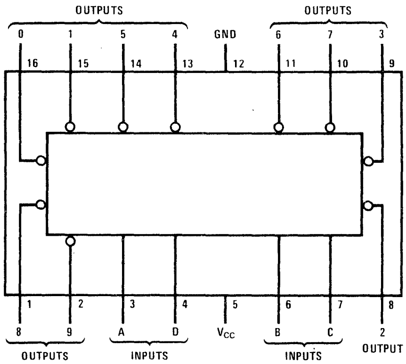
Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the DM54141/DM74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display.

Input clamp diodes are also provided to clamp negative-voltage transitions in order to minimize transmission-line effects.

Features

- Drive cold-cathode, numeric indicator tubes directly
- Fully decoded inputs
- Low leakage current
  - DM54/7441A 1.8μA @ 50V
  - DM54/74141 50μA @ 55V
- Low power dissipation
  - DM54/7441A 105 mW typical
  - DM54/74141 55 mW typical

Connection Diagram



5441A(J), (W); 7441A(J), (N), (W);
54141(J), (W); 74141(J), (N), (W)

Truth Tables

5441A/7441A

INPUT				OUTPUT ON*
D	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
(OVER RANGE)				
H	L	H	L	0
H	L	H	H	1
H	H	L	L	2
H	H	L	H	3
H	H	H	L	4
H	H	H	H	5

54141/74141

INPUT				OUTPUT ON*
D	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
(OVER RANGE)				
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = High Level, L = Low Level

*All other outputs are off

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM54/74 41A MIN	41A TYP(1)	41A MAX	DM54/74 141 MIN	141 TYP(1)	141 MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			N/A			−1.5	V
V_{OL}	On-State Output Voltage	V_{CC} = Min, I_O = 7 mA, −55°C to +70°C			2.5			2.5	V
		V_{CC} = Min, I_O = 7 mA, 125°C			3.0			3.0	V
I_{OH}	Off-State Reverse Current	V_{CC} = Max, V_O = 50V, T_A = 125°C			60				μA
		V_{CC} = Max, V_O = 50V, T_A = 70°C			40				μA
		V_{CC} = Max, V_O = 50V, T_A = −55°C, 0°C, 25°C			1.8				μA
		V_{CC} = Max, V_O = 55V						50	μA
I_{OH}	Off-State Reverse Current for Input Counts 10-15	V_{CC} = Max, V_O = 30V, T_A = 55°C			N/A			5	μA
		V_{CC} = Max, V_O = 30V, T_A = 70°C			N/A			15	μA
V_{OH}	Off-State Output Voltage	V_{CC} = Max, I_O = 0.5 mA				60			V
		V_{CC} = Max, I_O = 1.0 mA	70						V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, A Input		3	40			40	μA
		V_{CC} = Max, V_I = 2.4V, B, C, or D Input		3	40			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, A Input		−1.0	−1.6			−1.6	mA
		V_{CC} = Max, V_I = 0.4V, B, C, or D Input		−1.0	−1.6			−3.2	mA
I_{CC}	Supply Current	V_{CC} = Max(2)		21	36		11	25	mA

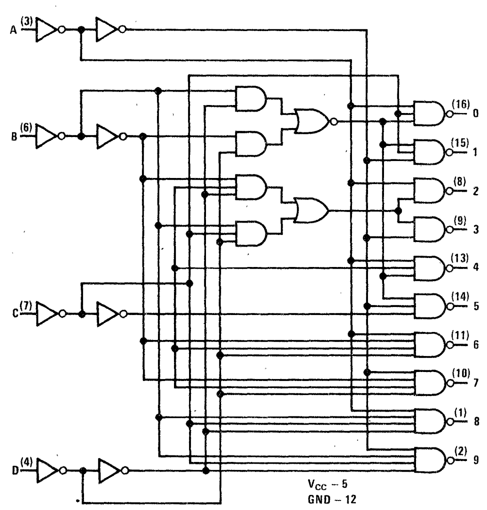
Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

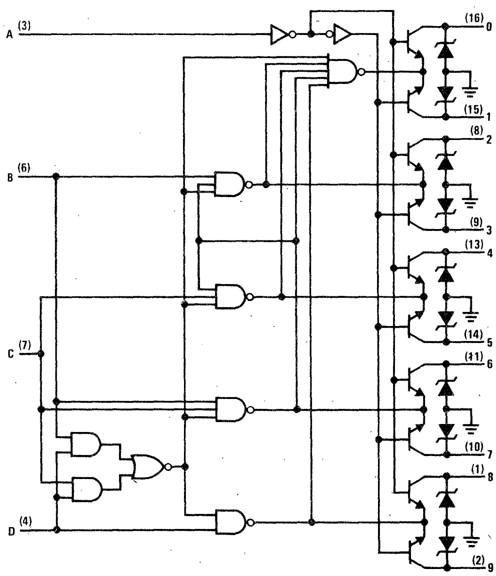
(2) I_{CC} is measured with all inputs grounded and outputs open.

Logic Diagrams

5441A/7441A



54141/74141



MSI

DM54/DM7442,L42A,LS42

BCD/Decimal Decoders

General Description

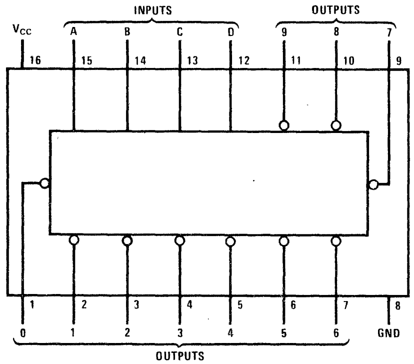
These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10-15) input conditions.

Features

- Diode clamped inputs
- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions

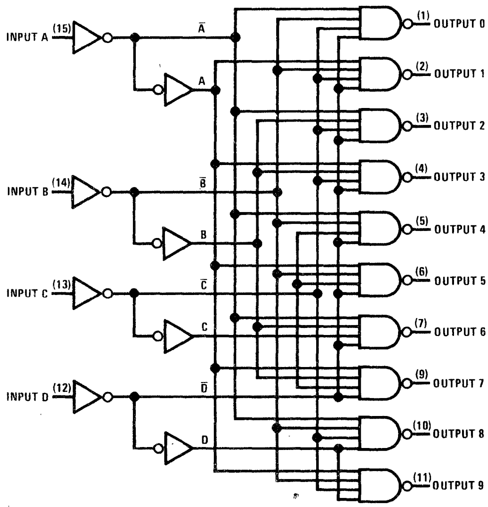
TYPE	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAY
42	140 mW	17 ns
L42A	15 mW	53 ns
LS42	35 mW	17 ns

Connection Diagram



5442(J), (W); 7442(J), (N), (W);
54L42A/74L42A(J), (N), (W);
54LS42/74LS42(J), (N), (W)

Logic Diagram



Truth Table

NO.	42, L42A, LS42 BCD INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level
L = Low Level

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS			DM54/74			DM54L/74L			DM54LS/74LS			UNITS
					42			L42A			LS42			
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			0.7	V
				DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5		N/A					V
			I_I = −18 mA						N/A				−1.5	
I_{OH}	High Level Output Current						−800			−200			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OH} = Max	DM54	2.4	3.4		2.4	3.4		2.5	3.5		V
				DM74	2.4	3.4		2.4	3.4		2.7	3.5		
I_{OL}	Low Level Output Current			DM54			16			2			4	mA
				DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = 4 mA	DM74								0.25	0.4	V
			I_{OL} = Max	DM54		0.2	0.4		0.15	0.3		0.25	0.4	
				DM74		0.2	0.4		0.2	0.4		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			0.1				mA
			V_I = 7V										0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40			10				μA
			V_I = 2.7V										20	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V for L42A							−0.18				mA
			V_I = 0.4V for Others				−1.6						−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−55	−3		−15	−30		−130	mA
				DM74	−18		−55	−3		−15	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max(3)		DM54		28	41		3.0	5.3		7	13	mA
				DM74		28	56		3.0	5.3		7	13	

Notes:

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		DM54/74 42				DM54L/74L L42A				DM54LS/74LS LS42				UNITS
		CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From A, B, C, or D Through 2 Levels of Logic	$C_L = 15$ pF, $R_L = 400\Omega$		14	25	$C_L = 50$ pF, $R_L = 4$ kΩ		65	130	$C_L = 15$ pF, $R_L = 2$ kΩ		14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From A, B, C, or D Through 3 Levels of Logic			17	30			70	140			17	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From A, B, C, and D Through 2 Levels of Logic			10	25			30	60			10	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From A, B, C, and D Through 3 Levels of Logic			17	30			35	70			17	30	ns

BCD/Decimal Decoders/Drivers

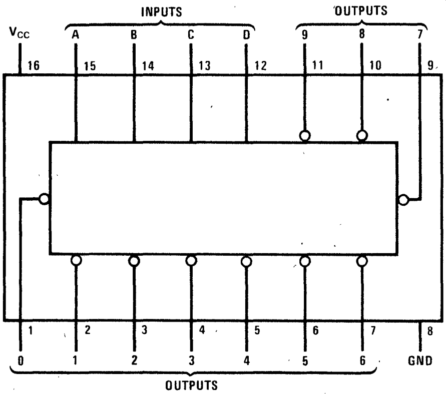
General Description

These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10-15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

Features

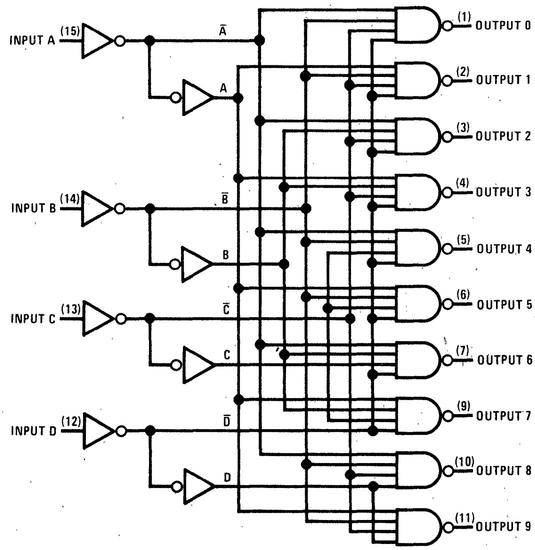
- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

Connection Diagram



5445(J), (W); 7445(J), (N), (W);
54145(J), (W); 74145(J), (N), (W)

Logic Diagram



Truth Table

NO.	INPUTS D	C	B	A	OUTPUTS 0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level (Off), L = Low Level (On)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54/74 45, 145 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
$V_{O(ON)}$	On-State Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V	$I_{O(ON)}$ = 80 mA		0.5	0.9	V
			$I_{O(ON)}$ = 20 mA			0.4	V
$V_{O(OFF)}$	Off-State Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, $I_{O(OFF)}$ = 250μA	45	30			V
			145	15			V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max(2)	DM54		43	62	mA
			DM74		43	70	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) I_{CC} is measured with all inputs grounded and outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM54/74 45, 145 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 100Ω			30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 100Ω			30	ns

BCD/7-Segment Decoders/Drivers

General Description

The 46A, 47A and LS47 feature active-low outputs designed for driving common-anode LED's or incandescent indicators directly; and the 48, LS48 and LS49 feature active-high outputs for driving lamp buffers or common-cathode LED's. All of the circuits except the LS49 have full ripple-blanking input/output controls and a lamp test input. The LS49 features a direct blanking input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

All of the circuits except the LS49 incorporate automatic leading and/or trailing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a high logic level. All types (including LS49) contain an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing), or to inhibit the outputs.

Features

- All circuit types feature lamp intensity modulation capability

5446A/7446A, 5447A/7447A, 54LS47/74LS47

- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

5448/7448, 54LS48/74LS48

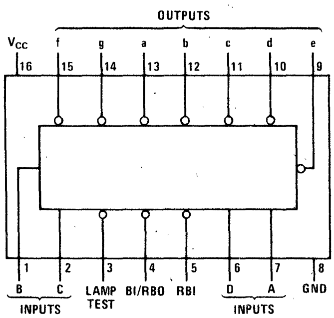
- Internal pull-ups eliminate need for external resistors
- Lamp-test provision
- Leading/trailing zero suppression

54LS49/74LS49

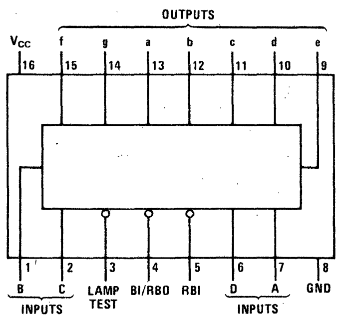
- Open-collector outputs
- Blanking input

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
DM5446A	low	open-collector	40 mA	30V	320 mW	J, N, W
DM5447A	low	open-collector	40 mA	15V	320 mW	J, N, W
DM5448	high	2-kΩ pull-up	6.4 mA	5.5V	265 mW	J, N, W
DM54LS47	low	open-collector	12 mA	15V	35 mW	J, N, W
DM54LS48	high	2 kΩ pull-up	2 mA	5.5V	125 mW	J, N, W
DM54LS49	high	open-collector	4 mA	5.5V	40 mW	J, N, W
DM7446A	low	open-collector	40 mA	30V	320 mW	J, N, W
DM7447A	low	open-collector	40 mA	15V	320 mW	J, N, W
DM7448	high	2-kΩ pull-up	6.4 mA	5.5V	265 mW	J, N, W
DM74LS47	low	open-collector	24 mA	15V	35 mW	J, N, W
DM74LS48	high	2 kΩ pull-up	6 mA	5.5V	125 mW	J, N, W
DM74LS49	high	open-collector	8 mA	5.5V	40 mW	J, N, W

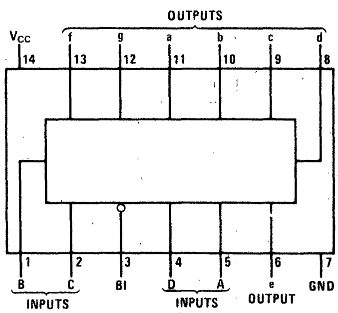
Connection Diagrams



5446A/7446A(J), (N), (W);
5447A/7447A(J), (N), (W);
54LS47/74LS47(J), (N), (W)



5448/7448(J), (N), (W);
54LS48/74LS48(J), (N), (W)



54LS49/74LS49(J), (N), (W)

LS47, LS48, LS49 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS		DM54/74 46A, 47A MIN	DM54/74 46A, 47A TYP(1)	DM54/74 46A, 47A MAX	DM54/74 48 MIN	DM54/74 48 TYP(1)	DM54/74 48 MAX	DM54LS/74LS LS47 MIN	DM54LS/74LS LS47 TYP(1)	DM54LS/74LS LS47 MAX	DM54LS/74LS LS48 MIN	DM54LS/74LS LS48 TYP(1)	DM54LS/74LS LS48 MAX	DM54LS/74LS LS49 MIN	DM54LS/74LS LS49 TYP(1)	DM54LS/74LS LS49 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7			0.7			0.7	V
				DM74			0.8			0.8			0.8			0.8			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA			−1.5			−1.5										V
				I_I = −18 mA									−1.5			−1.5			−1.5	
I_{OH}	High Level Output Current	a thru g	V_{CC} = Min, V_{IH} = 2V							−400						−100				µA
		BI/RBO	V_{IL} = Max				−200			−200			−50			−50				
			V_{OH} = 5.5V																250	
V_{OH}	High Level Output Voltage	a thru g	V_{CC} = Min, V_{IH} = 2V					2.4	4.2					2.4	4.2				5.5	V
		BI/RBO	V_{IL} = Max, I_{OH} = Max		2.4	3.7		2.4	3.7		2.4	4.2		2.4	4.2				N/A	
I_{OL}	Low Level Output Current	a thru g		DM54			40			6.4			12			2			4	mA
				DM74			40			6.4			24			6			8	
		BI/RBO		DM54			8			8			1.6			1.6			N/A	
				DM74			8			8			3.2			3.2			N/A	
V_{OL}	Low Level Output Voltage	a thru g	V_{IH} = 2V, V_{IL} = Max	I_{OL} = Max, DM54		0.3	0.4		0.27	0.4		0.25	0.4		0.25	0.4		0.25	0.4	V
				I_{OL} = Max, DM74		0.3	0.4		0.27	0.4		0.35	0.5		0.35	0.5		0.35	0.5	
		V_{CC} = Max		I_{OL} = Max/2, DM74 Only		N/A			N/A			0.25	0.4		0.25	0.4		0.25	0.4	
		BI/RBO		I_{OL} = Max, DM54		0.27	0.4		0.27	0.4		0.25	0.4		0.25	0.4		N/A		
				I_{OL} = Max, DM74		0.27	0.4		0.27	0.4		0.35	0.5		0.35	0.5				
		V_{CC} = Min		I_{OL} = Max/2, DM74 Only		N/A			N/A			0.25	0.4		0.25	0.4		N/A		
$I_{O(OFF)}$	Off-State Output Current	a thru g	V_{CC} = Max, V_{IH} = 2V, V_{IL} = Max	$V_{O(OFF)}$ = Max			0.25						0.25					N/A		mA
				V_O = 0.85V				−1.3	−2					−1.3	−2					
$V_{O(OFF)}$	Off-State Output Voltage	a thru g		46A			30													V
				Others			15			5.5			15			5.5			5.5	
I_I	Input Current at Maximum Input Voltage	Any Input except BI/RBO	V_{CC} = Max	V_I = 5.5V			1			1										mA
				V_I = 7V									0.1			0.1			1	
		BI/RBO		V_I = 7V									0.1						N/A	
I_{IH}	High Level Input Current	Any Input Except BI/RBO	V_{CC} = Max	V_I = 2.4V			40			40										µA
				V_I = 2.7V									20			20			20	
		BI/RBO		V_I = 2.7V									20						N/A	
I_{IL}	Low Level Input Current	Any Input Except BI/RBO	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6			−0.36			−0.36			−0.36	mA
		BI/RBO					−4			−4			−1			−1			N/A	
I_{OS}	Short Circuit Output Current	BI/RBO	V_{CC} = Max				−4			−4	−0.3		−2	−0.3		−2			N/A	mA
I_{CC}	Supply Current		V_{CC} = Max(2)	DM54		60	85		50	76		7	13		25	38		8	15	mA
				DM74		60	103		50	90		7	13		25	38		8	15	

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

DEVICE	CONDITIONS	t_{PLH} and t_{PHL} (ns) Propagation Delay Time From A Input			t_{PLH} and t_{PHL} (ns) Propagation Delay Time From RBI Input		
		MIN	TYP	MAX	MIN	TYP	MAX
46A, 47A	$C_L = 15$ pF, $R_L = 120\Omega$			100			100
48	$C_L = 15$ pF, $R_L = 1$ kΩ			100			100
LS47	$C_L = 15$ pF, $R_L = 665\Omega$			100			100
LS48	$C_L = 15$ pF, $R_L = 4$ kΩ			100			
	$C_L = 15$ pF, $R_L = 6$ kΩ						100
LS49	$C_L = 15$ pF, $R_L = 2$ kΩ			100			
	$C_L = 15$ pF, $R_L = 6$ kΩ						100

Notes

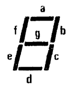
(1) All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

(2) I_{CC} is measured with all outputs open and all inputs at 4.5V.

Output Display

NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

SEGMENT IDENTIFICATION



Truth Tables

46A, 47A, LS47

DECIMAL OR FUNCTION	INPUTS						BI/RBO(1)	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	(2)
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(3)
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(4)
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(5)

48, LS48

DECIMAL OR FUNCTION	INPUTS						BI/RBO(1)	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	(2)
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	(3)
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	(4)
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	(5)

Notes

(1) BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

(2) The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

(3) When a low logic level is applied directly to the blanking input (BI), all segment outputs are H regardless of the level of any other input.

(4) When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).

(5) When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L.

H = High Level, L = Low Level, X = Don't Care

Truth Tables (Continued)

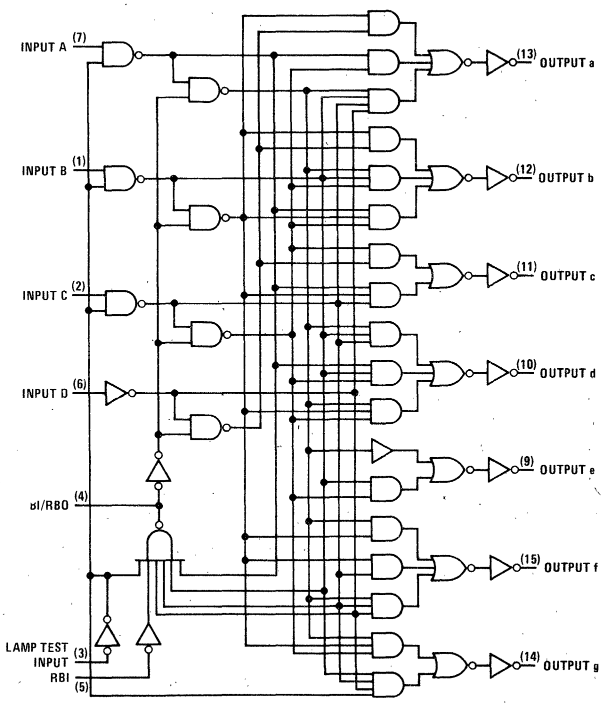
LS49

DECIMAL OR FUNCTION	INPUTS					OUTPUTS							NOTE
	D	C	B	A	BI	a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	L	(1)
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	(2)

Notes
(1) The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
(2) When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
H = High Level, L = Low Level, X = Don't Care

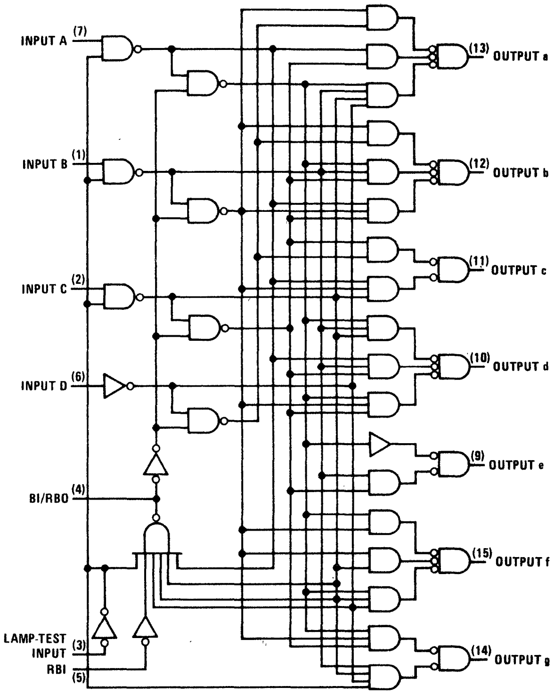
Logic Diagrams

46A, 47A, LS47

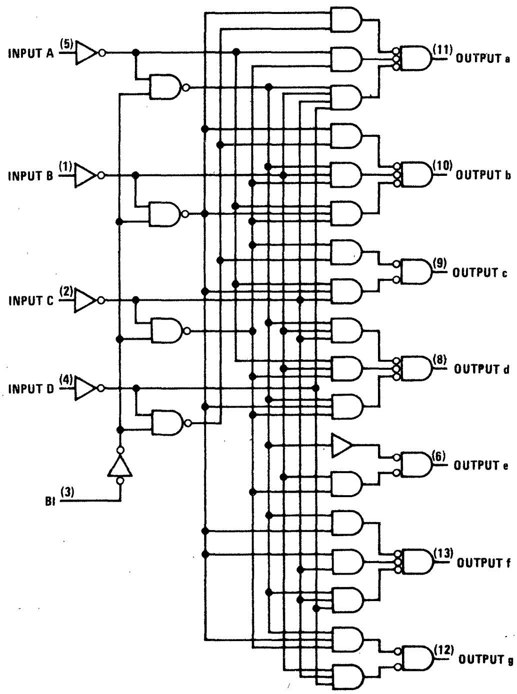


Logic Diagrams (Continued)

48, LS48



LS49



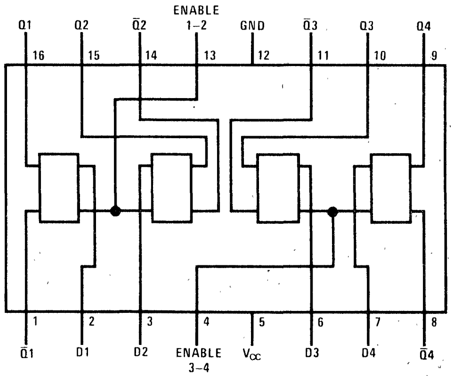
Quad Latches

General Description

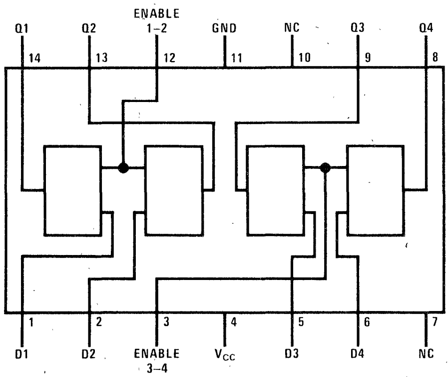
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The DM5475/DM7475, DM54L75A/DM74L75A, and DM54LS75/DM74LS75 feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages. For higher component density applications, the DM54LS77/DM74LS77 4-bit latches are available in 14-pin flat packages (only).

Connection Diagrams



5475/7475(J), (N), (W); 54L75A/74L75A(J), (N), (W);
54LS75/74LS75(J), (N), (W)



54LS77/74LS77(W)

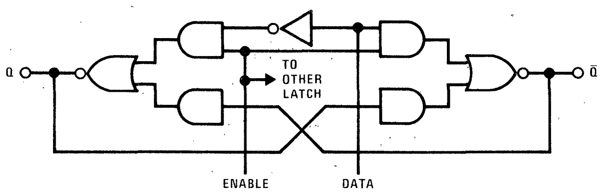
Truth Table (Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

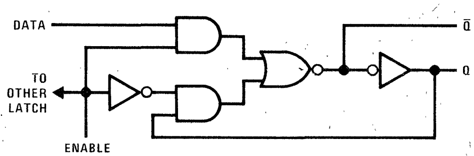
H = High Level, L = Low Level, X = Don't Care
Q_0 = The Level of Q Before the High-to-Low Transition of G

Logic Diagrams (Each Latch)

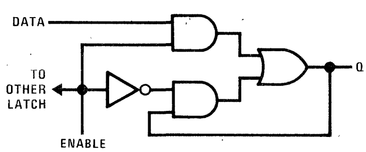
75, L75



LS75



LS77



Tentative Data For LS75, LS77

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM54/74 75 MIN	DM54/74 75 TYP(1)	DM54/74 75 MAX	DM54L/74L L75A MIN	DM54L/74L L75A TYP(1)	DM54L/74L L75A MAX	DM54LS/74LS LS75, LS77 MIN	DM54LS/74LS LS75, LS77 TYP(1)	DM54LS/74LS LS75, LS77 MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			2			V
V_{IL}	Low Level Input Voltage	DM54			0.8			0.7			0.7	V
		DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA			−1.5			−1.5				V
		V_{CC} = Min, $I_I = -18$ mA									−1.5	
I_{OH}	High Level Output Current				−400			−200			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max; DM54	2.4	3.4		2.4	3.4		2.5	3.5		V
		DM74	2.4	3.4		2.4	3.4		2.7	3.5		
I_{OL}	Low Level Output Current	DM54			16			2			4	mA
		DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max; I_{OL} = 4 mA; DM74								0.25	0.4	V
		I_{OL} = Max; DM54		0.2	0.4			0.3		0.25	0.4	
		I_{OL} = Max; DM74		0.2	0.4		0.2	0.4		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V; D Input			1			0.2				mA
		V_I = 5.5V; G Input			1			0.4				
		V_I = 7V; D Input									0.1	
		V_I = 7V; G Input									0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V; D Input			80			20				μA
		V_I = 2.4V; G Input			80			40				
		V_I = 2.7V; D Input									20	
		V_I = 2.7V; G Input									80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V, 54L/74L, V_I = 0.4V, Others; D Input			−3.2			−0.36			−0.4	mA
		G Input			−3.2			−0.72			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2); DM54	−20		−55	−3	−9	−15	−30		−130	mA
		DM74	−18		−55	−3	−9	−15	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max(3); DM54; LS75								6.3	12	mA
		DM54; Others		32	46		3.5	5.0		6.9	13	
		DM74; LS75								6.3	12	
		DM74; Others		32	50		3.5	5.0		6.9	13	

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	DM54/74 75 CONDITIONS	MIN	TYP	MAX	DM54L/74L L75A CONDITIONS	MIN	TYP	MAX	DM54LS/74LS CONDITIONS	LS75 MIN	LS75 TYP	LS75 MAX	LS77 MIN	LS77 TYP	LS77 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	D	Q	$C_L = 15$ pF, $R_L = 400\Omega$		16	30	$C_L = 50$ pF, $R_L = 4$ kΩ		55	100	$C_L = 15$ pF, $R_L = 2$ kΩ		15	27		11	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	25			50	100			9	17		9	17	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	D	$\overline{Q}$			24	40			75	120			12	20			N/A	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7	15			32	80			7	15			N/A	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G	Q			16	30			50	100			15	27		10	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7	15			32	80			14	25		10	18	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G	$\overline{Q}$			16	30			48	100			16	30			N/A	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7	15			38	80			7	15			N/A	
t_W	Width of Enabling Pulse				20				100				20			20			ns
t_{SETUP}	Setup Time				20				100				20			20			ns
t_{HOLD}	Hold Time				5				25				0			0			ns

Notes

(1) All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

(2) Not more than one output should be shorted at a time, and for the DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CC} is tested with all inputs grounded and all outputs open.

4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

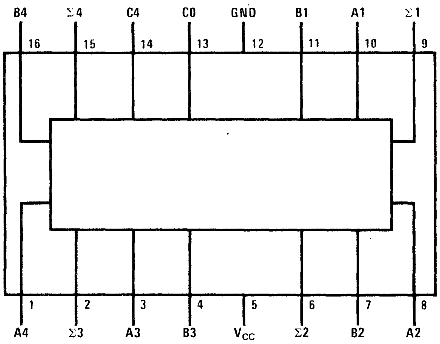
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

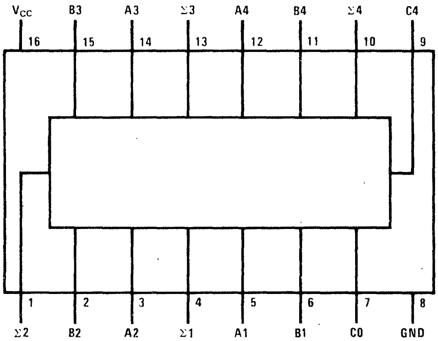
- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry

TYPE	TYPICAL ADD TIMES TWO 8-BIT WORDS	TYPICAL ADD TIMES TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER 4-BIT ADDER
83	23 ns	43 ns	290 mW
LS83A	25 ns	45 ns	95 mW
LS283	25 ns	45 ns	95 mW

Connection Diagrams and Truth Table



5483(J), (W); 7483(J), (N), (W);
54LS83A/74LS83A(J), (N), (W)



54LS283/74LS283(J), (N), (W)

INPUT				OUTPUT WHEN C0 = L / WHEN C2 = L			OUTPUT WHEN C0 = H / WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

Note : Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

LS83A, LS283 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Conditions			DM54/74 83 MIN	DM54/74 83 TYP(1)	DM54/74 83 MAX	DM54LS/74LS LS83A, LS283 MIN	DM54LS/74LS LS83A, LS283 TYP(1)	DM54LS/74LS LS83A, LS283 MAX	UNITS
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.8			0.7	V
					DM74			0.8			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	$I_I = -12$ mA				−1.5				V
				$I_I = -18$ mA							−1.5	
I_{OH}	High Level Output Current	Any Output Except C4						−800			−400	μA
		Output C4						−400			−400	
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V		DM54	2.4	3.4		2.5	3.4		V
			V_{IL} = Max, I_{OH} = Max		DM74	2.4	3.4		2.7	3.4		
I_{OL}	Low Level Output Current	Any Output Except C4			DM54			16			4	mA
					DM74			16			8	
		Output C4			DM54			8			4	
					DM74			8			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min	I_{OL} = 4 mA						0.25	0.4	V
			V_{IH} = 2V	I_{OL} = 8 mA	DM74					0.35	0.5	
			V_{IL} = Max	I_{OL} = Max			0.2	0.4				
I_I	Input Current at Maximum Input Voltage	Any A or B	V_{CC} = Max	V_I = 5.5V				1				mA
				V_I = 7V							0.2	
		C0		V_I = 5.5V				1				
				V_I = 7V							0.1	
I_{IH}	High Level Input Current	Any A or B	V_{CC} = Max	V_I = 2.4V				80				μA
				V_I = 2.7V							40	
		C0		V_I = 2.4V				80				
				V_I = 2.7V							20	
I_{IL}	Low Level Input Current	Any A or B	V_{CC} = Max, V_I = 0.4V					−3.2			−0.8	mA
		C0						−3.2			−0.4	
I_{OS}	Short Circuit Output Current	Any Output Except C4	V_{CC} = Max(2)		DM54	−20		−55	−30		−130	mA
					DM74	−18		−55	−30		−130	
		Output C4			DM54	−20		−70	−30		−130	
					DM74	−18		−70	−30		−130	
I_{CC}	Supply Current		V_{CC} = Max Outputs Open	All Inputs Grounded						22	39	mA
				All B Low, Other Inputs at 4.5V						19	34	
				All Inputs at 4.5V			58	79		19	34	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

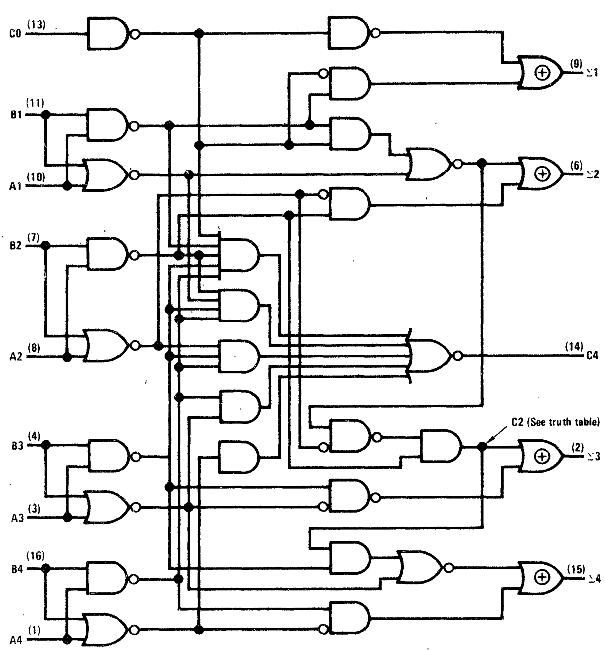
(2) Only one output should be shorted at a time, and for 54LS/74LS duration of short circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	DM54/74 83 CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS83A, LS283 CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C0	Σ_1 or Σ_2	$C_L = 15\ pF$, $R_L = 400\Omega$		22	32	$C_L = 15\ pF$, $R_L = 2\ k\Omega$		16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					20	32			15	24	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C0	Σ_3			28	47			16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22	38			15	24	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C0	Σ_4			28	47			16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					28	47			15	24	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	Σ_i				38			15	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						33			15	24	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C0	C4	$C_L = 15\ pF$, $R_L = 780\Omega$		12	19			11	17	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12	19			11	17	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	C4			12	19			11	17	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12	19			12	17	ns

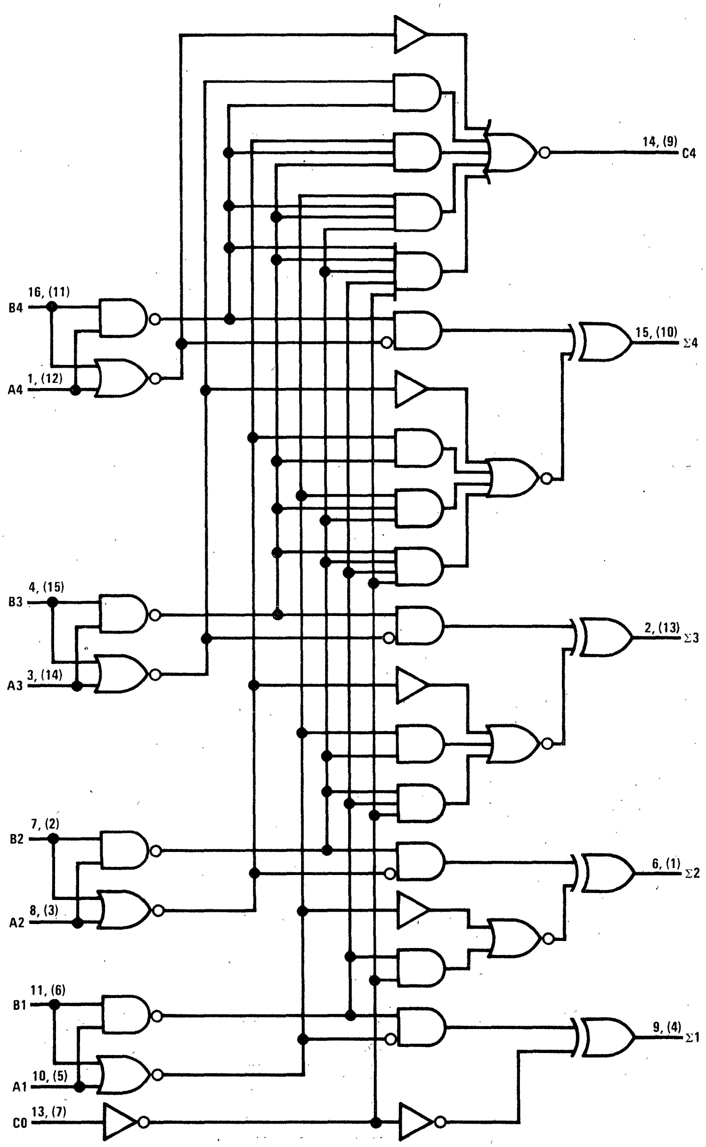
Logic Diagrams

83



Logic Diagrams (Continued)

LS83A, LS283



Note: Pin numbers shown in parenthesis are for LS283

4-Bit Magnitude Comparators

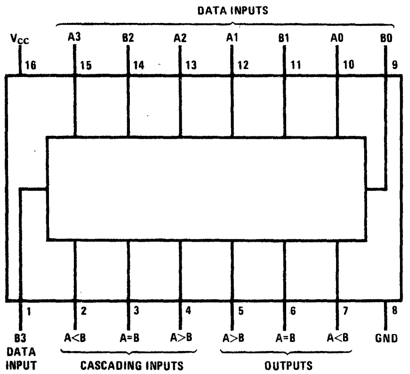
General Description

These four-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input and in addition for the L85, low-level voltages applied to the A > B and A < B inputs. The cascading paths of the 85, and LS85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words.

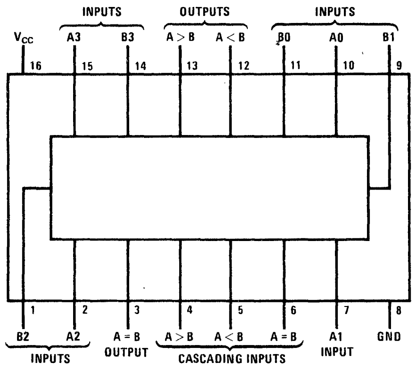
Features

TYPE	TYPICAL POWER DISSIPATION	TYPICAL DELAY (4-BIT WORDS)
85	275 mW	23 ns
L85	20 mW	55 ns
LS85	52 mW	24 ns

Connection Diagrams



5485(J), (W); 7485(J), (N), (W); 54LS85/74LS85(J), (N), (W)



54L85/74L85(J), (N), (W)

Truth Tables

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

85, LS85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

L85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = High Level, L = Low Level, X = Don't Care

LS85 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS			DM54/74 85 MIN	DM54/74 85 TYP(1)	DM54/74 85 MAX	DM54L/74L L85 MIN	DM54L/74L L85 TYP(1)	DM54L/74L L85 MAX	DM54LS/74LS LS85 MIN	DM54LS/74LS LS85 TYP(1)	DM54LS/74LS LS85 MAX	UNITS
V_{IH}	High Level Input Voltage					2			2	1.3		2			V
V_{IL}	Low Level Input Voltage				DM54			0.8		1.3	0.7			0.7	V
					DM74			0.8		1.3	0.7			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA				−1.5			N/A				V
				I_I = −18 mA							N/A			−1.5	
I_{OH}	High Level Output Current							−800			−200			−400	µA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max			2.4			2.4			2.4	3.4		V
I_{OL}	Low Level Output Current				DM54			16			2			4	mA
					DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = Max	DM54			0.4		0.15	0.3		0.25	0.4	V
					DM74			0.4		0.2	0.4		0.35	0.5	
				I_{OL} = 4 mA	DM74								0.25	0.4	
I_I	Input Current at Maximum Input Voltage	A < B, A > B, or A = B (5)	V_{CC} = Max	V_I = 5.5V				1.0			0.1				mA
				V_I = 7V										0.1	
		All Other Inputs		V_I = 5.5V				1.0			0.3				
				V_I = 7V										0.3	
I_{IH}	High Level Input Current	A < B, A > B, or A = B (5)	V_{CC} = Max	V_I = 2.4V				40			10				µA
				V_I = 2.7V										20	
		All Other Inputs		V_I = 2.4V				120			30				
				V_I = 2.7V										60	
I_{IL}	Low Level Input Current	A < B, A > B, or A = B (5)	V_{CC} = Max	V_I = 0.3V							−0.18				mA
				V_I = 0.4V				−1.6						−0.4	
		All Other Inputs		V_I = 0.3V							−0.54				
				V_I = 0.4V				−4.8						−1.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		DM54	−20		−55	−3		−15	−30		−130	mA
					DM74	−18		−55	−3		−15	−30		−130	
I_{CC}	Supply Current		V_{CC} = Max	Condition A	(3)						6.6				mA
				Condition B	(3)						7.0				
					(4)		55	88					10.4	20	

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	DM54/74 85 CONDITIONS	MIN	TYP	MAX	DM54L/74L L85 CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS85 CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B Data Input	A < B, A > B	1	$C_L = 15\ pF$, $R_L = 400\Omega$		7		$C_L = 50\ pF$, $R_L = 4\ k\Omega$		70	115	$C_L = 15\ pF$, $R_L = 2\ k\Omega$		14		ns
				2			12				70	115			19		
				3			17	26			70	115			24	36	
			A = B	4			23	35			70	115			23	40	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Any A or B Data Input	A < B, A > B	1			11				55	90			11		ns
				2			15				55	90			15		
				3			20	30			55	90			20	30	
			A = B	4			20	30			55	90			20	30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A < B or A = B	A > B	1			7	11			55	100			14	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A < B or A = B	A > B	1			11	17			40	65			11	17	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A = B	A = B	2			13	20			55	100			13	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A = B	A = B	2			11	17			40	65			11	17	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A > B or A = B	A < B	1			7	11			55	100			14	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A > B or A = B	A < B	1			11	17			40	65			11	17	ns

Notes

(1) All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

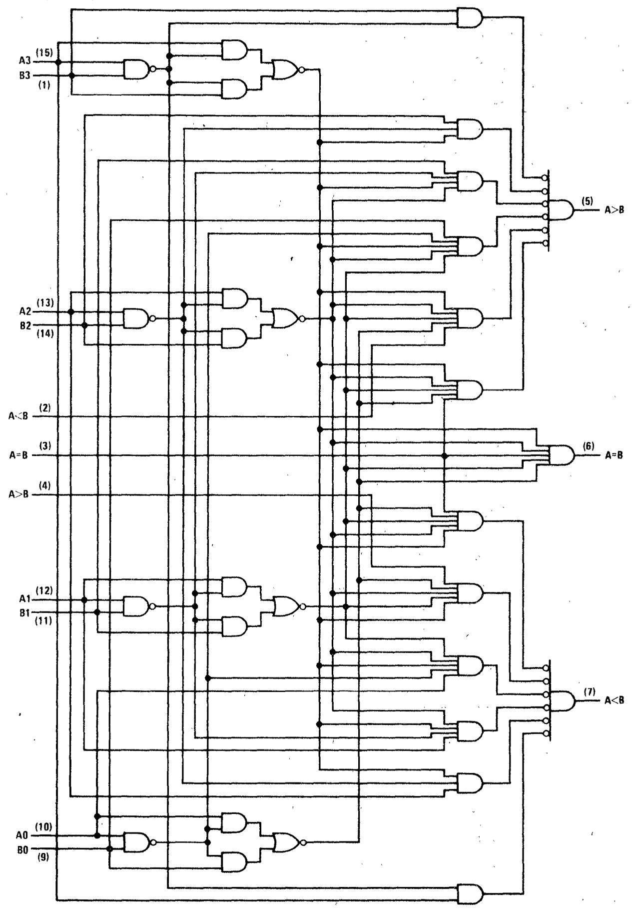
(3) With all outputs open, I_{CC} is measured for Condition A with all inputs at 4.5V, and for Condition B with all inputs grounded.

(4) I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5V.

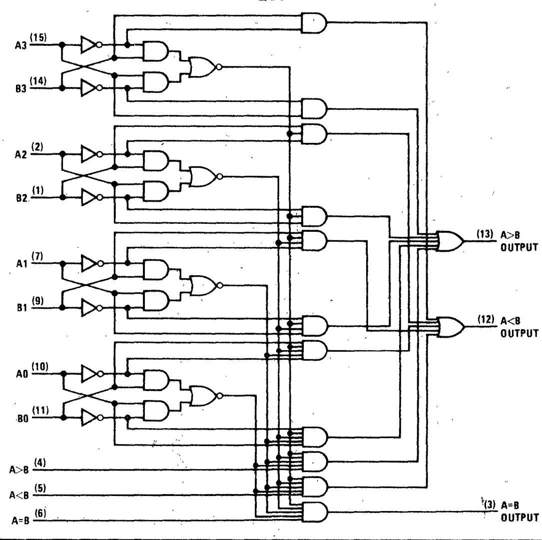
(5) The condition A = B applies to L85 values only. For DM5485/DM7485 and LS85 use the values for "All Other Inputs."

Logic Diagrams

85, LS85



L85



256-Bit Read Only Memories

General Description

These custom-programmed, 256-bit, read-only memories are organized as 32 words of eight bits each. Each 32-word memory array is addressed in straight 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the 32 address gates and cause all eight outputs to remain high (off). Data, as specified by the customer, are permanently programmed into the monolithic structure for the 256-bit locations. This organization is expandable to n-words of N-bit length.

The address of an eight-bit word is accomplished through the buffered, binary select inputs which are decoded by the 32, five-input address gates. When the memory-enable input is high, all 32 gate outputs are low, turning off the eight output buffers.

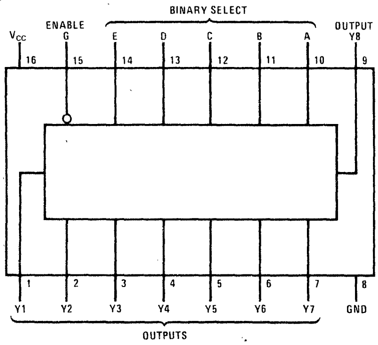
Data are programmed into the memory at the 32, eight-emitter transistors. The programming process involves connecting or not connecting each of the 256 emitters. If an emitter is connected, a low-level voltage is read out of that bit location when its decoding gate is addressed. If the emitter is not connected, a high-level voltage is read when addressed. Those decoding-gate output emitters which are used are connected to their respective bit lines to drive the eight output buffers. Since only one decoding gate is addressed at a time, only one of the 32 transistors can supply current to the output buffers at a time.

Input buffers lower the fan-in requirement to only one normalized DM54/74 load for all inputs including enable (G). The open-collector outputs are capable of sinking 12 milliamperes of current and may be wire-AND connected to increase the number of words available. An external pull-up resistor from each output to the supply line (V_{CC}) is required to define the high-level output voltage. Where multiple devices are used in a memory system, the enable input allows easy decoding of additional address bits.

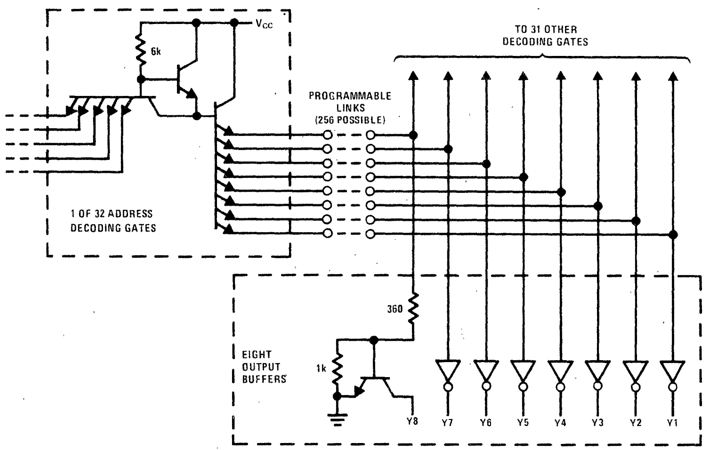
Features

- Typical access time: 20 ns
- Typical power dissipation: 240 mW
- Applications in computer subroutines
- Useful in display systems and readouts
- Memory organized as 32 words of 8 bits each
- Input clamping diodes simplify system design
- Open-collector outputs permit wire-AND capability

Connection and Schematic Diagrams



5488(J), (W); 7488(J), (N), (W)



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM54/74 88 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, V_{OH} = 5.5V			40	μA
I_{OL}	Low Level Output Current				12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 12 mA		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1	mA
I_{CCH}	Supply Current, All Outputs High	V_{CC} = Max(2)		37	65	mA
I_{CCL}	Supply Current, All Outputs Low	V_{CC} = Max(2)		48	80	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) All 32 words are addressed separately to ensure that the supply current does not exceed the stated maximum. The typical value shown is for the worst-case condition of all eight outputs driven low at one time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74 88 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Any	C_L = 30 pF, R_{L1} = 400Ω, R_{L2} = 600Ω		19	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable	Any			18	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Any			21	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Any			17	35	ns

Ordering Instructions

Programming instructions for the DM5488 or DM7488 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table of the requested part. This function table, showing output conditions for each of the 32 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the word specified and describes the levels at the eight outputs for that word. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

Supplementary Ordering Data

Submit the following information with the data cards:

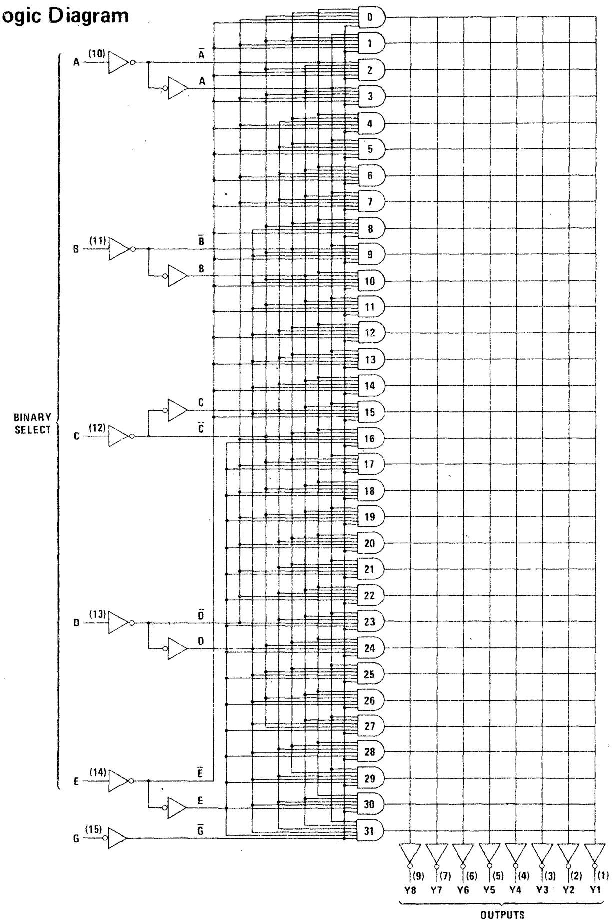
a. Customer's name and address
b. Customer's purchase order number
c. Customer's drawing number

Data Card Format

Column

Column	
1–2	Punch a right-justified integer representing the positive-logic binary input address (00–31) for the word described on the card.
3–4	Blank
5	Punch "H," "L," or "X" for output Y8. H = high-voltage-level output, L = low-voltage-level output, X = output irrelevant.
6–9	Blank
10	Punch "H," "L," or "X" for output Y7.
11–14	Blank
15	Punch "H," "L," or "X" for output Y6.
16–19	Blank
20	Punch "H," "L," or "X" for output Y5.
21–24	Blank
25	Punch "H," "L," or "X" for output Y4.
26–29	Blank
30	Punch "H," "L," or "X" for output Y3.
31–34	Blank
35	Punch "H," "L," or "X" for output Y2.
36–39	Blank
40	Punch "H," "L," or "X" for output Y1.
41–49	Blank
50–51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53–55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57–58	Punch the last two digits of the current year.
59	Blank
60–61	Punch "DM"
62–65	Punch the National Semiconductor part number 5488 or 7488.
66–70	Blank

Logic Diagram



Word Select Table

WORD	INPUTS				
	E	D	C	B	A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

H = High Level, L = Low Level

64-Bit Read/Write Memories

General Description

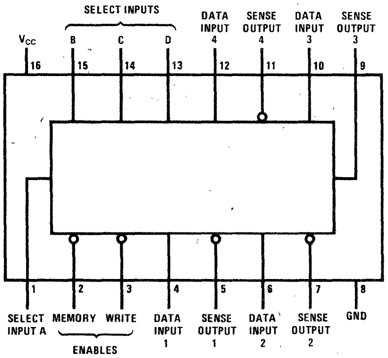
The DM5489/DM7489, DM54L89A/DM74L89A are fully decoded 64-bit RAMs organized as 16, 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

The "A" suffix on the low power versions is used to denote that full "tenth-power" technology has been employed in building this RAM.

Features

- For application as a "scratch pad" memory with nondestructive read-out
- Fully decoded memory organized as 16 words of four bits each
- Fast access time DM54/74—35 ns typical; DM54L/74L—110 ns
- Diode-clamped, buffered inputs
- Open-collector outputs provide wire-OR capability
- Typical power dissipation DM54/74—400 mW; DM54L/74L—75 mW
- Pin compatible with 3101, MM5501

Connection Diagram

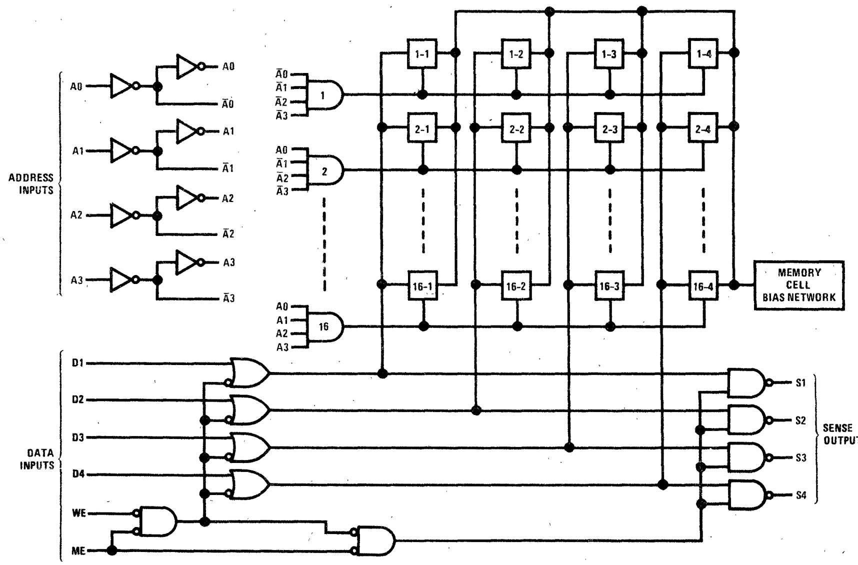


5489(J); 7489(J), (N); 54L89A/74L89A(J), (N), (W)

Truth Table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 89 MIN	TYP(1)	MAX	DM54L/74L L89A MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V	DM54			100			50	μA
		V_{IL} = Max, V_{OH} = 5.5V	DM74			20			50	μA
V_{OH}	High Level Output Voltage					5.5			5.5	V
I_{OL}	Low Level Output Current		DM54			12			2.0	mA
			DM74			12			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	DM54			0.4			0.3	V
		V_{IL} = Max, I_{OL} = Max	DM74			0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V						−0.18	mA
		V_{CC} = Max	V_I = 0.4V			−1.6				mA
I_{CC}	Supply Current	V_{CC} = Max(2)			80	120		15	19	mA
C_O	Off-State Output Capacitance	V_{CC} = 5V, V_O = 2.0V, f = 1 MHz			6			N/A		pF

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) I_{CC} is measured with all inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	DM54/74 89 MIN	TYP	MAX	CONDITIONS	DM54L/74L L89A MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Memory Enable	C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600Ω		23	35	C_L = 50 pF, R_L = 4 kΩ		64	90	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Memory Enable			23	35			33	60	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Select			34	50			90	150	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Select			35	50			78	150	ns
t_{SR}	Sense Recovery Time After Writing			35	50			110	165	ns
t_W	Width of Write-Enable Pulse		40				50			ns
t_{SETUP}	Setup Time, Data Input With Respect to Write Enable		0				0			ns
t_{SETUP}	Select Input Setup Time With Respect to Write Enable		0				0			ns
t_{HOLD}	Hold Time, Data Input With Respect to Write Enable		0				0			ns
t_{HOLD}	Select Input Hold Time after Writing		5				0			ns

MSI DM54/DM7490A,L90,LS90,92A,LS92,93A,L93,LS93

Decade, Divide by 12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A, L90, and LS90, divide-by-six for the 92A and LS92, and divide-by-eight for the 93A, L93, and LS93.

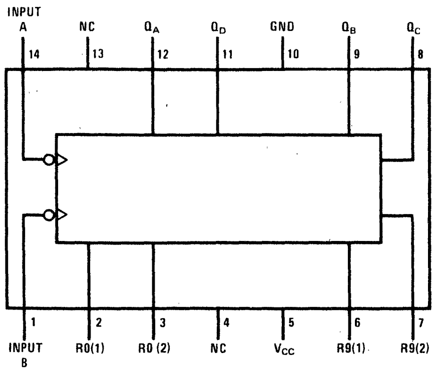
All of these counters have a gated zero reset and the 90A, L90, and LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A, L90, or LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

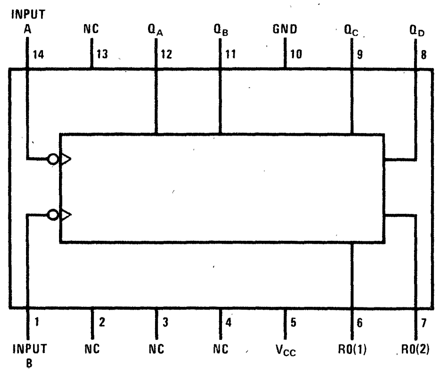
Features

TYPE	TYPICAL POWER DISSIPATION	COUNT FREQUENCY
90A	145 mW	42 MHz
L90	20 mW	11 MHz
LS90	45 mW	42 MHz
92A, 93A	130 mW	42 MHz
LS92, LS93	45 mW	42 MHz
L93	16 mW	15 MHz

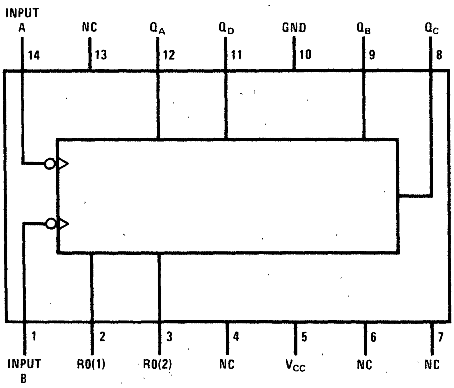
Connection Diagrams



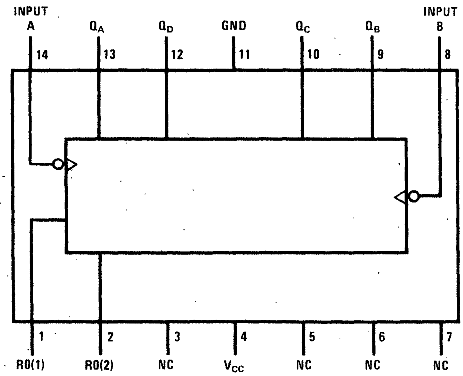
5490A/7490A(J), (N), (W);
54L90/74L90(J), (N), (W);
54LS90/74LS90(J), (N), (W)



5492A/7492A(J), (N), (W);
54LS92/74LS92(J), (N), (W)



5493A/7493A(J), (N), (W);
54LS93/74LS93(J), (N), (W)



54L93/74L93(J), (N), (W)

LS90, LS92, LS93 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS		DM54/74 90A, 92A, 93A MIN	TYP(1)	MAX	DM54L/74L L90, L93 MIN	TYP(1)	MAX	DM54LS/74LS LS90, LS92, LS93 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			0.7	V
				DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5		N/A					V
			V_{CC} = Min, I_I = −18 mA						N/A				−1.5	
I_{OH}	High Level Output Current						−800			−200			−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	DM54	2.4	3.4		2.4			2.5	3.4		V
				DM74	2.4	3.4		2.4			2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			2			4	mA
				DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max (3)	DM54		0.2	0.4		0.15	0.3		0.25	0.4	V
				DM74		0.2	0.4		0.2	0.4		0.35	0.5	
			I_{OL} = 4 mA	DM74								0.25	0.4	
I_I	Input Current at Maximum Input Voltage	Any Reset	V_{CC} = Min, V_I = 5.5V				1			0.1				mA
			V_{CC} = Min, V_I = 7V										0.1	
		A Input	V_{CC} = Min, V_I = 5.5V				1			0.2			0.4	
		B Input	V_{CC} = Min, V_I = 5.5V	L90						0.4				
				Others			1			0.2			0.8	
I_{IH}	High Level Input Current	Any Reset	V_{CC} = Max, V_I = 2.7V for LS, V_I = 2.4V for Others				40			10			20	μA
		A Input					80			20			120	
		B Input		93			80			20			40	
				Others			120			40			80	
I_{IL}	Low Level Input Current	Any Reset	V_{CC} = Max, V_I = 0.3V for L, V_I = 0.4V for Others				−1.6			−0.18			−0.4	mA
		A Input					−3.2			−0.36			−2.4	
		B Input		93			−3.2			−0.36			−1.6	
				Others			−4.8			−0.72			−3.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	DM54	−20		−57	−3	−9	−15	−30		−130	mA
				DM74	−18		−57	−3	−9	−15	−30		−130	
I_{CC}	Supply Current		V_{CC} = Max(4)	90A		29	42							mA
				Others		26	39			5.5		9	15	

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74									DM54L/74L						UNITS
					90A, LS90			92A, LS92			93A, LS93			L90			L93			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum Count Frequency	A	Q_A	C_L = 50 pF For L90 and L93 C_L = 15 pF For All Others R_L = 400Ω For 90A, 92A and 93A R_L = 2 kΩ For LS90, LS92 and LS93 R_L = 4 kΩ For L90 and L93	32	42		32	42		32	42		6	11		6	15		MHz
		B	Q_B		16			16			16									
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A	Q_A			10	16		10	16		10	16							ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12	18		12	18		12	18							
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A	Q_D			32	48		32	48		46	70		175	300		210	400	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					34	50		34	50		46	70		190	300		230	400	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	B	Q_B			10	16		10	16		10	16							ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	21		14	21		14	21							
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	B	Q_C			21	32		10	16		21	32							ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					23	35		14	21		23	35							
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	B	Q_D			21	32		21	32		34	51							ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					23	35		23	35		34	51							
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Set-to-0	Any			26	40		26	40		26	40							ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Set-to-9	Q_A, Q_D			20	30													ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Q_B, Q_C			26	40													
t_W	Pulse Width — A Input				15			15			15			90			90			ns
	Pulse Width — B Input				30			30			30			90			90			
	Pulse Width — Reset Input				15			15			15			200			200			
t_{SETUP}	Reset Inactive State Setup Time				25			25			25			200			200			ns

Notes

(1) All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) Q_A outputs are tested at I_{OL} = max plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

(4) I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Truth Tables

90A, L90, LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

90A, L90, LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

92A, LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

93A, L93, LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

90A, L90, LS90
RESET/COUNT TRUTH TABLE

RESET INPUTS				OUTPUT			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

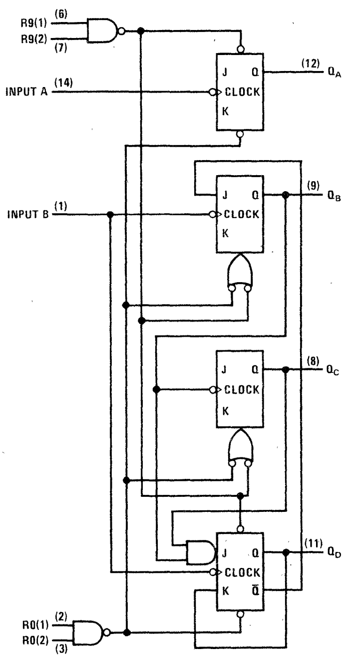
Notes:
(A) Output Q_A is connected to input B for BCD count.
(B) Output Q_D is connected to input A for bi-quinary count.
(C) Output Q_A is connected to input B.
(D) H = High Level, L = Low Level, X = Don't Care.

92A, LS92, 93A, L93, LS93
RESET/COUNT TRUTH TABLE

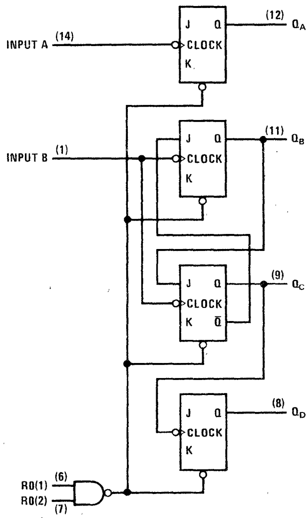
RESET INPUTS		OUTPUT			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Logic Diagrams

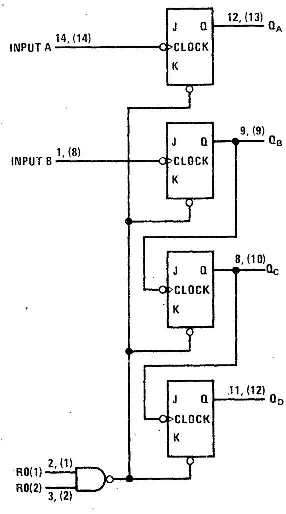
90A, L90, LS90



92A, LS92



93A, L93, LS93



Note: Numbers in parenthesis are for L93 only.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

8-Bit Serial Shift Registers

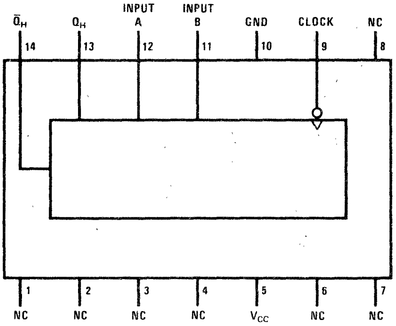
General Description

These serial-in, serial-out 8-bit shift registers are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift-register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

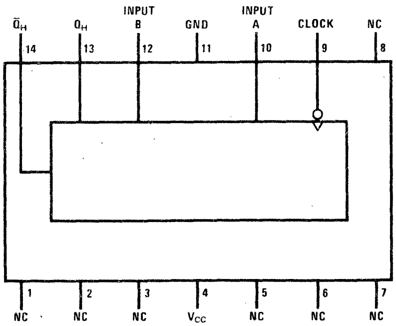
Features

TYPE	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
91A	22 MHz	175 mW
L91	8 MHz	17.5 mW

Connection Diagrams



5491A/7491A(J), (N);
54L91/74L91(J), (N)



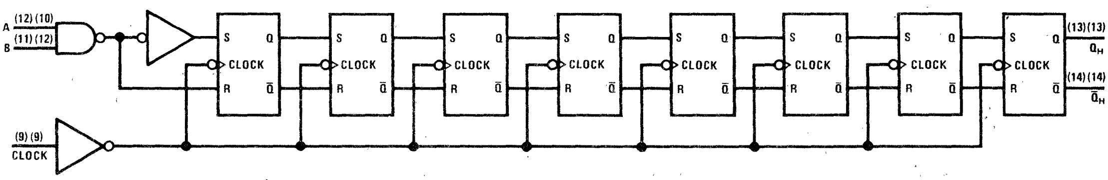
5491A/7491A(W);
54L91/74L91(W)

Truth Table

INPUTS AT t_n		OUTPUTS AT t_{n+8}	
A	B	Q_H	$\bar{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

H = High, L = Low,
X = Don't Care
t_n = Reference bit time, clock low,
t_{n+8} = Bit time after 8 low-to-high clock transitions.

Logic Diagram



Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54/74 91A MIN	TYP(1)	MAX	DM54L/74L L91 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
I_{OH}	High Level Output Current					−800			−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OH} = Max		2.4	3.5		2.4	2.8		V
I_{OL}	Low Level Output Current		DM54			16			2	mA
			DM74			16			3.6	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	DM54		0.22	0.4		0.15	0.3	V
		V_{IL} = Max, I_{OL} = Max	DM74		0.22	0.4		0.2	0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V						−0.18	mA
			V_I = 0.4V			−1.6				
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM54	−20		−57	−3	−8	−15	mA
			DM74	−18		−57	−3	−8	−15	
I_{CC}	Supply Current	V_{CC} = Max(3)	DM54		35	50		3.5	6.6	mA
			DM74		35	58		3.5	6.6	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM54/74 91A MIN	TYP	MAX	CONDITIONS	DM54L/74L L91 MIN	TYP	MAX	UNITS
f_{max}	Maximum Clock Frequency	C_L = 15 pF R_L = 400Ω	10	22		C_L = 50 pF R_L = 4 kΩ	4	8		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output			18	40			40	80	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			27	40			65	130	ns
$t_{W(CLOCK)}$	Width of Clock Input Pulse		25				120			ns
t_{SETUP}	Setup Time		25				120			ns
t_{HOLD}	Hold Time		0				0			ns

4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

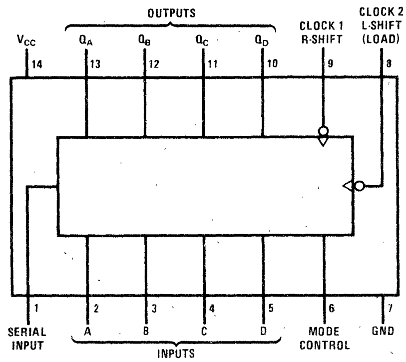
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

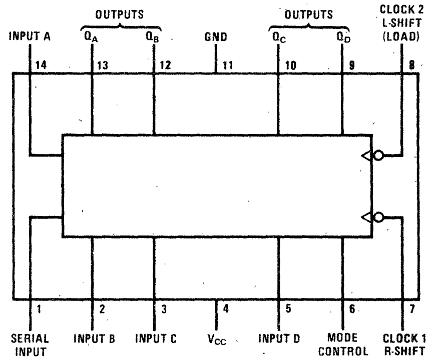
Features

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
95	36 MHz	250 mW
L95	14 MHz	24 mW
LS95B	36 MHz	65 mW

Connection Diagrams

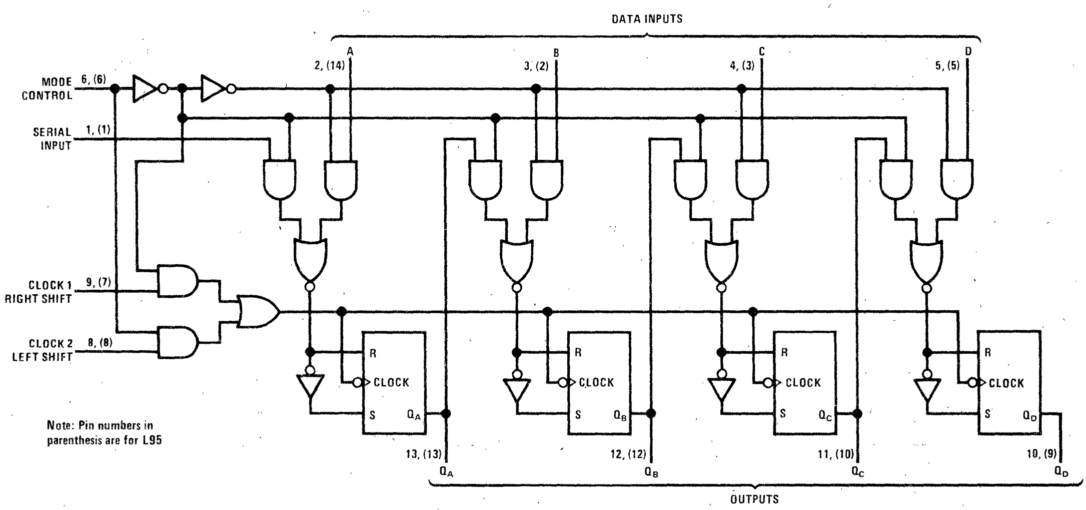


5495(J), (W); 7495(J), (N), (W); 54LS95B/74LS95B(J), (N), (W)



54L95/74L95(J), (N), (W)

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS			DM54/74 95			DM54L/74L L95			DM54LS/74LS LS95B			UNITS
						MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage					2			2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.8			0.7			0.7	V
					DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA				−1.5		N/A					V
				I_I = −18 mA						N/A				−1.5	
I_{OH}	High Level Output Current							−800			−200			−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V		DM54	2.4	3.4		2.4	3.1		2.5	3.4		V
			V_{IL} = Max, I_{OH} = Max		DM74	2.4	3.4		2.4	3.1		2.7	3.4		
I_{OL}	Low Level Output Current				DM54			16			2			4	mA
					DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min	I_{OL} = Max	DM54		0.2	0.4		0.13	0.3		0.25	0.4	V
			V_{IH} = 2V		DM74		0.2	0.4		0.2	0.4		0.35	0.5	
			V_{IL} = Max	I_{OL} = 4 mA	DM74								0.25	0.4	
I_I	Input Current at Maximum Input Voltage	Mode Control	V_{CC} = Max	V_I = 5.5V				1			0.2				mA
		Others						1			0.1				
		Clock Inputs		V_I = 7V										0.2	
		Others												0.1	
I_{IH}	High Level Input Current	Mode Control	V_{CC} = Max	V_I = 2.4V				80			20				μA
		Others						40			10				
		Clock Inputs		V_I = 2.7V										40	
		Others												20	
I_{IL}	Low Level Input Current	Mode Control	V_{CC} = Max	V_I = 0.3V							−0.36				mA
		Others									−0.18				
		Mode Control		V_I = 0.4V				−3.2						−0.4	
		Clocks						−1.6						−0.8	
		Others						−1.6						−0.4	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)			−18		−57	−3	−9	−15	−30		−130	mA
I_{CC}	Supply Current		V_{CC} = Max(3)				50	75		4.8	8		13	21	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5V; and a momentary 3V, then ground, applied to both clock inputs.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		DM54/74 95 CONDITIONS	MIN	TYP	MAX	DM54L/74L L95 CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS95B CONDITIONS	MIN	TYP	MAX	UNITS
f_{max}	Maximum Clock Frequency	$C_L = 15$ pF, $R_L = 400\Omega$	25	36		$C_L = 50$ pF, $R_L = 4$ kΩ	6	14		$C_L = 15$ pF, $R_L = 2$ kΩ	25	36		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock			25	35			42	90			18	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock			25	35			48	90			21	32	ns
$t_{W(CLOCK)}$	Width of Clock Pulse		15				90				25			ns
t_{SETUP}	Setup Time, High-Level Data		20	10			50				20			ns
t_{SETUP}	Setup Time, Low-Level Data		20	10			50				20			ns
t_{HOLD}	Hold Time, High-Level or Low-Level Data		0	−10			0				10			ns
$t_{ENABLE1}$	Time to Enable Clock 1		20				120				20			ns
$t_{ENABLE2}$	Time to Enable Clock 2		15				100				20			ns
$t_{INHIBIT1}$	Time to Inhibit Clock 1		10				0				20			ns
$t_{INHIBIT2}$	Time to Inhibit Clock 2		10				0				20			ns

Truth Table

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions)

↓= Transition from high to low level, ↑ = Transition from low to high level

a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

5-Bit Shift Registers

General Description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may also be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is low. Clearing is independent of the level of the clock input.

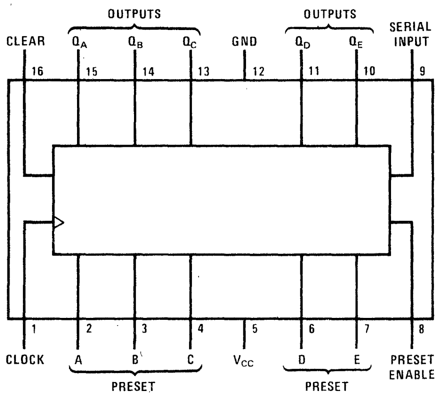
The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting is also independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

Features

- N-bit serial-to-parallel converter
- N-bit parallel-to-serial converter
- N-bit storage register

Connection Diagram



5496(J), (W); 7496(J), (N), (W);
54LS96/74LS96(J), (N), (W)

Truth Table

INPUTS									OUTPUTS				
CLEAR	PRESET ENABLE	PRESET					CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
		A	B	C	D	E							
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)
X = don't care (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc., respectively before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively before the most recent ↑ transition of the clock.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS			DM54/74 96 MIN	DM54/74 96 TYP(1)	DM54/74 96 MAX	DM54LS/74LS LS96 MIN	DM54LS/74LS LS96 TYP(1)	DM54LS/74LS LS96 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7	V
				DM74			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5				V
			I_I = −18 mA							−1.5	
I_{OH}	High Level Output Current						−400			−400	µA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = −400µA		DM54	2.4	3.4		2.5	3.5		V
				DM74	2.4	3.4		2.7	3.5		
I_{OL}	Low Level Output Current			DM54			16			4	mA
				DM74			16			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.25	0.4	V
				DM74		0.2	0.4		0.35	0.5	
			I_{OL} = 4 mA	DM74					0.25	0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1				mA
			V_I = 7V							0.1	
I_{IH}	High Level Input Current — Any Input Except Preset Enable	V_{CC} = Max	V_I = 2.4V				40				µA
			V_I = 2.7V							20	
	Preset Enable		V_I = 2.4V				200				
			V_I = 2.7V							20	
I_{IL}	Low Level Input Current — Any Input Except Preset Enable	V_{CC} = Max, V_I = 0.4V					−1.6			−0.4	mA
	Preset Enable						−8			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−57	−30		−130	mA
				DM74	−18		−57	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max(3)		DM54		48	68		12	20	mA
				DM74		48	79		12	20	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

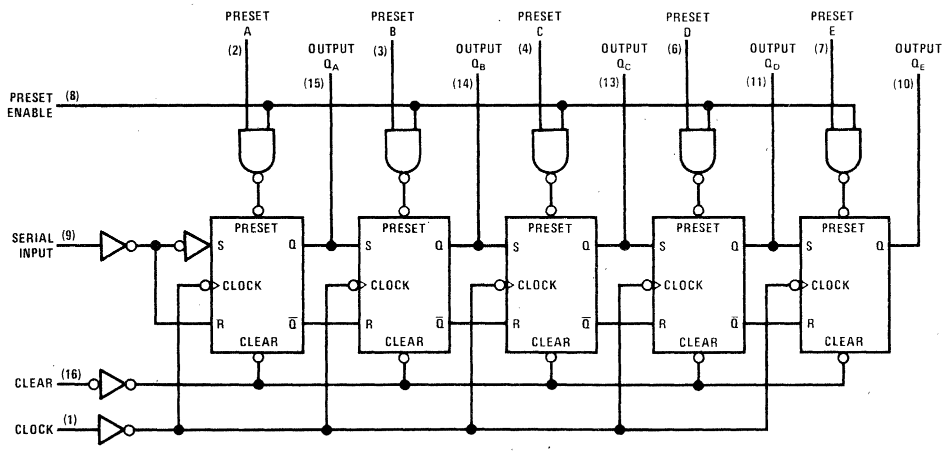
(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

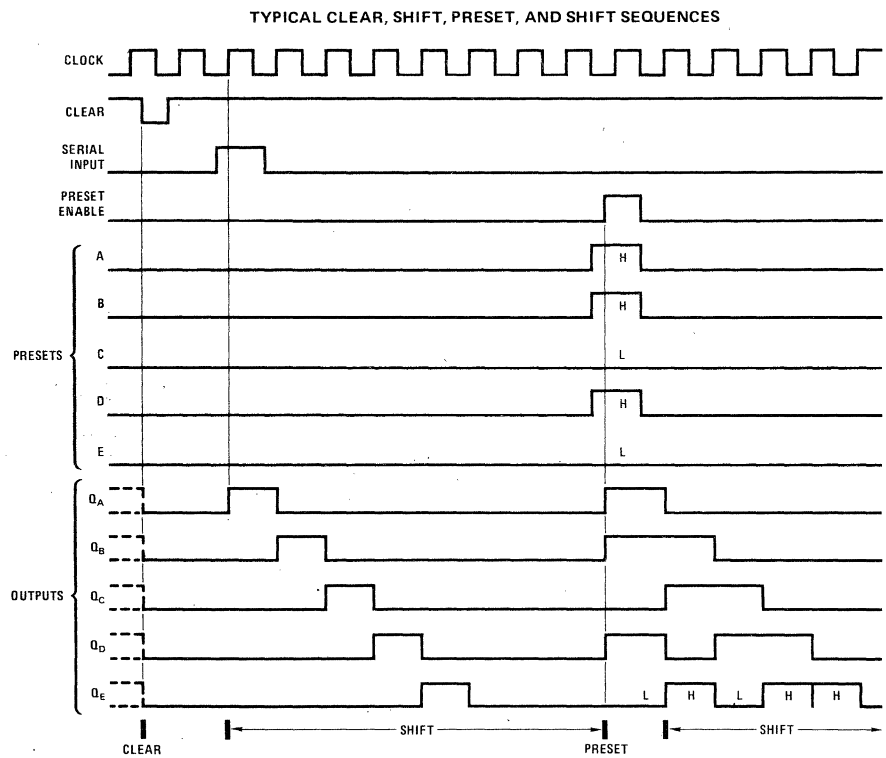
Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	DM54/74 96 CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS96 CONDITIONS	MIN	TYP	MAX	UNITS
f_{max}	Maximum Shift Frequency		10				10			MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock	C_L = 15 pF, R_L = 400Ω		25	40	C_L = 15 pF, R_L = 2 kΩ		25	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock			25	40			25	40	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Preset or Preset Enable			25	35			28	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clear				55				55	ns
$t_{W(CLOCK)}$	Width of Clock Input Pulse		35				35			ns
t_W	Width of Preset and Clear Input Pulse		30				30			ns
t_{SETUP}	Serial Input Setup Time		30				30			ns
t_{HOLD}	Serial Input Hold Time		0				0			ns

Logic Diagram



Timing Diagram



4-Bit Storage Registers

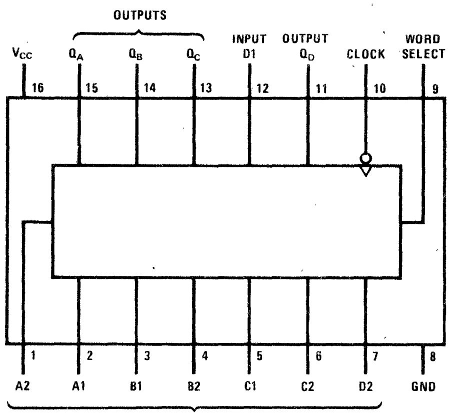
General Description

These data selectors/storage registers are composed of four S-R master-slave flip-flops, four AND-OR INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high level input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

Typical clock frequency is 12 MHz.

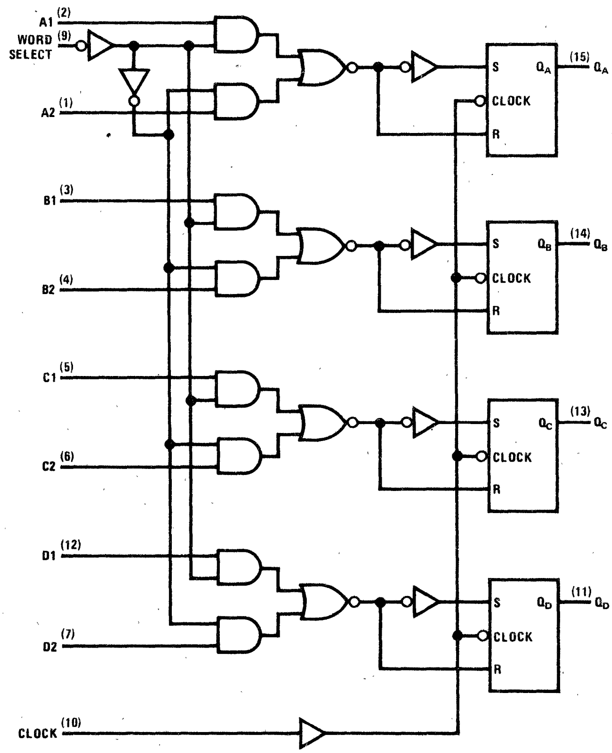
Connection Diagram



Word select low for word 1, word select high for word 2, see description

54L98/74L98(J), (N), (W)

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54L/74L L98 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.7	V
I_{OH}	High Level Output Current					−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.7V, I_{OH} = −200μA		2.4			V
I_{OL}	Low Level Output Current		DM54			2	mA
			DM74			3.6	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.7V, I_{OL} = Max	DM54		0.15	0.3	V
			DM74			0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max		−3	−9	−15	mA
I_{CC}	Supply Current	V_{CC} = Max(2)			6	8	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER		CONDITIONS	DM54L/74L L98 MIN	TYP	MAX	UNITS
f_{max}	Maximum Clock Frequency		C_L = 50 pF, R_L = 4 kΩ	6	12		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock				40	80	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock				65	100	ns
$t_{W(CLOCK)}$	Width of Clock Pulse			100	65		ns
$t_{SETUP(H)}$	Setup Time for High-Level Data	A, B, C, or D		100			ns
		Word Select		150			
$t_{SETUP(L)}$	Setup Time for Low-Level Data	A, B, C, or D		120			ns
		Word Select		100			

Dual Voltage Controlled Oscillators

General Description

The DM54LS124/DM74LS124 features two fully independent voltage-controlled oscillators (VCO's) in a single monolithic chip. The output frequency of each is established by a single external component, either a capacitor or a crystal, in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. An enable input is provided that can be used to start or stop the output pulses when it is low or high, respectively. The internal oscillator runs continuously, even while the output is disabled. A pulse synchronizer ensures that the first output pulse is neither clipped nor extended. Duty cycle of the output pulses is fixed at approximately 50 percent.

The highly stable oscillator can be set to operate at any frequency between 0.12 Hz and 50 MHz typically. The output frequency can be approximated as follows:

$$f_O = \frac{500}{C_{EXT}}$$

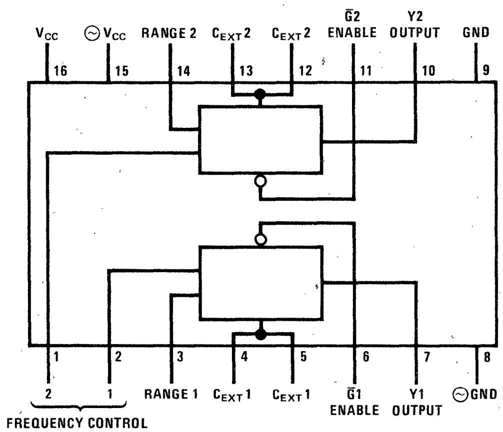
where: f_O = output frequency in MHz
C_{EXT} = external capacitance in pF

The enable input and the buffered output operate at standard Schottky-clamped TTL levels. The enable input is one standard load in each series. Although these devices can operate from a single 5-volt supply, separate supply-voltage and ground pins are provided for the digital logic and for the oscillator/range control circuits so that effective isolation can be accomplished in the system.

Features

- Two fully independent VCO's in a 16-pin package
- Output frequency set by single external component:
  Crystal for high-stability fixed-frequency operation
  Capacitor for fixed- or variable-frequency operation
- Separate supply voltage pins for isolation of inputs and oscillators from logic circuitry
- Stable operation over specified temperature and/or supply voltage ranges

Connection Diagram



Note: While the enable input is low, the output is enabled. While the enable input is high, the output is high.

54LS124/74LS124(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS		DM54 LS124 MIN	DM54 LS124 TYP(1)	DM54 LS124 MAX	DM74 LS124 MIN	DM74 LS124 TYP(1)	DM74 LS124 MAX	UNITS
V_{IH}	High Level Input Voltage at Enable				2			2			V
V_{IL}	Low Level Input Voltage at Enable						0.7			0.8	V
V_I	Input Clamp Voltage at Enable		V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current						−1.2			−1.2	mA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, I_{OH} = −1.2 mA		2.5	3.4		2.7	3.4		V
I_{OL}	Low Level Output Current						12			24	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{ENABLE} = V_{IL} Pins 4 and 13 = V_{CC}(Min)−2V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	V
I_I	Input Current	Freq Control or range	V_{CC} = Max	V_I = 5V		50	250		50	250	μA
				V_I = 1V		10	50		10	50	μA
I_I	Input Current at Maximum Input Voltage	Enable	V_{CC} = Max, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	Enable	V_{CC} = Max, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	Enable	V_{CC} = Max, V_I = 0.5V				−0.4			−0.4	mA
I_{OS}	Short Circuit Output Current		V_{CC} = Max, V_{ENABLE} = 4.5V(2)		−30		−150	−30		−150	mA
I_{CC}	Supply Current, Total into Pins 15 and 16		V_{CC} = Max(3)			22	37		22	37	mA
V_I	Input Voltage at Frequency Control or Range Input				0		5	0		5	V

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

(3) I_{CC} is measured with the outputs disabled and open.

Switching Characteristics V_{CC} = 5V, R_L = 667Ω, C_L = 45 pF, T_A = 25°C

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_o	Output Frequency	C_{EXT} = 2 pF	$V_{I(FREQ)}$ = 5V, $V_{I(RNG)}$ = 0V	35	50		MHz
			$V_{I(FREQ)}$ = 0V, $V_{I(RNG)}$ = 5V	11	20		MHz
	Output Duty Cycle	C_{EXT} = 8.3 pF to 500μF			50%		
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Enable	$f_o \geq 1$ Hz			30+(4)		ns

Notes

(4) The delay will typically be 30 ns plus up to one half the period of one cycle (i.e. 30 ns to 30 ns + 5 x $10^8/f_{o(Hz)}$) depending upon the timing of the enable pulse with respect to the signal generated by the internal oscillator.

Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 and S138 decode one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 and S139 comprise two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

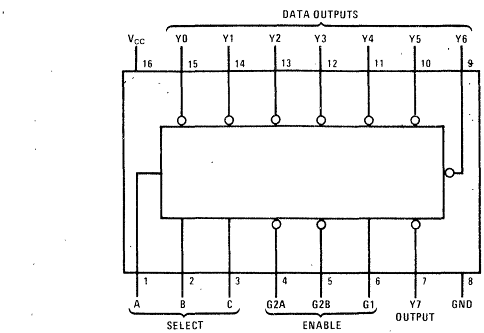
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

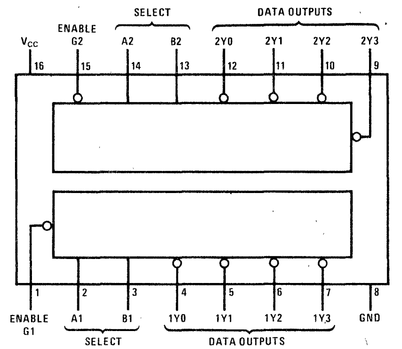
- Designed specifically for high-speed:
  - Memory decoders
  - Data transmission systems
- S138 and LS138 3-to-8-line decoders incorporate 3 enable inputs to simplify cascading and/or data reception
- S139 and LS139 contain two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance

TYPE	TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC)	TYPICAL POWER DISSIPATION
LS138	21 ns	32 mW
S138	8 ns	245 mW
LS139	21 ns	34 mW
S139	7.5 ns	300 mW

Connection and Logic Diagrams

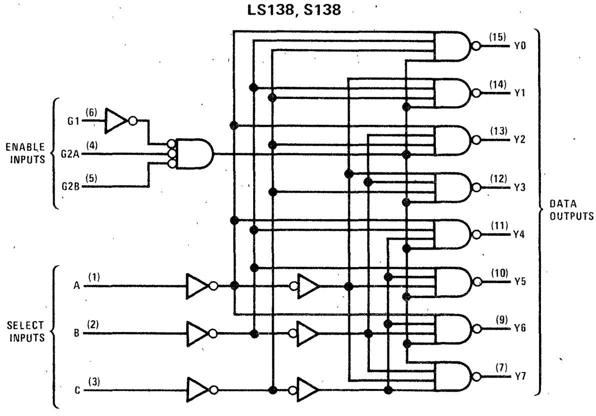


54LS138/74LS138(J), (N), (W); 74S138(N)

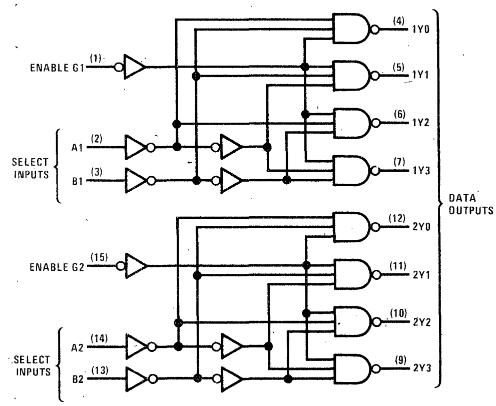


54LS139/74LS139(J), (N), (W); 74S139(N)

LS138, S138



LS139, S139



To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS			DM54LS/74LS LS138, LS139			DM74S S138, S139			UNITS
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.7			N/A	V
				DM74			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5			−1.2	V
I_{OH}	High Level Output Current						−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OH} = Max		DM54	2.5	3.4		N/A			V
				DM74	2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			4			N/A	mA
				DM74			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max	I_{OL} = Max	DM54		0.25	0.4			N/A	V
				DM74		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74			0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V							1	mA
			V_I = 7V				0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.7V				20			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−0.36				mA
			V_I = 0.5V							−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−30		−130			N/A	mA
				DM74	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max Outputs Enabled and Open		LS138, S138		6.3	10		49	74	mA
				LS139, S139		6.8	11		60	90	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	CONDITIONS	DM54LS/74LS LS138 MIN	DM54LS/74LS LS138 TYP	DM54LS/74LS LS138 MAX	DM54LS/74LS LS139 MIN	DM54LS/74LS LS139 TYP	DM54LS/74LS LS139 MAX	CONDITIONS	DM74S S138 MIN	DM74S S138 TYP	DM74S S138 MAX	DM74S S139 MIN	DM74S S139 TYP	DM74S S139 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Binary Select	Any	2	$C_L = 15$ pF, $R_L = 2\,k\Omega$		13	20		13	20	$C_L = 15$ pF, $R_L = 280\Omega$		4.5	7		5	7.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Binary Select	Any	2			27	41		22	33			7	10.5		6.5	10	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Binary Select	Any	3			18	27		18	29			7.5	12		7	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Binary Select	Any	3			26	39		25	38			8	12		8	12	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Any	2			12	18		16	24			5	8		5	8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable	Any	2			21	32		21	32			7	11		6.5	10	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Any	3			17	26			N/A			7	11			N/A	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable	Any	3			25	38			N/A			7	11			N/A	ns

Truth Tables

LS138, S138

INPUTS ENABLE G1	INPUTS ENABLE G2*	INPUTS SELECT C	INPUTS SELECT B	INPUTS SELECT A	OUTPUTS Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = High level, L = low level, X = don't care

LS139, S139

INPUTS ENABLE G	INPUTS SELECT B	INPUTS SELECT A	OUTPUTS Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Priority Encoders

General Description

These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. The DM54147 and DM74147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All inputs are buffered to represent one normalized Series 54/74 load. The DM54148 and DM74148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

Features

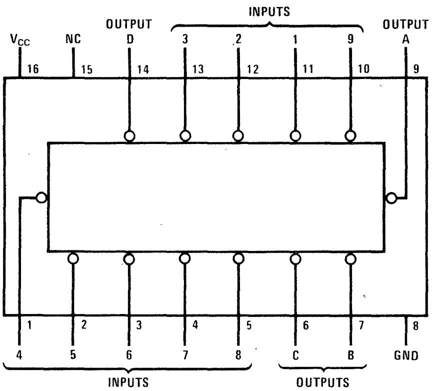
DM54147, DM74147

- Encodes 10-line decimal to 4-line BCD
- Applications include:
  - Keyboard encoding
  - Range selection
- Typical data delay 10 ns
- Typical power dissipation 225 mW

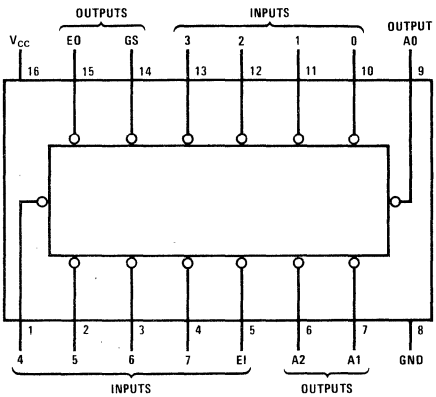
DM54148, DM74148

- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators
- Typical data delay 10 ns
- Typical power dissipation 190 mW

Connection Diagrams



54147(J), (W); 74147(J), (N), (W)



54148(J), (W); 74148(J), (N), (W)

Truth Tables

54147/74147

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

54148/74148

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High Logic Level, L = Low Logic Level, X = Don't Care

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS		DM54/74 147 MIN	147 TYP(1)	147 MAX	148 MIN	148 TYP(1)	148 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current						−800			−800	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA		2.4			2.4			V
I_{OL}	Low Level Output Current						16			16	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	0 Input	V_{CC} = Max, V_I = 2.4V				N/A			40	μA
		Others					40			80	
I_{IL}	Low Level Input Current	0 Input	V_{CC} = Max, V_I = 0.4V				N/A			−1.6	mA
		Others					−1.6			−3.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		−35		−85	−35		−85	mA
I_{CC}	Supply Current		V_{CC} = Max (3)	Condition 1		50	70		40	60	mA
				Condition 2		42	62		35	55	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

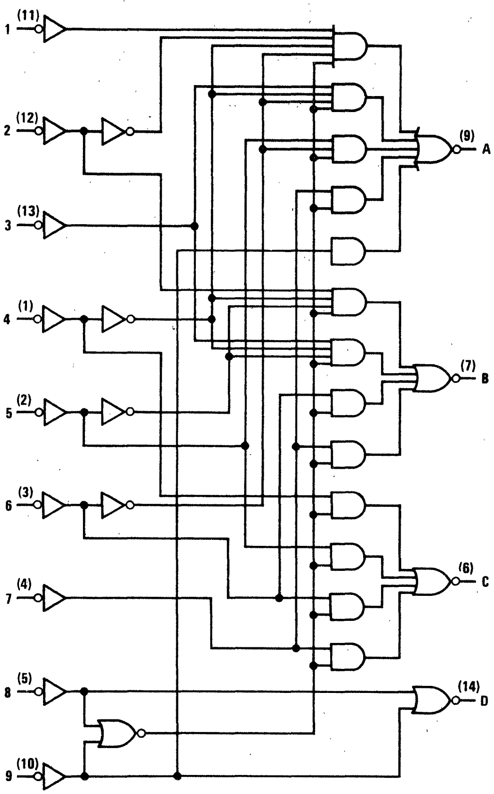
(3) For DM54147/DM74147, I_{CC} (condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open. For DM54148/DM74148, I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

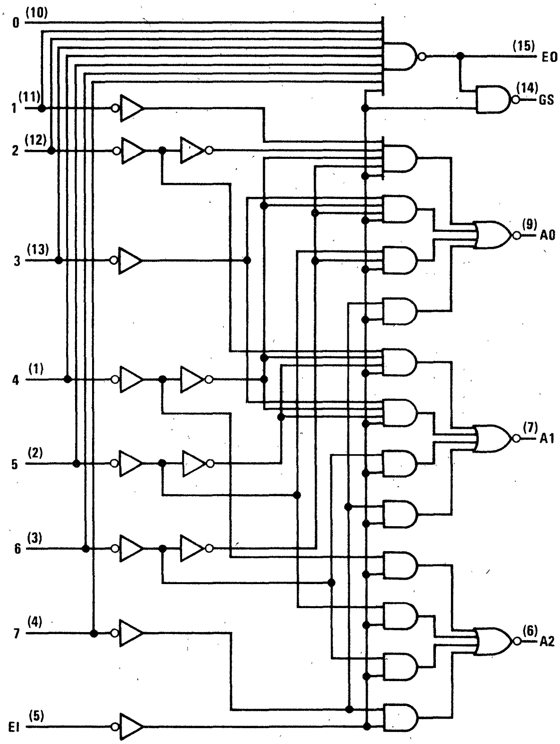
PARAMETER		FROM (INPUT)	TO (OUTPUT)	WAVEFORM	CONDITIONS	DM54/74 147 MIN	DM54/74 147 TYP	DM54/74 147 MAX	DM54/74 148 MIN	DM54/74 148 TYP	DM54/74 148 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	0 thru 9	A, B, C, D	In-Phase Output	$C_L = 15$ pF, $R_L = 400\Omega$		9	14		10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	0 thru 9	A, B, C, D	In-Phase Output			7	11		9	14	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	0 thru 9	A, B, C, D	Out-of-Phase Output			13	19		13	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	0 thru 9	A, B, C, D	Out-of-Phase Output			12	19		12	19	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	0 thru 7	EO	Out-of-Phase Output			N/A			6	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	0 thru 7	EO	Out-of-Phase Output			N/A			14	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	0 thru 7	GS	In-Phase Output			N/A			18	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	0 thru 7	GS	In-Phase Output			N/A			14	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	EI	A0, A1, or A2	In-Phase Output			N/A			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	EI	A0, A1, or A2	In-Phase Output			N/A			10	15	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	EI	GS	In-Phase Output			N/A			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	EI	GS	In-Phase Output			N/A			10	15	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	EI	EO	In-Phase Output			N/A			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	EI	EO	In-Phase Output			N/A			17	30	ns

Logic Diagrams

147



148



Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A, LS151, and S151 select one-of-eight data sources. The 150, 151A, LS151, and S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

The 151A, LS151, and S151 feature complementary W and Y outputs whereas the 150 has an inverted (W) output only.

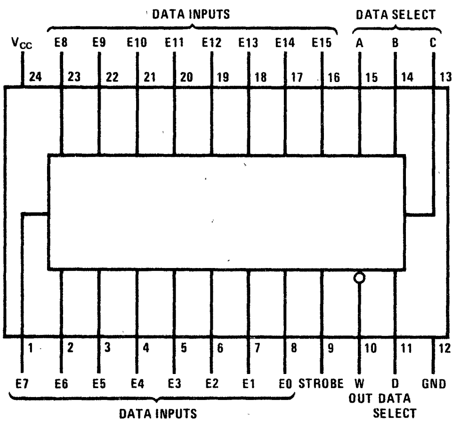
The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

Features

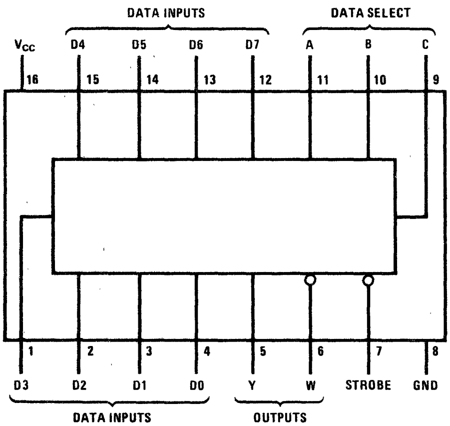
- 150 selects one-of-sixteen data lines
- Others select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
150	11 ns	200 mW
151A	9 ns	135 mW
LS151	12.5 ns	30 mW
S151	4.5 ns	225 mW

Connection Diagrams



54150(J), (F); 74150(J), (N), (F)



54151A(J), (W); 74151A(J), (N), (W); 54LS151/74LS151(J), (N), (W); 74S151(N)

Truth Tables

54150/74150

INPUTS					OUTPUT
SELECT				STROBE	W
D	C	B	A	S	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

54151A/74151A, 54LS151/74LS151, 74S151

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input

D0, D1 . . . D7 = the level of the respective D input

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS			DM54/74 150, 151A MIN	DM54/74 150, 151A TYP(1)	DM54/74 150, 151A MAX	DM54/74 LS151 MIN	DM54/74 LS151 TYP(1)	DM54/74 LS151 MAX	DM74S S151 MIN	DM74S S151 TYP(1)	DM74S S151 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			N/A	V
				DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5							V
			I_I = −18 mA							−1.5			−1.2	
I_{OH}	High Level Output Current						−800			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		DM54	2.4			2.5	3.4		N/A			V
				DM74	2.4			2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			4			N/A	mA
				DM74			16			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = Max	DM54			0.4		0.25	0.4			N/A	V
				DM74			0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74						0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1						1	mA
			V_I = 7V							0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−1.6			−0.4				mA
			V_I = 0.5V										−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−55	−30		−130			N/A	mA
				DM74	−18		−55	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max(3)		150		40	68							mA
				151A		27	48							
				Others					6	10		45	70	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS or DM74S duration of short circuit should not exceed one second.

(3) I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

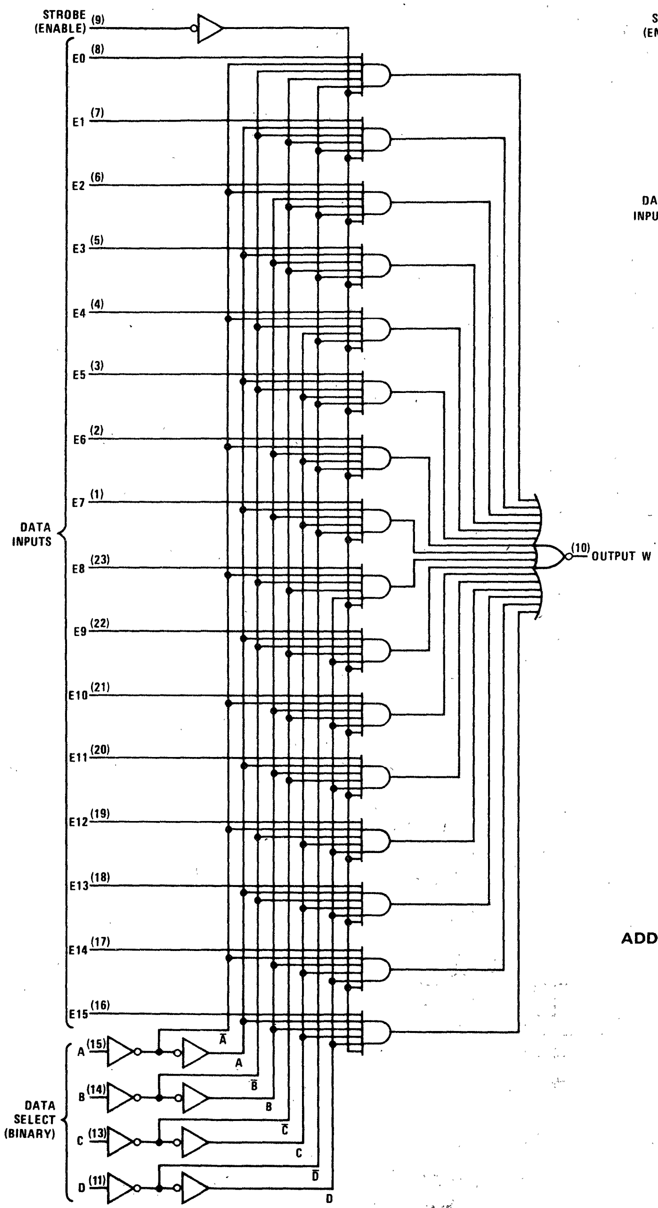
(4) National Semiconductor temporarily reserves the right to ship DM54LS/DM74LS151 devices which have a minimum I_{OS} = 5.0 mA.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

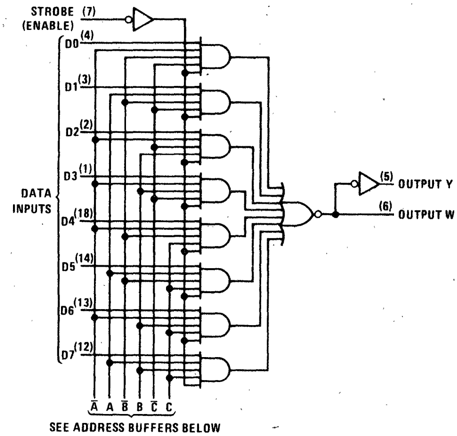
	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74						CONDITIONS	DM54LS/74LS			CONDITIONS	DM74S			UNITS
					150			151A				LS151				S151			
					MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX		MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select (4 levels)	Y	$C_L = 15$ pF $R_L = 400\Omega$		N/A			23	38	$C_L = 15$ pF $R_L = 2$ kΩ		27	43	$C_L = 15$ pF $R_L = 280\Omega$		12	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select (4 levels)	Y			N/A			23	30			18	30			12	18	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select (3 levels)	W			21	35		16	26			14	23			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select (3 levels)	W			22	33		16	30			20	32			9	13.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	Y			N/A			25	33			26	42			11	16.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	Y			N/A			19	30			20	32			12	18	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	W			15.5	24		11	21			15	24			9	13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	W			21	30		17	25			18	30			8.5	12	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	D0 thru D7	Y			N/A			17	24			20	32			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	D0 thru D7	Y			N/A			18	24			16	26			8	12	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	E0 thru E15 or D0 thru D7	W			13	20		10	14			13	21			4.5	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	E0 thru E15 or D0 thru D7	W			8.5	14		8	14			12	20			4.5	7	ns

Logic Diagrams

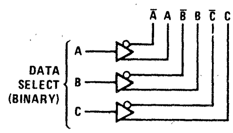
150



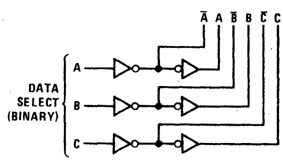
151A, S151



ADDRESS BUFFERS FOR 54151A/74151A



ADDRESS BUFFERS FOR 54LS151/74LS151, 74S151



Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

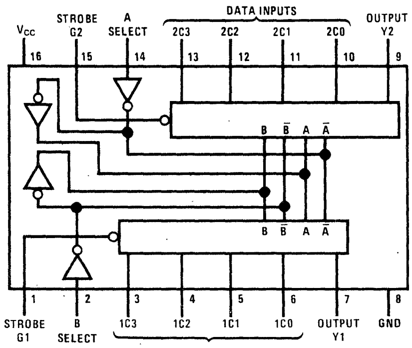
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIMES FROM DATA	FROM STROBE	FROM SELECT	TYPICAL POWER DISSIPATION
153	11 ns	18 ns	20 ns	170 mW
LS153	14 ns	19 ns	22 ns	31 mW
S153	6 ns	9.5 ns	12 ns	225 mW

Connection Diagram



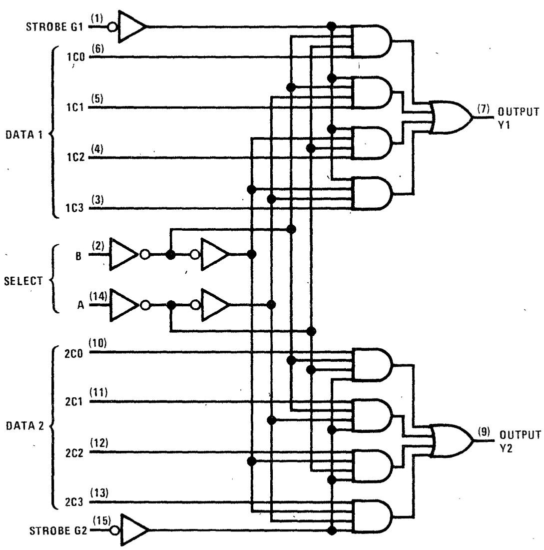
54153(J), (W); 74153(J), (N), (W); 54LS153/74LS153(J), (N), (W); 74S153(N)

Truth Table

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS			DM54/74 153 MIN	DM54/74 153 TYP(1)	DM54/74 153 MAX	DM54LS/74LS LS153 MIN	DM54LS/74LS LS153 TYP(1)	DM54LS/74LS LS153 MAX	DM74S S153 MIN	DM74S S153 TYP(1)	DM74S S153 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			N/A	V
				DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	$I_I = -12$ mA				−1.5							V
			$I_I = -18$ mA							−1.5			−1.2	
I_{OH}	High Level Output Current						−800			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V		DM54	2.4	3.2		2.5	3.4		N/A			V
		V_{IL} = Max, I_{OH} = Max		DM74	2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			4			N/A	mA
				DM74			16			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = Max	DM54		0.2	0.4		0.25	0.4			N/A	V
		V_{IH} = 2V		DM74		0.2	0.4		0.35	0.5			0.5	
		V_{IL} = Max	I_{OL} = 4 mA	DM74LS						0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1						1	mA
			V_I = 7V							0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−1.6			−0.36				mA
			V_I = 0.5V										−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−55	−30		−130			N/A	mA
				DM74	−18		−57	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max(3)		DM54		34	52		6.2	10			N/A	mA
				DM74		34	60		6.2	10		45	70	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS or DM74S duration of short circuit should not exceed one second.

(3) I_{CCL} is measured with the outputs open and all inputs grounded.

(4) National Semiconductor temporarily reserves the right to ship DM54LS/DM74LS153 devices which have a minimum I_{OS} = 5.0 mA.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	DM54/74 153 CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS153 CONDITIONS	MIN	TYP	MAX	DM74S S153 CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Y	$C_L = 30$ pF, $R_L = 400\Omega$		11	18	$C_L = 15$ pF, $R_L = 2$ kΩ		10	15	$C_L = 15$ pF, $R_L = 280\Omega$		6	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Y			10	23			17	26			6	9	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Y			20	34			19	29			11.5	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Y			20	34			25	38			12	18	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	Y			19	30			16	24			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	Y			17	23			21	32			9	13.5	ns

4-Line to 16-Line Decoders/Demultiplexers

General Description

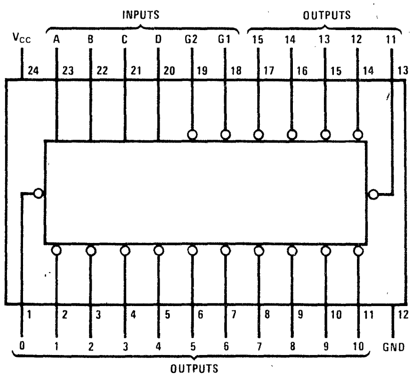
Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

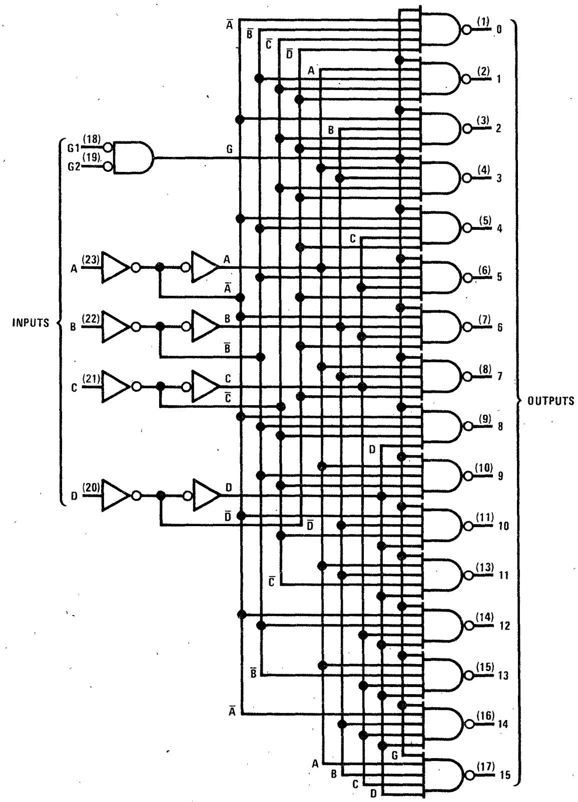
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs

TYPE	TYPICAL PROPAGATION DELAY 3 LEVELS OF LOGIC	TYPICAL PROPAGATION DELAY STROBE	TYPICAL POWER DISSIPATION
154	19 ns	18 ns	170 mW
L154A	55 ns	45 ns	24 mW
LS154	23 ns	19 ns	45 mW

Connection and Logic Diagrams



54154(J), (F); 74154(J), (N), (F); 54L154A/74L154A(J), (N), (F); 54LS154/74LS154(J), (N), (F)



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54/74 154			DM54L/74L L154A			DM54LS/74LS LS154(4)			UNITS
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7			0.7	V
			DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA			−1.5			N/A				V
			I_I = −18 mA									−1.5	
I_{OH}	High Level Output Current					−800			−200			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	DM54	2.4	3.4		2.4	2.8		2.5	3.5		V
		V_{IL} = Max, I_{OH} = Max	DM74	2.4	3.4		2.4	2.8		2.7	3.5		
I_{OL}	Low Level Output Current		DM54			16			2			4	mA
			DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	DM54		0.25	0.4		0.15	0.3		0.25	0.4	V
		V_{IL} = Max, I_{OL} = Max	DM74		0.25	0.4		0.20	0.4		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V			1			0.1				mA
			V_I = 7V									0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V			40			10				μA
			V_I = 2.7V									20	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V						−0.18				mA
			V_I = 0.4V			−1.6						−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM54	−20		−55	−3	−9	−15	−30		−130	mA
			DM74	−18		−57	−3	−9	−15	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max(3)	DM54		34	49		4.8	6.0		9	14	mA
			DM74		34	56		4.8	6.0		9	14	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CC} is measured with all inputs grounded and all outputs open.

(4) Tentative data.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		DM54/74				DM54L/74L				DM54LS/74LS				UNITS
		154				L154A				LS154(4)				
		CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output, From A, B, C, or D Inputs Through 3 Levels of Logic	$C_L = 15\ pF$, $R_L = 400\Omega$		18	36	$C_L = 50\ pF$, $R_L = 4\ k\Omega$		35	70	$C_L = 15\ pF$, $R_L = 2\ k\Omega$		24	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output, From A, B, C, or D Inputs Through 3 Levels of Logic	$C_L = 15\ pF$, $R_L = 400\Omega$		21	33	$C_L = 50\ pF$, $R_L = 4\ k\Omega$		75	150	$C_L = 15\ pF$, $R_L = 2\ k\Omega$		22	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output, From Either Strobe Input	$C_L = 15\ pF$, $R_L = 400\Omega$		17	30	$C_L = 50\ pF$, $R_L = 4\ k\Omega$		35	70	$C_L = 15\ pF$, $R_L = 2\ k\Omega$		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output, From Either Strobe Input	$C_L = 15\ pF$, $R_L = 400\Omega$		18	27	$C_L = 50\ pF$, $R_L = 4\ k\Omega$		55	110	$C_L = 15\ pF$, $R_L = 2\ k\Omega$		18	27	ns

Truth Table

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Dual 2-Line to 4-Line Decoders/Demultiplexers

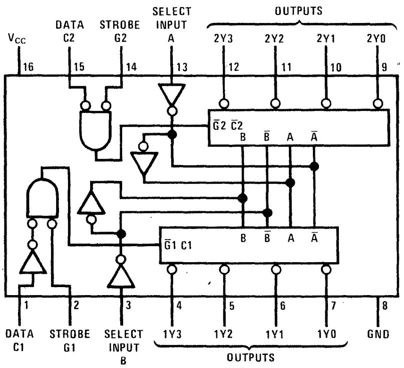
General Description

These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

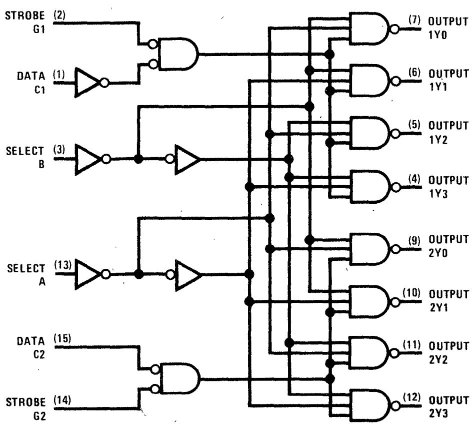
- Applications:
  - Dual 2-to-4-line decoder
  - Dual 1-to-4-line demultiplexer
  - 3-to-8-line decoder
  - 1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design
- Choice of outputs:
  - Totem-pole (155, LS155)
  - Open-collector (156, LS156)

Connection Diagram



54155(J), (W); 74155(J), (N), (W);
54LS155/74LS155(J), (N), (W);
54156(J), (W); 74156(J), (N), (W);
54LS156/74LS156(J), (N), (W)

Logic Diagram



Truth Tables

2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	1Y0	1Y1	1Y2	1Y3
B	A	G1	C1				
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	2Y0	2Y1	2Y2	2Y3
B	A	G2	C2				
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE-TO-8-LINE DECODER OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs C1 and C2 connected together
‡G = inputs G1 and G2 connected together
H = high level, L = low level, X = don't care

LS155, LS156 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 155 MIN	155 TYP(1)	155 MAX	156 MIN	156 TYP(1)	156 MAX	DM54LS/74LS LS155 MIN	LS155 TYP(1)	LS155 MAX	LS156 MIN	LS156 TYP(1)	LS156 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.8			0.7			0.7	V
			DM74			0.8			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA			−1.5			−1.5							V
			I_I = −18 mA									−1.5			−1.5	
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, V_{OH} = 5.5V							250						100	µA
						−800						−400				
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	DM54	2.4						2.5	3.4					V
			DM74	2.4						2.7	3.4					
									5.5						5.5	
I_{OL}	Low Level Output Current		DM54			16			16			4			4	mA
			DM74			16			16			8			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V	I_{OL} = 4 mA								0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA, DM74								0.35	0.5		0.35	0.5	
			I_{OL} = 16 mA			0.4			0.4							
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V			1			1							mA
			V_I = 7V									0.1			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V			40			40							µA
			V_I = 2.7V									20			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6			−0.36			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM54	−20	−32	−55		N/A		−30		−130		N/A		mA
			DM74	−18	−32	−55				−30		−130				
I_{CC}	Supply Current	V_{CC} = Max(3)	DM54		25	35		25	35		6.1	10		6.1	10	mA
			DM74		25	40		25	40		6.1	10		6.1	10	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CC} is measured with outputs open, A, B, and C1 inputs at 4.5V, and C2, G1 and G2 inputs grounded.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	DM54/74							DM54LS/74LS							UNITS
					CONDITIONS	155			156			CONDITIONS	LS155			LS156			
						MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A, B, C2 G1 or G2	Y	2	$C_L = 15$ pF $R_L = 400\Omega$		13	20		15	23	$C_L = 15$ pF $R_L = 2$ kΩ		10	15		25	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A, B, C2 G1 or G2	Y	2			18	27		19	30			19	30		34	51	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A or B	Y	3			18	27		21	32			17	26		31	46	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A or B	Y	3			17	26		18	27			19	30		34	51	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C1	Y	3			17	24		19	27			18	27		32	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C1	Y	3			17	26		18	27			18	27		32	48	ns

Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 157, L157A, LS157, and S157 present true data whereas the LS158 and S158 present inverted data to minimize propagation delay time.

Applications

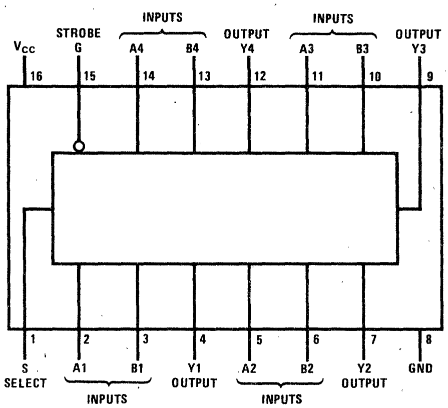
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

- Buffered inputs and outputs
- Three speed/power ranges available

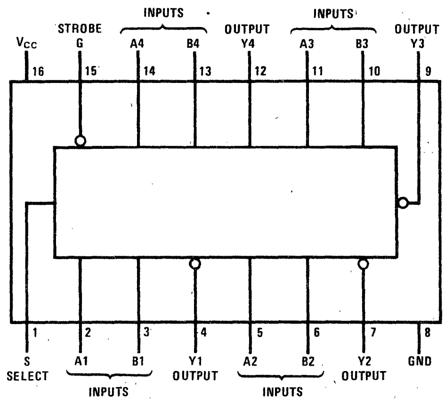
TYPE	TYPICAL PROPAGATION TIME	TYPICAL POWER DISSIPATION
157	9 ns	150 mW
L157A	40 ns	15 mW
LS157	9 ns	49 mW
S157	5 ns	250 mW
LS158	7 ns	24 mW
S158	4 ns	195 mW

Connection Diagrams



Low level at S selects A inputs
High level at S selects B inputs

54157(J), (W); 74157(J), (N), (W);
54L157A/74L157A(J), (N), (W);
54LS157/74LS157(J), (N), (W); 74S157(N)



Low level at S selects A inputs
High level at S selects B inputs

54LS158/74LS158(J), (N), (W);
74S158(N)

Truth Table

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	157, L157A LS157, S157	LS158 S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

LS157, LS158 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS			DM54/74 157			DM54L/74L L157A			DM54LS/74LS LS157, LS158			DM74S S157, S158			UNITS
						MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage					2			2			2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.8			0.7			0.7			N/A	V
					DM74			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA				−1.5			N/A							V
				I_I = −18 mA										−1.5			−1.2	
I_{OH}	High Level Output Current							−800			−200			−400			−1000	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.4			2.5	3.4		N/A			V
					DM74	2.4	3.4		2.4			2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current				DM54			16			2			4			N/A	mA
					DM74			16			3.6			8			20	
V_{OL}	Low Level Output Voltage		V_{CC} = Min	I_{OL} = 4 mA	DM74								0.25	0.4				V
			V_{IH} = 2V	I_{OL} = Max	DM54			0.4			0.3		0.25	0.4			N/A	
			V_{IL} = Max		DM74			0.4			0.4		0.35	0.5			0.5	
I_I	Input Current at Maximum Input Voltage	Any Input	V_{CC} = Max	V_I = 5.5V				1			0.1						1	mA
		S or G Input		V_I = 7V										0.2				
		A or B Input												0.1				
I_{IH}	High Level Input Current	Any Input	V_{CC} = Max	V_I = 2.4V				40			10							μA
		S or G Input		V_I = 2.7V										40			50	
		A or B Input												20			50	
I_{IL}	Low Level Input Current	Any Input	V_{CC} = Max	V_I = 0.3V							−0.18							mA
		S or G Input		V_I = 0.4V				−1.6						−0.8				
		A or B Input						−1.6						−0.4				
		Any Input		V_I = 0.5V													−2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		DM54	−20		−55	−3	−9	−15	−30		−130		N/A		mA
					DM74	−18		−55	−3	−9	−15	−30		−130	−40		−100	
I_{CC}	Supply Current		V_{CC} = Max(3)		157		30	48		3	4		9.7	16		50	78	mA
					158		N/A			N/A			4.8	8		39	61	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for the DM54LS/74LS or DM74S duration of the short circuit should not exceed one second.

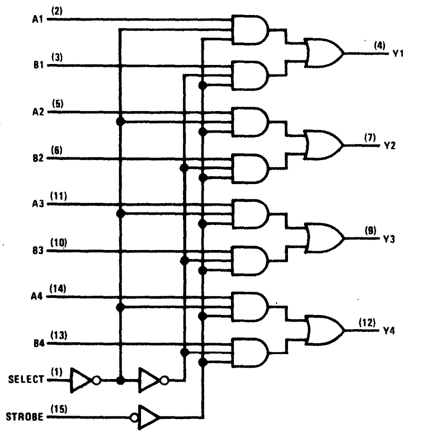
(3) I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

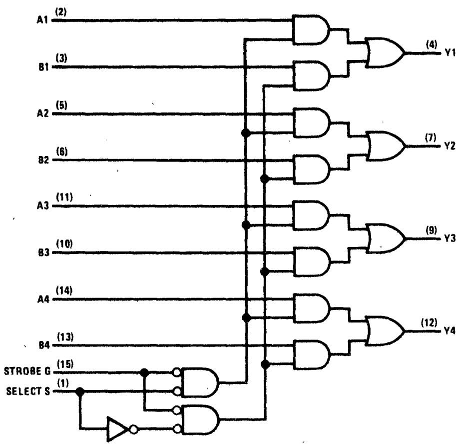
PARAMETER			FROM (INPUT)	DM54/74 157 CONDITIONS	MIN	TYP	MAX	DM54L/74L L157A CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS157, LS158 CONDITIONS	MIN	TYP	MAX	DM74S S157, S158 CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	157	Data	$C_L = 15$ pF, $R_L = 400\Omega$		8	14	$C_L = 50$ pF, $R_L = 4$ kΩ		40	80	$C_L = 15$ pF, $R_L = 2$ kΩ		9	14	$C_L = 15$ pF, $R_L = 280\Omega$		5	7.5	ns
		158				N/A				N/A				8	13			4	6	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	157				10	14			40	80			12	19			4.5	6.5	ns
		158				N/A				N/A				8	13			4	6	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	157	Strobe			13	20			60	120			16	25			8.5	12.5	ns
		158				N/A				N/A				14	25			6.5	11.5	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	157				14	21			60	120			17	27			7.5	12	ns
		158				N/A				N/A				16	27			7	12	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	157	Select			15	23			70	140			16.5	26			9.5	15	ns
		158				N/A				N/A				13	20			8	12	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	157				17	27			50	100			19	30			9.5	15	ns
		158				N/A				N/A				16	24			8	12	

Logic Diagrams

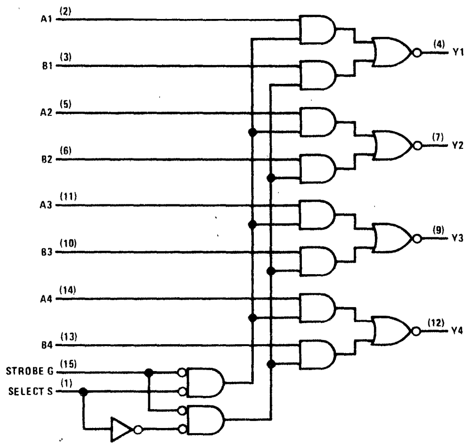
157, L157A



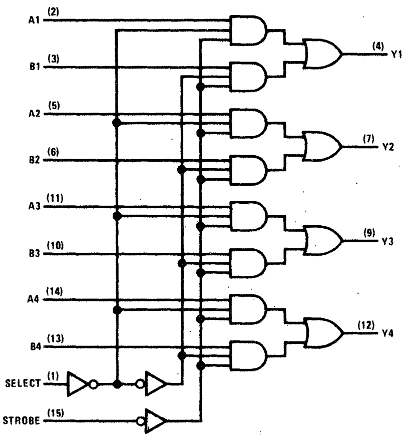
LS157



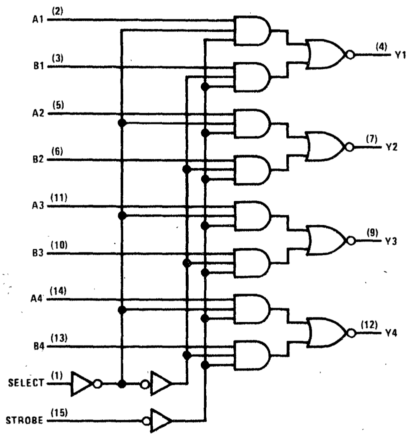
LS158



S157



S158



Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 160A, 162A, LS160, LS162, are decade counters and the 161A, 163A, LS161, LS163 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input of the 160A through 163A or LS160 through LS163 are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the 160A, 161A, LS160, and LS161 is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the 162A, 163A, LS162, LS163, is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low-to-high transitions at the clear input of the 162A and 163A are also permissible regardless of the logic levels on the clock, enable, or load inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the 160A through 163A or LS160 through LS163, may occur regardless of the logic level on the clock.

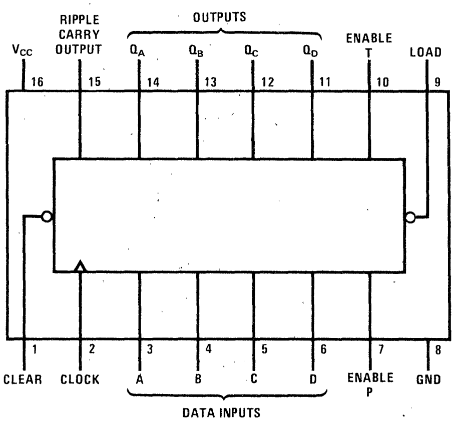
LS160 through LS163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
160 thru 163	14 ns	35 MHz	315 mW
LS160 thru LS163	14 ns	32 MHz	93 mW

Connection Diagram



54160A(J), (W); 74160A(J), (N), (W);
54LS160/74LS160(J), (N), (W);
54161A(J), (W); 74161A(J), (N), (W);
54LS161/74LS161(J), (N), (W);
54162A(J), (W); 74162A(J), (N), (W);
54LS162/74LS162(J), (N), (W);
54163A(J), (W); 74163A(J), (N), (W);
54LS163/74LS163(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS			DM54/74 160A, 161A 162A, 163A MIN	TYP(1)	MAX	DM54LS/74LS LS160, LS161 LS162, LS163 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.8			0.7	V
					DM74			0.8			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA				−1.5				V
				I_I = −18 mA							−1.5	
I_{OH}	High Level Output Current							−800			−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V		DM54	2.4	3.4		2.5	3.4		V
			V_{IL} = Max, I_{OH} = Max		DM74	2.4	3.4		2.7	3.4		
I_{OL}	Low Level Output Current				DM54			16			4	mA
					DM74			16			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min	I_{OL} = Max	DM54		0.2	0.4		0.25	0.4	V
			V_{IH} = 2V		DM74		0.2	0.4		0.35	0.5	
			V_{IL} = Max	I_{OL} = 4 mA	DM74					0.25	0.4	
I_I	Input Current ax Maximum Input Voltage	All		V_I = 5.5V				1				mA
		Data or Enable P	V_{CC} = Max	V_I = 7V							0.1	
		Load, Clock, or Enable T									0.2	
		Clear (LS160, LS161)									0.1	
		Clear (LS162, LS163)									0.2	
I_{IH}	High Level Input Current	Load	V_{CC} = Max V_I = 2.4V (160A–163A) V_I = 2.7V (LS160–LS163)					40			40	μA
		Clock, Enable T						80			40	
		Data						40			20	
		Enable P						40			20	
		Clear (160, 161)						40			20	
		Clear (162, 163)						40			40	
I_{IL}	Low Level Input Current	Data, Enable P	V_{CC} = Max	V_I = 0.4V				−1.6			−0.4	mA
		Clock						−3.2			−1.2	
		Load						−1.6			−0.8	
		Enable T						−3.2			−0.8	
		Clear (160, 161)						−1.6			−0.4	
		Clear (162, 163)						−1.6			−0.8	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		DM54	−20		−57	−30		−130	mA
					DM74	−18		−57	−30		−130	
I_{CCH}	Supply Current, All Outputs High		V_{CC} = Max(3)		DM54		59	85		18	31	mA
					DM74		59	94		18	31	
I_{CCL}	Supply Current, All Outputs Low		V_{CC} = Max(4)		DM54		63	91		19	32	mA
					DM74		63	101		19	32	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

(4) I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER			FROM (INPUT)	TO (OUTPUT)	DM54/74 160A, 161A, 162A, 163A CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS160, LS161, LS162, LS163 CONDITIONS	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 400Ω	25	35		C_L = 15 pF, R_L = 2 kΩ	25	32		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Ripple carry			18	27			23	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Ripple carry			16	24			23	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock (Load Input High)	Any Q			14	20			16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock (Load Input High)	Any Q			16	23			18	27	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock (Load Input Low)	Any Q			14	21			17	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock (Load Input Low)	Any Q			18	25			19	29	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Enable T	Ripple carry			10	15			15	23	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Enable T	Ripple carry			12	16			15	23	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear (5)	Any Q			24	36			26	38	ns
$t_{W(CLOCK)}$	Width of Clock Pulse					25				25			ns
$t_{W(CLEAR)}$	Width of Clear Pulse					20				20			ns
t_{SETUP}	Setup Time	Data Inputs A, B, C, D				20				20			ns
		Enable P				20				25			ns
		Load				25				25			ns
		Clear(6)				20				25			ns
t_{HOLD}	Hold Time at Any Input					0				0			ns

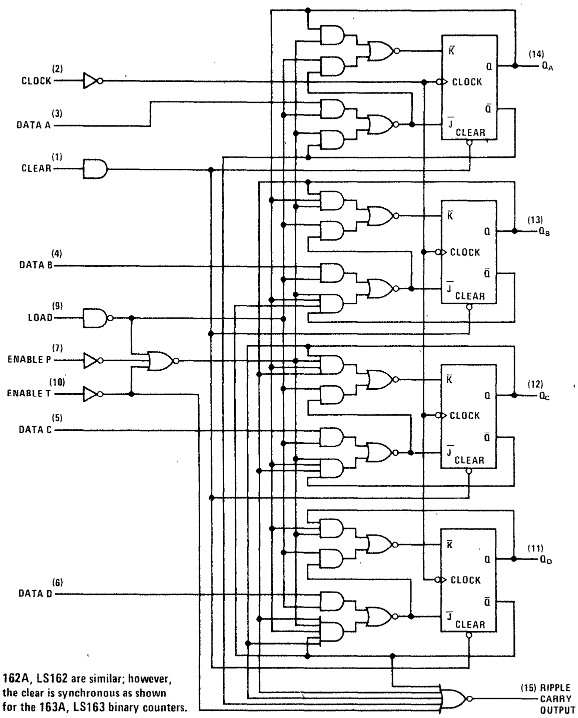
Notes

(5) Propagation delay for clearing is measured from the clear input for the 160A, LS160, 161A and LS161 or from the clock input transition for the 162A, LS162, 163A and LS163.

(6) This applies only for 162, 163, LS162 and LS163, which have synchronous clear inputs.

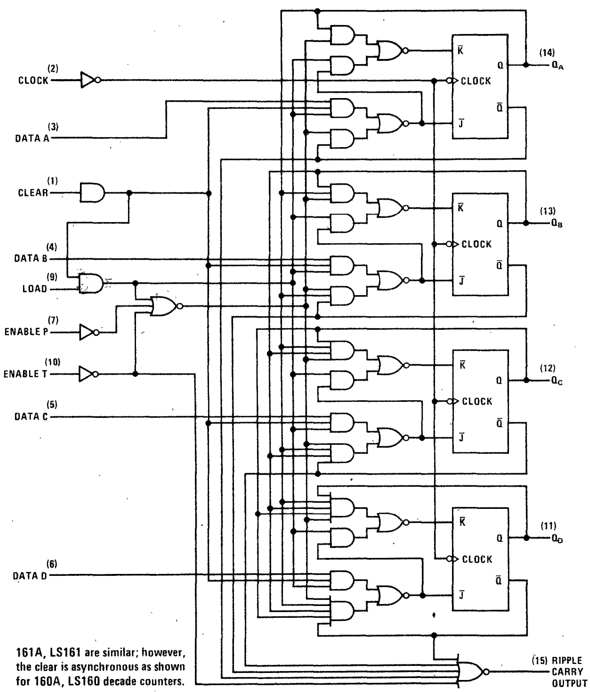
Logic Diagrams

160A, LS160



162A, LS162 are similar; however, the clear is synchronous as shown for the 163A, LS163 binary counters.

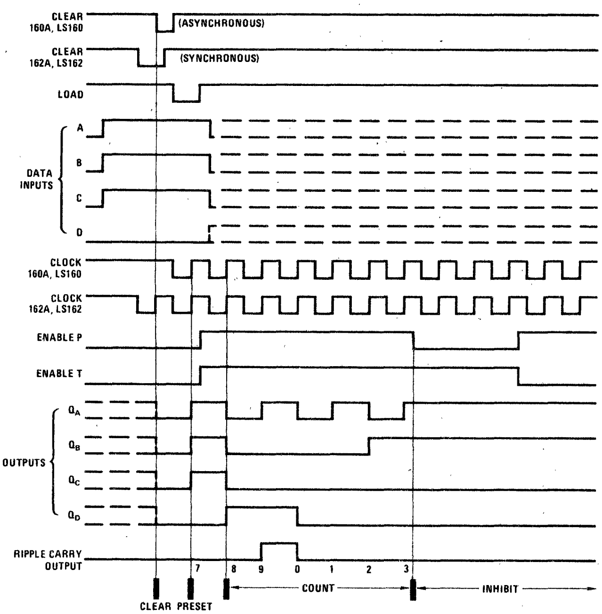
163A, LS163



161A, LS161 are similar; however, the clear is asynchronous as shown for 160A, LS160 decade counters.

Timing Diagrams

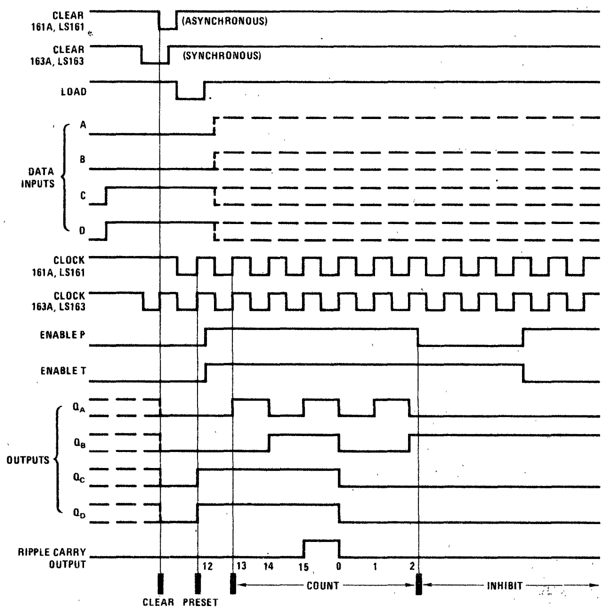
160, 162, LS160, LS162 SYNCHRONOUS DECADE COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES



Sequence:

(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

161, LS161, 163, LS163 SYNCHRONOUS BINARY COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

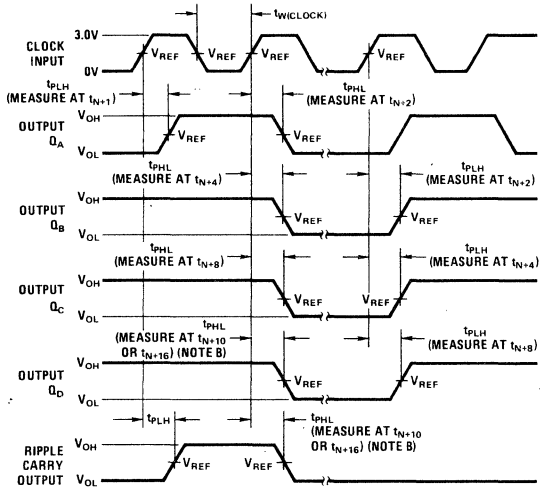


Sequence:

(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Parameter Measurement Information

SWITCHING TIME WAVEFORMS



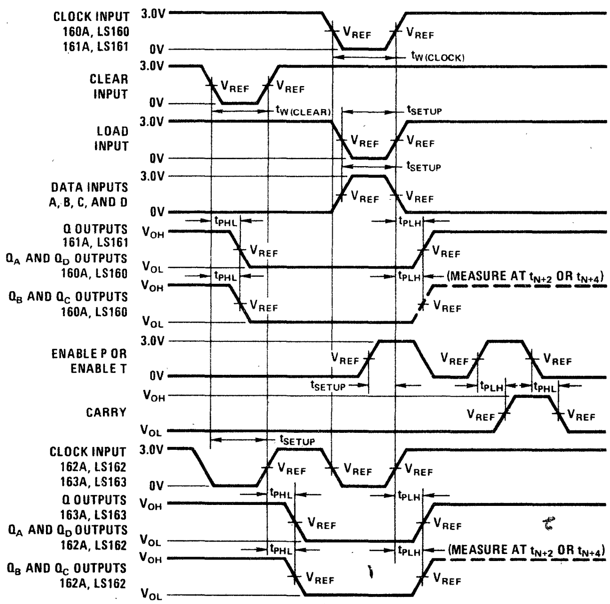
Notes:

(A) The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, for 160A through 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for LS160 through LS163, $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{MAX}.

(B) Outputs Q_D and carry are tested at t_{n+10} for 160A, 162A, LS160, LS162, and at t_{n+16} for 161A, 163A, LS161, LS163, where t_n is the bit time when all outputs are low.

(C) For 160A through 163A, V_{REF} = 1.5V; for LS160 through LS163, V_{REF} = 1.3V.

SWITCHING TIME WAVEFORMS



Notes:

(A) The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For 160A through 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns, and for LS160 through LS163, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

(B) Enable P and enable T setup times are measured at t_{n+0}.

(C) For 160A through 163A, V_{REF} = 1.5V; for LS160 through LS163, V_{REF} = 1.3V.

8-Bit Serial In/Parallel Out Shift Registers

General Description

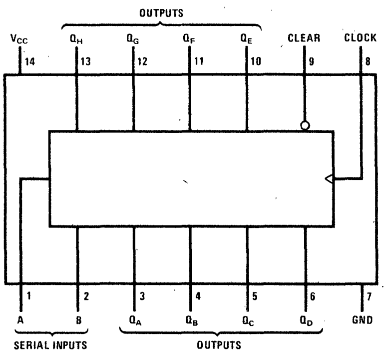
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear

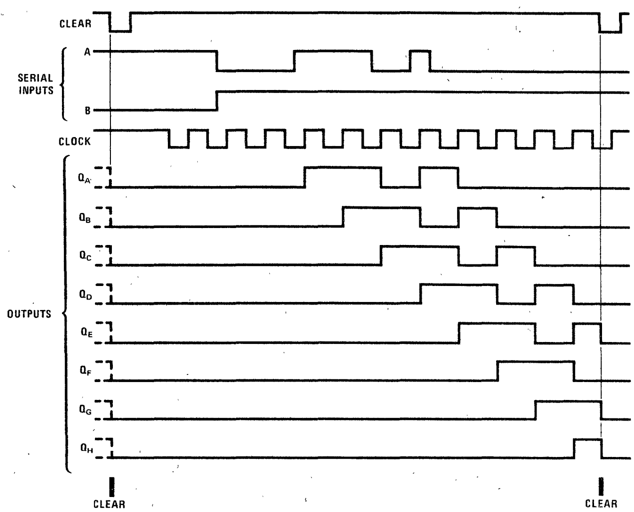
TYPE	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
164	36 MHz	185 mW
L164A	14 MHz	30 mW
LS164	36 MHz	80 mW

Connection Diagram

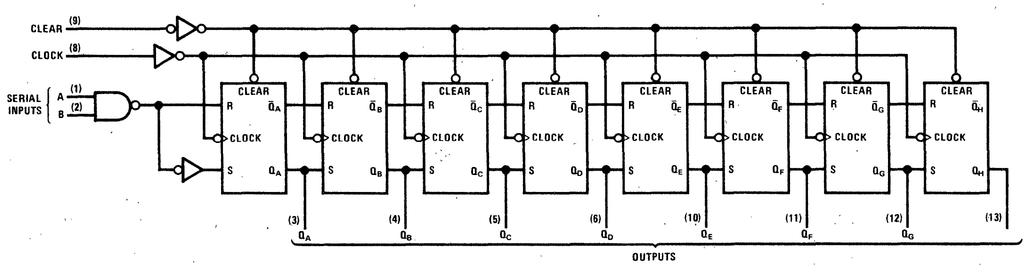


54164(J), (W); 74164(J), (N), (W); 54L164A/74L164A(J), (N), (W); 54LS164/74LS164(J), (N), (W)

Timing Diagram



Logic Diagram



LS164 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS			DM54/74 164 MIN	DM54/74 164 TYP(1)	DM54/74 164 MAX	DM54L/74L L164A MIN	DM54L/74L L164A TYP(1)	DM54L/74L L164A MAX	DM54LS/74LS LS164 MIN	DM54LS/74LS LS164 TYP(1)	DM54LS/74LS LS164 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			0.7	V
				DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5			N/A				V
			I_I = −18 mA										−1.5	
I_{OH}	High Level Output Current						−400			−200			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V		DM54	2.4	3.2		2.4			2.5	3.5		V
		V_{IL} = Max, I_{OH} = Max		DM74	2.4	3.2		2.4			2.7	3.5		
I_{OL}	Low Level Output Current			DM54			8			2			4	mA
				DM74			8			3.6			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = Max	DM54		0.2	0.4			0.3		0.25	0.4	V
		V_{IH} = 2V		DM74		0.2	0.4			0.4		0.35	0.5	
		V_{IL} = Max	I_{OL} = 4 mA	DM74								0.25	0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V	Clear			1			0.2				mA
				Other			1			0.1				
			V_I = 7V	All									0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V	Clear			40			20				μA
				Other			40			10				
			V_I = 2.7V	All									20	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V, L164A	Clear			−1.6			−0.36			−0.4	mA
			V_I = 0.4V, Others	Other			−1.6			−0.18			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−10		−27.5	−3	−9	−15	−30		−130	mA
				DM74	−9		−27.5	−3	−9	−15	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max(3)				37	54		6	9		16	27	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V, applied to clear.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER	CONDITIONS		DM54/74 164 MIN	DM54/74 164 TYP	DM54/74 164 MAX	DM54L/74L L164A MIN	DM54L/74L L164A TYP	DM54L/74L L164A MAX	DM54LS/74LS LS164 MIN	DM54LS/74LS LS164 TYP	DM54LS/74LS LS164 MAX	UNITS
f_{MAX}	Maximum Clock Frequency		C_L = 15 pF	25	36		6	14		25	36		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level Outputs From Clear Input	R_L = 800Ω for the 164	C_L = 15 pF		24	36					24	36	ns
			C_L = 50 pF		28	42		75	120				
t_{PLH}	Propagation Delay Time, Low-to-High Level Outputs From Clock Input	R_L = 4 kΩ for the L164A	C_L = 15 pF	8	17	27					17	27	ns
			C_L = 50 pF	10	20	30		50	85				
t_{PHL}	Propagation Delay Time, High-to-Low Level Outputs From the Clock Input	R_L = 2 kΩ for the LS164	C_L = 15 pF	10	21	32					21	32	ns
			C_L = 50 pF	10	25	37		90	135				
t_W	Width of Clock or Clear Input Pulse			20			60	40		20			ns
t_{SETUP}	Data Setup Time			15			40	20		15			ns
t_{HOLD}	Data Hold Time			5			20	−5		5			ns

Truth Table

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B . . .	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

8-Bit Pararallel In/Serial Out Shift Registers

General Description

These are 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

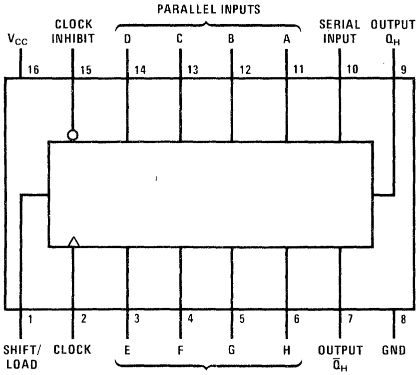
Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion

TYPE	TYPICAL FREQUENCY	TYPICAL POWER DISSIPATION
165	20 MHz	200 mW
L165A	14 MHz	30 mW

Connection Diagram



54165(J), (W); 74165(J), (N), (W);
54L165A/74L165A(J), (N), (W)

Truth Table

INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low-to-high level
a . . . h = The level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM54/74 165 MIN	DM54/74 165 TYP(1)	DM54/74 165 MAX	DM54L/74L L165A MIN	DM54L/74L L165A TYP(1)	DM54L/74L L165A MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5			N/A	V
I_{OH}	High Level Output Current				−800			−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	2.4			2.4			V
I_{OL}	Low Level Output Current	DM54			16			2	mA
		DM74			16			3.6	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max — DM54		0.2	0.4			0.3	V
		DM74		0.2	0.4			0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			0.1	mA
I_{IH}	High Level Input Current — Load Input	V_{CC} = Max, V_I = 2.4V			80			30	μA
	Other Inputs				40			10	
I_{IL}	Low Level Input Current — Load Input	V_{CC} = Max, V_I = 0.3V for L165A			−3.2			−0.54	mA
	Other Inputs	V_{CC} = Max, V_I = 0.4V for 165			−1.6			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2) — DM54	−20		−55	−3	−9	−15	mA
		DM74	−18		−55	−3	−9	−15	
I_{CC}	Supply Current	V_{CC} = Max(3)		40	63			9.5	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

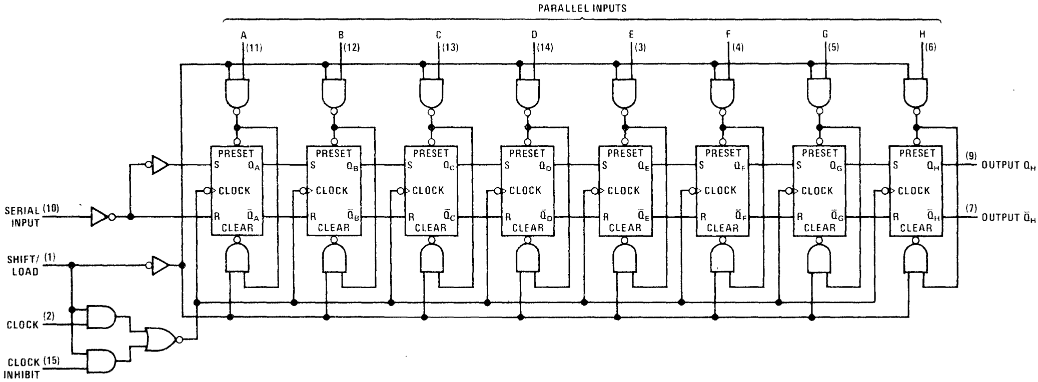
(2) Not more than one output should be shorted at a time.

(3) With the outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

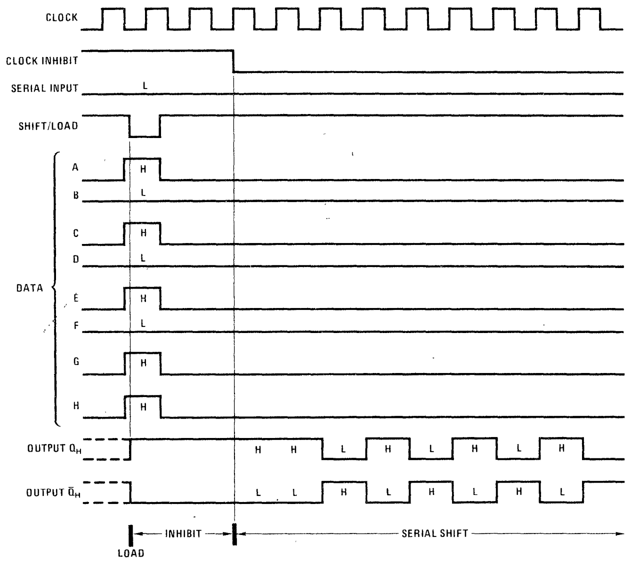
	PARAMETER	FROM (INPUT)	TO (OUTPUT)	DM54/74 165 CONDITIONS	MIN	TYP	MAX	DM54L/74L L165A CONDITIONS	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				14	20			6	14		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Load	Any	C_L = 15 pF, R_L = 400Ω		34	50	C_L = 50 pF, R_L = 4 kΩ		44	88	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Load	Any			42	60			62	124	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Any			26	40			35	70	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock	Any			35	50			50	100	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	H	Q_H			25	40			33	66	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	H	Q_H			36	50			56	112	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	H	$\overline{Q}_H$			25	40			33	66	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	H	$\overline{Q}_H$			36	50			56	112	ns
$t_{W(CLOCK)}$	Width of Clock Input Pulse				35	25			100			ns
$t_{W(LOAD)}$	Width of Load Input Pulse				35	24			100			ns
t_{SETUP}	Parallel Input Setup Time				25	10			44	22		ns
t_{SETUP}	Serial Input Setup Time				40	23			44	22		ns
t_{HOLD}	Hold Time at Any Input				5				10			ns

Logic Diagram



Timing Diagram

TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCES

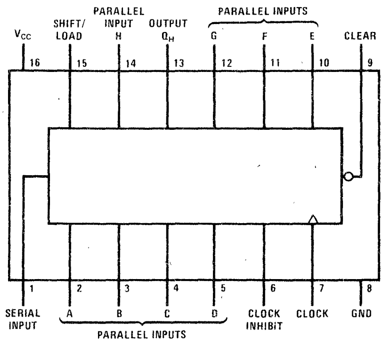


8-Bit Parallel In/Serial Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Connection Diagram



54166/74166(J), (N)

Truth Table

INPUTS						INTERNAL OUTPUTS		OUTPUT Q_H
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

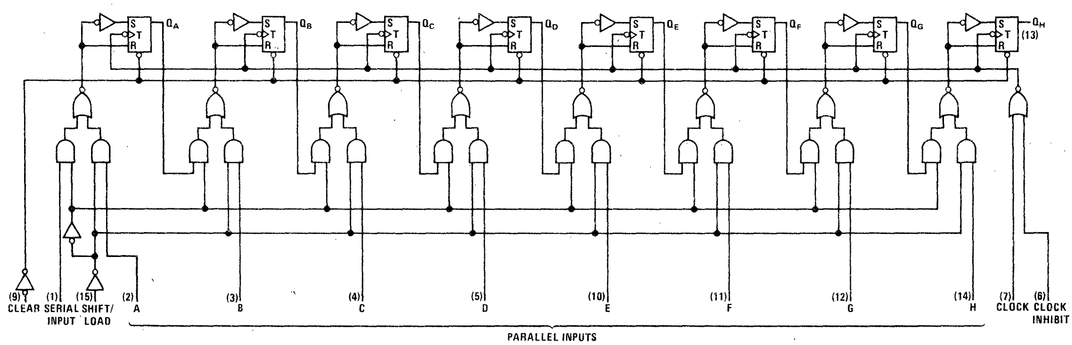
↑ = Transition from low to high level

a . . . h = The level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 166 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −800μA		2.4			V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max(3)	DM54		72	104	mA
			DM74		72	116	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

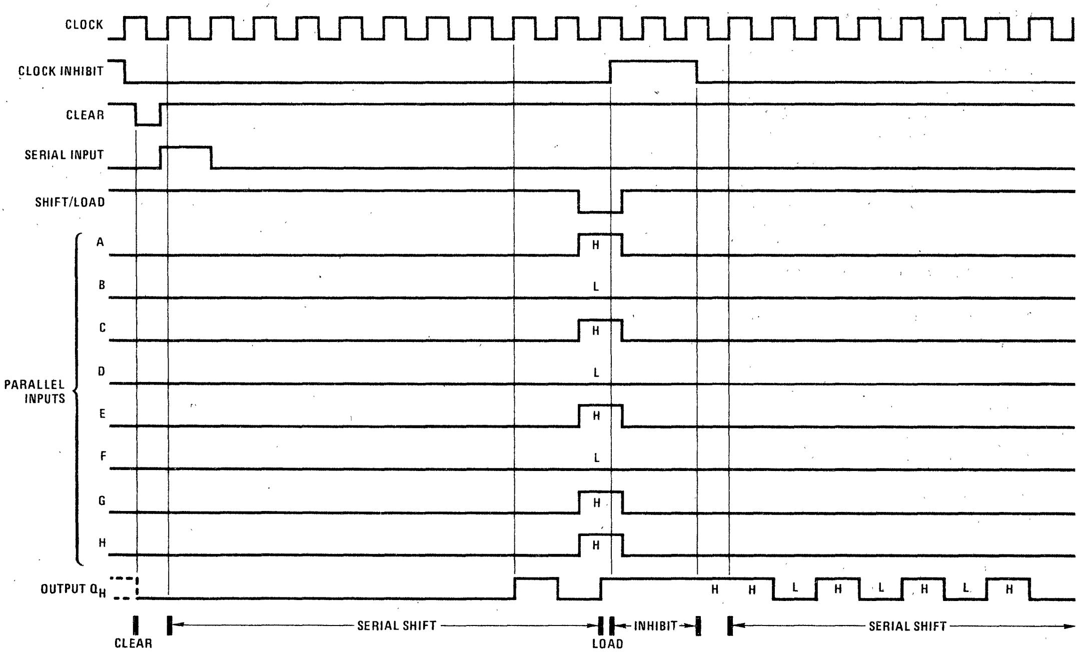
(3) With all outputs open, 4.5V applied to the serial input, all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	DM54/74 166 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clear			23	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock		8	20	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock		8	17	26	ns
t_W	Width of Clock or Clear Pulse		20			ns
t_{SETUP}	Mode Control Setup Time		30			ns
t_{SETUP}	Data Setup Time		20			ns
t_{HOLD}	Hold Time at Any Input		0			ns

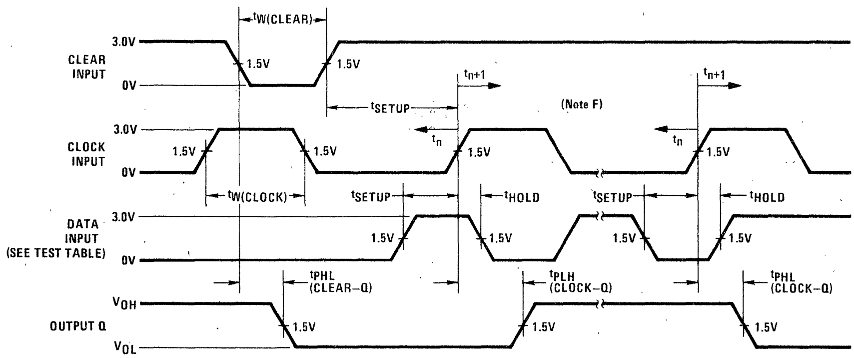
Timing Diagram

TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES



Parameter Measurement Information

VOLTAGE WAVEFORMS



Notes

(A) The clock pulse has the following characteristics: $t_{W(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{W(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns. When testing f_{MAX}, vary the clock PRR.

(B) C_L includes probe and jig capacitance.

(C) All diodes are 1N3064.

(D) A clear pulse is applied prior to each test.

(E) Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

(F) t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
H	0V	Q_H at t_{n+1}
Serial Input	4.5V	Q_H at t_{n+8}

Synchronous 4-Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

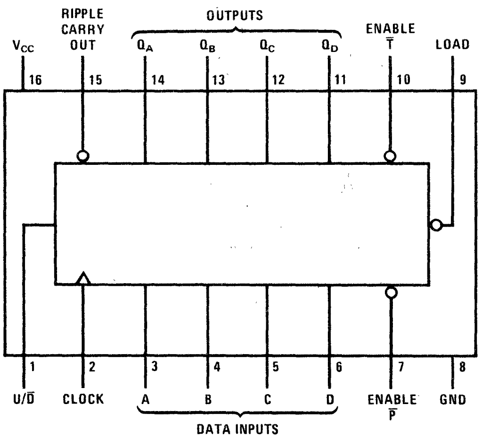
The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Fully synchronous operation for counting and programming
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Fully independent clock circuit

Connection Diagram



54LS168/74LS168(J), (N), (W); 54LS169/74LS169(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS		DM54LS/74LS168, LS169 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage			DM54			0.7	V
				DM74			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current						−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = −400μA	DM54	2.5	3.4		V
				DM74	2.7	3.4		
I_{OL}	Low Level Output Current			DM54			4	mA
				DM74			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max; I_{OL} = 4 mA			0.25	0.4	V
			I_{OL} = 8 mA,	DM74		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = Max, V_I = 7V				0.1	mA
		Clock, $\overline{T}$					0.2	
		Load					0.3	
I_{IH}	High Level Input Current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = Max, V_I = 2.7V				20	μA
		Clock, $\overline{T}$					40	
		Load					60	
I_{IL}	Low Level Input Current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = Max, V_I = 0.4V				−0.4	mA
		$\overline{T}$					−0.8	
		Load, Clock					−1.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		−30		−130	mA
I_{CC}	Supply Current		V_{CC} = Max(3)			20	34	mA

Notes (1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) I_{CC} is measured after applying a momentary 4.5V, then ground, to the clock input with all other inputs grounded and the outputs open.

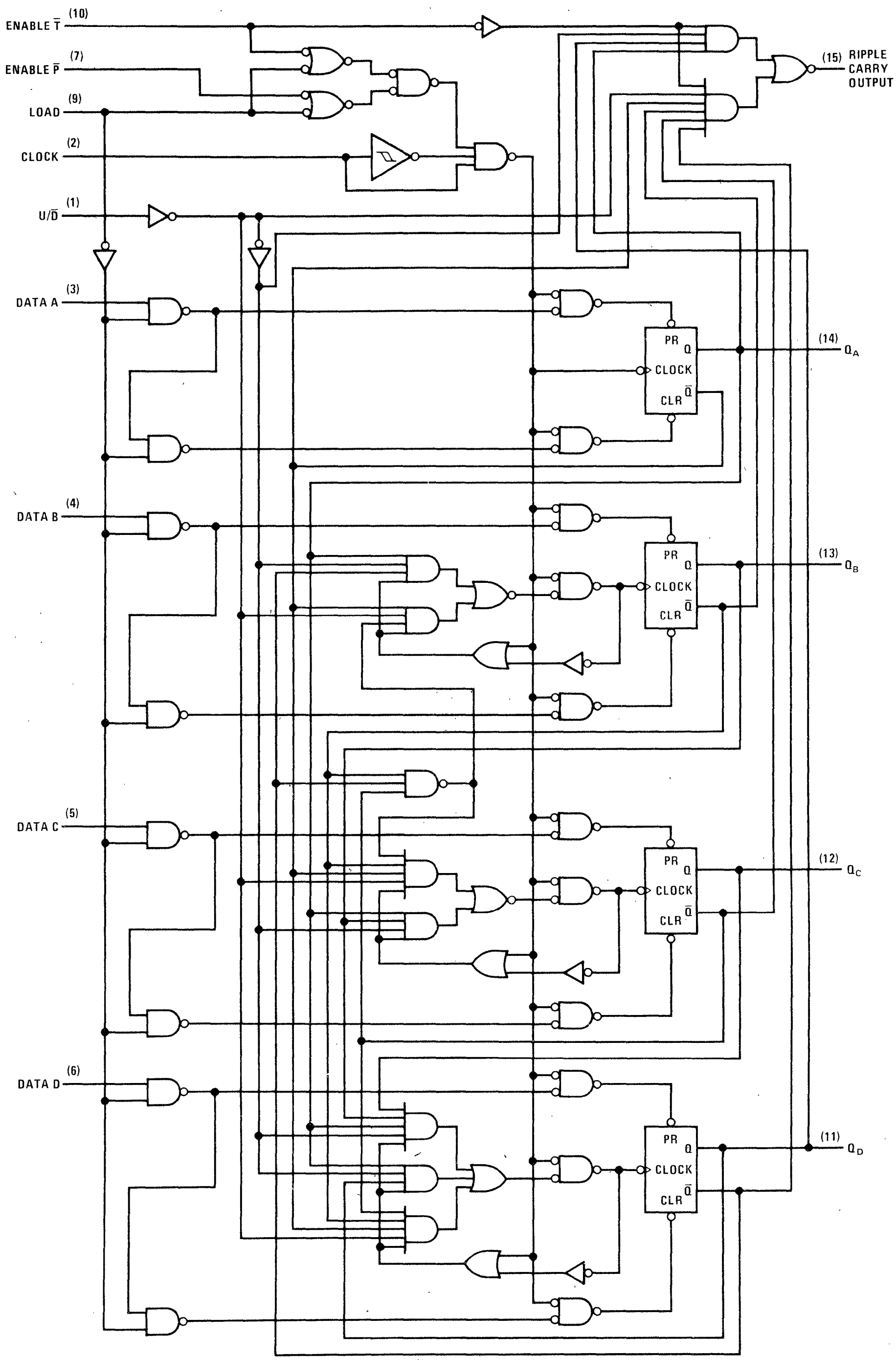
Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54LS/74LS168, LS169 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 2 kΩ,	25	32		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Ripple Carry			23	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Ripple Carry			23	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Any Q			13	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Any Q			15	23	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Enable $\overline{T}$	Ripple Carry			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Enable $\overline{T}$	Ripple Carry			16	23	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Up/Down (4)	Ripple Carry			17	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Up/Down (4)	Ripple Carry			19	29	ns
$t_{W(CLOCK)}$	Width of Clock Pulse (High or Low)					25			ns
t_{SETUP}	Setup Time	Data Inputs A, B, C, D				20			ns
		Enable $\overline{P}$ or $\overline{T}$				25			
		Load				25			
		Up/Down				30			
t_{HOLD}	Hold Time	Data Inputs A, B, C, D				0			ns
		Enable $\overline{P}$ or $\overline{T}$				0			
		Load, Up/Down				0			

Notes (4) Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for LS168 or 15 for LS169), the ripple carry output will be out of phase.

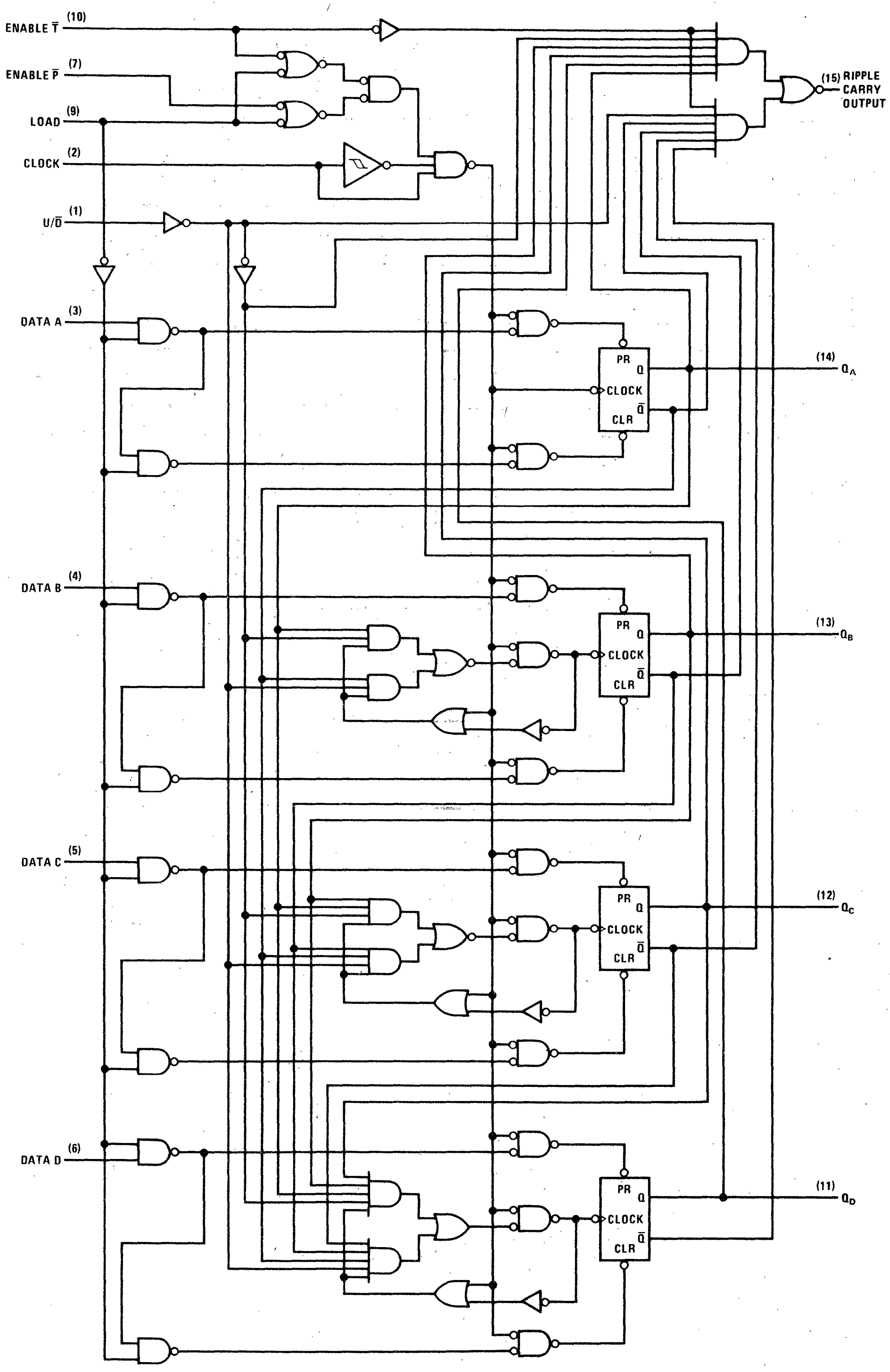
Logic Diagrams

LS168 DECADE COUNTERS



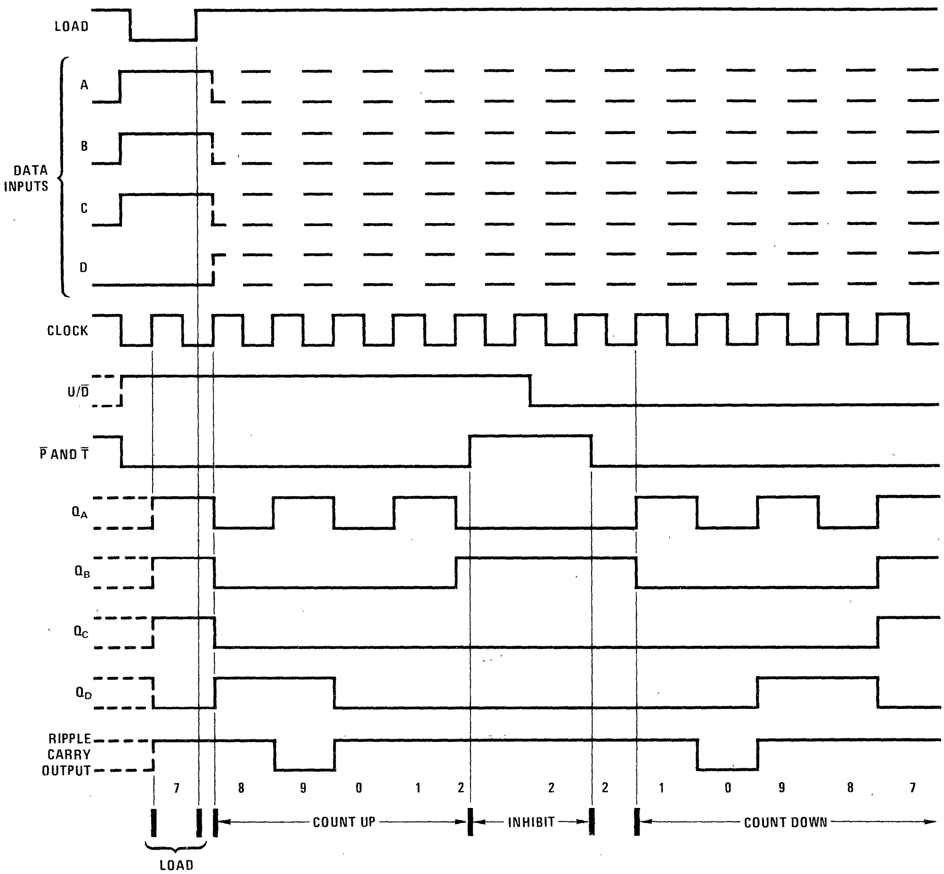
Logic Diagrams (Continued)

LS169 BINARY COUNTERS



Timing Diagrams

LS168 DECADE COUNTERS
TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES



Sequence:

(1) Load (preset) to BCD seven

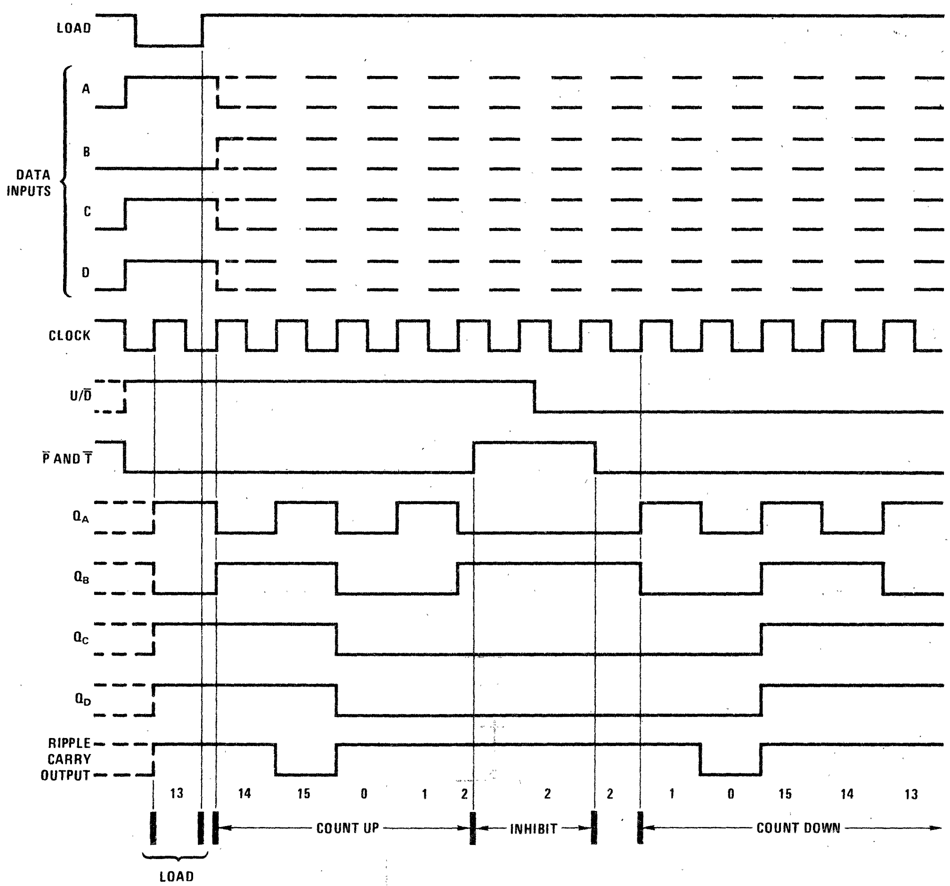
(2) Count up to eight, nine, zero, one and two

(3) Inhibit

(4) Count down to one, zero, nine, eight and seven

Timing Diagrams (Continued)

LS169 BINARY COUNTERS
TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES



Sequence:

(1) Load (preset) to binary thirteen

(2) Count up to fourteen, fifteen, zero, one and two

(3) Inhibit

(4) Count down to one, zero, fifteen, fourteen and thirteen

4 by 4 Register Files

General Description

These 16-bit TTL register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addessssing the four word locations to either write-in or retrieve data. This permits writing into one location and reading from another word location, simultaneously.

Four data inputs are available to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct reading of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

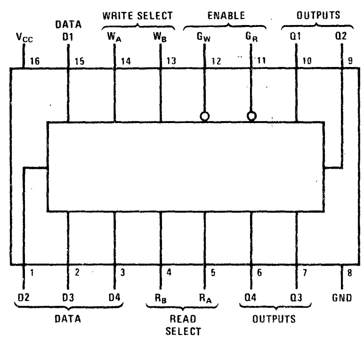
This arrangement—data entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 ns typical) and the read time (25 ns typical). The register file has a nondestructive readout in that data is not lost when addressed.

All 170 inputs and all inputs except the read enable and write enable of the LS170 are buffered to lower the drive requirements to one standard load. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

Features

- Separate addressing permits simultaneous reading and writing
- Fast access times — typically 20 ns
- Organized as 4 words of 4 bits
- Expandable to 1024 words of n-bits
- For use as:
  - Scratch-pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Open-collector outputs with low maximum off-state current:
  - 170 — 30μA
  - LS170 — 20μA
- DM54LS670 and DM74LS670 are similar but have TRI-STATE outputs

Connection Diagram



74170(J), (N);
54LS170/74LS170(J), (N), (W)

Truth Tables

WRITE TRUTH TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ TRUTH TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

Notes

(A) H = High Level, L = Low Level, X = Don't Care
(B) (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
(C) Q_0 = The level of Q before the indicated input conditions were established.
(D) W0B1 = The first bit of word 0, etc.

LS170 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM74 170 MIN	DM74 170 TYP(1)	DM74 170 MAX	DM54LS/74LS LS170 MIN	DM54LS/74LS LS170 TYP(1)	DM54LS/74LS LS170 MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage	DM54			N/A			0.7	V
		DM74			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA			−1.5				V
		V_{CC} = Min, $I_I = -18$ mA						−1.5	
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, V_{OH} = 5.5V			30			20	μA
V_{OH}	High Level Output Voltage				5.5			5.5	V
I_{OL}	Low Level Output Current	DM54			N/A			4	mA
		DM74			16			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max; I_{OL} = 4 mA, DM74					0.25	0.4	V
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max; I_{OL} = Max, DM54			N/A		0.25	0.4	
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max; I_{OL} = Max, DM74		0.2	0.4		0.35	0.5	
I_I	Input Current at Maximum Input Voltage — Any	V_{CC} = Max, V_I = 5.5V			1				mA
	Any D, R, or W	V_{CC} = Max, V_I = 7V						0.1	
	G_R or G_W	V_{CC} = Max, V_I = 7V						0.2	
I_{IH}	High Level Input Current — Any	V_{CC} = Max, V_I = 2.4V			40				μA
	Any D, R, or W	V_{CC} = Max, V_I = 2.7V						20	
	G_R or G_W	V_{CC} = Max, V_I = 2.7V						40	
I_{IL}	Low Level Input Current — Any D, R, or W	V_{CC} = Max, V_I = 0.4V			−1.6			−0.4	mA
	G_R or G_W	V_{CC} = Max, V_I = 0.4V			−1.6			−0.8	
I_{CC}	Supply Current	V_{CC} = Max(2)		127	150		25	40	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) I_{CC} is measured under the following worst-case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER		FROM (INPUT)	TO (OUTPUT)	DM74 170 CONDITIONS	DM74 170 MIN	DM74 170 TYP	DM74 170 MAX	DM54LS/74LS LS170 CONDITIONS	LS170 MIN	LS170 TYP	LS170 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Read Enable	Any Q	$C_L = 15\ pF$, $R_L = 400\Omega$		10	15	$C_L = 15\ pF$, $R_L = 2\ k\Omega$		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						20	30			20	30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Read Select	Any Q			23	35			25	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						30	40			24	40	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Write Enable	Any Q			25	40			30	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						34	45			26	40	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Data	Any Q			20	30			30	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						30	45			22	35	
t_W	Width of Write-Enable or Read-Enable Pulse					25				25			ns
t_{SETUP}	Setup Times, High- or Low-Level Data(3)	Data Input With Respect to Write Enable, $t_{SETUP(D)}$				10				10			ns
		Write Select With Respect to Write Enable, $t_{SETUP(W)}$				15				15			ns
t_{HOLD}	Hold Times, High- or Low-Level Data(3)	Data Input With Respect to Write Enable, $t_{HOLD(D)}$				15				15			ns
		Write Select With Respect to Write Enable, $t_{HOLD(W)}$				5				5			ns
t_{LATCH}	Latch Time for New Data(4)					25				25			ns

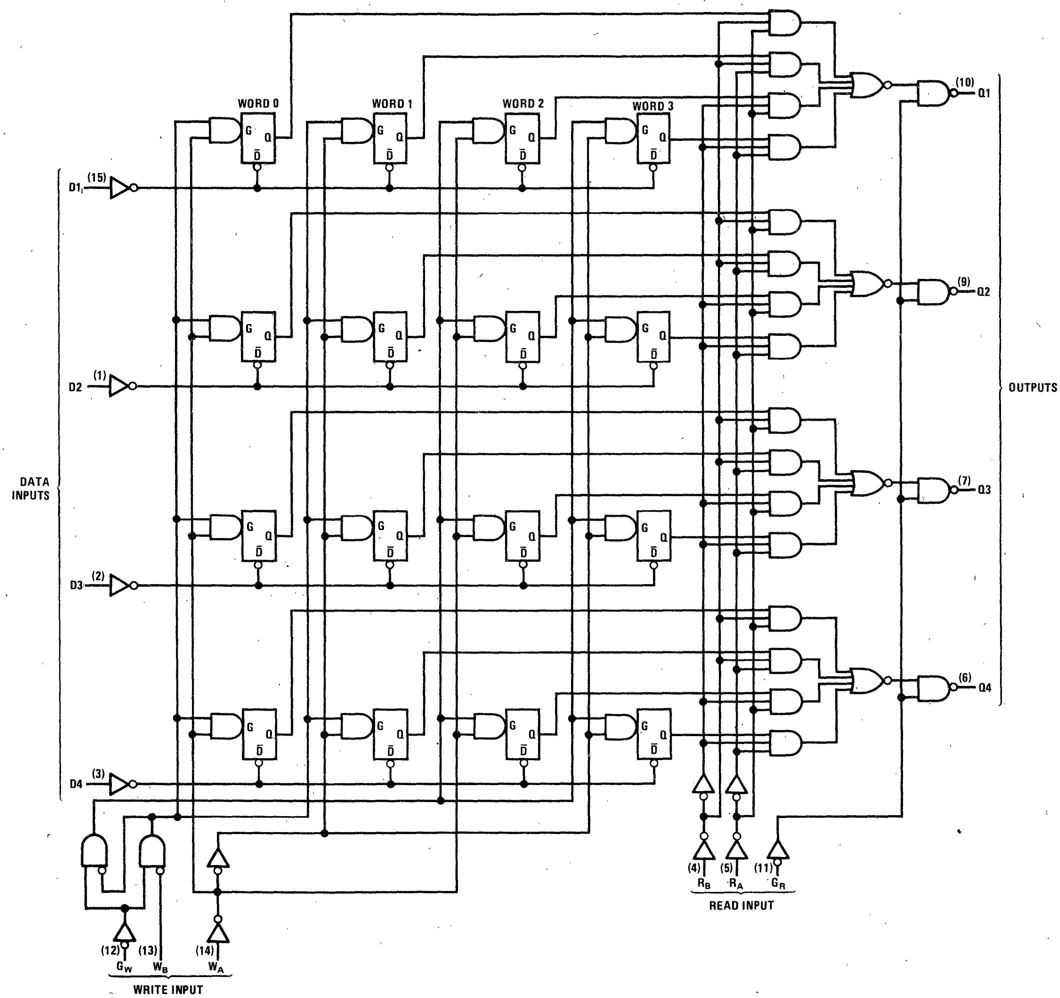
Notes

(3) Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{SETUP(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{HOLD(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

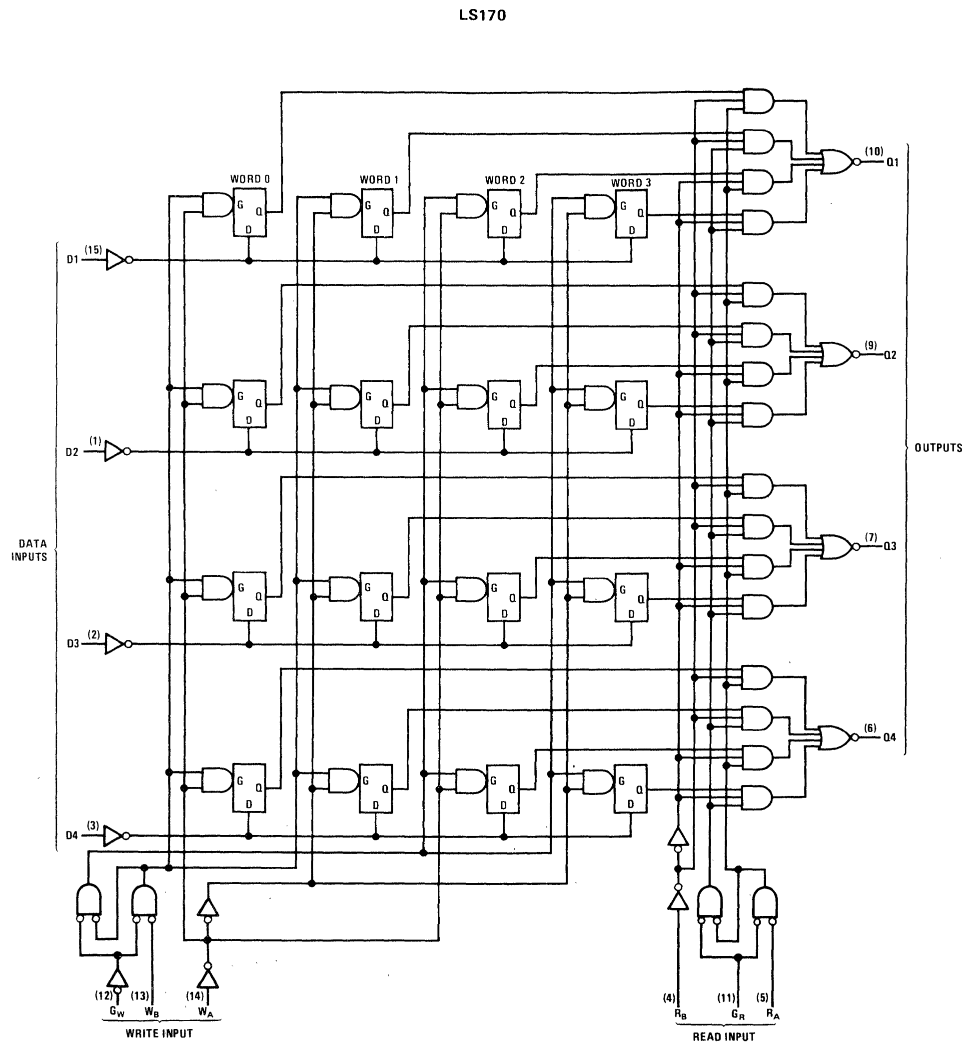
(4) Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

Logic Diagrams

170



Logic Diagrams (Continued)



TRI-STATE Quad D Registers

General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the truth table.

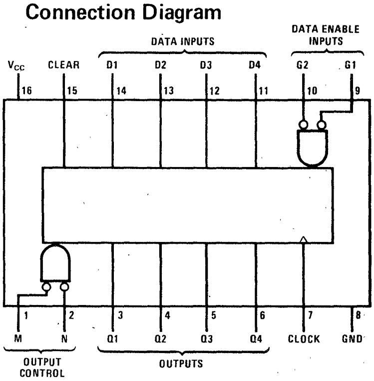
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers

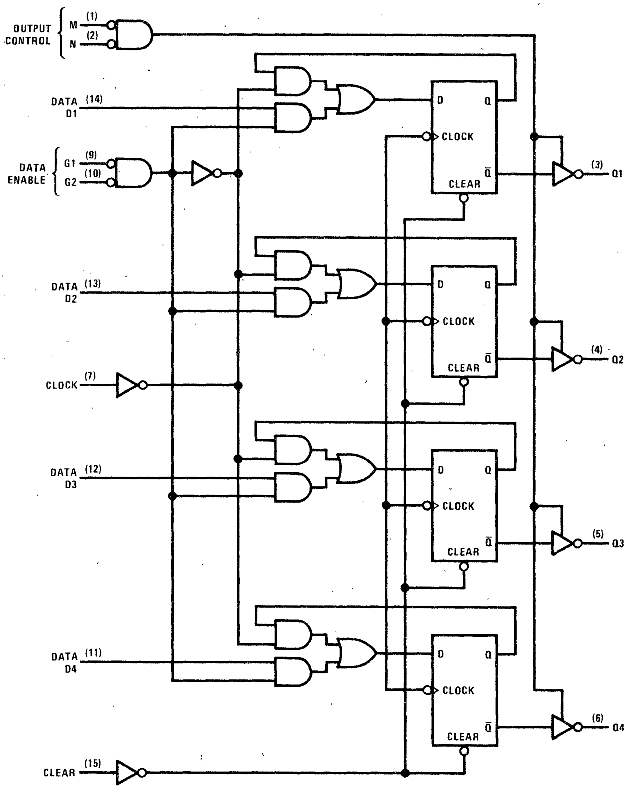
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL FREQUENCY	TYPICAL POWER DISSIPATION
173	18 ns	30 MHz	250 mW
LS173	18 ns	30 MHz	85 mW

Connection Diagram



54173(J), (W); 74173(J), (N), (W); 54LS173/74LS173(J), (N), (W)

Logic Diagram



Truth Table

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
Q_0 = the level of Q before the indicated steady state input conditions were established

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 173 MIN	TYP(1)	MAX	DM54LS/74LS LS173(4) MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7	V
			DM74			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA			−1.5				V
			I_I = −18 mA						−1.5	
I_{OH}	High Level Output Current		DM54			−2			−1.0	mA
			DM74			−5.2			−2.6	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	DM54	2.4			2.5			V
			DM74	2.4			2.7			
I_{OL}	Low Level Output Current		DM54			16			4	mA
			DM74			16			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max	DM54			0.4			0.4	V
			DM74			0.4			0.5	
		I_{OL} = 4 mA	DM74						0.4	
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V	V_O = 0.4V			−40			−20	μA
			V_O = 2.4V			40				
			V_O = 2.7V						20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V			1				mA
			V_I = 7.0V						0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V			40				μA
			V_I = 2.7V						20	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V			−1.6			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−70	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			50	72		17	24	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CC} is measured with all outputs open; clear grounded following momentary connection to 4.5V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5V.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER		CONDITIONS	DM54/74 173 MIN	TYP	MAX	CONDITIONS	DM54LS/74LS LS173(4) MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency		C_L = 50 pF, R_L = 400Ω	25	30		C_L = 15 pF, R_L = 2 kΩ	25	30		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clear				18	27			18	27	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock				16	25			16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock				20	28			20	28	ns
t_{ZH}	Output Enable Time to High Level			7	16	30		7	16	30	ns
t_{ZL}	Output Enable Time to Low Level			7	21	30		7	21	30	ns
t_{HZ}	Output Disable Time From High Level		C_L = 5 pF, R_L = 400Ω	3	5	14	C_L = 5 pF, R_L = 2 kΩ	3	5	14	ns
t_{LZ}	Output Disable Time From Low Level			3	11	20		3	11	20	ns
t_W	Width of Clock or Clear Pulse			20				20			ns
t_{SETUP}	Setup Time	Data Enable		17				17			ns
		Data		10				10			
		Clear Inactive State		10				10			
t_{HOLD}	Hold Time	Data Enable		2				2			ns
		Data		10				10			

Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

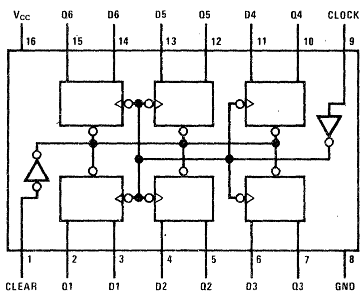
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

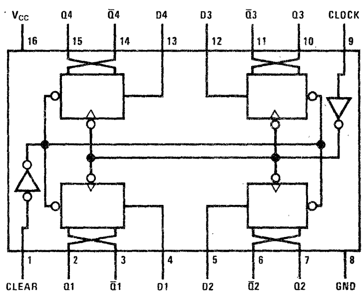
- 174, LS174, S174 contain six flip-flops with single-rail outputs
- 175, LS175, S175 contain four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators

TYPE	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
174, 175	40 MHz	38 mW
LS174, LS175	40 MHz	14 mW
S174, S175	110 MHz	75 mW

Connection Diagrams



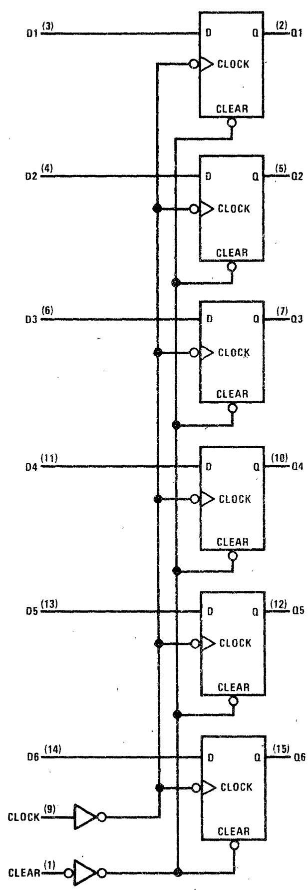
54174(J), (W); 74174(J), (N), (W);
54LS174/74LS174(J), (N), (W); 74S174(N)



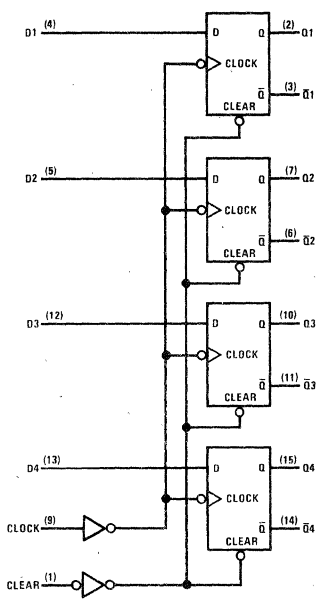
54175(J), (W); 74175(J), (N), (W);
54LS175/74LS175(J), (N), (W); 74S175(N)

Logic Diagrams

174



175



S174, S175 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 174, 175 MIN	TYP(1)	MAX	DM54LS/74LS LS174, LS175 MIN	TYP(1)	MAX	DM74S S174, S175 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7			N/A	V
			DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA			−1.5							V
			I_I = −18 mA						−1.5			−1.2	
I_{OH}	High Level Output Current					−800			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	DM54	2.4			2.5	3.5			N/A		V
			DM74	2.4			2.7	3.5		2.7	3.4		
I_{OL}	Low Level Output Current		DM54			16			4			N/A	mA
			DM74			16			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max; I_{OL} = Max	DM54			0.4		0.25	0.4			N/A	V
		I_{OL} = Max	DM74			0.4		0.35	0.5			0.5	
		I_{OL} = 4 mA	DM74						0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V			1						1	mA
			V_I = 7V						0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V			40							μA
			V_I = 2.7V						20			50	
I_{IL}	Low Level Input Current — Clock, Clear	V_{CC} = Max	V_I = 0.4V			−1.6			−0.4				mA
	Data		V_I = 0.4V			−1.6			−0.36				
	Any		V_I = 0.5V									−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM54	−20		−57	−30		−130		N/A		mA
			DM74	−18		−57	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max(3)	174, LS174, S174		45	65		16	26		90	144	mA
			175, LS175, S175		30	45		11	18		60	96	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS and DM74S duration of short circuit should not exceed one second.

(3) With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to clock.

(4) National Semiconductor temporarily reserves the right to ship DM54LS/DM74LS174, LS175 devices which have a minimum I_{OS} = 5.0 mA.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER			DM54/74 174, 175 CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS174, LS175 CONDITIONS	MIN	TYP	MAX	DM74S S174, S175 CONDITIONS	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency		C_L = 15 pF R_L = 400Ω	30	40		C_L = 15 pF R_L = 2 kΩ	30	40		C_L = 15 pF R_L = 280Ω	75	110		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clear (175 Only)				14	25			16	25			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clear				20	30			23	35			13	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock				14	25			20	30			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock				17	25			23	35			11.5	17	ns
t_W	Pulse Width	Clock		20				20				7			ns
		Clear		20				20				10			
t_{SETUP}	Setup Time	Data Input		20				20				5			ns
		Clear Inactive-State		30				25				5			
t_{HOLD}	Data Hold Time			0				5				3			ns

Truth Table (Each Flip-Flop)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = 175, LS175, and S175 only

Presettable Decade and Binary Counters

General Description

These high-speed counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (176, 196) or a divide-by-two and a divide-by-eight counter (177, 197). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

TYPICAL COUNT CONFIGURATIONS 176, 196 AND LS196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table.

2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

177, 197 AND LS197

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.

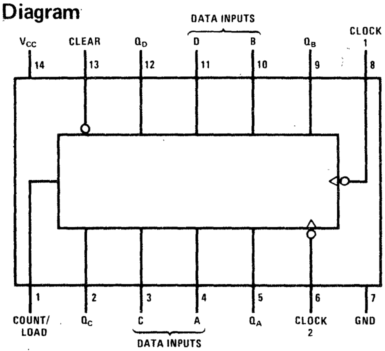
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

Features

- Performs BCD, bi-quinary, or binary counting
- Fully programmable
- Fully independent clear input
- Output Q_A maintains full fan-out capability in addition to driving clock-2 input

TYPE	TYPICAL COUNT FREQUENCY CLOCK 1	TYPICAL COUNT FREQUENCY CLOCK 2	TYPICAL POWER DISSIPATION
176, 177	50 MHz	25 MHz	150 mW
196, 197	50 MHz	25 MHz	240 mW
LS196, LS197	40 MHz	20 MHz	80 mW

Connection Diagram



Note: Low input to clear sets Q_A, Q_B, Q_C and Q_D low.

54176(J); 74176(J), (N); 54177(J); 74177(J), (N);
54196/74196(J), (N); 54LS196/74LS196(J), (N), (W);
54197/74197(J), (N); 54LS197/74LS197(J), (N), (W)

LS196, LS197 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS		DM54/74 176, 177 MIN	DM54/74 176, 177 TYP(1)	DM54/74 176, 177 MAX	DM54/74 196, 197 MIN	DM54/74 196, 197 TYP(1)	DM54/74 196, 197 MAX	DM54LS/74LS LS196, LS197 MIN	DM54LS/74LS LS196, LS197 TYP(1)	DM54LS/74LS LS196, LS197 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7	V
				DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA			−1.5			−1.5				V
				I_I = −18 mA									−1.5	
I_{OH}	High Level Output Current						−800			−800			−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OH} = Max	DM54	2.4	3.4		2.4	3.4		2.5	3.4		V
				DM74	2.4	3.4		2.4	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			16			4	mA
				DM74			16			16			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min	I_{OL} = 4 mA									0.4	V
			V_{IH} = 2V	I_{OL} = 8 mA, DM74									0.5	
			V_{IL} = Max(3)	I_{OL} = 16 mA		0.2	0.4		0.2	0.4				
I_I	Input Current at Maximum Input Voltage	Data, Count/Load	V_{CC} = Max, V_I = 5.5V				1			1			0.1	mA
		Clear, Clock 1					1			1			0.2	
		Clock 2		176, 196			1			1			0.4	
				177, 197			1			1			0.2	
I_{IH}	High Level Input Current	Data, Count/Load	V_{CC} = Max, V_I = 2.4V V_I = 2.7V (LS196, LS197)				40			40			20	μA
		Clear, Clock 1					80			80			40	
		Clock 2		176, 196			120			120			80	
				177, 197			80			80			40	
I_{IL}	Low Level Input Current	Data, Count/Load	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6			−0.36	mA
		Clear					−3.2			−3.2			−0.72	
		Clock 1					−4.8			−4.8			−2.4	
		Clock 2		176, 196			−4.8			−6.4			−2.8	
				177, 197			−3.2			−3.2			−1.3	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	DM54	−20		−57	−20		−57	−30		−130	mA
				DM74	−18		−57	−18		−57	−30		−130	
I_{CC}	Supply Current		V_{CC} = Max(4)			30	48		39	54		16	27	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.

(4) I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	DM54/74 CONDITIONS	176, 177 MIN	176, 177 TYP	176, 177 MAX	196, 197 MIN	196, 197 TYP	196, 197 MAX	DM54LS/74LS CONDITIONS	LS196 MIN	LS196 TYP	LS196 MAX	LS197 MIN	LS197 TYP	LS197 MAX	UNITS
f_{MAX}	Maximum Input Count Frequency	Clock 1	Q_A	$C_L = 15 pF$, $R_L = 400\Omega$	35	50		40	50		$C_L = 15 pF$, $R_L = 2 k\Omega$(5)	30	40		30	40		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 1	Q_A			9	13		9	13			8	15		8	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 1	Q_A			11	17		11	16			13	20		14	21	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 2	Q_B			12	18		12	18			16	24		12	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 2	Q_B			14	21		14	21			22	33		23	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 2	Q_C			27	41		24	36			38	57		34	51	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 2	Q_C			34	51		28	42			41	62		42	63	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 2	Q_D 176, 196			13	20		14	21			12	18				ns
			Q_D 177, 197			44	66		36	54						55	78	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 2	Q_D 176, 196			17	26		16	23			30	45				ns
			Q_D 177, 197			50	75		42	63						63	95	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A, B, C, D	Q_A, Q_B, Q_C, Q_D			19	29		16	24			20	30		18	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A, B, C, D	Q_A, Q_B, Q_C, Q_D			31	46		25	38			29	44		29	44	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Load	Any			29	43		22	33			27	41		26	39	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Load	Any			32	48		24	36			30	45		30	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Any			32	48		25	37			34	51		34	51	ns
t_W	Pulse Width: Clock-1 Input				14			14				20			20			ns
	Pulse Width: Clock-2 Input				28			28				30			30			
	Pulse Width: Clear				25			25				15			15			
	Pulse Width: Load				20			20				20			20			
t_{HOLD}	Input Hold Time: High-Level Data				$t_{W(LOAD)}$			$t_{W(LOAD)}$				$t_{W(LOAD)}$			$t_{W(LOAD)}$			ns
	Input Hold Time: Low-Level Data				$t_{W(LOAD)}$			$t_{W(LOAD)}$				$t_{W(LOAD)}$			$t_{W(LOAD)}$			
t_{SETUP}	Input Setup Time: High-Level Data				15			10				10			10			ns
	Input Setup Time: Low-Level Data				20			15				15			15			
t_{ENABLE}	Count Enable Time(6)				25			30				20			20			ns

Notes

(5) Load circuit, input conditions, and voltage waveforms are the same as those for the 176, 177 except that for the LS196, LS197 $t_r \leq 15$ ns, $t_f \leq 6$ ns, and $V_{REF} = 1.3V$ (as opposed to 1.5V).

(6) Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

Truth Tables

176, 196, LS196
DECADE (BCD)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

176, 196, LS196
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

177, 197, LS197
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

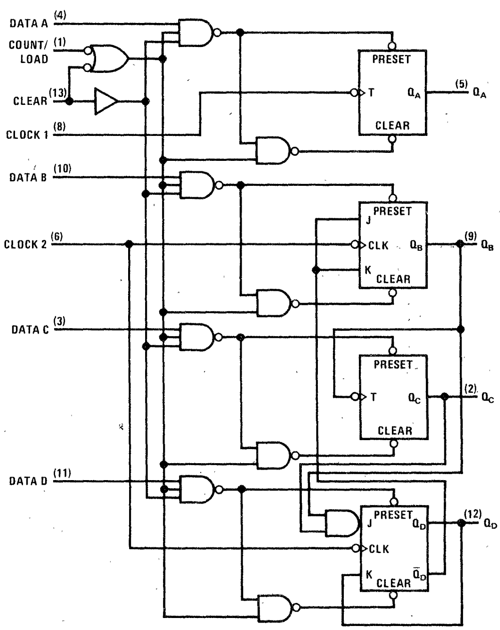
H = High Level, L = Low Level

Notes:

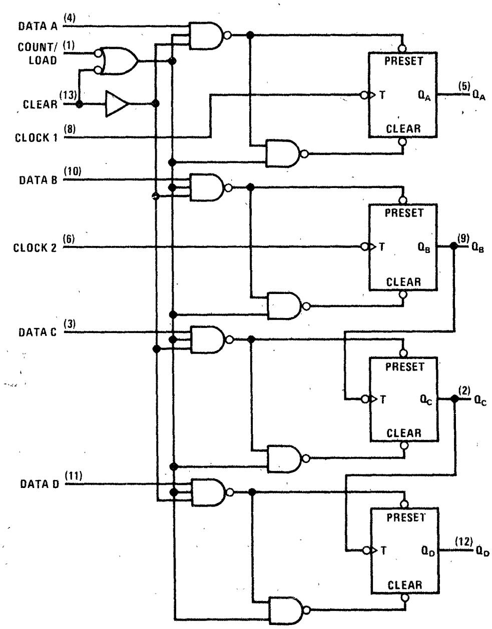
(A) Output Q_A connected to clock-2 input.
(B) Output Q_D connected to clock-1 input.

Logic Diagrams

196, LS196



197, LS197



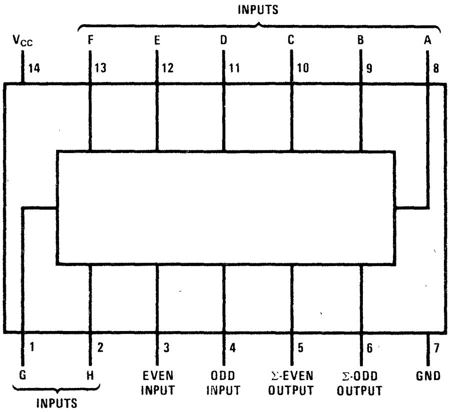
9-Bit Parity Generators/Checkers

General Description

These universal 9-bit (8 data bits plus 1 parity bit) parity generators/checkers feature odd/even outputs and control inputs to facilitate operation in either odd or even parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs.

Connection Diagram



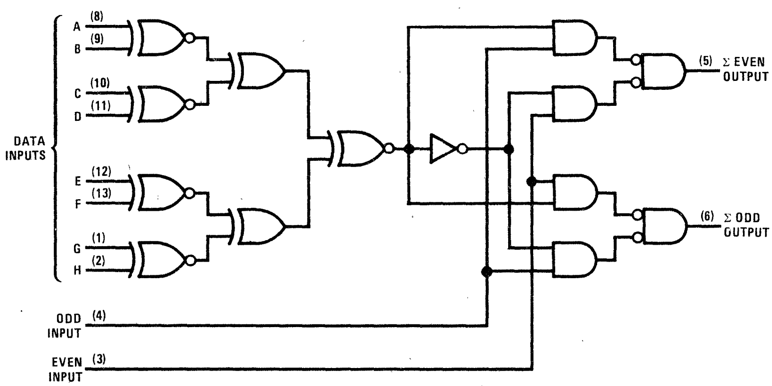
54180(J), (W); 74180(J), (N), (W)

Truth Table

INPUTS			OUTPUTS	
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = High Level, L = Low Level, X = Don't Care

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Conditions		DM54/74 180 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current						−800	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA		2.4			V
I_{OL}	Low Level Output Current						16	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA				0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	Any Data Input	V_{CC} = Max, V_I = 2.4V				40	μA
		Even or Odd Input					80	
I_{IL}	Low Level Input Current	Any Data Input	V_{CC} = Max, V_I = 0.4V				−1.6	mA
		Even or Odd Input					−3.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	DM54	−20		−55	mA
				DM74	−18		−55	
I_{CC}	Supply Current		V_{CC} = Max(3)	DM54		34	49	mA
				DM74		34	56	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) I_{CC} is measured with even and odd inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54/74 180 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Σ Even	C_L = 15 pF, R_L = 400Ω Odd Input Grounded		40	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					45	68	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Σ Odd			32	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	38	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Σ Even	C_L = 15 pF, R_L = 400Ω Even Input Grounded		32	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	38	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Σ Odd			40	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					45	68	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Even or Odd	Σ Even or Σ Odd	C_L = 15 pF, R_L = 400Ω		13	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7	10	ns

Arithmetic Logic Unit/Function Generators

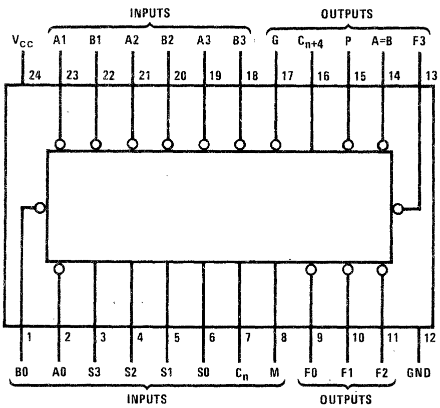
General Description

These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54182/DM74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54182/DM74182. (Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words

Connection Diagram



54181(J); 74181(J), (N)

Pin Designations

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	19, 21, 23, 2	WORD A INPUTS
B3, B2, B1, B0	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION-SELECT INPUTS
C_n	7	INV. CARRY INPUT
M	8	MODE CONTROL INPUT
F3, F2, F1, F0	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT,
C_{n+4}	16	INV. CARRY OUTPUT
G	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GND	12	GROUND

NUMBER OF BITS	TYPICAL ADDITION TIMES	PACKAGE COUNT		CARRY METHOD BETWEEN ALU's
		ARITHMETIC/ LOGIC UNITS	LOOK AHEAD CARRY GENERATORS	
1 to 4	20 ns	1	0	NONE
5 to 8	30 ns	2	0	RIPPLE
9 to 16	30 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	50 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A–B–1, which requires an end-around or forced carry to provide A–B.

The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The DM54181/DM74181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table 1; those obtained with the signal designations of *Figure 2* are given in Table 2.

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-Low Data (Table II)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-HIGH DATA (FIGURE 1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	$A \leq B$	$A \geq B$
H	L	$A > B$	$A < B$
L	H	$A < B$	$A > B$
L	L	$A \geq B$	$A \leq B$

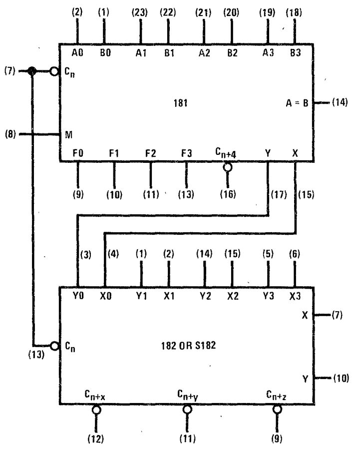


FIGURE 1

TABLE 1

SELECTION				ACTIVE HIGH DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = \overline{AB}$	F = A PLUS $A\overline{B}$	F = A PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS $A\overline{B}$	F = (A + B) PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = (A + \overline{B})$ PLUS AB	$F = (A + \overline{B})$ PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	$F = (A + \overline{B})$ PLUS A	$F = (A + \overline{B})$ PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

General Description (Continued)

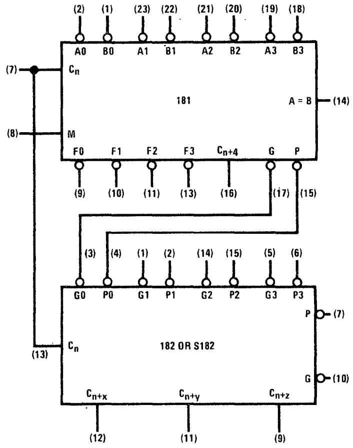


FIGURE 2

TABLE 2

SELECTION				ACTIVE LOW DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS $(A + \overline{B})$	F = A PLUS $(A + \overline{B})$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS $(A + \overline{B})$	F = AB PLUS $(A + \overline{B})$ PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	F = $(A + \overline{B})$ PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $A\overline{B}$ PLUS (A + B)	F = $A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS			DM54/74 181 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage					2			V
V_{IL}	Low Level Input Voltage							0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA					−1.5	V
I_{OH}	High Level Output Current (Any Output Except A = B)							−800	μA
I_{OH}	High Level Output Current (A = B Output Only)		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, V_{OH} = 5.5V					250	μA
V_{OH}	High Level Output Voltage (Any Output Except A = B)		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −800μA			2.4			V
I_{OL}	Low Level Output Current							16	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA					0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V					1	mA
I_{IH}	High Level Input Current	Mode Input	V_{CC} = Max, V_I = 2.4V					40	μA
		Any A or B Input						120	
		Any S Input						160	
		Carry Input						200	
I_{IL}	Low Level Input Current	Mode Input	V_{CC} = Max, V_I = 0.4V					−1.6	mA
		Any A or B Input						−4.8	
		Any S Input						−6.4	
		Carry Input						−8.0	
I_{OS}	Short Circuit Output Current (Any Output Except A = B)		V_{CC} = Max(2)		DM54	−20		−55	mA
					DM74	−18		−57	
I_{CC}	Supply Current		V_{CC} = Max(3)	Condition A	DM54		88	127	mA
					DM74		88	140	
				Condition B	DM54		92	135	
					DM74		92	150	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) With outputs open, I_{CC} is measured for the following conditions:

A. S0 through S3, M, and A inputs are at 4.5V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5V, all other inputs are grounded.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74 181 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+4}			9	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	19	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22	33	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22	33	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	Any F	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		11	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12	18	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	19	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					15	25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)		12	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					17	25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					17	25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)		18	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					19	30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		14	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 4.5V (logic mode)		17	28	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					19	30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	A = B	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		26	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	40	

Parameter Measurement Information

LOGIC MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = M = 4.5V, S0 = S3 = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT: APPLY 4.5V	OTHER INPUT SAME BIT: APPLY GND	OTHER DATA INPUTS: APPLY 4.5V	OTHER DATA INPUTS: APPLY GND	OUTPUT UNDER TEST	OUTPUT WAVEFORM
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase

Parameter Measurement Information (Continued)

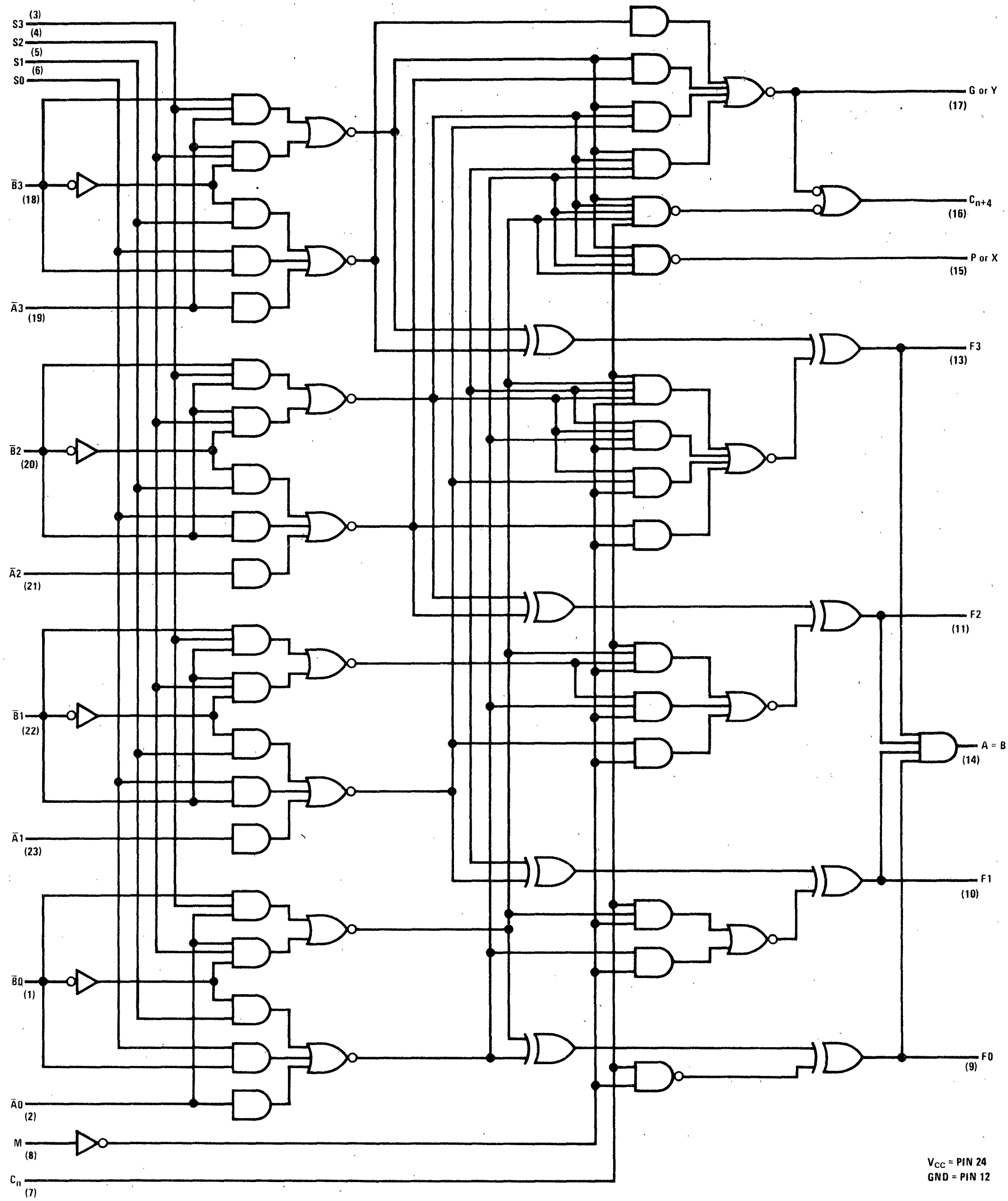
$\overline{\text{SUM}}$ MODE TEST TABLE
FUNCTION INPUTS: S0 = S3 = 4.5V, S1 = S2 = M = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A	All B	Any F or C_{n+4}	In-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase

$\overline{\text{DIFF}}$ MODE TEST TABLE
FUNCTION INPUTS: S1 = S2 = 4.5V, S0 = S3 = M = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A and B	None	C_{n+4} or any F	In-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_{n+4}	In-Phase

Logic Diagram



Look-Ahead Carry Generators

General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 or S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 182 and S182 are:

$$C_{n+x} = \overline{G0} + \overline{P0}\,C_n$$

$$C_{n+y} = \overline{G1} + \overline{P1}\,\overline{G0} + \overline{P1}\,\overline{P0}\,C_n$$

$$C_{n+z} = \overline{G2} + \overline{P2}\,\overline{G1} + \overline{P2}\,\overline{P1}\,\overline{G0} + \overline{P2}\,\overline{P1}\,\overline{P0}\,C_n$$

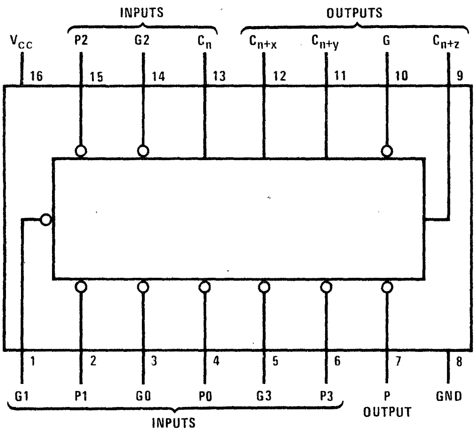
$$\overline{G} = \overline{G3}\,(\overline{P3} + \overline{G2})\,(\overline{P3} + \overline{P2} + \overline{G1})\,(\overline{P3} + \overline{P2} + \overline{P1} + \overline{G0})$$

$$\overline{P} = \overline{P3}\,\overline{P2}\,\overline{P1}\,\overline{P0}$$

Features

TYPE	TYPICAL PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
182	12 ns	180 mW
S182	7 ns	260 mW

Connection Diagram



54182(J); 74182(J), (N); 74S182(N)

Pin Designations

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE LOW CARRY GENERATE OUTPUT
P	7	ACTIVE LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

74S182 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS			DM54/74 182 MIN	TYP(1)	MAX	DM74S S182 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage							0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA				−1.5				V
				I_I = −18 mA							−1.2	
I_{OH}	High Level Output Current							−800			−1000	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V	V_{IL} = 0.8V, I_{OH} = Max	DM54	2.4			N/A			V
					DM74	2.4			2.7	3.4		
I_{OL}	Low Level Output Current							16			20	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V	V_{IL} = 0.8V, I_{OL} = Max				0.4			0.5	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V					1			1	mA
I_{IH}	High Level Input Current	C_n Input	V_{CC} = Max	V_I = 2.4V (182)				80			50	μA
		P3 Input		V_I = 2.7V (S182)				120			100	
		P2 Input						160			150	
		P0, P1, or G3 Input						200			200	
		G0 or G2 Input						360			350	
		G1 Input						400			400	
I_{IL}	Low Level Input Current	C_n Input	V_{CC} = Max	V_I = 0.4V (182)				−3.2			−2	mA
		P3 Input		V_I = 0.5V (S182)				−4.8			−4	
		P2 Input						−6.4			−6	
		P0, P1, or G3 Input						−8.0			−8	
		G0 or G2 Input						−14.4			−14	
		G1 Input						−16			−16	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)			−40		−100	−40		−100	mA
I_{CCH}	Supply Current, All Outputs High		V_{CC} = 5V(3)				27			35		mA
I_{CCL}	Supply Current, All Outputs Low		V_{CC} = Max(4)		DM54		45	65	N/A			mA
					DM74		45	72		69	109	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

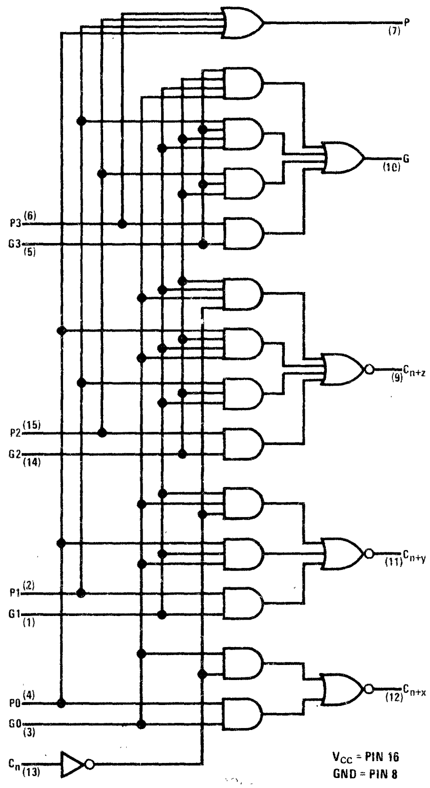
(3) I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.

(4) I_{CCL} is measured with all outputs open; inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

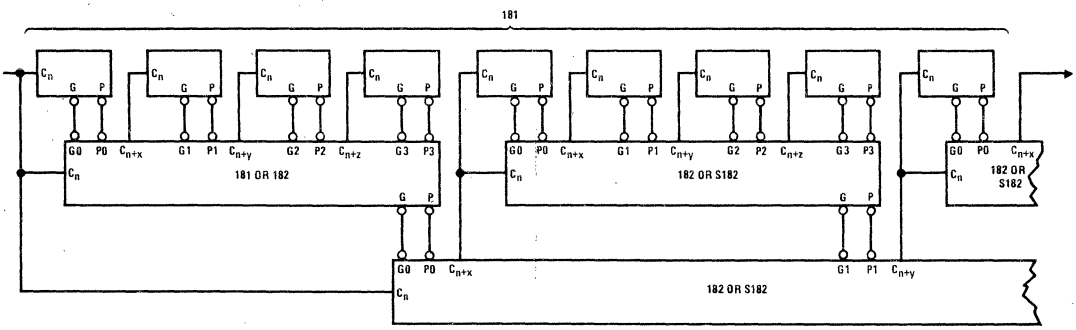
	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74 182 MIN	TYP	MAX	DM74S S182 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	R_L = 400Ω, C_L = 15 pF (182)		11	17		4.5	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	22		4.5	7	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P1, P2, or P3	G			11	17		5	7.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	22		7	10.5	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	P0, P1, P2, or P3	P	R_L = 280Ω, C_L = 15 pF (S182)		11	17		4.5	6.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	22		6.5	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			11	17		6.5	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	22		7	10.5	

Logic Diagram



Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS



A and B inputs, and F outputs of 181 are not shown.

BCD-to-Binary and Binary-to-BCD Converters

General Description

These monolithic converters are derived from the 256-bit read only memories, DM5488 and DM7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1, as shown in the truth tables. These converters demonstrate the versatility of a read only memory in that an unlimited number of reference tables or conversion tables may be built into a system. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

An overriding enable input is provided on each converter which when taken high inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the 185A and all "don't care" conditions of the 184 are programmed high. The outputs are of the open-collector type.

DM54184 AND DM74184 BCD-TO-BINARY CONVERTERS

The 6-bit BCD-to-binary function of the DM54184 and DM74184 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.

b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the DM54184 and DM74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the truth table when the devices are connected as shown.

DM54185A AND DM74185A BINARY-TO-BCD CONVERTERS

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

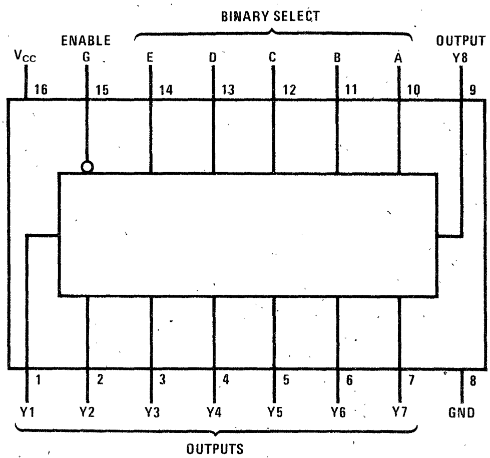
a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.

b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.

c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

(Continued)

Connection Diagram



54184(J), (W); 74184(J), (N), (W);
54185A(J), (W); 74185A(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM54/74 184, 185A MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, V_{OH} = 5.5V			100	μA
I_{OL}	Low Level Output Current				12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 12 mA			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1	mA
I_{CCH}	Supply Current, All Outputs High	V_{CC} = Max		40	65	mA
I_{CCL}	Supply Current, All Programmed Outputs Low	V_{CC} = Max		50	80	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Enable G	C_L = 15 pF, R_{L1} = 400Ω, R_{L2} = 600Ω		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Enable G			20	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Binary Select			20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Binary Select			20	35	ns

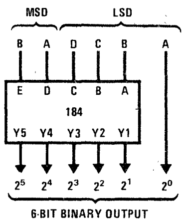
General Description (Continued)

DM54184 AND DM74184 BCD-TO-BINARY

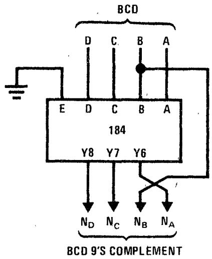
TABLE I
PACKAGE COUNT AND DELAY TIMES FOR BCD-TO-BINARY CONVERSION

INPUT (DECADES)	PACKAGES REQUIRED	TOTAL DELAY TIMES (ns) TYP	MAX
2	2	56	80
3	6	140	200
4	11	196	280
5	19	280	400
6	28	364	520

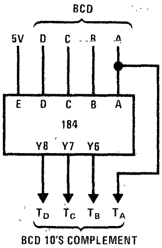
6-BIT CONVERTER



BCD 9'S COMPLEMENT CONVERTER



BCD 10'S COMPLEMENT CONVERTER



Truth Tables

BCD-TO-BINARY CONVERTER

BCD WORDS	INPUTS (See Note A) E	D	C	B	A	G	OUTPUTS (See Note B) Y5	Y4	Y3	Y2	Y1
0 1	L	L	L	L	L	L	L	L	L	L	L
2 3	L	L	L	L	H	L	L	L	L	L	H
4 5	L	L	L	H	L	L	L	L	L	H	L
6 7	L	L	L	H	H	L	L	L	L	H	H
8 9	L	L	H	L	L	L	L	L	H	L	L
10 11	L	H	L	L	L	L	L	L	H	L	H
12 13	L	H	L	L	H	L	L	L	H	H	L
14 15	L	H	L	H	L	L	L	L	H	H	H
16 17	L	H	L	H	H	L	L	H	L	L	L
18 19	L	H	H	L	L	L	L	H	L	L	H
20 21	H	L	L	L	L	L	L	H	L	H	L
22 23	H	L	L	L	H	L	L	H	L	H	H
24 25	H	L	L	H	L	L	L	H	H	L	L
26 27	H	L	L	H	H	L	L	H	H	L	H
28 29	H	L	H	L	L	L	L	H	H	H	L
30 31	H	H	L	L	L	L	L	H	H	H	H
32 33	H	H	L	L	H	L	H	L	L	L	L
34 35	H	H	L	H	L	L	H	L	L	L	H
36 37	H	H	L	H	H	L	H	L	L	H	L
38 39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	H	H	H	H	H

BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

BCD WORD	INPUTS (See Note C) E†	D	C	B	A	G	OUTPUTS (See Note D) Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Notes:

(A) Input conditions other than those shown produce highs at outputs Y1 through Y5.

(B) Output Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

(C) Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

(D) Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

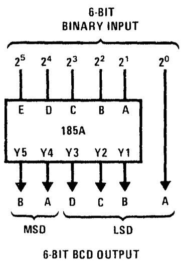
General Description (Continued)

DM54185A AND DM74185A BINARY-TO-BCD

TABLE II
PACKAGE COUNT AND DELAY TIMES
FOR BINARY-TO-BCD CONVERSION

INPUT (BITS)	PACKAGES REQUIRED	TOTAL DELAY TIME (ns)	
		TYP	MAX
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-BIT CONVERTER



Truth Tables (Continued)

BINARY WORDS	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2 3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4 5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12 13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14 15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22 23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24 25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26 27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28 29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30 31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32 33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34 35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36 37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38 39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42 43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44 45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46 47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48 49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50 51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52 53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54 55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56 57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58 59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60 61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62 63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Typical Applications

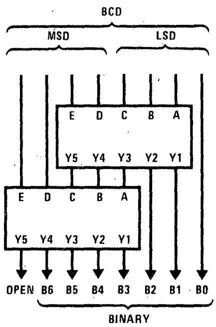


FIGURE 1: BCD-TO-BINARY CONVERTER FOR TWO BCD DECADES

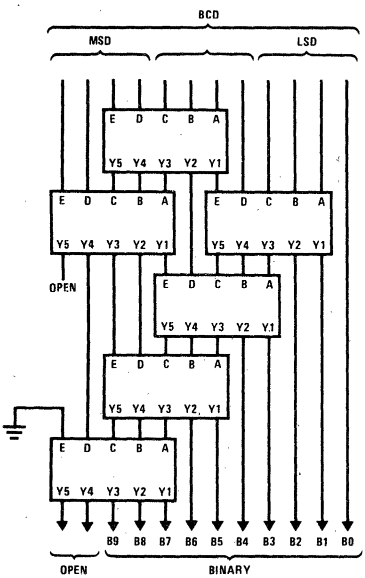


FIGURE 2: BCD-TO-BINARY CONVERTER FOR THREE BCD DECADES

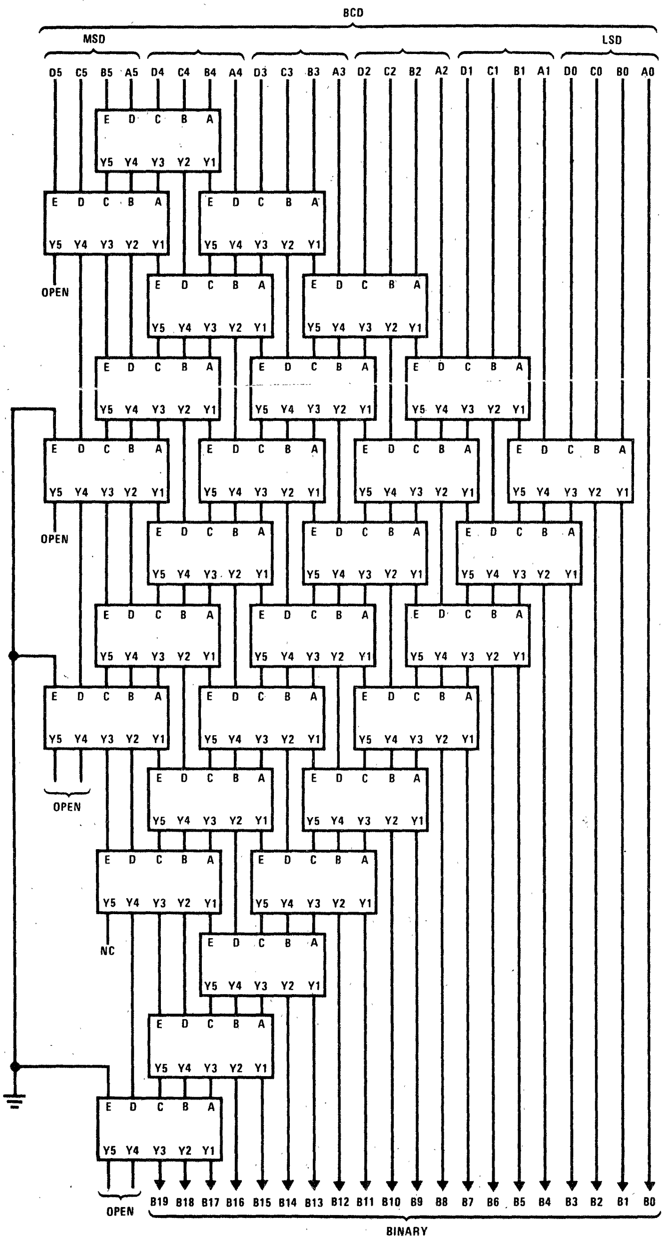


FIGURE 3: BCD-TO-BINARY CONVERTER FOR SIX BCD DECADES

MSD — Most significant decade
LSD — Least significant decade
Each rectangle represents a DM54184 or DM74184

Typical Applications (Continued)

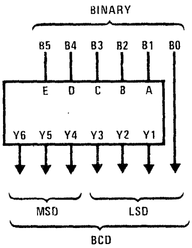


FIGURE 4: 6-BIT BINARY-TO-BCD CONVERTER

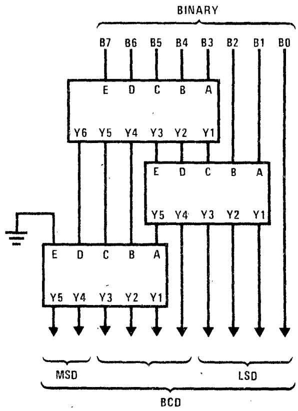


FIGURE 5: 8-BIT BINARY-TO-BCD CONVERTER

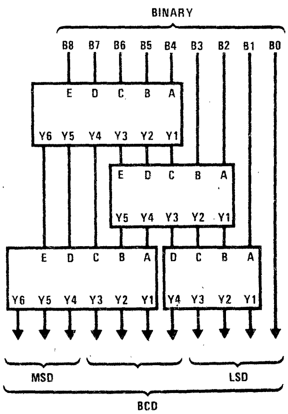


FIGURE 6: 9-BIT BINARY-TO-BCD CONVERTER

MSD — Most significant decade
LSD — Least significant decade

Notes

(A) Each rectangle represents a DM54185A or a DM74185A.
(B) All unused E inputs are grounded.

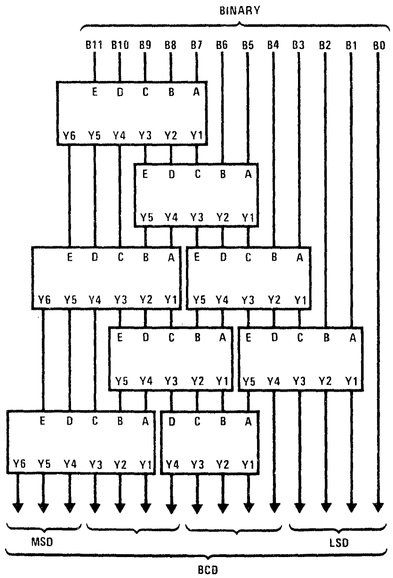


FIGURE 7: 12-BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

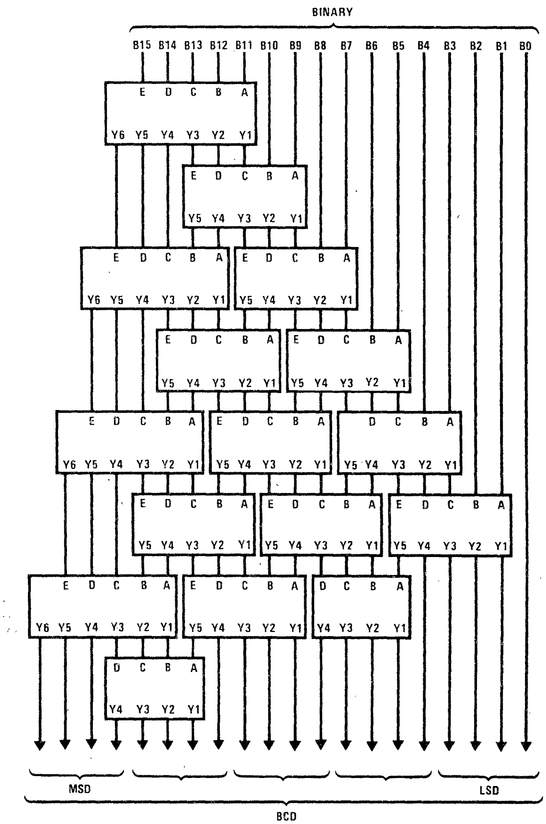


FIGURE 8: 16-BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

1024-Bit Read Only Memories

General Description

These circuits are custom-programmed, 1024-bit read only memories organized as 256 words of four bits each. These high-speed TTL memory arrays are addressed in straight eight-bit binary, with full on-chip decoding. Two overriding memory-enable inputs are provided which, when either one or both are taken high, will inhibit the function causing all four outputs to remain high (off). Data, as specified by the customer, are permanently programmed into the 1024-bit locations. This organization is expandable to 41,472 words of n-bits, with no additional output buffering.

The address of a four-bit word is accomplished through the buffered binary select inputs, with low-level voltages at both enable inputs. The most significant binary select inputs, D through H, are decoded internally in the X plane to select one-of-32 lines, and the least significant bits, A, B, and C, are internally decoded in the Y plane to accomplish one-of-eight decoding to drive the four output buffers. Where multiple devices are used in a memory system, the enable input allows easy decoding of additional address bits.

Data are programmed into the memory cell at the emitters of a 32-by-32 matrix of transistors. In the X plane each of the 32 address decoding gate outputs supply common base drive to 32 transistors. In the Y plane the 32 transistors are arranged into four groups of eight. This permits each of the bit lines to be terminated in four one-of-eight decoders, which achieves the four-bit word length.

The open-collector outputs are capable of sinking 16 milliamperes of current and may be wire-AND connected to increase the number of words available. An external pull-up resistor is recommended for definition of the high (off) level output voltage.

The customer can specify the output logic level desired at each of the 1024 bit locations by completing the supplementary ordering data and a set of data cards, punched in accordance with the data format shown under ordering instructions. It is important that the customer specify not only the output levels desired at all 1024 bit locations, but also the other information requested.

WORD SELECTION

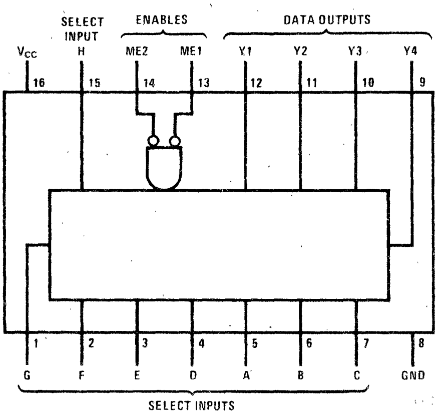
Word selection is accomplished in a conventional 8-bit positive-logic binary code with the A select input being the least-significant bit progressing alphabetically through the select inputs to H which is the most-significant bit.

Features

- Organized as 256 words by 4 bits
- Ideal for microprogramming, reference tables and code converters
- Easily expandable
- Fully decoded, buffered inputs
- Diode-clamped inputs
- Full fan-out, open-collector outputs

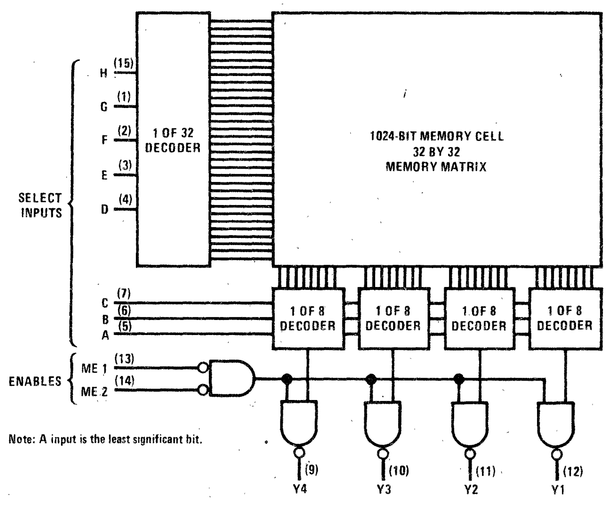
TYPE	TYPICAL ACCESS TIME	TYPICAL POWER DISSIPATION
187	37 ns	0.36 mW/Bit
L187A	90 ns	0.09 mW/Bit

Connection Diagram



54187(J); 74187(J), (N);
54L187A/74L187A(J), (N), (W)

Logic Diagram



Note: A input is the least significant bit.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 187 MIN	DM54/74 187 TYP(1)	DM54/74 187 MAX	DM54L/74L L187A MIN	DM54L/74L L187A TYP(1)	DM54L/74L L187A MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, V_{OH} = 5.5V				40			50	μA
V_{OH}	High Level Output Voltage					5.5			5.5	V
I_{OL}	Low Level Output Current		DM54			16			2.0	mA
			DM74			16			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OL} = Max	DM54			0.4			0.3	V
			DM74			0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V						−0.18	mA
			V_I = 0.4V			−1				mA
I_{CC}	Supply Current	V_{CC} = Max(2)			75	110		18	25	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) With outputs open and both ME inputs grounded, I_{CC} is measured first by selecting a word which contains the maximum number of programmed high level outputs, then by selecting a word which contains the maximum number of programmed low level outputs.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	DM54/74 187 CONDITIONS	MIN	TYP	MAX	DM54L/74L L187A CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Enable	C_L = 30 pF to GND R_{L1} = 300Ω to V_{CC} R_{L2} = 600Ω to GND		20	30	C_L = 15 pF R_L = 2 kΩ		85	130	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Enable			20	30			46	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Select			36	60			120	180	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Select			37	60			65	98	ns

Ordering Instructions

Programming instructions for the 187 or L187A are solicited in the form of a sequenced deck of 32 standard 80 column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the levels at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

Ordering Instructions (Continued)

DATA CARD FORMAT

Column	
1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8- 9	Blank
10-13	Punch "H," "L," or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high voltage level output, L = low voltage level output, X = don't care.
14	Blank
15-18	Punch "H," "L," or "X" for the second set of outputs.
19	Blank
20-23	Punch "H," "L," or "X" for the third set of outputs.
24	Blank
25-28	Punch "H," "L," or "X" for the fourth set of outputs.
29	Blank
30-33	Punch "H," "L," or "X" for the fifth set of outputs.
34	Blank
35-38	Punch "H," "L," or "X" for the sixth set of outputs.
39	Blank
40-43	Punch "H," "L," or "X" for the seventh set of outputs.
44	Blank
45-48	Punch "H," "L," or "X" for the eighth set of outputs.
49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53–55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "DM"
62-66	Punch a left-justified integer representing the National Semiconductor part number, 54187, 54L187A, 74187, or 74L187A.
67-70	Blank

TRI-STATE 64-Bit Read/Write Memories

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four-bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of open-collector with the speed of a totem-pole output. It can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristics of the TTL totem-pole output. Systems utilizing data-bus lines with a defined pull-up impedance can employ the open-collector DM54S289/DM74S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of these outputs are bus-connected, the high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

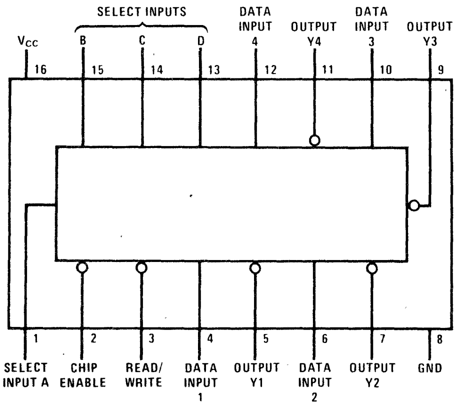
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs will be in the high-impedance state.

The fast access time of the DM54S189 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 ns. The high capacitive-drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM54S189 outputs being at a high impedance during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Features

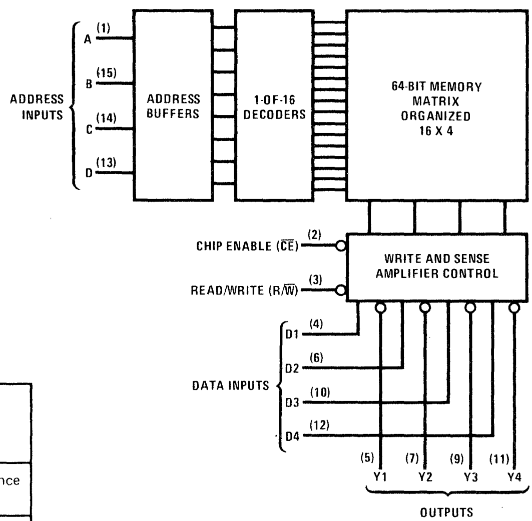
- Schottky-clamped for high-speed applications:
  - access from chip-enable input 12 ns typ
  - access from address inputs 25 ns typ
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- DM54S289/DM74S289 are functionally equivalent, have open-collector outputs, and are compatible with Intel 3101A in most applications
- Chip-enable input simplifies system decoding

Connection Diagram



54S189(J); 74S189(J), (N)

Logic Diagram



Truth Table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/WRITE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = High Level
L = Low Level
X = Don't Care

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM54S189			DM74S189			UNITS
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2			−1.2	V
I_{OH}	High Level Output Current				−2.0			−6.5	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max	2.4	3.4		2.4	3.2		V
I_{OL}	Low Level Output Current				16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA			0.50			0.45	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V; V_O = 0.45V		−50			−50		μA
		V_O = 2.4V		50			50		
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			25			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V			−0.25			−0.25	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−30		−100	−30		−100	mA
I_{CC}	Supply Current	V_{CC} = Max		75	110		75	110	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

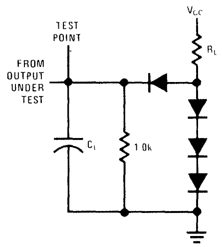
(2) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER		CONDITIONS	DM54S189			DM74S189			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Access Time From Address				25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level from Chip Enable		C_L = 30 pF, R_L = 280Ω		12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level from Read/Write				22	40		22	35	ns
t_{CZL}	Output Enable Time to Low Level from Chip Enable				22	40		22	35	ns
t_{WZL}	Output Enable Time to Low Level from Read/Write				22	40		22	35	ns
t_{CHZ}	Output Disable Time from High Level from Chip Enable		C_L = 5 pF, R_L = 280Ω		12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level from Read/Write				12			12		ns
t_{CLZ}	Output Disable Time from Low Level from Chip Enable				12	25		12	17	ns
t_{WLZ}	Output Disable Time from Low Level from Read/Write				12			12		ns
t_{WP}	Width of Write-Enable Pulse			25			25			ns
t_{ASW}	Setup Time	Address		0			0			ns
t_{CSW}		Chip Enable		0			0			
t_{DSW}		Data		25			25			
t_{AHW}	Hold Time	Address		0			0			ns
t_{CHW}		Chip Enable		0			0			
t_{DHW}		Data		0			0			

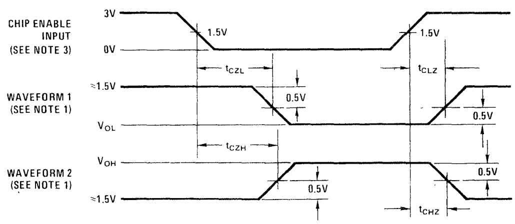
Parameter Measurement Information

LOAD CIRCUIT

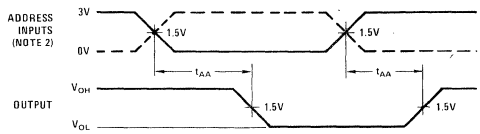


C_L includes probe and jig capacitance.
All diodes are 1N3064.

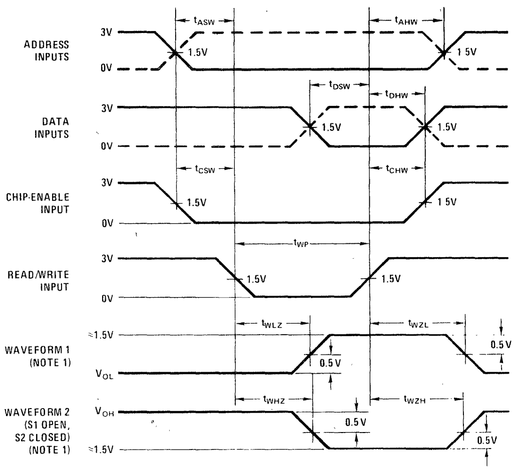
ENABLE AND DISABLE TIME FROM CHIP ENABLE



ACCESS TIME FROM ADDRESS INPUTS



WRITE CYCLE



Notes

(1) Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

(2) When measuring delay times from address inputs, the chip enable input is low and the read/write input is high.

(3) When measuring delay times from chip enable input, the address inputs are steady-state and the read/write input is high.

(4) Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{OUT} \approx 50\Omega$.

Synchronous Up/Down Counters with Mode Control

General Description

These circuits are synchronous, reversible, up/down counters. The 191 and LS191 are 4-bit binary counters and the 190 and LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

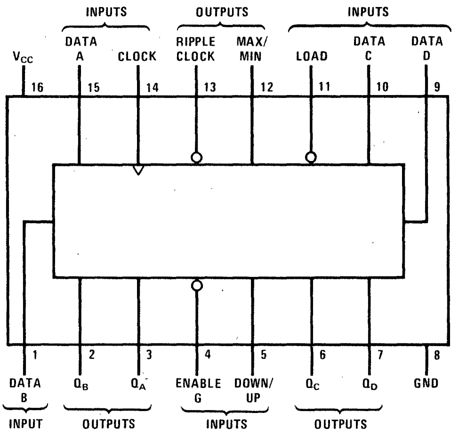
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Counts 8-4-2-1 BCD or binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications

TYPE	AVERAGE PROPAGATION DELAY	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
190, 191	20 ns	25 MHz	325 mW
LS190, LS191	20 ns	25 MHz	100 mW

Connection Diagram



Asynchronous inputs: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

54190/74190(J), (N), (W); 54LS190/74LS190(J), (N), (W); 54191/74191(J), (N), (W); 54LS191/74LS191(J), (N), (W)

LS190, LS191 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS			DM54/74 190, 191 MIN	DM54/74 190, 191 TYP(1)	DM54/74 190, 191 MAX	DM54LS/74LS LS190, LS191 MIN	DM54LS/74LS LS190, LS191 TYP(1)	DM54LS/74LS LS190, LS191 MAX	UNITS
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.8			0.7	V
					DM74			0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA				−1.5				V
				I_I = −18 mA							−1.5	V
I_{OH}	High Level Output Current							−800			−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.5	3.4		V
					DM74	2.4	3.4		2.7	3.4		V
I_{OL}	Low Level Output Current				DM54			16			4	mA
					DM74			16			8	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.25	0.4	V
				I_{OL} = Max	DM74		0.2	0.4		0.35	0.5	V
				I_{OL} = 4 mA	DM74						0.4	V
I_I	Input Current at Maximum Input Voltage	Enable	V_{CC} = Max	V_I = 5.5V				1				mA
		Enable		V_I = 7V							0.3	mA
		Others		V_I = 5.5V				1				mA
		Others		V_I = 7V							0.1	mA
I_{IH}	High Level Input Current	Enable	V_{CC} = Max	V_I = 2.4V				120				μA
		Enable		V_I = 2.7V							60	μA
		Others		V_I = 2.4V				40				μA
		Others		V_I = 2.7V							20	μA
I_{IL}	Low Level Input Current	Enable	V_{CC} = Max, V_I = 0.4V					−4.8			−1.08	mA
		Others						−1.6			−0.4	mA
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		DM54	−20		−65	−30		−130	mA
					DM74	−18		−65	−30		−130	mA
I_{CC}	Supply Current		V_{CC} = Max(3)		DM54		65	99		20	35	mA
					DM74		65	105		20	35	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

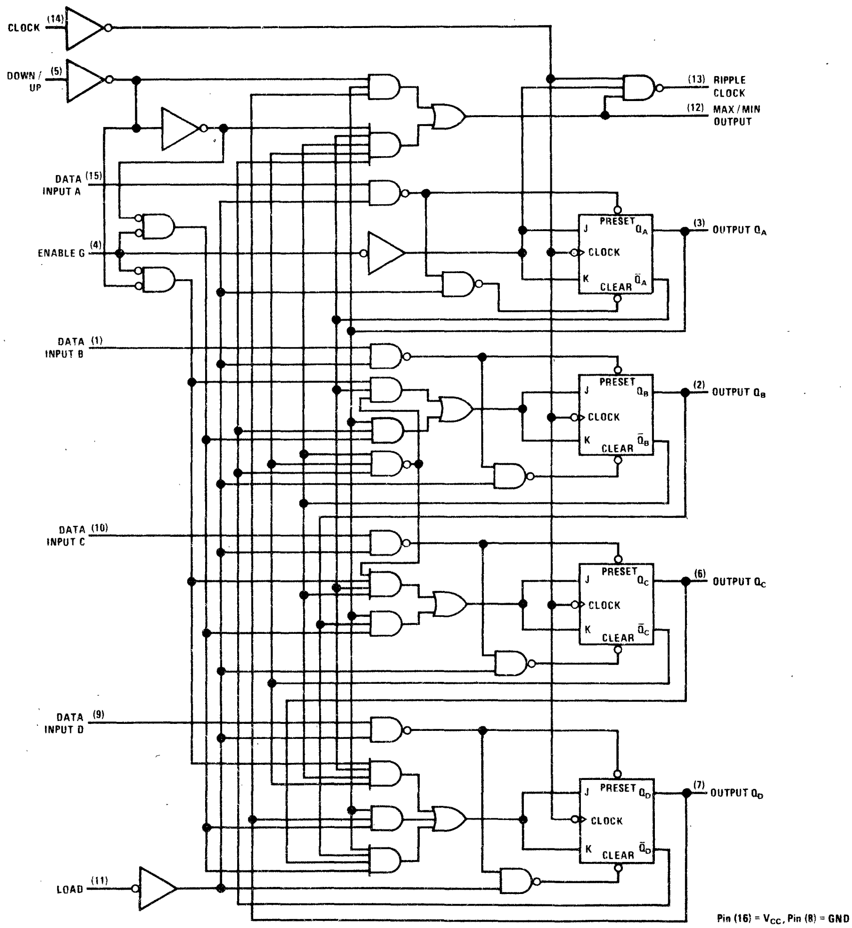
(3) I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74 190, 191 MIN	DM54/74 190, 191 TYP	DM54/74 190, 191 MAX	DM54LS/74LS LS190, LS191 MIN	DM54LS/74LS LS190, LS191 TYP	DM54LS/74LS LS190, LS191 MAX	UNITS
f_{MAX}	Maximum Clock Frequency			$C_L = 15$ pF, $R_L = 400\Omega$ (54/74) $C_L = 15$ pF $R_L = 2$ kΩ (54LS/74LS)	20	25		20	25		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Load	Q_A, Q_B, Q_C, Q_D			22	33		22	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Load	Q_A, Q_B, Q_C, Q_D			33	50		33	50	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			14	22		14	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			35	50		35	50	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Ripple Clock			13	20		13	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock	Ripple Clock			16	24		16	24	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Q_A, Q_B, Q_C, Q_D			16	24		16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock	Q_A, Q_B, Q_C, Q_D			24	36		24	36	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Max/Min			28	42		28	42	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock	Max/Min			37	52		37	52	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Down/Up	Ripple Clock			30	45		30	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Down/Up	Ripple Clock			30	45		30	45	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Down/Up	Max/Min			21	33		21	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Down/Up	Max/Min			22	33		22	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Ripple Clock						21	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable	Ripple Clock						22	33	ns
$t_{W(CLOCK)}$	Width of Clock Input Pulse				25			25			ns
$t_{W(LOAD)}$	Width of Load Input Pulse				35			35			ns
t_{SETUP}	Data Setup Time				20			20			ns
t_{HOLD}	Data Hold Time				0			0			ns
t_{ENABLE}	Enable Time to Clock							30			ns

Logic Diagrams

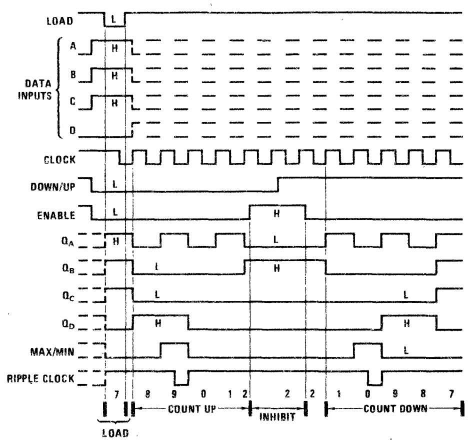
190, LS190 DECADE COUNTERS



Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

190, LS190 DECADE COUNTERS
TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES



Sequence:

(1) Load (preset) to BCD seven

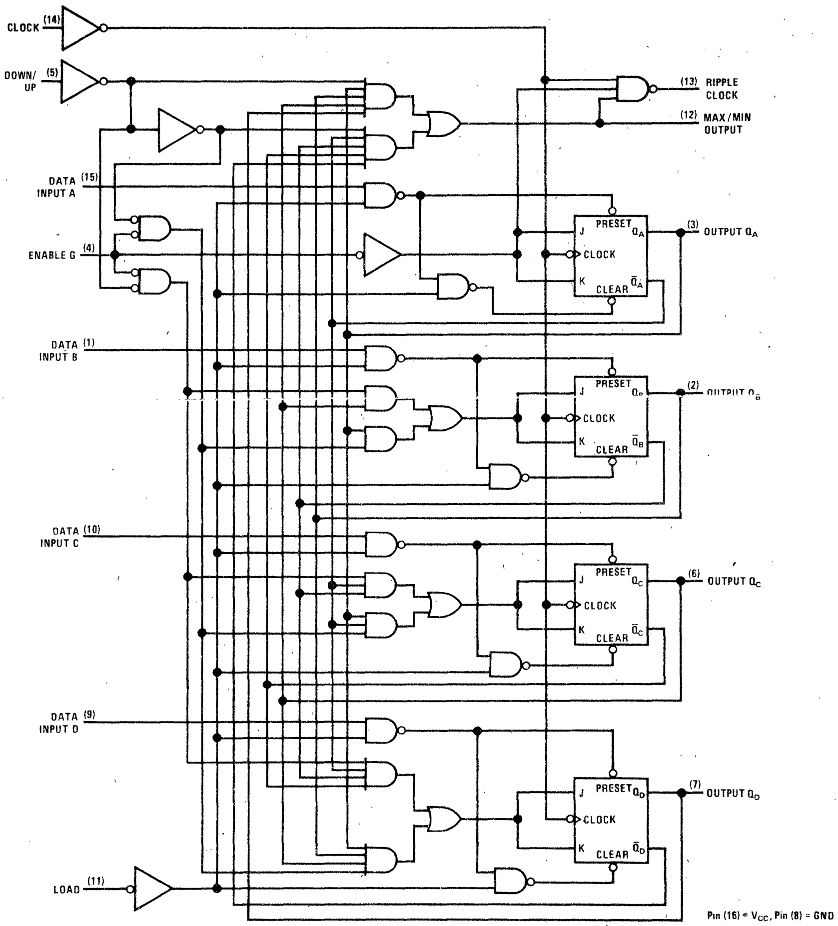
(2) Count up to eight, nine, zero, one, and two

(3) Inhibit

(4) Count down to one, zero, nine, eight, and seven

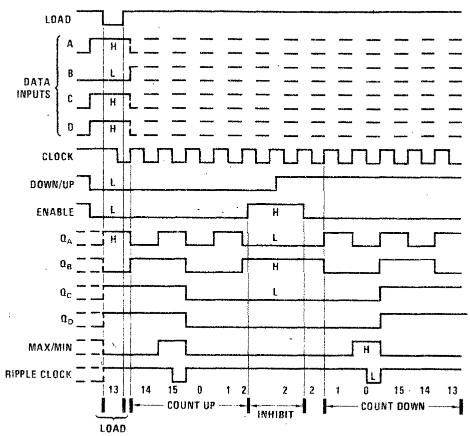
Logic Diagrams (Continued)

191, LS191 BINARY COUNTERS



Timing Diagrams (Continued)

191, LS191 DECODE COUNTERS TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES



Sequence:

(1) Load (preset) to binary thirteen

(2) Count up to fourteen, fifteen, zero, one, and two

(3) Inhibit

(4) Count down to one, zero, fifteen, fourteen, and thirteen

Synchronous Up/Down Counters with Dual Clock

General Description

These circuits are synchronous up/down counters; the 192, L192 and LS192 circuits are BCD counters and the 193, L193 and LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

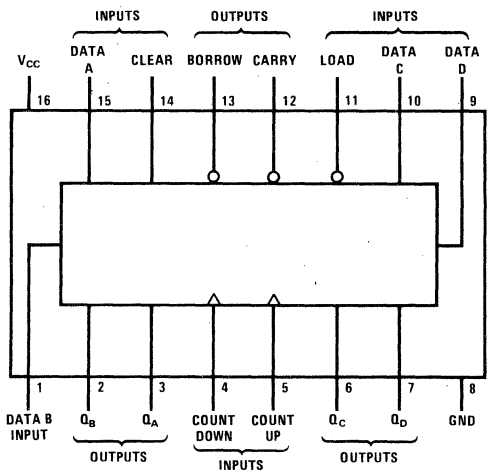
These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

TYPE	TYPICAL COUNT FREQUENCY	TYPICAL POWER DISSIPATION
192, 193	25 MHz	325 mW
L192, L193	12 MHz	40 mW
LS192, LS193	32 MHz	95 mW

Connection Diagram



Note: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D.

54192(J), (W); 74192(J), (N), (W); 54L192/74L192(J), (N), (W); 54LS192/74LS192(J), (N), (W); 54193(J), (W); 74193(J), (N), (W); 54L193/74L193(J), (N), (W); 54LS193/74LS193(J), (N), (W)

LS192, LS193 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 192, 193 MIN	TYP(1)	MAX	DM54L/74L L192, L193 MIN	TYP(1)	MAX	DM54LS/74LS LS192, LS193 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7			0.7	V
			DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5				V
		V_{CC} = Min, I_I = −18 mA										−1.5	
I_{OH}	High Level Output Current					−400			−200			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	DM54	2.4			2.4			2.5	3.4		V
			DM74	2.4			2.4			2.7	3.4		
I_{OL}	Low Level Output Current		DM54			16			2			4	mA
			DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM54			0.4		0.15	0.3		0.25	0.4	V
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM74			0.4		0.2	0.4		0.35	0.5	
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = 4 mA	DM74									0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			0.1				mA
		V_{CC} = Max, V_I = 7V										0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40		<1	10				μA
		V_{CC} = Max, V_I = 2.7V										20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V						−0.10	−0.18				mA
		V_{CC} = Max, V_I = 0.4V				−1.6						−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM54	−20		−55	−3	−9	−15	−30		−130	mA
			DM74	−18		−55	−3	−9	−15	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max(3)	DM54		65	89		8	13		19	34	mA
			DM74		65	102		8	13		19	34	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

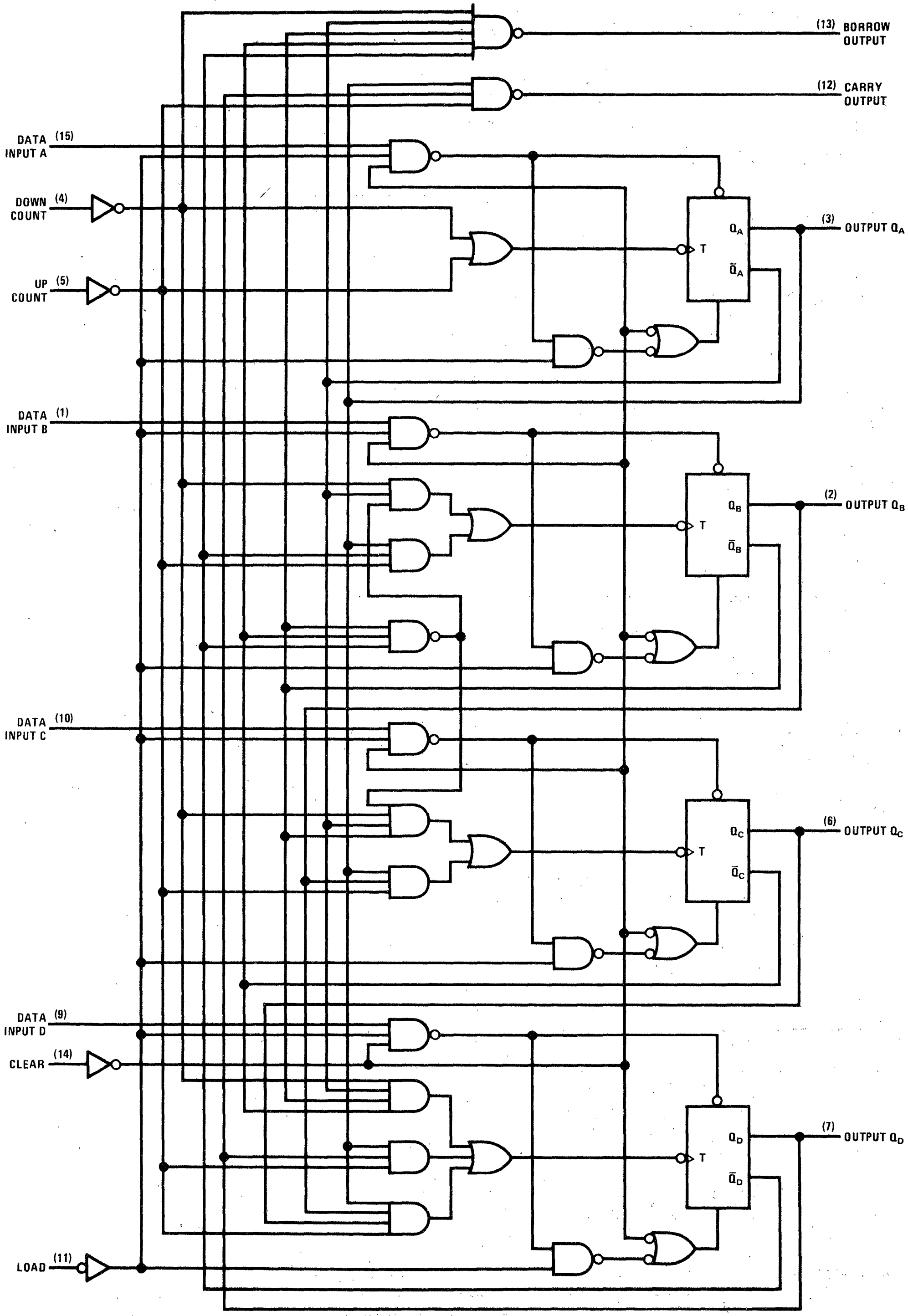
(3) I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM INPUT	TO OUTPUT	DM54/74 192, 193				DM54L/74L L192, L193				DM54LS/74LS LS192, LS193				UNITS
				CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	
f_{MAX}	Maximum Clock Frequency			C_L = 15 pF, R_L = 400Ω	20	25		C_L = 50 pF, R_L = 4 kΩ	6	12		C_L = 15 pF, R_L = 2 kΩ	25	32		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Count up	Carry			17	26			30	60			17	26	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Count up	Carry			16	24			60	120			21	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Count down	Borrow			16	24			30	60			16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Count down	Borrow			16	24			50	100			21	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Either Count	Q			25	38			45	90			25	38	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Either Count	Q			31	47			75	150			31	47	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Load	Q			27	40			55	110			27	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Load	Q			29	40			105	200			29	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Q			22	35			95	190			22	35	ns
t_W	Width of Any Input Pulse				25				70				20			ns
t_{SETUP}	Data Setup Time				20				30				20			ns
t_{HOLD}	Data Hold Time				0				0				0			ns

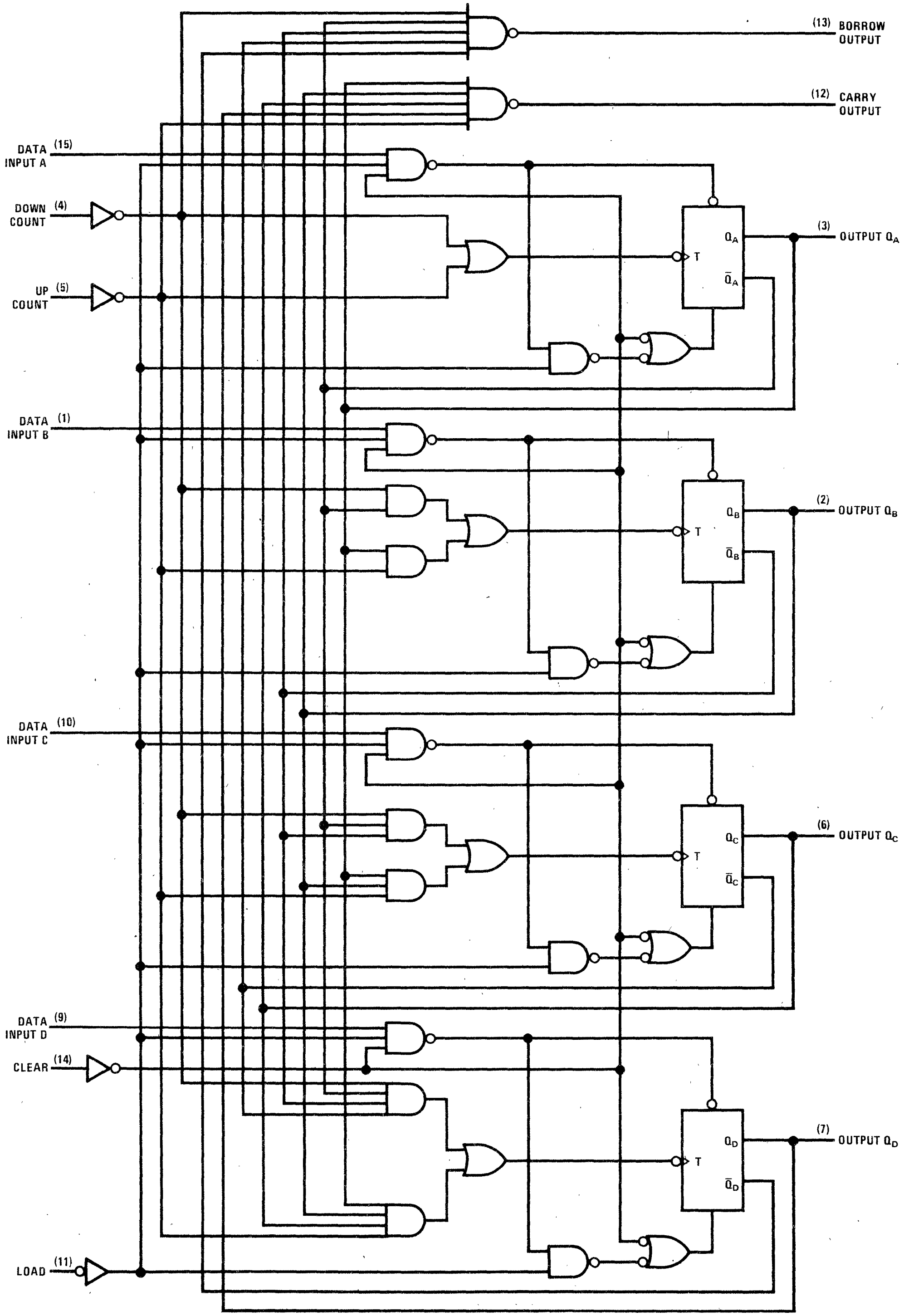
Logic Diagrams

192, L192, LS192



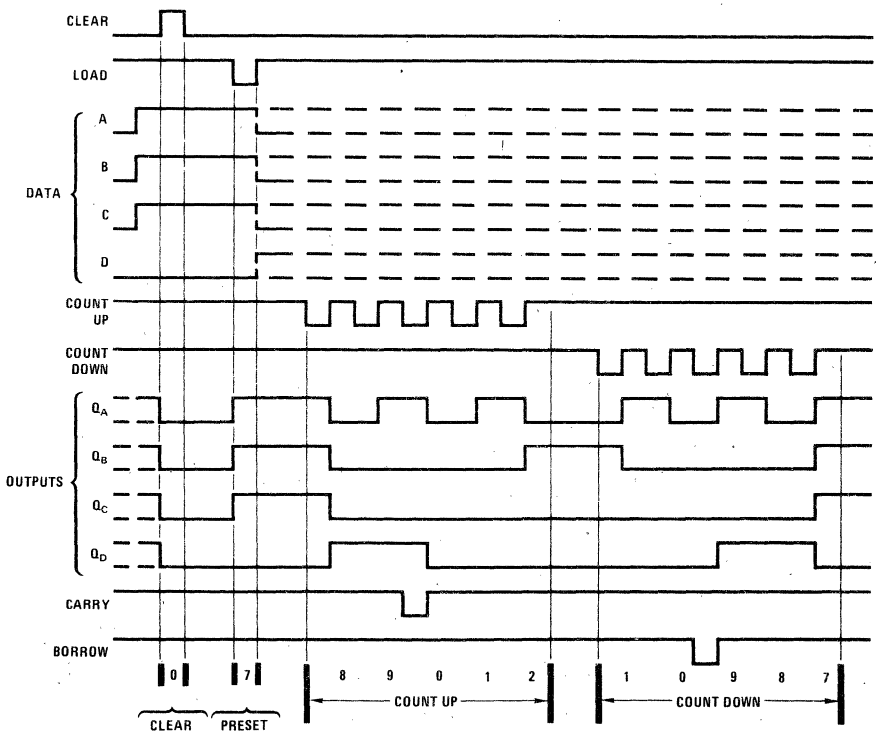
Logic Diagrams (Continued)

193, L193, LS193



Timing Diagrams

192, L192, LS192 DECADE COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



Sequence:

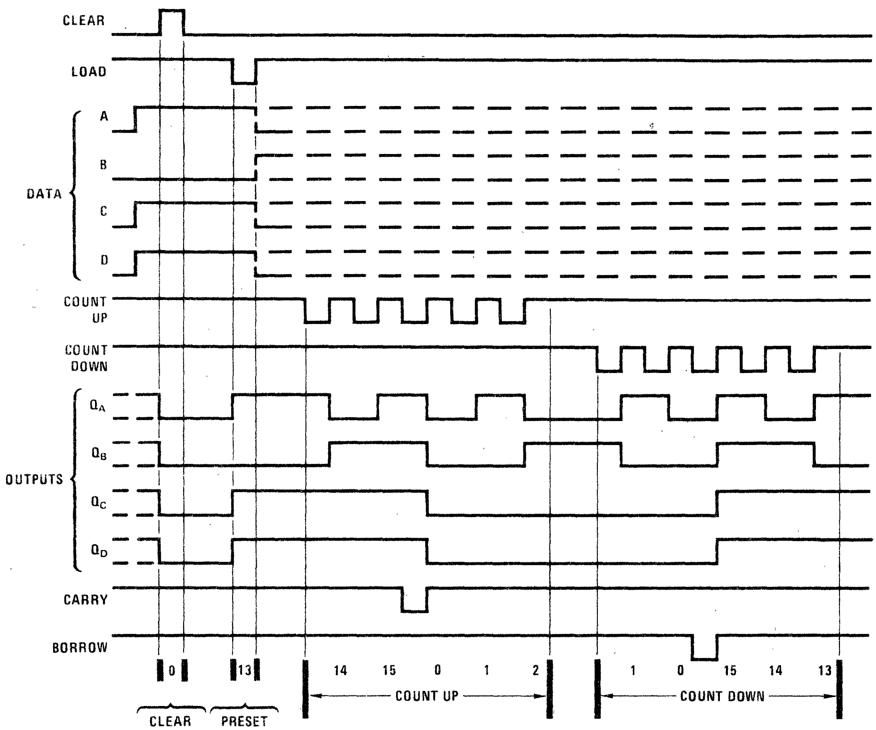
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one, and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

Notes:

(A) Clear overrides load, data, and count inputs.
(B) When counting up, count-down input must be high; when counting down, count-up input must be high.

Timing Diagrams (Continued)

193, L193, LS193 BINARY COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



Sequence:

(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Notes:

(A) Clear overrides load, data, and count inputs.
(B) When counting up, count-down input must be high; when counting down, count-up input must be high.

4-Bit Bidirectional Universal Shift Registers

General Description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

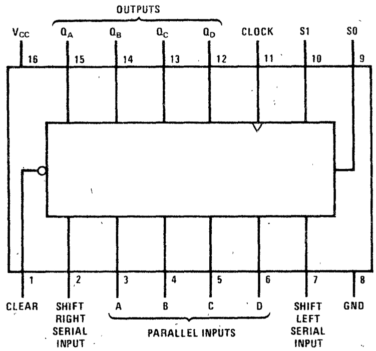
Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the DM54194/DM74194 should be changed only while the clock input is high.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

TYPE	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
194	36 MHz	195 mW
LS194A	36 MHz	75 mW
S194	105 MHz	425 mW

Connection Diagram



54194(J), (W); 74194(J), (N), (W); 54LS194A/74LS194A(J), (N), (W); 74S194(N)

Truth Table

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS			DM54/74 194 MIN	DM54/74 194 TYP(1)	DM54/74 194 MAX	DM54LS/74LS LS194A MIN	DM54LS/74LS LS194A TYP(1)	DM54LS/74LS LS194A MAX	DM74S S194 MIN	DM74S S194 TYP(1)	DM74S S194 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			N/A	V
				DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5							V
			I_I = −18 mA							−1.5			−1.2	
I_{OH}	High Level Output Current						−800			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.5	3.5			N/A		V
				DM74	2.4	3.4		2.7	3.5		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			4			N/A	mA
				DM74			16			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.25	0.4			N/A	V
				DM74		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74					0.25	0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1						1	mA
			V_I = 7V							0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40						50	μA
			V_I = 2.7V							20				
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−1.6			−0.4			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−57	−30		−130		N/A		mA
				DM74	−18		−57	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max(3)				39	63		15	23		85	135	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS or DM74S duration of short circuit should not exceed one second.

(3) With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5V applied to clock.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER		DM54/74 194 CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS194A CONDITIONS	MIN	TYP	MAX	DM74S S194 CONDITIONS	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency		$C_L = 15$ pF, $R_L = 400\Omega$	25	36		$C_L = 15$ pF, $R_L = 2$ kΩ	25	36		$C_L = 15$ pF, $R_L = 280\Omega$	70	105		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clear				19	30			19	30			12.5	18.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock				14	22			14	22		4	8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock				14	22			17	22		4	11	16.5	ns
$t_{W(CLOCK)}$	Width of Clock Pulse			20				20				7			ns
$t_{W(CLEAR)}$	Width of Clear Pulse			20				20				12			ns
t_{SETUP}	Setup Time	Mode Control		30				30				11			ns
		Serial and Parallel Data		20				20				5			ns
		Clear Inactive State		25				25				9			ns
t_{HOLD}	Hold Time at Any Input			0				0				3			ns

Logic Diagrams

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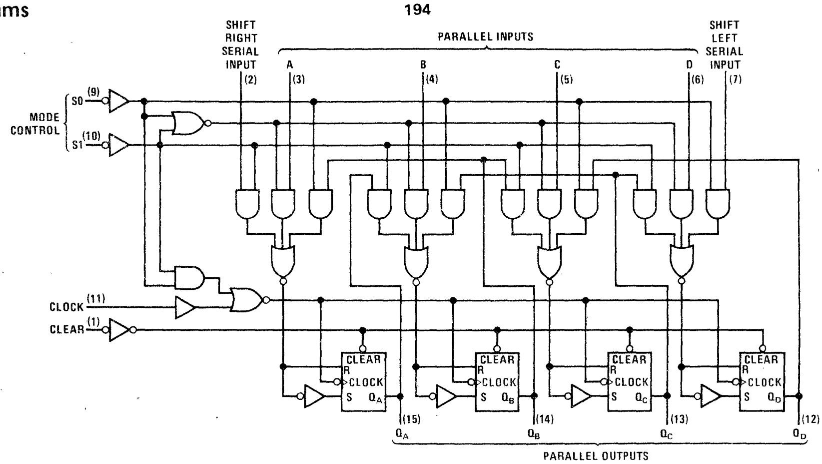
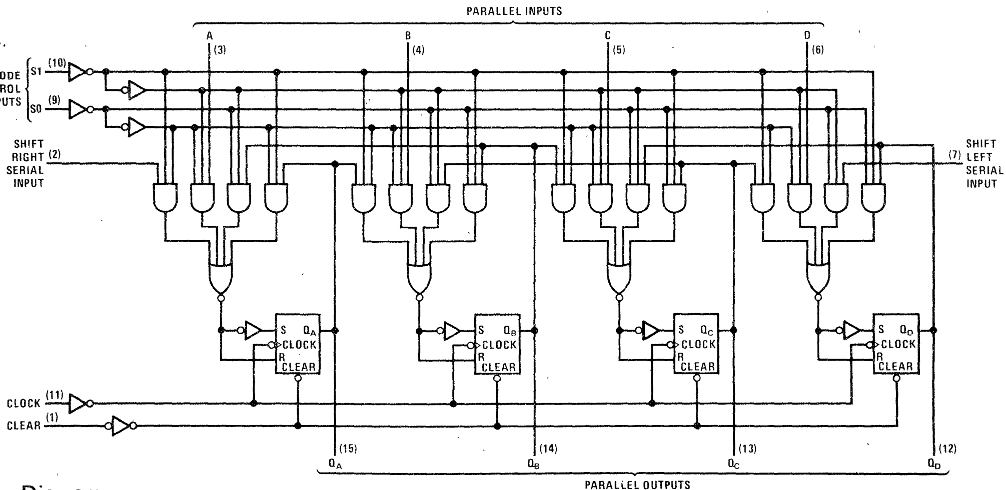
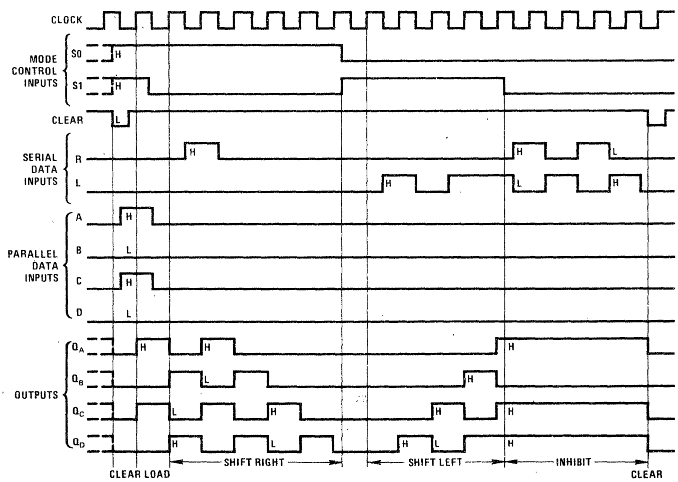


LS194A, S194



Timing Diagram

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES



4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

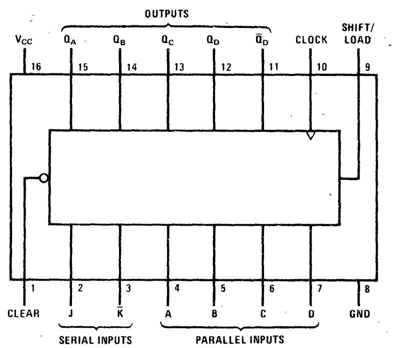
The high-performance S195, with a 105 MHz typical shift frequency, is particularly attractive for very high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters

TYPE	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
195	39 MHz	195 mW
LS195A	39 MHz	70 mW
S195	105 MHz	350 mW

Connection Diagram



54195(J), (W); 74195(J), (N), (W); 54LS195A/74LS195A(J), (N), (W); 74S195(N)

Truth Table

INPUTS									OUTPUTS				
CLEAR	SHIFT/LOAD	CLOCK	SERIAL J	SERIAL $\overline{K}$	PARALLEL A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a, b, c, d = The level of steady state input at A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, or Q_C, respectively, before the most recent transition of the clock.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 195 MIN	DM54/74 195 TYP(1)	DM54/74 195 MAX	DM54LS/74LS LS195A MIN	DM54LS/74LS LS195A TYP(1)	DM54LS/74LS LS195A MAX	DM74S S195 MIN	DM74S S195 TYP(1)	DM74S S195 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7			N/A	V
			DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5							V
		V_{CC} = Min, $I_I = -18$ mA							−1.5			−1.2	
I_{OH}	High Level Output Current					−800			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	DM54	2.4	3.4		2.5	3.4			N/A		V
			DM74	2.4	3.4		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current		DM54			16			4			N/A	mA
			DM74			16			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM54		0.2	0.4		0.25	0.4			N/A	V
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM74		0.2	0.4		0.35	0.5			0.5	
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = 4 mA	DM74					0.25	0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1						1	mA
		V_{CC} = Max, V_I = 7V							0.1				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40							μA
		V_{CC} = Max, V_I = 2.7V							20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6			−0.4				mA
		V_{CC} = Max, V_I = 0.5V										−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM54	−20		−57	−30		−130		N/A		mA
			DM74	−18		−57	−30		−130	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max(3)			39	63		14	21		70	109	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

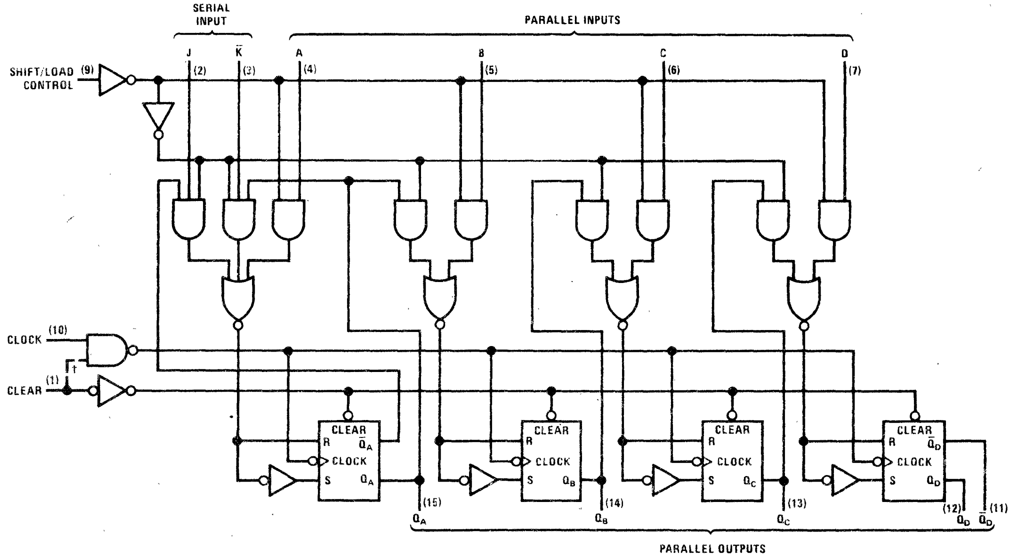
(2) Not more than one output should be shorted at a time, and for DM54LS/74LS or DM74S duration of short circuit should not exceed one second.

(3) With all outputs open, shift/load grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to clear and then applying a momentary ground, followed by 4.5V, to clock.

Switching Characteristics $V_{CC} = 5V, T_A = 25^{\circ}C$

PARAMETER			DM54/74 195 CONDITIONS	MIN	TYP	MAX	DM54LS/74LS LS195 CONDITIONS	MIN	TYP	MAX	DM74S S195 CONDITIONS	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency		$C_L = 15$ pF, $R_L = 400\Omega$	30	39		$C_L = 15$ pF, $R_L = 2$ kΩ	30	39		$C_L = 15$ pF, $R_L = 280\Omega$	70	105		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clear				19	30			19	30			12.5	18.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock				14	22			14	22			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock				17	26			17	26			11	16.5	ns
$t_{W(CLOCK)}$	Width of Clock Input Pulse			16				16				7			ns
$t_{W(CLEAR)}$	Width of Clear Input Pulse			12				12				12			ns
t_{SETUP}	Setup Time	Shift/Load		25				25				11			ns
		Serial and Parallel Data		15				15				5			
		Clear Inactive-State		25				25				9			
$t_{RELEASE}$	Shift/Load Release Time					10				10				6	ns
t_{HOLD}	Serial and Parallel Data Hold Time			0				0				3			ns

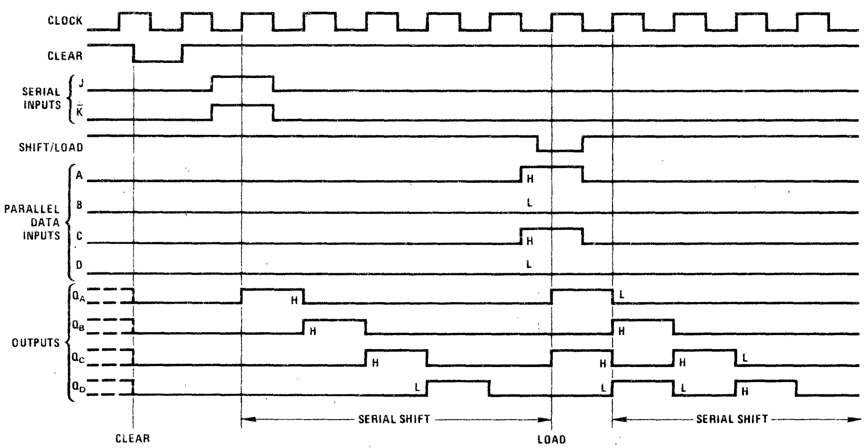
Logic Diagram



†This connection is made on 195 only.

Timing Diagram

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



8-Bit Shift Registers

General Description

These 8-bit shift registers feature buffered inputs to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes to minimize switching transients and simplify system design. Maximum input clock frequency is typically 35 MHz and power dissipation is typically 360 mW.

DM54198/DM74198

These bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. They feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_H)
Shift left (in the direction Q_H toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S0 and S1 high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

DM54199/DM74199

These registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

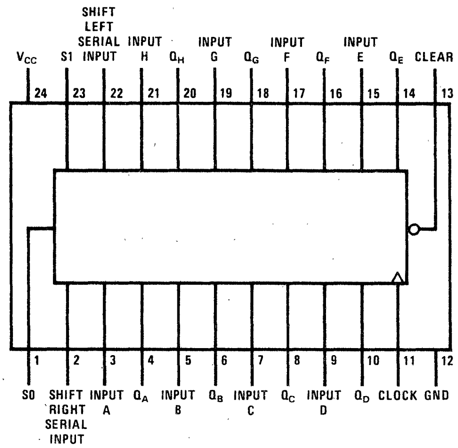
Parallel (broadside) load
Shift (in the direction Q_A toward Q_H)
Inhibit clock (do nothing)

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

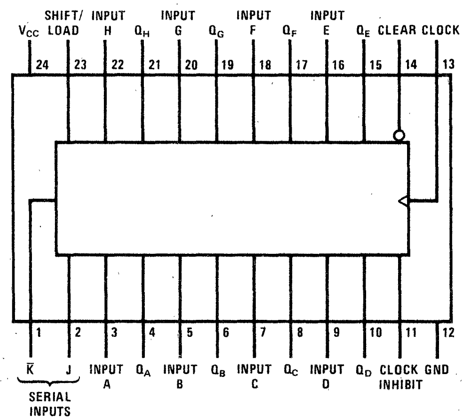
Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-$\overline{K}$ inputs. See the truth table for levels required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either clock input high inhibits clocking; but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

Connection Diagrams



54198/74198(J), (N)



54199/74199(J), (N)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 198, 199 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −800μA		2.4			V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (See Conditions for I_{CC} Table)	DM54		72	104	mA
			DM74		72	116	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	DM54/74 198, 199 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Input Count Frequency	C_L = 15 pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clear			23	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From Clock			20	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From Clock			17	26	ns
t_W	Width of Clock or Clear Pulse		20			ns
t_{SETUP}	Mode-Control Setup Time		30			ns
t_{SETUP}	Data Setup Time		20			ns
t_{HOLD}	Hold Time at Any Input		0			ns

Conditions for I_{CC} (All outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
198	Serial Input, S0, S1	Clock	Clear, Inputs A thru H
199	J, $\overline{K}$, Inputs A thru H	Clock	Clock Inhibit, Clear, Shift/Load

Truth Tables

198

INPUTS							OUTPUTS				
CLEAR	MODE		CLOCK	SERIAL		PARALLEL	Q_A	Q_B	...	Q_G	Q_H
	S1	S0		LEFT	RIGHT	A . . . H					
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}
H	H	H	↑	X	X	a . . . h	a	b		g	h
H	L	H	↑	X	H	X	H	Q_{An}		Q_{Fn}	Q_{Gn}
H	L	H	↑	X	L	X	L	Q_{An}		Q_{Fn}	Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	H
H	H	L	↑	L	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	L
H	L	L	X	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't care (any input, including transitions)

↑ = Transition from low to high level

a . . . h = The level of steady state input at inputs A thru H, respectively.

Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = The level of Q_A, Q_B, Q_G, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, etc. = The level of Q_A, Q_B, etc., respectively, before the most-recent ↑ transition of the clock.

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INPUTS							OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL		PARALLEL	Q_A	Q_B	Q_C	...	Q_H
				J	$\overline{K}$	A . . . H					
L	X	X	X	X	X	X	L	L	L		L
H	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}		Q_{H0}
H	L	L	↑	X	X	a . . . h	a	b	c		h
H	H	L	↑	L	H	X	Q_{A0}	Q_{A0}	Q_{B0}		Q_{Gn}
H	H	L	↑	L	L	X	L	Q_{An}	Q_{Bn}		Q_{Gn}
H	H	L	↑	H	H	X	H	Q_{An}	Q_{Bn}		Q_{Gn}
H	H	L	↑	H	L	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}		Q_{Gn}
H	X	H	↑	X	X	X	Q_{A0}	Q_{B0}	Q_{B0}		Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't care (any input, including transitions)

↑ = Transition from low to high level

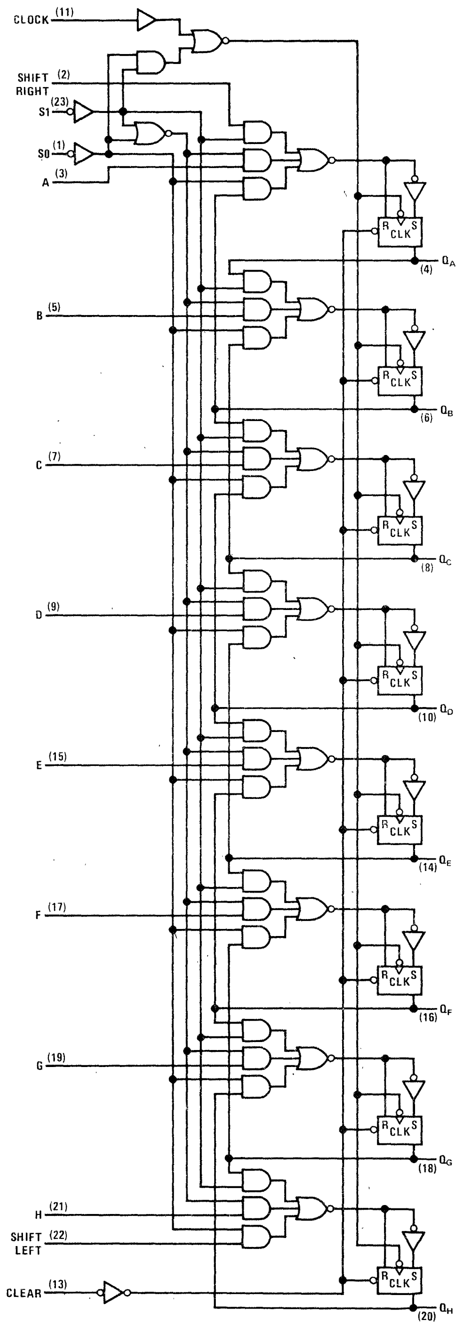
a . . . h = The level of steady state input at inputs A thru H, respectively.

Q_{A0}, Q_{B0}, Q_{C0} . . . Q_{H0} = The level of Q_A, Q_B, or Q_C thru Q_H, respectively, before the indicated steady-state input conditions were established.

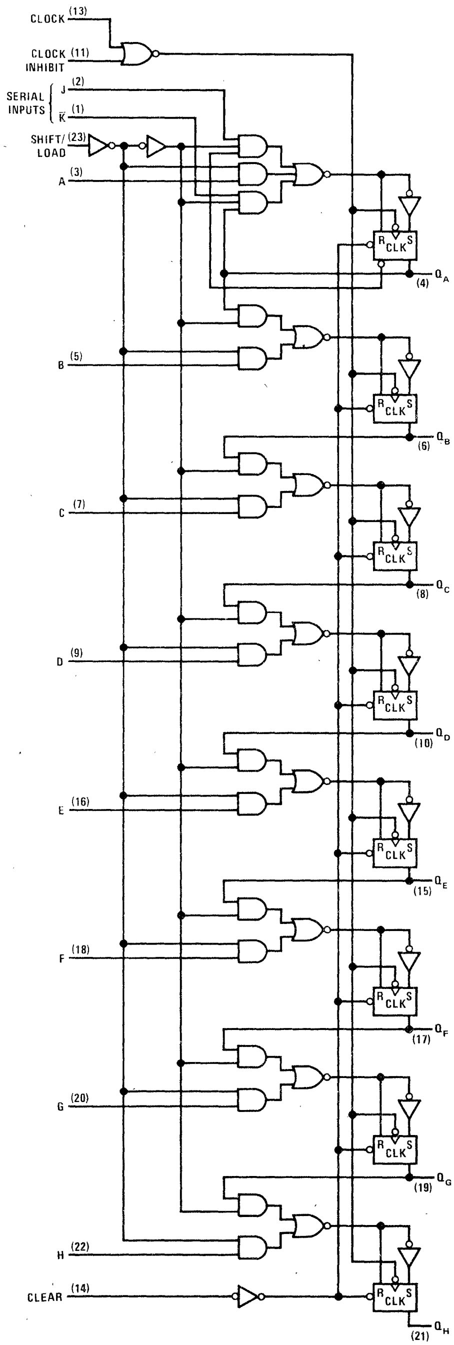
Q_{An}, Q_{Bn} . . . Q_{Gn} = The level of Q_A or Q_B thru Q_G, respectively, before the most-recent ↑ transition of the clock.

Logic Diagrams

198

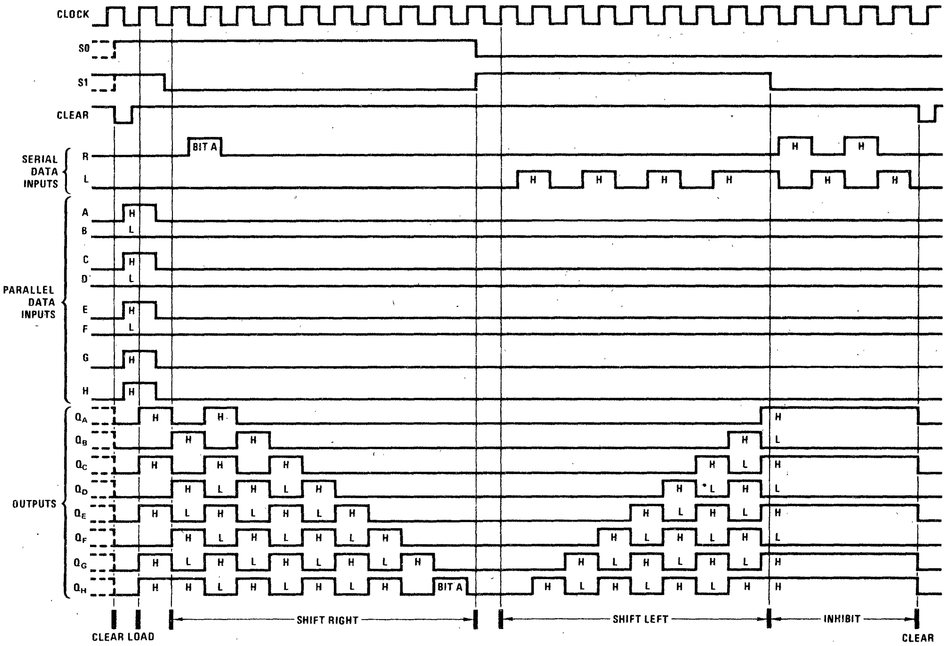


199

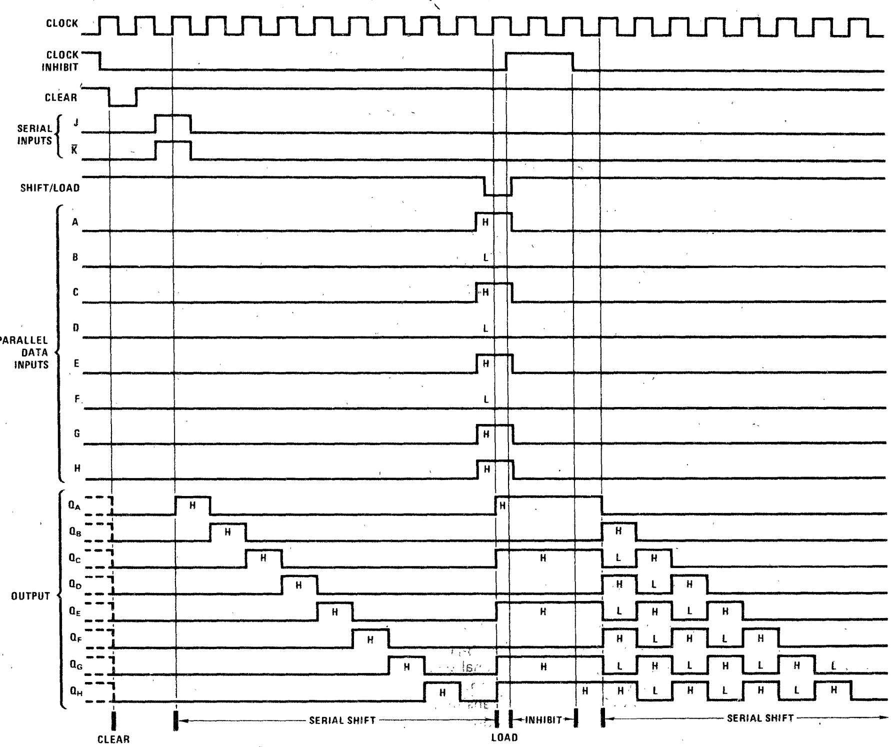


Timing Diagrams

198
TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES



199
TYPICAL CLEAR, SHIFT, LOAD, AND INHIBIT SEQUENCES



Parameter Measurement Information

198
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S_1	S_0	OUTPUT TESTED (SEE NOTE E)
A	4.5V	4.5V	Q_A at t_{n+1}
B	4.5V	4.5V	Q_B at t_{n+1}
C	4.5V	4.5V	Q_C at t_{n+1}
D	4.5V	4.5V	Q_D at t_{n+1}
E	4.5V	4.5V	Q_E at t_{n+1}
F	4.5V	4.5V	Q_F at t_{n+1}
G	4.5V	4.5V	Q_G at t_{n+1}
H	4.5V	4.5V	Q_H at t_{n+1}
L Serial Input	4.5V	0V	Q_A at t_{n+8}
R Serial Input	0V	4.5V	Q_H at t_{n+8}

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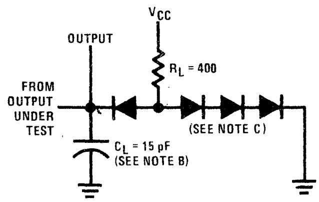
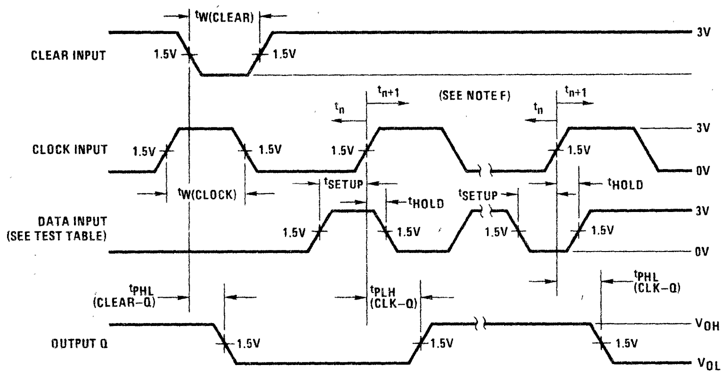
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
A	0V	Q_A at t_{n+1}
B	0V	Q_B at t_{n+1}
C	0V	Q_C at t_{n+1}
D	0V	Q_D at t_{n+1}
E	0V	Q_E at t_{n+1}
F	0V	Q_F at t_{n+1}
G	0V	Q_G at t_{n+1}
H	0V	Q_H at t_{n+1}
J and $\overline{K}$	4.5V	Q_H at t_{n+8}

LOAD FOR OUTPUT UNDER TEST



SWITCHING TIME WAVEFORMS



Notes

(A) The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns. When testing f_{MAX}, vary the clock PRR.

(B) C_L includes probe and jig capacitance.

(C) All diodes are 1N3064.

(D) A clear pulse is applied prior to each test.

(E) Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

(F) t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after clocking transitions

TRI-STATE 256-Bit Read/Write Memories

General Description

The DM54S200/DM74S200 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 mA, only one-eighth that of a normal Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristics of the TTL totem-pole output.

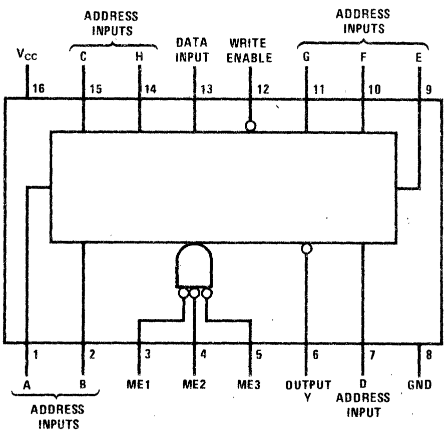
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and the write-enable input are low. While the write-enable input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be in the high-impedance state.

Features

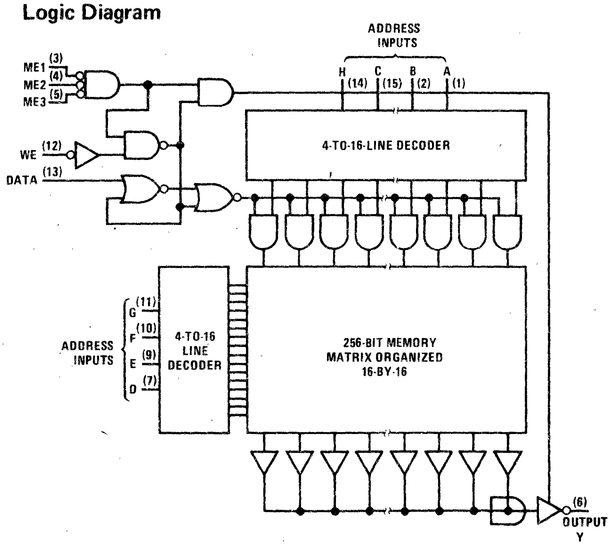
- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 20 ns typ
  - Access from address inputs 31 ns typ
  - Power dissipation 1.7 mW/bit typ
- TRI-STATE output for driving bus-organized systems and/or highly capacitive loads
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

Connection Diagram



54S200(J), (W); 74S200(J), (N), (W)

Logic Diagram



Truth Table

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = High Level, L = Low Level, X = irrelevant

† = For memory enable; L = All ME inputs low

H = One or more ME inputs high

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54S/74S S200 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OH}	High Level Output Current		DM54			−2.0	mA
			DM74			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4			V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA	DM54			0.5	V
			DM74			0.45	V
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2.0V	V_O = 0.45V			−50	μA
			V_O = 2.4V			50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−100	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			87	130	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

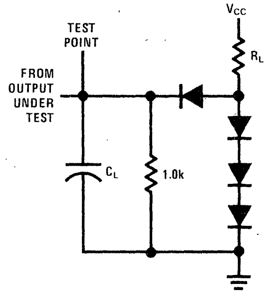
(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) I_{CC} is measured with the write enable and memory enable grounded, all other inputs at 4.5V and the output open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

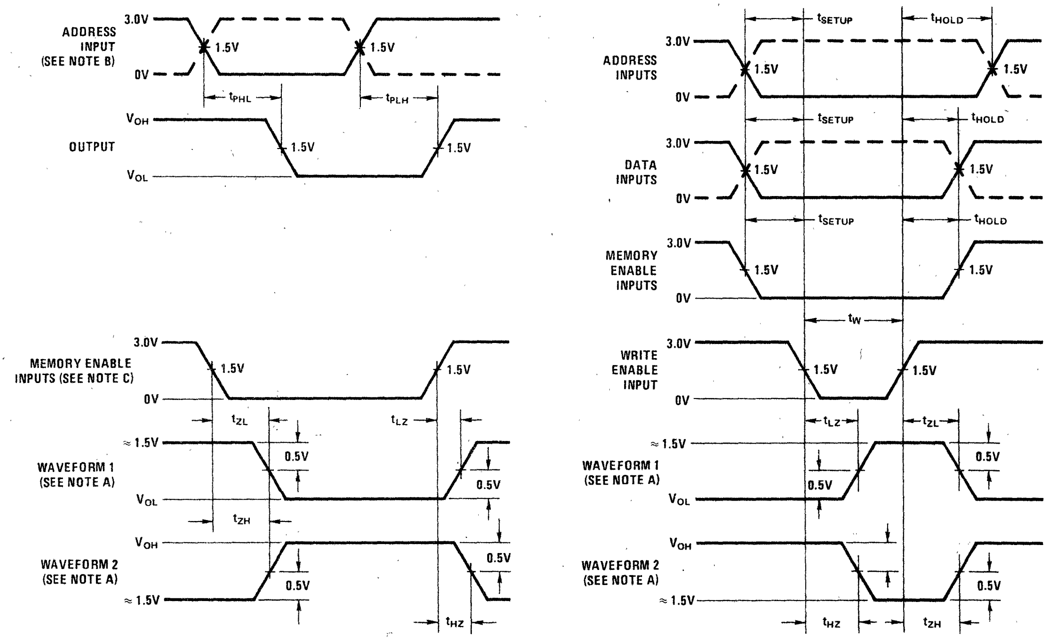
	PARAMETER		CONDITIONS	54S200 MIN	54S200 TYP	54S200 MAX	74S200 MIN	74S200 TYP	74S200 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Access Time From Address	C_L = 15 pF, R_L = 280Ω		33	70		33	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Access Time From Address	C_L = 15 pF, R_L = 280Ω		29	70		29	50	ns
t_{ZH}	Output Enable Time To High Level	Access Time From Memory Enable	C_L = 15 pF, R_L = 280Ω		21	45		21	35	ns
t_{ZL}	Output Enable Time To Low Level	Access Time From Memory Enable	C_L = 15 pF, R_L = 280Ω		10	30		10	20	ns
t_{ZH}	Output Enable Time To High Level	Sense Recovery Time From Write Enable	C_L = 15 pF, R_L = 280Ω		24	50		24	40	ns
t_{ZL}	Output Enable Time To Low Level	Sense Recovery Time From Write Enable	C_L = 15 pF, R_L = 280Ω		12	50		12	40	ns
t_{HZ}	Output Disable Time From High Level	Disable Time From Memory Enable	C_L = 5.0 pF, R_L = 280Ω		7.0	30		7.0	20	ns
t_{LZ}	Output Disable Time From Low Level	Disable Time From Memory Enable	C_L = 5.0 pF, R_L = 280Ω		20	45		20	35	ns
t_{HZ}	Output Disable Time From High Level	Disable Time From Write Enable	C_L = 5.0 pF, R_L = 280Ω		13	40		13	30	ns
t_{LZ}	Output Disable Time From Low Level	Disable Time From Write Enable	C_L = 5.0 pF, R_L = 280Ω		16	40		16	30	ns
t_W	Width of Write Enable Pulse			50			40			ns
t_{SETUP}	Setup Time	Address to Write Enable		0			0			ns
		Data to Write Enable		0			0			ns
		Memory Enable to Write Enable		0			0			ns
t_{HOLD}	Hold Time	Address From Write Enable		10			10			ns
		Data From Write Enable		10			10			ns
		Memory Enable to Write Enable		0			0			ns

AC Test Circuit



C_L includes probe and jig capacitance.
All diodes are 1N3064.

Switching Time Waveforms



Notes:

(A) Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

(B) When measuring delay times from address inputs, the memory enable inputs are low and the write enable input is high.

(C) When measuring delay times from memory enable inputs, the address inputs are steady-state and the write enable input is high.

(D) Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR ≤ 1.0 MHz, and $Z_{OUT} \approx 50\Omega$.

256-Bit Read/Write Memories with Open Collector Outputs

General Description

The DM54S206/DM74S206 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normal Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

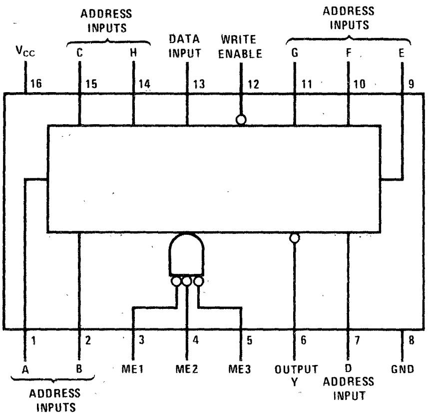
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and the write-enable input are low. While the write-enable input is low, the output is off.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be off.

Features

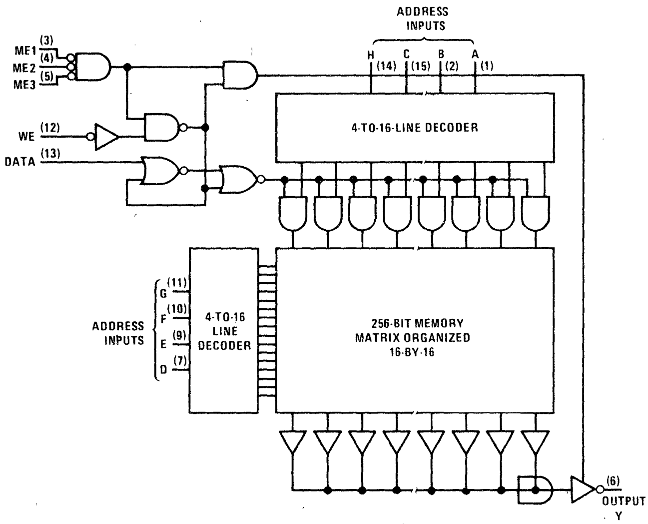
- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 17 ns typ
  - Access from address inputs 35 ns typ
  - Power dissipation 1.4 mW/bit typ
- Open-collector output for word expansion
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

Connection Diagram



54S206(J), (W); 74S206(J), (N), (W)

Logic Diagram



Truth Table

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	Hi-Z
Read	L	H	Stored Data
Inhibit	H	X	Hi-Z

H = high level, L = low level, X = irrelevant

†For memory enable: L = all ME inputs low;
H = one or more ME inputs high.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54S/74S S206 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA	DM54			0.5	V
			DM74			0.45	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{CC}	Supply Current	V_{CC} = Max(2)			70	130	mA

Notes

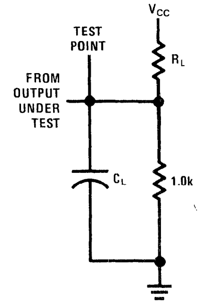
(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER		CONDITIONS	DM54S/74S 54S206 MIN	TYP	MAX	74S206 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Access Times from Address	C_L = 15 pF, R_L = 300Ω		38	80		38	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Access Times from Address			32	80		32	60	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Disable Time from Memory Enable			21	45		21	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable Time from Memory Enable			13	35		13	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Disable Time from Write Enable			20	50		20	40	ns
t_{SR}	Sense Recovery Time				14	50		14	40	ns
t_W	Width of Write Enable Pulse			50			40			ns
t_{SETUP}	Setup Time	Address to Write Enable		0			0			ns
		Data to Write Enable		0			0			
		Memory Enable to Write Enable		0			0			
t_{HOLD}	Hold Time	Address from Write Enable		10			10			ns
		Data from Write Enable		10			10			
		Memory Enable to Write Enable		0			0			

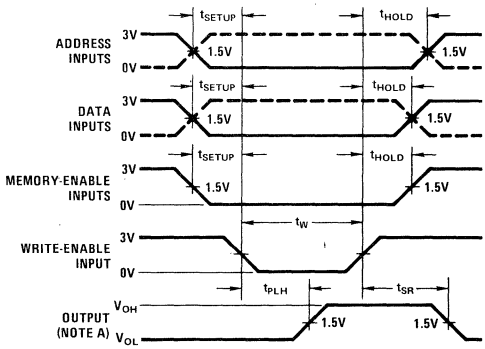
AC Test Circuit



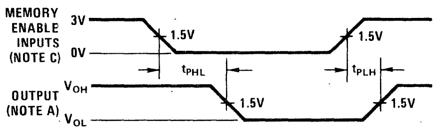
C_L includes probe and jig capacitance.

Switching Time Waveforms

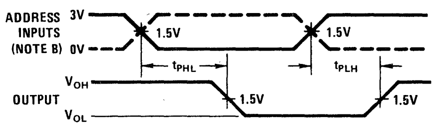
WRITE CYCLE



ACCESS (ENABLE) TIME AND DISABLE TIME FROM MEMORY ENABLE



ACCESS TIME FROM ADDRESS INPUTS



Notes:

(A) Waveform shown is for the output with internal conditions such that the output is low except when disabled.

(B) When measuring delay times from address inputs, the memory-enable inputs are low and the write-enable input is high.

(C) When measuring delay times from memory-enable inputs, the address inputs are steady-state and the write-enable input is high.

(D) Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{OUT} \approx 50\Omega$.

TRI-STATE Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

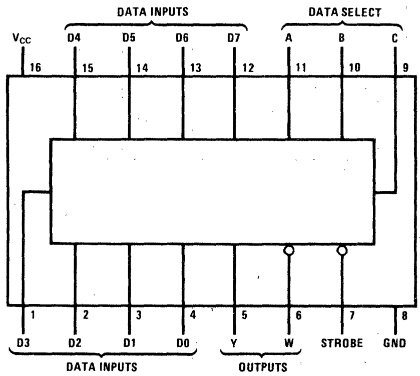
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE versions of 151, LS151, S151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data

TYPE	MAX NO. OF COMMON OUTPUTS	TYPICAL PROP DELAY TIME (D TO Y)	TYPICAL POWER DISSIPATION
54251	49	17 ns	155 mW
74251	129	17 ns	155 mW
54LS251	49	17 ns	35 mW
74LS251	129	17 ns	35 mW
74S251	129	8 ns	275 mW

Connection Diagram



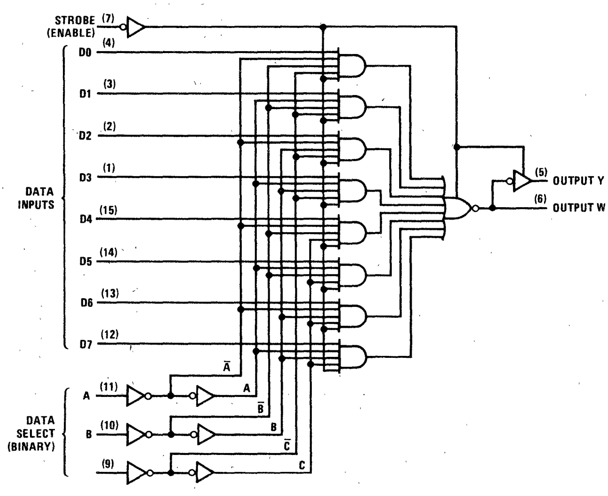
54251(J), (W); 74251(J), (N), (W); 54LS251/74LS251(J), (N), (W); 74S251(N)

Truth Table

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1. . .D7 = The level of the respective D input.

Logic Diagram



LS251, S251 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54/74 251 MIN	DM54/74 251 TYP(1)	DM54/74 251 MAX	DM54LS/74LS LS251 MIN	DM54LS/74LS LS251 TYP(1)	DM54LS/74LS LS251 MAX	DM74S S251 MIN	DM74S S251 TYP(1)	DM74S S251 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7			N/A	V
			DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5							V
		V_{CC} = Min, $I_I = -18$ mA							−1.5			−1.2	
I_{OH}	High Level Output Current		DM54			−2			−1			N/A	mA
			DM74			−5.2			−2.6			−6.5	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	DM54	2.4			2.4				N/A		V
			DM74	2.4			2.4			2.4	3.2		
I_{OL}	Low Level Output Current		DM54			16			4			N/A	mA
			DM74			16			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM54			0.4		0.25	0.4			N/A	V
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM74			0.4		0.35	0.5			0.5	
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = 4 mA	DM74						0.4				
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = Max	V_O = 0.4V			−40			−20				μA
			V_O = 0.5V									−50	
			V_O = 2.4V			40			20			50	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V			1						1	mA
			V_I = 7V						0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V			40							μA
			V_I = 2.7V						20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V			−1.6			−0.4				mA
			V_I = 0.5V									−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−18		−55	−30		−130	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max(3)	Strobe Grounded		31	51		6.1	10		55	85	mA
			Strobe at 4.5V		31	51		7.1	12		55	85	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS or DM74S duration of short circuit should not exceed one second.

(3) All outputs open, all inputs at 4.5V.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

				DM54/74				DM54LS/74LS				DM74S				
PARAMETER		FROM (INPUT)	TO (OUTPUT)	251				LS251				S251				UNITS
				CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A, B, or C (4 levels)	Y	$C_L = 50$ pF, $R_L = 400\Omega$		22	36	$C_L = 15$ pF, $R_L = 2$ kΩ		29	45	$C_L = 15$ pF, $R_L = 280\Omega$		12	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					23	36			28	45			13	19.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A, B, or C (3 levels)	W			18	29			20	33			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					16	27			21	33			9	13.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any D	Y			17	28			17	28			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					18	28			18	28			8	12	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any D	W			11	15			10	15			4.5	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					10	15			9	15			4.5	7	ns
t_{ZH}	Output Enable Time to High Level	Strobe	Y			15	27			30	45	$C_L = 50$ pF, $R_L = 280\Omega$		13	19.5	ns
t_{ZL}	Output Enable Time to Low Level					18	36			26	40			14	21	ns
t_{ZH}	Output Enable Time to High Level	Strobe	W			15	27			17	27			13	19.5	ns
t_{ZL}	Output Enable Time to Low Level					19	38			24	40			14	21	ns
t_{HZ}	Output Disable Time from High Level	Strobe	Y	$C_L = 5$ pF, $R_L = 400\Omega$		4	8	$C_L = 5$ pF, $R_L = 2$ kΩ		30	45	$C_L = 5$ pF, $R_L = 280\Omega$		5.5	8.5	ns
t_{LZ}	Output Disable Time from Low Level					14	23			15	25			9	14	ns
t_{HZ}	Output Disable Time from High Level	Strobe	W			4	8			37	55			5.5	8.5	ns
t_{LZ}	Output Disable Time from Low Level					15	23			15	25			9	14	ns

TRI-STATE Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

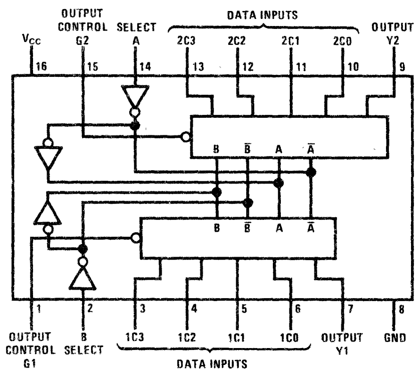
The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

Features

- TRI-STATE version of LS153, S153 with same pin-out
- Schottky-diode-clamped transistors
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fan-out totem-pole outputs

TYPE	TYPICAL PROPAGATION DELAY		TYPICAL POWER DISSIPATION
LS253	Data to Output	12 ns	35 mW
	Select to Output	21 ns	
S253	Data to Output	6 ns	275 mW
	Select to Output	12 ns	

Connection Diagram



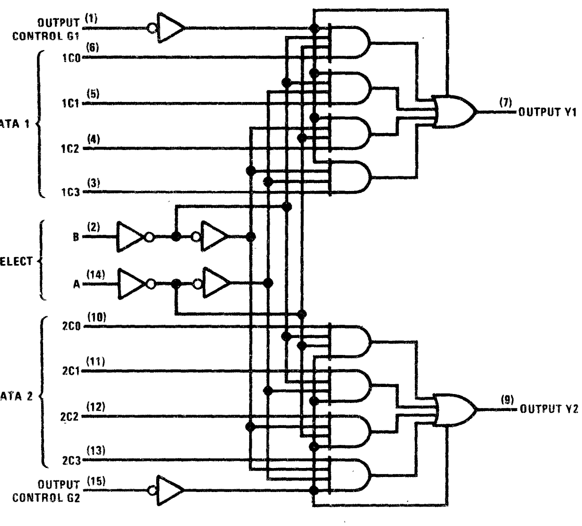
54LS253/74LS253(J), (N), (W); 74S253(N)

Truth Table

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care,
Z = High Impedance

Logic Diagram



S253 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			DM54LS/74LS LS253 MIN	TYP(1)	MAX	DM74 S253 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.7			N/A	V
				DM74			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5			−1.2	V
I_{OH}	High Level Output Current			DM54			−1			N/A	mA
				DM74			−2.6			−6.5	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4			N/A		V
				DM74	2.4	3.1		2.7	3.2		
I_{OL}	Low Level Output Current			DM54			4			N/A	mA
				DM74			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = Max	DM54			0.4			N/A	V
				DM74			0.5			0.5	
			I_{OL} = 4 mA	DM74			0.4				
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = Max	V_O = 0.4V				−20				μA
			V_O = 0.5V							−50	
			V_O = 2.4V				20			50	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V							1.0	mA
			V_I = 7V				0.1				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−0.36				mA
			V_I = 0.5V							−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)			−30		−130	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max(3)	Condition A			7	12				mA
			Condition B			8.5	14				
			All Outputs Open						55	70	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) I_{CC} is measured with the outputs open under the following conditions:
A. All inputs grounded.
B. Output control at 4.5V, all inputs grounded.

(4) National Semiconductor temporarily reserves the right to ship DM54/DM74LS253 devices which have a minimum I_{OS} = 5.0 mA.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	From (Input)	To (Output)	DM54LS/74LS LS253 Conditions	MIN	TYP	MAX	DM74 S253 Conditions	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Y	C_L = 15 pF, R_L = 2 kΩ		17	25	C_L = 15 pF, R_L = 280Ω		6	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Y			13	20			6	9	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Y			30	45			11.5	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Y			21	32			12	18	ns
t_{ZH}	Output Enable Time to High Level	Output Control	Y			15	23	C_L = 50 pF, R_L = 280Ω		13	19.5	ns
t_{ZL}	Output Enable Time to Low Level	Output Control	Y			15	23			14	21	ns
t_{HZ}	Output Disable Time From High Level	Output Control	Y	C_L = 5 pF, R_L = 2 kΩ		27	41	C_L = 5 pF, R_L = 280Ω		5.5	8.5	ns
t_{LZ}	Output Disable Time From Low Level	Output Control	Y			18	27			9	14	ns

TRI-STATE Quad 2-Data Selectors/Multiplexers

General Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

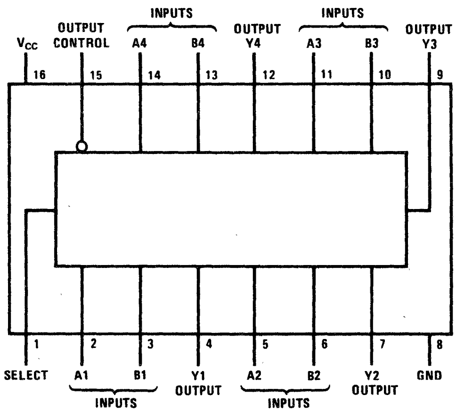
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

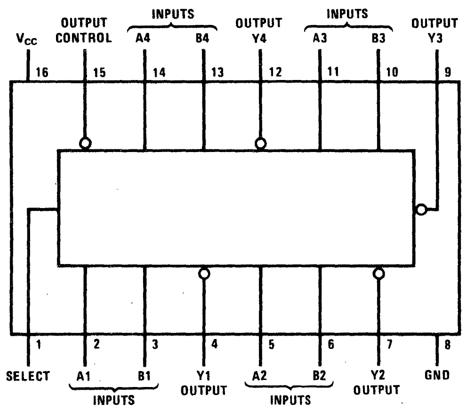
- TRI-STATE versions LS157, S157, LS158, S158, with same pin-outs
- Schottky-clamped for significant improvement in A–C performance
- Provides bus interface from multiple sources in high-performance systems

TYPE	AVERAGE PROPAGATION DELAY FROM DATA INPUT	TYPICAL POWER DISSIPATION
LS257	12 ns	50 mW
LS258	12 ns	35 mW
S257	4.8 ns	320 mW
S258	4 ns	280 mW

Connection and Logic Diagrams

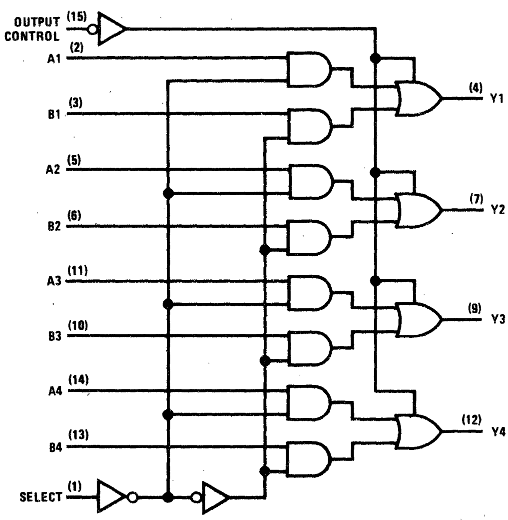


54LS257/74LS257(J), (N), (W); 74S257(N)

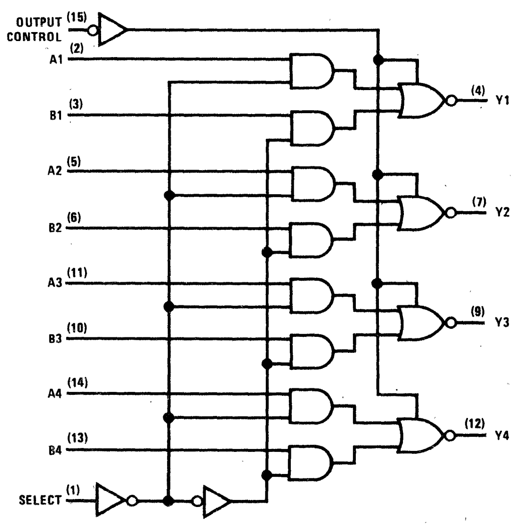


54LS258/74LS258(J), (N), (W); 74S258(N)

LS257, S257



LS258, S258



To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS			DM54LS/74LS LS257, LS258 MIN	TYP(1)	MAX	DM74S S257, S258 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.7			N/A	V
					DM74			0.8			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −18 mA					−1.5			−1.2	V
I_{OH}	High Level Output Current				DM54			−1.0			N/A	mA
					DM74			−2.6			−6.5	
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V		DM54	2.4	3.4		N/A			V
			V_{IL} = Max, I_{OH} = Max		DM74	2.4	3.1		2.4	3.2		
I_{OL}	Low Level Output Current				DM54			4			N/A	mA
					DM74			8			20	
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V	I_{OL} = Max	DM54		0.25	0.4			N/A	V
			V_{IL} = Max		DM74		0.35	0.5			0.5	
				I_{OL} = 4 mA	DM74		0.25	0.4				
$I_{O(OFF)}$	Off State (High Impedance State) Output Current		V_{CC} = Max	V_O = 0.4V				−20				μA
			V_{IH} = 2V	V_O = 0.5V							−50	
			V_{IL} = Max	V_O = 2.4V				20			50	
I_I	Input Current at Maximum Input Voltage	S Input	V_{CC} = Max	V_I = 5.5V							1	mA
				V_I = 7V				0.2				
		Any Other		V_I = 5.5V							1	
				V_I = 7V				0.1				
I_{IH}	High Level Input Current	S Input	V_{CC} = Max, V_I = 2.7V					40			50	μA
		Any Other						20			50	
I_{IL}	Low Level Input Current	S Input	V_{CC} = Max	V_I = 0.4V				−0.8				mA
				V_I = 0.5V							−2	
		Any Other		V_I = 0.4V				−0.4				
				V_I = 0.5V							−2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)			−30		−130	−40		−100	mA
I_{CC}	Supply Current	All Outputs High	V_{CC} = Max(3)	LS257, S257			5.9	10		44	68	mA
		All Outputs Low					9.2	16		60	93	
		All Outputs Off					10	17		64	99	
		All Outputs High		LS258, S258			4.1	7		36	56	
		All Outputs Low					6.2	11		52	81	
		All Outputs Off					7.0	12		56	87	

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	DM54LS/74LS				DM74S							UNITS
				LS257, LS258					S257			S258			
				CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Any	$C_L = 15$ pF, $R_L = 2$ kΩ		12	18	$C_L = 15$ pF, $R_L = 280Ω$		5	7.5		4	6	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Any			12	18			4.5	6.5		4	6	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Any			14	21			8.5	15		8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Any			14	21			8.5	15		7.5	12	ns
t_{ZH}	Output Enable Time to High Level	Output Control	Any			20	30			13	19.5		13	19.5	ns
t_{ZL}	Output Enable Time to Low Level	Output Control	Any			20	30			14	21		14	21	ns
t_{HZ}	Output Disable Time From High Level	Output Control	Any	$C_L = 5$ pF, $R_L = 2$ kΩ		20	30	$C_L = 5$ pF, $R_L = 280Ω$		5.5	8.5		5.5	8.5	ns
t_{LZ}	Output Disable Time From Low Level	Output Control	Any			17	25			9	14		9	14	ns

Notes

(1) All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

(3) I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

Truth Table

INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	LS257 S257	LS258 S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care,
Z = High Impedance (off)

Quad $\bar{S}$-$\bar{R}$ Latches

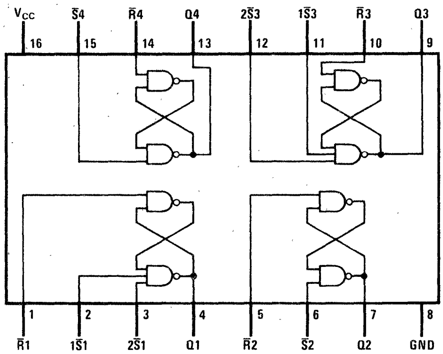
General Description

These latches are ideally suited for use as temporary storage of binary information between processing units and I/O units. When either one of the data inputs is at a low logic level, the output will follow the level of the $\bar{R}$ input. When both data inputs are high, the output will remain latched in its previous state. When both inputs are low, the output will go high. However, this high level may not persist when either one of the data inputs returns to the high state.

Features

- For more advanced design $\bar{S}$-$\bar{R}$ latches, see DM7544/8544
- Typical power dissipation 19 mW
- Typical propagation delay 12 ns

Connection Diagram



54LS279/74LS279(J), (N), (W)

Truth Table

INPUTS		OUTPUT
S†	$\bar{R}$	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = High Level

L = Low Level

Q_0 = The level of Q before the indicated input conditions were established.

* This output level is pseudo stable: that is, it may not persist when the $\bar{S}$ and $\bar{R}$ inputs return to their inactive (high) level.

† For latches with double $\bar{S}$ inputs:
H = both $\bar{S}$ inputs high
L = one or both $\bar{S}$ inputs low

To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS			DM54LS/74LS LS279 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage			DM54			0.7	V
				DM74			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
I_{OH}	High Level Output Current						−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = −400μA		DM54	2.5	3.5		V
				DM74	2.7	3.5		
I_{OL}	Low Level Output Current			DM54			4	mA
				DM74			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = 4 mA			0.25	0.4	V
			I_{OL} = 8 mA	DM74		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)			−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max (3)				3.8	7	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) I_{CC} is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5V, and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output From $\overline{S}$ Input	C_L = 15 pF, R_L = 2 kΩ		12	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From $\overline{S}$ Input			9	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output From $\overline{R}$ Input			15	27	ns

9-Bit Parity Generators/Checkers

General Description

These universal, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry, and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is easily expanded by cascading.

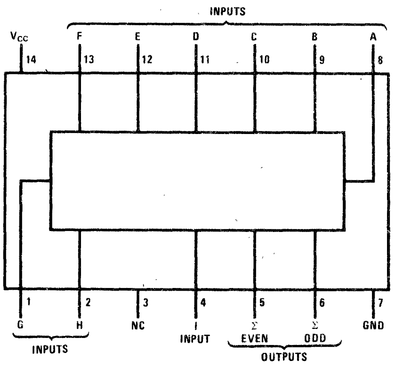
The S280 can be used to upgrade the performance of most systems utilizing the DM74180 parity generator/checker. Although the S280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4, and no internal connection at pin 3. This permits the S280 to be substituted for the 180 in existing designs to produce an identical function, even if S280's are mixed with existing 180's.

Input buffers are provided so that each input represents only one normal 74S load, and full fan-out to 10 normal Series 74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normal Series 74S loads is provided at high logic levels, to facilitate connection of unused inputs to used inputs.

Features

- Generates either odd or even parity for nine data lines
- Cascadable for n-bits
- Can be used to upgrade existing systems using MSI parity circuits
- Typical data-to-output delay—14 ns

Connection Diagram

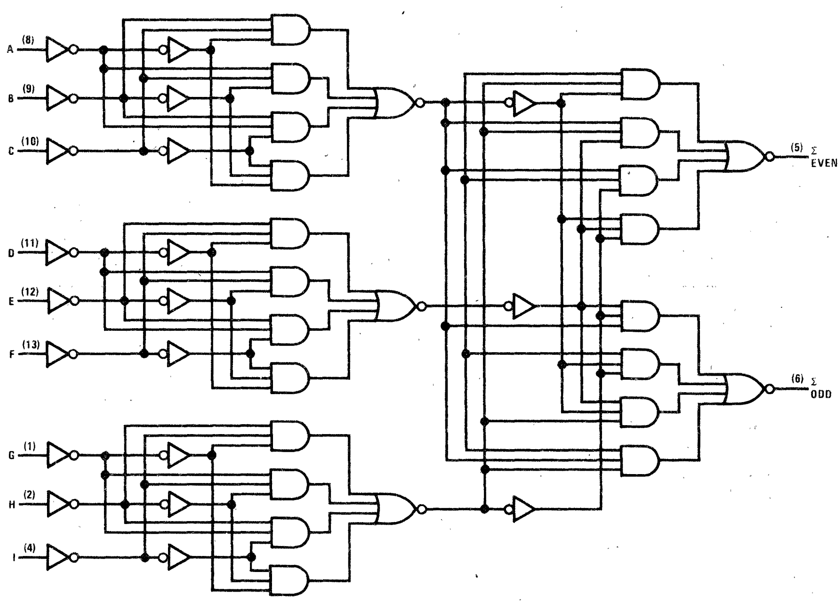


74S280(N)

Truth Table

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM74S S280 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{OH}	High Level Output Current				−1	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1 mA	2.7	3.4		V
I_{OL}	Low Level Output Current				20	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20 mA			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max(3)		67	105	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

(3) I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM74S S280 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Σ Even	C_L = 15 pF, R_L = 180Ω		14	21	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Σ Even			11.5	18	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Σ Odd			14	21	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Σ Odd			11.5	18	ns

Typical Applications

Three S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 25 ns. (See *Figure 1.*)

As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (S86) or 3-input (S135) exclusive-OR gate for 18 or 27-line parity applications.

Longer word lengths can be implemented by cascading S280's. As shown in *Figure 2,* parity can be generated for word lengths up to 81 bits in typically 25 ns.

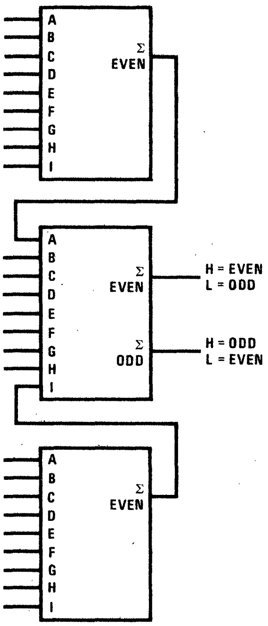


FIGURE 1: 25-LINE PARITY/GENERATOR CHECKER

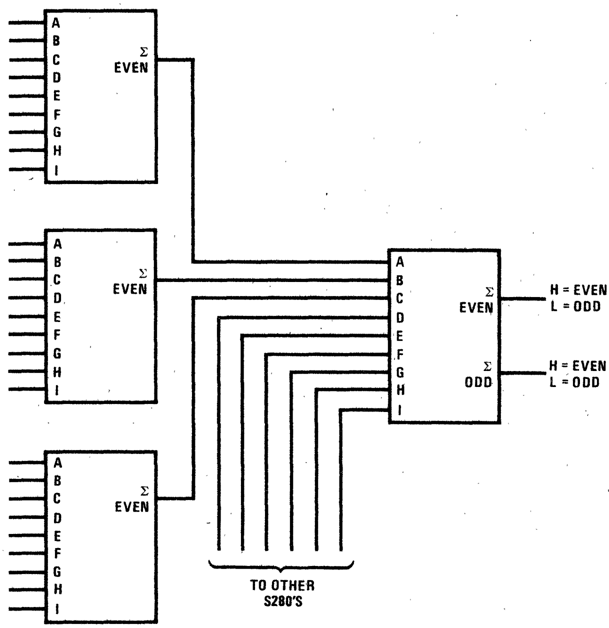


FIGURE 2: 81-LINE PARITY/GENERATOR CHECKER

4-Bit Parallel Binary Accumulators

General Description

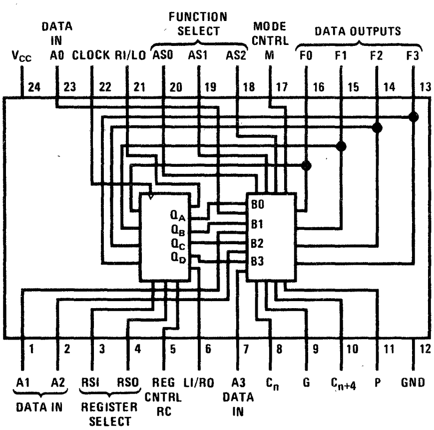
These Schottky-clamped four-bit accumulators integrate high-performance versions of an arithmetic logic unit/ function generator, and a shift/storage matrix in a single circuit. The arithmetic logic unit (ALU) portion provides the capability of 16 arithmetic/logic type operations, as detailed in Table I. The accumulator includes an exchange of subtract operands by which either A—B or B—A can be accomplished directly. The ALU is controlled by three function-select inputs (AS0, AS1, AS2) and a mode-control input (M). When the mode-control input is high, the ALU may perform any of seven logic functions on two binary variables, as detailed in Table II. Full carry look-ahead is provided for fast, simultaneous carry generation. The carry input (C_n) and propagate and generate outputs (P, G) are implemented for direct use with the DM74S182 look-ahead/carry generators. This permits systems to be implemented with the added advantage of full look-ahead across any word length to minimize the accumulator delay times. Once data is loaded into the accumulator, the typical add time with full look-ahead is 29 nanoseconds for 16-bit words.

The shift/storage matrix has capabilities similar to the DM74S194 universal bidirectional shift register, with the added advantage of multiplexed input/output (I/O) cascading lines which comprehend arithmetic shift functions having a sign bit, such as 2's complements. The matrix can be used to perform either logic or arithmetic shifts in either direction (left or right), parallel load, or hold. Control of the register is accomplished with three inputs: register control (RC) and register selection (RS0, RS1). The cascading input/output lines incorporate TRI-STATE outputs multiplexed with an input. The least-significant cascading bit is combined with the A0/F0 circuitry to provide the shift-right input and the shift-left output (RI/LO), and the most significant bit is coupled with the A3/F3 circuitry to provide the shift-left input and the shift-right output (LI/RO).

Features

- Logic mode operation provides seven Boolean functions of the two variables
- Full shifting capabilities:
  - Logic shift (left or right)
  - Arithmetic shift (left or right) for sign bit protection
  - Hold
  - Parallel load
- Expandable to handle n-bit words with full carry look-ahead
- 15 arithmetic/logic operations:
  - Add
  - Subtract (B—A or A—B)
  - Complement
  - Increment
  - Transfer
  - Plus 10 other functions
- Full 4-bit binary accumulator in a single package

Connection Diagram



74S281(N)

Truth Tables Notes Shown on Following Page

TABLE I—ARITHMETIC FUNCTIONS
Mode Control (M) = Low

ALU SELECTION			ACTIVE HIGH DATA	
AS2	AS1	AS0	C_n = H (with carry)	C_n = L (no carry)
L	L	L	F0 = L, F1 = F2 = F3 = H	F_n = H
L	L	H	F = B MINUS A	F = B MINUS A MINUS 1
L	H	L	F = A MINUS B	F = A MINUS B MINUS 1
L	H	H	F = A PLUS B PLUS 1	F = A PLUS B
H	L	L	F = B PLUS 1	$F_n = B_n$
H	L	H	F = $\overline{B}$ PLUS 1	$\overline{F_n} = \overline{B_n}$
H	H	L	F = A PLUS 1	$F_n = A_n$
H	H	H	F = $\overline{A}$ PLUS 1	$F_n = \overline{A_n}$

TABLE II—LOGIC FUNCTIONS
Mode Control (M) = High
Carry Input (C_n) = X (Don't Care)

ALU SELECTION			ACTIVE-HIGH DATA FUNCTION
AS2	AS1	AS0	
L	L	L	$F_n = L$
L	X	H	$F_n = A_n \oplus B_n$
L	H	L	$F_n = \overline{A_n \oplus B_n}$
H	L	L	$F_n = A_n B_n$
H	L	H	$F_n = \overline{A_n + B_n}$
H	H	L	$F_n = \overline{A_n B_n}$
H	H	H	$F_n = A_n + B_n$

Truth Tables (Continued)

TABLE III—SHIFT MODE FUNCTIONS
C_n = M = S0 = S1 = Low, and S2 = High

REGISTER SELECTION		REGISTER CONTROL INPUT	SHIFT-MATRIX INPUTS				CLOCK INPUT	INPUT/ OUTPUT RI/LO	SHIFT-MATRIX OUTPUTS (INTERNAL)				INPUT/ OUTPUT LI/RO
RS1	RS0		F0	F1	F2	F3			Q_A	Q_B	Q_C	Q_D	
L	L	X	f0	f1	f2	f3	↑	Z	f0	f1	f2	f3	Z
L	H	L	Q_{Bn}	Q_{Cn}	Q_{Dn}	li	↑	Q_{Bn}	Q_{Bn}	Q_{Cn}	Q_{Dn}	li	li
L	H	H	Q_{A0}	Q_{Cn}	Q_{Dn}	li	↑	Q_{Bn}	Q_{Bn}	Q_{Cn}	li	Q_{D0}	li
H	L	L	ri	Q_{An}	Q_{Bn}	Q_{Cn}	↑	ri	ri	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	H	ri	Q_{An}	Q_{Bn}	Q_{D0}	↑	ri	ri	Q_{An}	Q_{Bn}	Q_{D0}	Q_{Cn}
H	H	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	↑	Z	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Z
X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	X

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
Z = High Impedance (output off)
↑ = Transition from low to high level
f0, f1, f2, f3, ri, li = The level of steady-state conditions at F0, F1, F2, F3, RI/LO or LI/RO respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent transition of the clock.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS	DM74S S281 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	Any Input Except LI/RO and RI/LO	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{OH}	High Level Output Current	Any Output Except LI/RO and RI/LO				−1	mA
		LI/RO and RI/LO				−2	mA
V_{OH}	High Level Output Voltage	Any Output Except LI/RO and RI/LO	V_{CC} = Min, V_{IH} = 2V	2.7	3.4		V
		LI/RO, RI/LO	V_{IL} = 0.8V, I_{OH} = Max	2.4	3.4		V
I_{OL}	Low Level Output Current	Any Output Except LI/RO and RI/LO				20	mA
		LI/RO and RI/LO				10	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_I	Input Current at Maximum Input Voltage(3)		V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	RS0, RS1	V_{CC} = Max, V_I = 2.7V			50	μA
		M, Clock				150	
		LI/RO, RI/LO(3)				200	
		AS2				300	
		Others				250	
I_{IL}	Low Level Input Current	RS0, RS1, LI/RO(3)	V_{CC} = Max, V_I = 0.5V			−2	mA
		RI/LO				−3	
		M, Clock				−4	
		AS0, AS1				−6	
		Others				−8	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	−40		−110	mA
I_{CC}	Supply Current		V_{CC} = Max		144	230	mA

Notes
(1) All typical values are at V_{CC} = 5V, T_A = 25°C.
(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.
(3) When testing input current at the RI/LO or LI/RO terminals, the output under test must be in the high-impedance (off) state.

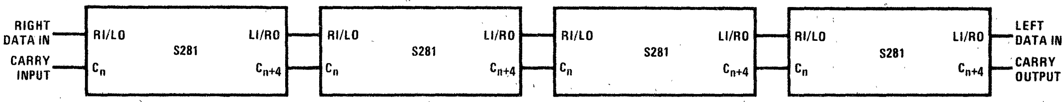
Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM74S S281 MIN	DM74S S281 TYP	DM74S S281 MAX	UNITS
f_{MAX}	Clock Frequency (For Shifting)				50			MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+4}	C_L = 15 pF; I/O Outputs: R_L = 560Ω; Other Outputs: R_L = 280Ω		10	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					10	20	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A	C_{n+4}			18	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					18	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	Any F			10	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					10	20	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A	G			14	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	24	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A	P			12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12	20	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i	F_i			20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					20	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_0	RI/LO			30	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30	45	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_3	LI/RO			30	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30	45	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	F_0	RI/LO			7	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7	11	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	F_3	LI/RO			7	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7	11	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any AS	Any F or C_{n+4}			28	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					28	45	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any AS	P or G			20	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Any F			30	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30	45	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	RI/LO or LI/RO			35	55	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					35	55	ns
$t_{W(CLOCK)}$	Width of Clock Pulse				8			ns
t_{SETUP}	Data Setup Time With Respect to Clock				0↑ (5)			ns
t_{HOLD}	Data Hold Time With Respect to Clock				18↑ (5)			ns

Notes

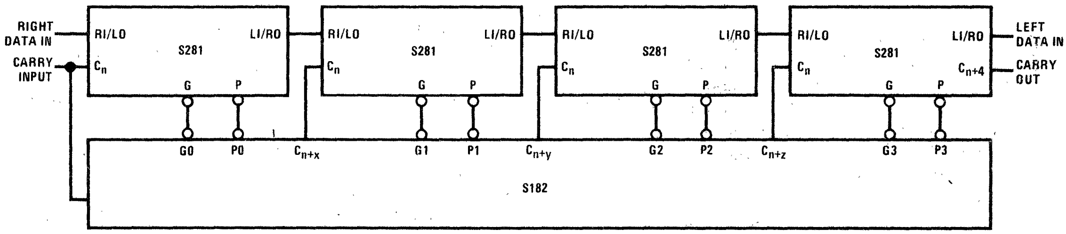
(5) ↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

Typical Applications



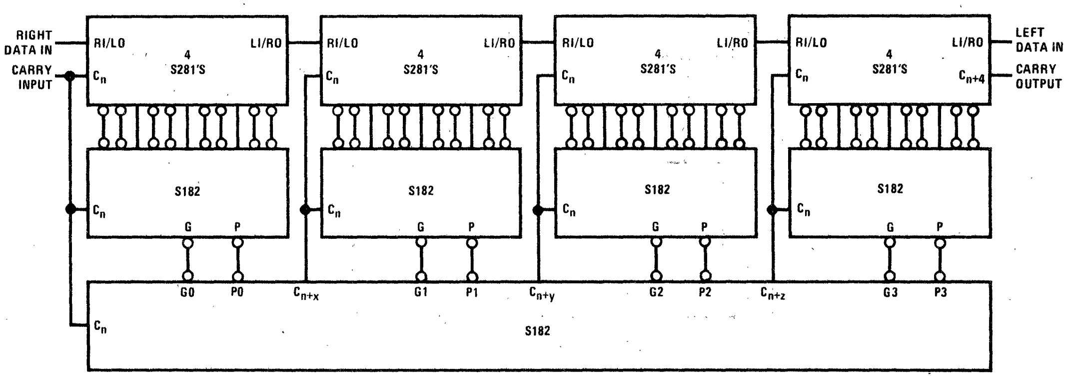
Enter and store time: 38 ns typ
Each successive addition to stored data: 44 ns typ

FIGURE A: 16-BIT BINARY ACCUMULATOR USING FOUR DM74S281 CIRCUITS IN RIPPLE-CARRY MODE



Enter and store time: 37 ns typ
Each successive addition to stored data: 29 ns typ

FIGURE B: 16-BIT BINARY ACCUMULATOR USING FOUR DM74S281 CIRCUITS AND ONE DM74S182 FOR FULL CARRY LOOK-AHEAD



Enter and store time: 42 ns typ
Each successive addition to stored data: 34 ns typ

FIGURE C: 64-BIT BINARY ACCUMULATOR USING 16 DM74S281 CIRCUITS AND FIVE DM74S182 CIRCUITS FOR FULL CARRY LOOK-AHEAD

1024-Bit Programmable Read Only Memories

General Description

These circuits are field-programmable, 1024-bit, read-only memories organized as 256 words of four bits each. This high-speed, Schottky-clamped, TTL memory array is addressed in 8-bit binary with full on-chip decoding. Two overriding chip-select inputs are provided which, when either one or both are high, cause all four outputs to be off (high Z state for S287). This memory features PNP input transistors, which reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a standard Series 74S load. The organization is expandable with no additional output buffering.

The address of a 4-bit word is accomplished through the buffered binary select inputs, with a low level at both chip-select inputs. Where multiple devices are used in a memory system, the chip-select inputs allow easy decoding of additional address bits.

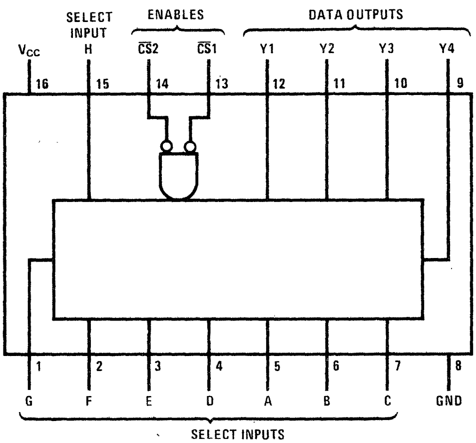
Data can be electronically programmed at any of the 1024-bit locations. Prior to programming, the memory contains a low logic level output condition at all bit locations. The programming procedure open-circuits metal links, which results in a high logic level output at the selected locations. The procedure is irreversible; once altered, the output for that bit is permanently programmed to provide a high logic level. Outputs never having been altered may later be programmed to supply a high level output. Operation of the device within the recommended operating conditions will not alter the memory content.

These programmable memories can be used to replace the DM74187, as they are functionally and mechanically identical.

Features

- Fully decoded, low-current PNP inputs
- S387 has open-collector outputs for easy word expansion
- S287 is functionally equivalent but has TRI-STATE outputs
- Provides the versatility of custom designs virtually "off the shelf"
- Applications include:
  - Microprogramming
  - Look-up tables for any fixed program
  - Parallel Code Converters
  - Sequence, routine, and subroutine generators
  - Random logic function generator
- Interchangeable with most other 256 words by 4-bit TTL PROMs/ROMs
- Fully compatible with most TTL and other saturated low level logic families
- Schottky-clamped for high performance:
  - Chip-select access time 15 ns typ
  - Address access time 30 ns typ

Connection Diagram



54S287(J); 74S287(J), (N);
54S387(J); 74S387(J), (N)

To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54S/74S S287 MIN	S287 TYP(1)	S287 MAX	S387 MIN	S387 TYP(1)	S387 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2			−1.2	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V	V_{OH} = 2.4V			N/A			50	μA
			V_{OH} = 5.5V			N/A			100	μA
			DM54			−2.0			N/A	mA
			DM74			−6.5			N/A	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4	3.2				5.5	V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA				0.5			0.5	V
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V	V_O = 0.5V			−50			N/A	μA
			V_O = 2.4V			50			N/A	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−100		N/A		mA
I_{CC}	Supply Current	V_{CC} = Max(3)			100	135		100	135	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

(3) I_{CC} is measured with outputs open and both $\overline{CS}$ inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	DM54S/74S S287 CONDITIONS	S287 MIN	S287 TYP	S287 MAX	S387 CONDITIONS	S387 MIN	S387 TYP	S387 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address	Any	C_L = 30 pF, R_L = 400Ω		30		C_L = 30 pF to GND, R_{L1} = 400Ω to V_{CC}, R_{L2} = 600Ω to GND		35		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address	Any			30				35		ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Chip Select	Any			N/A				15		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Chip Select	Any			N/A				15		ns
t_{ZH}	Output Enable Time to High Level	Chip Select	Any			15				N/A		ns
t_{ZL}	Output Enable Time to Low Level	Chip Select	Any			15				N/A		ns
t_{HZ}	Output Disable Time From High Level	Chip Select	Any	C_L = 5 pF, R_L = 400Ω		12				N/A		ns
t_{LZ}	Output Disable Time From Low Level	Chip Select	Any			12				N/A		ns

Notes

(4) When measuring times from address inputs, both $\overline{CS}1$ and $\overline{CS}2$ are low. When measuring times from chip-select inputs, the address inputs are held steady.

64-Bit Read/Write Memories with Open Collector Outputs

General Description

These 64-bit active element memories are Schottky-clamped TTL arrays organized as 16 words of four bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a (standard) Series 54S/74S load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are at a high logic level (off).

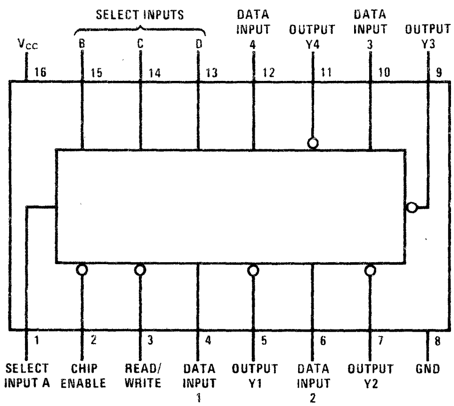
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable input is low. When the chip-enable input is high, the outputs are high (off).

The fast access time of the S289 makes it particularly attractive for implementing high performance memory functions requiring access times on the order of 25 ns. The unique functional capability of the S289 outputs being high during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus organized system without the need for interface circuits.

Features

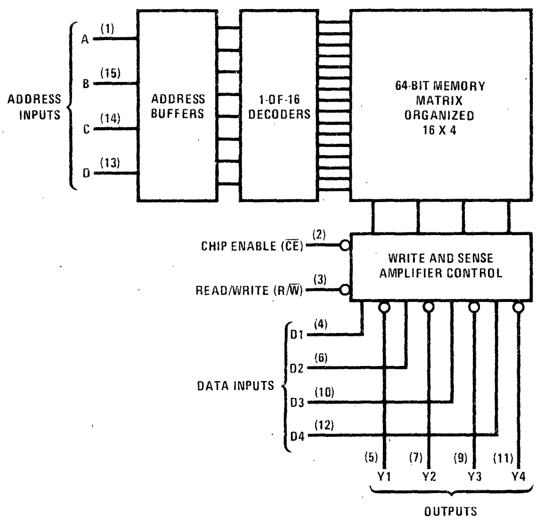
- Schottky-clamped for high-speed applications:
  - Access from chip-enable inputs 12 ns typ
  - Access from address inputs 25 ns typ
- Open-collector outputs for controlled-impedance bus lines
- DM54S189/DM74S189 are functionally equivalent but have TRI-STATE outputs
- Chip-enable input simplifies system decoding
- Compatible with Intel 3101A in most applications

Connection Diagram



54S289(J); 74S289(J), (W)

Logic Diagram



Truth Table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = High Level, L = Low Level, X = Don't Care

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54S/74S S289 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	μA
V_{OH}	High Level Output Voltage					5.5	V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA	DM54			0.5	V
			DM74			0.45	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{CC}	Supply Current	V_{CC} = Max(2)			75	105	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

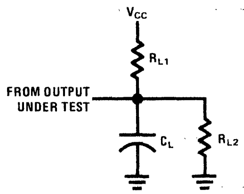
(2) I_{CC} is measured with all inputs grounded, and the outputs open.

Switching Characteristics over recommended operating ranges of V_{CC} and T_A (unless otherwise noted)

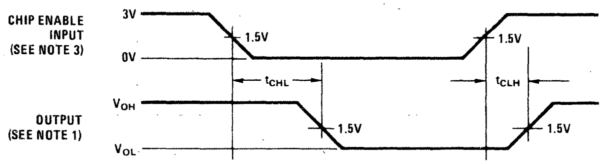
PARAMETER			CONDITIONS	DM54S S289 MIN	TYP	MAX	DM74S S289 MIN	TYP	MAX	UNITS
t_{AA}	Access Times From Address		C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600Ω		25	50		25	35	ns
t_{CLH}	Disable Time From Chip Enable				12	25		12	17	ns
t_{CHL}	Enable Time From Chip Enable				12	25		12	17	ns
t_{WHL}	Sense-Recovery Time From Read/Write				22	40		22	35	ns
t_{WP}	Width of Write-Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Setup Time	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time	Address From Read/Write		0			0			ns
t_{DHW}		Data From Read/Write		0			0			ns
t_{CHW}		Chip Enable From Read/Write		0			0			ns

Parameter Measurement Information

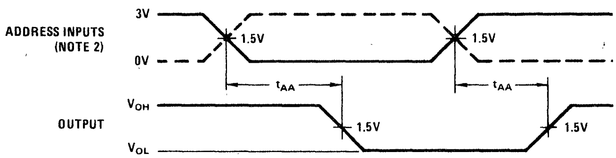
LOAD CIRCUIT



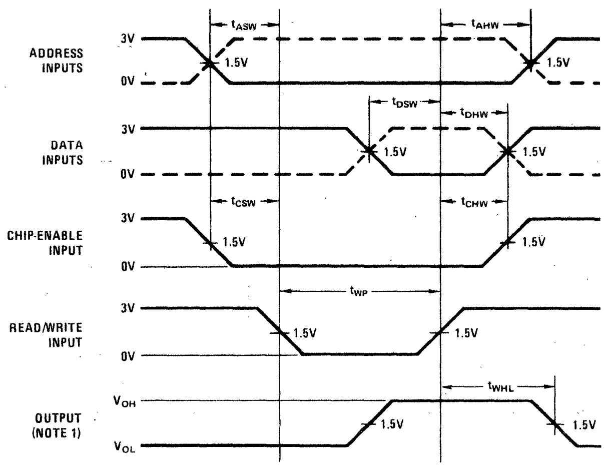
ENABLE AND DISABLE TIME FROM CHIP ENABLE



ACCESS TIME FROM ADDRESS INPUTS



WRITE CYCLE



Notes

(1) Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

(2) When measuring delay times from address inputs, the chip enable input is low and the read/write input is high.

(3) When measuring delay times from chip enable input, the address inputs are steady state and the read/write input is high.

(4) Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} \approx 50\Omega$.

TRI-STATE 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, mode, and output control inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high to low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

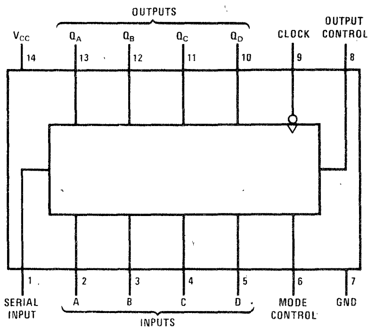
Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the register is not affected.

Features

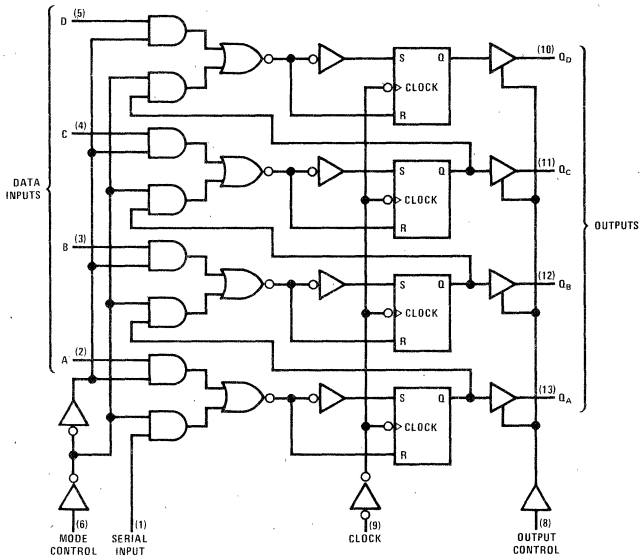
- TRI-STATE versions of DM54LS95B/DM74LS95B
- Schottky diode clamped transistors
- Low power dissipation (enabled) 70 mW typical
- Applications:
  N-bit serial-to-parallel converter
  N-bit parallel-to-serial converter
  N-bit storage register

Connection Diagram



54LS295A/74LS295A(J), (N), (W)

Logic Diagram



Truth Table

INPUTS							OUTPUTS			
MODE CONTROL	CLOCK	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
			A	B	C	D				
H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}

When the output control is low, the outputs are disabled to the high-impedance state; however, sequential operation of the registers is not affected.

H = High Level (steady-state), L = Low Level (steady-state), X = Don't Care (any input including transitions)
↓ = Transition from high to low level
a, b, c, d = The level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.
†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54LS LS295A MIN	DM54LS LS295A TYP(1)	DM54LS LS295A MAX	DM74LS LS295A MIN	DM74LS LS295A TYP(1)	DM74LS LS295A MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−1			−2.6	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.4	3.1		V
I_{OL}	Low Level Output Current					4			8	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{IL} = Max	I_{OL} = 8 mA					0.35	0.5	
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V	V_O = 0.4V			−20			−20	μA
		V_{IL} = Max	V_O = 2.7V			20			20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−130	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max(3)	Condition A		14	23		14	23	mA
			Condition B		15	25		15	25	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) I_{CC} is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the following conditions:
A. Output control at 4.5V and a momentary 3V, then ground, applied to clock input.
B. Output control and clock input grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM54LS/74LS LS295A MIN	DM54LS/74LS LS295A TYP	DM54LS/74LS LS295A MAX	UNITS
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 400Ω	20	28		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output			40	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			47	70	ns
t_{ZH}	Output Enable Time to High Level			15	25	ns
t_{ZL}	Output Enable Time to Low Level			21	30	ns
t_{HZ}	Output Disable Time From High Level	C_L = 5 pF, R_L = 400Ω		39	60	ns
t_{LZ}	Output Disable Time From Low Level			32	50	ns
$t_{W(CLOCK)}$	Width of Clock Pulse		25			ns
t_{SETUP}	Setup Time, High Level or Low Level Data		20			ns
t_{HOLD}	Hold Time, High Level or Low Level Data		20			ns

Quad 2-Multiplexers with Storage

General Description

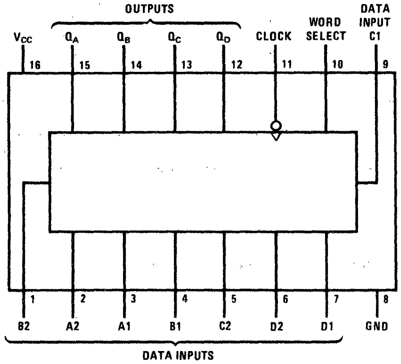
These integrated circuits provide essentially the equivalent functional capabilities of two separate MSI functions (DM54157/DM74157 or DM54LS157/DM74LS157 and DM54175/DM74175 or DM54LS175/DM74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is entered into the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is then clocked to the output terminals on the negative-going edge of the clock pulse.

Features

- Selects one of two 4-bit data sources and stores data synchronously with system clock
- Applications:
  - Dual source for operands and constants in arithmetic processor; can release processor register files for acquiring new data
  - Implement separate registers capable of parallel exchange of contents, yet retain external load capability
  - Universal type register for implementing various shift patterns; even has compound left-right capabilities

Connection Diagram



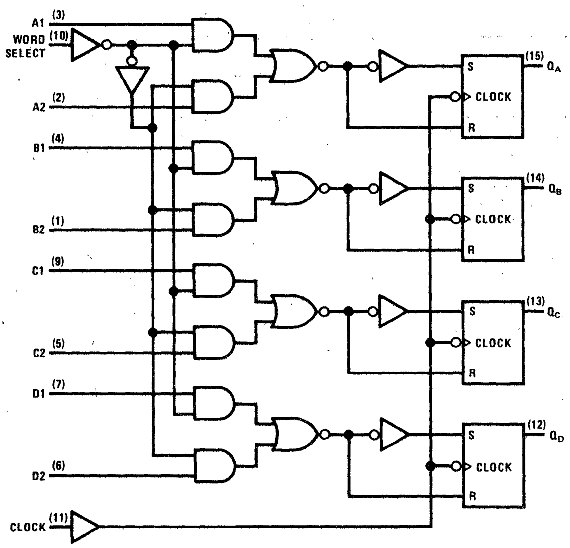
54LS298/74LS298(J), (N), (W)

Truth Table

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↓ = Transition from high to low level
a1, a2, etc. = The level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = The level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS			DM54LS/74LS LS298 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage			DM54			0.7	V
				DM74			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
I_{OH}	High Level Output Current						−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V		DM54	2.5	3.4		V
		V_{IL} = Max, I_{OH} = −400μA		DM74	2.7	3.4		
I_{OL}	Low Level Output Current			DM54			4	mA
				DM74			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OL} = 4 mA			0.25	0.4	V
		V_{IL} = Max	I_{OL} = 8 mA	DM74		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)			−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max(3)				13	21	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5V, followed by ground, to the clock input.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER			CONDITIONS	DM54LS/74LS LS298 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		C_L = 15 pF, R_L = 2 kΩ		18	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				21	32	ns
t_W	Width of Clock Pulse, High or Low Level			20			ns
t_{SETUP}	Setup Time	Data		15			ns
		Word Select		25			
t_{HOLD}	Hold Time	Data		5			ns
		Word Select		0			

Typical Applications

Figure 1 illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.

When the word select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered into the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the LS298 is a register that can be designed specifically for supporting multiplier or division operations. *Figure 2* is an example of a one place/two place shift register.

When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

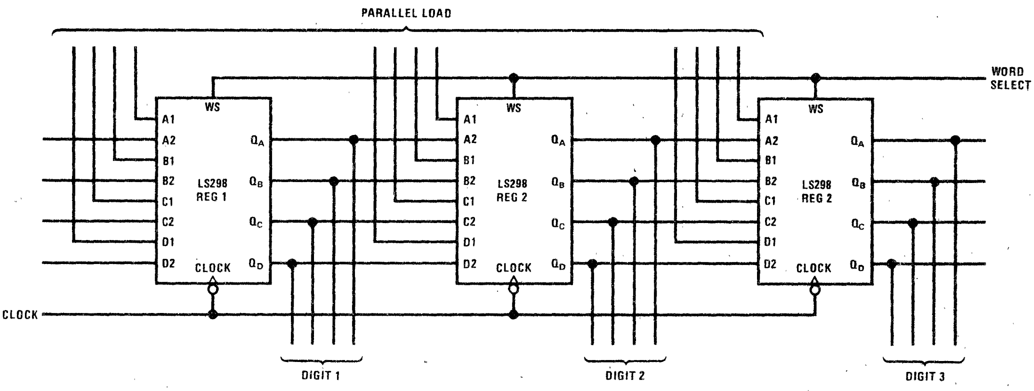


FIGURE 1

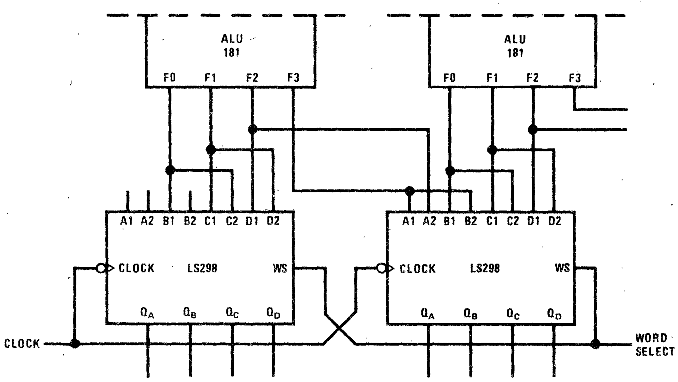


FIGURE 2

TRI-STATE Octal D Flip-Flops

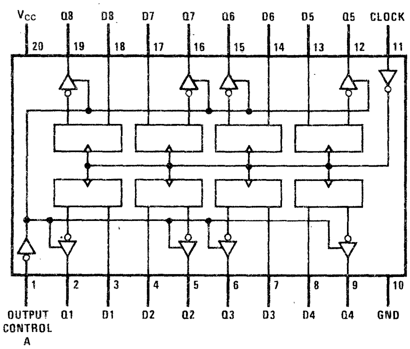
General Description

These 8-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs capable of driving highly-capacitive or low-impedance loads. When the output control is taken to a high logic level, the outputs go into the high impedance state. When a low logic level is applied to the output control, data at the D inputs are loaded into their respective flip-flops on the next positive-going transition of the clock. Clocked flip-flops provide fully synchronous operation and, in addition, these devices come in the new 20-pin dual-in-line packages with the 0.3" centers.

Features

- TRI-STATE bus driving outputs
- Parallel access for loading and reading
- Many applications
  - Holding/working registers
  - I/O register port
  - Buffer registers
  - Register files
- Typical propagation delay 19 ns

Connection Diagram

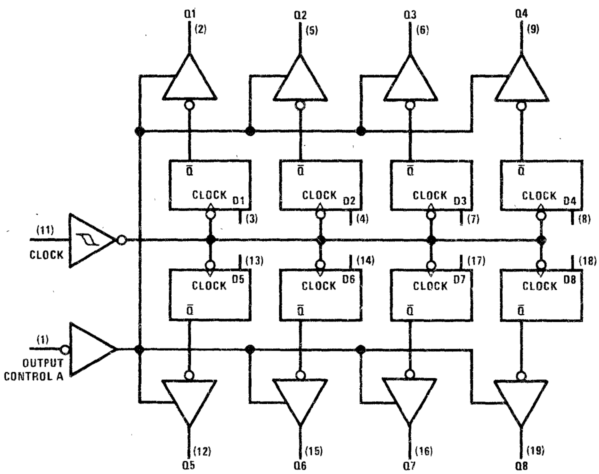


54LS374/74LS374(N)

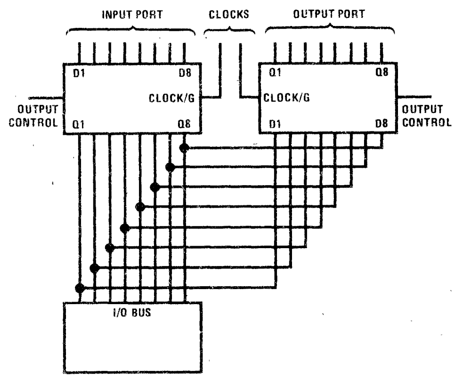
Truth Table

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

Logic Diagram



Typical Application



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54 LS374 MIN	DM54 LS374 TYP(1)	DM54 LS374 MAX	DM74 LS374 MIN	DM74 LS374 TYP(1)	DM74 LS374 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−1.0			−5.0	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −1 mA	2.5						V
		V_{IH} = 2V	I_{OH} = −2.6 mA				2.7			V
		V_{IL} = Max	I_{OH} = −5 mA				2.4			V
I_{OL}	Low Level Output Current					4			8	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	I_{OL} = 4 mA			0.4			0.4	V
		V_{IL} = Max	I_{OL} = 8 mA						0.5	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V	V_O = 0.4V			−20			−20	μA
		V_{IL} = Max	V_O = 2.7V			20			20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−130	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max				50			50	mA

Notes:

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER		FROM	TO	CONDITIONS	DM54LS/74LS LS374 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 2 kΩ	25	30		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Output			18	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Output			20	30	ns
t_{ZH}	Output Enable Time to High Level						15	20	ns
t_{ZL}	Output Enable Time to Low Level						10	20	ns
t_{HZ}	Output Disable Time from High Level				C_L = 5 pF, R_L = 2 kΩ		13	20	ns
t_{LZ}	Output Disable Time from Low Level						15	20	ns
t_{SETUP}	Setup Time	Data				10			ns
		Output Control				20			ns
t_{HOLD}	Hold Time	Data				10			ns
		Output Control				2			ns

TRI-STATE 4-Bit Cascadable Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, load/shift, output control and direct overriding clear inputs.

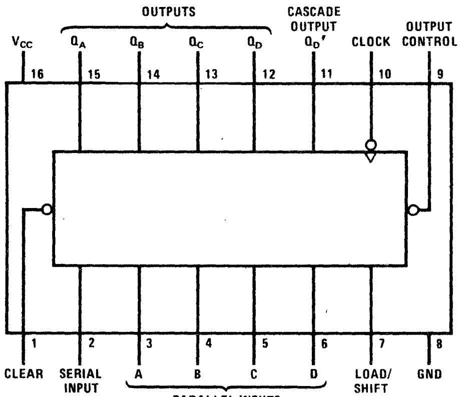
Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high to low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at the output control input. The outputs then present a high impedance, and neither load nor drive the bus line; however, sequential operation of the registers is not affected. During the high-impedance mode, the output at $Q_D{}'$ is still available for cascading.

Features

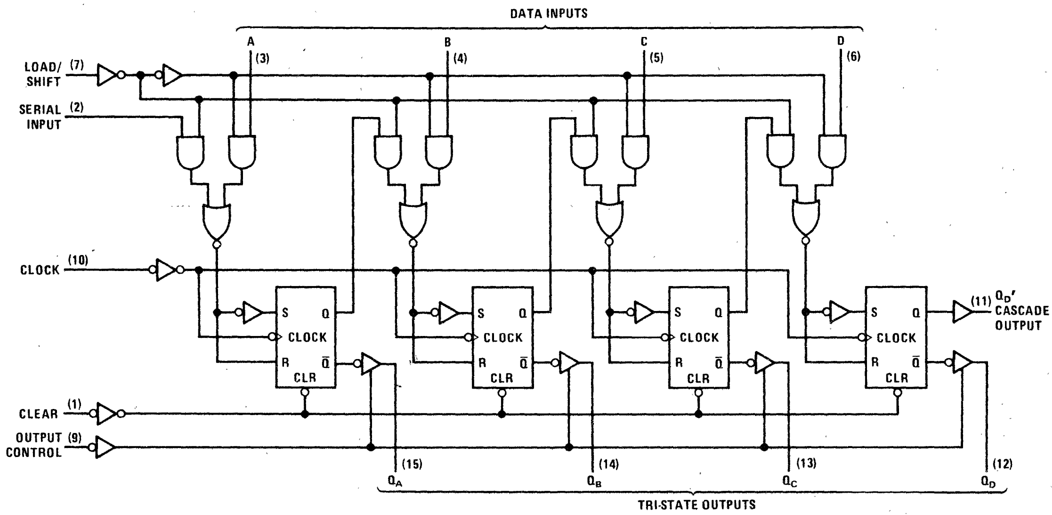
- Applications:
  - N-bit serial-to-parallel converter
  - N-bit parallel-to-serial converter
  - N-bit storage register
- TRI-STATE, 4-bit, cascadable, parallel-in, parallel-out registers
- Schottky diode clamped transistors
- Low power dissipation (enabled) 75 mW typical

Connection Diagram



54LS395/74LS395(J), (N), (W)

Logic Diagram



Truth Table

INPUTS								TRI-STATE OUTPUTS				CASCADE OUTPUT
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D	Q_D'
				A	B	C	D					
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

H = High Level (steady state), L = Low Level (steady state),

X = Don't Care (any input including transitions)

↓ = Transition from high to low level.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}, = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the more recent ↓ transition of the clock.

When the output control is high, the TRI-STATE outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_D' are not affected.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54LS LS395 MIN	TYP(1)	MAX	DM74LS LS395 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−1			−2.6	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.4	3.1		V
I_{OL}	Low Level Output Current					4			8	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = Max	V_O = 0.4V			−20			−20	µA
			V_O = 2.7V			20			20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20			20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−130	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max(3)	Condition A		18	29		18	29	mA
			Condition B		15	25		15	25	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) I_{CC} is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the following conditions:
  A. Output control at 4.5V and a momentary 3V, then ground, applied to clock input.
  B. Output control and clock input grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM54LS/74LS LS395 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency		25	35		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 400Ω		18	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			21	32	ns
t_{ZH}	Output Enable Time to High Level			15	25	ns
t_{ZL}	Output Enable Time to Low Level			20	30	ns
t_{HZ}	Output Disable Time From High Level	C_L = 5 pF, R_L = 400Ω		30	50	ns
t_{LZ}	Output Disable Time From Low Level			30	50	ns
$t_{W(CLOCK)}$	Width of Clock Pulse		25			ns
t_{SETUP}	Setup Time, High Level or Low Level Data		20			ns
t_{HOLD}	Hold Time, High Level or Low Level Data		10			ns

TRI-STATE 4 by 4 Register Files

General Description

These register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location, and reading from another word location, simultaneously.

Four data inputs are available to supply the word to be stored. Location of the word is determined by the write select inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

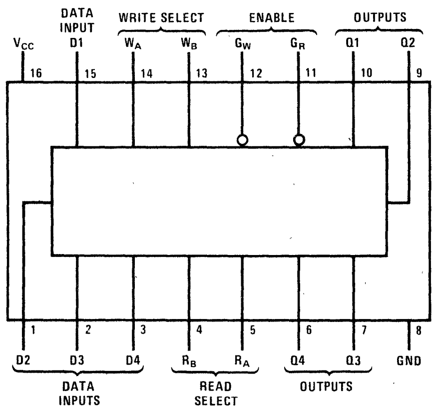
This arrangement—data entry addressing separate from data read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 ns typical) and the read time (24 ns typical). The register file has a non-volatile readout in that data is not lost when addressed.

All inputs (except read enable and write enable) are buffered to lower the drive requirements to one normal Series 54LS/74LS load, and input clamping diodes minimize switching transients to simplify system design. High speed, double ended AND-OR-INVERT gates are employed for the read-address function and have high sink current, TRI-STATE outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

Features

- For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Separate read/write addressing permits simultaneous reading and writing
- Organized as 4 words of 4 bits
- Expandable to 512 words of n-bits
- TRI-STATE versions of DM54LS170/DM74LS170
- Fast access times 20 ns typ

Connection Diagram



54LS670/74LS670(J), (N), (W)

Truth Tables

WRITE TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Notes:

(A) H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (Off)

(B) (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

(C) Q_0 = The level of Q before the indicated input conditions were established.

(D) W0B1 = The first bit of word 0, etc.

To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM54LS LS670 MIN	DM54LS LS670 TYP(1)	DM54LS LS670 MAX	DM74LS LS670 MIN	DM74LS LS670 TYP(1)	DM74LS LS670 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−1.0			−2.6	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		2.5	3.4		2.7	3.4		V
I_{OL}	Low Level Output Current					4			8	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = Max	V_O = 0.4V			−20			−20	μA
			V_O = 2.7V			20			20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V	Any D, R, or W			0.1			0.1	mA
			G_W			0.2			0.2	
			G_R			0.3			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Any D, R, or W			20			20	μA
			G_W			40			40	
			G_R			60			60	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Any D, R, or W			−0.4			−0.4	mA
			G_W			−0.8			−0.8	
			G_R			−1.2			−1.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−130	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			30	50		30	50	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

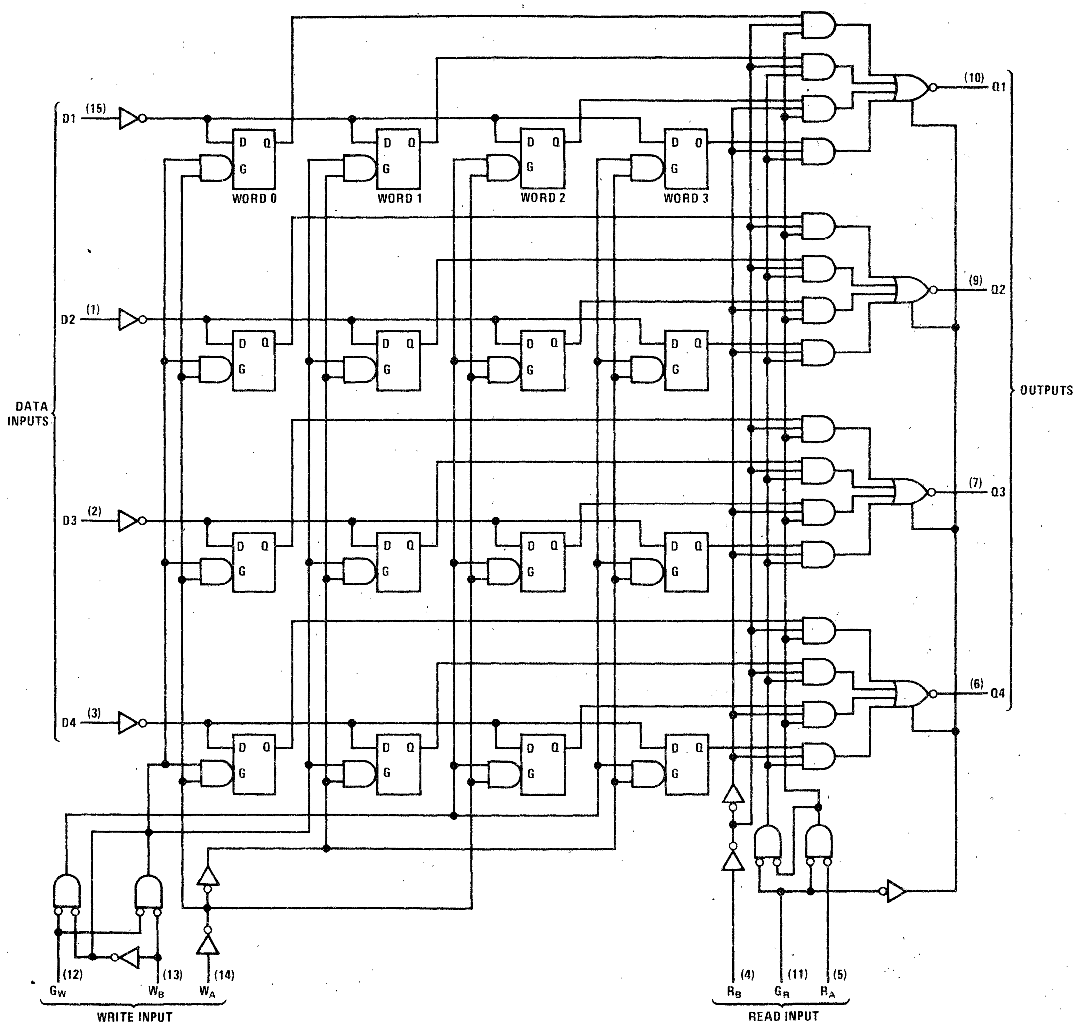
	PARAMETER		FROM (INPUT)	TO (OUTPUT)	DM54LS/74LS LS670 CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Read Select	Any Q	$C_L = 15$ pF, $R_L = 2$ kΩ		23	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Read Select	Any Q	$C_L = 15$ pF, $R_L = 2$ kΩ		25	45	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Write Enable	Any Q	$C_L = 15$ pF, $R_L = 2$ kΩ		26	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Write Enable	Any Q	$C_L = 15$ pF, $R_L = 2$ kΩ		28	50	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Data	Any Q	$C_L = 15$ pF, $R_L = 2$ kΩ		25	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Data	Any Q	$C_L = 15$ pF, $R_L = 2$ kΩ		23	40	ns
t_{ZH}	Output Enable Time to High Level		Read Enable	Any Q	$C_L = 5$ pF, $R_L = 2$ kΩ		15	35	ns
t_{ZL}	Output Enable Time to Low Level		Read Enable	Any Q	$C_L = 5$ pF, $R_L = 2$ kΩ		22	40	ns
t_{HZ}	Output Disable Time From High Level		Read Enable	Any Q	$C_L = 5$ pF, $R_L = 2$ kΩ		30	50	ns
t_{LZ}	Output Disable Time From Low Level		Read Enable	Any Q	$C_L = 5$ pF, $R_L = 2$ kΩ		16	35	ns
t_W	Width of Write-Enable or Read-Enable Pulse					25			ns
t_{SETUP}	Setup Times, High or Low Level Data(4)	Data Input With Respect to Write-Enable, $t_{SETUP(D)}$				10			ns
		Write-Select With Respect to Write-Enable, $t_{SETUP(W)}$				15			ns
t_{HOLD}	Hold Times, High or Low Level Data(4)	Data Input With Respect to Write-Enable, $t_{HOLD(D)}$				15			ns
		Write-Select With Respect to Write-Enable, $t_{HOLD(W)}$				5			ns
t_{LATCH}	Latch Time for New Data(5)					25			ns

Notes

(4) Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{SETUP(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{HOLD(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

(5) Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

Logic Diagram



National Semiconductor
PROPRIETARY DEVICES
Section 3

RATINGS		7X/8X SERIES	7XL/8XL SERIES	71LS/81LS DIODE INPUTS	71LS/81LS EMITTER INPUTS	75S/85S SERIES	UNITS
Maximum Allowable Supply Voltage		7	8	7	7	7	V
Guaranteed Operating Supply Voltage Range	Mil	4.50 to 5.50					V
	Coml	4.75 to 5.25					
Maximum Input Voltage		5.5	5.5	7	5.5	5.5	V
Maximum Voltage to Open-Collector Outputs*		7	8	7	7	7	V
Operating Free-Air Temperature Range	Mil	–55 to +125					°C
	Coml	0 to +70					
Storage Temperature Range		–65 to +150					°C

Proprietary

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Proprietary

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Quad 2-Input NAND Gates with Resistive Pull Up

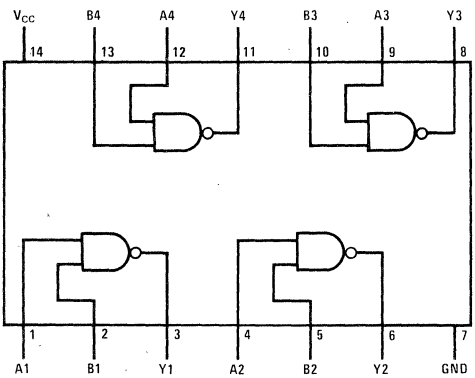
General Description

These quad two-input NAND gates feature internally-connected, 20 kΩ pull-up resistors on the outputs. The pinout is the same as the very popular DM54L03/DM74L03, and these devices provide the same "one-tenth-power technology" as well.

Features

- Typical power dissipation 12 mW
- Typical propagation delay 115 ns

Connection Diagram



80L06(N)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM80L L06 MIN	DM80L L06 TYP(1)	DM80L L06 MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.7	V
I_{OH}	High Level Output Current				200	μA
V_{OH}	High Level Output Voltage	$V_{CC} = 5.0V$, $V_{IL} = 0.7V$, $I_{OH} = 100\mu A$	2.0	2.5		V
I_{OL}	Low Level Output Current				3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, $V_{IH} = 2V$			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, $V_I = 5.5V$			100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, $V_I = 2.4V$		<1	10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, $V_I = 0.3V$		−0.12	−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−0.17	−0.25	−0.33	mA
I_{CCH}	Supply Current (Total with Outputs High)	V_{CC} = Max, $V_I = 0$		0.48	0.8	mA
I_{CCL}	Supply Current (Total with Outputs Low)	V_{CC} = Max, $V_I = 5V$		2.38	3.68	mA

Notes

(1) All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER	FROM	TO	CONDITIONS	DM80L L06 MIN	DM80L L06 TYP	DM80L L06 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Input	Output	$C_L = 15$ pF, $R_L = 4\ k\Omega$		193	290	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Input	Output			37	56	ns

DM7090/8090 Quad Inverter plus Dual 2-Input NAND Gates
DM7091/8091 Quad 2-Input NAND Buffers
DM7092/8092 Dual 5-Input NAND Gates

General Description

DM7090/DM8090

These devices optimize the flexible utilization of the popular 16-pin package by providing two, 2-input NAND gates plus four inverters in the same package. The electrical specifications are completely compatible with all series 54/74 devices.

DM7091/DM8091

These devices provide four, 2-input NAND buffers in the same package, each with a fan-out of 30 standard TTL loads. These devices are very similar to the popular DM5437/DM7437; however, the DIP pinout is the same as the 5401/7401, whereas the DIP pinout of the 5437/7437 is the same as the 5400/7400.

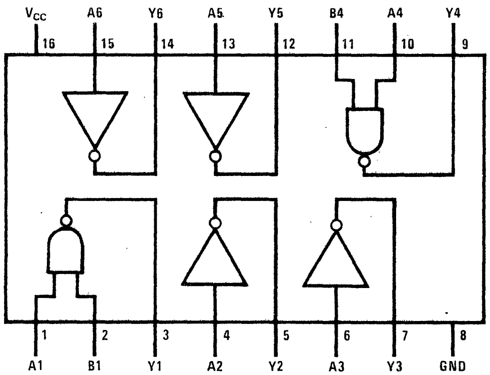
DM7092/DM8092

These devices provide two, 5-input NAND gates in the same package. Their primary advantage is that they fill a product void in the popular DM5400/DM7400 family. The electrical specifications are completely compatible with the series 54/74 devices.

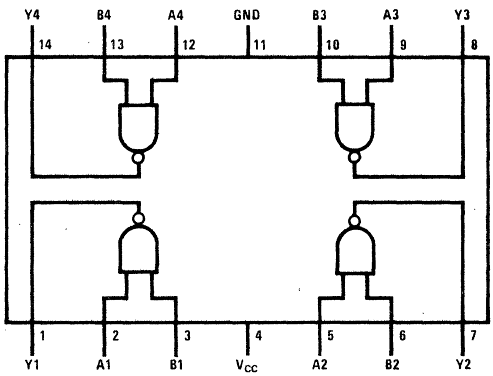
Features

- Typical propagation delay 11 ns
- Typical power dissipation
  - DM7090/DM8090 115 mW
  - DM7091/DM8091 155 mW
  - DM7092/DM8092 35 mW

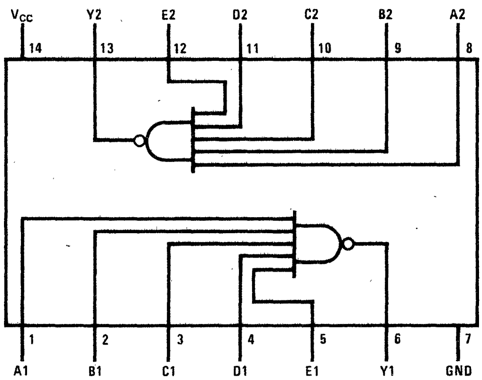
Connection Diagrams



7090/8090(J), (N), (W)



7091/8091(J), (N), (W)



7092/8092(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM70/80 90 MIN	90 TYP(1)	90 MAX	91 MIN	91 TYP(1)	91 MAX	92 MIN	92 TYP(1)	92 MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, T_A = 25°C			−1.5			−1.5			−1.5	V
I_{OH}	High Level Output Current				−400			−1200			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = Max	2.4			2.4			2.4			V
I_{OL}	Low Level Output Current				16			48			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2.0V, I_{OL} = Max			0.4			0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40			40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6			−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−18		−55	−18		−70	−18		−55	mA
I_{CCH}	Supply Current (Total with Outputs High)	V_{CC} = Max, V_I = 0			11			15			3.6	mA
I_{CCL}	Supply Current (Total with Outputs Low)	V_{CC} = Max, V_I = 5.0V			31			46			10.2	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS	DM70/80 90 MIN	90 TYP	90 MAX	91 MIN	91 TYP	91 MAX	92 MIN	92 TYP	92 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Input	Output	C_L = 15 pF, R_L = 400Ω		13	25		13	22		13	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Input	Output			9	15		8	15		8	15	ns

TRI-STATE Quad Buffers

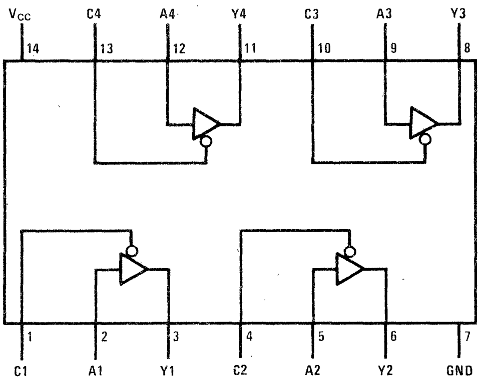
General Description

The DM7093/DM8093 and DM7094/DM8094 are quad two-input buffers which accept normal TTL or DTL input levels; and have outputs which provide either normal low-impedance TTL characteristics, or a high-impedance third logic state. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state. The other input simply passes the non-inverted data through the buffer. The DM7093/DM8093 provides the high-impedance state when a high logic level is applied to the control input, the DM7094/DM8094 when a low logic level is applied to the control input. The low output impedance of these devices provides good capacitive-drive capability and rapid transition from the low to the high logic levels, thus assuring both speed and waveform integrity. It is possible to connect as many as 128 devices to a common bus line, and still have adequate drive capability.

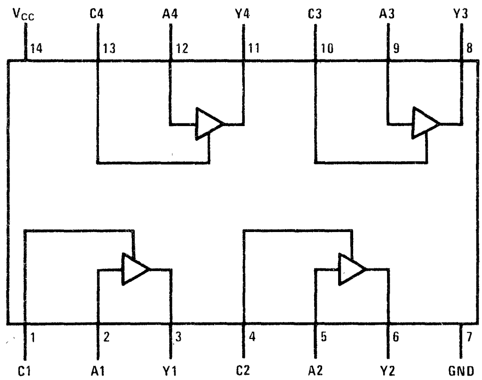
Features

- Pin equivalent to DM54125/74125 (7093/8093) and DM54126/74126 (7094/8094)
- Up to 128 devices can be connected to a common bus line
- High capacitive-drive capability
- Independent control of each buffer
- Typical propagation delay—12 ns

Connection Diagrams



7093/8093(J), (N), (W)



7094/8094(J), (N), (W)

Truth Tables

DM7093/DM8093

DATA	CONTROL	OUTPUT
H	L	H
L	L	L
X	H	Hi-Z

DM7094/DM8094

DATA	CONTROL	OUTPUT
H	H	H
L	H	L
X	L	Hi-Z

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM70 93, 94 MIN	DM70 93, 94 TYP(1)	DM70 93, 94 MAX	DM80 93, 94 MIN	DM80 93, 94 TYP(1)	DM80 93, 94 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−2.0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4	3.4		2.4	3.1		V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V V_{IL} = 0.8V	V_O = 0.4V			−40			−40	μA
			V_O = 2.4V			40			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−70	−28		−70	mA
I_{CCH}	Supply Current (Total, Outputs High)	V_{CC} = Max			32	54		32	54	mA
I_{CCL}	Supply Current (Total, Outputs Low)	V_{CC} = Max			36	62		36	62	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	DM70/80 93 MIN	DM70/80 93 TYP	DM70/80 93 MAX	DM70/80 94 MIN	DM70/80 94 TYP	DM70/80 94 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 400Ω		10	15		10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	18		12	18	ns
t_{ZH}	Output Enable Time to High Level			12	18		13	19	ns
t_{ZL}	Output Enable Time to Low Level			16	25		16	25	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 400Ω		5	8		10	16	ns
t_{LZ}	Output Disable Time from Low Level			9	14		14	20	ns

TRI-STATE Hex Buffers

General Description

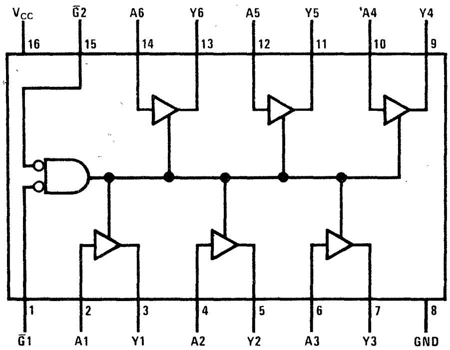
These devices provide six, two-input buffers in each package. Both the standard (7400 compatible) TTL technology, and the "true tenth-power" (74L compatible) low power versions are available for each of the four types. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 95 and 97 present the true data at the outputs, while the 96 and 98 are inverting. On the 95 and 96 versions, all six control lines for TRI-STATE enable are common in a single line. On the 97 and 98 versions, four buffers are enabled from a common line, and the other two buffers from a separate common line. In all cases, the outputs are placed in the TRI-STATE condition by applying a high logic level to the control pins. With either the standard TTL or the low power versions of these circuits, it is possible to connect over 100 like devices to a common bus line and still have adequate drive capability.

Features

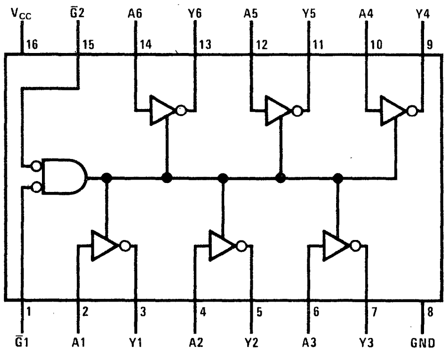
TYPE	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAY
95, 97	325 mW	12 ns
L95, L97	20 mW	34 ns
96, 98	295 mW	11 ns
L96, L98	15 mW	31 ns

- Pin equivalent to DM54365 (95), DM54366 (96), DM54367 (97), DM54368 (98)

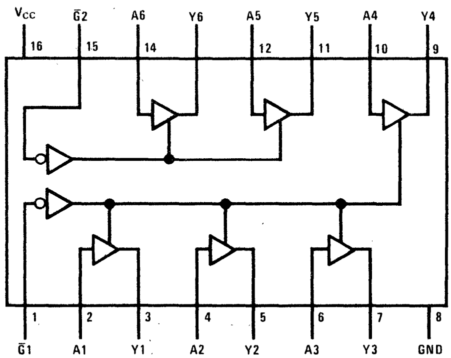
Connection Diagrams



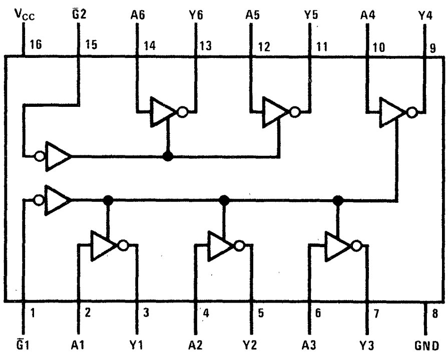
7095(J), (W); 8095(J), (N), (W);
70L95/80L95(J), (N), (W)



7096(J), (W); 8096(J), (N), (W);
70L96/80L96(J), (N), (W)



7097(J), (W); 8097(J), (N), (W);
70L97/80L97(J), (N), (W)



7098(J), (W); 8098(J), (N), (W);
70L98/80L98(J), (N), (W)

Truth Tables (Each Driver)

95, L95

INPUTS			OUTPUT
$\bar{G}1$	$\bar{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	H
L	L	L	L

96, L96

INPUTS			OUTPUT
$\bar{G}1$	$\bar{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	L
L	L	L	H

97, L97

INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Hi-Z
L	H	H
L	L	L

98, L98

INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Hi-Z
L	H	L
L	L	H

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM70/80 95, 96, 97, 98 MIN	TYP(1)	MAX	DM70L/80L L95, L96, L97, L98 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High Level Output Current	DM70			−2.0			−1.0	mA
		DM80			−5.2			−1.0	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max	2.4	3.1		2.4			V
I_{OL}	Low Level Output Current	DM70			32			2.0	mA
		DM80			32			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max, DM70			0.4			0.3	V
		DM80			0.4			0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = Max, V_O = 0.3V						−10	µA
		V_O = 0.4V			−40				µA
		V_O = 2.4V			40			10	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40			10	µA
I_{IL}	Low Level Input Current, A Input	V_{CC} = Max, Both $\overline{G}$ Inputs at 2V, V_I = 0.3V						−10	µA
		V_I = 0.5V			−40				µA
		Both $\overline{G}$ Inputs at 0.4V, V_I = 0.3V						−0.18	mA
		V_I = 0.4V			−1.6				mA
	$\overline{G}$ Input	V_I = 0.3V						−0.18	mA
		V_I = 0.4V			−1.6				mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−40		−115	−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max, 95, 97		65	85		4.0	5.8	mA
		96, 98		59	77		3.0	4.5	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for the DM70/DM8095, 96, 97, 98 duration of short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS BOTH	STD.	LOW POWER	DM70/80 95, 97 TYP	MAX	96, 98 TYP	MAX	DM70L/80L L95, L97 TYP	MAX	L96, L98 TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF	R_L = 400Ω	R_L = 4 kΩ	10	16	11	17	30	60	26	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				14	22	10	16	37	75	35	53	ns
t_{ZH}	Output Enable Time to High Level				21	35	21	35	47	96	42	90	ns
t_{ZL}	Output Enable Time to Low Level				24	37	24	37	21	45	42	75	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF			6	11	6	11	47	90	25	43	ns
t_{LZ}	Output Disable Time from Low Level				16	27	16	27	30	63	34	63	ns

TRI-STATE Quad 2-Input NAND Buffers

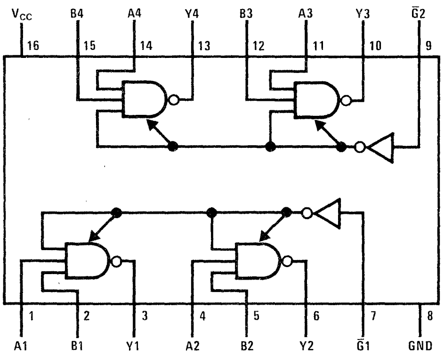
General Description

These devices provide four, two-input NAND buffers in each package. They accept normal TTL or DTL input levels, and have outputs which provide either normal low-impedance TTL characteristics, or a high-impedance third logic state. There are two independent disable lines, each of which controls two gates. When the disable input is taken to a high logic level, the outputs go into the high-impedance state. The low output impedance of these devices provides good capacitive-drive capability and rapid transition from the low to the high logic levels, thus assuring both speed and waveform integrity.

Features

- Combines logic gating with TRI-STATE outputs
- Typical propagation delay 9 ns
- High capacitive-drive capability
- Up to 128 devices can be connected to a common bus line

Connection Diagram



7099/8099(J), (N), (W)

Truth Table

DISABLE	INPUTS		OUTPUT
$\overline{G}$	A	B	Y
L	L	H	H
L	H	L	H
L	L	L	H
L	H	H	L
H	X	X	Hi-Z

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM7099 MIN	DM7099 TYP(1)	DM7099 MAX	DM8099 MIN	DM8099 TYP(1)	DM8099 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−2.0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 0.4V			−40			−40	µA
			V_O = 2.4V			40			40	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			40	µA
I_{IL}	Low Level Input Current, Either Data Input	V_{CC} = Max	$\overline{G}$ Input at 2V, V_I = 0.4V			−40			−40	µA
	Low Level Input Current, Either Data Input	V_{CC} = Max	$\overline{G}$ Input at 0.4V, V_I = 0.4V			−1.6			−1.6	mA
	Low Level Input Current, $\overline{G}$ Input	V_{CC} = Max	V_I = 0.4V			−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−25		−70	−25		−70	mA
I_{CC}	Supply Current	V_{CC} = Max				35			35	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM70/8099 MIN	DM70/8099 TYP	DM70/8099 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 400Ω		10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 50 pF, R_L = 400Ω		8	15	ns
t_{ZH}	Output Enable Time to High Level	C_L = 50 pF, R_L = 400Ω		13	20	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 50 pF, R_L = 400Ω		13	20	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 400Ω		4	7	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5 pF, R_L = 400Ω		11	17	ns

TRI-STATE Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

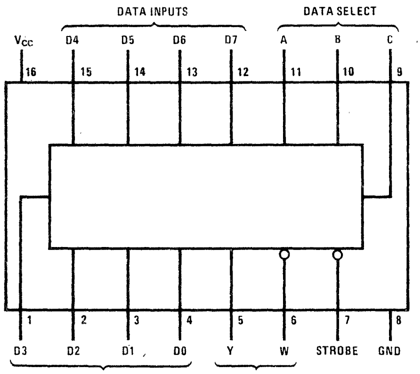
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE versions of DM54/74151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Pin equivalent DM54251/DM74251

TYPE	MAX NO. OF COMMON OUTPUTS	TYPICAL PROP DELAY TIME (D TO Y)	TYPICAL POWER DISSIPATION
DM7121	49	17 ns	155 mW
DM8121	129	17 ns	155 mW

Connection Diagram



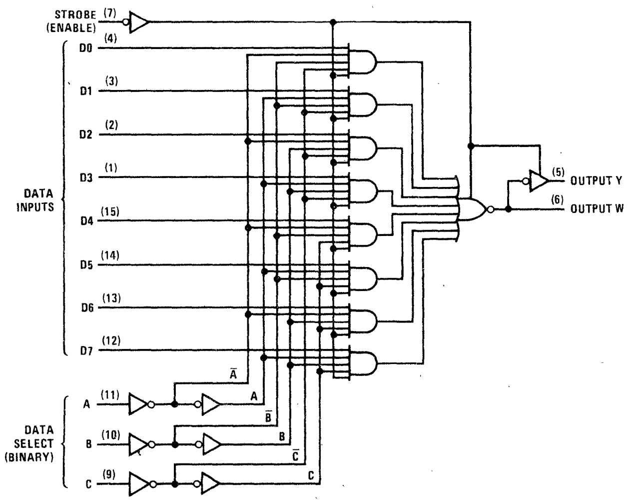
7121(J), (W); 8121(J), (N), (W)

Truth Table

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1. . .D7 = The level of the respective D input.

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM71/81 21 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current		DM54			−2	mA
			DM74			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4			V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA				0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			31	51	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) All inputs at 4.5V and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM71/81 21 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A, B, or C (4 levels)	Y	C_L = 50 pF, R_L = 400Ω		22	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A, B, or C (4 levels)	Y			23	36	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A, B, or C (3 levels)	W			18	29	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A, B, or C (3 levels)	W			16	27	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any D	Y			17	28	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Any D	Y			18	28	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any D	W			11	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Any D	W			10	15	ns
t_{ZH}	Output Enable Time to High Level	Strobe	Y			15	27	ns
t_{ZL}	Output Enable Time to Low Level	Strobe	Y			18	36	ns
t_{ZH}	Output Enable Time to High Level	Strobe	W			15	27	ns
t_{ZL}	Output Enable Time to Low Level	Strobe	W			19	38	ns
t_{HZ}	Output Disable Time from High Level	Strobe	Y	C_L = 5 pF, R_L = 400Ω		4	8	ns
t_{LZ}	Output Disable Time from Low Level	Strobe	Y			14	23	ns
t_{HZ}	Output Disable Time from High Level	Strobe	W			4	8	ns
t_{LZ}	Output Disable Time from Low Level	Strobe	W			15	23	ns

Quad 2-Input Data Selectors/Multiplexers

General Description

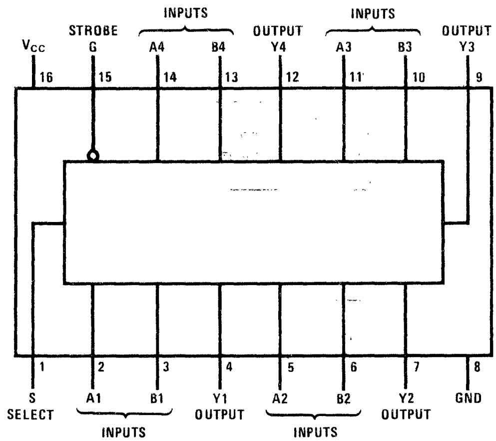
These devices contain four, two-input multiplexers with common input select logic and common output disable circuitry. The DM71L22/81L22 provides conventional totem-pole output TTL construction, whereas the DM7123/8123 and the DM71L23/81L23 provide both conventional TTL outputs and TRI-STATE outputs. When the enable/strobe input is at a low logic level, the outputs of all devices are conventional TTL. However, when the enable/strobe input is raised to a high logic level, the outputs of the DM71L22/81L22 go to the low logic state, and the outputs of the DM7123/8123 and DM71L23/81L23 go to the high-impedance third state. These devices provide the designer with TRI-STATE and/or low power pin/pin replacements for the popular 9322 and 54/74157 multiplexers.

Features

- Pin equivalents popular 9322 and 54/74157 multiplexers
- Both conventional TTL and TRI-STATE outputs available
- Both conventional TTL and "one-tenth-power technology" available

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL POWER DISSIPATION
7123/8123	9.5 ns	200 mW
71L22/81L22	40 ns	15 mW
71L23/81L23	40 ns	20 mW

Connection Diagram



71L22/81L22(J), (N), (W); 7123(J), (W);
8123(J), (N), (W); 71L23/81L23(J), (N), (W)

Truth Tables

L22

STROBE	SELECT	INPUTS A	INPUTS B	OUTPUT Y
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	L

23, L23

ENABLE	SELECT	INPUTS A	INPUTS B	OUTPUT Y
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Hi-Z

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM71/81 23 MIN	DM71/81 23 TYP(1)	DM71/81 23 MAX	DM71L/81L L22 MIN	DM71L/81L L22 TYP(1)	DM71L/81L L22 MAX	DM71L/81L L23 MIN	DM71L/81L L23 TYP(1)	DM71L/81L L23 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, T_A = 25°C				−1.5			N/A			N/A	V
I_{OH}	High Level Output Current		DM71			−2.0			−0.2			−0.2	mA
			DM81			−5.2			−0.2			−0.2	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OH} = Max		2.4			2.4	2.8		2.4	2.8		V
I_{OL}	Low Level Output Current		DM71			16			2.0			2.0	mA
			DM81			16			3.6			3.6	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OL} = Max	DM71			0.4		0.15	0.3		0.15	0.3	V
			DM81			0.4		0.20	0.4		0.20	0.4	
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max	V_O = 0.3V						N/A			−40	µA
		V_{IH} = 2V	V_O = 0.4V			−40			N/A				
		V_{IL} = Max	V_O = 2.4V			40			N/A			20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			10			10	µA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V						−0.18			−0.18	mA
			V_I = 0.4V		−1.0	−1.6							
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30	−50	−70	−3	−9	−15	−3	−9	−15	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			40	51		3	4		4	5.3	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) I_{CC} is measured with all inputs grounded, and all outputs open.

DM71/DM81L22,23,L23

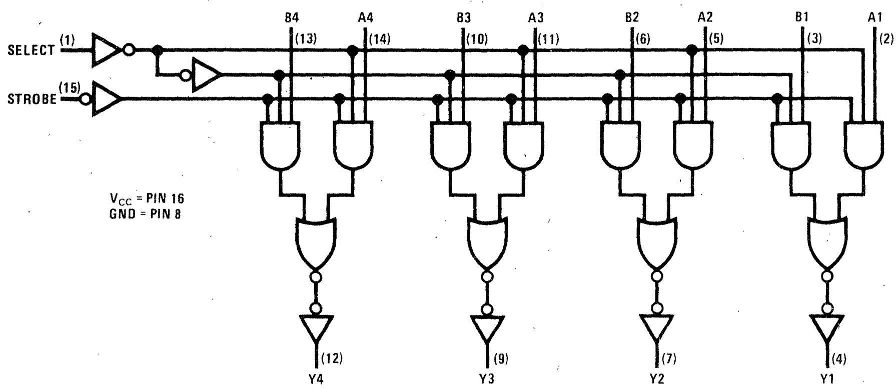
Proprietary

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

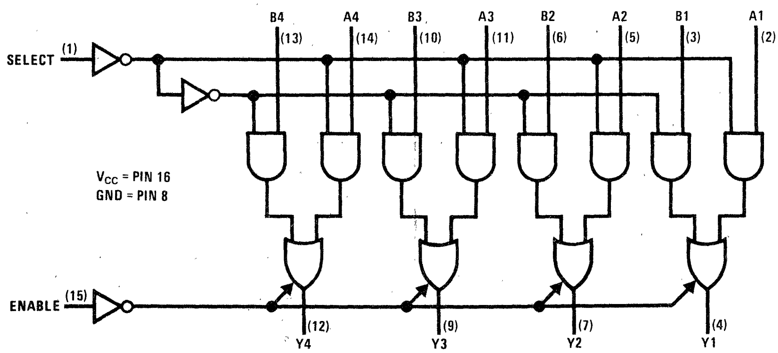
PARAMETER		FROM	TO	CONDITIONS DM71/81	CONDITIONS DM71L/81L	DM71/81 23 MIN	DM71/81 23 TYP	DM71/81 23 MAX	DM71L/81L L22 MIN	DM71L/81L L22 TYP	DM71L/81L L22 MAX	DM71L/81L L23 MIN	DM71L/81L L23 TYP	DM71L/81L L23 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	$C_L = 50$ pF, $R_L = 400\Omega$	$C_L = 50$ pF, $R_L = 4$ kΩ	4	8	15	20	40	80	20	40	80	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output			5	11	18	20	40	80	20	40	80	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	Output				N/A		30	60	120		N/A		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	Output				N/A		30	60	120		N/A		ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Output			5	15	23	35	70	140	35	70	140	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Output			8	17	24	25	50	100	25	50	100	ns
t_{ZH}	Output Enable Time to High Level					9	18	25		N/A		15	30	60	ns
t_{ZL}	Output Enable Time to Low Level					10	23	30		N/A		20	35	70	ns
t_{HZ}	Output Disable Time from High Level			$C_L = 5$ pF, $R_L = 400\Omega$	$C_L = 5$ pF, $R_L = 4$ kΩ	4	7	11		N/A		15	30	60	ns
t_{LZ}	Output Disable Time from Low Level					9	19	27		N/A		35	75	150	ns

Logic Diagrams

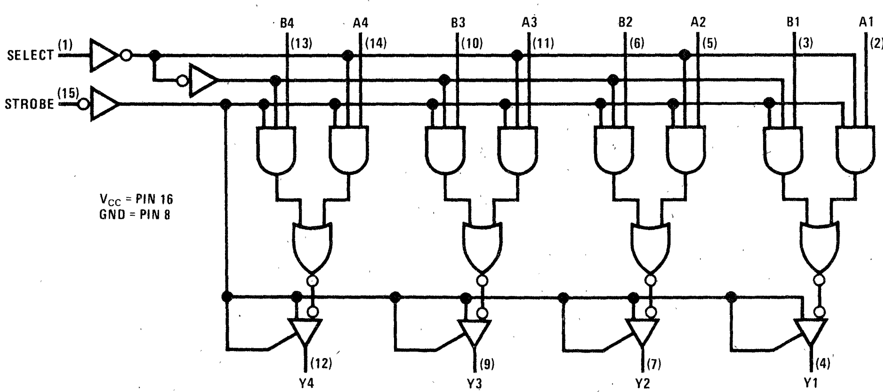
L22



23



L23



Magnitude Comparators

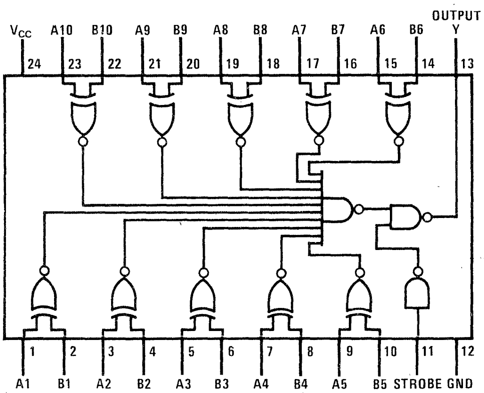
General Description

These devices offer comparisons to determine equality between two binary words. The DM7130/DM8130 compares two ten-bit words, and the DM7160/DM8160 compares two six-bit words. A strobe override is provided on both devices. When the strobe is taken to a high logic level, the output is forced to a high logic level. The devices also feature open collector outputs for expansion.

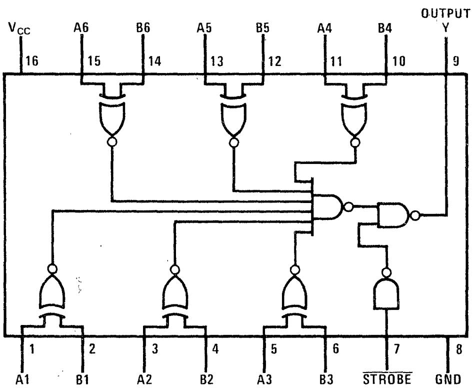
Features

- Typical propagation delay 21 ns
- Typical power dissipation
  - DM7130/8130 240 mW
  - DM7160/8160 205 mW
- Open-collector outputs for expansion

Connection Diagrams



7130(J), (F); 8130(J), (N), (F)



7160(J), (W); 8160(J), (N), (W)

Truth Table

CONDITION	$\overline{STROBE}$ S	OUTPUT Y
A = B, A ≠ B	H	H
A = B	L	H
A ≠ B	L	L

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM71/81 30 MIN	30 TYP(1)	30 MAX	60 MIN	60 TYP(1)	60 MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA T_A = 25°C			−1.5			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V V_{OH} = 5.5V			100			100	μA
V_{OH}	High Level Output Voltage				5.5			5.5	V
I_{OL}	Low Level Output Current				16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6			−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max		48	70		41	60	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM71/81 30 MIN	30 TYP	30 MAX	60 MIN	60 TYP	60 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 15 pF, R_L = 400Ω		15	25		15	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output			27	40		27	40	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	Output			9	18		9	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	Output			20	30		20	30	ns

6-Bit Unified Bus Comparators

General Description

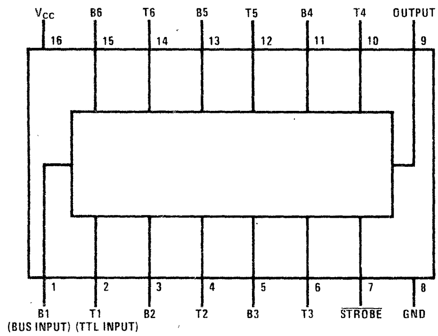
The DM7131/DM8131, DM7136/DM8136 compare two binary words of two-to-six-bits in length, and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65V typical hysteresis, which provides 1.4V noise immunity. The DM7131/DM8131 has active pull-up outputs and goes to the low state upon equality. The DM7136/DM8136 has open-collector outputs which go to the high state upon equality, and is expandable to n bits by collector-ORing. Both devices have an output latch which is strobe controlled.

The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to a logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

Features

- Low bus input current 15μA typ
- High bus input noise immunity 1.4 typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

Connection Diagram



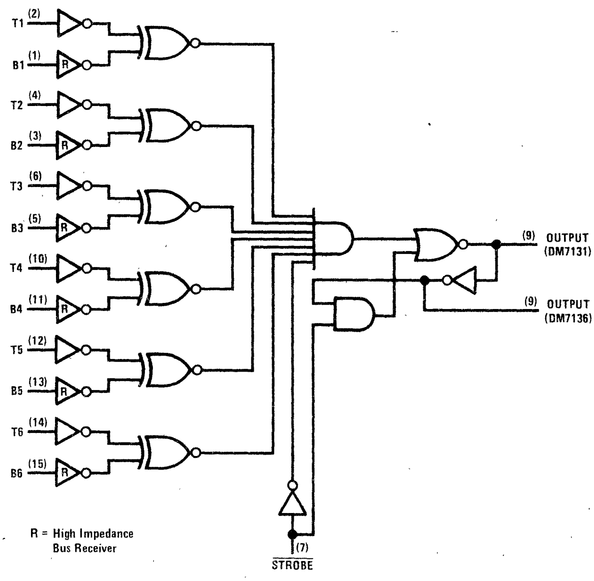
7131(J), (W); 8131(J), (N), (W);
7136(J), (W); 8136(J), (N), (W)

Truth Table

CONDITION	$\overline{\text{STROBE}}$	OUTPUT DM71/8131	OUTPUT DM71/8136
T = B, T ≠ B	H	Q_{N-1} *	Q_{N-1} *
T = B	L	L	H
T ≠ B	L	H	L

*Latched in previous state

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM71/81 31 MIN	31 TYP(1)	31 MAX	36 MIN	36 TYP(1)	36 MAX	UNITS
V_{IH}	High Level Input Voltage	(Exc. Bus Inputs)		2			2			V
V_{IL}	Low Level Input Voltage	(Exc. Bus Inputs)				0.8			0.8	V
V_{T+}	Positive Going Threshold Voltage	V_{CC} = 5V, Bus Inputs	DM71	1.40	1.75	2.0	1.40	1.75	2.0	V
			DM81	1.45	1.75	1.95	1.45	1.75	1.95	
V_{T-}	Negative Going Threshold Voltage	V_{CC} = 5V, Bus Inputs	DM71	0.90	1.10	1.35	0.90	1.10	1.35	V
			DM81	0.95	1.10	1.30	0.95	1.10	1.30	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, T_A = 25°C				−1.5			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V	V_{OH} = 5.5V						250	μA
						−400				
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4					5.5	V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V	TTL Input			1			1	mA
			Strobe			2			2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	TTL Input			40			40	μA
			Strobe			80			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	TTL Input			−1.6			−1.6	mA
			Strobe			−2.4			−2.4	
I_{IN}	Bus Input Current	V_I = 4V	V_{CC} = Max		15	50		15	50	μA
			V_{CC} = 0		1	50		1	50	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−18		−55		N/A		mA
I_{CC}	Supply Current	V_{CC} = Max			50	74		50	74	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM71/81 31 MIN	31 TYP	31 MAX	36 MIN	36 TYP	36 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	TTL Input	Output	C_L = 15 pF, R_L = 400Ω		20	30		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	TTL Input	Output			20	30		20	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Bus Input	Output			30	45		30	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Bus Input	Output			30	45		30	45	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe Input	Output			20	30		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe Input	Output			20	30		20	30	ns

TRI-STATE Octal Buffers

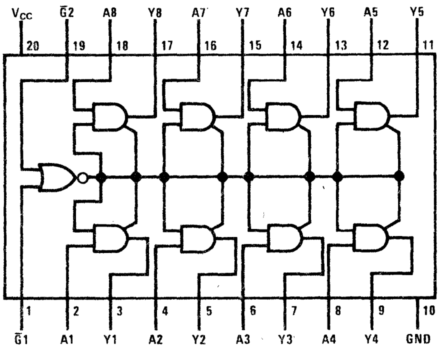
General Description

These devices provide eight, two-input buffers in each package. All employ the newest low power-Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 95 and 97 present true data at the outputs, while the 96 and 98 are inverting. On the 95 and 96 versions, all eight TRI-STATE enable lines are common, with access through a 2-input NOR gate. On the 97 and 98 versions, four buffers are enabled from one common line, and the other four buffers are enabled from another common line. In all cases the outputs are placed in the TRI-STATE condition by applying a high logic level to the enable pins. These devices represent octal, low power-Schottky versions of the very popular DM70/8095, 96, 97, and 98 TRI-STATE hex buffers.

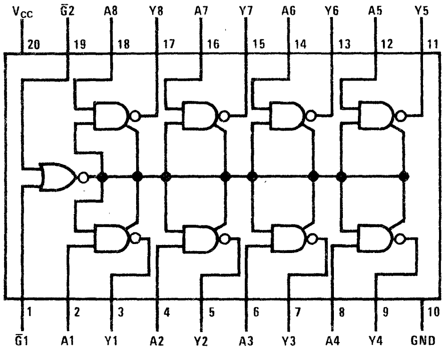
Features

- Octal versions of popular DM8095, 8096, 8097, 8098
- Typical power dissipation
  - LS95, LS97 80 mW
  - LS96, LS98 65 mW
- Typical propagation delay
  - LS95, LS97 13 ns
  - LS96, LS98 10 ns
- Low power-Schottky, TRI-STATE technology

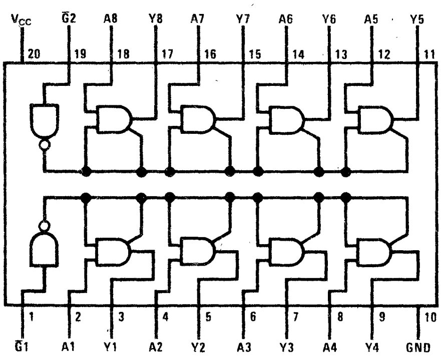
Connection Diagrams



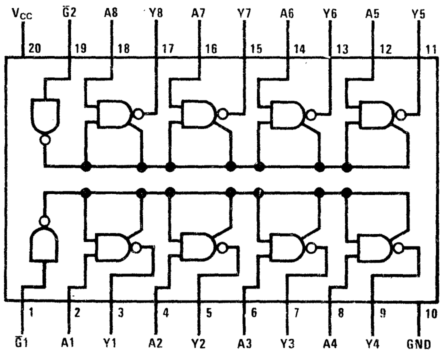
71LS95/81LS95(N)



71LS96/81LS96(N)



71LS97/81LS97(N)



71LS98/81LS98(N)

Truth Tables

LS95

INPUTS			OUTPUT
$\bar{G}1$	$\bar{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

LS96

INPUTS			OUTPUT
$\bar{G}1$	$\bar{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

LS97

INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Z
L	H	H
L	L	L

LS98

INPUTS		OUTPUT
$\bar{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM71LS LS95, LS96, LS97, LS98			DM81LS LS95, LS96, LS97, LS98			UNITS
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High Level Output Current				−1.0			−2.6	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V; I_{OH} = Max	2.5			2.7			V
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V; I_{OH} = −5 mA		N/A		2.4			V
I_{OL}	Low Level Output Current				8			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.4			0.5	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V; V_O = 0.4V			−20			−20	µA
		V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V; V_O = 2.4V			20			20	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20			20	µA
I_{IL}	Low Level Input Current, A Input	V_{CC} = Max, Both $\overline{G}$ Inputs at 2V, V_I = 0.5V			−20			−20	µA
	Low Level Input Current, A Input	V_{CC} = Max, Both $\overline{G}$ Inputs at 0.4V, V_I = 0.4V			−0.36			−0.36	mA
	Low Level Input Current, $\overline{G}$ Input	V_{CC} = Max, V_I = 0.4V			−0.36			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−30	−60	−130	−30	−60	−130	mA
I_{CC}	Supply Current	V_{CC} = Max; 95, 97		16	26		16	26	mA
		V_{CC} = Max; 96, 98		13	21		13	21	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	DM71LS/81LS LS95, LS97			LS96, LS98			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 2 kΩ		11	16		6	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 2 kΩ		15	22		13	17	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, R_L = 2 kΩ		16	25		17	27	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, R_L = 2 kΩ		13	20		16	25	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 2 kΩ		13	20		13	20	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5 pF, R_L = 2 kΩ		19	27		18	27	ns

4-Bit Magnitude Comparators

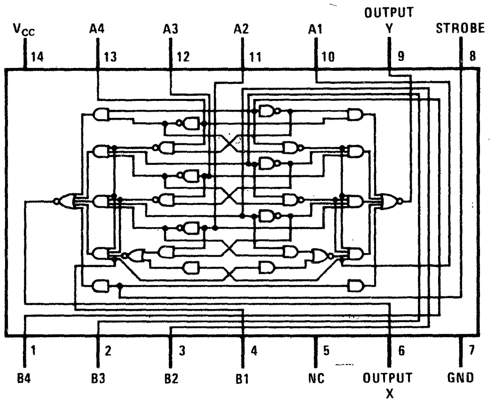
General Description

These devices compare two binary words of four bits in length; and the outputs indicate 1) word A > word B, 2) word A < word B, or 3) word A = word B. A strobe input overrides all other inputs, and when taken to a high logic level, places both outputs in the low state. Comparison of words longer than four bits each may be accomplished through the use of additional DM7200/DM8200 devices.

Features

- Typical power dissipation 175 mW
- Typical propagation delay 20 ns

Connection Diagram



A4, B4 are most significant bits.

7200/8200(J), (N), (W)

Truth Table

INPUTS		OUTPUTS	
CONDITION	STROBE	X	Y
DON'T CARE	H	L	L
A > B	L	H	L
A < B	L	L	H
A = B	L	H	H

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM72/82 00 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{OH}	High Level Output Current				−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −400μA	2.4			V
I_{OL}	Low Level Output Current				16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max		35	53	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM72/82 00 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 15 pF R_L = 400Ω		24	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output			17	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	Output			15	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	Output			8	18	ns
t_{SETUP}	Setup Time				10	0		ns
t_{HOLD}	Hold Time				0	−10		ns

8-Line Data Selectors/Multiplexers

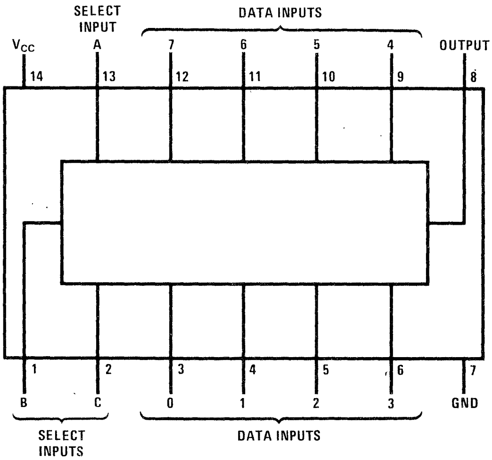
General Description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired one of eight data sources. The DM7211/8211 have a strobe input, which must be at a low logic level to enable these devices. A high logic level on the strobe latches the output in a high logic state, regardless of the conditions on the other inputs. Depending upon the 3-bit binary number applied to the select lines, the non-inverted data present on the selected input is passed to the output. The circuit can also be used to convert parallel input data to serial output data. If 8 bits of parallel information are applied to the inputs, and if the binary numbers 000 through 111 are sequenced on the select lines, the output will provide a serial presentation of the input bits.

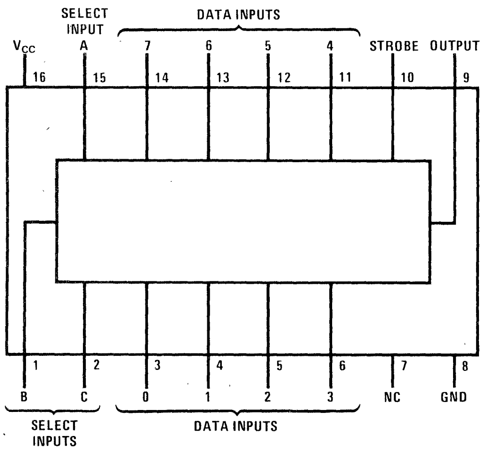
Features

- Full on-chip decoding
- Series 54/74 compatible
- Converts parallel data to serial data
- One volt typical noise immunity
- Typical propagation delay 22 ns
- Typical power dissipation 100 mW

Connection Diagrams



7210(J), (W); 8210(J), (N), (W)



7211(J), (W); 8211(J), (N), (W)

Truth Table

SELECT INPUTS C	B	A	STROBE (DM7211/DM8211 ONLY)	DATA INPUTS 0	1	2	3	4	5	6	7	OUTPUT
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
L	L	H	L	X	L	X	X	X	X	X	X	L
L	L	H	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
L	H	H	L	X	X	X	L	X	X	X	X	L
L	H	H	L	X	X	X	H	X	X	X	X	H
H	L	L	L	X	X	X	X	L	X	X	X	L
H	L	L	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
H	H	L	L	X	X	X	X	X	X	L	X	L
H	H	L	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	H

H = High Level
L = Low Level
X = Don't Care

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM72/82						UNITS
			10			11			
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA T_A = 25°C			−1.5			−1.5	V
I_{OH}	High Level Output Current				−400			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V I_{OH} = −400μA	2.4			2.4			V
I_{OL}	Low Level Output Current				16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V I_{OL} = 16 mA			0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−18		−55	−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max(3)		20	33		20	33	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) I_{CC} is measured with all inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS	DM72/82						UNITS
					10			11			
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 15 pF, R_L = 400Ω		23	32		23	32	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output			21	30		21	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	Output			N/A			21	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	Output			N/A			19	27	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Output			31	43		31	43	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Output			31	42		31	42	ns

Logic Diagrams

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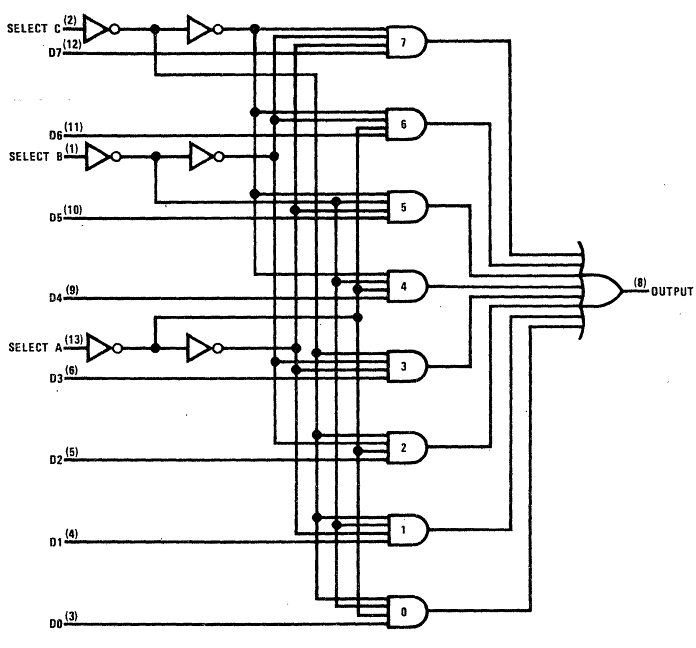

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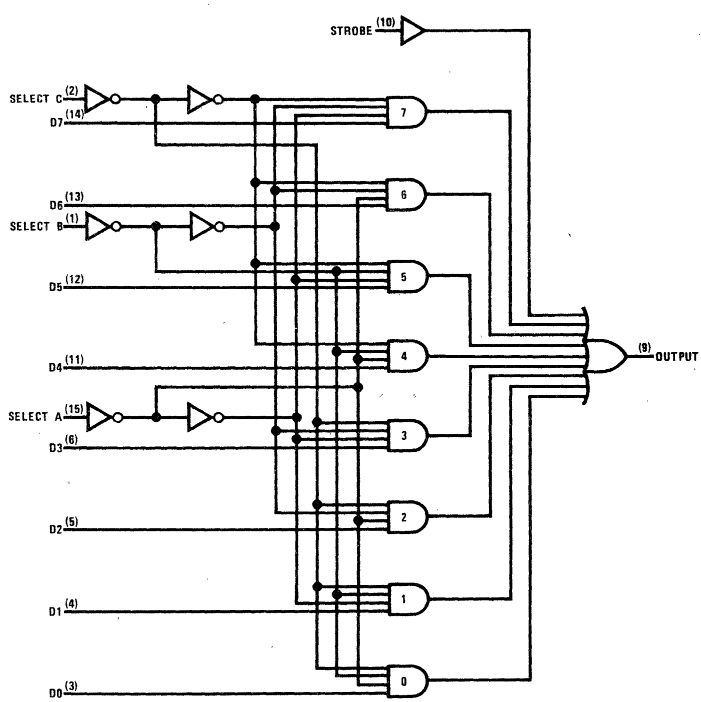


TRI-STATE Data Selectors/Multiplexers

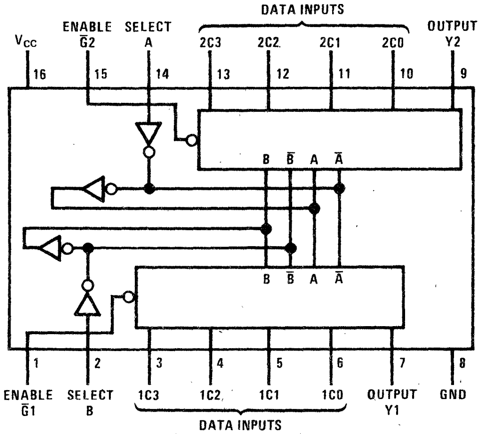
General Description

These devices are the TRI-STATE versions of the very popular DM54153 (DM7214) and DM54150 (DM7219) data selectors/multiplexers. They contain full on-chip decoding to select the desired data input. The DM7214/8214 is a dual, four-line multiplexer, while the DM7219/8219 selects one of sixteen input data lines, depending upon the binary number applied to the select inputs. The DM7214/8214 has common select lines, which therefore select the same input line of both multiplexers. However, the two outputs can be individually controlled by means of the separate enable lines; which, when taken to a high logic level, places the output in the high-impedance TRI-STATE condition. The data at the output of the DM7214/8214 is true, whereas the DM7219/8219 is inverted.

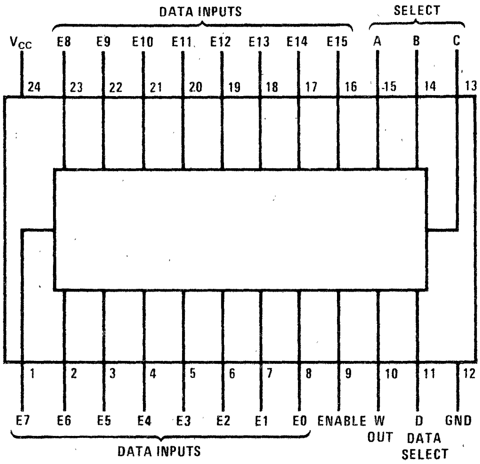
Features

- TRI-STATE pin equivalents to popular 54/74 TTL devices
  - DM7214/8214 – 54153/74153
  - DM7219/8219 – 54150/74150
- Typical propagation delay
  - DM7214/8214 13.5 ns
  - DM7219/8219 11 ns
- Typical power dissipation
  - DM7214/8214 170 mW
  - DM7219/8219 225 mW
- Strobe/enable override

Connection Diagrams



7214(J), (W); 8214(J), (N), (W)



7219(J), (F); 8219(J), (N), (F)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM72/82 14 MIN	14 TYP(1)	14 MAX	19 MIN	19 TYP(1)	19 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current		DM72			−2.0			−2.0	mA
			DM82			−5.2			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max V_{IH} = 2V V_{IL} = 0.8V	V_O = 0.4V			−40			−40	μA
			V_O = 2.4V			40			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−18		−55	−28		−100	mA
I_{CC}	Supply Current	V_{CC} = Max(3)	DM72		34	56		45	68	mA
			DM82		34	65		45	68	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for the DM7219/DM8219 duration of short circuit should not exceed one second.

(3) I_{CC} is measured with all inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM72/82 14 MIN	14 TYP	14 MAX	19 MIN	19 TYP	19 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 50 pF, R_L = 400Ω		15	23		13	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output	C_L = 50 pF, R_L = 400Ω		12	18		9	14	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Output	C_L = 50 pF, R_L = 400Ω		20	34		21	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Output	C_L = 50 pF, R_L = 400Ω		20	34		22	33	ns
t_{ZH}	Output Enable Time to High Level			C_L = 50 pF, R_L = 400Ω		12	18		15	23	ns
t_{ZL}	Output Enable Time to Low Level			C_L = 50 pF, R_L = 400Ω		14	21		17	27	ns
t_{HZ}	Output Disable Time from High Level			C_L = 5 pF, R_L = 400Ω		5	10		5	10	ns
t_{LZ}	Output Disable Time from Low Level			C_L = 5 pF, R_L = 400Ω		15	23		21	30	ns

Truth Tables

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SELECT INPUTS		DATA INPUTS				ENABLE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Hi-Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

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SELECT				ENABLE	DATA INPUTS																OUTPUT
D	C	B	A	$\overline{G}$	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	Y
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Hi-Z
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L

Logic Diagrams

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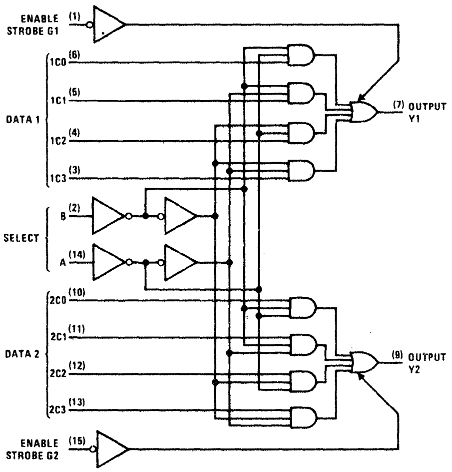

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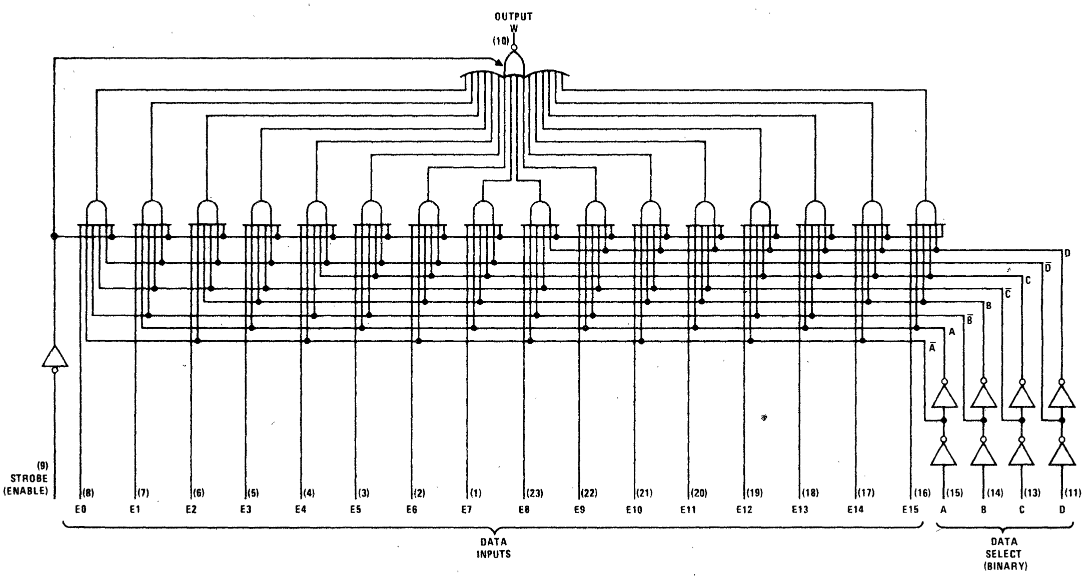


9-Bit Parity Generators/Checkers

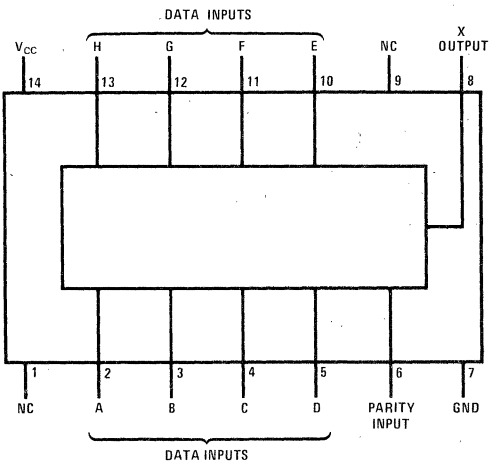
General Description

These circuits can be used both to check for parity and to generate a parity bit. When the generation of a parity bit is desired, the eight data inputs are connected to the transmission lines. If a low logic level is then connected to the parity input, the circuit will generate odd parity. The succeeding parity checker will acknowledge an odd number of "1's" (odd parity) with a low logic level on its output. If a high logic level is connected to the parity input of the first parity generator, the parity checker will acknowledge even parity with a high logic level on its output, although the output of the parity generator will be low.

Features

- Typical propagation delay 34 ns
- Typical power dissipation 130 mW

Connection Diagram



7220/8220(J), (N), (W)

Truth Table

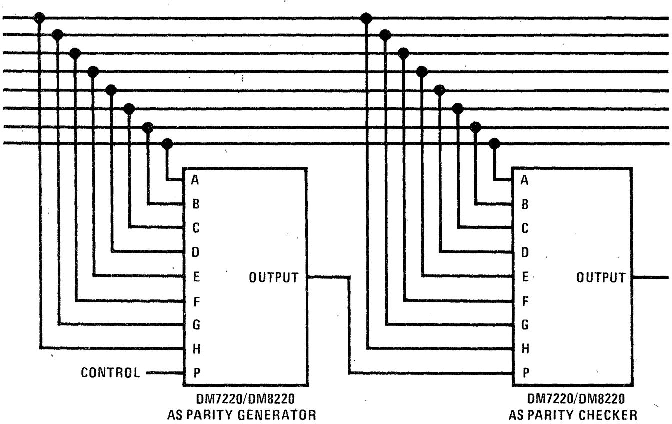
PARITY INPUT	OUTPUT*	INPUTS A THRU H
H	L	Even number of inputs are High
L	L	Odd number of inputs are High

*Single device

Typical Application

If the control line is a logical "0" the parity generator will generate odd parity. The parity checker will acknowledge the presence of an odd number of "1's" (odd parity) with a logical "0" on its output.

If the control line is a logical "1" the parity generator will generate even parity. The parity checker will acknowledge the presence of an even number of "1's" (even parity) with a logical "1" on its output.



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM72 20 MIN	DM72 20 TYP(1)	DM72 20 MAX	DM82 20 MIN	DM82 20 TYP(1)	DM82 20 MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA T_A = 25°C			−1.5			−1.5	V
I_{OH}	High Level Output Current				−400			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −400μA	2.4			2.4			V
I_{OL}	Low Level Output Current				16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−20		−55	−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max		26	35		26	35	mA

Notes

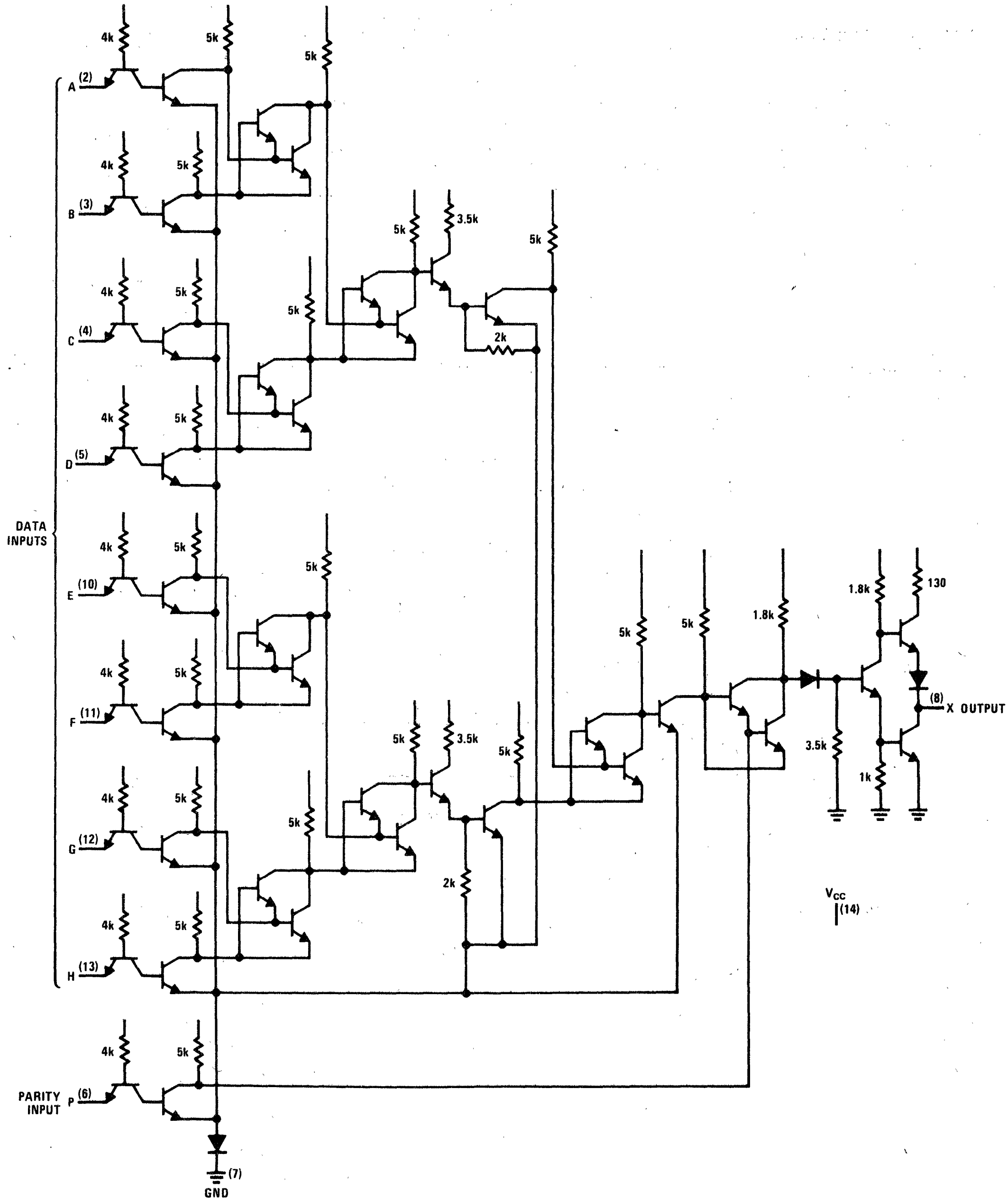
(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS	DM72/DM82 20 MIN	DM72/DM82 20 TYP	DM72/DM82 20 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data Inputs	Output	C_L = 15 pF, R_L = 400Ω		36	58	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data Inputs	Output			32	52	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Parity Input	Output			21	35	ns
t_{PHL}	Propagation Delay Time, High-to Low Level Output	Parity Input	Output			14	25	ns

Schematic Diagram



1-Line to 8-Line Demultiplexers

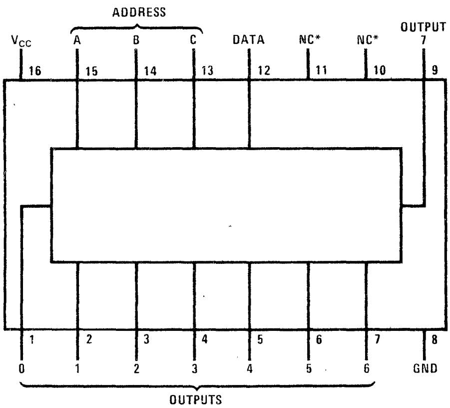
General Description

These circuits demultiplex a data train, and route the data to one of eight outputs. The binary code which is applied to three address lines determines which unique output receives the data. When the data input is at a logical "0," only the addressed output will be a logical "0." When the data input is at a logical "1," all outputs, and therefore the addressed output, will be at a logical "1."

Features

- Typical power dissipation 140 mW
- Typical propagation delay 25 ns

Connection Diagram



*Do not make connection to pins 10 or 11.

7223(J); 8223(J), (N)

Truth Table

DATA INPUT	ADDRESS INPUTS			OUTPUTS							
	C	B	A	0	1	2	3	4	5	6	7
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	H	H	H	H	H	H	H	H

X = Don't Care

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM72 23 MIN	DM72 23 TYP(1)	DM72 23 MAX	DM82 23 MIN	DM82 23 TYP(1)	DM82 23 MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High Level Output Current				−400			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −400μA	2.4			2.4			V
I_{OL}	Low Level Output Current				16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−20		−55	−18		−57	mA
I_{CC}	Supply Current	V_{CC} = Max		28	41		28	41	mA

Notes
(1) All typical values are at V_{CC} = 5V, T_A = 25°C.
(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	DM72/82 23 MIN	DM72/82 23 TYP	DM72/82 23 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 400Ω		26	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			24	35	ns

TRI-STATE Dual 2/4 Demultiplexers

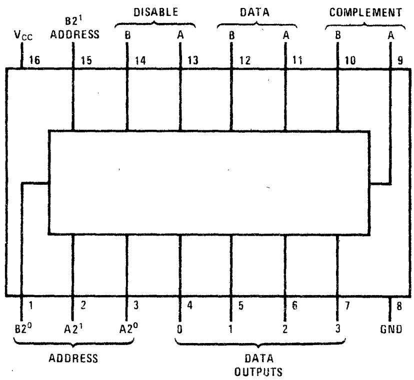
General Description

These circuits route both a data input, as well as its complement, to two of four output lines, depending upon the binary code applied to the address lines. There are two separate data lines, separate address lines for each, as well as the complement of each data line. Which set of address lines is active depends upon which disable line has a low logic level applied. The disable inputs have the additional feature that when both have a high logic level applied, the outputs go to the third (high-impedance) state.

Features

- Separate input disables
- Data complement capability
- Typical propagation delay 20 ns
- Low output impedance — high drive capability

Connection Diagram



7230(J), (W); 8230(J), (N), (W)

Truth Table

DATA A	COMP A	DATA B	COMP B	ADDRESS A 2^1	ADDRESS A 2^0	ADDRESS B 2^1	ADDRESS B 2^0	DIS A	DIS B	OUT 0	OUT 1	OUT 2	OUT 3
L	L	X	X	L	L	X	X	L	H	L	H	H	H
L	H	X	X	L	L	X	X	L	H	H	H	H	H
H	L	X	X	L	L	X	X	L	H	H	H	H	H
H	H	X	X	L	L	X	X	L	H	L	H	H	H
L	L	X	X	L	H	X	X	L	H	H	L	H	H
L	H	X	X	L	H	X	X	L	H	H	H	H	H
H	L	X	X	L	H	X	X	L	H	H	H	H	H
H	H	X	X	L	H	X	X	L	H	H	L	H	H
L	L	X	X	H	L	X	X	L	H	H	H	L	H
L	H	X	X	H	L	X	X	L	H	H	H	H	H
H	L	X	X	H	L	X	X	L	H	H	H	H	H
H	H	X	X	H	L	X	X	L	H	H	H	L	H
L	L	X	X	H	H	X	X	L	H	H	H	H	L
L	H	X	X	H	H	X	X	L	H	H	H	H	H
H	L	X	X	H	H	X	X	L	H	H	H	H	H
H	H	X	X	H	H	X	X	L	H	H	H	H	L
X	X	L	L	X	X	L	L	H	L	L	H	H	H
X	X	L	H	X	X	L	L	H	L	H	H	H	H
X	X	H	L	X	X	L	L	H	L	H	H	H	H
X	X	H	H	X	X	L	L	H	L	L	H	H	H
X	X	L	L	X	X	L	H	H	L	H	L	H	H
X	X	L	H	X	X	L	H	H	L	H	H	H	H
X	X	H	L	X	X	L	H	H	L	H	H	H	H
X	X	H	H	X	X	L	H	H	L	H	L	H	H
X	X	L	L	X	X	H	L	H	L	H	H	L	H
X	X	L	H	X	X	H	L	H	L	H	H	H	H
X	X	H	L	X	X	H	L	H	L	H	H	H	H
X	X	H	H	X	X	H	L	H	L	H	H	L	H
X	X	L	L	X	X	H	H	H	L	H	H	H	L
X	X	L	H	X	X	H	H	H	L	H	H	H	H
X	X	H	L	X	X	H	H	H	L	H	H	H	H
X	X	H	H	X	X	H	H	H	L	H	H	H	L
X	X	X	X	X	X	X	X	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM72 30 MIN	DM72 30 TYP(1)	DM72 30 MAX	DM82 30 MIN	DM82 30 TYP(1)	DM82 30 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, T_A = 25°C				−1.5			−1.5	V
I_{OH}	High Level Output Current					−2.0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4	3.5		2.4	3.5		V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 0.4V			−40			−40	μA
			V_O = 2.4V			40			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Disable			80			80	μA
			Other			40			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Disable		−2.0	−3.2		−2.0	−3.2	mA
			Other		−1.0	−1.6		−1.0	−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−70	−28		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			48	75		48	75	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

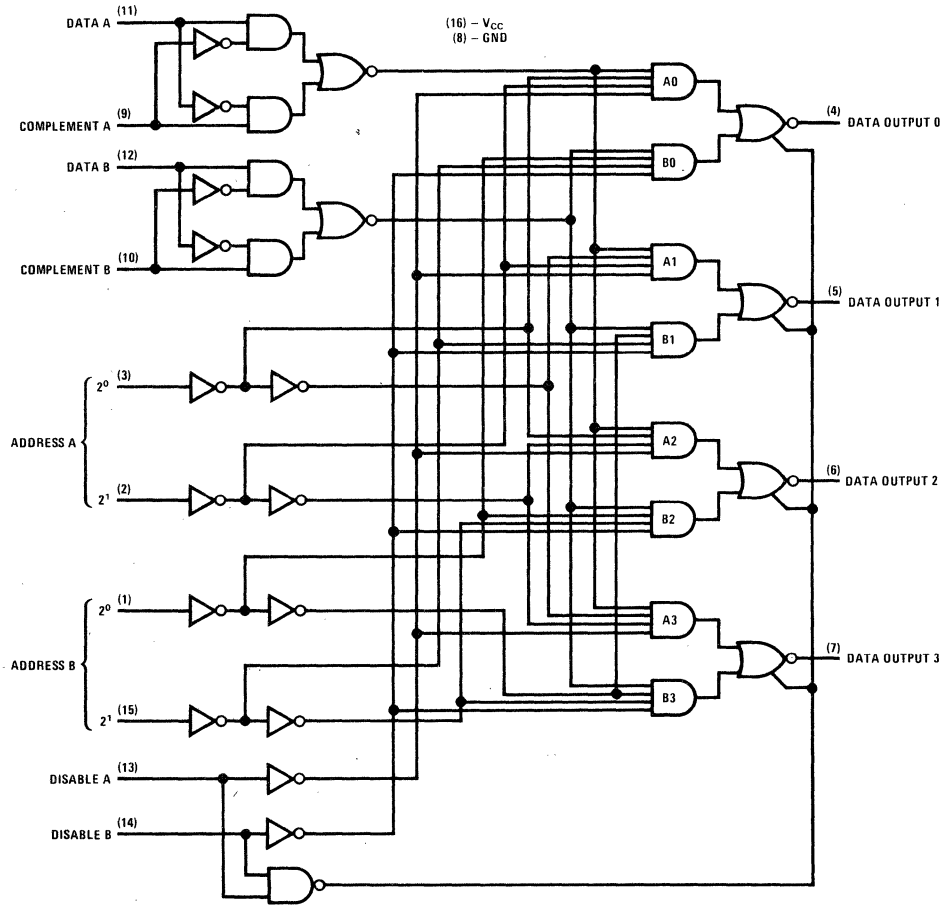
	PARAMETER	FROM	TO	CONDITIONS		DM72/82 30 MIN	DM72/82 30 TYP	DM72/82 30 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	Inverting	C_L = 50 pF, R_L = 400Ω		20	36	ns
				Non-Inverting			13	24	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output	Inverting			18	26	ns
				Non-Inverting			18	26	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address(3)	Output				20	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address(3)	Output				20	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Disable(4)	Output				13	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Disable(4)	Output				16	25	ns
t_{ZH}	Output Enable Time to High Level						15	23	ns
t_{ZL}	Output Enable Time to Low Level						18	27	ns
t_{HZ}	Output Disable Time from High Level				C_L = 5 pF, R_L = 400Ω		7	14	ns
t_{LZ}	Output Disable Time from Low Level						15	27	ns

Notes

(3) The only conditions under which a t_{PHL} from the Address inputs can be observed is when an output goes from being nonselected to being selected and the information being routed to that output is a logical "0." If the information had been a logical "1," no change would have occurred and no measurement could have been made. Similarly, the only time a t_{PLH} from the Address inputs can be observed, is when an output goes from being selected to being nonselected and the information that had been routed to that output was a logical "0." If the information had been a logical "1," no change would have occurred and no measurement could have been made.

(4) Information in Note 3 concerning t_{PLH} and t_{PLH} from the address inputs are applicable here also.

Logic Diagram



Dual/Quad Gated Flip-Flops

General Description

The DM7511/8511 or the low-power versions DM75L11/85L11, are dual, gated, D-type flip-flops. Each flip-flop has its own clock, clear line, and two gated inputs. Both gate inputs must be low to enable data transfer to the output.

The DM7512/8512, and DM75L12/85L12 are dual, gated flip-flops which can operate in either a J-K mode, or as D-type flip-flops. They have a common clock and common, asynchronous clear, but have separate mode inputs such that one side can operate as J-K while the other side operates as a D-type flip-flop.

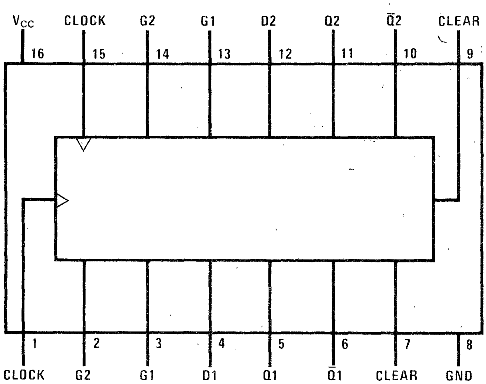
The DM7613/8613, and DM76L13/86L13 are quad, gated, D-type flip-flops with common clock, common clear, and gated input. When a high logic level is applied to the gated input, data entry to the flip-flop is inhibited.

Features

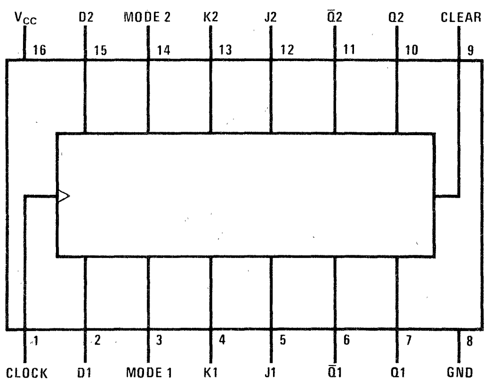
- Positive-edge triggered
- Do-nothing state
- Buffered inputs

TYPE	TYPICAL TOGGLE RATE	TYPICAL POWER DISSIPATION
DM7511/8511	45 MHz	210 mW
DM75L11/85L11	9 MHz	17.5 mW
DM7512/8512	28 MHz	220 mW
DM75L12/85L12	10 MHz	16.0 mW
DM7613/8613	30 MHz	290 mW
DM76L13/86L13	7 MHz	28.5 mW

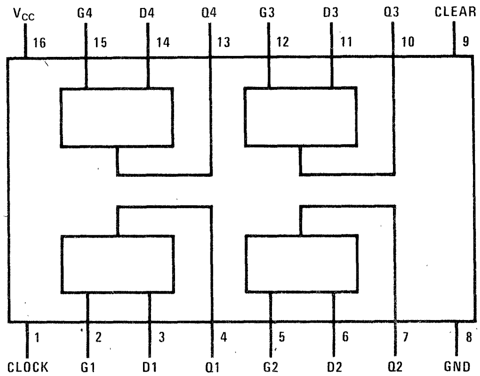
Connection Diagrams



7511/8511(J), (N), (W); 75L11/85L11(J), (N), (W)



7512/8512(J), (N), (W); 75L12/85L12(J), (N), (W)



7613/8613(J), (N), (W); 76L13/86L13(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM75/85 11, 12			DM76/86 13			DM75L/85L11, 12 DM76L/86L13			UNITS
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5			N/A	V
I_{OH}	High Level Output Current					−800			−800			−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OH} = Max		2.4			2.4			2.4			V
I_{OL}	Low Level Output Current		Military			16			16			2.0	mA
			Commercial			16			16			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OL} = Max	Military			0.4			0.4			0.3	V
			Commercial			0.4			0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0			1.0			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			40			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V									−0.18	mA
			V_I = 0.4V			−1.6			−1.6				mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−18		−55	−18		−55	−3	−9	−15	mA
I_{CC}	Supply Current	V_{CC} = Max(3)	11, L11		42	55					3.5	4.9	mA
			12, L12		44	57					3.2	4.5	mA
			13, L13					58	76		5.7	7.9	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) Supply current is measured with clear/clock at 3V, all other inputs at 0V.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER			FROM	TO	CONDITIONS	DM75/85 11, L11 MIN	DM75/85 11, L11 TYP	DM75/85 11, L11 MAX	DM75/85 12, L12 MIN	DM75/85 12, L12 TYP	DM75/85 12, L12 MAX	DM76/86 13, L13 MIN	DM76/86 13, L13 TYP	DM76/86 13, L13 MAX	UNITS
f_{MAX}	Maximum Clock Frequency				$C_L = 15\ pF$, $R_L = 400\Omega$ (Standard); $C_L = 50\ pF$, $R_L = 4\ k\Omega$ (Low Power)	30	45		20	28		20	30		MHz
						6	9		6	10		5	7		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Q			14	20		21	35		17	24	ns
							55	95		35	70		41	60	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Q			19	30		26	40		22	33	ns
							75	125		60	120		70	100	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clear	$\overline{Q}$			14	20		22	35		N/A		ns
							55	95		32	65		N/A		
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear	Q			19	30		26	40		21	31	ns
							75	125		57	114		68	100	
$t_{W(CLOCK)}$	Width of Clock Pulse					20	11		25	15		24	16		ns
						100	30		100	30		100	50		
$t_{W(CLEAR)}$	Width of Clear Pulse					20	10		25	13		27	18		ns
						100	30		100	30		100	50		
t_{SETUP}	Setup Time	J, D Inputs				15	9		15	9		24	16		ns
						80	40		110	55		100	55		
		Mode Inputs					N/A		30	20			N/A		ns
							N/A		150	85			N/A		
		K Inputs					N/A		20	13			N/A		ns
							N/A		150	80			N/A		
		G1 or G2 Inputs				30	21			N/A		30	21		ns
						120	60			N/A		150	85		
t_{HOLD}	Hold Time	All				0			0			0			ns
						0			0			0			

Truth Tables

11, L11

D	G1	G2	CLR	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	L	L	L	H
H	L	L	L	H	L
X	H	X	L	Q_n	$\overline{Q}_n$
X	X	H	L	Q_n	$\overline{Q}_n$
X	X	X	H	L	H*

12, L12

J	K	M	CLEAR	Q_{n+1}
L	L	H	L	Q_n
H	L	H	L	H
L	H	H	L	L
H	H	H	L	$\overline{Q}_n$
X	X	L	L	D
X	X	X	H	L*

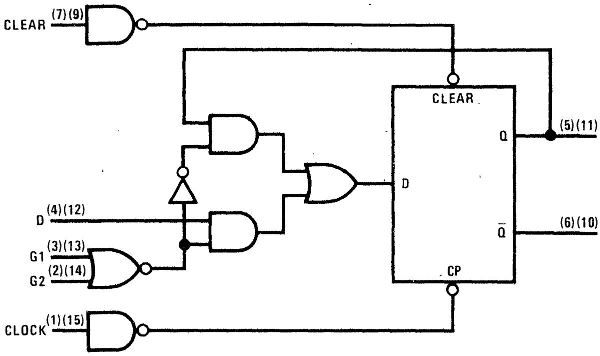
13, L13

D	G	CLR	Q_{n+1}
H	L	L	H
L	L	L	L
X	H	L	Q_n
X	X	H	L*

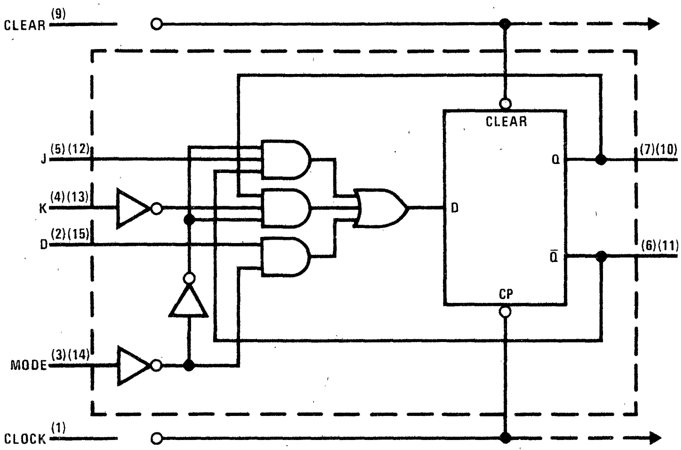
*Asynchronous Transition
X = Don't Care

Logic Diagrams

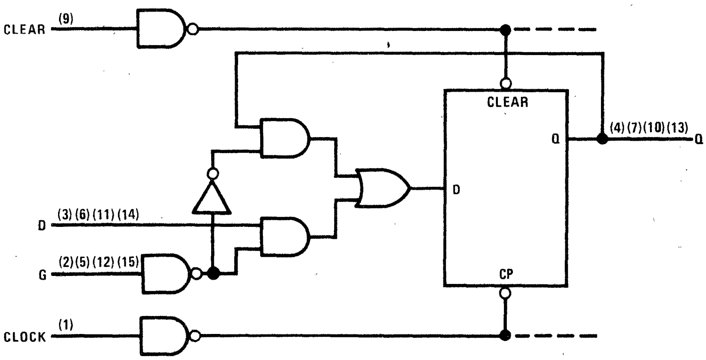
11, L11



12, L12



13, L13



Proprietary

DM75/DM8520

Modulo-N Dividers

General Description

Although extremely versatile in a number of applications, the primary uses of these circuits are in two areas:

1. MODULO-N DIVIDER
   A single DM7520/DM8520 can be programmed without external components to divide by any number from 2 to 15. Cascading of these dividers will provide division by any number from 2 to very large numbers.

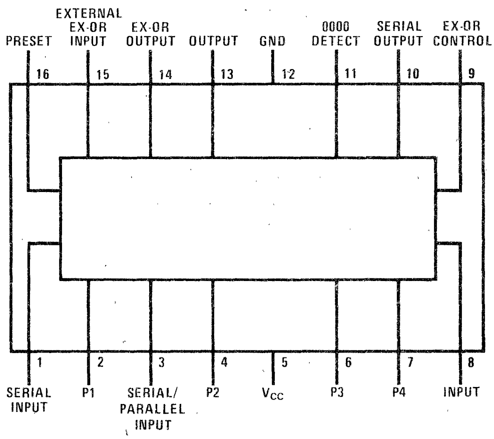
2. SHIFT REGISTER
   Since the basic organization of the logic is that of a serial shift register, the device may be used where four-bit parallel-in-serial-out shifting is required.

(continued)

Features

- Fully programmable divider—any number from 2 to ∞
- Also functions as a four-bit parallel shift register
- Typical propagation delay 36 ns
- Typical power dissipation 250 mW

Connection Diagram



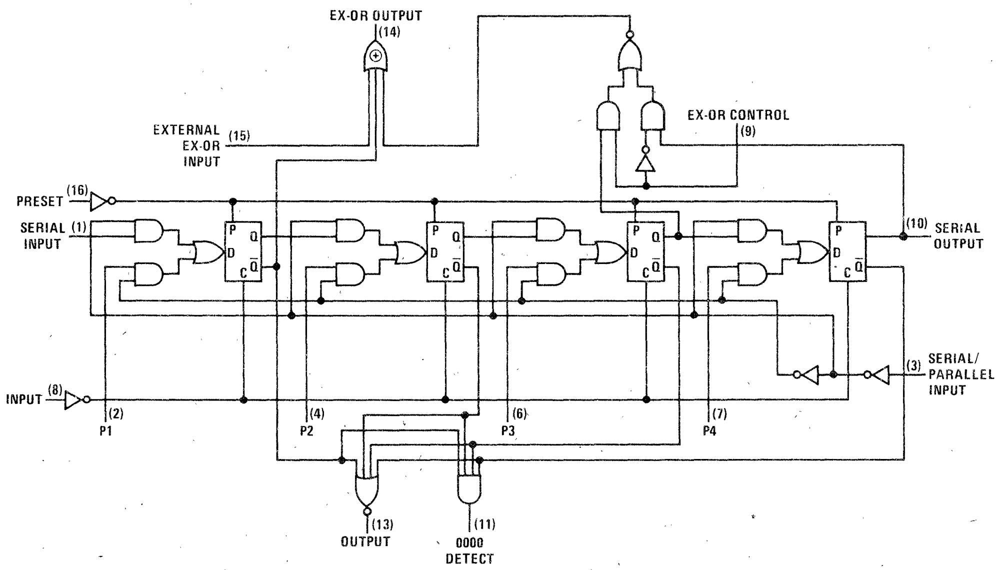
7520(J), (W); 8520(J), (N), (W)

Truth Table

TABLE FOR DIVISION BY N

SETTING				÷BY
P1	P2	P3	P4	
H	H	H	L	2
H	H	L	L	3
H	L	L	L	4
L	L	L	H	5
L	L	H	L	6
L	H	L	L	7
H	L	L	H	8
L	L	H	H	9
L	H	H	L	10
H	H	L	H	11
H	L	H	L	12
L	H	L	H	13
H	L	H	H	14
L	H	H	H	15

Logic Diagram



General Description (Continued)

THEORY OF OPERATION

The basic operation of the DM7520/DM8520 is derived from the fact that when several outputs of a shift register are EXCLUSIVE OR'ed and the result fed back to the register's input, a unique progression of stable states results on the outputs of the flip-flops. Depending upon which outputs are EXCLUSIVE OR'ed, the number of different states can be varied. Even if optimum gating is provided the most states which can be obtained is $2^n - 1$, where n is equal to the number of flip-flops in the register. The all-zero state is precluded; and, therefore, the maximum number of states is always one less than the theoretical maximum number. Since the DM7520/DM8520 contains four flip-flops, its maximum number of states is 15. Because the 1111 state occurs only once during a 15-state sequence this state is detected, and its output becomes the output of the divider.

To obtain frequency division by numbers other than the maximum, it is necessary to cause the register to "jump" immediately from its initial 1111 to the state which it would normally reach in 16–m (m = desired frequency division) pulses. For example, to divide by eleven it would be necessary to jump to the fifth state and then simply allow the register to normally progress forward to its original state. The output of the divider is also used as a control pulse. Since the 1111 state is detected and since the "jump-state" information is of interest only at the time that this state is reached, the OUTPUT is used to gate the parallel inputs, through the SERIAL/PARALLEL input, so that it recognizes this "jump-state" information only at this time. Subsequently as the states change, the parallel input information is locked from the divider.

Should the divider ever be accidentally set in the forbidden 0000 state, an output is provided to detect this state. If this output is in turn fed into the EXTERNAL EX-OR input, a 1 will be forced into the register at the next clock pulse, thus clearing the unallowed state.

A PRESET input is provided which when taken to a logical "1" level overrides all other inputs and sets the register to the 1111 state.

To summarize, the following connections should be made for operation of a single DM7520/DM8520.

Ex-Or Output to Serial Input
0000 Detect to External Ex-Or Input
Output to Serial/Parallel Input
Preset to Ground
Ex-Or Control to Ground

To divide by numbers greater than 15, it is necessary to cascade DM7520/DM8520's. Both the OUTPUT and the 0000 DETECT output are capable of being connected directly to other like outputs, thus providing the "WIRED-OR" configuration. These outputs should be connected to the similar outputs on other dividers for proper operation. All SERIAL/PARALLEL inputs should be connected to the common OUTPUT.

Figure 1 indicates connections for 2 dividers or a maximum frequency division of 255.

To divide by numbers between 16 and 255, the table in *Figure 2* will apply.

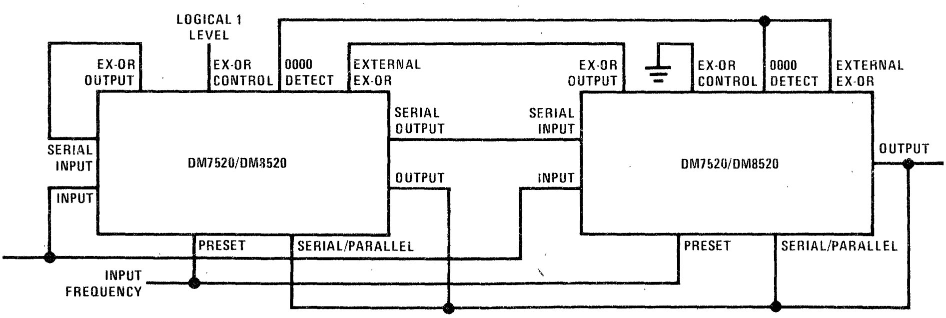


FIGURE 1. CONNECTION FOR 2 DIVIDERS FOR MAXIMUM FREQUENCY DIVISION OF 255

THEORY OF OPERATION (Continued)

SETTING									SETTING									SETTING								
DIVIDER 1				DIVIDER 2				BY	DIVIDER 1				DIVIDER 2				BY	DIVIDER 1				DIVIDER 2				BY
P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4	
L	H	H	H	H	H	H	H	255	H	L	L	L	H	L	L	H	195	L	L	H	H	H	L	L	H	135
H	L	H	H	H	H	H	H	254	H	H	L	L	L	H	L	L	194	H	L	L	H	H	H	L	L	134
L	H	L	H	H	H	H	H	253	H	H	H	L	L	L	H	L	193	L	H	L	L	H	H	H	L	133
L	L	H	L	H	H	H	H	252	L	H	H	H	L	L	L	H	192	H	L	H	L	L	H	H	H	132
H	L	L	H	L	H	H	H	251	L	L	H	H	H	L	L	L	191	H	H	L	H	L	L	H	H	131
L	H	L	L	H	L	H	H	250	L	L	L	H	H	H	L	L	190	L	H	H	L	H	L	L	H	130
L	L	H	L	L	H	L	H	249	H	L	L	L	H	H	H	L	189	H	L	H	H	L	H	L	L	129
L	L	L	H	L	L	H	L	248	L	H	L	L	L	H	H	H	188	L	H	L	H	H	L	H	L	128
L	L	L	L	H	L	L	H	247	H	L	H	L	L	L	H	H	187	H	L	H	L	H	H	L	H	127
L	L	L	L	L	H	L	L	246	H	H	L	H	L	L	L	H	186	L	H	L	H	L	H	H	L	126
L	L	L	L	L	L	H	L	245	L	H	H	L	H	L	L	L	185	L	L	H	L	H	L	H	H	125
L	L	L	L	L	L	L	H	244	L	L	H	H	L	H	L	L	184	H	L	L	H	L	H	L	H	124
H	L	L	L	L	L	L	L	243	H	L	L	H	H	L	H	L	183	L	H	L	L	H	L	H	L	123
H	H	L	L	L	L	L	L	242	L	H	L	L	H	H	L	H	182	H	L	H	L	L	H	L	H	122
H	H	H	L	L	L	L	L	241	L	L	H	L	L	H	H	L	181	H	H	L	H	L	L	H	L	121
L	H	H	H	L	L	L	L	240	H	L	L	H	L	L	H	H	180	H	H	H	L	H	L	L	H	120
H	L	H	H	H	L	L	L	239	L	H	L	L	H	L	L	H	179	L	H	H	H	L	H	L	L	119
H	H	L	H	H	H	L	L	238	L	L	H	L	L	H	L	L	178	H	L	H	H	H	L	H	L	118
L	H	H	L	H	H	H	L	237	H	L	L	H	L	L	H	L	177	H	H	L	H	H	H	L	H	117
L	L	H	H	L	H	H	H	236	H	H	L	L	H	L	L	H	176	H	H	H	L	H	H	H	L	116
L	L	L	H	H	L	H	H	235	H	H	H	L	L	H	L	L	175	H	H	H	H	L	H	H	H	115
L	L	L	L	H	H	L	H	234	L	H	H	H	L	L	H	L	174	H	H	H	H	H	L	H	H	114
L	L	L	L	L	H	H	L	233	H	L	H	H	H	L	L	H	173	L	H	H	H	H	H	L	H	113
L	L	L	L	L	L	H	H	232	L	H	L	H	H	H	L	L	172	H	L	H	H	H	H	H	L	112
H	L	L	L	L	L	L	H	231	H	L	H	L	H	H	H	L	171	H	H	L	H	H	H	H	H	111
L	H	L	L	L	L	L	L	230	H	H	L	H	L	H	H	H	170	H	H	H	L	H	H	H	H	110
L	L	H	L	L	L	L	L	229	L	H	H	L	H	L	H	H	169	L	H	H	H	L	H	H	H	109
H	L	L	H	L	L	L	L	228	H	L	H	H	L	H	L	H	168	L	L	H	H	H	L	H	H	108
H	H	L	L	H	L	L	L	227	H	H	L	H	H	L	H	L	167	H	L	L	H	H	H	L	H	107
L	H	H	L	L	H	L	L	226	L	H	H	L	H	H	L	H	166	H	H	L	L	H	H	H	L	106
H	L	H	H	L	L	H	L	225	H	L	H	H	L	H	H	L	165	L	H	H	L	L	H	H	H	105
L	H	L	H	H	L	L	H	224	L	H	L	H	H	L	H	H	164	L	L	H	H	L	L	H	H	104
L	L	H	L	H	H	L	L	223	L	L	H	L	H	H	L	H	163	L	L	L	H	H	L	L	H	103
L	L	L	H	L	H	H	L	222	H	L	L	H	L	H	H	L	162	L	L	L	L	H	H	L	L	102
L	L	L	L	H	L	H	H	221	H	H	L	L	H	L	H	H	161	H	L	L	L	L	H	H	L	101
L	L	L	L	L	H	L	H	220	H	H	H	L	L	H	L	H	160	H	H	L	L	L	L	H	H	100
H	L	L	L	L	L	H	L	219	H	H	H	H	L	L	H	L	159	L	H	H	L	L	L	L	H	99
H	H	L	L	L	L	L	H	218	L	H	H	H	H	L	L	H	158	L	L	H	H	L	L	L	L	98
L	H	H	L	L	L	L	L	217	H	L	H	H	H	H	L	L	157	H	L	L	H	H	L	L	L	97
H	L	H	H	L	L	L	L	216	H	H	L	H	H	H	H	L	156	L	H	L	L	H	H	L	L	96
L	H	L	H	H	L	L	L	215	L	H	H	L	H	H	H	H	155	H	L	H	L	L	H	H	L	95
H	L	H	L	H	H	L	L	214	H	L	H	H	L	H	H	H	154	L	H	L	H	L	L	H	H	94
H	H	L	H	L	H	H	L	213	H	H	L	H	H	L	H	H	153	H	L	H	L	H	L	L	H	93
H	H	H	L	H	L	H	H	212	H	H	H	L	H	H	L	H	152	L	H	L	H	L	H	L	L	92
L	H	H	H	L	H	L	H	211	L	H	H	H	L	H	H	L	151	L	L	H	L	H	L	H	L	91
L	L	H	H	H	L	H	L	210	H	L	H	H	H	L	H	H	150	L	L	L	H	L	H	L	H	90
L	L	L	H	H	H	L	H	209	L	H	L	H	H	H	L	H	149	H	L	L	L	H	L	H	L	89
L	L	L	L	H	H	H	L	208	L	L	H	L	H	H	H	L	148	L	H	L	L	L	H	L	H	88
H	L	L	L	L	H	H	H	207	L	L	L	H	L	H	H	H	147	H	L	H	L	L	L	H	L	87
L	H	L	L	L	L	H	H	206	H	L	L	L	H	L	H	H	146	L	H	L	H	L	L	L	H	86
H	L	H	L	L	L	L	H	205	H	H	L	L	L	H	L	H	145	H	L	H	L	H	L	L	L	85
H	H	L	H	L	L	L	L	204	L	H	H	L	L	L	H	L	144	H	H	L	H	L	H	L	L	84
H	H	H	L	H	L	L	L	203	H	L	H	H	L	L	L	H	143	H	H	H	L	H	L	H	L	83
H	H	H	H	L	H	L	L	202	H	H	L	H	H	L	L	L	142	H	H	H	H	L	H	L	H	82
L	H	H	H	H	L	H	L	201	L	H	H	L	H	H	L	L	141	H	H	H	H	H	L	H	L	81
L	L	H	H	H	H	L	H	200	L	L	H	H	L	H	H	L	140	H	H	H	H	H	H	L	H	80
H	L	L	H	H	H	H	L	199	H	L	L	H	H	L	H	H	139	L	H	H	H	H	H	H	L	79
L	H	L	L	H	H	H	H	198	H	H	L	L	H	H	L	H	138	L	L	H	H	H	H	H	H	78
L	L	H	L	L	H	H	H	197	H	H	H	L	L	H	H	L	137	H	L	L	H	H	H	H	H	77
L	L	L	H	L	L	H	H	196	L	H	H	H	L	L	H	H	136	H	H	L	L	H	H	H	L	76

FIGURE 2. DM7520/DM8520 SHIFT REGISTER DIVIDER INPUT CODING TABLE (2 PACKAGE COMBINATIONS)

THEORY OF OPERATION (Continued)

SETTING									SETTING									SETTING								
DIVIDER 1				DIVIDER 2				BY	DIVIDER 1				DIVIDER 2				BY	DIVIDER 1				DIVIDER 2				BY
P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4	
H	H	H	L	L	H	H	H	75	L	L	H	H	H	H	L	L	50	L	H	H	L	L	H	H	L	25
H	H	H	H	L	L	H	H	74	L	L	L	H	H	H	H	L	49	H	L	H	H	L	L	H	H	24
H	H	H	H	H	L	L	H	73	H	L	L	L	H	H	H	H	48	H	H	L	H	H	L	L	H	23
L	H	H	H	H	H	L	L	72	H	H	L	L	L	H	H	H	47	H	H	H	L	H	H	L	L	22
L	L	H	H	H	H	H	L	71	L	H	H	L	L	L	H	H	46	H	H	H	H	L	H	H	L	21
L	L	L	H	H	H	H	H	70	L	L	H	H	L	L	L	H	45	L	H	H	H	H	L	H	H	20
L	L	L	L	H	H	H	H	69	L	L	L	H	H	L	L	L	44	H	L	H	H	H	H	L	H	19
L	L	L	L	L	H	H	H	68	H	L	L	L	H	H	L	L	43	L	H	L	H	H	H	H	L	18
H	L	L	L	L	L	H	H	67	L	H	L	L	L	H	H	L	42	H	L	H	L	H	H	H	H	17
L	H	L	L	L	L	L	H	66	L	L	H	L	L	L	H	H	41	L	H	L	H	L	H	H	H	16
H	L	H	L	L	L	L	L	65	L	L	L	H	L	L	L	H	40	H	L	H	L	H	L	H	H	15
L	H	L	H	L	L	L	L	64	H	L	L	L	H	L	L	L	39	L	H	L	H	L	H	L	H	14
L	L	H	L	H	L	L	L	63	L	H	L	L	L	H	L	L	38	H	L	H	L	H	L	H	L	13
L	L	L	H	L	H	L	L	62	L	L	H	L	L	L	H	L	37	H	H	L	H	L	H	L	H	12
L	L	L	L	H	L	H	L	61	H	L	L	H	L	L	L	H	36	L	H	H	L	H	L	H	L	11
H	L	L	L	L	H	L	H	60	L	H	L	L	H	L	L	L	35	L	L	H	H	L	H	L	H	10
L	H	L	L	L	L	H	L	59	H	L	H	L	L	H	L	L	34	L	L	L	H	H	L	H	L	9
L	L	H	L	L	L	L	H	58	L	H	L	H	L	L	H	L	33	H	L	L	L	H	H	L	H	8
L	L	L	H	L	L	L	L	57	L	L	H	L	H	L	L	H	32	H	H	L	L	L	H	H	L	7
L	L	L	L	H	L	L	L	56	H	L	L	H	L	H	L	L	31	H	H	H	L	L	L	H	H	6
H	L	L	L	L	H	L	L	55	H	H	L	L	H	L	H	L	30	H	H	H	H	L	L	L	H	5
H	H	L	L	L	L	H	L	54	L	H	H	L	L	H	L	H	29	H	H	H	H	H	L	L	L	4
H	H	H	L	L	L	L	H	53	L	L	H	H	L	L	H	L	28	H	H	H	H	H	H	L	L	3
H	H	H	H	L	L	L	L	52	H	L	L	H	H	L	L	H	27	H	H	H	H	H	H	H	L	2
L	H	H	H	H	L	L	L	51	H	H	L	L	H	H	L	L	26									

FIGURE 2. DM7520/DM8520 SHIFT REGISTER DIVIDER INPUT CODING TABLE (2 PACKAGE COMBINATIONS) (CONTINUED)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM7520			DM8520			UNITS
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−400			−400	µA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −400µA		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Ex-Or Input			80			80	µA
			Others			40			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Ex-Or Input			−3.2			−3.2	mA
			Others			−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−20		−55	−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max			50	75		50	75	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

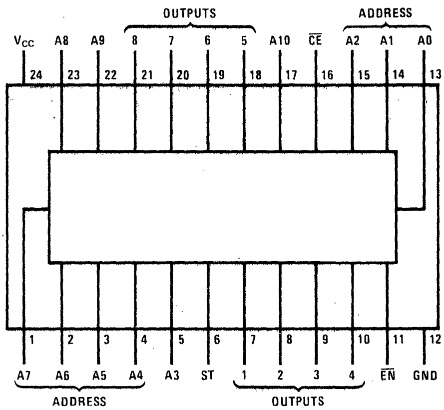
	PARAMETER	CONDITIONS	DM75/85 20 MIN	DM75/85 20 TYP	DM75/85 20 MAX	UNITS
f_{MAX}	Maximum Clock Frequency	$C_L = 15$ pF, $R_L = 400\Omega$	15	20		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			38	55	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output			35	50	ns

TRI-STATE 16K Read Only Memories

General Description

The DM8531 is a 16,384-bit bipolar, mask-programmable ROM organized as 2048, 8-bit words. Eleven address inputs select the desired one-of-2048 words. All eleven address inputs and one of the two enable inputs have a latch feature. The latch function is controlled by the strobe input. The two enable lines are used to either enable or disable the circuit. TRI-STATE outputs allow for expansion to greater numbers of words without sacrifice in speed, as would be the case with open-collector outputs.

Connection Diagram

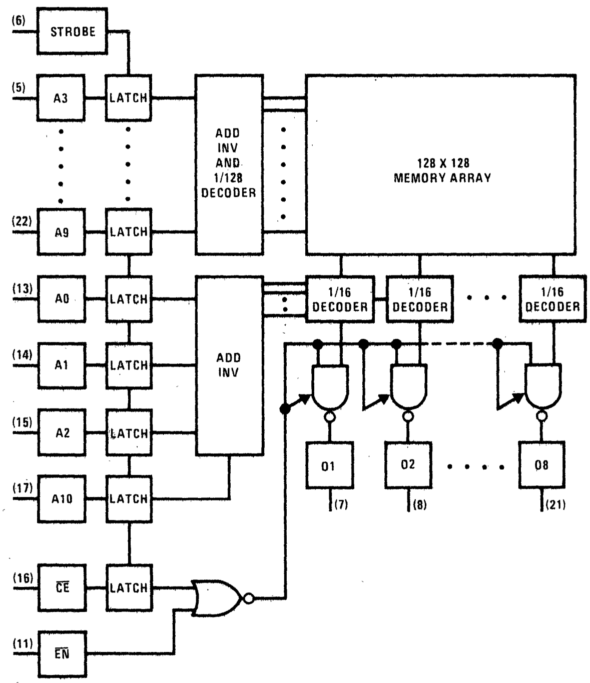


8531(J), (N)

Truth Table

t			t + 1			
$\overline{CE}$	$\overline{EN}$	ST	$\overline{CE}$	$\overline{EN}$	ST	OUTPUTS
X	X	X	L	L	H	Read stored data
X	X	X	H	X	H	Hi-Z
X	X	X	X	H	H	Hi-Z
L	X	H	X	L	L	Read stored data for address inputs at t
H	X	H	X	X	L	Hi-Z
X	X	X	X	H	L	Hi-Z

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM8531 MIN	DM8531 TYP(1)	DM8531 MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −400μA		2.4			V
I_{OL}	Low Level Output Current					6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 6 mA				0.45	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−15		−50	mA
I_{CC}	Supply Current	V_{CC} = Max			115	160	mA

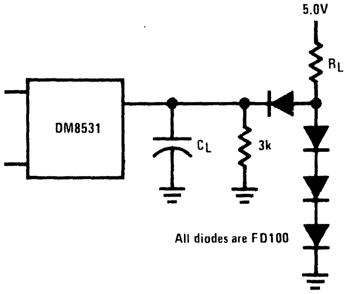
Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.
(2) Not more than one output should be shorted at a time.
(3) Tentative data.

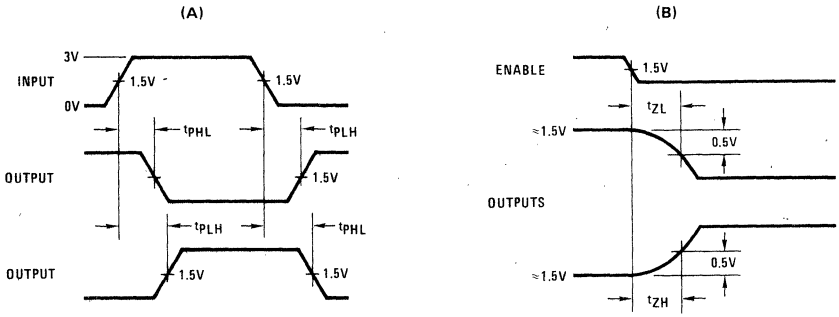
Switching Characteristics V_{CC} = 5V, T_A = 25°C

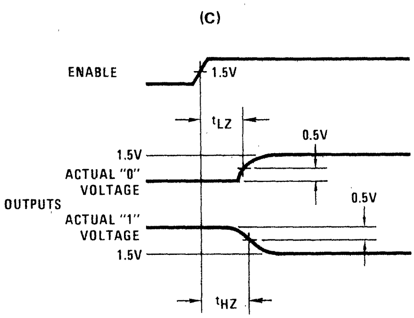
	PARAMETER	FROM	TO	CONDITIONS	DM8531 MIN	DM8531 TYP	DM8531 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address	Output	C_L = 50 pF, R_L = 600Ω		200	450	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address	Output			150	450	ns
t_{ZH}	Output Enable Time to High Level					40	80	ns
t_{ZL}	Output Enable Time to Low Level					70	165	ns
t_S	Address, Chip Enable ($\overline{CE}$) Set-Up Time				30	10		ns
t_H	Address, Chip Enable ($\overline{CE}$) Hold Time				30	10		ns
t_{HZ}	Output Disable Time from High Level			C_L = 5 pF, R_L = 600Ω		20	50	ns
t_{LZ}	Output Disable Time from Low Level					40	60	ns
t_W	Minimum Strobe Pulse Width				40	20		ns
t_{ST}	Strobe Access Time					250	450	ns

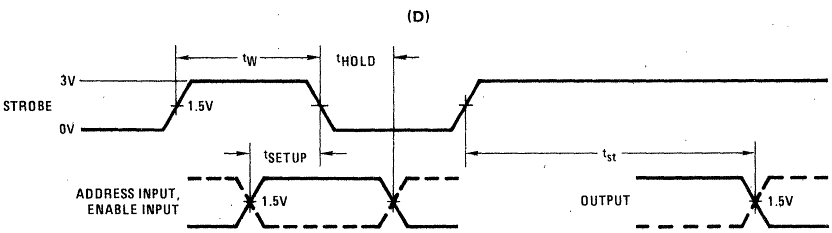
AC Test Circuit



Switching Time Waveforms







f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
Duty Cycle = 50%

TRI-STATE Quad I/O Registers

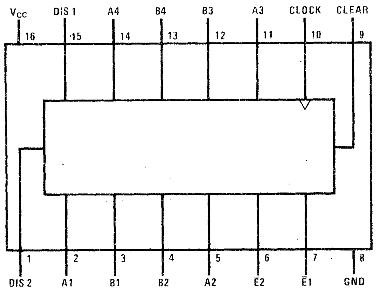
General Description

These circuits are four-bit storage registers having two terminals per bit, which may be used as either inputs or outputs while tied to their individual bus lines. Storage capability is also provided by means of positive-edge triggered flip-flops having a common clock and asynchronous clear. Each I/O terminal can be forced into the high-impedance state by applying a high logic level to its disable control. The four A outputs are tied together on one disable control, while the four B outputs are tied together on a separate disable control.

Features

- TRI-STATE outputs
- Typical clock frequency 40 MHz
- Typical propagation delay 24 ns
- Typical power dissipation 400 mW

Connection Diagram



7542(J), (W); 8542(J), (N), (W)

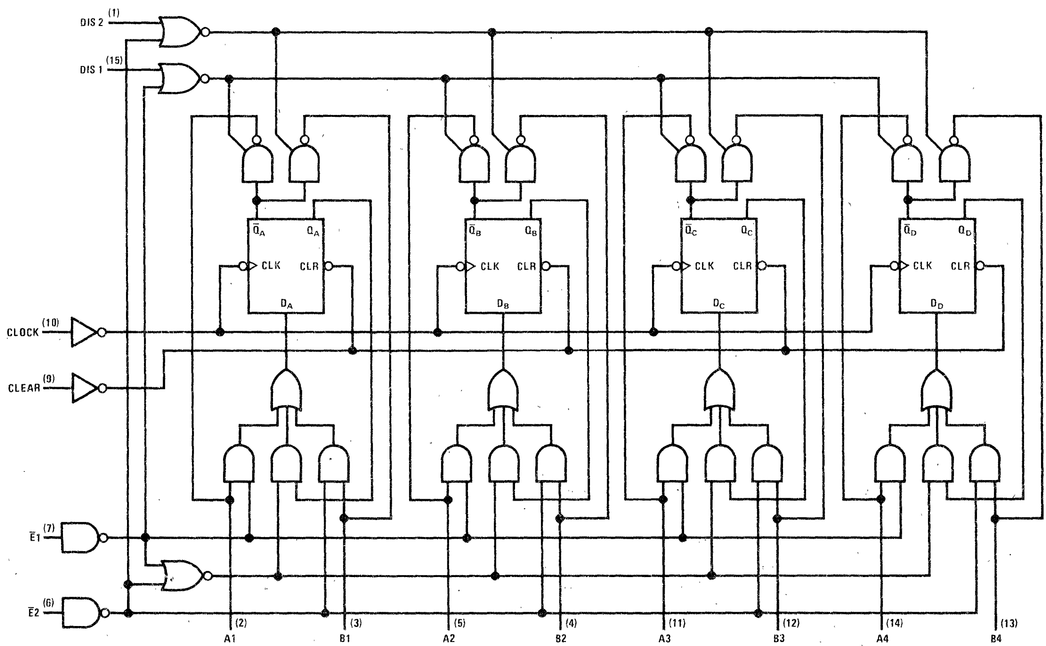
Truth Table

MODES OF OPERATION

DIS 1	DIS 2	Ē1	Ē2	A (1–4)	B (1–4)	COMMENTS
L	H	H	H	Q	Hi-Z	Output data to Bus A
H	L	H	H	Hi-Z	Q	Output data to Bus B
L	L	H	H	Q	Q	Output data to both buses
H	H	H	H	Hi-Z	Hi-Z	Store data with output in high impedance state
X	L	L	H	Data	Q_n	Enter data from Bus A
X	H	L	H	Data	Hi-Z	Enter data from Bus A
L	X	H	L	Q_n	Data	Enter data from Bus B
H	X	H	L	Hi-Z	Data	Enter data from Bus B
X	X	L	L	Data	Data	Enter data from both buses (logical "1" on either will dominate)

Clear = Logical "1," puts all outputs to L state.
X = Don't Care
Q_n = Data After Clock Transition

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM7542 MIN	DM7542 TYP(1)	DM7542 MAX	DM8542 MIN	DM8542 TYP(1)	DM8542 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−2.0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V V_{IL} = 0.8V	V_O = 0.4V			−40			−40	μA
			V_O = 2.4V			40			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.0	−1.6		−1.0	−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−25		−70	−25		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			80	120		80	120	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER			FROM	TO	CONDITIONS	DM75/8542 MIN	DM75/8542 TYP	DM75/8542 MAX	UNITS
f_{MAX}	Maximum Clock Frequency				C_L = 50 pF, R_L = 400Ω	30	40		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Output	C_L = 50 pF, R_L = 400Ω		25	38	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Output	C_L = 50 pF, R_L = 400Ω		23	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear	Output	C_L = 50 pF, R_L = 400Ω		24	36	ns
t_{ZH}	Output Enable Time to High Level				C_L = 50 pF, R_L = 400Ω		20	30	ns
t_{ZL}	Output Enable Time to Low Level				C_L = 50 pF, R_L = 400Ω		17	25	ns
t_{HZ}	Output Disable Time from High Level				C_L = 5 pF, R_L = 400Ω		6	15	ns
t_{LZ}	Output Disable Time from Low Level				C_L = 5 pF, R_L = 400Ω		15	25	ns
$t_{W(CLOCK)}$	Clock Pulse Width				C_L = 50 pF, R_L = 400Ω	20			ns
$t_{W(CLEAR)}$	Clear Pulse Width				C_L = 50 pF, R_L = 400Ω	20			ns
t_{SETUP}	Enable Setup Time	High Level			C_L = 50 pF, R_L = 400Ω	20	12		ns
		Low Level				20	13		ns
t_{SETUP}	Data Setup Time	High Level			C_L = 50 pF, R_L = 400Ω	5.0	−4.0		ns
		Low Level				10	4.5		ns
t_{HOLD}	Data Hold Time	High Level			C_L = 50 pF, R_L = 400Ω	5.0	−3.5		ns
		Low Level				10	4.5		ns

TRI-STATE Quad Switch Debouncers

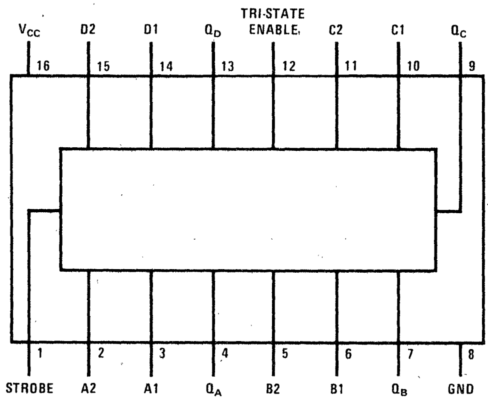
General Description

These circuits are for use in front panels, and similar applications where contact bounce must be eliminated. Within the single package, these circuits do the job of four R-S latches plus pull-up resistors. A strobe is also available which permits sampling of the switch information at a predetermined time. TRI-STATE outputs are also provided for direct connections to the switch line bus.

Features

- Replaces SN54279/74279
- Eliminates push-button noise
- Allows clocked devices to be operated from switches
- Maximum power dissipation 250 mW
- Bus-line connectable
- TRI-STATE outputs
- Typical propagation delay 18 ns

Connection Diagram

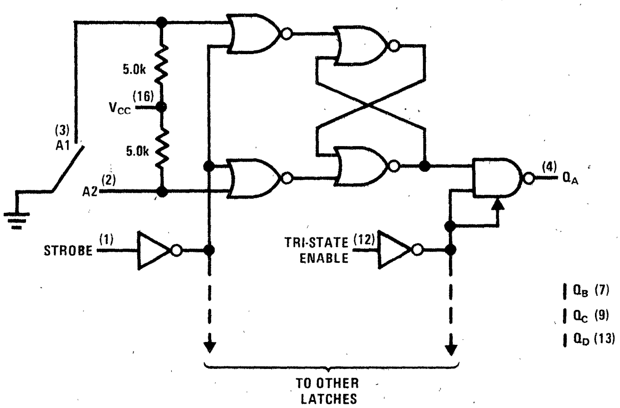


7544/8544(J), (N), (W)

Truth Table

A1	A2	TRI-STATE ENABLE	STROBE	$Q_{A(t)}$
X	X	H	X	Hi-Z
X	X	L	L	$Q_{A(t-1)}$
L	L	L	⌐L	Indeterminate
L	H	L	H	L
H	L	L	H	H
H	H	L	H	$Q_{A(t)}$

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	PARAMETER	CONDITIONS		DM75 44 MIN	DM75 44 TYP(1)	DM75 44 MAX	DM85 44 MIN	DM85 44 TYP(1)	DM85 44 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−2.0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 0.4V			−40			−40	µA
			V_O = 2.4V			40			40	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Strobe/Enable			−1.6			−1.6	mA
			Data			−2.5			−2.5	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−18	−30	−55	−18	−30	−55	mA
I_{CC}	Supply Current	V_{CC} = Max				50			50	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	PARAMETER	FROM	TO	CONDITIONS	DM75/85 44 MIN	DM75/85 44 TYP	DM75/85 44 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 50 pF, R_L = 400Ω		20	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output	C_L = 50 pF, R_L = 400Ω		17	30	ns
t_{ZH}	Output Enable Time to High Level			C_L = 50 pF, R_L = 400Ω		15	25	ns
t_{ZL}	Output Enable Time to Low Level			C_L = 50 pF, R_L = 400Ω		12	24	ns
t_{HZ}	Output Disable Time from High Level			C_L = 5 pF, R_L = 400Ω		5	10	ns
t_{LZ}	Output Disable Time from Low Level			C_L = 5 pF, R_L = 400Ω		10	20	ns

TRI-STATE 8-Bit Universal I/O Shift Registers

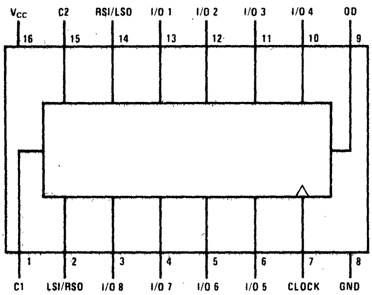
General Description

These circuits are TRI-STATE, 8-bit, edge-triggered, universal shift registers which are capable of operating in any of the following modes: shift left, shift right, parallel load, or inhibit. Since the clock is edge-triggered, the control lines which determine the mode of operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Features

- Positive-edge triggered clock
- "Do nothing" state without gating the clock
- Both parallel and serial data lines are TRI-STATE
- High impedance state does not impede shift mode with parallel outputs

Connection Diagram



7546(J), (W); 8546(J), (N), (W)

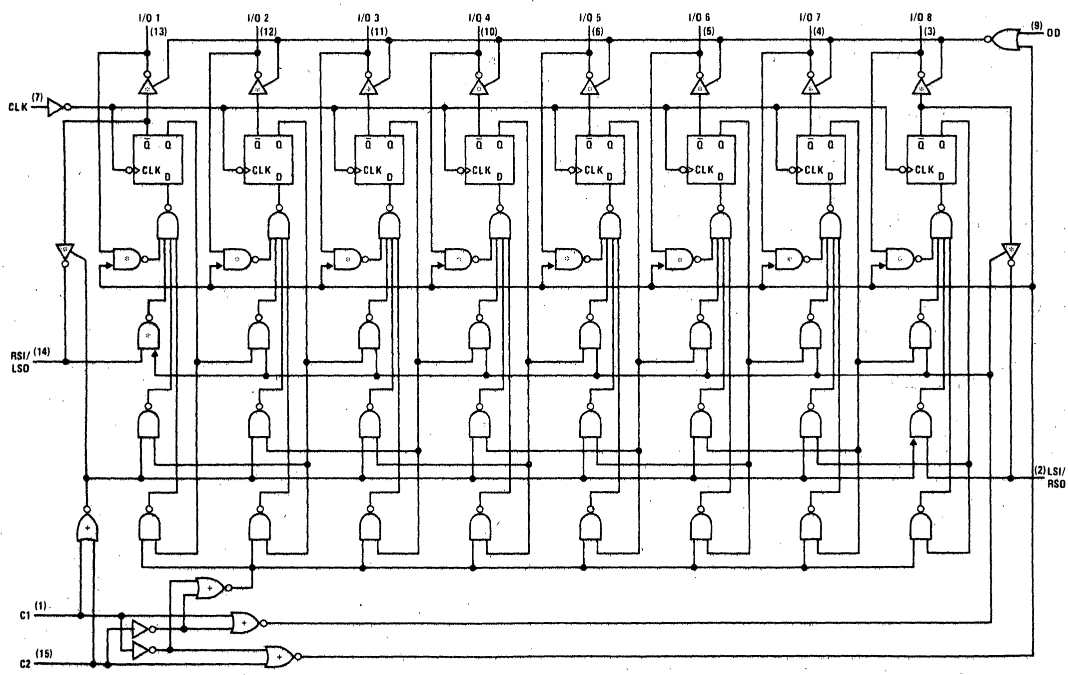
Truth Table

OD	C1	C2	MODE OF OPERATION	STATE OF PARALLEL I/O	STATE OF SERIAL I/O RSI/LSO	STATE OF SERIAL I/O LSI/RSO
L	H	H	Inhibit	Q_{OUT}	Hi-Z*	Hi-Z*
H	H	H	Inhibit	Hi-Z*	Hi-Z*	Hi-Z*
X	H	L	Parallel Load	Data In	Hi-Z*	Hi-Z*
L	L	H	Right Shift	Q_{OUT}	Data In	$Q_{OUT\ 8}$
H	L	H	Right Shift	Hi-Z*	Data In	$Q_{OUT\ 8}$
L	L	L	Left Shift	Q_{OUT}	$Q_{OUT\ 1}$	Data In
H	L	L	Left Shift	Hi-Z*	$Q_{OUT\ 1}$	Data In

OD = Output Disable (C1, C2 = Mode Controls)

*Both Input and Output of the I/O pin are in the high impedance state.

Logic Diagram



*TRI-STATE GATE

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM7546 MIN	DM7546 TYP(1)	DM7546 MAX	DM8546 MIN	DM8546 TYP(1)	DM8546 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−2.0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V V_{IL} = 0.8V	V_O = 0.4V			−40			−40	μA
			V_O = 2.4V			40			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	C2 Input			80			80	μA
			Others			40			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	C2 Input			−3.2			−3.2	mA
			Others			−1.6			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−70	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			80	115		80	125	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

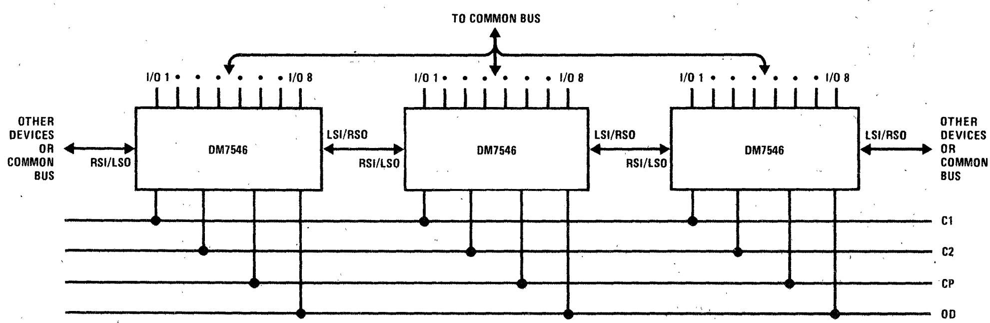
	PARAMETER	CONDITIONS	DM75/8546 MIN	DM75/8546 TYP	DM75/8546 MAX	UNITS
f_{MAX}	Maximum Clock Frequency	C_L = 50 pF, R_L = 400Ω	15	22		MHz
t_{PLH}	Propagation Delay, Low-to-High Level, From Clock to Output	C_L = 50 pF, R_L = 400Ω		16	24	ns
t_{PHL}	Propagation Delay, High-to-Low Level, From Clock to Output	C_L = 50 pF, R_L = 400Ω		27	40	ns
t_{ZH}	Propagation Delay From High Impedance State to High Logic Level (From Output Disable)	C_L = 50 pF, R_L = 400Ω		22	33	ns
t_{ZH}	Propagation Delay From High Impedance State to High Logic Level (From Mode Control C1/C2)	C_L = 50 pF, R_L = 400Ω		13	20	ns
t_{ZL}	Propagation Delay From High Impedance State to Low Logic Level (From Output Disable)	C_L = 50 pF, R_L = 400Ω		18	27	ns
t_{ZL}	Propagation Delay From High Impedance State to Low Logic Level (From Mode Control C1/C2)	C_L = 50 pF, R_L = 400Ω		15	23	ns
t_{HZ}	Propagation Delay From High Logic Level to High Impedance State (From Output Disable)	C_L = 5 pF, R_L = 400Ω		5	8	ns
t_{HZ}	Propagation Delay From High Logic Level to High Impedance State (From Mode Control C1/C2)	C_L = 5 pF, R_L = 400Ω		9	14	ns
t_{LZ}	Propagation Delay From Low Logic Level to High Impedance State (From Output Disable)	C_L = 5 pF, R_L = 400Ω		16	24	ns
t_{LZ}	Propagation Delay From Low Logic Level to High Impedance State (From Mode Control C1/C2)	C_L = 5 pF, R_L = 400Ω		17	26	ns

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		CONDITIONS	DM75/85 46 MIN	TYP	MAX	UNITS
$t_{W(CLOCK)}$	Clock Pulse Width	$C_L = 50$ pF, $R_L = 400\Omega$	18	12		ns
$t_{SETUP\ (HIGH)}$	Serial Data		38	25		ns
$t_{SETUP\ (HIGH)}$	Parallel Data		33	22		ns
$t_{SETUP\ (LOW)}$	Serial Data		21	14		ns
$t_{SETUP\ (LOW)}$	Parallel Data		18	12		ns
$t_{HOLD\ (HIGH)}$	Serial Data		0	−11		ns
$t_{HOLD\ (HIGH)}$	Parallel Data		0	−11		ns
$t_{HOLD\ (LOW)}$	Serial Data		0	−22		ns
$t_{HOLD\ (LOW)}$	Parallel Data		0	−21		ns
SETUP AND HOLD TIMES BETWEEN CHANGES IN MODE CONTROL AND CLOCKING						
t_{SETUP}	Parallel Load to Right Shift	$C_L = 50$ pF, $R_L = 400\Omega$	32	21		ns
t_{SETUP}	Parallel Load to Left Shift		40	27		ns
t_{SETUP}	Right Shift to Parallel Load		60	40		ns
t_{SETUP}	Left Shift to Parallel Load		53	35		ns
t_{SETUP}	Right Shift to Left Shift		33	21		ns
t_{SETUP}	Left Shift to Right Shift		56	37		ns
t_{SETUP}	Inhibit to Right Shift		57	38		ns
t_{SETUP}	Inhibit to Left Shift		65	43		ns
t_{SETUP}	Right Shift to Inhibit		50	33		ns
t_{SETUP}	Left Shift to Inhibit		50	32		ns
t_{HOLD}	Parallel Load to Right Shift		9	6		ns
t_{HOLD}	Parallel Load to Left Shift		6	4		ns
t_{HOLD}	Right Shift to Parallel Load		0	−13		ns
t_{HOLD}	Left Shift to Parallel Load		0	−46		ns
t_{HOLD}	Right Shift to Left Shift		0	−10		ns
t_{HOLD}	Left Shift to Right Shift		0	−23		ns
t_{HOLD}	Inhibit to Right Shift		0	−18		ns
t_{HOLD}	Inhibit to Left Shift		0	−16		ns
t_{HOLD}	Right Shift to Inhibit		0	−12		ns
t_{HOLD}	Left Shift to Inhibit		0	−29		ns

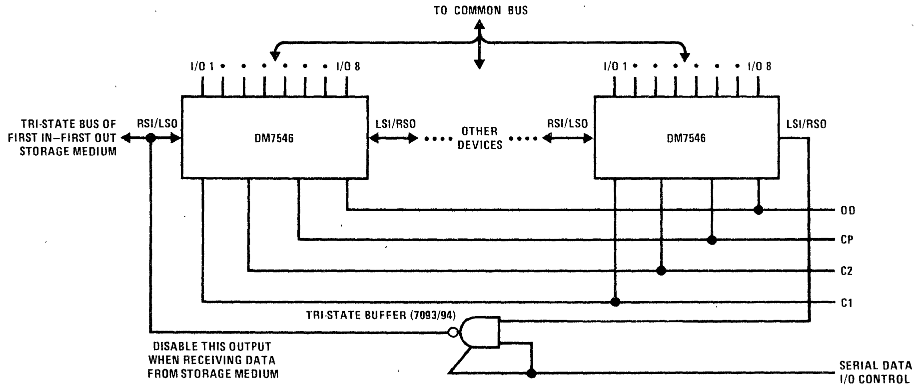
Typical Applications

CASCADING DEVICES



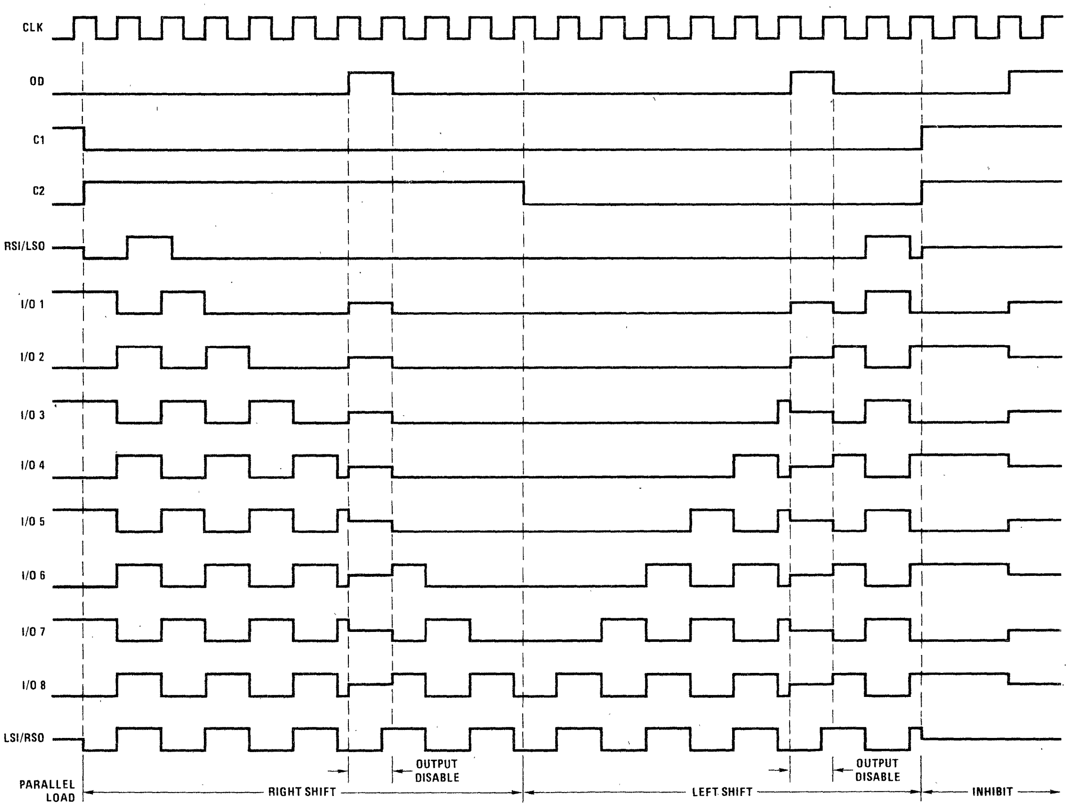
Typical Applications (Continued)

SERIAL DATA TRANSFER TO A FIRST IN-FIRST OUT STORAGE MEDIUM



Timing Diagram

TYPICAL PARALLEL LOAD, RIGHT SHIFT, LEFT SHIFT AND INHIBIT SEQUENCES

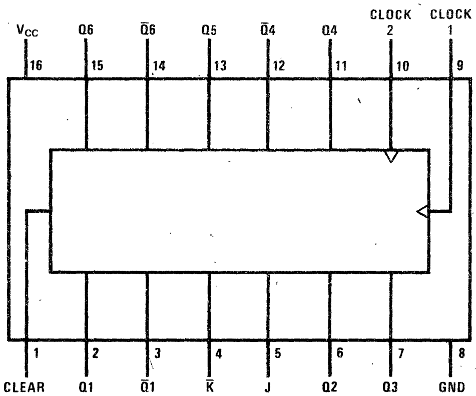


6-Bit Shift Registers

General Description

These 6-bit shift registers feature J-$\overline{K}$ serial inputs, parallel outputs, and a direct overriding clear. All inputs are buffered to lower the input drive requirements to one standard DM74S load. Furthermore, shifting is synchronous, and occurs on the positive-going edge of the clock pulse. These shift registers are particularly well-suited for very high speed data processing systems.

Connection Diagram



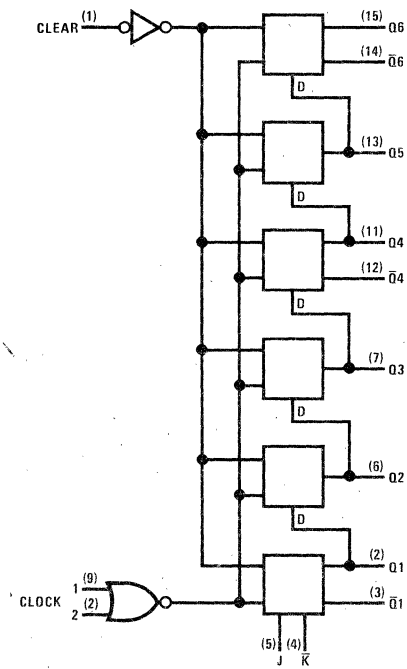
Truth Table

INPUTS					OUTPUTS					
CLEAR	CLOCKS 1	CLOCKS 2	J	$\overline{K}$	Q1	Q2	Q3	Q4	Q5	Q6
L	X	X	X	X	L	L	L	L	L	L
H	L	L	X	X	$Q1_0$	$Q2_0$	$Q3_0$	$Q4_0$	$Q5_0$	$Q6_0$
H	L	H	X	X	$Q1_0$	$Q2_0$	$Q3_0$	$Q4_0$	$Q5_0$	$Q6_0$
H	H	L	X	X	$Q1_0$	$Q2_0$	$Q3_0$	$Q4_0$	$Q5_0$	$Q6_0$
H	H	H	X	X	$Q1_0$	$Q2_0$	$Q3_0$	$Q4_0$	$Q5_0$	$Q6_0$
H	↑	L	L	L	L	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	↑	L	L	H	$Q1_N$	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	↑	L	H	L	$\overline{Q1}_N$	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	↑	L	H	H	H	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	L	↑	L	L	L	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	L	↑	L	H	$Q1_N$	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	L	↑	H	L	$\overline{Q1}_N$	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	L	↑	H	H	H	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$
H	↑	H	X	X	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$	$Q6_N$
H	H	↑	X	X	$Q1_N$	$Q2_N$	$Q3_N$	$Q4_N$	$Q5_N$	$Q6_N$

$Q1_0$, $Q2_0$, etc. = The level of Q1, Q2, etc. before the indicated steady-state input conditions were established.

$Q1_N$, $Q2_N$, etc. = The level of Q1, Q2, etc. before the most-recent ↑ transition of the clock; indicates a 1-bit shift.

Logic Diagram



To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM85S S50 MIN	DM85S S50 TYP(1)	DM85S S50 MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{OH}	High Level Output Current				−1.0	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −1 mA	2.7	3.4		V
I_{OL}	Low Level Output Current				20	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 20 mA			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max		90	150	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS	DM85S S50 MIN	DM85S S50 TYP	DM85S S50 MAX	UNITS
f_{MAX}	Maximum Clock Frequency			C_L = 15 pF, R_L = 280Ω	75	110		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Q or $\overline{Q}$			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock	Q or $\overline{Q}$			12	18	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clear	$\overline{Q}$			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Q			13	20	ns

TRI-STATE 4-Bit D Type Registers

General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the truth table.

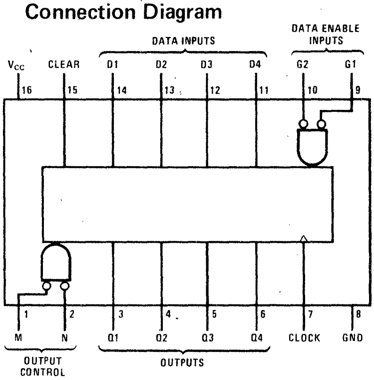
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers

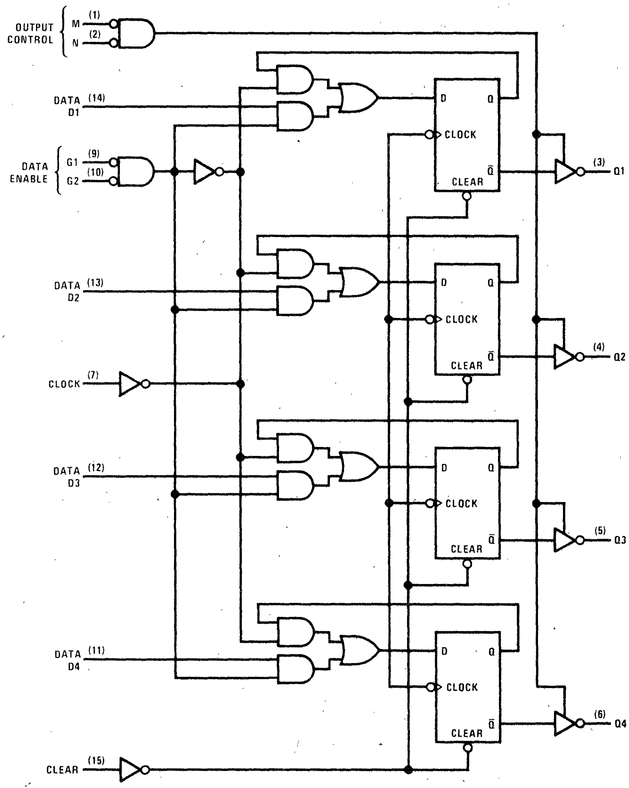
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL FREQUENCY	TYPICAL POWER DISSIPATION
7551/8551	18 ns	30 MHz	250 mW
75L51/85L51	59 ns	15 MHz	27.5 mW

Connection Diagram



7551(J), (W); 8551(J), (N), (W);
75L51/85L51(J), (N), (W)

Logic Diagram



Truth Table

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
Q_0 = the level of Q before the indicated steady state input conditions were established

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM75/85 51 MIN	TYP(1)	MAX	DM75L/85L L51 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5			N/A	V
I_{OH}	High Level Output Current		DM75			−2.0			−1.0	mA
			DM85			−5.2			−1.0	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current		DM75			16			2.0	mA
			DM85			16			3.6	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V	DM75			0.4		0.15	0.3	V
		V_{IL} = Max, I_{OL} = Max	DM85			0.4		0.2	0.4	
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.3V						−40	μA
		V_{IH} = 2V	V_O = 0.4V			−40				
		V_{IL} = Max	V_O = 2.4V			40			20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1		0.01	0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40		1	10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V						−0.18	mA
			V_I = 0.4V			−1.6				
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−70	−3	−8	−15	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			50	72		5.5	9	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) I_{CC} is measured with all outputs open; clear grounded following momentary connection to 4.5V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5V.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER		FROM	TO	CONDITIONS BOTH	STD.	LOW POWER	DM75/85 51 MIN	TYP	MAX	DM75L/85L L51 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				C_L = 50 pF	R_L = 400Ω	R_L = 4 kΩ	25	30		6	15		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear	Output	C_L = 50 pF	R_L = 400Ω	R_L = 4 kΩ		18	27		72	110	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Output	C_L = 50 pF	R_L = 400Ω	R_L = 4 kΩ		16	25		39	70	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Output	C_L = 50 pF	R_L = 400Ω	R_L = 4 kΩ		20	28		77	120	ns
t_{ZH}	Output Enable Time to High Level				C_L = 50 pF	R_L = 400Ω	R_L = 4 kΩ	7	16	30		28	55	ns
t_{ZL}	Output Enable Time to Low Level				C_L = 50 pF	R_L = 400Ω	R_L = 4 kΩ	7	21	30		35	60	ns
t_{HZ}	Output Disable Time from High Level				C_L = 5 pF	R_L = 400Ω	R_L = 4 kΩ	3	5	14		18	50	ns
t_{LZ}	Output Disable Time from Low Level				C_L = 5 pF	R_L = 400Ω	R_L = 4 kΩ	3	11	20		32	75	ns
t_W	Width of Clock or Clear Pulse							20			100			ns
t_{SETUP}	Setup Time	Data Enable						17			45			ns
		Data						10			30			
		Clear Inactive State						10			30			
t_{HOLD}	Hold Time	Data Enable						2			0			ns
		Data						10			10			

TRI-STATE Synchronous Counters/Latches

General Description

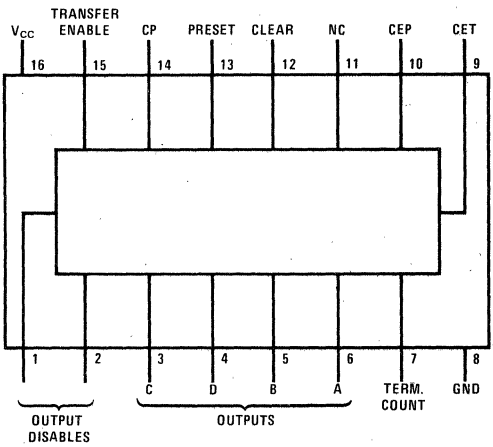
These circuits logically combine the functions of counters for frequency division, latches to store the data from the counters, and output buffer gates which provide both standard TTL outputs as well as high-impedance outputs for multiplexing of data. The counters are fully synchronous, and are made up of four edge-triggered JK flip-flops. To further facilitate operation, the Count Mode and Terminal Count outputs are also operable when the data outputs are in the high-impedance state or the latch mode.

Features

- DM7552/8552 DM75L52/85L52 — Decade counter/latch
- DM7554/8554 DM75L54/85L54 — Binary counter/latch

TYPE	TYPICAL POWER DISSIPATION	TYPICAL CLOCK FREQUENCY
52, 54	330 mW	23 MHz
L52, L54	38 mW	11 MHz

Connection Diagram



7552(J), (W); 8552(J), (N), (W);
75L52/85L52(J), (N), (W);
7554(J), (W); 8554(J), (N), (W);
75L54/85L54(J), (N), (W)

Truth Table

INPUTS							OUTPUTS				
OD1	OD2	CEP	CET	CLEAR	PRESET	TE	A	B	C	D	TC
H	X	X	X	X	X	X	"High Impedance State"				*
X	H	X	X	X	X	X	"High Impedance State"				*
L	L	X	X	H	X	H	L	L	L	L	L
L	L	X	X	L	H	H	H	H	H	H	*
L	L	X	X	X	X	L	LATCH				*
L	L	H	H	L	L	H	COUNT				*

*Function of the count sequence.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM75/85 52, 54 MIN	TYP(1)	MAX	DM75L/85L L52, L54 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			N/A	V
I_{OH}	High Level Output Current		DM75			−2.0			−1.0	mA
			DM85			−5.2			−1.0	
V_{OH}	High Level Output Voltage, Terminal Count	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OH} = 0.2 mA				2.4	2.8		V
			I_{OH} = 0.4 mA	2.4	3.3					
	High Level Output Voltage, Others		I_{OH} = Max	2.4	3.3		2.4	2.7		
I_{OL}	Low Level Output Current		DM75			16			2.0	mA
			DM85			16			3.6	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM75		0.2	0.4		0.15	0.3	V
			DM85		0.2	0.4		0.2	0.4	
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = Max	V_O = 0.3V						−40	μA
			V_O = 0.4V			−40				
			V_O = 2.4V			40			20	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V	CET Input			2		0.02	0.2	mA
			Others			1		0.01	0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	CET Input			80		2	20	μA
			Others			40		1	10	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Std.), V_I = 0.3V (75L/85L)	CET Input		−2.0	−3.2		−0.24	−0.36	mA
			Others		−1.0	−1.6		−0.12	−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	TC Output	−20		−55	−3	−8	−15	mA
			Others	−30		−70	−3	−8	−15	
I_{CC}	Supply Current	V_{CC} = Max			66	106		7.6	13	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM7552/8552 or DM7554/8554 duration of short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS BOTH	STD.	LOW POWER	DM75/85 52, 54 MIN	TYP	MAX	DM75L/85L L52, L54 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency			C_L = 50 pF	R_L = 400Ω	R_L = 4 kΩ	15	23		6	11		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Output					34	70		115	220	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock	Output					23	45		75	150	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Transfer Enable	Output					26	50		90	160	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Transfer Enable	Output					26	50		90	160	ns
t_{ZH}	Output Enable Time to High Level							21	45		75	150	ns
t_{ZL}	Output Enable Time to Low Level							25	50		90	150	ns
t_{HZ}	Output Disable Time from High Level			C_L = 5 pF				3	8		8	15	ns
t_{LZ}	Output Disable Time from Low Level							17	40		57	105	ns

Mode of Operation

When the Transfer Enable (TE) is at a logical "1" level, the data transfer paths between the counter outputs and the output buffer gates are maintained. When the Transfer Enable is at a logical "0" level, the data transfer paths are inhibited, and the state of the output buffer gates are locked in by the latches. The counter and Terminal Count (TC) output remain operable during this time.

Asynchronous Clear resets the counter to 0000.

Asynchronous Preset sets the counter to 1111. The 1111 state may be used in the 52 for blanking out leading zeroes in visual displays. The next clock pulse will advance the 52 to 0001 which denotes the first count of the blanked zero. The next clock pulse will advance the 54 to 0000.

The Terminal Count (TC) output is active high when the counters are at terminal count and the CET is high. The Terminal Count logic equations are:

(52) $TC = CET \cdot A \cdot \overline{B} \cdot \overline{C} \cdot D$

(54) $TC = CET \cdot A \cdot B \cdot C \cdot D$

The following logic levels control the device:

- The counters change state on the positive-going transition of the clock.
- Clearing or presetting is enabled by taking the respective input to a logical "1" level.
- To enable the count mode both CET and CEP inputs must be at a logical "1" level.
- To latch the outputs the Transfer Enable (TE) input must be taken to the logical "0" level.
- To place the TRI-STATE outputs into the "third-state," either of the Output Disable (OD) inputs must be taken to the logical "1" level.

The clock input must be high during the high to low transition of CEP and/or CET for correct logic operation. The CEP and CET inputs may be used in a high speed look ahead technique.

Counter stages can be cascaded to provide multiple stage BCD or Binary synchronous counting by using the 52 or the 54 respectively. With a Terminal Count (TC) fan out of ten, eleven stages are able to operate at the maximum frequency equivalent to a two stage counter.

The characters displayed can be held with a low level on the strobe line while the counters can continue counting. The display can be updated at any time by applying a positive pulse to the strobe line.

DM7552/DM8552
DM75L52/DM85L52
DECADE COUNT SEQUENCE

COUNT	OUTPUTS				
	A	B	C	D	TC
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	H
**If Preset Applied					
Next	H	H	H	H	L
Count	H	L	L	L	L

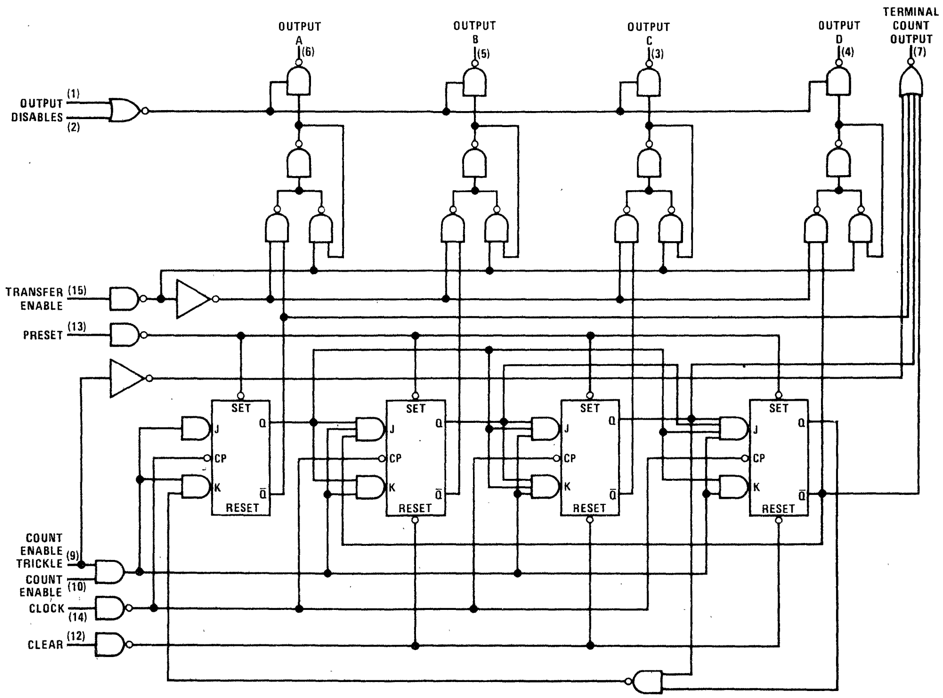
**The 1111 state may be used in conjunction with certain decoder/drivers (DM7446A, 7447A, 7448) for blanking leading zeroes.

DM7554/DM8554
DM75L54/DM85L54
BINARY COUNT SEQUENCE

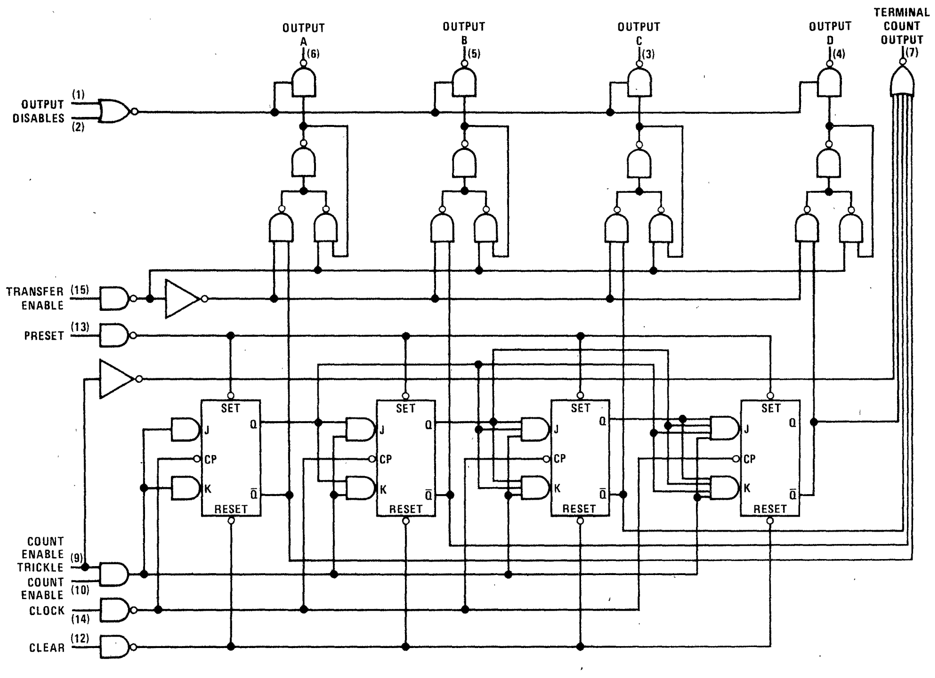
COUNT	OUTPUTS				
	A	B	C	D	TC
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	H

Logic Diagrams

52, L52

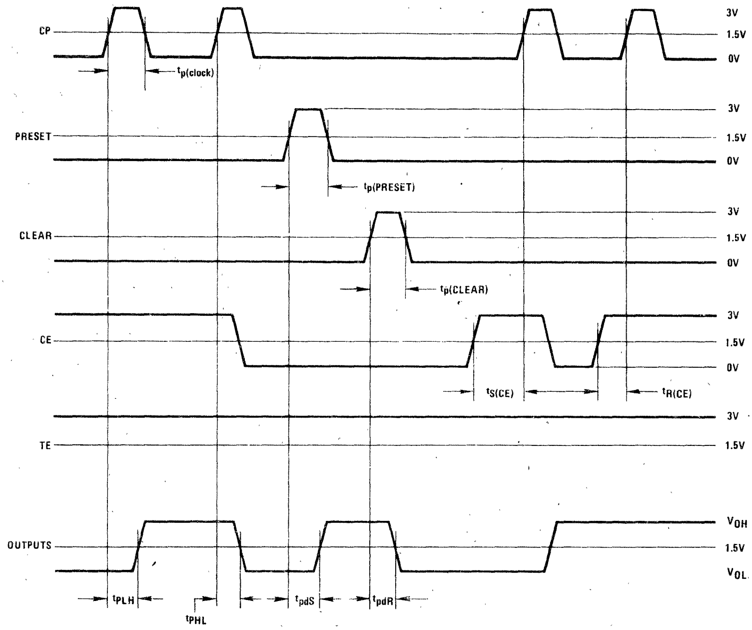


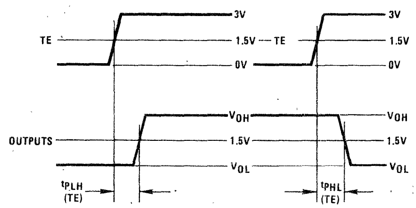
54, L54



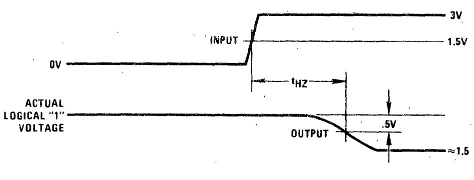
Switching Time Waveforms

52, 54

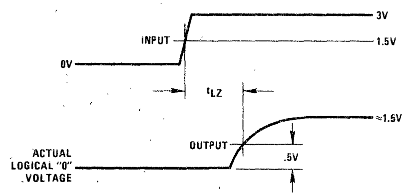




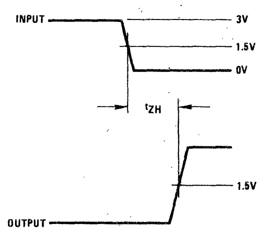
t_{HZ}



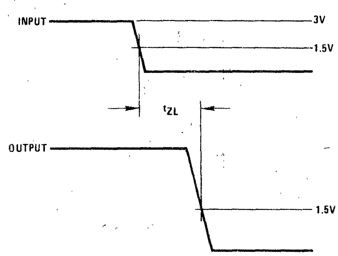
t_{LZ}



t_{ZH}

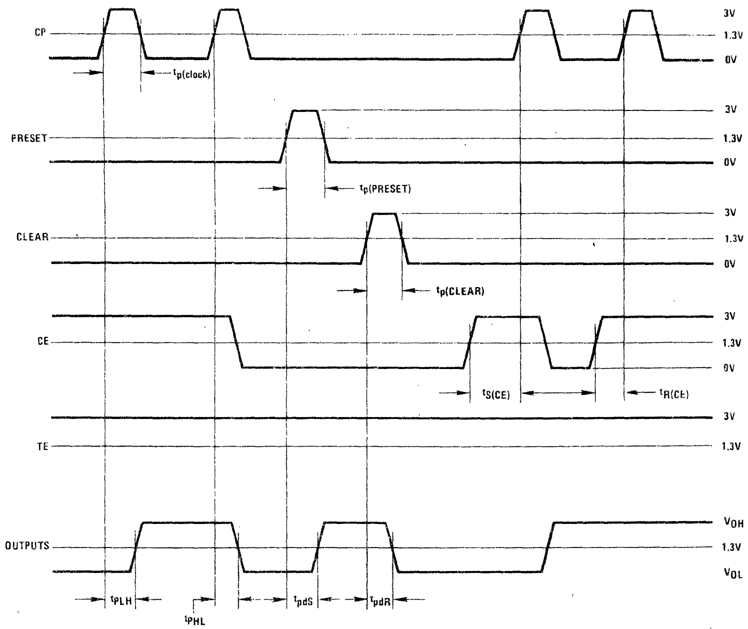


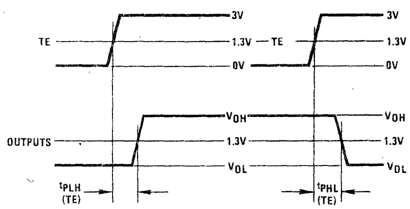
t_{ZL}



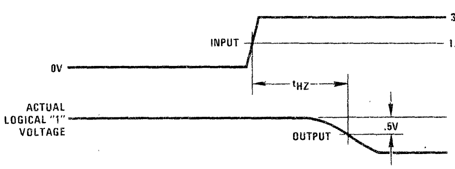
Switching Time Waveforms (Continued)

L52, L54

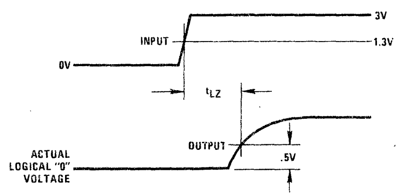




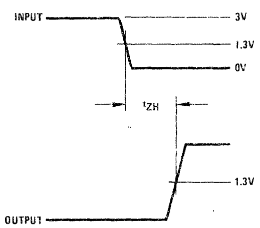
t_{HZ}



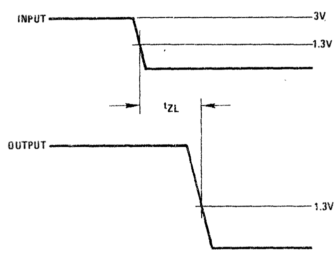
t_{LZ}



t_{ZH}



t_{ZL}



TRI-STATE 8-Bit Latches

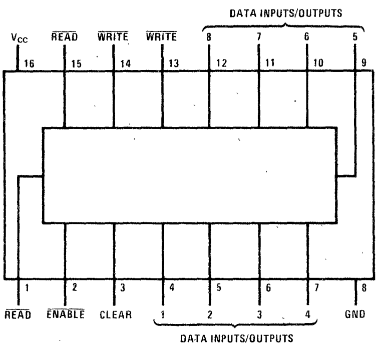
General Description

By utilizing TRI-STATE circuitry on the outputs, the inputs and outputs can be accessed on the same pins, and these circuits provide eight separate $\overline{R}$-$\overline{S}$ latches in the popular 16-pin package. While in the high-impedance state, the inputs and outputs are disabled and no information can be entered. When both $\overline{\text{WRITE}}$ inputs are brought to a low logic level, the outputs are disabled and new information may be entered at the inputs. When a low logic level is applied to both $\overline{\text{READ}}$ inputs, and a high logic level to both $\overline{\text{WRITE}}$ inputs, the inputs are rendered inactive and data may be read from the outputs.

Features

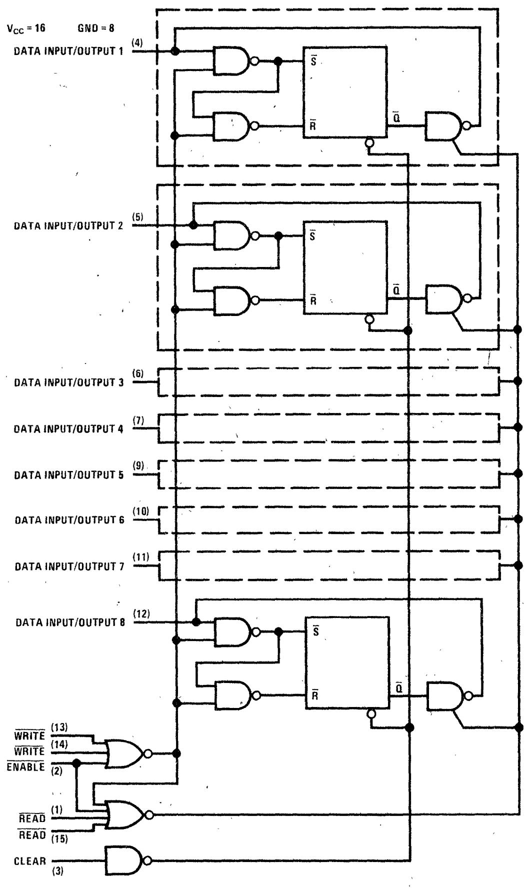
- TRI-STATE I/O pins
- 8 latches in popular 16-pin package
- Typical propagation delay—22 ns

Connection Diagram



7553(J), (W); 8553(J), (N), (W)

Logic Diagram



Truth Table

CLEAR	$\overline{\text{ENABLE}}$	$\overline{\text{READ}}$*	$\overline{\text{WRITE}}$**	OPERATION	STATE OF BUS
H	L	L	H	Enter L	L
H	L	L	L	Enter L	Hi-Z
L	X	H	H	Do Nothing	Hi-Z
L	H	X	X	Do Nothing	Hi-Z
L	L	X	L	Write	H or L***
L	L	L	H	Read	H or L***

*Both Read Inputs
**Both Write Inputs
***Depends on State of Latch

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM75 53 MIN	DM75 53 TYP(1)	DM75 53 MAX	DM85 53 MIN	DM85 53 TYP(1)	DM85 53 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−2 0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V V_{IL} = 0.8V	V_O = 0.4V			−40			−40	μA
			V_O = 2.4V			40			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−28		−70	−28		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			66	93		66	93	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER			FROM	TO	CONDITIONS	DM75/85 53 MIN	DM75/85 53 TYP	DM75/85 53 MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear	Output	C_L = 50 pF, R_L = 400Ω		21	32	ns
t_{ZH}	Output Enable Time to High Level				C_L = 50 pF, R_L = 400Ω		22	33	ns
t_{ZL}	Output Enable Time to Low Level				C_L = 50 pF, R_L = 400Ω		25	38	ns
t_{HZ}	Output Disable Time from High Level				C_L = 5 pF, R_L = 400Ω		7	12	ns
t_{LZ}	Output Disable Time from Low Level				C_L = 5 pF, R_L = 400Ω		20	30	ns
t_W	Minimum Pulse Width	Clear				15	10		ns
		$\overline{\text{Write}}$				40	28		
t_{SETUP}	Minimum Data Setup Time	High Level				20	14		ns
		Low Level				36	26		
t_{HOLD}	Minimum Data Hold Time	High Level				−15	−26		ns
		Low Level				−8	−14		

TRI-STATE Programmable Decade/Binary Counters

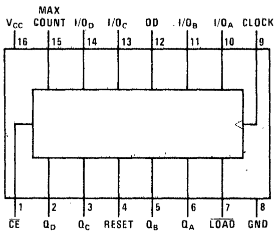
General Description

These circuits are synchronous, edge-sensitive, fully-programmable 4-bit counters. The counters feature both conventional totem-pole and TRI-STATE outputs; such that when the outputs are in the high-impedance mode, they can be used to enter data from the bus lines. In addition, the clear input operates completely independent of all other inputs. During the programming operation, data is loaded into the flip-flops on the positive-going edge of the clock pulse. To facilitate cascading of these counters, the MAX COUNT output can be tied directly into the count enable input.

Features

- DM7555/8555—Decade counter
- DM7556/8556—Binary counter
- Typical clock frequency 35 MHz
- TRI-STATE outputs
- Fully independent clear
- Synchronous loading
- Cascading circuitry provided internally

Connection Diagram



7555(J), (W); 8555(J), (N), (W); 7556(J), (W); 8556(J), (N), (W)

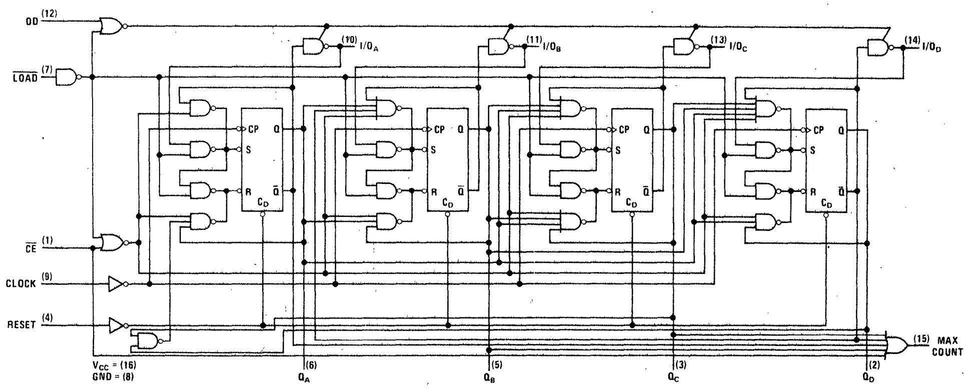
Truth Table

J	K	M	CLEAR	Q_{n+1}
0	0	1	0	Q_n
1	0	1	0	1
0	1	1	0	0
1	1	1	0	$\overline{Q}_n$
X	X	0	0	D
X	X	X	1	0*

*Asynchronous Transition
Note: See Timing Diagrams

Logic Diagrams

55



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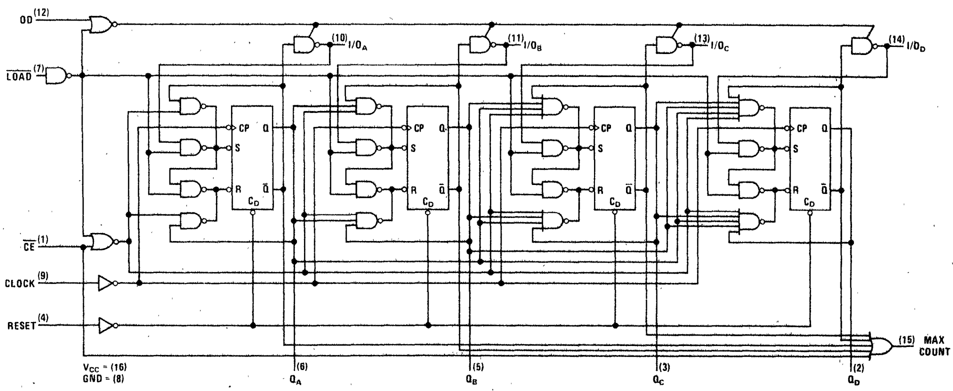


Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM75/8555 MIN	DM75/8555 TYP(1)	DM75/8555 MAX	DM75/8556 MIN	DM75/8556 TYP(1)	DM75/8556 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current		DM75			−2.0			−2.0	mA
			DM85			−5.2			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA		0.4			0.4			V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = Max	V_O = 0.4V			−40			−40	μA
			V_O = 2.4V			40			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−25		−70	−25		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			80	110		75	100	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

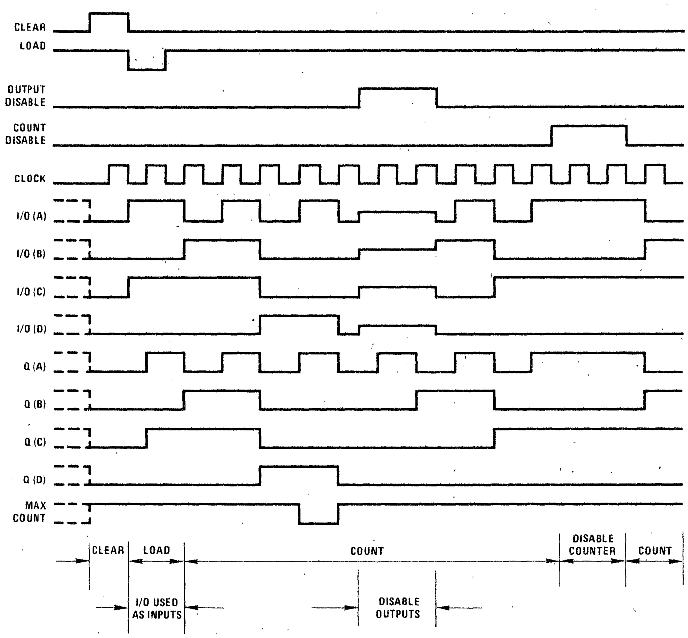
(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER		FROM	TO	CONDITIONS	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				C_L = 50 pF, R_L = 400Ω	25	35		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Output			15	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Output			34	44	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Max Count			23	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Max Count			23	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear	Output			30	44	ns
t_{ZH}	Output Enable Time to High Level						13	20	ns
t_{ZL}	Output Enable Time to Low Level						14	20	ns
t_{HZ}	Output Disable Time from High Level				C_L = 5 pF, R_L = 400Ω		6	12	ns
t_{LZ}	Output Disable Time from Low Level						12	20	ns
t_W	Minimum Pulse Width	Clock				25			ns
		Clear				20			
		Load				30			
$t_{\overline{CE}}$	Count Enable Time	Setup				30			ns
		Hold				−30			
$t_{SETUP(1)}$	Setup Time — High Logic Level	Data				25			ns
		Load				30			
$t_{HOLD(1)}$	Hold Time — High Logic Level	Data				5			ns
		Load				−10			
$t_{SETUP(0)}$	Setup Time — Low Logic Level	Data				30			ns
		Load				25			
$t_{HOLD(0)}$	Hold Time — Low Logic Level	Data				5			ns
		Load				−10			

Timing Diagrams

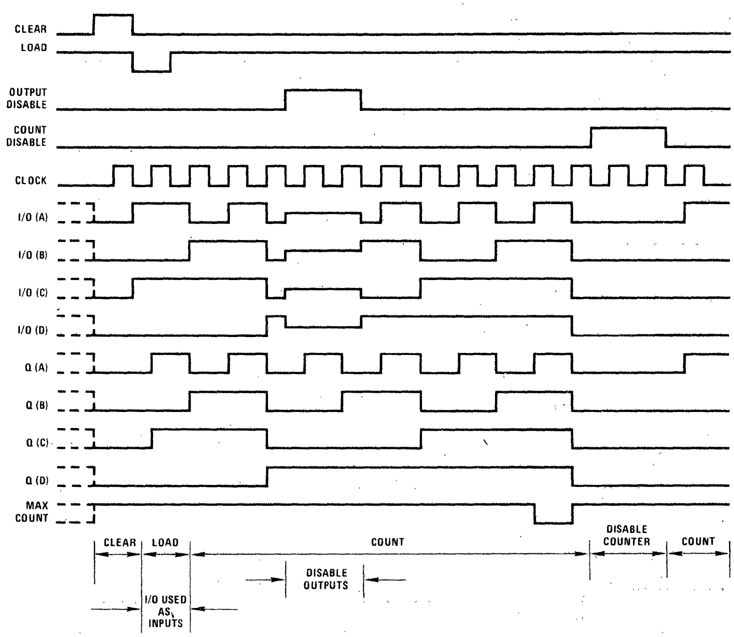
55 TYPICAL CLEAR, PRESET, COUNT, INHIBIT SEQUENCE



Sequence

(1) Clear to zero.
(2) Load BCD five.
(3) Count six, seven, eight, nine, zero, one, two, three, four.
(4) Disable TRI-STATE outputs.
(5) Disable counter.
(6) Count to six.

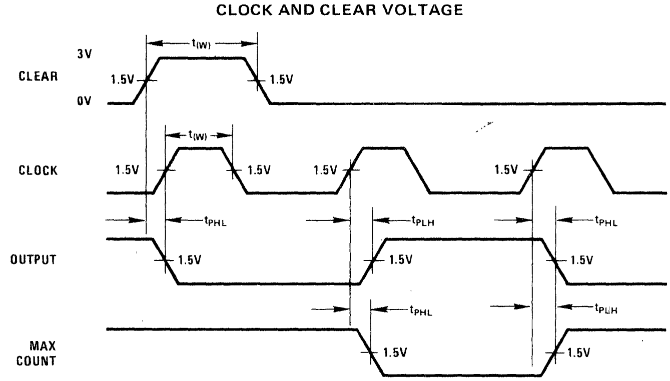
56 TYPICAL CLEAR, PRESET, COUNT, INHIBIT SEQUENCE

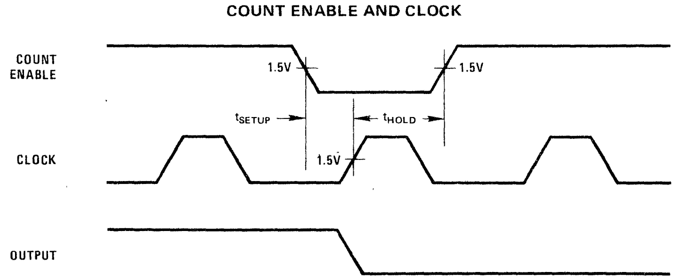


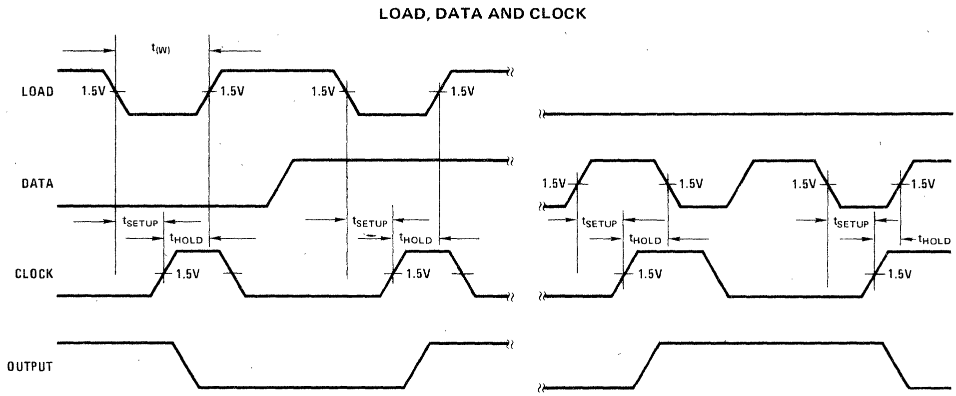
Sequence

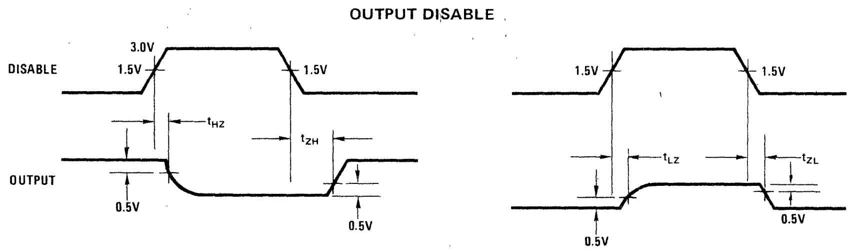
(1) Clear to zero.
(2) Load binary five.
(3) Count six, seven, eight, nine, ten, eleven, twelve, thirteen, fourteen, fifteen, zero.
(4) Disable TRI-STATE outputs.
(5) Disable counter.
(6) Count to one.

Switching Time Waveforms









Synchronous 4-Bit Up/Down Decade Counters

General Description

These circuits are synchronous up/down counters; the 60 and L60 circuits are BCD counters and the 63 and L63 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

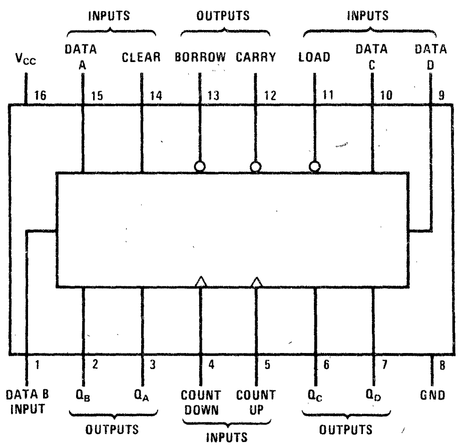
These circuits are synchronous up/down counters; the 60 and L60 circuits are BCD counters and the 63 and L63 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

TYPE	TYPICAL COUNT FREQUENCY	TYPICAL POWER DISSIPATION
60, 63	25 MHz	325 mW
L60, L63	12 MHz	40 mW

Connection Diagram



7560(J), (W); 8560(J), (N), (W);
75L60/85L60(J), (N), (W);
7563(J), (W); 8563(J), (N), (W);
75L63/85L63(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM75/85 60, 63 MIN	TYP(1)	MAX	DM75L/85L L60, L63 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−400			−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current		DM75			16			2.0	mA
			DM85			16			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM75			0.4		0.15	0.3	V
			DM85			0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40		<1	10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V					−0.10	−0.18	mA
		V_{CC} = Max	V_I = 0.4V			−1.6				mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM75	−20		−55	−3	−9	−15	mA
			DM85	−18		−55	−3	−9	−15	mA
I_{CC}	Supply Current	V_{CC} = Max(3)	DM75		65	89		8	13	mA
			DM85		65	102		8	13	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

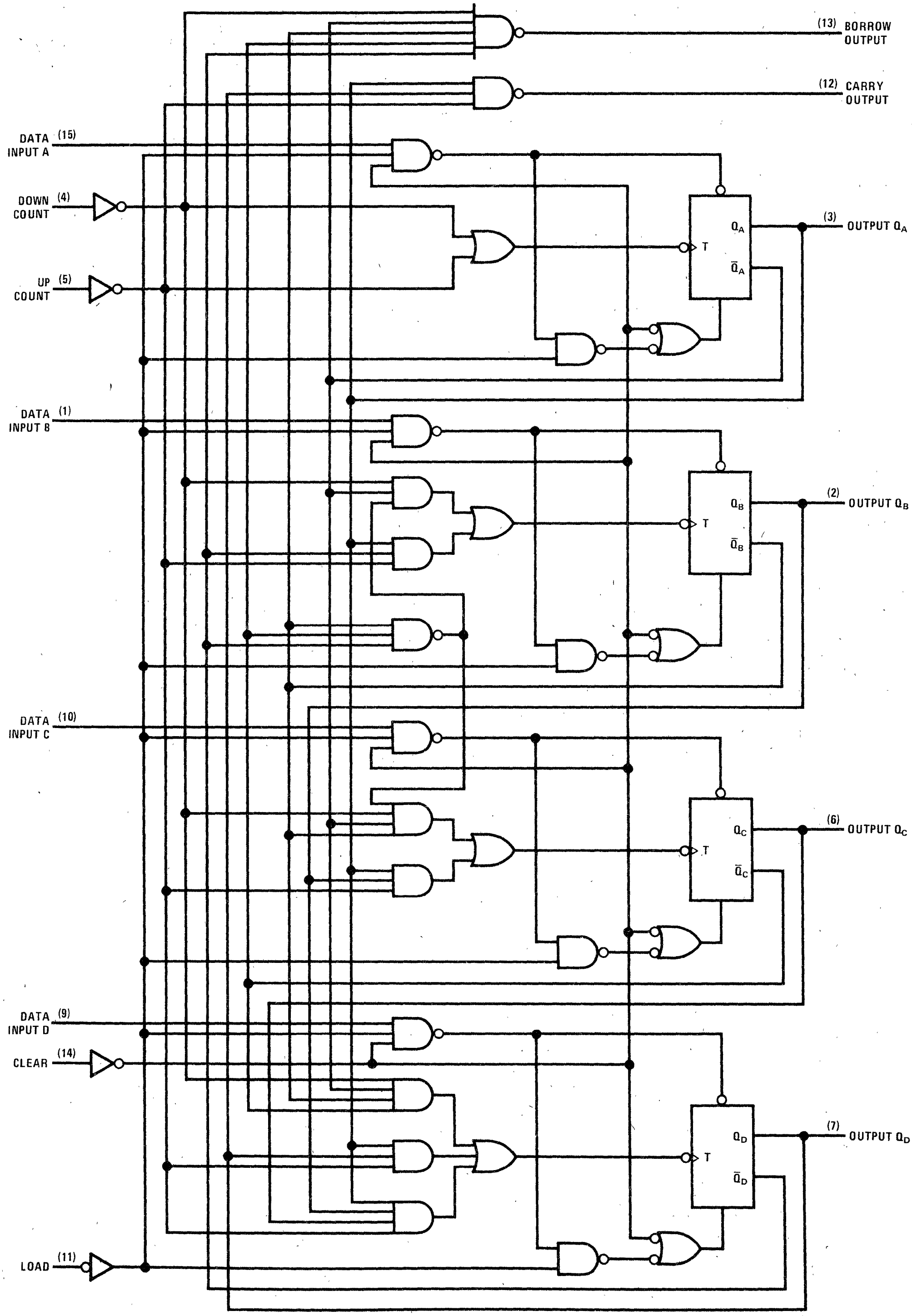
(3) I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM INPUT	TO OUTPUT	DM75/85 60, 63 CONDITIONS	MIN	TYP	MAX	DM75L/85L L60, L63 CONDITIONS	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency			C_L = 15 pF, R_L = 400Ω	20	25		C_L = 50 pF, R_L = 4 kΩ	6	12		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Count up	Carry			17	26			30	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Count up	Carry			16	24			60	120	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Count down	Borrow			16	24			30	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Count down	Borrow			16	24			50	100	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Either Count	Q			25	38			45	90	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Either Count	Q			31	47			75	150	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Load	Q			27	40			55	110	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Load	Q			29	40			105	200	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Q			22	35			95	190	ns
t_W	Width of Any Input Pulse				25				70			ns
t_{SETUP}	Data Setup Time				20				30			ns
t_{HOLD}	Data Hold Time				0				0			ns

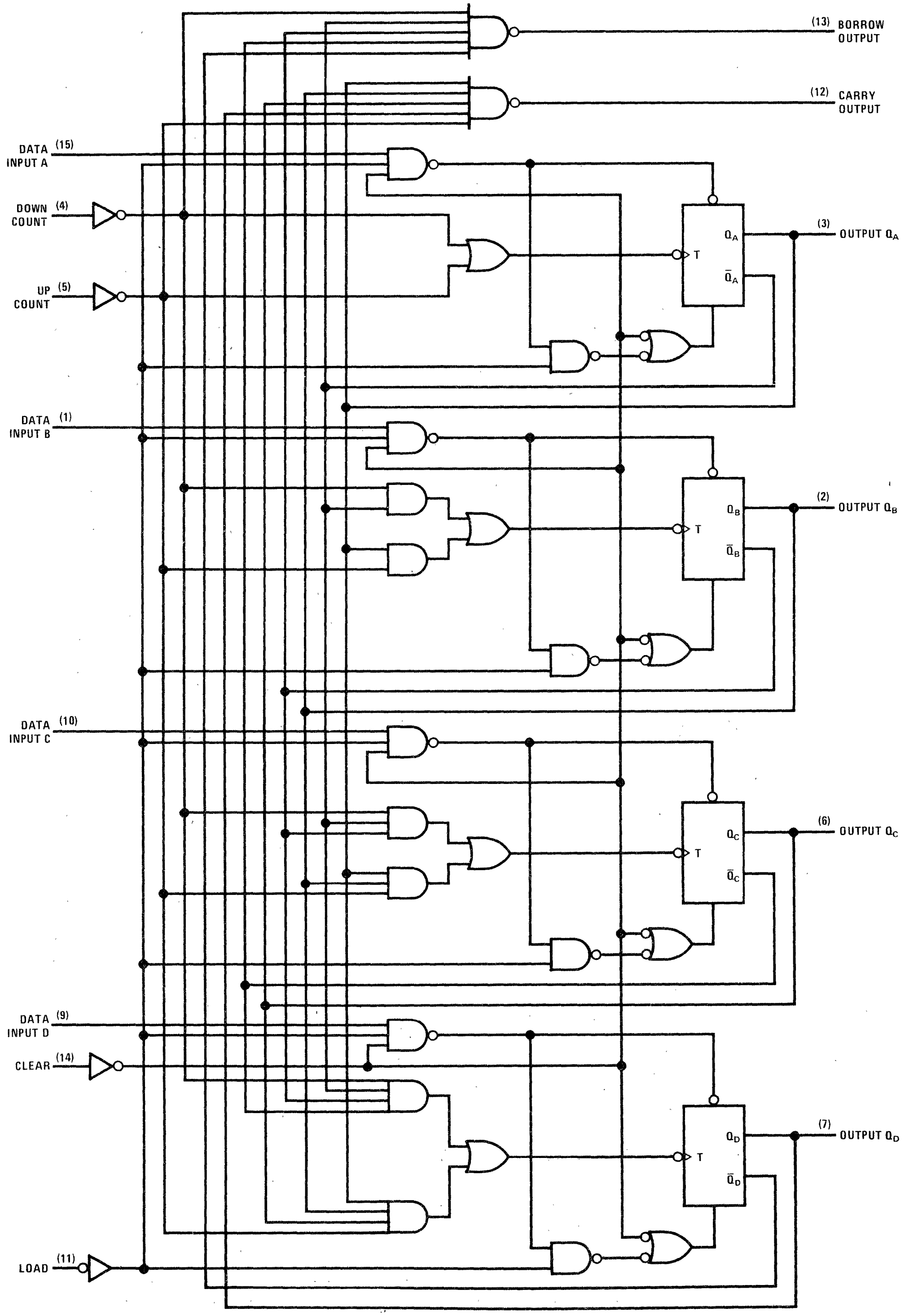
Logic Diagrams

60, L60



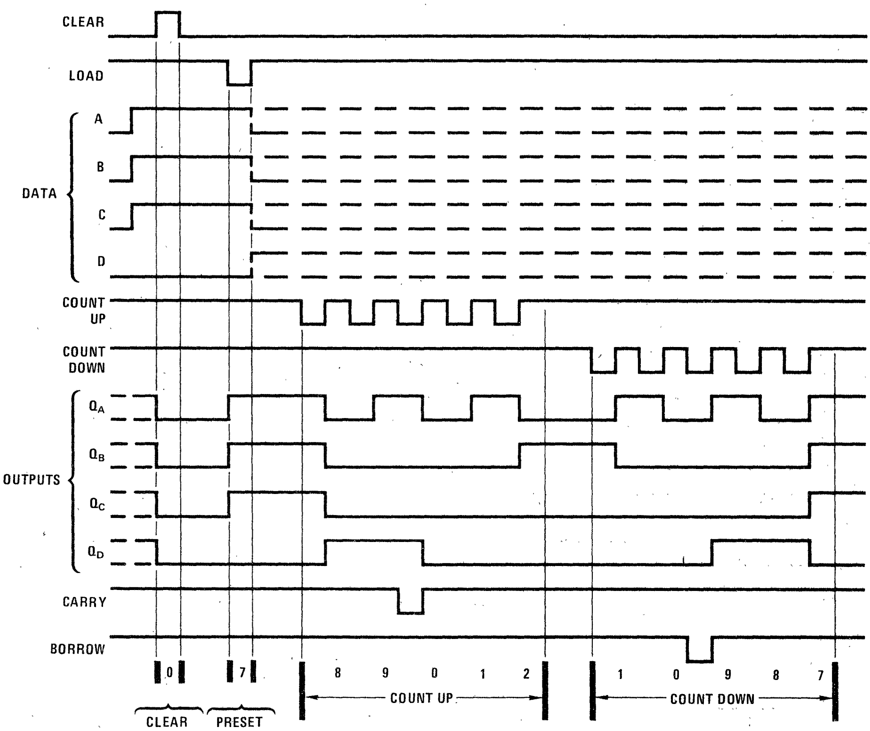
Logic Diagrams (Continued)

63, L63



Timing Diagrams

60, L60 DECADE COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



Sequence:

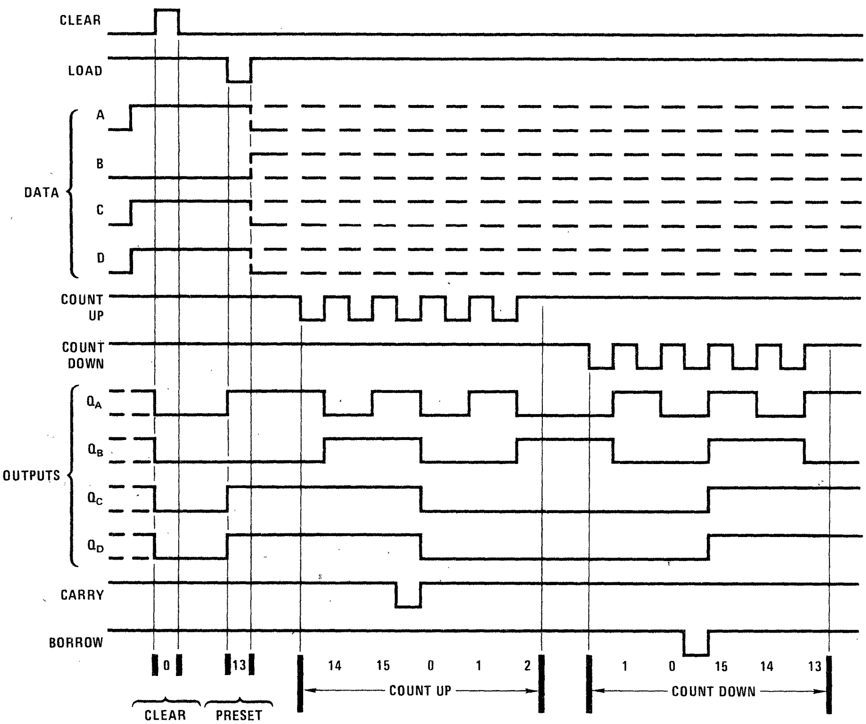
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one, and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

Notes:

(A) Clear overrides load, data, and count inputs.
(B) When counting up, count-down input must be high; when counting down, count-up input must be high.

Timing Diagrams (Continued)

63, L63 BINARY COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



Sequence:

(1) Clear outputs to zero.

(2) Load (preset) to binary thirteen.

(3) Count up to fourteen, fifteen, carry, zero, one, and two.

(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Notes:

(A) Clear overrides load, data, and count inputs.

(B) When counting up, count-down input must be high; when counting down, count-up input must be high.

64-Bit Edge Triggered Registers

General Description

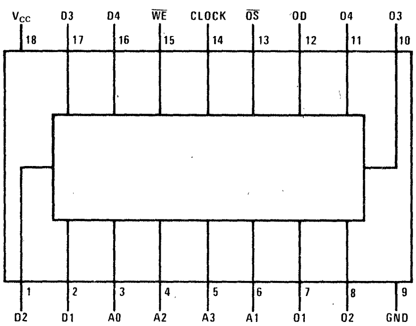
The DM75S68/DM85S68 is an addressable "D" register file. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

Features

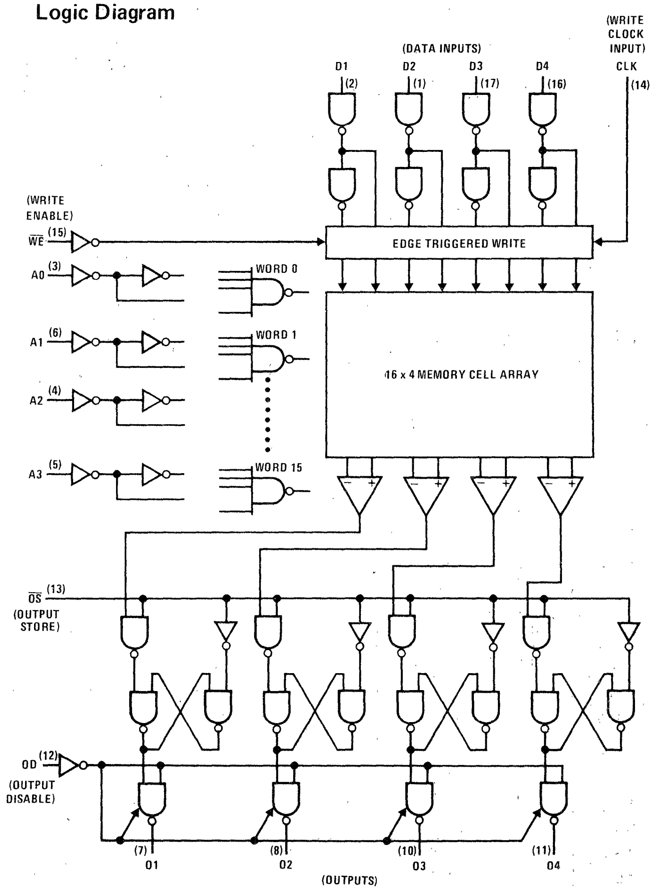
- On chip output register
- Edge triggered write
- High speed 30 ns typ
- TRI-STATE outputs
- Optimized for register stack applications
- Typical power dissipation 350 mW
- 18-pin package

Connection Diagram



75S68(D); 85S68(D), (N)

Logic Diagram



To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS			DM75S/85S S68 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA					−1.2	V
I_{OH}	High Level Output Current			DM75			−2.0	mA
				DM85			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA	DM75	2.4			V
			I_{OH} = −5.2 mA	DM85				
I_{OL}	Low Level Output Current						16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		DM75			0.5	V
				DM85			0.45	
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.5V				−40	μA
			V_O = 2.4V				+40	
I_I	Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V					1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Clock Input				50	μA
			All Others				25	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Clock Input				−500	μA
			All Others				−250	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)			−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max				70	100	mA

Notes
(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) Not more than one output should be shorted at a time.

Switching Characteristics

PARAMETER			CONDITIONS	DM75S MIN	DM75S TYP	DM75S MAX	DM85S MIN	DM85S TYP	DM85S MAX	UNITS
t_{AA}	Access Time	Address to Output	C_L = 30 pF, R_L = 400Ω		30	55		30	40	ns
t_{OSA}		Output Store to Output			20	35		20	30	ns
t_{CA}		Clock to Output			25	50		25	40	ns
t_{ZH}	Output Enable to High Level				20	40		20	35	ns
t_{ZL}	Output Enable to Low Level				14	30		14	24	ns
t_{HZ}	Output Disable Time From High Level		C_L = 5 pF, R_L = 400Ω		10	18		10	15	ns
t_{LZ}	Output Disable Time From Low Level				12	22		12	18	ns
t_{ASC}	Set-Up Time	Address to Clock		25	5		15	5		ns
t_{DSC}		Data to Clock		15	0		5	0		ns
t_{ASOS}		Address to Output Store		40	15		30	15		ns
t_{WESC}		Write Enable Set-Up Time		10	0		5	0		ns
t_{OSSC}		Store Before Write		15	0		10	0		ns
t_{AHC}	Hold Time	Address From Clock		15	5		10	5		ns
t_{DHC}		Data From Clock		20	5		15	5		ns
t_{AHOS}		Address From Output Store		10	0		5	0		ns
t_{WEHC}		Write Enable Hold Time		20	5		15	5		ns

Typical Applications

The DM85S68 can enhance the dynamic performance of a TTL processor, since it may safely operate using single phase clocking instead of the multiphase clocking systems being used currently. This simple feature not only enhances the system's dynamic performance, since multiple levels of registers need not be activated, but also reduces component count by elimination of one set of buffer registers. For example, note the simplicity of the register file/ALU loop shown in *Figure 1.*

In a 4-bit slice with zero delay within the arithmetic logic unit, a level-triggered memory with buffering to prevent logic oscillation requires about 80 ns to make the loop whereas the DM85S68 does it in 35 ns. With a 30 ns delay in the ALU, the two compared system speeds are 110 ns and 65 ns, respectively.

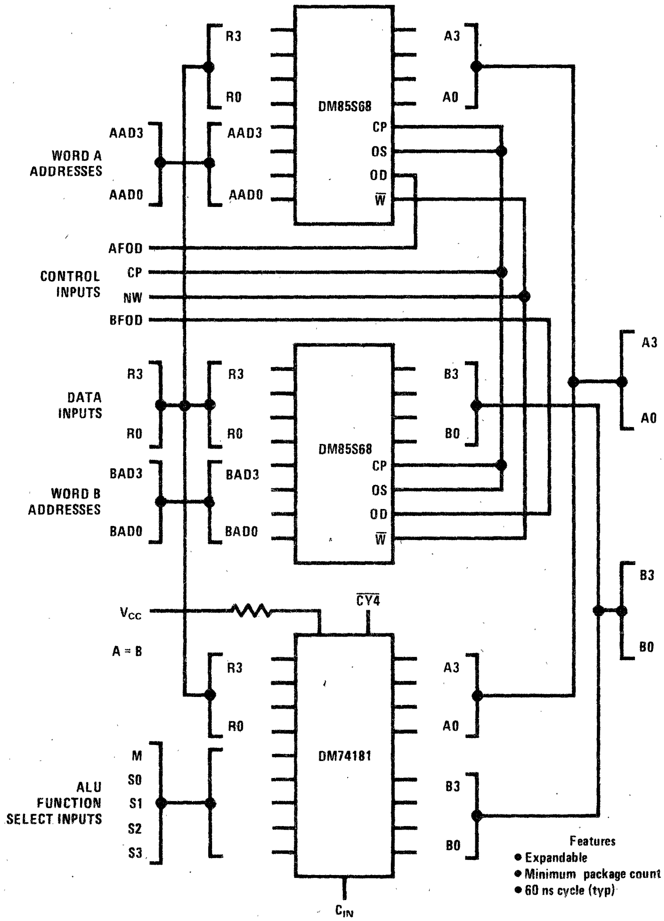
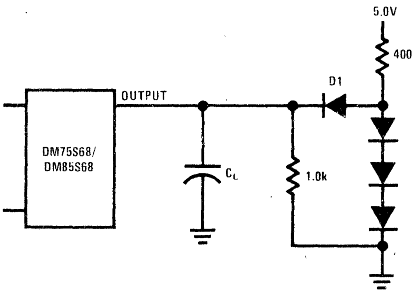


FIGURE 1. 4-BIT REGISTER ALU

Truth Table

OD	$\overline{WE}$	CLK	$\overline{OS}$	MODE	OUTPUTS
L	X	X	L	Output Store	Data From Last Addressed Location
X	L	⌐	X	Write Data	Dependent on State of OD and $\overline{OS}$
L	X	X	H	Read Data	Data Stored in Addressed Location
H	X	X	L	Output Store	Hi-Z
H	X	X	H	Output Disable	Hi-Z

AC Test Circuit and Switching Time Waveforms



C_L includes probe and jig capacitance
All diodes are 1N3064

WRITE CYCLE

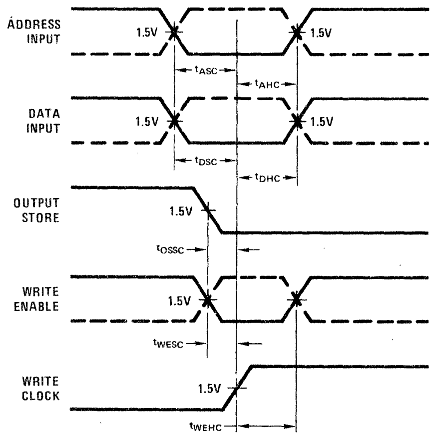


FIGURE 2. CLOCK SET-UP AND HOLD TIME

READ CYCLE

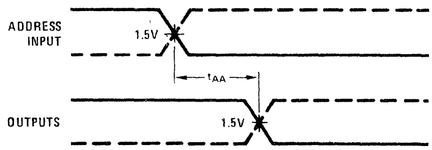


FIGURE 4. ADDRESS TO OUTPUT ACCESS TIME

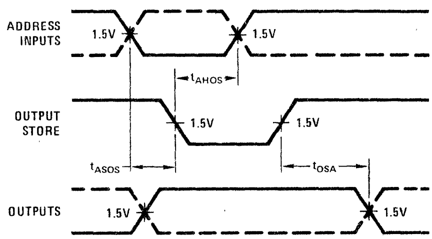


FIGURE 5. OUTPUT STORE ACCESS, SET-UP AND HOLD TIME

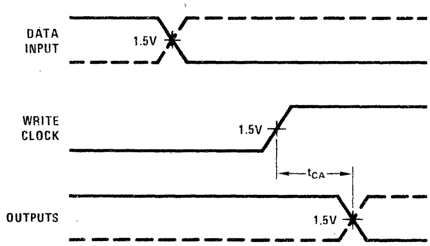


FIGURE 3. CLOCK TO OUTPUT ACCESS

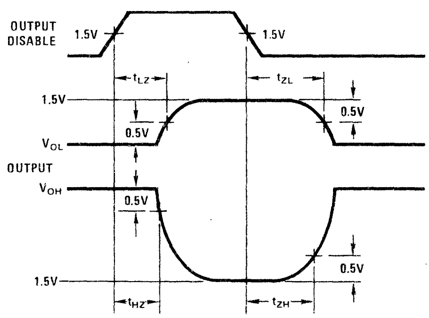


FIGURE 6. OUTPUT DISABLE AND ENABLE TIME

Note: Input waveforms supplied by pulse generator having the following characteristics: V = 3.0V, $t_R \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, and Z_{OUT} = 50 MΩ.

8-Bit Serial In/Parallel Out Shift Registers

General Description

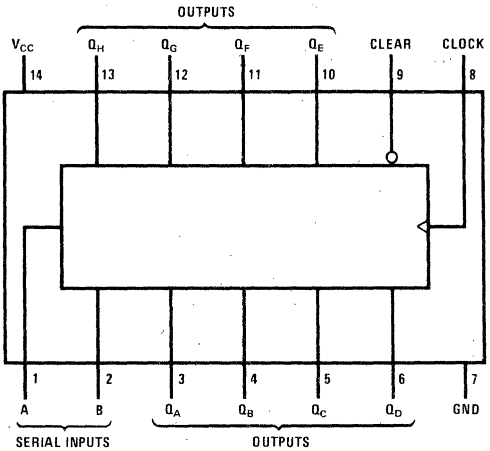
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

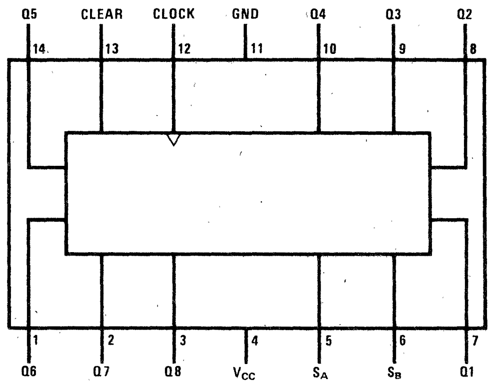
- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear

TYPE	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
70	36 MHz	185 mW
L70	14 MHz	30 mW

Connection Diagrams



7570(J), (W); 8570(J), (N), (W)



76L70/86L70(W)

Truth Table

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B . . .	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM75/85 70 MIN	DM75/85 70 TYP(1)	DM75/85 70 MAX	DM76L/86L L70 MIN	DM76L/86L L70 TYP(1)	DM76L/86L L70 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			N/A	V
I_{OH}	High Level Output Current					−400			−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OH} = Max		2.4	3.2		2.4			V
I_{OL}	Low Level Output Current		DM75, 76L			8			2	mA
			DM85, 86L			8			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OL} = Max	DM75, 76L		0.2	0.4			0.3	V
			DM85, 86L		0.2	0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V	Clear			1			0.2	mA
			Other			1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Clear			40			20	μA
			Other			40			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V (DM76L, 86L) V_I = 0.4V (DM75, 85)	Clear			−1.6			−0.36	mA
			Other			−1.6			−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM75, 76L	−10		−27.5	−3	−9	−15	mA
			DM85, 86L	−9		−27.5	−3	−9	−15	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			37	54		6	9	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

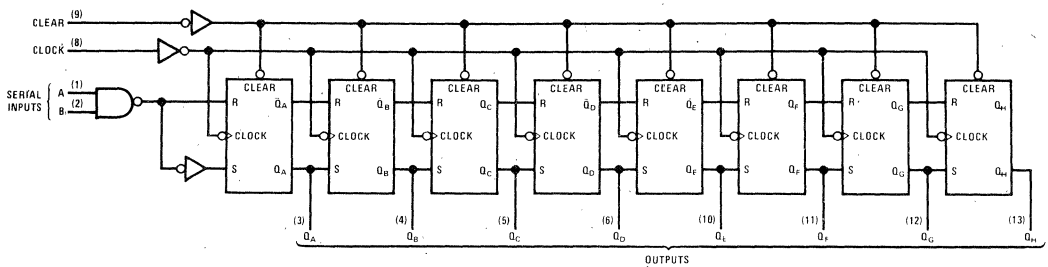
(2) Not more than one output should be shorted at a time.

(3) I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V, applied to clear.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

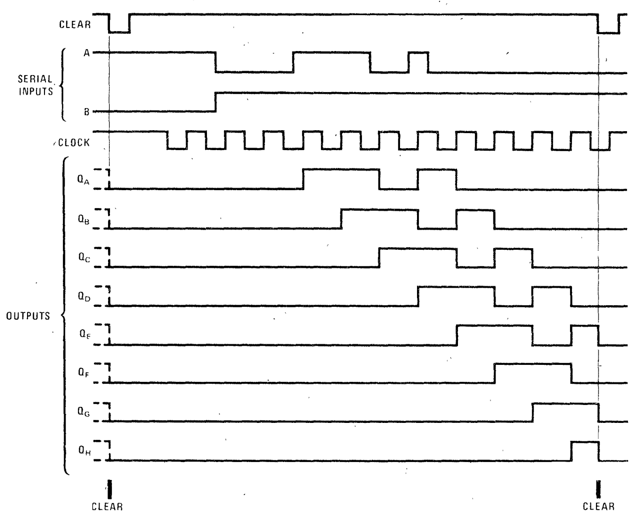
PARAMETER		CONDITIONS		DM75/85 70 MIN	DM75/85 70 TYP	DM75/85 70 MAX	DM76L/86L L70 MIN	DM76L/86L L70 TYP	DM76L/86L L70 MAX	UNITS
f_{MAX}	Maximum Clock Frequency	R_L = 800Ω (DM75, 85) R_L = 4 kΩ (DM76L, 86L)	C_L = 15 pF	25	36		6	14		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level Outputs From Clear Input		C_L = 15 pF		24	36				ns
			C_L = 50 pF		28	42		75	120	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Outputs From Clock Input		C_L = 15 pF	8	17	27				ns
			C_L = 50 pF	10	20	30		50	85	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Outputs From the Clock Input		C_L = 15 pF	10	21	32				ns
			C_L = 50 pF	10	25	37		90	135	ns
t_W	Width of Clock or Clear Input Pulse			20			60	40		ns
t_{SETUP}	Data Setup Time			15			40	20		ns
t_{HOLD}	Data Hold Time			5			20	−5		ns

Logic Diagram



Timing Diagram

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



1024-Bit Field Programmable Read Only Memories

General Description

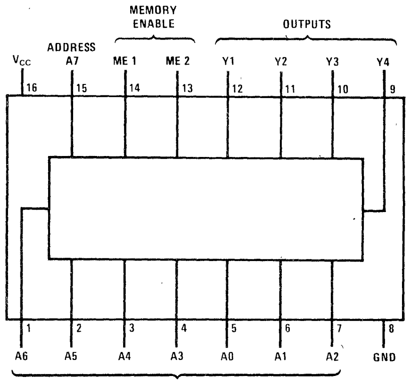
The DM7573/DM8573 is a field-programmable read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight address inputs. Two overriding memory enable inputs are provided; when either or both of the enable inputs are taken to a high state, all the outputs will be turned off. A logical "1" has been built into each bit location. A logical "0" can be programmed into any bit by selecting the proper word, disabling the chip, and applying a programming pulse to the proper output.

An additional feature of the DM7573/DM8573 is that its outputs can be tested in the logical "0" state without permanently programming the memory. In order to place all outputs in the logical "0" state, a 10V level is applied to the most significant address input, Pin 15. This feature will allow a much more complete test to be made before a part is shipped, thus minimizing customer problems.

Features

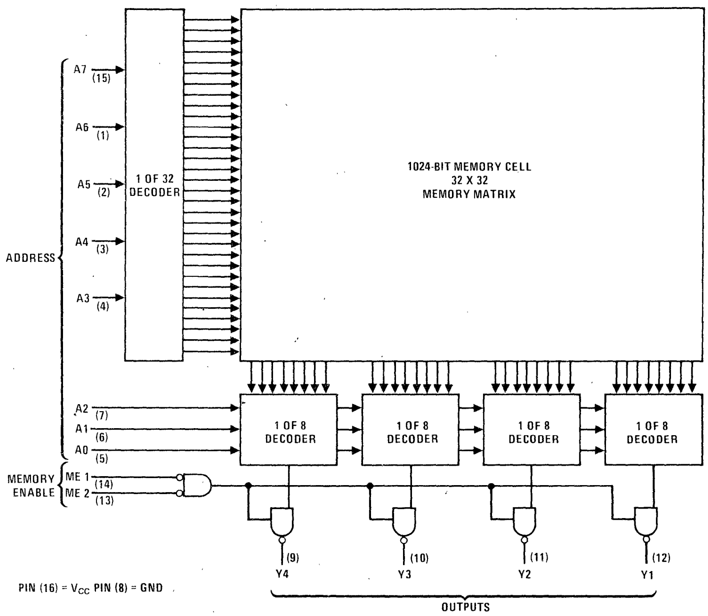
- Pin-compatible with SN54187/SN74187
- Outputs can be fully tested before programming
- Typical power dissipation 400 mW
- Propagation delay 60 ns

Connection Diagram



7573(J); 8573(J), (N)

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM75/85 73 MIN	DM75/85 73 TYP(1)	DM75/85 73 MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Max, V_{OH} = 4.0V			50	μA
I_{OL}	Low Level Output Current				16	mA
V_{OL}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1	mA
I_{CC}	Supply Current	V_{CC} = Max		80	110	mA

Notes

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

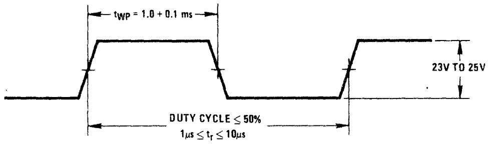
PARAMETER		FROM	TO	CONDITIONS	DM75/85 73 MIN	DM75/85 73 TYP	DM75/85 73 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address	Output	C_L = 30 pF R_{L1} = 600Ω To Gnd R_{L2} = 300Ω To V_{CC}		60	80	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address	Output			60	80	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Output			28	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable	Output			28	40	ns

Programming Procedure

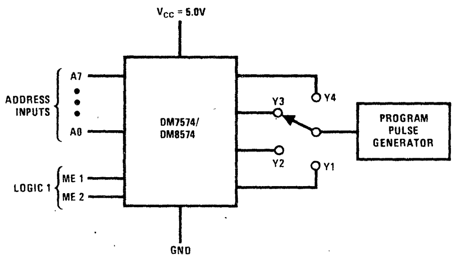
The DM7573/DM8573 is manufactured such that the outputs are high for all addresses. To program a logic zero (low output level), the following procedure should be followed:

1. Apply a V_{CC} voltage of 5.0V and select the word to be programmed using address inputs A7 – A0.
2. Apply a high level (logic 1) to either or both of the ENABLE inputs (Pins 13 and 14).
3. Apply a programming pulse to the output where a low level is desired. The voltage should be 23V to 25V; the current should be limited to 70 mA. Apply the pulse as shown in the diagram. A reduction in current of approximately 15 mA indicates the bit is programmed.
4. To verify that the bit has been programmed, apply a logic zero to both of the enable inputs and check for a low level on the programmed output.
5. Advance to the next output and/or word, programming only one bit at a time.

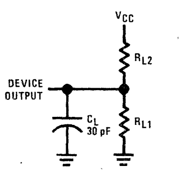
PROGRAMMING PULSE



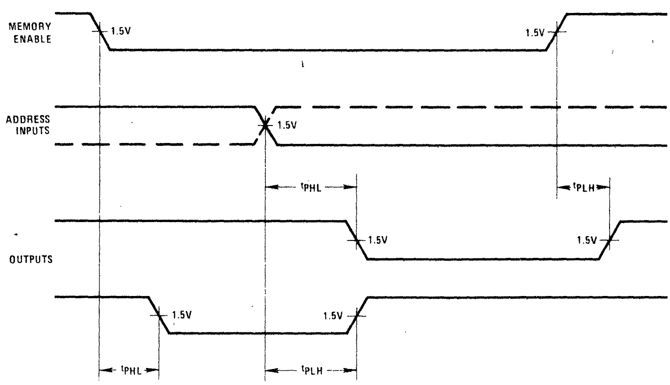
PROGRAMMING CONNECTIONS



AC Test Circuit and Switching Time Waveforms



C_L includes probe and jig capacitance.



Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns; $t_f \leq 10$ ns, PRR = 1 MHz, PDC = 50%, Amplitude = 3.0V, and $Z_0 = 50\Omega$.

TRI-STATE 1024-Bit Field Programmable Read Only Memories

General Description

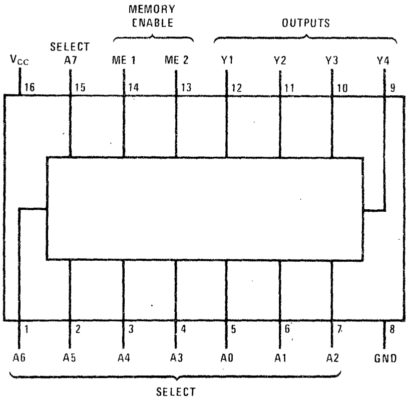
The DM7574/DM8574 is a field-programmable read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided; when either or both of the enable inputs are taken to a high state, all the outputs go to the high impedance state. A logical "1" has been built into each bit location. A logical "0" can be programmed into any bit by selecting the proper word, disabling the chip, and applying a programming pulse to the proper output.

An additional feature of the DM7574/DM8574 is that its outputs can be tested in the logical "0" state without permanently programming the memory. In order to place all outputs in the logical "0" state, a 10V level is applied to the most significant address input, Pin 15. This feature will allow a much more complete test to be made before a part is shipped, thus minimizing customer problems.

Features

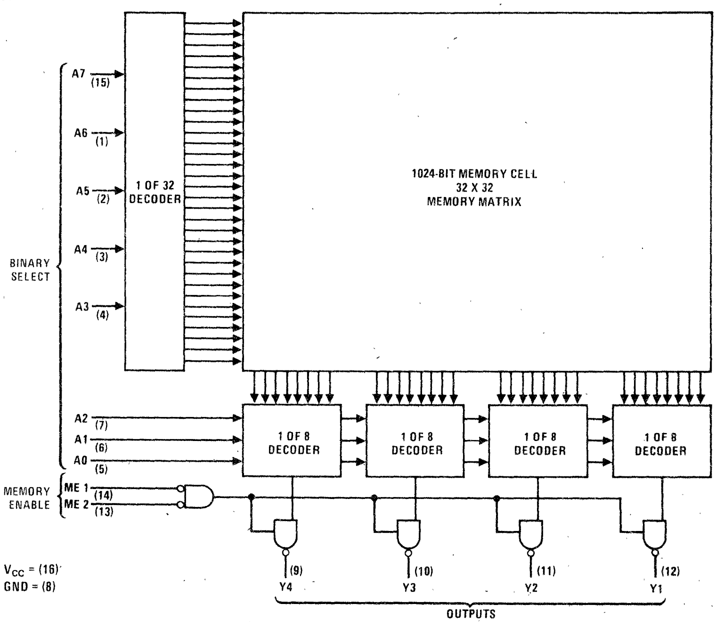
- Pin compatible with SN54187/SN74187
- Outputs can be fully tested before programming
- Typical power dissipation 400 mW
- Propagation delay 60 ns

Connection Diagram



7574(J); 8574(J), (N)

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM75/85 74 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current		DM75			−2.0	mA
			DM85			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Max, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4			V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−15		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			80	110	mA

Notes

(1) All typical values are at V_{CC} = 5V and T_A = 25°C

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

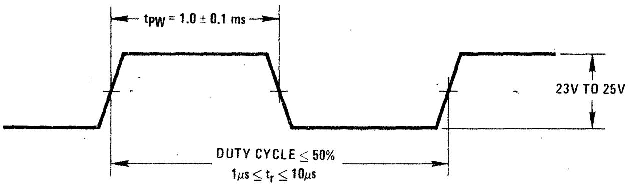
PARAMETER		FROM	TO	CONDITIONS	DM75/85 74 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address	Output	C_L = 30 pF, R_L = 600Ω		60	80	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address	Output			60	80	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Output			28	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable	Output			28	40	ns

Programming Procedure

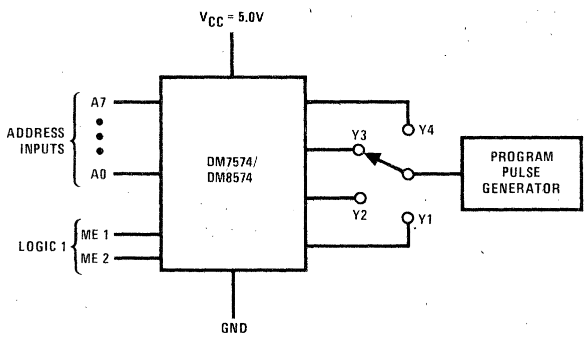
The DM7574/DM8574 is manufactured such that the outputs are high for all addresses. To program a logic zero (low output level), the following procedure should be followed:

1. Apply a V_{CC} voltage of 5.0V and select the word to be programmed using address inputs A7 – A0.
2. Apply a high level (logic 1) to either or both of the ENABLE inputs (Pins 13 and 14).
3. Apply a programming pulse to the output where a low level is desired. The voltage should be 23V to 25V; the current should be limited to 70 mA. Apply the pulse as shown in the diagram. A reduction in current of approximately 15 mA indicates the bit is programmed.
4. To verify that the bit has been programmed, apply a logic zero to both of the enable inputs and check for a low level on the programmed output.
5. Advance to the next output and/or word, programming only one bit at a time.

PROGRAMMING PULSE



PROGRAMMING CONNECTIONS



Programmable Logic Arrays

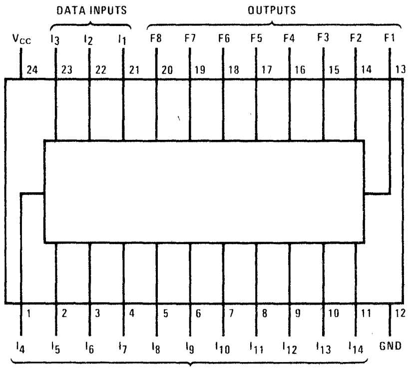
General Description

The DM7575/DM8575 and DM7576/DM8576 are mask-programmable logic arrays designed for use in applications where random logic is required. The devices have fourteen data inputs and eight outputs. Each output provides a sum of product terms where each product term can contain any combination of 14 variables or their complements. The total number of product terms which can be provided is 96. Any product term which is repeated is counted only once. Since some functions are more easily represented in their inverted form, an option is provided to allow for either the true or complement of the function on each output. The products are particularly useful in providing control logic for digital systems. The DM7575/DM8575 has a conventional totem-pole output whereas the DM7576/DM8576 is provided with a passive pullup output. This latter configuration is useful in expanding functions by connection of outputs of different packages.

Features

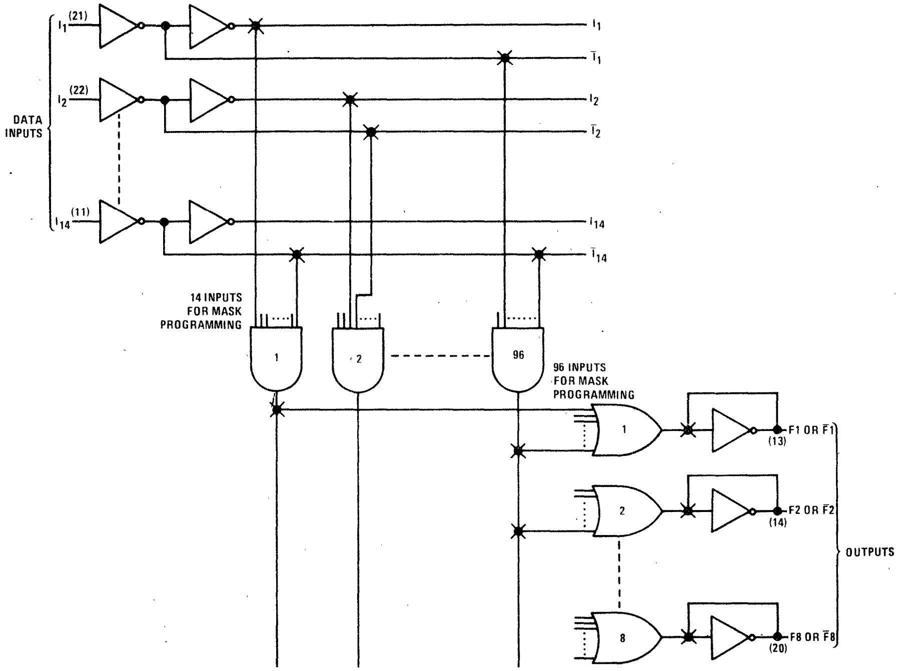
- A 2^{14}-by-8 (128k) bit memory would be needed to provide equivalent function
- Typical delay 90 ns
- Typical power dissipation 550 mW

Connection Diagram



7575(J); 8575(J), (N); 7576(J); 8576(J), (N)

Logic Diagram



NOTE: ✖ IS A MASK-PROGRAMMABLE CONNECTION

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM75/85 75, 76 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current		DM75/8575			−800	µA
		V_{OH} = 5.5V	DM75/8576			100	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	DM75/8575	2.4			V
			DM75/8576			5.5	
I_{OL}	Low Level Output Current					12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 12 mA				0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM75	−20		−55	mA
			DM85	-18		−55	
I_{CC}	Supply Current	V_{CC} = Max			110	170	mA

Notes

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM75/85 75, 76 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 50 pF, R_L = 400Ω		80	150	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output			100	150	ns

PLA Programming Information

Information to program the PLA can be supplied in one of two formats:

1. Punched 80-column cards
2. The applicable section of this data sheet (manual entry of information).

PUNCHED CARDS

CARD 1: (Used to determine whether outputs are presented in their true or inverted form. If this card is not used it is assumed that all eight outputs are true.)

Col. 1-6: DM7575 or DM8575 or DM7576 or DM8576.

PLA Programming Information (Continued)

Col. 7-9: (Blank)

Col 10-17: Output Data. Outputs are F8 (most significant) to F1 (least significant). All eight outputs must be specified.

A 'T' in an output location indicates that the output is true.

A 'C' in an output location indicates that the output is complemented (inverted).

Col. 18-39: (Blank)

Col. 40-75: This space is reserved for any unique letters/numbers desired by the customer (special part number, program number, etc.). However the exact combination of characters must appear on all cards, associated with that particular device.

Col. 76-78: (Blank)

Col. 79-80: 00

CARDS 2-97: Term Data Cards. Used to specify the input and output conditions.

Col. 1-6: DM7575 or DM8575 or DM7576 or DM8576.

Col. 7-9: (Blank)

Col. 10-17: Output Connections. Outputs are F8, (most significant) to F1 (least significant). This field describes the outputs on which the product term appears.

A '+' in one of the eight output locations indicates that the term described by the card is one of the "OR" terms in that output.

A '(blank)' in one of the eight output locations indicates that the term described by the card is not one of the "OR" terms in that output.

(Care should be exercised in punching this particular field; since in most cases, unless a product term is repeated, this field will appear as one '+' and seven blanks.)

Col. 18: (Blank)

Col. 19: = (equal sign)

Col. 20: (Blank)

Col. 21-34: Input Data. Inputs are I13 (most significant) to I0 (least significant).

An 'H' in one of the fourteen locations indicates that input appears in the high state in the output term.

An 'L' in one of the fourteen input locations indicates that input appears in the low state in the output term.

An 'X' in one of the fourteen input locations indicates that input does not appear in the output term.

Col. 35-39: (Blank)

Col. 40-75: This space is reserved for any unique letter/number desired by the customer (special part number, program number, etc.). However the exact combination of characters must appear on all cards, associated with that particular device. The purpose of this section is to prevent mixing of cards.

Col. 76-78: (Blank)

Col. 79-80: Product Term Number 01 to 96. (All 96 cards need not be used.) Zero in column 79 may be suppressed.

MANUAL ENTRY

The matrix-blank shown in this data sheet can be used in lieu of punched cards to submit information for programming the PLA.

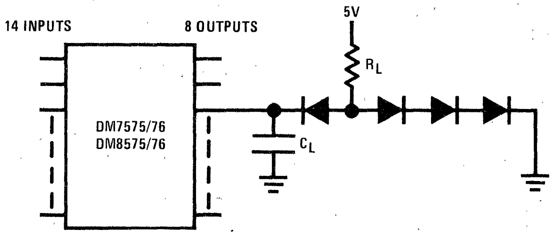
INSTRUCTIONS

1. Circle the appropriate part number. In the event a catalog part is not being purchased, circle the closest catalog part number. If an electrical screen is required between the military and commercial devices, the military designation should be circled.
2. Customer should write the name of his company.
3. Enter the total number of unique product terms found in all eight outputs. Repeated terms count only once.
4. Output Inverter Option. Under the appropriate output designation specify a 'T' when the high (true) level is desired on the output for the given input conditions. Specify a 'C' if the complement is needed.
5. Matrix
   a. Input data. This block is used to describe what comprises each of the 96 (maximum) product terms. In each row, opposite the appropriate Product Term number, information on the fourteen Input Data locations is entered. Information must be entered on all 14 inputs.
      1). Enter an "H" under the appropriate input designation if that particular input appears in the product term as a high (true) level.
      2). Enter an "L" under the appropriate input designation if that particular input appears in the product term as a low (complemented) level.
      3). Enter an "X" under the appropriate input designation if that particular input does not appear in the product term.

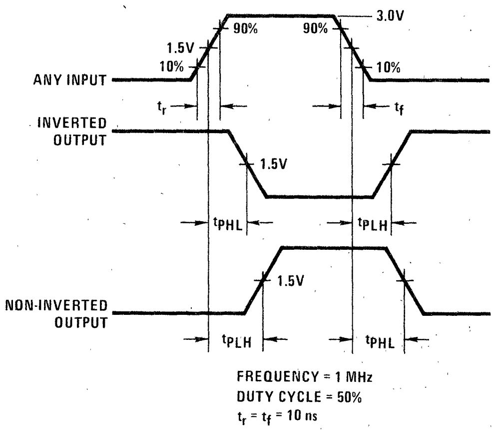
      If less than 96 product terms are used leave all spaces for the unused terms blank.

   b. Output Data. This block is used to describe the outputs on which the product terms appear.
      1). Enter a '+' under the appropriate output designation if the product term is contained in that output's expression.
      2). Leave a location blank if the product term is not contained in that output's expression.

AC Test Circuit



Switching Time Waveforms



Truth Table/Order Blank

1. PART NO. — (DM7575, DM8575, DM7576, DM8576)

2. CUSTOMER IDENTIFICATION —

3. TOTAL NO. OF UNIQUE PRODUCT TERMS USED —
(Repeated Terms Count Only Once)

F8	F7	F6	F5	F4	F3	F2	F1

4. OUTPUT INVERTER OPTION

5. MATRIX

PRODUCT TERM	INPUT DATA															OUTPUT DATA								
		I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F8	F7	F6	F5	F4	F3	F2	F1	
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Truth Table/Order Blank (Continued)

PRODUCT TERM	INPUT DATA															OUTPUT DATA								
		I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F8	F7	F6	F5	F4	F3	F2	F1	
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256-Bit Programmable Read Only Memories

General Description

The DM7577/DM8577 is a field-programmable, 256-bit, read only memory organized as 32 words of 8 bits each. This monolithic, high-speed, transistor-transistor-logic (TTL) memory array is addressed in 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain high. The organization is expandable to 1,856 words of n-bits with no additional output buffering.

The address of an 8-bit word is accomplished through the buffered binary select inputs in coincidence with a low logic level at the enable input. Where multiple DM7577/DM8577 devices are used in a memory system, the enable input allows easy decoding of additional address bits.

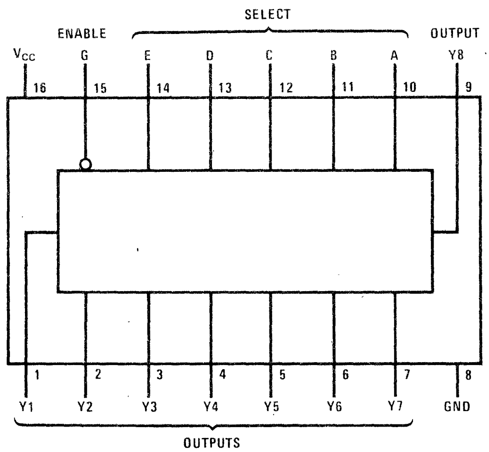
Data can be electronically programmed, as desired, at any of the 256-bit locations of the DM7577/DM8577 in accordance with the programming procedure specified. Prior to programming, the memory contains a high-logic-level output condition at all 256 bit locations. The programming procedure open-circuits nichrome links which results in a low-logic-level output at selected locations. The procedure is irreversible and, once altered, the output for that bit is permanently programmed to provide a low logic level. Outputs never having been altered may later be programmed to supply a low-level output. Operation of the unit within the recommended operating conditions will not alter the memory content.

The mask-programmable DM5488/DM7488 can be used to replace the DM7577/DM8577 as they are functionally and mechanically identical.

Features

- Field programmable for custom or prototype memories
- Mask-programmable DM5488/DM7488 is a direct replacement for the DM7577/DM8577
- Typical access time 35 ns
- Organized as 32 words of 8-bits each
- Ideal for microprogramming and code converters
- Open-collector outputs are easily expanded
- Fully-decoded buffered inputs
- Fully compatible with most TTL and DTL circuits
- Pin compatible with SN74188A

Connection Diagram



7577(J); 8577(J), (N)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM75/85 77 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, V_{OH} = 5.5V			100	μA
I_{OL}	Low Level Output Current				12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 12 mA			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max(2)		50	80	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max(3)		82	110	mA

Notes

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) I_{CCH} is measured with all inputs at 4.5V, all outputs open.

(3) I_{CCL} is measured with enable input grounded, all other inputs at 4.5V, and all outputs open. The typical value shown is for the worst-case condition of all eight outputs low at one time. This condition may not be possible after the device has been programmed.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM75/85 77 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Any	C_L = 30 pF to GND R_{L1} = 400Ω to V_{CC} R_{L2} = 600Ω to GND		22	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable	Any			15	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Any			35	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Any			35	50	ns

Programming Procedure

1. Apply steady-state supply voltage (V_{CC} = 5.0V, GND = 0V) and address the word to be programmed with specified input voltages.

2. Disable the outputs by applying a high logic level to the enable input.

3. Only one bit location is programmed at a time. Open circuit all outputs except the one to be programmed as a low logic level.

4. Apply the specified programming pulse to the output to be programmed. The recommended pulse width is 1.0 ms.

The bit programmed may be verified by checking the output for a low logic level after the enable input reaches a low logic level.

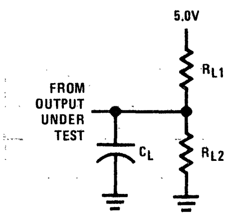
5. Repeat steps 2 through 4 for each output of this address to be programmed as a low level.

6. Advance to next address location and repeat steps 2 through 5.

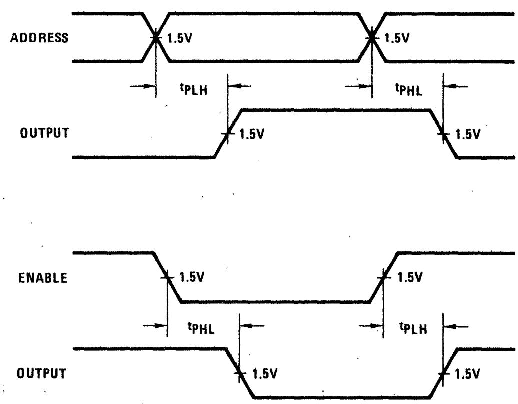
Recommended Conditions for Programming

CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}		5.0		5.5	V
Input Voltage	Low Level	0		0.5	V
	High Level	2.4		5.0	V
Programming Pulse Amplitude		20		22	V
Programming Pulse Rise Time		1.0	5.0	10	μs
Programming Pulse Current Limit		100		200	mA
Programming Pulse Width		10	20	50	ms
Case Temperature		25		75	°C

AC Test Circuit and Switching Time Waveforms



C_L includes probe and jig capacitance.



Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, PDC = 50%, Amplitude = 3.0V, and $Z_0 = 50\Omega$.

TRI-STATE 256-Bit Programmable Read Only Memories

General Description

The DM7578/DM8578 is a field-programmable, 256-bit, read only memory organized as 32 words of 8 bits each. This monolithic, high-speed, transistor-transistor-logic (TTL) memory array is addressed in 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain in the high impedance (Z) state.

The address of an 8-bit word is accomplished through the buffered binary select inputs in coincidence with a low logic level at the enable input. Where multiple DM7578/DM8578 devices are used in a memory system, the enable input allows easy decoding of additional address bits. The TRI-STATE outputs eliminate the need for external pull-up resistors, and provide good capacitance drive capability.

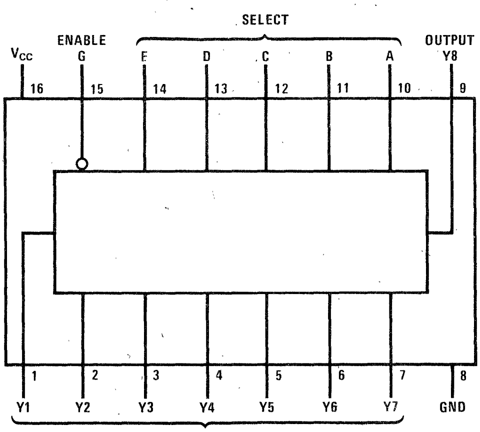
Data can be electronically programmed, as desired, at any of the 256-bit locations of the DM7578/DM8578 in accordance with the programming procedure specified. Prior to programming, the memory contains a high-logic-level output condition at all 256 bit locations. The programming procedure open-circuits nichrome links which results in a low-logic-level output at selected locations. The procedure is irreversible and, once altered, the output for that bit is permanently programmed to provide a low logic level. Outputs never having been altered may later be programmed to supply a low-level output. Operation of the unit within the recommended operating conditions will not alter the memory content.

The mask-programmable DM7598/DM8598 can be used to replace the DM7578/DM8578 as they are functionally and mechanically identical.

Features

- Field programmable for custom or prototype memories
- Mask-programmable DM7598/DM8598 is a direct replacement for the DM7578/DM8578.
- Typical access time 35 ns
- Organized as 32 words of 8-bits each
- Ideal for microprogramming and code converters
- TRI-STATE outputs are easily expanded
- Fully-decoded buffered inputs
- Fully compatible with most TTL and DTL circuits
- Pin compatible with SN74188A

Connection Diagram



7578(J); 8578(J), (N)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM75/85 78 MIN	DM75/85 78 TYP(1)	DM75/85 78 MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current		DM75			−2.0	mA
			DM85			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4			V
I_{OL}	Low Level Output Current					12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 12 mA				0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max V_{IH} = 2.0V	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			82	110	mA

Notes

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

(3) I_{CC} is measured with all inputs at 4.5V, all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM75/85 78 MIN	DM75/85 78 TYP	DM75/85 78 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Any	C_L = 50 pF R_L = 400Ω		35	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Any	C_L = 50 pF R_L = 400Ω		35	50	ns
t_{ZH}	Output Enable Time to High Level	Enable	Any	C_L = 50 pF R_L = 400Ω		19	35	ns
t_{ZL}	Output Enable Time to Low Level	Enable	Any	C_L = 50 pF R_L = 400Ω		17	35	ns
t_{HZ}	Output Disable Time from High Level	Enable	Any	C_L = 5 pF R_L = 400Ω		11	35	ns
t_{LZ}	Output Disable Time from Low Level	Enable	Any	C_L = 5 pF R_L = 400Ω		21	35	ns

Programming Procedure

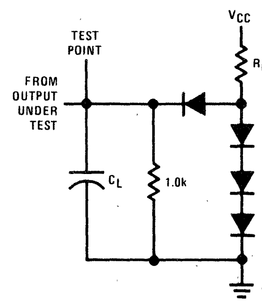
1. Apply steady-state supply voltage (V_{CC} = 5.0V, GND = 0V) and address the word to be programmed with specified input voltages.
2. Disable the outputs by applying a high logic level to the enable input.
3. Only one bit location is programmed at a time. Open circuit all outputs except the one to be programmed as a low logic level.
4. Apply the specified programming pulse to the output to be programmed. The recommended pulse width is 1.0 ms.

   The bit programmed may be verified by checking the output for a low logic level after the enable input reaches a low logic level.
5. Repeat steps 2 through 4 for each output of this address to be programmed as a low level.
6. Advance to next address location and repeat steps 2 through 5.

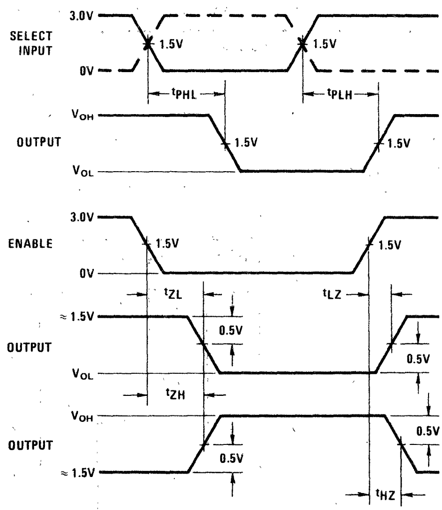
Recommended Conditions for Programming

CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		5		5.5	V
Input Voltage	Low Level	0		0.5	V
	High Level	2.4		5	V
Programming Pulse Amplitude		20		22	V
Programming Pulse Rise Time		1	5	10	μs
Programming Pulse Current Limit		100		200	mA
Programming Pulse Width		10	1.0	50	ms
Case Temperature		25		75	°C

AC Test Circuit and Switching Time Waveforms



C_L includes probe and jig capacitance.
All diodes are 1N3064.



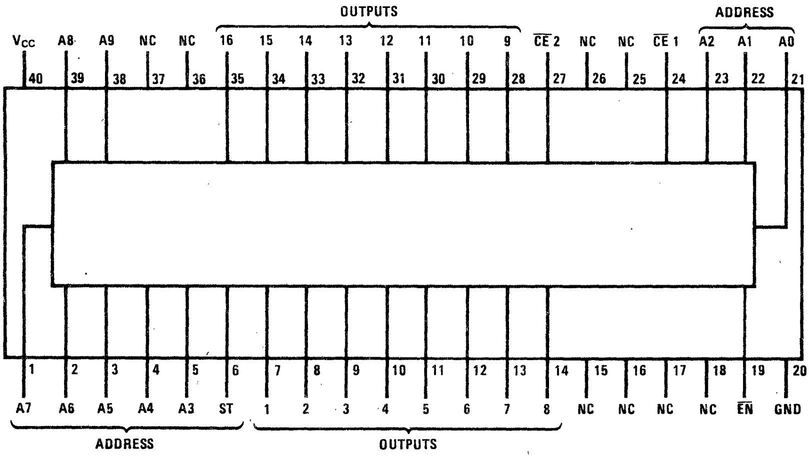
Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, PDC = 50%, Amplitude = 3.0V and $Z_O = 50\Omega$

TRI-STATE 16K Read Only Memories

General Description

The DM8581 is a 16,384-bit, bipolar, mask-programmable ROM organized as 1024, 16-bit words. Ten address inputs select the desired one-of-1024 words. All ten address inputs, and two of the three enable inputs have a latch feature. The latch function is controlled by the strobe input. The three enable lines are used to either enable or disable the circuit. TRI-STATE outputs allow for expansion to greater number of words without sacrifice in speed as would be the case with open-collector outputs.

Connection Diagram



8581(D), (N)

Truth Table

$\overline{CE}$ 1 t	$\overline{CE}$ 2 t	ST t	$\overline{CE}$ 1 t+1	$\overline{CE}$ 2 t+1	$\overline{EN}$ t+1	ST t+1	OUTPUT t+1
X	X	X	L	L	L	H	Read stored data for add inputs at t+1
X	X	X	H	X	X	H	Hi-Z
X	X	X	X	H	X	H	Hi-Z
X	X	X	X	X	H	H	Hi-Z
L	L	H	X	X	L	L	Read stored data for add inputs at t
H	X	H	X	X	X	L	Hi-Z
X	H	H	X	X	X	L	Hi-Z
X	X	X	X	X	H	L	Hi-Z

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM8581 MIN	DM8581 TYP(1)	DM8581 MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −400μA		2.4			V
I_{OL}	Low Level Output Current					6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 6 mA				0.45	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−15		−50	mA
I_{CC}	Supply Current	V_{CC} = Max			115	160	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

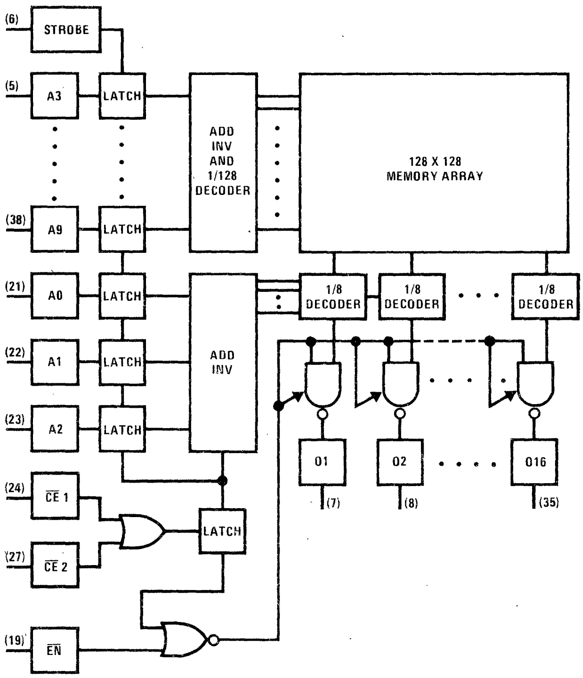
(2) Not more than one output should be shorted at a time.

(3) Tentative data

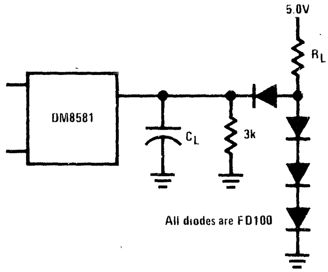
Switching Characteristics

	PARAMETER	FROM	TO	CONDITIONS	DM8581 MIN	DM8581 TYP	DM8581 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address	Output	C_L = 50 pF, R_L = 600Ω		200	450	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address	Output	C_L = 50 pF, R_L = 600Ω		150	450	ns
t_{ZH}	Output Enable Time to High Level			C_L = 50 pF, R_L = 600Ω		40	80	ns
t_{ZL}	Output Enable Time to Low Level			C_L = 50 pF, R_L = 600Ω		70	165	ns
t_S	Address, Chip Enable ($\overline{CE}$) Set-Up Time			C_L = 50 pF, R_L = 600Ω	30	10		ns
t_H	Address, Chip Enable ($\overline{CE}$) Hold Time			C_L = 50 pF, R_L = 600Ω	30	10		ns
t_{HZ}	Output Disable Time from High Level			C_L = 5 pF, R_L = 600Ω		20	50	ns
t_{LZ}	Output Disable Time from Low Level			C_L = 5 pF, R_L = 600Ω		40	60	ns
t_W	Minimum Strobe Pulse Width				40	20		ns
t_{ST}	Strobe Access Time					250	450	ns

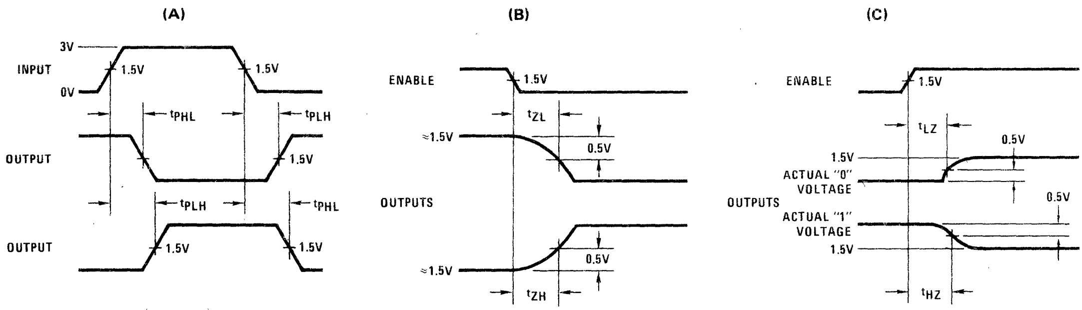
Logic Diagram

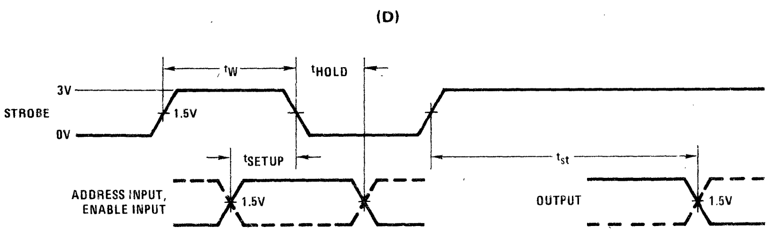


AC Test Circuit



Switching Time Waveforms





f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
Duty Cycle = 50%

8-Bit Parallel In/Serial Out Shift Registers

General Description

These are 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

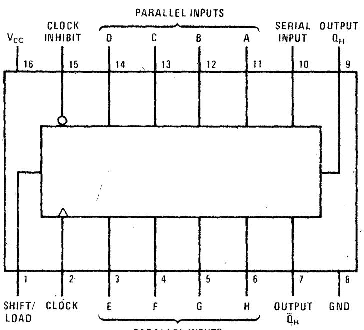
Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion

TYPE	TYPICAL FREQUENCY	TYPICAL POWER DISSIPATION
90	20 MHz	200 mW
L90	14 MHz	30 mW

Connection Diagram



7590(J), (W); 8590(J), (N), (W); 76L90/86L90(J), (N), (W)

Truth Table

INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

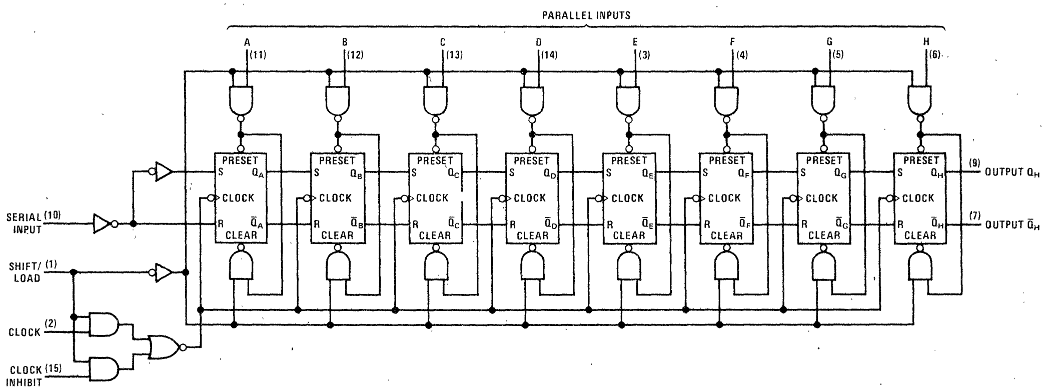
↑ = Transition from low-to-high level

a . . . h = The level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM75/85 90 MIN	DM75/85 90 TYP(1)	DM75/85 90 MAX	DM76L/86L L90 MIN	DM76L/86L L90 TYP(1)	DM76L/86L L90 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			N/A	V
I_{OH}	High Level Output Current					−800			−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current		DM75, DM76			16			2	mA
			DM85, DM86			16			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OL} = Max	DM75, DM76		0.2	0.4			0.3	V
			DM85, DM86		0.2	0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			0.1	mA
I_{IH}	High Level Input Current — Load Input	V_{CC} = Max, V_I = 2.4V				80			30	μA
	High Level Input Current — Other Inputs	V_{CC} = Max, V_I = 2.4V				40			10	μA
I_{IL}	Low Level Input Current — Load Input	V_{CC} = Max,	V_I = 0.3V (DM76/86)			−3.2			−0.54	mA
	Low Level Input Current — Other Inputs	V_{CC} = Max,	V_I = 0.4V (DM75/85)			−1.6			−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM75, DM76	−20		−55	−3	−9	−15	mA
			DM85, DM86	−18		−55	−3	−9	−15	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			40	63			9.5	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

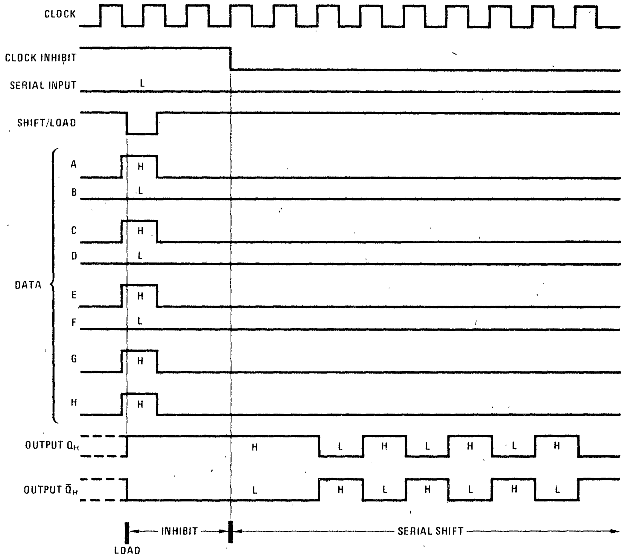
(3) With the outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

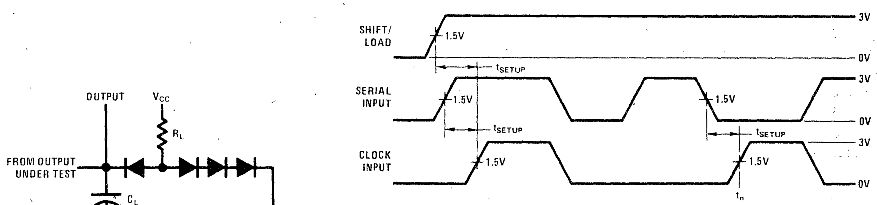
	PARAMETER	FROM (INPUT)	TO (OUTPUT)	DM75/85 90 CONDITIONS	MIN	TYP	MAX	DM76L/86L L90 CONDITIONS	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency			C_L = 15 pF, R_L = 400Ω	14	20			6	14		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Load	Any	C_L = 15 pF, R_L = 400Ω		34	50	C_L = 50 pF, R_L = 4 kΩ		44	88	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Load	Any			42	60			62	124	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Any			26	40			35	70	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock	Any			35	50			50	100	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	H	Q_H			25	40			33	66	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	H	Q_H			36	50			56	112	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	H	$\overline{Q}_H$			25	40			33	66	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	H	$\overline{Q}_H$			36	50			56	112	ns
$t_{W(CLOCK)}$	Width of Clock Input Pulse				35	25			100			ns
$t_{W(LOAD)}$	Width of Load Input Pulse				35	24			100			ns
t_{SETUP}	Parallel Input Setup Time				25	10			44	22		ns
t_{SETUP}	Serial Input Setup Time				40	23			44	22		ns
t_{HOLD}	Hold Time at Any Input				5				10			ns

Timing Diagram

TYPICAL SHIFT, LOAD AND INHIBIT SEQUENCES



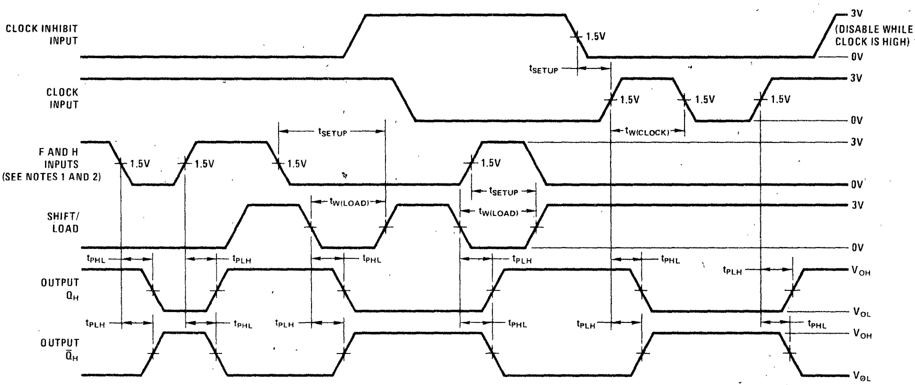
AC Test Circuit and Switching Time Waveforms



Notes

(1) The eight data inputs and the clock inhibit input are low. Results are monitored at output Q_H at t_{n+7}.

(2) The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{OUT} \approx 50\Omega$.



Notes

(1) The remaining six data inputs and the serial input are low.

(2) Prior to test, high level data is loaded into H input.

(3) The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$. When testing f_{MAX}, vary clock PRR.

4096-Bit Read Only Memories

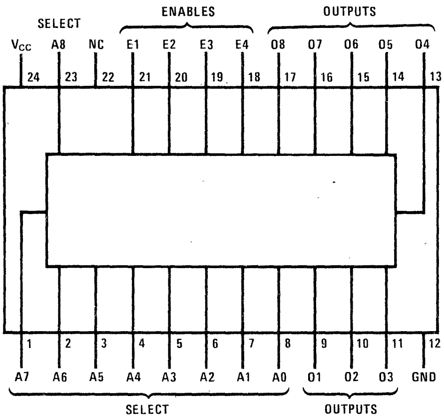
General Description

The DM7595/DM8595 and DM7795/DM8795 are 4096-bit, bipolar, mask-programmable ROMs organized as 512 eight-bit words. Nine address inputs select the desired one-of-512 words. Four enable lines are used to either enable or disable the circuit. The two devices differ in the enable logic. Truth tables and logic diagrams for each device are shown below. Open collector outputs allow for expansion to a greater number of words.

Features

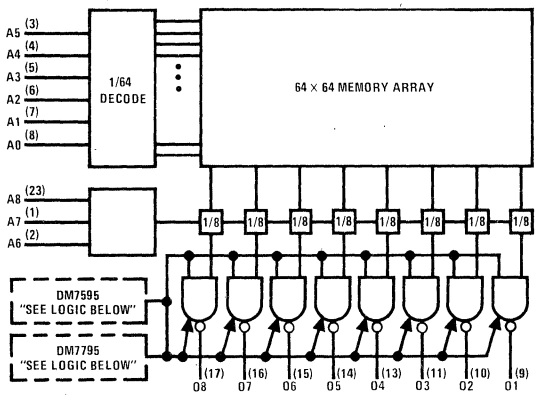
- Series 54/74 specification compatibility
- Pin compatible with Monolithic Memories 5240/6240
- Typical address time 80 ns
- Open collector outputs

Connection Diagram



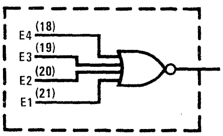
7595(J); 8595(J), (N);
7795(J); 8795(J), (N)

Logic Diagram



Logic Diagrams and Truth Tables for Enable Circuitry

DM7595/DM8595

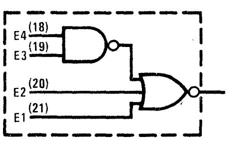


DM7595/DM8595

E1	E2	E3	E4	OUTPUT
L	L	L	L	Read Stored Data
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

X = Don't Care
ENABLE = $\overline{E1} \cdot \overline{E2} \cdot \overline{E3} \cdot \overline{E4}$

DM7795/DM8795



DM7795/DM8795

E1	E2	E3	E4	OUTPUT
L	L	H	H	Read Stored Data
H	X	X	X	H
X	H	X	X	H
X	X	L	X	H
X	X	X	L	H

X = Don't Care
ENABLE = $\overline{E1} \cdot \overline{E2} \cdot E3 \cdot E4$

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM75/85, DM77/87 95 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Max, V_O = 5.5V			100	μA
I_{OL}	Low Level Output Current				12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_O = 12 mA			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.0	mA
I_{CC}	Supply Current	V_{CC} = Max		103	158	mA

Notes
(1) All typical values are at V_{CC} = 5V at T_A = 25°C.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		PARAMETER CONDITIONS	TEST CONDITIONS	DM7595,DM7795 MIN	TYP	MAX	DM8595,DM8795 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low to High Level Output	Access Time from Address	C_L = 30 pF R_L = 400Ω		80	150		80	120	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Access Time from Address			80	150		80	120	ns
t_{PLH}	Output Disable Time to High Level	Disable Time from Memory Enables			60	120		60	90	ns
t_{PHL}	Output Enable Time to Low Level	Access Times from Memory Enables			60	120		60	90	ns

80-Column Card Program Data Format

Col. 1-3: 3 Character ID code (any 3 alpha-numeric characters). Must be the same on all cards associated with a particular pattern, but different for the ID code used on other patterns. The purpose of this code is to prevent mixing of cards.

Col. 4: (Blank)

Col. 5-12: Word Data. Order is 08 (most significant) to 01 (least significant). *Note 1.* Characters—For TTL high level are: H or 1. Characters—For TTL low are L or 0. "Don't Care" is X.

Col. 13: (Blank)

Col. 14-21: Word Data—same format as 5-12.

Col. 22: (Blank)

Col. 23-30: Word Data

Col. 31: (Blank)

Col. 32-39: Word Data

Col. 40: (Blank)

Col. 41-48: Word Data

Col. 49: (Blank)

Col. 50-57: Word Data

Col. 58: (Blank)

Col. 59-66: Word Data

Col. 67: (Blank)

Col. 68-75: Word Data

Col. 76-78: (Blank)

Col. 79-80: Card sequence number. 1 to 64. Leading zeros may be punched or suppressed. *(Note 2)*

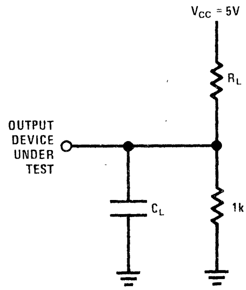
Notes

(1) The words are listed in sequence beginning on the first card with the word associated with address 0 and ending on the last card with the word associated with address 511. Address input A8 is the most significant; A0, the least significant.

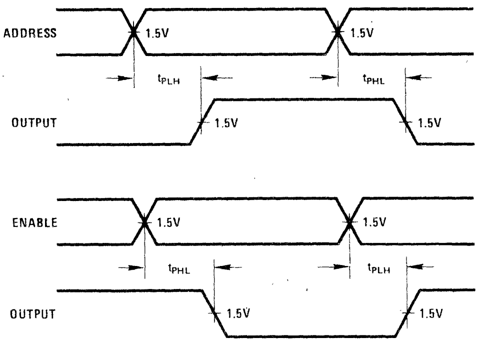
(2) Card sequence numbers reference a specific group of 8 words, i.e.:

Card 01: Word address 0 to 7
Card 02: Word address 8 to 15
Card 03: Word address 16 to 23
. .
. .
Card 64: Word address 504 to 511.

AC Test Circuit



Switching Time Waveforms



Input waveforms are supplied by pulse generators having the following characteristics: $t \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, Amplitude = 3.0V, PDC = 50%, and Z_O = 50Ω.

TRI-STATE 4096-Bit Read Only Memories

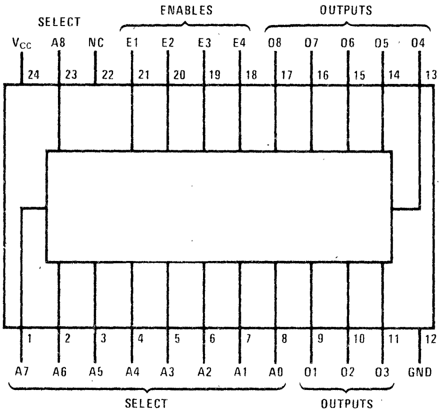
General Description

The DM7596/DM8596 and DM7796/DM8796 are 4096-bit, bipolar, mask-programmable ROMs organized as 512 eight-bit words. Nine address inputs select the desired one-of-512 words. Four enable lines are used to either enable or disable the circuit. The two devices differ in the enable logic. Truth tables and logic diagrams for each device are shown below. TRI-STATE outputs allow for expansion to greater numbers of words without sacrifice in speed as would be the case with open-collector outputs.

Features

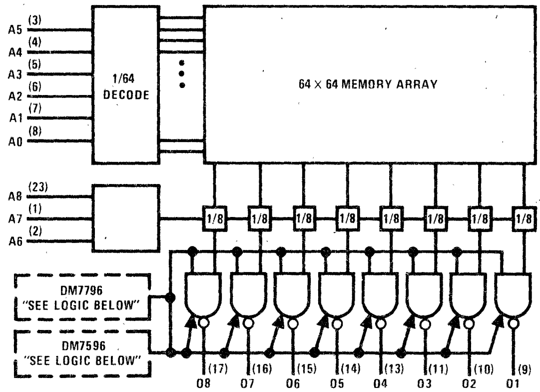
- Series 54/74 specification compatibility
- Pin compatible with Monolithic Memories MM5241/MM6241
- Typical address time 80 ns
- TRI-STATE outputs

Connection Diagram



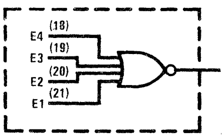
7596(J); 8596(J), (N);
7796(J); 8796(J), (N)

Logic Diagram



Logic Diagrams and Truth Tables for Enable Circuitry

DM7596/DM8596



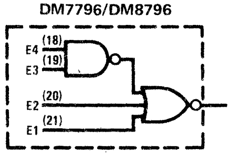
DM7596/DM8596

E1	E2	E3	E4	OUTPUT
L	L	L	L	Read Stored Data
H	X	X	X	Hi - Z
X	H	X	X	Hi - Z
X	X	H	X	Hi - Z
X	X	X	H	Hi - Z

X = Don't Care

ENABLE = $\overline{E1} \cdot \overline{E2} \cdot \overline{E3} \cdot \overline{E4}$

DM7796/DM8796



DM7796/DM8796

E1	E2	E3	E4	OUTPUT
L	L	H	H	Read Stored Data
H	X	X	X	Hi - Z
X	H	X	X	Hi - Z
X	X	L	X	Hi - Z
X	X	X	L	Hi - Z

X = Don't Care

ENABLE = $\overline{E1} \cdot \overline{E2} \cdot E3 \cdot E4$

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM75/85, DM77/87 96 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_O = −2 mA		2.4			V
I_{OL}	Low Level Output Current					12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_O = 12 mA				0.4	V
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Min, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max(2)		−15		−70	mA
I_{CC}	Supply Current	V_{CC} = Max, Inputs Grounded			106	170	mA

Notes

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		PARAMETER CONDITIONS	TEST CONDITIONS	DM7596,DM7796 MIN	TYP	MAX	DM8596,DM8796 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low to High Level Output	Access Time from Address	C_L = 50 pF, R_L = 400Ω		80	150		80	120	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Access Time from Address			80	150		80	120	ns
t_{ZH}	Output Enable Time to High Level	Access Times from Memory Enables			40	120		40	90	ns
t_{ZL}	Output Enable Time to Low Level	Access Times from Memory Enables			60	120		60	90	ns
t_{HZ}	Output Disable Time from High Level	Disable Times from Memory Enables	C_L = 5.0 pF, R_L = 400Ω		20	70		20	50	ns
t_{LZ}	Output Disable Time from Low Level	Disable Times from Memory Enables			25	70		25	50	ns

80-Column Card Program Data Format

Col. 1-3: 3 Character ID code (any 3 alpha-numeric characters). Must be the same on all cards associated with a particular pattern, but different for the ID code used on other patterns. The purpose of this code is to prevent mixing of cards.

Col. 4: (Blank)

Col. 5-12: Word Data. Order is 08 (most significant) to 01 (least significant). Note 1. Characters—For TTL high level are: H or 1. Characters—For TTL low are L or 0. "Don't Care" is X.

Col. 13: (Blank)

Col. 14-21: Word Data—same format as 5-12.

Col. 22: (Blank)

Col. 23–30: Word Data

Col. 31: (Blank)

Col. 32-39: Word Data

Col. 40: (Blank)

Col. 41-48: Word Data

Col. 49: (Blank)

Col. 50-57: Word Data

Col. 58: (Blank)

Col. 59-66: Word Data

Col. 67: (Blank)

Col. 68-75: Word Data

Col. 76-78: (Blank)

Col. 79-80: Card sequence number. 1 to 64. Leading zeros may be punched or suppressed. (Note 2)

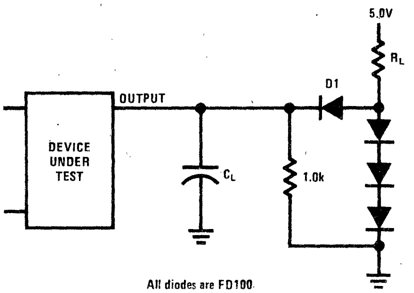
Notes

(1) The words are listed in sequence beginning on the first card with the word associated with address 0 and ending on the last card with the word associated with address 511. Address input A8 is the most significant; A0, the least significant.

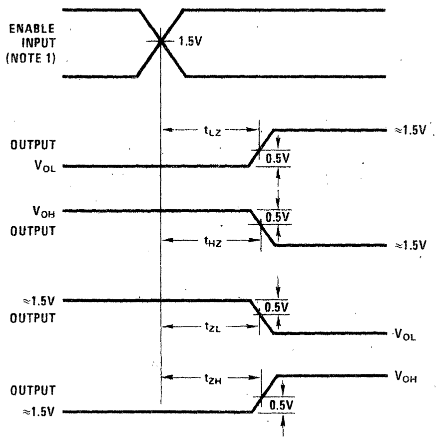
(2) Card sequence numbers reference a specific group of 8 words, i.e.:

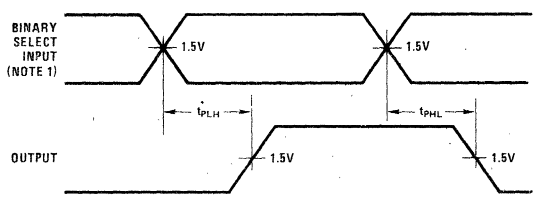
Card 01: Word address 0 to 7
Card 02: Word address 8 to 15
Card 03: Word address 16 to 23
. .
. .
. .
Card 64: Word address 504 to 511

AC Test Circuit and Switching Time Waveforms



All diodes are FD100





Note 1: Input waveforms are supplied by pulse generators having the following characteristics:
$t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, PDC = 50%, Amplitude = 3.0V, and $Z_O = 50\Omega$.

TRI-STATE 1024-Bit Read Only Memories

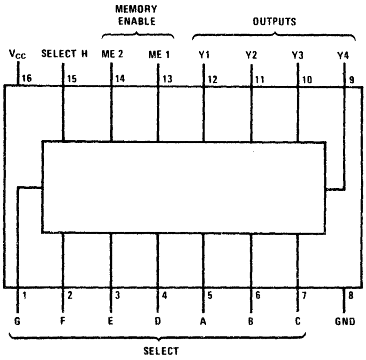
General Description

The DM7597/DM8597 is a custom-programmed read only memory organized as 256 4-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided, which when mask-programmed in one of three options described will cause all four outptus to either read the normal memory contents or go to the "high impedance" state. In this state both the upper and lower output transistors are turned "OFF." The outputs may therefore be paralleled to increase word capacity; since in the high-impedance state they present only a minimal load to the active output.

Features

- TRI-STATE outputs
- Pin compatible with DM54187/DM74187
- 35 ns typical delay from address to output
- Can be expanded to 32,768 4-bit words by simple paralleling of outputs
- Programmable memory enable inputs

Connection Diagram



7597(J); 8597(J), (N)

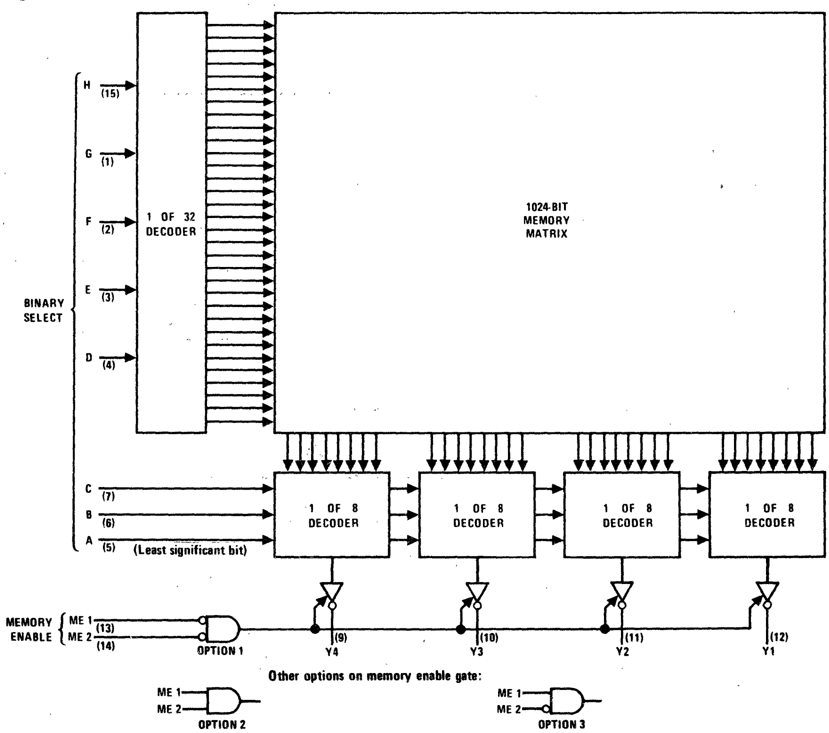
Truth Table

PROGRAMMABLE MEMORY ENABLE OPTIONS

OPTION	ME1	ME2	OUTPUTS
1	L	L	Normal
	H	X	Hi-Z
	X	H	Hi-Z
2	H	H	Normal
	L	X	Hi-Z
	X	L	Hi-Z
3	H	L	Normal
	X	H	Hi-Z
	L	X	Hi-Z

X = Don't Care

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM75/85 97 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current		DM75			−2.0	mA
			DM85			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4			V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max				0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			75	110	mA

Notes
(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM75/85 97 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address	Output	C_L = 50 pF, R_L = 400Ω		31	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address	Output			39	60	ns
t_{ZH}	Output Enable Time to High Level	Enable	Any			20	30	ns
t_{ZL}	Output Enable Time to Low Level	Enable	Any			20	30	ns
t_{HZ}	Output Disable Time from High Level	Enable	Any	C_L = 5 pF, R_L = 400Ω		20	30	ns
t_{LZ}	Output Disable Time from Low Level	Enable	Any			20	30	ns

Ordering Instructions

Programming instructions for the DM7597 or DM8597 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

Supplementary Ordering Data

Submit the following information with the data cards:

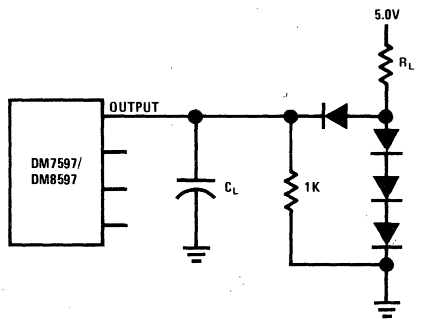
a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number

Data Card Format

Column

1-3 Punch a right-justified integer representing the binary input address (00-248) for the first set of outputs described on the card.
4 Punch a "–" (minus sign)
5-7 Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8-9 Blank
10-13 Punch "H," "L," or "X" for bits four, three, two and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high level output, L = low level output, X = output irrelevant.
14 Blank
15-18 Punch "H," "L," or "X" for the second set of outputs.
19 Blank
20-23 Punch "H," "L," or "X" for the third set of outputs.
24 Blank
25-28 Punch "H," "L," or "X" for the fourth set of outputs.
29 Blank
30-33 Punch "H," "L," or "X" for the fifth set of outputs.
34 Blank
35-38 Punch "H," "L," or "X" for the sixth set of outputs.
39 Blank
40-43 Punch "H," "L," or "X" for the seventh set of outputs.
44 Blank
45-48 Punch "H," "L," or "X" for the eighth set of outputs.
49 Blank
50-51 Punch a right-justified integer representing the current calendar day of the month.
52 Blank
53-55 Punch an alphabetic abbreviation representing the current month.
56 Blank
57-58 Punch the last two digits of the current year.
59 Blank
60-61 Punch "DM"
62-65 Punch 7597 or 8597
66-70 Blank
71 Punch 1, 2 or 3 for memory enable option desired (assumed 1 if not punched).

AC Test Circuit



TRI-STATE 256-Bit Read Only Memories

General Description

The DM7598/DM8598 is a mask-programmed 256-bit read only memory, organized as 32, 8-bit words. A 5-bit input code selects the appropriate word which then appears on the eight outputs. An enable input overrides the select inputs and blanks all outputs.

Although the DM7598/DM8598 can have its outputs tied together for word-expansion, the outputs are not open-collector, but rather the familiar totem-pole output with the capability of being placed in a "third-state." This unique TRI-STATE concept allows outputs to be tied together and then connected to a common bus line. Normal TTL outputs cannot be connected due to the low-impedance logical "1" output current which one device would have to sink from the other. If, however, on all but one of the connected devices both the upper and lower output transistors are turned "OFF," then the one remaining device in the normal low impedance state will have to supply to, or sink from, the other devices only a small amount of leakage current.

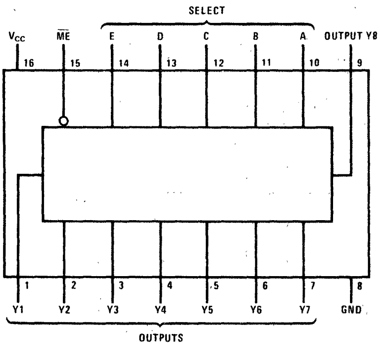
While it is true that in a TTL system open-collector gates could be used to perform the logic function of these TRI-STATE elements, neither waveform integrity nor optimum speed would be achieved. The low output impedance of the DM7598/DM8598 provides good capacitance drive capability and rapid transition from the logical "0" to logical "1" level, thus assuring both speed and waveform integrity.

It is possible to connect as many as 128 DM8598s to a common bus line and still have adequate drive capability to allow fan-out from the bus.

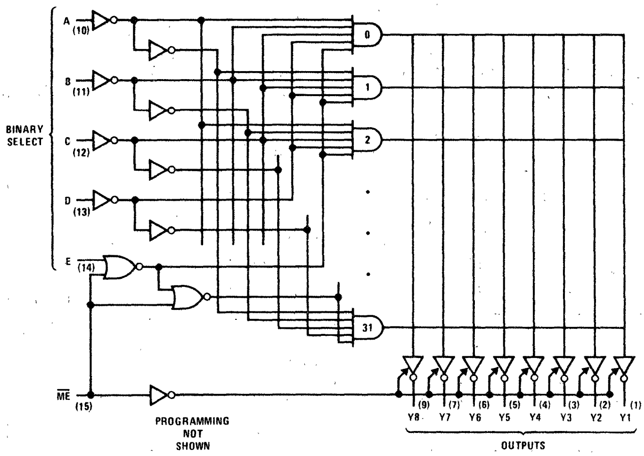
Features

- TRI-STATE outputs
- Pin compatible with DM5488/DM7488
- Organized as 32 8-bit words
- Full internal decoding
- 26 ns typical access time
- 350 mW typical power dissipation
- Designed for bus-organized systems

Connection and Logic Diagrams



7598(J); 8598(J), (N)



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

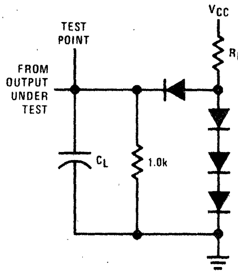
PARAMETER		CONDITIONS		DM75/85 98 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current		DM75			−2.0	mA
			DM85			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max		2.4			V
I_{OL}	Low Level Output Current					12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 12 mA				0.4	V
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.4V			−40	µA
			V_O = 2.4V			40	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Min, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				25	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max(2)		−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max, Inputs Grounded			70	99	mA

Notes
(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) Not more than one output should be shorted at a time.

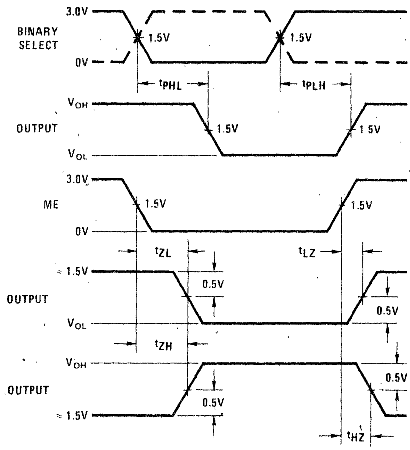
Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		PARAMETER CONDITIONS	CONDITIONS	DM75 MIN	DM75 TYP	DM75 MAX	DM85 MIN	DM85 TYP	DM85 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low to High Level Output	Access Time from Address	C_L = 50 pF R_L = 400Ω		23	65		23	50	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Access Time from Address			29	65		29	50	ns
t_{ZH}	Output Enable Time to High Level	Access Time from Memory Enable			16	40		16	30	ns
t_{ZL}	Output Enable Time to Low Level	Access Time from Memory Enable			20	40		20	30	ns
t_{HZ}	Output Disable Time from High Level	Disable Time from Memory Enable	C_L = 5.0 pF R_L = 400Ω		10	30		10	20	ns
t_{LZ}	Output Disable Time from Low Level	Disable Time from Memory Enable			22	45		22	40	ns

AC Test Circuit and Switching Time Waveforms



C_L includes probe and jig capacitance.
All diodes are 1N3064.



Note: Input waveforms are supplied by pulse generators having the following characteristics: $t_n \leq 10$ ns, $t_S \leq 10$ ns, PRR ≤ 1.0 MHz and $Z_{OUT} \approx 50\Omega$.

Truth Table

A special pattern has been generated for the DM7598/DM8598. The AA pattern provides a sine look up table. The 5-bit input code linearly devides 90° into 32 equal segments. Each 8-bit output is therefore the sine of the angle applied.

EXAMPLE: Input 11010 means 26/32 of 90°, or about 73°. The corresponding output 1110100 indicates (1/2 + 1/4 + 1/8 + 1/16 + 1/64) or about 0.95, which is close to the sine of 73°. Rounding-off has not been employed, since without rounding-off, it is possible to extend the accuracy with additional ROMs.

WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	$\overline{ME}$	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L
1	L	L	L	L	H	L	L	L	L	L	H	H	L	L
2	L	L	L	H	L	L	L	L	L	H	H	L	L	H
3	L	L	L	H	H	L	L	L	H	L	L	H	L	H
4	L	L	H	L	L	L	L	L	H	H	L	L	L	H
5	L	L	H	L	H	L	L	L	H	H	H	H	H	L
6	L	L	H	H	L	L	L	H	L	L	H	L	H	L
7	L	L	H	H	H	L	L	H	L	H	L	H	H	L
8	L	H	L	L	L	L	L	H	H	L	L	L	L	H
9	L	H	L	L	H	L	L	H	H	L	H	H	L	H
10	L	H	L	H	L	L	L	H	H	H	H	L	L	L
11	L	H	L	H	H	L	H	L	L	L	L	L	H	H
12	L	H	H	L	L	L	H	L	L	L	H	H	H	L
13	L	H	H	L	H	L	H	L	L	H	H	L	L	L
14	L	H	H	H	L	L	H	L	H	L	L	L	H	L
15	L	H	H	H	H	L	H	L	H	L	H	L	H	H
16	H	L	L	L	L	L	H	L	H	H	L	H	L	H
17	H	L	L	L	H	L	H	L	H	H	H	H	L	H
18	H	L	L	H	L	L	H	H	L	L	L	H	L	H
19	H	L	L	H	H	L	H	H	L	L	H	H	L	H
20	H	L	H	L	L	L	H	H	L	H	L	H	L	L
21	H	L	H	L	H	L	H	H	L	H	H	L	H	H
22	H	L	H	H	L	L	H	H	H	L	L	L	L	H
23	H	L	H	H	H	L	H	H	H	L	L	H	H	H
24	H	H	L	L	L	L	H	H	H	L	H	H	L	L
25	H	H	L	L	H	L	H	H	H	H	L	L	L	H
26	H	H	L	H	L	L	H	H	H	H	L	H	L	L
27	H	H	L	H	H	L	H	H	H	H	H	L	L	L
28	H	H	H	L	L	L	H	H	H	H	H	L	H	H
29	H	H	H	L	H	L	H	H	H	H	H	H	L	H
30	H	H	H	H	L	L	H	H	H	H	H	H	H	L
31	H	H	H	H	H	L	H	H	H	H	H	H	H	H
All	X	X	X	X	X	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

X = Don't Care

Truth Table/Order Blank

The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words (256 bits). The customer does this by filling out the Truth Table on this data sheet, and sending it in with his purchase order

WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	$\overline{ME}$	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	L	L	L	L	L	L								
1	L	L	L	L	H	L								
2	L	L	L	H	L	L								
3	L	L	L	H	H	L								
4	L	L	H	L	L	L								
5	L	L	H	L	H	L								
6	L	L	H	H	L	L								
7	L	L	H	H	H	L								
8	L	H	L	L	L	L								
9	L	H	L	L	H	L								
10	L	H	L	H	L	L								
11	L	H	L	H	H	L								
12	L	H	H	L	L	L								
13	L	H	H	L	H	L								
14	L	H	H	H	L	L								
15	L	H	H	H	H	L								
16	H	L	L	L	L	L								
17	H	L	L	L	H	L								
18	H	L	L	H	L	L								
19	H	L	L	H	H	L								
20	H	L	H	L	L	L								
21	H	L	H	L	H	L								
22	H	L	H	H	L	L								
23	H	L	H	H	H	L								
24	H	H	L	L	L	L								
25	H	H	L	L	H	L								
26	H	H	L	H	L	L								
27	H	H	L	H	H	L								
28	H	H	H	L	L	L								
29	H	H	H	L	H	L								
30	H	H	H	H	L	L								
31	H	H	H	H	H	L								
All	X	X	X	X	X	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

X = Don't Care

Notice: This sheet must be completed and signed by an authorized representative of the customer's company before an order can be entered.

To be used by National only

__________ Part Number

__________ S.O. Number

__________ Date Received

____________________ __________

Authorized Representative Date

____

Company

Desired Part ☐ DM7598 ☐ DM8598

Ordering Instructions

Programming instructions for the DM7598/DM8598 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table of the requested part. This function table, showing output conditions for each of the 32 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the word specified and describes the levels at the eight outputs for that word. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

Supplementary Ordering Data

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number

The following information will be furnished to the customer:
a) National's part number
b) National's sales order number
c) Date received

Data Card Format

Col. 1–2: Punch a right-justified integer representing the positive-logic binary input address (00–31) for the word described on the card.

Col. 3–4: Blank

Col. 5: Punch "H" or "L" for output Y8. H = high-voltage level output, L = low-voltage level output.

Col. 6–9: Blank

Col. 10: Punch "H" or "L" for output Y7.

Col. 11–14: Blank

Col. 15: Punch "H" or "L" for output Y6.

Col. 16–19: Blank

Col. 20: Punch "H" or "L" for output Y5.

Col. 21–24: Blank

Col. 25: Punch "H" or "L" for output Y4.

Col. 26–29: Blank

Col. 30: Punch "H" or "L" for output Y3.

Col. 31–34: Blank

Col. 35: Punch "H" or "L" for output Y2.

Col. 36–39: Blank

Col. 40: Punch "H" or "L" for output Y1.

Col. 41–49: Blank

Col. 50–51: Punch a right-justified integer representing the current calendar day of the month.

Col. 52: Blank

Col. 53–55: Punch an alphabetic abbreviation representing the current month.

Col. 56: Blank

Col. 57–58: Punch the last two digits of the current year.

Col. 59: Blank

Col. 60–61: Punch "DM,"

Col. 62–66: Punch "7598" or "8598."

Col. 67–68: Blank

Col. 69–80: These columns may be used for any customer information or identification.

TRI-STATE 64-Bit Random Access Memories

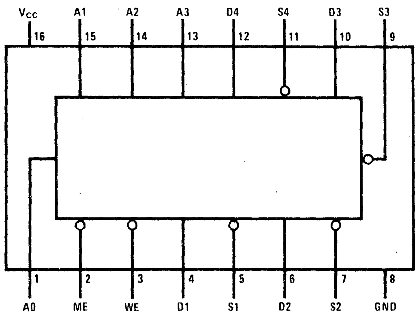
General Description

The DM7599/DM8599 is a fully decoded 64-bit RAM organized as 16 4-bit words.The memory is addressed by applying a binary number to the four address inputs. After addressing, information may be either written into or read from the memory. To write, both the memory enable and the write enable inputs must be in the logical "0" state. Information applied to the four write inputs will then be written into the addressed location. To read information from the memory the memory enable input must be in the logical "0" state and the write enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the memory enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus line without the use of pull-up resistors. All memories except one are gated into the high impedance state while the one selected memory exhibits the normal low impedance output characteristics of TTL.

Features

- TRI-STATE outputs
- Same pin-out as DM5489/DM7489
- Organized as 16, 4-bit words
- Expandable to 2048, 4-bit words without additional resistors (DM8599 only)
- Typical access from chip enable 20 ns
- Typical access time 28 ns

Connection Diagram

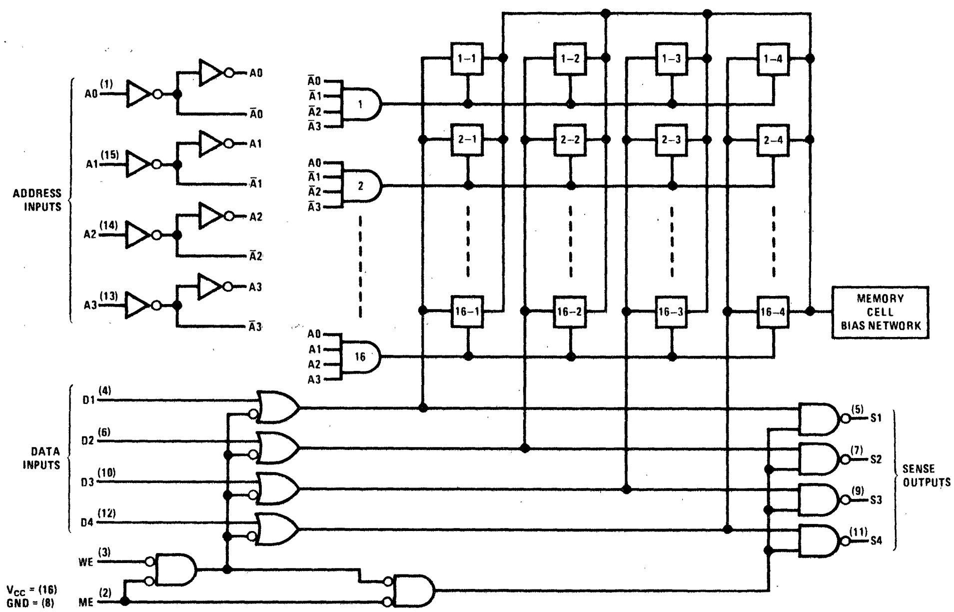


7599(J); 8599(J), (N)

Truth Table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
L	L	Write	Hi-Z
L	H	Read	Complement of Data Stored in Memory
H	X	Hold	Hi-Z

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM75/85 99 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current		DM75			−2.0	mA
			DM85			−5.2	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max				2.4	V
I_{OL}	Low Level Output Current					12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 12 mA				0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			80	120	mA

Notes:

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

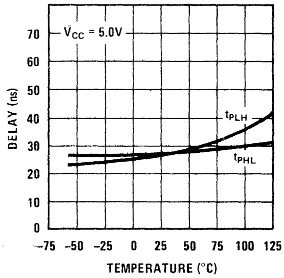
(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

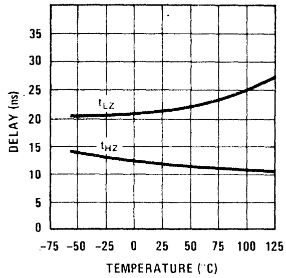
	PARAMETER		FROM	TO	CONDITIONS	DM75/85 99 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Address	Output	C_L = 50 pF, R_L = 400Ω		27	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Address	Output			28	45	ns
t_{ZH}	Output Enable Time to High Level		ME	Output			14	20	ns
t_{ZL}	Output Enable Time to Low Level		ME	Output			19	30	ns
t_{HZ}	Output Disable Time from High Level		ME	Output	C_L = 5 pF, R_L = 400Ω		12	20	ns
t_{LZ}	Output Disable Time from Low Level		ME	Output			21	30	ns
t_{SETUP}	Setup Time	Address				0	−17		ns
		Data				0	−15		
t_{HOLD}	Hold Time	Address				5	−7		ns
		Data				0	−14		
t_{WP}	Write Enable Pulse Width					40	23		ns
t_{SR}	Sense Recovery Time						42	60	ns

Typical Performance Curves

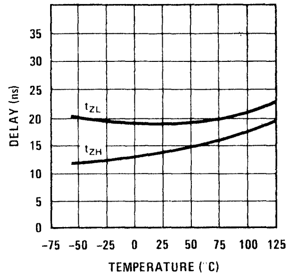
DELAY FROM ADDRESS TO OUTPUT



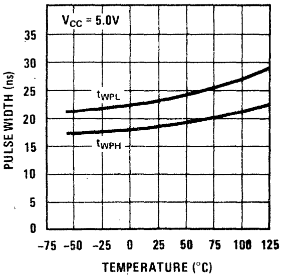
DELAY FROM ENABLE TO HIGH IMPEDANCE STATE



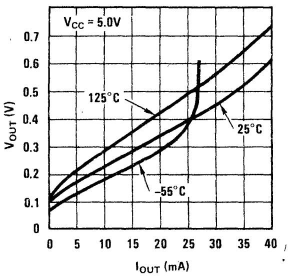
DELAY FROM ENABLE TO LOW IMPEDANCE STATE



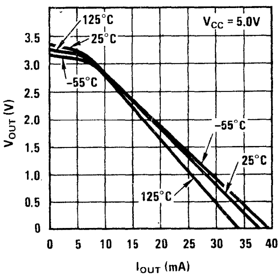
MINIMUM WRITE PULSE WIDTH



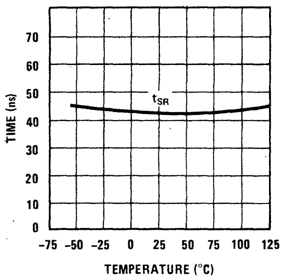
LOGICAL "0" OUTPUT VOLTAGE VS SINK CURRENT



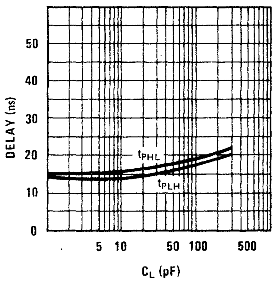
LOGICAL "1" OUTPUT VOLTAGE VS SOURCE CURRENT



SENSE RECOVERY TIME

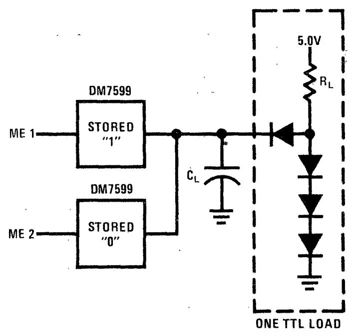


DELAY FROM ENABLE TO OUTPUT VS LOAD CAPACITANCE



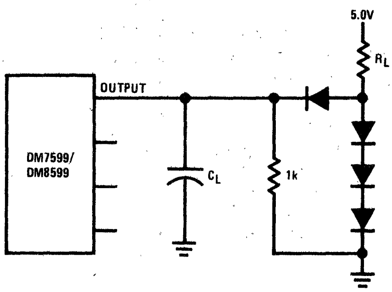
Test Circuit

TEST CIRCUIT FOR DELAY VS LOAD CAPACITANCE



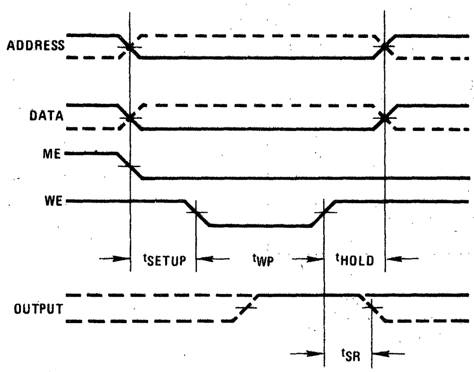
Note: In a typical application the output of the TRI-STATE memories might be wired together and one would be switching to the low impedance state at the same time the circuit previously selected would be switching back into the high impedance state. The measurements of delay versus load capacitance were made under conditions which simulate actual operating conditions in an application. (See test circuit.)

AC Test Circuit

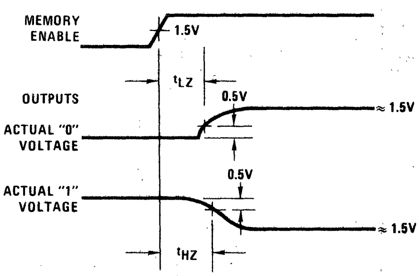


Switching Time Waveforms

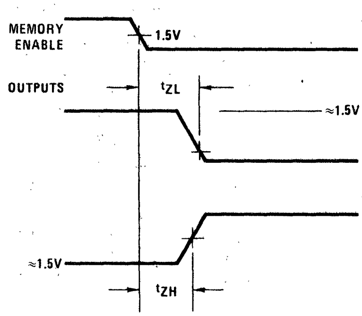
WRITE CYCLE



t_{LZ} & t_{HZ}



t_{ZL} & t_{ZH}



Note: The pulse generator has the following characteristics: V = 3.0V, t_r = 15 ns, t_f = 5.0 ns, f = 500 kHz, duty cycle = 50%, Z_{OUT} = 50Ω, V_t = 1.3V @ 25°C.

TRI-STATE Magnitude Comparators with A almost equal B

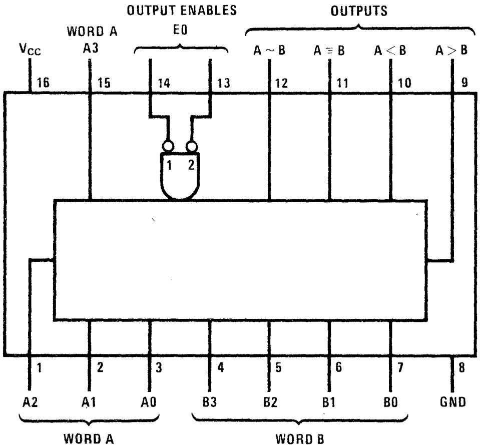
General Description

These circuits are low power, 4-bit, magnitude comparators which provide both standard totem-pole TTL outputs as well as TRI-STATE outputs. A comparison of two, 4-bit words is performed, and the result indicated by the four outputs: A > B, A < B, A ≡ B, and A ~ B. The A ~ B output is unique with this device, and is enabled only when Word A is within one binary count of Word B. The comparison is expandable to any number, without the need for external gates. The maximum speed method of cascading, and typical comparison times are shown in *Figures 1 and 2.*

Features

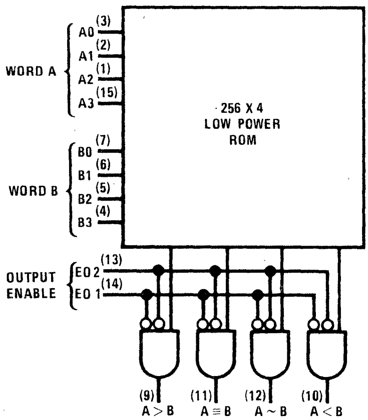
- TRI-STATE outputs
- May be cascaded to compare words of greater length
- Typical power dissipation 75 mW
- Four separate outputs
  - A ≡ B
  - A < B
  - A > B
  - A ~ B
- A almost equal to B (A ~ B) output permits look-ahead and anticipation of a match (A ≡ B)

Connection Diagram



76L24/86L24(J), (N), (W)

Logic Diagram



Truth Table

COMPARING INPUTS (MSB)			(LSB)	ENABLE INPUTS		OUTPUTS			
A3 B3	A2 B2	A1 B1	A0 B0	E01	E02	A < B	A ≡ B	A ~ B	A > B
A3 > B3	A2 > B2	A1 > B1	A0 > B0	L	L	L	L	H	H
A3 < B3	A2 < B2	A1 < B1	A0 < B0	L	L	H	L	H	L
A3 = B3	A2 > B2	X	X	L	L	L	L	L	H
A3 = B3	A2 < B2	X	X	L	L	H	L	L	L
A3 = B3	A2 = B2	A1 > B1	X	L	L	L	L	L	H
A3 = B3	A2 = B2	A1 < B1	X	L	L	H	L	L	L
A3 = B3*	A2 = B2	A1 = B1	A0 > B0	L	L	L	L	H	H
A3 = B3**	A2 = B2	A1 = B1	A0 < B0	L	L	H	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	L	L
X	X	X	X	H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
X	X	X	X	X	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z

*Word A > Word B By 1
**Word A < Word B By 1
H = High Level, L = Low Level, X = Don't Care

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM76 L24 MIN	DM76 L24 TYP(1)	DM76 L24 MAX	DM86 L24 MIN	DM86 L24 TYP(1)	DM86 L24 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−1.0			−1.0	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.7V, $I_{OH} = -1.0$ mA		2.4			2.4			V
I_{OL}	Low Level Output Current					2.0			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.7V, I_{OL} = Max				0.3			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V V_{IL} = 0.7V	V_O = 0.3V			−40			−40	μA
			V_O = 2.4V			40			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				100			100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−180			−180	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−6		−30	−6		−30	mA
I_{CC}	Supply Current	V_{CC} = Max, V_I = 0V			15	20		15	20	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS	DM76L/86L L24 MIN	DM76L/86L L24 TYP	DM76L/86L L24 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 50 pF, R_L = 4 kΩ		86	130	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output	C_L = 50 pF, R_L = 4 kΩ		55	85	ns
t_{ZH}	Output Enable Time to High Level			C_L = 50 pF, R_L = 4 kΩ		34	51	ns
t_{ZL}	Output Enable Time to Low Level			C_L = 50 pF, R_L = 4 kΩ		47	70	ns
t_{HZ}	Output Disable Time from High Level			C_L = 5 pF, R_L = 4 kΩ		15	23	ns
t_{LZ}	Output Disable Time from Low Level			C_L = 5 pF, R_L = 4 kΩ		57	86	ns

Typical Applications

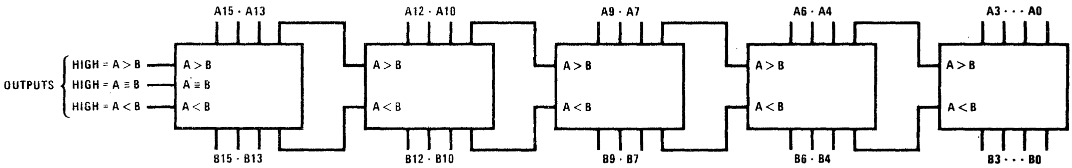


FIGURE 1. 16-BIT COMPARATOR, MAXIMUM LOGIC EXPANSION (NOT SUITABLE FOR A ~ B)

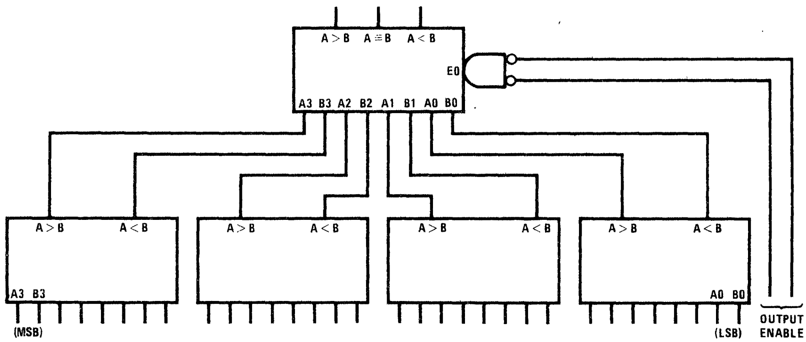
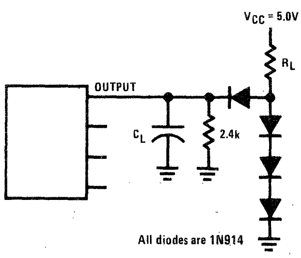
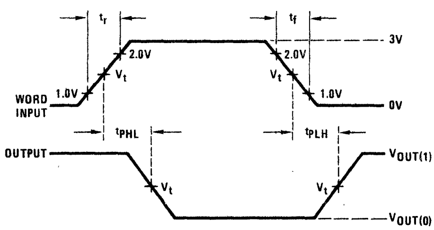


FIGURE 2. MAXIMUM SPEED EXPANSION (NOT SUITABLE FOR A ~ B)

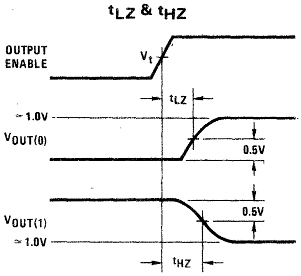
COMPARE *(FIGURE 2)*	CIRCUIT DELAY	NUMBER OF CIRCUITS
1-4 BITS	1 DELAY	1
5-7 BITS	2 DELAYS	2
8-10 BITS	2 DELAYS	3
11-13 BITS	2 DELAYS	4
14-16 BITS	2 DELAYS	5

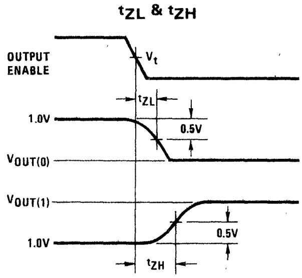
AC Test Circuit and Switching Time Waveforms





OUTPUT ENABLE





Note: The pulse generator has the following characteristics: V = 3.0V, t_r = 15 ns, t_f = 5.0 ns, f = 500 kHz, duty cycle = 50%, Z_{OUT} = 50Ω. V_t = 1.3V @ 25°C.

TRI-STATE 7-Segment to BCD Decoder

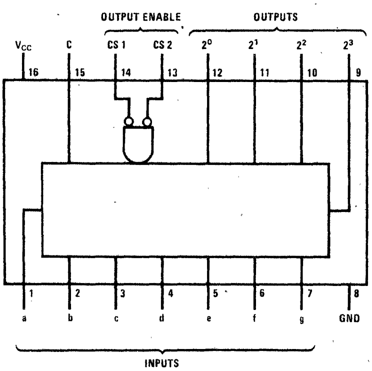
General Description

These circuits are low power converters which accept 7-segment data on the inputs, and provide binary-coded decimal (BCD) data on the outputs. An input control line is also provided, in the event that the 7-segment input data is presented in inverted form. The BCD outputs are normally of the standard totem-pole TTL type, however they may also be converted to high-impedance (TRI-STATE) types by applying a high logic level to either of the two output enable pins.

Features

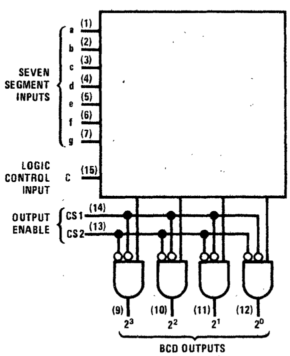
- TRI-STATE outputs
- Typical power dissipation 75 mW
- Typical propagation delay 70 ns

Connection Diagram

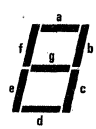


76L25/86L25(J), (N), (W)

Logic Diagram



Segment Identification



Truth Table

DIGIT	a	b	c	d	e	f	g	CTL	CS 1	CS 2	2^3	2^2	2^1	2^0
0	H	H	H	H	H	H	L	H	L	L	L	L	L	L
1	L	H	H	L	L	L	L	H	L	L	L	L	L	H
2	H	H	L	H	H	L	H	H	L	L	L	L	H	L
3	H	H	H	H	L	L	H	H	L	L	L	L	H	H
4	L	H	H	L	L	H	H	H	L	L	L	H	L	L
5	H	L	H	H	L	H	H	H	L	L	L	H	L	H
b	L	L	H	H	H	H	H	H	L	L	L	H	H	L
6	H	L	H	H	H	H	H	H	L	L	L	H	H	L
7	H	H	H	L	L	L	L	H	L	L	L	H	H	H
8	H	H	H	H	H	H	H	H	L	L	H	L	L	L
9	H	H	H	L	L	H	H	H	L	L	H	L	L	H
9	H	H	H	H	L	H	H	H	L	L	H	L	L	H
BLANK	L	L	L	L	L	L	L	H	L	L	H	H	H	H
L	L	L	L	H	H	H	L	H	L	L	H	H	L	H
E	H	L	L	H	H	H	H	H	L	L	H	H	H	L
A	H	H	H	L	H	H	H	H	L	L	H	L	H	L
P	H	H	L	L	H	H	H	H	L	L	H	L	H	H
-	L	L	L	L	L	L	H	H	L	L	H	H	L	L
0	L	L	L	L	L	L	H	L	L	L	L	L	L	L
1	H	L	L	H	H	H	H	L	L	L	L	L	L	H
2	L	L	H	L	L	H	L	L	L	L	L	L	H	L
3	L	L	L	L	H	H	L	L	L	L	L	L	H	H
4	H	L	L	H	H	L	L	L	L	L	L	H	L	L
5	L	H	L	L	H	L	L	L	L	L	L	H	L	H
b	H	H	L	L	L	L	L	L	L	L	L	H	H	L
6	L	H	L	L	L	L	L	L	L	L	L	H	H	L
7	L	L	L	H	H	H	H	L	L	L	L	H	H	H
8	L	L	L	L	L	L	L	L	L	L	H	L	L	L
9	L	L	L	H	H	L	L	L	L	L	H	L	L	H
9	L	L	L	L	H	L	L	L	L	L	H	L	L	H
BLANK	H	H	H	H	H	H	H	L	L	L	H	H	H	H
L	H	H	H	L	L	L	H	L	L	L	H	H	L	H
E	L	H	H	L	L	L	L	L	L	L	H	H	H	L
A	L	L	L	H	L	L	L	L	L	L	H	L	H	L
P	L	L	H	H	L	L	L	L	L	L	H	L	H	H
-	H	H	H	H	H	H	L	L	L	L	H	H	L	L
	X	X	X	X	X	X	X	X	H	X	Z	Z	Z	Z
	X	X	X	X	X	X	X	X	X	H	Z	Z	Z	Z
	All Other Input Combinations								L	L	H	H	H	H

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM76L L25 MIN	DM76L L25 TYP(1)	DM76L L25 MAX	DM86L L25 MIN	DM86L L25 TYP(1)	DM86L L25 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−1.0			−1.0	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.7V, $I_{OH} = -1.0$ mA		2.4			2.4			V
I_{OL}	Low Level Output Current					2.0			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.7V, I_{OL} = Max				0.3			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V V_{IL} = 0.7V	V_O = 0.3V			−40			−40	μA
			V_O = 2.4V			40			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				100			100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−180			−180	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−6		−30	−6		−30	mA
I_{CC}	Supply Current	V_{CC} = Max, V_I = 0V			15	20		15	20	mA

Notes

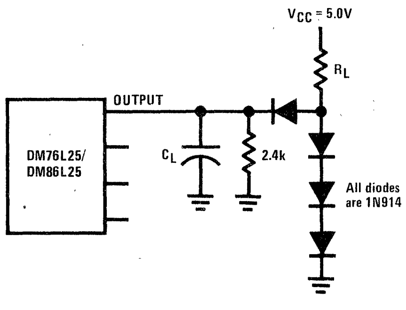
(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

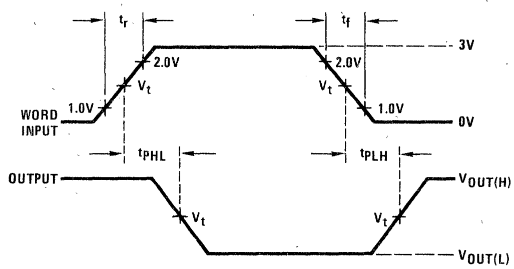
Switching Characteristics V_{CC} = 5V, T_A = 25°C

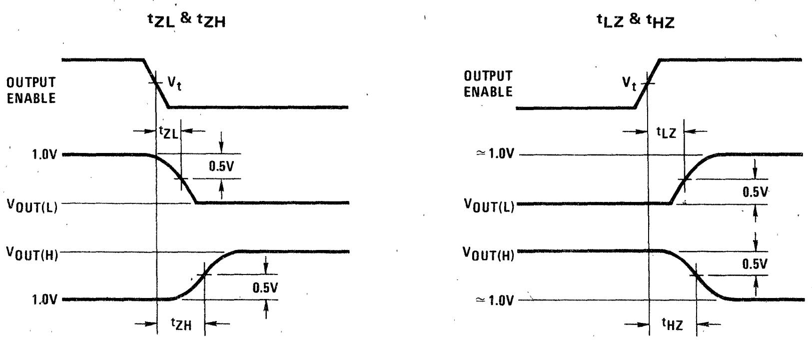
PARAMETER		FROM	TO	CONDITIONS	DM76L/86L L25 MIN	DM76L/86L L25 TYP	DM76L/86L L25 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 50 pF, R_L = 4 kΩ		86	130	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output			55	85	ns
t_{ZH}	Output Enable Time to High Level					34	51	ns
t_{ZL}	Output Enable Time to Low Level					47	70	ns
t_{HZ}	Output Disable Time from High Level			C_L = 5 pF, R_L = 4 kΩ		15	23	ns
t_{LZ}	Output Disable Time from Low Level					57	86	ns

AC Test Circuit



Switching Time Waveforms





Note: The pulse generator has the following characteristics: V = 3.0V, t_r = 15 ns, t_f = 5.0 ns, f = 500 kHz, duty cycle = 50%, Z_{OUT} = 50Ω, V_t = 1.3V @ 25°C.

Presettable Decade/Binary Counters

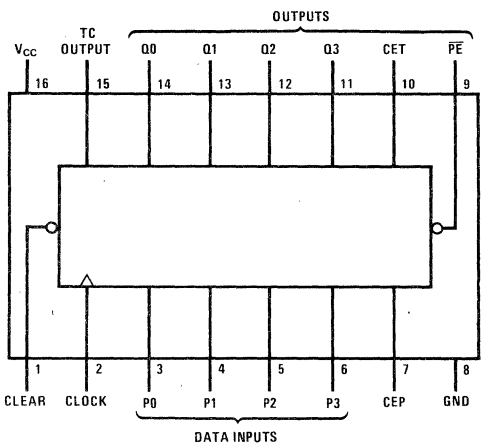
General Description

These synchronous, presettable counters are true tenth-power versions of the popular DM54160A/DM74160A, DM54161A/DM74161A, DM9310, and DM9316 counters. They feature an internal carry/look ahead for high-speed cascading, and trigger on the positive-going transition of the clock pulse. The counters are fully programmable; and, since presetting is synchronous, applying a low logic level to the load input disables the counter and forces the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs. Low-to-high transitions at the load inputs are acceptable, regardless of the logic levels on the clock or enable inputs. The clear (reset) function is asynchronous, and a low level applied to the clear input sets all four outputs low regardless of the levels on the clock, load, or enable inputs. In high-speed cascading arrangements, both count-enable inputs (P, T) must be high to count, and input T is fed forward to enable the ripple carry output. This high-level overflow ripple carry pulse can be used to enable successive stages. High-to-low level transitions at the P or T enable inputs are permitted, regardless of the logic level on the clock.

Features

- Low power versions popular counters
  DM76L75/DM86L75 = DM54160A/DM74160A, DM9310 – decade counter
  DM76L76/DM86L76 = DM54161A/DM74161A, DM9316 – binary counter
- Internal look-ahead for fast cascading
- Counters are fully synchronous and presettable
- Typical power dissipation 33 mW

Connection Diagram



76L75/86L75(J), (N), (W);
76L76/86L76(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM76L L75, L76 MIN	DM76L L75, L76 TYP(1)	DM76L L75, L76 MAX	DM86L L75, L76 MIN	DM86L L75, L76 TYP(1)	DM86L L75, L76 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.7	V
I_{OH}	High Level Output Current					−200			−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.7V, I_{OH} = −200μA		2.4	3.1		2.4	3.1		V
I_{OL}	Low Level Output Current					2.0			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.7V, I_{OL} = Max			0.2	0.3		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V	CET Input			200			200	μA
			Others			100			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	CET Input			20			20	μA
			Others			10			10	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	CET Input			−360			−360	μA
			Others			−180			−180	
I_{OS}	Short Circuit Output Current	V_{CC} = Max		−3	−9	−15	−3	−9	−15	mA
I_{CC}	Supply Current	V_{CC} = Max			6.5	9		6.5	9	mA

Notes

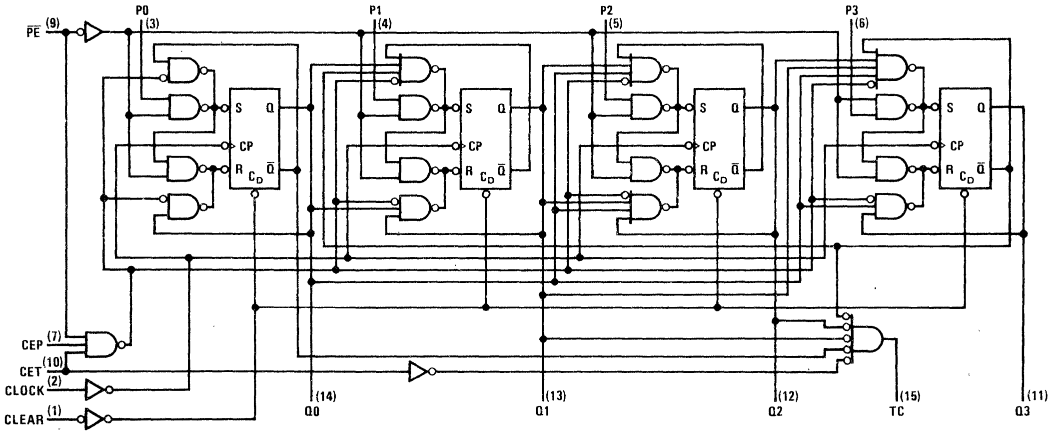
(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

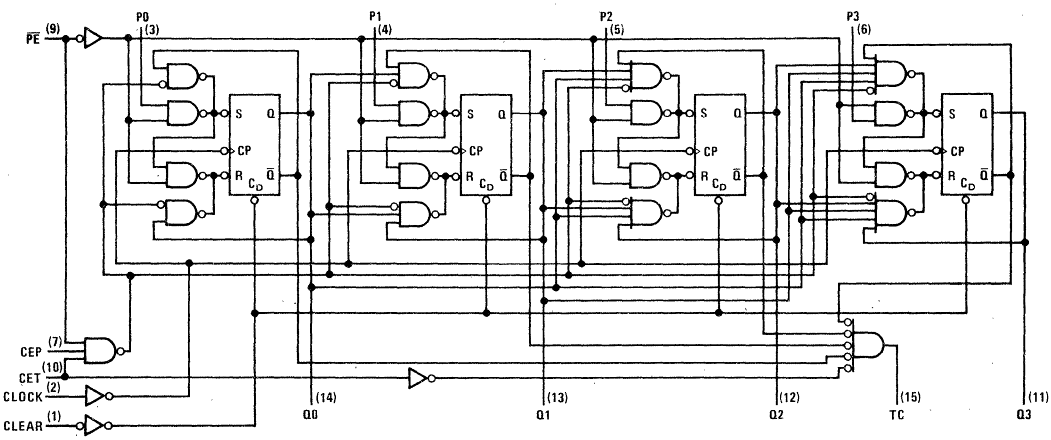
	PARAMETER		FROM	TO	CONDITIONS	DM76L/86L L75, L76 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				C_L = 50 pF, R_L = 4 kΩ	6	13		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Q Output			45	75	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Q Output			65	110	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	TC Output			70	115	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	TC Output			85	140	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		CET	TC Output			35	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		CET	TC Output			35	60	ns
$t_{W(CLOCK)}$	Minimum Pulse Width					60	25		ns
$t_{W(RESET)}$	Minimum Pulse Width					80	30		ns
t_{SETUP}	Setup Time	CE				65	40		ns
		P Inputs				30	15		
		Parallel Entry				65	40		
t_{HOLD}	Hold Time	CE				80	50		ns
		P Inputs				30	15		
		Parallel Entry				65	40		

Logic Diagrams

76L75/86L75 (DECADE)



76L76/86L76 (BINARY)



V_{CC} = (16)
GND = (8)

7 by 9 Character Generators

General Description

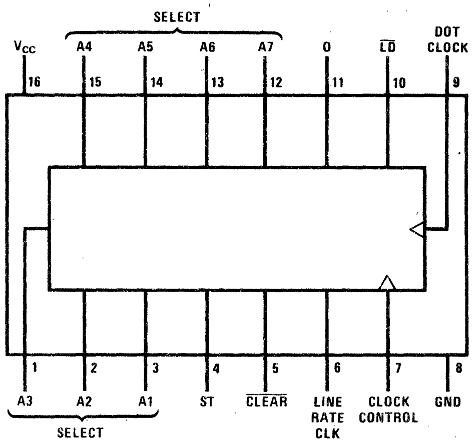
The DM7678/8678 and DM7679/DM8679 are bipolar character generators. A maximum of 64 characters can be displayed in a 7X9 dot matrix. Shifted characters can be generated by the on-chip subtractor. On-chip line counter and parallel-in-serial-out shift register reduce package pin-out.

The clear input and the load input are active low. $\overline{\text{Load}}$ is synchronous with the Dot Rate Clock. Both the line rate clock and the dot rate clock are positive triggered. When the strobe input receives a low signal, the character address will be held at the inputs.

Features

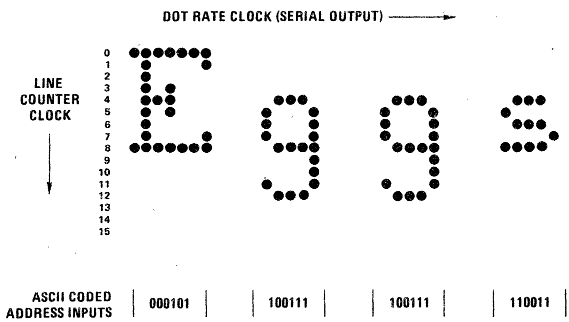
- TRI-STATE outputs
- On-chip input latches
- On-chip line counter
- On-chip shift register
- Serial output
- 20 MHz typical clock rate
- Shifted characters

Connection Diagram



7678(J); 8678(J), (N);
7679(J); 8679(J), (N)

Character Display Example



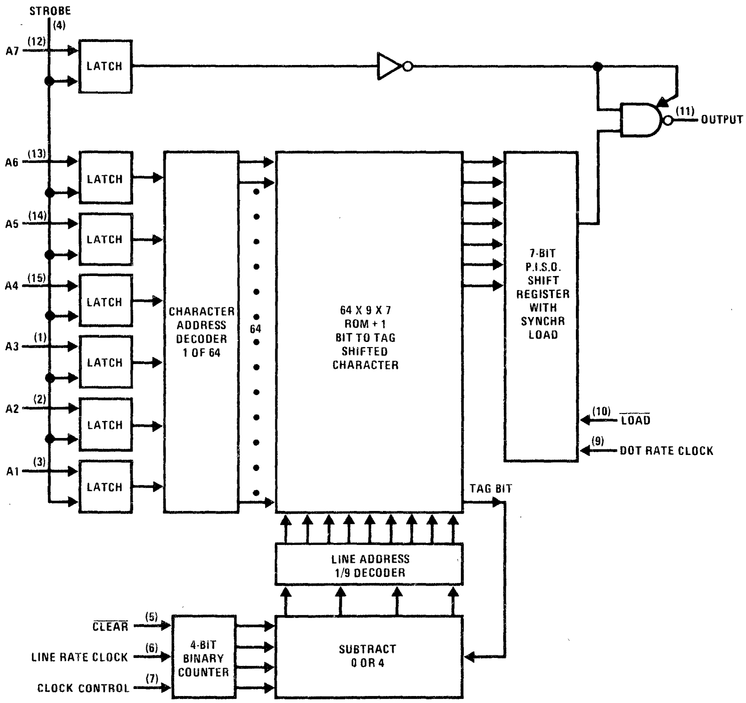
Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM76/86 78, 79 MIN	TYP(1)	MAX	UNITS
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −2 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA			0.4	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.8	mA
I_{CC}	Supply Current	V_{CC} = Max		100		mA
f_{MAX}	Maximum Clock Frequency	V_{CC} = 5V, T_A = 25°C		20		MHz

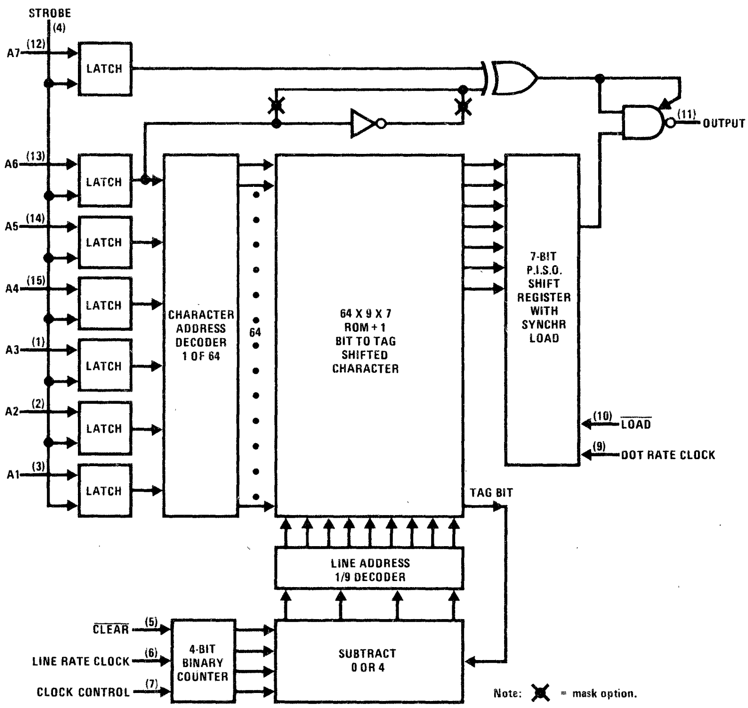
Notes:
(1) All typical values are at V_{CC} = 5V, T_A = 25°C

Logic Diagrams

78



79

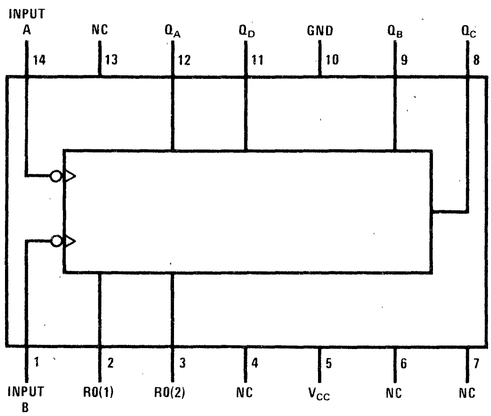


Binary Counters

General Description

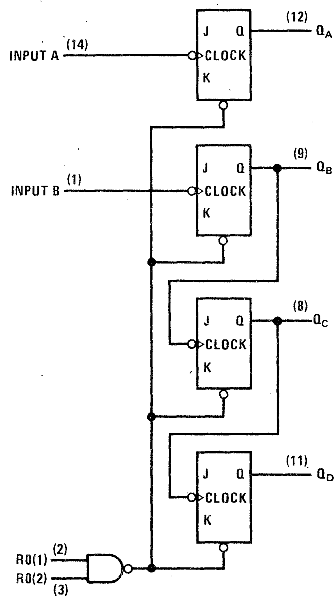
These circuits are full tenth-power versions of the popular DM5493A/DM7493A binary counters. The important feature is that they provide the same pinout as the DM5493A/DM7493A, whereas the DM54L93/DM74L93 has a completely different pinout. Otherwise they offer the same features and electrical characteristics as the DM54L93/DM74L93. To employ the maximum count length, the B input is connected to the Q_A output. The input count pulses are applied to the A input, and the outputs are as described below in the truth table.

Connection Diagram



76L93/86L93(J), (N), (W)

Logic Diagram



Truth Tables

RESET/COUNT TRUTH TABLE

RESET INPUTS		OUTPUT			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

COUNT SEQUENCE TABLE

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM76L L93 MIN	DM76L L93 TYP(1)	DM76L L93 MAX	DM86L L93 MIN	DM86L L93 TYP(1)	DM86L L93 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.7	V
I_{OH}	High Level Output Current					−200			−200	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.7V, I_{OH} = −200μA		2.4	2.8		2.4	2.8		V
I_{OL}	Low Level Output Current					2.0			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.7V, I_{OL} = Max			0.15	0.3		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V	Reset			100			100	μA
			A Input			200			200	
			B Input			200			200	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Reset			10			10	μA
			A Input			20			20	
			B Input			20			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Reset			−180			−180	μA
			A Input			−360			−360	
			B Input			−360			−360	
I_{OS}	Short Circuit Output Current	V_{CC} = Max		−3	−9	−15	−3	−9	−15	mA
I_{CC}	Supply Current	V_{CC} = Max(2)				5.5			5.5	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS	DM76L/86L L93 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency			C_L = 50 pF, R_L = 4 kΩ	6	15		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A	Q_D			210	400	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	A	Q_D			230	400	ns
t_W	Pulse Width (All Inputs)				200			ns
t_{SETUP}	Reset Inactive State Setup Time				200			ns

TRI-STATE 1024-Bit Read Only Memories

General Description

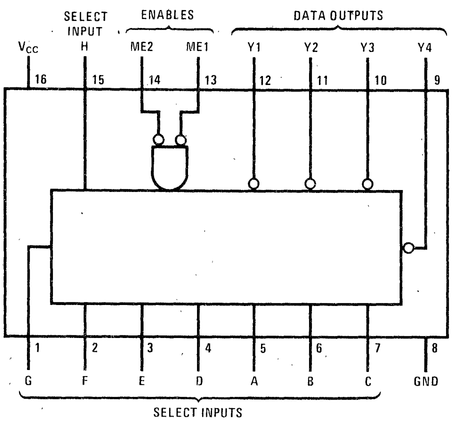
The DM76L97/DM86L97 is a custom-programmed Read Only Memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs.

Two overriding memory enable inputs are provided which when mask-programmed in one of the three options described will cause all four outputs to read either the normal memory contents or go to the high impedance state.

Features

- Full tenth-power technology
- Pin compatible with SN54187/SN74187
- Typical power dissipation 75 mW
- Typical access time 70 ns
- Custom-programmed memory enable inputs
- TRI-STATE outputs

Connection Diagram



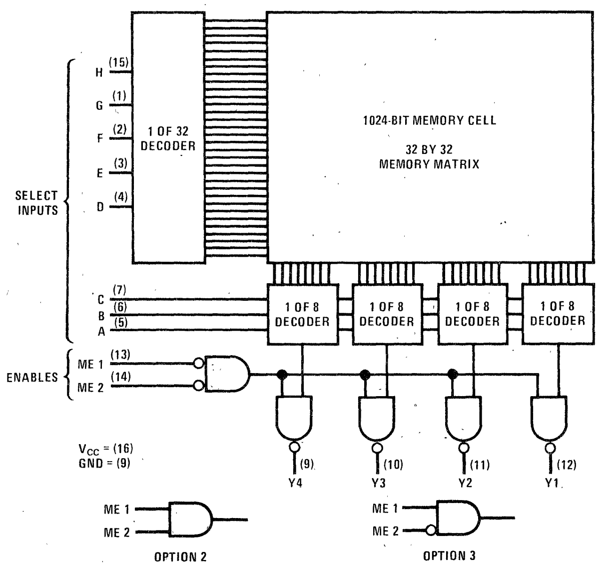
76L97/86L97(J), (N), (W)

Truth Table

OPTION	ME1	ME2	OUTPUTS
1	L	L	Normal
	H	X	High Impedance
	X	H	High Impedance
2	H	H	Normal
	L	X	High Impedance
	X	L	High Impedance
3	H	L	Normal
	X	H	High Impedance
	L	X	High Impedance

X = Don't Care

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM76L/86L L97 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−1.0	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −1.0 mA		2.4			V
I_{OL}	Low Level Output Current		DM76			2.0	mA
			DM86			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM76			0.3	V
			DM86			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−180	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−6		−30	mA
I_{CC}	Supply Current	V_{CC} = Max			15	20	mA

Notes

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS	DM76L/86L L97 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address	Output	C_L = 50 pF, R_L = 4kΩ		86	130	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address	Output	C_L = 50 pF, R_L = 4kΩ		55	85	ns
t_{ZH}	Output Enable Time to High Level	Enable	Any	C_L = 50 pF, R_L = 4kΩ		34	51	ns
t_{ZL}	Output Enable Time to Low Level	Enable	Any	C_L = 50 pF, R_L = 4kΩ		47	70	ns
t_{HZ}	Output Disable Time from High Level	Enable	Any	C_L = 5.0 pF, R_L = 4kΩ		15	23	ns
t_{LZ}	Output Disable Time from Low Level	Enable	Any	C_L = 5.0 pF, R_L = 4kΩ		57	86	ns

Ordering Instructions

Programming instructions for the DM76L97 or DM86L97 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

Supplementary Ordering Data

Submit the following information with the data cards:

a) Customer's name and address

b) Customer's purchase order number

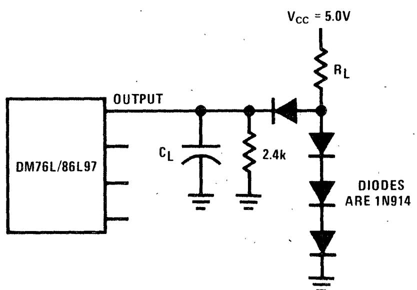
c) Customer's drawing number.

Data Card Format

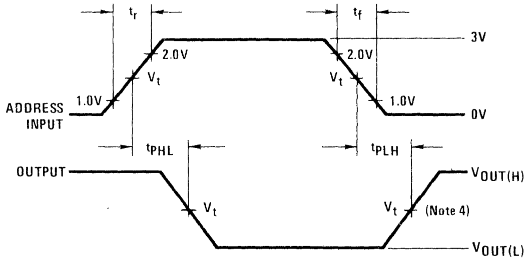
Column

1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8- 9	Blank
10-13	Punch "H," "L," or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. (H = high level output, L = low level output, X = don't care.)
14	Blank
15-18	Punch "H," "L," or "X" for the second set of outputs.
19	Blank
20-23	Punch "H," "L," or "X" for the third set of outputs.
24	Blank
25-28	Punch "H," "L," or "X" for the fourth set of outputs.
29	Blank
30-33	Punch "H," "L," or "X" for the fifth set of outputs.
34	Blank
35-38	Punch "H," "L," or "X" for the sixth set of outputs.
39	Blank
40-43	Punch "H," "L," or "X" for the seventh set of outputs.
44	Blank
45-48	Punch "H," "L," or "X" for the eighth set of outputs.
49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "DM"
62-67	Punch the National Semiconductor part number DM76L97 or DM86L97.
68-70	Blank

AC Test Circuit

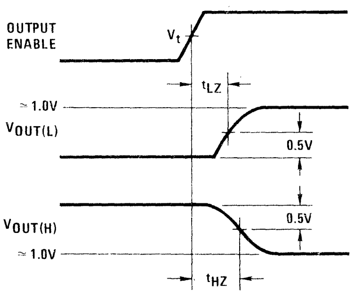


Switching Time Waveforms

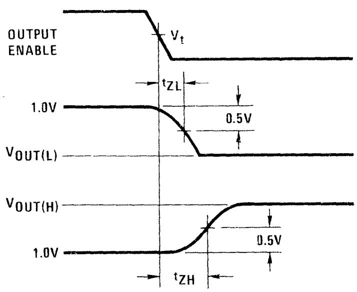


MEMORY ENABLE

t_{LZ} & t_{HZ}



t_{ZL} & t_{ZH}



Note: The pulse generator has the following characteristics: $V = 3.0V$, $t_r = 15$ ns, $t_f = 5.0$ ns, $f = 500$ kHz, duty cycle = 50%, $Z_{OUT} = 50\Omega$. $V_t = 1.3V$ @ 25°C.

TRI-STATE 64-Bit Random Access Memories

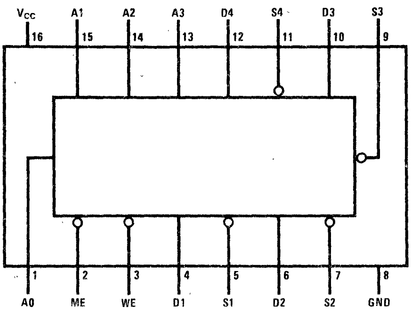
General Description

The DM76L99/DM86L99 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory, the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 75 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance state while the one selected memory exhibits the normal totem-pole, low impedance output characteristics of TTL.

Features

- Same pin-out as SN5489/SN7489, 3101, MM5501
- Organized as 16, 4-bit words
- Expandable to 1200, 4-bit words without additional resistors
- Typical access from chip enable 50 ns
- Typical access time 80 ns
- Typical power dissipation 75 mW

Connection Diagram

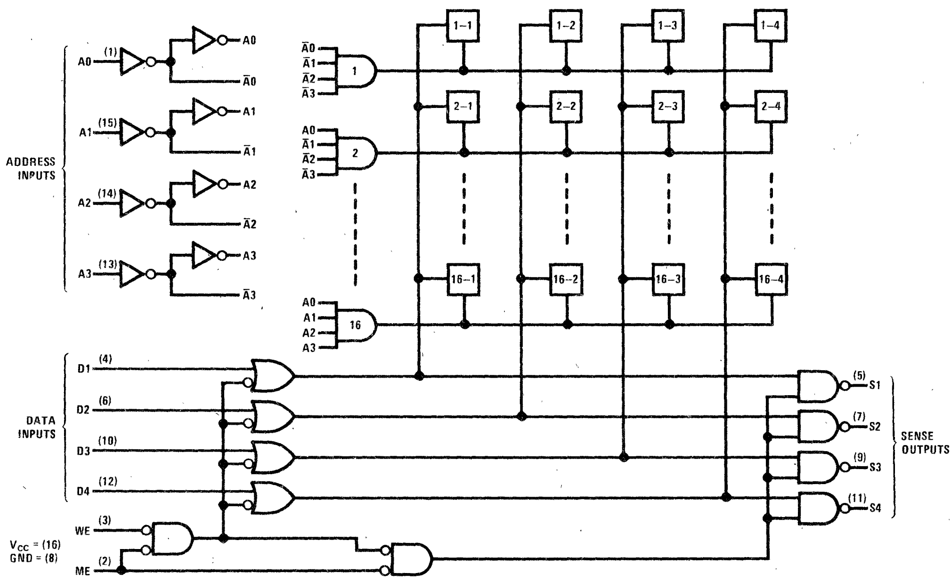


76L99/86L99(J), (N), (W)

Truth Table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
L	L	Write	Hi-Z
L	H	Read	Complement of Data Stored in Memory
H	X	Hold	Hi-Z

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM76L/86L L99 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = Min		2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min				0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−1.0	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −1.0 mA		2.4			V
I_{OL}	Low Level Output Current		DM76L			2.0	mA
			DM86L			3.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM76L			0.3	V
			DM86L			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max	V_O = 0.3V			−40	μA
			V_O = 2.4V			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−180	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−6		−30	mA
I_{CC}	Supply Current	V_{CC} = Max			15	19	mA

Notes

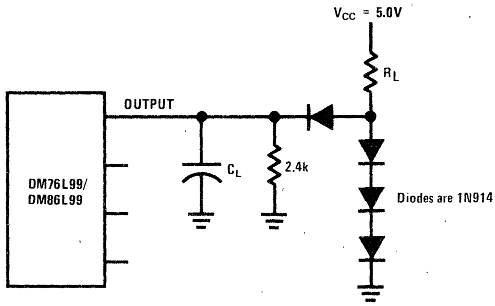
(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

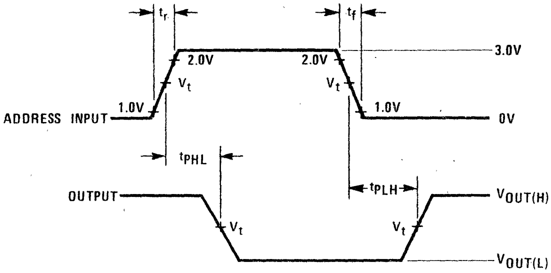
Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER			FROM	TO	CONDITIONS	DM76L/86L L99 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Address	Output	C_L = 50 pF, R_L = 4 kΩ		51	120	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Address	Output			77	150	ns
$t_{\overline{EN}}$	Output Disable Time from Write Enable		WE	Output			73	110	ns
t_{SR}	Sense Recovery Time from Write Enable		WE	Output			110	165	ns
t_{ZH}	Output Enable Time to High Level		ME	Output			30	50	ns
t_{ZL}	Output Enable Time to Low Level		ME	Output			29	43	ns
t_{HZ}	Output Disable Time from High Level		ME	Output	C_L = 5 pF, R_L = 4 kΩ		18	27	ns
t_{LZ}	Output Disable Time from Low Level		ME	Output			37	56	ns
t_{SETUP}	Setup Time	Data				0			ns
		Address				0			ns
		ME				0			ns
t_{HOLD}	Hold Time	Data				0			ns
		Address				0			ns
		ME				0			ns
t_{WP}	Write Enable Pulse Width					50	30		ns

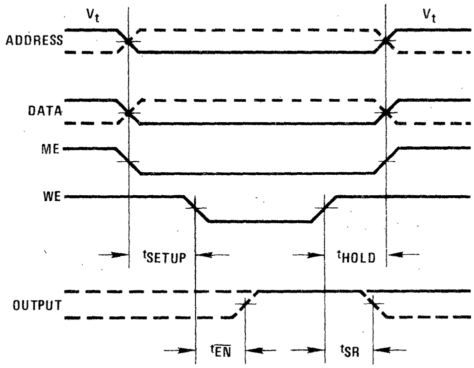
AC Test Circuit



Switching Time Waveforms

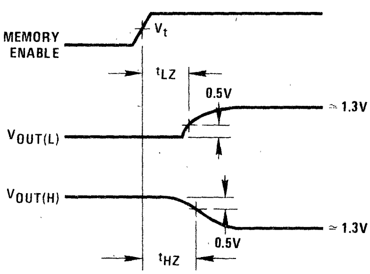


WRITE CYCLE

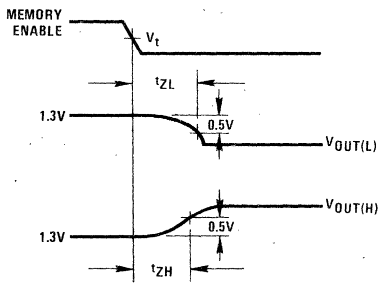


MEMORY ENABLE

t_{LZ} & t_{HZ}



t_{ZL} & t_{ZH}



Note: The pulse generator has the following characteristics: V = 3.0V, t_r = 15 ns, t_f = 5.0 ns, f = 500 kHz, duty cycle = 50%, Z_{OUT} = 50Ω, V_t = 1.3V @ 25°C.

Dual Retriggerable Resettable One Shots

General Description

The DM7853/DM8853 is a dual, retriggerable, resettable monostable multivibrator similar to the DM9602/DM8602 but with a unique input triggering logic.

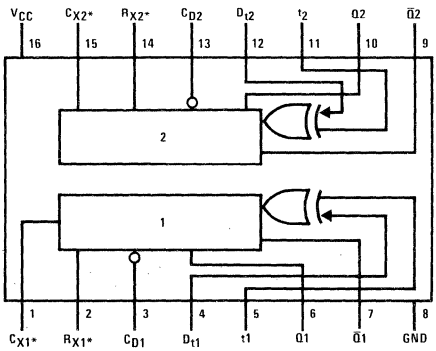
This device has two trigger inputs—a standard input and a delayed input—which are Exclusive OR'ed together. In the dual-edge triggering mode, the two inputs are tied together. On either a positive or negative transition the Exclusive-OR logic is satisfied for a length of time equal to the delay on the delayed input—approximately 15 ns—thus triggering or retriggering the one-shot.

Once fired, the accuracy and performance of the DM7853/DM8853 is identical to that of the DM9602/DM8602.

Features

- 72 ns to ∞ output width range
- Retriggerable 0 to 100% duty cycle
- TTL input gating—leading AND/OR trailing edge triggering
- Complementary TTL outputs
- Pulse width compensated for V_{CC} and temperature variations
- Resettable

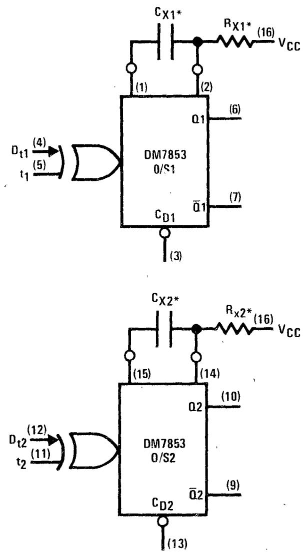
Connection Diagram



*Pins for external timing

7853/8853(J), (N), (W)

Logic Diagrams



*A non-inverting buffer with delay

Truth Tables

TRIGGERING TRUTH TABLE

t	D_t	C_D	OPERATION
L → H	L	H	Trigger
H	H → L	H	Trigger
H → L	H	H	Trigger
L	L → H	H	Trigger
H → L	Same as t	H	Trigger
L → H	Same as t	H	Trigger
X	X	L	Reset

LOADING RULES

INPUTS	LOAD	
	HIGH	LOW
3, 4, 5, 11, 12, 13	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6, 7, 9, 10	16 U.L.	8 U.L.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS(2)		DM7853 MIN	DM7853 TYP(1)	DM7853 MAX	DM8853 MIN	DM8853 TYP(1)	DM8853 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−800			−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA(3)		2.4	3.3		2.4	3.4		V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA(3)			0.2	0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V			10	60		10	60	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V		−1.1	−1.6				mA
			V_I = 0.45V					−1.0	−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, V_{OUT} = 1.0V(3)				−25			−35	mA
I_{CC}	Supply Current	V_{CC} = Max			55	72		55	72	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

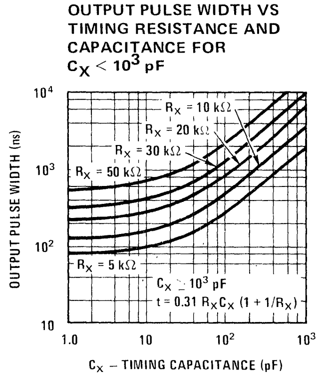
(2) Unless otherwise noted, 10 kΩ resistor placed between R_X and V_{CC} for all tests.

(3) Ground Pin 1 (15) for V_{OL} on Pin 7 (9), or for V_{OH} on Pin 6 (10), or for I_{OS} on Pin 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for V_{OL} on Pin 6 (10), or for V_{OH} on Pin 7 (9), or for I_{OS} on Pin 7 (9).

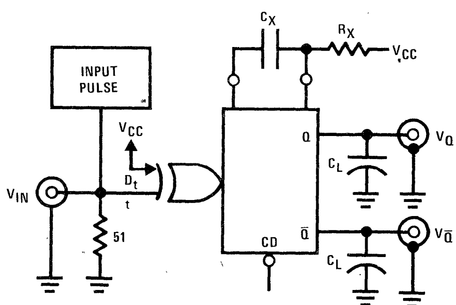
Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM7853 MIN	DM7853 TYP	DM7853 MAX	DM8853 MIN	DM8853 TYP	DM8853 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Standard Trigger Input	Q	C_L = 15 pF, R_X = 5 kΩ, C_X = 0		25	35		25	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Standard Trigger Input	$\bar{Q}$			29	43		29	48	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Delayed Trigger Input	Q			40	53		40	58	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Delayed Trigger Input	$\bar{Q}$			44	61		44	66	ns
$t_{W(MIN)}$	Minimum Possible Output Pulse Q					72	90		72	100	ns
	Minimum Possible Output Pulse $\bar{Q}$					78	100		78	110	ns
t_W	Pulse Width Tolerance			C_X = 1000 pF, R_X = 10 kΩ	3.08	3.42	3.76	3.08	3.42	3.76	μs
C_{STRAY}	Maximum Allowable Wiring Capacitance			Pins (2) and (14) to GND			50			50	pF
R_X	Timing Resistor				5		25	5		50	kΩ

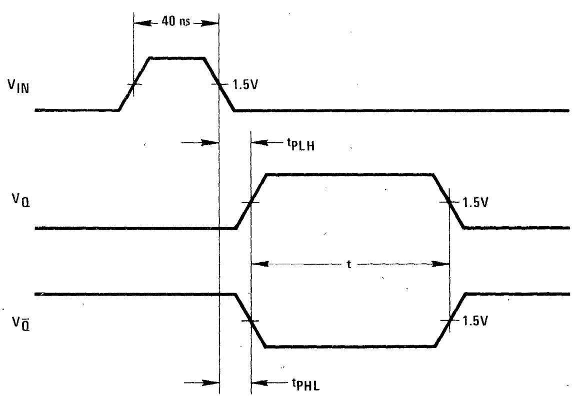
Typical Performance Characteristics



Switching Circuit



Switching Time Waveforms



INPUT PULSES
f = 100 kHz
AMP = 3.0V
WIDTH = 40 ns
$t_r = t_f \leq 10$ ns

TRI-STATE 4-Bit Parallel Binary Multipliers

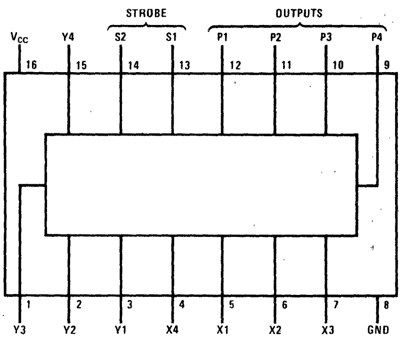
General Description

These circuits are capable of multiplying together two 4-bit binary numbers when used together in pairs. The DM7875A/8875A provides the most significant four bits, and the DM7875B/8875B provides the least significant four bits. Since the largest number that can be obtained by multiplying two 4-bit numbers is 225 (15 x 15), the eight output pins (four from each package) are sufficient to produce this number. Both the multiplier and the multiplicand must be connected to the eight input pins of each device. These devices are pin compatible with the SN54284/74284, and SN54285/74285; but have the advantage that these circuits provide either standard totem-pole TTL or TRI-STATE outputs. A gated two-input strobe control is provided. When either one, or both, of the strobe inputs is raised to a high logic level the outputs are forced into the high-impedance state. Thus, multiple devices may be connected to a common bus line.

Features

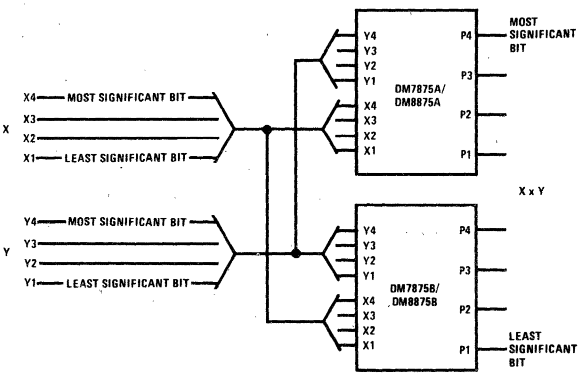
- Pin compatible replacements for
  SN54284/74284 (DM7875A/8875A)
  SN54285/74285 (DM7875B/8875B)
- TRI-STATE outputs
- Typical propagation delay 35 ns

Connection Diagram

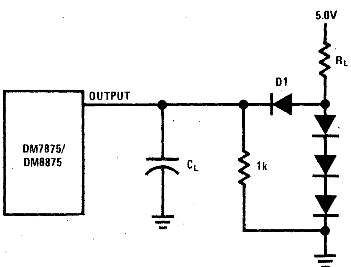


7875A(J); 8875A(J), (N);
7875B(J); 8875B(J), (N)

Typical Application



AC Test Circuit



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM78 75A, 75B MIN	DM78 75A, 75B TYP(1)	DM78 75A, 75B MAX	DM88 75A, 75B MIN	DM88 75A, 75B TYP(1)	DM88 75A, 75B MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−2.0			−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 0.4V			−40			−40	μA
			V_O = 2.4V			40			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.0			−1.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−20		−70	−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max(3)			75	110		75	110	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

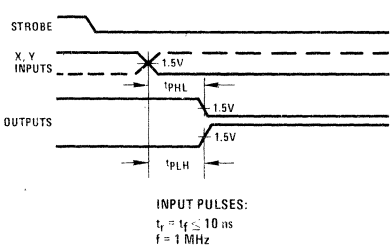
(2) Not more than one output should be shorted at a time.

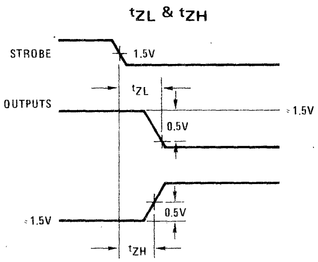
(3) I_{CC} is measured with all inputs grounded.

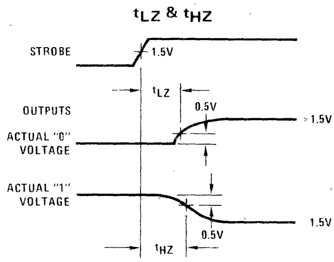
Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS	DM78/88 75A, 75B MIN	DM78/88 75A, 75B TYP	DM78/88 75A, 75B MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output	C_L = 50 pF, R_L = 400Ω		35	60	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output	C_L = 50 pF, R_L = 400Ω		35	60	ns
t_{ZH}	Output Enable Time to High Level			C_L = 50 pF, R_L = 400Ω		20	30	ns
t_{ZL}	Output Enable Time to Low Level			C_L = 50 pF, R_L = 400Ω		20	30	ns
t_{HZ}	Output Disable Time from High Level			C_L = 5 pF, R_L = 400Ω		20	30	ns
t_{LZ}	Output Disable Time from Low Level			C_L = 5 pF, R_L = 400Ω		20	30	ns

Switching Time Waveforms







TRI-STATE BCD to Binary/Binary to BCD Converters

General Description

These circuits are the TRI-STATE versions of the popular BCD to binary and binary to BCD converters, DM74184 and DM74185A respectively. They are derived from the 256-bit ROM, DM8598. Emitter connections are made to provide direct read out of converted codes at outputs Y8 through Y1, as shown in the truth tables. Both converters comprehend the fact that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter. Thus a 6-bit converter is produced in each case, and both devices are cascadable.

An overriding enable input is provided on each converter which, when taken high, inhibits the function, causing all outputs to go into the high-impedance state. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the 185A and all "don't care" conditions of the 184 are programmed high.

DM8898 BCD-TO-BINARY CONVERTERS

The 6-bit BCD-to-binary function of the DM8898 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.
b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the DM8898 is programmed to generate BCD 9's complement or BCD 10's complement. In each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the truth table when the devices are connected as shown.

DM8899 BINARY-TO-BCD CONVERTERS

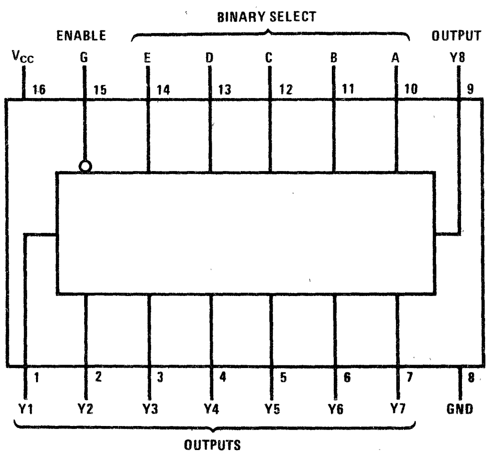
The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

Features

- TRI-STATE versions DM74184, DM74185A
- Typical propagation delay 30 ns

Connection Diagram



8898(N); 8899(N)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM88 98, 99 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−5.2	mA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −5.2 mA		2.4			V
I_{OL}	Low Level Output Current					12	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 12 mA				0.4	V
$I_{O(OFF)}$	Off State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 0.4V			−40	μA
			V_O = 2.4V			40	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max, V_I = 0V			70	99	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM88 98, 99 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Binary Select	Output	C_L = 50 pF, R_L = 400Ω		29	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Binary Select	Output	C_L = 50 pF, R_L = 400Ω		33	50	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Output	C_L = 50 pF, R_L = 400Ω		23	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable	Output	C_L = 50 pF, R_L = 400Ω		29	40	ns
t_{ZH}	Output Enable Time to High Level			C_L = 50 pF, R_L = 400Ω		16	25	ns
t_{ZL}	Output Enable Time to Low Level			C_L = 50 pF, R_L = 400Ω		26	40	ns
t_{HZ}	Output Disable Time from High Level			C_L = 5 pF, R_L = 400Ω		13	20	ns
t_{LZ}	Output Disable Time from Low Level			C_L = 5 pF, R_L = 400Ω		24	36	ns

Truth Tables

BCD-TO-BINARY CONVERTER

BCD WORDS	INPUTS (See Note A)						OUTPUTS (See Note B)				
	E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0 1	L	L	L	L	L	L	L	L	L	L	L
2 3	L	L	L	L	H	L	L	L	L	L	H
4 5	L	L	L	H	L	L	L	L	L	H	L
6 7	L	L	L	H	H	L	L	L	L	H	H
8 9	L	L	H	L	L	L	L	L	H	L	L
10 11	L	H	L	L	L	L	L	L	H	L	H
12 13	L	H	L	L	H	L	L	L	H	H	L
14 15	L	H	L	H	L	L	L	L	H	H	H
16 17	L	H	L	H	H	L	L	H	L	L	L
18 19	L	H	H	L	L	L	L	H	L	L	H
20 21	H	L	L	L	L	L	L	H	L	H	L
22 23	H	L	L	L	H	L	L	H	L	H	H
24 25	H	L	L	H	L	L	L	H	H	L	L
26 27	H	L	L	H	H	L	L	H	H	L	H
28 29	H	L	H	L	L	L	L	H	H	H	L
30 31	H	H	L	L	L	L	L	H	H	H	H
32 33	H	H	L	L	H	L	H	L	L	L	L
34 35	H	H	L	H	L	L	H	L	L	L	H
36 37	H	H	L	H	H	L	H	L	L	H	L
38 39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	Z	Z	Z	Z	Z

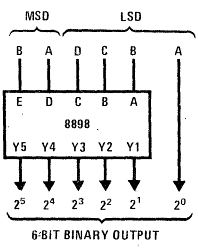
H = High Level, L = Low Level,
X = Don't Care, Z = High Impedance

BCD 9's OR BCD 10's COMPLEMENT CONVERTER

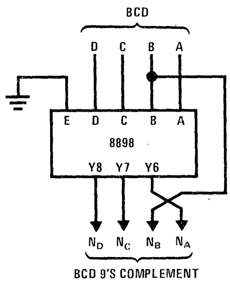
BCD WORD	INPUTS (See Note C)						OUTPUTS (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	Z	Z	Z

H = High Level, L = Low Level,
X = Don't Care, Z = High Impedance

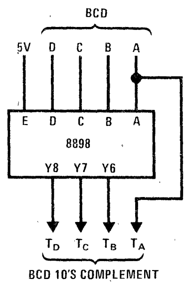
6-BIT CONVERTER



BCD 9's COMPLEMENT CONVERTER



BCD 10's COMPLEMENT CONVERTER



Notes:

(A) Input conditions other than those shown produce highs at outputs Y1 through Y5.
(B) Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.
(C) Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.
(D) Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

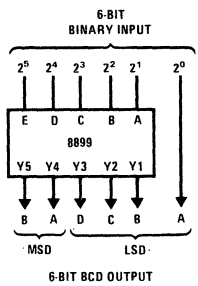
Truth Tables (Continued)

BINARY-TO-BCD CONVERTER

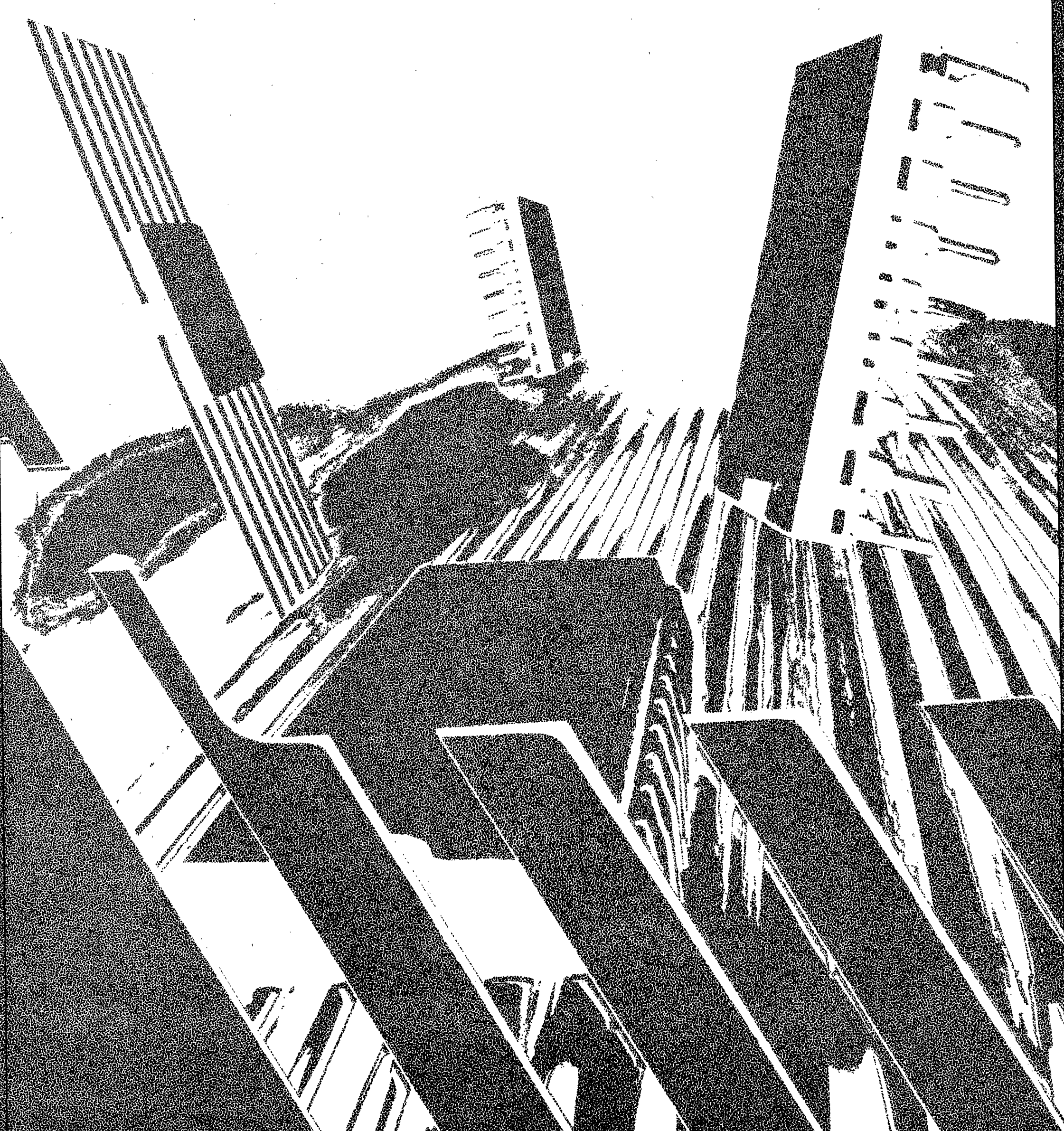
BINARY WORDS	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2 3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4 5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12 13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14 15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22 23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24 25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26 27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28 29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30 31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32 33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34 35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36 37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38 39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42 43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44 45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46 47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48 49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50 51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52 53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54 55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56 57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58 59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60 61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62 63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

6-BIT CONVERTER



National Semiconductor
ADDITIONAL DEVICES
Section 4



RATINGS		DTL	2502 SERIES	72XX/ 82XX	9000C SERIES	93XX/ 83XX	96XX/ 86XX	UNITS
Maximum Allowable Supply Voltage		8	7	7	7	7	7	V
Guaranteed Operating Supply Voltage Range	Mil	N/A	4.50 to 5.50		N/A	4.50 to 5.50		V
	Coml	5	4.75 to 5.25		4.75–5.25	4.75 to 5.25		
Maximum Input Voltage		5.5	5.5	5.5	5.5	5.5	5.5	V
Maximum Voltage to Open-Collector Outputs		8	7	7	7	7	7	V
Operating Free-Air Temperature Range	Mil	N/A	−55 to +125		N/A	−55 to +125		°C
	Coml	0 to +75	0 to +70		0 to +75			
Storage Temperature Range		−65 to +150						°C

Additional Devices — Table of Contents

DTL Circuits

General Description

The National Semiconductor family of DTL is a complete line of compatible monolithic integrated circuits designed to operate at medium speed with medium power dissipation and high fan-out. The DTL family is available in 14-pin epoxy B or ceramic dual-in-line packages for operation over the 0°C to +75°C temperature range.

The DTL line is composed of a variety of NAND gates that allow complete design flexibility. The gates are available with either 6k pull-up resistors for low power dissipation, or 2k pull-up resistors for increased speed. The gate outputs can be wired together to achieve the wired-OR function.

The NAND gates are complemented with the DM932 and DM957 buffers which provide higher fan-out; the DM944 and DM958 power gates which have an open collector, and the DM933 extender which allows increased fan-in for both buffers and DM930 and DM961 gates.

The flip-flops in this family are of the direct coupled master-slave type, with direct clear and direct set lines. The dual flip-flops include ones with either common or separate clocks.

The DM945 and DM948 are R-S flip-flops which can be externally cross coupled to perform in the JK mode. They are of the master-slave type with output buffers to provide isolation from the output load. These flip-flops feature both asynchronous set and clear lines. The DM945 has a 6k pull-up resistor and the DM948 has a 2k pull-up resistor.

The DM9093 and DM9094 are dual JK flip-flops of the DM945 and DM948 variety respectively. Both flip-flops have separate clocks and no asynchronous clear lines.

The DM9097 and DM9099 are dual JK flip-flops of the DM948 and DM945 variety respectively. Both flip-flops have common clocks and both asynchronous set and clear lines.

The DM930 series is directly compatible with the TTL devices manufactured by National and can be used in conjunction with them in those portions of a system where speed is not the main consideration.

Features

- **NAND Gates**
  - DM930, DM961 - dual four input gates with expanders
  - DM935, DM936, DM937 - hex inverters
  - DM946, DM949 - quad two input gates
  - DM962, DM963 - triple three input gates
  - DM1800, DM1801 - dual five input gates
- **Buffers/Extenders**
  - DM932 - dual four input buffer with expander
  - DM933 - dual four-input extender
  - DM944 - dual four input power gate with expander
  - DM957 - quad two input buffer
  - DM958 - quad two input power gate
- **Flip-Flops**
  - DM945, DM948 - RS flip-flops
  - DM9093, DM9094, DM9097, DM9099 - dual JK flip-flops

Truth Tables

SYNCHRONOUS TRUTH TABLE

t_n				$t_n + 1$
S1 Pin 3	S2 Pin 4	C1 Pin 12	C2 Pin 11	Q Pin 6
L	X	L	X	Q_n
L	X	X	L	Q_n
X	L	L	X	Q_n
X	L	X	L	Q_n
L	X	H	H	L
X	L	H	H	L
H	H	L	X	H
H	H	X	L	H
H	H	H	H	*

* — Indeterminate State
X — Don't Care

ASYNCHRONOUS TRUTH TABLE

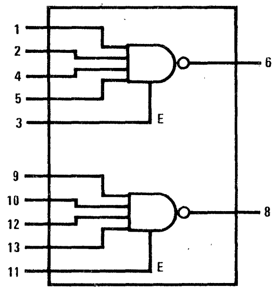
S_D Pin 10	C_D Pin 5	Q Pin 6	$\bar{Q}$ Pin 9
H	H	NC	NC
L	H	H	L
H	L	L	H
L	L	H	H

JK TRUTH TABLE

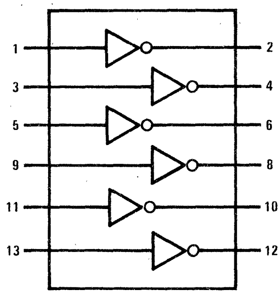
t_n		$t_n + 1$
S1 Pin 3	C1 Pin 12	Q Pin 6
L	L	Q_n
H	L	H
L	H	L
H	H	$\bar{Q}_n$

(Connect S2 to $\bar{Q}$, C2 to Q) Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs, and are independent of all other inputs.

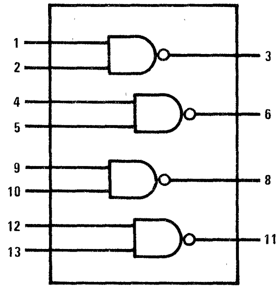
Connection and Logic Diagrams



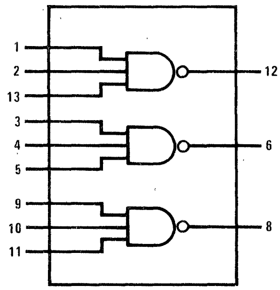
930(J), (N); 932(J), (N); 944(J), (N); 961(J), (N); 1800(J), (N); 1801(J), (N)



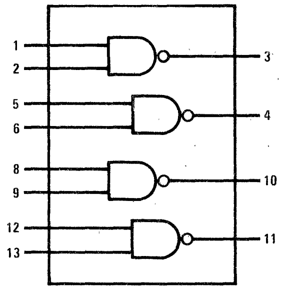
935(J), (N); 936(J), (N); 937(J), (N)



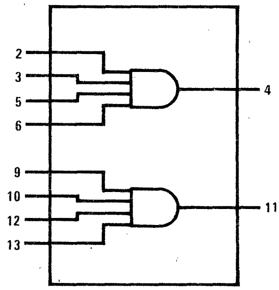
946(J), (N); 949(J), (N)



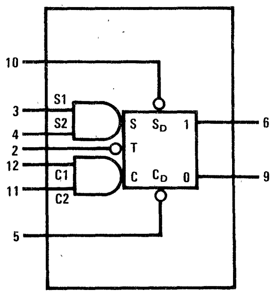
962(J), (N); 963(J), (N)



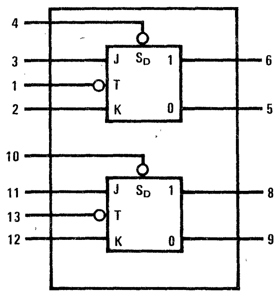
957(J), (N); 958(J), (N)



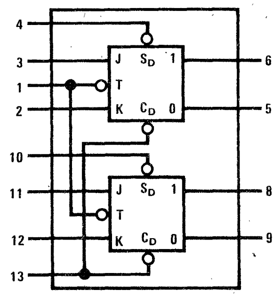
933(J), (N)



945(J), (N); 948(J), (N)



9093(J), (N); 9094(J), (N)



9097(J), (N); 9099(J), (N)

Electrical Characteristics (V_{CC} = 5.0V)

	PARAMETER	CONDITIONS		DM930, DM935, DM936, DM937, DM946 DM949, DM961, DM962, DM963, DM1800, DM1801						UNITS
				0°C		25°C		75°C		
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{CEX}	Output Leakage Current	V_I = 0, V_O = 5V	2k Gates				100			μA
			6k Gates				100			
V_{OH}	High Level Output Voltage(1)	V_{IL} = Max, I_{OH} = Max		2.6		2.6		2.5		V
V_{OL}	Low Level Output Voltage	V_I = V_{IH}, I_{OL} = Max			0.45		0.45		0.50	V
I_{IH}	High Level Input Current (1)	V_I = V_R			5		5		10	μA
I_{IL}	Low Level Input Current	V_I = V_F			−1.40		−1.40		−1.33	mA
I_{OS}	Short Circuit Output Current	V_I = 0	2k Gates			−1.85	−3.90			mA
			6k Gates		1.30	−0.61	−1.30		−1.25	
I_{CC1}	Supply Current	V_{CC} = 5V, V_I = V_R	2k Gates				5.9			mA
			6k Gates				4			
I_{CC2}	Supply Current	V_{CC} = 8V, V_I = 0					4			mA
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 30 pF, R_L = 3.9 kΩ	2k Gates			15	60			ns
			6k Gates			25	80			
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 50 pF, R_L = 400Ω	2k Gates			10	30			ns
			6k Gates			10	30			

Notes
(1) Applies to all gates except DM935.

Test Conditions

GATES

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_R VOLTS	V_F VOLTS	V_{CEX} VOLTS	(6k) I_{OL} (mA)	(2k) I_{OL} (mA)	(6k) I_{OH} (mA)	(2k) I_{OH} (mA)
0°C	2.0	1.2	4.0	0.45	–	12.0	11.0	−0.12	−0.5
+25°C	1.9	1.1	4.0	0.45	5.0	12.0	11.0	−0.12	−0.5
+75°C	1.8	0.95	4.0	0.50	–	11.4	10.4	−0.12	−0.5

Electrical Characteristics (V_{CC} = 5.0V)

	PARAMETER	CONDITIONS		DM932, DM933, DM944, DM957, DM958						UNITS
				0°C		25°C		75°C		
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$I_{IL} = I_{FD}$	933	0.75	0.90	0.68	0.82	0.60	0.75	V
I_{CEX}	Output Leakage Current	$V_I = 0$, $V_O = 5V$	932, 957				100			µA
			944, 958		25		100		200	
V_{OH}	High Level Output Voltage	$V_I = V_{IL}$, I_{OH} = Max	932, 957	2.6		2.6		2.5		V
V_{OL}	Low Level Output Voltage	$V_I = V_{IH}$, I_{OL} = Max	All Except 933		0.45		0.45		0.50	V
I_{IH}	High Level Input Current	$V_I = V_R$	933		5		5		10	µA
			Others		5		5		10	
I_{IL}	Low Level Input Current	$V_I = V_F$	All Except 933		−1.40		−1.40		−1.33	mA
I_{OS}	Short Circuit Output Current	$V_I = 0$	932, 957		−16		−16		−14	mA
I_{CC1}	Supply Current	$V_{CC} = 5V$, $V_I = V_R$	932				30.0			mA
			944				22.5			
			957				60.0			
			958				4.5			
I_{CC2}	Supply Current	$V_{CC} = 8V$, $V_I = 0$	All Except 933				4			mA
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 500 pF, R_L = 510Ω	932, 957			25	80			ns
		C_L = 20 pF, R_L = 510Ω	944, 958			15	50			
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 500 pF, R_L = 150Ω	932, 957			15	40			ns
		C_L = 100 pF, R_L = 150Ω	944, 958			10	35			

Test Conditions

BUFFERS/EXTENDERS

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_R VOLTS	V_F VOLTS	V_{CEX} VOLTS	I_{FD} mA	932 957 I_{OL} (mA)	944 958 I_{OL} (mA)	932 957 I_{OH} (mA)
0°C	2.0	1.2	4.0	0.45	—	−2	36	40	−2.0
+25°C	1.9	1.1	4.0	0.45	5.0	−2	36	40	−2.5
+75°C	1.8	0.95	4.0	0.50	—	−2	34	36	−3.0

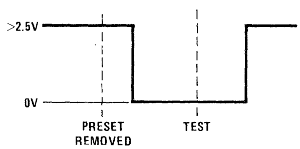
Electrical Characteristics (V_{CC} = 5.0V)

	PARAMETER	CONDITIONS			DM945, DM948, DM9093, DM9094 DM9097, DM9099 0°C MIN	0°C MAX	25°C MIN	25°C MAX	75°C MIN	75°C MAX	UNITS
I_{CEX}	Output Leakage Current	V_I = 0, V_O = 5V		945, 948				100			μA
V_{OH}	High Level Output Voltage	V_I = V_{IL} I_{OH} = Max	Data	945, 948	2.6		2.6		2.5		V
			Set, Reset	945, 948	2.6		2.6		2.6		
			All	9093, 9094 9097, 9099	2.6		2.6		2.5		
V_{OL}	Low Level Output Voltage	V_I = V_{IH}, I_{OL} = Max		All		0.45		0.45		0.50	V
I_{IH}	High Level Input Current	V_I = V_R	Data	945, 948		5.0		5.0		10.0	μA
			Set, Reset	945, 948		5.0		5.0		10.0	
			Clock	945, 948		30		30		40	
				9093, 9094		20		20		30	
				9097, 9099		40		40		60	
			Clear	9097, 9099		10		10		20	
			All Except Clocks, and Direct Clear on 9097, 9099	9093, 9094 9097, 9099		5.0		5.0		10.0	
I_{IL}	Low Level Input Current	V_I = V_F	Data	All		−0.95		−0.95		−0.90	mA
			Set, Reset	945, 948		−2.8		−2.8		−2.67	
			Direct Set	9093, 9094 9097, 9099		−2.8		−2.8		−2.67	
			Clock	945		−2.8		−2.8		−2.66	
				948, 9093 9094		−2.8		−2.8		−2.67	
			Clock, Direct Clear	9097, 9099		−5.6		−5.6		−5.34	
I_{OS}	Short Circuit Output Current	V_I = 0		2k	−1.77	−4.2	−1.77	−4.2	−1.60	−4.0	mA
				6k	−0.59	−1.41	−0.59	−1.41	−0.55	−1.38	
I_{CC1}	Supply Current	V_{CC} = 5V (Inputs Open)		945				14			mA
				948				17			
				9093, 9099				28			
				9094, 9097				34			
I_{CC2}	Supply Current	V_{CC} = 8V, V_I = 0		945				18			mA
				948				23			
				9093, 9099				36			
				9094, 9097				45			
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 30 pF, R_L = 2 kΩ		2k			25	75			ns
				6k			25	100			
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 50 pF, R_L = 330Ω					15	55			ns

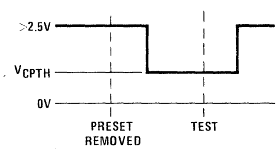
Test Conditions

FLIP-FLOPS

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_R VOLTS	V_F VOLTS	V_{CEX} VOLTS	945 9093 9099 (6k) V_{CPTH} (VOLTS)	948 9094 9097 (2k) V_{CPTH} (VOLTS)	945 9093 9099 (6k) I_{OL} (mA)	948 9094 9097 (2k) I_{OL} (mA)	945 9093 9099 (6k) I_{OH} (mA)	948 9094 9097 (2k) I_{OH} (mA)
0°C	2.0	1.2	4.0	0.45	–	1.15	1.30	16.8	15.4	−0.12	−0.5
+25°C	1.9	1.1	4.0	0.45	5.0	0.95	1.15	16.8	15.4	−0.12	−0.5
+75°C	1.8	0.95	4.0	0.50	–	0.65	0.85	16.0	14.6	−0.12	−0.5



CP_a



CP_b

Successive Approximation Registers

General Description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary (in combination with a D/A converter) to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable.

The DM2503 has 8 bits and is expandable without serial capability.

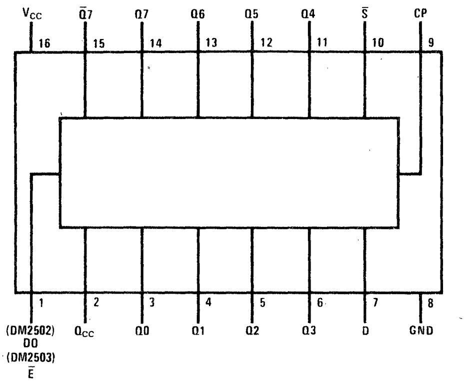
The DM2504 has 12 bits with serial capability and expandability.

All three devices are available in ceramic DIP, ceramic flatpak, and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

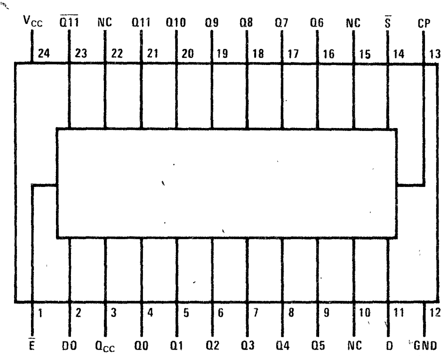
Features

- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

Connection Diagrams



2502(J), (W); 2502C(J), (N), (W);
2503(J), (W); 2503C(J), (N), (W)



2504(J), (F); 2504C(J), (N), (F)

Truth Table

TIME	INPUTS			OUTPUTS(1)									
t_n	D	$\overline{S}$	$\overline{E}$(2)	D0(3)	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

Notes

(1) Truth table for DM2504 is extended to include 12 outputs.

(2) Truth table for DM2502 does not include $\overline{E}$ column or last line in truth table shown.

(3) Truth table for DM2503 does not include D0 column.

H = High Level
L = Low Level
X = Don't Care
NC = No Change

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM25 02, 02C MIN	TYP(1)	MAX	DM25 03, 03C MIN	TYP(1)	MAX	DM25 04, 04C MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5			−1.5	V
I_{OH}	High Level Output Current					−480			−480			−480	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −480μA		2.4	3.6		2.4	3.6		2.4	3.6		V
I_{OL}	Low Level Output Current					9.6			9.6			9.6	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 9.6 mA			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max	CP Input		6	40		6	40		6	40	μA
		V_I = 2.4V	D, $\overline{E}$, $\overline{S}$ Inputs		12	80		12	80		12	80	
I_{IL}	Low Level Input Current	V_{CC} = Max	CP, $\overline{S}$ Inputs		−1.0	−1.6		−1.0	−1.6		−1.0	−1.6	mA
		V_I = 0.4V	D, $\overline{E}$ Inputs		−2.0	−3.2		−2.0	−3.2		−2.0	−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−10	−20	−45	−10	−20	−45	−10	−20	−45	mA
I_{CC}	Supply Current	V_{CC} = Max	Military		65	85		60	80		90	110	mA
			Commercial		65	95		60	90		90	124	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER			FROM	TO	CONDITIONS	DM25 02, 02C MIN	TYP	MAX	DM25 03, 03C MIN	TYP	MAX	DM25 04, 04C MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 400Ω	15	21		15	21		15	21		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		CP	Output		10	26	38	10	26	38	10	26	38	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		CP	Output		10	18	28	10	18	28	10	18	28	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		$\overline{E}$	Q7 (Q11) CP High $\overline{S}$ Low			N/A			13	19		13	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		$\overline{E}$	Q7 (Q11) CP High $\overline{S}$ Low			N/A			16	24		16	24	ns
t_W	Width of Clock Pulse	Low Level				42	30		42	30		42	30		ns
		High Level				24	17		24	17		24	17		
t_{SETUP}	Setup Time	$\overline{S}$ Input				16	9		16	9		16	9		ns
		D Input				8	4		8	4		8	4		

Application Information

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator 1/2 full range + 1/2 LSB and using the complement of the MSB ($\overline{Q}$7 or $\overline{Q}$11) with a binary D/A converter. Offset binary is used in the same manner but with the MSB (Q7 or Q11). BCD D/A converters can be used with the addition of illegal code suppression logic.

ACTIVE HIGH OR ACTIVE LOW LOGIC

The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start signal resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below ±1/2 LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +1/2 LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −1/2 LSB.

Definition of Terms (See Timing Diagram)

CP: The clock input of the register.

D: The serial data input of the register.

DO: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_i i = 7 (11) to 0: The outputs of the register.

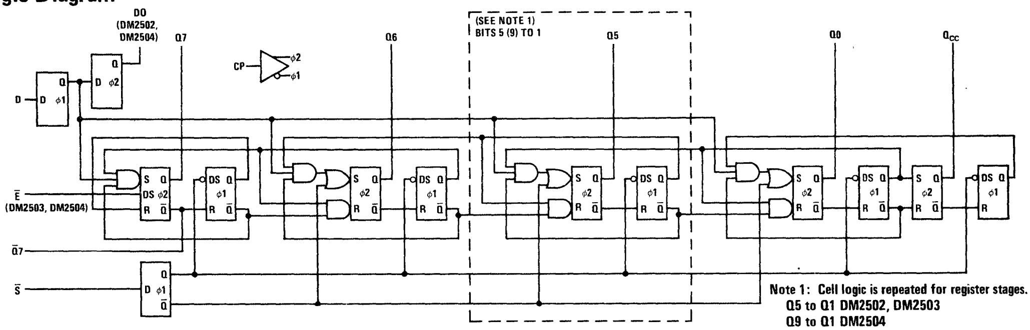
Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

Q7 (11): The true output of the MSB of the register.

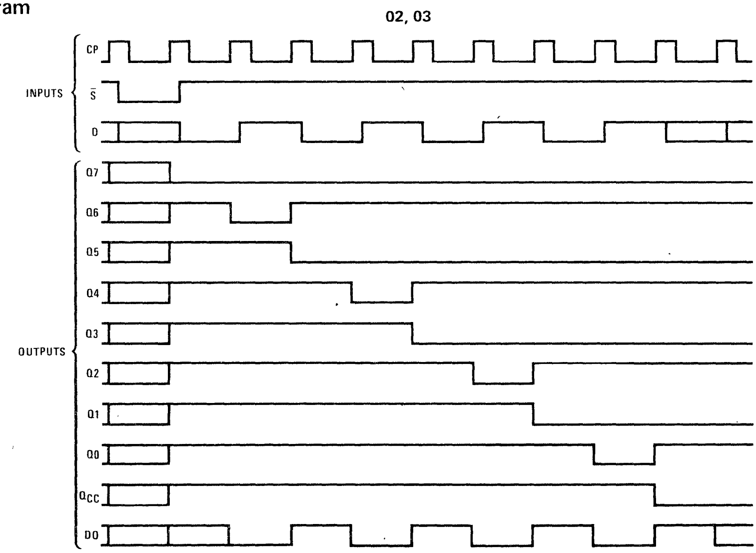
$\overline{Q}$7 (11): The complement output of the MSB of the register.

$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

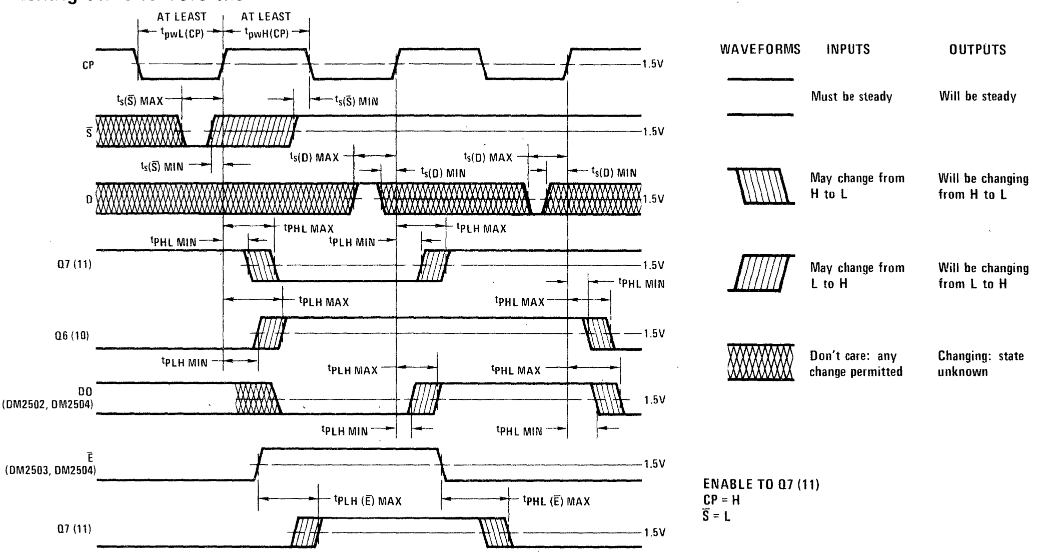
Logic Diagram



Timing Diagram



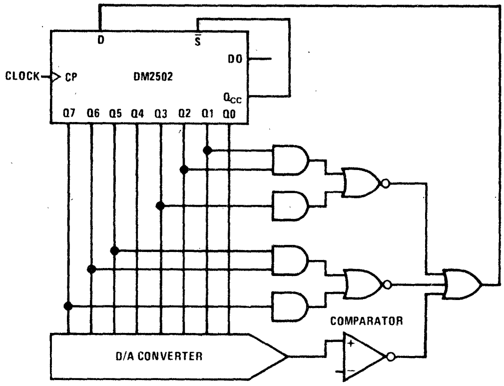
Switching Time Waveforms



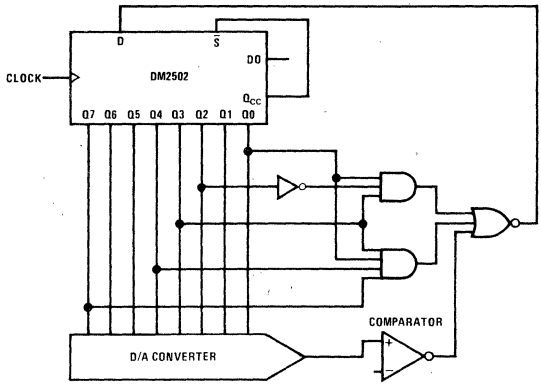
Typical Applications

BCD ILLEGAL CODE SUPPRESSION

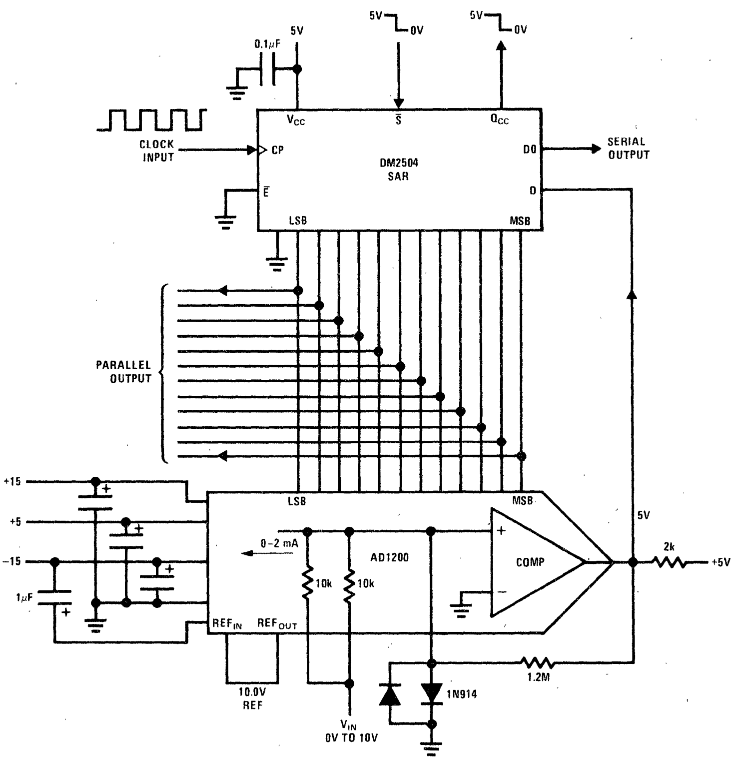
ACTIVE HIGH



ACTIVE LOW



HIGH SPEED 12-BIT A/D CONVERTER



Presettable Counters

General Description

These high-speed counters consist of four dc-coupled, master-slave flip-flops which are internally interconnected to provide divide-by-two, divide-by-four, divide-by-five, divide-by-six, divide-by-eight, divide-by-ten, divide-by-twelve, or divide-by-sixteen operations. The counters are fully programmable; that is, the outputs may be preset to any number by placing a low logic level on the count/load input and entering the desired number at the data inputs. Transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters also feature a direct clear which, when placed at a low logic level, sets all outputs low regardless of the conditions on the clocks.

Typical Count Configurations

DM7280/DM8280, DM7290/DM8290

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

DM7281/DM8281, DM7291/DM8291

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table for the DM7281/8281, DM7291/8291.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

DM7288/DM8288

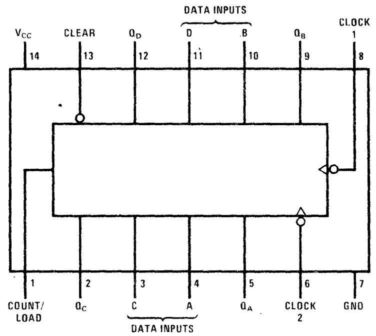
The 8288 divide-by-twelve counter is a four-bit subsystem consisting of divide-by-two and divide-by-six counters in a 14-pin package. For divide-by-twelve operation, output A is connected externally to the clock-2 input.

Features

- Direct replacements Signetics 8280, 8281, 8288, 8290, 8291
- Pin-for-pin with popular Series 54 counters:
  8280, 8290—54176, 54196
  8281, 8291—54177, 54197
- Fully programmable
- Independent clear input
- Performs BCD, bi-quinary, or quinary counting
- Output Q_A maintains full fan-out while driving clock 2

TYPE	TYPICAL CLOCK FREQUENCY CLOCK 1	TYPICAL CLOCK FREQUENCY CLOCK 2	TYPICAL POWER DISSIPATION
7280/8280 7281/8281 7288/8288	50 MHz	25 MHz	150 mW
7290/8290 7291/8291	50 MHz	25 MHz	150 mW

Connection Diagram



7280(J), (W); 8280(J), (N), (W); 7281(J), (W); 8281(J), (N), (W); 7288(J), (W); 8288(J), (N), (W); 7290/8290(J), (N), (W); 7291/8291(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM72/82 80, 81 MIN	80, 81 TYP(1)	80, 81 MAX	88 MIN	88 TYP(1)	88 MAX	90, 91 MIN	90, 91 TYP(1)	90, 91 MAX	UNITS
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5			−1.5	V
I_{OH}	High Level Output Current					−800			−800			−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −800μA		2.6			2.6			2.6			V
I_{OL}	Low Level Output Current					16			16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 4.5V	Count/Load, Data			40			40			40	μA
			Clear, Clock 1			80			80			80	
			Clock 2 (8281, 8291)			40			N/A			80	
			Clock 2 (Others)			80			80			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Count/Load			−1.6			−1.6			−1.6	mA
			Data			−1.2			−1.2			−1.2	
			Clear			−3.2			−3.2			−2.8	
			Clk 1, Clk 2 (8280, 8290)			−3.2			−3.2			−4.8	
			Clock 2 (Others)			−1.6			−1.6			−2.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−18		−57	−18		−57	−18		−57	mA
I_{CC}	Supply Current	V_{CC} = Max			30	45		30	45		30	48	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS		DM72/82 80, 81 MIN	TYP	MAX	88 MIN	TYP	MAX	90, 91 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency	Clock 1	Q_A			35	50		35	50		40	50		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 1	Q_A				9	13		9	13		9	13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 1	Q_A				11	17		11	17		11	17	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 2	Q_B				12	18		12	18		12	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 2	Q_B				14	21		14	21		14	21	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 2	Q_C				27	41		27	41		24	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 2	Q_C				34	51		34	51		28	42	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 2	Q_D	8280, 8288, 8290	C_L = 15 pF, R_L = 400Ω		13	20		13	20		14	21	ns
				8281, 8291			44	66		N/A			36	54	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 2	Q_D	8280, 8288, 8290			17	26		17	26		16	23	ns
				8281, 8291			50	75		N/A			42	63	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any Data Input	Any Output				19	29		19	29		16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Any Data Input	Any Output				31	46		31	46		25	38	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Load	Any Output				29	43		29	43		22	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Load	Any Output				32	48		32	48		24	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Any Output				32	48		32	48		25	37	ns
t_W	Pulse Width				Clock 1	14			14			14			ns
					Clock 2	28			28			28			
					Clear	25			25			25			
					Load	20			20			20			
t_{HOLD}	Input Hold Time				High-Level Data	$t_{W(LOAD)}$			$t_{W(LOAD)}$			$t_{W(LOAD)}$			ns
					Low-Level Data	$t_{W(LOAD)}$			$t_{W(LOAD)}$			$t_{W(LOAD)}$			
t_{SETUP}	Input Setup Time				High-Level Data	15			15			10			ns
					Low-Level Data	20			20			15			
t_{ENABLE}	Count Enable Time					25			25			30			ns

Truth Tables

80, 90
DECADE (BCD)
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

80, 90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

81, 91
TRUTH TABLE
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

88
TRUTH TABLE

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H

H = High Level, L = Low Level

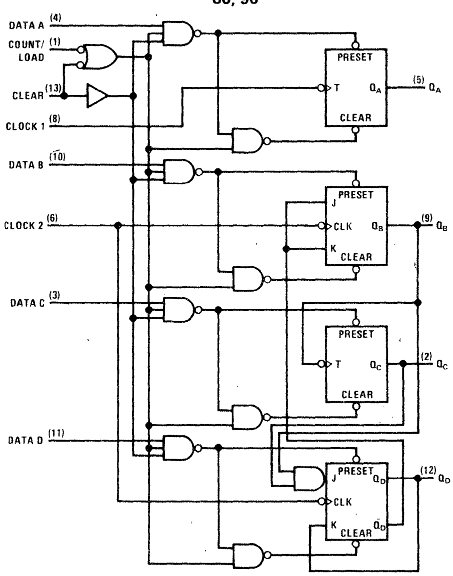
Notes:

(A) Output Q_A connected to clock 2 input.

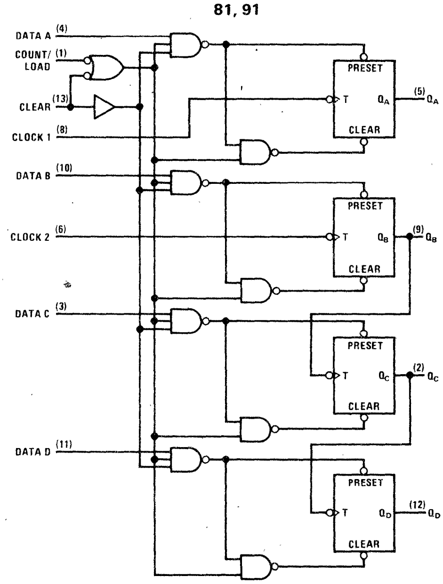
(B) Output Q_D connected to clock 1 input.

Logic Diagrams

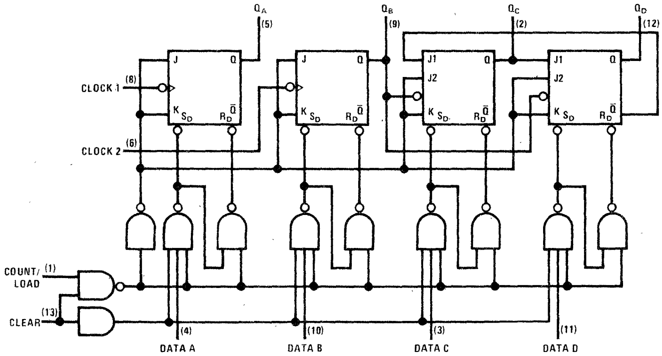
80, 90



81, 91



88



Gates/Inverters

General Description

DM9000C series devices are designed to be used in existing systems as replacements for Fairchild 9000-type circuits. These DM9000C circuits offer several significant advantages over 9000 type circuits, some of which are:

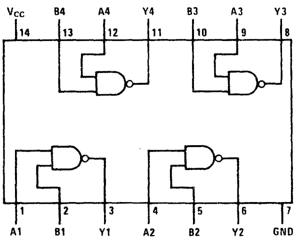
- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.
- Power dissipation of DM9000C circuits is in most cases lower than that for the equivalent 9000 type.

DM9000C circuits are characterized for operation over the industrial temperature range of 0°C to 75°C.

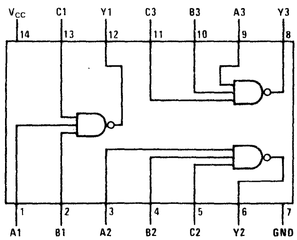
For new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Included are several families of compatible TTL circuits offering a choice of specific performance ranges (see Sections 1 and 2); and are designed to serve any application from industrial numerical controllers or high-speed computers, to sophisticated high-reliability aerospace and defense systems. Series 54/74 pin-for-pin equivalents are available for the following SSI types:

DM9000C SERIES	EQUIVALENT SERIES 74
DM9002C	DM7400
DM9003C	DM7410
DM9004C	DM7420
DM9005C	DM7450
DM9006C	DM74H60
DM9008C	DM74H53
DM9009C	DM7440
DM9012C	DM7403
DM9016C	DM7404
DM9024C	DM74109

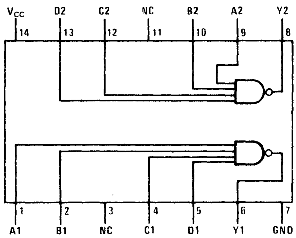
Connection Diagrams



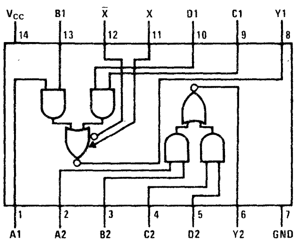
9002C(J), (N); 9012C(J), (N)



9003C(J), (N)

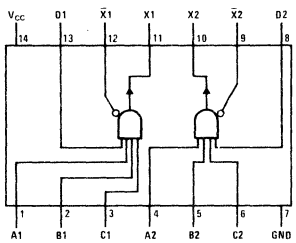


9004C(J), (N); 9009C(J), (N)

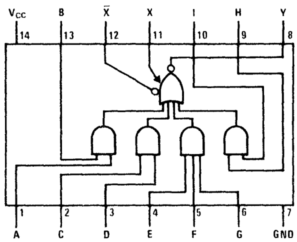


X = Output of Expander

9005C(J), (N)

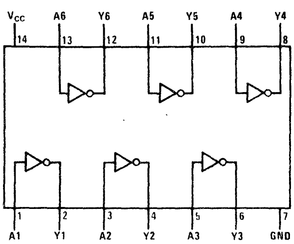


9006C(J), (N)



X = Output of Expander

9008C(J), (N)



9016C(J), (N)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM90 02C, 03C 04C, 16C MIN	02C, 03C 04C, 16C MAX	05C EXPANDABLE GATE MIN	05C EXPANDABLE GATE MAX	05C NON-EXPANDABLE GATE MIN	05C NON-EXPANDABLE GATE MAX	06C, 08C MIN	06C, 08C MAX	09C MIN	09C MAX	12C MIN	12C MAX	UNITS
V_{IH}	High Level Input Voltage	0°C	1.9		1.9		1.9		1.9		1.9		1.9		V
		25°C	1.8		1.8		1.8		1.8		1.8		1.8		V
		75°C	1.6		1.6		1.6		1.6		1.6		1.6		V
V_{IL}	Low Level Input Voltage			0.85		0.85		0.85		0.85		0.85		0.85	V
V_I	Input Clamp Voltage	V_{CC} = 4.75V, I_I = −12 mA		−1.5		−1.5		−1.5		−1.5		−1.5		−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.75V, V_{IL} = 0.85V, V_{OH} = 5.5V		−1.2		−1.2		−1.2		−1.2		−3.6		0.25	mA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, V_{IL} = 0.85V, I_{OH} = −1.2 mA	2.4		2.4		2.4		2.4				N/A		V
		V_{CC} = 4.75V, V_{IL} = 0.85V, I_{OH} = −3.6 mA									2.4		N/A		V
I_{OL}	Low Level Output Current			50		50		50		50		100		50	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 5.25V, V_{IH} = Min, I_{OL} = 16 mA		0.45		0.45		0.45		0.45				0.45	V
		V_{CC} = 5.25V, V_{IH} = Min, I_{OL} = 48 mA										0.45			V
		V_{CC} = 4.75V, V_{IH} = Min, I_{OL} = 14.1 mA		0.45		0.45		0.45		0.45				0.45	V
		V_{CC} = 4.75V, V_{IH} = Min, I_{OL} = 42.3 mA										0.45			V
I_{IH}	High Level Input Current	V_{CC} = 5.25V, V_I = 4.5V, Other Inputs at Ground		60		90		60		90		120		60	μA
I_{IL}	Low Level Input Current	V_I = 0.45V, Other Inputs at 5.25V, V_{CC} = 5.25V		−1.6		−2.4		−1.6		−2.4		−3.2		−1.6	mA
		V_I = 0.45V, Other Inputs at 5.25V, V_{CC} = 4.75V		−1.41		−2.12		−1.41		−2.12		−2.82		−1.41	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.25V(1)	−18	−55	−20	−70	−20	−70	−40	−100	−20	−70	N/A		mA
I_{CCH}	Supply Current, All Outputs High	V_{CC} = 5V		1.7		5.1		3.4		10.2		3.4		1.7	mA
I_{CCL}	Supply Current, All Outputs Low	V_{CC} = 5V		6.1		13.6		7.7		17.7		14.6		6.1	mA
ΔI_{CCH}	ΔSupply Current Additional Supply Current when one DM9006C Extender is connected to a DM9005C Gate in the Logical "1" State	V_{CC} = 5V		N/A		2.05		N/A		2.05		N/A		N/A	mA
ΔI_{CCL}	Additional . . . . in the Logical "0" State	V_{CC} = 5V		N/A		2.54		N/A		2.54		N/A		N/A	mA
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 400Ω (2)(3), V_{CC} = 5V, T_A = 25°C	3	13	3	15	3	12	3	15	3	17	3	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 400Ω (2)(3), V_{CC} = 5V, T_A = 25°C	3	15	3	12	3	14	3	12	2	13	3	15	ns

Notes

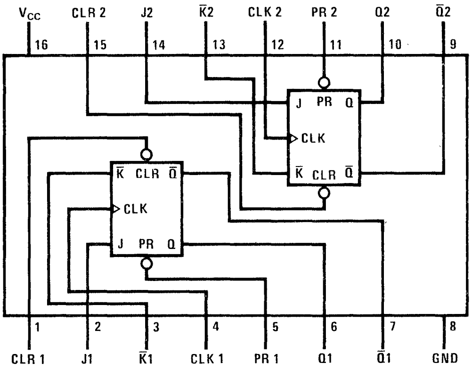
(1) Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

(2) For testing t_{PLH} of DM9012C, R_L = 4 kΩ.

(3) t_{PLH} and t_{PHL} for DM9006C = 4 ns max. additional, as measured through the DM9005C.

Dual J-K Flip-Flops with Preset and Clear

Connection Diagram



9024/8024(J), (N), (W)

Truth Table

24

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}0$

H = High Level (Steady State), L = Low Level (Steady State),
X = Don't Care
↑ = Transition from low to high level
Q0 = The level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable. That is, it will not persist when preset and clear inputs return to their inactive (high) level.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		CONDITIONS			DM90 24 MIN	DM90 24 MAX	DM80 24 MIN	DM80 24 MAX	UNITS
V_{IH}	High Level Input Voltage				T_A = Min	2.0		1.9		V
					T_A = 25°C	1.7		1.8		V
					T_A = Max	1.4		1.6		V
V_{IL}	Low Level Input Voltage						0.9		0.85	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5		−1.5	V
I_{OH}	High Level Output Current						−1.2		−1.2	mA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1.2 mA			2.4		2.4		V
I_{OL}	Low Level Output Current						12.4		14.1	mA
V_{OL}	Low Level Output Voltage		V_{IH} = Min V_{IL} = Max	V_{CC} = Min	I_{OL} = 12.4 mA		0.40			V
				V_{CC} = Min	I_{OL} = 14.1 mA				0.45	V
				V_{CC} = Max	I_{OL} = 16 mA		0.40		0.45	V
I_{IH}	High Level Input Current	J, K, $\overline{J}$ or $\overline{K}$	V_{CC} = Max, V_I = 4.5V Other Inputs at Gnd	T_A = 25°C and 125°C (DM90) T_A = 25°C and 75°C (DM80)			60		60	μA
		Clock					120		120	μA
		Preset					120		120	μA
		Clear					240		240	μA
I_{IL}	Low Level Input Current	J, K, $\overline{J}$ or $\overline{K}$	V_I = 0.40V (DM90) V_I = 0.45V (DM80) Other Inputs at 4.5V	V_{CC} = Max			−1.6		−1.6	mA
		Clock		V_{CC} = Max			−3.2		−3.2	mA
		Preset		V_{CC} = Max			−3.2		−3.2	mA
		Clear		V_{CC} = Max			−4.8		−4.8	mA
		J, K, $\overline{J}$ or $\overline{K}$		V_{CC} = Min			−1.24		−1.41	mA
		Clock		V_{CC} = Min			−2.48		−2.82	mA
		Preset		V_{CC} = Min			−2.48		−2.82	mA
		Clear		V_{CC} = Min			−3.72		−4.23	mA
I_{OS}	Short Circuit Output Current		V_{CC} = Max(1)			−30	−85	−30	−85	mA
I_{CC}	Supply Current		V_{CC} = 5V, T_A = 25°C(2)				28		28	mA

Notes

(1) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

(2) I_{CC} is measured with all outputs open, first with preset at 4.5V and all other inputs grounded, then with clear at 4.5V and all other inputs grounded.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Parameter			From (Input)	To (Output)	Conditions	DM90/8024 Min	Typ	Max	Units
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 400Ω	30	40		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Preset	Q			9	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Preset	$\overline{Q}$			18	29	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clear	$\overline{Q}$			9	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear	Q			17	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Q or $\overline{Q}$			12	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Q or $\overline{Q}$			19	28	ns
t_W	Pulse Width	Clock High				20			ns
		Clock Low				20			ns
		Preset or Clear Low				20			ns
t_{SETUP}	Input Setup Time(3)					15↑			ns
t_{HOLD}	Input Hold Time(3)					10↑			ns

Notes

(3) ↑ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge.

DM93/DM8300

4-Bit Parallel-Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, J$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load and shift (in direction Q_A toward Q_D).

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops, and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

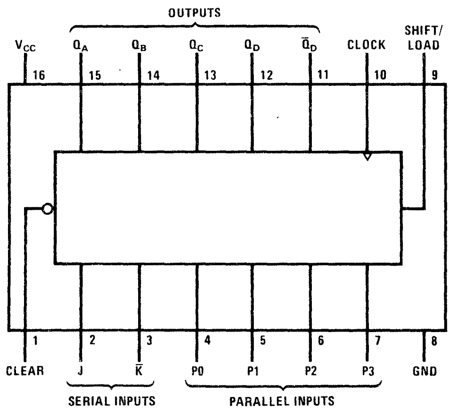
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J$\overline{K}$ inputs. These inputs permit the first stage to perform as a J$\overline{K}$, D or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs, including the clock, are buffered to lower the drive requirements to one normalized Series 54/74 load.

Features

- Direct replacement for Fairchild 9300
- Fully buffered inputs
- Direct overriding clear
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Positive edge-triggered clocking
- J and $\overline{K}$ inputs to first stage
- Typical shift frequency—39 MHz

Connection Diagram



9300/8300(J), (N), (W)

Truth Table

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL J	SERIAL $\overline{K}$	PARALLEL P0	P1	P2	P3	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Bn}	$\overline{Q}_{Cn}$

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↑ = Transition from low-to-high level
a, b, c, d = The level of steady state input at P0, P1, P2, or P3, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B or Q_C, respectively, before the most recent ↑ transition of the clock.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM93/83 00 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5	V
I_{OH}	High Level Output Current					−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, $I_{OH} = -800\mu A$		2.4			V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max(3)	9300			86	mA
			8300			92	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) With all outputs open, shift/load grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to clear, and then applying a momentary ground, followed by 4.5V, to clock.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

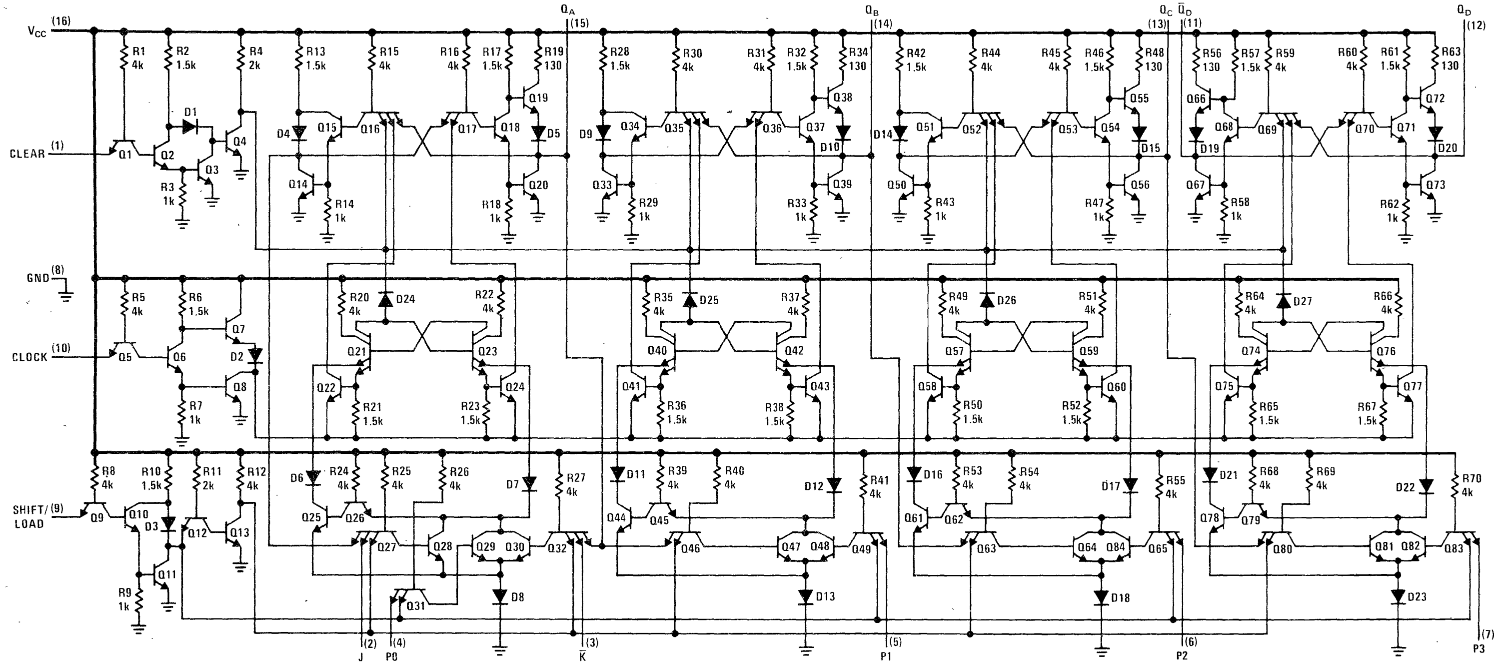
PARAMETER			CONDITIONS	DM93/83 00 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency		C_L = 15 pF, R_L = 400Ω	30	39		MHz
t_{PHL}	Propagation Delay Time, High-to-Low Level (Q) Output from Clear				19	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from Clock				14	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from Clock				17	26	ns
$t_{W(CLOCK)}$	Width of Clock Input Pulse			16	11		ns
$t_{W(CLEAR)}$	Width of Clear Input Pulse			30	15		ns
t_{SETUP}	Setup Time (4)	Shift/Load		30	13		ns
		Serial and Parallel Data		20	13		
		Clear Inactive-State		30	13		
$t_{RELEASE}$	Shift/Load Release Time (5)					10	ns
t_{HOLD}	Serial and Parallel Data Hold Time			0	−11		ns

Notes

(4) SET UP TIME: t_{SETUP} is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

(5) RELEASE TIME: $t_{RELEASE}$ is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) *not* to respond.

Schematic Diagram



1 of 10 Decoders

General Description

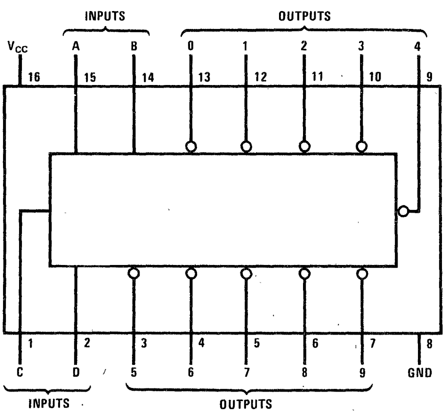
These BCD-to-decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain "OFF" for all invalid input conditions.

These circuits provide familiar TTL inputs and outputs which are compatible for use with other TTL and DTL circuits. DC noise margins are typically 1V and power dissipation is typically 125 mW. The diode-clamped, buffered inputs represent only one normalized Series 54/74 load.

Features

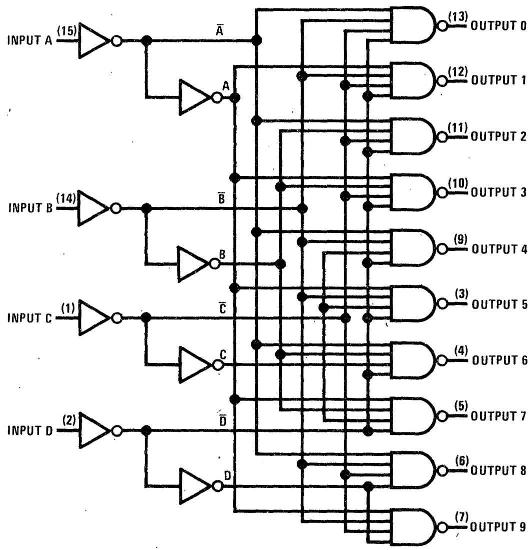
- Direct replacement for Fairchild 9301 and Signetics 8252
- Diode-clamped inputs
- All outputs are high for invalid BCD input conditions
- Typical power dissipation 125 mW
- Typical propagation delay 20 ns

Connection Diagram



9301(J), (W); 8301(J), (N), (W)

Logic Diagram



Truth Table

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	L	H	H	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	L	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	L	H	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	H	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM93/83 01			UNITS
			MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{OH}	High Level Output Current				−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −800μA	2.4			V
I_{OL}	Low Level Output Current				16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max(3)		25	41	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) I_{CC} is measured with the outputs open and all inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DM93/83 01			UNITS
			MIN	TYP	MAX	
t_{PHL}	Propagation Delay Time, High-to-Low Level, Any Output from A, B, C, or D	C_L = 15 pF, R_L = 400Ω		19	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level, Any Output from A, B, C, or D			20	30	ns

Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection to the AND-OR-INVERT gates.

The DM9309/8309 contains two separate 4-bit multiplexers with complementary Y and $\overline{Y}$ outputs; however, the two sections have common address select inputs.

The DM9312/8312 is a single 8-bit multiplexer with complementary outputs and a strobe control. When the strobe is low, the function is enabled. When a high logic level is applied to the strobe, the outputs are latched.

Features

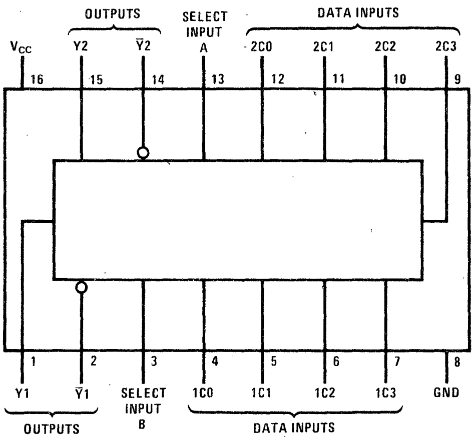
DM9309/8309

- Direct replacement for Fairchild 9309
- Complementary outputs
- Dual one-of-four data selectors

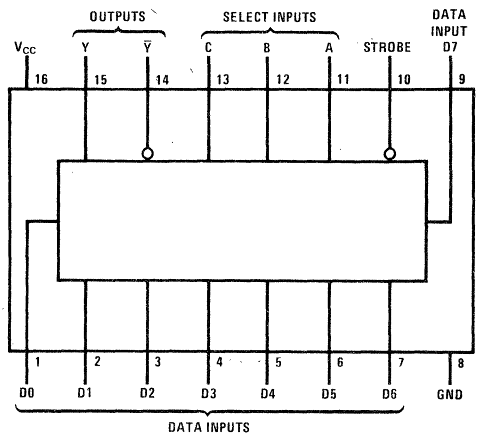
DM9312/8312

- Direct replacement for Fairchild 9312
- Selects one-of-eight data sources
- Performs parallel to serial conversion
- Strobe controlled outputs
- Complementary outputs

Connection Diagrams



9309(J), (W); 8309(J), (N), (W)



9312(J), (W); 8312(J), (N), (W)

Truth Tables

09

INPUTS						OUTPUTS	
SELECT		DATA				Y	$\overline{Y}$
B	A	C0	C1	C2	C3		
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	H	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care.

12

INPUTS				OUTPUTS	
SELECT			STROBE	Y	$\overline{Y}$
C	B	A	G		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care.
D0, D1 . . . D7 = The level of the respective D input.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM93/83 09, 12 MIN	DM93/83 09, 12 TYP(1)	DM93/83 09, 12 MAX	UNITS
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{OH}	High Level Output Current				−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4		V
I_{OL}	Low Level Output Current				16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−30		−85	mA
I_{CC}	Supply Current	V_{CC} = Max(3)		27	44	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25C.

(2) Not more than one output should be shorted at a time.

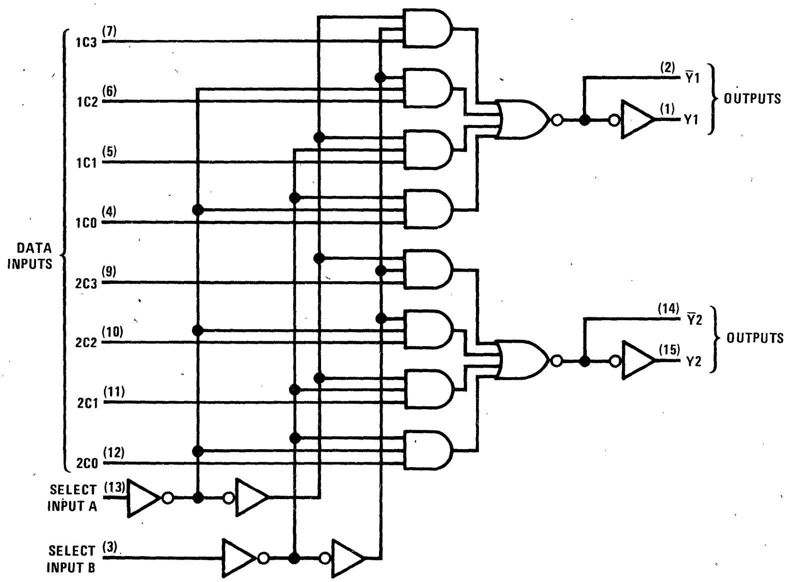
(3) I_{CC} is measured with the outputs open and all inputs at 4.5V for the DM9309/8309, and with the strobe and data select inputs at 4.5V, all other inputs and outputs open for the DM9312/8312.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS	DM93/83 09 MIN	DM93/83 09 TYP	DM93/83 09 MAX	DM93/83 12 MIN	DM93/83 12 TYP	DM93/83 12 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	Y	C_L = 15 pF R_L = 400Ω		27	40		22	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	Y			23	36		23	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	$\bar{Y}$			17	24		18	28	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	$\bar{Y}$			20	29		16	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Y			18	27		16	23	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Y			23	34		17	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	$\bar{Y}$			14	21		9	13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	$\bar{Y}$			9	13		9	13	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	Y			N/A			22	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	Y			N/A			21	32	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	$\bar{Y}$			N/A			13	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	$\bar{Y}$			N/A			15	21	ns

Logic Diagrams

09



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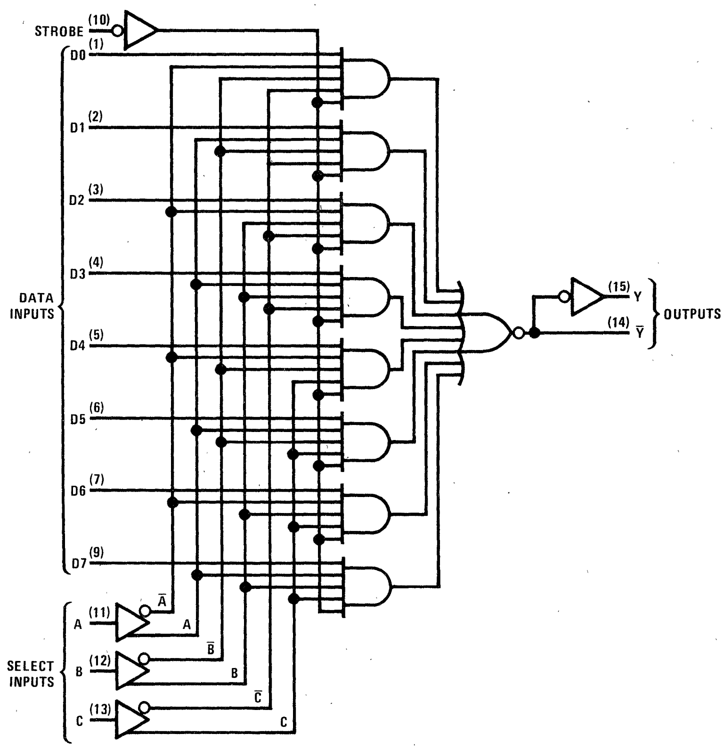


Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM9310/DM8310 are decade counters and the DM9316/DM8316 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

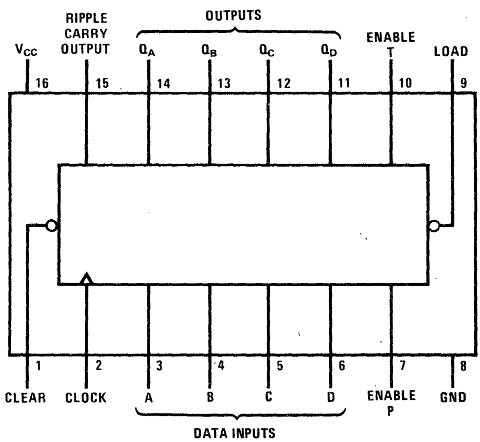
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripply carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

Features

- Direct replacement for Fairchild 9310, 9316
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters

  9310 – 54160A/74160A (decade)
  9316 – 54161A/74161A (binary)

Connection Diagram



9310(J), (W); 8310(J), (N), (W);
9316(J), (W); 8316(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS		DM93/83 10, 16 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current						−800	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA		2.4	3.4		V
I_{OL}	Low Level Output Current						16	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	Clock or Enable T	V_{CC} = Max, V_I = 2.4V				80	μA
		Other Inputs					40	
I_{IL}	Low Level Input Current	Clock or Enable T	V_{CC} = Max, V_I = 0.4V				−3.2	mA
		Other Inputs					−1.6	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	DM93	−20		−57	mA
				DM83	−18		−57	
I_{CCH}	Supply Current (High Level)		V_{CC} = Max(3)	DM93		59	85	mA
				DM83		59	94	
I_{CCL}	Supply Current (Low Level)		V_{CC} = Max(4)	DM93		63	91	mA
				DM83		63	101	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

(4) I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER			FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM93/83 10, 16 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				$C_L = 15$ pF, $R_L = 400\Omega$	25	35		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Ripple carry			18	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock	Ripple carry			16	24	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock (Load Input High)	Any Q			14	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock (Load Input High)	Any Q			16	23	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock (Load Input Low)	Any Q			14	21	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clock (Load Input Low)	Any Q			18	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Enable T	Ripple carry			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Enable T	Ripple carry			12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear	Any Q			24	36	ns
$t_{W(CLOCK)}$	Width of Clock Pulse					25			ns
$t_{W(CLEAR)}$	Width of Clear Pulse					20			ns
t_{SETUP}	Setup Time	Data Inputs A, B, C, D				20			ns
		Enable P				20			ns
		Load				25			ns
		Clear				20			ns
t_{HOLD}	Hold Time at Any Input (5)					0			ns

Notes

(5) The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V to 2V, whichever is longer.

Logic Diagrams

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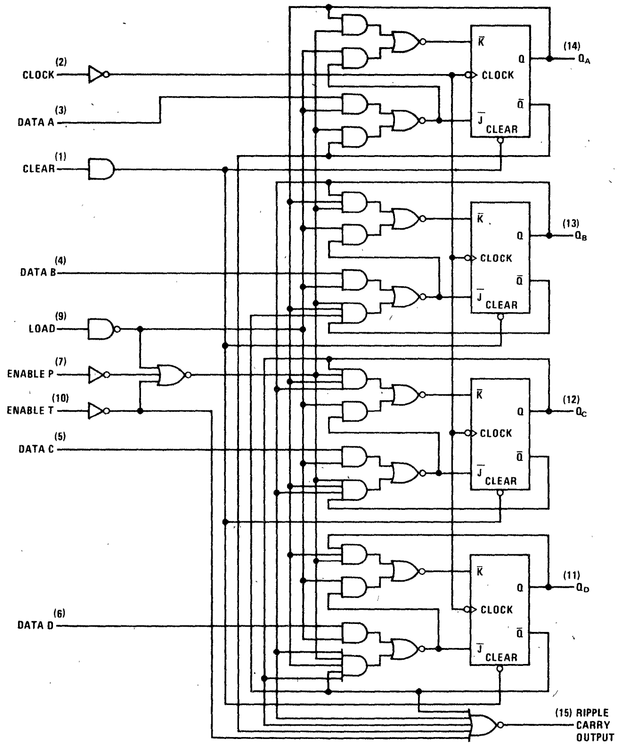

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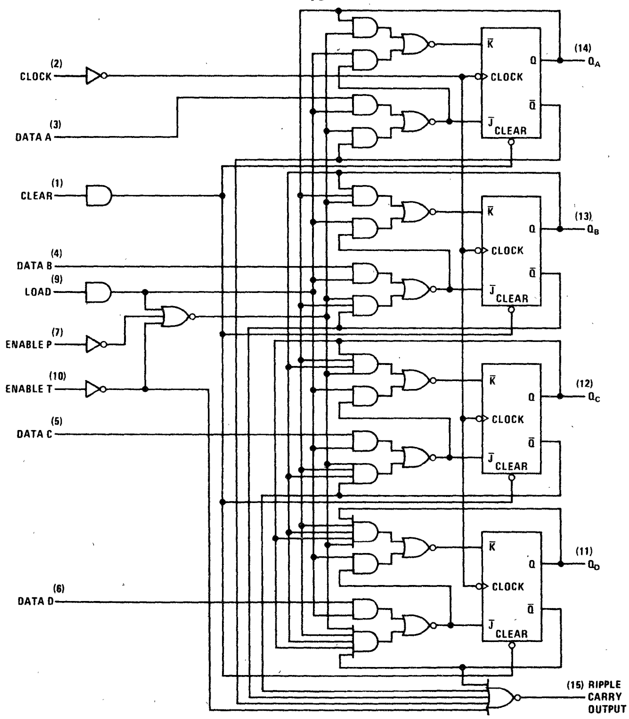
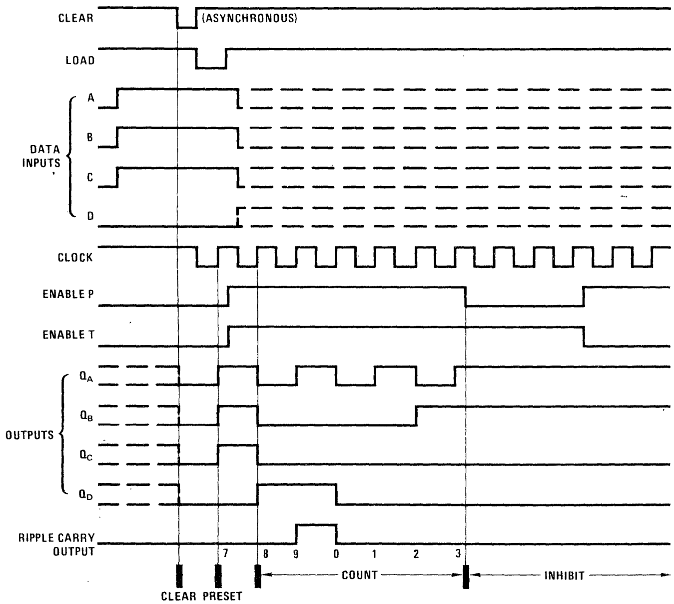


Timing Diagrams

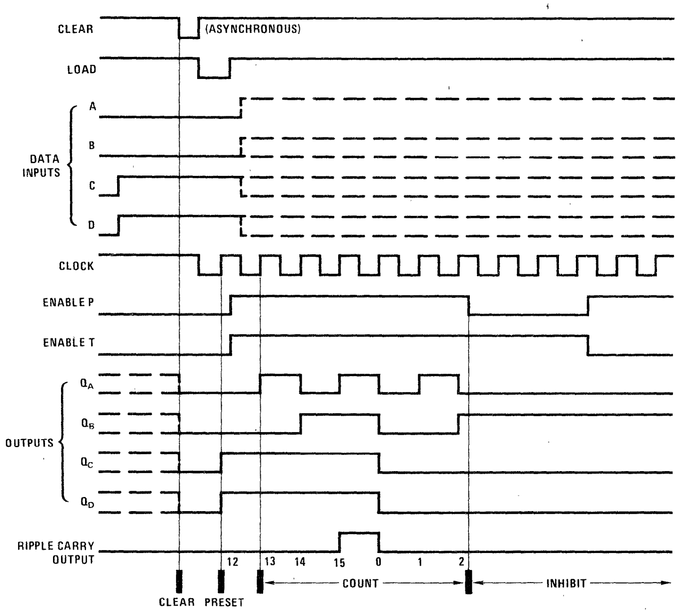
9310/8310 SYNCHRONOUS DECADE COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES



Sequence:

(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

9316/8316 SYNCHRONOUS BINARY COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

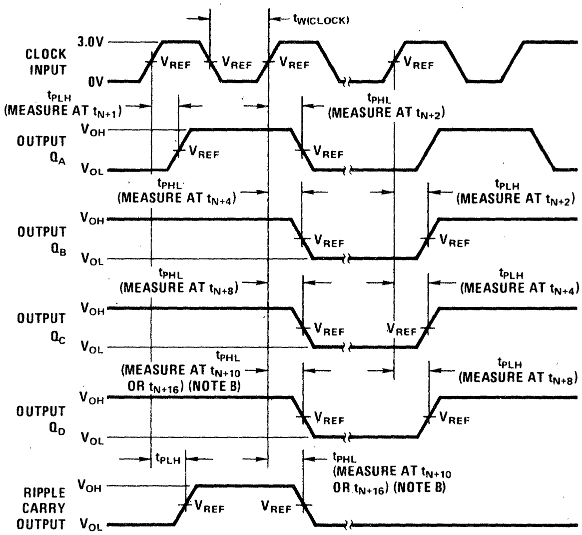


Sequence:

(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Parameter Measurement Information

SWITCHING TIME WAVEFORMS



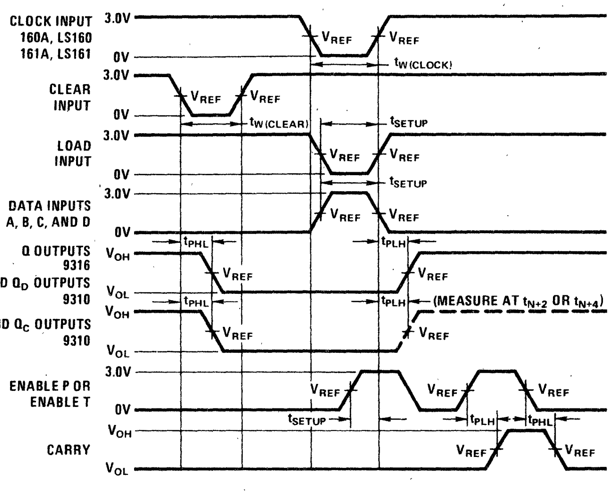
Notes:

(A) The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

(B) Outputs Q_D and carry are tested at t_{n+10} for 9310/8310, and at t_{n+16} for 9316/8316, where t_n is the bit time when all outputs are low.

(C) $V_{REF} = 1.5V$.

SWITCHING TIME WAVEFORMS



Notes:

(A) The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

(B) Enable P and enable T setup times are measured at t_{n+0}.

(C) $V_{REF} = 1.5V$.

4-Line to 16-Line Decoders/Demultiplexers

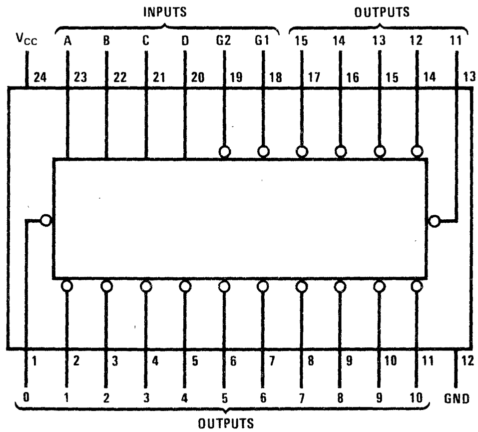
General Description

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Direct replacement for Fairchild 9311
- Pin for pin with popular 54154/74154
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay 19 ns
- Typical power dissipation 170 mW

Connection Diagram



9311(J), (F); 8311(J), (N), (F)

Truth Table

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM93/83 11 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −800μA		2.4	3.4		V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA			0.25	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	DM93	−20		−55	mA
			DM83	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max(3)	DM93		34	49	mA
			DM83		34	56	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

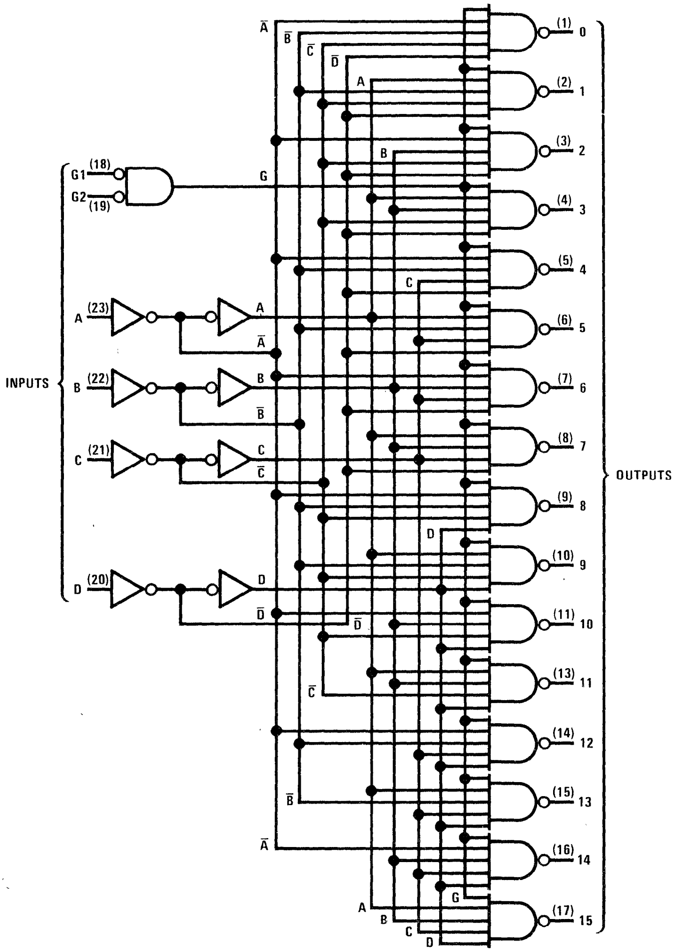
(2) Not more than one output should be shorted at a time.

(3) I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	DM93/83 11 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output, From A, B, C, or D Inputs Through 3 Levels of Logic	C_L = 15 pF R_L = 400Ω		18	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output, From A, B, C, or D Inputs Through 3 Levels of Logic			21	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output, From Either Strobe Input			17	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output, From Either Strobe Input			18	27	ns

Logic Diagram



Priority Encoders

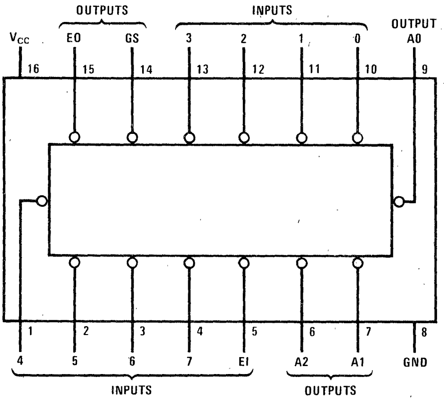
General Description

These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. All inputs are buffered to represent one normalized Series 54/74 load. The DM9318 and DM8318 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

Features

- Direct replacement for Fairchild 9318
- Pin for pin with popular DM54148/74148
- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators
- Typical data delay 10 ns
- Typical power dissipation 190 mW

Connection Diagram



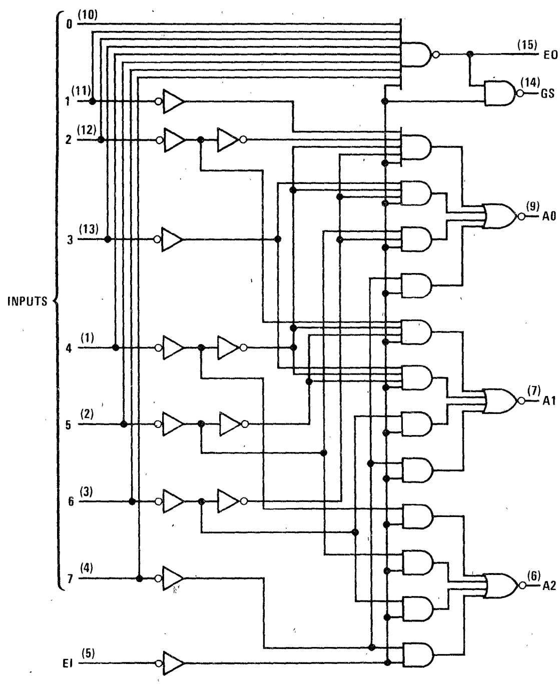
9318(J), (W); 8318(J), (N), (W)

Truth Table

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High Logic Level, L = Low Logic Level, X = Don't Care

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS	DM93/83 18 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = -12 mA			−1.5	V
I_{OH}	High Level Output Current					−800	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA	2.4			V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA			0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	0 Input	V_{CC} = Max, V_I = 2.4V			40	μA
		Others				80	
I_{IL}	Low Level Input Current	0 Input	V_{CC} = Max, V_I = 0.4V			−1.6	mA
		Others				−3.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)	−35		−85	mA
I_{CC}	Supply Current		V_{CC} = Max (3), Condition 1		40	60	mA
			Condition 2		35	55	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) I_{CC} (condition 1) is measured with inputs 7 and E1 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	WAVEFORM	CONDITIONS	DM93/83 18 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	0 thru 7	A, B, C, D	In-Phase Output	C_L = 15 pF, R_L = 400Ω		10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						9	14	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	0 thru 7	A, B, C, D	Out-of-Phase Output			13	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						12	19	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	0 thru 7	EO	Out-of-Phase Output			6	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						14	21	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	0 thru 7	GS	In-Phase Output			18	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						14	21	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	EI	A0, A1, or A2	In-Phase Output			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						10	15	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	EI	GS	In-Phase Output			8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						10	15	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	EI	EO	In-Phase Output			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						17	26	ns

Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. True data is presented at the outputs.

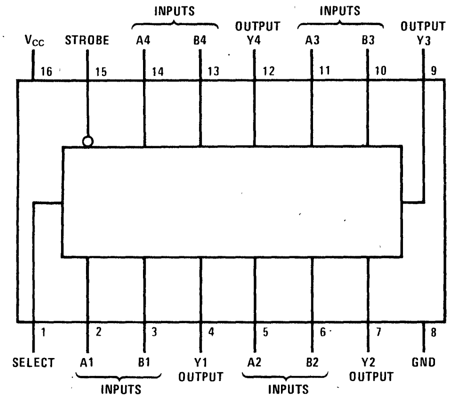
Features

- Direct replacement for Fairchild 9322
- Pin-for-pin with popular DM54157/74157
- Buffered inputs and outputs

Applications

- Expand any data input point
- Multiplex dual-data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Connection Diagram



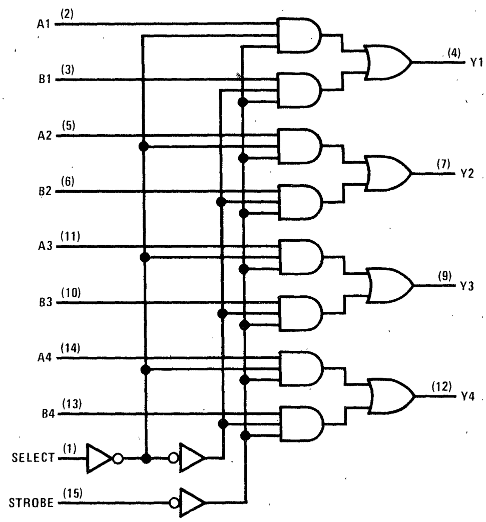
9322(J), (W); 8322(J), (N), (W)

Truth Table

INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS	DM93 22 MIN	DM93 22 TYP(1)	DM93 22 MAX	DM83 22 MIN	DM83 22 TYP(1)	DM83 22 MAX	UNITS
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High Level Output Current				−800			−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4		2.4	3.4		V
I_{OL}	Low Level Output Current				16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)	−20		−55	−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max(3)		30	48		30	48	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM (INPUT)	CONDITIONS	DM93/83 22 MIN	DM93/83 22 TYP	DM93/83 22 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	C_L = 15 pF, R_L = 400Ω		8	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	C_L = 15 pF, R_L = 400Ω		10	14	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Strobe	C_L = 15 pF, R_L = 400Ω		13	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Strobe	C_L = 15 pF, R_L = 400Ω		14	21	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Select	C_L = 15 pF, R_L = 400Ω		15	23	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Select	C_L = 15 pF, R_L = 400Ω		17	27	ns

8-Bit Addressable Latches

General Description

The DM9334/DM8334 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level high outputs. The device also incorporates an active level low common clear for resetting all latches, as well as an active level low enable.

The DM9334/DM8334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the low state. In the clear mode all outputs are low and unaffected by the address and data inputs.

When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operation of the product.

Features

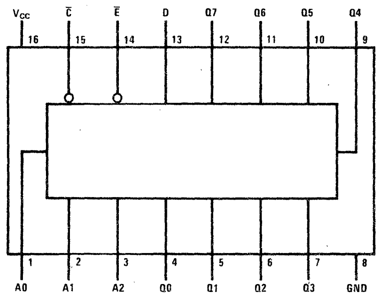
- Direct replacement for Fairchild 9334
- Common clear
- Easily expandable
- Random (addressable) data entry
- Serial to parallel capability
- 8 bits of storage/output of each bit available
- Active high demultiplexing/decoding capability

Truth Tables

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active High Eight-Channel Demultiplexer
H	L	Clear

X = Don't Care Condition
L = Low Voltage Level
H = High Voltage Level
Q_{N-1} = Previous Output State

Connection Diagram



9334/8334(J), (N), (W)

INPUTS						PRESENT OUTPUT STATES								
$\overline{C}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} ⟶								MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} ⟶					ADDRESSABLE LATCH
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} ⟶						
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} ⟶						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} ⟶						
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
H	L	L	H	H	H	Q_{N-1} ⟶						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} ⟶						Q_{N-1}	H	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM93/83 34 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current					−800	µA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800µA		2.4	3.6		V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	$\bar{E}$ Input		15	60	µA
			Others		10	40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	$\bar{E}$ Input		−1.44	−2.4	mA
			Others		−0.96	−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−30	−65	−100	mA
I_{CC}	Supply Current	V_{CC} = Max			56	86	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

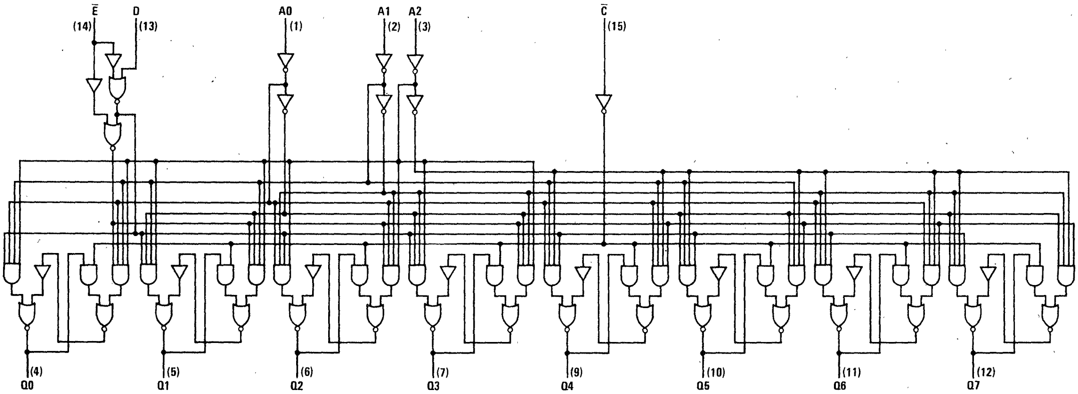
Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM	TO	CONDITIONS	DM93/83 34 MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Output *(Figure 1)*	C_L = 15 pF, R_L = 400Ω		19	28	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Enable	Output *(Figure 1)*			18	27	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Data	Output *(Figure 2)*			24	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Data	Output *(Figure 2)*			19	28	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Address	Output *(Figure 3)*			23	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Address	Output *(Figure 3)*			21	35	ns
t_{PHL}	Propagation Delay Time, Low-to-High Level Output	Clear	Output *(Figure 5)*			21	31	ns
t_W	Enable Pulse Width *(Figure 1)*				19	13		ns
t_{SETUP}	High Data to Enable *(Figure 4)*				20	13		ns
	Low Data to Enable *(Figure 4)*				20	14		ns
	Address to Enable(3) *(Figure 6)*				10	5		ns
t_{HOLD}	High Data to Enable *(Figure 4)*				0	−10		ns
	Low Data to Enable *(Figure 4)*				0	−13		ns

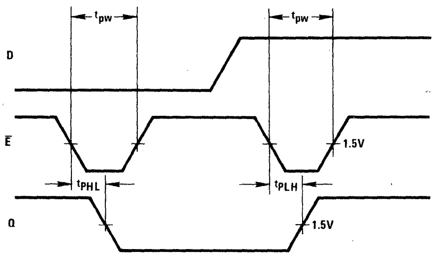
Notes

(3) The Address to Enable Set-Up Time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

Logic Diagram

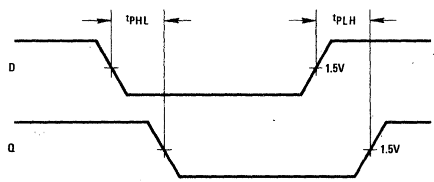


Switching Time Waveforms



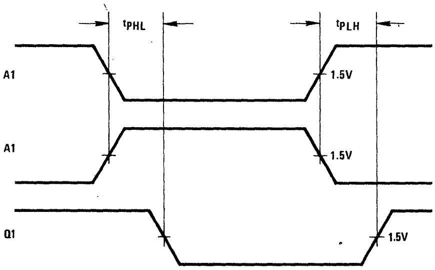
OTHER CONDITIONS: C̄ = H, A = STABLE

FIGURE 1



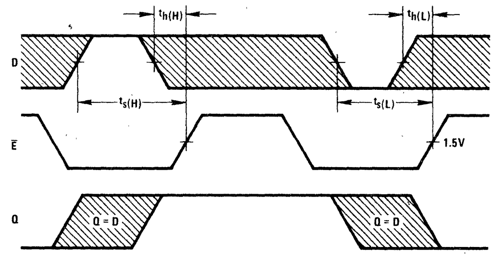
OTHER CONDITIONS: Ē = L, C̄ = H, A = STABLE

FIGURE 2



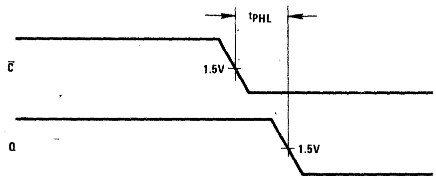
OTHER CONDITIONS: Ē = L, C̄ = L, D = H

FIGURE 3



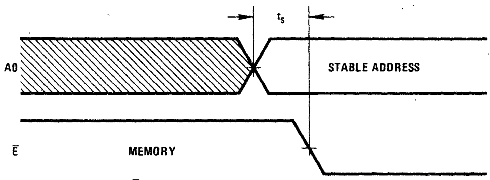
OTHER CONDITIONS: C̄ = H, A = STABLE

FIGURE 4



OTHER CONDITIONS: Ē = H

FIGURE 5



OTHER CONDITIONS: C̄ = H

FIGURE 6

Note. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

Retriggerable One Shots

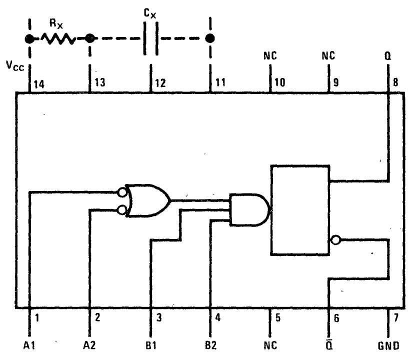
General Description

These retriggerable one shots provide the designer with four inputs; two active high and two active low. This permits a choice of either leading-edge or trailing-edge triggering, independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge again. The retriggerable feature allows for output pulse widths to be expanded. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. Retriggering may be inhibited by tying the $\overline{Q}$ output to an active low input.

Features

- High speed operation—input repetition rate > 10 MHz
- Flexibility of operation—optional retriggering/lock-out capability
- Output pulse width range—50 ns to ∞
- Leading or trailing edge triggering
- Complementary outputs/inputs
- Input clamping diodes
- DTL/TTL compatible logic levels

Connection Diagram

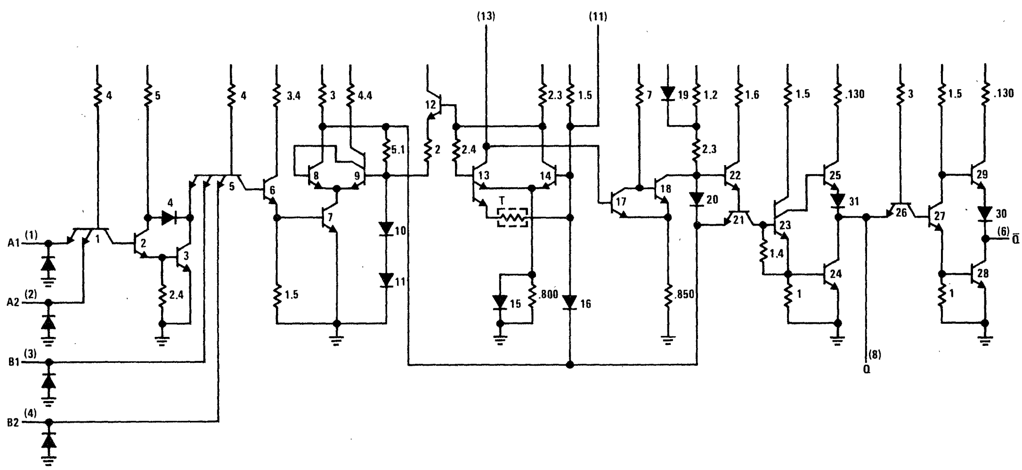


9601/8601(J), (N), (W)

Truth Table

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⊓	⊔
L	X	H	↑	⊓	⊔
X	L	H	H	L	H
X	L	↑	H	⊓	⊔
X	L	H	↑	⊓	⊔
H	↓	H	H	⊓	⊔
↓	↓	H	H	⊓	⊔
↓	H	H	H	⊓	⊔

Schematic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM9601 MIN	DM9601 TYP(1)	DM9601 MAX	DM8601 MIN	DM8601 TYP(1)	DM8601 MAX	UNITS
V_{IH}	High Level Input Voltage		$T_A = -55°C$	2.0						V
			$T_A = 0°C$				1.9			
			$T_A = 25°C$	1.7			1.8			
			$T_A = 75°C$				1.6			
			$T_A = 125°C$	1.5						
V_{IL}	Low Level Input Voltage		$T_A = -55°C$			0.85				V
			$T_A = 0°C$						0.85	
			$T_A = 25°C$			0.90			0.85	
			$T_A = 75°C$						0.85	
			$T_A = 125°C$			0.85				
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−720			−960	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max		2.4			2.4			V
I_{OL}	Low Level Output Current					10			12.8	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max				0.40			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V			15	60		15	60	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.40V			−1.6				mA
			V_I = 0.45V						−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−10		−40	−10		−40	mA
I_{CC}	Supply Current	V_{CC} = Max				25			25	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) Unless otherwise specified, R_X = 10 kΩ between Pin 13 and V_{CC} on all tests.

(4) Ground Pin 11 for V_{OL} test on Pin 6, V_{OH} test on Pin 8 and I_{OS} test on Pin 8. Open Pin 11 for V_{OL} test on Pin 8, V_{OH} test on Pin 6 and I_{OS} test on Pin 6.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER			CONDITIONS	DM9601 MIN	DM9601 TYP	DM9601 MAX	DM8601 MIN	DM8601 TYP	DM8601 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Negative Trigger Input to True Output	C_L = 15 pF, C_X = 0, R_X = 5 kΩ		25	40		25	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Negative Trigger Input to Complement Output			25	40		25	40	ns
$t_{PW(MIN)}$	Minimum True Output Pulse Width				45	65		45	65	ns
t_{PW}	Pulse Width		R_X = 10 kΩ, C_X = 1000 pF	3.08	3.42	3.76	3.08	3.42	3.76	μs
C_{STRAY}	Maximum Allowable Wiring Capacitance		Pin 13 to GND			50			50	pF
R_X	External Timing Resistor			5		25	5		50	kΩ

Operating Rules

1. An external resistor R_X and an external capacitor C_X are required for operation. The value of R_X can vary between the limits shown in switching characteristics. The value of C_X is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width t_{PW} may be calculated as follows:

$$t_{PW} = 0.32\, R_X C_X \left[1 + \frac{0.7}{R_X}\right] \text{ (for } C_X \geq 10^3 \text{ pF)}$$

   R_X in kΩ, C_X in pF and t_{PW} in ns.
   (For $C_X < 10^3$ pF, see curve.)
3. R_X and C_X must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, R_X may be split up such that at least $R_{X(MIN)}$ must be as close as possible to the circuit and the remote portion of the trimming resistor $R < R_{X(MAX)} - R_X$.
4. Set-up time (t_1) for input trigger pulse must be >40 ns. (See *Figure 1*).
   Release time (t_2) for input trigger pulse must be >40 ns. (See *Figure 2*).
5. Retrigger pulse width (see *Figure 3*) is calculated as follows:

$$t_W = t_{PW} + t_{PLH} = 0.32\, R_X C_X \left[1 + \frac{0.7}{R_X}\right] + t_{PLH}$$

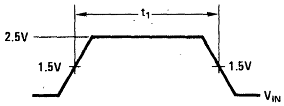


FIGURE 1

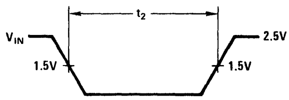


FIGURE 2

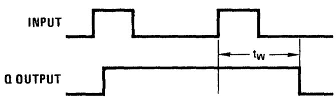
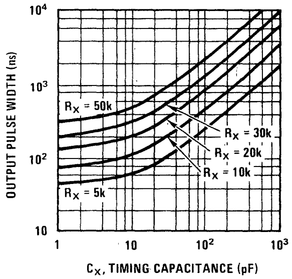


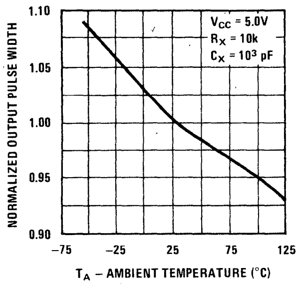
FIGURE 3

Typical Performance Characteristics

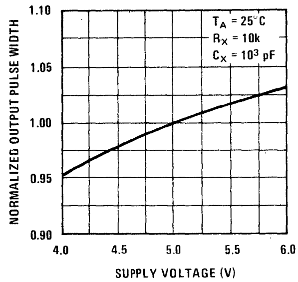
OUTPUT PULSE WIDTH VS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF



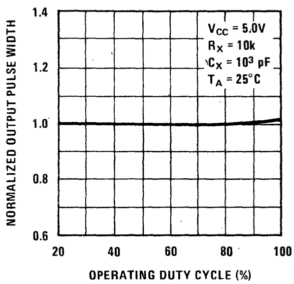
NORMALIZED OUTPUT PULSE WIDTH VS AMBIENT TEMPERATURE



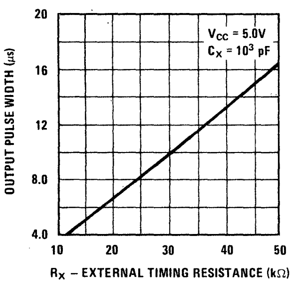
NORMALIZED OUTPUT PULSE WIDTH VS SUPPLY VOLTAGE



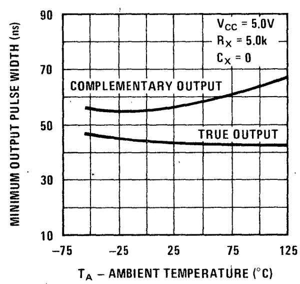
NORMALIZED OUTPUT PULSE WIDTH VS OPERATING DUTY CYCLE



PULSE WIDTH VS TIMING RESISTANCE



OUTPUT PULSE WIDTH VS AMBIENT TEMPERATURE



Dual Retriggerable, Resettable One Shots

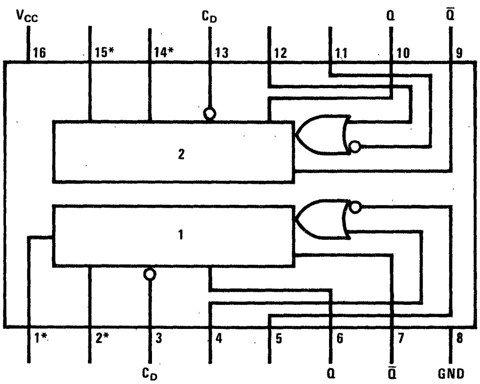
General Description

These dual resettable, retriggerable one shots have two inputs per function; one which is active high, and one which is active low. This allows the designer to employ either leading-edge or trailing-edge triggering, which is independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is allowed to rapidly discharge and then charge again. The retriggerable feature permits output pulse widths to be extended. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. The output pulse may then be terminated at any time by applying a low logic level to the RESET pin. Retriggering may be inhibited by either connecting the Q output to an active high input, or the $\overline{Q}$ output to an active low input.

Features

- 70 ns to ∞ output width range
- Resettable and retriggerable—0% to 100% duty cycle
- TTL input gating—leading or trailing edge triggering
- Complementary TTL outputs
- Optional retrigger lock-out capability
- Pulse width compensated for V_{CC} and temperature variations

Connection Diagram



*Pins for external timing

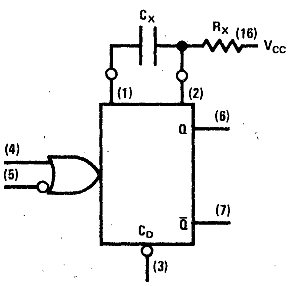
9602/8602(J), (N), (W)

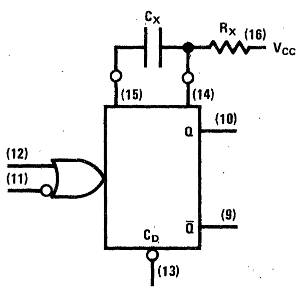
Truth Table

PIN NO'S.			OPERATION
5(11)	4(12)	3(13)	
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Logic Diagrams





Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	CONDITIONS		DM9602 MIN	DM9602 TYP(1)	DM9602 MAX	DM8602 MIN	DM8602 TYP(1)	DM8602 MAX	UNITS
V_{IH}	High Level Input Voltage		$T_A = -55°C$	2.0						V
			$T_A = 0°C$				1.9			
			$T_A = 25°C$	1.7			1.8			
			$T_A = 75°C$				1.65			
			$T_A = 125°C$	1.5						
V_{IL}	Low Level Input Voltage		$T_A = -55°C$			0.85				V
			$T_A = 0°C$						0.85	
			$T_A = 25°C$			0.90			0.85	
			$T_A = 75°C$						0.85	
			$T_A = 125°C$			0.85				
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5			−1.5	V
I_{OH}	High Level Output Current					−800			−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, $I_{OH} = -800\mu A$		2.4			2.4			V
I_{OL}	Low Level Output Current					16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = 16 mA				0.40			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V			10	60		10	60	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.40V			−1.6				mA
			V_I = 0.45V						−1.6	
		V_{CC} = Min	V_I = 0.40V			−1.24				
			V_I = 0.45V						−1.41	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)				−25			−35	mA
I_{CC}	Supply Current	V_{CC} = Max			39	45		39	50	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

(3) Unless otherwise noted, R_X = 10 kΩ for all tests.

(4) Ground Pin 1 (15) for V_{OL} on Pin 7 (9), or for V_{OH} on Pin 6 (10), or for I_{OS} on Pins 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for V_{OL} on Pin 6 (10), or for V_{OH} on Pin 7 (9), or for I_{OS} on Pin 7 (9).

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER		CONDITIONS	DM9602 MIN	DM9602 TYP	DM9602 MAX	DM8602 MIN	DM8602 TYP	DM8602 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Negative Trigger Input to True Output	C_L = 15 pF, C_X = 0, R_X = 5 kΩ		25	35		25	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Negative Trigger Input To Complement Output			29	43		29	48	ns
$t_{PW (MIN)}$	Minimum True Output Pulse Width				72	90		72	100	ns
	Minimum Complement Pulse Width				78	100		78	110	
t_{PW}	Pulse Width		R_X = 10 kΩ; C_X = 1000 pF	3.08	3.42	3.76	3.08	3.42	3.76	μs
C_{STRAY}	Maximum Allowable Wiring Capacitance		Pins 2, 14 to GND			50			50	pF
R_X	External Timing Resistor			5		25	5		50	kΩ

Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.

2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.

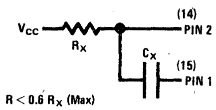
3. The output pulse with (t) is defined as follows:

$$t = 0.31\ R_X C_X \left[1 + \frac{1}{R_X}\right]$$

where R_X is in kΩ, C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see *Figure 1.*

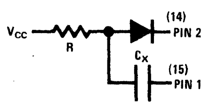
4. If electrolytic type capacitors are to be used, the following three configurations are recommended:

   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0V is less than 3μA, and the inverse capacitor leakage at 1.0V is less than 5μA over the operational temperature range.



   B. Use with high inverse leakage current electrolytic capacitors:
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

$$t \approx 0.3\ RC_X$$



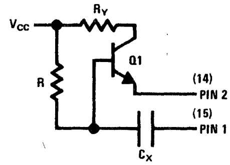
   C. Use to obtain extended pulse widths:
   This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

   $R < R_X$ (0.7) (h_{FE} Q1) or < 2.5 MΩ, whichever is the lesser

   R_X (min) $< R_Y < R_X$ (max)
   (5 kΩ $\leq R_Y \leq$ 10 kΩ is recommended)

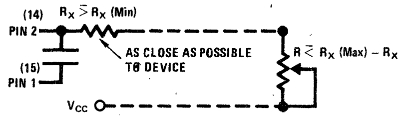
   Q1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962.

$$t \approx 0.3\ RC_X$$



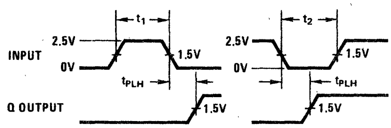
   This configuration is not recommended with retriggerable operation.

5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



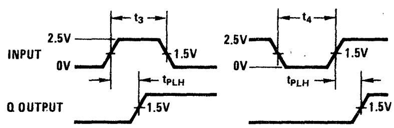
6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

7. Input Trigger Pulse Rules (See Triggering Truth Table)



Input to Pin 5 (11), Pin 4 (12) = LOW (Pin 3 (13) = HIGH)

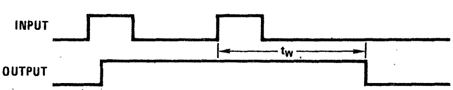
t_1, t_3 = Min. Positive Input Pulse Width > 40 ns
t_2, t_4 = Min. Negative Input Pulse Width > 40 ns



Input to Pin 4 (12), Pin 5 (11) = HIGH (Pin 3 (13) = HIGH)

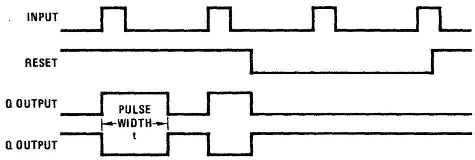
8. The retriggerable pulse width is calculated as shown below:

$$t_W = t + t_{PLH} = 0.31\ R_X\ C_X \left(1 + \frac{1}{R_X}\right) + t_{PLH}$$



Operating Rules (Continued)

The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X (ns) after the initial trigger pulse. (i.e., during the discharge cycle).



9. Reset Operation – An overriding clear (active LOW level) is provided on each one shot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.

10. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1µF bypass capacitor between V_{CC} and Ground located near the DM9602/DM8602 is recommended.

Typical Performance Characteristics

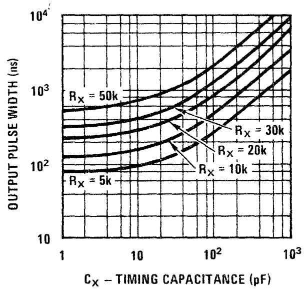


FIGURE 1. OUTPUT PULSE WIDTH VS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

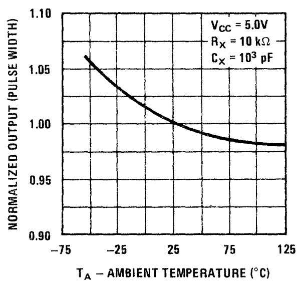


FIGURE 2. NORMALIZED OUTPUT PULSE WIDTH VS AMBIENT TEMPERATURE

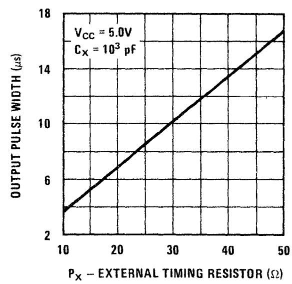


FIGURE 3. PULSE WIDTH VS TIMING RESISTOR

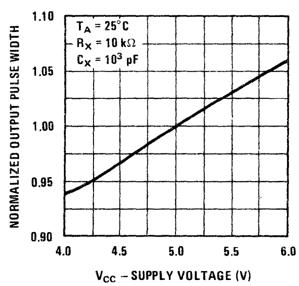


FIGURE 4. NORMALIZED OUTPUT PULSE WIDTH VS SUPPLY VOLTAGE

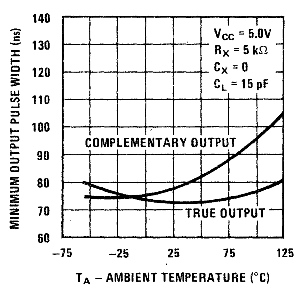


FIGURE 5. MINIMUM OUTPUT PULSE WIDTH VS AMBIENT TEMPERATURE

Notes

Notes

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