MOS

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MOS INTEGRATED CIRCUITS

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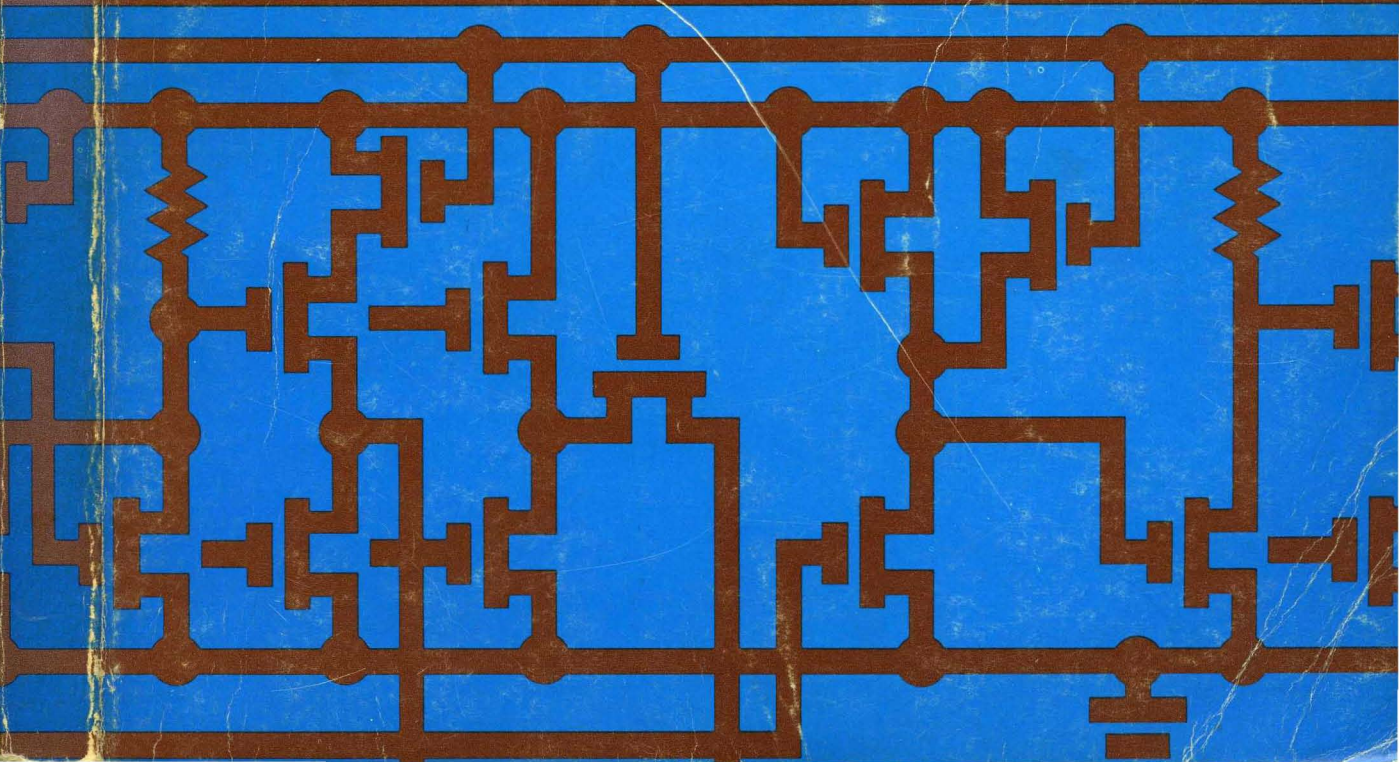

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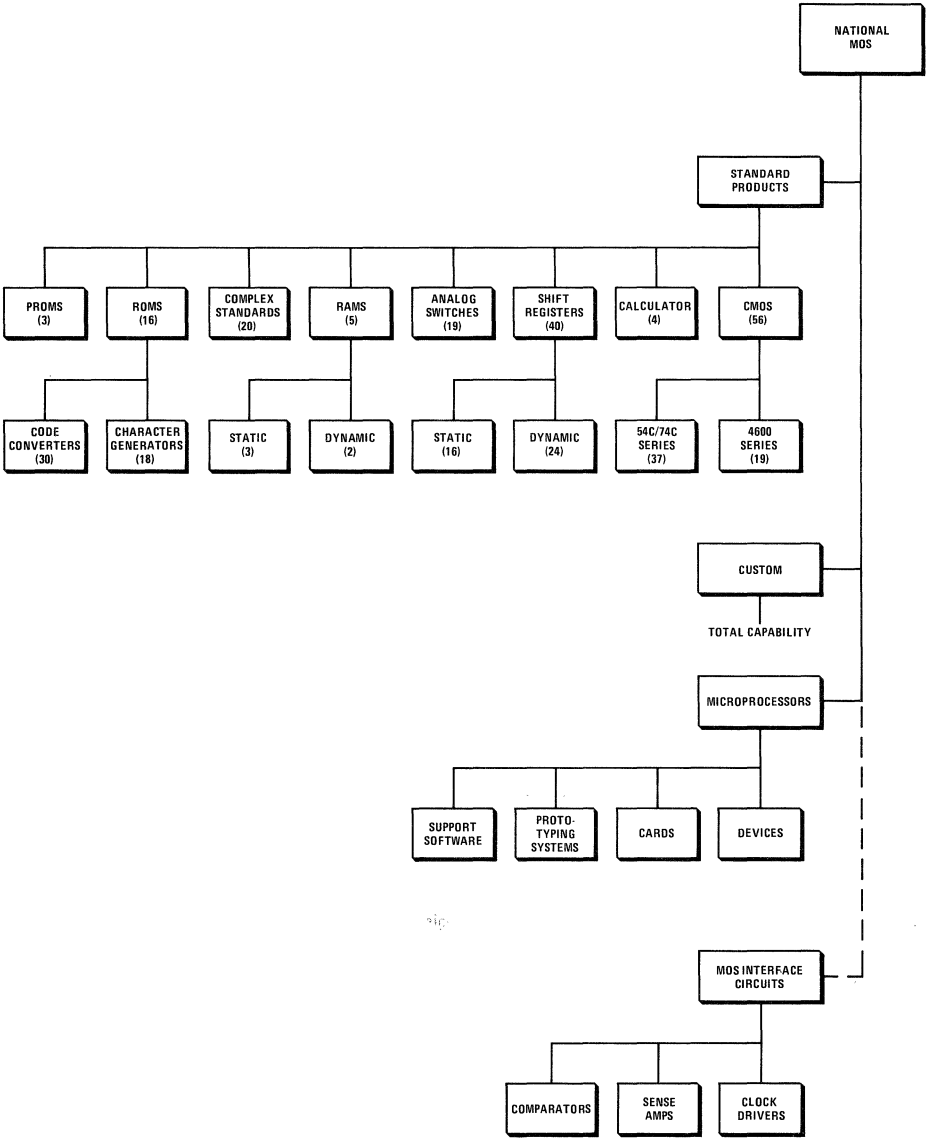
Introduction

Here is National's newest MOS handbook containing information on the largest standard MOS product line in the industry. Extra copies of this handbook, plus those on our other major product lines — digital, linear and transistors — are also available. To receive your handbooks, contact a National sales office, representative or distributor.



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	Max Freq or Min Access Time	V_{SS}	V_{DD}	V_{DD2} or V_{GG}	Clock Swing
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MM400/MM500 Dual 25-Bit Dynamic Shift Register	1.0 MHz	+10	GND	None	16
MM401/MM501 Dual 25-Bit Dynamic Shift Register	1.0 MHz	+10	GND	None	16
MM402/MM502 Dual 50-Bit Dynamic Shift Register	1.0 MHz	+10	GND	None	16
MM403/MM503 Dual 50-Bit Dynamic Shift Register	1.0 MHz	+10	GND	None	16
MM406/MM506 Dual 100-Bit Dynamic Shift Register	1.0 MHz	+10	GND	None	16
MM407/MM507 Dual 100-Bit Dynamic Shift Register	1.0 MHz	+10	GND	None	16
MM1402A 1024-Bit Dynamic Shift Register	5.0 MHz	+5.0	5.0	None	17
MM1403A 1024-Bit Dynamic Shift Register	5.0 MHz	+5.0	5.0	None	17
MM1404A 1024-Bit Dynamic Shift Register	5.0 MHz	+5.0	-5.0	None	17
MM4001A/MM5001A Dual 64-Bit Dynamic Shift Register	2.5 MHz	+5.0	None	-12	17
MM4006A/MM5006A Dual 100-Bit Dynamic Shift Register	2.5 MHz	+5.0	None	-12	17
MM4007/MM5007 Dual 100-Bit Mask Programmable Shift Register	2.5 MHz	+5.0	None	-12	17
MM4010A/MM5010A Dual 64-Bit Accumulator	2.5 MHz	+5.0	None	-12	17
MM4013/MM5013 1024-Bit Register/Accumulator	2.5 MHz	+5.0	None	-12	17
MM4015A/MM5015A Triple 60 + 4-Bit Register/Accumulator	2.5 MHz	+5.0	None	-12	17
MM4016/MM5016 512-Bit Dynamic Shift Register	2.5 MHz	+5.0	None	12	17
MM4017/MM5017 Dual 512-Bit Dynamic Shift Register	2.5 MHz	+5.0	None	12	17
MM4019/MM5019 Dual 256-Bit Mask Programmable Shift Register	2.5 MHz	+5.0	None	12	17
MM5023 Quad 80-Bit Dynamic Shift Register	2.5 MHz	+5.0	GND	-12	TTL
MM5024A 1024-Bit Dynamic Shift Register	5.0 MHz	+5.0	-5.0	None	17
MM4025/MM5025 Dual 1024-Bit Dynamic Shift Register	3.0 MHz	+5.0	GND	-12	17
MM4026/MM5026 Dual 1024-Bit Dynamic Shift Register	3.0 MHz	+5.0	GND	-12	17
MM4027/MM5027 2048-Bit Dynamic Shift Register	3.0 MHz	+5.0	GND	-12	17
MM4104/MM5104 Dynamic Shift Register	2.5 MHz	+5.0	None	-12	17
Static Shift Registers					
MM404/MM504 Dual 16-Bit Static Register	1.0 MHz	+10	GND	-6.0	16
MM405/MM505 Dual 32-Bit Static Register	1.0 MHz	+10	GND	-6.0	16
MM4040/MM5040 Dual 16-Bit Static Shift Register	2.2 MHz	+5.0	GND	-12	17
MM4050A/MM5050A Dual 32-Bit Static Shift Register	1.6 MHz	+5.0	GND	-12	17
MM4051A/MM5051A Dual 32-Bit Static Shift Register-Split Clock	1.6 MHz	+5.0	GND	-12	17
MM4052/MM5052 Dual 80-Bit Static Shift Register	1.6 MHz	+5.0	GND	-12	17
MM4053/MM5053 Dual 100-Bit Static Shift Register	1.6 MHz	+5.0	GND	-12	17
MM5054 Dual 64/72/80-Bit Static Shift Register	2.2 MHz	+5.0	GND	-12	TTL
MM4055/MM5055 Quad 128-Bit Static Shift Register	1.5 MHz	+5.0	GND	-12	TTL
MM4056/MM5056 Dual 256-Bit Static Shift Register	1.5 MHz	+5.0	GND	-12	TTL
MM4057/MM5057 512-Bit Static Shift Register	1.5 MHz	+5.0	GND	-12	TTL
MM5058 1024-Bit Static Shift Register	1.5 MHz	+5.0	GND	-12	TTL
MM5060 Dual 144-Bit Mask Programmable Static Shift Register	1.5 MHz	+5.0	GND	-12	TTL
MM5061 Quad 100-Bit Static Shift Register	1.5 MHz	+5.0	GND	-12	TTL
PROMs/ROMs					
MM3501 1024-Bit Read-Only Memory	4.0 μs	0	-13	-27	None
MM5202A Electrically Programmable 2048-Bit PROM	1.0 μs	+5.0	-12	-12	None
MM4203/MM5203 2048-Bit Electrically Programmable PROM	1.0 μs	+5.0	-12	-12	None
MM5204 Electrically Programmable 4096-Bit PROM	—	+5.0	-12	-12	None
MM4210/MM5210 1024-Bit Read-Only Memory	650 ns	+12	-12	-12	None
MM4211/MM5211 1024-Bit Read-Only Memory	950 ns	+5.0	-12	-12	None
MM5212 12,288-Bit Read-Only Memory	5.0 μs	+5.0	-12	-12	None
MM4213/MM5213 2048-Bit Read-Only Memory	750 ns	+5.0	-12	-12	None
MM4214/MM5214 4096-Bit Read-Only Memory	1.0 μs	+5.0	-12	-12	None
MM5215 12,288-Bit Read-Only Memory	3.0 μs	+12	0V	-12	None
MM4220/MM5220 1024-Bit Read-Only Memory	650 ns	+12	-12	-12	None
MM4221/MM5221 1024-Bit Read-Only Memory	950 ns	+5.0	-12	-12	None
MM4229/MM5229 3072-Bit Read-Only Memory (Open Drain)	1.4 μs	+5.0	-12	-12	None
MM4230/MM5230 2048-Bit Read-Only Memory	725 ns	+12	-12	-12	None
MM4231/MM5231 2048-Bit Read-Only Memory	950 ns	+5.0	-12	-12	None
MM4232/MM5232 4096-Bit Static Read-Only Memory	1.0 μs	+5.0	-12	-12	None
MM4233/MM5233 4096-Bit Read-Only Memory	1.0 μs	+5.0	-12	-12	None
MM4240/MM5240 2560-Bit Static Character Generator	600 ns	+12	-12	-12	None
MM4241/MM5241 3072-Bit Static Read-Only Memory	900 ns	+5.0	-12	-12	None
RAMs					
MM1101 256-Bit Fully Decoded Static Random Access Memory	1.5 μs	+5.0	-7.0	-10	None
MM11011 256-Bit Fully Decoded Static Random Access Memory	1.0 μs	+5.0	-7.0	-10	None
MM1101A 256-Bit Fully Decoded Static Random Access Memory	1.5 μs	+5.0	-9.0	-9.0	None
MM1101A1 256-Bit Fully Decoded Static Random Access Memory	1.0 μs	+5.0	-9.0	-9.0	None
MM1101A2 256-Bit Fully Decoded Static Random Access Memory	500 ns	+5.0	-9.0	-9.0	None
MM2102 1024-Bit Fully Decoded Static Random Access Memory	1.0 μs	+5.0	None	None	None
MM4250 256-Bit Fully Decoded Static Random Access Memory	650 ns	+5.0	-5.0	-9.0	None
MM4262/MM5262 2048-Bit Fully Decoded Dynamic R/W Memory	365 ns	+5.5	-15	+8.5*	19

*V_{BB}

Dynamic Shift Registers

*MM400/MM500 series dynamic shift registers

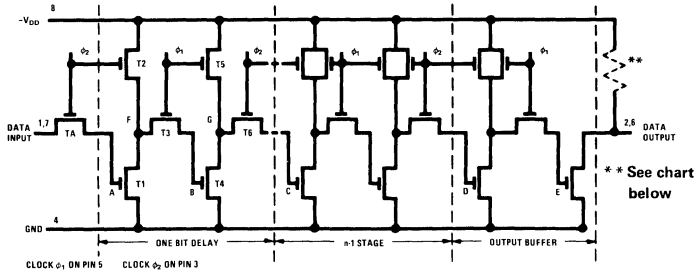
general description

The National Semiconductor line of dynamic shift registers are built on a single silicon chip utilizing MOS P channel enhancement mode transistors. Designed to operate over a wide frequency spectrum, these devices can be used in any sequential digital system that employs a two phase clocking system. The low threshold transistors used permit operation with a V_{DD} supply voltage of −10V and a −16V clock amplitude to obtain these device features:

- Direct DTL or TTL compatibility
- High Frequency Operation — 1 MHz guaranteed
- Low Power Consumption — 0.8 mW/bit @ 1 MHz
- Minimum Operating Frequency Guarantee — 600Hz @ 25°C
- Military and Commercial Temperature Ranges
  MM400 Series −55°C to +125°C
  MM500 Series 0°C to +70°C
- Low Output Impedance (V_{OH}) — 500 ohms
- Clock inputs directly compatible with MH0009, two phase clock driver

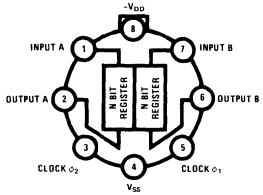
The power dissipation of the device decreases as the operating frequency is decreased; at 10 kHz typical dissipation is 6 μW/bit. The minimum operating frequency is also reduced substantially at lower temperatures; typical minimum frequency of operation at 25°C is 100 Hz.

schematic and connection diagrams



** See chart below

Metal Can Package

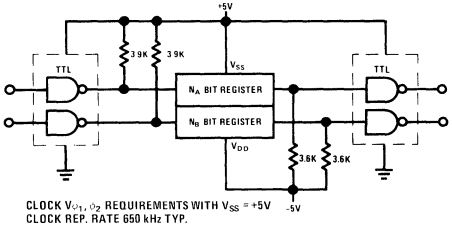


Note: Pin 4 connected to case.
TOP VIEW

Order Number MM400H, MM500H, MM401H, MM501H, MM402H, MM502H, MM403H, MM503H, MM406H, MM506H, MM407H or MM507H
See Package 23

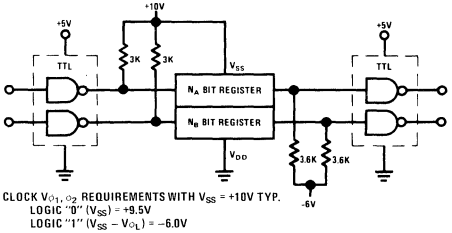
typical applications

FIGURE 1 – TTL/MOS Interface–Low Frequency
(see clock timing graph for detail)



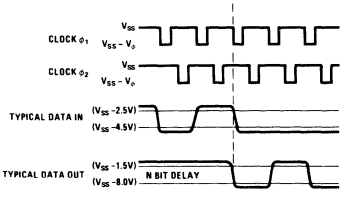
CLOCK Vφ1, φ2 REQUIREMENTS WITH VSS = +5V
CLOCK REP. RATE 650 kHz TYP.
LOGIC "0" (VSS) = +4.5V
LOGIC "1" (VSS − Vφ1) = −10V

FIGURE 2 – TTL/MOS Interfaces



CLOCK Vφ1, φ2 REQUIREMENTS WITH VSS = +10V TYP.
LOGIC "0" (VSS) = +9.5V
LOGIC "1" (VSS − Vφ1) = −6.0V

Waveforms for Applications



Standard Register Configurations †

CONFIGURATION	OPEN DRAIN OUTPUT		20 KΩ OUTPUT	
	−55°C to +125°C	−25°C to +70°C	−55°C to +125°C	−25°C to +70°C
Dual 25 bit	MM400	MM500	MM401	MM501
Dual 50 bit	MM402	MM502	MM403	MM503
*Dual 100 bit	MM406	MM506	MM407	MM507

†For other length registers consult your National representative.
*For New Designs, See MM4006A/MM5006A Data Sheet.

absolute maximum ratings

Drain Voltage ($-V_{DD}$)	+0.5V to −25V
Clock Inputs ($V\phi_1$, $V\phi_2$)	+0.5V to −25V
Data Inputs	+0.5V to −25V
Power Dissipation (Note 1)	500 mW
Operating Temperature	
MM400 Series	−55°C to +125°C
MM500 Series	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Repetition Rate	See Fig. 2	See Note 5		1.0	MHz
	See Fig. 1	See Note 5		0.5	MHz
Clock Input Capacitance (Pins 3 & 5)	f = 1.0 MHz, 0V Bias				
	MM400, 401, 500, 501		22	40	pF
	MM402, 403, 502, 503		40	60	pF
	MM406, 407, 506, 507		85	100	pF
	−20V Bias				
	MM400, 401, 500, 501		18	25	pF
	MM402, 403, 502, 503		32	40	pF
	MM406, 407, 506, 507		55	65	pF
Data Output Voltage Levels					
MOS to MOS	V_{DD} = −10V, V_{SS} = GND				
Logic "0" (V_{OH})	freq = 1 MHz max. Input (d.c.)			V_{SS} −1.5	V
Logic "1" (V_{OL})		V_{SS} −8.0V			V
MOS to TTL (Fig. 1)	V_{DD} = GND, V_{SS} = +10V freq = 1 MHz max. Input (d.c.)				
Logic "0" (V_{OH})	I_L = 2.5 mA } See Note 6	2.5			V
Logic "1" (V_{OL})	I_L = −1.6 mA } See Note 6			0.4	V
MOS to TTL (Fig. 2)	V_{DD} = −5V, V_{SS} = +5V (V_{SS} = 4.75 min) freq = 0.5 MHz max.				
Logic "0" (V_{OH})	I_L = 2.5 mA } See Note 6	2.5			V
Logic "1" (V_{OL})	I_L = −1.6 mA } See Note 6			0.4	V
Breakdown Voltage	1.0 μA Test Current T_A = 25°C				
On Pin 1	GND on Pins 2, 3, 4, 5, 6, 7 −8V on Pin 8	−25			V
On Pin 2 (Note 3)	GND on Pins 1, 4, 6, 7, 8 −8V on Pins 3, 5	−25			V
On Pin 6 (Note 3)	GND on Pins 1, 2, 4, 7, 8 −8V on Pins 3, 5	−25			V
On Pin 7	GND on Pins 1, 2, 3, 4, 5, 6 −8V on Pin 8	−25			V
Leakage Current	T_A = 25°C				
Pin 1	V_1 = −18V, V_8 = −8V All Other Pins at GND			0.5	μA
Pin 2 (Note 4)	V_2 = −18V, V_3 = V_5 = −8V All Other Pins at GND			0.5	μA
Pin 6 (Note 4)	V_6 = −18V, V_3 = V_5 = −8V All Other Pins at GND			0.5	μA
Pin 7	V_7 = −18V, V_8 = −8V All Other Pins at GND			0.5	μA
Pin 8 (Note 4)	V_8 = −8V All Other Pins at GND			0.5	μA
Power Supply Current Drain	Outputs at Logic "1" 1 MHz Operations, T_A = 25°C (ϕ_1 = 0.4 μs, ϕ_2 = 0.2 μs)				
	MM400,401,500,501		4.5	9.0	mA
	MM402,403,502,503		9.0	14.0	(Average)
	MM406,407,506,507		18.0	30.0	

electrical drive requirements

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Pulse Width	See Timing Diagram				
ϕ_1 Clock pw		0.4		10.0	μs
ϕ_2 Clock pw		0.2		10.0	μs
Clock Delay, ϕ_d	See Definition	0.1			μs
Clock Pulse Transition $t_{r\phi}$, $t_{f\phi}$	1 MHz, ϕ_{pw} = 0.2 μs			0.05	μs
	100 kHz, ϕ_{pw} = 0.2 μs			0.5	μs
	10 kHz, ϕ_{pw} = 10 μs			5.0	μs
Clock Input Level (V_ϕ)					
Logic "0" ($V_{\phi H}$)			V_{SS} −0.5	V_{SS} −1.5	V
Logic "1" ($V_{\phi L}$)		V_{SS} −14.5	V_{SS} −16.0	V_{SS} −18.0	V
Data Pulse Width t_{dw}		0.4			μs
Data Setup Time t_{ds}		0.1			μs
Data Input Voltage Levels					
MOS to MOS					
Logic "0" (V_{IH})	V_{DD} = −10V, V_{SS} = GND			2.0	V
Logic "1" (V_{IL})	freq = 1 MHz max.	−7.0			V
TTL to MOS (Fig. 1)					
Logic "0" (V_{IH})	V_{DD} = GND, V_{SS} = +10V			V_{SS} 2.0	V
Logic "1" (V_{IL})	freq = 1 MHz max.	V_{SS} −7.0			V
TTL to MOS (Fig. 2)					
Logic "0" (V_{IH})	V_{DD} = −5V, V_{SS} = +5V			V_{SS} 1.5	V
Logic "1" (V_{IL})	(V_{SS} = 4.75 min)				
	freq = 0.5 MHz max.	V_{SS} −4.2			V

Note 1: For operating at elevated temperatures, the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +150°C/W junction to ambient. The full rating applies for case temperatures to +125°C for MM400 Series and +70°C for MM500 Series units.

Note 2: These specifications apply over the indicated operating temperature ranges for V_{SS} = 0V and −11V < V_{DD} < −9.5V and 20 kΩ connected between pins 2 and 8 and between pins 6 and 8 without measurement load of less than 10 pF in parallel with 10 MΩ to ground unless otherwise specified. On the MM401/MM501, MM403/MM503, and MM407/MM507 optional versions which include 20 kΩ pull-up resistors internal to package, the external 20 kΩ resistors are not used in measurement circuits.

Note 3: For the odd number devices, MM401, MM403 and MM407, the output of pins 2 and 6 will exhibit a resistance when measured with the following bias conditions: pins 1, 6 and 8 = GND: pins 3 and 5 = −16V; pin 4 = open; measure pins 2 and 6 = 25k ≤ R_{OUT} ≤ 15 kΩ.

Note 4: Not for internal resistor devices.

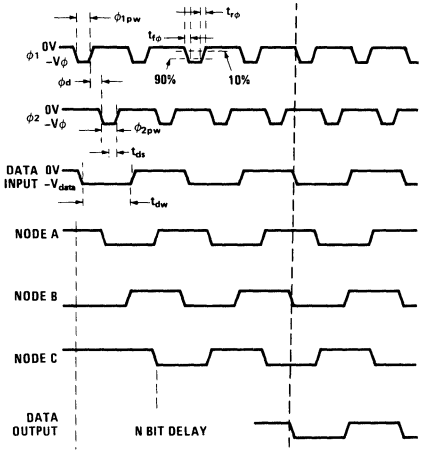
Note 5: See minimum operating frequency graph.

Note 6: In the logic "0" (V_{OH}) level the MOS register output will be sourcing 2.5 mA into the load combination of the pull-down resistors and the gate leakage current. In the logic "1" V_{OL} level I_L represents the current that the pull-down resistor and the internal 20k resistor combination will sink in order to insure current sinking capability for one gate.

operation

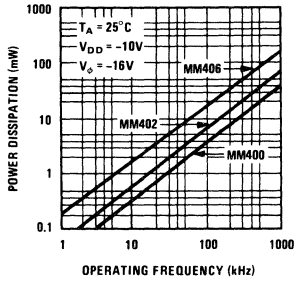
Each bit of delay shown in the circuit schematic consists of two inverters T1 and T4 accompanied by clocked load resistors T2 and T5 and two coupling devices T3 and T6. The circuit functions as follows: When ϕ_2 goes negative (one state) the coupling unit TA and the load resistor T2 are clocked ON allowing information at the input to be transferred to node A turning T1 ON or OFF depending on the state of the input. For example, if a negative potential (near $-V_{DD}$ level) is transferred from the input to the gate to source capacitance at node A, then T1 turns ON allowing node F to be at $\frac{-V_{DD}}{2}$. When ϕ_2 returns to its zero state (ground level) T2 turns OFF allowing node F to discharge to zero volts. When ϕ_1 goes negative (one state) the coupling unit T3 and the load resistor T5 are clocked ON allowing information at node F to be transferred to node B. T4 is held OFF if node F was at ground potential and is turned ON if node F had been at $-V_{DD}$ potential. Continuing the example above, T4 is held OFF and node G is at $-V_{DD}$ since T5 is ON during ϕ_1 clock pulse. When ϕ_1 returns to its zero state, node G maintains a $-V_{DD}$ voltage level. This voltage level is maintained at node G until the ϕ_2 clock appears. The bit delay demonstrated in this example is repeated through each half of the dual register.

timing diagram

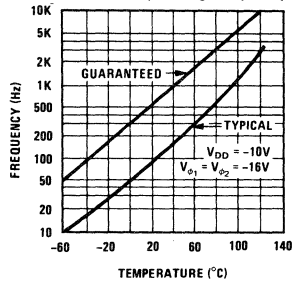


performance characteristics

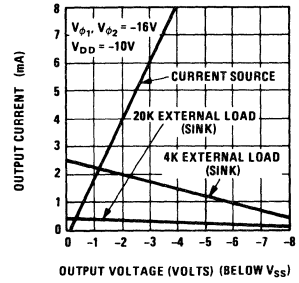
Power Dissipation vs Maximum Frequency



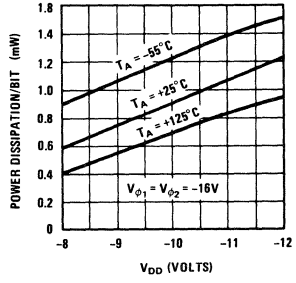
Minimum Operating Frequency



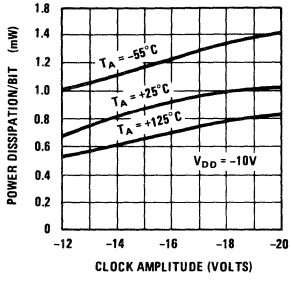
Output Sink/Source Current



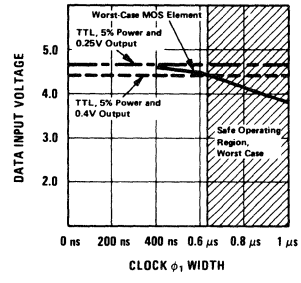
Power Dissipation/Bit vs. Supply Voltage



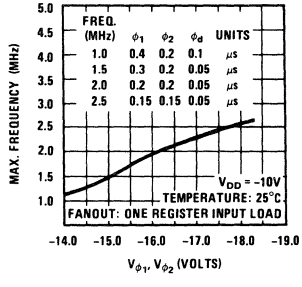
Power Dissipation/Bit vs. Clock Amplitude



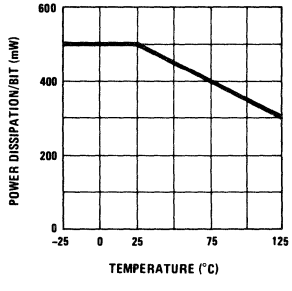
Clock Timing, Direct-Coupled TTL or DTL



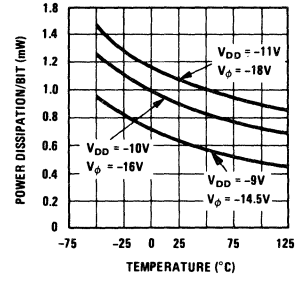
Clock Amplitude V_{ϕ_1}, V_{ϕ_2} vs. Maximum Frequency



Maximum Package Power Dissipation



Power Dissipation/Bit vs. Temperature



Note: All typical performance data is gathered with ϕ_{pw} = 0.4 μ; ϕ_{2pw} = 0.2 μs; ϕ_d = 0.1 μs; f = 1 MHz; except as otherwise noted.

Dynamic Shift Registers

MM1402A/MM1403A/MM1404A/MM5024A
1024-bit dynamic shift registers

general description

The MM1402A/MM1403A/MM1404A/MM5024A 1024-bit dynamic shift registers are MOS monolithic integrated circuits using silicon gate technology to achieve bipolar compatibility. 5 MHz data rates are achieved by on-chip multiplexing. The clock rate is one-half the data rate; i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

All devices in the family can operate from +5V, −5V, or +5V, −9V power supplies.

features

- Guaranteed 5 MHz operation
- Low power dissipation .1 mW/bit at 1 MHz
- DTL/TTL compatible
- Low clock capacitance 125 pF
- Low clock leakage $\leq 1\ \mu A$
- Inputs protected against static charge
- Operation from +5V, −5V or +5V, −9V power supplies
- Seven standard configurations

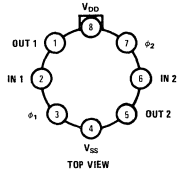
MM1402AD	Quad 256-bit
MM1402AN	Quad 256-bit
MM1403AH	Dual 512-bit
MM1403AN	Dual 512-bit
MM1404AH	Single 1024-bit
MM1404AN	Single 1024-bit
MM5024AH	Single 1024-bit with internal pull-down resistor

applications

- Radar and sonar processors
- CRT displays
- Terminals
- Desk top calculators
- Disk and drum replacement
- Computer peripherals
- Buffer memory
- Special purpose computers—signal processors, digital filtering and correlators, receivers, spectral compressors and digital differential analyzers
- Telephone equipment
- Medical equipment

connection diagrams

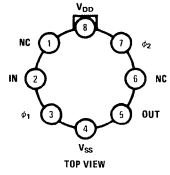
Metal Can Package



TOP VIEW

Order Number MM1403AH
See Package 23

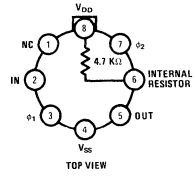
Metal Can Package



TOP VIEW

Order Number MM1404AH
See Package 23

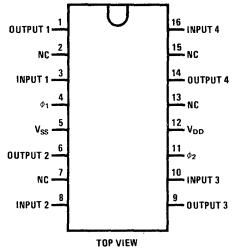
Metal Can Package



TOP VIEW

Order Number MM5024AH
See Package 23

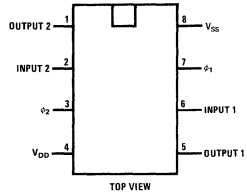
Dual-In-Line Package



TOP VIEW

Order Number MM1402AD
See Package 3
Order Number MM1402AN
See Package 15

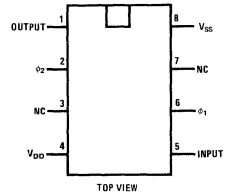
Dual-In-Line Package



TOP VIEW

Order Number MM1403AN
See Package 12

Dual-In-Line Package



TOP VIEW

Order Number MM1404AN
See Package 12

absolute maximum ratings

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW at T_A = 25°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A = −25°C to +70°C, V_{SS} = 5V ±5%, V_{DD} = −5V ±5% or −9V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical Low Level (V_{IL})		V_{SS} − 10.0		V_{SS} − 4.2	V
Logical High Level (V_{IH})		V_{SS} − 1.7		V_{SS} + 0.3	V
Data Input Leakage Current	V_{IN} = −15V, T_A = 25°C, All Other Pins GND		<10	500	nA
Input Capacitance	V_{IN} = V_{SS}		5	10	pF
Clock Input Levels	V_{DD} = −5V ± 5%				
Logical Low Level ($V_{\phi L}$)		V_{SS} − 17		V_{SS} − 15	V
Logical High Level ($V_{\phi H}$)		V_{SS} − 1		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)	V_{DD} = −9V ± 5%	V_{SS} − 14.7		V_{SS} − 12.6	V
Logical High Level ($V_{\phi H}$)		V_{SS} − 1		V_{SS} + 0.3	V
Clock Leakage Current	Min $V_{\phi L}$, T_A = 25°C		10	1000	nA
Clock Capacitance	V_ϕ = V_{SS}		90	125	pF
Data Output Levels					
Logical Low Level (V_{OL})	R_{L1} = 3k to V_{DD}, I_{OL} = 1.6 mA, V_{DD} = −5V ± 5%		−0.3	0.5	V
Logical High Level (V_{OH})	R_{L1} = 3k to V_{DD}, I_{OH} = 100 μA	2.4	3.5		V
Logical Low Level (V_{OL})	R_{L1} = 4.7k to V_{DD}, I_{OL} = 1.6 mA, V_{DD} = −9V ± 5%		−0.3	0.5	V
Logical High Level (V_{OH})	R_{L1} = 4.7k to V_{DD}, I_{OH} = 100 μA	2.4	3.5		V
Logical High Level (V_{OH})	R_{L2} = 4.7k to V_{DD}, V_{DD} = −5V ± 5%	V_{SS} − 1.9	V_{SS} − 1		V
Logical High Level (V_{OH})	R_{L2} = 6.2k to V_{DD}, V_{DD} = −9V ± 5% R_{L3} = 3.9k to V_{SS}	V_{SS} − 1.9	V_{SS} − 1		V
Power Supply Current (I_{DD})	T_A = 25°C, V_{DD} = −5V ± 5% Output Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, $V_{\phi L}$ = V_{SS} − 17V		35	50	mA
	T_A = 0°C			56	mA
	T_A = 25°C, V_{DD} = −9V ± 5% Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, $V_{\phi L}$ = V_{SS} − 14.7V		30	40	mA
	T_A = 0°C			45	mA
Data Output Leakage Current	V_{OUT} = 0.0V, T_A = 25°C, $V_{\phi 1}$ = $V_{\phi 2}$ = V_{SS} − 10V, All Other Pins +5V		<10	1000	nA
Internal Resistor (MM5024A)	T_A = 25°C	3.7	4.7	5.2	kΩ
Output Capacitance	V_{OUT} = V_{SS}, f = 1 MHz		5	10	pF

ac characteristics

T_A = −0°C to +70°C, V_{SS} = 5V ±5%

PARAMETER	V_{DD} = −5V ± 5%		V_{DD} = −9V ± 5%		UNITS
	MIN	MAX	MIN	MAX	
Clock Frequency (ϕ_f)	Note 1	2.5	Note 1	1.5	MHz
Data Frequency		5.0		3.0	MHz
Clock Pulse Width (ϕ_{PW})	0.130	10	0.170	10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	10	Note 1	10	Note 1	ns
Clock Transition Times (ϕt_r, ϕt_f)		1000		1000	ns
Data Input Delay Time (t_{ds})	30		60		ns
Data Input Hold Time (t_{dH})	20		20		ns
Data Output Propagation Delay		90		110	ns

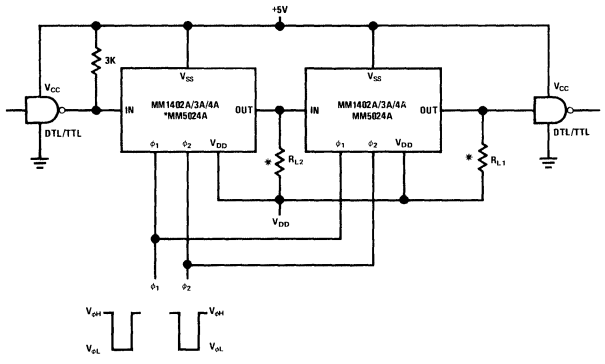
Note 1: Minimum clock frequency is a function of temperature and clock phase delay times, ϕ_d and $\overline{\phi}_d$ as shown by the ϕ_f versus temperature and ϕ_d, $\overline{\phi}_d$ versus temperature curves. The lowest guaranteed clock frequency can be attained by making ϕ_d equal to $\overline{\phi}_d$. The minimum guaranteed clock frequency is:

$\phi_f(\text{min}) \cong 1/(\phi_d + \overline{\phi}_d)$ for the condition ($\phi t_r = \phi t_f << \phi_{PW} << \phi_d$ or $\overline{\phi}_d$), where the variables may not exceed the guaranteed maximums.

Note 2: Capacitance is guaranteed by periodic testing.

typical application

DTL/TTL to MOS Interface



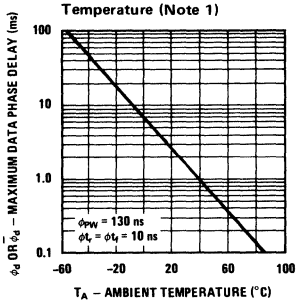
*A 4.7 kΩ resistors is included on the chip in the MM5024A and is connected between Pin 6 and V_{DD}.

R_L Load Resistor Value for Different V_{DD} Supplies

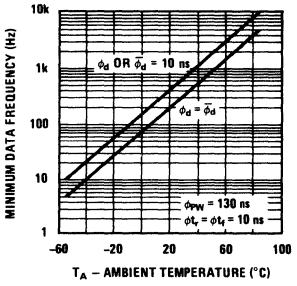
	V_{SS} = 5V V_{DD} = −5V	V_{SS} = 5V V_{DD} = −9V
R_{L1}	3.0k	4.7k
R_{L2}	4.7k	6.8k
R_{L3}	Not required	Not required

performance curves

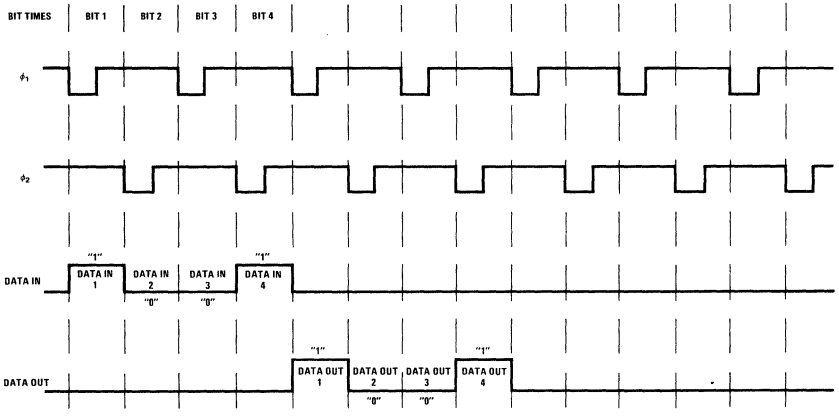
Guaranteed Maximum Data Phase Delay Times vs Temperature (Note 1)



Guaranteed Minimum Data Frequency vs Temperature (Note 1)

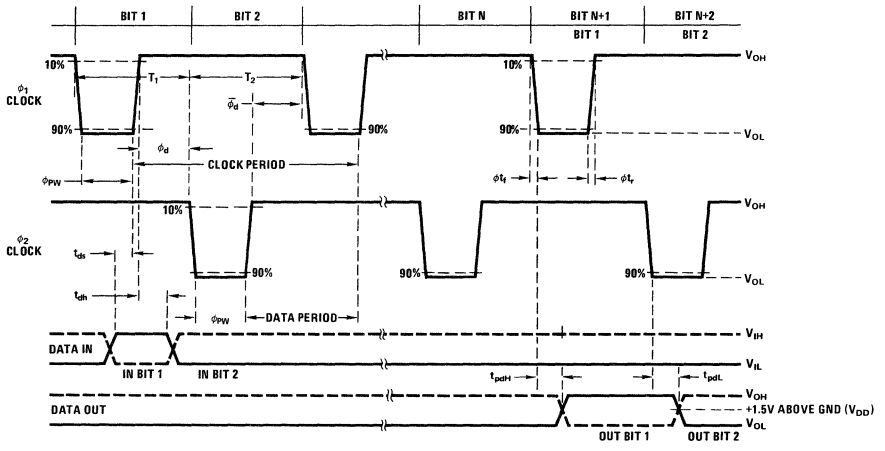


switching time waveforms



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ_1 time, it exists at ϕ_1 time. (Beginning on $\phi_{1's}$ negative going edge and ending on the succeeding $\phi_{2's}$ negative going edge.)

timing diagram



Dynamic Shift Registers

MM4001A/MM5001A dual 64-bit dynamic shift register
MM4010A/MM5010A dual 64-bit accumulator

general description

The MM4001A/MM5001A dual 64-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P-channel enhancement mode low threshold technology. The device consists of two 64-bit registers with independent two phase clocks and is guaranteed to operate at a 2.5 MHz operating frequency for CRT display applications.

The MM4010A/MM5010A is a dual accumulator function capable of operating at very high frequency. The device is also constructed on a single silicon chip utilizing MOS P-channel enhancement transistors. With the recirculate control line at an MOS logic "0" state, the device functions as an accumulator. A logic "1" state at the recirculate control line allows external information to enter the register serially. It is important to note that recirculation of data is performed internally, independent of the output circuit thus making it insensitive to output loading.

features

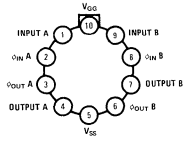
- High frequency operation — 3.3 MHz typ
- Low power consumption — 0.4 mW/bit at 1 MHz
- DTL/TTL compatibility — +5V, −12V power supplies, push-pull output stage
- Minimum operating frequency — guaranteed 250 Hz at 25°C
- Application versatility — "Split clock" operation, independent control of each register for MM4001A/MM5001A

applications

- Business machine
- CRT refresh memory
- Delay line memory
- Arithmetic operations

connection diagrams

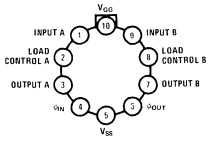
Metal Can Package



Note: Pin 5 connected to case.
TOP VIEW

Order Number MM4001AH or MM5001AH
See Package 24

Metal Can Package



Note: Pin 5 connected to case.
TOP VIEW

Order Number MM4010AH or MM5010AH
See Package 24

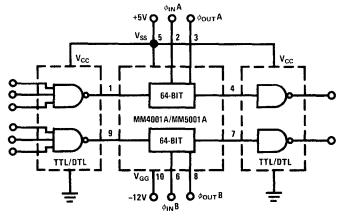
load control truth table

MM4010A/MM5010A

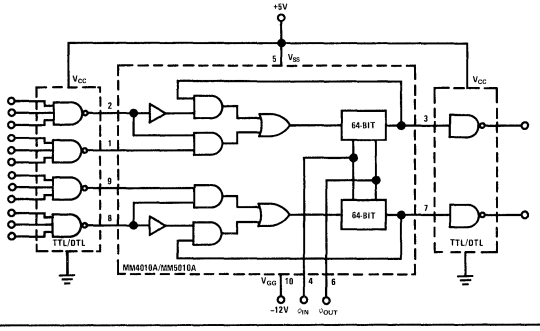
LOGICAL HIGH LEVEL (V_{LCH})	LOGICAL LOW LEVEL (V_{LCL})
Recirculates "old" data	Loads "new" data

typical applications

MM4001A/MM5001A TTL/MOS Interface



MM4010A/MM5010A TTL/MOS Interface



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range	
MM4010A/MM4001A	−55°C to +125°C
MM5010A/MM5001A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2		3.0	5.0	pF
Load Control Input Levels					
Logical HIGH Level (V_{LCH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{LCL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Load Control Input Leakage	V_{IN} = −20V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND				
MM4001A/MM5001A Note 2			17	20	pF
MM4010A/MM5010A Note 2			34	40	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data=0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.0	3.0	mA
	ϕ_f = 1 MHz		3.0	4.5	mA
	ϕ_f = 2.5 MHz		5.0	7.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10	μs
Clock Phase Delay Times ($\phi_d, \overline{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1	μs
Partial Bit Times (T)	Note 1				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Load Control Input Setup Time (t_{LCS})		80	30		ns
Load Control Input Hold Time (t_{LCh})		20	0		ns
Data Output Propagation Delay					
From ϕ_{OUT}	See ac test circuit				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times, T_{IN} and T_{OUT}, as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

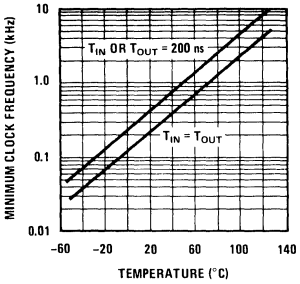
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$

where T_{IN} and T_{OUT} may not exceed the guaranteed maximums.

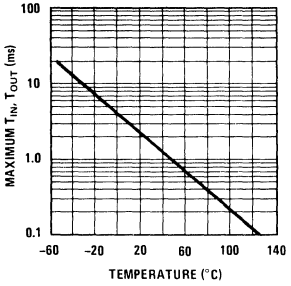
Note 2: Capacitance is guaranteed by lot sample testing.

performance characteristics

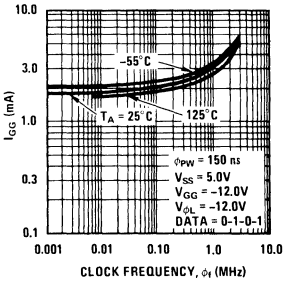
Guaranteed Minimum Clock Frequency vs Temperature (Note 1)



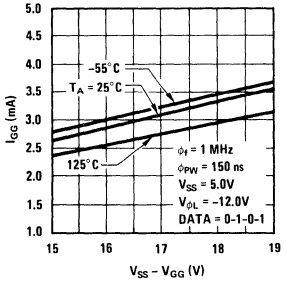
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 1)



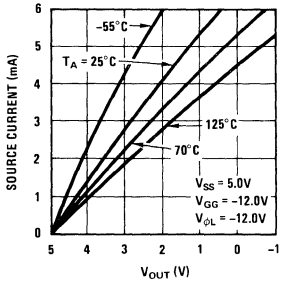
Typical Power Supply Current vs Clock Frequency



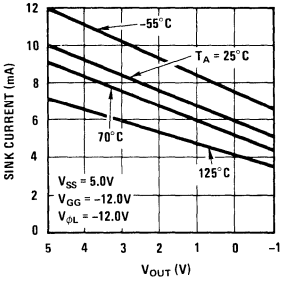
Typical Power Supply Current vs Voltage



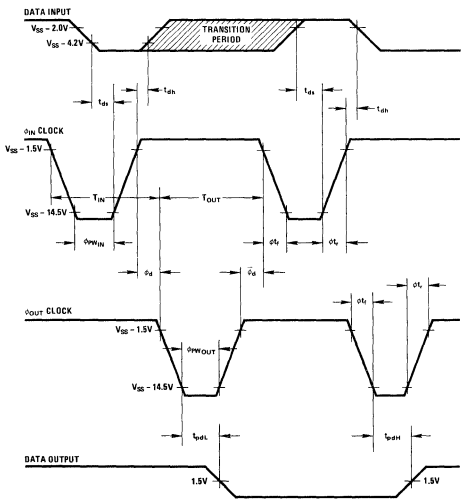
Typical Data Output Source Current vs Data Output Voltage



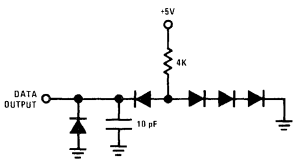
Typical Data Output Sink Current vs Data Output Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM4006A/MM5006A dual 100-bit shift register
MM4007/MM5007 dual 100-bit mask programmable shift register
MM4019/MM5019 dual 256-bit mask programmable shift register

general description

The MM4007/MM5007 and MM4019/MM5019 are monolithic dual 100-bit and dual 256-bit dynamic shift registers utilizing P-channel enhancement mode technology to achieve bipolar compatibility. The length of the registers may be varied at manufacture by the altering of the metal mask providing custom length of both registers. Additional connection between registers may be accomplished at the metal mask to provide single shift register lengths of up to 200 or 512-bits, with or without an appropriate tap provided at the juncture. The MM5006A is an MM5007 programmed as a dual 100-bit shift register.

For the MM4007/MM5007 N = 20 to 100 bits
For the MM4019/MM5019 N = 40 to 256 bits

STANDARD LENGTHS:

MM4006A	Dual 100-bit
MM4007/AA	Dual 80-bit
MM4019	Dual 256-bit

CUSTOM LENGTHS:

The programmed shift registers are assigned a letter code for each option. These are designated by a pair of letters after the number code but before the package designation such as

MM5007/AA/H

which is a 0°C to +70°C dual 80-bit dynamic shift register in the TO-99 package. Pattern codes are assigned by National upon initial order entry. See MOS Brief 14 for a more detailed description of the custom mask.

features

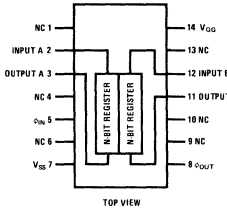
- Bipolar compatibility — Standard +5V, −12V power supplies
- Mask programmable length
  - MM4007/MM5007 — dual 20-100 bits
  - MM4019/MM5019 — dual 40-256 bits
- Low clock capacitance
  - MM4007/MM5007 — 65 pF max
  - MM4019/MM5019 — 125 pF max
- Standard clock frequency — 250 Hz min — typical at 25°C; 2.5 MHz max — guaranteed over temp
- Full temperature range
  - MM4007,MM4019 — −55°C to +125°C
  - MM5007,MM5019 — 0°C to +70°C

applications

- Custom shift registers
- CRT recirculate display

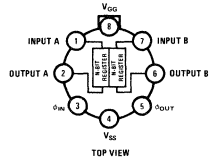
connection diagrams

Dual-In-Line Package



TOP VIEW

Note: Pin 7 connected to case.



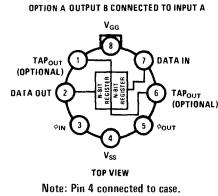
TOP VIEW

Note: Pin 4 connected to case.

Standard Connection

Metal Can Packages

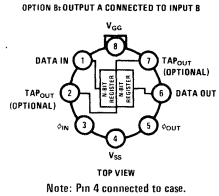
OPTION A OUTPUT B CONNECTED TO INPUT A



TOP VIEW

Note: Pin 4 connected to case.

OPTION B: OUTPUT A CONNECTED TO INPUT B



TOP VIEW

Note: Pin 4 connected to case.

Optional Connections

ordering information

DUAL 80-BIT	DUAL 100-BIT	DUAL 100-BIT	DUAL 256-BIT	PROGRAMMABLE 20 to 100 Bits	PROGRAMMABLE 40 to 256 Bits	SEE PACKAGE
MM4007AA/D	MM4006AD	MM4007D	MM4019D	MM4007XX/D	MM4019XX/D	2
MM4007AA/H	MM4006AH	MM4007H	MM4019H	MM4007XX/H	MM4019XX/H	23
MM5007AA/D	MM5006AD	MM5007D	MM5019D	MM5007XX/D	MM5019XX/D	2
MM5007AA/H	MM5006AH	MM5007H	MM5019H	MM5007XX/H	MM5019XX/H	23

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range	
MM4006A,MM4007,MM4019	−55°C to +125°C
MM5006A,MM5007,MM5019	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −2.0V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)				
MM4006A/MM5006A & MM4007/MM5007			50	65	pF
MM4019/MM5019			95	125	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
MM4006A/MM5006A & MM4007/MM5007	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.0	3.0	mA
MM4019/MM5019			2.5	3.5	mA
MM4006A/MM5006A & MM4007/MM5007	ϕ_f = 1.0 MHz		4.0	6.0	mA
MM4019/MM5019			5.0	7.0	mA
MM4006A/MM5006A & MM4007/MM5007	ϕ_f = 2.5 MHz		6.0	9.0	mA
MM4019/MM5019			9.0	12.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns	.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 2)	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			1.0	μs
Partial Bit Times (T)	(Note 2)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	(See ac test circuit)				
Delay to High Level (t_{pdH})			150	200	ns
Delay to Low Level (t_{pdL})			150	200	ns

Note 1: Capacitance is guaranteed by periodic testing.

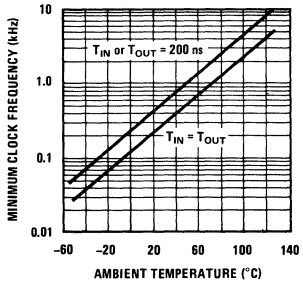
Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi f(min) = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

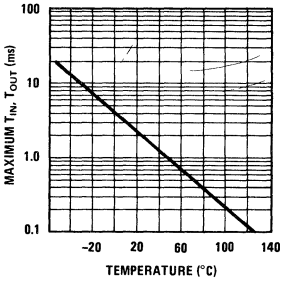
Note 3: Minimum clock frequency and partial bit time curves are guaranteed by testing at a high temperature point.

performance characteristics

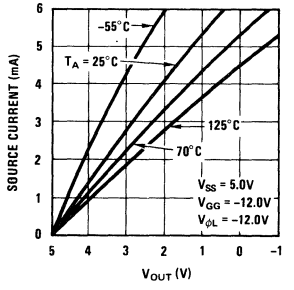
Guaranteed Minimum Clock Frequency vs Temperature (Note 2)



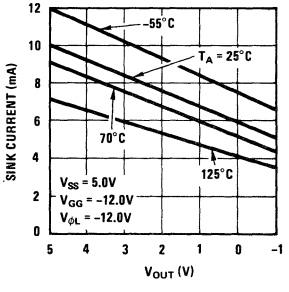
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 2)



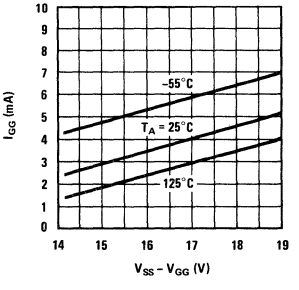
Typical Data Output Source Current vs Voltage



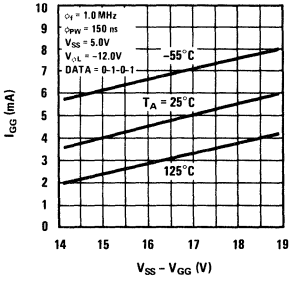
Typical Data Output Sink Current vs Voltage



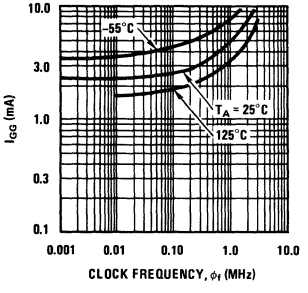
Typical Power Supply Current vs Voltage MM4006A/MM5006A MM4007/MM5007



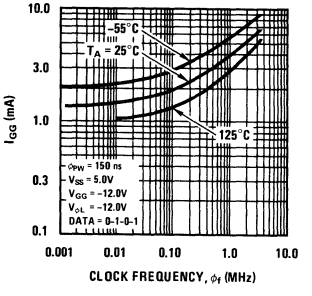
Typical Power Supply Current vs Voltage MM4019/MM5019



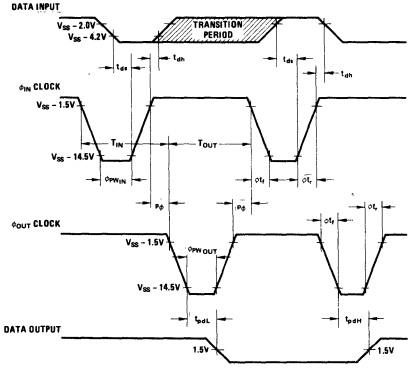
Typical Power Supply Current vs Clock Frequency MM4019/MM5019



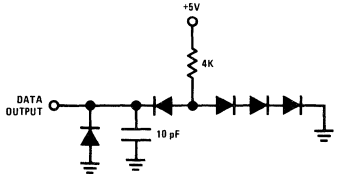
Typical Power Supply Current vs Clock Frequency MM4006A/MM5006A/ MM4007/MM5007



switching waveforms



ac test circuit



Dynamic Shift Registers

MM4013/MM5013 1024-bit dynamic shift register/accumulator

general description

The MM4013/MM5013 1024-bit dynamic shift register/accumulator is an MOS monolithic integrated circuit using P-channel enhancement mode low threshold technology to achieve direct bipolar compatibility. There is on-chip logic to load and recirculate data, and a read control for enabling the bus-ORable TRI-STATE™ push pull output stage.

features

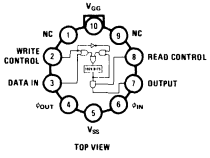
- Bipolar compatibility — Standard +5V, −12V power supplies; No pull down or pull up resistors required
- Package option — TO-99 or molded 8-pin mini-DIP
- Low clock capacitance — 160 pF max
- Wide frequency range — ϕ_f min = 400 Hz @ 25°C typ; ϕ_f max = 2.5 MHz over temp. guaranteed
- Built-in recirculate — Exclusive-OR and recirculate loop on-chip
- TRI-STATE output — Allows wire-OR bus structure on output
- Full temperature operation
  - MM4013 −55°C to +125°C
  - MM5013 0°C to +70°C

applications

- "Silicon Store" replacement for drum and disc memories
- File memories
- CRT refresh

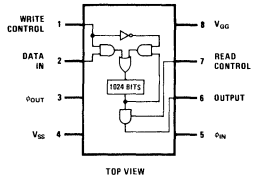
connection diagrams

Metal Can Package



Order Number MM4013H or MM5013H
See Package 24

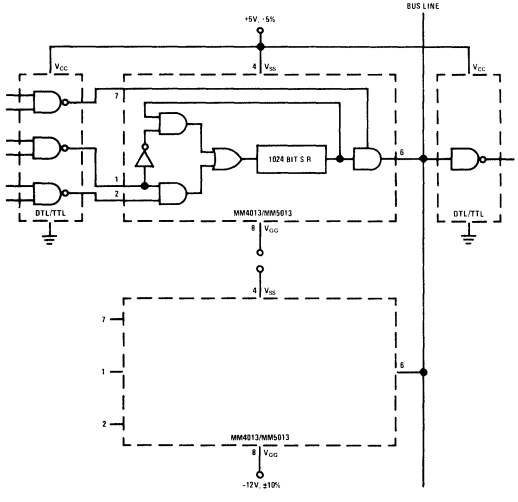
Dual-In-Line Package



Order Number MM4013D or MM5013D
See Package 1
Order Number MM5013N
See Package 12

typical applications

TTL/MOS Interface



truth table

(Positive Logic)
Logic "1" = V_{IH} = Logical HIGH Level
Logic "0" = V_{IL} = Logical LOW Level

WRITE	READ	FUNCTION
0	0	Recirculate Output Disabled
0	1	Recirculate Output Enabled
1	0	Write Mode Output Disabled
1	1	Write Mode Output Enabled

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 22
Operating Temperature Range MM4013	−55°C to +125°C
MM5013	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} −18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		3.0	5.0	pF
Control Input Levels					
Logical HIGH Level (V_H)		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_L)		V_{SS} − 18.5		V_{SS} − 4.2	V
Control Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20.0V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		140	190	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Data Output Leakage	V_{OUT} = −5.0V, T_A = 25°C Output in High Impedance State			10.0	μA
Power Supply Current I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.60	3.0	mA
	ϕ_f = 1.0 MHz		5.3	8.0	mA
	ϕ_f = 2.5 MHz		10.3	15.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 2)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 2)	10.0			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1.0	μs
Partial Bit Times (T)	(Note 2)				
Input Partial Bit Time (T_{IN})		0.2		100	μs
Output Partial Bit Time (T_{OUT})		0.2		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Write Setup Time (t_{ds})		80	30		ns
Write Hold Time (t_{dh})		20	0		ns
Read Setup Time (t_{RS})		0			ns
Read Hold Time (t_{Rh})		0			ns
Data Output Propagation Delay from ϕ_{OUT}	(see ac test circuit)				
Delay to HIGH Level (t_{pd1})			150	200	ns
Delay to LOW Level (t_{pd0})			150	200	ns
Propagation Delay From Read Control Disable to HIGH Impedance State:					
Delay From HIGH Level (t_{1H})			150	200	ns
Delay From LOW Level (t_{0H})			150	200	ns
Propagation Delay From Read Control Enable to LOW Impedance State:					
Delay to HIGH Level (t_{H1})			150	200	ns
Delay to LOW Level (t_{H0})			150	200	ns

Note 1: Capacitance is guaranteed by periodic testing.

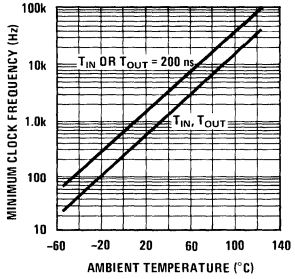
Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

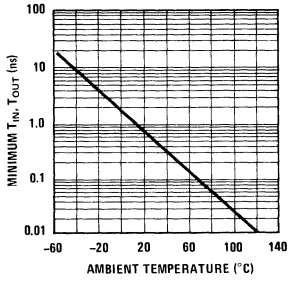
Note 3: Minimum clock frequency and partial bit time curves are guaranteed by testing at a high temperature point.

performance characteristics

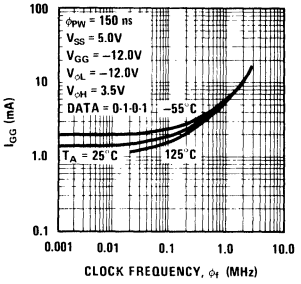
Guaranteed Minimum Clock Frequency vs Temperature (Note 2)



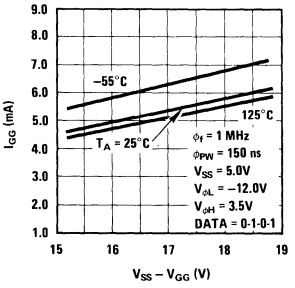
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 2)



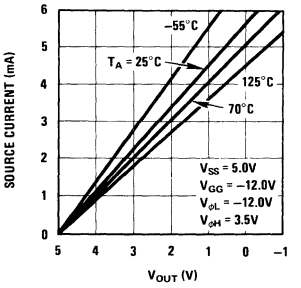
Typical Power Supply Current vs Clock Frequency



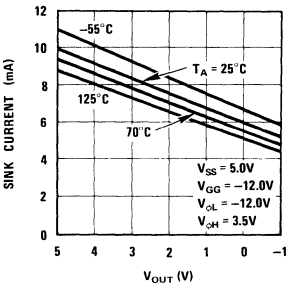
Typical Power Supply Current vs Voltage



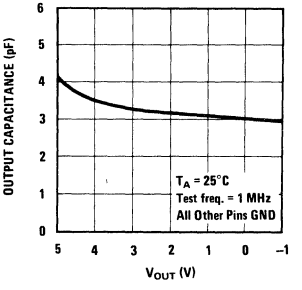
Typical Data Output Source Current vs Data Output Voltage



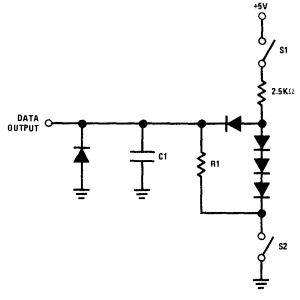
Typical Data Output Sink Current vs Data Output Voltage



Typical Tri-State Data Output Capacitance vs Voltage



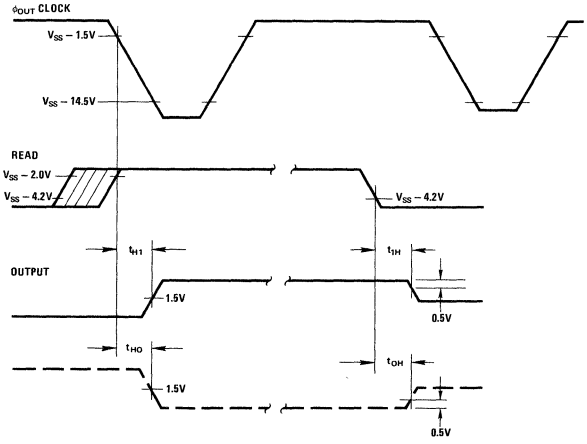
ac test circuit



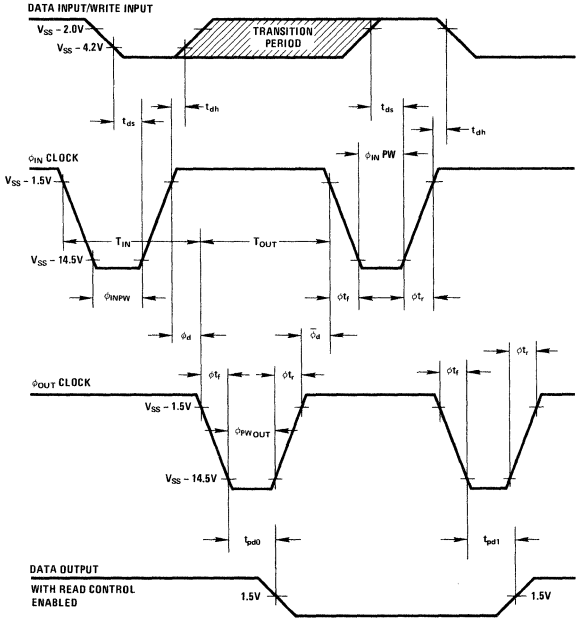
truth table

DELAY	S1	S2	R1	C1
t_{pd0}	Closed	Closed	35K	20 pF
t_{pd1}	Closed	Closed	35K	20 pF
t_{0H}	Closed	Closed	2.5K	5 pF
t_{1H}	Closed	Closed	2.5K	5 pF
t_{H0}	Closed	Open	35K	20 pF
t_{H1}	Open	Closed	35K	20 pF

switching time waveforms



The level of the output when it is in the high impedance state is determined by the external circuitry. The correct data will always appear, after some propagation delay, when the read control is enabled. The guaranteed delay from the high impedance state to the low impedance state requires that the read control is enabled on or before the leading edge of ϕ_{OUT}.



Dynamic Shift Registers

MM4015A/MM5015A triple 60+4 bit accumulator/register

general description

The MM4015A/MM5015A triple 60+4 bit dynamic accumulator is a monolithic MOS integrated circuit utilizing P-channel enhancement mode low threshold technology. The device consists of three independent shift registers with logic to control the entry of external data or to recirculate the data stored in that register. A common two phase clock is required to operate the device.

features

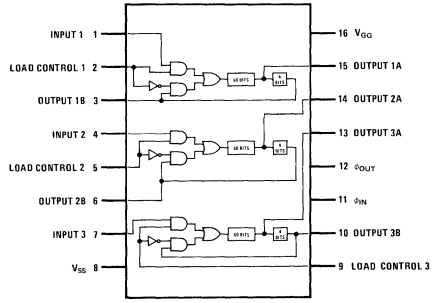
- Direct DTL and TTL compatibility — No pull-up or pull-down resistors required
- High frequency operation — 2.5 MHz guaranteed
- Low frequency operation — 250 Hz at 25°C guaranteed
- Low power consumption — 0.4 mW/bit typically at 1 MHz
- Recirculate logic on-chip
- BCD correction look ahead tap

applications

- Data storage registers in BCD arithmetic applications
- Basic accumulator functions
- Business machine memory applications
- Recirculating delay line

connection diagram

Dual-In-Line Package



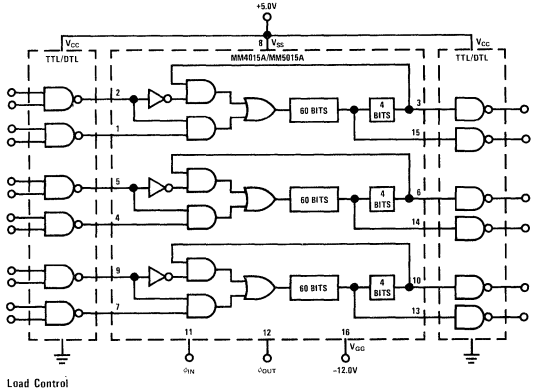
Note: Pin 8 connected to case.

TOP VIEW

Order Number MM4015AD or MM5015AD
See Package 3

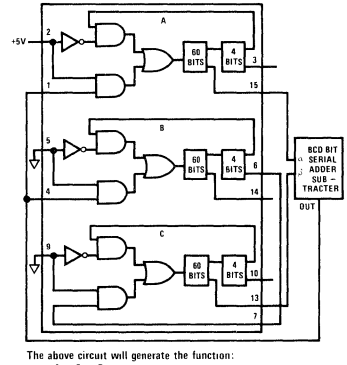
typical applications

TTL/MOS Interface



Load Control
Logical Low – Data is Loaded
Logical High – Data is Recirculated

Typical Arithmetic Configuration



The above circuit will generate the function:
A + C → B
B → C
A → A

absolute maximum ratings

Voltage at Any Pin		V_{SS} + 0.3V to V_{SS} − 22.0V
Operating Temperature Range	MM4015A	−55°C to +125°C
	MM5015A	0°C to +70°C
Storage Temperature Range		−65°C to +150°C

electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND See Note 2		3.0	5.0	pF
Load Control Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Load Control Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND See Note 2		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND See Note 2		45.0	60.0	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = +5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.2	3.0	mA
	ϕ_f = 1 MHz		4.5	5.5	mA
	ϕ_f = 2.5 MHz		7.0	8.5	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10.0	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1.0	μs
Partial Bit Times (T)	Note 1				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Load Input Setup Time (t_{ls})		80	30		ns
Load Input Hold Time (t_{lh})		20	0		ns
Data Output Propagation Delay From ϕ_{OUT}					
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

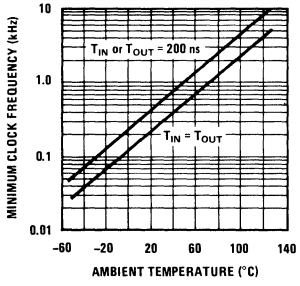
Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

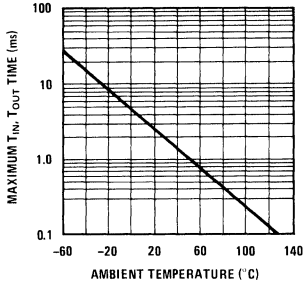
Note 2: Capacitance is guaranteed by periodic testing.

performance characteristics

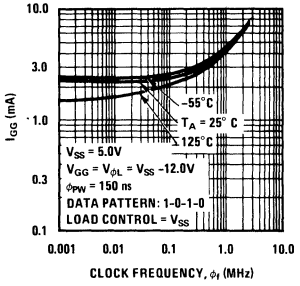
Typical Minimum Clock Frequency vs Temperature (Note 1)



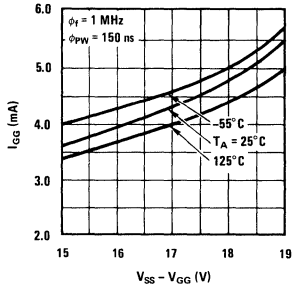
Typical Maximum Partial Bit Times vs Temperature (Note 1)



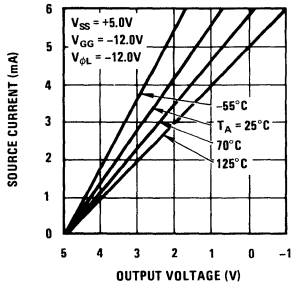
Power Supply Current vs Clock Frequency



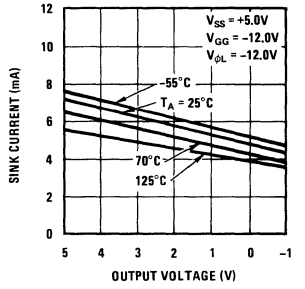
Power Supply Current vs Voltage



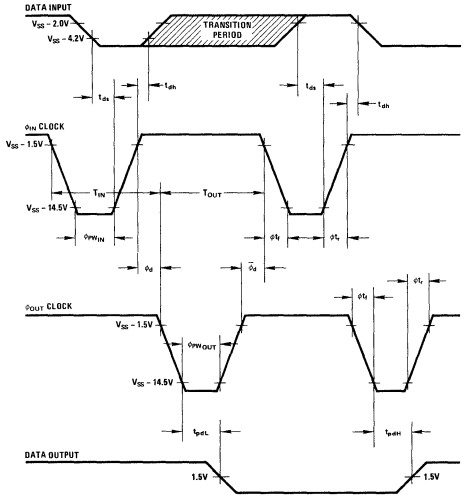
Data Output Source Current vs Voltage



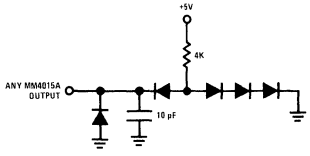
Data Output Sink Current vs Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM4016/MM5016 512-bit dynamic shift register

general description

The MM4016/MM5016 512-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. An input tap provides the option of using the device as either a 500 or 512-bit register.

features

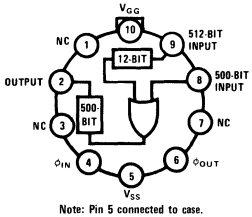
- Bipolar compatibility — +5V, −12V operation. No pull-up or pull-down resistors required.
- Package option — TO-100 or choice of two Dual-In-Line Packages
- Fewer clock drivers required — Clock line capacitance of 100 pF typ
- System flexibility — 300 Hz guaranteed min. operating frequency at 25°C. 500 or 512-bit register length.
- Military and Commercial Temperature Ranges
  MM4016 −55°C to +125°C
  MM5016 0°C to +70°C
- Low power dissipation — < 0.17 mW/bit at 1 MHz max. < 30 μW/bit at 100 kHz typ.

applications

- Glass and magnetostrictive delay line replacement.
- CRT refresh memory.
- Radar delay line.
- Drum memory storage (silicon store)
- Long serial memory.

connection diagrams

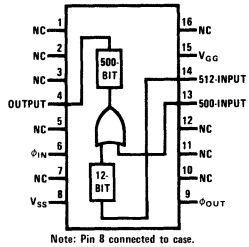
Metal Can Package



Note: Pin 5 connected to case.
TOP VIEW

Order Number MM4016H or MM5016H
See Package 24

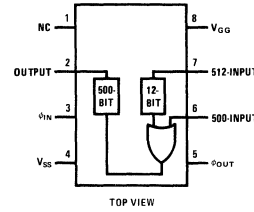
Dual-In-Line Package



Note: Pin 8 connected to case.
TOP VIEW

Order Number MM4016D or MM5016D
See Package 3

Dual-In-Line Package

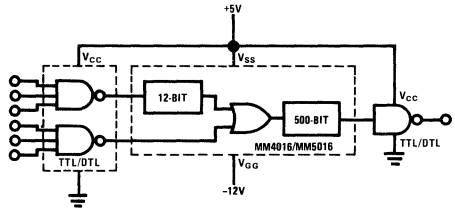


TOP VIEW

Order Number MM5016N
See Package 12

typical application

TTL/MOS Interface



Note: The unused input pin must be connected to V_{SS}.

absolute maximum ratings

Voltage at Any Pin		V_{SS} + 0.3V to V_{SS} −22V
Operating Temperature Range	MM4016	−55°C to +125°C
	MM5016	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = − 20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 2)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND, (Note 2)		100	120	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		1.0	2.0	mA
	ϕ_f = 1 MHz		3.5	5.0	mA
	ϕ_f = 2.5 MHz		7.0	10.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 1)	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			1	μs
Partial Bit Times (T)	(Note 1)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit.				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

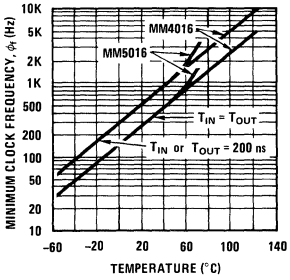
Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi f(min) = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

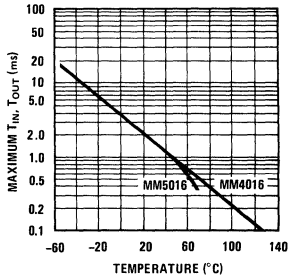
Note 2: Capacitance is guaranteed by periodic testing.

performance characteristics

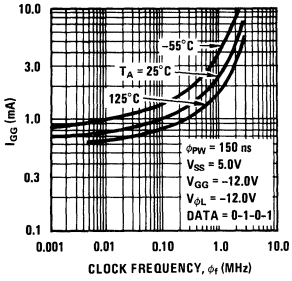
Typical Minimum Clock Frequency vs Temperature (Note 1)



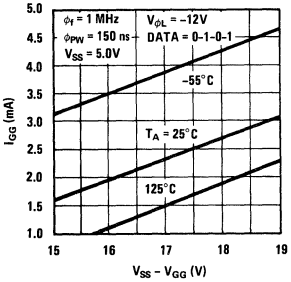
Typical Maximum T_{IN} and T_{OUT} vs Temperature (Note 1)



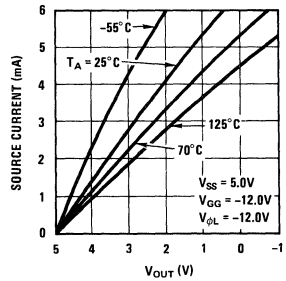
Typical Power Supply Current vs Clock Frequency



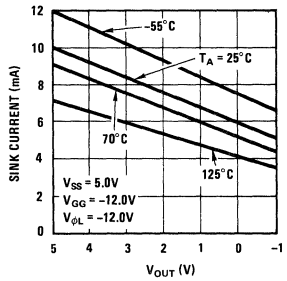
Typical Power Supply Current vs Voltage



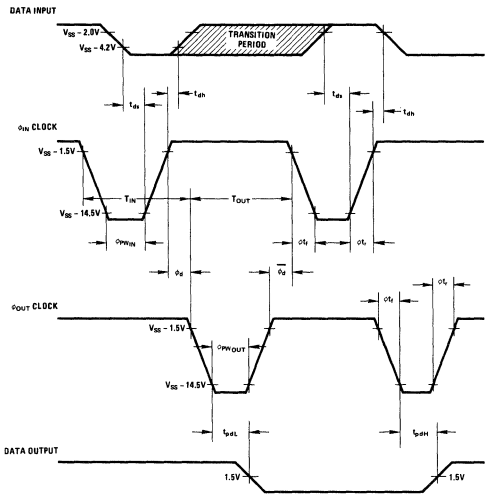
Typical Data Output Source Current vs Voltage



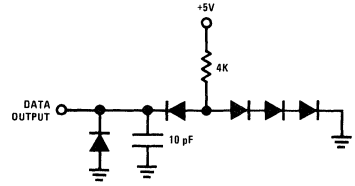
Typical Data Output Sink Current vs Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM4017/MM5017 dual 512-bit dynamic shift register

general description

The MM4017/MM5017 dual 512-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. An input tap provides the option of using either register in a 500-bit or 512-bit configuration.

features

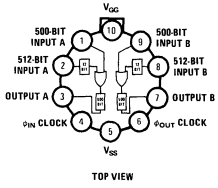
- Standard +5V, −12V supplies — Bipolar compatibility. No pull-up or pull-down resistors required.
- Package option TO-100 or Dual-In-Line Package.
- Fewer clock drivers required — Clock line capacitance of 140 pF typ.
- System flexibility — 400 Hz guaranteed min. operating frequency at 25°C. 500 or 512-bit register length.
- Military and Commercial Temperature Ranges
  MM4017 −55°C to +125°C
  MM5017 0°C to +70°C
- Low power dissipation — <0.17 mW/bit at 1 MHz max. < 30 μW/bit at 100 kHz typ.

applications

- Glass and magnetostrictive delay line replacement
- CRT refresh memory
- Radar delay line
- Drum memory storage (silicon store)
- Long serial memory

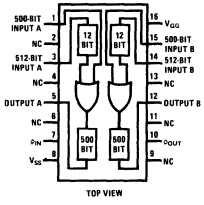
connection diagrams

Metal Can Package



Order Number MM4017H or MM5017H
See Package 24

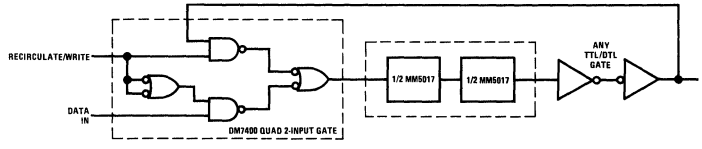
Dual-In-Line Package



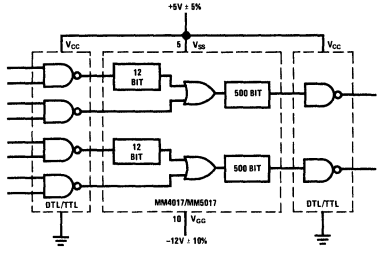
Order Number MM4017D or MM5017D
See Package 3
Order Number MM5017N
See Package 15

typical applications

1000 or 1024 Bit Accumulator



TTL/MOS Interface



Note: Unused input(s) should be tied to V_{SS}.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} - 22
Operating Temperature MM4017	-55°C to +125°C
MM5017	0°C to +70°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = -12.0V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} - 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} -18.5		V_{SS} - 4.2	V
Data Input Leakage	V_{IN} = -20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0V, f = 1 MHz, All Other Pins GND		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} - 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} -18.5		V_{SS} - 14.5	V
Clock Input Leakage	V_ϕ = -20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0V, f = 1 MHz, All Other Pins GND		140	160	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = -0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = -12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = -12V, Data = 0-1-0-1				
	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		2.1	3.2	mA
	ϕ_f = 1 MHz		7.0	10.5	mA
	ϕ_f = 2.5 MHz		10.0	14.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			1.0	μs
Partial Bit Times (T)					
Input Partial Bit Time (T_{IN})		0.20		Note 1	μs
Output Partial Bit Time (T_{OUT})		0.20		Note 1	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

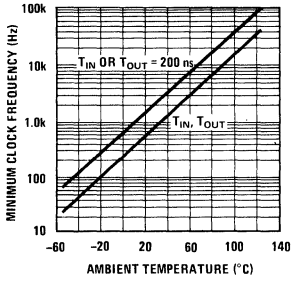
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

Note 2: The curves are guaranteed by testing at a high temperature point.

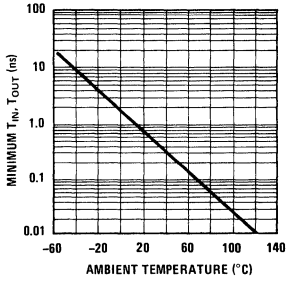
Note 3: Capacitance is guaranteed by periodic testing.

performance characteristics

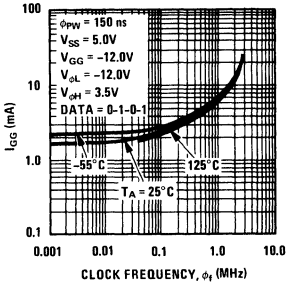
Guaranteed Minimum Clock Frequency vs Temperature (Notes 1 and 2)



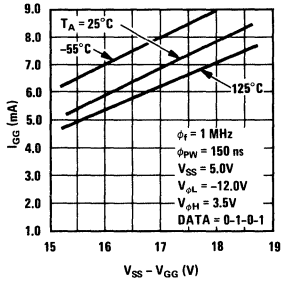
Guaranteed Maximum T_{IN} and T_{OUT} (Notes 1 and 2)



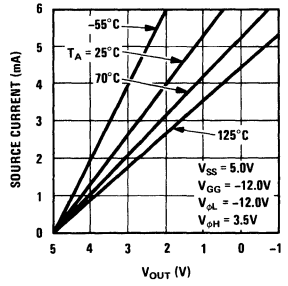
Typical Power Supply Current vs Clock Frequency



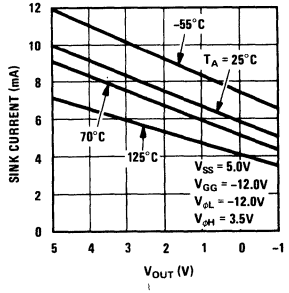
Typical Power Supply Current vs Voltage



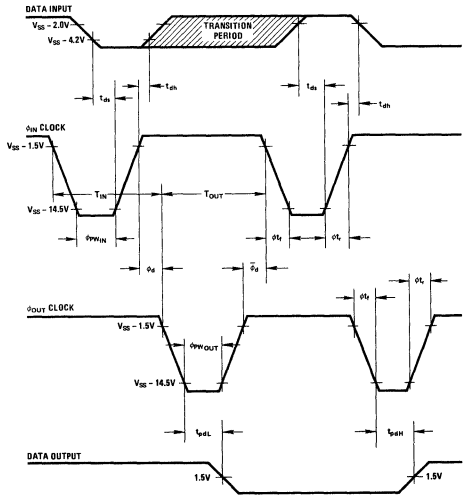
Typical Data Output Source Current vs Data Output Voltage



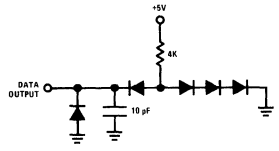
Typical Data Output Sink Current vs Data Output Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM5023 quad 80-bit dynamic shift register

general description

The MM5023 quad 80-bit dynamic shift register is a monolithic MOS integrated circuit using ion implanted P-channel technology. Pull-up resistors are provided on each logic input thus all inputs are directly TTL/DTL compatible. Push-pull output buffers can drive TTL/DTL directly.

Each register has logic to load and recirculate data. All four registers operate from a common single-phase clock.

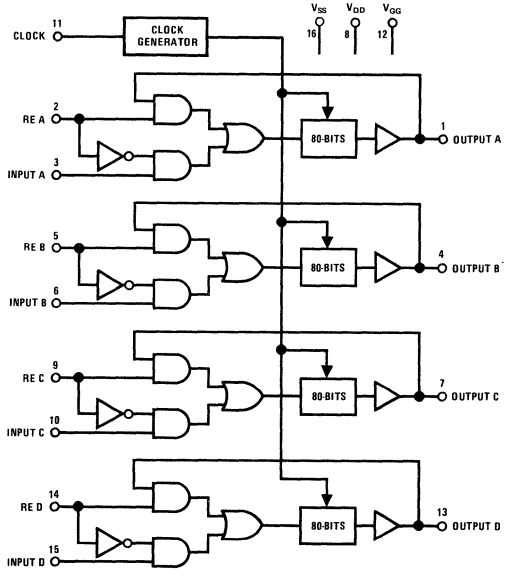
features

- TTL compatibility on all inputs and outputs
- +5V, −12V power supplies
- Single phase TTL level clock
- 2.5 MHz clock rate
- Internal pull-up resistors on all logic inputs
- Load and recirculate logic on each register
- Input protection against static charge

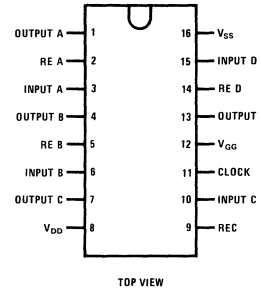
applications

- Delay lines
- Buffer data storage
- CRT display systems
- Digital filters
- Terminals

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5023D
See Package 3
Order Number MM5023N
See Package 15

absolute maximum ratings

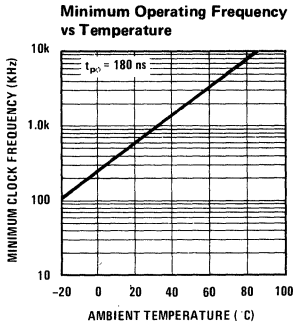
Supply Voltage, V_{DD}	V_{SS} − 10V
Supply Voltage, V_{GG}	V_{SS} − 20V
Voltage at Any Input or Output	V_{SS} + 0.3 to V_{SS} − 10V
Operating Free-Air Temperature Range	0°C to +75°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

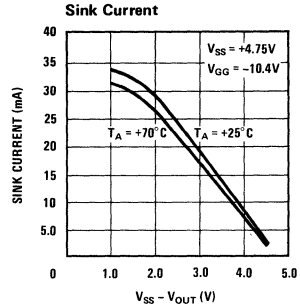
electrical characteristics V_{SS} = +5.0V ±5%, V_{DD} = GND, V_{GG} = −12V ±5%. T_A within operating temperature range unless otherwise stated.

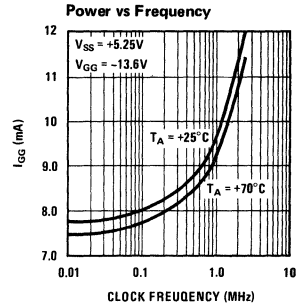
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, RE, and Clock Input Levels	(Note 2)				
Logical High Level (V_{IH})		V_{SS} − 1.5	+5.0	V_{SS} + 0.3	V
Logical Low Level (V_{IL})			0	0.8	V
Data, RE, and Clock Input Leakage	V_{IN} = V_{SS} − 5.0V, T_A = 25°C All Other Pins GND			1.0	μA
Data and RE Input Capacitance	V_{IN} = V_{SS}, f = 1.0 MHz, All Other Pins GND (Note 1)		4.0	6.0	pF
Clock Input Capacitance	V_ϕ = V_{SS}, f = 1.0 MHz, All Other Pins GND (Note 1)		16	25	pF
Data, RE, and Clock Input Current					
Logical "1"	V_{IN} = V_{SS}			10	μA
Logical "0"	V_{IN} = V_{SS} − 5.0V	0.6	1.1	1.6	mA
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.1 mA	V_{SS} − 1.0		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current	T_A = 25°C, V_{GG} = −12.6V, ϕ_{PW} = 180 ns V_{SS} = +5.0V, DATA = 0-1-0-1, V_{DD} = 0V				
I_{GG}	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		7.5	11	mA
	ϕ_f = 1.0 MHz		9.5	12	mA
	ϕ_f = 2.5 MHz		12	15	mA
I_{DD}	0.01 MHz ≤ ϕ_f = 0.01 MHz		24	35	mA
	ϕ_f = 1.0 MHz		24	35	mA
	ϕ_f = 2.5 MHz		24	35	mA
Clock Frequency (ϕ_f)	ϕt_r = ϕt_f = 10 ns	0.01		2.5	MHz
Clock Pulsewidth (ϕ_{PW}, $\overline{\phi_{PW}}$)	ϕt_r = ϕt_f = 10 ns	0.180		100	μs
Clock Transition Times (ϕt_r, ϕt_f)				5.0	μs
Data Input Setup Time (t_{ds})		150			ns
Data Input Hold Time (t_{dh})		0			ns
RE Control Setup (t_{rs})		150			ns
RE Control Hold (t_{rh})		0			ns
Data Output Propagation Delay From ϕ	15 pF Output Capacitance				
Delay to High Level (t_{pdH})			100	200	ns
Delay to Low Level (t_{pdL})			100	200	ns

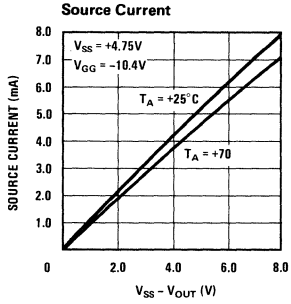
Note 1: Capacitance is guaranteed by periodic testing.
Note 2: Pull-up resistors to 5.0V are provided internally.

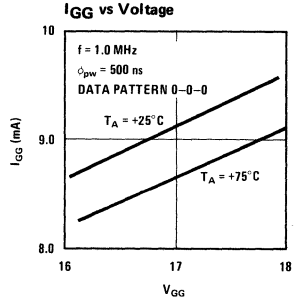
typical performance characteristics



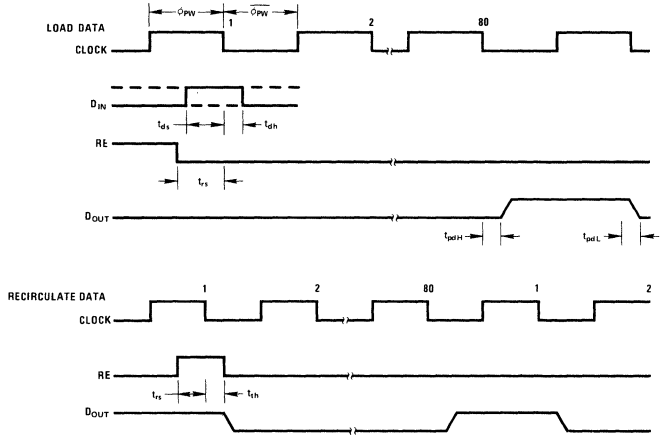








switching time waveforms



Note: All timing relationships are referenced to the 50% point, except for clock rise and fall times which are measured to the 10% and 90% point.

truth table

Positive Logic

logic "1" = V_{IH} = Logical High Level (V_{SS})
logic "0" = V_{IL} = Logical Low Level (V_{DD})

Load/Recirculate	Function
1	Recirculate
0	Load Data

Dynamic Shift Registers

MM4025/MM5025 dual 1024-bit dynamic shift register
MM4026/MM5026 dual 1024-bit dynamic shift register
MM4027/MM5027 2048-bit dynamic shift register

general description

These 2048-bit dynamic shift registers are MOS monolithic integrated circuits using P-channel silicon gate technology. They employ a push-pull output for bipolar compatability and on-chip multiplexing to achieve a 6 MHz data rate. The clock rate is one-half the data rate, i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

The MM4025/MM5025 and MM4027/MM5027 have on-chip logic to load and recirculate data.

The MM4026/MM5026 has an individual logic-select line to load one of the two inputs on each of the 1024-bit registers.

features

- Bipolar compatibility — Standard +5V, −12V power supplies
- High frequency of operation — 6 MHz guaranteed
- Low power dissipation — 120 μW/bit at 1 MHz ϕ rate 0°C, guaranteed
- Low clock capacitance — 190 pF max
- Wide operating temperature range
  MM4025,MM4026,MM4027 −55°C to +125°C
  MM5025,MM5026,MM5027 0°C to 70°C

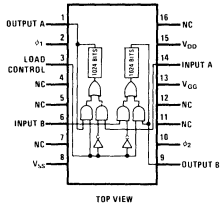
applications

- "Silicon store" replacement for drum and disc memories
- CRT displays
- Buffer memories

logic and connection diagrams

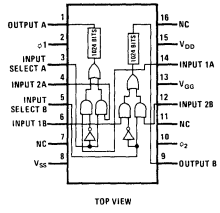
Military Temperature Range

Dual-In-Line Package



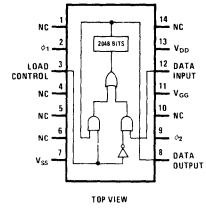
Order Number MM4025D or MM5025D
See Package 3

Dual-In-Line Package



Order Number MM4026D or MM5026D
See Package 3

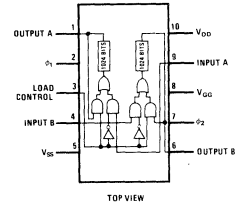
Flat Package



Order Number MM4027F or MM5027F
See Package 26

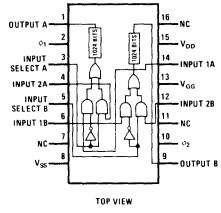
Commercial Temperature Range

Dual-In-Line Package



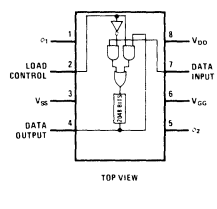
Order Number MM5025N
See Package 13

Dual-In-Line Package



Order Number MM5026N
See Package 15

Dual-In-Line Package



Order Number MM5027N
See Package 12

absolute maximum ratings

Voltage at Any Pin With Respect to V_{SS}	+0.3 to −20.0V
Operating Ambient Temperature Range	
MM4025,MM4026,MM4027	−55°C to +125°C
MM5025,MM5026,MM5027	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics V_{SS} = +5.0V ± 5%, V_{DD} = GND, V_{GG} = −12.0V ±10%

T_A within operating temperature range unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.7		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −10V, T_A = 25°C, All other pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0V, f = 1 MHz, All other pins GND (Note 1)		2.5	5.0	pF
Load/Select Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.7		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Load/Select Input Leakage	V_{IN} = −10V, T_A = 25°C, All other pins GND		0.01	0.5	μA
Load/Select Input Capacitance	V_{IN} = 0V, f = 1 MHz, All other pins GND (Note 1)		4.0	7.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.0		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −15V, T_A = 25°C, All other pins GND		.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0V, f = 1 MHz, All other pins GND (Note 1)		165	190	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA	0.0		0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12.0V, ϕ_{PW} = 115 ns V_{SS} = 5.0V, $V_{\phi L}$ = −12.0V, DATA = Note 4 V_{DD} = 0.0V				
	0.01 MHz $\phi_f \leq$ 0.1 MHz		2	3.5	mA
	ϕ_f = 1.0 MHz		2	3.5	mA
	ϕ_f = 3.0 MHz		2	3.5	mA
I_{DD}	0.01 MHz $\phi_f \leq$ 0.1 MHz		8	15	mA
	ϕ_f = 1.0 MHz		22	32	mA
	ϕ_f = 3.0 MHz		48	70	mA
Clock Frequency (ϕ_f)					
MM4025,MM4026,MM4027	$\phi t_r = \phi t_f$ = 20 ns (Note 2, Note 3 & Note 5)	0.06	2.0	1.0	MHz
MM5025,MM5026,MM5027		0.01	4.0	3.0	MHz
Clock Pulsewidth (ϕ_{PW})					
MM4025,MM4026,MM4027	$\phi t_r = \phi t_f$ = 20 ns, Data Rate = 2 ϕ_f	0.115		8.0	μs
MM5025,MM5026,MM5027		0.115		10	μs
Clock Phase Delay Times (ϕ_d,$\bar{\phi}_d$)	See Curves	10			ns
Clock Transition Times (ϕt_r, ϕt_f)				0.5	μs
Partial Bit Times (T)	(Note 2, Note 3)				
T_1 Partial Bit Time					
MM4025,MM4026,MM4027		0.165		16.5	μs
MM5025,MM5026,MM5027		0.165		100	μs
T_2 Partial Bit Time					
MM4025,MM4026,MM4027		0.165		16.5	μs
MM5025,MM5026,MM5027		0.165		100	
Data & Load/Select Input Setup Time (t_{ds})				35	ns
Data & Load/Select Input Hold Time (t_{dh})				20	ns
Data Output Propogation Delay from ϕ					
Delay to High Level (t_{pdH})	15 pF Output Capacitance			80	ns
Delay to Low Level (t_{pdL})				80	ns

Note 1: Capacitance is guaranteed by periodic testing.

Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_1 and T_2) as shown by ϕ_f versus temperature and T_1, T_2 versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_1 equal to T_2. The minimum guaranteed clock frequency: ϕ_f (min) = 1/(T_1 + T_2) where T_1 and T_2 do not exceed the guaranteed maximum.

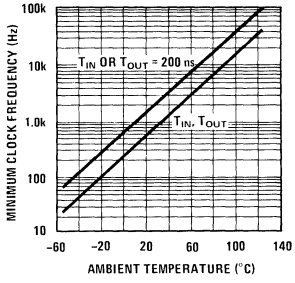
Note 3: Minimum clock frequency and partial bit time curves are guaranteed by testing at a high temperature point.

Note 4: For data pattern of 1111000011110000 etc.

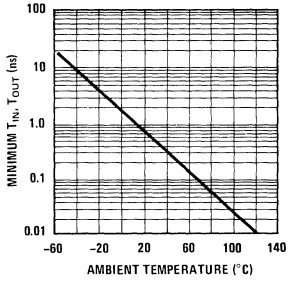
Note 5: Maximum frequency limited by maximum package power dissipation for MM4025, MM4026 and MM4027.

guaranteed performance characteristics

Guaranteed Minimum Clock Frequency vs Temperature (Note 2)

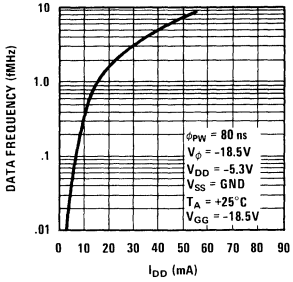


Guaranteed Maximum T_1 and T_2 vs Temperature (Note 2)

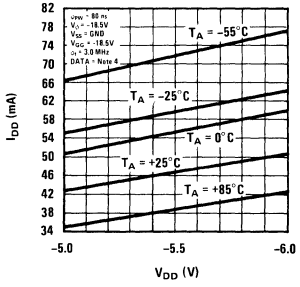


typical performance characteristics

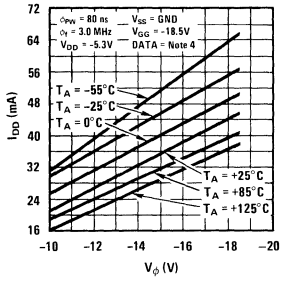
Power Supply Current vs Data Rate



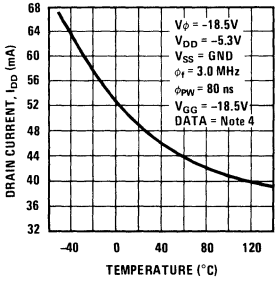
Power Supply Current vs V_{DD}



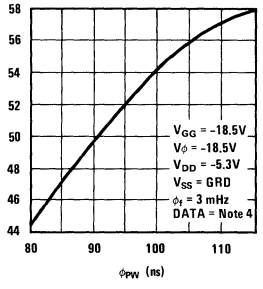
Power Supply Current vs Clock Voltage V_ϕ



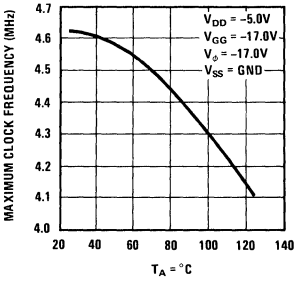
Power Supply Current vs Temperature



Power Supply Current vs Clock Pulse Width ϕ_{PW}

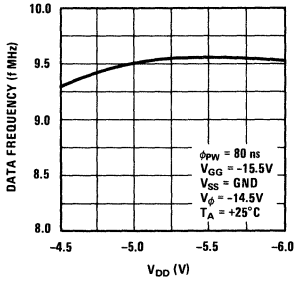


Maximum Clock Frequency vs Temperature

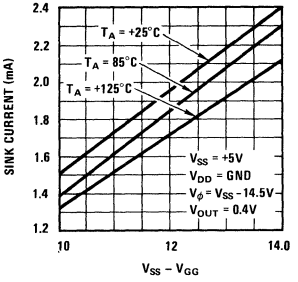


typical performance characteristics (con't)

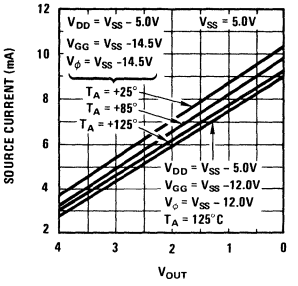
Maximum Data Rate vs V_{DD}



Typical Sink Current vs V_{GG}

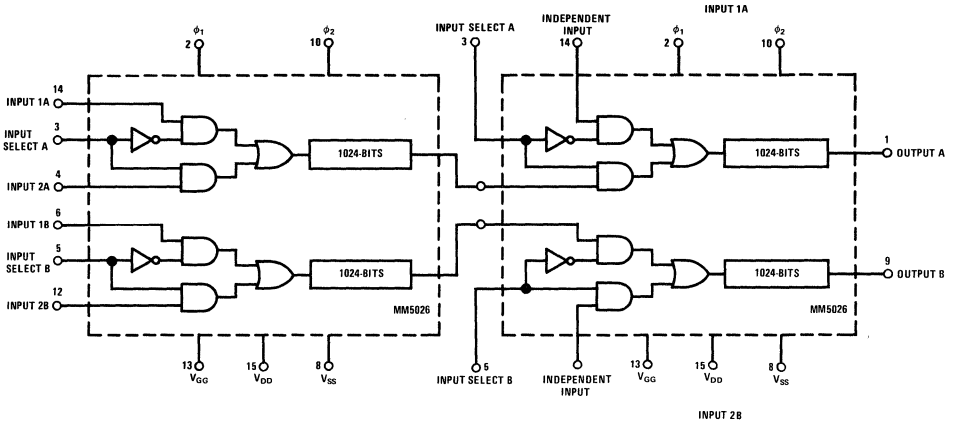


Typical Data Output Source Current vs Data Output Voltage

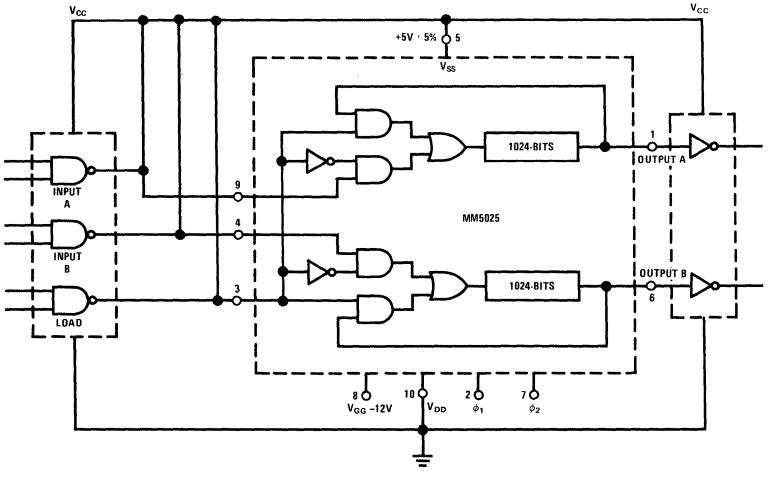


typical applications

Memory Expansion



TTL/MOS Interface



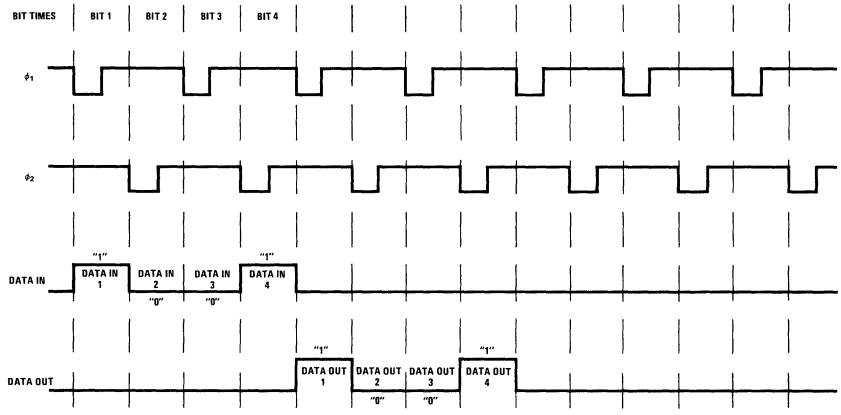
truth tables

Positive Logic
Logic "1" = V_{IH} = Logical High Level Logic "0" = V_{IL} = Logical Low Level

Write/Recirculate	Function
1	Recirculate
0	Load Data

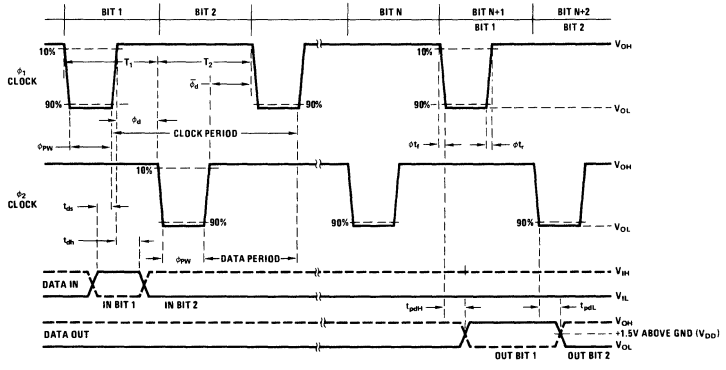
Input Select A	Function
1	Select Input 2A
0	Select Input 1A
Input Select B	**Function**
1	Select Input 2B
0	Select Input 1B

switching time waveforms



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ_1 time, it exits at ϕ_1 time, (beginning on $\phi_{1's}$ negative going edge and ending on the succeeding $\phi_{2's}$ negative going edge).

timing diagram



Dynamic Shift Registers

MM4104/MM5104 dynamic shift register

general description

The MM4104/MM5104 360/359, 228/287, 40/32 bit dynamic shift register is a monolithic MOS integrated circuit utilizing p-channel enhancement mode low threshold technology to achieve bipolar compatibility. The register lengths are lengthened or shortened by hard wiring the length select line to V_{GG} or V_{SS}. The lengths available are: 40, 288, 328, 360, 400, 560, 688; or 32, 287, 319, 359, 391, 446, 678.

features

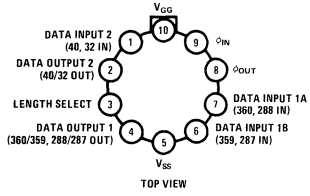
- DTL/TTL compatibility — +5V, −12V power supply. No pull-up or pull-down resistors required
- Multiple length registers — Electrically adjustable 360/359, 288/287, 40/32 bit registers
- Wide frequency range — 250 Hz min. guar. at 25°C; 2.5 MHz max. guar. over temp.

applications

- Data store
- CRT displays
- Business machine

connection diagram

Metal Can Package

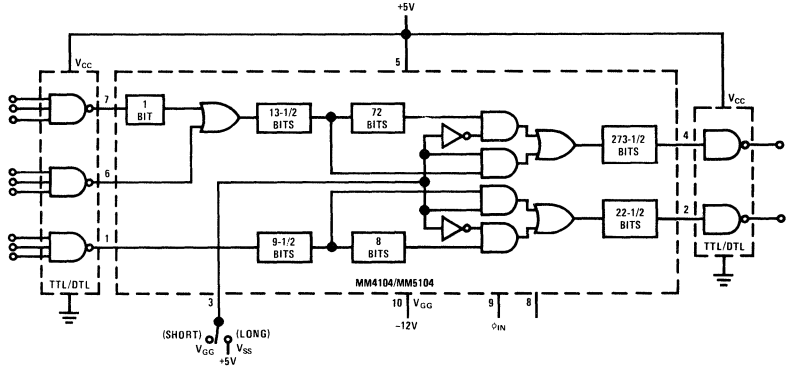


TOP VIEW

Order Number MM4104H or MM5104H
See Package 24

typical applications

TTL/MOS Interface



Note: V_{GG} on pin 3 results in a 288-bit register between pin 7 and pin 4 and a 287-bit register between pins 6 and 4. The unused input (6 or 7) must be returned to V_{SS}. Also, there is a 32-bit register between pins 1 and 2.

V_{SS} on pin 3 results in a 360 bit register between pin 7 and pin 4 and a 359-bit register between pins 6 and 4. The unused input (6 or 7) must be returned to V_{SS}. Also, there is a 40-bit register between pins 1 and 2.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range MM4104	−55°C to 125°C
MM5104	−25°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

(T_A within operating temperature range, V_{SS} = +5.0V, ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} −4.2	V
Data Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		3.0	5.0	pF
Length Select Input Levels					
Logical HIGH Level (V_{LSH})		V_{SS}		V_{SS} + 0.3	V
Logical LOW Level (V_{LSL})		V_{SS} − 18.5		V_{GG}	V
Length Select Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Length Select Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		6.0	9.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} −18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		85	100	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.5	2.5	mA
	ϕ_f = 1 MHz		3.5	5.0	mA
	ϕ_f = 2.5 MHz		7.0	10.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\,\mu s$	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	(Note 1)	10			ns
Clock Transition Time (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\,\mu s$			1	μs
Partial Bit Times (T)	(Note 1)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit.				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

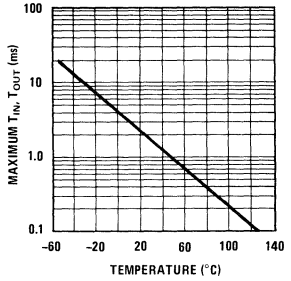
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

Note 2: The curves are guaranteed by testing at a high temperature point.

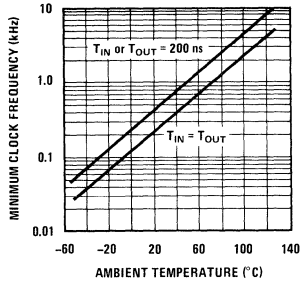
Note 3: Capacitance is guaranteed by periodic testing.

performance characteristics

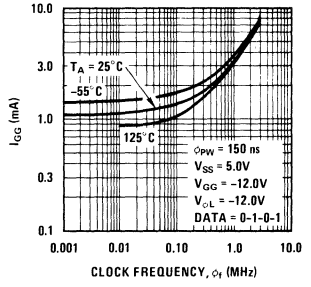
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Notes 1, 2)



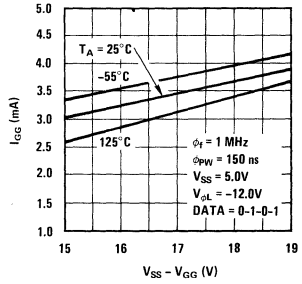
Guaranteed Minimum Clock Frequency vs Temperature (Notes 1, 2)



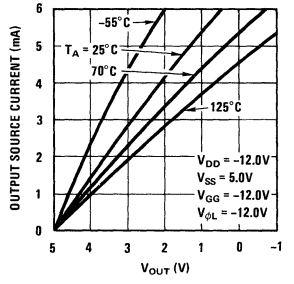
Typical Power Supply Current vs Clock Frequency



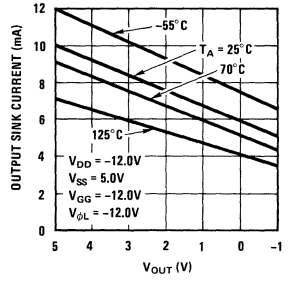
Typical Power Supply Current vs V_{GG}



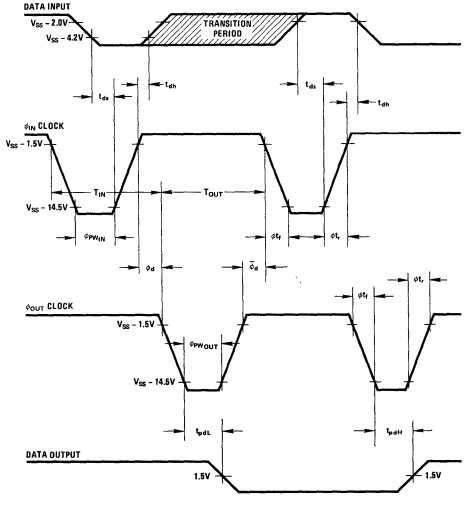
Typical Output Source Current vs Voltage



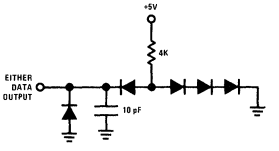
Typical Output Sink Current vs Voltage



switching time waveforms



ac test circuit



Static Shift Registers

*MM404/MM504 dual 16 bit static register
*MM405/MM505 dual 32 bit static register

general description

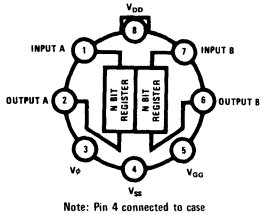
The National Semiconductor line of MOS static shift registers are monolithic integrated circuits utilizing P-channel enhancement mode transistors. The use of a low threshold technology permits operation with a V_{DD} supply voltage of −10 volts and a V_{GG} supply and clock amplitude voltage of less than −16 volts. These registers require only a single clock input to operate from DC to 1 MHz in either synchronous or asynchronous systems. Each register cell is designed specifically to avoid race conditions during latching, thus insuring operation under all conditions specified in the electrical characteristics.

Additional features include:

- Bipolar compatibility
- Single phase clock input
- High frequency operation 1.0 MHz
- Low power consumption 1.7 mW/bit typ
- Output impedance (V_{OH}) 500Ω typ
- Military and commercial temperature ranges
  - MM404, MM405 −55°C to +125°C
  - MM504, MM505 0°C to +70°C

connection diagram

Metal Can Package



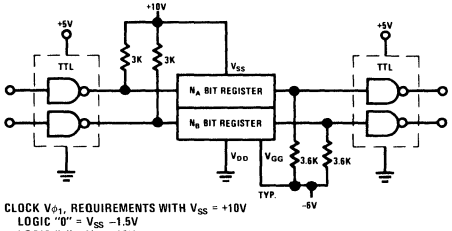
Note: Pin 4 connected to case

TOP VIEW

Order Number MM404H, MM504H, MM405H or MM505H
See Package 23

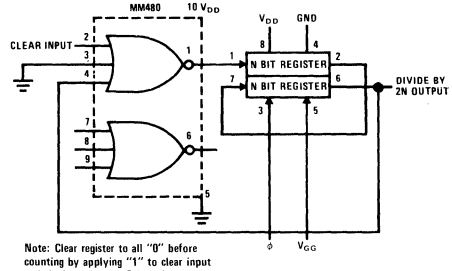
typical applications

TTL/MOS Interface



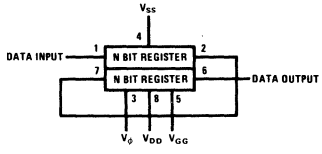
CLOCK V_{ϕ_1}, REQUIREMENTS WITH V_{SS} = +10V
LOGIC "0" = V_{SS} −1.5V
LOGIC "1" = V_{SS} −16V

2N Bit Johnson Counter

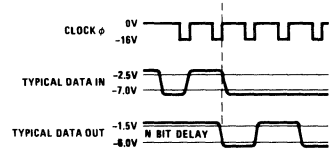


Note: Clear register to all "0" before counting by applying "1" to clear input and clocking through 2N clock cycles.

Single 2N Bit Register



Waveforms for Applications



*For New Designs, see MM4040/MM5040, MM4050A/MM5050A.

absolute maximum ratings

Drain Voltage (V_{DD})		+0.5V to −25V
Gate Voltage (V_{GG})		+0.5V to −25V
Clock Input ($V_{\phi 1}$)		+0.5V to −25V
Data Inputs		+0.5V to −25V
Power Dissipation (Note 1)		300 mW
Operating Temperature	MM404, MM405	−55°C to +125°C
	MM504, MM505	0°C to +70°C
Storage Temperature		−65°C to +150°C

electrical drive requirements (Note 1)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Clock pulse Width					
ϕ_1 Clock, ϕ_{1pw}		0.4		10	μs
Clock Pulse Risetime, $t_{r\phi}$	1 MHz with ϕ_{pw} = 0.4 μs			0.05	μs
Falltime, $t_{f\phi}$	100 kHz with ϕ_{pw} = 2 μs			0.6	μs
	10 kHz with ϕ_{pw} = 10 μs			2.0	μs
Clock Input Level					
Logic "$V_{\phi H}$"			V_{SS} −0.5	V_{SS} −1.5	V
Logic "$V_{\phi L}$"		V_{SS} −14.5	V_{SS} −16.0	V_{SS} −18.0	V
Data Input Voltage Levels					
Logic "V_{IH}"				V_{SS} −2.5	V
Logic "V_{IL}"		V_{SS} −7.0			V
Data Setup Time, t_{ds}		0.2			μs
Data Hold Time, t_{dh}		0.03			μs

electrical characteristics (Note 2)

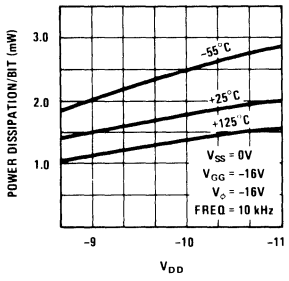
PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Clock Repetition Rate	Fan-Out "1"		dc		1.0	MHz
Data Output Voltage Levels						
Logic "V_{OH}"					V_{SS} −1.5	V
Logic "V_{OL}"			V_{SS} −8.0			V
Data Input Capacitance (Each Input)	f = 1 MHz V_{IN} = 0V			1.5	3.0	pF
Clock Line Capacitance	f = 1 MHz, −20V Bias	MM404, MM504		9.5	15	pF
		MM405, MM505		18	30	pF
	0V Bias	MM404, MM504		15.0	20	pF
		MM405, MM505		25	40	pF
Output Impedance	Outputs at Logic "0"			0.5	1.0	kΩ
Input Leakage Current	T_A = 25°C					
Pin 1	V_{IN} = −18V All Other Pins at GND				0.5	μA
Power Supply Current Drain (V_{DD})	Outputs at Logic "0" 1 MHz Operation T_A = 25°C					
	MM404, MM504			5.5	10.0	mA
	MM405, MM505			10.0	15.0	mA

Note 1: For operating at elevated temperatures, the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +150°C/W junction to ambient. The full rating applies for case temperatures to +125°C.

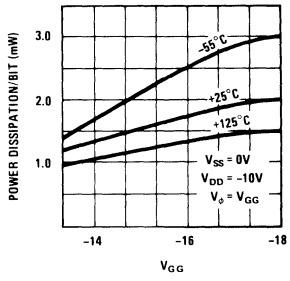
Note 2: These specifications apply over the specified temperature ranges for $-11V < V_{DD} < -9.5V$, and $-18V < V_{GG} < -14.5V$ and clock repetition rate of 10 kHz with output measurement load of less than 10 pF in parallel with 10 MΩ to ground unless otherwise specified.

performance characteristics

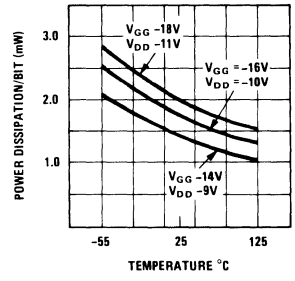
Power Dissipation vs V_{DD}



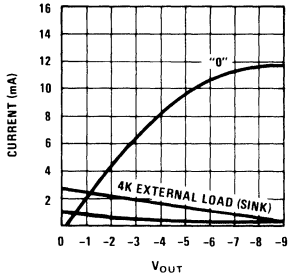
Power Dissipation vs V_{GG}



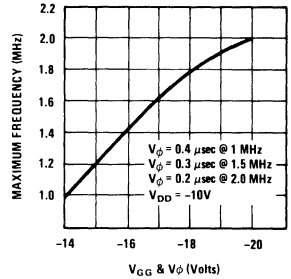
Power Dissipation vs Temp.



V_{OUT} vs Load Current



Max. Frequency vs Supply Voltages



operation

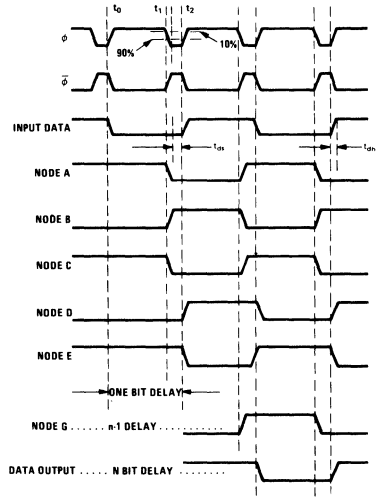
A diagram of a one-bit static register employing two clock phases (ϕ, $\overline{\phi}$) is shown in the schematic. The register requires only one external clock phase (ϕ) since the second clock ($\overline{\phi}$) is generated internally by T_{19} and 15K; this configuration simplifies the input drive requirements.

The basic cell functions as follows. Each bit of delay consists of three inverters T_2, T_4, and T_8 in conjunction with three MOS load resistors T_3, T_5, and T_9 followed by three coupling devices T_1, T_6, and T_7. The timing diagram shows the sequence of operation. Assume the input is at a logic "1" level during t_1 time. When the clock (ϕ) goes to a logic "1" level, two operations take place simultaneously. First, transistor T_1 turns "ON", transferring the input data (logic "1" level) to the gate to source capacitance (C_1) of T_2. The voltage stored on C_1 is sufficient to turn T_2 "ON" discharging node B. With the gate to source capacitance (C_2) of T_4 discharged, T_4 turns "OFF" placing a logic "1" level at node C. Concurrently ϕ turns T_{19} "ON" generating the complement of ϕ, that is $\overline{\phi}$ and in turn $\overline{\phi}$ is used to turn T_6 and T_7 "OFF". This action allows the register's previous information to be temporarily stored on the gate to source capacitance C_3 of T_8. The output at node E during this timing sequence remains unchanged. However, during t_2 time, clock ϕ returns to ground; concurrently $\overline{\phi}$ goes to a logic "1" level turning T_1 "OFF" allowing T_6 and T_7 to turn "ON". The information which was previously stored on the gate of T_8 discharges to a logic "0" level causing the output at node E to switch to a logic "1" level thereby obtaining the required one-bit of delay.

Likewise the information at node C is fed back to node A latching T_2 in the "ON" state.

When a logic "0" level is presented at the register input, the sequence is once again repeated. The bit delay demonstrated in this example is repeated for each half of the dual static register.

timing diagram



Static Shift Registers

MM4040/MM5040 dual 16-bit static shift register

general description

The MM4040/MM5040 dual 16-bit static shift register is a monolithic integrated circuit utilizing P channel enhancement mode low threshold technology to achieve direct bipolar compatibility on the inputs and outputs. The device requires only a single phase clock.

features

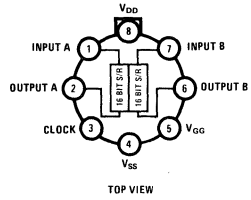
- Bipolar compatibility — +5, −12V operation; No pull-up or pull-down resistors needed
- High frequency operation — 2.2 MHz guaranteed
- Single phase clock

applications

- Static data buffer
- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

connection diagram

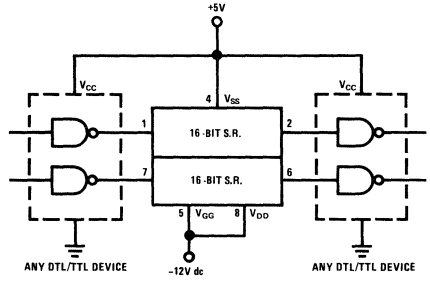
Metal Can Package



TOP VIEW

Order Number MM4040H or MM5040H
See Package 23

typical application



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22
Operating Temperature Range MM4040	−55°C to +125°C
MM5040	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

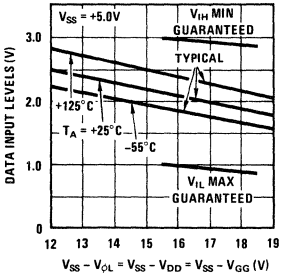
T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{SS} - V_{DD}$ = 9V to 18.5V, V_{GG} = −12V ±10%, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND			0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		2.5	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND			1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		19	22	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4			V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current	T_A = +25°C, V_{GG} = −12V, ϕ_{PW} = 200 ns, V_{SS} = 5V, V_{DD} = −12V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
I_{GG}	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.0	2.0	mA
	ϕ_f = 1.0 MHz		1.8	3.0	mA
	ϕ_f = 2.0 MHz		3.0	4.0	mA
I_{DD}	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		5.0	9.0	mA
	ϕ_f = 1.0 MHz		5.1	9.0	mA
	ϕ_f = 2.0 MHz		5.2	9.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns	DC	3.0	2.2	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_r + \phi t_f + \phi_{PW} \leq$ 10.5 ns	.200	.100	10.0	μs
Clock Transition Times ($\phi t_r + \phi t_f$)	$\phi t_r + \phi t_f + \phi_{PW} \leq$ 10.5 ns			1.0	μs
Data Input Setup Time (t_{ds})		120	60		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ	See test circuit				
Delay to High Level (t_{pdH})			200	300	ns
Delay to Low Level (t_{pdL})			200	300	ns

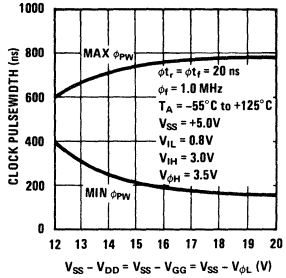
Note 1: Capacitance values are guaranteed by statistical lot sample testing.

guaranteed performance characteristics

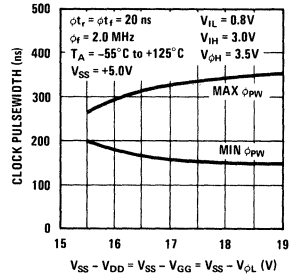
Data Input Levels vs Supply Voltage



1.0 MHz Operating Curve

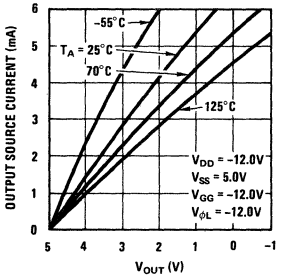


2.0 MHz Operating Curve

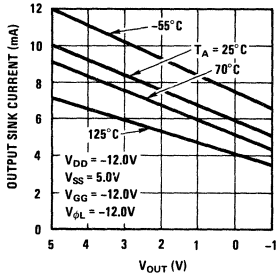


typical performance characteristics

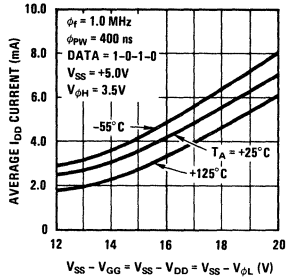
Data Output Source Current vs Voltage



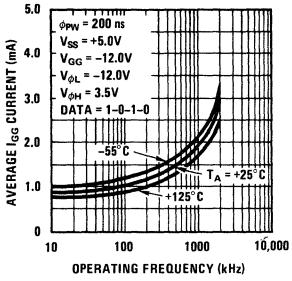
Data Output Sink Current vs Voltage



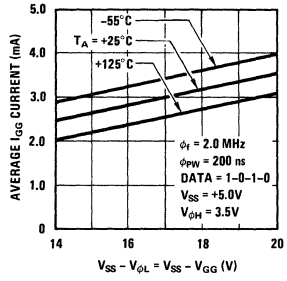
Power Supply Current vs Voltage



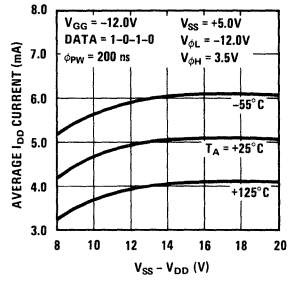
Power Supply Current vs Operating Frequency



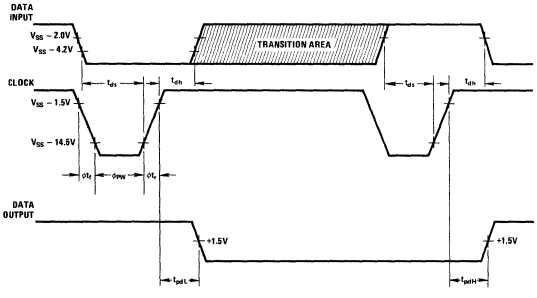
Power Supply Current



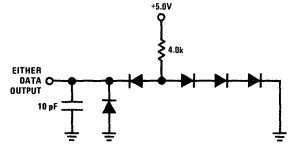
Power Supply Current



switching time waveforms



test circuit



Static Shift Registers

MM4050A/MM5050A dual 32-bit static shift register
MM4051A/MM5051A dual 32-bit static shift register–split clock

general description

The MM4050A/MM5050A and MM4051A/MM5051A dual 32-bit static shift registers are monolithic MOS integrated circuits utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. Operation to 2.2 MHz is achieved with a single phase clock. The MM4051A/MM5051A is a bonding option of the MM4050A/MM5050A to provide independent clock control of each register.

features

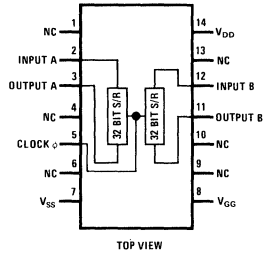
- Bipolar compatibility — +5V, −12V operation; No pull-up or pull-down resistors needed
- High frequency operation — dc to 2.2 MHz
- Single phase clock
- Improved drive capability — Push-pull outputs
- Military and commercial temperature ranges
  - MM4050A, MM4051A — −55°C to +125°C
  - MM5050A, MM5051A — 0°C to +70°C

applications

- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

logic and connection diagrams

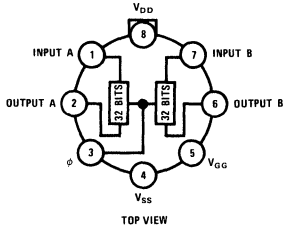
Dual-In-Line Package



TOP VIEW

Order Number MM4050AD or MM5050AD
See Package 2

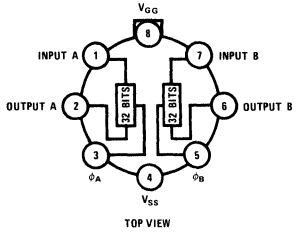
Metal Can Package



TOP VIEW

Order Number MM4050AH or MM5050AH
See Package 23

Metal Can Package

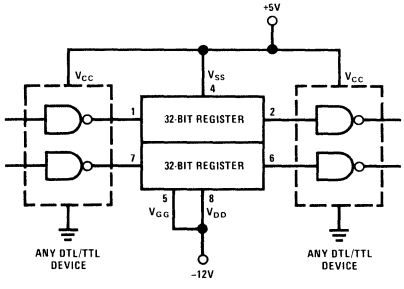


TOP VIEW

Order Number MM4051AH or MM5051AH
See Package 23

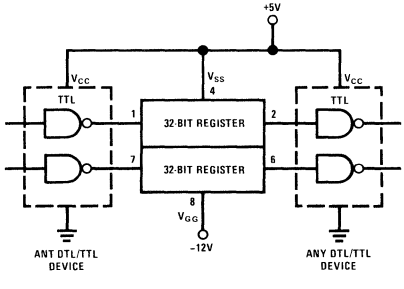
typical applications

TTL/MOS Interface



MM4050A/MM5050A

TTL/MOS Interface



MM4051A/MM5051A

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range MM4050A/MM4051A	−55°C to +125°C
MM5050A/MM5051A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

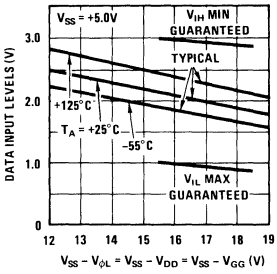
T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{SS} − V_{DD} = 9V to 18.5V, V_{GG} = −12V ±10%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND			0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		2.5	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} −14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND			1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		25	35	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4			V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = +25°C, V_{GG} = −12.0V, ϕ_{PW} = 200 ns V_{SS} = +5.0V, $V_{\phi L}$ = −12.0V, Data = 0-1-0-1 V_{DD} = −12.0V				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.6	3.5	mA
	ϕ_f = 1.0 MHz		3.8	8	mA
	ϕ_f = 2.0 MHz		4.6	11.0	mA
I_{DD}	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.7	5.0	mA
	ϕ_f ≤ 1.0 MHz		2.9	5.0	mA
	ϕ_f ≤ 2.0 MHz		3.1	5.0	mA
Clock Frequency (ϕ_f)	ϕt_r = ϕt_f = 20 ns	DC	3.0	2.2	MHz
Clock Pulsewidth (ϕ_{PW})	ϕt_r + ϕt_f + ϕ_{PW} ≤ 10.5 μs	0.2	0.100	10.0	μs
Clock Transition Times (ϕt_r, ϕt_f)	ϕt_r + ϕt_f + ϕ_{PW} ≤ 10.5 μs			1.0	μs
Data Input Setup Time (t_{ds})		80	50		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay From ϕ					
Delay to HIGH Level (t_{pdH})	See ac test circuit		150	300	ns
Delay to LOW Level (t_{pdL})			150	300	ns

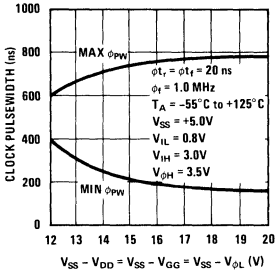
Note 1: Capacitance values are guaranteed by periodic testing.

guaranteed performance characteristics

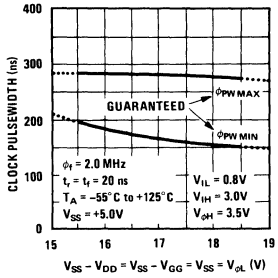
Data Input Voltage vs Supply



1.0 MHz Operating Curve

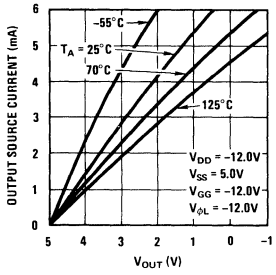


2.0 MHz Operating Curve

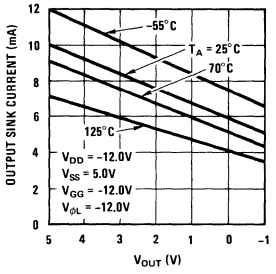


typical performance characteristics

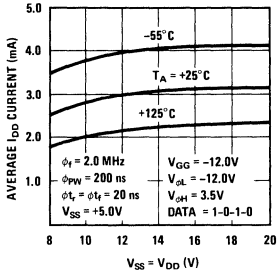
Data Output Source Current vs Voltage



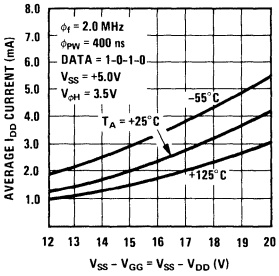
Output Sink Current vs Voltage



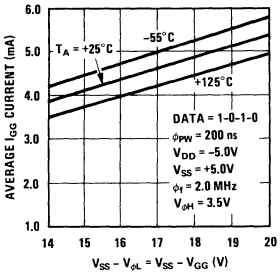
Power Supply Current



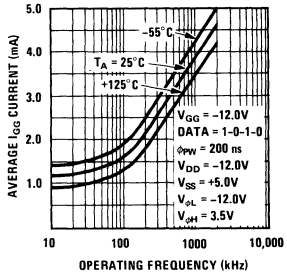
Power Supply Current vs Voltage



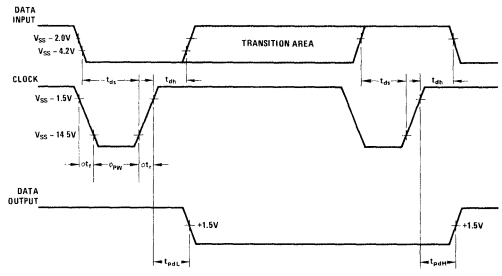
Power Supply Current



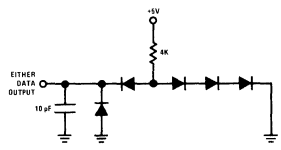
Power Supply Current vs Operating Frequency



switching time waveforms



ac test circuit



Static Shift Registers

MM4052/MM5052 dual 80 bit static shift register
MM4053/MM5053 dual 100-bit static shift register

general description

The MM4052/MM5052 dual 80-bit and MM4053/MM5053 dual 100-bit static shift registers are monolithic integrated circuits utilizing P channel enhancement mode low threshold technology to achieve direct bipolar compatibility on the inputs and outputs. The devices require only a single phase clock.

features

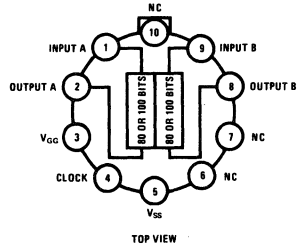
- Bipolar compatibility — +5, −12V operation; No pull-up or pull-down resistors needed
- High frequency operation — 1.6 MHz guarantee
- Single phase clock
- Improved drive capability — push-pull outputs

applications

- Static data buffer
- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

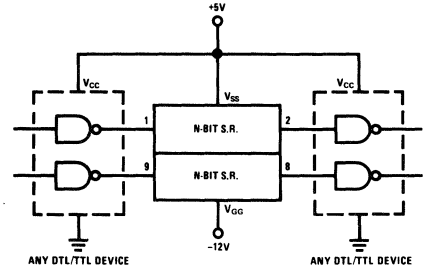
connection diagram

Metal Can Package



Order Number MM4052H, MM5052H, MM4053H or MM5053H
See Package 24

typical application



absolute maximum ratings

Voltage @ Any Pin	V_{SS} +0.3V to V_{SS} −22V
Operating Temperature Range	
MM4052/MM4053	−55°C to +85°C (Ambient)
	−55°C to +125°C (Case)
MM5052/MM5053	0°C to +70°C (Ambient)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

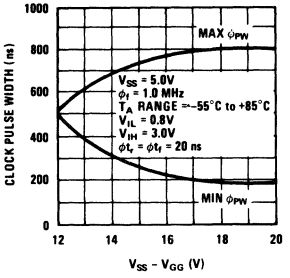
electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5% and V_{GG} = −12V ±10%, unless otherwise specified.

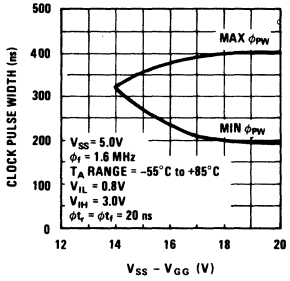
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 2.0			V
Logical Low Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C All other pins GND		.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1.0 MHz All other pins GND		3.0	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS}	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_{IN} = −20V, T_A = 25°C All other pins GND			1.0	μA
Clock Input Capacitance	V_{IN} = 0.0V, f = 1.0 MHz All other pins GND		22	28	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −500 μA	2.4V	4.8	V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA		−3.0	0.4	V
Logical High Level (V_{OH})	I_{SOURCE} = −10 μA	V_{SS} − 1.0	V_{SS}	V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 10 μA		V_{SS} − 12.0	V_{SS} − 7.0	V
Power Supply Current	T_A = 25°C ϕ_f = 1.6 MHz				
(I_{GG}) MM4052/MM5052	V_{GG} = V_{SS} − 17V $V_{\phi L}$ = V_{SS} − 17V		9.5	12.5	mA
(I_{GG}) MM4053/MM5053			12.0	16.0	mA
Propagation Delays from Clock					
Propagation Delay to a High (t_{pdH})	See waveform		200	300	ns
Propagation Delay to a Low (t_{pdL})	See waveform		200	300	ns
Clock Frequency (ϕ_f)	See operating curves	0		1.6	MHz
Clock Pulse Width (ϕ_{PW})	See operating curves $\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.25		10	μs
Clock Transition Times					
Risetime (ϕt_r)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			5	μs
Falltime (ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			5	μs
Data Input Setup Time (t_{ds})		80	50		ns
Data Input Hold Time (t_{dh})		20	0		ns

guaranteed performance characteristics

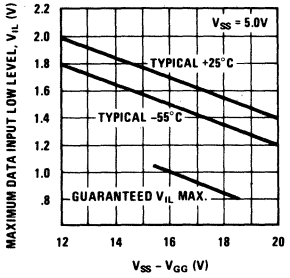
1.0 MHz Operating Curve



1.6 MHz Operating Curve

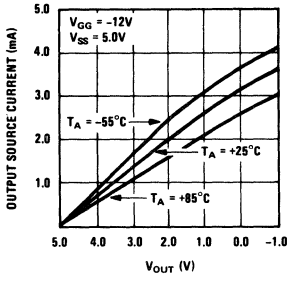


Maximum Data Input Low Level vs Supply Voltage

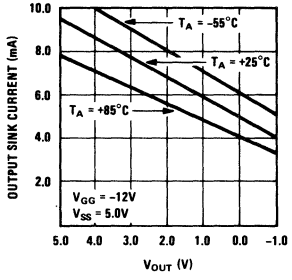


typical performance characteristics

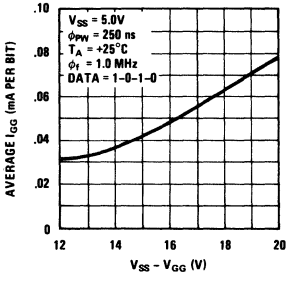
Data Output Source Current vs Data Output Voltage



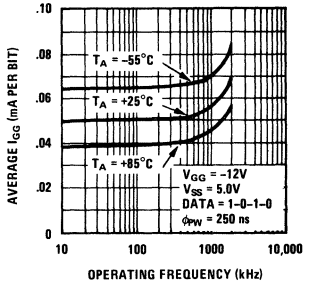
Data Output Sink Current vs Data Output Voltage



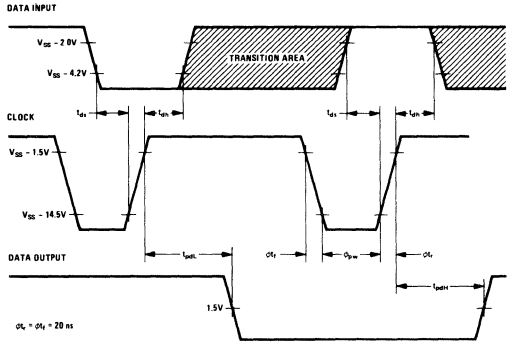
Power Supply Current



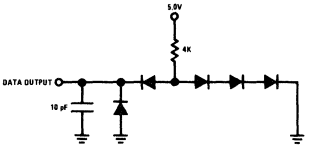
Power Supply Current



switching time waveforms



ac test circuit



Static Shift Registers

MM5054 dual 64/72/80-bit static shift register

general description

The MM5054 dual 80-bit static shift register is a monolithic MOS integrated circuit utilizing silicon gate low threshold technology to achieve complete bipolar compatibility. The device has input and output taps that also provide register lengths of 64 or 72 bits.

The single phase bipolar compatible clock lines may be driven by any conventional DTL or TTL circuit. The registers may be operated as a dual register by connecting the clock lines A and B together, or as two independent registers. Two clock control lines provide independent logical control of the shift register clock lines.

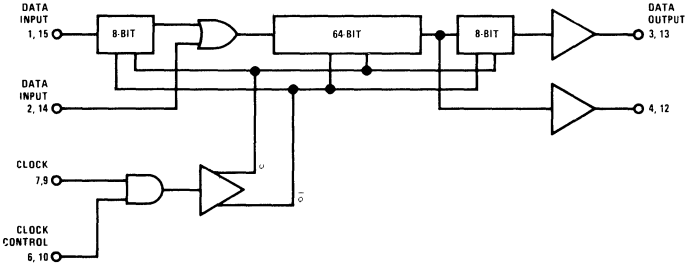
features

- Complete bipolar compatibility — DTL/TTL input/output and clock line compatibility without additional components
- Standard supplies — +5.0V, −12V
- High freq. operation — DC to 3.0 MHz typ
- Single phase clock — DTL/TTL compatible on-chip clock driver
- Low clock line capacitance — 8.0 pF max
- System flexibility — Split clock or common clock operation. Logical control of clock lines
- Low power dissipation — <600 μW/bit typ

applications

- Teletype data buffers
- Printer memory – 80, 128, 136, 144 bit lengths
- Telemetry and data sampling systems
- Serial memory storage

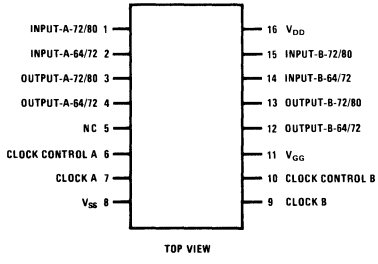
logic diagram



The unused data inputs and clock controls should be connected to V_{SS} to ensure proper operation.
Logic diagram shows 1/2 of the unit.

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5054D
See Package 3
Order Number MM5054N
See Package 15

truth table

Positive Logic

CLOCK CONTROL	CLOCK
Low	Inhibited
High	Active

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 20V
Operating Ambient Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	600 mW @ 25°C

dc electrical characteristics

T_A within operating range, V_{GG} = −12V ±10%, V_{DD} = GND, V_{SS} = 5.0V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Clock Control, and Clock Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})				V_{SS} − 4.2	V
Input Leakages	V_{IN} = −10V, T_A = 25°C All Other Pins GND			0.5	μA
Data Input Capacitance	V_{IN} = 0V, f = 1.0 MHz All Other Pins GND (Note 1)		4.5	6.0	pF
Clock and Clock Control Capacitance	V_{IN} = 0V, f = 1.0 MHz (Note 1)		6.0	8.0	pF
Data Output Levels	(Figure 1)				
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA		0.15	0.4	V
Power Supply Current	ϕ_f = 1.5 MHz, T_A = 25°C				
(I_{GG} + I_{DD} = I_{SS}) I_{GG}	V_{SS} = 5.0V, V_{DD} = GND		7.0	10	mA
I_{DD}	V_{GG} = −12V		5.0	8.0	mA

ac electrical characteristics

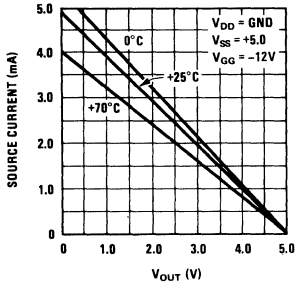
T_A within operating range, V_{GG} = −12V ±10%, V_{DD} = GND, V_{SS} = 5.0V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency (ϕ_f)	ϕt_r, $\phi t_f \leq$ 10 ns (Note 2)	DC	3.0	1.5	MHz
Clock Pulsewidth (ϕ_{PW})					
ϕ_{PW}	$\phi t_r = \phi t_f \leq$ 10 ns	0.25	0.180	10	μs
$\overline{\phi_{PW}}$	$\phi t_r = \phi t_f \leq$ 10 ns	0.38			μs
Clock Transition Times					
Clock Risetime (ϕt_r)				500	ns
Clock Falltime (ϕt_f)				500	ns
Clock Control Setup Time (t_{CS})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	0			ns
Clock Control Hold Time (t_{ch})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	0			ns
Data Input Setup Time (t_{ds})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	60	30		ns
Data Input Hold Time (t_{dh})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	40	20		ns
Data Output Propagation Delay	(Figures 1 and 2)				
From Clock	$\phi t_r = \phi t_f$ = 10 ns				
Delay to Output High Level (t_{pdH})			200	300	ns
Delay to Output Low Level (t_{pdL})			200	300	ns

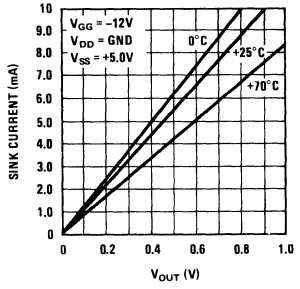
Note 1: Capacitance is guaranteed by periodic testing.
Note 2: For static operation clock must remain at V_{IL}.

typical performance characteristics

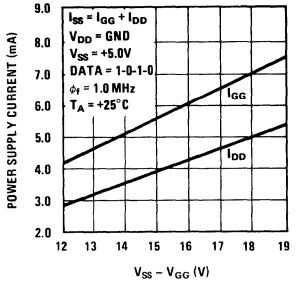
Typical Data Output Source Current vs Data Output Voltage



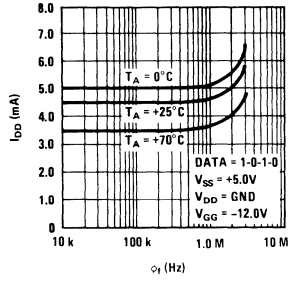
Typical Data Output Sink Current vs Data Output Voltage



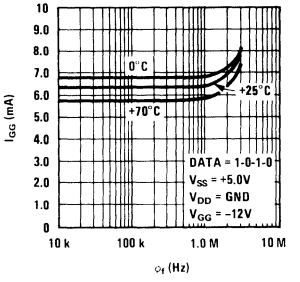
Typical Power Supply Current vs V_{GG}



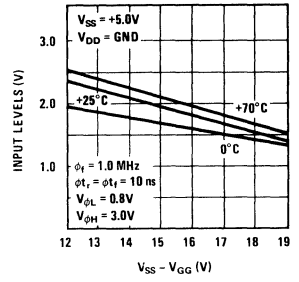
Typical I_{DD} vs Clock Frequency



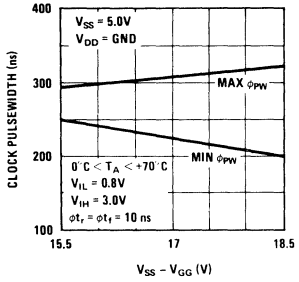
Typical I_{GG} vs Clock Frequency



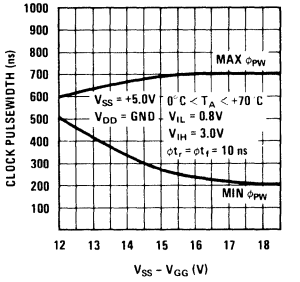
Typical Input Levels vs V_{GG}



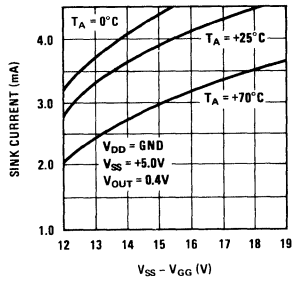
Typical 2.2 MHz Operating Curve



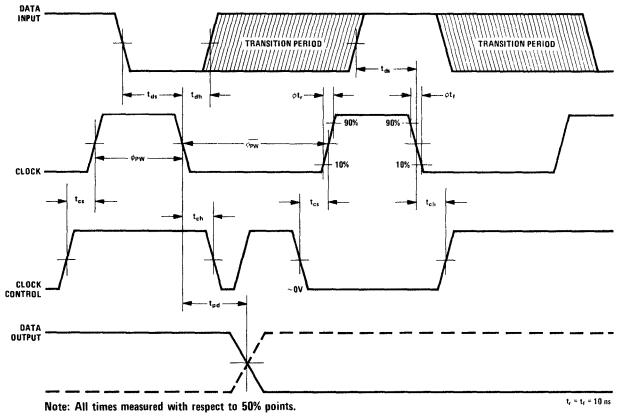
Typical 1.0 MHz Operating Curve



Typical Data Output Sink Current vs V_{GG}



switching time waveforms



Note: All times measured with respect to 50% points.

$t_r = t_f$ = 10 ns

FIGURE 1

ac test circuit

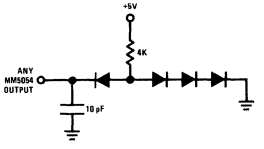


FIGURE 2

Static Shift Registers

MM4055/MM5055 quad 128-bit static shift register
MM4056/MM5056 dual 256-bit static shift register
MM4057/MM5057 512-bit static shift register

general description

The MM4055/MM5055, MM4056/MM5056, MM4057/MM5057 512-bit static shift registers are MOS monolithic integrated circuits using silicon gate technology to achieve bipolar compatibility. They have a guaranteed operating frequency of 1.0 and 1.5 MHz respectively, and an on chip clock generator allows TTL level clock driver for complete TTL compatibility.

features

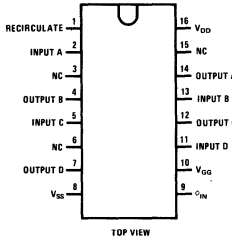
- Guaranteed operation
  - 1.5 MHz 0°C to +70°C
  - 1.0 MHz −55°C to +125°C
- Single TTL compatible clock, on chip clock generator
- Low clock capacitance 10 pF (typ)
- Operates from +5.0V, GND, and −12V
- Three configurations
  - MM4055/MM5055 Quad 128 bit
  - MM4056/MM5056 Dual 256 bit
  - MM4057/MM5057 Single 512 bit
- Internal recirculate

applications

- CRT displays
- Terminals
- Disk and drum replacements
- Buffer memory

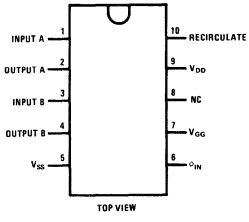
connection diagrams

Dual-In-Line Package



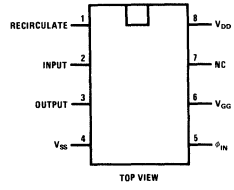
Order Number MM4055D or MM5055D
See Package 3
Order Number MM5055N
See Package 15

Dual-In-Line Package



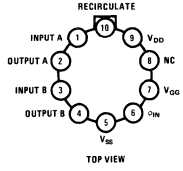
Order Number MM5056N
See Package 13

Dual-In-Line Package



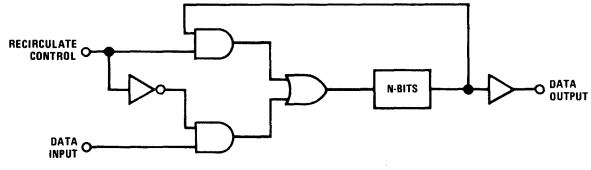
Order Number MM4057D or MM5057D
See Package 1
Order Number MM5057N
See Package 12

Metal Can Package



Order Number MM4056H or MM5056H
See Package 24

logic diagram



absolute maximum ratings (Note 1)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW @ $T_A = 25^\circ C$
Operating Temperature Range	
MM5055, MM5056, MM5057	0°C to 70°C
MM4055, MM4056, MM4057	−55°C to 125°C Case
Storage Temperature Range	−65°C to 160°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (MM4055, MM4056, MM4057)

$T_A = -55^\circ C$ to $+125^\circ C$, $V_{SS} = 5.0V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, $V_{DD} = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Recirculate and Clock Input Levels					
Logical High Level (V_{IH})		$V_{SS} - 1.0$		$V_{SS} + 0.3$	V
Logical Low Level (V_{IL})		$V_{SS} - 15$		$V_{SS} - 4.2$	V
Data, Recirculate and Clock Input Leakage	$V_{IN} = -10V$, $T_A = 25^\circ C$ All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	$V_{IN} = 0V$, f = 1 MHz All Other Pins GND (Note 2)		4.5	6.0	pF
Recirculate Input Capacitance	$V_{IN} = 0V$, f = 1 MHz All Other Pins GND (Note 2)		3.0	6.0	pF
Clock Capacitance	$V_{IN} = 0V$, f = 1 MHz All Other Pins GND (Note 2)		10	14	pF
Data Output Levels					
Logical High Level (V_{OH})	$I_{SOURCE} = -0.5$ mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	$I_{SINK} = 1.6$ mA	V_{DD}		0.4	V
Power Supply Current	$T_A = 25^\circ C$, $V_{GG} = -12V$, $V_{SS} = 5.0V$ $V_{DD} = 0V$, $\phi_{PW} = 230$ ns Data = 0-1-0-1 · · ·				
I_{GG}	$\phi_f \leq 0.1$ MHz		6.5	9.0	mA
	$\phi_f \leq 1.6$ MHz		10.5	15.5	mA
I_{DD} (Note 4)	$\phi_f \leq 0.1$ MHz		13	18	mA
	$\phi_f \leq 1.6$ MHz		15	20	mA
Clock Frequency (ϕ_f)	$\phi_{tr}, \phi_{tf} \leq 10$ ns (Note 5)		2.2	1.0	MHz
Clock Pulse Width					
(ϕ_{PW})	$\phi_{tr}, \phi_{tf} \leq 10$ ns (See ac Test Circuit)	−400	0.280	10	μs
$\overline{(\phi_{PW})}$	$\phi_{tr}, \phi_{tf} \leq 10$ ns (See ac Test Circuit)	−400	0.160	dc	μs
Data Input Setup Time (t_{ds})	$t_r, t_f \leq 10$ ns For Load Conditions See ac Test Circuit	260			ns
Data Input Hold Time (t_{dH})		120			ns
Recirculate Setup Time (t_{ds})		260			ns
Recirculate Hold Time (t_{dH})		120			ns
Data Output Propagation Delay					
Delay to High Level (t_{pdH})			350	700	ns
Delay to Low Level (t_{pdL})			350	700	ns

electrical characteristics (con't) (MM5055, MM5056, MM5057)

$T_A = 0°C$ to $+70°C$, $V_{SS} = 5.0V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, $V_{DD} = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Recirculate and Clock Input Levels					
Logical High Level (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 0.3$	V
Logical Low Level (V_{IL})		$V_{SS} - 15$		$V_{SS} - 4.2$	V
Data, Recirculate and Clock Input Leakage	$V_{IN} = -10V$, $T_A = 25°C$ All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND (Note 2)		4.5	6.0	pF
Recirculate Input Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND (Note 2)		3.0	6.0	pF
Clock Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND (Note 2)		10	14	pF
Data Output Levels					
Logical High Level (V_{OH})	$I_{SOURCE} = -0.5$ mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	$I_{SINK} = 1.6$ mA	V_{DD}		0.4	V
Power Supply Current	$T_A = 25°C$, $V_{GG} = -12V$, $V_{SS} = 5.0V$ $V_{DD} = 0V$, $\phi_{PW} = 230$ ns Data = 0-1-0-1 • • •				
I_{GG}	$\phi_f \leq 0.1$ MHz		6.5	9.0	mA
	$\phi_f \leq 2.2$ MHz		13	19	mA
I_{DD} (Note 4)	$\phi_f \leq 0.1$ MHz		13	18	mA
	$\phi_f \leq 2.2$ MHz		15	20	mA
Clock Frequency (ϕ_f)	$\phi_{tr}, \phi_{tf} \leq 10$ ns (Note 5)		3.0	1.5	MHz
Clock Pulse Width					
($\underline{\phi_{PW}}$)	$\phi_{tr}, \phi_{tf} \leq 10$ ns	0.230	0.100	100	μs
(ϕ_{PW})	$\phi_{tr}, \phi_{tf} \leq 10$ ns	0.300	0.100	dc	μs
Data Input Setup Time (t_{ds})	$t_r, t_f \leq 10$ ns For Load Conditions See Test Circuit	110			ns
Data Input Hold Time (t_{dH})		40			ns
Recirculate Setup Time (t_{ds})		110			ns
Recirculate Hold Time (t_{dH})		40			ns
Data Output Propagation Delay					
Delay to High Level (t_{pdH})			250	345	ns
Delay to Low Level (t_{pdL})			250	345	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

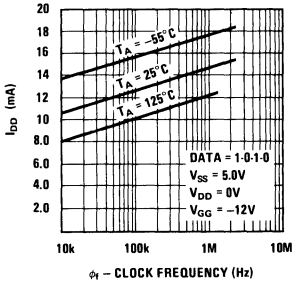
Note 3: Positive true logic notation is used:
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: Outputs not loaded when measuring I_{DD}. Add 1.6 mA to I_{DD} for each TTL load to compute worst case power.

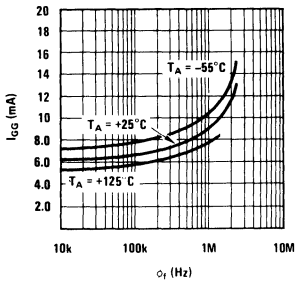
Note 5: For static operation clock must remain at V_{IL}.

typical performance characteristics

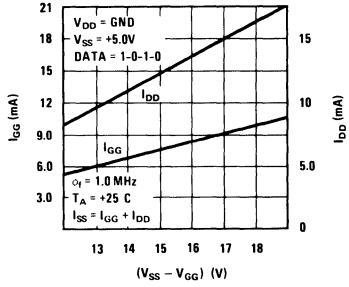
Typical I_{DD} vs Clock Frequency



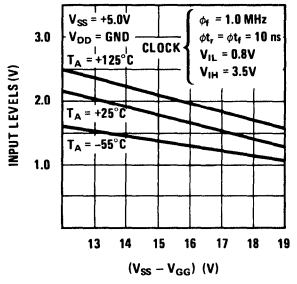
Typical I_{GG} vs Clock Frequency



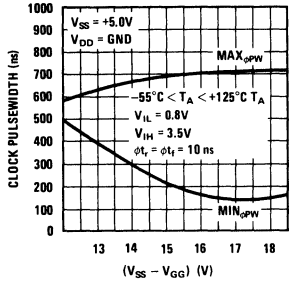
Typical Power Supply Current vs V_{GG}



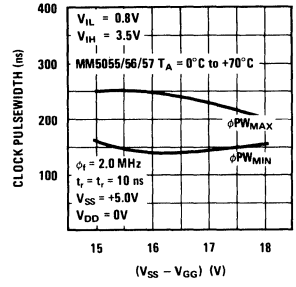
Typical Input Levels vs V_{GG}



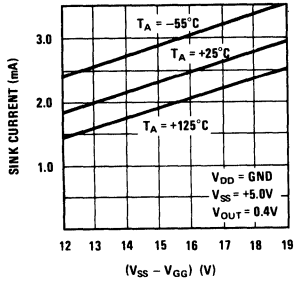
Typical 1.0 MHz Operating Curve



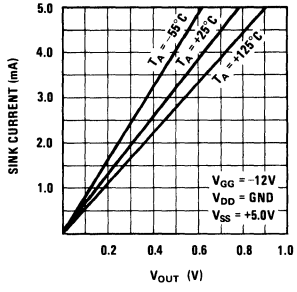
Typical 2.0 MHz Operating Curve



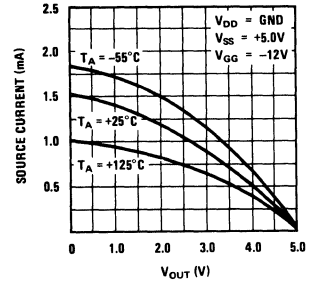
Typical Data Output Sink Current vs V_{GG}



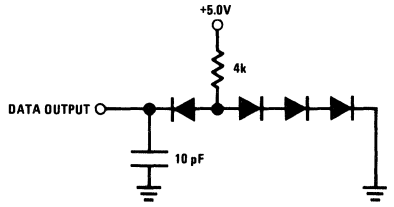
Typical Output Sink Current vs Data Output Voltage



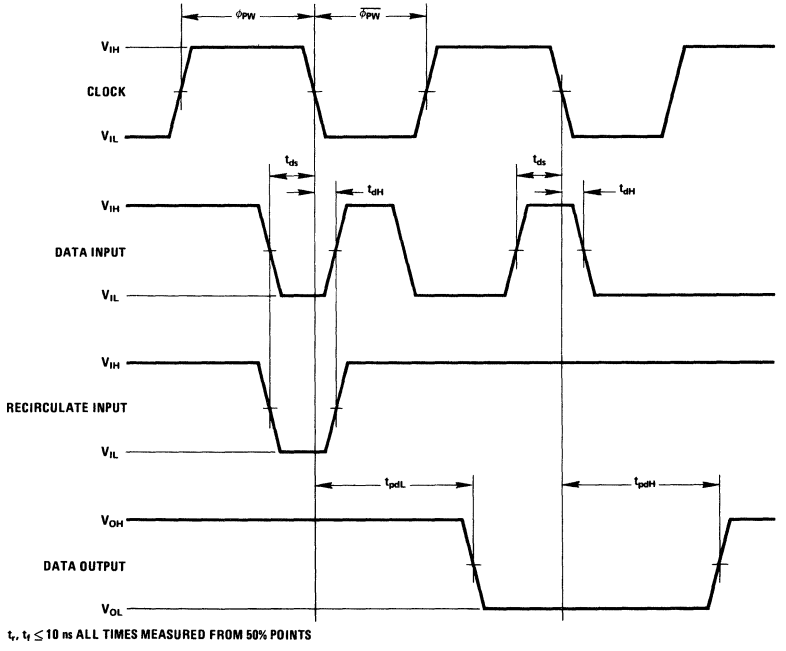
Typical Data Output Source Current vs Data Output Voltage



test circuit



switching time waveforms



$t_r, t_f \leq 10$ ns ALL TIMES MEASURED FROM 50% POINTS

Static Shift Registers

MM5058 1024-bit static shift register

general description

The MM5058 is a monolithic 1024-bit static shift register utilizing a low threshold P-channel silicon gate technology to achieve bipolar compatibility. "Stream select" logic on the chip chooses between two inputs, facilitating external recirculate operation. This in addition to an internal clock-driver, thus providing a single external TTL/DTL clock, makes this device flexible and convenient to integrate into existing TTL/DTL or MOS systems.

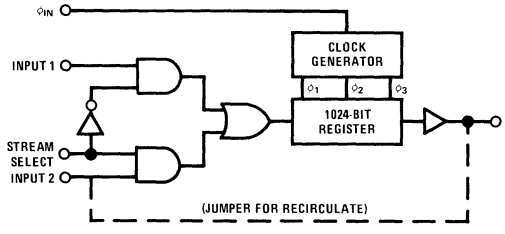
features

- Bipolar compatibility — All inputs, outputs, and clock interface directly with standard TTL/DTL circuits with no external components
- Single phase clock — On chip clock driver provides single TTL/DTL level clock with low input capacitance
- High frequency operation — DC to 1.5 MHz guaranteed
- Standard power supplies — +5.0V and −12V
- Small package — 8-pin mini DIP
- Low power consumption — 250μW/bit typ
- Stream select for easy external recirculate

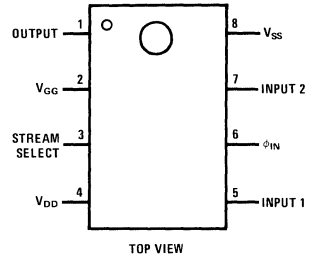
applications

- Sequential access memories
- Static buffer memories
- CRT refresh
- Delay lines
- Drum memory replacement

logic and connection diagrams



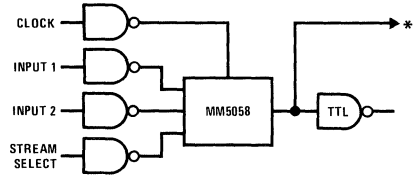
Dual-In-Line Package



TOP VIEW

Order Number MM5058N
See Package 12

ac test circuit



*PROPAGATION DELAYS MEASURED AT MM5058 OUTPUT.

truth table

STREAM SELECT	FUNCTION
LOGIC "0"	INPUT 1
LOGIC "1"	INPUT 2

absolute maximum ratings (Note 1)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to -20V
Power Dissipation	535 mW @ T_A = 25°C
Operating Temperature Range	0°C to +70°C Ambient
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within specified operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Input Leakage (All Inputs)	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.05	0.5	μA
Input Capacitance (Note 2)	V_{IN} = 0V, f = 1.0 MHz (Note 1) All Other Pins (GND)		3.0	7.0	pF
Data Output Levels, TTL Load					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4	3.5		V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA	V_{DD}		0.4	V
Power Supply Current	DATA = 0-1-0-1				
I_{GG}	ϕ_f = 1.5 MHz Continuous Operation		8.0	13	mA
I_{SS}	DATA = 0-1-0-1 ϕ_f = 1.5 MHz Continuous Operation		38	60	mA

ac electrical characteristics

T_A within specified operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 10 ns		3.0	1.5	MHz
Clock Pulse Width					
ϕ_{PW}	$\phi t_r = \phi t_f$ = 10 ns	0.350	0.100	100	μs
$\overline{\phi_{PW}}$	$\phi t_r = \phi t_f$ = 10 ns	0.250		DC	μs
Clock Pulse Transition (t_r, t_f)				1.0	μs
Data Input Setup Time (t_{DS})	$t_r = t_f \leq$ 10 ns See AC Test Circuit for Load Conditions	100			ns
Data Input Hold Time (t_{DH})		30			ns
Stream Select Setup Time (t_{SS})		150			ns
Stream Select Hold Time (t_{SH})		30			ns
Data Output Propagation Delay From ϕ_{IN}					
Delay to High Level (t_{pdH})			200	300	ns
Delay to Low Level (t_{pdL})			200	300	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

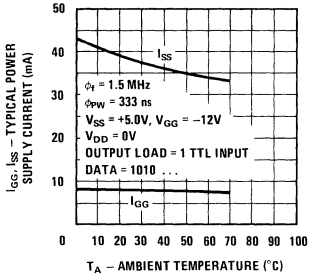
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logic "1" = most positive voltage level; Logic "0" = most negative voltage level.

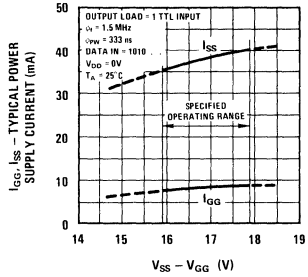
Note 4: Typical values apply for V_{SS} = 5.0V, V_{GG} = −12V, V_{DD} = 0V, and T_A = 25°C.

typical performance characteristics

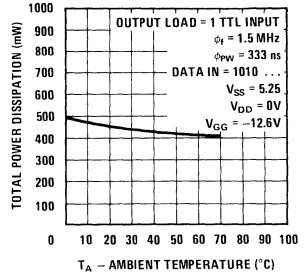
Typical Power Supply Current vs Temperature



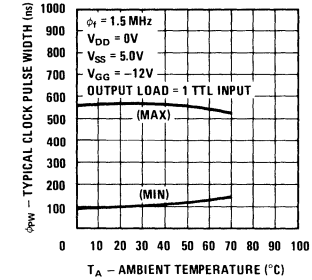
Typical Power Supply Current vs Supply Voltage



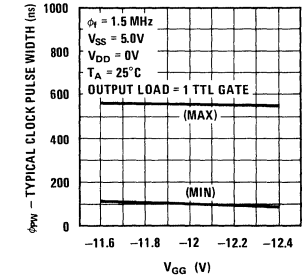
Guaranteed Power Consumption vs Temperature



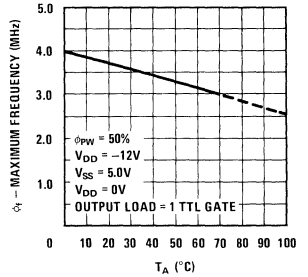
Typical Clock Pulse Width vs Ambient Temperature



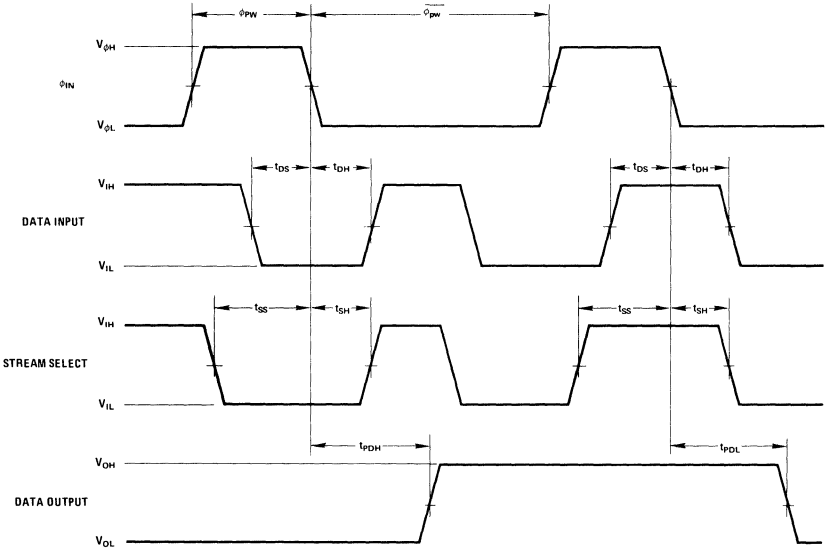
Typical Clock Pulse Width vs V_{GG}



Typical Maximum Frequency vs Ambient Temperature



switching time waveforms



NOTE 1: TIMES MEASURED AT 50% POINTS WITH t_r, $t_f \leq 10$ ns.
NOTE 2: FOR DC STORAGE CLOCK MUST REMAIN AT $V_{\phi L}$.

Static Shift Registers

MM5060 dual 144-bit mask programmable static shift register

general description

The MM5060 is a monolithic dual 144-bit static shift register/accumulator utilizing a silicon gate low threshold P-channel enhancement mode technology to achieve complete bipolar compatibility. The device can be programmed by metal mask option to custom lengths from 125 to 144-bits in one bit increments.

Standard Lengths:

MM5060AA
Dual 128-Bit Shift Register/Accumulator
MM5060AB
Dual 132-Bit Shift Register/Accumulator
MM5060AC
Dual 133-Bit Shift Register/Accumulator
MM5060AD
Dual 144-Bit Shift Register/Accumulator

Custom Lengths:

The programmed shift registers are assigned a letter code for each option. These are designated by a pair of letters after the number code but before the package designation such as MM5060AD/D which is a 0°C to +70°C dual 144-bit shift register/accumulator in an 8-lead cavity dual-in-line package. Pattern codes are assigned by National upon entry of order.

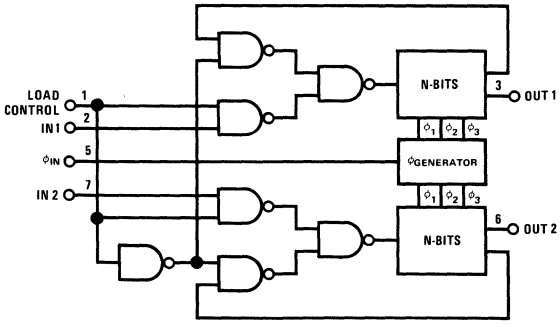
features

- Complete bipolar compatibility — input/output and clock input completely DTL/TTL compatible without additional components
- Standard Supplies +5V, −12V
- High frequency operation — DC to 3.0 MHz typical
- Single phase clock — DTL/TTL compatible on chip clock
- Low clock line capacitance 6.0 pF max.

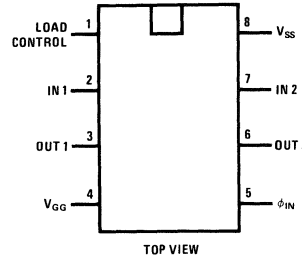
applications

- Printer memory — any length from 125 to 144-bits per line
- Telemetry systems and data sampling
- Serial memory storage

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5060AA/D, MM5060AB/D, MM5060AC/D, MM5060AD/D or MM5060XX/D
See Package 1

Order Number MM5060AA/N, MM5060AB/N, MM5060AC/N, MM5060AD/N or MM5060XX/N
See Package 12

truth table

LOAD CONTROL	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

absolute maximum ratings

Data and Clock Input Voltages and Supply Voltages with respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW @ T_A = 25°C
Operating Temperature Range	
MM5060	0°C to +70°C (Ambient)
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

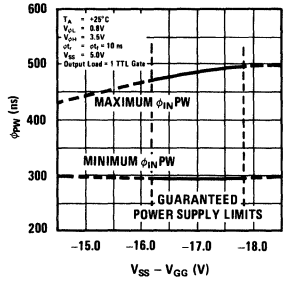
T_A within specified operating temperature range, V_{SS} = 5.0V ±5%, V_{GG} −12.0V ±5%, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10.0		V_{SS} − 4.2	
Data Input Leakage	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		3.0	5.0	pF
Load Control Input Levels					
Logical High Level (V_H)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_L)		V_{SS} − 10.0		V_{SS} − 4.2	V
Load Control Input Leakage	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		3.0	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 10.0		V_{SS} − 4.2	V
Clock Input Leakage	V_ϕ = −10.0V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		3.5	6.0	pF
Data Output Levels TTL Load					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	3.0	3.5		V
Logical High Level MOS Load (V_{OH})	I_{SOURCE} = −0.01 mA	4.0	4.5		V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current (I_{GG})	T_A = 25°C, V_{GG} = −12V ϕ_{PW} = 300 ns, V_{SS} = +5.0V Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		20.0	24.0	mA
	ϕ_f = 1.0 MHz		21.0	25.0	mA
	ϕ_f = 1.5 MHz		22.0	26.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 10 ns, T_A = 25°C	DC	3.0	1.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_r = \phi t_f$ = 10 ns, T_A = 25°C	0.300	0.100	100	μs
($\overline{\phi_{PW}}$)		0.200		DC	μs
Clock Pulse Transition (ϕt_r, ϕt_r)				1	μs
Data Input Setup Time (t_{ds})	T_A = 25°C, t_r, t_f = 10 ns	70			ns
Data Input Hold Time (t_{dh})	T_A = 25°C, t_r, t_f = 10 ns	50			ns
Load Control Setup (t_{ds})	T_A = 25°C, t_r, t_f = 10 ns	70			ns
Load Control Hold (t_{dh})	T_A = 25°C, t_r, t_f = 10 ns	50			ns
Data Output Propagation Delay from ϕ in	T_A = 25°C, t_r, t_f = 10 ns				
Delay to High Level (t_{pdH})			250	350	ns
Delay to Low Level (t_{pdL})			250	350	ns

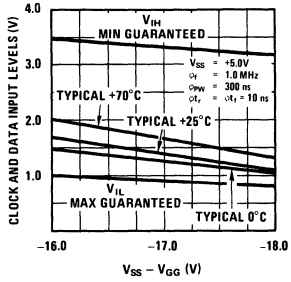
Note 1: Capacitance is guaranteed by periodic testing.

typical performance characteristics

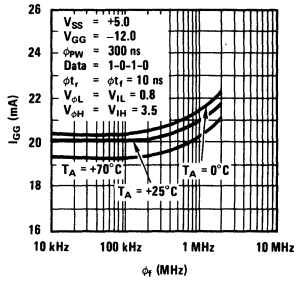
Guaranteed 1.5 MHz Operating Curve



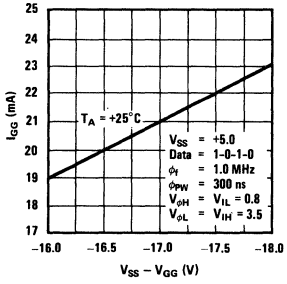
Guaranteed Input Voltage Levels vs Supply Voltage



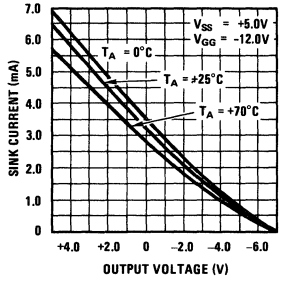
Typical I_{GG} vs Clock Frequency Under TTL Load



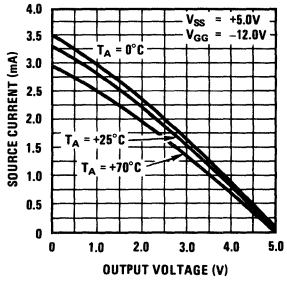
Typical Power Supply Current vs Voltage Under TTL Load



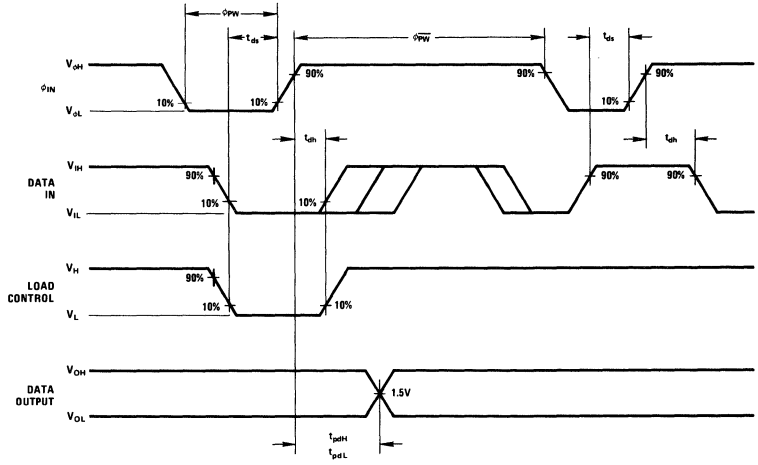
Typical Output Sink Current vs Output Voltage



Typical Output Source Current vs Output Voltage



switching time waveforms



Note: DC storage is accomplished during ϕ_{PW} time.

Static Shift Registers

MM5061 quad 100-bit static shift register

general description

The MM5061 quad 100-bit static shift register is a MOS monolithic integrated circuit using silicon gate technology to achieve bipolar compatibility. It has a guaranteed operating frequency of 2.2 MHz and an on chip clock generator.

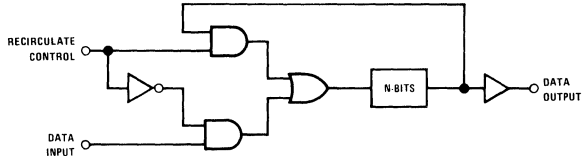
features

- Guaranteed 2.2 MHz operation
- Single TTL compatible clock on chip clock generator
- Low clock capacitance 10 typ, 14 max.
- Operates from +5V, GND, and -12V
- Configuration Quad 100-bit
- Internal recirculate

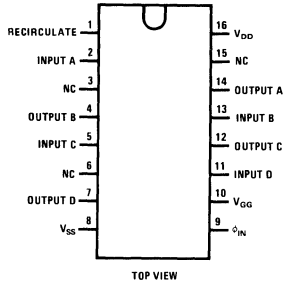
applications

- CRT displays
- Terminals
- Disk and drum replacements
- Buffer memory

logic and connection diagrams



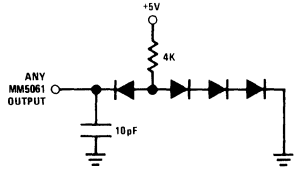
Dual-In-Line Package



TOP VIEW

Order Number MM5061D
See Package 3
Order Number MM5061N
See Package 15

test circuit



truth table

RECIRCULATE CONTROL	FUNCTION
1	Data Recirculates
0	Register Accepts Input Data

absolute maximum ratings (Note 1)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW @ T_A = 25°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{GG} = −12V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Level					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −10.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance (Note 2)	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND		4.5	6.0	pF
Recirculate Input Levels					
Logical High Level (V_H)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_L)		V_{SS} − 10		V_{SS} − 4.2	V
Recirculate Input Leakage	V_{IN} = 10.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Recirculate Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND		3.0	6.0	pF
Clock Input Levels					
Logical High Level (V_{OH})		V_{SS} - 1.0		V_{SS} + 0.3	V
Logical Low Level (V_{OL})		V_{SS} - 10.0		V_{SS} − 4.2	V
Clock Input Leakage	V_ϕ = −10.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Clock Capacitance (Note 2)			10.0	14.0	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −3.0 mA	2.85		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current (I_{GG})	T_A = 25°C, V_{GG} = −12.0V, ϕ_{PW} = 160 ns, V_{SS} = +5.0V, V_{OL} = 0.8V, Data = 0-1-0-1, V_{DD} = 0.0V				
	$\phi_f \leq$ 0.1 MHz		6.5	9.0	mA
	ϕ_f = 2.2 MHz		13.0	19.0	mA
(I_{DD})(Note 4)	$\phi_f \leq$ 0.1 MHz		13.0	18.0	mA
	$\phi_f \leq$ 2.2 MHz		15.0	20.0	mA
Clock Frequency ϕ_f	$\phi t_r = \phi t_f \leq$ 10 ns		3.0	2.2	MHz
Clock Pulse Width ϕ_{PW}	$\phi t_r = \phi t_f \leq$ 10 ns	0.230	0.100	10.0	μs
$\overline{\phi_{PW}}$	$\phi t_r = \phi t_f \leq$ 10 ns	0.200		DC	μs
Data Input Setup Time (t_{dS})	$t_r, t_f \leq$ 10 ns For Load Conditions see Test Circuit	100			ns
Data Input Hold Time (t_{dH})		40			ns
Recirculate Setup (t_{dS})		100			ns
Recirculate Hold (t_{dH})		40			ns
Data Output Propagation Delay from ϕ					
Delay to High Level (t_{pdH})			250	350	ns
Delay to Low Level (t_{pdL})			250	350	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

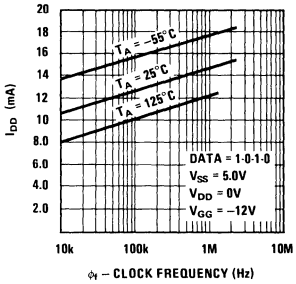
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logic "1" = most positive voltage level; Logic "0" = most negative voltage level.

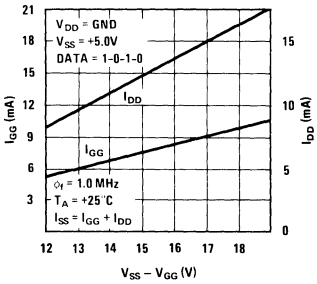
Note 4: Outputs not loaded when measuring I_{DD} therefore I_{DD} will increase by 1.6 mA for each TTL load (TTL "0" level output).

typical performance characteristics

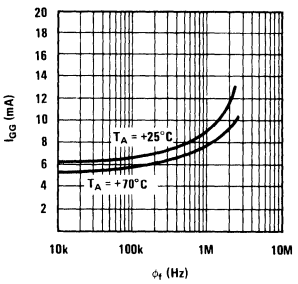
Typical I_{DD} vs Clock Frequency



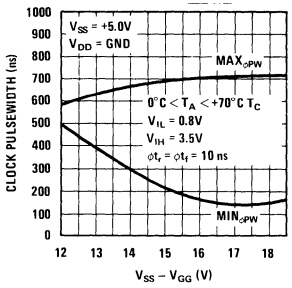
Typical Power Supply Current vs V_{GG}



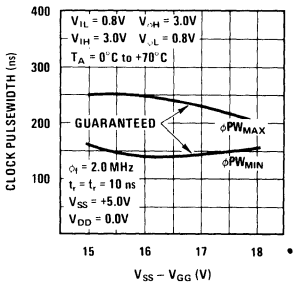
Typical I_{GG} vs Clock Frequency



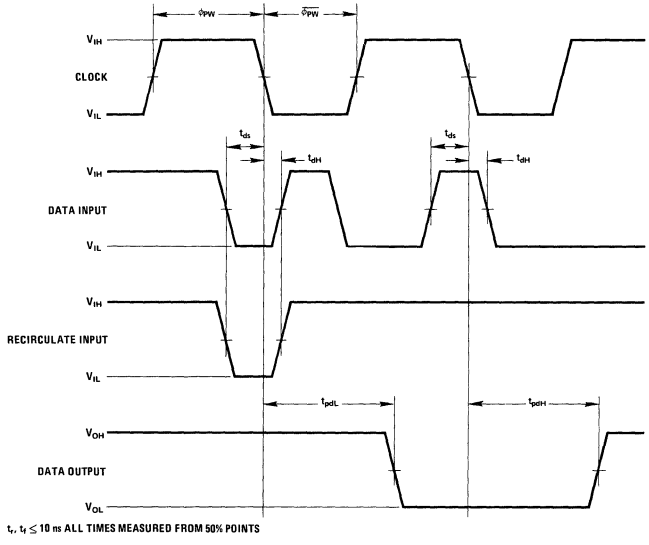
Guaranteed 1.0 MHz Operating Curve



Guaranteed 2.0 MHz Operating Curve



switching time waveforms



t_r, $t_f \leq 10$ ns ALL TIMES MEASURED FROM 50% POINTS

PROMs/ROMs

MM3501 1024-bit read-only memory

general description

The MM3501 is a 1024-bit read-only memory programmed in a 128 word by 8 bit format. It is an MOS monolithic integrated circuit utilizing P-channel enhancement mode technology. The fixed program memory is specified by the customer and customized by modifying one mask in the fabrication process. This results in a fast turn-around, low cost custom memory.

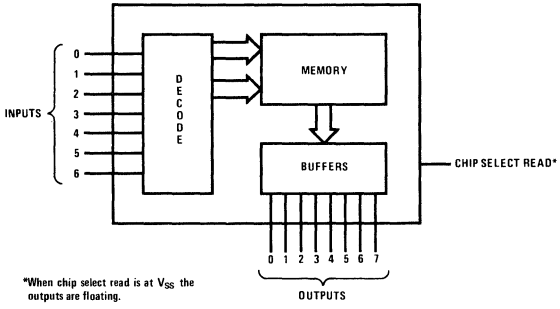
features

- Chip select
- 1.5 μs typical access time
- 115 mW typical static operation
- Low power consumption
- Bipolar compatible outputs

applications

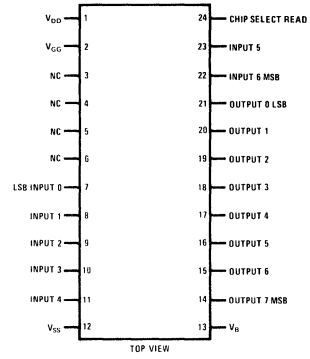
- Microprogramming
- Code conversion
- Table lookup
- Control logic

logic and connection diagrams



*When chip select read is at V_{SS} the outputs are floating.

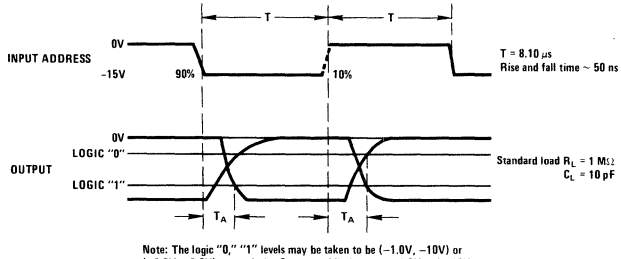
Dual-In-Line Package



Order Number MM3501J
See Package 11
Order Number MM3501N
See Package 18

switching time waveforms

Access and Chip Select Times



Note: The logic "0," "1" levels may be taken to be (−1.0V, −10V) or (−2.0V, −9.0V) respectively. Guaranteed limits are at −1.0V and −10V.

Note: For programming information see AN-100.

absolute maximum ratings

All Voltages and Data Input Lines with Respect to V_{SS}	−30V to +0.3V
Power Dissipation	250 mW
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (soldering, 10 sec.)	300°C

electrical characteristics

T_A within operating temperature range $V_{DD} = -13V \pm 1.0V$, $V_{GG} = -27V \pm 2.0V$, $V_B = -27V \pm 2.0V$, $V_{SS} = 0V$ (GND), unless otherwise noted.

CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
Input Logic Levels					
Logic "0"		$V_{SS}-2.0$		V_{SS}	V
Logic "1"				$V_{SS}-9.0$	V
Input Capacitance	(Note 4)		7.0	15	pF
Input Leakage	$V_{IN} = -15V$ (Note 5)			1.0	μA
Output Logic Levels					
Logic "0"	$I_L = -10\mu A$	$V_{SS}-1.0$		V_{SS}	V
Logic "1"	$I_L = +10\mu A$			$V_{SS}-10$	V
Access Time (T_A)	$R_L = 1.0\ M\Omega$, $C_L = 10$ pF (Notes 2 and 3, See Waveform)		1.5	4.0	μs
Output Current					
Logic "1"	$V_{OUT} = -4.6V$ (Forced) ($V_B = V_{DD}$)	1.6			mA
Logic "0"	$V_{OUT} = -1.0V$ (Forced) (Note 6)	−0.15	−0.24		mA
Logic "1"	$V_{OUT} = -10V$ (Forced) (Note 6)	0.30	0.85		mA
Supply Current Drain					
I_{DD}	$V_{DD} = -14V$, $V_{GG} = -29V$			6.5	mA
I_{GG}	(Note 2)			4.0	mA
Power Consumption	(Notes 1 and 2)		115	215	mW

Note 1: Exclusive of I_B (load current)
Note 2: $T_A = +25°C$.
Note 3: Sample tested.
Note 4: Guaranteed by design.
Note 5: Address and chip select inputs all pins grounded except the one under test
Note 6: $V_{DD} = -12V$, $V_{GG} = -25V$ (worst case condition of measurement)

PROMs/ROMs

MM5202A electrically programmable 2048-bit read only memory (PROM)

general description

The MM5202A is a 2048-bit static read only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256-8-bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 50V pulse.

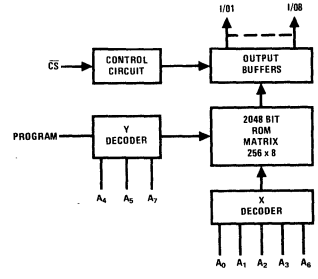
features

- Field programmable
- Bipolar compatibility +5.0V, −9.0V operation
- High speed operation 1.0μs max access time
- Pin compatible with INTEL 1602A, 1702A during read operation only
- Program on an approved MM5203 programmer
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- "Q" quartz lid version erasable with short wave ultra-violet light (i.e. 253.7 n.m.)
- Chip select output control
- 256 x 8

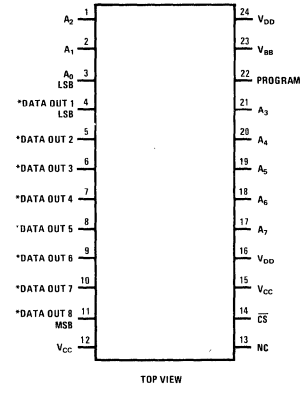
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

block and connection diagrams



Dual-In-Line Package



*This pin is the data input lead during programming.

Order Number MM5202AD
See Package 6
Order Number MM5202AQ
See Package 21

Note: For programming information see AN-100.

absolute maximum ratings

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.5V to −20V
Power Dissipation	1.0W
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A = 0°C to +70°C, V_{SS} = +5.0V ±5%, V_{DD} = −9.0V ±5%, V_{BB} = PROGRAM = V_{SS} unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current (I_{LI})	V_{IN} = 0V			1.0	μA
Output Leakage (I_{LO})	V_{OUT} = 0V, $\overline{CS}$ = V_{SS} − 2.0			1.0	μA
Power Supply Current (I_{SS})	$\overline{CS}$ = V_{SS} − 2.0		25	35	mA
Input LOW Voltage (V_{IL})		V_{SS} − 10		V_{SS} − 4.0	V
Input HIGH Voltage (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Output LOW Voltage (V_{OL})	1.6 mA Sink			0.40	V
Output Clamp Current (I_{CF})	V_{DD} = −12.6V, V_{OUT} = −1.0V, T_A = 0°C		8.0	14.0	mA
Output HIGH Voltage (V_{OH})	0.5 mA Source	2.4			V
Data Hold Time (T_{OH})	(Min Access Time) Figures 1 & 2			100	ns
Access Time (T_{ACC})	Figures 1 & 2 (Note 6)			1.0	μs
Chip Select Time (T_{CO})	Figures 1 & 3			500	ns
Chip Deselect Time (T_{OD})	Figures 1 & 3			500	ns
Allowable Chip Select Delay (t_{CS})	Figures 1 & 2. Allowable delay in selecting chip after change of address without affecting access time.			100	ns
Input Capacitance (C_{IN})	V_{IN} = V_{SS}, f = 1.0 MHz (Note 1)		8.0	15	pF
Output Capacitance (C_{OUT})	V_{OUT} = V_{SS}, f = 1.0 MHz (Note 1) $\overline{CS}$ = V_{SS} − 2.0		8.0	15	pF

programming characteristics (See Note 2 and Figure 4)

T_A = 25°C, V_{SS} = 0V, V_{BB} = +12V ±10%, $\overline{CS}$ = 0V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address and Data Input Load Current (I_{LD})	V_{IN} = −50V		0	10	mA
Program Load Current (I_{LP})	V_{IN} = −50V		0	10	mA
V_{BB} Supply Load Current (I_{LB})			0	10	mA
Peak I_{DD} Supply Load Current (I_{LDD})(Note 3)	V_{DD} = $V_{PROGRAM}$ = −50V		650		mA
Input High Voltage (V_{IHP})		−2.0		+0.3	V
Address and Data Input Low Voltage (V_{ILP})		−50		−40	V
Pulsed Input Low Voltage: V_{DD}, and Program, V_{DLP}		−50		−48	V
V_{DD} Pulse Duty Cycle				2.0	%
Program Pulse Width (t_{PW})(Note 4)	V_{DD} = $V_{PROGRAM}$ = −50V			20	ms
Data and Address Set Up Time (t_{DW})		1.0			μs
Data and Address Hold Time (t_{DH})		0			μs
Pulsed V_{DD} Supply Overlap (t_{SS})		1.0		100	μs
Pulsed V_{DD} Supply Overlap (t_{SH})		−0.1		3.0	ms
V_{DD}, Program, Address, and Input Rise and Fall Times				1.0	μs

Note 1: Capacitances are not tested on a production basis but are periodically sampled.

Note 2: The MM5202A should be programmed only on an approved MM5203 programmer.

Note 3: I_{DDP} flows only during program period t_{PWP}. Average power supply current I_{LDD} is typically 15 mA at 2% duty cycle.

Note 4: Maximum duty cycle of t_{PW} should not be greater than 2% of cycle time so that power dissipation is minimized. To guarantee long term memory retention the program cycle should be repeated ten times with t_{PW} = 20 ms or the equivalent thereof, i.e., 20 cycles of t_{PW} = 10 ms.

Note 5: T_{ACC} = 1000 ns + 25 (N−1) where N is the number of chips wired-OR together.

Note 6: Measured under continuous operation.

operation of the MM5202A in program mode

Initially, all 2048-bits of the MM5202A are in the HIGH state. Information is introduced by selectively programming LOWS in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the Read mode. The eight output terminals are used as data inputs to determine the information pattern in the 8-bits of each word. A LOW data input level (−50V) will leave a HIGH and a HIGH data input level will allow programming of a LOW. All 8-bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. The duty cycle of the V_{DD} pulse (amplitude and width as specified on page 4) should be limited to 2%. The address should be applied for at least 1.0μs before application of the Program pulse. In programming mode, data inputs 1 – 8 are pins 4 – 11 respectively. Chip select should be disabled (HIGH).

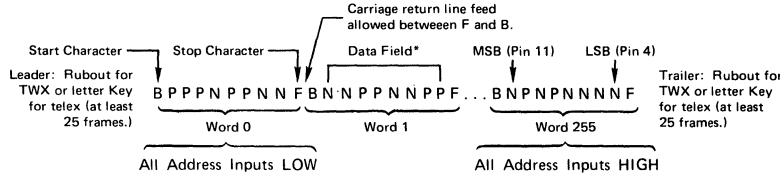
Positive logic is used during the read mode for addresses and data out. Address 0 corresponds to all address inputs at V_{IL} and address 255_{10} corresponds to all address inputs at V_{IH}. A "1" or a P at a data output corresponds to V_{OH}. A "0" or an N at a data output corresponds to V_{OL}. Positive logic is also used during the programming mode for addresses. Address 0 corresponds to all address inputs at V_{ILP} and address 255_{10} corresponds to all address inputs at V_{IHP}.

Negative logic is used during the programming mode for data in. A "1" or a P at a data input corresponds to V_{ILP}. A "0" or an N at a data input corresponds to V_{IHP}.

MODE	DATA AND ADDRESS LINES HIGH	DATA AND ADDRESS LINES LOW	V_{SS}	V_{BB}	V_{DD}	PROGRAM	$\overline{CS}$
Read	V_{SS} − 2.0	V_{SS} − 4.0	+5.0	V_{SS}	−9.0	V_{SS}	V_{SS} − 4.0V
Program	V_{SS} −2.0	V_{SS} − 40	GND	+12	−48 (Pulse)	−48 (Pulse)	GND

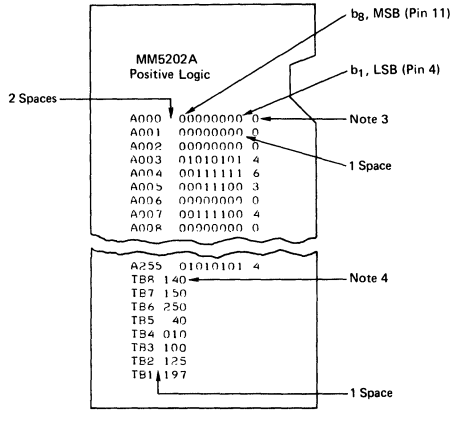
preferred tape format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example.



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 256 words must be entered, beginning with word 0.

alternate format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

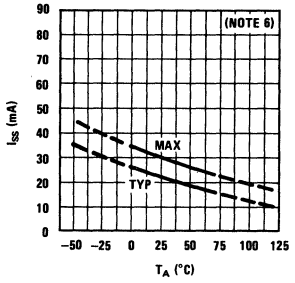
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

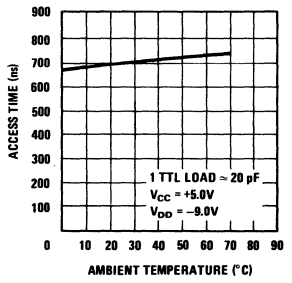
Note 4: The total number of "1" bits in each output column or bit position.

typical performance characteristics

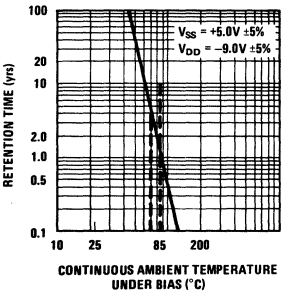
Maximum Supply Current I_{SS} as a Function of Temperature



Typical Access Time vs Temperature



Guaranteed Memory Retention Time Under Bias as a Function of Temperature



access time diagrams

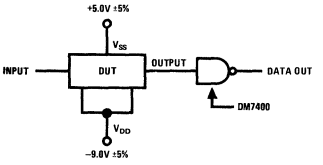


FIGURE 1.

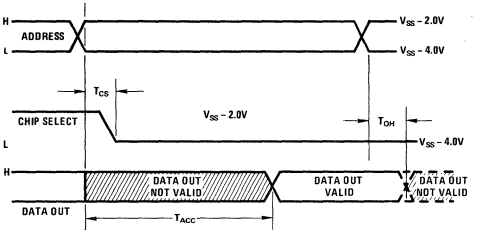


FIGURE 2.

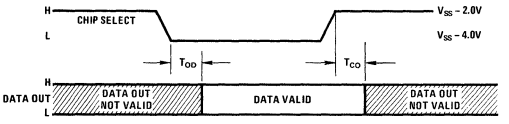


FIGURE 3.

program waveforms

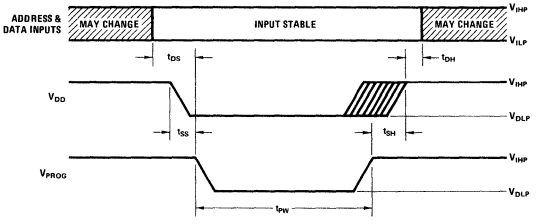
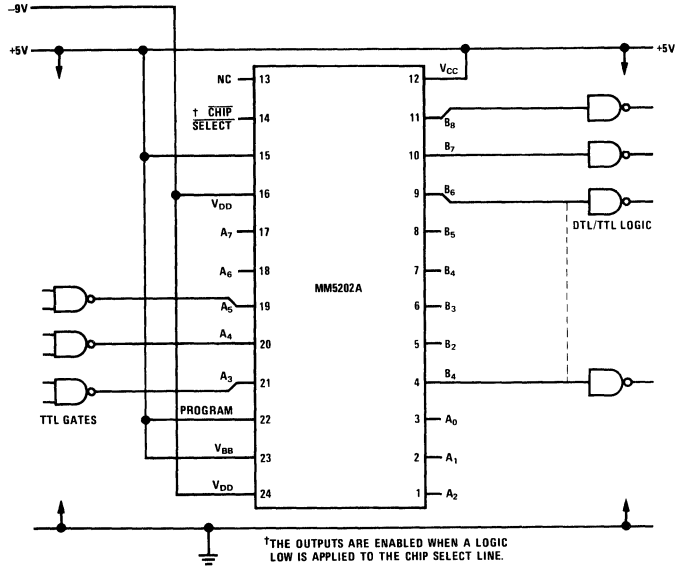


FIGURE 4.

typical application

256 x 8 pROM Showing TTL Interface



PROMs/ROMs

MM4203/MM5203 electrically programmable 2048-bit read only memory (PROM)

general description

The MM4203/MM5203 is a 2048-bit static read-only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256-8-bit words or 512-4-bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 50 volt pulse. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

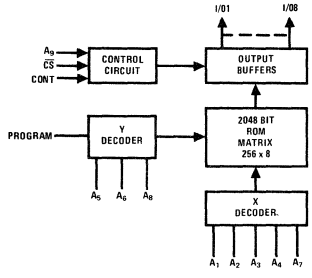
features

- Field programmable
- Bipolar compatibility +5V, −12V operation
- High speed operation 1μs max access time
- Pin compatible with MM5213, MM5231 mask programmable ROMs
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- "Q" quartz lid version erasable with short wave ultra-violet light (i.e. 253.7 n.m.)
- Chip select output control
- 256 x 8 or 512 x 4 organization

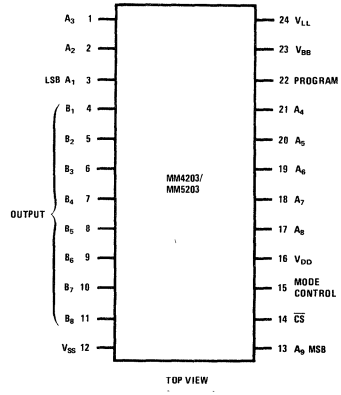
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

block and connection diagrams



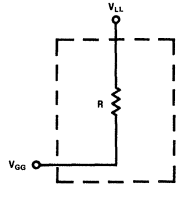
Dual-In-Line Package



Order Number MM4203D or MM5203D
See Package 6
Order Number MM4203Q or MM5203Q
See Package 21

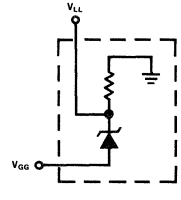
typical applications

FIGURE 1. Power Saver for Small Memory Arrays



Assume || V_{LL} || min = || −3V ||
$V_{GG} - V_{LL}$ min = R (1.6 mA) (N)
where N = 7 for 5 x 7 font
N = 8 for 6 x 8 font

FIGURE 2. Power Saver for Large Memory Arrays



Note: For programming information see AN-100.

absolute maximum ratings

All Input or Output Voltages with Respect to V_{BB} Except During Programming: +.3V to −20V
Power Dissipation: 1W
Operating Temperature Range MM4203: −55°C to 85°C
MM5203: 0°C to 70°C
Storage Temperature Range: −65°C to 125°C
Lead Temperature (Soldering, 10 sec): 300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, $V_{DD} = V_{LL}$ = −12V, ±5%, V_{BB} = PROGRAM = V_{SS} unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current, I_{LI}	V_{IN} = 0V			1	μA
Output Leakage, I_{LO}	V_{OUT} = 0V $\overline{CS} = V_{SS}$ - 2.0			1	μA
Power Supply Current, I_{SS}	T_A = 25°C $\overline{CS} = V_{SS}$ - 2.0		35	55	mA
Input LOW Voltage, V_{IL}		V_{DD} - 10		V_{SS} - 4.2	V
Input HIGH Voltage, V_{IH}		V_{SS} - 1.5		V_{SS} + .3	V
Output LOW Voltage, V_{OL}	1.6 mA sink $-12.6V < V_{LL} < -3V$			.40	V
Output Clamp Current, I_{CF}	V_{LL} = -3.0V V_{OUT} = -1.0V (Note 8) T_A = 0°C		3.5	6.0	mA
	V_{LL} = -12.6V V_{OUT} = -1.0V (Note 8) T_A = 0°C		8.0	15.0	mA
Output HIGH Voltage, V_{OH}	0.8 mA source	2.4			V
Data Hold Time, T_{OH}	(Min Access Time) Figures 1 & 2			100	ns
Access Time, T_{ACC}	T_A = 25°C Figures 1 & 2 (Note 6)		.700	1	μs
Chip Select Time, T_{CO}	Figures 1 & 3			500	ns
Chip Deselect Time, T_{OD}	Figures 1 & 3			500	ns
Allowable Chip Select Delay, t_{CS}	Figures 1 & 2 Allowable delay in selecting chip after change of address without affecting access time.			100	ns
Input Capacitance, C_{IN}	$V_{IN} = V_{SS}$ } f = 1.0 MHz (Note 2)		8	15	pF
Output Capacitance, C_{OUT}	$V_{OUT} = V_{SS}$ } $\overline{CS} = V_{SS}$ - 2.0		8	15	pF

programming characteristics (see Figure 4)

T_A = 25°C, V_{SS} = 0V, V_{BB} = +12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address and Data Input Load Current, I_{LD}	V_{IN} = −50V		0	10	mA
Program Load Current, I_{LP}	V_{IN} = −50V		0	10	mA
V_{BB} Supply Load Current, I_{LB}			0	10	mA
Peak I_{DD} Supply Load Current I_{LDD} (Note 3)	$V_{DD} = V_{program}$ = −50V		650		mA
Input High Voltage, V_{IHP}		−2		+.3	V
Address and Data Input Low Voltage, V_{ILP}		−50		−40	V
Pulsed Input Low Voltage:					
V_{DD}, and Program, V_{DLP}		−50		−48	V
V_{LL}	(Note 5)	−50		0	V
V_{DD} Pulse Duty Cycle				2	%
Program Pulse Width, t_{PW} (Note 4)	$V_{DD} = V_{program}$ = −50V			20	ms
Data and Address Set Up Time, t_{DW}		1			μs
Data and Address Hold Time, t_{DH}		0			μs
Pulsed V_{DD} Supply Overlap, t_{SS}		1		100	μs
Pulsed V_{DD} Supply Overlap, t_{SH}		−.1		3	ms
V_{DD}, Program, Address, and Input Rise and Fall Times				1	μs

Note 1: During programming, data is always applied in the 256 x 8 mode, regardless of the logic state of Ag and mode control.

Note 2: Capacitances are not tested on a production basis but are periodically sampled.

Note 3: I_{DDP} flows only during program period $t_{\phi PWP}$. Average power supply current I_{DDP} is typically 15 mA at 2% duty cycle.

Note 4: Maximum duty cycle of $t_{\phi PW}$ should not be greater than 2% of cycle time so that power dissipation is minimized. To guarantee long term memory retention the program cycle should be repeated five times with $t_{\phi PW}$ = 20 ms or the equivalent thereof, i.e. 10 cycles of $t_{\phi PW}$ = 10 ms.

operation of the MM4203/MM5203 in program mode

Initially, all 2048 bits of the MM4203/MM5203 are in the HIGH state. Information is introduced by selectively programming LOWS in the proper bit locations. (Note 1)

Word address selection is done by the same decoding circuitry used in the Read mode. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A LOW data input level (−50V) will leave a HIGH and a HIGH data input level will allow programming of a LOW. All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. The duty cycle of the V_{DD} pulse (amplitude and width as specified on page 4) should be limited to 2%. This can be increased to 4% if forced air cooling is used to cool the package. The address should be applied for at least 1μs before application of the Program pulse. In programming mode, data inputs 1–8 are pins 4–11 respectively regardless of the logic state of A_9 and mode control. Chip select should be disabled (HIGH).

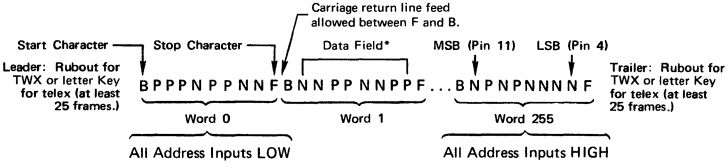
Positive logic is used during the read mode for addresses and data out. Address 0 corresponds to all address inputs at V_{IL} and address 255_{10} corresponds to all address inputs at V_{IH}. A "1" or a P at a data output corresponds to V_{OH}. A "0" or an N at a data output corresponds to V_{OL}. Positive logic is also used during the programming mode for addresses. Address 0 corresponds to all address inputs at V_{ILP} and address 255_{10} corresponds to all address inputs at V_{IHP}.

Negative logic is used during the programming mode for data in. A "1" or a P at a data input corresponds to V_{ILP}. A "0" or an N at a data input corresponds to V_{IHP}.

MODE	DATA AND ADDRESS LINES HIGH	DATA AND ADDRESS LINES LOW	V_{SS}	V_{BB}	V_{DD}	PROGRAM	$\overline{CS}$	V_{LL}
Read	V_{SS} − 2.0	V_{SS} − 4.0	+5	V_{SS}	−12	V_{SS}	V_{SS} − 4V	−3V to −12V
Program	V_{SS} −2.0	V_{SS} − 40	GND	+12	−48 (Pulse)	−48 (Pulse)	GND	GND to −50V

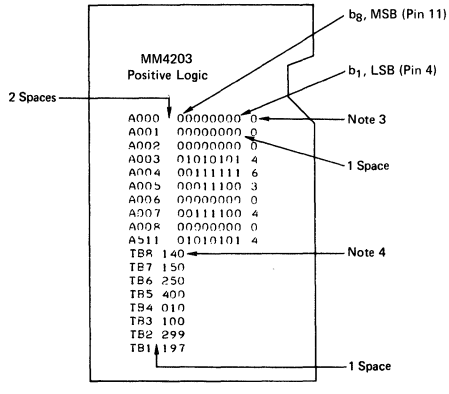
preferred tape format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 256 words must be entered, beginning with word 0.

alternate format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

access time diagrams

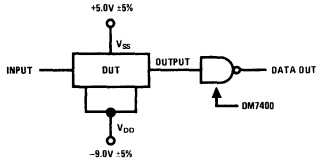


Figure 1

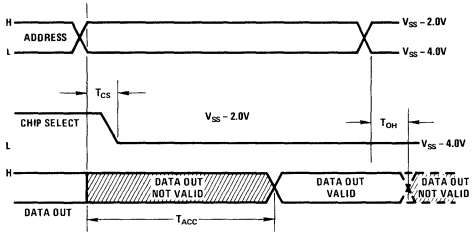


Figure 2

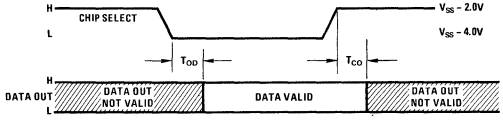
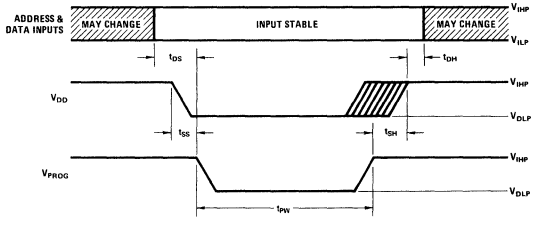


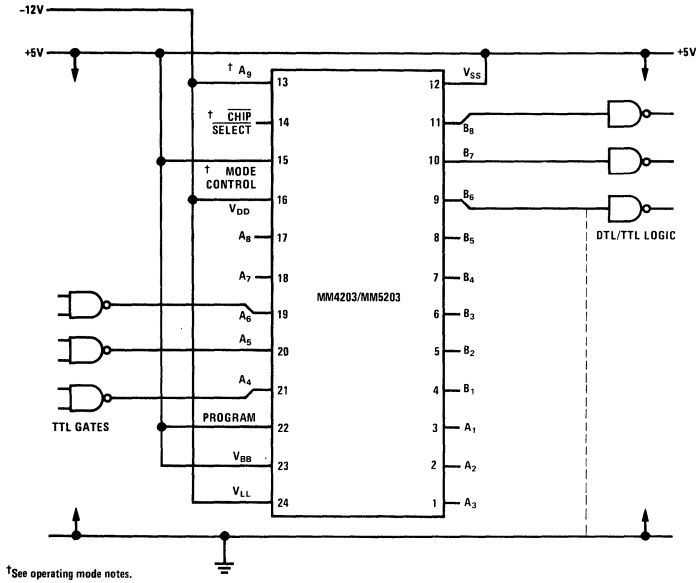
Figure 3

program waveforms



typical applications

256 x 8 PROM Showing TTL Interface



†See operating mode notes.

Operating Modes

256 x 8 ROM connection (shown)
Mode Control – HIGH (V_{SS})
A_9 – LOW

512 x 4 ROM connections
Mode Control – LOW (GND or V_{DD})
A_9 – Logic HIGH enables the odd (B_1, B_3 ... B_7) outputs
– Logic LOW enables the even (B_2, B_4 ... B_8) outputs

The outputs are enabled when a logic LOW is applied to the Chip Select line.

Programming is accomplished in 256 x 8 mode only.

PROMs/ROMs

MM5204 electrically programmable 4096-bit read only memory (PROM)

TENTATIVE DATA

general description

The MM5204 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a 50V pulse. A logic input, "Power Saver," is provided which gives a 5 to 1 decrease in power when the memory is not being accessed.

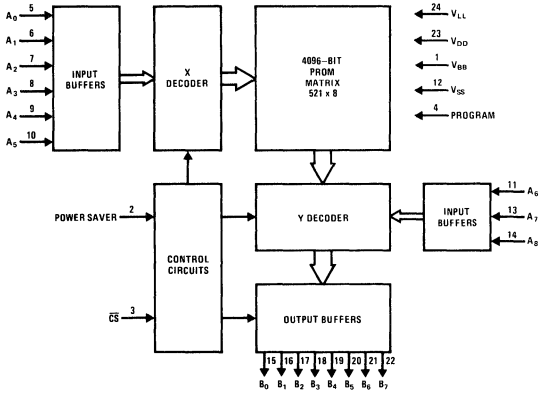
features

- Field programmable
- Fast program time 5 minutes for 4096-bits
- Fast access time 750 ns typ
- DTL/TTL compatibility
- Standard power supplies +5.0V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultra-violet light (i.e., 253.7 nm)
- "Power Saver" control for low power applications

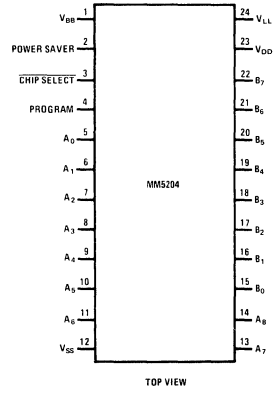
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

block and connection diagrams



Dual-In-Line Package



Order Number MM5204D
See Package 6

Order Number MM5204Q
See Package 21

Note: For programming information see AN-100.

absolute maximum ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	1.0 W
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Inputs					
Input Low Voltage (V_{IL})		V_{SS} − 14		V_{SS} − 4.2	V
Input High Voltage (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Input Current (I_{LI})	V_{IN} = 0V			1.0	μA
Outputs					
Output Low Voltage (V_{OL})	I_{OL} = 1.6 mA	V_{LL}		0.4	V
Output High Voltage (V_{OH})	I_{OH} = −0.8 mA	2.4		V_{SS}	V
Output Leakage Current (I_{LO})	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
Power Supply Current	T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}		28		mA
	T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}		6.0		mA

ac electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Access Time (t_{ACC})	T_A = 70°C (Figure 1) (Note 4)		0.75		μs
Power Saver Setup Time (t_{PS})	(Figure 1)		70		ns
Chip Select Delay (t_{CS})	Allowable delay in selecting device after address change without degrading T_{ACC} (Figure 1)		300		ns
Data Hold Time (t_{OH})	(Figure 1)		150		ns
Chip Select or Power Saver Setup Time (t_{CO})	(Figure 2)		300		ns
Chip Select or Power Saver Deselect Time (t_{OD})	(Figure 2)		300		ns
Input Capacitance (C_{IN}) (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz (Note 2)		8.0	15	pF
Output Capacitance (C_{OUT}) (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz (Note 2)		8.0	15	pF

electrical programming characteristics

(See Figure 3)(Note 5) T_A = 25°C, V_{SS} = CS = 0V, V_{BB} = 12V ±5%, V_{LL} = 0V to −14V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address and Data Input Load Current (I_{LD})	V_{IN} = −12V		0		mA
Program Load Current (I_{LP})	V_{IN} = −50V		−45		mA
V_{BB} Load Current (I_{LBB})			10		mA
I_{DD} Load Current (I_{LDD})	V_{DD} = PROGRAM = −50V		−20		mA
Address, Data and Power Saver Input High Voltage (V_{IHP})		−2.0		0.3	V
Address Data and Power Saver Input Low Voltage (V_{ILP})		−14		−11	V
V_{DD} and Program High Voltage (V_{DHP})		−2.0		0.5	V

electrical programming characteristics (con't)

(See Figure 3)(Note 5) $T_A = 25°C$, $V_{SS} = CS = 0V$, $V_{BB} = 12V \pm 5\%$, $V_{LL} = 0V$ to $-14V$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} and Program Low Voltage (V_{DLP})		−50		−48	V
V_{BB} Low Voltage (V_{BLP})		0		0.4	V
V_{BB} High Voltage (V_{BHP})		11.4		12.6	V
V_{DD} Pulse Duty Cycle				25	%
Program Pulse Width (t_{PW})		2.5		5.0	ms
Data and Address Setup Time (t_{DS})		40			μs
Data and Address Hold Time (t_{DH})		0			μs
Pulsed V_{DD} Setup Time (t_{SS})		40		100	μs
Pulsed V_{DD} Hold Time (t_{SH})		0			μs
Pulsed V_{BB} Setup Time (t_{BS})		1.0			μs
Pulsed V_{BB} Hold Time (t_{BH})		0			μs
Power Saver Setup Time (t_{PSS})		1.0			μs
Power Saver Hold Time (t_{PSH})		0			μs
V_{DD}, Program, Address and Data Rise and Fall Time (t_r, t_f)				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

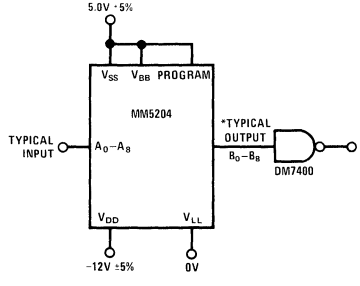
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used:
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: $T_{ACC} = 1500$ ns + 25(N−1) where N is the number of devices wire-OR'ed together.

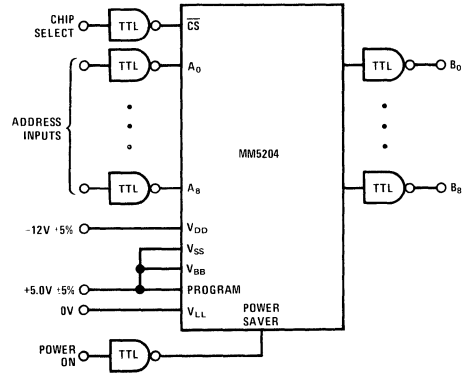
Note 5: Each address location, selected by inputs A_0 through A_8, must be programmed as shown in the timing diagram (Figure 3) for a minimum of 32 cycles at $t_{PW} = 5.0$ ms, or equivalent (i.e. 64 cycles at $t_{PW} = 2.5$ ms).

ac test circuit



*t_{ACC}, t_{OH}, t_{CO}, and t_{OD} measured at output of MM5204.

typical application



operation of the MM5204 in program mode

There are two methods of programming the MM5204 pROM: The first method is to ship units with all 4096 bits programmed to the logic "0" state, allowing the customer to selectively program logic "1's" in the desired bit locations. The second method is to submit to National Semiconductor the desired bit pattern, in either of the formats shown below, and the pROM's will be preprogrammed prior to shipment. In addition National distributors have programming capabilities available.

The table of programming electrical characteristics and Figure 3 give the conditions for the programming of the MM5204. In the programming mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A_0 through A_8, data inputs are B_0 through B_8 and write operation is controlled by pulsing the PROGRAM input. Since the pROM is initially programmed with all "0"'s a V_{ILP} on any data input B_0 through B_8 will leave the stored "0"'s undisturbed and a V_{IHP} on any data input B_0 through B_8 will write a logic "1" into that location.

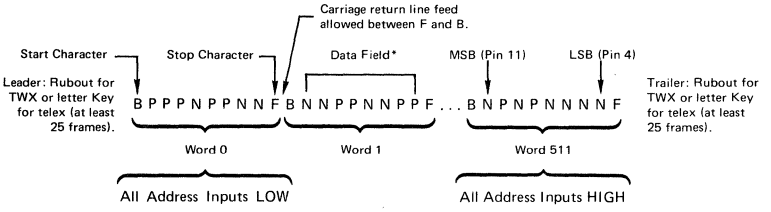
Table I describes the voltage conditions for operating the pROM in the read only mode and the program mode.

TABLE I.

MODE	POWER SAVER, DATA AND ADDRESS LINES		V_{SS}	V_{BB}	V_{DD}		PROGRAM		V_{LL}	CS
	LOGIC "1"	LOGIC "0"			−12V ±5%		5.0V ±5%			
					LOGIC "1"	LOGIC "0"	LOGIC "1"	LOGIC "0"		
Read Only	V_{IH}	V_{IL}	5.0V ±5%	5.0V ±5%					0V	V_{IL}
Program	V_{IHP}	V_{ILP}	0V	12V ±5%	V_{DHP}	V_{DLP}	V_{DHP}	V_{DLP}	0V to −14V	0V

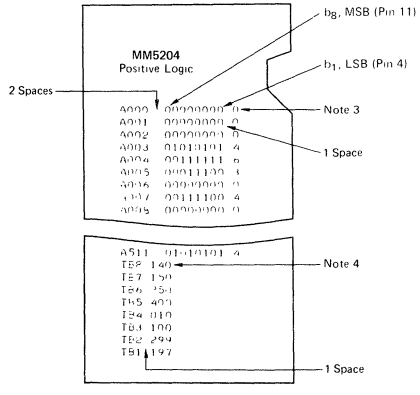
alternate format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered, beginning with word 0.

preferred format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

switching time waveforms

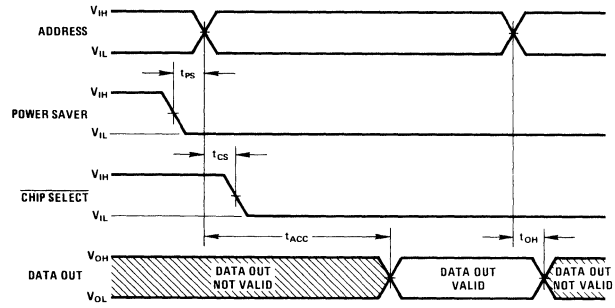


FIGURE 1. Access Time From Address to Data Out

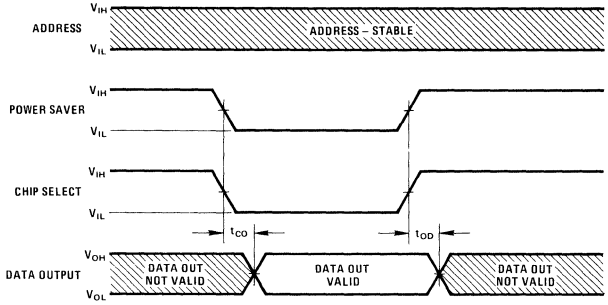


FIGURE 2. Access Time From Power Saver or Chip Select to Output

programming waveforms

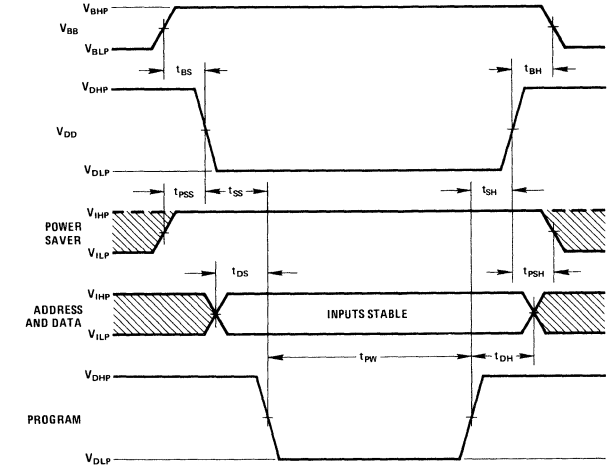


FIGURE 3. Programming Waveforms

PROMs/ROMs

MM4210/MM5210 1024-bit read only memory

general description

The MM4210/MM5210 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

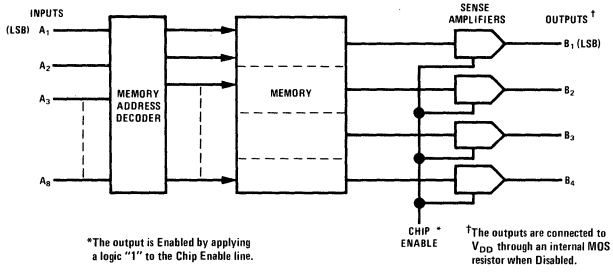
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

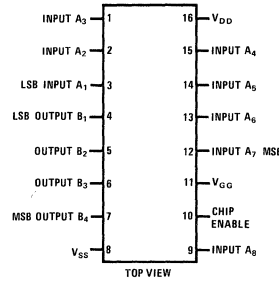
block and connection diagrams



*The output is Enabled by applying a logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

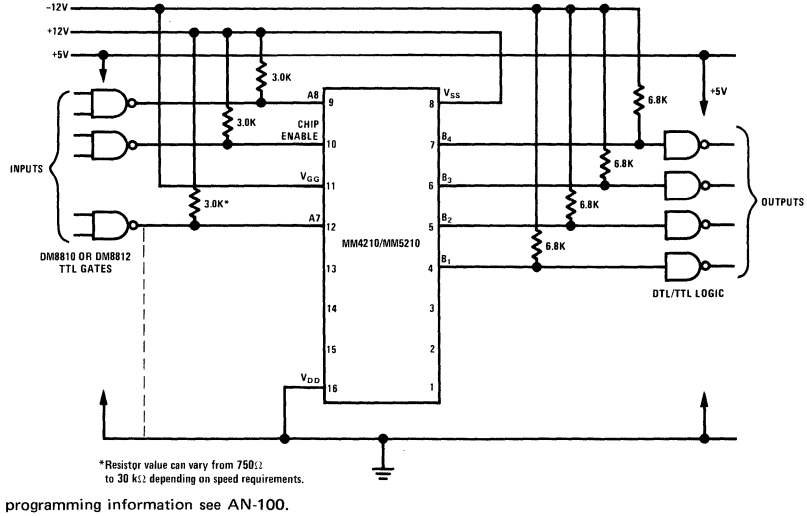
Dual-In-Line Package



Order Number MM4210J or MM5210J
See Package 10
Order Number MM5210N
See Package 15

typical application

256 x 4 Bit ROM Showing TTL Interface



*Resistor value can vary from 750Ω to 30 kΩ depending on speed requirements.

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		$V_{SS}-30V$
V_{DD} Supply Voltage		$V_{SS}-15V$
Input Voltage		$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)$
Storage Temperature		$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature	MM4210	$-55^{\circ}C$ to $+125^{\circ}C$
	MM5210	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 10 sec)		$300^{\circ}C$

electrical characteristics

T_A within operating temperature range, $V_{SS} = +12V \pm 5\%$ and $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load			$V_{SS}-9.0$	V
Logical "0"		$V_{SS}-1.0$			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				$V_{SS}-8.0$	V
Logical "0"		$V_{SS}-2.0$			V
Power Supply Current	$T_A = 25^{\circ}C$				
V_{SS}			19	25	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}-12V$			1	μA
Input Capacitance	f = 1.0 MHz $V_{IN} = 0V$		5		pF
Access Time (Notes 2, 3)	$T_A = 25^{\circ}C$				
T_{ACCESS}	(See Timing Diagram) $V_{SS} = +12V$ $V_{GG} = -12V$	150	500	650	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

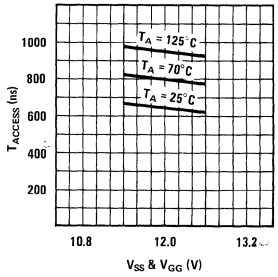
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

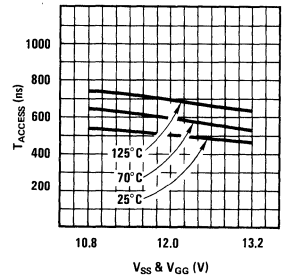
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

performance characteristics

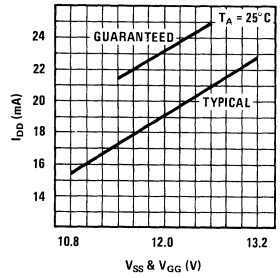
Guaranteed Access Time vs Supply Voltages



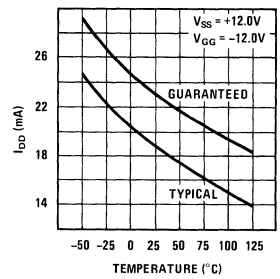
Typical Access Time vs Supply Voltages



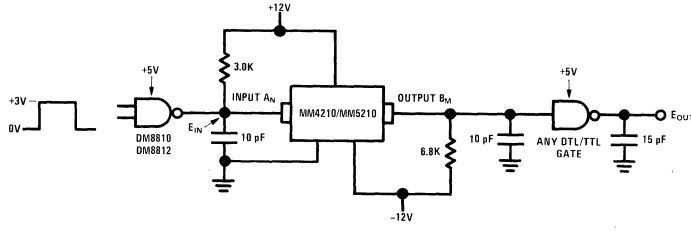
Power Supply Current vs Voltage

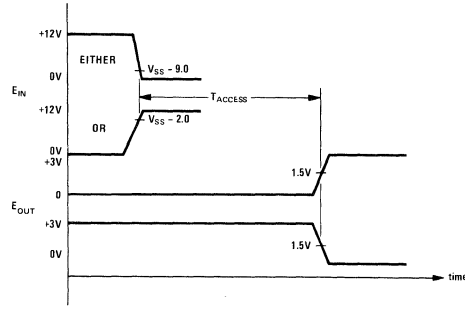


Power Supply Current vs Temperature



timing diagram/address time





PROMs/ROMs

MM4211/MM5211 1024-bit read only memory

general description

The MM4211/MM5211 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication.

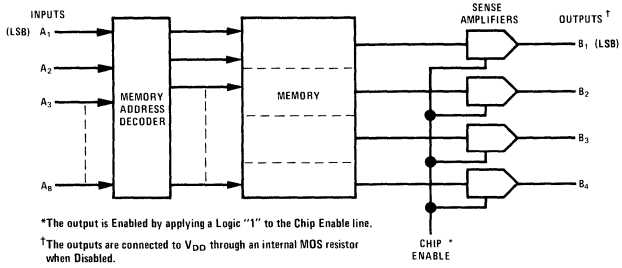
features

- Bipolar compatibility +5V, −12V operation
- High speed operation < 700 ns typ
- Static operation no clocks required
- Common data busing output wire AND capability
- Chip enable output control

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming

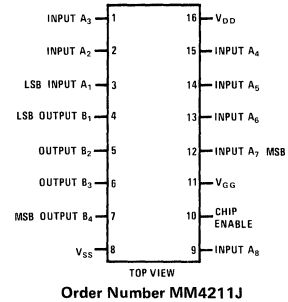
block and connection diagrams



*The output is Enabled by applying a Logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

Dual-In-Line Package

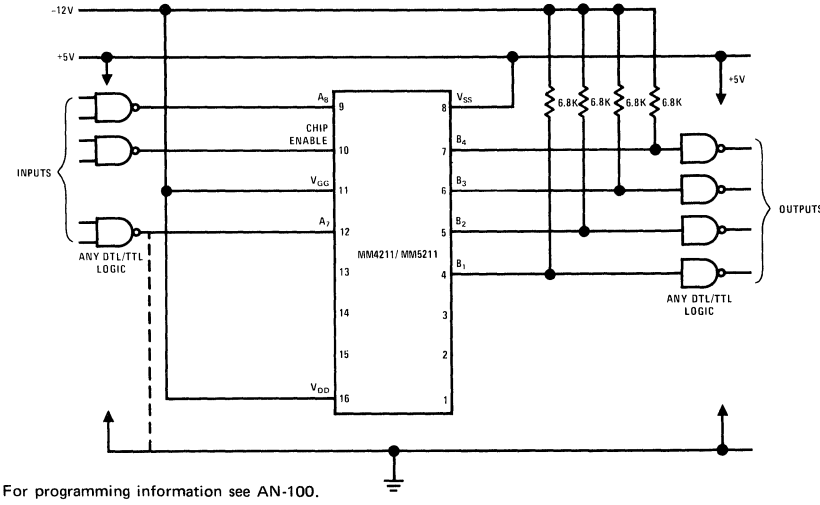


Order Number MM4211J or MM5211J
See Package 10

Order Number MM5211N
See Package 15

typical application

256 x 4 Bit ROM Showing TTL Interface



Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature	–65°C to +150°C
Operating Temperature MM4211	–55°C to +125°C
MM5211	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{GG} = V_{DD} = –12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8K ±5% to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		6.5	12.0	mA
I_{GG} (Note 1)	V_{GG} = V_{DD} = –12V			1	μA
Input Leakage	V_{IN} = V_{SS} – 12V			1	μA
Input Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		15	25	pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = 5V V_{GG} = V_{DD} = –12V		700	950	ns
Output AND Connection (Note 3)	6.8K ±5% to V_{GG} Plus One Standard Series 54/74 Gate			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

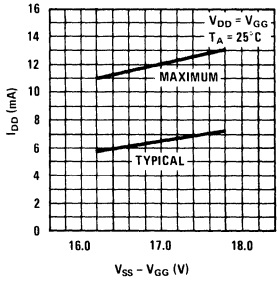
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 3: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N –1) (50) ns
Where N = Number of AND connections.

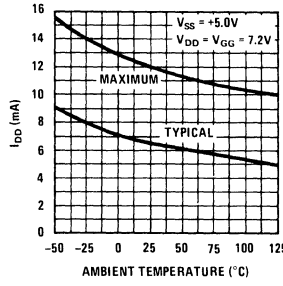
Note 4: Capacitance guaranteed by design.

performance characteristics

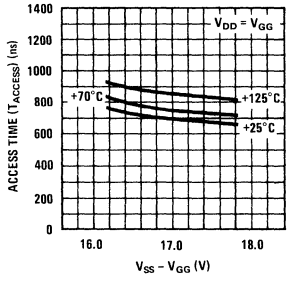
Power Supply Current vs
Power Supply Voltages



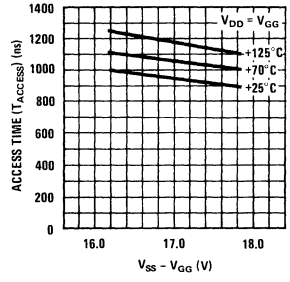
Power Supply Current vs
Ambient Temperature



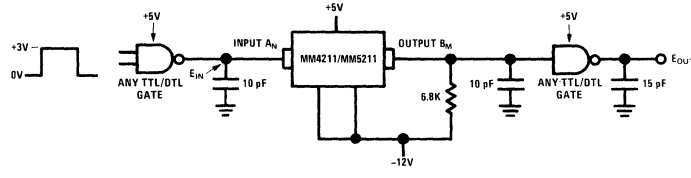
Typical Access Time vs
Power Supply Voltages

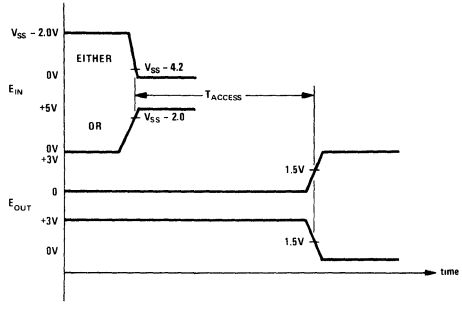


Guaranteed Access Time vs
Power Supply Voltages



timing diagram/address time





PROMs/ROMs

MM5212 12,288-bit read only memory

general description

The MM5212 12,288-bit read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology and ion-implanted resistors. Open drain outputs provide a TTL compatible wire OR capability with the addition of a 6.8 kΩ resistor. The ROM is organized in a 1024 word by 12-bit organization.

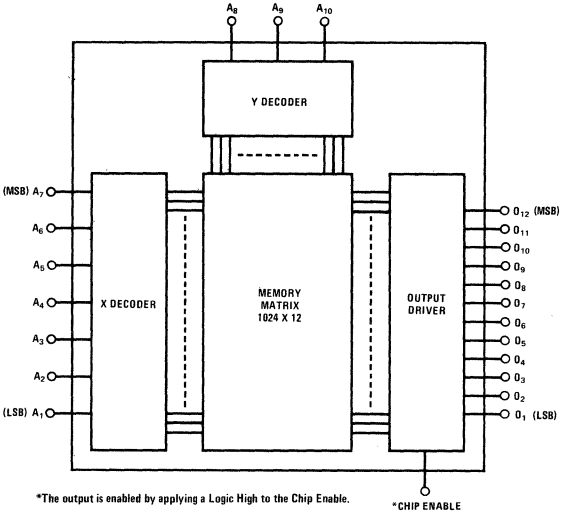
features

- Standard supplies +5.0V, −12V
- Open drain outputs Wire OR capability
- Static operation No clocks
- TTL compatible inputs and outputs

applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

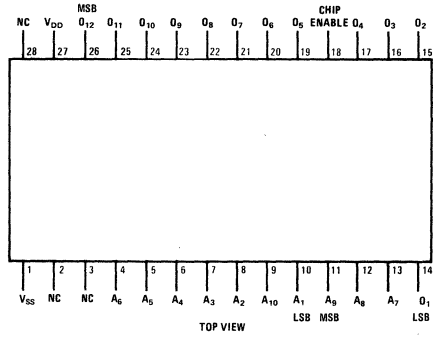
schematic diagram



*The output is enabled by applying a Logic High to the Chip Enable.

connection diagram

Dual-In-Line Package



Note: For programming information see AN-100.

Order Number MM5212AD
See Package 7

Order Number MM5212AN
See Package 19

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.5V to V_{SS} − 22V
Power Dissipation at 25°C Ambient	800 mW
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

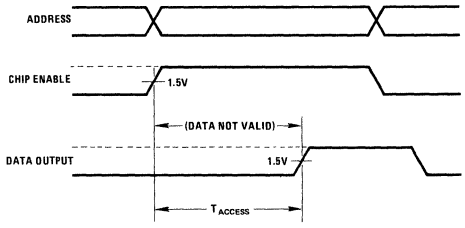
electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels (Note 1)					
Logical High Level (V_{IH})		+2.8			V
Logical Low Level (V_{IL})				+0.8	V
Data Output Levels (Note 1)					
Logical High Level (V_{OH})	6.8 kΩ ±5% to V_{DD} Plus One	+2.4			V
Logical Low Level (V_{OL})	Standard Series 54/74 Gate			+0.4	V
Output Current Capability					
Logical High Level (V_{IH})	V_{OUT} = 2.4V	2.5			mA
Power Supply Current	T_A = 25°C, V_{SS} = +5.0V				
I_{DD}	V_{DD} = −12V		6.0	10.0	mA
Standby Power Dissipation	V_{SS} = +5.0V, V_{DD} = −12V Chip Enable LOW			170.0	mW
Input Leakage	V_{IN} = V_{SS} −10V			1.0	μA
Address Time	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = +5.0V V_{DD} = −12V	.25	3.5	5.0	μs

Note 1: Positive logic definition.

switching time waveforms



PROMs/ROMs

MM4213/MM5213 2048-bit read only memory

general description

The MM4213/MM5213 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

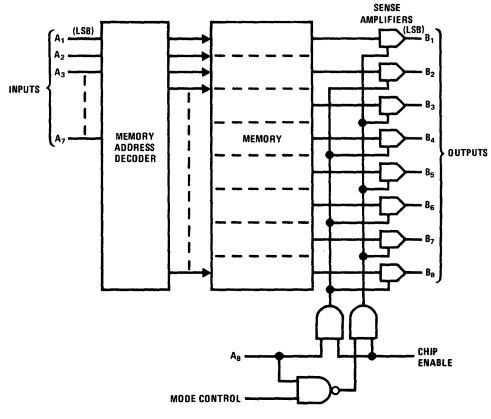
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 600 ns typ
- Pin compatible with MM5203 pROM
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control
- TRI-STATE output

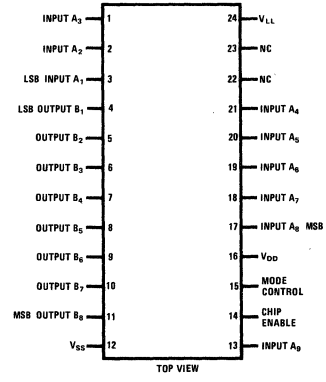
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

block and connection diagrams



Dual-In-Line Package



Order Number MM4213J or MM5213J
See Package 11
Order Number MM5213N
See Package 18

typical applications

FIGURE 1. Power Saver for Small Memory Arrays

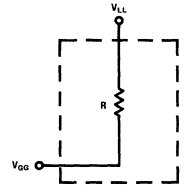
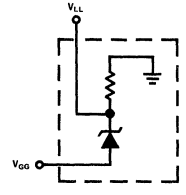


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME ||VLL ||MIN = ||−3V ||
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

Note: For programming information see AN-100.

absolute maximum ratings

V_{LL} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.3)\ V$
Storage Temperature	–65°C to +150°C
Operating Temperature MM4213	–55°C to +125°C
MM5213	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Capability					
Logical "1"	V_{OUT} = 2.4V	200			μA
Logical "0"	V_{OUT} = 0.4V	–1.6			mA
Input Voltage Levels					
Logical "0"				V_{SS} – 4.0	V
Logical "1"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{SS} (Note 2)	V_{SS} = +5V		20	35	mA
	$V_{LL} = V_{DD}$ = –12V				
Input Leakage	V_{IN} = –12V			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		5		pF
Address Time	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = +5.0V		600	850	ns
	$V_{GG} - V_{DD}$ = –12.0V				
Output AND Connections (Note 4)				10	

Note 1: These specifications apply for V_{SS} = +5.0V ±5%, V_{LL} = –12V, and T_A = –55°C to +125°C (MM4213), T_A = –25°C to +70°C (MM5213) unless otherwise specified.

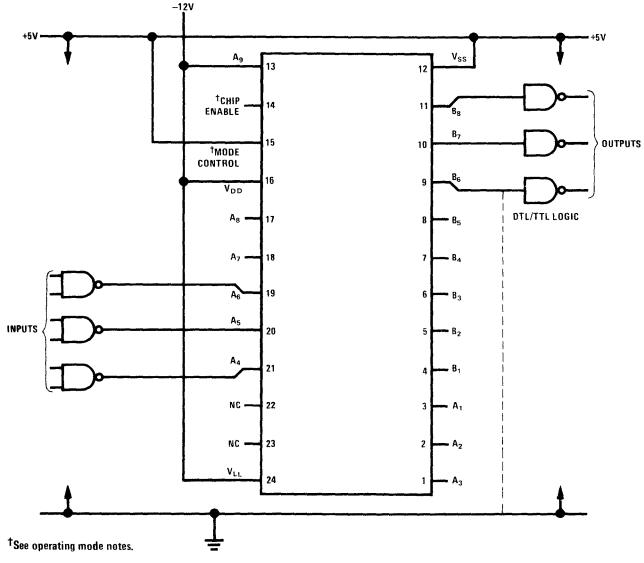
Note 2: Outputs open.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate.

Note 4: The address time in the TTL load configuration follows the equation: T_{ACCESS} = The specified limit + (N – 1) (25) ns. Where N = Number of AND connections.

Note 5: Capacitances are measured on a lot sample basis only.

typical applications (con't)



†See operating mode notes.

Operating Modes

256 x 8 ROM connection (shown)
Mode Control – Logic "0"
A_9 – Logic "1"

512 x 4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd ($B_1, B_3 \ldots B_9$) outputs
– Logic "1" Enables the even ($B_2, B_4 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

Logic levels are negative true MOS logic.

Mode Control should be "hard wired" to V_{LL} (Logical "1") or V_{SS} (Logical "0").

PROMs/ROMs

MM4214/MM5214 4096-bit static read only memory

general description

The MM4214/MM5214 4096-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit memory organization.

Customer programs may be submitted for production in a paper tape or punched card format.

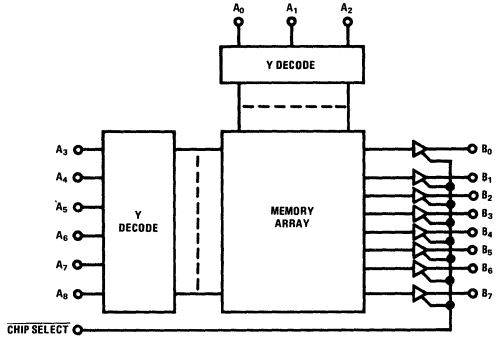
features

- Pin compatible with MM5204 PROM
- Bipolar compatibility — No external components required
- Standard supplies — +5.0V, −12V
- Bus ORable output — TRI-STATE outputs
- Static operation — No clocks required

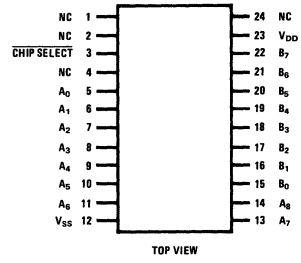
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



Dual-In-Line Package

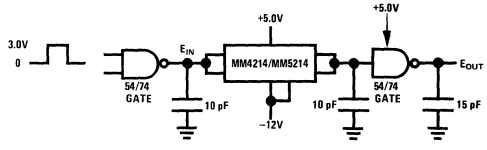


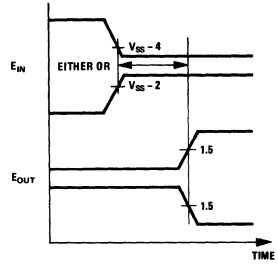
TOP VIEW

Order Number MM4214J or MM5214J
See Package 11

Order Number MM5214N
See Package 18

timing diagram/address time





Note: For programming information see AN-100.

absolute maximum ratings

V_{DD} Supply Voltage	V_{SS} − 20V	Operating Temperature Range	
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.03)\ V$	MM4214	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	MM5214	−25°C to +70°C
		Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical Low Level (V_{IL})	I_L = 1.6 mA Sink			0.4	V
Logical High Level (V_{IH})	I_L = 100μA Source	2.4			V
Input Voltage Levels					
Logical Low Level (V_L)				V_{SS}−4.0	V
Logical High Level (V_H)		V_{SS}−2.0			V
Power Supply Current (I_{SS}) (Note 4)	V_{SS} = 5.0V, V_{DD} = −12V, T_A = 25°C		23	37	mA
Input Leakage	$V_{IN} = V_{SS} - 10V$			1.0	μA
Input Capacitance (Note 2)	f = 1.0 MHz, V_{IN} = 0V		5.0	10	pF
Output Capacitance (Note 2)	f = 1.0 MHz, V_{IN} = 0V		4.0	10	pF
Address Time (T_{ACCESS}) (Note 1)	V_{DD} = −12V, V_{SS} = 5.0V, T_A = 25°C	150		1000	ns
Output AND Connections (Note 3)				20	

Note 1: Capacitances are measured periodically only.

Note 2: Address is measured from the change of data on any input or chip enable line to the output of a TTL gate. (See Timing Diagram.)

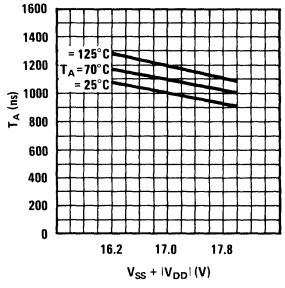
Note 3: The address time follows the following equation: T_{ACCESS} = The specified limit + (N−1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

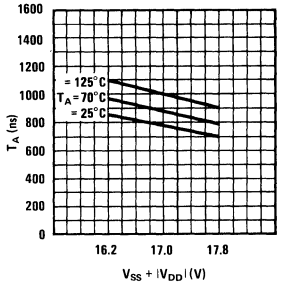
Note 5: Positive true logic notation is used. Logic "1" = most positive voltage level. Logic "0" = most negative voltage level.

typical performance characteristics

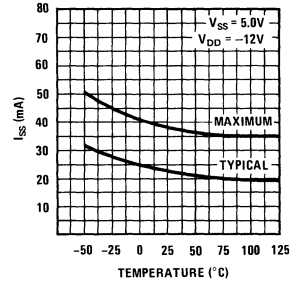
Guaranteed Access Time vs Supply Voltage



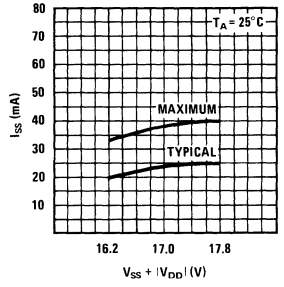
Typical Access Time vs Supply Voltage



Power Supply Current vs Temperature



Power Supply Current vs Voltage



PROMs/ROMs

MM5215 12,288-bit read only memory

general description

The MM5215 12,288-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology and ion-implanted resistors. TRI-STATE® outputs provide wire-OR capability without loading common data lines or reducing system access times. The ROM is organized in a 1024 x 12 bit word configuration. The V_{GG} supply may be brought to 0V to reduce internal power dissipation in the non-enabled mode to 10μW/bit.

Customer programs may be submitted on Hollerith coded punched cards.

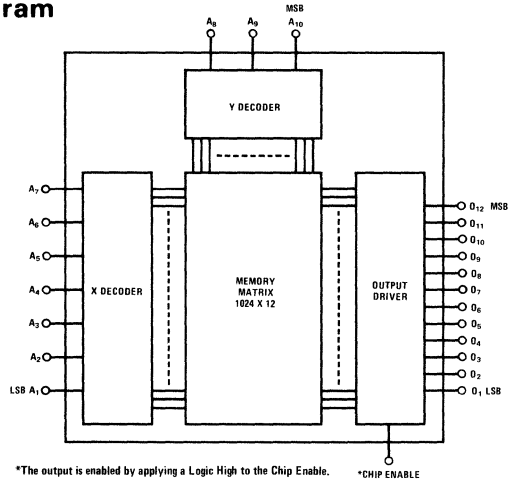
features

- Static operation
- TRI-STATE outputs
- No clocks required
- +12V and −12V supplies
- Pin compatible with E.A. 3800

applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

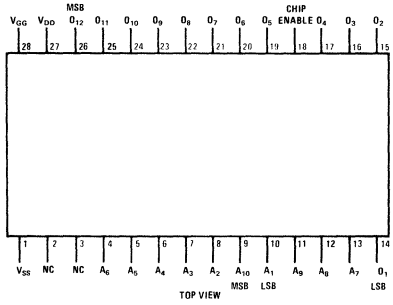
schematic diagram



*The output is enabled by applying a Logic High to the Chip Enable.

connection diagram

Dual-In-Line Package



Note: For programming information see AN-100.

Order Number MM5215AD
See Package 7

Order Number MM5215AN
See Package 19

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} +0.5V to V_{SS} −30V
Input Voltage	V_{SS} +0 5V to V_{SS} −30V
Power Dissipation at 25°C Ambient	800 mW
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

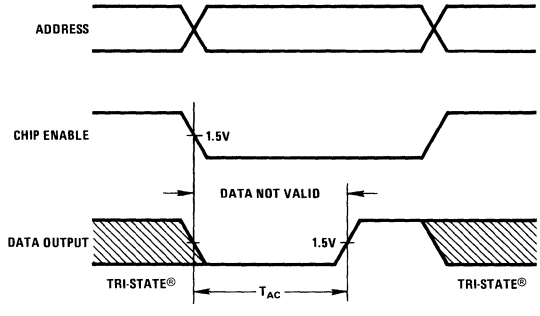
electrical characteristics

T_A within operating temperature range V_{SS} = +12V ±1.0V, V_{DD} = 0V, V_{GG} = −12V ±1.0V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Levels					
Logical "1"	(Note 1)			V_{SS} − 9.0	V
Logical "0"	(Note 1)	V_{SS} − 2.0			V
Output Voltage Levels					
Logical "1"	No Load			V_{DD}	V
Logical "0"	No Load	V_{SS}			V
Output Current					
Logical "1"	V_O = V_{SS}	2.5			mA
	V_O = V_{SS} − 6.0V	0.7			mA
Logical "0"	V_O = V_{SS} − 12V	−2.0			mA
	V_O = V_{SS} − 6.0V	−1.5			mA
Power Supply Current					
I_{SS}	V_{SS} = +13V, V_{DD} = 0V, V_{GG} = −13V			30	mA
I_{GG}	V_{SS} = +13V, V_{DD} = 0V, V_{GG} = −13V			15	mA
Standby Power Dissipation	V_{SS} = +12V, V_{DD} = 0V V_{GG} = 0V, T_A = 25°C			150	mW
	V_{SS} = +12V, V_{DD} = 0V V_{GG} = −12V, T_A = 25°C			300	mW
Address Time					
T_{ACCESS}	T_A = 25°C			3.0	μs

Note 1: Positive logic definition.

switching time waveforms



PROMs/ROMs

MM4220/MM5220 1024-bit read only memory

general description

The MM4220/MM5220 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

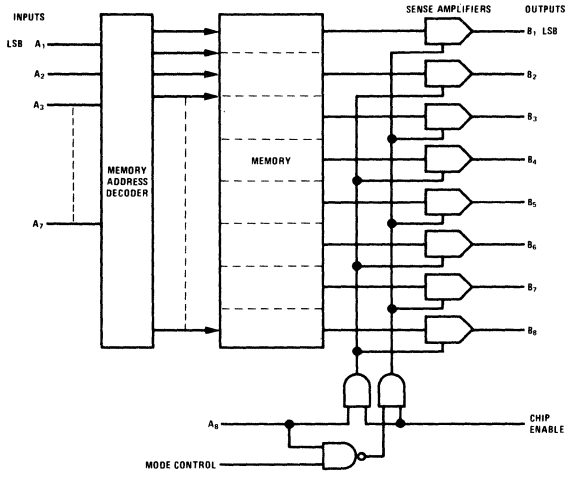
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

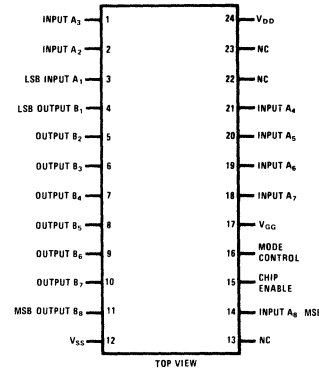
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming

block and connection diagrams



Dual-In-Line Package



Order Number MM4220J
or MM5220J
See Package 11

Order Number MM5220N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage	$V_{SS}-30V$
V_{DD} Supply Voltage	$V_{SS}-15V$
Input Voltage	$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)V$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature MM4220	$-55^{\circ}C$ to $+125^{\circ}C$
MM5220	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

electrical characteristics

T_A within operating temperature range, $V_{SS} = +12V \pm 5\%$ and $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			$V_{SS}-9.0$	V
Logical "0"		$V_{SS}-1.0$			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				$V_{SS}-8.0$	V
Logical "0"		$V_{SS}-2.0$			V
Power Supply Current	$T_A = 25^{\circ}C$				
V_{SS}			19	25	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}-12V$			1	μA
Input Capacitance	f = 1.0 MHz $V_{IN} = 0V$		5		pF
Access Time (Notes 2, 3)	$T_A = 25^{\circ}C$				
T_{ACCESS}	(See Timing Diagram) $V_{SS} = +12V$ $V_{GG} = -12V$	150	500	650	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

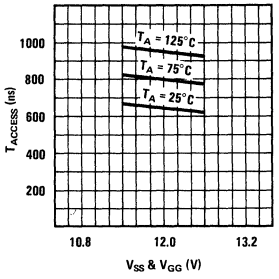
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

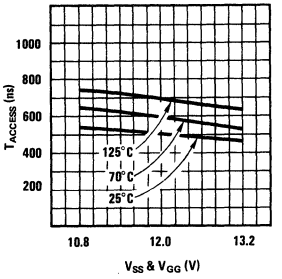
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

performance characteristics

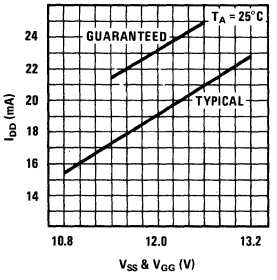
Guaranteed Access Time vs Supply Voltages



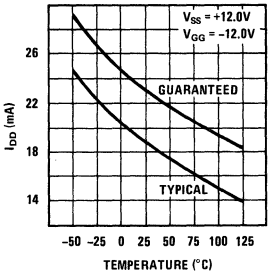
Typical Access Time vs Supply Voltages



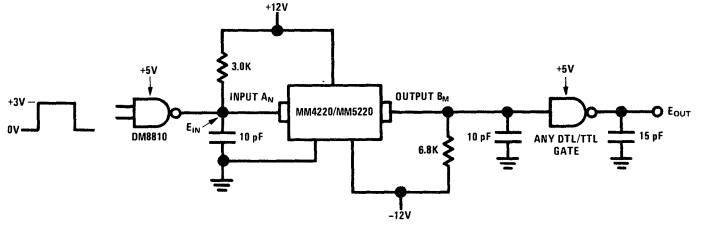
Power Supply Current vs Voltage

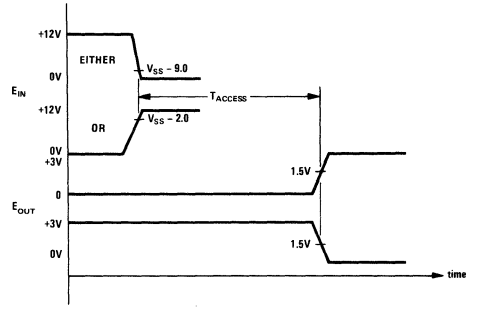


Power Supply Current vs Temperature



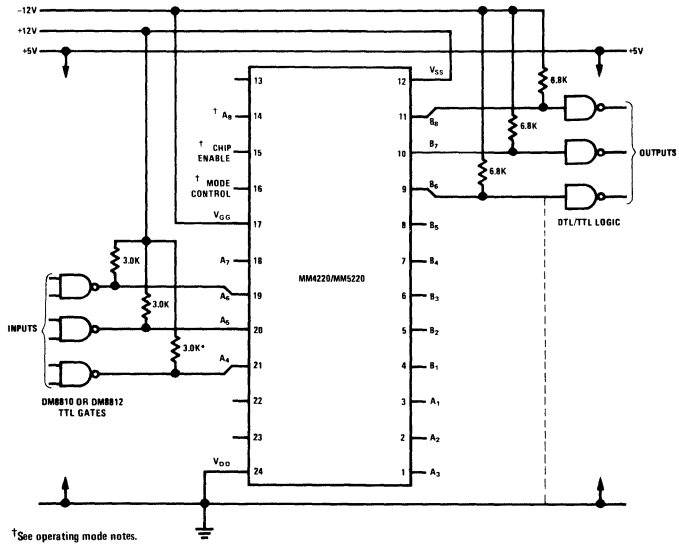
timing diagram/address time





typical application

128-8 Bit ROM Showing TTL Interface



†See operating mode notes.

*R values can vary from 740 to 30 kΩ depending on speed requirements.

OPERATING MODES

128x8 ROM connection
Mode Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Mode Control – Logic "1"
A_8 – Logic "0" Enables the odd ($B_1 \ldots B_7$) outputs
– Logic "1" Enables the even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

The logic levels are in negative voltage logic notation.

PROMs/ROMs

MM4221/MM5221 1024-bit read only memory

general description

The MM4221/MM5221 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

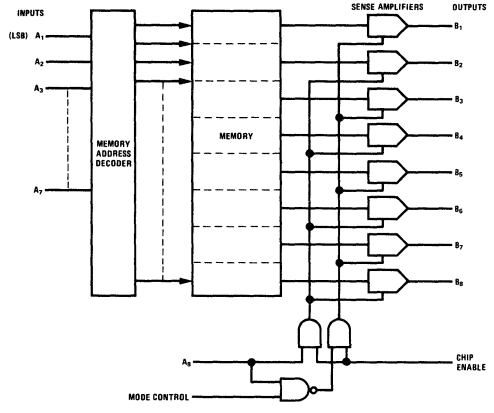
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — <700 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control

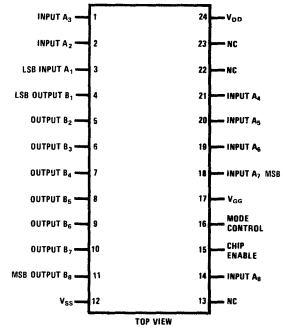
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

block and connection diagrams



Dual-In-Line Package



Order Number MM4221J or MM5221J
See Package 11
Order Number MM5221N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature	–65°C to +150°C
Operating Temperature MM4221	–55°C to +125°C
MM5221	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, $V_{GG} = V_{DD}$ = –12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		6.5	12.0	mA
I_{GG} (Note 1)	$V_{GG} = V_{DD}$ = –12V			1	μA
Input Leakage	$V_{IN} = V_{SS}$ – 12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		15	25	pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = 5V $V_{GG} = V_{DD}$ = –12V		700	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{GG} Plus One Standard Series 54/74 Gate			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

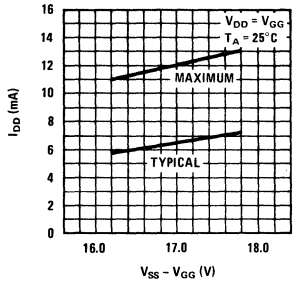
Note 2: Address time is measured from the change of data on any input except mode control or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 3: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns
Where N = Number of AND connections.

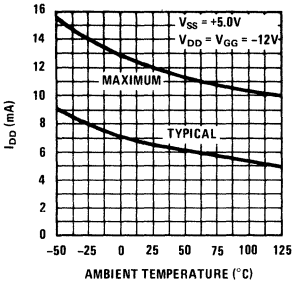
Note 4: Capacitance guaranteed by design.

performance characteristics

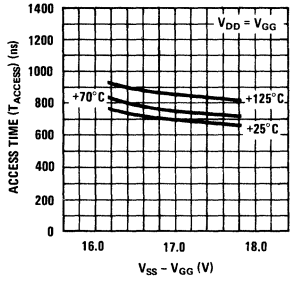
Power Supply Current vs
Power Supply Voltages



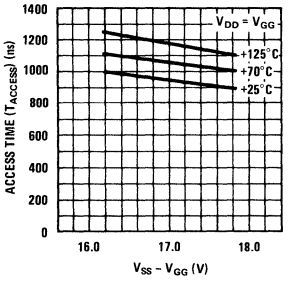
Power Supply Current vs
Ambient Temperature



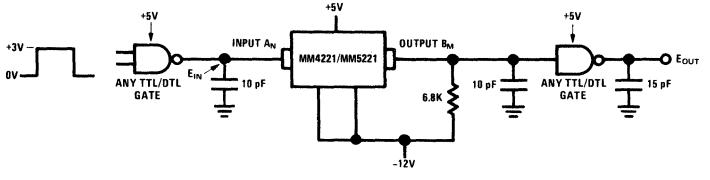
Typical Access Time vs
Power Supply Voltages

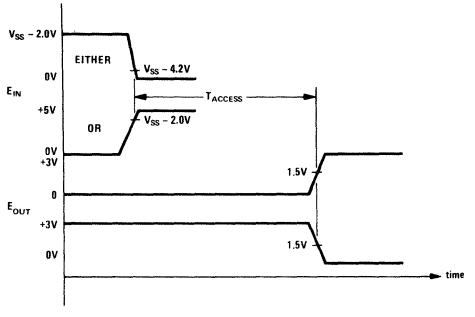


Guaranteed Access Time vs
Power Supply Voltages



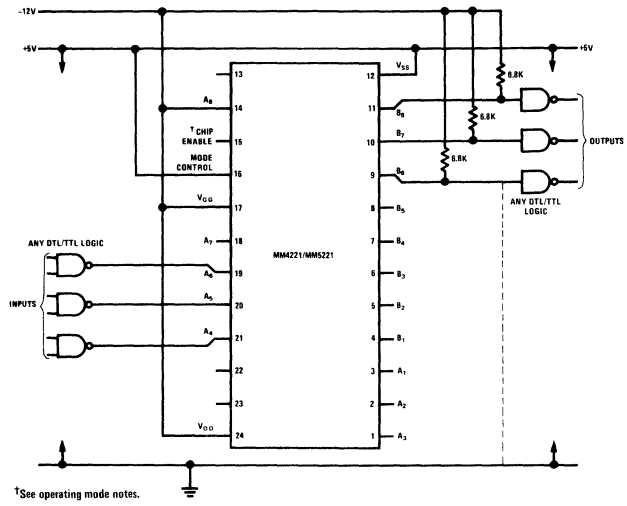
timing diagram/address time





typical application

128-8 Bit ROM Showing TTL Interface



OPERATING MODES

128x8 ROM connection
Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Control – Logic "1"
A_8 – Enables the odd ($B_1 \ldots B_7$) or even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to ground through an internal MOS resistor when "Disabled."

Logic levels are negative true MOS logic.

Mode control should be "hard wired" to either V_{DD} (logical "1") or V_{SS} (logical "0").

The logic levels are in negative voltage logic notation.

PROMs/ROMs

MM4229/MM5229 3072-bit read only memory (open drain)

general description

The MM4229/MM5229 is a 3072-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized in a 256 x 12 bit word configuration.

Customer programs may be supplied on Hollerith coded punched cards.

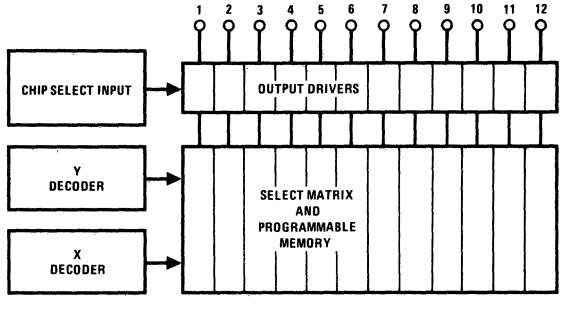
features

- TTL compatible
- Low standby power
- Programmable chip select inputs
- Typical 1.0μs access time
- Open drain outputs allow wire-OR of up to 8 devices

applications

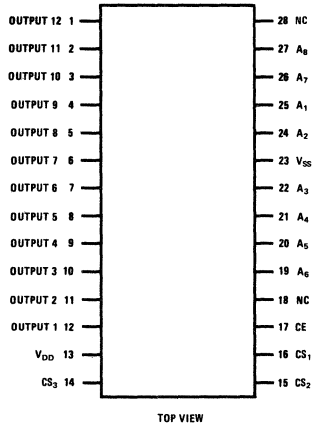
- Code conversion
- Random logic synthesis
- Table look-up
- Microprogramming

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Note: For programming information see AN-100.

Order Number MM4229D or MM5229D
See Package 7

Order Number MM5229N
See Package 19

absolute maximum ratings

All Inputs or Outputs with Respect to the Most Positive Voltage V_{SS} (Substrate)	+0.3V to −20V
Supply Voltage V_{DD} and V_D with Respect to V_{SS} (Substrate)	+3.0V to −20V
Operating Temperature Range	
MM4229	−55°C to +125°C
MM5229	−25°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

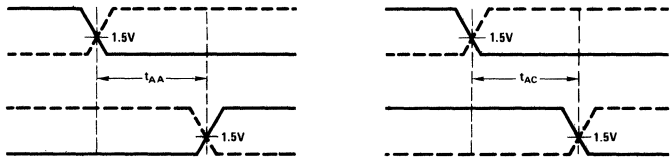
T_A within operating temperature range, V_{DD} = −12V ±10%, V_{SS} = +5V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})	V_{SS} = +4.75V	+2.4			V
Logical Low Level (V_{IL})	V_{SS} = +4.75V			+0.8	V
Data Output Levels					
Logical High Level (V_{OH})	6.8 kΩ ±5% to V_{DD} Plus One	+2.4			V
Logical Low Level (V_{OL})	Standard Series 54/74 Gate			+0.4	V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Data Input Leakage (I_{RI})	$V_{IN} - V_{SS}$ = −5V			2.0	μA
Data Output Leakage (I_{RO})	$V_{OUT} - V_{SS}$ = −5V (Note 1)			2.0	μA
Data Input Capacitance (C_{IN})	$V_{IN} - V_{SS}$ = 0V			5.0	pF
Data Output Capacitance (C_{OUT})	$V_{OUT} - V_{SS}$ = 0V			8.0	pF
Access Time (T_A)					
Address Response (t_{AA})	C_L = 20 pF		1.0	1.4	μs
C Inhibit Response (t_{AC})	C_L = 20 pF		0.8	1.2	μs
Active Power Supply					
V_{DD} Supply (I_{DD})	V_{SS} = +5V, V_1 = 0V		25	32	mA
V_{SS} Supply (I_{SS})	V_{DD} = 12V, T_A = 25°C		25	32	mA
Data Input Currents					
Logical High Level (I_{IH})	$V_{IN} - V_{SS}$ = −2.4V			2.0	μA
Logical Low Level (I_{IL})	$V_{IN} - V_{SS}$ = 5V			2.0	μA
Standby Power Supply					
I_{DD}	V_{SS} = +5V, V_1 = 0V		12	18	mA
I_{SS}	V_{DD} = −12V, T_A = 25°C		12	18	mA

Note 1: Chip inhibited or de-selected.

Note 2: The above logic levels are indicated in negative logic notation.

switching time waveforms



Definitions:

Access Time: Represents the total propagation delay through input translation decode for memory selection and output sense amplification of the memory signal and is measured from the last input transition through 1.5V to the last output transition through 1.5V.

Chip Enable: The output source and sink transistors are turned off in the chip inhibit and chip de-select mode to allow OR-tieing of output for easy memory expansion.

Chip Select: The outputs are enabled and data from the selected memory location will appear at the outputs. The chip select and chip enable inputs are programmable for decoderless word expansion.

PROMs/ROMs

MM4230/MM5230 2048-bit read only memory

general description

The MM4230/MM5230 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

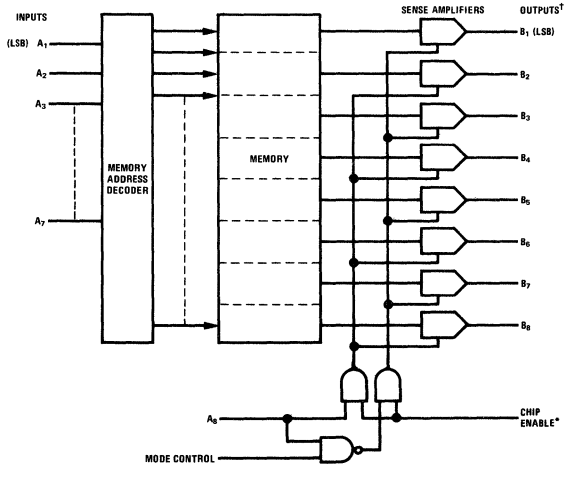
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

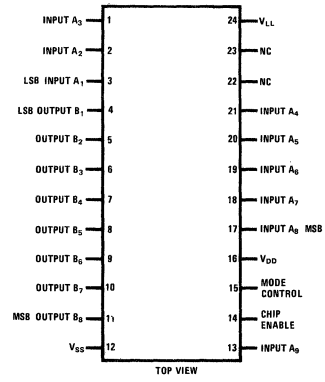
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

block and connection diagrams



Dual-In-Line Package



Order Number MM4230J
or MM5230J
See Package 11
Order Number MM5230N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		$V_{SS}-30V$
V_{DD} Supply Voltage		$V_{SS}-15V$
Input Voltage		$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)V$
Storage Temperature		$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature	MM4230	$-55^{\circ}C$ to $+125^{\circ}C$
	MM5230	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 10 sec)		$300^{\circ}C$

electrical characteristics

T_A within operating temperature range, V_{SS} = +12V ±5% and V_{GG} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			V_{SS} −9.0	V
Logical "0"		V_{SS} −1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} −8.0	V
Logical "0"		V_{SS} −2.0			V
Power Supply Current	$T_A = 25^{\circ}C$				
V_{SS}			24	40	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}$ −12V			1	μA
Input Capacitance	f = 1.0 MHz V_{IN} = 0V		5		pF
Access Time (Notes 2, 3)	$T_A = 25^{\circ}C$				
T_{ACCESS}	(See Timing Diagram) V_{SS} = +12V V_{GG} = −12V	150	500	725	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

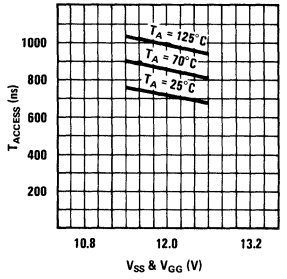
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

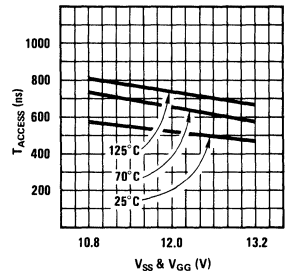
Note 4: The above logic levels are indicated in negative logic notation.

performance characteristics

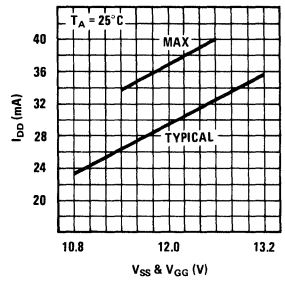
Guaranteed Access Time vs Supply Voltages



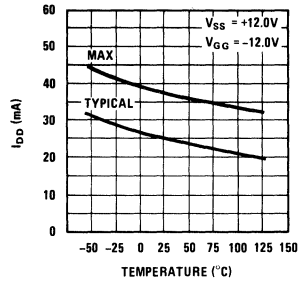
Typical Access Time vs Supply Voltages



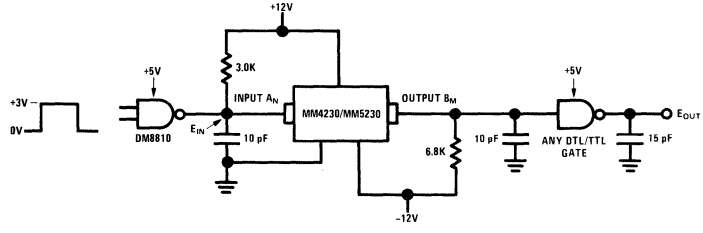
Power Supply Current vs Voltages

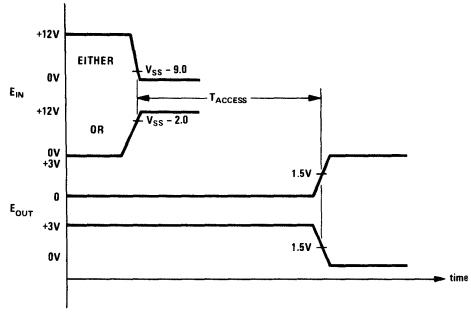


Power Supply Current vs Temperature



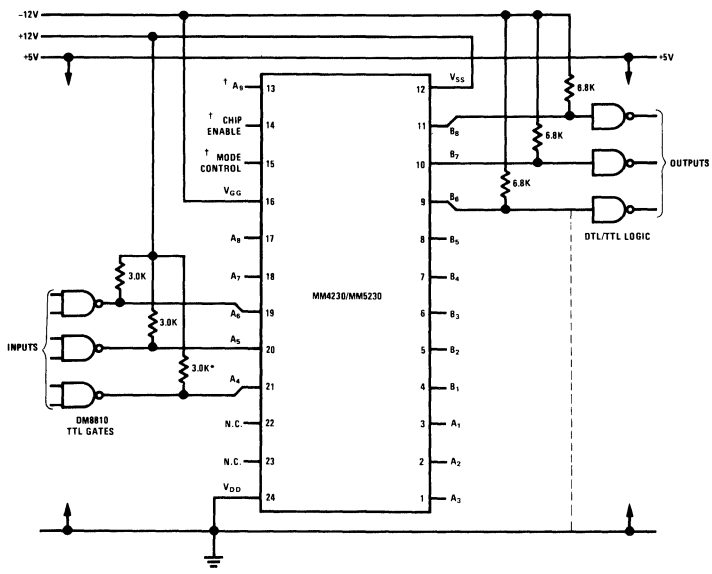
timing diagram/address time





typical application

256 x 8 Bit ROM Showing TTL Interface



†See operating mode notes.
*R values can vary from 740Ω to 30 kΩ.

OPERATING MODES

128x8 ROM connection
Mode Control – Logic "0"
A_9 – Logic "1"

256x4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd ($B_1 \ldots B_7$) outputs
– Logic "1" Enables the even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

The logic levels are in negative voltage logic notation.

PROMs/ROMs

MM4231/MM5231 2048-bit read only memory

general description

The MM4231/MM5231 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

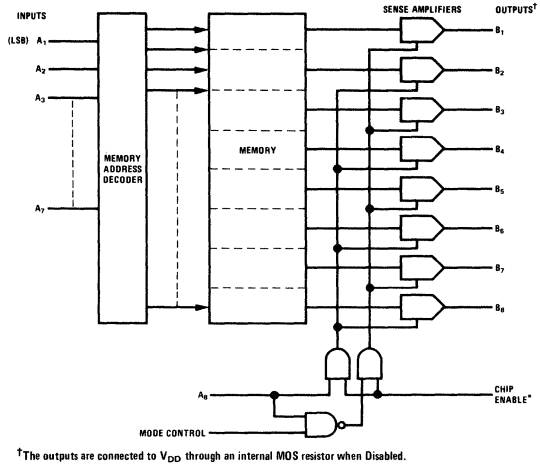
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 640 ns typ.
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

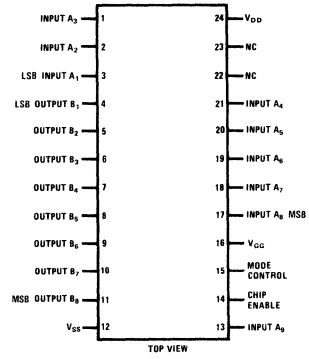
block and connection diagrams



†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

*The output is enabled by applying a Logic "1" to the Chip Enable line.

Dual-In-Line Package



Order Number MM4231J or MM5231J
See Package 11

Order Number MM5231N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{DD} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		−65°C to +150°C
Operating Temperature	MM4231	−55°C to +125°C
	MM5231	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{DD} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		15	30	mA
I_{GG} (Note 1)	$V_{GG} = V_{DD}$ = −12V			1	μA
Input Leakage	V_{IN} = −12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance	f = 1.0 MHz, V_{IN} = 0V		15		pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C V_{SS} = +5.0V $V_{GG} = V_{DD}$ = −12.0V		640	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{DD} Plus One Standard Series 54/74 Gate			8	

Note 1: These specifications apply for V_{SS} = +5V ±5%, $V_{GG} = V_{DD}$ = −12V, ±5%, and T_A = −55°C to +125°C (MM4231), T_A = −25°C to +70°C (MM5231) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

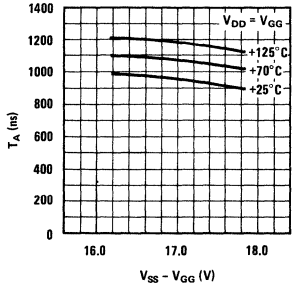
Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns.
Where N = Number of AND connections.

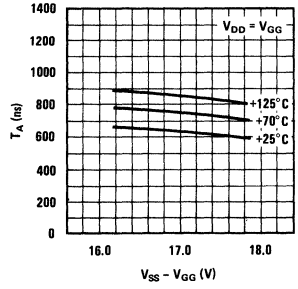
Note 5: Capacitances are measured on a lot sample basis only.

performance characteristics

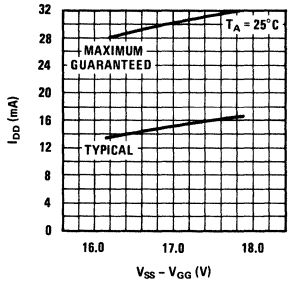
Guaranteed Access Time (T_A) vs Power Supply Voltage



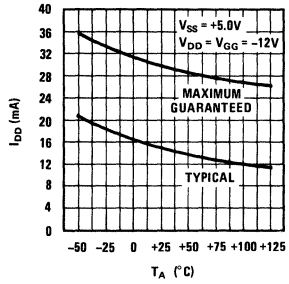
Typical Access Time (T_A) vs Power Supply Voltage



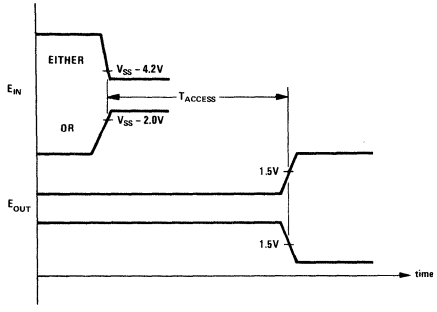
Power Supply Current vs Power Supply Voltage

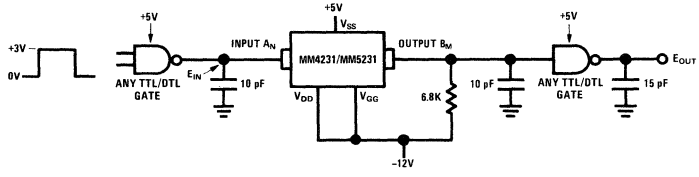


Power Supply Current vs Ambient Temperature



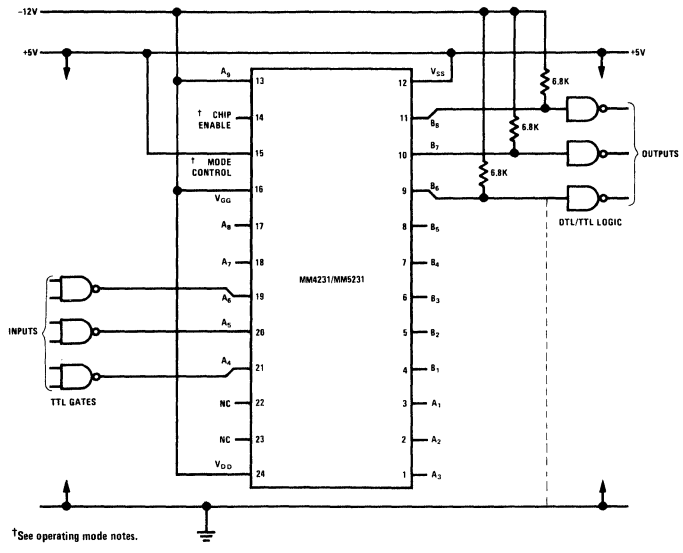
timing diagram/address time





typical application

256 x 8 Bit ROM Showing TTL Interface



Operating Modes

256 x 8 ROM connection (shown)
Mode Control – Logic "0"
A_9 – Logic "1"

512 x 4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd (B_1, B_3 . . . B_9) outputs
– Logic "1" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

Logic levels are negative true MOS logic.

Mode Control should be "hard wired" to V_{DD} (Logical "1") or V_{SS} (Logical "0").

The logic levels are in negative voltage logic notation.

PROMs/ROMs

MM4232/MM5232 4096-bit static read-only memory

general description

The MM4232/MM5232 4096-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit or 1024 word x 4-bit memory organization that is controlled by the mode control input. Programmable Chip Enables (CE_1 and CE_2) provide logic control of up to 16K bits without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

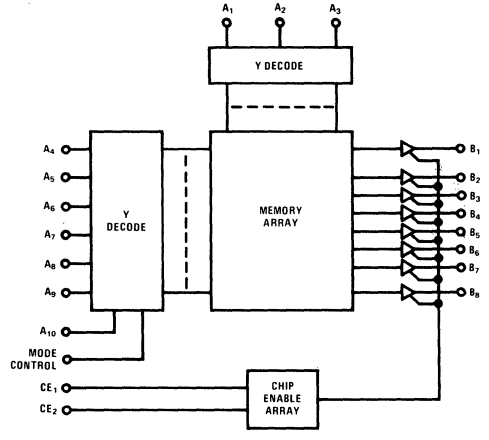
features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two-programmable Chip Enable lines

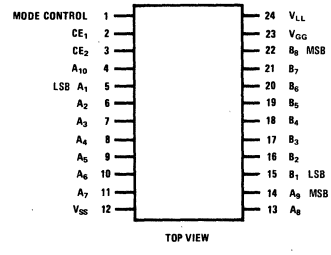
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



Dual-In-Line Package



Order Number MM4232J or MM5232J
See Package 11
Order Number MM5232N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{LL} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range		–65°C to +150°C
Operating Temperature Range	MM4232	–55°C to +125°C
	MM5232	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics POSITIVE LOGIC

T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{GG} = V_{DD}$ = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical "0", V_{OL}	I_L = 1.6 mA Sink			.4	V
Logical "1", V_{OH}	I_L = 100 μA Source	2.4			V
Input Voltage Levels					
Logical "0", V_{IL}		V_{GG}		V_{SS} – 4.0	V
Logical "1", V_{IH}		V_{SS} – 2.0		V_{SS} + 0.3	V
Power Supply Current					
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −12, T_A = 25°C		23	37	mA
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −3, T_A = 125°C		12	20	mA
Input Leakage	$V_{IN} = V_{SS}$ – 10V			1	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	15	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2)	T_A = 25°C, V_{SS} = 5	150		1000	ns
T_{ACCESS}	$V_{GG} = V_{LL}$ = −12V				
Output AND Connections (Note 3)				20	

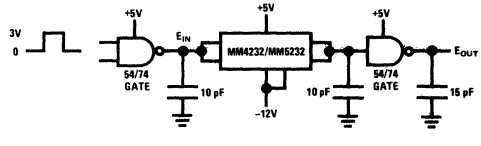
Note 1: Capacitances are measured periodically only.

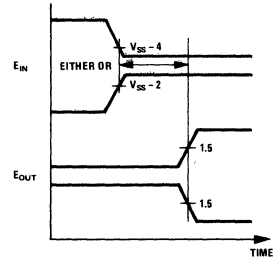
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

Note 3: The address time follows the following equation: T_{ACCESS} = the specified limit + (N – 1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

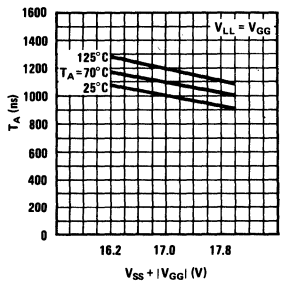
timing diagram/address time



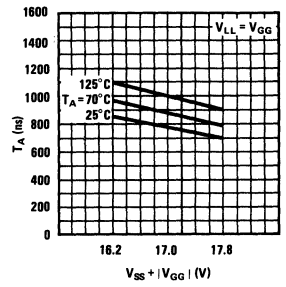


performance characteristics

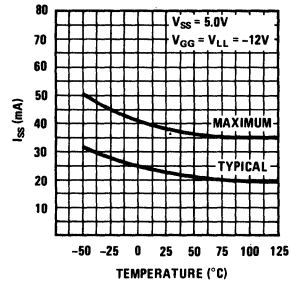
Guaranteed Access Time vs Supply Voltage



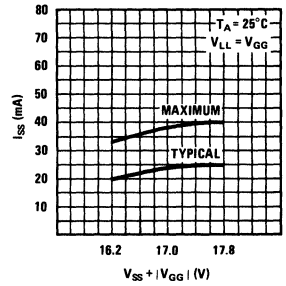
Typical Access Time vs Supply Voltage



Power Supply Current vs Temperature

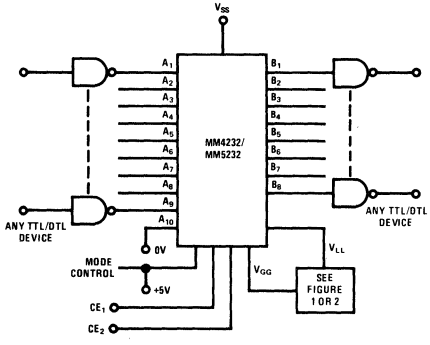


Power Supply Current vs Voltage



typical applications

TTL/MOS Interface

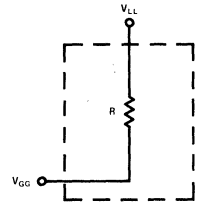


Operating Modes

512 x 8 ROM connection
Mode Control = V_{IH}
$A_{10} = V_{IL}$

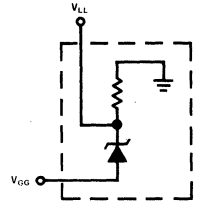
1024 x 4 ROM connection
Mode Control = V_{IL}
$A_{10} = V_{IL}$ enables the odd ($B_1 \ldots B_7$) outputs
V_{IH} enables the even ($B_2 \ldots B_8$) outputs

FIGURE 1. Power Saver for Small Memory Arrays



ASSUME $|V_{LL}|_{MIN} = |-3V|$
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

FIGURE 2. Power Saver for Large Memory Arrays



Note: Both chip enables may be programmed to provide any of four combinations. Example if CE_1 = 1 and CE_2 = 1 outputs (Positive Logic) would be enabled only when device pins 2 and 3 are Logic "1". The outputs will be in the third state when disabled.

PROMs/ROMs

MM4233/MM5233 4096-bit read only memory

general description

The MM4233/MM5233 4096-bit static read only memory is a monolithic MOS integrated circuit utilizing P-channel ion-implanted enhancement mode low threshold technology to achieve bipolar compatibility. The ROM is organized in a 512 word x 8-bit format.

Four programmable chip selects provide logic control of the TRI-STATE® outputs, allowing wire OR capability of up to 16 ROM's without loading common data lines or reducing systems access times. A separate output supply lead V_{DD} is provided to reduce internal power dissipation in the output stages.

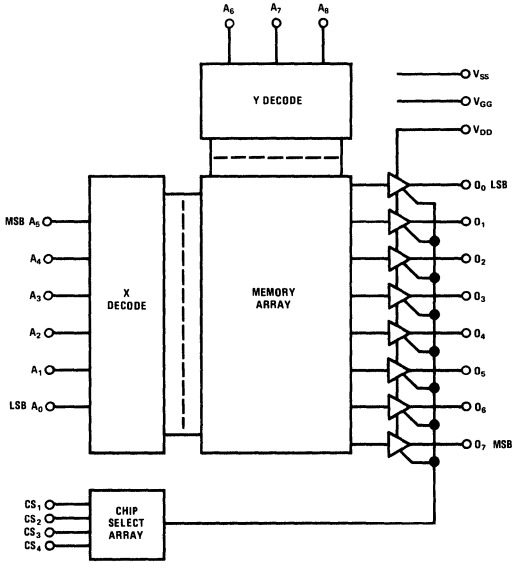
features

- Pin for pin compatible with the Fairchild 3514
- Bipolar compatible — No external components required
- Standard supplies — +5.0V, −12V
- TRI-STATE outputs — Bus ORable outputs
- Static operation — No clocks required
- Multiple ROM control — Four programmable chip select lines

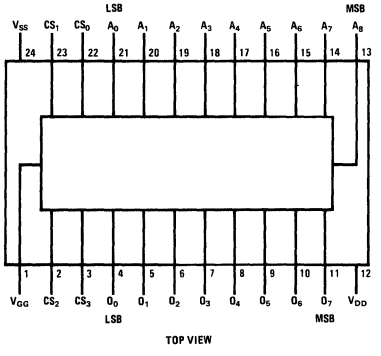
applications

- Code conversion
- Microprogramming
- Control logic
- Table look-up

logic and connection diagrams



Dual-In-Line Package



Order Number MM4233J or MM5233J
See Package 11

Order Number MM5233N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.5V to V_{SS} − 20 V
Power Dissipation at 25°C Ambient	0.8W
Operating Temperature	
MM4233	−55°C to +125°C
MM5233	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

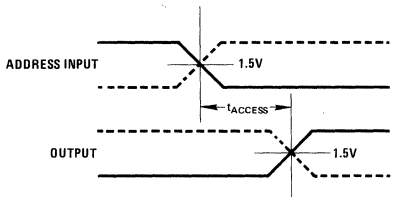
electrical characteristics

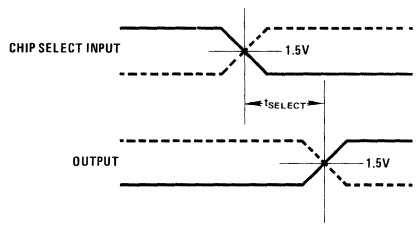
V_{SS} = +5.0V ±5%, V_{DD} = 0V, V_{GG} = −12V ±5%, T_A = −55°C to +125°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical Low	I_L = 2.4 mA Sink			0.4	V
Logical High	I_L = 0.5 mA Source	2.4			V
Input Voltage Levels					
Logical Low				V_{SS} − 4.0	V
Logical High		V_{SS} − 1.0			V
Power Supply Current	T_A = 25°C				
I_{SS}	(Note 1)		21	30	mA
I_{DD}				1.0	mA
I_{GG}			21	30	mA
Input Leakage	V_{IN} = V_{SS} −10V			1.0	μA
Input Capacitance (Note 2)	f = 1 MHz, V_{IN} = V_{SS}			5.0	pF
Output Capacitance (Note 2)	f = 1 MHz, V_{OUT} = V_{SS}			9.0	pF
Address Time	T_A = 25°C				
T_{ACCESS}	(Note 3 and Note 4)			1000	ns
Select Time	T_A = 25°C				
T_{SELECT}	(Note 3 and Note 4)			800	ns

Note 1: Outputs open.
Note 2: Capacitances are measured periodically only.
Note 3: See timing diagram.
Note 4: 1.5 TTL load, C_L = 20 pF.

switching time waveforms





PROMs/ROMs

MM4240/MM5240 2560-bit static character generator

general description

The MM4240/MM5240 2560-bit static character generator is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology. Six character address and three row address input lines provide access to 64–8 x 5 characters. Customer-generated single or multiple package character fonts are easily programmed by completing a pattern selection form. A standard 7 x 5 raster scan font is available by ordering the MM4240AA/MM5240AA.

The MM4240/MM5240 may be used as a 512 x 5-bit read only memory for applications other than character generation.

features

- Bipolar compatibility
- High speed operation—500 ns max
- ±12 volt power supplies
- Static operation—no clocks required
- Multiple ROM logic application—chip enable output control
- Standard fonts available—off-the-shelf delivery

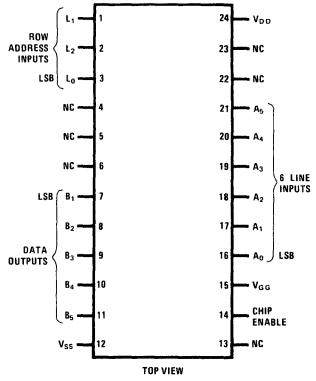
applications

- Character generation
- Random logic synthesis
- Microprogramming
- Table look-up

3

connection diagram

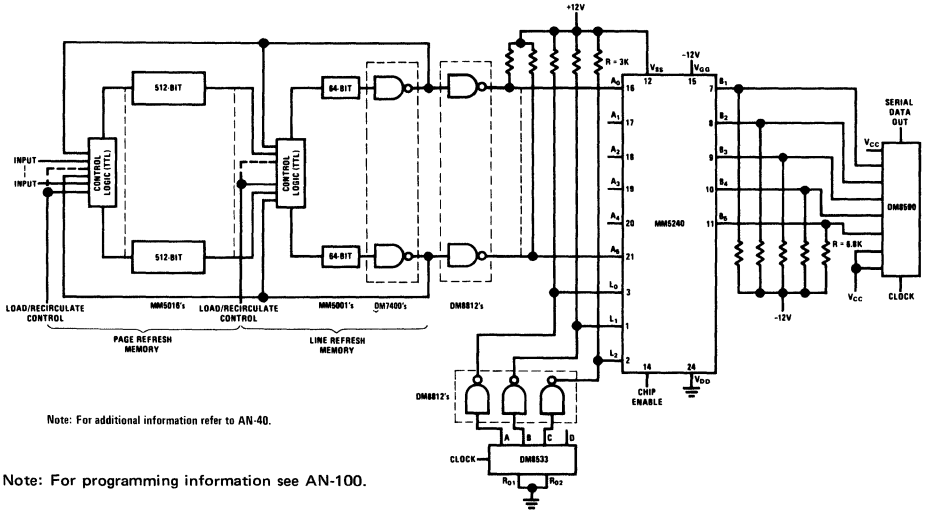
Dual-In-Line Package



TOP VIEW

Order Number MM4240J
or MM5240J
See Package 11
Order Number MM5240N
See Package 18

typical application



Note: For additional information refer to AN-40.

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 30V
V_{DD} Supply Voltage		V_{SS} – 15V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		–65°C to +150°C
Operating Temperature	MM4240	–55°C to +125°C
	MM5240	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	IMΩ to GND			V_{SS} – 9.0	V
Logical "0"		V_{SS} – 1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.5			V
Output Current Capability					
Logical "0"	$V_{OUT} = V_{SS} - 6.0V$	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 8.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	$T_A = 25°C$				
I_{DD}	MOS Load		25	40	mA
I_{GG} (Note 2)				1	μA
Input Leakage	$V_{IN} = V_{SS} - 12V$			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		5	8	pF
V_{GG} Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		25	40	pF
Address Time (Note 3)	See Timing Diagram				
T_{ACCESS}	$T_A = 25°C$	150	425	500	ns
Output AND Connection	MOS Load			4	
(Note 4)	TTL Load			10	

Note 1: These specifications apply for V_{SS} = +12V ±5%, V_{GG} = –12V ±5%, and T_A = –55°C to +125°C (MM4240) T_A = 0°C to +70°C (MM5240) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns

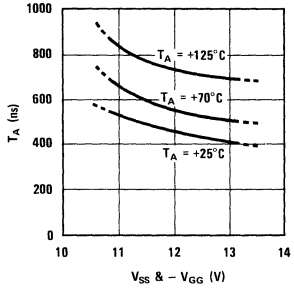
Where N = Number of AND connections.

The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

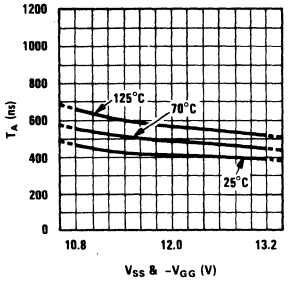
Note 5: Guaranteed by design.

performance characteristics

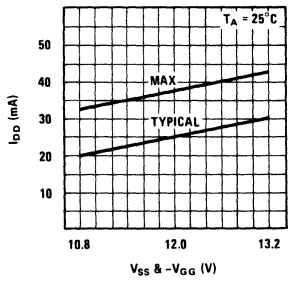
Guaranteed Access Time (T_A) vs Supply Voltage



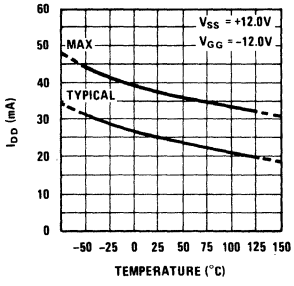
Typical Access Time (T_A) vs Supply Voltage



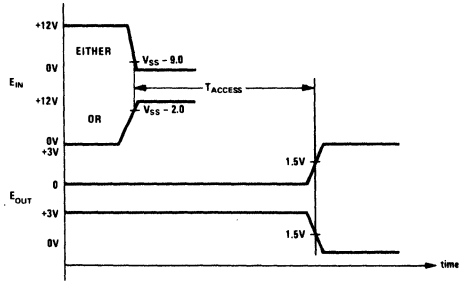
Power Supply Current vs Voltage

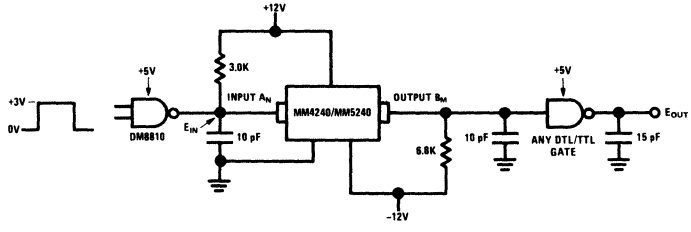


V_{DD} Power Supply Current vs Temperature

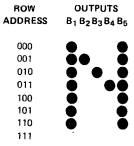


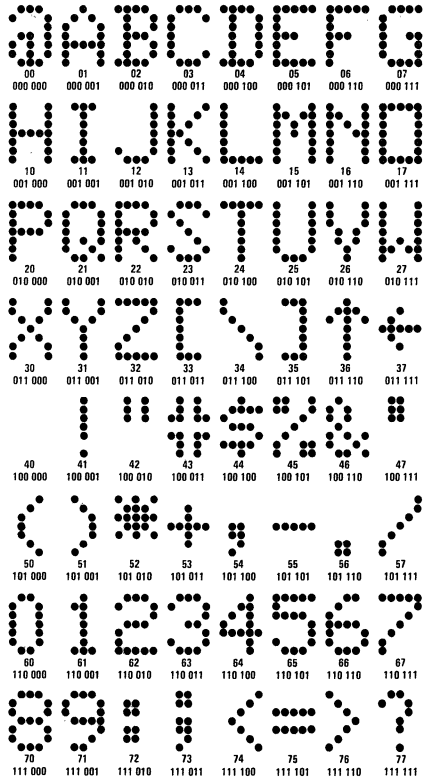
timing diagram/address time





MM4240AA/MM5240AA character font





PROMs/ROMs

MM4241/MM5241 3072-bit static read-only memory

general description

The MM4241/MM5241 3072-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 64 x 6 word by 8-bit memory organization. Programmable Chip Enables (CE_1 and CE_2) provide logic control of multiple packages without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

features

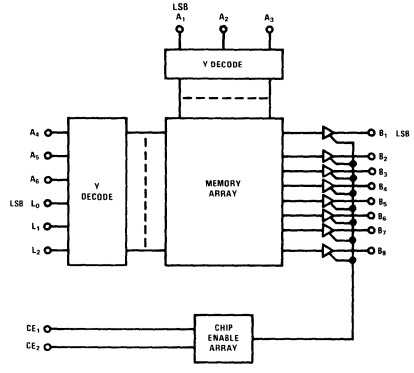
■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two programmable Chip Enable lines

applications

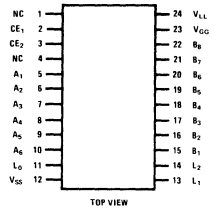
- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

3

logic and connection diagrams



Dual-In-Line Package



Order Number MM4241J
or MM5241J
See Package 11
Order Number MM5241N
See Package 18

typical applications

TTL/MOS Interface

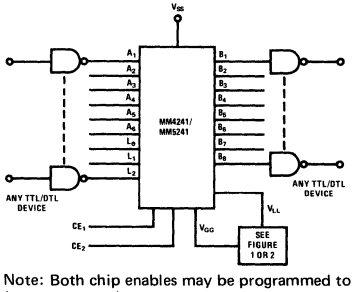


FIGURE 1. Power Saver for Small Memory Arrays

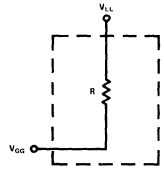
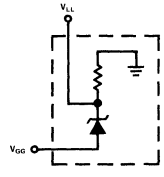


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME ||VLL ||MIN = ||−3V ||
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

Note: Both chip enables may be programmed to provide any of four combinations. Example: If $CE_1 = 1$ and $CE_2 = 1$ outputs (Negative Logic) would be enabled only when device pins 2 and 3 are negative (Logic "1"). The outputs will be in the third state when disabled. L_0, L_1 and L_2 (device pins 11, 13 and 14) are in positive logic (1 = most positive voltage levels = $V_S - 2V$; 0 = most negative voltage level = $V_{SS} - 4V$).

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{LL} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	MM4241	−55°C to +125°C
	MM5241	−25°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics NEGATIVE LOGIC (Note 5)

T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{GG} = V_{DD}$ = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical "1"	I_L = 1.6 mA sink			.4	V
Logical "0"	I_L = 100 μA source	2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} – 4.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current					
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −12, T_A = 25°C		23	37	mA
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −3, T_A = 125°C			20	mA
Input Leakage	$V_{IN} = V_{SS}$ – 10V			1	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	15	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2) T_{ACCESS}	T_A = 25°C, V_{SS} = 5 $V_{GG} = V_{LL}$ = −12V	150	700	900	ns
Output AND Connections (Note 3)				20	

Note 1: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 2: Capacitances are measured periodically only.

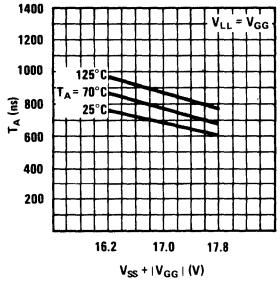
Note 3:. The address time follows the following equation: T_{ACCESS} = the specified limit + (N – 1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

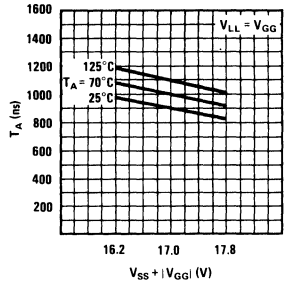
Note 5: All addresses and outputs are in negative true logic with the exception of L_0, L_1, and L_2 which are in positive logic.

performance characteristics

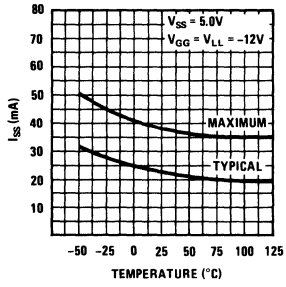
Typical Access Time vs Supply Voltage



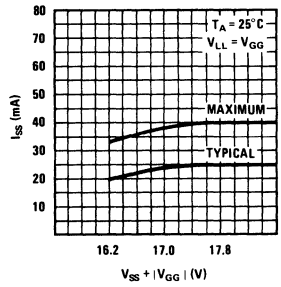
Guaranteed Access Time vs Supply Voltage



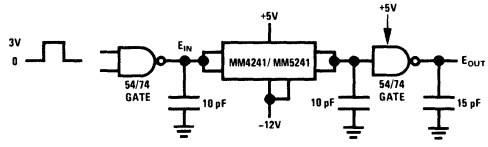
Power Supply Current vs Temperature

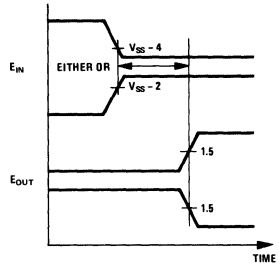


Power Supply Current vs Voltage



timing diagram/address time





MM1101/MM11011/MM1101A/MM1101A1/MM1101A2, MM4250
256-bit fully decoded static random access memory

general description

The MM1101 family of fully decoded 256 word x 1-bit random access memories are monolithic MOS integrated circuits using silicon gate low threshold technology to achieve bipolar compatibility. They are static, require no clocks, and hold information indefinitely, subject to the integrity of the power supply voltages.

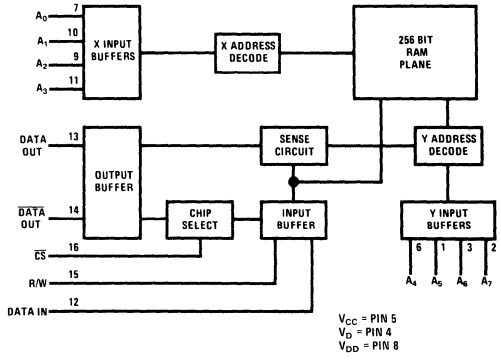
features

- Fast access times MM1101A2 500 ns max
  MM11011, MM1101A1 1.0 μs max
  MM1101, MM1101A 1.5 μs max
  MM4250 650 ns max
- Improved speed/power product MM1101A2 1/3 of 1101A
- Low power operation 1.5 mW/bit
- Fewer system components - bipolar compatible input and output
- Second source flexibility - MM1101, MM1101A MM11011, MM1101A1 second sources available
- TRI-STATE™ output - wired OR capability
- Specified ambient temperature 0°C to +70°C, for MM1101 family; −55°C to +125°C for MM4250

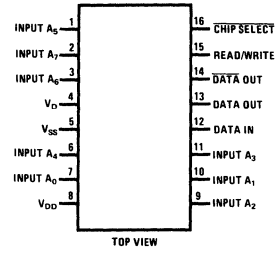
applications

- High speed buffer memories
- Local memory store

block and connection diagrams



Dual-In-Line Package



Order Number MM1101D, MM1101AD, MM1101A1D, MM1101A2D, MM11011D or MM4250D
See Package 3

Order Number MM1101N, MM1101AN, MM1101A1N, MM1101A2N or MM11011N
See Package 15

absolute maximum ratings

All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{SS}	+0.3V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{SS}	−16V
Power Dissipation at Room Temperature	700 mW
Operating Temperature	
MM1101 Family	0°C to +70°C ambient
MM4250	−55°C to +125°C ambient
Storage Temperature	−66°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

dc characteristics

T_A = 0°C to +70°C for MM1101 Family, T_A = −55°C to +125°C for MM4250;
V_{SS} = +5V ±5%, V_D = V_{DD} = −9V ±5% for MM4250, MM1101A, MM1101A1, MM1101A2;
V_{SS} = +5V ±5%, V_D = −10V ±5%, V_{DD} = −7V ±5%, for MM1101, MM11011 (unless otherwise specified).

SYMBOL	TEST	CONDITIONS	MM1101 FAMILY MIN	MM1101 FAMILY TYP	MM1101 FAMILY MAX	MM4250 MIN	MM4250 TYP	MM4250 MAX	UNITS
I_{LI}	Input Load Current (All Input Pins)	V_{IN} = 0.0		0.001	0.5			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0.0V, CS = V_{SS} − 2.0V		0.001	0.5			1.0	µA
MM4250 I_{DD}	Power Supply Current, V_{DD}	T_A = 25°C, Continuous Operation		13.0	19.0		13.0	19.0	mA
MM1101A I_{DD}	Power Supply Current, V_{DD}	T_A = 0°C, Continuous Operation			25.0			25.0	mA
MM1101A1 I_D	Power Supply Current, V_D	T_A = 25°C, I_{DL} = 0.0 mA		12.0	18.0		12.0	18.0	mA
MM1101A2 I_D	Power Supply Current, V_D	T_A = 0°C			24.0			24.0	mA
V_{IL}	Input LOW Voltage		V_{SS} − 10		V_{SS} − 4.2	V_{SS} − 10		V_{SS} − 4.2	V
V_{IH}	Input HIGH Voltage		V_{SS} − 2.0		V_{SS} + 0.3	V_{SS} − 2.0		V_{SS} + 0.3	V
I_{OL}	Output Sink Current	V_{OUT} = +0.45V, T_A = 25°C	3.0	8.0		3.0	8.0		mA
I_{OL}	Output Sink Current	V_{OUT} = +0.45V, T_A = 70°C	2.0			2.0			mA
I_{CF}	Output Clamp Current	V_{OUT} = −1.0V, T_A = 0°C		6.0	13.0		6.0	13.0	mA
I_{OH}	Output Source Current	V_{OUT} = 0.0V, T_A = +25°C	−3.0	−8.0		−3.0	−8.0		mA
I_{OH}	Output Source Current	V_{OUT} = 0.0V, T_A = +70°C	−2.0	−7.0		−2.0	−7.0		mA
V_{OH}	Output HIGH Voltage	I_{OH} = −100 µA	3.5	4.9		3.5	4.9		V
C_{IN}	Input Capacitance (Note 3) (All Input Pins)	V_{IN} = V_{SS}, f = 1 MHz		7.0	10.0		7.0	10.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = V_{SS}, f = 1 MHz		7.0	10.0		7.0	10.0	pF
C_V	V_D Power Supply Capacitance	V_D = V_{SS}, f = 1 MHz		20.0	35.0		20.0	35.0	pF
MM1101 I_{DD}	Power Supply Current, V_{DD}	T_A = 25°C, Continuous Operation		14.0	18.0				mA
MM11011 I_D	Power Supply Current, V_D	T_A = 25°C, I_{OL} = 0.0 mA		17.0	20.0				mA

ac characteristics

T_A = 0°C to +70°C for MM1101 Family, T_A = −55°C to +125°C for MM4250;
V_{SS} = +5V ±5%, V_D = V_{DD} = −9V ±5% for MM4250, MM1101A, MM1101A1, MM1101A2;
V_{SS} = +5V ±5%, V_D = −10V ±5%, V_{DD} = −7V ±5%, for MM1101, MM11011 (unless otherwise specified).

SYMBOL	TEST	MIN	TYP (Note 2)	MAX	UNITS
t_{rc}	Read Cycle MM1101, MM1101A	1.5			µs
	MM11011, MM1101A1	1.0			µs
	MM1101A2	500.0			ns
	MM4250	650.0			ns
t_{ac}	Address to Chip Select Delay				
	MM1101, MM1101A,			1.2 (Note 4)	µs
	MM11011, MM1101A1			0.7 (Note 4)	µs
	MM1101A			0.2 (Note 4)	µs
	MM4250			0.35 (Note 4)	µs
t_a	Access Time MM1101, MM1101A		0.85	1.5	µs
	MM11011, MM1101A1		0.65	1.0	µs
	MM1101A2		400.0	500.0	ns
	MM4250		400.0	650.0	ns
t_{oh}	Previous Read Data Valid	50.0			ns

Note 1: All voltage measurements are referenced to ground.
Note 2: Typical values are at T_A = +25°C and nominal supply voltages.
Note 3: Capacitances are measured periodically only.
Note 4: Maximum value for t_{ac} measured at minimum read cycle.

ac characteristics (con't)

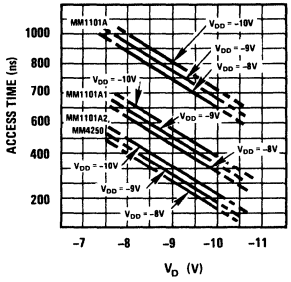
WRITE CYCLE (MM1101, MM11011, MM1101A, MM1101A1, MM1101A2)

SYMBOL	TEST	MIN	TYP (Note 2)	MAX	UNITS
t_{WC}	Write Cycle	0.8			μs
t_{WD}	Address to Write Pulse Delay	0.3			μs
t_{WP}	Write Pulse Width	0.4			μs
t_{DW}	Data Set up Time	0.3			μs
t_{DH}	Data Hold Time	0.1			μs
WRITE CYCLE (MM4250)					
t_{wc}	Write Cycle	1.0			μs
t_{wd}	Address to Write Pulse Delay	0.35			μs
t_{wp}	Write Pulse Width	0.50			μs
t_{dw}	Data Set-up Time	0.35			μs
t_{dh}	Data Hold Time	0.15			μs
CHIP SELECT AND DESELECT (MM1101, MM11011, MM1101A, MM1101A1, MM1101A2, MM4250)					
t_{CW}	Chip Select Pulse Width	0.4			μs
t_{CS}	Access Time Through Chip Select Input		0.2	0.3	μs
t_{CD}	Chip Deselect Time		0.1	0.3	μs

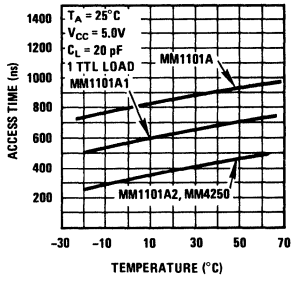
Note 1: All voltage measurements are referenced to ground.
Note 2: Typical values are at T_A = +25°C and nominal supply voltages.
Note 3: Capacitances are measured periodically only.
Note 4: Maximum value for t_{ac} measured at minimum read cycle.

typical performance characteristics

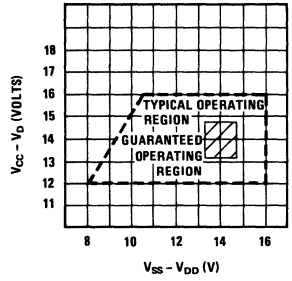
Typical Access Time vs Voltage



Typical Access Time vs Temperature

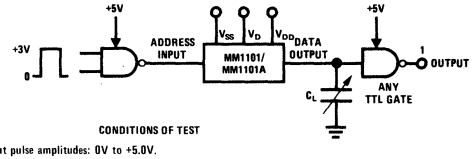


MM1101A, MM1101A1, MM1101A2, MM4250 Operating Region



ac test circuit

Test Setup for MM1101A and MM1101A Speed Measurement

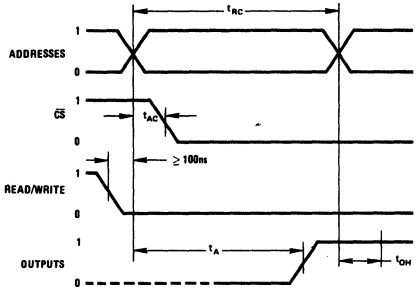


CONDITIONS OF TEST

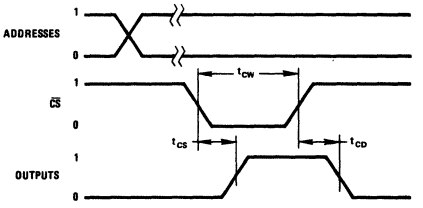
Input pulse amplitudes: 0V to +5.0V.
Input pulse rise and fall times ≤ 10 ns.
Speed measurements are referenced to the 1.5V level (unless otherwise noted); at the output of the TTL gate (t_{pd} ≤ 10 ns) C_L ≤ 20 pF.

switching time waveforms

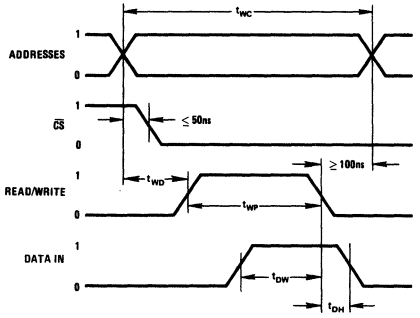
Read Cycle



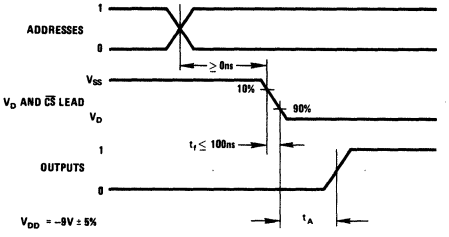
Chip Select and Deselect



Write Cycle



Power Switching For Reduced Power Applications



Note 1: All inputs of the MM1101A accept standard TTL outputs with V_{CC} = +5.0V ±5%.
Note 2: Maximum value for t_{AC} measured at minimum read cycle.

MM2102 1024-bit fully decoded static random access memory

general description

The MM2102 is a 1024 word by one bit static random access read write memory manufactured using N-channel enhancement mode silicon gate technology. Static storage cells eliminate the need for clocks and refresh. Data in and data out have the same polarity and the read operation is nondestructive.

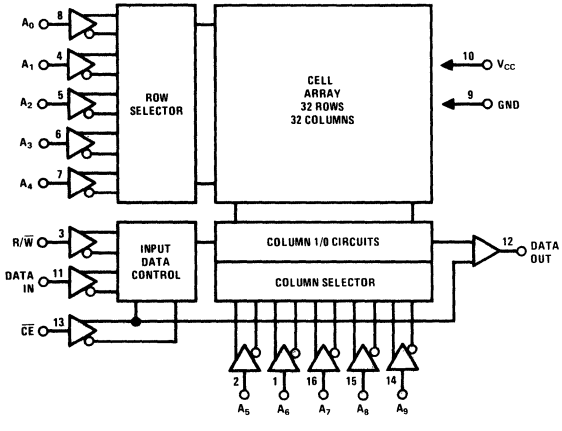
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single +5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

The simple interface and high performance make the MM2102 ideally suited for those applications, for large and small storage capacity, where cost is an important design consideration.

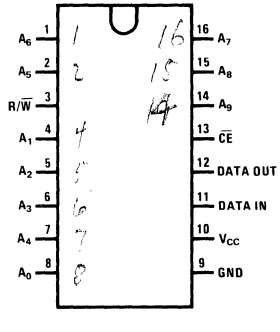
features

- Single +5.0V supply
- All inputs and output directly DTL/TTL compatible
- Static operation – no clocks or refreshing required
- Low power 150 mW typ
- High speed 500 ns typ
- TRI-STATE output for bus interface
- Chip enable allows simple memory expansion
- On chip address decode
- All inputs protected against static discharge
- Low cost 16-pin Epoxy B package

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM2102D
See Package 3
Order Number MM2102N
See Package 15

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

(T_A within operating temperature range, V_{CC} = 5.0V ±5%, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Logic "1" Input Voltage (V_{IH})		2.2		V_{CC}	V
Logic "0" Input Voltage (V_{IL})		−0.5		0.65	V
Logic "1" Output Voltage (V_{OH})	I_{OH} = −100μA	2.2			V
Logic "0" Output Voltage (V_{OL})	I_{OL} = 1.9 mA			0.45	V
Input Load Current (I_{LI})	V_{IN} = 0 to 5.25V			10	μA
Output Leakage Current (I_{LOH})	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V			10	μA
Output Leakage Current (I_{LOL})	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V			−100	μA
Power Supply Current (I_{CC1})	All Inputs = 5.25V, Data Out Open T_A = 25°C		30	60	mA
Power Supply Current (I_{CC2})	All Inputs = 5.25V Data Out Open T_A = 0°C			70	mA

ac electrical characteristics

(T_A within operating temperature range, V_{CC} = 5.0V ±5%, unless otherwise specified.)
See ac test circuit and switching time waveforms.

PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
READ CYCLE					
Read Cycle (t_{RC})	R/$\overline{W}$ = V_{IH}	1000			ns
Access Time (t_A)			500	1000	ns
Chip Enable to Output Time (t_{CO})				500	ns
Previous Read Data Valid With Respect to Address (t_{OH1})		50			ns
Previous Read Data Valid With Respect to Chip, Enable (t_{OH2})		0			ns
WRITE CYCLE					
Write Cycle (t_{WC})		1000			ns
Address to Write Set Up Time (t_{AW})		200			ns
Write Pulse Width (t_{WP})		750			ns
Write Recovery Time (t_{WR})		50			ns
Data Set Up Time (t_{DW})		800			ns
Data Hold Time (t_{DH})		100			ns
Chip Enable to Write Set Up Time (t_{CW})		900			ns
CAPACITANCE					
Input Capacitance (All Inputs) (C_{IN})	V_{IN} = 0V, T_A = 25°C, f = 1.0 MHz, (Note 2)		3.0		pF
Output Capacitance (C_{OUT})	V_{OUT} = 0V, T_A = 25°C, f = 1.0 MHz, (Note 2)		7.0		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

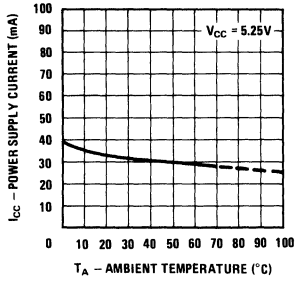
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used; Logic "1" = most positive voltage level; Logic "0" = most negative voltage level.

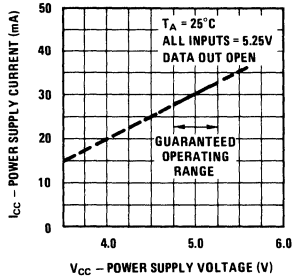
Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

typical performance characteristics

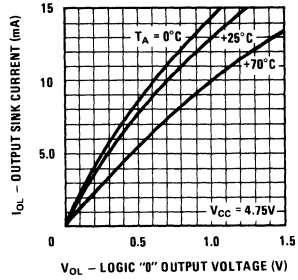
Power Supply Current vs Temperature



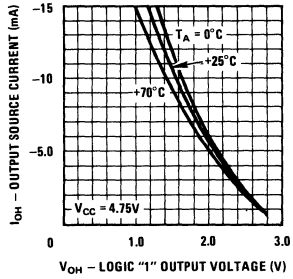
Power Supply Current vs Supply Voltage



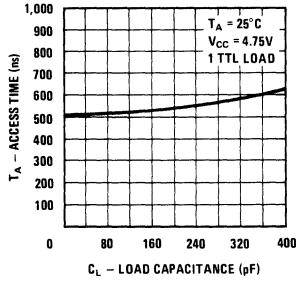
Output Sink Current vs Output Voltage



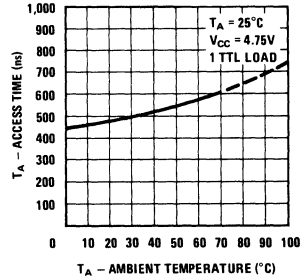
Output Source Current vs Output Voltage



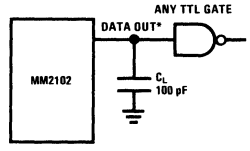
Access Time vs Load Capacitance



Access Time vs Temperature



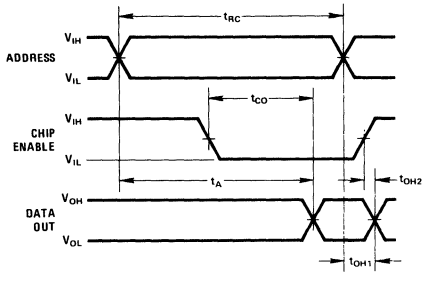
ac test circuit



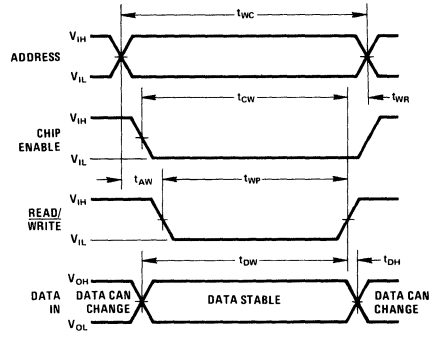
*DELAY TIMES MEASURED AT MM2102 OUTPUT.

switching time waveforms

Read Cycle



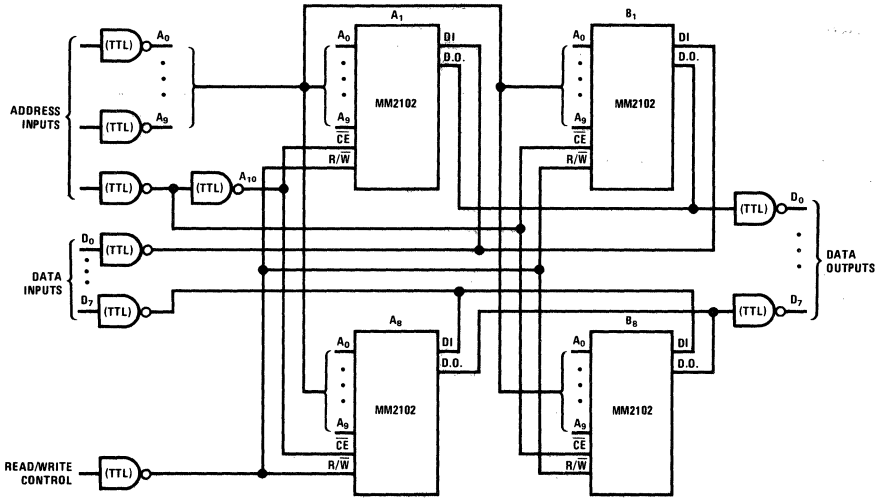
Write Cycle



NOTE: ALL TIMES MEASURED WITH RESPECT TO 1.5V LEVEL WITH t_r AND $t_f \leq 20$ ns.

typical application

2k Word 8-Bit Memory System



MM4262/MM5262 2048-bit fully decoded dynamic random access read/write memory

general description

The MM4262/MM5262 is a fully decoded 2048 word by 1 bit dynamic read/write random access memory fabricated using National Semiconductor's proprietary silicon gate low threshold technology. All inputs except the clocks are TTL compatible. The output provides a current pulse allowing a large number of devices to be bussed together without compromising system performance due to capacitive loading. The current pulse output is converted to TTL levels by means of a sense amplifier.

features

	MM4262	MM5262
■ Fast access time	470 ns (max)	365 ns (max)
■ Fast cycle time		
Short Read	565 ns (min)	475 ns (min)
Read/Write	750 ns (min)	635 ns (min)
Write	750 ns (min)	635 ns (min)
■ Refresh cycle	1.0 ms	2.0 ms

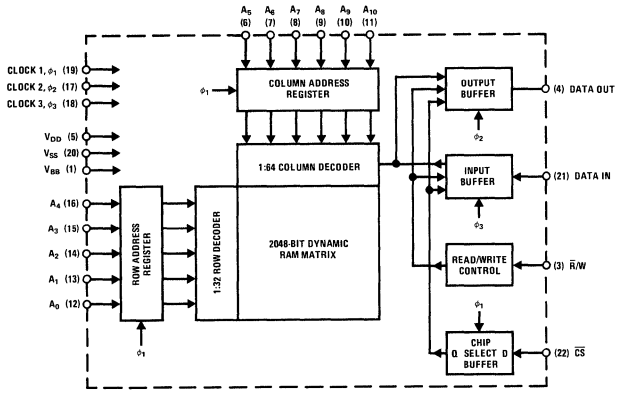
	MM4262	MM5262
■ Low power		
Operating	360 mW (max)	400 mW (max)
Standby	2.5 mW (max)	2.5 mW (max)

- Power supplies +5.0V, +8.5V, −15V
- Low overhead circuits Fully decoded with internal memory address register
- System oriented design
  - Bipolar compatible except for clocks
  - Current sense output
  - Chip Select for easy memory expansion
- Package 22 pin DIP (Cavity and Molded)
- Device protection All inputs and outputs protected against static charge

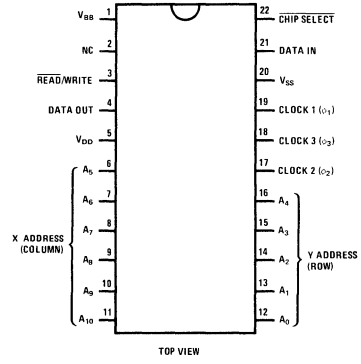
applications

- Core memory replacement
- Mainframe memory
- Buffer storage
- Non-volatile memory using battery back up

block and connection diagrams



Dual-In-Line Package



Order Number MM4262D or MM5262D
See Package 5

Order Number MM5262N
See Package 17

recommended interface circuits

CLOCK DRIVERS:	MH0026 MH8808
SENSE AMPLIFIERS:	LM167 LM168 DM7806/DM8806

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{BB} + 0.3V to V_{BB} − 27V (Note 16)
Power Dissipation	1.0W
Operating Temperature Range	
MM4262 (T_{CASE})	−55°C to +125°C
MM5262 ($T_{AMBIENT}$)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics MM4262 ($-55°C \leq T_{CASE} \leq +125°C$, V_{SS} = 5.0V ±0.25V, $V_{BB} - V_{SS}$ = 3.5V ±0.5V, V_{DD} = −15V ±1.0V, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
Inputs ($\overline{\text{Chip Select}}$, $\overline{\text{Read}}$/Write, Addresses, Data In)	(Notes 14, 15)				
Voltage					
Logical "1" (V_{IH})		V_{SS} − 1.5		V_{SS} + 1.0	V
Logical "0" (V_{IL})		V_{SS} − 10		V_{SS} 4.2	V
Current	$0 \leq V_{IN} \leq V_{SS}$			1.0	μA
Clock Inputs					
Voltage					
Logical "1" ($V_{\phi H}$)		V_{SS} − 1.0		V_{SS} + 1.0	V
Logical "0" ($V_{\phi L}$)		V_{DD} − 1.0		V_{DD} + 1.0	V
Current	V_{IN} = −16V			50	μA
Outputs	(Note 15)				
Current					
Logical "0" (I_{OL})	V_{OUT} = 0V			100	μA
Logical "1" (I_{OH})	V_{OUT} = 1.2V, $\overline{CS}$ = 0.4V			6.0	mA
	V_{OUT} = 1.8V, $\overline{CS}$ = 0.4V	500			μA
Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = 3.5V			10	μA
Power Supply Current	(Note 17) T_A = 25°C, $V_{BB} - V_{SS}$ = 3.5V, V_{SS} = 5.0V, V_{DD} = −15V, V_{OUT} = 1.2V, Reading 1's at T_{CYCLE} = 750 ns				
(I_{DD})			12	18	mA
(I_{BB})	Operating			150	μA
	Standby (No Clocks)			100	μA

ac electrical characteristics MM4262 (All times measured from 50% points, t_r, $t_f \leq 20$ ns, see ac test circuit and timing diagram, conditions under dc electrical characteristics apply.)

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
ϕ_1 Clock Pulse Width (T_{1PW})	(Note 4)	115	70		ns
ϕ_2 Clock Pulse Width (T_{2PW})	(Note 6)	275	160	400	ns
ϕ_3 Clock Pulse Width (T_{3PW})	(Note 8)	110	60		ns
ϕ_1 Clock to ϕ_2 Clock Delay (T_{12})	(Note 5)	110	60		ns
ϕ_2 Clock to ϕ_3 Clock Delay (T_{23})	(Note 7)	65	10		ns
ϕ_3 Clock to ϕ_1 Clock Delay (T_{31})	(Note 9)	75	40		ns
$\overline{\text{Chip Select}}$ and Address Set Up Time (T_{AS})		100	60		ns
$\overline{\text{Chip Select}}$ and Address Hold Time (T_{AH})		110	50		ns
$\overline{\text{Read}}$/Write Read Set Up Time (T_{RWS3})		85	30		ns
$\overline{\text{Read}}$/Write Read Hold Time (T_{RWH3})		65	30		ns
$\overline{\text{Read}}$/Write Write Set Up Time (T_{RWS1})		95	30		ns
$\overline{\text{Read}}$/Write Write Hold Time (T_{RWD3})		25	0		ns
Logical "1" Data In Set Up Time (T_{DS1})	(Note 10)	180	60		ns
Logical "0" Data In Set Up Time (T_{DS2})	(Note 10)	75	30		ns
Data In Hold Time (T_{DH1})		70	20		ns
Read Access Time (T_{ACC2})			150	260	ns
Read Access Time (T_{ACC1})	$T_{ACC1} = T_{AS} + T_{12} + T_{ACC2}$		300	470	ns

ac electrical characteristics (con't) MM4262

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
Read Only Cycle ($T_{SHORT/READ}$)	(Note 11)	565			ns
Read, Write, Read Modify Write Cycle (T_{CYCLE})		750			ns
Refresh Time	(Note 12)			1.0	ms
Output Hold Time (T_{OH})	(Note 13)	1000			ns
$\overline{\text{Chip Select}}$, Address, $\overline{\text{Read}}$/Write, Data In, Data Out Capacitance (C_X)	(Note 2) $V_{BB} - V_{SS} = 3.5V$, $V_{SS} = 5.0V$ $V_{TEST} = 5.0\ V_{DC}$ With ≤ 15 mV RMS at f = 1 MHz			7.0	pF
ϕ_1 Clock Capacitance (C_1)				50	pF
ϕ_2 Clock Capacitance (C_2)				25	pF
ϕ_3 Clock Capacitance (C_3)				25	pF
Clock Rise/Fall Time				100	ns
Input Rise/Fall Time				50	ns

dc electrical characteristics MM5262 $0°C \leq T_A \leq +70°C$, $V_{SS} = 5.0V \pm 0.25V$, $V_{BB} - V_{SS} = 3.5V \pm 0.5V$, $V_{DD} = -15V \pm 1.0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
Inputs ($\overline{\text{Chip Select}}$, $\overline{\text{Read}}$/Write, Addresses, Data In)	(Notes 14 and 15)				
Voltage					
Logical "1" (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 1.0$	V
Logical "0" (V_{IL})		$V_{SS} - 10$		$V_{SS} - 4.2$	V
Current	$0V \leq V_{IN} \leq V_{SS}$			1.0	μA
Clock Inputs					
Voltage					
Logical "1" ($V_{\phi H}$)		$V_{SS} - 1.0$		$V_{SS} + 1.0$	V
Logical "0" ($V_{\phi L}$)		$V_{DD} - 1.0$		$V_{DD} + 1.0$	V
Current	$V_{IN} = -16V$			50	μA
Output	(Note 15)				
Current					
Logical "0" (I_{OL})	$V_{OUT} = 0V$			100	μA
Logical "1" (I_{OH})	$V_{OUT} = 1.2V$, $\overline{CS} = 0.4V$			6.0	mA
	$V_{OUT} = 1.8V$, $\overline{CS} = 0.4V$	600			μA
Leakage Current	$V_{OUT} = 0V$, $\overline{CS} = 3.5V$			10	μA
Power Supply Current	(Note 17) $T_A = 25°C$, $V_{BB} - V_{SS} = 3.5V$, $V_{SS} = 5.0V$, $V_{DD} = -15V$, $V_{OUT} = 1.2V$, Reading 1's at $T_{CYCLE} = 635$ ns				
(I_{DD})			13	20	mA
(I_{BB})	Operating			150	μA
	Standby (No Clocks)			100	μA

ac electrical characteristics MM5262 (All times measured from 50% points, t_r, $t_f \leq 20$ ns, see ac test circuit and timing diagram, conditions under dc electrical characteristics apply.)

PARAMETER	CONDITIONS	MIN	TYP (Note 13)	MAX	UNITS
ϕ_1 Clock Pulse Width (T_{1PW})	(Note 4)	95	70		ns
ϕ_2 Clock Pulse Width (T_{2PW})	(Note 6)	240	160	400	ns
ϕ_3 Clock Pulse Width (T_{3PW})	(Note 8)	100	60		ns
ϕ_1 Clock to ϕ_2 Clock Delay (T_{12})	(Note 5)	90	60		ns
ϕ_2 Clock to ϕ_3 Clock Delay (T_{23})	(Note 7)	50	10		ns
ϕ_3 Clock to ϕ_1 Clock Delay (T_{31})	(Note 9)	60	40		ns
$\overline{\text{Chip Select}}$ and Address Set Up Time (T_{AS})		80	60		ns
$\overline{\text{Chip Select}}$ and Address Hold Time (T_{AH})		90	50		ns
$\overline{\text{Read}}$/Write Read Set Up Time (T_{RWS3})		70	30		ns
$\overline{\text{Read}}$/Write Read Hold Time (T_{RWH3})		65	30		ns
$\overline{\text{Read}}$/Write Write Set Up Time (T_{RWS1})		75	30		ns

ac electrical characteristics (con't) MM5262

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
$\overline{\text{Read}}$/Write Write Hold Time (T_{RWD3})		25	0		ns
Logical "1" Data In Set Up Time (T_{DS1})	(Note 10)	120	60		ns
Logical "0" Data In Set Up Time (T_{DS2})	(Note 10)	60	30		ns
Data In Hold Time (T_{DH1})		50	20		ns
Read Access Time (T_{ACC2})			150	195	ns
Read Access Time (T_{ACC1})	$T_{ACC1} = T_{AS} + T_{12} + T_{ACC2}$		300	365	ns
Read Only Cycle ($T_{SHORT/READ}$)	(Note 11)	475			ns
Read, Write, Read Modify Write Cycle (T_{CYCLE})		635			ns
Refresh Time	(Note 12)			2.0	ms
Output Hold Time (T_{OH})	(Note 13)	1000			ns
$\overline{\text{Chip Select}}$, Address, $\overline{\text{Read}}$/Write, Data In, Data Out Capacitance (C_X)	(Note 2) $V_{BB} - V_{SS} = 3.5V$, $V_{SS} = 5.0V$ $V_{TEST} = 5.0\ V_{DC}$ With ≤ 15 mV RMS at f = 1.0 MHz			7.0	pF
ϕ_1 Clock Capacitance (C_1)				50	pF
ϕ_2 Clock Capacitance (C_2)				25	pF
ϕ_3 Clock Capacitance (C_3)				25	pF
Clock Rise/Fall Time				100	ns
Input Rise/Fall Time				50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: T_{1PW}, ϕ_1 clock — used to change input logic address and $\overline{\text{chip select}}$.

Note 5: T_{12}, interval between clock 1 and 2 — for decode.

Note 6: T_{2PW}, ϕ_2 clock — cell access.

Note 7: T_{23}, interval between clock 2 and 3 — decision time.

Note 8: T_{3PW}, ϕ_3 clock — write or refresh clock.

Note 9: T_{31}, write recovery time.

Note 10: If a "1" is being written then data in must go high T_{DS1} before the end of ϕ_2 and remain in that state until T_{DH1} after ϕ_3 goes low. If a "0" is being written, data in must go low at least T_{DS2} before ϕ_3, and remain in that state until T_{DH1} after ϕ_3 goes low.

Note 11: For a short read cycle, ϕ_3 may be inhibited and the next cycle may begin T_{23} after ϕ_2.

Note 12: Addresses A_0 through A_4 are the row addresses. To accomplish a refresh, at least one location in each row must be accessed during any 2 ms period for the MM5262 and 1 ms for the MM4262. The row will refresh when reading or writing with the chip disabled or enabled as long as ϕ_3 is applied.

Note 13: During a read cycle the output will remain valid until the next ϕ_1 or T_{OH} whichever is less. During a read modify write or write cycle the output will remain valid until ϕ_3 time.

Note 14: The chip is enabled when $\overline{\text{chip select}}$ is at a logic "0."

Note 15: If a logic "1" (3.5V) is written, when it is read the output will source more than 600μA.

Note 16: Under power turn on conditions care must be taken to insure that V_{BB} is always the most positive potential in the system or large transient currents could result, causing permanent damage.

Note 17: An approximate relationship for I_{DD} is:

$$I_{DD\,max} = A\frac{T_{1PW}}{T_{CYC}} + B\frac{T_{2PW}}{T_{CYC}} + C\frac{1000\text{ ns}}{T_{CYC}}$$

where: A = 20 @ 25°C A = 23 @ 0°C A = 32 @ −55°C
B = 4.5 @ 25°C B = 5.2 @ 0°C B = 7.2 @ −55°C
C = 10 @ 25°C C = 10 @ 0°C C = 12 @ −55°C

Note 18: Typical values for $T_A = 25°C$, $V_{SS} = 5.0V$, $V_{BB} = 8.5V$, and $V_{DD} = -15V$.

timing and operation

The MM4262/MM5262 has four basic modes of operation: (1) read, (2) write, (3) read modify write and (4) refresh. Each, of these modes, is commonly used in memory systems. To make the timing and control considerations perfectly clear each mode will be discussed separately.

READ OPERATION

The read operation consists of reading previously stored data out of randomly selected address locations. The read operation may be performed in one of two ways.

The first method is by use of the $\overline{\text{Read}}/\overline{\text{Write}}$ control. As indicated in Figure 1, if the $\overline{\text{Read}}$/Write input goes low, for at least the time specified by $T_{RWS3} + T_{RWH3}$, the information will be read out of the selected memory location. The output will remain valid for $T_{OH(max)}$ or until the next ϕ_1 clock pulse, whichever is less.

The second method involves gating the ϕ_3 clock pulse. A write operation can only occur when the ϕ_3 clock is present. Thus by applying a logical "1" to the $\overline{\text{Read}}$/Write control (write mode) and not applying the ϕ_3 clock, the memory will read out information from the selected location. In other words the memory will be operating in the read mode. There are advantages in gating the ϕ_3 clock. First, since ϕ_3 clock is a high level signal, power will be reduced. Second, since in the read mode ϕ_3 has been eliminated, ϕ_1 may be applied after the T_{23} delay. This will shorten the read cycle by the $T_{3PW} + T_{31}$ interval. The short read cycle is then:

$$T_{SHORT\ READ} = T_{CYCLE} - (T_{3PW} + T_{31})$$
$$= (635 - 160)\ ns = 475\ ns \text{ for MM5262}$$
$$= (750 - 185)\ ns = 565\ ns \text{ for MM4262}$$

WRITE OPERATION

The write operation consists of storing new information into randomly selected address locations. Just as in the case of the read mode, write may be performed by using the $\overline{\text{Read}}$/Write control or by gating the ϕ_3 clock. The ϕ_3 clock is essential to the write operation and unless it is present, a write will not occur regardless of the state of the $\overline{\text{Read}}$/Write control.

READ MODIFY WRITE OPERATION

The read modify write operation consists of reading information out of a randomly selected memory location and then writing new information into this same location. The important point to remember in understanding this mode is that information is always read out of the selected address location regardless of the state of the $\overline{\text{Read}}$/Write control. In this sense, the $\overline{\text{Read}}$/Write control may be thought of as a write inhibit control.

Then, in the write mode, information will be output T_{ACC2} after the leading edge of the ϕ_2 clock and held until the start of the ϕ_3 clock. The write operation procedes in a normal manner and new information, present on the Data In line, will be written into the selected memory location.

If the Data In and Data Out lines are interfaced to a common data I/O bus, the T_{23} interval must be increased a sufficient amount to transfer the read data onto the common I/O bus and to change the I/O bus to the new information to be written. This, of course, will increase T_{CYC} by the same amount that T_{23} is increased.

REFRESH OPERATION

Because the storage mechanism of a dynamic RAM is charge retention on a capacitor, and leakage paths exist, these capacitors must be recharged or "refreshed" periodically. For the MM5262 the maximum time between refresh intervals must be less than or equal to 2.0 ms. For the MM4262 the maximum refresh interval is 1.0 ms.

The MM4262/MM5262 refreshes on a row basis. That is, when any location within a row is refreshed all locations in that row are refreshed. There are 32 rows in the RAM matrix, corresponding to addresses A_0 through A_4.

Refresh is accomplished within a row whenever the ϕ_3 clock is applied. It does not matter if the memory is in read mode, write mode, selected or not selected. The most common method of refreshing the memory is to place $\overline{CS}$ at V_{IH} and sequence the clocks through a normal read or write cycle with the ϕ_3 clock applied. Note that if, during normal system operation, each row is written into or read out of at an interval of 2.0 ms (1.0 ms for the MM4262) or less, refresh is not required as a separate operation.

Now that the four modes of operation have been defined a step by step description of a write cycle will serve to further clarify the operation of the MM4262/MM5262 RAM.

Any cycle is initiated by the leading edge of the ϕ_1 clock. For a device to be selected it must receive a ϕ_1 clock and $\overline{CS}$ must be at V_{IL} for the interval specified by T_{AS} and T_{AH}. Note that the ϕ_1 clock must be applied to deselect a device also (see block diagram). When a device is not selected, the output buffer assumes a high impedance state and the input buffer inhibits input data.

In addition to gating $\overline{CS}$ information into the device, the ϕ_1 clock also gates in address information (see block diagram). Address inputs, A_0 through A_{10}, must be stable for the interval specified by T_{AS} and T_{AH}.

timing and operation (con't)

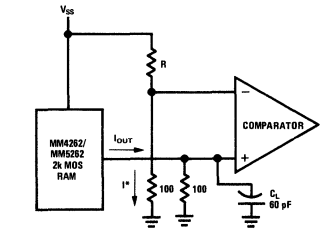
Assuming the read/write operation is to be controlled by the $\overline{\text{Read}}$/Write input, this input must be at V_{IH} for an interval of T_{RWS1} prior to the trailing edge of ϕ_1 clock, and remain at V_{IH} until T_{RWD3} after the trailing edge of the ϕ_3 clock. Note that if the $\overline{\text{Read}}$/Write input is low, during the T_{RWS3} plus T_{RWH3} interval the write operation is internally inhibited, allowing only a refresh to occur.

The ϕ_2 clock gates the information corresponding to the selected address through the output buffer (see block diagram) to the Data Out pin. The delay from leading edge of the ϕ_2 clock to valid data out is T_{ACC2}, Read Access Time. Note that even though the memory is in the write mode, data is being read out. Data out will remain valid only until the start of the ϕ_3 clock, because $\overline{\text{Read}}$/Write is at V_{IH}.

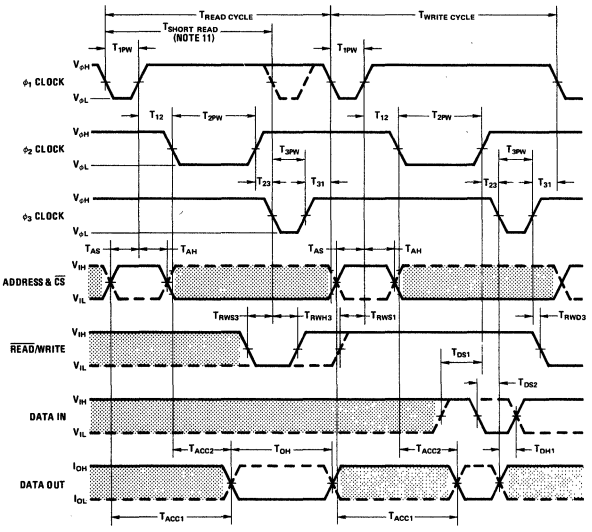
The actual write operation, as stated previously, is controlled by the ϕ_3 clock. The amount of time Data In must be stable is dependent on whether a logical "1" or a logical "0" is to be written. If a logical "1" is to be written, Data In must be stable T_{DS1} prior to the trailing edge of the ϕ_2 clock and remain stable until T_{DH1} after the leading edge of the ϕ_3 clock. If a logical "0" is to be written, Data In must be stable T_{DS2} prior to the leading edge of the ϕ_3 clock and remain stable until T_{DH1} after the leading edge of the ϕ_3 clock.

T_{31} after the trailing edge of the ϕ_3 clock another ϕ_1 clock may be applied to initiate the next cycle. Note that if the next address location is in another device the ϕ_1 clock must still be applied to deselect the current device. This becomes important when clock decoding is used to reduce power consumption in a memory system (see Application Note AN-86).

ac test circuit and switching time waveforms



*I = 500μA for MM4262
I = 600μA for MM5262



NOTE: Shaded areas are "don't care" conditions. All times measured with t_r, $t_f \leq 20$ ns.

FIGURE 1.

Clock Drivers

MH0007/MH0007C dc coupled MOS clock driver

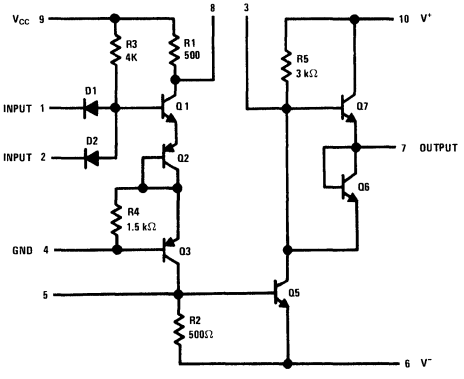
general description

The MH0007 is a voltage translator and power booster designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with inputs or clocks of MOS FET type devices. The design allows the user a wide latitude in selection of supply voltages, and is especially useful in normally "off" applications, since power dissipation is typically only 5 milliwatts in the "off" state.

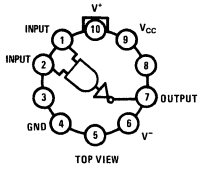
features

- 30 volts (max) output swing
- Standard 5V power supply
- Peak currents in excess of ±300 mA available
- Compatible with all MOS devices
- High speed: 5 MHz with nominal load
- External trimming possible for increased performance

schematic and connection diagram



Metal Can Package

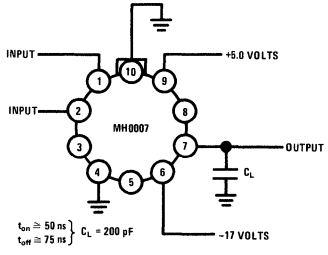


TOP VIEW

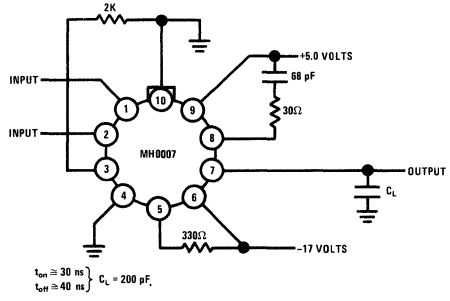
Order Number MM0007H
or MM0007CH
See Package 24

typical applications

Switching Time Test Configuration



High Speed Operation



absolute maximum ratings

V_{CC} Supply Voltage		8.0V
V^- Supply Voltage		−40V
V^+ Supply Voltage		+28V
$(V^+ - V^-)$ Voltage Differential		30V
Input Voltage		5.5V
Power Dissipation (T_A = 25°C)		800 mW
Peak Output Current		±500 mA
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	MH0007	−55°C to +125°C
	MH0007C	0°C to +85°C
Lead Temperature (Soldering, 10 seconds)		300°C

electrical characteristics (Note 1)

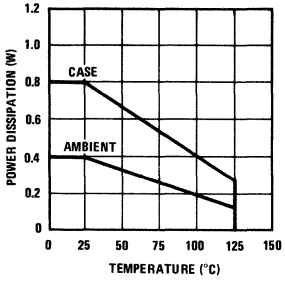
PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.2			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			100	μA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V		1.0	1.5	mA
Logical "1" Output Voltage	V_{CC} = 5.5V, I_{OUT} = 30 mA, V_{IN} = 0.8V	$V^+ - 4.0$			V
	V_{CC} = 5.5V, I_{OUT} = 1 mA, V_{IN} = 0.8V	$V^+ - 2.0$			V
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 30 mA, V_{IN} = 2.2V			$V^- + 2.0$	V
Transition Time to Logical "0" Output	C_L = 200 pF (Note 3)		50		ns
Transition Time to Logical "1" Output	C_L = 200 pF (Note 3)		75		ns

Note 1: Min/max limits apply across the guaranteed range of −55°C to +125°C for the MH0007, and from 0°C to +85°C for the MH0007C, for all allowable values of V^- and V^+.

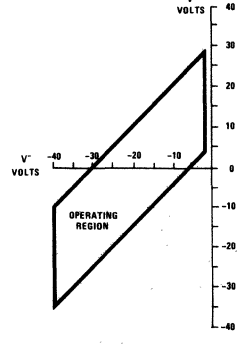
Note 2: All typical values measured at T_A = 25°C with V_{CC} = 5.0V, V^- = −25V, V^+ = 0V.

Note 3: Transition time measured from time V_{IN} = 50% value until V_{OUT} has reduced 80% of final value.

Maximum Power Dissipation



Allowable Values for V^- and V^+



Clock Drivers

MH0009/MH0009C dc coupled two phase MOS clock driver

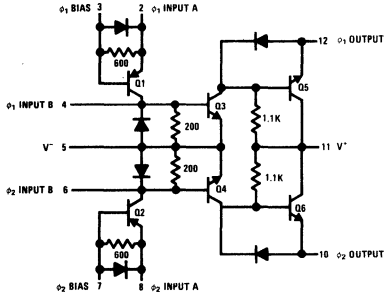
general description

The MH0009/MH0009C is high speed, DC coupled, dual MOS clock driver designed to operate in conjunction with high speed line drivers such as the DM8830, DM7440, or DM7093. The transition from TTL/DTL to MOS logic level is accomplished by PNP input transistors which also assure accurate control of the output pulse width.

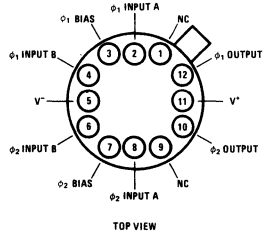
features

- DC logically controlled operation
- Output Swings – to 30V
- Output Currents – in excess of ±500 nA
- High rep rate – in excess of 2 MHz
- Low standby power

schematic and connection diagrams



Metal Can Package



TOP VIEW

Order Number MH0009G
or MH0009CG
See Package 25

typical application

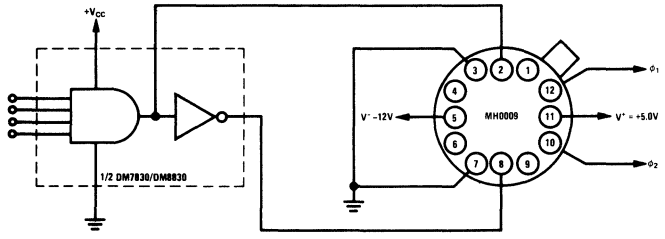


FIGURE 1

absolute maximum ratings

V^- Supply Voltage: Differential (Pin 5 to Pin 3) or (Pin 5 to Pin 7)	−40V
V^+ Supply Voltage: Differential (Pin 11 to Pin 5)	30V
Input Current: (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±500 mA
Power Dissipation (Note 2 and Figure 2)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature: MH0009	−55°C to +125°C
MH0009C	0°C to 85°C
Lead Temperature (Soldering, 10 Sec.)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ON}	C_{IN} = .0022 μF C_L = .001 μF		10	35	ns
t_{rise}	C_{IN} = .0022 μF C_L = .001 μF		40	50	ns
Pulse Width (50% to 50%)	C_{IN} = .0022 μF C_L = .001 μF	340	400	440	ns
t_{fall}	C_{IN} = .0022 μF C_L = .001 μF		80	120	ns
t_{delay}	C_{IN} = 600 pF C_L = 200 pF		10		ns
t_{rise}	C_{IN} = 600 pF C_L = 200 pF		15		ns
Pulse Width (50% to 50%)	C_{IN} = 600 pF C_L = 200 pF	40	70	120	ns
t_{fall}	C_{IN} = 600 pF C_L = 200 pF		40		ns

Note 1: Characteristics apply for circuit of Figure 1. With V^- = −20V; V^+ = 0V; V_{CC} = 5.0V. Minimum and maximum limits apply from −55°C to +125°C for the MM0009 and from 0°C to +85°C for the MH0009C. Typical values are for T_A = 25°C.

Note 2: Transient power is given by $P = fC_L (V^+ - V^-)^2$ watts, where: f = repetition rate, C_L = load capacitance, and $(V^+ - V^-)$ = output swing.

Note 3: For typical performance data see the MH0013/MH0013C data sheet.

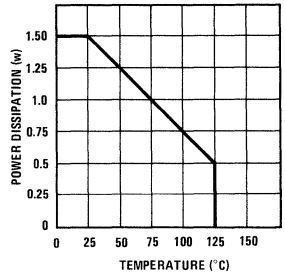


FIGURE 2. Maximum Power Dissipation

Clock Drivers

MH0012/MH0012C high speed MOS clock driver

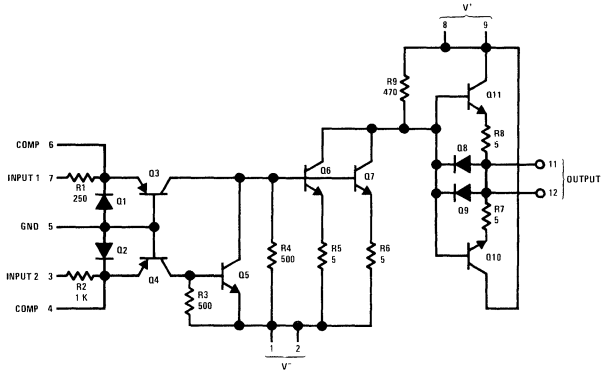
general description

The MH0012/MH0012C is a high performance clock driver that is designed to be driven by the DM7830/DM8830 or other line drivers or buffers with high output current capability. It will provide a fixed width pulse suitable for driving MOS shift registers and other clocked MOS devices.

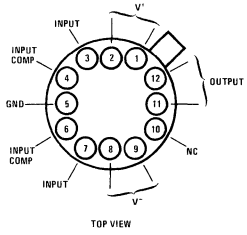
features

- High output voltage swings—12 to 30 volts
- High output current drive capability—1000 mA peak
- High repetition rate—10 MHz at 18 volts into 100 pF
- Low standby power—less than 30 mW

schematic and connection diagrams

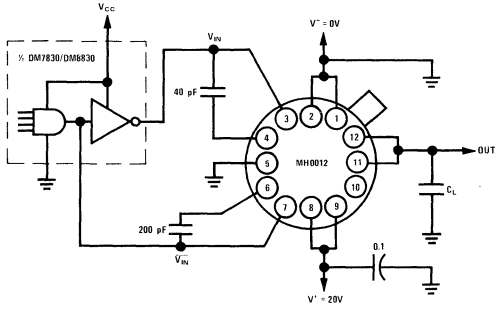


Metal Can Package

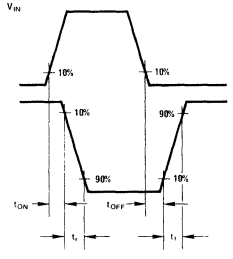


Order Number MH0012G
or MH0012CG
See Package 25

typical application (ac test circuit)



timing diagram



absolute maximum ratings

V^- Supply Voltage: Differential (Pin 1 or 2 to Pin 5) −40V
V^+ Supply Voltage: Differential (Pin 8 or 9 to Pin 1 or 2) 30V
Input Current: (Pin 3 or 7) ±75 mA
Peak Output Current ±1000 mA
Maximum Output Load–See Figure 2
Power Dissipation–See Figure 1 1.5W
Storage Temperature −65°C to +150°C
Operating Temperature: MH0012 −55°C to +125°C
MH0012C 0°C to +85°C
Lead Temperature (Soldering, 10 sec) 300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} < V^- + 2V$		1.0	2.0	V
Logic "0" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} > V^+ - 1.5V$	0.4	0.6		V
Logic "1" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = 1mA$, $V_{IN} = 2.0V$		$V^- + 1.0$	$V^- + 2.0$	V
Logic "0" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = -1mA$, $V_{IN} = 0.4V$	$V^+ - 1.5$	$V^+ - 0.7$		V
I_{DC} (V^- Supply)	$V^+ - V^- = 20V$, $V_{IN} = 2.0V$		34	60	mA

ac electrical characteristics

PARAMETER	CONDITIONS (Note 3)	MIN	TYP	MAX	UNITS
Turn-On Delay (t_{ON})	$V^+ - V^- = 20V$, $V_{CC} = 5.0V$, $C_L = 200$ pF, f = 1.0 MHz, $T_A = 25°C$		10	15	ns
Rise Time (t_r)			5	10	ns
Turn-Off Delay (t_{OFF})			35	50	ns
Fall Time (t_f)			35	45	ns

Note 1: Characteristics apply for circuit of Figure 1. Min and max limits apply from −55°C to +125°C for the MH0012 and from 0°C to +85°C for the MH0012C. Typical values are for $T_A = 25°C$.

Note 2: Due to the very fast rise and fall times, and the high currents involved, extremely short connections and good by passing techniques are required.

Note 3: All conditions apply for each parameter.

Power Dissipation

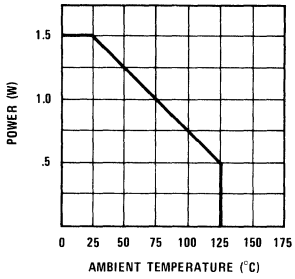


Figure 1.

Maximum Output Load vs Voltage Swing vs Rise Times

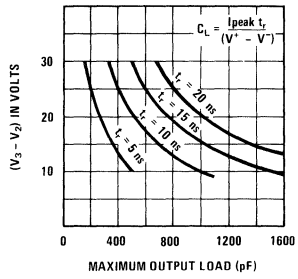
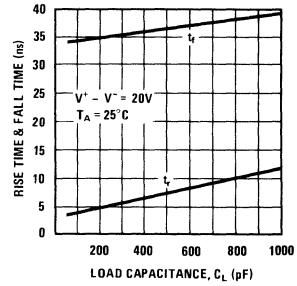


Figure 2.

Rise and Fall Times vs Load Capacitance



applications information

Power Dissipation Considerations

The power dissipated by the MH0012 may be divided into three areas of operation = ON, OFF and switching. The OFF power is approximately 30 mW and is dissipated by R_2 when Pin 3 is in the logic "1" state. The OFF power is neglible and will be ignored in the subsequent discussion. The ON power is dissipated primarily by Q_3 and R_9 and is given by:

$$P_{ON} \cong [V^- I_{IN} + \frac{(V^+ - V^-)^2}{R_9}] \text{ DC} \quad (1)$$

Where:

$$\text{DC} = \text{Duty Cycle} = \frac{\text{ON Time}}{\text{ON Time \& OFF Time}}$$

I_{IN} is given by $\frac{V_{IN} - V_{BE3}}{R_1}$ and equation (1) becomes:

$$P_{ON} = \left[\frac{(V_{IN} - V_{BE3})|V^-|}{R_1} + \frac{(V^+ - V^-)^2}{R_9}\right] \text{DC} \quad (2)$$

For $V_{IN} = 2.5V$, $V_{BE3} = 0.7V$, $V^+ = 0V$, $V^- = -20V$, and DC = 20%, $P_{ON} \cong 200$ mW.

The transient power incurred during switching is given by:

$$P_{AC} = (V^+ - V^-)^2 C_L f \quad (3)$$

For $V^+ = 0V$, $V^- = -20V$, $C_L = 200$ pF, and f = 5.0 MHz, $P_{AC} = 400$ mW.

The total power is given by:

$$P_T = P_{AC} + P_{ON} \quad (4)$$

$$P_T \leq P_{MAX}$$

For the above example, $P_T = 600$ mW.

Clock Drivers

MH0013/MH0013C two phase MOS clock driver

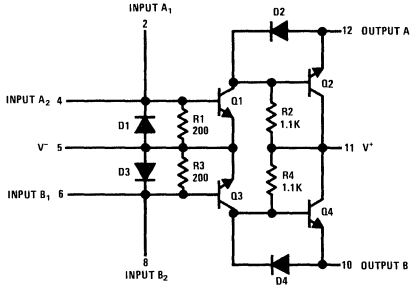
general description

The MH0013/MH0013C is a general purpose clock driver that is designed to be driven by DTL or TTL line drivers or buffers with high output current capability. It will provide fixed width clock pulses for both high threshold and low threshold MOS devices. Two external input coupling capacitors set the pulse width maximum, below which the output pulse width will closely follow the input pulse width or logic control of output pulse width may be obtained by using larger value input capacitors and no input resistors.

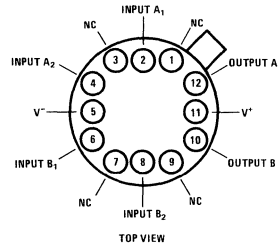
features

- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 500 mA
- High Repetition Rate—up to 5.0 MHz
- Pin Compatible with the MH0009/MH0009C
- "Zero" Quiescent Power

schematic and connection diagrams

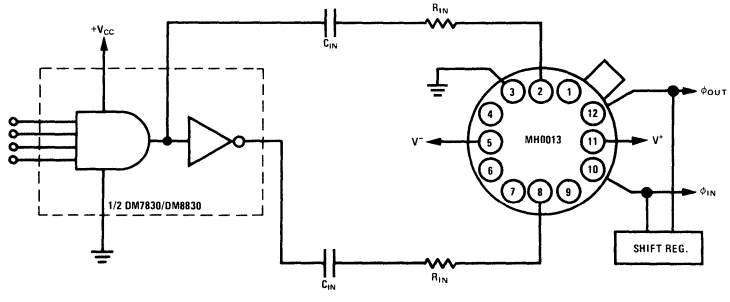


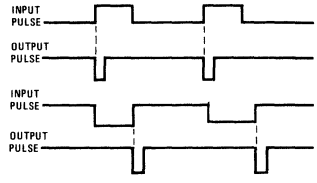
Metal Can Package



Order Number MH0013G
or MH0013CG
See Package 25

typical applications





absolute maximum ratings

$(V^+ - V^-)$ Voltage Differential	30V	Storage Temperature	−65°C to +150°C
Input Current (Pin 2, 4, 6 or 8)	±75 mA	Operating Temperature MH0013	−55°C to +125°C
Peak Output Current	±600 mA	MH0013C	0°C to +85°C
Power Dissipation (Figure 7)	1.5W	Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1 and Figure 8)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "0" Output Voltage	I_{OUT} = −50 mA I_{IN} = 1.0 mA	$V^+ - 3.0$	$V^+ - 1.0$		V
	I_{OUT} = −10 mA I_{IN} = 1.0 mA		$V^- - 0.7$	$V^+ - 0.5$	V
Logical "1" Output Voltage	I_{OUT} = 50 mA I_{IN} = 10 mA		$V^- + 1.5$	$V^- + 2.0$	V
					V
Power Supply Leakage Current	$(V^+ - V^-)$ = 30V $I_{OUT} = I_{IN}$ = 0 mA		1.0	100	μA
Negative Input Voltage Clamp	I_{IN} = − 10 mA	$V^- - 1.2$	$V^- - 0.8$		V
$t_{d\,ON}$			20	35	ns
t_{rise}			35	50	ns
$t_{d\,OFF}$ (Note 2)	C_{IN} = 0.0022 μF R_{IN} = 0Ω		30	60	ns
t_{fall} (Note 2)	C_L = 0.001 μF	40	50	80	ns
t_{fall} (Note 3)		40	70	120	ns
Pulse Width (50% to 50%) (Note 3)		340	420	490	ns
t_{rise}	C_{IN} = 500 pF		15		ns
t_{fall}	R_{IN} = 0Ω		20		ns
Pulse Width (50% to 50%) (Note 3)	C_L = 200 pF		110		ns
Positive Output Voltage Swing			$V^+ - 0.7V$		V
Negative Output Voltage Swing			$V^- + 0.7V$		V

Note 1: Min/max limits apply over guaranteed operating temperature range of −55°C to +125°C for MH0013 and 0°C to +85°C for MH0013C, with V^- = −20V and V^+ = 0V unless otherwise specified. Typical values are for 25°C.

Note 2: Parameter values apply for clock pulse width determined by input pulse width.

Note 3: Parameter values apply for input pulse width greater than output clock pulse width.

TABLE I. Typical Drive Capability of One Half MH0013 at 70°C Ambient

$(V_3 - V_2)$ VOLTS	FREQUENCY MHz	PULSE WIDTH ns	TYPICAL R_{IN} Ω	TYPICAL C_{IN} pF	OUTPUT DRIVE CAPABILITY IN pF[1]	RISE TIME LIMIT ns[2]
28					50	–
20	4.0	100	0	750	200	7
16					350	10
28					100	5
20	2.0	200	10	1600	400	14
16					700	19
28					400	19
20	1.0	200	0	2300	1000	34
16					1700	45
28					2800	130
20	0.5	500	10	4000	5500	183
16					9300	248

Note 1: Output load is the maximum load that can be driven at 70°C without exceeding the package rating under the given conditions.

Note 2: The rise time given is the minimum that can be used without exceeding the peak transient output current for the full rated output load.

performance characteristics

FIGURE 1. Output Load vs Voltage Swing

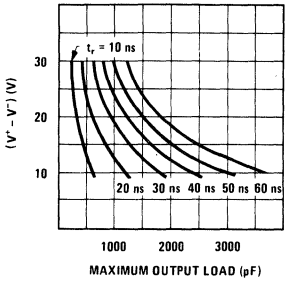


FIGURE 2. Transient Power vs Rep. Rate vs C_L

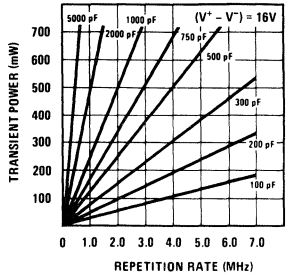
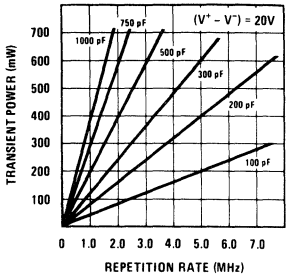


FIGURE 3. Transient Power vs Rep. Rate vs C_L



performance characteristics (con't)

FIGURE 4. Average Internal Power vs Output Swing vs Duty Cycle

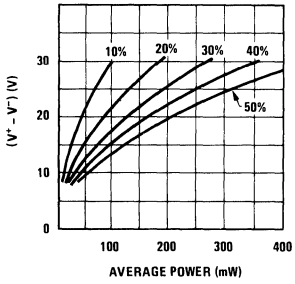


FIGURE 5. Typical Clock Pulse Variations vs Ambient Temperature

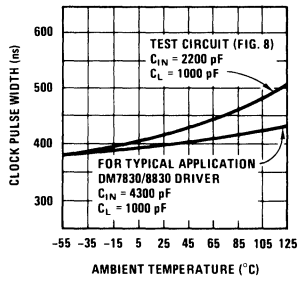


FIGURE 6. R_{IN} vs C_{IN} vs Pulse Width

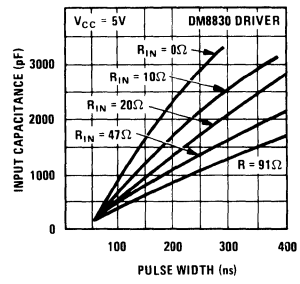
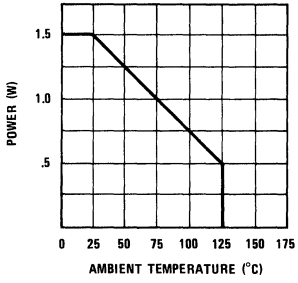


FIGURE 7. Package Power Derating



circuit operation

Input current forced into the base of Q1 through the coupling capacitor C_{IN} causes Q1 to be driven into saturation, swinging the output to $V^- + V_{CE}(SAT) + V_{DIODE}$.

When the input current has decayed, or has been switched, such that Q1 turns off, Q2 receives base drive through R2, turning Q2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q1 always switches off before Q2 begins to supply current; hence, high internal transient currents from V^+ to V^- cannot occur.

pulse width

Maximum output pulse width is a function of the input driver characteristics and the coupling capacitance and resistance. After being turned on, the input current must fall from its initial value I_{IN} peak to below the input threshold current I_{IN} min $\simeq V_{BE}/R1$ for the clock driver to turn off. For example, referring to the test circuit of Figure 8, the output pulse width, 50% to 50%, is given by

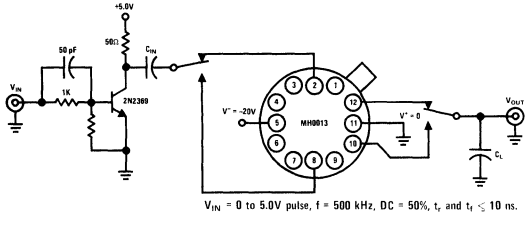
$$pw_{OUT} \cong \frac{1}{2}(t_{rise} + t_{fall}) + R_O C_{IN} \ln \frac{I_{IN}\ peak}{I_{IN}\ min} \cong 400\ ns.$$

For operation with the input pulse shorter than the above maximum pulse width, the output pulse width will be directly determined by the input pulse width.

$$pw_{OUT} = pw_{IN} + t_{dOFF} + t_{dON} + \frac{1}{2}(t_{fall} + t_{rise})$$

Typical maximum pulse width for various C_{IN} and R_{IN} values are given in Figure 6.

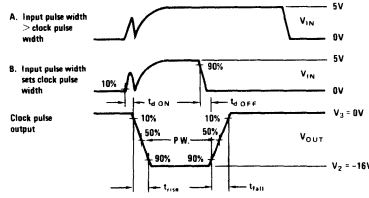
ac test circuit



V_{IN} = 0 to 5.0V pulse, f = 500 kHz, DC = 50%, t_r and $t_f \leq 10$ ns.

Figure 8

timing diagram



fan-out calculation

The drive capability of the MH0013 is a function of system requirements, i.e., speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition. Some typical fan-outs for conditions are given in Table 1.

Transient Current

The maximum peak output current of the MH0013 is given as 600 mA. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{T_R} \qquad (1)$$

This can give a maximum limit to the load.

Figure 1 shows maximum voltage swing and capacitive load for various rise times.

1. *Transient Output Power*

The average transient power (P_{AC}) dissipated is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (F).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times F \qquad (2)$$

Figures 2 and 3 show transient power for two different values of $(V^+ - V^-)$ versus output load and frequency.

2. *Internal Power*

"0" State

Negligible (<3 mW)

"1" State

$$P_{INT} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle.} \qquad (3)$$

Figure 4 gives various values of internal power versus ouptut voltage and duty cycle.

3. *Input Power*

The average input power is a function of the input current and duty cycle. Due to input voltage clamping, this power contribution is small and can therefore be neglected. At maximum duty cycle of 50%, at 25°C, the average input power is less than 10 mW per phase for $R_{IN}C_{IN}$ controlled pulse widths. For pulse widths much shorter than $R_{IN}C_{IN}$, and maximum duty cycle of 50%, input power could be as high as 30 mW, since I_{IN} peak is maintained for the full duration of the pulse width.

4. *Package Power Dissipation*

Total Average Power = Transient Output Power + Internal Power + Input Power

Typical Example *Calculation for One Half MH0013C*

How many MM506 shift registers can be driven by an MH0013C driver at 1 MHz using a clock pulse width of 400 ns, rise time 30–50 ns and 16 volts amplitude over the temperature range 0–70°C?

Power Dissipation

From the graph of power dissipation versus temperature, Figure 7, it can be seen that an MH0013C at 70°C can dissipate 1W without a heat sink; therefore, each half can dissipate 500 mW.

Transient Peak Current Limitation

From Figure 1 (equation 1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 1140 pF.

Average Internal Power

Figure 4 (equation 3) gives an average power of 102 mW at 16V 40% duty cycle.

Input power will be a maximum of 8 mW.

Transient Output Power

For one half of the MH0013C

500 mW = 102 mW + 8 mW
+ transient output power

390 mW = transient output power

Using Figure 2 (equation 2) at 16V, 1 MHz and 390 mW, each half of the MH0013C can drive a 1520 pF load. This is, however, in excess of the load derived from the transient current limitation (Figure 1, equation 1), and so a maximum load of 1140 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{1140}{80}$ or 14 registers.

For nonsymmetrical clock widths, drive capability is improved.

Clock Drivers

MH0025/MH0025C two phase MOS clock driver

general description

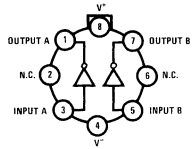
The MH0025/MH0025C is monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL/DTL line drivers or buffers such as the DM932, DM8830, or DM7440. Two input coupling capacitors are used to perform the level shift from TTL/DTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse widths may be set by selection of the input capacitors eliminating the need for tight input pulse control.

features

- 8-lead TO-5 or 8-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DM932, DM8830, DM7440(SN7440)
- "Zero" Quiescent Power

connection diagrams

Metal Can Package

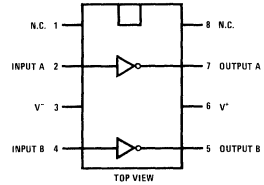


Note: Pin 4 connected to case.

TOP VIEW

Order Number MH0025H or MH0025CH
See Package 23

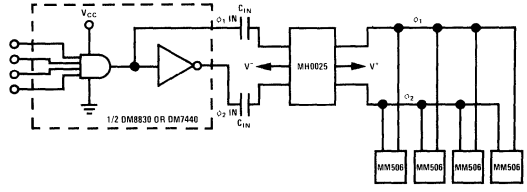
Dual-In-Line Package



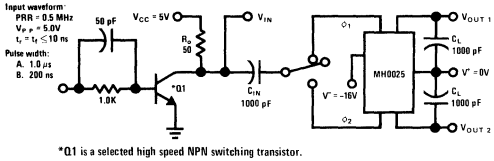
TOP VIEW

Order Number MH0025CN
See Package 12

typical application

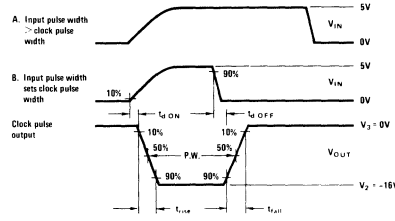


ac test circuit



*Q1 is a selected high speed NPN switching transistor.

timing diagram



absolute maximum ratings

$(V^+ - V^-)$ Voltage Differential	30V
Input Current	100 mA
Peak Output Current	1.5A
Power Dissipation	See Curves
Storage Temperature	−65°C to +150°C
Operating Temperature MH0025	−55°C to +125°C
MH0025C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1) See test circuit.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$T_{d_{ON}}$			15	30	ns
T_{rise}	C_{IN} = .001 μF		25	50	ns
$T_{d_{OFF}}$ (Note 2)	R_{IN} = 0Ω		30	60	ns
T_{fall} (Note 2)	C_L = .001 μF	60	90	120	ns
T_{fall} (Note 3)		100	150	250	ns
P.W. (50% to 50%) (Note 3)			500		ns
Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA	$V^+ - 1.0$	$V^+ - 0.7V$		V
Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA		$V^- + 0.7V$	$V^- + 1.5V$	V

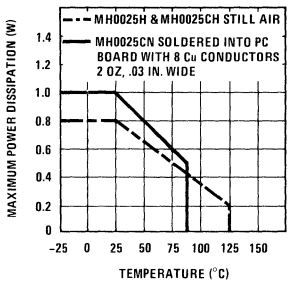
Note 1. Min/Max limits apply across the guaranteed operating temperature range of −55°C to +125°C for MH0025 and 0°C to 85°C for MH0025C. Typical values are for +25°C.

Note 2. Parameter values apply for clock pulse width determined by input pulse width.

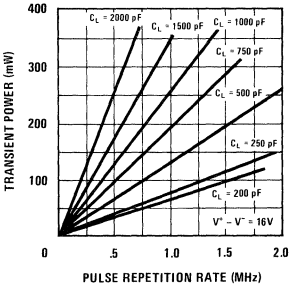
Note 3. Parameter values apply for input pulse width greater than output clock pulse width.

performance characteristics

Package Power Derating

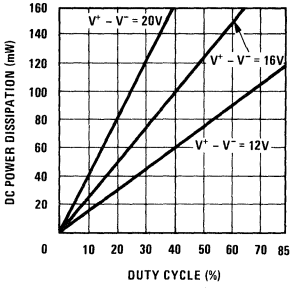


Transient Power vs Rep. Rate



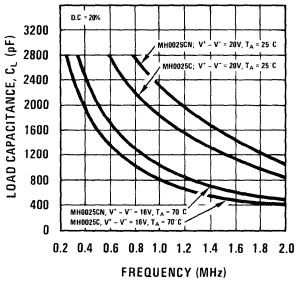
$P_{AC} = (V^+ - V^-)^2 f C_L$

DC Power (P_{DC}) vs Duty Cycle



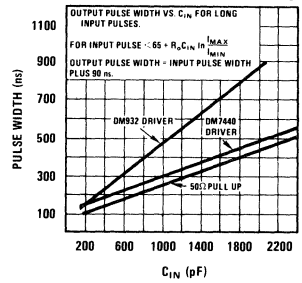
$$P_{DC} = \frac{(V^+ - V^-)^2 (DC)}{1k}$$

Maximum Load Capacitance



$$C_L < \frac{(P_{MAX})(1k) - (V^+ - V^-)^2 (DC)}{(f)(1k)(V^+ - V^-)^2} \leq \frac{(I_{pk})(t_r)}{V^+ - V^-}$$

Output P.W. Controlled by C_{IN}



I_{MAX} = Peak current delivered by driver

$I_{MIN} \geq (V_{BE}/R1) = (0.6/1k)$

applications information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents form V^- to V^+ cannot occur.

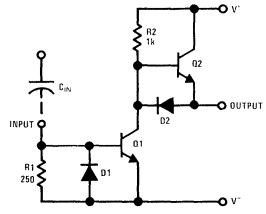


FIGURE 1. MH0025 Schematic (One-Half Circuit)

Fan-Out Calculation

The drive capability of the MH0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the MH0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns For $V^+ - V^- = 20V$, I = 0.8A.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, f = 1.0 MHz, C_L = 1000 pF, P_{AC} = 400 mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

= 80 mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power

example calculation

How many MM506 shift registers can be driven by an MH0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30-50 ns and 16V amplitude over the temperature range 0-70°C?

Power Dissipation:

At 70°C the MH0025CN can dissipate 630 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one half of the MH0025C, 630 mW ÷ 2 can be dissipated.

315 mW = 50 mW + transient output power

265 mW = transient output power

Using equation (2) at 16V, 1 MHz and 250 mW, each half of the MH0025CN can drive a 975 pF load. This is, less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 975 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{975}{80}$ or 12 registers.

5

Clock Drivers

MH0026/MH0026C 5 MHz two phase MOS clock driver

general description

The MH0026/MH0026C is a low cost monolithic high speed two phase MOS clock driver and interface circuit. Unique circuit design along with advanced processing provide both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 series gates and flip-flops or from drivers such as the DM8830 or DM7440. The MH0026 is intended for applications in which the output pulse width is logically controlled: i.e., the output pulse width is equal to the input pulse width.

features

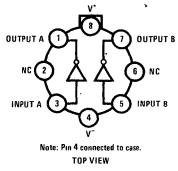
- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on load
- Low power consumption in MOS "O" state—2 mW
- Drives to 0.4V of GND for RAM address drive

The MH0026 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16 bit MM1103 RAM memory system. Information on the correct usage of the MH0026 in these as well as other systems is included in the Application Section. A thorough understanding of its usage will insure optimum performance of the device.

The device is available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt TO-8 packages.

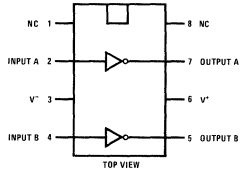
connection diagrams

Metal Can Package



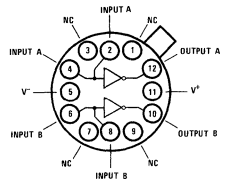
Order Number MH0026H or MH0026CH
See Package 23

Dual-In-Line Package



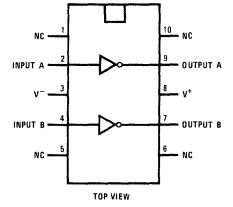
Order Number MH0026J or MH0026CJ
See Package 9

Metal Can Package



Order Number MH0026G or MH0026CG
See Package 25

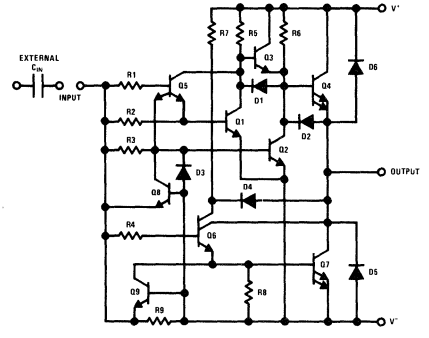
Flat Package



Order Number MH0026F or MH0026CF
See Package 25A

schematic diagram

(1/2 of Circuit Shown)



absolute maximum ratings (Notes 1 & 2)

$V^+ - V^-$ Differential Voltage		22V
Input Current		100 mA
Input Voltage ($V_{IN} - V^-$)		5.5V
Peak Output Current		1.5A
Power Dissipation		See curves
Operating Temperature Range	MH0026	−55°C to +125°C
	MH0026C	0°C to 85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Logic "1" Input Voltage	$V_{OUT} = V^- + 1.0V$	2.5	1.5		V
Logic "1" Input Current	$V_{IN} - V^- = 2.5V$, $V_{OUT} = V^- + 1.0V$		10	15	mA
Logic "0" Input Voltage	$V_{OUT} = V^+ - 1.0V$		0.6	0.4	V
Logic "0" Input Current	$V_{IN} - V^- = 0V$, $V_{OUT} = V^+ - 1.0V$		−0.005	−10	μA
Logic "0" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$ $V_{IN} = -11.6$	4.0	4.3		V
Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$	$V^+ - 1.0$	$V^+ - 0.7$		V
Logic "1" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$ $V_{IN} = -9.5V$		−11.5	−11.0	V
Logic "1" Output Voltage	$V_{IN} - V^- = 2.5V$		$V^- + 0.5$	$V^- + 1.0$	V
"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.5V$		30	40	mA
"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0.0V$		10	100	μA

ac electrical characteristics (Notes 1 & 2, AC test circuit)

Turn-On Delay (t_{ON})		5.0	7.5	12	ns
Turn-Off Delay (t_{OFF})		5.0	12	15	ns
Rise time (t_r) – Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		12		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		15	18	ns
	$C_L = 1000$ pF		20	35	ns
Falltime (t_f) – Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		10		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		12	16	ns
	$C_L = 1000$ pF		17	25	ns

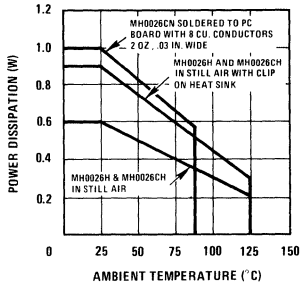
Note 1: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range −55°C to +125°C for the MH0026 and 0°C to +85°C for the MH0026C.

Note 2: All typical values for the $T_A = 25°C$.

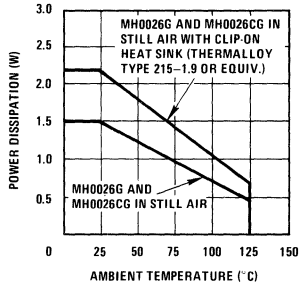
Note 3: Rise and fall times are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall. See waveforms.

typical performance characteristics

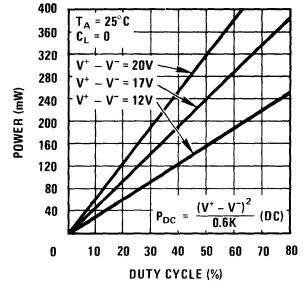
TO-5 & DIP Power Ratings



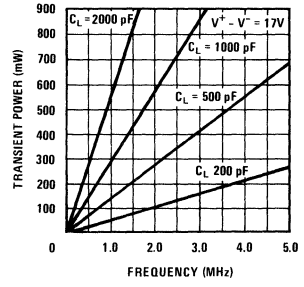
TO-8 Package Power Rating



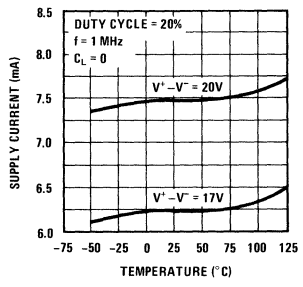
DC Power (P_{DC}) vs Duty Cycle



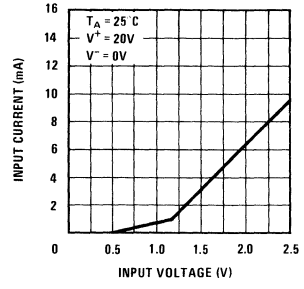
Transient Power (P_{AC}) vs Frequency



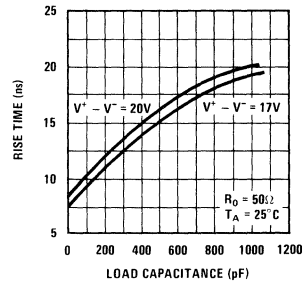
Supply Current vs Temperature



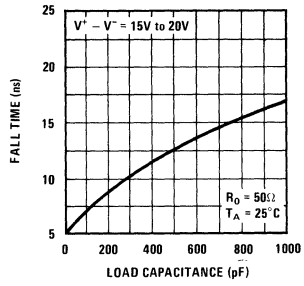
Input Current vs Input Voltage



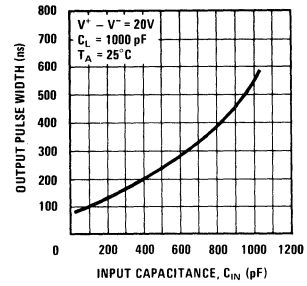
Rise Time vs Load Capacitance



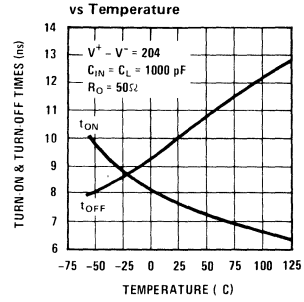
Fall Time vs Load Capacitance



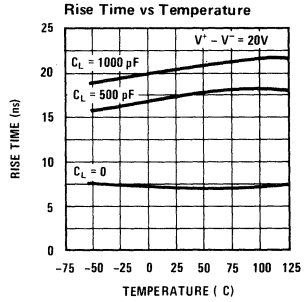
Optimum Input Capacitance vs Output Pulse Width



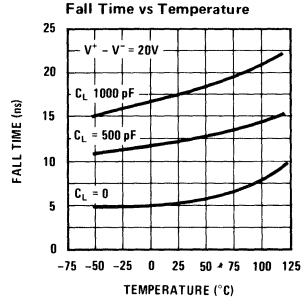
Turn-On & Turn-Off Time vs Temperature



Rise Time vs Temperature

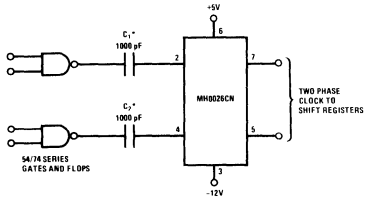


Fall Time vs Temperature

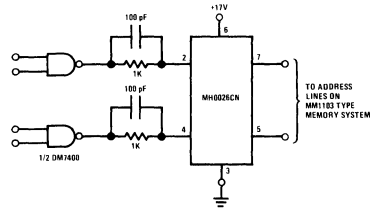


typical applications

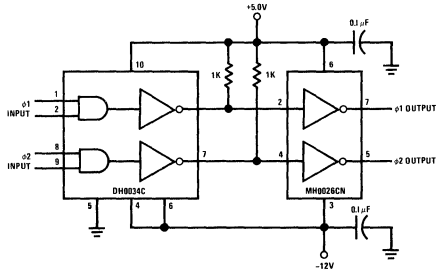
AC Coupled MOS Clock Driver



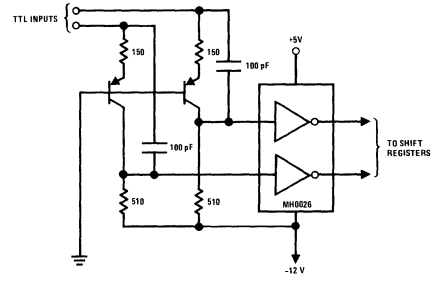
DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



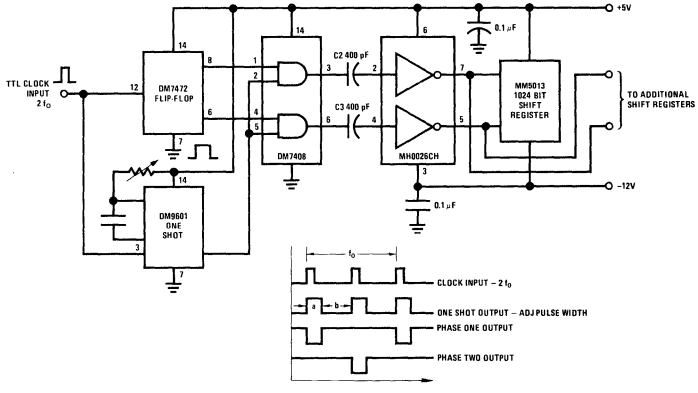
DC Coupled MOS Clock Driver



Transistor Coupled MOS Clock Driver

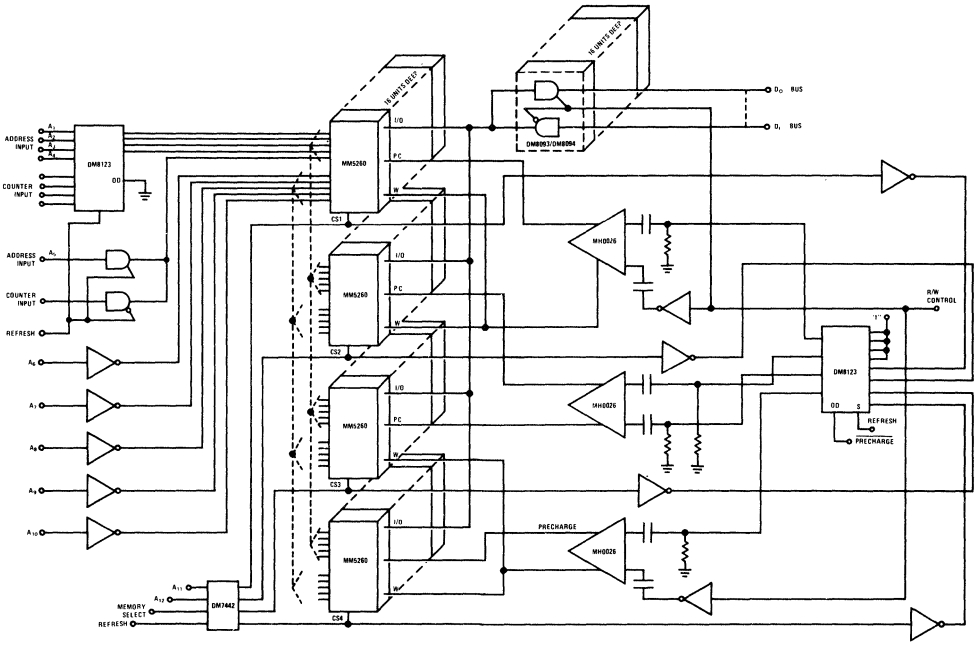


Logically Controlled AC Coupled Clock Driver

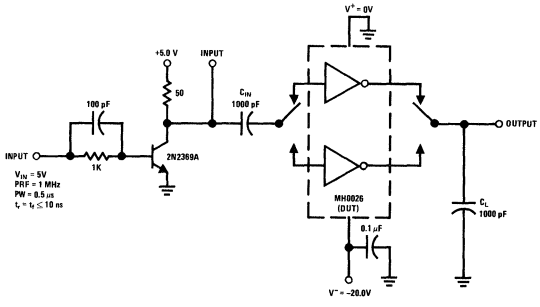


typical applications (con't)

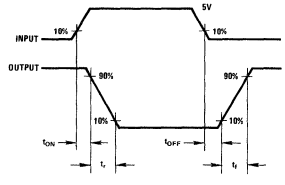
Precharge Driver for MOS RAM Memories



ac test circuit



switching time waveforms



application information

1.0 Introduction

The MH0026 is capable of delivering 30 watts peak power (1.5 amps at 20V needed to rapidly charge large capacitative loads) while its package is limited to the watt range. This section describes the operation of the circuit and how to obtain optimum system performance. If additional design information is required, please contact your local National field application engineer.

2.0 Theory of Operation

Conventional MOS clock drivers like the MH0013 and similar devices have relied on the circuit configuration in Figure 1. The AC coupling of an input pulse allows the device to work over a wide

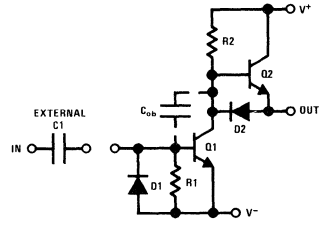


FIGURE 1. Conventional MOS Clock Drive

application information (con't)

range of supplies while the output pulse width may be controlled by the time constant $-R_1 \times C_1$.

D_2 provides 0.7V of dead-zone thus preventing Q_1 and Q_2 from conducting at the same time. In order to drive large capacitive loads, Q_1 and Q_2 are large geometry devices but C_{ob} now limits useful output rise time. A high voltage TTL output stage (Figure 2) could be used; however, during switching until the stored charge is removed from Q_1, both output devices conduct at the same time. This is familiar in TTL with supply line glitches in the order of 60 to 100 mA. A clock driver built this way would introduce 1.5 amp spikes into the supply lines.

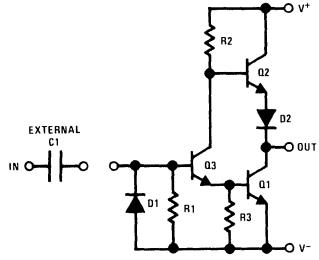


FIGURE 2. Alternate MOS Clock Drive

Unique circuit design and advanced semiconductor processing overcome these clasic problems allowing the high volume manufacture of a device, the MH0026, that delivers 1.5A peak output currents with 20ns rise and fall times into 1000pF loads. In

a simplified diagram, D_1 (Figure 3) provides 0.7V dead zone so that Q_3 is turned ON for a rising input pulse and Q_2 OFF prior to Q_1 turning ON a few nanoseconds later. D_2 prevents zenering of the emitter-base junction of Q_2 and provides an initial discharge path for the load via Q_3. During a falling input, the stored charge in Q_3 is used beneficially to keep Q_3 ON thus preventing Q_2 from conducting until Q_1 is OFF. Q_1 stored charge is quickly discharged by means of common-base transistor Q_4.

The complete circuit of the MH0026 (see schematic on page 130 basically makes Darlingtons out of each of the transistors in Figure 3.

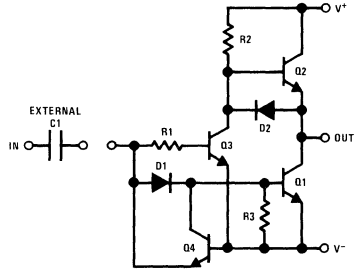


FIGURE 3. Simplified MH0026

When the output of the TTL input element (not shown) goes to the logic "1" state, current is supplied through C_{IN} to the base of Q_1 and Q_2 turning them ON, and Q_3 and Q_4 OFF when the input voltages reaches 0.7V. Initial discharge of the load as well as E-B protection for Q_3 and Q_4 are provided by D_1 and D_2. When the input voltage reaches about 1.5V, Q_6 and Q_7 begin to conduct and the load is rapidly discharged by Q_7. As the input goes low, the input side of C_{IN} goes negative with respect to V^- causing Q_8 and Q_9 to conduct momentarily to assure rapid turn-off of Q_2 and Q_7 respectively. When Q_1 and Q_2 turn OFF, Darlington connected Q_3 and Q_4 rapidly charge the load toward V^+ volts. R_6 assures that the output will reach to within one V_{BE} of the V^+ supply.

The real secret of the device's performance is proper selection of transistor geometries and resistor values so that Q_4 and Q_7 do not conduct at the same time while minimizing delay from input to output.

3.0 Power Dissipation Considerations

There are four considerations in determining power dissipations.

1. Average DC power
2. Average AC power
3. Package and heat sink selection
4. Remember—2 drivers per package

The total average power dissipated by the MH0026 is the sum of the DC power and AC transient power. The total must be less than given package power ratings.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Since the device dissipates only 2mW with output voltage high (MOS logic "0"), the dominating factor in average DC power is duty cycle or the percent of time in output voltage low state (MOS logic "1"). Percent of total power contributed by P_{DC} is usually neglible in shift register applications where duty cycle is less than 25%. P_{DC} dominates in RAM address line driver applications where duty cycle can exceed 50%.

3.1 DC Power (per driver)

DC Power is given by:

$$P_{DC} = (V^+ - V^-) \times (I_{S(Low)}) \times \left(\frac{\text{ON time}}{\text{OFF time—ON time}}\right)$$

or P_{DC} = (Output Low Power) X (Duty Cycle)

where: $I_{S(Low)} = I_S @ V^+ - V^- = \frac{V_S}{20V}$

5

application information (con't)

Example 1: (V^+ = +5V, V^- = -12V)

a) Duty cycle = 25%, therefore

P_{DC} = 17V X 40mA X 17/20 X 25%

P_{DC} = 145mW worst-case, each side

P_{DC} = 109mW typically

b) Duty cycle = 5%

P_{DC} = 21mW

c) See graph.

The above illustrates that for shift register applications, the minimum clock width allowable for the given type of shift register should be used in order to drive the largest number of registers per clock driver.

Example 2: (V^+ = +17V, V^- = GND):

a) Duty cycle = 50%

P_{DC} = 290mW worst-case

P_{DC} = 218mW typically

b) Duty cycle = 100%

P_{DC} = 580mW

Thus for RAM address line applications, package type and heat sink technique will limit drive capability rather than AC power.

3.2 AC Transient Power (per driver)

AC Transient power is given by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L$$

where: f = frequency of operation

C_L = Load capacitance (including all strays and wiring)

Example 3: (V^+ = +5V, V^- = -12V)

P_{AC} = 17 X 17 X f(MHz) X 10^6 X C_L(nF) X 10^{-9}

P_{AC} = 290mW per MHz per 1000pF

Thus at 5MHz, a 1000pF load will cause any driver to dissipate one and one half watts. For long shift registers, a driver with the highest package power rating will drive the largest number of bits for the lowest cost per bit.

3.3 Package Selection

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs illustrate derating for various operating temperatures.

3.31 TO-5 ("H") Package: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 900mW with clip on heat sink (derate at 6.0mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving capability by 50%.

3.32 8-Pin ("N") Molded Mini-DIP: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 1.0 watt soldered to PC board (derate at 6.6mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600mW when mounted in a socket and not one watt until it is soldered down.)

3.33 TO-8 ("G") Package: Rated at 1.5 watts still air (derate at 10mW/°C above 25°C) and 2.3 watts with clip on heat sink (Thermalloy type 215-1.9 or equivalent—derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

3.4 Summary—Package Power Considerations

The maximum capacitative load that the MH0026 can drive is thus determined by package type, heat sink technique, ambient temperature, AC power (which is proportional to frequency and capacitive load) and DC power (which is principally determined by duty cycle). Combining equations previously given, the following formula is valid for any clock driver with negligible input power and negligible power in output high state:

$$C_L \text{ (max in pF)} = \frac{10^{-3}}{n} \times \frac{P_{max(mW)}(T_A, pkg) \times R_{eq} - (V^+ - V^-)^2 \times (Dc) \times 10^3}{(V^+ - V^-)^2 \times Req \times f(MHz)}$$

$$C_L \text{ (max in pF)} = .5 \times 10^{-3} \times \frac{P_{max}(mW) \times 500 - V_S^2 \times Dc \times 10^3}{V_S^2 \times 500 \times f(MHz)}$$

Where: n = number of drivers per pkg. (2 for the MH0026)

$P_{max(mW)}(T_A, pkg)$ = Package power rating in milliwatts for given package, heat sink, and max, ambient temperature (See graphs)

application information (con't)

R_{eq} = equivalent internal resistance

$R_{eq} = (V^+ - V^-)/I_{S(Low)}$ = 500 ohms (worst case over temperature for the MH0026 or 660 ohms typically)

$V_S = (V^+ - V^-)$ = total supply voltage across device

Dc = Duty Cycle =

$$\frac{\text{Time in output low state}}{\text{Time in output low + Time in output high state}}$$

Table I illustrates MH0026 drive capability under various system conditions.

4.0 Pulse Width Control

The MH0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + t_r + t_f = PW_{IN} + 25ns$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the MH0026 discharges to just above the devices threshold (about 1.5V). If the input is allowed to discharge below the threshold, t_{OFF} and t_f will be degraded. The graph on page 132 shows optimum values for C_{IN} vs desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN} = (2 \times 10^{-3})\,(PW)_{OUT}$$

For an output pulse width of 500ns, the optimum value for C_{IN} is:

$$C_{IN} = (2 \times 10^{-3})(500 \times 10^{-9}) \cong 1000pF$$

5.0 Rise & Fall Time Considerations (Note 3)

The MH0026's peak output current is limited to 1.5A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leqslant 1.5A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V)(250 \times 10^{-12} + C_L)$$

Where: ΔV = The change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

For $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20V)(250 \times 10^{-12} + 10^{-12}) = 25ns$$

For small values of C_L, equation above predicts optimistic values for t_r. The graph on page 132 shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2R\left(C_S + \frac{C_L}{h_{FE} + 1}\right)$$

6.0 Clock Overshoot

The output waveform of the MH0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the ouput of the MH0026. The critical valve for $R_s = 2\sqrt{LCL}$ where

TABLE 1. Worst Case Maximum Drive Capability for MH0026*

PACKAGE TYPE		TO-8 WITH HEAT SINK		TO-8 FREE AIR		MINI-DIP SOLDERED DOWN		TO-5 AND MINI-DIP FREE AIR	
Max. Operating Frequency	Max. Ambient Temp. ↓ / → Duty Cycle	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C
100kHz	5%	30 k	24 k	19 k	15 k	13 k	10k	7.5k	5.8k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2.7k	2k	1.5k	1.1k
1MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	430
2MHz	25%	1.4k	1.1k	850	650	550	400	280	190
5MHz	25%	620	470	380	290	240	170	120	80
10MHz	25%	280	220	170	130	110	79	–	–

*Values in pF and assume both sides in use as non-overlaping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$.

application information (con't)

L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_s is readily determined emperically, and values typically range between 10 and 51 ohms. R_s does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2 R_S C_L$$

7.0 Clock Line Cross Talk

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the MH0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output has to drop at least 2 V_{BE} before Q_3 and Q_4 come on and pull the output back to V^+. A simple method for eliminating or minimizing this effect is to add bleed resistors between the MH0026 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2k and 10k ohms.

8.0 Power Supply Decoupling

Power supply decoupling is a widespread and accepted practice. Decoupling of V^+ to V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each MH0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.

Clock Drivers

MH7803/MH8803 two phase oscillator/clock driver

general description

The MH7803 is a self contained two phase oscillator/clock driver. It requires no external components to generate one of three primary oscillator frequencies and pulse widths. Other frequencies can easily be obtained by programming input voltages. Three sets of outputs are provided: damped and un-damped MOS outputs and TTL monitor outputs. The MOS outputs easily drive 500 pF loads with less than 150 ns rise and fall times. In addition the outputs have current limiting to protect against momentary shorts to the supplies.

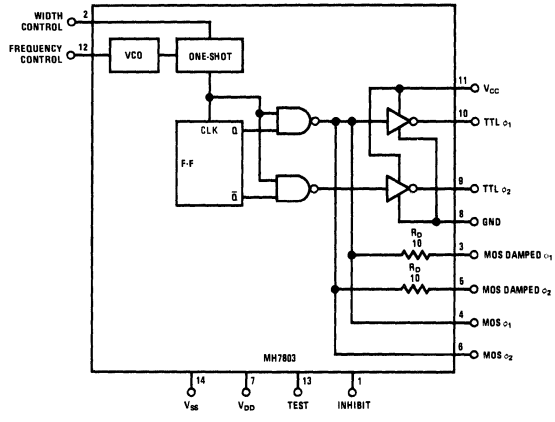
The MH7803 and MH8803 are available in a 14 lead cavity DIP. The MH8803 is also available in a 14 pin molded DIP.

features

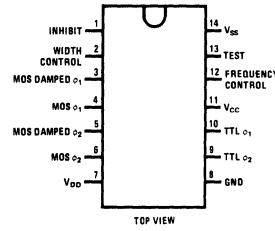
- Two phase non-overlapping outputs
- No external timing components required
- Frequency adjustable from 100 kHz to 500 kHz
- Pulse width adjustable from 260 ns to 1.4μs
- Damped and un-damped MOS outputs
- TTL monitor outputs

5

block and connection diagrams



Dual-In-Line Package



Order Number MH7803J or MH8803J
See Package 9

Order Number MH7803N
See Package 14

absolute maximum ratings

$V_{SS} - V_{DD}$	22V	Operating Temperature Range	
V_{CC} – GND	7.0V	MH7803	–55°C to +125°C
Pulse Width Adjust Voltage	V_{SS} + 0.5V	MH8803	0°C to +70°C
Frequency Adjust Voltage	V_{SS} + 0.5V	Storage Temperature Range	–65°C to +150°C
$V_{SS} - V_{DD}$ Minimum	14V	Lead Temperature (Soldering, 10 seconds)	300°C
Test and Inhibit Input Voltages	V_{SS}		

electrical characteristics (Note 1)

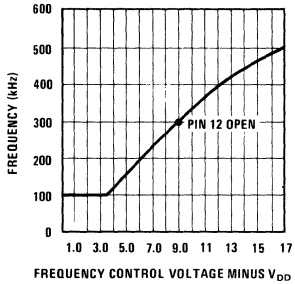
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	Pin 12 at 17V, T_A = 25°C	300	500	600	kHz
	Pin 12 Open, T_A = 25°C	175	300	350	kHz
	Pin 12 at 0V, T_A = 25°C	60	100	150	kHz
Frequency Change from 25°C					
MH7803	Pin 12 at 17V		±20	±30	%
MH8803	Pin 12 at 17V		±10	±15	%
Pulse Width (Note 2)	Pin 2 at 17V, T_A = 25°C	0.2	0.26	0.4	μs
	Pin 2 Open, T_A = 25°C	0.5	0.75	1.3	μs
	Pin 2 at 0V, T_A = 25°C	1.0	1.4	2.6	μs
Pulse Width Change from 25°C					
MH7803	Pin 2 at 17V		±20	±30	%
MH8803	Pin 2 at 17V		±10	±15	%
MOS V_{OH}	I_{OH} = –100μA	V_{SS}–1.1	V_{SS}–0.8		V
MOS V_{OL}	I_{OL} = 2.0 mA		V_{DD}+0.15	V_{DD}+0.5	V
TTL V_{OH}	I_{OH} = –200μA	2.4	3.7		V
TTL V_{OL}					
MH7803	I_{OL} = 2.0 mA		0.17	0.3	V
MH8803	I_{OL} = 3.2 mA		0.2	0.4	V
TTL I_{OS}		3.0	8.0	15	mA
MOS Output Current Limit			70		mA
I_{SS}	Pins 2, 12, 13 at 0V, and Pin 1 at –0.3V		10	17	mA
I_{CC}	Pins 2, 12, at 0V, and Pin 1 at –0.3V		0.75	1.1	mA
R_D					
MH7803		7.0	10	13	Ω
MH8803		5.0	10	15	Ω
MOS t_R, t_f	C_L = 500 pF, T_A = 25°C		100	150	ns
	C_L = 50 pF, T_A = 25°C		20	30	ns

Note 1: These specifications apply for the MH7803 at $V_{SS} - V_{DD}$ = 17V ±10% and over –55°C to +125°C; for the MH8803 at $V_{SS} - V_{DD}$ = 17V ±5% and over 0°C to +70°C unless otherwise specified.

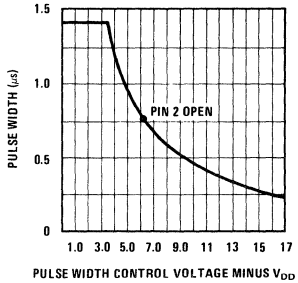
Note 2: The duty cycle can not physically exceed 50% at any output. At high frequencies the frequency adjust pin will affect the pulse width by limiting the duty cycle to slightly less than 50%. Under this condition the pulse width spec does not apply.

typical performance characteristics

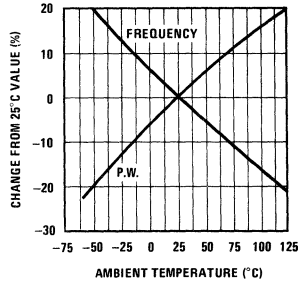
Frequency Control Voltage



Pulse Width Control Voltage

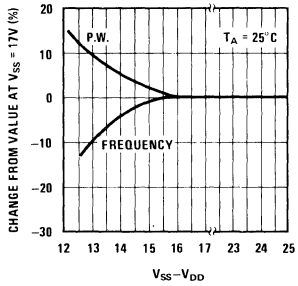


Frequency and Pulse Width vs Temperature

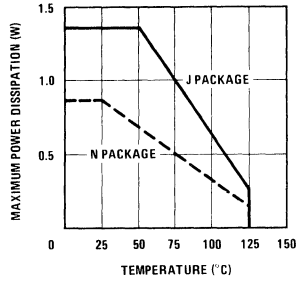


typical performance characteristics (con't)

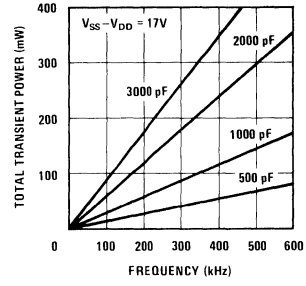
Frequency and Pulse Width vs $V_{SS}-V_{DD}$



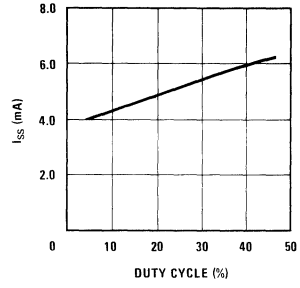
Maximum Package Dissipation



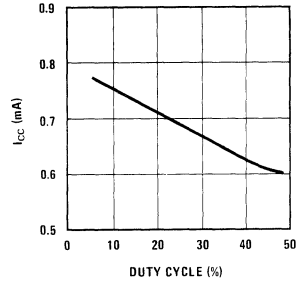
Total Transient Power vs Frequency vs Total C_L



I_{SS} vs Duty Cycle



I_{CC} vs Duty Cycle



applications information

TTL MONITOR OUTPUTS

The TTL outputs are extra functions provided for monitor or synchronization applications. In some systems these outputs may not be required. For these cases the V_{CC} pin may be left open and the TTL circuitry power consumption will be virtually zero.

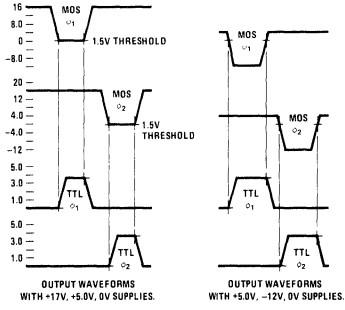
The TTL outputs are slaved to the MOS outputs. Thus the TTL outputs start to switch when the MOS outputs cross the TTL threshold voltage (about 1.5V above ground). Figure 1 depicts the effect of different supply voltages on the TTL waveform when the MOS outputs are driving capacitive loads.

DAMPED MOS OUTPUTS

An extra set of MOS outputs provides a 10 ohm resistor in series with each output line. These resistors give the output pulses an R-C rolloff which tends to minimize ringing or peaking problems associated with board layout.

INHIBIT AND TEST INPUTS

The INHIBIT and TEST inputs are designed to facilitate testing of the device. They were not included in the IC for system use.



(A) (B)

FIGURE 1.

Typically they perform as follows:

INHIBIT Input: in the low state prevents pulses from being initiated on either phase output.

High Level Input:

$$V_{IH} \geq V_{DD} + 2.0V$$

Low Level Input:

$$V_{DD} + 0.2V \geq V_{IL} \geq V_{DD} - 0.5V$$

applications information (con't)

TEST Input: in the low state forces a ONE state on all outputs. The test input should only be used with the INHIBIT input also in the low state.

High Level:

$$V_{IH} \geq V_{DD} + 8.0V$$

Low Level:

$$V_{DD} + 0.5V \geq V_{IL} \geq V_{DD}$$

A pull-up resistor is connected from the TEST pin to V_{SS} internally.

POWER CONSIDERATIONS

Internal power dissipation is affected by three factors:

- dc power
- ac power
- package dissipation capability

The total average power dissipation is the summation of the dc power and ac power. This sum must be less than the maximum package dissipation capability at the particular operating temperature to insure safe operation, i.e.:

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Where

$$P_{AC} = P_{AC\,TTL} + P_{AC\,MOS}$$

$$P_{AC} = [(V_{CC} - GND)^2 \times f \times C_L]_{TTL} + [(V_{SS} - V_{DD})^2 \times f \times C_L]_{MOS}$$

And

$$P_{DC} = (I_{CC}) \times (V_{CC} - GND) + (I_{SS}) \times (V_{SS} - V_{DD})$$

for I_{CC} and I_{SS} selected at the appropriate duty cycle.

For practical cases the $P_{AC\,TTL}$ can be neglected as being very small compared to $P_{AC\,MOS}$.

Thus P_{DISS} is the sum of the MOS transient power (total for both sides of the MH7803) and the standby power of the TTL and MOS sections of the MH7803.

DECOUPLING

It is recommended that each device be decoupled with a 0.1μF capacitor from V_{SS} to V_{DD}. If there is noise on the supply lines, better frequency and pulse width stability can be obtained by connecting a 0.001μF capacitor from the frequency control pin to V_{DD} and another 0.001μF capacitor from the pulse width control pin to V_{DD}.

Clock Drivers

MH8808 dual high speed MOS clock driver

general description

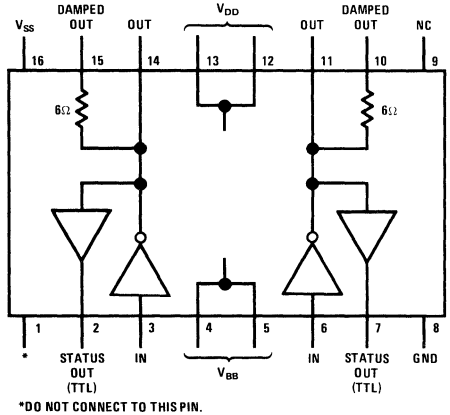
The MH8808 is a high speed dual MOS clock driver intended to drive the two phases of a memory array of 500 pF per phase at rates up to 4.0 MHz. The design includes output current limiting for controlled rise and fall times. Two DTL/TTL compatible status outputs monitor clock outputs and provide a corresponding TTL logic level for status indication. Both direct and internally damped outputs are available for each phase to suite the particular application. It is ideally suited for driving MM5262 2.0k RAMs.

features

- High Speed: 18 ns typ delay and 20 ns typ rise and fall times with 500 pF load
- Current limited outputs ±450 mA typ
- TTL compatible status outputs
- Direct and damped outputs available
- 1W dissipation capability at 25°C T_A
- 16 pin cavity dual-in-line package
- Output high level clamped to +5V

connection diagram

Dual-In-Line Package



*DO NOT CONNECT TO THIS PIN.

TOP VIEW

Order Number MH8808J
See Package 10

absolute maximum ratings

V_{SS}	+7V
$V_{BB} - V_{DD}$	26V
Total Power Dissipation (Note 1)	1W
Operating Temperature Range	0°C to +70°C

electrical characteristics

The following apply for V_{BB} = +8.0V, V_{SS} = +5.0V, V_{DD} = −15V, T_A = 25°C unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	V_{IN} = −9.0V (Note 2)			10	mA
Output Low Voltage	I_{OUT} = +1.0 mA, V_{IN} = −10V (Note 2)	−14			V
Output High Voltage	I_{OUT} = −1.0 mA, V_{IN} = −14V	4.5		5.5	V
Status "1" Voltage	I_{OUT} = −250μA, V_{IN} = −14V	3.0			V
Status "0" Voltage	I_{OUT} = 20 mA, V_{IN} = −10V (Note 2)			0.5	V
Output Damping Resistor (I_{BB})	V_{IN} = −11.5V, V_{SS} = +5.8V, V_{DD} = −17.5V, V_{BB} = +8.5V (Note 2)			37	mA
Output Damping Resistor (I_{SS})	V_{IN} = −11.5V, V_{SS} = +5.8V, V_{DD} = −17.5V, V_{BB} = +8.5V (Note 2)			24	mA
Output Damping Resistor (I_{DD})	V_{IN} = −11.5V, V_{SS} = +5.8V, V_{DD} = −17.5V, V_{BB} = +8.5V (Note 2)			−56	mA
Output Rise Time	C_L = 500 pF			26	ns
Output Fall Time	C_L = 500 pF			26	ns
Delay to Negative-Going Output	C_L = 500 pF	7.0		22	ns
Delay to Positive-Going Output	C_L = 500 pF	10		30	ns

Note 1: Maximum junction temperature is 110°C. For operation above 25°C derate at 85°C/W θ_{JA} for still air.
Note 2: Test only one input high (more positive) at a time.

Analog Switches

MM450/MM550, MM451/MM551
MM452/MM552, MM455/MM555 MOS analog switches

general description

The MM450, and MM550 series each contain four p channel MOS enhancement mode transistors built on a single monolithic chip. The four transistors are arranged as follows:

MM450, MM550	Dual Differential Switch
MM451, MM551	Four Channel Switch
MM452, MM552	Four MOS Transistor Package
MM455, MM555	Three MOS Transistor Package

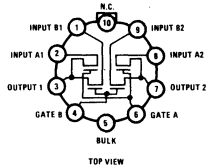
These devices are useful in many airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors (V_{TH} = 2 volts) permits operations with large analog input swings (± 10 volts) at low gate voltages (−20 volts). Significant features, then, include:

- Large Analog Input Swing ±10 Volts
- Low Supply Voltage V_{BULK} = +10 Volts, V_{GG} = −20 Volts
- Low ON Resistance V_{IN} = −10V 150Ω; V_{IN} = +10V 75Ω
- Low Leakage Current 200 pA @ 25°C
- Input Gate Protection
- Zero Offset Voltage

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

schematic and connection diagrams

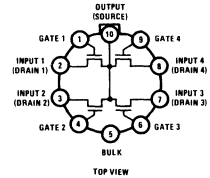
Metal Can Package



Note: Pin 5 connected to case and device bulk.

Order Number MM450H
or MM550H
See Package 24

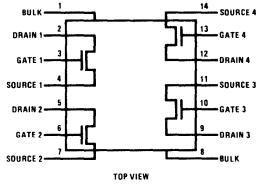
Metal Can Package



Note: Pin 5 connected to case and device bulk.

Order Number MM451H
or MM551H
See Package 24

Flat Package



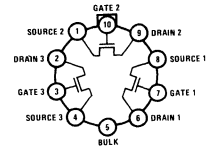
Note 1: Pins 1 and 8 connected to case and device bulk. Drain and Source may be interchanged. MM452F, MM552F.

Note 2: MM452D and MM552D (dual-in-line packages) have same pin connections as MM452F and MM552F shown above.

Order Number MM452D
or MM552D
See Package 2

Order Number MM452F
or MM552F
See Package 26

Metal Can Package



Note: Pin 5 connected to case and device bulk. Drain and Source may be interchanged.

Order Number MM455H
or MM555H
See Package 24

6

absolute maximum ratings

	MM450, MM451, MM452, MM455	MM550, MM551, MM552, MM555
Gate Voltage (V_{GG})	+10V to −30V	+10V to −30V
Bulk Voltage (V_{BULK})	+10V	+10V
Analog Input (V_{IN})	+10V to −20V	+10V to −20V
Power Dissipation	200 mW	200 mW
Operating Temperature	−55°C to +125°C	0°C to +70°C
Storage Temperature	−65°C to +150°C	−65°C to +150°C

electrical characteristics

STATIC CHARACTERISTICS (Note 1)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage				±10	V
Threshold Voltage ($V_{GS(T)}$)	V_{DG} = 0, I_D = 1 μA	1.0	2.2	3.0	V
ON Resistance	V_{IN} = −10V		150	600	Ω
ON Resistance	V_{IN} = V_{SS}		75	200	Ω
OFF Resistance			10^{10}		Ω
Gate Leakage Current (I_{GSB})	V_{GS} = −25V, V_{BS} = 0, T_A = 25°C		20		pA
Input (Drain) Leakage Current					
MM450, MM451, MM452, MM455	T_A = 25°C		0.025	100	nA
	T_A = 85°C		0.002	1.0	μA
	T_A = 125°C		0.025	1.0	μA
Input (Drain) Leakage Current					
MM550, MM551, MM552, MM555	T_A = 25°C		0.1	100	nA
	T_A = 70°C		0.030	1.0	μA
Output (Source) Leakage Current					
MM450, MM451, MM452, MM455	T_A = 25°C		0.040	100	nA
Output (Source) Leakage Current					
MM450	T_A = 85°C			1.0	μA
MM451	T_A = 85°C			1.0	μA
MM452, MM455	T_A = 85°C			1.0	μA
MM450, MM451, MM452, MM455	T_A = 125°C			1.0	μA
Output (Source) Leakage Current					
MM550	T_A = 70°C			1.0	μA
MM551	T_A = 70°C			1.0	μA
MM552, MM555	T_A = 70°C			1.0	μA
DYNAMIC CHARACTERISTICS					
Large Signal Transconductance	V_{DS} = −10V, I_D = 10 mA f = 1 kHz		4000		μmhos

CAPACITANCE CHARACTERISTICS (Note 2)

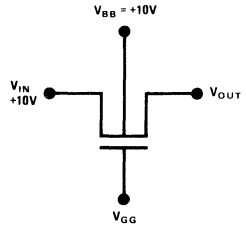
PARAMETER	DEVICE TYPE	MIN	TYP	MAX	UNITS
Analog Input (Drain) Capacitance (C_{DB})	ALL		8	10	pF
Output (Source) Capacitance (C_{SB})	MM450, MM550		11	14	pF
	MM451, MM551		20	24	pF
	MM452, MM552		7.5	11	pF
	MM455, MM555		7.5	11	pF
Gate Input Capacitance (C_{GB})	MM450, MM550		10	13	pF
	MM451, MM551		5.5	8	pF
	MM452, MM552		5.5	9	pF
	MM455, MM555		5.5	9	pF
Gate to Output Capacitance (C_{GS})	ALL		3.0	5	pF

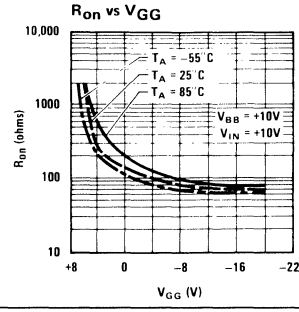
Note 1: The resistance specifications apply for $-55°C \leq T_A \leq +85°C$, V_{GG} = −20V, V_{BULK} = +10V, and a test current of 1 mA. Leakage current is measured with all pins held at ground except the pin being measured which is biased at −25V.

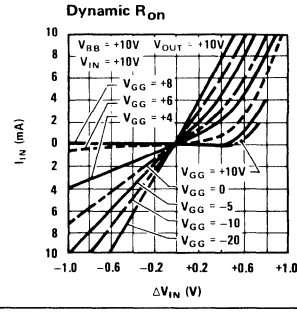
Note 2: All capacitance measurements are made at 0V bias at 1 MHz.

typical dynamic input characteristics (T_A = 25°C Unless Otherwise Noted)

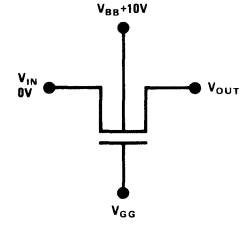
CONDITION 1:
ANALOG INPUT VOLTAGE
AT +10 VOLTS

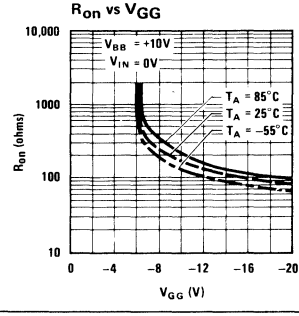


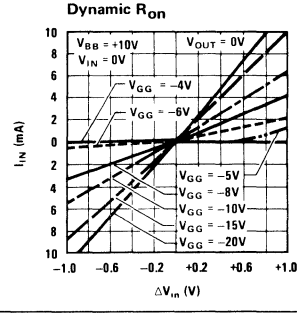




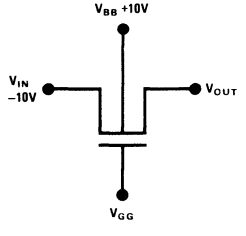
CONDITION 2:
ANALOG INPUT VOLTAGE
AT 0 VOLTS

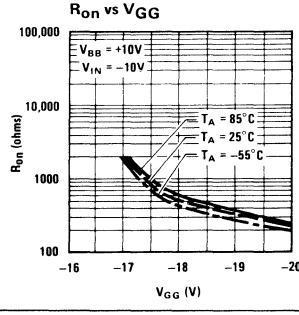


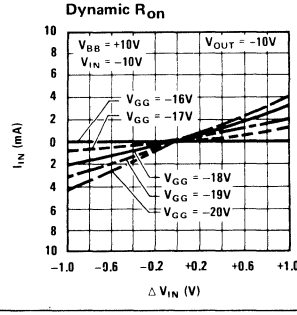


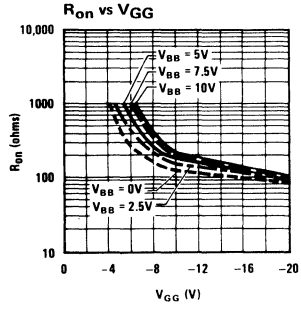


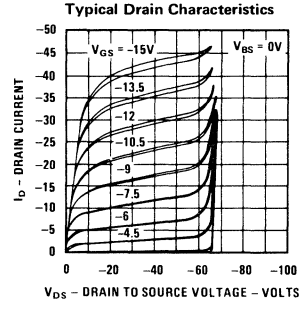
CONDITION 3:
ANALOG INPUT VOLTAGE
AT −10 VOLTS

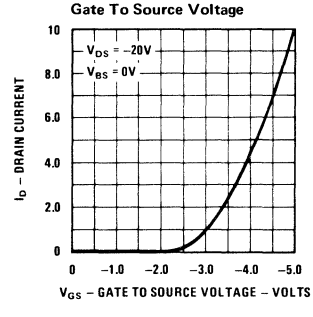








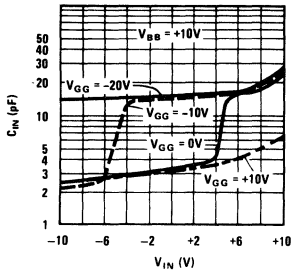




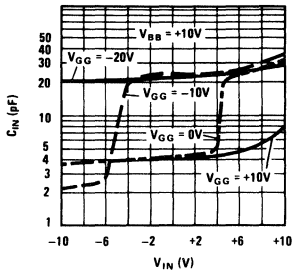
6

typical input capacitances

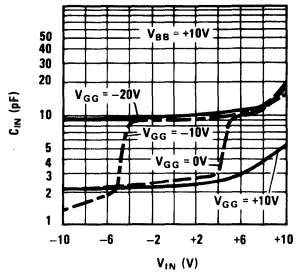
MM450, MM550
C_{IN} vs V_{IN}



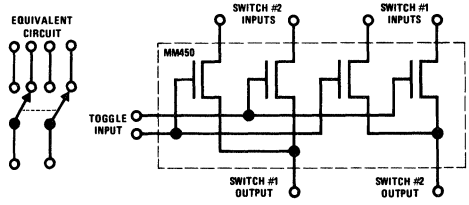
MM451, MM551
C_{IN} vs V_{IN}



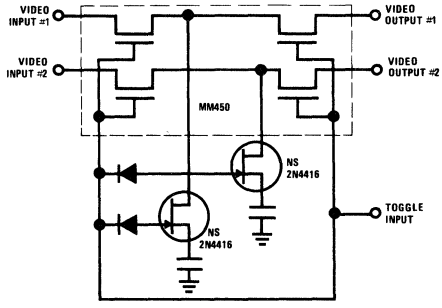
MM452, MM552, MM455, MM555
C_{IN} vs V_{IN}



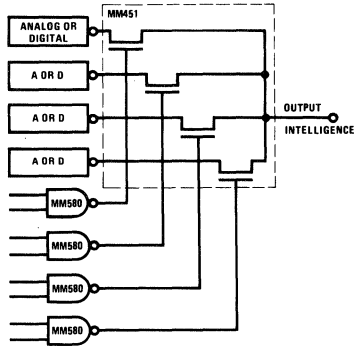
typical applications



DPDT Analog Switch



DPST High-Frequency Switch



4-Channel Multiplexer*

*Expansion in the number of data input lines is possible by using multiple level series switches allowing the same decode gates to be used for all lower rank decoding.

Analog Switches

MM454/MM554 four-channel commutator

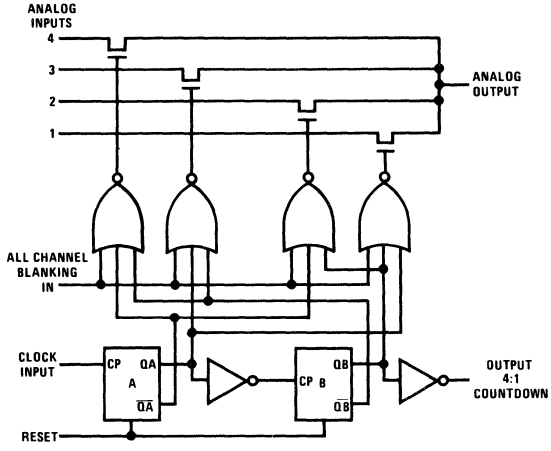
general description

The MM454/MM554 is a four-channel analog commutator capable of switching four analog input channels sequentially onto an output line. The device is constructed on a single silicon chip using MOS P Channel enhancement transistors; it contains all the digital circuitry necessary to sequentially turn ON the four analog switch transistors permitting multiplexing of the analog input data. The device features:

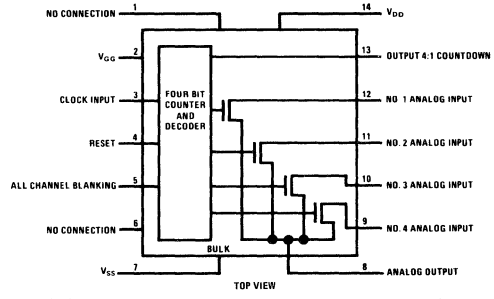
- High Analog Voltage Handling ±10V
- High Commutating Rate 500 kHz
- Low Leakage Current (T_A = 25°C) 200 pA
  (T_A = 85°C) 50 nA
- All Channel Blanking input provided
- Reset capability provided
- Low ON Resistance 200Ω

In addition, the MM454/MM554 can easily be applied where submultiplexing is required since a 4:1 clock countdown signal is provided which can drive the clock input of subsequent MM454/MM554 units.

logic and connection diagrams



Flat Package



Note: Pin 7 connected to case and to device bulk. Nominal Operating Voltages: V_{GG} = −24V; V_{DD} = 0V; V_{SS} = +12V, RESET BIAS = +12V (0V for RESET), ALL CHANNEL BLANKING BIAS = +12V (0V for BLANKING)

Order Number MM454F
or MM554F
See Package 26

absolute maximum ratings (Note 1)

Gate Voltage (V_{GG})	+10V to −30V
Bulk Voltage (V_{SS})	+10V
Analog Input (V_{IN})	+10V to −20V
Power Dissipation	200 mW
Operating Temperature MM454	−55°C to +125°C
MM554	0°C to +70°C
Storage Temperature	−65°C to +150°C

static characteristics (Note 2)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage					±10	V
ON Resistance		V_{IN} = −10V		170	600	Ω
ON Resistance		V_{IN} = V_{SS}		90	200	Ω
OFF Resistance				10^{10}		Ω
Analog Input Leakage Current	MM454	T_A = 25°C		0.050	100	nA
	MM454	T_A = 85°C		0.006	1.0	μA
	MM554	T_A = 25°C		0.0001	100	nA
	MM554	T_A = 70°C		0.030	1.0	μA
Analog Output Leakage Current	MM454	T_A = 25°C		0.100	100	nA
	MM454	T_A = 85°C		30	1.0	μA
	MM554	T_A = 25°C		0.0001	100	nA
	MM554	T_A = 70°C		0.030	1.0	μA
V_{SS} Supply Current Drain		V_{SS} = +12V		3.8	5.5	mA
V_{GG} Supply Current Drain		V_{GG} = −24V		2.4	3.5	mA

capacitance characteristics

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Analog Input Capacitance Channel OFF	I_{IN} = 0		4	6	pF
Analog Input Capacitance Channel ON	I_{IN} = 0		20	24	pF
Analog Output Capacitance	I_{IN} = 0		20	24	pF
Clock Input	V_{CL} = +12V		2.0		pF
Reset Input	V_{RESET} = +12V		2.0		pF
Blanking Input	V_{BLANK} = +12V		2.0		pF

clock characteristics (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Clock Input (HIGH)[4]		V_{SS} − 2		V_{SS}	V
Clock Input (LOW)		−5	0	+5	V
Clock Input Rise Time (POS GOING)		No requirement			
Clock Input Fall Time (NEG GOING)				20	μsec
Countdown Output (POS) V_{OH}		V_{SS} −2		V_{SS}	V
Countdown Output (NEG) V_{OL}			0		V
Maximum Commutation Rate		0.5	2.0		MHz
V_{SS}		+10.0	+12	+14	V

Note 1: Maximum ratings are limiting values above which the device may be damaged. All voltages referenced to V_{DD} = 0.

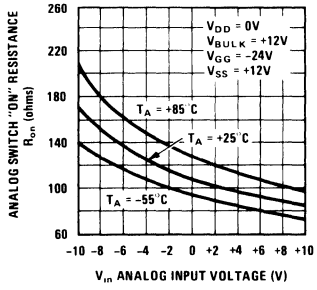
Note 2: These specifications apply over the indicated operating temperature range for V_{GG} = −24V, V_{DD} = 0V, V_{SS} = +12V, V_{RESET} = +12V. ON resistance measured at 1 mA, OFF resistance and leakage measured with all analog inputs and output common. Capacitance measured at 1 MHz.

Note 3: Operating conditions in Note 2 apply. V_{SS} to V_{DD} (0V) voltage is applied to counting and gating circuits. V_{GG} is required only for analog switch biasing. All logic inputs are high resistance and are essentially capacitive.

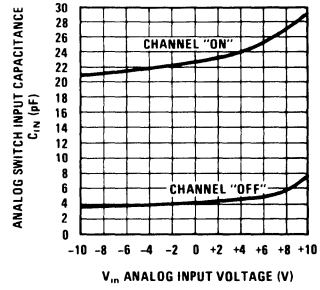
Note 4: Logic input voltage must not be more positive than V_{SS}.

typical performance characteristics

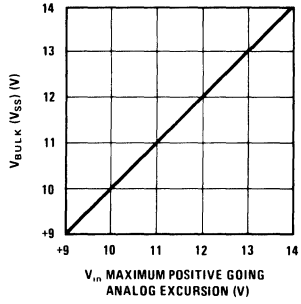
R_{ON} vs Analog Voltage



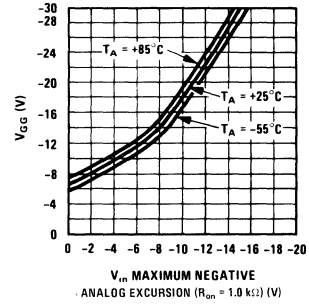
C_{IN} vs V_{IN}



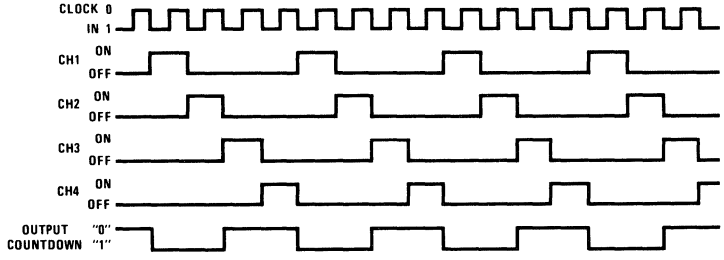
Plus V_{IN} (max) vs V_{BULK}



Minus V_{IN} (max) vs V_{GG}



timing diagram



NOTE: "0" LEVEL = +12V
"1" LEVEL = 0V (GND)

6

Analog Switches

AH0014/AH0014C* DPDT, AH0015/AH0015C quad SPST, AH0019/AH0019C* dual DPST-TTL/DTL compatible MOS analog switches

general description

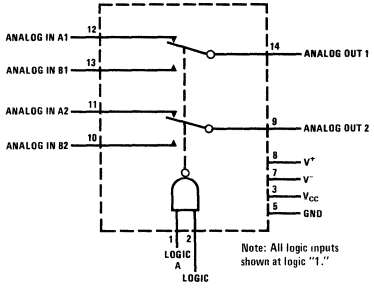
This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors; the second chip is a bipolar I.C. gate and level shifter. The series is available in both hermetic dual-in-line package and flatpack.

features

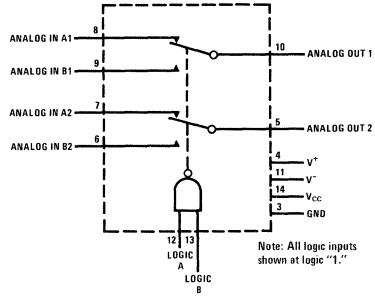
- Large analog voltage switching ±10V
- Fast switching speed 500 ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications. For information on other National analog switches and analog interface elements, see listing on last page.

block and connection diagrams

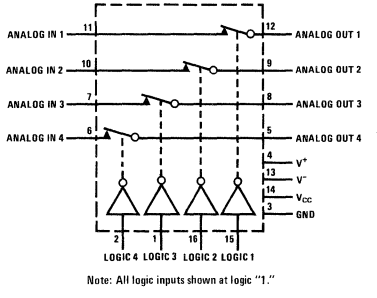


Order Number AH0014F or AH0014CF See Package 26



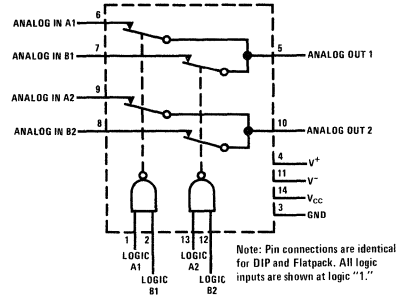
Order Number AH0014D or AH0014CD See Package 2

Quad SPST



Order Number AH0015D or AH0015CD See Package 2

Dual DPST



Order Number AH0019D or AH0019CD See Package 2

Order Number AH0019F or AH0019CF See Package 26

*Previously called NH0014/NH0014C and NH0019/NH0019C

absolute maximum ratings

V_{CC} Supply Voltage	7.0V
V^- Supply Voltage	−30V
V^+ Supply Voltage	+30V
V^+/V^- Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AH0014, AH0015, AH0019	−55°C to +125°C
AH0014C, AH0015C, AH0019C	−25°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 0.4V		0.2	0.4	mA
Power Supply Current Logical "1" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 0V				
AH0014, AH0014C			1.5	3.0	mA
AH0015, AH0015C			0.22	0.41	mA
AH0019, AH0019C			0.22	0.41	mA
Analog Switch ON Resistance – each gate	V_{IN} (Analog) = +10V		75	200	Ω
	V_{IN} (Analog) = −10V		150	600	Ω
Analog Switch OFF Resistance			10^{11}		Ω
Analog Switch Input Leakage Current – each input (Note 4)	V_{IN} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		25	200	pA
	T_A = 125°C		25	200	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.1	10	nA
	T_A = 70°C		30	100	nA
Analog Switch Output Leakage Current – each output (Note 4)	V_{OUT} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		40	400	pA
	T_A = 125°C		40	400	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.05	10	nA
	T_A = 70°C		4	50	nA
Analog Input (Drain) Capacitance	1 MHz @ Zero Bias		8	10	pF
Output Source Capacitance	1 MHz @ Zero Bias		11	13	pF
Analog Turn-OFF Time – t_{OFF}	See test circuit; T_A = 25°C		400	500	ns
Analog Turn-ON Time – t_{ON}	See test circuit; T_A = 25°C				
AH0014, AH0014C			350	425	ns
AH0015, AH0015C			100	150	ns
AH0019, AH0019C			100	150	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for AH0014, AH0015, AH0019 and −25°C to +85°C for AH0014C, AH0015C, AH0019C. V^- = −20V. V^+ = +10V and an analog test current of 1.0 mA unless otherwise specified.

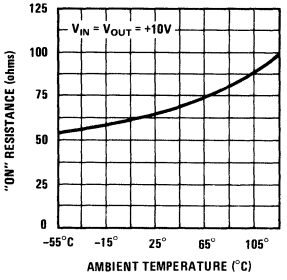
Note 2: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V. V^+ = +10V, V^- = −22V.

Note 3: Current measured is drawn from V_{CC} supply.

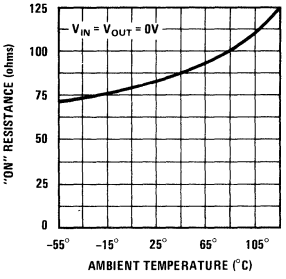
Note 4: All analog switch pins except measurement pin are tied to V^+.

analog switch characteristics (Note 2)

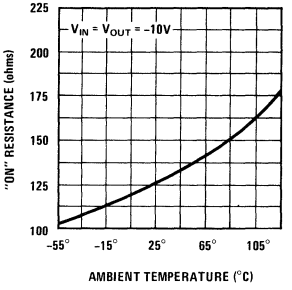
R_{ON} vs Temperature



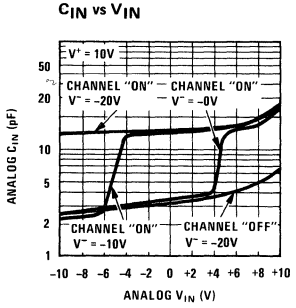
R_{ON} vs Temperature



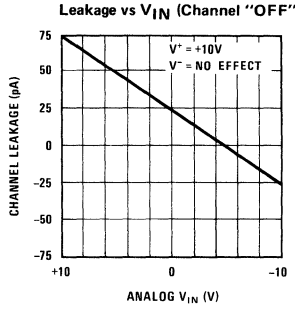
R_{ON} vs Temperature



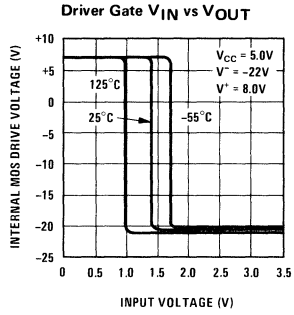
C_{IN} vs V_{IN}



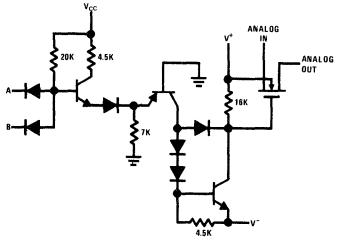
Leakage vs V_{IN} (Channel "OFF")



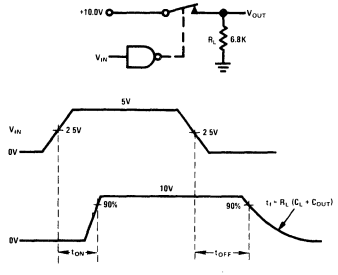
Driver Gate V_{IN} vs V_{OUT}



Schematic (Single Driver Gate and MOS Switch Shown)

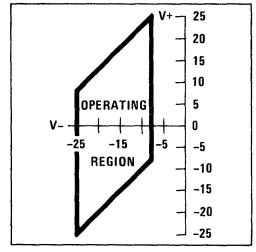


Analog Switching Time Test Circuit



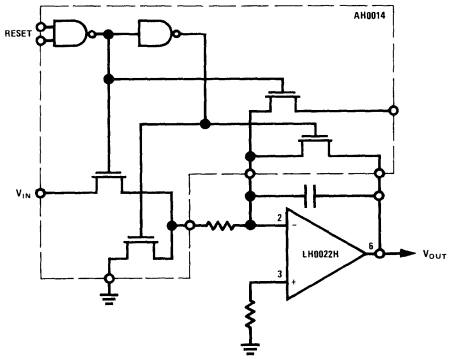
selecting power supply voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V^- is shown on the X axis. It must be between –25V and –8V. The allowable range for power supply V^+ is governed by supply V^-. With a value chosen for V^-, V^+ may be selected as any value along a vertical line passing through the V^- value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.

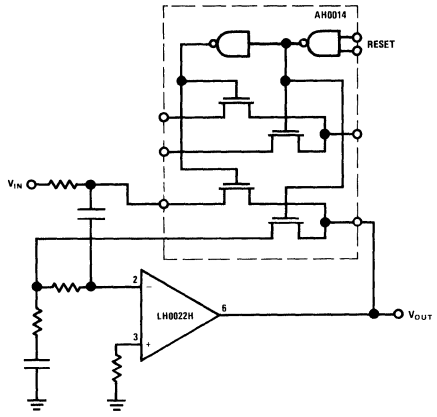


typical applications

Integrator



Reset Stabilized Amplifier



analog switch data sheets

For additional applications information, see the following:

AN-28 High-Speed MOS Commutators, Mrazek
AN-33 Analog-Signal Commutation, Wollesen
AN-38 MOS Analog Switches, Stump/Wollesen

For information on other National analog switches and interface circuits, see the following data sheets:

MOS Analog Switches

Dual Differential – MM450/MM550
Triple – MM455/MM555
Quad – MM452/MM552
Four Channel – MM451/MM551
Four Channel with Commutator – MM454/MM554
Six Channel – AM2009/AM2009C

TTL/DTL Compatible MOS

Eight Channel MUX – AM3705/AM3705C

TTL/DTL Compatible J-FET

Dual DPST
Dual SPST
Dual DPDT (Diff)
SPDT (Diff)
} AH0100/AH0100C Series

High Level Compatible J-FET

DPST – AH2114/AH2114C

Ultra High Speed J-FET

±10V; 30Ω – AM1000
±15V; 50Ω – AM1001
±10V; 100Ω – AM1002

N-Channel Discrete J-FET Switches

5 Ohm – 2N5432
7 Ohm – 2N5433
10 Ohm – 2N5434

Analog Switch Drivers

TTL Dual Level Translator – DM7800/DM8800
TTL Dual High Speed Translator – DH0034/DH0034C
Analog Comparator/Level Translator – LM111 Series

Sample and Hold Circuits

Low Drift Precision – LH0023/LH0023C
High Speed – LH0043/LH0043C

Plus a complete line of amplifiers, comparators, and voltage regulators.

Analog Switches

AH0120/AH0130/AH0140/AH0150/AH0160 series analog switches

general description

The AH0100 series represents a complete family of junction FET analog switches. The inherent flexibility of the family allows the designer to tailor the device selection to the particular application. Switch configurations available include dual DPST, dual SPST, DPDT, and SPDT. $r_{ds(ON)}$ ranges from 10 ohms through 100 ohms. The series is available in both 14 lead flat pack and 14 lead cavity DIP.

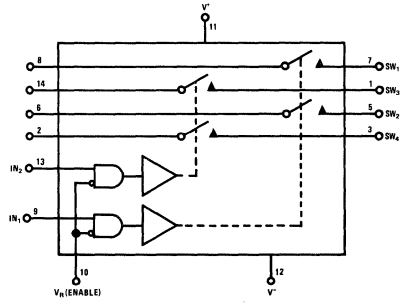
features

- TTL/DTL and RTL compatible logic inputs
- Up to 20V p-p analog input signal
- $r_{ds(ON)}$ less than 10Ω (AH0140, AH0141, AH0145, AH0146)
- Analog signals in excess of 1 MHz
- "OFF" power less than 1 mW
- Gate to drain bleed resistors eliminated
- Fast switching, t_{ON} is typically .4 μs, t_{OFF} is 1.0 μs
- Operation from standard op amp supply voltages, ±15V, available (AH0150/AH0160 series)
- Pin compatible with the popular DG 100 series.

The AH0100 series is designed to fulfill a wide variety of analog switching applications including commutators, multiplexers, D/A converters, sample and hold circuits, and modulators/demodulators. The AH0100 series is guaranteed over the temperature range −55°C to +125°C; whereas, the AH0100C series is guaranteed over the temperature range −25°C to +85°C.

logic and connection diagrams

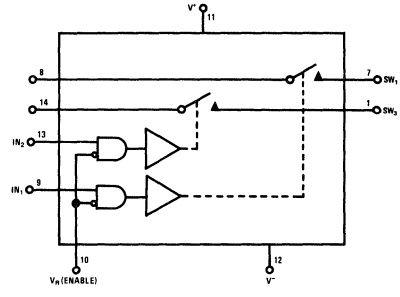
DUAL DPST



HIGH LEVEL (±10V)
AH0140 (10Ω)
AH0129 (30Ω)
AH0126 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0153 (15Ω)
AH0154 (50Ω)

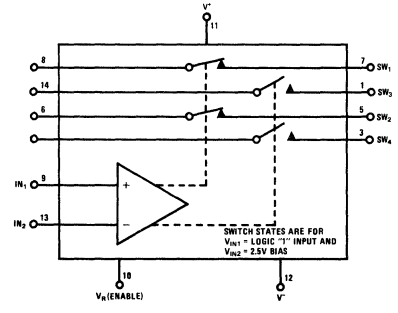
DUAL SPST



HIGH LEVEL (±10V)
AH0141 (10Ω)
AH0133 (30Ω)
AH0134 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0151 (15Ω)
AH0152 (50Ω)

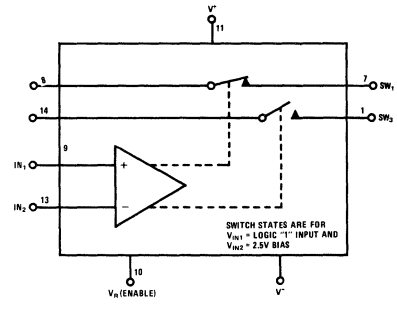
DPDT (Diff)



HIGH LEVEL (±10V)
AH0145 (10Ω)
AH0139 (30Ω)
AH0142 (80Ω)

MEDIUM LEVEL (±7.5)
AH0163 (15Ω)
AH0164 (50Ω)

SPDT (Diff)



HIGH LEVEL (±10V)
AH0146 (10Ω)
AH0144 (30Ω)
AH0143 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0161 (15Ω)
AH0162 (50Ω)

Order Number AH0XXXD
See Package 2

Order Number AH0XXXF
See Package 26

absolute maximum ratings

	High Level	Medium Level
Total Supply Voltage ($V^+ - V^-$)	36V	34V
Analog Signal Voltage ($V^+ - V_A$ or $V_A - V^-$)	30V	25V
Positive Supply Voltage to Reference ($V^+ - V_R$)	25V	25V
Negative Supply Voltage to Reference ($V_R - V^-$)	22V	22V
Positive Supply Voltage to Input ($V^+ - V_{IN}$)	25V	25V
Input Voltage to Reference ($V_{IN} - V_R$)	±6V	±6V
Differential Input Voltage ($V_{IN} - V_{IN2}$)	±6V	±6V
Input Current, Any Terminal	30 mA	30 mA
Power Dissipation		See Curve
Operating Temperature Range AH0100 Series	−55°C to +125°C	
AH0100C Series	0°C to +85°C	
Storage Temperature Range	−65°C to +150°C	
Lead Temperature (Soldering, 10 sec)	300°C	

electrical characteristics for "HIGH LEVEL" Switches (Note 1)

PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DPDT (DIFF)	SPDT (DIFF)	$V^+ = 12.0V$, $V^- = -18.0V$, $V_R = 0.0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	2.0	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	.1	µA
							Over Temp. Range		2.0	µA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	−1.0	−1.8	mA
							Over Temp. Range		−2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	−1.0	−1.4	mA
							Over Temp. Range		−1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	−1.0	−10	µA
							Over Temp. Range		−25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	−1.0	−10	µA
							Over Temp. Range		−25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0126	AH0134	AH0142	AH0143	$V_D = 10V$	$T_A = 25°C$	45	80	Ω
						$I_D = 1$ mA	Over Temp. Range		150	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0129	AH0133	AH0139	AH0144	$V_D = 10V$	$T_A = 25°C$	25	30	Ω
						$I_D = 1$ mA	Over Temp. Range		60	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0140	AH0141	AH0145	AH0146	$V_D = 10V$	$T_A = 25°C$	8	10	Ω
						$I_F = 1$ mA	Over Temp. Range		20	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -10V$	$T_A = 25°C$	.01	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	$V_{DS} = ±20V$	$T_A = 25°C$	0.8	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0140	AH0141	AH0145	AH0146	$V_{DS} = ±20V$	$T_A = 25°C$	4	10	nA
							Over Temp. Range		1.0	µA
Switch Turn-ON Time	t_{ON}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		0.5	0.8	µs
Switch Turn-ON Time	t_{ON}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		0.8	1.0	µs
Switch Turn-OFF Time	t_{OFF}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		0.9	1.6	µs
Switch Turn-OFF Time	t_{OFF}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		1.1	2.5	µs

Note 1: Unless otherwise specified these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

electrical characteristics for "MEDIUM LEVEL" Switches (Note 1)

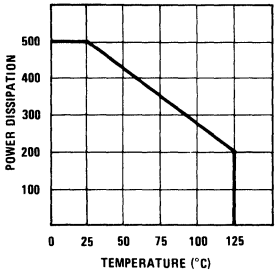
PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DUAL DPDT	SPDT (DIFF)	$V^+ = +15.0V$, $V^- = -15V$, $V_R = 0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	20	60	μA
							Over Temp. Range		120	μA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	0.1	μA
							Over Temp. Range		2	μA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.8	mA
							Over Temp. Range		-2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.4	mA
							Over Temp. Range		-1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	μA
							Over Temp. Range		25	μA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	μA
							Over Temp. Range		-25	μA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	μA
							Over Temp. Range		-25	μA
Switch ON Resistance	$r_{ds(ON)}$	AH0153	AH0151	AH0163	AH0161	$V_D = 7.5V$, $I_D = 1$ mA	$T_A = 25°C$	10	15	Ω
							Over Temp. Range		30	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0154	AH0152	AH0164	AH0162	$V_D = 7.5V$, $I_D = 1$ mA	$T_A = 25°C$	45	50	Ω
							Over Temp. Range		100	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -7.5V$	$T_A = 25°C$	.01	2	nA
							Over Temp. Range		500	nA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0153	AH0151	AH0163	AH0161	$V_{DS} = \pm 15V$	$T_A = 25°C$	5	10	nA
							Over Temp. Range		1.0	μA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0154	AH0152	AH0164	AH0162	$V_{DS} = \pm 15.0V$	$T_A = 25°C$	1.0	2.0	nA
							Over Temp. Range		200	nA
Switch Turn-ON Time	t_{ON}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.8	1.0	μs
Switch Turn-ON Time	t_{ON}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.5	0.8	μs
Switch Turn-OFF Time	t_{OFF}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		1.1	2.5	μs
Switch Turn-OFF Time	t_{OFF}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.9	1.5	μs

Note 1: Unless otherwise specified these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

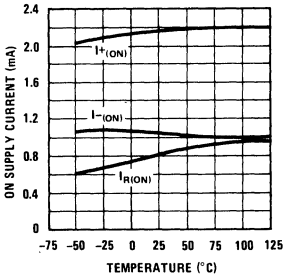
Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

typical performance characteristics

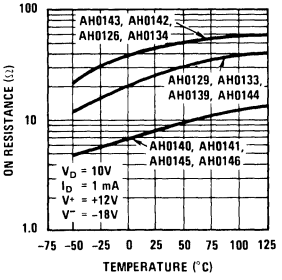
Power Dissipation vs Temperature



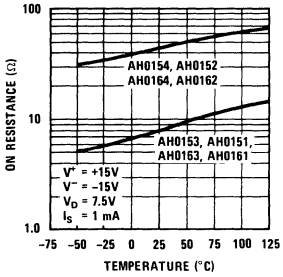
ON Supply Current vs Temperature



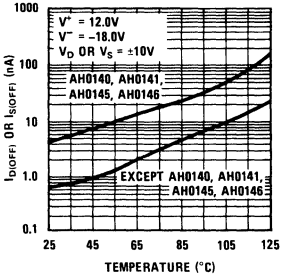
rds(ON) vs Temperature AH0120 thru AH0140 Series



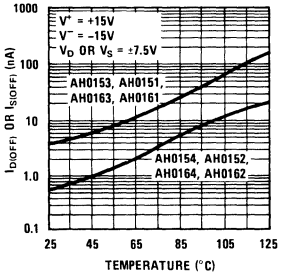
rds(ON) vs Temperature AH0150/AH0160 Series



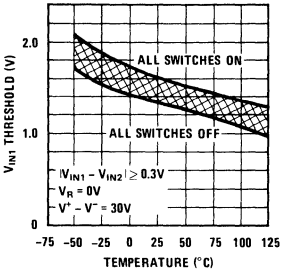
Leakage Current vs Temperature AH0120, AH0130, & AH0140



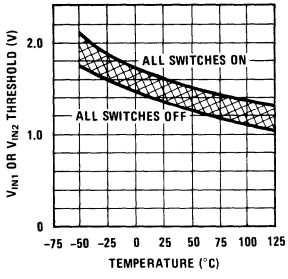
Leakage Current vs Temperature AH0150 & AH0160



Single Ended Switch Input Threshold vs Temperature

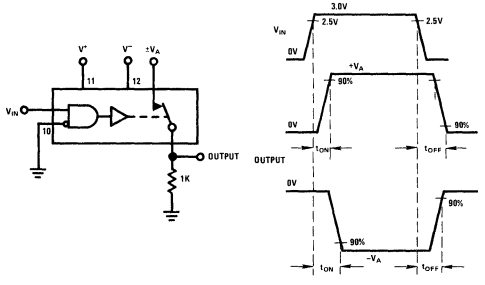


Differential Switch Input Threshold vs Temperature

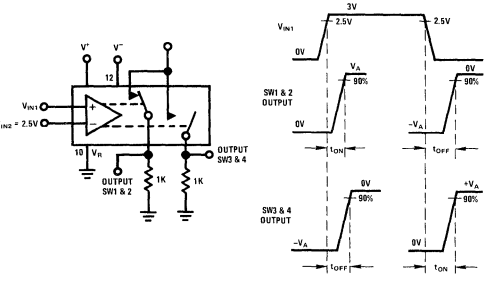


switching time test circuits

Single Ended Input



Differential Input



applications information

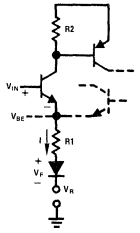
1. INPUT LOGIC COMPATIBILITY

A. Voltage Considerations

In general, the AH0100 series is compatible with most DTL, TTL, and RTL logic families. The ON-input threshold is determined by the V_{BE} of the input transistor plus the V_f of the diode in the emitter leg, plus I x R_1, plus V_R. At room temperature and V_R = 0V, the nominal ON threshold is: 0.7V+0.7V+0.2V, = 1.6V. Over temperature and manufacturing tolerances, the threshold may be as high as 2.5V and as low as 0.8V. The rules for proper operation are:

$V_{IN} - V_R \geq 2.5V$ All switches ON

$V_{IN} - V_R \leq 0.8V$ All switches OFF



B. Input Current Considerations

$I_{IN(ON)}$, the current drawn by the driver with V_{IN} = 2.5V is typically 20 μA at 25°C and is guaranteed less than 120 μA over temperature. DTL, such as the DM930 series can supply 180 μA at logic "1" voltages in excess of 2.5V. TTL output levels are comparable at 400 μA. The DTL and TTL can drive the AH0100 series directly. However, at low temperature, DC noise margin in the logic "1" state is eroded with DTL. A pull-up resistor of 10 kΩ is recommended when using DTL over military temperature range.

If more than one driver is to be driven by a DM930 series (6K) gate, an external pull-up resistor should be added. The value is given by:

$$R_P = \frac{11}{N-1} \text{ for } N > 2$$

where:

R_P = value of the pull-up resistor in kΩ

N = number of drivers.

C. Input Slew Rate

The slew rate of the logic input must be in excess of 0.3V/μs in order to assure proper operation of the analog switch. DTL, TTL, and RTL output rise times are far in excess of the minimum slew rate requirements. Discrete logic designs, however, should include consideration of input rise time.

2. ENABLE CONTROL

The application of a positive signal at the V_R terminal will open all switches. The V_R (ENABLE) signal must be capable of rising to within 0.8V of $V_{IN(ON)}$ in the OFF state and of sinking $I_{R(ON)}$ milliamps in the ON state (at $V_{IN(ON)} - V_R >$ 2.5V). The V_R terminal can be driven from most TTL and DTL gates.

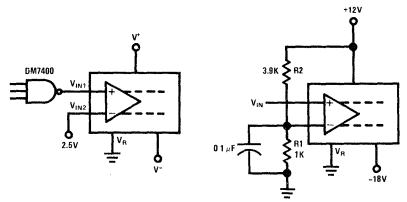
3. DIFFERENTIAL INPUT CONSIDERATIONS

The differential switch driver is essentially a differential amplifier. The input requirements for proper operation are:

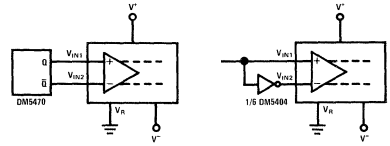
$|V_{IN1} - V_{IN2}| \geq 0.3V$

$2.5 \leq (V_{IN1} \text{ or } V_{IN2}) - V_R \leq 5V$

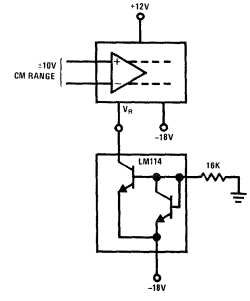
The differential driver may be furnished by a DC level as shown below. The level may be derived from a voltage divider to V^+ or the 5V V_{CC} of the DTL logic. In order to assure proper operation, the divider should be "stiff" with respect to I_{IN2}. Bypassing R1 with a 0.1 μF disc capacitor will prevent degradation of t_{ON} and t_{OFF}.



Alternatively, the differential driver may be driven from a TTL flip-flop or inverter.



Connection of a 1 mA current source between V_R and V^- will allow operation over a ±10V common mode range. Differential input voltage must be less than the 6V breakdown, and input threshold of 2.5V and 300mV differential overdrive still prevail.



4. ANALOG VOLTAGE CONSIDERATIONS

The rules for operating the AH0100 series at supply voltages other than those specified essentially breakdown into OFF and ON considerations. The OFF considerations are dictated by the maximum negative swing of the analog signal and the pinch off of the JFET switch. In the OFF state, the gate of the FET is at $V^- + V_{BE} + V_{SAT}$ or about 1.0V above the V^- potential. The maximum V_P of the FET switches is 7V. The most negative analog voltage, V_A, swing which can be accomodated for any given supply voltage is:

$$|V_A| \leq |V^-| - V_P - V_{BE} - V_{SAT} \text{ or}$$

$$|V_A| \leq |V^-| - 8.0 \text{ or } |V^-| \geq |V_A| + 8.0V$$

For the standard high level switches, $V_A \leq |-18| + 8 = -10V$. The value for V^+ is dictated by the maximum positive swing of the analog input voltage. Essentially the collector to base junction of the turn-on PNP must remain reversed biased for all positive value of analog input voltage. The base of the PNP is at $V^+ - V_{SAT} - V_{BE}$ or $V^+ - 1.0V$. The PNP's collector base junction should have at least 1.0V reverse bias. Hence, the most positive analog voltage swing which may be accommodated for a given value of V^+ is:

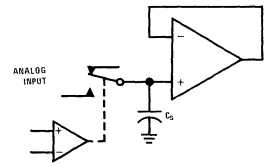
$$V_A \leq V^+ - V_{SAT} - V_{BE} - 1.0V \text{ or}$$

$$V_A \leq V^+ - 2.0V \text{ or } V^+ \geq V_A + 2.0V$$

For the standard high level switches, $V_A = 12 - 2.0V = +10V$.

5. SWITCHING TRANSIENTS

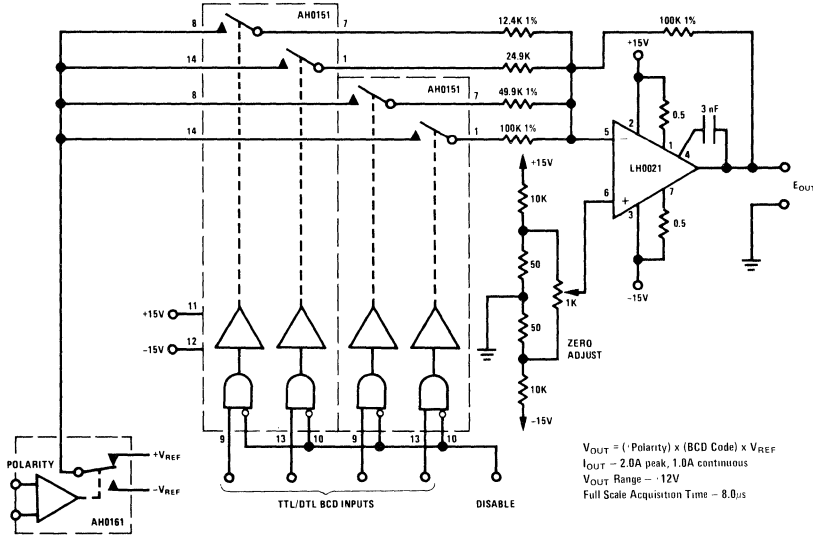
Due to charge stored in the gate-to-source and gate-to-drain capacitances of the FET switch, transients may appear in the output during switching. This is particularly true during the OFF to ON transition. The magnitude and duration of the transient may be minimized by making source and load impedance levels as small as practical.



Furthermore, transients may be minimized by operating the switches in the differential mode; i.e., the charge delivered to the load during the ON to OFF transition is, to a large extent, cancelled by the OFF to ON transition.

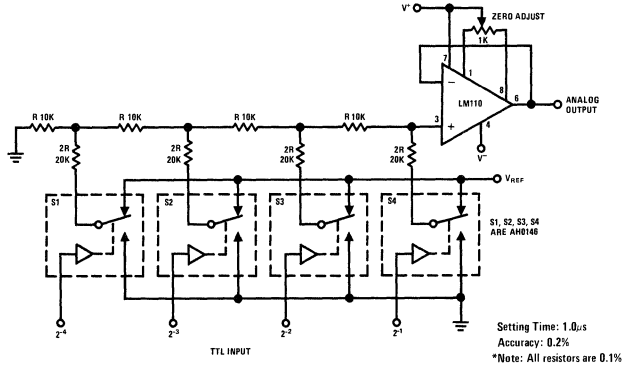
typical applications

Programmable One Amp Power Supply



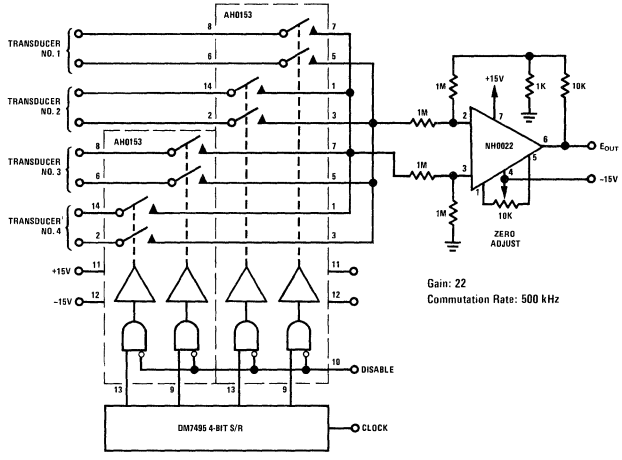
typical applications (con't)

Four to Ten Bit D to A Converter (4 Bits Shown)



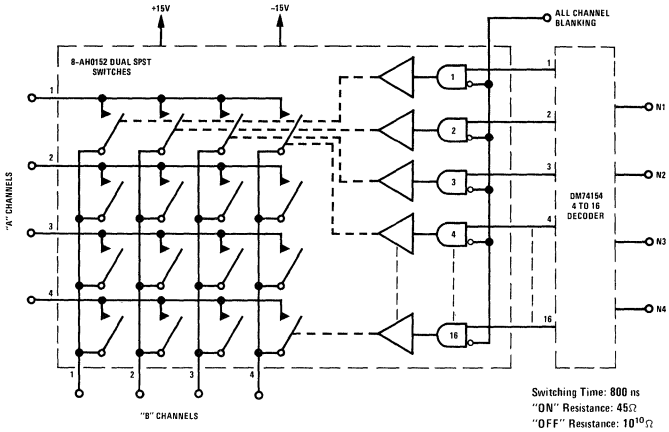
Setting Time: 1.0μs
Accuracy: 0.2%
*Note: All resistors are 0.1%

Four Channel Differential Transducer Commutator



Gain: 22
Commutation Rate: 500 kHz

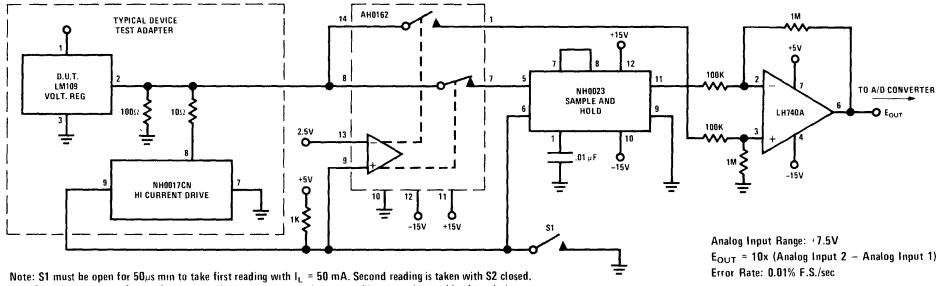
4 x 4 Cross Point Analog Switch



Switching Time: 800 ns
"ON" Resistance: 45Ω
"OFF" Resistance: 10^{10}Ω

typical applications (con't)

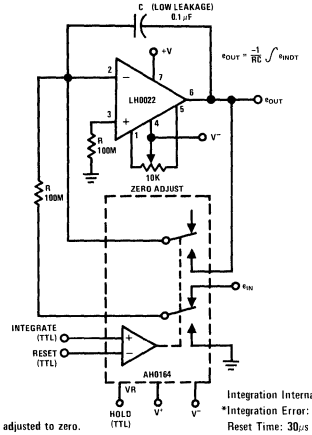
Delta Measurement System for Automatic Linear Circuit Tester



Note: S1 must be open for 50µs min to take first reading with I_L = 50 mA. Second reading is taken with S2 closed. With S1 and other set-up forcing functions under computer control, system will measure line and load regulation on voltage regulators, voltage gain, offset current, CMRR and PSRR on op amps as well as other circuits requiring measurement of the change of a parameter with the change of a forcing function.

Analog Input Range: ±7.5V
E_{OUT} = 10x (Analog Input 2 − Analog Input 1)
Error Rate: 0.01% F.S./sec

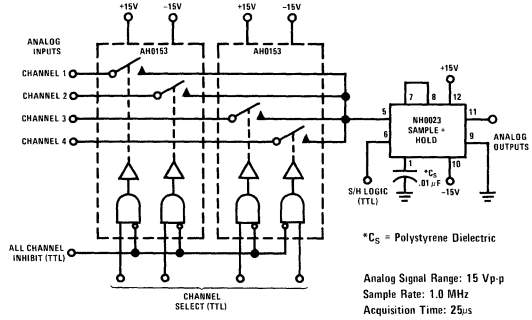
Precision Long Time Constant Integrator with Reset



*Note: V_{OS} adjusted to zero.

Integration Internal: 10 sec
*Integration Error: 100µV
Reset Time: 30µs

Four Channel Commutator

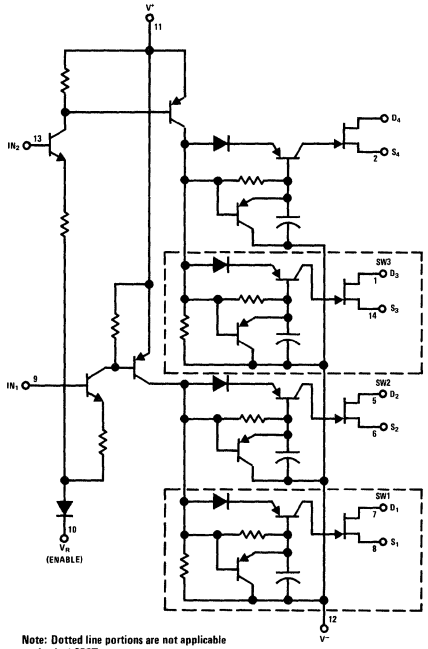


*C_S = Polystyrene Dielectric

Analog Signal Range: 15 Vp-p
Sample Rate: 1.0 MHz
Acquisition Time: 25µs
Drift Rate: 0.5 mV/sec

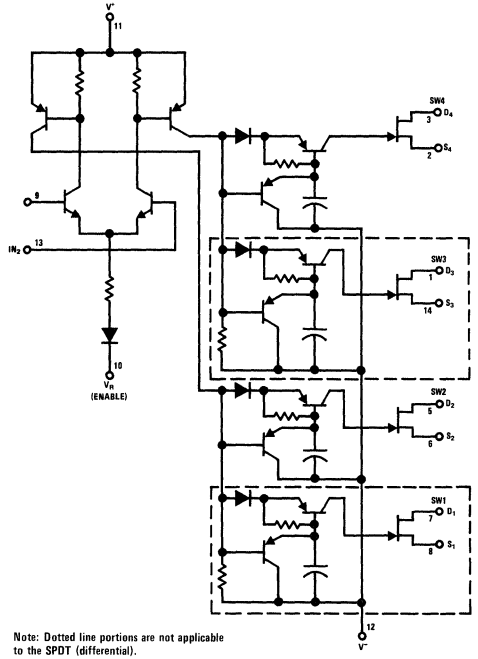
schematic diagrams

DUAL DPST and DUAL SPST



Note: Dotted line portions are not applicable to the dual SPST.

DPDT (diff.) and SPDT (diff.)



Note: Dotted line portions are not applicable to the SPDT (differential).

Analog Switches

AH2114/AH2114C DPST analog switch general description

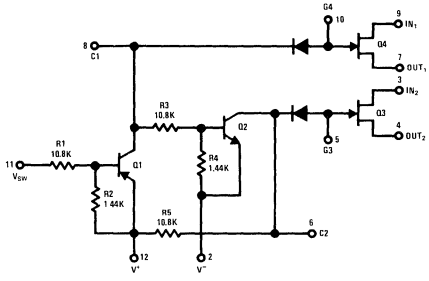
The AH2114 is a DPST analog switch circuit comprised of two junction FET switches and their associated driver. The AH2114 is designed to fulfill a wide variety of high level analog switching applications including multiplexers, A to D Converters, integrators, and choppers.

features

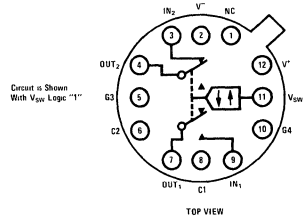
- Low ON resistance, typically 75Ω
- High OFF resistance, typically $10^{11}\Omega$
- Large output voltage swing, typically ±10V
- Powered from standard op-amp supply voltages of ±15V
- Input signals in excess of 1 MHz
- Turn-ON and turn-OFF times typically 1 μs

The AH2114 is guaranteed over the temperature range −55°C to +125°C whereas the AH2114C is guaranteed over the temperature range 0°C to +85°C.

schematic and connection diagrams



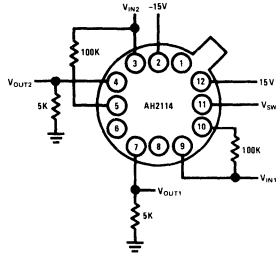
Metal Can Package



TOP VIEW

Order Number AH2114G
or AH2114CG
See Package 25

ac test circuit and waveforms



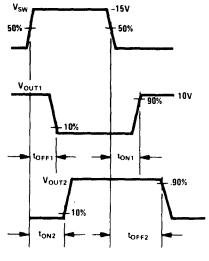
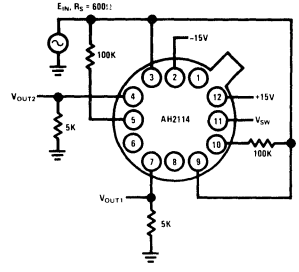


FIGURE 1.



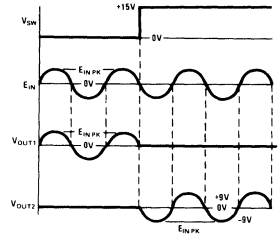


FIGURE 2.

absolute maximum ratings

Vplus Supply Voltage	+25V
Vminus Supply Voltage	−25V
Vplus−Vminus Differential Voltage	40V
Logic Input Voltage	25V
Power Dissipation	1.36W
Operating Temperature Range	
AH2114	−55°C to +125°C
AH2114C	0°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	AH2114			AH2114C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Static Drain-Source "On" Resistance	I_D = 1.0 mA, V_{GS} = 0V, T_A = 25°C		75	100		75	125	Ω
	I_D = 1.0 mA, V_{GS} = 0V			150			160	Ω
Drain-Gate Leakage Current	V_{DS} = 20V, V_{GS} = −7V, T_A = 25°C		0.2	1.0		0.2	5.0	nA
				60			60	nA
FET Gate-Source Breakdown Voltage	I_G = 1.0 μA, V_{DS} = 0V	35			35			V
Drain-Gate Capacitance	V_{DG} = 20V, I_S = 0, f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Source-Gate Capacitance	V_{DG} = 20V, I_D = 0, f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Input 1 Turn-ON Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		3.5	60		3.5	60	ns
Input 2 Turn-ON Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		1.2	1.5		1.2	1.2	μs
Input 1 Turn-OFF Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		0.6	0.75		0.6	0.75	μs
Input 2 Turn-OFF Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		50	80		50	80	ns
DC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V
AC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V

Note 1: Unless otherwise specified these specifications apply for pin 12 connected to +15V, pin 2 connected to −15V, −55°C to +125°C for the AH2114, and 0°C to +85°C for the AH2114C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 100°C/W above +25°C.

Analog Switches

AM1000,AM1001,AM1002 silicon N-channel high speed analog switch

general description

The AM1000 series are junction FET integrated circuit analog switches. These devices commutate faster and with less voltage spiking than any other analog switch presently available. By comparison, discrete JFET switches require elaborate drive circuits to obtain reasonable performance for high toggle rates. Encapsulated in a four pin TO-72 package, these units require a minimum of circuit board area. Switching transients are greatly reduced by a monolithic integrated circuit process. The resulting analog switch device provides the following features:

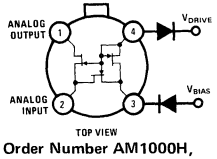
- Low ON Resistance 30Ω
- High Analog Signal Frequency 100 MHz
- High Toggle Rate 4 MHz
- Low Leakage Current 250 pA
- Large Analog Signal Swing ±15V
- Break Before Make Action

The AM1000 series of analog switches are particularly suitable for the following applications:

- High Speed Commutators
- Multiplexers
- Sample and Hold Circuits
- Reset Switching
- Video Switching

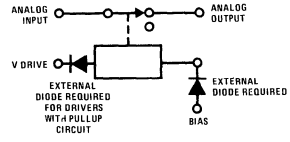
schematic diagram

TO-72 Package



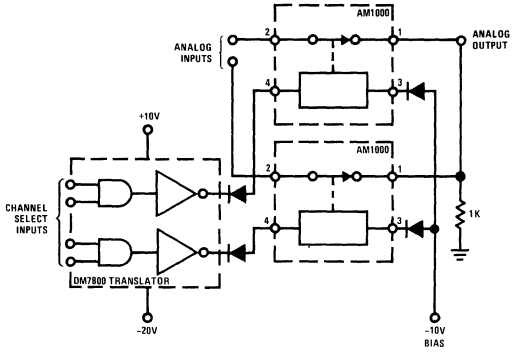
Order Number AM1000H, AM1001H or AM1002H
See Package 22

equivalent circuit

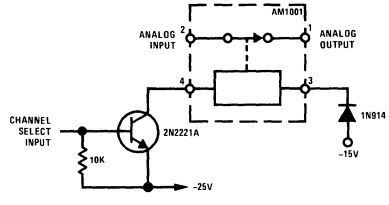


typical applications

±10 Volt Swing Analog Switch 0.5% Accuracy



±15 Volt Swing Analog Switch



absolute maximum ratings

	AM1001	AM1000 AM1002
V_{IN} (Note 1)	+50V	+40V
V_{OUT} (Note 1)	+50V	+40V
V_{DRIVE} (Note 1)	−50V	−40V
V_{BIAS} (Note 1)	+50V	+40V

Power Dissipation @ T_A = 25°C	300 mW
Linear Derating Factor	1.7 mW/°C
Power Dissipation @ T_C = 125°C	150 mW
Linear Derating Factor	6 mW/°C
Maximum Junction Operating Temperature	−55°C to +150°C
Storage Temperature	+200°C
Lead Temperature (Solding, 10 sec)	+300°C

electrical characteristics

ON CHARACTERISTICS (Note 2)

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
R_{ON}	V_{DRIVE} = +15V, V_{BIAS} = −15V I_{IN} = 1 mA, V_{OUT} = 0V	AM1001	20	40	50	Ω
R_{ON}	V_{DRIVE} = +10V, V_{BIAS} = −10V I_{IN} = 1 mA, V_{OUT} = 0V	AM1000 AM1002	20 20	25 50	30 100	Ω Ω

OFF CHARACTERISTICS

PARAMETER	CONDITION	AM1000 AM1001			AM1002			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$I_{OUT(OFF)}$	V_{DRIVE} = −20V, V_{BIAS} = −10V V_{IN} = −10V, V_{OUT} = +10V							
	T_A = +25°C		.05	.25		0.5	1	nA
	T_A = +125°C		.025	.25		0.2	1	μA
$I_{OUT(OFF)}$	V_{DRIVE} = −20V, V_{BIAS} = −10V V_{IN} = +10V, V_{OUT} = −10V							
	T_A = +25°C		.05	.25		0.5	1	nA
	T_A = +125°C		.05	.25		0.2	1	μA

DRIVE CHARACTERISTICS (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
I_{DRIVE} (Switch OFF)	V_{DRIVE} = −20V, V_{BIAS} = −10V AM1000, 1001, 1002 V_{IN} = ±10V, V_{OUT} = ±10V		5	10	mA

SWITCHING CHARACTERISTICS

PARAMETER	CONDITION	AM1000 MAX	AM1001 MAX	AM1002 MAX	UNITS
t_{ON}	See Switching Time Test Circuit	100	150	200	ns
t_{OFF}		100	100	100	ns

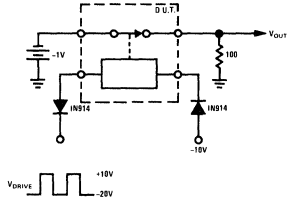
Note 1: The maximum voltage ratings may be applied between any pin or pins simultaneously. Power dissipation may be exceeded in some modes if the voltage pulse exceeds 10 ms. Normal operation will not cause excessive power dissipation even in a "DC" switching application.

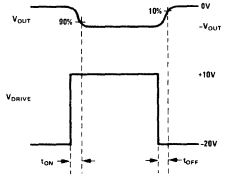
Note 2: All parameters are measured with external silicon diodes. See electrical connection diagram for proper diode placement.

Note 3: I_{BIAS} (Switch OFF) is equal to I_{DRIVE} (Switch OFF). $I_{(BIAS)}$ (Switch ON), is equal to external diode leakage.

Note 4: Rise and fall times of V_{DRIVE} shall be 15 ns maximum for switching time testing.

switching time test circuit and waveforms





Analog Switches

AM2009/AM2009C six channel MOS multiplex switch

general description

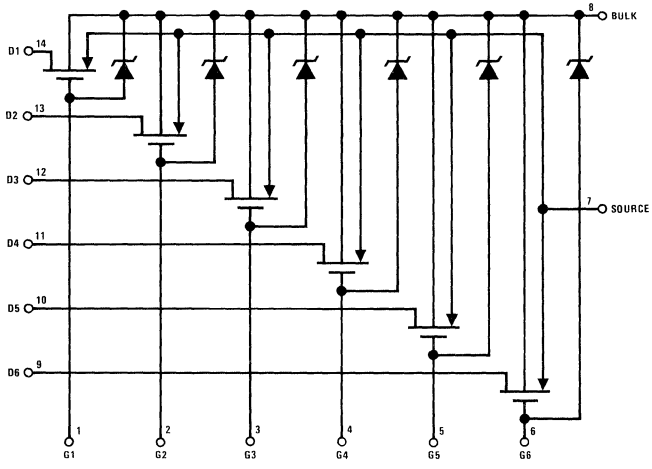
The AM2009/AM2009C is a six channel multiplex switch constructed on a single silicon chip using low threshold P-Channel MOS process. The gate of each MOS device is protected by a diode circuit.

features

- 150 ohms typical low "ON" resistance
- 100 pA typical low "OFF" leakage
- ±10V typical large analog voltage range
- Zero inherent offset voltage
- Normally off with zero gate voltage

The AM2009/AM2009C is designed for applications such as time division multiplexing of analog or digital signals. Switching speeds are primarly determined by conditions external to the device such as signal source impedance, capacitive loading and the total number of channels used in parallel.

schematic diagram

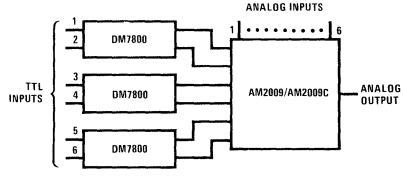


Order Number AM2009D or AM2009CD
See Package 2

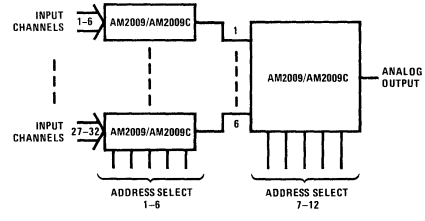
Order Number AM2009F or AM2009CF
See Package 26

typical applications

TTL Compatible 6 Channel MUX



32 Channel MUX



absolute maximum ratings (V_{BULK} = 0V)

Voltage on Any Source or Drain	-30V	Total Power Dissipation (at T_A = 25°C)	900 mW
Voltage on Any Gate	-35V	Power Dissipation — each gate circuit	150 mW
Positive Voltage on Any Pin	+0.3V	Operating Temperature Range AM2009	-55°C to +125°C
Source or Drain Current	50 mA	AM2009C	-25°C to +85°C
Gate Current (forward direction of zener clamp)	0.1 mA	Storage Temperature Range	-65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Threshold Voltage	$V_{GS} = V_{DS}$, $I_{DS} = -1\ \mu A$	-1.0		-3.0	V
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		150	250	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		500	1250	Ω
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$			325	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$			1500	Ω
Gate Leakage	$V_{GS} = -20V$, Note 2			1.0	μA
	$V_{GS} = -20V$, Note 2, $T_A = 25°C$		100		pA
Input Leakage	$V_{DS} = -20V$, Note 2			1.0	μA
	$V_{DS} = -20V$, Note 2, $T_A = 25°C$		100		pA
Output Leakage	$V_{SD} = -20V$, Note 2			3.0	μA
	$V_{SD} = -20V$, Note 2, $T_A = 25°C$		500		pA
Gate-Bulk Breakdown Voltage	$I_{GB} = -10\ \mu A$, Note 2	-35			V
Source-Drain Breakdown Voltage	$I_{SD} = -10\ \mu A$, $V_{GD} = 0$, Note 2	-30			V
Drain-Source Breakdown Voltage	$I_{DS} = -10\ \mu A$, $V_{GS} = 0$, Note 2	-30			V
Transconductance			4000		mhos
Gate Capacitance	Note 3, f = 1 MHz		4.7	8	pF
Input Capacitance	Note 3, f = 1 MHz		4.6	8	pF
Output Capacitance	Note 3, f = 1 MHz		16	20	pF

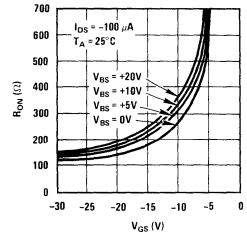
Note 1: Ratings apply over the specified temperature range and V_{BULK} = 0, unless otherwise specified.

Note 2: All other pins grounded.

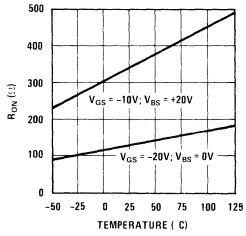
Note 3: Capacitance measured on dual-in-line package between pin under measurement to all other pins. Capacitances are guaranteed by design.

typical performance characteristics

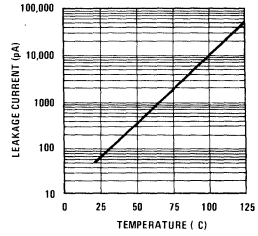
"ON" Resistance vs Gate-to-Source Voltage



"ON" Resistance vs T Temperature



Input Leakage Current vs Temperature



Analog Switches

AM3705/AM3705C 8-channel MOS analog multiplexer

general description

The AM3705/AM3705C is an eight-channel MOS analog multiplex switch. TTL compatible logic inputs that require no level shifting or input pull-up resistors and operation over a wide range of supply voltages is obtained by constructing the device with low threshold P-channel enhancement MOS technology. To simplify external logic requirements, a one-of-eight decoder and an output enable are included in the device.

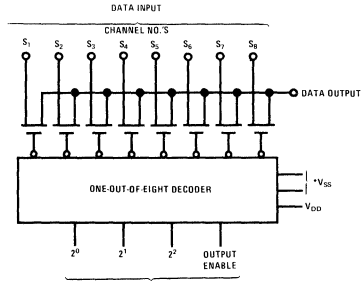
Important design features include:

- TTL/DTL compatible input logic levels
- Operation from standard +5V and −15V supplies
- Wide analog voltage range — ±5V
- One-of-eight decoder on chip
- Output enable control
- Low ON resistance — 150Ω
- Input gate protection
- Low leakage currents — 0.5 nA

The AM3705/AM3705C is designed as a low cost analog multiplex switch to fulfill a wide variety of data acquisition and data distribution applications including cross-point switching, MUX front ends for A/D converters, process controllers, automatic test gear, programmable power supplies and other military or industrial instrumentation applications.

For information on other National analog switches, see listing on last page of this data sheet.

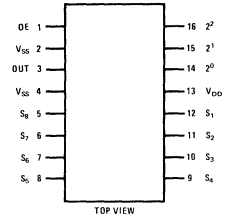
block diagram (MIL-STD-806B)



*Both V_{SS} lines are internally connected; either one or both may be used.

connection diagram

Dual-In-Line and Flat Package



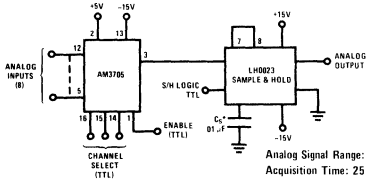
Order Number AM3705D
or AM3705CD
See Package 3

truth table

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

typical applications

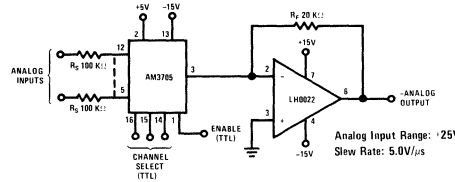
Buffered 8-Channel Multiplex, Sample and Hold



*Polystyrene Dielectric

Analog Signal Range: ±5.0V
Acquisition Time: 25 ns
Drift Rate: 0.5 mV/sec
Aperture Time: 250 ns

Wide Input Range Analog Switch



Analog Input Range: ±25V
Slew Rate: 5.0V/μs

absolute maximum ratings

Positive Voltage on Any Pin (Note 1)		+0.3V
Negative Voltage on Any Pin (Note 1)		−35V
Source to Drain Current		±30 mA
Logic Input Current		±0.1 mA
Power Dissipation (Note 2)		500 mW
Operating Temperature Range	AM3705	−55°C to +125°C
	AM3705C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 3)

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
ON Resistance	R_{ON}	$V_{IN} = V_{SS}$; $I_{OUT} = 100\ \mu A$		80	250	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\ \mu A$		160	400	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\ \mu A$				
AM3705		$T_A = +125°C$			400	Ω
AM3705C		$T_A = +70°C$			400	Ω
ON Resistance	R_{ON}	$V_{IN} = +5V$; $V_{DD} = -15V$; $I_{OUT} = 100\ \mu A$		100		Ω
ON Resistance	R_{ON}	$V_{IN} = 0V$, $V_{DD} = -15V$, $I_{OUT} = -100\ \mu A$		150		Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $V_{DD} = -15V$; $I_{OUT} = -100\ \mu A$		250		Ω
OFF Resistance	R_{OFF}			10^{10}		Ω
Output Leakage Current	I_{LO}	$V_{SS} - V_{OUT} = 15V$		0.5	10	nA
AM3705	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 125°C$		150	500	nA
AM3705C	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 70°C$		35	500	nA
Data Input Leakage Current	I_{LDI}	$V_{SS} - V_{IN} = 15V$		0.1	3.0	nA
AM3705	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 125°C$		25	500	nA
AM3705C	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 70°C$		0.5	500	nA
Logic Input Leakage Current	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$		.001	1	μA
AM3705	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 125°C$		.05	10	μA
AM3705C	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 70°C$		.05	10	μA
Logic Input LOW Level	V_{IL}	$V_{SS} = +5.0V$		0.5	1.0	V
Logic Input LOW Level	V_{IL}		V_{DD}		$V_{SS} - 4.0$	V
Logic Input HIGH Level	V_{IH}	$V_{SS} = +5.0V$	3.0	3.5		V
Logic Input HIGH Level	V_{IH}		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
Channel Switching Time-Positive	t^+	Switching Time Test Circuit		300		ns
Channel Switching Time-Negative	t^-	Switching Time Test Circuit		600		ns
Channel Separation		f = 1 kHz		62		dB
Output Capacitance	C_{db}	$V_{SS} - V_{OUT} = 0$; f = 1 MHz		35		pF
Data Input Capacitance	C_{sb}	$V_{SS} - V_{DIP} = 0$; f = 1 MHz		6.0		pF
Logic Input Capacitance	C_{cg}	$V_{SS} - V_{Logic\ In} = 0$; f = 1 MHz		6.0		pF
Power Dissipation	P_D	$V_{DD} = -31V$, $V_{SS} = 0V$		125	175	mW

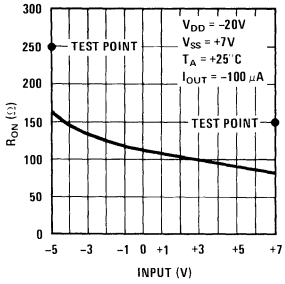
Note 1: All voltages referenced to V_{SS}.

Note 2: Rating applies for ambient temperatures to +25°C, derate linearly at 3.0 mW/°C for ambient temperatures above +25°C.

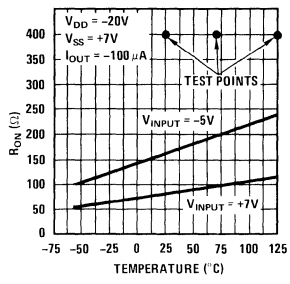
Note 3: Specifications apply for $T_A = 25°C$, $-24V \leq V_{DD} \leq -20V$, and $+5.0V \leq V_{SS} \leq +7.0V$; unless otherwise specified (all voltages are referenced to ground).

typical performance characteristics

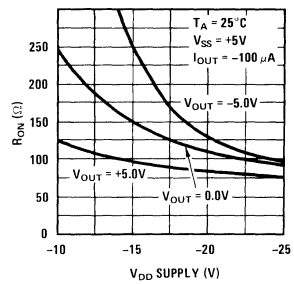
ON Resistance vs Analog Input Voltage



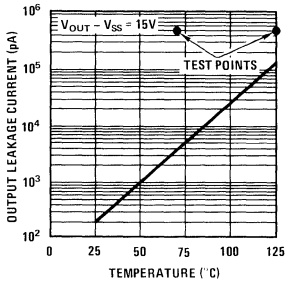
ON Resistance vs Ambient Temperature



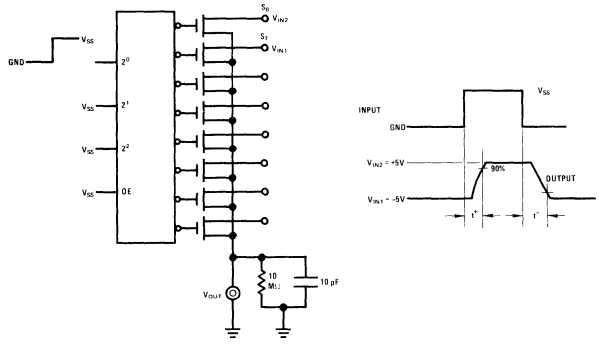
ON Resistance vs V_{DD} Supply Voltage



Output Leakage Current vs Ambient Temperature

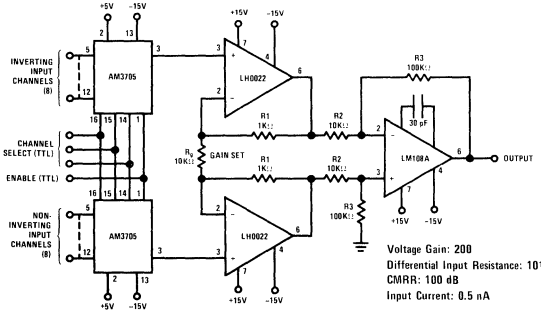


switching time test circuit

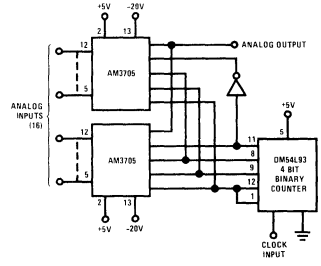


typical applications (con't.)

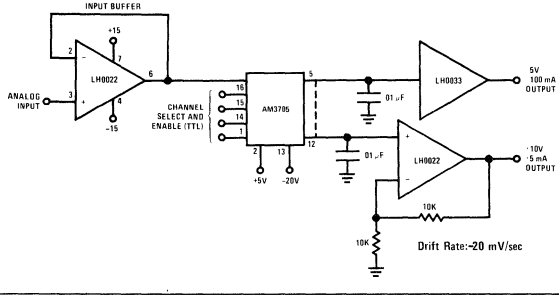
Differential Input MUX



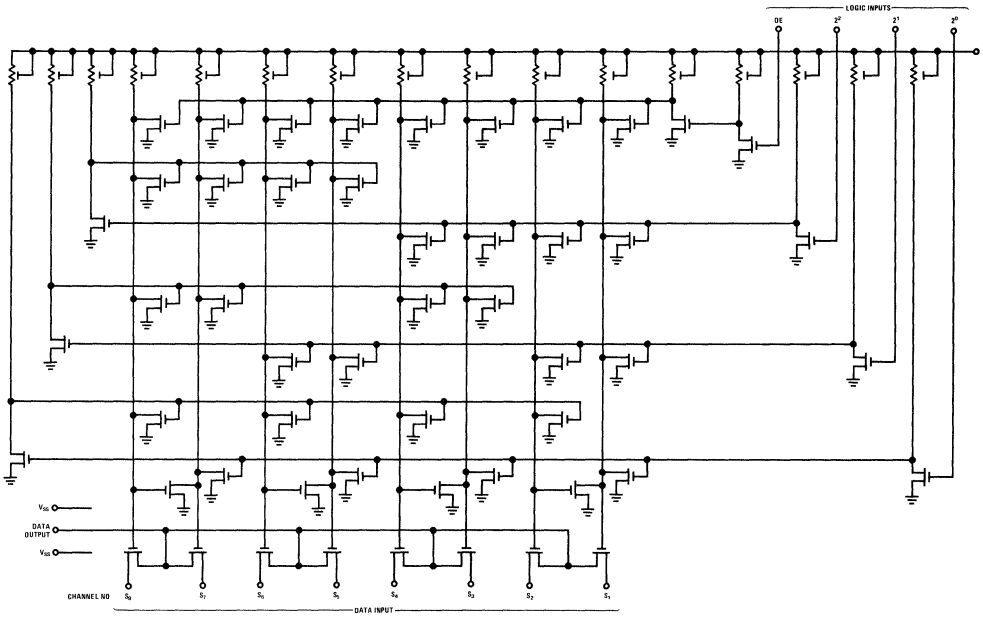
16-Channel Commutator



8-Channel Demultiplexer with Sample and Hold



schematic diagram



analog switch data sheets

For specifications on other National analog switches and analog interface circuits, see the following data sheets:

MOS Analog Switches

Dual Differential – MM450/MM550
Triple – MM455/MM555
Quad – MM452/MM552
Four Channel – MM451/MM551
Four Channel with Commutator – MM454/MM554
Six Channel – AM2009/AM2009C

TTL/DTL Compatible MOS

DPDT – AH0014/AH0014C
Quad SPST – AH0015/AH0015C
DPST – AH0019/AH0019C

TTL/DTL Compatible J-FET

Dual DPST, Dual SPST, Dual DPDT (Diff), SPDT (Diff) – AH0100/AH0100C Series

High Level Compatible J-FET

DPST – AH2114/AH2114C

Ultra High Speed J-FET

±10V; 30Ω – AM1000
±15V; 50Ω – AM1001
±10V; 100Ω – AM1002

N-Channel Discrete J-FET Switches

5 Ohm – 2N5432
7 Ohm – 2N5433
10 Ohm – 2N5434

ANALOG SWITCH DRIVERS

TTL Dual Level Translator – DM7800/DM8800
TTL Dual High Speed Translator – DH0034/DH0034C
Analog Comparator/Level Translator – LM111 Series

SAMPLE AND HOLD CIRCUITS

Low Drift Precision – LH0023/LH0023C
High Speed – LH0043/LH0043C

Plus a complete line of amplifiers comparators and voltage regulators.

ROM Character Generators

MM4220NP/MM5220NP, MM4230NN/MM5230NN, MM4230NO/MM5230NO, 7×9 horizontal scan display character generator

general description

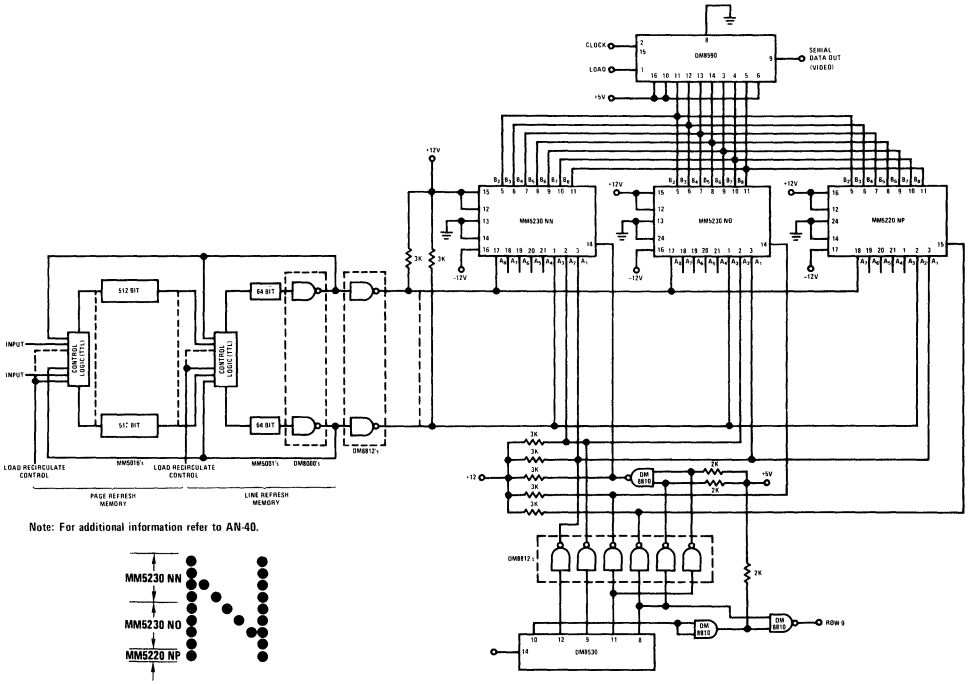
The MM4220NP/MM5220NP is a 1024-bit read-only memory and the MM4230NN/MM5230NN and MM4230NO/MM5230NO are 2048-bit read-only memories programmed to generate a font of 64 7x9 dot-type raster or horizontal-scan characters.

The typical application shows the ASCII-address system. The display refresh memory, built with MOS dynamic shift registers, and the TTL control techniques are similar to those described in *Application Note AN-40*. Designs for vertical-scan fonts, printer character generators, and designs for fonts larger than 7x9 are also outlined in *AN-40*.

For full electrical, environmental and mechanical details, refer to the MM4220/MM5220 and MM4230/MM5230 data sheets.

typical application

7x9 Character Generator System



Note: For additional information refer to AN-40.

Order Number MM4220NP/J, MM5220NP/J, MM4230NN/J, MM5230NN/J, MM4230NO/J, or MM5230NO/J
See Package 11

Order Number MM5220NP/N, MM5230NN/N, or MM5230NO/N
See Package 18

character font

Note: Input addresses are in six bit ASCII code and are shown in the sequence A_0, A_1 ... A_5.

ROM Character Generators

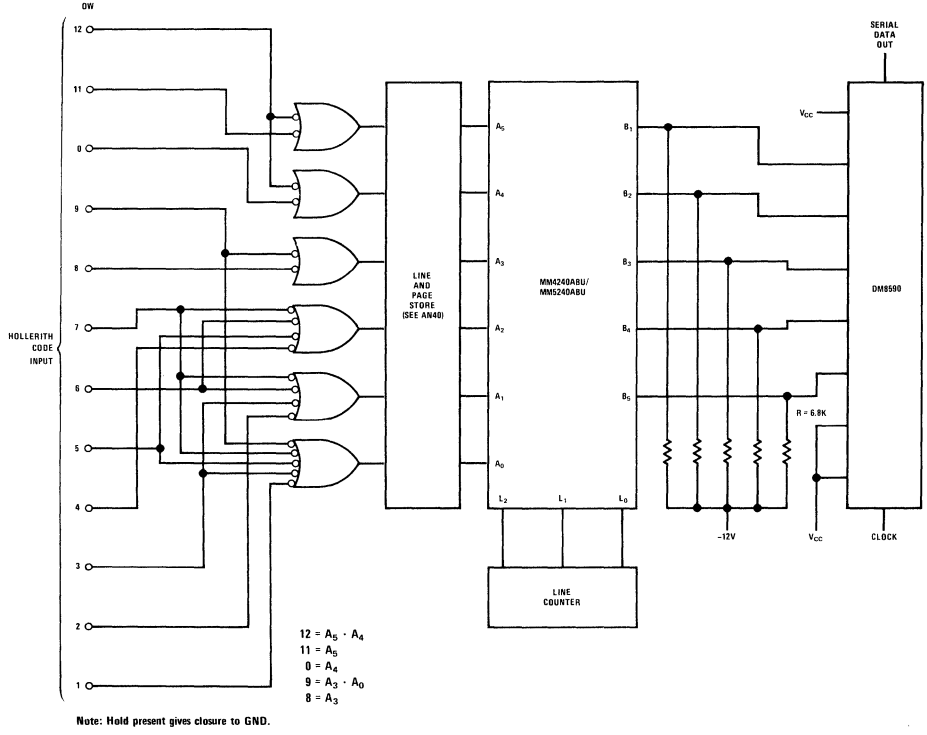
MM4240ABU/MM5240ABU hollerith character generator

general description

The MM4240ABU/MM5240ABU is a 64 x 8 x 5 read-only memory programmed to display a 64-character subset of the Hollerith 12-line code, normally used in punching 80 column cards. Compression from 12 lines to the six needed to make up a 64-character set may be accomplished as shown in the typical application.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

typical application



Note: Hold present gives closure to GND.

Order Number MM4240ABU/J or MM5240ABU/J
See Package 11
Order Number MM5240ABU/N
See Package 18

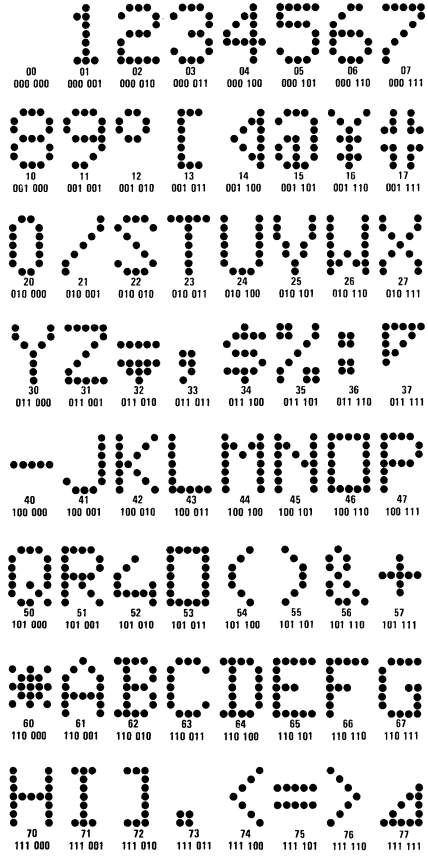
7

code table

HOLLERITH INPUT CODE (NON-COMPRESSED)				OCTAL SEQUENCE	GRAPHIC DISPLAY
				00	(space)
			1	01	1
			2	02	2
			3	03	3
			4	04	4
			5	05	5
			6	06	6
			7	07	7
		8		10	8
	9			11	9
		8	2	12	
		8	3	13	
		8	4	14	
		8	5	15	
		8	6	16	
		8	7	17	
				20	
	0			21	0
	0		1	22	/
	0		2	23	S
	0		3	24	T
	0		4	25	U
	0		5	26	V
	0		6	27	W
	0		7	28	X
	0	8		30	Y
	0	9		31	Z
	0	8	2	32	
	0	8	3	33	
	0	8	4	34	
	0	8	5	35	
	0	8	6	36	
	0	8	7	37	
	11			40	
	11		1	41	J
	11		2	42	K
	11		3	43	L
	11		4	44	M
	11		5	45	N
	11		6	46	O
	11		7	47	P
	11	8		50	Q
	11	9		51	R
	11	8	2	52	
	11	8	3	53	
	11	8	4	54	
	11	8	5	55	
	11	8	6	56	
	11	8	7	57	
12				60	
12			1	61	A
12			2	62	B
12			3	63	C
12			4	64	D
12			5	65	E
12			6	66	F
12			7	67	G
12		8		70	H
12		9		71	I
12		8	2	72	
12		8	3	73	. (period)
12		8	4	74	
12		8	5	75	
12		8	6	76	
12		8	7	77	

character font

MM4240ABU/MM5240ABU



ROM Character Generators

MM4240ABZ/MM5240ABZ EBCDIC-8 character generator

general description

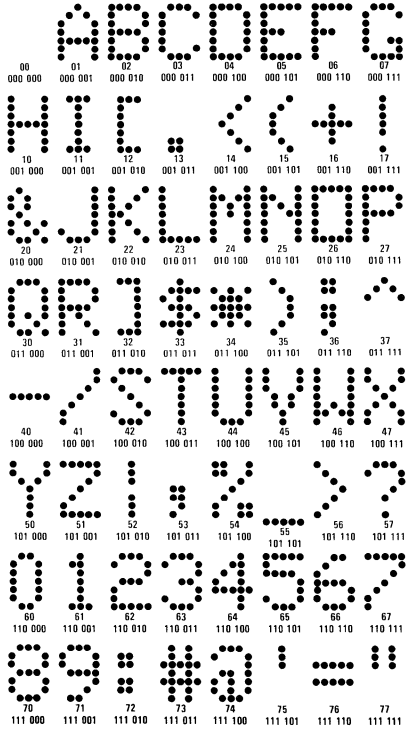
The MM4240ABZ/MM5240ABZ is a 64 x 8 x 5 read only memory that has been programmed to display the 64 character graphic subset of EBCDIC-8, an Extended Binary Coded Decimal Interchange Code with character assignments and locations conforming to the American Standard x 3.26-1970 (see MM5230QX data sheet for full EBCDIC-8 table).

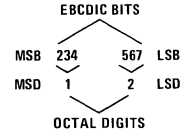
Compression of the eight bits of EBCDIC-8 to the six needed for a 64-character subset is accomplished by simply ignoring the two most significant EBCDIC bits, bit 0 and bit 1.

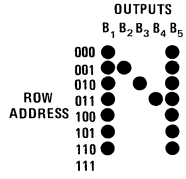
The octal character address digits are then formed as shown below.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

character font







Order Number MM4240ABZ/J or MM5240ABZ/J
See Package 11

Order Number MM5240ABZ/N
See Package 18

7

ROM Character Generators

MM4240ACA/MM5240ACA EBCDIC character generator

general description

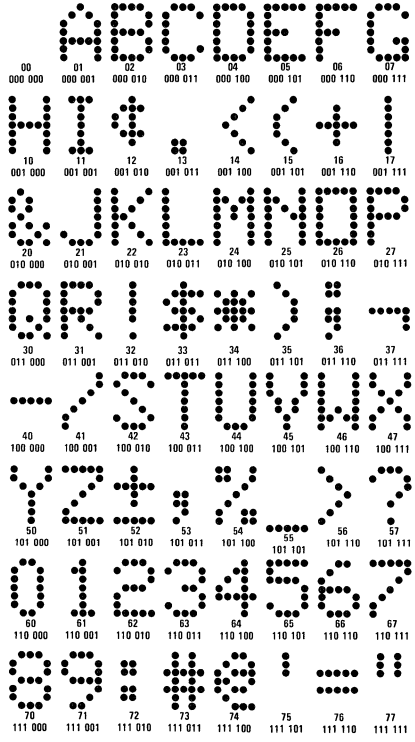
The MM4240ACA/MM5240ACA is a 64 x 8 x 5 read only memory that has been programmed to display the 64 character graphic subset of EBCDIC, an Extended Binary Coded Decimal Interchange code typically used in IBM systems.

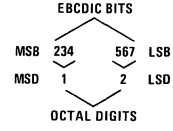
Compression of the eight bits of EBCDIC to the six needed for a 64-character subset is accomplished by simply ignoring the two most significant EBCDIC bits, bit zero and bit one.

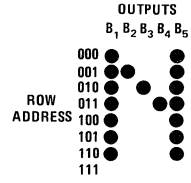
The octal character address digits are then formed as shown below.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

character font







Order Number MM4240ACA/J or MM5240ACA/J
See Package 11

Order Number MM5240ACA/N
See Package 18

ROM Code Converters

SK0003 sine/cosine look-up table kit general description

The SK0003 Sine/Cosine Look-Up Table Kit consists of four MOS ROMs: three MM4210/MM5210's and one MM4220/MM5220-1024 bit static read only memories. They are P-channel enhancement mode monolithic MOS integrated circuits utilizing a low threshold technology.

THE SINE FUNCTION

The SK0003 implements the equation $\sin\theta$ = sin M cos L + cos M sin L. Cos L was assumed to be 1 in the equation. However, it is a variable between 1 and 0.99998 and is a function of round off error. Worst case error is 1–5/8 bits in LSB at address 1415 (62.25°). The error increases from zero to .002% every 8 bits, therefore, the MM4220/MM5220 provides the error correction factor $\cos(M - 2.81^\circ)$ sin L in the equation $\sin\theta = \sin M + \cos(M - 2.81^\circ)$ sin L. The circuitry to perform this function is shown in Figure 1. Additional information is available in *MOS Brief 10.*

THE COSINE FUNCTION

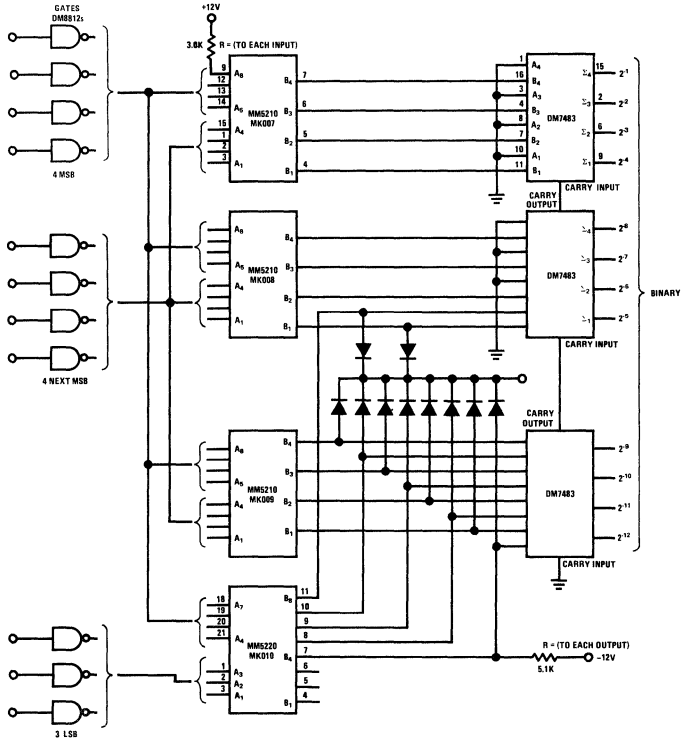
To generate the cosine function $\cos\theta = \sin(\theta - 90^\circ)$, the input must be complemented and a logical "1" added. Figure 2A is a logic diagram of the circuitry used to provide the cosine function, as well as providing both sine and cosine functions in the same system. 11-bit resolution and 12-bit accuracy ±1–5/8-bits is achieved in this configuration.

A reduction in logic can be achieved as shown in Figure 2B if a loss in resolution of 1/2-bit in an 11-bit input or 1/4-bit in a 10-bit input is acceptable.

ELECTRICAL CHARACTERISTICS

Refer to the appropriate data sheet for each device shown in the figures. The devices noted are: MM4210/MM5210, MM4220/MM5220, DM5483/DM7483, DM7812/DM8812 and DM5486/DM7486.

logic diagram



Order Number SK0003C
or
Order Number SK0003M

FIGURE 1. SK0003 Logic Diagram (Kit Includes ROMs Only). This Circuit Provides 11-Bit Resolution and 12-Bit Accuracy in a θ to Sin θ Converter.

logic diagram

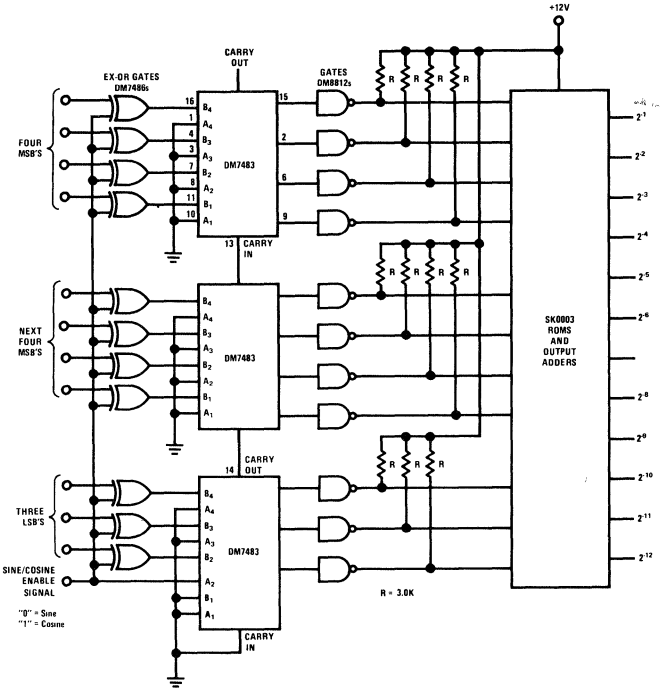


FIGURE 2A. Sine/Cosine Conversion Provides 11-Bit Resolution, 12-Bit ±1-5/8 Bit Accuracy.

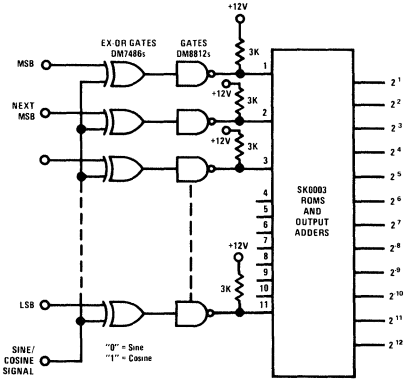


FIGURE 2B. Sine/Cosine Conversion with Cosine Approximated. (Cosine Conversion has 10-Bits Input Resolution and 12-Bit ±1-5/8-Bit Accuracy.)

ROM Code Converters

MM4220AE/MM5220AE ASCII-7 to hollerith code converter

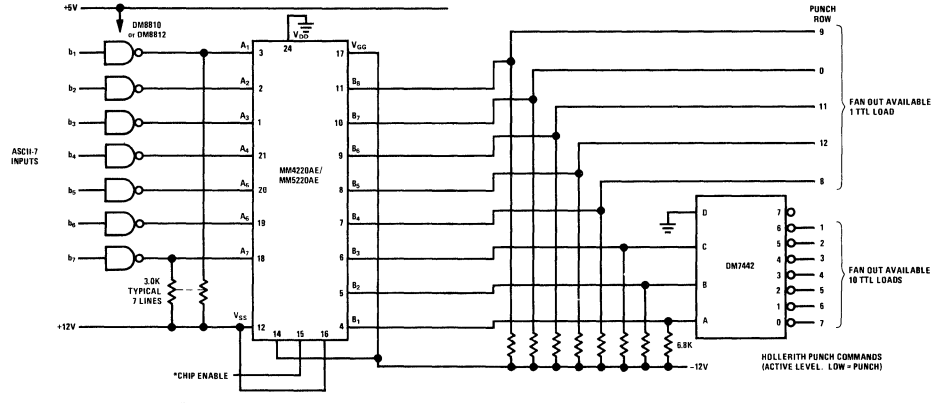
general description

The MM4220AE/MM5220AE 1024-bit read-only memory has been programmed to convert the 128 entries of the American Standard Code for Information Interchange in seven bits (ASCII-7) to Hollerith code (compressed to eight bits). The conversion performed follows the recommendation of American National Standard ANSI x 3.26–1970, Hollerith punched card code.

The typical application shows a recommended circuit for re-expansion of the Hollerith code to twelve lines.

For electrical, environmental and mechanical details, refer to the MM4220/MM5220 data sheet.

typical application



*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM, Logic "0" ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative, Logic "0," more positive.

Order Number MM4220AE/J or MM5220AE/J
See Package 11
Order Number MM5220AE/N
See Package 18

code conversion tables

$b_4\ b_3\ b_2\ b_1$	COL / ROW	b_7 0, b_6 0, b_5 0	b_7 0, b_6 0, b_5 1	b_7 0, b_6 1, b_5 0	b_7 0, b_6 1, b_5 1	b_7 1, b_6 0, b_5 0	b_7 1, b_6 0, b_5 1	b_7 1, b_6 1, b_5 0	b_7 1, b_6 1, b_5 1
		0	1	2	3	4	5	6	7
0000	0	NUL 12-0-9-8-1	DLE 12-11-9-8-1	SP NO PCH	0 0	@ 8-4	P 11-7	` 8-1	p 12-11-7
0001	1	SCH 12-9-1	DC1 11-9-1	! ① 12-8-7	1 1	A 12-1	Q 11-8	a 12-0-1	q 12-11-8
0010	2	STX 12-9-2	DC2 11-9-2	" 8-7	2 2	B 12-2	R 11-9	b 12-0-2	r 12-11-9
0011	3	ETX 12-9-3	DC3 11-9-3	# 8-3	3 3	C 12-3	S 0-2	c 12-0-3	s 11-0-2
0100	4	ECT 9-7	DC4 9-8-4	$ 11-8-3	4 4	D 12-4	T 0-3	d 12-0-4	t 11-0-3
0101	5	ENQ 0-9-8-5	NAK 9-8-5	% 0-8-4	5 5	E 12-5	U 0-4	e 12-0-5	u 11-0-4
0110	6	ACK 0-9-8-6	SYN 9-2	& 12	6 6	F 12-6	V 0-5	f 12-0-6	v 11-0-5
0111	7	BEL 0-9-8-7	ETB 0-9-6	' 8-5	7 7	G 12-7	W 0-6	g 12-0-7	w 11-0-6
1000	8	BS 11-9-6	CAN 11-9-8	(12-8-5	8 8	H 12-8	X 0-7	h 12-0-8	x 11-0-7
1001	9	HT 12-9-5	EM 11-9-8-1	) 11-8-5	9 9	I 12-9	Y 0-8	i 12-0-9	y 11-0-8
1010	10	IF 0-9-5	SUB 9-8-7	* 11-8-4	: 8-2	J 11-1	Z 0-9	j 12-11-1	z 11-0-9
1011	11	VT 12-9-8-3	ESC 0-9-7	+ 12-8-6	; 11-8-6	K 11-2	[12-8-2	k 12-11-2	{ 12-0
1100	12	FF 12-9-8-4	FS 11-9-8-4	, 0-8-3	< 12-8-4	L 11-3	\ 0-8-2	l 12-11-3	¦ 12-11
1101	13	CR 12-9-8-5	GS 11-9-8-5	– 11	= 8-6	M 11-4	] 11-8-2	m 12-11-4	} 11-0
1110	14	SO 12-9-8-6	RS 11-9-8-6	. 12-8-3	> 0-8-6	N 11-5	∧ ② 11-8-7	n 12-11-5	~ 11-0-1
1111	15	SI 12-9-8-7	US 11-9-8-7	/ 0-1	? 0-8-7	O 11-6	– 0-8-5	o 12-11-6	DEL 12-9-7

① may be "|"

② may be "¬"

③ The top line in each entry to the table represents an assigned character (Columns 0 to 7).
The bottom line in each entry is the corresponding card hole-pattern.

code conversion tables(con't)

ADD-RESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	B1
0	1	1	0	1	1	0	0	1
1	1	0	0	1	0	0	0	1
2	1	0	0	1	0	0	1	0
3	1	0	0	1	0	0	1	1
4	1	0	0	0	0	1	1	1
5	1	1	0	0	1	1	0	1
6	1	1	0	0	1	1	1	0
7	1	1	0	0	1	1	1	1
8	1	0	1	0	0	1	1	0
9	1	0	0	1	0	1	0	1
10	1	1	0	0	0	1	0	1
11	1	0	0	1	1	0	1	1
12	1	0	0	1	1	1	0	0
13	1	0	0	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	1	1	1	1	1
16	1	0	1	1	1	0	0	1
17	1	0	1	0	0	0	0	1
18	1	0	1	0	0	0	1	0
19	1	0	1	0	0	0	1	1
20	1	0	0	0	1	1	0	0
21	1	0	0	0	1	1	0	1
22	1	0	0	0	0	0	1	0
23	1	1	0	0	0	1	1	0
24	1	0	1	0	1	0	0	0
25	1	0	1	0	1	0	0	1
26	1	0	0	0	1	1	1	1
27	1	1	0	0	0	1	1	1
28	1	0	1	0	1	1	0	0
29	1	0	1	0	1	1	0	1
30	1	0	1	0	1	1	1	0
31	1	0	1	0	1	1	1	1
32	0	0	0	0	0	0	0	0
33	0	0	0	1	1	1	1	1
34	0	0	0	0	1	1	1	1
35	0	0	0	0	1	0	1	1
36	0	0	1	0	1	0	1	1
37	0	1	0	0	1	1	0	0
38	0	0	0	1	0	0	0	0
39	0	0	0	0	1	1	0	1
40	0	0	0	1	1	1	0	1
41	0	0	1	0	1	1	0	1
42	0	0	1	0	1	1	0	0
ROW	9	0	11	12	8	4	2	1

ADD-RESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	B1
43	0	0	0	1	1	1	1	0
44	0	1	0	0	1	0	1	1
45	0	0	1	0	0	0	0	0
46	0	0	0	1	1	0	1	1
47	0	1	0	0	0	0	0	1
48	0	1	0	0	0	0	0	0
49	0	0	0	0	0	0	0	1
50	0	0	0	0	0	0	1	0
51	0	0	0	0	0	0	1	1
52	0	0	0	0	0	1	0	0
53	0	0	0	0	0	1	0	1
54	0	0	0	0	0	1	1	0
55	0	0	0	0	0	1	1	1
56	0	0	0	0	1	0	0	0
57	1	0	0	0	0	0	0	0
58	0	0	0	0	1	0	1	0
59	0	0	1	0	1	1	1	0
60	0	0	0	1	1	1	0	0
61	0	0	0	0	1	1	1	0
62	0	1	0	0	1	1	1	0
63	0	1	0	0	1	1	1	1
64	0	0	0	0	1	1	0	0
65	0	0	0	1	0	0	0	1
66	0	0	0	1	0	0	1	0
67	0	0	0	1	0	0	1	1
68	0	0	0	1	0	1	0	0
69	0	0	0	1	0	1	0	1
70	0	0	0	1	0	1	1	0
71	0	0	0	1	0	1	1	1
72	0	0	0	1	1	0	0	0
73	1	0	0	1	0	0	0	0
74	0	0	1	0	0	0	0	1
75	0	0	1	0	0	0	1	0
76	0	0	1	0	0	0	1	1
77	0	0	1	0	0	1	0	0
78	0	0	1	0	0	1	0	1
79	0	0	1	0	0	1	1	0
80	0	0	1	0	0	1	1	1
81	0	0	1	0	1	0	0	0
82	1	0	1	0	0	0	0	0
83	0	1	0	0	0	0	1	0
84	0	1	0	0	0	0	1	1
85	0	1	0	0	0	1	0	0
ROW	9	0	11	12	8	4	2	1

ADD-RESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	B1
86	0	1	0	0	0	1	0	1
87	0	1	0	0	0	1	1	0
88	0	1	0	0	0	1	1	1
89	0	1	0	0	1	0	0	0
90	1	1	0	0	0	0	0	0
91	0	0	0	1	1	0	1	0
92	0	1	0	0	1	0	1	0
93	0	0	1	0	1	0	1	0
94	0	0	1	0	1	1	1	1
95	0	1	0	0	1	1	0	1
96	0	0	0	0	1	0	0	1
97	0	1	0	1	0	0	0	1
98	0	1	0	1	0	0	1	0
99	0	1	0	1	0	0	1	1
100	0	1	0	1	0	1	0	0
101	0	1	0	1	0	1	0	1
102	0	1	0	1	0	1	1	0
103	0	1	0	1	0	1	1	1
104	0	1	0	1	1	0	0	0
105	1	1	0	1	0	0	0	0
106	0	0	1	1	0	0	0	1
107	0	0	1	1	0	0	1	0
108	0	0	1	1	0	0	1	1
109	0	0	1	1	0	1	0	0
110	0	0	1	1	0	1	0	1
111	0	0	1	1	0	1	1	0
112	0	0	1	1	0	1	1	1
113	0	0	1	1	1	0	0	0
114	1	0	1	1	0	0	0	0
115	0	1	1	0	0	0	1	0
116	0	1	1	0	0	0	1	1
117	0	1	1	0	0	1	0	0
118	0	1	1	0	0	1	0	1
119	0	1	1	0	0	1	1	0
120	0	1	1	0	0	1	1	1
121	0	1	1	0	1	0	0	0
122	1	1	1	0	0	0	0	0
123	0	1	0	1	0	0	0	0
124	0	0	1	1	0	0	0	0
125	0	1	1	0	0	0	0	0
126	0	1	1	0	0	0	0	1
127	1	0	0	1	0	1	1	1
ROW	9	0	11	12	8	4	2	1

ROM Code Converters

MM4220AP/MM5220AP
BCDIC-to-ASCII code converter

general description

The MM4220AP/MM5220AP is used for the conversion of the Binary Coded Decimal Interchange Code(BCDIC) to the American Standard Code for Information Interchange (ASCII).

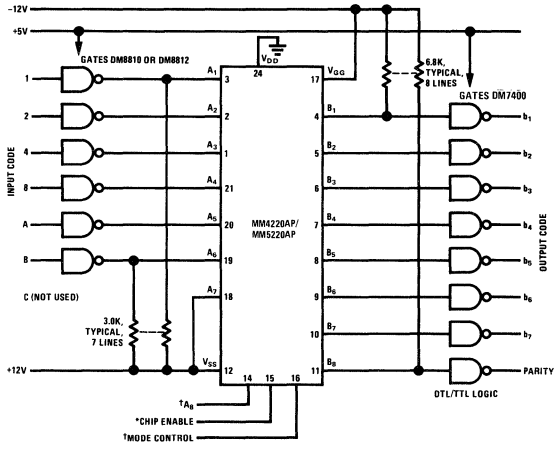
The input is a seven-bit BCDIC code with the exception of the parity (check) bit (pin 18) which is returned to +12V dc. The alternate set of input symbols is also shown in the Conversion Table for reference.

The output is a seven-bit ASCII code, with an eighth bit generated for even parity.

device characteristics

For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

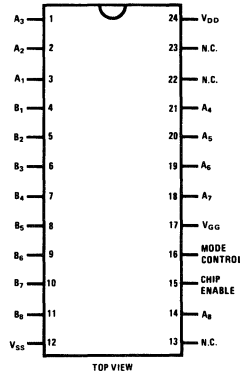
typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4220AP/J or MM5220AP/J
See Package 11
Order Number MM5220AP/N
See Package 18

code conversion table

ROM ADDRESS	FUNCTION INPUT BCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT CODE	B	A	8	4	2	1	OUTPUT EP	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	Space	Space	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1
2	2	2	0	0	0	0	0	1	0	1	0	1	1	0	0	1	0
3	3	3	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1
4	4	4	0	0	0	0	1	0	0	1	0	1	1	0	1	0	0
5	5	5	0	0	0	0	1	0	1	0	0	1	1	0	1	0	1
6	6	6	0	0	0	0	1	1	0	0	0	1	1	0	1	1	0
7	7	7	0	0	0	0	1	1	1	1	0	1	1	0	1	1	1
8	8	8	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
9	9	9	0	0	0	1	0	0	1	0	0	1	1	1	0	0	1
10	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	0
11	# or =	#	0	0	0	1	0	1	1	1	0	1	1	0	0	1	1
12	@ or '	@	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0
13	:	:	0	0	0	1	1	0	1	0	0	1	1	1	0	1	0
14	>	>	0	0	0	1	1	1	0	1	0	1	1	1	1	1	0
15	√	?	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1
16	Blank	[	0	0	1	0	0	0	0	1	1	0	1	1	0	1	1
17	/	/	0	0	1	0	0	0	1	1	0	1	0	1	1	1	1
18	S	S	0	0	1	0	0	1	0	0	1	0	1	0	0	1	1
19	T	T	0	0	1	0	0	1	1	1	1	0	1	0	1	0	0
20	U	U	0	0	1	0	1	0	0	0	1	0	1	0	1	0	1
21	V	V	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0
22	W	W	0	0	1	0	1	1	0	1	1	0	1	0	1	1	1
23	X	X	0	0	1	0	1	1	1	1	1	0	1	1	0	0	0
24	Y	Y	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1
25	Z	Z	0	0	1	1	0	0	1	0	1	0	1	1	0	1	0
26	‡	LF	0	0	1	1	0	1	0	0	0	0	0	1	0	1	0
27	,	,	0	0	1	1	0	1	1	1	0	1	0	1	1	0	0
28	% or (	%	0	0	1	1	1	0	0	1	0	1	0	0	1	0	1
29	∨	HT	0	0	1	1	1	0	1	0	0	0	0	1	0	0	1
30	\	'	0	0	1	1	1	1	0	0	0	1	0	0	1	1	1
31	⫴	"	0	0	1	1	1	1	1	0	0	1	0	0	0	1	0
32	–	–	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1
33	J	J	0	1	0	0	0	0	1	1	1	0	0	1	0	1	0
34	K	K	0	1	0	0	0	1	0	0	1	0	0	1	0	1	1
35	L	L	0	1	0	0	0	1	1	1	1	0	0	1	1	0	0
36	M	M	0	1	0	0	1	0	0	0	1	0	0	1	1	0	1
37	N	N	0	1	0	0	1	0	1	0	1	0	0	1	1	1	0
38	O	O	0	1	0	0	1	1	0	1	1	0	0	1	1	1	1
39	P	P	0	1	0	0	1	1	1	0	1	0	1	0	0	0	0
40	Q	Q	0	1	0	1	0	0	0	1	1	0	1	0	0	0	1
41	R	R	0	1	0	1	0	0	1	1	1	0	1	0	0	1	0
42	!	!	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1
43	$	$	0	1	0	1	0	1	1	0	0	1	0	0	1	0	0
44	*	*	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0
45	)	)	0	1	0	1	1	0	1	1	0	1	0	1	0	0	1
46	;	;	0	1	0	1	1	1	0	1	0	1	1	1	0	1	1
47	Δ	]	0	1	0	1	1	1	1	1	1	0	1	1	1	0	1
48	& or +	&	0	1	1	0	0	0	0	1	0	1	0	0	1	1	0
49	A	A	0	1	1	0	0	0	1	0	1	0	0	0	0	0	1
50	B	B	0	1	1	0	0	1	0	0	1	0	0	0	0	1	0
51	C	C	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
52	D	D	0	1	1	0	1	0	0	0	1	0	0	0	1	0	0
53	E	E	0	1	1	0	1	0	1	1	1	0	0	0	1	0	1
54	F	F	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0
55	G	G	0	1	1	0	1	1	1	0	1	0	0	0	1	1	1
56	H	H	0	1	1	1	0	0	0	0	1	0	0	1	0	0	0
57	I	I	0	1	1	1	0	0	1	1	1	0	0	1	0	0	1
58	?	+	0	1	1	1	0	1	0	0	0	1	0	1	0	1	1
59	.	.	0	1	1	1	0	1	1	0	0	1	0	1	1	1	0
60	¤ or)	⌒	0	1	1	1	1	0	0	1	1	0	1	1	1	1	0
61	[	(	0	1	1	1	1	0	1	0	0	1	0	1	0	0	0
62	<	<	0	1	1	1	1	1	0	0	0	1	1	1	1	0	0
63	‡	CR	0	1	1	1	1	1	1	1	0	0	0	1	1	0	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM Code Converters

MM4220BL/MM5220BL baudot-to-ASCII code converter

general description

The MM4220BL/MM5220BL is used for conversion of the Communications Set Baudot code to the American Standard Code for Information Interchange (ASCII).

The Baudot and ASCII codes have different formats. ASCII has a unique code combination for each alphabetic, numerical, or control character. The correct interpretation of a five bit Baudot is dependent upon knowing its previous history; whether upper or lower case was *last* selected. In effect a sixth-bit, which can be called the Case Bit, is required to uniquely identify the Baudot input. The latch circuit shown in the typical application can store this information and will generate the Case Bit. If the bit is externally supplied, the feedback and latch circuits can be deleted (as shown with the X's).

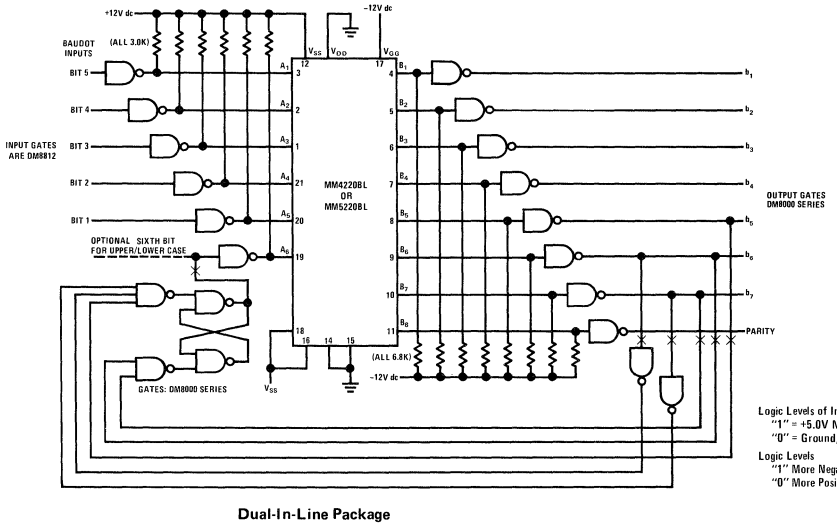
The accompanying table is applicable for the code conversion scheme as shown (or its alternate) rather than for the device itself. The input and output codes are defined at the TTL gates with the logic trues high (Logic "1" = +5 volts, nominal; Logic "0" = Ground, nominal).

device characteristics

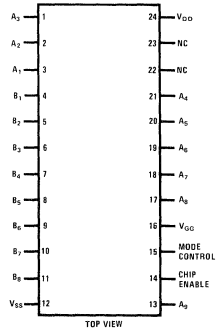
For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical application and connection diagram

Baudot to ASCII



Dual-In-Line Package



Order Number MM4220BL/J or MM5220BL/J
See Package 11

Order Number MM5220BL/N
See Package 18

code conversion tables

ROM ADDRESS	FUNCTION INPUT BAUDOT SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT CASE	BAUDOT 1	2	3	4	5	OUTPUT ASCII EP	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	Blank	NULL	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	T	T	0	0	0	0	0	1	1	1	0	1	0	1	0	0
2	CR	CR	0	0	0	0	1	0	1	0	0	0	1	1	0	1
3	O	O	0	0	0	0	1	1	1	1	0	0	1	1	1	1
4	Space	Space	0	0	0	1	0	0	1	0	1	0	0	0	0	0
5	H	H	0	0	0	1	0	1	0	1	0	0	1	0	0	0
6	N	N	0	0	0	1	1	0	0	1	0	0	1	1	1	0
7	M	M	0	0	0	1	1	1	0	1	0	0	1	1	0	1
8	LF	LF	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0
9	L	L	0	0	1	0	0	1	1	1	0	0	1	1	0	0
10	R	R	0	0	1	0	1	0	1	1	0	1	0	0	1	0
11	G	G	0	0	1	0	1	1	0	1	0	0	0	1	1	1
12	I	I	0	0	1	1	0	0	1	1	0	0	1	0	0	1
13	P	P	0	0	1	1	0	1	0	1	0	1	0	0	0	0
14	C	C	0	0	1	1	1	0	1	1	0	0	0	0	1	1
15	V	V	0	0	1	1	1	1	0	1	0	1	0	1	1	0
16	E	E	0	1	0	0	0	0	1	1	0	0	0	1	0	1
17	Z	Z	0	1	0	0	0	1	0	1	0	1	1	0	1	0
18	D	D	0	1	0	0	1	0	0	1	0	0	0	1	0	0
19	B	B	0	1	0	0	1	1	0	1	0	0	0	0	1	0
20	S	S	0	1	0	1	0	0	0	1	0	1	0	0	1	1
21	Y	Y	0	1	0	1	0	1	0	1	0	1	1	0	0	1
22	F	F	0	1	0	1	1	0	1	1	0	0	0	1	1	0
23	X	X	0	1	0	1	1	1	1	1	0	1	1	0	0	0
24	A	A	0	1	1	0	0	0	0	1	0	0	0	0	0	1
25	W	W	0	1	1	0	0	1	1	1	0	1	0	1	1	1
26	J	J	0	1	1	0	1	0	1	1	0	0	1	0	1	0
27	Upper	IS1/Can	0	1	1	0	1	1	0	0	0	1	1	0	0	0
28	U	U	0	1	1	1	0	0	0	1	0	1	0	1	0	1
29	Q	Q	0	1	1	1	0	1	1	1	0	1	0	0	0	1
30	K	K	0	1	1	1	1	0	0	1	0	0	1	0	1	1
31	Lower	Delete	0	1	1	1	1	1	1	1	1	1	1	1	1	1
32	Blank	NULL	1	0	0	0	0	0	0	0	0	0	0	0	0	0
33	5	5	1	0	0	0	0	1	0	0	1	1	0	1	0	1
34	CR	CR	1	0	0	0	1	0	1	0	0	0	1	1	0	1
35	9	9	1	0	0	0	1	1	0	0	1	1	1	0	0	1
36	Space	Space	1	0	0	1	0	0	1	0	1	0	0	0	0	0
37	#/£ S/S	BS/FE	1	0	0	1	0	1	1	0	0	0	1	0	0	0
38	,	,	1	0	0	1	1	0	1	0	1	0	1	1	0	0
39	.	.	1	0	0	1	1	1	0	0	1	0	1	1	1	0
40	LF	LF	1	0	1	0	0	0	0	0	0	0	1	0	1	0
41	)	)	1	0	1	0	0	1	1	0	1	0	1	0	0	1
42	4	4	1	0	1	0	1	0	1	0	1	1	0	1	0	0
43	&	&	1	0	1	0	1	1	1	0	1	0	0	1	1	0
44	8	8	1	0	1	1	0	0	1	0	0	1	1	1	0	0
45	0	0	1	0	1	1	0	1	0	0	1	1	0	0	0	0
46	:	:	1	0	1	1	1	0	0	0	1	1	1	0	1	0
47	;	;	1	0	1	1	1	1	1	0	1	1	1	0	1	1
48	3	3	1	1	0	0	0	0	0	0	1	1	0	0	1	1
49	"	"	1	1	0	0	0	1	0	0	1	0	0	0	1	0
50	$	$	1	1	0	0	1	0	0	0	1	0	0	1	0	0
51	?	?	1	1	0	0	1	1	0	0	1	1	1	1	1	1
52	Bell	Bell	1	1	0	1	0	0	1	0	0	0	0	1	1	1
53	6	6	1	1	0	1	0	1	0	0	1	1	0	1	1	0
54	!	!	1	1	0	1	1	0	0	0	1	0	0	0	0	1
55	/	/	1	1	0	1	1	1	1	0	1	0	1	1	1	1
56	—	—	1	1	1	0	0	0	0	0	1	0	1	1	0	1
57	2	2	1	1	1	0	0	1	1	0	1	1	0	0	1	0
58	'	'	1	1	1	0	1	0	0	0	1	0	0	1	1	1
59	Upper	Can	1	1	1	0	1	1	0	0	0	1	1	0	0	0
60	7	7	1	1	1	1	0	0	1	0	1	1	0	1	1	1
61	1	1	1	1	1	1	0	1	1	0	1	1	0	0	0	1
62	(	(	1	1	1	1	1	0	0	0	1	0	1	0	0	0
63	Lower	Delete	1	1	1	1	1	1	1	1	1	1	1	1	1	1

LEGEND:
EP = Even Parity
LF = Line Feed
CR = Carriage Return
Can = Cancel
IS1 = Information Separator #1
S/S = Stop/Start
BS = Back Space

ROM Code Converters

MM4220BM/MM5220BM sine look-up table

general description

The MM4220BM/MM5220BM is a 1024-monolithic MOS read only memory that has been programmed to solve for the sine value x of a known angle θ; i.e., to obtain the solution of the equation $x = \sin \theta$.

Values of θ are defined in the look up table for $0^\circ \leq \theta < 90^\circ$ (quadrant I) which has corresponding solutions of $0 \leq x < 1$. For values of $90^\circ < \theta \leq 180^\circ$ (quadrant II), enter the complement $(180^\circ - \theta)$ to obtain the correct solution. Solutions for quadrants III and IV differ in sign with I and II. This is summarized in Table 1.

This input is divided into 128 parts for θ in each quadrant. Thus, the appropriate input address is $(\theta^1/90^\circ)(128)$ to the nearest whole integer. The actual input code to the ROM is the input address expressed in binary, with A_1 being the least significant bit.

The output is the value of X expressed in binary. The output lines $B_1, B_2, \ldots . B_8$ are binary place values 1/2, 1/4, ... 1/256. The sign for negative values of X is externally generated.

The 8 bit output code has been rounded off from a larger word code, i.e., where A_9 was a binary "1" it carried into the LSB of the eight bit code, where A_9 was a binary "0" it was simply dropped.

EXAMPLE

Find the sine of 45°.

The input address is (45/90) 128 = 64 or 1000000, as expressed in binary. The converter generates the output .10110101 whose decimal equivalent is 0.707131. Thus, $\sin 45^\circ = 0.707$.

Find the sine of 210°.

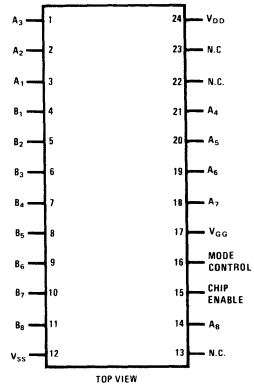
This value is in quadrant III; therefore $\theta^1 = 210^\circ - 180^\circ = 30^\circ$. The input address is then (30/90) $128 \cong 43$ to the nearest whole integer. The binary input to the ROM is then 0101011. The output value is .10000001 or 0.503906. Thus, $\sin 210^\circ = -0.504$, with the sign generated by the external logic. The solution is within 1%; note that address 43 is actually equal to 30.23°.

device characteristics

For full electrical, environmental and mechanical details refer to the MM4220/MM5220 1024-bit read only memory data sheet.

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM4220BM/J or MM5220BM/J
See Package 11
Order Number MM5220BM/N
See Package 18

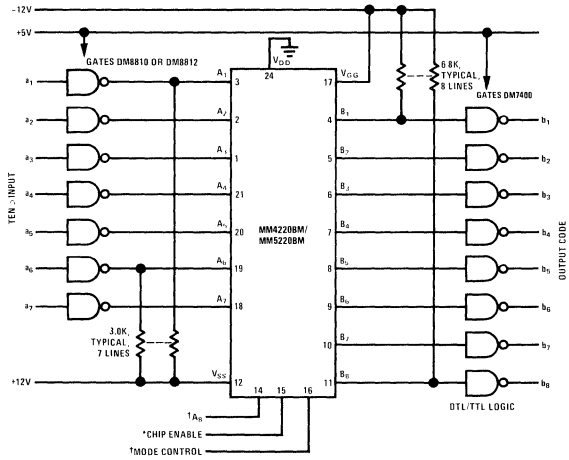
pattern selection form

ADDRESS REFERENCE	FUNCTION INPUT		CODE OUTPUT							
	DEGREES	RADIANS	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
0	.00	.000	0	0	0	0	0	0	0	0
1	.70	.012	1	1	0	0	0	0	0	0
2	1.41	.025	0	1	1	0	0	0	0	0
3	2.11	.037	1	0	0	1	0	0	0	0
4	2.81	.049	0	0	1	1	0	0	0	0
5	3.52	.061	1	1	1	1	0	0	0	0
6	4.22	.074	1	1	0	0	1	0	0	0
7	4.92	.086	0	1	1	0	1	0	0	0
8	5.63	.098	1	0	0	1	1	0	0	0
9	6.33	.110	0	0	1	1	1	0	0	0
10	7.03	.123	1	1	1	1	1	0	0	0
11	7.73	.135	0	1	0	0	0	1	0	0
12	8.44	.147	1	0	1	0	0	1	0	0
13	9.14	.160	0	0	0	1	0	1	0	0
14	9.84	.172	0	0	1	1	0	1	0	0
15	10.55	.184	1	1	1	1	0	1	0	0
16	11.25	.196	0	1	0	0	1	1	0	0
17	11.95	.209	1	0	1	0	1	1	0	0
18	12.66	.221	0	0	0	1	1	1	0	0
19	13.36	.233	1	1	0	1	1	1	0	0
20	14.06	.245	0	1	1	1	1	1	0	0
21	14.77	.258	1	0	0	0	0	0	1	0
22	15.47	.270	0	0	1	0	0	0	1	0
23	16.17	.282	1	1	1	0	0	0	1	0
24	16.88	.295	0	1	0	1	0	0	1	0
25	17.58	.307	1	0	1	1	0	0	1	0
26	18.28	.319	0	0	0	0	1	0	1	0
27	18.98	.331	1	1	0	0	1	0	1	0
28	19.69	.344	0	1	1	0	1	0	1	0
29	20.39	.356	1	0	0	1	1	0	1	0
30	21.09	.368	0	0	1	1	1	0	1	0
31	21.80	.380	1	1	1	1	1	0	1	0
32	22.50	.393	0	1	0	0	0	1	1	0
33	23.20	.405	1	1	1	0	0	1	1	0
34	23.91	.417	1	1	1	0	0	1	1	0
35	24.61	.430	0	1	0	1	0	1	1	0
36	25.31	.442	1	0	1	1	0	1	1	0
37	26.02	.454	0	0	0	0	1	1	1	0
38	26.72	.466	1	1	0	0	1	1	1	0
39	27.42	.479	0	1	1	0	1	1	1	0
40	28.13	.491	0	0	0	1	1	1	1	0
41	28.83	.503	1	1	0	1	1	1	1	0
42	29.53	.515	0	1	1	1	1	1	1	0
43	30.23	.528	0	0	0	0	0	0	0	1
44	30.94	.540	1	1	0	0	0	0	0	1
45	31.64	.552	0	1	1	0	0	0	0	1
46	32.34	.565	1	0	0	1	0	0	0	1
47	33.05	.577	1	1	0	1	0	0	0	1
48	33.75	.589	0	1	1	1	0	0	0	1
49	34.45	.601	1	0	0	0	1	0	0	1
50	35.16	.614	1	1	0	0	1	0	0	1
51	35.86	.626	0	1	1	0	1	0	0	1
52	36.56	.638	0	0	0	1	1	0	0	1
53	37.27	.650	1	1	0	1	1	0	0	1
54	37.97	.663	1	0	1	1	1	0	0	1
55	38.67	.675	0	0	0	0	0	1	0	1
56	39.37	.687	0	1	0	0	0	1	0	1
57	40.08	.699	1	0	1	0	0	1	0	1
58	40.78	.712	1	1	1	0	0	1	0	1
59	41.48	.724	1	0	0	1	0	1	0	1
60	42.19	.736	0	0	1	1	0	1	0	1
61	42.89	.749	0	1	1	1	0	1	0	1
62	43.59	.761	0	0	0	0	1	1	0	1
63	44.30	.773	1	1	0	0	1	1	0	1

pattern selection form(con't)

ADDRESS REFERENCE	FUNCTION INPUT		CODE OUTPUT							
	DEGREES	RADIANS	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
64	45.00	.785	1	0	1	0	1	1	0	1
65	45.70	.798	1	1	1	0	1	1	0	1
66	46.41	.810	1	0	0	1	1	1	0	1
67	47.11	.822	1	1	0	1	1	1	0	1
68	47.81	.834	1	0	1	1	1	1	0	1
69	48.52	.847	0	0	0	0	0	0	1	1
70	49.22	.859	0	1	0	0	0	0	1	1
71	49.92	.871	0	0	1	0	0	0	1	1
72	50.62	.884	0	1	1	0	0	0	1	1
73	51.33	.896	0	0	0	1	0	0	1	1
74	52.03	.908	0	1	0	1	0	0	1	1
75	52.73	.920	1	1	0	1	0	0	1	1
76	53.44	.933	1	0	1	1	0	0	1	1
77	54.14	.945	1	1	1	1	0	0	1	1
78	54.84	.957	1	0	0	0	1	0	1	1
79	55.55	.969	1	1	0	0	1	0	1	1
80	56.25	.982	1	0	1	0	1	0	1	1
81	56.95	.994	0	1	1	0	1	0	1	1
82	57.66	1.006	0	0	0	1	1	0	1	1
83	58.36	1.019	0	1	0	1	1	0	1	1
84	59.06	1.031	1	1	0	1	1	0	1	1
85	59.77	1.043	1	0	1	1	1	0	1	1
86	60.47	1.055	0	1	1	1	1	0	1	1
87	61.17	1.068	0	0	0	0	0	1	1	1
88	61.87	1.080	0	1	0	0	0	1	1	1
89	62.58	1.092	1	1	0	0	0	1	1	1
90	63.28	1.104	0	0	1	0	0	1	1	1
91	63.98	1.117	0	1	1	0	0	1	1	1
92	64.69	1.129	1	1	1	0	0	1	1	1
93	65.39	1.141	0	0	0	1	0	1	1	1
94	66.09	1.154	0	1	0	1	0	1	1	1
95	66.80	1.166	1	1	0	1	0	1	1	1
96	67.50	1.178	0	0	1	1	0	1	1	1
97	68.20	1.190	1	0	1	1	0	1	1	1
98	68.91	1.203	1	1	1	1	0	1	1	1
99	69.61	1.215	0	0	0	0	1	1	1	1
100	70.31	1.227	1	0	0	0	1	1	1	1
101	71.02	1.239	0	1	0	0	1	1	1	1
102	71.72	1.252	1	1	0	0	1	1	1	1
103	72.42	1.264	0	0	1	0	1	1	1	1
104	73.12	1.276	1	0	1	0	1	1	1	1
105	73.83	1.289	0	1	1	0	1	1	1	1
106	74.53	1.301	0	1	1	0	1	1	1	1
107	75.23	1.313	1	1	1	0	1	1	1	1
108	75.94	1.325	0	0	0	1	1	1	1	1
109	76.64	1.338	1	0	0	1	1	1	1	1
110	77.34	1.350	0	1	0	1	1	1	1	1
111	78.05	1.362	0	1	0	1	1	1	1	1
112	78.75	1.374	1	1	0	1	1	1	1	1
113	79.45	1.387	1	1	0	1	1	1	1	1
114	80.16	1.399	0	0	1	1	1	1	1	1
115	80.86	1.411	0	0	1	1	1	1	1	1
116	81.56	1.424	1	0	1	1	1	1	1	1
117	82.27	1.436	1	0	1	1	1	1	1	1
118	82.97	1.448	0	1	1	1	1	1	1	1
119	83.67	1.460	0	1	1	1	1	1	1	1
120	84.38	1.473	1	1	1	1	1	1	1	1
121	85.08	1.485	1	1	1	1	1	1	1	1
122	85.78	1.497	1	1	1	1	1	1	1	1
123	86.48	1.509	1	1	1	1	1	1	1	1
124	87.19	1.522	1	1	1	1	1	1	1	1
125	87.89	1.534	1	1	1	1	1	1	1	1
126	88.59	1.546	1	1	1	1	1	1	1	1
127	89.30	1.559	1	1	1	1	1	1	1	1

typical application



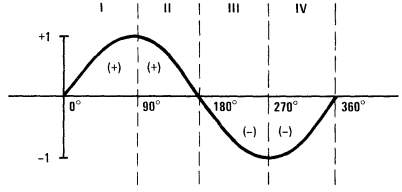
†Mode Control = Logic "0," A_8 = Logic "1."

*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
OTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

Table 1. SINE

	INPUT		OUTPUT	
Quadrant	**Range**	**Entry to ROM (θ^1)**	**Binary Value**	**Sign**
I	$\geq 0^\circ < 90^\circ$	Direct	Direct Reading	+
II	$> 90^\circ \leq 180^\circ$	$180^\circ - X$	Direct Reading	+
III	$\geq 180^\circ < 270^\circ$	$X - 180^\circ$	Direct Reading	-
IV	$> 270^\circ \leq 360^\circ$	$360^\circ - X$	Direct Reading	-



ROM Code Converters

MM4220BN/MM5220BN arctangent look-up table

general description

The MM4220BN/MM5220BN is a 1024-bit monolithic MOS read only memory that has been programmed to solve for the angle θ whose tangent value x is known; i.e., to obtain the solution to the equation: $\theta = \arctan x$.

Values of x are defined in the Look Up table for $0 \leq x < 1$ with angles corresponding from $0^\circ \leq \theta < 45^\circ$. For values $x \geq 1$, the reciprocal of x (i.e., 1/x) must be entered and the output angle must be complemented to obtain the actual value.

The input is divided into 128 equal parts for x. Thus, the appropriate input address is (128)(x) to the nearest whole integer for obtaining the appropriate ROM address. The input code is the ROM address expressed in binary with A_1 being the least significant bit. For input values greater than unity, the decimal reciprocal is to be taken prior to entry of the binary address.

The output has been normalized for 45°. To obtain the true angular reading, the output should be multiplied by 45°, i.e.: $\theta = (\theta_{output}) \times 45^\circ$ where θ_{output} is the decimal equivalent of the output. The output code is the normalized value of the angle θ expressed in binary. The output lines B_1, B_2, ... B_8 are binary place values 1/2, 1/4, ... 1/256. To obtain angles between 45° and 89.6° which occur when input values of x are equal to or greater than unity, either complement the output binary code and add a 1, or complement the resultant angular value (i.e., subtract from 90°).

The 8-bit output code has been rounded off. That is, if another bit of even lower significance had been computed for the given arctangent value was a binary "1", it would have carried over into the LSB of the eight bit code. If it was a binary "0", it would have been dropped.

EXAMPLE

Find the angle whose tangent is 0.258.

The input address is 128 x 0.258, or 33 to the nearest integer. Expressed in binary, this is 0100001, and is the actual input code to the converter. The converter will generate the binary value .01010010, whose decimal equivalent is 0.3203125.

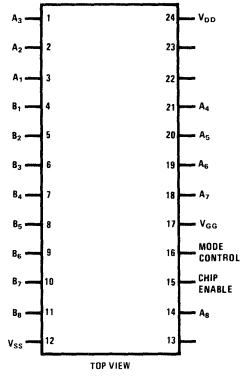
Thus, $\theta = 0.320 \times 45^\circ = 14.4^\circ$

device characteristics

For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

connection diagram

Dual-In-Line Package



Order Number MM4220BN/J or MM5220BN/J
See Package 11
Order Number MM5220BN/N
See Package 18

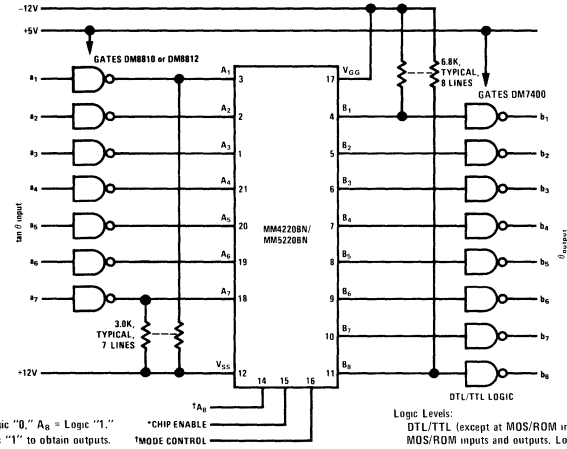
pattern selection form

ADDRESS 128 (x)	OUTPUT CODE (θ_{OUTPUT}) B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
2	1	0	1	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	0	1	0	1	0	0	0	0
5	0	0	1	1	0	0	0	0
6	1	1	1	1	0	0	0	0
7	0	1	0	0	1	0	0	0
8	0	0	1	0	1	0	0	0
9	1	1	1	0	1	0	0	0
10	1	0	0	1	1	0	0	0
11	0	0	1	1	1	0	0	0
12	0	1	1	1	1	0	0	0
13	1	0	0	0	0	1	0	0
14	1	1	0	0	0	1	0	0
15	0	1	1	0	0	1	0	0
16	0	0	0	1	0	1	0	0
17	1	1	0	1	0	1	0	0
18	1	0	1	1	0	1	0	0
19	0	0	0	0	1	1	0	0
20	0	1	0	0	1	1	0	0
21	1	0	1	0	1	1	0	0
22	1	1	1	0	1	1	0	0
23	0	1	0	1	1	1	0	0
24	0	0	1	1	1	1	0	0
25	1	1	1	1	1	1	0	0
26	1	0	0	0	0	0	1	0
27	0	0	1	0	0	0	1	0
28	0	1	1	0	0	0	1	0
29	0	0	0	1	0	0	1	0
30	1	1	0	1	0	0	1	0
31	1	0	1	1	0	0	1	0
32	0	0	0	0	1	0	1	0
33	0	1	0	0	1	0	1	0
34	0	0	1	0	1	0	1	0
35	1	1	1	0	1	0	1	0
36	1	0	0	1	1	0	1	0
37	1	1	0	1	1	0	1	0
38	0	1	1	1	1	0	1	0
39	0	0	0	0	0	1	1	0
40	0	1	0	0	0	1	1	0
41	1	0	1	0	0	1	1	0
42	1	1	1	0	0	1	1	0
43	1	0	0	1	0	1	1	0
44	0	0	1	1	0	1	1	0
45	0	1	1	1	0	1	1	0
46	0	0	0	0	1	1	1	0
47	0	1	0	0	1	1	1	0
48	1	0	1	0	1	1	1	0
49	1	1	1	0	1	1	1	0
50	1	0	0	1	1	1	1	0
51	1	1	0	1	1	1	1	0
52	0	1	1	1	1	1	1	0
53	0	0	0	0	0	0	0	1
54	0	1	0	0	0	0	0	1
55	0	0	1	0	0	0	0	1
56	0	1	1	0	0	0	0	1
57	0	0	0	1	0	0	0	1
58	0	1	0	1	0	0	0	1
59	1	0	1	1	0	0	0	1
60	1	1	1	1	0	0	0	1
61	1	0	0	0	1	0	0	1
62	1	1	0	0	1	0	0	1
63	1	0	1	0	1	0	0	1
64	1	1	1	0	1	0	0	1
65	1	0	0	1	1	0	0	1
66	1	1	0	1	1	0	0	1
67	1	0	1	1	1	0	0	1
68	1	1	1	1	1	0	0	1
69	1	0	0	0	0	1	0	1
70	1	1	0	0	0	1	0	1
71	1	0	1	0	0	1	0	1
72	1	1	1	0	0	1	0	1
73	1	0	0	1	0	1	0	1
74	1	1	0	1	0	1	0	1
75	1	0	1	1	0	1	0	1
76	0	1	1	1	0	1	0	1
77	0	0	0	0	1	1	0	1
78	0	1	0	0	1	1	0	1
79	0	0	1	0	1	1	0	1
80	0	1	1	0	1	1	0	1
81	0	0	0	1	1	1	0	1
82	1	0	0	1	1	1	0	1
83	1	1	0	1	1	1	0	1
84	1	0	1	1	1	1	0	1
85	1	1	1	1	1	1	0	1
86	1	0	0	0	0	0	1	1
87	0	1	0	0	0	0	1	1
88	0	0	1	0	0	0	1	1
89	0	1	1	0	0	0	1	1
90	1	1	1	0	0	0	1	1
91	1	0	0	1	0	0	1	1
92	1	1	0	1	0	0	1	1
93	1	0	1	1	0	0	1	1
94	0	1	1	1	0	0	1	1
95	0	0	0	0	1	0	1	1
96	1	0	0	0	1	0	1	1
97	1	1	0	0	1	0	1	1
98	1	0	1	0	1	0	1	1
99	0	1	1	0	1	0	1	1
100	0	0	0	1	1	0	1	1
101	1	0	0	1	1	0	1	1
102	1	1	0	1	1	0	1	1
103	1	0	1	1	1	0	1	1
104	0	1	1	1	1	0	1	1
105	0	0	0	0	0	1	1	1
106	1	0	0	0	0	1	1	1
107	1	1	0	0	0	1	1	1
108	0	0	1	0	0	1	1	1
109	0	1	1	0	0	1	1	1
110	1	1	1	0	0	1	1	1
111	1	0	0	1	0	1	1	1
112	0	1	0	1	0	1	1	1
113	1	1	0	1	0	1	1	1
114	1	0	1	1	0	1	1	1
115	0	1	1	1	0	1	1	1
116	0	0	0	0	1	1	1	1
117	1	0	0	0	1	1	1	1
118	1	1	0	0	1	1	1	1
119	0	0	1	0	1	1	1	1
120	1	0	1	0	1	1	1	1
121	1	1	1	0	1	1	1	1
122	0	0	0	1	1	1	1	1
123	1	0	0	1	1	1	1	1
124	1	1	0	1	1	1	1	1
125	0	0	1	1	1	1	1	1
126	1	0	1	1	1	1	1	1
127	0	1	1	1	1	1	1	1

Note: 1 more negative output.
0 more positive output.

MM522BN

typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive

8

ROM Code Converters

MM4220DF/MM5220DF

"quick brown fox" generator

general description

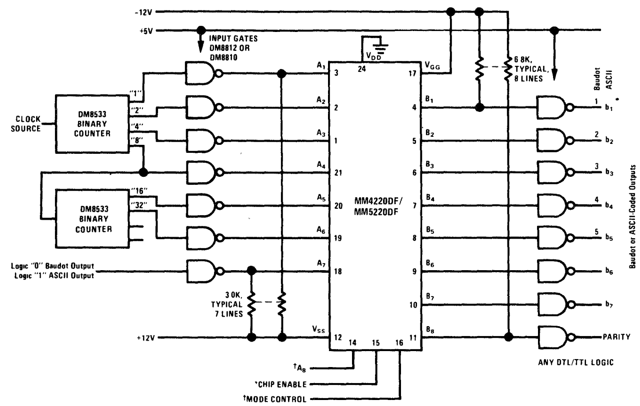
The MM4220DF/MM5220DF is designed for exercising and rapid testing of ASCII and Baudot-coded keyboards, typing mechanisms, and data communications links by generating the internationally accepted "Quick Brown Fox" message.

The input is a 7-bit binary sequential count. The output of a 6 stage up-counter can be used; a seventh bit selects the desired code. The message is generated in the 5-bit Baudot Communications Set code with a binary count input of 0 to 63. The message is generated in the 7-bit American Standard Code for Information Interchange (ASCII) along with an even parity bit for a binary count input of 64 to 127.

device characteristics

The message generator is fully contained on a monolithic MOS integrated circuit chip utilizing low threshold voltage technology for increased DTL/TTL compatibility. For complete electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical applications



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

Outputs for circuit shown
Baudot: Logic "0" = "punch"
ASCII: Logic inversion

A typical application showing the ASCII-coded test message as received at a computer terminal.

```
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
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THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
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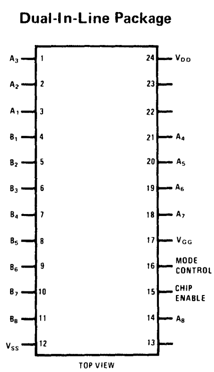
connection diagram

Dual-In-Line Package



Order Number MM4220DF/J or MM5220DF/J
See Package 11
Order Number MM5220DF/N
See Package 18

code conversion table

ADDRESS	OUTPUT CHARACTER	OUTPUT CODE (Baudot) –	–	–	5	4	3	2	1	ADDRESS	OUTPUT CHARACTER	OUTPUT CODE (PARITY / ASCII) PARITY	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	CR	1	1	1	1	0	1	1	1	64	NULL	0	0	0	0	0	0	0	0
1	CR	1	1	1	1	0	1	1	1	65	CR	0	1	1	1	0	0	1	0
2	LF	1	1	1	1	1	1	0	1	66	CR	0	1	1	1	0	0	1	0
3	Ltr	1	1	1	0	0	0	0	0	67	LF	1	1	1	1	0	1	0	1
4	T	1	1	1	0	1	1	1	1	68	T	0	0	1	0	1	0	1	1
5	H	1	1	1	0	1	0	1	1	69	H	1	0	1	1	0	1	1	1
6	E	1	1	1	1	1	1	1	0	70	E	0	0	1	1	1	0	1	0
7	SP	1	1	1	1	1	0	1	1	71	SP	0	1	0	1	1	1	1	1
8	Q	1	1	1	0	1	0	0	0	72	Q	0	0	1	0	1	1	1	0
9	U	1	1	1	1	1	0	0	0	73	U	1	0	1	0	1	0	1	0
10	I	1	1	1	1	1	0	0	1	74	I	0	0	1	1	0	1	1	0
11	C	1	1	1	1	0	0	0	1	75	C	0	0	1	1	1	1	0	0
12	K	1	1	1	1	0	0	0	0	76	K	1	0	1	1	0	1	0	0
13	SP	1	1	1	1	1	0	1	1	77	SP	0	1	0	1	1	1	1	1
14	B	1	1	1	0	0	1	1	0	78	B	1	0	1	1	1	1	0	1
15	R	1	1	1	1	0	1	0	1	79	R	0	0	1	0	1	1	0	1
16	O	1	1	1	0	0	1	1	1	80	O	0	0	1	1	0	0	0	0
17	W	1	1	1	0	1	1	0	0	81	W	0	0	1	0	1	0	0	0
18	N	1	1	1	1	0	0	1	1	82	N	1	0	1	1	0	0	0	1
19	SP	1	1	1	1	1	0	1	1	83	SP	0	1	0	1	1	1	1	1
20	F	1	1	1	1	0	0	1	0	84	F	0	0	1	1	1	0	0	1
21	O	1	1	1	0	0	1	1	1	85	O	0	0	1	1	0	0	0	0
22	X	1	1	1	0	0	0	1	0	86	X	0	0	1	0	0	1	1	1
23	SP	1	1	1	1	1	0	1	1	87	SP	0	1	0	1	1	1	1	1
24	J	1	1	1	1	0	1	0	0	88	J	0	0	1	1	0	1	0	1
25	U	1	1	1	1	1	0	0	0	89	U	1	0	1	0	1	0	1	0
26	M	1	1	1	0	0	0	1	1	90	M	1	0	1	1	0	0	1	0
27	P	1	1	1	0	1	0	0	1	91	P	1	0	1	0	1	1	1	1
28	S	1	1	1	1	1	0	1	0	92	S	1	0	1	0	1	1	0	0
29	SP	1	1	1	1	1	0	1	1	93	SP	0	1	0	1	1	1	1	1
30	O	1	1	1	0	0	1	1	1	94	O	0	0	1	1	0	0	0	0
31	V	1	1	1	0	0	0	0	1	95	V	1	0	1	0	1	0	0	1
32	E	1	1	1	1	1	1	1	0	96	E	0	0	1	1	1	0	1	0
33	R	1	1	1	1	0	1	0	1	97	R	0	0	1	0	1	1	0	1
34	SP	1	1	1	1	1	0	1	1	98	SP	0	1	0	1	1	1	1	1
35	T	1	1	1	0	1	1	1	1	99	T	0	0	1	0	1	0	1	1
36	H	1	1	1	0	1	0	1	1	100	H	1	0	1	1	0	1	1	1
37	E	1	1	1	1	1	1	1	0	101	E	0	0	1	1	1	0	1	0
38	SP	1	1	1	1	1	0	1	1	102	SP	0	1	0	1	1	1	1	1
39	L	1	1	1	0	1	1	0	1	103	L	0	0	1	1	0	0	1	1
40	A	1	1	1	1	1	1	0	0	104	A	1	0	1	1	1	1	1	0
41	Z	1	1	1	0	1	1	1	0	105	Z	1	0	1	0	0	1	0	1
42	Y	1	1	1	0	1	0	1	0	106	Y	1	0	1	0	0	1	1	0
43	SP	1	1	1	1	1	0	1	1	107	SP	0	1	0	1	1	1	1	1
44	D	1	1	1	1	0	1	1	0	108	D	1	0	1	1	1	0	1	1
45	O	1	1	1	0	0	1	1	1	109	O	0	0	1	1	0	0	0	0
46	G	1	1	1	0	0	1	0	1	110	G	1	0	1	1	1	0	0	0
47	SP	1	1	1	1	1	0	1	1	111	SP	0	1	0	1	1	1	1	1
48	Fig.	1	1	1	0	0	1	0	0	112	1	0	1	0	0	1	1	1	0
49	1	1	1	1	0	1	0	0	0	113	2	0	1	0	0	1	1	0	1
50	2	1	1	1	0	1	1	0	0	114	3	1	1	0	0	1	1	0	0
51	3	1	1	1	1	1	1	1	0	115	4	0	1	0	0	1	0	1	1
52	4	1	1	1	1	0	1	0	1	116	5	1	1	0	0	1	0	1	0
53	5	1	1	1	0	1	1	1	1	117	6	1	1	0	0	1	0	0	1
54	6	1	1	1	0	1	0	1	0	118	7	0	1	0	0	1	0	0	0
55	7	1	1	1	1	1	0	0	0	119	8	0	1	0	0	0	1	1	1
56	8	1	1	1	1	1	0	0	1	120	9	1	1	0	0	0	1	1	0
57	9	1	1	1	0	0	1	1	1	121	0	1	1	0	0	1	1	1	1
58	0	1	1	1	0	1	0	0	1	122	SP	0	1	0	1	1	1	1	1
59	SP	1	1	1	1	1	0	1	1	123	D	1	0	1	1	1	0	1	1
60	Ltr.	1	1	1	0	0	0	0	0	124	E	0	0	1	1	1	0	1	0
61	D	1	1	1	1	0	1	1	0	125	SP	0	1	0	1	1	1	1	1
62	E	1	1	1	1	1	1	1	0	126	DEL	0	0	0	0	0	0	0	0
63	SP	1	1	1	1	1	0	1	1	127	DEL	0	0	0	0	0	0	0	0
		B8	B7	B6	B5	B4	B3	B2	B1			B8	B7	B6	B5	B4	B3	B2	B1
		Baudot: Logic "0" = "punch"										ASCII: Logic inversion							

SP = Space

Note: When chip enable input is at a logical 0, all outputs are at a logical 1.

8

ROM Code Converters

MM4220EK/MM5220EK
BCDIC-to-EBCDIC and ASCII-to-EBCDIC code converter

general description

The MM4220EK/MM5220EK is a 1024-bit read only memory that has been programmed to convert both Binary Coded Decimal Interchange Code (BCDIC) and the American Standard Code for Information Interchange (ASCII) to Extended Binary Coded Decimal Interchange Code (EBCDIC).

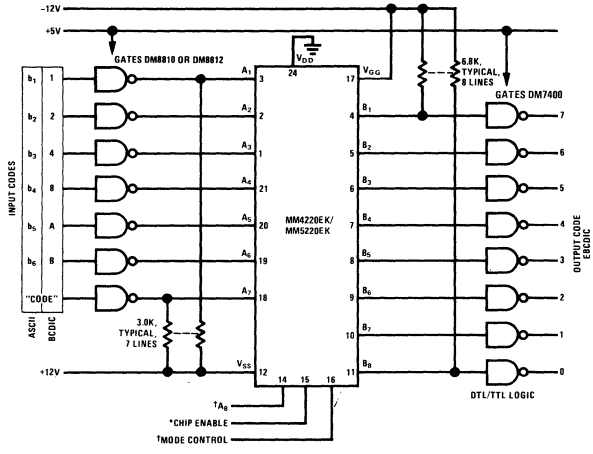
The BCDIC-to-EBCDIC converter is located in the first 64 8-bit bytes of the ROM. The unused parity check bit (the most significant input BCDIC bit) is always a "0".

The ASCII-to-EBCDIC converter is located in the second 64 8-bit bytes of the ROM. Thus, the input ASCII code in addresses 64 through 127 has a "1" in the most significant (A_7) bit which is used with the selection logic. The resulting 6-bit ASCII input is for display—only upper case and numerical codes, since it will not accept the control commands or the lower case characters.

device characteristics

For full electrical, environmental and mechanical details, refer to the MM4220/MM5220 1024-bit only memory data sheet.

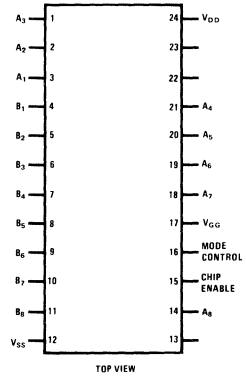
typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4220EK/J or MM5220EK/J
See Package 11
Order Number MM5220EK/N
See Package 18

code conversion tables

ROM ADDRESS	FUNCTION INPUT BCDIC SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT BCDIC CODE	B	A	8	4	2	1	CODE OUTPUT EBCDIC 0	1	2	3	4	5	6	7
0	Space	Space	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1
2	2	2	0	0	0	0	0	1	0	1	1	1	1	0	0	1	0
3	3	3	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1
4	4	4	0	0	0	0	1	0	0	1	1	1	1	0	1	0	0
5	5	5	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1
6	6	6	0	0	0	0	1	1	0	1	1	1	1	0	1	1	0
7	7	7	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
8	8	8	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0
9	9	9	0	0	0	1	0	0	1	1	1	1	1	1	0	0	1
10	0	0	0	0	0	1	0	1	0	1	1	1	1	0	0	0	0
11	# or =	#	0	0	0	1	0	1	1	0	1	1	1	1	0	1	1
12	@ or '	@	0	0	0	1	1	0	0	0	1	1	1	1	1	0	0
13	:	:	0	0	0	1	1	0	1	0	1	1	1	1	0	1	0
14	>	>	0	0	0	1	1	1	0	0	1	1	0	1	1	1	0
15	√(TM)	TM	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1
16	Space	Space	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
17	/	/	0	0	1	0	0	0	1	0	1	1	0	0	0	0	1
18	S	S	0	0	1	0	0	1	0	1	1	1	0	0	0	1	0
19	T	T	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1
20	U	U	0	0	1	0	1	0	0	1	1	1	0	0	1	0	0
21	V	V	0	0	1	0	1	0	1	1	1	1	0	0	1	0	1
22	W	W	0	0	1	0	1	1	0	1	1	1	0	0	1	1	0
23	X	X	0	0	1	0	1	1	1	1	1	1	0	0	1	1	1
24	Y	Y	0	0	1	1	0	0	0	1	1	1	0	1	0	0	0
25	Z	Z	0	0	1	1	0	0	1	1	1	1	0	1	0	0	1
26	‡(RM)	RM	0	0	1	1	0	1	0	1	1	1	0	0	0	0	0
27	,	,	0	0	1	1	0	1	1	0	1	1	0	1	0	1	1
28	% or (	%	0	0	1	1	1	0	0	0	1	1	0	1	1	0	0
29	v	+	0	0	1	1	1	0	1	0	1	0	0	1	1	1	0
30	\	¢	0	0	1	1	1	1	0	0	1	0	0	1	0	1	0
31	≠	=	0	0	1	1	1	1	1	0	1	1	1	1	1	1	0
32	-	-	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0
33	J	J	0	1	0	0	0	0	1	1	1	0	1	0	0	0	1
34	K	K	0	1	0	0	0	1	0	1	1	0	1	0	0	1	0
35	L	L	0	1	0	0	0	1	1	1	1	0	1	0	0	1	1
36	M	M	0	1	0	0	1	0	0	1	1	0	1	0	1	0	0
37	N	N	0	1	0	0	1	0	1	1	1	0	1	0	1	0	1
38	O	O	0	1	0	0	1	1	0	1	1	0	1	0	1	1	0
39	P	P	0	1	0	0	1	1	1	1	1	0	1	0	1	1	1
40	Q	Q	0	1	0	1	0	0	0	1	1	0	1	1	0	0	0
41	R	R	0	1	0	1	0	0	1	1	1	0	1	1	0	0	1
42	!	!	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0
43	$	$	0	1	0	1	0	1	1	0	1	0	1	1	0	1	1
44	*	*	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0
45	]	)	0	1	0	1	1	0	1	0	1	0	1	1	1	0	1
46	;	;	0	1	0	1	1	1	0	0	1	0	1	1	1	1	0
47	△	"	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1
48	& or +	&	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0
49	A	A	0	1	1	0	0	0	1	1	1	0	0	0	0	0	1
50	B	B	0	1	1	0	0	1	0	1	1	0	0	0	0	1	0
51	C	C	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
52	D	D	0	1	1	0	1	0	0	1	1	0	0	0	1	0	0
53	E	E	0	1	1	0	1	0	1	1	1	0	0	0	1	0	1
54	F	F	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0
55	G	G	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1
56	H	H	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0
57	I	I	0	1	1	1	0	0	1	1	1	0	0	1	0	0	1
58	?	?	0	1	1	1	0	1	0	0	1	1	0	1	1	1	1
59	.	.	0	1	1	1	0	1	1	0	1	0	0	1	0	1	1
60	¤ or)	¤	0	1	1	1	1	0	0	0	1	1	0	1	0	1	0
61	[	(	0	1	1	1	1	0	1	0	1	0	0	1	1	0	1
62	<	<	0	1	1	1	1	1	0	0	1	0	0	1	1	0	0
63	‡	'	0	1	1	1	1	1	1	0	1	1	1	1	1	0	1

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code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT CODE	b_6	b_5	b_4	b_3	b_2	b_1	OUTPUT EBCDIC 0	1	2	3	4	5	6	7
64	@	@	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
65	A	A	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1
66	B	B	1	0	0	0	0	1	0	1	1	0	0	0	0	1	0
67	C	C	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
68	D	D	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0
69	E	E	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1
70	F	F	1	0	0	0	1	1	0	1	1	0	0	0	1	1	0
71	G	G	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
72	H	H	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0
73	I	I	1	0	0	1	0	0	1	1	1	0	0	1	0	0	1
74	J	J	1	0	0	1	0	1	0	1	1	0	1	0	0	0	1
75	K	K	1	0	0	1	0	1	1	1	1	0	1	0	0	1	0
76	L	L	1	0	0	1	1	0	0	1	1	0	1	0	0	1	1
77	M	M	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0
78	N	N	1	0	0	1	1	1	0	1	1	0	1	0	1	0	1
79	O	O	1	0	0	1	1	1	1	1	1	0	1	0	1	1	0
80	P	P	1	0	1	0	0	0	0	1	1	0	1	0	1	1	1
81	Q	Q	1	0	1	0	0	0	1	1	1	0	1	1	0	0	0
82	R	R	1	0	1	0	0	1	0	1	1	0	1	1	0	0	1
83	S	S	1	0	1	0	0	1	1	1	1	1	0	0	0	1	0
84	T	T	1	0	1	0	1	0	0	1	1	1	0	0	0	1	1
85	U	U	1	0	1	0	1	0	1	1	1	1	0	0	1	0	0
86	V	V	1	0	1	0	1	1	0	1	1	1	0	0	1	0	1
87	W	W	1	0	1	0	1	1	1	1	1	1	0	0	1	1	0
88	X	X	1	0	1	1	0	0	0	1	1	1	0	0	1	1	1
89	Y	Y	1	0	1	1	0	0	1	1	1	1	0	1	0	0	0
90	Z	Z	1	0	1	1	0	1	0	1	1	1	0	1	0	0	1
91	[	(	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1
92	\	\	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0
93	]	)	1	0	1	1	1	0	1	0	1	0	1	1	1	0	1
94	⌒ or ^	¬	1	0	1	1	1	1	0	0	1	0	1	1	1	1	1
95	–	–	1	0	1	1	1	1	1	0	1	1	0	1	1	0	1
96	Space	Space	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0
97	!	!	1	1	0	0	0	0	1	0	1	0	1	1	0	1	0
98	"	"	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1
99	#	#	1	1	0	0	0	1	1	0	1	1	1	1	0	1	1
100	$	$	1	1	0	0	1	0	0	0	1	0	1	1	0	1	1
101	%	%	1	1	0	0	1	0	1	0	1	1	0	1	1	0	0
102	&	&	1	1	0	0	1	1	0	0	1	0	1	0	0	0	0
103	'	'	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1
104	(	(	1	1	0	1	0	0	0	0	1	0	0	1	1	0	1
105	)	)	1	1	0	1	0	0	1	0	1	0	1	1	1	0	1
106	*	*	1	1	0	1	0	1	0	0	1	0	1	1	1	0	0
107	+	+	1	1	0	1	0	1	1	0	1	0	0	1	1	1	0
108	,	,	1	1	0	1	1	0	0	0	1	1	0	1	0	1	1
109	-	-	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0
110	.	.	1	1	0	1	1	1	0	0	1	0	0	1	0	1	1
111	/	/	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1
112	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
113	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1
114	2	2	1	1	1	0	0	1	0	1	1	1	1	0	0	1	0
115	3	3	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1
116	4	4	1	1	1	0	1	0	0	1	1	1	1	0	1	0	0
117	5	5	1	1	1	0	1	0	1	1	1	1	1	0	1	0	1
118	6	6	1	1	1	0	1	1	0	1	1	1	1	0	1	1	0
119	7	7	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
120	8	8	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0
121	9	9	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1
122	:	:	1	1	1	1	0	1	0	0	1	1	1	1	0	1	0
123	;	;	1	1	1	1	0	1	1	0	1	0	1	1	1	1	0
124	<	<	1	1	1	1	1	0	0	0	1	0	0	1	1	0	0
125	=	=	1	1	1	1	1	0	1	0	1	1	1	1	1	1	0
126	>	>	1	1	1	1	1	1	0	0	1	1	0	1	1	1	0
127	?	?	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1

ROM Code Converters

MM4220LR/MM5220LR BCDIC to ASCII-7/ ASCII-7 to BCDIC code converter

general description

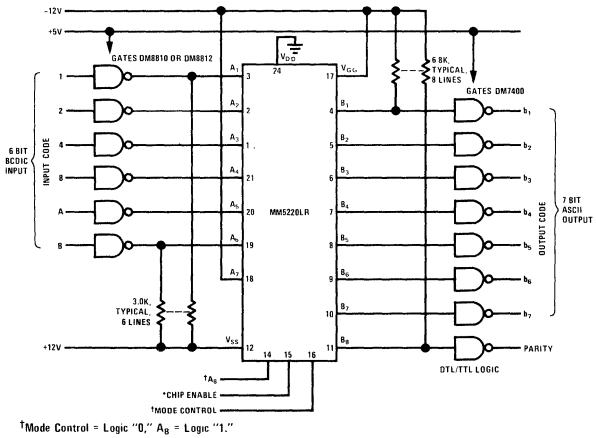
The MM4220LR/MM5220LR is a 128 x 8 read only memory which has been programmed to convert the 64 characters of the Binary Coded Decimal Interchange Code (BCDIC) to the American Standard code for Information Interchange in seven bits (ASCII-7).

The first half of the ROM, from address 0 to address 63, converts the 64 character ASCII graphic subset to BCDIC. The tables show the character assignments and their binary equivalents.

For electrical, environmental and mechanical details, refer to the MM4220/MM5220 data sheet.

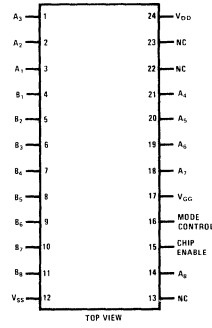
typical applications and connection diagram

BCDIC to ASCII



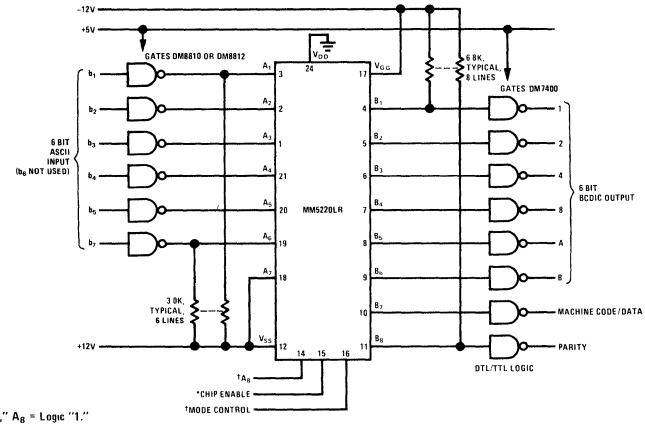
†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

Dual-In-Line Package



Order Number MM4220LR/J or MM5220LR/J
See Package 11
Order Number MM5220LR/N
See Package 18

ASCII to BCDIC



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

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code conversion tables

ASCII to BCDIC

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT BCDIC SYMBOL	CODE INPUT CODE E	ASCII b_7	b_5	b_4	b_3	b_2	b_1	OUTPUT MC/ DATA	EP	B	BCDIC A	8	4	2	1
0	SP	SP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	!	!	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0
2	"	+++	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1
3	#	#	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1
4	$	$	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1
5	%	%	0	0	0	0	1	0	1	0	1	0	1	1	1	0	0
6	&	&	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0
7	'	V	0	0	0	0	1	1	1	0	0	0	1	1	1	0	1
8	(	Blank	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0
9	)	Δ	0	0	0	1	0	0	1	0	1	1	0	1	1	1	1
10	*	*	0	0	0	1	0	1	0	0	1	1	0	1	1	0	0
11	VT	‡	0	0	0	1	0	1	1	1	0	0	1	1	0	1	0
12	,	,	0	0	0	1	1	0	0	0	0	0	1	1	0	1	1
13	CR	‡	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1
14	.	.	0	0	0	1	1	1	0	0	1	1	1	1	0	1	1
15	/	/	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1
16	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0
17	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	1
18	2	2	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0
19	3	3	0	0	1	0	0	1	1	0	0	0	0	0	0	1	1
20	4	4	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0
21	5	5	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1
22	6	6	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0
23	7	7	0	0	1	0	1	1	1	0	1	0	0	0	1	1	1
24	8	8	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0
25	9	9	0	0	1	1	0	0	1	0	0	0	0	1	0	0	1
26	:	:	0	0	1	1	0	1	0	0	1	0	0	1	1	0	1
27	;	;	0	0	1	1	0	1	1	0	0	1	0	1	1	1	0
28	<	<	0	0	1	1	1	0	0	0	1	1	1	1	1	1	0
29	=	√	0	0	1	1	1	0	1	0	0	0	0	1	1	1	1
30	>	>	0	0	1	1	1	1	0	0	1	0	0	1	1	1	0
31	?	?	0	0	1	1	1	1	1	0	0	1	1	1	0	1	0
32	@	@	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0
33	A	A	0	1	0	0	0	0	1	0	1	1	1	0	0	0	1
34	B	B	0	1	0	0	0	1	0	0	1	1	1	0	0	1	0
35	C	C	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1
36	D	D	0	1	0	0	1	0	0	0	1	1	1	0	1	0	0
37	E	E	0	1	0	0	1	0	1	0	0	1	1	0	1	0	1
38	F	F	0	1	0	0	1	1	0	0	0	1	1	0	1	1	0
39	G	G	0	1	0	0	1	1	1	0	1	1	1	0	1	1	1
40	H	H	0	1	0	1	0	0	0	0	1	1	1	1	0	0	0
41	I	I	0	1	0	1	0	0	1	0	0	1	1	1	0	0	1
42	J	J	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1
43	K	K	0	1	0	1	0	1	1	0	0	1	0	0	0	1	0
44	L	L	0	1	0	1	1	0	0	0	1	1	0	0	0	1	1
45	M	M	0	1	0	1	1	0	1	0	0	1	0	0	1	0	0
46	N	N	0	1	0	1	1	1	0	0	1	1	0	0	1	0	1
47	O	O	0	1	0	1	1	1	1	0	1	1	0	0	1	1	0
48	P	P	0	1	1	0	0	0	0	0	0	1	0	0	1	1	1
49	Q	Q	0	1	1	0	0	0	1	0	0	1	0	1	0	0	0
50	R	R	0	1	1	0	0	1	0	0	1	1	0	1	0	0	1
51	S	S	0	1	1	0	0	1	1	0	0	0	1	0	0	1	0
52	T	T	0	1	1	0	1	0	0	0	1	0	1	0	0	1	1
53	U	U	0	1	1	0	1	0	1	0	0	0	1	0	1	0	0
54	V	V	0	1	1	0	1	1	0	0	1	0	1	0	1	0	1
55	W	W	0	1	1	0	1	1	1	0	1	0	1	0	1	1	0
56	X	X	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1
57	Y	Y	0	1	1	1	0	0	1	0	0	0	1	1	0	0	0
58	Z	Z	0	1	1	1	0	1	0	0	1	0	1	1	0	0	1
59	[	[	0	1	1	1	0	1	1	0	1	1	1	1	1	0	1
60	\	\	0	1	1	1	1	0	0	0	0	0	1	1	1	1	0
61	]	]	0	1	1	1	1	0	1	0	0	1	0	1	1	0	1
62	^	¤	0	1	1	1	1	1	0	0	0	1	1	1	1	0	0
63	–	–	0	1	1	1	1	1	1	0	1	1	0	0	0	0	0
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

code conversion tables(con't)

BCDIC to ASCII

ROM ADDRESS	FUNCTION: INPUT BCDIC, SYMBOL	FUNCTION: OUTPUT ASCII SYMBOL	CODE: INPUT CODE	INPUT BCDIC B	A	8	4	2	1	PARITY	OUTPUT ASCII b_7	b_6	b_5	b_4	b_3	b_2	b_1
64	SP	SP	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
65	1	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	1
66	2	2	1	0	0	0	0	1	0	1	0	1	1	0	0	1	0
67	3	3	1	0	0	0	0	1	1	0	0	1	1	0	0	1	1
68	4	4	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0
69	5	5	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1
70	6	6	1	0	0	0	1	1	0	0	0	1	1	0	1	1	0
71	7	7	1	0	0	0	1	1	1	1	0	1	1	0	1	1	1
72	8	8	1	0	0	1	0	0	0	1	0	1	1	1	0	0	0
73	9	9	1	0	0	1	0	0	1	0	0	1	1	1	0	0	1
74	0	0	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0
75	#	#	1	0	0	1	0	1	1	1	0	1	0	0	0	1	1
76	@	@	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0
77	:	:	1	0	0	1	1	0	1	0	0	1	1	1	0	1	0
78	>	>	1	0	0	1	1	1	0	1	0	1	1	1	1	1	0
79	√	=	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1
80	Blank	(	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0
81	/	/	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1
82	S	S	1	0	1	0	0	1	0	0	1	0	1	0	0	1	1
83	T	T	1	0	1	0	0	1	1	1	1	0	1	0	1	0	0
84	U	U	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1
85	V	V	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0
86	W	W	1	0	1	0	1	1	0	1	1	0	1	0	1	1	1
87	X	X	1	0	1	0	1	1	1	1	1	0	1	1	0	0	0
88	Y	Y	1	0	1	1	0	0	0	0	1	0	1	1	0	0	1
89	Z	Z	1	0	1	1	0	0	1	0	1	0	1	1	0	1	0
90	†	VT	1	0	1	1	0	1	0	1	0	0	0	1	0	1	1
91	,	,	1	0	1	1	0	1	1	1	0	1	0	1	1	0	0
92	%	%	1	0	1	1	1	0	0	1	0	1	0	0	1	0	1
93	V	'	1	0	1	1	1	0	1	0	0	1	0	0	1	1	1
94	\	\	1	0	1	1	1	1	0	0	1	0	1	1	1	0	0
95	+++	"	1	0	1	1	1	1	1	0	0	1	0	0	0	1	0
96	–	–	1	1	0	0	0	0	0	0	1	0	1	1	1	1	1
97	J	J	1	1	0	0	0	0	1	1	1	0	0	1	0	1	0
98	K	K	1	1	0	0	0	1	0	0	1	0	0	1	0	1	1
99	L	L	1	1	0	0	0	1	1	1	1	0	0	1	1	0	0
100	M	M	1	1	0	0	1	0	0	0	1	0	0	1	1	0	1
101	N	N	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0
102	O	O	1	1	0	0	1	1	0	1	1	0	0	1	1	1	1
103	P	P	1	1	0	0	1	1	1	0	1	0	1	0	0	0	0
104	Q	Q	1	1	0	1	0	0	0	1	1	0	1	0	0	0	1
105	R	R	1	1	0	1	0	0	1	1	1	0	1	0	0	1	0
106	!	!	1	1	0	1	0	1	0	0	0	1	0	0	0	0	1
107	$	$	1	1	0	1	0	1	1	0	0	1	0	0	1	0	0
108	*	*	1	1	0	1	1	0	0	1	0	1	0	1	0	1	0
109	]	]	1	1	0	1	1	0	1	1	1	0	1	1	1	0	1
110	;	;	1	1	0	1	1	1	0	1	0	1	1	1	0	1	1
111	Δ	)	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1
112	&	&	1	1	1	0	0	0	0	1	0	1	0	0	1	1	0
113	A	A	1	1	1	0	0	0	1	0	1	0	0	0	0	0	1
114	B	B	1	1	1	0	0	1	0	0	1	0	0	0	0	1	0
115	C	C	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
116	D	D	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0
117	E	E	1	1	1	0	1	0	1	1	1	0	0	0	1	0	1
118	F	F	1	1	1	0	1	1	0	1	1	0	0	0	1	1	0
119	G	G	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1
120	H	H	1	1	1	1	0	0	0	0	1	0	0	1	0	0	0
121	I	I	1	1	1	1	0	0	1	1	1	0	0	1	0	0	1
122	?	?	1	1	1	1	0	1	0	0	0	1	1	1	1	1	1
123	.	.	1	1	1	1	0	1	1	0	0	1	0	1	1	1	0
124	¤	∩	1	1	1	1	1	0	0	1	1	0	1	1	1	1	0
125	[	[	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1
126	<	<	1	1	1	1	1	1	0	0	0	1	1	1	1	0	0
127	‡	CR	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM Code Converters

MM4221RQ/MM5221RQ ASCII-7 to EIA RS244A/ EIA RS244A to ASCII-7

general description

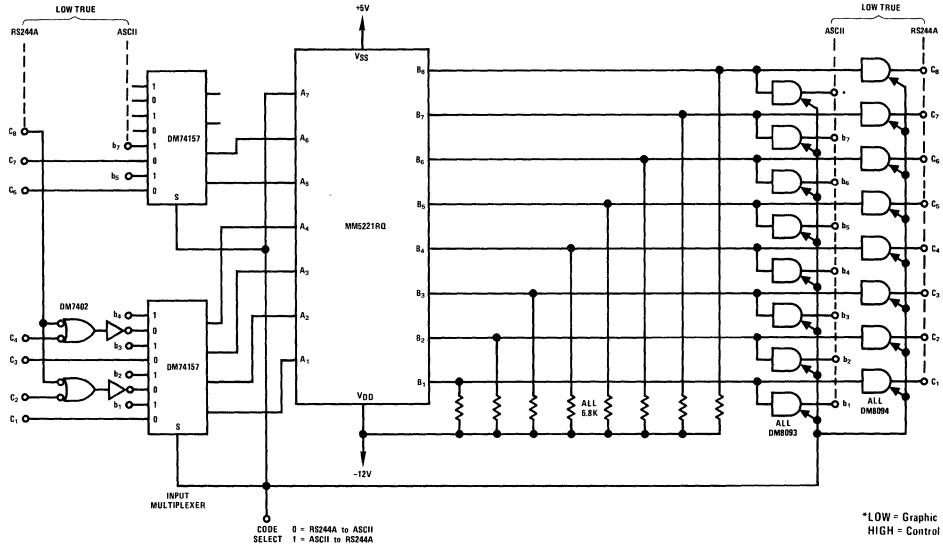
The MM4221RQ/MM5221RQ is a 1024-bit read only memory that has been programmed to convert between the American Standard Code for Information Interchange, compressed to six bits, and the Electronic Industries Association numerical control standard code, RS244A. The second group of addresses, from 64 to 127, effects the reverse conversion.

applications information

In the first 64 entries, compression of ASCII-7 to six bits has been accomplished by dropping bit b_6, and substituting the control codes listed for certain unused ASCII graphic symbols.

In the second 64 entries, the RS244A parity check bit, C_5 is ignored. The bit C_8, used only for the end of block code (EOB) is used externally to detect existence of this symbol, and to insert a redundant code, $C_4 \cdot C_2$ (ROM address 74). This code will be translated arbitrarily as an ASCII EXT.

typical application



Order Number MM4221RQ/J or MM5221RQ/J
See Package 11

Order Number MM5221RQ/N
See Package 18

code conversion tables

ASCII to RS244A

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EIA SYMBOL	CODE	CODE INPUT b_7	b_5	b_4	b_3	b_2	b_1	CODE OUTPUT c_8	c_7	c_6	c_5	c_4	c_3	c_2	c_1
0	SP	SP	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1			0	0	0	0	0	0	1								
2			0	0	0	0	0	1	0								
3	ETX	EOB	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
4	EOT	EOR	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1
5	%	%	0							0	1	0	1	1	0	1	1
6	&	&	0							0	0	0	0	1	1	1	0
7			0														
8	BS	BS	0							0	0	1	0	1	0	1	0
9	HT	TAB	0							0	0	1	1	1	1	1	0
10			0							0	0	0	0	0	0	0	0
11	+	+	0							0	1	1	1	0	0	0	0
12	,	,	0							0	0	1	1	1	0	1	1
13	–	–	0							0	1	0	0	0	0	0	0
14	.	.	0							0	1	1	0	1	0	1	1
15	/	/	0							0	0	1	1	0	0	0	1
16	0	0	0							0	0	1	0	0	0	0	0
17	1	1	0							0	0	0	0	0	0	0	1
18	2	2	0							0	0	0	0	0	0	1	0
19	3	3	0							0	0	0	1	0	0	1	1
20	4	4	0							0	0	0	0	0	1	0	0
21	5	5	0							0	0	0	1	0	1	0	1
22	6	6	0							0	0	0	1	0	1	1	0
23	7	7	0							0	0	0	0	0	1	1	1
24	8	8	0							0	0	0	0	1	0	0	0
25	9	9	0							0	0	0	1	1	0	0	1
26			0														
27		UC	0														
28	FS	LC	0							0	1	1	1	1	0	1	0
29	GS		0							0	1	1	1	1	1	0	0
30			0														
31			0														
32			0														
33	a	a	0							0	1	1	0	0	0	0	1
34	b	b	0							0	1	1	0	0	0	1	0
35	c	c	0							0	1	1	1	0	0	1	1
36	d	d	0							0	1	1	0	0	1	0	0
37	e	e	0							0	1	1	0	0	1	0	1
38	f	f	0							0	1	1	1	0	1	1	0
39	g	g	0							0	1	1	0	0	1	1	1
40	h	h	0							0	1	1	0	1	0	0	0
41	i	i	0							0	1	1	1	1	0	0	1
42	j	j	0							0	1	0	1	0	0	0	1
43	k	k	0							0	1	0	1	0	0	1	0
44	l	l	0							0	1	0	0	0	0	1	1
45	m	m	0							0	1	0	1	0	1	0	0
46	n	n	0							0	1	0	0	0	1	0	1
47	o	o	0							0	1	0	0	0	1	1	0
48	p	p	0							0	1	0	1	0	1	1	1
49	q	q	0							0	1	0	1	1	0	0	0
50	r	r	0							0	1	0	0	1	0	0	1
51	s	s	0							0	0	1	1	0	0	1	0
52	t	t	0							0	0	1	0	0	0	1	1
53	u	u	0							0	0	1	1	0	1	0	0
54	v	v	0							0	0	1	0	0	1	0	1
55	w	w	0							0	0	1	0	0	1	1	0
56	x	x	0							0	0	1	1	0	1	1	1
57	y	y	0							0	0	1	1	1	0	0	0
58	z	z	0							0	0	1	0	1	0	0	1
59			0														
60			0														
61			0														
62			0														
63	DEL	DEL	0							0	1	1	1	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

Increasing Binary Sequence

code conversion tables(con't)

RS244A to ASCII

ROM ADDRESS	FUNCTION INPUT EIA SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE	CODE INPUT c_7	c_6	c_4	c_3	c_2	c_1	OUTPUT CC/G	b_7	b_6	b_5	b_4	b_3	b_2	b_1
64	Space	Space	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0
65	1	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	1
66	2	2	1	0	0	0	0	1	0	1	0	1	1	0	0	1	0
67	3	3	1	0	0	0	0	1	1	1	0	1	1	0	0	1	1
68	4	4	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0
69	5	5	1	0	0	0	1	0	1	1	0	1	1	0	1	0	1
70	6	6	1							1	0	1	1	0	1	1	0
71	7	7	1							1	0	1	1	0	1	1	1
72	8	8	1							1	0	1	1	1	0	0	0
73	9	9	1							1	0	1	1	1	0	0	1
74	EOB	ETX	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1
75	EOR	EOT	1							0	0	0	0	0	1	0	0
76			1														
77			1														
78	&	&	1							1	0	1	0	0	1	1	0
79			1														
80	0	0	1							1	0	1	1	0	0	0	0
81	1	1	1							1	0	1	0	1	1	1	1
82	s	s	1							1	1	1	1	0	0	1	1
83	t	t	1							1	1	1	1	0	1	0	0
84	u	u	1							1	1	1	1	0	1	0	1
85	v	v	1							1	1	1	1	0	1	1	0
86	w	w	1							1	1	1	1	0	1	1	1
87	x	x	1							1	1	1	1	1	0	0	0
88	y	y	1							1	1	1	1	1	0	0	1
89	z	z	1							1	1	1	1	1	0	1	0
90	BS	BS	1							0	0	0	0	1	0	0	0
91	,	,	1							1	0	1	0	1	1	0	0
92			1														
93			1														
94	TAB	HT	1							0	0	0	0	1	0	0	1
95			1														
96	–	–	1	1	0	0	0	0	0	1	0	1	0	1	1	0	1
97	j	j	1	1	0	0	0	0	1	1	1	1	0	1	0	1	0
98	k	k	1							1	1	1	0	1	0	1	1
99	l	l	1							1	1	1	0	1	1	0	0
100	m	m	1							1	1	1	0	1	1	0	1
101	n	n	1							1	1	1	0	1	1	1	0
102	o	o	1							1	1	1	0	1	1	1	1
103	p	p	1							1	1	1	1	0	0	0	0
104	q	q	1							1	1	1	1	0	0	0	1
105	r	r	1							1	1	1	1	0	0	1	0
106			1														
107	%	%	1							1	0	1	0	0	1	0	1
108			1														
109			1														
110			1														
111			1														
112	+	+	1							1	0	1	0	1	0	1	1
113	a	a	1							1	1	1	0	0	0	0	1
114	b	b	1							1	1	1	0	0	0	1	0
115	c	c	1							1	1	1	0	0	0	1	1
116	d	d	1							1	1	1	0	0	1	0	0
117	e	e	1							1	1	1	0	0	1	0	1
118	f	f	1							1	1	1	0	0	1	1	0
119	g	g	1							1	1	1	0	0	1	1	1
120	h	h	1							1	1	1	0	1	0	0	0
121	i	i	1							1	1	1	0	1	0	0	1
122	LC	GS	1							0	0	0	1	1	1	0	1
123	.	.	1							1	0	1	0	1	1	1	0
124	UC	FS	1							0	0	0	1	1	1	0	0
125			1														
126			1														
127	DEL	DEL	1							0	1	1	1	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

Increasing Binary Sequence

ROM Code Converters

MM4221RR/MM5221RR ASCII-7 to EBCDIC code converter

general description

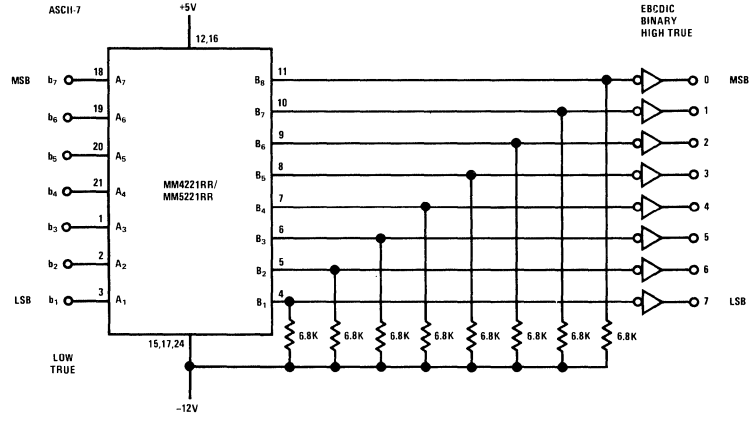
The MM4221RR/MM5221RR is a 1024-bit read-only memory that has been programmed to convert between the 128 characters of ASCII-7, the American Standard Code for Information Interchange in seven bits, and EBCDIC, an extended binary coded decimal interchange code. This conversion follows the EBCDIC character assignments used in the IBM 1130 computer.

Certain arbitrary assignments have also been made for maximum usefulness, and in these two areas the part differs from the MM4230QY/MM5230QY, which follows American National Standard ANSI X3.26 recommendations for character assignments.

For electrical, environmental and mechanical details, refer to the MM4221/MM5221 data sheet.

typical application

ASCII-7 to EBCDIC



Order Number MM4221RR/J or MM5221RR/J
See Package 11
Order Number MM5221RR/N
See Package 18

code conversion tables

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT MSB						LSB	CODE OUTPUT MSB							LSB
0	NULL	NULL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	SOH	SOH	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
2	STX	STX	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
3	ETX	ETX	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
4	EOT	EOT	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1
5	ENQ	ENQ	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1
6	ACK	ACK	0	0	0	0	1	1	0	0	0	1	0	1	1	1	0
7	BEL	BEL	0	0	0	0	1	1	1	0	0	1	0	1	1	1	1
8	BS	BS	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0
9	HT	HT	0	0	0	1	0	0	1	0	0	0	0	0	1	0	1
10	LF	LF	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1
11	VT	VT	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1
12	FF	FF	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0
13	CR	CR	0	0	0	1	1	0	1	0	0	0	0	1	1	0	1
14	S0	S0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0
15	S1	S1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
16	DLE	DLE	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
17	DC1	DC1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
18	DC2	DC2								0	0	0	1	0	0	1	0
19	DC3	DC3								0	0	0	1	0	0	1	1
20	DC4	RS								0	0	1	1	0	1	0	1
21	NAK	NAK								0	0	1	1	1	1	0	1
22	SYN	SYN								0	0	1	1	0	0	1	0
23	ETB	EOB								0	0	1	0	0	1	1	0
24	CAN	CAN								0	0	0	1	1	0	0	0
25	EM	EM								0	0	0	1	1	0	0	1
26	SUB	SUB								0	0	1	1	1	1	1	1
27	ESC	BYP								0	0	1	0	0	1	0	0
28	FS	FLS								0	0	0	1	1	1	0	0
29	GS	GS								0	0	0	1	1	1	0	1
30	RS	RDS								0	0	0	1	1	1	1	0
31	US	US								0	0	0	1	1	1	1	1
32	SP	SP	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
33	!	!								0	1	0	1	1	0	1	0
34	"	"								0	1	1	1	1	1	1	1
35	#	#								0	1	1	1	1	0	1	1
36	$	$								0	1	0	1	1	0	1	1
37	%	%								0	1	1	0	1	1	0	0
38	&	&								0	1	0	1	0	0	0	0
39	'	'								0	1	1	1	1	1	0	1
40	(	(								0	1	0	0	1	1	0	1
41	)	)								0	1	0	1	1	1	0	1
42	*	*								0	1	0	1	1	1	0	0
43	+	+								0	1	0	0	1	1	1	0
44	,	,								0	1	1	0	1	0	1	1
45	–	–								0	1	1	0	0	0	0	0
46	.	.								0	1	0	0	1	0	1	1
47	/	/								0	1	1	0	0	0	0	1
48	0	0								1	1	1	1	0	0	0	0
49	1	1								1	1	1	1	0	0	0	1
50	2	2								1	1	1	1	0	0	1	0
51	3	3								1	1	1	1	0	0	1	1
52	4	4								1	1	1	1	0	1	0	0
53	5	5								1	1	1	1	0	1	0	1
54	6	6								1	1	1	1	0	1	1	0
55	7	7								1	1	1	1	0	1	1	1
56	8	8								1	1	1	1	1	0	0	0
57	9	9								1	1	1	1	1	0	0	1
58	:	:								0	1	1	1	1	0	1	0
59	;	;								0	1	0	1	1	1	1	0
60	<	<								0	1	0	0	1	1	0	0
61	=	=								0	1	1	1	1	1	1	0
62	>	>								0	1	1	0	1	1	1	0
63	?	?								0	1	1	0	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

CONTINUING BINARY SEQUENCE

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT MSB						LSB	CODE OUTPUT MSB							LSB
64	@	@	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
65	A	A								1	1	0	0	0	0	0	1
66	B	B								1	1	0	0	0	0	1	0
67	C	C								1	1	0	0	0	0	1	1
68	D	D								1	1	0	0	0	1	0	0
69	E	E								1	1	0	0	0	1	0	1
70	F	F								1	1	0	0	0	1	1	0
71	G	G								1	1	0	0	0	1	1	1
72	H	H								1	1	0	0	1	0	0	0
73	I	I								1	1	0	0	1	0	0	1
74	J	J								1	1	0	1	0	0	0	1
75	K	K								1	1	0	1	0	0	1	0
76	L	L								1	1	0	1	0	0	1	1
77	M	M								1	1	0	1	0	1	0	0
78	N	N								1	1	0	1	0	1	0	1
79	O	O								1	1	0	1	0	1	1	0
80	P	P								1	1	0	1	0	1	1	1
81	Q	Q				CONTINUING BINARY SEQUENCE				1	1	0	1	1	0	0	0
82	R	R								1	1	0	1	1	0	0	1
83	S	S								1	1	1	0	0	0	1	0
84	T	T								1	1	1	0	0	0	1	1
85	U	U								1	1	1	0	0	1	0	0
86	V	V								1	1	1	0	0	1	0	1
87	W	W								1	1	1	0	0	1	1	0
88	X	X								1	1	1	0	0	1	1	1
89	Y	Y								1	1	1	0	1	0	0	0
90	Z	Z								1	1	1	0	1	0	0	1
91	[	[								1	0	1	0	1	1	0	1
92	\	NL								0	0	0	1	0	1	0	1
93	]	]								1	0	1	1	1	1	0	1
94	^	¬								0	1	0	1	1	1	1	1
95	–	–								0	1	1	0	1	1	0	1
96	`	RES	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0
97	a	a								1	0	0	0	0	0	0	1
98	b	b								1	0	0	0	0	0	1	0
99	c	c								1	0	0	0	0	0	1	1
100	d	d								1	0	0	0	0	1	0	0
101	e	e								1	0	0	0	0	1	0	1
102	f	f								1	0	0	0	0	1	1	0
103	g	g								1	0	0	0	0	1	1	1
104	h	h								1	0	0	0	1	0	0	0
105	i	i								1	0	0	0	1	0	0	1
106	j	j								1	0	0	1	0	0	0	1
107	k	k								1	0	0	1	0	0	1	0
108	l	l								1	0	0	1	0	0	1	1
109	m	m								1	0	0	1	0	1	0	0
110	n	n								1	0	0	1	0	1	0	1
111	o	o								1	0	0	1	0	1	1	0
112	p	p								1	0	0	1	0	1	1	1
113	q	q								1	0	0	1	1	0	0	0
114	r	r								1	0	0	1	1	0	0	1
115	s	s								1	0	1	0	0	0	1	0
116	t	t								1	0	1	0	0	0	1	1
117	u	u								1	0	1	0	0	1	0	0
118	v	v								1	0	1	0	0	1	0	1
119	w	w								1	0	1	0	0	1	1	0
120	x	x								1	0	1	0	0	1	1	1
121	y	y								1	0	1	0	1	0	0	0
122	z	z								1	0	1	0	1	0	0	1
123	{	{								1	0	0	0	1	0	1	1
124	¦	¦								0	1	0	0	1	1	1	1
125	}	}								1	0	0	1	1	0	1	1
126	~	¢								0	1	0	0	1	0	1	0
127	DEL	DEL								0	0	0	0	0	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

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ROM Code Converters

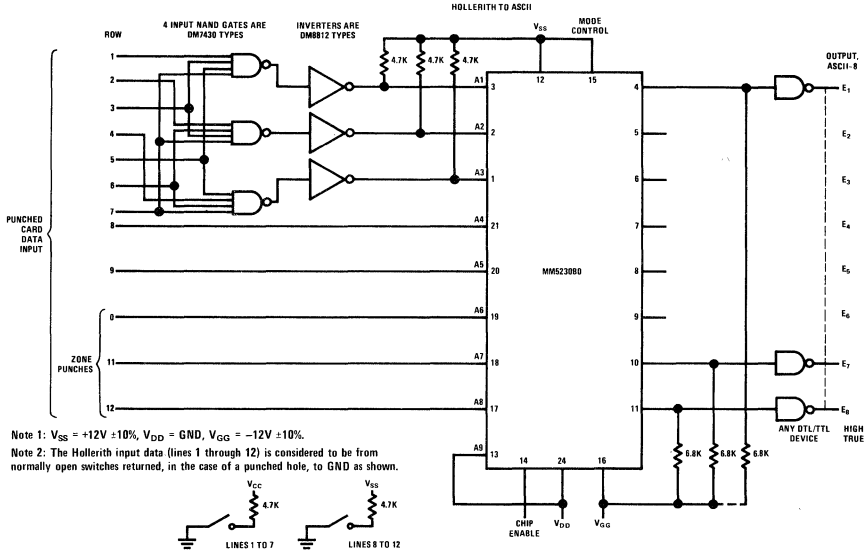
MM4230BO/MM5230BO hollerith to ASCII code converter

general description

The MM4230BO/MM5230BO 2048-bit MOS read-only memory has been programmed to convert the 12 line Hollerith punched card code to eight level ASCII. This conversion conforms to the American National Standard (ANSI x 3.26 – 1970). Three TTL 4-input NAND gates, and three inverters are used to compress the 12 Hollerith lines to eight-line binary encoded form suitable for use by the read-only memory. This application is shown below.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

typical application

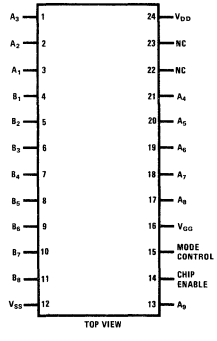


Note 1: V_{SS} = +12V ±10%, V_{DD} = GND, V_{GG} = −12V ±10%.

Note 2: The Hollerith input data (lines 1 through 12) is considered to be from normally open switches returned, in the case of a punched hole, to GND as shown.

connection diagram

Dual-In-Line Package



Order Number MM4230BO-1/J or MM5230BO-1/J
See Package 11
Order Number MM5230BO-1/N
See Package 18

code conversion table

Hollerith to ASCII

	12	11	0		12 0	12 11	11 0	12 11 0	12	11	0		12 0	12 11	11 0	12 11 0	
	&	-	ϕ	SP	{	¦	}	11/10	10/8	11/1	11/9	`	12/3	12/10	13/1	13/8	8-1
1	A	J	/	1	a	j	~	13/9	SOH	DC1	8/1	9/1	10/0	10/9	9/15	11/11	9 -1
2	B	K	S	2	b	k	s	13/10	STX	DC2	8/2	SYN	10/1	10/10	11/2	11/12	9 -2
3	C	L	T	3	c	l	t	13/11	ETX	DC3	8/3	9/3	10/2	10/11	11/3	11/13	9 -3
4	D	M	U	4	d	m	u	13/12	9/12	9/13	8/4	9/4	10/3	10/12	11/4	11/14	9 -4
5	E	N	V	5	e	n	v	13/13	HT	8/5	LF	9/5	10/4	10/13	11/5	11/15	9 -5
6	F	O	W	6	f	o	w	13/14	8/6	BS	ETB	9/6	10/5	10/14	11/6	12/0	9 -6
7	G	P	X	7	g	p	x	13/15	DEL	8/7	ESC	EOT	10/6	10/15	11/7	12/1	9 -7
8	H	Q	Y	8	h	q	y	14/0	9/7	CAN	8/8	9/8	10/7	11/0	11/8	12/2	9 -8
9	I	R	Z	9	i	r	z	14/1	8/13	EM	8/9	9/9	NUL	DLE	8/0	9/0	9-8-1
8-2	[	]	\	:	12/4	12/11	13/2	14/2	8/14	9/2	8/10	9/10	14/8	14/14	15/4	15/10	9-8-2
8-3	.	$	,	#	12/5	12/12	13/3	14/3	VT	8/15	8/11	9/11	14/9	14/15	15/5	15/11	9-8-3
8-4	<	*	%	@	12/6	12/13	13/4	14/4	FF	FS	8/12	DC4	14/10	15/0	15/6	15/12	9-8-4
8-5	(	)	_	'	12/7	12/14	13/5	14/5	CR	GS	ENQ	NAK	14/11	15/1	15/7	15/13	9-8-5
8-6	+	;	>	=	12/8	12/15	13/6	14/6	SO	RS	ACK	9/14	14/12	15/2	15/8	15/14	9-8-6
8-7	! ①	^ ②	?	"	12/9	13/0	13/7	14/7	SI	US	BEL	SUB	14/13	15/3	15/9	15/15	9-8-7

① may be "|"
② may be "¬"

Note: The entries of Form A/B refer to the unassigned locations in the right hand side of the ASII table (bit E_8 = 1) designated for specialist use. (See National Bureau of Standards Technical Note No. 478.

Note: For the full ASCII-8 Code Table, see MM4230QY/MM5230QY data sheet.

ROM Code Converters

MM4230FE/MM5230FE selectric-to-EBCDIC/ EBCDIC-to-selectric code converter

general description

The MM4230FE/MM5230FE provides for the conversion of IBM Selectric Correspondence Code to Extended Binary Coded Decimal Interchange Code (EBCDIC) in both directions. These two decoders are contained on a monolithic MOS device.

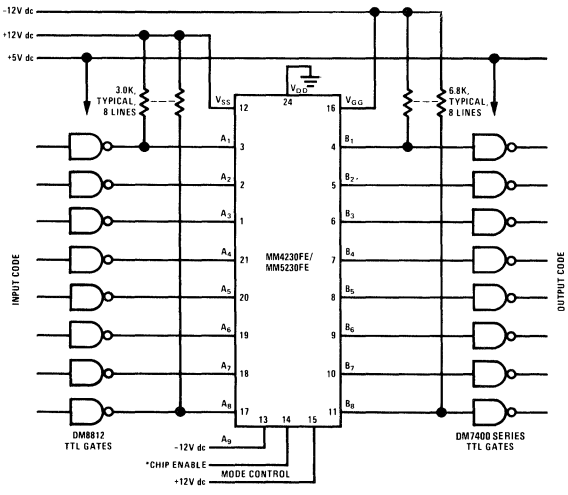
The Selectric-to-EBCDIC converter is located in binary addresses 0 through 127. Input bit A7 is used as a single line command to determine whether upper (denoted by a "1") or a lower (denoted by a "0") case has been selected.

The EBCDIC-to-Selectric converter is located in binary addresses 128 through 255. Since not all EBCDIC control commands have Selectric code counterparts, it is not necessary to encode bit position 0 (A8), which is used instead as the code converter selection bit. In addition to the Selectric Correspondence output code bits there is a bit to indicate upper or lower case. The odd parity bit generated does not account for the case bit.

device characteristics

For full electrical, environmental, and mechanical details refer to the MM4230/MM5230 2048-bit read only memory data sheet.

typical application

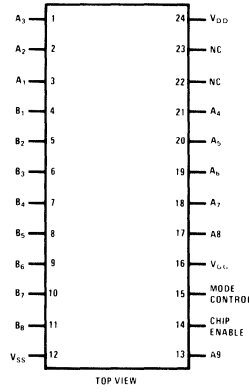


*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM, Logic "0" ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative, Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4230FE/J or MM5230FE/J
See Package 11

Order Number MM5230FE/N
See Package 18

code conversion table—selectric-to-EBCDIC

ROM ADDRESS	FUNCTION INPUT SELECTRIC SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT CODE E	CASE	R_5	R_2	R_1	R_{2A}	T_1	T_2	OUTPUT EBCDIC 0	1	2	3	4	5	6	7
0	–	–	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
1	b	b	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0
2	w	w	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	0
3	9	9	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1
4	q	q	0	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0
5	k	k	0	0	0	0	0	1	0	1	1	0	0	1	0	0	1	0
6	i	i	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0	1
7	6	6	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0
8	y	y	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0
9	h	h	0	0	0	0	1	0	0	1	1	0	0	0	1	0	0	0
10	s	s	0	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0
11	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0
12	p	p	0	0	0	0	1	1	0	0	1	0	0	1	0	1	1	1
13	e	e	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	1
14	'	'	0	0	0	0	1	1	1	0	0	1	1	1	1	1	0	1
15	5	5	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	1
16		NULL	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17		NULL	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
18		NULL	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
19		NULL	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
20	=	=	0	0	0	1	0	1	0	0	0	1	1	1	1	1	1	0
21	n	n	0	0	0	1	0	1	0	1	1	0	0	1	0	1	0	1
22	.	.	0	0	0	1	0	1	1	0	0	1	0	0	1	0	1	1
23	2	2	0	0	0	1	0	1	1	1	1	1	1	1	0	0	1	0
24		NULL	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
25		NULL	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0
26		NULL	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
27		NULL	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0
28	j	j	0	0	0	1	1	1	0	0	1	0	0	1	0	0	0	1
29	t	t	0	0	0	1	1	1	0	1	1	0	1	0	0	0	1	1
30		NULL	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
31	z	z	0	0	0	1	1	1	1	1	1	0	1	0	1	0	0	1
32		NULL	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
33		NULL	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
34		NULL	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
35		NULL	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0
36	,	,	0	0	1	0	0	1	0	0	0	1	1	0	1	0	1	1
37	c	c	0	0	1	0	0	1	0	1	1	0	0	0	0	0	1	1
38	a	a	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	1
39	8	8	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0	0
40	/	/	0	0	1	0	1	0	0	0	0	1	1	0	0	0	0	1
41	l	l	0	0	1	0	1	0	0	1	1	0	0	1	0	0	1	1
42	o	o	0	0	1	0	1	0	1	0	1	0	0	1	0	1	1	0
43	4	4	0	0	1	0	1	0	1	1	1	1	1	1	0	1	0	0
44	;	;	0	0	1	0	1	1	0	0	0	1	0	1	1	1	1	0
45	d	d	0	0	1	0	1	1	0	1	1	0	0	0	0	1	0	0
46	r	r	0	0	1	0	1	1	1	0	1	0	0	1	1	0	0	1
47	7	7	0	0	1	0	1	1	1	1	1	1	1	1	0	1	1	1
48		NULL	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
49		NULL	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
50		NULL	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
51		NULL	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
52	f	f	0	0	1	1	0	1	0	0	1	0	0	0	0	1	1	0
53	u	u	0	0	1	1	0	1	0	1	1	0	1	0	0	1	0	0
54	v	v	0	0	1	1	0	1	1	0	1	0	1	0	0	1	0	1
55	3	3	0	0	1	1	0	1	1	1	1	1	1	1	0	0	1	1
56		NULL	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
57		NULL	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0
58		NULL	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
59		NULL	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
60	g	g	0	0	1	1	1	1	0	0	1	0	0	0	0	1	1	1
61	x	x	0	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1
62	m	m	0	0	1	1	1	1	1	0	1	0	0	1	0	1	0	0
63	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

8

code conversion table—selectric-to-EBCDIC(con't)

ROM ADDRESS	FUNCTION INPUT SELECTRIC SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT CODE	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2	OUTPUT EBCDIC 0	1	2	3	4	5	6	7
64	–	–	0	1	0	0	0	0	0	0	0	1	1	0	1	1	0	1
65	B	B	0	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0
66	W	W	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	0
67	(	(	0	1	0	0	0	0	1	1	0	1	0	0	1	1	0	1
68	Q	Q	0	1	0	0	0	1	0	0	1	1	0	1	1	0	0	0
69	K	K	0	1	0	0	0	1	0	1	1	1	0	1	0	0	1	0
70	I	I	0	1	0	0	0	1	1	0	1	1	0	0	1	0	0	1
71	¢	¢	0	1	0	0	0	1	1	1	0	1	0	0	1	0	1	0
72	Y	Y	0	1	0	0	1	0	0	0	1	1	1	0	1	0	0	0
73	H	H	0	1	0	0	1	0	0	1	1	1	0	0	1	0	0	0
74	S	S	0	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0
75	)	)	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	1
76	P	P	0	1	0	0	1	1	0	0	1	1	0	1	0	1	1	1
77	E	E	0	1	0	0	1	1	0	1	1	1	0	0	0	1	0	1
78	"	"	0	1	0	0	1	1	1	0	0	1	1	1	1	1	1	1
79	%	%	0	1	0	0	1	1	1	1	0	1	1	0	1	1	0	0
80		NULL	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
81		NULL	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0
82		NULL	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
83		NULL	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0
84	+	+	0	1	0	1	0	1	0	0	0	1	0	0	1	1	1	0
85	N	N	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1
86	.	.	0	1	0	1	0	1	1	0	0	1	0	0	1	0	1	1
87	@	@	0	1	0	1	0	1	1	1	0	1	1	1	1	1	0	0
88		NULL	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
89		NULL	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0
90		NULL	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
91		NULL	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0
92	J	J	0	1	0	1	1	1	0	0	1	1	0	1	0	0	0	1
93	T	T	0	1	0	1	1	1	0	1	1	1	1	0	0	0	1	1
94		NULL	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0
95	Z	Z	0	1	0	1	1	1	1	1	1	1	1	0	1	0	0	1
96		NULL	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
97		NULL	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0
98		NULL	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
99		NULL	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0
100	,	,	0	1	1	0	0	1	0	0	0	1	1	0	1	0	1	1
101	C	C	0	1	1	0	0	1	0	1	1	1	0	0	0	0	1	1
102	A	A	0	1	1	0	0	1	1	0	1	1	0	0	0	0	0	1
103	*	*	0	1	1	0	0	1	1	1	0	1	0	1	1	1	0	0
104	?	?	0	1	1	0	1	0	0	0	0	1	1	0	1	1	1	1
105	L	L	0	1	1	0	1	0	0	1	1	1	0	1	0	0	1	1
106	O	O	0	1	1	0	1	0	1	0	1	1	0	1	0	1	1	0
107	$	$	0	1	1	0	1	0	1	1	0	1	0	1	1	0	1	1
108	:	:	0	1	1	0	1	1	0	0	0	1	1	1	1	0	1	0
109	D	D	0	1	1	0	1	1	0	1	1	1	0	0	0	1	0	0
110	R	R	0	1	1	0	1	1	1	0	1	1	0	1	1	0	0	1
111	&	&	0	1	1	0	1	1	1	1	0	1	0	1	1	0	0	0
112		NULL	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
113		NULL	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
114		NULL	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0
115		NULL	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0
116	F	F	0	1	1	1	0	1	0	0	1	1	0	0	0	1	1	0
117	U	U	0	1	1	1	0	1	0	1	1	1	1	0	0	1	0	0
118	V	V	0	1	1	1	0	1	1	0	1	1	1	0	0	1	0	1
119	#	#	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	1
120		NULL	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
121		NULL	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
122		NULL	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
123		NULL	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
124	G	G	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1	1
125	X	X	0	1	1	1	1	1	0	1	1	1	1	0	0	1	1	1
126	M	M	0	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0
127	±	NULL	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

code conversion table—EBCDIC-to-selectric

ROM ADDRESS	FUNCTION INPUT: EBCDIC SYMBOL	FUNCTION OUTPUT: SELECTRIC SYMBOL	CODE INPUT: CODE	EBCDIC 1	EBCDIC 2	EBCDIC 3	EBCDIC 4	EBCDIC 5	EBCDIC 6	EBCDIC 7	OUTPUT: PARITY	OUTPUT: CASE	SELECTRIC R_5	SELECTRIC R_2	SELECTRIC R_1	SELECTRIC R_{2A}	SELECTRIC T_1	SELECTRIC T_2
128	NUL	–	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
129	SOH a	a	1	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0
130	STX b	b	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
131	ETX c	c	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1
132	PF d	d	1	0	0	0	0	1	0	0	1	0	1	0	1	1	0	1
133	HT e	e	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1
134	LC f	f	1	0	0	0	0	1	1	0	0	0	1	1	0	1	0	0
135	DEL g	g	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0
136	h	h	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1
137	i	i	1	0	0	0	1	0	0	1	1	0	0	0	0	1	1	0
138	SMM	–	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
139	VT	–	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0
140	FF	–	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
141	CR	–	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0
142	SO	–	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
143	SI	–	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
144	DLE	–	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
145	DC1 j	j	1	0	0	1	0	0	0	1	0	0	0	1	1	1	0	0
146	DC2 k	k	1	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1
147	TM l	l	1	0	0	1	0	0	1	1	0	0	1	0	1	0	0	1
148	RES m	m	1	0	0	1	0	1	0	0	0	0	1	1	1	1	1	0
149	NL n	n	1	0	0	1	0	1	0	1	0	0	0	1	0	1	0	1
150	BS o	o	1	0	0	1	0	1	1	0	0	0	1	0	1	0	1	0
151	IL p	p	1	0	0	1	0	1	1	1	1	0	0	0	1	1	0	0
152	CAN q	q	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0
153	EM r	r	1	0	0	1	1	0	0	1	1	0	1	0	1	1	1	0
154	CC	–	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
155	CU1	–	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0
156	IFS	–	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
157	IGS	–	1	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0
158	IRS	–	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
159	IUS	–	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0
160	DS	–	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
161	SOS	–	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
162	FS s	s	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0
163	t	t	1	0	1	0	0	0	1	1	1	0	0	1	1	1	0	1
164	BYP u	u	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	1
165	LF v	v	1	0	1	0	0	1	0	1	1	0	1	1	0	1	1	0
166	ETB w	w	1	0	1	0	0	1	1	0	0	0	0	0	0	0	1	0
167	ESC x	x	1	0	1	0	0	1	1	1	0	0	1	1	1	1	0	1
168	y	y	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0
169	z	z	1	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1
170	SM	–	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
171	CU2	–	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0
172		–	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
173	ENQ	–	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0
174	ACK	–	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
175	BEL	–	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0
176		–	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
177		–	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
178	SYN	–	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
179		–	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
180	PN	–	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
181	RS	–	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0
182	UC	–	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
183	EOT	–	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0
184		–	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
185		–	1	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0
186		–	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
187	CU3	–	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
188	DC4	–	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
189	NAK	–	1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0
190		–	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0
191	SUB	–	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

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code conversion table—EBCDIC-to-selectric(con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT SELECTRIC SYMBOL	CODE INPUT EBCDIC CODE	1	2	3	4	5	6	7	OUTPUT PARITY	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2
192	Space	—	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
193	A	A	1	1	0	0	0	0	0	1	0	1	1	0	0	1	1	0
194	B	B	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1
195	C	C	1	1	0	0	0	0	1	1	0	1	1	0	0	1	0	1
196	D	D	1	1	0	0	0	1	0	0	1	1	1	0	1	1	0	1
197	E	E	1	1	0	0	0	1	0	1	0	1	0	0	1	1	0	1
198	F	F	1	1	0	0	0	1	1	0	0	1	1	1	0	1	0	0
199	G	G	1	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0
200	H	H	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1
201	I	I	1	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0
202	¢	¢	1	1	0	0	1	0	1	0	0	1	0	0	0	1	1	1
203	.	.	1	1	0	0	1	0	1	1	0	0	0	1	0	1	1	0
204	<	—	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
205	(	(	1	1	0	0	1	1	0	1	1	1	0	0	0	0	1	1
206	+	+	1	1	0	0	1	1	1	0	1	1	0	1	0	1	0	0
207	'	—	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
208	&	&	1	1	0	1	0	0	0	0	0	1	1	0	1	1	1	1
209	J	J	1	1	0	1	0	0	0	1	0	1	0	1	1	1	0	0
210	K	K	1	1	0	1	0	0	1	0	1	1	0	0	0	1	0	1
211	L	L	1	1	0	1	0	0	1	1	0	1	1	0	1	0	0	1
212	M	M	1	1	0	1	0	1	0	0	0	1	1	1	1	1	1	0
213	N	N	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
214	O	O	1	1	0	1	0	1	1	0	0	1	1	0	1	0	1	0
215	P	P	1	1	0	1	0	1	1	1	1	1	0	0	1	1	0	0
216	Q	Q	1	1	0	1	1	0	0	0	0	1	0	0	0	1	0	0
217	R	R	1	1	0	1	1	0	0	1	1	1	1	0	1	1	1	0
218	!	—	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
219	$	$	1	1	0	1	1	0	1	1	1	1	1	0	1	0	1	1
220	★ or *	*	1	1	0	1	1	1	0	0	1	1	1	0	0	1	1	1
221	)	)	1	1	0	1	1	1	0	1	0	1	0	0	1	0	1	1
222	;	;	1	1	0	1	1	1	1	0	0	0	1	0	1	1	0	0
223	¬	—	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0
224	—	—	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
225	/	/	1	1	1	0	0	0	0	1	1	0	1	0	1	0	0	0
226	S	S	1	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0
227	T	T	1	1	1	0	0	0	1	1	1	1	0	1	1	1	0	1
228	U	U	1	1	1	0	0	1	0	0	1	1	1	1	0	1	0	1
229	V	V	1	1	1	0	0	1	0	1	1	1	1	1	0	1	1	0
230	W	W	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0
231	X	X	1	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1
232	Y	Y	1	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0
233	Z	Z	1	1	1	0	1	0	0	1	0	1	0	1	1	1	1	1
234		—	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
235	,	,	1	1	1	0	1	0	1	1	1	0	1	0	0	1	0	0
236	%	%	1	1	1	0	1	1	0	0	1	1	0	0	1	1	1	1
237	- or —	–	1	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0
238	>	–	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0
239	?	?	1	1	1	0	1	1	1	1	1	1	1	0	1	0	0	0
240	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	1
241	1	1	1	1	1	1	0	0	0	1	1	0	1	1	1	1	1	1
242	2	2	1	1	1	1	0	0	1	0	1	0	0	1	0	1	1	1
243	3	3	1	1	1	1	0	0	1	1	0	0	1	1	0	1	1	1
244	4	4	1	1	1	1	0	1	0	0	1	0	1	0	1	0	1	1
245	5	5	1	1	1	1	0	1	0	1	1	0	0	0	1	1	1	1
246	6	6	1	1	1	1	0	1	1	0	0	0	0	0	0	1	1	1
247	7	7	1	1	1	1	0	1	1	1	0	0	1	0	1	1	1	1
248	8	8	1	1	1	1	1	0	0	0	1	0	1	0	0	1	1	1
249	9	9	1	1	1	1	1	0	0	1	1	0	0	0	0	0	1	1
250	:	:	1	1	1	1	1	0	1	0	0	1	1	0	1	1	0	0
251	#	#	1	1	1	1	1	0	1	1	0	1	1	1	0	1	1	1
252	@	@	1	1	1	1	1	1	0	0	1	1	0	1	0	1	1	1
253	'	'	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	0
254	=	=	1	1	1	1	1	1	1	0	1	0	0	1	0	1	0	0
255	"	"	1	1	1	1	1	1	1	1	0	1	0	0	1	1	1	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

ROM Code Converters

MM4230JT/MM5230JT BCDIC to EBCDIC/ EBCDIC to BCDIC code converter

general description

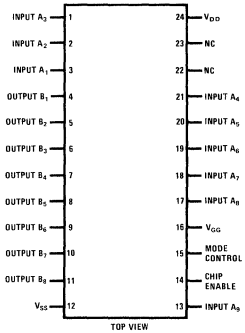
The MM4230JT/MM5230JT is a 2048-bit read-only memory that has been programmed to convert from the 64-entry, 6-bit Binary Coded Decimal Interchange Code (BCDIC) to the eight-bit extended BCD interchange code (EBCDIC) and back again. The tables show the two translations in binary.

Character assignments for the EBCDIC are given to IBM1130 specifications. All the non-alphanumeric assignments in BCDIC are subject to specialist usage, and care should be taken over them.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

connection diagram

Dual-In-Line Package

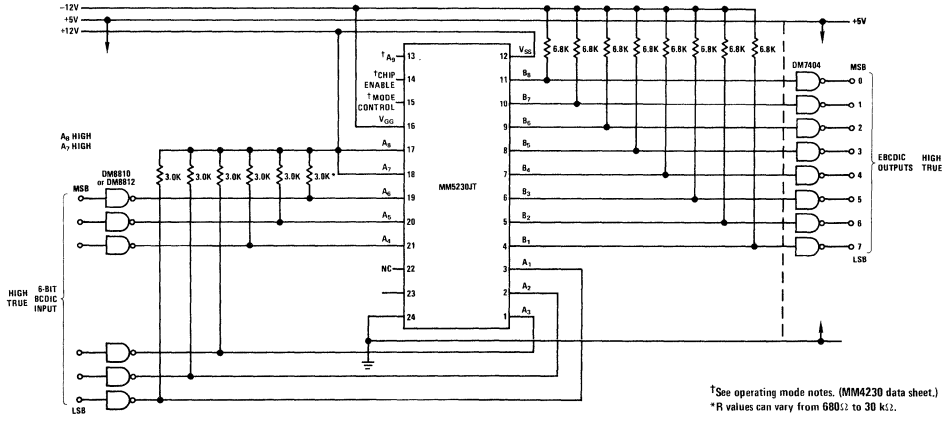


Order Number MM4230JT/J
or MM5230JT/J
See Package 11

Order Number MM5230JT/N
See Package 18

typical applications

BCDIC to EBCDIC



†See operating mode notes. (MM4230 data sheet.)
*R values can vary from 680Ω to 30 kΩ.

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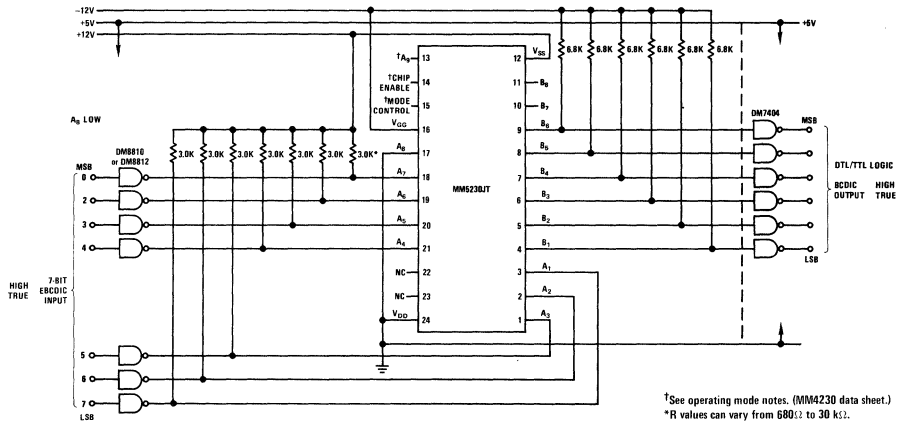
typical applications (con't)

EBCDIC to BCDIC



†See operating mode notes. (MM4230 data sheet.)
*R values can vary from 680Ω to 30 kΩ.

code conversion tables

BCDIC to EBCDIC

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	BCDIC SYMBOL	EBCDIC SYMBOL	EBCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
0	NULL	NULL	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	0	0	0	1
2	2	2	1	1	1	1	0	0	1	0
3	3	3	1	1	1	1	0	0	1	1
4	4	4	1	1	1	1	0	1	0	0
5	5	5	1	1	1	1	0	1	0	1
6	6	6	1	1	1	1	0	1	1	0
7	7	7	1	1	1	1	0	1	1	1
8	8	8	1	1	1	1	1	0	0	0
9	9	9	1	1	1	1	1	0	0	1
10	0	0	1	1	1	1	0	0	0	0
11	#	#	0	1	1	1	1	0	1	1
12	@	@	0	1	1	1	1	1	0	0
13	'	'	0	1	1	1	1	1	0	1
14	=	=	0	1	1	1	1	1	1	0
15	"	"	0	1	1	1	1	1	1	1
16	Space	Space	0	1	0	0	0	0	0	0
17	/	/	0	1	1	0	0	0	0	1
18	S	S	1	1	1	0	0	0	1	0
19	T	T	1	1	1	0	0	0	1	1
20	U	U	1	1	1	0	0	1	0	0
21	V	V	1	1	1	0	0	1	0	1
22	W	W	1	1	1	0	0	1	1	0
23	X	X	1	1	1	0	0	1	1	1
24	Y	Y	1	1	1	0	1	0	0	0
25	Z	Z	1	1	1	0	1	0	0	1
26	NULL	NULL	0	1	0	0	0	0	0	0
27	,	,	0	1	1	0	1	0	1	1
28	%	%	0	1	1	0	1	1	0	0
29	—	—	0	1	1	0	1	1	0	1
30	>	>	0	1	1	0	1	1	1	0
31	?	?	0	1	1	0	1	1	1	1
32	-	-	0	1	1	0	0	0	0	0
33	J	J	1	1	0	1	0	0	0	1
34	K	K	1	1	0	1	0	0	1	0
35	L	L	1	1	0	1	0	0	1	1
36	M	M	1	1	0	1	0	1	0	0
37	N	N	1	1	0	1	0	1	0	1
38	O	O	1	1	0	1	0	1	1	0
39	P	P	1	1	0	1	1	1	1	1
40	Q	Q	1	1	0	1	1	0	0	0
41	R	R	1	1	0	1	1	0	0	1
42	!	!	0	1	0	1	1	0	1	0
43	$	$	0	1	0	1	1	0	1	1
44	*	*	0	1	0	1	1	1	0	0
45	)	)	0	1	0	1	1	1	0	1
46	;	;	0	1	0	1	1	1	1	0
47	¬	¬	0	1	0	1	1	1	1	1
48	&	&	0	1	0	1	0	0	0	0
49	A	A	1	1	0	0	0	0	0	1
50	B	B	1	1	0	0	0	0	1	0
51	C	C	1	1	0	0	0	0	1	1
52	D	D	1	1	0	0	0	1	0	0
53	E	E	1	1	0	0	0	1	0	1
54	F	F	1	1	0	0	0	1	1	0
55	G	G	1	1	0	0	0	1	1	1
56	H	H	1	1	0	0	1	0	0	0
57	I	I	1	1	0	0	1	0	0	1
58	¢	¢	0	1	0	0	1	0	1	0
59	.	.	0	1	0	0	1	0	1	1
60	<	<	0	1	0	0	1	1	0	0
61	(	(	0	1	0	0	1	1	0	1
62	+	+	0	1	0	0	1	1	1	0
63	|	|	0	1	0	0	1	1	1	1

code conversion tables(con't)

BCDIC to EBCDIC (con't)

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	BCDIC	EBCDIC	EBCDIC							
	SYMBOL	SYMBOL	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
64	0	0	1	1	1	1	0	0	0	0
65	1	1	1	1	1	1	0	0	0	1
66	2	2	1	1	1	1	0	0	1	0
67	3	3	1	1	1	1	0	0	1	1
68	4	4	1	1	1	1	0	1	0	0
69	5	5	1	1	1	1	0	1	0	1
70	6	6	1	1	1	1	0	1	1	0
71	NULL	NULL	0	0	0	0	0	0	0	0
72	7	7	1	1	1	1	0	1	1	1
73	8	8	1	1	1	1	1	0	0	0
74	9	9	1	1	1	1	1	0	0	1
75	NULL	NULL	0	0	0	0	0	0	0	0
76	NULL	NULL	0	0	0	0	0	0	0	0
77	NULL	NULL	0	0	0	0	0	0	0	0
78	NULL	NULL	0	0	0	0	0	0	0	0
79	NULL	NULL	0	0	0	0	0	0	0	0
80	NULL	NULL	0	0	0	0	0	0	0	0
81	NULL	NULL	0	0	0	0	0	0	0	0
82	NULL	NULL	0	0	0	0	0	0	0	0
83	NULL	NULL	0	0	0	0	0	0	0	0
84	NULL	NULL	0	0	0	0	0	0	0	0
85	NULL	NULL	0	0	0	0	0	0	0	0
86	NULL	NULL	0	0	0	0	0	0	0	0
87	NULL	NULL	0	0	0	0	0	0	0	0
88	NULL	NULL	0	0	0	0	0	0	0	0
89	NULL	NULL	0	0	0	0	0	0	0	0
90	NULL	NULL	0	0	0	0	0	0	0	0
91	NULL	NULL	0	0	0	0	0	0	0	0
92	NULL	NULL	0	0	0	0	0	0	0	0
93	NULL	NULL	0	0	0	0	0	0	0	0
94	NULL	NULL	0	0	0	0	0	0	0	0
95	NULL	NULL	0	0	0	0	0	0	0	0
96	NULL	NULL	0	0	0	0	0	0	0	0
97	NULL	NULL	0	0	0	0	0	0	0	0
98	NULL	NULL	0	0	0	0	0	0	0	0
99	NULL	NULL	0	0	0	0	0	0	0	0
100	NULL	NULL	0	0	0	0	0	0	0	0
101	NULL	NULL	0	0	0	0	0	0	0	0
102	NULL	NULL	0	0	0	0	0	0	0	0
103	NULL	NULL	0	0	0	0	0	0	0	0
104	NULL	NULL	0	0	0	0	0	0	0	0
105	NULL	NULL	0	0	0	0	0	0	0	0
106	NULL	NULL	0	0	0	0	0	0	0	0
107	NULL	NULL	0	0	0	0	0	0	0	0
108	NULL	NULL	0	0	0	0	0	0	0	0
109	NULL	NULL	0	0	0	0	0	0	0	0
110	NULL	NULL	0	0	0	0	0	0	0	0
111	NULL	NULL	0	0	0	0	0	0	0	0
112	NULL	NULL	0	0	0	0	0	0	0	0
113	NULL	NULL	0	0	0	0	0	0	0	0
114	NULL	NULL	0	0	0	0	0	0	0	0
115	NULL	NULL	0	0	0	0	0	0	0	0
116	NULL	NULL	0	0	0	0	0	0	0	0
117	NULL	NULL	0	0	0	0	0	0	0	0
118	NULL	NULL	0	0	0	0	0	0	0	0
119	NULL	NULL	0	0	0	0	0	0	0	0
120	NULL	NULL	0	0	0	0	0	0	0	0
121	NULL	NULL	0	0	0	0	0	0	0	0
122	NULL	NULL	0	0	0	0	0	0	0	0
123	NULL	NULL	0	0	0	0	0	0	0	0
124	NULL	NULL	0	0	0	0	0	0	0	0
125	NULL	NULL	0	0	0	0	0	0	0	0
126	NULL	NULL	0	0	0	0	0	0	0	0
127	NULL	NULL	0	0	0	0	0	0	0	0

code conversion tables(con't)

EBCDIC to BCDIC

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	EBCDIC SYMBOL	BCDIC SYMBOL	BCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
128	NULL	NULL	0	0	0	0	0	0	0	0
129	NULL	NULL	0	0	0	0	0	0	0	0
130	NULL	NULL	0	0	0	0	0	0	0	0
131	NULL	NULL	0	0	0	0	0	0	0	0
132	NULL	NULL	0	0	0	0	0	0	0	0
133	–	–	0	0	0	1	0	0	0	0
134	–	–	0	0	0	1	0	0	0	0
135	NULL	NULL	0	0	0	0	0	0	0	0
136	NULL	NULL	0	0	0	0	0	0	0	0
137	–	–	0	0	0	1	0	0	0	0
138	¢	¢	0	0	1	1	1	0	1	0
139	.	.	0	0	1	1	1	0	1	1
140	<	<	0	0	1	1	1	1	0	0
141	(	(	0	0	1	1	1	1	0	1
142	+	+	0	0	1	1	1	1	1	0
143	|	|	0	0	1	1	1	1	1	1
144	&	&	0	0	1	1	0	0	0	0
145	NULL	NULL	0	0	0	0	0	0	0	0
146	NULL	NULL	0	0	0	0	0	0	0	0
147	NULL	NULL	0	0	0	0	0	0	0	0
148	NULL	NULL	0	0	0	0	0	0	0	0
149	–	–	0	0	0	1	0	0	0	0
150	–	–	0	0	0	1	0	0	0	0
151	NULL	NULL	0	0	0	0	0	0	0	0
152	NULL	NULL	0	0	0	0	0	0	0	0
153	!	!	0	0	0	0	0	0	0	0
154	$	$	0	0	1	0	1	0	1	0
155	*	*	0	0	1	0	1	0	1	1
156	)	)	0	0	1	0	1	1	0	0
157	;	;	0	0	1	0	1	1	0	1
158	¬	¬	0	0	1	0	1	1	1	0
159	–	–	0	0	1	0	1	1	1	1
160	/	/	0	0	1	0	0	0	0	0
161	⌟	⌟	0	0	0	1	0	0	0	1
162	NULL	NULL	0	0	0	0	0	0	0	0
163	NULL	NULL	0	0	0	0	0	0	0	0
164	NULL	NULL	0	0	0	0	0	0	0	0
165	NULL	NULL	0	0	0	0	0	0	0	0
166	NULL	NULL	0	0	0	0	0	0	0	0
167	NULL	NULL	0	0	0	0	0	0	0	0
168	NULL	NULL	0	0	0	0	0	0	0	0
169	NULL	NULL	0	0	0	0	0	0	0	0
170	NULL	NULL	0	0	0	0	0	0	0	0
171	,	,	0	0	0	1	1	0	1	1
172	%	%	0	0	0	1	1	1	0	0
173	–	–	0	0	0	1	1	1	0	1
174	>	>	0	0	0	1	1	1	1	0
175	?	?	0	0	0	1	1	1	1	1
176	NULL	NULL	0	0	0	0	0	0	0	0
177	NULL	NULL	0	0	0	0	0	0	0	0
178	NULL	NULL	0	0	0	0	0	0	0	0
179	NULL	NULL	0	0	0	0	0	0	0	0
180	NULL	NULL	0	0	0	0	0	0	0	0
181	–	–	0	0	0	1	0	0	0	0
182	–	–	0	0	0	1	0	0	0	0
183	NULL	NULL	0	0	0	0	0	0	0	0
184	NULL	NULL	0	0	0	0	0	0	0	0
185	NULL	NULL	0	0	0	0	0	0	0	0
186	:	:	0	0	0	0	0	0	0	0
187	#	#	0	0	0	0	1	0	1	1
188	@	@	0	0	0	0	1	1	0	0
189	'	'	0	0	0	0	1	1	0	1
190	=	=	0	0	0	0	1	1	1	0
191	"	"	0	0	0	0	1	1	1	1

code conversion tables(con't)

EBCDIC to BCDIC (con't)

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	EBCDIC SYMBOL	BCDIC SYMBOL	BCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
192	-	-	0	0	0	1	0	0	0	0
193	A	A	0	0	1	1	0	0	0	1
194	B	B	0	0	1	1	0	0	1	0
195	C	C	0	0	1	1	0	0	1	1
196	D	D	0	0	1	1	0	1	0	0
197	E	E	0	0	1	1	0	1	0	1
198	F	F	0	0	1	1	0	1	1	0
199	G	G	0	0	1	1	0	1	1	1
200	H	H	0	0	1	1	1	0	0	0
201	I	I	0	0	1	1	1	0	0	1
202	NULL	NULL	0	0	0	0	0	0	0	0
203	NULL	NULL	0	0	0	0	0	0	0	0
204	NULL	NULL	0	0	0	0	0	0	0	0
205	NULL	NULL	0	0	0	0	0	0	0	0
206	NULL	NULL	0	0	0	0	0	0	0	0
207	NULL	NULL	0	0	0	0	0	0	0	0
208	NULL	NULL	0	0	0	0	0	0	0	0
209	J	J	0	0	1	0	0	0	0	1
210	K	K	0	0	1	0	0	0	1	0
211	L	L	0	0	1	0	0	0	1	1
212	M	M	0	0	1	0	0	1	0	0
213	N	N	0	0	1	0	0	1	0	1
214	O	O	0	0	1	0	0	1	1	0
215	P	P	0	0	1	0	0	1	1	1
216	Q	Q	0	0	1	0	1	0	0	0
217	R	R	0	0	1	0	1	0	0	1
218	NULL	NULL	0	0	0	0	0	0	0	0
219	NULL	NULL	0	0	0	0	0	0	0	0
220	NULL	NULL	0	0	0	0	0	0	0	0
221	NULL	NULL	0	0	0	0	0	0	0	0
222	NULL	NULL	0	0	0	0	0	0	0	0
223	NULL	NULL	0	0	0	0	0	0	0	0
224	NULL	NULL	0	0	0	0	0	0	0	0
225	NULL	NULL	0	0	0	0	0	0	0	0
226	S	S	0	0	0	1	0	0	1	0
227	T	T	0	0	0	1	0	0	1	1
228	U	U	0	0	0	1	0	1	0	0
229	V	V	0	0	0	1	0	1	0	1
230	W	W	0	0	0	1	0	1	1	0
231	X	X	0	0	0	1	0	1	1	1
232	Y	Y	0	0	0	1	1	0	0	0
233	Z	Z	0	0	0	1	1	0	0	1
234	NULL	NULL	0	0	0	0	0	0	0	0
235	NULL	NULL	0	0	0	0	0	0	0	0
236	NULL	NULL	0	0	0	0	0	0	0	0
237	NULL	NULL	0	0	0	0	0	0	0	0
238	NULL	NULL	0	0	0	0	0	0	0	0
239	NULL	NULL	0	0	0	0	0	0	0	0
240	0	0	0	0	0	0	1	0	1	0
241	1	1	0	0	0	0	0	0	0	1
242	2	2	0	0	0	0	0	0	1	0
243	3	3	0	0	0	0	0	0	1	1
244	4	4	0	0	0	0	0	1	0	0
245	5	5	0	0	0	0	0	1	0	1
246	6	6	0	0	0	0	0	1	1	0
247	7	7	0	0	0	0	0	1	1	1
248	8	8	0	0	0	0	1	0	0	0
249	9	9	0	0	0	0	1	0	0	1
250	NULL	NULL	0	0	0	0	0	0	0	0
251	NULL	NULL	0	0	0	0	0	0	0	0
252	NULL	NULL	0	0	0	0	0	0	0	0
253	NULL	NULL	0	0	0	0	0	0	0	0
254	NULL	NULL	0	0	0	0	0	0	0	0
255	NULL	NULL	0	0	0	0	0	0	0	0

ROM Code Converters

MM4230KP/MM5230KP ASCII-7 to selectric code converter

general description

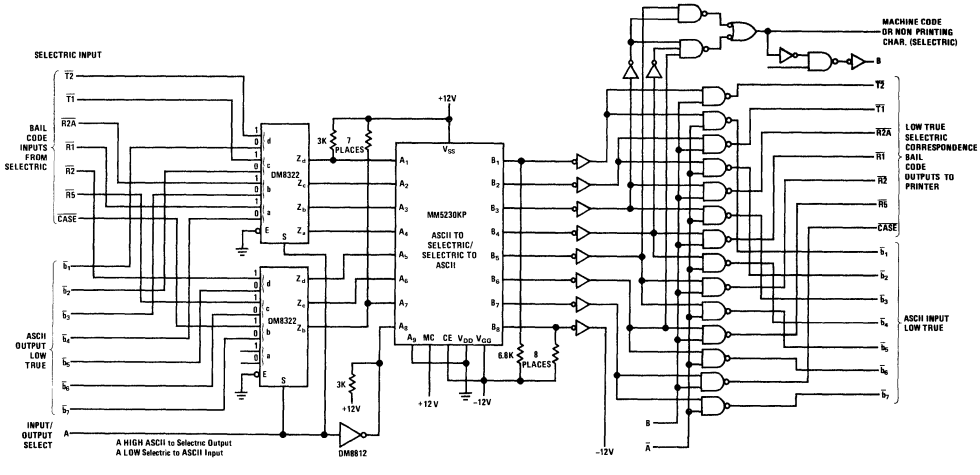
The MM4230KP/MM5230KP MOS read-only memory has been programmed to perform the conversion between the American Standard Code for Information Interchange in seven bits (ASCII) and the Selectric correspondence bail code transmitted and received by the IBM Series 7 input/output printers.

application hints

The ASCII field and Selectric bail code field as defined do not map exactly: for instance "space" is handled as a normal 7-bit code in ASCII, but is handled as a unique switch and solenoid pair in the Selectric printer. And even among the graphic characters, ± and ¢ exist only for Selectric, and > and < only for ASCII. The former problem is handled in the MM4230KP/MM5230KP by exploiting the inherent redundancy of the bail code (see Table 2). The latter inconsistency is resolved by making arbitrary equivalences between the unique characters. The two tables show the treatment of both the characters which have equivalents in both codes, and those characters, and the functions, which do not. Encoding and decoding the Selectric functions that the user requires is a matter of conventional Boolean logic. A typical example is shown below.

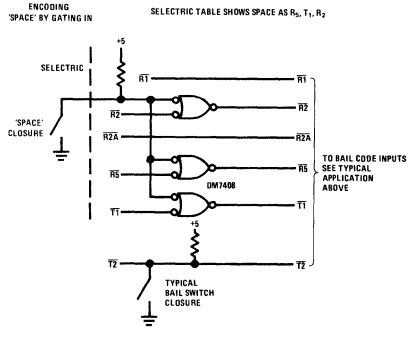
For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

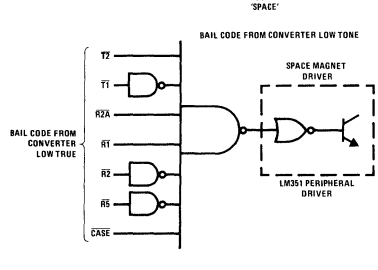
typical applications



Encoding 'Space' by Gating In on Input

Decoding 'Space' on Output





Order Number MM4230KP-2/J or MM5230KP-2/J
See Package 11

Order Number MM5230KP-2/N
See Package 18

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code conversion tables

Table 1. ASCII-7 to Selectric

Bits b_7 b_6 b_5 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4	b_3	b_2	b_1	Row ↓ / Column →	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL 02	DLE 0A	SP 62	0	@	P	` 25	p
0	0	0	1	1	SOH 12	DCI IA	!	1	A	Q	a	q
0	0	1	0	2	STX 22	DC2 2A	"	2	B	R	b	r
0	0	1	1	3	ETX 32	DC3 3A	#	3	C	S	c	s
0	1	0	0	4	EOT 03	DC4 0B	$	4	D	T	d	t
0	1	0	1	5	ENQ 13	NAK 1B	%	5	E	U	e	u
0	1	1	0	6	ACK 23	SYN 2B	&	6	F	V	f	v
0	1	1	1	7	BEL 33	ETB 3B	' 25	7	G	W	g	w
1	0	0	0	8	BS 42	CAN 4A	(	8	H	X	h	x
1	0	0	1	9	HT 52	EM 5A	)	9	I	Y	i	y
1	0	1	0	A	LF 53	SUB 6A	*	:	J	Z	j	z
1	0	1	1	B	VT 72	ESC 7A	+	;	K	[7F	k	} 7F
1	1	0	0	C	FF 72	FS 4B	,	< 40	L	\ 60	l	¦ 48
1	1	0	1	D	CR 53	GS 5B	–	=	M	] 77	m	} 77
1	1	1	0	E	SO 63	RS 6B	.	> 50	N	^ 70	n	~ 58
1	1	1	1	F	SI 73	US 7B	/	?	O	_	o	DEL 00

code conversion tables (con't)

Table 2. Selectric to ASCII-7

R_5 → / T_1 → / T_2 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
S ↓	R_{2A} ↓	R_2 ↓	R_1 ↓	Row ↓ / Column →	0	1	2	3	4	5	6	7
0	0	0	0	0	¯ 2/D	b	w	9	< 3/C	> 3/E	\ 5/C	^ 5/E
0	0	0	1	1	y	h	s	0 3/0	/	| 6/C	° 6/F	4
0	0	1	0	2	NUL 0/0	SOH 0/1	STX 0/2	ETX 0/3	BS 0/8	TAB 0/9	SP 2/0	IND 0/A
0	0	1	1	3	EOT C/4	ENQ 0/5	ACK 0/6	BELL 0/7		CR 0/D	SO 0/E	SI 0/F
0	1	0	0	4	Q	k	i	6	' 2/C	c	a	8
0	1	0	1	5	P	e	' 2/7	5	; 3/B	d	r	7
0	1	1	0	6	= 3/D	n	. 2/E	2	f	u	v	3
0	1	1	1	7	J	t	½! 2/1	z	g	x	m	1
1	0	0	0	8	_	B	W	(	! 7/C	~ 7/E		
1	0	0	1	9	Y	H	S	)	?	L	° 4/F	$
1	0	1	0	A	DLE 1/0	DC1 1/1	DC2 1/2	DC3 1/3	CAN 1/8	EM 1/9	SUB 1/A	ESC 1/B
1	0	1	1	B	DC4 1/4	NAK 1/5	SYN 1/6	ETB 1/7	FS 1/C	GS 1/0	RS 1/E	US 1/F
1	1	0	0	C	Q	K	| 4/9	¢ 6/3	, 2/C	C	A	*
1	1	0	1	D	P	E	"	%	:	D	R	&
1	1	1	0	E	+	N	. 2/E	@	F	U	V	#
1	1	1	1	F	J	T	¼° F/F	Z	G	X	M	±[5/B

Entries Thus are Redundant Bail Codes

ASCII shown thus: Column No./Row No.

8

ROM Code Converters

MM4230QW/MM5230QW hollerith to EBCDIC code converter

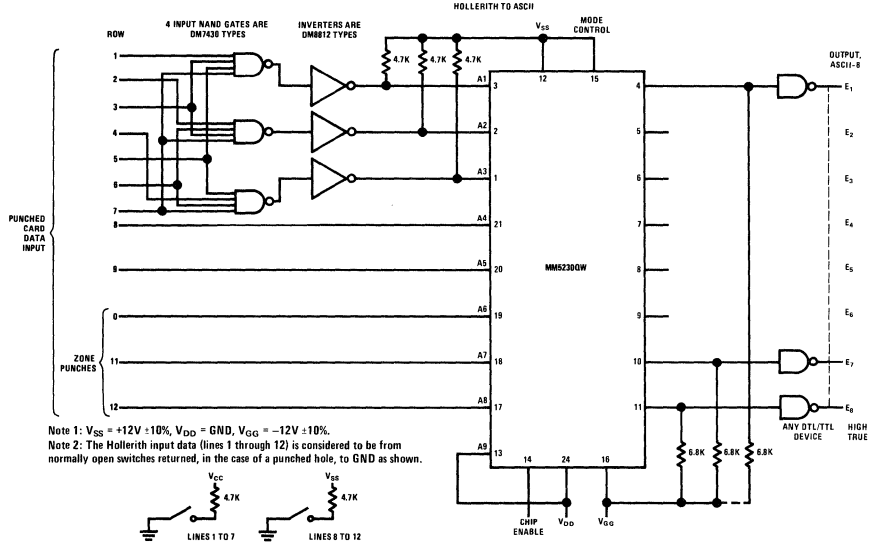
general description

The MM4230QW/MM5230QW 2048-bit MOS read only memory has been programmed to convert the 12 line Hollerith Code to the 8 line EBCDIC Code. Three TTL 4-input NAND gates and three TTL inverters are used to compress the 12 Hollerith lines to eight line binary encoded form suitable for use by the ROM.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

typical application

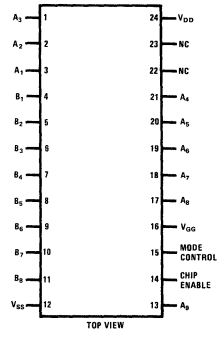
Hollerith to EBCDIC



Note 1: V_{SS} = +12V ±10%, V_{DD} = GND, V_{GG} = −12V ±10%.
Note 2: The Hollerith input data (lines 1 through 12) is considered to be from normally open switches returned, in the case of a punched hole, to GND as shown.

connection diagram

Dual-In-Line Package



Order Number MM4230QW/J or MM5230QW/J
See Package 11
Order Number MM5230QW/N
See Package 18

code conversion table

Hollerith to EBCDIC

	12	11	0		12 0	12 11	11 0	12 11 0	12	11	0		12 0	12 11	11 0	12 11 0	
	&	-	ϕ	SP	{	¦	¦	70	49	59	69	`	80	90	A0	B0	8-1
1	A	J	/	1	a	j	~	B1	SOH	DC1	21	31	41	51	E1	71	9 -1
2	B	K	S	2	b	k	s	B2	STX	DC2	22	SYN	42	52	62	72	9 -2
3	C	L	T	3	c	l	t	B3	ETX	DC3	23	33	43	53	63	73	9 -3
4	D	M	U	4	d	m	u	B4	04	14	24	34	44	54	64	74	9 -4
5	E	N	V	5	e	n	v	B5	HT	15	LF	35	45	55	65	75	9 -5
6	F	O	W	6	f	o	w	B6	06	BS	ETB	36	46	56	66	76	9 -6
7	G	P	X	7	g	p	x	B7	DEL	17	ESC	EOT	47	57	67	77	9 -7
8	H	Q	Y	8	h	q	y	B8	08	CAN	28	38	48	58	68	78	9 -8
9	I	R	Z	9	i	r	z	B9	09	EM	29	39	NUL	DLE	20	30	9-8-1
8-2	[	]	\	:	8A	9A	AA	BA	0A	1A	2A	3A	CA	DA	EA	FA	9-8-2
8-3	.	$	,	#	8B	9B	AB	BB	VT	1B	2B	3B	CB	DB	EB	FB	9-8-3
8-4	<	*	%	@	8C	9C	AC	BC	FF	FS	2C	DC4	CC	DC	EC	FC	9-8-4
8-5	(	)	–	'	8D	9D	AD	BD	CR	GS	ENQ	NAK	CD	DD	ED	FD	9-8-5
8-6	+	;	>	=	8E	9E	AE	BE	SO	RS	ACK	3E	CE	DE	EE	FE	9-8-6
8-7	! ①	^ ②	?	"	8F	9F	AF	BF	SI	US	BEL	SUB	CF	DF	EF	FF	9-8-7

① may be "|"
② may be "¬"

Note: Unassigned entries e.g. AF refer to the EBCDIC code as a 16 x 16 table, column then row, in hexidecimal notation.

Note: The relationship between Hollerith as 256 valid punch combinations and EBCDIC as eight binary digits is well established. This converter conforms to this practice. The assignments shown in the table above are the recommendations of the American National Standards Institute. For details on alternate non-alphanumeric graphic and control codes, see ANSI x 3.26 – 1970.

ROM Code Converters

MM4230QX/MM5230QX

EBCDIC-8-to-ASCII-8 code converter

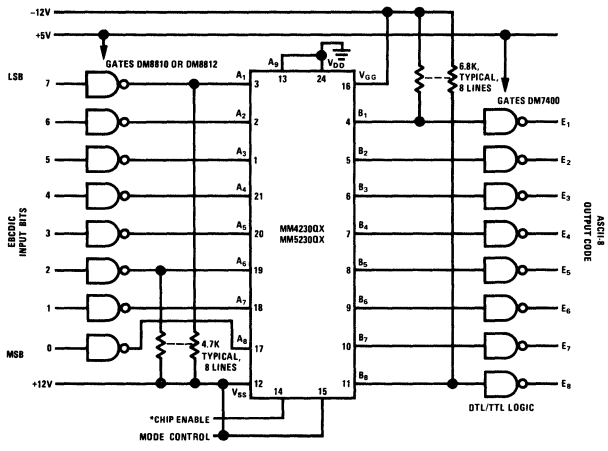
general description

The MM4230QX/MM5230QX is a 2048-bit read only memory that has been programmed to convert Extended Binary Coded Decimal Interchange Code (EBCDIC) to the American Standard Code for Information Interchange extended to eight bits (ASCII-8).

The conversion conforms to the practice established by the American National Standard ANSIx 3.26–1970. Exact details are shown in the code table.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 2048-bit read only memory data sheet.

typical application

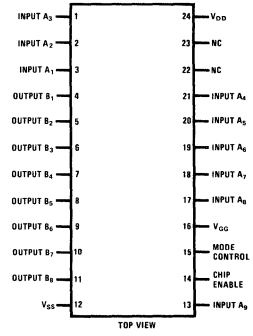


*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM, Logic "0" ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative, Logic "0," more positive.

connection diagram

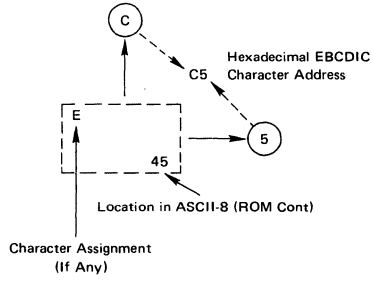
Dual-In-Line Package



Order Number MM4230QX/J or MM5230QX/J
See Package 11
Order Number MM5230QX/N
See Package 18

code conversion table

4 5 6 7	Column → / Row ↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
	0 → 0 1 → 0 2 → 0 3 → 0	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1	
0 0 0 0	0	NUL 00	DLE 10	80	90	SP 20	& 26	– 2D	BA	C3	CA	D1	D8	{ 7B	} 7D	\ 5C	0 30	0
0 0 0 1	1	SOH 01	DC1 11	81	91	A0	A9	/ 2F	BB	a 61	j 6A	~ 7E	D9	A 41	J 4A	9F	1 31	1
0 0 1 0	2	STX 02	DC2 12	82	SYN 16	A1	AA	B2	BC	b 62	k 6B	s 73	DA	B 42	K 4B	S 53	2 32	2
0 0 1 1	3	ETX 03	DC3 13	83	93	A2	AB	B3	BD	c 63	l 6C	t 74	DB	C 43	L 4C	T 54	3 33	3
0 1 0 0	4	9C	9D	84	94	A3	AC	B4	BE	d 64	m 6D	u 75	DC	D 44	M 4D	U 55	4 34	4
0 1 0 1	5	HT 09	85	LF OA	95	A4	AD	B5	BF	e 65	n 6E	v 76	DD	E 45	N 4E	V 56	5 35	5
0 1 1 0	6	86	BS 08	ETB 17	96	A5	AE	B6	C0	f 66	o 6F	w 77	DE	F 46	O 4F	W 57	6 36	6
0 1 1 1	7	DEL 7F	87	ESC 1B	EOT 04	A6	AF	B7	C1	h 67	p 70	x 78	DF	G 47	P 50	X 58	7 37	7
1 0 0 0	8	97	CAN 18	88	98	A7	B0	B8	C2	i 68	q 71	y 79	E0	H 48	Q 51	Y 59	8 38	8
1 0 0 1	9	8D	EM 19	89	99	A8	B1	B9	` 60	‘ 69	r 72	z 7A	E1	I 49	R 52	Z 5A	9 39	9
1 0 1 0	A	8E	92	8A	9A	[5B	] 5D	; 7C	3A	C4	CB	D2	E2	E8	EE	F4	FA	A
1 0 1 1	B	VT 0B	8F	8B	9B	. 2E	$ 24	, 2C	# 23	C5	CC	D3	E3	E9	EF	F5	FB	B
1 1 0 0	C	FF 0C	FS 1C	8C	DC4 14	< 3C	* 2A	% 25	@ 40	C6	CD	D4	E4	EA	F0	F6	FC	C
1 1 0 1	D	CR 0D	GS 1D	ENQ 05	NAK 15	(28	) 29	– 5F	· 27	C7	CE	D5	E5	EB	F1	F7	FD	D
1 1 1 0	E	SO 0E	RS 1E	ACK 06	9E	+ 2B	: 3B	> 3E	= 3D	C8	CF	D6	E6	EC	F2	F8	FE	E
1 1 1 1	F	SI 0F	US 1F	BEL 07	SUB 1A	! 21	^ 5E	? 3F	" 22	C9	DO	D7	E7	ED	F3	F9	EO FF	F



8

ROM Code Converters

MM4230QY/MM5230QY

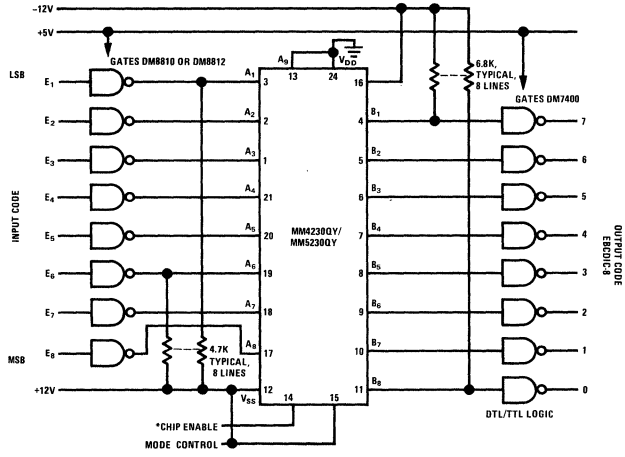
ASCII-8 -to- EBCDIC-8 code converter

general description

The MM4230QY/MM5230QY is a 2048-bit read only memory that has been programmed to convert the American Standard Code for Information Interchange extended to eight bits, (ASCII-8) to Extended Binary Coded Decimal Interchange Code (EBCDIC-8). The conversion conforms to the practice established by the American National Standard ANSIx3.26 1970. Exact details are shown in the code table.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 2048-bit read only memory data sheet.

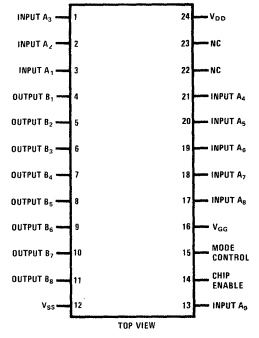
typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4230QY/J
or MM5230QY/J
See Package 11

Order Number MM5230QY/N
See Package 18

code conversion table

b_4 b_3 b_2 b_1	Row ↓ / Column →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Row ↓ / Column ←
	b_8 →	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
	b_7 →	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	
	b_6 →	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	
	b_5 →	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
0 0 0 0	0	NUL 00	DLE 10	SP 40	0 0 F0	@ 7C	P D7	\ 79	p 97	20	30	41	58	76	9F	B8	DC	0
0 0 0 1	1	SOH 01	DC1 11	! ① 4F	1 F1	A C1	Q D8	a 81	q 98	21	31	42	59	77	AO	B9	DD	1
0 0 1 0	2	STX 02	DC2 12	" 7F	2 F2	B C2	R D9	b 82	r 99	22	1A	43	62	78	AA	BA	DE	2
0 0 1 1	3	ETX 03	DC3 13	# 7B	3 F3	C C3	S E2	c 83	s A2	23	33	44	63	80	AB	BB	DF	3
0 1 0 0	4	ECT 37	DC4 3C	$ 5B	4 F4	D C4	T E3	d 84	t A3	24	34	45	64	8A	AC	BC	EA	4
0 1 0 1	5	ENQ 2D	NAK 3D	% 6C	5 F5	E C5	U E4	e 85	u A4	15	35	46	65	8B	AD	BD	EB	5
0 1 1 0	6	ACK 2E	SYN 32	& 50	6 F6	F C6	V E5	f 86	v A5	06	36	47	66	8C	AE	BE	EC	6
0 1 1 1	7	BEL 2F	ETB 26	' 7D	7 F7	G C7	W E6	g 87	w A6	17	08	48	67	8D	AF	BF	ED	7
1 0 0 0	8	BS 16	CAN 18	(4D	8 F8	H C8	X E7	h 88	x A7	28	38	49	68	8E	B0	CA	EE	8
1 0 0 1	9	HT 05	EM 19	) 5D	9 F9	I C9	Y E8	i 89	y A8	29	39	51	69	8F	B1	CB	EF	9
1 0 1 0	A	IF 25	SUB 3F	* 5C	7A	J D1	Z E9	j 91	z A9	2A	3A	52	70	90	B2	CC	FA	10
1 0 1 1	B	VT OB	ESC 27	+ 4E	. 5E	K D2	[4A	k 92	{ CO	2B	3B	53	71	9A	B3	CD	FB	11
1 1 0 0	C	FF OC	FS 1C	, 6B	< 4C	L D3	\ E0	l 93	| 6A	2C	04	54	72	9B	B4	CE	FC	12
1 1 0 1	D	CR OD	GS 1D	- 60	= 7E	M D4	] 5A	m 94	} D0	09	14	55	73	9C	B5	CF	FD	13
1 1 1 0	E	SO OE	RS 1E	. 4B	> 6E	N D5	^② 5F	n 95	~ A1	0A	3E	56	74	9D	B6	DA	FE	14
1 1 1 1	F	SI OF	US 1F	/ 61	? 6F	O D6	– 6D	o 96	DEL 07	1B	E1	57	75	9E	B7	DB	EO FF	15

1 may be "1"
2 may be "¬"
3 The top line in each entry to the table represents an assigned character (Columns 0 to 7). The bottom line in each entry is the corresponding EBCDIC Code, in hexadecimal notation.

The Hexadecimal EBCDIC entry is formed thus:

Eight EBCDIC bits

MSB 0 1 2 3 4 5 6 7 LSB

1st Digit 2nd Digit

Example: 0 1 0 1 1 1 0 0 or *

5 C

To convert ASCII-8 asterisk (*) to EBCDIC-8

E_8 E_1

* in ASCII is a 2A or binary 0010 1010

applying this as an address to the MM5230QY/MM4230QY

bit-0 bit-7

gives the output 0101 1100, which is an EBCDIC-8 asterisk.

8

ROM Code Converters

MM4230RS/MM5230RS binary to modulo-n divider code converter

general description

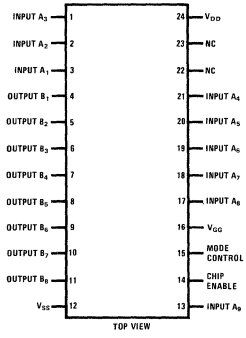
The MM4230RS/MM5230RS binary to modulo-n divider code converter is set up to generate the program input settings for a pair of DM7520/DM8520 modulo-n dividers, in order to divide by any binary number from one to 255. Detailed instructions for use of the DM7520/DM8520 are given in its data sheet.

Applying the required division ratio, in binary, to the inputs of the ROM as shown, generates two sets of four program inputs, one for each of the 2 DM7520/DM8520 dividers.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

connection diagram

Dual-In-Line Package

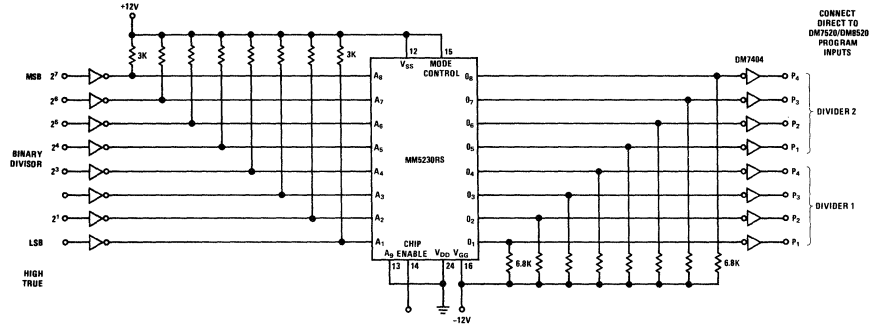


Order Number MM4230RS/J or MM5230RS/J
See Package 11

Order Number MM5230RS/N
See Package 18

typical application

Binary to Modulo-n Divider



code conversion table

SETTING								÷BY
DIVIDER 1				DIVIDER 2				
B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	
0	1	1	1	1	1	1	1	255
1	0	1	1	1	1	1	1	254
0	1	0	1	1	1	1	1	253
0	0	1	0	1	1	1	1	252
1	0	0	1	0	1	1	1	251
0	1	0	0	1	0	1	1	250
0	0	1	0	0	1	0	1	249
0	0	0	1	0	0	1	0	248
0	0	0	0	1	0	0	1	247
0	0	0	0	0	1	0	0	246
0	0	0	0	0	0	1	0	245
0	0	0	0	0	0	0	1	244
1	0	0	0	0	0	0	0	243
1	1	0	0	0	0	0	0	242
1	1	1	0	0	0	0	0	241
0	1	1	1	0	0	0	0	240
1	0	1	1	1	0	0	0	239
1	1	0	1	1	1	0	0	238
0	1	1	0	1	1	1	0	237
0	0	1	1	0	1	1	1	236
0	0	0	1	1	0	1	1	235
0	0	0	0	1	1	0	1	234
0	0	0	0	0	1	1	0	233
0	0	0	0	0	0	1	1	232
1	0	0	0	0	0	0	1	231
0	1	0	0	0	0	0	0	230
0	0	1	0	0	0	0	0	229
1	0	0	1	0	0	0	0	228
1	1	0	0	1	0	0	0	227
0	1	1	0	0	1	0	0	226
1	0	1	1	0	0	1	0	225
0	1	0	1	1	0	0	1	224
0	0	1	0	1	1	0	0	223
0	0	0	1	0	1	1	0	222
0	0	0	0	1	0	1	1	221
0	0	0	0	0	1	0	1	220
1	0	0	0	0	0	1	0	219
1	1	0	0	0	0	0	1	218
0	1	1	0	0	0	0	0	217
1	0	1	1	0	0	0	0	216
0	1	0	1	1	0	0	0	215
1	0	1	0	1	1	0	0	214
1	1	0	1	0	1	1	0	213
1	1	1	0	1	0	1	1	212
0	1	1	1	0	1	0	1	211
0	0	1	1	1	0	1	0	210
0	0	0	1	1	1	0	1	209
0	0	0	0	1	1	1	0	208
1	0	0	0	0	1	1	1	207
0	1	0	0	0	0	1	1	206
1	0	1	0	0	0	0	1	205
1	1	0	1	0	0	0	0	204
1	1	1	0	1	0	0	0	203
1	1	1	1	0	1	0	0	202
0	1	1	1	1	0	1	0	201
0	0	1	1	1	1	0	1	200
1	0	0	1	1	1	1	0	199
0	1	0	0	1	1	1	1	198
0	0	1	0	0	1	1	1	197
0	0	0	1	0	0	1	1	196
1	0	0	0	1	0	0	1	195
1	1	0	0	0	1	0	0	194
1	1	1	0	0	0	1	0	193
0	1	1	1	0	0	0	1	192
0	0	1	1	1	0	0	0	191
0	0	0	1	1	1	0	0	190
1	0	0	0	1	1	1	0	189
0	1	0	0	0	1	1	1	188
1	0	1	0	0	0	1	1	187
1	1	0	1	0	0	0	1	186
0	1	1	0	1	0	0	0	185
0	0	1	1	0	1	0	0	184
1	0	0	1	1	0	1	0	183
0	1	0	0	1	1	0	1	182
0	0	1	0	0	1	1	0	181
1	0	0	1	0	0	1	1	180
0	1	0	0	1	0	0	1	179
0	0	1	0	0	1	0	0	178
1	0	0	1	0	0	1	0	177
1	1	0	0	1	0	0	1	176
1	1	1	0	0	1	0	0	175
0	1	1	1	0	0	1	0	174
1	0	1	1	1	0	0	1	173
0	1	0	1	1	1	0	0	172
1	0	1	0	1	1	1	0	171
1	1	0	1	0	1	1	1	170
0	1	1	0	1	0	1	1	169
1	0	1	1	0	1	0	1	168
1	1	0	1	1	0	1	0	167
0	1	1	0	1	1	0	1	166

SETTING								÷BY
DIVIDER 1				DIVIDER 2				
B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	
1	0	1	1	0	1	1	0	165
0	1	0	1	1	0	1	1	164
0	0	1	0	1	1	0	1	163
1	0	0	1	0	1	1	0	162
1	1	0	0	1	0	1	1	161
1	1	1	0	0	1	0	1	160
1	1	1	1	0	0	1	0	159
0	1	1	1	1	0	0	1	158
1	0	1	1	1	1	0	0	157
1	1	0	1	1	1	1	0	156
0	1	1	0	1	1	1	1	155
1	0	1	1	1	0	1	1	154
1	1	0	1	1	1	0	1	153
1	1	1	0	1	1	1	0	152
0	1	1	1	0	1	1	0	151
1	0	1	1	1	0	1	1	150
0	1	0	1	1	1	0	1	149
0	0	1	0	1	1	1	0	148
0	0	0	1	0	1	1	1	147
0	0	0	0	1	0	1	1	146
1	1	0	0	0	1	0	1	145
1	1	0	0	0	0	1	0	144
1	1	1	0	0	0	0	1	143
1	1	1	1	0	0	0	0	142
0	1	1	1	1	0	0	0	141
0	0	1	1	1	1	0	0	140
0	0	0	1	1	1	1	0	139
1	0	0	0	1	1	1	1	138
1	1	0	0	0	1	1	1	137
0	1	1	0	0	0	1	1	136
0	0	1	1	1	0	0	1	135
0	0	0	1	1	1	0	0	134
1	0	0	0	1	1	1	0	133
0	1	0	0	0	1	1	1	132
0	0	1	0	0	0	1	1	131
0	0	0	1	0	0	0	1	130
1	0	0	0	1	0	0	0	129
0	1	0	0	0	1	0	0	128
0	0	1	0	0	0	1	0	127
1	0	0	1	0	0	0	1	126
0	1	0	0	1	0	0	0	125
1	0	1	0	0	1	0	0	124
0	1	0	1	0	0	1	0	123
1	0	1	0	0	0	0	1	122
1	0	0	1	0	0	0	0	121
1	1	0	0	1	0	1	0	120
0	1	1	0	0	1	0	1	119
0	0	1	1	0	0	1	0	118
1	0	0	1	1	0	0	1	117
1	1	0	0	1	1	0	0	116
0	1	1	0	0	1	1	0	115
1	0	1	1	0	0	1	1	114
1	1	0	1	1	0	0	1	113
1	1	1	0	1	1	0	0	112
1	1	1	1	0	1	1	0	111
0	1	1	1	1	0	1	1	110
1	0	1	1	1	1	0	1	109
0	1	0	1	1	1	1	0	108
1	0	1	0	1	1	1	1	107
0	1	0	1	0	1	1	1	106
0	0	1	1	1	0	1	1	105
1	0	0	1	0	1	0	1	104
1	0	1	0	1	0	1	0	103
1	1	0	1	0	1	0	1	102
0	1	1	0	1	0	1	0	101
0	0	1	1	0	1	0	1	100
0	0	0	1	1	0	1	0	99
1	0	0	0	1	1	0	1	98
1	1	0	0	0	1	1	0	97
1	1	1	0	0	0	1	1	96
1	1	1	1	0	0	0	1	95
1	1	1	1	1	0	0	0	94
1	1	1	1	1	1	0	0	93
1	1	1	1	1	1	1	0	92

SETTING								÷BY
DIVIDER 1				DIVIDER 2				
B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	
1	1	1	0	0	1	1	1	75
1	1	1	1	0	0	1	1	74
1	1	1	1	1	0	0	1	73
0	1	1	1	1	1	1	0	72
0	0	1	1	1	1	1	0	71
0	0	0	1	1	1	1	1	70
0	0	0	0	1	1	1	1	69
0	0	0	0	0	1	1	1	68
1	0	0	0	0	0	1	1	67
0	1	0	0	0	0	0	1	66
1	0	1	0	0	0	0	0	65
0	1	0	1	0	0	0	0	64
0	0	1	0	1	0	0	0	63
0	0	0	1	0	1	0	0	62
0	0	0	0	1	0	1	0	61
1	0	0	0	0	1	0	1	60
0	1	0	0	0	0	1	0	59
0	0	1	0	0	0	0	1	58
0	0	0	1	0	0	0	0	57
0	0	0	0	1	0	0	0	56
1	0	0	0	0	1	0	0	55
1	1	0	0	0	0	1	0	54
1	1	1	0	0	0	0	1	53
1	1	1	1	0	0	0	0	52
0	1	1	1	1	0	0	0	51
0	0	1	1	1	1	0	0	50
0	0	0	1	1	1	1	0	49
1	0	0	0	1	1	1	1	48
1	1	0	0	0	1	1	1	47
0	1	1	0	0	0	1	1	46
0	0	1	1	0	0	0	1	45
0	0	0	1	1	0	0	0	44
1	0	0	0	1	1	0	0	43
0	1	0	0	0	1	1	0	42
0	0	1	0	0	0	1	1	41
0	0	0	1	0	0	0	1	40
1	0	0	0	1	0	0	0	39
0	1	0	0	0	1	0	0	38
0	0	1	0	0	0	1	0	37
1	0	0	1	0	0	0	1	36
0	1	0	0	1	0	0	0	35
1	0	1	0	0	1	0	0	34
0	1	0	1	0	0	1	0	33
0	0	1	0	1	0	0	1	32
1	0	0	1	0	1	0	0	31
1	1	0	0	1	0	1	0	30
0	1	1	0	0	1	0	1	29
0	0	1	1	0	0	1	0	28
1	0	0	1	1	0	0	1	27
1	1	0	0	1	1	0	0	26
0	1	1	0	0	1	1	0	25
1	0	1	1	0	0	1	1	24
1	1	0	1	1	0	0	1	23
1	1	1	0	1	1	0	0	22
1	1	1	1	0	1	1	0	21
0	1	1	1	1	0	1	1	20
1	0	1	1	1	1	0	1	19
0	1	0	1	1	1	1	0	18
1	0	1	0	1	1	1	1	17
0	1	0	1	0	1	1	1	16
1	0	1	0	1	0	1	1	15
1	0	1	1	0	1	0	1	14
1	0	1	0	1	0	1	0	13
1	1	0	1	0	1	0	1	12
0	1	1	0	1	1	0	0	11
0	0	1	1	0	1	0	1	10
0	0	0	1	1	0	0	1	9
1	0	0	0	1	1	0	1	8
1	1	0	0	0	1	1	0	7
1	1	1	0	0	0	1	1	6
1	1	1	1	0	0	0	1	5
1	1	1	1	1	0	0	0	4
1	1	1	1	1	1	0	0	3
1	1	1	1	1	1	1	0	2

8

ROM Code Converters

MM4231RP/MM5231RP EBCDIC to ASCII-7 code converter

general description

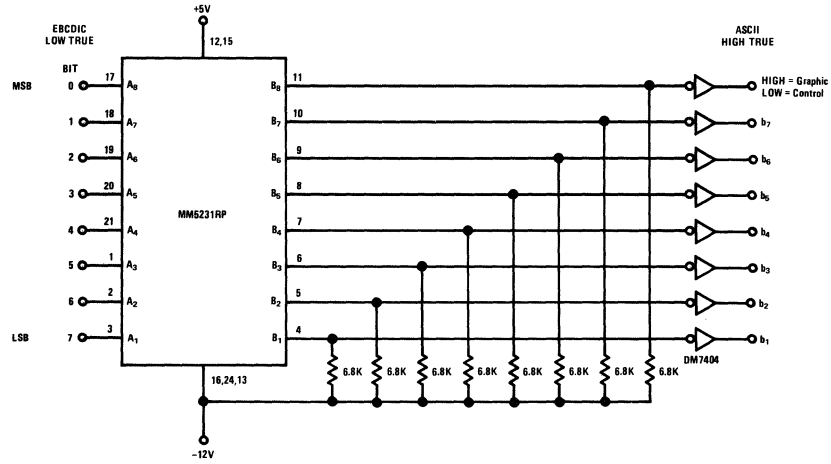
The MM4231RP/MM5231RP is a 2048-bit read-only memory that has been programmed to convert from EBCDIC, an extended binary coded decimal interchange code used in the IBM1130 computer, to ASCII-7, the American Standard Code for Information Interchange in seven bits.

This conversion differs from the ANSI x 3.26 conversion of the MM4230QX/MM5230QX in that it follows certain earlier IBM1130 character assignments. Also certain EBCDIC control codes are arbitrarily preserved and translated (see translation chart on truth table).

For electrical, environmental and mechanical details, refer to the MM4231/MM5231 data sheet.

typical application

EBCDIC TO ASCII-7



Order Number MM4231RP-2/J or MM5231RP-2/J
See Package 11

Order Number MM5231RP-2/N
See Package 18

code conversion tables

ROM ADDRESS	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT								OUTPUT							
	EBCDIC SYMBOL	ASCII SYMBOL	MSB							LSB	CC/G	MSB						LSB
0	NULL	NUL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	SOH	SOH	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
2	STX	STX	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
3	ETX	ETX	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
4	PF		0	0	0	0	0	1	0	0								
5	HT	HT									0	0	0	0	1	0	0	1
6	LC																	
7	DEL	DEL									0	1	1	1	1	1	1	1
8																		
9																		
10	SMM																	
11	VT	VT									0	0	0	0	1	0	1	1
12	FF	FF									0	0	0	0	1	1	0	0
13	CR	CR									0	0	0	0	1	1	0	1
14	S0	S0									0	0	0	0	1	1	1	0
15	S1	S1									0	0	0	0	1	1	1	1
16	DLE	DLE									0	0	0	1	0	0	0	0
17	DC1	DC1									0	0	0	1	0	0	0	1
18	DC2	DC2									0	0	0	1	0	0	1	0
19	DC3	DC3									0	0	0	1	0	0	1	1
20	RES	'									1	1	1	0	0	0	0	0
21	NL	\									1	1	0	1	1	1	0	0
22	BS	BS									0	0	0	0	1	0	0	0
23	IDL																	
24	CAN	CAN									0	0	0	1	1	0	0	0
25	EM	EM									0	0	0	1	1	0	0	1
26	CC																	
27	CUI																	
28	FLS	FS									0	0	0	1	1	1	0	0
29	GS	GS									0	0	0	1	1	1	0	1
30	RDS	RS									0	0	0	1	1	1	1	0
31	US	US									0	0	0	1	1	1	1	1
32	DS																	
33	SOS																	
34	FS																	
35																		
36	BYP										0	0	0	0	0	0	0	0
37	LF	LF									0	0	0	0	1	0	1	0
38	EOB	ETB									0	0	0	1	0	1	1	1
39	PRE	ESC									0	0	0	1	1	0	1	1
40																		
41																		
42	SM																	
43	CU2																	
44																		
45	ENQ	ENQ									0	0	0	0	0	1	0	1
46	ACK	ACK									0	0	0	0	0	1	1	0
47	BEL	BEL									0	0	0	0	0	1	1	1
48																		
49																		
50	SYN	SYN									0	0	0	1	0	1	1	0
51																		
52	PN																	
53	RS	DC4									0	0	0	1	0	1	0	0
54	UC																	
55	EOT	EOT									0	0	0	0	0	1	0	0
56																		
57																		
58																		
59	CU3																	
60	DCA																	
61	NAK	NAK									0	0	0	1	0	1	0	1
62																		
63	SUB	SUB									0	0	0	1	1	0	1	0
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

CONTINUING BINARY SEQUENCE

8

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB ... LSB	CC/G	OUTPUT MSB						LSB
64	SP	SP		1	0	1	0	0	0	0	0
65											
66											
67											
68											
69											
70											
71											
72											
73											
74	¢	~		1	1	1	1	1	1	1	0
75	.	.		1	0	1	0	1	1	1	0
76	<	<		1	0	1	1	1	1	0	0
77	(	(		1	0	1	0	1	0	0	0
78	+	+		1	0	1	0	1	0	1	1
79	¦	¦		1	1	1	1	1	1	0	0
80	&	&		1	0	1	0	0	1	1	0
81											
82											
83											
84											
85											
86											
87											
88											
89											
90	!	!		1	0	1	0	0	0	0	1
91	$	$		1	0	1	0	0	1	0	0
92	*	*		1	0	1	0	1	0	1	0
93	)	)		1	0	1	0	1	0	0	1
94	;	;	CONTINUING BINARY SEQUENCE	1	0	1	1	1	0	1	1
95	¬	^		1	1	0	1	1	1	1	0
96	–	–		1	0	1	0	1	1	0	1
97	/	/		1	0	1	0	1	1	1	1
98											
99											
100											
101											
102											
103											
104											
105											
106											
107	,	,		1	0	1	0	1	1	0	0
108	%	%		1	0	1	0	0	1	0	1
109	—	—		1	1	0	1	1	1	1	1
110	>	>		1	0	1	1	1	1	1	0
111	?	?		1	0	1	1	1	1	1	1
112											
113											
114											
115											
116											
117											
118											
119											
120											
121											
122	:	:		1	0	1	1	1	0	1	0
123	#	#		1	0	1	0	0	0	1	1
124	@	@		1	1	0	0	0	0	0	0
125	'	'		1	0	1	0	0	1	1	1
126	=	=		1	0	1	1	1	1	0	1
127	"	"		1	0	1	0	0	0	1	0
			A_8 | A_7 | A_6 | A_5 | A_4 | A_3 | A_2 | A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB							LSB	CC/G	OUTPUT MSB						LSB
128																		
129	a	a									1	1	1	0	0	0	0	1
130	b	b									1	1	1	0	0	0	1	0
131	c	c									1	1	1	0	0	0	1	1
132	d	d									1	1	1	0	0	1	0	0
133	e	e									1	1	1	0	0	1	0	1
134	f	f									1	1	1	0	0	1	1	0
135	g	g									1	1	1	0	0	1	1	1
136	h	h									1	1	1	0	1	0	0	0
137	i	i									1	1	1	0	1	0	0	1
138																		
139	{	{									1	1	1	1	1	0	1	1
140																		
141																		
142																		
143																		
144																		
145	j	j									1	1	1	0	1	0	1	0
146	k	k									1	1	1	0	1	0	1	1
147	l	l									1	1	1	0	1	1	0	0
148	m	m									1	1	1	0	1	1	0	1
149	n	n									1	1	1	0	1	1	1	0
150	o	o									1	1	1	0	1	1	1	1
151	p	p									1	1	1	1	0	0	0	0
152	q	q									1	1	1	1	0	0	0	1
153	r	r									1	1	1	1	0	0	1	0
154																		
155	}	}									1	1	1	1	1	1	0	1
156																		
157																		
158																		
159																		
160																		
161																		
162	s	s									1	1	1	1	0	0	1	1
163	t	t									1	1	1	1	0	1	0	0
164	u	u									1	1	1	1	0	1	0	1
165	v	v									1	1	1	1	0	1	1	0
166	w	w									1	1	1	1	0	1	1	1
167	x	x									1	1	1	1	1	0	0	0
168	y	y									1	1	1	1	1	0	0	1
169	z	z									1	1	1	1	1	0	1	0
170																		
171																		
172																		
173	[	[									1	1	0	1	1	0	1	1
174																		
175																		
176																		
177																		
178																		
179																		
180																		
181																		
182																		
183																		
184																		
185																		
186																		
187																		
188																		
189	]	]									1	1	0	1	1	1	0	1
190																		
191																		
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

CONTINUING BINARY SEQUENCE

8

code conversion tables(con't)

	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT								OUTPUT							
ROM ADDRESS	EBCDIC SYMBOL	ASCII SYMBOL	MSB							LSB	CC/G	MSB						LSB
192	+ ZERO																	
193	A	A									1	1	0	0	0	0	0	1
194	B	B									1	1	0	0	0	0	1	0
195	C	C									1	1	0	0	0	0	1	1
196	D	D									1	1	0	0	0	1	0	0
197	E	E									1	1	0	0	0	1	0	1
198	F	F									1	1	0	0	0	1	1	0
199	G	G									1	1	0	0	0	1	1	1
200	H	H									1	1	0	0	1	0	0	0
201	I	I									1	1	0	0	1	0	0	1
202																		
203																		
204																		
205																		
206																		
207																		
208	-ZERO																	
209	J	J									1	1	0	0	1	0	1	0
210	K	K									1	1	0	0	1	0	1	1
211	L	L									1	1	0	0	1	1	0	0
212	M	M									1	1	0	0	1	1	0	1
213	N	N									1	1	0	0	1	1	1	0
214	O	O									1	1	0	0	1	1	1	1
215	P	P									1	1	0	1	0	0	0	0
216	Q	Q									1	1	0	1	0	0	0	1
217	R	R									1	1	0	1	0	0	1	0
218																		
219																		
220																		
221																		
222			CONTINUING BINARY SEQUENCE															
223																		
224																		
225																		
226	S	S									1	1	0	1	0	0	1	1
227	T	T									1	1	0	1	0	1	0	0
228	U	U									1	1	0	1	0	1	0	1
229	V	V									1	1	0	1	0	1	1	0
230	W	W									1	1	0	1	0	1	1	1
231	X	X									1	1	0	1	1	0	0	0
232	Y	Y									1	1	0	1	1	0	0	1
233	Z	Z									1	1	0	1	1	0	1	0
234																		
235																		
236																		
237																		
238																		
239																		
240	0	0									1	0	1	1	0	0	0	0
241	1	1									1	0	1	1	0	0	0	1
242	2	2									1	0	1	1	0	0	1	0
243	3	3									1	0	1	1	0	0	1	1
244	4	4									1	0	1	1	0	1	0	0
245	5	5									1	0	1	1	0	1	0	1
246	6	6									1	0	1	1	0	1	1	0
247	7	7									1	0	1	1	0	1	1	1
248	8	8									1	0	1	1	1	0	0	0
249	9	9									1	0	1	1	1	0	0	1
250																		
251			1	1	1	1	1	0	1	1								
252			1	1	1	1	1	1	0	0								
253			1	1	1	1	1	1	0	1								
254			1	1	1	1	1	1	1	0								
255			1	1	1	1	1	1	1	1								
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM Code Converters

MM4232/MM5232 AEI, AEJ, AEK sine look up table

general description

The MM4232/MM5232 AEI, AEJ and AEK are all P-channel enhancement mode MOS read-only memories, each storing 4096 bits. They are programmed to generate the sine function of any angle expressed as a binary fraction of a right-angle. They may be combined and arranged to provide a look-up table of varying resolution and accuracy, to meet almost any system requirement for generation of the sine function.

application information

Figures 1 through 4 show the four ways that these parts may be combined. The table shows the performance of all combinations.

performance specifications

FIGURE	ROM NO. USED	RESOLUTION (= INPUT WORD LENGTH)	OUTPUT WORD LENGTH	ACCURACY	ADDER PACKAGES REQUIRED
1	AEI	9 bits	8 bits	+0 −1 bit in 8	0
2	AEI + AEJ	9 bits	16 bits	± 1/2 bit in 16	0
3	AEI + AEJ + AEK	12 bits	16 bits	± 3/4 bit in 14	4
4	AEI + AEJ + 2 AEK's	15 bits	16 bits	±1 bit in 14	6

SINE LOOK-UP TABLE WITH HIGH RESOLUTION AND ACCURACY

Theoretical Background

The table is based upon the equation:

$$\sin (M + L) = \sin M \cos L + \cos M \sin L \qquad (1)$$

By splitting M and L each into two parts MM, ML, and LM, LL, and (assuming M >> L) the following equation is obtained.

$$\begin{aligned} &\sin (M + L) \approx \sin (MM + ML) \qquad (2)\\ &+ \cos (MM + 1/2 \text{ LSB of } MM) \sin LM\\ &+ \cos (MM + 1/2 \text{ LSB of } MM) \sin LL\\ &\approx \sin (MM + ML)\\ &+ \cos (MM + 1/2 \text{ LSB of } MM) (\sin LM + \sin LL) \end{aligned}$$

The following approximations have been used:

$$\cos (LM + LL) \approx 1$$
$$\sin (LM + LL) \approx \sin (LM) + \sin (LL)$$
$$\cos (MM + ML) \approx \cos (MM + 1/2 \text{ LSB of } MM)$$

By taking MM = 6 bits, ML = 3 bits, LM = 3 bits, and LL = 3 bits, 15 bits resolution is obtained. The accuracy has been computed by comparing the values of Equation 2 with the ideal value of the sine of an angle θ resolved into 2^{15} increments in the range $0 \leq \theta < \pi/2$.

This error, due to the mathematical approximation, is $\pm 3.2 \times 10^{-5}$ maximum, corresponding to ±1 bit in 15 bits. In addition to the mathematical error, an inevitable round-off error in the 16th bit is introduced. As there are 3 LSB outputs to be added (Figure 4), the maximum round-off error will be ±1-1/2 bit in 16 bits or $\pm 2.3 \times 10^{-5}$. The theoretical maximum total error will then be $\pm (3.2 + 2.3) \times 10^{-5} = \pm 5.5 \times 10^{-5}$, which is slightly less than ±1 bit in 14 bits.

A computer analysis shows that the actual errors in the table as implemented are as follows:

$+4.4 \times 10^{-5}$ (at 61.872°)

-4.7×10^{-5} (at 83.142°)

As the sine function is very linear in the LM-LL range, the third term of Equation 2 can be considered as being $1/(2)^3$ of the second term without significant error. Therefore, the same pattern can be used for the two lower ROMs in Figure 4, and a total of three different masks are needed. In addition, six 4-bit adders are used.

Order Number MM4232J or MM5232J
See Package 11

Order Number MM5232N
See Package 18

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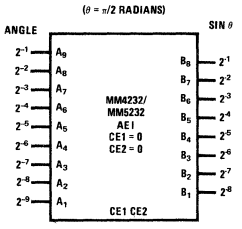


FIGURE 1

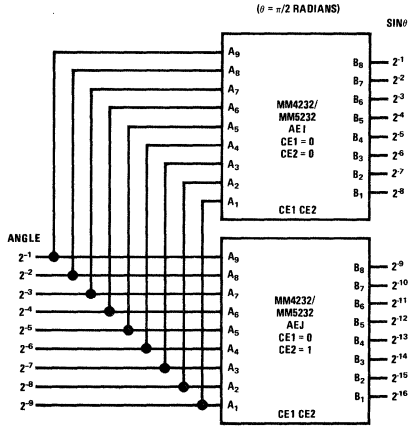


FIGURE 2

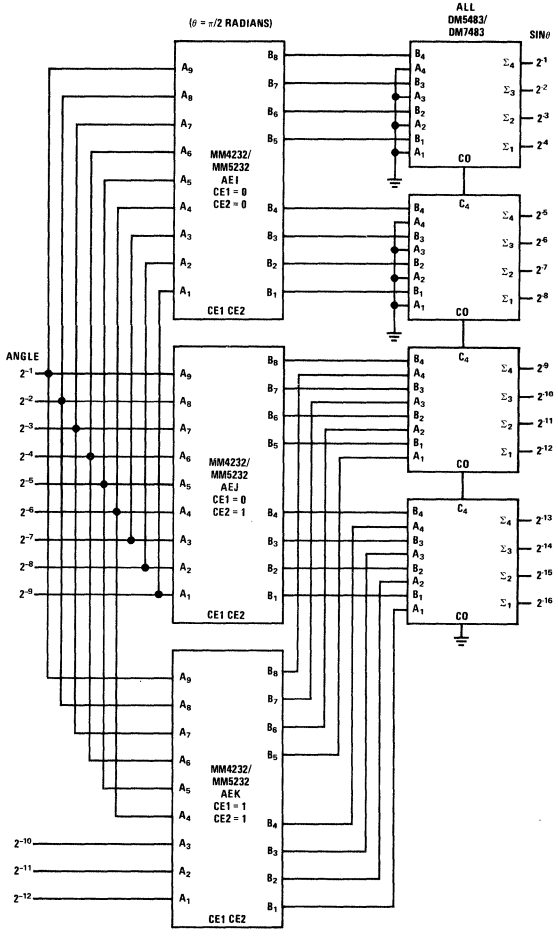


FIGURE 3.

Note: Angles are expressed as binary fractions of a right-angle.

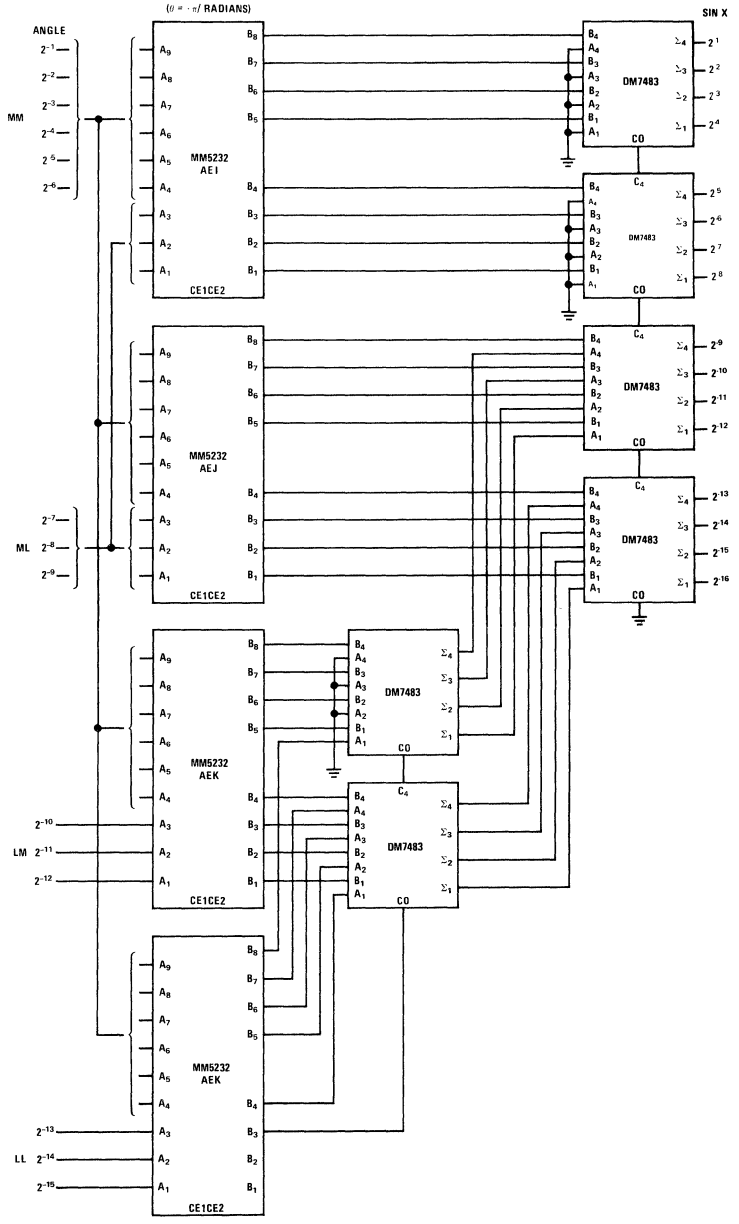
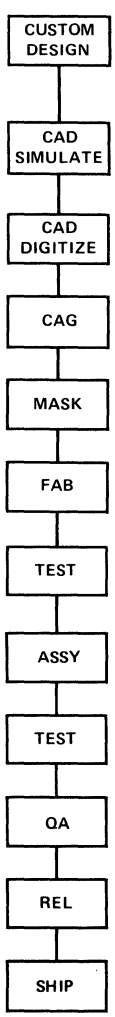


FIGURE 4

Note: Angles are expressed as binary fractions of a right angle.

Custom MOS/LSI

Custom MOS/LSI Product Flow



Interface between Customer and Design/Production Engineers	Product Definition
Time Sharing Computer Simulates Static and Dynamic Performance and Worst Case Parameters	Partitioning Simulation
Calma Digitizing System	Drafting Digitizing
David Mann Reticle Generator	10X Reticle Generation
David Mann 6-Barrel Step & Repeat Camera	Mask Making
Wafer Fabrication	Volume Wafer Production Santa Clara Facility
Teradyne J277, J283 Macrodata MD200 Fairchild Sentry 600	100% Waver Probe Test
Assembly	Volume Assembly, Worldwide
Teradyne J277, J283 Macrodata MD200 Fairchild Sentry 600	100% Finished Product Test
Quality Assurance	Internal Spec to MIL-STD 883
Reliability	High Rel Processing Available on all Products
Shipping	

INTRODUCTION

While custom and standard MOS have advantages over each other for specific applications, there is a high demand for both in today's electronics industry. In most cases, the true test of whether a system can most economically be implemented with standard, custom, or both, can only be determined after partitioning. If the quantities in question do not exceed a few hundred units per year, the standard product approach is probably the best solution. However, if the total number of units is many thousand per year, then customizing is usually the best approach.

Custom MOS circuits are designed to do a specific job. You are not buying capability that is not needed. The entire chip is devoted to performing your specific function. Advantages are:

1) Fewer Packages
2) Lower Power Dissipation
3) Smaller P.C. Boards
4) Proprietary Design

These advantages result in lower system costs and protection of your system design.

RESOURCES

National has brought together a group of experienced circuit and system designers, separate from the standard product group, to offer a custom MOS/LSI design service to the industry. This group is prepared to aid in the logic design of a system, partition the system into feasible LSI circuits if the design requires more than one chip, develop the chips, assist the customer in prototype system checkout, and put the design into production.

National has one of the most advanced IC manufacturing facilities in the industry. Your custom design will go through the same production facilities where National's standard MOS products are manufactured, and thus benefit from our long experience in MOS processing.

As with its bipolar circuits, the key to National's MOS program is volume production. We are a leading producer of shift registers, read-only memories, and random access memories. In the latter category, National is supplying many second source and proprietary static and dynamic RAMs as well as several advanced large-capacity RAMs.

National was the first company to offer MOS circuits that operate at voltage levels directly compatible with TTL. (Previously, level-shifters were needed if high-voltage MOS and low-voltage TTL were to work together). To achieve this so-called low-level MOS operation, National pioneered in the fabrication of circuits made from silicon cut along the (1-0-0) axis of the crystal. Subsequently, other companies developed bipolar compatible MOS circuits also.

1-0-0 P-channel metal gate and 1-1-1 silicon gate technologies are presently utilized by National in our standard MOS products. These processes have become industry standards. All of the P-channel MOS process devices offer bipolar compatibility.

Metal gate devices operate to 1.5 MHz. This technology is well-suited to random logic and ROM applications. Higher logic densities and operating frequencies approaching 5 MHz can be achieved by using silicon gate technology. This process lends itself to RAMs, registers, and random logic applications.

Static and dynamic logic is available in both metal and silicon gate devices. In general, less power is dissipated if dynamic logic is employed, which also offers the advantage of synchronous operation and eliminates hazards due to race conditions. In any event, power dissipation of typical LSI functions (up to 1000 gate functions) approach 500 mW in devices fabricated with either metal gate or silicon gate technology.

Complementary MOS (CMOS) technology is presently being used on many custom products. Structured logic, ROMs, RAMs, and registers, designed with CMOS cannot achieve the density of P-channel MOS. However, quiescent power and dissipations are less than one microwatt per gate. Operation to 10 MHz can be achieved. One of the advantages of CMOS is that power dissipation is a function of frequency, with the DC (quiescent) state consuming the least power.

The N-channel process is also undergoing development at National. This process allows higher density and high frequency operation than P-channel.

Ion implantation is a technique that can be applied to any of the previously mentioned processes. It allows threshold voltages to be adjusted to a desired level by implanting ions in the gate region. Depletion load devices and large value ohmic resistors are also being made with ion implantation, which greatly improves packing density on LSI chips.

DESIGN

Your custom design will benefit from National's longtime experience in the MOS business. Extensive use of computer-aided design (CAD) and computer simulation programs assure proper operation of your circuit before it goes into production.

All designs are verified with a circuit analysis program to assure proper operation. Worst case signal paths are checked to see that no signal race conditions exist.

Circuit layouts are performed using advanced CAD techniques. CAD system bypasses manual artwork generation entirely and goes directly from a digitized layout to 10X reciticles eliminating the need for rubylith and intermediate reduction steps. National's photomask generation laboratory is one of the best equipped in the industry including the Calma Digitizing System, the David Mann Pattern Generator, and 6-barrel Step and Repeat camera.

TESTING

National has a number of LSI testers that allow complete checkout of structured logic (ROMs, RAMs, shift registers, etc.) and random combinational logic. The random logic testers are computer programmed to test to the customer's input/output logic specifications. On-line testers include Teradyne J283, J277, Macrodata 230-2 LSI tester and Fairchild Sentry 600.

After fabrication, each wafer is checked for threshold voltage, breakdown voltage, oxide rupture and sheet resistivity. The wafer then goes into functional test. The logic on each die is thoroughly exercised. This 100% test of each wafer eliminates any functional defective die from being packaged.

After packaging, all devices are stressed to environmental extremes. The packaged devices are then returned for another functional test. Depending on the customer's requirement, packages can be tested under a variety of environmental conditions and can be subjected to a burn-in cycle. Full MIL-STD 883 processing is offered on all National custom and standard MOS devices.

QUALITY ASSURANCE

National's quality assurance department has a complete and comprehensive quality control program which effectively controls component parts and vendors at a quality level of functional, workmanship and dimensional criteria. The QA program also covers in-process controls of assembled devices, final electrical test, marking and final shipment of approved product. All procedures are documented at specification control and at respective quality inspection stations. Weekly and monthly reports are generated for quick feedback of information for corrective action purposes.

All inspections are performed to specified internal AQL inspection levels which meet or exceed MIL-STD 883.

RELIABILITY

The reliability evaluation program in effect at National is a continuous monitor on the process stability of assembled devices on extended life test. Tests which are performed on a continuous basis on each process are:

(a) High Temperature Operating Life Test (extended life)

(b) High Temperature Storage Test (extended life)

MIL-STD 883, which specifies testing procedures for integrated circuits, was innovatively handled by National. The company adopted 883 specs as its own, rather than to set up one procedure for military orders and another for industrial customers. Therefore, there are no dual standards at National. All devices are given the same quality control treatment and the company inventories devices with guaranteed 883 specs.

All standard devices undergo MIL-STD 883 testing. They are 100% subjected to a temperature cycle per Method 1003 Condition D, fine leak test per Method 1014 Condition A, Helium 5×10^{-7}, and gross leak test per Method 1014 Condition C.

The company has been informed by the National Aeronautics and Space Administration that it has received line certification under MIL-M-38510, the new military standard defining acceptable procedures for producing devices.

A customer may request any special rel processing per Document NSC/0002. The intent of this document is to provide the user with the ability to procure any integrated circuit manufactured by National to any class of MIL-STD 883 processing.

PACKAGES

National offers a variety of dual-in-line packages (DIPs), metal cans, flat packs, and specialized packages. Both ceramic and molded packages are available.

All packages meet the standard JEDEC registered outlines. Lead finishes are available in either gold or tin. The ceramic packages meet a leakage of 5×10^{-7} std cc He/sec leak rate. National's molded packages are the most advanced in the industry and afford reliability which rivals the ceramic packages.

Complex Standards

MM5307 baud rate generator/programmable divider

general description

The National Semiconductor MM5307 baud rate generator/programmable divider is an MOS/LSI P-channel enhancement mode device. A master clock for the device is generated externally. An internal ROM controls a divider circuit which produces the output frequency. Logic levels on the four control pins select between sixteen output frequencies. The frequencies are chosen from the following possible divisors: 2N, for $3 \leq N \leq 2048$; 2N + 1 and 2N + 0.5 for $4 \leq N \leq 2048$. Also one of the sixteen frequencies may be gated from the external frequency input. The MM5307AA is supplied with the divisors shown in Table I.

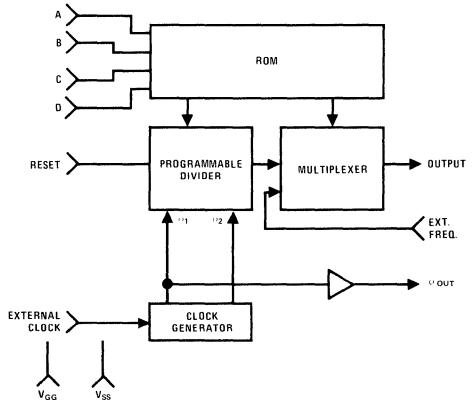
features

- Choice of 16 output frequencies from 1 crystal
- External frequency input pin
- Internal ROM allows generation of other frequencies on order
- Bipolar compatibility
- 1.0 MHz master clock frequency

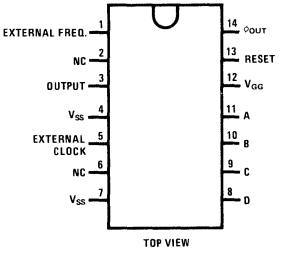
applications

- DAR/T clocks
- System clocks
- Electrically programmable counters

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5307 AA/D
See Package 2
Order Number MM5307AA/N
See Package 14

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absolute maximum ratings

Voltage at Any Pin With Respect to V_{SS}	+0.3V to V_{SS} − 20V
Power Dissipation	700 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating range, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP (NOTE 3)	MAX	UNITS
All Inputs					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 18		V_{SS} − 4.2	V
Leakage	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Capacitance	V_{IN} = 0V, f = 1.0 MHz All Other Pins GND (Note 1)		3.5	7.0	pF
Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	V_{SS} − 2.6	V_{SS}		V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			V_{SS} − 4.6	V
Power Supply Current (I_{GG})	f = 1.0 MHz		25	35	mA

ac electrical characteristics

T_A within operating range, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNITS
Master Frequency		0.01	1.5	1.0	MHz
Access Time (T_A)	C_L = 50 pF (Note 2)			16	μs
Reset Delay Time (t_{RD})	f = Master Clock Frequency			500 + 4/f	ns
Reset Pulse Width (R_{PW})		500 + 4/f			ns
Output Delay From Reset (t_{OD})				500 + 4/f	ns
Output Duty Cycle	T = Output Period f = Master Frequency		0.5T ±1/f		

Note 1: Capacitance is guaranteed by periodic measurement.

Note 2: Access time is defined as the time from a change in control inputs (A, B, C, D) to a stable output frequency. Access time is a function of frequency. The following formula may be used to calculate maximum access time for any master frequency: $T_A = 2.8\mu s + 1/f \times 13$, f is in MHz.

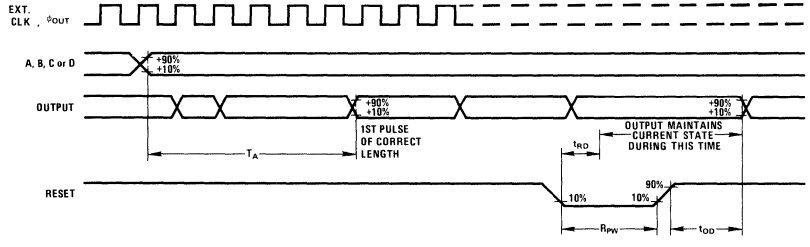
Note 3: Typical values for T_A = 25°C, V_{SS} = 5.0V and V_{GG} = −12V.

truth table

TABLE I. MM5307AA Output Details (921.6 kHz Master Clock Frequency)

CONTROL PINS A B C D	DIVISOR	OUTPUT FREQ kHz	COMMON BAUD RATES (OUTPUT FREQ/16)
0 0 0 1	1152	0.800	50
0 0 1 0	768	1.200	75
0 0 1 1	524	1.760	110
0 1 0 0	428.5	2.152	134.5
0 1 0 1	384	2.400	150
0 1 1 0	192	4.800	300
0 1 1 1	96	9.600	600
1 0 0 0	64	14.400	900
1 0 0 1	48	19.200	1200
1 0 1 0	32	28.800	1800
1 0 1 1	24	38.400	2400
1 1 0 0	16	57.600	3600
1 1 0 1	12	76.800	4800
1 1 1 0	8	115.200	7200
1 1 1 1	6	153.600	9600
0 0 0 0	–	EXT	–

timing diagram



Complex Standards

MM5309, MM5315 digital clocks

general description

These digital clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion implanted depletion mode devices. The devices provide all the logic required to build several types of clocks. Two display modes (four or six digits) facilitate end-product designs of varied sophistication. The circuits interface to LED and gas discharge displays with minimal additional components, and require only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking) or 24 hours. Outputs consist of multiplexed display drives ($\overline{BCD}$ and 7-segment) and digit enables. The devices operate over a power supply range of 11V to 19V and do not require a regulated supply. The MM5309 and MM5315 clocks are packaged in a 28 lead dual-in-line package.

features

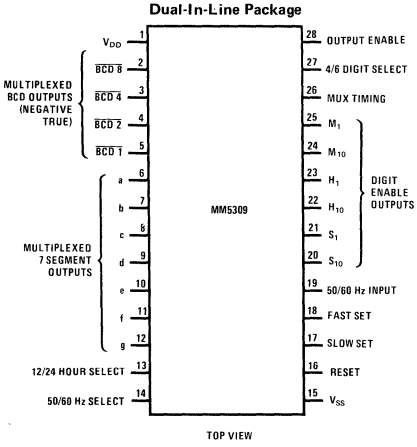
- Reset
- 50 or 60 Hz operation
- 4 to 6 digit display mode
- 12 or 24 hour display format
- Leading-zero blanking (12-hour format)
- $\overline{BCD}$ and 7-segment outputs
- Single power supply
- Fast and slow set controls
- Output enable control
- Internal multiplex oscillator
- Hold count control

applications

- Desk clocks
- Automobile clocks
- Industrial clocks
- Military clocks
- Interval timers

connection diagrams

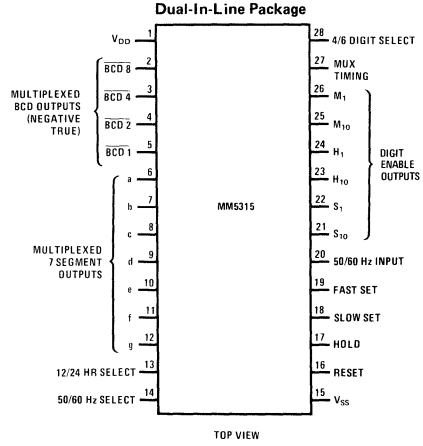
Dual-In-Line Package



TOP VIEW

Order Number 5309N
See Package 19

Dual-In-Line Package



TOP VIEW

Order Number MM5315N
See Package 19

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 20V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = +14V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{SS} (V_{DD} = 0V)	11	14	19	V
Power Supply Current	V_{SS} = +14V (No Output Loads)		2.0	10	mA
50/60 Hz Input Frequency		dc	50 or 60	60k	Hz
50/60 Hz Input Voltage					
Logical High Level		V_{SS} − 2.0	V_{SS} − 1.0	V_{SS}	V
Logical Low Level		−2.0	0	4.0	V
Multiplex Frequency	Determined by External R & C	dc	1.0	60	kHz
All Logic Inputs					
Logical High Level	Internal 20 kΩ Resistor to V_{SS}		V_{SS}		V
Logical Low Level		-2.0	0	4.0	V
$\overline{BCD}$ and 7-Segment Outputs					
Logical High Level	Loaded 2.0 kΩ to V_{DD}	2.0	5.0	20	mA source
Logical Low Level				0.01	mA source
Digital Enable Outputs					
Logical High Level				0.3	mA source
Logical Low Level	Loaded 100Ω to V_{SS}	5.0	10	25	mA sink

functional description

A block diagram of the MM5309 and MM5315 digital clocks is shown in Figure 1. Connection diagrams for these devices are shown on the front page. The following discussions are based on Figure 1.

50 or 60 Hz Input: This input is applied to a Schmitt trigger shaping circuit which provides approximately five volts of hysteresis and allows using a filtered sinewave input. A simple RC filter such as shown in Figure 10 should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the time keeping function.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1-pps timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{DD}. An internal 20 kΩ pull-up resistor is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation. As shown in Figure 1, the prescale counter provides both 1-pps and 10-pps signals, which can be brought out as bonding options.

Time Setting Inputs: Both fast and slow setting inputs, as well as a hold input, are provided. Internal 20 kΩ pull-up resistors provide the normal timekeeping function. Switching any of these inputs (one at a time) to V_{DD} results in the desired time setting function.

The three gates in the counter chain (Figure 1) are used for setting time. During normal operation, gate A connects the shaper output to a prescale counter (÷ 50 or ÷ 60); gates B and C cascade the remaining counters. Gate A is used to inhibit the input to the counters for the duration of slow, fast or hold time-setting input activity. Gate B is used to connect the shaper output directly to a seconds counter (÷ 60), the condition for slow advance. Likewise, gate C connects the shaper output directly to a minutes counter (÷ 60) for fast advance.

Fast set then, advances hours information at one hour per second and slow set advances minutes information at one minute per second.

12 or 24 Hour Select Input: This input is used to program the hours counter to divide by either 12 or 24, thereby providing the desired display format.

functional description (con't)

The 12-hour display format is selected by connecting this input to V_{DD}; leaving the input unconnected (internal 20 kΩ pull-up) selects the 24-hour format.

Output Multiplexer Operation: The seconds, minutes, and hours counters continuously reflect the time of day. Outputs from each counter (indicative of both units and tens of seconds, minutes, and hours) are time-division multiplexed to provide digit-sequential access to the time data. Thus, instead of requiring 42 leads to interconnect a six-digit clock and its display (7 segments per digit), only 13 output leads are required. The multiplexer is addressed by a multiplex divider decoder, which is driven by a multiplex oscillator. The oscillator and external timing components set the frequency of the multiplexing function and, as controlled by the 4 or 6 digit select input, the divider determines whether data will be output for 4 or 6 digits. A zero-blanking circuit suppresses the zero that would otherwise sometimes appear in the tens-of-hours display; blanking is effective only in the 12-hour format. The multiplexer addresses also become the display digit-enable outputs. The multiplexer outputs are applied to a decoder which is used to address a programmable (code converting) ROM. This ROM generates the final output codes, i.e., $\overline{BCD}$ and 7-segment. The sequential output order is from digit-6 (unit seconds) thru digit-1 (tens of hours).

Multiplex Timing Input: The multiplex oscillator is shown in Figure 2. Adding an external resistor and capacitor to this circuit via the multiplex timing input (as shown in Figure 10) produces a relaxation oscillator. The waveform at this input is a quasi-sawtooth that is squared by the shaping action of the Schmitt trigger in Figure 2. Figure 3 provides guidelines for selecting the external components relative to desired multiplex frequency.

Figure 4 illustrates two methods of synchronizing the multiplex oscillator to an external timebase. The external RC timing components may be omitted and this input may be driven by an external timebase; the required logic levels are the same as the 50 or 60 Hz input.

Reset: Applying V_{DD} to this input resets the counters to 0:00:00.00 in 12 hour format and 00:00:00.00 in 24 hour formats leaving the input unconnected (internal 20 kΩ pull-up) selects normal operation.

4 or 6 Digit Select Input: Like the other control inputs, this input is provided with an internal 20 kΩ pull-up resistor. With no input connection the clock outputs data for a 4 digit display. Applying V_{DD} to this input provides a 6 digit display.

Output Enable Input: With this pin unconnected the $\overline{BCD}$ and 7-segment outputs are enabled (via an internal 20 kΩ pull-up). Switching V_{DD} to this input inhibits these outputs. (Not applicable to MM4315 clock.)

Output Circuits: Figure 5-A illustrates the circuit used for the $\overline{BCD}$ and 7-segment outputs. Figure 5-B shows the digit enable output circuit. Figure 6 illustrates interfacing these outputs to standard and low-power TTL. Figures 7 and 8 illustrate methods of interfacing these outputs to common-anode and common-cathode LED displays, respectively. A method of interfacing these clocks to gas-discharge display tubes is shown in Figure 9. When driving gas-discharge displays which enclose more than one digit in a common gas envelope, it is necessary to inhibit the segment drive voltage(s) during inter-digit transitions. Figure 9 also illustrates a method of generating a voltage for application to the output enable input to accomplish the required inter-digit blanking.

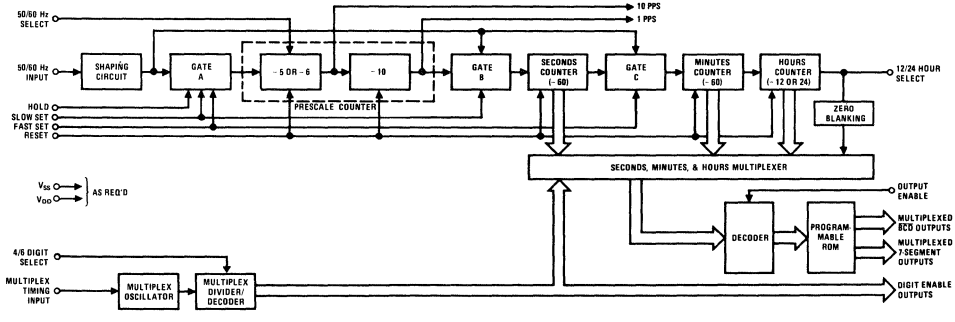


FIGURE 1. MM5309, MM5315 Digital Clock Block Diagram

functional description (con't)

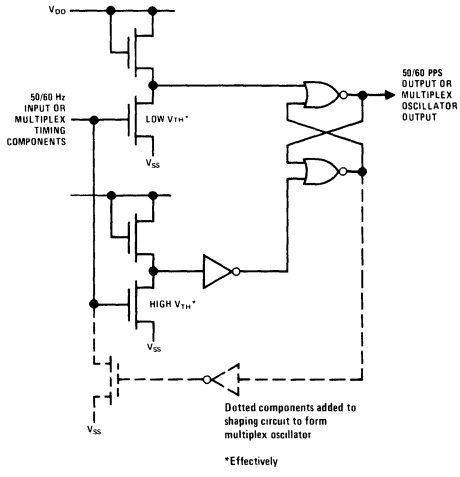


FIGURE 2. 50/60 Hz Shaping Circuit/Multiplex Oscillator

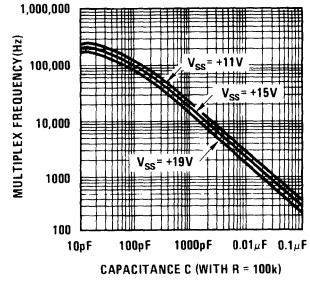
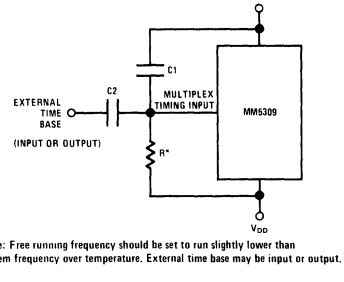


FIGURE 3. Multiplex Timing Component-Selection Guide



Note: Free running frequency should be set to run slightly lower than system frequency over temperature. External time base may be input or output.

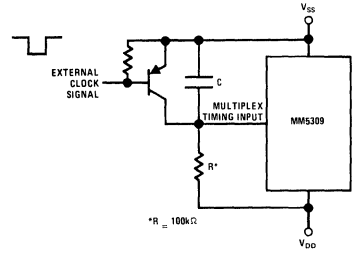
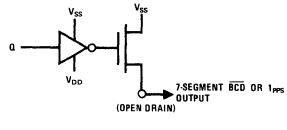
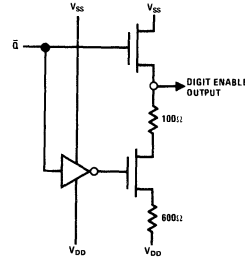


FIGURE 4. Synchronizing or Triggering Multiplex Oscillators



(A)



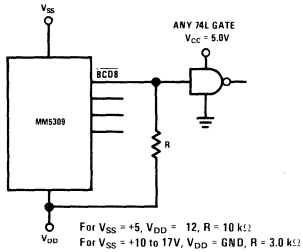
(B)

FIGURE 5. Output Circuits

10

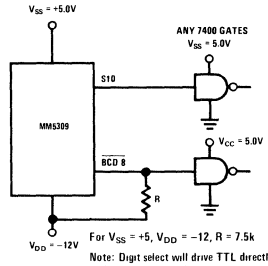
functional description (con't)

MOS to Low Power TTL Interface



For V_{SS} = +5, V_{DD} = 12, R = 10 kΩ
For V_{SS} = +10 to 17V, V_{DD} = GND, R = 3.0 kΩ

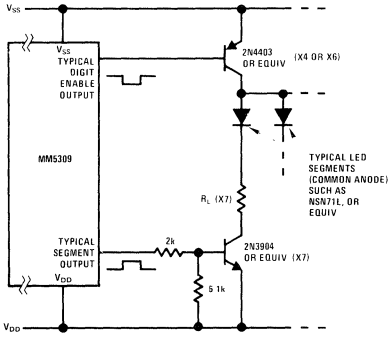
MOS to TTL Interface



For V_{SS} = +5, V_{DD} = −12, R = 7.5k

Note: Digit select will drive TTL directly when +5, −12 supplies are used.

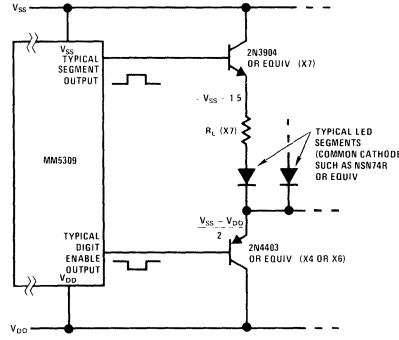
FIGURE 6. Interfacing TTL



$$R_L = \frac{V_{SS} \quad V_{DD} \quad V_F \quad 0.6V}{N(I_F)}$$

Where R_L is in kΩ
And V_F = forward drop of LED
0.6V ≈ voltage drop of transistors
N = number of digits in display
I_F = required average LED current

FIGURE 7. Interfacing Common-Anode LED Displays



$$R_L = \frac{(V_{SS} \quad V_{DD})/2 \quad V_F \quad 1.5V}{N(I_F)}$$

Where R_L is in kΩ
And V_F = forward drop of LED
0.9V = voltage drop of transistors
N = number of digits in display
I_F = required average LED current

FIGURE 8. Interfacing Common-Cathode LED Displays

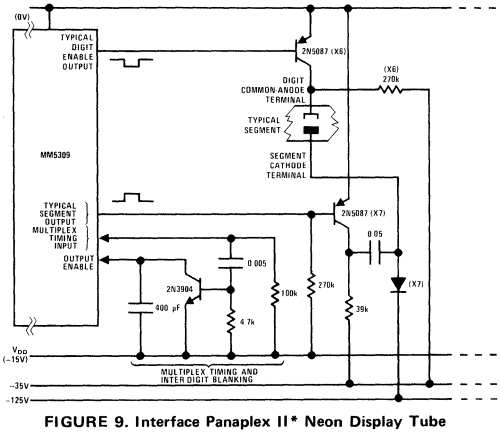


FIGURE 9. Interface Panaplex II* Neon Display Tube

*TM of Burroughs Corp.

functional description (con't)

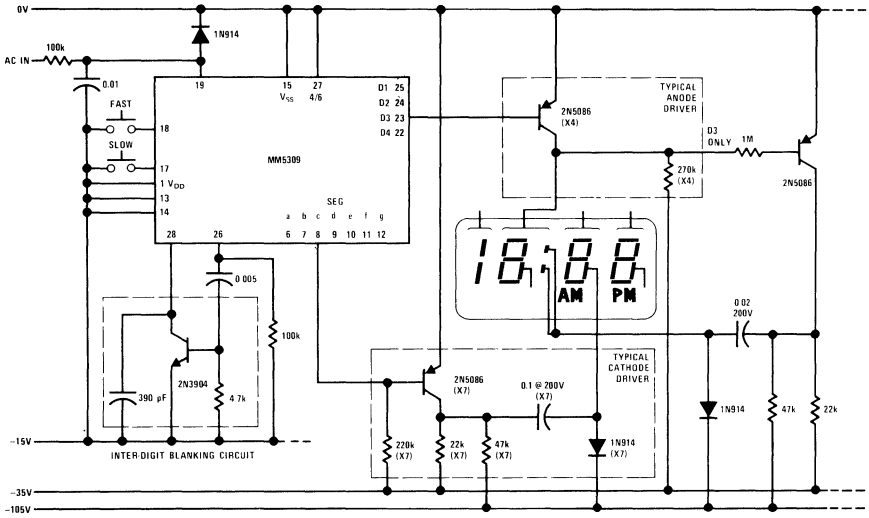


FIGURE 10. MM5309 Driving Gas-Discharge Display, Typical Applications

Complex Standards

MM5311,MM5312,MM5313,MM5314, digital clocks

general description

These digital clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode devices. The devices provide all the logic required to build several types of clocks. Two display modes (four or six digits) facilitate end-product designs of varied sophistication. The circuits interface to LED and gas discharge displays with minimal additional components, and require only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking) or 24 hours. Outputs consist of multiplexed display drives ($\overline{BCD}$ and 7-segment) and digit enables. The devices operate over a power supply range of 11 to 19V and do not require a regulated supply. The MM5311 through MM5314 clocks are packaged in 24 and 28 lead dual-in-line packages.

features

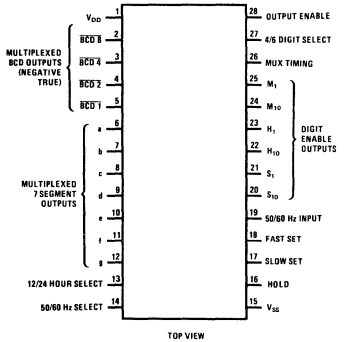
- 50 or 60 Hz operation
- 4 to 6 digit display mode
- 12 or 24 hour display format
- Leading-zero blanking (12-hour format)
- $\overline{BCD}$ and 7-segment outputs
- Single power supply
- Fast and slow set controls
- Output enable control
- Internal multiplex oscillator
- Hold count control

applications

- Desk clocks
- Automobile clocks
- Industrial clocks
- Military clocks

connection diagrams

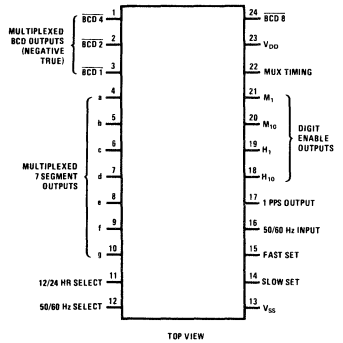
Dual-In-Line Package



TOP VIEW

Order Number MM5311D See Package 7 **Order Number MM5311N** See Package 19

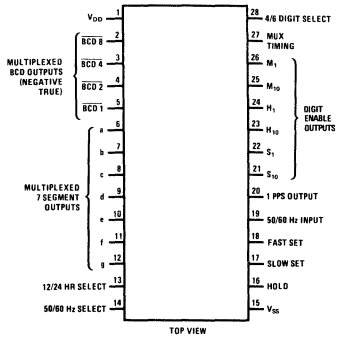
Dual-In-Line Package



TOP VIEW

Order Number MM5312D See Package 6 **Order Number MM5312N** See Package 18

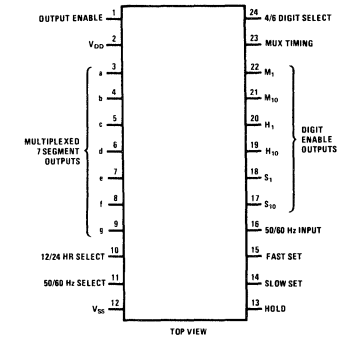
Dual-In-Line Package



TOP VIEW

Order Number MM5313D See Package 7 **Order Number MM5313N** See Package 19

Dual-In-Line Package



TOP VIEW

Order Number MM5314D See Package 6 **Order Number MM5314N** See Package 18

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 20V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = +14V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{SS} (V_{DD} = 0V)	11	14	19	V
Power Supply Current	V_{SS} = +14V (No Output Loads)		8.0	15	mA
50/60 Hz Input Frequency		dc	50 or 60	60k	Hz
50/60 Hz Input Voltage					
Logical High Level		V_{SS} − 2.0	V_{SS} − 1.0	V_{SS}	V
Logical Low Level		−2.0	0	4.0	V
Multiplex Frequency	Determined by External R & C	dc	1.0	60	kHz
All Logic Inputs					
Logical High Level	Internal 20kΩ Resistor to V_{SS}		V_{SS}		V
Logical Low Level		−2.0	0	4.0	V
$\overline{BCD}$ and 7-Segment Outputs					
Logical High Level	Loaded 2kΩ to V_{DD}	2.0	5.0	20	mA source
Logical Low Level				0.01	mA source
Digital Enable Outputs					
Logical High Level				0.3	mA source
Logical Low Level	Loaded 100Ω to V_{SS}	5.0	10.0	25	mA sink

functional description

A block diagram of the MM5311 thru MM5314 digital clocks is shown in Figure 1. The various functional capabilities of the clocks are listed in Table 1. Connection diagrams for these devices are shown on page 1. The following discussions are based on Figure 1.

50 or 60 Hz Input: This input is applied to a Schmitt trigger shaping circuit which provides approximately five volts of hysteresis and allows using a filtered sinewave input. A simple RC filter such as shown in Figure 10 should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the time keeping function.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1-pps timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{DD}. An internal 20 kΩ pull-up resistor is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation. As shown in Figure 1, the prescale counter provides both 1-pps and 10-pps signals. As shown in Table 1, the MM5312 and MM5313 clocks provide the 1-pps signal as an output. On these clocks, the 10-pps signal (in place of the 1-pps signal) may be selected as an output via a lead-bonding option.

Time Setting Inputs: Both fast and slow setting inputs, as well as a hold input, are provided. Internal 20 kΩ pull-up resistors provide the normal timekeeping function. Switching any of these inputs (one at a time) to V_{DD} results in the desired time setting function.

The three gates in the counter chain (Figure 1) are used for setting time. During normal operation, gate A connects the shaper output to a prescale counter (÷ 50 or ÷ 60); gates B and C cascade the remaining counters. Gate A is used to inhibit the input to the counters for the duration of slow, fast or hold time-setting input activity. Gate B is used to connect the shaper output directly to a seconds counter (÷ 60), the condition for slow advance. Likewise, gate C connects the shaper output directly to a minutes counter (÷ 60) for fast advance.

Fast set then, advances hours information at one hour per second and slow set advances minutes information at one minute per second.

12 or 24 Hour Select Input: This input is used to program the hours counter to divide by either 12 or 24, thereby providing the desired display format. The 12-hour display format is selected by connecting this input to V_{DD}; leaving the input unconnected (internal 20 kΩ pull-up) selects the 24-hour format.

Output Multiplexer Operation: The seconds, minutes, and hours counters continuously reflect the time of day. Outputs from each counter (indicative of both units and tens of seconds, minutes, and hours) are time-division multiplexed to provide digit-sequential access to the time data. Thus, instead of requiring 42 leads to interconnect a six-digit clock and its display (7 segments per digit), only 13 output leads are required. The multiplexer is addressed by a multiplex divider decoder, which is driven by a multiplex oscillator. The oscillator and external timing components set the frequency of the multiplexing function and, as controlled by the 4 or 6 digit select

functional description (con't)

input, the divider determines whether data will be output for 4 or 6 digits. A zero-blanking circuit suppresses the zero that would otherwise sometimes appear in the tens-of-hours display; blanking is effective only in the 12-hour format. The multiplexer addresses also become the display digit-enable outputs. The multiplexer outputs are applied to a decoder which is used to address a programmable (code converting) ROM. This ROM generates the final output codes, i.e., $\overline{BCD}$ and 7-segment. The sequential output order is from digit-6 (unit seconds) thru digit-1 (tens of hours).

Multiplex Timing Input: The multiplex oscillator is shown in Figure 2. Adding an external resistor and capacitor to this circuit via the multiplex timing input (as shown in Figure 10) produces a relaxation oscillator. The waveform at this input is a quasi-sawtooth that is squared by the shaping action of the schmitt trigger in Figure 2. Figure 3 provides guidelines for selecting the external components relative to desired multiplex frequency. Figure 4 illustrates two methods of synchronizing the multiplex oscillator to an external timebase. The external RC timing components may be omitted and this input may be driven by an external timebase; the required logic levels are the same as the 50 or 60 Hz input.

4 or 6 Digit Select Input: Like the other control inputs, this input is provided with an internal 20 kΩ pull-up resistor. With no input connection the clock outputs data for a 4 digit display. Applying V_{DD} to this input provides a 6 digit display (not applicable to the MM5312 clock, see Table 1).

Output Enable Input: With this pin unconnected the $\overline{BCD}$ and 7-segment outputs are enabled (via an internal 20 kΩ pull-up). Switching V_{DD} to this input inhibits these outputs.

Output Circuits: Figure 5-A illustrates the circuit used for the $\overline{BCD}$ and 7-segment outputs. Figure 5-B shows the digit enable output circuit. Figure 6 illustrates interfacing these outputs to standard and low-power TTL. Figures 7 and 8 illustrate methods of interfacing these outputs to common-anode and common-cathode LED displays, respectively. A method of interfacing these clocks to gas-discharge display tubes is shown in Figure 9. When driving gas-discharge displays which enclose more than one digit in a common gas envelope, it is necessary to inhibit the segment drive voltage(s) during inter-digit transitions. Figure 9 also illustrates a method of generating a voltage for application to the output enable input to accomplish the required inter-digit blanking.

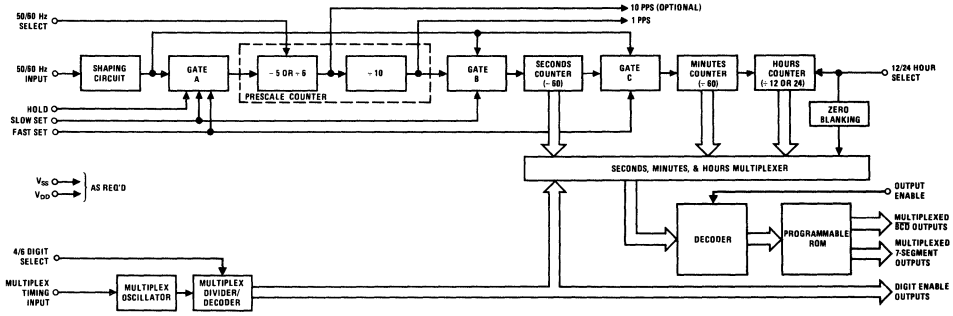


FIGURE 1. MM5311 thru MM5314 Digital Clocks, Block Diagram

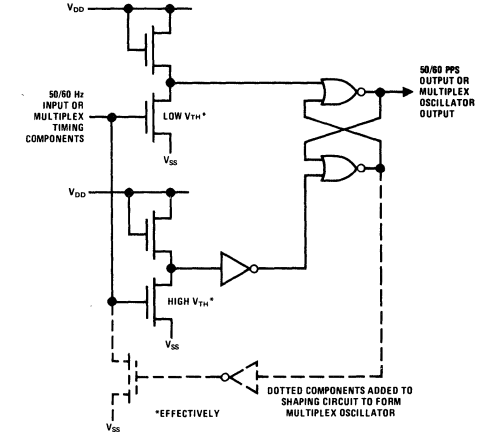


FIGURE 2. 50/60 Hz Shaping Circuit/Multiplex Oscillator

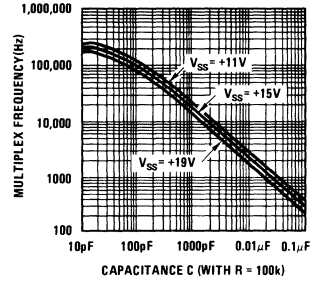
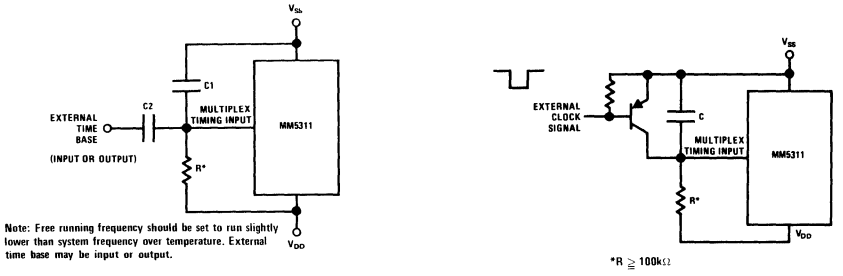


FIGURE 3. Multiplex Timing Component-Selection Guide

functional description (con't)



Note: Free running frequency should be set to run slightly lower than system frequency over temperature. External time base may be input or output.

FIGURE 4. Synchronizing or Triggering Multiplex Oscillators

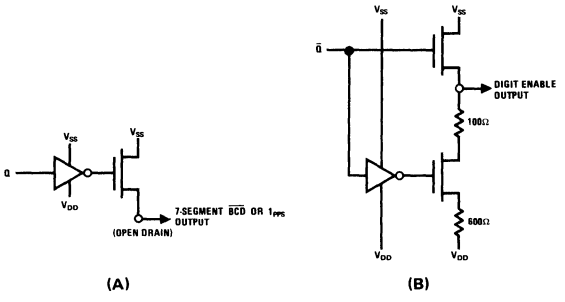


FIGURE 5. Output Circuits

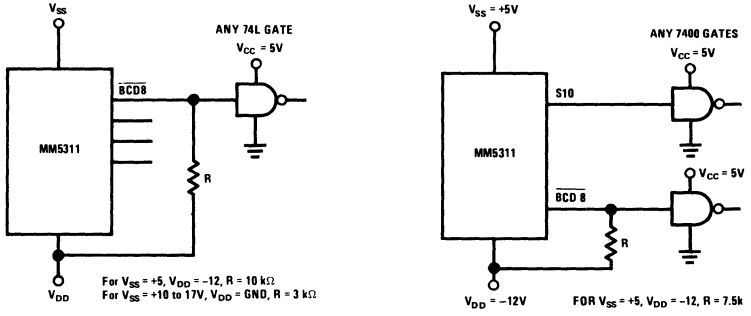
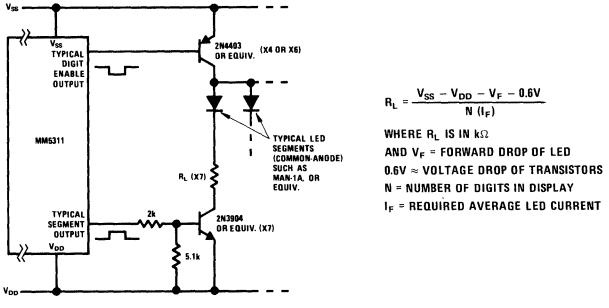


FIGURE 6. Interfacing TTL



$$R_L = \frac{V_{SS} - V_{DD} - V_F - 0.6V}{N\ (I_F)}$$

WHERE R_L IS IN kΩ
AND V_F = FORWARD DROP OF LED
0.6V ≈ VOLTAGE DROP OF TRANSISTORS
N = NUMBER OF DIGITS IN DISPLAY
I_F = REQUIRED AVERAGE LED CURRENT

FIGURE 7. Interfacing Common-Anode LED Displays

10

functional description (con't)

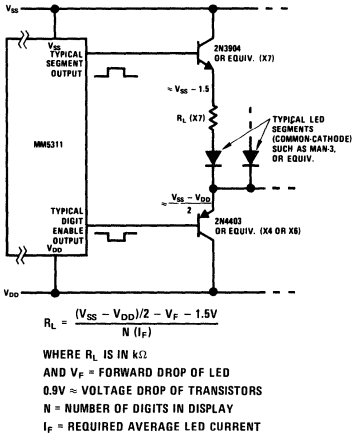


FIGURE 8. Interfacing Common-Cathode LED Displays

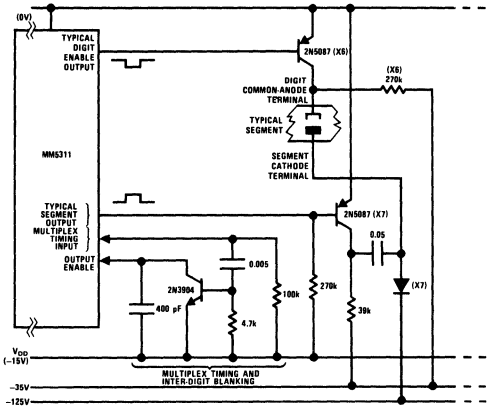


FIGURE 9. Interfacing Panaplex II* Neon Display Tube

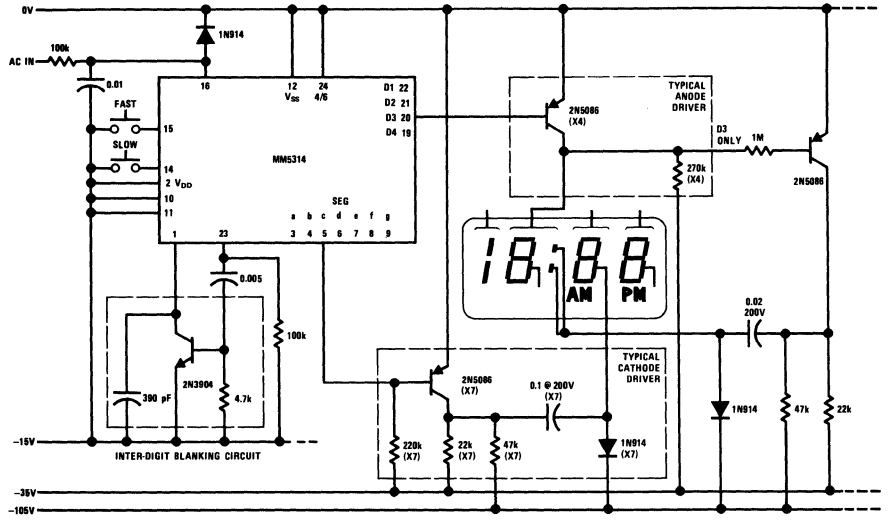


FIGURE 10. MM5314AN Driving Gas-Discharge Display, Typical Application

*TM of Burroughs Corp.

Complex Standards

MM5316 digital alarm clock

general description

The MM5316 digital alarm clock is a monolithic MOS integrated circuit utilizing p-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. It provides all the logic required to build several types of clocks and timers. Four display modes (time, seconds, alarm and sleep) are provided to optimize circuit utility. The circuit interfaces directly with seven-segment fluorescent tubes or liquid crystal displays, and requires only a single power supply. The time-keeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking and AM/PM indication) or 24 hours. Outputs consist of display drives, sleep (e.g., timed radio turn-off), and alarm enable. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. The device operates over a power supply range of 8 to 29 volts and does not require a regulated supply. The MM5316 is packaged in a 40-lead dual-in-line package.

features

- 50 or 60 Hz operation
- Single power supply
- Low power dissipation (32 mW at 8V)
- 12 or 24 hour display format
- AM/PM outputs } 12-hour format
- Leading-zero blanking }
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Blanking/brightness control capability
- Elimination of illegal time display at turn-on
- Direct interface to fluorescent tubes or liquid crystal displays
- 9-minute snooze alarm
- Presettable 59-minute sleep timer

applications

- Alarm clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Stopwatches
- Industrial clocks
- Military clocks
- Portable clocks
- Photography timers
- Industrial timers
- Appliance timers
- Sequential controllers

block and connection diagrams

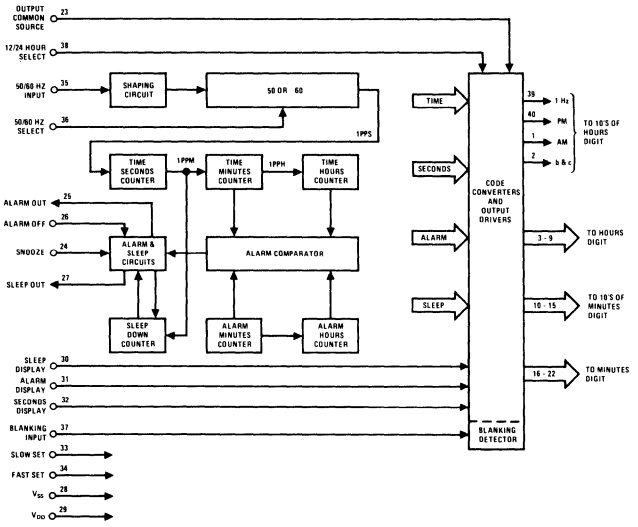
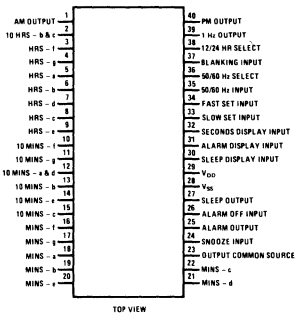


FIGURE 1. MM5316 Digital Alarm Clock, Block Diagram

Dual-In-Line Package



Order Number MM5316D
See Package 8
Order Number MM5316N
See Package 20

FIGURE 2. Connection Diagram

absolute maximum ratings

Voltage at Any Pin	V_{SS} +0.3 to V_{SS} −29V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating range, V_{SS} = +8 to +29V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage:	V_{SS} (V_{DD} = 0V)	+8		+29	V
Power Supply Current:	no output loads				
	V_{SS} = +8V		2	4	mA
	V_{SS} = +29V		3	5	mA
50/60 Hz Input:					
Frequency		DC	50 or 60	30k	Hz
Voltage					
Logical High Level		V_{SS}−1		V_{SS}	V
Logical Low Level		V_{DD}		V_{DD}+1	V
Blanking Input Voltage:					
Logical High Level		V_{SS}−2		V_{SS}	V
Logical Low Level		V_{DD}		V_{SS}−4	V
All Other Input Voltages:					
Logical High Level		V_{SS}−1		V_{SS}	V
Logical Low Level	Internal 2.5 MΩ Resistor to V_{DD}	V_{DD}	V_{DD}	V_{DD} + 2	V
Power Failure Detect Voltage:	(V_{SS} Voltage)	9		20	V
Output Currents:	V_{SS} = +21 to +29V, V_{DD} = 0V				
1 Hz Display					
Logical High Level	V_{OH} = V_{SS} − 2V	1500			μA
Logical Low Level	V_{OL} = V_{DD}			1	μA
10's of Hours (b&c), 10's of Minutes (a&d)					
Logical High Level	V_{OH} = V_{SS} − 2V	1000			μA
Logical Low Level	V_{OL} = V_{DD}			1	μA
All Other Display, Alarm and Sleep Outputs					
Logical High Level	V_{OH} = V_{SS} − 2V	500			μA
Logical Low Level	V_{OL} = V_{DD}			1	μA

functional description

A block diagram of the MM5316 digital alarm clock is shown in Figure 1. The various display modes provided by this clock are listed in Table 1. The functions of the setting controls are listed in Table 2. Figure 2 is a connection diagram. The following discussions are based on Figure 1.

50 or 60 Hz Input (pin 35): A shaping circuit (Figure 3) is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 6V of hysteresis. A simple RC filter, such as shown in Figure 7, should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input (pin 36): A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1-pps time base. This counter is programmed to divide by 60 simply by leaving pin 38 unconnected; pull-down to V_{DD} is provided by an internal 2.5 MΩ resistor. Operation at 50 Hz is programmed by connecting pin 38 to V_{SS}.

Display Mode Select Inputs (pins 30 thru 32): In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal 2.5 MΩ pull-down resistors allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table 1. Alternate display modes are selected by applying V_{SS} to the appropriate pin. As shown in Figure 1 the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs (pins 33 and 34): Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table 2. Again, internal 2.5 MΩ pull-down resistors are provided; application of V_{SS} to these pins effects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM, in the 12-hour format (00:00:00 in the 24-hour format), by selecting seconds display and actuating both slow and fast set inputs.

Blanking Control Input (pin 37): Connecting this Schmitt trigger input to V_{DD} places all display drivers in a non-conducting, high-impedance state, thereby inhibiting the display. See Figures 3 and 4. Conversely, V_{SS} applied to this input enables the display.

Output Common Source Connection (pin 23): All display output drivers are open-drain devices with all sources common to pin 23 (Figure 4). When using fluorescent tube displays, V_{SS} or a display brightness control voltage is permanently connected to this pin. Since the brightness of a fluorescent tube display is dependent on the anode (segment) voltage, applying a variable voltage to pin 23 results in a display brightness control. This control is shown in Figure 7. However, when using liquid crystal displays, the lifetime of the display device is optimized when AC drive voltages are provided. The common source connection of the MM5316 output drivers facilitates generating AC drive voltages. An interface circuit for driving liquid crystal displays is shown in Figure 5.

12 or 24 Hour Select Input (pin 38): By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal 2.5 MΩ pull-down resistor is again provided. Connecting this pin to V_{SS} programs the 24-hour display format. Also, the output connections (pins 1, 2, 39 and 40) are different for each format. Figure 6 illustrates these differences. In addition to displaying 10's of hours, this digit provides an AM/PM indication (12-hour format only) and the power failure indication. In the 12-hour format, AM indication is provided by segment "f"; PM indication by segment "e." The power failure indication consists of a flashing of the AM or PM indicator at a 1-Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal. In the 24-hour format, the power failure indication consists of flashing segments "c" and "f" for times less than 10 hours, and of a flashing segment "c" for times equal to or greater than 10 hours but less than 20 hours; and a flashing segment "g" for times equal to or greater than 20 hours.

Alarm Operation and Output (pin 25): The alarm comparator (Figure 1) senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver (Figure 4), the MM5316 output that is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input (pin 24) or reset by the alarm off input (pin 26).

Snooze Alarm Input (pin 24): Momentarily connecting pin 24 to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-down to V_{DD} by an internal 2.5 MΩ resistor. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

functional description (con't)

Alarm Off Input (pin 26): Momentarily connecting pin 26 to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal 2.5 MΩ resistor. The momentary alarm off input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm off input should remain at V_{SS}.

Sleep Timer and Output (pin 27): The sleep output at pin 27 can be used to turn off a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (Table 1) and setting the desired time interval (Table 2). This automatically results in a current-source output via pin 27, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning off the radio. This turn-off may also be manually controlled (at any time in the countdown) by a momemtary V_{SS} connection to the snooze input (pin 24). The output circuitry is the same as the other outputs (Figure 4).

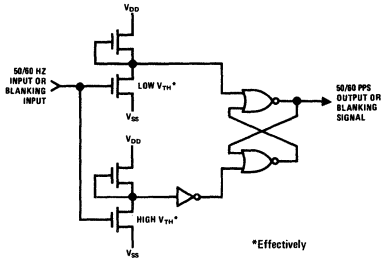


FIGURE 3. 50/60 Hz or Blanking Input Shaping Circuits

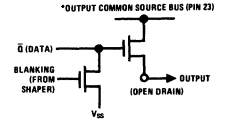
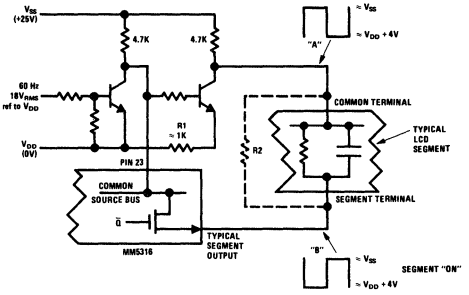


FIGURE 4. Output Circuits



Note 1: R1 should be chosen for equal peak-to-peak swings at points "A" and "B," so there is no dc component placed on the segment.

Note 2: R2 may or may not be required, depending on the display used and the parasitic circuit capacitance associated with the segment output. This resistor should be just small enough to assure that off segments are not visible.

FIGURE 5. Liquid Crystal Display Interface

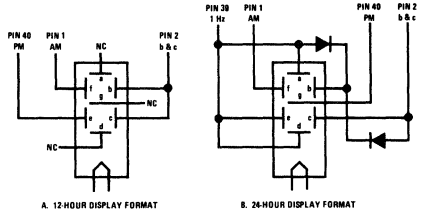


FIGURE 6. Wiring Ten's-of-hours Digit

functional description (con't)

TABLE 1. MM5316 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

TABLE 2. MM5316 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 00:00 (24-hour format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (12-hour format)
	Both	Time Resets to 00:00:00 (24-hour format)
Sleep	Slow	Substracts Count at 2 Hz
	Fast	Substracts Count at 60 Hz
	Both	Substracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

typical application

Figure 7 is a schematic diagram of a general purpose alarm clock using the MM5316 and a fluorescent tube display.

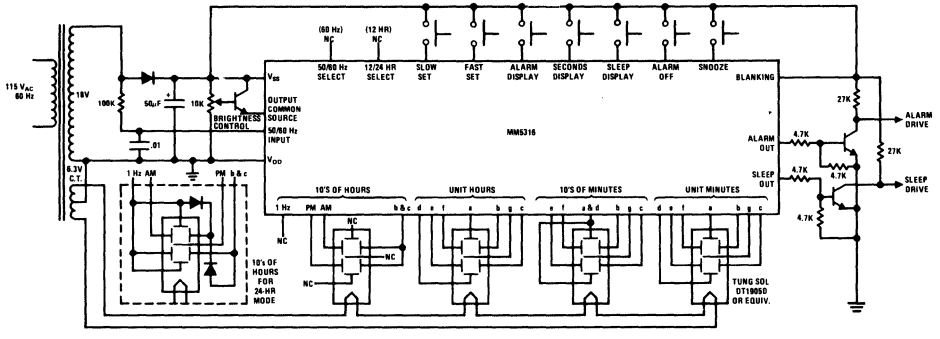


FIGURE 7. Typical Application

Complex Standards

MM4320/MM5320 TV camera sync generator

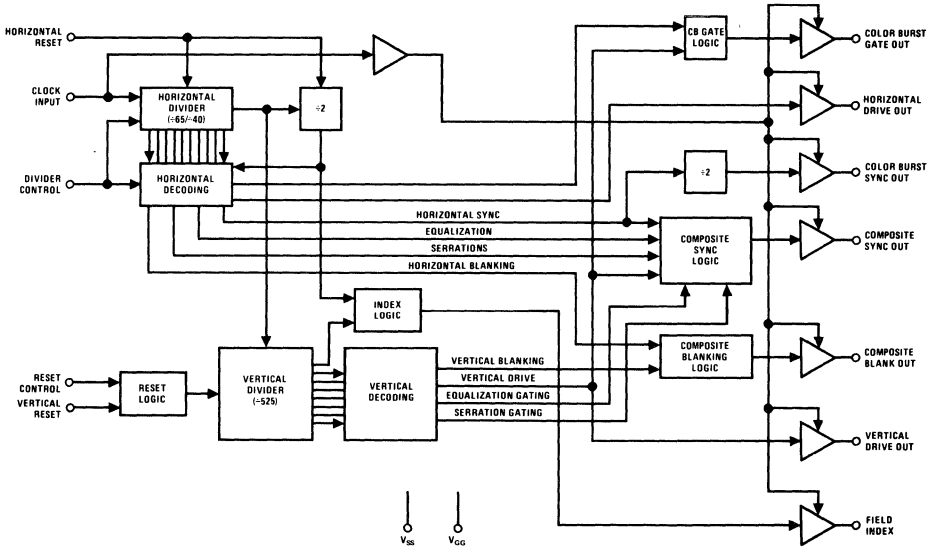
general description

The MM4320/MM5320 TV camera sync generator is an MOS, P-channel enhancement mode, LSI chip designed to supply the basic sync functions for either color or monochrome 525 line/60 Hz interlaced camera and video recorder applications. Required power supplies are +5V and −12V, or any other combination resulting in V_{SS} − 17V. All inputs and outputs are TTL compatible without the use of external components. Military and commercial temperature ranges are available.

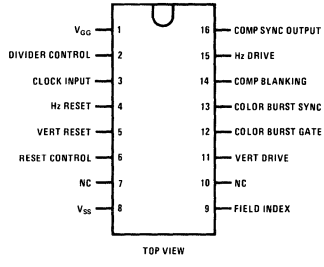
features

- Multi-function gen lock input provides flexible control of multiple camera installations
- 16 lead dual-in-line package
- Conventional +5V, −12V power supplies
- Uses 2.04545 MHz or 1.260 MHz input reference
- Field indexing provided for VTR applications
- Color burst gate and sync allow stable color operation

logic and connection diagrams



Dual-In-Line Package



Order Number MM4320D
or MM5320D
See Package 3

Order Number MM5320N
See Package 15

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 22
Operating Temperature	
MM4320	−55°C to +85°C
MM5320	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 18		V_{SS} − 4.2	V
Input Leakage	V_{IN} = −10V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Input Capacitance	V_{IN} = 0V, f = 1.0 MHz, All Other Pins GND (Note 1)		3.5	6.0	pF
Clock Input Leakage	V_{IN} = −10V, T_A = 25°C, All Other Pins GND			0.5	μA
Clock Input Capacitance	V_{IN} = 0V, f = 1.0 MHz, All Other Pins GND (Note 1)		3.5	6.0	pF
Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Logical Low Level (V_{OL})	MOS Load	V_{SS} − 12.5	V_{SS} − 11	V_{SS} − 9.0	V
Power Supply Current (I_{GG})	T_A = +25°C, V_{GG} = −12V, ϕ_{PW} = 235 ns, V_{SS} = +5.0V, Input Clock Frequency = 2.04545 MHz		24	36	mA

ac electrical characteristics

T_A within operating temperature range V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Pulse Width (ϕ_{PW})	Input Clock Frequency = 2.04545 MHz, ϕt_r, ϕt_f = 20 ns				
	MM4320	210	235	260	ns
	MM5320	190	235	280	ns
Input Clock Pulse Width (ϕ_{PW})	Input Clock Frequency = 1.26 MHz, ϕt_r = ϕt_f = 20 ns (Note 3)				
	MM4320	530	545	560	ns
	MM5320	520	545	570	ns
Horizontal Reset Pulse Width	Within 400 ns after the Falling Edge of Master Clock (Figure 5) Rise and Fall Time = 20 ns	500	600	800	ns
Output Propagation Delay (t_{pd})					
Logical High Level (V_{OH})	Capacitance at the Output = 15 pF		500	750	ns
Logical Low Level (V_{OL})	(Figure 5)		500	750	ns
Field Index Pulse Width	Within 400 ns after the Falling Edge of Master Clock (Figure 5) (Note 2) Rise and Fall Time = 20 ns	500	600	700	ns

Note 1: Capacitance is guaranteed by periodic testing.

Note 2: Field index output available only for master clock of 1.26 MHz.

Note 3: If field index is not required the clock pulse width is:

MM4320 400 ns ≤ ϕ_{PW} ≤ 560 ns

MM5320 300 ns ≤ ϕ_{PW} ≤ 570 ns

10

functional description

EXTERNAL CONTROL LEVELS

Horizontal Reset occurs for Logic "0," this resets the horizontal counter to a state shown in Figure 2, 3.

Vertical Reset occurs for Logic "0," this resets the vertical counter to a state determined by reset control input as shown below:

RESET CONTROL INPUT	PERMITS THE VERTICAL COUNTER TO RESET TO THE:
V_{IH}, (V_{SS})	0 th count
V_{IL}, (V_{GG})	11 th count

Logic "0" = V_{IL}

Logic "1" = V_{IH}

Divide select input = V_{IL}, (V_{GG}) for master clock frequency of 1.26 MHz.

Divide select input = V_{IH}, (V_{SS}) for master clock frequency of 2.04545 MHz.

INPUTS

The user may select either of two input clock frequencies by properly programming the Divider Control pin. In one case the input frequency is 2.04545 MHz; which is 14.318180 MHz divided by seven. The other is eighty times the horizontal frequency, or 1.260 MHz. The divider control will be programmed by connecting it to V_{IH} (V_{SS}) and V_{IL}, (V_{GG}) respectively.

There are separate *Vertical* and *Horizontal Reset* inputs which allow directly resetting the appropriate divider(s) by a control pulse generated by external means. Both horizontal and vertical dividers may be reset simultaneously by connecting the *Vertical* and *Horizontal Reset* pins together and driving them with the same reset signal. Actual resetting of the vertical divider is to either of two states, depending upon the state of the *Reset Control* input; to zero, or to the fifth vertical serration pulse (eleven 0.5H time intervals from leading edge of *Vertical Blanking*). Refer to the reset table above. The horizontal divider will always be reset to a position which is 8 input clock pulses from the leading edge of the serration gate in the horizontal timing scheme (Figure 2 and 3). The generator is reset to the odd field (field one). The *Field Index* output pulse occurs once each odd field at the leading edge of *Vertical Blanking.* It can be used to reset, or "gen-lock," similar sync generator chips by connecting it to their *Vertical* and *Horizontal Reset* inputs.

OUTPUTS

The generator supplies the following standard output functions: *Horizontal Drive Out, Vertical Drive Out, Composite Blanking Out, Composite Sync Out* and the *Color Burst Gate.*

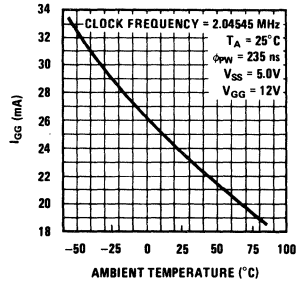
In addition, *Field Index* and *Color Burst Sync* outputs are provided. The *Field Index* identifies the odd field, or field one, by occurring for two clock periods at the leading edge of Vertical Blanking in that field. Thus, its rate is 30 Hz. As described above, it can also be used to "gen-lock" other sync generator chips.

The *Color Burst Sync* output signal occurs at half the horizontal rate with the same timing as the *Color Burst Gate* output. It may be used to sync the color burst as it will have the same delay characteristics as the other outputs (including, of course, the *Color Burst Gate*) — the color burst sync is present during the vertical interval.

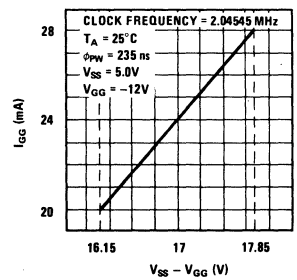
Differences in phasing between outputs are minimized by the use of identical push-pull output buffers clocked by the internal clock.

typical performance characteristics

Typical I_{GG} vs Temperature



Typical I_{GG} vs Power Supply Voltage ($V_{SS} - V_{GG}$)



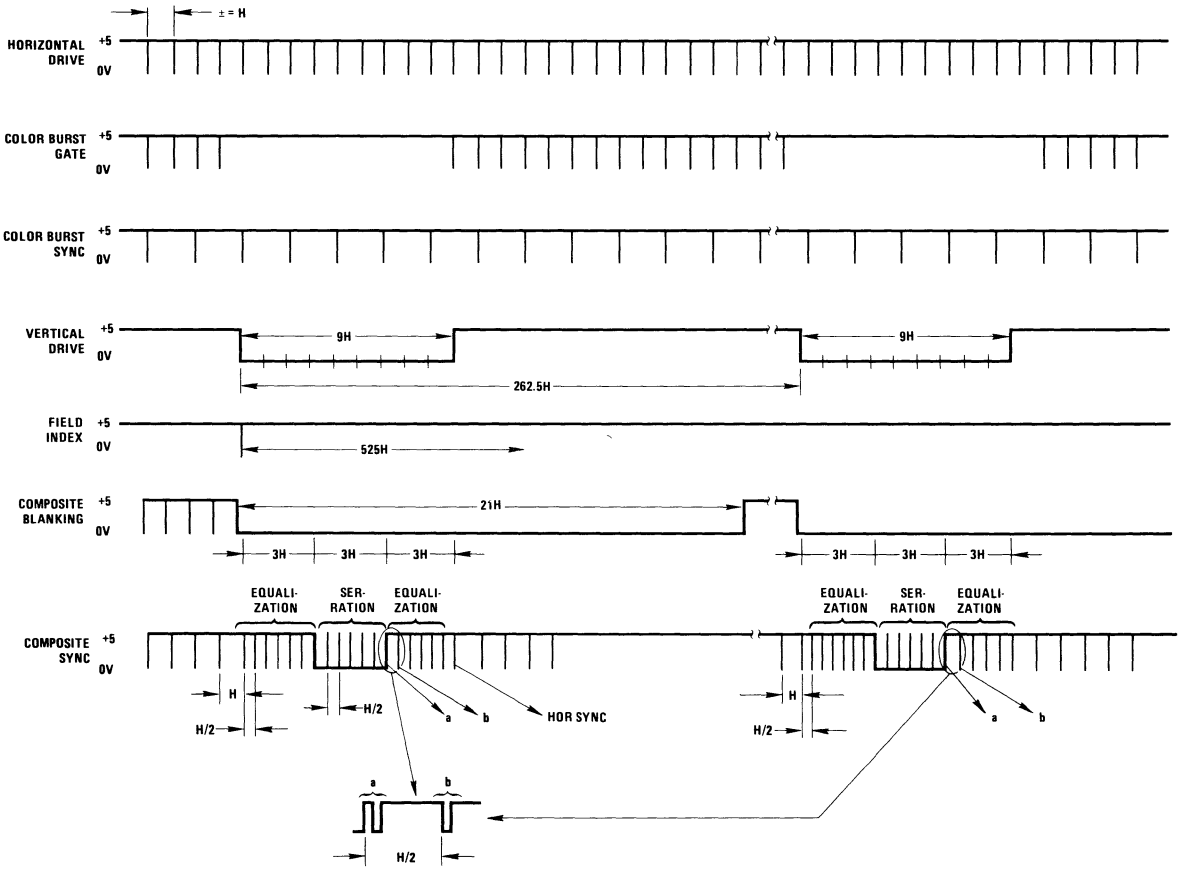

± = H
HORIZONTAL DRIVE
+5
0V
COLOR BURST GATE
COLOR BURST SYNC
VERTICAL DRIVE
9H
262.5H
FIELD INDEX
525H
COMPOSITE BLANKING
21H
3H
EQUALI-ZATION
SER-RATION
COMPOSITE SYNC
H
H/2
a
b
HOR SYNC

FIGURE 1.

switching time waveforms (con't)

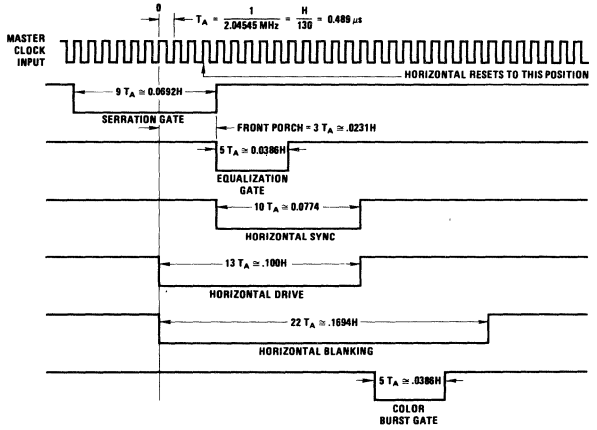


FIGURE 2. Horizontal Timing Master Clock = 2.04545 MHz

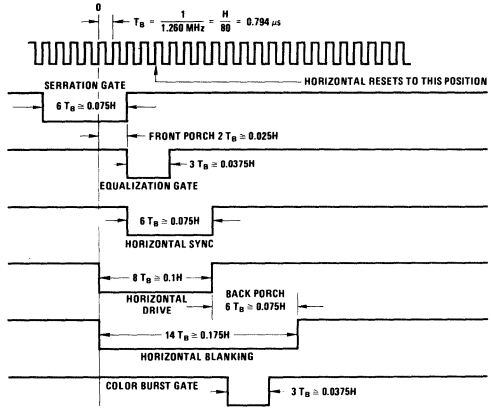


FIGURE 3. Horizontal Timing Master Clock = 1.26 MHz

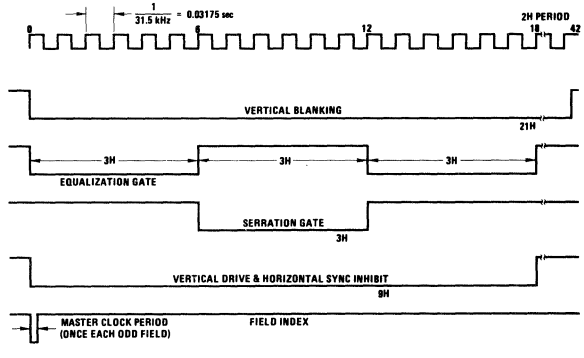


FIGURE 4. Vertical Timing

switching time waveforms (con't)

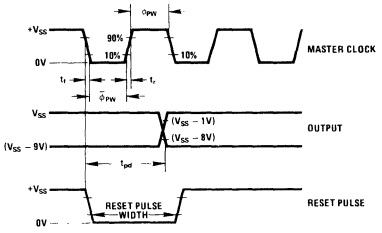
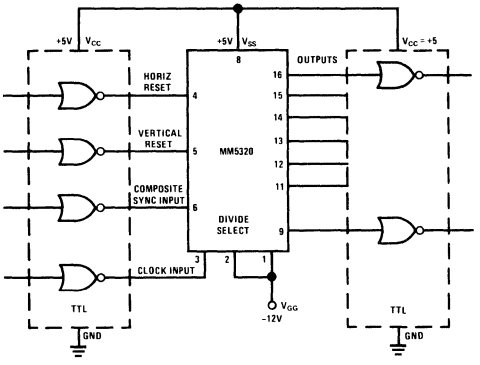


FIGURE 5.

typical application



TTL Interface

Complex Standards

MM5370, MM5371 digital alarm clocks

general description

The MM5370 and MM5371 digital alarm clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. They provide all the logic required to build several types of clocks and timers. Three display modes (time, alarm and sleep) are provided to optimize circuit utility. The circuits interface simply with 7-segment gas discharge displays. The timekeeping function operates from either a 60 Hz (MM5370) or 50 Hz (MM5371) input, and the display format may be either 12 hours (with leading-zero blanking and AM/PM indication) or 24 hours. Outputs consist of display drives, alarm enable and sleep (e.g., timed radio turn-off). Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. The devices operate over a power supply range of 8.0 to 29V and do not require a regulated power supply. These clocks are packaged in 28-pin DIP.

features

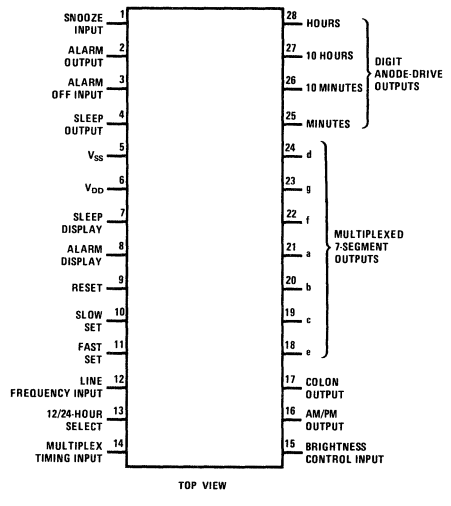
- 50 or 60 Hz operation
- Single power supply
- Low power dissipation
- 12 or 24-hour display format
- Colon drive output
- AM/PM drive output in 12-hour format
- Leading-zero blanking in 12-hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Brightness control capability
- Simple interface to gas discharge displays
- Elimination of illegal time display at turn-on
- Presettable 59-minute sleep timer
- 9-minute snooze timer

applications

- Alarm clocks
- Desk clocks
- Clock/radios
- Automobile clocks
- Industrial clocks
- Military clocks
- Appliance timers

connection diagram

Dual-In-Line Package



Order Number MM5370D
or MM5371D
See Package 7
Order Number MM5370N
or MM5311N
See Package 19

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 29V
Voltage at Any Display Output Pin	V_{SS} + 0.3V to V_{SS} − 55V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 0V, V_{DD} = −21V to −29V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage		−8.0	−25	−29	V
Power Supply Current	No Output Loads			5.0	mA
60 Hz (or 50 Hz) Input					
Frequency MM5370		dc	60	30k	Hz
Frequency MM5371		dc	50	30k	Hz
Voltage					
Logical High Level		V_{SS} − 1.0		V_{SS}	V
Logical Low Level		V_{DD}		V_{DD} + 1.0	V
Brightness Control Voltage					
Logical High Level		V_{SS} − 2.0		V_{SS}	V
Logical Low Level		V_{DD}		V_{SS} − 4.0	V
All Other Input Voltages					
Logical High Level		V_{SS} − 1.0		V_{SS}	V
Logical Low Level	Internal 2.5 MΩ resistor to V_{DD}	V_{DD}		V_{DD} + 2.0	V
Multiplex Frequency	Determined by Ext. RC	dc	6.0	60	kHz
Power Failure Detect Voltage	(V_{DD} Voltage)	0	−3.0	−8.0	V
Output Currents	V_{DD} = −21V to −29V, V_{SS} = 0V				
Digit Anode Outputs					
Logical High Level (on)	V_{OH} = V_{SS} − 5.0V	8.0			mA
Logical Low Level (off)	V_{OL} = V_{SS} − 45V			40	μA
Segment Cathode Outputs					
Logical High Level (off)	V_{OH} = V_{SS} − 5.0V	2.0			mA
Logical Low Level (on)	V_{OL} = V_{SS} − 45V			10	μA
Alarm and Sleep Outputs					
Logical High Level (on)	V_{OH} = V_{SS} − 2.0V	1.5			mA
Logical Low Level (off)	V_{OL} = V_{DD} + 2.0V	−10			μA

10

functional description

A block diagram of the MM5370 and MM5371 clocks is shown in Figure 1. The various display modes provided by these clocks are listed in Table I. The functions of the controls are listed in Table II. A connection diagram for these devices is shown on page 1. Unless indicated otherwise, the following discussions are based on Figure 1.

Line Frequency Input (pin 12): A shaping circuit is provided to square the 60 Hz (MM5370) or 50 Hz (MM5371) input. This circuit allows use of a sinewave input. The Schmitt trigger shaper (Figure 2) is designed to provide approximately 6V of hysteresis. A simple RC filter, such as shown in Figure 8, should be used to remove possible line-voltage transients that could cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the timekeeping function. A prescale counter divides the line input frequency to obtain a 1-pps timebase.

Display Mode Select Inputs (pins 7 and 8): In the absence of either of these inputs, the display drivers output time-of-day information to the display. Internal 2.5 MΩ pull-down (to V_{DD}) resistors allow use of simple SPST switches for

functional description (con't)

connecting these inputs to V_{SS}, thereby selecting alternate display modes. If more than one mode is simultaneously selected, the priorities are as noted in Table I. As shown in Figure 1 the multiplexed code converter receives time, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the multiplexed code converter inputs and ultimately (via output drivers) to the display.

Time Setting Inputs (pins 10 and 11): Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal 2.5 MΩ pull-down resistors are provided; application of V_{SS} to these pins effects the control functions. Note that the control functions proper are determined by the selected display mode. An optional hold-time control function can be obtained as shown in Figure 8.

Reset Input (pin 9): Applying V_{SS} to this input results in resetting the timekeeping function of the clock; a 2.5 MΩ pull-down resistor is provided at this input. Time is reset to 12:00 AM in the 12-hour format, or 00:00 in the 24-hour format. See Table II.

12 or 24-Hour Select Input (pin 13): By leaving this pin unconnected, the clock is programmed to provide a 12-hour display format. This format provides for zero-blanking the most significant display digit (ten's of hours). An internal 2.5 MΩ pull-down resistor is again provided; connecting this pin to V_{SS} programs the 24-hour display format.

Output Multiplexer Operation: Depending upon the selected display mode (see Table I), outputs from the appropriate internal counter are time division multiplexed to provide digit-sequential access to the data. Thus, instead of requiring 28 leads to interconnect a four-digit clock and its display (7-segments per digit), only 11 output leads are required. Note that the MM5370 and MM5371 actually provide 13 outputs (4 digit-anode drive outputs plus 9 "segment" cathode drive outputs). The two additional "segment" drives are provided to accommodate displays which feature a colon and/or AM/PM indication. The colon output is switched at a 1-Hz rate to provide a blinking colon as a short-time indication that the clock is operating. The multiplexed code converter and output drivers are controlled by a multiplex oscillator. The oscillator and external timing components set the frequency of the multiplexing function. Each digit anode is sequentially enabled for a time equal to the period of one cycle of the multiplex oscillator frequency.

When driving gas discharge displays which enclose more than one digit in a common gas envelope, it is necessary to either (1) inhibit the segment drive voltage(s) for a short time during inter-digit transitions, or (2) avoid physically adjacent inter-digit transitions. The MM5370 and MM5371 clocks utilize an interlaced output sequence to eliminate the need for inter-digit blanking circuitry and to prevent display arcing problems. The digit sequence is: (1) digit no. 1 (ten's of hours), (2) digit no. 3 (ten's of minutes), (3) blank for one digit time, (4) digit no. 2 (unit hours), (5) digit no. 4 (unit minutes), (6) blank for one digit time, etc. The two blanking intervals are provided to recharge level-translating capacitors located in the display segment drive lines (see Figure 8). Both segment data and digit enables are blanked. Figure 3 is a timing diagram which illustrates output timing.

Multiplex Timing Input (pin 14): The multiplex oscillator is shown in Figure 4. Adding an external resistor and capacitor to this circuit via the multiplex timing input produces a relaxation oscillator. The waveform at this input is a quasi-sawtooth that is squared by the shaping action of the Schmitt trigger in Figure 4. Figure 5 provides guidelines for selecting the external components relative to the desired multiplex frequency. Figure 6 illustrates a method of synchronizing or driving the multiplex oscillator with an external timebase. The external RC timing components may be omitted and this input driven by an external timebase; the required logic levels are the same as the 60 Hz or 50 Hz input.

Output Circuits: All display output drivers are open-drain devices with sources common to V_{SS} (pin 5) see Figure 7. Figure 8 illustrates interfacing the clock outputs and a gas discharge display.

Brightness Control Input (pin 15): Since display brightness is a function of cathode segment current, a capability of interrupting this current for a variable precentage of the digit interval results in a brightness control. Connecting this Schmitt trigger input (see Figure 2) to V_{DD} places all cathode segment drive voltages at the high level, thereby inhibiting the display. Conversely, V_{SS} applied to this input enables the cathode segment drives. The Schmitt trigger shaper provides approximately one volt of hysteresis, which facilitates using a waveform such as a sawtooth with a variable slope (or variable dc component) to effect the shaper output duty cycle and, therefore, the display brightness. The control waveform should be derived from the multiplex frequency; a circuit is included in Figure 8.

Alarm Operation and Output (pin 2): An alarm comparator (see Figure 1) senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. This latch enables the alarm output driver (see Figure 7), the output of which is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during

functional description (con't)

which the alarm will sound if the latch output is not temporarily inhibited by another latch set by the snooze input (pin 1) or reset by the alarm off input (pin 3). Alarm time setting and resetting are outlined in Table II.

Alarm Off Input (pin 3): Momentarily connecting this pin to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal resistor. The momentary alarm off input also readies the alarm latch for the next alarm comparator output; the alarm will sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm input should remain at V_{SS}.

Snooze Timer Input (pin 1): Momentarily connecting this pin to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled to V_{DD} by an internal 2.5 MΩ resistor. The snooze feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Sleep Timer and Output (pin 4): The sleep output at pin 4 can be used to turn off a radio (or other appliance) after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (see Table I) and setting the desired time interval (see Table II). This automatically results in a current-source output via pin 4 which can be used to turn on a radio. When the sleep counter, which counts downwards, reaches 00 minutes a latch is reset and the sleep output drive current is removed, thereby turning off the radio. This turn-off also may be manually controlled (at any time in the count-down) by a momentary V_{SS} connection to the snooze input (pin 1). This input is also returned to V_{DD} by 2.5 MΩ. The output circuitry is the same as the alarm output (see Figure 7).

AM/PM Cathode Output (pin 16): Current with this writing, gas-discharge clock displays are available with two types of AM/PM indications, (1) AM and PM indicators common to digits three and four, respectively; and (2) a PM-only indication common to digit one. Figure 3 illustrates an AM/PM cathode drive output that is compatible with both display types. Note that this same output also provides a non-blinking (steady) colon drive common to digit two.

Colon Cathode Output (pin 17): As an optional indication of clock operation, some users may prefer to display a 1-Hz activity. As shown in Figure 3, a cathode drive output is provided to facilitate a blinking colon.

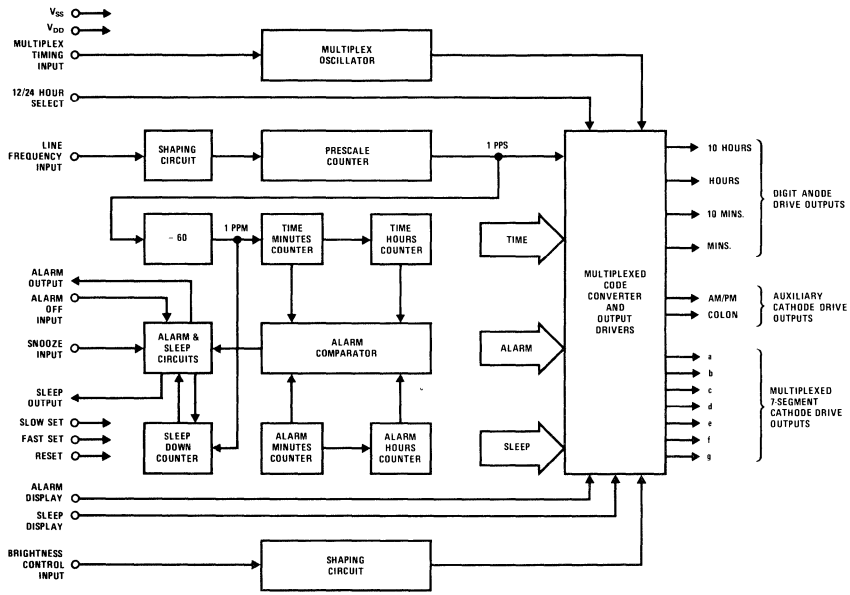


FIGURE 1. MM5370 and MM5371 Digital Alarm Clock, Block Diagram

functional description (con't)

TABLE I. MM5370 and MM5371 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time	10's of Hours	Unit Hours	10's of Minutes	Unit Minutes
Alarm	10's of Hours	Unit Hours	10's of Minutes	Unit Minutes
Sleep	Blanked	Blanked	10's of Minutes	Unit Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

Table II. MM5370 and MM5371 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
Time*	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
	Reset	Time Resets to 12:00 AM (12-hour format)
	Reset	Time Resets to 00:00 (24-hour format)
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 00:00 (24-hour format)
Sleep	Slow	Subtracts Count at 2 Hz Rate
	Fast	Subtracts Count at 60 Hz Rate
	Both	Subtracts Count at 60 Hz Rate

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

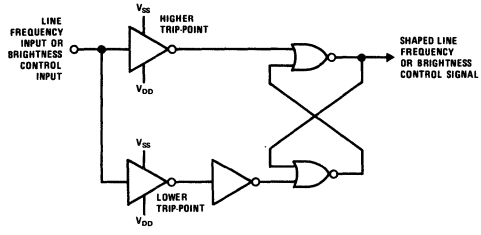


FIGURE 2. 60 Hz (or 50 Hz) Input (or Brightness Control Input) Shaping Circuit

functional description (con't)

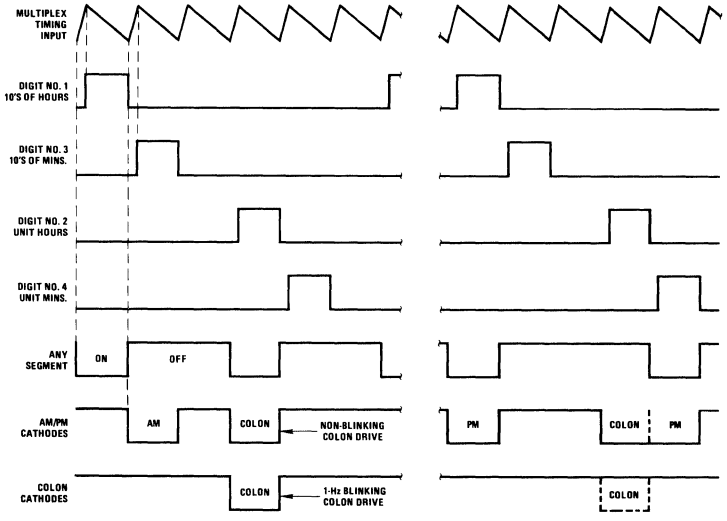


FIGURE 3. Output Timing Diagram

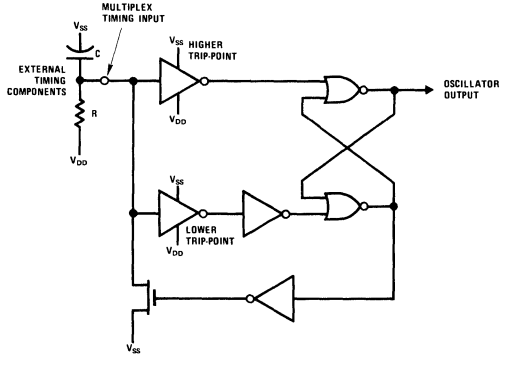


FIGURE 4. Multiplex Oscillator Circuit

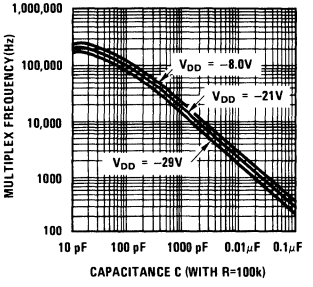
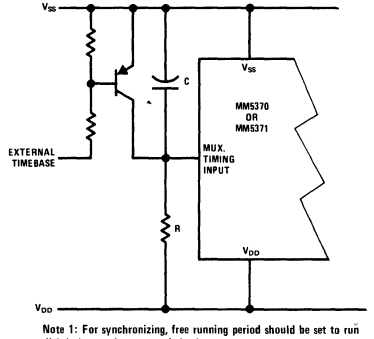


FIGURE 5. Multiplex Timing Component-Selection Guide



Note 1: For synchronizing, free running period should be set to run slightly longer than external timebase over temperature.

Note 2: For driving, timing capacitor should be deleted.

FIGURE 6. Synchronizing or Driving Multiplex Oscillator

functional description (con't)

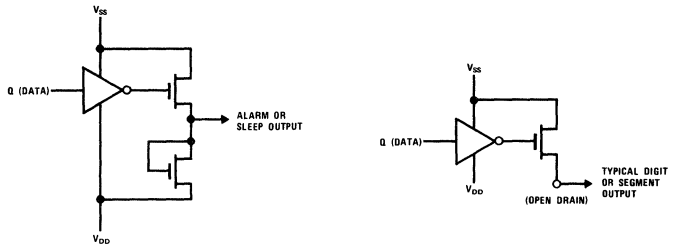


FIGURE 7. Output Circuits

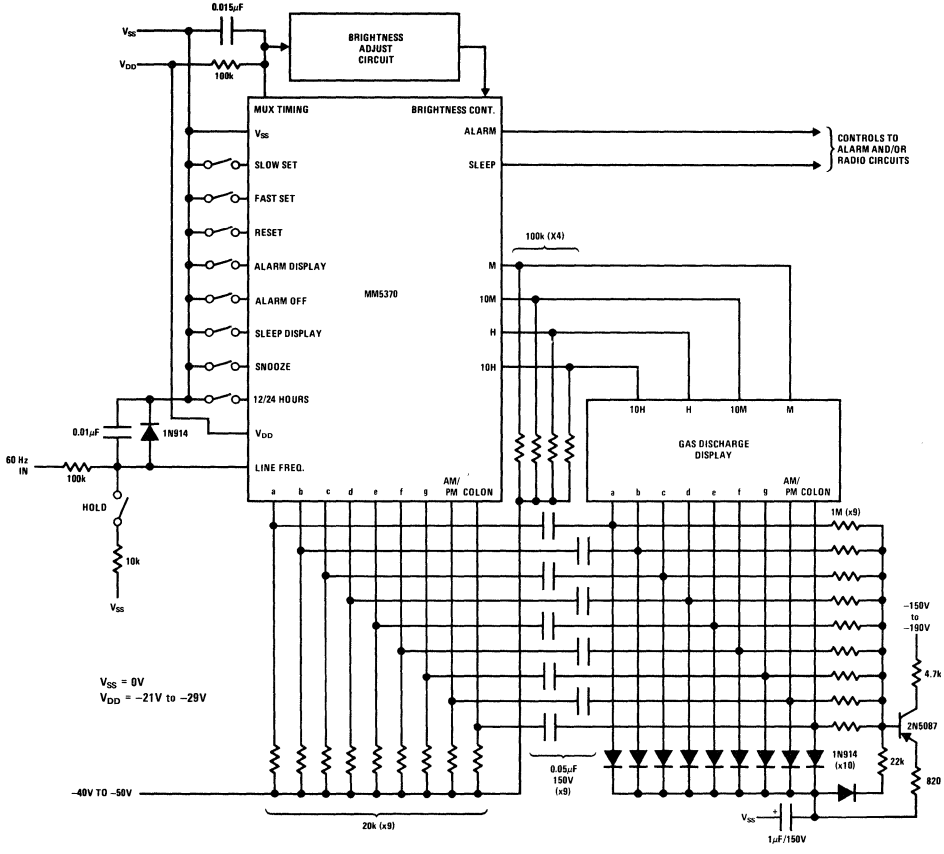


FIGURE 8. Typical Application

Complex Standards

MM5375AA/MM5375AB/MM5375AC/ MM5375AD/MM5375AE digital alarm clock

general description

The MM5375 digital alarm clock is a monolithic MOS integrated circuit utilizing p-channel low threshold, enhancement mode and ion-implanted depletion mode devices. It provides all the logic to give a four or six digit twelve or twenty-four hour display from a 50 or 60 Hz input. Inputs include time setting, 60 Hz input, display brightness control, alarm set, snooze, alarm off, and multiplex oscillator frequency control. Outputs consist of 8-segment selects (eighth segment for AM/PM and colon indications), digit enables, and alarm signal consisting of a 500 Hz to 1,000 Hz, squarewave (frequency externally adjustable) gated on and off at a 2.0 Hz rate. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication.

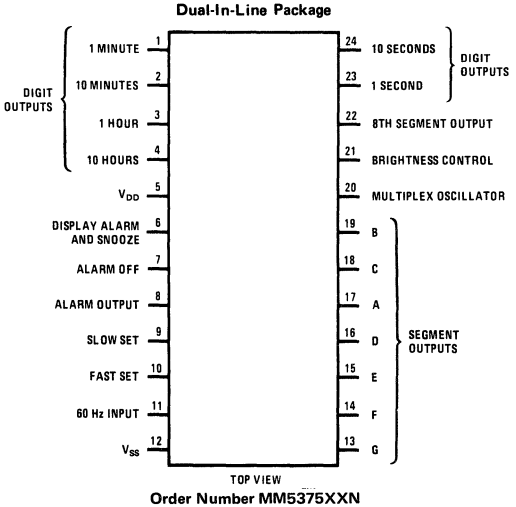
features

- 50/60 Hz operation
- Single power supply
- Low power dissipation
- 12/24 hour display format
- AM/PM indication
- Calendar register option
- Elapsed time register option
- 24-hour alarm setting
- All counters resetable
- Fast and slow set controls
- Power failure indication
- Brightness control capability
- No illegal time display at turn-on
- Alarm tone output
- Simple interface to gas-discharge displays and LED's
- 6 to 8 minute snooze alarm
- Internal digit multiplex oscillator
- Leading zero blanking
- Activity indicator
- 4 or 6 digit operation

applications

- Alarm clocks
- Desk clocks
- Automobile clocks
- Industrial clocks
- Military clocks

connection diagram



Order Number MM5375XXN
See Package 18

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 29V
Voltage at Any Display Output Pin	V_{SS} + 0.3V to V_{SS} − 55V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 0V, V_{DD} = −21V to −29V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply					
Voltage (V_{DD})	Excluding Outputs	−8.0	−25	−29	V
Voltage (V_{DD})	Outputs Driving Displays	−21	−25	−29	V
Current	Excluding Outputs		2.5	8.0	mA
60 Hz Input					
Frequency		DC	60	30k	Hz
Logic High		V_{SS}−1.0		V_{SS}	V
Logic Low		V_{DD}	V_{DD}	V_{DD}+1.0	V
Brightness Control Range % of Digit Time	Determined by External R and C	0	75	95	%
Multiplex Oscillator Frequency Input	Determined by External R and C	DC	6.0	30	kHz
All Other Input Voltages					
Logical High Level		V_{SS}−1.0		V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+2.0	V
Power Failure Detect Voltage	(V_{DD} Voltage)	0	−3.0	−8.0	V
Output Current	V_{DD} = −21V to −29V				
Digit Select Outputs	V_{SS} = 0V				
Logic High	V_{OH} = V_{SS} − 5.0V	8.0			mA
Logic Low	V_{OL} = V_{SS} − 45V			40	μA
Segment Outputs					
Logic High	V_{OH} = V_{SS} − 5.0V	2.0			mA
Logic Low	V_{OL} = V_{SS} − 45V			10	μA
Alarm Output					
Logic High	V_{OH} = V_{SS} − 2.0V	1.5			mA
Logic Low	V_{OL} = V_{DD} + 2.0V	−0.1			μA

functional description

A block diagram of the MM5375 series of alarm clocks is shown in Figure 1. The two display modes are listed in Table I. The functions of the setting controls are listed in Table II. The following discussions are based on Figure 1.

60 Hz Input (Pin 11): A shaping circuit is provided to square the 60 Hz input (50 Hz optional). This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 3.0V of hysteresis. The shaper output drives a counter chain which performs the timekeeping function.

Time Setting Inputs (Pins 9 and 10): The time-setting control functions are affected by the application of V_{SS} to these two pins, which are internally pulled to the power supply. Activating Fast Set (pin 10) causes the minutes counter to advance at a 60 Hz rate, thus clocking the hours counter at a rate of 1 hour per second. Slow Set (pin 9) advances the minutes counter at a rate of 2 minutes/second. Activating either Fast Set or Slow Set resets the seconds counter to zero. When Fast Set and Slow Set are activated simultaneously, all counters are reset to 12:00 p.m. and remain in that count until Slow Set is deactivated. The two time setting inputs affect only the counters that are displayed (either the time keeping counters or the alarm counters).

functional description (con't)

8 Segment Test (Pin 24): For testing purposes, all eight segment output lines may be activated by connecting pin 24 (S10 digit output) to V_{SS}.

Brightness Control (Pin 21): Brightness of the display may be varied by use of an external time constant. This time constant is used in the integrated circuit to control the pulse width or duty cycle of the six digit enable outputs. See Figure 2.

Activity Indication (Pin 23): When all six digits are being used, it is not necessary to blink the colon to indicate operation of the clock, because the seconds digits provide this information. When only four digits are in use, the S1 digit (pin 23) may be connected to V_{SS}. In this case, the colon flashes at a 1.0 Hz rate.

Multiplex Frequency (Pin 20): Applying an external time constant to this pin allows the multiplex frequency to be adjusted. See Figure 2.

Alarm Off (Pin 7): Whenever the Alarm Off pin is connected to V_{SS}, the alarm will not be activated. If this pin is left open, whenever the minutes and hours counters reach the count to which the alarm has been set, the alarm will be activated. The alarm signal consists of a tone (1/6 of multiplex oscillator frequency) of from 500 Hz to 1,000 Hz, which is gated on and off at a 2.0 Hz rate (constant on optional), the frequency of this tone is externally adjustable by varying the time constant to the multiplex oscillator (pin 20). The alarm will remain activated until the Alarm Off input is again connected to V_{SS}.

Alarm Set and Snooze (Pin 6): Whenever this pin is connected to V_{SS}, the alarm time will be displayed, and the alarm time may be advanced by use of the hours set and minutes set inputs as mentioned above. This pin must be left open to allow time to be displayed (or set). If the alarm output signal is activated, and this pin is momentarily connected to V_{SS}, the alarm signal will be interrupted for a period of 6 to 8 minutes.

Power Failure Indication: If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of clock, the AM or PM and colon indicator will flash at a 2.0 Hz rate. If power drops completely, the clock will reset itself (on resumption of power) to a legal state, and the AM or PM and colon indicators will flash at a 2.0 Hz rate. In addition to the flashing AM or PM and colon indicator, if a power failure occurs when alarm off (pin 7) is at V_{DD} (logic 0), the alarm output will be activated (nonactivated optional). A logic 1 (V_{SS}) on pin 7 will deactivate the alarm signal.

8 Segment Outputs (Pins 13 – 19 and 22): These outputs contain multiplexed information for the display of seven segment numerical readouts. The eighth segment is for the activation of AM/PM and colon(s) as included in the Gas Discharge displays for which these outputs are designed.

Digit Enable Outputs (Pins 1 – 4 and 23 and 24): These outputs are used to select the six digits and are synchronized with the segment outputs. If pin 23 is grounded, segment outputs will be blanked during the scanning of the seconds digits.

AM/PM Operation: AM or PM indication is obtained through the use of the eighth segment output (pin 22). The indicators are integral to the Gas Discharge Display. AM and PM indication is provided only during setting operations and alarm display (continuous display optional).

TABLE I. Display Modes

SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4	DIGIT NO. 5	DIGIT NO. 6
Time Display	10's of Hours	Units Hours	10's of Mins.	Units Mins.	10's of Secs.	Units Secs.
Alarm Display	10's of Hours	Units Hours	10's of Mins.	Units Mins.	0	0

TABLE II. Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
Time Display	Slow	Minutes advance at 2.0 Hz rate and seconds are held in a reset (00) condition.
	Fast	Minutes advance at 60 Hz rate and seconds are held in a reset (00) condition.
	Both	Time resets to 12:00 p.m.
Alarm Display	Slow	Alarm minutes advance at a 2.0 Hz rate.
	Fast	Alarm minutes advance at a 60 Hz rate.
	Both	Alarm resets to 12:00 p.m.

programmable options

PROGRAMMABLE OPTIONS		PART #				
FEATURE	OPTION	AA	AB	AC	AD	AE
Input Frequency	60 Hz	X	X		X	X
	50 Hz			X		
Time Display	12 hour	X	X		X	
	24 hour			X		X
Duplicate Register	Alarm Counter	X	X			
	Date Counter			X		
	Minute Timer				X	
	Second Timer					X
Alarm Signal	Tone	X	X			X
	DC Level			X	X	
Alarm Output	Modulated @ 2.0 Hz	X	X		X	X
	Not Modulated			X		
Alarm at Power Failure	ON	X	X			
	OFF			X	X	X
Segment Output Polarity	V_{SS} for Display		X		X	
	V_{DD} for Display	X		X		X
AM or PM Indication	Off during time display	X	X			
	Displayed at all times			X	X	X

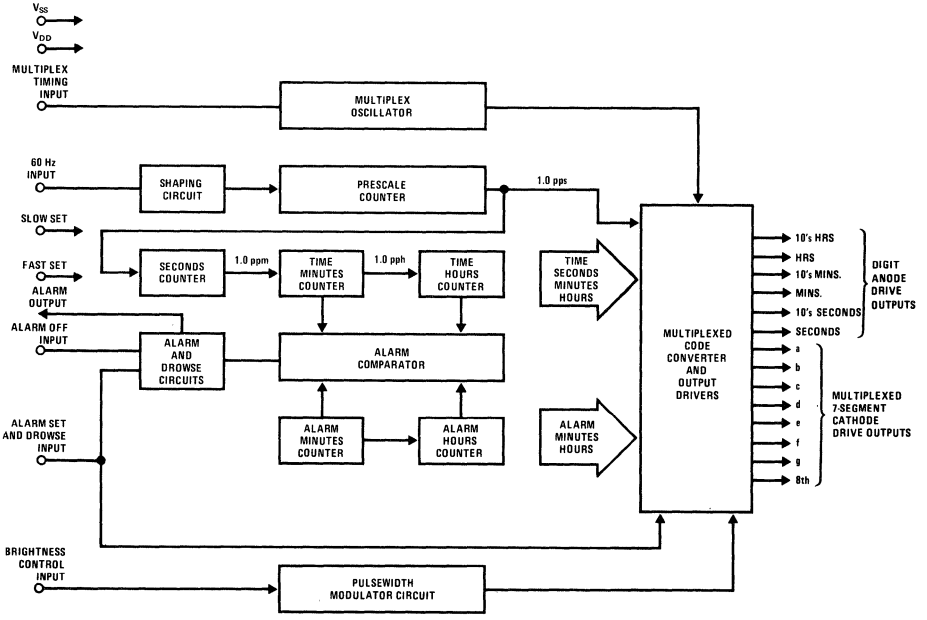


FIGURE 1. Block Diagram

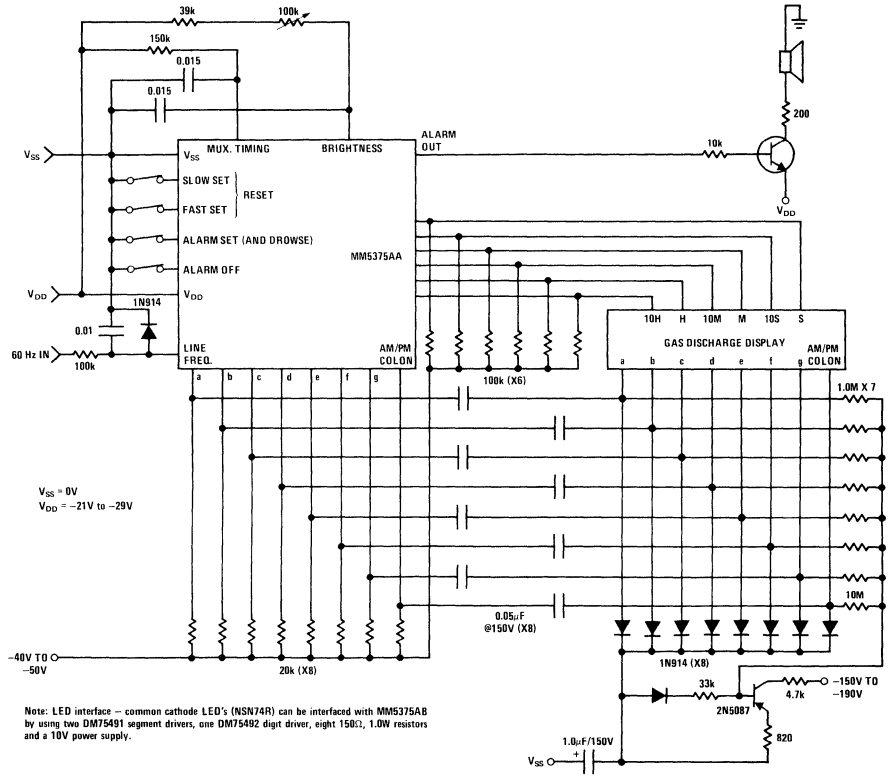


FIGURE 2. Typical Application

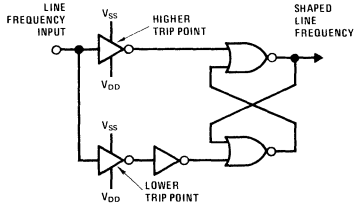


FIGURE 3. 60 Hz Shaping Circuit

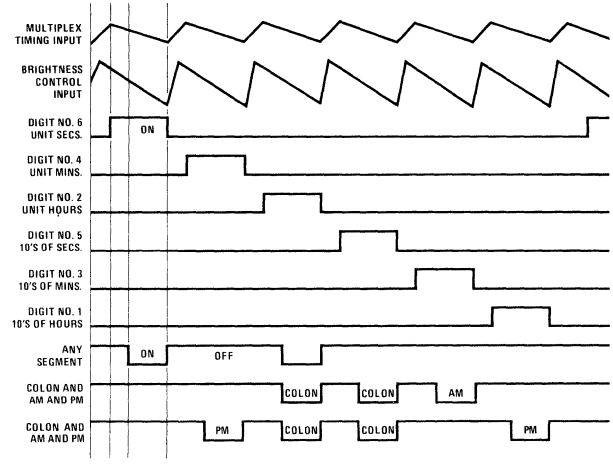


FIGURE 4. Output Timing Diagram

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Complex Standards

MM5554 frequency divider

general description

The MM5554 frequency divider provides six stages of binary division to produce six octave-related outputs of an electronic musical instrument tone generator. Each divider stage consists of an asynchronous, DC-coupled flip-flop. The six stages are internally connected in cascades of one, two, and three flip-flops. Each flip-flop drives a push-pull output buffer, which provides low output impedance in both logic states. Two of the internal cascades also provide trigger outputs for use in cascading the divider stages. The timing diagram shown results from connecting the same input trigger to all three inputs.

The MM5554 complements the MM5555/MM5556 chromatic frequency generator; output characteristics and power supply requirements are compatible. The MM5554 is packaged in a 14-lead dual-in-line package.

features

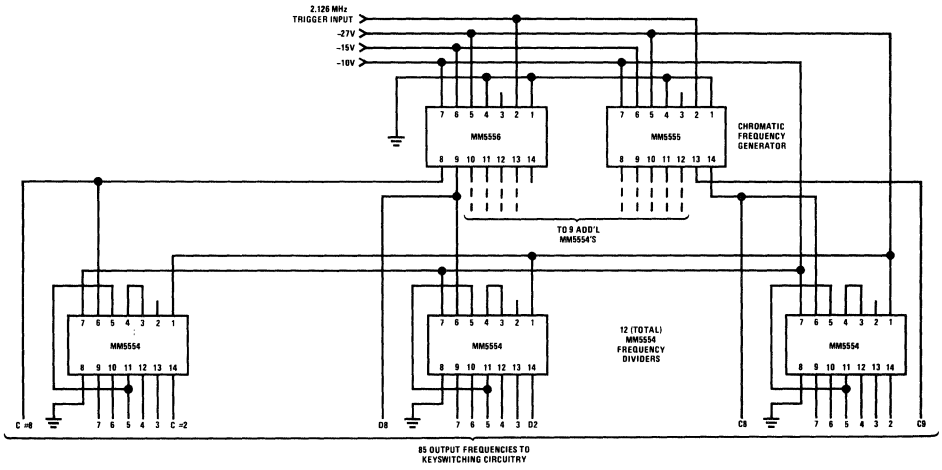
- 0 to 500 kHz toggle frequency
- 1–, 2–, 3–stage partitioning

applications

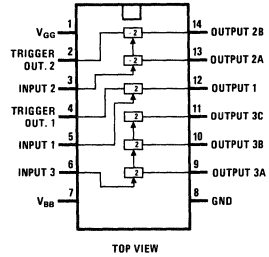
- Electronic organs
- Electronic music synthesizers
- Musical instrument tuners

logic and connection diagrams

Typical Organ Tone Generator



Dual-In-Line Package



Order Number MM5554N
See Package 14

absolute maximum ratings

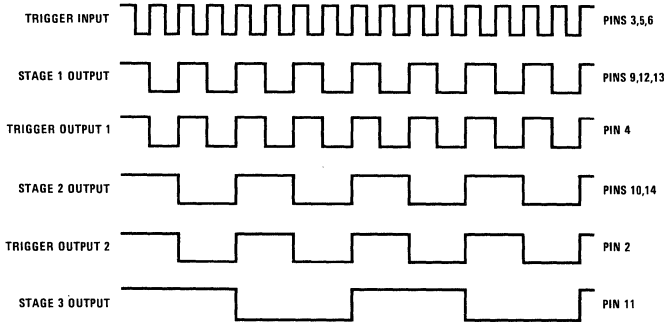
	SYMBOL	MIN	MAX	UNITS
Logic Supply Voltage	V_{GG}	+0.3	-33	V
Buffer Supply Voltage	V_{BB}	+0.3	-18	V
Trigger Input Voltage	V_{IT}	+0.3	-18	V
Power Dissipation	P_D		250	mW
Storage Temperature	T_S	-55	+100	°C
Operating Temperature	T_A	0	+70	°C

electrical characteristics

T_A within operating range (V_{GG} = -27 ±2V, V_{BB} = -10 ± .5V), unless otherwise noted.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Inputs:					
Frequency	f_{IT}	DC		500	kHz
Rise and Fall Times (10% to 90%)	t_r, t_f			25	μs
Pulse Width (at 90%)	pw	1			μs
Logical High Level	V_{ITH}	+0.3	0	-2.5	V
Logical Low Level	V_{ITL}	- 7.0	-10	-18	V
Leakage Current @ V_{ITL} = -18V	I_{ITL}			1.0	μA
Trigger Outputs: (loaded 10M ohm to ground, T_A = 25°C)					
Logical High Level	V_{OTH}	0		-1.5	V
Logical Low Level	V_{OTL}	-10			V
Outputs: (loaded 20K ohm to ground and 20K ohm to V_{BB}, T_A = 25°C)					
Logical High Level	V_{OH}	0		-1.0	V
Logical Low Level	V_{OL}	-8.0		V_{BB}	V
Supply Currents: (no output loads, T_A = 25°C)					
Logic Supply	I_{GG}		2	4	mA
Buffer Supply	I_{BB}			20	μA

timing diagram



Complex Standards

MM5555, MM5556 chromatic frequency generators

general description

The National Semiconductor MM5555, MM5556 chromatic frequency generators are MOS/LSI frequency synthesizers designed to generate musical frequencies. The circuits provide thirteen semitone outputs, fully spanning the equal tempered octave. The divisors have been carefully selected to offer excellent tuning accuracy and to eliminate any "locked" (just-intoned) fifths. Output characteristics are fully compatible with the MM5554 Frequency Divider. The MM5555 or MM5556 is packaged in a 14-lead dual-in-line package.

features

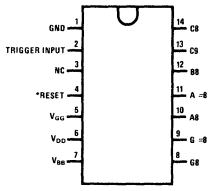
- Single-phase squarewave input
- 7 kHz to 2.2 MHz input frequency
- Accuracy of 0.5129 cent

applications

- Electronic organs
- Electronic music synthesizers
- Musical instrument tuners

connection and logic diagrams

Dual-In-Line Package

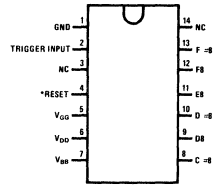


TOP VIEW

Order Number MM5555N
See Package 14

*Used only for testing. Pin 4 is normally grounded.

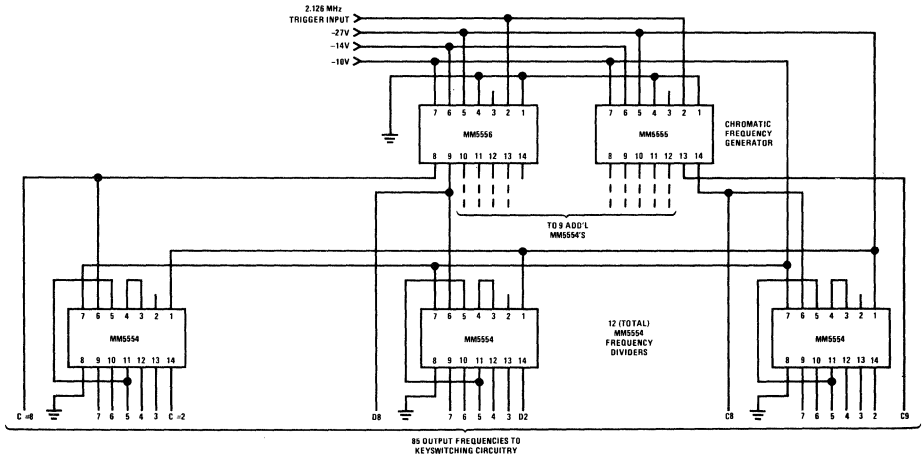
Dual-In-Line Package



TOP VIEW

Order Number MM5556N
See Package 14

Typical Organ Tone Generator



output details (2.12608–MHz input)

MM5555

NOTE	DIVISOR	OUTPUT FREQUENCY	E.T.S. FREQUENCY	CENT ERROR
C8	508	4185.20	4186.01	-0.326
C9	254	8370.39	8372.02	-0.326
B8	269	7903.64	7902.13	+0.321
A =8	285	7459.93	7458.62	+0.295
A8	302	7040.00	7040.00	0
G =8	320	6644.00	6644.88	-0.221
G8	339	6271 62	6271 93	-0.082

MM5556

NOTE	DIVISOR	OUTPUT FREQUENCY	E.T.S. FREQUENCY	CENT ERROR
F =8	359	5922.23	5919 91	+0 658
F8	380.5	5587.60	5587 65	-0.017
E8	403	5275.63	5274.04	+0.507
D =8	427	4979.11	4978.03	+0.364
D8	452.5	4698.52	4698.64	-0.042
C =8	479.5	4433.95	4434.92	-0.368

absolute maximum ratings

	SYMBOL	MIN	MAX	UNITS		SYMBOL	MIN	MAX	UNITS
Clock Generator Voltage	V_{GG}	+0.3	−33	V	Power Dissipation	P_D	–	800	mW
Logic Supply Voltage	V_{DD}	+0.3	−25	V	Storage Temperature	T_S	−55	+100	°C
Buffer Supply Voltage	V_{BB}	+0.3	−18	V	Operating Temperature	T_A	0	+70	°C
Trigger Input Voltage	V_{IT}	+0.3	−18	V					

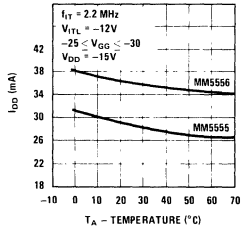
electrical characteristics

T_A within operating range (V_{GG} = −27V ±2V, V_{DD} = −14V ±1V, V_{BB} = −10V ±0.5V), unless otherwise noted.

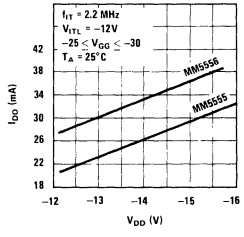
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Trigger Input					
Frequency	f_{IT}	7.0	2126.08	2200	kHz
Capacitance	C_{IT}	–	–	7.0	pF/pkg
Rise and Fall Times (10% to 90% at 2.2 MHz)	t_r, t_f	–	–	30	ns
Pulse Width (at −5.0V)	pw	0.4T	–	0.6T	$(T = \frac{1}{f_{IT}})$
Logical High Level	V_{ITH}	+0.3	0	−2.0	V
Logical Low Level	V_{ITL}	−8.0	−10	−16	V
Leakage Current	I_{ITL}	–	–	1.0	μA
Buffer Outputs: (loaded 20 kΩ to ground and 20 kΩ to V_{BB}, T_A = 25°C)					
Logical High Level	V_{OH}	0	–	−1.0	V
Logical Low Level	V_{OL}	−8.0	–	V_{BB}	V
C8 Duty Cycle	–	–	50	–	%
C #8 thru C9 Duty Cycle	–	–	30	–	%
Supply Currents: (no output loads, T_A = 25°C)					
Clock Generator Supply	I_{GG}	1.5	3.0	3.5	mA
Logic Supply MM5555	I_{DD}	16	26	34	mA
Logic Supply MM5556	I_{DD}	22	33	40	mA
Buffer Supply	I_{BB}	–	–	25	μA

typical performance characteristics

I_{DD} vs Ambient Temperature T_A



I_{DD} vs V_{DD}



Complex Standards

MM5725 one chip calculator

general description

The MM5725 is an 8-digit calculator on one MOS/LSI chip. It uses three registers to provide the four arithmetic functions (+, −, x, and ÷). The calculator has a 16-place decimal point register and self-contained oscillator and clock driver. In addition to operating the machine the internal clock provides timed key-bounce protection. Calculations are handled in floating point in both entry and result display. Results are right justified to eight significant digits in all calculations. Leading zeros are suppressed.

The 8-digit display is automatically multiplexed and presented in standard 7-segment form. Eight digit select output signals (T_1 through T_8) appear sequentially from least to most significant, while the segment outputs (S_a through S_g, and DP) provide the decoded figures and the decimal point. Minus sign indication appears on a separate line, at the same time as the least significant digit.

The eight digit select lines are also used to scan the keyboard, which is arranged as an 8 x 4 array (see Figure 2); four lines return the keyboard entries into the chip.

features

- 8 Digit multiplexed display
- Four functions (+, −, x, and ÷)
- Full floating point input
- Full floating point output
- True credit balance
- Chain calculations
- Overflow indication
- Leading zero suppression
- Trailing zero suppression in division
- Decimal point memory to 16 digits
- Seven segment decoder on chip
- On chip clock oscillator and driver
- Key-bounce elimination

key description

Clear: should be depressed twice when power is first turned on. A single zero and decimal point will then be displayed in the extreme right digit position. In all further operations, a digit will always be displayed in at least that position. During operations, the clear key combines the function of a "clear entry" and "clear accumulator." A first depression clears the display of all digits entered since the last calculation, and will restore the result of the last calculation, if any, to the display. If no prior result is present in the accumulator, a single zero without decimal point will be displayed.

A second depression will clear the accumulator and display, leaving a single zero and decimal point in the extreme right digit position.

Numerics: are entered from the right. If a previous result exists in the accumulator, it will remain in there while the first numeric entry clears it from the display, and appears in its place. At any point in the entry of the string of numerics, the user may insert a decimal point. Once a *decimal point* is entered, it remains displayed to the right of the units digit. Additional decimal point entries and any numerics after the eighth are disregarded. No overflow can result on input.

When the new number has been fully entered, an operation may be selected. The operator key (+, −, x, ÷) is selected by the user after the operands (accumulator and display) are present in the machine. The operations will now be described in detail.

Add/Enter: adds the display register to the accumulator, enters the sum into the accumulator, and displays the new accumulator content. If the accumulator was empty, it enters the displayed number into the accumulator, and continues to display the same number.

Subtract: subtracts the display register from the accumulator, stores the result in the accumulator, and displays the new accumulator content. If the new result is negative, the minus sign indicator lights, and will remain lit so long as the accumulator remains negative.

Multiply: multiplies the accumulator by the display register, stores the result in the accumulator and displays it. If the product exceeds 99,999,999, its eight most significant digits will be displayed without a decimal point. Further multiplication of the accumulator is allowable if the result will not exceed $10^{16} - 1$. If a product exceeds this value, the machine will *overflow*, lose all content, and display all zeroes with all decimal points.

Divide: divides the accumulator by the display register, stores the result in the accumulator, and displays it. If the result of a multiplication, or of a division by a number less than one, results in a display with no decimal point, the point may be located by successive division by powers of ten. (It is often convenient to divide by 1,000 to shift a result three decimal points at a time.) Unlike some less sophisticated designs, the MM5725 keeps results of divisions as far to the right in the display as possible (see division examples *b* and *c* below) and so gives indication of a result with a remainder more than eight orders of magnitude below the most significant digit in a result. The remainder is not directly retrievable.

Order Number MM5725N
See Package 19

absolute maximum ratings

Voltage at any pin except V_{GG} relative to V_{SS} (all others GND)	+0.3V to −28V
Voltage at V_{GG} pin relative to V_{SS} (all others GND)	+0.3V to −38V
Voltage at pins T_1 through T_8 relative to V_{SS} (with V_{DD} = −28V)	+0.3V to −55V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to 150°C

operating voltage range

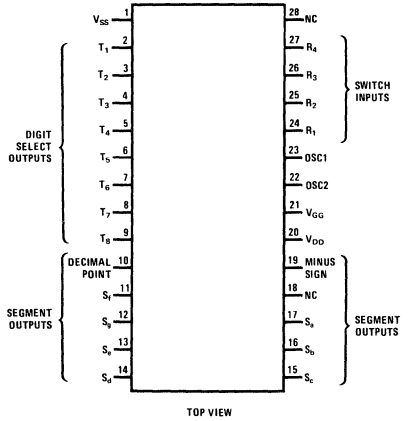
V_{SS} = 0V
V_{DD} = −28V ±7%
V_{GG} = −35V ±7%

electrical characteristics

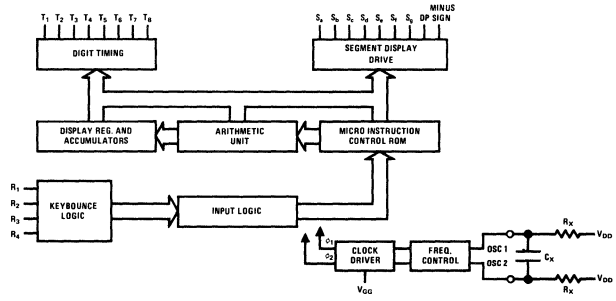
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_{DD})	V_{DD} = −28V		10.0	18.0	mA
Supply Current (I_{GG})	V_{GG} = −35V		2.0	2.7	mA
Switch Input Current (R_1 - R_4), (Internal Resistor to V_{DD})	$0 \leq V_{IN} \leq -30V$			100	μA
Digit Select Output Current (T_1 - T_8), (open drain)	V_{OUT} = −8.0V, V_{DD} = −28V	4	5		mA
Segment Output Current (S_a - S_g, MS, DP), (push-pull)	V_{OUT} = −2.0V (Segment on)	−300	−500		μA
	V_{OUT} = −10.0V (Segment off)	+300	+500		μA

connection diagram

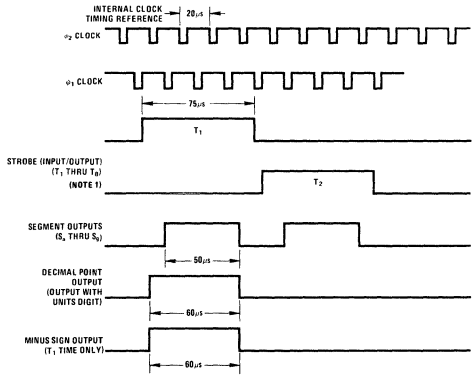
Dual-In-Line Package



calculator chip system organization



timing diagram



Note 1: Used to strobe keyboard for input conditions, and to multiplex digit outputs for display.

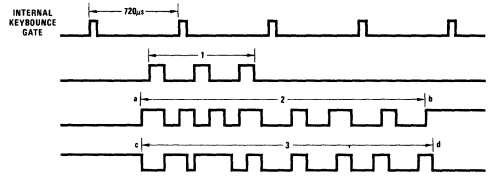
Note 2: Times shown are nominal.

keybounce protection

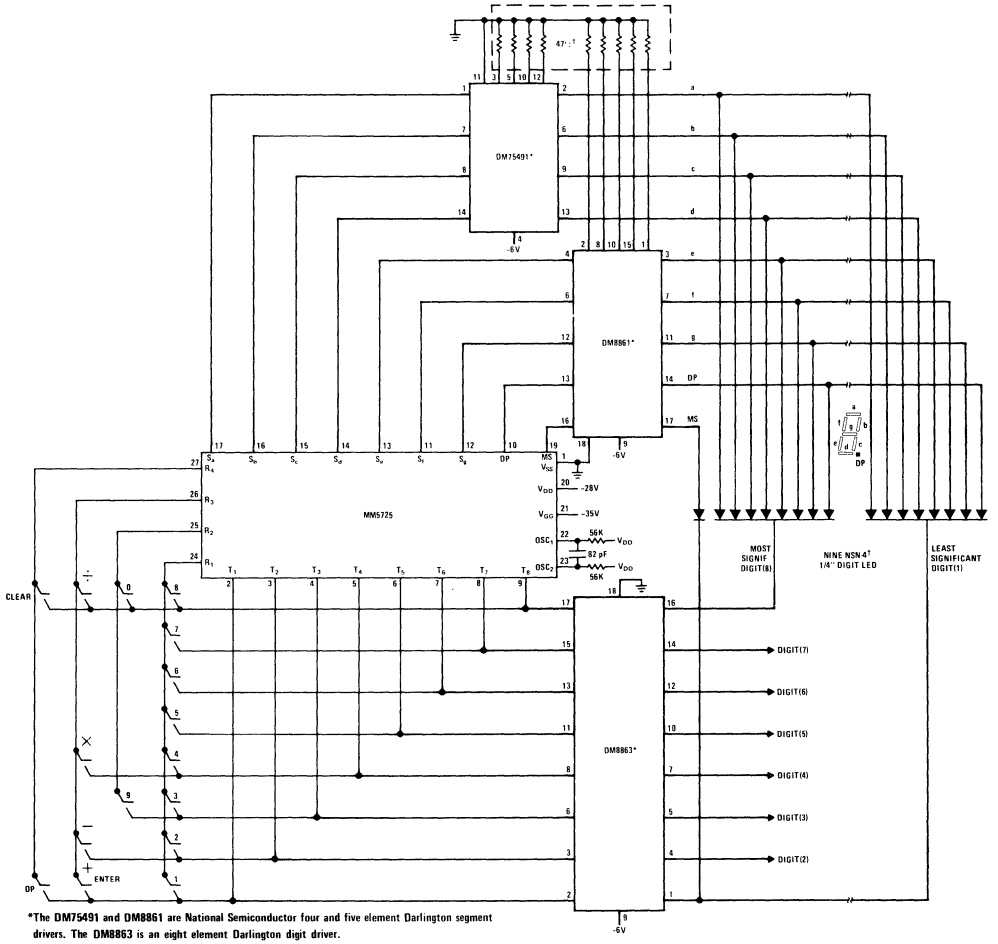
Keybounce protection in the MM5725 is ensured by a series of latches and interlocks operated from the internal clocking scheme. The protection intervals are derived from the scan period, nominally 720μs, and are shown in the table.

TABLE. Worst Acceptable Switch Characteristics

CHARACTERISTIC	SCAN PERIODS	TYPICAL TIME
Widest discrete noise burst which will not cause false data entry	1	.72 ms (1)
Longest switch bounce tolerable as switch closes	3	2.16 ms (2)
Longest switch bounce tolerable as switch opens	3	2.16 ms (3)



a. Point where switch first closes
b. Point where switch must be fully closed
c. Point where switch first opens
d. Point where switch must be fully open



*The DM75491 and DM8861 are National Semiconductor four and five element Darlington segment drivers. The DM8863 is an eight element Darlington digit driver.

†Alternatively use two NSN33 triple 1/8" digits and one NSN133 double 1/8" digit with seperate minus sign, and change resistor values to 100Ω.

FIGURE 1. Typical Application – LED Display

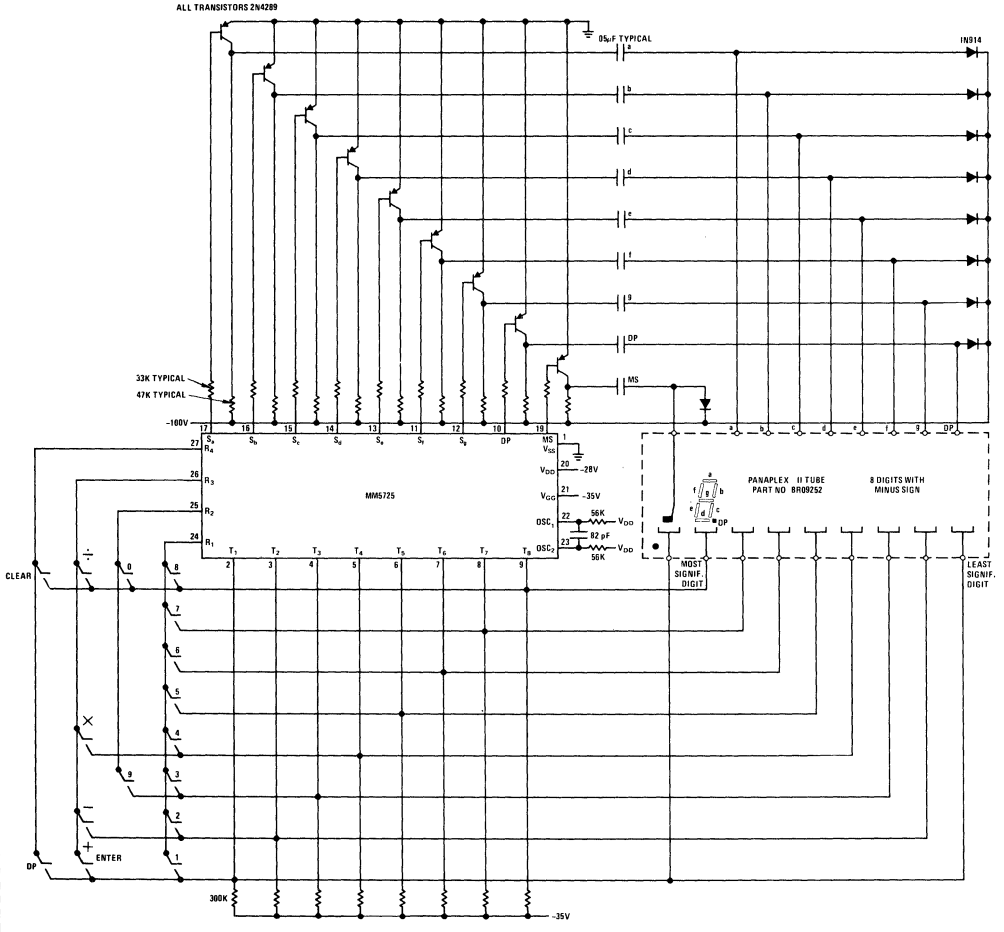


FIGURE 2. MM5725 Interface to Panaplex II* Neon Display Tube

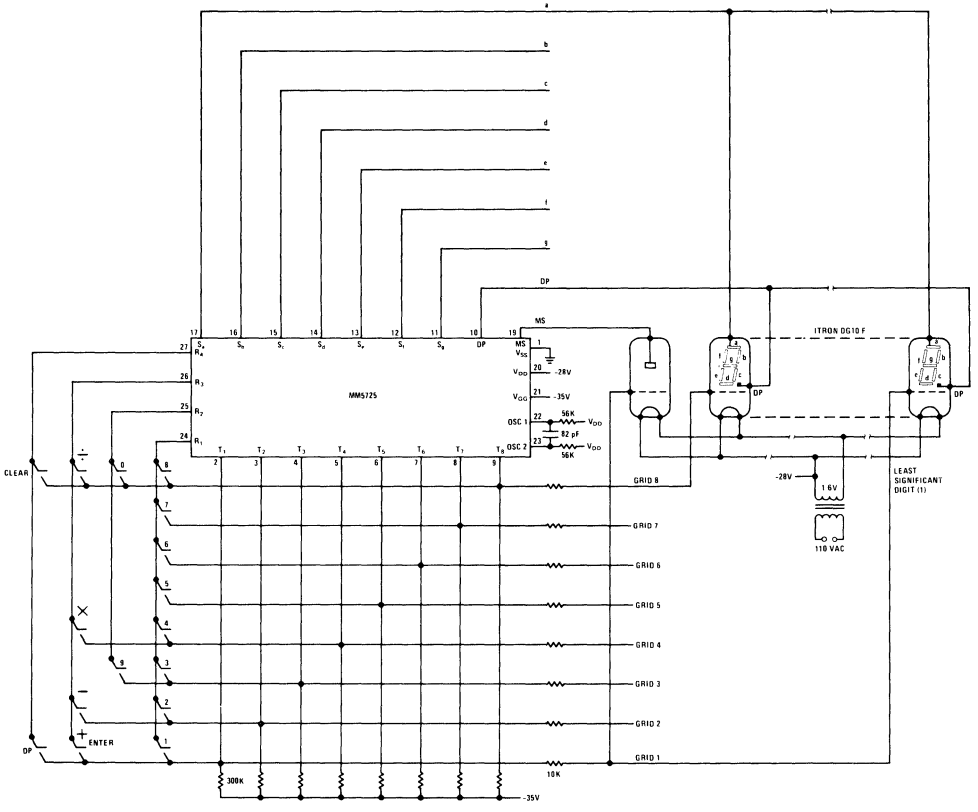
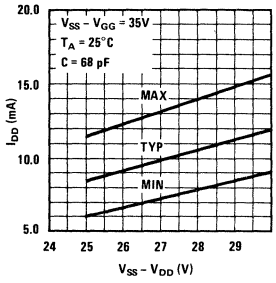


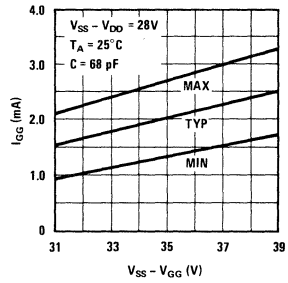
FIGURE 3. MM5725 Interface to Fluorescent Vacuum Display Tubes

performance curves

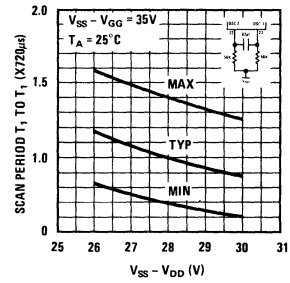
I_{DD} vs V_{DD}



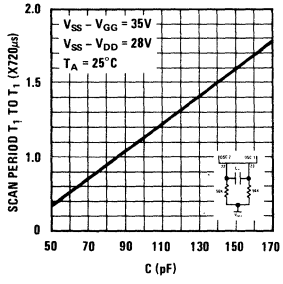
I_{GG} vs V_{GG}



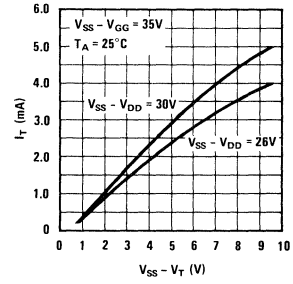
Scan Period vs V_{DD}



Typical Scan Period vs C_X



Typical Digit Current vs Digit Voltage



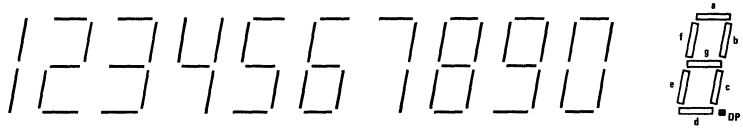


FIGURE 4. MM5725 Display Font

accounting machine notation

The MM5725 performs its arithmetic according to a logic form known as Polish notation. In this notation, as pointed out in the description on page one, the new number keyed into the machine operates on the previously accumulated result only when the operator key (+, −, x, ÷) is struck. And at that point, the result appears. There is no separate equals (=) key, as all four operator keys perform the function of generating the result of a calculation. The use of an operator key after the data entry is a very natural mode of operation in, for instance, credit balance transactions. For calculator users without previous training, as one might typically classify first-time low-cost calculator buyers, it is equally natural to extend the Polish notation to the multiply and divide operations.

Users who have been exposed to electric accounting machines, however, may be confused by this routine. Those machines usually use a hybrid notation, Polish in addition and subtraction, but algebraic in multiplication and division: for example A x B = . The MM5725 may be used in such machines by adding a key, wired in parallel to the +/Enter key, called ($\frac{X}{\div}$) and by marking the existing multiplication and division keys $\frac{X}{=}$ and $\frac{\div}{=}$.

The operation of A x B = C may now be compared

Polish Entry	"Pseudo-Hybrid" Key Caps
2	2
+/Enter	$\frac{X}{\div}$ Actually causes entry
3	3
x 6 appears	$\frac{X}{=}$ 6 appears

and E ÷ F = G_T looks like this:

8	8
+/Enter	$\frac{X}{\div}$
4	4
÷ 2 appears	$\frac{\div}{=}$ 2 appears

sample calculations

CALCULATION	KEY PROCEDURE	DISPLAY – 8	7	6	5	4	3	2	1
Entry									
Initial setting after clear operation									0.
Enter number 37.48	3								3.
	7							3	7.
	.							3	7.
	4						3	7.	4
Result	8					3	7.	4	8
Addition									
a) 3.1 + 4.11 = 7.21									0.
	3								3.
	.								3.
	1							3.	1
	+ (Enter)							3.	1
	4								4.
	.								4.
	1							4.	1
	1						4.	1	1
Result	+						7.	2	1
b) 0 + 4.11 = 4.11									0.
	4								4.
	.								4.
	1							4.	1
	1						4.	1	1
Result	+						4.	1	1
c) −7.032 + 3 = −4.032									0.
	7								7.
	.								7.
	0							7.	0
	3						7.	0	3
	2					7.	0	3	2
	−	−				7.	0	3	2
	3								3.
Result	+	−				4.	0	3	2
d) 4.0053114 + 8 = 12.005311									
Assume 4.0053114 result from previous calculation	.	4.	0	0	5	3	1	1	4
	8								8.
Result	+	1	2.	0	0	5	3	1	1
Subtraction									
a) 4 − 2.1 = 1.9									0.
	4								4.
	+ (Enter)								4.
	2								2.
	.								2.
	1							2.	1
Result	−							1.	9

sample calculations (con't)

CALCULATION	KEY PROCEDURE	DISPLAY – 8	7	6	5	4	3	2	1
b) 0 – 3.97 = –3.97									0.
	3								3.
	.								3.
	9							3.	9
	7						3.	9	7
Result	–	–					3.	9	7
c) –4.6 – 3.11 = –7.71									0.
	4								4.
	.								4.
	6							4.	6
	–	–						4.	6
	3	–							3.
	.	–							3.
	1	–						3.	1
	1	–					3.	1	1
Result	–	–					7.	7	1
Multiplication a) 4 x 5 = 20									0.
	4								4.
	+ (Enter)								4.
	5								5.
Result	x							2	0.
b) above result x 5 = 100	5								5.
Result	x						1	0	0.
c) –49.6 x 0.42 = –20.832									0.
	4								4.
	9							4	9.
	.							4	9.
	6						4	9.	6
	–	–					4	9.	6
	.	–							0.
	4	–						0.	4
	2	–					0.	4	2
Result	x				2	0.	8	3	2
d) 8765.432 x 100. = 876543.20				8	7	6	5.	4	3	2
assume first digit result from	1								1.
previous calculation	0							1	0.
	0						1	0	0.
Result	x	8	7	6	5	4	3	2	0
Division a) 4 ÷ 3 = 1.3333333									0.
	4								4.
	+ (Enter)								4.
	3								3.
Result	÷	1.	3	3	3	3	3	3	3

sample calculations (con't)

CALCULATION	KEY PROCEDURE	DISPLAY – 8 7 6 5 4 3 2 1
b) 30 ÷ 4 = 7.5		0.
	3	3.
Since no remainder beyond 5	0	3 0.
all trailing zeros suppressed	+ (Enter)	3 0.
	4	4.
Result	÷	7. 5
c) 45 ÷ 9.9999999	4	4.
= 4.5000000	5	4 5.
	+ (Enter)	4 5.
	9	9.
	.	9.
	9	9. 9
	9	9 9 9
	9	9 9 9 9
	9	9 9 9 9 9
	9	9 9 9 9 9
	9	9 9 9 9 9
	9	9. 9 9 9 9 9
Result	÷	4. 5 0 0 0 0 0
(zeros are shown when remainder exists)		
d) 42.6 ÷ 6 = 7.1		0.
	4	4.
	2	4 2.
	.	4 2.
	6	4 2. 6
	+ (Enter)	4 2. 6
	6	6.
Result	÷	7. 1
e) 527 ÷ 0.003 = 175666.66		0.
	5	5
	2	5 2
	7	5 2 7
	+ (Enter)	5 2 7
	.	0.
	0	0. 0
	0	0. 0 0
	3	0. 0 0 3
	÷	1 7 5 6 6 6. 6 6

sample calculations (con't)

CALCULATION	KEY PROCEDURE	DISPLAY – 8	7	6	5	4	3	2	1
Chain Calculation									
a) 3.7 + 4.85 – 3.49 = 5.06									0.
	3								3.
	.								3.
	7							3.	7
	+ (Enter)							3.	7
	4								4.
	.								4.
	8							4.	8
	5						4.	8	5
	+						8.	5	5
	3								3.
	.								3.
	4							3.	4
	9						3.	4	9
Result	–						5.	0	6
b) 472 x .018 + 3.1 = 11.596									0.
	4								4.
	7							4	7.
	2						4	7	2.
	+ (Enter)						4	7	2.
	.								0.
	0							0.	0
	1						0.	0	1
	8					0.	0	1	8
	x								
	=					8.	4	9	6
	3								3.
	.								3.
	1							3.	1
Result	+				1	1.	5	9	6
c) $\frac{(246 - 37.8) \times 4.5}{9} = 104.1$									0.
	2								2.
	4							2	4.
	6						2	4	6.
	+ (Enter)						2	4	6.
	3								3.
	7							3	7.
	.							3	7.
	8						3	7.	8
	–					2	0	8.	2
	4								4.
	.								4.
	5							4.	5
	x					9	3	6.	9
	9								9.
Result	÷					1	0	4.	1

sample calculations (con't)

CALCULATION	KEY PROCEDURE	DISPLAY –	8	7	6	5	4	3	2	1
d) $\frac{266475 \times 8624}{187.9} = 12230337.$					2	6	6	4	7	5.
	8									8.
Assume first number from previous result	6								8	6.
	2							8	6	2.
	4						8	6	2	4.
Note that decimal point capacity of display has been exceeded, but is stored in memory.	x		2	2	9	8	0	8	0	4
	1									1.
	8								1	8.
	7							1	8	7.
	.							1	8	7.
	9						1	8	7.	9
Result	÷		1	2	2	3	0	3	3	7.
Decimal point appears										

Complex Standards

MM5736 MOS/LSI 6 digit calculator

general description

The MM5736 employs three working registers to provide add, subtract, multiply and divide functions. It includes on-chip key debounce and interfaces directly with the keyboard matrix as shown in Figure 2 and 3. A one-of-six output provides the strobe signals necessary to enable the appropriate digit for display; segment data for each digit appears during the appropriate strobe. See Figure 1 for digit and segment timing. Leading zero blanking has been incorporated to conserve battery life. Average battery life is estimated to be between 10 and 20 hours depending upon battery quality, operating schedule and the average number of digits displayed.

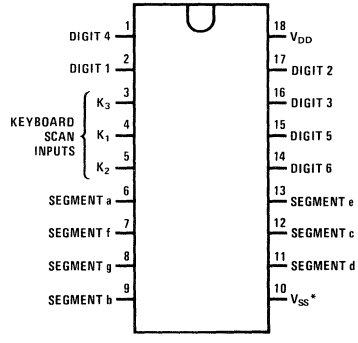
With the addition of a single-pole slide switch, a decimal point may be lit at an appropriate digit in the display; e.g., the third digit will present a dollars and cents format for users who generally use the calculator to balance checkbooks or keep track of supermarket expenditures. (Figures 2 and 3 indicate this feature using the NSN66A LED display, which has a decimal point between the second and third digits.)

features

- Six digit display
- Four functions (+, −, X, ÷)
- Chain operations
- Auto summing, convenient counting by any radix, and auto squaring
- Floating negative sign indicator for true credit balance
- Three different error indications
- Leading zero blanking
- On-chip oscillator uses no external components
- Effective keyboard bounce protection
- Interfaces with keyboard directly
- 9.0V battery operation with a typical power dissipation less than 30 mW—resulting in a battery life in excess of 15 operating hours with normal use

connection diagram

Dual-In-Line Package



TOP VIEW

*V_{SS} always most positive supply.

Order Number MM5736N
See Package 16

absolute maximum ratings

Operating Temperature	0°C to +70°C Ambient
Storage Temperature	−55°C to +150°C Ambient
Voltage on Any Pin Relative to V_{SS}	+0.3V to −12V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

$V_{SS} - 6.5V \leq V_{DD} \leq V_{SS} - 9.5V$ (V_{SS} is always the most positive potential)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$V_{DD} = V_{SS} - 9.5V$, $T_A = 25°C$		3.7	6.0	mA
Keyboard Scan Input Levels (K1, K2, K3)					
Logical High Level		$V_{SS} - 2.5$			V
Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{SS} - 5.0$	V
	$V_{DD} = V_{SS} - 9.5V$			$V_{SS} - 6.0$	V
Digit Buffer Output Levels (D1 Through D6)					
Logical High Level	$I_{OUT} = -1.2$ mA	$V_{SS} - 1.5$		V_{SS}	V
Logical Low Level	$V_{DD} = V_{SS} - 6.5V$	V_{DD}		$V_{SS} - 6.0$	V
	$V_{DD} = V_{SS} - 9.5V$	V_{DD}		$V_{SS} - 7.0$	V
Segment Output Current (Sa Through Sg)	$T_A = 25°C$				
Source Current	$V_{OUT} = V_{SS} - 3.8V$, $V_{DD} = V_{SS} - 6.5V$	−3.0			mA
	$V_{OUT} = V_{SS} - 4.2V$, $V_{DD} = V_{SS} - 7.25V$		−7.3		mA
	$V_{OUT} = V_{SS} - 7.8V$, $V_{DD} = V_{SS} - 9.5V$			−15	mA

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time (Figure 1)		0.42		1.60	ms
Digit Time (Figure 1)		70		267	μs
Interdigit Blanking Time (Figure 1)			4.0		μs
Digit Output Transition Rise and Fall Times	$C_{LOAD} = 100$ pF		2.0		μs
Keyboard Sensing Inputs (K1, K2, K3)	$C_{LOAD} = 100$ pF				
High to Low Transition Time After Key Release			4.0		μs
Key Bounce — Output Stability Time		2.8	7.0	11.4	ms
(The time a keyboard sensing input must be continuously higher than the minimum logical high level to be accepted as a key closure, or lower than the maximum logical low level to be accepted as a key release.)					

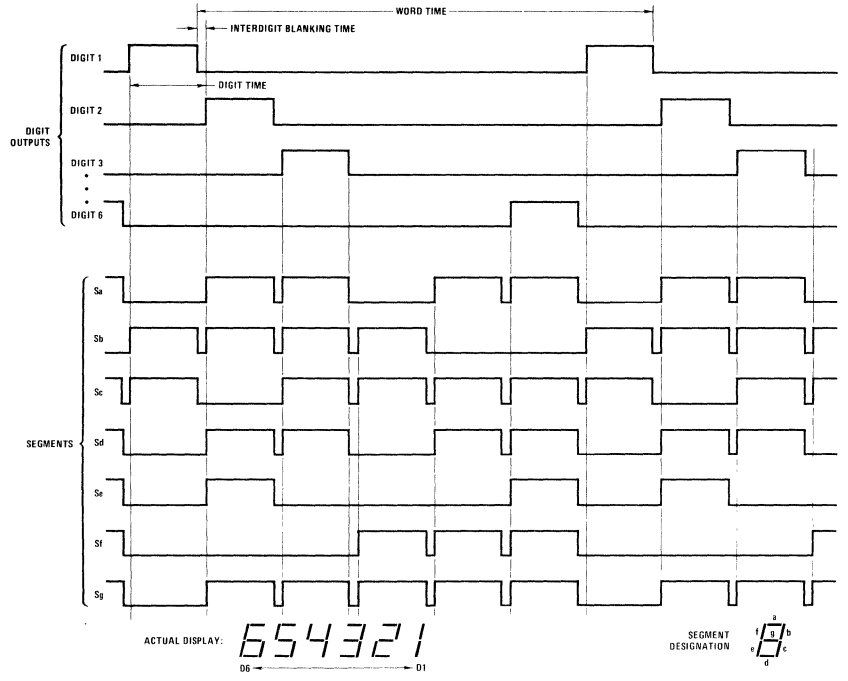


FIGURE 1. Timing Diagram

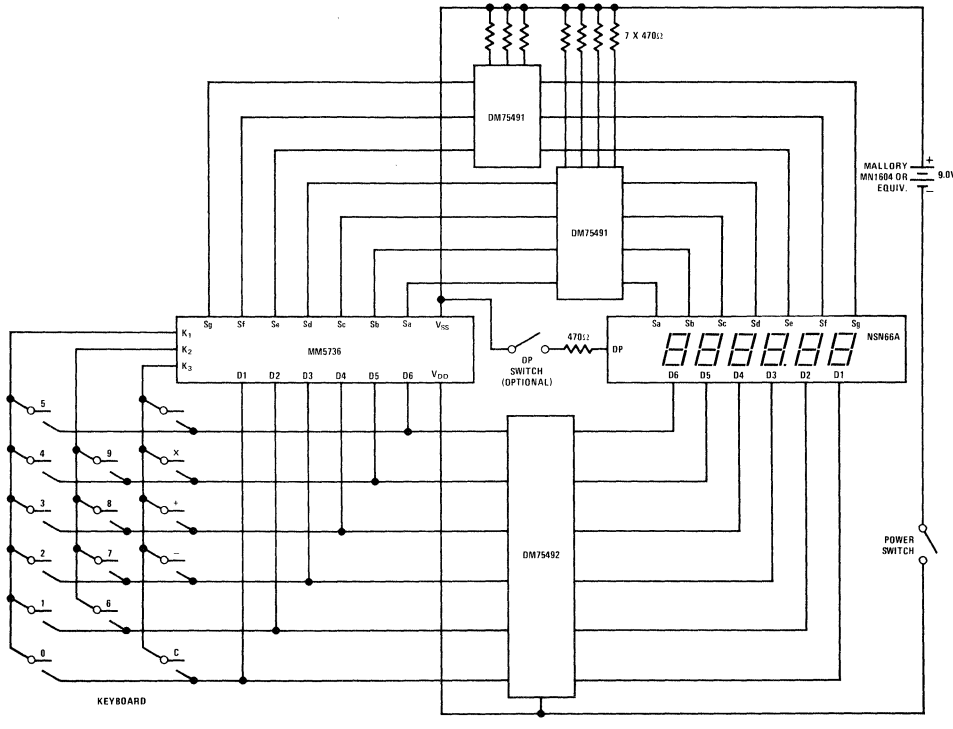


FIGURE 2. Recommended Calculator Configuration with MM5736

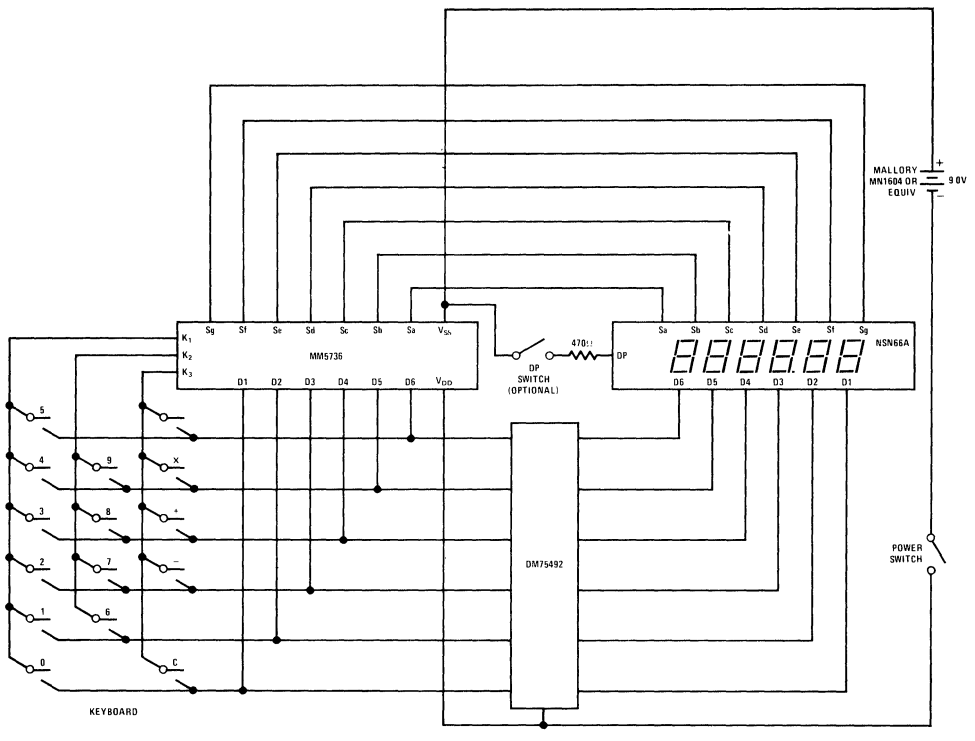


FIGURE 3. Optional Calculator Configuration with MM5736

keyboard bounce and noise rejection characteristics

The MM5736 calculator is designed to interface with low cost keyboards. These keyboards are usually the least desirable from a noise and false entry standpoint. When a key closure is sensed by the calculator, an internal timeout is started. Any peturbations which occur during the timeout will reset the timer to zero so that a key is only accepted as vaild after a noise-free time out period. Noise that persists indefinitely will inhibit key entry. Key releases are checked in the same manner.

Low cost conductor loaded elastomeric keyboards often have key-pressure versus contact resistance characteristics that can create almost continuous noise during "teasing" or low pressure key depressions. The MM5736 keyboard scanning circuitry can accept a series switch resistance up to 50 kΩ as a valid closure, which combined with the internal resettable debounce timer, insures reliable key operations under a variety of conditions and keyboards.

range of the calculator

The MM5736 is capable of displaying six significant positive digits and five negative digits:

$$-99999 \leq \text{Display} \leq +999999$$

The display scans from right (LSD) to left (MSD). Digit 1 time (Figure 1) corresponds to LSD.

error conditions

The following is a list of error conditions which are displayed by the MM5736. If any of these conditions occur, the machine automatically locks out all key entries except CLEAR.

Error	Display
(1) Too many numbers entered	EXXXXX
(2) Negative solution too large	EEXXXX
(3) Positive Solution too large	EXXXXX
(4) Divide by 0	EEEEEE

key description

Clear Key:

a. Operation during number entry

1. First depression functions as a clear entry when followed by a number reentry.
2. Second depression functions as a clear all.

b. Operation after function key will clear all registers.

c. Power on: Two depressions are required at power on to clear the machine.

0 Through 9 Keys:

a. First entry clears the display register and enters the digit into the least significant digit.

b. Second through sixth entry shifts the display register left one digit and enters the digit into the least significant digit.

c. Seventh entry shifts the display register right one digit and displays an E in the most significant digit of the display register.

Add Key: Depression of this key will add the number entered to the accumulator and display the results. Further depressions without number entry will result in a repeated addition of the entry to the accumulator.

Subtraction Key: Depression of this key will subtract the number entered from the accumulator and display the results. Further depressions without number entry will result in repeated subtractions of the entry from the accumulator.

Multiplication Key: Depression of this key will result in a multiplication of the number entered by the accumulator with the results being displayed. If no entry is made, the number being displayed will be squared.

Divide Key: Depression of this key will result in a division of the accumulator by the number entered, with the results being displayed.

examples

BALANCING A CHECK BOOK

Key	Display
C	0
35323	35323
+	35323
10018	10018
−	25305
9595	9595
−	15710
16000	16000
−	− 290
35000	35000
+	34710

examples (con't)

MULTIPLICATION

Key	Display
C	0
1000	1000
+	1000
4	4
x	4000

DIVISION

Key	Display
C	0
1000	1000
+	1000
3	3
÷	333

CHAIN OPERATIONS

Key	Display
C	0
1500	1500
+	1500
400	400
−	1100
2	2
x	2200
7	7
÷	314

AUTO SQUARING

Key	Display
C	0
3	3
+	3
x	9
x	81

REPETITIVE ADD/SUBTRACT (AUTO SUMMING)

Key	Display
C	0
3	3
+	3
+	6
+	9
−	6
−	3

CLEAR ENTRY

Key	Display
C	0
3	3
+	3
4	4
C	0
5	5
+	8
C	0
9	9
+	9

Complex Standards

MM5738 calculator

general description

The MM5738 calculator was designed with "low system cost" as a major criterion. Through advanced design techniques National Semiconductor has been able to incorporate many desirable features into the MM5738 and still offer significant overall cost effectiveness, probably best emphasized by evaluating the additional components required to fabricate a competitors complete hand-held calculator.

Other than a single DM8864 digit driver, there are *NO* external components necessary to interface the MM5738 to the LED display, keyboard and 9.0V battery of a finished calculator. Figure 1 shows the keyboard matrix and interconnections of these elements.

The MM5738 uses the familiar algebraic notation performing addition, subtraction, multiplication division and percentage operations on positive or negative eight digit, floating point numbers. It is capable of doing chain or constant problems while retaining another number in an independent memory register. The contents of the memory register are only altered upon the depression of the *Memory Store* key and are unaffected by any clear or recall memory operations.

The MM5738 provides an on-chip key debounce circuit that interfaces directly with the appropriate keyboard matrix (Figure 1). While a digit driver is required, the MM5738 can drive the segments of most common cathode LED displays directly. The one-of-nine digit outputs provide the strobe signals necessary to enable the proper digit for display; segment data for each digit appears during the appropriate strobe (Figure 2). The ninth digit is used as a sign or error indicator, and in conjunction with the DM8864 digit driver, as a low voltage indicator. (The decimal point of the ninth digit is usually used as the low voltage indication alerting the user to the need for battery replacement in the near future, without interfering with his normal use of the calculator.) The negative sign always resides one position to the left of the most significant digit of negative numbers and therefore only appears in the ninth position when an eight digit negative number is being displayed.

Leading zero blanking and a display turnoff circuit have been incorporated into the MM5738 to conserve battery life. Battery life is estimated to be between 10 and 15 hours, depending upon battery quality, operating schedule and the average number of digits displayed.

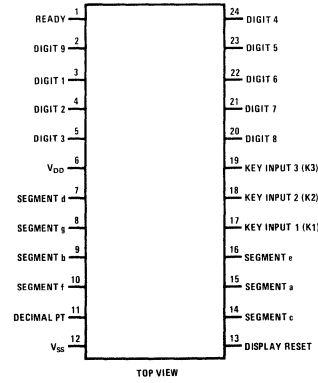
The *READY* pin from the MM5738 is an output signal used to indicate when the calculator is performing an operation. This signal may be helpful if the device is used in a system other than a calculator or for optimizing testing. It is possible to defeat the key debounce circuit for faster key entries.

features

- Full 8-digit capacity
- 5-functions (+, −, x, ÷, %)
- Chain operations
- 2-key memory
- Constant operations independent of memory
- Auto squaring
- Percent discount and tax operations
- Floating decimal point for ease of operation
- Floating negative sign indicator. Tracks most significant digit.
- Convenient algebraic key entry notation
- Leading zero blanking
- On-chip oscillator uses no external components
- Display turnoff (after 16 seconds) with no external components
- Requires only a digit driver to interface with an LED display
- Key debounce uses no external components
- Direct 9.0V battery compatibility

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5738N
See Package 18

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS}
(All other pins connected to V_{SS}) +0.3V to −12.0V
Ambient Operating Temperature 0°C to +70°C
Ambient Storage Temperature −55°C to +150°C
Lead Temperature (Soldering, 10 seconds) 300°C

operating voltage range

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$

(V_{SS} always defined as most positive supply voltage)

dc electrical characteristics (Tentative)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS} - 9.5V$ $T_A = 25°C$			10.5	mA
Keyboard Scan Input Levels (K1 through K3)					
Logical High Level		$V_{SS}-2.5$			V
Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{SS}-5.0$	V
	$V_{DD} = V_{SS} - 9.5V$			$V_{SS}-6.0$	V
Display Reset Input Levels					
Logical High Level		$V_{SS}-1.5$			V
Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{SS}-3.5$	V
	$V_{DD} = V_{SS} - 9.5V$			$V_{SS}-4.5$	V
Digit Buffer Output Levels (D1 through D9)					
Logical High Level	$I_{OUT} = -1.2$ mA, $V_{DD} = V_{SS} - 6.5V$	$V_{SS}-1.5$			V
Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{SS}-6.0$	V
	$V_{DD} = V_{SS} - 9.5V$			$V_{SS}-7.0$	V
Source Current, $T_A = 25°C$	$V_{OUT} = V_{SS} - 3.6V$, $V_{DD} = V_{SS} - 6.5V$	−5.0			mA
	$V_{OUT} = V_{SS} - 5.0V$, $V_{DD} = V_{SS} - 8.0V$		−10		mA
	$V_{OUT} = V_{SS} - 6.5V$, $V_{DD} = V_{SS} - 9.5V$			−15	mA

ac electrical characteristics (Tentative)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time (Figure 2)		0.64		2.4	ms
Digit Time (Figure 2)		70		267	μs
Interdigit Blanking Time (Figure 2)			4.0		μs
Digit Output Transition Times					
Rise	$C_{LOAD} = 100$ pF		2.0		μs
Fall	$C_{LOAD} = 100$ pF		5.0		μs
Keyboard Scan Inputs High to Low Transition Time After Key Release	$C_{LOAD} = 100$ pF		4.0		μs
Key Bounce-out Stability Time (The Time a Keyboard Scan Input Must be Continuously Higher than the Minimum Logical High Level to be Accepted as a Key Closure, or Lower than the Maximum Logical Low Level to be Accepted as a Key Release.)		4.5		17	ms
Display Cutoff Time (The Time After the Last Valid Key Closure at Which the 7 Most-Significant Bits Will be Blanked.)		9.0	16	37	seconds
Calculation Time (Worse Case For: 99999999 ÷ 1 = 99999999.)		0.093		0.35	seconds

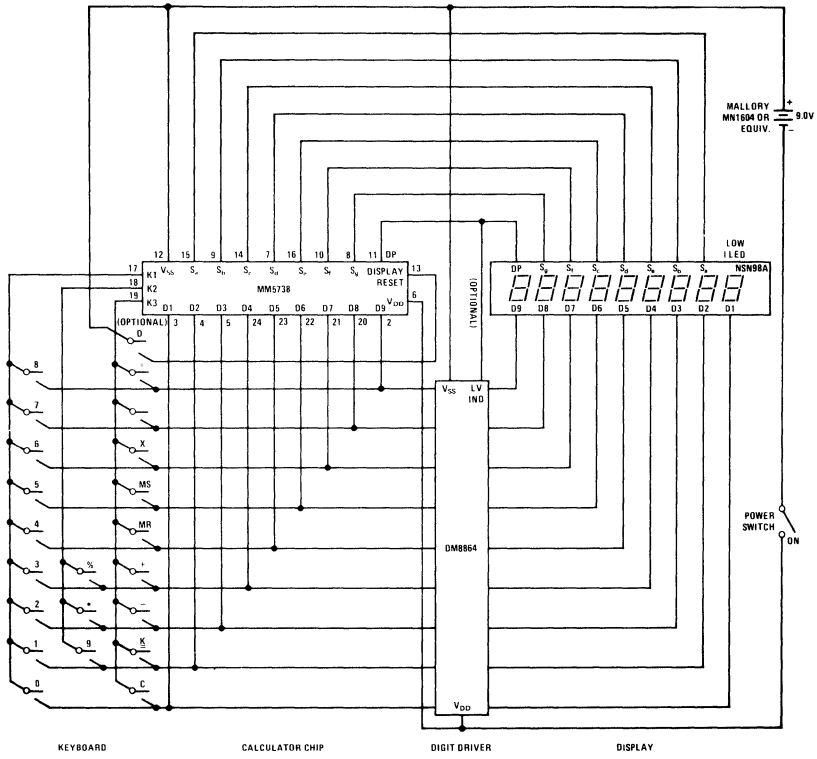


FIGURE 1. MM5738 Calculator with Low Voltage Indicator and Display

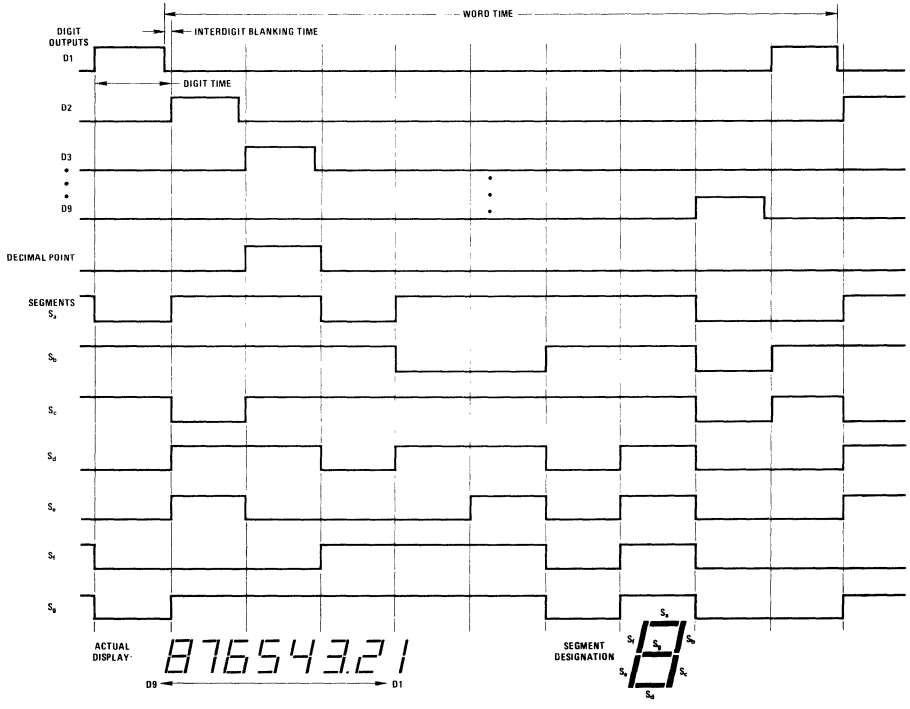


FIGURE 2. Display Timing Diagram

BOUNCE AND NOISE REJECTION

The MM5738 calculator can successfully interface with low cost keyboards. These keyboards are usually the least desirable from a noise and false entry standpoint. When a key closure is sensed by the calculator, an internal timeout is started. Any voltage perturbations of significant magnitude which occur on the *Key Input* Lines (K1, K2 or K3) during the timeout will reset the timer to zero. A key is only accepted as valid after a noise-free timeout period; noise that persists indefinitely will inhibit key entry. Key releases are checked in the same manner.

Low cost conductor loaded elastomeric keyboards often have a key-pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions. The MM5738 defines a series switch resistance up to 50 kΩ to be a valid key closure which combined with the resettable debounce timer insures reliable operation under a variety of such conditions.

DISPLAY TURNOFF

The MM5738 has an internal timer which will turn off the seven most significant LEDs when no key closures have been made for a period of sixteen seconds. The previous display will reappear when the *DISPLAY RESET* pin is momentarily connected to V_{SS}. Any other key depressed after a display turnoff reactivates the display, modifying it appropriately. This circuit requires no external components, other than a *DISPLAY RESET* switch (which could be physically part of the keyboard). The option can be disabled by hardwiring the *DISPLAY RESET* pin to V_{SS}.

ERROR CONDITIONS

In the event of an overflow, the MM5738 will display an E and at least the seven most significant digits of the answer, except in the case of division by 0.

An E will also appear if the action of the percent key results in underflow of the decimal point. Once in an error condition, all keys except the *CLEAR* key are ignored. The contents of the memory register are never altered by an error condition or the subsequent clear operation.

KEY OPERATIONS

I. Clear Key

A. Operation during number entry (acts as a clear entry key).

1. First depression clears the entry and displays a previous result.
2. Second depression clears all registers except memory register and displays a zero without decimal point in the least significant digit (LSD).

B. Operation after a function key will clear all registers except the memory register.

C. Operation following Power On: Two depressions are required.

II. Display Key (Momentarily connecting V_{SS} to *DISPLAY RESET* pin.)

A. Depressed before display turn-off will reset the internal timer, and extend the time before turn-off occurs.

B. Depressed after display turn-off will reset the internal timer and return the display without altering the information.

C. Any key depression will also reset the internal timer and activate an updated display.

III. Number Entries

A. First Entry clears the display register and enters the number into the LSD of the register.

B. Second through eighth Entry shifts the display register left one digit and enters the number into the LSD of the register.

C. Subsequent Entries are ignored. Also, only seven positions are allowed to follow the decimal point. Therefore, the eighth number entry after a decimal point would be ignored.

IV. Decimal Point Key

A. First depression of this key will enter a decimal point in the least significant position of the display register. If there have not been previous number entries, the display will show a zero and a decimal point in the LSD.

B. Subsequent depressions of this key before a function key entry will be ignored.

V. Percent Key

Each depression of this key will shift the decimal point two places to the left. If the display has no decimal point, one is inserted in the second position. If shifting results in loss of the decimal point, an E will appear in the ninth LED and the machine will lock out further entries until *CLEAR* is depressed.

A. Depression after a function key will perform the operation described above on the result being displayed and the machine will go to the number entry mode.

B. Depression while in the number entry mode will perform the operation described above.

VI. Memory Store Key

Depression of this key will store the display register information in the memory register. The memory will only retain magnitude information; i.e., it does not store sign data.

VII. Memory Recall Key

Depression of this key will recall the number stored in the memory register and insert it into the display register just as if it had been keyed in as an entry.

VIII. Add Key

A. Depression of this key after an equal key will re-enter the results from the equal operation and record the fact that an addition is the next function to be executed.

B. Depression of this key while in the number entry mode will:

1. Indicate the end of the entry.
2. Perform the previously recorded function, if any.
3. Record the fact that an addition is the next function to be executed.

C. Depression of this key after the subtraction, multiplication, division or an earlier add key, without an interceding number entry, will record the fact that an addition is next function to be executed.

IX. Subtraction Key

Same action as the add key except that subtract will be recorded instead of addition.

X. Multiplication Key

Same action as the add key except that multiplication will be recorded instead of addition.

XI. Division Key

Same action as the add key except that division will be recorded instead of addition.

XII. Equal Key

A. Depression of this key while in the number entry mode will:

1. Indicate the end of the entry.
2. Perform the previously recorded function.
3. Record the fact that an equal key has been depressed.

B. Depression of this key after the add, subtract or divide key, without an interceding number entry, will be ignored.

C. Depression of this key after a multiplication key, without an interceding number entry, will result in an auto squaring of the number being displayed. Subsequent equal key depressions will continue to auto square.

XIII. Constant Key

The number entry following each multiplication or division key is automatically stored in a constant register. (This register is *not* the memory register.)

A. Depression of the constant key while in the multiplication mode will result in multiplying the display by the constant register. The value of the constant remains unchanged.

B. Depression of the constant key while in the division mode will result in dividing the display by the constant register. The value of the constant remains unchanged.

C. Multiple depressions of the constant key is a technique for raising a number to an integer power. The integer may be positive or negative. See the examples.

D. Operation of the constant key in the proper sequence is used for percent discount and tax add on problems. See the examples.

sample problems

I. Addition and Subtraction

A. 23.37 + 243.00 − 489.16 = −222.79

KEY	DISPLAY	COMMENTS
C		
C	0	First C is clear entry.
2	2	
3	23	
·	23.	
3	23.3	
7	23.37	
+	23.37	
243	243	
−	266.37	Perform addition.
489.17	489.17	Wrong entry.
C	266.37	Clear entry; return previous total.
489.16	489.16	
=	−222.79	Floating negative indicator.

sample problems (con't)

II. Multiplication

A. 5 x 3.14 = 15.7

KEY	DISPLAY	COMMENTS
C		
C	0	
5	5	
x	5.	
3.1 4	3.1 4	Second entry stored as constant.
=	1 5.7	

B. Continue with a constant operation:

7 x 3.14 = 21.98
.003 x 3.14 = 0.00942

KEY	DISPLAY	COMMENTS
7	7	
K=	2 1.9 8	K= is a dynamic key that is decoded with the others in the keyboard matrix. (Figure 1)
.0 0 3	0.0 0 3	
K=	0.0 0 9 4 2	

III. Auto Squaring and Raising a Number to a Positive Power (See V for Negative Powers)

A. $5.25^2 = 27.5625$

KEY	DISPLAY	COMMENTS
C		
C	0	
5.2 5	5.2 5	
x	5.2 5	
=	2 7.5 6 2 5	5.25 is stored as a constant.

B. $6.37^3 = 258.47485$,
$6.37^4 = 1646.4847$ and
$6.37^8 = 2710911.8$

KEY	DISPLAY	COMMENTS
C		
C	0	
6.3 7	6.3 7	
X	6.3 7	
=	4 0.5 7 6 9	6.37^2
K=	2 5 8.4 7 4 8 5	6.37^3
K=	1 6 4 6.4 8 4 7	6.37^4
=	2 7 1 0 9 1 1.8	= while in X mode always squares the display and also stores a new constant.

IV. Division

A. .4 ÷ .3 = 1.3333333

KEY	DISPLAY	COMMENTS
C		
C	0	
.4	0.4	
÷	0.4	Second entry stored as constant.
.3	0.3	
=	1.3 3 3 3 3 3 3	

sample problems (con't)

B. Continue, with constant calculations:

.0005 ÷ .3 = 0.0016666
3 ÷ .3 = 10.

KEY	DISPLAY	COMMENTS
.0005	0.0005	
K	0.00016666	
3	3	
K	10.	

V. Raising a Number to a Negative Power

A. 4.3176^{-3} = 0.0124243

KEY	DISPLAY	COMMENTS
C		
C	0	
1	1	
÷	1	
4.3176	4.3176	Constant is stored.
=	0.2316101	
K	0.0536432	
K	0.0124243	

B. $.7356^{-5}$ = 4.6429217

KEY	DISPLAY	COMMENTS
C		
C	0	
1	1	
÷	1	
.7356	0.7356	
=	1.359434	
K	1.848061	
K	2.512317	
K	3.41533	
K	4.642917	

C. $.7356^{-9}$ = 15.85708 using auto square and memory

KEY	DISPLAY	COMMENTS
C		
C	0	
1	1	
÷	1	
.7356	0.7356	
S	0.7356	Store to memory.
=	1.359434	$.7356^{-1}$
X	1.359434	Re-enter results.
=	1.848060 8	$.7356^{-2}$
=	3.41532 87	$.7356^{-4}$
=	11.66447	$.7356^{-8}$
÷	11.66447	Re-enter results.
R	0.7356	Recall memory.
=	15.85708	$.7356^{-9}$

sample problems (con't)

VI. Chain Operations Using Memory and %

$$\frac{-(131/19.6) + (0.045 - 26.31) \times 1001.2}{37.65} \times 87\% = 607.8030$$

KEY	DISPLAY	COMMENTS
C		
C	0	
1 3 1	1 3 1	
÷	1 3 1	
1 9.6	1 9.6	
=	6.6 8 3 6 7 3	
S	6.6 8 3 6 7 3	Store to memory.
.0 4 5	0.0 4 5	
−	0.0 4 5	
2 6.3 1	2 6.3 1	
X	−2 6.2 6 5	
1 0 0 1.2	1 0 0 1.2	
−	−2 6 2 9 6.5 1 8	
R	6.6 8 3 6 7 3	Recall from memory.
÷	−2 6 3 0 3.2 0 1	
3 7.6 5	3 7.6 5	
X	−6 9 8.6 2 4 1	
8 7	8 7	
%	0.8 7	% can be used with +, −, x, or ÷.
=	−6 0 7.8 0 2 9 6	

VII. Evaluating an Expense Account Using Memory

	Mon	Tues	Wed	Thurs	Fri	Total
Breakfast		1.25	1.37	1.75	1.37	5.74
Lunch	2.65	1.97	2.35	3.15	2.98	13.10
Dinner	7.50	6.85	8.32	7.25		29.92
Lodging	21.50	21.50	21.50	21.50		86.00
Telephone	1.75	.75	.00	1.97		4.47
Transportation	3.75		3.25		3.75	10.75
Totals	37.15	32.32	36.79	35.62	8.10	149.98

KEY	DISPLAY	COMMENTS
C		
C	0	Find weekly totals:
1.2 5	1.2 5	
+	1.2 5	
1.3 7	1.3 7	
+	2.6 2	
1.7 5	1.7 5	
+	4.3 7	
1.3 7	1.3 7	
=	5.7 4	Breakfast total.
S	5.7 4	Store to memory.
2.6 5	2.6 5	
+	2.6 5	
1.9 7	1.9 7	
+	4.6 2	
2.3 5	2.3 5	
+	6.9 7	
3.1 5	3.1 5	
+	1 0.1 2	
2.9 8	2.9 8	

sample problems (con't)

VII. Continued

KEY	DISPLAY	COMMENTS
+	1 3.1	Lunch total.
R	5.7 4	
=	1 8.8 4	Calculate and store.
S	1 8.8 4	New subtotal.
7.5 0	7.5	
+	7.5	
6.8 5	6.8 5	
+	1 4.3 5	
8.3 2	8.3 2	
+	2 2.6 7	
7.2 5	7.2 5	
+	2 9.9 2	Dinner total.
R	1 8.8 4	
=	4 8.7 6	Calculate and store.
S	4 8.7 6	New subtotal.
2 1.5 0	2 1.5 0	
X	2 1.5 0	
4	4	
+	8 6.	Lodging total.
R	4 8.7 6	
=	1 3 4.7 6	Calculate and store.
S	1 3 4.7 6	New subtotal.
1.7 5	1.7 5	
+	1.7 5	
0.7 5	0.7 5	
+	2.5	
1.9 7	1.9 7	
+	4.4 7	Phone total.
R	1 3 4.7 6	
=	1 3 9.2 3	Calculate and store.
S	1 3 9.2 3	New subtotal.
3.7 5	3.7 5	
+	3.7 5	
3.2 5	3.2 5	
+	7.	
3.7 5	3.7 5	
+	1 0.7 5	Cab total.
R	1 3 9.2 3	
=	1 4 9.9 8	Calculate total.

The same technique is used to find the daily subtotals and the double-check of the accumulative total.

VIII. Evaluate a Polynomial Using Constant and Memory

Find: $3x^3 + 2x^2 + 3.1x - 16 = ?$, for $x = 5.1$

KEY	DISPLAY	COMMENTS
C		
C	0	
3	3	
X	3	
5.1	5.1	
=	1 5.3	
K	7 8.0 3	
K	3 9 7.9 5 3	Calculate $3x^3$
S	3 9 7.9 5 3	Store $3x^3$
2	2	

sample problems (con't)

VIII. Continued

KEY	DISPLAY	COMMENTS
K	1 0.2	
K	5 2.0 2	Calculate $2x^2$
+	5 2.0 2	Re-enter $2x^2$
R	3 9 7.9 5 3	Recall $3x^3$
=	4 4 9.9 7 3	Calculate $3x^3 + 2x^2$
S	4 4 9.9 7 3	Store $3x^3 + 2x^2$
3.1	3.1	
X	3.1	
K	1 5.8 1	Calculate 3.1x
+	1 5.8 1	Re-enter 3.1x
R	4 4 9.9 7 3	Recall $3x^3 + 2x^2$
−	4 6 5.7 8 3	Calculate $3x^3 + 2x^2 + 3.1x$
1 6	1 6	
=	4 4 9.7 8 3	Calculate $3x^3 + 2x^2 + 3.1x - 16$

IX. Evaluate a Polynomial after Factoring. (Note the Convenience of Algebraic Notation.)

Find: $23.4x^3 - 5.3x^2 + .6x - 178 = ?$, for $x = 2.7$

Factoring: $[(23.4x - 5.3)x + .6]x - 178 = ?$

KEY	DISPLAY	COMMENTS
C		
C	0	
2 3.4	2 3.4	
X	2 3.4	
2.7 6	2.7 6	
S	2.7 6	Store X to memory for further use and to save key entry.
−	6 4.5 8 4	
5.3	5.3	
X	5 9.2 8 4	
R	2.7 6	
+	1 6 3.6 2 3 8 4	
.6	0.6	
X	1 6 4.2 2 3 8 4	
R	2.7 6	
−	4 5 3.2 5 7 7 9	
1 7 8	1 7 8	
=	2 7 5.2 5 7 7 9	

X. Adding and Subtracting Percentages

3.5% + 2.7% − 12.6% + 3.1% = −0.033

KEY	DISPLAY	COMMENTS
C		
C	0	
3.5	3.5	
%	0.0 3 5	% key moves decimal point 2 positions to left.
+	0.0 3 5	
2.7	2.7	
%	0.0 2 7	
−	0.0 6 2	
1 2.6	1 2.6	
%	0.1 2 6	
+	−0.0 6 4	
3.1	3.1	
%	0.0 3 1	
=	−0.0 3 3	

sample problems (con't)

XI. Multiplication and Division Using % Key

A. Find the 5.5% tax on the following items: $135.63, $127.35, $189.79.

KEY	DISPLAY	COMMENTS
C		
C	0	
135.63	135.63	
X	135.63	
5.5	5.5	5.5% is stored as constant.
%	0.055	
=	7.459 65	5.5% of $135.63 is $7.46.
127.35	127.35	
K	7.004 25	5.5% of $127.35 is $7.80.
189.79	189.79	
K	10.438 45	5.5% of $189.79 is $10.44.

B. Mark-up Problem

Find the retail price of the following items if they are to be marked-up 33% over these wholesale prices: $89.50, $127.29, $149.95.

KEY	DISPLAY	COMMENTS
C		
C	0	
89.50	89.50	
÷	89.50	
77	77	Items are at 77% of retail.
%	0.77	
=	116.233 76	
127.29	127.29	
K	165.311 6	
149.95	149.95	
K	194.740 2	

C. Find 5% tax on a $129.99 item and then add it on to find total cost to customer.

KEY	DISPLAY	COMMENTS
C		
C	0	
5	5	On this type of problem the percentage must be entered first.
%	0.05	
X	0.05	
129.99	129.99	
+	6.499 5	Tax is calculated, then added on.
K	136.489 5	Total cost is calculated.

D. A salesman, whose commission on a $975.37 sale is 18%, wants to know what his profit is and how much to send to the company.

KEY	DISPLAY	COMMENTS
C		
C	0	
18	18	
%	0.18	On this type of problem the percentage must be entered first.
X	0.18	
975.37	975.37	
−	175.566 6	Profit is calculated then discounted.
K	799.803 4	Difference is calculated

sample problems (con't)

XII. Problem Using % and Memory

A color TV which is normally priced at $599.99 is marked down 20%. When purchased, the following figures are required:

1. Amount of savings to customer.
2. Sales price
3. 6% sales tax
4. Total amount of transaction

KEY	DISPLAY	COMMENTS
C		
C	0	
2 0	2 0	
%	0.2 0	Enter percentage first.
X	0.2 0	
5 9 9.9 9	5 9 9.9 9	
−	1 1 9.9 9 8	Savings to customer.
K	4 7 9.9 9 2	Sales price.
S	4 7 9.9 9 2	Store sales price.
6	6	
%	0.0 6	Enter percentage first.
X	0.0 6	
R	4 7 9.9 9 2	Recall sales price.
+	2 8.7 9 9 5 2	Tax due.
K	5 0 8.7 9 1 5 2	Amount of transaction.

Complex Standards

MM5739 calculator

general description

The MM5739 employs three working registers to provide add, subtract, multiply and divide functions. It includes on-chip key debounce and interfaces directly with the keyboard matrix as shown in Figure 2. While a digit driver is required, the MM5739 can drive the segments of most LED displays directly. A one-of-nine output provides the strobe signals necessary to enable the appropriate digit for display; segment data for each digit appears during the appropriate strobe. See Figure 1 for digit and segment timing. Leading zero blanking and a 16 second display turnoff circuit have been incorporated to conserve battery life. Battery life is estimated to be between 10 and 20 hours, depending upon battery quality, operating schedule and the average number of digits displayed.

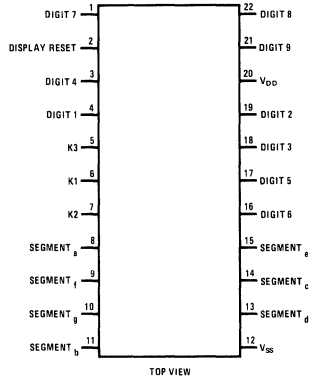
For the additional cost of a single pole slide switch, a decimal point may be lit at any convenient point in the display; i.e., zero decimal point or two decimal point position. (Figure 2 indicates the wiring for a decimal point in the dollars/cents position.) This would be helpful for users who are generally operating in an "adding machine" mode; e.g. housewives when balancing their checkbooks or keeping track of supermarket expenditures.

features

- 9-digit display
- 4-functions (+, −, x, ÷)
- Chain operations
- Auto summing, convenient counting by any radix, and auto squaring
- Floating negative sign indicator for true credit balance
- 3-different error indications
- Leading zero blanking
- On-chip oscillator uses no external components
- Display turnoff after 16 seconds with no external components
- Effective keyboard bounce protection
- Requires only a digit driver to interface with a LED display
- Interfaces with keyboard directly
- 9.0V battery operation with a typical power dissipation less than 35 mW—resulting in a battery life in excess of 15 hours with normal use.

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5739N
See Package 17

absolute maximum ratings

Operating Temperature (Ambient)	0°C to +70°C
Storage Temperature (Ambient)	−55°C to +150°C
Voltage on Any Pin Relative to V_{SS} (All others V_{SS})	+0.3V to −12V
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$V_{SS} - 6.5V \leq V_{DD} \leq V_{SS} - 9.5V$ (V_{SS} is always the most positive supply)

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$V_{DD} = V_{SS} - 9.5V$, $T_A = 25°C$		3.7	7.5	mA
Keyboard Scan Input Levels (K1, K2, K3)					
Logical High Level		$V_{SS} - 2.5$			V
Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{SS} - 5.0$	V
	$V_{DD} = V_{SS} - 9.5V$			$V_{SS} - 6.0$	V
Digit Buffer Output Levels (D1 through D9)					
Logical High Level	$I_{OUT} = -1.2$ mA	$V_{SS} - 1.5V$		V_{SS}	V
Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{SS} - 6.0$	V
	$V_{DD} = V_{SS} - 9.5V$			$V_{SS} - 7.0$	V
Segment Output Current (S_a through S_g)	$T_A = 25°C$				
Source Current	$V_{OUT} = V_{SS} - 3.8V$, $V_{DD} = V_{SS} - 6.5V$	−4.2	−7.5		mA
	$V_{OUT} = V_{SS} - 4.2V$, $V_{DD} = V_{SS} - 7.25V$		−10		mA
	$V_{OUT} = V_{SS} - 7.8V$, $V_{DD} = V_{SS} - 9.5V$			−20	mA

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time (Figure 1)		0.64	1.50	2.40	ms
Digit Time (Figure 1)		70		267	μs
Interdigit Blanking Time (Figure 1)			4.0		μs
Digit Output Transition Times (Rise and Fall)	$C_{LOAD} = 100$ pF		2.0		μs
Keyboard Sensing Inputs (K1, K2, K3) High to Low Transition Time, after Key Release	$C_{LOAD} = 100$ pF		4.0		μs
Key Bounce-Out Stability Time (The time a keyboard serving input must be continuously higher than the minimum Logical High Level to be accepted as a key closure, or lower than the maximum Logical Low Level to be accepted as a key release.)		4.5		17	ms
Display Cutoff Time		9.0	20	37	seconds

BOUNCE AND NOISE REJECTION

The MM5739 calculator is designed to interface with low cost keyboards. These keyboards are usually the least desirable from a noise and false entry standpoint. When a key closure is sensed by the calculator, an internal timeout is started. Any perturbations which occur during the time-out will reset the timer to zero. A key is only accepted as valid after a noise-free Key Bounce-out Stability Time as defined in the electrical characteristics section. Noise that persists indefinitely will inhibit key entry. Key releases are checked in the same manner.

Low cost conductor loaded elastomeric keyboards often have a key-pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions when interfaced with some keyboard scanning techniques. The MM5739 senses a series switch resistance up to 50 kΩ as a valid key closure, providing a reliable interface under these conditions.

DISPLAY TURNOFF CIRCUIT

The MM5739 has an internal timer which will turn off the 8 most significant digits of the display when no key closures are made for a period of 20 seconds (typically); The previous display will reappear when the *DISPLAY RESET* pin is momentarily connected to V_{SS}. In addition, any key depressed after a display turnoff reactivates the display, modifying it appropriately. This circuit requires no external components and can be disabled by hardwiring the *DISPLAY RESET* input to V_{SS}.

RANGE OF THE CALCULATOR

The MM5739 is capable of displaying nine significant positive digits and eight negative digits:

$$-99\ 999\ 999 \leq \text{Display} \leq 999\ 999\ 999$$

The display scans from right (LSD) to left (MSD). Digit 1 time (Figure 1) corresponds to LSD.

ERROR CONDITIONS

The following is a list of error conditions which are displayed by the MM5739. If any of these conditions occur the machine automatically locks out all key entries except clear.

Error	Display
(1) Too many numbers entered	EXXXXX
(2) Negative solution too large	EEXXXX
(3) Positive Solution too large	EXXXXX
(4) Divide by 0	EEEEEE

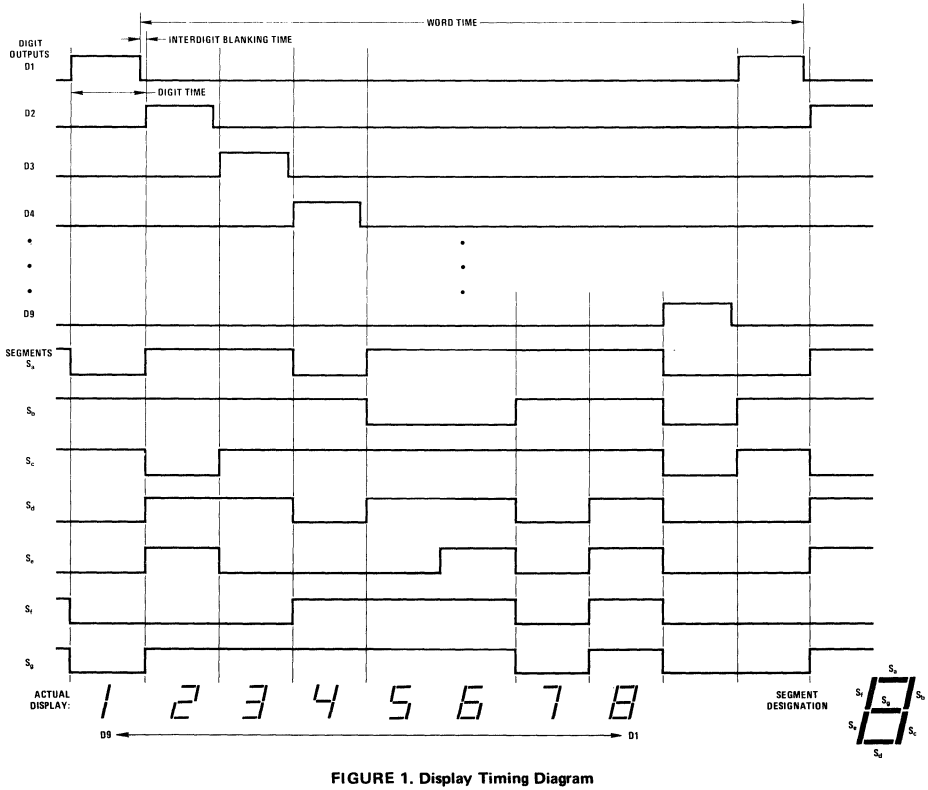


FIGURE 1. Display Timing Diagram

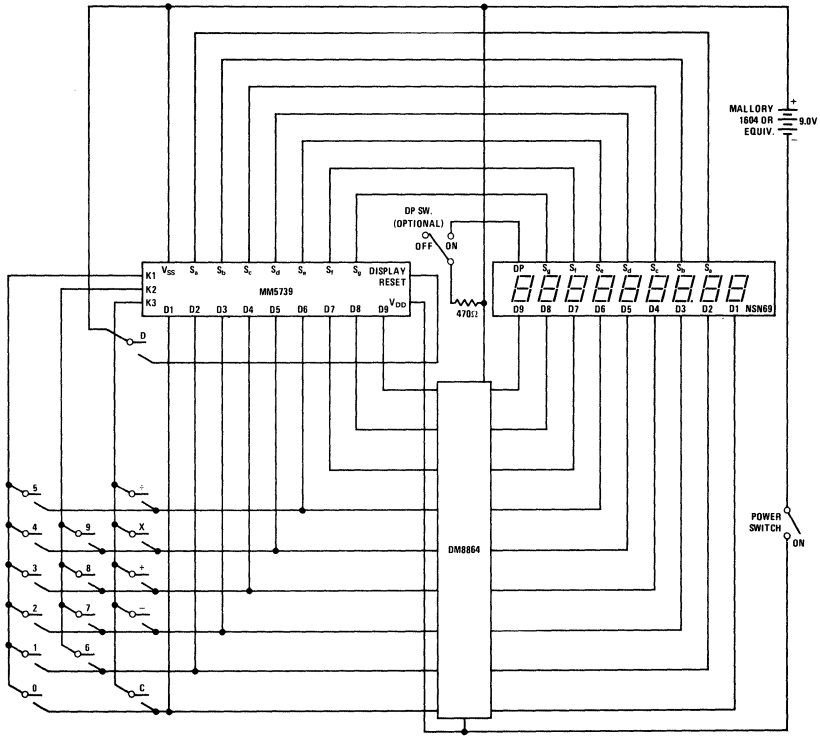


FIGURE 2a. Recommended MM5739 Calculator Schematic with Display Cutoff Feature

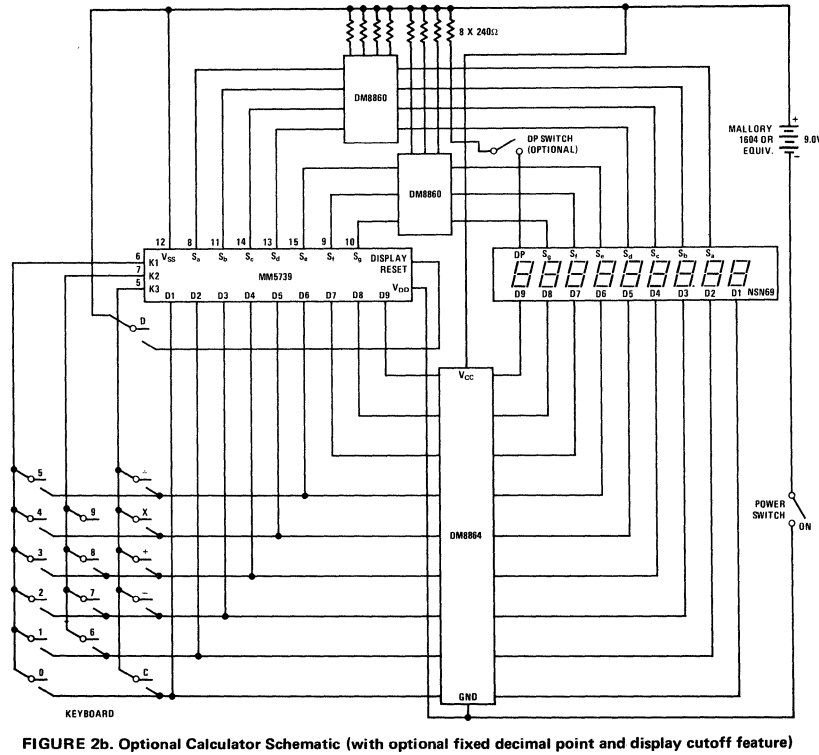


FIGURE 2b. Optional Calculator Schematic (with optional fixed decimal point and display cutoff feature)

key operations

Clear Key:

a. Operation during number entry.
   1. First depression functions as a clear entry.
   2. Second depression functions as a clear all.
b. Operation after function key will clear all registers.
c. Power On: Two depressions are required at power on to clear the machine.

0 Through 9 Keys

a. First Entry clears the display register and enters the digit into the least significant digit.
b. Second through Ninth Entry shifts the display register left one digit and enters the digit into the least significant digit.
c. Tenth Entry shifts the display register right one digit and displays an E in the most significant digit of the display register.

Add Key: Depression of this key will add the number entered to the accumulator and display the results. Further depressions without number entry will result in a repeated addition of the entry to the accumulator.

Subtraction Key: Depression of this key will subtract the number entered from the accumulator and display the result. Further depressions without number entry will result in repeated subtractions of the entry from the accumulator.

Multiplication Key: Depression of this key will result in a multiplication of the number entered by the accumulator with the results being displayed. If no entry is made, the number being displayed will be squared.

Divide Key: Depression of this key will result in a division of the accumulator by the number entered, with the results being displayed.

examples

Balancing a Checkbook:

Key	Display
C	0
987635323	987635323
+	987635323
10018	10018
−	987625305
9595	9595
−	987615710
987616000	987616000
−	−290
35000	35000
+	34710

examples (con't)

Multiplication:

Key	Display
C	0
1000	1000
+	1000
4	4
x	4000

Division:

Key	Display
C	0
1000	1000
+	1000
3	3
÷	333

Chain Operations:

Key	Display
C	0
1500	1500
+	1500
400	400
−	1100
2	2
x	2200
7	7
÷	314

Auto Squaring:

Key	Display
C	0
3	3
+	3
x	9
x	81

Repetitive Add/Subtract Auto Summing:

Key	Display
C	0
3	3
+	3
+	6
+	9
−	6
−	3

Clear Entry:

Key	Display
C	0
3	3
+	3
4	4
C	3
5	5
+	8
C	0
9	9
+	9

Complex Standards

MM5740 90-key keyboard encoder

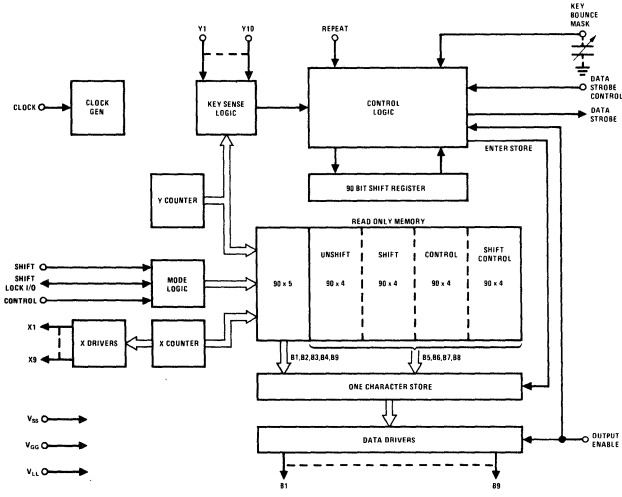
general description

The MM5740 MOS/LSI keyboard encoder is a complete keyboard interface system capable of encoding 90 single pole single throw switch closures into a usable 9-bit code. It is organized as a bit paired system and is capable of N key or two key rollover. The MM5740 is fabricated with silicon gate technology and provides for direct TTL/DTL compatibility on Data and Strobe outputs without the use of any special interface components.

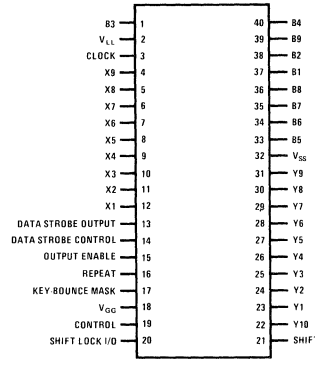
features

- TRI-STATE® data outputs directly compatible with TTL/DTL or MOS logic
- Function inputs directly compatible with TTL/DTL logic
- Only one TTL level clock required
- N key/two key rollover (mask programmable)
- 90 key-quad mode capability
- One character data storage
- Repeat function (selectable)
- Shift lock with indicator capability
- Key bounce masking by single external capacitor
- Level or pulse data strobe output
- Data strobe pulse width control

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5740AAA/D, MM5740AAB/D or MM5740XXX/D
See Package 8

Order Number MM5740AAA/N, MM5740AAB/N or MM5740XXX/N
See Package 20

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absolute maximum ratings

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW at T_A = +25°C
Operating Temperature	−25°C to +70°C ambient
Storage Temperature	−65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1,5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Repetition Rate		10		200	kHz
Clock Pulse Width	Rep. Rate = 200 kHz	2.4		2.6	μs
	Rep. Rate = 10 kHz	20		80	μs
Clock Amplitude					
Logic Level "0"				+2.4	V
Logic Level "1"		+0.4			V
Clock Transition Times					
Risetime	Rep. Rate = 200 kHz			100	ns
Falltime	Rep. Rate = 200 kHz			100	ns
Clock Input Capacitance			5.0		pF
Data Input Levels, Y1 thru Y10					
Logic Level "0"				V_{SS} − 1.5	V
Logic Level "1"		−3.0			V
Logic Level "0"				+2.4	V
Logic Level "1"		+0.4			V
Data Strobe Control					
Logic Level "0"				+3.5	V
Logic Level "1"		+0.4			V
Data Output Levels, X1 thru X9					
Logic Level "0"	When Connected to Y1 thru Y10			V_{SS} − 0.75	V
Logic Level "1"	via Switch Matrix, (C_L = 75 pF)	−3.0			V
B1 thru B9 and Data Strobe					
Logic Level "0"	I = 100μA (Note 2)			V_{SS} − 1.0	V
Logic Level "1"	I = 1.6 mA (Note 2)	+0.4			V
Shift Lock Voltage Open	Before Closure		V_{GG} − 2.0		V
Shift Lock Voltage Closed	Switch Closed		V_{SS}		V
Shift Lock Voltage Locked	After Release, (I = 1.0 mA) (Figure 2)		V_{SS} − 5.0	V_{SS} − 8.0	V
Transition Times					
Data Strobe (T_{DS1})	C_L = 100 pF, I = 1.6 mA			2.5	μs
Data Strobe (T_{DS0})	C_L = 100 pF, I = 100μA			1.0	μs
Data Output Levels					
(T_{DO1})	C_L = 100 pF, I = 1.6 mA			2.5	μs
(T_{DO0})	C_L = 100 pF, I = 100μA			1.0	μs
Output Enable Setup Time (T_{OES})		2.5			μs
Output Enable Release Time (T_{OER})		2.5			μs
Repeat Input Pulse Width (T_{RPW})	(Note 3)				
	f_{CLOCK} = 10 kHz	10			ms
	f_{CLOCK} = 200 kHz	0.5			ms
Power Supply Current	I_{GG}, I_{SS}		20	35	mA

Note 1: These specifications apply for V_{SS} = +5.0 VDC ±5%, V_{GG} = −12.0 VDC ±5%, V_{LL} = GND and T_A = 0°C to +70°C.

Note 2: When outputs B1 thru B9 and Data Strobe are driving TTL/DTL $V_{SS} - V_{LL} \leq 5.25V$. When driving MOS, $V_{SS} - V_{LL} \leq 10.0V$.

Note 3: Trpw min. = $100 \times \frac{1}{f_{clock}}$

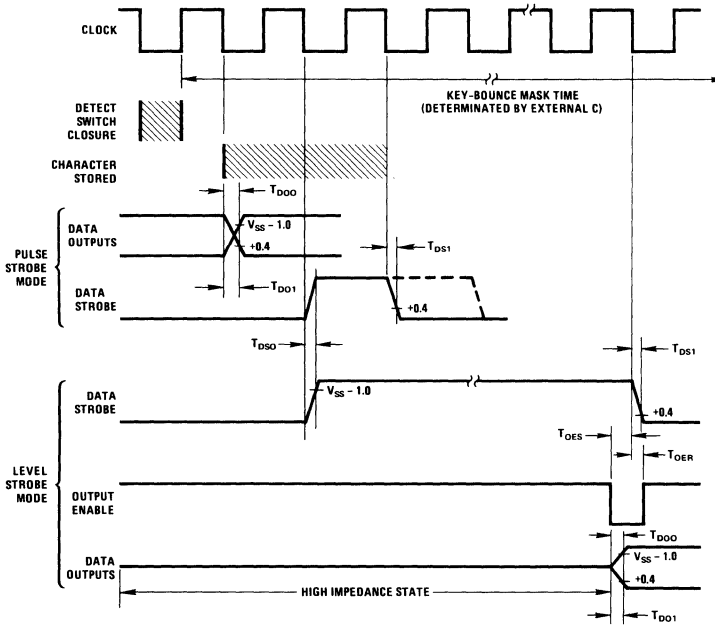
Note 4: If shift and control inputs are derived from a single pole, single throw switch closure to V_{SS}, a 100 OHM resistor returned to V_{LL} (GND) is required on these inputs.

Note 5: The following inputs have internal pull-up resistors to V_{SS}: clock, output enable, repeat, shift, control.

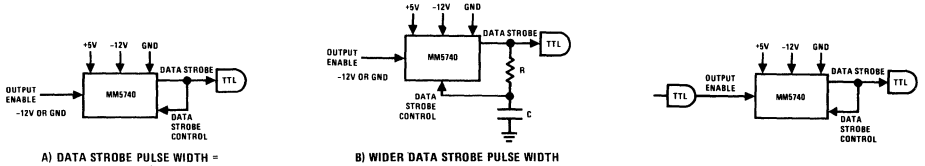
description of pin functions

NAME	PIN NO.	FUNCTION
X1-X9	4-12	These pins are chip outputs which are used to drive the key switch matrix. When activated (at the appropriate scan time) they are driven high.
Y1-Y10	22-31	Pins 22-31 are the Y sense inputs which are connected to the X drive lines via the key switch matrix. They are internally precharged to a low state and are pulled high upon switch closure.
B1-B9	1, 33-40	These are the data outputs which represent the code for each keyswitch. They are TRI-STATE outputs with direct TTL compatibility. When the output enable input (Pin 15) is high, these outputs are in the third state.
Data Strobe Output	13	The function of this pin is to indicate that valid data has been entered by the keyboard and is ready for acceptance. An active data strobe is indicated by a high level. The data strobe may be operated in the pulse or level mode as indicated by the timing diagram.
Data Strobe Control	14	The basic purpose of this input is to provide data strobe output pulse width control. When connected to the data strobe output (Pin 13), the data strobe will exhibit a one bit wide pulse width. The pulse width may be varied by interposing an RC network between the data strobe output and the strobe control input. For level mode of operation the data strobe control input may be tied to V_{SS} or to the data strobe output.
Output Enable	15	This input serves to TRI-STATE the data output (B1-B9) lines. In addition, it controls the return of the data strobe to the idle condition (low state) which is needed in the level strobe mode of operation.
Repeat	16	The repeat input is designed to accept a repeat signal via the repeat key. One data strobe will be issued for each positive interval of the repeat signal. Thus, if a 10 Hz signal is applied to the repeat input via the repeat switch, a 10 character per second data strobe will be issued when a data key and the repeat key are held depressed.
Key-Bounce Mask	17	This pin is intended as a timing node to mask switch key-bounce. The mask time interval is generated by connecting a capacitor to this pin.
Shift	21	When this input is brought to a logic "0" (V_{SS}) level, the encoder will assume the shifted character mode.
Control	19	A logic "0" places the encoder in the control character mode.
Shift Lock I/O	20	This pin is intended to serve as an input when the shift lock key is depressed. It places the encoder in the shift mode. Upon release of the key, the shift mode will be maintained and this pin will serve as an output to drive an indicator. This function is reset by depressing the shift key.
Clock	3	A TTL compatible clock signal is applied to this pin. A bit time is defined as the time from one negative going transition to the succeeding negative going transition of the clock.
V_{SS}	32	+5.0V supply
V_{LL}	2	Ground
V_{GG}	18	−12V supply

timing diagram



applications information



A) DATA STROBE PULSE WIDTH = ONE CLOCK PERIOD

B) WIDER DATA STROBE PULSE WIDTH CONTROLLED BY RC

Pulse Data Strobe Mode

Level Data Strobe Mode

key bounce capacitor values

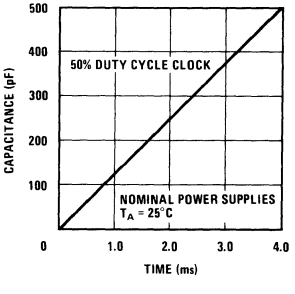


FIGURE 1. Key-Bounce Mask Time

application

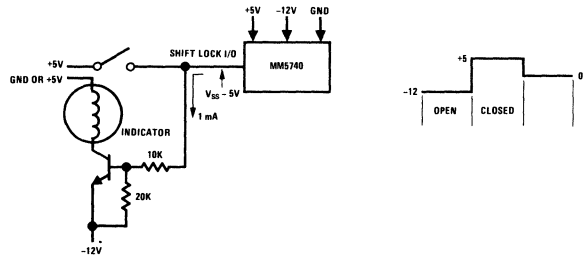
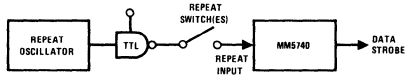
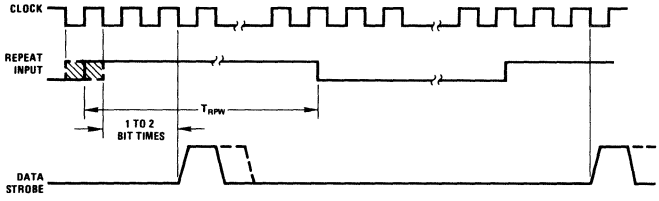


FIGURE 2. Shift Logic I/O Interface

repeat switch function



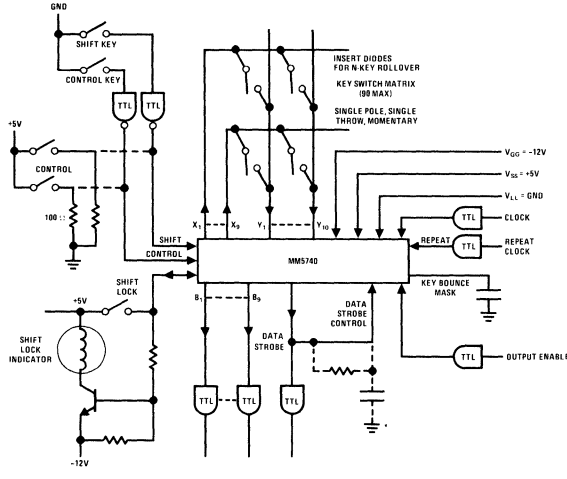
Repeat Switch Connections



Note: Both Repeat Switch and a Data Key must be depressed to enable repeat function. For N-Key Rollover, the data outputs will represent the current valid data key (N Key Roll during Repeat).

Repeat Function

typical applications



CODE ASSIGNMENT CHART

Customer: _____

Date: _____

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
(Note 3)	1																									
	2																									
	3																									
	4																									
	5																									
	6																									
	7																									
	8																									
	9																									
	10																									
	1																									
	2																									
	3																									
	4																									
	5																									
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	10																									
	1																									
	2																									
	3																									
	4																									
	5																									
	6																									
	7																									
	8																									
	9																									
	10																									

☐ N-Key Rollover

☐ 2 Key Rollover

Page ☐ of 3 (Note 1)

Note: Use B8 if parity bit is desired

Note 1: 3 code assignment charts are required for each keyboard encoder pattern. Fill in a "1" or "0" in each output box (B_1 thru B_9). Indicate page number.

Note 2: The matrix is 9 "X" locations by 10 "Y" locations.

Note 3: Write in 10 one's, 10 two's, etc. in successive X address locations up to 9. This will fill 3 charts. The first page will have address matrix location 1,1; 1,2: 1,3... 1,10; 2,1; 2,2... 2,10; 3,1, etc. up to 3,10. Page 2 has 4,1 to 6,10. Page 3 has 7,1 to 9,10.

Note 4: A contact closure at the address matrix location will cause the appropriate bit pattern to appear at the output in negative true logic. V_{OH} = "0"; V_{OL} = "1."

Note 5: See application note AN-80 for coding example.

MM5740AAB, MM5740AAA CODE ASSIGNMENT CHARTS

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
1	1	0	0	0	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	8	8	8	8
1	2	0	0	1	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	4	4	4	4
1	3	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	5	5	5	5
1	4	1	0	0	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	1	1
1	5	0	1	0	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	2	2	2	2
1	6	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	3	3	3	3
1	7	0	0	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	↻	↻	↻	↻
1	8	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	6	6	6	6
1	9	1	0	0	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	9	9	9	9
1	10	1	1	1	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	7	7	7	7
2	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FF	FF	FF	FF
2	2	1	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	CR	CR	CR	CR
2	3	0	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	FS	FS	FS	FS
2	4	1	0	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	GS	GS	GS	GS
2	5	1	1	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	VT	VT	VT	VT
2	6	0	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	SO	SO	SO	SO
2	7	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	SP	SP	SP	SP
2	8	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	HT	HT	HT	HT
2	9	0	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	BS	BS	BS	BS
2	10	1	0	1	1	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1				
3	1	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	↺	↺	↺	↺
3	2	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LF	LF	LF	LF
3	3	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	1	0	0	0	0	P	@	DLE	NUL
3	4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	DEL	DEL	DEL	DEL
3	5	1	1	0	1	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	,	+	,	+
3	6	0	1	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	-	•	-	-
3	7	1	1	1	1	0	0	1	0	1	1	1	0	0	0	1	0	1	1	1	0	0	/	?	/	?
3	8	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	P	P	DLE	DLE
3	9	1	1	1	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	SI	SI
3	10	0	1	0	1	1	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1		•		•

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
4	1	1	0	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	9	)	9	)
4	2	1	0	0	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	I	!	HT	HT
4	3	1	1	1	1	1	0	0	1	1	1	0	1	0	0	0	0	0	1	0	0	1	0		SI	US
4	4	1	1	0	1	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	K	[	VT	ESC
4	5	0	0	1	1	0	0	0	1	1	1	0	1	0	0	0	0	0	1	0	0	1	L		FF	FS
4	6	0	0	1	1	0	0	1	0	1	1	1	0	0	0	1	0	1	1	1	0	0	,	<	,	<
4	7	0	1	1	1	1	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	1	•	>	•	>
4	8	0	0	1	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	L	L	FF	FF
4	9	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	K	K	VT	VT
4	10	0	0	0	1	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	8	(	8	(
5	1	0	1	1	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	6	&	6	&
5	2	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	U	U	NAK	NAK
5	3	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	Y	Y	EM	EM
5	4	0	1	0	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	J	J	LF	LF
5	5	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	H	H	BS	BS
5	6	1	0	1	1	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	M	J	CR	GS
5	7	0	1	1	1	1	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	N	^	SO	RS
5	8	1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	M	M	CR	CR
5	9	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	N	N	SO	SO
5	10	1	1	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	7	'	7	'
6	1	1	0	1	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	5	%	5	%
6	2	0	1	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	R	R	DC2	DC2
6	3	0	0	1	0	0	1	0	1	0	1	0	1	1	1	0	0	0	1	0	0	0	T	T	DC4	DC4
6	4	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	F	F	ACK	ACK
6	5	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	G	G	BEL	BEL
6	6	0	1	1	0	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0	0	V	V	SYN	SYN
6	7	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	B	B	STX	STX
6	8	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	CAN	CAN	CAN	CAN
6	9	1	0	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	EM	EM	EM	EM
6	10	0	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	4	S	4	S

Negative True Logic

$B_1 - B_7$ = ASCII Code
B_8 = Even parity (on $B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8$)
B_9 = Selective Repeat Bit

Note: Use B_8 if parity bit is desired.

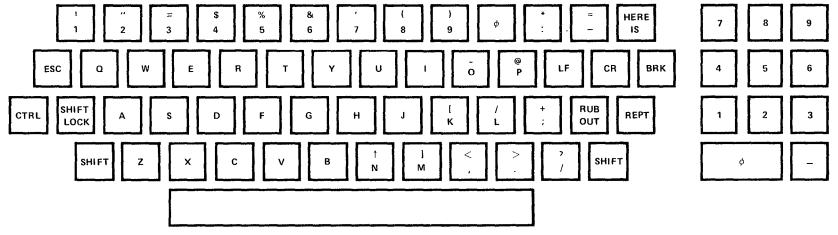
MM5740AAE, MM5740AAF CODE ASSIGNMENT CHARTS (CONTINUED)

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
7	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	DC2	DC2	DC2	DC2
7	2	1	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	E	E	ENG	ENG
7	3	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	DC3	DC3	DC3	DC3
7	4	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	D	D	EOT	EOT
7	5	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	DC4	DC4	DC4	DC4
7	6	1	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	C	C	ETX	ETX
7	7	1	0	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	NAK	NAK	NAK	NAK
7	8	0	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	SYN	SYN	SYN	SYN
7	9	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	ETB	ETB	ETB	ETB
7	10	1	1	0	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	3	#	3	#
8	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ENQ	ENQ	ENQ	ENQ
8	2	1	1	1	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	W	W	ETB	ETB
8	3	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ACK	ACK	ACK	ACK
8	4	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	S	S	DC3	DC3
8	5	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	BEL	BEL	BEL	BEL
8	6	0	0	0	1	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	X	X	CAN	CAN
8	7	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SI	SI	SI	SI
8	8	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	DLE	DLE	DLE	DLE
8	9	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	DC1	DC1	DC1	DC1
8	10	0	1	0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	2	"	2	"
9	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NUL	NUL	NUL	NUL
9	2	1	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	Q	Q	DC1	DC1
9	3	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	ESC	ESC	ESC	ESC
9	4	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	A	A	SOH	SOH
9	5	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	SOH	SOH	SOH	SOH
9	6	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	Z	Z	SUB	SUB
9	7	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	STX	STX	STX	STX
9	8	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ETX	ETX	ETX	ETX
9	9	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	EOT	EOT	EOT	EOT
9	10	1	0	0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	/	'	/	'

Negative True Logic

B_1 - B_7 = ASCII Code
B_8 = Even parity (on B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8)
B_9 = Selective Repeat Bit

Note: Use B_8 if parity bit is desired.



ASR

ASR 33
MM5740AAE (N-KEY ROLLOVER)
MM5740AAF (2-KEY ROLLOVER)

Typical Keyborad Arrangement

Interface Circuits

DM7800/DM8800 dual voltage translator

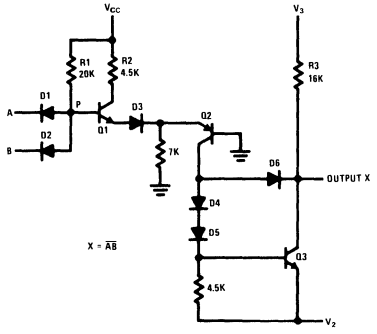
general description

The DM7800/DM8800 are dual voltage translators designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with high impedance junction or MOS FET-type devices. The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

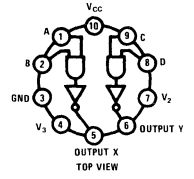
features

- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:
  DM7800 −55°C to +125°C
  DM8800 0°C to +70°C
- Compatible with all MOS devices

schematic and connection diagrams



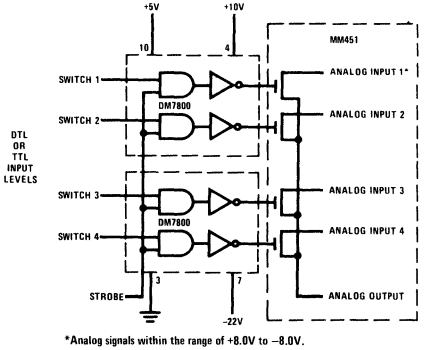
Metal Can Package



Order Number DM7800H
or DM8800H
See Package 24

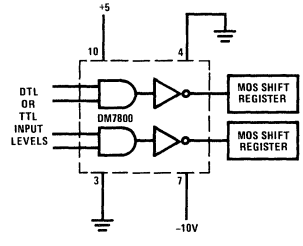
typical applications

4-Channel Analog Switch



*Analog signals within the range of +8.0V to −8.0V.

Bipolar to MOS Interfacing



absolute maximum ratings

V_{CC} Supply Voltage	7.0V
V_2 Supply Voltage	−30V
V_3 Supply Voltage	+30V
V_3-V_2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM7800	−55°C to +125°C
DM8800	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Logical "1" Input Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V			0.8	V
Logical "1" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 2.4V			5	μA
Logical "1" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0.4V		−0.2	−0.4	mA
Output Leakage Current (Note 2)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0.8V (Note 5)			10	μA
Output Collector Resistor		T_A = 25°C	11.5	16.0	20.0	kΩ
Logical "0" Output Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V, V_{IN} = 2.0V (Note 5)			V_2 + 2.0	V
Power Supply Current Logical "0" (Note 3) (Each Gate)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "1" (Note 3) (Each Gate)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0V		0.22	0.41	mA
Transition Time to Logical "0" Output		T_A = 25°C C = 15 pF (Note 6)	25	70	125	ns
Transition Time to Logical "1" Output		T_A = 25°C C = 15 pF (Note 7)	25	62	125	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for the DM7800 and 0°C to +70°C for the DM8800 unless otherwise specified.
Note 2: Current measured is drawn from V_3 supply.
Note 3: Current measured is drawn from V_{CC} supply.
Note 4: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.
Note 5: Specification applies for all allowable values of V_2 and V_3.
Note 6: Measured from 1.5V on input to 50% level on output.
Note 7: Measured from 1.5V on input to logic "0" voltage, plus 1V.

theory of operation

The two input diodes perform the AND function on TTL or DTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2. The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL and DTL, the interfacing with these types of circuits is achieved.

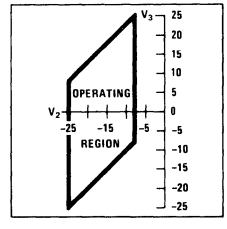
Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2. Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and to Q_3. And when Q_3 turns on the output voltage drops to the logical "0" level.

The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to −25V can be applied to V_2. Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3.

Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the output voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.

selecting power supply voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V_2 is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V_3 is governed by supply V_2. With a value chosen for V_2, V_3 may be selected as any value along a vertical line passing through the V_2 value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



Interface Circuits

DM7802/DM8802, DM7806/DM8806
high speed MOS to TTL level converters

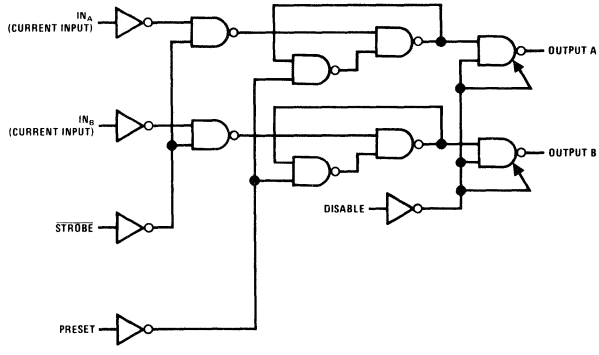
general description

The DM7802/DM8802, DM7806/DM8806 are high speed MOS to TTL level converters. These circuits act as an interface level converter between MOS and TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE® output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

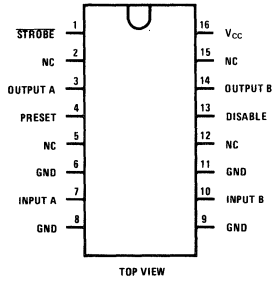
features

- Very low output impedance — high drive ability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter

logic and connection diagrams



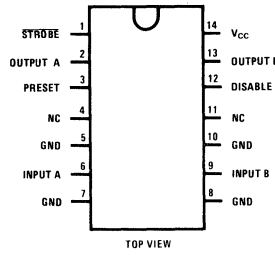
Dual-In-Line Package



Order Number DM7802J, DM8802J, DM7806J or DM8806J
See Package 10

Order Number DM8802N or DM8806N
See Package 15

Flat Package



Order Number DM7806W or DM8806W
See Package 27

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7802, DM7806	4.5	5.5	V
DM8802, DM8806	4.75	5.25	V
Temperature (T_A)			
DM7802, DM7806	−55	+125	°C
DM8802, DM8806	0	+70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Current	V_{CC} = Min	500			μA
Logical "0" Input Current	V_{CC} = Min			200	μA
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −1.5 mA	2.4			V
Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA			0.4	V
Third State Output Current	V_{CC} = Max, V_O = 2.4V			40	μA
	V_{CC} = Max, V_O = 0.4V			−40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
	V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Supply Current	V_{CC} = Max, $V_{IN(DISABLE)}$ = 2 Other Inputs = ϕV			40	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
Output Short Circuit Current (Note 3)	V_{CC} = Max, V_O = 0V				
	DM7802, DM7806	−20		−70	mA
	DM8802, DM8806	−18		−70	mA
Propagation Delay to a Logical "0" From STROBE to Output (t_{ds})	V_{CC} = 5.0V (See Figure 1) T_A = 25°C		17	25	ns
Propagation Delay to a Logical "1" From Preset to Output (t_{dp})	V_{CC} = 5.0V (See Figure 1) T_A = 25°C		22	32	ns
Delay From Disable Input to High Impedance State (From Logical "1" Level)(t_{1H})	V_{CC} = 5.0V (See Figure 2) T_A = 25°C		7.0	11	ns
Delay From Disable Input to High Impedance State (From Logical "0" Level)(t_{0H})	V_{CC} = 5.0V (See Figure 3) T_A = 25°C		17	25	ns
Delay From Disable Input to Logical "1" Level (From High Impedance State)(t_{H1})	V_{CC} = 5.0V (See Figure 2) T_A = 25°C		9.0	14	ns
Delay From Disable Input to Logical "0" Level (From High Impedance State)(t_{H0})	V_{CC} = 5.0V (See Figure 3) T_A = 25°C		13.5	16	ns

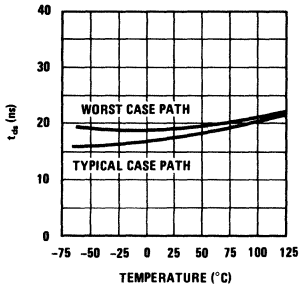
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7802, DM7806 and across the 0°C to +70°C range for the DM8802, DM8806. All typicals are given for V_{CC} = 5.0V, T_A = 25°C.

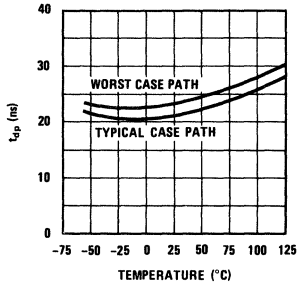
Note 3: Only one output at a time should be shorted.

typical performance characteristics

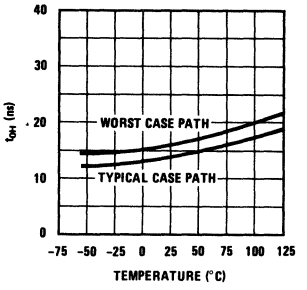
t_{ds} vs Temperature



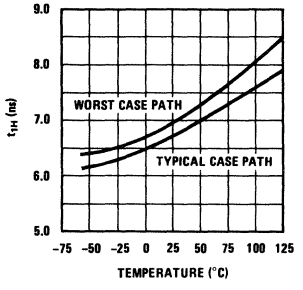
t_{dp} vs Temperature



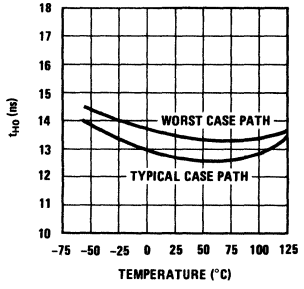
t_{0H} vs Temperature



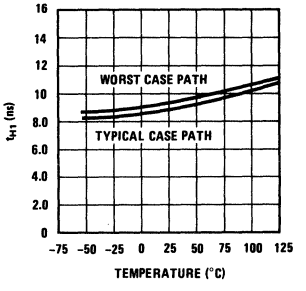
t_{1H} vs Temperature



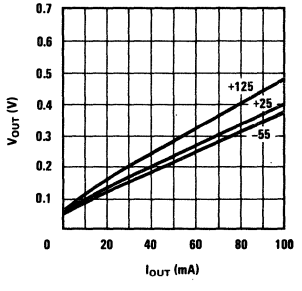
t_{H0} vs Temperature



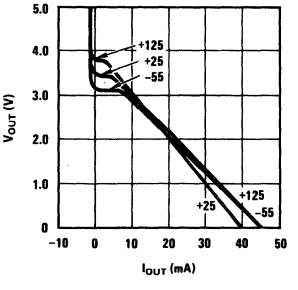
t_{H1} vs Temperature



V_{OUT} vs I_{OUT} Logical "0"



V_{OUT} vs I_{OUT} Logical "1"

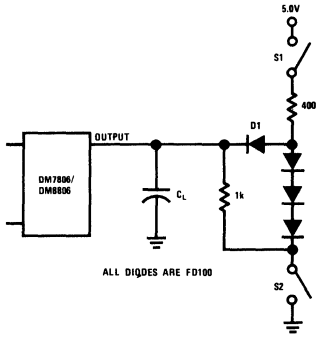


truth table

IN A OR B	ST	P	D	Q_A OR Q_B
0	1	1	0	1
1	1	1	0	1
0	0	1	0	0
1	0	1	0	1
X	X	X	1	Hi-Z

X = Don't care

ac load circuit

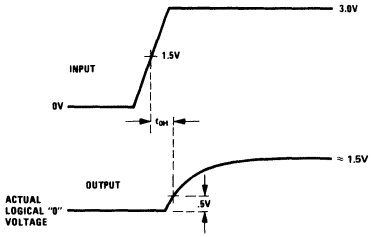


	SWITCH S_1	SWITCH S_2	C_L
t_{dp}	Closed	Closed	50 pF
t_{ds}	Closed	Closed	50 pF
t_{0H}	Closed	Closed	*5 pF
t_{1H}	Closed	Closed	*5 pF
t_{H0}	Closed	Open	50 pF
t_{H1}	Open	Closed	50 pF

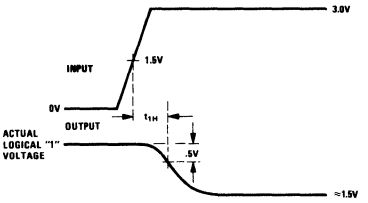
*Jig capacitance

switching time waveforms

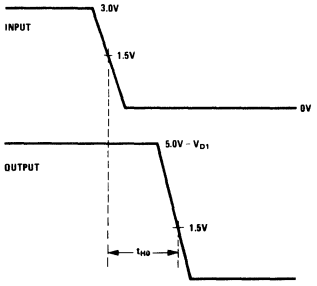
t_{0H}



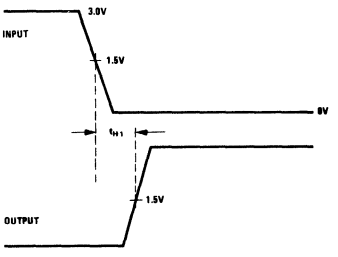
t_{1H}



t_{H0}



t_{H1}



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ac test circuits and switching time waveforms

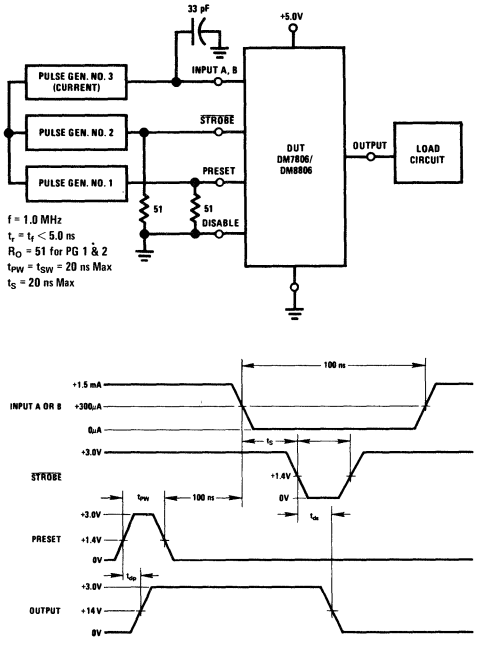


FIGURE 1. DM7802/DM8802, DM7806/DM8806 AC Test

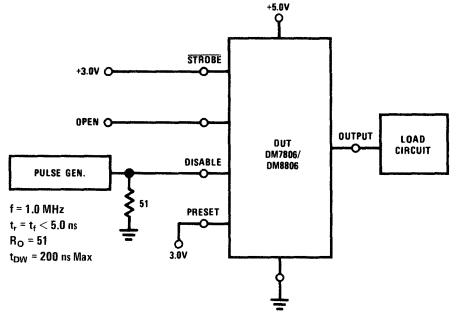


FIGURE 2. (For t_{1H}, t_{H1})

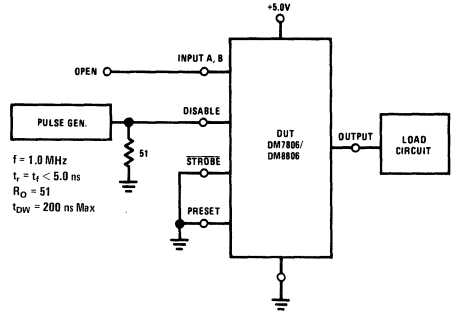


FIGURE 3. (For t_{0H}, t_{H0})

Interface Circuits

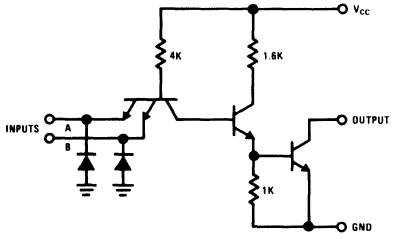
DM7810/DM8810 quad 2-input TTL-MOS interface gate
DM7811/DM8811 quad 2-input TTL-MOS interface gate
DM7812/DM8812 TTL-MOS hex inverter

general description

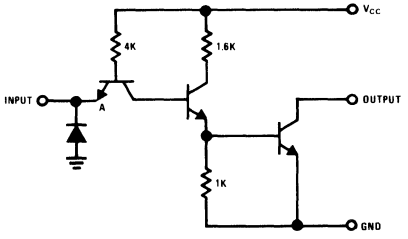
These Series 54/74 compatible gates are high output voltage versions of the DM5401/DM7401 (SN5401/SN7401), DM5403/DM7403 (SN5403/SN7403), and DM5405/DM7405 (SN5405/SN7405). Their open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

In addition the devices may be used in applications where it is desirable to drive low current relays or lamps that require up to 14 volts.

schematic and connection diagrams

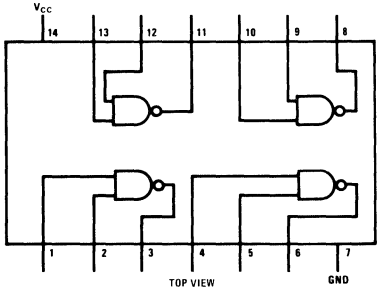


DM7810/DM8810, DM7811/DM8811



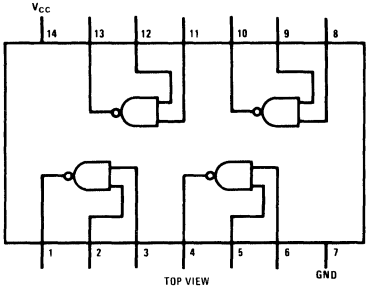
DM7812/DM8812

Dual-In-Line Package



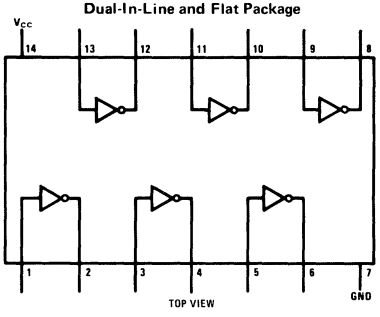
Order Number DM7810J or DM8810J
See Package 9
Order Number DM7810N or DM8810N
See Package 14

Dual-In-Line and Flat Package



Order Number DM7811J or DM8811J
See Package 9
Order Number DM7811N or DM8811N
See Package 14
Order Number DM7811W or DM8811W
See Package 27

Dual-In-Line and Flat Package



Order Number DM7812J or DM8812J
See Package 9
Order Number DM7812N or DM8812N
See Package 14
Order Number DM7812W or DM8812W
See Package 27

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absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Output Voltage	14V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

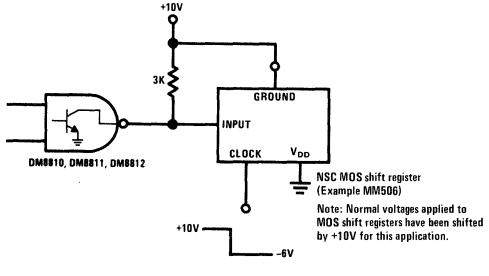
	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM78XX	4.75	5.25	V
DM88XX	4.75	5.25	V
Temperature (T_A)			
DM78XX	−55	+125	°C
DM88XX	0	70	°C

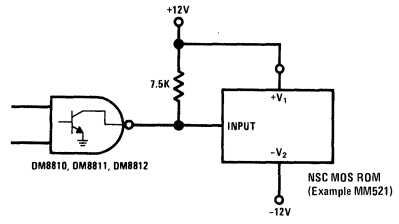
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Current	V_{CC} = Min V_{IN} = 0.8V V_{OUT} = 10V V_{IN} = 0.0V			250 40	μA μA
Logical "1" Output Breakdown Voltage	V_{CC} = Min, V_{IN} = 0V I_{OUT} = 1 mA	14			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Supply Current — Logical "0" (Each Gate)	V_{CC} = Max, V_{IN} = 5.0V		3.0	5.1	mA
Supply Current — Logical "1" (Each Gate)	V_{CC} = Max, V_{IN} = 0V		1.0	1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	4	12	18	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	18	29	45	ns

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM78XX and across the 0°C to 70°C range for the DM88XX. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

typical applications





Interface Circuits

DM8861 MOS-to-LED 5-segment driver
DM8863 MOS-to-LED 8-digit driver

general description

The DM8861 and DM8863 are designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays.

The DM8861 is a 5-segment driver capable of sinking or sourcing up to 50 mA from each driver.

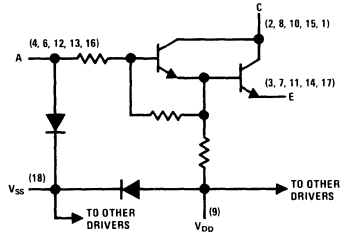
The DM8863 is an 8-digit driver. Each driver is capable of sinking up to 500 mA.

features

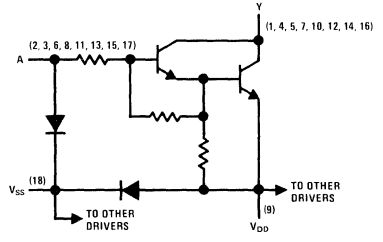
- Source or sink capability per driver, DM8861 — 50 mA
- Sink capability per driver, DM8863 — 500 mA
- MOS compatibility (low input current)
- Low standby power
- High gain Darlington circuits

schematic and connection diagrams

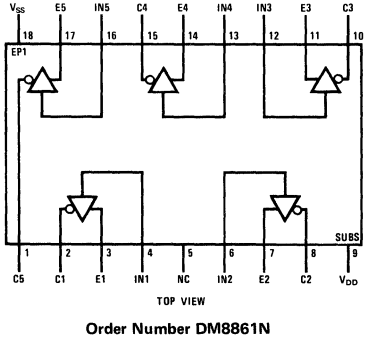
DM8861



DM8863

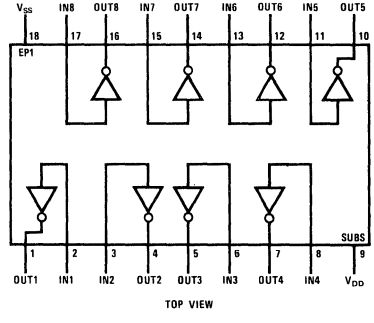


Dual-In-Line Package



Order Number DM8861N
See Package 16

Dual-In-Line Package



Order Number DM8863N
See Package 16

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absolute maximum ratings

	DM8861	DM8863
Input Voltage Range (Note 1)	−5V to V_{SS}	−5V to V_{SS}
Collector (Output) Voltage (Note 2)	10V	10V
Collector (Output)-to-Input Voltage	10V	10V
Emitter-to-Ground Voltage ($V_I \geq 5V$)	10V	
Emitter-to-Input Voltage	5V	
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V
Collector (Output) Current		
Each Collector (Output)	50 mA	500 mA
All Collectors (Output)	200 mA	600 mA
Continuous Total Dissipation	800 mW	800 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C

dc electrical characteristics

DM8861 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
On State Collector Emitter Voltage ($V_{CE\ ON}$)	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA, T_A = 25°C		.9	1.2	V
On State Collector Emitter Voltage ($V_{CE\ ON}$)	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA			1.5	V
Off State Collector Current ($I_{C\ OFF}$)	V_C = 10V, V_E = 0, I_{IN} = 40μA			100	μA
Off Set Collector Current ($I_{C\ OFF}$)	V_C = 10V, V_E = 0, V_{IN} = .7V			100	μA
Input Current at Maximum Input Voltage (I_I)	V_{IN} = 10V, V_E = 0, I_C = 20 mA		2.2	3.3	mA
Emitter Reverse Current (I_E)	V_{IN} = 0, V_E = 5V, I_C = 0			100	μA
Current Into V_{SS} Terminal (I_{SS})				1	mA

DM8863 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Low Level Output Voltage (V_{OL})	V_{IN} = 7V, I_{OUT} = 500 mA, T_A = 25°C		1.5		V
Low Level Output Voltage (V_{OL})	V_{IN} = 7V, I_{OUT} = 500 mA			1.6	V
High Level Output Current (I_{OH})	V_{OH} = 10V, I_{IN} = 40μA			250	μA
High Level Output Current (I_{OH})	V_{OH} = 10V, V_{IN} = .5V			250	μA
Input Current at Maximum Input Voltage (I_I)	V_{IN} = 10V, I_{OL} = 20 mA			2	mA
Current Into V_{SS} Terminal (I_{SS})				1	mA

ac switching characteristics

DM8861 (V_{SS} = 7.5V, T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time, Low to High Level Output (Collector) (t_{PLH})	V_{IH} = 4.5V, V_E = 0		100		ns
Propagation Delay Time, High to Low Level Output (Collector) (t_{PHL})	R_L = 200Ω, C_L = 15 pF		20		ns

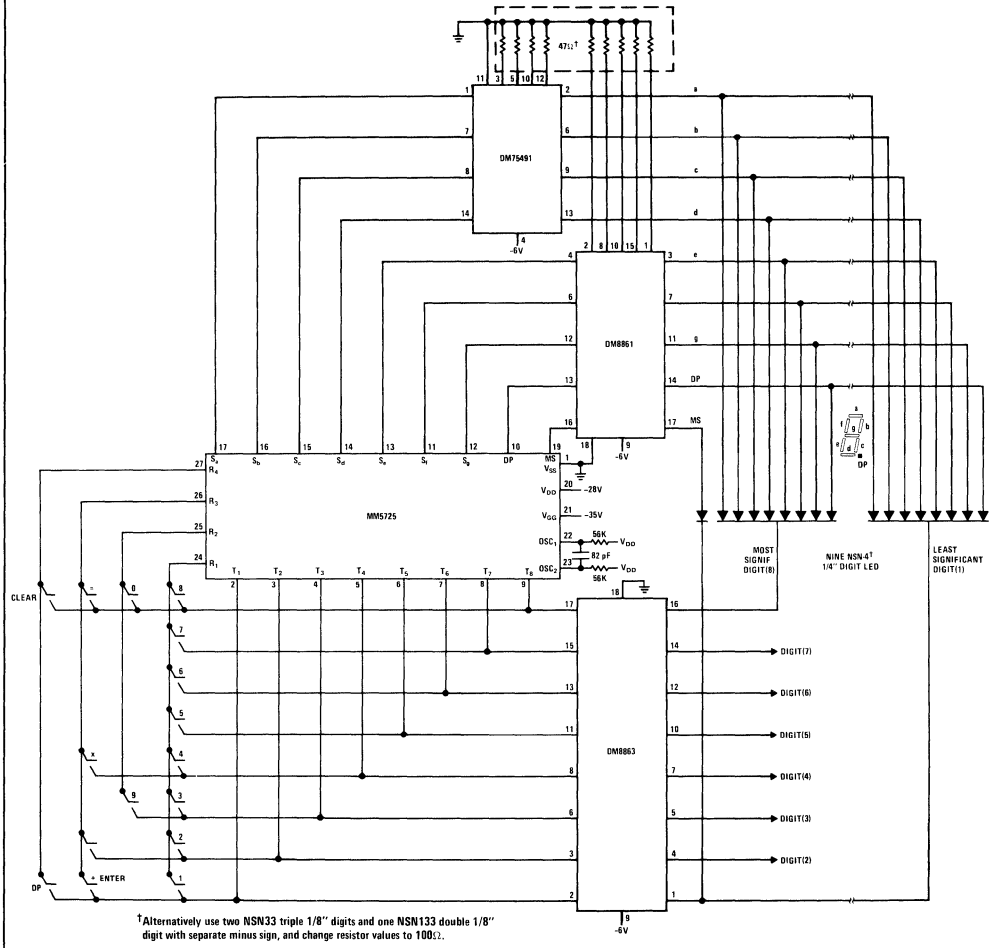
DM8863 (V_{SS} = 7.5V, T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time, Low to High Level Output (t_{PLH})	V_{IH} = 8V, R_L = 21Ω,		300		ns
Propagation Delay Time, High to Low Level Output (t_{PHL})	C_L = 15 pF		30		ns

Note 1: The input is the only device terminal which may be negative with respect to ground.
Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

typical application

8-Digit Calculator With LED Display



†Alternatively use two NSN33 triple 1/8" digits and one NSN133 double 1/8" digit with separate minus sign, and change resistor values to 100Ω.

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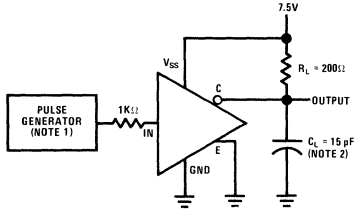
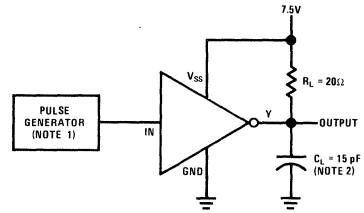
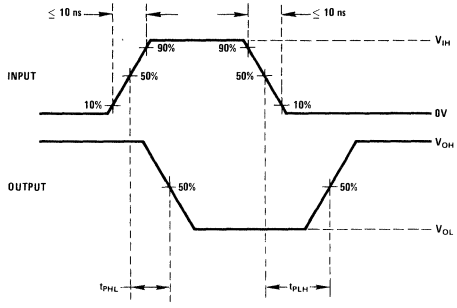
ac test circuits and waveforms



DM8861



DM8863



Note 1: The pulse generator has the following characteristics:
Z_{OUT} = 50Ω, PRR = 100 kHz, t_W = 1.0μs.
Note 2: C_L includes probe and jig capacitance.

Interface Circuits

DM8885 MOS to high voltage cathode buffer

general discription

The DM8885 interfaces MOS calculator or counter-latch-decoder-driver circuits directly to seven-segment high-voltage gas-filled displays. The six inputs A, B, D, E, F, G are decoded to drive the seven segments of the tube.

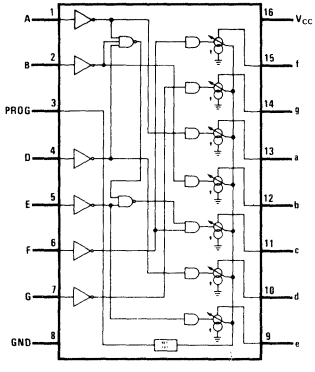
Each output constitutes a switchable, adjustable current source which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sources have a voltage compliance from 3V to at least 80V. Each current source is ratioed to the b-output current as required for even illumination of all segments. Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting a program resistor (R_P) from V_{CC} to the program input.

features

- Current source outputs
- Adjustable output currents 0.2 to 1.5 mA
- High output breakdown voltage 80V min
- Suitable for multiplex operation
- Low fan-in and low power
- Blanking via program input
- Also drives overrange, polarity, decimal point cathodes

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM8885N
See Package 15

truth tables

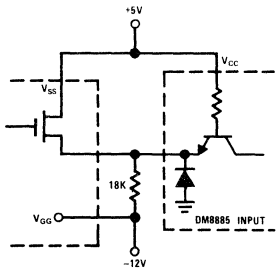
A	B	D	E	F	G	DISPLAY
1	1	1	1	1	0	0
0	1	0	0	0	0	1
1	1	1	1	0	1	2
1	1	1	0	0	1	3
0	1	0	0	1	1	4
1	0	1	0	1	1	5
1	0	1	1	1	1	6
1	1	0	0	0	0	7
1	1	1	1	1	1	8
1	1	1	0	1	1	9
0	0	1	1	1	1	b
1	1	0	0	1	1	q
1	1	0	1	1	1	A
0	1	0	1	1	1	H
0	1	1	1	1	0	U
0	0	0	0	0	1	-
0	0	0	0	0	0	

INPUT*	OUTPUT*
0	1 (OFF)
1	0 (ON)

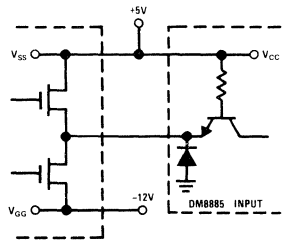
*Positive Logic

$C = (\bar{A}\cdot\bar{B}\cdot\bar{D} + E)\,F$

typical applications



Open-Drain MOS Output



Push-Pull MOS Output

absolute maximum ratings

V_{CC}	7V
Input Voltage	6V
Segment Output Voltage	80V
Power Dissipation (Note 1)	600 mW
Transient Segment Output Current (Note 2)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage	V_{CC} = 4.75V	2.0			V
Logic "0" Input Voltage	V_{CC} = 4.75V			0.8	V
Logic "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V		2	15	μA
	V_{CC} = 5.25V, V_{IN} = 5.5V		4	400	μA
Logic "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V		-300	-600	μA
Power Supply Current	V_{CC} = 5.25V, All Inputs = 0V, R_P = 2.2k		22	31	mA
Input Diode Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C		-0.9	-1.5	V
Segment Outputs:					
Outputs a, f, g On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	0.84	0.93	1.02	
Output c On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	1.12	1.25	1.38	
Output d On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	0.90	1.00	1.10	
Output e On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	0.99	1.10	1.21	
Output b On Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 18.1k	0.18	0.20	0.22	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 7.03k	0.45	0.50	0.55	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 3.40k	0.90	1.00	1.10	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 2.20k	1.35	1.50	1.65	mA
Output Saturation Voltage	V_{CC} = 4.75V, I_{OUT} b = 2 mA, R_P = 1k ± 5% (Note 4)		0.8	2.5	V
Output Leakage Current	V_{OUT} = 75V, V_{IN} = 0.8V, R_P > 1k		0.003	3	μA
	V_{OUT} = 75V, V_{PROG} = 0.4V		0.003	3	μA
Output Breakdown Voltage	I_{OUT} = 250 μA, V_{IN} = 0.8V	80	110		V
Propagation Delays:					
Input to Segment Output	V_{CC} = 5V, T_A = 25°C		0.4	10	μs

Note 1: Maximum junction temperature is 130°C. For operating at elevated temperatures, the device must be derated based on a thermal resistance of 150°C/W θ_{JA}.

Note 2: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in DC applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +70°C, unless otherwise specified. Typicals are for V_{CC} = 5V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: For saturation mode the segment output currents are externally limited and ratioed.

typical performance characteristics (see DM7880 data sheet)

Interface Circuits

DM75491 MOS-to-LED quad segment driver
DM75492 MOS-to-LED hex digit driver

general description

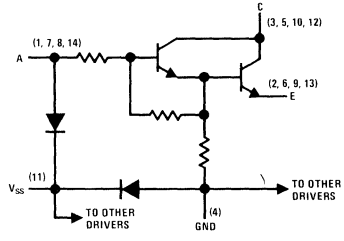
The DM75491 and DM75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

features

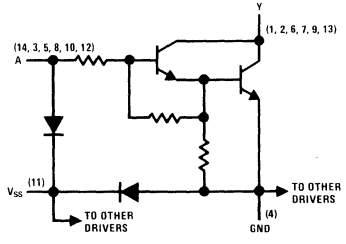
- Source or sink capability per driver (DM75491) 50 mA
- Sink capability per driver (DM75492) 250 mA
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

schematic and connection diagrams

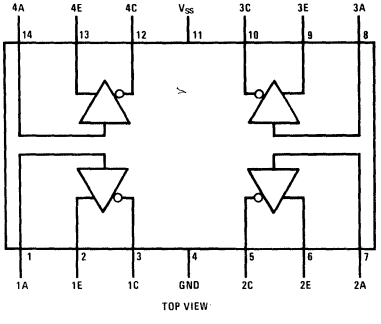
DM75491 (each driver)



DM75492 (each driver)



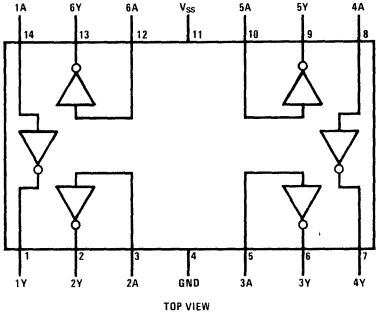
DM75491 Dual-In-Line Package



TOP VIEW

Order Number DM75491J
See Package 9
Order Number DM75491N
See Package 14

DM75492 Dual-In-Line Package



TOP VIEW

Order Number DM75492J
See Package 9
Order Number DM75492N
See Package 14

absolute maximum ratings

	DM75491	DM75492
Input Voltage Range (Note 1)	−5V to V_{SS}	−5V to V_{SS}
Collector Output Voltage (Note 2)	10V	10V
Collector Output to Input Voltage	10V	10V
Emitter to Ground Voltage ($V_I \geq 5V$)	10V	
Emitter to Input Voltage	5V	
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V
Collector Output Current		
Each Collector Output	50 mA	250 mA
All Collector Outputs	200 mA	600 mA
Continuous Total Dissipation	800 mW	800 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C

dc electrical characteristics

DM75491 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On State Collector Emitter Voltage ($V_{CE\ ON}$)	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA, T_A = 25°C		.9	1.2	V
On State Collector Emitter Voltage ($V_{CE\ ON}$)	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA			1.5	V
Off State Collector Current ($I_{C\ OFF}$)	V_C = 10V, V_E = 0, I_{IN} = 40μA			100	μA
Off State Collector Current ($I_{C\ OFF}$)	V_C = 10V, V_E = 0, V_{IN} = .7V			100	μA
Input Current at Maximum Input Voltage (I_I)	V_{IN} = 10V, V_E = 0, I_C = 20 mA		2.2	3.3	mA
Emitter Reverse Current (I_E)	V_{IN} = 0, V_E = 5V, I_C = 0			100	μA
Current Into V_{SS} Terminal (I_{SS})				1	mA

DM75492 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Level Output Voltage (V_{OL})	Input = 6.5V through 1 kΩ, I_{OUT} = 250 mA T_A = 25°C		.9	1.2	V
Low Level Output Voltage (V_{OL})	Input = 6.5V through 1 kΩ, I_{OUT} = 250 mA			1.5	V
High Level Output Current (I_{OH})	V_{OH} = 10V, I_{IN} = 40μA			200	μA
High Level Output Current (I_{OH})	V_{OH} = 10V, V_{IN} = .5V			200	μA
Input Current at Maximum Input Voltage (I_I)	V_{IN} = 10V, I_{OL} = 20 mA		2.2	3.3	mA
Current Into V_{SS} Terminal (I_{SS})				1	mA

ac switching characteristics

DM75491 (V_{SS} = 7.5V, T_A = 25°C)

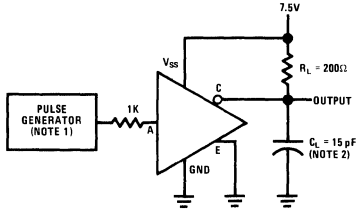
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (Collector) (t_{PLH})	V_{IH} = 4.5V, V_E = 0,		100		ns
Propagation Delay Time, High to Low Level Output (Collector) (t_{PHL})	R_L = 200Ω, C_L = 15 pF		20		ns

DM75492 (V_{SS} = 7.5V, T_A = 25°C)

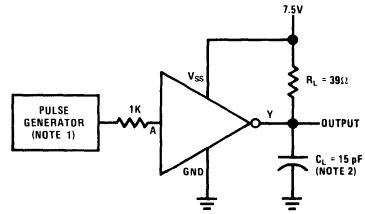
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (t_{PLH})	V_{IH} = 7.5V, R_L = 39Ω,		300		ns
Propagation Delay Time, High to Low Level Output (t_{PHL})	C_L = 15 pF		30		ns

Note 1: The input is the only device terminal which may be negative with respect to ground.
Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

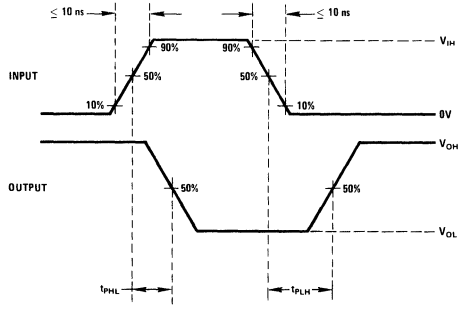
ac test circuits and switching time waveforms



DM75491



DM75492



NOTE 1: THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: Z_{OUT} = 50Ω, PRR = 100 KHz, t_W = 1 μs.

NOTE 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.

1.1

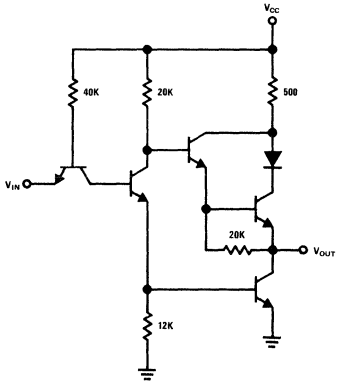
Interface Circuits

DM88L12 TTL-MOS hex inverter/ interface gate

general description

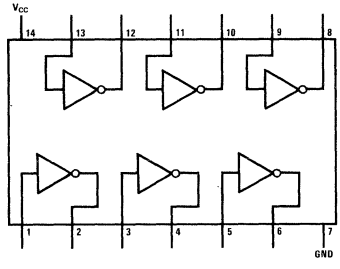
The DM88L12 is a low power TTL to MOS hex inverter element. The outputs may be "pulled up" to +14V in the logical "1" state, thus providing guaranteed interface between TTL and MOS logic levels. The gate may also be operated with V_{CC} levels up to +14V without resistive pull-ups at the outputs and still providing a guaranteed logical "1" level of V_{CC} − 2.2V with an output current of −200 μA.

schematic and connection diagrams



Note: Shown is schematic for each inverter.

Dual-In-Line and Flat Package

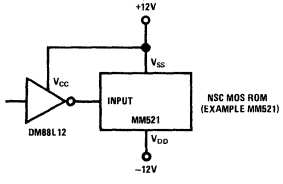


TOP VIEW

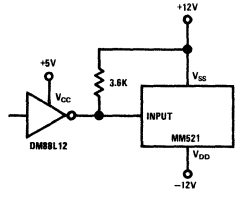
Order Number DM88L12J
See Package 9
Order Number DM88L12N
See Package 14
Order Number DM88L12F
See Package 26

typical applications

TTL Interface to MOS ROM Without Resistive Pull-Up



TTL Interface to MOS ROM With Resistive Pull-Up



ac test circuits

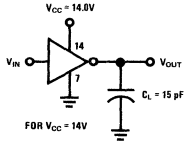


Figure 1

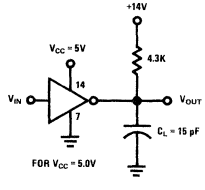
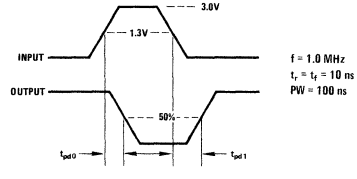


Figure 2

switching time waveforms



absolute maximum ratings (Note 1)

Supply Voltage	15V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
DM78L12	4.5	5.5	V
DM88L12	4.75	5.25	V
Temperature			
DM78L12	−55	125	°C
DM88L12	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 14.0V			2.0	1.3		V
	V_{CC} = Min			2.0	1.3		V
Logical "0" Input Voltage	V_{CC} = 14.0V				1.3	0.7	V
	V_{CC} = Min				1.3	0.7	V
Logical "1" Output Voltage	V_{CC} = 14.0V	V_{IN} = 0.7V	I_{OUT} = −200 μA	11.8	12.0		V
	V_{CC} = Min	V_{IN} = 0.7V	I_{OUT} = +200 μA	14.5	15.0		V
	V_{CC} = Min	V_{IN} = 0V	I_{OUT} = −5.0μA	V_{CC} = 1.1V			V
Logical "0" Output Voltage	V_{CC} = 14.0V	V_{IN} = 2.0V	I_{OUT} = 12 mA		0.5	1.0	V
	V_{CC} = Min	V_{IN} = 2.0V	I_{OUT} = 3.6 mA		0.2	0.4	V
Logical "1" Input Current	V_{CC} = 14.0V	V_{IN} = 2.4V			<1	20	μA
	V_{CC} = Max	V_{IN} = 2.4V			<1	10	μA
	V_{CC} = 14.0V	V_{IN} = 5.5V			<1	100	μA
	V_{CC} = Max	V_{IN} = 5.5V			<1	100	μA
Logical "0" Input Current	V_{CC} = 14.0V	V_{IN} = 0.4V			−320	−500	μA
	V_{CC} = Max	V_{IN} = 0.4V			−100	−180	μA
Output Short Circuit Current (Note 3)	V_{CC} = 14.0V	V_{OUT} = 0V		−10	−25	−50	mA
	V_{CC} = Max	V_{OUT} = 0V		−3	−8	−15	mA
Supply Current — Logical "1" (Each Inverter)	V_{CC} = 14.0V	V_{IN} = 0V			0.32	0.50	mA
	V_{CC} = Max	V_{IN} = 0V			0.11	0.16	mA
Logical "0"	V_{CC} = 14.0V	V_{IN} = 5.25V			1.0	1.5	mA
	V_{CC} = Max	V_{IN} = 5.25V			0.3	0.5	mA
Propagation Delay to a Logical "0" from Input to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	See Figure 2			27	45	ns
Propagation Delay to a Logical "0" from Input to Output, t_{pd0}	V_{CC} = 14.0V, T_A = 25°C	See Figure 1			11	20	ns
Propagation Delay to a Logical "1" from Input to Output, t_{pd1} (Note 4)	V_{CC} = 5.0V, T_A = 25°C	See Figure 2			79	100	ns
Propagation Delay to a Logical "1" from Input to Output, t_{pd1}	V_{CC} = 14.0V, T_A = 25°C	See Figure 1			34	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM78L12 and across the 0°C to +70°C range for the DM88L12. All typicals are given for V_{CC} = 5.0V and T_A = 25°C, or for V_{CC} = 14.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Note 4: t_{pd1} for V_{CC} = 5.0V is dependent upon the resistance and capacitance used.

Interface Circuits

LM139/LM239/LM339 quad comparator

general description

The LM139 series consists of four independent voltage comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM339 will directly interface with MOS logic — where the low power drain of the LM339 is a distinct advantage over standard comparators.

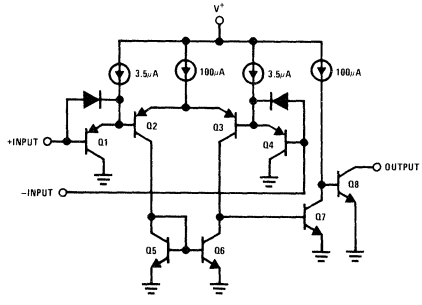
advantages

- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

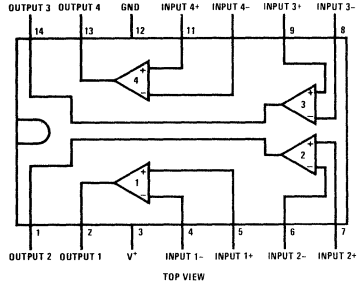
features

- Wide single supply
  Voltage range 2 V_{DC} to 36 V_{DC}
  or dual supplies ±1 V_{DC} to ±18 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage (1 mW/comparator at +5 V_{DC})
- Low input biasing current 35 nA
- Low input offset current 3 nA
  and offset voltage 3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 1 mV at 5μA
  saturation voltage 70 mV at 1 mA
- Output voltage compatible with TTL (fanout of 2), DTL, ECL, MOS and CMOS logic systems

schematic and connection diagrams

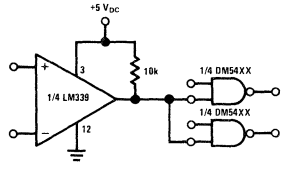


Dual-In-Line and Flat Package

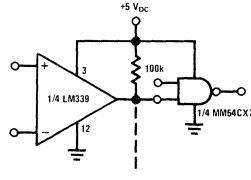


Order Number LM139D, LM239D or LM339D
See Package 2
Order Number LM339N
See Package 14
Order Number LM139F
See Package 26

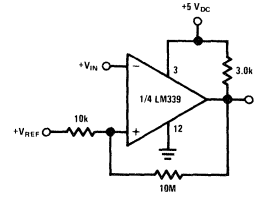
typical applications



Driving TTL



Driving CMOS



Comparator with Hysteresis

absolute maximum ratings

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Molded DIP (LM339N)	570 mW
Cavity DIP (LM139D, LM239D & LM339D)	900 mW
Flat Pack (LM139F)	800 mW
Output Short-Circuit to GND (Note 2)	Continuous
Input Current (V_{IN} < −0.3 V_{DC})(Note 3)	50 mA
Operating Temperature Range	
LM339	0°C to +70°C
LM239	−25°C to +85°C
LM139	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (V^+ = +5.0 V_{DC}, see Note 4)

PARAMETER	CONDITIONS	LM139			LM239, LM339			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	At Output Switch Point, $V_O \cong 1.4\ V_{DC}$, V_{REF} = +1.4 V_{DC} and $R_S = 0\Omega$, T_A = +25°C		±2.0	±5.0		±2.0	±5.0	mV_{DC}
Input Bias Current (Note 5)	$I_{IN(+)}$ or $I_{IN(-)}$ With Output in Linear Range, T_A = +25°C		25	100		25	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = +25°C		±3.0	±25		±5.0	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 6)	T_A = +25°C	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	$R_L = \infty$ On All Comparators T_A = +25°C		0.8	2.0		0.8	2.0	mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, T_A = +25°C		200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4 V_{DC}, V_{RL} = 5.0 V_{DC} and R_L = 5.1 kΩ		300			300		ns
Response Time (Note 7)	V_{RL} = 5.0 V_{DC} and R_L = 5.1 kΩ, T_A = +25°C		1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq +1.0\ V_{DC}$, $V_{IN(+)} = 0$ and $V_O \leq +1.5\ V_{DC}$, T_A = +25°C	6	16		6	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq +1.0\ V_{DC}$, $V_{IN(+)} = 0$ and $I_{SINK} \leq 4.0$ mA, T_A = +25°C		250	500		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq +1.0\ V_{DC}$, $V_{IN(-)} = 0$ and V_{OUT} = 5.0 V_{DC}, T_A = +25°C		0.1			0.1		nA_{DC}
Input Offset Voltage	At Output Switch Point, $V_O \cong 1.4\ V_{DC}$; V_{REF} = +1.4 V_{DC} and $R_S = 0\Omega$			9.0			9.0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ With Output in Linear Range			300			400	nA_{DC}
Input Common-Mode Voltage Range		0		V^+−2.0	0		V^+−2.0	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq +1.0\ V_{DC}$, $V_{IN(+)} = 0$ and $I_{SINK} \leq 4.0$ mA			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq +1.0\ V_{DC}$, $V_{IN(-)} = 0$ and V_{OUT} = 30 V_{DC}			1.0			1.0	μA_{DC}
Differential Input Voltage (Note 8)	Keep All V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used)			36			36	V_{DC}

Note 1: For operating at high temperatures, the LM339 must be derated based on a +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a +150°C maximum junction temperature. The low bias dissipation on the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC}.

Note 4: These specifications apply for V^+ = +5.0 V_{DC} and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM239, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C and the LM339 temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.

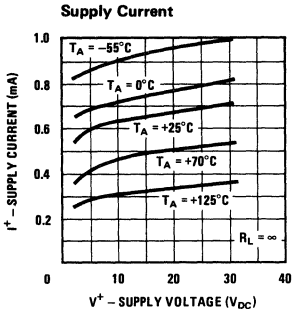
Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

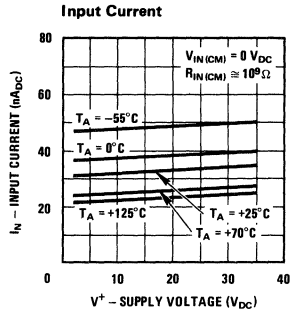
Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ − 1.5V, but either or both inputs can go to +30 V_{DC} without damage.

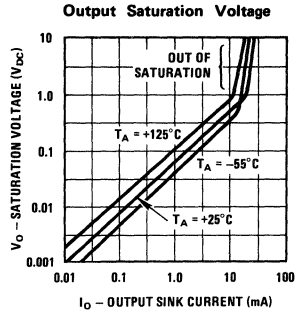
Note 7: The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

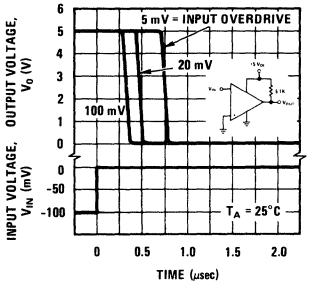
Note 8: The positive excursions of the inputs can exceed the power supply voltage level, and if the other input voltage remains within the common-mode voltage range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply voltage, if used).

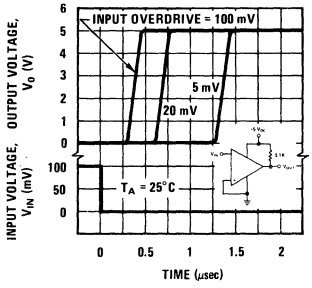
typical performance characteristics











application hints

The LM139 is a high gain, wide bandwidth device; which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $<10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

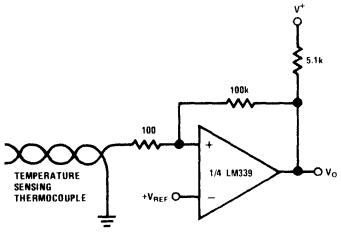
The bias network of the LM139 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $2V_{DC}$ to $30\ V_{DC}$.

It is usually unnecessary to use a bypass capacitor across the power supply line.

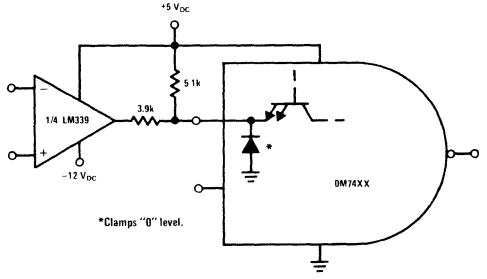
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode and input resistor can be used as shown in the applications section.

The output of the LM139 is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139 package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

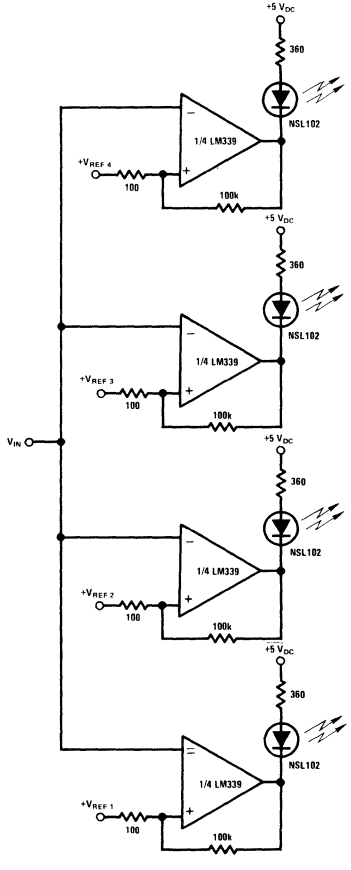
typical applications (con't)



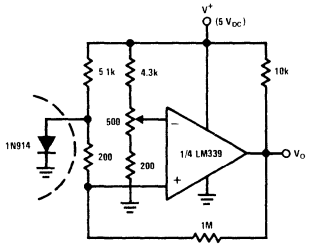
Ground Referenced Thermocouple in Single Supply System



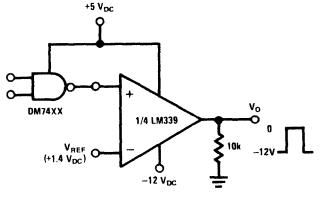
MOS to TTL Logic Translator



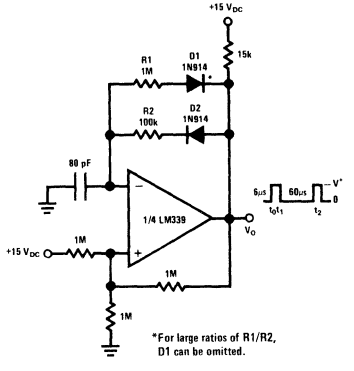
Visible Voltage Indicator



Remote Temperature Sensing



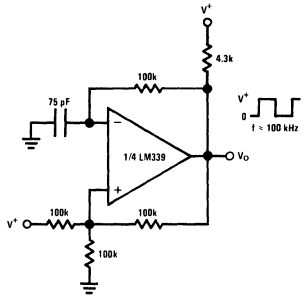
TTL to MOS Logic Converter



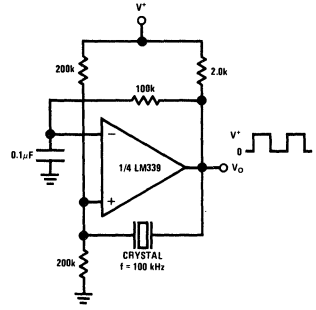
*For large ratios of R1/R2, D1 can be omitted.

Pulse Generator

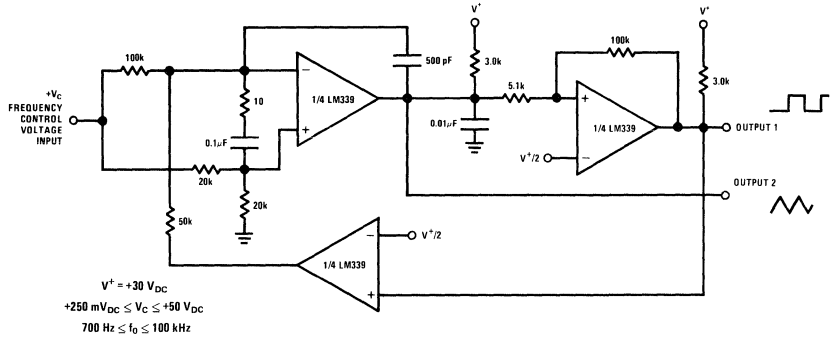
typical applications (con't)



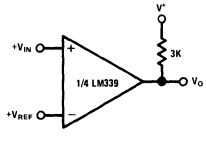
Squarewave Oscillator



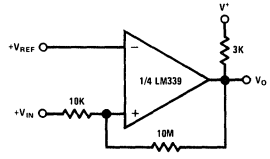
Crystal Controlled Oscillator



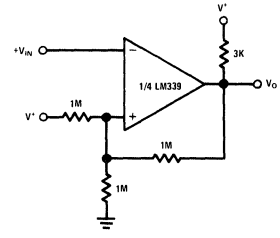
Two-Decade High-Frequency VCO



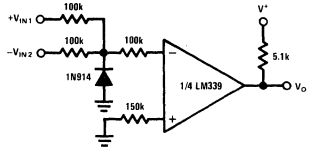
Basic Comparator



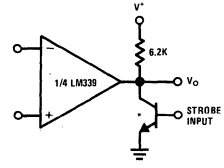
Non-Inverting Comparator with Hysteresis



Inverting Comparator with Hysteresis



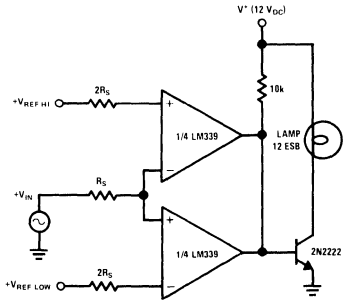
Comparing Input Voltages of Opposite Polarity



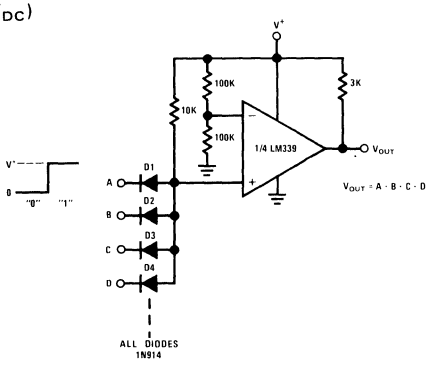
*OR logic gate without pull-up resistor.

Output Strobing

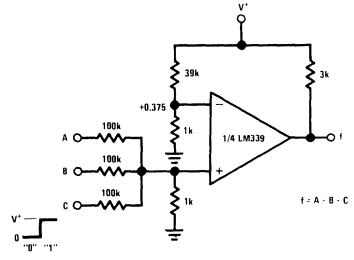
typical applications (con't) ($V^+ = 15\ V_{DC}$)



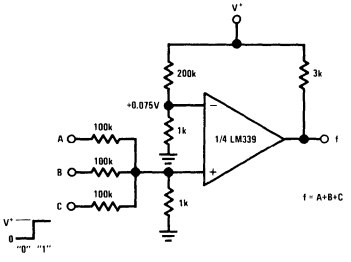
Limit Comparator



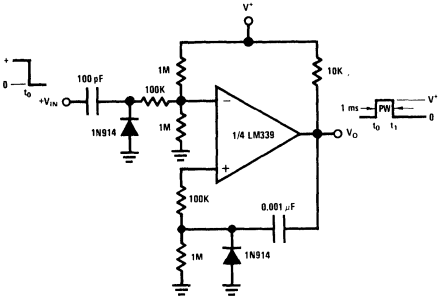
Large Fan-in AND Gate



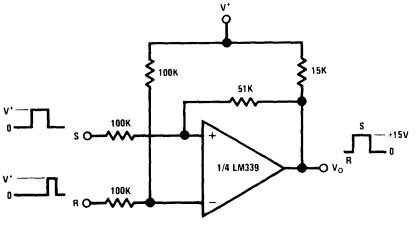
AND Gate



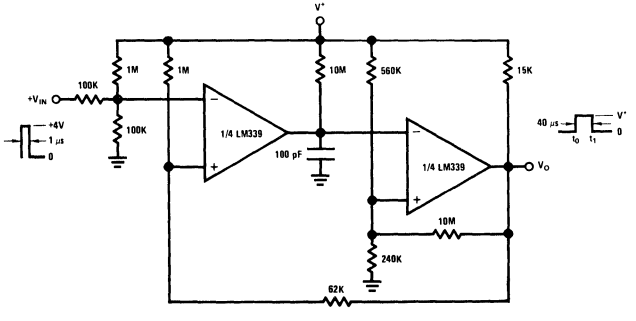
OR Gate



One-Shot Multivibrator

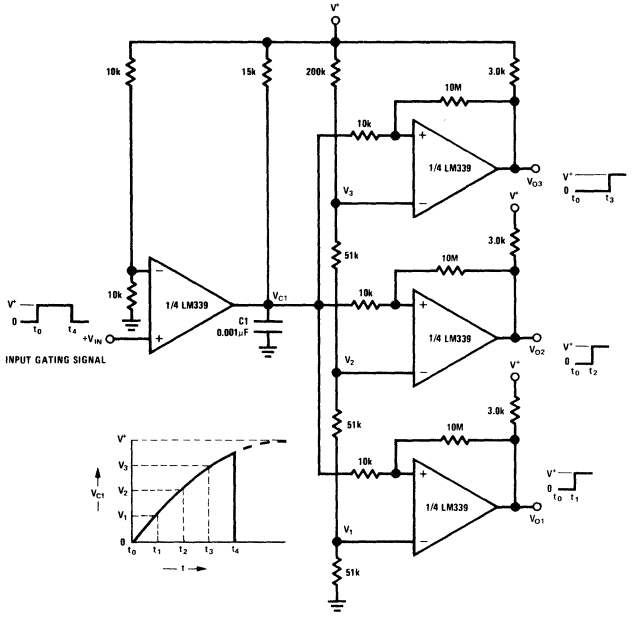


Bi-Stable Multivibrator

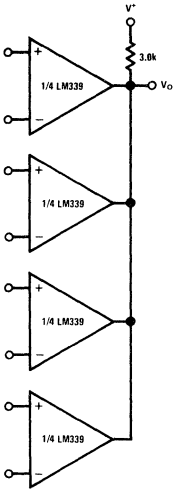


One-Shot Multivibrator with Input Lock Out

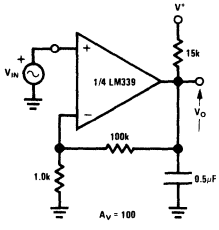
typical applications (con't) ($V^+ = 15\ V_{DC}$)



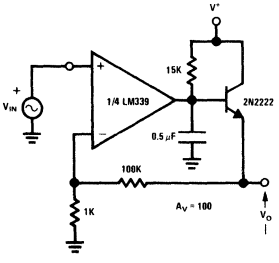
Time Delay Generator



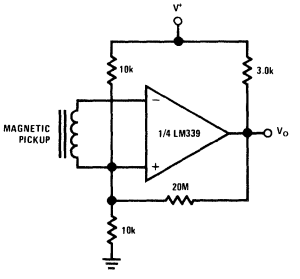
ORing the Outputs



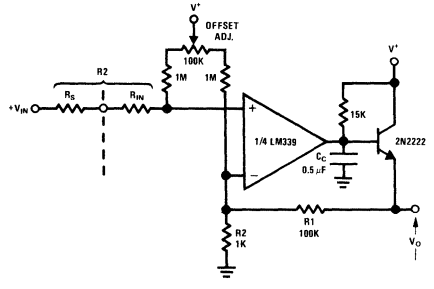
Low Frequency Op Amp



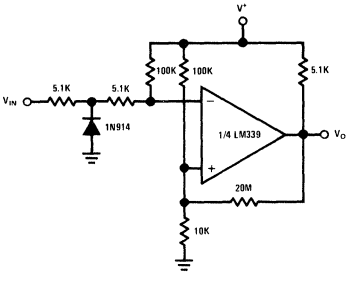
Low Frequency Op Amp
($V_O = 0V$ for $V_{IN} = 0V$)



Transducer Amplifier

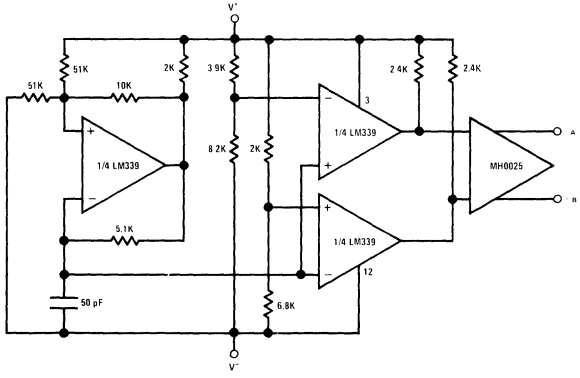


Low Frequency Op Amp with Offset Adjust

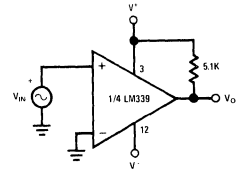


Zero Crossing Detector (Single Power Supply)

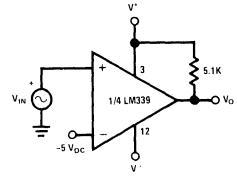
split-supply applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)



MOS Clock Driver



Zero Crossing Detector



Comparator With a Negative Reference

Interface Circuits

LM55107A/LM75107A,LM55108A/LM75108A, LM163/LM363 dual line receivers LM75207,LM75208,LM363A dual MOS sense amplifiers

general description

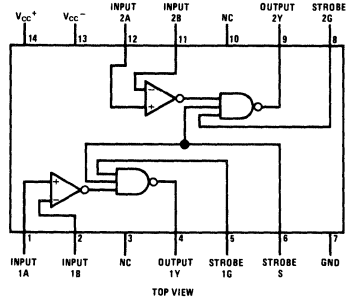
The nine products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers or MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the LM55109/LM75109 and LM55110/LM75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the LM75207, LM75208 and LM363A make them ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators. TRI-STATE® products enhance bused organizations.

features

- High speed 17 ns typ
- TTL compatible
- Input sensitivity ±10 mV or ±25 mV
- Input common-mode range ±3V
- High input impedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- TRI-STATE outputs for high speed buses
- Dual circuits
- Sensitivity guaranteed over full common-mode range
- Logic input clamp diodes
- 14 pin cavity or molded dual-in-line package
- Standard supply voltages ±5V

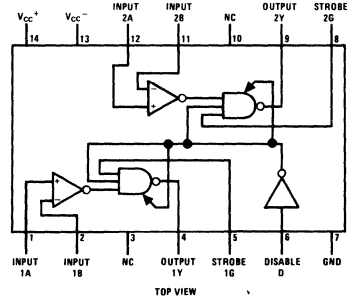
connection diagrams

Dual-In-Line Package



Order Number LM55107AJ, LM75107AJ, LM55108AJ, LM75108AJ, LM75207J or LM75208J
See Package 9
Order Number LM75207N or LM75208N
See Package 14

Dual-In-Line Package



Order Number LM163J, LM363J or LM363AJ
See Package 9
Order Number LM163N, LM363N or LM363AN
See Package 14

product selection guide

TEMPERATURE→ / PACKAGE→	$-55°C \leq T_A \leq +125°C$ CAVITY DIP	$0°C \leq T_A \leq +70°C$ CAVITY OR MOLDED DIP	
INPUT SENSITIVITY→ / OUTPUT LOGIC↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-up TTL Open Collector TTL TRI-STATE	LM55107A LM55108A LM163	LM75107A LM75108A LM363	LM75207 LM75208 LM363A

absolute maximum ratings

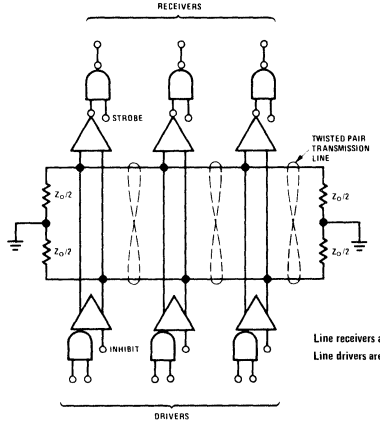
Supply Voltage, V_{CC}^+	7V	Strobe Input Voltage	5.5V
Supply Voltage, V_{CC}^-	−7V	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	±6V	Power Dissipation	600 mW
Common Mode Input Voltage	±5V	Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	LM55107A, LM55108A, LM163			LM75107A, LM75207 LM75108A, LM75208 LM363, LM363A		
	MIN	NOM	MAX	MIN	NOM	MAX
Supply Voltage V_{CC}^+	4.5V	5V	5.5V	4.75V	5V	5.25V
Supply Voltage V_{CC}^-	−4.5V	−5V	−5.5V	−4.75V	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

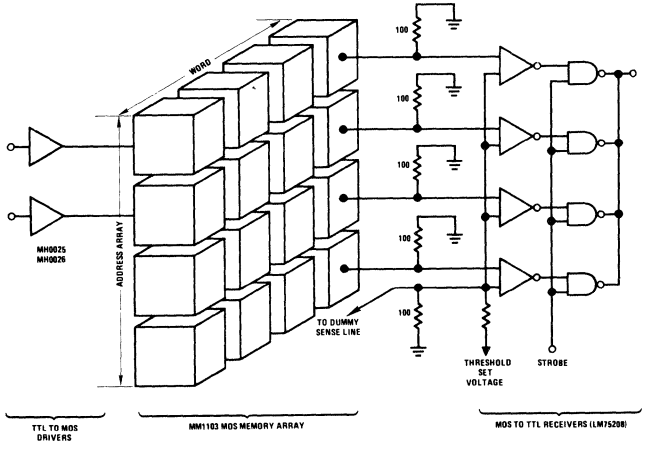
typical applications

Line Receiver Used in a Party-Line or Data-Bus System



Line receivers are LM75107/LM75108 or LM163.
Line drivers are LM55109/LM55110 or DM7831.

Line Receiver Used in MOS Memory System



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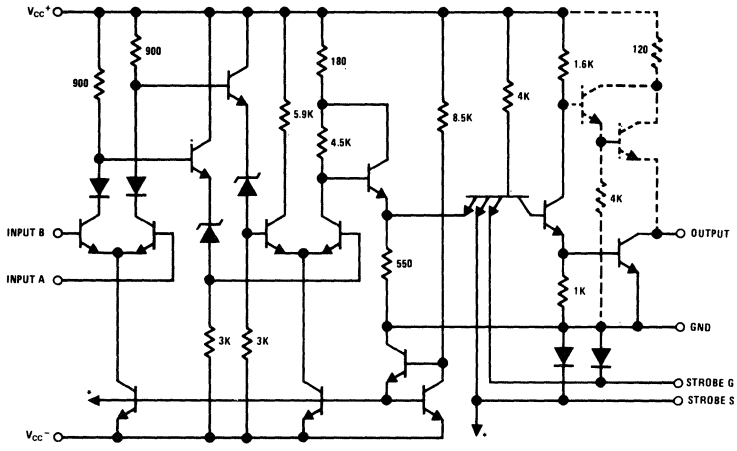
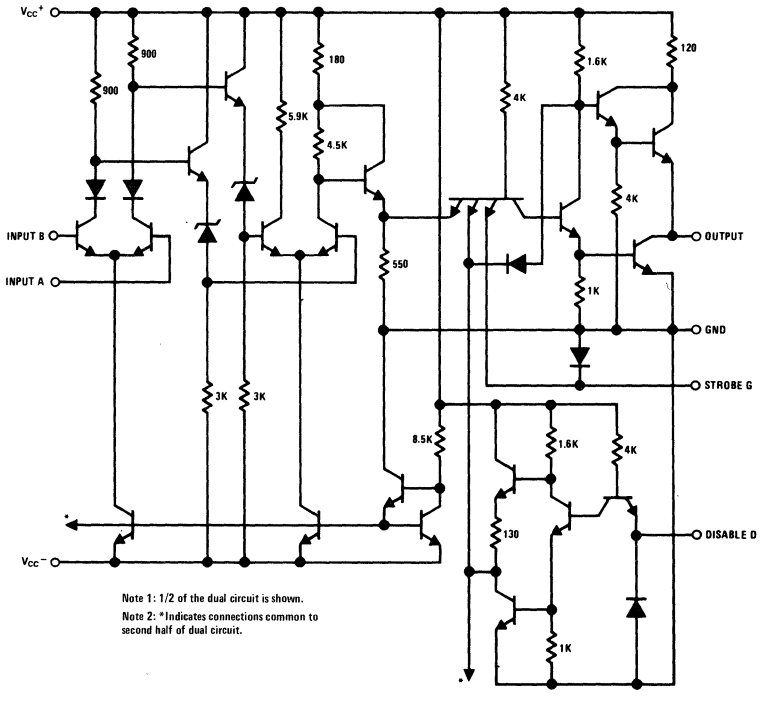
schematic diagrams

LM55107A/LM75107A, LM75207
LM55108A/LM75108A, LM75208



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit.
Note 3: Components shown with dash lines are applicable to the LM55107A, LM75107A, and LM75207 only.

LM163/LM363, LM363A



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit.

LM55107A/LM75107A, LM55108A/LM75108A

dc electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55107A/LM75107A			LM55108A/LM75108A			
		MIN	TYP	MAX	MIN	TYP	MAX	
High Level Input Current Into 1A, 1B, 2A or 2B (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V		30	75		30	75	μA
Low Level Input Current Into 1A, 1B, 2A or 2B (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = −3V to 3V			−10			−10	μA
High Level Input Current Into 1G or 2G (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2.4V			40			40	μA
High Level Input Current Into 1G or 2G (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			1			1	mA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(S)}$ = 0.4V			−1.6			−1.6	mA
High Level Input Current Into S (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2.4V			80			80	μA
High Level Input Current Into S (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			2			2	mA
Low Level Input Current Into S (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(S)}$ = 0.4V			−3.2			−3.2	mA
High Level Output Voltage (V_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −400μA, V_{ID} = 25 mV, V_{IC} = −3V to 3V	2.4						V
Low Level Output Voltage (V_{OL})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, V_{IC} = −3V to 3V			0.4			0.4	V
High Level Output Current (I_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min V_{OH} = Max V_{CC}^+						250	μA
Short Circuit Output Current (I_{OS})	V_{CC}^+ = Max, V_{CC}^- = Max	−18		−70				mA
High Logic Level Supply Current From V_{CC} (I_{CCH}^+)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C		18	30		18	30	mA
High Logic Level Supply Current From V_{CC} (I_{CCH}^-)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C		−8.4	−15		−8.4	−15	mA
Input Clamp Voltage on G or S (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1.5		−1	−1.5	V

ac switching characteristics (V_{CC}^+ = 5V, V_{CC}^- = −5V, T_A = 25°C)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55107A/LM75107A			LM55108A/LM75108A			
		MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 390Ω, C_L = 50 pF		17	25				ns
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 390Ω, C_L = 15 pF					19	25	ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 390Ω, C_L = 50 pF		17	25				ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 390Ω, C_L = 15 pF					19	25	ns
Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output ($t_{PLH(S)}$)	R_L = 390Ω, C_L = 50 pF		10	15				ns
Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output ($t_{PLH(S)}$)	R_L = 390Ω, C_L = 15 pF					13	20	ns
Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output ($t_{PHL(S)}$)	R_L = 390Ω, C_L = 50 pF		8	15				ns
Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output ($t_{PHL(S)}$)	R_L = 390Ω, C_L = 15 pF					13	20	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

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LM75207, LM75208
dc electrical characteristics ($0°C \leq T_A \leq +70°C$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM75207			LM75208			
		MIN	TYP	MAX	MIN	TYP	MAX	
High Level Input Current Into 1A, 1B, 2A or 2B (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V		30	75		30	75	μA
Low Level Input Current Into 1A, 1B, 2A or 2B (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = −3V to 3V			−10			−10	μA
High Level Input Current Into 1G or 2G (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2.4V			40			40	μA
High Level Input Current Into 1G or 2G (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			1			1	mA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(S)}$ = 0.4V			−1 6			−1 6	mA
High Level Input Current Into S (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2.4V			80			80	μA
High Level Input Current Into S (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			2			2	mA
Low Level Input Current Into S (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(S)}$ = 0.4V			−3.2			−3.2	mA
High Level Output Voltage (V_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −400μA, V_{ID} = 10 mV, V_{IC} = −3V to 3V	2 4						V
Low Level Output Voltage (V_{OL})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, V_{IC} = −3V to 3V			0 4			0.4	V
High Level Output Current (I_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min V_{OH} = Max V_{CC}^+						250	μA
Short Circuit Output Current (I_{OS})	V_{CC}^+ = Max, V_{CC}^- = Max	−18		−70				mA
High Logic Level Supply Current From V_{CC} (I_{CCH}^+)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 10 mV, T_A = 25°C		18	30		18	30	mA
High Logic Level Supply Current From V_{CC} (I_{CCH}^-)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 10 mV, T_A = 25°C		−8.4	−15		−8.4	−15	mA
Input Clamp Voltage on G or S (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1.5		−1	−1.5	V

ac switching characteristics ($V_{CC}^+ = 5V$, $V_{CC}^- = -5V$, $T_A = 25°C$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM75207			LM75208			
		MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 470Ω, C_L = 15 pF			35				ns
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 470Ω, C_L = 15 pF						35	ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to output (Note 1) ($t_{PHL(D)}$)	R_L = 470Ω, C_L = 15 pF			20				ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 470Ω, C_L = 15 pF						20	ns
Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output ($t_{PLH(S)}$)	R_L = 470Ω, C_L = 15 pF			17				ns
Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output ($t_{PLH(S)}$)	R_L = 470Ω, C_L = 15 pF						17	ns
Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output ($t_{PHL(S)}$)	R_L = 470Ω, C_L = 15 pF			17				ns
Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output ($t_{PHL(S)}$)	R_L = 470Ω, C_L = 15 pF						17	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.

LM163/LM363

dc electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	LIMITS LM163/LM363 MIN	TYP	MAX	UNITS
High Level Input Current Into 1A, 1B, 2A or 2B (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V		30	75	μA
Low Level Input Current Into 1A, 1B, 2A or 2B (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = −3V to 3V			−10	μA
High Level Input Current Into 1G, 2G or D (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2.4V			40	μA
High Level Input Current Into 1G, 2G or D (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			1	mA
Low Level Input Current Into D (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0.4V			−1.6	mA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, $V_{IL(G)}$ = 0.4V			−40	μA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0.8V, $V_{IL(G)}$ = 0.4V			−1.6	mA
High Level Output Voltage (V_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −2 mA, V_{ID} = 25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V	2.4			V
Low Level Output Voltage (V_{OL})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V			0.4	V
Output Disable Current (I_{OD})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, V_{OUT} = 2.4V			40	μA
Output Disable Current (I_{OD})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, V_{OUT} = 0.4V			−40	μA
Short Circuit Output Current (I_{OS})	V_{CC}^+ = Max, $V_{IL(D)}$ = 0.8V, V_{CC}^- = Max	−18		−70	mA
High Logic Level Supply Current From V_{CC}^+ (I_{CCH}^+)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C		28	40	mA
High Logic Level Supply Current From V_{CC}^- (I_{CCH}^-)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C		−8.4	−15	mA
Input Clamp Voltage on G or D (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1.5	V

ac switching characteristics (V_{CC}^+ = 5V, V_{CC}^- = −5V, T_A = 25°C)

PARAMETER	CONDITIONS	LIMITS LM163/LM363 MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 390Ω, C_L = 50 pF		17	25	ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 390Ω, C_L = 50 pF		17	25	ns
Propagation Delay Time, Low to High Level, From Strobe Input G to Output ($t_{PLH(S)}$)	R_L = 390Ω, C_L = 50 pF		10	15	ns
Propagation Delay Time, High to Low Level, From Strobe Input G to Output ($t_{PHL(S)}$)	R_L = 390Ω, C_L = 50 pF		8	15	ns
Disable Low to High to Output High to Off (t_{1H})	R_L = 390Ω, C_L = 5 pF			20	ns
Disable Low to High to Output Low to Off (t_{0H})	R_L = 390Ω, C_L = 5 pF			30	ns
Disable High to Low to Output Off to High (t_{H1})	R_L = 1k to 0V, C_L = 50 pF			25	ns
Disable High to Low to Output Off to Low (t_{H0})	R_L = 390Ω, C_L = 50 pF			25	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

LM363A
dc electrical characteristics ($0°C \leq T_A \leq +70°C$)

PARAMETER	CONDITIONS	LIMITS LM363A MIN	LIMITS LM363A TYP	LIMITS LM363A MAX	UNITS
High Level Input Current Into 1A, 1B, 2A or 2B (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V		30	75	μA
Low Level Input Current Into 1A, 1B, 2A or 2B (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = −3V to 3V			−10	μA
High Level Input Current Into 1G, 2G or D (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2.4V			40	μA
High Level Input Current Into 1G, 2G or D (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			1	mA
Low Level Input Current Into D (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0.4V			−1.6	mA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, $V_{IL(G)}$ = 0.4V			−40	μA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0.8V, $V_{IL(G)}$ = 0.4V			−1.6	mA
High Level Output Voltage (V_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −2 mA, V_{ID} = 10 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V	2.4			V
Low Level Output Voltage (V_{OL})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V			0.4	V
Output Disable Current (I_{OD})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, V_{OUT} = 2.4V			40	μA
Output Disable Current (I_{OD})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, V_{OUT} = 0.4V			−40	μA
Short Circuit Output Current (I_{OS})	V_{CC}^+ = Max, $V_{IL(D)}$ = 0.8V, V_{CC}^- = Max	−18		−70	mA
High Logic Level Supply Current From V_{CC}^+ (I_{CCH}^+)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 10 mV, T_A = 25°C		28	40	mA
High Logic Level Supply Current From V_{CC}^- (I_{CCH}^-)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 10 mV, T_A = 25°C		−8.4	−15	mA
Input Clamp Voltage on G or D (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1.5	V

ac switching characteristics ($V_{CC}^+ = 5V$, $V_{CC}^- = -5V$, $T_A = 25°C$)

PARAMETER	CONDITIONS	LIMITS LM363A MIN	LIMITS LM363A TYP	LIMITS LM363A MAX	UNITS
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 470Ω, C_L = 15 pF			35	ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 470Ω, C_L = 15 pF			20	ns
Propagation Delay Time, Low to High Level, From Strobe Input G to Output ($t_{PLH(S)}$)	R_L = 470Ω, C_L = 15 pF			17	ns
Propagation Delay Time, High to Low Level, From Strobe Input G to Output ($t_{PHL(S)}$)	R_L = 470Ω, C_L = 15 pF			17	ns
Disable Low to High to Output High to Off (t_{1H})	R_L = 470Ω, C_L = 5 pF			20	ns
Disable Low to High to Output Low to Off (t_{0H})	R_L = 470Ω, C_L = 5 pF			30	ns
Disable High to Low to Output Off to High (t_{H1})	R_L = 1k to 0V, C_L = 15 pF			25	ns
Disable High to Low to Output Off to Low (t_{H0})	R_L = 470Ω, C_L = 15 pF			25	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Microprocessors

INTRODUCTION

National Semiconductor produces a family of Microprocessors built around the MM5750 and MM5751 LSI processor building blocks described in this section. Because this family spans a range from chip sets thru card assemblies to complete microcomputer systems, National can support the microprocessor user at any desired level of building complexity.

The microprocessor assemblies and systems presently available are described below. Software support for these products includes both resident and cross-assemblers; as well as debug programs, relocating loaders, and diagnostics.

16-BIT PRODUCTS

IMP-16C/200, IMP-16C/300: These are complete microprocessors on 8 1/2" x 11" PC cards. They include those architectural features described in the MM5750 and MM5751 data sheets, as well as:

- 256 words of Read/Write Memory
- Sockets for 512 words of PROM
- Interrupt Capability
- Conditional Jump and User Flag Logic

The IMP-16C/200 has a 43-instruction set, with one empty socket to accept a second CROM which extends the set to 60 instructions. The IMP-16C/300 includes both CROM's for a full 60-instruction set. That is the only difference between the two.

IMP-16L/300: This is a microprocessor card similar to the IMP-16C cards described above, but without any on-card memory. Other differences include:

- Direct Memory Access Capability
- Vectored Priority Interrupt Logic
- Single-Bus I/O Structure

This card is supplied with two CROM's, providing a 60-instruction set.

IMP-16P/304, IMP-16P/308: The IMP-16P's are prototyping systems to aid the IMP-16C card or chip set user in the development of interfaces and applications software. They include a IMP-16C card, chassis, front panel, power supply, 4k or 8k of Read/Write Memory, and interfaces for TTY and card reader. A resident assembler and other system software are supplied with the IMP-16P.

IMP-16L/304, IMP-16L/308: These IMP-16L systems are prototyping tools to aid the IMP-16L card user in the development of interfaces and applications software. They include a IMP-16L card, 4k or 8k of Read/Write Memory, and a TTY interface. A resident assembler and other system software are supplied with the IMP-16L.

8-BIT PRODUCTS

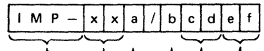
IMP-8C/200: This is a complete microprocessor on an 8 1/2" x 11" PC card. It includes those architectual features described in the MM5750 and MM5751 data sheets, as well as:

- 256 bytes of Read/Write Memory
- Sockets for 2k bytes of PROM
- Interrupt Capability
- Conditional Jump and User Flag Logic

IMP-8P/208: This is a prototyping system to aid the IMP-8C card or chip set user in the development of interfaces and applications software. It includes an IMP-8C card, a chassis, front panel, power supply, 8k bytes of Read/Write Memory, and interfaces for TTY and card reader. System software is supplied with the system.

For more detailed information on the above products, request a Product Description from your local sales representative.

IMP-SERIES PRODUCT NUMBER SYSTEM



FAMILY NAME

THIS DESIGNATOR IS THE SAME FOR ALL MEMBERS OF THE FAMILY

NUMBER OF BITS

4, 8, 16, ETC. FOR ITEMS NOT ASSOCIATED WITH FIXED WORD LENGTH, USE '00'.

MAJOR DEVICE CODE

THIS FIELD INDICATES THE MAJOR DEVICE WITH WHICH THE PARTICULAR ITEM IS ASSOCIATED.

C – IMP – 16C CARD
L/P – SYSTEMS & ASSOCIATED COMPONENTS
A – COMPONENTS THAT CUT ACROSS CARD OR SYSTEM LINES.
S – SOFTWARE
H – MECHANICAL HDWR. THAT CUTS ACROSS CARD/SYSTEM LINES.
F – FIRMWARE

SUB – CODE EXPANSION

e IS EXPANSION FOR HDWR, REV LEVEL FOR MANUALS. SEE NEXT SHEET FOR SFTWR.

DEVICE SUB – CODE

THE MEANING OF THIS FIELD IS DEPENDENT UPON THE DEVICE OR CLASS CODE.

MEMORIES

SIZE OF MEMORY (IN WORDS x1k FOR CARDS, x100 FOR CHIPS

CARDS / SYSTEMS

AMOUNT OF MEMORY IN THE SYSTEM, IN 1k INCREMENTS. SYSTEMS WITH LESS THAN 1k OF MEMORY (LIKE IMP-16C) WILL USE '00'.

SOFTWARE / MANUALS

NUMBER SEQUENTIALLY, START AT 00 IN ORDER OF RELEASE.

PERIPHERALS / HDWR

00-09 – BTC & GEN'L OPTIONS
10-19 – TTY's & PRINTERS
20-29 – CARD EQUIP.
30-39 – MAG. TAPES
40-49 – DISCS
50-59 – PAPER TAPE
60-69 – DATA COM
70-79 – ADC/DAC, ETC.
80-89 – POWER, CHASSIS, & MOUNTING
90-99 – CABLES & MISC.

DEVICE CLASS CODE or **SOFTWARE CLASS CODE**

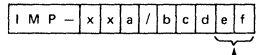
FIELD INDICATES A CLASS OF DEVICE ASSOCIATED WITH SOME MAJOR CATEGORY ABOVE.

0 – MEMORY
1 – DEVICE/SYSTEM WITHOUT SPACE FOR EXTENDED CROM.
2 – DEVICE/SYSTEM WITH SOCKET FOR EXTENDED CROM.
3.– DEVICE/SYSTEM WITH EXTENDED CROM.
4,7 – UNUSED AT PRESENT.
8 – PERIPHERAL OR CHASSIS PART.
9 – HARDWARE MANUAL.
5 – CHIP SETS.
6 – DICE.

FIELD INDICATES CLASS OF SOFTWARE WITHIN A WORD SIZE. USE THESE CODES IF DEVICE CODE IS "S" ONLY.

0 – UTILITY ROUTINES
1 – ASSEMBLERS
2 – COMPILERS & INTERPRETERS
3 – OPERATING SYSTEMS
4 – MATH ROUTINES
5 – DIAGNOSTICS
6 – APPLICATION PROGRAMS
9 – SFTWR PACKAGES INCLUDING SFTWR. MANUALS.

SOFTWARE SUB-CODES



USE THIS SET OF SUB-CODES FOR SOFTWARE AND LISTINGS ONLY. (a = S)

(e) – MEDIUM

A – LISTING
B – SOURCE P. TAPE
C – OBJ. P. TAPE
D – SOURCE 7TK M.T., 556BPI
E – OBJ. 7TK M.T., 556BPI
F – SOURCE 7TK M.T., 800 BPI
G – OBJ 7TK M.T., 800 BPI
H – SOURCE 9TK N.T., 800 BPI
I – OBJ 9TK M.T., 800 BPI
J – SOURCE 9TK M.T., 1600 BPI
K – OBJ 9TK M.T., 1600 BPI
L – SOURCE CASSETTE
M – OBJ CASSETTE
N – SOURCE ON DISC
O – OBJ ON DISC
R – V AVAILABLE
W – USER WRITE-UP
P – SOURCE CARDS
Q – OBJ CARDS
Y – MANUAL

(f) – REVISION

REV. LEVELS ARE ASSIGNED SEQUENTIALLY STARTING WITH (A).
A – W NORMAL RELEASE
X – PRE-RELEASE
Z – OBSOLETE; AVAIL. FOR REPLACEMENT ONLY

IMP-SERIES MICROPROCESSORS LIST

MODEL	PRODUCT DESCRIPTION
	IMP-16L HARDWARE
IMP-16L/300	16-bit microprocessor on 8-1/2 x 11" printed circuit card. Includes the following features: • Extended Instruction Set (60 instructions) • Direct Memory Access Logic • Priority Interrupt Logic • Address Capability for 65k of Memory
IMP-16L/304	16-bit, Microcomputer prototyping system to aid the system designer in working with the IMP-16L microprocessor card. Includes: • IMP-16L/300 Microprocessor Card • Basic Software Package • Control Panel and Chassis • Power Supply with power for up to 8k of memory • 4k Read/Write Memory • TTY Controller • 8 Slots additional card mounting capacity
IMP-16L/308	Same as IMP-16L/304 but includes 8k words of Read/Write memory
IMP-16L/004	4096 word, 16-bit Read/Write memory card for IMP-16L. Size is 8-1/2 x 11".
IMP-16L/825W	IMP-16L Card Reader Controller for DOCUMATION Card Reader (2 pc cards plus software)
	IMP-16P AND IMP-16C HARDWARE
IMP-16C/200	16-bit parallel microprocessor system packaged on an 8-1/2 x 11 printed circuit card. Includes the following features: • 256 words of 16-bit RAM memory • Sockets for 512 words of ROM memory • Interrupt logic • Address capability for 65k of memory (off card) • Socket for Extended Instruction Set CROM
IMP-16C/300	Same as IMP-16C/200 above, but includes Extended Instruction Set CROM (IMP-16A/522N).
IMP-16P/204	16-bit microcomputer prototyping system, to aid the system designer in working with the IMP-16C microprocessor card. Includes: • IMP-16C/200 Microprocessor Card • Chassis, Front Panel, and Power Supply • 4k Read/Write Memory • TTY/Card Reader Interface • Basic Software Package • 7 slots additional card capacity
IMP-16P/208	Same as IMP-16P/204 but includes 8k words of Read/Write Memory
IMP-16P/304	Same as IMP-16P/204, but includes Extended Instruction Set CROM.
IMP-16P/308	Same as IMP-16P/208 but includes Extended Instruction Set CROM.
IMP-16P/004	4096 word, 16-bit Read/Write memory card (8-1/2" x 11") for use with IMP-16C/200 and IMP-16P/20x. Requires one IMP-16P/0042 Timing and Control Card for 1-8 memory cards.
IMP-16P/004T	Timing and Control Card to support IMP-16P/004 RAM memory cards used with IMP-16C/200 and IMP-16P/10x. One card supports up to 8 RAM memory cards. Size is 8-1/2" x 11".
IMP-16C/882	Control panel board for use with IMP-16C, provides programmer easy access to functional areas of the card. Includes PC board, data switches, display lights, and controls.
	16-BIT FIRMWARE AND SOFTWARE
IMP-16F/500	2-PROM set, including Memory Diagnostics, control panel service routine, and sample programs for IMP-16C cards. (CMEMDI)
IMP-16F/501	4-ROM set including complete IMP-16 CPU Diagnostics, for IMP-16C card. (ROMDI)
IMP-16F/000	2-PROM set including service routines for TTY and Control Panel, for IMP-16C card. (CUTIL)

IMP-SERIES MICROPROCESSORS LIST (Con't.)

MODEL	PRODUCT DESCRIPTION
IMP-16F/002	2-PROM set including software debug routines to be used with IMP-16F/000 above, an IMP-16C card and a TTY. (DEBUGC)
IMP-16S/900A	IMP-16 Cross Assembler, for use on IBM System 360/370 or other large-scale computers with at least 100k bytes of available memory. Written in ANSI FORTRAN 4, accepts IMP-16 machine language. Package includes: • FORTRAN Source Card Deck (IMP-16S/100P) • Assembler Manual (IMP-16S/102Y) • Assembler Source Listing (IMP-16S/100A) • 360/370 Assembler Installation Manual (IMP-16S/114Y) • Assembler Internal Description Manual (IMP-16S/103Y) Package includes all items, but each item is also available individually, at price shown in parenthesis. Note that a version of this Cross-Assembler is also available through the terminal network of Tymshare Corp. Contact local Tymshare office.
	MANUALS – 16-BIT EQUIPMENT
IMP-16C/921	IMP-16C Application Manual
IMP-16C/935	IMP-16C Interface Guide
IMP-16C/936	IMP-16C/P Product Description
IMP-16L/924	IMP-16L Product Description
IMP-16L/925	IMP-16 Utility Reference Manual
IMP-16L/928	IMP-16L User's Manual
IMP-16S/102Y	IMP-16 Programming and Assembler Manual
IMP-16S/103Y	IMP-16 Assembler Internal Description Manual
IMP-16S/118Y	IMP-16 Tymshare User's Manual
	IMP-8C AND IMP-8P HARDWARE
	IMP-8C PROCESSOR CARD
IMP-8C/200	8-bit parallel microprocessor system packaged on an 8-1/2" x 11" printed circuit card. Includes: • 256 words of 8-bit Read/Write Memory • Sockets for 2048 words of PROM Memory • Interrupt logic • Address Capability for 65k of Memory (off card)
IMP-8P/208	8-bit microcomputer prototyping system to aid the system designer in working with the IMP-8C microprocessor card. Includes: • 8k Bytes of Read/Write Memory • IMP-8C/200 Microprocessor Card • Chassis, Front Panel, and Power Supply • TTY/Card Reader Controller • 6 Slots of Additional card mounting capacity • Basic Software Package
IMP-8P/216	Same as IMP-8P/208, but includes 16k bytes of Read/Write Memory.
	8-BIT FIRMWARE AND SOFTWARE
IMP-8F/501	8-PROM package including CPU diagnostic routines
IMP-8S/900	IMP-8 Cross-Assembler for use on IBM System 360/370 or other large-scale computers with at least 100k bytes of available memory. Written in ANSI, FORTRAN 4, accepts IMP-8 assembly language mnemonics and outputs IMP-8 machine language. Package includes: • FORTRAN Source Card Deck • Assembler Manual • Assembler Source Listing • 360/370 Assembler Installation Manual Note that a version of this Cross Assembler is also available through the terminal networks of the Tymshare Corp. (Contact local Tymshare office), and General Electric Information Services.

IMP-SERIES MICROPROCESSORS LIST (Con't.)

MODEL	PRODUCT DESCRIPTION
	8-BIT EQUIPMENT MANUALS
IMP-8C/932	IMP-8C Application Manual
IMP-8P/930	IMP-8C/P Product Description
IMP-8P/933	IMP-8P User's Manual
IMP-8S/040Y	IMP-8P Utility Reference Manual
IMP-8S/134Y	IMP-8 Programming and Assembler Manual
	MECHANICAL ASSEMBLIES
IMP-00H/880	6 Slot Card Cage with six 144-pin wire-wrap connectors for mounting IMP series microcomputers, memories, and I/O controllers. Mounts in IMP-16L, -16P, or -8P chassis.
IMP-00H/881	6 Slot Card Cage as above, but with three 144-in wire-wrap connectors, spaced for use with IMP-00H/89x wire-wrap Prototyping Cards.
IMP-00H/891	Prototyping Card, 8-1/2 x 11" with 144-pin connection on one edge, and pre-drilled to hold 64 16-pin wire-wrap sockets or 58 16-pin and 4 24-pin wire-wrap sockets (not included). Mounts in 6-slot Card Cage.
IMP-00H/882	144-Pin Single Card Connector for IMP-series cards.
IMP-00H/892	Prototyping Card, 8-1/2 x 11", with 144-pin connection on one edge, and pre-drilled to hold up to 90 wire-wrap sockets (not included) in any combination of 16-pin and 24-pin configurations. (24-pin uses two socket positions.)
IMP-00H/890	Extender Card for use with IMP Series cards and card cages. Includes 144-pin male and female connectors, and will raise a logic card clear of the card cage for easy access to components.
	PERIPHERALS FOR USE WITH IMP-16L, -16P, -8P
IMP-00/825	Documation 300 CPM Card Reader and Cable
IMP-00/810	ASR-33 Teletype and Cable
	MICROPROCESSOR CHIP SETS
IMP-16A/500D	16-bit Microprocessor Chip Set including four Register Arithmetic Logic Units (RALUs) and one Control Read Only Memory (CROM) with standard 43-instruction set.
IMP-16A/502D	16-bit Microprocessor Chip Set as above, but including a second CROM with the extended 60-instruction set.
IMP-8A/500D	8-bit Microprocessor Chip Set including 2 RALUs and one CROM with the standard 38-instruction set.
IMP-00A/520D	Register, Arithmetic and Logic Unit (RALU) used in the above mentioned Chip Sets. This device is a 4-bit processor slice for use in 4 to 32-bit computers.
IMP-16A/521D	Control Read-Only Memory (CROM) used to microprogram four RALUs for the standard 16-bit, 43-instruction set.
IMP-16A/522D	CROM used to microprogram four RALUs for the extended 16-bit, 17-instruction set. Intended for use with the IMP-16A/521D, above.
IMP-8A/520D	CROM used to microprogram 2 RALUs for the standard 8-bit, 38-instruction set.
MM5203Q	Unprogrammed PROMs, 256 x 8 bit, for use with all IMP series microprocessors.
MM5203D	MM5203D may be electrically programmed once, while MM5203Q may be erased with UV light and re-programmed.
	CHIP SET MANUALS
IMP-00A/905	Microprocessor Chip Set Product Description.

Microprocessors

IMP MM5750 MOS/LSI register and arithmetic logic unit (RALU)

general description

The MM5750 is a member of a new family of microprocessor elements, and is a monolithic MOS/LSI circuit utilizing standard P-channel, enhancement mode, silicon gate technology. It provides a 4-bit slice of the register and arithmetic portion of a general purpose controller/processor. RALU's may be stacked in parallel for longer word lengths. The RALU is designed to be used with other members of National's IMP family (in particular the MM5751 CROM) to form a complete processor. Each RALU provides 96 bits of storage in the form of 4 bits in each of 7 general registers, a status register and a 16-word last in, first out (LIFO) stack. The arithmetic and logic unit performs ADD, AND, OR and exclusive OR operations on true and complemented data from the registers at nearly 10^6 operations per second. A shifter is provided for single bit left or right shifts and an I/O data multiplexer for communication with an external data bus. Control is provided over a 4-bit, time multiplexed command bus.

The RALU operates on +5V and −12V supplies with 4-phase, non-overlapping clocks. Signals which are intended for interface with the MM5751 CROM are MOS level, while those which are intended for interface with the rest of the processor system are TTL levels.

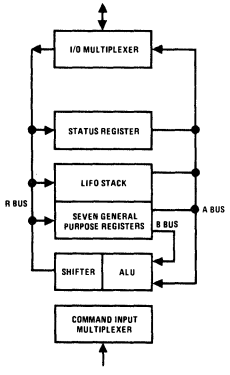
features

■ 4-bit slice of register and arithmetic logic block	Expandable to 32-bit word
■ Arithmetic and logic operations	ADD, AND, OR, Exclusive OR
■ 7 general purpose registers	Functions not pre-assigned
■ 4-bit status register	Overflow, Link, Carry, general flag
■ 16 word stack	Last in, first out
■ Multiplexed I/O data bus	4-bit, bipolar compatible
■ Multiplexed command bus	4-bit MOS levels
■ High speed operation	~ 700 kHz
■ Standard supplies	+5V, −12V
■ Bipolar compatibility	Drives TTL
■ 4-phase clock	Non-overlapping
■ Standard package	24-pin DIP

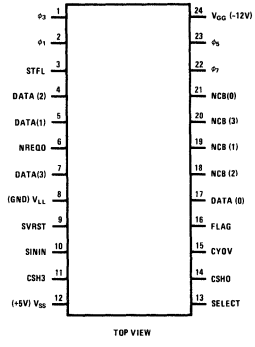
applications

- General purpose processor
- Distributed and multiprocessors
- Process controllers
- Machine tool controllers
- Small business machines
- Terminal controllers
- Test system and instrument control
- Traffic controller

block and connection diagrams



Dual-In-Line Package



Order Number IMP-00A/520D
See Package 6

Order Number IMP-00A/520N
See Package 18

absolute maximum ratings

All Input or Output Voltages With Respect to Most Positive Supply Voltage V_{SS}	+0.3V to −20V
Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W Maximum at +25°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

dc electrical characteristics

(T_A = 0°C to +70°C, V_{SS} = +5V ±5%, V_{GG} = −12V ±5%, V_{LL} = GND)

PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNITS
Logic "1" Input (MOS and TTL) ($V_{IN(1)}$) (Note 1)		V_{SS} − 0.8			V
Logic "0" Input (MOS) ($V_{IN(0)}$)				V_{SS} − 7.0	V
Logic "0" Input (TTL) ($V_{IN(0)}$)				V_{SS} − 4.0	V
Logic "0" Input Current (TTL) ($I_{IN(0)}$)	V_{IN} = 0V			−1.75	mA
Input Leakage Current (MOS) (I_L)	V_{IN} = +5.0V to −12V			±1.0	μA
Logic "1" Output (MOS) ($V_{OUT(1)}$)		V_{SS} − 0.4			V
Logic "0" Output (MOS) ($V_{OUT(0)}$)		V_{SS} − 8.0			V
Logic "1" Output (TTL) ($V_{OUT(1)}$)	I_{OUT} = 0.2 mA	2.4			V
Logic "0" Output (TTL) ($V_{OUT(0)}$)	I_{OUT} = −1.6 mA			0.4	V
Pull-up Transistor "on" Resistance ($P_{PULL-UP}$)(Note 1)	V_{IN} = V_{SS} − 1.0V	3.0		5.0	kΩ
Signal Line Input Capacitance (C_S) for SELECT, SVRST, SININ, DATA (0), (1), (2), (3)	V_{IN} = V_{SS}, f_T = 700 kHz		7.0	10	pF
CSH0, CSH3 Input Capacitance (C_S)	V_{IN} = V_{SS}, f_T = 700 kHz		11	14	pF
Clock Input Capacitance (C_C)	V_{IN} = V_{SS}, f_T = 700 kHz	30	40	55	pF
Clock "1" Level ($V_{\phi(1)}$) (Note 4)		V_{SS} − 1.0		V_{SS}	V
Clock "0" Level ($V_{\phi(0)}$)		V_{GG} − 1.0		V_{GG} + 1.0	V
Load Capacitance for DATA(0), (1), (2), (3), CSH0, CSH3 (C_L)	V_{IN} = 0V, f_T = 700 kHz			25	pF
CYOV, FLAG				20	pF
STFL, NREQ0				30	pF
Current Sinking Resistors Required on CYOV, STFL, NREQ0 (R_{SINK}) (Note 3)	From Pin to V_{GG}	4.6		5.8	kΩ
Power Dissipation (P_D) (T_1 − T_8 Equal Width)	f = 700 kHz		550	750	mW

Note 1: Internal pull-up provided for TTL inputs. Refer to Figure 3 and text.

Note 2: Max = most positive; Min = most negative.

Note 3: Required to drive 74H loads. Larger resistance values may be used to drive standard or low power TTL.

Note 4: Clamp diodes and series damping resistors may be required to prevent clock overshoot.

FUNCTIONAL DESCRIPTION OF RALU

A diagram of the RALU is shown in Figure 1. Seven general registers (labelled R_1–R_7) are provided. Any of the seven registers may be loaded onto the A- or B-bus for processing by the arithmetic and logic unit (ALU). The data on the A-bus may be complemented before being loaded on the IA-bus, which serves as the input to the ALU. The operations which may be performed by the ALU are ADD, AND, OR and exclusive OR. The ADD operation adds IA and B and the carry (CSH0) from pin 14. A carry output (CSH3) is provided by pin 11. The result of the ALU operation is available to the shifter via the S-bus. The shifter provides a one bit left or right shift (or no shift) and transfers the shift information in and out of pins 11 and 14. Output data from the shifter may be returned to any of the registers over the R-bus.

A 16 word last in, first out stack (LIFO) is provided and may be accessed over the A- and R-buses. When the bottom word of the stack becomes non-zero a stack full signal (STFL) is provided at pin 3. Status information is provided by a 4-bit status register. Link, Overflow, Carry and Flag indicators are provided in bit positions 3, 2, 1 and 0 respectively (where bit 3 is the most significant bit). The Link flag may be included in shift operations (under control of the Select input) and the Overflow and Carry flags provide information on the result of ADD operations. A general purpose status flag (Flag) is also provided which may be used for interrupt enable or other functions where it is desirable to save status bits on the stack. Also, the Link, Overflow and Carry functions may be disabled, allowing these flags to be used for general purpose application. This is

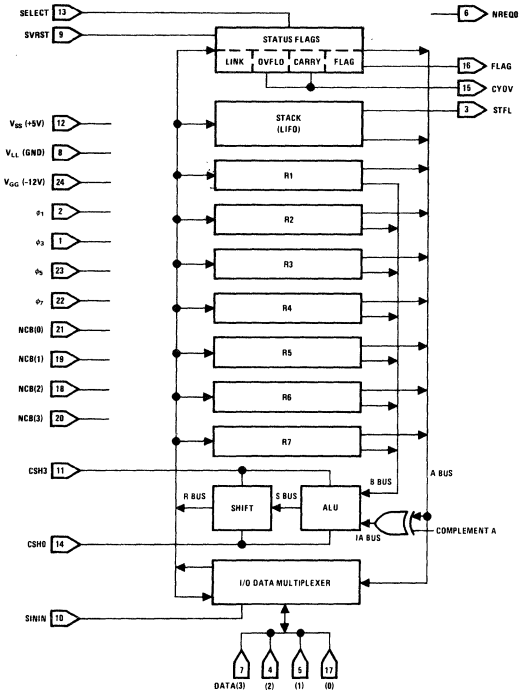


FIGURE 1. RALU Block Diagram

described in the section detailing control signals for the RALU.

Communication between the RALU and the rest of the system is provided by the I/O data multiplexer. This logic provides for loading the R-bus from the external data bus, as well as sending data from the A- and R-buses. Details of signal functions and timing are presented in the following sections. Positive true logic signals are used ("1" = most positive voltage, "0" = most negative voltage). Signal names beginning with N are complemented signals.

FUNCTIONAL DESCRIPTION OF SIGNALS

Signal timing for the RALU is shown in Figure 2. The timing diagram is divided into 8 time intervals (T_1-T_8) based on the 4-phase non-overlapping clocks. The clock inputs have MOS levels of +5V and −12V and occur during the odd time intervals. Thus phase 1 clock is a logic "0" (−12V) during T_1 and a logic "1" (+5V) during T_2-T_8.

Commands

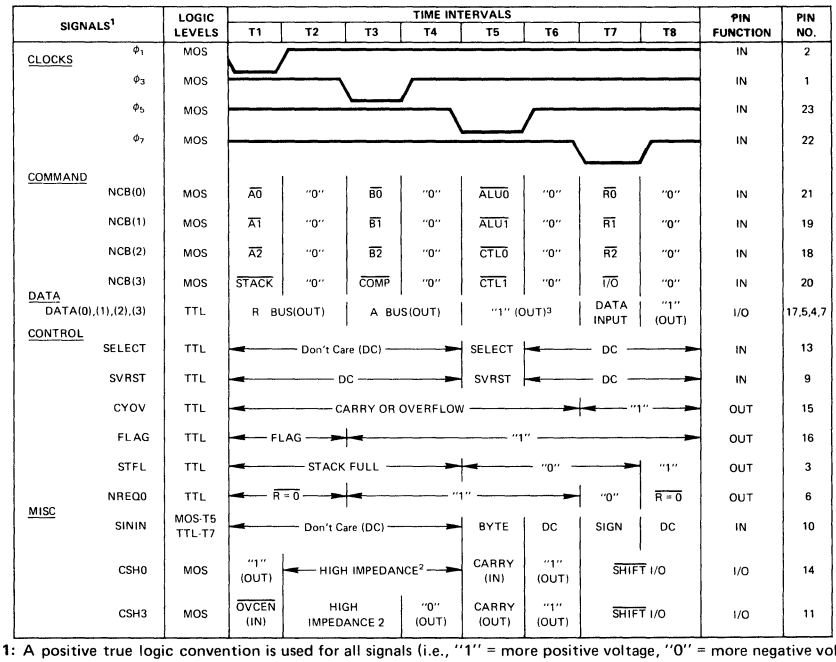
The command inputs to the RALU occur on pins 21, 19, 18, and 20 which correspond to command bits NCB(0), (1), (2), and (3) respectively. The command inputs are complemented MOS signals and are multiplexed over the 4 odd time intervals in each RALU cycle (T_1, T_3, T_5, T_7). The inputs must be driven negative to logic "0" during the even time intervals. The command functions for each bit are indicated in the diagram. During T_1, the three least-significant command bits specify the address of the register (R_1-R_7) to be loaded on the A-bus. If NCB(0), (1), and (2) are all logic "1" the A-bus is set equal to zero. The fourth command bit NCB(3) is used to enable stack operations. If NCB(3) is at a logic "1" (most positive level) no stack operations occur. If it is a logic "0" stack operations are enabled, but will only occur if the A or R-bus address is zero. If the A-bus address is zero the stack will be pulled onto the A-bus. If the R-bus address is zero, the R-bus will be pushed onto the stack.

During T_3 the three least-significant bits specify the address of the register (R_1-R_7) to be loaded on the B-bus. (Note that stack and flags cannot be accessed over the B-bus. An address of zero always gives zero data, however, NCBX's = all 1's.) The most-significant bit specifies that the A-bus is to be complemented when it is transferred to the IA-bus.

During T_5, NCB(1) and NCB(0) specify the ALU operation to be performed as follows: 00-AND, 01-XOR, 10-OR, 11-ADD. NCB(3) and NCB(2) are used to specify control functions as follows: 00-No-OP, 01-R-bus control, 10-shift S-bus left 1-bit position during transfer to R-bus, 11-shift S-bus right 1-bit position during transfer to R-bus.

The R-bus control code is used in conjunction with the I/O control bit (NCB(3) at T_7) and the Byte input (SININ at T_5) to set the value of the R-bus as shown below and in Table I (RALU command code summary).

During T_7 the three least significant bits specify the address of the register (R_1-R_7) to be loaded



Note 1: A positive true logic convention is used for all signals (i.e., "1" = more positive voltage, "0" = more negative voltage). Signal names beginning with N are complemented signals.

Note 2: CSH0 and CSH3 high impedance state for intervals T_2 through T_4 is the TRI-STATE mode for output drivers.

Note 3: "1" (OUT) means RALU is driving this node to the "1" logic level during the defined interval. For bidirectional I/O lines the logic state is defined as "in" or "out."

FIGURE 2. RALU Timing Diagram

from the R-bus. The most-significant bit specifies that the R-bus is to be set equal to the output of the I/O multiplexer rather than the shifter (unless R-bus control was specified at T_5). Reference R-bus control states Table I.

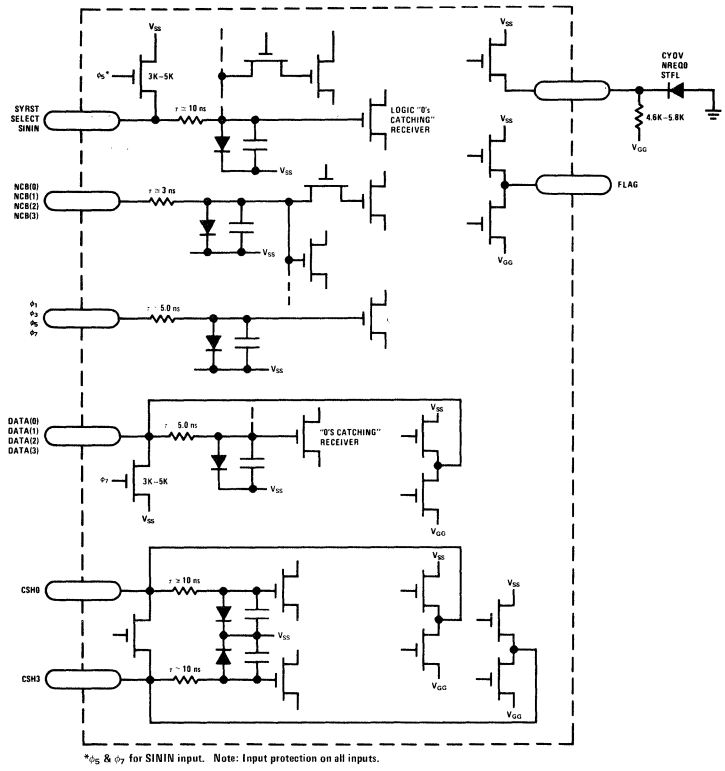
Data

The data transfers between the RALU and memory or peripheral devices occur on pins 17, 5, 4, and 7 which correspond to data bits DATA(0), (1), (2) and (3) respectively. During T_1 and T_2 the data lines are driven with the value of the R-bus which occurred at the end of the *previous timing cycle.* This output may be used by the CROM chip for conditional branch inputs. During T_3 and T_4 the data lines are driven with the value that was loaded onto the A-bus during the current timing cycle. This output is typically used for address and data output to system memory or peripheral devices. During T_5 and T_6 the data lines are driven to a logic "1." During T_7 the data lines are used for input to the RALU from system memory or peripheral devices. *The data receivers are "zeroes catching" so the data lines must not be allowed to go negative during T_7 unless the data input is to be a logic zero.* During T_8 the data lines are again driven to a logic "1" by the RALU. As with all TTL inputs on the RALU a 3K–5K pull-up is provided on the chip to insure an adequate logic "1" level (see Figure 3). The pull-up is provided by an MOS transistor which is turned on only during the data input interval. At other times it is in the "off" or high impedance state.

Control Signals

The RALU control lines provide a means of using the RALU status flags. The SELECT line is used as an input at T_5 ("zeroes catching") and is unused at other times. If the SELECT line is a logic "1" at T_5 the Overflow status flag will be selected as the output on the Carry or Overflow (CYOV) line (pin 15) during the *following* cycle. If the RALU is in the most significant byte of a processor (as specified by the Byte input on the SININ line) the Link status flag will be included in any shift that occurs in the current cycle. The shift will be a five (5) bit shift with the Link in the most significant bit position. If the Select input is a logic "0" at T_5 the Carry status flag will be selected at the CYOV output and shift operations will not affect the Link.

The Save/Restore (SVRST) line is used as an input during T_5 ("zeroes catching") and provides a means of modifying the status flags over the data bus. If SVRST is a logic "1" during T_5 the status flags will be loaded onto the A-bus during the *following cycle (at T_1),* provided the A-bus address bits NCB(2), (1), and (0), at T_1 during that cycle are a logic "1." If a pull stack operation has been specified by NCB(3), (2), (1), and (0) at T_1, the SVRST input at T_7 will inhibit it and instead the status flags will be loaded on the A-bus. Table II specifies the control bits and the data that occurs on the A-bus at T_1. The SVRST line also causes the status flags to be loaded from the R-bus at the end of the following cycle. (The status of



*ϕ_6 & ϕ_7 for SININ input. Note: Input protection on all inputs.

FIGURE 3. RALU Driver and Receiver Buffers

SVRST during *one cycle* only affects conditions in the *following cycle.*) This will occur in parallel with the loading of any other register specified by the R-bus address. Table III specifies the control bits and the results that occur on the R-bus.

The CYOV line provides an output signal indicating the state of the Carry or Overflow status flag as determined by the Select input. The Flag output indicates the state of the general purpose status flag. The stack full (STFL) output goes true when the bottom word of the stack is non-zero *at the start of the preceding cycle.* The result bus equals zero (NREQ0) output goes to logic "0" level when the R-bus contains all zeroes. The CYOV, STFL and NREQ0 outputs require an external resistor connected to V_{GG}.

Miscellaneous Signals

The SININ line is used to input information as to whether the RALU is in the most or least significant byte of a processor word (at T_5) and also the sign value which is propagated to the most significant byte (at T_7) when the R-bus control function is specified. If SININ is a logic "1" at T_5 the RALU will enable the functions of the most significant byte. The functions enabled are inclusion of the Link in shift operations and setting the R-bus to zero or sign as specified by the R-bus control code. If SININ at T_5 is a logic "0" the functions are not enabled.

The carry input (CSH0) and carry output (CSH3) lines are used primarily for transfer of carry and shift information between RALU's or between RALU and CROM. If an ADD operation is specified, the value of carry input (CSH0) at T_5 will be added to the IA and B-bus inputs to the ALU. The resulting carry output from the most significant bit will occur on CSH3 at T_5. When a left shift is specified, the shift output from the most significant bit occurs on CSH3 at T_7 and T_8 while the shift input ("zeroes catching") to the least significant bit must be provided on CSH0 during T_7 and T_8. The pins exchange roles for a right shift. During T_1 the CSH3 input (if a logic "0" at T_1) is used to enable the Overflow and Carry flags to be set to the result of an ADD operation, *if an ADD is specified for the current cycle.* The Carry flag is set equal to the value of the ripple carry out of the most significant bit of the ALU. The Overflow flag is set if there is a two's complement arithmetic overflow (i.e. sign of both operands was the same and the sign of the result is different). For systems using multiple RALU's the Overflow and Carry flags of all but the most significant RALU will be disabled by the logic "1" output of CSH0 generated by the adjacent RALU at T_1. These flags may therefore be used for general purpose functions.

TABLE I. RALU Commands

1.A Command Inputs

COMMAND BITS[1]

TIME INTERVAL	NCB(3)	NCB(2)	NCB(1)	NCB(0)
T1	STACK	← A BUS →		
T3	COMP	← B BUS →		
T5	← CTL →		← ALU →	
T7	I/O	← R BUS →		

1.B Command Codes[3]

ALU FUNCTIONS

NCB(1), (0) @ T5	FUNCTION
11	AND
10	XOR
01	OR
00	ADD

CTL FUNCTIONS

NCB(3), (2) @ T5	FUNCTION
11	NONE
10	R BUS CONTROL
01	SHIFT LEFT
00	SHIFT RIGHT

A, B & R BUS ADDRESSES

NCB(2), (1), (0)	ADDRESS
111	ZEROES, FLAGS, STACK[2]
110	R1
101	R2
100	R3
011	R4
010	R5
001	R6
000	R7

R BUS CONTROL

I/O (NCB(3) @ T7)	BYTE (SININ @ T5)	R BUS VALUE
1	0	OUTPUT OF SHIFTER
1	1	OUTPUT OF SHIFTER
0	0	OUTPUT OF I/O MUX
0	1	VALUE OF SIGN INPUT ON SININ @ T7

Note 1: Commands are complemented signals.

Note 2: See text and Tables II and III for addressing flags and stack.

Note 3: Logic values shown are values which must be applied to NCB inputs to get indicated results.

TABLE II. Binary Table for A Bus Addressing (Time Interval T_1)

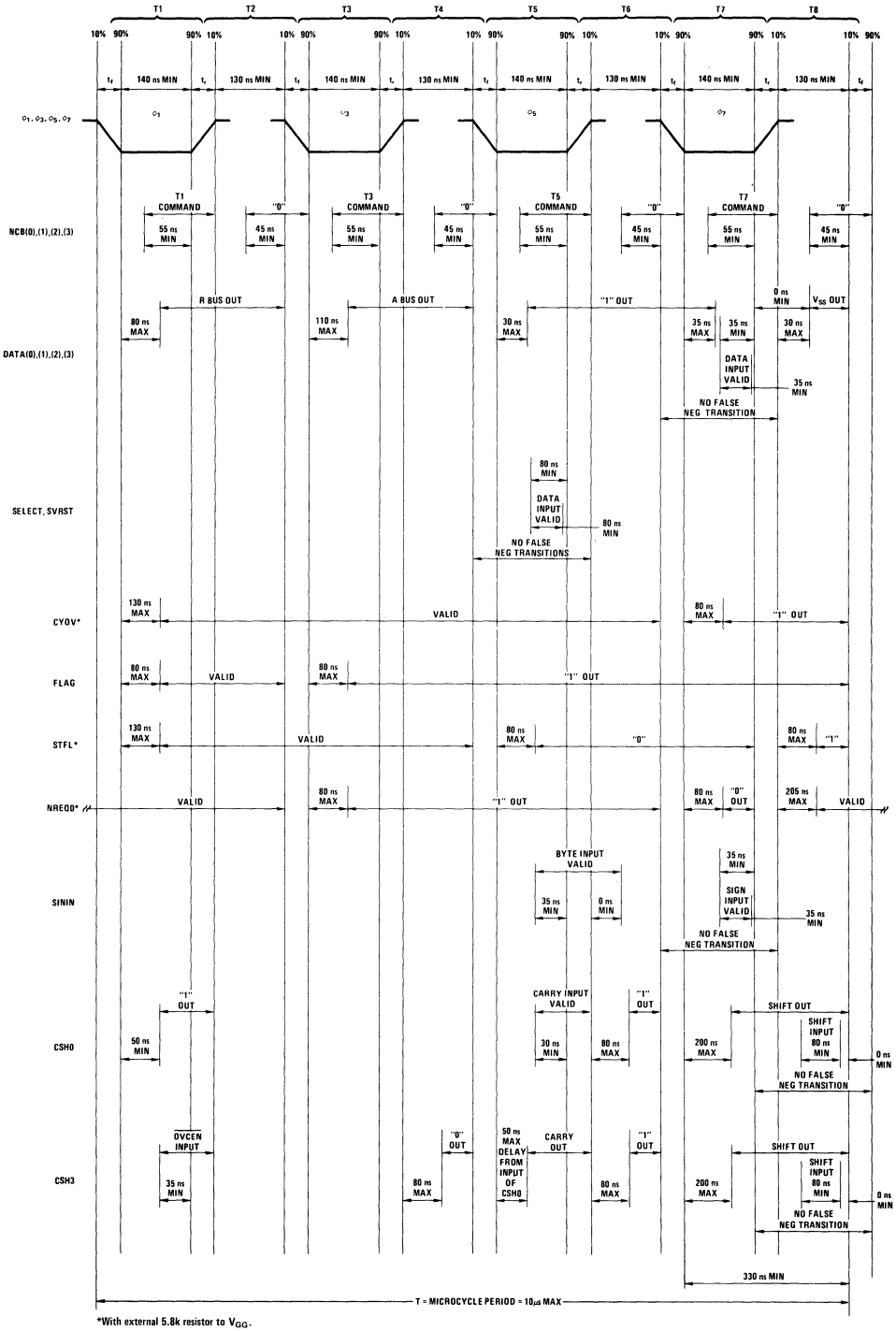
INPUTS		RESULTING DATA ON A BUS
SVRST @ Previous Cycle T_5	NCB (3), (2), (1), (0) @ Current Cycle T_1	
0	1 1 1 1	All Zero's
0	1 1 1 0	Contents of R_1
0	1 1 0 1	Contents of R_2
0	1 1 0 0	Contents of R_3
0	1 0 1 1	Contents of R_4
0	1 0 1 0	Contents of R_5
0	1 0 0 1	Contents of R_6
0	1 0 0 0	Contents of R_7
0	0 1 1 1	Pull Stack
0	0 1 1 0	Contents of R_1
0	0 1 0 1	Contents of R_2
0	0 1 0 0	Contents of R_3
0	0 0 1 1	Contents of R_4
0	0 0 1 0	Contents of R_5
0	0 0 0 1	Contents of R_6
0	0 0 0 0	Contents of R_7
1	1 1 1 1	Status Flags
1	1 1 1 0	Contents of R_1
1	1 1 0 1	Contents of R_2
1	1 1 0 0	Contents of R_3
1	1 0 1 1	Contents of R_4
1	1 0 1 0	Contents of R_5
1	1 0 0 1	Contents of R_6
1	1 0 0 0	Contents of R_7
1	0 1 1 1	Status Flags
1	0 1 1 0	Contents of R_1
1	0 1 0 1	Contents of R_2
1	0 1 0 0	Contents of R_3
1	0 0 1 1	Contents of R_4
1	0 0 1 0	Contents of R_5
1	0 0 0 1	Contents of R_6
1	0 0 0 0	Contents of R_7

Note: Logic values shown are what must be applied to NCB (which is a complemented signal) to get desired results.

TABLE III. Binary Table for R Bus Addressing (Time Interval T_7)

INPUTS		REGISTER LOADED FROM R BUS
SVRST @ Previous Cycle T_5	NCB (3) @ Current Cycle T_1 and NCB (2), (1), (0) @ Current Cycle T_7	
0	1 1 1 1	Not Stored
0	1 1 1 0	R_1
0	1 1 0 1	R_2
0	1 1 0 0	R_3
0	1 0 1 1	R_4
0	1 0 1 0	R_5
0	1 0 0 1	R_6
0	1 0 0 0	R_7
0	0 1 1 1	Push Stack
0	0 1 1 0	R_1
0	0 1 0 1	R_2
0	0 1 0 0	R_3
0	0 0 1 1	R_4
0	0 0 1 0	R_5
0	0 0 0 1	R_6
0	0 0 0 0	R_7
1	1 1 1 1	Status Flags
1	1 1 1 0	Status Flags and R_1
1	1 1 0 1	Status Flags and R_2
1	1 1 0 0	Status Flags and R_3
1	1 0 1 1	Status Flags and R_4
1	1 0 1 0	Status Flags and R_5
1	1 0 0 1	Status Flags and R_6
1	1 0 0 0	Status Flags and R_7
1	0 1 1 1	Status Flags and Push Stack
1	0 1 1 0	Status Flags and R_1
1	0 1 0 1	Status Flags and R_2
1	0 1 0 0	Status Flags and R_3
1	0 0 1 1	Status Flags and R_4
1	0 0 1 0	Status Flags and R_5
1	0 0 0 1	Status Flags and R_6
1	0 0 0 0	Status Flags and R_7

Note: Logic values shown are what must be applied to NCB inputs to get results shown.



*With external 5.8k resistor to V_{GG}.
Note: t_r and t_f = 250 ns max.

FIGURE 4. RALU Signal Timing Specifications
(T_A = 0°C to +70°C, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, V_{LL} = GND)

Recommended Start-up Conditions

Power supplies must be within specification for ten microseconds (10μs) before clocks are started. (Note: All internal nodes must be in a discharged state before start-up.) When power supplies are cycled on and off rapidly the nodes must be discharged by running the clocks for one (1) microcycle (T_1-T_8) after power is removed from the RALU.

It is recommended that STFL and CYOV be tied to V_{SS} if not used.

SIGNAL TIMING SPECIFICATIONS

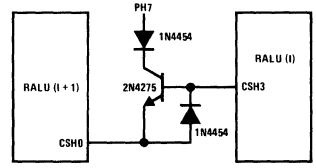
The timing specifications for all RALU signals are shown in Figure 4. These specifications apply over the complete range of recommended operating conditions (T_A = 0°C to +70°C, V_{SS} = +5V ±5%, V_{GG} = −12V ±5%). Time intervals are defined with respect to the 10% and 90% points of the four MOS clock inputs. The clocks have a maximum rise and fall time of 250 ns. The command inputs on the NCB lines must be valid a minimum of 55 ns prior to the end of the odd time intervals (see Figure 3). Data inputs to the RALU over the data lines must be valid for at least 35 ns during T_7 and *must never go falsely negative to a logic zero, during T_7, due to the "zeroes catching" nature of the receiver.* It will often simplify interface design if input data to the RALU is gated onto the data bus during parts of T_6 and T_8 as well as during the required interval T_7. The logic "1" outputs of the RALU data lines at T_6 and T_8 may be overridden by the data input drive; however, the increased power dissipation will lower the maximum allowable ambient temperature for the chip. (Note: The logic "1" output drive has a minimum impedance of 300Ω to V_{SS}.)

The specification of the carry output (CSH3) applies only when the carry input to CSH0 is valid prior to the start of T_5. If the CSH0 input is not valid at the start of T_5 then the CSH3 output will become valid a maximum of 50 ns after the input becomes valid. In a typical 16-bit application the carry input (CSH0) to the least significant RALU will be valid at the start of T_5, however, the carry input to the more significant RALU's will be delayed, since it must first be generated at the CSH3 output of the preceeding less significant RALU.

As indicated on the CSH0 timing specification, the latest the CSH0 input can become valid for a proper RALU ADD operation to occur is 30 ns before the end of T_5.

The output from CSH3 is valid within 50 ns of a valid input at CSH0. In a system with multiple RALU's the carry must propagate through each RALU and provide a valid input to the most significant RALU at least 30 ns before the end of T_5. For a system with N RALU's, the minimum width of T_5 to allow for carry propagation is approximately $40N + 1.5N^2$ ns ($N \leq 8$). However, this is strongly affected by the carry line capacitance (this capacitance should be minimized as much as possible, especially for the high order bits).

For systems where N is large, T_5 should be streched to provide the additional time. Alternatively the buffer circuit shown in the figure below may be used between RALU's. A single buffer between the center RALU's will typically reduce the carry propagation time by more than 30%, however the noise margin is reduced somewhat.



Microprocessors

IMP MM5751 MOS/LSI control and read only memory unit (CROM)

general description

The MM5751 Control and Read Only Memory Unit (CROM) is a member of a new family of microprocessor devices, and is a monolithic MOS/LSI circuit utilizing standard P-channel, enhancement mode, silicon gate technology. It provides read only microprogram storage and control logic and is designed for use with the MM5750 Register and Arithmetic Logic Unit (RALU). The CROM provides storage for one-hundred microinstructions of 23 bits each. Circuitry is also provided for program sequencing, subroutine execution, and translation of microinstructions into RALU commands. One CROM may be used with 1 to 8 RALU's to implement systems with 4 to 32-bit word lengths. Multiple CROM's may be used to provide expanded capability. CROM's are available with standard 8- and 16-bit instruction sets. (Other sets may be available in the future.)

The CROM operates on +5V and −12V supplies with 4-phase, non-overlapping clocks. Signals which are intended for interface with the MM5750 RALU are MOS level, while those which are intended for interfacing with the rest of the system are TTL levels.

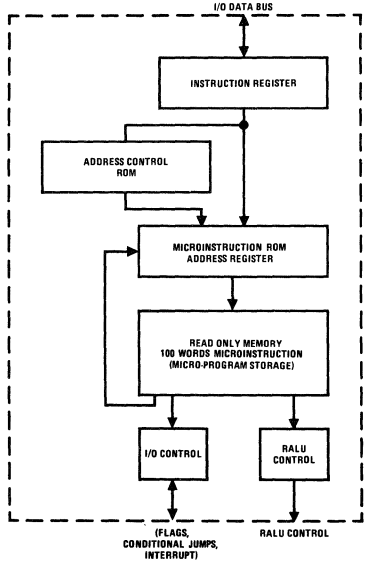
features

- Standard supplies +5V, −12V
- Bipolar compatibility Drives TTL
- Standard package 24 pin DIP
- High speed ~ 700 kHz
- Microprogrammable 100 words
- Subroutine capability Return address register
- Expandable Up to 4 CROM's

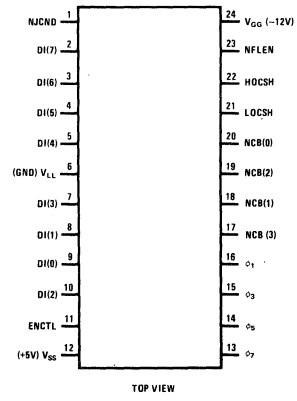
applications

- Standard IMP instruction sets
- Expansion of standard instruction sets
- Custom instruction sets
- Custom application control programs
- Control of 4 to 32-bit microprocessors when used with MM5750—Register and Arithmetic Logic Unit

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number IMP-16A/521D (16-bit std. CROM), IMP-16A/522D (16-bit extended CROM), or IMP-8A/521D (8-bit std. CROM)
See Package 6

Order Number IMP-16A/521N (16-bit std. CROM), IMP-16A/522N (16-bit extended CROM), or IMP-8A/521N (8-bit std. CROM)
See Package 18

absolute maximum ratings

All Input or Output Voltages With Respect to Most Positive Supply Voltage (V_{SS})	+0.3V to −20V
Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W Maximum at +25°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

electrical characteristics

(T_A = 0°C to +70°C; V_{SS} = +5V ±5%; V_{GG} = −12V ±5%, V_{LL} = GND)

PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNITS
Logic "1" Input (MOS and TTL) ($V_{IN(1)}$) (Note 1)		V_{SS} − 0.8			V
Logic "0" Input (MOS) ($V_{IN(0)}$)				V_{SS} − 7.0	V
Logic "0" Input (TTL) ($V_{IN(0)}$)				V_{SS} − 4.0	V
Logic "0" Input Current (TTL) ($I_{IN(0)}$)	V_{IN} = 0V			−1.75	mA
Input Leakage Current (MOS) (I_L)	V_{IN} = +5.0 to −12V			±1.0	μA
Logic "1" Output (MOS) ($V_{OUT(1)}$)		V_{SS} − 0.4			V
Logic "0" Output (MOS) ($V_{OUT(0)}$)				V_{SS} − 8.0	V
Logic "1" Output (TTL) ($V_{OUT(1)}$)	I_{OUT} = 0.2 mA	2.4			V
Logic "0" Output (TTL) ($V_{OUT(0)}$)	I_{OUT} = −2.0 mA (Note 3)			0.4	V
Pull-up Transistor "on" Resistance ($R_{PULL-UP}$) (Note 1)	V_{IN} = V_{SS} − 1.0V	3.0		5.0	kΩ
DI(0) − DI(7) Input Capacitance (C_S)	V_{IN} = V_{SS}, f_T = 700 kHz		5.0	10	pF
NJCND, ENCTL, LOCSH, HOCSH Input Capacitance	V_{IN} = V_{SS}, f_T = 700 kHz		11	14	pF
Clock Input Capacitance (C_C)	V_{IN} = V_{SS}, f_T = 700 kHz	30	40	60	pF
Clock "1" Level ($V_{\phi(1)}$) (Note 4)		V_{SS} − 1.0		V_{SS}	V
Clock "0" Level ($V_{\phi(0)}$)		V_{GG} − 1.0		V_{GG} + 1.0	V
Load Capacitance For D1(0), (1), (2), (3) (C_L)				25	pF
HOCSH, LOCSH				22	pF
ENCTL, NFLEN				20	pF
NCB(0), (1), (2), (3)				50	pF
Power Dissipation (P_D) (T_1 − T_8 Equal Width)	f = 700 kHz		600	850	mW

Note 1: Internal pullup provided for TTL inputs. Refer to Figure 3 and text.
Note 2: Max. = most positive; Min. = most negative.
Note 3: I_{OUT} = −1.6 mA for NFLEN (Pin 23).
Note 4: Clamp diodes and series damping resistors may be required to prevent clock overshoot.

FUNCTIONAL DESCRIPTION

A block diagram of the Control and Read Only Memory (CROM) chip is shown in Figure 1. The ROM provides storage for one-hundred 23-bit microinstructions. This is sufficient to implement a macroinstruction set comparable to many mini-computers, or to provide a control program directly in microcode. In cases where larger programs are desired, up to four CROM chips may be used in a single processor. (CROM's which implement 8- and 16-bit instruction sets are available as standard products.)

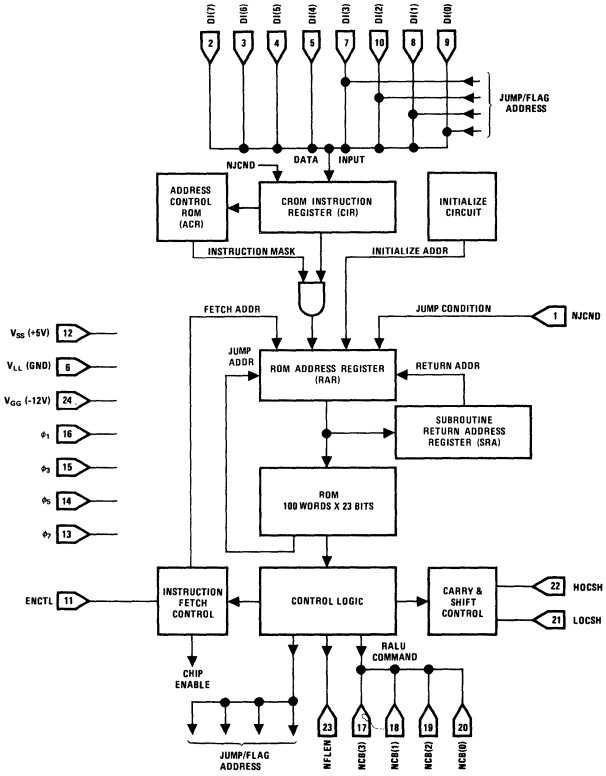
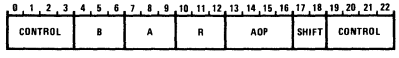


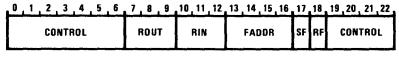
FIGURE 1. CROM Block Diagram

TABLE I. IMP Microinstruction Word Formats

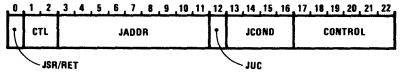
ARITHMETIC INSTRUCTIONS



I/O INSTRUCTIONS



JUMP INSTRUCTIONS



A simplified version of the ROM bit functions is indicated in Table I. For explanation purposes the functions have been divided into three classes. The class is specified by the control fields, which are also used for special functions. The arithmetic class allows specification of the registers to be loaded on the A and B-bus of the RALU, the ALU operation to be performed (AOP), a shift operation and the register to be loaded from the R-bus. The I/O class provides fields for addressing a register for data output and a register for data input as well as setting (SF) and/or resetting (RF) one of 16 external control flags to indicate the type of I/O transfer. The microinstruction jump class provides a 9-bit address field, selection of up to 16 jump conditions (JCOND), an unconditional jump command (JUC) and specification of a subroutine jump or return (JSR/RET). (The jump condition and flag logic is provided off the chip to save pins. Standard product bipolar MSI circuits are available which provide eight control flags in a single addressable latch and 8 or 16 jump conditions with a single multiplexer.)

The ROM has 9 programmable address inputs which come from the ROM address register (RAR). The RAR is a 9-bit synchronous counter with parallel load inputs which normally counts sequentially through ROM addresses. When a program branch is desired the contents of the RAR may be altered by parallel loading from one of several sources. One possibility is to load an address specified by the microcode stored in the ROM. This may be either a conditional or unconditional branch. Conditional branches are controlled by the jump condition input (NJCND). An external jump condition multiplexer drives NJCND and may apply one of up to 16 conditions to the input. The condition applied is selected by the jump/flag address which is sent out over pins DI(0), (1), (2), and (3) at the beginning of each microinstruction cycle. The RAR may also be loaded from the subroutine address register (SRA). This register is loaded from the RAR if a jump to subroutine is specified by the microcode. The SRA is loaded back into the RAR when a return from subroutine is executed. There are two programmable addresses which may be loaded into the RAR. These are the address of the instruction fetch routine, which will be loaded into the RAR when a new macroinstruction is to be "fetched" from the system memory, and the address of the initialize routine, which will be loaded when the power is turned on. The final method of loading the RAR is from the CROM instruction register (CIR). This register is loaded from external memory, or an I/O device, with a macroinstruction to be executed. The CIR is loaded into the RAR as commanded by the microprogrammed "fetch" routine. The CIR bits are masked by the outputs of the Address Control ROM (ACR) before being loaded into the RAR. The masking is used to set bits which are not part of the instruction opcode to zero. There are 12 masks available; the one used is selected by the current contents of the CIR (i.e., each instruction selects its own mask). The selection code and masks are both programmable.

The HOCSH and LOCSH (High and Low Order Carry/Shift) signals are used to implement carry and shift operations. LOCSH is used to provide a low order carry in for the ALU. This is useful for incrementing, two's complementing a number or emitting (serial) bit patterns to the ALU. During circular shift operations HOCSH and LOCSH are tied together by an internal transistor, allowing shifts to propagate between the most and least significant ALU bits. In the case of open shifts the HOCSH and LOCSH pins provide trailing zeroes to be shifted into the ALU.

Control information from the CROM to the RALU is sent over four time-multiplexed lines (NCB(0), (1), (2), and (3)). Four 4-bit commands are sent each microinstruction cycle. These lines go to all RALU chips in parallel. The enable control pin (ENCTL) and the chip enable circuitry are used for systems having more than one CROM (for microprograms with more than 100 words).

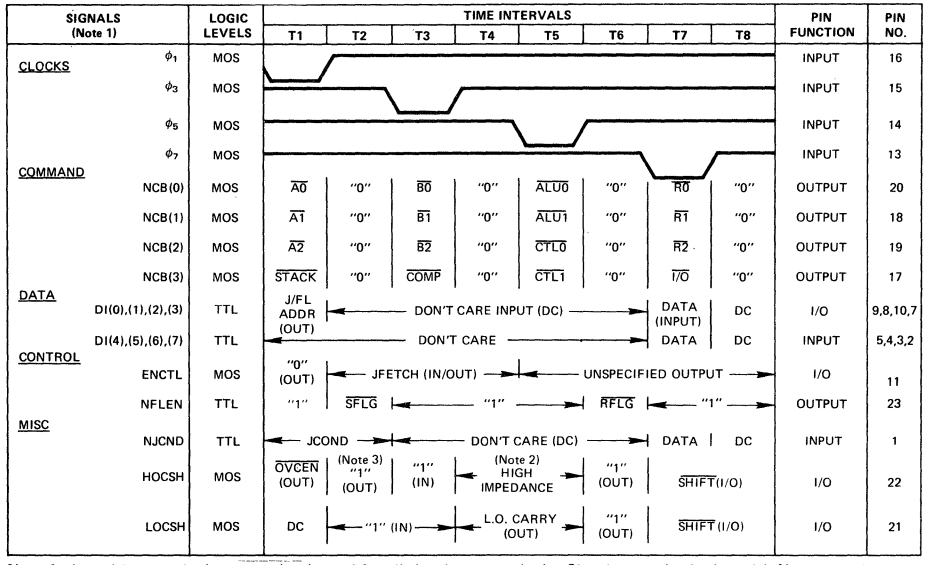
Details of signal functions and timing are presented in the following sections. Positive true logic signals are used ("1" = more positive voltage, "0" = more negative voltage). Signal names beginning with N are complemented signals.

FUNCTIONAL DESCRIPTION OF SIGNALS

The timing diagram (Figure 2) is divided into 8 time intervals (T_1 - T_8) based on the 4-phase non-overlapping clocks. The clock inputs have MOS levels of +5V and -12V and occur during the odd time intervals. Thus phase 1 is a logic "0" (-12V) during T_1 and a logic "1" (+5V) during T_2 - T_8.

Commands

The command outputs to the RALU occur on pins 20, 18, 19, and 17 which correspond to command bits NCB(0), (1), (2), and (3). The command outputs are complemented MOS signals and are multiplexed over the 4 odd time intervals in each cycle (T_1, T_3, T_5, T_7). Outputs are driven negative to logic "0" during the even time intervals. The command functions for each bit are indicated in the diagram. During T_1, the three least significant command bits specify the address of the register to be loaded onto the A-bus. Registers R_1 - R_7 are addressed by binary values of 1 - 7 respectively. A value of zero causes the A-bus to be set equal to zero. The fourth command bit is used to enable stack operations. If NCB(3) is at a logic "1" (most positive level) no stack operation occurs. If it is at a logic "0" stack operations are enabled, but will only occur if the A or R-bus address is zero. If the A-bus address is zero the stack will be pulled onto the A-bus. If the R-bus address is zero, the R-bus will be pushed onto the stack.



Note 1: A positive true logic convention is used for all signals except clocks. Signal names beginning with N are complemented signals.

Note 2: HOCSH at T4 and T5 is in the TRI-STATE high impedance output mode of CROM load drivers.

Note 3: "1" (OUT) means CROM is driving this node to the logic "1" level during the defined interval. For I/O lines the logic state is defined as "in" or "out." Input or output nodes are defined only as "1" or "0."

FIGURE 2. CROM Timing Diagram

During T_3 the three least significant bits specify the address of the register (R_1 - R_7) to be loaded on the B-bus. The most significant bit specifies that the A-bus is to be complemented when it is transferred to the IA-bus. During T_5 NCB(1) and NCB(0) specify the ALU operation to be performed, while NCB(3) and NCB(2) are used to specify control functions.

During T_7 the three least significant bits specify the address of the register (R_1 - R_7) to be loaded from the R-bus. The most significant bit specifies that the R-bus is to be set equal to the output of the I/O multiplexer rather than the shifter.

Data

Instructions to the CROM are transferred over the data input lines (DI(0) - DI(7)) into bits 0 - 7 of the CIR. (Bit 8 of the CIR is loaded from the NJCND input.) Data input occurs at T_7. As with all TTL inputs on the CROM a 3k - 5k pull-up is provided on the chip to insure an adequate logic "1" level (see Figure 3). The pull-up is provided by an MOS transistor which is turned on only during the data input interval (T_7). At other times it is in the "off" or high impedance state. Signal lines DI(0) - DI(3) are also used to output a 4-bit address to the control flags and jump conditions. This address output becomes valid during T_1 and must be stored in an external latch at the end of T_1.

Control Signals

The enable control (ENCTL) is a "wired-or" signal line required for operation of multiple CROM's. It provides a logic "1" output at T_2 - T_4 whenever a branch to the instruction fetch routine occurs, and responds to a logic "1" input at T_2 - T_4 by executing a branch to the instruction fetch routine and disabling if the instruction has not been implemented in that particular CROM. The flag enable (NFLEN) control output is used to set or reset flags addressed by DI(0) - DI(3) at T_1 of the current cycle. A logic "0" output at T_2 specifies setting of the addressed flag while a logic "0" output at T_6 specifies resetting.

Miscellaneous Signals

The jump condition input line (NJCND) is used to input conditional branch information at T_1 and T_2 as specified by the jump condition addressed by DI(0) - DI(3) at T_1. If the input is a logic "0" and a conditional branch has been specified for the current cycle, a branch will occur. The NJCND input is also used to load data into CIR(8) at T_7.

The high and low order carry/shift lines (HOCSH and LOCSH) are used to provide shift and carry information to the RALU chips. If a circular shift has been specified, HOCSH and LOCSH are connected together on the CROM during T_7 and T_8 by a low on-resistance MOS transistor switch. For

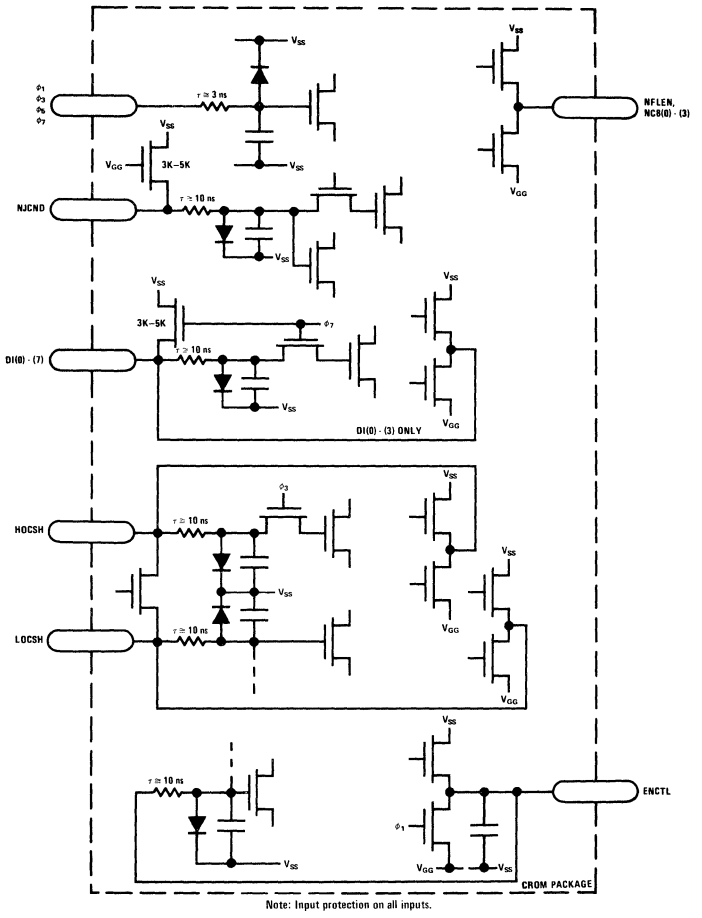
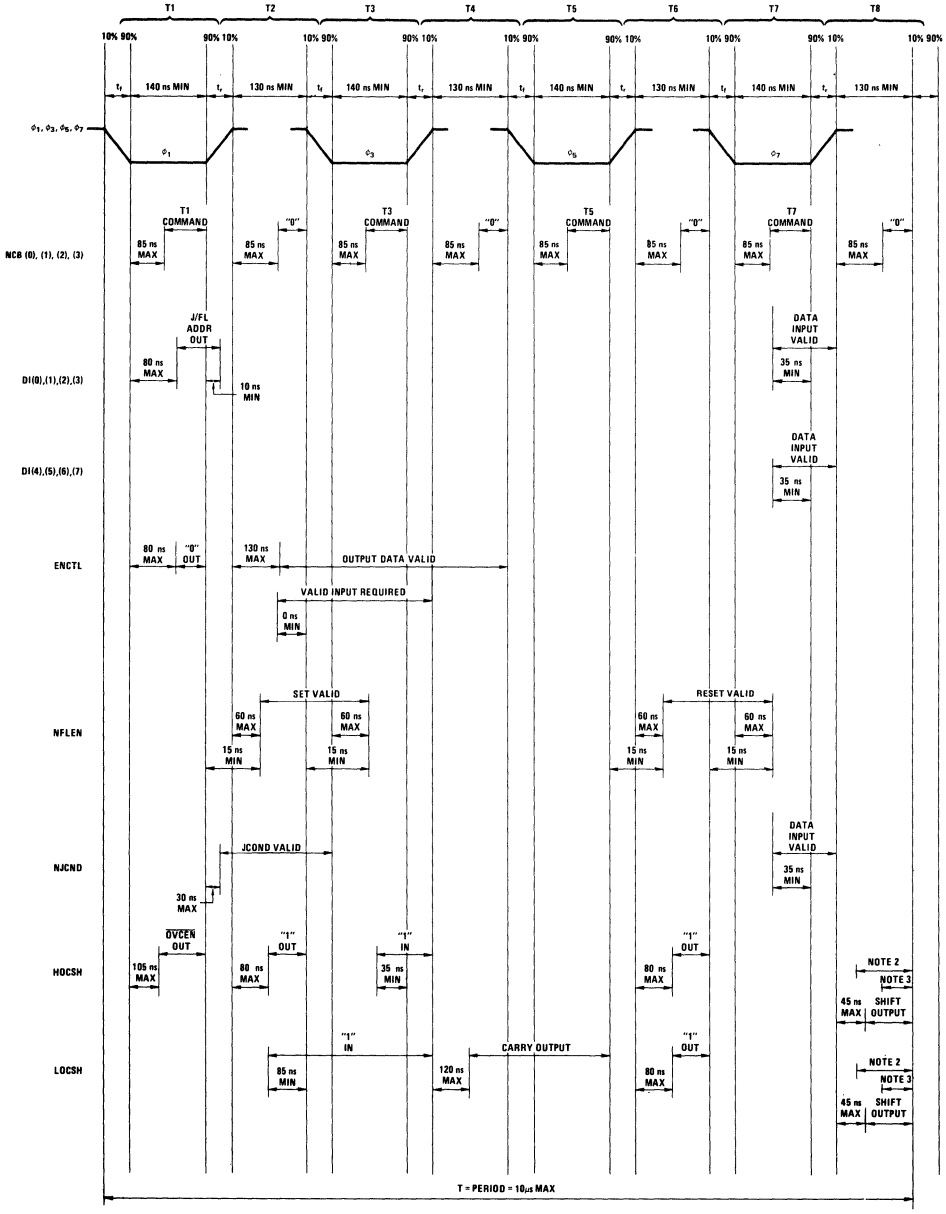


FIGURE 3. CROM Driver and Receiver Buffer

the case of a circular left shift HOCSH serves as an input driven by the most significant RALU and LOCSH serves as an output to the least significant RALU and follows the voltage input at HOCSH. The direction of data transfer is reversed for circular right shift. In the case of open ended shifts the CROM output (LOSCH for left shift and HOCSH for right shift) provides a logic "1" to the RALU (since the shift data is complemented this will provide a trailing "0" for the shift operation) and ignores the shift input data from the RALU. The carry input to the least significant RALU is provided by LOCSH at T_4 and T_5. The overflow and carry flags on the RALU are enabled by the output of HOCSH at T_1. A logic "1" input is required to HOCSH at T_3. This line is precharged to a logic "1" at T_2. A logic "1" input is required for LOCSH at T_2 and T_3. The LOCSH input will be precharged to a logic "1" at T_1 when connected to CSH0 of an RALU.

SIGNAL TIMING SPECIFICATIONS

The timing specifications for all CROM signals are shown in Figure 4. These specifications apply over the complete range of recommended operating conditions. Time intervals are defined with respect to the 10% and 90% points of the four MOS clock inputs. The command outputs on the NCB bus become valid within the first 85 ns of the odd time intervals. These lines are driven to a logic zero within the first 85 ns of the even time intervals. The jump condition and flag address outputs on DI(0) – DI(3) become valid within the first 80 ns of T_1 and remain valid for at least 10 ns after the 90% point at the end of T_1. Data inputs to all DI lines must be valid for at least the last 35 ns of T_7 and must remain valid until the 10% point at the start of T_8. Timing for the remaining signals is similar. (Note that signals may not change state during "valid" time intervals.)



Note 1: t_r and t_f = 250 ns max.
Note 2: Rotate input valid 130 ns max.
Note 3: Rotate output valid 80 ns min.

FIGURE 4. CROM Signal Timing Specifications

(T_A = 0°C to +70°C, V_{SS} = +5V ±5%, V_{GG} = −12V ±5%, V_{LL} = GND)

THE SYSTEMS APPROACH TO CHARACTER GENERATORS

A huge new market for man/machine interfaces is being created by the increasing availability of low cost data processing through computer time sharing, LSI calculators, minicomputers and digital business and control systems. In turn, the pressure is on to design CRT terminals, displays and teleprinters that are at least as compact and inexpensive as the new data processors.

MOS integrated circuit producers are in the thick of this competition. They have begun making read only memories and shift registers with enough storage capacity to put an appreciable dent in terminal and printer costs. Entire alphanumeric character fonts and CRT refresh channels now can be fabricated as single-chip arrays. Low threshold MOS processes and designs have been refined to make the storage arrays more compatible with bipolar logic and standard power supplies.

These developments have won MOS a place on the alphanumeric side of the readout family tree in Figure 1 (and some inroads are being made on the other side—see Appendix in this App. Note. In fact, MOS has pushed beyond the state of the art. MOS/TTL assemblies can generate characters faster than they can be handled by moderately priced CRT video circuitry or printer mechanisms. However, the increased storage capacity and speed also make higher performance systems feasible. For example, designers are considering larger fonts that make characters more legible. Large fonts have generally been economically impractical in the past because even a small increase in font size can double the memory size needed.

MOS ROMS AND REGISTERS

Large capacity, high speed, and bipolar compatibility strike directly at the problems involved in lowering data terminal costs. To generate and update readouts with many characters and symbols takes thousands of bits of storage and fast manipulation of data and control signals. If this capability is supplied in a central processor, it must be paid for in the form of central system overhead and communications costs. Using pre-LSI memory techniques in the terminals, however, can easily double the cost of each console.[1]

Storage capacities per MOS chip have increased at least tenfold in the past few years, with comparable reductions in assembly costs. By the close of 1969, MOS/TTL character generators cost about half as much as those built with bipolar devices. The newest ROMs (read only memories) for character generation represent the integration of some 3,000 diodes and 50 packages of IC gates. One terminal manufacturer who made the changeover late in 1969 replaced six large printed circuit boards with one plug-in card.

The largest MOS ROMs mass produced last year stored 1024 and 2048 bits—general purpose sizes used for table lookup, microprogramming and random-logic functions as well as character generation. A typical generator contained three 1024-bit ROMs, such as National Semiconductor's SK0001 and SK0002 kits (see Table 1 and Figures 2 and 3). Generating the standard 64 ASCII-selected characters in a 5 x 7 font requires a storage capac-

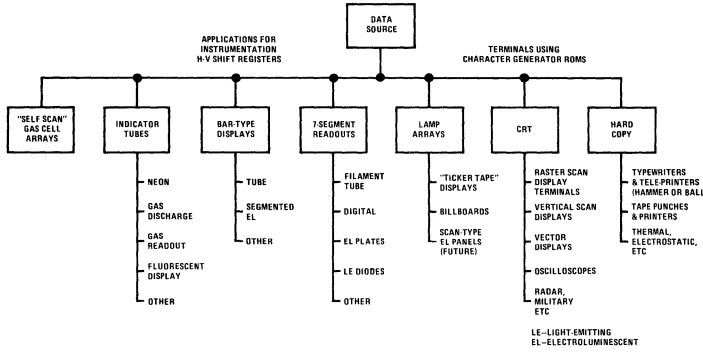


Figure 1. Display Family Tree

ity of at least 5 x 7 x 64. Each logical "1" bit stored in the ROM produces a black dot on a printout or a bright spot on a CRT screen, and each "0" bit a blank space.

Table 1. ROM Combinations for Various Fonts

FONT	CHARACTERISTICS	PARTS REQUIRED
5 x 7	Raster Scan	SK0001 or MM5240
7 x 5	Vertical Scan static ROM required	SK0002 or MM5241
7 x 9	Raster Scan	MM5241 (2 required)
9 x 7	Vertical Scan static ROM required	MM5240 (2 required)
8 x 10	Raster Scan	MM5241 (2 required)
10 x 8	Vertical Scan static ROM required	MM5240 (2 required)
9 x 11	Raster Scan	MM5240 (3 required)
11 x 9	Vertical Scan static ROM required	MM5241 (3 required)
12 x 16	Raster Scan	MM523 (6 required)
16 x 12	Vertical Scan static ROM required	MM5241 (4 required)

Two new soon-to-be-announced ROMs are the MM5240, storing 64 x 8 x 5 bits, and the MM5241 storing 64 x 6 x 8 bits. Each chip also contains decoding logic and sense amplifiers (as do the 1024 and 2048-bit chips). Thus, one ROM is ample for a standard 5 x 7 or 7 x 5 font. The added capacity can implement special needs, such as dropping comma tails below the other characters and symbols. But its main purpose is in providing the logic and programming flexibility that enables ROMs to be operated in tandem to generate the larger font sizes indicated in Table 1. The additional capacity costs little in terms of silicon real estate because these devices are made by low-threshold processes with p-channel-enhancement mode MOSFETs as the storage elements—the most LSI-able type of MOS.

In the past, when diode matrixes were used as character generators, the 5 x 7 or 7 x 5 fonts gave the best cost/legibility tradeoff. Because the new ROMs lower the cost per function, the 8 x 10 font will probably become the most attractive.

The input-output configurations of the MM5240 and MM5241 are outlined in Figure 4 for a standard ASCII-addressed font. The 6-bit ASCII code words will address any of 64 characters (2^6). The control logic generates the three additional address

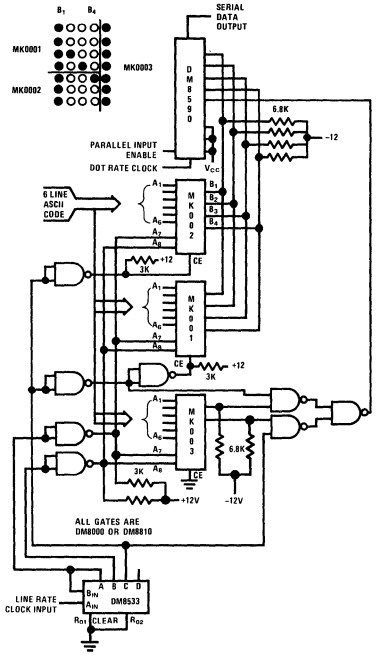


Figure 2a. Three-ROM Raster Scan Character Generators

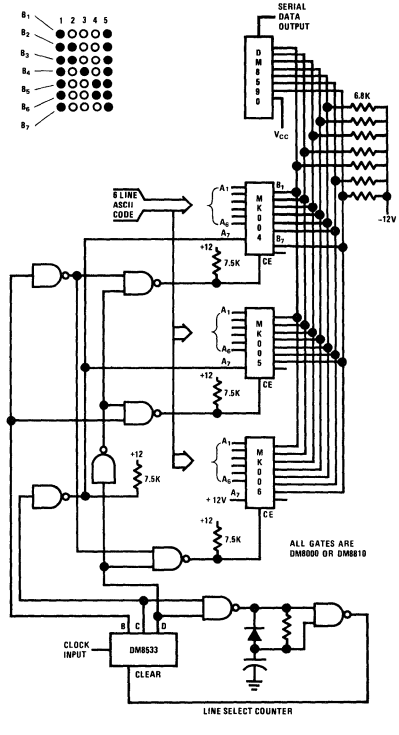


Figure 2b. Character Generator For Tape Printers and Other Vertical Scan Applications

CHARACTER SELECT

I_1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
I_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
I_3	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
I_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
CHAR.	0	8	4	12	2	10	6	14	1	9	5	13	3	11	7	15

ROW
I_5 I_6

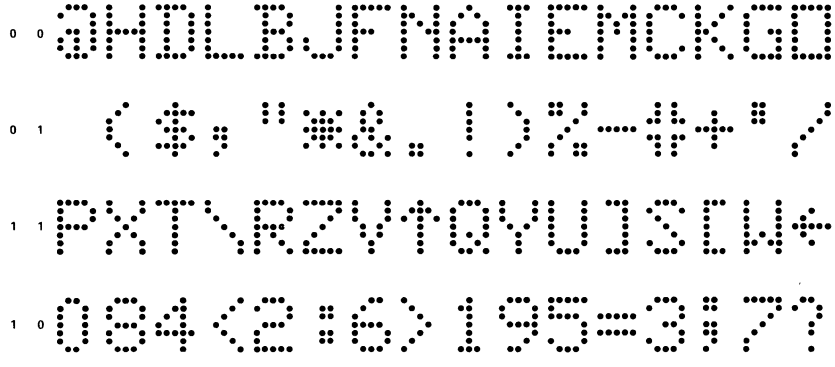


Figure 3a. Raster Scan Character Font

CHARACTER SELECT

I_6	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
I_5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
I_4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
I_3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
CHAR.	0	8	4	12	2	10	6	14	1	9	5	13	3	11	7	15

ROW
I_2 I_1

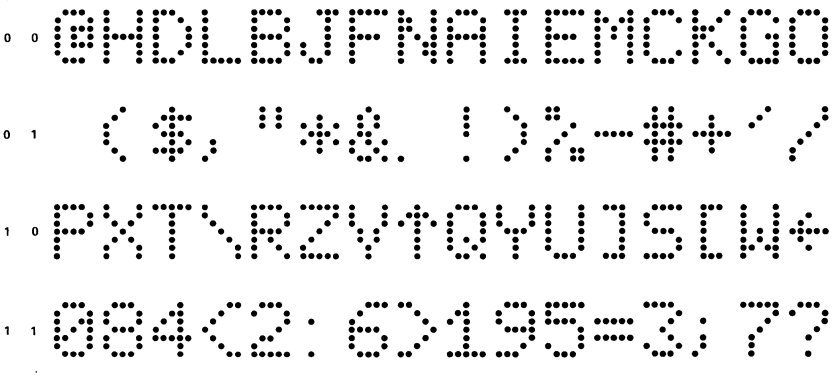


Figure 3b. Vertical Scan Character Font

bits needed to select the individual lines or columns of dots that form the characters in the

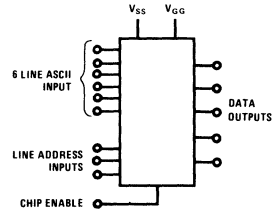


Figure 4a. MM5240 Raster Scan Character Generator Element

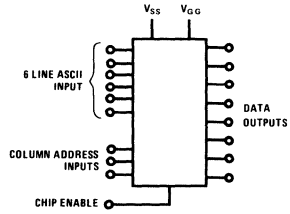


Figure 4b. MM5241 Vertical Scan Character Generator Element

5 x 7 x 64 dot matrix. The output bits forming each dot line or column are presented in parallel. The parallel outputs are serialized by a TTL register and used to control the CRT beam or the printer mechanism. To simplify the selection process, the ROMs are programmed to generate the lines or columns in the correct sequence when addressed by the sequential outputs of a TTL counter.

As for registers, they became quite popular during 1969 because a CRT refresh memory of up to about 5,000 bits—enough for a display of more than 800 characters—could be built less expensively with MOS dynamic registers than with delay lines.[2] This was achieved with registers containing 200 storage stages per chip. During 1970, dynamic registers up to 512 bits long will go into mass production, giving rise to predictions of significant savings in refresh memory costs. Whether savings that large can actually be realized will depend upon how quickly the new devices catch on and go into volume production.

Aside from cost per function, other pertinent consideration are temperature sensitivity and functional flexibility. In a refresh memory, register outputs are fed back to the inputs. On each recirculation, the data readdresses the ROM, regenerating (refreshing) the display (Figure 5). The recirculation times must correspond to the CRT scanning time to keep the display legible. MOS register delay times are relatively insensitive to temperature variations because they are established by system clock rates rather than physical parameters.

Also, special requirements of data entry and output for display formatting and editing can be implemented much more easily with registers than with physical delay lines. Data bit positions in the recirculation loops are maintained in alignment and can be monitored and modulated precisely by the control logic (one recirculation loop is needed for each data bit—six loops, for example, in an ASCII-addressed system). Data entry and output for display or transmission thus becomes a straightforward exercise in logic design.

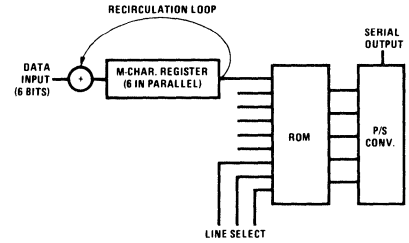


Figure 5. Basic Digital Character Generator and CRT Refresh Memory

BIPOLAR COMPATIBILITY

A dynamic register is one that must be clocked at some minimum frequency. Data is retained in the form of charge storage and the charges would eventually leak out of the storage nodes if not re-established. In contrast, the ROMs being discussed are static devices, generating an output only when addressed. Specifically, they are designed and programmed to be sequenced by TTL ICs. Furthermore, the new generations of ROMs and registers accept and put out bipolar level signals and operate off +5 volt and −12 volt power supplies.

These features eliminate any need for special level-translating circuits between the MOS and bipolar devices. Also, special power supplies are not generally required because ±12V as well as ±5V supplies are usually provided in terminals for other parts of the system. Such compatibility is a convenience and a cost saver in any digital system containing MOS storage subsystems and bipolar logic, since it minimizes the interface and drive complexity. In terminals, though, compatibility is practically essential for efficient operation and lowest cost per function.

First, as the detailed system diagrams show, many of the interconnections have a MOS device at one end and a TTL device at the other, so that a large number of level translators would be needed if they were not compatible.

Second, several control logic operations must occur between memory outputs, and the output-serializing device must operate at least six or eight times as fast as the word (dot line or column) output rate of the ROM. Obviously, if high speed

control logic—preferably TTL MSI devices such as single-chip binary counters and 8-bit parallel-input/serial-output shift registers—were not used, the character generating process would be slowed excessively. This would limit the number of characters that could be displayed in a CRT refresh cycle or printed out in a given time. The new generation of MOS ROMs can deliver up to eight bits in parallel in about 700 nanoseconds, compared with a microsecond or more for last year's models. Logic speeds around 10 MHz are therefore desirable (several times higher than the speed that can be achieved by MOS gates.) Likewise, dynamic registers can now easily be run at rates above 2 MHz—double the speed of early mass produced registers—so the logic controlling refresh storages must also be faster.

The improved compatibility and higher speed are largely due to better design and processing of the input and output stages of the registers and the sense amplifiers of the ROMs. They don't increase the complexity of the MOS circuitry, unlike other techniques for increasing MOS speed, and therefore they have permitted the capacity increases cited.

The net benefit to the system designer of this approach to MOS design is that it enables the system designer to capitalize on the best features of each technology—MOS storage for high density and low cost, and TTL for high speed processing of data and control signals. This is what produces lowest cost per function in most digital systems.

CRT RASTER SCAN DISPLAYS

The basic refresh mode in Figure 5 limits the number of characters that can be displayed. A better way of generating and refreshing raster scan displays, particularly those with many rows or lines of characters, is outlined in Figure 6. Figure 7 illustrates the timing and logical implementation for a multiple row system.

As before, coded data from a communications link or the console keyboard passes through the registers and addresses the character generator. In these examples, the 6-bit ASCII input and the 3-bit control logic input generate raster scan character formats that allow a conventional TV monitor to be used as a display. Communications codes other than ASCII can be used.

If the ROM contains a 5 x 7 font, each 5-bit character line output will form five horizontal bright spots on the CRT. That is, each ROM output generates one-seventh of each character in a row of displayed characters. The output is serialized by the TTL register and used to intensity modulate the CRT beam as it sweeps across the screen.

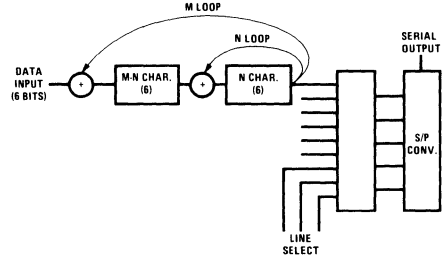


Figure 6. (M-N)+N Technique for Large Page Displays

The refresh memory registers are divided into M-N and N sections to facilitate page displays. M is the total number of characters displayed in several rows (lines of the page) and N is the number of characters in each row. To form such a display with single-loop registers, as in Figure 5, would take seven recirculations of all M data words during each refresh cycle of the CRT. The technique in Figures 6 and 7 only requires high speed recirculation of N bits at a time, with advantages that will be discussed shortly.

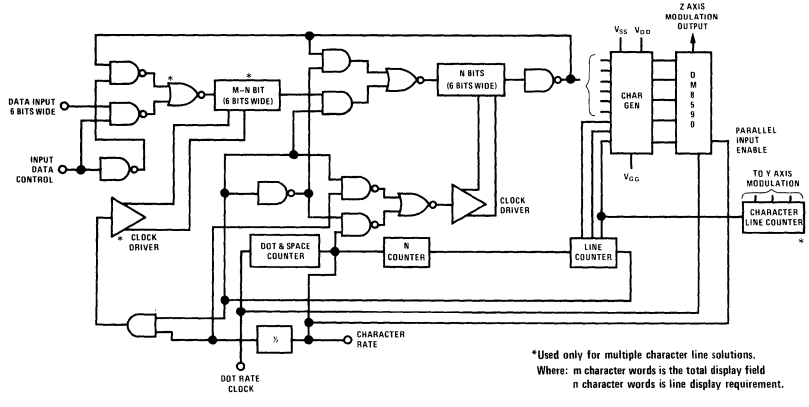


Figure 7. Multiple Row Raster Scan Display System

Assume that on the first sweep of the CRT beam, the ROM is being addressed by the six register outputs representing characters N_1, N_2, N_3, etc. The first horizontal, 5-dot line of each character in the display row are displayed in sequence. Then the line address inputs to the ROM from the control logic change to their second state at the time that N_1 has completed its recirculation to the N register's outputs. Thus, on the second CRT sweep, the second series of 5-dot lines are displayed horizontally for all N characters. At the end of seven recirculations, the complete row of N characters is on the display.

Now, the contents of the N register are not returned to the input of the N register. Instead, they are fed back to the input of the M-N register and this register is clocked to load the N register with the second group of N characters. The M-N register is then held still while the N register recirculates seven times to generate the second row of characters on the display. After all M characters are on the display, the first group of N characters is reloaded into the N register and the entire process is repeated to refresh the display.

Human factors—chiefly the eye's response time—dictate that the display be refreshed at least 30 to 35 times a second for good legibility. Most designers prefer to refresh at 60 Hz power line frequency because it is generally the most convenient frequency.

Besides generating the line address inputs (that is, the number of recirculations of the N register), the control logic keeps track of the number of dots and spaces in he output bit stream. The spaces between characters in a display row are inserted as "0" bits when the ROM outputs are serialized by the TTL register. The counters also control the loading and recirculations of the MOS registers in the refresh memory subsystem.

A multiple row raster scan display could be generated with the M-loop technique in Figure 5 but, the implementation is difficult and impractical. This technique is more appropriate for single row displays. Using this method of display, all M characters to be displayed must recirculate seven times to generate a 5 x 7 horizontal scan, so all stages of the registers must operate at the full character rate. To form several rows with a single-loop memory requires an interlaced scan rather than an ordinary raster scan. The first series of 5-dot lines are generated by the first N character outputs as before, but the next set of N inputs to the ROM will generate the first group of 5-dot lines in the second row of characters on the display. Therefore, the beam must jump to the new line position. To display four rows of 5 x 7 characters, for instance, would require a staircase generator that would step the beam by the height of nine scan lines (seven dot lines, plus two blank spacing lines between rows) three times after the initial scan. Then, as the second of the seven recirculations begins, the beam would have to be shifted an additional line to start the second series of line scans—and so forth.

The M-N-N technique does not require any more register stages than the M-loop technique and significantly reduces control and drive circuit requirements—again producing a lower cost per function.

REFRESH MEMORY MODULATION

The technique employed in the M-N-N refresh memory is called "clock modulation". In other applications, it has already been found to significantly reduce total storage costs.[3] It helps minimize power dissipation—in most terminals, the amount of power consumed is unimportant in itself since line power is used, but registers are powered by clock drivers and the cost and complexity of the drive network is certainly important. Furthermore, the technique allows long, very high-density MOS circuits, produced by relatively inexpensive low threshold (bipolar compatible) processes to operate at very high effective character rates.

As shown in Figure 7, the raster scan system uses nine clock intervals to generate a row of characters on the display. Seven are for the high-speed recirculations. During the other two intervals, the first N characters are fed back from the output of the N register to the input of the M-N register while the N register is loaded from the M-N register with a new row's worth of characters. Since two intervals are used for this operation, the registers operate at only half the character rate. The rest of the time, the M-N register is charge-quiescent. Its average clock frequency is only about 11% of the character rate.

In other words, most of the refresh memory (perhaps 90% in a large display system) operates at only half the character rate (say 1 MHz instead of 2 MHz) only two-ninths of the time. The savings in the drive network alone can be judged from the power-frequency plot for a typical MOS dynamic register (Figure 8)[3]. In addition, the designer can

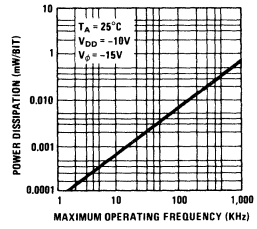


Figure 8. Power vs Frequency Plot of Typical MOS Dynamic Register

increase the number of characters generated per refresh cycle, for a larger display, or increase the number of dot lines, for a larger font, or both.

Remember, though, that dynamic registers must be clocked to retain data. How long can the M-N register be turned off? Long enough for practical applications. The guaranteed minimum frequency is temperature dependent, since temperature affects charge-storage time. The minimum for National Semiconductor's MM-series registers is 500 Hz at 25°C, rising to 3 kHz at 70°C (maximum operating temperature is 125°C, but that is not a display environment). At room temperature, the registers can safely be quiescent for as long as 2 msec. (The typical MM register will actually hold data for 10 msec.) Suppose the N register stores 40 characters and operates at 2 MHz. The quiescent period can be as short as 40 x 7 x 0.5 = 140 μs. If standard TV raster timing is maintained then the quiescent period will be 7 x 63 μs = 441 μs. Obviously, the designer has great leeway in character rates, operating temperatures, and register capacities.

Other applications in displays for clock modulation include input-output buffering of data during data reception and transmission,[2] or during display editing and formatting through the console keyboard. The register rates can be adjusted via control logic to accommodate differences between I/O and recirculation rates. Note that the gating in Figure 7 permits data entry under TTL control into either register section.

CHARACTER GENERATION

The first generally available MOS character generators were kits such as those in Figure 2, using three 1024-bit ROMs (MM521). Although single-chip generators were being developed in 1969, they were in very short supply. The kits cost about half as much as diode generators and thus allowed terminal manufacturers to start the changeover to MOS.

The kits are also a good place to begin describing character generator operation in this application note, because they provide an "exploded view" of multi-ROM generator operation. Similar techniques will be needed to build larger fonts with the new devices. The external gating functions shown in Figure 2 are not needed for these fonts when the MM5240 and MM5241 are used. The "assembly" of the dot patterns is taken care of in the programming of the ROMs. However, to generate a large font, such as 8 x 10 or 12 x 16, with the new ROMs will require operation of two to four ROMs.

Each MM521 in the SK0001 raster scan kit can store 256 4-bit dot patterns. As the inset letter "N" in Figure 2a indicates, the MK001 ROM stores the first four 4-dot line segments of each of the 5 x 7 characters, the MK002 stores 4-bit segments of the other three-dot lines, and MK003 supplies the fifth bit of each of the seven-dot lines. All ROMs are addressed simultaneously.

The 6-bit ASCII code was devised to select 64 (2^6) characters. However, an 8-bit address is used to select the dot lines and the 6-bit ASCII code from the 256 (2^8) word locations in each ROM. These two additional bits are supplied by the A and B outputs of a TTL binary counter DM8533 (SN7493) and the counter's C output is used to commutate the MK001 and MK002. The ROMs are enabled by an output at the TTL logical "0" level. Thus, with the gating shown, the MK001 is enabled during the first four of seven line-rate clock inputs and the MK002 during the remaining three inputs.

The MK003 is continuously enabled by grounding the chip-enabled pin, CE. It must generate a 1-bit output for each of the 7 x 64 dot lines in the 64-character set, which implies a 9-bit address. Rather than produce a special ROM just for this function—which would make it expensive—the MM521 was programmed to generate 256 2-bit outputs from the 8-bit address. The counter's C output simply gates out the unwanted bit.

For a 5 x 7 font, the new single-chip character generators are simply programmed to generate all 5 bits in each dot line, from a 9-bit address. Standard programming provides the 64-character ASCII set, but special characters can be substituted by changing the stored dot patterns. The reprogramming process consists of altering an etching mask that controls gate insultation thickness in the MOS field effect transistors of the storage array. If the oxide is left thick, the transistor will not switch when selected by the decoding logic, generating a "0" output from that location.

Figure 9 indicates why the storage capacity of the MM5240 is 5 x 8 x 64 rather than 5 x 7 x 64—each ROM can generate half of the 8 x 10 x 64 character set. The ROMs can be addressed simultaneously, as before, and be commutated by the

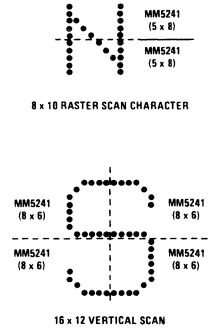


Figure 9. Multiple ROM Character Fonts

control logic to put out the 8-dot horizontal lines in the correct sequence. For very high speed character generation, the addressing of the ROMs can be skewed or overlapped so that the outputs from one are generated while the inputs to the other are being decoded. The only real limitations to the

character generation rates achievable with such techniques are the speed of the bit serializing logic and the bandwidth of the video circuitry.

CONTROL LOGIC

Starting with the dot/character or dot and space counter in Figure 7, the counter moduli are set to accomplish the following functions:

- The dot and space counter determines the number of horizontal spacing bits between characters in the character row on the display. Its output is loaded into the parallel inputs of the DM8590 serial-in/parallel-out shift register. For a 5 x 7 font, for example, a modulus of six inserts one spacing bit (logical "0" bit) between each 5-dot group in the serialized stream. During line recirculation periods, this counter also drives the N counter at the character shift rate of the N register.
- The N counter causes the line select counter to change state at the end of every recirculation of the row data in the N register. It generates a pulse at intervals of 6N dot clock periods (assuming one spacing bit).
- The line select counter generates seven sets of the three address bits that sequence dot-line selection from the ROM.
- A character line counter is needed in some raster-scan displays to keep track of which page line has just been generated. This time is signified by the C or D output of the line select counter.

Outputs of the first three counters actuate the register clock drivers, keeping the line select bits in synch with the data code. If the line select counter is a 4-bit binary device, eight states are available on the ABC outputs (000 through 111). The D output can be used to provide a ninth state and the reset function. Only seven states are needed for line select, so the eighth and ninth states provide the interval needed for loading the N register from the M-N register, as previously described.

VERTICAL SCANNERS AND PRINTERS

Vertical scan character generators are generally used in hard copy applications. Also, a vertical scan type of character generator can sometimes be more suitable for CRT displays than raster scan.

Displays or printouts of calculators and small business machines often show only numerals and a limited variety of symbols—not enough for a full alphanumeric generator. Such fonts are easily programmed into a small ROM such as the 1024-bit MM522, which stores 128 8-bit words. There's room for 16-5 x 7 dot characters on the chip.

These ROMs are also used in the SK0002 kit for a 64-character ASCII-addressed font (Figures 2b and 3b), which requires the storage of 320 7-dot columns and a 7-bit address. Connected as shown, the DM8533 TTL binary counter will reset on the count of 16. And with the gating and interconnections shown, the column select cycle is:

Counter Outputs DCB	ROMs Enabled
DCB	
000	MK004
001	MK005
010	MK004
011	MK005
100	MK006
101	reset (instantaneous)

A CRT beam can be intensity modulated by the serialized output, as in the raster scan technique. However, the electron beam traces either a sawtooth or pedestal-type scan pattern on the screen (Figure 10). Every column of each character in the display line is scanned in sequence, starting at the left-hand side of the screen.

The sawtooth scan is straightforward, but the pedestal scan requires that the bit order be reversed in the second and fourth columns. To do this, the outputs of the MK005 ROM are simply connected to the output buses in the reverse order (i.e., output 1 to bus 7, output 2 to bus 6, etc.).

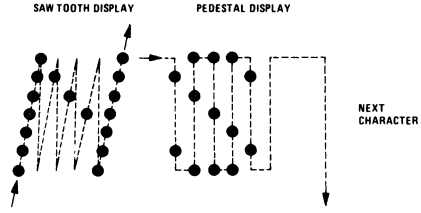


Figure 10a. Two Techniques for Vertical Scan

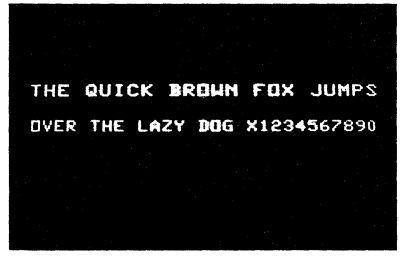


Figure 10b. Example of Character Generation Using Pedestal-type Scan.

Long shift registers, operating at relatively slow rates can be used. The character rate—the register shift rate—is no more than 1/6 of the column-select rate for a 5 x 7 font, since the beam traces one complete character before going on the next one. A dot counter loads spacing bits between characters via the TTL shift register, a character counter triggers the sawtooth or pedestal scanning patterns, and a row counter would control positioning of the beam in a page display system.

In the new single ROM (MM5241) version of this system, (Figure 11), a 9-bit address is needed, 6 bits for the ASCII code and 3 bits for dot column select, Since the ROM stores five dot columns for each of 64 characters in a 5 x 7 font, 3 decode line are necessary. Also, the ROMs are programmed differently for sawtooth or pedestal scanning. Because the output pins are committed for all columns, external connections cannot simply be used to reverse output bit order.

Hard-copy printers can use the same fonts as vertical scan CRT displays. MOS registers may be used for data input buffering, but of course refresh registers are not generally required. The character generator output may be used to select some combination of 35 hammers, needles or electrodes that print the 5 x 7 dot patterns on the paper. One technique for handling the character generator output is shown in Figure 12.

In Figure 12, a TTL counter connected to divide by six (five columns and the blank column space between characters) generates the column select address. The ROM's outputs are accumulated in TTL latches (or held in TTL serial-in/parallel-out shift registers). When all dots for a character are ready, they are printed. In tape printing applications in which a 7-transducer array sequentially prints or punches a column at a time as the paper moves under the transducers, the ROM outputs can be used as they are generated unless storage is required for some other purpose.

Character generators are not needed for conventional electromechanical typewriters. But MOS ROMs do have a role here—one version of the MM521, for example, is programmed to convert the ASCII communications code into the Selectric code used to control ball-type printers.

PRINTING APPLICATIONS

The application of character generators in a printing application is normally quite different from that of the display system. Most printers require that a total character font be available before the print is executed. An example of a practical method of accomplishing this (Figure 12) is to sequence the character generator element through the font sequence. Each of the character columns or rows is addressed. The character generator output data at each of these address intervals is transferred into bipolar memory. This

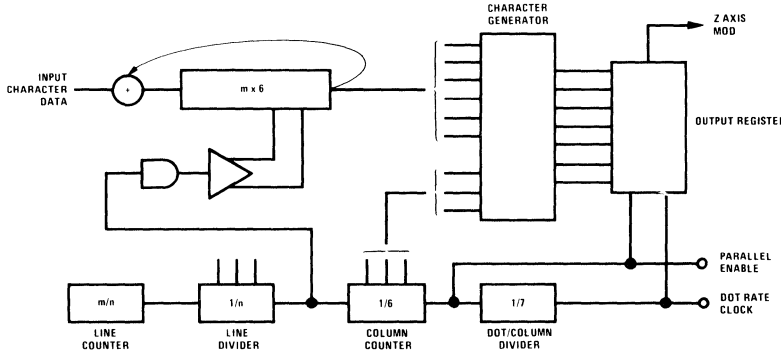


Figure 11. Vertical Scan Display System

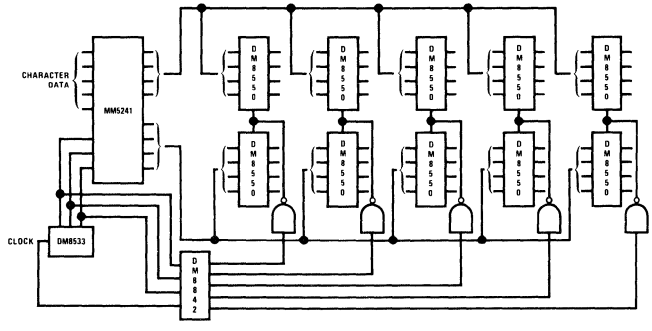


Figure 12. Printer Application Block Diagram

memory not only satisfies the memory storage but also the general power buffer which is required between the MOS character generator and the electromechanical on thermo electric printer. In the printer application there may be a requirement to buffer the input data with data storage because of the relative differences in data and printer rates but generally there is no need to retain the printed character intelligence.

The data transfer from the character generator to the bipolar memory in Figure 12 is accomplished by sequencing the column address lines and enabling the appropriate memory simultaneously. Each pair of DM8550s (SN7475s) then contains the data for one of the five columns in a character. The DM8842 (SN7442)—one in 10 decoder provides the decoding functions which are connected to the enable line on the quad latches.

LARGER, FASTER SYSTEMS

Most low cost terminal designs have been based on the 5 x 7 font because of the high cost of diode matrixes and wideband video circuits. But it is by no means the most legible font. A 5 x 7 font is acceptable for applications in which the display changes slowly, but human engineering studies indicate that it causes severe eyestrain when an operator reads rapidly changing data.

The greatest portion of the discussion has dealt with a 5 x 7 font. A full 64 character display can be coded into a single MOS package. Now that LSI has entered the scene, we see a different trend towards larger, more stylized font. The economy of MOS ROMs will provide the customer with a more legible character font at the present cost of "discrete" character generators. An analysis of the most practical solutions to various fonts are tabulated in Table 2. The part types which have been used to generate a 64 x 7 x 5 raster scan font are the SK0001-3 ROM kit or the MM5240 which is under development. The vertical scan font is satisfied by the SK0002-3 ROM bit or the MM5241 which is under development. If we examine the other possible fonts, these same two monolithic elements will satisfy the requirements if they were 64 x 8 x 5 and 64 x 6 x 8 respectively. Therefore, the added memory storage is being incorporated into the MM5240 and MM5241. In some of these cases the font is scanned in the horizontal dimension while in others the font is scanned in the vertical dimension. You find both the 8 x 5 and 6 x 8 elements capable of satisfying the font matrix requirement. Since all the ROMs listed are static by design, there are no special clocking hardships induced with the solution of any of these larger fonts. This is not true for all dynamic ROM solutions.

As mentioned before and shown in the table, the same ROM element is used in both raster scan or vertical scan applications. If we recall the design solutions showing the refresh memory and character generator for a 5 x 7 display, the first thing which is apparent is that the sequencing of the character generator is different in each of the two basic techniques. In one case the character generator is sequenced at the character rate (raster scan) while in the other case the generator element is sequenced at the column rate (vertical scan) of the font.

Since a display utilizing the vertical scan techniques has input address changes at some multiple of the display character rate, a clocking system for a dynamic ROM character generator must be supplied. This requires the addition of a frequency divider and clock generator which results in a higher system cost when dynamic ROMs are used.

A second consideration which should not be overlooked in systems cost is the compatibility of ROMs in multi-package character fonts. Optimum ROM usage and organization will result in lower systems cost. ROMs will also find applications in micro-programming and code conversion where synchronous operation is preferred.

The 8 x 10 font is much better and 12 x 16 is almost optimum for legibility. Small, lower case characters can be sharply defined, too, and they almost appear to be drawn with continuous strokes.

System designers considering these fonts for low-cost displays run, at present, into CRT cost problems. The least expensive displays are television-type CRTs with limited video bandwidth. Bandwidth also limits the number of characters that can be displayed simultaneously. Not counting the times required for beam retrace and functions other than character generation, which reduce the time available in a refresh cycle for dot handling, the necessary bandwidth is roughly:

BW = (dots and spacing bits per character)
× (characters per display row or page)
× (refresh rate)

TV-type CRTs have a maximum bandwidth of about 4 MHz, of which only about 2.5 MHz is generally useful. If one uses a 5 x 7 font with one spacing bit (6 x 7 total) at a 60-Hz refresh rate, each displayed character needs 2.52 kHz of bandwidth, so the limit is about 1,000 characters. In contrast, the new ROMs take as little as 700 nanoseconds to generate a dot line, or about 5 μs per character. That's fast enough to generate 200,000 characters a second, or a display of more than 3,000 characters at the 60-Hz refresh rate. The actual dot rate in the serial bit stream to the CRT can approach 10 MHz. And if larger fonts are generated in some multiplexed addressing mode, the required bandwidth can be much higher.

Luckily, these problems are not insurmountable and there are alternatives to using oscilloscope-quality CRTs or storage tubes, which are fine for high performance applications but too rich for low cost terminals.

Obviously, the designer can drop the refresh rates. New CRTs with longer persistence phosphors facilitate this. Also, CRT manufacturers have been responding to the new terminal market by working on bandwidth improvements, and they are apparently going to reach 10 MHz in moderately priced video systems soon.

Finally, the designer is not obliged to display his characters digitally just because he uses a MOS ROM. Don't forget that the ROM is really working as a code converter, generating a 35-bit machine language code from a communications code. The language translation can be whatever the situation requires.

All that need be done is update methods used in analog displays, which form characters with strokes rather than dot lines or columns. The ROMs can be programmed such that the bit outputs, when integrated, control X and Y ramp generators. The slopes of the ramp functions are determined by the number of bits in a sequence and the lengths are determined by the locations chosen for turn-off bits. As in the vertical scan technique, the ROM is addressed at the character rate.

Even though some characters can be formed with one or two strokes (I, L, etc.), equal time should be given to all characters in a page display to keep the character rows aligned. A standard sized area of the MOSFET array, such as 6 x 8 or 5 x 8 should be used for each character. Most patterns would thus be a combination of stroke and no-stroke outputs. The single-chip fonts have an 8-stroke capacity for each of 64 characters which is more legible than the standard segmented type of instrument readout, since slant lines could be generated wherever needed.

APPENDIX

WHAT ABOUT INSTRUMENTS AND CONTROLS?

While it is safe to predict that 1970 will be "the year of the MOS" in alphanumeric terminals, MOS applications in numeric readouts are just beginning to emerge.

A new device with considerable promise in this field is a high voltage, MOS static shift register, the MM5081. Developed by National, it has a TTL-compatible serial input, 10 parallel outputs that can stand off −55V, 10 latching-type storage stages, and a serial output.

This novel combination of functions means that the MM5081 can drive lamps, numeric indicator tubes, filament tubes in segmented number and symbols displays, electroluminescent panels, and the new gas-cell arrays. In short, it provides MOS with a good foothold on the numeric side of the readout family tree in Figure 1.

The register stages can either shift the bits to the serial output for recirculation or store the data indefinitely. Hence, displayed characters can be swept along a line of indicators, "frozen" on a stationary display, or made to reappear periodically at any desired repetition rate.

A code-converting/character-generating ROM can be placed at the register input, to display numbers and symbols or alphanumerics. A designer can get almost as much flexibility from a lamp or panel display as from a CRT display. In fact, the first application of the MM5081 is controlling a matrix of neon lamps in a moving billboard display.

Some applications for character generators in instruments are also cropping up. Displaying range scales on an oscilloscope is a good idea that can be improved upon with the new ROMs. The display frees the operator of the chores of mentally calculating scale factors and manually writing these on scope photos. With an alphanumeric font, the camera can also record information such as test conditions, date and time of test, identification numbers, etc. Photo sequences and the data needed to analyze the curves can be coordinated automatically.

Similarly, a ROM can be programmed to display standard curves for go-no-go equipment checkout operations. For example, if a radar's pulse amplifier should have certain output characteristics, the ROM generates the correct output curves through a digital-to-analog converter and stroke generator. When an actual operating characteristic and the reference curve are displayed simultaneously, the operator can tell at a glance whether the radar is functioning properly. Many curves or general purpose curve segments can be programmed into a ROM and picked out as needed with selector switches or a ROM microprogrammer.

ROMs can be programmed as lookup tables, random-logic synthesizers,[4] encoders, decoders, and microprogrammers as well as character generators. A single ROM can perform limited combinations of these functions, virtually qualifying it as a microcomputer. It has been suggested that this capability be used in control panels to perform functions like actuating an alarm when a transducer level goes out of range and initiating corrective action. ROM addresses can be derived from digital meter circuitry. In multi-point measuring systems, this would provide the solid state equivalent of a rack of meter relays.

DEFINITIONS OF DISPLAY TERMS

Font: A set of printing or display characters of a particular style and size. A typical dot-character font is 5 x 7, referring to the number of dot locations per character.

Dot Character: A character formed by a pattern of bright dots on a CRT screen or dark spots on hard copy, rather than by continuous strokes. The dot

pattern corresponds to bit-storage patterns in a digital memory.

Column: In a dot character matrix for vertical scanning, a column is a vertical series of dots. On a page display, a column contains several vertically aligned characters. In this article, a column refers to a dot column.

Row: A horizontally aligned group of characters on a display.

Line: In this report, line refers to the number of dots displayed in a single scan when a raster scan character is generated. In a 5 x 7 dot character, there are seven lines of 5 dots each.

Page: A display consisting of several rows of characters, corresponding to lines on a printed page.

Raster Scan: See Figure 9.

Vertical Scan: Two types of CRT vertical scans are shown in Figure 10. In hard copy applications, the dots in a column or character may be printed simultaneously by the printing transducers rather than being scanned.

Sawtooth Scan: See Figure 10.

Pedestal Scan: See Figure 10.

Dynamic Element: A digital device that must be clocked. A dynamic shift register must be clocked to retain data. A dynamic ROM is clocked to decode the address and generate an output.

Static Element: A device that does not have to be clocked to retain data. A static ROM uses direct coupled decoding for bit selection and static output buffers.

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HIGH VOLTAGE SHIFT REGISTERS MOVE DISPLAYS

There was a time when one had to go to Times Square or Picadilly Circus to see a moving lamp display. But now they're going into stadium scoreboards, stock brokers' offices, waiting rooms and many other places where an attention-getting man-machine interface is wanted.

Naturally, display designers would like to make the control and drive circuitry more compact and less expensive. What's needed to replace the banks of discrete switching devices is storage and switching high-voltage circuits in monolithic form. That's exactly why National developed the MM5081 high-voltage MOS shift register.

This unusual IC is the first MOS device capable of driving gas-discharge tubes and other high-voltage display elements without going through a bipolar buffer such as a transistor or SCR. Moreover, it can "walk" the message around and around the display when operated in a recirculating mode. The latter feature provides a clear-cut division between system functions – the MM5081's take on the responsibility of display operation per se, while the system logic need only format messages and control updating by invading the registers. In other words, the main system logic need pay only intermittent attention to display operation. If the main system is a data-processing computer, for instance, it can handle the display like any other peripheral. Relieved of responsibilities for moving and refreshing the display, the main system can do more data processing between display updates.

REGISTER PLUS SWITCHES

Figure 1 shows in simplified form how one MM5081 would be connected to drive a bank of 10 neon lamps. A data bit stream is entered into the serial input and shifted at the clock rate to the serial output. Then, it can be routed back to the input and recirculated to repeat the display motion.

The states of the data bits circulating through the register control the switching of the MOS output transistors. When a bit in the true state (MOS logical "1") is being stepped down the 10 register stages, the lamps will turn on and off in sequence at the register clock rate. In this mode, the clock rate is the display rate. A typical display rate will move the light along by no more than two or three lamps per second, making any message displayed on parallel rows of lamps easy to follow and read. A latch-type register cell that can shift at frequencies to DC and a single-phase clock input are used in the MM5081 to achieve this effect. However, the logic formatting the data for display will have to run at some higher rate. If the control system has other functions as well, it may be desirable to load the register at a clock rate in the hundreds of kilohertz. At such a high rate, the bit stream flashes by the 10 parallel output switches too rapidly to see the lamps being turned on. After loading, when the main system logic is freed, the clock rate is dropped to the display rate and the message is seen. The message simply recirculates at the display rate until new data is ready for loading.

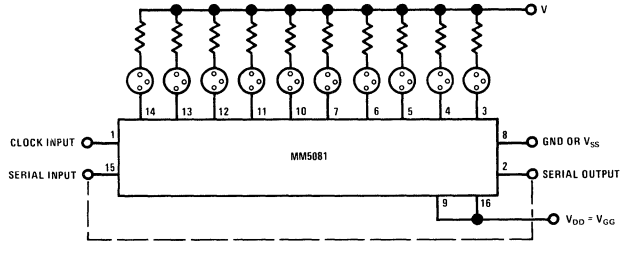

FIGURE 1. Block Diagram

The use of high-speed logic for control is facilitated by making the MM5081 with low-threshold, p-channel, enhancement-mode MOS transistors. As a rule, a low threshold device allows data to be entered at bipolar logic levels.

The output transistors do not need a large gate-voltage change to turn on and off. They are also low-threshold devices in this sense. But they have to withstand transients up to 100 volts and stand off steady state voltages up to 55V to operate lamp-type displays reliably. Adequate gate logic voltages for the output transistors must be ensured to make the lamps glow brightly when they should be on or to make them free of any residual glow due to switch leakage when the switching transistors are turned off. That is, a low R_{ON} and high R_{OFF} must be ensured despite very high voltage on the MOSFET drains. Because a pullup resistor is used, the input gate should be a TTL or DTL device with an uncommitted-collector output able to withstand at least 10V. Among such devices are the DM8810, DM8811 or DM7426 (SN7426) quad NOR-gates, or the DM8812 hex inverter. All these TTL devices will stand off to 14V.

The other two gates used in the input switch can be any TTL or DTL types. The arrangement shown brings the serial output back to the serial input through the top gate when the "new data enable" line is low (DTL/TTL logical "0") or permits the registers to be reloaded with new data when the enable line is high. A pull-down resistor is placed on the register output to handle 1.6 mA the current sinking required for operation of the TTL or DTL recirculation control gate.

TICKER-TAPE DISPLAY

A straightforward type of moving lamp display is illustrated in Figures 2 and 3. Simple messages such as CALLING DR. CASEY . . . CALLING DR. CASEY . . . DR. CASEY, PLEASE REPORT TO SURGERY . . . or stock quotes, or a series of instrument readings would be displayed as 7X5 characters by this system. That is, each character would be a lighted lamp pattern selected from a moving matrix seven lamps high by five lamps with a moving column of lamps turned off between characters. The off column is a space bit in each lamp row.

Assume that the display is long enough for 33 characters. Each row requires 33X6 lamps and 198 register stages. Each row is a cascade of 20 MM5081's. The input of the first register and the

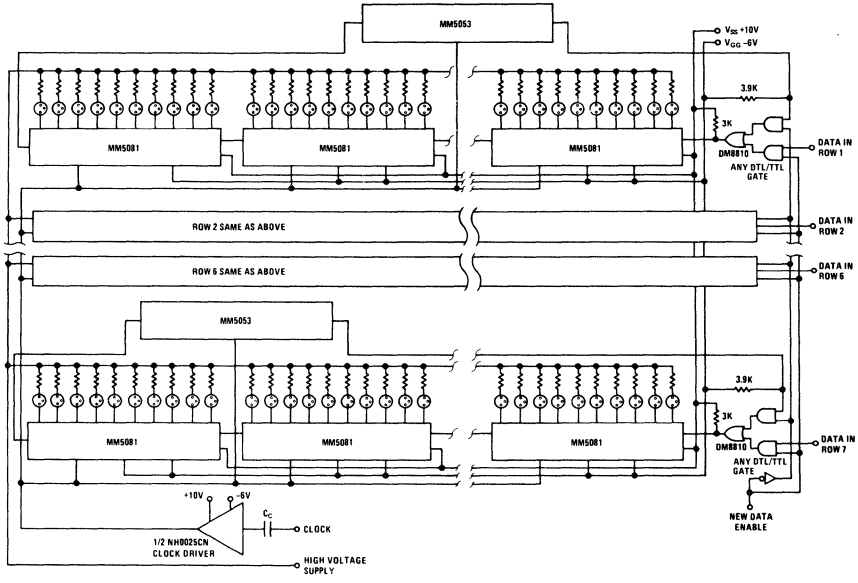

FIGURE 2. 7XN Bit Shift Register and Display

output of the last register are connected as in Figure 1, and the registers in between are simply daisy-chained by connecting each serial output to the next serial input. All seven rows would use 140 register packages.

The character data for this type of system can be formatted by a standard character generator. For instance, the standard ASCII code can address a bipolar compatible read-only memory such as National's MM5241AA, which is programmed to generate 5X7 dot-type characters for CRT display. However, in the lamp display system, the display refresh function is handled without an additional memory. The column bits are entered in each register chain, as before, through the input gating at a rate determined by the clock rate supplied the MH0025C clock driver. The MH0025C is a two-phase driver. However, since the MM5081 takes a single-phase clock input (converted to a two-phase clock inside the register package), only one of the dual drivers in the MH0025C package is shown (the other half can be used to share the clock-drive load).

After the registers are loaded, the clock into the driver is dropped to a frequency of 2 Hz, if the register was loaded at a higher frequency. This rate is stabilized by the coupling capacitor C_C. The coupling capacitor on this type of driver determines the maximum pulse width, but the minimum pulse width is established by the clock signal. So, at the lower frequency, the characters sweep smoothly from right to left across the display lamps. They repeat the message every 100 seconds because 200 register stages are in each of the seven parallel rows.

Both the clock driver and the registers operate off the 10V and –6V power supplied.

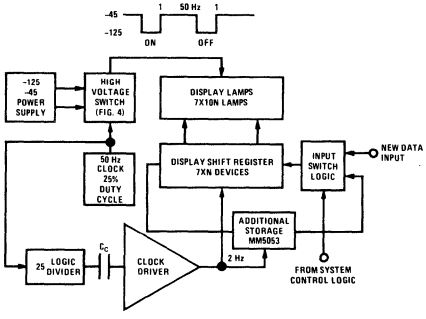

FIGURE 3. System Block Diagram

DISPLAY DRIVE

The high voltage supply (shown in the block diagram in Figure 3) is generated from a high voltage switch. The purpose is to limit the current and voltage across the lamps and the MOS output transistors to ensure that they operate reliably and have long lives. Also, the method reduces power consumption and allows lower power, inexpensive high-voltage power supplies to be used.

The high-voltage switch seen in Figure 3 and detailed in Figure 4 switches at a rate of 50 Hz and a duty cycle of 25%. Thus, when any of the MOS output transistors is on, the lamp that is "on" during that 250 msec display-rate interval (100% duty cycle at 2 Hz) is actually on for only 5 msec at a time. Then it turns off for 15 msec. This refresh rate was chosen because it provides a good lamp intensity with no apparent flicker.

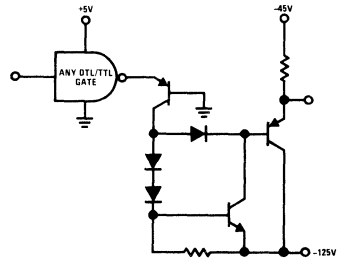

FIGURE 4. High Voltage Switch

The –125V supply turns on the lamps, and the –45V supply turns them off. But what is actually being used is the voltage difference, or bias. Most glow-discharge lamps require a 65V starting voltage and a 60V holding voltage. The switch keeps the lamps alternating between these levels while the MOS transistors are on, but imposes a maximum voltage of only –65V on the MOS transistors (that is, 125–60V) for the 5 msec "on" time. The MM5081 can easily take this – the spec allows –100V at 60 Hz (or 16.66 msec) and they are stress-tested to this level.

INDUSTRIAL DISPLAYS

The characters displayed can be any kind of symbol within the resolution of the lamp array – from letters to cartoon characters – and within the flexibility of the controls. Getting patterns to move back and forth while changing shape is technically feasible, but would require complex clocking techniques to put the bits in the desired location. Static pictorial displays would be fairly simple to implement, merely requiring loading of the registers at a high rate followed by storage at a DC display rate for the desired time. Although the characters would appear static, the high-voltage switch would keep the actual duty rate low.

There are many potential new applications for moving-lamp displays in industrial control systems. Functions such as process flow rates through several feeder pipelines or subassembly line rate in an assembly plant, cannot easily be set up on a CRT display. Complex computer graphic techniques or very expensive multi-gun displays may be needed.

The clock rates and lengths of a number of rows of lamps can readily be adjusted by hand-operated controls, such as voltage-controlled oscillators and gating between registers chosen by selector switches. Any feeder-line display rate that can be represented by the display rate could therefore be varied at a compressed scale of time and distance until the display operator arrived at the optimum balance of rates. This is a visual approach to a problem that generally requires complex mathematics and analog computers to solve.

Nor do the rows of lamps have to be aligned. Individual rows might represent route sections in a transportation network between junctions. By driving each section at a display rate simulating the speed of a particular train, and switching the "train" of moving lights from row to row via switches at the junctions (serial output to serial input register connections), control personnel could simulate system operation. Problems such as tie-ups – or worse – at junctions could be worked out by varying display rates for the trains whose schedules conflicted.

LOW FREQUENCY OPERATION WITH DYNAMIC SHIFT REGISTERS

In many dynamic shift register applications, it is advantageous to operate the circuit at low clock frequencies or in clock burst modes where high frequency clock rate periods are followed by long intervals in which the clocks are absent. To insure that his system will operate correctly under these conditions, the designer should be aware of the limitations of the type of shift register he is using.

There are two basic forms of dynamic shift register cells: the ratioless and the ratio. The ratioless circuit of Figure 1a is based on a capacitor precharge concept. During ϕ_{IN} clock time, node B is precharged by transistor Q_3; i.e., Q_3 is turned on by ϕ_{IN}, creating a low impedance path from node B to V_{GG} which charges the node capacitor C_2 to a negative voltage. Data is coupled at the same time through transfer transistor Q_1 to node A, the gate of Q_2. If the incoming data is a positive or "0" level, Q_2 will be in a high impedance off state, and node B will charge to a negative voltage one threshold more positive than the ϕ_{IN} clock amplitude.

When ϕ_{IN} returns to a positive level. Q_3 is shut off, isolating the precharged voltage of node B. The stored charge of node B, coupled with an additional increment contributed by C_4, redistributes between nodes B and C when the ϕ_{OUT} clock turns on transistor Q_4. The redistributed charge develops a negative voltage "1" level across C_3 which becomes isolated when ϕ_{OUT} returns to a "0" level. The "1" level turns on Q_5, resulting in a low impedance path between the output of the cell and V_{SS}, establishing a "0" level at the output.

In the ratioless cell, there are two nodes which become isolated from any charge replenishing source during normal operation of the circuit: nodes B and C. These are the nodes which establish the low frequency limitations of the cell. In most designs node C, the gate of the logic transistor Q_5, is the limiting node because total capacitance is less. If we had assumed the initial data coupled by Q_1 during ϕ_{IN} to be a "1" level, then node A would of course be the limiting node of the cell.

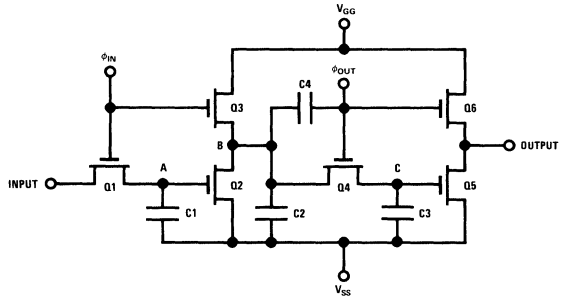

FIGURE 1a. Ratioless Dynamic Shift Register Cell

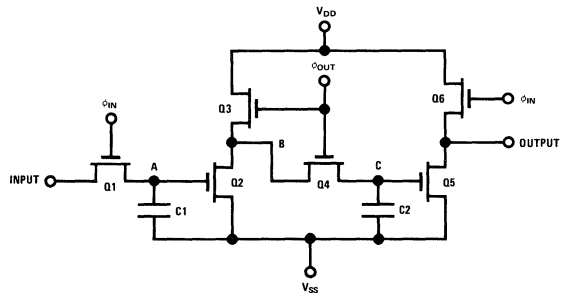

FIGURE 1b. Ratio Type Dynamic Shift Register Cell

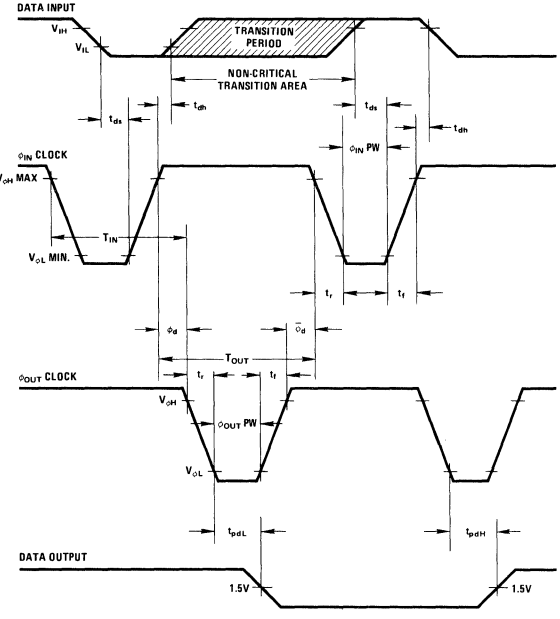

FIGURE 2. Timing Diagram For Two Phase Dynamic Shift Registers

The ratio dynamic shift register cell of Figure 1b has only one isolated node which limits minimum frequency operation. It, like the ratioless cell, is the gate node of the logic transistor. The ratio cell does not rely on stored precharge to establish a "1" level on a succeeding logic gate mode. If a "0" level had been transferred to node A of the ratio cell by Q_1 during ϕ_{IN} time, Q_2 would be off. A ϕ_{OUT} "1" level would turn on Q_3 and Q_4 creating a charging path between node C and V_{DD}, resulting in a "1" level at node C. The node would be isolated by Q_4, just as in the ratioless cell, when ϕ_{OUT} returns to a "0" level.

If the data coupled by Q_1 had been a "1", both Q_2 and Q_3 would be on during ϕ_{OUT} time. To establish a "0" at node B in that case, an electrical ratio between the on impedance of Q_2 and Q_3 must be considered by the cell designer.

Charge must be stored at the logic transistor gate node of the ratioless cell for the period of time between leading edges of the two phase clocks. This is because no charge enters the node B and C network after the leading edge of the transfer clock (ϕ_{OUT}) and there is no way for charge which leaks off the nodes to be replaced. This portion of the clock period is defined as a Partial Bit Time. The Partial Bit Time between the leading edge of ϕ_{IN} and the leading edge of ϕ_{OUT} is the T_{IN} period, and the time between the leading edge of ϕ_{OUT} and the leading edge of ϕ_{IN} is T_{OUT} (Figure 2).

The period of the minimum operating frequency is the sum of the two, or

$$\phi_f\,(\text{MIN}) = \frac{1}{T_{IN} + T_{OUT}} \qquad (1)$$

Obviously the lowest operating frequency can be attained when T_{IN} and T_{OUT} are each at their maximum limit and therefore equal. This says that for minimum frequency, 50% clock phasing should be used, i.e., the clocks should be equally spaced within the bit time.

The ratio cell has a similar storage requirement, but with one difference. During the time the transfer clock (ϕ_{OUT} in Figure 1b) is on, a source of charge is available to node C through the ON transistors Q_3 and Q_4, assuming Q_2 is OFF. Therefore, charge must be stored on the critical capacitor C_2 only after the transfer clock has returned to a "0" level, and isolated the node. This required storage time is usually referred to as Clock Phase Delay Time (ϕ_d). The phase delay time between the trailing edge of ϕ_{IN} and the leading edge of ϕ_{OUT} is ϕ_d; the time between the trailing edge of ϕ_{OUT} and the leading edge of ϕ_{IN} is $\overline{\phi}_d$ (Figure 2). Minimum clock operating frequency is:

$$\phi_f\,(\text{MIN}) = \frac{1}{\phi_{IN}\,PW + \phi_d + \phi_{OUT}\,PW + \overline{\phi}_d} \qquad (2)$$

assuming clock rise and fall time $\ll \phi_{PW}$.

Optimum low frequency operation can be obtained when the clock pulsewidths and phase delays are maximized and made equal. In most cases this would mean 10 μs clock pulsewidths and 50% clock phasing. For power or system application reasons it is usually not convenient to use such wide pulsewidths, and the minimum clock frequency is simplified to

$$\phi_f\,(\text{MIN}) \cong \frac{1}{\phi_d + \overline{\phi}_d} \qquad (3)$$

assuming $\phi_{PW} \ll \phi_d$ or $\overline{\phi}_d$.

Maximum Partial Bit Times and Clock Phase Delays for a given circuit are a measure of the ability of the critical nodes within the cell to store a minimum voltage level. Charge is usually lost due to leakage currents associated with the semiconductor junctions of the nodes. The total reverse leakage current for a p-n junction is the sum of three components; the bulk diffusion current, charge generation current and surface leakage current. Within the normal operating junction temperature range of MOS shift registers (−55°C to 150°C), the charge generation current is the primary component of leakage. Charge generation is usually attributed to recombination centers within the depletion layer of the junction. Leakage current generated in this manner is usually approximated by the expression

$$I_L = KT^{3/2}\,\epsilon^{-7020/T} \qquad (4)$$

Where T = Junction temperature, °K

K = Proportionality constant

I_L = Leakage current of P-N junction

Therefore Partial Bit Times and Clock Phase Delays will be a definite function of temperature. Figure 3 shows a curve for Partial Bit Times as a function of temperature for a typical shift register using a ratio-less cell. Figure 4 gives the corresponding minimum operating frequency versus temperature for two cases: when $T_{IN} = T_{OUT}$ (50% clock phasing), and when one of the Partial Bit Times is minimized, the other maximized. Minimum Partial Bit Time is:

$$T_{(MIN)} = \phi\,PW_{(MIN)} + \phi_{tr} + \phi_{tf} + \phi_{d(MIN)} \qquad (5)$$

Any Partial Bit Time between minimum and maximum at a given temperature can be used. The minimum clock rate would be calculated using Equation 1.

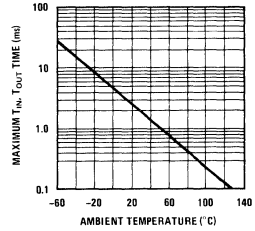

FIGURE 3. Maximum Partial Bit Time vs Ambient Temperature

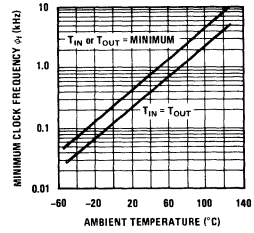

FIGURE 4. Minimum Clock Frequency vs Ambient Temperature

If the shift register utilizes a ratio cell, a curve identical to Figure 3 could be used to obtain maximum Clock Phase Delays for any required temperature. Equation 2 or Equation 3 could then be used to calculate minimum clock frequency at that temperature.

The shift register user can often increase his margin of safety when operating at low frequency, or for long periods of time with the clocks stopped, by designing the system with that operation in mind. The ambient operating temperature of the registers should always be minimized. The cell requires a minimum voltage at the critical node to operate, and the time to discharge the node to that value is dependent upon the initial voltage, as well as capacitance and leakage:

$$t_d \approx \frac{C_{NODE}\,(V_{INITIAL} - V_{MIN})}{I_L} \qquad (6)$$

t_d = T_{IN} or T_{OUT} for ratioless cells;

= ϕ_d or $\overline{\phi}_d$ for ratio cells

C_{NODE} = Total capacitance at critical node

$V_{INITIAL}$ = Voltage at critical node immediately after isolation of that node by transfer clock.

V_{MIN} = Minimum voltage required at critical node for operation.

I_L = Total leakage current at critical node.

The initial voltage can be optimized in two ways: by using the highest clock amplitude possible and by allowing something greater than minimum clock pulsewidth to insure that the maximum amount of charge is coupled to the node (and in the case of the ratioless cell, that the maximum precharge voltage is obtained before transfer). A high value of V_{GG} or V_{DD}, the negative supply voltage, increases on-chip power and therefore junction temperature, as well as increasing the minimum required node voltage. It is a good idea, therefore, to stay away from very high supply voltages. When both the clock driver reference voltage and V_{GG} or V_{DD} are the same supply, the best tradeoff is toward the higher end of the specified range, however. One other consideration which applies during operation at any frequency, but particularly at low frequency, is excursions of the clock line more positive than V_{SS}. This forward biases internal junctions which results in parasitic PNP transistors. If the collector of the parasitic PNP happens to be a critical node, the circuit will fail. Because critical nodes are often closer to the minimum required voltage during low frequency operation, registers are usually more sensitive to positive clock spikes.

When calculating temperature effects of a system operating in the clock burst mode, the designer must remember that power dissipation in the shift register is approximately double at 2.5 MHz what it is at 100 kHz. High frequency bursts will heat the chip, causing high junction temperatures which reduce the time the clocks can be off.

SUMMARY

Dynamic shift registers can be operated at very low clock rates if manufacturers data sheets are consulted and the proper clock phasing is used. Added margin can be designed into systems by keeping clock amplitudes high, the clock pulsewidths 10 to 20% wider than specified minimums, power supplies low and temperatures as low as possible. Beware of circuit board hot spots which increase the temperature of individual packages, or extensive interlead coupling or ringing which could result in positive clock spikes.

AMERICAN AND EUROPEAN FONTS IN STANDARD CHARACTER GENERATORS

Ten popular American and European 64-character subsets for displays and printers are now available from National as single-chip, standard character generators. These parts, listed in Table 1, are sold off-the-shelf without a ROM masking charge.

The ROMs are static, bipolar-compatible types, operating without clocks on standard power supplies. Row and column access times are typically 450 and 700 ns respectively. An MM4240/MM5240 2560-bit ROM is used for the 5 x 7 horizontal-scan fonts and an MM4241/MM5241 3072-bit ROM for the 7 x 5 vertical-scan fonts. The MM4240 and MM4241 operate at −55°C to +125°C and the MM5240 and MM5241 at −25°C to +70°C.

Input-output configurations and character formats for the ROMs are shown in Figures 1 and 2. Application Note *AN-40 The Systems Approach to Character Generators* gives examples of line and column address-control logic, and CRT and printer operating techniques.

TYPE NUMBER	CODE	64-CHARACTER SUBSET	FIGURE
Horizontal Scan (5 x 7)			
MM4240AA/MM5240AA	ASCII	Upper-case alphanumeric	3
MM4240AE/MM5240AE	ASCII	Lower-case alpha and symbols	4
MM4240ABU/MM5240ABU	Hollerith	Upper-case alphanumeric	5
MM4240ABZ/MM5240ABZ	EBCDIC-8	Upper-case alphanumeric	6
MM4240ACA/MM5240ACA	EBCDIC	Upper-case alphanumeric (IBM)	7
Vertical Scan (7 x 5)			
MM4241ABL/MM5241ABL	ASCII	Upper-case alphanumeric	8
MM4241ABV/MM5241ABV	ECMA	Upper-case A/N, Scandinavian	9
MM4241ABW/MM5241ABW	ECMA	Upper-case A/N, German	10
MM4241ABX/MM5241ABX	ECMA	Upper-case A/N, general European (French, British, Italian)	11
MM4241ABY/MM5241ABY	ECMA	Upper-case A/N, Spanish	12

TABLE 1. Single-Chip, Standard Horizontal-Scan and Vertical-Scan Character Generators

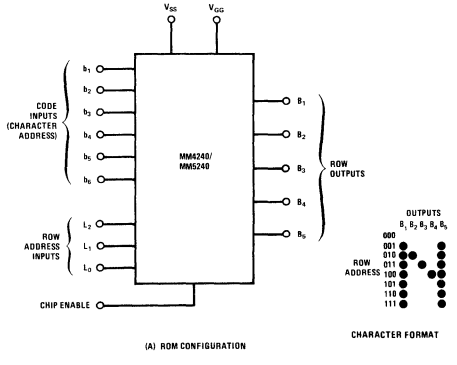

FIGURE 1. Horizontal-Scan Character Generator ROM

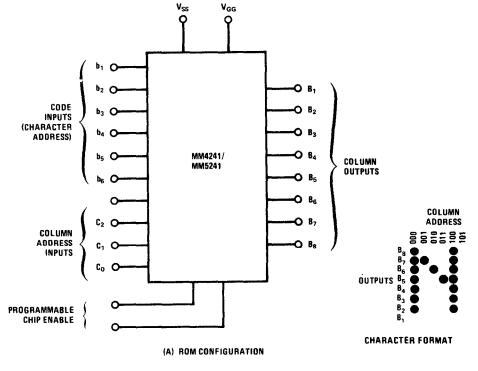

FIGURE 2. Vertical-Scan Character Generator ROM

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Note that each ROM has a chip-enable input to permit multi-ROM operation with common control logic. For instance, two horizontal-scan ASCII character generators may be operated in tandem to obtain upper and lower-case characters. In this case, chip-enable would be controlled with bit b_6 of the normal 7-bit ASCII code, and its complement, $\overline{b_6}$.

HORIZONTAL SCAN FONTS

The subsets of 64 5 x 7 characters in the horizontal-scan fonts are the ones most commonly used in low-cost TV and CRT raster-scan displays and dot-matrix line printers.

MM4240AA/MM5240AA contains the ASCII-6 preferred graphic subset, formed from ASCII-7 by ignoring bit b_6. The remaining six bits form two octal address characters. One is formed by the three more significant bits, b_7, b_5 and b_4, and the second by b_3, b_2 and b_1.

Also, characters 36 and 37 in ASCII (x3.4 1968)* are respectively a carat (or circumflex), and an underscore. These are awkward in a video display, so they are replaced by the more useful arrows. (The arrows are related to characters in an older teletypewriter set.) This font, shown in Figure 3, is also described on the MM4240/MM5240 data sheet (which should be referred to for operating characteristics of all the horizontal-scan character generators).

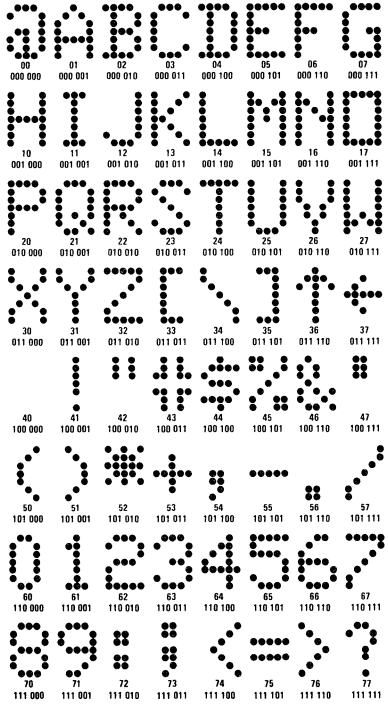

FIGURE 3. MM4240AA/MM5240AA Horizontal-Scan ASCII-7 Graphic Subset

MM4240AE/MM5240AE generates unique symbols describing the ASCII-7 control codes, as well as lower-case letters (Figure 4). The designer may not wish to display or dot-print the symbols. Since the symbols are generated only when the most significant address bit is logic "0", this bit line may be used to disable the chip, and blank the screen when control signals are transmitted. If not, the system designer can use the symbols as he likes.

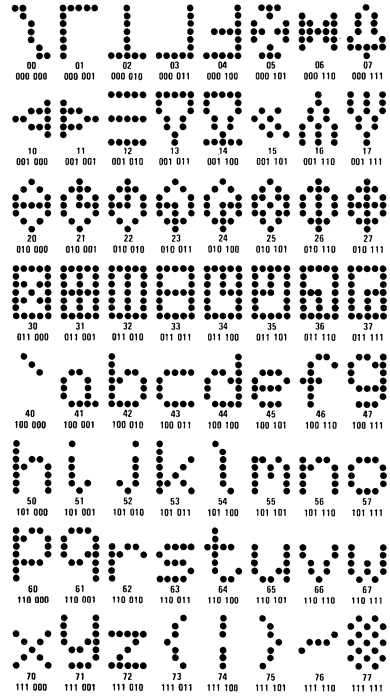

FIGURE 4. MM4240AE/MM5240AE Horizontal-Scan ASCII-7 Lower-Case Graphic and Control Symbol Subset

The Hollerith character subset in Figure 5b is formed by using six gates to compress the 12-line Hollerith code to the 6-bit address for 64 characters, as shown in Figure 5a

As shown in Figure 6, an ASCII-compatible subset is provided by the EBCDIC-8 character generator (MM4240ABZ/MM5240ABZ) by simply ignoring the two most significant bits, b_0 and b_1, in the EBCDIC-8 code. The ABZ version follows the ANSI standard, while the ACA version follows the IBM style. A cent sign, and IBM's logical OR and logic NOT signs are given by the ACA subset (characters 12, 17, and 37). And a plus or minus sign is provided, as character 52. (See Figure 7.)

*American National Standards Institute (ANSI)

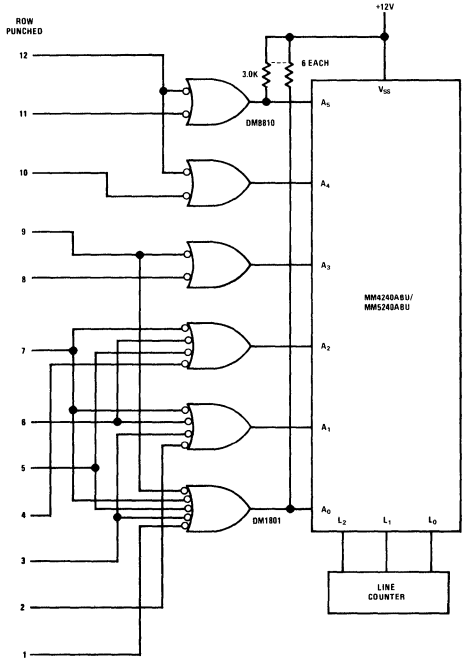

FIGURE 5a. MM4240ABU/MM5240ABU Typical Address Inputs

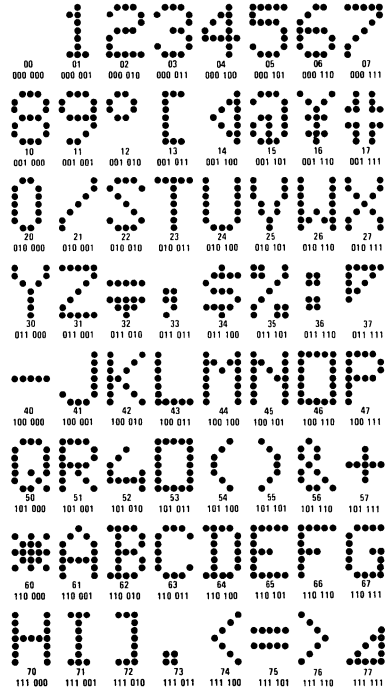

FIGURE 5b. MM4240ABU/MM5240ABU Horizontal Scan Hollerith Graphics Subset

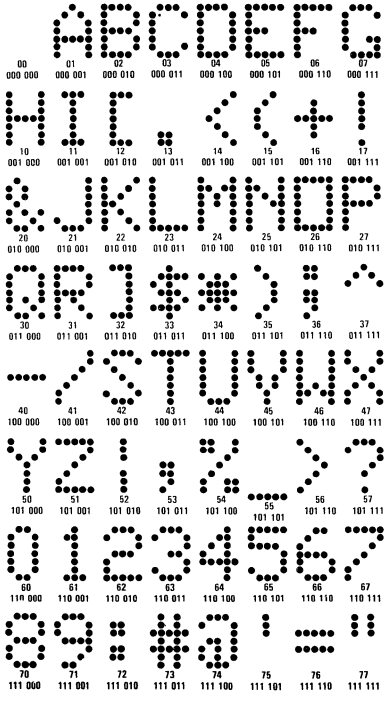

FIGURE 6. MM4240BABZ/MM5240BABZ Horizontal-Scan EBCDIC-8 Graphic Subset

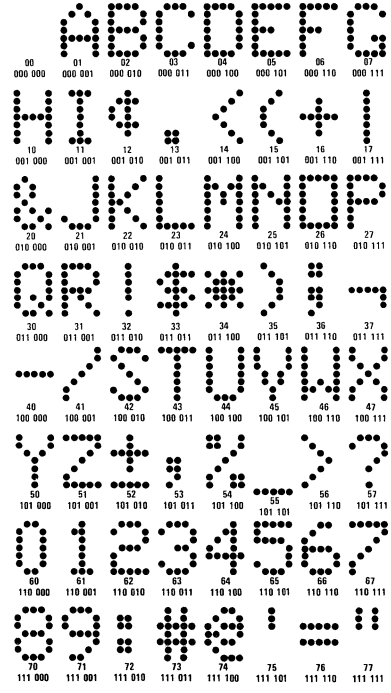

FIGURE 7. MM4240ACA/MM5240ACA Horizontal-Scan IBM EBCDIC Graphic Subset

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VERTICAL SCAN FONTS

All five of the standard vertical-scan subsets in Figures 8 through 12 are generated with 6-bit codes derived from code recommendations R646 of the International Organization for Standardization. These recommendations cover ASCII-7, European ECMA-7 and CCITT alphabet number 5.

The ASCII subset for American use, in Figure 8, is practically identical to the horizontal-scan subset. Those in Figures 9 through 12 follow preferred character styles in the countries indicated. The underscore (character 37) is dropped below the line so that it may be used as a cursor.

Vertical-scan character generators are generally used in dot-matrix tape printers, ink-dot spray printers and high-definition sawtooth or pedestal-scan CRT displays. They may also be used to control raster-scan TV tubes or CRTs if the tube is turned on its side so that the raster scan is made vertically to provide a page-like format.

With standard programming, the bits in the column outputs are sequenced for a sawtooth scan with dot columns running in the same direction, as illustrated in Figure 13a. For a pedestal scan, Figure 13b, alternate columns can be reversed by putting an 8-bit shift left/shift right TTL shift register (DM74198) on the output as illustrated in Figure 14.

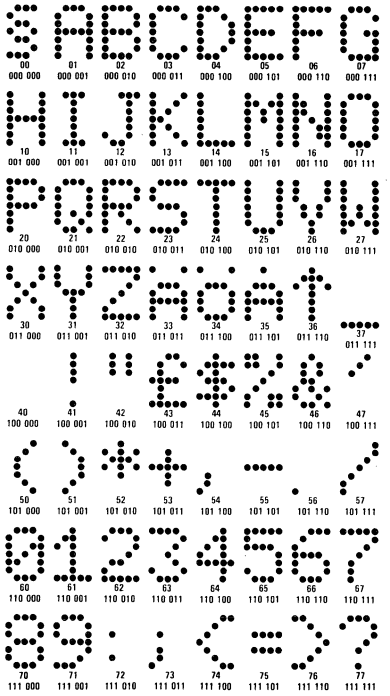


FIGURE 9. MM4241ABV/MM5241ABV Vertical Scan ECMA-7 Font for Scandinavian Use

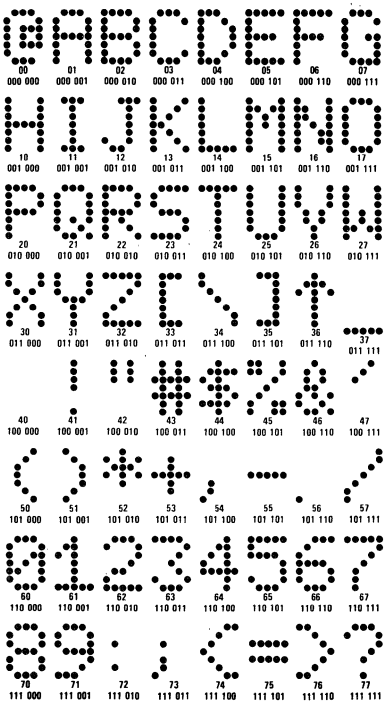


FIGURE 8. MM4241ABL/MM5241ABL Vertical-Scan ASCII-7 Graphic Subset

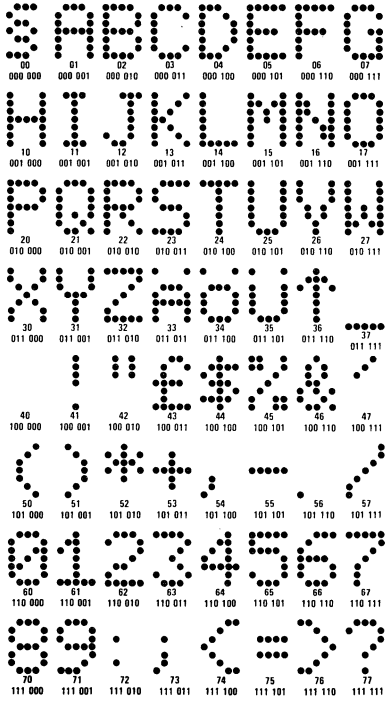


FIGURE 10. MM4241ABW/MM5241ABW Vertical-Scan ECMA-7 Font for German Use

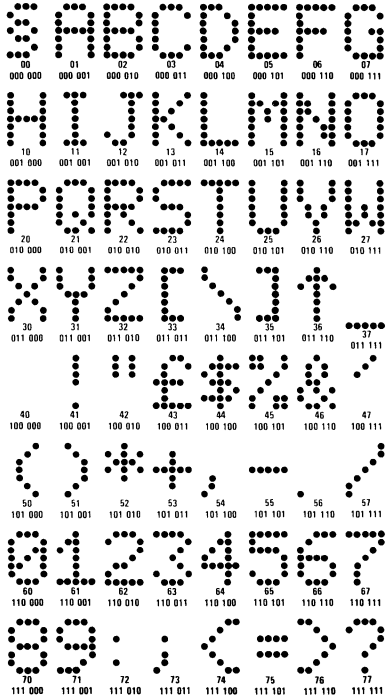


FIGURE 11. MM4241ABX/MM5241ABX Vertical-Scan ECMA-7 Font for General European Use (French, British, Italian)

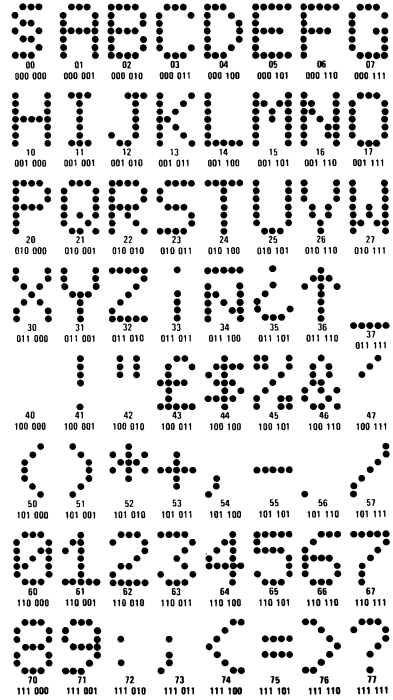


FIGURE 12. MM4241ABY/MM5241ABY Vertical-Scan ECMA-7 Font for Spanish Use

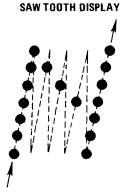


FIGURE 13a. Sawtooth Vertical Scan

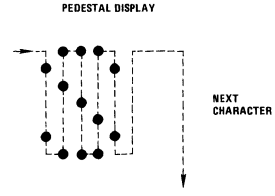


FIGURE 13b. Pedestal Vertical Scan

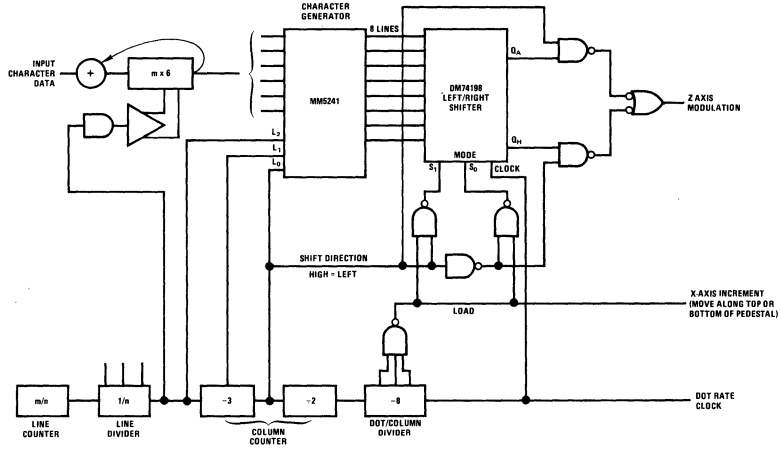


FIGURE 14. Conversion of Sawtooth Output to Pedestal Scan

CUSTOM FONTS

The two ROMs can also be custom-programmed to provide special characters, or fonts larger than 5 x 7. The MM4240/MM5240 actually stores 64 5 x 8 characters or character segments and the MM4241/MM5241 stores 64 8 x 6 characters or segments. They are not limited to 5 x 7 and 7 x 5.

For example, the extra height may be used in an otherwise 5 x 7 font to drop the tails of commas, semicolons and lower-case letters below the bottom line of the capital letters. Fonts as large as 16 x 12 are entirely practical without additional control logic, using the chip-enable feature of four MM5241s. Large-font organizations are discussed in AN-40.

APPLYING MODERN CLOCK DRIVERS TO MOS MEMORIES

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input wave forms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAM's (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, two new monolithic integrated circuit drivers, the MH0025 and MH0026 are selected as examples because of their low cost.

The MH0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage-gold doped process utilizing a collector sinker to minimize $V_{CE\,SAT}$.

The MH0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Of course each of us is careful of details but reminders such as "turn on the power supplies" or "don't reverse supply polarity" sometimes solve a not-so-obvious problem. This section is intended to review and answer design questions like "how much should I decouple supplies?"

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking

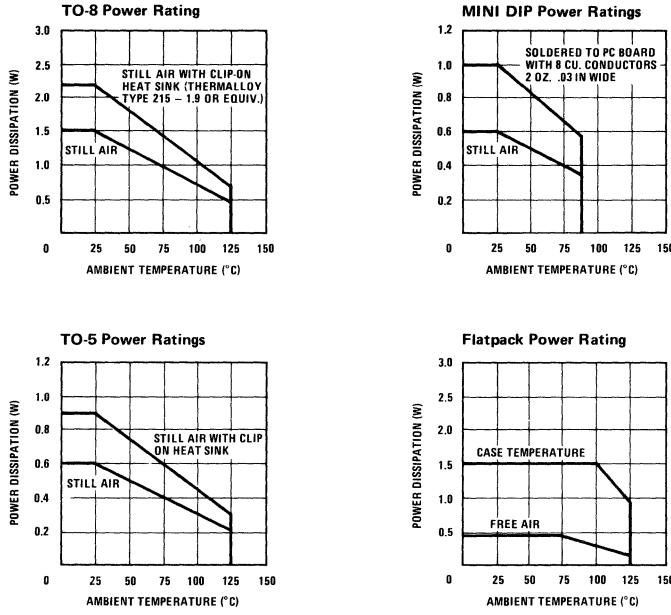
TABLE I. MH0025 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0.0022μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0.0001μF, R_O = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	$I_{IN} \triangleq$ 10mA, I_{OUT} = 1mA	$V^- + 1.0$	V
On Supply Current (V^+)	I_{IN} = 10mA	17	mA

TABLE II. MH0026 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		7.5	ns
t_{OFF}	C_{IN} = 0.001μF, R_{IN} = 0Ω	7.5	ns
t_r	R_0 = 50Ω, C_L = 1000pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = -1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 0.5$	V
On Supply Current (V^+)	I_{IN} = 10mA	28	mA

TABLE III. Package Power Ratings



required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

The TO-5 ("H") package is rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 900mW with clip on heat sink (derate at 6.0mW/°C above 25°C). This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on-heat sink increases driving capability by 50%.

The 8 pin ("N") molded mini-DIP is rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 1.0W soldered to P.C. board (derate at 6.6mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600mW when mounted in a socket and not one watt until it is soldered down.)

The TO-8 ("G") package is rated at 1.5W still air (derate at 10mW/°C above 25°C) and 2.3W with with clip on heat sink (Wakefield type 215-1.9 or equivalent-derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

The 14 pin cavity DIP is rated at 600mW free air. While some rate this package at 1W *case* temperature, National does not recommend its use for clock drivers. This is because from a user point of view, it is impossible to get more than 400 to 500mW rating under normal system conditions; i.e., there is no practical way to conduct heat away from the device other than air.

Other package types range in size and power handling capability. Most have the disadvantage of being in non-standard sizes and are difficult to mount in a system.

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

- Package and heat sink selection
- Average DC power, P_{DC}
- Average AC power, P_{AC}
- Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of DC power and AC power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \qquad (1)$$

Average DC power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \quad (2)$$

For most types of clock drivers, the first two terms are neglible (less than 10mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

Req = Equivalent device resistance in the "ON" state

$= V^+ - V^-/I_{S(ON)} \quad (3)$

DC = Duty Cycle

$= \frac{\text{"ON" Time}}{\text{"ON" Time + "OFF" Time}}$

For the MH0025, Req is typically 1kΩ while Req is typically 600Ω for the MH0026. Graphical solutions for P_{DC} appear in Figure 1. For example if $V^+ = +5V$, $V^- = -12V$, Req = 500Ω, and DC = 25%, then P_{DC} = 145mW. However, if the duty cycle was only 5%, P_{DC} = 29mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

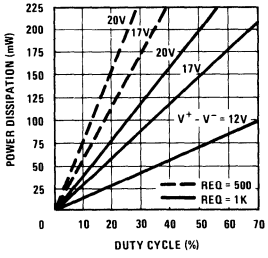


FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \quad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in Figure 2. Thus, any type of clock driver will dissipate internally 290mW per MHz per thousand pF of load. At 5MHz, this would be 1.5W for a 1000pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

Combining equations (1), (2), (3), and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

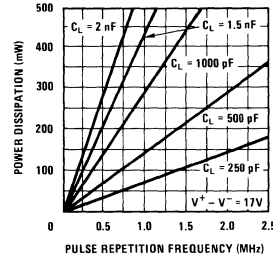


FIGURE 2. P_{AC} vs PRF

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \quad (5)$$

As an example, the MH0025CN can dissipate 630mW at $T_A = 70°C$ when soldered to a printed circuit board. Req is approximately equal to 1k. For $V^+ = 5V$, $V^- = -12V$, f = 1MHz, and DC = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(630 \times 10^{-3})}{(2)(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$$C_L \leq 880pF \text{ (each driver)}$$

A typical application might involve driving an MM5013 triple 64-bit shift register with the MH0025. Using the conditions above and the clock line capacitance of the MM5013 of 60pF, a single MH0025 can drive 880pF/60pF, or 14 MM5013's.

Similarly, the MH0026CG can dissipate 1.0W at 75°C. For $V^+ = 5V$, $V^- = -12V$, f = 2MHz, and DC = 20%, the maximum load capacitance which may be driven is:

$$C_L \leq 2 \times \frac{1}{10^6}\left[\frac{(1.0)}{(2)(17)^2} - \frac{0.2}{600}\right]$$

$$C_L \leq 700pF \text{ (each driver)}$$

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TABLE IV. Worst Case Maximum Drive Capability for MH0026*

PACKAGE TYPE		TO-8 WITH HEAT SINK		TO-8 FREE AIR		MINI-DIP SOLDERED DOWN		TO-5 AND MINI-DIP FREE AIR	
Max. Operating Frequency	Max. Ambient Temp. → / Duty Cycle ↓	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C
100kHz	5%	30 k	24 k	19 k	15 k	13 k	10k	7.5k	5.8k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2.7k	2k	1.5k	1.1k
1MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	430
2MHz	25%	1.4k	1.1k	850	650	550	400	280	190
5MHz	25%	620	470	380	290	240	170	120	80
10MHz	25%	280	220	170	130	110	79	–	–

*Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$. For loads greater than 1200 pF, rise and fall times will be limited by output current.

Returning to the MM5013 example, a single MH0026 can drive 700pF/60pF, or 11 5013's. Using the above equations, Table IV has been calculated for quick reference. In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, AC power (which depends on frequency, voltage across the device, and capacitive load) and DC power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (c) peak transient current available. Details of these are included in Appendixes I and II. Figures AI-3, AI-4, AII-2, and AIII-3 illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver, and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ peak}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this app. note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vise versa for fall times. Since MOS logic is inverted from normal TTL, "risetime" as used in this note is "voltage fall" and "fall time" is "voltage rise."

Power Supply Decoupling

Although power supply decoupling is a wide spread and accepted practice, the question often arises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in Figure 3. In this instance, a small damping resistor is inserted

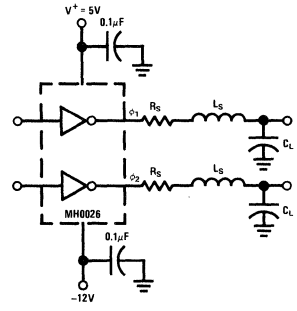

FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r\,(max)} = t_{f\,(max)} \leq 2.2\ R_S\ C_L \qquad (7)$$

One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2 f C_L$ and accordingly the resistor wattage rating will generally be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. Figure 4

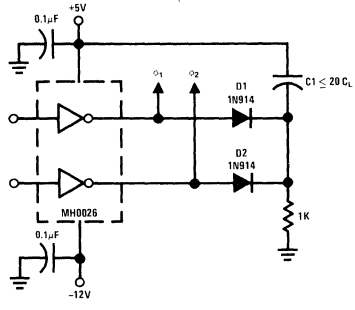

FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice versa) during the transition of ϕ_1 to MOS logic "1." The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Figure 5 illustrates the problem.

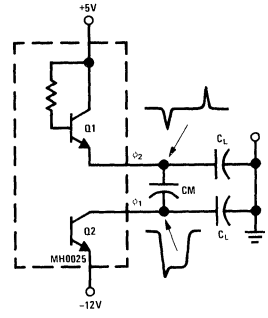

FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q_1 is "OFF" since only μA are drawn from the device. A simple method of minimizing cross-talk is shown in Figure 6.

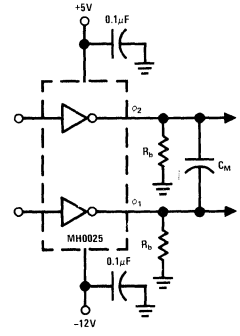

FIGURE 6. Use of Bleed Resistors to Minimize Clock-Line Crosstalk

Bleed resistors are connected between the clock driver and ground causing a current of a few mA to flow. The output impedance of the clock driver is reduced and the negative spike is thus minimized. Values for R_b depend on layout and the number of registers being driven. Typical values are between 1k and 10kΩ.

A major point should be emphasized with regard to clock-line crosstalk, i.e., even if the output impedance of the driver is zero ohms, self inductance between the clock driver and registers will cause the clock lines to spike on the transitions. Hence, the technique shown in Figure 6 works reasonably well for small systems.

For large systems, the circuit of Figure 7 is recommended. In this instance, Q_1 and Q_2 are turned "ON" just prior to the clocks transition to logic "1." The spike is therefore clamped by the $V_{CE\ (sat)}$ of Q_1 and Q_2. A key feature of the circuit is that the clamps are physically placed adjacent the register thus minimizing the inductance between the clamp and the load.

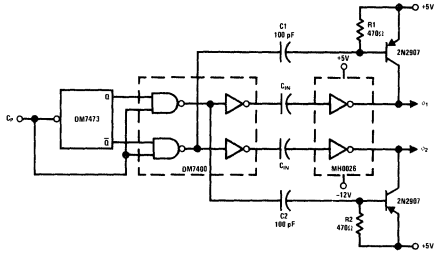

FIGURE 7. Cross Talk Minimization Circuit

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to DC level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the MH0025 and MH0026 utilize input capacitors when level shifting from TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of both the MH0025 and MH0026.

CONCLUSION

The practical aspects of driving MOS memories with new low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the MH0025 and MH0026 provide superior performance for most MOS input interface applications.

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3. Dale Mrazek, *"MOS Delay Lines,"* National Semiconductor, AN-25, April 1969.

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6. Richard Percival, *"Dynamic MOS Shift Registers can also simulate Stack and Silo Memories,"* Electronics Magazine, Nov. 8, 1971.

7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, Aug. 1971.

8. Don Femling, *"Using the MM5704 Keyboard Interface in Keyboard Systems,"* National Semiconductor, AN-52.

APPENDIX I

MH0025 Circuit Operation

The schematic diagram of the MH0025 is shown in Figure AI-1. With the TTL driver in the logic "0" state Q_1 is "OFF" and Q_2 is "ON" and the output is at approximately one V_{BE} below the V^+ supply.

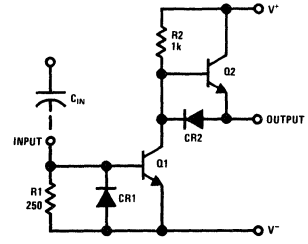


FIGURE AI-1. MH0026 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q_1, through C_{IN}, turning it "ON." As the collector of Q_1 goes negative, Q_2 turns OFF. Diode CR_2 assures turn-on of Q_1 prior to Q_2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q_2's base emitter junction.

The negative voltage transition (to MOS logic "1") will be quite linear since the capacitive load will force Q_1 into its linear region until the load is discharged and Q_1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q_1 turns "OFF" and Q_2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the MH0025 is primarily a function of the AC load, C_L, the available input current and total voltage swing. As shown in Figure AI-2, the input current must

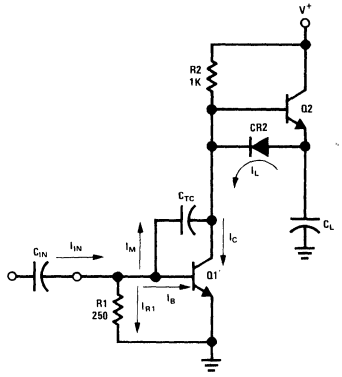


FIGURE AI-2. Rise Time Model for the MH0025

charge the Miller capacitance of Q_1, C_{TC}, as well as supply sufficient base drive to Q_1 to discharge C_L rapidly. By inspection:

$$I_{IN} = I_M + I_B + I_{R1} \qquad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M >> I_{R1} \text{ \& } I_B >> I_{R1}$$

$$I_B = I_{IN} - C_{TC}\frac{\Delta V}{\Delta t} \qquad \text{(AI-2)}$$

If the current through R_2 is ignored,

$$I_C = I_B h_{FEQ1} = I_L + I_M \qquad \text{(AI-3)}$$

where:

$$I_L = C_L \frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, AI-3 yields:

$$\frac{\Delta V}{\Delta t}[C_L + C_{TC}(h_{FEQ1}+1)] = h_{FEQ1} I_{IN} \qquad \text{(AI-4)}$$

or

$$t_r \cong \frac{[C_L + (h_{FEQ1}+1)C_{TC}]\,\Delta V}{h_{FEQ1} I_{IN}} \qquad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a MH0025 loaded with 1000 pF, rise times of:

$$\frac{(1000\text{pF} + 250\text{pF})\ (17\text{V})}{(50\text{mA})\ (20)}$$

or 21ns may be expected for V^+=5.0V, V^-=-12V. Figure AI-3 gives rise time for various values of C_L.

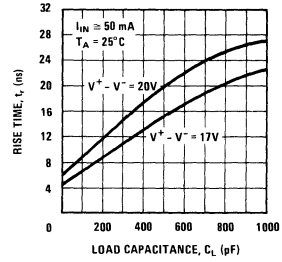


FIGURE AI-3. Rise Time vs C_L for the MH0025

Fall Time Considerations

The MOS logic fall time (voltage rise) of the MH0025 is dictated by the load, C_L, and the output capacitance of Q_1. The fall time equivalent circuit of MH0025 may be approximated with the circuit of Figure AI-4. In actual practice, the base

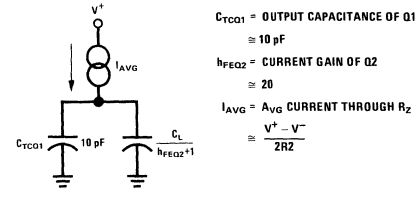


FIGURE AI-4. Fall Time Equivalent Circuit

drive to Q_2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic

values at the end. Figure AI-5 shows t_f as function of C_L.

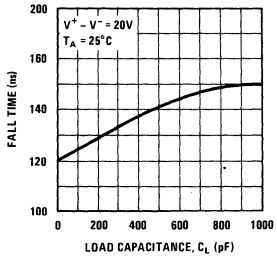


FIGURE AI-5. MH0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R_2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \qquad \text{(AI-6)}$$

or

$$t_f \cong 2R_2 \left(C_{TCQ1} + \frac{C_L}{h_{FEQ1+1}}\right) \qquad \text{(AI-7)}$$

MH0025 Input Drive Requirements

Since the MH0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50 to 60 mA region. It is therefore a good idea to drive the MH0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the MH0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The MH0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output

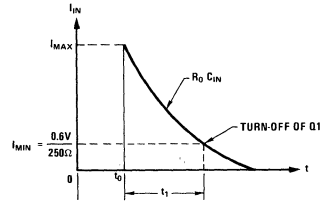


FIGURE AI-6. MH0025 Input Current Waveform

pulse width. In the latter mode a long pulse is supplied to the MH0025. The input current is of the general shape as shown in Figure AI-6. I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50 to 60 mA). Q_1 will begin to turn-off when I_{IN} decays below V_{BE}/R_1 or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R_0 C_{IN}} \qquad \text{(AI-8)}$$

Where:

R_0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \frac{V_{BE}}{R_1}$ and solving for t_1 yields:

$$t_1 = R_0 C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R_0 C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-10)}$$

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200pF is:

$$t_{PW} \cong \frac{25ns + 150ns}{2} + (65\Omega)(2{,}200pF) \ln \frac{50mA}{2.5mA} = 517ns$$

A plot of pulse width for various types of drivers is shown in Figure AI-7. For applications in which

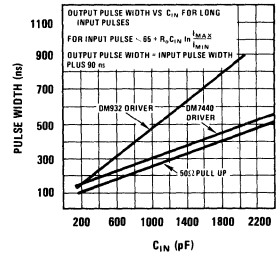


FIGURE AI-7. Output PW Controlled by C_{IN}

the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

The MH0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and plus 20V. The MH0025 is shown in Figure AI-8 driving the address or pre-charge line in the logically controlled mode.

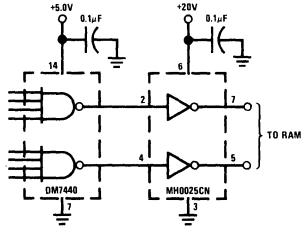


FIGURE AI-8. DC Coupled MH0025 Driving 1103 RAM.

If DC operation to a negative level is desired, a level translator such as the DM7800 or DH0034 may be employed as shown in Figure AI-9. Finally, the level shift may be accomplished using PNP transistors are shown in Figure AI-10.

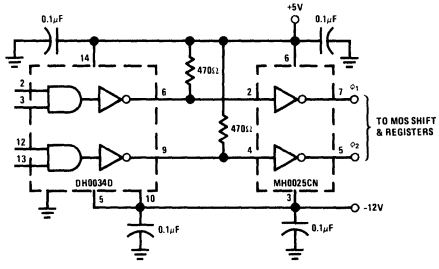


FIGURE AI-9. DC Coupled Clock Driver Using DH0034.

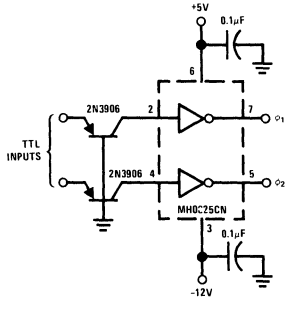


FIGURE AI-10. Transistor Coupled MH0025 Clock Driver.

APPENDIX II

MH0026 Circuit Operation

The schematic of the MH0026 is shown in Figure AII-1. The device is typically AC coupled on the input and responds to input current as does the MH0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q_1, Q_2, Q_5, Q_6, and Q_7 are "OFF" allowing Q_3 and Q_4 to come "ON." R_6 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q_1 and Q_2 turning them "ON." Simultaneously, Q_3 and Q_4 are snapped "OFF." As the input voltage rises (to about 1.2V), Q_5 and Q_6 turn-on. Multiple emitter transistor Q_5 provides additional base drive to Q_1 and Q_2 assuring their complete and rapid turn-on. Since Q_3 and Q_4 were rapidly turned OFF minimal power supply current spiking will occur when Q_7 comes "ON."

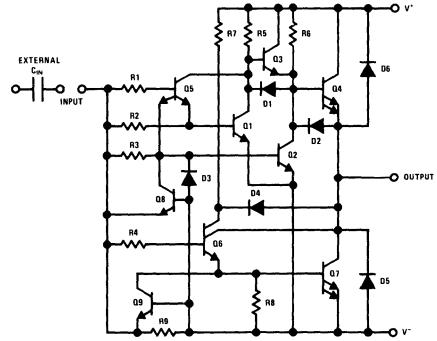


FIGURE AII-1. MH0025 Schematic (One-Half Circuit)

Q_6 now provides sufficient base drive to Q_7 to turn it "ON." The load capacitance is then rapidly discharged toward V^-. Diode D_4 affords a low impedance path to Q_6's collector which provides additional drive to the load through current gain of Q_7. Diodes D_1 and D_2 prevent avalanching Q_3's and Q_4's base-emitter junction as the collectors of Q_1 and Q_2 go negative. The output of the MH0026 continues negative stopping about 0.5V more positive than V^-.

When the TTL input returns to logic "0," the input voltage to the MH0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q_8 and Q_9 turn-on, pulling stored base charge out of Q_7 and Q_2 assuring their rapid turn-off. With Q_1, Q_2, Q_6 and Q_7 off, Darlington connected Q_3 and Q_4 turn-on and rapidly charge the load to within a V_{BE} of V^+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the MH0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\ \Delta V \qquad \text{(AII-1)}$$

For C_L = 1000pF, V^+ = 5.0V, V^- = -12V, $t_r \cong$ 21ns. Figure AII-2 shows MH0026 rise times vs. C_L.

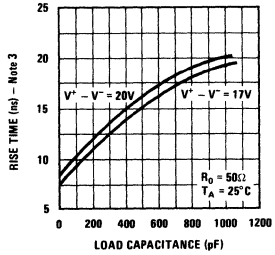


FIGURE AII-2. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the MH0026 is determined primarily by the capacitance Miller capacitance of Q_5 and Q_1 and R_5. The fall time may be predicted by:

$$t_f \cong (2.2)(R_5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q_3
= 2pF

$h_{FE}{}^2 = (h_{FEQ3}+1)(h_{FEQ4}+1)$
$\cong$ 500

For the values given and C_L = 1000pF, $t_f \cong$ 17.5ns. Figure AII-3 gives t_f for various values of C_L.

MH0026 Input Drive Requirements

The MH0026 was designed to be driven by standard 54/74 elements. The device's input characteristics

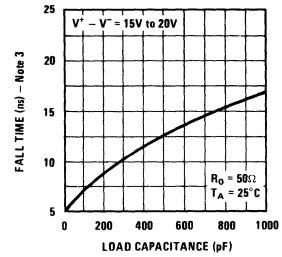


FIGURE AII-3. Fall Time vs Load Capacitance

are shown in Figure AII-4. There is breakpoint at $V_{IN} \cong$ 0.6V which corresponds to turn-on of Q_1 and Q_2. The input current then rises with a slope of about 600Ω ($R_2 \parallel R_3$) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q_5 and Q_6. The slope at this point is about 150Ω ($R_1 \parallel R_2 \parallel R_3 \parallel R_4$).

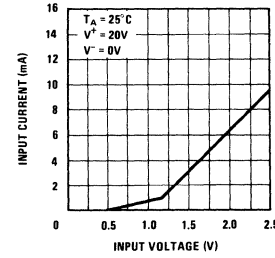


FIGURE AII-4. Input Current vs Input Voltage

The current demanded by the input is in the 5 to 10mA region. A standard 54/74 gate can source currents in excess of 20mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a MH0026. As far as the MH0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the MH0025 and MH0026 is that the MH0026 requires that the output pulse width be logically controlled. In short, the input pulse width $\cong$ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the MH0026 "ON." As before:

$$t_1 = R_0 C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AII-3)}$$

or

$$C_{IN} = \frac{t_1}{R_0 \ln \frac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

In this case R_0 equals the sum of the TTL gate output impedance plus the input impedance of the MH0026 (about 150Ω). I_{MIN} from Figure AII-5 is about 1mA. A standard 54/74 series gate has an high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20mA into 1.2V. For an output pulse width of 500ns,

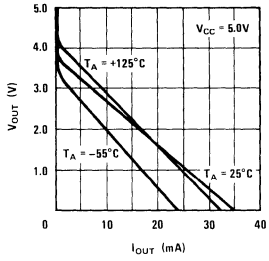


FIGURE AII-5. Logical "1" Output Voltage vs Source Current

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega)\ln \frac{20mA}{1mA}} = 560pF$$

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, MH0026, and temperature variations.

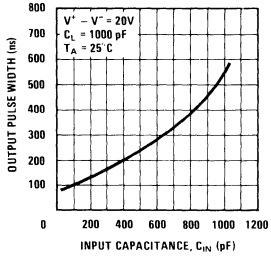


FIGURE AII-6. Optimum Input Capacitance vs Output Pulse Width

A plot of optimum value for C_{IN} vs desired output pulse width is shown in Figure AII-6.

DC Coupled Applications

The MH0026 may be applied in direct coupled applications. Figure AII-7 shows the device driving address or pre-charge lines on an MM1103 RAM.

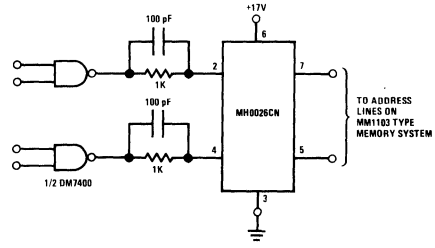


FIGURE AII-7. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a DC level shift, the circuit of Figure AII-8 or AII-9 are recommended.

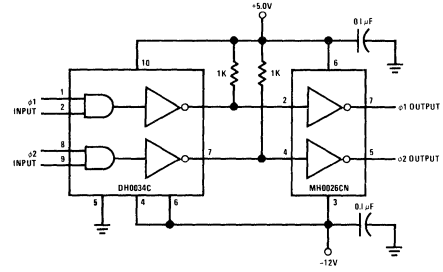


FIGURE AII-8. Transistor Coupled MOS Clock Driver

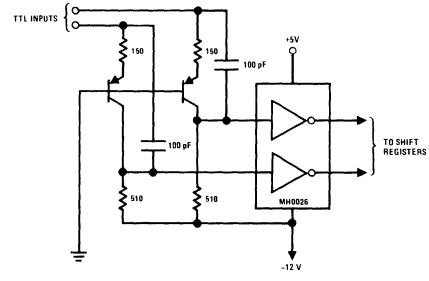


FIGURE AII-9. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007 Direct coupled, single phase, TTL compatible clock driver.

MH0009 Two phase, direct or AC coupled clock driver.

MH0012 10MHz, single phase direct coupled clock driver.

MH0013 Two phase, AC coupled clock driver.

MH0025 Low cost, two phase clock driver.

MH0026 Low cost, two phase, high speed clock driver.

MH8808 Dual clock driver for MM5262 2k RAM.

MOS Oscillator/Clock Drivers

MH7803/MH7807 – Complete two phase clock system for MOS micro-processors and calculators.

MOS RAM Memory Address and Precharge Drivers

MH8804 Quad TTL to 1103 address driver.

MH8805 Dual TTL to 1103 address driver.

MH0025 Dual address and precharge driver.

MH0026 Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034 Dual high speed TTL to negative level converter.

DM7800 Dual TTL to negative level converter.

DM7810/DM7812/DM7819 – Open collector TTL to positive high level MOS converter gates.

DM78L12 Active pull-up TTL to positive high level MOS converter gates.

MOS to TTL Level Converters and Sense Amps

DM7802/DM7806* – Dual sense amp for MM5262 2k MOS RAM memory.

LM165 Series* – Hex sense amp MOS to TTL.

LM163/LM75107/LM75207* – Dual sense amp for MM1103 1k MOS RAM memory.

Voltage Regulators for MOS Systems

LM109/LM140 Series – Positive regulators.

LM120 Series – Negative regulators.

LM125 Series* – Dual +/– regulators.

*To be announced.

MOS KEYBOARD ENCODING

INTRODUCTION

The use of MOS large scale integration has made it possible to provide, in a single integrated circuit, all of the components necessary for economic implementation of the keyboard encoding function. The MM5740 is a complete keyboard interface system capable of providing quad mode 90 key keyboard encoding. In addition to the basic problem of translating a switch closure to a coded output, the MM5740 provides all of the functions necessary for modern keyboard system design. The salient features include programmable N-key or 2-key rollover, TRI-STATE® parallel data outputs with a one character memory and externally controllable pulse or level data strobe modes. Added conveniences are on-chip clock generation from a single TTL input, external RC control of strobe pulse width and capacitor control of key bounce mask time, single pin shift lock/shift indicator capability and repeat key function.

THEORY OF OPERATION

In order to better understand the following discussion, reference should be made to Figure 1 which shows a functional block diagram of the MM5740 as well as the pin connection diagram.

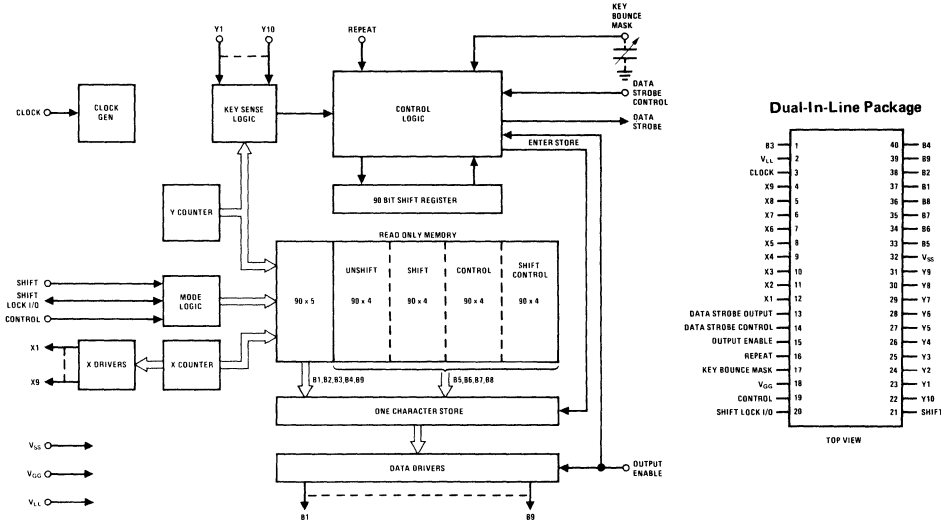


FIGURE 1. Block and Connection Diagrams

A dynamic scanning technique is utilized to detect and pinpoint keyswitch activity on the keyboard. In this method, two ring counters are employed. A 9-bit X counter monitors the rows of the switch matrix while the columns are monitored by a 10-bit Y counter. Since there are 9 x 10 = 90 possible counter states, ninety data switches may be defined by their X-Y coordinates.

Every scan time (90-bit times), all keys are interrogated in turn to determine their status. Each particular key is interrogated every 90-bits or once each keyboard scan cycle. This is implemented by employing the X counter as drivers to drive each row of the switch matrix in turn. The Y counter enables the sensing of each column of the switch matrix. Therefore, if a switch is closed it will be detected when its row (X coordinate) is driven and its column (Y coordinate) is sensed. This corresponds to the particular X-Y time (one of 90 time slots in the scan) defining the closed switch. A key detect pulse at the X-Y time in question is issued and this is used to define the status of that particular key.

The above discussion has shown us how to detect a key closure and pinpoint which key switch it was. We must now take this information and provide a coded bit pattern for that key. In addition to scanning the key switch matrix, the X and Y counters are used to scan the contents of a Read Only Memory which contains the bit pattern for each key switch. For example, when switch X_1, Y_1 is being interrogated (at X_1-Y_1 time), the counters are addressing the memory location in the ROM which contains the code for switch X_1Y_1. If the key is closed, a key detect pulse will be issued. At this time, the ROM contents are strobed into latches which then hold the code pattern for key X_1, Y_1. It should be noted that the scanning of the switch matrix and ROM occur simultaneously and repetitively. The clocks are never stopped, instead information is obtained dynamically.

For each keyswitch it is possible to have four modes. These are determined by the status of the SHIFT and CONTROL keys which are inputs to the MM5740. There are four possible code patterns for each key as determined by the mode switches. These code patterns are related in that, for any key, in any of its modes, only four of its 9-bits may vary. All code patterns are programmed at the time of manufacture using a single mask variation.

Rollover

The MM5740 keyboard encoder chip is capable of either N-key or 2-key rollover. The customers' preference is programmed on the same mask used to define the code pattern for the keyswitches. N-key rollover is defined as the ability to issue a code each time a new key is depressed regardless of the status of all other keys. This means that each time a new key is depressed, a code for that key would be issued even if other keys are still depressed. This type of rollover is ideal for fast typing applications, since the typist does not have to train herself to release the currently depressed key before she depresses a new one. Even in slower typing applications, burst typing of typical trigrams such as "THE" and "ERE" can be a problem if N-key rollover is not employed.

In 2-key rollover, a code is issued at the time of depressing a new key, provided all other keys are released. If a key is depressed a code will be issued and the keyboard will be ignored until that switch has been released. If two depressions are performed in turn the first will be recognized and the second code will be issued when the first key is released.

N-key rollover is accomplished by remembering the status of each key on the previous scan cycle. This is achieved by using a 90-bit shift register whose input is the key detect signal. If the input and output of the shift register are monitored, it is possible to compare the status of each key on the past scan (output of shift register) with its status on the current scan (input of shift register). A valid key closure is present only if the input of the shift register is true and its output false. A release is present when the input is false and the output is true. The other two cases (00 and 11) correspond to no change in status; either released or depressed. The ROM word is strobed into the output latches only when a valid key closure is detected.

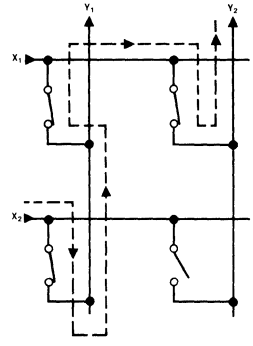
Once a previously closed key is released it then becomes possible to accept it as a valid closure if it is depressed again. For 2-key rollover, the same criterion is used to determine a valid key closure. However, after a key has been depressed no further entries will be acted upon until that key has been released. It should be also noted that the depression of the SHIFT and/or CONTROL keys after the depression of a data key will be ignored. The mode control keys must be depressed before depressing the data keys.

Masking the Bounce

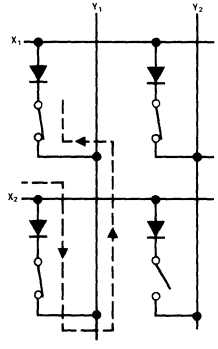
Most keyswitches, primarily mechanical or reed, will exhibit a bounce characteristic upon both depression and release. In normal operation, many keyboard scans could occur during the time of switch bounce. It is then necessary to make sure that this bounce is not recognized as multiple depressions and/or releases. As soon as the scanner detects a change in key status, an internal time delay is activated which instructs the encoder to ignore keyboard activity. At the end of the time out (usually several milliseconds), when switch bounce has subsided, the encoder resumes interrogating the switch matrix. The time delay is continuously variable with an external capacitance connected to pin 17 of the MM5740. Typical time delays are illustrated in Figure 1 of the data sheet. The continuously variable bounce masking allows the MM5740 to be used with a wide range of commercial key switches.

The Phantom Key

In keyboard system design, a frequent question arises about the use of diodes in the keyswitch matrix. The need for diodes in series with each keyswitch stems from the fact that, under certain conditions, an undepressed key will appear as one which is depressed. Consequently an undesired additional character will be transmitted. Since an open keyswitch was detected, this keyswitch is often termed the phantom key. In order to better understand this problem, reference should be made to Figure 2. In this diagram, phantom switch X_2Y_2 will be detected since there exists a closed path from the X_2 drive line to the Y_2 sense line which does not pass through the open switch X_2Y_2. By placing diodes in series with each keyswitch, this problem is eliminated since the sneak path has been blocked.



(a) NO DIODES



(b) DIODES BLOCK SNEAK PATH

FIGURE 2. Phantom Key Illustration

For a phantom key situation to occur it is necessary that at least 3 switches be closed and that they are located at the corners of some matrix rectangle. In addition, if a 2-key rollover encoder is used no diodes are required since the keyboard will be ignored if one key remains depressed.

For an N-key rollover keyboard, if it can be certain that no more than 2 keys will remain closed, no diodes are required. If this condition cannot be guaranteed it is possible, by clever key station layout, that when 3 keys are down they do not form the corners of a matrix rectangle. When none of the above restrictions can be met and true N-key rollover is required, it becomes necessary to insert diodes in series with the key switches. For uniformity it is recommended that a diode be used with each switch. However, diodes are not required along the diagonal coordinates of the switch matrix and may be omitted if desired. It should be noted that this discussion pertains to switches which form a contact between the matrix coordinate lines. These include physical contact types such as mechanical or reed. For solid state or capacitive switches where there is isolation between an X-Y coordinate, this problem may not apply.

Input-Output Interfacing

In order to better see how the MM5740 can be connected to external components, an understanding of its input/output capabilities is necessary. All functional control inputs as well as the Data output lines (B_1-B_9) and the Data Strobe output are directly TTL compatible. The functional control inputs are clock, output enable, repeat, shift and control. These input pins may be driven from a standard TTL logic gate which also drives 10 other TTL loads. Thus the worst case input levels are specified at +0.4 and +2.4V. The code data output and data strobe lines can directly drive one standard TTL load and 100 pF at 200 kHz. If the clock frequency is reduced the capacitive load may be increased proportionally. The matrix drive (X_1-X_9) and sense (Y_1-Y_{10}) lines are normally connected to each other via the switch matrix. Typical waveforms for these signals are shown in Figure 3.

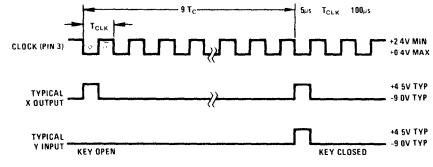


FIGURE 3. Matrix Signal Waveforms

Both the X and Y lines are unconditionally precharged toward the V_{GG} supply (-12V) when the clock is high. At the appropriate bit times of the scan cycle, each X line will go high during the time that the clock is low. For an open switch the Y line will remain negative. When a switch is closed the X line pulse will be transmitted to the Y input causing it to go high. The Y line will re-establish itself to the idle (negative level) condition during the next high level of the clock.

The X lines are capable of driving 75 picofarads at a 200 kHz clock rate. If the clock rate is reduced the load capacitance may be increased proportionally. Figure 4 is a schematic of the X output and Y input circuit of the encoder as it is normally connected to a matrix switch. The Y input has a high impedance device (.5 - 1MΩ) to the V_{GG} supply. This device is intended to support the idle

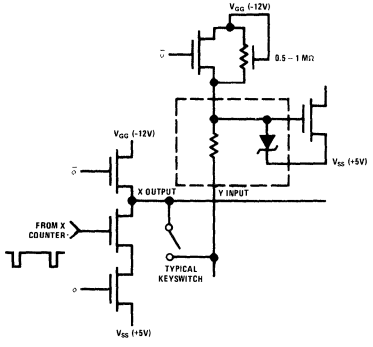


FIGURE 4. X Output – Y Input Schematic

level during low frequency operation. If capacitive or solid state switches are used it may be necessary to buffer the X and Y pins of the MM5740 from the keyswitch matrix. For this purpose reference should be made to Figure 5 which shows the typical X and Y line voltage-current characteristic. The right hand portion of the curve describes the X line active high characteristic while the left hand portion illustrates the X and Y characteristic when trying to charge toward the V_{GG} supply. These curves are useful for designing buffer circuitry driven by the X outputs or intended to drive the Y inputs of the MM5740.

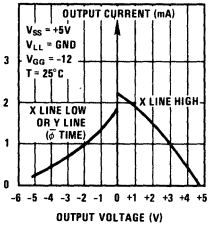


FIGURE 5. Typical X & Y Line Voltage – Current Characteristics

Shift Lock Operation

In many keyboards it is desirable to operate the keyboard in the shift mode for an indefinite period of time. This would occur, for instance, if it was desired to type a letter in upper case. A keyboard encoded with the MM5740 provides this function electronically, eliminating costly mechanically interlocked switches.

When the shift lock key is depressed, the keyboard assumes the shift mode. If the shift lock switch is then released, the keyboard remains locked in the shift mode. In addition, the shift lock pin (MM5740 pin 20) then operates as an output driver and supplies current to drive a shift lock indicator. This indicator signals the operator that the keyboard is in the shift lock mode. When it is desired to terminate this mode of operation, the shift key is momentarily depressed extinguishing the indicator light and placing the encoder in the unshifted mode. It should be noted that the shift lock keyswitch need only be a momentary single pole-single throw normally open switch. It is especially convenient to use a momentary lighted push button keyswitch for this application. Figure 6 illustrates a typical circuit diagram for implementing the shift lock function.

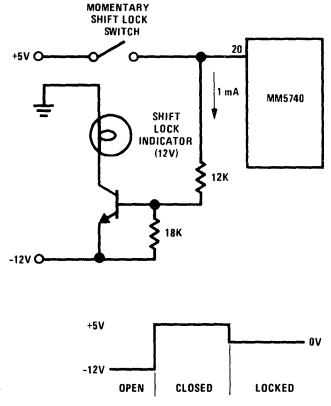


FIGURE 6. Shift Lock I/O Interface

Repeat Function

A useful feature contained in many keyboard systems is the repeat character key. By depressing this key and a data key the data character will be repeated. In addition to repeated character entry this function is useful for such things as underlining, back spacing and cursor control.

An incoming repeat clock (TTL level) at the desired rate is accepted by the MM5740. This clock is internally synchronized to the keyboard clock and is used to pulse the data strobe signal at the repeat rate. The pulse width of the data strobe is variable and its determination will be discussed shortly. This pulse occurs at the scan bit position occupied by the character key in question. Since the repeat clock is asychronous with the encoder clock, it is necessary that the repeat pulse width be at least as wide as one scan time (90 encoder clock periods). For most applications this presents no problem since the encoder clock rate will be several orders of magnitude faster than the repeat rate.

Program Unused Code Bits For Special Functions

In most cases only seven bits are required to generate the character codes. This leaves bits eight and nine available to provide other keyboard functions with a minimum of extra hardware. If parity is desired bit 8 is programmed to supply this function. For applications where special character control is required it is possible to use bits 8 and 9 to satisfy this need. For example, in a terminal application the display control keys are sometimes treated as non-transmit characters. In such situations, the ninth bit could be programmed to serve as a strobe inhibit. With this arrangement, the B_9 output (pin 39) is gated with the Data Strobe to prevent transmission for the appropriate characters.

Another frequent application occurs when it is required that only certain characters on the keyboard be allowed to repeat. This may be accomplished by programming bit 9 of the character code as a repeat inhibit bit. When gated with the repeat oscillator, a selective repeat input is supplied to the encoder via the repeat key. Since bit 9 is common in all modes, the repeat will be inhibited or enabled for every mode of the key in question. If it is desired to selectively repeat the same key in different modes, bit 8 may be used as the inhibit bit since this bit is programmable in each of the four possible keyboard modes.

In situations where it is desired to class characters in sets which are to be processed differently, some code bits may be programmed to provide a process recognition code. For example, by programming bits 8 and 9 as process recognition bits, keyboard characters may be divided into four classes for separate processing. When a character is entered, the processor or keyboard controller will examine the process code and channel the information to the appropriate processing logic or execute a predetermined routine according to character class.

It should be emphasized that any of the code bits may be programmed to provide additional features as explained above and that bits 8 and 9 are the most frequently available extra bits when using a standard seven bit code. Figure 7 illustrates a typical arrangement for implementing the transmit inhibit and selective repeat functions.

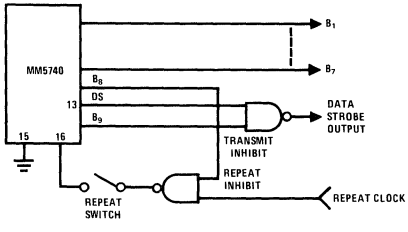


FIGURE 7. Typical Transmit Inhibit and Selective Repeat Arrangement

Data Strobe, Data Strobe Control and Output Enable

In order for the keyboard to effectively communicate with the system to which it is connected, it must supply a signal which alerts that system when data has been entered. This requirement is met by the Data Strobe output (pin 13). Once a valid character has been entered by the keyboard and is stored in the output latches of the MM5740, a Data Strobe is issued. The Data Strobe signal may take on several formats which will be discussed shortly.

The function of the Data Strobe Control input (pin 14) is to control the resetting of the Data Strobe once it has been activated. The Output Enable (pin 15) is also an encoder input and it serves two purposes. Firstly, it serves as the TRI-STATE control for the code data output lines (B_1-B_9). Secondly, it is used to control the resetting of the Data Strobe Output.

In order to better understand the interrelationship of these functions reference should be made to Figure 8 which illustrates the pertinent logic.

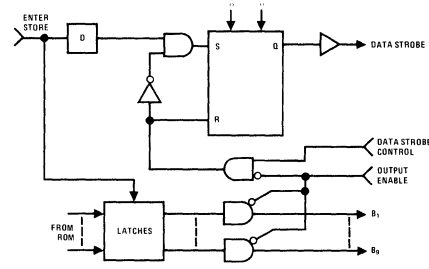


FIGURE 8. Data Strobe, Data Strobe Control and Output Enable Logic

When a valid key is entered an Enter Store signal is generated which enables the output latches to accept coded data from the ROM. The Enter Store signal, after being delayed one bit time, forms the set term of an RS flip flop. This flip flop inputs at $\overline{\phi}$ time (clock high) and outputs at ϕ time when the clock is low. The Data Strobe will go high when the flip flop is set, indicating that data is ready and stored in the output latches. The Data Strobe Control and Output Enable form the reset term for the Data Strobe flip flop. When the Data Strobe control is high and the Output Enable is low, the Data Strobe output will be reset. In addition, when the output enable is high the data output lines are placed in the high impedance state.

Now that the basic logic relationships are understood we will discuss typical applications concerning these functions. For a pulse mode data strobe, the output enable is grounded (always enabled) and the Data Strobe is tied directly to the Data Strobe Control. With this connection, a pulse which is one bit time wide will appear on the Data Strobe line to indicate available data is present. If a pulse width greater than 1 bit time is required,

it may easily be achieved by inserting an RC network between pin 13 and pin 14 as shown in Figure 9. The pulse width is approximately 0.6 RC. This feature eliminates the need for a one-shot circuit often found in many keyboard systems. By allowing for a resistor and capacitor on the printed circuit board, a variable pulse width can be achieved without affecting board layout. If a one bit wide strobe is desired, a wire link can replace the space taken by the resistor and the capacitor is left out.

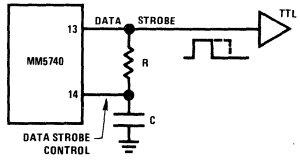


FIGURE 9. Variable Width Pulse Data Strobe

In many applications, it is more convenient to have a level strobe mode of operation. For example, in bus structured systems where there are many keyboards and/or other peripherals connected to the main processing system a controlled level strobe is desired. Such a configuration is illustrated in Figure 10. In this situation many peripherals share a TRI-STATE bus. When a peripheral such as the

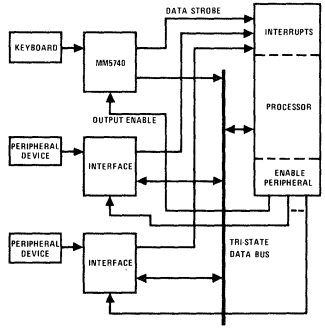


FIGURE 10. Keyboard Use in a Bus-Structured Interrupt System

keyboard has data available, the Data Strobe goes high. This signal interrupts the processor. At the appropriate time, the processor will respond to this interrupt by setting a flag. This flag can be used to enter a read peripheral mode and send an enable signal to the keyboard. When the output enable of the MM5740 goes low the Data Outputs are presented to the TRI-STATE bus for acceptance by the processor. On the next negative edge of the clock, the data strobe will be automatically reset. At this point the keyboard and processor have completed a data exchange and conditions are such that additional data may be entered. Of course the time periods of concern in such a design are dictated by the keyboard activity rate and the processor organization.

In most situations, the processor will readily accept data presented by the keyboard at normal keyboard rates. If conditions are such that the processor will be busy for periods of time longer than the time between keyboard entries, then a buffer memory will be needed to store those entries. These considerations pertain to total system design and will vary in each particular situation.

For the purpose of further illustrating the use of the data strobe, data strobe control and output enable, let us consider the particular application where it is desired to poll several keyboards in a system. We will consider that the keyboards can be either localized or at remote locations and that a scanning interrogation technique will be used.

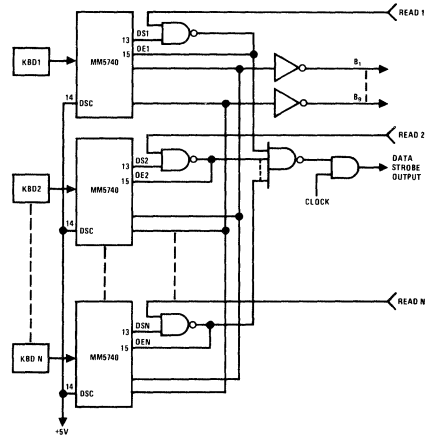


FIGURE 11. Polling System for Localized Keyboards

In Figure 11 such a polling set up is shown for localized keyboards and the associated timing diagram is shown in Figure 12. Since the keyboards are local, the wiring capacitance can be reasonable enough to make use of the TRI-STATE feature of the MM5740 and allow all encoders to share a common data bus. When a character is entered from any keyboard, the corresponding data strobe line (pin 13) will go high. When the keyboard is read, the output enable line will go low, taking the data lines out of the high impedance state. One bit time later, the data strobe will be automatically reset which in turn will drive the output enable high again. This removes that keyboard from the data bus and allows the remaining keyboards to be interrogated. The data strobes for each keyboard are combined and gated with the clock to form a single data strobe output to the receiving system. When the receiving system sees the data strobe pulse, the output data is stable and ready for acceptance.

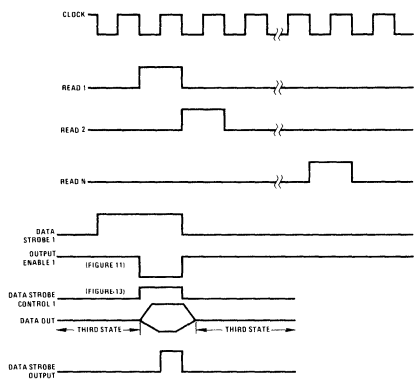


FIGURE 12. Timing Diagram for Keyboard Polling System

When this application applies to remote keyboards or a heavily loaded TTL bus, the keyboard encoders must be buffered. This may be accomplished as shown in Figure 13 by using TTL TRI-STATE devices between the encoders and the common bus. In this technique, the keyboard encoders are always enabled by grounding pin 15. When the data strobe goes high and the keyboard is interrogated, the data strobe control line will go high. This takes the data output gates out of the high impedance state. On the next positive clock the data will be stable and ready for acceptance by the receiving system. In addition, the fact that the data strobe control went high will reset the data strobe on the next negative edge of the clock.

Use Two Encoders for 180 Key Capability

Some special applications may require an N-key rollover encoder capable of handling a keyboard with greater than 90 keyswitches. Such situations are easily handled by using two MM5740 encoders to provide a capability of up to 180 keyswitches. Figure 14 illustrates how such a system is configured and Figure 15 shows typical timing waveforms. It should be noted that such a configuration is achieved with a minimum of peripheral circuitry.

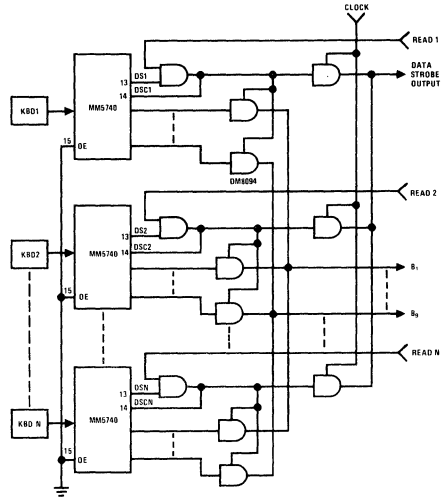


FIGURE 13. Polling System for Remote Keyboards

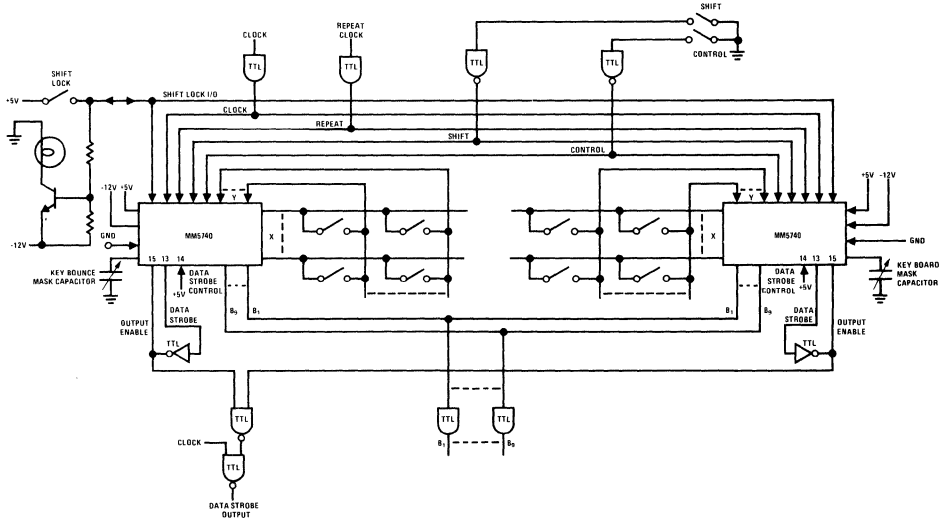


FIGURE 14. Two Encoders Give 180 Key, N-Key Rollover Operation

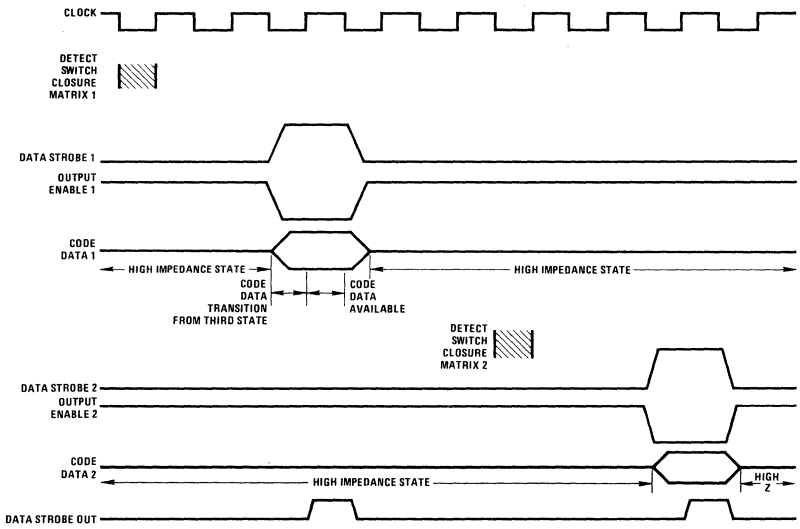


FIGURE 15. Typical Timing Diagram – 2 Encoder Expansion Operations

The keyswitches (up to 180) are wired in two X-Y matrices; one set for each MM5740 encoder. Both encoders operate asynchronously with respect to each other; at any time the scan position in one matrix may not be the same scan position in the second matrix. The essential point to remember is that no two keys may be depressed at "exactly" the same time and still result in a valid code output. This assumption is quite valid in that there is always some finite time period between the depression of a key and the depression of a succeeding key, even though that time may be as low as 5-10 ms. Anyone using a keyboard as an input device to his system must know what the maximum keyboard activity rate will be for his particular application. This information tells the system designer how much keybounce he can tolerate, what the encoder frequency should be, the type of rollover to specify, the width of the data strobe, whether his system is fast enough to accept asynchronous data from the keyboard without a buffer store and many other vital design specifications.

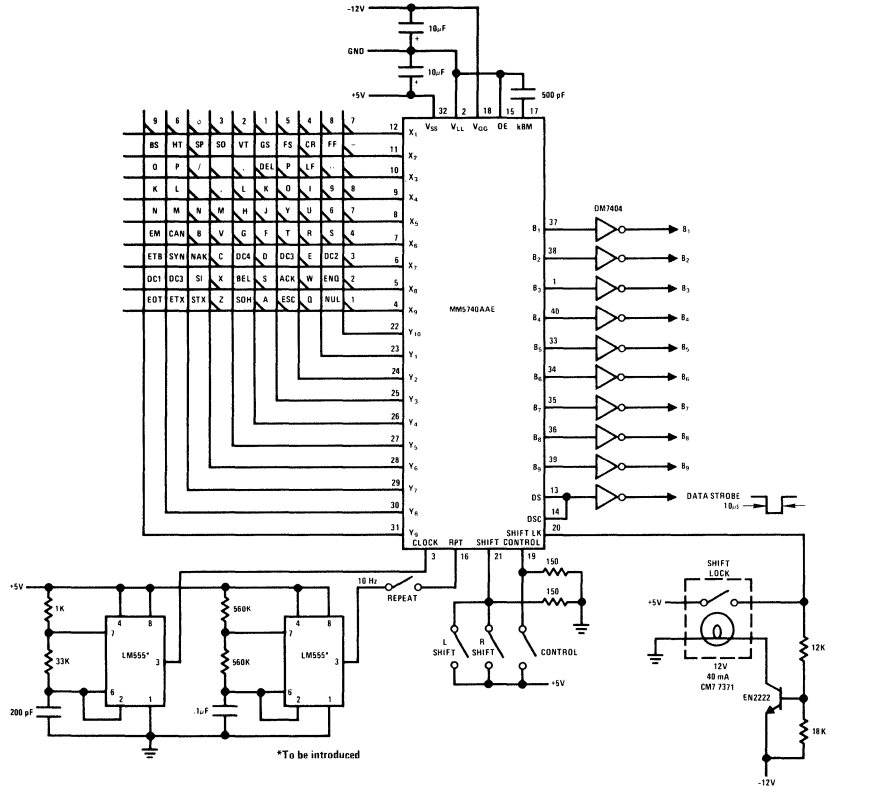
The above discussion relates to the application shown in Figure 14 in the following way. With no activity on the keyboard the data outputs of both encoders are in the third or high impedance state. A valid key closure in one matrix activates the data strobe and code data outputs of the corresponding encoder removing it from the high impedance state. The second encoder remains in the high impedance state. Resetting of the data strobe is automatically accomplished via the output enable pin and results in a one bit time wide data strobe output pulse. Code data is valid during the time that the output enable is low and the clock is high. After the first data strobe is reset both encoders are in the idle condition. If a valid closure is now detected in the second switch matrix, the second encoder performs exactly like the first one did a short time earlier. During this activity, the first encoder is in the high impedance state. The data strobe outputs from each encoder are combined in a 7400 gate to provide one data strobe output line for the keyboard system.

Since both key switch matrices are physically part of the same keyboard, two keys will not be activated at exactly the same time. Therefore, each encoder, operating asychronously with respect to the other, perform as separate entities. However, the receiving system which communicates with the keyboard encoders cannot distinguish that there are two encoders and two sub-matrices. Externally this arrangement appears as a single encoder with up to 180 key capability.

Complete ASR 33 Keyboard System

By using the MM5740AAE or MM5740AAF, typical ASR 33 type communications keyboards may be configured. These parts are available as standard off the shelf units. While both versions contain the same ROM encoding (all 90 key positions), the AAE provides N-key rollover and the AAF is programmed for 2-key rollover. It should be noted that many variations of ASR 33 keyboards may be configured by connecting to the appropriate matrix coordinates.

One common keyboard system is shown in Figure 16. The associated keyboard layout is shown in Figure 17 while the key codes are shown in Figure 18. It is apparent that a minimum of external hardware is needed to configure a total keyboard. The ease with which the MM5740 is able to interface with inexpensive TTL circuitry eliminates the need for many external resistors and level translators. It should also be noted that MM5740 TTL inputs may be supplied from standard TTL logic without any restrictions on the TTL-TTL loading. For example, the MM5740 clock input may be supplied from a standard TTL gate which also drives 10 other TTL loads. By incorporating any of the techniques discussed previously many variations of this basic keyboard system may be implemented with a minimum of additional hardware.



Note 1: Matrix coordinates not shown with switch are not used for this particular configuration. These coordinates, however, are programmed for the characters shown and may be used if desired.

Note 2: N-key rollover – MM5740AAE, 2-key rollover – MM5470AAF.

Note 3: Clock frequency = 100 kHz

Note 4: Scan cycle = 900μs

Note 5: Repeat rate = 10 characters per second

Note 6: Key bounce mask time = 4.0 ms

Note 7: Data strobe = 10μs pulse

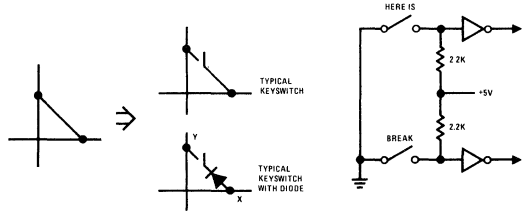
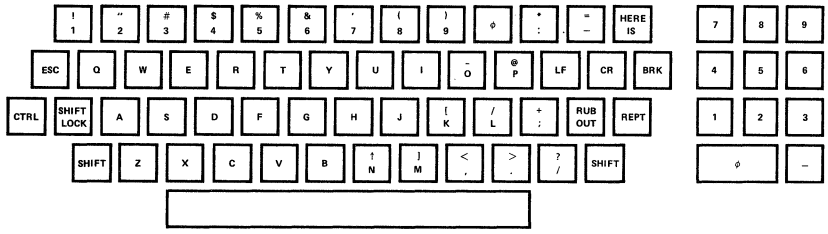


FIGURE 16. ASR-33 Keyboard



ASR 33
MM5740AAE (N-key rollover)
MM5740AAF (2-key rollover)

FIGURE 17. Typical Keyboard Arrangement

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
1	1	0	0	0	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	8	8	8	8
1	2	0	0	1	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	4	4	4	4
1	3	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	5	5	5	5
1	4	1	0	0	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	1	1
1	5	0	1	0	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	2	2	2	2
1	6	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	3	3	3	3
1	7	0	0	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	☼	☼	☼	☼
1	8	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	6	6	6	6
1	9	1	0	0	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	9	9	9	9
1	10	1	1	1	0	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	7	7	7	7
2	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FF	FF	FF	FF
2	2	1	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	CR	CR	CR	CR
2	3	0	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	FS	FS	FS	FS
2	4	1	0	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	GS	GS	GS	GS
2	5	1	1	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	VT	VT	VT	VT
2	6	0	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	SO	SO	SO	SO
2	7	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	SP	SP	SP	SP
2	8	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	HT	HT	HT	HT
2	9	0	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	BS	BS	BS	BS
2	10	1	0	1	1	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	~	~	^	^
3	1	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	ϕ	ϕ	ϕ	ϕ
3	2	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LF	LF	LF	LF
3	3	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	1	0	0	0	0	P	@	DLE	NUL
3	4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	DEL	DEL	DEL	DEL
3	5	1	1	0	1	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	,	+	,	+
3	6	0	1	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	·	·	·	·
3	7	1	1	1	1	0	0	1	0	1	1	1	0	0	0	1	0	1	1	1	0	0	/	?	/	?
3	8	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	P	P	DLE	DLE
3	9	1	1	1	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	SI	SI
3	10	0	1	0	1	1	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1		*	.	*

Negative True Logic

$B_1 - B_7$ = ASCII Code
B_8 = Even parity (on $B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8$)
B_9 = Selective Repeat Bit

Note: Use B_8 if parity bit is desired.

FIGURE 18. Code Assignment Chart

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
4	1	1	0	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	9	)	9	)
4	2	1	0	0	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	I	I	HT	HT
4	3	1	1	1	1	1	0	0	1	1	1	0	1	0	0	0	0	0	1	0	0	1	O	—	SI	US
4	4	1	1	0	1	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	K	!	VT	ESC
4	5	0	0	1	1	0	0	0	1	1	1	0	1	0	0	0	0	0	1	0	0	1	L	\	FF	FS
4	6	0	0	1	1	0	0	1	0	1	1	1	0	0	0	1	0	1	1	1	0	0	.	^	.	.
4	7	0	1	1	1	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	.	.	.	.
4	8	0	0	1	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	L	L	FF	FF
4	9	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	K	K	VT	VT
4	10	0	0	0	1	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	8	(	8	(
5	1	0	1	1	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	6	&	6	&
5	2	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	U	U	NAK	NAK
5	3	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	Y	Y	EM	EM
5	4	0	1	0	1	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	J	J	LF	LF
5	5	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	H	H	BS	BS
5	6	1	0	1	1	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	M		CR	GS
5	7	0	1	1	1	1	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	N	^	SO	RS
5	8	1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	M	M	CR	CR
5	9	0	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	N	N	SO	SO
5	10	1	1	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	7	'	7	'
6	1	1	0	1	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	5	%	5	%
6	2	0	1	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	R	R	DC2	DC2
6	3	0	0	1	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	T	T	DC4	DC4
6	4	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	F	F	ACK	ACK
6	5	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	G	G	BEL	BEL
6	6	0	1	1	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	V	V	SYN	SYN
6	7	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	B	B	STX	STX
6	8	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	CAN	CAN	CAN	CAN
6	9	1	0	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	EM	EM	EM	EM
6	10	0	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	4	$	4	$

Negative True Logic

$B_1 - B_7$ = ASCII Code
B_8 = Even parity (on $B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8$)
B_9 = Selective Repeat Bit

Note: Use B_8 if parity bit is desired.

MATRIX ADDRESS		COMMON					UNSHIFT				SHIFT				CONTROL				SHIFT CONTROL				CHARACTER			
X	Y	B_1	B_2	B_3	B_4	B_9	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	US	S	C	SC
7	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	DC2	DC2	DC2	DC2
7	2	1	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	E	E	ENQ	ENQ
7	3	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	DC3	DC3	DC3	DC3
7	4	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	D	D	EOT	EOT
7	5	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	DC4	DC4	DC4	DC4
7	6	1	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	C	C	ETX	ETX
7	7	1	0	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	NAK	NAK	NAK	NAK
7	8	0	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	SYN	SYN	SYN	SYN
7	9	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	ETB	ETB	ETB	ETB
7	10	1	1	0	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	3	#	3	#
8	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ENQ	ENQ	ENQ	ENQ
8	2	1	1	1	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	W	W	ETB	ETB
8	3	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ACK	ACK	ACK	ACK
8	4	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	S	S	DC3	DC3
8	5	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	BEL	BEL	BEL	BEL
8	6	0	0	0	1	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	X	X	CAN	CAN
8	7	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SI	SI	SI	SI
8	8	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	DLE	DLE	DLE	DLE
8	9	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	DC1	DC1	DC1	DC1
8	10	0	1	0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	2	"	2	"
9	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NUL	NUL	NUL	NUL
9	2	1	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	0	Q	Q	DC1	DC1
9	3	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	ESC	ESC	ESC	ESC
9	4	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	A	A	SOH	SOH
9	5	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	SOH	SOH	SOH	SOH
9	6	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	Z	Z	SUB	SUB
9	7	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	STX	STX	STX	STX
9	8	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ETX	ETX	ETX	ETX
9	9	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	EOT	EOT	EOT	EOT
9	10	1	0	0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	1	'	1	'

Negative True Logic

$B_1 - B_7$ = ASCII Code
B_8 = Even parity (on $B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8$)
B_9 = Selective Repeat Bit

Note: Use B_8 if parity bit is desired.

FIGURE 18. Code Assignment Chart (cont'd)

CONCLUSION

The MM5740 keyboard encoder offers a wide versatility of features not found in conventional MSI designs. In addition, performance specifications of the MM5740 far exceed those of other MOS encoders currently available. The wide range of clock frequency, low power dissipation, variable bounce masking, ease of interface, rollover capability and its many other notable features make the MM5740 a logical choice for your keyboard encoding function. This encoder has been designed not only as a powerful part of any keyboard system but also with the intention of minimizing the amount of additional keyboard electronics and simplifying the interaction of the keyboard with other system components with which it must communicate. As a result, the MM5740 should go a long way toward improving the cost-performance basis of keyboard oriented systems.

SAVING ROMs IN HIGH-RESOLUTION DOT-MATRIX DISPLAYS AND PRINTERS

INTRODUCTION

Conventionally, the number of bits in a digital character generator's read only memory is proportional to the number of dots in the character matrix. That is, the ROM array ordinarily doubles and redoubles in size as one scales up the resolution or changes from an upper-case to an upper-case/lower-case font.

Fortunately, such progressions may not be required. Reorganizing the ROMs to suit the specific application often save thousands of bits and allows the designer to use smaller, faster, more economical monolithic ROMs. As a simple example, expanding the array in 32-character subsets rather than the more conventional 64-character subsets will enhance performance and save up to 25% of ROM capacity in typical UC/LC applications.

Savings much greater than 25% are possible when the matrix size reaches a point where several monolithic ROMs are needed to store the font. We have found a two-stage, column-generation approach called "intermediate coding" to be much more efficient than straightforward dot-matrix generation. It exploits the fact that column patterns tend to become highly redundant as the matrix size increases.

One version of this new technique automatically proportions character widths as in letterpress printing. This gives each character a more natural shape and eliminates the irregular spacings usually seen around "I" and other narrow characters. Yet the control logic is simple and the ROM savings approach 40% at typical font sizes.

Such advantages are available immediately, without development of special ROMs. The designs can be implemented with standard MOS or bipolar ROMs currently in production. In fact, intermediate coding broadens the cost/performance options by allowing a combination of MOS and bipolar ROMs to be used.

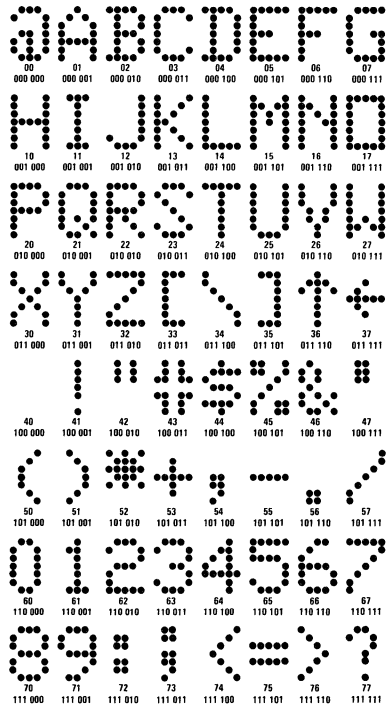
DOT-CHARACTER FONTS

Dot-character styles ranging in complexity from 5 x 7 to 12 x 24 or more dots per character have been developed to meet the human-engineering standard of various industries using digital displays and printers. The more popular sizes are listed in Table I.

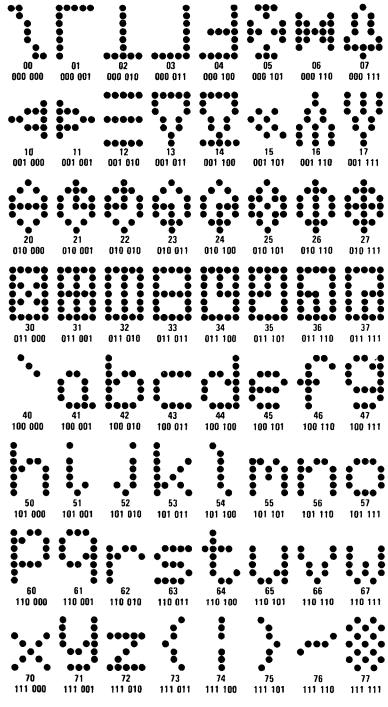
The 5 x 7 fonts, such as Figure 1, lead in applications volume due to their use in low-cost data

TABLE I. Typical Dot-Matrix Character Fonts

SIZE AND SCANNING	DOTS PER CHARACTER	THEORETICAL CHARACTER ROM	DESIGN EFFECTIVENESS	PRACTICAL DESIGNS
5 x 7				
Horizontal	35	64 x 7 x 5 = 2 — 1/2k	1.00	Fig. 3
7 x 5				
Vertical	35	64 x 5 x 7 = 2,560	1.00	Fig. 3
7 x 9				
Horizontal	63	64 x 9 x 7 = 4,032	0.67	Fig. 6
9 x 7				
Vertical	63	64 x 7 x 9 = 4,032	1.00	Figs. 5 & 8
7 x 12 & 8 x 12				
Horizontal	96	64 x 12 x 8 = 6,144 and 96 x 12 x 8 = 8,216	1.00 1.00	Figs. 6 & 7
12 x 7 & 12 x 8				
64 Character Vertical	96	64 x 8 x 12 = 6,144	1.00	Fig. 8C
96 Character Vertical	96	96 x 8 x 12 = 9,216	1.00	Fig. 8B
12 x 16				
64 Character Horizontal	192	64 x 16 x 12 = 12,288	1.50 for Fig. 9A	Fig. 9A
96 Character Horizontal	192	96 x 16 x 12 = 18,432	1.50 Fig. 9	Fig. 9B
16 x 12				
64 Character Vertical	192	64 x 12 x 16 = 12,288	1.50 for Fig. 9A	Figs. 6, 7, & 9
96 Character Vertical	192	96 x 12 x 16 = 18,432	1.50 for Fig. 9B	
24 x 12				
64 Character Vertical	288	64 x 12 x 24 = 18,432	2.00 for Fig. 9B	Figs. 6, 7, & 9
64 x 13 x 10 to 64 x 13 x 16				
64 Character Variable Font Width	208	64 x 13 x 16 = 13,312	3.06 for Fig. 10	Fig. 10



(A) Upper-Case Font



(B) Lower-Case Font

FIGURE 1. ASCII Full Set Font of 128 5 x 7 Characters

interface terminals (although some terminal manufacturers are going to larger sizes in response to complaints that 5 x 7 presentations cause eyestrain). In other applications, a standard is often set by older printing techniques. To cite a few examples: business-machine users are accustomed to typewriting; advertisers want characters with "sales appeal" on their billboard displays; scoreboards and traffic-control signs must be read easily at a distance; and electronic printing systems may have to simulate several metal type fonts.

The matrix size is frequently enlarged to improve lower-case character definition in UC/LC applications. A 5 x 7 font typically grows to 7 x 9 for UC and 7 x 12 for LC, as in Figure 2. Likewise, 7 x 9 is expanded to 8 x 12 and 12 x 16 to 12 x 24 for lower-cases.

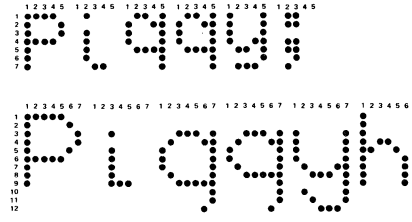


FIGURE 2. UC/LC Characters at 5 x 7 and 7 x 12 Matrix Sizes

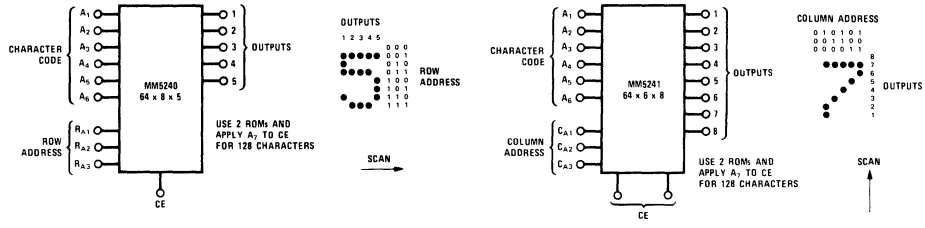
At 5 x 7, it is most economical, as a rule, to program a "full set" of 128 UC/LC characters in standard character-generator ROMs. The full set in Figure 1 is stored in two 64-character MOS ROMs. This provides a mass-production base and equalizes access times. If the 32 special symbols generated with the ASCII control codes are not usable, they are simply blanked by disenabling the lower-case ROM when the seventh ASCII bit is "0." But if the font is scaled up to simulate typewriting, for example, this practice becomes wasteful since 96 characters would suffice.

Another complication is that many specialized font sizes, such as 11 x 9, do not fit neatly into standard ROMs made in building block sizes. In other words, one cannot store the font in a minimum-sized ROM array without paying the extra costs of custom ROM development or specialized low-volumn ROMs.

CHARACTER-GENERATOR ROMs

Consequently, character-generator ROMs have been developed that adapt to a variety of font sizes. They may not exactly fit the theoretical matrix array at odd sizes. but that is easily offset by the economy of parts standardization.

Two such MOS ROMs are outlined in Figure 3 with their addressing for 5 x 7 horizontal scanning and 7 x 5 vertical scanning. The vertical-scan subsystem in Figure 4 shows the amount of support logic typically required in a display.



(A) 5 x 7 Horizontal-Scan, 64-Characters

(B) 7 x 5 Vertical-Scan, 64-Characters

FIGURE 3. MM5240 and MM5241 Standard Character-Generator ROMs

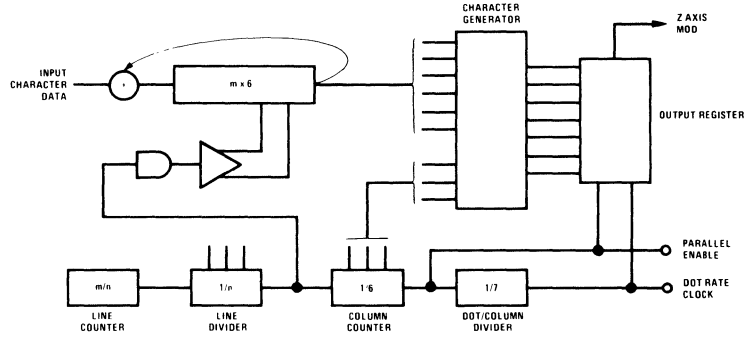


FIGURE 4. Typical 7 x 5 Vertical-Scan Display Generator Subsystem

The MM5240 expands straightforwardly in 64-character increments to larger fonts, such as the 9 x 7 or 10 x 8 arrays in Figure 5A. An expansion such as Figure 5B would be used to provide a full set UC/LC font. These expansions keep the character rate the same as at 5 x 7, whereas doubling the size of each monolithic ROM would not.

32-CHARACTER BLOCKS

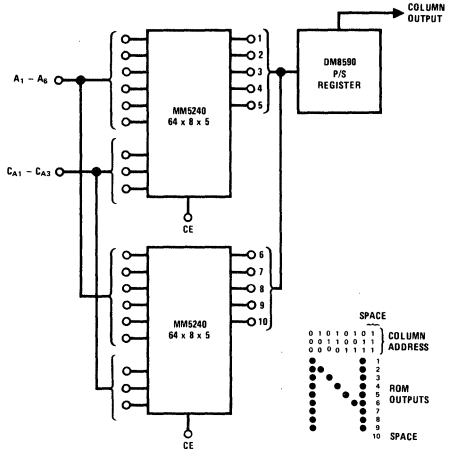
A similar expansion of the MM5241, as in Figure 6A, would provide 7 x 9 to 8 x 12 horizontal-scan fonts. However, the direct 64-character expansion places a ROM-enabling operation in the middle of the character. Such operations are common in large-font generator designs.

A simple solution to this problem is to "steal" a character-address input, use it as a row-address input, and then use a chip-enable input as a character input (Figure 6B). This provides a 32-character or 64-character block enabled during the between-characters spacing interval. A 32-character block would be the only ROM required in a system using only numbers and symbols.

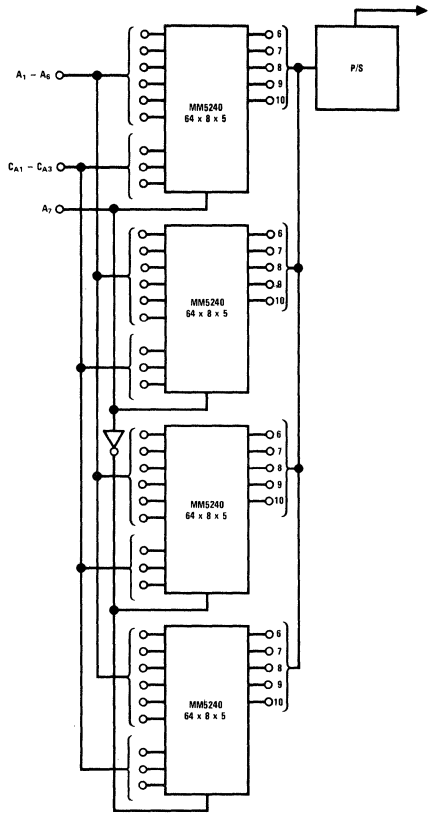
However, the chief attraction of this conversion is in UC/LC applications. Figure 7 shows how to use three ROMs to generate 96 7 x 9 to 8 x 12 horizontal-scan characters—a 25% savings compared with a "full set" expansion. The chip-enable inputs are programmed to sense the sixth and seventh character-address bits. External decoders aren't needed.

If each ROM in Figure 7 is replaced with a parallel assembly of three ROMs (24 outputs), the result is a 24 x 12, 96-character vertical-scan generator with the same character rate as at 8 x 12. In other words, the 32-character approach maintains the benefits of parts standardization and performance up to a very high resolution.

Other ROMs can be used in this fashion. In Figure 8, the MM5227 TRI-STATE® and MM5288 256 x 12 ROMs are shown in expansions that complement those of the MM5241. These ROMs provide access times well under a microsecond. For rates in the nanosecond range, general-purpose bipolar ROMs with four or eight outputs, such as the DM8597 256 x 4 and DM8596 512 x 8 can be worked into similar organizations.

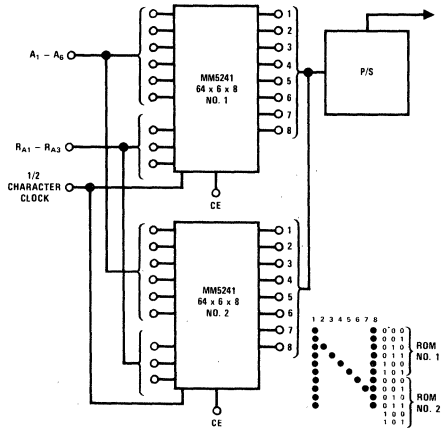


(A) 9 x 7 or 10 x 8 Vertical-Scan, 64-Characters

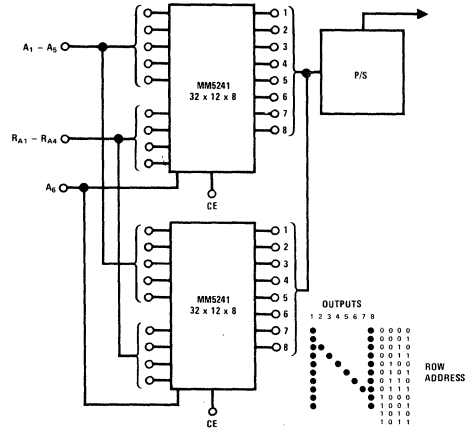


(B) 9 x 7 or 10 x 8 Vertical-Scan, 128-Characters

FIGURE 5. Expansion of MM5240 to Larger Fonts



(A) 7 x 9 to 8 x 12 Horizontal-Scan, 64-Characters



(B) 7 x 9 to 8 x 12 Horizontal-Scan, 64-Characters

FIGURE 6. Conventional and Improved MM5241 Expansions to 8 x 12

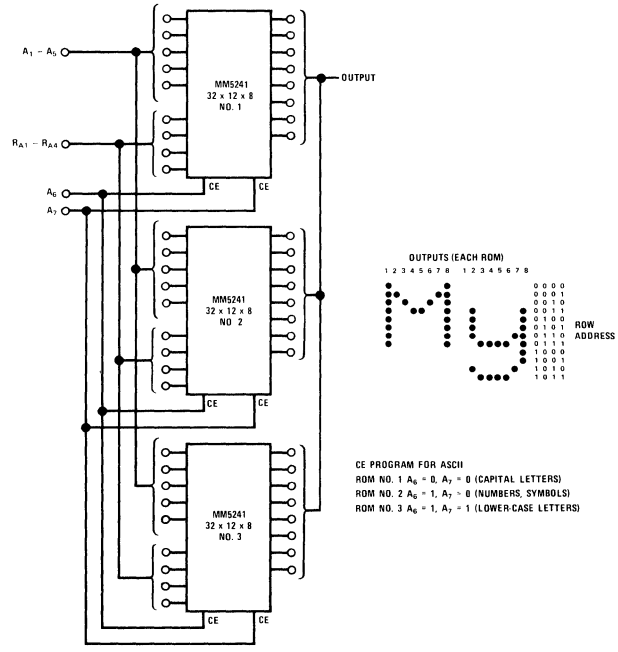
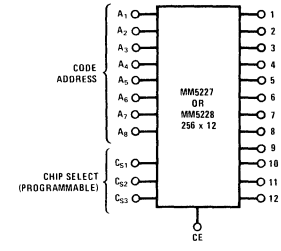
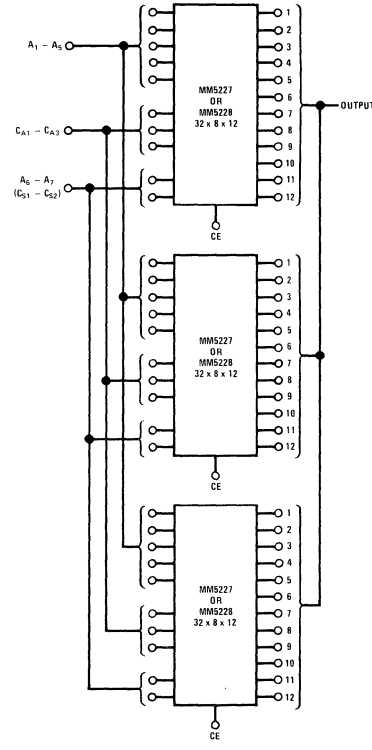


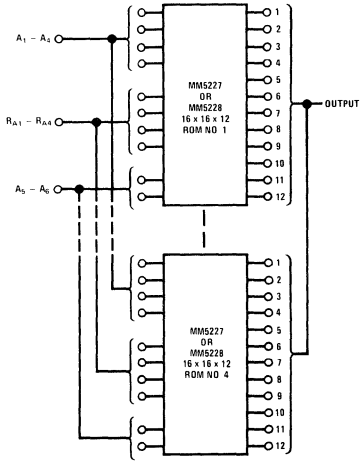
FIGURE 7. Using 32-Character Expansions for 7 x 12 or 8 x 12, 96-Character Generator



(A) Basic ROM



(B) 9 x 7 to 12 x 8 Vertical-Scan, 96-Characters



(C) 12 x 16 Horizontal-Scan, 64-Characters

FIGURE 8. Addressing General-Purpose ROMs as Character Generators

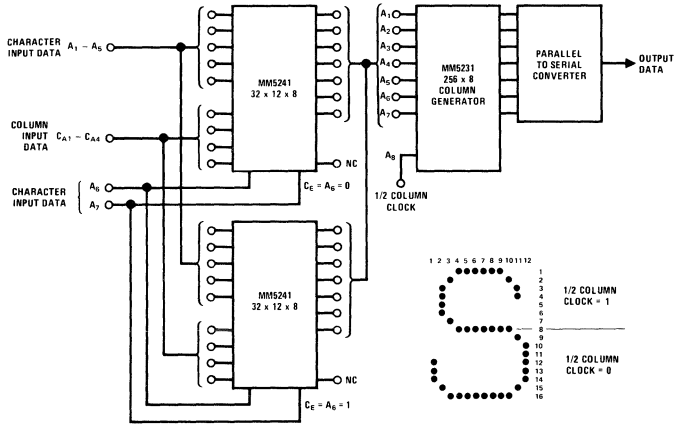
13

INTERMEDIATE CODING

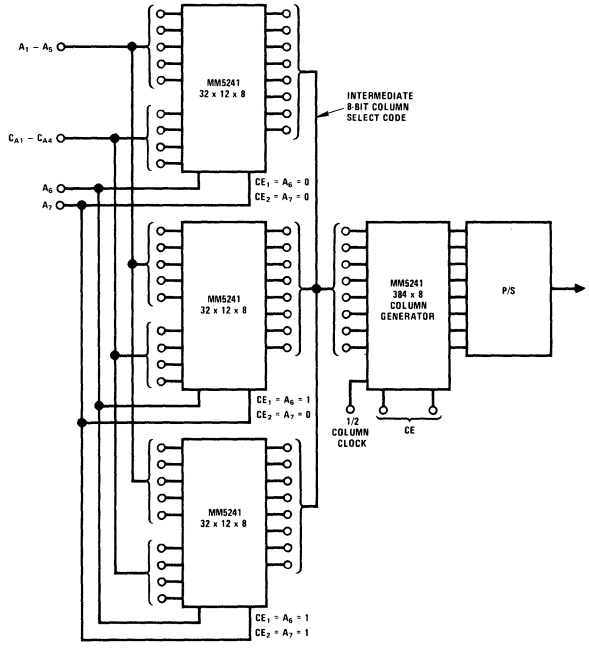
Designs proportioned to the matrix size are not the most efficient at the larger font sizes. It pays to analyze the actual character patterns to determine whether other organizations can be used.

For example, the full-dot columns in such vertical-scan characters as b, B, d, D, H, T, etc., are usually identical. An upper-case font typically contains only 60 unique column patterns at 7 x 5, 110 at 9 x 7, 120 at 11 x 9, and 122 at 16 x 12. Theoretically, they could all have been unique, since there is a possible pattern variation ranging from 128 to 65,536 (2^7 to 2^{16}). UC/LC and horizontal-scan fonts are more variable than upper-case vertical-scan fonts, but they are still far from worst-case.

This analysis led to the organization in Figure 9A. Instead of doubling the 64 x 12 x 8 organization to produce fonts up to 16 x 12, it adds only a 2k



(A) 12 x 16 Vertical Scan (UC)



(B) 16 x 12, 96-Character Generator (UC/LC)

FIGURE 9. Intermediate Coding Designs (MOS ROM Organizations)

ROM. Up to 128 unique column patterns are stored in 8-bit, half-column segments in the MM5231 256 x 8 ROM. These are accessed with 7-bit intermediate codes selected with the input array and a half-column clock at a submultiple of the dot rate. The intermediate codes necessary to form each character are simply listed in character-generator fashion in the input code converters. At 16 x 12, the savings for an upper-case font are 12k − 8k or 4 kilobits—33%.

Since the 8-bit outputs of the MM5241 ROMs actually allow 128 unique columns to be selected, the savings could grow rapidly through several expansion levels even without further rearranging. If more than 128 unique column codes are required the second ROM in the storing can be changed to possibly a 512 x 8 ROM (MM5232) therefore giving 256 unique columns which can be generated for the larger fonts and character group sets (96 characters or 128 characters).

Assume a 16 x 12, 96-character requirement. MM5241 ROMs added as in Figure 9B would provide 192 unique column patterns and the savings would be at least 18k − 12k = 6k.

It might be necessary at the 24 x 12 UC/LC size to use two MM5227 256 x 12 ROMs in parallel, but this would still save 27k − 15k = 12k (or perhaps 36k − 18k in a 128-character application, using four input and two output ROMs). The efficiency grows with font size because the column patterns become more redundant.

At first glance, the organization appears to double the access time because there are two stages to be accessed in sequence. But since there is no feedback, the stages can operate in a ripple mode. Thus, an 8-bit bipolar register can be inserted between the stages to temporarily store each intermediate code. This restores the overall access time to that of the slowest ROM in the series (e.g., less than a microsecond for MOS ROMs) and the character rate is essentially the same as that achieved with conventional ROM techniques.

Alternatively, the output ROM, input ROM, or both may be bipolar to increase the rate. The DM8596 512 x 8 ROM fits most large-font geometries quite well and costs less than sub-assemblies of 1k bipolar ROMs. Again, an intermediate register will maximize the rate.

REPEAT-PATTERN CODING

Some character styles have bold "double dot" or similar patterns that result in a high probability of the same column pattern repeating sequentially in the same character. This characteristic is common in "ticker tape" systems, large-panel and billboard displays, news bulletins broadcast to appear as a running line across a television picture, and so forth. Typical fonts exhibit less than 256 actual changes of column patterns through a 64-character sequence, not the worst-case of 320 at 7 x 5, 640 at 10 x 8, and so forth. Therefore, an organization that holds the column output static until it has to change would be highly efficient.

Figure 10 is a practical design for upper-case fonts with 10 x 10 to 13 x 10 matrices. It saves nearly 40% of ROM capacity. Moreover, the matrix width varies with the character shape as can be seen in the example word LIMB. The characters look more natural and are evenly spaced. Column height is changed by programming the outputs to be used.

Proportional spacing makes this organization an excellent choice for ink-dot spray printers and other "line of type" printing applications, as well as vertical-scan displays.

This technique does not lend itself directly to raster-scan displays since characters are scanned sequentially on one raster line at a time rather than completing a character before starting a new character. To use this technique on raster-scan an intermediate storage memory would be necessary for as a line memories.

PROGRAMMING AND OPERATION

Assume a nominal matrix size of 13 x 10. This takes a 256 x 16 ROM array. Each 16-bit output word contains a 13-dot column pattern, a 2-bit repeat code and, in the last word of a character, an EOC bit (end of character "1" bit). Address location 0000 0000 is reserved for an all-zero spacing column.

The first address of each character is listed in the small input ROM at locations where they will be accessed by the standard code. The intermediate code will then be the starting address and the next column-select codes for each character will be generated sequentially by the logic.

Suppose characters @ through K occupy locations 0000 0001 through 0010 1111 in the main ROM. Then, L's three words occupy locations 0011 0000 through 0011 0010, M starts at 0011 0011, and so forth. L takes three words at the 13 x 10 size since the 2-dot bar pattern can be repeated only four times with a 2-bit repeat code. If the columns were programmed 12 or less dots high, a 3-bit repeat code could be used. L would be generated with two words and single-pattern characters like "dash" with one word. This solution uses only 2 x 16 bits of storage for the character L and compared with its present technique of 10 x 12 = 120 bits.

Now, let's generate LIMB. First, the standard code for L (e.g. 001 100) is converted to 0011 0000, which sets the address counter. The address counter access that word in the main ROM, and the repeat code in the output sets the master counter to time out in two column scanning intervals.

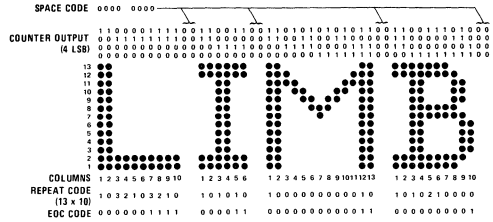
L's first two columns are thus formed. At the master counter's terminal state, the address counter advances to 0011 0001, the master counter is reset

to time out in four column intervals, the address counter advances again, and word 0011 0010 is accessed during four intervals.

This last word includes an EOC bit. When EOC and the time-out state of the master counter coincide, gate 1 clears the address counter. Now address 0000 0000 generates the space pattern in two spacing columns. When the master counter reaches its second state, gate 2 enables the address counter's parallel preset inputs. Finally, the input ROM sets the counter to the starting address for I and the process continues through I, M and B.

Proportional spacing is inherent. So is high-speed since the input ROM is a small bipolar array. The main ROM can be either MOS or bipolar general-purpose ROMs. This organization should also expand efficiently since the repeat probability tends to rise with matrix width.

In printing applications involving more complex characters, the operational advantages might be of more interest than ROM savings. For example, two 64 x 6 x 8 or 512 x 8 ROMs might be used as an UC/LC generator with the ninth address input a direct shift control.



(Repeat Pattern Character Quality and Coding Example)

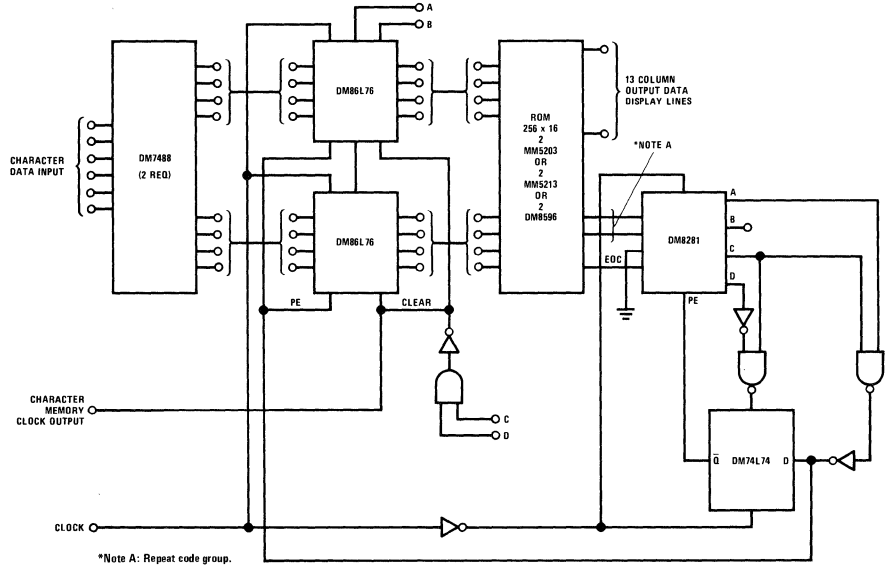


FIGURE 10. Repeat-Pattern Vertical-Scan Generator

A SIMPLE POWER SAVING TECHNIQUE FOR THE MM5262 2k RAM

INTRODUCTION

The MM5262 is a state of the art RAM designed to operate efficiently in modern bus organized systems. Most bused systems present the address information to the data bus only during the early portion of the machine cycle and then transfer data during the remainder of the cycle. The MM5262, unlike many other RAMs, does not need a memory address register to hold the address stable on its inputs during the complete cycle because the address is clocked into the MM5262 on-chip address register by Phase 1. The address and chip select signals need only be applied during Phase 1 and the Phase 1 to Phase 2 gap.

SAVING POWER

Because of the very low power dissipation of the MM5262 when the clocks are turned off (< 2.0 mW), a method for decoding the clocks of unselected chips in the memory array would result in a sizable decrease in power consumption. A problem arises because to deselect a chip, a Phase 1 pulse must be applied to clock the disable signal into the chip. There would be little advantage in allowing Phase 1 to free run and decoding only Phase 2 and Phase 3 because approximately 75% of the power dissipation is associated with Phase 1. The best solution is a decoding arrangement where the disabling of Phase 1 is delayed by one cycle and the enabling of Phase 1 is not delayed. The chip will receive one extra Phase 1 pulse to disable it and will no longer draw power until it is again enabled. The power then becomes worst case when alternately accessing two chips. Both chips will draw power continuously while all other deselected chips draw 0.1 mA each. Table I shows expected power supply currents for various size memories per bit of word width: column II – average power supply current with only one chip selected; column III – average power supply current under worst case conditions of alternately selecting two chips; and column V – worst case average current including refresh (assuming a 635 ns cycle time). The peak current during refresh, assuming all chips are refreshed at the same time, is equal to the total number of chips multiplied by 20 mA maximum per chip. During an interval of 2.0 ms, the memory will cycle almost 3,000 times, of which only 32 cycles must be devoted to refresh; therefore, the average refresh power will be one percent of the peak power or 0.2 mA per chip. Comparable savings in clock driver power dissipation are also realized.

Using the data from Table I for a common application, such as an 8k-by-16 memory for a minicomputer, the power is cut to half that required without decoding. In a large memory, such as 64k words, the power is cut by a factor

TABLE I.

NUMBER OF WORDS	CHIPS PER BIT OF WORD WIDTH	MAXIMUM POWER SUPPLY CURRENT (mA)/PER BIT OF WORD WIDTH					
		I NO CLOCK DECODING	II CLOCK DECODING ONE CHIP SELECTED	III CLOCK DECODING TWO CHIPS ALTERNATELY SELECTED	IV ADDITIONAL AVERAGE REFRESH CURRENT	V NS TOTAL WORST CASE	6003 (4 mA STANDBY CURRENT)
2,048	1.0	20				20	10
4,096	2.0	40	20.1	40	0	40	20
8,192	4.0	80	20.3	40.2	0.4	40.6	28.2
16,384	8.0	160	20.7	40.6	1.2	41.8	44.6
32,768	16	320	21.5	41.4	2.8	44.2	77.4
65,536	32	640	23.1	43	6.0	49	143
131,072	64	1,280	26.3	46.2	12.4	58.6	274

N = Number of words in 2048 increments N $\geq$ 4096
B = Number of bits/words
t_{CYCLE} = Memory cycle time

$$\underbrace{I_{DD}\,(AVG)_{MAX}}_{V} = B\Bigg\{\underbrace{2 \times 20 + \left(\frac{N}{2048} - 2\right) \times 0.1}_{III} + \underbrace{\left(\frac{N}{2048} - 2\right) \times \frac{32\,t_{CYCLE}}{2\text{ ms}} \times 20}_{IV}\Bigg\}$$

of 13. Figure 1 shows a plot of memory current as a function of memory size with a comparison of the nearest equivalent 2k RAM.

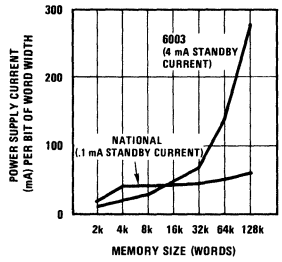


FIGURE 1. Memory Size vs 2k RAM Power Supply Current

A memory system configured as 8k words by 16-bits per word, for example, would draw 80 mA times 16-bits (1.28 Amps) if undecoded. If the same memory is decoded, the current drops to 40.6 mA times 16-bits (650 mA) which is half the current of the undecoded memory. In a large system, such as 64k words by 32-bits per word the savings is even greater. Undecoded the supply current is 640 mA times 32-bits (20.5 Amps) while the same memory when the clocks are decoded draws 49 mA times 32-bits (1.6 Amps). The power for the decoded memory then is one-thirteenth of that required for the undecoded memory.

LOGIC IMPLEMENTATION

Figure 2 shows the logic required to implement the power saving technique, Figure 3 is a timing diagram for the logic, and Figure 4 is a block diagram of an 8k word by 16-bit/word module.

In operation the clock decoder in Figure 2 will supply clock pulses during any cycle in which the chip is selected (Figure 3 – cycle 1 and cycle 6) or when the memory is being refreshed (Figure 3 – cycle 4) and will supply an extra Phase 1 pulse on the first cycle after deselecting the chip (Figure 3 – cycle 2). During all remaining cycles the chip is deselected and no clock pulses are supplied to the chips.

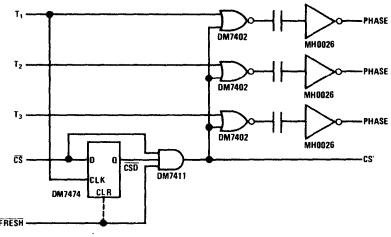


FIGURE 2. MM5262 Clock Decoding Logic

There are three practical considerations to be aware of when using this circuit. First is that, although the power supplies need only be large enough to supply the average current to the memory and its clock drivers, the capacitance bypassing the power supplies should be large enough to supply the peak current during refresh without excessive power supply droop. The second consideration is that if T1 goes to the low state prior to CS or $\overline{\text{REFRESH}}$ going low, the leading edge of Phase 1 will be delayed according to the delay in chip select and T1 pulse width may have to be increased to ensure that the minimum Phase 1 pulse width is supplied to the chip. The third is that if $\overline{\text{REFRESH}}$ goes high after T1 goes low a glitch will be produced on Phase 1. If $\overline{\text{REFRESH}}$ is connected to the clear input of

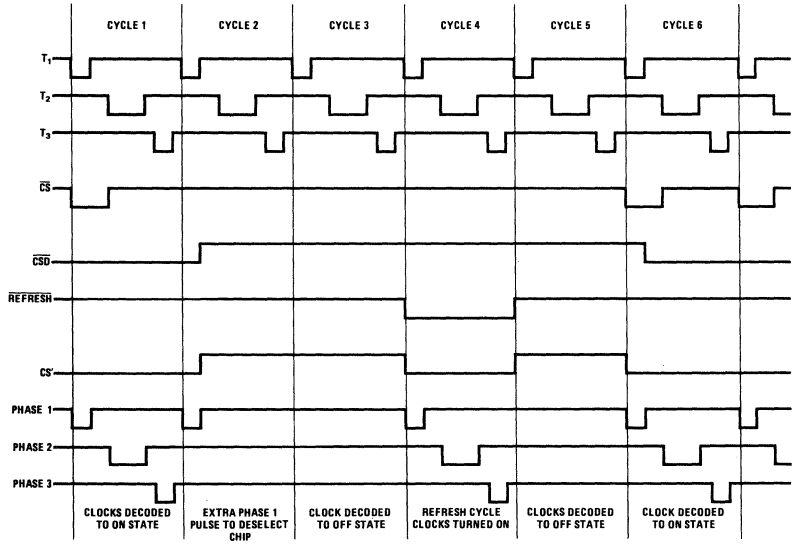


FIGURE 3. MM5262 Clock Decoding Timing Diagram

the DM7474, as shown by the dotted line in Figure 2, the glitch will be extended into a full Phase 1 pulse.

The extra Phase 1 pulse after a refresh cycle will not cause any problems but it will change the value of the refresh current. If refresh is implemented by doing one refresh cycle every 62.4μs, the refresh power will be doubled over what it would be if 32 refresh cycles are done consecutively every 2.0 ms. This is due to the fact that with 32 consecutive refresh cycles the memory receives 33 Phase 1 clocks and with a refresh cycle every 62.4μs the memory receives 64 Phase 1 clocks.

One advantage of connecting $\overline{\text{REFRESH}}$ to the clear input of the DM7474 is that $\overline{\text{REFRESH}}$ is no longer required to be applied for the entire cycle and may return to a one after the positive edge of T1.

It is perhaps of more interest to examine an actual system to determine the effects of clock decoding. As an example a complete 8k-by-16-bit memory has been designed and is shown in Figure 4. This system is not optimized but will serve as a good comparative example. Table II shows power consumption for operating and standby modes with clock decoding and Table III gives power consumption without clock decoding. A comparison between these tables shows a 42% decrease in power consumption by employing clock decoding. Table IV shows various memories mechanized using the basic 8k-by-16 module. Power consumption is given with and without clock decoding for cycle times of 635 ns and 1,000 ns. It is clear from these tables that as memory size increases clock decoding becomes essential. Saying this another way, the ratio of a memory components operating power to standby power is an important parameter for the designer.

TABLE II. Power Consumption of 8k x 16 Module (With t_{CYCLE} = 635 ns and Clock Decoding)

	I_{CC} (mA) @ 5.25V		I_{DD} (mA) @ −16V		I_{BB} (mA) @ 8.75V	
	OPERATING	STANDBY	OPERATING	STANDBY	OPERATING	STANDBY
TTL	1,180	1,180	0	0	0	0
MH0026	124	1.2	111	1.1	0	0
MM5262	699	12.8	650	19.2	8.0	6.5
Total Current	2,003	1,194	761	20.3	8.0	6.5
Total Power (Watts)	10.5	6.3	12.2	0.33	0.07	0.057

Total Operating Power = 10.5 + 12.2 + 0.07 ≅ 22.8 Watts
Total Standby Power = 6.3 + 0.33 + 0.057 = 6.7 Watts

TABLE III. Power Consumption of 8k x 16 Module (With t_{CYCLE} = 635 ns and No Clock Decoding)

	I_{CC} (mA) @ 5.25V	I_{DD} (mA) @ −16V	I_{BB} (mA) @ 8.75V
	OPERATING	OPERATING	OPERATING
TTL	1,180	0	0
MH0026	241	231	0
MM5262	1,333	1,290	9.6
Total Current	2,754	1,521	9.6
Total Power (Watts)	14.4	24.4	0.875

Total Operating Power = 14.4 + 24.4 + 0.875 ≅ 39.3 Watts

TABLE IV. Power Consumption of Larger Memory Systems Using Multiple 8k x 16 Modules

MEMORY SIZE	NUMBER OF CARDS	TOTAL POWER (Watts) t_{CYCLE} = 635 ns		TOTAL POWER (Watts) t_{CYCLE} = 1,000 ns	
		CLOCK DECODING	NO CLOCK DECODING	CLOCK DECODING	NO CLOCK DECODING
8k x 16	1	22.8	39.3	16.9	25.8
8k x 32	2	45.6	78.6	33.8	51.6
16k x 16	2	29.5	78.6	23.5	51.6
16k x 32	4	59	157.2	47	103.2
32k x 16	4	42.9	157.2	36.7	103.2
32k x 32	8	85.8	314.4	73.4	206.4

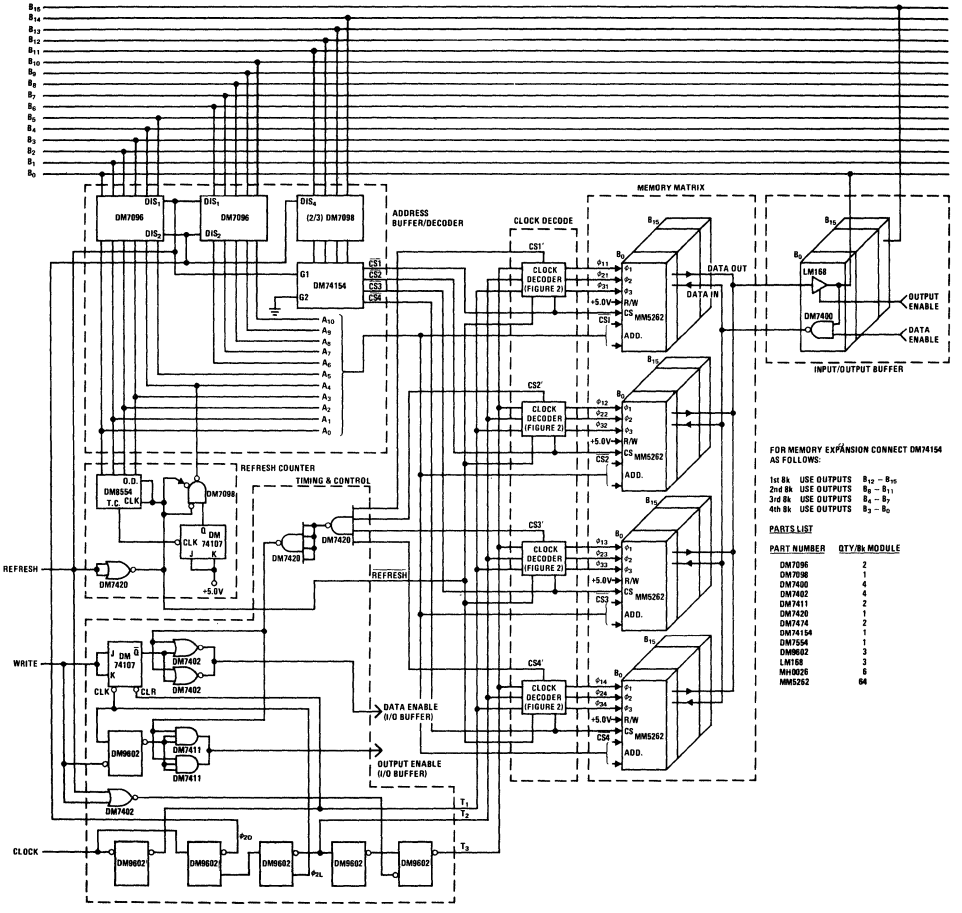


FIGURE 4. 8k x 16 Memory Module

CUSTOM ROM PROGRAMMING

INTRODUCTION

Custom ROM programs are submitted to National in three formats: paper tape, punched cards or truth table with punched cards being the preferred. These programs are converted into machine language and outputted on a magnetic tape. This magnetic tape is used to make the programmable gate mask and the test tape. Wafers are held in inventory at gate mask. The wafers are then completed using the custom gate mask and tested at the wafer level. The wafer is then scribed and the good dice assembled. After assembly the units are tested using the custom test tape to assure the correct output pattern for every address.

When MOS was in its infancy the design engineers called a logic ONE a low voltage because a P-channel MOS transistor is turned on with a negative bias applied. This became known as NEGATIVE logic and was the opposite of TTL's POSITIVE logic. As the MOS technology evolved and TTL compatibility became a reality it became desirous to use the same logic in MOS as in TTL. Therefore the first ROMs to come out were specified in NEGATIVE logic and the new ROMs are specified in POSITIVE logic. Extra care must be taken in entering ROM codes that it is clear which logic level is used. National has programs to convert NEGATIVE logic to POSITIVE or POSITIVE to NEGATIVE so ROMs can be entered in either logic but the customer must specify which logic it is.

DEFINITIONS

Logic Definitions

NEGATIVE Logic: "0" = V_H = the more positive voltage. "1" = V_L = the more negative voltage.

POSITIVE Logic: "0" = V_L = the more negative voltage. "1" = V_H = the more positive voltage.

Input Output Definitions

Address: A_1 is the least significant input address on ROMs. L_0 is the least significant input address on character generators.

Outputs: B_1 is the least significant output.

INFORMATION NEEDED

So that National can better serve its customers the following information *must* be submitted with each ROM code.

National Semiconductor Corporation
2900 Semiconductor Dr., Santa Clara, CA 95051
Phone (408) 732-500 TWX 910-339-9240

				NATIONAL PART NUMBER
				ROM LETTER CODE (NATIONAL USE ONLY)
NAME				DATE
ADDRESS				CUSTOMER PRINT OR I.D. NO.
CITY		STATE	ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE		DATE

TRUTH TABLE FORMS

Use the appropriate form for submitting truth tables.

Form I

MM3501	MM5204	MM4214/MM5214	MM4231/MM5231
MM5201	MM4210/MM5210	MM4220/MM5220	MM4232/MM5232
MM5202	MM4211/MM5211	MM4221/MM5221	MM4233/MM5233
MM4203/MM5203	MM4213/MM5213	MM4230/MM5230	

ADD-RESS	OUTPUT CODE NOTE: 1 B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ __0									
__ __1									
__ __2									
__ __3									
__ __4									
__ __5									
__ __6									
__ __7									
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__ 43									
__ 44									
__ 45									
__ 46									
__ 47									
__ 48									
__ 49									
TB									

ADD-RESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ 50									
__ 51									
__ 52									
__ 53									
__ 54									
__ 55									
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__ 57									
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__ 97									
__ 98									
__ 99									
TB									

Note 1: The Appropriate Logic Level box must be checked or order will *not* be accepted.
- ☐ POSITIVE Logic on Addresses and Outputs
- ☐ NEGATIVE Logic on Addresses and Outputs

Note 2: The MM4232/MM5232 and MM4233/MM5233 have programmable chip selects and the logic level to enable the chip must be specified. CS 1 __ CS 2 __ CS 3 __ CS 4__

Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

Form II

MM5212
MM5215
MM4229/MM5229 (Positive logic only)

ADDRESS	OUTPUT CODE NOTE: 1 B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ __ 0													
__ __ 1													
__ __ 2													
__ __ 3													
__ __ 4													
__ __ 5													
__ __ 6													
__ __ 7													
__ __ 8													
__ __ 9													
__ 10													
__ 11													
__ 12													
__ 13													
__ 14													
__ 15													
__ 16													
__ 17													
__ 18													
__ 19													
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__ 35													
__ 36													
__ 37													
__ 38													
__ 39													
__ 40													
__ 41													
__ 42													
__ 43													
__ 44													
__ 45													
__ 46													
__ 47													
__ 48													
__ 49													
TB													

ADDRESS	OUTPUT CODE NOTE: 1 B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ 50													
__ 51													
__ 52													
__ 53													
__ 54													
__ 55													
__ 56													
__ 57													
__ 58													
__ 59													
__ 60													
__ 61													
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__ 87													
__ 88													
__ 89													
__ 90													
__ 91													
__ 92													
__ 93													
__ 94													
__ 95													
__ 96													
__ 97													
__ 98													
__ 99													
TB													

Note 1: The Appropriate Logic Level box must be checked or order will *not* be accepted.
- ☐ POSITIVE Logic on Address and Outputs
- ☐ NEGATIVE Logic on Address and Outputs

Note 2: The MM4229/MM5229 has programmable chip selects. Specify the Logic Level to enable the Chip (Positive Logic)
CS 1 ___ CS 2 ___ CS 3 ___

Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

Form III

MM4240/MM5240

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS (DECIMAL)	OUTPUT WORD B_1	B_2	B_3	B_4	B_5	SUM
_0	0 ($L_2L_1L_0$ 000)						
	1 (001)						
	2 (010)						
	3 (011)						
	4 (100)						
	5 (110)						
	6 (110)						
	7 (111)						
_1	0 (000)						
	1 (001)						
	2 (010)						
	3 (011)						
	4 (100)						
	5 (110)						
	6 (110)						
	7 (111)						
_2	0 (000)						
	1 (001)						
	2 (010)						
	3 (011)						
	4 (100)						
	5 (110)						
	6 (110)						
	7 (111)						
_3	0 (000)						
	1 (001)						
	2 (010)						
	3 (011)						
	4 (100)						
	5 (110)						
	6 (110)						
	7 (111)						
	TB						

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS (DECIMAL)	OUTPUT WORD B_1	B_2	B_3	B_4	B_5	SUM
_4	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
_5	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
_6	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
_7	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
	TB						

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS (DECIMAL)	OUTPUT WORD B_1	B_2	B_3	B_4	B_5	SUM
_8	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
_9	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
	TB						

Note 1: A logic "1" = most negative voltage. A logic "0" = most positive voltage.

Note 2: Line address (L_0, L_1, L_2) are the row or column select lines in a character generator application. In a read only memory application, A_5 shall be considered the MSB and L_0 the LSB.

Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

Form IV

MM4241/MM5241

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS DECIMAL	LSB B1	B2	B3	B4	B5	B6	B7	B8	SUM
_0	0 (L_2 L_1 L_0 0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 1 0)									
_1	0 (0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 1 0)									
_2	0 (0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 1 0)									
_3	0 (0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 0 1)									
_4	0									
	1									
	2									
	3									
	4									
	5									
	TB									

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS DECIMAL	LSB B1	B2	B3	B4	B5	B6	B7	B8	SUM
_5	0									
	1									
	2									
	3									
	4									
	5									
_6	0									
	1									
	2									
	3									
	4									
	5									
_7	0									
	1									
	2									
	3									
	4									
	5									
_8	0									
	1									
	2									
	3									
	4									
	5									
_9	0									
	1									
	2									
	3									
	4									
	5									
	TB									

Note 1: On the character address and output word negative logic is used:
A logic "1" most negative voltage
A logic "0" most positive voltage
on the line address positive logic is used:
A logic "0" most negative voltage
A logic "1" most positive voltage

Note 2: Line address (L_0, L_1, L_2) are the column select lines in a character generator application. In a read only memory application A_6 shall be considered the MSB and L_0 the LSB.

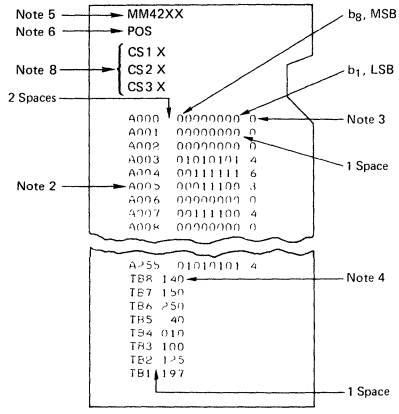
Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

TAPE ENTRY FORMAT

Tape format for the following ROMs.

MM3501	MM4214/MM5214	MM4231/MM5231
MM4210/MM5210	MM4220/MM5220	MM4232/MM5232
MM4211/MM5211	MM4221/MM5221	MM4233/MM5233
MM4213/MM5213	MM4230/MM5230	



8-BIT TAPE FORMAT

Note 1: The code is a 7-bit ASCII code on 8 punch tape.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number if "1" bits in each output column or bit position.

Note 5: Specify product type.

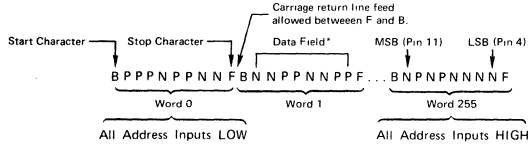
Note 6: Must type POS logic, or NEG logic depending on which is used.

Note 7: LOGIC ON ADDRESS AND OUTPUTS must be the same (either POS or NEG).

Note 8: Specify the pattern necessary to enable the ROM on the ROMS that need chip selects.

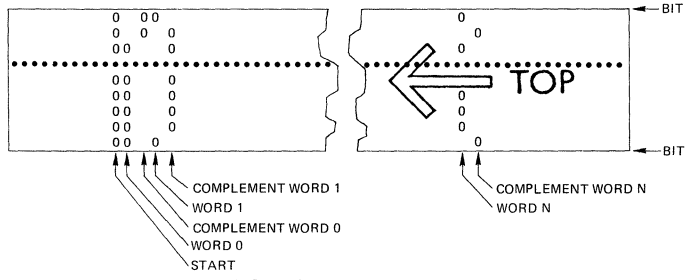
Tape format for the MM5202, MM4203/MM5203 and MM4204/MM5204.

PROM TAPE P AND N FORMAT



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start be rubbed out. Data for exactly 256 words must be entered, beginning with word 0. P = "1" or the more positive voltage. N = "0" or most negative voltage. When the MM4204/MM5204 is used the word length is 512.

PROM TAPE BINARY FORMAT



Note 1: Tape must be all blank except for the 513 words punched.

Note 2: Tape must start with a START punch.

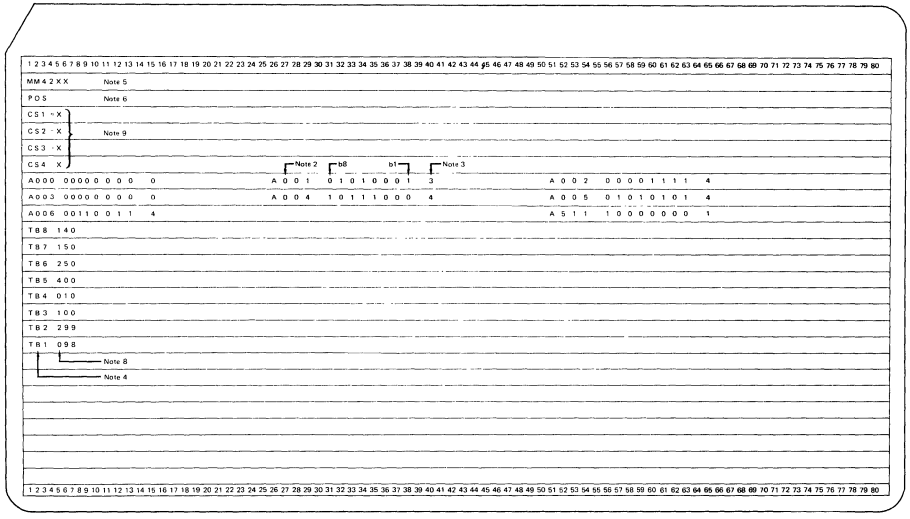
Note 3: Data is comprised of two words the first being the actual Data the second being the complement of the data.

Note 4: A punch is equal to a "1" or most positive voltage and the omission of a punch is a "0" or the more negative voltage.

When programming the MM5202 or MM4203/MM5203 it should be remembered that the opposite logic from what is programmed will appear on the output of the PROM. In otherwords a P on the tape will program a Logic "0" or V_L in the PROM.

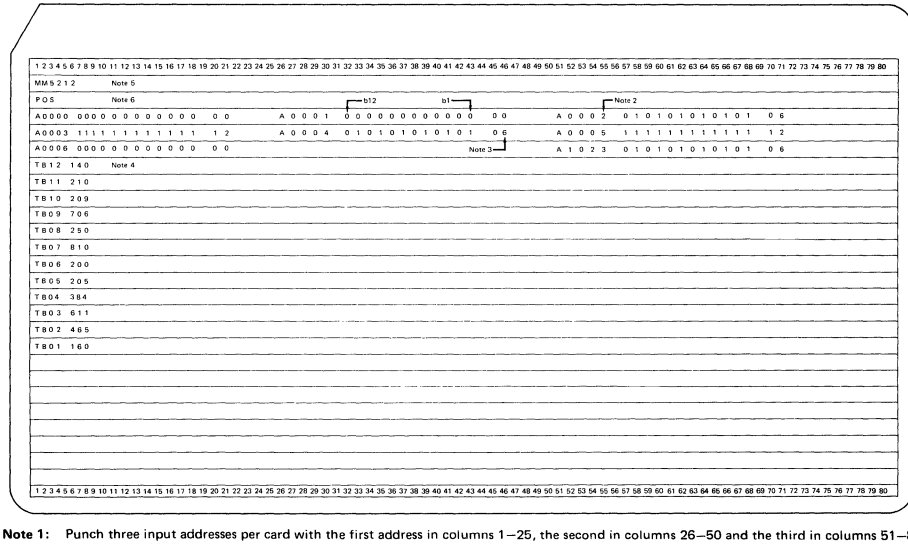
CARD ENTRY FORMAT

Card format for the: MM3501, MM4210/MM5210, MM4211/MM5211, MM4213/MM5213, MM4214/MM5214, MM4220/MM5220, MM4221/MM5221, MM4230/MM5230, MM4231/MM5231, MM4232/MM5232, MM4233/MM5233



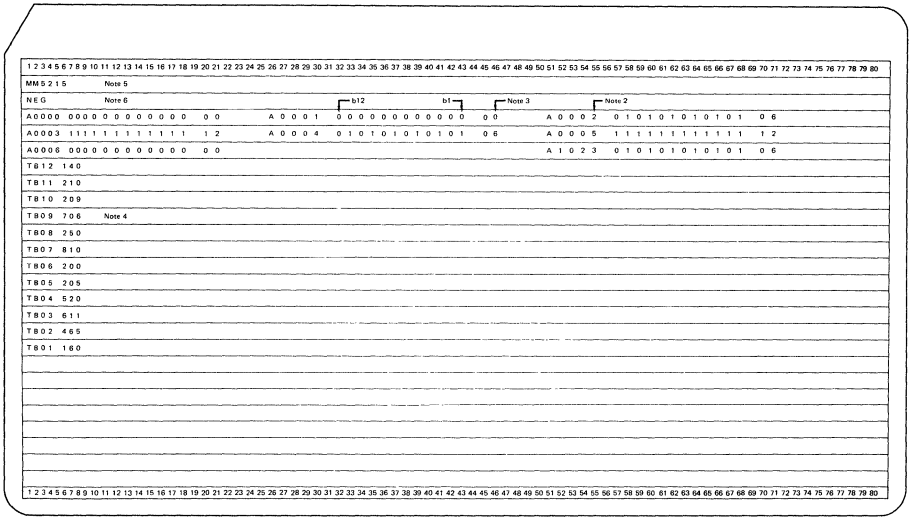
Note 1: Punch three input addresses per card with the first address in columns 1–25, the second in columns 26–50 and the third in columns 51–80.
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 3: The total number of "1" bits in the output word.
Note 4: The total number if "1" bits in each output column or bit position.
Note 5: Specify product type.
Note 6: Must type POS logic or NEG logic depending on which is used.
Note 7: LOGIC ON ADDRESS, OUTPUTS AND CHIP ENABLE must be the same (either POS or NEG).
Note 8: Leading zeros must be punched.
Note 9: Specify the Chip Select Logic Levels that will enable the ROM where necessary.

Card format for the MM5212.



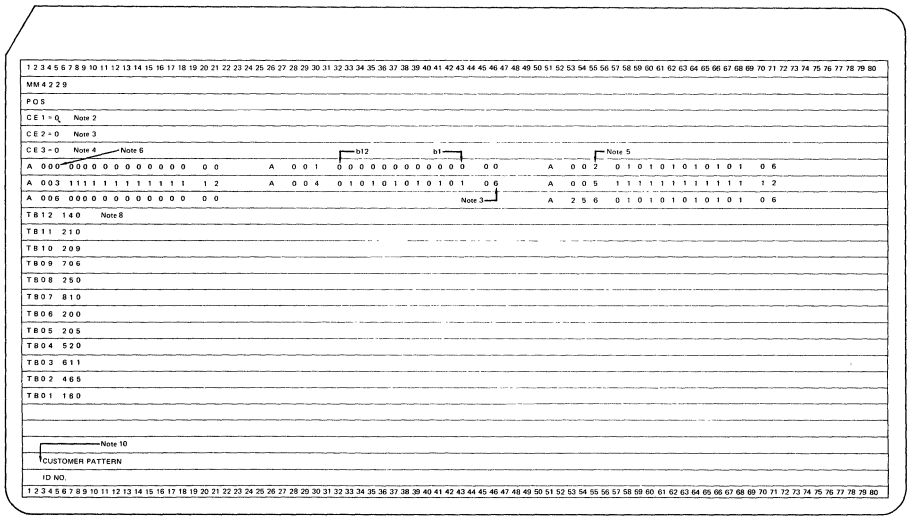
Note 1: Punch three input addresses per card with the first address in columns 1–25, the second in columns 26–50 and the third in columns 51–80.
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 3: The total number of "1" bits in the output word.
Note 4: The total number if "1" bits in each output column or bit position.
Note 5: Specify product type.
Note 6: Must type POS logic.
Note 7: POSITIVE LOGIC ON ADDRESS AND OUTPUTS.
Note 8: "1" more positive output. "0" more negative output.
Note 9: Leading zeroes must be punched.

Card format for the MM5215.



Note 1: Punch three input addresses per card with the first in columns 1–25, the second in columns 26–50, and the third in columns 51–80.
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 3: The total number of "1" bits in the output word.
Note 4: The total number if "1" bits in each output column or bit position.
Note 5: Specify product type.
Note 6: Must type negative logic.
Note 7: NEGATIVE LOGIC ON ADDRESS AND OUTPUTS.
Note 8: "1" more negative output, "0" more positive output.
Note 9: Leading zeroes must be punched.

Card format for the MM4229/MM5229.



Note 1: The code is Hollerith as punched on IBM Model 029.
Note 2: Corresponds to Pin 16
Note 3: Corresponds to Pin 15
Note 4: Corresponds to Pin 14
Note 5: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 6: All 256 address (0–255) must be coded.
Note 7: The total number of "1's" in each input word.
Note 8: The total number of "1's" in each output column.
Note 9: Leading zeros must be punched.
Note 10: The customer may use his own ID designation if he does not punch the first column.
Note 11: Positive logic on address and outputs "1" more positive voltage "0" more negative voltage.

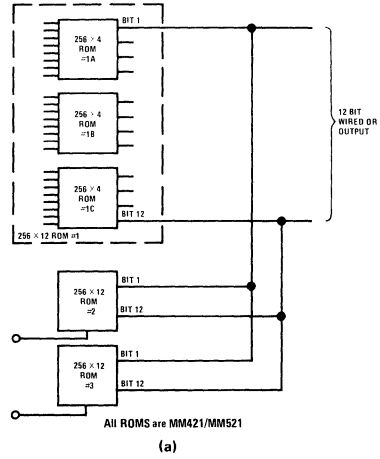
TRIG FUNCTION GENERATORS

Accuracy is the major design variable of trigonometric lookup tables built with MOS read-only memories. Only a few ROMs are needed for most practical applications, but accuracy can be made to increase very rapidly with memory capacity if interpolation techniques are used.

For instance, without interpolation a single 1024-bit ROM can store 128 angular increments and generate an 8-bit output that will be better than 99.9% of the handbook value (Table 1).

ADDRESS	DEGREES	BINARY OUTPUT	DECIMAL SINE
0	0	.00000000	0.000
1	0.7	.00000011	0.012
2	1.4	.00000110	0.023
3	2.1	.00001001	0.035
.			
.			
.			
127	89.3	.11111111	0.996

TABLE 1. MM422BM/MM522BM Sine Function Generator



(a)

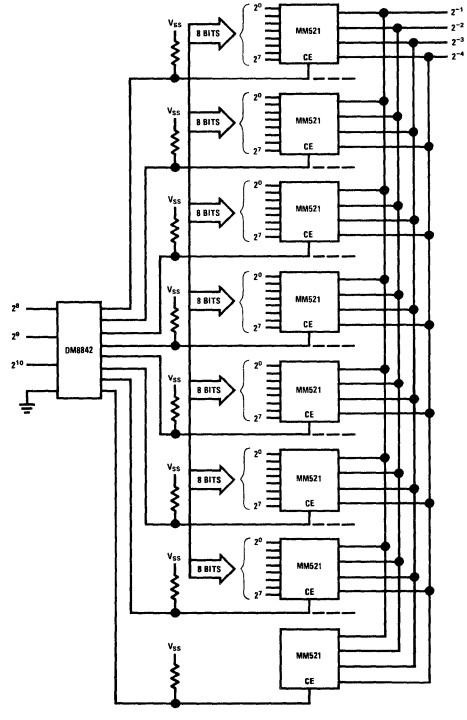
If one simply cascaded ROMs to improve input resolution and output accuracy for a high-accuracy trig solution (X=sin θ) as in Figure 1, large numbers of ROMs might be needed. This 24-ROM system stores 2048 12-bit values of sin x (or other trig functions), giving angular resolution of 1 part in 2^{11} (0.05%) and output accuracy of 1 part in 2^{12} (0.024%). The system in Figure 2 has the same resolution and is accurate to the limit of its 12 output bits (0.024%), which makes it just as good. But it only requires four 1024-bit ROMs and three 4-bit TTL full adders, so it only costs about one-fifth as much as the more obvious solution of Figure 1.

Instead of producing x = sin θ, the Figure 2 system divides the angle into two parts and implements the equation

$$x = \sin\theta = \sin(M + L)$$
$$= \sin M \cos L + \cos M \sin L$$

It can be programmed for any angular range. Assume the range is 0 to 90 degrees and let M be the 8 most significant bits of θ and L be the 3 least significant bits of θ (θ being the 11-bit input angular increments, equal to 90°/2048, or 0.044 deg.) as in Table 2.

With an 8-bit address, the three 256x4 ROMs will give the 12-bit value of sin M at increments of M = 90°/2^8, or 0.352 deg. The cos L can only vary between 1 and 0.99998. So we assume cos L=1 and store values of sin M at 0.352 deg. resolution



(b)

FIGURE 1. Conventional 2048-Increment Sine Table Uses 24 ROMs

in the top three ROMs, reducing the equation to

$$\sin\theta = \sin M + \cos M \sin L$$

Values of the second term are stored in the fourth ROM. The maximum value of the second term in the above equation can only be cos Msin L = 0.00539 where cos M_{max} = 1, sin L_{max} = 0.00539. This is the maximum value to be added to sin M above. Only the five least significant bits of a 12-bit output are needed to form the maximum output, so an MM522 is used in its 128x8 configuration.

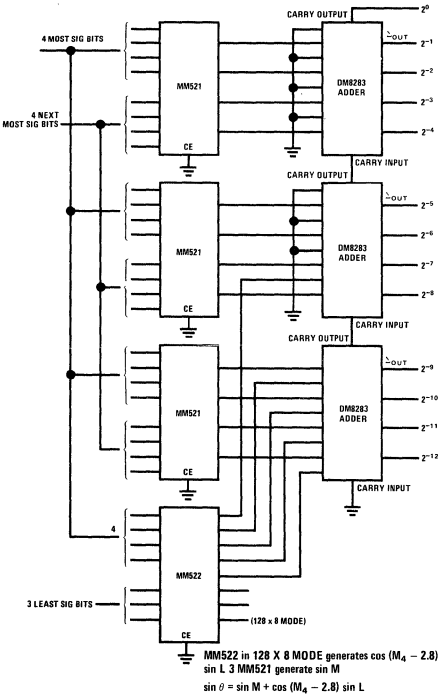


FIGURE 2. Four-ROM Lookup Table Generates 2048 Values of Sin x by Interpolation Technique.

Let the 4 most significant bits of M be called M_4 and the angle at these increments be $X_m = 90°/2^4$ = 5.63 deg. Sin L (the 3 least significant bits of θ) has the same maximum as before and cos M_4 has a maximum of cos 5.63 deg. = 0.99517, and continuing as follows:

$$\cos(11.26) = 0.98076$$

$$\cos(16.89) = 0.95686$$

$$\cos(84.37) = 0.09810$$

through the 16 increments of M_4. Now

$$\sin\theta = \sin M + \cos M_4 \sin L$$

and the appropriate cos M sin L values are stored in the fourth ROM. In effect, we have divided the 0° to 90° sine curve into 16 slope sectors with M_4, each sector into 16 subsections with M, and each subsection into 8 interpolation segments with L.

Since we are using an approximation, accuracy is not quite as good as the Figure 1 system. The additional error term is cos L, assumed 1 but actually is a variable between 1 and 0.99998. At every eighth increment, L is zero, making cos M

ADDRESS	M			L	
	M_4				
0					0
1					1
2				1	0
3				1	1
4				1	0 0
5				1	0 1
6				1	1 0
7				1	1 1
8			1	0	0 0
9			1	0	0 1
16			1 0	0	0 0
32			1 0 0	0	0 0
64			1 0 0 0	0	0 0
128		1	0 0 0 0	0	0 0
256		1 0	0 0 0 0	0	0 0
512		1 0 0	0 0 0 0	0	0 0
1024		1 0 0 0	0 0 0 0	0	0 0
2048-1		1 1 1 1	1 1 1 1	1	1 1

L = 0.044°

M = 0.352°

M_4 = 5.63°

TABLE 2. Programming of 2048-Increment Sine Table

sin L=0, and sin x=sin M to 12-bit accuracy. Then the error rises to a limit of near 0.002% at every eighth increment where L is 0.352–0.044. This error can be halved by adjusting the fourth ROM's output so that

$$\sin\theta = \sin M + \cos(M - 2.81°) \sin L$$

If five ROMs are used—four MM521's and all eight outputs of the MM522—15-bit accuracy can be achieved, and thus improving the accuracy by a factor of eight. The resolution could also be smaller, of course, if the angular range were smaller as in an application involving a sensor with a limited field of view. Variations of the system could be used to space the increments irregularly to compensate for sensor nonlinearities, to improve accuracy in specific angular ranges.

This example has a binary fraction output, like the sine function generator in Table 1. For instance, the 8-bit output at the 64th increment representing sin x = sin 45° is 10110101. This equals $1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} + 0 \times 2^{-5} + 1 \times 2^{-6} + 0 \times 2^{-7} + 1 \times 2^{-8}$, which reduces to 181/256 or 0.7070. Handbooks give the four-place sine of 45° as 0.7071, so at this increment the output is accurate to approximately 0.01%. This table, the MM422BM/MM522BM, is used in fast Fourier transform, radar, and other signal-processing applications.

Other standard tables that are available off the shelf include an arctan generator, several code generators (EBCDIC to ASCII, BCD to Selectric, and Selectric to BCD) and ASCII-addressed character generators for electronic, electrical and electromechanical display and printout systems. All interface with TTL logic and operate off 12-volt power supplies. Write for data sheets, or use one of our programming tables to jot down any special input-output logic functions you need.

MASK PROGRAMMING SPECIALIZES MOS SHIFT REGISTER DESIGNS

A quick, economical way of customizing MOS shift register bit lengths is programming the metallization mask, the mask that defines the thin-film wiring pattern etched on the silicon wafer. Metallization etching is the most convenient process step to specialize because it is consistent from wafer to wafer and is the last major process step before testing.

Utilizing this technique, National Semiconductor has developed two variable-length dynamic MOS register designs. Both of them, MM4007/MM5007 and MM4019/MM5019, are bipolar compatible. Dual registers 20 to 256 bits long, single registers 40 to 512 bits long, and a variety of taps and pinouts provide the system designer with a method of obtaining custom length shift registers quickly and at reasonable cost.

Up to metal masking, wafer design and fabrication are standardized. No time is lost—or money spent—in developing custom arrays or tuning up the process. Automatic test systems further reduce turnaround time and production costs.

Programming the metallization mask mainly involves routing signal connections past selected storage cells to adjust total register length to the desired number of cells. Wire-bonding changes provide output tap options.

DUAL REGISTER DESIGNS

Basically, each of the variable-length types is a dual register (Figure 1 and Table 1A).

There are enough storage cells, I/O stages, clock and power supply lines on each MM4007 chip to make up to two 100-bit registers. The minimum length of each register half, M_A and M_B, is 20 bits. The programmable parts, P_A and P_B, may be 0 to 80 bits long. Lengths need not be equal. For instance, register A may be 29 bits and register B 76 bits (P_A = 9, P_B = 56).

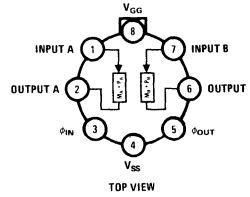


FIGURE 1. Dual Shift Registers

An MM4019/MM5019 chip is similarly organized, except that M_A and M_B are 40 bits and P_A and P_B vary from 0 to 216 bits. Again, lengths may be unequal, such as 240 bits in the A half and 136 bits in the B half.

Clock and supply line pin locations are standardized, but I/O pinouts are selectable. The I/O terminals on the chip may be bonded to package pins which are more convenient for the PC board layout. For example, a couple of board feedthroughs might be eliminated by bonding the A register input to Pin 7 (rather than Pin 1) if data comes in from the right and exits on the left. Or, A and B could share an input pin when they have the same signal source.

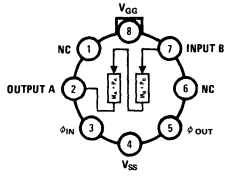
TABLE 1 Register Length Options

	MM4007/MM5007			MM4019/MM5019		
	M (BITS)	P (BITS)	TOTAL (BITS)	M (BITS)	P (BITS)	TOTAL (BITS)
A. DUAL REGISTERS						
A Register	20	0 to 80	20 to 100	40	0 to 216	40 to 256
B Register	20	0 to 80	20 to 100	40	0 to 216	40 to 256
B. SINGLE REGISTERS	$M_A + M_B$	$P_A + P_B$		$M_A + M_B$	$P_A + P_B$	
	40	0 to 160	40 to 200	80	0 to 432	80 to 512
C. TAPPED SINGLE REGISTERS Total register length same as single registers with tap locations determined by either half of the dual registers.						

SINGLE-REGISTER OPTIONS

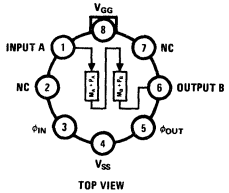
Since clock rates are synchronized by the common clock inputs, the registers may also be serially connected inside the package, as diagrammed in Figure 2. One output is internally connected to the other input.

This extends the maximum length of an MM4007/MM5007 to 200 bits and the MM4019/MM5019 maximum to 512 bits. However, each half still has the same minimum, so the minimums become 40 and 80 bits, respectively (Table 1B). Again, the customer specifies the most convenient I/O pin connections.



TOP VIEW

FIGURE 2a

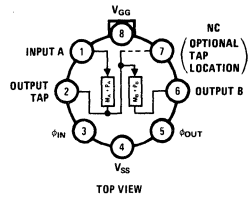


TOP VIEW

FIGURE 2b

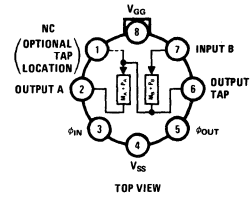
FIGURE 2. Single Registers

Going to the output tap designs of Figure 3 takes only one more wire bond; from the first register output to any available pin. Tap locations are selected by specifying the bit lengths of each of the dual registers. For example, an MM5007 105 bits long may be tapped at any stage from 20 to 85 bits. Generally, this flexibility makes input taps unnecessary—an output at 29 bits in a 105-bit register usually serves the same purpose as an input at 76 bits.



TOP VIEW

FIGURE 3a



TOP VIEW

FIGURE 3b

FIGURE 3. Output Tap Options

OPERATING CHARACTERISTICS

All specifications, except bit lengths, are the same as those of other MM4000/MM5000 series dynamic shift registers with the same number of I/O stages.

Clock-line capacitance, power dissipation, as well as other AC and DC parameters, are independent of the lengths programmed. This is accomplished by standardizing clock and supply wiring patterns to achieve minimum turnaround time and cost.

The MM4007/MM5007 and MM4019/MM5019 are fabricated using a low-threshold, p-channel enhancement-mode technology developed for the MM4000/MM5000 series of registers. This means that they are bipolar compatible, sensing TTL or DTL data without input pull-up resistors and driving TTL or DTL loads without output pull-down resistors. They operate on standard +5V and −12V supplies. The clock frequency range is also the same, from 300 Hz to 2.5 MHz, guaranteed.

Either TO-99 or dual-in-line packages may be specified. MM4007 and MM4019 operate at −55°C to +125°C. MM5007 and MM5019 are commerical types, specified for −25°C to +70°C.

DOUBLE-CLOCKING CUTS STANDARD REGISTERS TO NON-STANDARD SIZES

INTRODUCTION

It may be more economical to make a standard MOS register appear shorter, logically, than to have a special register made to order. A double-clocking technique uses up the unwanted length by causing input bits to be stored twice and then to be read out as individual bits when they reach the end of the register.

Figure 1 shows the clock format. A double clock applied for N of the normal input data intervals at a fixed portion of the total recirculation time

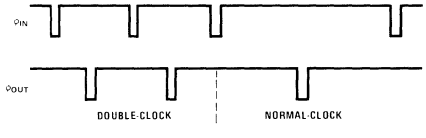


FIGURE 1. Clock rate is doubled for N data input periods to make the register appear shorter by N bits, and then resumes normal frequency.

will shorten the register by N stages and clock periods. If N is 2, a 1-0 input data sequence would be stored as 1-1-0-0. Since these appear as the output at the time the clock is again doubled, the output gate only detects 1-0.

Suppose a parallel array of eight 1991-bit registers is needed to store 1991 8-bit words in a buffer memory. Each could be a subassembly as in Figure 2. The MM5013 and MM5016 are standard 1024-bit and 512-bit register and the MM5019 is mask-programmed to order in sizes up to single 512 or dual 256-bits.

The design in Figure 3 provides the same length with two MM5013 registers. The eight registers are assembled with 16 instead of 24 packages.

Also, the second MM5013 costs less than an MM5016/MM5019 combination (the longer the register the less the cost per bit). The only addition to overhead logic is the decoder and dual clock generator formed with the logic in the dotted lines—one DM7473 dual J-K flip-flop and half a package each of DM7400 and DM7420 gates.

In the example, N = 2048 − 1991, or 57. Therefore, the registers should be clocked at double frequency for the first 57 data periods of the recirculation time. The extra logic decodes the bit-counter output and generates the 114 clocks needed.

There are some limitations to this technique. Obviously, the normal rate should not be more than half the maximum clock rate for the registers

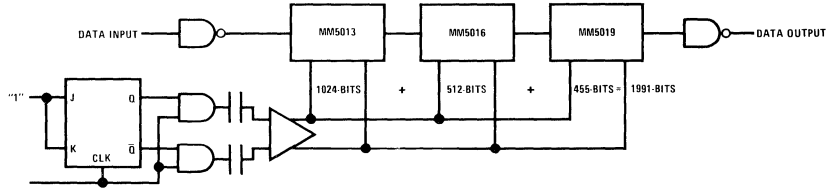


FIGURE 2. Mask-programmable MM5019 register may be used to assemble odd-length registers.

used. Also, if too many bits are subtracted, the clock-drive loading may be affected adversely. The driver power requirement is proportional to average frequency. In the example, it is increased by f(2048/1991) or 2.8%, which has little effect. But if an MM5016 was shortened from 512 to 397 bits, the increase in power would be 28%. In this case, instead of shortening the MM5016, it may be more practical to order an MM5019 at the desired length. At still shorter lengths, the MM5007 mask-programmable dual 100-bit programmable register should be considered. Generally speaking, double-clocking becomes more cost-effective when the system register length is long.

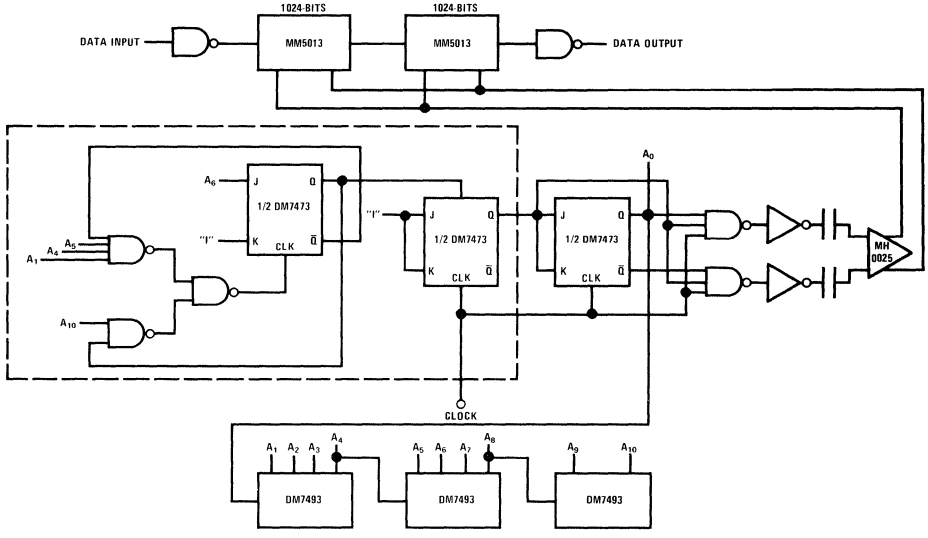


FIGURE 3. A 2048-bit register is made to appear only 1991 bits long by the logic within the dotted lines.

Definition of Terms

Clock Repetition Rate: The range of clock frequencies for which register operation is guaranteed.

Clock Frequency ϕ_f: The range of clock frequencies which register operation is guaranteed. Maximum clock frequencies are dependent upon minimum and maximum clock pulse width restrictions, as presented by the Guaranteed Operating Curves.

Clock Delay ϕ_d: ϕ_d is defined to be that minimum amount of time that must expire after ϕ_1 has undergone a $V_{\phi L}$ to $V_{\phi H}$ transition and the start of a ϕ_2 $V_{\phi H}$ to $V_{\phi L}$ transition. The same spacings apply, when ϕ_2 preceeds ϕ_1.

Clock Phase Delay ϕ_d, $\overline{\phi}_d$: The time between the $V_{\phi H}$ levels of ϕ_{IN} and ϕ_{OUT}. ϕ_d is the time between the trailing edge of ϕ_{IN} and the leading edge of ϕ_{OUT}. $\overline{\phi}_d$ is the time between the trailing edge of ϕ_{OUT} and the leading edge of ϕ_{IN}.

Clock Pulse Risetime, $t_{r\phi}$: The time delay between the 10% and 90% voltage points on the clock pulse as it traverses between its logic $V_{\phi L}$ and logic $V_{\phi H}$ levels.

Clock Pulse Falltime, $t_{f\phi}$: The time delay between the 10% to 90% voltage points on the clock pulse as it traverses between its logic $V_{\phi H}$ and logic $V_{\phi L}$ levels.

Clock Pulse Width, ϕ_{PW}: The duration of time that the clock pulse is greater than 1.5V.

Clock Input Levels: The voltage levels (logic $V_{\phi L}$ or $V_{\phi H}$) which the clock driver must assume to insure proper device operation.

Clock Control Setup Time, t_{cs}: The time prior to the clock Low to High transition at which the clock control must be at its desired logic level.

Clock Control Hold Time, t_{ch}: The time after the High to Low transition for which the clock control must be held at its desired logic level.

Data Setup Time, t_{ds}: The time prior to the clock High to Low transition at which the data input level must be present to guarantee being clocked into the register by that clock pulse.

Data Pulse Width, t_{dw}: The time during which the data pulse is in its V_{IH} or V_{IL} state.

Data Hold Time, t_{dh}: The time after the clock High to Low transition which the data input level must be held to guarantee being clocked into the register by that clock pulse.

Data Input Voltage Levels: The voltage levels (logic V_{IL} or V_{IH}) which the data input terminal must assume to insure proper logic inputs.

Data Output Voltage Levels: The output voltage levels (logic V_{OL} or V_{OH}) which the output will assume under normal operating conditions.

Data Input Capacitance: The capacitance between the data input terminal and ground reference measured at 1 MHz.

Output Resistance to Ground: The resistance between the output terminal and ground with the output in the logic V_{OH} state.

Partial Bit Times T_{IN}, T_{OUT}: The time between leading edges of clocks, measured at the $V_{\phi H}$ levels. T_{IN} is the time between the leading edge of ϕ_{IN} and the leading edge of ϕ_{OUT}. T_{OUT} is the time between the leading edge of ϕ_{OUT} and the leading edge of ϕ_{IN}.

Output Sink Current: The current which flows into the output terminal of the register when the output is a logical low level. Conventional current flow is assumed.

Output Source Current: The current which flows out of the output terminal of the register when the output is a logical High level. Conventional current flow is assumed.

Output Voltage Levels: The logical Low level, V_{OL}, is the more negative level. This is the state in which the output is capable of sinking current. The logical High level, V_{OH}, is the more positive level. This is the state in which the output is capable of sourcing current.

V_{GG} Current Drain: The average current flow out of the V_{GG} terminal of the package with the output open circuited.

Power Supply Voltage, V_{GG}: The negative power supply potential required for proper device operation; referenced to V_{SS}.

Power Supply Return, V_{SS}: The V_{SS} terminal is the reference point for the device. It must always be the most positive potential applied to the device.

V_{SS} Current Drain: The average current flow into the V_{SS} terminal of the package. It is equal to the sum of the I_{GG} and I_{DD} currents.

Power Supply Voltage, V_{DD}: The negative power supply potential required for proper device operation, referenced to V_{SS}.

Clock Input Voltage Levels, $V_{\phi H}$ $V_{\phi L}$: The voltage levels (logic "1" or "0") which the clock driver must assume to insure proper device operation.

Data Output Voltage Levels, V_{OH}, V_{OL}: The output voltage levels (logic "1" or "0") which the output will assume with a specified load connected between output and V_{SS} line.

Data Input Voltage Levels, $V_{IH}V_{IL}$: The voltage levels (logic "1" or "0") which the data input terminal must assume to insure proper logic inputs.

Control Release Time, t_{cr}: The maximum time that a load command signal can be changed prior to the $V_{\phi L}$ to $V_{\phi H}$ transition of the output clock, ϕ_{OUT}, without affecting the data during bit time t_n.

Control Initiate Window: The time in which a load command signal must be applied to affect bit time t_n. This time extends from the start of t_{cr} to the start of t_{cs}.

Control Hold Time: The time that the load command signal must remain stable during t_n bit time. See control timing diagram.

Physical Dimensions

PACKAGES

DUAL-IN-LINE PACKAGES

(N) Devices ordered with "N" suffix are supplied in molded dual-in-line package. Molding material is EPOXY B, a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is Alloy 42 with a hot solder dipped surface to allow for ease of solderability.

(J) Devices ordered with the "J" suffix are supplied in either the 14-pin, 16-pin, or 24-pin ceramic dual-in-line package. The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

(D) Devices ordered with the "D" suffix are supplied in glass/metal dual-in-line package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.

(Q) Devices ordered with the "Q" suffix are supplied in a glass/metal dual-in-line with a quartz cover.

METAL CAN PACKAGES

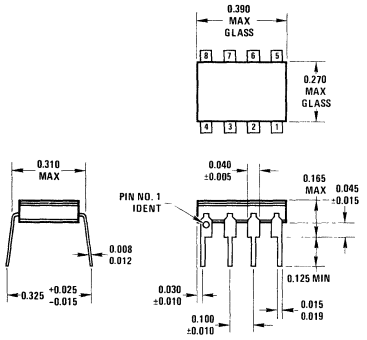
(H) Devices ordered with the "H" suffix are supplied in either 4-pin TO-72 style, 8-pin or 10-pin TO-5 style metal can package. The cap is chrome-plated kovar and the leads are gold-plated kovar.

(G) Devices ordered with the "G" suffix are supplied in a 12-pin TO-8 style metal can package. The cap is chrome-plated kovar and the leads are gold plated kovar.

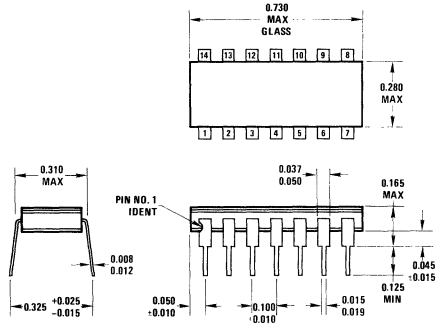
FLAT PACKAGES

(W) Devices ordered with the "W" suffix are supplied in the 14-pin, ceramic flat package. The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

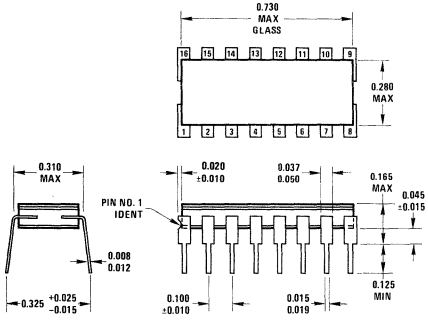
(F) Devices ordered with the "F" suffix are supplied in the 14-pin, glass/metal flat package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.



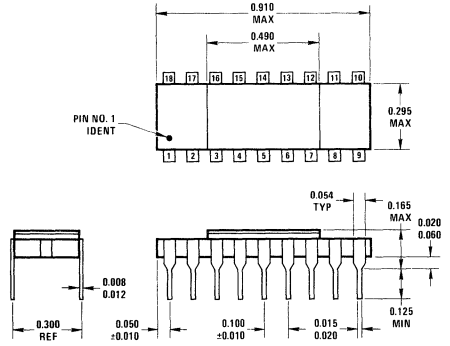
Package 1
8-Lead Cavity DIP (D)



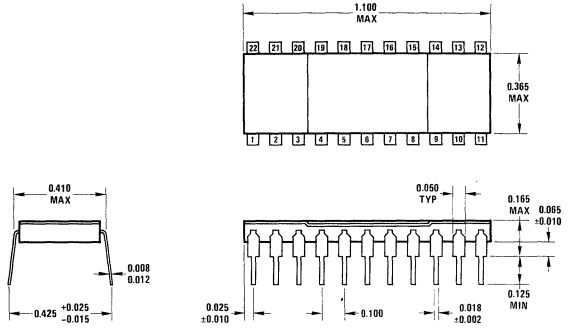
Package 2
14-Lead Cavity DIP (D)



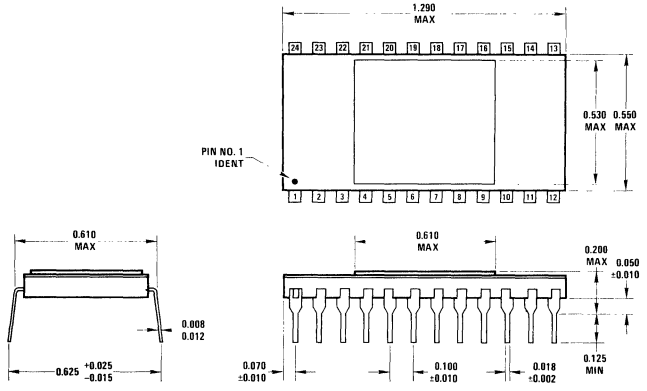
Package 3
16-Lead Cavity DIP (D)



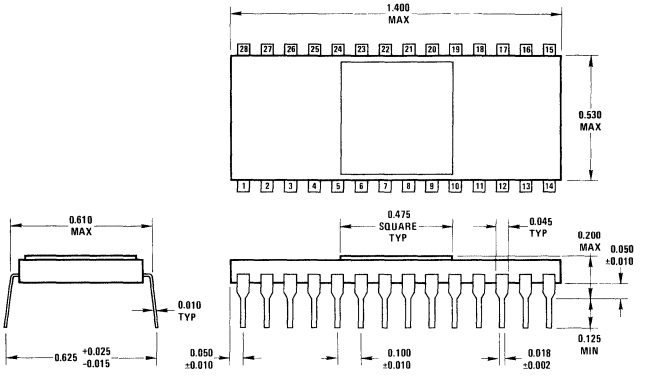
Package 4
18-Lead Cavity DIP (D)



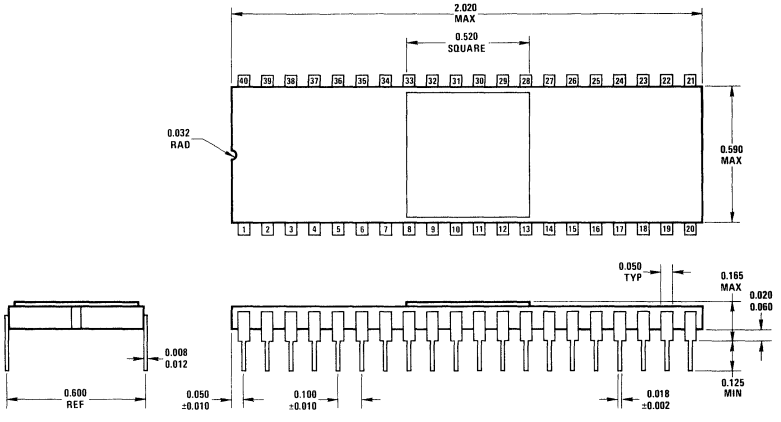
Package 5
22-Lead Cavity DIP (D)



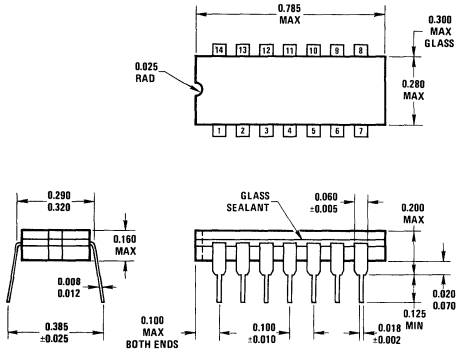
Package 6
24-Lead Cavity DIP (D)



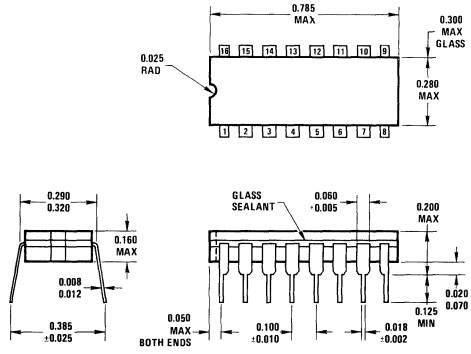
Package 7
28-Lead Cavity DIP (D)



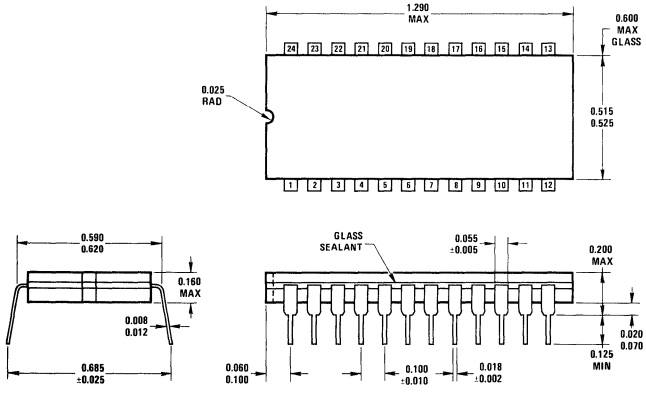
Package 8
40-Lead Cavity DIP (D)



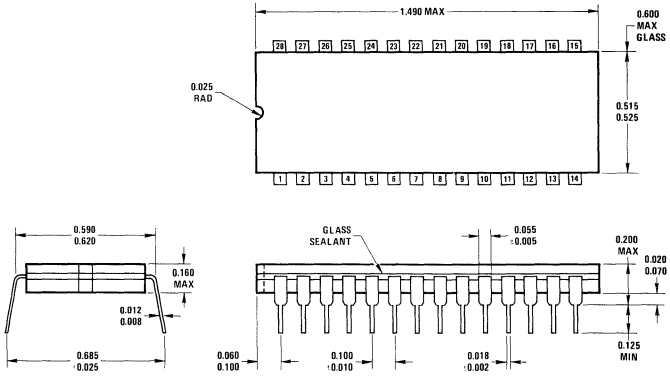
Package 9
14-Lead Cavity DIP (J)



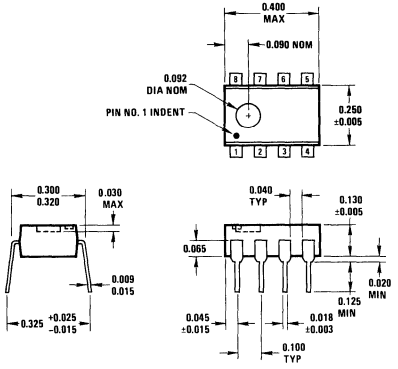
Package 10
16-Lead Cavity DIP (J)



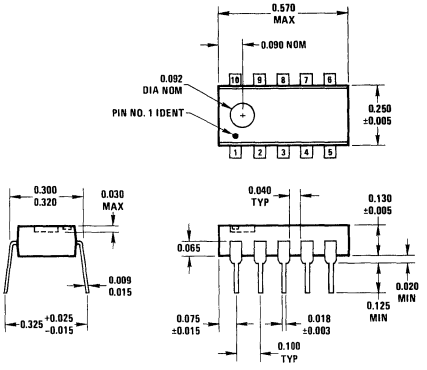
Package 11
24-Lead Cavity DIP (J)



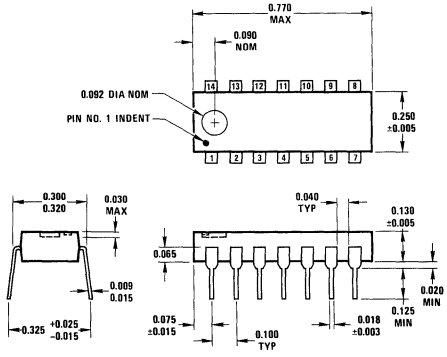
Package 11A
28 Lead Cavity DIP (J)



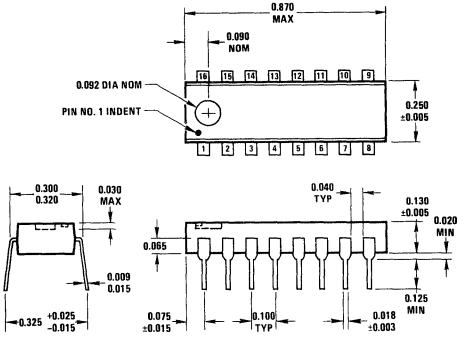
Package 12
8-Lead Molded DIP (N)



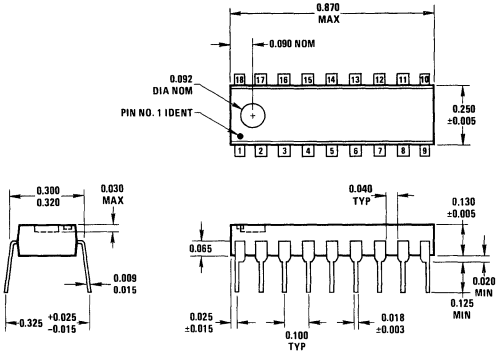
Package 13
10-Lead Molded DIP (N)



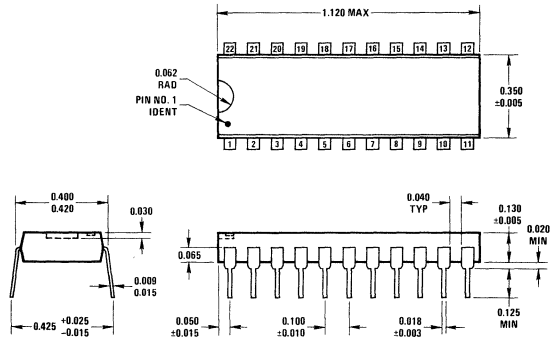
Package 14
14-Lead Molded DIP (N)



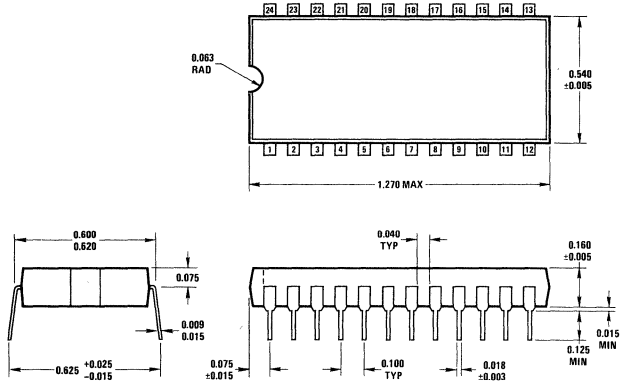
Package 15
16-Lead Molded DIP (N)



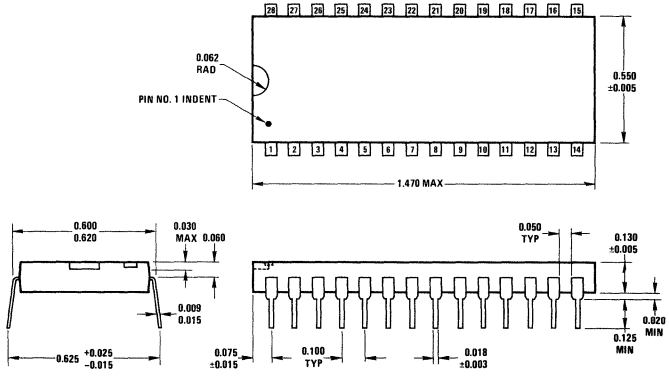
Package 16
18-Lead Molded DIP (N)



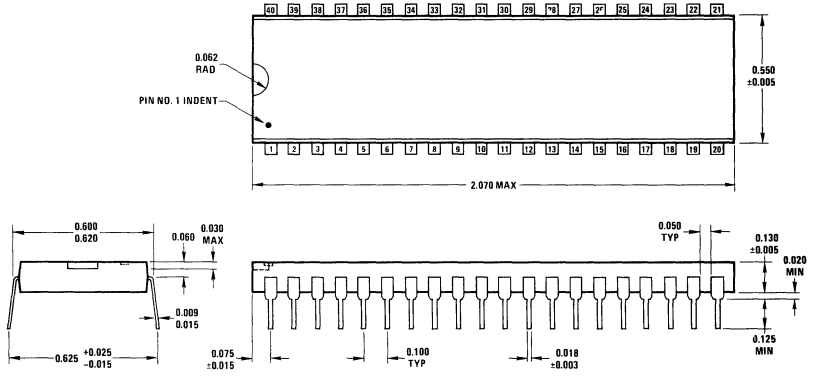
Package 17
22-Lead Molded DIP (N)



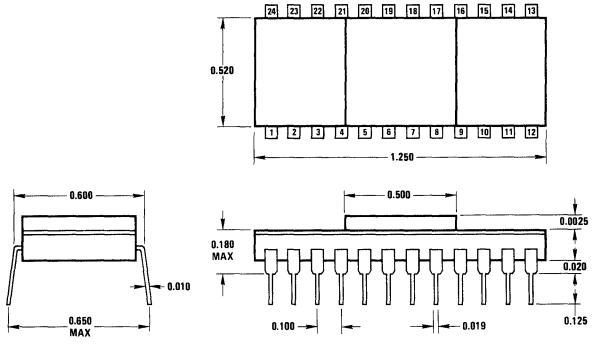
Package 18
24-Lead Molded DIP (N)



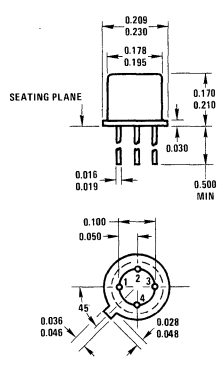
Package 19
28-Lead Molded DIP (N)



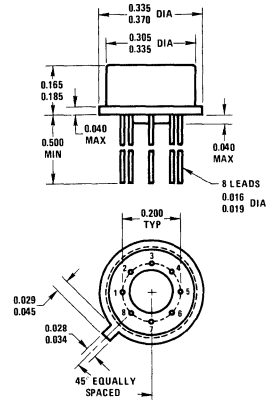
Package 20
40-Lead Molded DIP (N)



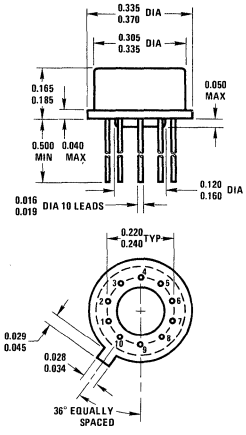
Package 21
24-Lead Quartz Lid Cavity DIP (Q)



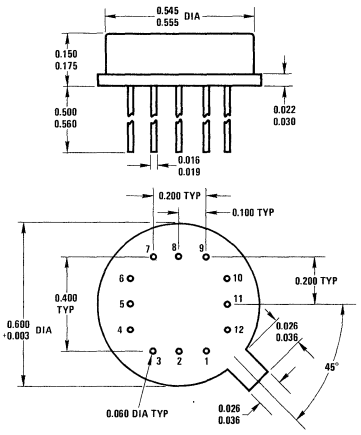
Package 22
4-Lead TO-72 Metal Can Package (H)



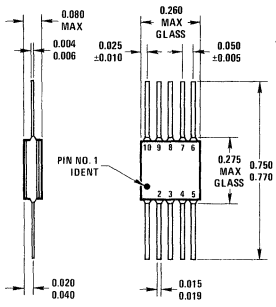
Package 23
8-Lead TO-5 Metal Can Package (H)



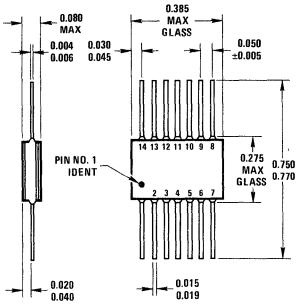
Package 24
10-Lead TO-5 Metal Can Package (H)



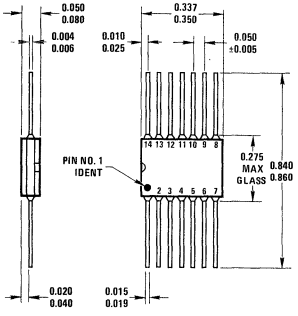
Package 25
12-Lead TO-8 Metal Can Package (G)



Package 25A
10-Lead Flat Package (F)



Package 26
14-Lead Flat Package (F)



Package 27
14-Lead Flat Package (W)

INCHES TO MILLIMETERS CONVERSION TABLE					
INCHES	MM	INCHES	MM	INCHES	MM
0.001	0.0254	0.010	0.254	0.100	2.54
0.002	0.0508	0.020	0.508	0.200	5.08
0.003	0.0762	0.030	0.762	0.300	7.62
0.004	0.1016	0.040	1.016	0.400	10.16
0.005	0.1270	0.050	1.270	0.500	12.70
0.006	0.1524	0.060	1.524	0.600	15.24
0.007	0.1778	0.070	1.778	0.700	17.78
0.008	0.2032	0.080	2.032	0.800	20.32
0.009	0.2286	0.090	2.286	0.900	22.86

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