155 Mb/s ATM Twisted Pair Signaling with the DP83223A TWISTER

National Semiconductor
Application Note 966
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September 1994

1.0 INTRODUCTION

The National Semiconductor DP83223A TWISTER transceiver was designed for binary or three level signaling at data rates up to and beyond 155 Mb/s. The DP83223A TWISTER was also designed to provide robust operation for lengths of 100Ω Cat-5 UTP or 150Ω STP cabling up to and beyond 100 meters. The ATM Forum Physical Layer Subworking Group has drafted a working document which specifies the protocol for 155 Mb/s STS-3c signaling over 100Ω Cat-5 UTP or 150Ω STP twisted pair cabling. The DP83223A TWISTER Transceiver is 100% compliant with this document, providing an integrated, cost effective and reliable solution. This application note provides information to assist in the understanding and design of a 155 Mb/s ATM Twisted Pair PMD based on the DP83223A TWISTER.

2.0 OVERVIEW

The subjects covered in this application note include a Connection Diagram, PMD Schematics with Circuit Details, Layout Considerations, and Magnetics. Additionally, appendices covering a bill of materials for a typical UTP design and common mode termination references are included.

The requirements for compliance to the PMD working Draft are outlined herein. In general terms, the transmitting and receiving nodes must effectively couple the serial bit stream to and from the twisted pair media. This transmission must be compliant with the AOI (Active Output Interface), the AII (Active Input Interface) as well as the twisted pair Channel Characteristics as defined in the working draft document. More specifically, the ATM PMD working draft defines the differential signal encoding, signal decoding and media types as:

- ENCODE = 1V pk-pk differential NRZ Binary
- DECODE = Receive end Equalization
- MEDIA = Up to 100M of 100Ω Category 5 Unshielded Twisted pair or 150Ω Shielded Twisted Pair.

Note: Media types should conform to the EIA/TIA 574 for STP and EIA/TIA 568 and TSB-36 for UTP specifications.

3.0 CONNECTION DIAGRAM

The DP83223A TWISTER allows for a simple, cost-effective design while requiring minimal board space. The Connection diagram in *Figure 1* illustrates the general placement and interconnection of the PMD relative to the TC (Transmission Convergence) Layer and the twisted pair cabling.

4.0 PMD SCHEMATIC

The schematic examples given in *Figures 2* and *3* provide detailed 100Ω UTP and 150Ω STP designs respectively which may be integrated directly onto a motherboard. With only minor modifications, this design may be used to create an ORM (Optical Replacement Module). Refer to section 4.1.1.2 for further information concerning ORM applications.

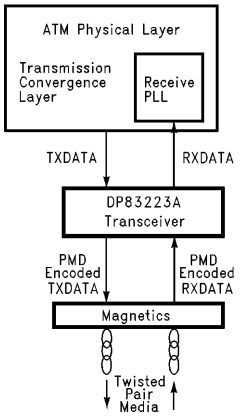

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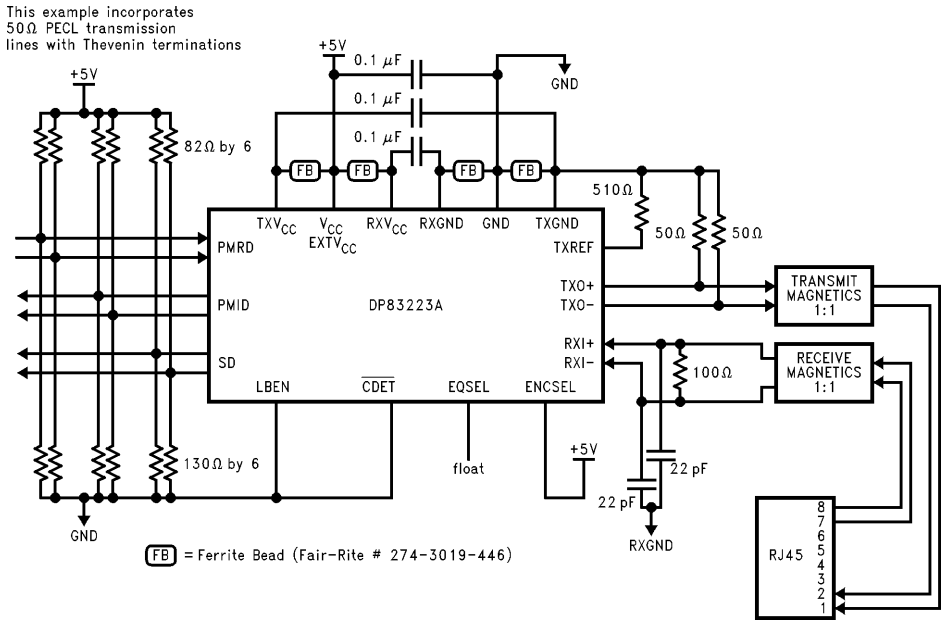
FIGURE 1. Typical ATM STS-3c Twisted Pair System Connection

RRD-B30M75/Printed in U. S. A.



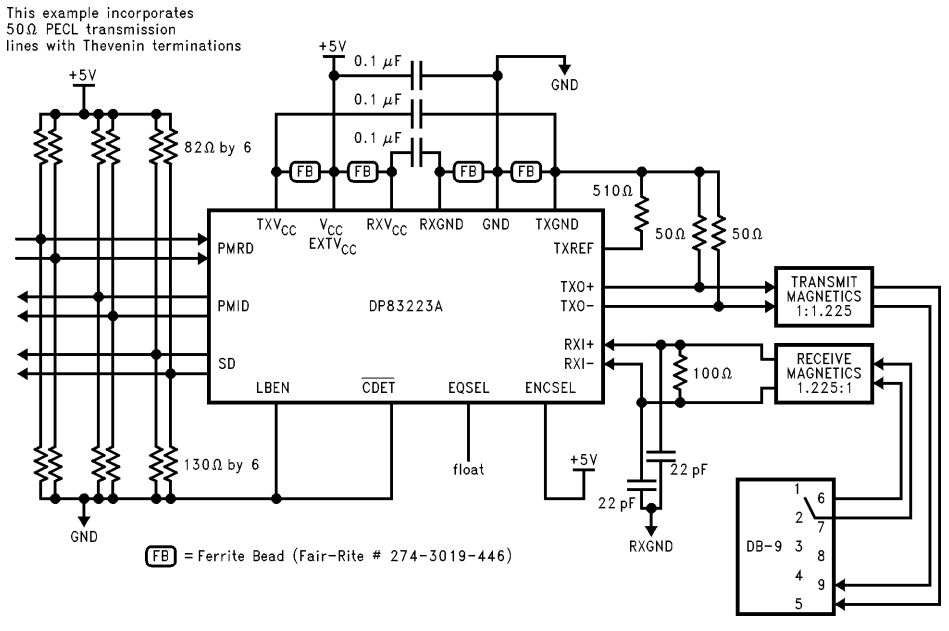
This schematic does not include any common mode termination.

Refer to Appendix B for optional common mode termination information.

RJ45 pinout for UTP 155 M/bs ATM:

Transmit+ = pin 1
Transmit− = pin 2
Receive+ = pin 7
Receive− = pin 8

FIGURE 2. Typical 155 Mb/s 100Ω CAT-5 UTP PMD Schematic



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This schematic does not include any common mode termination.

Refer to Appendix B for optional common mode termination information.

STP DB-9 pinout for 155 M/bs ATM:

Transmit+ = pin 5
Transmit− = pin 9
Receive+ = pin 1
Receive− = pin 6
Shield = Chassis Ground

FIGURE 3. Typical 155 Mb/s 150Ω Type 1 STP PMD Schematic

4.1 Circuit Details

The schematics given in *Figures 2* and *3* contain several common functional parameters that require further explanation. The important differences between an STP and UTP implementation are also described. The following subsections attempt to clarify the designs, providing a more thorough understanding.

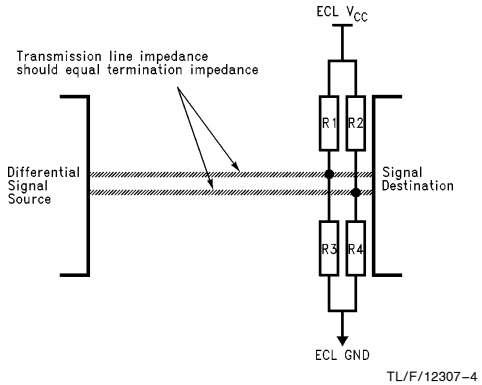
4.1.1 PECL Terminations

All PECL (Pseudo ECL) signals interfacing the TC (Transmission Convergence) Layer with the PMD require appropriate terminations. These signals include PMRD±, PMID± and SD±. There are important options to be considered when choosing the best termination scheme for a given implementation. There are also additional design guidelines available for reference which can be found in the F100K ECL Logic Databook and Design Guide published by National Semiconductor.

4.1.1.1 Cost vs. Power

Several factors must be considered when choosing a PECL termination scheme for a given implementation.

To reduce complexity and minimize costs, a Thevenin equivalent PECL termination approach which requires only two resistors per PECL signal should be considered. For a 50Ω transmission line impedance, the Thevenin equivalent consists of an 82Ω resistor from the signal to the +5V ECL supply and a 130Ω resistor from the signal to the ECL Ground return. This equivalent termination should be placed as close to the end of the transmission line(s) as possible (refer to *Figure 4*). The choice of the Thevenin equivalent termination is best suited for single-port design such as an end-station adapter card where quite often, only the three differential pairs listed in 4.1.1 require high speed PECL termination.



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For 50Ω trace impedance:

R1, R2 = 82Ω
R3, R4 = 130Ω

For higher trace impedance:

R1, R2 = 1.6 × desired impedance
R3, R4 = 2.6 × desired impedance

FIGURE 4. Thevenin Equivalent PECL Termination

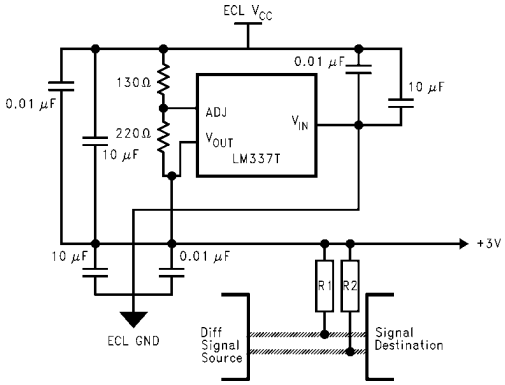
Note that each differential pair of Thevenin terminations draws approximately 30 mA of additional current from the +5V supply. For an 8-port hub consisting typically of up to 24 PECL interfaces, as much as 3.6W of additional power is required just to support the Thevenin termination scheme.

For a multi-port implementation such as a hub or switch configuration, power requirements may mandate a lower power termination technique. In this case, a dedicated rail supporting direct 50Ω termination is a good alternative to the Thevenin equivalent as it requires approximately half the power. *Figure 5* illustrates the use of the National Semiconductor LM337T Adjustable Voltage Regulator which provides a +3V supply (V_{CC} − 2V) for +5V PECL termination.

For further power conservation, the designer may optionally choose a microstrip transmission line with a higher characteristic impedance. Since all PECL interfaces to the DP83223A TWISTER are differential, the small change in output logic levels caused by a shift in termination current is minimal. More than sufficient differential logic margins will be maintained for termination impedances up to 100Ω. In addition, the higher characteristic impedance and higher termination resistance will result in slightly longer risetimes which the designer must keep in mind when choosing transmission line distances and component placement. In brief, the shorter the transmission line and the more controlled its characteristic impedance, the better the signal transfer. The choice of higher transmission line impedances and terminations is viable for either Thevenin or Direct termination techniques.

4.1.1.2 ORM vs. Direct Integration

The implementation of choice may be an ORM (Optical Replacement Module) instead of direct integration. The most obvious benefit of an ORM is the inherent flexibility in use of either Fiber or Twisted Pair for a given port design.



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R1, R2 = 50Ω or desired resistance (50Ω < Ω < 100Ω)

FIGURE 5. Direct PECL Termination

The selection of an ORM requires that the implementor understand two important factors in their design and use. Since an ORM is intended as a direct replacement for an Optical Data Link module, it is necessary to place the ECL termination on the Motherboard and not on the ORM to guarantee compatibility. It is also important for the implementor to be aware that the SD− (Signal Detect compliment) signal has been omitted from some 9-pin LCF implementations. The cost vs. power factors discussed in section 4.1.1.1 are valid for ORM implementations as well as direct integration.

4.1.2 Twisted Pair Forward Termination

Given a differential transmit amplitude of 1V pk-pk, a standard 1:1 isolation transformer at the receive input provides for optimized adaptive equalization performance for CAT-5 implementations. For compliancy to the STP specification and to maintain matched impedance to the 150Ω characteristic impedance, 1:1.225 turns ratio is required for the transmit magnetics. The reciprocal, 1.225:1, is required for the receive magnetics. Using these step-up and step-down transformers for 150Ω applications allows the use of the same components and component values for termination and noise filtering that are employed for 100Ω applications. *Figure 6* illustrates suggested placement and values for the forward cable termination. Additionally, by incorporating the two bandwidth limiting capacitors as shown in *Figure 6,* increased immunity to differential and common mode noise is achieved.

4.1.3 Twisted Pair Back Termination

Figure 7 illustrates the suggested implementation for the twisted pair back termination required for a balanced system impedance. It is suggested that the TXGND (Transmit Ground) of the DP83223A TWISTER be used as the return for the back termination of either UTP or STP cable types.

4.1.4 Transmit Amplitude

The TXREF pin of the DP83223A TWISTER offers amplitude adjustment of the transmitted signal onto the media. Assuming the use of 1:1 transformers for UTP applications and 1:1.225 transformers for STP applications, the equation for selecting the appropriate resistor value (R_{REF}) for a desired V_{OUT} is given as:

where:

> R_{REF} is the TX amplitude reference resistor in Ω

> Z_{CABLE} is the effective characteristic differential impedance of the twisted pair cable in Ω

> V_{OUT} is the differential peak-peak output voltage in V

> 5.12 is related to the reference scaling factor

Please refer to section 4.0 for proper connection of the TXREF pin.

5.0 PINOUT SUMMARY

For ease of reference, the pinout of the DP83223 TWISTER is summarized herein. Refer to the DP83223 TWISTER FDDI Datasheet for the detailed pin descriptions.

UTP RX Magnetics = 1:1
STP RX Magnetics = 1.225:1
R1 = 100Ω for UTP or STP
C1, C2 = 22 pF for UTP or STP

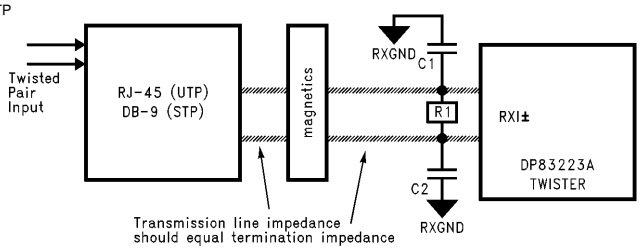

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FIGURE 6. Forward Cable Termination

UTP TX Magnetics = 1:1
STP TX Magnetics = 1.225:1
R2 = R3 = 50Ω for UTP or STP

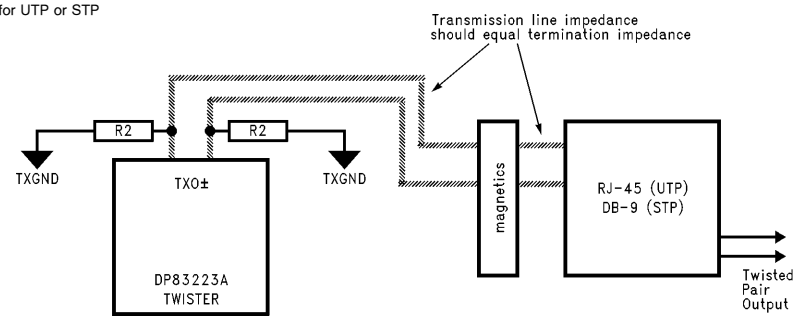

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FIGURE 7. Back Cable Termination

Signal	Pin No.	Description	Type
V_{CC}	13, 26	V_{CC}	Supply
GND	14, 22	GND	Supply
RXV_{CC}	4, 27	Receive V_{CC}	Supply
RXGND	3, 28	Receive GND	Supply
TXV_{CC}	5, 11	Transmit V_{CC}	Supply
TXGND	7, 10	Transmit GND	Supply
$EXTV_{CC}$	23	External V_{CC}	Supply
RXI ±	2, 1	Receive Data Inputs	Differential Voltage In
PMID ±	25, 24	Physical Media Indicate Data	ECL Out
PMRD ±	15, 16	Physical Media Request Data	ECL In
TXO ±	9, 8	Transmit Data Outputs	Differential Current Out
SD ±	20, 21	Signal Detect Outputs	ECL Out
TXREF	6	Transmit Amplitude Reference	Current Out
ENCSEL	12	Encode Select Input	CMOS In
LBEN	19	Loopback Enable	CMOS In
EQSEL	17	Equalization Select	3-Level Select
$\overline{OE}$	18	Output Enable Bar	CMOS Schmitt Trig In

6.0 FUNCTIONAL TRUTH TABLES

The DP83223A TWISTER incorporates a high degree of functional flexibility. The following subsections provide the logical truth tables for various functional options.

6.1 Output Enable

$\overline{OE}$	TXO	PMID ±
0	Follow PMRD	Follow RXI
1	TRI-STATE®	Static

$\overline{OE}$ should be tied low for normal operation.

6.2 Equalization Select

EQSEL	Mode
< 1.5V	Full EQ
Float	Adaptive EQ
> 3.0V	EQ Off

EQSEL should be allowed to float for 155 Mb/s ATM applications.

6.3 Encode Select

ENCSEL	Mode
0	MLT-3
1	Binary

ENCSEL should be tied to a CMOS logic high level for 155 Mb/s ATM applications.

6.4 Loopback Select

LBEN	Mode
0	Normal
1	Loopback

The Loopback Function is intended for board diagnostics. In Loopback mode, the ECL signal applied to the PMRD inputs will appear at the PMID outputs regardless of the signal present at the RXI inputs.

The LBEN pin should be tied to a CMOS logic level for normal 155 Mb/s ATM applications.

7.0 LAYOUT CONSIDERATIONS

Careful circuit layout is essential for meeting EMC/EMI requirements as well as ensuring robust overall performance. The following subsections examine power and ground issues, shielding suggestions and example PMD layouts.

It is important to note that the suggestions provided in this section will not, in and of themselves, guarantee compliance to specific EMC/EMI standards.

7.1 Power and Ground Layout

Many high frequency board designs take advantage of multiple layer topologies. Multiple board layers can be used to provide good impedance control of transmission line signal traces, increased noise margins to crosstalk and enhanced supply noise decoupling. While power and ground plane separation can be achieved on adjacent layers, additional separation can be achieved on a given single layer as well. These single layer plane separations are commonly referred to as islands. The use of islands can be beneficial in effectively separating two or more sensitive, unique power or ground planes within a given design.

The example given in *Figure 8* illustrates a desirable separation of three different power and ground planes for use with the DP83223A TWISTER. Note that Ferrite beads are used to bridge the Islands allowing for very low loss DC interconnect while providing good attenuation for AC coupled noise at critical frequencies. This design is recommended only for implementations which provide sufficient board area for creating islands of significant size. Creating islands for very small layout areas such as the 1″ x 1.5″ 9-pin LCF footprint require an alternate design. When islands become too small they begin to loose their planar properties. *Figure 9* illustrates an alternative layout recommendation for very small area implementations such as the 9-pin ORM.

7.2 Shielding

Physical shielding can help to decrease radiated emissions. The use of shielded RJ45 (UTP) or DB-9 (STP) connectors is good practice. The shields of these connectors are commonly connected directly to chassis ground of the system.

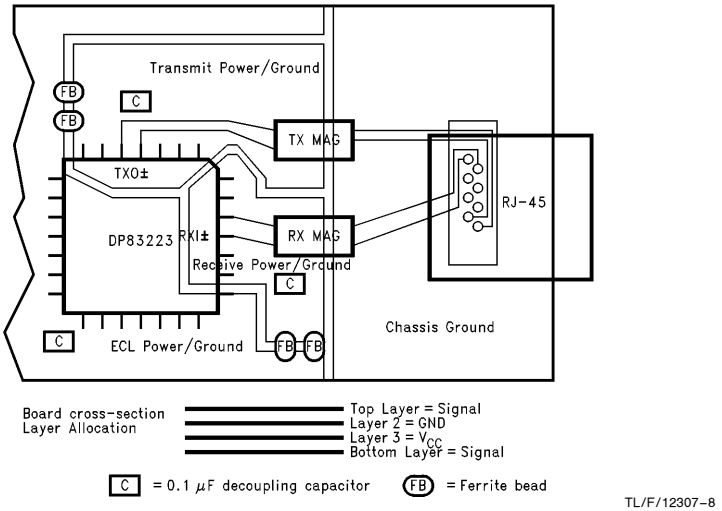

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FIGURE 8. Typical UTP Motherboard Layout

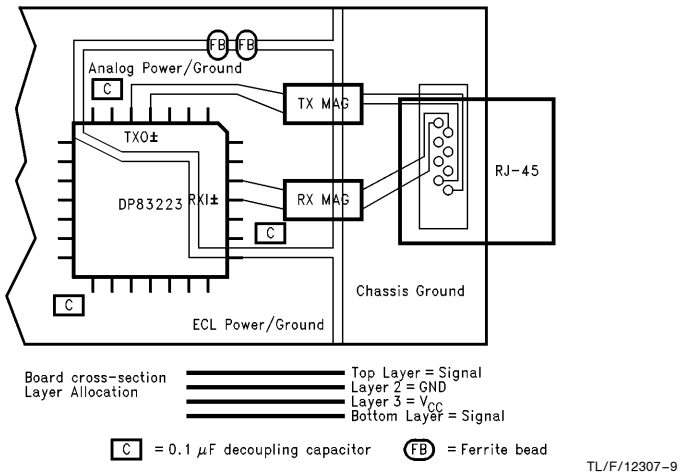

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FIGURE 9. Typical UTP ORM Layout

8.0 MAGNETICS

Effective system performance requires transmit and receive transformers for coupling the differential signal to and from the twisted pair cabling. The evolving design of magnetics for high speed networking technologies, such as FDDI over copper, offers a basic design for 155 Mb/s ATM signaling as well. National Semiconductor has worked with several magnetics companies to create designs and product for test and use with the DP83223A TWISTER. The following subsections examine the requirements for transmit and receive magnetics. The transmit and receive magnetics, as available from various vendors, may be physically separate components or a single module containing both components. The transformer center taps may optionally be used for common mode termination. Refer to Appendix B for further information.

8.1 Transmit Magnetics

The diagram in *Figure 10* illustrates the basic design for the transmit magnetics suggested for use with the DP83223A TWISTER.

8.2 Receive Magnetics

The diagram in *Figure 11* illustrates the basic design for the receive magnetics suggested for use with the DP83223A TWISTER.

8.3 Magnetics Manufacturers

Please contact your preferred magnetics vendor for the latest product information and part numbers.

Bel Fuse, Inc.
5362 W. 78th St.
Indianapolis, IN 46268-4147
(317) 876-0044

Coilcraft, Inc.
1102 Silver Lake Rd.
Cary, Illinois 60013
(708) 639-6400

Filmag
(a Technitrol Company)
9445 Farnham Street
San Diego, CA 92123
(619) 569-6577

Nano Pulse Industries
440 Nibus St.
Brea, CA 92622
(714) 529-2600

Pulse Engineering
P.O. box 12235
San Diego, CA 92112
(619) 674-8100

Valor Electronics, Inc.
9715 Business Park Ave.
San Diego, CA 92131
(619) 537-2619 or
(619) 537-2631

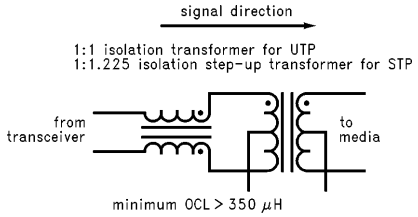

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FIGURE 10. Transmit Magnetics

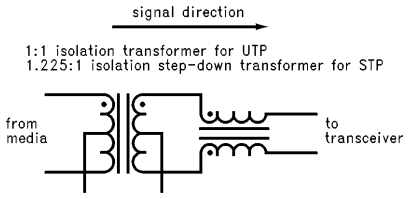

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FIGURE 11. Receive Magnetics

APPENDIX A

BILL OF MATERIALS

The following B.O.M. contains all components necessary to complete the UTP motherboard design example given in section 4.0.

ICs:

National Semiconductor DP83223A TWISTER (1)

PECL Termination Resistors:

82Ω 1/8wt 5% (6)
130Ω 1/8wt 5% (6)

Cable Termination and TXREF Resistors

50Ω 1/8wt 1% (2)
100Ω 1/8wt 1% (1)
510Ω 1/8wt 1% (1)

Decoupling Capacitors:

0.1 μF 16V 5% (3)

Optional Bandwidth Limiting Capacitors

22 pF 16V 1% (2)

Ferrites:

Fair-Rite # 274-3019-446/7 (4)

Magnetics:

Contact magnetics vendor of choice

Connectors:

Shielded PC-mount RJ45-8 (1)

APPENDIX B

COMMON MODE TERMINATION

The effects of common mode termination have been shown, in some cases, to help increase margins to both EMI radiation and susceptibility. However, it should be noted that careful PMD circuit design and shielding practices will have a significant effect on EMC related performance.

Common mode termination has been the subject of much testing and discussion throughout various Network Standards meetings. Annexes to the FDDI TWISTED PAIR PHYSICAL LAYER MEDIUM DEPENDENT (TP-PMD) ANSI Standard as well as the ATM Physical Medium Interface Specification for 155 Mb/s over Twisted Pair Cable Draft 0.3 (155-C5-UTP-PMD) define the use for and give examples of common mode termination. To obtain a copy of the ANSI FDDI TP-PMD Standard, contact Global Engineering in Englewood, CO. Tel 1-800-854-7179

REFERENCES

1. National Semiconductor DP83223A device specification.

2. FDDI TWISTED PAIR PHYSICAL LAYER MEDIUM DEPENDENT (TP-PMD) Working Draft Proposed American National Standard Rev 2.1 dated 2/94

3. The ATM Forum—ATM Physical Medium Interface Specification for 155 Mb/s over Twisted Pair Cable Draft (155-C5-UTP-PMD)

4. EIA/TIA 574, 568, and TSB-36 specifications

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