Microcontroller Interface to the ADC12038 Families

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1.0 GENERAL OVERVIEW

The ADC12038 families are 12-bit plus sign sampling ADC converters with serial I/O. These devices have configurable analog multiplexers with 2, 4, or 8 input channels. On request, these A/Ds perform a self calibration routine that minimizes linearity, zero, and full-scale errors. To minimize power consumption these devices have a power down mode that can be accessed by hardware (PD pin) or by a software instruction.

The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ and HPC™ families of controllers, and can easily interface with standard shift registers and microprocessors. The conversion resolution can be selected by a software instruction to be 8-bits, 8-bits + sign, 12-bits or 12-bits + sign. 8-bit and 8-bit + sign conversions take less time than 12-bit and 12-bit + sign conversions (21 clock periods versus 44). In addition, selection of the output data format can be software programmable to be:

1. 8-bits, 8-bits + sign, 12-bits, 12-bits + sign, 16-bits or 16-bits + sign in length
2. MSB or LSB first
3. Left or Right justified

There are three ADC12038 families: Low voltage, High speed and standard. Each family includes four different combinations of analog inputs and features as summarized in Table I.

TABLE I. Summary of the Differences of the Devices in the Three ADC12038 Families

Device Number	Operating Supply Voltage and Power Dissipation	Maximum Clock Frequency (MHz)	Maximum Sampling Rate (kHz)	Number of MUX Inputs	MUX OUT and A/D IN Pins	Hardware Power Down Control (PD Pin)	Package Size and Type
ADC12030	5V ±10%	5 MHz	73 kHz	2	NO	NO	16-pin DIP & SO
ADC12032				2	YES	NO	20-pin DIP & SO
ADC12034	33 mW (max) @5V			4	YES	YES	24-pin DIP & SO
ADC12038				8	YES	YES	28-pin DIP & SO
ADC12L030	3.3V ±10%			2	NO	NO	16-pin DIP & SO
ADC12L032				2	YES	NO	20-pin DIP & SO
ADC12L034	15 mW (max) @3.3V			4	YES	YES	24-pin DIP & SO
ADC12L038				8	YES	YES	28-pin DIP & SO
ADC12H030	5V ±10%	8 MHz	116 kHz	2	NO	NO	16-pin DIP & SO
ADC12H032				2	YES	NO	20-pin DIP & SO
ADC12H034	36 mW (max) @5V			4	YES	YES	24-pin DIP & SO
ADC12H038				8	YES	YES	28-pin DIP & SO

Throughout this application note we will refer to the ADC12038. Any of this information will also apply to all the devices in the ADC12038 families. The device data sheets should be used in conjunction with this application note to help you understand the operation of these devices. The scope of this application note will focus on the digital interface. A brief overview of the digital functionality of these devices is included.

1.1 The Serial Interface

The ADC12038 families of analog-to-digital converters can be programmed for many modes of operation through their serial digital interface. The serial interface for the ADC12038 is comprised of the digital control lines SCLK, $\overline{\text{CS}}$, DO, DI, EOC, $\overline{\text{DOR}}$, PD and $\overline{\text{CONV}}$. Table II gives a brief pin description for each of these control lines.

TABLE II. Digital Control Pin Descriptions

Pin Name	Description
SCLK	This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. With $\overline{\text{CS}}$ low the rising edge of SCLK loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the ADC. With $\overline{\text{CS}}$ low the falling edge shifts of SCLK the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{\text{CS}}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{\text{CS}}$ is toggled the falling edge of $\overline{\text{CS}}$ always clocks out the first bit of data. $\overline{\text{CS}}$ should be brought low when SCLK is low.
$\overline{\text{CS}}$	This is the chip select pin. When a logic low is applied to this pin the device is selected, activating the DO, DI, and SCLK serial interface lines. The falling edge of $\overline{\text{CS}}$ resets a conversion in progress and starts the sequence for a new conversion. When $\overline{\text{CS}}$ is brought low during a conversion in progress, the conversion is prematurely ended and the data in the output latches may be corrupted, requiring the data output at this time to be ignored. $\overline{\text{CS}}$ should be brought low when SCLK is low.
DI	The data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. Table IV, Table V, Table VI, and Table VII show the assignments of the multiplexer address and the mode select data.
DO	The data output pin. This pin is an active push/pull output when $\overline{\text{CS}}$ is Low. When $\overline{\text{CS}}$ is High this output is in TRI-STATE®. The ADC conversion result and converter status data are clocked out by the falling edge of SCLK on this pin.
EOC	This pin is an active push/pull output and indicates the status of the device. When Low, it signals that the ADC is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.
$\overline{\text{DOR}}$	This is the data output ready pin. This pin is an active push/pull output. It is useful only when $\overline{\text{CS}}$ is toggled.
$\overline{\text{CONV}}$	A logic Low is required on this pin to program any mode or change the ADC's configuration (12-bit conversion, 8-bit conversion, Auto Cal, Auto Zero etc.) as listed in the Mode Programming Table (Table IV). When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{\text{CS}}$ low and Pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero are in progress.
PD	This is the power down pin. When PD is high, the ADC is powered down; when PD is low, the ADC is powered up.

The interplay of these lines can be graphically seen in the timing diagram of *Figure 1.*

The chip select pin ($\overline{CS}$) enables the logic inputs and DO output. Eight bits of data that control the ADC are clocked in on the digital input pin (DI) by the rising edge of the serial clock (SCLK) when $\overline{CS}$ is low. Taking $\overline{CS}$ will output the first bit of data (DBO) on DO. While $\overline{CS}$ is low, the falling edge of SCLK clocks the data out on the digital output pin (DO). $\overline{CS}$ should only be brought low when SCLK is low. The functions of the convert input ($\overline{CONV}$), data output ready ($\overline{DOR}$) and end of conversion output (EOC) pins are covered in more detail in the data sheet. The simplest interface to the ADC12038 requires only 4 control lines: DO, DI, SCLK and $\overline{CS}$. For this case $\overline{CONV}$ and PD are grounded and EOC and $\overline{DOR}$ outputs are not used.

1.2 The Serial Output Word Format

The diagram in *Figure 2* shows a 16-bit serial output word. The ADC12038 family can be programmed to provide unsigned output data in 8-bit, 12-bit, or 16-bit word lengths or signed data in 9-bit, 13-bit, or 17-bit word lengths. The data format can be right- or left-justified, MSB or LSB first. Table III summarizes the available serial output data formats. Table IV describes the serial input word required to select the available serial output data formats.

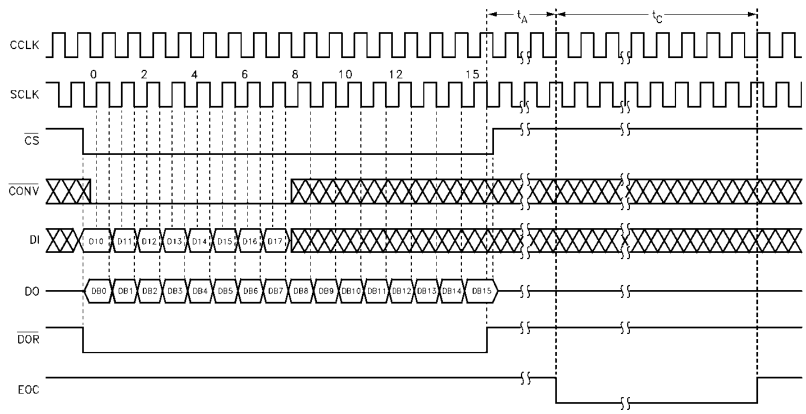

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FIGURE 1. Timing Diagram for a 12-Bit Plus Sign Conversion with a 16-Bit Serial Output Word Format on DO

TABLE III. Data Out Formats

DO Formats			DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	DB16
with Sign	MSB First	17 Bits	Sign	Sign	Sign	Sign	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB
		13 Bits	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB				
		9 Bits	Sign	MSB	6	5	4	3	2	1	LSB								
	LSB First	17 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign	Sign	Sign	Sign	Sign
		13 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign				
		9 Bits	LSB	1	2	3	4	5	6	MSB	Sign								
without Sign	MSB First	16 Bits	0	0	0	0	MSB	10	9	8	7	6	5	4	3	2	1	LSB	
		12 Bits	MSB	10	9	8	7	6	5	4	3	2	1	LSB					
		8 Bits	MSB	6	5	4	3	2	1	LSB									
	LSB First	16 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	0	0	0	0	
		12 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB					
		8 Bits	LSB	1	2	3	4	5	6	MSB									

The falling edge of SCLK strobes out the digital word on DO when $\overline{CS}$ is low. The digital word length will vary in accord with the digital word format. Thus for 8-bits + sign resolution 9 clock cycles are required.

As shown in the timing diagram *(Figure 1),* the acquisition time (the period of time during which the analog input is being sampled) starts on the falling edge of the last data clock cycle. For 16 bits of data that would be the 16th clock; for 8 bits of data that would be the 8th clock. The length of the acquisition time may be programmed by the user with an instruction, (see Table IV). The acquisition time can be set to 6, 10, 18, or 34 CCLK cycles.

1.3 Selecting Output Word Format and Mode

While $\overline{CS}$ is low, the rising edge of SCLK strobes in the data bits DI0–DI7 on the DI control line. For the ADC12038, the values of DI0–DI7 determine the digital output word format, mode select, and multiplexer configuration. For the ADC12034, 7 bits of data (DI0–DI6) are required. The ADC12032, and ADC12030 require only 6 bits of data (DI0–DI5). Mode Select determines the number of clock periods for the acquisition time (t_A), software power up/down, Auto Cal, Auto Zero and other functions as shown in Table IV.

TABLE IV. Mode Programing

ADC12038	**DI0**	**DI1**	**DI2**	**DI3**	**DI4**	**DI5**	**DI6**	**DI7**	**Mode Select (Current)**	**DO Format (next Conversion Cycle)**
ADC12034	**DI0**	**DI1**	**DI2**		**DI3**	**DI4**	**DI5**	**DI6**		
ADC12030 and ADC12032	**DI0**	**DI1**			**DI2**	**DI3**	**DI4**	**DI5**		
	MUX Address see Table V, VI or VII				L	L	L	L	12-Bit Conversion	12- or 13-Bit MSB First
	MUX Address see Table V, VI or VII				L	L	L	H	12-Bit Conversion	16-Bit MSB First
	MUX Address see Table V, VI or VII				L	L	H	L	8-Bit Conversion	8- or 9-Bit MSB First
	L	L	L	L	L	L	H	H	12-Bit Conversion of Full-Scale	12- or 13-Bit MSB First
	MUX Address see Table V, VI or VII				L	H	L	L	12-Bit Conversion	12- or 13-Bit LSB First
	MUX Address see Table V, VI or VII				L	H	L	H	12-Bit Conversion	16-Bit LSB First
	MUX Address see Table V, VI or VII				L	H	H	L	8-Bit Conversion	8- or 9-Bit LSB First
	L	L	L	L	L	H	H	H	12-Bit Conversion of Offset	12- or 13-Bit LSB First
	L	L	L	L	H	L	L	L	Auto Cal	No Change
	L	L	L	L	H	L	L	H	Auto Zero	No Change
	L	L	L	L	H	L	H	L	Power Up	No Change
	L	L	L	L	H	L	H	H	Power Down	No Change
	L	L	L	L	H	H	L	L	Read Status Register (LSB First)	No Change
	L	L	L	L	H	H	L	H	Data Out without Sign	No Change
	H	L	L	L	H	H	L	H	Data Out with Sign	No Change
	L	L	L	L	H	H	H	L	Acquisition Time—4 CCLK Cycles	No Change
	L	H	L	L	H	H	H	L	Acquisition Time—8 CCLK Cycles	No Change
	H	L	L	L	H	H	H	L	Acquisition Time—16 CCLK Cycles	No Change
	H	H	L	L	H	H	H	L	Acquisition Time—32 CCLK Cycles	No Change
	L	L	L	L	H	H	H	H	User Mode	No Change
	H	L	L	L	H	H	H	H	Test Mode (CH1–CH7 become Active Outputs)	No Change

Note: The A/D powers up with No CAL, No Auto-Zero, 10 CCLK Cycles Acquisition time, sign bit on, 13-bit MSB First format, power up, and user mode.

1.4 Multiplexer Addressing

The analog input channel configuration is selected during mode programming using the "MUX address" bits in Table IV. These bits and their effects are defined in Table V, Table VI and Table VII.

TABLE V. ADC12038 Multiplexer Addressing

MUX Address				Analog Channel Addressed and Assignment with A/D IN1 tied to MUXOUT1 and A/D IN2 tied to MUXOUT2									A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	DI3	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM	A/D IN1	A/D IN2	MUXOUT1	MUXOUT2	
L	L	L	L	+	−								+	−	CH0	CH1	Differential
L	L	L	H			+	−						+	−	CH2	CH3	
L	L	H	L					+	−				+	−	CH4	CH5	
L	L	H	H							+	−		+	−	CH6	CH7	
L	H	L	L	−	+								−	+	CH0	CH1	
L	H	L	H			−	+						−	+	CH2	CH3	
L	H	H	L					−	+				−	+	CH4	CH5	
L	H	H	H							−	+		−	+	CH6	CH7	
H	L	L	L	+								−	+	−	CH0	COM	Single-Ended
H	L	L	H			+						−	+	−	CH2	COM	
H	L	H	L					+				−	+	−	CH4	COM	
H	L	H	H							+		−	+	−	CH6	COM	
H	H	L	L		+							−	+	−	CH1	COM	
H	H	L	H				+					−	+	−	CH3	COM	
H	H	H	L						+			−	+	−	CH5	COM	
H	H	H	H								+	−	+	−	CH7	COM	

TABLE VI. ADC12034 Multiplexer Addressing

MUX Address			Analog Channel Addressed and Assignment with A/D IN1 tied to MUXOUT1 and A/D IN2 tied to MUXOUT2					A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	CH0	CH1	CH2	CH3	COM	A/D IN1	A/D IN2	MUXOUT1	MUXOUT2	
L	L	L	+	−				+	−	CH0	CH1	Differential
L	L	H			+	−		+	−	CH2	CH3	
L	H	L	−	+				−	+	CH0	CH1	
L	H	H			−	+		−	+	CH2	CH3	
H	L	L	+				−	+	−	CH0	COM	Single-Ended
H	L	H			+		−	+	−	CH2	COM	
H	H	L		+			−	+	−	CH1	COM	
H	H	H				+	−	+	−	CH3	COM	

TABLE VII. ADC12032 and ADC12030 Multiplexer Addressing

MUX Address		Analog Channel Addressed and Assignment with A/D IN1 tied to MUXOUT1 and A/D IN2 tied to MUXOUT2			A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	CH0	CH1	COM	A/D IN1	A/D IN2	MUXOUT1	MUXOUT2	
L	L	+	−		+	−	CH0	CH1	Differential
L	H	−	+		−	+	CH0	CH1	
H	L	+		−	+	−	CH0	COM	Single-Ended
H	H		+	−	+	−	CH1	COM	

Note: MUXOUT1, MUXOUT2, A/D IN1 and A/D IN2 pins are not available on the ADC12030. A/D IN1 is tied internally to MUXOUT1: A/D IN2 is tied internally to MUXOUT2.

As can be seen in the tables, 4, 3 or 2 bits of the serial digital input word control the channel selection. These bits are part of an 8-, 7-, or 6-bit serial word that controls the function of the devices.

1.5 Status Register Definition

On request, the ADC12038 provides status information indicating power up or power down status, output data format, Auto-Cal status, and User/Test Mode status. Table VIII defines the digital output data obtained after requesting a "Status Read".

When $\overline{CS}$ is used it is not necessary to clock all the status bits out. $\overline{CS}$ may be brought high at any time to restart a new serial data communication.

1.6 Programming Procedure

The example in *Figure 2* shows a typical sequence of events after power is applied to the ADC12038:

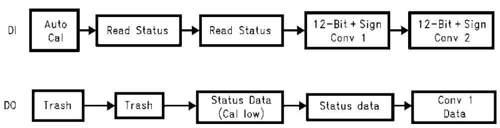

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FIGURE 2. Typical Instruction Sequence after Power Up

The first instruction to the ADC via DI initiates Auto Cal. The data output on DO at that time is meaningless and is completely random. To obtain the specified accuracy of the device it is necessary to issue an Auto Cal instruction after the power supply and reference voltage to the device have been given enough time to stabilize. The Auto Cal instruction initiates an internal calibration sequence without which the specified accuracy of the device would be unattainable. To determine whether the Auto Cal has been completed, a Read Status instruction is issued to the device. Again, the data obtained while issuing the Read Status instruction has no significance since the Auto Cal instruction modifies the data in the output shift register. To retrieve the status information an additional read status instruction is issued to the ADC. At this time the status data is available on DO. If the Cal signal in the status word is low, Auto Cal has been completed. Therefore, the next instruction issued can start a conversion. The data output, while clocking in the "start conversion request", is again status information. Status can not be read during a conversion. To preserve the integrity of the A/D conversion, there is no end of conversion bit in the status word. If $\overline{CS}$ is brought low during a conversion, that conversion is stopped and never completed. EOC can be used to determine the end of a conversion or the A/D controller can keep track in software of when it would be appropriate to communicate to the A/D again. Once it has been determined that the A/D has completed a conversion another instruction can be transmitted to the A/D. The data from this conversion can be accessed when the next instruction is issued to the A/D.

TABLE VIII. Status Register

Status Bit Location	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
Status Bit	PU	PD	Cal	8 or 9	12 or 13	16 or 17	Sign	Justification	Test Mode
Function	Device Status			DO Output Format Status					
	"High" indicates a Power Up State	"High" indicates a Power Down State	"High" indicates an Auto-Cal Sequence is in progress	"High" indicates an 8- or 9-bit format	"High" indicates a 12- or 13-bit format	"High" indicates a 16- or 17-bit format	"High" indicates that the sign bit is included. When "Low", the sign bit is not included.	When "High", the conversion result will be output MSB first. When "Low", the result will be output LSB first.	When "High", the device is in test mode. When "Low", the device is in user mode.

2.0 GENERAL FLOW CHART FOR A MICROCONTROLLER INTERFACE

Below is a flow chart that can be used for a microcontroller interface to the ADC12038. The data required by the ADC12038 is given in parentheses. The timing diagrams shown to the right are suggested for each instruction issued to the ADC.

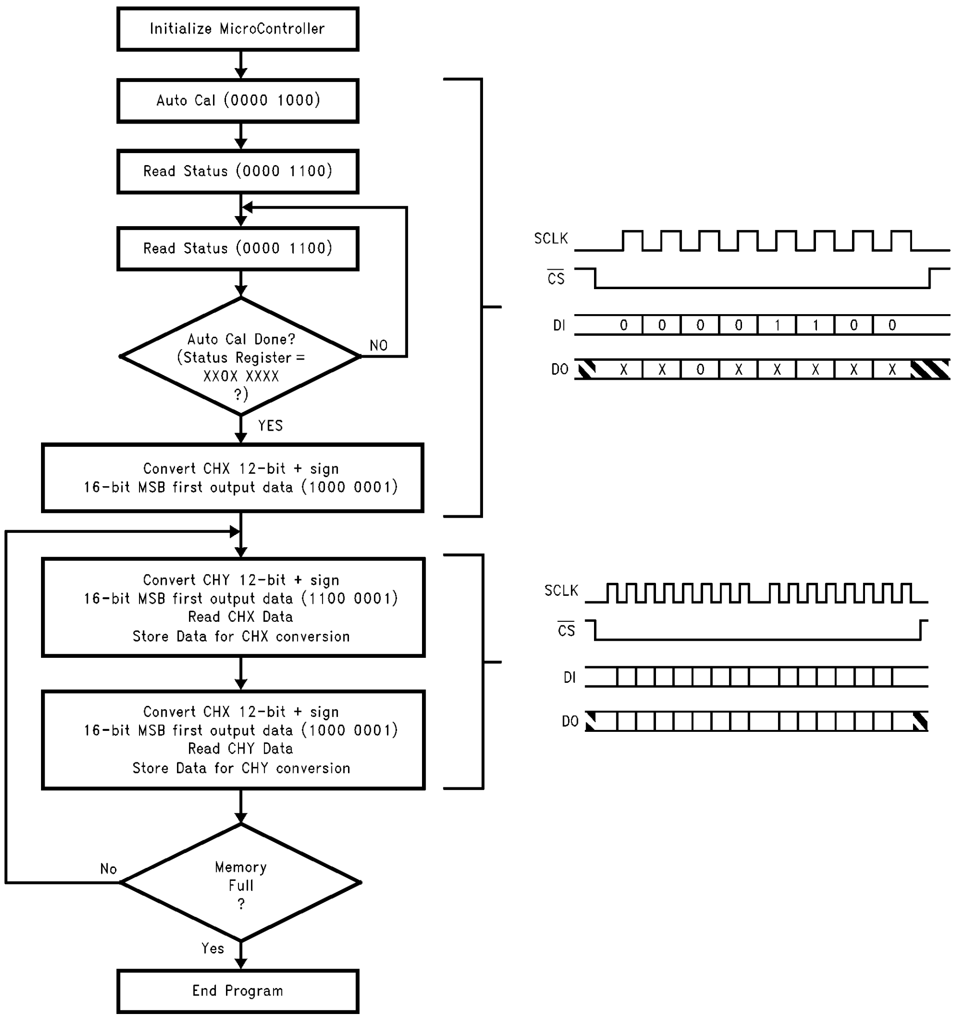

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FIGURE 3. ADC12038 Program Flow Chart and Timing

3.0 EXAMPLES OF MICROCONTROLLER HARDWARE IMPLEMENTATIONS

3.1 The 68HC11

Figure 4 shows the hardware interface to a Motorola M68HC11 microcontroller. Motorola's SPI (Serial Peripheral Interface) SCK, MISO, and MOSI lines are directly tied to the SCLK, DO and DI of the ADC12038. Port B bit 0 is used to generate the $\overline{CS}$ to the ADC.

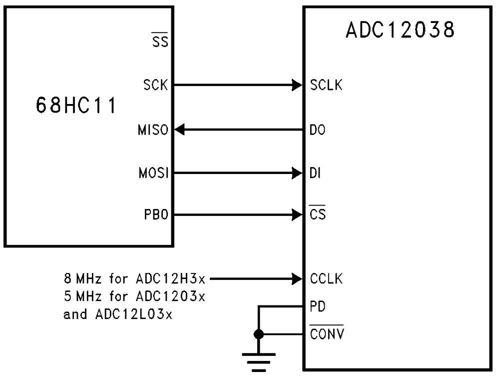

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FIGURE 4. 68HC11 ADC12038 Hardware Interface

3.2 National's HPC and COP

The serial I/O for these devices is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ and HPC™ families of controllers. The output data format is software-programmable, making the serial interface extremely flexible and an ideal choice for many applications. Shown in *Figure 5* is an implementation of an National Semiconductor HPC microcontroller interface. The SK (Serial clocK), SI (Serial Input data) and SO (Serial Output data) lines of the HPC, used in Nationals MICROWIRE interface, are tied directly to the ADC12038. Port B, bit 6 is used to generate a $\overline{CS}$ for the ADC.

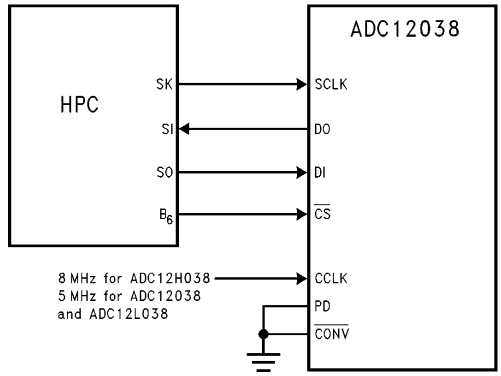

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FIGURE 5. HPC to ADC12038 Hardware Interface

3.3 The 8051

FIGURE 6 shows the ADC12038 connected to an Intel 8051. The 8051 serial interface does not support the protocol of the serial interface for this device. Therefore three port lines from the 8051 (P1.0, P1.1 and P1.2) can be used to talk to the ADC. The software toggles these lines directly to form the signals necessary to control the ADC.

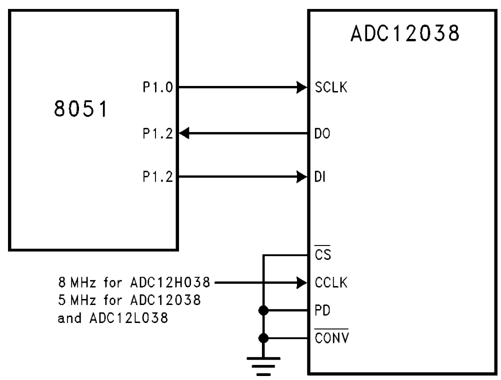

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FIGURE 6. 8051 ADC12038 Hardware Interface

4.0 68HC11 SPI INTERFACE

This section will describe in detail an SPI interface to the ADC12038. *Figure 7*, shown below, is a detailed schematic of the interface. The Motorola M68HC11EVB evaluation board was used to verify the program included at the end of this section. Therefore, the schematic shown here shows the connections required to the 68HC11 evaluation board.

4.1 68HC11 SPI Port and Register Initialization for the ADC12038

The 68HC11 SPI (Serial Peripheral Interchange) interface is ideal for driving the ADC12038. The SCK, MISO, and MOSI lines of the SPI tie directly to the SCLK, DO and DI lines of the ADC. $\overline{CS}$ for the ADC is generated using a line of the 68HC11's output port B. Here is a brief overview of the 68HC11 ports and registers used by the SPI.

The 68HC11 has four I/O ports. Port D can be set up as a general purpose I/O port or it can be used for the SPI interface and SCI (Serial Control Interface). The signal assignments for port D when used for SPI or SCI follow:

PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
X	X	SS	SCK	MOSI	MISO	TXD	RXD

SS (Slave Select), SCK (Serial ClocK), MOSI (Master Output Slave Input), MISO (Master Input Slave Output) are used for the SPI. SCI uses TXD and RXD.

There are two registers in the 68HC11 that need to be initialized: the DDRD (Data Direction Register for port D) and the SPCR (Serial Peripheral Control Register).

- **DDRD**

If ones are placed in the locations corresponding to the signal assignments for port D, those signals will be selected as outputs (except for the SS location). A one placed in the SS location disables that function. The SS input can be used for synchronizing master/slave communications between 68HC11s on the SPI bus. If SS is enabled and the 68HC11 is set as master then the SS input should be hard wired to a logical "high" for our case. Shown below is the data required to initialize DDRD for the ADC12038 interface. SS is disabled; SCK and MOSI are set as outputs; MISO is set as an input. TXD and RXD are not used but are set as input and output.

PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
X	X	1	1	1	0	1	0

DDRD resides at address i009. On the 68HC11 development board this address is 1009. All register addresses on the development board start at 1000. 0000 through 0FFF are used by the software that controls the development board. In an actual system the registers can be remapped to any 4k boundary by software.

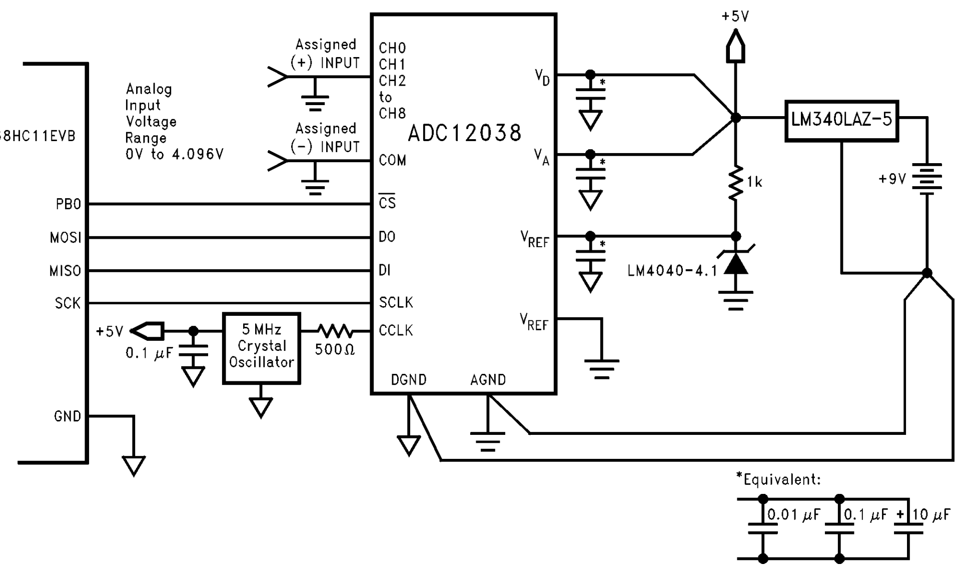

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FIGURE 7. Detailed Schematic of ADC12038 to M68HC11EVB Interface

- **SPCR**

On power up the SPI is disabled. The data stored in the SPCR (Serial Peripheral Control Register) controls how the SPI functions. SPCR resides at address 1028 for the development board. The table below summarizes the functions of the bits in this register. The SPIE (Serial Peripheral Interrupt Enable) bit when set to 1 allows the use of an interrupt to signal when an I/O exchange has completed. The SPE (Serial Peripheral Enable) bit when set to 1 enables the SPI. DWOM bit when set to 1 sets the outputs of port D to open drain. When this bit is low port D has totem pole outputs. MSTR bit controls whether this 68HC11 is a master or slave. When set to a 1 the 68HC11 is set as a master. In the slave mode SCK is an input. The CPOL and CPHA control the inactive level of the SCK output as well as which edge of the SCK output strobes the data out or in on the MISO or MOSI pins of port D. With both these bits set low the timing is as shown in *Figure 8*.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
0	1	0	1	0	0	0	0

The 68HC11 clocks in the data on MISO using the rising edge of SCK. Data on MOSI changes on the falling edge of SCK. This timing matches what the ADC12038 expects. SPR1 and SPR2 control the frequency of SCK as shown in Table IX.

TABLE IX. SCK Frequency Control

XTAL Frequency	Internal Processor Clock	SCK Frequency	Internal Processor Clock Divide by	SPR1	SPR0
8 MHz	2 MHz	1 MHz	2	0	0
8 MHz	2 MHz	500 kHz	4	0	1
8 MHz	2 MHz	250 kHz	8	1	0
8 MHz	2 MHz	125 kHz	16	1	1

The SPSR (SPI Status Register) logs the status of the SPI I/O interchange. The only bit that is of concern is the SPIF which when set signals that the SPI interchange is complete.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPIF							

SPDR (SPI Data Register) is an 8-bit register used to exchange input and output data on the SPI. A write to this register will initiate an SPI exchange. The data input to the 68HC11 after an SPI exchange will reside in this register. This register resides at address 1029 for the development system.

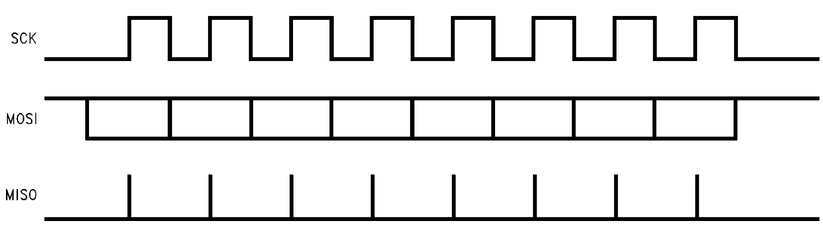

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FIGURE 8. SPI Timing Diagram Required for the ADC12038

4.2 68HC11 Program Listing

The following program listing follows the flow chart given in Section 2.0.

```
**********************************************************************************************
                         *       Emmy Denton              3/4/93
                         *
                         *       ADC12'38 MC68HC11 SPI Interface
                         *
                         *
                         *       This program
                         *               1. Initializes the SPI interface
                         *               2. Starts a self calibration
                         *               3. Fills memory locations C200-C2FF with
                         *                conversions of CH0 and CH1 set up as single ended,
                         *                12-bit +sign MSB first
                         *
**********************************************************************************************
                         *
0081                     CH0CONV   EQU      %10000001        ADC DI FOR CH0 CONVERSION
00c1                     CH1CONV   EQU      %11000001        ADC DI FOR CH1 CONVERSION
0008                     CAL       EQU      $08              ADC DI FOR CALIBRAITON
000c                     STATUS    EQU      $0C              ADC DI FOR STATUS READ
c1ff                     STARTDATA EQU      $C1FF            START ADDRESS - 1 FOR CONVERSION RESULTS
c2ff                     ENDDATA   EQU      $C2FF            END ADDRESS FOR CONVERSION RESULTS
1009                     DDRD      EQU      $1009            DATA DIRECTION REGISTER ADDRESS
1028                     SPCR      EQU      $1028            SPI CONTROL REGISTER ADDRESS
1029                     SPSR      EQU      $1029            SPI STATUS REGISTER ADDRESS
102a                     SPDR      EQU      $102A            SPI DATA REGISTER ADDRESS
1004                     PORTB     EQU      $1004            PORT B ADDRESS
1008                     PORTD     EQU      $1008            PORT D ADDRESS (SPI OUTPUT)


c000                               ORG      $C000            STARTING ADDRESS OF PROGRAM*





                         *******
                         *       INITIALIZE SPI INTERFACE PORT
                         *******
c000 86 20                         LDAA     #$20
c002 b7 10 08                      STAA     PORTD            SET SCK TO 0, MISO TO 0, SS TO 1

c005 86 3a                         LDAA     #$3A             SET DDRD: DISABLE SS; SCK, MOSI, TXD - OUTPUTS;
c007 b7 10 09                      STAA     DDRD                       MISO,RXD - INPUTS.
                         *
c00a 86 50                         LDAA     #$50             SET SPCR
c00c b7 10 28                      STAA     SPCR





                         *******
                         *       INITIALIZE PORT B AND X INDEX REGISTER
                         *******
c00f f6 10 04                      LDAB     PORTB            PLACE PORT B DATA INTO ACC B
c012 ca 01                         ORAB     #$01             (BIT 0 OF PORT B IS ADC CS) SET CS OF ADC HIGH
c014 f7 10 04                      STAB     PORTB
c017 ce c1 ff                      LDX      #STARTDATA       SET X INDEX REGISTER TO START OF ADC DATA
                         *



                         *
```

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```
                   *******
                   *       ADC MAIN PROGRAM
                   *******
                   *

c01a 86 08         MAIN     LDAA    #CAL
c01c bd c0 53               JSR     EBWRADC          ACC A JUNK START CALIBRATION
c01f 86 0c                  LDAA    #STATUS          READ STATUS
c021 bd c0 53               JSR     EBWRADC          JUNK IN ACCUMULATOR
                   *
c024 86 0c         CALWAIT  LDAA    #STATUS
c026 bd c0 53               JSR     EBWRADC          READ ADC STATUS
c029 84 20                  ANDA    #$20             MASK STATUS BIT
c02b 26 f7                  BNE     CALWAIT          IF Z=1 JUMP TO CALWAIT
                   *
c02d 86 81                  LDAA    #CH0CONV
c02f bd c0 53               JSR     EBWRADC          START CH0 CONVERSION DO IS JUNK
                   *
                   *
c032 86 c1         CONV     LDAA    #CH1CONV         START CH1 CONVERSION
c034 bd c0 6e               JSR     SBWRADC

c037 08                     INX
c038 a7 00                  STAA    0,X              STORE CH0 DATA
c03a 08                     INX
c03b e7 00                  STAB    0,X

c03d 86 81                  LDAA    #CH0CONV         START CH0 CONVERSION
c03f bd c0 6e               JSR     SBWRADC

c042 08                     INX
c043 a7 00                  STAA    0,X              STORE CH1 DATA
c045 08                     INX
c046 e7 00              STAB 0,X

c048 8c c2 ff               CPX     #ENDDATA         IS MEMORY FOR DATA FULL
c04b 26 e5                  BNE     CONV             IF NOT DO ANOTHER 2 CONVERSIONS
c04d ce c1 ff               LDX     #STARTDATA
c050 01                     NOP
c051 01                     NOP
c052 01                     NOP
                   *
                            END




                   *******
                   *        EBWRADC - Subroutine to Output/Input 8 bits to/from ADC (SPI port)
                   *        UPON ENTERING SUBROUTINe - ACCUMULATOR A HAS DATA TO OUTPUT TO ADC
                   *        UPON EXITING SUBROUTINE - ACCUMULATOR A HAS DATA FROM ADC
                   *******
c053 f6 10 04      EBWRADC  LDAB    PORTB            READ PREVIOUSE SETTING OF PORTB
c056 c4 fe                  ANDB    #$FE             SET CS LOW (BIT 0 OF PORTB)
c058 f7 10 04               STAB    PORTB
c05b b7 10 2a               STAA    SPDR             WRITE ACCUMULATOR A TO SPI PORT AND READ SPI

c05e b6 10 29      SPIWTA   LDAA    SPSR             WAIT FOR SPI INTERFACE
c061 84 80                  ANDA    #$80             AND RESET SPI FOR ANOTHER TIMING SEQUENCE
c063 27 f9                  BEQ     SPIWTA

c065 b6 10 2a               LDAA    SPDR             LOAD SPI DATA INTO ACCUMULATOR A
c068 ca 01                  ORAB    #$01             SET CS HIGH
c06a f7 10 04               STAB    PORTB
c06d 39                     RTS
```

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```
                         *
                         *******
                         *       SBWRADC - Subroutine to Output/Input 16 bits to/from ADC (SPI port)
                         *       UPON ENTERING SUBROUTINE - ACCUMULATOR A and B HAVE DATA TO OUTPUT TO ADC
                         *       UPON EXITING SUBROUTINE - ACCUMULATOR A AND B HAVE DATA FROM ADC
                         *******


c06e f6 10 04            SBWRADC LDAB    PORTB             READ PREVIOUS SETTING OF PORTB
c071 c4 fe                       ANDB    #$FE              SET CS LOW (BIT 0 OF PORTB)
c073 f7 10 04                    STAB    PORTB
c076 b7 10 2a                    STAA    SPDR              WRITE ACCUMULATOR A TO SPI PORT AND READ BYTE 1

c079 b6 10 29            SPIWTB  LDAA    SPSR              WAIT FOR SPI INTERFACE
c07c 84 80                       ANDA    #$80              AND RESET SPI FOR ANOTHER TIMING SEQUENCE
c07e 27 f9                       BEQ     SPIWTB

c080 f6 10 2a                    LDAB    SPDR              LOAD SPI DATA (BYTE 1) INTO ACCUMULATOR B
c083 b7 10 2a                    STAA    SPDR              WRITE ACCUMULATOR A TO SPI PORT AND READ BYTE 2

c086 b6 10 29            SPIWTC  LDAA    SPSR              WAIT FOR SPI INTERFACE
c089 84 80                       ANDA    #$80              AND RESET SPI FOR ANOTHER TIMING SEQUENCE
c08b 27 f9                       BEQ     SPIWTC

c08d b6 10 04                    LDAA    PORTB             SET CS HIGH
c090 8a 01                       ORAA    #$01
c092 b7 10 04                    STAA    PORTB
c095 b6 10 2a                    LDAA    SPDR              LOAD SPI DATA (BYTE 2) INTO ACCUMULATOR A

c098 39                          RTS
                         *
```

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REFERENCES

National Semiconductor Microcontroller Databook

Motorola MC68HC11 Reference Manual #M68HC11RM/AD

Motorola MC68HC11A8/1/0 Data Sheet

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