Introduction to Single Chip Microwave PLLs

ABSTRACT

Synthesizer and Phase Locked Loop (PLL) figures of merit including phase noise, spurious output and lock time, at microwave frequencies, are examined. Measurement methods for these parameters and supporting software are discussed in detail. The requirements for the loop filter, the charge pump, the dual modulus prescaler and their effects on PLL performance are analyzed.
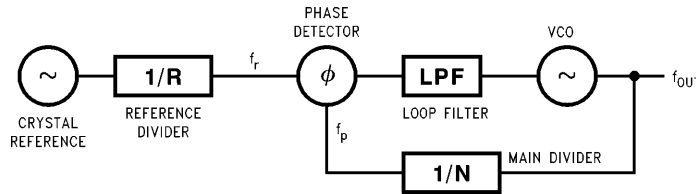
INTRODUCTION

Phase Locked Loops are used for many radio applications including frequency synthesizers, carrier recovery and clock recovery circuits, tunable filters, frequency multipliers, receiver demodulators and modulators. This application note will concentrate on the use of a PLL as a frequency synthesizer, as shown in *Figure 1.*

There are two main reasons for using a PLL as a frequency synthesizer. One is to translate the frequency accuracy of a high quality signal source to a tunable signal source. The second is to translate the noise characteristics of a high quality signal source to a lower quality signal source. The block diagram of a basic PLL is shown in *Figure 1.* The high quality signal source, in this case, is a crystal reference.

A single chip PLL consists of the reference divider, the main divider (including a dual modulus prescaler), the phase detector and a charge pump.

FIGURE 1. Block Diagram of a Basic Phase Locked Loop

SYNTHESIZER AND PLL FIGURES OF MERIT

Phase noise is a measure of the spectral purity of the tone produced by the PLL. It is dependent on the noise characteristics of the crystal oscillator reference and the VCO as well as some noise contribution of the dividers. Phase noise is defined as the ratio of the single sideband power (within a 1 Hz bandwidth at some offset frequency) to the total carrier power. Phase noise is often measured in units of dBc/Hz.
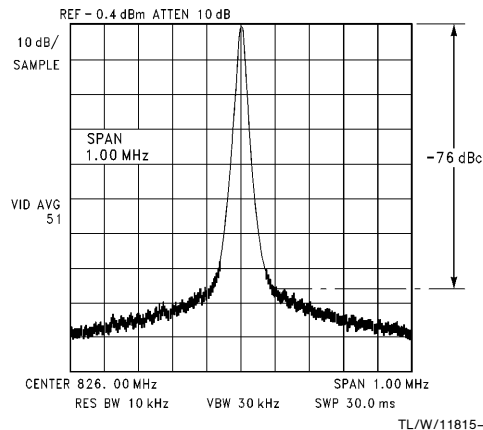
Spurious output is a measure of the level of the reference spurs (sometimes referred to as reference sidebands) on the output tone. The reference spurs appear on the output tone at the center frequency $\pm$ the reference frequency and at integer multiples of the reference frequency. For example, a PLL operating at 836 MHz with a reference frequency of 25 kHz will have reference spurs at 836.025 MHz, 835.075 MHz, 836.050 MHz, 835.050 MHz, etc.

Lock time or switching speed is a measure of the settling time of the PLL once a change in frequency has been initiated. The frequency step and the frequency accuracy to define "locked" must both be defined for this measurement to be useful.

PHASE NOISE MEASUREMENT METHODS

The phase noise characteristics of the PLL can be measured on a spectrum analyzer or using a phase noise test set. The spectrum analyzer test technique is described here. Phase noise is measured in units of dBc/Hz. This is done at several offsets from the output signal such as 1 kHz, 10 kHz and 100 kHz. The spectrum analyzer is tuned to the desired center frequency and the span is adjusted so the appropriate offset frequency can be viewed. The difference between the level of the carrier and the noise level minus 10 [log (resolution bandwidth)] is equal to the phase noise in dBc/Hz. The resolution bandwidth is read directly from the spectrum analyzer. The phase noise result in dBc/Hz is a negative number. Since phase noise is measured in dBc/Hz the measurement is always normalized to a 1 Hz bandwidth. The video averaging feature of the analyzer is used to better determine the noise level. An example of such a measurement, for the LMX1501A PLL using a reference frequency of 25 kHz, is shown in *Figure 2.* Refer to the LMX1501A data sheet for application circuits.

FIGURE 2. An 826 MHz Synthesizer Phase Noise Measurement @ 100 kHz = −116 dBc/Hz. Using the LMX1501A PLL.

Example Phase Noise Calculation

phase noise

$$(@100 \text{ kHz}) = -76 \text{ dBc} - 10 \bullet \log(\text{res.BW})$$
$$= -76 \text{ dBc} - 10 \bullet \log (10 \text{ kHz})$$
$$= (-76 - 10 \bullet 4) \text{ dBc/Hz}$$
$$= -116 \text{ dBc/Hz}$$

REFERENCE SIDEBAND MEASUREMENT METHODS

The reference sidebands can be seen on a spectrum ana-lyzer and are measured in dBc. The analyzer is set to the desired center frequency and the span is set to allow the reference sidebands to be viewed. For example, to see the reference spurs for a 1.7 MHz reference frequency the span would be set to 10 MHz. The spurious output is the differ-ence between the level of the PLL tone (at the center fre-quency) and the level of the reference spur (at the center frequency ± the reference frequency). In *Figure 3,* the ref-erence sidebands for a 1.7 MHz reference frequency are about 78 dB down from the PLL tone, or −78 dBc. Refer to the LMX2320 data sheet for application circuits.
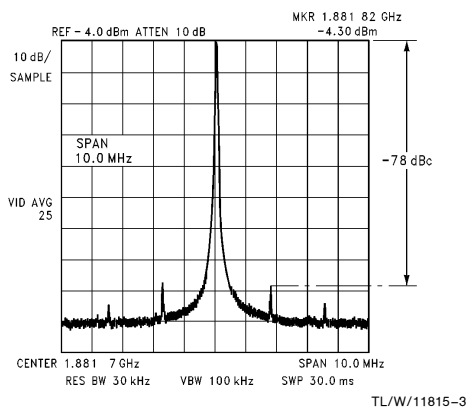

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**FIGURE 3. An 1881 MHz Synthesizer with a
Reference Frequency of 1.7 MHz and Sidebands
@ 1.7 MHz = −78 dBc. Using the LMX2320 PLL.**

SWITCHING SPEED MEASUREMENT METHODS

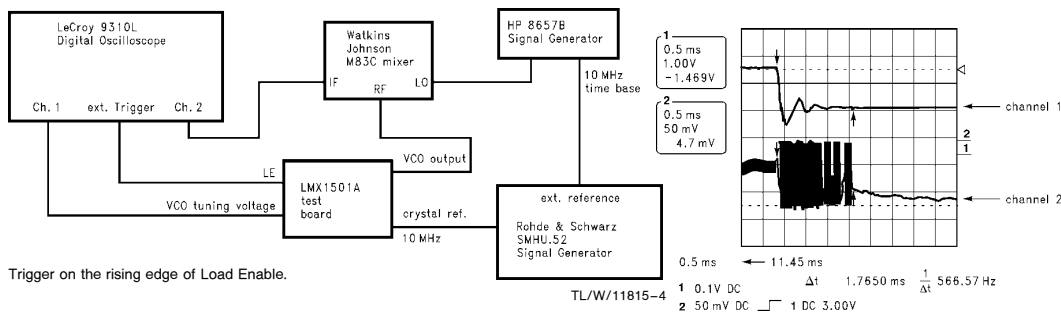Switching speed is measured on an oscilloscope by probing the VCO tuning voltage. The transient response will be seen directly. This method shows the damping characteristics of the loop but does not provide the accuracy of the frequency match.

Figure 4 illustrates an evaluation method using a mixer to determine the accuracy of the frequency match. The signal generator is phase locked to the crystal reference input to the PLL. This is accomplished by using a signal generator for the crystal reference and having the 10 MHz reference used as an external reference for the other signal generator. The output of the VCO is mixed with a signal (from a signal generator) at the desired frequency (using the mixer as a phase detector). When the frequencies are matched a DC voltage appears at the output of the mixer. When the fre-quencies are mismatched a beat note appears at the output of the mixer. Either of these signals is viewed on a scope. The peak to peak amplitude of the beat note represents a phase offset of ±180°. The slope of the beat note repre-sents a change in phase divided by time, which is equivalent to frequency. This frequency represents the frequency mis-match. As the slope of the line approaches zero the fre-quencies converge, and the loop locks. This method gives a frequency accuracy within 100 Hz.

An example of the above two types of switching speed mea-surements is shown in *Figure 4.* Channel 1 shows the VCO tuning voltage and channel 2 shows the output of the mixer IF port.

A third method uses a spectrum analyzer to view the tran-sient response by setting the frequency span to 0 Hz. The display is effectively now frequency versus time. The video band width should be set on maximum. The frequency off-set will be equal to the resolution bandwidth setting at 10 dB down from the top on the vertical axis. This is due to the filter characteristics of the analyzer. To be fully accurate the external trigger of the analyzer should be triggered off the loading of the new frequency. This method is not recom-mended for measuring lock times under 10 milliseconds be-cause on some spectrum analyzers the display response time of the analyzer is longer than a few milliseconds and erroneous data can result. A modulation domain analyzer can also be used to measure switching speed. It displays frequency versus time directly but it is not available in all labs.

Trigger on the rising edge of Load Enable.

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**FIGURE 4. Test Setup and Lock Time for 10 MHz Step = 1.77 ms
using a LMX1501A with a Reference Frequency of 25 kHz.**

2

SUPPORTING SOFTWARE

A software program of some kind is needed in order to program the PLL chip to test it. National Semiconductors LMX series of PLL chips are programmed via a three line MICROWIRE™ serial interface (clock, data, load enable). National Semiconductor Corporation provides a DOS program to allow the user to program the chip from the parallel port of a DOS personal computer. The user enters the frequency of operation, the reference frequency and the crystal frequency then presses one key to load in the appropriate divider values. The frequency can be tuned in steps of the reference frequency and a switching mode is available to test the lock time. The user enters the number of steps and the PLL will switch between the two frequencies. The user interface for the program is function key driven. Detailed operating instructions are provided with the software. For more information on the PLL software program contact:

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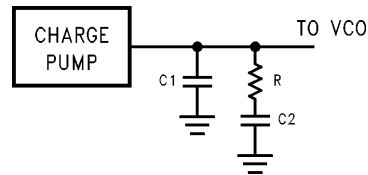D-8080 Furstenteldbruck
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LOOP FILTER

The design of the loop filter involves a trade off between reference sidebands and switching speed. The loop filter must be designed for the correct balance between reference spurs and lock time that the system requires. Generally, the narrower the loop bandwidth the lower the reference spurs but the longer the lock time. The circuit in *Figure 5* shows a type 2 third order passive loop filter configuration and its transfer function.
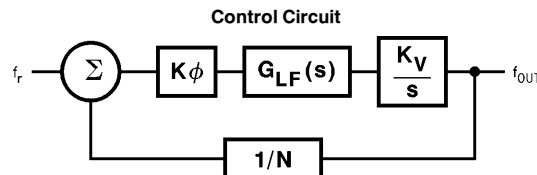

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$$G_{LF}(s) = \frac{R \bullet C2 \bullet s + 1}{s\,(C2 + C1\,(R \bullet C2 \bullet s + 1))}$$
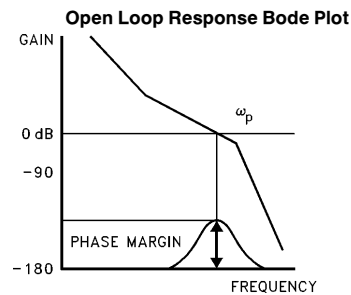
FIGURE 5. Passive Loop Filter Circuit and Loop Filter Transfer Function.

A type 2 loop has two integrators within the loop, a VCO and an integrator/filter. The order of the loop is determined by number of poles of the transfer function. Using the phase detector and VCO constants (K_ϕ and K_V) and the loop filter transfer function (G_{LF}) the open loop Bode plot can be calculated. K_ϕ and K_V are available from the PLL IC and VCO manufacturers. The control circuit, the open loop transfer function and the open loop Bode plot are shown in *Figure 6*. The loop bandwidth is shown on the Bode plot as (ω_p) the point of unity gain.

TL/W/11815–8

(G = Forward transfer function, H = Feed back)

Open Loop Transfer Equation

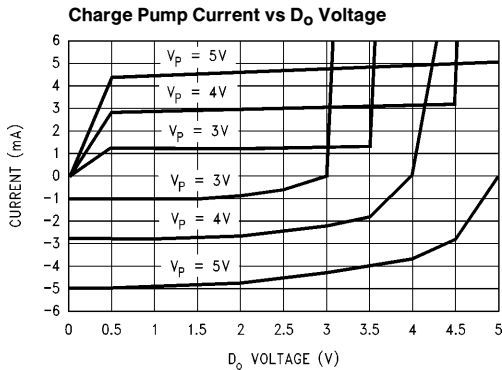$$GH(s) = \frac{K_\phi\,G_{LF}(s)\,K_V}{Ns}$$

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FIGURE 6. Control Circuit, Open Loop Equation and Bode Plot

CHARGE PUMP AND PHASE DETECTOR

A current charge pump and a phase frequency detector are implemented in National Semiconductor's LMX series of PLL chips. To increase the VCO frequency the charge pump outputs a pump up (source) current. To decrease the VCO frequency the charge pump outputs a pump down (sink) current. This current pulse charges the voltage of the capacitor C1. The charge pump is capable of supplying a controlled charge to the loop filter over a wide range of voltages, as shown in *Figure 7.*

The phase detector and charge pump are difficult to characterize separately. The figures of merit for the combination include linearity, sensitivity and deadband range. The linearity of the charge produced by the charge pump with respect to the detected phase error is critical to providing low spurious and low phase noise. The sensitivity (K_ϕ) is measured in mA/radian and depends on the charge pump current capability. Current mode charge pumps commonly have a dead zone where the gain changes dramatically for a very small phase error. The divider outputs fr and fp are a series of pulses whose relative timing reflect the phase or frequency error, as shown in *Figure 8.* At some point the pulses are too close together for the phase frequency detector to dis-

tinguish them. This is the deadband or dead zone, as shown in *Figure 9.* The LMX series of PLLs use a proprietary feedback method to minimize deadband.

Charge Pump Current vs D_O Voltage

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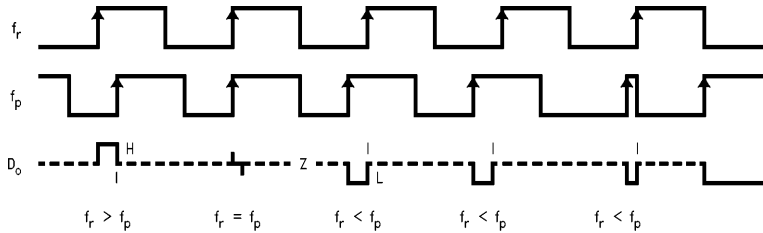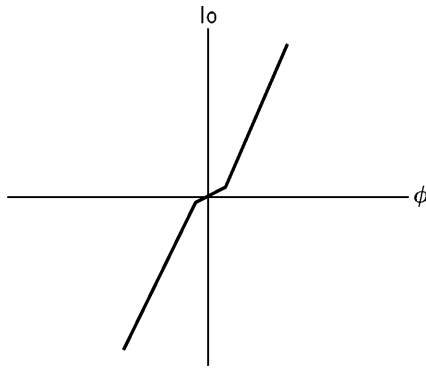**FIGURE 7. Charge Pump Current vs Voltage for the LMX Series of PLL Chips**

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FIGURE 8. Phase/Frequency Error Pulses

Phase Detector/Charge Pump Linearity

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FIGURE 9. Charge Pump Current vs. Phase Error, showing Deadband.

DUAL MODULUS PRESCALER

Dual modulus prescalers allow operation of the divider chain at high frequencies while most of the divider operates at a lower frequency. However, this capability sets limits on the range of the divider. The divider is made up of an A counter and a B counter. The A counter is the swallow counter and the B counter is the programmable divider. The condition for a legal divide ratio is that $B \geq A$.

The necessary divide number (N) is calculated by dividing the desired frequency by the reference frequency.

$$f_{out} = N f_{ref} = \frac{N}{R} f_{crystal}$$

$$R = \text{reference divide ratio} = \frac{\text{crystal frequency}}{f_{ref}}$$

The output frequency must be an integer multiple of the reference frequency. Once the divide ratio is calculated a check can be made to determine whether it is above the minimum continuous divide ratio. The minimum continuous divide ratio is equal to $P(P-1)$ where P is the prescaler divider. For example the minimum divide ratio for a 64/65 prescaler is $64(64-1)$ or 4032. If the divide ratio required (N) is below the minimum continuous divide ratio it may be a legal number but it must be verified that $B \geq A$. The values for A and B can be calculated from the following equations:

$$B = N \text{ div } P$$
$$A = N \text{ mod } P$$

A divide ratio that is above the minimum continuous divide ratio or satisfies the condition $B \geq A$ is a legal divide number. The PLL will not operate if it is programmed with an illegal divide number. For example, in choosing a prescaler for a DECT (Digital European Cordless Telephony) system the required divide ratios for the transmit side would be 1089 to 1098. The frequencies of operation for DECT are 1881.792MHz to 1897.344 MHz with a channel spacing of 1.728 MHz. The reference frequency used is 1.728 MHz.

$$\frac{1881.792}{1.728} = 1089 \quad \text{and} \quad \frac{1897.344}{1.728} = 1098$$

The minimum continuous divide ratio for a 64/65 prescaler is $64(64-1)$ or 4032. The minimum continuous divide ratio for a 128/129 prescaler is $128(128-1)$ or 16,256. For DECT the divide ratios required do not exceed the minimum continuous divide ratio for a 64/65 or 128/129 prescaler. Therefore, it must be verified that the condition of $B \geq A$ holds true. This is determined as follows:

TABLE I. Example Dual Modulus Prescaler Calculation

N	64/65		128/129	
	B	A	B	A
1089	17	1	8	65
1090	17	2	8	66
-	-	-	-	-
-	-	-	-	-
-	-	-	-	-
1097	17	9	8	73
1098	17	10	8	74

For the 64/65 prescaler, Table 1 shows $B \geq A$ therefore it can be used. The 128/129 prescaler cannot be used since $A > B$. The above calculation demonstrates that a 64/65 prescaler can be used in the DECT system for the transmit PLL.

CONCLUSION

The performance of a PLL as a frequency synthesizer is measured in terms of phase noise, spurious output and lock time. The techniques for measuring these parameters have been discussed. The loop filter, charge pump/phase detector and dual modulus prescaler and their impact on PLL performance have been analyzed. Example performance metrics were demonstrated for National Semiconductor's LMX series of PLL chips. These ICs provide the capability to produce a low power, low noise, low spurious and fast switching frequency synthesizer. With a properly designed loop filter excellent performance can be achieved. The LMX series of PLL chips provide the building block around which a high performance frequency synthesizer can be designed.

References

W.F. Egan: *Frequency Synthesizers By Phase Lock,* John Wiley and Sons, 1981

F.M. Gardner: *Phaselock Techniques, Wiley, 1989*

F.M. Gardner: *"Charge-Pump Phase-Lock Loops",* IEEE Transactions on Communications, Com-28, No. 11, November 1980

U.L. Rohde: *Digital PLL Frequency Synthesizers: Theory and Design,* Prentice Hall, 1983

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