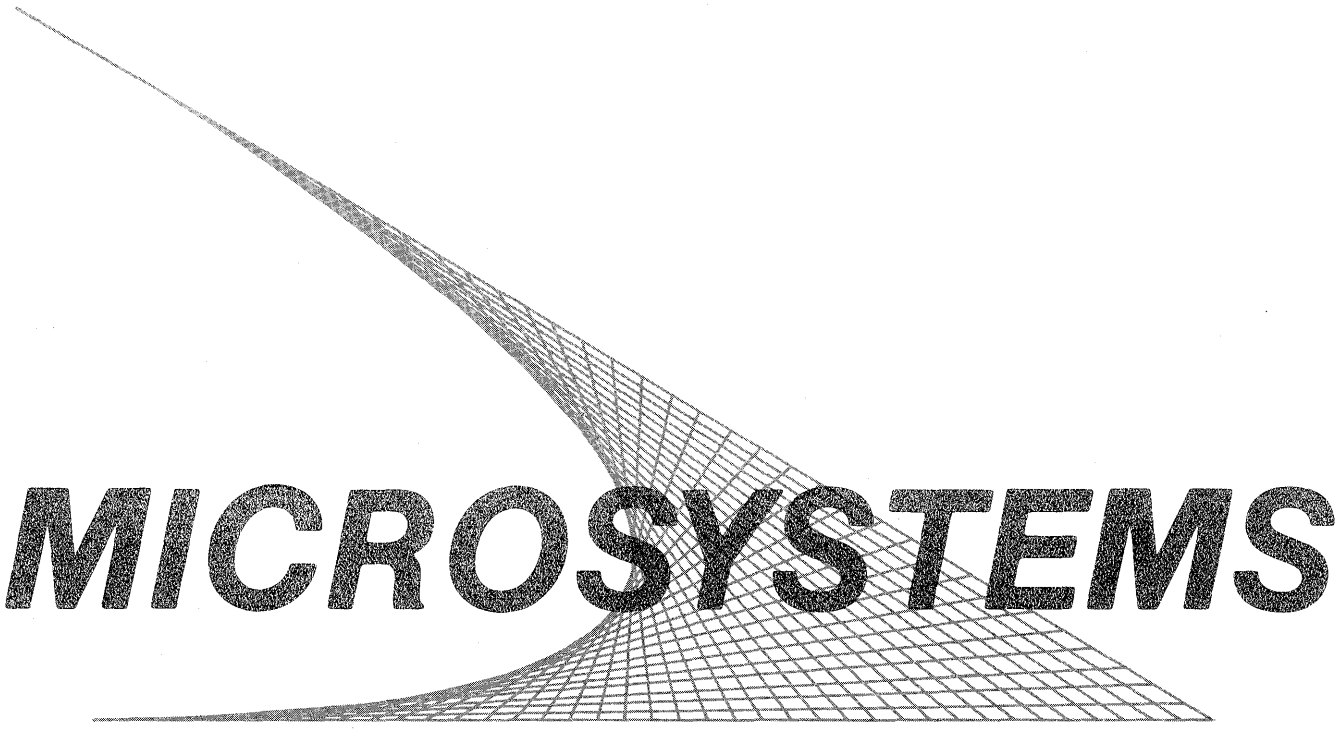
MOTOROLA

MVME410/D2

MVME410
Dual Parallel Port Module
User's Manual



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MVME410/D2

AUGUST 1983

MVME410

DUAL PARALLEL PORT MODULE

USER'S MANUAL

Second Edition

First Edition October 1982

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Microsystems Warranty and Repair for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

Throughout this manual, the X in the signal mnemonic of peripheral signals (i.e., PXCB1, PXCB2) denotes the following:

X = 1 denotes J1 front panel connector

X = 2 denotes J16 front panel connector

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation and installation instructions, operating instructions, functional description, and support information for the MVME410 Dual Parallel Port Module (referred to as DPP throughout this manual). The DPP is shown in Figure 1-1.

1.2 FEATURES

Features of the DPP are listed below.

- Motorola I/O Channel compatible.
- Single-wide VME board form factor.
- Centronics printer standard interface compatible.
- Two MC6821 Peripheral Interface Adapter (PIA) buffered ports.
- Each port capable of driving two of four I/O Channel interrupt lines.
- 16 peripheral data lines per port, each capable of sinking 24 mA.
- Four peripheral control lines per port -- two input only and two individually configurable as input or output.
- Each group of eight peripheral data lines is hardware strappable as input only, output only, or bidirectional under software control.
- Will interface two asynchronous parallel data hard copy printers to the I/O Channel.
- Operates with I/O Channel master to drive hard copy printers.
- Self-test FAIL LED indicator.

1.3 SPECIFICATIONS

General specifications for the DPP are given in Table 1-1. Table 1-2 gives peripheral signal specifications.

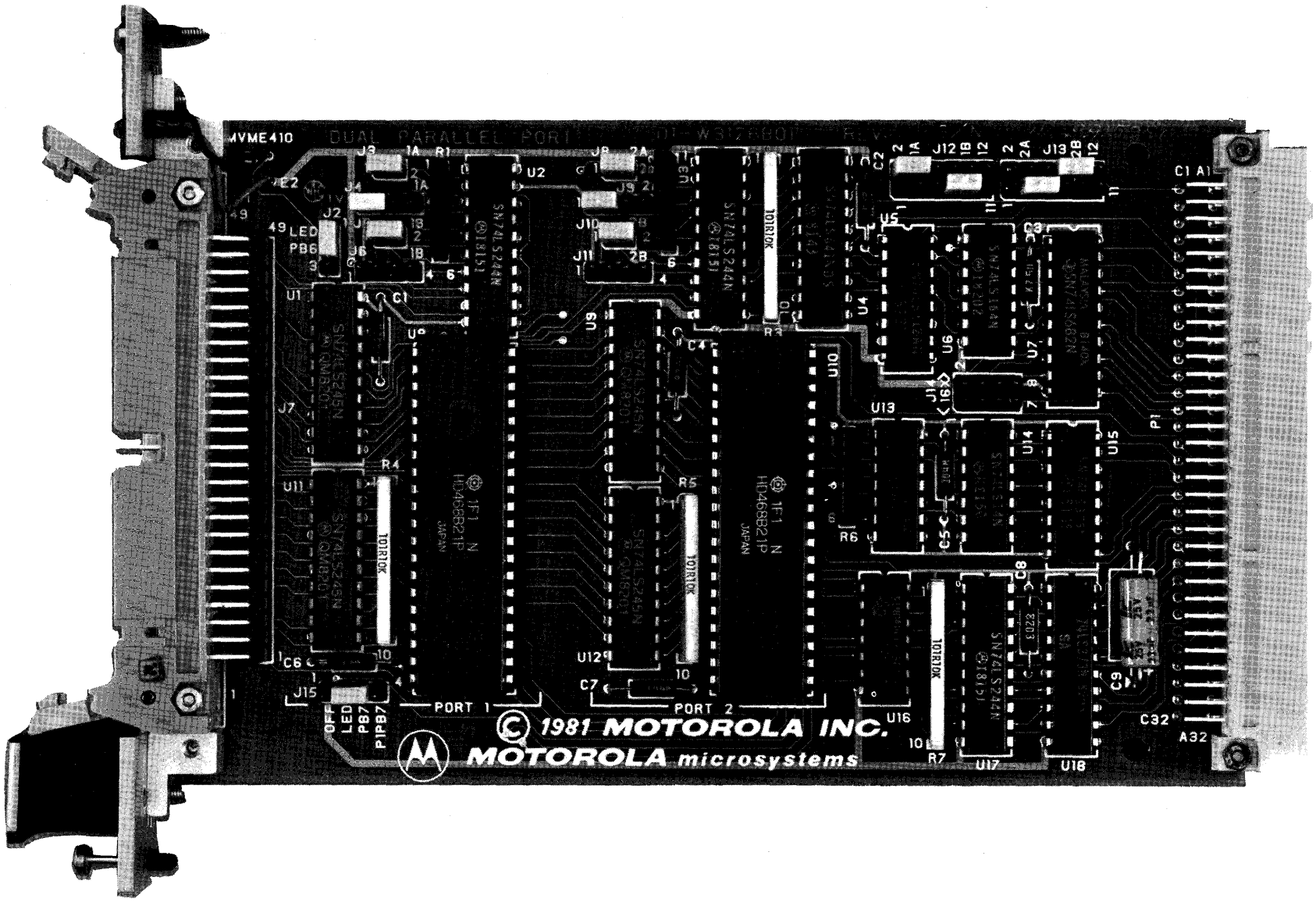


FIGURE 1-1. Dual Parallel Port Module

TABLE 1-1. Dual Parallel Port Module Specifications

CHARACTERISTIC	SPECIFICATIONS
Power requirements	+5 Vdc @ 762 mA typical 991 mA maximum
Temperature	
Operating	0° to 70° C
Storage	-40° to 85° C
Relative humidity	0% to 90% (non-condensing)
Physical characteristics	
PC board only	
Height	6.30 in. (160 mm)
Depth	3.94 in. (100 mm)
Thickness	0.59 in. (15 mm)
PC board with connectors and board stiffener	
Height	7.40 in. (188 mm)
Depth	5.12 in. (130 mm)
Thickness	0.83 in. (21 mm)

TABLE 1-2. Peripheral Signal Specifications

SIGNALS (1)	CHARACTERISTIC	SPECIFICATIONS
P1PA0-P1PA7, P1PB0-P1PB7, P2PA0-P2PA7, P2PB0-P2PB7, P1CA1-P1CB1, P2CA1-P2CB1	High level input voltage	2 volts dc minimum
	Low level input voltage	0.8 volts dc maximum
	High level output voltage with IOH = -15 mA	2 volts dc minimum
	Low level output voltage with IOL = 24 mA	0.5 volts dc maximum
	Off state output current with high level output voltage applied	10 uA maximum
	Off state output current with low level output voltage applied	-200 uA maximum
	High level input current with VIH = 2.7 volts dc	20 uA maximum
	Low level input current with VIL = 0.4 volts dc	-0.2 mA maximum

NOTE:

(1) Refer to schematic diagram. Peripheral signals P1CA2,P1CB2, P2CA2, and P2CB2 have the same specifications except that the off state characteristics do not apply. Any of the signals that are configured as inputs (except PXCA1 and PXCB1) should not be allowed to float; therefore, any input signals not driven by the peripheral should be held in either a high state or a low state.

1.4 GENERAL DESCRIPTION

The DPP is an I/O Channel-compatible dual printer interface module. This module conforms to the single-wide VME board form factor and connects to the I/O Channel with a 64-pin DIN standard connector. The DPP is used to expand the resources of an I/O Channel master to include two printer interfaces, one printer interface and a general-purpose 16-bit parallel data I/O port, or two general-purpose 16-bit parallel data I/O ports.

Two PIA's (with buffers on their peripheral sides) are employed to implement the two parallel data ports. In addition to having an I/O Channel interface, each of the PIA's is capable of driving up to two of the I/O Channel interrupt lines. A front panel FAIL LED indicator is provided to indicate a module malfunction.

The user must provide a connector-compatible I/O Channel backplane or ribbon cable for DPP connection to the I/O Channel master. Refer to the I/O Channel Specification Manual, Motorola publication number M68RIOCS, for interfacing and backplane information. The user must also provide compatible cables for DPP connection (via front panel connectors) to peripheral devices.

1.5 RELATED DOCUMENTATION

The Input/Output Channel Specification Manual, M68RIOCS, is applicable to the DPP.

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides unpacking, hardware preparation, and installation instructions for the Dual Parallel Port Module.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment.

2.3 HARDWARE PREPARATION

This section describes the hardware preparation of the DPP module prior to system installation. The DPP has been factory tested for system operation and is shipped with factory-installed jumpers. These factory-installed jumper connections should be verified to ensure that the components are properly configured for system operation. The DPP is configured to interface the I/O Channel master with Centronics printer-compatible equipment.

There are 13 headers on the DPP, as shown in Figure 2-1. They are J2-J6 and J8-J15. Table 2-1 lists each header, its function and factory-installed jumper configuration.

For signal names such as P1CA2, etc., refer to the schematic diagram.

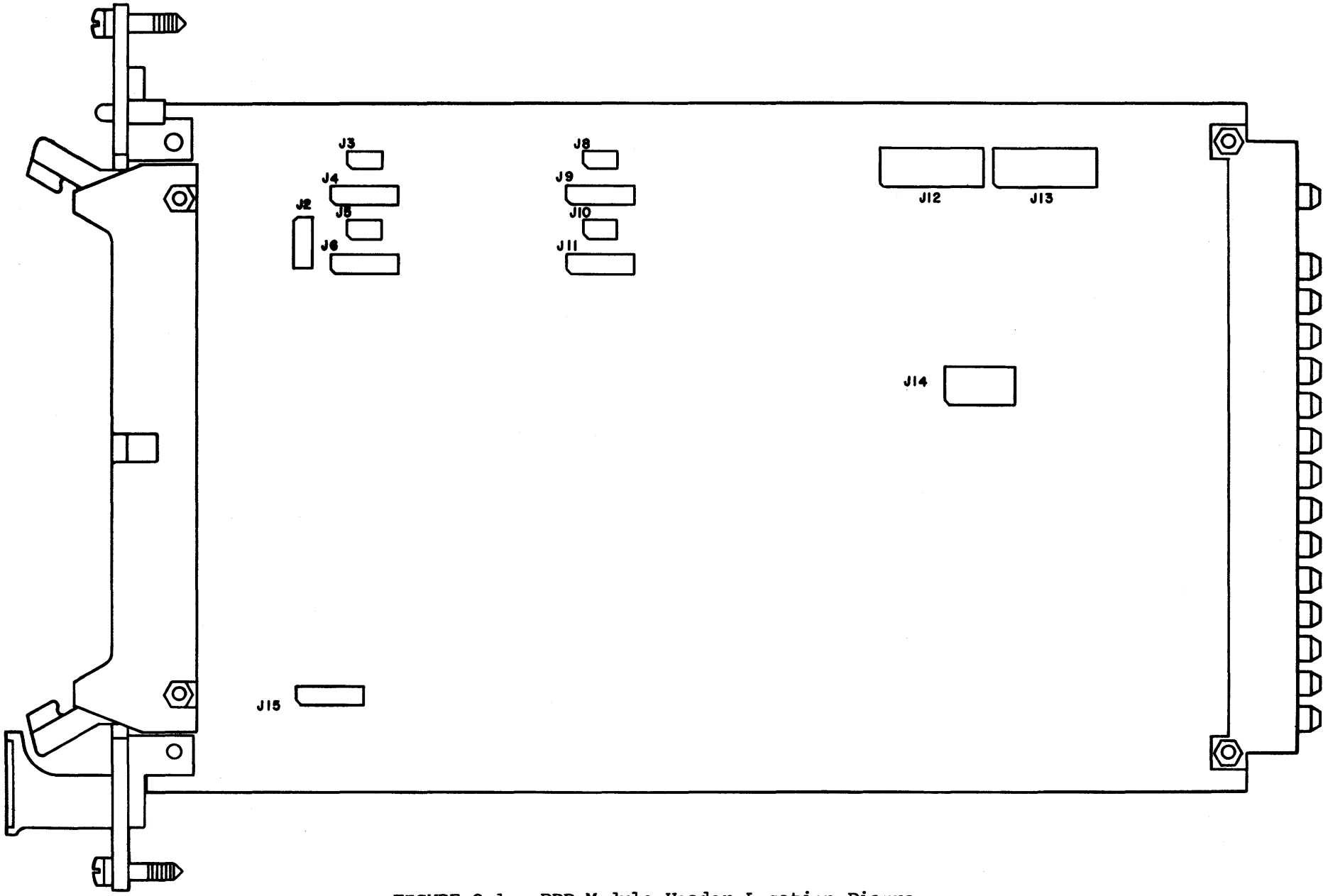


FIGURE 2-1. DPP Module Header Location Diagram

TABLE 2-1. DPP Module Headers

HEADER NUMBER	FUNCTION	FACTORY CONFIGURATION
J2	LED monitor	2-3
J3	Port 1 (P1CA2, P1PA0-P1PA7) direction	1-2
J4	Port 1 (P1CA2, P1PA0-P1PA7) direction	1-2
J5	Port 1 (P1CB2, P1PB0-P1PB7) direction	1-2
J6	Port 1 (P1CB2, P1PB0-P1PB7) direction	No jumper
J8	Port 2 (P2CA2, P2PA0-P2PA7) direction	1-2
J9	Port 2 (P2CA2, P2PA0-P2PA7) direction	1-2
J10	Port 2 (P2CB2, P2PB0-P2PB7) direction	1-2
J11	Port 2 (P2CB2, P2PB0-P2PB7) direction	No jumper
J12	Interrupt select	2-4, 7-9
J13	Interrupt select	3-5, 8-10
J14	Base address select	No jumper
J15	LED control	2-3

2.3.1 LED Monitor Header (J2)

Header J2 is jumpered between pins 2 and 3, as shown in Figure 2-2, and should not be altered.

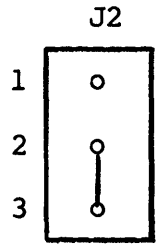


FIGURE 2-2. LED Monitor Header (J2)

2.3.2 Port 1 Direction Headers (J3, J4)

Headers J3 and J4 together control the direction of signal lines P1CA2 and P1PA0-P1PA7. The factory configuration of each header is shown in Figure 2-3. Table 2-2 lists the jumper configurations that determine whether the lines are inputs or outputs.

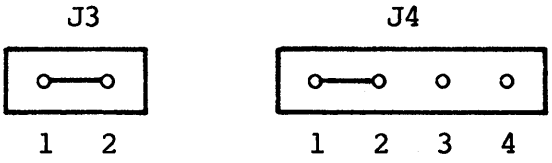


FIGURE 2-3. Port 1 Direction Headers (J3, J4)

TABLE 2-2. Headers J3 and J4 Configurations

HEADER JUMPER	PINS CONNECTED	REMARKS
J3	none	P1CA2 is not used; P1PA0-P1PA7 are outputs.
J4	1-2	
J3	none	P1CA2 is not used; P1PA0-P1PA7 are inputs when U8-39 (CA2) is high, and outputs when U8-39 (CA2) is low.
J4	2-3	
J3	none	P1CA2 is an input; P1PA0-P1PA7 are inputs.
J4	3-4	
J3	none	P1CA2 is an input; P1PA0-P1PA7 are outputs.
J4	1-2, 3-4	
J3	none	P1CA2 is not used; P1PA0-P1PA7 are inputs.
J4	none	
J3	1-2	P1CA2 is an output; P1PA0-P1PA7 are inputs.
J4	none	
J3	1-2 (1)	P1CA2 is an output; P1PA0-P1PA7 are outputs.
J4	1-2 (1)	

NOTE: (1) Factory-installed jumper placement.

2.3.3 Port 1 Direction Headers (J5, J6)

Headers J5 and J6 together control the direction of signal lines P1CB2 and P1PB0-P1PB7. The factory configuration of each header is shown in Figure 2-4. Table 2-3 lists the jumper configurations that determine whether the lines are inputs or outputs.

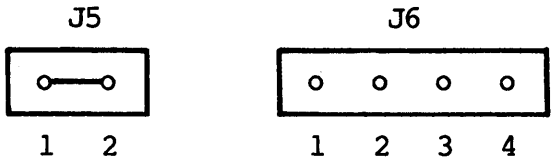


FIGURE 2-4. Port 1 Direction Headers (J5, J6)

TABLE 2-3. Headers J5 and J6 Configurations

HEADER JUMPER	PINS CONNECTED	REMARKS
J5	none	P1CB2 is not used; P1PB0-P1PB7 are outputs.
J6	1-2	
J5	none	P1CB2 is not used; P1PB0-P1PB7 are inputs when U8-19 (CB2) is high, and outputs when U8-19 (CB2) is low.
J6	2-3	
J5	none	P1CB2 is an input; P1PB0-P1PB7 are inputs.
J6	3-4	
J5	none	P1CB2 is an input; P1PB0-P1PB7 are outputs.
J6	1-2, 3-4	
J5	none	P1CB2 is not used; P1PB0-P1PB7 are inputs.
J6	none	
J5	1-2 (1)	P1CB2 is an output; P1PB0-P1PB7 are inputs.
J6	none (1)	
J5	1-2	P1CB2 is an ouput; P1PB0-P1PB7 are outputs.
J6	1-2	

NOTE: (1) Factory-installed jumper placement.

2.3.4 Port 2 Direction Headers (J8, J9)

Headers J8 and J9 together control the direction of signal lines P2CA2 and P2PA0-P2PA7. The factory configuration of each header is shown in Figure 2-5. Table 2-4 lists the jumper configurations that determine whether the lines are inputs or outputs.

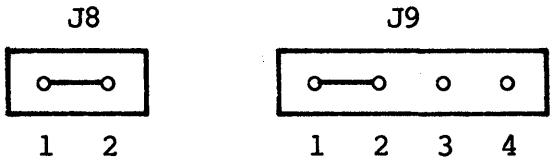


FIGURE 2-5. Port 2 Direction Headers (J8, J9)

TABLE 2-4. Headers J8 and J9 Configurations

HEADER JUMPER	PINS CONNECTED	REMARKS
J8	none	P2CA2 is not used; P2PA0-P2PA7 are outputs.
J9	1-2	
J8	none	P2CA2 is not used; P2PA0-P2PA7 are inputs when U10-39 (CA2) is high, and outputs when U10-39 (CA2) is low.
J9	2-3	
J8	none	P2CA2 is an input; P2PA0-P2PA7 are inputs.
J9	3-4	
J8	none	P2CA2 is an input; P2PA0-P2PA7 are outputs.
J9	1-2, 3-4	
J8	none	P2CA2 is not used; P2PA0-P2PA7 are inputs.
J9	none	
J8	1-2	P2CA2 is an output; P2PA0-P2PA7 are inputs.
J9	none	
J8	1-2 (1)	P2CA2 is an output; P2PA0-P2PA7 are outputs.
J9	1-2 (1)	

NOTE: (1) Factory-installed jumper placement.

2.3.5 Port 2 Direction Headers (J10, J11)

Headers J10 and J11 together control the direction of signal lines P2CB2 and P2PB0-P2PB7. The factory configuration of each header is shown in Figure 2-6. Table 2-5 lists the jumper configurations that determine whether the lines are inputs or outputs.

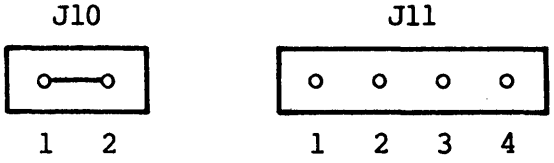


FIGURE 2-6. Port 2 Direction Headers (J10, J11)

TABLE 2-5. Headers J10 and J11 Configurations

HEADER JUMPER	PINS CONNECTED	REMARKS
J10	none	P2CB2 is not used; P2PB0-P2PB7 are outputs.
J11	1-2	
J10	none	P2CB2 is not used; P2PB0-P2PB7 are inputs when U10-19 (CB2) is high, and outputs when U10-19 (CB2) is low.
J11	2-3	
J10	none	P2CB2 is an input; P2PB0-P2PB7 are inputs.
J11	3-4	
J10	none	P2CB2 is an input; P2PB0-P2PB7 are outputs.
J11	1-2, 3-4	
J10	none	P2CB2 is not used; P2PB0-P2PB7 are inputs..
J11	none	
J10	1-2 (1)	P2CB2 is an output; P2PB0-P2PB7 are inputs.
J11	none (1)	
J10	1-2	P2CB2 is an output; P2PB0-P2PB7 are outputs.
J11	1-2	

NOTE: (1) Factory-installed jumper placement.

2.3.6 Interrupt Select Headers (J12, J13)

Headers J12 and J13 together determine which PIA signal or signals -- [IRQ1A*], [IRQ1B*], [IRQ2A*], or [IRQ2B*] -- will drive which I/O Channel interrupt line (INT1*-INT4*). One, any combination, or all of the PIA signals can be connected to a single I/O Channel interrupt line at the same time, but a single PIA signal should not be connected to more than one I/O Channel interrupt line.

The two headers comprise four sets of six contacts (1-6 and 7-12). Each set of six contacts controls one PIA to I/O Channel connection. The factory configuration of each header is shown in Figure 2-7. Table 2-6 lists the jumper configurations that determine PIA signal to I/O interrupt line connections.

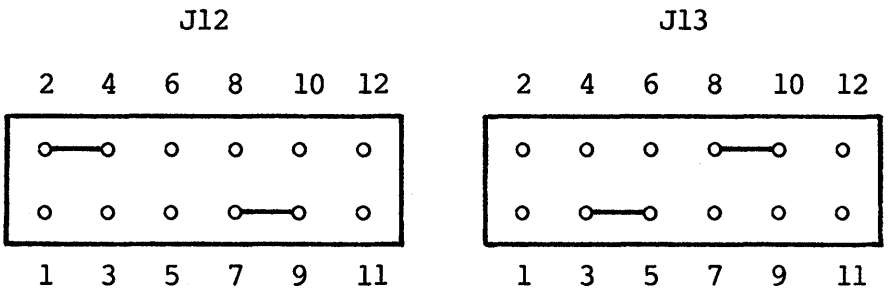


FIGURE 2-7. Interrupt Select Headers (J12, J13)

TABLE 2-6. Headers J12 and J13 Configurations

HEADER JUMPER	PINS CONNECTED	REMARKS
J12	1-3	[IRQ1A*] connected to INT2*
J12	2-4 (1)	[IRQ1A*] connected to INT1*
J12	3-5	[IRQ1A*] connected to INT3*
J12	4-6	[IRQ1A*] connected to INT4*
J12	7-9 (1)	[IRQ1B*] connected to INT2*
J12	8-10	[IRQ1B*] connected to INT1*
J12	9-11	[IRQ1B*] connected to INT3*
J12	10-12	[IRQ1B*] connected to INT4*
J13	1-3	[IRQ2A*] connected to INT2*
J13	2-4	[IRQ2A*] connected to INT1*
J13	3-5 (1)	[IRQ2A*] connected to INT3*
J13	4-6	[IRQ2A*] connected to INT4*
J13	7-9	[IRQ2B*] connected to INT2*
J13	8-10 (1)	[IRQ2B*] connected to INT1*
J13	9-11	[IRQ2B*] connected to INT3*
J13	10-12	[IRQ2B*] connected to INT4*

NOTE: (1) Factory installed jumper placement.

2.3.7 Base Address Select Header (J14)

Header J14 can be configured to have the DPP occupy any $10 byte block within the first $100 byte block of the I/O Channel memory map (see Figure 4-2). Each of the two ports appears twice in the $10 byte block. The factory configuration of the header is shown in Figure 2-8. Table 2-7 lists the jumper configurations that select the desired location within the I/O Channel memory map.

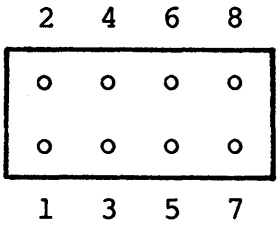


FIGURE 2-8. Base Address Select Header (J14)

TABLE 2-7. Header J14 Configurations

PINS CONNECTED	REMARKS
1-2, 3-4, 5-6, 7-8	Base address is $00
1-2, 3-4, 5-6	Base address is $10
1-2, 3-4, 7-8	Base address is $20
1-2, 3-4	Base address is $30
1-2, 5-6, 7-8	Base address is $40
1-2, 5-6	Base address is $50
1-2, 7-8	Base address is $60
1-2	Base address is $70
3-4, 5-6, 7-8	Base address is $80
3-4, 5-6	Base address is $90
3-4, 7-8	Base address is $A0
3-4	Base address is $B0
5-6, 7-8	Base address is $C0
5-6	Base address is $D0
7-8	Base address is $E0
none (1)	Base address is $F0

NOTE: (1) Factory-installed jumper placement.

2.3.8 LED Control Header (J15)

The configuration of header J15 controls front panel FAIL LED indicator DS1 and signal [P1PB7]. When the LED can be turned on by the [LED] signal, the [P1PB7] signal is disabled (refer to the schematic diagram in Chapter 5). When the [P1PB7] signal is enabled, the [LED] signal is low and will hold the LED off. The factory configuration of the header is shown in Figure 2-9. Table 2-8 lists the jumper configurations that select the desired condition.

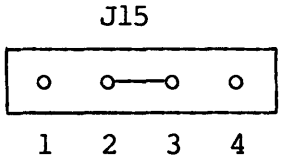


FIGURE 2-9. LED Control Header (J15)

TABLE 2-8. Header J15 Configurations

PINS CONNECTED	REMARKS
2-3 (1)	FAIL LED is functionally operational and signal [P1PB7] is disabled.
1-2 3-4	Signal [P1PB7] is enabled and FAIL LED is disabled.

NOTE: (1) Factory-installed jumper placement. If J6-1 and 2 are connected and J15-2 and 3 are connected, then J15-4 should be connected to J15-3.

2.4 INSTALLATION INSTRUCTIONS

When the DPP has been configured as desired by the user, it is ready to be installed in a VME chassis or an I/Omodule 5-slot card cage.

2.4.1 Installation in VME Chassis

The DPP is installed in a VME chassis as follows:

a. Turn all equipment power OFF.

CAUTION

CONNECTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

b. Insert DPP in any single-width card slot.

c. Secure in place with two captive screws.

d. Peripheral connection to DPP port 1 and/or port 2 is accomplished by mating a double-row, 50-pin, female ribbon connector, such as a 3M 3425-5000, to male connectors J1 and J16 on the DPP front panel, as shown in Figure 2-10. Printer cable assembly, Motorola part number M68KVMPRTCE, can be used. Connect the other end of the ribbon cable to a printer with a Centronics printer-compatible interface.

e. Equipment power may be turned ON.

2.4.2 Installation in 5-Slot I/Omodule Card Cage

The DPP is installed in a 5-slot I/Omodule card cage as follows:

a. Turn all equipment power OFF.

CAUTION

CONNECTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

b. If card cage in part of VERSAmodule chassis, remove card slot cover plate.

c. Insert DPP in slot and secure with two captive screws.

d. Peripheral connection to DPP port 1 and/or port 2 is accomplished by mating a double-row, 50-pin, female ribbon connector, such as a 3M 3425-5000, to male connectors J1 and J16 on the DPP front panel, as shown in Figure 2-10. Printer cable assembly, Motorola part number M68KVMPRTCE, can be used. Connect the other end of the ribbon cable to a printer with a Centronics printer-compatible interface.

e. Equipment power may be turned ON.

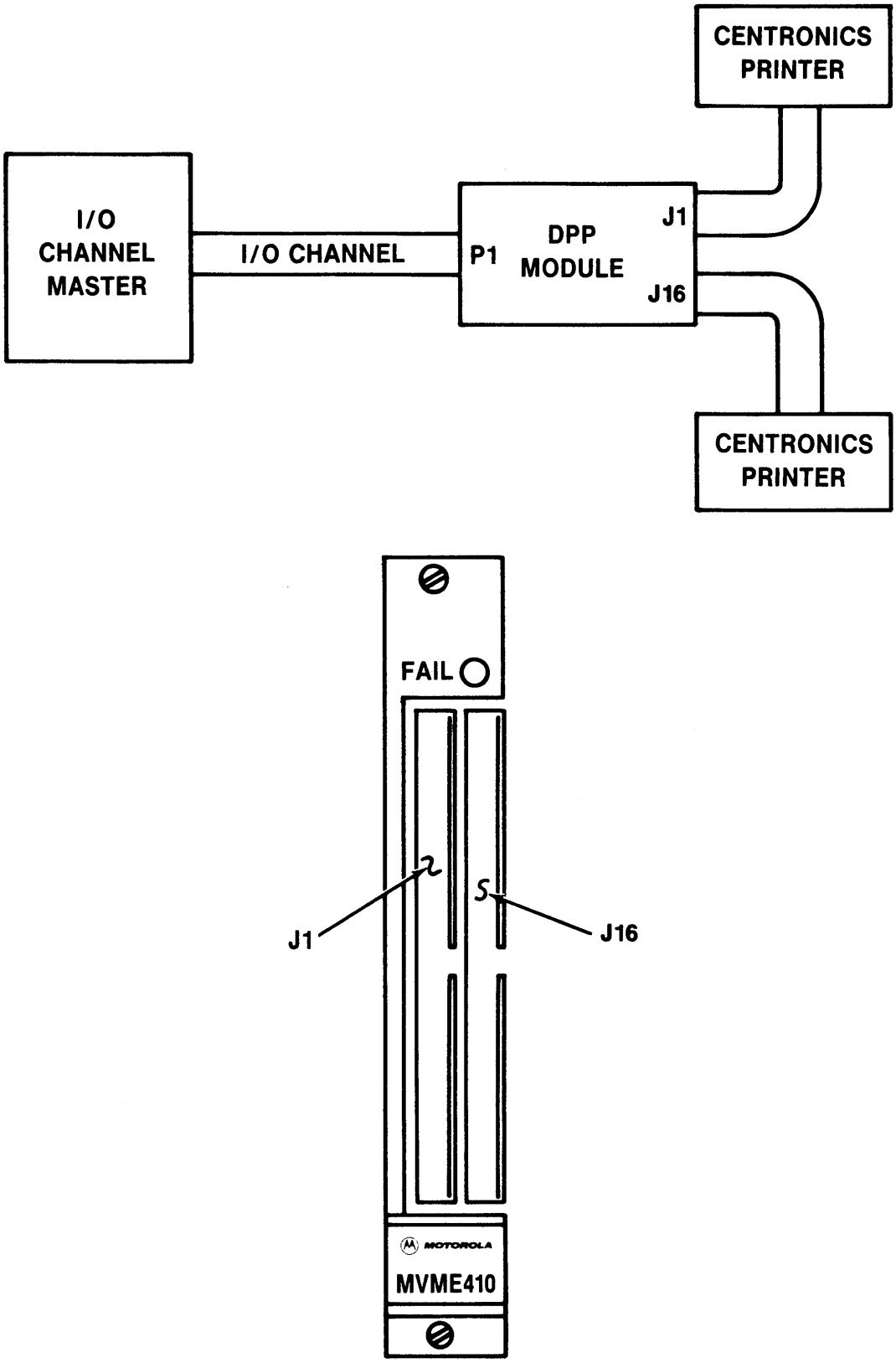


FIGURE 2-10. Typical DPP Interface Cabling Diagram

CHAPTER 3

OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the necessary information to initialize and operate the Dual Parallel Port Module in a typical system.

3.2 INDICATOR

The DPP contains one indicator -- a front panel red FAIL LED. If header J15 is jumpered between pins 2-3, the FAIL indicator will illuminate when an I/O Channel reset or a software-controlled module failure occurs.

3.3 OPERATING PROCEDURE

Following is a typical procedure showing how to use the DPP to interface with a Centronics printer.

a. Apply power to the system equipment.

b. Select the printer.

c. If the VERSAmodule contains VERSAbug EPROM's, then the VERSAbug 2.0 Printer Attach (PA) command can now be used.

d. Figure 3-1 is a typical driver routine that can be used to drive the printer.

```
                        ************************************************************************
                        *        VM02 RTTLIO PARALLEL PORT 1 INITIALIZATION ROUTINE            *
                        ************************************************************************
                        *FUNCTION:  Initialize Parallel Port 1 of the RTTLIO for driving a     *
                        *printer.                                                              *
                        ************************************************************************
                        *INPUT PARAMETERS:  NONE                                               *
                        ************************************************************************
                        *OUTPUT PARAMETERS: NONE                                               *
                        ************************************************************************
                        *REGISTERS ALTERED: NONE                                               *
                        ************************************************************************

            00001000    THISPR    EQU     $1000                 START OF THIS PROGRAM
            00F801E1    PBASE     EQU     $F801E1               BASE ADDRESS OF PARALLEL PORT 1
            00000000    PDATA     EQU     $0                    OFFSET OF A SIDE PERIPHERAL DATA REG.  FROM BASE
            00000004    PDATB     EQU     $4                    OFFSET OF B SIDE PERIPHERAL DATA REG.  FROM BASE
            00000002    PCNTRLA   EQU     $2                    OFFSET OF A SIDE CONTROL REGISTER FROM BASE
            00000006    PCNTRLB   EQU     $6                    OFFSET OF B SIDE CONTROL REG.  FROM BASE
            00000002    PSTATA    EQU     PCNTRLA               OFFSET OF A SIDE STATUS REGISTER FROM BASE
            00000006    PSTATB    EQU     PCNTRLB               OFFSET OF B SIDE STATUS  REG.  FROM BASE
            00000000    PDDRA     EQU     PDATA                 OFFSET OF A SIDE DATA DIRECTION REG.  FROM BASE
            00000004    PDDRB     EQU     PDATB                 OFFSET OF B SIDE DATA DIRECTION REG.  FROM BASE

            00001000              ORG     THISPR
00001000    00000000    INITPIA   DS.W    0
00001000 2F08           INITSAVE  MOVE.L  A0,-(A7)              GET SOME WORKING REGISTERS
00001002 40E7                     MOVE.W  SR,-(A7)              SAVE 68000 STATUS REG

00001004 41F900F801E1             LEA     PBASE,A0              POINT A0 AT PORT 1

0000100A 117C00380002 INITDDRA    MOVE.B  #$38,PCNTRLA(A0)      POINT AT DDRA
00001010 10BC00FF                 MOVE.B  #$FF,PDDRA(A0)        DDRA MAKES PERPH DATA A OUTPUTS

00001014 117C003C0002 INITCTRA    MOVE.B  #$3C,PCNTRLA(A0)      CA2=OUTPUT(HIGH RIGHT NOW), SET FLAG
                      *                                       ON LOW TO HIGH, INT DISABLED

0000101A 117C00380006 INITDDRB    MOVE.B  #$38,PCNTRLB(A0)      POINT AT DDRB
00001020 117C00000004             MOVE.B  #$00,PDDRB(A0)        DDRB MAKES PERPH DATA B INPUTS

00001026 117C003C0006 INITCTRB    MOVE.B  #$3C,PCNTRLB(A0)      CB2=OUTPUT(HIGH RIGHT NOW), SET FLAG
                      *                                       ON LOW TO HIGH, INT DISABLED

0000102C 46DF         INITRSTR    MOVE.W  (A7)+,SR              RESTORE 68000 STATUS REGISTER
0000102E 205F                     MOVE.L  (A7)+,A0              RESTORE A0

00001030 4E75                     RTS
```

FIGURE 3-1. Typical Printer Driver Routine (Sheet 1 of 3)

```
MOTOROLA M68000 ASM VERSION  1.30SMD :   50.RTTLIO  .DRIVER  .SA 08/09/82 14:52:12

                        ********************************************************************
                        *        VM02 PRINTER DRIVER USING THE RTTLIO PARALLEL PORT 1       *
                        ********************************************************************
                        *FUNCTION:  Send the character contained in D0 to a Printer through  *
                        *an RTTLIO board(Board strapped to appear at Block 15).  If the      *
                        *Printer is not selected then return from this subroutine with D1.B= *
                        *Non-zero.  If the printer is selected and the character is sent     *
                        *successfully then return with D1.B=zero                            *
                        ********************************************************************
                        *INPUT PARAMETERS:  D0.B CONTAINS THE ASCII CODE OF THE CHARACTER TO *
                        *BE SENT.                                                           *
                        ********************************************************************
                        *OUTPUT PARAMETERS:  BIT 0 OF D1 = 0 IF THE PRINTER IS NOT SELECTED, *
                        *BIT 1 OF D1 = 1 IF THE PRINTER IS OUT OF PAPER.     D1.B = $01 IF   *
                        *THE PRINTER WAS SELECTED, WAS NOT OUT OF PAPER, AND THE CHARACTER   *
                        *WAS SENT SUCCESSFULLY.  IF NO ACKNOWLEDGE IS EVER RECIEVED THEN THIS*
                        *ROUTINE IS NEVER EXITED.                                           *
                        ********************************************************************
                        *REGISTERS ALTERED: D1.B                                            *
                        ********************************************************************

           00000002     PACKN    EQU      PSTATA              OFFSET OF A SIDE STATUS REG. FROM BASE
           00000002     PSTRB    EQU      PCNTRLA             OFFSET OF A SIDE CONTROL REG. FROM BASE
           00000004     PRDY     EQU      PDATB               OFFSET OF B SIDE PERIPHERAL DATA REG. FROM BASE

00001032 00000000       PCHAR    DS.W     0
00001032 48E72080       PSAVE    MOVEM.L  D2/A0,-(A7)         GET SOME WORKING REGISTERS
00001036 40E7                    MOVE.W   SR,-(A7)            SAVE 68000 STATUS REGISTER

00001038 41F900F801E1            LEA      PBASE,A0            A0=BASE ADDRESS OF PORT 1

0000103E 14280004                MOVE.B   PRDY(A0),D2         GET THE STATUS OF PAPER AND SELECT
00001042 02020003                AND.B    #%00000011,D2       PAPER OUT=BIT 1,SELECT=BIT 0
00001046 1202                    MOVE.B   D2,D1               SAVE RESULTS IN D1 AS OUTPUT PARAMETER
00001048 5302                    SUB.B    #$01,D2             IF PRINTER NOT SELECTED OR PAPER OUT
0000104A 6618                    BNE.S    PRSTR               THEN RETURN WITH D1.B#$01(ERROR)

0000104C 1080           PSEND    MOVE.B   D0,PDATA(A0)        ELSE SEND CHARACTER TO PRINTER

0000104E 1410           PACKNCLR MOVE.B   PDATA(A0),D2        DO DUMMY READ OF PIA PERIPHERAL DATA
                        *                                REGISTER IN ORDER TO CLEAR ACKNOWLEGDE FLAG
```

FIGURE 3-1. Typical Printer Driver Routine (Sheet 2 of 3)

```
 93
 94   00001050 117C00340002 PSTROBE  MOVE.B   #$34,PSTRB(A0)          MAKE DATA STROBE GO LOW
 95   00001056 117C003C0002          MOVE.B   #$3C,PSTRB(A0)          THEN HIGH
 96
 97   0000105C 082800070002 PACKNGE  BTST.B   #7,PACKN(A0)            IF CHARACTER NOT ACKNOWLEDGED
 98   00001062 67F8                  BEQ.S    PACKNGE                 THEN WAIT FOR IT TO BE
 99
100   00001064 46DF          PRSTR   MOVE.W   (A7)+,SR                RESTORE 68000 STATUS REGISTER
101   00001066 4CDF0104              MOVEM.L  (A7)+,D2/A0             RESTORE REGISTERS
102
103   0000106A 4E75          PRTRN   RTS
104
105                                  END
```

```
MOTOROLA M68000 ASM VERSION  1.30SMD :  50.RTTLIO   DRIVER  .SA 08/09/82 14:52:12

SYMBOL TABLE LISTING

SYMBOL NAME     SECT   VALUE       SYMBOL NAME     SECT   VALUE

INITCTRA               00001014    PDATA                  00000000
INITCTRB               00001026    PDATB                  00000004
INITDDRA               0000100A    PDDRA                  00000000
INITDDRB               0000101A    PDDRB                  00000004
INITPIA                00001000    PRDY                   00000004
INITRSTR               0000102C    PRSTR                  00001064
INITSAVE               00001000    PRTRN                  0000106A
PACKN                  00000002    PSAVE                  00001032
PACKNCLR               0000104E    PSEND                  0000104C
PACKNGE                0000105C    PSTATA                 00000002
PBASE                  00F801E1    PSTATB                 00000006
PCHAR                  00001032    PSTRB                  00000002
PCNTRLA                00000002    PSTROBE                00001050
PCNTRLB                00000006    THISPR                 00001000
```

FIGURE 3-1. Typical Printer Driver Routine (Sheet 3 of 3)

CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides the overall block diagram level descriptions for the Dual Parallel Port Module. A general description provides an overview of the module, followed by a detailed description of each section of the DPP.

4.2 GENERAL DESCRIPTION

The DPP is designed to provide a parallel interface between an I/O Channel (bus) master and one or two printers, with a Centronics interface.

The DPP employs an MC6821 chip to latch output printer data, drive printer control lines, and monitor printer handshake and status lines. The MC6821 data sheet contains additional information on the MC6821.

The DPP provides two general-purpose, parallel, printer ports. Figure 4-1 is a block diagram of the DPP. As shown in Figure 4-1, the DPP has a common I/O Channel interface section and two parallel port sections. Each of the parallel port sections consists of a peripheral interface adapter (PIA) with TTL buffers that provide drive capability on the peripheral side. The two parallel ports are identical except for a FAIL LED indicator that is strappable to port 1.

4.3 I/O CHANNEL INTERFACE

The I/O Channel interface section provides map decoding logic, access control logic, and interrupt logic. An explanation of each follows.

4.3.1 Map Decoding Logic

The DPP is strap-selectable to appear at any $10 byte block within the first $100 byte block of the I/O Channel memory map, as shown in Figure 4-2. If the selected base address is $C0 the $10 block byte upper boundary is one bit less than $D0. Each port appears twice in the $10 byte area. To set the base address of the DPP, see block select header J14 information in Chapter 2.

Table 4-1 shows the addresses of the registers within each of the DPP parallel ports with respect to the DPP base address.

4.3.2 Access Control Logic

The access control logic provides an asynchronous I/O Channel to a synchronous MC68B21 interface. The interface operation is transparent to software on the I/O Channel master.

4.3.3 Interrupt Logic

Each of the two PIA's has two lines -- [IRQ1A*] and [IRQ1B*], and [IRQ2A*] and IRQ2B*]. One or more of these signals can be strapped to drive one of the I/O Channel interrupt lines, INT1*-INT4*. The various combinations are controlled by interrupt select headers J12 and J13 (see Chapter 2).

If a port is connected to a printer, it may be software configured to drive [IRQ1A*] when the printer gives an acknowledge, and/or to drive [IRQ1B*] when the printer indicates a fault condition. Interrupts cannot be caused by the BUSY, PAPER OUT, or SELECT lines from the printer. They are brought in only as peripheral data inputs to the B side of the PIA.

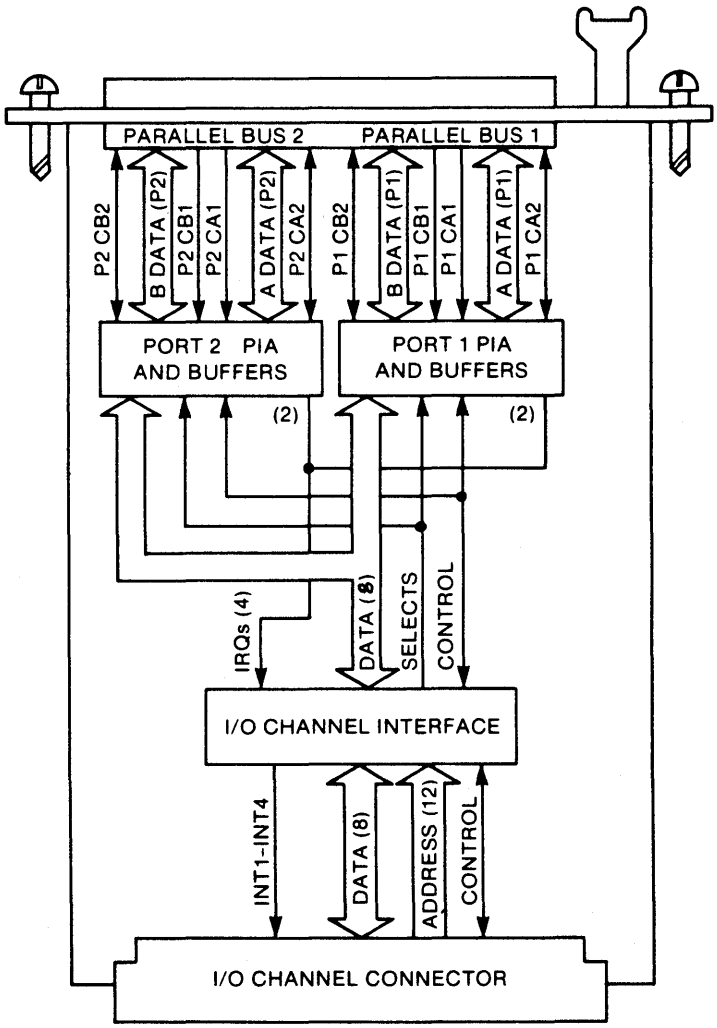


FIGURE 4-1. DPP Module Block Diagram

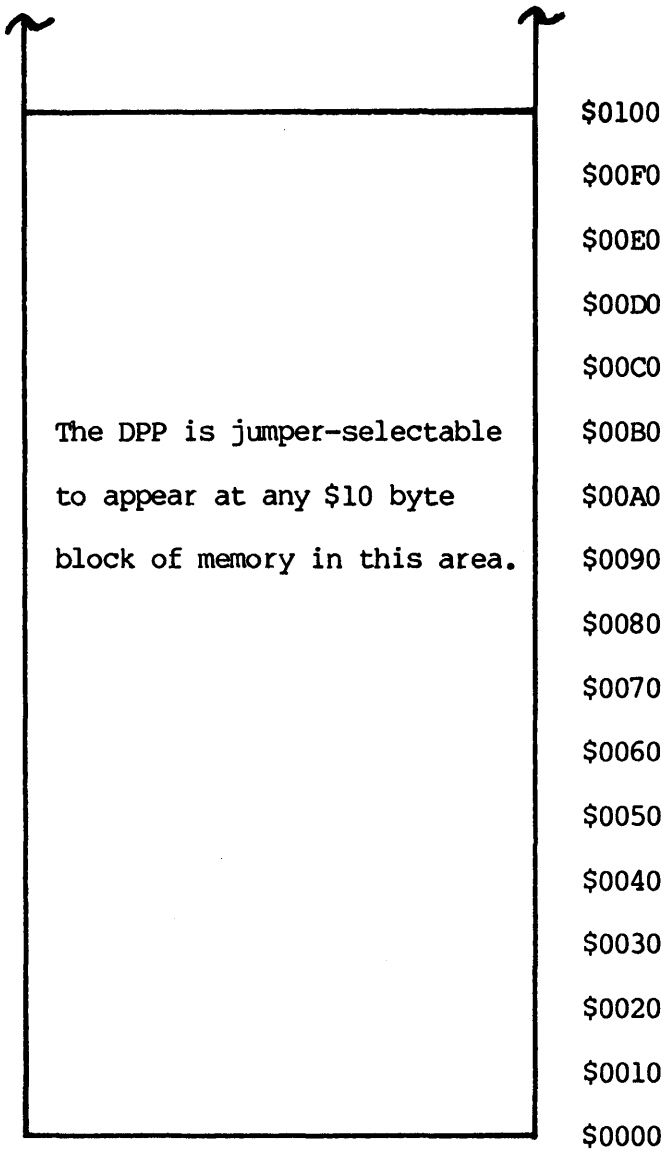


FIGURE 4-2. I/O Channel Memory Map

TABLE 4-1. DPP Module Register Addresses

OFFSET FROM DPP MODULE BASE ADDRESS	CONTROL REGISTER BIT CRA-2	CONTROL REGISTER BIT CRB-2	REGISTER	PORT #
F	X	X	Control register B	2
E	X	0	Data direction register B	2
E	X	1	Peripheral register B	2
D	X	X	Control register A	2
C	0	X	Data direction register A	2
C	1	X	Peripheral register A	2
B	X	X	Control register B	1
A	X	0	Data direction register B	1
A	X	1	Peripheral register B	1
9	X	X	Control register A	1
8	0	X	Data direction register A	1
8	1	X	Peripheral register A	1
7	X	X	Control register B	2
6	X	0	Data direction register B	2
6	X	1	Peripheral register B	2
5	X	X	Control register A	2
4	0	X	Data direction register A	2
4	1	X	Peripheral register A	2
3	X	X	Control register B	1
2	X	0	Data direction register B	1
2	X	1	Peripheral register B	1
1	X	X	Control register A	1
0	0	X	Data direction register A	1
0	1	X	Peripheral register A	1

NOTE: X denotes a don't care condition.

4.4 PARALLEL PORT 1

Parallel port 1 employs an MC68B21 (PIA) for its logic functions. The MC6821 Data Sheet explains how to use it. Pay particular attention to the sections that deal with programming the PIA. In addition to the information provided in the PIA manual, the following information is necessary to use the DPP.

All the peripheral data and peripheral control lines on the PIA are buffered with TTL drivers/receivers. Because these lines are buffered, care must be taken to make the directions of the peripheral line coming from the PIA compatible with the direction of the buffer on that line.

CA1 (U8-40) and CB1 (U8-18) are buffered to become P1CA1 and P1CB1, respectively. Their buffers are always inputs, as defined by the PIA; therefore, no buffer fight can ever exist on these lines.

CA2 (U8-39) and CB2 (U8-19) are buffered to become P1CA2 and P1CB2, respectively. Each one can be programmed as an input or as an output in the PIA. Each PIA TTL buffer is hardware strappable as an input or as an output. Therefore, the possibility of a buffer fight exists for one case only -- when the line is programmed as an output by the PIA and its TTL buffer is strapped as an input. Consequently, the programmed direction of the line and the strapped direction of the line should be the same. For direction strapping, see the port 1 information in Chapter 2.

PA0-PA7 are buffered to become P1PA0-P1PA7, respectively. The direction of each one of these lines is individually programmable within the PIA. However, the direction of their buffers is not individually strappable in hardware. The buffers for these lines are strapped as either all inputs or as all outputs, or they are strapped so that their direction is an input when CA2 is at a logic high or an output when CA2 is at a logic low. The possibility for a buffer fight exists for any case in which a line is programmed as an output and the buffers are strapped/programmed as inputs. The programmed direction of the lines and the strapped/programmed direction of the buffers should be the same. For direction strapping, see the port 1 information in Chapter 2.

PB0-PB7 relate to P1PB0-P1PB7 in the same way that PA0-PA7 relate to P1PA0-P1PA7 with the following exception. When J15 is strapped such that [PB7] controls the FAIL LED indicator, then PB7 is severed from [P1PB7], and it may be programmed as an output even though the direction of the P1PB0-P1PB7 buffers may be inputs. In this configuration, driving PB7 low turns on the FAIL LED and driving PB7 high turns off the FAIL LED.

4.5 PARALLEL PORT 2

Parallel port 2 is identical to parallel port 1 except that port 2 does not have a FAIL LED indicator connectable to PB7. Therefore, the special case covered in the port 1 explanation with respect to the LED does not apply to port 2.

4.6 LIMITATIONS

Following are certain options of the MC6821 which are not supported by the DPP.

a. The direction of port 1 CA2 or port 2 CA2 is hardware strappable but not dynamically alterable.

b. The data direction registers must be configured to set their corresponding peripheral data lines to be a block of eight inputs or a block of eight outputs, depending on the hardware option that is being used. The direction of individual peripheral data lines is not allowed to differ from that of the whole set of eight peripheral data lines.

c. The Read Strobe with E Restore mode of the PIA will cause a 250-ns pulse that is shorter than the minimum time required by the Centronics data strobe line. This requires that the Set/Reset CA2 mode be used to control the data strobe line to a Centronics printer.

d. The FAIL LED indicator may use PB7 of port 1. If so, PB7 may not be used for peripheral devices.

4.7 MODULE I/O TIMING

Table 4-2 and Figure 4-3 show the performance characteristics of the DPP from the I/O Channel side. All data transfers on the I/O Channel are between the master and a slave, and are initiated by the master. All data transfers are asynchronous and rely on two interlocked signal lines -- STB* and XACK*. STB* is generated by the master and initiates a data transfer. XACK* is generated by the addressed slave to indicate that the data transfer has been acknowledged.

TABLE 4-2. I/O Channel Timing Signal Characteristics

TIMING PARAMETER		VALUE IN NANOSECONDS	
NUMBER	DESCRIPTION	TYPICAL	MAX
1	STB* low to XACK* low	990	1300
2	STB* high to XACK* high	122	184

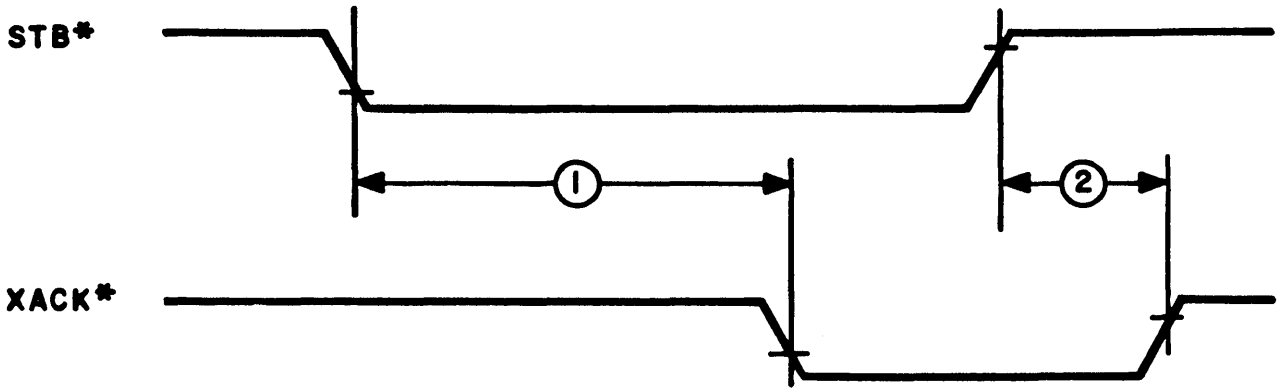


FIGURE 4-3. I/O Channel Side Timing Signal Diagram

4.8 MODULE PERIPHERAL TIMING

Timing characteristics for the PIA are contained in the PIA data sheet. However, the signals used on the DPP peripheral side are buffered. Buffers introduce delays that make some of the characteristics at the peripheral connectors different from the characteristics at the PIA. Those characteristics which are most important are given in Table 4-3. Refer to Figure 4-4 for the related timing diagrams.

TABLE 4-3. Peripheral Timing Signal Characteristics

TIMING PARAMETER		VALUE IN NANOSECONDS	
NUMBER	DESCRIPTION	TYPICAL	MAX
1	Control output pulse width	250	
2	Rise and fall time for PXCB1, PXCB2		N/A
3	Delay time, PXCA1 active transition to PXCA2 positive transition		1036
4	Delay time, data valid to PXCB2 negative transition	14	
5	Control output pulse width	250	
6	Delay time, PXCB1 active transition to PXCB2 positive transition		1036
7	Interrupt input pulse time	500	
8	Interrupt response time		1025

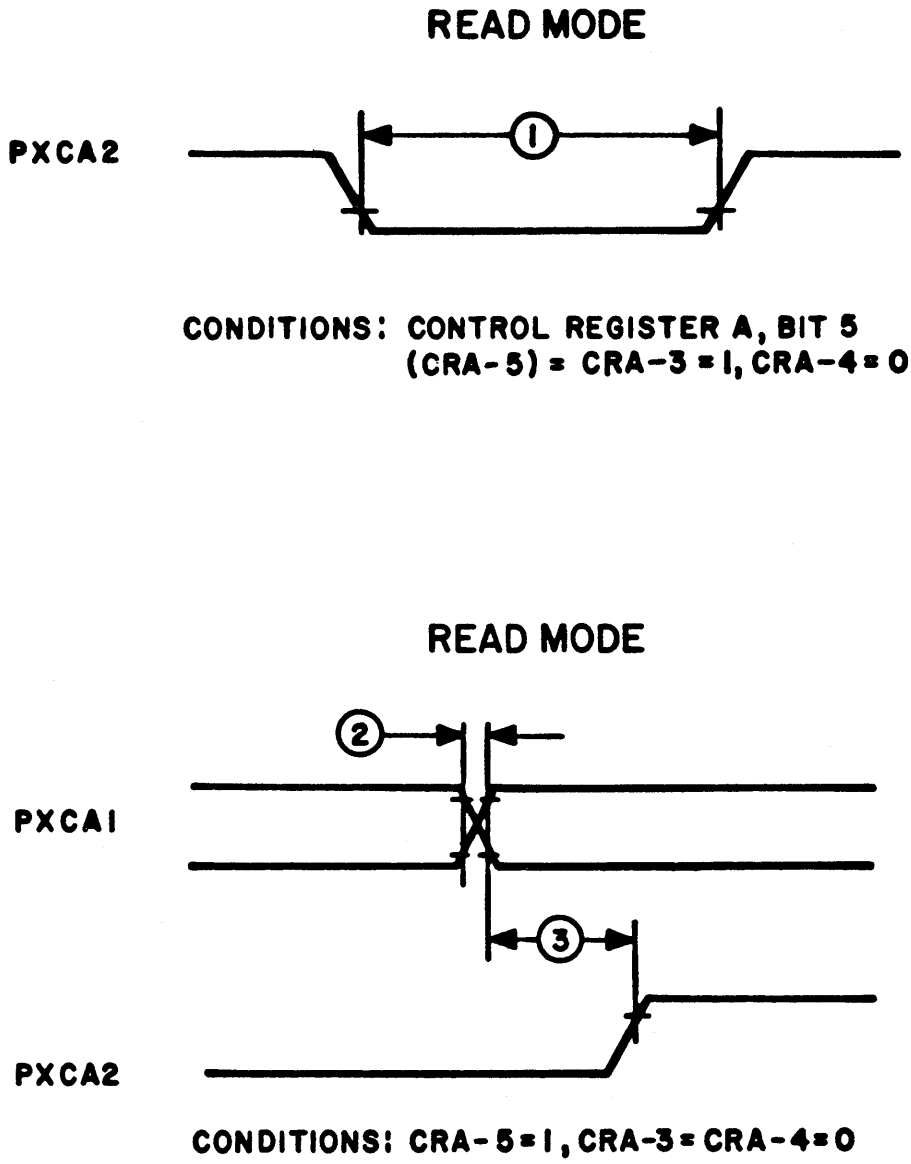
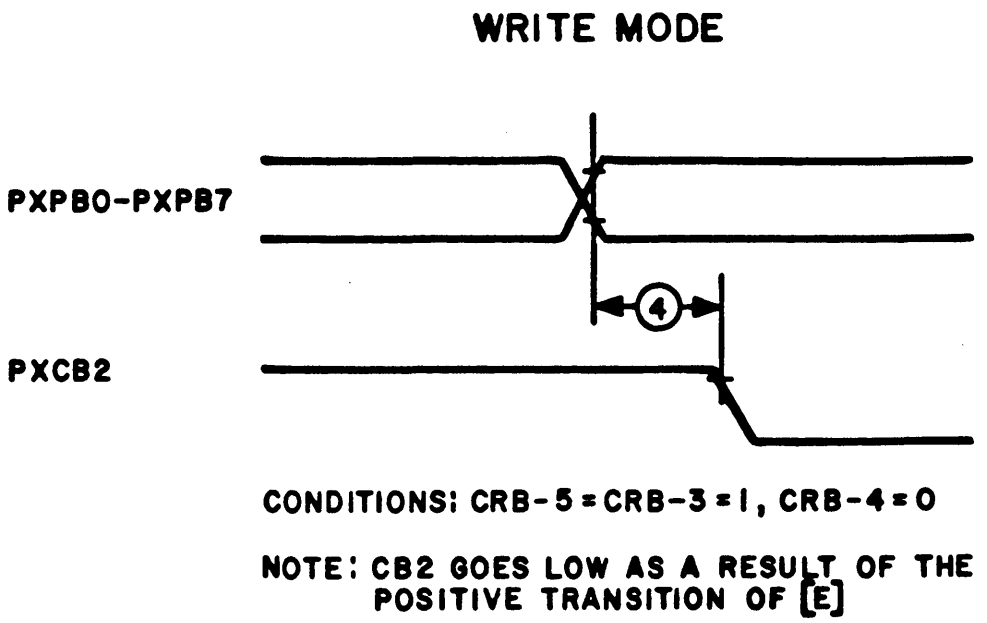


FIGURE 4-4. Peripheral Side Timing Signal Diagram (Sheet 1 of 3)



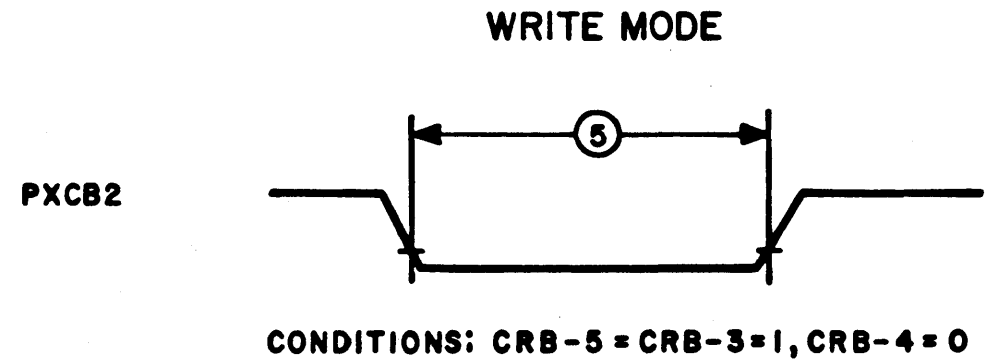
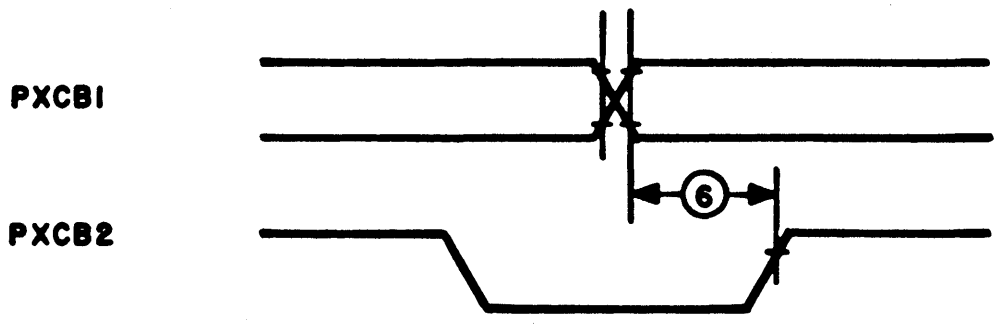


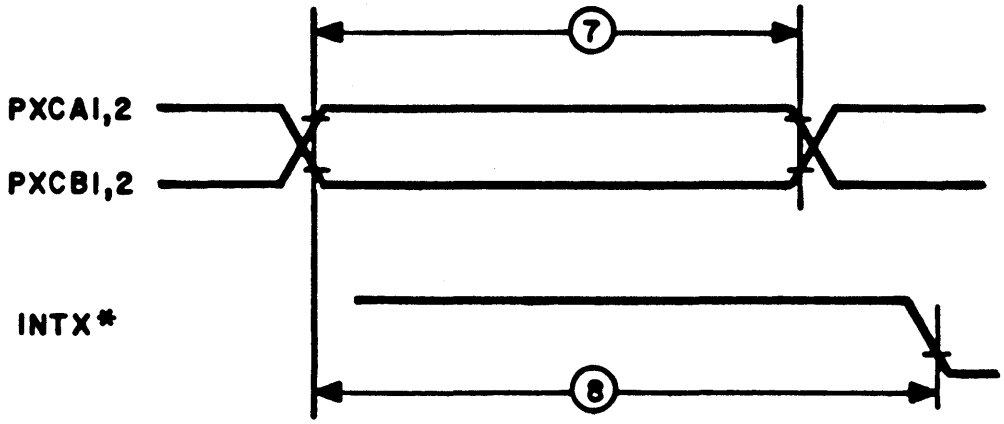
FIGURE 4-4. Peripheral Side Timing Signal Diagram (Sheet 2 of 3)

WRITE MODE



CONDITIONS: CRB-5=1, CRB-3=CRB-4=0

INT* RESPONSE



NOTE: INTX* = THE I/O CHANNEL INTERRUPT (INT 1 - INT 4) THAT IS DRIVEN BY [IRQX*/B*]. ASSUMES THE INTERRUPT ENABLE BITS ARE SET

FIGURE 4-4. Peripheral Side Timing Signal Diagram (Sheet 3 of 3)

CHAPTER 5

SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the connector signal descriptions, parts list and associated parts location diagram, and a schematic diagram for the Dual Parallel Port Module.

5.2 CONNECTOR SIGNAL DESCRIPTIONS

The DPP has three interface connectors -- one to connect it to the I/O Channel and two to connect it to Centronics printer-compatible interface peripheral devices.

5.2.1 I/O Channel Connector

The I/O Channel connector P1 on the DPP is a standard DIN 41612 triple-row, 64-pin, male connector. The backplane/ribbon cable uses the female connector. Table 5-1 lists the connector P1 pin assignments. Additional information on this connector can be obtained from the I/O Channel Specification Manual.

5.2.2 Peripheral Connectors

Front panel connectors J1 and J16 on the DPP are double-row, 50-pin, male connectors. They mate to a female ribbon connector such as a 3M 3425-5000. Table 5-2 lists the front panel connectors J1 and J16 pin assignments by pin number, signal mnemonic, and signal name and description.

5.3 PARTS LIST

Table 5-3 lists the components of the DPP. A parts location diagram for the module is provided in Figure 5-1. This parts list reflects the latest issue of DPP module at the time of printing.

5.4 DIAGRAMS

Figure 5-2 is the schematic diagram for the DPP.

TABLE 5-1. I/O Connector P1 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A10, A17-A19, A24,A25, A31,A32, C11,C20, C25,C31, C32	GND	GROUND
A11	A11	ADDRESS bus (bit 11) - One of 11 input signals used to selectively access the DPP.
A12	A10	ADDRESS bus (bit 10) - Same as bit A11 on pin A11.
A13	A8	ADDRESS bus (bit 8) - Same as bit A11 on pin A11.
A14	A6	ADDRESS bus (bit 6) - Same as bit A11 on pin A11.
A15	A4	ADDRESS bus (bit 4) - Same as bit A11 on pin A11.
A16	A2	ADDRESS bus (bit 2) - Input signal used to select port 1 when low and port 2 when high during a DPP cycle.
A20	D7	DATA bus (bit 7) - Bidirectional signal used to transmit data between the I/O Channel master and the DPP during read and write cycles.
A21	D6	DATA bus (bit 6) - Same as bit D7 on pin A20.
A22	D4	DATA bus (bit 4) - Same as bit D7 on pin A20.
A23	D2	DATA bus (bit 2) - Same as bit D7 on pin A20.
A26,C26	-12V	Not used by DPP.
A27, C8-C10, C27	(Reserved)	Not used by DPP.
A28,C28	+12V	Not used by DPP.
A29,A30, C29,C30	+5V	+5 Vdc Power - Used by the module logic circuits.
C1	INT4*	INTERRUPT REQUEST 4 - One of four active low output signal lines used by the DPP to interrupt the I/O Channel master.
C2	INT3*	INTERRUPT REQUEST 3 - Same as signal INT4* on pin C1.
C3	INT2*	INTERRUPT REQUEST 2 - Same as signal INT4* on pin C1.

TABLE 5-1. I/O Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C4	INT1*	INTERRUPT REQUEST 1 - Same as signal INT4* on pin C1.
C5	IORES*	INPUT/OUTPUT RESET - Active low input signal used to reset the DPP.
C6	XACK*	TRANSMIT ACKNOWLEDGE - Active low output signal used to advise the I/O Channel master that write data is latched or read data is available.
C7	CLK	CLOCK - Free-running input signal used by the DPP for internal synchronization and timing.
C12	A9	ADDRESS bus (bit 9) - Same as bit A11 on pin A11.
C13	A7	ADDRESS bus (bit 7) - Same as bit A11 on pin A11.
C14	A5	ADDRESS bus (bit 5) - Same as bit A11 on pin A11.
C15	A3	ADDRESS bus (bit 3) - Not used.
C16	A1	ADDRESS bus (bit 1) - Same as bit A11 on pin A11.
C17	A0	ADDRESS bus (bit 0) - Same as bit A11 on pin A11.
C18	STB*	STROBE - The high to low transition of this input signal indicates to the DPP that an I/O Channel cycle is starting. The low to high transition indicates to the DPP that the current I/O Channel cycle has ended.
C19	WT*	WRITE - An input signal that is low when the I/O Channel is in a write cycle, and high when the I/O Channel is in a read cycle.
C21	D5	DATA bus (bit 5) - Same as bit D7 on pin A20.
C22	D3	DATA bus (bit 3) - Same as bit D7 on pin A20.
C23	D1	DATA bus (bit 1) - Same as bit D7 on pin A20.
C24	D0	DATA bus (bit 0) - Same as bit D7 on pin A20

TABLE 5-2. Peripheral Connectors J1 and J16 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	PXCB2	INPUT PRIME - A low-level output signal which clears the printer buffer and initializes the logic. (Not used by all printers)
2-6, 10-50 (even numbers)		GROUND
3	GND	GROUND
5	PXCB1	FAULT - A low-level input signal that indicates a printer fault condition such as paper empty, light detect, or a deselect condition. (Not used by all printers)
7,41, 45,49	(Reserved)	N/A
8	(None)	No connection.
9	PXPB7	N/A
11	PXPB6	N/A
13	PXPB5	N/A
15	PXPB4	N/A
17	PXPB3	N/A
19	PXPB2	BUSY - An input signal indicating that the printer cannot receive data.
21	PXPB1	OUT OF PAPER - A high-level input indicating the printer is out of paper.
23	PXPB0	SELECT - A high-level input signal indicating that the printer is selected.
25	PXPA7	PERIPHERAL DATA LINE (PD8) - Output data to printer from PA7 of PIA.
27	PXPA6	PERIPHERAL DATA LINE (PD7) - Same as pin 25 except bit A6.
29	PXPA5	PERIPHERAL DATA LINE (PD6) - Same as pin 25 except bit A5.
31	PXPA4	PERIPHERAL DATA LINE (PD5) - Same as pin 25 except bit A4.
33	PXPA3	PERIPHERAL DATA LINE (PD4) - Same as pin 25 except bit A3.
35	PXPA2	PERIPHERAL DATA LINE (PD3) - Same as pin 25 except bit A2.

TABLE 5-2. Peripheral Connectors J1 and J16 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
37	PXPA1	PERIPHERAL DATA LINE (PD2) - Same as pin 25 except bit A1.
39	PXPA0	PERIPHERAL DATA LINE (PD1) - Same as pin 25 except bit A0.
43	PXCA2	DATA STROBE - An output pulse used to clock data from the MPU to the printer logic. The pulse is active low and at least 1.0 us wide.
47	PXCA1	ACKNOWLEDGE - A low-level input pulse indicating the input of a character into memory or the end of a functional operation.

TABLE 5-3. DPP Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8126B01	Printed wiring board
C1,C2,C3,C4, C5,C6,C7,C8	21SW992C025	Capacitor, ceramic, .1 uF @ 50 Vdc
C9	23NW9618A33	Capacitor, electrolytic, 22 uF @ 25 Vdc
DS1	48NW9612A34	Indicator light, red, 5 Vdc
J1	28NW9802D76	Connector, right angle, 50-pin
J2	28NW9802D04	Header, single-row post, 3-pin
J3,J5,J8,J10	28NW9802D01	Header, double-row post, 2-pin
J4,J6,J9,J11,J15	28NW9802E30	Header, single-row post, 4-pin
J7	28NW9802E41	Connector, socket, 50-pin
J12,J13	28NW9802C63	Header, double-row post, 12-pin
J14	28NW9802C43	Header, double-row post, 8-pin
J16	28-W4262B01	Connector, socket, 50-pin (Stacked on J1)

TABLE 5-3. DPP Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
P1	28NW9802E05	Connector, plug, 64-pin
R1,R2,R6	51NW9626A22	Resistor network, 5/10k ohm
R3,R4,R5,R7	51NW9626A37	Resistor network, 9/10k ohm
U1,U9,U11,U12	51NW9615E96	I.C. SN74LS245
U2,U3,U17	51NW9615F02	I.C. 74LS244N
U4	51NW9615H93	I.C. SN74LS641N
U5	51NW9615H92	I.C. N74LS112N
U6	51NW9615F41	I.C. DM74LS164N
U7	51NW9615H41	I.C. SN74LS682N
U8,U10	51NW9615D85	I.C. MC68B21P
U13	51NW9615G38	I.C. SN74LS38N
U14	51NW9615E93	I.C. SN74LS14N
U15	51NW9615G12	I.C. SN74LS375N
U16	51NW9615C56	I.C. SN74S08N
U18	51NW9615E98	I.C. SN74LS373N
	09NW9811A22	Socket, I.C., DIL, 40-pin (use at U8 and U10)
	29NW9805B17	Jumper, shorting, insulated (use at J2-J5, J8-J10, J12, J13, J15)

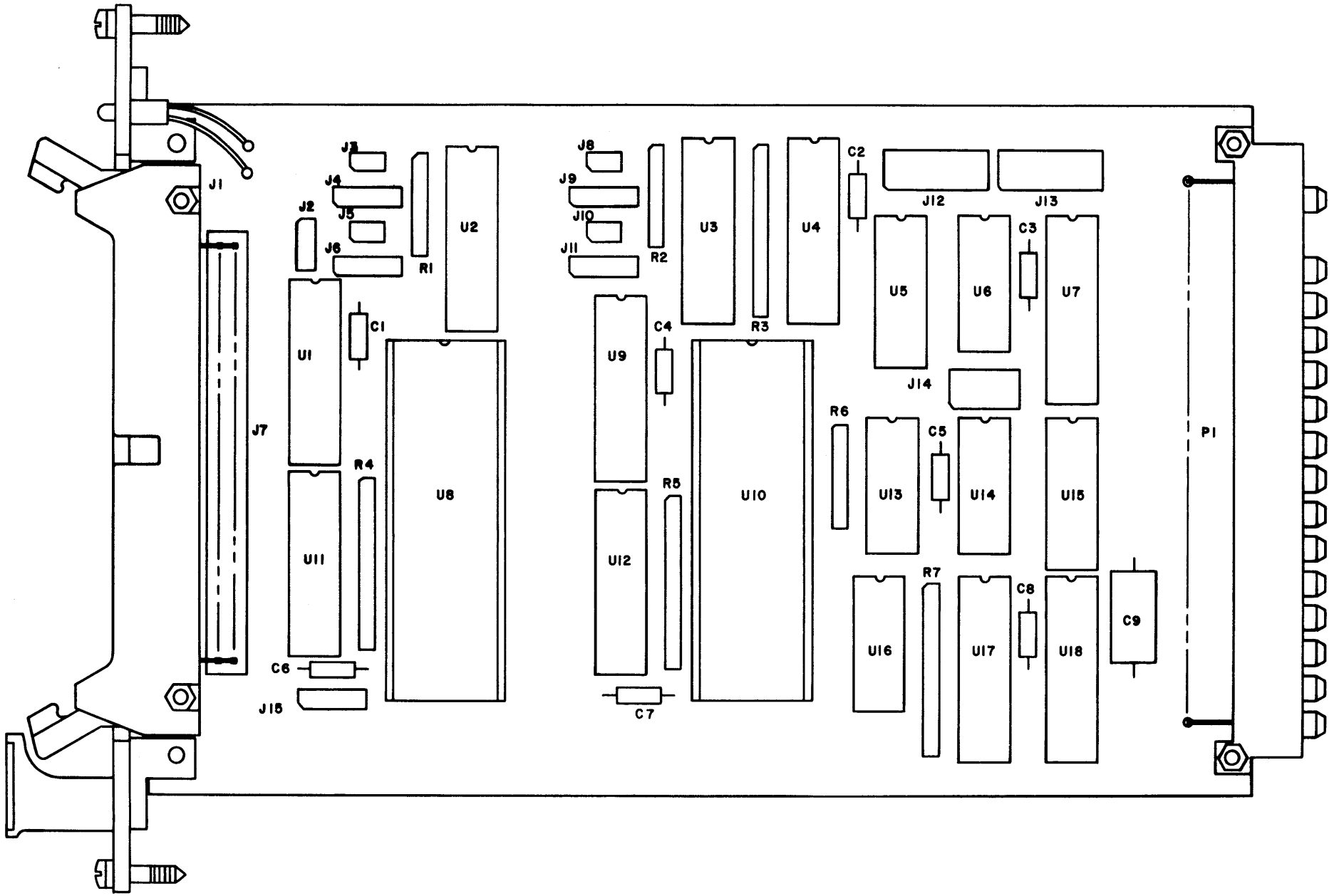
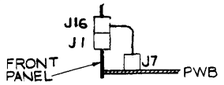


FIGURE 5-1. DPP Module Parts Location Diagram

NOTES:

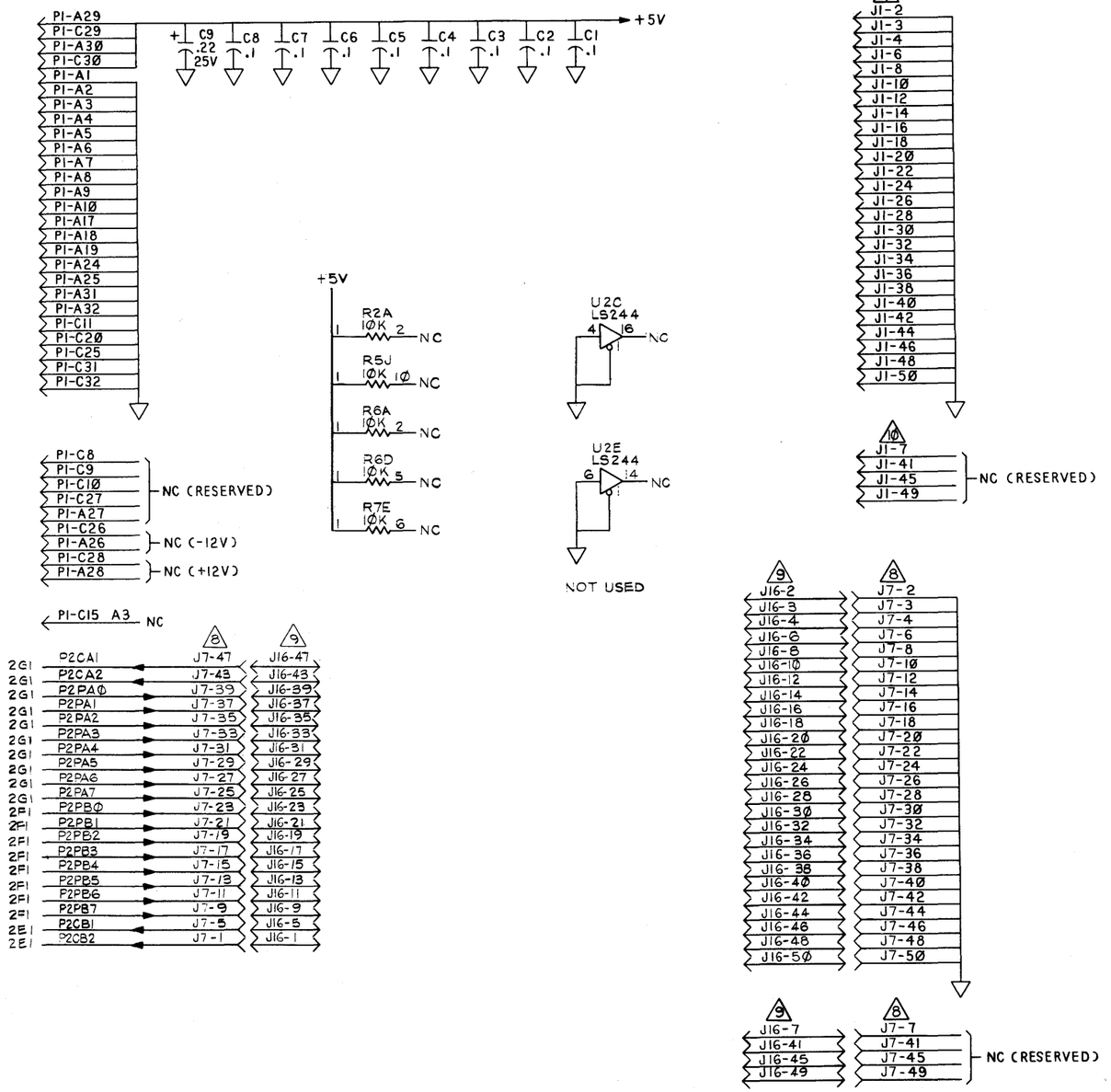
1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ± 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES – ACTIVE LOW SIGNAL.
   [ ] DENOTES – ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING. FOR FULL PART TYPE, REFER TO TABLE I.
8. DENOTES PWB HEADER CONNECTOR.
9. DENOTES FRONT PANEL CONNECTOR.
10. DENOTES PWB–FRONT PANEL CONNECTOR.



7 TABLE I

REF DES	TYPE 4	GND	+5V
U1	74LS245	10	20
U2	74LS244	10	20
U3	74LS244	10	20
U4	74LS641	10	20
U5	74LS112	8	16
U6	74LS164	7	14
U7	74LS268	10	20
U8	MC68B21	1	20
U9	74LS245	10	20
U10	MC68B21	1	20
U11	74LS245	10	20
U12	74LS245	10	20
U13	74LS38	7	14
U14	74LS14	7	14
U15	74LS375	8	16
U16	74S08	7	14
U17	74LS244	10	20
U18	74LS373	10	20

U18	
R7	
J15	
E2	
C9	
DS1	
HIGHEST NUMBER USED	NOT USED
REFERENCE	DESIGNATIONS



63EW3126B REV D SH 1 OF 2

FIGURE 5-2. DPP Module Schematic Diagram (Sheet 1 of 2)

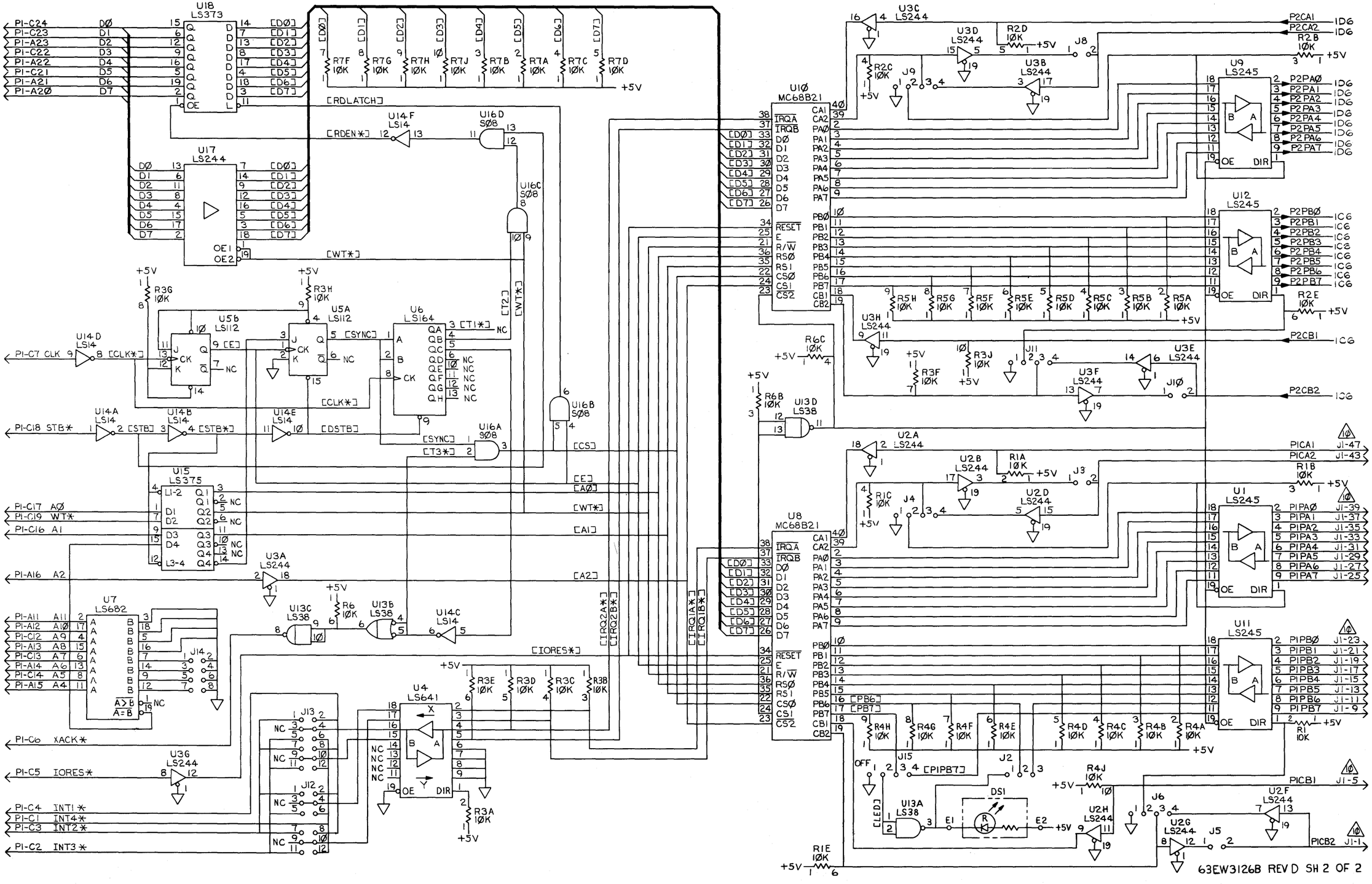


FIGURE 5-2. DPP Module Schematic Diagram (Sheet 2 of 2)

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