MVME327A/D1

MVME327A
VMEbus To SCSI Bus Adapter
And
MVME717
Transition Module
User's Manual

MOTOROLA

MVME327A

VMEbus TO SCSI BUS ADAPTER

AND

MVME717

TRANSITION MODULE

USER'S MANUAL

(MVME327A/D1)

PREFACE

This manual provides general information, hardware preparation, installation instructions, functional description, and support information for the MVME327A VMEbus to SCSI Bus Adapter with Floppy Interface, P2 Adapter Board, and MVME717 Transition Module for the MVME327A.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *related documentation* paragraph in Chapter 1 of this manual.

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERFERENCE.

First Edition July 1988

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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CHAPTER 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation, installation instructions, functional description, and support information for the MVME327A VMEbus to SCSI Bus Adapter with Floppy Interface, P2 Adapter Board, and MVME717 Transition Module for the MVME327A.

1.2 FEATURES

The features of the MVME327A include:

- MC68010 microprocessor running at 10 MHz.
- Two 32-pin EPROM sockets for onboard firmware and application software.
- 128Kb static RAM (four 32K x 8 devices).
- VMEbus master interface for DMA operations.
- VMEbus interrupter realized through the MC68153.
- SCSI interface provided on connector P2 (through P2 Adapter Board).
- Intelligent SCSI protocol controller realized through the WD33C93 SCSI Bus Interface Controller (SBIC).
- Synchronous SCSI data transfer capability realized through the WD33C93 SBIC.
- Programmable burst control on the VMEbus realized through jumpers for time on the VMEbus and for time off the VMEbus.
- SYSFAIL driver and front panel indicator.
- Onboard firmware to realize the Buffered Pipe Protocol (BPP) for interprocessor communications.
- VMEbus slave interface for the BPP.
- Onboard firmware to control SCSI disk and tape controllers.
- Onboard firmware to provide TARGET role support for interprocessor communication over the SCSI bus.
- Local floppy disk interface for bootload and backup (supports 1.2Mb format).
- Timer (MC68230) for local timing functions.

1.3 SPECIFICATION

The MVME327A specifications are identified in Table 1-1.

TABLE 1-1. MVME327A Specifications

CHARACTERISTICS	SPECIFICATION
Microprocessor	MC68010 10 MHz
Memory size capability	
RAM	128Kb
EPROM	Two sockets for up to 256Kb
Indicators	FAIL LED on front panel
Operating temperature	0 degrees C to +55 degrees C at point of entry of forced air (approximately 330 LFM) (refer to paragraph 1.3.1)
Storage temperature	-20 degrees C to +80 degrees C
Operating humidity	5% to 95% (non-condensing)
Power requirements	+5 Vdc +/- 5%, 4.23 A (typ), 4.59 A (max.)
Physical characteristics	Double height VME board with front panel
Board dimensions	
Height	233.35 mm (9.187 in.)
Depth	160 mm (6.299 in.)
Front panel	
Height	262 mm (10.48 in.)
Width	20 mm (0.8 in.)

1.3.1 Cooling Requirements

The Motorola MVME327A is specified, designed, and tested to operate reliably with an incoming air temperature range from 0 degrees C to 55 degrees C (32 degrees to 131 degrees F) with forced air cooling at a velocity typically achievable by using a 71 CFM axial fan. Temperature qualification is performed in a standard Motorola VMEsystem 1000 chassis. Twenty-five watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of three axial fans, rated at 71 CFM per fan, is placed directly under the VME card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 6 CFM and 330 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55 degrees C with increased airflow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

1.3.2 FCC Compliance

The MVME327A and MVME717 were tested in an FCC-compliant chassis, and meets the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

a. Shielded cables on all external I/O ports.

b. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.

c. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.

d. Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented; failure to do so could compromise the FCC compliance of the equipment containing the module.

1.4 GENERAL DESCRIPTION

The MVME327A is an intelligent host adapter between the standard 32-bit VMEbus and the standard 8-bit parallel (SCSI) bus. Its targeted application is to provide an intelligent interface from VMEbus MPU modules to SCSI disk and tape controllers. Another targeted application is to provide a gateway to the VMEbus as a TARGET on the SCSI bus for interprocessor interactions.

The MVME327A is designed to prioritize SCSI bus activity over floppy drive activity. This goal is achieved through hardware and firmware priority schemes. The floppy interface has a very low priority on the module. Floppy disk activity is not to interfere with the operation of the SCSI bus. Floppy data is double buffered and only block transfers are used in order to prevent overrun or underrun. **THE RESULTING SLOW FLOPPY RESPONSE TIMES ARE INHERENT TO THE SYSTEM AND CANNOT BE ALTERED.**

A secondary application of the MVME327A is to provide a SCSI device that has access to the VMEbus. This SCSI TARGET provides message and command handling capabilities as a processor class device. The applications for MVME327A as a processor class target on the SCSI bus have not been assigned, so the onboard firmware only addresses services provided in TARGET role. The actual implementation of TARGET firmware is application and/or user driven.

1.5 RELATED DOCUMENTATION

The following publications may provide additional helpful information. If not shipped with this product, they may be purchased from Motorola Literature Distribution Center, 616 West 24th Street, Tempe, AZ 85282; telephone (602) 994-6561.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
MC68010 16-Bit Virtual Memory Microprocessor User's Manual	M68010UM
MVME327A Firmware User's Manual	MVME327AFW
The VMEbus Specification	HB212
MC68230 Parallel Interface/Timer Data Sheet	MC68230
MC68153 Bus Interrupter Module Data Sheet	MC68153

NOTE: Although not shown in the above list, each Motorola MCD manual publication number is suffixed with characters which represent the revision level of the document, such as "/D2" (the second revision of a manual); supplement bears the same number as the manual but has a suffix such as "/A1" (the first supplement to the manual).

The following publications are available from the sources indicated.

WD33C92 and WD33C93 SCSI Bus Interface Controller Data Manual; Western Digital, 2445 McCabe Way, Irvine, CA 92714.

WD37C65 Floppy Disk Subsystem Controller Data Sheet; Western Digital, 2445 McCabe Way, Irvine, CA 92714.

1.6 MANUAL TERMINOLOGY

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, activation and deactivation are used to specify forcing a signal to a particular state. In particular, activation and activate refer to a signal that is active or true; deactivation and deactivate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides unpacking, hardware preparation, and installation instructions for the MVME327A.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier's agent be present during unpacking/inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment.

2.3 HARDWARE PREPARATION

To select the desired configuration and ensure proper operation of the MVME327A, certain modifications may be made to the module. These modifications are made through jumper arrangements. Header locations are shown in Figure 2-1. The module is shipped with factory-installed jumper configurations which make the module ready for operation in a VMEbus system.

The header functions and possible options are listed in Table 2-1.

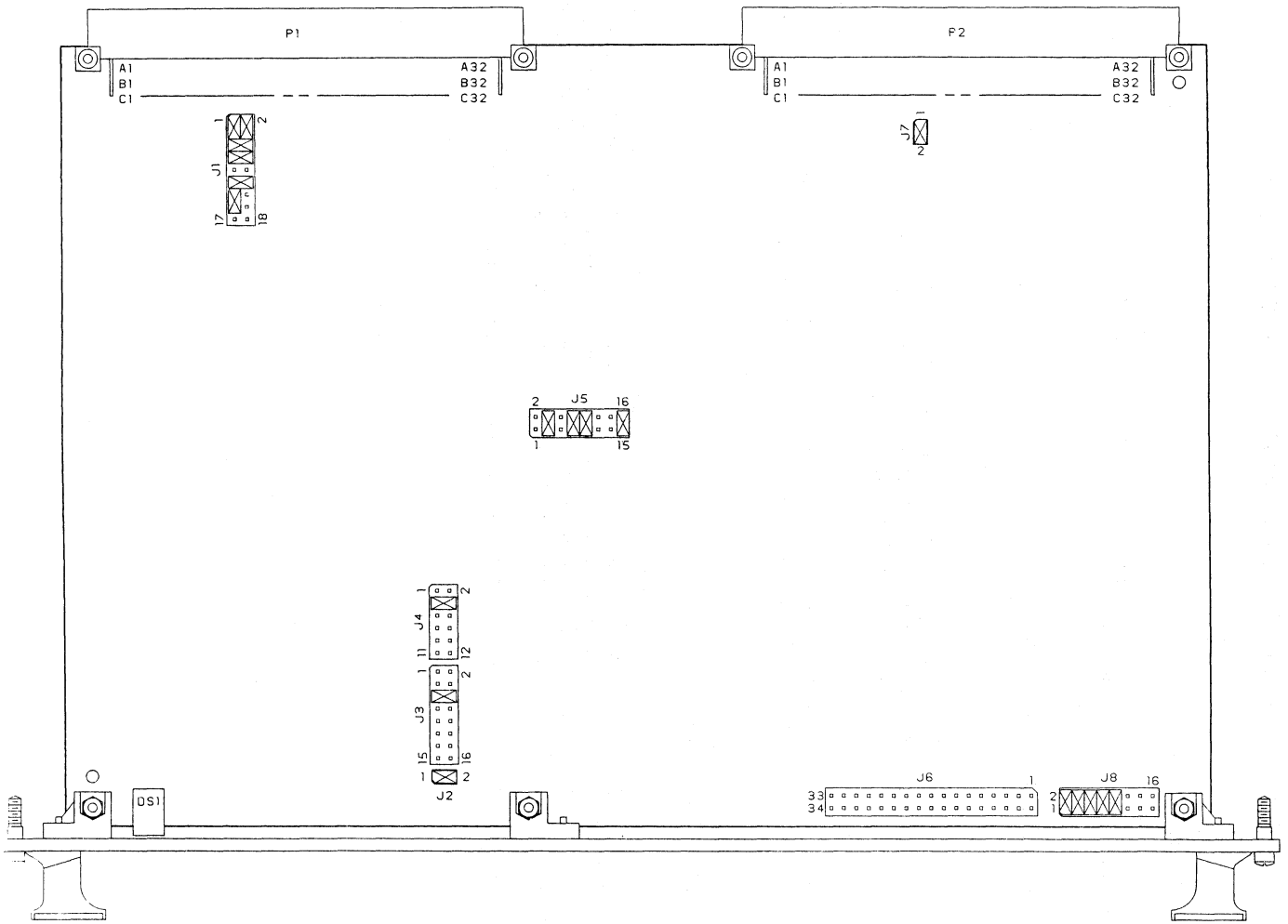


FIGURE 2-1. MVME327A Header Locations

TABLE 2-1. MVME327A Header Functions

HEADER	FUNCTION	OPTIONS
J1	Bus Request Level	Select level 0, 1, 2, or 3
J2	Local Bus Time-out Enable	Enable/disable local bus time-out
J3	Time On bus Select	Select 4, 8, 16, 32, 64, 128, 256, or no time limit
J4	Time Off Bus Select	Select 0, 2, 4, 8, 16, or 32 microseconds
J5	Slave Address Select	Select any 256 byte boundary in the short I/O address space
J7	Terminator Power	Enable/disable Vcc to terminator power on SCSI bus
J8	Firmware Configuration	Select status register MSB as 0 or 1

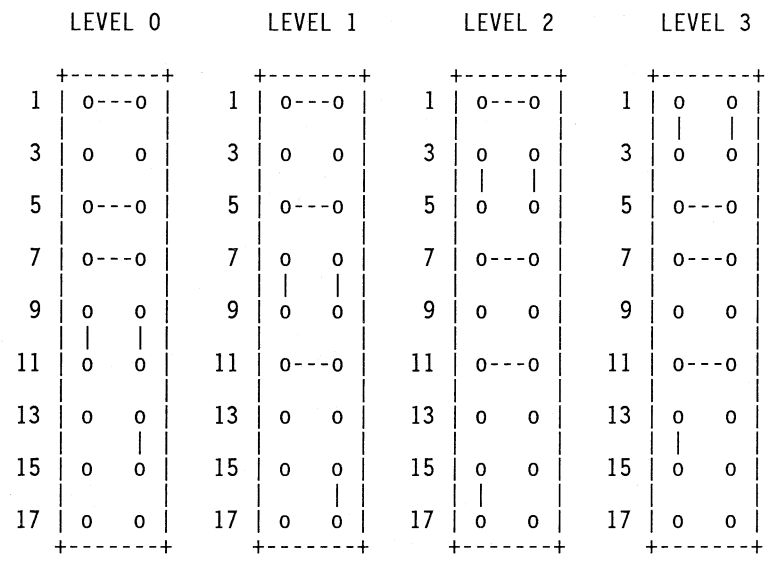
2.3.1 **Bus Request Level Select Header (J1)**

Header J1 determines the VMEbus request priority level. Four levels are available. Refer to the table below. The factory-shipped configuration is level 3.

In VME systems containing a single level bus arbiter, the VMEbus bus request must be configured for level 3. For use with a multi-level arbiter, any one of the four priority levels may be selected.

In multi-level arbitration systems, the bus grant daisy-chain signals which are not used by the MVME327A module are passed down the bus.

Header J1 configuration for each priority level is shown in the figures and table below.



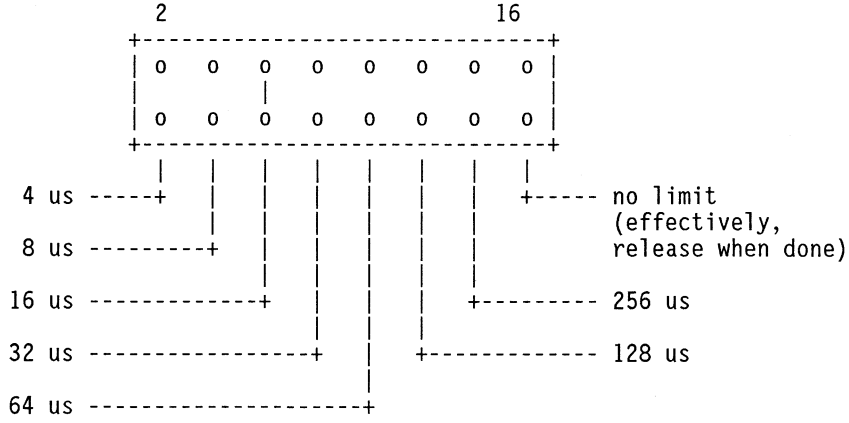
J1 CONNECTIONS	BUS REQUEST PRIORITY LEVEL
1-2, 5-6, 7-8, 9-11, 10-12, 14-16	level 0
1-2, 5-6, 7-9, 8-10, 11-12, 16-18	level 1
1-2, 3-5, 4-6, 7-8, 11-12, 15-17	level 2
1-3, 2-4, 5-6, 7-8, 11-12, 13-15	level 3

2.3.2 Local Bus Time-Out Enable Select Header (J2)

Header J2 allows the local bus time-outs to occur. The MVME327A is factory configured as enabled as shown below.

2.3.3 Time On Bus Select Header (J3)

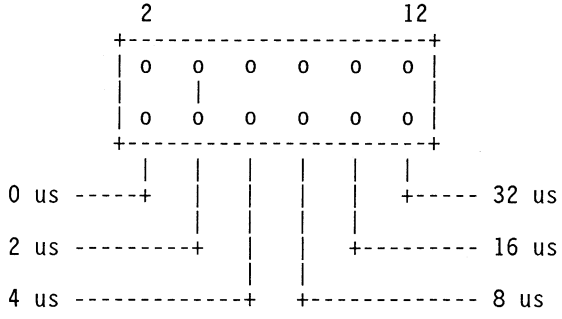
Header J3 is used to select the time limit that the MVME327A should spend on the VMEbus when bursting data to/from the SCSI bus. When the MVME327A acquires the VMEbus, a timer is started; when the timer expires, the VMEbus requester is told to release VMEbus mastership. Eight jumper positions are provided: 4, 8, 16, 32, 64, 128, and 256 microseconds and the last position which does not use a time limit. The DMA controller transfers data until the FIFOs are full or empty. The MVME327A is factory configured for 16 microseconds.



J3 CONNECTIONS	TIME ON BUS
1-2	4 microseconds
3-4	8 microseconds
5-6	16 microseconds
7-8	32 microseconds
9-10	64 microseconds
11-12	128 microseconds
13-14	256 microseconds
15-16	No limit (release when done)

2.3.4 Time Off Bus Select Header (J4)

Header J4 is used to select the time limit that the MVME327A should observe before reissuing a VMEbus request to acquire the VMEbus. After the VMEbus mastership is released, a timer is started; when the timer expires, the VMEbus requester is allowed to reissue a bus request for the VMEbus. Six jumper positions are provided: 0, 2, 4, 8, 16, and 32 microseconds. The MVME327A is factory configured for 2 microseconds.



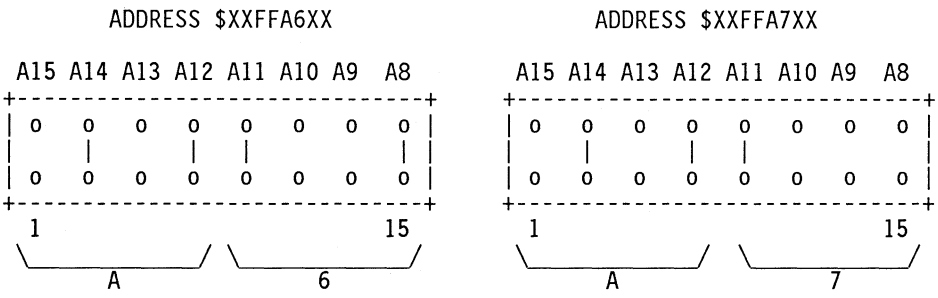
J4 CONNECTIONS	TIME OFF BUS
1-2	0 microseconds
3-4	2 microseconds
5-6	4 microseconds
7-8	8 microseconds
9-10	16 microseconds
11-12	32 microseconds

2.3.5 Slave Address Select Header (J5)

The MVME327A responds to address modifier codes $29 and $2D on the VMEbus. When a VMEbus master drives these address modifier codes on the VMEbus, only a 16-bit address is decoded for short I/O space. Eight jumper positions are provided on header J3 for selection of a 256 byte page in short I/O space. The factory-shipped configuration for the MVME327A is for the page corresponding to address $XXFFA6XX.

A 256 byte page out of the short VMEbus I/O space is provided for the IPC interface registers. Two pages have been assigned for two MVME327A modules used in Motorola systems.

The figures and table below shows the configuration for the two addresses.



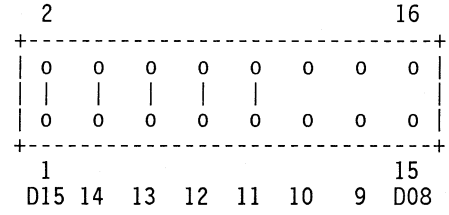
J5 CONNECTIONS	SHORT I/O SPACE ADDRESS
3-4, 7-8, 9-10, 15-16	first MVME327A at address $XXFFA6XX
3-4, 7-8, 9-10	second MVME327A at address $XXFFA7XX

2.3.6 Enable/Disable Terminator Power Select Header (J7)

Because the MVME327A is a dual initiator/target, it must be capable of providing terminator power to the SCSI bus. Header J7 is used to enable/disable this terminator power generation for the SCSI bus. Bus terminators are installed in sockets so that the user may configure the MVME327A for the terminators if it is at the end of the bus and for no terminators if it is in the middle of the bus. The module is factory configured with terminator power enabled (jumper installed).

2.3.7 Firmware Configuration Select Header (J8)

Header J8 is used for firmware configuration. The status of header J8 is readable by the local processor in the most significant byte of the status register. When a jumper is installed, the corresponding bit is read as a 0. A 1 is read if the jumper is not installed. The as-shipped factory configuration is as shown below. Refer to the MVME327AFW Firmware Manual for more detailed information.



2.4 INSTALLATION INSTRUCTIONS

When the MVME327A has been configured as desired by the user, it can be installed in the system as follows:

a. Turn all equipment power OFF and disconnect power cable from ac power source.

CAUTION

CONNECTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS EQUIPMENT. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

b. Remove the filler panel from the appropriate card slot.

c. Insert the MVME327A in any slot other than the first slot which is reserved for a system controller.

d. Secure the module with two screws on the front panel.

e. At the step b slot on the backplane, remove the jumpers for IACKIN*/IACKOUT* and BGIN*/BGOUT*.

f. Install P2 adapter board according to installation instructions in Chapter 5.

g. Install MVME717 module (if used) according to installation instructions in Chapter 6.

h. Turn equipment power ON.

CHAPTER 3 - FUNCTIONAL DESCRIPTION

3.1 INTRODUCTION

This chapter provides the user of the MVME327A with a block level functional description of the hardware and firmware.

3.2 FUNCTIONAL DESCRIPTION

The MVME327A is an intelligent host adapter between the standard 32-bit VMEbus and the standard 8-bit parallel (SCSI) bus. Its targeted application is to provide an intelligent interface from VMEbus MPU modules to SCSI disk and tape controllers. Another targeted application is to provide a gateway to the VMEbus as a TARGET on the SCSI bus for interprocessor interactions.

A typical computer system usually contains some type of mass storage interface for file and data storage. The SCSI bus is a general purpose, 8-bit parallel bus. SCSI mass storage devices are available today from a multitude of manufacturers. The SCSI bus is a de facto standard controller bus. The MVME327A is an intelligent interface adapter from the VMEbus to the SCSI bus. VME MPU modules that do not contain a local mass storage interface may use the MVME327A to access resources on the SCSI bus to fulfill a system's mass storage requirements. Another function provided on the MVME327A is a local floppy interface of up to two drives. Having the floppy interface locally relieves the system integrator from having to incorporate a SCSI floppy drive or a VMEbus floppy controller. Below is a list of Motorola Microcomputer Division MPU modules that may use the MVME327A to provide a link to the SCSI bus.

MVME101	MVME133
MVME104	MVME133A
MVME105	MVME133XT
MVME106	MVME134
MVME110	MVME135
MVME12X	MVME136
MVME130	MVME140
MVME131	MVME141
MVME132	

The MVME107, MVME117/MVME117A, and also the MVME147 contain a local interface to the SCSI bus, so an added interface to the same bus is redundant.

The MVME327A is designed to keep the SCSI bus going no matter what activity is taking place on the floppy drives. This goal is achieved through hardware and firmware priority schemes. The floppy interface has a very low priority on the module. Floppy disk activity is not to interfere with the operation of the primary SCSI bus. **THE RESULTING SLOW FLOPPY RESPONSE TIMES ARE INHERENT TO THE SYSTEM AND CANNOT BE ALTERED.**

A secondary application of the MVME327A is to provide a SCSI device that has access to the VMEbus. This SCSI TARGET provides message and command handling capabilities as a processor class device. The applications for MVME327A as a processor class target on the SCSI bus are user-defined, so the onboard firmware only provides services in TARGET role. The actual implementation of TARGET firmware is application and/or user driven.

The basic function for the onboard MVME327A firmware is to accept requests through the Buffered Pipe Protocol (BPP) from various users (drivers) on the VMEbus and to carry out these high level requests through a series of SCSI commands to SCSI devices. Other functions of the firmware are to execute floppy disk commands, create and delete the BPP channels upon request, and test the hardware on power up and upon request.

In order to provide a compatible firmware interface, the MVME327A Intelligent Peripheral Controller (IPC) interface consists of a set of basic commands sent through the Command/Status Register (CSR) interface and a set of commands sent in packets via virtual channels. The CSR commands establish and maintain the virtual channels for host/IPC communications. After one or more virtual channels are created, all other commands are transmitted between the host CPU and the IPC on these channels. Multiple VMEbus masters may use the MVME327A at the same time through their virtual channels.

Aside from the software abort interrupt used in DEBUG and ACFAIL, the highest level (and therefore the highest priority) interrupt comes from the MVME327A timer (level 6). Next in line of priority is the MVME327A Data Channel Controller (DCC) (level 5) followed by the SCSI interface (level 4). The VMEbus interface and a local software interrupt both share the next level (level 3) but each has a different vector so they call different service routines. The floppy interface (level 2) is the next in priority followed by another software interrupt (level 1).

Given the above priority scheme for the interrupt structure on the MVME327A, the interactions in the MVME327A firmware are described in a possible scenario below.

After the MVME327A powers up, performs the power up diagnostics, and releases access to the TAS register, the onboard firmware enables interrupts and waits for events from the VMEbus and/or the SCSI bus. Following the user request for a channel initialization, the operating system driver gains access to the IPC CSR space and begins channel initialization by writing to the CSR. The driver interrupts the MME327A by writing to its interrupt register. Shortly after the interrupt register is accessed by a driver, an interrupt (level 3) is generated on the MVME327A.

The local processor examines the source of the interrupt and decodes it as a channel initialization interrupt. After the initialization procedure is completed by the MVME327A, the local processor again waits for an interrupt. The same driver now places an entry (envelope) in the initialized command pipe and again interrupts the MVME327A. The local processor decodes the interrupt command entry, copies the envelope information over the VMEbus to a local envelope, and dequeues the envelope from the pipe. The local firmware then

processes the local envelope, determines that it is a command for a floppy drive, places the local envelope in the floppy input queue, and generates a local software interrupt (level 1). After placing the entry in the floppy input queue, the firmware returns to the interrupted routine.

Before level 1 interrupt handler can dequeue the entry from the floppy input queue, however, another driver requests a channel initialization and interrupts (level 3) the processor by writing to the ATN bit. After another channel is initialized by the MVME327A, the firmware returns control to the preempted routine. At this time the firmware finds the floppy input queue entry and calls the floppy command processing routine.

Now an envelope is placed in the newly created channel pipe and another CSR interrupt (level 3) is generated by the user. This interrupt occurs before the floppy command can be processed fully. The local firmware processes the envelope, determines that it is a command for the SCSI bus, places an entry in the SCSI input queue, and generates a local interrupt (also level 3) so that SCSI processing can continue without being interfered with any floppy or adapter commands (which operate at level 2 or below). The firmware then exits from this Interrupt Service Routine (ISR) to allow entry to the SCSI level 3 ISR.

The SCSI level 3 ISR finds an entry in the SCSI input queue and initiates a SCSI module request. This request is accomplished by removing the entry from the input queue and calling the SCSI module (through a subroutine call) with the queue entry as a passed parameter.

Assuming that an initiator role request was sent by the driver, the SCSI module begins the SCSI protocol to perform the requested initiator command. When the SCSI module is active, the local MVME327A processor executes at either interrupt level 3 (entry from the local interrupt), level 5 (DCC interrupt), or level 4 (SCSI interface chip). When the SCSI transactions have completed, the SCSI module is most likely at interrupt level 4 because a disconnect interrupt is the most likely event that terminates the SCSI thread. After the thread is terminated, the SCSI module returns status to the user through the BPP and returns from the interrupt.

At this time, the floppy command processing routine resumes. The command runs to completion, and control is returned to the calling routine. The firmware then returns status to the user through the BPP and the floppy operation is finished.

At any time during the floppy command processing, a higher priority task could take precedence. For example, another floppy command envelope could be dequeued from the BPP pipe or another entire SCSI command could be executed between the time the floppy command was started and the time it was finished.

Multi-host interfaces are allowed through the MVME327A. Reservation of resources is a subject that has been considered by the SCSI standard. The reservation of SCSI resources on a host-to-host basis on the VMEbus is handled by the MVME327A. In other words, if VMEbus host A sends a write descriptor

command to the MVME327A with the intent of formatting a particular disk drive on the SCSI bus, and if VMEbus host B sends a different write descriptor command to the MVME327A, there is a danger that when host A issues the format command, the drive is formatted with host B parameters. The MVME327A firmware handles this type of problem with the implementation of the RESERVE command (refer to MVME327FW user's manual).

3.3 BLOCK DIAGRAM DESCRIPTION

For the purpose of the following description, the MVME327A is regarded as consisting of function blocks as shown in Figure 3-1.

For details of the MVME327A hardware, schematic diagrams and an assembly drawing are included in Chapter 4.

3.3.1 Local Processor

An MC68010 microprocessor provides the required functionality with a few needed enhancements. An address extension register provides the upper address bits necessary for the A:32 VMEbus interface. An address modifier register provides for the correct code to be sent during VMEbus accesses.

3.3.2 Map Decoder

The local memory map of the MVME327A is split into two parts: one for local resources and one for VME accesses. The local memory map is shown in Table 3-1.

TABLE 3-1. Memory Map

ADDRESS	DEVICE(S)	COMMENT
000000-01FFFF	LOCAL RAM	128Kb
	000000-00FFFF	Low RAM (first socket pair)
	010000-01FFFF	High RAM (second socket pair)
	01FF00-01FFFF	IPC registers are the last page of high RAM
020000-0FFFFF	LOCAL RESOURCES	Described below:
020000-02FFFF	IDT7201A	8-bit access to DCC FIFO's (ODD ONLY)
030000-03FFFF	MSR	Module status register
040000-04FFFF	WD33C93	SCSI bus (ODD ONLY)

TABLE 3-1. Memory Map

ADDRESS	DEVICE(S)	COMMENT
		.
070000-07FFFF	Floppy Interface	
	070001-070003	WD37C65
	070005	WD37C65 operations register
	070007	WD37C65 control register
		.
080000-08FFFF	IDT7202	Floppy FIFO (ODD ONLY)
		.
090000-09FFFF	Address Modifier Registers	
	090000	DCC AM register (byte) (WRITE ONLY)
	090001	Processor AM register (byte) (WRITE ONLY)
	090002	Address extension register (word) (WRITE ONLY)
		.
0A0000-0AFFFF	Data Channel Controller	
	0A0000	Word counter (word) (R/W)
	0A0002	Upper address counter (word) (WRITE ONLY)
	0A0004	Lower address counter (word) (WRITE ONLY)
		.
0B0000-0BFFFF	MC68230	Programmable interface/timer (ODD ONLY)
0C0000-0CFFFF	MC68153	Bus Interrupter Module (BIM) (ODD ONLY)
		.
0D0000-0DFFFF		For factory use only
100000-13FFFF	LOCAL EPROM	256Kb max. with 128K x 8 devices
120000-7FFFFF	RESERVED	Unused
800000-FFFFFF	VMEbus	All accesses to the VMEbus have A23=1 The address extension register replaces A23

Below are the various local control and status bits for the MVME327A.

ADDRESS	DEVICE(S)	BIT	ASSIGNMENT (level)
1FF06	SHADOW REGISTER	D15	BUSY (R/W) (1)
		D14	CSRRST (R) (0)
		D13	ATNIRQ (R/W) (0)
		D12	INHSFAIL (R/W) (0)
		D11	SW6EN (W) (0) BRDFAIL (R) (1)
		D10	SW6 (R/W) (0) (NOTE)
		D09	Spare (R/W) (0)
		D08	Spare (R/W) (0)
30001	Module Status Register	D15-D08	Firmware config header
		D07	Floppy interrupt request* (0)
		D06	DMABERR* (0)
		D05	Floppy FIFO full* (0)
		D04	Floppy FIFO empty* (0)
		D03	DMA interrupt (0)
		D02	SCSI interrupt flag (1)
		D01	SCSI data request (1)
		D00	SCSI RAM chip select* (0)
40001	WD33C93 ADDRESS REGISTER	D07-D00	Write only
40001	WD33C93 AUX STATUS REGISTER	D07-D00	Read only
40003	WD33C93 Internal Registers	D07-D00	Read/write
70001	WD37C65 Main Status Register	D07-D00	
70003	WD37C65 Data Register	D07-D00	
70005	WD37C65 Operations Register	D07-D00	
70007	WD37C65 Control Register	D07-D00	
90000	DCC AM Register	D15	Don't care
		D14	Don't care
		D13-D08	AM5-AM0
90001	uP AM Register	D07	Don't care
		D06	Don't care
		D05-D00	AM5-AM0
90002	Address Extension Register	D15-D07	VME A31-VME A23
		D06-D00	Don't care
A0000	DCC Word Counter	D15-D00	2's complement word count

ADDRESS	DEVICE(S)	BIT	ASSIGNMENT (level)
A0002	DCC Address Counter (MSW)	D15	Don't care
		D14-D00	VME A31-VME A17
A0004	DCC Address Counter (LSW)	D15-D00	VME A16-VME A01
B000D	PI/T Port A Control Register Output H2	D03	DCC word and address counter load* (0)
B000F	PI/T Port B Control Register Output H4	D03	Precompensation value (1)
B0011	PI/T Port A Data Register	D07	DMA enable* (0)
		D06	SCSI FIFO reset* (0)
		D05	Floppy chip reset (1)
		D04	Floppy DMA enable* (0)
		D03	Floppy DMA interrupt enable* (0)
		D02	From floppy (DMA direction)(1)
		D01	CSR reset enable* (0)
		D00	Floppy RPM* (0)
B0013	PI/T Port B Data Register	D07	Master interrupt enable* (0)
		D06	Software interrupt LVL 3* (0)
		D05	Software interrupt LVL 1* (0)
		D04	Drive SFAIL (1)
		D03	Activate SCSI bus RESET* (0)
		D02	SCSI RESET interrupt enable* (0)
		D01	External SCSI interrupt enable (1)
		D00	DMA FLUSH* (0)
B0019	PI/T Port C Data Register	D07	Word counter enable (1)
		D06	Byte swap (1)
		D05	Floppy FIFO reset* (0)
		D04	DMA FIFO state reset* (0)
		D03	Timer interrupt request* (0)
		D02	MOTORON* (0)
		D01	From SCSI* (DMA direction) (0)
		D00	Data size 32-bit* (0)

ADDRESS	DEVICE(S)	BIT	ASSIGNMENT (level)
B001B	PI/T Port Status Register		
	Input H1	D04/D00	Local time-out flag* (0/1) (refer to MC68230 manual)
	Input H3	D06	Floppy ready (1)

NOTE: SW6 can only be set if SW6EN is already set. When set, SW6 generates a software interrupt on level 6 with vector ID of $49.

3.3.3 Multiprocessing VMEbus Interface Logic

The IPC control register (offset $06 in the CSR space) provides the following multiprocessing features:

Bit 15 - BUSY bit. If set, the MVME327A is not capable of accepting any type of request. The module is not in the initialized state and is not capable of any activity. After a reset, this bit is set by hardware. When the MVME327A is completely initialized and ready for commands, the onboard firmware clears this bit. **If this bit is set, the other status and control bits are NOT VALID.**

Bit 14 - RESET bit. If set by a VMEbus master other than the MVME327A, the MVME327A is held in RESET until this bit is cleared by a VMEbus master. After a system reset, this bit is cleared by hardware.

Bit 13 - ATN bit. If set, a local level 3 interrupt is generated on the MVME327A. The local MVME327A processor clears this bit. A VMEbus master sets this bit to generate a local interrupt in order to alert the MVME327A about a pending event. After a reset, this bit is cleared by hardware.

Bit 12 - INHIBIT SYSFAIL. If this bit is set, the MVME327A is not capable of activating the SYSFAIL* signal on the VMEbus. After a reset, this bit is cleared by hardware.

Bit 11 - SW6EN. (Write only) When this bit is set, the SW6 interrupt is enabled. This bit can only be set by the local processor.

BRDFAIL. (Read only) This bit is set when the FAIL LED is on.

Bit 10 - SW6. (R/W) When this bit is set by the local processor or a VMEbus master and the enable bit is set (SW6EN = 1), a level 6 interrupt is sent to the local processor. This bit is cleared by reset.

Bits 9,8 - These bits are readable and writeable from the VMEbus or the local processor. These bits are cleared by reset.

3.3.4 Address Modifier Register(s)

Two write only address modifier registers are provided: one for the data channel controller and one for the local processor.

When a command packet is sent to the MVME327A, an Address Modifier (AM) code is sent to tell the MVME327A how to transfer data over the VMEbus. This is the code that the MVME327A should drive on the bus during the data transfers for that particular packet. An AM register is used to load the particular code to be used during the DMA transfers. When the local processor accesses BPP envelopes and packets, the AM codes that were passed to the MVME327A during channel initialization are to be driven on the VMEbus. A second AM register for processor accesses is needed so that the DCC and the MC68010 may access the VMEbus with different (if appropriate) AM codes.

3.3.5 IPC Registers

The IPC registers are located in the local RAM array. Below is the implementation scheme.

The last 256-byte page of the local RAM array is shared on the VMEbus for communication between a VMEbus MPU module and the MVME327A. An 8-bit shadow register is provided in the space mapped by the 256-byte page to control various functions defined in paragraph 3.3.3. This shadow register (offset $6) appears in the 256-byte page 16 times. Only 8 words of the 128 words reserved for this shared space are assigned for the current BPP implementation. The remaining 90 plus words of shared memory are reserved for future needs and for diagnostics.

3.3.6 Address Extension Register

A 9-bit write only register is used to expand the addressing capability of the MC68010 to 32 bits. The contents of this register are activated on the VME address bus whenever the MC68010 accesses the VMEbus. Bit A23 of the MC68010 address bus is used to signal the onboard map decoder that a VMEbus access is taking place. The local firmware must offset every VMEbus address by $00800000 to ensure that the local decoder decodes the address as a VMEbus access.

3.3.7 Local EPROM and RAM

Local EPROM and RAM for the local processor, sufficient to support BPP and the self test requirements, with expansion capabilities is provided as follows:

Two 32-pin EPROM sockets accept 64K x 8 or 128K x 8 devices. The maximum capacity for EPROM is 512Kb. The 16-bit interface to the EPROM does not incur any wait cycles.

The onboard RAM consists of four 28-pin 32K x 8 static RAMs. The local RAM capacity is therefore 128Kb. Only the 256-byte page allocated for the IPC CSR registers is accessible from the VMEbus. The local RAM interface does not incur any wait cycles.

3.3.8 SYSFAIL Logic

A globally accessible register allows a master on the VMEbus to disable the activation of the SYSFAIL* signal. This globally accessible register is also accessible locally. The MVME327A drives SYSFAIL* when the SYSFAIL signal is enabled and the board FAIL LED is on.

3.3.9 VMEbus Interrupter

The MC68153 Bus Interrupter Module (BIM) provides four independent interrupt channels to the VMEbus from the MVME327A. The allocation of channels is controlled by the local firmware. Each channel is capable of generating an interrupt on any of seven levels. Each channel is also capable of providing a software programmable vector when the VMEbus IACK cycle is detected.

3.3.10 Floppy Interface

A 1Kb FIFO along with the floppy interface chip buffers data to and from the floppy interface. This buffer alleviates the processor bandwidth requirements for floppy service. The LSI floppy controller is the WD37C65. This controller combines the data separator along with the control circuitry to provide an integrated floppy subsystem. Drive select signals are generated through the WD37C65 for two floppy drives. The RPM* signal is generated through the MC68230. A low (0) on the RPM* line means high density. A high (1) means normal density. **PC/AT compatible disk formats are supported on the MVME327A. These 1.2Mb floppies require a dual-speed floppy drive for proper operation.**

3.3.11 VMEbus Master Interface (A:24,A:32/D:16,D:32)

The VMEbus requester on the MVME327A requests the VMEbus for two devices: the MC68010 (8-bit and 16-bit transfers) and the DCC (16-bit and 32-bit transfers). The local MC68010 processor bursts data from the VMEbus to its internal registers and from its internal registers to the VMEbus. Whenever the MC68010 performs a non-VMEbus access, the VMEbus requester is told to release the VMEbus to another master. The DCC finishes VMEbus activity whenever it has no data to transfer (FIFO's empty or full, or transfer complete) or whenever a VMEbus bus error is received during one of its cycles. Whenever the DCC has no activity to perform on the VMEbus, it tells the VMEbus requester to release the VMEbus to another master.

So that the MVME327A does not become a VMEbus hog, a Time on bus/Time off bus scheme is used to control the amount of time that the MVME327A spends on the VMEbus. Time on the VMEbus is controlled so that the MVME327A bursts for a specified time limit. In other words, when the MVME327A acquires the VMEbus, a timer is started; when the timer expires, the VMEbus requester releases VMEbus mastership. Time off the bus is controlled so that the MVME327A does not issue another VMEbus request until a specified time limit. This is done to allow other VMEbus masters to acquire the bus. In other words, after the VMEbus mastership is released, a timer is started; when the timer expires, the VMEbus requester is allowed to issue a bus request for the VMEbus.

Time on bus is selectable on header J3. The selectable times are: 4, 8, 16, 32, 64, 128, 256 microseconds or no time limit (release when done).

Time off bus is selectable on header J4. The selectable times are: 0, 2, 4, 8, 16 microseconds.

3.3.12 Local Bus Arbiter

The MC68010 and a VMEbus master may gain control of the MVME327A local bus. The MC68010 uses the local bus to access local memory, local I/O, and the VMEbus. A VMEbus master uses the local bus to gain access to the last 256-byte page of local RAM (shared with the VMEbus).

3.3.13 Data Channel Controller

The MVME327A DCC provides buffering and byte packing and unpacking for data that is transferred through the WD33C93 to/from the SCSI bus during the DATA IN and DATA OUT phases. Two FIFO's provide buffering for data coming from the SCSI bus and two FIFO's provide buffering for data going to the SCSI bus. These memory devices allow simultaneous read and write operations and provide a true dual ported buffer that allows the SCSI transfers to proceed uninterrupted by VMEbus transfers.

The MVME327A DCC has the capability of performing either 16-bit or 32-bit data transfers over the VMEbus. Several requirements are imposed by the implementation of the DCC for 32-bit transfers. First, the VMEbus buffer address must be longword aligned. And second, the transfer count must be an even number of long words. If the above requirements are met and if the user indicates that memory is 32-bits wide, then the data bus width may be chosen as 32 bits. Bit D00 of the PI/T port C data register selects the data bus size (0 = 32/1 = 16). **The MVME327A DCC does not perform 8-bit transfers on the VMEbus.**

The WD33C93 (set up in the buffer access-DBA mode) reads/writes bytes from/to the FIFO's by directly providing the required read/write strobes. A toggle flip-flop changes state after each read/write strobe to the FIFO's and controls the multiplexing operation in and out of the FIFO's. The initial state of this flip-flop is initialized for byte-swap or no byte-swap. Byte-swap (as far as the MVME327A is concerned) refers to the packing scheme that places a lower addressed byte in the lower half (D07-D00) of a 16-bit bus. No byte-swap refers to the packing scheme that places a lower addressed byte in the upper half (D15-D08) of a 16-bit bus. Because Motorola processors have the lower addressed byte of a word in the upper half of a 16-bit bus, the no byte-swap option is consistent with the Motorola processor scheme.

3.3.14 **SCSI Interface**

The SCSI interface transfers data asynchronously in bursts up to 1.5Mb per second. In synchronous mode, the interface transfers data in bursts up to 4Mb per second.

The WD33C93 SCSI protocol controller from Western Digital interfaces to the SCSI bus. The 48 mA drivers necessary to conform with the SCSI requirements are part of the WD33C93. Only the single ended implementation of the SCSI standard is supported with this chip. The 4Mb per second synchronous transfer rate required is achievable only with the Direct Buffer (DB) access mode of the WD33C93. The FIFO memory is interfaced directly to the WD33C93 to accommodate the DB mode of operation. Assuming that a VMEbus bandwidth of 1 MHz for 32-bit transfers and a VMEbus bandwidth of 2 MHz for 16-bit transfers is available, the MVME327A is able to sustain the 4Mb per second continuous data rate on the SCSI bus. (The MVME327A packs bytes into longwords or words, so the bandwidth requirement on the VMEbus is cut in half or fourth, depending on the system configuration: 16-bit or 32-bit data transfers.)

3.3.15 **SCSI Bus**

The MVME327A provides only the single-ended SCSI option. Connector P2, through the P2 Adapter Board, is used to route the SCSI signals. Because the MVME327A is a dual initiator/target, it must provide terminator power to the SCSI bus as specified in the SCSI draft. Header J4 is provided to allow/disallow terminator power for the SCSI bus. Bus terminators are installed in sockets so that the user may configure the MVME327A for the terminators if it is at the end of the bus and for no terminators if it is in the middle of the bus. The P2 Adapter Board and a transition module (MVME717) is offered along with the MVME327A to provide standard connections for customers with cabling requirements to an outside box or to an internal (inside an enclosure) SCSI device.

3.3.16 Interrupt Handler

A PAL-based interrupt handler provides the necessary priority encoding and decoding for the locally and bus generated interrupts.

Below is a list of the interrupt sources and their priorities on the MVME327A.

NOTE

The MVME327A is not a VMEbus interrupt handler.

Interrupt Source

INTERRUPT SOURCE	LEVEL	VECTOR
ACFAIL	7	$40
Software Abort	7	$41
Timer	6	$42
IPC Control Register (SW6)	6	$49
Data Channel Controller	5	$43
SCSI Interface (primary)	4	$44
Software Interrupt	3	$45
IPC Control Register (ATN)	3	$46
Floppy Interface	2	$48
Software Interrupt	1	$47

3.3.17 High-performance DMA Interface

A discrete DCC transfers data at a maximum rate of 16Mb per second. This data rate is based on a synchronous design that may execute a VMEbus cycle with a minimum of four clock cycles. The 16Mb per second rate is achievable only with 32-bit transfers. Word transfers still require 4 clock cycles (minimum) to execute, providing 8Mb per second. The 4 clock cycles assumes a maximum delay of 50 ns between the activation of the data and address strobes and the activation of DTACK* and also assumes a maximum delay of 50 ns between the deactivation of strobes and deactivation of DTACK*. The implementation of the DCC is **not** a true DMA controller because it is not able to perform memory to memory transfers but is only able to perform SCSI to VMEbus and VMEbus to SCSI transfers.

CHAPTER 4 - SUPPORT INFORMATION

4.1 INTRODUCTION

This chapter provides the interconnection signals, parts list with parts location illustration, and schematic diagram for the MVME327A module.

4.2 INTERCONNECT SIGNALS

The MVME327A module interconnects with the VMEbus through connector P1, with the VMEbus and serial ports through connector P2.

4.2.1 Connector P1 Interconnect Signals

Connector P1 is a standard DIN 41612 triple-row, 96-pin male connector. The MVME327A interconnects with the VMEbus through rows A, B, and C of P1 and through row B of P2. Each pin connection, signal mnemonic, and signal characteristic for the connector are listed in Table 4-1.

TABLE 4-1. Connector P1 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A8	D00-D07	Data bus (bits 0-7) - eight of 32 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
A9	GND	GROUND - connected to the MVME327A ground plane.
A10	SYSCLK	Not used.
A11	GND	GROUND - connected to the MVME327A ground plane.
A12	DS1*	DATA STROBE 1 - signal that indicates which part of the data bus is transferring data. It is driven by the MVME327A when it is the VMEbus master. It is received by the MVME327A when it is a VMEbus slave.
A13	DS0*	DATA STROBE 0 - signal that indicates which part of the data bus is transferring data. It is driven by the MVME327A when it is the VMEbus master. It is received by the MVME327A when it is a VMEbus slave and a VMEbus interrupter.

TABLE 4-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A14	WRITE*	WRITE - signal that specifies the direction of data transfers. It is driven by the MVME327A as a VMEbus master and received by the MVME327A as a slave.
A15	GND	GROUND - connected to the MVME327A ground plane.
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - signal that indicates that valid data is available on the data bus during a read cycle or that it has been accepted during a write cycle. It is received by the MVME327A as a VMEbus master and driven by the MVME327A as a VMEbus slave and as a VMEbus interrupter.
A17	GND	GROUND - connected to the MVME327A ground plane.
A18	AS*	ADDRESS STROBE - the falling edge of this signal indicates that a valid address, address modifier, LWORD*, and IACK* are available on the VMEbus. It is driven by the MVME327A as a VMEbus master and received by it as a VMEbus slave and as a VMEbus interrupter.
A19	GND	GROUND - connected to the MVME327A ground plane.
A20	IACK*	INTERRUPT ACKNOWLEDGE - signal that indicates an interrupt acknowledge cycle on the VMEbus.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - IACKIN* and IACKOUT* form a daisy-chained signal. The MVME327A drives IACKOUT* low if there is an activated IACKIN* and the interrupt acknowledge level is not for this module.
A22	IACKOUT*	INTERRUPT ACKNOWLEDGE OUT - see IACKIN*.
A23	AM4	ADDRESS MODIFIER (bit 4) - one of the three-state lines that provide additional information about the address bus, such as size, and cycle type. It is driven by the MVME327A as a master and received by the MVME327A as a slave.
A24-A30	A07-A01	ADDRESS bus (bits 7-1) - seven of 31 three-state lines that specify an address in the memory map. They are driven by the MVME327A as a master and received by the MVME327A as a slave.

TABLE 4-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A31	-12 VDC	-12 Vdc power.
A32	+5 VDC	+5 Vdc power - used by the logic circuits on the MVME327A. Connected to the MVME327A +5V plane.
B1	BBSY*	BUS BUSY - this signal is driven true by the MVME327A when it is VMEbus master.
B2	BCLR*	Not used.
B3	ACFAIL*	AC FAILURE - the MVME327A monitors this signal line to detect ac power failure.
B4	BG0IN*	BUS GRANT IN (level 0) - this signal going true at the input to the MVME327A indicates that it may become VMEbus master if it is configured for level 0. If the MVME327A is not requesting VMEbus mastership, then it drives the BG0OUT* signal line low. The other three bus grant lines are tied directly to the corresponding bus grant out lines.
B5	BG0OUT*	BUS GRANT OUT (level 0) - see BG0IN*.
B6	BG1IN*	BUS GRANT IN (level 1) - same as BG0IN* on pin B4.
B7	BG1OUT*	BUS GRANT OUT (level 1) - same as BG0OUT* on pin B5.
B8	BG2IN*	BUS GRANT IN (level 2) - same as BG0IN* on pin B4.
B9	BG2OUT*	BUS GRANT OUT (level 2) - same as BG0OUT* on pin B5.
B10	BG3IN*	BUS GRANT IN (level 3) - same as BG0IN* on pin B4.
B11	BG3OUT*	BUS GRANT OUT (level 3) - same as BG0OUT* on pin B5.
B12	BR0*	BUS REQUEST (level 0) - signal line driven by the MVME327A when it desires to become VMEbus master (if it is configured for level 0).
B13	BR1*	BUS REQUEST (level 1) - same as BR0* on pin B12.

TABLE 4-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B14	BR2*	BUS REQUEST (level 2) - same as BR0* on pin B12.
B15	BR3*	BUS REQUEST (level 3) - same as BR0* on pin B12.
B16-B19	AM0-AM3	ADDRESS MODIFIER (bits 0-3) - same as AM4 on pin A23.
B20	GND	GROUND - connected to the MVME327A ground plane.
B21	SERCLK	Not used.
B22	SERDAT*	Not used.
B23	GND	GROUND - connected to the MVME327A ground plane.
B24-B30	IRQ7*-IRQ1*	INTERRUPT REQUEST (7-1) - seven prioritized interrupt requests to the VMEbus driven by the MVME327A. Level 7 is the highest priority.
B31	+5V STDBY	Not used.
B32	+5 VDC	+5 Vdc power - same as +5 VDC on pin A32.
C1-C8	D08-D15	DATA bus (bits 8-15) - same as D00-D07 on pins A1-A8.
C9	GND	GROUND - connected to the MVME327A ground plane.
C10	SYSFAIL*	SYSTEM FAIL - signal driven by the MVME327A when [DRVSFAIL] is true. BRDFAIL is true and INHIBIT SYSFAIL is false.
C11	BERR*	BUS ERROR - monitored by the MVME327A when it is the VMEbus master.
C12	SYSRESET*	SYSTEM RESET - An input to the MVME327A that causes all of its devices to be reset.
C13	LWORD*	LONGWORD - signal driven true by the MVME327A when it does a 32-bit data transfer over the VMEbus. Also monitored by the MVME327A to distinguish 32-bit from 16-bit data accesses to its RAM from the VMEbus. 32-bit transfers are not allowed when the MVME327A is a VMEbus slave.

TABLE 4-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C14	AM5	ADDRESS MODIFIER (bit 5) - same as AM4 on pin A23.
C15-C30	A23-A08	ADDRESS bus (bits 23-08) - 16 of 31 three-state lines that specify an address in the memory map. They are driven by the MVME327A as a master. A15-A01 are received by the MVME327A as a slave.
C31	+12 VDC	+12 Vdc power.
C32	+5 VDC	+5 Vdc power - used by the logic circuits on the MVME327A. Connected to the MVME327A +5V plane.

4.2.2 Connector P2 Interconnect Signals

Connector P2 is a standard DIN 41612 triple-row, 96-pin male connector. The MVME327A interconnects with the VMEbus through rows A, B, and C of P1 and through row B of P2. Connector P2 is pin-for-pin compatible with connector P2 on the P2 adapter. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 4-2.

TABLE 4-2. Connector P2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A3	PDB1*,PDB3* PDB5*	DATA BUS (SCSI) (bits 1, 3, 5) - three of eight data bits on the SCSI bus.
A4-A32	GND	GROUND - connected to the MVME327A ground plane.
B1	+5 VDC	+5 Vdc power - used by the logic circuits on the MVME327A. Connected to the MVME327A +5V plane.
B2	GND	GROUND - connected to the MVME327A ground plane.
B3	Reserved	Not used.
B4-B11	A24-A31	ADDRESS bus (bits 24-31) - eight of 31 three-state lines that specify an address in the memory map. They are driven by the MVME327A as a master.

TABLE 4-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B12	GND	GROUND - connected to MVME327A ground plane.
B13	+5 VDC	+5 Vdc power - used by the logic circuits on the MVME327A. Connected to the MVME327A +5V plane.
B14-B21	D16-D23	DATA bus (bits 16-23) - eight of 32 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
B22	GND	GROUND - connected to MVME327A ground plane.
B23-B30	D24-D31	DATA bus (bits 24-31) - eight of 32 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
B31	GND	GROUND - connected to MVME327A ground plane.
B32	+5 VDC	+5 Vdc power - used by the logic circuits on the MVME327A. Connected to the MVME327A +5V plane.
C1-C5	PDB0*,PDB2*, PDB4*,PDB6*, PDB7*	DATA BUS (SCSI) (bits 0, 2, 4, 6, 7) - same as PDB1, PDB3, PDB5 on P2 pin A1-A3. Bit seven is the most significant bit and the highest priority during the arbitration phase.
C6	PDBP*	DATA BUS PARITY (SCSI) - data parity is odd. Use of parity is a system option. Parity is not valid during arbitration phase.
C7	PTERMPWR	TERMINATOR POWER (SCSI)
C8	PATN*	ATTENTION (SCSI) - signal driven by the initiator. Indicates the attention condition.
C9	PBSY*	BUS BUSY (SCSI) - signal that indicates that the bus is being used.
C10	PACK*	ACKNOWLEDGE (SCSI) - signal driven by an initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.
C11	PRST*	RESET (SCSI) - signal that indicates the RESET condition.
C12	PMSG*	MESSAGE (SCSI) - signal driven by the target during the message phases.

TABLE 4-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C13	PSEL*	SELECT (SCSI) - signal used by the initiator to select a target or by a target to reselect an initiator.
C14	PC/D*	CONTROL/DATA (SCSI) - signal driven by the target. It indicates whether control or data information is on the data bus.
C15	PREQ*	REQUEST (SCSI) - signal driven by the target to indicate a request for a REQ/ACK data transfer handshake.
C16	PI/O*	INPUT/OUTPUT (SCSI) - signal driven by a target which controls the direction of data movement on the SCSI bus. This signal is also used to distinguish between selection and reselection phases.
C17	RPM*	DENSITY (FLOPPY) - allows control of motor speed/density on dual speed/density drives. 0 = high density. 1 = normal density.
C18	SELECT4*	DRIVE SELECT 4 (FLOPPY) - this signal, when low, connects the drive 4 I/O interface to the control lines.
C19	INDEX*	INDEX (FLOPPY) - this signal is driven by the drive once each revolution to indicate the beginning of a track. This line is valid on the high to low transition.
C20	SELECT1*	DRIVE SELECT 1 (FLOPPY) - this signal, when low, connects the drive 1 I/O interface to the control lines.
C21	SELECT2*	DRIVE SELECT 2 (FLOPPY) - this signal, when low, connects the drive 2 I/O interface to the control lines.
C22	SELECT3*	DRIVE SELECT 3 (FLOPPY) - this signal, when low, connects the drive 3 I/O interface to the control lines.
C23	MOTORON*	MOTOR ON (FLOPPY) - when this signal is low, the motor(s) in the 5-1/4 inch floppy drives are energized and start accelerating to operating speed.

TABLE 4-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C24	DIRECTION*	DIRECTION (FLOPPY) - this signal defines the direction of motion of the read/write heads when the STEP line (pin C25) is pulsed. A high level when the STEP line is pulsed causes the read/write heads to move out away from the center of the disk. A low level when the STEP line is pulsed causes the read/write heads to move in towards the center of the disk.
C25	STEP*	HEAD STEP (FLOPPY) - this signal causes the read/write heads to move in the direction defined by the DIRECTION signal (pin C24).
C26	WRITE DATA*	WRITE DATA (FLOPPY) - this line carries the encoded write data to be recorded on the diskette.
C27	WRITE GATE*	WRITE GATE (FLOPPY) - this signal controls the read/write mode of the selected drive. The write circuitry is enabled when WRITE GATE is low, provided the diskette is not write protected.
C28	TRACK 00*	TRACK ZERO (FLOPPY) - this signal indicates the read/write heads are positioned at cylinder zero (the outermost data track).
C29	WRITE PROTECT*	WRITE PROTECT (FLOPPY) - this signal indicates the diskette in the drive is write-protected.
C30	READ DATA*	READ DATA (FLOPPY) - this line carries composite serial data from the selected diskette to the controller.
C31	SIDE SELECT*	SIDE SELECT (FLOPPY) - this signal indicates when read/write head is used on the selected drive. When this signal is high, head 0 is selected. When this signal is low, head 1 is selected.
C32	READY*	READY (FLOPPY) - this line is an output from a floppy drive indicating that the drive is ready.

4.3 PARTS LIST

The components of the MVME327A are listed in Table 4-3. The parts locations are shown in Figure 4-1. These parts reflect the latest issue of hardware at the time of printing.

TABLE 4-3. MVME327A Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8550B01A	Printed wiring board
CR1	48NW9607A01	Rectifier, 1N4001
C1-C3,C5-C14, C16-C24,C26-C34,C36-C47, C49-C56,C59-C72	21NW9632A03	Capacitor, fixed, ceramic, 0.1 uF @ 50 Vdc
C4,C15,C25, C35,C48,C57, C58	23NW9618A71	Capacitor, electrolytic, 47 uF @ 10 Vdc
DL1	51NW9615W46	Delay module, DS1000M-50
DS1	48NW9612A49	LED, red
F1,F2	65NW9622A26	Fuse, micro, 1 amp, 125 V
J1-J5,J7,J8	29NW9805C07	Pin, autoinsert (82 required)
J6	28NW9802F66	Header, 34-pin
P1,P2	28NW9802E51	Connector, 96-pin
R1	06SW-124A25	Resistor, fixed, film, 100 ohm, 5%, 1/4 W
R2-R5,R7,R11, R14,R15,R21, R22,R23,R25-R27,R29-R35	51NW9626B56	Resistor network, 9/10k ohm
R6,R8	51NW9626B93	Resistor network, 4/22 ohm
R9,R10,R12, R13,R16,R24, R28	51NW9626B59	Resistor network, 9/2.7k ohm
R17-R20	51NW9626A60	Resistor network, 6/220/330 ohm

TABLE 4-3. MVME327A Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U1-U3	(NOTE)	I.C. programmed
U4,U8,U82, U90	51NW9615V98	I.C. N74F652N
U5-U7,U9,U10	(NOTE)	I.C. programmed
U11,U74	51NW9615R55	I.C. N74F38N
U12	(NOTE)	I.C. programmed
U13,U18,U94	51NW9615J39	I.C. 74F74PC
U14,U15	(NOTE)	I.C. programmed
U16,U21,U26, U38,U40,U70, U71,U78,U86	51NW9615V50	I.C. IDT74FCT244AP
U17	51NW9615U16	I.C. IDT74AHCT240P
U19,U20	(NOTE)	I.C. programmed
U22,U27,U39, U41,U67	51NW9615W05	I.C. IDT74FCT373AP
U23,U28	51NW9615V26	I.C. N74HCT4020N
U24,U25	(NOTE)	I.C. programmed
U29,U72	51NW9615V85	I.C. IDT74FCT374AP
U30	(NOTE)	I.C. programmed
U31	51NW9615H83	I.C. SN74LS641-1N
U32	51NW9615W07	I.C. IDT74FCT521AP
U33,U34	(NOTE)	I.C. programmed
U35,U55	51NW9615K71	I.C. 74F04PC
U36	51NW9615K66	I.C. 74F32PC
U37,U42	(NOTE)	I.C. programmed
U43	51NW9615Y33	I.C. 74F133N

TABLE 4-3. MVME327A Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U44	51NW9615U47	I.C. 74F113PC
U45,U46,U48	(NOTE)	I.C. programmed
U49	51NW9615M11	I.C. MC68010P10
U50,U87	51NW9615N32	I.C. 74F164PC
U51,U56,U81, U89	51NW9615V28	I.C. IDT74AHCT245P
U52,U57,U64, U66	51NW9615N26	I.C. SN74LS461NS
U53,U54,U58, U59	(NOTE)	I.C. programmed
U60,U61,U68, U69	51NW9615U69	I.C. UPD43256C-10
U62	51NW9615S88	I.C. MC68153P
U65	51NW9615V78	I.C. IDT74FCT823AP
U73	51NW9615K70	I.C. 74F08PC
U75,U76,U83	51NW9615V45	I.C. IDT7201SA50P
U77	51NW9615U45	I.C. WD33C93PL
U79	51NW9615V33	I.C. N74F14N
U80,U88	51NW9615P74	I.C. N74F373D
U85	51NW9615U63	I.C. WD37C65PL
U92	51NW9615V46	I.C. IDT720SA120P
U93	51NW9615U28	I.C. MC68230P10
Y1	48AW1015B12	Crystal oscillator, 32.0 MHz, 0.01%
Y2	48AW1015B03	Crystal oscillator, 20.0 MHz, 0.01%

TABLE 4-3. MVME327A Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	28NW9802E08	Connector, single socket (use at F1,F2)
	09NW9811A90	Socket, SIL, 8 pin (use at R17-R19)
	09-W4659B14	Socket, SIL, 14 pin (use at U60,U61,U68,U69, U75,U76,U83,U84,U92)
	09-W4659B16	Socket, SIL, 16 pin (use at U34,U42)
	09-W4659B20	Socket, SIL, 20 pin (use at U62,U77,U85)
	09NW9811A78	Socket, DIL, 20 pin (use at U9,U59)
	09-W4659B24	Socket, SIL, 24 pin (use at U93)
	09NW9811B01	Socket, DIL, 24 pin (use at U5,U12,U33,U46, U53,U58)
	09NW9811A16	Socket, DIL, 24 pin (use at U91)
	09-W4659B32	Socket, SIL, 32 pin (use at U49)
	29NW9805B17	Jumper, shorting, insulated (use at J1-J5, J7,J8)
	64-W5462B01	Front panel

NOTE: When ordering, use number labeled on part

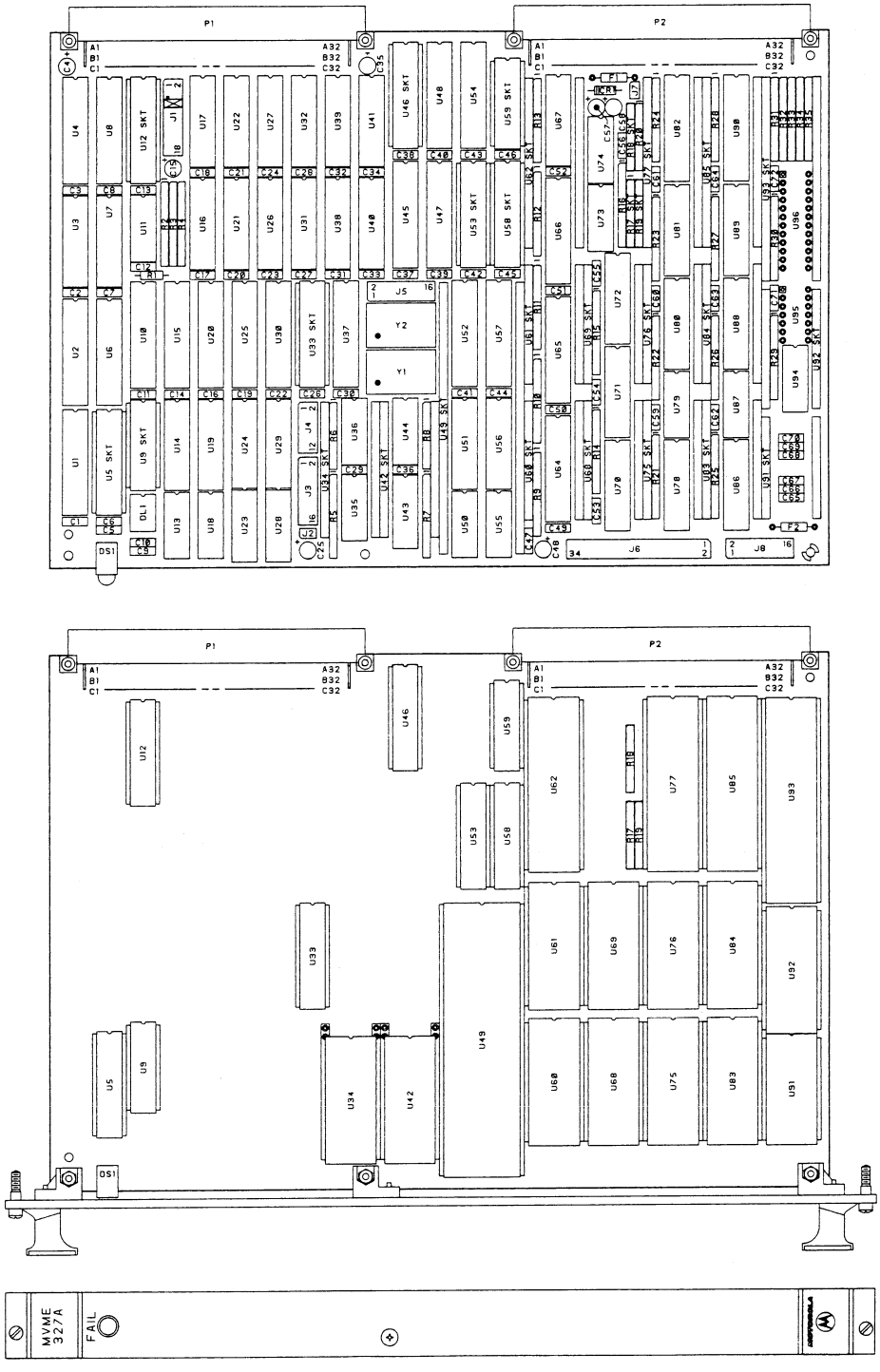


FIGURE 4-1. MVME327A Parts Location

4.4 SCHEMATIC DIAGRAM

The schematic diagram for the MVME327A is illustrated in Figure 4-2.

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3550B__, CURRENT REVISION/CONFIGURATION APPLIES.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, +/- 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
   ALL DELAYS ARE IN NS.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   <> DENOTES - VECTORED SIGNALS.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
7. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:
   (SHEET) 5 C7 (ZONE)

REF DES	TYPE (4)	GND	+5V
DL1	DELAY5M	4	8
U1	PALSF1	12	24
U2	PALVGNT	12	24
U3	PALVAM	10	20
U4	AS652	12	24
U5	PALIRQ	12	24
U6	PALVREQ	12	24
U7	PALVAM	10	20
U8	AS652	12	24
U9	PALVECT	10	20
U10	PALSTB	12	24
U11	F38	7	14
U12	PALSLAVE	12	24
U13	F74	7	14
U14	PALCNT	10	20
U15	PALBUF	12	24
U16	FCT244A	10	20
U17	AHCT240	10	20
U18	F74	7	14
U19	PALDMA1	10	20
U20	PALERR	12	24
U21	FCT244A	10	20
U22	FCT373A	10	20
U23	HCT4020	8	16
U24	SCSIFSTB	10	20
U25	PALVF1	12	24
U26	FCT244A	10	20
U27	FCT373A	10	20
U28	HCT4020	8	16
U29	FCT374A	10	20
U30	PALVF2	12	24
U31	LS641-1	10	20
U32	FCT521	10	20
U33	PALMAP4	12	24
U35	F04	7	14
U36	F32	7	14
U37	PALDTACK	12	24
U38	FCT244A	10	20
U39	FCT373A	10	20
U40	FCT244A	10	20
U41	FCT373A	10	20
U43	F133	8	16
U44	F113	7	14
U45	PALCOUNT	12	24
U46	PALSHREG	12	24
U47	PALCOUNT	12	24
U48	PALFLOP	12	24
U49	MC68010	16	14
		53	49
U50	F164	7	14
U51	AHCT245	10	20
U52	LS461A	12	24
U53	PALMAP	12	24
U54	PALBIM	12	24
U55	F04	7	14
U56	AHCT245	10	20
U57	LS461A	12	24
U58	PALMAP3	12	24
U59	PALMAP2	10	20
U60	TC55257	14	28

REF DES	TYPE (4)	GND	+5V
U61	TC55257	14	28
U62	MC68153	9	1
		10	11
		20	21
		31	30
U64	LS461A	12	24
U65	F823	12	24
U66	LS461A	12	24
U67	FCT373A	10	20
U68	TC55257	14	28
U69	TC55257	14	28
U70	FCT244A	10	20
U71	FCT244A	10	20
U72	F74	7	14
U73	F08	7	14
U74	F38	7	14
U75	IDT7201	14	28
U76	IDT7201	14	28
U77	WD33C93	3	40
		20	
		28	
		35	
U78	FCT244A	10	20
U79	F14	7	14
U80	F373	10	20
U81	AHCT245	10	20
U82	AS652	12	24
U83	IDT7201	14	28
U84	IDT7201	14	28
U85	WD37C65	31	40
U86	FCT244A	10	20
U87	F164	7	14
U88	F373	10	20
U89	AHCT245	10	20
U90	AS652	12	24
U91	MK48T02	12	24
U92	IDT7202	14	28
U93	MC68230	38	12
U94	F74	7	14
Y1	XTALOSC	7	14
Y2	XTALOSC	7	14

REF DES	SH
C1	2
C2	2
C3	2
C4	2
C5	2
C6	2
C7	2
C8	2
C9	2
C10	2
C11	2
C12	2
C13	2
C14	2
C15	2
C16	2
C17	2
C18	2
C19	2
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C30	2
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C45	2
C46	2
C47	2
C48	2
C49	2
C50	2
C51	2
C52	2
C53	2
C54	2
C55	2
C56	2
C57	2
C58	17
C59	2
C60	2

REF DES	SH
C61	2
C62	2
C63	2
C64	2
C65	2
C66	2
C67	2
C68	2
C69	2
C70	2
C71	2
C72	2
CR1	17
DL1	19
DS1	11
F1	17
F2	2
J1	13
J2	11
J3	20
J4	20
J5	10
J6	2
J7	17
J8	22
P1	3
P2	4
R1	11
R2	23
R3	2
R3	13
R3	16
R3	18
R3	19
R4	10
R5	7
R5	11
R5	13
R5	15
R5	19
R5	20
R6	7
R6	16
R7	2
R7	6
R7	18
R8	18
R9	6
R10	8
R11	2
R11	10
R11	11
R11	15
R11	23
R12	11
R13	8
R14	9
R15	9
R16	2
R16	10

REF DES	SH
R16	17
R16	18
R16	22
R17	17
R18	17
R19	17
R20	12
R21	8
R22	9
R23	9
R24	8
R25	22
R26	9
R27	9
R28	8
R29	9
R30	7
R30	14
R30	17
R30	22
R31	8
R32	11
R32	12
R32	14
R33	2
R33	7
R33	10
R33	14
R34	17
R35	12
R36	16
R37	12
U1	16
U2	13
U3	23
U4	8
U5	18
U6	13
U7	23
U8	8
U9	18
U10	19
U11	2
U11	11
U11	13
U12	10
U13	13
U13	16
U14	15
U15	20
U16	23
U17	20
U18	11
U18	13
U19	19
U20	11
U21	10
U21	19
U22	9
U23	11

REF DES	SH
U24	16
U25	16
U26	9
U27	9
U28	20
U29	16
U30	16
U31	11
U32	10
U33	7
U34	21
U35	2
U35	7
U35	13
U35	18
U35	19
U36	2
U36	17
U36	20
U37	6
U38	9
U39	9
U40	9
U41	10
U42	21
U43	7
U44	18
U45	15
U46	22
U47	15
U48	12
U49	6
U50	6
U51	8
U52	15
U53	7
U54	11
U55	2
U55	6
U55	10
U55	11
U55	13
U55	17
U56	8
U57	15
U58	7
U59	7
U60	21
U61	21
U62	11
U64	15
U65	9
U66	15
U67	9
U68	21
U69	21
U70	10
U71	22
U72	14
U73	14

REF DES	SH
U73	17
U74	2
U74	12
U74	17
U75	14
U76	14
U77	17
U78	22
U79	2
U79	12
U79	17
U79	22
U80	14
U81	17
U82	8
U83	14
U84	14
U85	12
U86	22
U87	10
U88	14
U89	12
U90	8
U91	23
U92	12
U93	22
U94	14
U94	17
U95	2
U96	2
Y1	18
Y2	18

POWER AND GROUND TABLES
63DW3550B0C REV C SH 1 OF 23

FIGURE 4-2. MVME327A Schematic Diagram

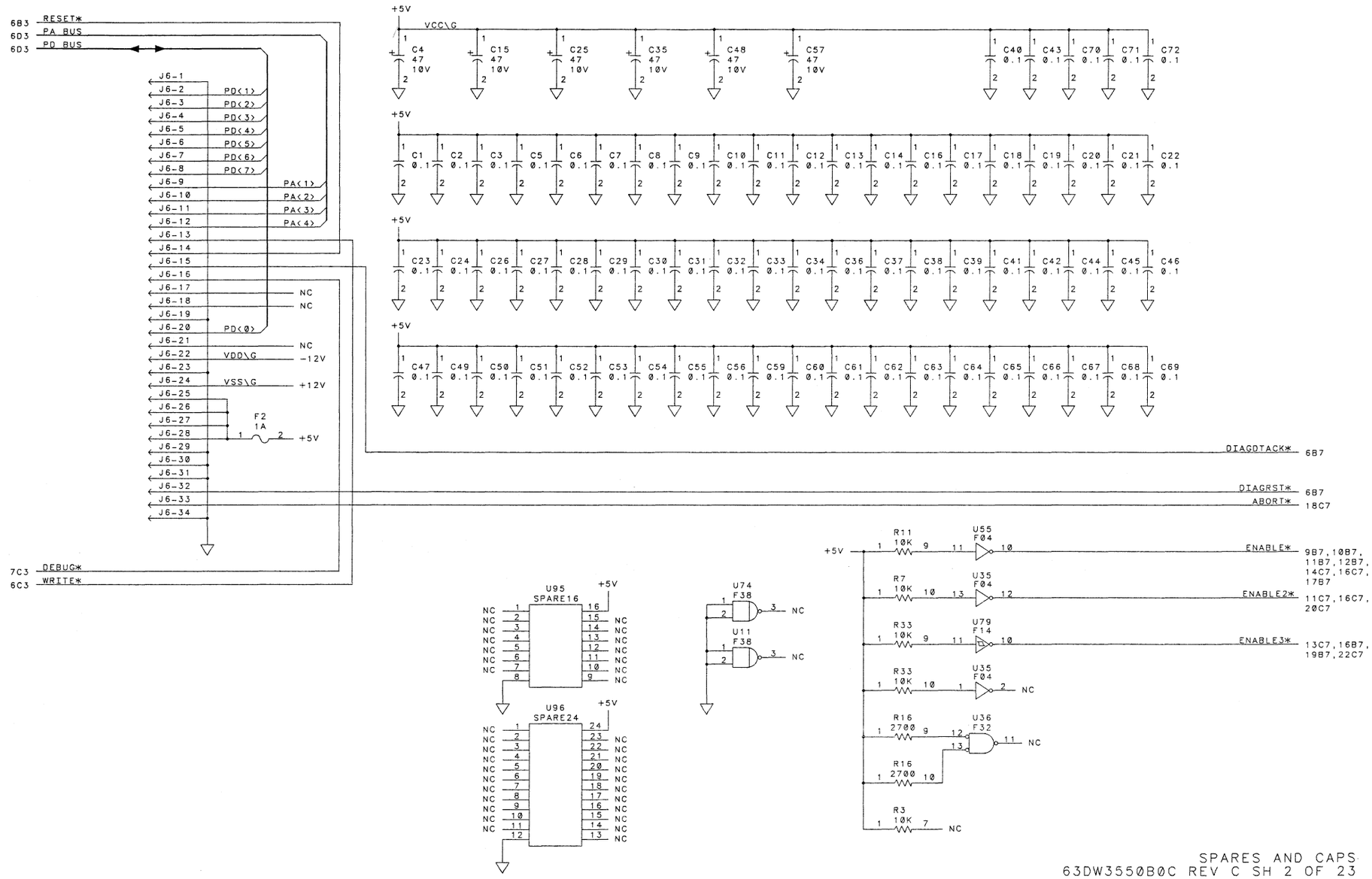
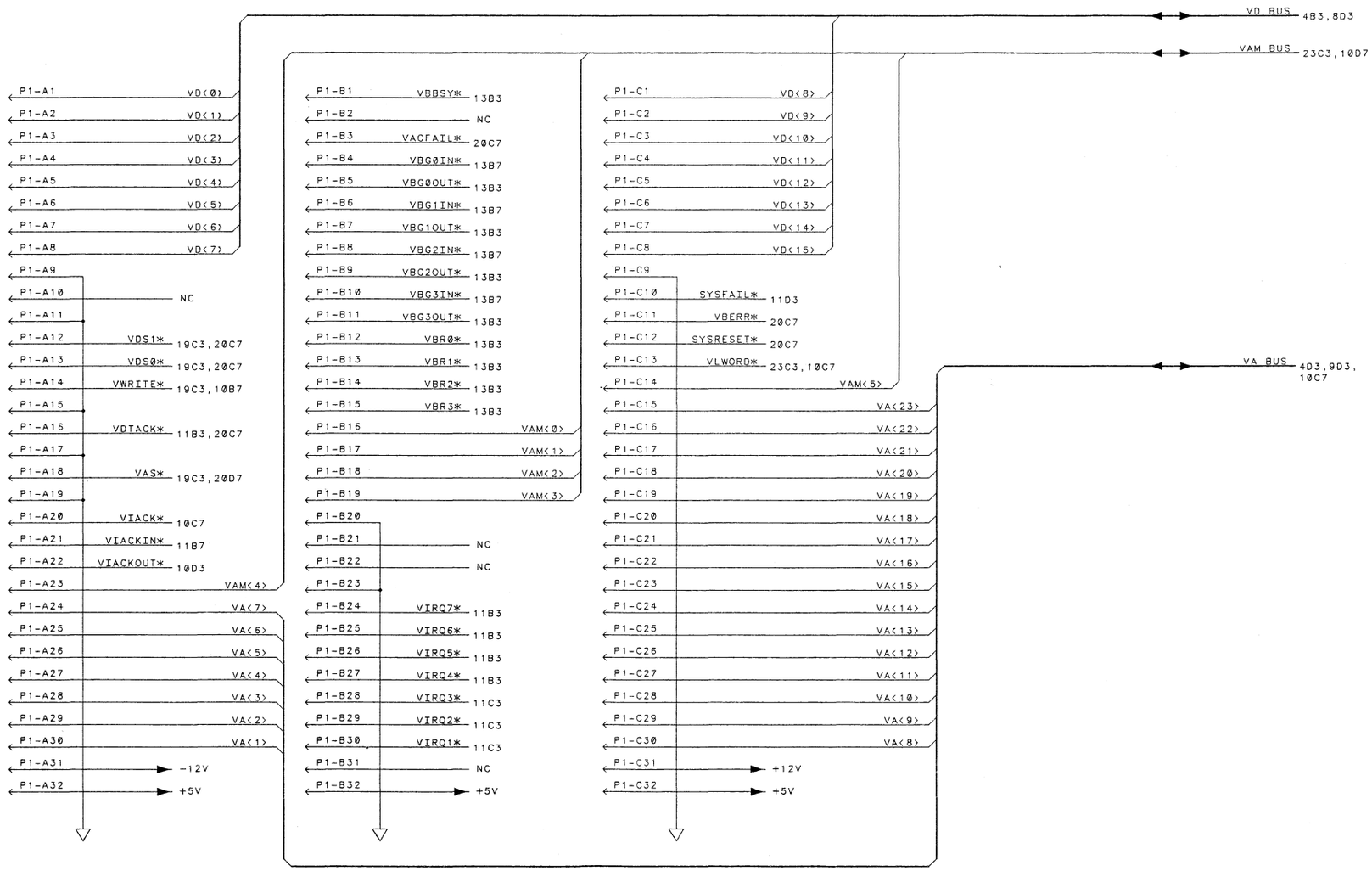
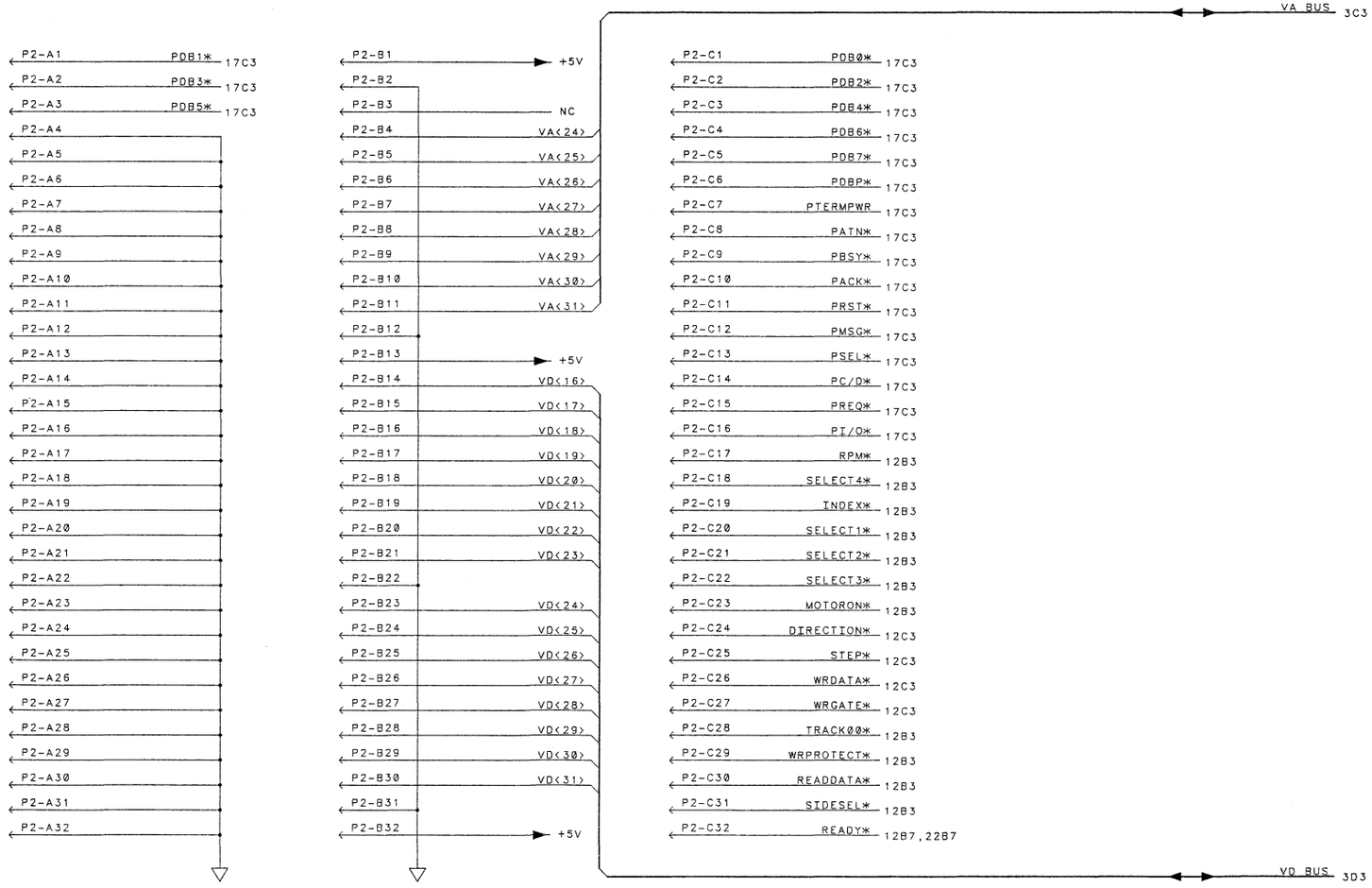


FIGURE 4-2. MVME327A Schematic Diagram 4-17/4-18



CONNECTOR P1
63DW3550B0C REV C SH 3 OF 23

FIGURE 4-2. MVME327A Schematic Diagram



CONNECTOR P2
63DW3550B0C REV C SH 4 OF 23

FIGURE 4-2. MVME327A Schematic Diagram 4-21/4-22

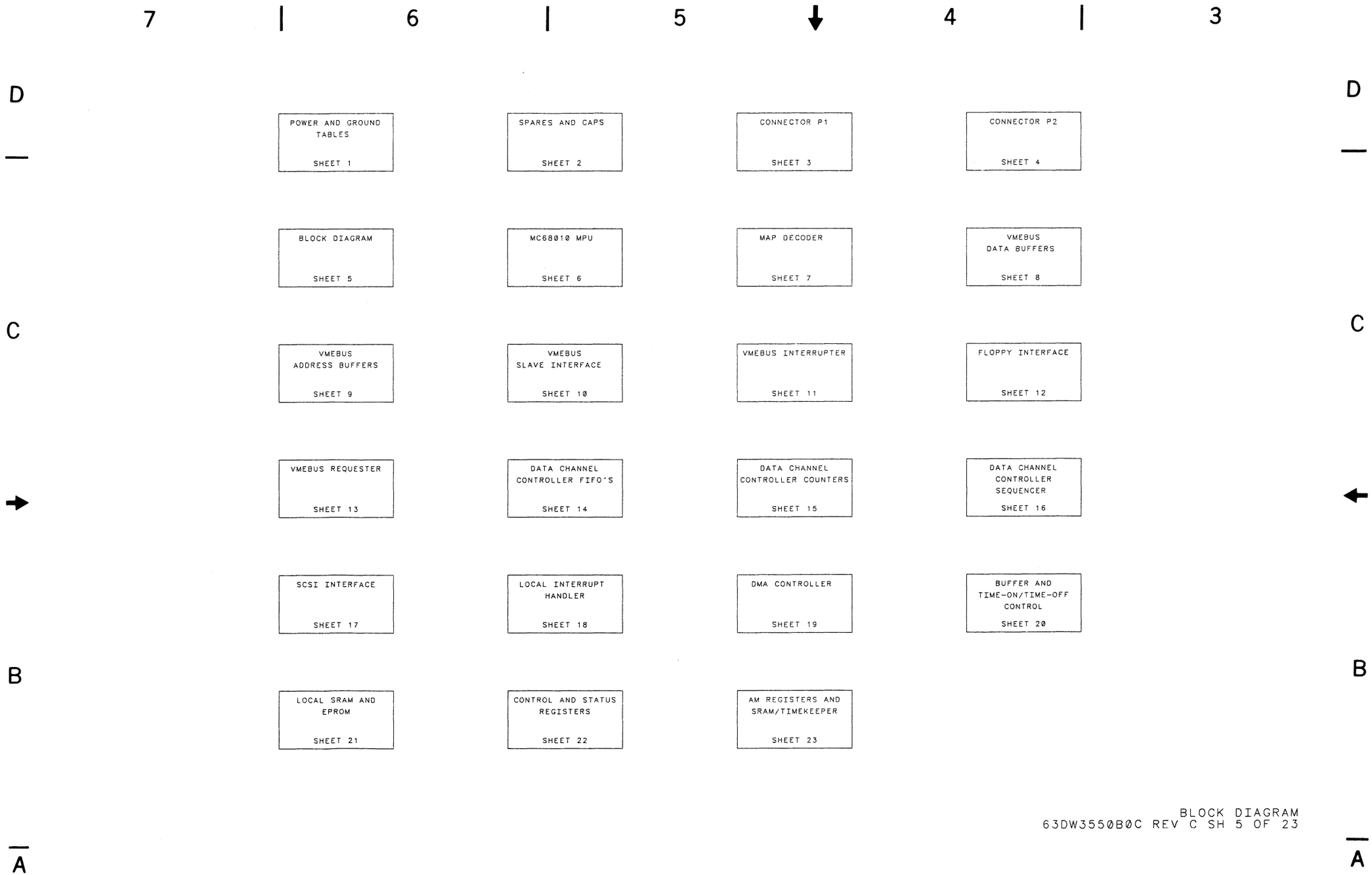
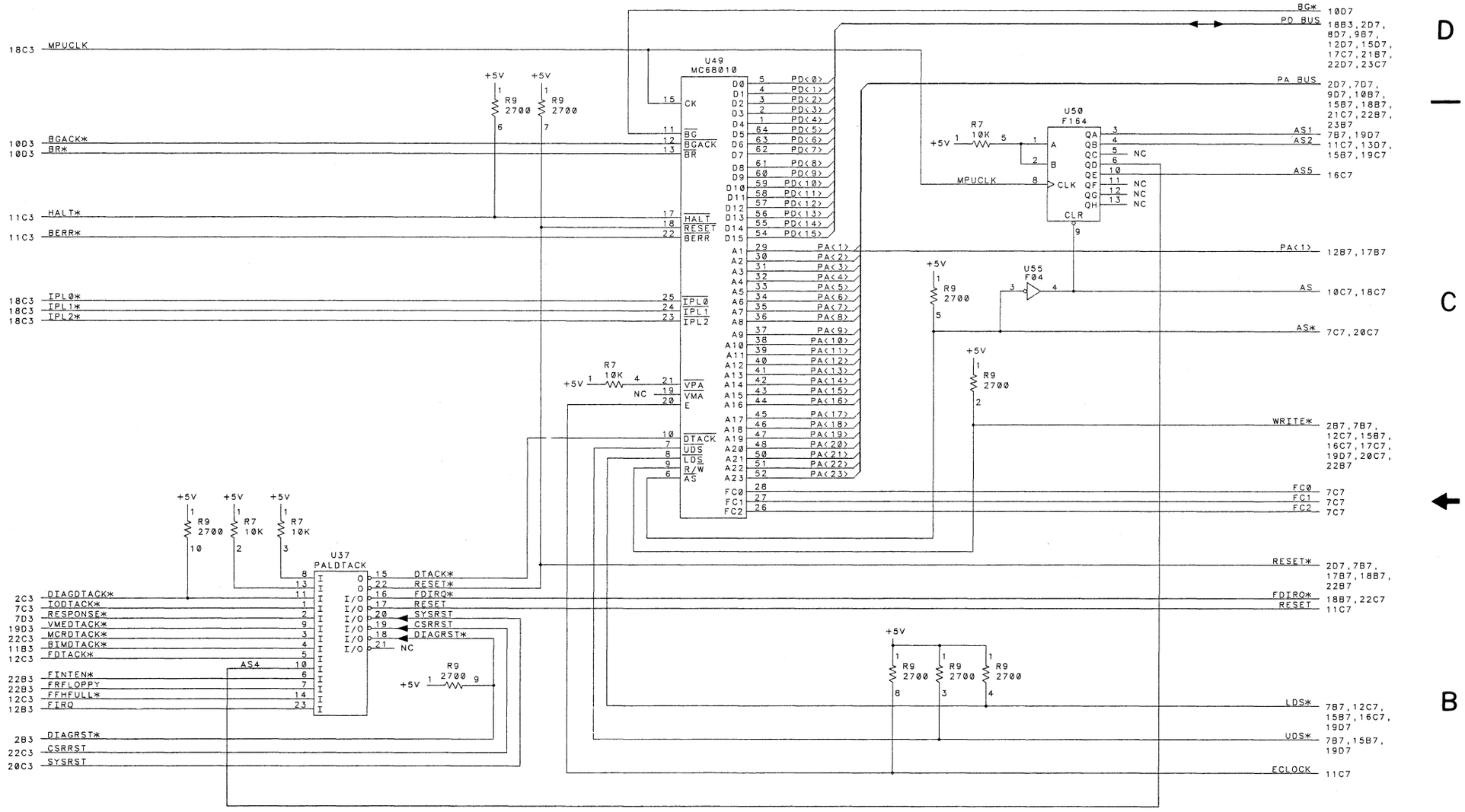


FIGURE 4-2. MVME327A Schematic Diagram



MPU
63DW3550B0C REV C SH 6 OF 23

FIGURE 4-2. MVME327A Schematic Diagram 4-25/4-26

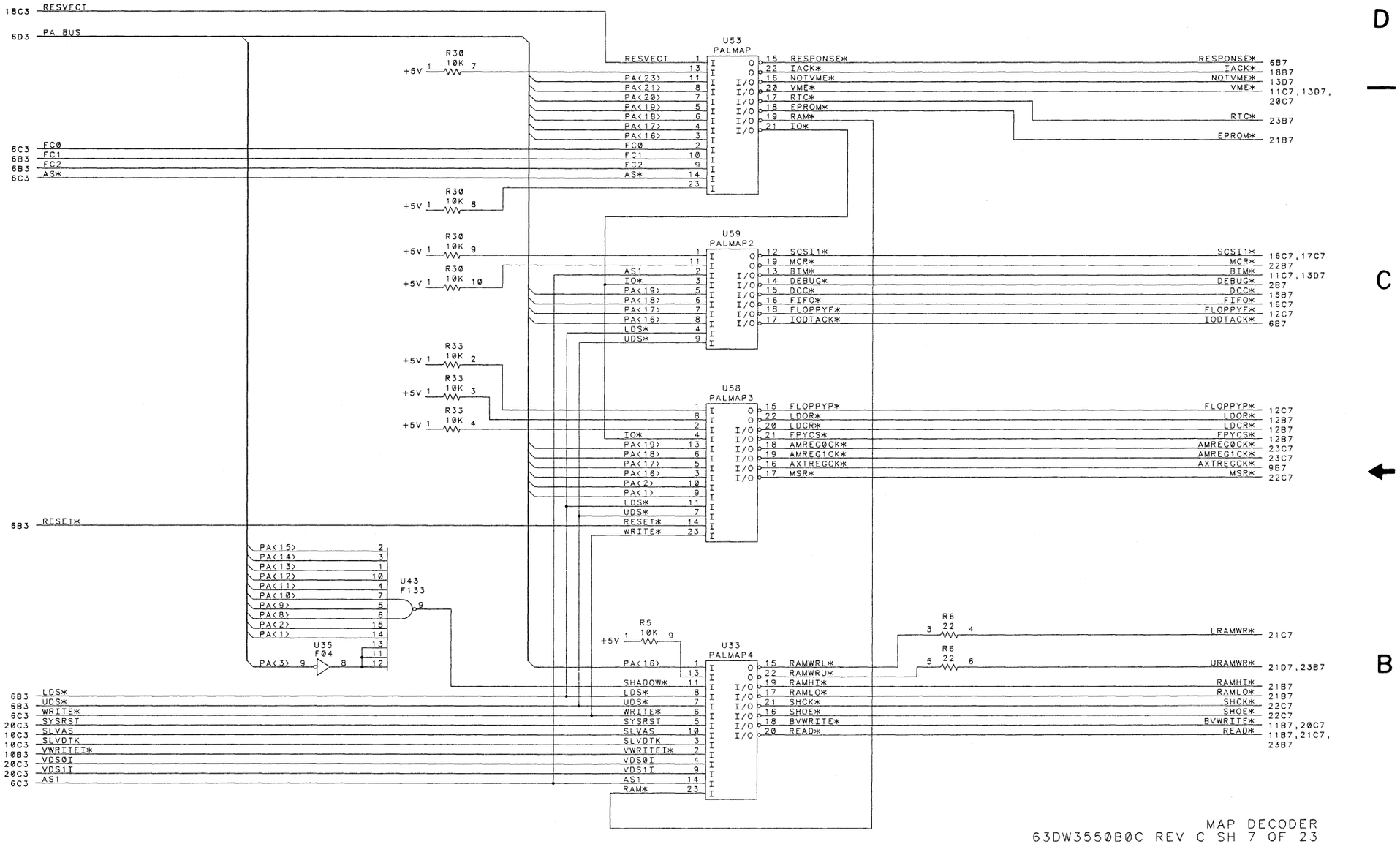


FIGURE 4-2. MVME327A Schematic Diagram 4-27/4-28

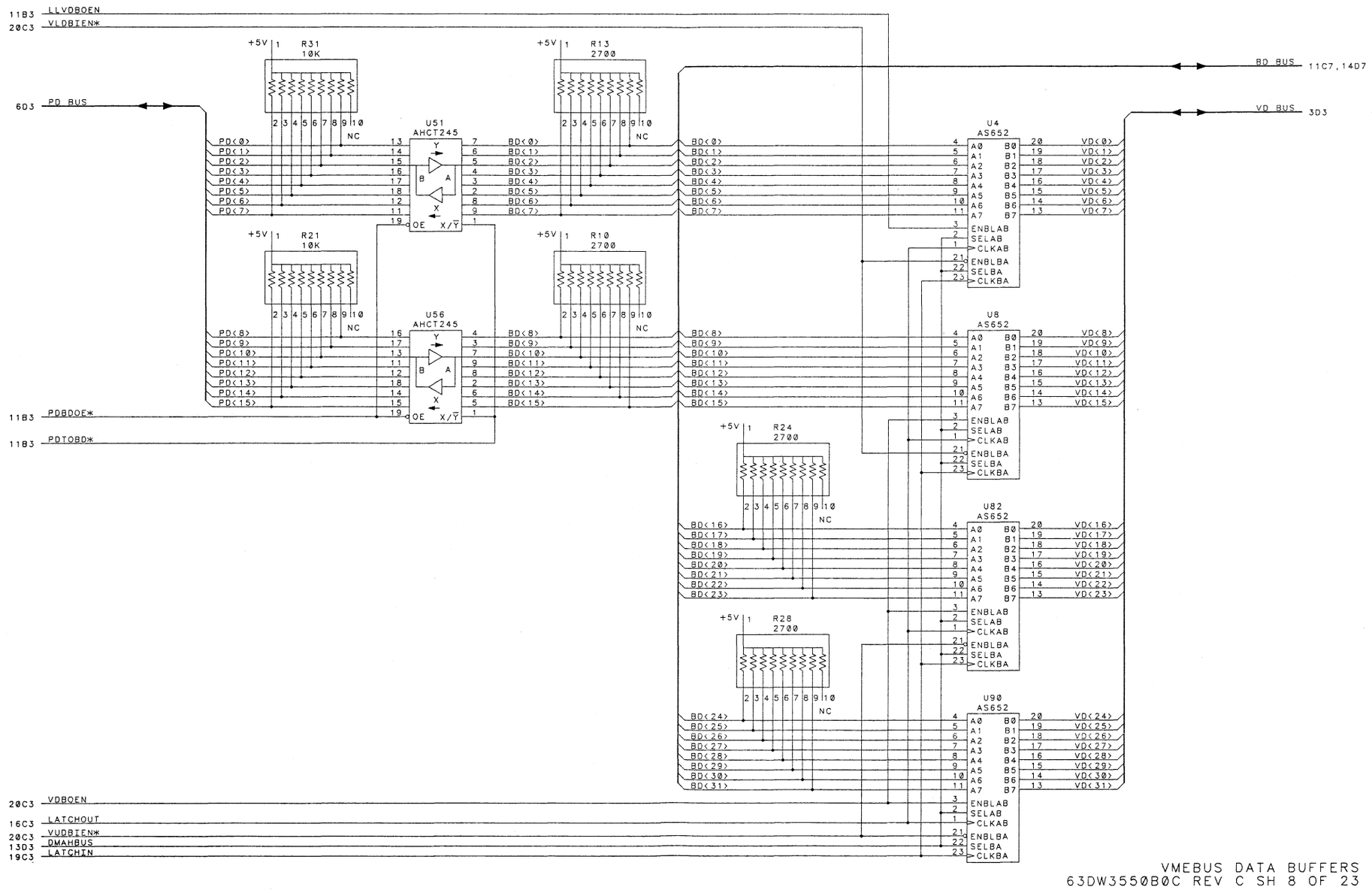


FIGURE 4-2. MVME327A Schematic Diagram 4-29/4-30

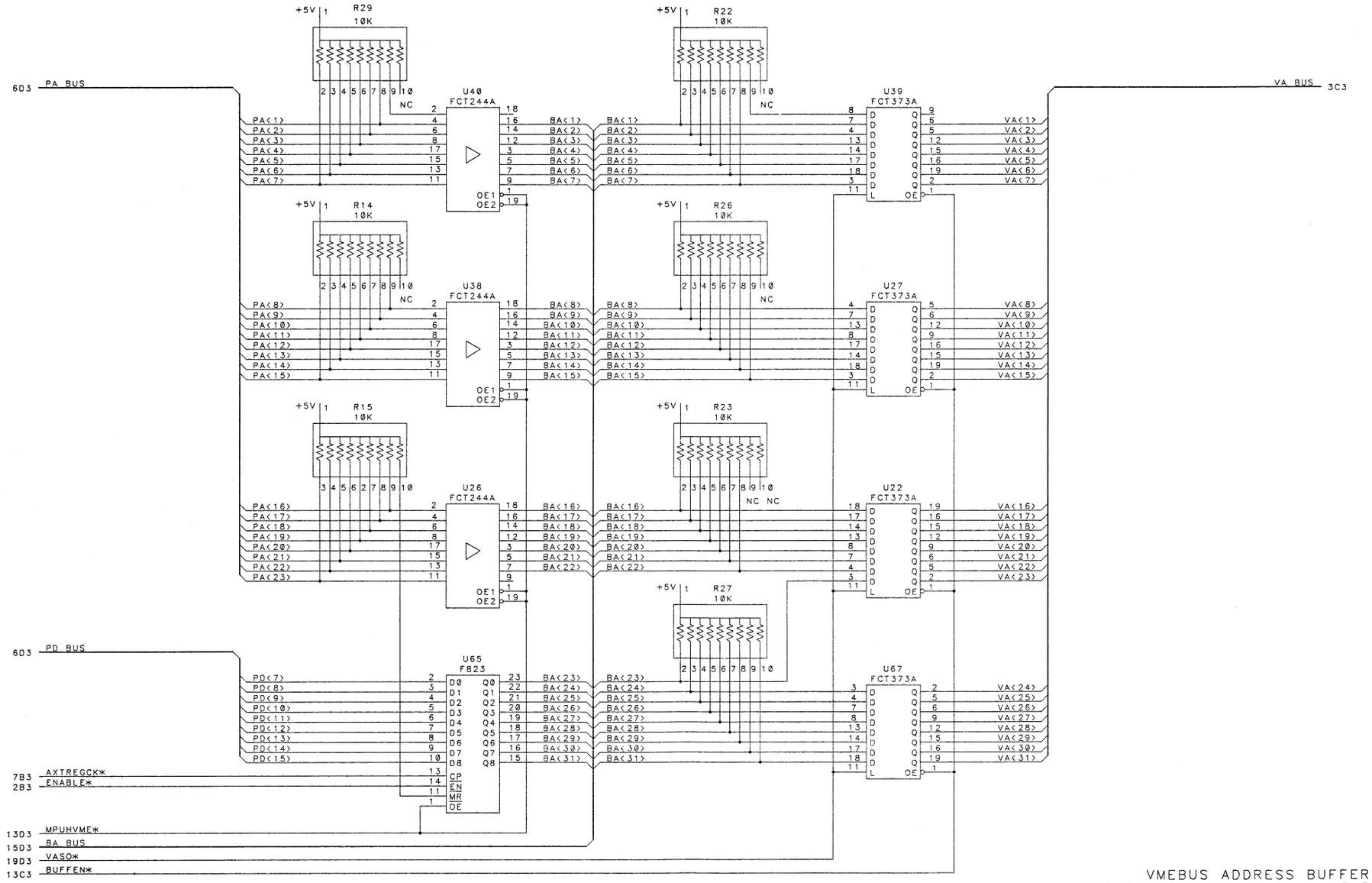
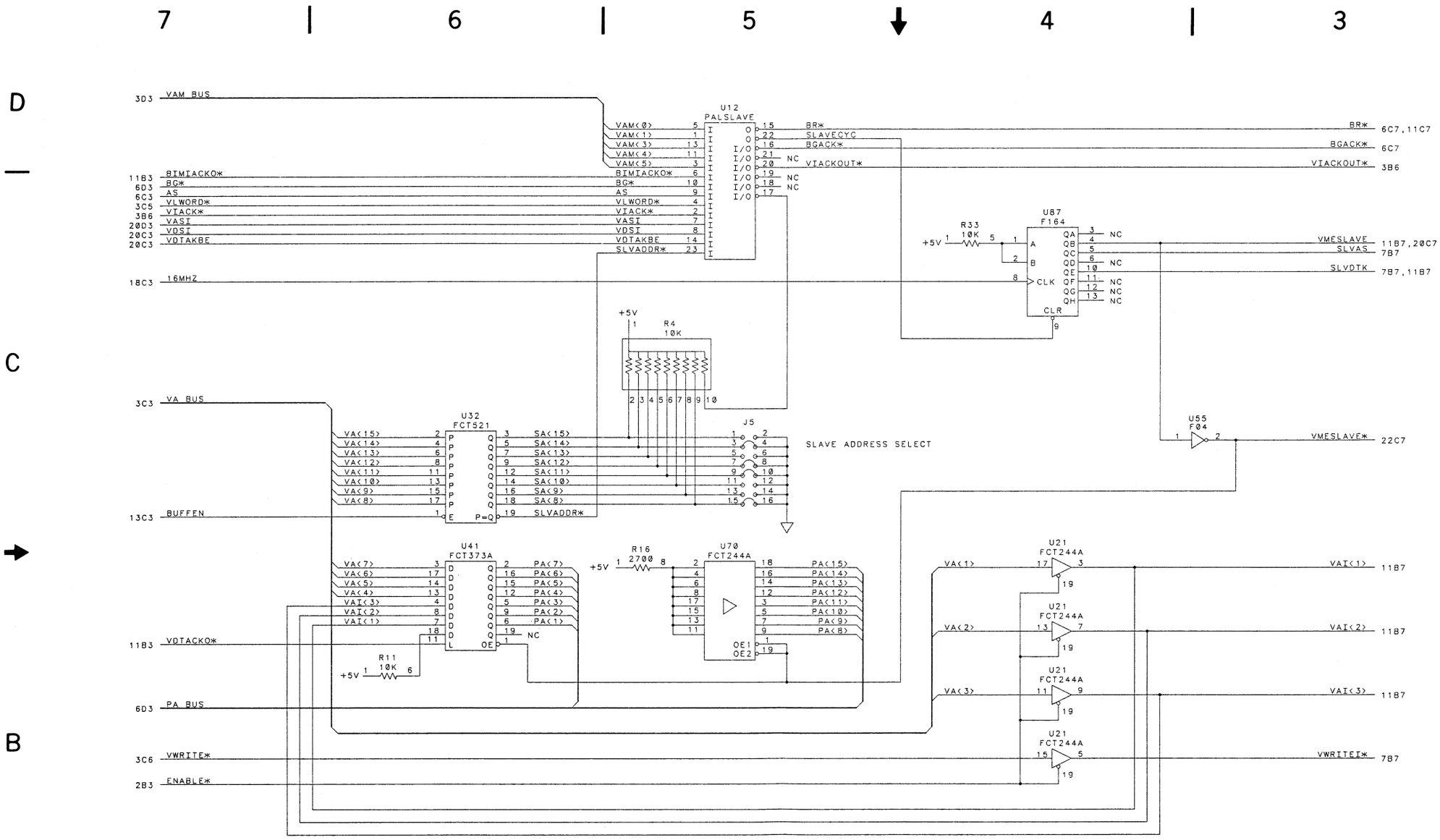


FIGURE 4-2. MVME327A Schematic Diagram 4-31/4-32



VMEBUS SLAVE INTERFACE
63DW3550B0C REV C SH 10 OF 23

FIGURE 4-2. MVME327A Schematic Diagram 4-33/4-34

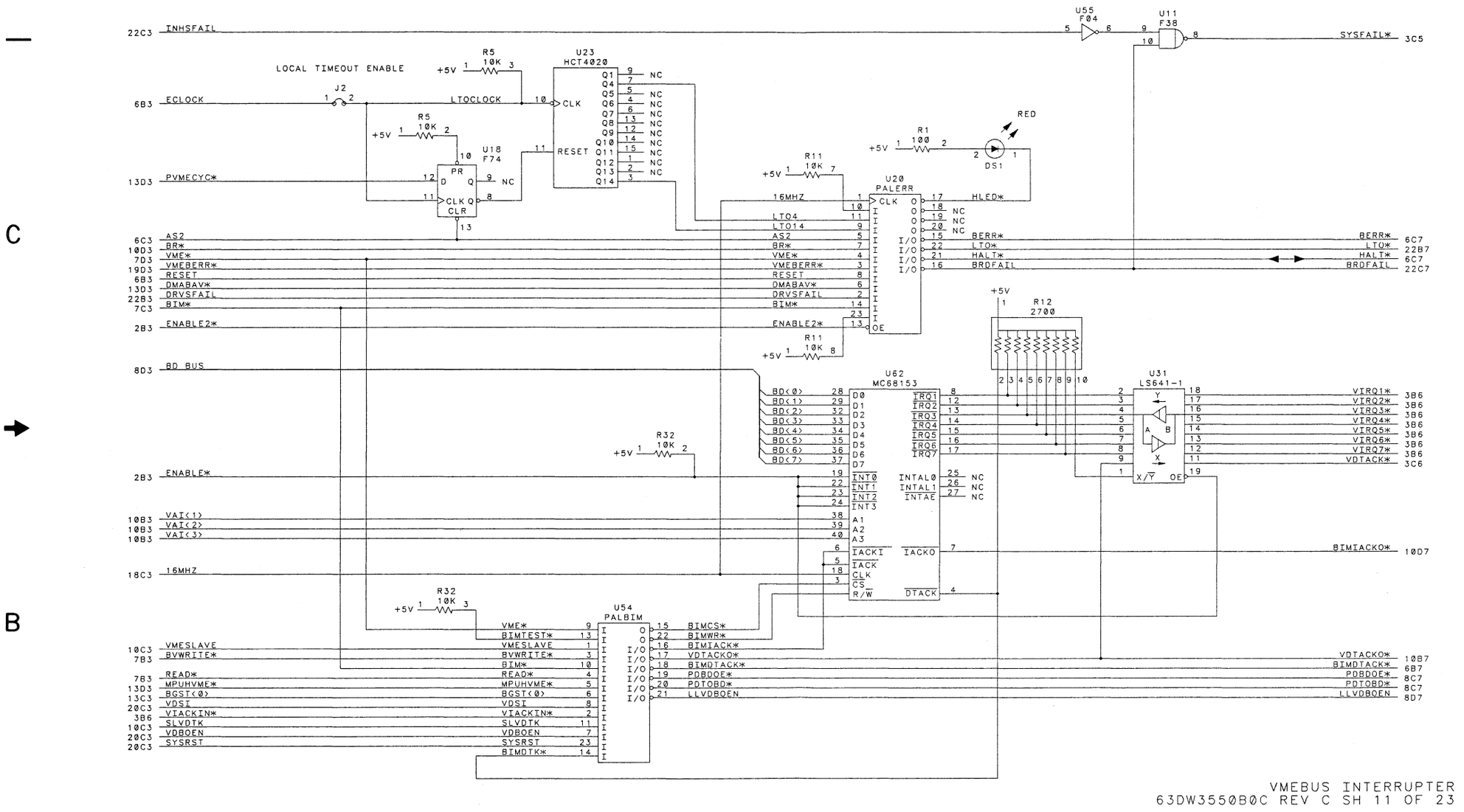


FIGURE 4-2. MVME327A Schematic Diagram

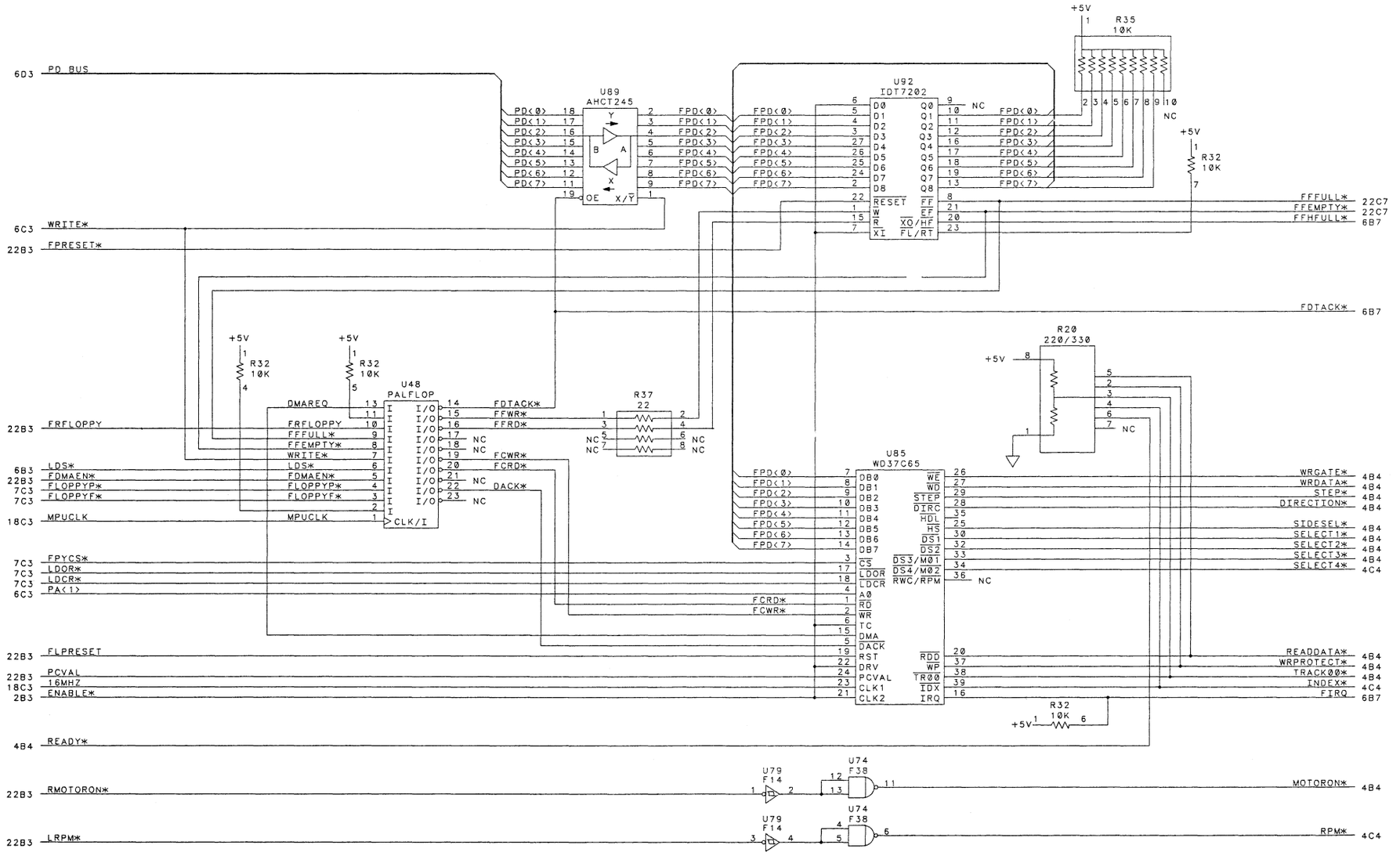


FIGURE 4-2. MVME327A Schematic Diagram 4-37/4-38

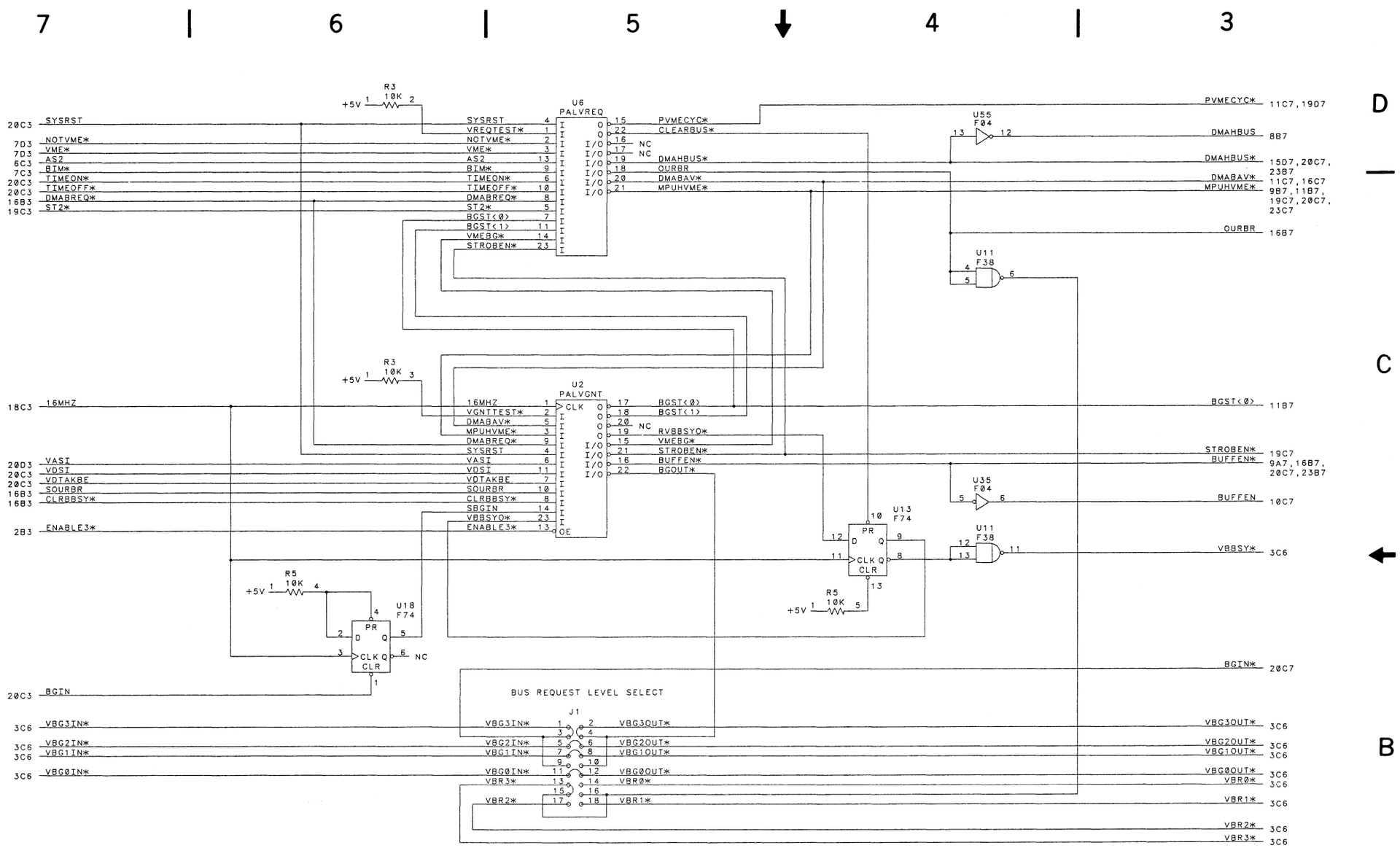


FIGURE 4-2. MVME327A Schematic Diagram 4-39/4-40

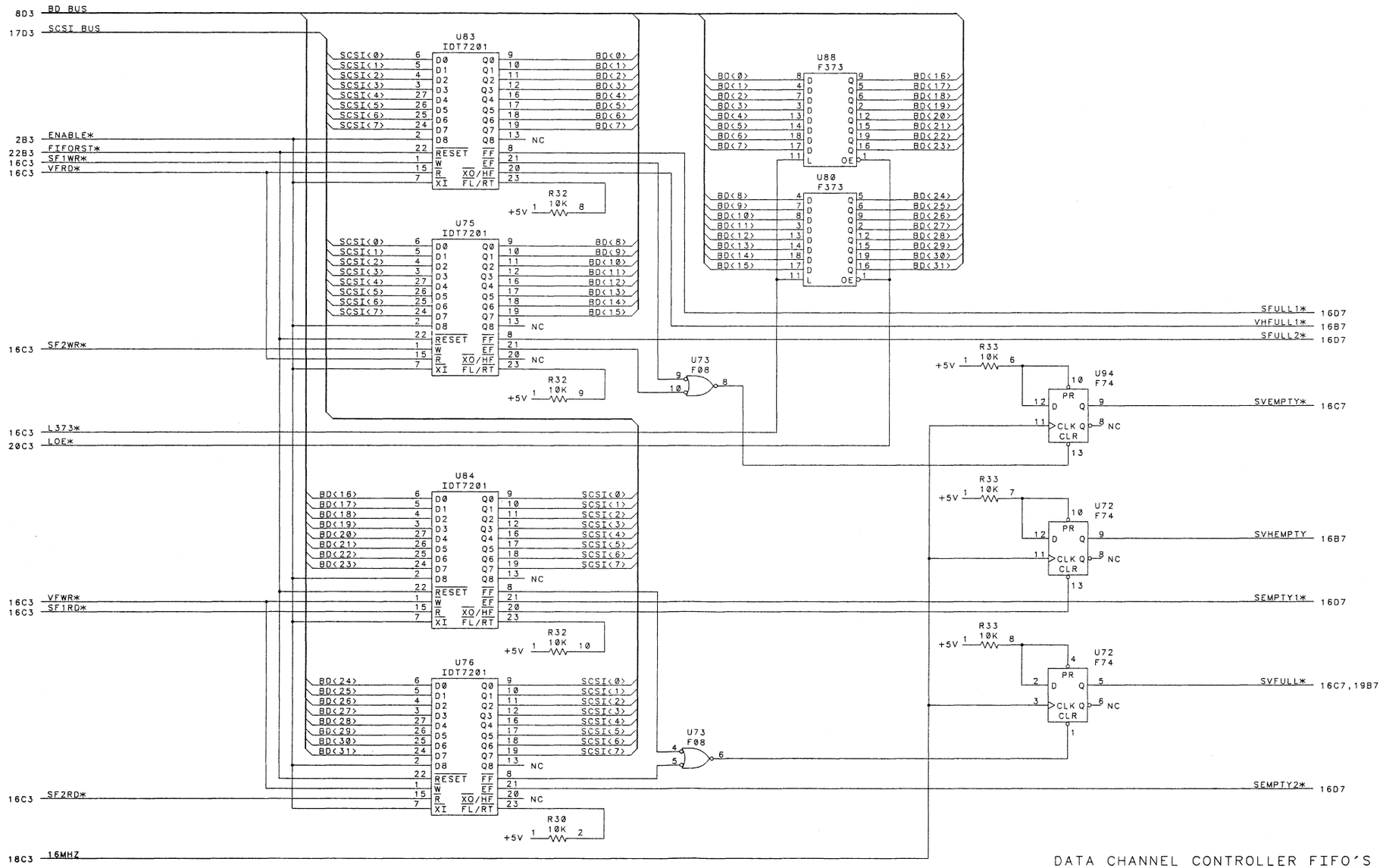


FIGURE 4-2. MVME327A Schematic Diagram 4-41/4-42

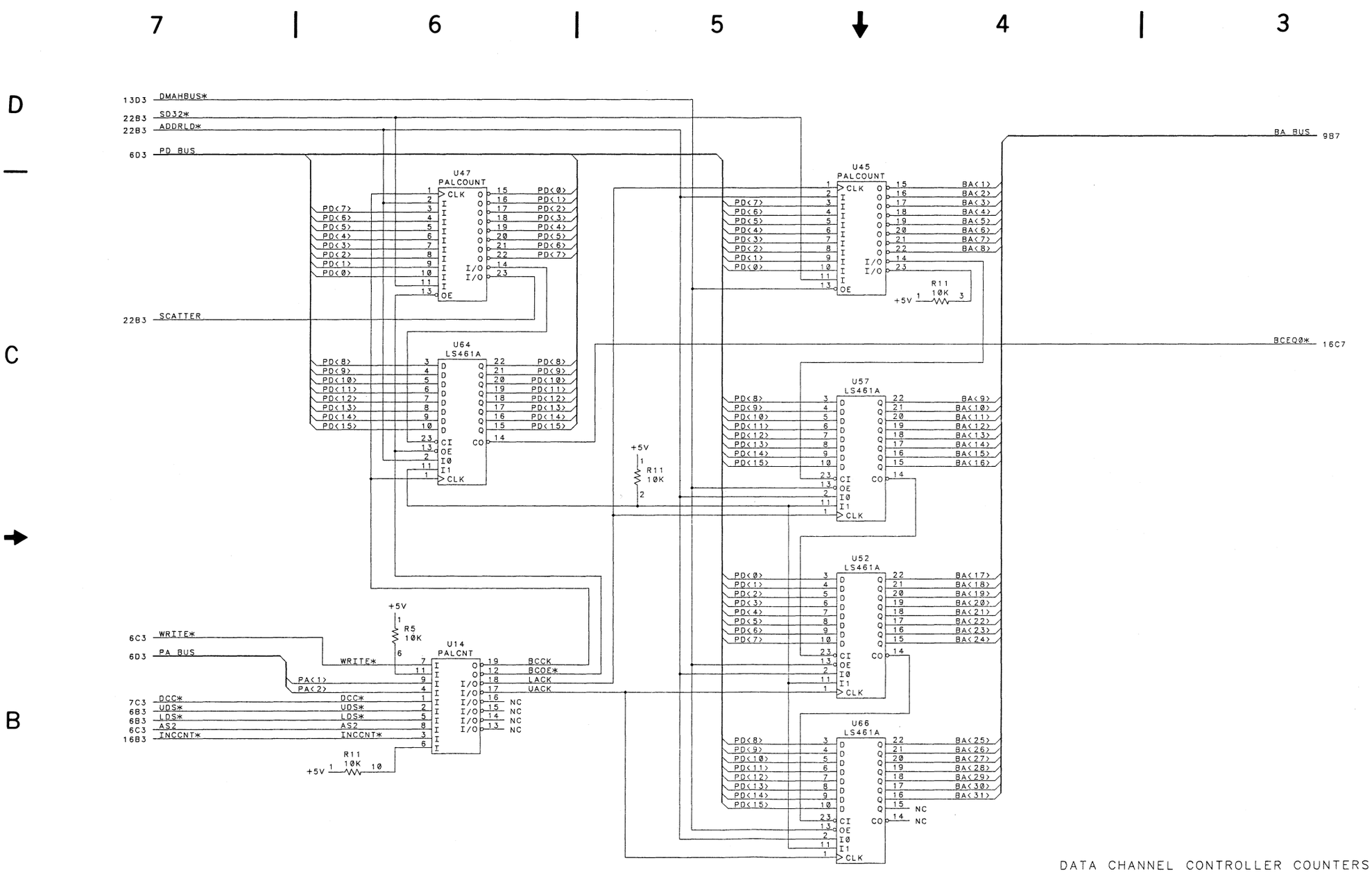


FIGURE 4-2. MVME327A Schematic Diagram 4-43/4-44

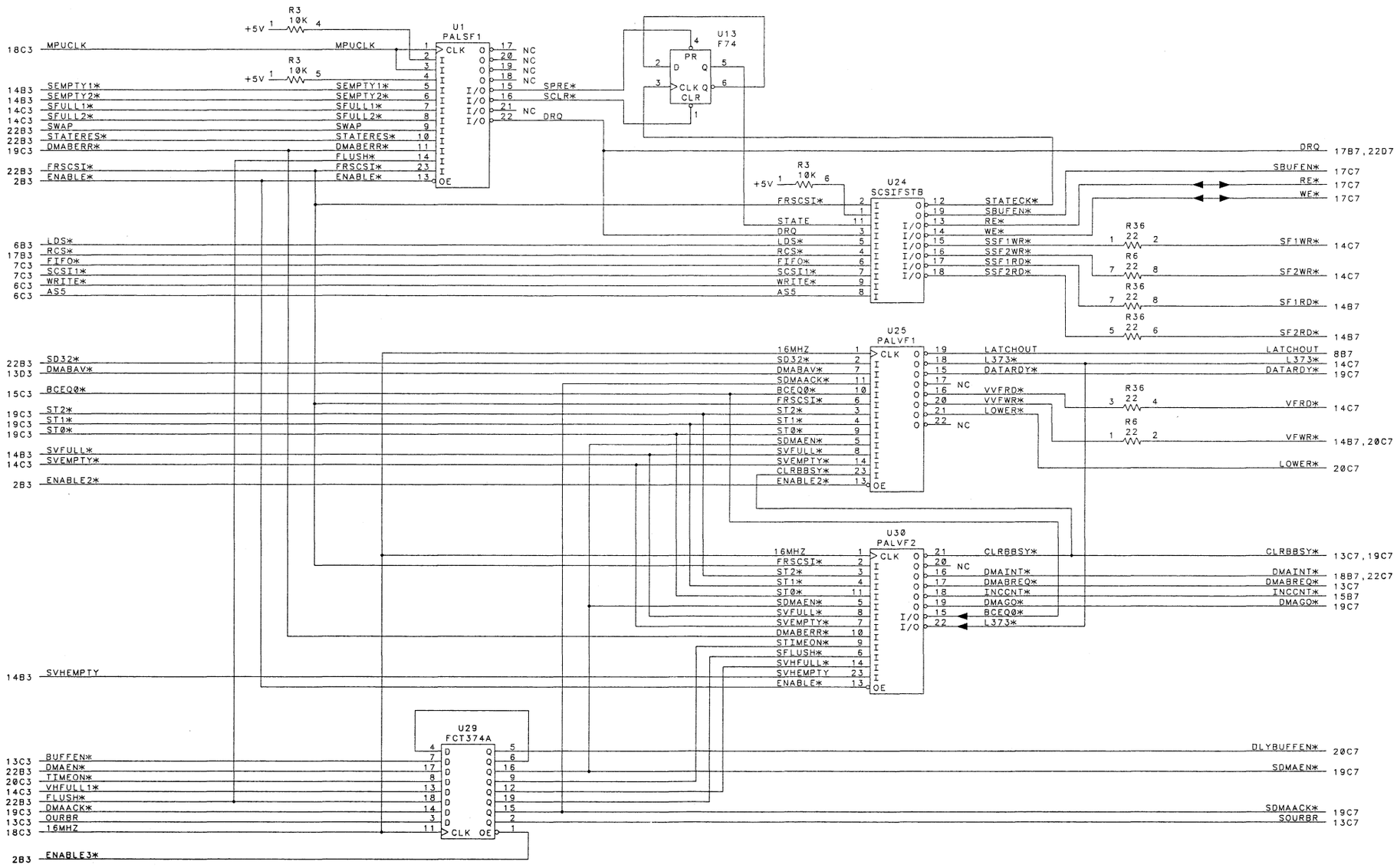
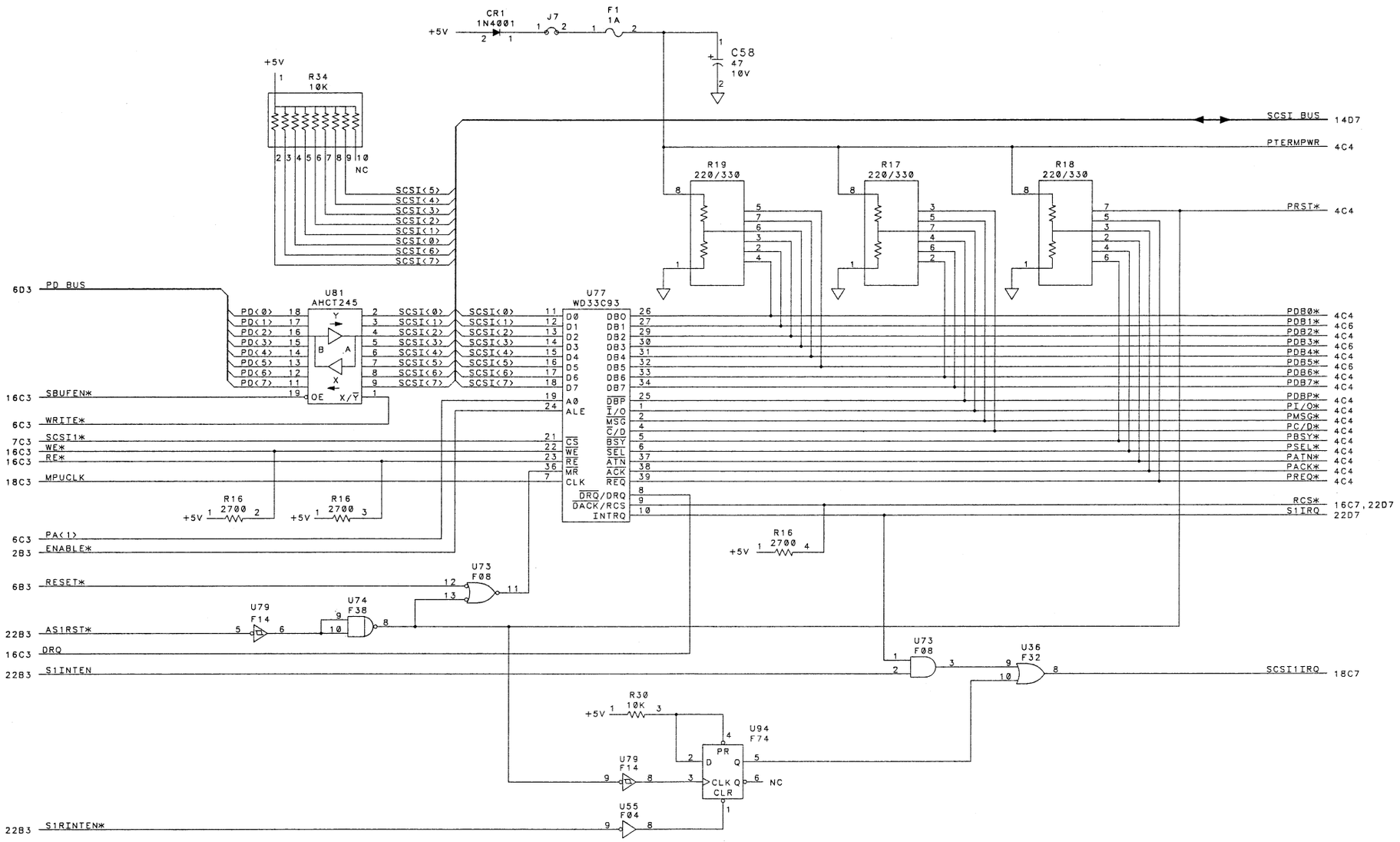
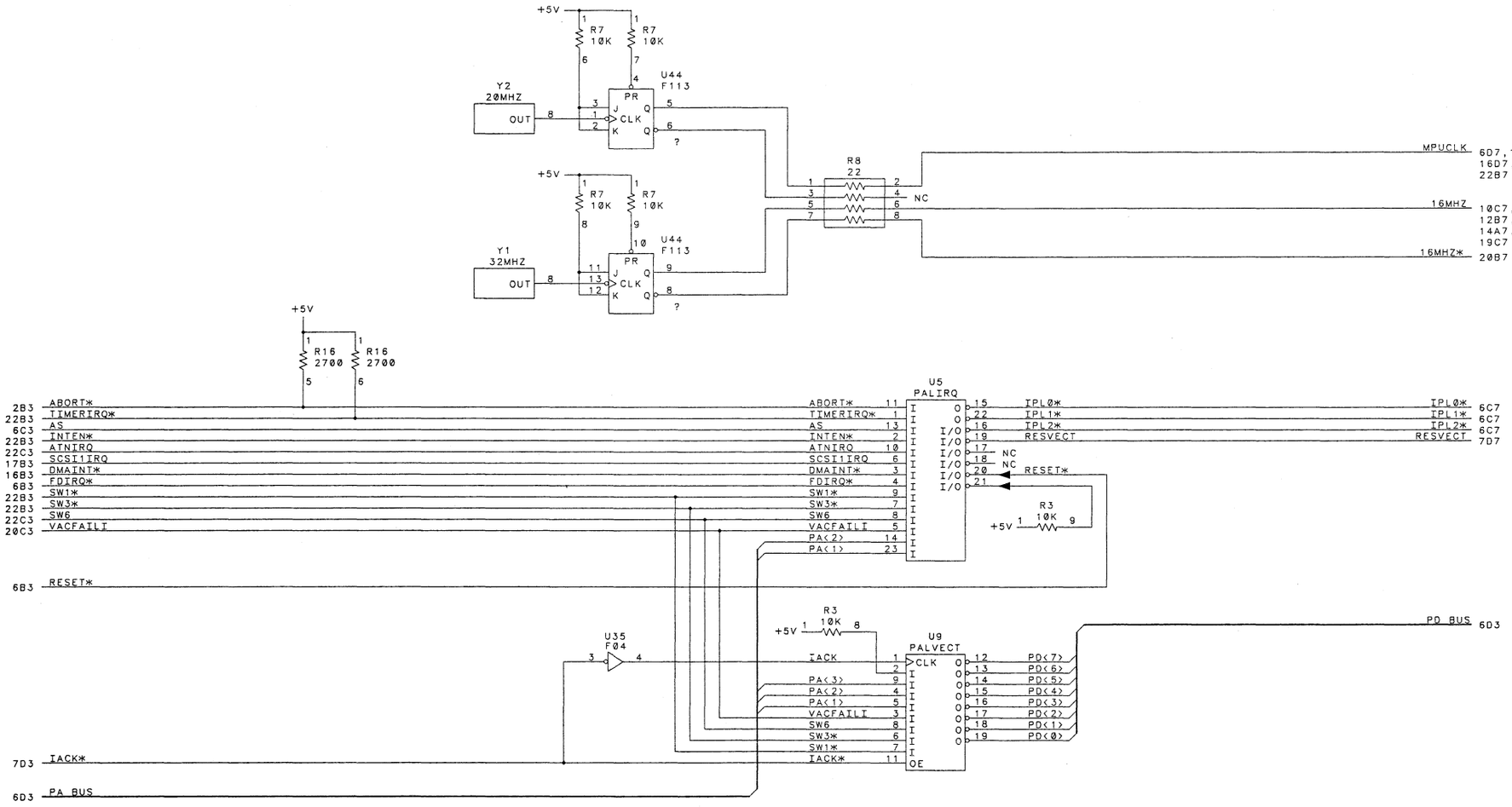


FIGURE 4-2. MVME327A Schematic Diagram



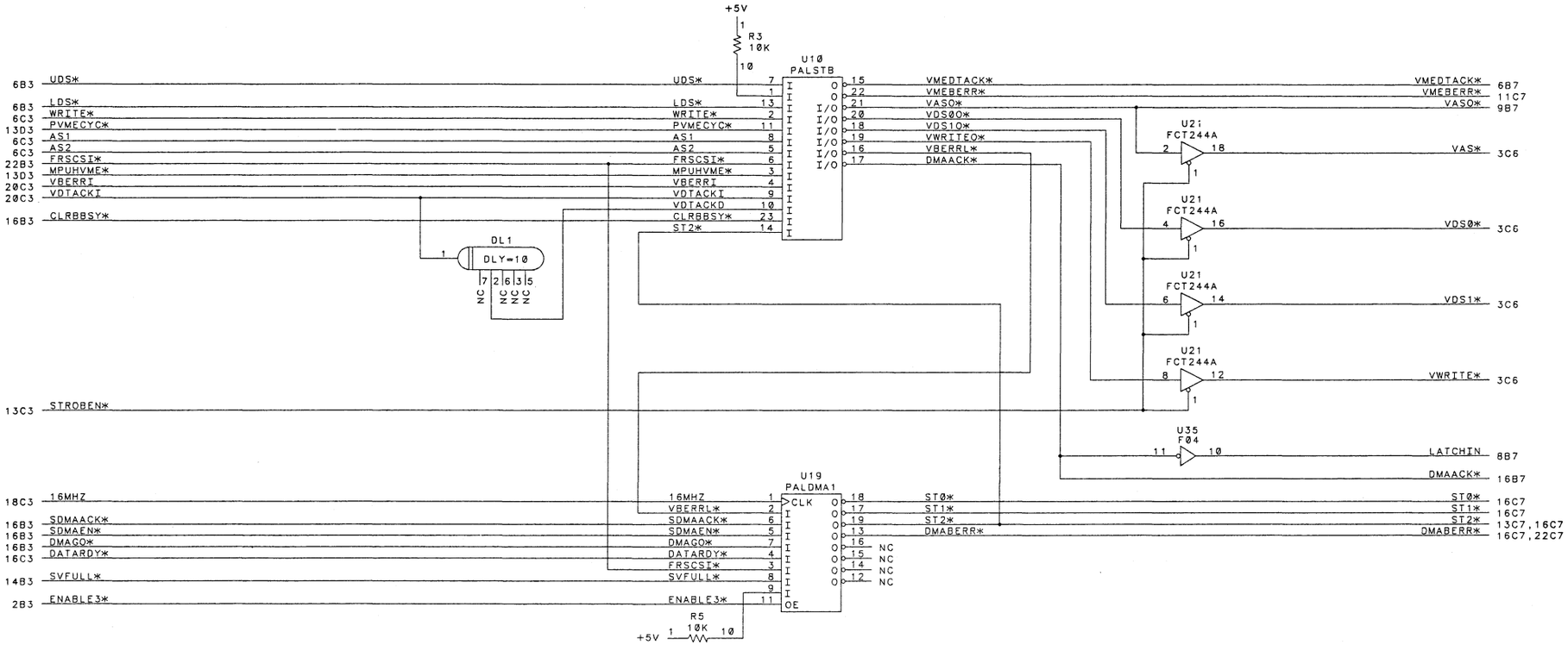
SCSI INTERFACE
63DW3550B0C REV C SH 17 OF 23

FIGURE 4-2. MVME327A Schematic Diagram



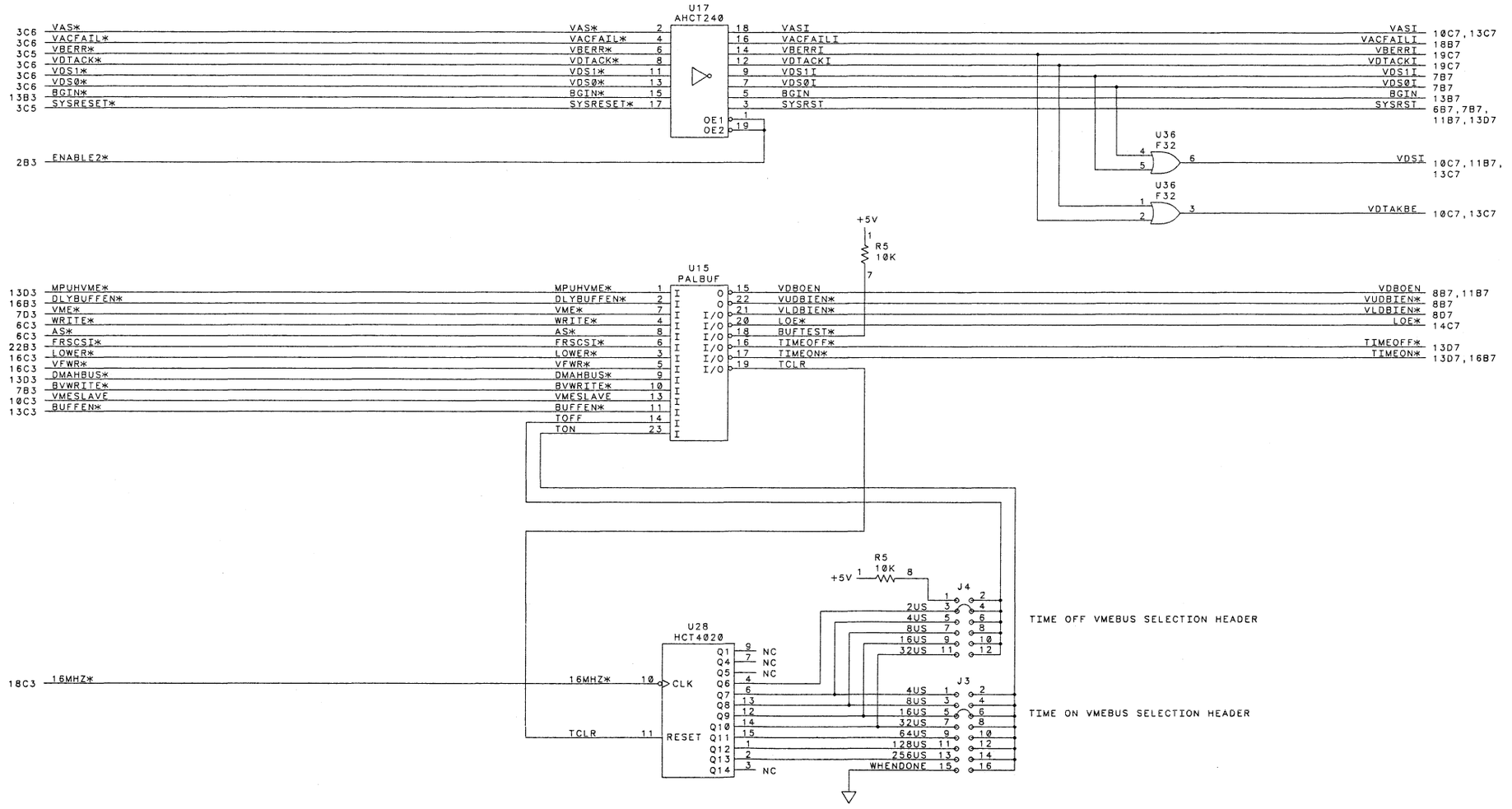
LOCAL INTERRUPT HANDLER
63DW3550B0C REV C SH 18 OF 23

FIGURE 4-2. MVME327A Schematic Diagram 4-49/4-50



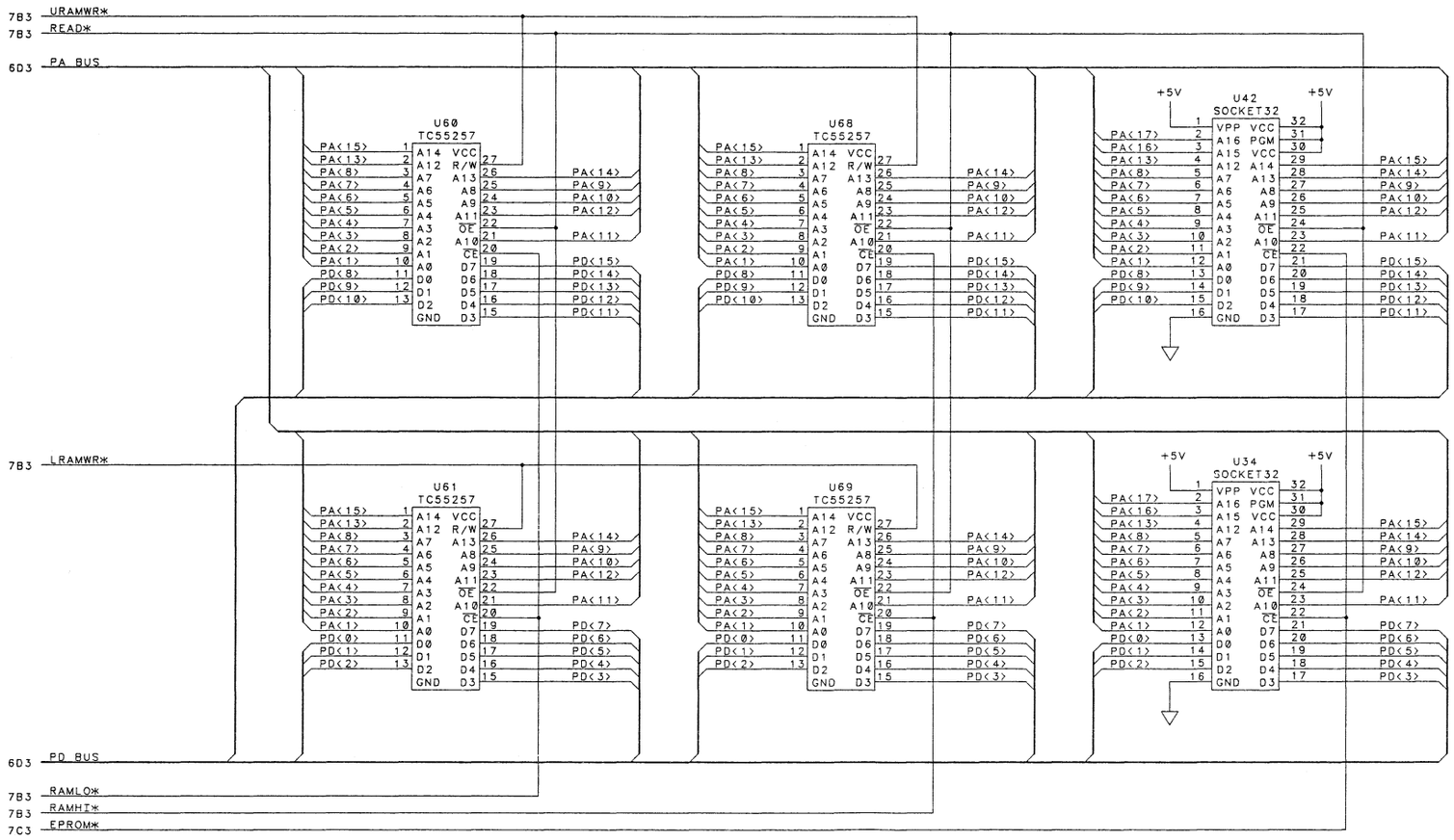
DMA CONTROLLER
63DW3550B0C REV C SH 19 OF 23

FIGURE 4-2. MVME327A Schematic Diagram



BUFFER AND TON/TOFF CONTROL
63DW3550B0C REV C SH 20 OF 23

FIGURE 4-2. MVME327A Schematic Diagram 4-53/4-54



LOCAL RAM AND EPROM
63DW3550B0C REV C SH 21 OF 23

FIGURE 4-2. MVME327A Schematic Diagram

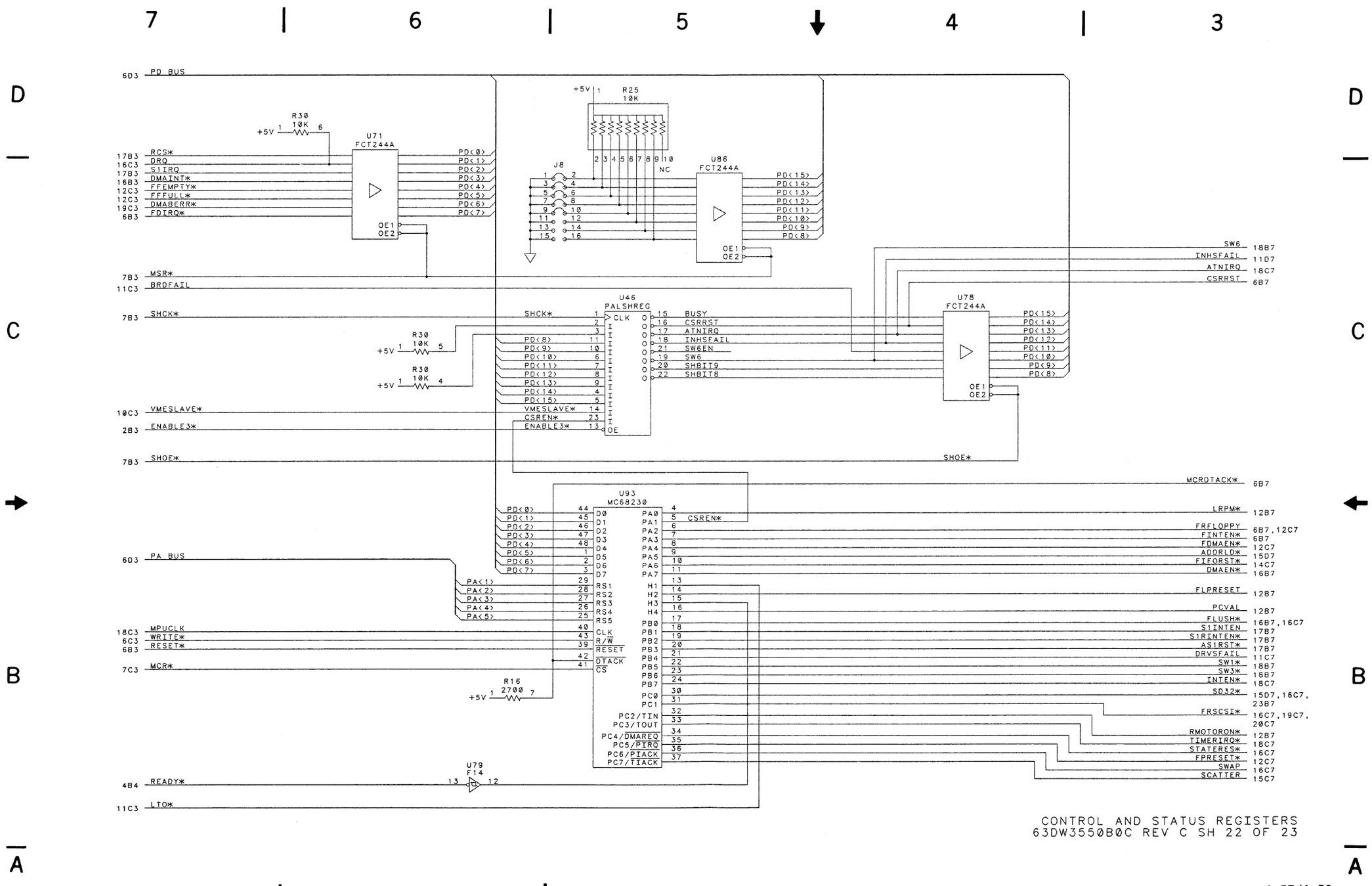
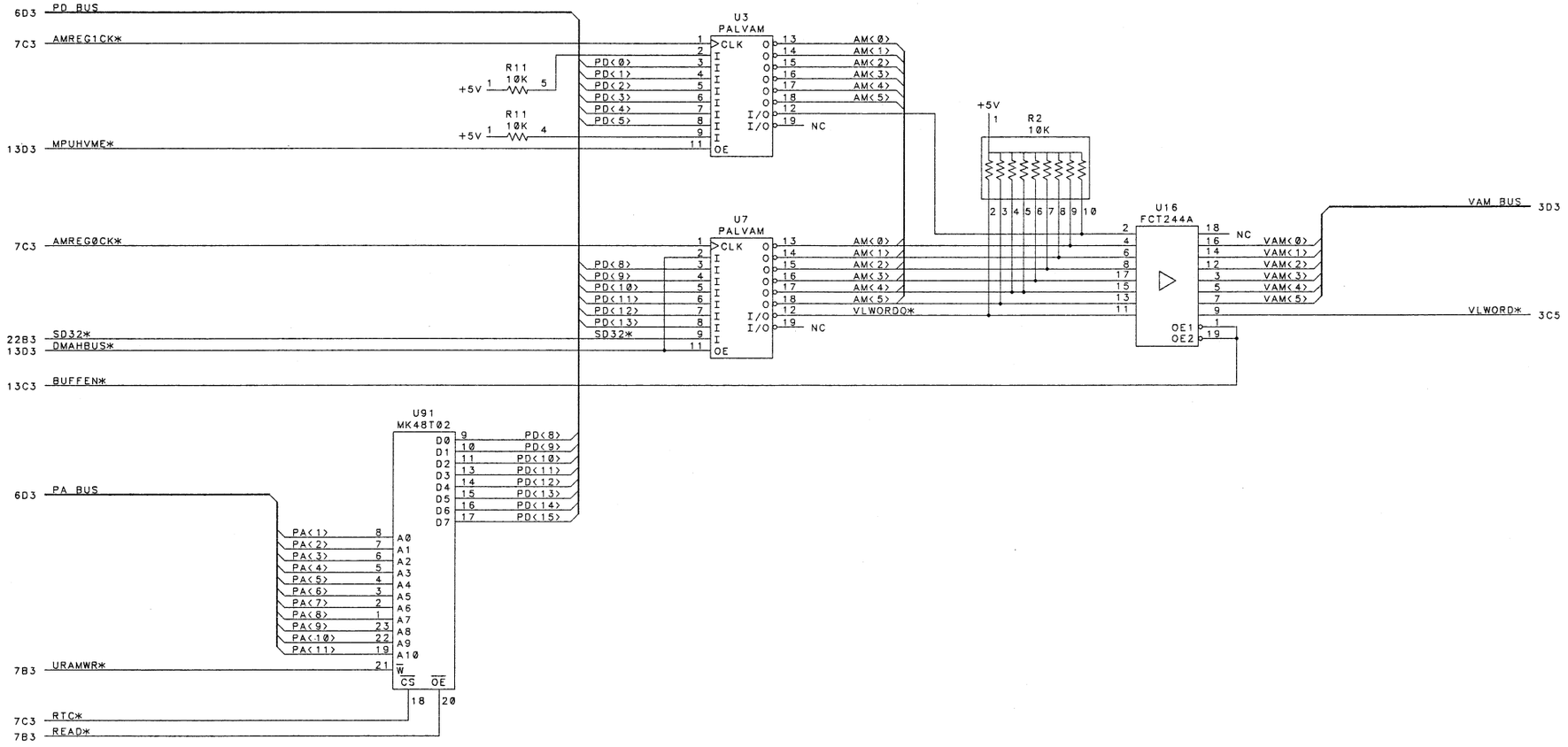


FIGURE 4-2. MVME327A Schematic Diagram



AM REGISTERS AND SRAM WITH TIMEKEEPER
63DW3550B0C REV C SH 23 OF 23

FIGURE 4-2. MVME327A Schematic Diagram

CHAPTER 5 - MVME327A P2 ADAPTER BOARD

5.1 INTRODUCTION

The P2 Adapter Board is used as the interface between the SCSI and floppy P2 connector on the MVME327A, the MVME717, and the peripheral devices. The P2 adapter board connects to the backplane P2 connector where the MVME327A is installed. A 50-pin connector is provided for SCSI signals. A 34-pin connector is provided for the floppy disk signals.

A user-supplied 50-conductor flat ribbon cable can be connected from the P2 adapter connector J1 to internal SCSI devices or to the MVME717.

A user-supplied 34-conductor flat ribbon cable can be connected from the P2 adapter connector J2 to an internal floppy disk drive.

The purpose of the P2 Adapter Board is to provide a true SCSI port as well as a floppy port internal to the chassis.

Connector locations are shown in Figure 5-1.

5.2 INTERCONNECT SIGNALS

The P2 Adapter Board connects directly to the MVME327A connector P2 through the chassis backplane. Connector J1 is the SCSI bus interface between the MVME327A, MVME717, and internal SCSI devices. Connector J2 is the floppy disk interface to internal floppy disk drives.

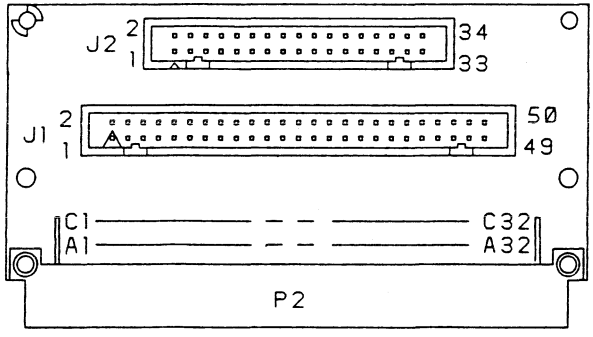


FIGURE 5-1. P2 Adapter Board Connector Locations

5.2.1 Connector P2 Interconnect Signals

Connector P2 is a standard DIN 41612 triple-row, 96-pin male connector. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 5-1.

TABLE 5-1. Connector P2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A3	DB1*,DB3* DB5*	DATA BUS (SCSI) (bits 1, 3, 5) - three of eight data bits on the SCSI bus.
A4-A32	GND	GROUND
B1-B32 except B2,B12, B22,B31		Not used.
	GND	GROUND
C1-C5	DB0*,DB2*, DB4*,DB6*, DB7*	DATA BUS (SCSI) (bits 0, 2, 4, 6, 7) - same as DB1, DB3, DB5 on P1 pin A1-A3. Bit seven is the most significant bit and the highest priority during the arbitration phase.
C6	DBP*	DATA BUS PARITY (SCSI) - data parity is odd. Use of parity is a system option. Parity is not valid during arbitration phase.
C7	TERMPWR	TERMINATOR POWER (SCSI)
C8	ATN*	ATTENTION (SCSI) - signal driven by the initiator. Indicates the attention condition.
C9	BSY*	BUS BUSY (SCSI) - signal that indicates that the bus is being used.
C10	ACK*	ACKNOWLEDGE (SCSI) - signal driven by an initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.
C11	RST*	RESET (SCSI) - signal that indicates the RESET condition.
C12	MSG*	MESSAGE (SCSI) - signal driven by the target during the message phases.
C13	SEL*	SELECT (SCSI) - signal used by the initiator to select a target or by a target to reselect an initiator.

TABLE 5-1. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C14	C/D*	CONTROL/DATA (SCSI) - signal driven by the target. It indicates whether control or data information is on the data bus.
C15	REQ*	REQUEST (SCSI) - signal driven by the target to indicate a request for a REQ/ACK data transfer handshake.
C16	I/O*	INPUT/OUTPUT (SCSI) - signal driven by a target which controls the direction of data movement on the SCSI bus. This signal is also used to distinguish between selection and reselection phases.
C17	RPM*	DENSITY (FLOPPY) - allows control of motor speed/density on dual speed/density drives.
C18	SELECT4*	DRIVE SELECT 4 (FLOPPY) - this signal, when low, connects the drive 4 I/O interface to the control lines.
C19	INDEX*	INDEX (FLOPPY) - this signal is driven by the drive once each revolution to indicate the beginning of a track. This line is valid on the high to low transition.
C20	SELECT1*	DRIVE SELECT 1 (FLOPPY) - this signal, when low, connects the drive 1 I/O interface to the control lines.
C21	SELECT2*	DRIVE SELECT 2 (FLOPPY) - this signal, when low, connects the drive 2 I/O interface to the control lines.
C22	SELECT3*	DRIVE SELECT 3 (FLOPPY) - this signal, when low, connects the drive 3 I/O interface to the control lines.
C23	MOTORON*	MOTOR ON (FLOPPY) - when this signal is low, the motor(s) in the 5-1/4 inch floppy drives are energized and start accelerating to operating speed.

TABLE 5-1. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C24	DIRECTION*	DIRECTION (FLOPPY) - this signal defines the direction of motion of the read/write heads when the STEP line (pin C25) is pulsed. A high level when the STEP line is pulsed causes the read/write heads to move out away from the center of the disk. A low level when the STEP line is pulsed causes the read/write heads to move in towards the center of the disk.
C25	STEP*	HEAD STEP (FLOPPY) - this signal causes the read/write heads to move in the direction defined by the DIRECTION signal (pin C24).
C26	WRITE DATA*	WRITE DATA (FLOPPY) - this line carries the encoded write data to be recorded on the diskette.
C27	WRITE GATE*	WRITE GATE (FLOPPY) - this signal controls the read/write mode of the selected drive. The write circuitry is enabled when WRITE GATE is low, provided the diskette is not write protected.
C28	TRACK 00*	TRACK ZERO (FLOPPY) - this signal indicates the read/write heads are positioned at cylinder zero (the outermost data track).
C29	WRITE PROTECT*	WRITE PROTECT (FLOPPY) - this signal indicates the diskette in the drive is write-protected.
C30	READ DATA*	READ DATA (FLOPPY) - this line carries composite serial data from the selected diskette to the controller.
C31	SIDE SELECT*	SIDE SELECT (FLOPPY) - this signal indicates when read/write head is used on the selected drive. When this signal is high, head 0 is selected. When this signal is low, head 1 is selected.
C32	READY*	READY (FLOPPY) - this line is driven by the floppy drive when it is ready.

5.2.2 Connectors J1 Interconnect Signals (SCSI)

Each pin connection, signal mnemonic, and signal characteristic for the connectors are listed in Table 5-2.

TABLE 5-2. Connectors J1 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1-19 (ODD)	GND	GROUND
2-16 (EVEN)	DB0*-DB7*	DATA BUS (SCSI) (bits 0-7) - the eight data bits on the SCSI bus.
18	DBP*	DATA BUS PARITY (SCSI) - data parity is odd. Use of parity is a system option. Parity is not valid during arbitration phase.
20-24	GND	GROUND
25		Not used.
26	TERMPWR	TERMINATOR POWER (SCSI)
27-31	GND	GROUND
32	ATN*	ATTENTION (SCSI) - signal driven by the initiator. Indicates the attention condition.
33-35	GND	GROUND
36	BSY*	BUS BUSY (SCSI) - signal that indicates that the bus is being used.
37-49 (ODD)	GND	GROUND
38	ACK*	ACKNOWLEDGE (SCSI) - signal driven by an initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.
40	RST*	RESET (SCSI) - signal that indicates the RESET condition.
42	MSG*	MESSAGE (SCSI) - signal driven by the target during the message phase.
44	SEL*	SELECT (SCSI) - signal used by the initiator to select a target or by a target to reselect an initiator.

TABLE 5-2. Connector J1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
46	C/D*	CONTROL/DATA (SCSI) - signal driven by the target. It indicates whether control or data information is on the data bus.
48	REQ*	REQUEST (SCSI) - signal driven by the target to indicate a request for a REQ/ACK data transfer handshake.
50	I/O*	INPUT/OUTPUT (SCSI) - signal driven by a target which controls the direction of data movement on the SCSI bus. This signal is also used to distinguish between selection and reselection phases.

5.2.3 Connector J2 Interconnect Signals

Connector J2 interconnects with the floppy drives in the user system. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 5-3.

TABLE 5-3. Connector J2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1-33 (ODD)	GND	GROUND
2	RPM*	DENSITY (FLOPPY) - allows optional control of motor speed/density on dual speed/density drives. 0 = high density. 1= normal density.
4		Not used.
6	SELECT4*	DRIVE SELECT 4 (FLOPPY) - this signal, when low, connects the drive 4 I/O interface to the control lines.
8	INDEX*	INDEX (FLOPPY) - this signal is driven by the drive once each revolution to indicate the beginning of a track. This line is valid on the high to low transition.

TABLE 5-3. Connector J2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
10	SELECT1*	DRIVE SELECT 1 (FLOPPY) - this signal, when low, connects the drive 1 I/O interface to the control lines.
12	SELECT2*	DRIVE SELECT 2 (FLOPPY) - this signal, when low, connects the drive 2 I/O interface to the control lines.
14	SELECT3*	DRIVE SELECT 3 (FLOPPY) - this signal, when low, connects the drive 3 I/O interface to the control lines.
16	MOTORON*	MOTOR ON (FLOPPY) - when this signal is low, the motor(s) in the 5-1/4 inch floppy drives are energized and start accelerating to operating speed.
18	DIRECTION*	DIRECTION (FLOPPY) - this signal defines the direction of motion of the read/write heads when the STEP line (pin 20) is pulsed. A high level when the STEP line is pulsed causes the read/write heads to move out away from the center of the disk. A low level when the STEP line is pulsed causes the read/write heads to move in towards the center of the disk.
20	STEP*	HEAD STEP (FLOPPY) - this signal causes the read/write heads to move in the direction defined by the DIRECTION signal (pin 18).
22	WRT DATA*	WRITE DATA (FLOPPY) - this line carries the encoded write data to be recorded on the diskette.
24	WRT GATE*	WRITE GATE (FLOPPY) - this signal controls the read/write mode of the selected drive. The write circuitry is enabled when WRITE GATE is low, provided the diskette is not write protected.
26	TRACK 00*	TRACK ZERO (FLOPPY) - this signal indicates the read/write heads are positioned at cylinder zero (the outermost data track).
28	WRT PRTCT*	WRITE PROTECT (FLOPPY) - this signal indicates the diskette in the drive is write-protected.

TABLE 5-3. Connector J2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
30	READ DATA*	READ DATA (FLOPPY) - this line carries composite serial data from the selected diskette to the controller.
32	SD SELECT*	SIDE SELECT (FLOPPY) - this signal indicates when read/write head is used on the selected drive. When this signal is high, head 0 is selected. When this signal is low, head 1 is selected.
34	READY*	READY (FLOPPY) - this line is driven by the floppy drive when it is ready.

5.3 INSTALLATION INSTRUCTIONS

To install the P2 Adapter Board in the system, proceed as follows:

a. Turn all equipment power OFF and disconnect power cable from ac power source.

CAUTION

CONNECTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS EQUIPMENT. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

b. Remove chassis cover as instructed in the equipment user's manual.

If SCSI devices are to be attached internal to the user system, proceed as follows and see Figure 5-2. (For external device attachment refer to Chapter 6.)

a. If the MVME327A is at one end of the cable, terminators must be installed on the MVME327A. If the MVME327A is in the middle of the cable, terminators must be removed from the MVME327A.

b. Install the P2 adapter board to the backplane directly in line with the P2 connector on the MVME327A. Be sure to orient pin 1 of the adapter with pin 1 of the backplane connector.

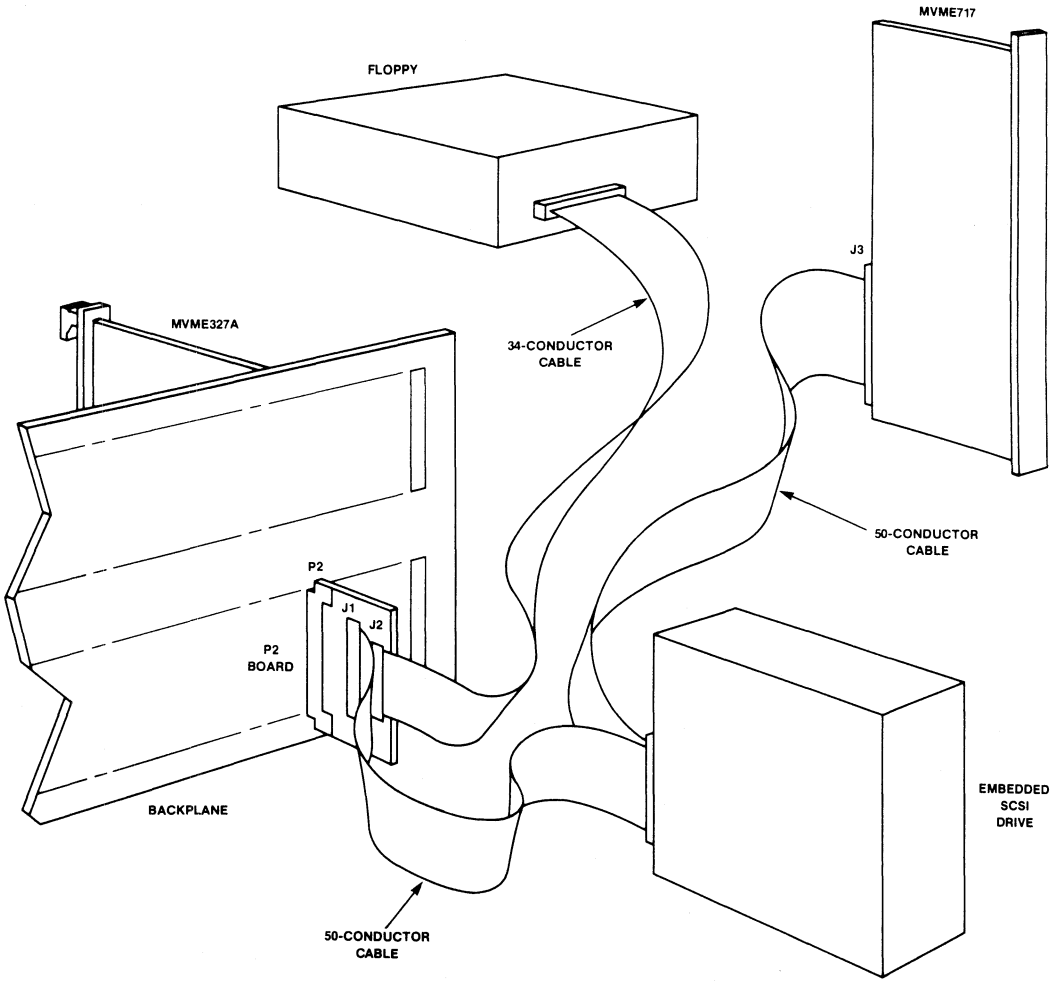


FIGURE 5-2. P2 Adapter Board Connections

c. Connect a user-supplied flat ribbon cable with compatible pinouts from connector J1 on the P2 adapter to the internal SCSI devices. Make sure the cable is terminated only at each end.

d. Make sure that cables will not be pinched by the cover and install cover previously removed.

e. Connect the power cable to the ac power source and turn the unit on.

To connect the P2 Adapter Board to floppy drives internal to the user system, proceed as follows:

a. Install the P2 adapter board to the backplane directly in line with the P2 connector on the MVME327A. Be sure to orient pin 1 of the adapter with pin 1 of the backplane connector.

5

b. Connect a user-supplied cable with compatible pinouts from connector J2 on the P2 adapter to the internal floppy drive.

c. Make sure that cables will not be pinched by the cover and install cover previously removed.

d. Connect the power cable to the ac power source and turn the unit on.

5.4 PARTS LIST

The components of the P2 Adapter Board are listed in Table 5-4. The parts locations are shown in Figure 5-3. These parts reflect the latest issue of hardware at the time of printing.

TABLE 5-4. P2 Adapter Board Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8544B01B	Printed wiring board
J1	28NW9802F67	Connector, 50-pin, MMM 3596-6002
J2	28NW9802F66	Connector, 34-pin, MMM 3594-6002
P1	28NW9802E71	Connector, 96-pin

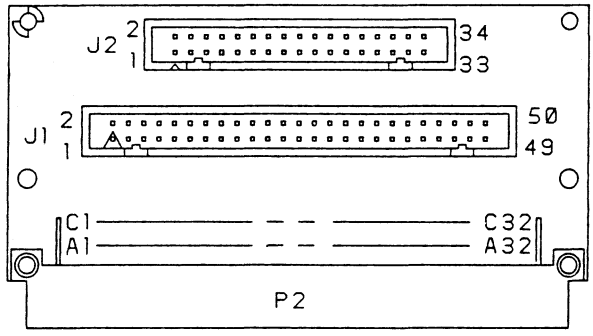
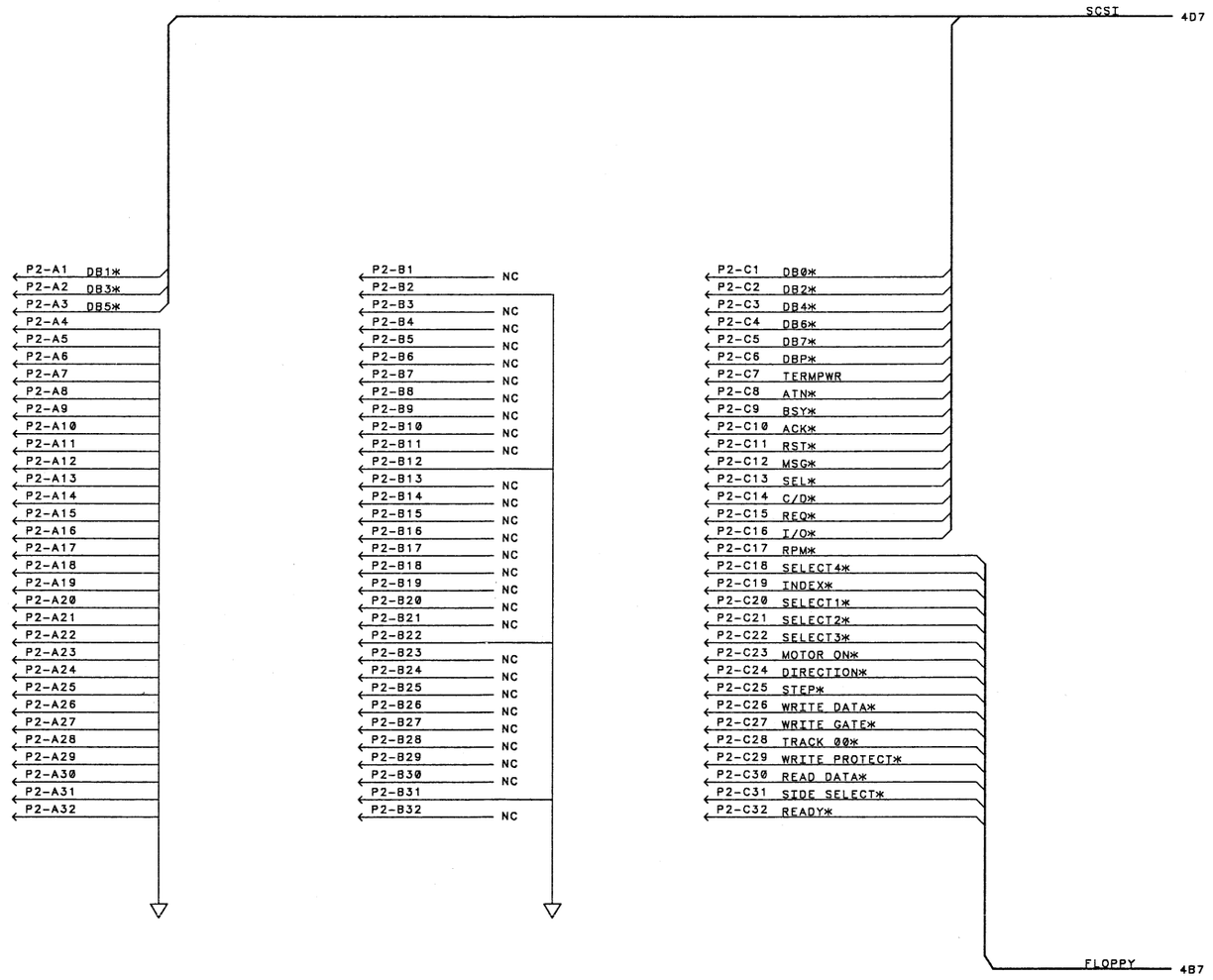


FIGURE 5-3. P2 Adapter Board Parts Location

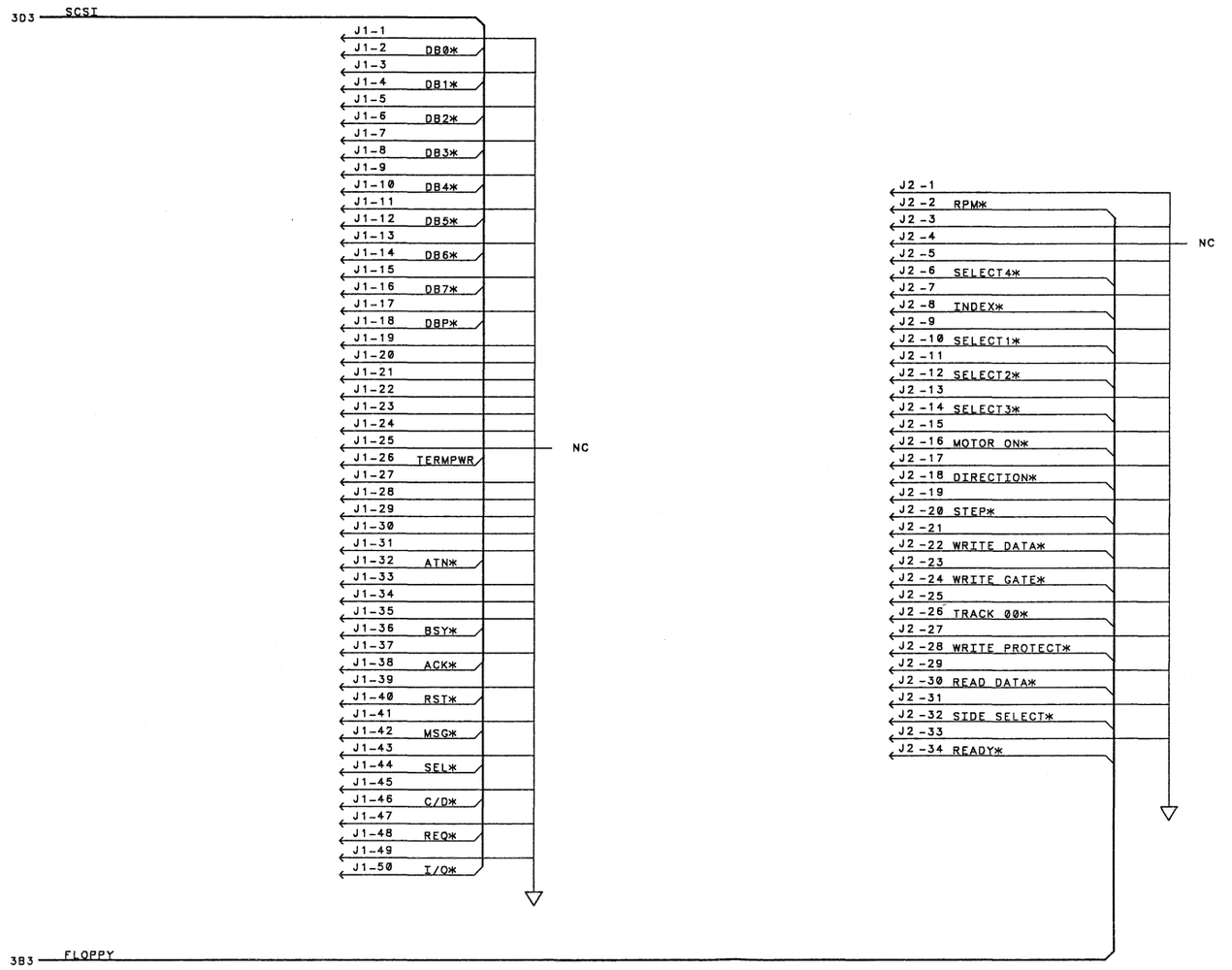
5.5 SCHEMATIC DIAGRAM

The P2 Adapter Board schematic diagram is illustrated in Figure 5-4.



63DW3544B0B REV A

FIGURE 5-4. P2 Adapter Schematic Diagram



63DW3544B0B REV A

FIGURE 5-4. P2 Adapter Schematic Diagram

CHAPTER 6 - MVME717 TRANSITION MODULE

6.1 INTRODUCTION

The MVME717 is used to connect a 50-conductor flat ribbon SCSI cable from the P2 Adapter Board to a shielded connector (SCSI alternative 2 single-ended) at the MVME717 front panel. This is useful to a user that needs to connect SCSI devices with flat ribbon cable on the inside of a chassis and also SCSI devices using a shielded cable outside of a chassis.

Because the MVME717 provides sockets (and terminators) for SCSI, the module can easily be configured for either the end of the SCSI cable or for a connection from inside a chassis to the outside.

A TERM PWR green LED on the front panel indicates SCSI terminator power.

The purpose of the MVME717 is to convert the SCSI single-ended non-shielded pinout to the SCSI single-ended shielded alternative 2 pinout.

Terminator and connector locations are shown in Figure 6-1.

6.2 TERMINATORS

Two SCSI terminator sockets (R1,R2) are provided. Terminating resistors are installed by the factory. Terminators must be installed on the end device or module. Make sure terminators are installed only at each end of the SCSI cable.

6.3 INTERCONNECT SIGNALS

The MVME717 connector J3 connects through a flat ribbon cable to the MVME327A P2 Adapter Board connector J1. Connector J1 on the MVME717 is the front panel connector SCSI INTERFACE.

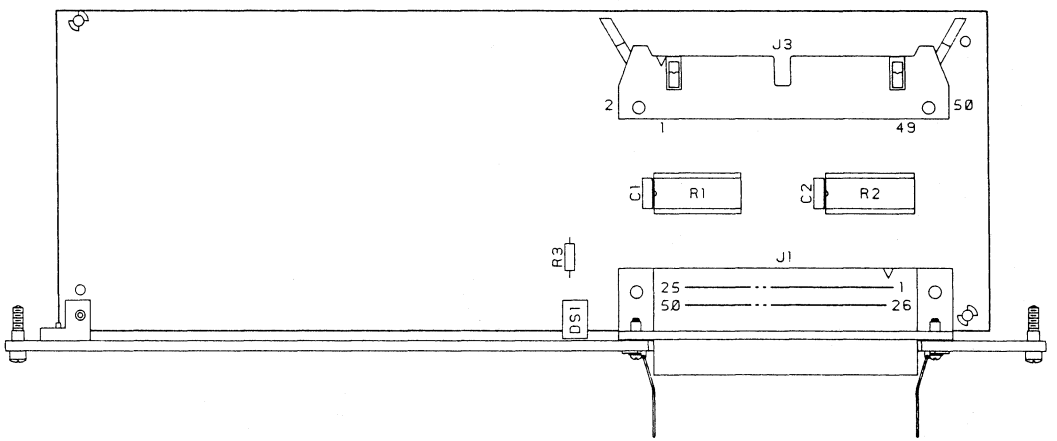


FIGURE 6-1. MVME717 Connector Locations

6.3.1 Connector J1 Interconnect Signals (SCSI INTERFACE)

Each pin connection, signal mnemonic, and signal characteristic for the connectors are listed in Table 6-2.

TABLE 6-1. Connector J1 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1-25	PGND	GROUND
13		Not used.
26-33	PDB0*-PDB7*	DATA BUS (SCSI) (bits 0-7) - the eight data bits on the SCSI bus.
34	PDBP*	DATA BUS PARITY (SCSI) - data parity is odd. Use of parity is a system option. Parity is not valid during arbitration phase.
35-37	PGND	GROUND
38	PTERMPWR	TERMINATOR POWER (SCSI)
39,40	PGND	GROUND
41	PATN*	ATTENTION (SCSI) - signal driven by the initiator. Indicates the attention condition.
42	PGND	GROUND
43	PBSY*	BUS BUSY (SCSI) - signal that indicates that the bus is being used.
44	PACK*	ACKNOWLEDGE (SCSI) - signal driven by an initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.
45	PRST*	RESET (SCSI) - signal that indicates the RESET condition.
46	PMSG*	MESSAGE (SCSI) - signal driven by the target during the message phase.
47	PSEL*	SELECT (SCSI) - signal used by the initiator to select a target or by a target to reselect an initiator.
48	PC/D*	CONTROL/DATA (SCSI) - signal driven by the target. It indicates whether control or data information is on the data bus.

TABLE 6-1. Connector J1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
49	PREQ*	REQUEST (SCSI) - signal driven by the target to indicate a request for a REQ/ACK data transfer handshake.
50	PI/O*	INPUT/OUTPUT (SCSI) - signal driven by a target which controls the direction of data movement on the SCSI bus. This signal is also used to distinguish between selection and reselection phases.

6.3.2 Connector J3 Interconnect Signals

Connector J3 interconnects through cable with connector J1 on the P2 Adapter Board. Each pin connection, signal mnemonic, and signal characteristic for the connector is listed in Table 6-2.

TABLE 6-2. Connector J3 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1-19 (ODD)	GND	GROUND
2-16 (EVEN)	DB0*-DB7*	DATA BUS (SCSI) (bits 0-7) - the eight data bits on the SCSI bus.
18	DBP*	DATA BUS PARITY (SCSI) - data parity is odd. Use of parity is a system option. Parity is not valid during arbitration phase.
20-24	GND	GROUND
25		Not used.
26	TERMPWR	TERMINATOR POWER (SCSI)
27-31	GND	GROUND
32	ATN*	ATTENTION (SCSI) - signal driven by the initiator. Indicates the attention condition.

TABLE 6-2. Connector J3 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
33-35	GND	GROUND
36	BSY*	BUS BUSY (SCSI) - signal that indicates that the bus is being used.
37-49 (ODD)	GND	GROUND
38	ACK*	ACKNOWLEDGE (SCSI) - signal driven by an initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.
40	RST*	RESET (SCSI) - signal that indicates the RESET condition.
42	MSG*	MESSAGE (SCSI) - signal driven by the target during the message phase.
44	SEL*	SELECT (SCSI) - signal used by the initiator to select a target or by a target to reselect an initiator.
46	C/D*	CONTROL/DATA (SCSI) - signal driven by the target. It indicates whether control or data information is on the data bus.
48	REQ*	REQUEST (SCSI) - signal driven by the target to indicate a request for a REQ/ACK data transfer handshake.
50	I/O*	INPUT/OUTPUT (SCSI) - signal driven by a target which controls the direction of data movement on the SCSI bus. This signal is also used to distinguish between selection and reselection phases.

6.4 INSTALLATION INSTRUCTIONS

The MVME717 can be connected as shown in Figure 6-2. To install the MVME717 in the system, proceed as follows:

a. Turn all equipment power OFF and disconnect power cable from ac power source.

CAUTION

CONNECTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS EQUIPMENT. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

b. Remove chassis cover as instructed in the equipment user's manual.

c. Remove the filler panel(s) from the appropriate card slot(s) at the rear of the chassis (if the chassis has a rear card cage).

d. Connect the cable supplied with the module or a user-supplied cable with compatible pinouts from connector J3 on the MVME717 to the P2 adapter board connector J1 and internal SCSI devices. For internal device connections and P2 adapter board installation refer to Chapter 5.

e. If a cable is being attached to the shielded connector J1 on the front panel to be used external to the system, remove the terminators on the MVME717.

f. If the MVME717 is the end of the cable, the terminators must be installed on the MVME717.

g. Insert the MVME717 module into the selected slot and tighten the attaching screws.

h. Make sure that cables will not be pinched by the cover and install cover previously removed.

i. Connect a user-supplied cable with compatible pinouts from connector J1 SCSI INTERFACE on the MVME717 front panel to the external SCSI device. The last device on the cable should terminate the bus.

j. Connect the power cable to the ac power source and turn the unit on.

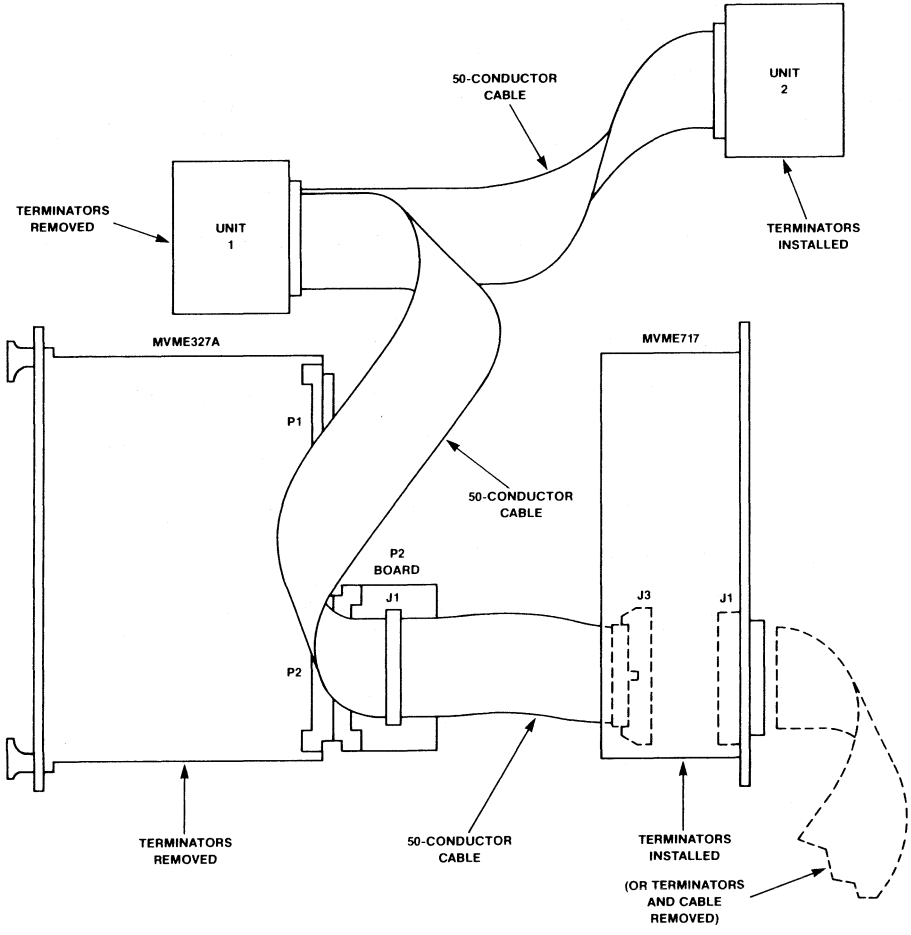


FIGURE 6-2. SCSI Connections

6.5 PARTS LIST

The components of the MVME717 are listed in Table 6-3. The parts locations are shown in Figure 6-3. These parts reflect the latest issue of hardware at the time of printing.

TABLE 6-3. MVME717 Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8543B01A	Printed wiring board
C1,C2	21NW9632A03	Capacitor, fixed, ceramic, 0.1 uF @ 50 Vdc
DS1	48NW9612A59	LED, green
J1	28NW9802H01	Connector, 50-pin, AMP 553813-3
J3	28NW9802D76	Connector, 50-pin, MMM 3433-1302
R1,R2	51NW9626A20	Resistor network, 14/220/330 (terminator)
R3	06SW-124A27	Resistor, fixed, film, 120 ohm, 5%, 1/4 W
	64-W5789B01A	Front panel
	09NW9811A86	Socket, DIL, 16-pin (use at R1,R2)

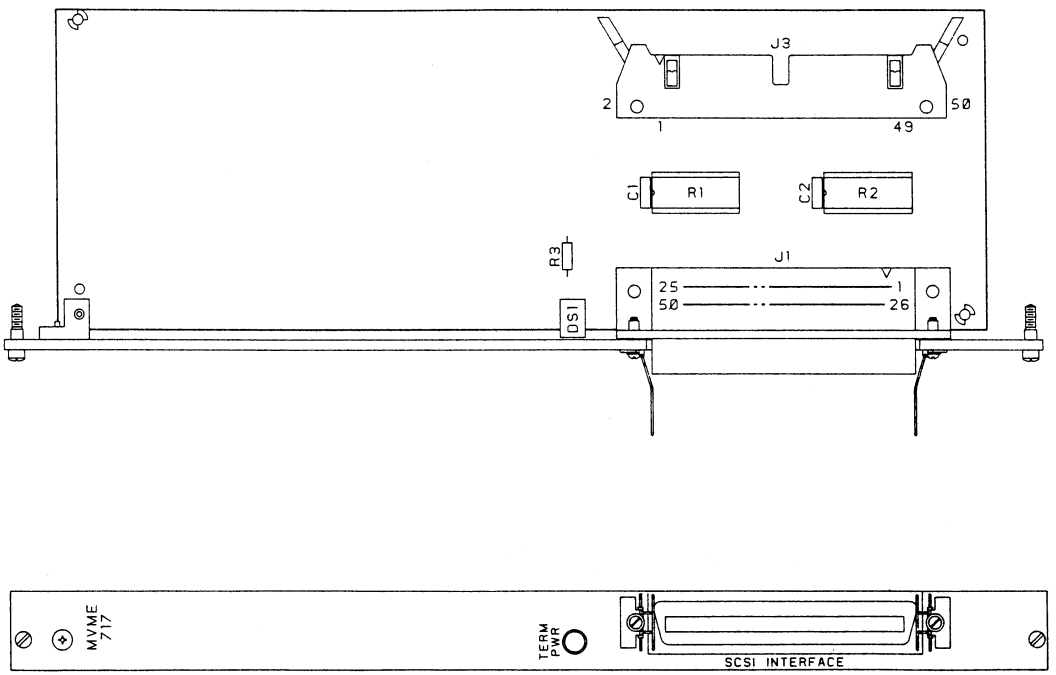


FIGURE 6-3. MVME717 Parts Location

6.6 SCHEMATIC DIAGRAM

The MVME717 schematic diagram is illustrated in Figure 6-4.

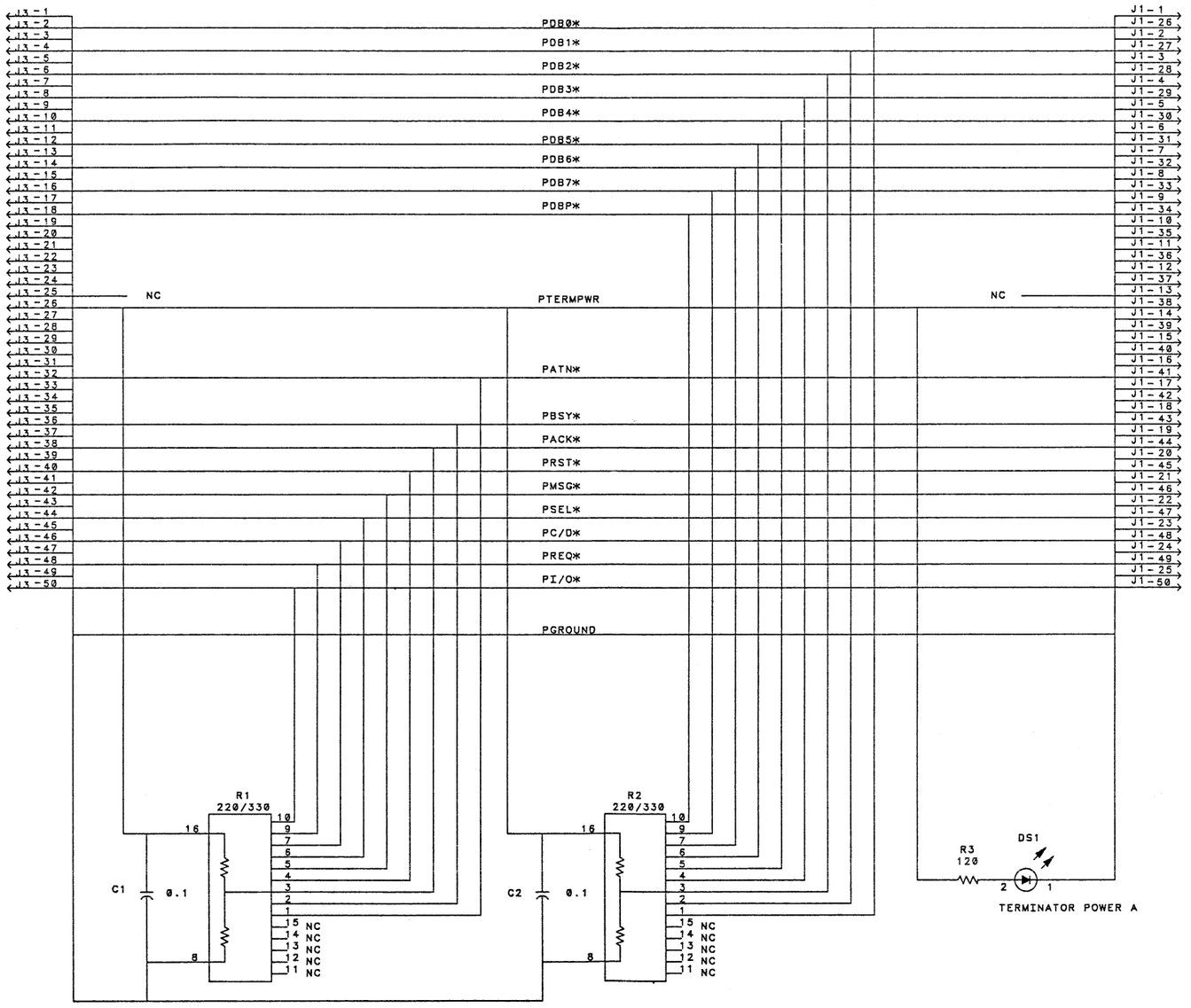


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FIGURE 6-4. MVME717 Schematic Diagram

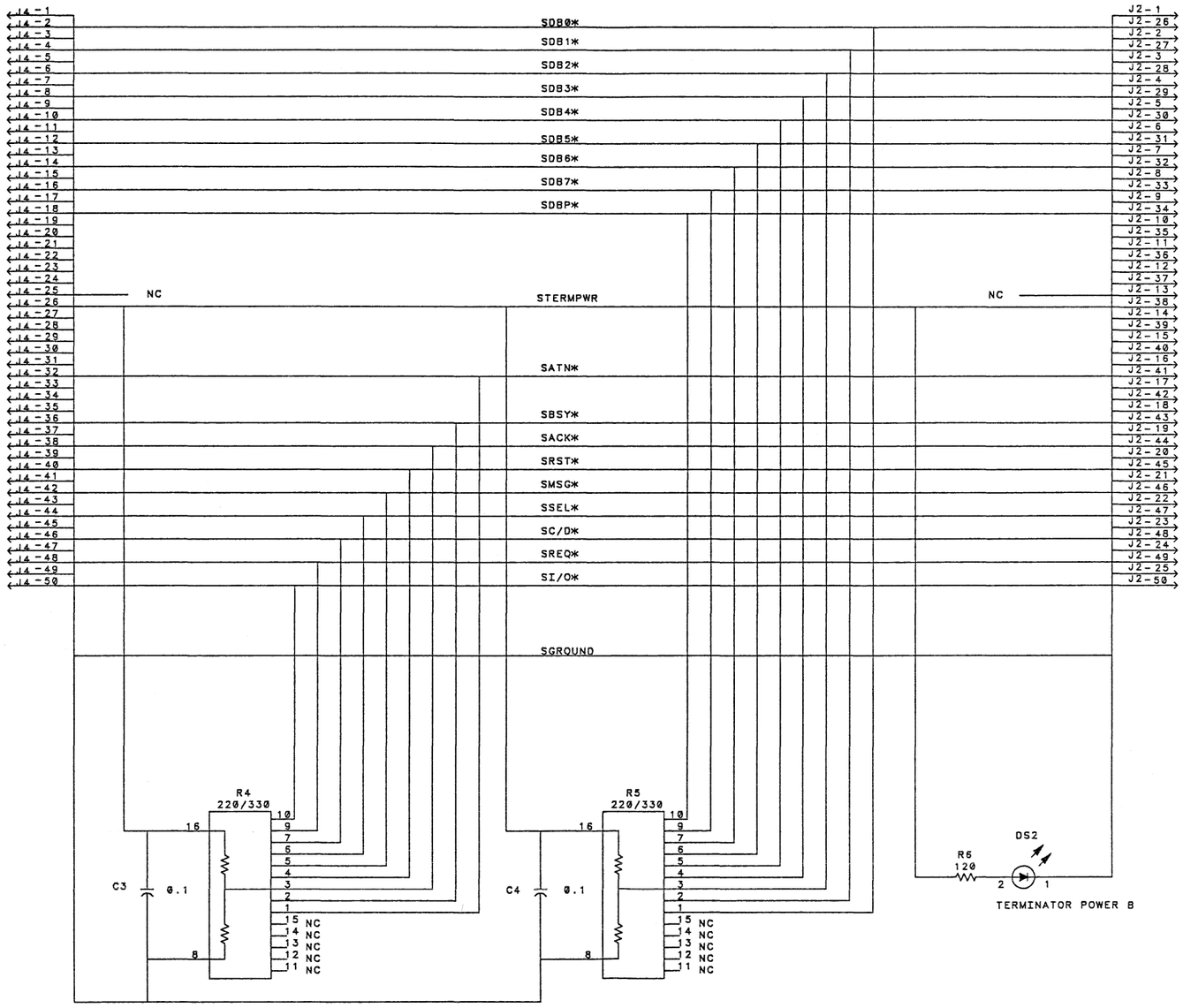

FIGURE 6-4. MVME717 Schematic Diagram 6-13/6-14

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