MVME162LX

Embedded Controller

User's Manual

(MVME162LX/D1)

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Preface

The *MVME162LX User's Manual* provides general information, hardware preparation and installation instructions, operating instructions, and a functional description for the MVME162LX Embedded Controller.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or work in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *Related Documentation* section in Chapter 1 of this manual.

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WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the documentation for this product, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A Computing Device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at the user's own expense, will be required to take whatever measures necessary to correct the interference.

Printed in the United States of America

November 1993

Safety Summary
Safety Depends On You

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola, Inc. assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Use Caution When Exposing or Handling the CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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GENERAL INFORMATION 1

Introduction

This manual provides general information, hardware preparation and installation instructions, operating instructions, and a functional description of the MVME162LX Embedded Controller (referred to as the MVME162LX throughout this manual).

Models

The MVME162LX is available in a number of models, which are listed in Table 1-1.

Table 1-1. MVME162LX Models

Model	Description
-200a	MC68LC040 microprocessor, 1 MB DRAM, 128 KB SRAM, no IndustryPack interface
-201a	MC68LC040 microprocessor, 1 MB DRAM, 128 KB SRAM
-202a	MC68040 microprocessor, 1 MB DRAM, 128 KB SRAM
-210a	MC68LC040 microprocessor, 4 MB DRAM, 128 KB SRAM
-211a	MC68LC040 microprocessor, 4 MB DRAM, SCSI, 128 KB SRAM
-212a	MC68LC040 microprocessor, 4 MB DRAM, Ethernet, 128 KB SRAM
-213a	MC68LC040 microprocessor, 4 MB DRAM, SCSI, Ethernet, 128 KB SRAM, 1 MB Flash memory
-220a	MC68040 microprocessor, 4 MB DRAM, 128 KB SRAM
-221a	MC68040 microprocessor, 4 MB DRAM, SCSI, 128 KB SRAM
-222a	MC68040 microprocessor, 4 MB DRAM, Ethernet, 128 KB SRAM
-223a	MC68040 microprocessor, 4 MB DRAM, SCSI, Ethernet, 128 KB SRAM, 1 MB Flash memory
-260a	MC68040 microprocessor, 16 MB ECC DRAM, 128 KB SRAM
-261a	MC68040 microprocessor, 16 MB ECC DRAM, SCSI, 128 KB SRAM
-262a	MC68040 microprocessor, 16 MB ECC DRAM, Ethernet, 128 KB SRAM
-263a	MC68040 microprocessor, 16 MB ECC DRAM, SCSI, Ethernet, 128 KB SRAM, 1 MB Flash memory

Table 1-1. MVME162LX Models (Continued)

Model	Description
-270a	MC68LC040 microprocessor, 2 MB SRAM
-271a	MC68LC040 microprocessor, 2 MB SRAM, SCSI
-272a	MC68LC040 microprocessor, 2 MB SRAM, Ethernet
-273a	MC68LC040 microprocessor, 2 MB SRAM, SCSI, Ethernet, 1 MB Flash memory
-280a	MC68040 microprocessor, 2 MB SRAM
-281a	MC68040 microprocessor, 2 MB SRAM, SCSI
-282a	MC68040 microprocessor, 2 MB SRAM, Ethernet
-283a	MC68040 microprocessor, 2 MB SRAM, SCSI, Ethernet, 1 MB Flash memory

NOTE: In the model designations above, the suffix *a* denotes the major revision level.

Features

Features of the MVME162LX include:

- ❏ 25-MHz 32-bit microprocessor: either an MC68LC040 Enhanced 32-bit Microprocessor with 8 KB of cache and MMU, or an optional 25-MHz MC68040 32-bit Microprocessor with 8 KB of cache, MMU, and FPU
- ❏ Dynamic Random Access Memory (DRAM): either 1 MB or 4 MB of shared DRAM with programmable parity on a mezzanine module, or 16 MB ECC DRAM on a mezzanine board
- ❏ Static Random Access Memory (SRAM): either 128 KB SRAM with battery backup, or 2 MB SRAM on a mezzanine board with battery backup
- ❏ Four JEDEC standard 32-pin DIP EPROM sockets (EPROMs may be shipped separately from the MVME162LX)
- ❏ 1 MB Flash memory (one Intel 28F008SA) with write protection. Optional.
- ❏ Four 32-bit programmable timers and programmable Watchdog Timer (MCchip)
- ❏ Two 32-bit programmable timers and programmable Watchdog Timer (optional VMEchip2)
- ❏ 8K by 8 Non-Volatile Random Access Memory (NVRAM) and Time of Day (TOD) clock with battery backup (Thompson MK48T08)

- Input/Output
  - EIA-232-D DTE serial interface with four serial ports (Zilog Z85230 controller)
  - Optional Small Computer Systems Interface (SCSI) bus interface with 32-bit local bus burst Direct Memory Access (DMA) (NCR 53C710 controller)
  - Optional LAN Ethernet transceiver interface with 32-bit local bus DMA (Intel 82596CA controller)
  - Two MVIP IndustryPack interfaces. Optional on some models.
- Optional VMEbus interface (VMEchip2)
  - VMEbus system controller functions
  - VMEbus interface to local bus (A24/A32, D8/D16/D32 (D8/D16/D32/D64BLT) (BLT = Block Transfer)
  - Local bus to VMEbus interface (A16/A24/A32, D8/D16/D32)
  - VMEbus interrupter
  - VMEbus interrupt handler
  - Global CSR for interprocessor communications
  - DMA for fast local memory - VMEbus transfers (A16/A24/A32, D16/D32[D16/D32/D64BLT])
- Switches and Light-Emitting Diodes (LEDs)
  - Two pushbutton switches (ABORT and RESET)
  - Four LEDs (FAIL, RUN, SCON, and FUSES)

Specifications

Table 1-2 lists the specifications for an MVME162LX without IndustryPacks. The subsequent sections detail cooling requirements and FCC compliance.

Table 1-2. MVME162LX Specifications

Characteristics	Specifications
Power requirements (with EPROMs; without IPs)	+5Vdc (± 5%), 3.5 A typical, 4.5 A maximum +12 Vdc (± 5%), 100 mA maximum -12 Vdc (± 5%), 100 mA maximum
Operating temperature	0˚ to 70˚ C exit air with forced air cooling (see NOTE)
Storage temperature	-40˚ to +85˚ C
Relative humidity	5% to 90% (noncondensing)
Physical dimensions PC board with mezzanine module only Height Depth Thickness PC board with connectors and front panel Height Depth Thickness	Double-high VMEboard 9.2 inches (233 mm) 6.3 inches (160 mm) 0.66 inch (17 mm) 10.3 inches (262 mm) 7.4 inches (188 mm) 0.80 inch (20 mm)

NOTE: Refer to the following sections on *Cooling Requirements* and *Special Requirements for Elevated-Temperature Operation*.

Cooling Requirements

The Motorola MVME162LX VMEmodule is specified, designed, and tested to operate reliably with an incoming air temperature range from 0˚ to 55˚ C (32˚ to 131˚ F) with forced air cooling at a velocity typically achievable by using a 100 CFM axial fan. Temperature qualification is performed in a standard Motorola MVME900 series chassis. Twenty-five-watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of three axial fans, rated at 100 CFM per fan, is placed directly under the VME card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test.

Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure that component vendor specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 490 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55˚ C with increased airflow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over the module.

Special Considerations for Elevated-Temperature Operation

The following information is for users whose applications for the MVME162LX may subject it to high temperatures.

The MVME162LX uses commercial grade devices. Therefore, it can operate in an environment with ambient air temperatures from 0˚ C to 70˚ C. Several factors influence the ambient temperature seen by components on the MVME162LX. Among them are inlet air temperature; air flow characteristics; number, types, and locations of IndustryPack (IP) modules; power dissipation of adjacent boards in the system, etc.

A temperature profile of the MVME162-223 was developed in an MVME945 12-slot VME chassis. This board was loaded with one GreenSpring IP-Dual P/T module (position a) and one GreenSpring IP-488 module (position b). One twenty-five-watt load board was installed adjacent to each side of the board under test. The exit air velocity was approximately 200 LFM between the MVME162LX and the IP-Dual P/T module. Under these conditions, a 10˚ C rise between the inlet and exit air was observed. At 70˚ C exit air temperature (60˚ C inlet air), the junction temperatures of devices on the MVME162LX were calculated (from the measured case temperatures) and did not exceed 100˚ C.

Caution **For elevated-temperature operation, the user must perform similar measurements and calculations to determine what operating margin exists in a specific environment.**

The following are some steps that the user can take to help make elevated-temperature operation possible:

1. Position the MVME162LX board in the chassis for maximum airflow over the component side of the board.
2. Avoid placing boards with high power dissipation adjacent to the MVME162LX.
3. Use low-power IP modules only.

FCC Compliance

The MVME162LX was tested *without* IndustryPacks in an FCC-compliant chassis and meets the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

1. Shielded cables on all external I/O ports.
2. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
3. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
4. Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the FCC compliance of the equipment containing the module.

General Description

The MVME162LX is a double-high VMEmodule equipped with an MC68LC040 or optional MC68040 microprocessor. (The MC68040 microprocessor has a floating-point coprocessor; the MC68LC040 does not.)

The MVME162LX has 1 MB/4 MB of parity-protected DRAM or 16 MB of ECC-protected DRAM; 128 KB SRAM (with battery backup) or 2 MB SRAM on a mezzanine board; a TOD clock (with battery backup); an optional LAN Ethernet transceiver interface with DMA, four serial ports (EIA-232-D); four to six tick timers with watchdog timer(s), optional SCSI bus interface with DMA, optional VMEbus interface (local bus to VMEbus/VMEbus to local bus, with A16/A24/A32, D8/D16/D32 bus widths and a VMEbus system controller).

Input/Output

Input/Output (I/O) signals are routed through industry-standard connectors on the MVME162LX front panel; no adapter boards or transition modules are necessary. I/O connections on the MVME162LX include an optional 68-pin SCSI connector, an optional DB15 Ethernet connector, and four 8-pin RJ45 serial connectors on the front panel. In addition, the panel has cutouts for routing of flat cables to the optional IndustryPack modules.

VMEbus Interface

The optional VMEchip2 ASIC is the VMEbus interface for the MVME162LX. (This option is a factory build and cannot be added in the field.) VMEchip2 features include:

- ❏ Two programmable 32-bit tick timers
- ❏ A programmable watchdog timer
- ❏ Programmable map decoders for the master and slave interfaces
- ❏ A VMEbus to/from local bus DMA controller
- ❏ A VMEbus to/from local bus non-DMA programmed access interface
- ❏ A VMEbus interrupter
- ❏ A VMEbus system controller
- ❏ A VMEbus interrupt handler
- ❏ A VMEbus requester

Processor-to-VMEbus transfers can be D8, D16, or D32. VMEchip2 DMA transfers to the VMEbus, however, can be D16, D32, D16/BLT, D32/BLT, or D64/MBLT.

No VMEbus Interface Option

If desired, the MVME162LX can function as an embedded controller without a VMEbus interface (i.e., without the optional VMEchip2). Contact your local Motorola sales office for ordering information.

MCchip and MCECC

The Memory Controller (MCchip) ASIC provides four 32-bit programmable tick timers and an interface to the LAN chip, SCSI chip, serial port chip, BBRAM, EPROM/Flash, SRAM, parity DRAM, reset control, watchdog

timers, access timers, and interrupter logic. The MCECC memory controller ASIC provides the programmable interface for the ECC-protected 16 MB DRAM mezzanine board.

Flash Memory and EPROM

The MVME162LX can be ordered with 1 MB of Flash memory and four EPROM sockets ready for the installation of the EPROMs, which may be ordered separately. Flash memory is a single Intel 28F008SA device organized in a 1Mbit x 8 configuration. The EPROM locations are standard JEDEC 32-pin DIP sockets accommodating four jumper-selectable densities (128 Kbit x 8; 256 Kbit X 8; 512 Kbit x 8; 1 Mbit x8). A jumper allows reset code to be fetched either from Flash memory or from the EPROM.

IndustryPack Modules

Up to two IndustryPack (IP) modules may be installed on the MVME162LX as an option. The interface between the IPs and MVME162LX is the IndustryPack Interface Controller (IPIC) ASIC. Access to the IPs is provided by two 3M connectors located behind the MVME162LX front panel.

Optional SCSI Interface

An NCR 53C710 coprocessor provides the SCSI interface for the MVME162LX. The SCSI connector is located on the MVME162LX front panel. SCSI bus terminators are located on the board.

Optional LAN Ethernet Transceiver Interface

An Intel 82596CA controller provides the LAN Ethernet transceiver interface for the MVME162LX. The LAN connector is located on the MVME162LX front panel.

Required Equipment

The following equipment is required to complete an MVME162LX system:

- ❏ System console terminal
- ❏ Disk drives and controllers
- ❏ Operating system

Transition modules are unnecessary, as the MVME162LX incorporates industry-standard SCSI, Ethernet, and RJ45 serial connectors on its front panel.

MVME162Bug Firmware

The 162Bug package, MVME162BUG, is a powerful evaluation and debugging tool for systems built around the MVME162 and MVME162LX CISC-based microcomputers. Facilities are available for loading and executing user programs under complete operator control for system evaluation. 162Bug includes commands for display and modification of memory, breakpoint and tracing capabilities, a powerful assembler/disassembler useful for patching programs, and a self-test at power-up which verifies the integrity of the system. Various 162Bug routines that handle I/O, data conversion, and string functions are available to user programs through the TRAP #15 system calls.

Note **MVME162Bug occupies 512 KB of EPROM space.**

Available Software

Available software for the MVME162LX includes the on-board debugger/monitor firmware, VMEexec driver packages for various IndustryPack modules, and numerous third-party applications for MC680*x*0-based systems. Contact your local Motorola sales office for more information.

Related Documentation

The following publications are applicable to the MVME162LX and may provide additional helpful information. If not shipped with this product, they may be purchased by contacting your local Motorola sales office. Non-Motorola documents may be purchased from the sources listed.

Document Title	Motorola Publication Number
MVME162Bug Debugging Package User's Manual	MVME162BUG
Debugging Package for Motorola 68K CISC CPUs User's Manual	68KBUG
MVME162LX Embedded Controller Programmer's Reference Guide	MVME162LXPG
M68040 Microprocessors User's Manual	M68040UM
MVME1*x*7 Data Sheet Package (for use with the MVME162[LX] and the MVME166/MVME167/MVME187)	68-1X7DS

Notes

Although not shown in the above list, each Motorola Computer Group manual publication number is suffixed with characters which represent the revision level of the document, such as "/D2" (the second revision of a manual); a supplement bears the same number as a manual but has a suffix such as "/D2A1" (the first supplement to the second edition of the manual).

The *MVME1x7 Data Sheet Package* is composed of vendor-supplied data sheets and manuals for the peripheral controllers used on the MVME162LX and other boards.

The following publications are available from the sources indicated.

Versatile Backplane Bus: VMEbus, ANSI/IEEE Std 1014-1987, The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017 (VMEbus Specification). This is also available as *Microprocessor system bus for 1 to 4 byte data, IEC 821 BUS*, Bureau Central de la Commission Electrotechnique Internationale; 3, rue de Varembé, Geneva, Switzerland.

ANSI Small Computer System Interface-2 (SCSI-2), Draft Document X3.131-198X, Revision 10c; Global Engineering Documents, P.O. Box 19539, Irvine, CA 92714.

IndustryPack Logic Interface Specification, Revision 1.0; GreenSpring Computers, Inc., 1204 O'Brien Drive, Menlo Park, CA 94025.

82596CA Local Area Network Coprocessor Data Sheet, Order Number 290218; and *82596 User's Manual*, Order Number 296853-001; Intel Corporation, Literature Sales, P.O. Box 58130, Santa Clara, CA 95052-8130.

NCR 53C710 SCSI I/O Processor, Data Manual Document #SCSIP-53C710; NCR Corporation, Microelectronics Products Division, Colorado Springs, CO.

MK48T08(B) Timekeeper™ and 8Kx8 Zeropower™ RAM data sheet in *Static RAMs Databook*, Order Code DBSRAM71; SGS-THOMPSON Microelectronics Group; North & South American Marketing Headquarters, 1000 East Bell Road, Phoenix, AZ 85022-2699.

Z85230 Serial Communications Controller Data Sheet; Zilog Inc.,, 210 Hacienda Avenue, Campbell, CA 95008-6609.

28F008SA FLASH Memory Data Sheet, Order Number 290435-001; Intel Literature Sales, P.O. Box 7641, Mt. Prospect, IL 60056-7641.

Support Information

You can obtain connector interconnect signal information, parts lists, and schematics for the MVME162LX free of charge by contacting your local Motorola sales office.

Manual Terminology

Throughout this manual, a convention is used which precedes data and address parameters by a character identifying the numeric format as follows:

$	dollar	specifies a hexadecimal character
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal.

An asterisk (*) following the signal name for signals which are level-significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge-significant denotes that the actions initiated by that signal occur on high-to-low transition.

In this manual, *assertion* and *negation* are used to specify forcing a signal to a particular state. In particular, *assertion* and *assert* refer to a signal that is active or true; *negation* and *negate* indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:

- A byte is eight bits, numbered 0 through 7, with bit 0 being the least significant.
- A word is 16 bits, numbered 0 through 15, with bit 0 being the least significant.
- A longword is 32 bits, numbered 0 through 31, with bit 0 being the least significant.

HARDWARE PREPARATION AND INSTALLATION 2

Introduction

This chapter provides unpacking instructions, hardware preparation guidelines, and installation instructions for the MVME162LX Embedded Controller.

Unpacking Instructions

Note **If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.**

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.

Caution **Avoid touching areas of integrated circuitry; static discharge can damage circuits.**

Hardware Preparation

To select the desired configuration and ensure proper operation of the MVME162LX, certain option modifications may be necessary before installation. The MVME162LX provides software control for most of these options. Some options cannot be modified in software, and consequently are set by installing or removing jumpers on headers. Most other modifications are performed by setting bits in control registers after the MVME162LX has been installed in a system. (The MVME162LX registers are described in Chapter 4, and/or in the *MVME162LX Embedded Controller Programmer's Reference Guide* as listed in *Related Documentation* in Chapter 1.)

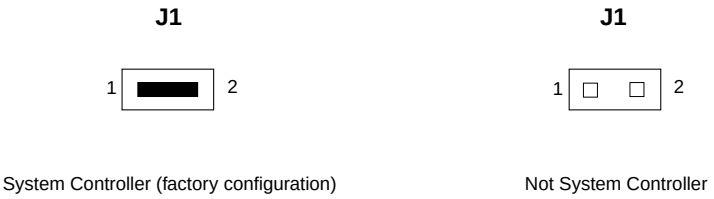
Figure 2-1 illustrates the placement of the switches, jumper headers, connectors, and LED indicators on the MVME162LX . The MVME162LX has been factory tested and is shipped with the factory jumper settings described in the following sections. The MVME162LX operates with its required and factory-installed Debug Monitor, MVME162Bug (162Bug), with these factory jumper settings. Settings can be made for:

- ❏ System controller selection (J1)
- ❏ General-purpose readable register configuration (J11)
- ❏ EPROM/Flash configuration (J12)
- ❏ SRAM backup power source selection (for onboard SRAM: J13 on the MVME162LX main module. For the SRAM mezzanine: J1 on the SRAM mezzanine)
- ❏ SCSI bus termination (J14)

System Controller Select Header (J1)

The MVME162LX is factory-configured as a VMEbus system controller (i.e., a jumper is installed across pins 1 and 2 of header J1). Remove the J1 jumper if the MVME162LX is not to be the system controller. Note that when the MVME162LX is functioning as system controller, the SCON LED is turned on.

Note **For MVME162LXs without the optional VMEbus interface (i.e., with no VMEchip2), the jumper may be installed or removed without affecting normal operation.**



System Controller (factory configuration)

Not System Controller

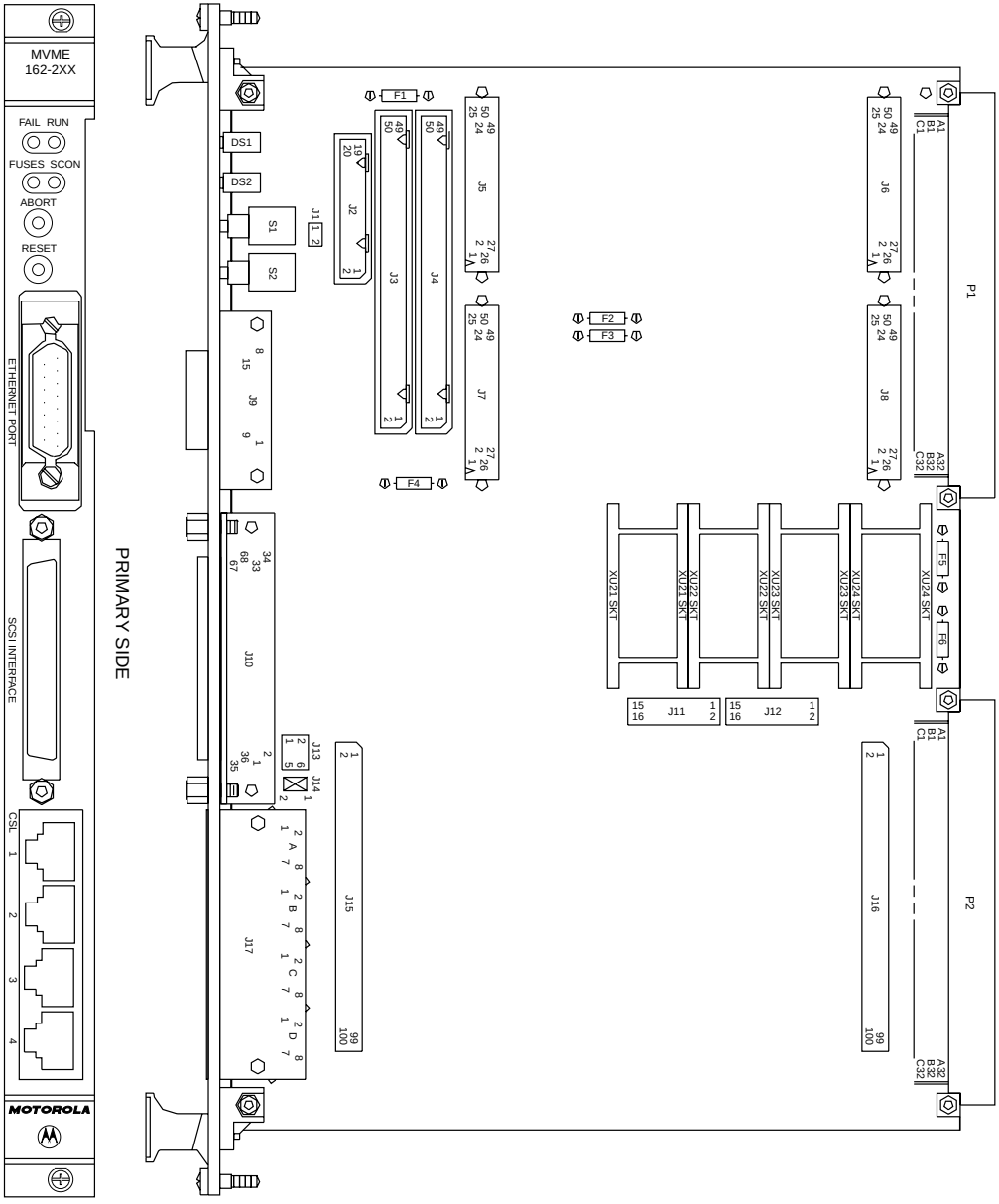


Figure 2-1. MVME162LX Switch, Header, Connector, Fuse, and LED Locations

2

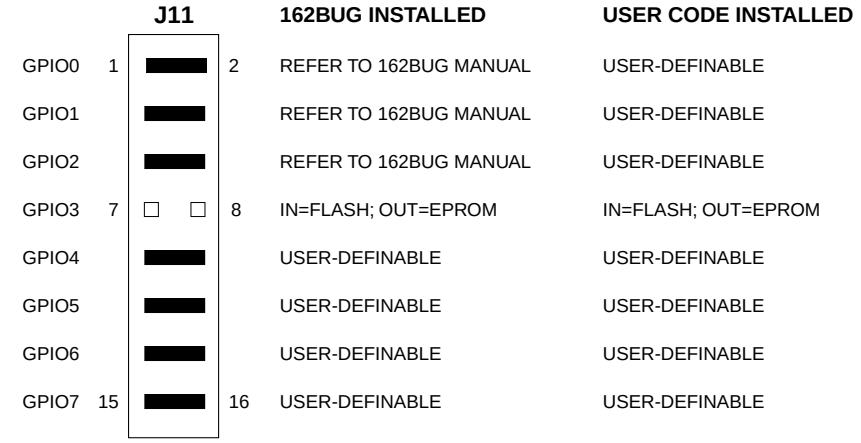
General-Purpose Readable Jumpers Header (J11)

Header J11 provides eight readable jumpers. These jumpers can be read as a register (at $FFF4202D) in the MCchip LCSR. The bit values are read as a zero when the jumper is installed, and as a one when the jumper is removed.

If the MVME162BUG firmware is installed, four jumpers are user-definable (pins 9-10, 11-12, 13-14, 15-16). If the MVME162BUG firmware is not installed, seven jumpers are user-definable (pins 1-2, 3-4, 5-6, 9-10, 11-12, 13-14, 15-16).

Note **Pins 7-8 (GPIO3) are reserved to select either the Flash memory map (jumper installed) or the EPROM memory map (jumper removed). They are not user-definable. The address ranges for the various EPROM/Flash configurations appear in the next section of this chapter.**

The MVME162LX is shipped from the factory with J11 set to all zeros (jumpers on all pins) except for GPIO3.

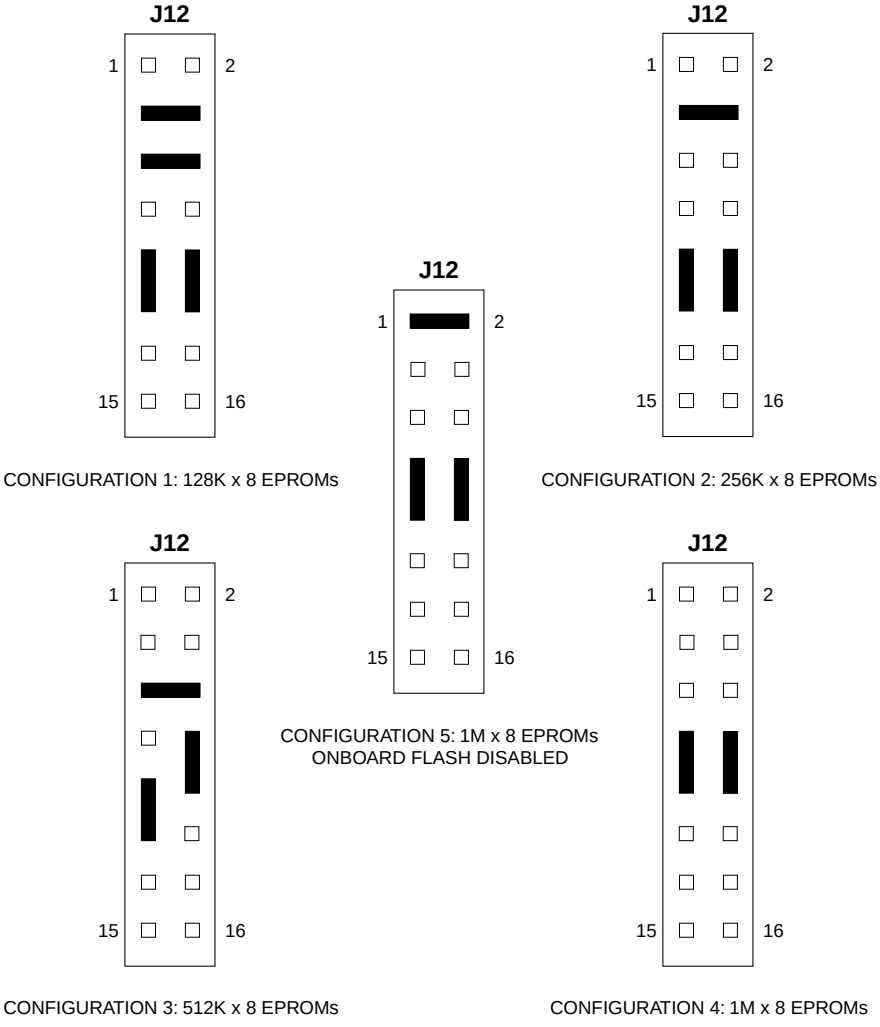


EPROMs Selected (factory configuration)

EPROM/Flash Configuration Header (J12)

The MVME162LX can be ordered with 1 MB of Flash memory and four EPROM sockets ready for the installation of the EPROMs, which may be ordered separately. The EPROM locations are standard JEDEC 32-pin DIP sockets that accommodate four jumper-selectable densities (128 Kbit x 8; 256 Kbit x 8; 512 Kbit x 8; 1 Mbit x 8) and permit disabling of the Flash memory.

Header J12 provides eight jumpers to configure the EPROM sockets.



The next five tables show the address range for each EPROM socket in all five configurations. GPIO3 (J11 pins 7-8) is a control bit in the MCchip ASIC that allows reset code to be fetched either from Flash memory or from EPROMs.

Table 2-1. EPROM/Flash Mapping—128K x 8 EPROMs

GPIO3		Address Range	Device Accessed
Removed	1	$FF800000 - $FF81FFFF	EPROM A (XU24)
		$FF820000 - $FF83FFFF	EPROM B (XU23)
		$FF840000 - $FF85FFFF	EPROM C (XU22)
		$FF860000 - $FF87FFFF	EPROM D (XU21)
		$FFA00000 - $FFBFFFFF	On-Board Flash
Installed	0	$FF800000 - $FF9FFFFF	On-Board Flash
		$FFA00000 - $FFA1FFFF	EPROM A (XU24)
		$FFA20000 - $FFA3FFFF	EPROM B (XU23)
		$FFA40000 - $FFA5FFFF	EPROM C (XU22)
		$FFA60000 - $FBA7FFFF	EPROM D (XU21)

Table 2-2. EPROM/Flash Mapping —256K x 8 EPROMs

GPIO3		Address Range	Device Accessed
Removed	1	$FF800000 - $FF83FFFF	EPROM A (XU24)
		$FF840000 - $FF87FFFF	EPROM B (XU23)
		$FF880000 - $FF8BFFFF	EPROM C (XU22)
		$FF8C0000 - $FF8FFFFF	EPROM D (XU21)
		$FFA00000 - $FFBFFFFF	On-Board Flash
Installed	0	$FF800000 - $FF9FFFFF	On-Board Flash
		$FFA00000 - $FFA3FFFF	EPROM A (XU24)
		$FFA40000 - $FFA7FFFF	EPROM B (XU23)
		$FFA80000 - $FFABFFFF	EPROM C (XU22)
		$FFAC0000 - $FBAFFFFF	EPROM D (XU21)

Table 2-3. EPROM/Flash Mapping—512K x 8 EPROMs

GPIO3		Address Range	Device Accessed
Removed	1	$FF800000 - $FF87FFFF	EPROM A (XU24)
		$FF880000 - $FF8FFFFF	EPROM B (XU23)
		$FF900000 - $FF97FFFF	EPROM C (XU22)
		$FF980000 - $FF9FFFFF	EPROM D (XU21)
		$FFA00000 - $FFBFFFFF	On-Board Flash
Installed	0	$FF800000 - $FF9FFFFF	On-Board Flash
		$FFA00000 - $FFA7FFFF	EPROM A (XU24)
		$FFA80000 - $FFAFFFFF	EPROM B (XU23)
		$FFB00000 - $FFB7FFFF	EPROM C (XU22)
		$FFB80000 - $FBF7FFFF	EPROM D (XU21)

Table 2-4. EPROM/Flash Mapping—1M x 8 EPROMs

GPIO3		Address Range	Device Accessed
Removed	1	$FF800000 - $FF8FFFFF	EPROM A (XU24)
		$FF900000 - $FF9FFFFF	EPROM B (XU23)
		Not used	EPROM C (XU22)
		Not used	EPROM D (XU21)
		$FFA00000 - $FFBFFFFF	On-Board Flash
Installed	0	$FF800000 - $FF9FFFFF	On-Board Flash
		$FFA00000 - $FFAFFFFF	EPROM A (XU24)
		$FFB00000 - $FFBFFFFF	EPROM B (XU23)
		Not used	EPROM C (XU22)
		Not used	EPROM D (XU21)

Table 2-5. EPROM/Flash Mapping—1M x 8 EPROMs, On-Board Flash Disabled

GPIO3		Address Range	Device Accessed
Removed	1	$FF800000 - $FF8FFFFF	EPROM A (XU24)
		$FF900000 - $FF9FFFFF	EPROM B (XU23)
		$FFA00000 - $FFAFFFFF	EPROM C (XU22)
		$FFB00000 - $FFBFFFFF	EPROM D (XU21)
		Not used	On-Board Flash
Installed	0	Not used	On-Board Flash
		$FF800000 - $FF8FFFFF	EPROM A (XU24)
		$FF900000 - $FF9FFFFF	EPROM B (XU23)
		$FFA00000 - $FFAFFFFF	EPROM C (XU22)
		$FFB00000 - $FFBFFFFF	EPROM D (XU21)

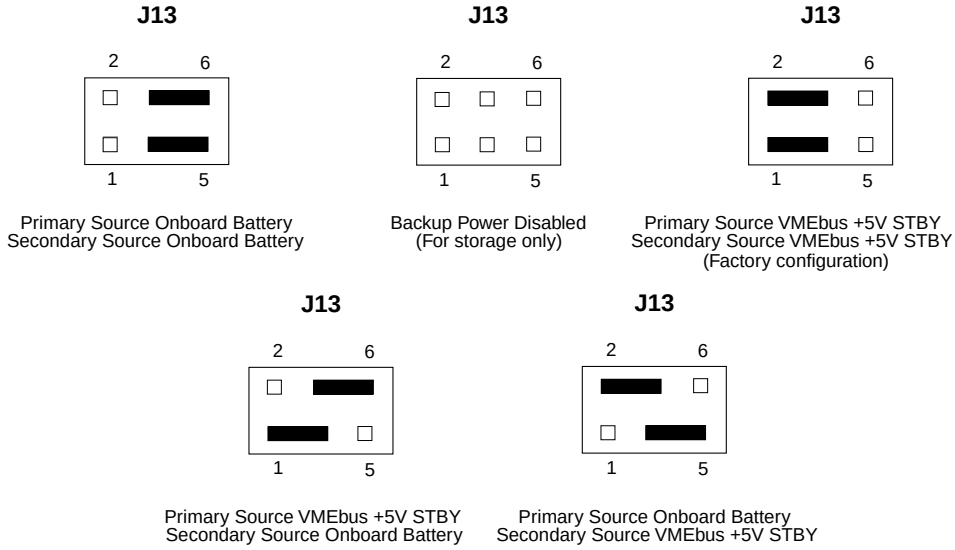
SRAM Backup Power Source Select Headers (J13, J1)

Header J13 determines the source for onboard static RAM backup power on the MVME162LX main module. Header J1 determines the source for backup power on the 2MB SRAM mezzanine board (if installed).

The following backup power configurations are available for onboard SRAM through header J13. In the factory configuration, the VMEbus +5V standby voltage serves as primary and secondary power source (the onboard battery is disconnected).

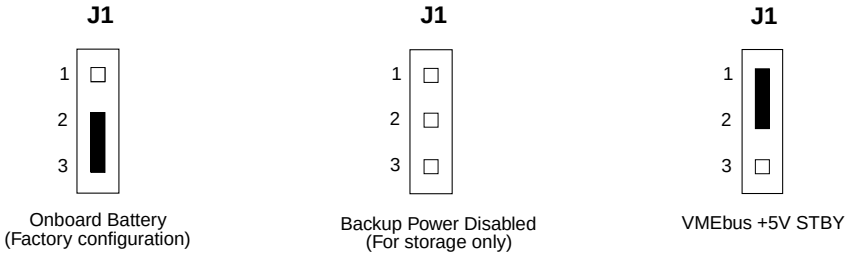
Note **For MVME162LXs without the optional VMEbus interface (i.e., without the VMEchip2 ASIC), you must select the on-board battery as the backup power source.**

Caution **Removing all jumpers may temporarily disable the SRAM. Do not remove all jumpers from J13, except for storage.**



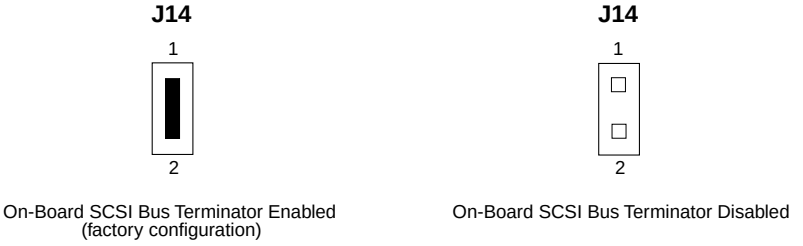
The following backup power configurations are available for the 2MB mezzanine SRAM through header J1 (located on the mezzanine). In the factory configuration, the onboard battery serves as secondary power source.

Caution **Removing the jumper may temporarily disable the SRAM mezzanine. Do not remove the jumper from J1, except for storage.**



SCSI Terminator Enable Header J14

The MVME162LX provides terminators for the SCSI bus. The SCSI terminators are enabled / disabled by a jumper on header J14. The SCSI terminators may be configured as follows.



Note **If the MVME162LX is to be used at one end of the SCSI bus, the SCSI bus terminators must be enabled.**

Memory Mezzanine Options

Two 100-pin connectors (J15 and J16) are provided on the MVME162LX main module to accommodate optional memory mezzanine boards. Three memory mezzanine options are available for the MVME162LX:

- ❏ 1 MB or 4 MB parity DRAM
- ❏ 16 MB ECC DRAM
- ❏ 2 MB SRAM with battery backup

The mezzanine boards may either be used individually or be combined in a stack (not more than two deep). The following connector options govern stacking arrangements:

- ❏ The 1 MB or 4 MB parity DRAM board has connectors on the bottom only; it must be either the only mezzanine or the top mezzanine.
- ❏ The 16 MB ECC DRAM and 2 MB SRAM boards are available with two connector options:
  - Connectors on the bottom only; must be either the only mezzanine or the top mezzanine
  - Both top and bottom connectors to facilitate stacking (note, however, that a stack can never contain two 2 MB SRAM boards due to the 2 MB maximum for SRAM storage)

When the mezzanines are stacked, the following combinations are possible:

Table 2-6. Memory Mezzanine Stacking Options

	SRAM Mezzanine	Parity DRAM Mezzanine	ECC DRAM Mezzanine
SRAM Mezzanine	No	Yes	Yes
Parity DRAM Mezzanine	Yes	No	Yes
ECC DRAM Mezzanine	Yes	Yes	Yes

Installation Instructions

The following sections describe the installation of IndustryPacks (IPs) on the MVME162LX and the installation of the MVME162LX in a VME chassis, and discuss system considerations relevant to the installation. Ensure that EPROM devices are installed as needed. Ensure that all header jumpers are configured as desired.

IP Installation on the MVME162LX

Up to two IndustryPack (IP) modules may be installed on the MVME162. Install the IPs on the MVME162LX as follows:

1. Each IP has two 50-pin connectors that plug into two corresponding 50-pin connectors on the MVME162LX: J5/J6, J7/J8. See Figure 2-1 for the MVME162LX connector locations.
   - Orient the IP(s) so that the tapered connector shells mate properly. Plug IP_a into connectors J5 and J6; plug IP_b into J7 and J8. If a double-sized IP is used, plug IP_ab into J5, J6, J7, and J8.
2. Two additional 50-pin connectors (J3 and J4) are provided behind the MVME162LX front panel for external cabling connections to the IP modules. There is a one-to-one correspondence between the signals on the cabling connectors and the signals on the associated IP connectors (i.e., J4 has the same IP_a signals as J5; J3 has the same IP_b signals as J7).
   - Connect user-supplied 50-pin cables to J3 and J4 as needed. Because of the varying requirements for each different kind of IP, Motorola does not supply these cables.
   - Bring the IP cables out the narrow slot in the MVME162LX front panel and attach them to the appropriate external equipment, depending on the nature of the particular IP(s).

MVME162LX Module Installation

With EPROMs and IndustryPacks installed and headers properly configured, proceed as follows to install the MVME162LX in the VME chassis:

1. Turn all equipment power OFF and disconnect the power cable from the AC power source.

Caution **Inserting or removing modules while power is applied could result in damage to module components.**

WARNING **Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.**

2. Remove the chassis cover as instructed in the user's manual for the equipment.
3. Remove the filler panel from the card slot where you are going to install the MVME162LX.
   - If you intend to use the MVME162LX as system controller, it must occupy the leftmost card slot (slot 1). The system controller must be in slot 1 to correctly initiate the bus-grant daisy-chain and to ensure proper operation of the IACK daisy-chain driver.
   - If you do not intend to use the MVME162LX as system controller, it can occupy any unused double-height card slot.
4. Slide the MVME162LX into the selected card slot. Be sure the module is seated properly in the P1 and P2 connectors on the backplane. Do not damage or bend connector pins.
5. Secure the MVME162LX in the chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
6. On the chassis backplane, remove the INTERRUPT ACKNOWLEDGE (IACK) and BUS GRANT (BG) jumpers from the header for the card slot occupied by the MVME162LX.
7. Connect the appropriate cable(s) to the MVME162LX panel connectors for the EIA-232-D serial ports, SCSI port, and LAN Ethernet port.
   - Note that some cables are not provided with the MVME162LX module and must be made or purchased by the user. (Motorola recommends shielded cable for all peripheral connections to minimize radiation.)
8. Connect the peripheral(s) to the cable(s). Appendix A supplies detailed information on the EIA-232-D signals supported. Appendix B describes the Ethernet LAN (*Local Area Network*) port connections. Appendix C describes the SCSI (*Small Computer System Interface*) I/O bus connections.
9. Install any other required VMEmodules in the system.
10. Replace the chassis cover.
11. Connect the power cable to the AC power source and turn the equipment power ON.

System Considerations

The MVME162LX draws power from both the P1 and the P2 connectors on the VMEbus backplane. P2 is also used for the upper 16 bits of data in 32-bit transfers, and for the upper 8 address lines in extended addressing mode. The MVME162LX may not operate properly without its main board connected to VMEbus backplane connectors P1 and P2.

Whether the MVME162LX operates as a VMEbus master or as a VMEbus slave, it is configured for 32 bits of address and 32 bits of data (A32/D32). However, it handles A16 or A24 devices in the address ranges indicated in Chapter 3. D8 and/or D16 devices in the system must be handled by the MC68040/ MC68LC040 software. Refer to the memory maps in Chapter 3.

The MVME162LX contains shared onboard DRAM whose base address is software-selectable. Both the onboard processor and offboard VMEbus devices see this local DRAM at base physical address $00000000, as programmed by the MVME162Bug firmware. This may be changed via software to any other base address. Refer to the *MVME162LX Embedded Controller Programmer's Reference Guide* for more information.

If the MVME162LX tries to access offboard resources in a nonexistent location and is not system controller, and if the system does not have a global bus timeout, the MVME162LX waits forever for the VMEbus cycle to complete. This will cause the system to lock up. There is only one situation in which the system might lack this global bus timeout: when the MVME162LX is not the system controller and there is no global bus timeout elsewhere in the system.

Multiple MVME162LXs may be installed in a single VME chassis. In general, hardware multiprocessor features are supported.

Note **If you are installing multiple MVME162LXs in an MVME945 chassis, do not install an MVME162LX in slot 12. The height of the IP modules may cause clearance difficulties in that slot position.**

Other MPUs on the VMEbus can interrupt, disable, communicate with, and determine the operational status of the processor(s). One register of the GCSR (global control/status register) set includes four bits that function as location monitors to allow one MVME162LX processor to broadcast a signal to any other MVME162LX processors. All eight registers are accessible from any local processor as well as from the VMEbus.

The MVME162LX provides +5 Vdc power to the remote LED/switch connector (J2) as well as to IP_b through a 2A fuse (F3) located near J7. Connector J2 is the interface for a remote control and indicator panel. If none of the LEDs light and the ABORT and RESET switches do not operate, check fuse F3.

The MVME162LX provides +12 Vdc power to the Ethernet transceiver interface through a 1A fuse (F1) located near J3. The FUSES LED lights to indicate that +12 Vdc is available. If the Ethernet transceiver fails to operate, check fuse F1.

The MVME162LX provides +5 Vdc to the SCSI bus TERMPWR signal through fuse F4, located near J7. One function of the FUSES LED (part of DS2) on the front panel is to monitor the SCSI bus TERMPWR signal; with the MVME162LX connected to an SCSI bus, the FUSES LED lights when there is SCSI terminator power. Because any device on the SCSI bus can provide TERMPWR, the LED does not directly indicate the condition of the fuse. If the LED flickers during SCSI bus operation, check the fuse. This display also indicates the status of the +5 Vdc (F2, F3), +12 Vdc (F5), and -12 Vdc (F6) fuses for the IP modules.

The MVME162LX uses two Zilog Z85230 serial port controllers to implement the four serial communications interfaces. Each interface supports CTS, DCD, RTS, and DTR control signals as well as the TXD and RXD transmit/receive data signals. Because the serial clocks are omitted in the MVME162LX implementation, serial communications are strictly asynchronous. The Z85230 is interfaced as DTE (data terminal equipment) with EIA-232-D signal levels. The serial ports are routed to four RJ45 connectors on the front panel.

For additional information on the EIA-232-D interface and its implementation in the MVME162LX, refer to Appendix A.

OPERATING INSTRUCTIONS 3

Introduction

This chapter provides information necessary to use the MVME162LX in a system configuration. This includes a description of the switches and LEDs, memory maps, and software initialization of the module.

Switches and LEDs

The MVME162LX front panel has ABORT and RESET switches and four LED (light-emitting diode) indicators (FAIL, RUN, SCON, FUSES).

ABORT Switch (S1)

When enabled by software, the ABORT switch generates an interrupt at a user-programmable level. It is normally used to abort program execution and return to the 162Bug debugger firmware located in the MVME162LX EPROMs and Flash memory.

The ABORT switch interrupter in the MCchip ASIC is an edge-sensitive interrupter connected to the ABORT switch. This interrupter is filtered to remove switch bounce.

RESET Switch (S2)

The RESET switch resets all onboard devices; it also drives SYSRESET* if the MVME162LX is operating as system controller. The RESET switch may be disabled by software.

The VMEchip2 includes both a global and a local reset driver. When the VMEchip2 operates as the VMEbus system controller, the reset driver provides a global system reset by asserting the VMEbus signal SYSRESET*. A SYSRESET* may be generated by the RESET switch, a power-up reset, a watchdog timeout, or by a control bit in the LCSR (local control/status register) in the VMEchip2. SYSRESET* remains asserted for at least 200 msec, as required by the VMEbus specification.

Similarly, the VMEchip2 provides an input signal and a control bit to initiate a local reset operation. By setting a control bit, software can maintain a board in a reset state, disabling a faulty board from participating in normal system operation. The local reset driver is enabled even when the VMEchip2 is not the

system controller. A local reset may be generated by the RESET switch, a power-up reset, a watchdog timeout, a VMEbus SYSRESET*, or by a control bit in the GCSR (global control/status register).

Note **For an MVME162LX without the VMEbus option (i.e., with no VMEchip2), the LCSR control bit is not available to reset the module. In this case, the watchdog timer is allowed to time out to reset the MVME162LX.**

Front Panel Indicators (DS1-DS4)

There are four LEDs on the MVME162LX front panel: FAIL, RUN, SCON, and FUSES.

- FAIL LED (red). Lights when the BRDFAIL* signal line is active or when the processor is halted. Part of DS1.
- RUN LED (green or amber). Lights when the local bus TIP* signal line is low. This indicates one of the local bus masters is executing a local bus cycle. Part of DS1.
- SCON LED (green). Lights when the VMEchip2 in the MVME162LX is the VMEbus system controller. Part of DS2.
- FUSES LED (green). Lights when +5 Vdc, +12 Vdc, and -12 Vdc power is available to the LAN, IP, and SCSI interfaces. Part of DS2.

Memory Maps

There are two points of view for memory maps:

- The mapping of all resources as viewed by local bus masters (local bus memory map)
- The mapping of onboard resources as viewed by VMEbus masters (VMEbus memory map)

Local Bus Memory Map

The local bus memory map is split into different address spaces by the Transfer Type (TT) signals. The local resources respond to the normal access and interrupt acknowledge codes.

Normal Address Range

The memory map of devices that respond to the normal address range is shown in the following tables. The normal address range is defined by the TT signals on the local bus. For the MVME162LX, transfer types 0, 1, and 2 define the normal address range. Table 3-1 defines the entire map ($00000000 to $FFFFFFFF). Many areas of the map are user-programmable, and suggested uses are shown in the table. The cache inhibit function is programmable in the MC68xx040 MMU. The onboard I/O space must be marked ''cache inhibit'' and serialized in its page table. Table 3-2 further defines the map for the local I/O devices.

Table 3-1. Local Bus Memory Map

Address Range	Devices Accessed	Port Width	Size	Software Cache Inhibit	Notes
Programmable	DRAM on Parity Mezzanine	D32	1 MB-4 MB	N	2
Programmable	DRAM on ECC Mezzanine	D32	16 MB	N	2
Programmable	On-Board SRAM	D32	128 KB	N	2, 7
Programmable	SRAM on Mezzanine	D32	2 MB	N	2, 7
Programmable	VMEbus A32/A24	D32/D16	--	?	4
Programmable	IP_a Memory	D32-D8	64 KB-8 MB	?	2, 4
Programmable	IP_b Memory	D32-D8	64 KB-8 MB	?	2, 4
$FF800000-$FF9FFFFF	Flash/EPROM	D32	2 MB	N	1, 5
$FFA00000-$FFBFFFFF	EPROM/Flash	D32	2 MB	N	5
$FFC00000-$FFDFFFFF	Not Decoded	D32	2 MB	N	7
$FFE00000-$FFE1FFFF	On-Board SRAM Default	D32	128 KB	N	7
$FFE80000-$FFEFFFFF	Not Decoded	--	512 KB	N	6
$FFF00000-$FFFEFFFF	Local I/O Devices (Refer to next table)	D32-D8	878 KB	Y	3
$FFFF0000-$FFFFFFFF	VMEbus A16	D32/D16	64 KB	?	2, 4

NOTES: 1. Devices mapped at $FFF80000-$FFF9FFFF also appear at $00000000-$001FFFFF when the ROM0 bit in the MCchip EPROM control register is high (ROM0=1). ROM0 is set to 1 after each reset. The ROM0 bit must be cleared before other resources (DRAM or SRAM) can be mapped in this range ($00000000 - $001FFFFF).

The EPROM/Flash memory map is also controlled by the EPROM size and by control bit V19 in the MCchip ASIC. Refer to the EPROM/Flash configuration tables in Chapter 2 for further details.

2. This area is user-programmable. The DRAM and SRAM decoder is programmed in the MCchip, the local-to-VMEbus decoders are programmed in the VMEchip2, and the IP memory space is programmed in the IPIC.
3. Size is approximate.
4. Cache inhibit depends on the devices in the area mapped.
5. The EPROM and Flash are dynamically sized by the MCchip ASIC from an 8-bit private bus to the 32-bit MPU local bus.
6. These areas are not decoded unless one of the programmable decoders is initialized to decode this space. If they are not decoded and the local timer is enabled, an access to this address range will generate a local bus timeout.
7. SRAM is 128 KB when no SRAM mezzanine is present. With an SRAM mezzanine board, the SRAM size is 2 MB and the on-board 128 KB SRAM is disabled.

Table 3-2 focuses on the ''Local I/O Devices'' portion of the local bus main memory map.

Note **The IPIC chip on the MVME162LX supports up to four IndustryPack (IP) interfaces, designated IP_a through IP_d. The MVME162LX itself accommodates two IPs: IP_a and IP_b. In the following map, the segments applicable to IP_c and IP_d are not used in the MVME162LX.**

Table 3-2. Local I/O Devices Memory Map

Address Range	Devices Accessed	Port Width	Size	Notes
$FFF00000 - $FFF3FFFF	Reserved	- -	256 KB	4
$FFF40000 - $FFF400FF	VMEchip2 (LCSR)	D32	256 B	1, 3
$FFF40100 - $FFF401FF	VMEchip2 (GCSR)	D32-D8	256 B	1, 3
$FFF40200 - $FFF40FFF	Reserved	- -	3.5 KB	4, 5
$FFF41000 - $FFF41FFF	Reserved	- -	4 KB	4
$FFF42000 - $FFF42FFF	MCchip	D32-D8	4 KB	1
$FFF43000 - $FFF430FF	MCECC #1	D8	256 B	1, 9
$FFF43100 - $FFF431FF	MCECC #2	D8	256 B	1, 9
$FFF43200 - $FFF43FFF	MCECCs (repeated)	- -	3.5 KB	1, 5, 9
$FFF44000 - $FFF44FFF	Reserved	- -	8 KB	4
$FFF45000 - $FFF45800	SCC #1 (Z85230)	D8	2 KB	1, 2
$FFF45801 - $FFF45FFF	SCC #2 (Z85230)	D8	2 KB	1, 2
$FFF46000 - $FFF46FFF	LAN (82596CA)	D32	4 KB	1, 6
$FFF47000 - $FFF47FFF	SCSI (53C710)	D32-D8	4 KB	1
$FFF48000 - $FFF57FFF	Reserved	- -	64 KB	4
$FFF58000 - $FFF5807F	IPIC IP_a I/O	D16	128 B	1
$FFF58080 - $FFF580FF	IPIC IP_a ID	D16	128 B	1
$FFF58100 - $FFF5817F	IPIC IP_b I/O	D16	128 B	1
$FFF58180 - $FFF581FF	IPIC IP_b ID Read	D16	128 B	1
$FFF58200 - $FFF5827F	IPIC IP_c I/O	D16	128 B	8
$FFF58280 - $FFF582FF	IPIC IP_c ID	D16	128 B	8
$FFF58300 - $FFF5837F	IPIC IP_d I/O	D16	128 B	8
$FFF58380 - $FFF583FF	IPIC IP_d ID Read	D16	128 B	8
$FFF58400 - $FFF584FF	IPIC IP_ab I/O	D32-D16	256 B	1
$FFF58500 - $FFF585FF	IPIC IP_cd I/O	D32-D16	256 B	8
$FFF58600 - $FFF586FF	IPIC IP_ab I/O Repeated	D32-D16	256 B	1
$FFF58700 - $FFF587FF	IPIC IP_cd I/O Repeated	D32-D16	256 B	8
$FFF58800 - $FFF5887F	Reserved	- -	128 B	1
$FFF58880 - $FFF588FF	Reserved	- -	128 B	1
$FFF58900 - $FFF5897F	Reserved	- -	128 B	1
$FFF58980 - $FFF589FF	Reserved	- -	128 B	1
$FFF58A00 - $FFF58A7F	Reserved	- -	128 B	1
$FFF58A80 - $FFF58AFF	Reserved	- -	128 B	1
$FFF58B00 - $FFF58B7F	Reserved	- -	128 B	1

Table 3-2. Local I/O Devices Memory Map (Continued)

Address Range	Devices Accessed	Port Width	Size	Notes
$FFF58B80 - $FFF58BFF	Reserved	- -	128 B	1
$FFF58C00 - $FFF58CFF	Reserved	- -	256 B	1
$FFF58D00 - $FFF58DFF	Reserved	- -	256 B	1
$FFF58E00 - $FFF58EFF	Reserved	- -	256 B	1
$FFF58F00 - $FFF58FFF	Reserved	- -	256 B	1
$FFFBC000 - $FFFBC01F	IPIC Registers	D32-D8	2 KB	1
$FFFBC800 - $FFFBC81F	Reserved	- -	2 KB	1
$FFFBD000 - $FFFBFFFF	Reserved	- -	12 KB	4
$FFFC0000 - $FFFC7FFF	MK48T08 (BBRAM, TOD Clock)	D32-D8	32 KB	1
$FFFC8000 - $FFFCBFFF	MK48T08 & Disable Flash writes	D32-D8	16 KB	1, 7
$FFFCC000 - $FFFCFFFF	MK48T08 & Enable Flash writes	D32-D8	16 KB	1, 7
$FFFD0000 - $FFFEFFFF	Reserved	- -	128 KB	4

NOTES:
1. For a complete description of the register bits, refer to the data sheet for the specific chip. For a more detailed memory map, refer to the following detailed peripheral device memory maps.
2. The SCC is an 8-bit device located on an MCchip private data bus. Byte access is required.
3. Writes to the LCSR in the VMEchip2 must be 32 bits. LCSR writes of 8 or 16 bits terminate with a TEA signal. Writes to the GCSR may be 8, 16 or 32 bits. Reads to the LCSR and GCSR may be 8, 16 or 32 bits. Byte reads should be used to read the interrupt vector.
4. This area does not return an acknowledge signal. If the local bus timer is enabled, the access times out and is terminated by a TEA signal.
5. Size is approximate.
6. Port commands to the 82596CA must be written as two 16-bit writes: upper word first and lower word second.
7. Refer to the Flash and EPROM Interface section in the MCchip description in Chapter 3.
8. Not used.
9. To use this area, the ECC mezzanine board must be installed. If it is not installed, no acknowledge signal is returned; if the local bus timer is enabled, the access times out and is terminated by a TEA signal.

Detailed I/O Memory Maps

Tables 3-3 through 3-13 provide detailed memory maps for the VMEchip2, the MCchip, the MCECC memory controller chip, the Zilog Z85230, the Intel 82596CA controller, the NCR 53C710 controller, the IPIC chip, and the MK48T08 BBRAM/TOD Clock.

Table 3-3. VMEchip2 Memory Map (Sheet 1 of 3) 3-9/3-10

Table 3-3. VMEchip2 Memory Map (Sheet 2 of 3) 3-11 / 3-12

Table 3- 3. VMEchip2 Memory Map (Sheet 3 of 3)

VMEchip2 GCSR Base Address = $FFF40100

L	V	15 Bit Numbers 8	7 Bit Numbers 0														
0	0	CHIP REVISION								CHIP ID							
4	2	LM3	LM2	LM1	LM0	SIG3	SIG2	SIG1	SIG0	RST	ISF	BF	SCON	SYSFL	X	X	X
8	4	GENERAL PURPOSE CONTROL AND STATUS REGISTER 0															
C	6	GENERAL PURPOSE CONTROL AND STATUS REGISTER 1															
10	8	GENERAL PURPOSE CONTROL AND STATUS REGISTER 2															
14	A	GENERAL PURPOSE CONTROL AND STATUS REGISTER 3															
18	C	GENERAL PURPOSE CONTROL AND STATUS REGISTER 4															
1C	E	GENERAL PURPOSE CONTROL AND STATUS REGISTER 5															

NOTES: 1. L = Local bus offset

2. V = VMEbus offset

Table 3-4. MCchip Register Map

MCchip Base Address = $FFF42000

Offset	D31-D24	D23-D16	D15-D8	D7-D0
$00	MCchip ID	MCchip Revision	General Control	Interrupt Vector Base Register
$04	Tick Timer 1 Compare Register			
$08	Tick Timer 1 Counter Register			
$0C	Tick Timer 2 Compare Register			
$10	Tick Timer 2 Counter Register			
$14	LSB Prescaler Count Register	Prescaler Clock Adjust	Tick Timer 2 Control	Tick Timer 1 Control
$18	Tick Timer 4 Interrupt Control	Tick Timer 3 Interrupt Control	Tick Timer 2 Interrupt Control	Tick Timer 1 Interrupt Control
$1C	DRAM Parity Error Interrupt Control	SCC Interrupt Control	Tick Timer 4 Control	Tick Timer 3 Control
$20	DRAM Space Base Address Register		SRAM Space Base Address Register	
$24	DRAM Space Size	DRAM/SRAM Options	SRAM Space Size	(*Reserved*)
$28	LANC Error Status	(*Reserved*)	LANC Interrupt Control	LANC Bus Error Interrupt Control
$2C	SCSI Error Status	General Purpose Inputs	MVME162LX Version	SCSI Interrupt Control
$30	Tick Timer 3 Compare Register			
$34	Tick Timer 3 Counter Register			
$38	Tick Timer 4 Compare Register			
$3C	Tick Timer 4 Counter Register			
$40	Bus Clock	PROM Access Time Control	Flash Access Time Control	ABORT Switch Interrupt Control
$44	RESET Switch Control	Watchdog Timer Control	Access & Watchdog Time Base Select	(*Reserved*)
$48	DRAM Control	(*Reserved*)	MPU Status	(*Reserved*)
$4C	32-bit Prescaler Count Register			

Table 3-5. MCECC Internal Register Memory Map

MCECC Base Address = $FFF43000 (1st); $FFF43100 (2nd)

Register Offset	Register Name	Register Bit Names							
		D31	D30	D29	D28	D27	D26	D25	D24
$00	CHIP ID	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
$04	CHIP REVISION	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0
$08	MEM CONFIG			FSTRD	1	0	MSIZ2	MSIZ1	MSIZ0
$0C	DUMMY 0	0	0	0	0	0	0	0	0
$10	DUMMY 1	0	0	0	0	0	0	0	0
$14	BASE ADDRESS	BAD31	BAD30	BAD29	BAD28	BAD27	BAD26	BAD25	BAD24
$18	DRAM CONTRL	BAD23	BAD22	RWB5	SWAIT	RWB3	NCEIEN	NCEBEN	RAMEN
$1C	BCLK FREQ	BCK7	BCK6	BCK5	BCK4	BCK3	BCK2	BCK1	BCK0
$20	DATA CONTRL	0	0	DERC	ZFILL	RWCKB	0	0	0
$24	SCRUB CNTRL	RACODE	RADATA	HITDIS	SCRB	SCRBEN	0	SBEIEN	IDIS
$28	SCRUB PERIOD	SBPD15	SBPD14	SBPD13	SBPD12	SBPD11	SBPD10	SBPD9	SBPD8
$2C	SCRUB PERIOD	SBPD7	SBPD6	SBPD5	SBPD4	SBPD3	SBPD2	SBPD1	SBPD0
$30	CHIP PRESCALE	CPS7	CPS6	CPS5	CPS4	CPS3	CPS2	CPS1	CPS0
$34	SCRUB TIME ON/OFF	SRDIS	0	STON2	STON1	STON0	STOFF2	STOFF1	STOFF0
$38	SCRUB PRESCALE	0	0	SPS21	SPS20	SPS19	SPS18	SPS17	SPS16
$3C	SCRUB PRESCALE	SPS15	SPS14	SPS13	SPS12	SPS11	SPS10	SPS9	SPS8
$40	SCRUB PRESCALE	SPS7	SPS6	SPS5	SPS4	SPS3	SPS2	SPS1	SPS0
$44	SCRUB TIMER	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8
$48	SCRUB TIMER	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
$4C	SCRUB ADDR CNTRL	0	0	0	0	0	SAC26	SAC25	SAC24
$50	SCRUB ADDR CNTRL	SAC23	SAC22	SAC21	SAC20	SAC19	SAC18	SAC17	SAC16
$54	SCRUB ADDR CNTRL	SAC15	SAC14	SAC13	SAC12	SAC11	SAC10	SAC9	SAC8
$58	SCRUB ADDR CNTRL	SAC7	SAC6	SAC5	SAC4	0	0	0	0
$5C	ERROR LOGGER	ERRLOG	ERD	ESCRB	ERA	EALT	0	MBE	SBE
$60	ERROR ADDRESS	EA31	EA30	EA29	EA28	EA27	EA26	EA25	EA24
$64	ERROR ADDRESS	EA23	EA22	EA21	EA20	EA19	EA18	EA17	EA16
$68	ERROR ADDRESS	EA15	EA14	EA13	EA12	EA11	EA10	EA9	EA8
$6C	ERROR ADDRESS	EA7	EA6	EA5	EA4	0	0	0	0
$70	ERROR SYNDROME	S7	S6	S5	S4	S3	S2	S1	S0
$74	DEFAULTS1	WRHDIS	STATCOL	FSTRD	SELI1	SELI0	RSIZ2	RSIZ1	RSIZ0
$78	DEFAULTS2	FRC_OPN	XY_FLIP	REFDIS	TVECT	NOCACHE	RESST2	RESST1	RESST0

Table 3-6. Z85230 SCC Register Addresses

SCC	SCC Register	Address
SCC #1	Port B Control	$FFF45001
	Port B Data	$FFF45003
	Port A Control	$FFF45005
	Port A Data	$FFF45007
SCC #2	Port B Control	$FFF45801
	Port B Data	$FFF45803
	Port A Control	$FFF45805
	Port A Data	$FFF45807

Table 3-7. 82596CA Ethernet LAN Memory Map

	Data Bits			
Address	**D31**	**D16**	**D15**	**D0**
$FFF46000	Upper Command Word		Lower Command Word	
$FFF46004	MPU Channel Attention (CA)			

NOTES: 1. Refer to the MPU Port and MPU Channel Attention registers in the *MVME162 Embedded Controller Programmer's Reference Guide*.

2. After resetting, you must write the System Configuration Pointer to the command registers before writing to the MPU Channel Attention register. Writes to the System Configuration Pointer must be upper word first, lower word second.

Table 3-8. 53C710 SCSI Memory Map

53C710 Register Address Map	Base Address is $FFF47000				
Big Endian Mode					**SCRIPTs and Little Endian Mode**
00	SIEN	SDID	SCNTL1	SCNTL0	00
04	SOCL	SODL	SXFER	SCID	04
08	SBCL	SBDL	SIDL	SFBR	08
0C	SSTAT2	SSTAT1	SSTAT0	DSTAT	0C
10	DSA				10
14	CTEST3	CTEST2	CTEST1	CTEST0	14
18	CTEST7	CTEST6	CTEST5	CTEST4	18
1C	TEMP				1C
20	LCRC	CTEST8	ISTAT	DFIFO	20
24	DCMD	DBC			24
28	DNAD				28
2C	DSP				2C
30	DSPS				30
34	SCRATCH				34
38	DCNTL	DWT	DIEN	DMODE	38
3C	ADDER				3C

NOTE: Accesses may be 8-bit or 32-bit, but not 16-bit.

IPIC Overall Memory Map

The following memory map table includes all devices selected by the IPIC map decoder.

Note **The IPIC chip on the MVME162LX supports up to four IndustryPack (IP) interfaces, designated IP_a through IP_d. The MVME162LX itself accommodates two IPs: IP_a and IP_b. In the maps that follow, the segments applicable to IP_c and IP_d are not used in the MVME162LX.**

Table 3-9. IPIC Overall Memory Map

Address Range	Selected Device	Port Width	Size
Programmable	IP_a/IP_ab Memory Space	D32-D8	64 KB-16 MB
Programmable	IP_b Memory Space	D16-D8	64 KB-8 MB
Programmable	IP_c/IP_cd Memory Space	D32-D8	64 KB-16 MB
Programmable	IP_d Memory Space	D16-D8	64 KB-8 MB
$FFF58000-$FFF5807F	IP_a I/O Space	D16	128 B
$FFF58080-$FFF580BF	IP_a ID Space	D16	64 B
$FFF580C0-$FFF580FF	IP_a ID Space Repeated	D16	64 B
$FFF58100-$FFF5817F	IP_b I/O Space	D16	128 B
$FFF58180-$FFF581BF	IP_b ID Space	D16	64 B
$FFF581C0-$FFF581FF	IP_b ID Space Repeated	D16	64 B
$FFF58200-$FFF5827F	IP_c I/O Space	D16	128 B
$FFF58280-$FFF582BF	IP_c ID Space	D16	64 B
$FFF582C0-$FFF582FF	IP_c ID Space Repeated	D16	64 B
$FFF58300-$FFF5837F	IP_d I/O Space	D16	128 B
$FFF58380-$FFF583BF	IP_d ID Space	D16	64 B
$FFF583C0-$FFF583FF	IP_d ID Space Repeated	D16	64 B
$FFF58400-$FFF584FF	IP_ab I/O Space	D32-D16	256 B
$FFF58500-$FFF585FF	IP_cd I/O Space	D32-D16	256 B
$FFF58600-$FFF586FF	IP_ab I/O Space Repeated	D32-D16	256 B
$FFF58700-$FFF587FF	IP_cd I/O Space Repeated	D32-D16	256 B
$FFFBC000-$FFFBC01F	Control/Status Registers	D32-D8	32 B

Table 3-10 contains a summary of the IPIC CSR registers. The CSR registers can be accessed as bytes, words, or longwords; they should not be accessed as lines. They are shown in the table as bytes.

Table 3-10. IPIC Memory Map—Control and Status Registers

IPIC Base Address = $FFFBC000

Register Offset	Register Name	Register Bit Names							
		D7	D6	D5	D4	D3	D2	D1	D0
$00	CHIP ID	0	0	1	0	0	0	1	1
$01	CHIP REVISION	0	0	0	0	0	0	0	0
$02	RESERVED	0	0	0	0	0	0	0	0
$03	RESERVED	0	0	0	0	0	0	0	0
$04	IP_a MEM BASE UPPER	a_BASE31	a_BASE30	a_BASE29	a_BASE28	a_BASE27	a_BASE26	a_BASE25	a_BASE24
$05	IP_a MEM BASE LOWER	a_BASE23	a_BASE22	a_BASE21	a_BASE20	a_BASE19	a_BASE18	a_BASE17	a_BASE16
$06	IP_b MEM BASE UPPER	b_BASE31	b_BASE30	b_BASE29	b_BASE28	b_BASE27	b_BASE26	b_BASE25	b_BASE24
$07	IP_b MEM BASE LOWER	b_BASE23	b_BASE22	b_BASE21	b_BASE20	b_BASE19	b_BASE18	b_BASE17	b_BASE16
$08	IP_c MEM BASE UPPER	c_BASE31	c_BASE30	c_BASE29	c_BASE28	c_BASE27	c_BASE26	c_BASE25	c_BASE24
$09	IP_c MEM BASE LOWER	c_BASE23	c_BASE22	c_BASE21	c_BASE20	c_BASE19	c_BASE18	c_BASE17	c_BASE16
$0A	IP_d MEM BASE UPPER	d_BASE31	d_BASE30	d_BASE29	d_BASE28	d_BASE27	d_BASE26	d_BASE25	d_BASE24
$0B	IP_d MEM BASE LOWER	d_BASE23	d_BASE22	d_BASE21	d_BASE20	d_BASE19	d_BASE18	d_BASE17	d_BASE16
$0C	IP_a MEM SIZE	a_SIZE23	a_SIZE22	a_SIZE21	a_SIZE20	a_SIZE19	a_SIZE18	a_SIZE17	a_SIZE16
$0D	IP_b MEM SIZE	b_SIZE23	b_SIZE22	b_SIZE21	b_SIZE20	b_SIZE19	b_SIZE18	b_SIZE17	b_SIZE16
$0E	IP_c MEM SIZE	c_SIZE23	c_SIZE22	c_SIZE21	c_SIZE20	c_SIZE19	c_SIZE18	c_SIZE17	c_SIZE16
$0F	IP_d MEM SIZE	d_SIZE23	d_SIZE22	d_SIZE21	d_SIZE20	d_SIZE19	d_SIZE18	d_SIZE17	d_SIZE16
$10	IP_a INT0 CONTROL	a0_PLTY	a0_E/L*	a0_INT	a0_IEN	a0_ICLR	a0_IL2	a0_IL1	a0_IL0
$11	IP_a INT1 CONTROL	a1_PLTY	a1_E/L*	a1_INT	a1_IEN	a1_ICLR	a1_IL2	a1_IL1	a1_IL0
$12	IP_b INT0 CONTROL	b0_PLTY	b0_E/L*	b0_INT	b0_IEN	b0_ICLR	b0_IL2	b0_IL1	b0_IL0
$13	IP_b INT1 CONTROL	b1_PLTY	b1_E/L*	b1_INT	b1_IEN	b1_ICLR	b1_IL2	b1_IL1	b1_IL0
$14	IP_c INT0 CONTROL	c0_PLTY	c0_E/L*	c0_INT	c0_IEN	c0_ICLR	c0_IL2	c0_IL1	c0_IL0
$15	IP_c INT1 CONTROL	c1_PLTY	c1_E/L*	c1_INT	c1_IEN	c1_ICLR	c1_IL2	c1_IL1	c1_IL0
$16	IP_d INT0 CONTROL	d0_PLTY	d0_E/L*	d0_INT	d0_IEN	d0_ICLR	d0_IL2	d0_IL1	d0_IL0
$17	IP_d INT1 CONTROL	d1_PLTY	d1_E/L*	d1_INT	d1_IEN	d1_ICLR	d1_IL2	d1_IL1	d1_IL0
$18	IP_a GENERAL CONTROL	a_ERR	0	a_RT1	a_RT0	a_WIDTH1	a_WIDTH0	0	a_MEN
$19	IP_a GENERAL CONTROL	b_ERR	0	b_RT1	b_RT0	b_WIDTH1	b_WIDTH0	0	b_MEN

Table 3-10. IPIC Memory Map—Control and Status Registers (Continued)

IPIC Base Address = $FFFBC000

Register Offset	Register Name	Register Bit Names							
		D7	D6	D5	D4	D3	D2	D1	D0
$1A	IP_b GENERAL CONTROL	c_ERR	0	c_RT1	c_RT0	c_WIDTH1	c_WIDTH0	0	c_MEN
$1B	IP_b GENERAL CONTROL	d_ERR	0	d_RT1	d_RT0	d_WIDTH1	d_WIDTH0	0	d_MEN
$1C	RESERVED	0	0	0	0	0	0	0	0
$1D	RESERVED	0	0	0	0	0	0	0	0
$1E	RESERVED	0	0	0	0	0	0	0	0
$1F	IP RESET	0	0	0	0	0	0	0	RES

Table 3-11. MK48T08 BBRAM/TOD Clock Memory Map

Address Range	Description	Size (Bytes)
$FFFC0000 - $FFFC0FFF	User Area	4096
$FFFC1000 - $FFFC10FF	Networking Area	256
$FFFC1100 - $FFFC16F7	Operating System Area	1528
$FFFC16F8 - $FFFC1EF7	Debugger Area	2048
$FFFC1EF8 - $FFFC1FF7	Configuration Area	256
$FFFC1FF8 - $FFFC1FFF	TOD Clock	8

Table 3-12. BBRAM Configuration Area Memory Map

Address Range	Description	Size (Bytes)
$FFFC1EF8 - $FFFC1EFB	Version	4
$FFFC1EFC - $FFFC1F07	Serial Number	12
$FFFC1F08 - $FFFC1F17	Board ID	16
$FFFC1F18 - $FFFC1F27	PWA	16
$FFFC1F28 - $FFFC1F2B	Speed	4
$FFFC1F2C - $FFFC1F31	Ethernet Address	6
$FFFC1F32 - $FFFC1F33	Reserved	2
$FFFC1F34 - $FFFC1F35	Local SCSI ID	2

Table 3-12. BBRAM Configuration Area Memory Map (Continued)

Address Range	Description	Size (Bytes)
$FFFC1F36 - $FFFC1F3D	Memory Mezzanine PWB	8
$FFFC1F3E - $FFFC1F45	Memory Mezzanine Serial Number	8
$FFFC1F46 - $FFFC1F4D	Serial Port 2 Personality PWB	8
$FFFC1F4E - $FFFC1F55	Serial Port 2 Personality Serial No.	8
$FFFC1F56 - $FFFC1F5D	IP_a Board ID	8
$FFFC1F5E - $FFFC1F65	IP_a Board Serial Number	8
$FFFC1F66 - $FFFC1F6D	IP_a Board PWB	8
$FFFC1F6E - $FFFC1F75	IP_b Board ID	8
$FFFC1F76 - $FFFC1F7D	IP_b Board Serial Number	8
$FFFC1F7E - $FFFC1F85	IP_b Board PWB	8
$FFFC1F86 - $FFFC1F8D	IP_c Board ID	8
$FFFC1F8E - $FFFC1F95	IP_c Board Serial Number	8
$FFFC1F96 - $FFFC1F9D	IP_c Board PWB	8
$FFFC1F9E - $FFFC1FA5	IP_d Board ID	8
$FFFC1FA6 - $FFFC1FAD	IP_d Board Serial Number	8
$FFFC1FAE - $FFFC1FB5	IP_d Board PWB	8
$FFFC1FB6 - $FFFC1FF6	Reserved	65
$FFFC1FF7	Checksum	1

Table 3-13. TOD Clock Memory Map

Address	Data Bits								Function	
	D7	D6	D5	D4	D3	D2	D1	D0		
$FFFC1FF8	W	R	S	--	--	--	--	--	CONTROL	
$FFFC1FF9	ST	--	--	--	--	--	--	--	SECONDS	00
$FFFC1FFA	x	--	--	--	--	--	--	--	MINUTES	00
$FFFC1FFB	x	x	--	--	--	--	--	--	HOUR	00
$FFFC1FFC	x	FT	x	x	x	--	--	--	DAY	01
$FFFC1FFD	x	x	--	--	--	--	--	--	DATE	01
$FFFC1FFE	x	x	x	--	--	--	--	--	MONTH	01
$FFFC1FFF	--	--	--	--	--	--	--	--	YEAR	00

NOTES: W = Write Bit R = Read Bit S = Signbit

ST = Stop Bit FT = Frequency Test x = Unused

BBRAM, TOD Clock Memory Map

The MK48T08 BBRAM (also called Non-Volatile RAM or NVRAM) is divided into six areas as shown in Table 3-11. The first five areas are defined by software, while the sixth area, the time-of-day (TOD) clock, is defined by the chip hardware. The first area is reserved for user data. The second area is used by Motorola networking software. The third area is used by the operating system. The fourth area is used by the MVME162LX board debugger (MVME162Bug). The fifth area, detailed in Table 3-12, is the configuration area. The sixth area, the TOD clock, detailed in Table 3-13, is defined by the chip hardware.

The data structure of the configuration bytes starts at $FFFC1EF8 and is as follows.

```
struct brdi_cnfg {
       char         version[4];
       char         serial[12];
       char         id[16];
       char         pwa[16];
       char         speed[4];
       char         ethernet[6];
       char         fill[2];
       char         lscsiid[2];
       char         mem_pwb[8];
       char         mem_serial[8];
       char         port2_pwb[8];
       char         port2_serial[8];
       char         ipa_brdid[8];
       char         ipa_serial[8];
       char         ipa_pwb[8];
       char         ipb_brdid[8];
       char         ipb_serial[8];
       char         ipb_pwb[8];
       char         ipc_brdid[8];
       char         ipc_serial[8];
       char         ipc_pwb[8];
       char         ipd_brdid[8];
       char         ipd_serial[8];
       char         ipd_pwb[8];
       char         reserved[65];
       char         cksum[1]; }
```

The fields are defined as follows:

1. Four bytes are reserved for the revision or version of this structure. This revision is stored in ASCII format, with the first two bytes being the major version numbers and the last two bytes being the minor version numbers. For example, if the version of this structure is 1.0, this field contains:

   `0100`

2. Twelve bytes are reserved for the serial number of the board in ASCII format. For example, this field could contain:

   `000000470476`

3. Sixteen bytes are reserved for the board ID in ASCII format. For example, for an MVME162LX board with MC68040, SCSI, Ethernet, 4MB DRAM, and 128 KB SRAM, this field contains:

   `MVME162-223` (The 11 characters are followed by five blanks.)

4. Sixteen bytes are reserved for the printed wiring assembly (PWA) number assigned to this board in ASCII format. This includes the `01-W` prefix. This is for the main logic board if more than one board is required for a set. Additional boards in a set are defined by a structure for that set. For example, for an MVME162LX board with MC68040, SCSI, Ethernet, 4MB DRAM, and 128 KB SRAM at revision A, the PWA field contains:

   `01-W3866B01A` (The 12 characters are followed by four blanks.)

5. Four bytes contain the speed of the board in MHz. The first two bytes are the whole number of MHz and the second two bytes are fractions of MHz. For example, for a 25.00 MHz board, this field contains:

   `2500`

6. Six bytes are reserved for the Ethernet address. The address is stored in hexadecimal format. (Refer to the detailed description in Chapter 4.) If the board does not support Ethernet, this field is filled with zeros.

7. These two bytes are reserved.

8. Two bytes are reserved for the local SCSI ID. The SCSI ID is stored in ASCII format.

9. Eight bytes are reserved for the printed wiring board (PWB) number assigned to the memory mezzanine board in ASCII format. This does *not* include the `01-W` prefix. For example, for a 4MB parity mezzanine at revision A, the PWB field contains:

   `3913B01A`

10. Eight bytes are reserved for the serial number assigned to the memory mezzanine board in ASCII format.

11. Eight bytes are reserved for the printed wiring board (PWB) number assigned to the serial port 2 personality board in ASCII format.
12. Eight bytes are reserved for the serial number assigned to the serial port 2 personality board in ASCII format.
13. Eight bytes are reserved for the board identifier, in ASCII format, assigned to the optional first IndustryPack a.
14. Eight bytes are reserved for the serial number, in ASCII format, assigned to the optional first IndustryPack a.
15. Eight bytes are reserved for the printed wiring board (PWB) number assigned to the optional first IndustryPack a.
16. Eight bytes are reserved for the board identifier, in ASCII format, assigned to the optional second IndustryPack b.
17. Eight bytes are reserved for the serial number, in ASCII format, assigned to the optional second IndustryPack b.
18. Eight bytes are reserved for the printed wiring board (PWB) number assigned to the optional second IndustryPack b.
19. Eight bytes are reserved for the board identifier, in ASCII format, assigned to the optional third IndustryPack c.
20. Eight bytes are reserved for the serial number, in ASCII format, assigned to the optional third IndustryPack c.
21. Eight bytes are reserved for the printed wiring board (PWB) number assigned to the optional third IndustryPack c.
22. Eight bytes are reserved for the board identifier, in ASCII format, assigned to the optional fourth IndustryPack d.
23. Eight bytes are reserved for the serial number, in ASCII format, assigned to the optional fourth IndustryPack d.
24. Eight bytes are reserved for the printed wiring board (PWB) number assigned to the optional fourth IndustryPack d.
25. Growth space (65 bytes) is reserved. This pads the structure to an even 256 bytes.
26. The final one byte of the area is reserved for a checksum (as defined in the *MVME162Bug Debugging Package User's Manual*) for security and data integrity of the configuration area of the NVRAM. This data is stored in hexadecimal format.

Interrupt Acknowledge Map

The local bus distinguishes interrupt acknowledge cycles from other cycles by placing the binary value %11 on TT1-TT0. It also specifies the level that is being acknowledged using TM2-TM0. The interrupt handler selects which device within that level is being acknowledged.

VMEbus Memory Map

This section describes the mapping of local resources as viewed by VMEbus masters.

VMEbus Accesses to the Local Bus

The VMEchip2 includes a user-programmable map decoder for the VMEbus-to-local-bus interface. The map decoder allows you to program the starting and ending address and the modifiers the MVME162LX responds to.

VMEbus Short I/O Memory Map

The VMEchip2 includes a user-programmable map decoder for the GCSR. The GCSR map decoder allows you to program the starting address of the GCSR in the VMEbus short I/O space.

Software Initialization

Most functions that have been done with switches or jumpers on other modules are done by setting control registers on the MVME162LX. At power-up or reset, the PROMs that contain the 162Bug debugging package set up the default values of many of these registers.

Specific programming details may be determined by study of the *M68040 Microprocessor User's Manual*. Then check the details of all the MVME162LX onboard registers as given in the *MVME162LX Embedded Controller Programmer's Reference Guide*.

Multi-MPU Programming Considerations

Good programming practice dictates that only one MPU at a time have control of the MVME162LX control registers. Of particular note are:

- ❏ Registers that modify the address map
- ❏ Registers that require two cycles to access
- ❏ VMEbus interrupt request registers

Local Reset Operation

Local reset (LRST) is a subset of system reset (SRST). Local reset can be generated five ways:

- ❑ Expiration of the watchdog timer
- ❑ Pressing the front panel RESET switch (if the system controller function is disabled)
- ❑ By asserting a bit in the board control register in the GCSR
- ❑ By SYSRESET*
- ❑ By powerup reset.

Note **The GCSR allows a VMEbus master to reset the local bus. This feature is very dangerous and should be used with caution. The local reset feature is a partial system reset, not a complete system reset such as powerup reset or SYSRESET*. When the local bus reset signal is asserted, a local bus cycle may be aborted. The VMEchip2 is connected to both the local bus and the VMEbus and if the aborted cycle is bound for the VMEbus, erratic operation may result. Communications between the local processor and a VMEbus master should use interrupts or mailbox locations; reset should not be used in normal communications. Reset should be used only when the local processor is halted or the local bus is hung and reset is the last resort.**

Any VMEbus access to the MVME162LX while it is in the reset state is ignored. If a global bus timer is enabled, a bus error is generated.

FUNCTIONAL DESCRIPTION 4

Introduction

This chapter describes the MVME162LX Embedded Controller on a block diagram level. The *Functional Description* provides an overview of the MVME162LX, followed by a detailed description of several blocks of MVME162LX circuitry. Figure 4-1 shows a block diagram of the MVME162LX main module. Figures 4-2 through 4-4 show block diagrams of the parity DRAM, ECC DRAM, and SRAM modules.

Descriptions of other MVME162LX blocks, including programmable registers in the ASICs and peripheral chips, are given in the *MVME162LX Embedded Controller Programmer's Reference Guide*. Refer to it for the rest of the functional description of the MVME162LX.

MVME162LX Functional Description

The MVME162LX is a high-functionality VMEbus single board computer designed around the MC68040/MC68LC040 chip. It has 1MB, 4MB, or 16MB of DRAM and four serial ports. Options include an SCSI mass storage interface, a LAN Ethernet transceiver interface, two MVIP IndustryPack interfaces, and 1 MB Flash memory.

Data Bus Structure

The local data bus on the MVME162LX is a 32-bit synchronous bus that is based on the MC68040 bus, and which supports burst transfers and snooping. The various local bus master and slave devices use the local bus to communicate. The local bus is arbitrated by priority type arbiter and the priority of the local bus masters from highest to lowest is: 82596CA LAN, memory mezzanine, NCR 53C710 SCSI, VMEbus, and MPU. Generally speaking, any master can access any slave; however, not all combinations pass the common sense test. Refer to the *MVME162LX Embedded Controller Programmer's Reference Guide* and to the user's guide for each device to determine its port size, data bus connection, and any restrictions that apply when accessing the device.

MC68040/MC68LC040 MPU

The MVME162LX is equipped with an MC68040 or MC68LC040 microprocessor. The MC68040/MC68LC040 have on-chip instruction and data caches; the MC68040 also provides a floating-point coprocessor. Refer to the *M68040 Microprocessor User's Manual* for more information.

EPROM and Flash Memory

The MVME162LX can be ordered with 1 MB of Flash memory and four EPROM sockets ready for the installation of the EPROMs, which may be ordered separately. Flash memory is a single Intel 28F008SA device organized in a 1Mbit x 8 configuration. The EPROM locations are standard JEDEC 32-pin DIP sockets accommodating four jumper-selectable densities (128 Kbit x 8; 256 Kbit X 8; 512 Kbit x 8; 1 Mbit x8). A jumper setting (GPIO3, pins 7-8 on J11) allows reset code to be fetched either from Flash memory (GPIO3 installed) or from EPROMs (GPIO3 removed).

SRAM

The MVME162LX provides 128 KB of 32-bit-wide onboard static RAM in a single non-interleaved architecture with onboard battery backup. As an option, a 2 MB SRAM mezzanine module with its own battery backup is available as well. When installed, the SRAM mezzanine disables the onboard SRAM to eliminate conflicts. Further details on SRAM configuration and specifics on SRAM performance can be found in the section on the SRAM Memory Controller in the MCchip Programming Model in the *MVME162LX Embedded Controller Programmer's Reference Guide*. The SRAM arrays are not parity protected.

The battery backup function for the onboard SRAM and the mezzanine SRAM is provided by a Dallas DS1210S device that supports primary and secondary power sources. In the event of a main board power failure, the DS1210S checks power sources and switches to the source with the higher voltage.

If the voltage of the backup source is less than two volts, the DS1210S blocks the second memory cycle; this allows software to provide an early warning to avoid data loss. Because the second access may be blocked during a power failure, software should do at least two accesses before relying on the data.

The MVME162LX provides jumpers (on J13) that allow either power source of the DS1210S to be connected to the VMEbus +5V STDBY pin or to one cell of the onboard battery. For example, the primary system backup source may be

a battery connected to the VMEbus +5V STDBY pin and the secondary source may be the onboard battery. If the system source should fail or the board is removed from the chassis, the onboard battery takes over.

Caution **For proper operation of the onboard SRAM, some jumper combination must be installed on the respective Backup Power Source Select Header. If one of the jumpers is used to select the battery, the battery must be installed on the MVME162LX. The SRAM may malfunction if inputs to the DS1210S are left unconnected.**

The SRAM is controlled by the MCchip, and the access time is programmable. Refer to the MCchip description in the *MVME162LX Embedded Controller Programmer's Reference Guide* for more detail.

About the Batteries

The power source for the onboard SRAM is a RAYOVAC FB1225 battery with two BR1225 type lithium cells which is socketed for easy removal and replacement. The power source for the mezzanine SRAM is a Sanyo CR2430 battery. Small capacitors are provided so that the batteries can be quickly replaced without data loss.

The lifetime of the batteries is very dependent on the ambient temperature of the board and the power-on duty cycle. The lithium batteries supplied on the MVME162LX and on the SRAM mezzanine module should provide at least two years of backup time with the board powered off and with an ambient temperature of 40° C. If the power-on duty cycle is 50% (the board is powered on half of the time), the battery lifetime is four years. At lower ambient temperatures, the backup time is significantly longer and may approach the shelf life of the battery.

When a board is stored, the battery should be disconnected to prolong battery life. This is especially important at high ambient temperatures. The MVME162LX is shipped with the batteries disconnected (i.e., with VMEbus +5V standby voltage selected as both primary and secondary power source). If you intend to use the battery as a power source, whether primary or secondary, it is necessary to reconfigure the jumpers on J20 before installing the module. Refer to *SRAM Backup Power Source Select Header J20* in Chapter 2 for available jumper configurations

The power leads from the battery are exposed on the solder side of the board. The board should not be placed on a conductive surface or stored in a conductive bag unless the battery is removed.

Caution **Lithium batteries incorporate inflammable materials such as lithium and organic solvents. If lithium batteries are mistreated or handled incorrectly, they may burst open and ignite, possible resulting in injury and/or fire. When dealing with lithium batteries, carefully follow the precautions listed below in order to prevent accidents.**

- ❏ Do not short-circuit.
- ❏ Do not disassemble, deform, or apply excessive pressure.
- ❏ Do not heat or incinerate.
- ❏ Do not apply solder directly.
- ❏ Do not use different models, or mix new and old batteries together.
- ❏ Do not charge.
- ❏ Always check proper polarity.

To remove the battery from the module, carefully pull the battery from the socket.

Before installing a new battery, ensure that the battery pins are clean. Note the battery polarity and press the battery into the socket. When the battery is in the socket, no soldering is required.

DRAM

The MVME162LX offers three DRAM options: either 1 MB or 4 MB shared DRAM with programmable parity on a mezzanine module, or 16 MB ECC DRAM on a mezzanine board. The DRAM architecture is non-interleaved for 1MB and interleaved for 4MB. Parity protection can be enabled with interrupts or bus exception when a parity error is detected. DRAM performance is specified in the section on the DRAM Memory Controller in the MCchip Programming Model in *MVME162LX Embedded Controller Programmer's Reference Guide*.

The DRAM map decoder can be programmed to accommodate different base address(es) and sizes of mezzanine boards. The onboard DRAM is disabled by a local bus reset and must be programmed before the DRAM can be accessed. Refer to the MCchip and MCECC descriptions in the *MVME162LX Embedded Controller Programmer's Reference Guide* for detailed programming information.

Most DRAM devices require some number of access cycles before the DRAMs are fully operational. Normally this requirement is met by the onboard refresh circuitry and normal DRAM initialization. However, software should insure a minimum of 10 initialization cycles are performed to each bank of RAM.

Battery Backed Up RAM and Clock

An MK48T08 RAM and clock chip is used on the MVME162LX. This chip provides a time-of-day clock, oscillator, crystal, power failure detection, memory write protection, 8 KB of RAM, and a battery in one 28-pin package. The clock provides seconds, minutes, hours, day, date, month, and year in BCD 24-hour format. Corrections for 28-, 29- (leap year), and 30-day months are automatically made. No interrupts are generated by the clock. Although the MK48T08 is an 8- bit device, the interface provided by the MCchip supports 8-, 16-, and 32-bit accesses to the MK48T08. Refer to the MCchip description in Chapter 3 and to the MK48T08 data sheet for detailed programming and battery life information.

VMEbus Interface and VMEchip2

The VMEchip2 provides:

- ❏ The local-bus-to-VMEbus interface
- ❏ The VMEbus-to-local-bus interface
- ❏ The DMA controller functions of the local VMEbus

The VMEchip2 can also provide the VMEbus system controller functions. Refer to the *MVME162LX Embedded Controller Programmer's Reference Guide* for detailed programming information.

Note that the ABORT switch logic in the VMEchip2 is not used. The GPI inputs to the VMEchip2 which are located at $FFF40088 bits 7-0 are not used. The ABORT switch interrupt is integrated into the MCchip ASIC at location $FFF42043. The GPI inputs are integrated into the MCchip ASIC at location $FFF4202C bits 23-16.

I/O Interfaces

The MVME162LX provides onboard I/O for many system applications. The I/O functions include serial ports and optional interfaces for IndustryPack (IP) modules, LAN Ethernet transceivers, and SCSI mass storage devices.

Serial Communications Interface

The MVME162LX uses two Zilog Z85230 serial port controllers to implement the four serial communications interfaces. Each interface supports CTS, DCD, RTS, and DTR control signals as well as the TXD and RXD transmit/receive data signals. Because the serial clocks are omitted in the MVME162LX implementation, serial communications are strictly asynchronous. The MVME162LX hardware supports serial baud rates of 110 B/sec to 38.4 KB/sec.

The Z85230 supplies an interrupt vector during interrupt acknowledge cycles. The vector is modified within the Z85230 according to the interrupt source. Interrupt request levels are programmed via the MCchip. Refer to the Z85230 data sheet listed in Chapter 1 and to the MCchip Programming Model in the *MVME162LX Embedded Controller Programmer's Reference Guide* for further information.

The Z85230s are interfaced as DTE (data terminal equipment) with EIA-232-D signal levels. The four serial ports are routed to four RJ45 telephone connectors on the MVME162LX front panel.

IndustryPack (IP) Interfaces

The IPIC ASIC on the MVME162LX supports up to four IndustryPack (IP) interfaces. The MVME162LX itself accommodates two IPs; these are accessible from the front panel. Refer to the IPIC Programming Model in the *MVME162LX Embedded Controller Programmer's Reference Guide* for details of the IP interface.

Ethernet Interface

The Intel 82596CA LAN controller is used to implement the Ethernet transceiver interface. The 82596CA accesses local RAM, using DMA operations to perform its normal functions. Because the 82596CA has small internal buffers and the VMEbus has an undefined latency period, buffer overrun may occur if the DMA is programmed to access the VMEbus. Therefore, the 82596CA should not be programmed to access the VMEbus.

Every MVME162LX is assigned an Ethernet station address. The address is $08003E2*xxxxx*, where *xxxxx* is the unique 5-nibble number assigned to the board (i.e., every MVME162LX has a different value for *xxxxx*).

Each MVME162LX has an Ethernet station address displayed on a label attached to backplane connector P2. In addition, the six bytes including the Ethernet station address are stored in the BBRAM configuration area. That is, 08003E2*xxxxx* is stored in the BBRAM. At an address of $FFFC1F2C, the upper four bytes (08003E2*x*) can be read. At an address of $FFFC1F30, the lower two

bytes (*xxxx*) can be read. Refer to the BBRAM/TOD Clock memory map description in Chapter 3. The MVME162LX debugger has the capability to retrieve or set the Ethernet station address.

If the data in the BBRAM is lost, the user should use the number on the label on backplane connector P2 to restore it.

The Ethernet transceiver interface is located on the MVME162LX main module. An industry-standard DB15 connector is located on the MVME162LX front panel.

The MCchip provides support functions for the 82596CA. Refer to the 82596CA user's guide and to the *MVME162LX Embedded Controller Programmer's Reference Guide* for detailed programming information.

SCSI Interface

The MVME162LX supports mass storage subsystems through the industry-standard SCSI bus. These subsystems may include hard and floppy disk drives, streaming tape drives, and other mass storage devices. The SCSI interface is implemented using the NCR 53C710 SCSI I/O controller.

Support functions for the NCR 53C710 are provided by the MCchip. Refer to the NCR 53C710 user's guide and to the *MVME162LX Embedded Controller Programmer's Reference Guide* for detailed programming information.

SCSI Termination

The individual configuring the system must ensure that the SCSI bus is properly terminated at both ends.

The MVME162LX main module provides terminators for the SCSI bus. The SCSI terminators are enabled/disabled by a jumper on header J14. If the SCSI bus ends at the MVME162LX module, then a jumper must be installed between J14 pins 1 and 2.

The MVME162LX provides +5 Vdc to the SCSI bus TERMPWR signal through fuse F4, located near J7. The FUSES LED (part of DS2) on the MVME162LX front panel monitors the SCSI bus TERMPWR signal in addition to LAN power; with the MVME162LX connected to an SCSI bus, the FUSES LED lights when SCSI terminator power is present.

Because any device on the SCSI bus can provide TERMPWR, the FUSES LED does not directly indicate the condition of the fuse. If the LED is not illuminated during SCSI bus operation, however, the fuse should be checked.

Local Resources

The MVME162LX includes many resources for the local processor. These include tick timers, software programmable hardware interrupts, watchdog timer, and local bus timeout.

Programmable Tick Timers

Four 32-bit programmable tick timers with 1 µs resolution are provided in the MCchip and two 32-bit programmable tick timers are provided in the optional VMEchip2. The tick timers can be programmed to generate periodic interrupts to the processor. Refer to the MCchip and VMEchip2 descriptions in the *MVME162LX Embedded Controller Programmer's Reference Guide* for detailed programming information.

Watchdog Timer

A watchdog timer is provided in both the MCchip and the optional VMEchip2. The timers operate independently but in parallel. When the watchdog timers are enabled, they must be reset by software within the programmed time or they will time out. The watchdog timers can be programmed to generate a SYSRESET signal, local reset signal, or board fail signal if they time out. Refer to the VMEchip2 and MCchip descriptions in the *MVME162LX Embedded Controller Programmer's Reference Guide* for detailed programming information.

Software-Programmable Hardware Interrupts

Eight software-programmable hardware interrupts are provided by the VMEchip2. These interrupts allow software to create a hardware interrupt. Refer to the VMEchip2 description in the *MVME162LX Embedded Controller Programmer's Reference Guide* for detailed programming information.

Local Bus Timeout

The MVME162LX provides timeout functions in the VMEchip2 and the MCchip for the local bus. When the timer is enabled and a local bus access times out, a Transfer Error Acknowledge (TEA) signal is sent to the local bus master. The timeout value is selectable by software for 8 µsec, 64 µsec, 256 µsec, or infinity. The local bus timer does not operate during VMEbus bound cycles. VMEbus bound cycles are timed by the VMEbus access timer and the VMEbus global timer. Refer to the VMEchip2 and MCchip descriptions in the *MVME162LX Embedded Controller Programmer's Reference Guide* for detailed programming information.

The MCchip also provides local bus timeout logic for MVME162LXs without the optional VMEbus interface (i.e., without the VMEchip2).

Timing Performance

This section provides performance information for the MVME162LX. The MVME162LX is designed to operate at 25 MHz.

Local Bus to DRAM/SRAM Cycle Times

The ECC DRAM, parity DRAM, and SRAM base address are programmable. The parity DRAM device size is also programmable. The DRAM controller assumes an interleaved architecture if the DRAM size requires eight physical devices (that is, when memory array size is 4MB and DRAM technology is 4 Mbits per device).

Parity checking and parity exception action are also programmable. The parity DRAM array size and device size are initialized in the DRAM Space Size Register.

Table 4-1. DRAM/SRAM Performance

	Random Read	Random Write	Burst Read	Burst Read
ECC DRAM (FSTRD=1)	4	2	4-1-1-1	2-1-1-1
ECC DRAM (FSTRD=0)	5	2	5-1-1-1	2-1-1-1
1 MB Parity DRAM	4	3	4-2-2-2	3-2-2-2
4 MB Parity DRAM	4	3	4-1-1-1	3-2-2-2
SRAM	5	5	5-3-3-3	5-3-3-3

NOTE: FSTRD (bit 29 in the MCECC internal registers) is located at $FFF43074. Its default value is 0.

EPROM/Flash Cycle Times

The EPROM/Flash cycle time is programmable from 3 to 10 bus clocks/byte (4 bytes = 12 to 40). (The actual cycle time may vary depending on the device speed.) The data transfers are 32 bits wide. Refer to the *MVME162LX Embedded Controller Programmer's Reference Guide*.

SCSI Transfers

The MVME162LX includes a SCSI mass storage bus interface with DMA controller. The SCSI DMA controller uses a FIFO buffer to interface the 8-bit SCSI bus to the 32-bit local bus. The FIFO buffer allows the SCSI DMA controller to efficiently transfer data to the local bus in four longword bursts.

This reduces local bus usage by the SCSI device. Refer to the MCchip Programming Model in *the MVME162LX Embedded Controller Programmer's Reference Guide*.

The transfer rate of the DMA controller is 44MB/sec at 25 MHz with parity off and interleaved DRAM and read cycles. Assuming a continuous transfer rate of 5MB/sec on the SCSI bus, 12% of the local bus bandwidth is used by transfers from the SCSI bus.

LAN DMA Transfers

The MVME162LX includes a LAN interface with DMA controller. The LAN DMA controller uses a FIFO buffer to interface the serial LAN bus to the 32-bit local bus. The FIFO buffer allows the LAN DMA controller to efficiently transfer data to the local bus.

The LAN DMA controller does not use burst transfers since the 82596CA does not execute MC68040 compatible burst cycles. Parity DRAM write cycles require 3 clock cycles; read cycles require 5 clock cycles with parity off and 6 clock cycles with parity on.

The transfer rate of the LAN DMA controller is 20MB/sec at 25 MHz with parity off. Assuming a continuous transfer rate of 1MB/sec on the LAN bus, 5% of the local bus bandwidth is used by transfers from the LAN bus.

Remote Status and Control

The remote status and control connector, J2, is a 20-pin connector located behind the front panel of the MVME162LX. It provides system designers with flexibility in accessing critical indicator and reset functions. This allows a system designer to construct a RESET/ABORT/LED panel that can be located remotely from the MVME162LX.

In addition to providing an LED display and access to the RESET and ABORT switches, this connector also includes two general-purpose TTL-level I/O pins and one general-purpose interrupt pin which can also function as a trigger input. The interrupt pin is level programmable.

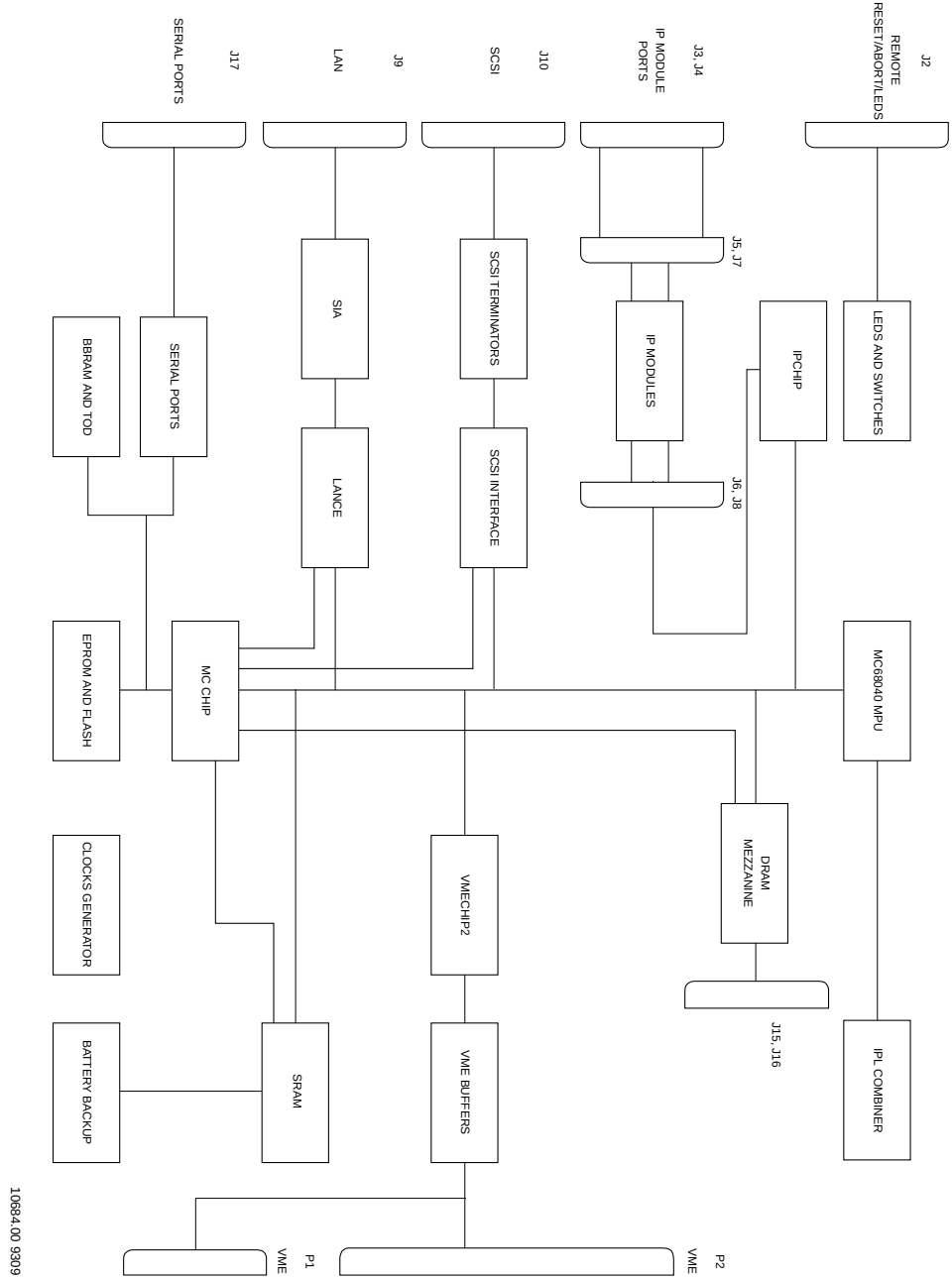


Figure 4-1. MVME162LX Main Module Block Diagram

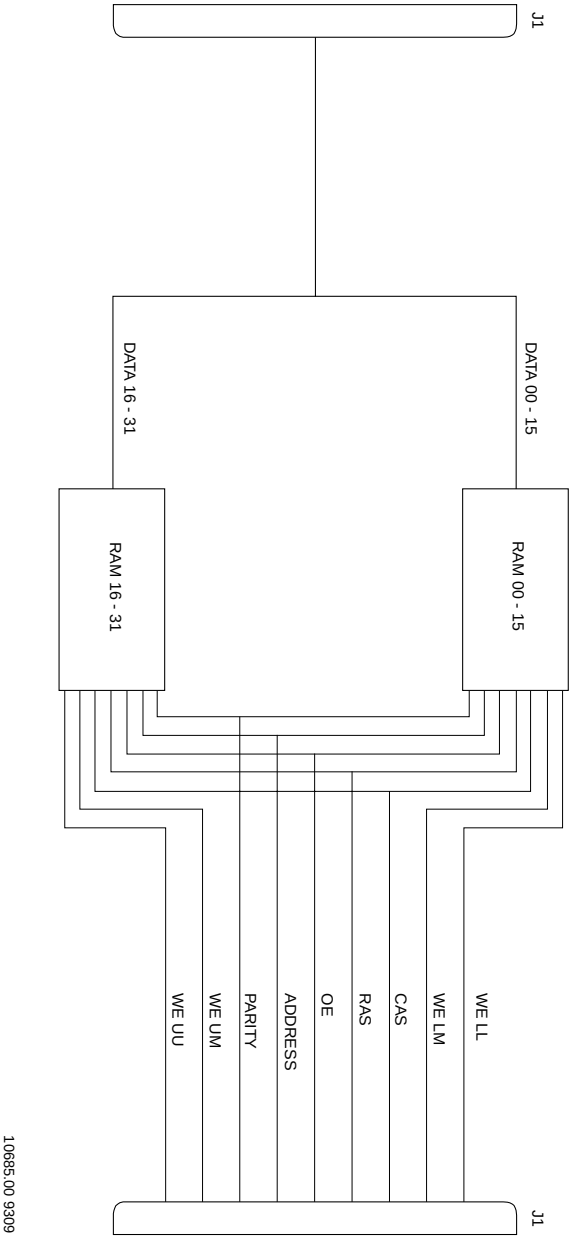


Figure 4-2. Parity DRAM Mezzanine Module Block Diagram

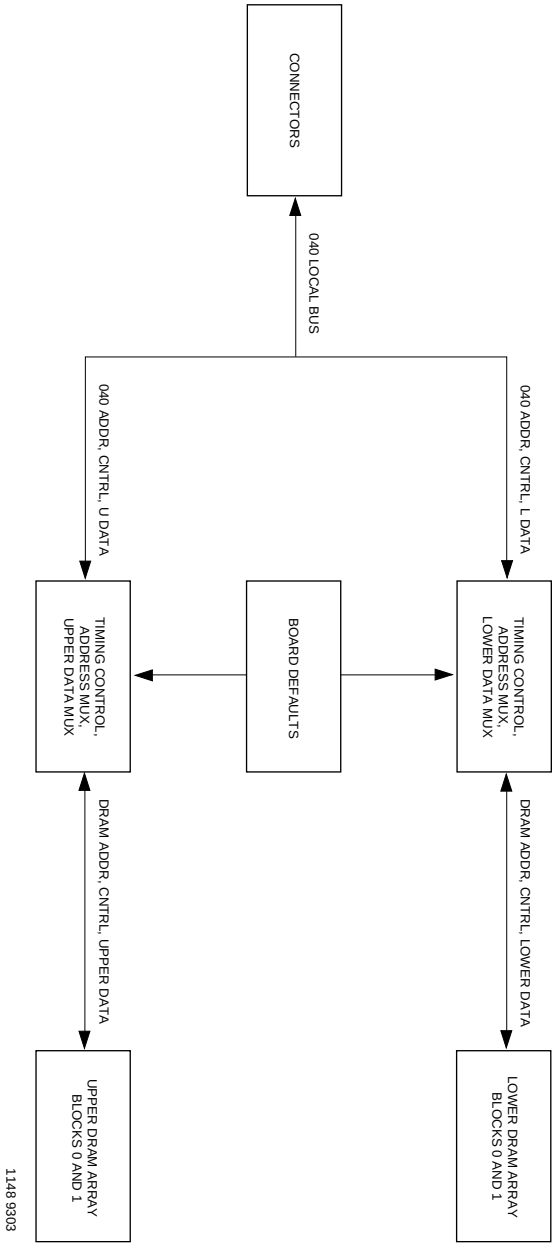


Figure 4-3. ECC DRAM Mezzanine Module Block Diagram

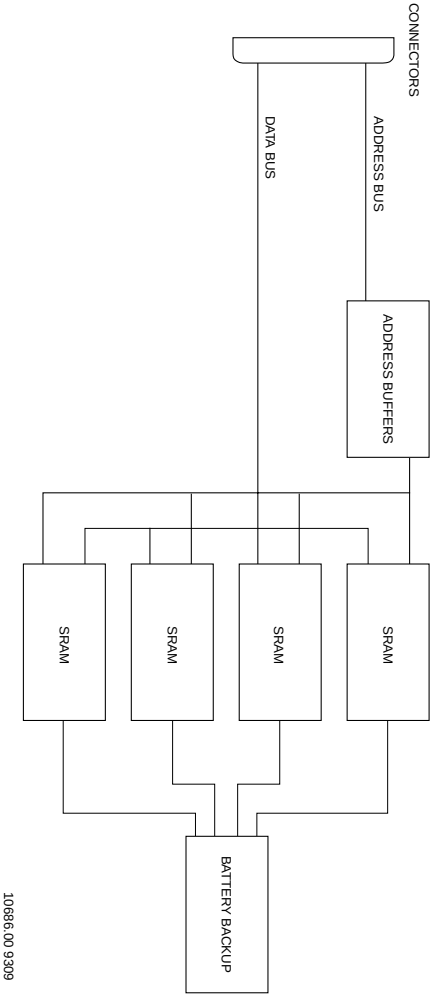


Figure 4-4. SRAM Mezzanine Module Block Diagram

EIA-232-D INTERCONNECTIONS

A

Connector J17 houses the four RJ45 sockets on the MVME162LX front panel which provide the serial interface connections. Table A-1 lists the pin numbers, signal mnemonics, and signal descriptions for the RJ45 connectors. The signals are identical for each serial port.

To interpret this information correctly, remember that the EIA-232-D interface was developed to connect a terminal to a modem. When computing equipment is interconnected without modems, one of the units must be configured as a terminal (data terminal equipment: DTE) and the other as a modem (data circuit-terminating equipment: DCE). Since computers are normally configured to work with terminals, they are said to be configured as a modem in most cases.

Table A-1. Connector J17 Interconnect Signals

Pin Number	Signal Mnemonic	Signal Name and Description
1	DCD	**Data Carrier Detect**. Output from modem to terminal to indicate that a valid carrier is being received.
2	RTS	**Request To Send**. Input to modem from terminal when required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.
3, 6	SG	**Signal Ground**. Common return line for all signals at the modem interface.
4	TxD	**Transmit Data**. Data to be transmitted; input to modem from terminal.
5	RxD	**Receive Data**. Data which is demodulated from the receive line; output from modem to terminal.
7	CTS	**Clear To Send**. Output from modem to terminal to indicate that message transmission can begin. When a modem is used, CTS follows the off-to-on transition of RTS after a time delay.
8	DTR	**Data Terminal Ready**. Input to modem from terminal; indicates that the terminal is ready to send or receive data.

The MVME162LX uses two Zilog Z85230 serial port controllers to implement the four serial communications interfaces. Each interface supports CTS, DCD, RTS, and DTR control signals as well as the TXD and RXD transmit/receive data signals. Because the serial clocks are omitted in the MVME162LX implementation, serial communications are strictly asynchronous. The Z85230 is interfaced as DTE (data terminal equipment) with EIA-232-D signal levels.

Figure A-1 diagrams the connections between the Z85230 and the RJ45 connectors.

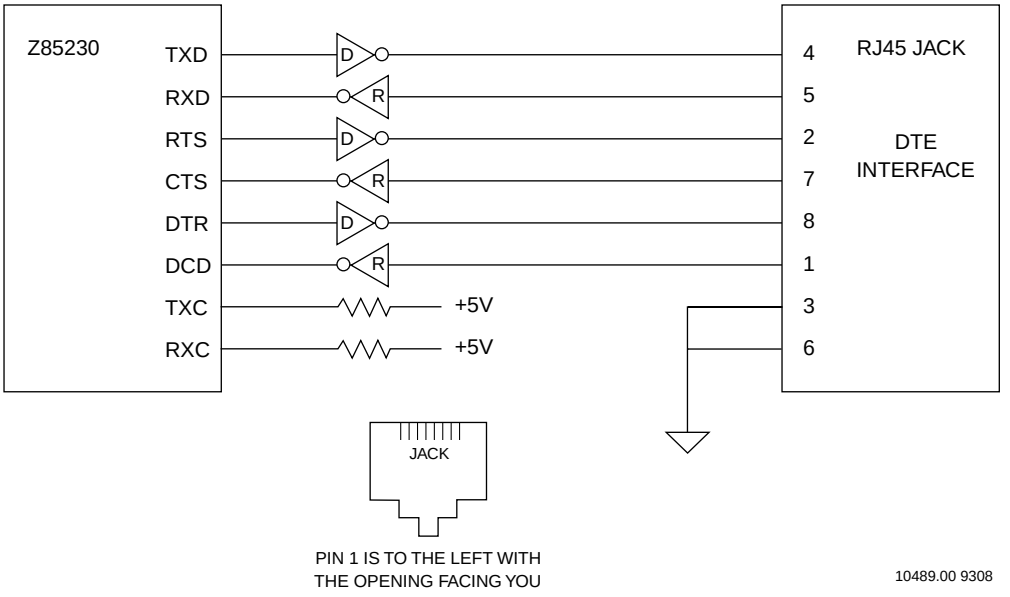


Figure A-1. Serial Interface Connections

Figure A-2 diagrams the pin assignments required in a cable to adapt a DB25 DTE device to the RJ45 connectors.

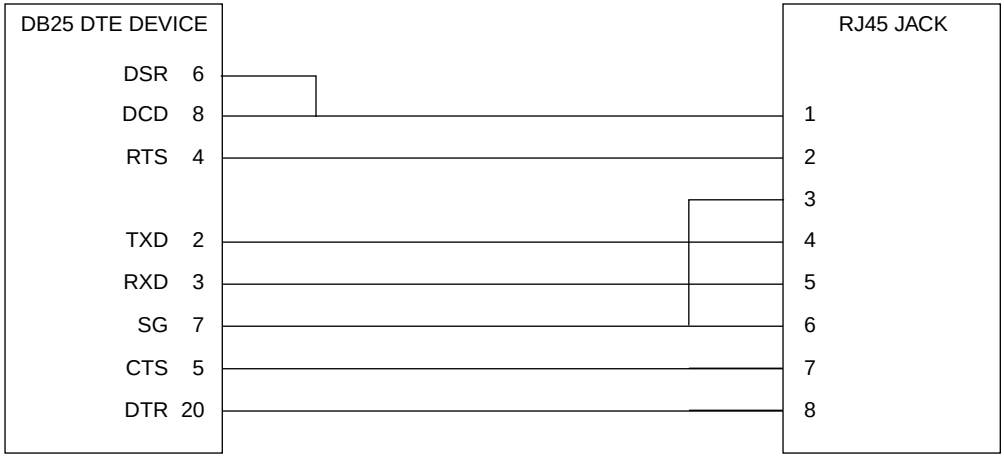


Figure A-2. DB25-DTE-to-RJ45 Adapter

Figure A-3 diagrams the pin assignments required in a cable to adapt a DB25 DCE device to the RJ45 connectors.

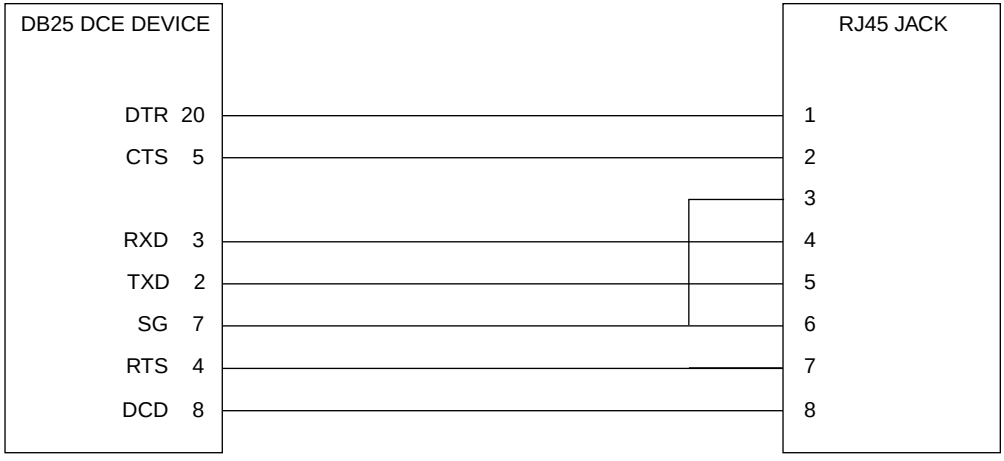


Figure A-3. DB25-DCE-to-RJ45 Adapter

Figure A-4 diagrams the pin assignments required in a typical eight-conductor serial cable having RJ45 connectors at both ends. Note that all wires are crossed.

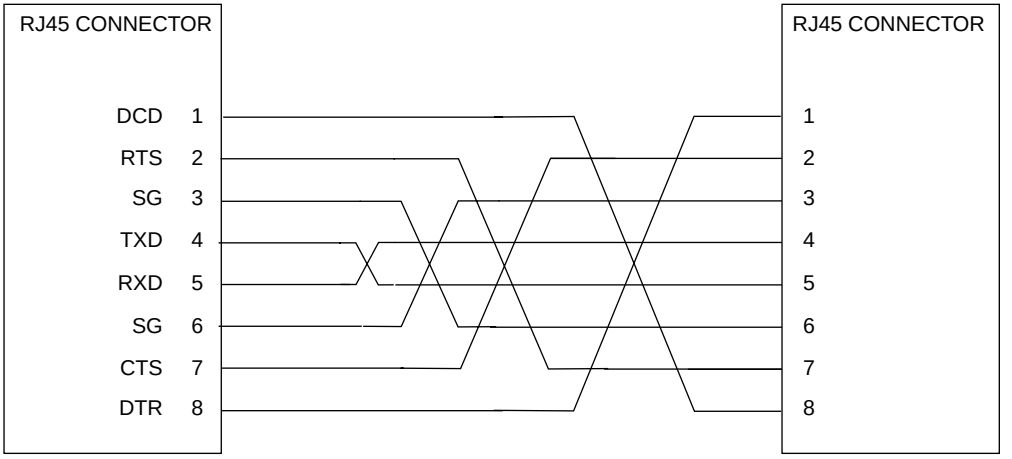


Figure A-4. Typical RJ45 Serial Cable

ETHERNET INTERCONNECTIONS B

Connector J9 is a 15-pin socket connector mounted on the front panel. It provides the Ethernet LAN (*Local Area Network*) port connections for the MVME162LX. Table B-1 lists the pin numbers, signal mnemonics, and signal descriptions for J9.

Table B-1. Ethernet Connector J9 Interconnect Signals

Pin Number	Signal Mnemonic	Signal Name and Description
1		**Ground**.
2	C+	**Collision +** (Ethernet input). A signal to indicate that multiple stations are contending for access to the transmission medium.
3	T+	**Transmit +** (Ethernet output). A line intended for operation into terminated transmission lines.
4		**Ground**.
5	R+	**Receive +** (Ethernet input). A data input sourced by the Medium Attachment Unit (MAU).
6		**Ground**.
7	NC	Not used.
8		**Ground**.
9	C–	**Collision -** (Ethernet input). Part of a differential pair.
10	T–	**Transmit -** (Ethernet output). Part of a differential pair.
11		**Ground**.
12	R–	**Receive -** (Ethernet input). Part of a differential pair.
13	+12VLAN	**+12 Vdc** power (fused on MVME162LX main module).
14		**Ground**.
15	NC	Not used.

SCSI INTERCONNECTIONS C

Connector J10 is a 68-pin socket connector mounted on the front panel. It provides the SCSI (*Small Computer System Interface*) I/O bus connections. Table C-1 lists the pin numbers, signal mnemonics, and signal descriptions for J10.

Table C-1. SCSI Connector J10 Interconnect Signals

Pin Number	Signal Mnemonic	Signal Name and Description
1-16		Return.
17, 18	TERMPWR	**Terminator Power**. +5 Vdc for SCSI terminators.
19	NC	Not used.
20-34	DTRB	Return.
35-38	DB12*-DB15*	**Data Bus** (bits 12-15). SCSI interconnect lines.
39	DBP1*	**Data Bus Parity 1** (parity for data bits 08-15). SCSI interconnect line.
40-47	DB00*-DB07*	**Data Bus** (bits 00-07). SCSI interconnect lines.
48	DBP*	**Data Bus Parity** (parity for data bits 00-07). SCSI interconnect line.
49, 50		Return.
51, 52	TERMPWR	**Terminator Power**. +5 Vdc for SCSI terminators.
53	NC	Not used.
54		Return.
55	ATN*	**Attention**. Driven by an initiator; indicates that the initiator has a message to send to the target.
56		Return.
57	BSY*	**Busy**. SCSI busy signal; indicates that the bus is in use.
58	ACK*	**Acknowledge**. Driven by an initiator; indicates an acknowledgement for a REQ/ACK data transfer handshake.
59	RST*	**Reset**. SCSI reset signal; clears the bus of all activity.
60	MSG*	**Message**. Driven by the target during the message transfer phase.
61	SEL*	**Select**. Used by the initiator to select a target or by a target to reselect an initiator.

Table C-1. SCSI Connector J10 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Name and Description
62	D/C*	**Data/Command**. Driven by the target; indicaters whether control or data information is on the data bus. True (low) indicates control information.
63	REQ*	**Request**. Driven by the target; indicates a request for a REQ/ACK data transfer handshake.
64	O/I*	**Output/Input**. Driven by a target; controls the direction of data movement on the SCSI bus. True (low) indicates input to the initiator. False (high) indicates output from the initiator. This signal is also used to distinguish between selection and reselection phases.
65-68	DB08*-DB11*	**Data Bus** (bits 08-11). SCSI interconnect lines.

Many SCSI interfaces use a 50-pin connector. Figure C-1 diagrams the interconnections found in a typical 68-pin (high-density) to 50-pin (low-density) SCSI adapter cable.

Figure C-1. Low-Density/High-Density SCSI Adapter Cable C-3/C-4

Mezzanine Connector J15 Interconnect Signals

Connector J15 is a standard double-row 100-pin socket connector mounted on the MVME162LX main module PWB (see Figure 2-1). It connects to a corresponding 100-pin plug connector on the ECC DRAM or 2 MB SRAM mezzanine board and (together with J16) carries the DRAM/SRAM address, data, and control signals to and from the mezzanine board. Table D-1 lists the pin numbers, signal mnemonics, and signal descriptions for J15.

Table D-1. Mezzanine Connector J15 Interconnect Signals

Pin Number	Signal Mnemonic	Signal Direction	Signal Name and Description
1	GND		**Ground**.
2	MPUCLK1	Input	**MPU Clock 1**. Bus clock (25 MHz).
3, 4	GND		**Ground**.
5	PURESET*	Input	**Power-Up Reset**.
6	LTS*	Bidirectional	**Local Transfer Start**. MC68040 transfer start strobe.
7	LBRESET*	Input	**Local Bus Reset**.
8	GND		**Ground**.
9	LRD	Bidirectional	**Local Read**. MC68040 read/write attribute.
10	LTIP*	Bidirectional	**Local Transfer In Progress**. MC68040 transfer-in-progress strobe.
11	GND		**Ground**.
12	SELECT	Input	**Select**. Mezzanine selection (ECC mezzanines only). High = first slot; low = second slot.
13	LLOCK*	Bidirectional	**Local Bus Lock**. MC68040 lock attribute.
14	LTA*	Bidirectional	**Local Transfer Acknowledge**. MC68040 transfer acknowledge.
15	LSIZ0	Bidirectional	**Local Transfer Size 0**. MC68040 transfer size attribute.
16	GND		**Ground**.

Table D-1. Mezzanine Connector J15 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Direction	Signal Name and Description
17	LSIZ1	Bidirectional	**Local Transfer Size 1**. MC68040 transfer size attribute.
18	LTEA*	Bidirectional	**Local Transfer Error Acknowledge**. MC68040 transfer error acknowledge.
19	GND		**Ground**.
20	SRAMDIS*	Output	**SRAM Disable**. Disable SRAM on main module.
21	LTM0	Bidirectional	**Local Transfer Modifier 0**. MC68040 transfer modifier attribute.
22	MIACKIN*	Output	**Local IACK**. Daisy-chain signal: Assert MIACKIN* if the IACK cycle is not for the mezzanine in question.
23	LTM1	Bidirectional	**Local Transfer Modifier 1**. MC68040 transfer modifier attribute.
24	GND		**Ground**.
25	LTM2	Bidirectional	**Local Transfer Modifier 2**. MC68040 transfer modifier attribute.
26	LST0	Bidirectional	**Local Error Status 0**. Valid only when LTEA* is asserted and LTA* is negated.
27	GND		**Ground**.
28	LST1	Bidirectional	**Local Error Status 1**. Valid only when LTEA* is asserted and LTA* is negated.
29	LSC0	Bidirectional	**Local Snoop Control 0**. MC68040 snoop control attribute.
30	MEZZIPL0*	Output	**Mezzanine Interrupt Line 0**. Encoded interrupt line from mezzanine.
31	LSC1	Bidirectional	**Local Snoop Control 1**. MC68040 snoop control attribute.
32	GND		**Ground**.
33	LTT0	Bidirectional	**Local Transfer Type 0**. MC68040 transfer type attribute.
34	MEZZIPL1*	Output	**Mezzanine Interrupt Line 1**. Encoded interrupt line from mezzanine.
35	GND		**Ground**.
36	MEZZIPL2*	Output	**Mezzanine Interrupt Line 2**. Encoded interrupt line from mezzanine.

Table D-1. Mezzanine Connector J15 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Direction	Signal Name and Description
37	LTT1	Bidirectional	**Local Transfer Type 1**. MC68040 transfer type attribute.
38	MEZZBR*	Output	**Mezzanine Bus Request**. Local bus request from mezzanine.
39	LMI*	Input	**Local Memory Inhibit**. MC68040 memory inhibit signal.
40	GND		**Ground**.
41	LOCKOK	Input	**Lock OK**. OK to start a locked bus cycle.
42	MEZZBG*	Input	**Mezzanine Bus Grant**. Local bus grant from mezzanine.
43	GND		**Ground**.
44	LBB*	Bidirectional	**Local Bus Busy**.
45	PEIRQ*	Output	**Parity Error Interrupt Request**. Issued to VMEchip from mezzanine.
46	SRAMSIZ0	Output	**SRAM Size 0**. Encoded SRAM size.
47			**Reserved**.
48	GND		**Ground**.
49	LA<0>	Bidirectional	**Local Address bus** (bit 0). MC68040 address line. Bit 0 is the least significant bit.
50	SRAMSIZ1	Output	**SRAM Size 1**. Encoded SRAM size.
51	GND		**Ground**.
52-55	LA<1>-LA<4>	Bidirectional	**Local Address bus** (bits 1-4). MC68040 address lines.
56	GND		**Ground**.
57, 58	LA<6>, LA<5>	Bidirectional	**Local Address bus** (bits 6, 5). MC68040 address lines.
59	GND	GND	**Ground**.
60-63	LA<7>-LA<10>	Bidirectional	**Local Address bus** (bits 7-10). MC68040 address lines.
64	GND		**Ground**.
65, 66	LA<12>, LA<11>	Bidirectional	**Local Address bus** (bits 12, 11). MC68040 address lines.
67	GND		**Ground**.
68-71	LA<13>-LA<16>	Bidirectional	**Local Address bus** (bits 13-16). MC68040 address lines.

Table D-1. Mezzanine Connector J15 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Direction	Signal Name and Description
72	GND		**Ground**.
73, 74	LA<18>, LA<17>	Bidirectional	**Local Address bus** (bits 18, 17). MC68040 address lines.
75	GND		**Ground**.
76-79	LA<19>- LA<22>	Bidirectional	**Local Address bus** (bits 19-22). MC68040 address lines.
80	GND		**Ground**.
81, 82	LA<24>, LA<23>	Bidirectional	**Local Address bus** (bits 24, 23). MC68040 address lines.
83	GND		**Ground**.
84-87	LA<25>- LA<28>	Bidirectional	**Local Address bus** (bits 25-28). MC68040 address lines.
88	GND		**Ground**.
89, 90	LA<30>, LA<29>	Bidirectional	**Local Address bus** (bits 30, 29). MC68040 address lines.
91			**Reserved**.
92	LA<31>	Bidirectional	**Local Address bus** (bit 31). MC68040 address line. Bit 31 is the most significant bit.
93	+12 V		**+12 Vdc Power**.
94	–12 V		**–12 Vdc Power**.
95	+12 V		**+12 Vdc Power**.
96	–12 V		**–12 Vdc Power**.
97, 98	GND		**Ground**.
99, 100	+5 V		**+5 Vdc Power**.

Mezzanine Connector J16 Interconnect Signals

Connector J16 is a standard double-row 100-pin socket connector mounted on the MVME162LX main module PWB (see Figure 2-1). It connects to a corresponding 100-pin plug connector on the ECC DRAM or 2 MB SRAM mezzanine board and (together with J15) carries the DRAM/SRAM address, data, and control signals to and from the mezzanine board. Table D-2 lists the pin numbers, signal mnemonics, and signal descriptions for J16.

Table D-2. Mezzanine Connector J16 Interconnect Signals

Pin Number	Signal Mnemonic	Signal Direction	Signal Name and Description
1	GND		**Ground**.
2, 3	LD<1>, LD<0>	Bidirectional	**Local Data bus** (bits 1, 0). MC68040 data lines. Bit 0 is the least significant bit.
4, 5	LD<3>, LD<2>	Bidirectional	**Local Data bus** (bits 3, 2). MC68040 data lines.
6	GND		**Ground**.
7, 8	LD<4>, LD<5>	Bidirectional	**Local Data bus** (bits 4, 5). MC68040 data lines.
9	GND		**Ground**.
10, 11	LD<7>, LD<6>	Bidirectional	**Local Data bus** (bits 7, 6). MC68040 data lines.
12, 13	LD<9>, LD<8>	Bidirectional	**Local Data bus** (bits 9, 8). MC68040 data lines.
14	GND		**Ground**.
15, 16	LD<10>, LD<11>	Bidirectional	**Local Data bus** (bits 10, 11). MC68040 data lines.
17	GND		**Ground**.
18, 19	LD<13>, LD<12>	Bidirectional	**Local Data bus** (bits 13, 12). MC68040 data lines.
20, 21	LD<15>, LD<14>	Bidirectional	**Local Data bus** (bits 15, 14). MC68040 data lines.
22	GND		**Ground**.
23, 24	LD<16>, LD<17>	Bidirectional	**Local Data bus** (bits 16, 17). MC68040 data lines.
25	GND		**Ground**.
26, 27	LD<19>, LD<18>	Bidirectional	**Local Data bus** (bits 19, 18). MC68040 data lines.

Table D-2. Mezzanine Connector J16 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Direction	Signal Name and Description
28, 29	LD<21>, LD<20>	Bidirectional	**Local Data bus** (bits 21, 20). MC68040 data lines.
30	GND		**Ground**.
31, 32	LD<22>, LD<23>	Bidirectional	**Local Data bus** (bits 22, 23). MC68040 data lines.
33	GND		**Ground**.
34, 35	LD<25>, LD<24>	Bidirectional	**Local Data bus** (bits 25, 24). MC68040 data lines.
36, 37	LD<27>, LD<26>	Bidirectional	**Local Data bus** (bits 27, 26). MC68040 data lines.
38	GND		**Ground**.
39, 40	LD<28>, LD<29>	Bidirectional	**Local Data bus** (bits 28, 29). MC68040 data lines.
41	GND		**Ground**.
42	LD<30>	Bidirectional	**Local Data bus** (bit 30). MC68040 data line.
43	DRAM_PD0	Bidirectional	**DRAM Parity Data** (bit 0). Bit 0 is the least significant bit.
44	LD<31>	Bidirectional	**Local Data bus** (bit 31). MC68040 data line. Bit 31 is the most significant bit.
45	DRAM_PD1	Bidirectional	**DRAM Parity Data** (bit 1).
46	GND		**Ground**.
47	DRAM_PD2	Bidirectional	**DRAM Parity Data** (bit 2).
48	MEZ0	Output	**Mezzanine 0**. Encoded DRAM size from mezzanine.
49	DRAM_PD3	Bidirectional	**DRAM Parity Data** (bit 3). Bit 3 is the most significant bit.
50	MEZ1	Output	**Mezzanine 1**. Encoded DRAM size from mezzanine.
51	GND		**Ground**.
52	MEZ2	Output	**Mezzanine 2**. Encoded DRAM size from mezzanine.
53	RDRAM_A0	Input	**DRAM Address** (bit 0). Parity DRAM row/column address line.
54	RDRAM_A5	Input	**DRAM Address** (bit 5). Parity DRAM row/column address line.

Table D-2. Mezzanine Connector J16 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Direction	Signal Name and Description
55	RDRAM_A1	Input	**DRAM Address** (bit 1). Parity DRAM row/column address line.
56	RDRAM_A6	Input	**DRAM Address** (bit 6). Parity DRAM row/column address line.
57	RDRAM_A2	Input	**DRAM Address** (bit 2). Parity DRAM row/column address line.
58	GND		**Ground**.
59	RDRAM_A3	Input	**DRAM Address** (bit 3). Parity DRAM row/column address line.
60	RDRAM_A7	Input	**DRAM Address** (bit 7). Parity DRAM row/column address line.
61	RDRAM_A4	Input	**DRAM Address** (bit 4). Parity DRAM row/column address line.
62	RDRAM_A8	Input	**DRAM Address** (bit 8). Parity DRAM row/column address line.
63	GND		**Ground**.
64	RDRAM_A9	Input	**DRAM Address** (bit 9). Parity DRAM row/column address line.
65	DRAMCAS0*	Input	**DRAM Column Address Strobe** (line 0). Parity DRAM column address strobe.
66	DRAMRAS*	Input	**DRAM Row Address Strobe**. Parity DRAM row address strobe.
67	DRAMCAS1*	Input	**DRAM Column Address Strobe** (line 1). Parity DRAM column address strobe.
68	GND		**Ground**.
69	DRAMCAS2*	Input	**DRAM Column Address Strobe** (line 2). Parity DRAM column address strobe.
70	DRAMOE0*	Input	**DRAM Output Enable** (line 0). Parity DRAM output enable signal.
71	DRAMCAS3*	Input	**DRAM Column Address Strobe** (line 3). Parity DRAM column address strobe.
72	DRAMOE1*	Input	**DRAM Output Enable** (line 1). Parity DRAM output enable signal.
73	GND		**Ground**.
74	DRAMOE2*	Input	**DRAM Output Enable** (line 2). Parity DRAM output enable signal.

Table D-2. Mezzanine Connector J16 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Direction	Signal Name and Description
75	DRAMWELL*	Input	**DRAM Write Enable** (lines D07-D00). Parity DRAM write enable signal.
76	DRAMOE3*	Input	**DRAM Output Enable** (line 3). Parity DRAM output enable signal.
77	SRAMWELL*	Input	**SRAM Write Enable** (lines D07-D00).
78	GND		**Ground**.
79	DRAMWELM*	Input	**DRAM Write Enable** (lines D15-D08). Parity DRAM write enable signal.
80	DRAMWEUM*	Input	**DRAM Write Enable** (lines D23-D16). Parity DRAM write enable signal.
81	SRAMWELM*	Input	**SRAM Write Enable** (lines D15-D08).
82	SRAMWEUM*	Input	**SRAM Write Enable** (lines D23-D16).
83	GND		**Ground**.
84	DRAMWEUU*	Input	**DRAM Write Enable** (lines D31-D24). Parity DRAM write enable signal.
85	SRAMCS0*	Input	**SRAM Chip Select** (line 0).
86	SRAMWEUU*	Input	**SRAM Write Enable** (lines D31-D24).
87	SRAMCS1*	Input	**SRAM Chip Select** (line 1).
88	GND		**Ground**.
89	SRAMCS2*	Input	**SRAM Chip Select** (line 2).
90	SRAM_PA2	Input	**SRAM Address** (bit 2).
91	SRAMCS3*	Input	**SRAM Chip Select** (line 3).
92	SRAM_PA3	Input	**SRAM Address** (bit 3).
93, 94			**Reserved**.
95	GND		**Ground**.
96	+5V STDBY		**+5 Vdc Standby**. Secondary power for system logic circuits.
97-100	+5 V		**+5 Vdc Power**.

Mezzanine Board Dimensions

The following drawings specify the dimensions critical to connector and mounting hole placement on the mezzanine boards used with the MVME162LX. They may be helpful in the event you wish to fabricate your own mezzanine boards for use with the MVME162LX.

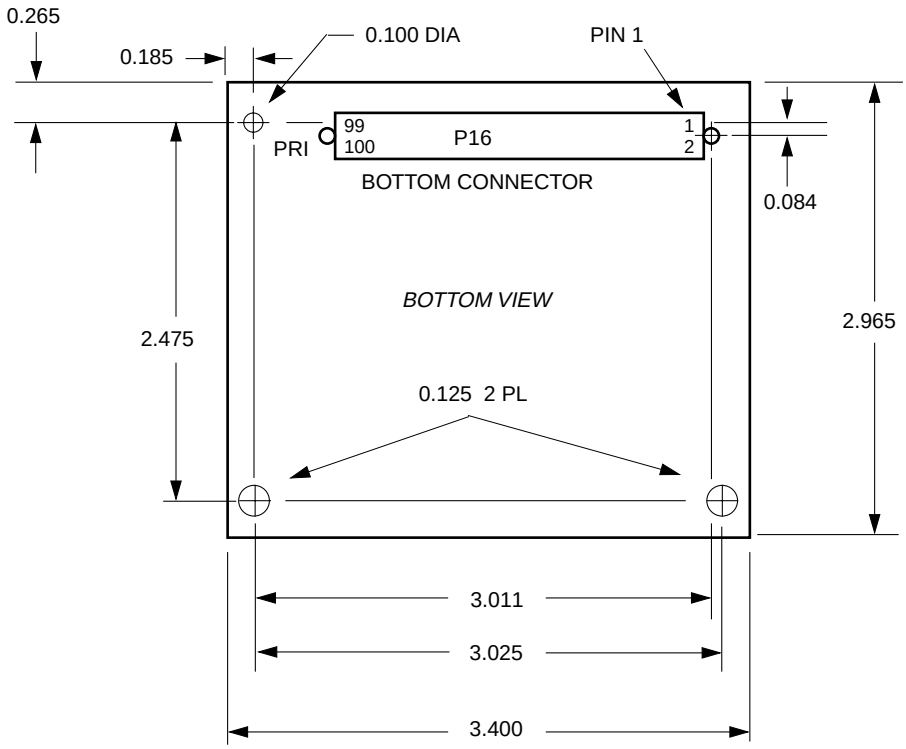


Figure D-1. Mezzanine Board Dimensions (Parity DRAM)

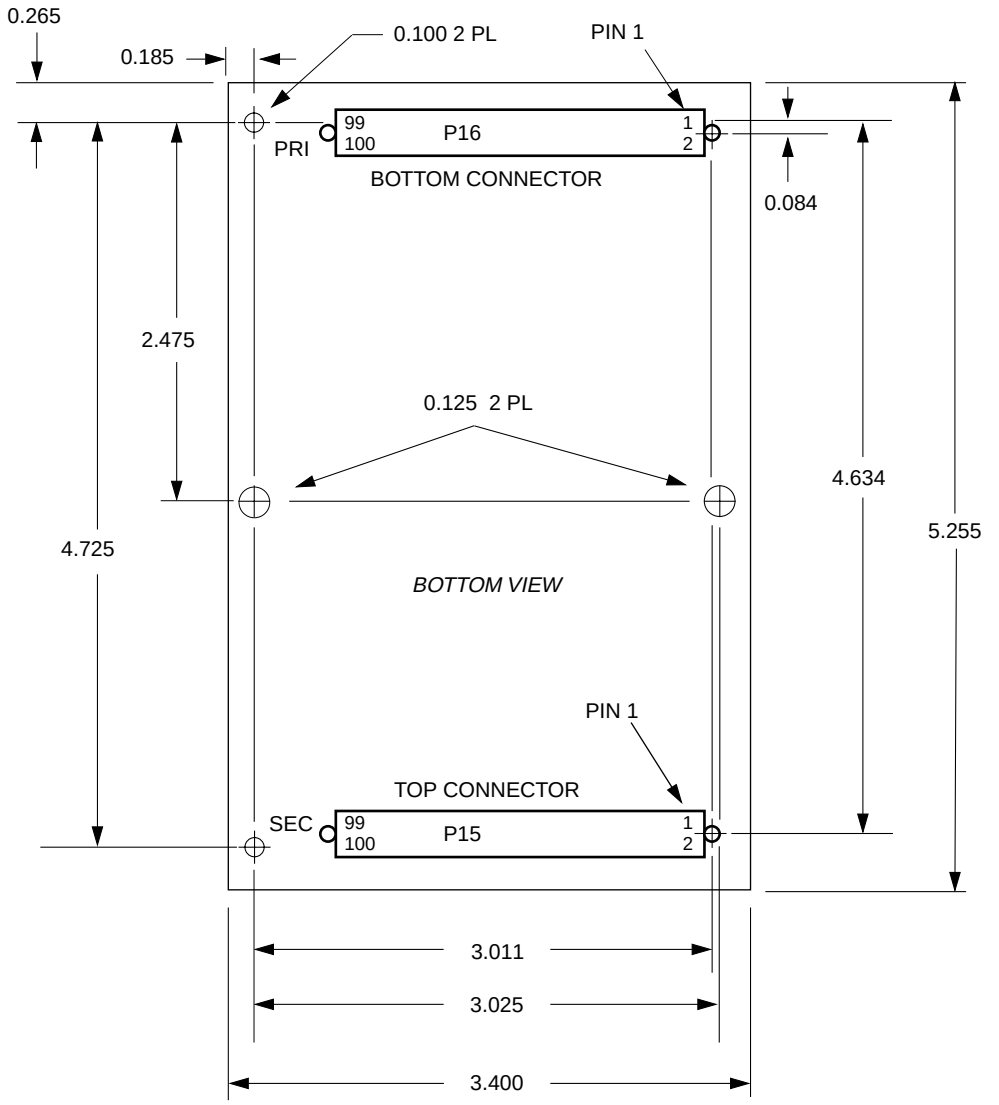


Figure D-2. Mezzanine Board Dimensions (SRAM and ECC DRAM)

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