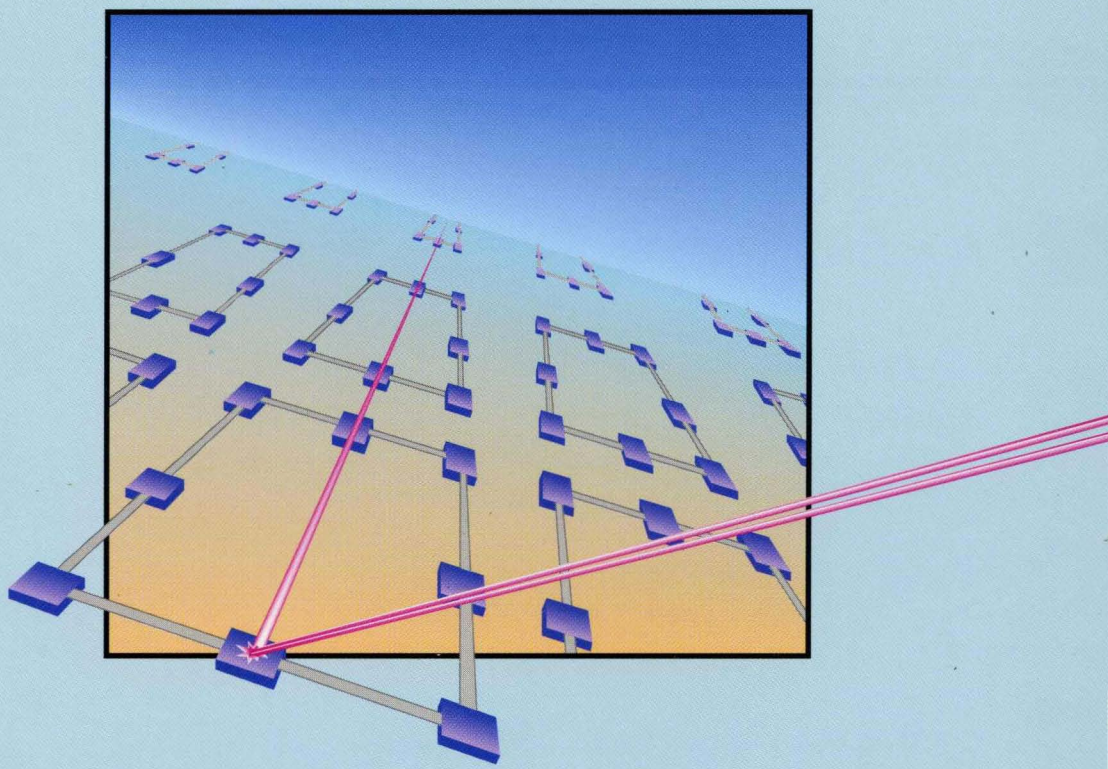
MC68836UM/AD

FDDI



Fiber Distributed Data Interface
User's Manual

MC68836

MOTOROLA

MOTOROLA

MC68836

FDDI Clock Generator

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FCG ACRONYM LIST

ANSI—American National Standards Institute

C0/Cm—Static Capacitance to Motional Capacitance

C_L—Load Capacitance

DC—Direct Current (Analog Voltage)

ECL—Emitter-Coupled Logic

ELM—MC68837 Elasticity Buffer and Link Monitor

FCG—MC68836 FDDI Clock Generator

FDDI—Fiber Distributed Data Interface

L/C—Inductance to Capacitance Ratio

LAN—Local Area Network

NRZ—Non-Return-to-Zero

NRZI—Non-Return-to-Zero, Invert on Ones

PC—Printed Circuit

PHY—Physical Layer

PLL—Phase-Locked Loop

SD—Signal Detect

TTL—Transistor-Transistor Logic

VCO—Voltage-Controlled Oscillator

VCXO—Voltage-Controlled Crystal Oscillator

SECTION 1
OVERVIEW

The FDDI is a LAN standard under ANSI auspices. The standard supports a 100-Mbits/sec fiber-optic-based token ring with up to 1000 stations; total ring length should not exceed 200 km with up to 2 km between stations. Users are encouraged to refer to the pertinent ANSI standard documents for further information.

1.1 INTRODUCTION

The MC68836 FDDI clock generator (FCG) implements the lower portion of the physical layer functions of the FDDI standard including clock recovery, data recovery, and NRZI conversions. The FCG also performs a 5-bit parallel to serial conversion during transmission and a serial to 5-bit parallel conversion during reception. The FCG uses the 5-bit parallel interface to communicate with the MC68837 ELM device. The FCG directly connects to fiber-optic modules through differential driver/receiver pins.

1.2 FEATURES

The FCG features are as follows:

- Full-Duplex Operation
- Recovers 125-MHz Clock from Incoming Serial NRZI Data Stream
- Reclocks Incoming Serial NRZI Data Stream Using Recovered Clock
- Converts NRZI Data to NRZ
- Converts Received Serial Bit Stream to 5-Bit Parallel Form
- Generates 25-MHz Receive Clock
- Blanks Receive Data When Signal Detect Is Inactive
- Generates 125-MHz Transmit Clock from either External 25-MHz Transmit Clock or On-Chip 25-MHz Crystal Oscillator
- Converts 5-Bit Parallel Transmit Data to 1-Bit Serial Data
- Converts Transmit NRZ Data to NRZI Data
- Loopback and Transmitter-Off Modes
- Three-State TTL Outputs Allow Board Testing
- Translates Between Pseudo-ECL Levels and TTL Levels

SECTION 2
FUNCTIONAL DESCRIPTION

This section describes the individual blocks in the FCG. Descriptions are related to functional operation only. For parametric specifications, refer to **Section 5 Electrical Characteristics**. Figure 2-1 is a functional block diagram of the complete chip.

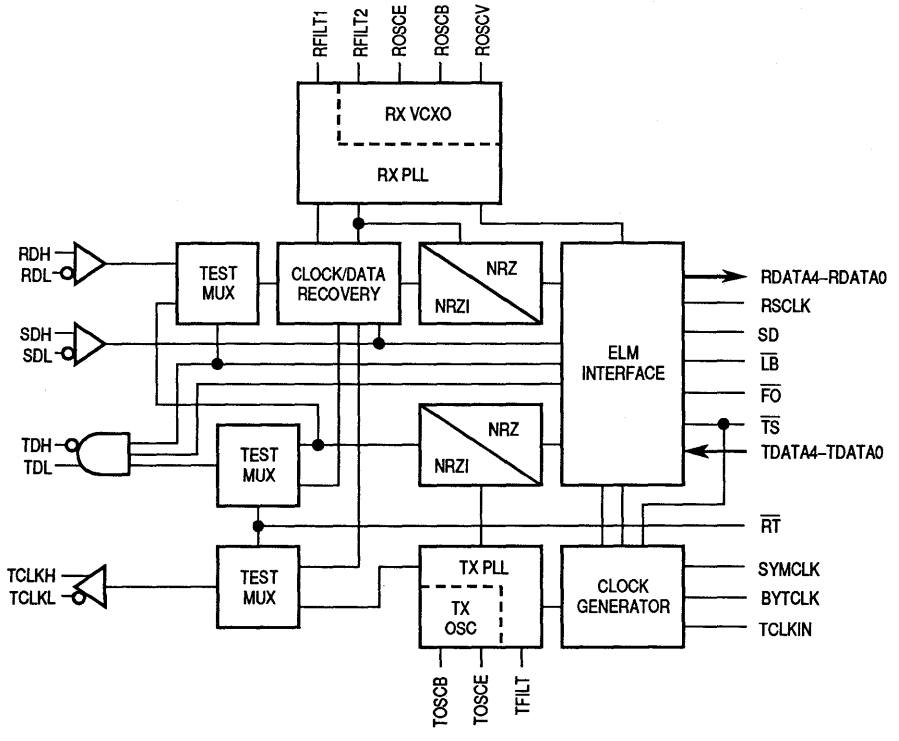


Figure 2-1. FCG Block Diagram

2.1 FCG-ELM INTERFACE

The FCG-ELM interface is a TTL-level interface composed of three parts: receive data, signal detect, and transmit data. The transmit and receive parts each have independent clocks.

2.1.1 Receive Data

Data received from the fiber-optic link is output on RDATA4–RDATA0. Five new bits are valid on each rising edge of RSCLK. RDATA4 is the first bit received, and RDATA0 is the last bit received from the serial interface. Functional timing is illustrated in Figure 2-2. RSCLK is derived from the incoming bit stream and is not necessarily synchronous with SYMCLK. Data on RDATA4–RDATA0 is not aligned to symbol boundaries. The MC68837 ELM concatenates successive 5-bit groups and synchronizes them to the JK symbols at the beginning of a frame. Symbol synchronization is maintained in the ELM for the duration of the frame.

2.1.2 Receive Signal Detect

SD is a level translation of SDH/SDL and indicates whether the fiber-optic receiver on RDH/RDL is receiving enough light energy to produce a correct output. When SD is not asserted low, RDATA4–RDATA0 are forced low, which is the quiet condition. SD is an asynchronous signal that changes whenever the SDH/SDL outputs change states.

2.1.3 Transmit Data

The 5-bit data symbols to be transmitted are input from the ELM chip on TDATA4–TDATA0. A new 5-bit symbol is input on each rising edge of SYMCLK. Successive 5-bit symbols are concatenated by the FCG as they are output to the fiber-optic transmitter. TDATA4 is the first bit transmitted, and TDATA0 is the last bit transmitted. Functional timing is shown in Figure 2-2. BYTCLK is derived from SYMCLK divided by 2.

Some system configurations, such as a concentrator, require that an external transmit clock be used by the FCG. This configuration can be implemented by providing a 25-MHz clock to TCLKIN to be used as the transmit clock instead of SYMCLK. All timing shown in Figure 2-2 that relates to SYMCLK will then apply to TCLKIN. When TCLKIN is used, a transmit crystal is not needed, and TOSCB should be connected to ground. In this mode, SYMCLK and BYTCLK are not used. Their frequencies and phases are locked to TCLKIN; however, absolute phases to TCLKIN are not guaranteed.

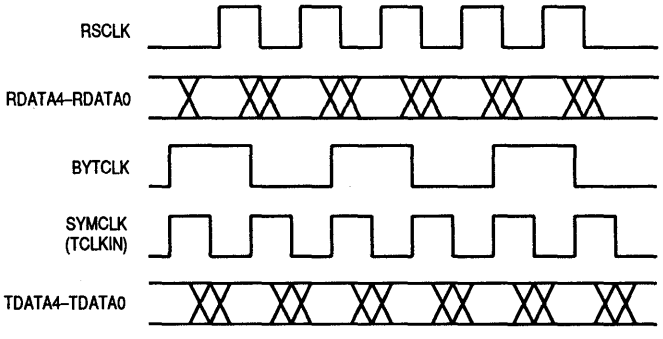


Figure 2-2. FCG-ELM Functional Timing

2.2 TEST AND CONTROL

Four pins, $\overline{LB}$, $\overline{FO}$, $\overline{TS}$, and $\overline{RT}$, are used for controlling the operating mode and for in-circuit and in-production testing of the FCG. Additionally, the TCLKH/TCLKL outputs are provided for diagnostic purposes.

2.2.1 Parallel Loopback

When $\overline{LB}$ is high, the FCG is in the normal mode, providing a method of testing most of the FCG while it is on the board. When $\overline{LB}$ is low, the FCG is in loopback mode. In this mode, the serial transmit data that would normally go to the TDH/TDL outputs is rerouted to the receive path and replaces the RDH/RDL inputs. This serial transmit data is then recovered by the receiver as if coming from the network and is reported on RDATA4–RDATA0. By comparing the transmitted data to the received data, circuitry included in the loopback path can be tested. In loopback mode, because the RDH/RDL inputs are not used, the SDH/SDL inputs are ignored; the SDH/SDL inputs need not be asserted for data to be produced on RDATA4–RDATA0. SD continues to report the state of SDH/SDL. During the loopback state, TDH is forced low and TDL is forced high, which is equivalent to the quiet or no-light state.

2.2.2 Fiber-Optic Off

When $\overline{FO}$ is low, TDH is forced low and TDL is forced high, which is the quiet or no-light state.

2.2.3 Three-State Control

When $\overline{TS}$ is low, all TTL outputs are forced into the high-impedance state. The following outputs are affected: SD, RDATA4–RDATA0, and RSCLK for receive and SYMCLK and BYTCLK for transmit.

2.2.4 Receive Test

$\overline{RT}$ is used for IC testing and is not intended for use at the board level. When $\overline{RT}$ is high, the FCG is in normal mode. When $\overline{RT}$ is low, RDH/RDL at 125 Mbps is rerouted to TDH/TDL, and TCLKH/TCLKL becomes the receive serial clock at 125 MHz. Rerouting is done after the PLL and the receiver retiming circuitry so that TDH/TDL carries recovered data and TCLKH/TCLKL carries the recovered clock. TDH/TDL is not guaranteed to meet the normal timing specifications in this mode.

2.2.5 Serial Loopback

This test is activated by simultaneously forcing $\overline{RT}$ and $\overline{TS}$ low. TDH/TDL will immediately reflect the input from RDH/RDL. Similarly, TCLKH/TCLKL will reflect the input from SDH/SDL in this special test mode.

2.3 FIBER-OPTIC INTERFACE

The interface to the fiber-optic transmitter and receiver is through differential raised-ECL signals. Normal ECL termination techniques (accounting for the voltage shift) should be used. See **Section 4 Applications** for a discussion of ECL termination techniques.

2.3.1 Transmit Data

The interface to the fiber-optic transmitter is provided by differential output signals, TDH/TDL. When TDH is high and TDL is low, the fiber-optic transmitter should output light. Conversely, when TDH is low and TDL is high, the fiber-optic transmitter should be in the quiet or no-light state.

2.3.2 Receive Data and Signal Detect

The interface to the fiber-optic receiver is provided by differential input signals, SDH/SDL and RDH/RDL. When SDH is high and SDL is low, it indicates that the receiver is getting enough light energy from the network and data on RDH/RDL is valid. When SDH is low and SDL is high (and $\overline{LB}$ is high), the FCG will report zeros (quiet) on the RDATA4–RDATA0 bus. During this time, the FCG will still attempt to lock onto the receive data. When RDH is high and RDL is low, the input is a logical one or light-on. When RDH is low and RDL is high, the input is a logical zero or no-light. During testing, these pins should always be opposite in polarity (raised-ECL levels) to ensure proper operation.

2.4 TRANSMITTER

The following paragraphs describe the operation of the transmitter, which consists of two major blocks: clock generation and data encoding.

2.4.1 Clock Generation

The transmitter has a flexible clocking mechanism where either an external 25-MHz signal or the on-chip crystal oscillator is the clock source. If a signal is present on TCLKIN, the signal from the on-chip crystal oscillator is not used. Switching between the on-chip signal source and the external signal source (TCLKIN) is automatic. If no signal is present on TCLKIN for more than approximately 320 ns, the on-chip signal is used. If TCLKIN is used, it is recommended that the crystal oscillator be disabled by connecting TOSCB to ground.

2.4.1.1 EXTERNAL CLOCK. To provide a clock to the FCG, feed a 25-MHz TTL-level signal into the TCLKIN pin and connect the TOSCB pin to ground. This disables the on-chip crystal oscillator. Of course, the frequency and jitter performance of the external clock signal must meet FDDI standards. SYMCLK and BYTCLK are derived from TCLKIN in this mode of operation, but they have an unknown phase relationship to TCLKIN and are not used.

2.4.1.2 CRYSTAL OSCILLATOR. The on-chip crystal oscillator is a Colpitts type where one pin of the crystal is connected to ground. When the crystal oscillator is used, TCLKIN should be connected to ground. When the crystal oscillator is used to provide clocks to the rest of the system, a few guidelines are needed. These are discussed in **Section 3 Signal Description.** SYMCLK and BYTCLK are derived from the on-chip crystal oscillator in this mode.

2.4.2 Frequency Multiplier

This block is a PLL that uses the 25-MHz signal as a reference. An internal VCO running at approximately 125 MHz is divided by 5 and then compared to the 25-MHz reference. The difference in phase (and frequency) is converted to a DC signal that controls the frequency of the VCO. This control voltage causes the VCO to track and phase-lock to the reference signal. The loop filter that limits the frequency response of the PLL control loop is set by the RC network connected to the TFILT pin.

2.4.3 NRZI Encoder

NRZI is a method of encoding a clock signal into a data stream. It operates by inverting the polarity of the output signal on every one bit and not inverting the output on zero data. A string of ones produces one transition per bit, and a string of zeros produces no transitions. There is a one-baud delay from the incoming bit to the encoded output. Figure 2-3 describes NRZI coding with its corresponding NRZ code. NRZI, along with 4B/5B encoding, assures the receive PLL of a certain minimum density of clock transitions for any given data pattern. The 4B/5B encoding is described in the MC68837UM/AD, *MC68837 User's Manual.* Note that the first NRZI baud is undefined since each successive baud is dependent on the previous baud. Strings of zeros could be either light-on or no-light as shown in Figure 2-3.

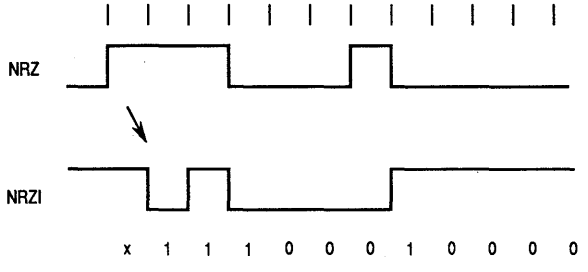


Figure 2-3. NRZI Code

2.4.4 Test Multiplexers

The test multiplexers are controlled by the $\overline{RT}$ pin. While $\overline{RT}$ is high, the normal signals are output by TDH/TDL and TCLKH/TCLKL. While $\overline{RT}$ is low, recovered clock and data from the receiver are output on TCLKH/TCLKL and TDH/TDL, respectively. The multiplexers are provided for test purposes only.

2.5 RECEIVER

The receiver consists of several blocks: NRZI decoder, clock recovery, clock generator, and PLL. Each block is discussed in the following paragraphs.

2.5.1 Clock Generator

The clock generator consists of a VCXO and two PLLs. One PLL is a frequency multiplier that takes the 20.8333-MHz VCXO signal and multiplies it by 6 to produce a 125-MHz clock. This PLL is similar to the frequency multiplier in the transmitter. The 20.8333-MHz was selected as the base frequency for the receiver to minimize any crosstalk problems between the transmitter and receiver. A second PLL is used to recover clock and data information from the received bit stream. The VCXO is controlled by the incoming bit stream and locks to it. A crystal oscillator is used in this PLL to improve the jitter tolerance. An adaptive phase detector is used to further enhance the performance.

2.5.2 Clock and Data Recovery

The clock and data recovery is the heart of the receiver. The 125-MHz clock from the VCO is compared in a phase detector to the incoming bit stream. If the VCO lags in phase, the VCXO (at 20.833 MHz) is told to slightly increase in frequency. Similarly, if the VCO leads in phase, the VCXO is told to decrease frequency. The loop bandwidth of this PLL is low and causes the data recovery circuit to track only low-frequency shifts.

The recovered (reconstructed) clock at 125 MHz is used to sample the data using an adaptive technique. The current sampling point is selected based on previous baud edges. The output of this block is an NRZI stream that is then converted to NRZ in the next block.

2.5.3 NRZI Decoder

The NRZI decoder is the reverse of the encoder on the transmitter. Received data bits are compared to the immediately preceding bit to determine if the current bit is a one or zero. Refer to **2.4.3 NRZI Encoder** for a discussion of NRZI coding. The decoded bit is then loaded into a 5-bit shift register, which is presented to the RDATA bus on each rising edge of SYMCLK. The FCG does not attempt to align to 5-bit symbol boundaries; this function is performed in the MC68837 ELM device.

2.5.4 Test Multiplexer

This multiplexer is used to loop transmitted data to the receiver input and is controlled by $\overline{LB}$. While $\overline{LB}$ is high, the receiver operates normally. While $\overline{LB}$ is low, data from the transmitter is connected to the receiver input and data present on RDH/RDL is ignored. During loopback, data is presented on RDATA4–RDATA0 regardless of the state of SDH/SDL.

SECTION 3
SIGNAL DESCRIPTION

The FDDI clock generator has 28 signal pins, 8 external component pins, 9 power pins, and 8 ground pins. Figure 3-1 illustrates a functional pinout. Descriptions for each of these pins is given in the following paragraphs.

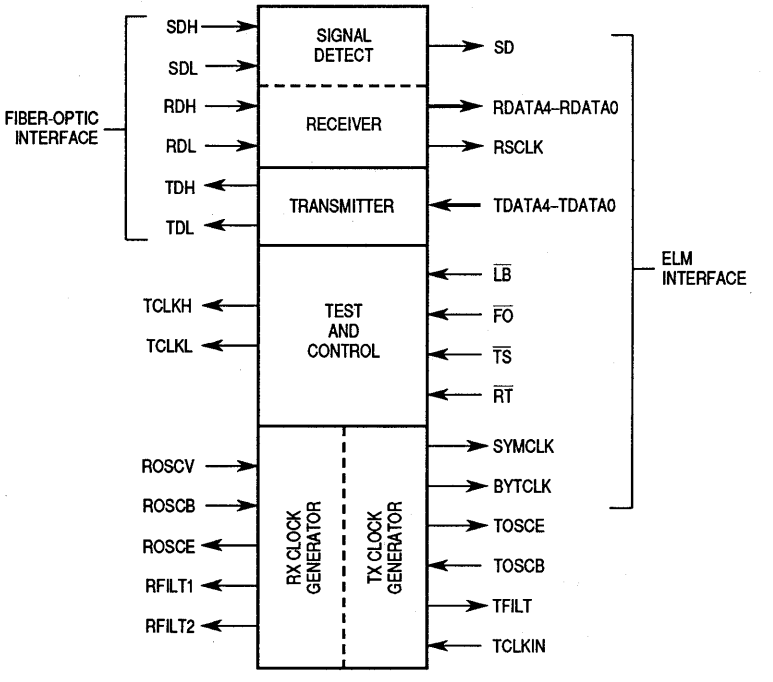


Figure 3-1. FCG Functional Pinout

3.1 ELM INTERFACE SIGNALS

The following paragraphs discuss the ELM interface signals.

Recovered Symbol Clock (RSCLK)

This 25-MHz output signal is phase-locked to the incoming receive data stream. RSCLK is used to clock out received data to the RDATA4–RDATA0 bus. This TTL-level signal is in the high-impedance state while $\overline{TS}$ is low.

Symbol Clock (SYMCLK)

This 25-MHz clock output signal is used by the FCG to clock TDATA4–TDATA0 into the FCG. It is a TTL-level signal that is in the high-impedance state while $\overline{TS}$ is low. This signal is derived from the internal VCO operating at 125 MHz and then dividing it by 5. SYMCLK is phase-locked to TCLKIN or the on-chip crystal oscillator, whichever is enabled; however, when TCLKIN is used, SYMCLK will be delayed. (SYMCLK is not used to latch data into the transmitter while TCLKIN is used.)

Byte Clock (BYTCLK)

This 12.5-MHz clock output signal is generated by the FCG for the ELM and MAC circuits and is derived from SYMCLK. It is a TTL-level signal that is the high-impedance state while $\overline{TS}$ is low.

Receive Data (RDATA4–RDATA0)

Data from this TTL-level parallel data bus is output synchronously with the rising edge of RSCLK. RDATA4–RDATA0 is the data from RDH/RDL after it has been retimed, converted to NRZ, and converted to parallel form. While $\overline{TS}$ is low, this data bus is the high-impedance state.

Signal Detect (SD)

This asynchronous output signal indicates the current state of the SDH/SDL input. It is a TTL-level signal that is in the high-impedance state while $\overline{TS}$ is low.

Transmit Data (TDATA4–TDATA0)

This parallel data input bus comes from the ELM. Five new data bits are latched into the transmitter every 40 ns on rising edges of SYMCLK (or TCLKIN if active). This data is transmitted serially at 125 MHz with TDATA4 transmitted first. This is a TTL-level bus.

3.2 FIBER-OPTIC INTERFACE SIGNALS

The FCG provides a direct interface to standard FDDI optical modules. This scheme uses raised ECL. The four signals use fully differential connections for a total of eight pins. Refer to **Section 4 Applications** for additional information on ECL connection techniques. These pins must be properly terminated to meet the specifications given in **Section 5 Electrical Characteristics.**

Receive Serial Data (RDH/RDL)

The receive serial data includes two pins. This input is serial NRZI data at 125 MHz from the fiber-optic receiver. This is a differential, raised-ECL signal.

Signal Detect Input (SDH/SDL)

The signal detect input includes two pins. This input comes from the fiber-optic receiver and indicates that the receive serial data is valid. This is a differential, raised-ECL signal.

Transmit Serial Data (TDH/TDL)

The transmit serial data includes two pins. This output provides serial NRZI data at 125 MHz to the fiber-optic transmitter. While the $\overline{RT}$ pin is low, these pins output demodulated, then remodulated data from the RDH/RDL pins. This is a differential, raised-ECL signal.

Transmit Serial Clock (TCLKH/TCLKL)

The transmit serial clock includes two pins. This 125-MHz output is only used for diagnostic testing. During normal operation, to reduce power consumption, each output should be tied to ground through a 1-kΩ resistor. This is a differential, raised-ECL signal.

NOTE

This signal does not represent the internal sample point of the data recovery circuit while in the receiver test mode.

3.3 OSCILLATORS AND PHASE-LOCKED LOOP SIGNALS

The following paragraphs describe the oscillators and phase-locked loop signals for both transmit and receive functions.

Transmit Clock In (TCLKIN)

This TTL-level signal is a 25-MHz optional clock input. If TCLKIN is not used, it should be connected to ground. While this signal is used, the on-chip transmit crystal oscillator is not used.

Transmitter Oscillator Base (TOSCB)

This internally biased input pin connects to the crystal oscillator transistor's base. See **3.6.1 Receive Crystal** for further details. When TCLKIN is used, this pin should be connected to ground.

Transmitter Oscillator Emitter (TOSCE)

This internally biased output pin connects to the crystal oscillator transistor's emitter. See **3.6.1 Receive Crystal** for further details. When TCLKIN is used, this pin should be left open.

Transmit PLL Loop Filter (TFILT)

This pin is the output of the PLL charge pump and drives an external lead-lag loop filter. An analog voltage of between 1.5 V and 4.0 V is present on this pin while the PLL is in lock.

Receiver Oscillator Base (ROSCB)

This internally biased pin connects to the receive crystal oscillator transistor's base. See **3.6.1 Receive Crystal** for further details.

Receiver Oscillator Emitter (ROSCE)

This internally biased pin connects to the receive crystal oscillator transistor's emitter. See **3.6.1 Receive Crystal** for further details.

Receiver Oscillator Voltage (ROSCV)

This signal is not used.

Receive PLL Loop Filter 1 (RFILT1)

This pin is the output of the receiver clock recovery PLL charge pump and drives an external lead-lag loop filter. An analog voltage (DC) of between 1.5 V and 4.0 V is present on this pin while the clock recovery PLL is in lock.

Receive PLL Loop Filter 2 (RFILT2)

This pin is the output of the receiver frequency multiplier PLL charge pump and drives an external lead-lag loop filter. An analog voltage (DC) of between 1.5 V and 4.0 V is present on this pin while the multiplier PLL is in lock.

3.4 TEST AND CONTROL SIGNALS

The following paragraphs discuss the test and control signals for the FCG.

Loopback ($\overline{LB}$)

While this input is low, the FCG disconnects the receive serial input and provides the serial transmit data to the receive path. During this time, TDH/TDL is forced low/high (no-light condition), and the SDH/SDL inputs are ignored. This TTL-level signal has an internal pullup resistor.

Fiber-Optic Off ($\overline{FO}$)

While this input is low, TDH/TDL is forced low/high (no-light condition). This TTL-level signal has an internal pullup resistor.

Three-State ($\overline{TS}$)

While this input is low, the ELM interface output pins are forced into the high-impedance state. Pins controlled by this signal are RDATA4–RDATA0, SD, BYTCLK, SYMCLK, and RSCLK. This TTL-level signal has an internal pullup resistor.

Receive Test ($\overline{RT}$)

While this input is low, the receive serial data at the slicer is output on TDH/TDL. At the same time, the clock signal controlling the slicer is output on the TCLKH/TCLKL pins. Data on the TDATA4–TDATA0 bus is ignored during this time. This test function is provided primarily for factory testing. In normal operation, this input should be connected to V_{CC}. This TTL-level signal has an internal pullup resistor.

3.5 POWER AND GROUND

The various circuit blocks are independently powered to assist the user's noise-reduction techniques. Table 3-1 lists the V_{CC} and V_{SS} pins and their associated sections.

Table 3-1. Power and Ground Pins

V_{CC}			V_{SS}		
Pin Number	**Pin Name**	**Description**	**Pin Number**	**Pin Name**	**Description**
50	V_{CCRTTL}	Rx TTL	51	V_{SSRTTL}	Rx TTL
52	$V_{CCRECL1}$	Rx ECL	1	V_{SSRECL}	Rx ECL
2	V_{CCRPLL}	Rx PLL	3	V_{SSRPLL}	Rx PLL
5	V_{CCRVCO}	Rx VCO	7	V_{SSRVCO}	Rx VCO
11	$V_{CCRECL2}$	Rx ECL	—	—	—
16	$V_{CCTECL1}$	Tx ECL	21	$V_{SSTECL1}$	Tx ECL
22	V_{CCTPLL}	Tx PLL	26	V_{SSTPLL}	Tx PLL
27	$V_{CCTECL2}$	Tx ECL	28	$V_{SSTECL2}$	Tx ECL
29	V_{CCTTTL}	Tx TTL	30	V_{SSTTTL}	Tx TTL

Due to the frequency of operation of this device, the user is advised to use good noise-reduction techniques. In general, ECL circuitry does not produce substantial noise on power and ground buses. However, it is recommended that the transmit and receive power and ground buses be separated to minimize any potential PLL crosstalk problems. TTL circuitry does contribute noise. As such, it is desirable to separate the ECL V_{CC} pins from the TTL pins and decouple them with low-pass filters.

3.6 EXTERNAL COMPONENTS

A few external passive components are required for the FCG to operate properly. These components are illustrated in Figure 3-2. Their recommended values are specified in Table 3-2. All resistor values are ±5%, and capacitor values are ±10%.

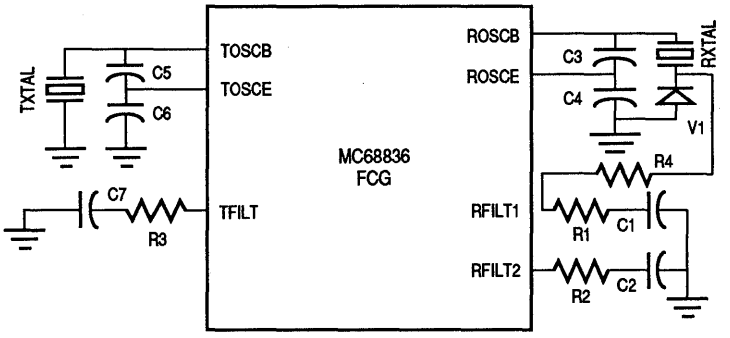


Figure 3-2. External Components

Table 3-2. Recommended Passive Component Values

Name	Value	Function
C1	470 pF	Rx Main PLL Filter
C2	3300 pF	Rx Frequency Multiplier Filter
C3	30 pF	Rx VCXO
C4	30 pF	Rx VCXO
C5	20 pF	Tx Oscillator
C6	20 pF	Tx Oscillator
C7	3300 pF	Tx Frequency Multiplier Filter
R1	24 kΩ	Rx Main PLL Filter
R2	470 Ω	Rx Frequency Multiplier Filter
R3	470 Ω	Tx Frequency Multiplier Filter
R4	10 kΩ	VCXO Control Signal
V1	MMBV105GL	Varactor Diode (Motorola)

3.6.1 Receive Crystal

The receiver requires an external crystal for proper operation. Since the receiver crystal oscillator is actually a VCXO, certain parameters of the crystal must be specified. Table 3-3 lists the important parameters. None of the parameters are difficult to meet, but motional capacitance and spurious response are not normally specified. Some crystal manufacturers use a static capacitance to motional capacitance (C0/Cm) ratio to specify pullability. Motional capacitance of this crystal is relatively high to allow increased pullability.

Table 3-3. Receive Crystal Specifications

Parameter	Value	Units
Frequency	20.833333	MHz
Load Capacitance	7.8 ± 0.2	pF
Frequency Tolerance	±10	PPM
Aging	±5	PPM/Year
Temperature Stability (0°C to 70°C)	±15	PPM
Oscillation Mode	Fundamental	—
Parameters at 25°C ± 2°C, Drive Level = 0.5 mW		
Shunt Capacitance	7±1	pF
Motional Capacitance	±5	fF (femtoFarads)
C0/Cm Ratio (max)	245	—
Series Resistance (max)	20	Ω
Spurious Responses (max)	> 5 dB below main within 500 kHz	—

Crystal resonators are mechanical devices that vibrate at the applied frequency. When the applied frequency is at a mechanically resonant point, the effective series resistance becomes low and the vibration amplitude increases. With high drive levels or low C0/Cm ratios (245 is a relatively low C0/Cm ratio), the mechanical vibrations can become non-uniform and cause resonances to occur near the desired frequency. If the equivalent series resistance becomes low enough at the spurious resonance, the oscillator may begin operating at that frequency rather than the desired frequency. Typically, spurious responses occur above the desired frequency within a few hundred kHz. The following specification requires that spurious responses be at least 5 dB below the main response. This is a safe level that will not allow the oscillator to operate on a spurious frequency.

Load capacitance is the total effective capacitance presented across the crystal resonator pins. The resonant frequency of the oscillator network and the crystal changes as the load capacitance changes. It dominates the resonant frequency equation since a crystal resonator has a very large L/C ratio. Relatively large changes in external components result in a small change in the overall resonant frequency. Figure 3-3 is a model of the VCXO including internal parasitic capacitances. Figure 3-4 illustrates the transformation of the circuit model to the load capacitance model.

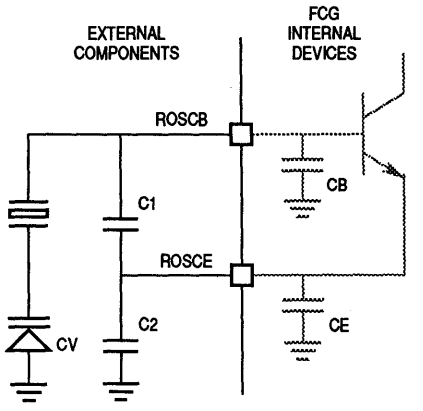


Figure 3-3. VCXO Model

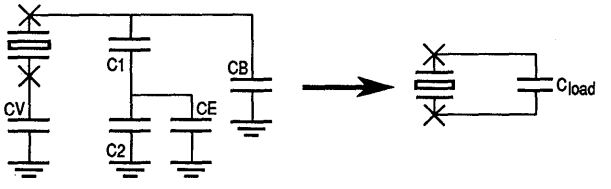


Figure 3-4. Load Capacitance Model

With a little algebra and simplification, the load capacitance equation becomes:

$$C_{load} \approx \frac{CV(C1C2+C1CE=C1CB+C2CB)}{C1\,(C2+CE+CB)+C2CB+CV(C1+C2+CE)}$$

C1 = 30 pF
C2 = 30 pF
CV = 12 pF
CB = 7 pF
CE = 7 pF

Substituting values, C_{load} becomes 7.8 pF. For correlation purposes, 7.8 pF is specified. The crystal manufacturer loads the crystals with 7.8 pF and measures the resonant frequency. The crystal can be pulled further (per ΔpF) at lower load capacitances, but the oscillator becomes more sensitive; a small variation in capacitance of any component (or stray) can move the resonant frequency out of specification. 7.8 pF is a good compromise between pullability and sensitivity to capacitor value variations.

NOTE

The MMBV105GL is a 10-pF device when measured at 4 V. When the control voltage is at a nominal 2.5 V, its capacitance is near 12 pF. The varactor can enter conduction at low tuning voltages and have a high-value capacitance (shunted by a relatively low-value resistance) with the recommended tuning resistor, R4. This provides even more tuning range.

3.6.2 Transmit Crystal

The transmit crystal is simpler in that it is a standard microprocessor crystal. The FDDI specification requires that the transmitter operate at 125 MHz ±50 PPM so the FCG needs a transmit crystal at 25.000 MHz with a total frequency tolerance of ±50 PPM (over time and temperature). To set the crystal oscillator on frequency, the load capacitance must be selected.

In this case, as one of the crystal pins is connected to V_{SS}, C_L is the capacitance to be measured by a capacitance meter at the TOSCB pin. All stray and pin capacitances should be included. Figure 3-5 is a simple model of the oscillator and the stray capacitances associated with the pins. Note that a capacitance meter cannot be used to measure the capacitance at this point because free-running AC signals internal to the chip interfere with the measurement of the meter. Other techniques using analog network analyzers may be used. The simple model of Figure 3-5 is sufficiently accurate for most applications.

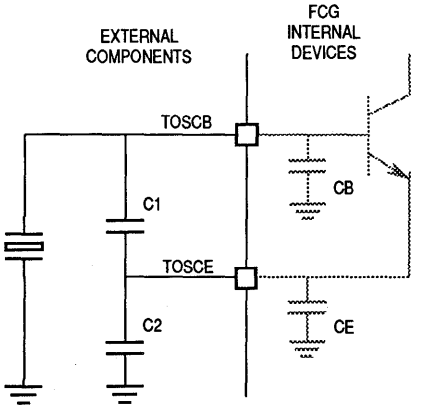


Figure 3-5. Transmitter Crystal Oscillator

For example, if C1 and C2 are 20 pF and CE and CB are each 7 pF, the equivalent capacitance is 18.5 pF. As it turns out, these values work just about perfectly for an 18-pF crystal. Experiments in the laboratory have demonstrated proper frequency operation with these values. Table 3-4 lists the recommended transmit crystal parameters.

Table 3-4. Transmit Crystal Specifications

Name	Value	Units
Frequency	25.00000	MHz
Load Capacitance	18	pF
Frequency Tolerance	±10	PPM
Aging	±2	PPM/Year
Temperature Stability (0°C to 70°C)	±5	PPM
Oscillation Mode	Fundamental	—
Parameters at 25°C ± 2°C, Drive Level = 0.5 mW		
Shunt Capacitance (max)	8	pF
Motional Capacitance (min)	10	fF (femtoFarads)
Series Resistance (max)	20	Ω
Spurious Responses (max)	> 5 dB below main within 500 kHz	—

3.6.3 Phase-Locked Loop Filters

Three PLL filters are associated with the FCG, one for each PLL. Each filter determines the dynamic characteristics of its PLL. In the case of the two-frequency multipliers, the requirements and the divide ratios are similar so the same filter components are selected. The transmitter loop bandwidth is 600 kHz, and the receiver loop bandwidth is 500 kHz when the recommended component values are used. Lockup time for these PLLs is about 2 µs.

The clock recovery PLL has different requirements. Since it is expected to remain stable in a relatively high jitter environment, its loop bandwidth is quite low. In this case, the recommended component values set the loop bandwidth to approximately 7 kHz. Lockup time will be in the range of 70 to 10 µs.

The phase detector gain coefficient (K_{ϕ}) for the three PLLs is approximately 1.59×10^{-4} A/radian. The VCO gain coefficient (K_V) is about 7.2×10^8 radian/V-sec for the two frequency multiplier PLLs. For the clock recovery PLL, K_V is about 5.2×10^3 radian/V-sec. These coefficients will allow the user to fine-tune the PLL performance in a particular application.

NOTE

These parameters are not guaranteed but are typical of what the user will see.

SECTION 4
APPLICATIONS

This section describes some applications for the FCG device. Since the FCG can operate as a master or slave, an application of a dual attached station is described. A brief discussion of PC board layout techniques is also provided.

4.1 DUAL ATTACHED STATION

There are two basic configurations for the FCG: master and slave. In the master mode, the FCG is the clock source. SYMCLK and BYTCLK are generated for use by the rest of the system. When operated as a slave, the FCG uses TCLKIN as the clock source. In both cases, on the receive side, RSCLK is generated by the FCG (in general, the receive clock is asynchronous from the transmit clock). The FCG automatically switches between master and slave operation. If a signal is present on TCLKIN, its signal will be used to clock data on the TDATA4-TDATA0 bus into the chip. If TCLKIN is idle, the signal from the on-chip crystal oscillator will be used. Figure 4-1 illustrates a dual attached station where one FCG is the system clock master; it provides SYMCLK and BYTCLK to the system. The slave FCG has its on-chip crystal oscillator disabled and uses TCLKIN as the reference. Note that SYMCLK and BYTCLK are still produced by the slave device, but they are delayed from TCLKIN. In this mode, these signals are not used to clock data into the FCG; they should not be used as timing references.

For a large system such as a concentrator where many PHY blocks are implemented, it may be more convenient to provide a master clock for the system. In this case, all FCGs would be operated as slaves, and all timing would be derived from the distributed system clock.

Figure 4-1 does not illustrate the receive crystal oscillator or the loop filters; they must still be implemented using the recommended components.

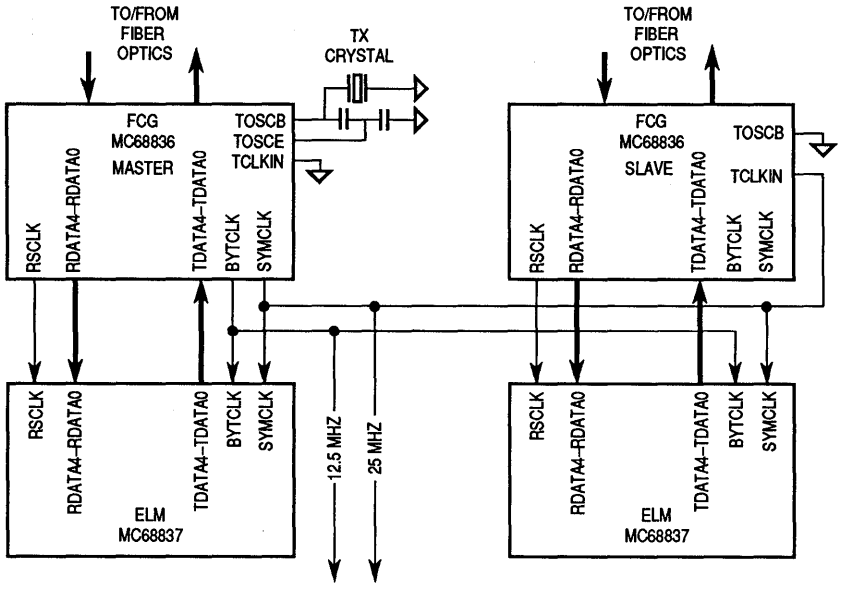


Figure 4-1. Dual Attached Station

4.2 PCB LAYOUT TECHNIQUES

The FCG is part of a high-speed system with analog and digital circuitry. Much effort has been put into the design of the FDDI chip set to minimize any problems with power supply noise, particularly in the case of the FCG. However, it is important that the user exercise care in the layout of the PC board to maximize the performance of the system. This section describes good engineering principles of PC board layout to enhance the operation of the FCG.

Ideally, power and ground buses (planes) appear to be infinite sources and sinks, respectively. If this were the case, grounding or power busing would never be a problem. However, inductance and resistance effects become significant factors at higher frequencies such as 125 MHz. Both effects tend to raise the impedance of power buses and grounds. Ground planes significantly improve the situation; they provide an inherently low inductance and resistance mechanism to distribute power. However, it is still possible for currents to flow in ground planes in ways that interact and cause noise problems.

4.3 POWER SUPPLY ISOLATION

The interface between the optical modules and the FCG uses raised ECL (pseudo-ECL). Its electrical characteristics are similar to ECL100K, but the voltages on the pins are raised to near V_{CC}. Normal ECL operates between –5.2 V and ground. The logic signals are nominally –0.9 V for a logic one and –1.8 V for a logic zero. Power supply rejection is designed into ECL devices in the form of regulators.

Raised ECL has a logic one at approximately 4.0 V and a logic zero at 3.1 V. Power supply rejection is somewhat limited with these voltages since the compliance is only about 1 V. The optical interface uses differential signals to improve the performance. Internally, differential drivers and receivers have inherent common-mode rejection within limits. Power supply noise spikes that extend into the active voltage range of the differential signals will degrade performance; thus, filtering is recommended to minimize noise on the V_{CC} pins. Figure 4-2 illustrates the differential interface between the fiber-optic module and the FCG.

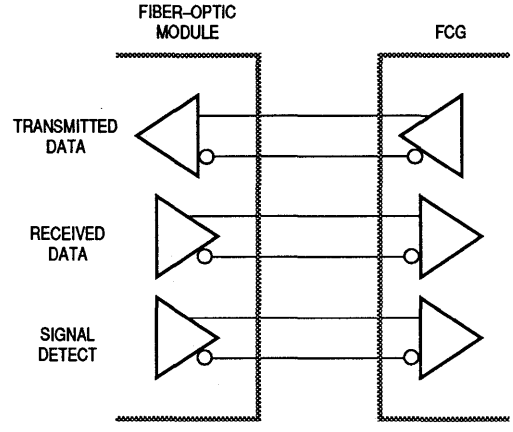


Figure 4-2. Differential Raised ECL Interface

Figure 4-3 illustrates recommended power supply filters for use with the FCG. The inductors are 1.8 µH, and the capacitors are 100-nF ceramics and 1-µF tantalums. It is difficult to specify the performance of the filters because the characteristic impedance of the power buses on the two sides of the filter is quite variable. The inductor was chosen so that its resonant frequency is at 125 MHz. Experimentation with the inductor's resonant frequency should be performed to optimize the performance. It is expected that significant frequency components will occur at 62.5 MHz and 125 MHz. Since the internal VCOs operate at 125 MHz, that was chosen as the frequency where the attenuation pole of the filter is placed.

Power to the individual sections should be drawn from an area of the power plane as near to the main power connector as possible. Running a separate power bus to the FCG section and then connecting the filters is probably the best choice. This minimizes any interaction with the TTL circuits.

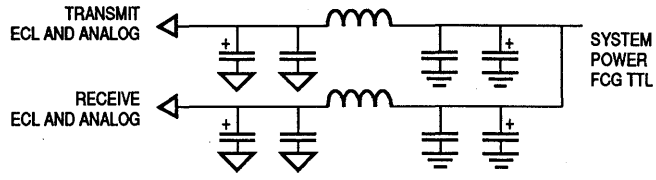


Figure 4-3. Power Distribution

Each triangle ground symbol in Figure 4-3 indicates a separate ground area. These are ultimately connected to the system ground near the power connector.

4.4 TRANSMISSION LINE TECHNIQUES

This discussion assumes that the reader is familiar with ECL characteristics. For complete information, refer to HB205, *MECL System Design Handbook*, and AN1051, *Transmission Line Effects in PCB Applications*. These documents are available from Motorola sales offices or the Literature Distribution Center.

4

If the PC board connections between the FCG and optical module are short, transmission line effects will not be significant. However, the ECL lines must still be terminated into a low impedance (50 Ω) to ensure good rise and fall times. If the connections are longer than about 2 in, transmission line techniques must be used. Matching the characteristic impedance of the transmission line improves the waveshape by removing any reflections on the conductor. Refer to AN1051/D, *Transmission Line Effects in PCB Applications*, for a complete discussion of relevant techniques. Typically, the characteristic impedance of a trace on a multi-layer PC board will be between 60 Ω and 100 Ω. A load resistor matching the characteristic impedance should be positioned at the end of the line near the input device's pin. Figure 4-4 illustrates this technique.

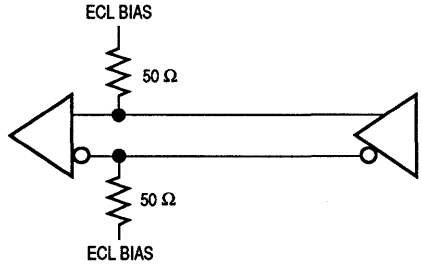
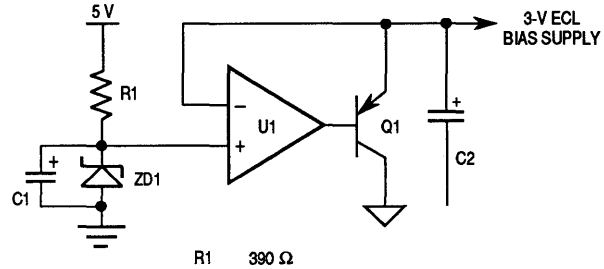


Figure 4-4. ECL Termination

Figure 4-5 illustrates a discrete method of generating the ECL bias supply. This supply should be well bypassed at the termination resistors to the local ground plane. Q1 and U1 form a Zener diode-like circuit with a capability of sinking 100 mA. The dynamic output impedance of this circuit is approximately 0.5 Ω at 40 mA. The collector of Q1 is connected to the local ground. The op-amp is powered by the main 5-V supply.

R1 is chosen to provide the proper bias current to the Zener diode. In this case, it provides 5 mA to meet the 1N5987B specification.



R1	390 Ω
C1	1μF
C2	1μF
ZD1	1N5987B
Q1	2N3905
U1	1/4 LM324

Figure 4-5. Discrete Bias Supply Generator

If an ECL bias supply is not desired, it is possible to use a Thevenin-equivalent network to terminate the lines. It consumes more power, but it is easier to implement. Basically, two resistors are connected in series between +5 V and GND. The equivalent parallel resistance is 50 Ω (or the characteristic impedance), and the voltage at the junction of the two resistors is set to 3.0 V. The formulas for the two resistor values are as follows:

$R1 = (2 * R2)/3$

$R2 = (5 * Z_0)/2$

where Z_0 is the characteristic impedance. For a characteristic impedance of 50 Ω, R1 = 83 Ω and R2 = 125 Ω. Figure 4-6 illustrates the termination network.

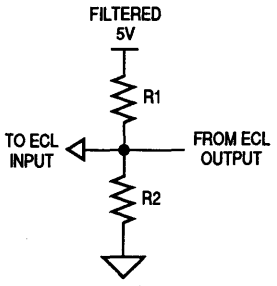


Figure 4-6. Thevenin Termination Network

SECTION 5
ELECTRICAL CHARACTERISTICS

5.1 MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	− 0.3	+ 7.0	Vdc
Input Voltage	V_{IN}	− 0.3	V_{CC}	Vdc
Operating Temperature Range	T_A	− 40	+ 85	°C
Storage Temperature Range	T_{stg}	− 55	+ 150	°C
Junction Temperature	T_j	− 40	+ 130	°C

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, normal precautions should be taken to avoid application of voltages higher than maximum-rated voltages to these high-impedance circuits. Tying unused inputs to the appropriate logic voltage level (e.g., either GND or V_{CC}) enhances reliability of operation.

5.2 DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	Vdc
TTL Input Voltage Low	V_{IL}	− 0.3	0.8	Vdc
TTL Input Voltage High	V_{IH}	2.0	V_{CC} + 0.3	Vdc
Input Leakage Current (see Note 1)	I_{IN}	400	—	µA
Input Leakage Current ($\overline{TS}$ pin) (see Note 2)	I_{IN}	800	—	µA
TTL Output Voltage High (I_{OH} = −0.4 mA)	V_{OH}	2.4	—	Vdc
TTL Output Voltage Low (I_{OL} = 4.0 mA)	V_{OL}	0.4	—	Vdc
TTL Output Leakage Current (hi-Z)	I_{OFF}	50	—	µA
ECL Output Voltage High (I_{OH} = 20 mA)	V_{OH}	V_{CC} − 1.1	V_{CC} − 0.8	Vdc
ECL Output Voltage Low (I_{OL} = 20 mA)	V_{OL}	V_{CC} − 1.9	V_{CC} − 1.6	Vdc
ECL Differential Input Voltage (see Note 3)	V_{IDIFF}	0.5	1.1	Vdc
ECL Input Common Mode (see Note 4)	V_{ICM}	V_{CC} − 1.9	V_{CC} − 0.8	Vdc
Power Supply Current	I_{DD}	—	300	mA
Supply Voltage Purity (see Note 5)	V_{CC}	50	mV P-P	

NOTE:
1. TTL inputs have internal pullup devices.
2. $\overline{TS}$ is actually two separate TTL inputs wire-bonded to the same pin.
3. For a logic high, RDL must be at least $V_{IDIFF(min)}$ but no more than $V_{IDIFF(max)}$ lower than RDH. For a logic low, RDL must be at least $V_{IDIFF(min)}$ but no more than $V_{IDIFF(max)}$ higher than RDH.
4. This is the range of valid signal voltages that may be applied to the ECL inputs for proper operation.
5. Noise on the V_{CC} lines must be less than 50 mV P-P for signals above 1 MHz. See **Section 4 Applications** for a discussion of power supply decoupling.

5.3. AC ELECTRICAL CHARACTERISTICS

The following paragraphs list the switching parameters for the FCG. These parameters are specified for the full operating temperature range.

5.3.1 TTL Interface

Clock outputs (RSCLK, SYMCLK, and BYTCLK) are specified with a load capacitance of 60 pF. All other outputs are specified with a load of 15 pF. Figure 5-1 illustrates the test load circuit. Switch points are defined as 0.4 V for low levels and 2.0 V for high levels. Time high and low tests are measured at 1.6 V (parameters 2, 3, 7, 8, 12, 13).

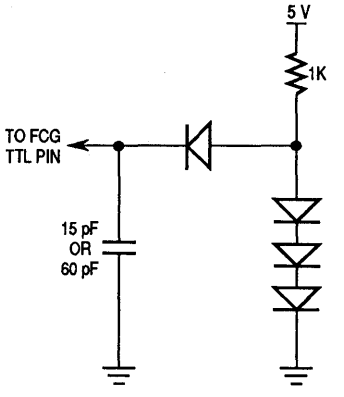


Figure 5-1. TTL Test Load

PARALLEL INTERFACE PARAMETERS (see Figure 5-2)

Num	Parameter	Min	Max	Unit
1[1]	RSCLK Period	33	50	ns
2[2]	RSCLK Time Low	20	26	ns
3[2]	RSCL Time High	14	20	ns
4	Time to RDATA Invalid	8	20	ns
5	Time to RDATA Valid	20	32	ns
6[3]	SYMCLK Period	33	50	ns
7[4]	SYMCLK Time Low	20	26	ns
8[4]	SYMCLK Time High	14	20	ns
9	Skew between SYMCLK and BYTCLK	2	7	ns
10[5]	TDATA Setup Time	12	40	ns
11[5]	TDATA Hold Time	0	28	ns
12[4]	BYTCLK Time Low	37	43	ns
13[4]	BYTCLK Time High	37	43	ns
14[6]	BYTCLK Period	66	100	ns

NOTE:

1. The receiver can operate over a range from 100 MHz to 150 MHz depending on the crystal used. Normally, the receiver will operate at the standard FDDI frequency of 125 MHz.
2. This parameter is specified with the receiver operating at 125 MHz (20.8333-MHz crystal).
3. The transmitter can operate over a range of 100 MHz to 150 MHz depending on the crystal used or the frequency of the signal applied to TCLKIN. Normally, the transmitter will operate at the standard FDDI frequency of 125 MHz.
4. This parameter is specified with the transmitter operating at 125 MHz (25-MHz crystal).
5. This is with respect to TCLKIN while TCLKIN is used and with respect to SYMCLK while the on-chip crystal oscillator is used.
6. BYTCLK is derived from SYMCLK.

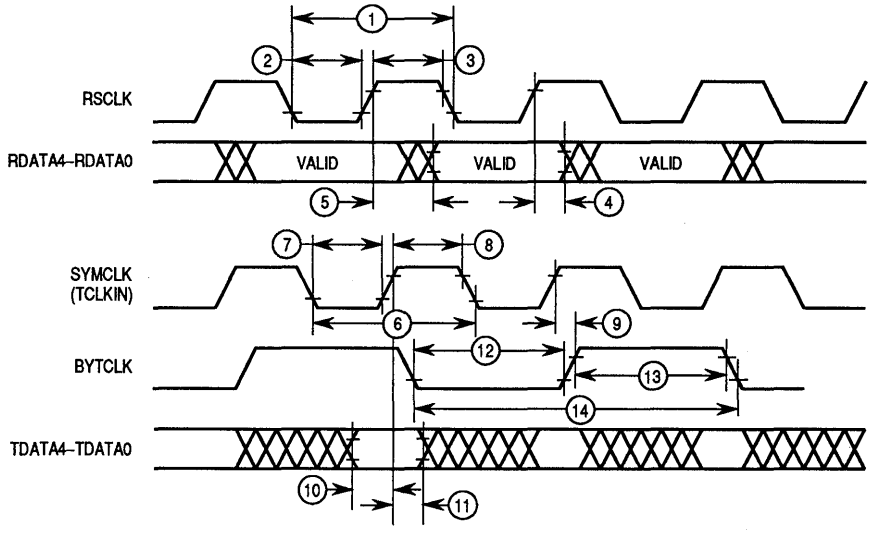


Figure 5-2. Parallel Interface Timing

TCLKIN TIMING PARAMETERS (see Figure 5-3)

Num	Parameter	Min	Max	Unit
15	TCLKIN Period (See note)	33	50	ns
16	TCLKIN Time Low	8	—	ns
17	TCLKIN Time High	8	—	ns

NOTE: The FCG can operate over a range from 100 to 150 MHz; however, the normal operating frequency is 125 MHz.

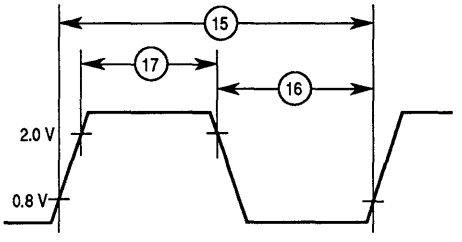


Figure 5-3. TCLKIN Timing

OUTPUT TTL EDGE TIMING (see Figure 5-4)

Num	Parameter	Min	Max	Unit
18	TTL Rise Time	—	12	ns
19	TTL Fall Time	—	12	ns

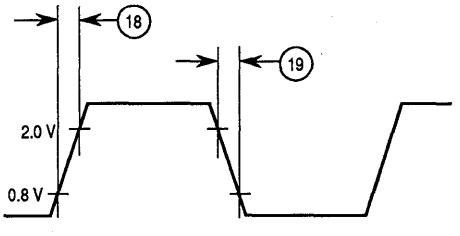
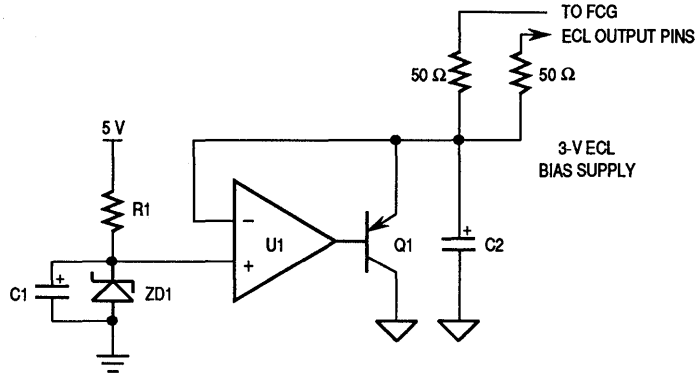


Figure 5-4. Output TTL Edge Timing

5.3.2 ECL Interface

Figure 5-5 illustrates the test load for the ECL interface pins. Since the ECL signals are differential, they are tested with a differential load. The signals must always be of opposite polarity (with respect to the logic levels) for proper operation.



R1	390 Ω
C1	1μF
C2	1μF
ZD1	1N5987B
Q1	2N3905
U1	1/4 LM324

Figure 5-5. ECL Test Load

ECL TIMING (see Figure 5-6)

Number	Parameter	Min	Max	Unit
20	ECL Rise Time	0.9	3.0	ns
21	ECL Fall Time	0.9	3.0	ns

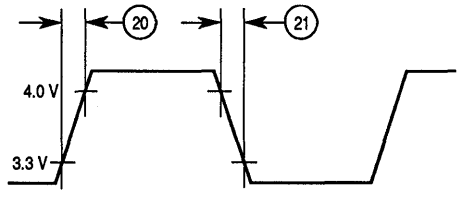


Figure 5-6. ECL Timing

SECTION 6
ORDERING INFORMATION AND MECHANICAL DATA

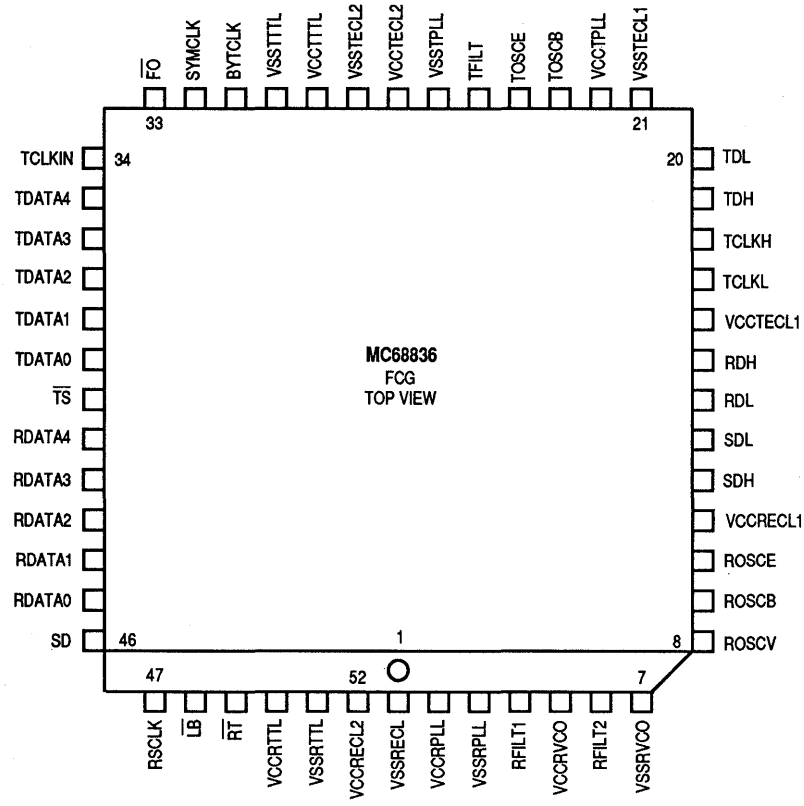
This section contains the ordering information, pin assignments, and package dimensions for the MC68836 FCG.

6.1 ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
52-Lead PLCC	25	0° to 70°C	XC68836FN

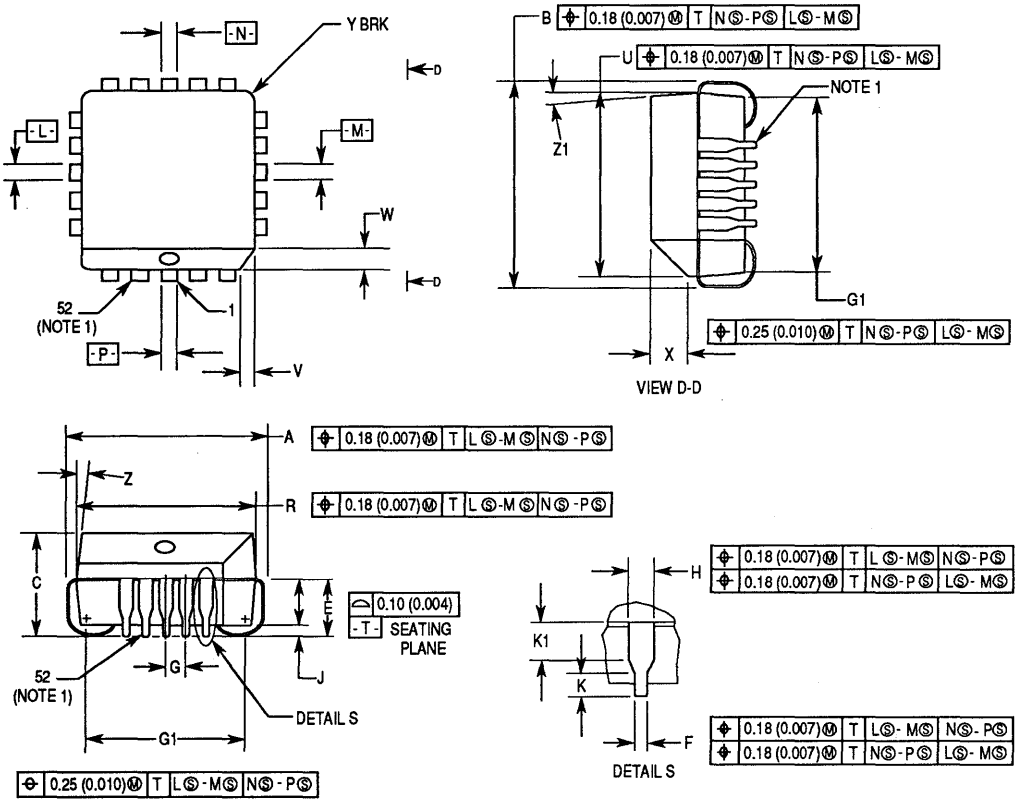
6

6.2 PIN ASSIGNMENT—52-LEAD PLASTIC LEADED CHIP CARRIER



6.3 PACKAGE DIMENSIONS

FN SUFFIX
PLASTIC LEADED
CHIP CARRIER
CASE 778-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.94	20.19	0.785	0.795
B	19.94	20.19	0.785	0.795
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	-	0.020	-
K	0.64	-	0.025	-
R	19.05	19.20	0.750	0.756
U	19.05	19.20	0.750	0.756
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	-	0.50	-	0.020
Z	2°	10°	2°	10°
G1	18.04	18.54	0.710	0.730
K1	1.02	-	0.040	-
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0. 010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

6

INDEX

I

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MOTOROLA

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