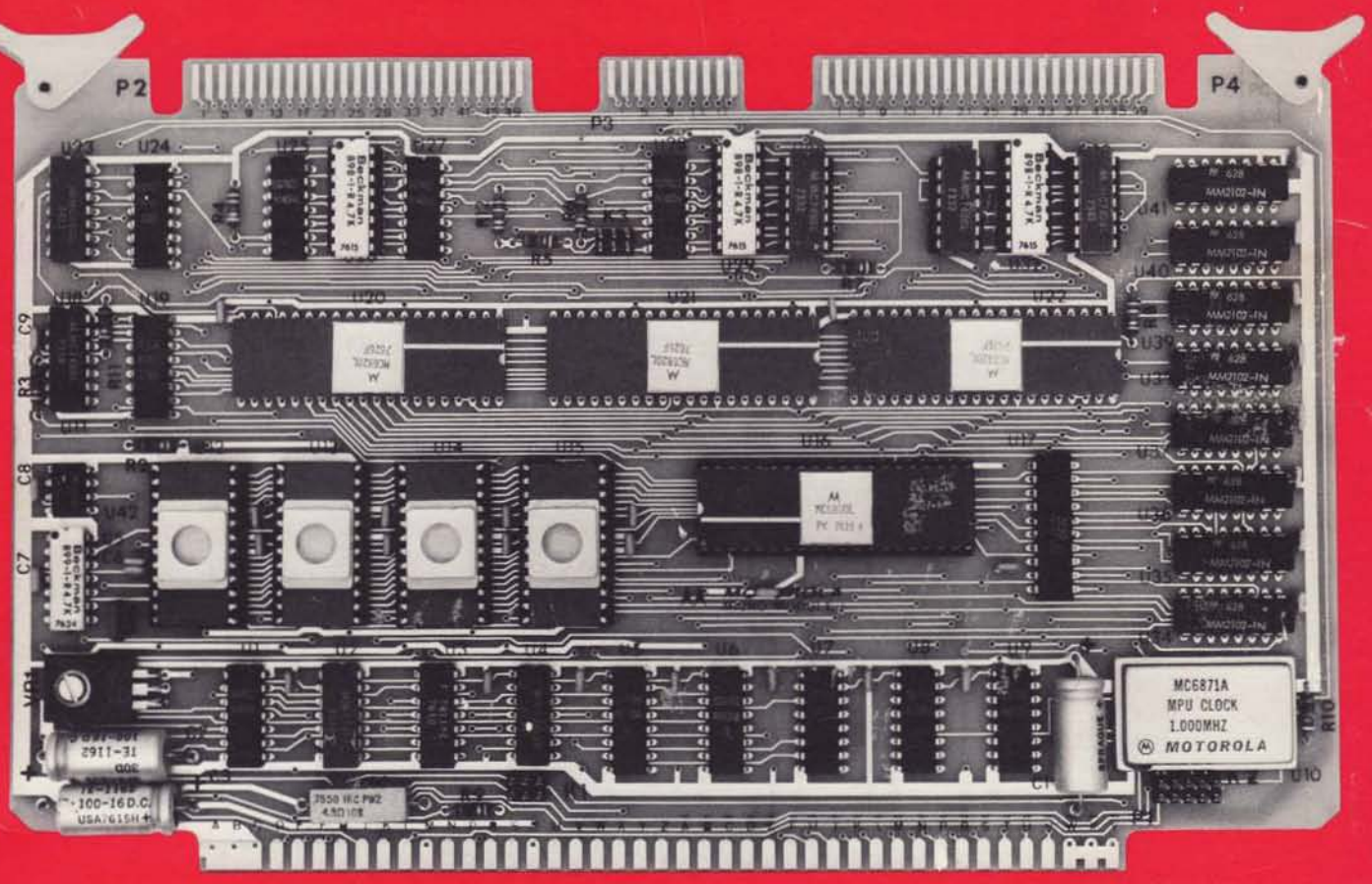
MOTOROLA

M68MM01(D4)

M68MM01

Monoboard Microcomputer 1

Micromodule 1



MICROSYSTEMS

M68MM01(D4)
April, 1979

M68MM01
MONOBOARD MICROCOMPUTER 1
MICROMODULE 1

Fourth Edition

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

Monoboard Microcomputer 1 (Micromodule 1), as shown in Figure 1-1, is a complete computer-on-a-board which will provide the OEM with a solution to most of his processing and control applications. This module, one of a family of Micromodules, contains the Microprocessor, the program EROM or ROM memory, RAM memory, programmable input/output interfaces, and the required clock, restart, bus interface, and control circuitry. All address references within this manual are shown in hexadecimal unless otherwise indicated.

1.2 FEATURES

The features of Monoboard Microcomputer 1 include:

- MC6800 Microprocessing Unit (MPU) with its associated clock oscillator, power on reset timer, and memory decoding logic.
- 1024 bytes of Random Access Memory (RAM).
- Sockets for up to 4096 bytes of Erasable Read Only Memory (EROM) or mask programmable Read Only Memory (ROM).
- Three programmable Peripheral Interface Adapter (PIA) devices providing 60 programmable Input/Output and control lines.
- Address, data, and control bus drivers to interface Monoboard Microcomputer 1 with other modules in the family or with the EXORciser.
- TTL signal level inputs and TTL signal level, three state, or open collector outputs.
- Optional mating connectors, and pullup resistors for PIA output lines (available on M68MM01-1 and M68MM01-2 only. See schematic and parts list.)

1.3 SPECIFICATIONS

Monoboard Microcomputer 1 specifications are identified in Table 1-1.

1.4 GENERAL DESCRIPTION

The Monoboard Microcomputer 1 provides the user with all of the processing and control power of an MC6800 Microprocessing Unit (MPU) working with 1K of RAM, up to 4K of EROM or ROM for programming, and three programmable Peripheral Interface Adapters (PIA). Additionally, the user has the option of interfacing Monoboard Microcomputer 1 (via its address, data, and control bus buffers) with other modules in the Micromodule family and with the EXORciser. The board also contains the required two-phase clock generator, the reset timer for power turn-on initialization, address bus decoding for establishing the addresses for each part, and the refresh circuit for use with optional external dynamic memories. The PIA's input/output signals are identified in Table 1-1.

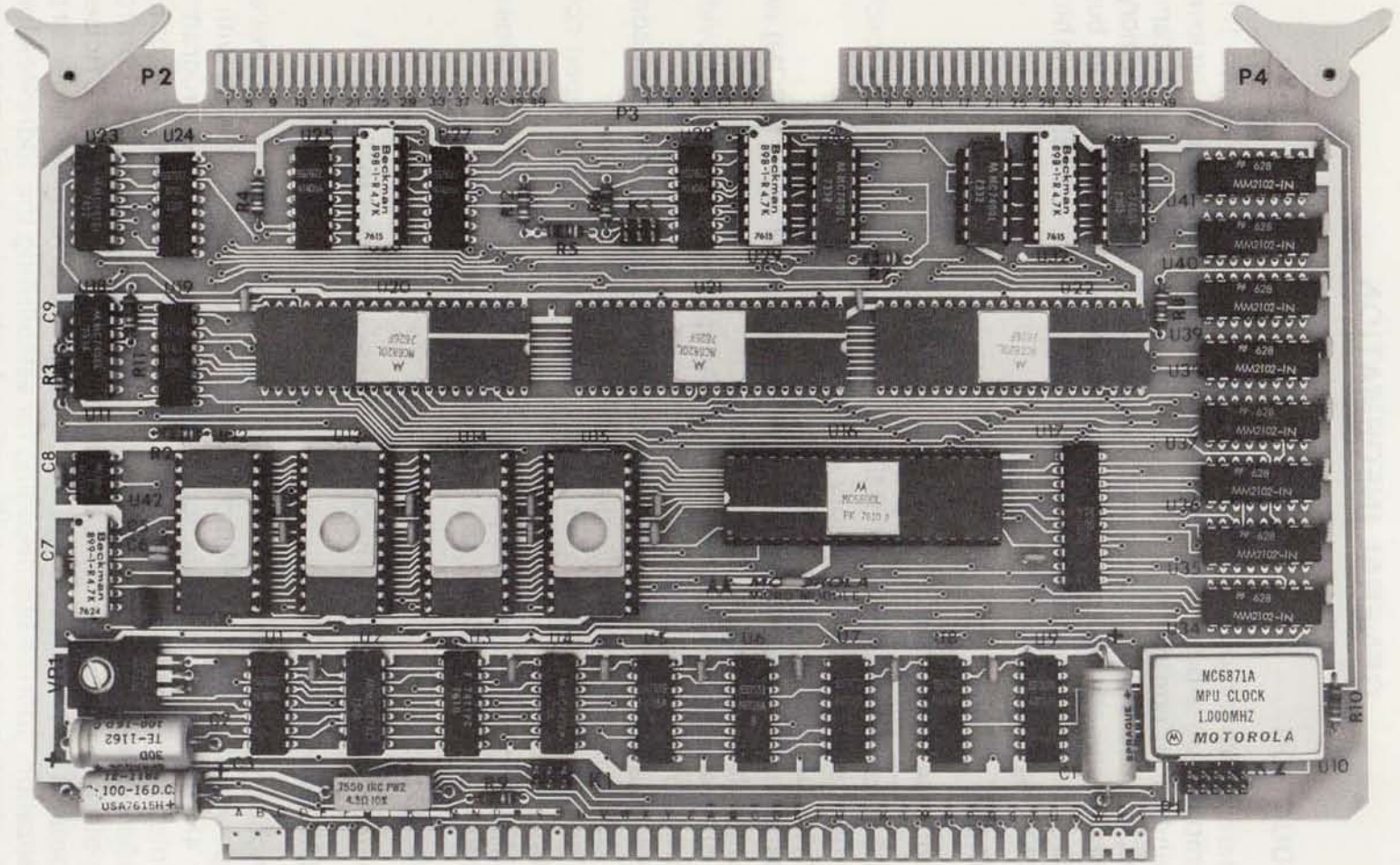


Figure 1-1. Monoboard Microcomputer 1

The 16-bit MPU address bus is decoded on the board and provides RAM (0000-03FF), the three PIA's (5800-580B) and ROM (C000-CFFF) addresses. Since these addresses are not fully decoded, there are certain nonavailable ambiguous addresses as shown in Figure 1-2. If additional Micromodules are to be used with Monoboard Microcomputer 1, their address must be selected to fall within the available memory locations(2000-4FFF and 6000-BFFF).

Monoboard Microcomputer 1 is also bus compatible with the M6800 EXORciser. This versatility provides the user with the means to develop and debug both his hardware and software and to troubleshoot production hardware. Thus, the user can take advantage of the EXORciser's optional memory and I/O modules.

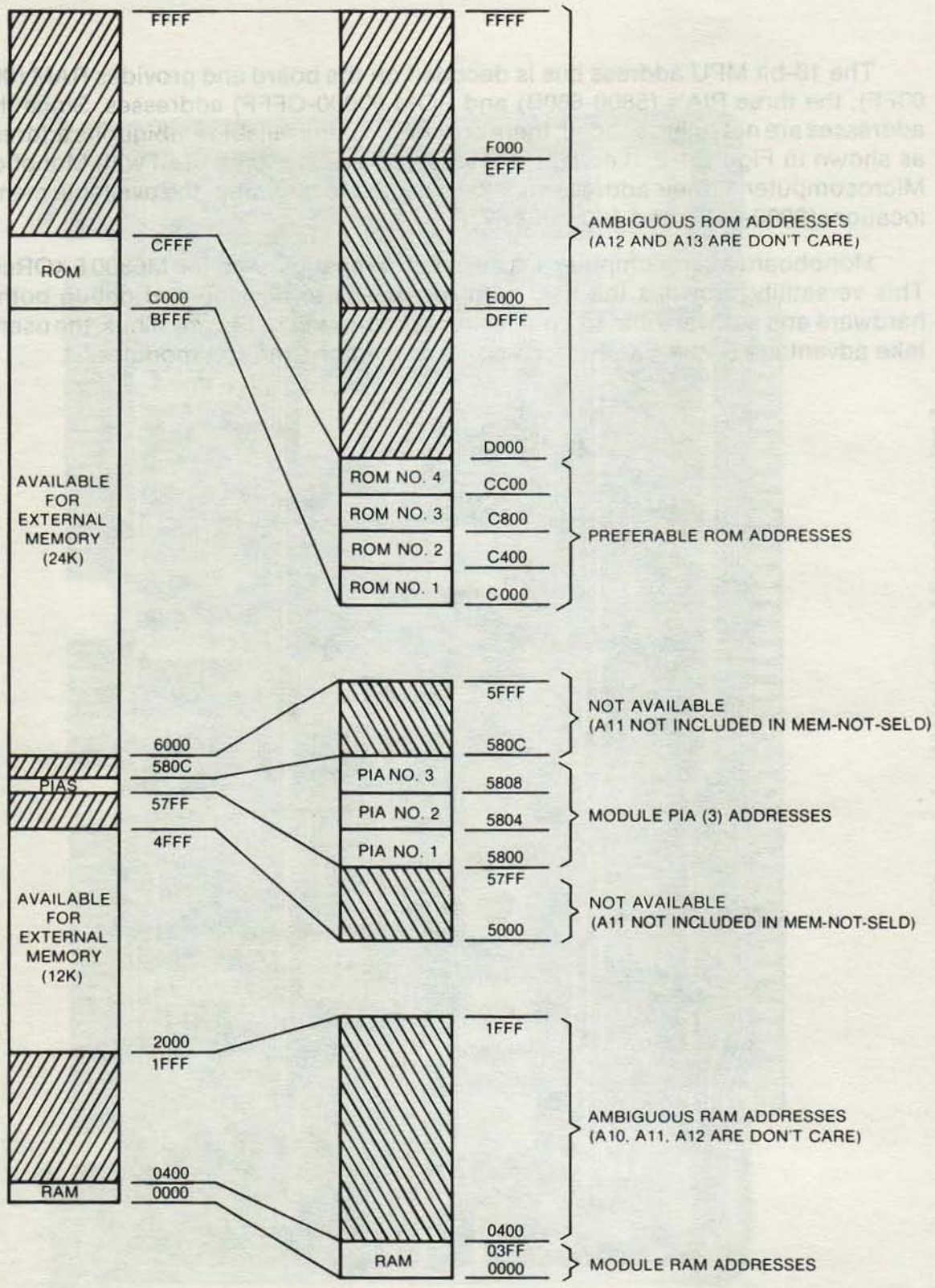


Figure 1-2. Monoboard Microcomputer 1 Address Map

Table 1-1. Monoboard Microcomputer 1 Specifications

CHARACTERISTICS	SPECIFICATIONS
Microprocessor	MC6800 MPU
Power Requirements	
Without EROMs/ROMs	+5Vdc at 1.1A(max) +12Vdc at 0mA -12Vdc at 5mA(max)
With four EROMs/ROMs	+5Vdc at 1.1A (max) +12Vdc at 260mA (max) -12Vdc at 180mA (max)
Word Size	
Data	8 bits
Address	16 bits
Instructions	8, 16, or 24 bits
Instructions	72 variable length instructions.
Addressing Modes	Seven Addressing Modes: Direct, Relative, Immediate, Indexed, Extended, Implied, and Accumulator.
Clock Signal	Crystal controlled 1 MHz with capability to work with dynamic memories.
Memory Size Capability	
ROM/EROM Memory (on board)	4K bytes of memory (sockets only)
RAM (on board)	1K byte of memory
I/O Addressing (on board)	3 MC6820 PIA 48 data lines 12 interrupt/control lines
External Memory	36K bytes available for external memory and I/O.
Interrupts	
Internal	IRQ maskable interrupt from PIA's
External	IRQ maskable interrupt and NMI nonmaskable interrupt.

Table 1-1. Monoboard Microcomputer 1 Specifications (Contd)

CHARACTERISTICS	SPECIFICATIONS
PIA1 Interface Signals	
CA1	TTL voltage compatible interrupt input with programmable active transition.
CA2	TTL voltage compatible line; programmable to act as an interrupt input or as a peripheral control output.
PA0-PA7	Eight TTL voltage compatible data lines that can be programmed to function as inputs or outputs.
CB1	TTL voltage compatible interrupt input with programmable active transition and buffered with inverting driver.
CB2	Peripheral control output buffered with inverting open-collector driver.
PB0-PB7	Eight data output lines buffered with inverting open-collector drivers.
PIA2 Interface Signals	
CA1	TTL voltage compatible interrupt input with programmable active transition.
CA2	TTL voltage compatible line; programmable to act as an interrupt input or as a peripheral control output.
PA0-PA7	Eight TTL voltage compatible data lines that can be programmed to function as inputs or outputs.
CB1	TTL voltage compatible interrupt input with programmable active transition and buffered with inverting driver.
CB2	Peripheral control output buffered with inverting open-collector driver.
PB0-PB3	Four data output lines buffered with inverting open-collector drivers.

Table 1-1. Monoboard Microcomputer 1 Specifications (Contd)

CHARACTERISTICS	SPECIFICATIONS
PB4-PB7	Four TTL voltage compatible data lines that are hardware configured inverting input or output lines. These data lines must be programmed to correspond to the optionally installed input or output buffers.
PIA3 Interface Signals	
CA1	TTL voltage compatible interrupt input with programmable active transition.
CA2	TTL voltage compatible line; programmable to act as an interrupt input or as a peripheral control output.
PA0-PA7	Eight TTL voltage compatible data lines that can be programmed to function as inputs or outputs.
CB1	TTL voltage compatible interrupt input with programmable active transition and buffered with inverting driver.
CB2	Peripheral control-output buffered with inverting open-collector driver.
PB0-PB7	Eight TTL voltage compatible data lines that are hardware configured inverting input or output lines. These data lines must be programmed to correspond to the optionally installed input or output buffers.
Line Terminators (CB2 and PB0–PB7 on all three PIA's)	Optional pull-up resistor divider or terminator (available on M68MM01-1 and M68MM01-2 only)
Operating Temperature	0° to 70°C.
Physical Characteristics	
Width x Height	9.75 in. x 6.00 in.
Board Thickness	0.062 in.
Bus Mating Connector Types	
Connector P1 (86 pin)	Stanford Applied Engineering SAC-43D/1-2 or equivalent
Connectors P2 and P4 (50 pin)	3M type 3415-0001 or equivalent
Connector P3 (20 pin)	3M type 3461-0001 or equivalent

CHAPTER 2
INSTALLATION INSTRUCTIONS, PROGRAMMING AND INTERCONNECTION CONSIDERATIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, programming, and interconnection instructions for the M68MM01 Monoboard Microcomputer 1. This chapter also discusses the module's interconnection signals.

2.2 UNPACKING INSTRUCTIONS

Unpack the Monoboard Microcomputer 1 from its shipping carton and, referring to the packing list, verify that all of the items are present. Save the packing materials for storing and reshipping of the module. If the shipping carton is damaged upon receipt, request that the carrier's agent be present while the module is being unpacked and inspected.

2.3 INSPECTION

Monoboard Microcomputer 1 should be inspected upon receipt for broken, damaged, or missing parts and physical damage to the printed circuit board.

2.4 INSTALLATION INSTRUCTIONS

Since Monoboard Microcomputer 1 is intended for user designed microcomputer based systems, no special installation instructions are provided. However, before installing the unit into the user's system or into the EXORciser, install the desired EROM or ROM devices into the appropriate sockets and remove all power from the system.

CAUTION

Inserting Monoboard Microcomputer 1 into a system while power is applied may result in damage to the components on the Micromodule.

2.5 PROGRAMMING

Development of the user's program for use with Monoboard Microcomputer 1 is quite straightforward as long as the user observes a few simple ground rules which are listed as follows:

a. The Random Access Memory (RAM) is assigned addresses 0000 through 03FF to take advantage of the direct addressing mode. Therefore, the initialization portion of the user's program should load the MPU Stack Pointer with 03FF unless an additional RAM module is used with the Micromodule.

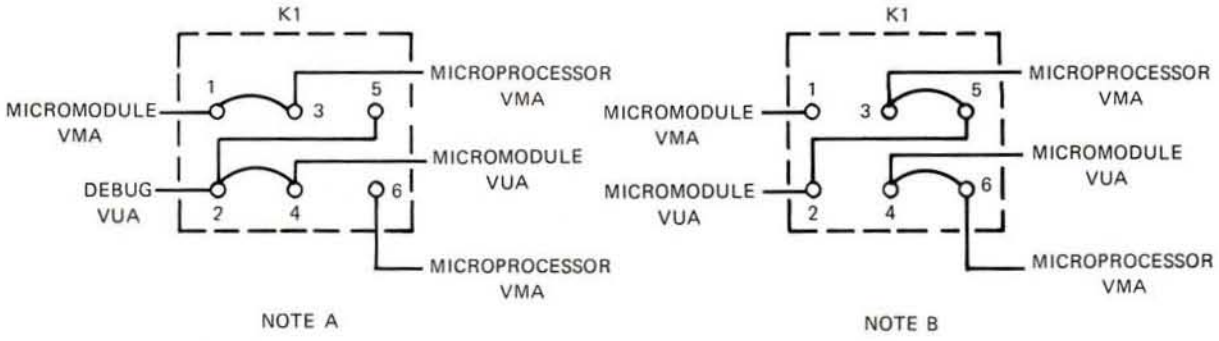
- Using the EXORciser's PROM Programmer Module to program the PROMS.
- Troubleshooting suspect systems.

2.5.2 HARDWARE PREPARATION

Three different on-board modifications provide the user with additional flexibility in using Monoboard Microcomputer 1. These modifications are described in the following paragraphs.

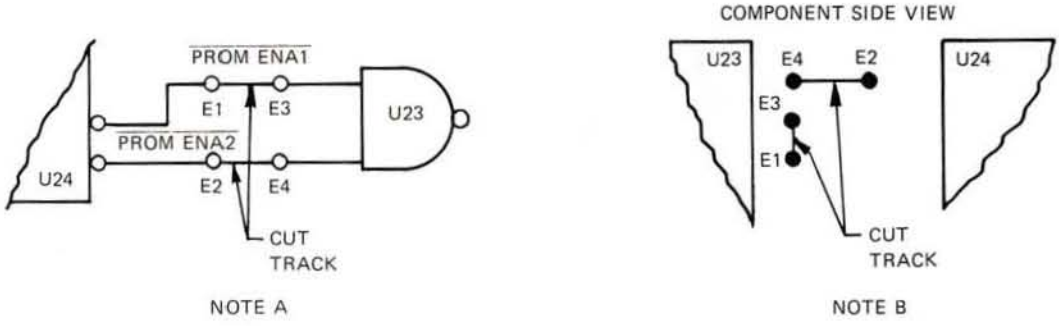
2.5.2.1 Operation With/Without Debug Module

A wirewrap socket (K1) is located on the board to configure Monoboard Microcomputer 1 for operation with the EXORciser's Debug Module (EXbug program). When operation with the Debug Module is desired, the VUA signal is supplied by the Debug Module and the jumper connections required are shown in note A. When the Debug Module is not used, the VUA signal must be the same as the VMA signal generated by the MPU. Therefore, the jumper connections required are shown in note B.



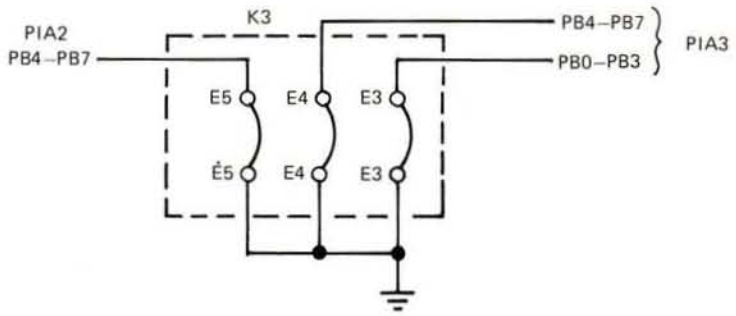
2.5.2.2 Operating with External Memory Devices

External memory devices can be used in place of the four on-board EROM devices by cutting the printed circuit wiring between terminals (E1/E3 and E2/E4) on the board. These terminals also permit the user to use jumper wires to reconnect the circuit for using the on-board EROM devices. This change is presented in schematic form in note A and in hardware form in note B.



2.5.2.3 Operating With Optional Input Configuration

As delivered, the section B peripheral data lines (PBO-PB7) of the three PIAs (U20, U21 and U22) are configured as outputs. Data lines PB4 through PB7 of PIA2 and PBO through PB7 of PIA3, however, may be reconfigured as inputs by replacing the socket mounted MC7400 devices (U30, U31 and U33) with MC7402 devices and connecting jumper wires to wire-wrap socket K3 as shown below.



2.5.3 PIA PROGRAMMING INFORMATION

The MPU addresses the PIAs as if they were memory. Therefore, all commands to the PIAs are executed by the MPU as memory reference instructions. The M6800 Microprocessor Applications Manual illustrates the PIA addressing and the operation being performed on the selected PIA register. Note that bit 2 of the PIA control register is used to specify either the PIA's peripheral interface registers or the data direction register. The proper state of the CRA2 and CRB2 bit must be loaded into the corresponding PIA control register before addressing its peripheral interface or direction register. For additional PIA programming information and considerations, refer to the M6800 Microprocessor Applications Manual.

2.5.4 $\overline{IRQ}$ (INTERRUPT REQUEST) AND INTERRUPT PRIORITIES

Monoboard Microcomputer 1 has seven potential sources of generating an $\overline{IRQ}$ input to the MPU; two from each of the three PIAs (depending on the user's program) and an available user input on the control bus. The MPU completes the instruction it is executing before it recognizes an $\overline{IRQ}$ input. Then, if the interrupt mask bit in the MPU's condition code register is not set, the MPU reads the vector address of the user's $\overline{IRQ}$ routine in memory locations CFF8 and CFF9.

If you are using more than one peripheral device capable of interrupting the MPU, you must prepare a software interrupt polling routine to interrogate each of these devices and determine the device initiating the interrupt. This polling routine, on determining the $\overline{IRQ}$ initiated device, causes the MPU to vector to the appropriate service routine.

In preparing the interrogation routine, you must assign priorities to the devices by assigning their position in the interrogation polling routine. The device interrogated first has the highest priority and the device interrogated last has the lowest priority.

2.6 MODULE INTERCONNECTIONS

Monoboard Microcomputer 1 is bus compatible with either the Micromodule bus or the EXORciser bus. These bus signals are identified in Table 2-1. This table lists each pin connection, signal mnemonic, and signal characteristic. Tables 2-2 through 2-4 identify the various PIA interface signals.

Table 2-1. Connector P1 Bus Interface Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
A, B, C	+5 VDC	+5 Vdc - Used for the module's logic circuits.
D	$\overline{IRQ}$	INTERRUPT REQUEST - This low level sensitive input signal requests that a MPU interrupt sequence be generated within the machine. The MPU will wait until it completes the instruction being executed before it recognizes the request. At that time, if the interrupt mask bit in the MPU condition code register is not set, the MPU will begin the interrupt sequence.
E	$\overline{NMI}$	NON-MASKABLE INTERRUPT - This low-going edge sensitive input signal requests that a non-maskable interrupt be generated within the machine. The MPU will wait until it completes the instruction being executed before it recognizes the $\overline{NMI}$ signal. At that time, the MPU will begin its non-maskable interrupt sequence.
F	VMA	VALID MEMORY ADDRESS - This output is available, jumper-selected, when Monoboard Microcomputer 1 is used with the EXORciser Debug Module to indicate that there is a valid memory address on the address bus. This pin is not used when Monoboard Microcomputer 1 is not configured for operation with the Debug Module.
H		Not Used.
J	$\phi 2$	Phase 2 clock signal.
K		Not Used.
L	MEMCLK	MEMORY CLOCK - This signal is an ungated TTL level$\phi 2$ clock used to refresh any dynamic memory used in the system
M	-12 VDC	-12 Vdc - Used to generate the -5 Vdc required by the Erasable Read Only Memories (EROM's).

Table 2-1. Connector P1 Bus Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
N		Not Used
P	BA	BUS AVAILABLE - This output signal will normally be a low level. When activated, it will go high indicating the MPU has halted and the address bus is available. This will occur if the Go/Halt line is in the Halt (low) state or the MPU is in the Wait state as a result of executing a Wait instruction. At such time, all the MPU three-state output drivers will go to their off (high impedance) state and other outputs to their normally inactive state. A maskable interrupt or non-maskable interrupt removes the MPU from the Wait state.
R, S		Not Used
T	+12 VDC	+12 Vdc - Used by the Erasable Read Only Memories (EROM's).
U-Z		Not Used.
$\overline{A}$-$\overline{F}$		Not Used.
$\overline{H}$	$\overline{D3}$	DATA bus (bit 3) - This bi-directional line, when enabled, provides a two-way data transfer between Monoboard Microcomputer 1 and any other plug-in modules in the system.
$\overline{J}$	$\overline{D7}$	DATA bus (bit 7) - Same as $\overline{D3}$ on P1-$\overline{H}$.
$\overline{K}$	$\overline{D2}$	DATA bus (bit 2) - Same as $\overline{D3}$ on P1-$\overline{H}$.
$\overline{L}$	$\overline{D6}$	DATA bus (bit 6) - Same as $\overline{D3}$ on P1-$\overline{H}$.
$\overline{M}$	A14	ADDRESS bus (bit 14) - This output address line, when enabled, allows the MPU to address any external memory locations used in the system.
$\overline{N}$	A13	ADDRESS bus (bit 13) - Same as A14 on P1-$\overline{M}$.
$\overline{P}$	A10	ADDRESS bus (bit 10) - Same as A14 on P1-$\overline{M}$.

Table 2-1. Connector P1 Bus Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
$\overline{R}$	A9	ADDRESS bus (bit 9) - Same as A14 on P1-$\overline{M}$.
$\overline{S}$	A6	ADDRESS bus (bit 6) - Same as A14 on P1-$\overline{M}$.
$\overline{T}$	A5	ADDRESS bus (bit 5) - Same as A14 on P1-$\overline{M}$.
$\overline{U}$	A2	ADDRESS bus (bit 2) - Same as A14 on P1-$\overline{M}$.
$\overline{V}$	A1	ADDRESS bus (bit 1) - Same as A14 on P1-$\overline{M}$.
$\overline{W}$, $\overline{X}$, $\overline{Y}$	COM	COMMON (ground)
1, 2, 3	+5 VDC	+5 Vdc - Used for the modules's logic circuits.
4	G/H	GO/HALT - When this input is in the high state, the MPU will fetch the instruction addressed by the program counter and start execution. When low, all activity in the MPU will be halted. This input is level sensitive. In the Halt mode, the MPU will stop at the end of an instruction, Bus Available will be at a high level, Valid Memory Address will be at a low level, and all other three-state lines will be in their off or high impedance state. The Halt line must go low with the leading edge of the phase one clock (ϕ1) to insure single instruction operation. If the Halt line does not go low with the leading edge of the phase one clock, one or two instruction operations may result, depending on when the halt line goes low relative to the phasing of the clock.
5	$\overline{\text{RESET}}$	RESET - This buffered input/output signal, when used as an output, provides Monoboard Microcomputer 1 reset circuit output to any external devices requiring a $\overline{\text{Reset}}$ signal. An external switch closure to ground may be applied to this pin to restart Monoboard Microcomputer 1.
6	R/W	READ/WRITE - This MPU output signal indicates to any external plug-in modules

Table 2-1. Connector P1 Bus Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
6 (contd)		whether the MC6800 MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Also, when the MC6800 is halted, this signal will be in the read state.
7, 8, 9		Not Used.
10	VUA	VALID USER'S ADDRESS - When Monoboard Microcomputer 1 is not being used with the EXORciser Debug Module, this pin is connected with a jumper to the buffered Valid Memory Address (VMA) signal. When Monoboard Microcomputer 1 is configured for use with the Debug Module, VUA is supplied as an input by the Debug Module.
11	-12 VDC	-12 Vdc - Same as -12 Vdc on P1-M.
12	$\overline{\text{REFREQ}}$	REFRESH REQUEST - This input signal, when low, initiates a memory refresh cycle of the dynamic memory modules. During the refresh operation, the clock circuit is inhibited from generating its $\phi 1$ and $\phi 2$ MPU clock signals but still generates the MEMCLK signal.
13	REF GRANT	REFRESH GRANT - This output signal, when high, instructs the dynamic memory modules to refresh their memories.
14, 15		Not Used
16	+12 VDC	+12 Vdc - Same as +12 Vdc on P1-T.
17-28		Not Used
29	$\overline{\text{D1}}$	DATA bus (bit 1) - Same as D3 on P1-$\overline{\text{H}}$.
30	$\overline{\text{D5}}$	DATA bus (bit 5) - Same as D3 on P1-$\overline{\text{H}}$.
31	$\overline{\text{D0}}$	DATA bus (bit 0) - Same as D3 on P1-$\overline{\text{H}}$.
32	$\overline{\text{D4}}$	DATA bus (bit 4) - Same as D3 on P1-$\overline{\text{H}}$.
33	A15	ADDRESS bus (bit 15) - Same as A14 on P1-$\overline{\text{M}}$.

Table 2-1. Connector P1 Bus Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
34	A12	ADDRESS bus (bit 12) - Same as A14 on P1-$\overline{M}$.
35	A11	ADDRESS bus (bit 11) - Same as A14 on P1-$\overline{M}$.
36	A8	ADDRESS bus (bit 8) - Same as A14 on P1-$\overline{M}$.
37	A7	ADDRESS bus (bit 7) - Same as A14 on P1-$\overline{M}$.
38	A4	ADDRESS bus (bit 6) - Same as A14 on P1-$\overline{M}$.
39	A3	ADDRESS bus (bit 3) - Same as A14 on P1-$\overline{M}$.
40	A0	ADDRESS bus (bit 0) - Same as A14 on P1-$\overline{M}$.
41, 42, 43	COM	COMMON (ground)

Table 2-2. Connector P2 PIA Interface Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
1	PA0-1	PERIPHERAL data line (section A, bit 0, PIA1) - This peripheral data line in Section A of PIA1 (U20) can be programmed to act either as an input line or as an output line. A "0" in bit 0 of the A data direction register causes this line to function as an input and a "1" causes this line to function as an output.
2	GND	GROUND - Signal return line.
3	PA1-1	PERIPHERAL data line (Section A, bit 1, PIA1) - Same as PA0-1 on pin 1 except bit 1 of the A data direction register controls this line.
4	GND	GROUND - Signal return line.
5	PA2-1	PERIPHERAL data line (Section 1, bit 2, PIA1) - Same as PA0-1 on pin 1 except bit 2 of the A data direction register controls this line.
6	GND	GROUND - Signal return line.
7	PA3-1	PERIPHERAL data line (Section A, bit 3, PIA1) - Same as PA0-1 on pin 1 except bit 3 of the A data direction register controls this line.
8	GND	GROUND - Signal return line.
9	PA4-1	PERIPHERAL data line (Section A, bit 4, PIA1) - Same as PA0-1 on pin 1 except bit 4 of the A data direction register controls this line.
10	GND	GROUND - Signal return line.
11	PA5-1	PERIPHERAL data line (Section A, bit 5, PIA1) - Same as PA0-1 on pin 1 except bit 5 of the A data direction register controls this line.
12	GND	GROUND - Signal return line.
13	PA6-1	PERIPHERAL data line (Section A, bit 6, PIA1) - Same as PA0-1 on pin 1

Table 2-2. Connector P2 PIA Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
13 (Contd)		except bit 6 of the A data direction register controls this line.
14	GND	GROUND - Signal return line.
15	PA7-1	PERIPHERAL data line (Section A, bit 7, PIA1) - Same as PA0-1 on pin 1 except bit 7 of the A data direction register controls this line.
16	GND	GROUND - Signal return line.
17	PB0-1	PERIPHERAL data line (Section B, bit 0, PIA1) - Negative true buffered output. This peripheral data line in Section B of PIA1 (U20) must be programmed to operate as an output line. A "1" in bit 0 of the B data direction register causes this line to function as an output.
18	GND	GROUND - Signal return line.
19	PB1-1	PERIPHERAL data line (Section B, bit 1, PIA1) - Same as PB0-1 on pin 17 except bit 1 of the B data direction register controls this line.
20	GND	GROUND - Signal return line.
21	PB2-1	PERIPHERAL data line (Section B, bit 2, PIA1) - Same as PB0-1 on pin 17 except bit 2 of the B data direction register controls this line.
22	GND	GROUND - Signal return line.
23	PB3-1	PERIPHERAL data line (Section B, bit 3, PIA1) - Same as PB0-1 on pin 17 except bit 3 of the B data direction register controls this line.
24	GND	GROUND - Signal return line.
25	PB4-1	PERIPHERAL data line (Section B, bit 4, PIA1) - Same as PB0-1 on pin 17 except bit 4 of the B data direction register controls this line.

Table 2-2. Connector P2 PIA Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
26	GND	GROUND - Signal return line.
27	PB5-1	PERIPHERAL data line (Section B, bit 5, PIA1) - Same as PB0-1 on pin 17 except bit 5 of the B data direction register controls this line.
28	GND	GROUND - Signal return line.
29	PB6-1	PERIPHERAL data line (Section B, bit 6, PIA1) - Same as PB0-1 on pin 17 except bit 6 of the B data direction register controls this line.
30	GND	GROUND - Signal return line.
31	PB7-1	PERIPHERAL data line (Section B, bit 7, PIA1) - Same as PB0-1 on pin 17 except bit 7 of the B data direction register controls this line.
32	GND	GROUND - Signal return line.
33	PA0-2	PERIPHERAL data line (Section A, bit 0, PIA2) -This peripheral data line in Section A of PIA2 (U21) can be programmed to act either as an input line or as an output line. A "0" in bit 0 of the A data direction register causes this line to function as an input and a "1" causes this line to function as an output.
34	GND	GROUND - Signal return line.
35	PA1-2	PERIPHERAL data line (Section A, bit 2, PIA2) - Same as PA0-2 on pin 33 except bit 1 of the A data direction register controls this line.
36	GND	GROUND - Signal return line.
37	PA2-2	PERIPHERAL data line (Section A, bit 2, PIA2) - Same as PA0-2 on pin 33 except bit 2 of the A data direction register controls this line.
38	GND	GROUND - Signal return line.

Table 2-3. Connector P3 PIA Interface Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
1	CA2-1	Peripheral CONTROL line (line CA2, PIA1) - This peripheral control line on PIA1 (U20) may be programmed to operate as an interrupt input line or as a peripheral control output line. The function of this line is program controlled by the A control register.
2	GND	GROUND - Signal return line.
3	CB1-1	Peripheral CONTROL line (line CB1, PIA1) - Negative true buffered input. This peripheral control line of PIA1 (U20) is an input line that sets the interrupt flag of the B control register. The active transition of the signal is program controlled by the B control register.
4	GND	GROUND - Signal return line.
5	CB2-1	Peripheral CONTROL line (line CB2, PIA1) - Negative true buffered output. This peripheral control line of PIA1 (U20) must be programmed to operate as a peripheral control output line. The function of this line is program controlled by the B control register.
6	GND	GROUND - Signal return line.
7	CA1-2	Peripheral CONTROL line (line CA1, PIA2) - This peripheral control line on PIA2 (U21) is an input line that sets the interrupt flag of the A control register. The active transition of this signal is program controlled by the A control register.
8	GND	GROUND - Signal return line.
9	CA2-2	Peripheral CONTROL line (line CA2, PIA2) - This peripheral control line on PIA2 (U21) may be programmed to operate as an interrupt control output line. The function of this line is program controlled by the A control register.

Table 2-3. Connector P3 PIA Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
10	GND	GROUND - Signal return line.
11	CB1-2	Peripheral CONTROL line (line CB1, PIA2) - Negative true buffered input. This peripheral control line of PIA2 (U21) is an input line that sets the interrupt flag of the B control register. The active transition of the signal is program controlled by the B control register.
12	GND	GROUND - Signal return line.
13	CB2-2	Peripheral CONTROL line (line CB2, PIA2) - Negative true buffered input. This peripheral control line of PIA2 (U21) is an input line that sets the interrupt flag of the B control register. The active transition of the signal is program controlled by the B control register.
14	GND	GROUND - Signal return line.
15	CA1-3	Peripheral CONTROL line (line CA1, PIA3) - Negative true buffered input. This peripheral control line on PIA3 (U22) is an input line that sets the interrupt flag of the A control register. The active transition of the signal is program controlled by the A control register.
16	GND	GROUND - Signal return line.
17	CA2-3	Peripheral CONTROL line (line CA2, PIA3) - Negative true buffered input. This peripheral control line of PIA3 (U22) is an input line that sets the interrupt flag of the B control register. The active transition of the signal is program controlled by the B control register.
18	GND	GROUND - Signal return line.

Table 2-3. Connector P3 PIA Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
19	CB1-3	Peripheral CONTROL line (line CB1, PIA3) - Negative true buffered input. This peripheral control line of PIA3 (U22) is an input line that sets the interrupt flag of the B control register. The active transition of the signal is program controlled by the B control register.
20	GND	GROUND - Signal return line.

Table 2-4. Connector P4 PIA Interface Signals

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
1	PB0-2	PERIPHERAL data line (section B, bit 0, PIA2) - Negative True Buffered Output. This peripheral data line in the B section of PIA2 (U30) must be programmed to operate as an output. A "1" in bit 0 of the B data direction register causes this line to function as an output.
2	GND	GROUND - Signal return line.
3	PB1-2	PERIPHERAL data line (section B, bit 1, PIA2) - Same as PB0-2 on pin 1 except bit 1 of the B data direction register controls this line.
4	GND	GROUND - Signal return line.
5	PB2-2	PERIPHERAL data line (section B, bit 2, PIA2) - Same as PB0-2 on pin 1 except bit 2 of the B data direction register controls this line.
6	GND	GROUND - Signal return line.
7	PB3-2	PERIPHERAL data line (section B, bit 3, PIA2) - Same as PB0-3 on pin 1 except bit 3 of the B data direction register controls this line.
8	GND	GROUND - Signal return line.
9	PB4-2	PERIPHERAL data line (section B, bit 4, PIA2) - Negative True Buffered Input/Output. This peripheral data line in section B of PIA2 (U21) can be programmed to operate either as an input line (option) or as an output line (as delivered). A "0" in bit 4 of the B data direction register causes this line to function as an input and a "1" causes this line to function as an output. Through the installation of the appropriate device and jumper connections on the module, this line is hardware configured to function as an input or as an output

Table 2-4. Connector P4 PIA Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
10	GND	GROUND - Signal return line.
11	PB5-2	PERIPHERAL data line (section B, bit 5, PIA2) - Same as PB4-2 on pin 9 except bit 5 of the B data direction register controls this line.
12	GND	GROUND - Signal return line.
13	PB6-2	PERIPHERAL data line (section B, bit 6, PIA2) - Same as PB4-2 on pin 9 except bit 6 of the B data direction register controls this line.
14	GND	GROUND - Signal return line.
15	PB7-2	PERIPHERAL data line (section B, bit 7, PIA2) - Same as PB4-2 on pin 9 except bit 7 of the B data direction register controls this line.
16	GND	GROUND - Signal return line.
17	PA0-3	PERIPHERAL data line (section A, bit 0, PIA3) - This peripheral data line in section A of PIA3 (U22) can be programmed to act either as an input line or as an output line. A "0" in bit 0 of the A data direction register causes this line to function as an input and a "1" causes this line to function as an output.
18	GND	GROUND - Signal return line.
19	PA1-3	PERIPHERAL data line (section A, bit 1, PIA3) - Same as PA0-3 on pin 17 except bit 1 of the A data direction register controls this line.
20	GND	GROUND - Signal return line.
21	PA2-3	PERIPHERAL data line (section A, bit 2, PIA3) - Same as PA0-3 on pin 17 except bit 2 of the A data direction register controls this line.
22	GND	GROUND - Signal return line.

Table 2-4. Connector P4 PIA Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
23	PA3-3	PERIPHERAL data line (section A, bit 3, PIA3) - Same as PA0-3 on pin 17 except bit 3 of the A data direction register controls this line.
24	GND	GROUND - Signal return line.
25	PA4-3	PERIPHERAL data line (section A, bit 4, PIA3) - Same as PA0-3 on pin 17 except bit 4 of the A data direction register controls this line.
26	GND	GROUND - Signal return line.
27	PA5-3	PERIPHERAL data line (section A, bit 5, PIA3) - Same as PA0-3 on pin 17 except bit 5 of the A data direction register controls this line.
28	GND	GROUND - Signal return line.
29	PA6-3	PERIPHERAL data line (section A, bit 6, PIA3) - Same as PA0-3 on pin 17 except bit 6 of the A data direction register controls this line.
30	GND	GROUND - Signal return line.
31	PA7-3	PERIPHERAL data line (section A, bit 7, PIA3) - Same as PA0-3 on pin 17 except bit 7 of the A data direction register controls this line.
32	GND	GROUND - Signal return line.
33	PB0-3	PERIPHERAL data line (section B, bit 0, PIA3) - Negative True Buffered Input/Output. This peripheral data line in section B of PIA3 (U22) can be programmed to operate either as an input line (option) or as an output line (as delivered). A "0" in bit 0 of the B data direction register causes this line to function as an input and a "1" causes this line to function as an output. Through the installation of the appropriate device

Table 2-4. Connector P4 PIA Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
33 (contd)		and jumper connections, this line is hardware configured to function as an input or as an output.
34	GND	GROUND - Signal return line.
35	PB1-3	PERIPHERAL data line (section B, bit 1, PIA3) - Same as PB0-3 on pin 33 except bit 1 in the B data direction register controls this line.
36	GND	GROUND - Signal return line.
37	PB2-3	PERIPHERAL data line (section B, bit 2, PIA3) - Same as PB0-3 on pin 33 except bit 2 in the B data direction register controls this line.
38	GND	GROUND - Signal return line.
39	PB3-3	PERIPHERAL data line (section B, bit 3, PIA3) - Same as PB0-3 on pin 33 except bit 3 in the B data direction register controls this line.
40	GND	GROUND - Signal return line.
41	PB4-3	PERIPHERAL data line (section B, bit 4, PIA3) - Same as PB0-3 on pin 33 except bit 4 in the B data direction register controls this line.
42	GND	GROUND - Signal return line.
43	PB5-3	PERIPHERAL data line (section B, bit 5, PIA3) - Same as PB0-3 on pin 33 except bit 5 in the B data direction register controls this line.
44	GND	GROUND - Signal return line.
45	PB6-3	PERIPHERAL data line (section B, bit 6, PIA3) - Same as PB0-3 on pin 33 except bit 6 in the B data direction register controls this line.
46	GND	GROUND - Signal return line.

Table 2-4. Connector P4 PIA Interface Signals (Contd)

PIN NUMBER	SIGNAL MNEMONICS	SIGNAL NAME AND DESCRIPTION
47	PB7-3	PERIPHERAL data line (section B, bit 7, PIA3) - Same as PB0-3 on pin 33 except bit 7 in the B data direction register controls this line.
48	GND	GROUND - Signal return line.
49	CB2-3	Peripheral CONTROL line (line CB2, PIA3) - Negative True Buffered Output. This peripheral control line of PIA3 (U22) must be programmed to operate as a peripheral control output line. The function of this line is program controlled by the B control register.
50	GND	GROUND - Signal return line.

CHAPTER 3
THEORY OF OPERATION

3.1 INTRODUCTION

This chapter provides a block diagram description of Monoboard Microcomputer 1. A block diagram is shown in Figure 3-1, while a schematic diagram is included in Figure 3-2.

3.2 BLOCK DIAGRAM DESCRIPTION

The restart circuit generates a low level $\overline{\text{RESET}}$ signal approximately 500 milliseconds after power is initially applied to Monoboard Microcomputer 1. This Micromodule is also capable of receiving an external $\overline{\text{RESET}}$ command via the Micromodule control bus. The $\overline{\text{RESET}}$ signal instructs the MC6800 Microprocessing Unit (MPU) to perform its initialization routine. This signal also resets the three PIAs.

The clock circuit generates the two non-overlapping clock signals (ϕ1 and ϕ2) required by the MPU. In addition, the ϕ1 clock pulse is inverted to produce the DBE (Data Bus Enable) signal. The DBE signal is applied to the MPU and to the read/write control circuit. The clock circuit also applies the ϕ2 clock signal to the PIA's and to the read/write control circuit. These signals (ϕ1, ϕ2, and DBE) enable the MPU to transfer data on the data bus during the ϕ2 clock time.

The refresh control flip-flop works in conjunction with the clock circuit to provide a dynamic memory refresh capability for any dynamic RAM module used within the system. Since Monoboard Microcomputer 1 incorporates only static type RAM devices, this refresh capability is not required. However, for any dynamic RAM module that might be used, this capability has been included. To initiate a refresh operation, the requesting module places a low level $\overline{\text{RR}}$ (Refresh Request) command on the Micromodule control bus. When the clock circuit produces the next MEM CLK (Memory Clock) pulse, the refresh control flip-flop loads the $\overline{\text{RR}}$ command and produces a low level Hold 1 command and a high level RG (Refresh Grant) command. The low level Hold 1 command is applied to the clock circuit, holding the ϕ1 clock output signal at a high level and the ϕ2 clock output signals at a low level. This temporarily halts the MPU. Note that this does not halt the MEM CLK output of the clock circuit. The high level RG command is supplied to the module initiating the refresh operation. This command instructs the requesting memory module to refresh itself using the MEM CLK signal and to remove the low level $\overline{\text{RR}}$ command from the control bus after the refresh operation has been completed. When the low level $\overline{\text{RR}}$ command is removed, the clock circuit is enabled to generate the ϕ1 and ϕ2 clock signals.

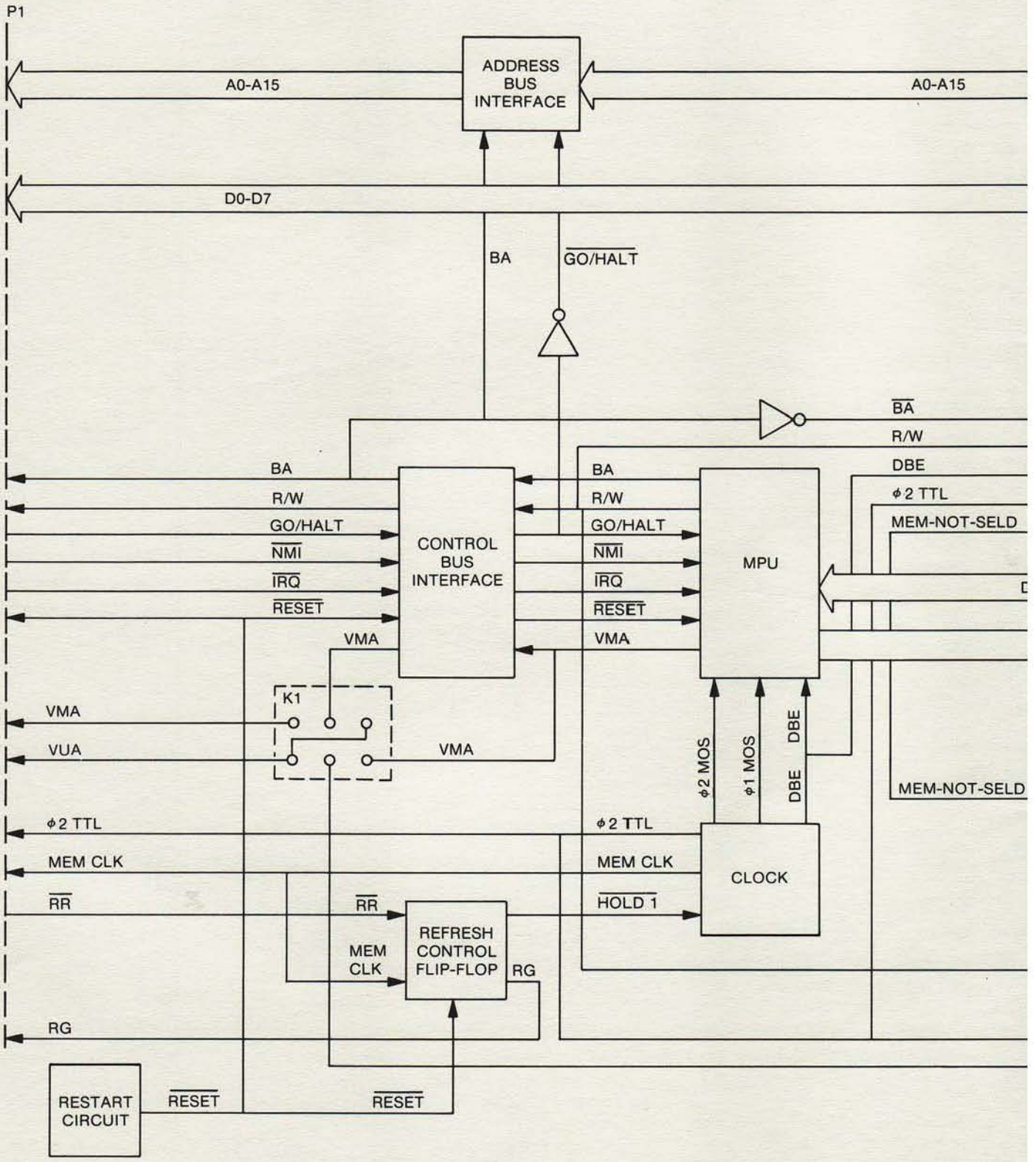
The Micromodule data bus is used to perform all data transfers between the MPU and the various memory devices (EROM/ROM, RAM, and PIA). Several each of these memory devices are located on Monoboard Microcomputer 1 with the capability of

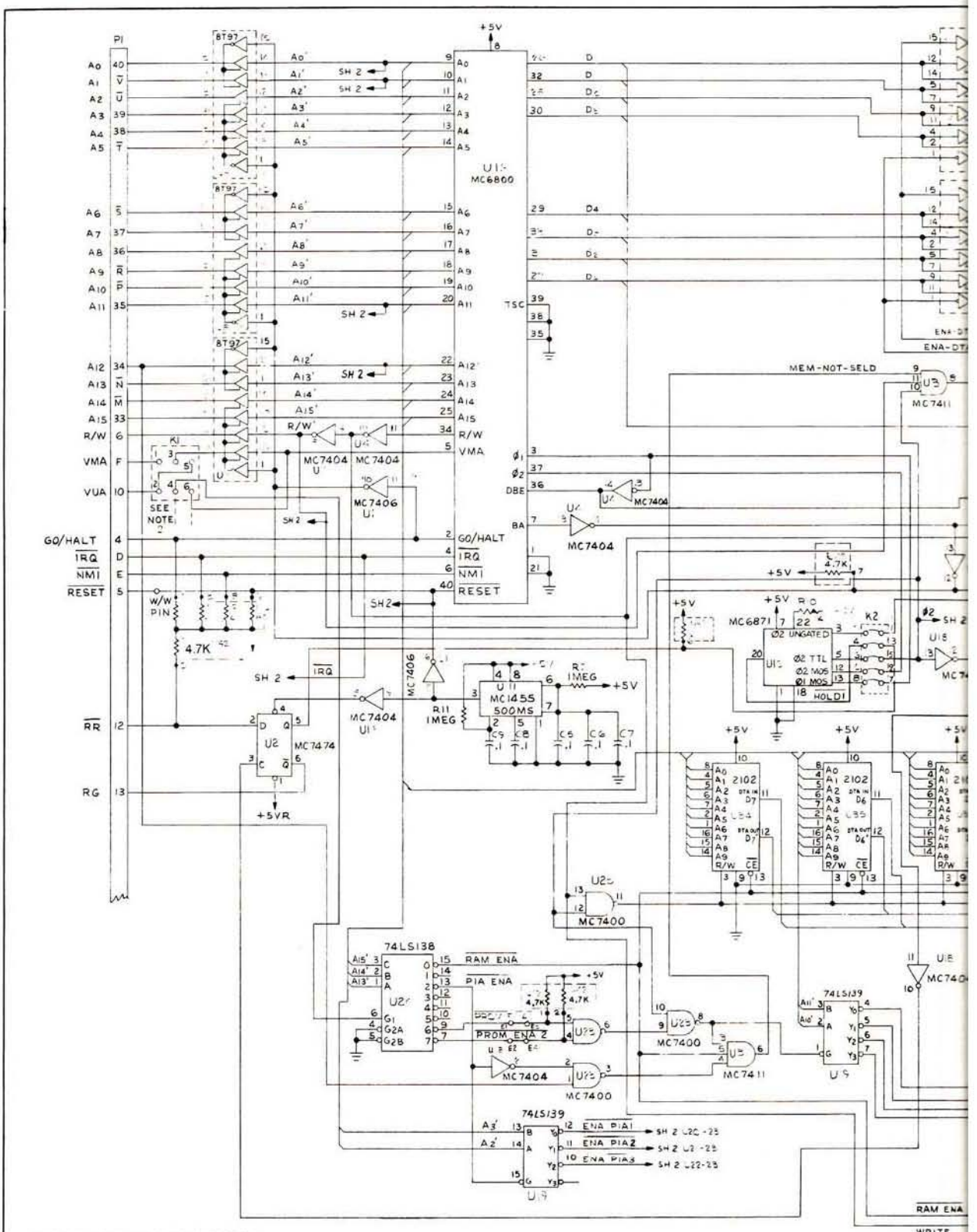
more memory devices being located externally to this module. However, all data transfers between Monoboard Microcomputer 1 and externally located memory devices must be made via the data bus interface. All of these data transfers are controlled by the read/write control circuit. During an MPU read operation, the MPU generates a high level R/W signal which is applied to the read/write control circuit. If none of the memory devices (EROM/ROM, RAM, or PIA) located on Monoboard Microcomputer 1 are selected (high level MEM-NOT-SELD signal), the read/write control circuit will generate a low level ENA-DTA-IN signal on the next low to high transition of the $\phi 2$ clock pulse. The low ENA-DTA-IN signal will enable only the input data buffers in the data bus interface. Data is then read into the MPU. During an MPU write operation, the MPU generates a low level R/W signal. If the BA (Bus Available) signal output of the MPU is also a low level (indicating that the address bus is being used), then the read/write circuit will generate a high level ENA-DTA-OUT signal on the next low to high transition of DBE signal. (Remember that the DBE signal is the inverse of the $\phi 1$ clock signal.) The high ENA-DTA-OUT signal will enable only the output data buffers in the data bus interface. Data is then written out of the MPU.

The Micromodule address bus is used by the MPU to select each of the memory locations within the Micromodule system. As previously stated, Monoboard Microcomputer 1 contains various memory devices (EROM/ROM, RAM, and PIA) with the capability of more memory devices being located externally to this module. Therefore, the various memory locations addressed by the MPU may be located either on or off the Monoboard Microcomputer 1, depending upon the application. The address decoder uses a non-fully decoded address decoding scheme to uniquely address each EROM/ROM, RAM, or PIA located on Monoboard Microcomputer 1. The address map shown in Figure 1-2 is a result of this decoding scheme. If the MPU generates an address for a memory location other than the locations shown in the address map, the address decoder will generate a high level MEM-NOT-SELD signal. This signal will then enable data from an external memory location to be read into the MPU via the data bus. The Micromodule address bus is enabled to output the MPU address bits to an external location whenever the MPU's BA signal output is low or the Micromodule control bus GO/HALT input is high. Otherwise, the address bus is in the high impedance (off) state.

Associated with the external address bits are the VMA and VUA signals. These two signals are jumper-selectable by means of wire-wrap connector K1. When Monoboard Microcomputer 1 is not being used in an EXORciser having a Debug Module installed, the VMA and VUA signals must be identical. However, during Micromodule debugging, the VUA signal must be provided by the Debug Module independent of the VMA signal. Paragraph 2.5.2.1 describes the connections that must be made to wire-wrap connector K1 when Monoboard Microcomputer 1 is being used with or without a Debug Module.

For special micromodules (M68MM01-1 and M68MM01-2), mating connectors are provided for P1, 2, 3, and 4, and resistor networks for PIA B-port lines. For the M68MM01-1, resistor networks U26, U29, and U32 provide 4.7 kΩ pullup terminations to +5V for the output of the open-collector drivers in U25, U27, U28, U30, U31, and U33. For the M68MM01-2, U26, U29, and U32 provide 200-ohm, 330-ohm divider terminations.


P1
ADDRESS BUS INTERFACE
A0-A15
A0-A15
D0-D7
BA
GO/HALT
BA
R/W
DBE
φ2 TTL
MEM-NOT-SELD
BA
R/W
GO/HALT
NMI
IRQ
RESET
VMA
CONTROL BUS INTERFACE
BA
R/W
GO/HALT
NMI
IRQ
RESET
VMA
MPU
K1
VMA
VUA
VMA
φ2 MOS
φ1 MOS
DBE
DBE
MEM-NOT-SELD
φ2 TTL
MEM CLK
RR
φ2 TTL
MEM CLK
HOLD 1
CLOCK
RR
MEM CLK
REFRESH CONTROL FLIP-FLOP
RG
RG
RESTART CIRCUIT
RESET
RESET



TYPICAL JUMPER CONFIGURATION:

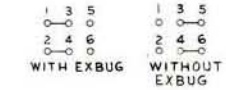
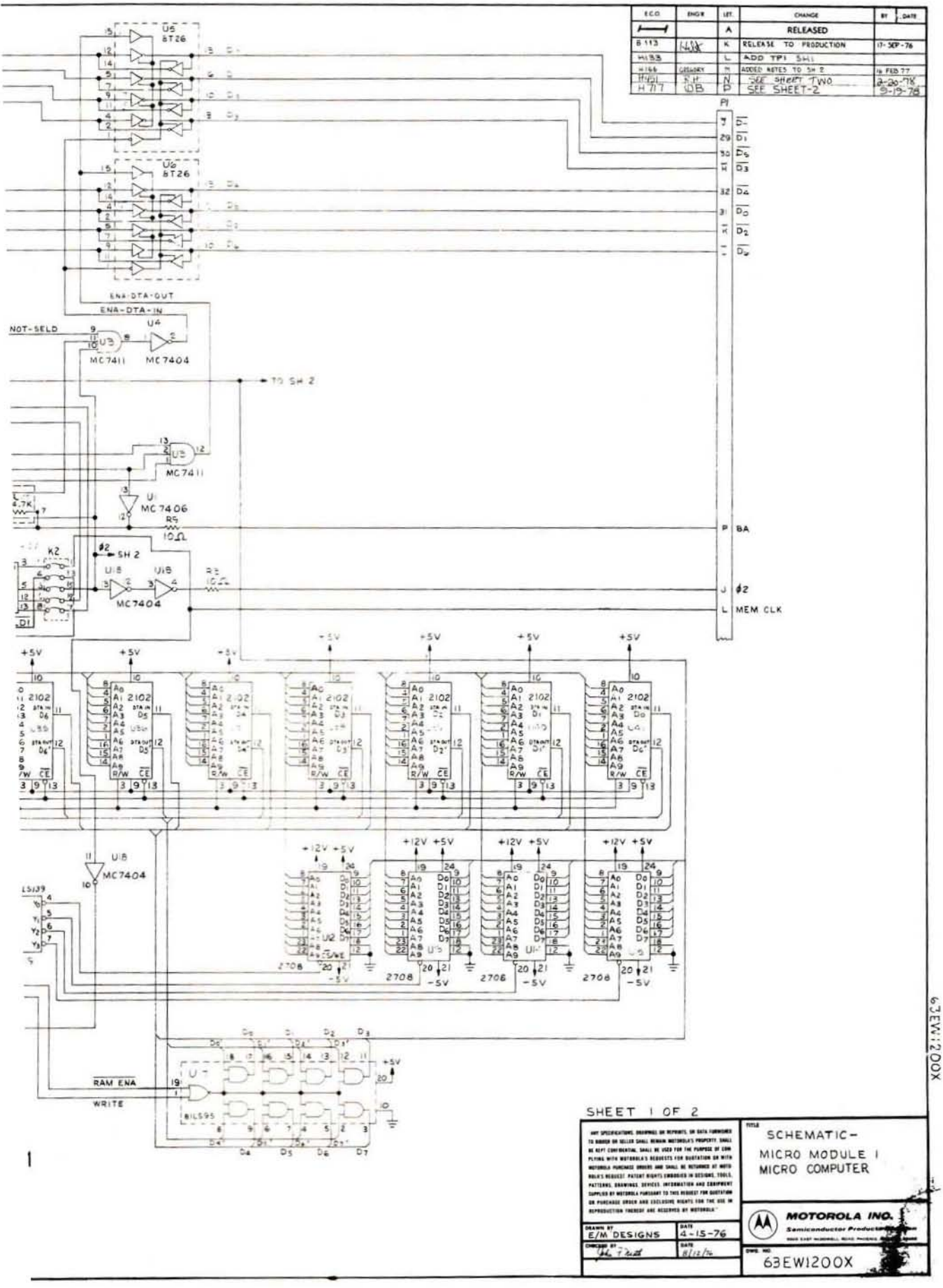


Figure 3-2. Monoboard Microcomputer 1 Schematic Diagram

NOTES:


ECO
ENGR
LET.
CHANGE
BY
DATE
A
RELEASED
B 113
K
RELEASE TO PRODUCTION
17-SEP-76
H133
L
ADD TP1 SH1
H166
GREGORY
N
ADDED NOTES TO SH 2
16 FEB 77
H191
K H
N
SEE SHEET TWO
2-20-78
H 717
DB
P
SEE SHEET-2
5-19-78
U5 8T26
U6 8T26
ENA-DTA-OUT
ENA-DTA-IN
NOT-SELD
MC7411
MC7404
TO SH 2
MC7406
10Ω
K2
SH 2
MC7404
+5V
-5V
+12V
2102
2708
LS139
RAM ENA
WRITE
8ILS95
P1
BA
MEM CLK
SHEET 1 OF 2
SCHEMATIC-
MICRO MODULE 1
MICRO COMPUTER
MOTOROLA INC.
Semiconductor Products
E/M DESIGNS
4-15-76
8/12/76
63EW1200X

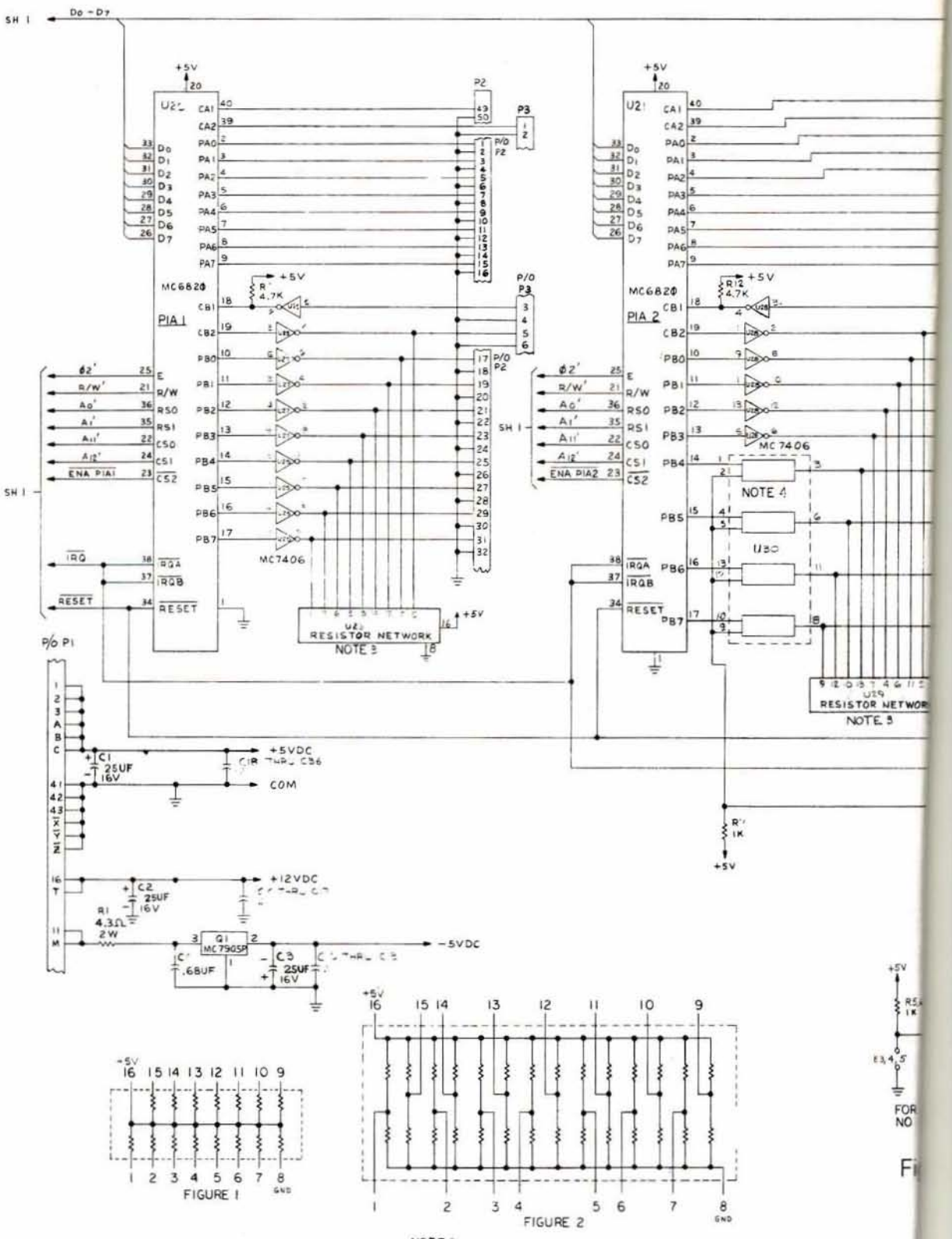


FIGURE 1

FIGURE 2

NOTE 3:
RESISTOR NETWORKS ARE CUSTOMER OPTIONS- RESISTOR PACK CONFIGURATIONS MAY BE AS IN EITHER FIGURE 1 OR 2.

NOTES CONTINUED:

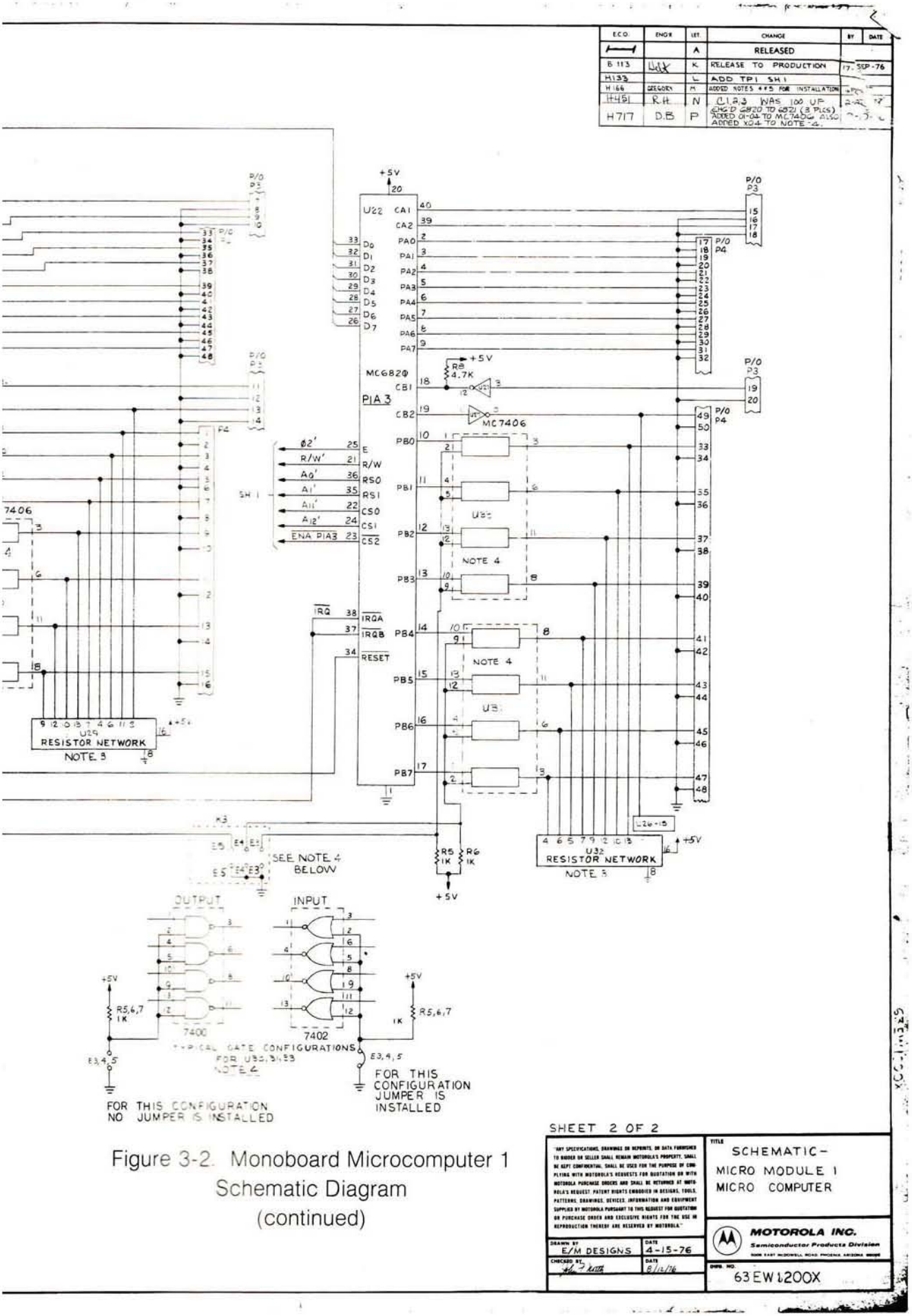


Figure 3-2. Monoboard Microcomputer 1 Schematic Diagram (continued)

CHAPTER 4
MAINTENANCE INFORMATION

4.1 INTRODUCTION

This chapter provides the parts list for Micromodule 1. The list reflects the latest issue of hardware at the time of printing. Parts locations are shown in Figure 4-1.

TABLE 4-1. Monoboard Microcomputer 1 (M68MM01) Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
—	84DW6200X01	Printed Wiring Board, Micromodule 1	AD
—	55NW9403A05	Ejector, Card, .062 thick, .250 wide (2 required)	AD
C1–C3	23NW9618A33	Capacitor, Electrolytic, 25μF @ 16Vdc	AD
C4*	21NW9604A18	Capacitor, Fixed Ceramic, .68μF @ 50Vdc	AD
	21NW9604A38	*Alternate: Capacitor, Fixed, Ceramic 1.0μF @ 25Vdc	AD
	21NW9604A08	*Alternate: Capacitor, Ceramic, 1μF @ 50 Vdc, 20%	AD
C5–C36	21NW9702A09	Capacitor, Ceramic, 0.1μF @ 50Vdc	AD
K1,K3	28NW9802B88	Header, Post, Double Row, 6-pin	AD
K2	28NW9802B22	Header, Post, Double Row, 10-pin	AD
R1	17NW9625A06	Resistor, Fixed, Wirewound, 4.3 ohms, 10%	AD
R2,R11	06SW-124B22	Resistor, Fixed Carbon, 1.0 Megohm, 5%, 1/4W	AD
R3,R9	06SW-124A01	Resistor, Fixed Carbon, 10 ohms, 5%, 1/4W	AD
R4,R8,R12	06SW-124A65	Resistor, Fixed Carbon, 4.7 kΩ, 5%, 1/4W	AD
R5,R6,R7,R10	06SW-124A49	Resistor, Fixed Carbon, 1 kΩ, 5%, 1/4W	AD
U1,U25,U27, U28	51NW9615A36	I.C. MC7406P	AD
U2	51NW9615A47	I.C. SN7474N (MC5479L)	AD
U3	51NW9615A68	I.C. MC3006P	AD
U4,U18	51NW9615A35	I.C. MC7404P	AD
U5,U6**	51NW9615B35	I.C. 8T26	AD
	51NW9615F96	**Alternate: I.C. SN75136N	AD
U7,U8,U9***	51NW9615B71	I.C. 8T97	AD
	51NW9615D23	***Alternate: I.C. 8T95	AD
U10	48NW9606A14	1.000 MHz Crystal Oscillator	AD

TABLE 4-1. Monoboard Microcomputer 1 (M68MM01) Parts List (Continued)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFECTIVITY
U11	51NW9615B65	I.C. MC1455P1	AD
U12,U13,U14, U15	—	ROM/EROM, 1K x 8 (customer supplied)	—
—	09NW9811A15	Socket, IC, Dual Inline, Low Profile, 24-pin, (used with U12,U13,U14,U15) (4 required)	AD
U16	51NW9615B69	I.C. MC6800P/L MPU	AD
—	09NW9811A22	Socket, IC, Dual Inline, Low Profile, 40-pin (used with U16,U20,U21,U22) (4 required)	AD
U17	51NW9615C68	I.C. DM81LS95N	AD
U19	51NW9615C70	I.C. SN74LS139N	AD
U20,U21,U22	51NW9615B27	I.C. MC6821P PIA	AD
U23,U30,U31, U33	51NW9615A32	I.C. MC7400P	AD
—	09NW9811A02	Socket, IC, Dual Inline, Low Profile, 14-pin (used with U23,U30,U31,U33) (4 required)	AD
U24	51NW9615C69	I.C. SN74LS138N	AD
U26,U29,U32	51NW9626A13	Resistor Network,4.7 kΩ, 15 per package (for M68MM01-1 only)	AD
	51NW9626A20	Resistor Network, 220-ohms/330-ohms, 14 per package (for M68MM01-2 only)	AD
—	09NW9811A04	Socket, IC, Dual Inline, Low Profile, 16-pin, (used with U26,U29,U32) (3 required)	AD
U34–U41	51NW9615D35	I.C. 2102AN RAM	AD
U42	51NW9626A05	Resistor Network, 4.7 kΩ per section	AD
VR1	51NW9615C39	I.C. MC7905CP	AD
—	43NW9002A47	Bushing, Insulator, Nylon, Shoulder (used with VR1)	AD
—	28NW9802A65	Connector, 86-pin (SAC-43D/8-2) (for M68MM01-1 only)	AD
—	28NW9802A72	Connector, 86-pin (for M68MM01-2 only)	AD
—	28NW9802B23	Connector, DIP, with flat cable cover (for M68MM01-1 and M68MM01-2 only)	AD
—	28NW9802A56	Connector, Card Edge, 50-contact, without ear (2 required) (for M68MM01-1 and M68MM01-2 only)	AD

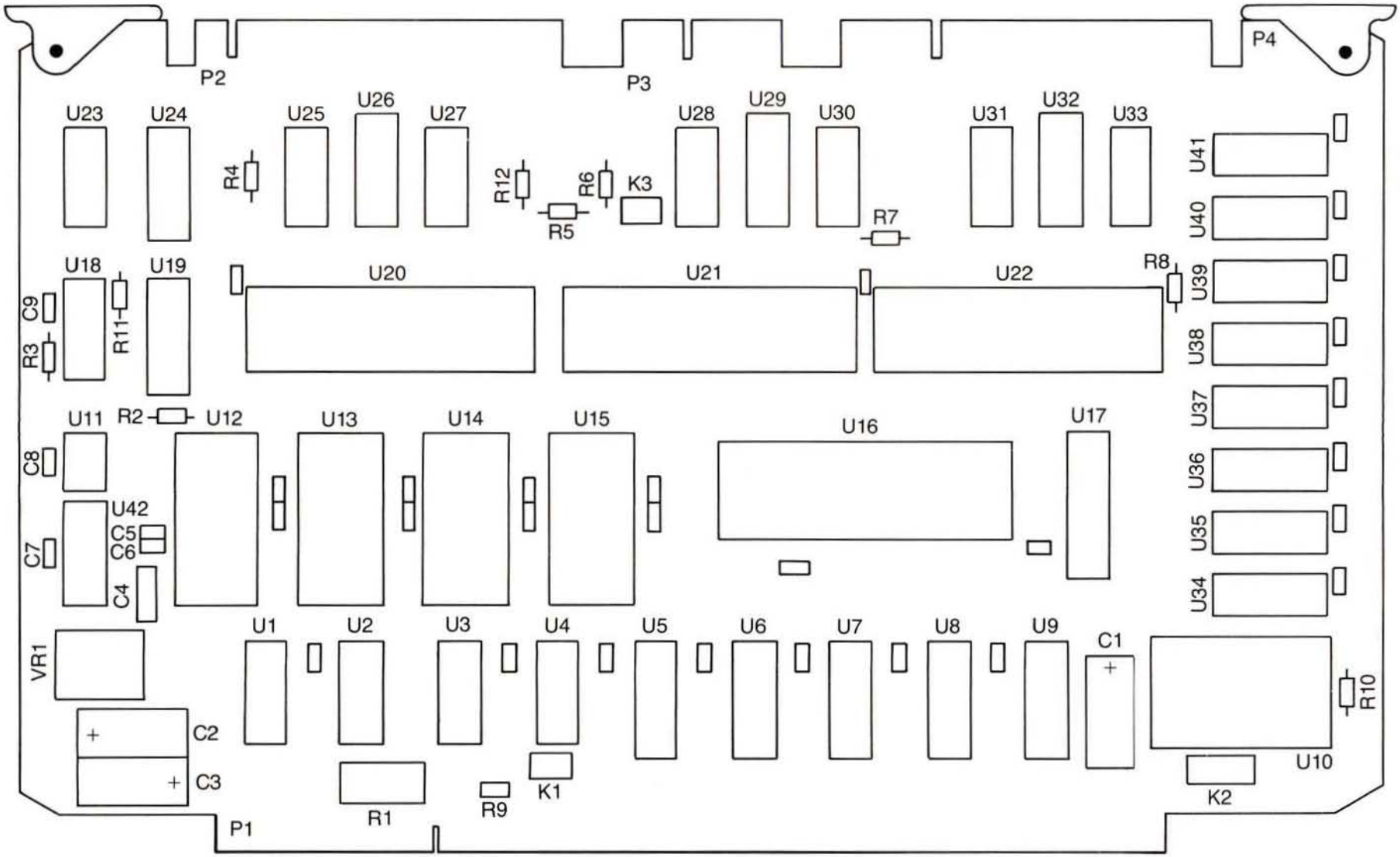


Figure 4-1. Monoboard Microcomputer 1 Parts Location

MOTOROLA

MICROSYSTEMS • 3102 North 56th Street • Phoenix, Arizona 85018