USERS MANUAL

FOR

MSC 3303

2-26-81

MONOSTORE VII/PLANAR
PDP-11 Add-In

SEMICONDUCTOR MEMORY SYSTEM

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SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides information for installing, operating, and maintaining the Monostore VII/Planar PDP-11 add-in memory systems. The material is arranged in five sections as follows:

Section I General Description

This section provides the scope, contents, and arrangement of the manual. A general description and a list of system specifications are also given.

Section II Installation and Operation

Instructions are provided for unpacking, inspecting and installing the memory system.

Section III Theory of Operation

An overall description of the memory system is provided along with a timing diagram to aid in understanding the system and to support troubleshooting.

Section IV Maintenance and Troubleshooting

This section gives recommended general maintenance procedures and troubleshooting information for diagnosing and locating a malfunction.

Section V Drawings

This section contains schematics, assembly, and parts list for the memory system.

1.2 General Description

The Monostore VII/Planar PDP-11 Add-In Memory System, P/N 303-0097-xxx, consists of a single planar 12Kx16 memory assembly. All electronics, DC conversion, and semiconductor dynamic N channel memory storage elements are contained on a single printed circuit board. The memory elements are mounted in IC sockets providing for ease of replacement.

All signal interface is made through the DEC™ DD-11A System Unit, sections CDEF. Data interfacing is provided by 16 bidirectional data bits. Addressing any one of the 12,288 words is provided by 14 binary address bits, together with command and control information to define the memory mode required.

The memory system uses the +5 V and -15 V power available on the DD-11A unit and generates additional voltages on the board.

The maximum capacity of the board is 12,288 words by 16 bits. The system can also be configured in 4,096 words by 16 bits or 8,192 words by 16 bits.

1.3 Modes of Operation (slave = memory system)

Name	Mnemonic	C Lines		Function	Octal Code
		C1	C0		
Data in	DATI	0	0	Data from slave to master	0
Data in, pause	DATIP	0	1	Data from slave to master	1
Data out	DATO	1	0	Data from master to slave	2
Data out Byte	DATOB	1	1	Transfers data from master to a single byte in slave. Data transmitted on D <15:08> for A00=1 D <07:00> for A00=0	3

NOTE: DEC IS A TRADEMARK OF DIGITAL EQUIPMENT CORPORATION.

1.4 System Specifications

Characteristics	Specification
Storage Capacity	4096 words x 16 bits 8192 words x 16 bits 12288 words x 16 bits
Cycle Time	1000 nsec SLOW SPEED 700 nsec STANDARD SPEED 580 nsec HIGH SPEED
Read Access Time	750 nsec SLOW SPEED 500 nsec STANDARD SPEED 400 nsec HIGH SPEED
Input Power	+5V, 2.7A -15V, 0.4A
Operating Environment	
Temperature	0^{o}C to +50^{o}C
Relative Humidity	90% maximum without condensation
Physical Dimensions	
Height	8.5 inches
Depth	0.5 inch*
Width	14.7 inches

* 1.0 inch for "non-switch" version.

SECTION II

INSTALLATION & OPERATION

2.1 INTRODUCTION

This section contains information for installation and operation of the memory system.

2.2 UNPACKING AND INSPECTION

Carefully remove the memory system from the shipping container. Remove any packing material from the assembly. Inspect the system for any damage or loose connections.

2.3 INSTALLING MEMORY SYSTEM

Remove the external bottom cover from the PDP-11 computer. Insert the memory system into the DD-11A System Unit, designated for small peripherals, in the CDEF sections. The cutaway portion of the board will align itself over the UNIBUS cable connector Sections A & B. Reassembly the bottom cover. The memory system is now ready for use.

NOTE: UNIBUS IS A TRADEMARK OF DIGITAL EQUIPMENT CORPORATION.

2.4 I/O SIGNALS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
CA1		CA2	+5V	DA1		DA2	+5V
CB1		CB2	-15V	DB1		DB2	-15V
CC1		CC2	GND	DC1	SEL6H	DC2	GND
CD1		CD2	D15L	DD1	OUT LOW H	DD2 DB2	BR7 BR7
CE1		CE2	DI4L	DE1	SEL4H	DE2	BR6
CF1		CF2	D13L	DF1	SEL OH	DF2	BR5
CH1	D11L	CH2	D12L	DH1	IN H	DH2	BR4
CJ1	INT B H	CJ2	D10L	DJ1	SEL 2H	DJ2	B REQUEST
CK1		CK2	D09L	DK1	OUT HIGH H	DK2	BG 7 IN H
CL1	INTR ENB BH	CL2	D08L	DL1	INIT L	DL2	BG 7 OUT H
CM1		CM2	D07L	DM1	INT ENB AH	DM2	BG 6 IN H
CN1		CN2	D04L	DN1	INT AH	DN2	BG 6 OUT H
CP1		CP2	D05L	DP1		DP2	BG 5 IN H
CR1		CR2	D01L	DR1		DR2	BG 5 OUT H
CS1		CS2	D00L	DS1		DS2	BG 4 IN H
CT1	GND	CT2	D03L	DT1	GND	DT2	BG 4 OUT H
CU1		CU2	D02L	DU1		DU2	BG IN AH
CV1		CV2	D06L	DV1	EXT CAP.	DV2	BG OUT BH

2.4 I/O SIGNALS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
CA1		CA2	+5V	DA1		DA2	+5V
CB1		CB2	-15V	DB1		DB2	-15V
CC1		CC2	GND	DC1	SEL6H	DC2	GND
CD1		CD2	D15L	DD1	OUT LOW H	DD2 DD2	BR7 BR7
CE1		CE2	D14L	DE1	SEL4H	DE2	BR6
CF1		CF2	D13L	DF1	SEL OH	DF2	BR5
CH1	D11L	CH2	D12L	DH1	IN H	DH2	BR4
CJ1	INT B H	CJ2	D10L	DJ1	SEL 2H	DJ2	B REQUEST
CK1		CK2	D09L	DK1	OUT HIGH H	DK2	BG 7 IN H
CL1	INTR ENB BH	CL2	D08L	DL1	INIT L	DL2	BG 7 OUT H
CM1		CM2	D07L	DM1	INT ENB AH	DM2	BG 6 IN H
CN1		CN2	D04L	DN1	INT AH	DN2	BG 6 OUT H
CP1		CP2	D05L	DP1		DP2	BG 5 IN H
CR1		CR2	D01L	DR1		DR2	BG 5 OUT H
CS1		CS2	D00L	DS1		DS2	BG 4 IN H
CT1	GND	CT2	D03L	DT1	GND	DT2	BG 4 OUT H
CU1		CU2	D02L	DU1		DU2	BG IN AH
CV1		CV2	D06L	DV1	EXT CAP.	DV2	BG OUT BH

2.4 I/O SIGNALS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
EA1	EXT GND	EA2	+5V	FA1	BG OUT BH	FA2	+5V
EB1	EXT CAP	EB2	-15V	FB1	BG IN AH	FB2	-15V
EC1	A12L	EC2	GND	FC1	SSYNL	FC2	GND
ED1	A17L	ED2	A15L	FD1	BBSYL	FD2	VECTOR BIT 2
EE1	MSYNL	EE2	A16L	FE1	BG IN BH	FE2	D02L
EF1	A02L	EF2	C1L	FF1	005L	FF2	DO6L
EH1	A01L	EH2	A00L	FH1	007L	FH2	INT ENB BH
EJ1	SSYNL	EJ2	COL	FJ1		FJ2	EXT GND
EK1	A14L	EK2	A13L	FK1	D08L	FK2	INT BH
EL1	A11L	EL2	TEST PT	FL1	D03L	FL2	INTR DONE AH
EM1	IN H	EM2	OUT HIGH H	FM1	INTRL	FM2	INTR DONE BH
EN 1	OUT LOW H	EN2	A08L	FN1	MSTR AL	FN2	D04L
EP1	A10L	EP2	A07L	FP1	BR BL	FP2	STRT INTR BL
ER1	A09L	ER2	SEL 4H	FR1	MSTR CLR AH	FR2	STRT INTR AL
ES1	SEL 6H	ES2	SEL 0H	FS1	MSTR CLR BH	FS2	MSTR BL
ET1	GND	ET2	SEL 2H	FT1	GND	FT2	SACK L
EU1	A06L	EU2	A04L	FU1	INTA H	FU2	BR AL
EV1	A05L	EV2	A03L	FV1	ENBA H	FV2	BG OUT AH

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

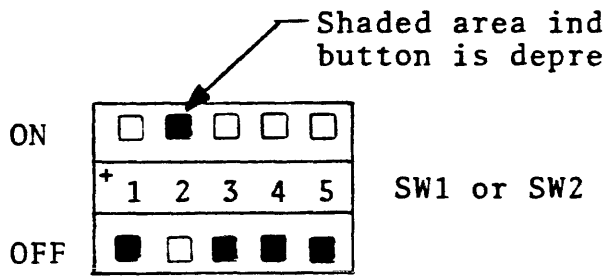
This section describes the overall organization and operation of this MO VII PL PDP-11 Add-in Semiconductor Memory System. The System has a maximum capacity of 12288 words of 16 bits.

This section is organized into the following major parts:

Description	Paragraph
Memory Location Programming	3.2
Address Channel	3.3
Data Channel	3.4
Timing Circuitry	3.5
DC Converter	3.6

3.2 MEMORY LOCATION PROGRAMMING

The memory location is programmed via wire jumpers or switches on the board. The user can program the memory to any location according to the following table:



.Example shown is for address 56xxxx.

MSF-1005 REV A

3.2 Memory Location Programming

MONOSTORE VII/PLANAR PDP-11 ADD-IN PROGRAMMING

Starting Address	L SW1 B Section- 1 2 3 4 5	H SW2 A Section 1 2 3 4 5	NOT PROGRAMMED K PROGRAM JUMPERS U V W X Y Z	MEMORY CAPACITY
0 0 0 0 0 0 OK	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 0 1 1 1 0 1	C E D B F C	4K 8K 12K
0 2 0 0 0 0 4K	1 1 1 1 0 1 1 1 1 0 1 1 1 1 0	1 1 1 1 0 1 1 1 0 1 1 1 1 0 0	D E C F F D	4K 8K 12K
0 4 0 0 0 0 8K	1 1 1 0 1 1 1 1 0 1 1 1 1 0 1	1 1 1 0 1 1 1 1 0 0 1 1 0 1 1	C F D F E C	4K 8K 12K
0 6 0 0 0 0 12K	1 1 1 0 0 1 1 1 0 0 1 1 1 0 0	1 1 1 0 0 1 1 0 1 1 1 1 0 1 0	D F C E E D	4K 8K 12K
1 0 0 0 0 0 16K	1 1 0 1 1 1 1 0 1 1 1 1 0 1 1	1 1 0 1 1 1 1 0 1 0 1 1 0 0 1	C E D B F C	4K 8K 12K
1 2 0 0 0 0 20K	1 1 0 1 0 1 1 0 1 0 1 1 0 1 0	1 1 0 1 0 1 1 0 0 1 1 1 0 0 0	D E C F F D	4K 8K 12K
1 4 0 0 0 0 24K	1 1 0 0 1 1 1 0 0 1 1 1 0 0 1	1 1 0 0 1 1 1 0 0 0 1 0 1 1 1	C F D F E C	4K 8K 12K
1 6 0 0 0 0 28K	1 1 0 0 0 1 1 0 0 0 1 1 0 0 0	1 1 0 0 0 1 0 1 1 1 1 0 1 1 0	D F C E E D	4K 8K 12K
	1 = Add Jumper or ON 0 = No Jumper or OFF			

SIZE A | CODE IDENT NO. 51513 | DWG NO. 100-0018-000 | REV D | SCALE | SHEET 10

MONOSTORE VII/PLANAR PDP-11 ADD-IN PROGRAMMING

Starting Address	L SW1 B Section- 1 2 3 4 5	H SW2 A Section 1 2 3 4 5	NOT PROGRAMMED K PROGRAM JUMPERS U V W X Y Z	MEMORY CAPACITY
2 0 0 0 0 0 32K	1 0 1 1 1 1 0 1 1 1 1 0 1 1 1	1 0 1 1 1 1 0 1 1 0 1 0 1 0 1	C B D B F C	4K 8K 12K
2 2 0 0 0 0 36K	1 0 1 1 0 1 0 1 1 0 1 0 1 1 0	1 0 1 1 0 1 0 1 0 1 1 0 1 0 0	D E C F F D	4K 8K 12K
2 4 0 0 0 0 40K	1 0 1 0 1 1 0 1 0 1 1 0 1 0 1	1 0 1 0 1 1 0 1 0 0 1 0 0 1 1	C F D F E C	4K 8K 12K
2 6 0 0 0 0 44K	1 0 1 0 0 1 0 1 0 0 1 0 1 0 0	1 0 1 0 0 1 0 0 1 1 1 0 0 1 0	D F C E E D	4K 8K 12K
3 0 0 0 0 0 48K	1 0 0 1 1 1 0 0 1 1 1 0 0 1 1	1 0 0 1 1 1 0 0 1 0 1 0 0 0 1	C E D E F C	4K 8K 12K
3 2 0 0 0 0 52K	1 0 0 1 0 1 0 0 1 0 1 0 0 1 0	1 0 0 1 0 1 0 0 0 1 1 0 0 0 0	D E C F F D	4K 8K 12K
3 4 0 0 0 0 56K	1 0 0 0 1 1 0 0 0 1 1 0 0 0 1	1 0 0 0 1 1 0 0 0 0 0 1 1 1 1	C F D F E C	4K 8K 12K
3 6 0 0 0 0 60K	1 0 0 0 0 1 0 0 0 0 1 0 0 0 0	1 0 0 0 0 0 1 1 1 1 0 1 1 1 0	D F C E E D	4K 8K 12K
	1 = Add Jumper or ON 0 = No Jumper or OFF			

SIZE A | CODE IDENT NO. 51513 | DWG NO. 100-0018-000 | REV D | SHEET 11 | SCALE

MSF-1005 REV A

MSF-1005 REV A

3.2 Memory Location Programming

MONOSTORE VII/PLANAR PDP-11 ADD-IN PROGRAMMING

Starting Address	L SW1 B Section- 1 2 3 4 5	H SW2 A Section 1 2 3 4 5	NOT PROGRAMMED K PROGRAM JUMPERS U V W X Y Z	MEMORY CAPACITY
4 0 0 0 0 0 64K	o 1 1 1 1 o 1 1 1 1 o 1 1 1 1	o 1 1 1 1 o 1 1 1 0 o 1 1 0 1	C B D E F C	4K 8K 12K
4 2 0 0 0 0 68K	o 1 1 1 0 o 1 1 1 0 o 1 1 1 0	o 1 1 1 0 o 1 1 0 1 o 1 1 0 0	D E C F F D	4K 8K 12K
4 4 0 0 0 0 72K	o 1 1 0 1 o 1 1 0 1 o 1 1 0 1	o 1 1 0 1 o 1 1 0 0 o 1 0 1 1	C F D F E C	4K 8K 12K
4 6 0 0 0 0 76K	o 1 1 0 0 o 1 1 0 0 o 1 1 0 0	o 1 1 0 0 o 1 0 1 1 o 1 0 1 0	D F C E E D	4K 8K 12K
5 0 0 0 0 0 80K	o 1 0 1 1 o 1 0 1 1 o 1 0 1 1	o 1 0 1 1 o 1 0 1 0 o 1 0 0 1	C E D E F C	4K 8K 12K
5 2 0 0 0 0 84K	o 1 0 1 0 o 1 0 1 0 o 1 0 1 0	o 1 0 1 0 o 1 0 0 1 o 1 0 0 0	D E C F F D	4K 8K 12K
5 4 0 0 0 0 88K	o 1 0 0 1 o 1 0 0 1 o 1 0 0 1	o 1 0 0 1 o 1 0 0 0 o 0 1 1 1	C F D F E C	4K 8K 12K
5 6 0 0 0 0 92K	o 1 0 0 0 o 1 0 0 0 o 1 0 0 0	o 1 0 0 0 o 0 1 1 1 o 0 1 1 0	D F C E E D	4K 8K 12K
	1 = Add Jumper or ON 0 = No Jumper or OFF			

SIZE A | CODE IDENT NO. 51513 | DWG NO. 100-0018-000 | REV D | SCALE | SHEET 12

3.2 Memory Location Programming

MONOSTORE VII/PLANAR PDP-11 ADD-IN PROGRAMMING

Starting Address	L SW1 B Section- 1 2 3 4 5	H SW2 A Section 1 2 3 4 5	NOT PROGRAMMED K PROGRAM JUMPERS U V W X Y Z	MEMORY CAPACITY
6 0 0 0 0 0 96K	o o 1 1 1 o o 1 1 1 o o 1 1 1	o o 1 1 1 o o 1 1 0 o o 1 0 1	C B D B F C	4K 8K 12K
6 2 0 0 0 0 100K	o o 1 1 0 o o 1 1 0 o o 1 1 0	o o 1 1 0 o o 1 0 1 o o 1 0 0	D B C F F D	4K 8K 12K
6 4 0 0 0 0 104K	o o 1 0 1 o o 1 0 1 o o 1 0 1	o o 1 0 1 o o 1 0 0 o o 0 1 1	C F D F E C	4K 8K 12K
6 6 0 0 0 0 108K	o o 1 0 0 o o 1 0 0 o o 1 0 0	o o 1 0 0 o o 0 1 1 o o 0 1 0	D F C E E D	4K 8K 12K
7 0 0 0 0 0 112K	o o 0 1 1 o o 0 1 1 o o 0 1 1	o o 0 1 1 o o 0 1 0 o o 0 0 1	C B D B F C	4K 8K 12K
7 2 0 0 0 0 116K	o o 0 1 0 o o 0 1 0 o o 0 1 0	o o 0 1 0 o o 0 0 1 o o 0 0 0	D B C F F D	4K 8K 12K
7 4 0 0 0 0 120K	o o 0 0 1 o o 0 0 1	o o 0 0 1 o o 0 0 0	C F D F E C	4K 8K
7 6 0 0 0 0 124K	o o o 0 0	1 1 0 0 0	D F C E E D	4K
	1 = Add Jumper or ON 0 = No Jumper or OFF			

SIZE	CODE IDENT NO.	DWG NO.	REV	SHEET
A	51513	100-0018-000	D	13

SCALE

The computer generated addresses A17L → A13L are compared against the programmed jumpers A and B sections. If the generated addresses are within the programmed range a memory cycle will be initiated by MSYNL signal. This circuitry is shown on sheets 2, 3, and 6 of the schematic in Section V.

3.3 ADDRESS CHANNEL

When a memory cycle is initiated the information on the address lines A00L → A13L is latched into an address register.

A01L → A06L - These address bits are multiplexed with another set of bits used for refreshing. They are then buffered in order to drive the complete memory array.

A07L → A12L - These address bits are buffered in order to drive the complete memory array.

A13L, A14L - These address bits are decoded to generate the 4K, 8K or 12K cenable pulse required by the memory elements. The cenable pulse then enables only one row of memory elements at any one time thereby preventing interraction of data bits.

The address channel and cenable circuits are shown on sheets 2 and 6 of the schematic in Section V.

3.4 DATA CHANNEL

When a memory cycle, DATO, is initiated the information contained on the D00L → D15L lines is latched into a write data register. The outputs of the register are then buffered in order to drive the data input lines of the memory storage elements. A write cycle is then performed and this data is stored in the memory elements at the address location specified on the AxxL lines.

When a memory cycle, DATI, is initiated the information previously stored in the memory elements is accessed and transmitted onto the D00L → D15L lines for use by the computer.

A DATOB is similar to a DATO cycle except on an 8 bit basis.
A DATIP is the same as a DATI cycle.
The data channel circuits are shown on sheets 4 and 5 of the schematic in Section V.

3.5 TIMING CIRCUITRY

The memory system contains delay line timing circuits which generate, directly or indirectly, all internal and I/O pulses or signals.

The MSYNL signal is received by the memory system and generates a read or write cycle depending upon whether C1L is a "0" or a "1" respectively. If it is a write cycle then SSYNL is sent back to the master unit signifying receipt of data and address info. If it is a read cycle SSYNL is delayed until data is on the DxxL lines and SSYNL is then generated telling the master that the data is available.

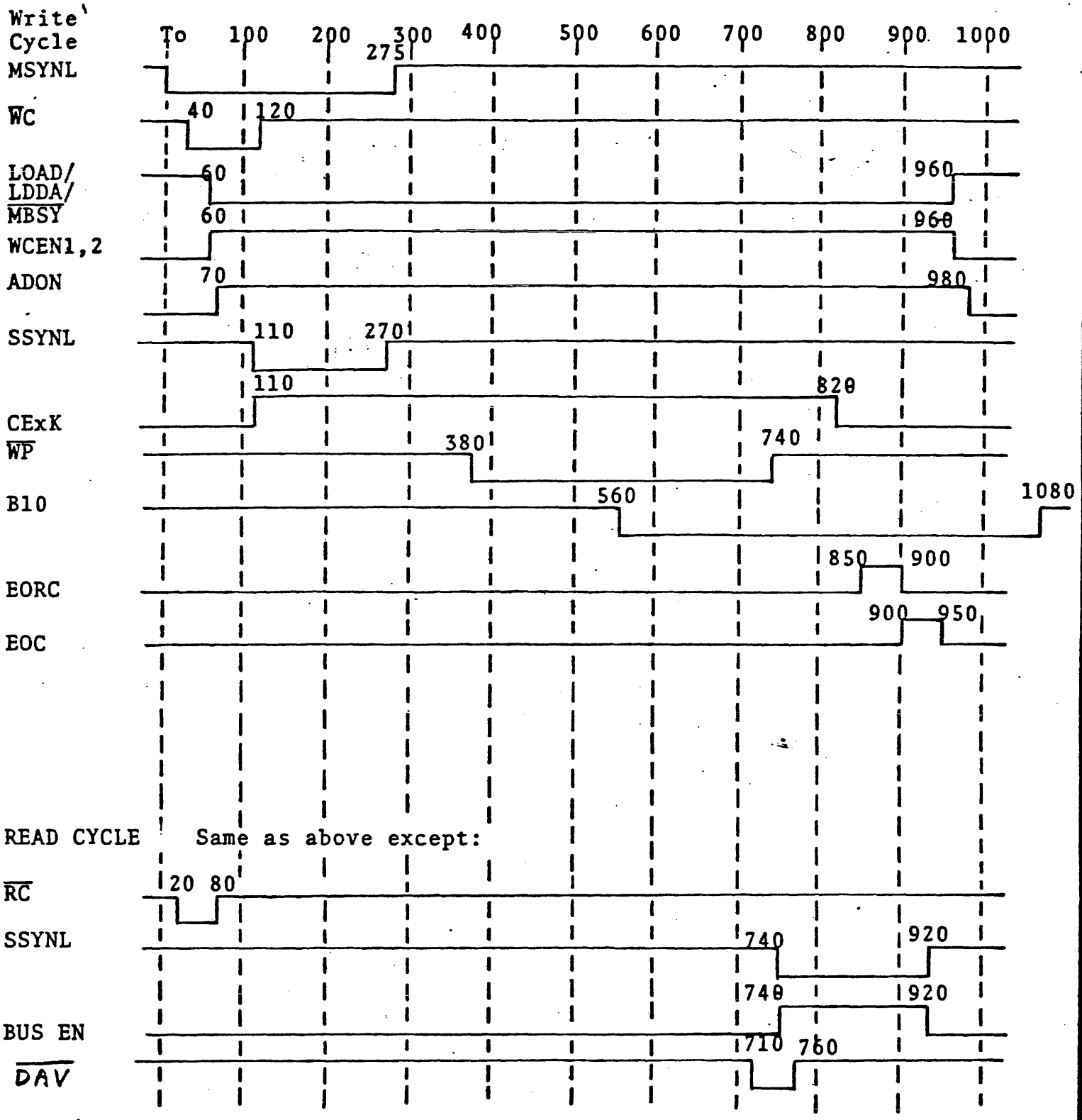
The timing circuitry generates pulses according to the following timing diagram:

MONOSTORE VII/PL PDP-11

TIMING DIAGRAM

SLOW SPEED (SEE SHT. 5)
ADD-IN MEMORY SYSTEM

750/1000

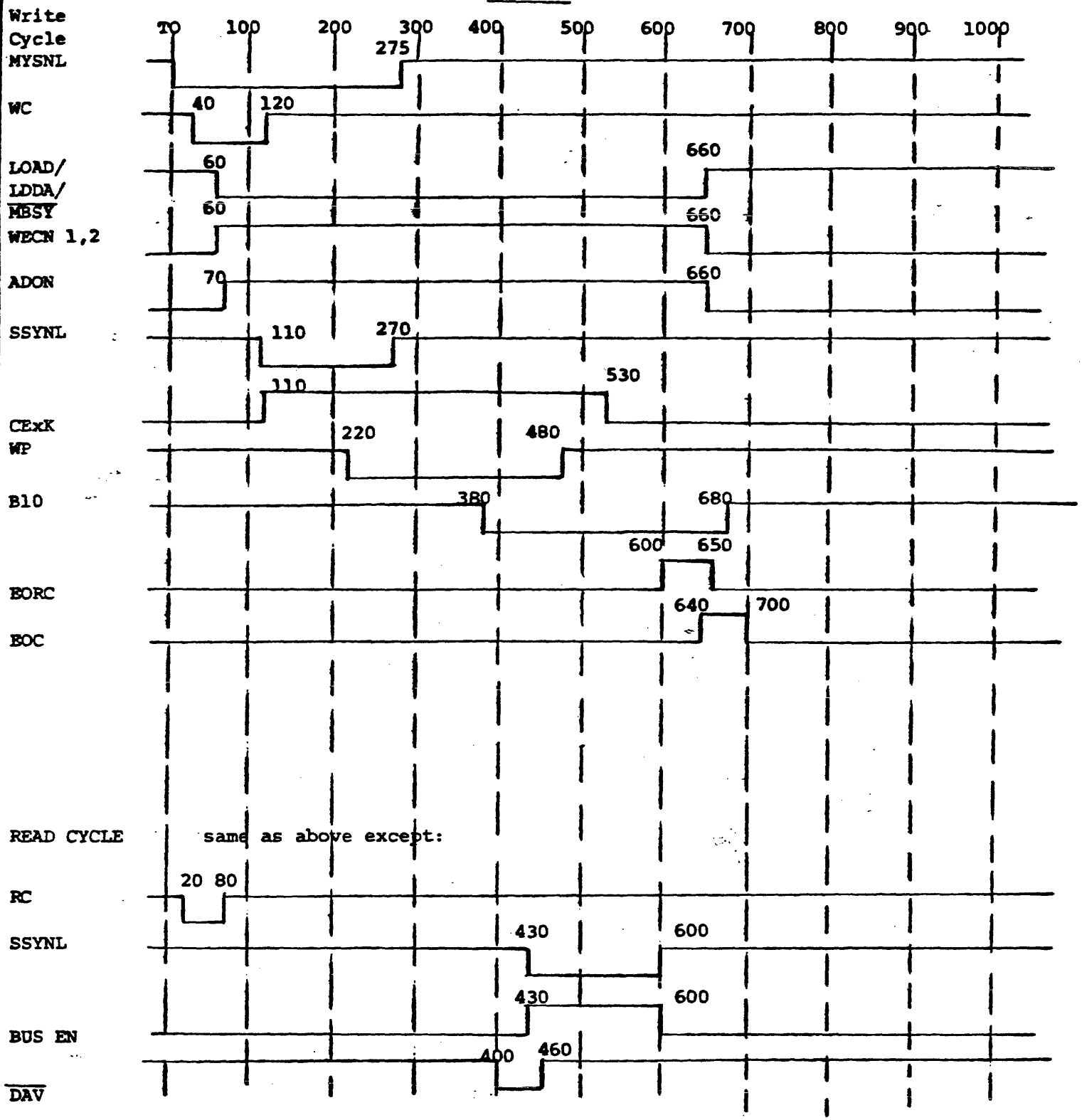


	SIZE	CODE IDENT NO.	DWG NO.
	A	51513	100-0018-000
	SCALE	REV F	SHEET 16

TIMING DIAGRAM STANDARD SPEED (SEE PAGE 5)

MONOSTORE VII/PL PDP-11 ADD-IN MEMORY SYSTEM

500/700

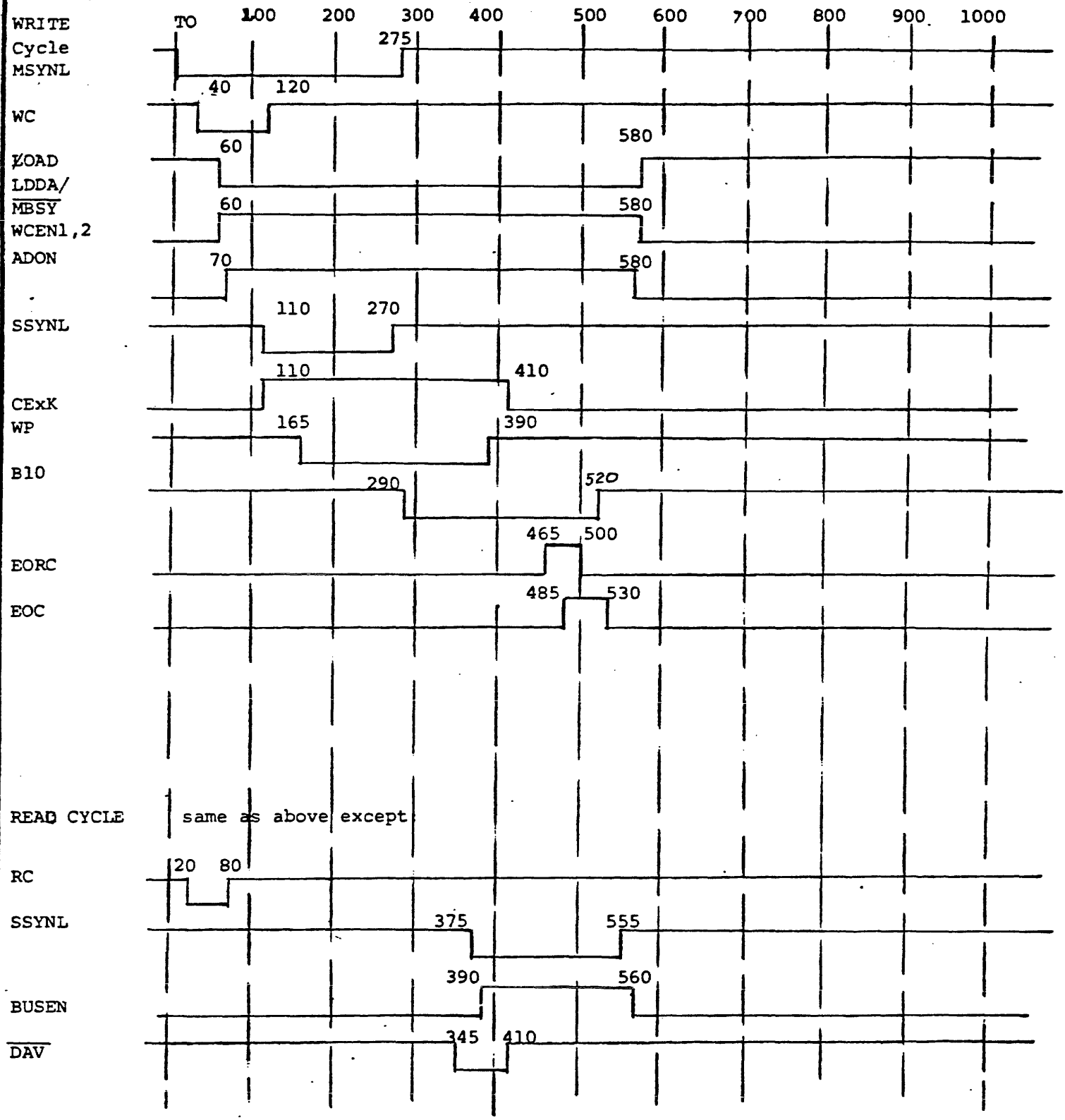


SIZE	CODE IDENT NO.	DWG NO.
A	51513	100-0018-000
SCALE	REV F	SHEET 17

TIMING DIAGRAM HIGH SPEED (SEE PAGE 5)

MONOSTORE VII/PL PDP-11 ADD-IN MEMORY SYSTEM

400/580



	SIZE	CODE IDENT NO.	DWG NO.
	A	51513	100-0018-000
	SCALE	REV F	SHEET 18

MSF—1005

There are 2 level transitions which travel down the two delay lines in series. The timing pulses are generated in such a way that the sequence of these transitions and the delay line taps used determine when a pulse will or will not be generated.

The memory elements are dynamic N-channel devices and require refreshing every 2 msec. The memory system uses "cycle steal" refreshing such that a normal cycle may be extended by 700 nsec approximately 2% of the time.

The timing circuitry is shown on sheet 6 of the schematic in Section V.

3.6 DC CONVERTER

The memory system contains a "DC to DC Converter" to convert -15V power to -5V and +12V power.

The -5v is series regulated down from the -15V level.

The +12V is generated by first converting the -15V to a nominal 20 Kilo-HZ signal, isolating it, and then rectifying and regulating it for +12V.

The DC converter circuit is shown on sheet 7 of the schematic in Section V.

SECTION IV

MAINTENANCE AND TROUBLESHOOTING

4.1 INTRODUCTION

This section presents troubleshooting instructions for ease of trouble location. Further localization of the trouble is to be found by means of the maintenance drawings in Section V. The theory of operation in Section III should be read and understood, along with a detailed review of the schematics in Section V in order to make effective use of this section.

4.2 PREVENTIVE MAINTENANCE

4.2.1 VISUAL INSPECTION

This inspection includes checking for loose programming wires, components, and discoloration of parts. The inspection should be performed with a minimum of prying or moving of parts.

4.2.2 CLEANING

Cleaning should be limited to removal of excess dust or particles. Never use any abrasive on any part of the gold fingers on the edge connectors. Low pressure compressed air can be used for removing dust or dirt and an aerosol cleaner can be used, with light brushing, to clean the gold contacts.

4.2.3 DC VOLTAGES

The DC voltages should be maintained as follows:

+5V ±5% +12V ±5%

-15V ±5% -5v ±5%

4.3 TROUBLESHOOTING

To facilitate troubleshooting the following information, cause and effect, can be used to isolate the problem to a particular area. From there on the schematics should be used to determine the exact component that is at fault.

Effect	Cause
Single bit failure all addresses.	Data receiver/driver/ write register/read register
Complete byte failure all addresses	WCEN pulse/strobe pulse/ COL circuitry.
Complete word failure, all addresses	DC voltages/refresh not working/ bus en pulse/ C1L circuitry/ WR pulse/strobe pulse.
Single bit failure, single address.	Memory element
Four bit failure, all addresses	Write register/read register
Complete word failure, a 4K section	CENABLE driver/ CEN programming jumpers/address register for A13L and A14L.
Complete byte failure, a 4K section.	CENABLE driver/ CEN programming jumpers/address register for A13L and A14L.

Effect	Cause
Complete or major part of word failure, 2 addresses	Address receiver/address register/ address buffer.
Timeout	A & B sets of jumpers/ SSYNL not generated/A13L → A17L comparison circuit.
Non-retention of data	Refresh circuit/DC voltages

SECTION V

DRAWINGS

ASSEMBLY	303-0097-000
SCHEMATIC	305-0097-000

REVISIONS

REV	ECO	DESCRIPTION	DATE	APP.
V	678	REVISED TO REDUCE NUMBER OF PAGES	6-14-77	[illegible]
W	0690	CORRECTED TYPING ERRORS	6-24-77	[illegible]
Y	1026	REVISED PER ECO DC 4/25/78	4-26-78	[illegible]
Z	1667	REVISED PER ECO DC 9/27/79	11-2-79	[illegible]
AA	2261	REVISED PER ECO ABSTRACT	5-16-80	[illegible]

NOTES: SEE SHEET 7.

REV STATUS OF SHEETS																												
	REV																											
	SHEET																											
	REV	AA	Z	AA	AA	AA	AA	AA																				
	SHEET	1	2	3	4	5	6	(7)																				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE:

SHEET 7 IS "D" SIZE

MATERIAL

		DATE
DRAWN	G.S.F.	6-9-77
CHECKED	[illegible]	6-14-77
APPROVED		
APPROVED		

MONOLITHIC SYSTEMS CORP.

P.C. BOARD ASSEMBLY
MSC-3303
MO VII PL/SPS

SIZE	CODE IDENT NO.	DWG NO.
A	51513	303-0097-000

SCALE NONE | REV AA | SHEET 1 of 7

DASH NO.	CONFIGURATION	MEM. ELEM. QTY/DASH NO. 313-0028-000	MEM. ELE. LOCATION	DELAY LINES (75) (U63, U73) 223-0001-001	223-0001-002	223-0001-003	P.C. BOARD 304-0097-001	304-0097-002
001	12Kx16	48	A	–	2	–	1	–
002	8Kx16	32	B	–	2	–	1	–
003	4Kx16	16	C	–	2	–	1	–
004	12Kx16	48	A	–	2	–	–	1
005	8Kx16	32	B	–	2	–	–	1
006	4Kx16	16	C	–	2	–	–	1
007	12Kx16	48	A	2	–	–	1	–
008	8Kx16	32	B	2	–	–	1	–
009	4Kx16	16	C	2	–	–	1	–
010	12Kx16	48	A	2	–	–	–	1
011	8Kx16	32	B	2	–	–	–	1
012	4Kx16	16	C	2	–	–	–	1
013	12Kx16	48	A	–	–	2	1	–
014	8Kx16	32	B	–	–	2	1	–
015	4Kx16	16	C	–	–	2	1	–
016	12Kx16	48	A	–	–	2	–	1
017	8Kx16	32	B	–	–	2	–	1
018	4Kx16	16	C	–	–	2	–	1

MEM. ELEM. LOCATION
A
U100-U147

B
U100-U131

C
U100-U115

SIZE	CODE IDENT NO.	DWG NO.
A	51513	303-0097-000

SCALE	REV	SHEET
NONE	Z	2

MSF-1015 REV A

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
			ALL	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
			4	210-0105-002	I.C. SN 74H10	U1,U3,U44,U64		1
			7	210-0200-002	I.C. SN 74H08	U2,U4,U31,U33,U34 U60,U65		2
			9	210-0605-001	I.C. SN 7475	U5,U8,U16,U18,U36 U38,U47,U51,U58		3
			11	210-0100-001	I.C. SN 7400	U6,U7,U9,U12,U15,U19 U22,U23,U26,U27,U42		4
			2	210-0716-001	I.C. SN 74193	U10,U13		5
			3	210-0806-002	I.C. SN 74H51	U11,U14,U17		6
			2	210-0307-001	I.C. SN 7437	U20,U54		7
			4	210-0718-005	I.C. SN 74LS197	U21,U24,U25,U28		8
			2	210-0107-002	I.C. SN 74H20	U29,U30		9
			5	210-0103-002	I.C. SN 74H04	U32,U40,U74,U75,U83		10
			6	210-0100-002	I.C. SN 74H00	U35,U39,U41,U43,U45 U55		11
			5	210-0308-001	I.C. SN 7438	U37,U56,U62,U66,U76		12
			10	210-1104-002	I.C. DS 8640	U46,U48,U57,U61, U67-72		13
			2	210-0906-001	I.C. SN 7485	U49,U59		14
			1	210-0816-001	I.C. SN 7486	U50		15
			1	210-0604-001	I.C. SN 7474	U52		16
			1	210-0504-001	I.C. SN 74123	U53		17
			3	210-1108-001	I.C. MH0026CH	U77-U79		18
			1	210-1107-001	I.C. 7808C	U80		19
			1	210-1102-001	I.C. LM304	U81		20
			1	210-0905-009	I.C. SN 7483AN	U82		21

SIZE A | CODE IDENT NO 51513 | DWG NO. 303-0097-000 | REV AA | SHEET 3

MSF-1015 REV A

SIZE	CODE IDENT NO	DWG NO.	REV	SHEET
A	51513	303-0097-000	AA	4

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
			ALL	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
								22
			6	201-0006-027	CAP 47 pf, 100V	C1-C6		23
			7	201-0018-004	CAP 6.8µf, 25V.	C7-C13		24
			1	201-0002-070	CAP .01µf, 50V.	C14		25
			2	201-0012-006	CAP 5µf, 150V.	C15, C16		26
			2	201-0015-031	CAP .05µf, 20V.	C17, C18		27
			1	201-0002-025	CAP .0047µf, 50V	C19		28
			1	201-0006-006	CAP 15 pf, 100V	C20		29
			1	201-0001-014	CAP 33µf, 10V.	C21		30
			11	201-0018-002	CAP 2.2µf, 25V.	C22, C23, C26-C34		31
			53	701-0001-003	CAP .1µf, 50V.	C24, C25, C35-C42, C51-C57, C68, C70-C104		32
			19	201-0018-001	CAP 6.8µf, 10V.	C58-C67, C43-C50, C105		33
								34
			2	206-0015-001	DIODE 1N4934	CR1, CR2		35
								36
			5	302-0173-001	CARD PULL			37
			2	208-0068-002	EYELET, ROLLED FLANGE	(U80)		38
			2	219-0005-007	HEAT SHRINK TUBING	(C15, C16)	3/8 I.D.	39
			48	204-0059-106	I.C. SOCKET	(U100-U147)	22 PIN	40
			10	208-0068-007	RIVET			41
			1	208-0069-004	SIL-PAD THERMAL COND.	(U80)		42

MSF-1015 REV A

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
			ALL	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
			3	208-0065-003	SCREW, NYLON	4-40 X 1/4" LG		43
			3	208-0064-005	STANDOFF,NYLON	1/4 O.D. X 3/8 X 4-40		44
			2	208-0066-004	TRANSIPAD	Q1,Q2		45
								46
			1	301-0038-001	INDUCTOR, 1W	L1		47
								48
			5	214-0007-065	RES NETWORK 470Ω	RN1-RN5	16 PIN	49
			1	214-0013-017	RES NETWORK 1K	RN6	14 PIN	50
								51
			6	214-0002-073	RES 1K,1/4W. 5%	R1-R6		52
			6	214-0002-087	RES 3.9K,1/4W. 5%	R7-R12		53
			6	214-0002-041	RES 47Ω,1/4W. 5%	R13-R18		54
			4	214-0002-056	RES 200Ω,1/4W. 5%	R19-R22		55
			1	214-0030-052	RES 560Ω,1W, 5%	R23		56
			2	214-0003-041	RES 47Ω,1/2W.,5%	R24,R25		57
			1	214-0002-XXX	RES S.A.T.,1/4W. 5%	R26		58
			1	214-0010-083	RES 511Ω,1/4W. 1%	R27		59
			1	214-0010-117	RES 2.61K,1/4W. 1%	R28		60
			1	214-0002-033	RES 22Ω,1/4W. 5%	R29		61
			1	214-0002-082	RES 2.4K,1/4W. 5%	R30		62
			4	214-0002-066	RES 510Ω,1/4W. 5%	R31-R34		63

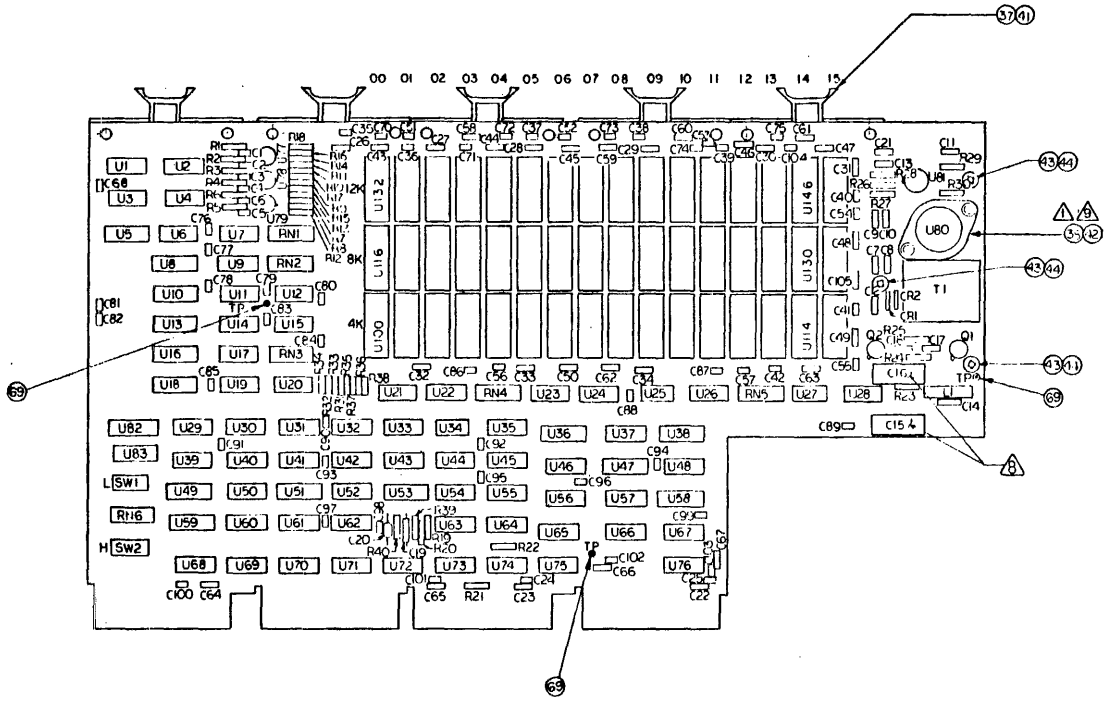
NONE | SIZE A | CODE IDENT NO 51513 | DWG NO. 303-0097-000 | REV AA | SHEET 5

MSF-1015 REV A

SIZE A | CODE IDENT NO 51513 | DWG NO. 303-0097-000 | REV AA | SHEET 6

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
			ALL	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
			4	214-0002-047	RES. 82 Ω 1/4W. 5%	R35-R38	BEND FOR .13 CENTERS	64
			1	214-0002-103	RES. 18K 1/4W. 5%	R39		65
			1	214-0002-0097	RES. 10K 1/4 W. 5%	R40		66
								67
			2	215-0008-003	DIP SWITCH 5 POS.	SW1, SW2		68
			3	208-0027-002	TERMINAL-SOLDER, P.C. BD.	(TP)		69
			1	216-0006-001	TRANSFORMER	T1		70
								71
			2	217-0003-001	TRANSISTOR 2N4238	Q1, Q2		72
			A/R	210-XXXX-XXX	MEMORY ELEMENTS 4K X 1 DYNAMIC	SEE SH. 2 FOR LOCATION AND QTY.	313-0028-000	73
								74
			A/R	223-0001-XXX	DELAY LINE	(U63, U73)	PER TABLE SH. 2	75
								76
								77
								78
								79
								80
								81
			REF	308-0027-000	P.T.R.			82
			REF	305-0097-000	SCHEMATIC			83
			REF	100-0018-000	MAIN. MANUAL			84
								85

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



9 RIVETS MUST BE SOLDERED, BOTH TOP AND BOTTOM.

8 VALUE MUST BE CHECKED BY QUALITY ASSURANCE BEFORE COVERING C15 & C16 WITH HEAT SHRINK ITEM 39.

7. ALL METAL CAN COMPONENTS MUST BE LOWER THAN ITEM 43.

6. WHEN HERMETICALLY SEALED COMPONENTS AND ASSEMBLIES ARE NOT REQUIRED THE DASH NUMBERS WILL BEGIN WITH 0XX. WHEN HERMETICALLY SEALED COMPONENTS AND ASSEMBLIES ARE REQUIRED, THE DASH NUMBERS WILL BEGIN WITH 5XX. ASSEMBLIES WILL BE MARKED ACCORDINGLY.

5. SOLDER PER 313-0005-000

4. FACTORY SERIAL NOS. TO BE MARKED IN A CLEAR AREA WITH NO OBSTRUCTION

3. MARK APPROPRIATE DASH NO. PER 313-0003-006

2. COMPONENT ALIGNMENT PER 313-0002-000.

1 INSTALL U80 AND ITEM 39 USING ITEM 42. SILICONE GREASE IS NOT USED ON THIS APPLICATION.

NOTES: (UNLESS OTHERWISE SPECIFIED)

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.X ±
.XXX

CONTRACT NO

APPROVALS DATE

DRAWN

CHECKED

MATERIAL

FINISH

NEXT ASSY USED ON

APPLICATION

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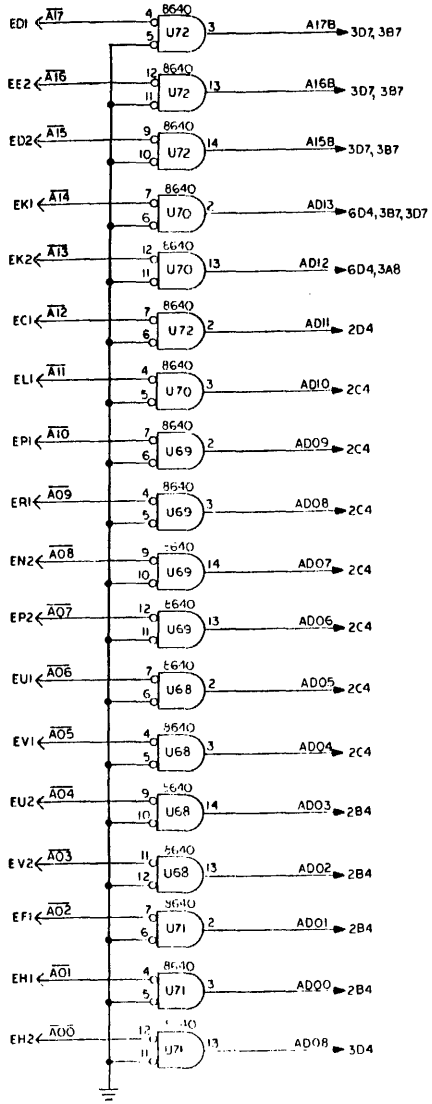
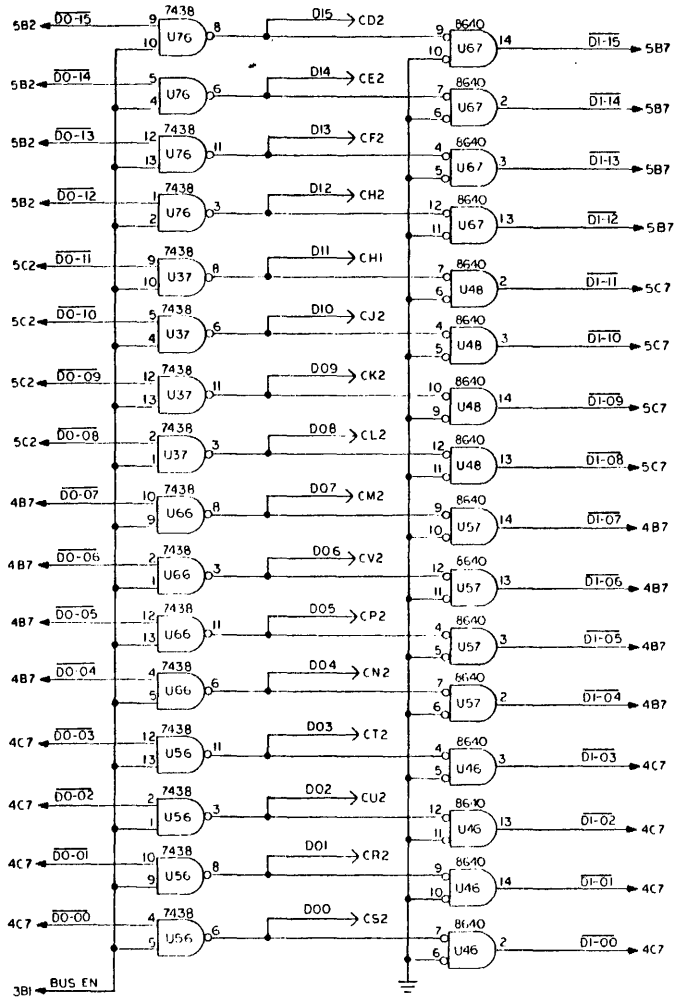
MONOLITHIC SYSTEMS CORP

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	51513	303-0097-000	Z

SCALE

SHEET 7





REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	ENG RELEASE ECO 0266?	10.1.14	TSP
	E	ADD TO SHT 7 ECO 0284	11.6.14	TSP
	F	ADD TO SHT 6 ECO 0292	12.2.14	TSP
	G	CHG'D CR2 WAS 1N4002 ECO 0302	1.9.15	TSP
	H	REVISED TIMING SHT 6 ECO 0310	3.26.15	TSP
	J	REVISED CAP VALUES SHT 7 ECO 0322	6.16.15	TSP
	K	REVISED PER ECO 0377	10-22-75	[illegible]
	L	CHANGED PER ECO 0673	6-2-77	[illegible]
	M	REVISED PER ECO 1025	4-26-78	[illegible]
	N-Y	REVISIONS NOT USED NEW ENG-002 PROCEDURE.		
	Z	REVISED PER ECO 1667	11/1/79	[illegible]

2 CAPACITORS IN MICROFARADS.
1. RESISTORS IN OHMS, 1/4W, ± 5%
NOTES. UNLESS OTHERWISE SPECIFIED

REV Z Z Z Z Z Z Z
SHEET 1 2 3 4 5 6 7
REVISION STATUS OF SHEETS

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX

MATERIAL

FINISH

NEXT ASSY USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

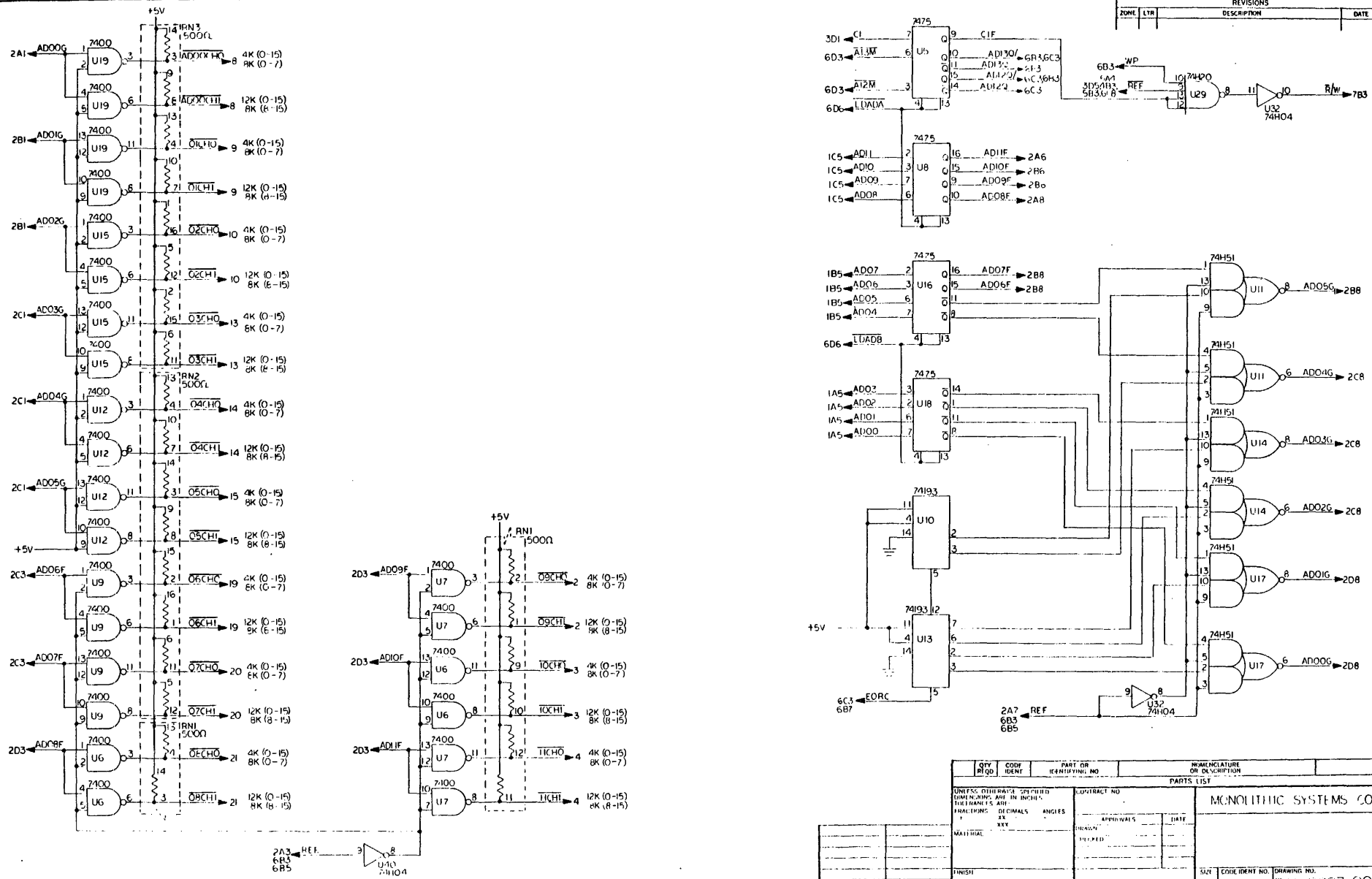
APPROVALS DATE

MONOLITHIC SYSTEMS CORP

P.C. BOARD SCHEMATIC
MSC 3303
MO VII PI/SPS

SIZE	CODE IDENT NO.	DRAWING NO.	
D	51513	305-0097-000	Z

SCALE NONE SHEET 1 OF 7



REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS | DATE

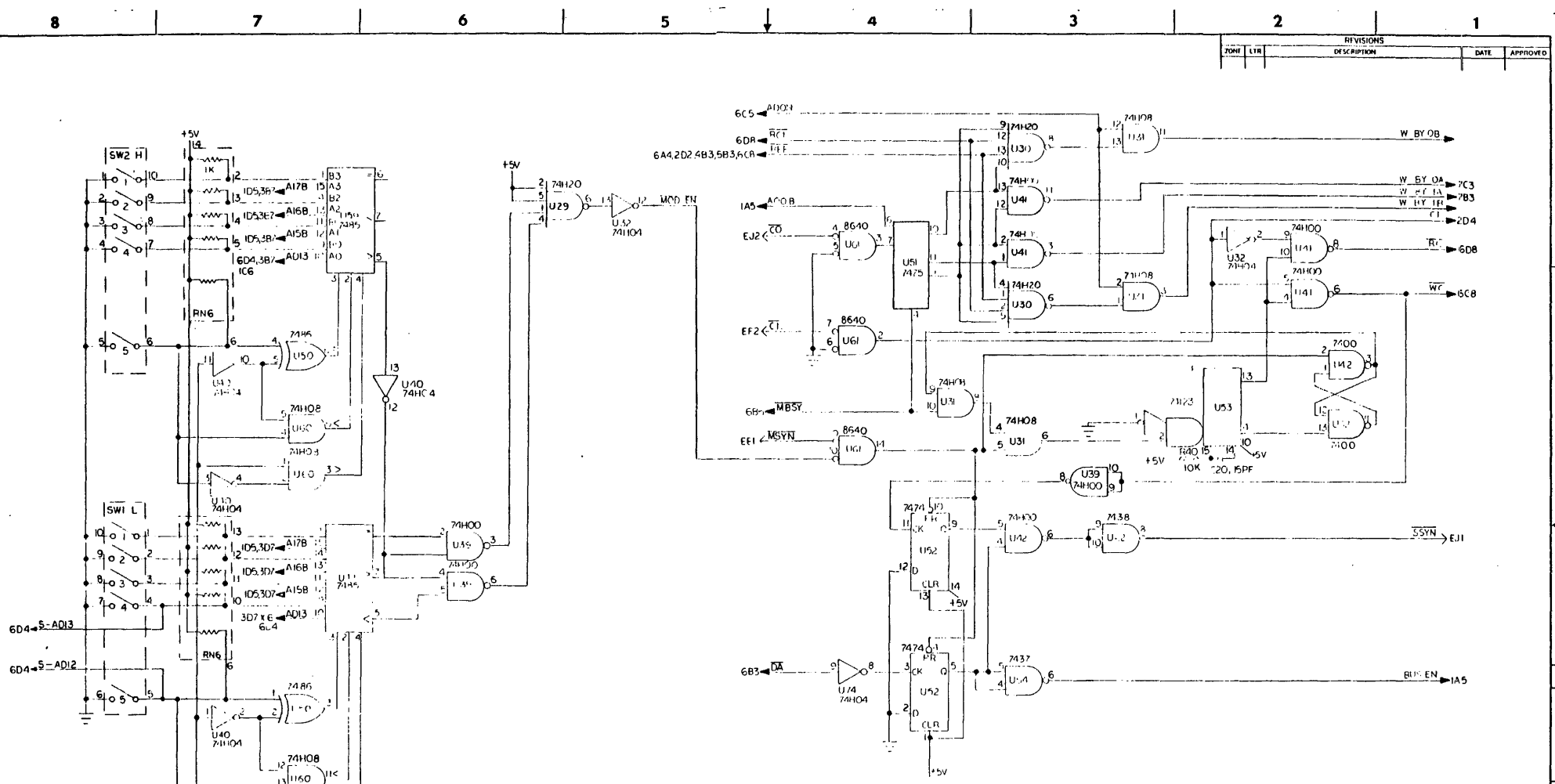
DRAWN

TRACED

MONOLITHIC SYSTEMS CORP.

SIZE D | CODE IDENT NO. 61613 | DRAWING NO. 300 0097-000 | Z

SCALE | SHEET 2 OF 7



REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX
XXX
MATERIAL
FINISH
NEXT ASSY USED ON
APPLICATION
DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN	
CHECKED	

MONOLITHIC SYSTEMS CORP.

SIZE	CODE IDENT NO.	DRAWING NO	
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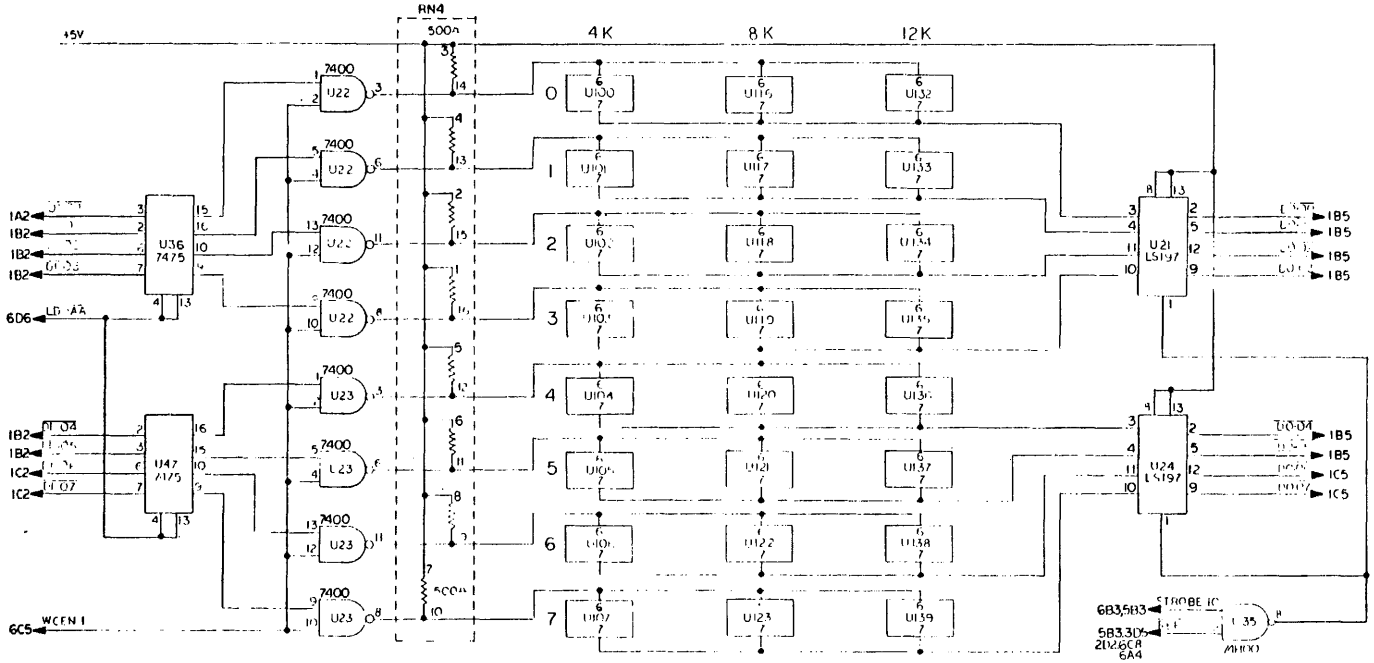
SCALE SHEET 2 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



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QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX .XXX

MATERIAL

FINISH

NEXT ASSY USED ON

APPLICATION

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CONTRACT NO

APPROVALS DATE

DRAWN

CHECKED

MONOLITHIC SYSTEMS CORP.

SIZE	CODE IDENT NO.	DRAWING NO.	
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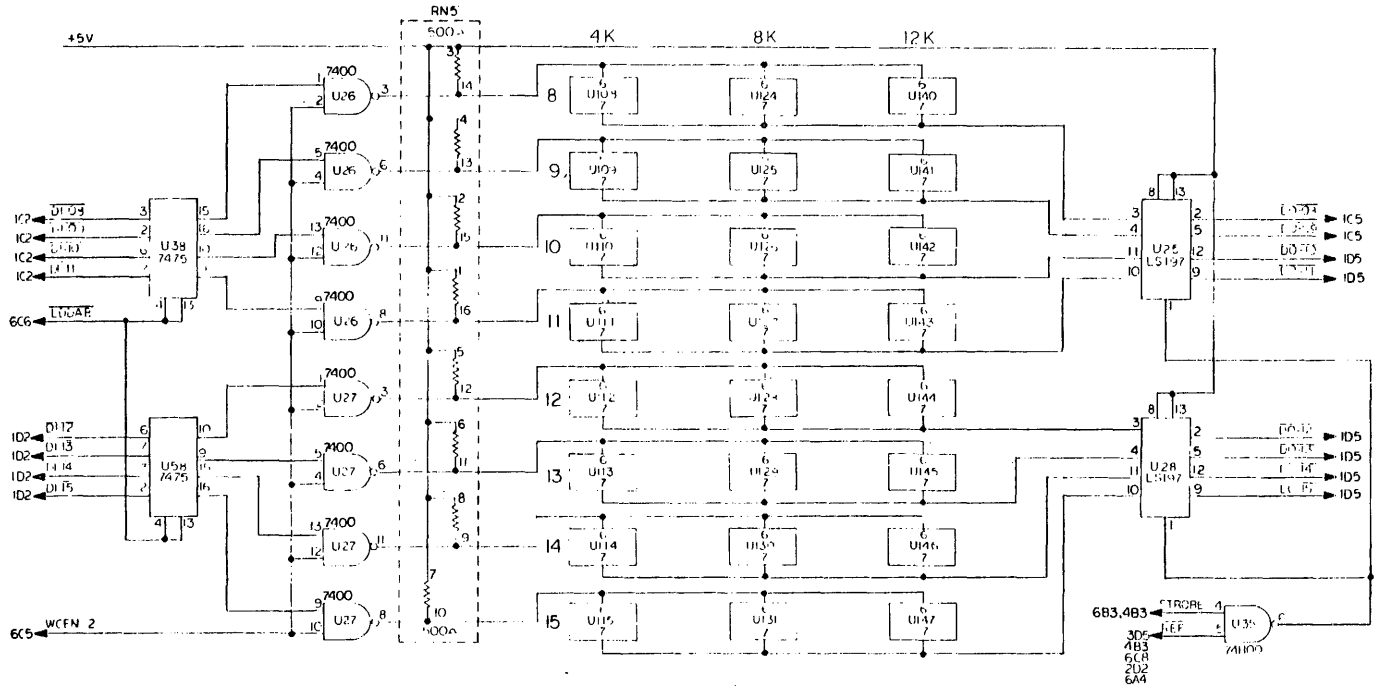
SCALE SHEET OF



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QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX .XXX

MATERIAL

FINISH

NEXT ASSY USED ON

APPLICATION

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CONTRACT NO

APPROVALS DATE

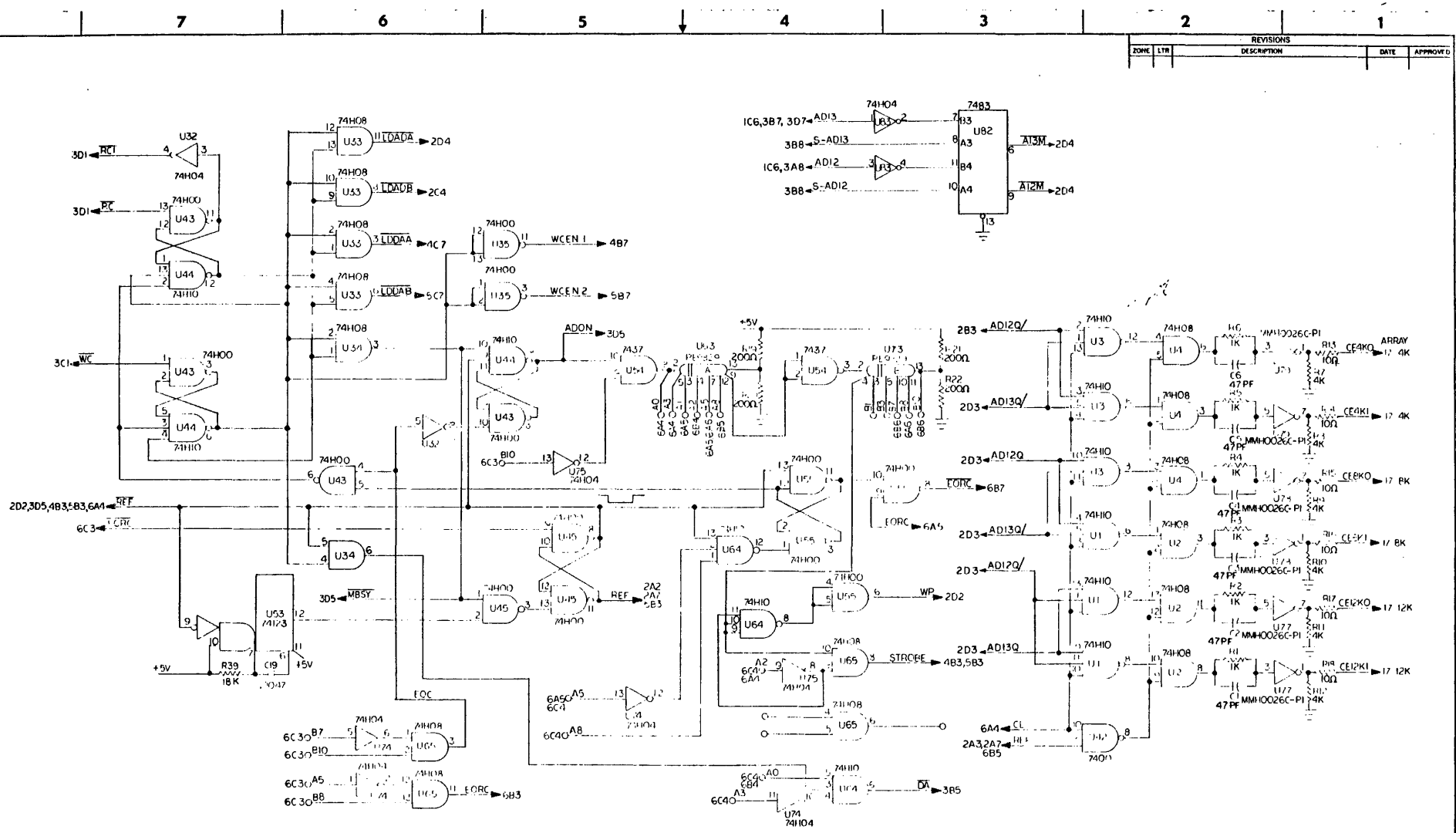
DRAWN

CHECKED

MONOLITHIC SYSTEMS CORP

SIZE D | CODE IDENT NO. | DRAWING NO. 305-0097-000 | 7

SCALE SHEET OF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ZONE | LTR | DESCRIPTION | DATE | APPROVED
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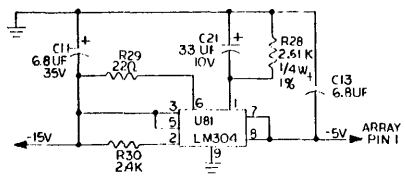
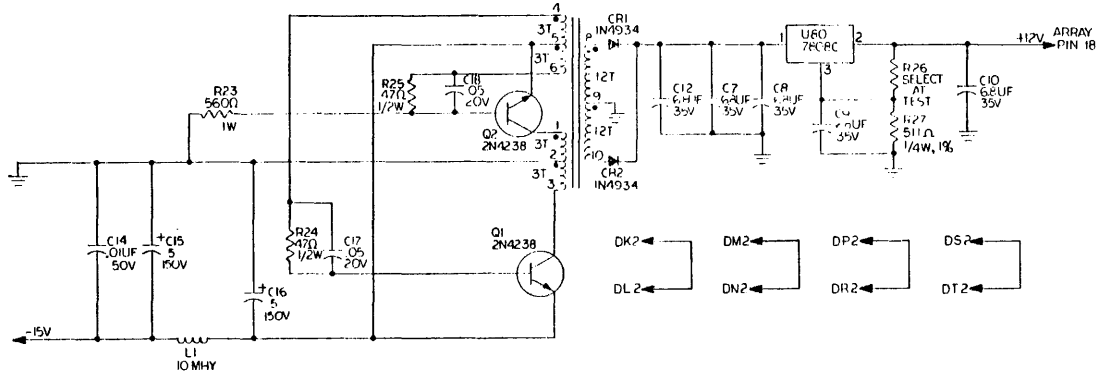
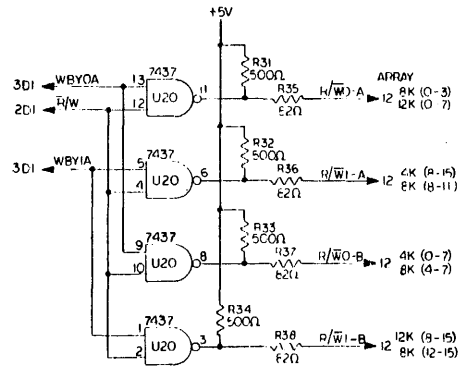
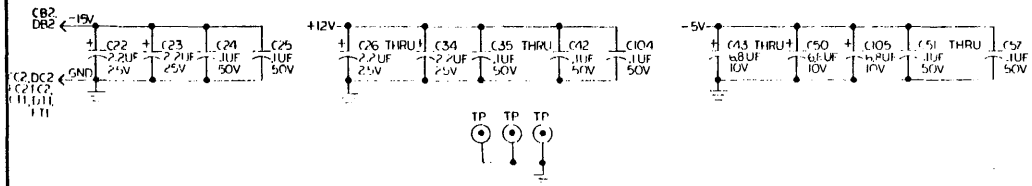
3D1 RC
3C1 WC
2D2,3D5,4B3,5B3,6A1 REF
6C3 EOC
3D5 MBSY
LDADA
LDADB
LDDAA
LDDAB
WCEN 1
WCEN 2
ADON
BIO
EORC
WP
STROBE
REF
EOC
DA
AT3M
AT2M
IC6,3B7, 3D7 AD13
3B8 S-AD13
IC6,3A8 AD12
3B8 S-AD12
2B3 AD12Q
2D3 AD13Q
ARRAY
+5V
R39 18K
C19 .0047
C6 47PF
MMH0026C-P1
PARTS LIST
MONOLITHIC SYSTEMS CORP.
DO NOT SCALE DRAWING
505-0007-000

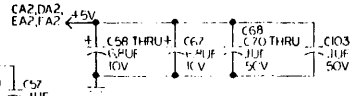
REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED











QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
		PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX .XXX

CONTRACT NO

APPROVALS DATE

MATERIAL

FINISH

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APPLICATION

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MONOLITHIC SYSTEMS CORP

SIZE	CODE IDENT NO.	DRAWING NO.	
D	91513	305 0097-000	Z

SCALE SHEET OF

Warranty Registration

Thank you for purchasing a Monolithic Systems Corp. product. So that we may expedite warranty service and provide future information about this product, please take a moment to fill out the information below and return to us.

Product Model: MSC_____

Serial number: _____

Why did you choose a Monolithic Systems product? _____

_____

What is your application for this product? _____

_____

What is the principal product/service at your location? _____

_____

Where did you first hear of Monolithic Systems products? _____

_____

Are you presently using any other Monolithic Systems product? If so, what? _____

_____

*Name*_____ *Title* _____

*Organization*_____

*Address*_____

*City, State, Zip*_____

*Phone*_____

Feedback

To make this manual as effective as possible, we would appreciate your comments and suggestions for its possible improvement.

Product Model: MSC_____

What information is not in this manual that would improve its usefulness? _____

_____

_____

What errors have you found? _____

_____

_____

How could the organization or presentation of information be improved? _____

_____

_____

Other suggestions or questions? _____

_____

*Name*_____ *Title* _____

*Organization*_____

*Address*_____

*City, State, Zip*_____

*Phone*_____

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Englewood, Colorado 80112