



MITSUBISHI 1992

SEMICONDUCTORS

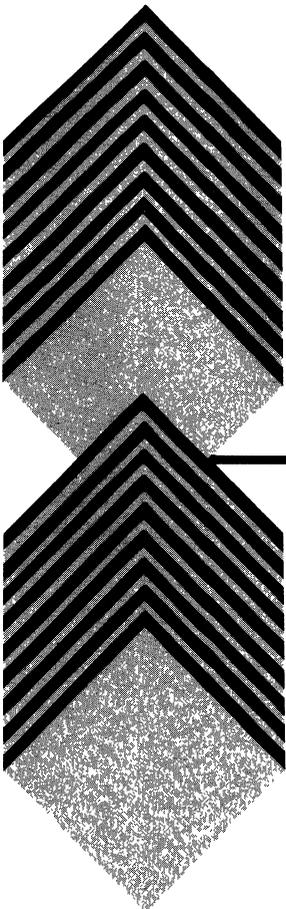
SINGLE-CHIP 8-BIT
MICROCOMPUTERS Vol. **1**

DATA BOOK

QCI

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 **MITSUBISHI
ELECTRIC**



MITSUBISHI 1992 SEMICONDUCTORS

SINGLE-CHIP 8-BIT MICROCOMPUTERS Vol. 1

DATA
BOOK

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Series MELPS 740 single-chip microcomputers

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ pwr dissipation (mW)	Min cycle time (μ s)	Max. frequency (MHz)		
M50708-XXXSP/FP ×	6K-Byte Mask-Prog. ROM, 128-Byte RAM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50740A-XXXSP/FP ×	3K-Byte Mask-Prog. ROM, 96-Byte RAM	C, Si	5±10%	15	2	4	52P4B/50P6	Note1
M50740ASP	External ROM Type, 96-Byte RAM	C, Si	5±10%	15	2	4	52P4B	Note1
M50741-XXXSP/FP ×	4K-Byte Mask-Prog. ROM, 96-Byte RAM	C, Si	5±10%	15	2	4	52P4B/50P6	Note1
M50742-XXXSP/FP ×	4K-Byte Mask-Prog. ROM, 128-Byte RAM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50743-XXXSP/FP ×	4K-Byte Mask-Prog. ROM, 128-Byte RAM	C, Si	5±10%	30	1	8	64P4B/72P6	Note1
M50744-XXXSP/FP ×	4K-Byte Mask-Prog. ROM, 144-Byte RAM	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50745-XXXSP/FP ×	6K-Byte Mask-Prog. ROM, 192-Byte RAM	C, Si	5±10%	15	2	4	64P4B/60P6	Note1
M50746-XXXSP/FP ×	6K-Byte Mask-Prog. ROM, 144-Byte RAM	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50747-XXXSP/FP ×	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±10%	30	1	8	64P4B/72P6	Note1
M50747H-XXXSP/FP	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±5%	45	0.67	12	64P4B/72P6	Note1
M50752-XXXSP ×	4K-Byte Mask-Prog. ROM, 128-Byte RAM, High Voltage Port, CR Oscillation Type	C, Si	5±10%	15	2	4	52P4B	Note1
M50753-XXXSP/FP	6K-Byte Mask-Prog. ROM, 96-Byte RAM, 8-Bit A-D Converter	C, Si	5±10%	15	2	4	64P4B/60P6	Note1
M50754-XXXSP/FP/GP	6K-Byte Mask-Prog. ROM, 160-Byte RAM, PWM, High Voltage Port, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6/64P6W	Note1
M50757-XXXSP ×	3K-Byte Mask-Prog. ROM, 96-Byte RAM, High Voltage Port, CR Oscillation Type	C, Si	5±10%	15	2	4	52P4B	Note1
M50758-XXXSP ×	3K-Byte Mask-Prog. ROM, 96-Byte RAM, High Voltage Port, Ceramic Oscillation Type	C, Si	5±10%	15	2	4	52P4B	Note1
M50930-XXXFP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	5±10%	15	1.86	4.3	80P6	Note2
M50931-XXXFP	4K-Byte Mask-Prog. ROM, 512-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	5±10%	15	1.86	4.3	80P6	
M50932-XXXFP	8K-Byte Mask-Prog. ROM, 512-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	5±10%	15	1.86	4.3	80P6	
M50933-XXXFP	6K-Byte Mask-Prog. ROM, 192-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	3.8~5.5	15	1.86	4.3	80P6	Note2
M50934-XXXFP	8K-Byte Mask-Prog. ROM, 256-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	3.8~5.5	15	1.86	4.3	80P6	
M50940-XXXSP/FP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, 8-Bit A-D Converter, High Voltage Port, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note2
M50941-XXXSP/FP	8K-Byte Mask-Prog. ROM, 192-Byte RAM, 8-Bit A-D Converter, High Voltage Port, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	
M50943-XXXSP/FP	8K-Byte Mask-Prog. ROM, 192-Byte RAM, 8-Bit A-D Converter, Serial I/O	C, Si	5±10%	30	1	8	64P4B/60P6	Note1
M50944-XXXSP/FP	12K-Byte Mask-Prog. ROM, 192-Byte RAM, 8-Bit A-D Converter, Two Serial I/Os	C, Si	3~5.5	15	1.91	4.19	64P4B/64P6S	Note2
M50945-XXXSP/FP	16K-Byte Mask-Prog. ROM, 256-Byte RAM, 8-Bit A-D Converter, High Voltage Port, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note2
M50950-XXXSP	6K-Byte Mask-Prog. ROM, 144-Byte RAM, High Voltage Port, Two Serial I/Os	C, Si	5±10%	20	1.6	5	52P4B	Note1
M50951-XXXSP	4K-Byte Mask-Prog. ROM, 144-Byte RAM, High Voltage Port, Two Serial I/Os	C, Si	5±10%	20	1.6	5	52P4B	Note1
M50954-XXXSP/FP/GP	8K-Byte Mask-Prog. ROM, 192-Byte RAM, PWM, High Voltage Port, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6/64P6W	Note1
M50955-XXXSP/FP/GP	10K-Byte Mask-Prog. ROM, 192-Byte RAM, PWM, High Voltage Port, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6/64P6W	Note1

* : New product ** : Under development

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MITSUBISHI MICROCOMPUTERS INDEX BY FUNCTION

Series MELPS 740 single-chip microcomputers (continued)

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ. pwr dissipation (mW)	Min cycle time (μ s)	Max frequency (MHz)		
M50957-XXXSP/FP	10K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, High Voltage Port, 4-Bit Comparator, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6	Note2
M50958-XXXSP/FP *	12K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, High Voltage Port, 4-Bit Comparator, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6	
M50959-XXXSP/FP *	16K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, High Voltage Port, 4-Bit Comparator, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6	
M50963-XXXSP/FP *	10K-Byte Mask-Prog. ROM, 160-Byte RAM, 8-Bit A-D Converter, 5-Bit D-A Converter, PWM, Serial I/O	C, Si	5 \pm 10%	15	2	4	64P4B/72P6	Note1
M50964-XXXSP/FP *	6K-Byte Mask-Prog. ROM, 160-Byte RAM, 8-Bit A-D Converter, 5-Bit D-A Converter, PWM, Serial I/O	C, Si	5 \pm 10%	15	2	4	64P4B/72P6	Note1
M50734SP/FP	External ROM, RAM Type, 5-Timer, 8-Bit A-D Converter, Serial I/O	C, Si	5 \pm 10%	30	1	8	64P4B/72P6	Note2
M50734SP/FP-10	External ROM, RAM Type, 5-Timer, 8-Bit A-D Converter, Serial I/O	C, Si	5 \pm 10%	35	0.8	10	64P4B/72P6	
M37100M8-XXXSP/FP	16K-Byte Mask-Prog ROM, 320-Byte RAM, Two Serial I/Os, A-D Converter, OSD Function	C, Si	5 \pm 10%	27.5	2	4	64P4B/80P6	2-3
M37102M8-XXXSP/FP *	16K-Byte Mask-Prog. ROM, 320-Byte RAM, Two Serial I/Os, A-D Converter, PWM, OSD Function	C, Si	5 \pm 10%	110	1	4	64P4B/80P6N	2-50
M37103M4-XXXSP *	8K-Byte Mask-Prog ROM, 320-Byte RAM, Serial I/O, A-D Converter, PWM, OSD Function	C, Si	5 \pm 10%	35	2	4	64P4B	2-101
M37120M6-XXXFP *	12K-Byte Mask-Prog. ROM, 256-Byte RAM, Serial I/O, A-D Converter, D-A Converter, OSD Function	C, Si	5 \pm 10%	75	1	4	80P6N	3-3
M37201M6-XXXSP *	24K-Byte Mask-Prog ROM, 384-Byte RAM, Two Serial I/Os, A-D Converter, PWM, OSD Function	C, Si	5 \pm 10%	110	1	4	64P4B	2-50
M37202M3-XXXSP **	12K-Byte Mask-Prog ROM, 256-Byte RAM, Serial I/O, A-D Converter, PWM, OSD Function, Four Timers	C, Si	5 \pm 10%	110	1	4	64P4B	2-147
M37204M8-XXXSP **	32K-Byte Mask-Prog. ROM, 512-Byte RAM, Serial I/O, A-D Converter, D-A Converter, PWM, OSD Function, Four Timers	C, Si	5 \pm 10%	110	1	4	64P4B	2-195
M37250M6-XXXSP *	24K-Byte Mask-Prog ROM, 384-Byte RAM, Serial I/O, A-D Converter, PWM, OSD Function, PLL Function, Four Timers	C, Si	5 \pm 10%	137.5	1	4	64P4B	2-251
M37260M6-XXXSP **	24K-Byte Mask-Prog ROM, 320-Byte RAM, 8-Byte Serial I/O, OSD Function, Four Timers	C, Si	5 \pm 10%	110	1	4	52P4B	2-299
M37408M2-XXXSP/FP **	4K-Byte Mask-Prog ROM, 128-Byte RAM, Dual-Port RAM, UART, Bus Interface, Timer	C, Si	5 \pm 10%	50	0.8	10	42P4B/44P6N	3-47
M37409M2-XXXSP/FP	4K-Byte Mask-Prog ROM, 128-Byte RAM, Dual-Port RAM, Three UARTs, Bus Interface, Timer	C, Si	5 \pm 10%	50	0.8	10	52P4B/56P6N	3-73
M37410M3HXXXFP	6K-Byte Mask-Prog. ROM, 192-Byte RAM, Serial I/O, A-D Converter, LCD Controller/Driver	C, Si	2.5~5.5	30	1	8	80P6S	3-101
M37410M4HXXXFP	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	2.5~5.5	30	1	8	80P6S	
M37410M6HXXXFP	12K-Byte Mask-Prog ROM, 256-Byte RAM	C, Si	2.5~5.5	30	1	8	80P6S	
M37412M4-XXXFP	8K-Byte Mask-Prog ROM, 160-Byte RAM, Serial I/O, PWM, 8-Bit A-D Converter, 5-Bit D-A Converter	C, Si	5 \pm 10%	15	2	4	72P6	3-137
M37413M4HXXXFP	8K-Byte Mask-Prog. ROM, 256-Byte RAM, Serial I/O, A-D Converter	C, Si	2.5~5.5	30	1	8	80P6S	3-167
M37413M6HXXXFP **	12K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	2.5~5.5	30	1	8	80P6S	
M37414M5-XXXFP *	10K-Byte Mask-Prog ROM, 160-Byte RAM, Serial I/O, PWM, 8-Bit A-D Converter, 5-Bit D-A Converter	C, Si	5 \pm 10%	15	2	4	72P6	3-199
M37415M4-XXXFP	8K-Byte Mask-Prog ROM, 512-Byte RAM, Serial I/O, LCD Controller/Driver, DTMF Generator	C, Si	2.5~5.5	20	2.5	3.2	80P6	3-230

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MITSUBISHI MICROCOMPUTERS INDEX BY FUNCTION

■ Series MELPS 740 single-chip microcomputers (continued)

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ pwr dissipation (mW)	Min cycle time (μ s)	Max frequency (MHz)		
M37418M2-XXXSP/FP *	4K-Byte Mask-Prog. ROM, 128-Byte RAM, UART, Comparator, Bus interface, Key on wake up	C, Si	5 \pm 10%	50	1	8	52P4B/56P6N	3-263
M37420M4-XXXSP	8K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, Serial I/O, A-D Converter, D-A Converter, Timer	C, Si	5 \pm 10%	30	1	8	52P4B	3-294
M37420M6-XXXSP	12K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5 \pm 10%	30	1	8	52P4B	
M37421M6-XXXSP/FP	12K-Byte Mask-Prog. ROM, 320-Byte RAM, PWM, Serial I/O, High Voltage Port, 4-Bit Comparator	C, Si	5 \pm 10%	25	0.95	4.2	64P4B/72P6	3-323
M37424M8-XXXSP **	16K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, Serial I/O, 8-Bit A-D Converter, 5-Bit D-A Converter, Timer	C, Si	5 \pm 10%	30	1	4	64P4B	3-354
M37524M4-XXXSP **	16K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, Serial I/O, 8-Bit A-D Converter, 5-Bit D-A Converter, Timer	C, Si	5 \pm 10%	30	1	4	64P4B	
M37428M4-XXXFP **	8K-Byte Mask-Prog. ROM, 384-Byte RAM, UART, LCD Controller/Driver, Timer	C, Si	5 \pm 10%	15	1	8	80P6N	3-391
M37450M2-XXXSP/FP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, 8-Bit A-D Converter, 8-Bit D-A Converter, UART, DBB, Three Timers, PWM	C, Si	5 \pm 10%	30	0.8	10	64P4B/80P6	Note3
M37450M4-XXXSP/FP	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5 \pm 10%	30	0.8	10	64P4B/80P6	
M37450M8-XXXSP/FP	16K-Byte Mask-Prog. ROM, 384-Byte RAM	C, Si	5 \pm 10%	30	0.8	10	64P4B/80P6	
M37450S1SP/FP	External ROM, 128-Byte RAM	C, Si	5 \pm 10%	30	0.8	10	64P4B/80P6	Note3
M37450S2SP/FP	External ROM, 256-Byte RAM	C, Si	5 \pm 10%	30	0.8	10	64P4B/80P6	
M37450S4SP/FP	External ROM, 384-Byte RAM	C, Si	5 \pm 10%	30	0.8	10	64P4B/80P6	
M37451M4-XXXSP/FP/GP *	8K-Byte Mask-Prog. ROM, 256-Byte RAM, 8-Bit A-D Converter, 8-Bit D-A Converter, UART, DBB, Three Timers, PWM	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N/80P6S	Note3
M37451M8-XXXSP/FP/GP *	16K-Byte Mask-Prog. ROM, 384-Byte RAM	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N/80P6S	Note3
M37451M8-XXXSP/FP/GP **	24K-Byte Mask-Prog. ROM, 512-Byte RAM	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N/80P6S	Note3
M37451SSP/FP/GP **	External ROM, 1024-Byte RAM	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N/80P6S	Note3
M37470M2-XXXSP *	4K-Byte Mask-Prog. ROM, 128-Byte RAM, Serial I/O, A-D Converter	C, Si	2.7~5.5	17.5	1	4	32P4B	Note3
M37470M4-XXXSP *	8K-Byte Mask-Prog. ROM, 192-Byte RAM	C, Si	2.7~5.5	17.5	1	4	32P4B	
M37470M8-XXXSP *	16K-Byte Mask-Prog. ROM, 384-Byte RAM	C, Si	2.7~5.5	17.5	1	4	32P4B	
M37471M2-XXXSP/FP *	4K-Byte Mask-Prog. ROM, 128-Byte RAM, Serial I/O, A-D Converter	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	Note3
M37471M4-XXXSP/FP *	8K-Byte Mask-Prog. ROM, 192-Byte RAM	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	
M37471M8-XXXSP/FP *	16K-Byte Mask-Prog. ROM, 384-Byte RAM	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	

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MITSUBISHI MICROCOMPUTERS INDEX BY FUNCTION

■ Extended operating temperature version of microcomputers

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ pwr dissipation (mW)	Min cycle time (μ s)	Max frequency (MHz)		
M50744T-XXXSP ×	4K-Byte Mask-Prog. ROM,144-Byte RAM, Extended Operating Temperature Version of M50744-XXXSP	C, Si	5 \pm 10%	15	2	4	64P4B	Note1
M50747T-XXXSP	8K-Byte Mask-Prog ROM,256-Byte RAM, Extended Operating Temperature Version of M50747-XXXSP	C, Si	5 \pm 10%	30	1	8	64P4B	Note1
M50753T-XXXSP	6K-Byte Mask-Prog. ROM,96-Byte RAM, Extended Operating Temperature Version of M50753-XXXSP	C, Si	5 \pm 10%	15	2	4	64P4B	Note1
M50930T-XXXFP	4K-Byte Mask-Prog ROM,128-Byte RAM, Extended Operating Temperature Version of M50930-XXXFP	C, Si	5 \pm 10%	20	1.86	4.3	80P6	Note1
M37450M4TXXXSP/J	8K-Byte Mask-Prog ROM, 256-Byte RAM, Extended Operating Temperature Version of M37450M4-XXXSP	C, Si	5 \pm 10%	30	0.8	10	64P4B/84P0	Note3
M37451M4DXXXSP/FP ★★	8K-Byte Mask-Prog. ROM, 256-Byte RAM, Extended Operating Temperature Version of M37451M4-XXXSP/FP	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N	Note3
M37451M8DXXXSP/FP ★★	16K-Byte Mask-Prog ROM, 384-Byte RAM, Extended Operating Temperature Version of M37451M8-XXXSP/FP	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N	Note3

■ Piggyback type microcomputers (EPROM mounted type)

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ pwr dissipation (mW)	Min cycle time (μ s)	Max frequency (MHz)		
M50740-PGYS	Piggyback for M50740/M50741	C, Si	5 \pm 5%	—	2	4	52S1M	Note1
M50742-PGYS	Piggyback for M50742/M50708	C, Si	5 \pm 5%	—	2	4	64S1M	Note1
M50743-PGYS	Piggyback for M50743	C, Si	5 \pm 5%	—	1	8	64S1M	Note1
M50745-PGYS	Piggyback for M50745	C, Si	5 \pm 5%	—	2	4	64S1M	Note1
M50752-PGYS	Piggyback for M50757/M50752	C, Si	5 \pm 5%	—	2	4	52S1M	Note1
M50753-PGYS	Piggyback for M50753	C, Si	5 \pm 5%	—	2	4	64S1M	Note1
M50931-PGYS	Piggyback for M50930/M50931/M50932	C, Si	5 \pm 5%	—	2	4	80S6M	Note1
M50945-PGYS	Piggyback for M50940/M50941/M50945	C, Si	5 \pm 5%	—	2	4	64S1M	Note2
M50950-PGYS	Piggyback for M50950/M50951	C, Si	5 \pm 5%	—	1.6	5	52S1M	Note1
M50955-PGYS	Piggyback for M50754/M50954/M50955	C, Si	5 \pm 5%	—	1.9	4.2	64S1M	Note1
M50957-PGYS	Piggyback for M50957/M50958/M50959	C, Si	5 \pm 5%	—	1.9	4.2	64S1M	Note2
M50964-PGYS	Piggyback for M50964/M50963	C, Si	5 \pm 5%	—	2	4	64S1M	Note1
M37409PSS *	Piggyback for M37409M2-XXXSP	C, Si	5 \pm 5%	—	0.8	10	52S1M	3—397
M37415PFS	Piggyback for M37415M4-XXXFP	C, Si	3.0~5.5	—	2.5	3.2	80S6M	3—402
M37421P-000SS M37421P-001SS	Piggyback for M37421M6-XXXSP	C, Si	5 \pm 5%	—	0.95	4.2	64S1M	3—410
M37450PSS	Piggyback for M37450M2/M4/M8-XXXSP	C, Si	5 \pm 5%	—	0.8	10	64S1M	Note3
M37450PFS	Piggyback for M37450M2/M4/M8-XXXFP	C, Si	5 \pm 5%	—	0.8	10	80S6M	Note3

★ : New product ★★ : Under development

Note1 : Refer to the "1989 MITSUBISHI SEMICONDUCTORS DATA BOOK (SINGLE-CHIP 8-BIT MICROCOMPUTERS)"

2 : Refer to the "1990 MITSUBISHI SEMICONDUCTORS DATA BOOK (SINGLE-CHIP 8-BIT MICROCOMPUTERS Enlarged edition)"

3 : Refer to the "1992 MITSUBISHI SEMICONDUCTORS DATA BOOK (SINGLE-CHIP 8-BIT MICROCOMPUTERS) vol 2"

※ : The production of this product is no longer planned due to announcement of new series or upgrades

MITSUBISHI MICROCOMPUTERS INDEX BY FUNCTION

■ Built-in PROM type microcomputers

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ. pwr dissipation (mW)	Min cycle time (μ s)	Max frequency (MHz)		
M50746E-XXXSP/FP	One Time Programmable Version of M50746-XXXSP/FP	C, Si	5 \pm 5%	15	2	4	64P4B/72P6	Note1
M50746ES/EFS	PROM Version of M50746-XXXSP/FP	C, Si	5 \pm 5%	15	2	4	64S1B/72S6	Note1
M50747E-XXXSP/FP	One Time Programmable Version of M50747-XXXSP/FP	C, Si	5 \pm 5%	30	1	8	64P4B/72P6	Note1
M50747ES/EFS	PROM Version of M50747-XXXSP/FP	C, Si	5 \pm 5%	30	1	8	64S1B/72S6	Note1
M50944E-XXXSP/FP	One Time Programmable Version of M50944-XXXSP/FP	C, Si	3~5.5	15	1.9	4.2	64P4B/64P6S	Note1
M50944ES	PROM Version of M50944-XXXSP	C, Si	3~5.5	15	1.9	4.2	64S1B	
M50957E-XXXSP	One Time Programmable Version of M50957-XXXSP	C, Si	5 \pm 5%	20	1.9	4.2	64P4B	Note1
M50957ES	PROM Version of M50957-XXXSP	C, Si	5 \pm 5%	20	1.9	4.2	64S1B	
M50963E-XXXSP/FP	One Time Programmable Version of M50963-XXXSP	C, Si	5 \pm 5%	15	2	4	64P4B/72P6	Note1
M50963ES/EFS	PROM Version of M50963-XXXSP/FP	C, Si	5 \pm 5%	15	2	4	64S1B/72S6	Note1
M37102E8-XXXSP/FP *	One Time Programmable Version of M37102M8-XXXSP/FP	C, Si	5 \pm 10%	110	1	4	64P4B/80P6N	2-354
M37120E6-XXXFP *	PROM Version of M37120M6-XXXFP	C, Si	5 \pm 5%	75	1	4	80P6N	3-416
M37201E6-XXXSP *	One Time Programmable Version of M37201M6-XXXSP		5 \pm 10%	110	1	4	64P4B	2-354
M37410E6HXXXFP	One Time Programmable Version of M37410M6H-XXXFP	C, Si	2.5~5.5	30	1	8	80P6S	3-423
M37410E6HFS	PROM Version of M37410M6H-XXXFP	C, Si	2.5~5.5	30	1	8	80S6	
M37412E5-XXXFP	One Time Programmable Version of M37412M4-XXXFP	C, Si	5 \pm 5%	15	2	4	72P6	3-434
M37413E6HXXXFP**	One Time Programmable Version of M37413M6H-XXXFP	C, Si	2.5~5.5	30	1	8	80P6S	3-448
M37413E6HFS **	PROM Version of M37413M6H-XXXFP	C, Si	5 \pm 5%	30	1	8	80S6	
M37414E5-XXXFP *	One Time Programmable Version of M37414M5-XXXFP	C, Si	5 \pm 5%	15	2	4	72P6	3-458
M37420E6-XXXSP *	One Time Programmable Version of M37420M6-XXXSP	C, Si	5 \pm 5%	30	1	8	52P4B	3-472
M37420E6SS *	PROM Version of M37420M6-XXXSP	C, Si	5 \pm 5%	30	1	8	52S1	
M37424E8-XXXSP **	One Time Programmable Version of M37424M8-XXXSP	C, Si	5 \pm 10%	30	1	4	64P4B	3-480
M37524E4-XXXSP **	One Time Programmable Version of M37524M4-XXXSP	C, Si	5 \pm 10%	30	1	4	64P4B	
M37450E4-XXXSP/FP	One Time Programmable Version of M37450M4-XXXSP/FP	C, Si	5 \pm 5%	30	0.8	10	64P4B/80P6	Note3
M37450E4SS/FS	PROM Version of M37450M4-XXXSP/FP	C, Si	5 \pm 5%	30	0.8	10	64S1B/80S6	
M37450E8-XXXSP/FP *	One Time Programmable Version of M37450M8-XXXSP/FP	C, Si	5 \pm 5%	30	0.8	10	64P4B/80P6	Note3
M37450E8SS/FS *	PROM Version of M37450M8-XXXSP/FP	C, Si	5 \pm 5%	30	0.8	10	64S1B/80D0	
M37450E4TXXXSP/J *	One Time Programmable Version of M37450M4TXXXSP/J	C, Si	5 \pm 5%	30	0.8	10	64P4B/84P0	Note3
M37451E4-XXXSP/FP/GP *	One Time Programmable Version of M37451M4-XXXSP/FP/GP	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N/80P6S	Note3
M37451E4SS/FS *	PROM Version of M37451M4-XXXSP/FP	C, Si	5 \pm 10%	40	0.64	12.5	64S1B/80D0	Note3
M37451E8-XXXSP/FP/GP *	One Time Programmable Version of M37451M8-XXXSP/FP/GP	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N/80P6S	Note3
M37451E8SS/FS *	PROM Version of M37451M8-XXXSP/FP	C, Si	5 \pm 10%	40	0.64	12.5	64S1B/80D0	Note3
M37451EC-XXXSP/FP/GP **	One Time Programmable Version of M37451MC-XXXSP/FP/GP	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N/80P6S	Note3
M37451ECSS/FS **	PROM Version of M37451MC-XXXSP/FP	C, Si	5 \pm 10%	40	0.64	12.5	64S1B/80D0	Note3
M37451E4DXXXSP/FP **	One Time Programmable Version of M37451M4TXXXSP/FP	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N	Note3
M37451E8DXXXSP/FP **	One Time Programmable Version of M37451M8TXXXSP/FP	C, Si	5 \pm 10%	40	0.64	12.5	64P4B/80P6N	Note3
M37470E4-XXXSP *	One Time Programmable Version of M37470M4-XXXSP	C, Si	2.7~5.5	17.5	1	4	32P4B	Note3
M37470E8-XXXSP *	One Time Programmable Version of M37470M8-XXXSP	C, Si	2.7~5.5	17.5	1	4	32P4B	Note3
M37471E4-XXXSP/FP *	One Time Programmable Version of M37471M4-XXXSP/FP	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	Note3
M37471E8-XXXSP/FP *	One Time Programmable Version of M37471M8-XXXSP/FP	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	Note3
M37471E8SS *	PROM Version of M37471M8-XXXSP	C, Si	2.7~5.5	17.5	1	4	42S1B	Note3

* : New product ** : Under development

Note1 : Refer to the "1989 MITSUBISHI SEMICONDUCTORS DATA BOOK (SINGLE-CHIP 8-BIT MICROCOMPUTERS)"

2 : Refer to the "1990 MITSUBISHI SEMICONDUCTORS DATA BOOK (SINGLE-CHIP 8-BIT MICROCOMPUTERS Enlarged edition)"

3 : Refer to the "1992 MITSUBISHI SEMICONDUCTORS DATA BOOK (SINGLE-CHIP 8-BIT MICROCOMPUTERS) vol 2"

※ : The production of this product is no longer planned due to announcement of new series or upgrades

■ Series 38000 single-chip microcomputers

Refer to the "1992 MITSUBISHI SEMICONDUCTORS DATA BOOK (SINGLE-CHIP 8-BIT MICROCOMPUTERS) Vol. 2."

MITSUBISHI MICROCOMPUTERS DEVELOPMENT SUPPORT SYSTEMS

Development support systems (1)

MELPS 740		Assembler	Debug system			For evaluation
Type name	Processor mode		Debugger	Option board	Control software	
M50740A-XXXSP/FP M50741-XXXSP/FP M50740ASP	Single-chip mode	SRA74	PC4000E	PCA4040	RTT74	M50740-PGYS
M50742-XXXSP/FP M50708-XXXSP/FP	Single-chip mode			PCA4042		M50742-PGYS
M50743-XXXSP/FP	Single-chip mode			PCA4043 or PCA4043R		M50743-PGYS
M50744-XXXSP/FP M50744T-XXXSP M50746-XXXSP/FP M50746E-XXXSP/FP M50746ES/EFS	Single-chip mode Microprocessor mode			PCA4044G02 or PCA4044R PCA4044XG02		M50746ES/EFS (Note 2)
M50745-XXXSP/FP	Single-chip mode			PCA4045 or PCA4045R		M50745-PGYS
M50747-XXXSP/FP M50747H-XXXSP/FP M50747T-XXXSP M50747E-XXXSP/FP M50747ES/EFS	Single-chip mode Microprocessor mode			PCA4047G02 or PCA4047RG02 PCA4047XG02 or PCA4047XR02		M50747ES/EFS (Note 2)
M50752-XXXSP M50757-XXXSP M50758-XXXSP	Single-chip mode			PCA4057		M50752-PGYS
M50753-XXXSP/FP M50753T-XXXSP	Single-chip mode			PCA4053		M50753-PGYS (Note 2)
M50754-XXXSP/FP/GP M50954-XXXSP/FP/GP M50955-XXXSP/FP/GP	Single-chip mode			PCA4054G02 or PCA4054RG02		M50955-PGYS
M50930-XXXFP M50930T-XXXFP M50931-XXXFP M50932-XXXFP M50933-XXXFP M50934-XXXFP	Single-chip mode			PCA4093 or PCA4093R		M50931-PGYS (Note 2,3)
M50940-XXXSP/FP M50941-XXXSP/FP M50945-XXXSP/FP	Single-chip mode			PCA4094 or PCA4094RG02		M50945-PGYS
M50943-XXXSP/FP	Single-chip mode			PCA4033		PCA4333G02 (Note 1)
M50944-XXXSP/FP M50944E-XXXSP/FP M50944ES	Single-chip mode			PCA7044		M50944ES
M50950-XXXSP M50951-XXXSP	Single-chip mode			PCA4095		M50950-PGYS
M50957-XXXSP/FP M50957E-XXXSP M50957ES M50958-XXXSP/FP M50959-XXXSP/FP	Single-chip mode			PCA4054G02 or PCA4054RG02		M50957-PGYS M50957ES
M50963-XXXSP/FP M50963E-XXXSP/FP M50963ES/EFS M50964-XXXSP/FP	Single-chip mode			PCA4064 or PCA4064R		M50963ES/EFS

★ : New products ★★ : Under development

Note 1 : Evaluation board

2 : Notes for operating temperature range about the extended operating temperature version microcomputer

3 : Notes for supply voltage range about the M50932-XXXFP, M50933-XXXFP.

MITSUBISHI MICROCOMPUTERS DEVELOPMENT SUPPORT SYSTEMS

Development support systems (2)

MELPS 740		Assembler	Debug system			For evaluation		
Type name	Processor mode		Debugger	Option board	Control software			
M37100M8-XXXSP/FP	Single-chip mode	SRA74	PC4000E	M37100T-OPT or M37100T2-RTT	RTT74	M37100P-000SS		
M37102M8-XXXSP/FP M37102E8-XXXSP/FP M37102E8SS/FS	Single-chip mode			M37102T-RTT		M37102E8SS/FS**		
M37103M4-XXXSP	Single-chip mode			M37100T2-RTT		—		
M37120M6-XXXFP M37120E6-XXXFP	Single-chip mode		M37120T-RTT	M37120E6-XXXFP*				
M37201M6-XXXSP M37201E6-XXXSP M37201E6SS	Single-chip mode		PC4000E + PC4600*	M37201T5-POD*	M37201E6SS**			
M37202M3-XXXSP M37202E3-XXXSP M37202E3SS					M37202E3SS**			
M37204M8-XXXSP M37204E8-XXXSP M37204E8SS					M37204E8SS**			
M37250M6-XXXSP M37250E6-XXXSP M37250E6SS					Single-chip mode	PC4000E	M37250T-RTT*	M37250E6SS**
M37260M6-XXXSP M37260E6-XXXSP M37260E6SS	Single-chip mode		PC4000E + PC4600*	M37260T5-POD*	M37260E6SS**			
	Microprocessor mode					M37260TX-OPT* (Be necessary to order producing this board)		
M37408M2-XXXSP/FP	Single-chip mode			PC4000E	—	RTT74	—	
M37409M2-XXXSP/FP	Single-chip mode				M37409T-OPT		M37409PSS*	
M37410M3HXXXFP M37410M4HXXXFP M37410M6HXXXFP M37410E6HXXXFP M37410E6HFS	Single-chip mode				M37410T-OPT		M37410E6HFS	
M37412M4-XXXFP M37412E5-XXXFP	Single-chip mode				M37412T-OPT		M37412E5-XXXFP	
M37413M4HXXXFP M37413M6HXXXFP M37413E6HXXXFP M37413E6HFS	Single-chip mode				M37413T-RTT		M37413E6HFS**	
M37414M5-XXXFP M37414E5-XXXFP	Single-chip mode				M37414T-RTT		M37414E5-XXXFP*	
M37415M4-XXXFP	Single-chip mode				M37415T-OPT		M37415PFS	
M37416M2-XXXSP/FP	Single-chip mode				M37416T-RTT*		—	
M37420M4-XXXSP M37420M6-XXXSP M37420E6-XXXSP M37420E6SS	Single-chip mode				M37420T-OPT		M37420E6SS*	
M37421M6-XXXSP/FP	Single-chip mode				M37421T-OPT		M37421P-000SS M37421P-001SS	
M37424M8-XXXSP M37424E8-XXXSP M37424E8SS	Single-chip mode				M37424T-RTT*		M37424E8SS**	
M37524M4-XXXSP M37524E4-XXXSP M37524E4SS	Single-chip mode				M37524T-RTT*		M37524E4SS**	
M37428M4-XXXFP	Single-chip mode				PC4000E + PC4600*(Note2)		M37428RFS	—

★ : New products ** : Under development

Note 1 : Evaluation board Note 2 : Be necessary to order exchanging the monitor ROM.

MITSUBISHI MICROCOMPUTERS DEVELOPMENT SUPPORT SYSTEMS

Development support systems (3)

MELPS 740		Assembler	Debug system			For evaluation
Type name	Processor mode		Debugger	Option board	Control software	
M50734SP/FP M50734SP-10	—		PC4000E	PCA4034G02 or PCA4034RG02		—

Development support systems (4) series 7450

Series 7450		Assembler	Debug system				For evaluation			
Type name	Processor mode		Control software	Base PC4000E		Base PC4600				
				Debugger	Option board	Debugger		Emulator MCU		
M37450M2-XXXSP/FP M37450M4-XXXSP/FP M37450M4TXXXSP/J M37450M8-XXXSP/FP M37450E4-XXXSP/FP M37450E4TXXXSP/J M37450E4SS/FS M37450E8-XXXSP/FP M37450E8SS/FS	Single-chip mode	SRA74	RTT74 (Note 1)	PC4000E	M37450T-OPT or M37450T-RTT	M37450RSS or M37450RFS (Note 2)	M37450PSS/PFS, M37450E4SS/FS or M37450E8SS/FS* (Note 3)			
M37450S1SP/FP M37450S2SP/FP M37450S4SP/FP	Microprocessor mode				M37450TX-OPT or M37450TX-RTT					
M37451M4-XXXSP/FP/GP M37451M8-XXXSP/FP/GP M37451MC-XXXSP/FP/GP M37451E4-XXXSP/FP/GP M37451E4SS/FS M37451E8-XXXSP/FP/GP M37451E8SS/FS M37451EC-XXXSP/FP/GP M37451ECSS/FS M37451M4DXXXSP/FP M37451M8DXXXSP/FP M37451E4DXXXSP/FP M37451E8DXXXSP/FP	Single-chip mode				PC4000E + PC4600*			—	M37451RSS or M37451RFS (Note 2)	M37451E4SS/FS*, M37451E8SS/FS* or M37451ECSS/FS** (Note 3)
M37451S1SSP/FP/GP	Microprocessor mode									

★ : New products

Note 1 : PC4600 is supported by software version up

2 : Pitch converter PCA4932 is necessary to RFS type

3 : Notes for operating temperature range about the extended operating temperature version microcomputer

Development support systems (5) series 7470

Series 7470		Assembler	Debug system			For evaluation
Type name	Processor mode		Control software	Debugger	Emulator MCU	
M37470M2-XXXSP M37470M4-XXXSP M37470M8-XXXSP M37470E4-XXXSP M37470E8-XXXSP	Single-chip mode	SRA74	RTT74 (Note 1)	PC4000E + PC4600*	M37471RSS (Note 2,3)	M37470E4-XXXSP* M37470E8-XXXSP*
M37471M2-XXXSP/FP M37471M4-XXXSP/FP M37471M8-XXXSP/FP M37471E4-XXXSP/FP M37471E8-XXXSP/FP M37471E8SS						M37471E8SS*

★ : New products

Note 1 : PC4600 is supported by software version up

2 : Pitch converter PCA4906 is necessary to M37470

3 : Pitch converter PCA4907 is necessary to QFP package type

MITSUBISHI MICROCOMPUTERS DEVELOPMENT SUPPORT SYSTEMS

Development support systems (6) series 38000

Type name	Assembler	Debug system			For evaluation
		Control software	Debugger	Emulation MCU	
M38002M2-XXXSP/FP M38002E2-XXXSP/FP M38002E2SS/FS M38002M4-XXXSP/FP M38002E4-XXXSP/FP M38002E4SS/FS M38003M6-XXXSP/FP M38003E6-XXXSP/FP M38003E6SS/FS M38004M8-XXXSP/FP M38004E8-XXXSP/FP M38004E8SS/FS M38007M4-XXXSP/FP M38007E4-XXXSP/FP M38007E4SS/FS	SRA74	RTT74 (Note 1)	PC4000E + PC4600*	M38007RSS (Note 2)	M38002E2SS/FS M38002E4SS/FS M38003E6SS/FS M38004E8SS/FS M38007E4SS/FS
M38042M3-XXXFP M38042E3-XXXFP M38042E3FS				Under development	M38042E3FS
M38062M3-XXXFP/GP M38062E3-XXXFP/GP M38062E3FS M38062M4-XXXFP/GP M38062E4-XXXFP/GP M38062E4FS M38063M6-XXXFP/GP M38063E6-XXXFP/GP M38063E6FS M38064M8-XXXFP/GP M38064E8-XXXFP/GP M38064E8FS				M38067RFS (Note 3)	M38062E3FS M38062E4FS M38063E6FS M38064E8FS
M38102M5-XXXSP/FP M38102E5-XXXSP/FP M38102E5SS M38103M6-XXXSP/FP M38103E6-XXXSP/FP M38103E6SS				M38107RSS (Note 2)	M38102E5SS M38103E6SS
M38112M4-XXXSP/FP M38112E4-XXXSP/FP M38112E4SS				M38117RSS (Note 2)	M38112E4SS
M38172M4-XXXFP M38172E4-XXXFP M38172E4FS M38173M6-XXXFP M38173E6-XXXFP M38173E6FS M38174M8-XXXFP M38174E8-XXXFP M38174E8FS				M38177RFS (Note 3)	M38172E4FS M38173E6FS M38174E8FS
M38184M8-XXXFP M38184E8-XXXFP M38184E8FS				M38187RFS** (Note 3)	M38184E8FS

★ : New products ** Under development

Note 1 : PC 4600 is supported by software version up

2 : Pitch converter M38007T-PRB is necessary to QFP package type

3 : Pitch converter PCA4932 is necessary

MITSUBISHI MICROCOMPUTERS DEVELOPMENT SUPPORT SYSTEMS

Program writing adapter for built-in PROM type microcomputers

Built-in PROM type microcomputers type name	Program writing adapter
M50746E-XXXSP	PCA4700G02
M50746ES	
M50746EFS	PCA4701G02
M50746E-XXXFP	
M50747E-XXXSP	PCA4700G02
M50747ES	
M50747E-XXXFP	PCA4701G02
M50747EFS	
M50944E-XXXSP	PCA4715
M50944ES	
M50944E-XXXFP	PCA4714
M50957E-XXXSP	PCA4703
M50957ES	
M50963E-XXXSP	PCA4700G02
M50963ES	
M50963E-XXXFP	PCA4701G02
M50963EFS	
M37102E8-XXXSP	PCA4724
M37102E8SS	
M37102E8-XXXFP	PCA4725
M37102E8FS	
M37120E6-XXXFP	PCA4716(Note 1)
M37201E6-XXXSP	PCA4723
M37201E6SS	
M37202E3-XXXSP	PCA4726*
M37202E3SS	
M37204E8-XXXSP	
M37204E8SS	
M37250E6-XXXSP	
M37250E6SS	
M37260E6-XXXSP	PCA4736*
M37260E6SS	
M37260E6-XXXFP	PCA4737*
M37260E6FS	
M37410E6HXXXFP	PCA4705
M37410E6HFS	PCA4706
M37412E5-XXXFP	PCA4720
M37413E6HXXXFP	PCA4728
M37413E6HFS	PCA4729
M37414E5-XXXFP	PCA4720
M37420E6-XXXSP	PCA4727
M37420E6SS	
M37424E8-XXXSP	PCA4721
M37424E8SS	
M37524E8-XXXSP	
M37524E8SS	PCA4710
M37450E4-XXXSP	
M37450E4SS	
M37450E8-XXXSP	
M37450E8SS	
M37451E4-XXXSP	
M37451E4SS	
M37451E8-XXXSP	
M37451E8SS	
M37451EC-XXXSP	

Program writing adapter for built-in PROM type microcomputers (continued)

Built-in PROM type microcomputers type name	Program writing adapter
M37451ECSS	PCA4710
M37450E4TXXXSP	
M37450E4TXXXJ	PCA4712(Note 1)
M37450E4-XXXFP	PCA4711
M37450E4FS	
M37450E8-XXXFP	
M37450E8FS	PCA4719
M37451E4FS	
M37451E8FS	
M37451ECFS	
M37451E4-XXXFP	PCA4751*
M37451E8-XXXFP	
M37451EC-XXXFP	
M37451E4-XXXGP	PCA4752*
M37451E8-XXXGP	
M37451EC-XXXGP	PCA4710
M37451E4DXXXSP	
M37451E8DXXXSP	
M37451E4DXXXFP	PCA4751*
M37451E8DXXXFP	
M37460E8-XXXFP	PCA4713(Note 1)
M37470E4-XXXSP	PCA4730
M37470E8-XXXSP	
M37471E4-XXXSP	
M37471E8-XXXSP	
M37471E8SS	
M37471E4-XXXFP	
M37471E8-XXXFP	PCA4731
M38002E2-XXXSP	Under development
M38002E2-XXXFP	
M38002E2SS	
M38002E2FS	PCA4738-64
M38002E4-XXXSP	
M38002E4-XXXFP	PCA4738F-64
M38002E4SS	PCA4738S-64
M38002E4FS	PCA4738L-64**
M38003E6-XXXSP	Under development
M38003E6-XXXFP	
M38003E6SS	
M38003E6FS	
M38004E8-XXXSP	
M38004E8-XXXFP	
M38004E8SS	
M38004E8FS	
M38007E4-XXXSP	
M38007E4-XXXFP	
M38007E4SS	
M38007E4FS	
M38042E3-XXXFP	
M38042E3FS	
M38062E3-XXXFP	
M38062E3-XXXGP	
M38062E3FS	

* : New product ** : Under development
Note 1 : Be necessary to order producing this board

MITSUBISHI MICROCOMPUTERS DEVELOPMENT SUPPORT SYSTEMS

Program writing adapter for built-in PROM type microcomputers (continued)

Built-in PROM type microcomputers type name	Program writing adapter
M38062E4-XXXFP	Under development
M38062E4-XXXGP	
M38062E4FS	
M38063E6-XXXFP	PCA4738F-80
M38063E6-XXXGP	PCA4738G-80
M38063E6FS	PCA4738L-80
M38064E8-XXXFP	Under development
M38064E8-XXXGP	
M38064E8FS	
M38102E5-XXXSP	PCA4738S-64
M38102E5-XXXFP	PCA4738F-64
M38102E5SS	PCA4738S-64
M38103E6-XXXSP	Under development
M38103E6-XXXFP	
M38103E6SS	
M38112E4-XXXSP	PCA4738S-64
M38112E4-XXXFP	PCA4738F-64
M38112E4SS	PCA4738S-64
M38172E4-XXXFP	Under development
M38172E4FS	
M38173E6-XXXFP	
M38173E6FS	
M38174E8-XXXFP	
M38174E8FS	
M38184E8-XXXFP	PCA4738F-100*
M38184E8FS	Under development

* : New product ** : Under development

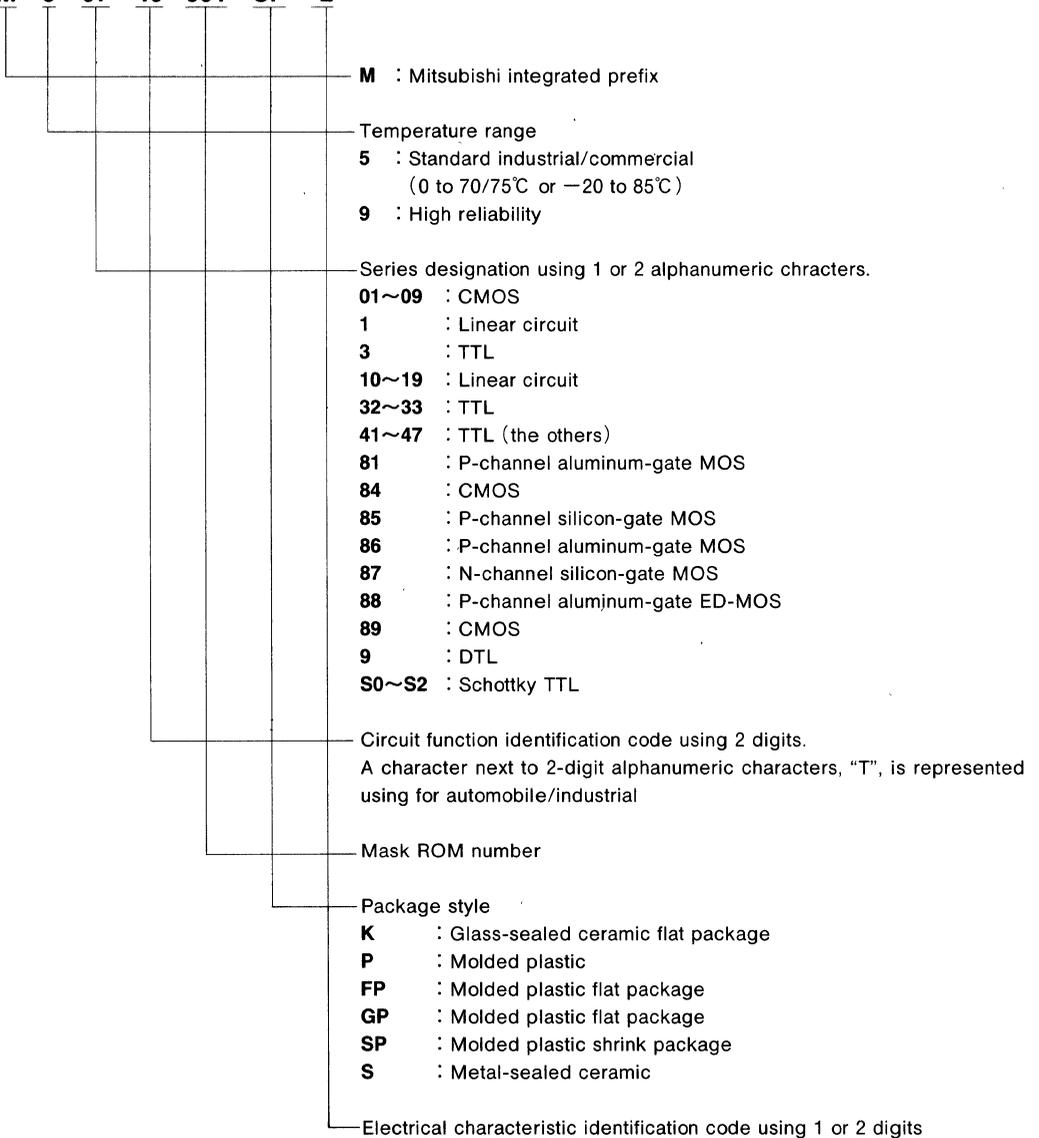
MITSUBISHI MICROCOMPUTERS ORDERING INFORMATION

FUNCTION CODE

Mitsubishi integrated circuits may be ordered using the following simplified alphanumeric type-codes which define the function of the IC/LSIs and the package style.

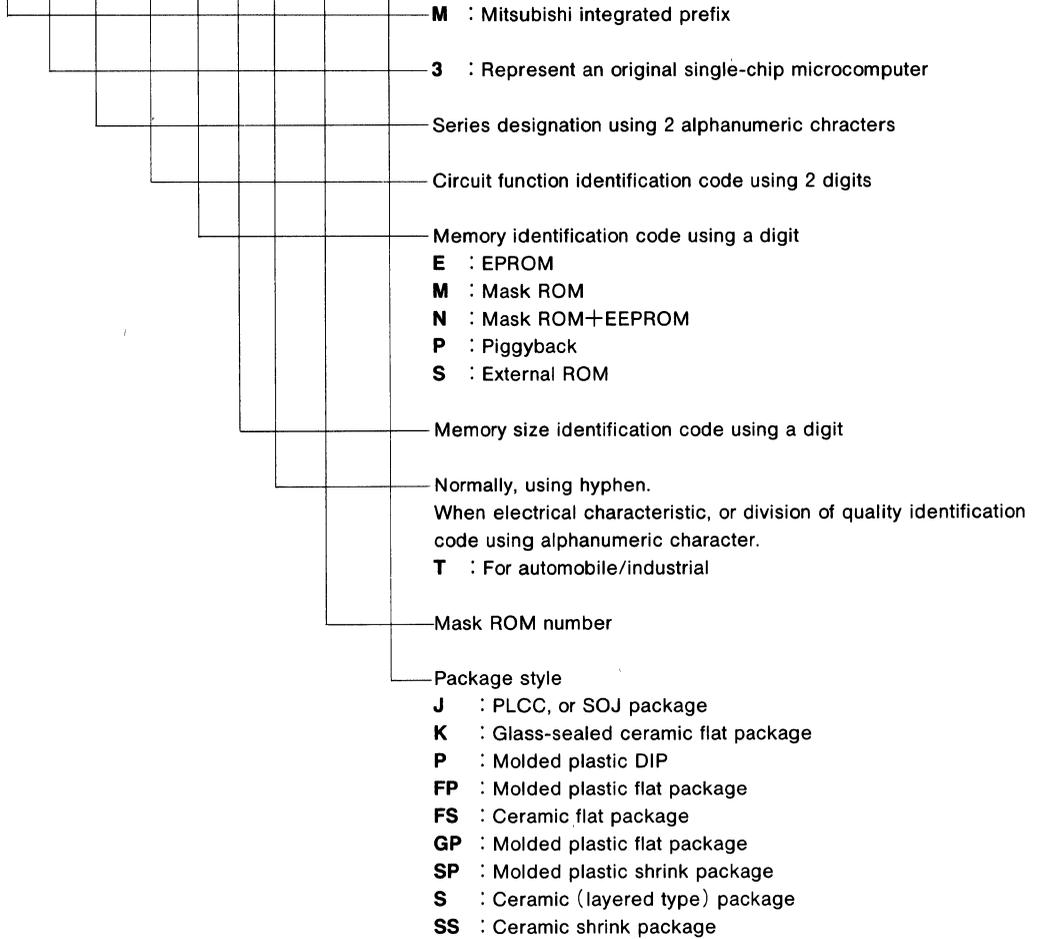
1. Mitsubishi Original Products

Example 1. **M 5 07 40 - 001 SP -2**



MITSUBISHI MICROCOMPUTERS ORDERING INFORMATION

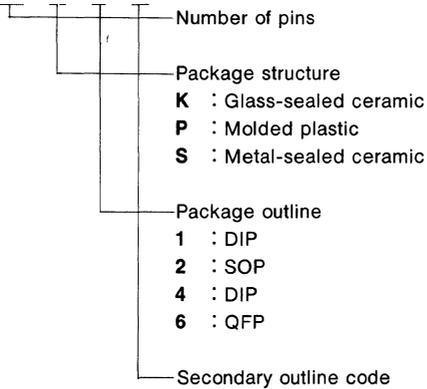
Example 2. **M 3 74 50 E 4 - 001 SP**



2. PACKAGE CODE

Package style may be specified by using the following simplified alphanumeric code.

Example : **42 P 4 B**



Number of pins

Package structure

K : Glass-sealed ceramic

P : Molded plastic

S : Metal-sealed ceramic

Package outline

1 : DIP

2 : SOP

4 : DIP

6 : QFP

Secondary outline code

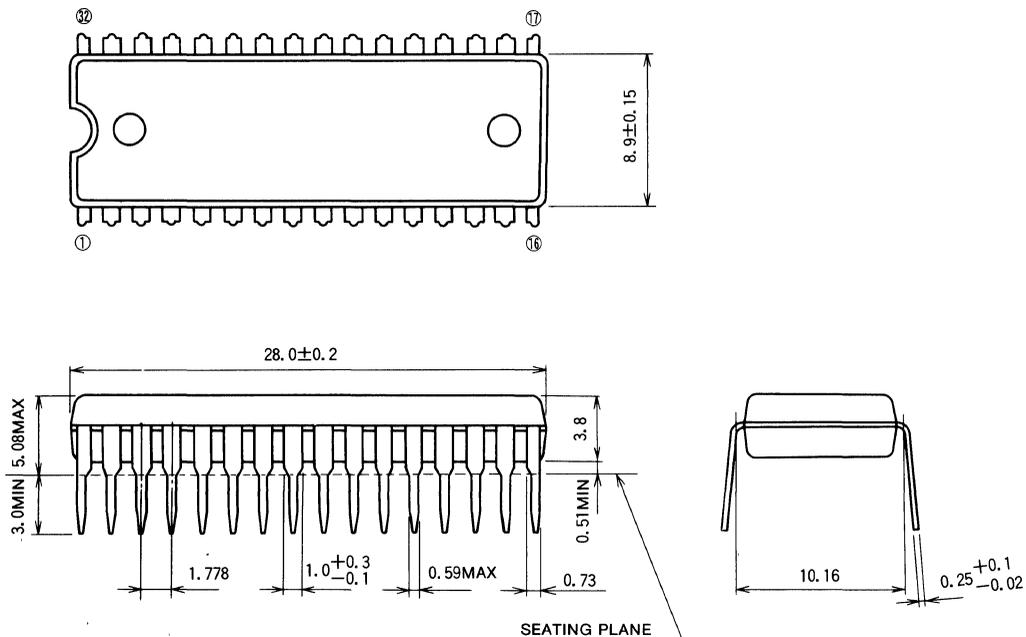
Special-purpose secondary codes describing outline are included as necessary. For details, contact your sales representative.

MITSUBISHI MICROCOMPUTERS PACKAGE OUTLINES

32P4B

32pin molded plastic DIP

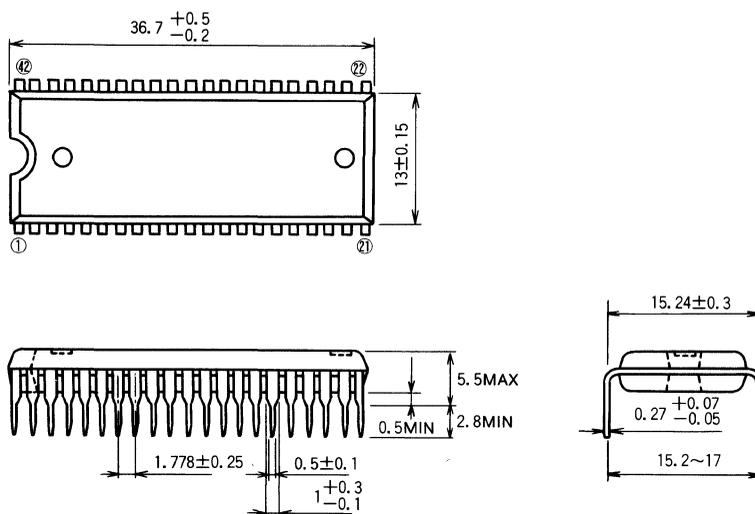
Dimension in mm



42P4B

42pin molded plastic DIP

Dimension in mm

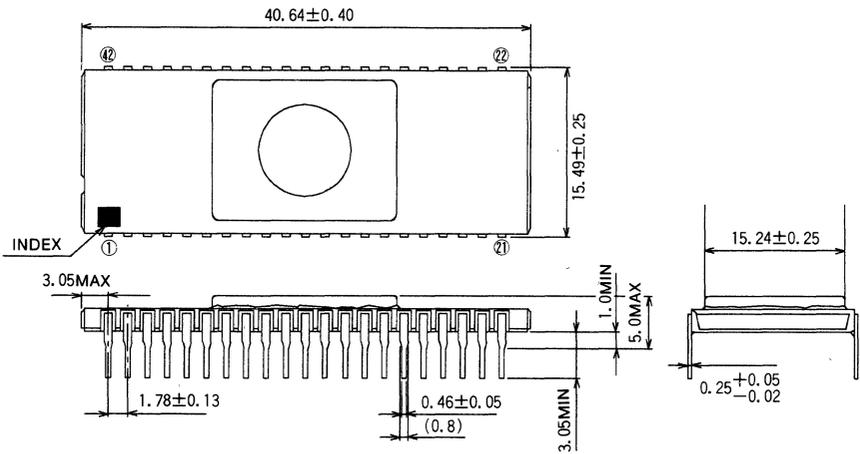


MITSUBISHI MICROCOMPUTERS PACKAGE OUTLINES

42S1B

42pin ceramic DIP

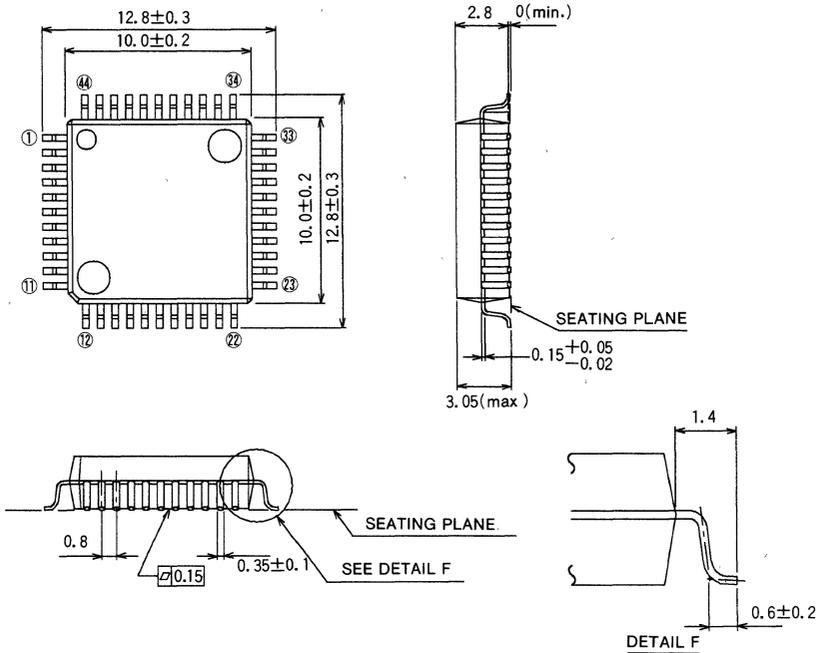
Dimension in mm

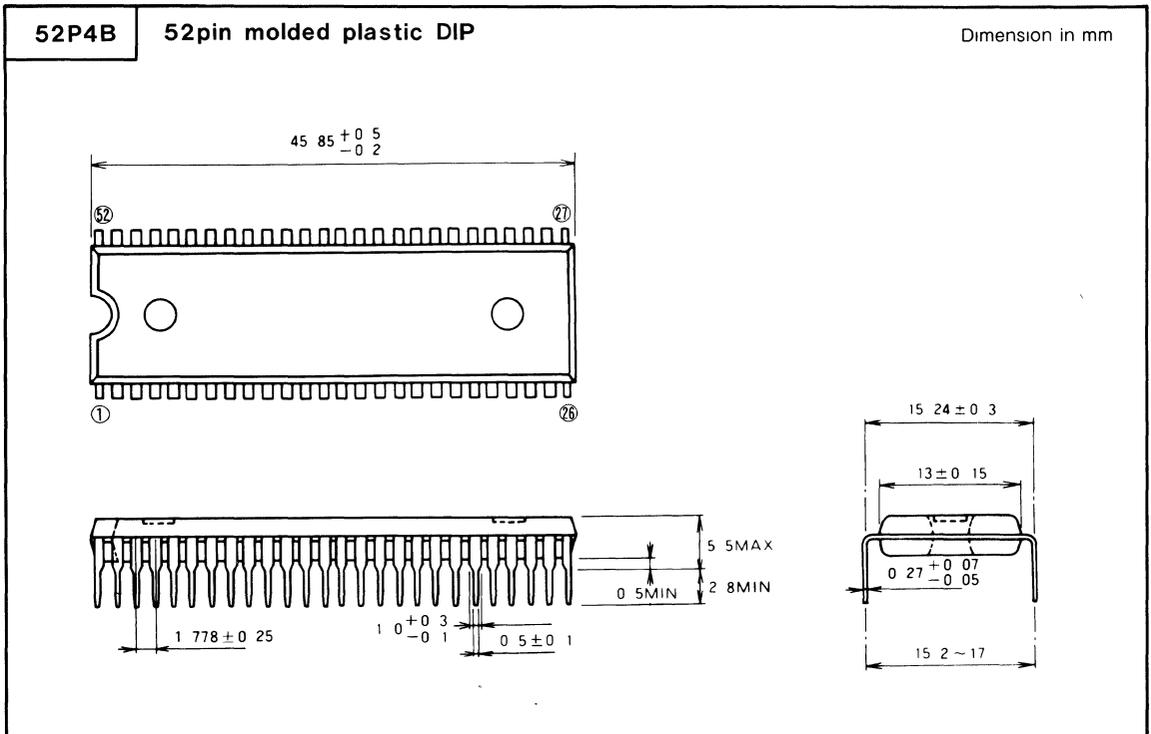
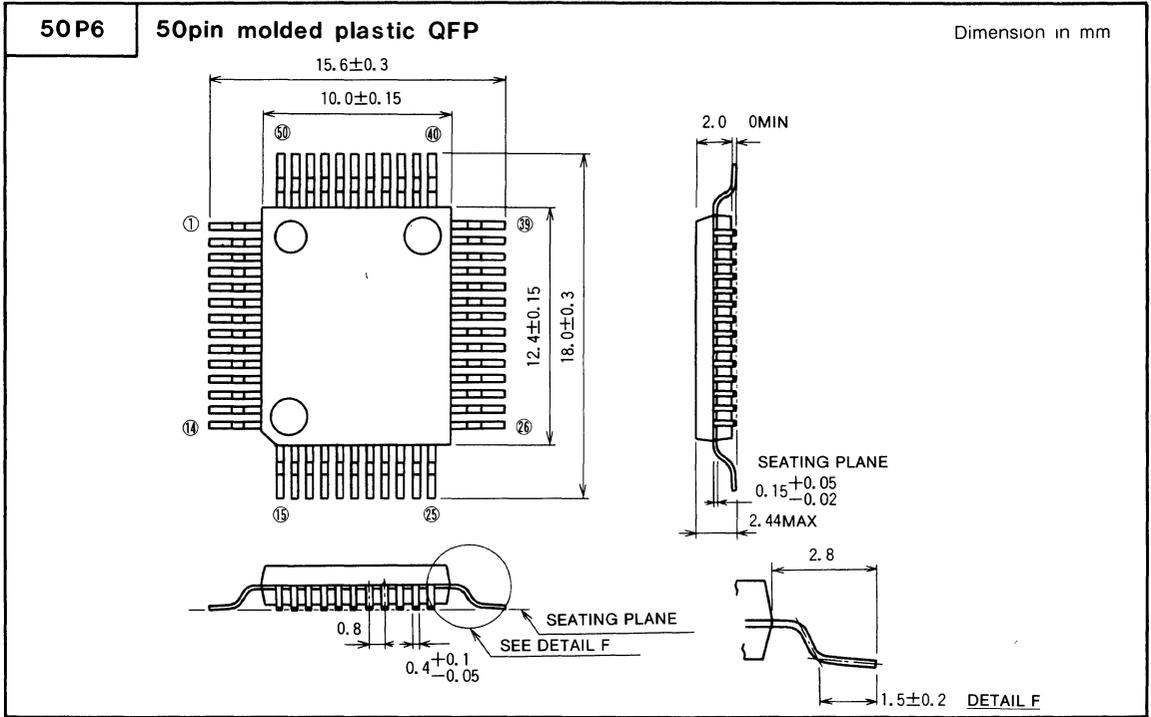


44P6N

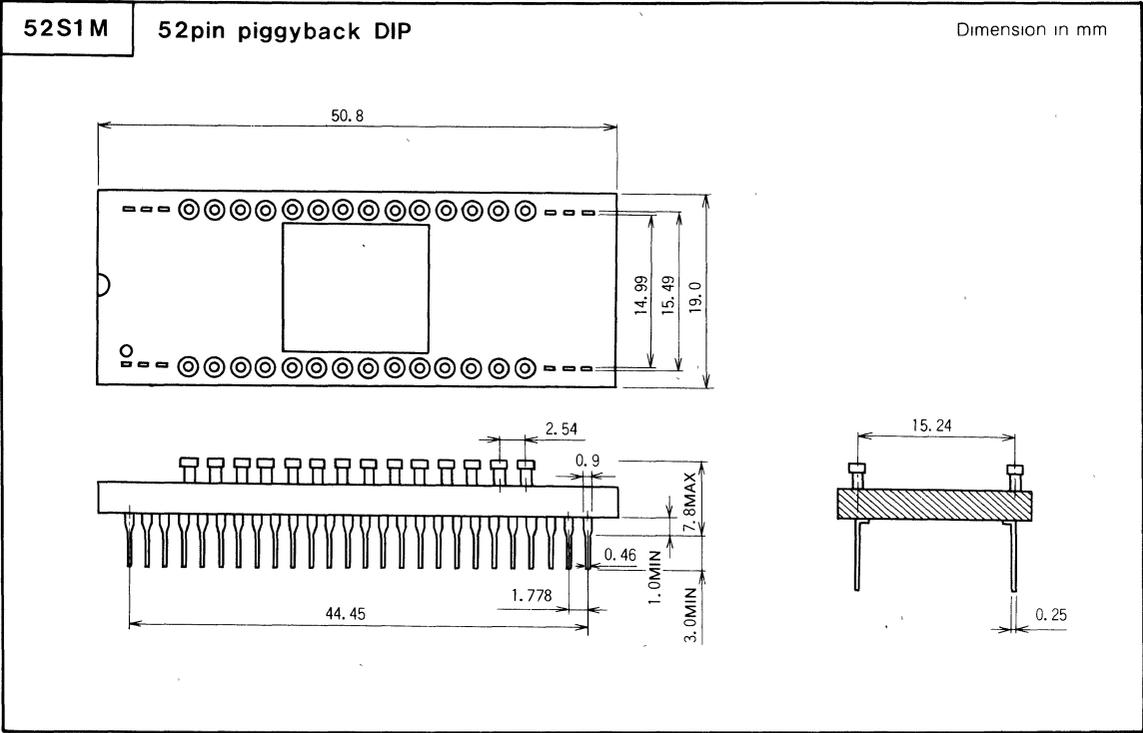
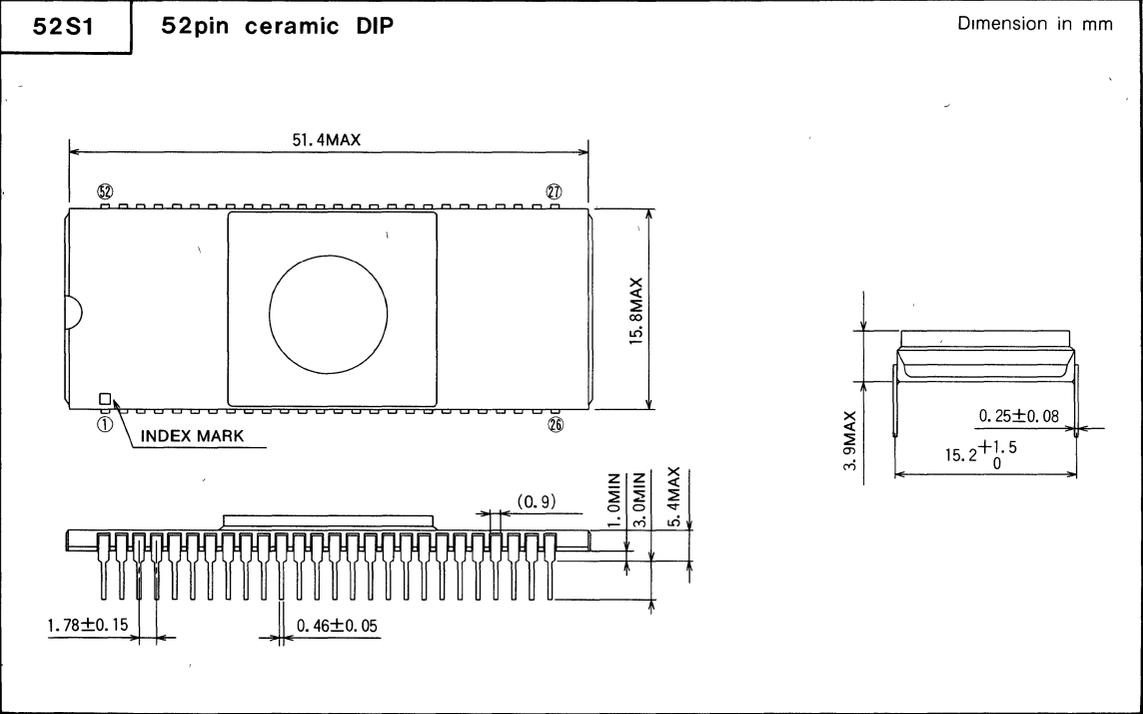
Plastic 44pin QFP

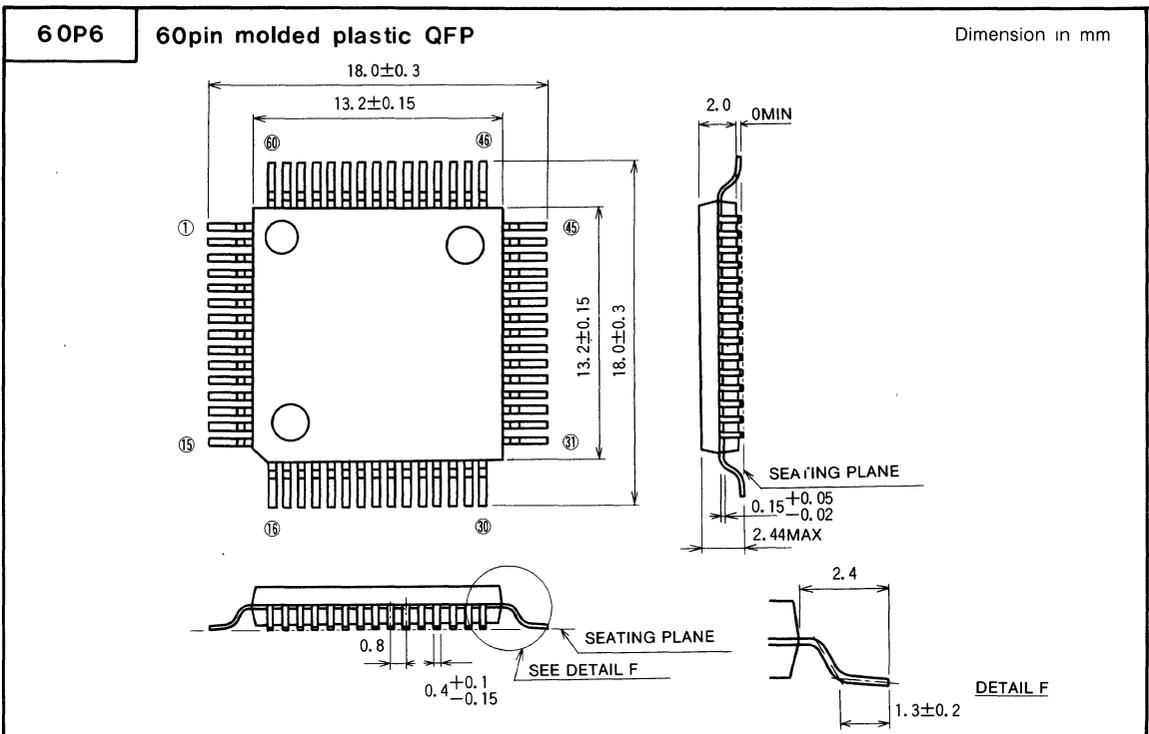
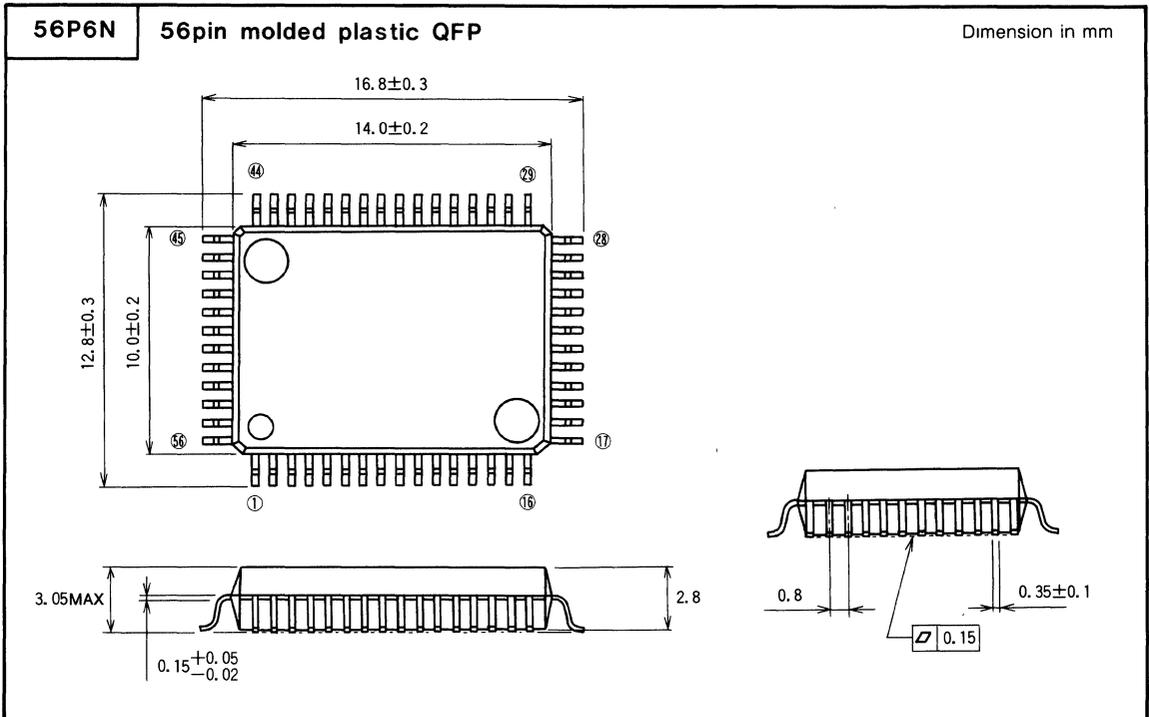
Dimension in mm

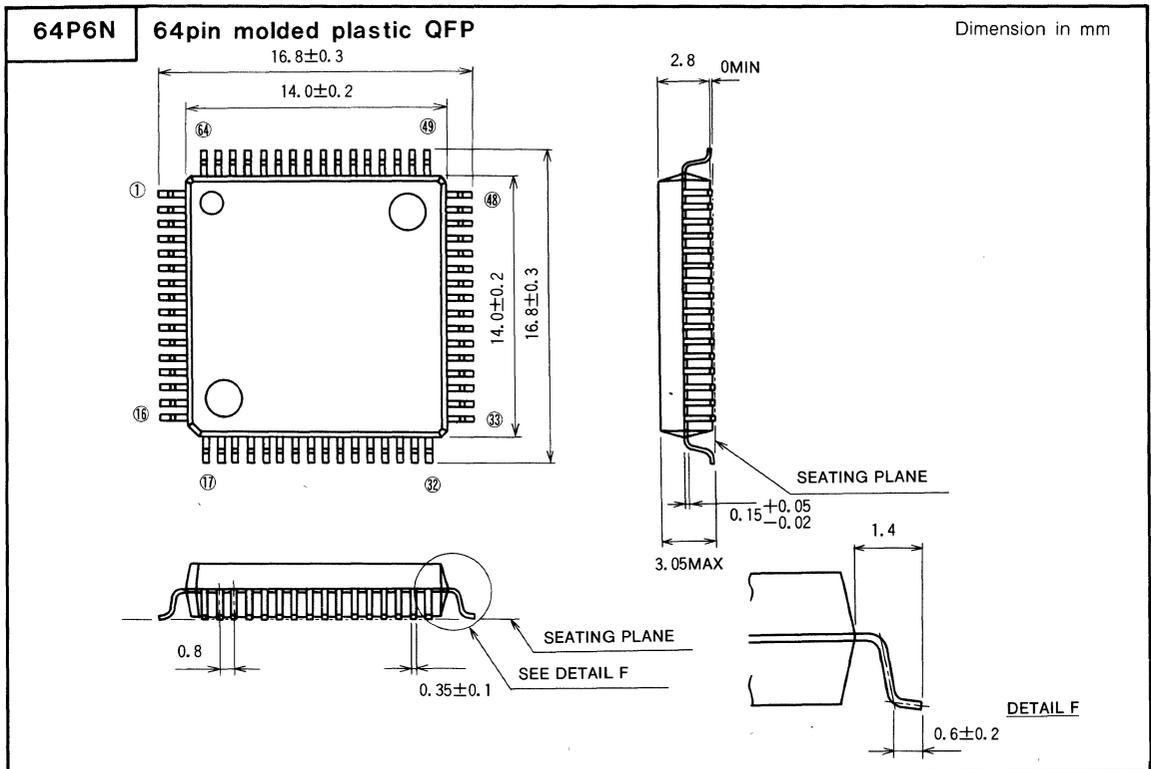
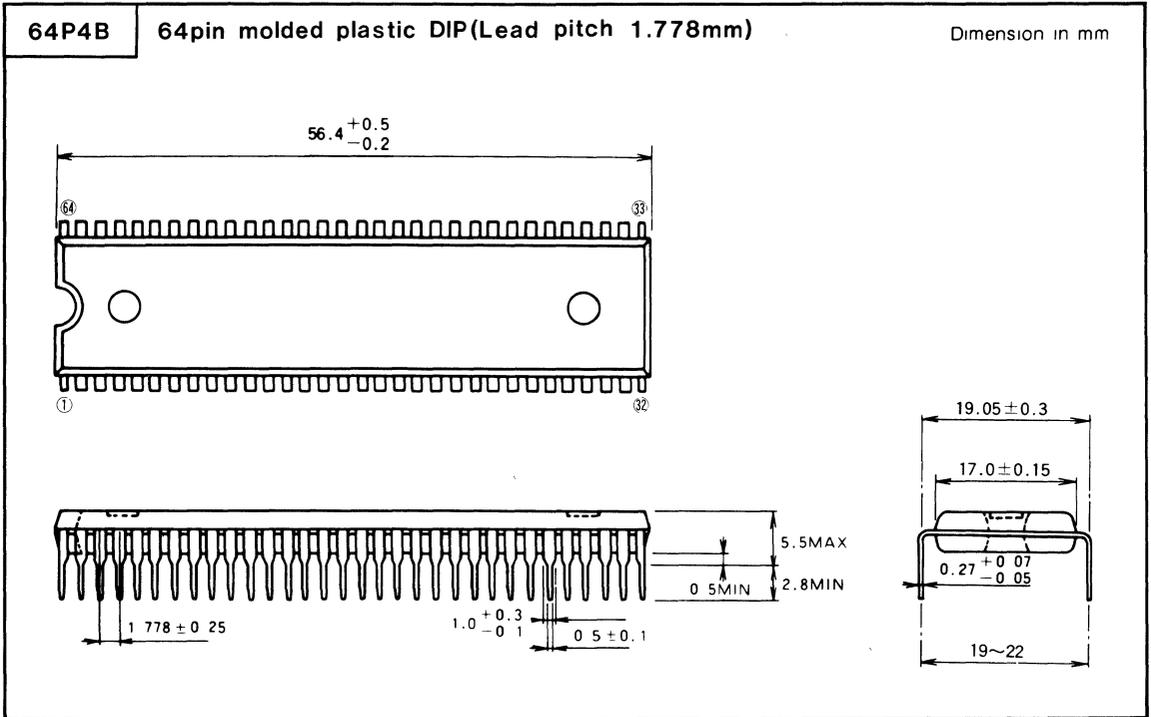


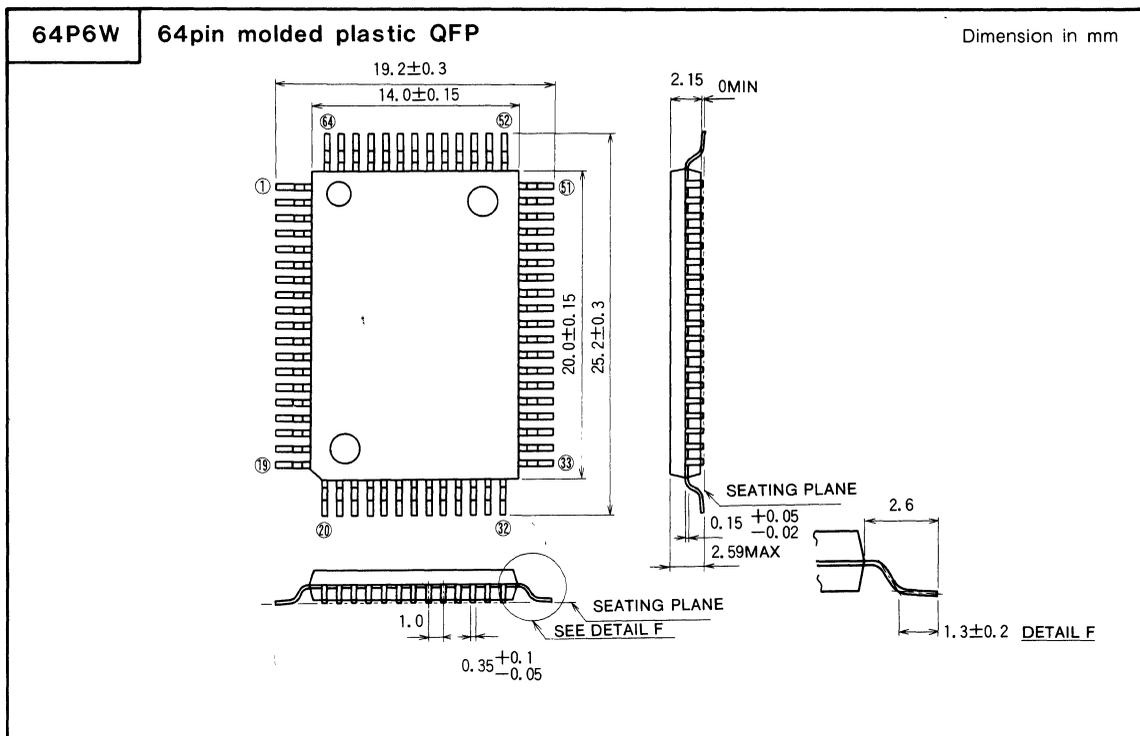
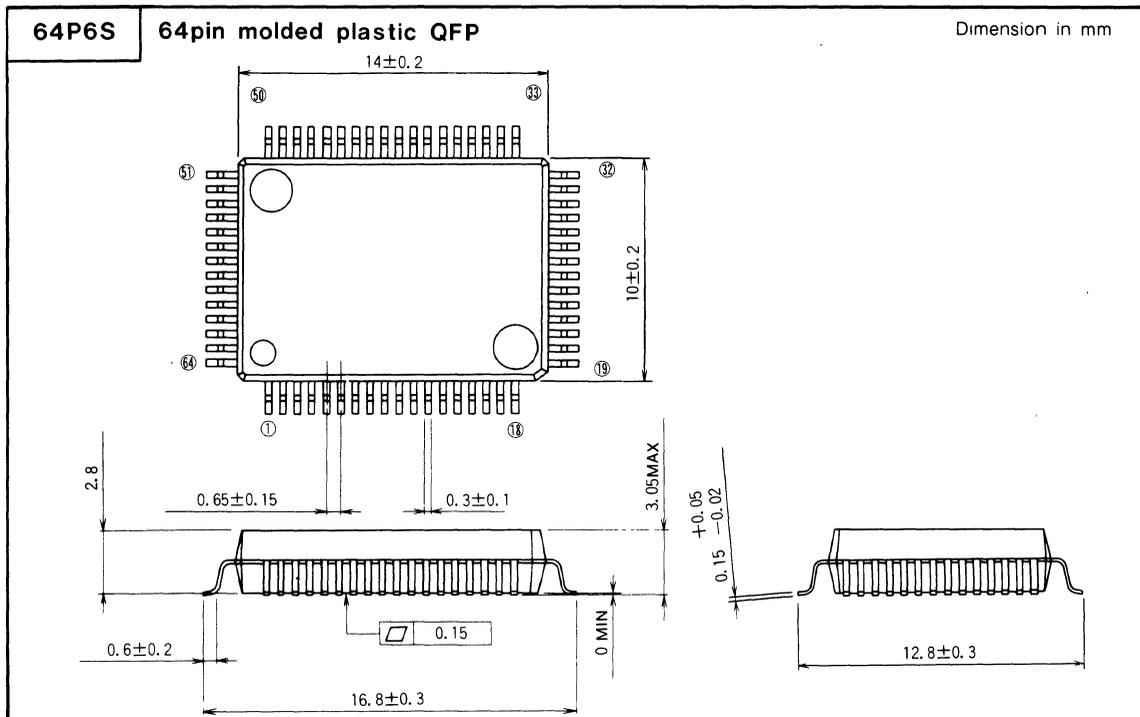


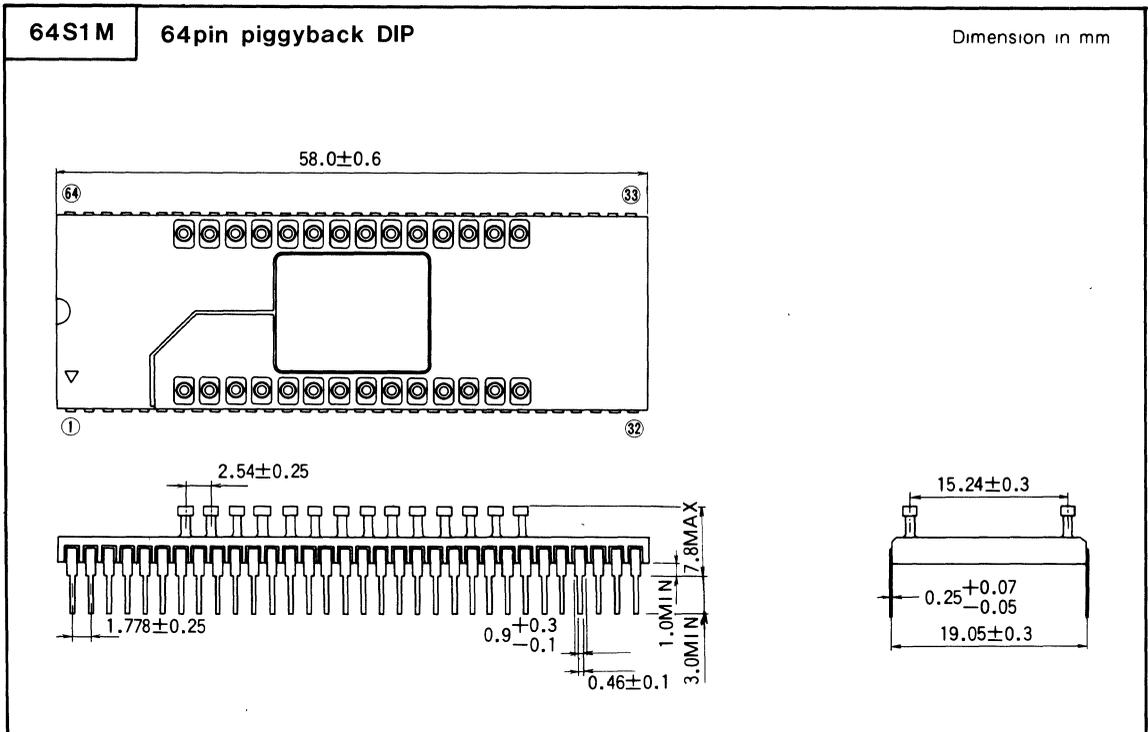
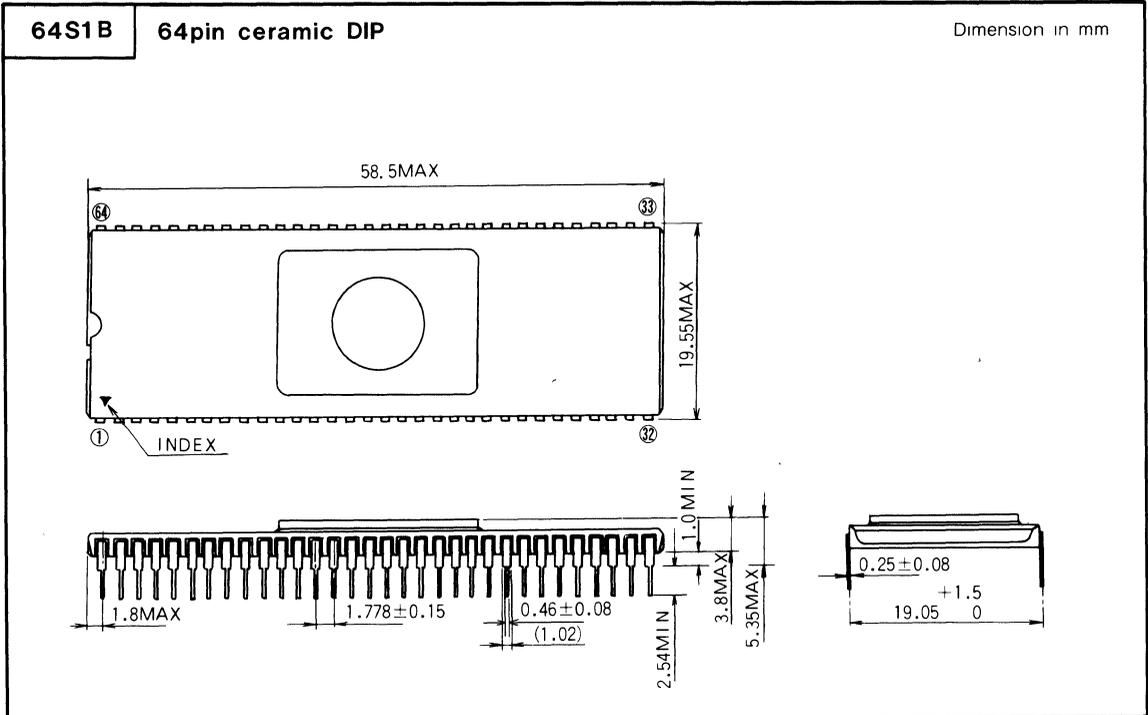
**MITSUBISHI MICROCOMPUTERS
PACKAGE OUTLINES**







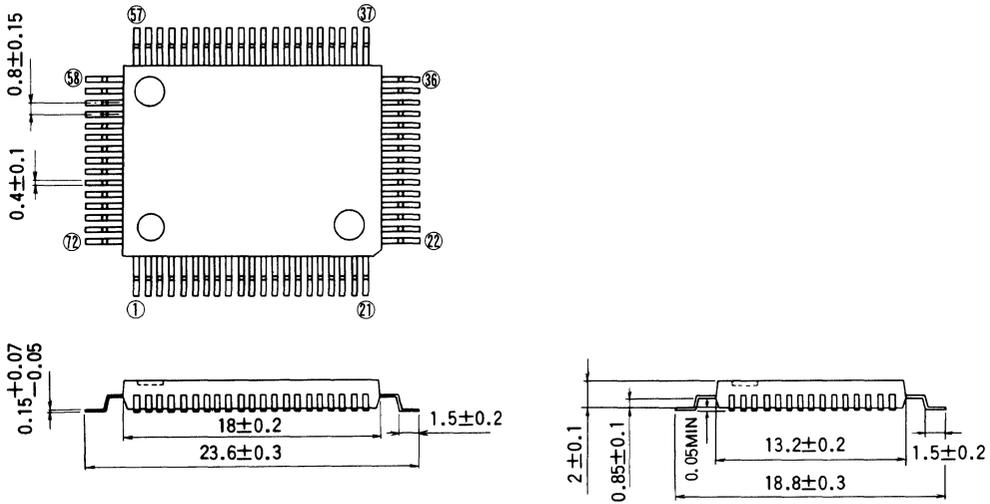




72P6

72pin molded plastic QFP

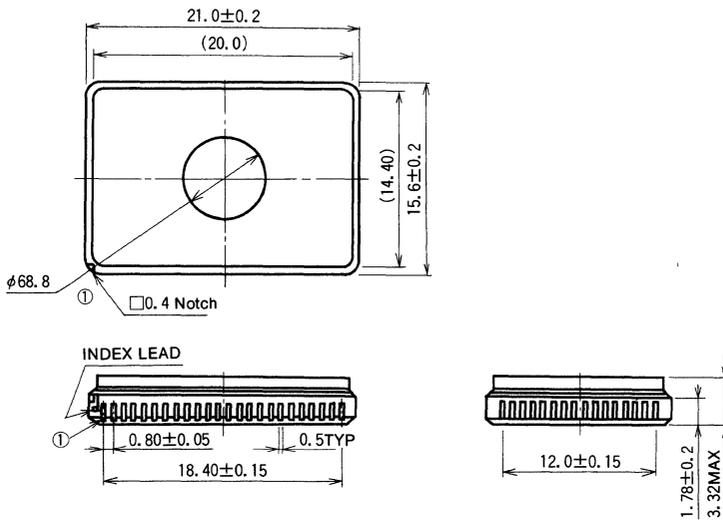
Dimension in mm



80D0

80pin molded ceramic LCC

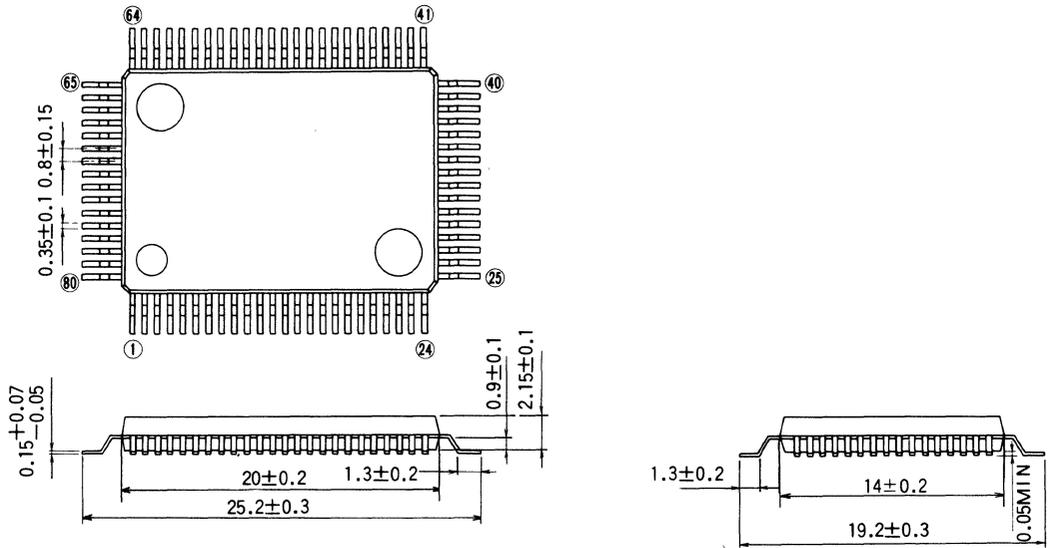
Dimension in mm



80P6

80pin molded plastic QFP

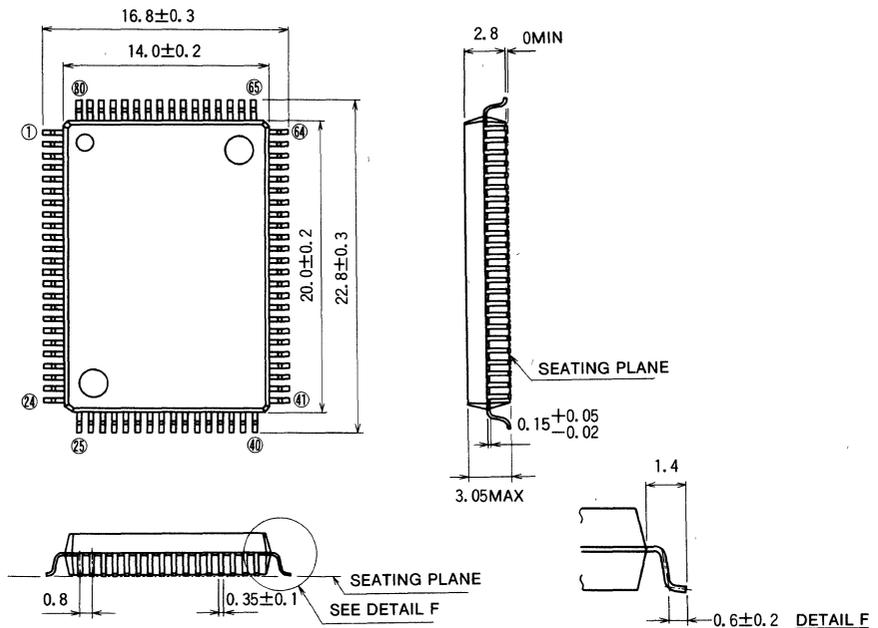
Dimension in mm

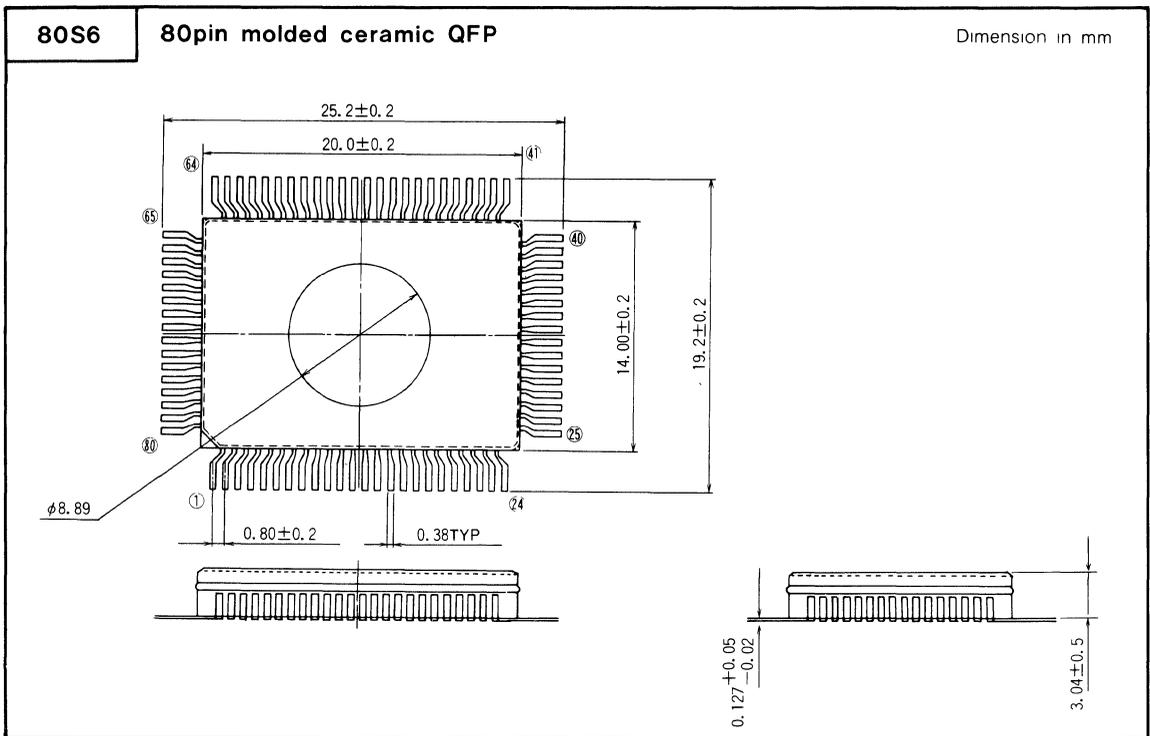
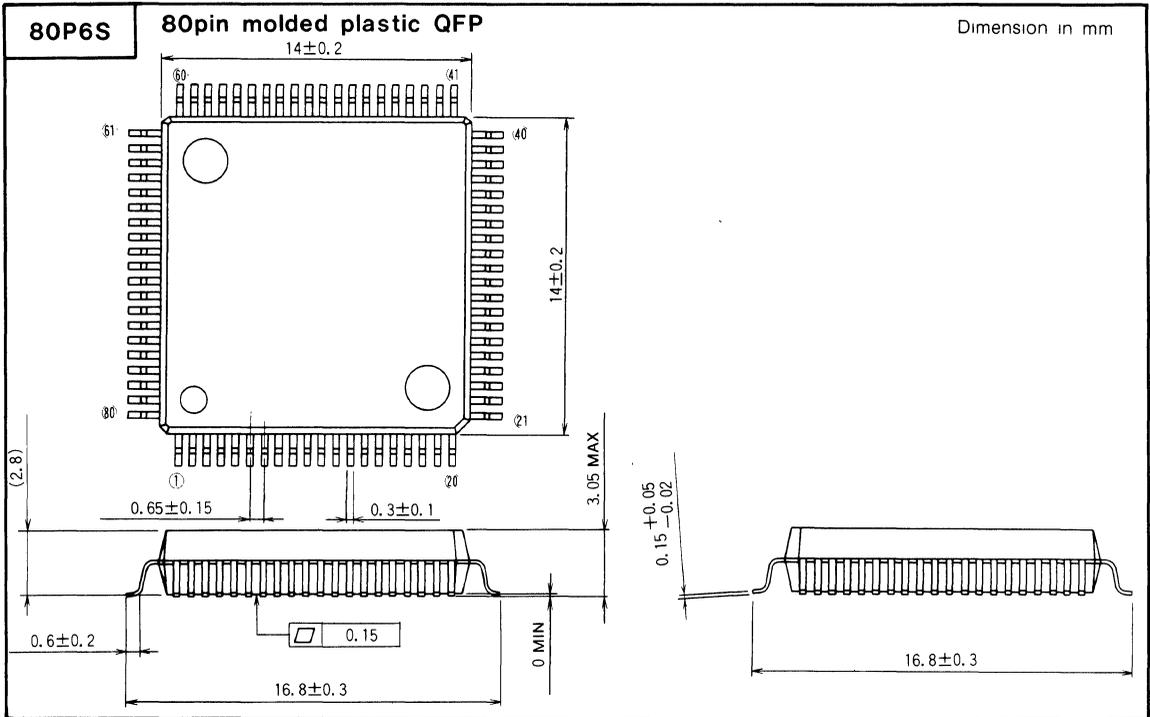


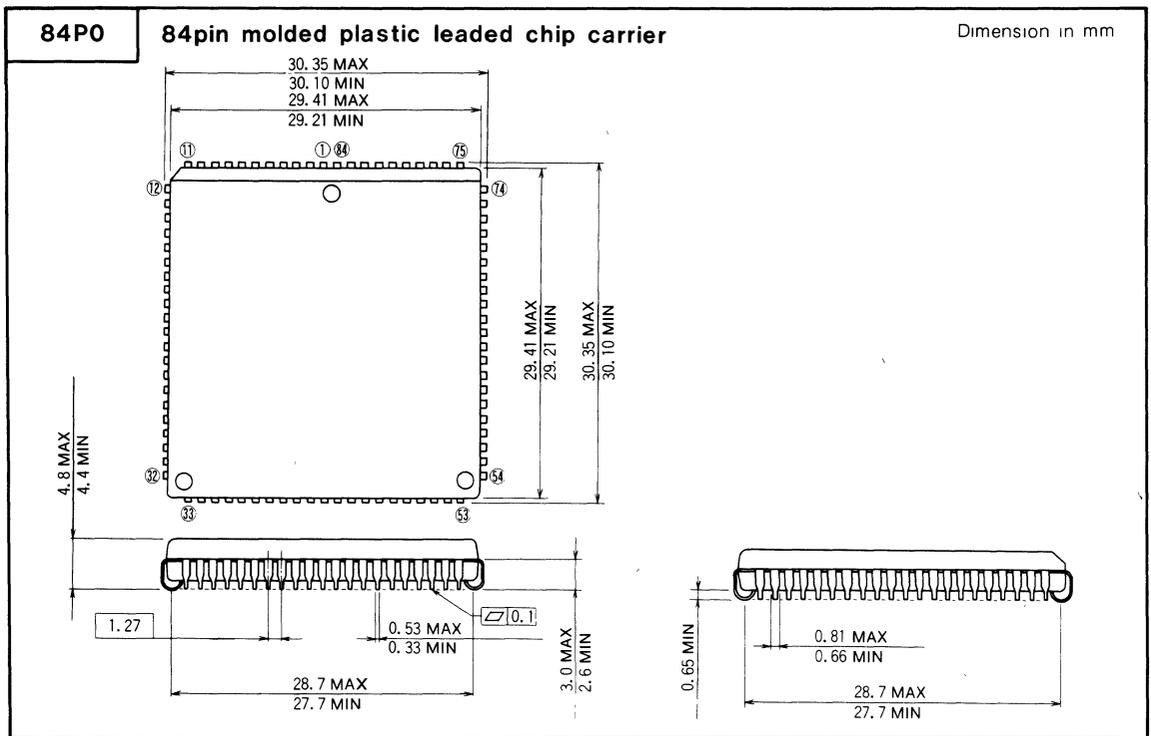
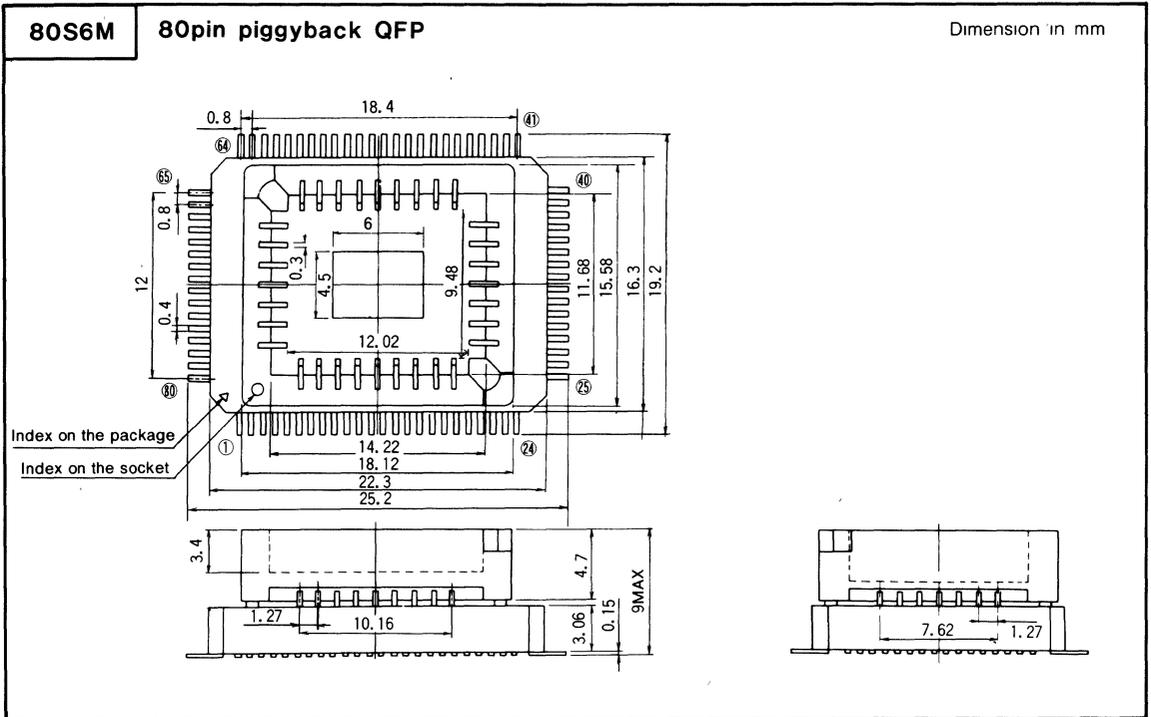
80P6N

80pin molded plastic QFP

Dimension in mm



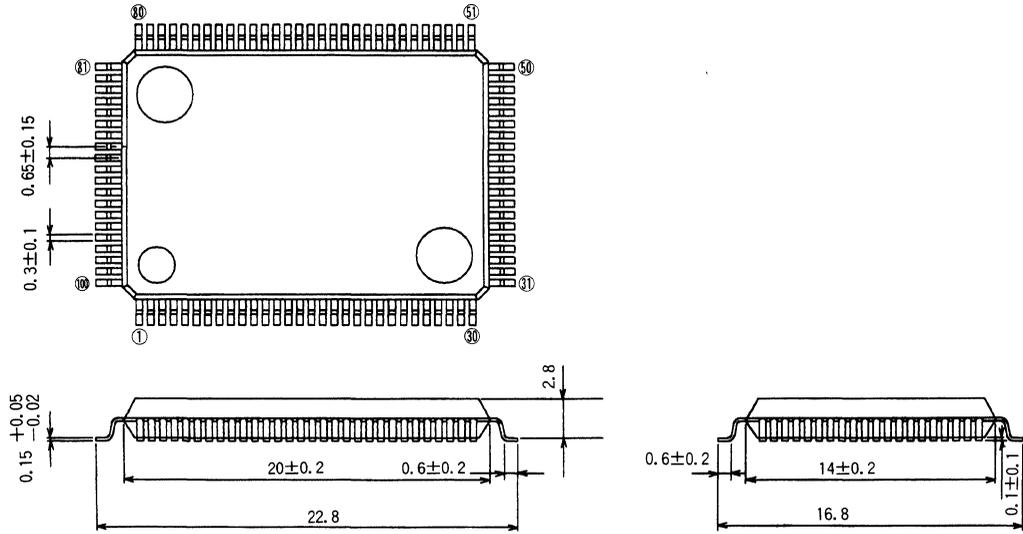




100P6S

Plastic 100pin QFP

Dimension in mm



LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

1. INTRODUCTION

A system of letter symbols to be used to represent the dynamic parameters of intergrated circuit memories and other sequential circuits especially for single-chip microcomputers, microprocessors and LSIs for peripheral circuits has been discussed internationally in the TC47 of the International Electrotechnical Committee (IEC). Finally the IEC has decided on the meeting of TC47 in February 1980 that this system of letter symbols will be a Central Office document and circulated to all countries to vote which means this system of letter symbols will be a international standard.

The system is applied in this LSI data book for the new products only. Future editions of this data book will be applied this system. The IEC document which describes "Letter symbols for dynamic parameters of sequential integrated circuits, including memories" is introduced below. In this data book, the dynamic parameters in the IEC document are applied to timing requirements and switching characteristics.

2. LETTER SYMBOLS

The system of letter symbols outlined in this document enables symbols to be generated for the dynamic parameters of complex sequential circuits, including memories, and also allows these symbols to be abbreviated to simple mnemonic symbols when no ambiguity is likely to arise.

2.1. General Form

The dynamic parameters are represented by the general symbol of the form -

$$t_{A(BC-DC)F} \dots\dots\dots (1)$$

where :

Subscript A indicates the type of dynamic parameter being represented, for example; cycle time, setup time, enable time, etc.

Subscript B indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur first, that is, at the beginning of the time interval. If this event actually occurs last, that is, at the end of the time interval, the value of the time interval is negative.

Subscript C indicates the direction of the transition and/or the final state or level of the signal represented by B. When two letters are used, the initial state or level is also indicated.

Subscript D indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur last, that is, at the end of the time interval. If this event actually occurs first, that is, at the beginning of the time interval, the value of the time interval is negative.

Subscript E indicates the direction of the transition and/or the final state or level of the signal represented by D. When two letters are used, the initial state or level is also indicated.

Subscript F indicates additional information such as mode of operation, test conditions, etc.

- Note: 1 Subscripts A to F may each consists of one or more letters
 2 Subscripts D and E are not used for transition times
 3 The "-" in the symbol (1) above is used to indicate "to", hence the symbol represents the time interval from signal event B occurring to signal event D occurring, and it is important to note that this convention is used for all dynamic parameters including hold times. Where no misunderstanding can occur the hyphen may be omitted

2.2. Abbreviated Form

The general symbol given above may be abbreviated when no misunderstanding is likely to arise. For example to :

$$t_{A(B-D)}$$

or $t_{A(B)}$

or $t_{A(D)}$ — often used for hold times

or t_{AF} — no brackets are used in this case

or t_A

or t_{BC-DE} — often used for unclassified time intervals

2.3. Allocation of Subscripts

In allocating letter symbols for the subscripts, the most commonly used subscripts are given single letters where practicable and those less commonly used are designated by up to three letters. As far as possible, some form of mnemonic representation is used. Longer letter symbols may be used for specialised signals or terminals if this aids understanding.

3. SUBSCRIPT A (For Type of Dynamic Parameter)

The subscript A represents the type of dynamic parameter to be designated by the symbol and, for memories, the parameters may be divided into two classes :

- a) those that are timing requirements for the memory and

MITSUBISHI MICROCOMPUTERS

LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

b) those that are characteristics of the memory. The letter symbols so far proposed for memory circuits are listed in sub-clauses 3.1 and 3.2 below. All subscripts A should be in lower-case.

3.1. Timing Requirements

The letter symbols for the timing requirements of semiconductor memories are as follows :

Term	Subscript
Cycle time	c
Time interval between two signal events	d
Fall time	f
Hold time	h
Precharging time	pc
Rise time	r
Recovery time	rec
Refresh time interval	rf
Setup time	su
Transition time	t
Pulse duration (width)	w

3.2. Characteristics

The letter symbols for the dynamic characteristics of semiconductor memories are as follows :

Characteristic	Subscript
Access time	a
Disable time	dis
Enable time	en
Propagation time	P
Recovery time	rec
Transition time	T
Valid time	v

Note: Recovery time for use as a characteristic is limited to sense recovery time.

4. SUBSCRIPTS B AND D (For Signal Name or Terminal Name)

The letter symbols for the signal name or the name of the terminal are as given below. All subscripts B and D should be in upper-case.

Signal or terminal	Subscript
Address	A
Clock	C
Column address	CA
Column address strobe	CAS
Data input	D
Data input/output	DQ
Chip enable	E

Erase	ER
Output enable	G
Program	PR
Data output	Q
Read	R
Row address	RA
Row address strobe	RAS
Refresh	RF
Read/Write	RW
Chip select	S
Write (write enable)	W

Note 1 In the letter symbols for time intervals, bars over the subscripts, for example CAS, should not be used.

- It should be noted, when further letter symbols are chosen, that the sub-script should not end with H, K, V, X, or Z (See clause 5)
- If the same terminal, or signal, can be used for two functions (for example Data input/output, Read/Write) the waveform should be labelled with the dual function, if appropriate, but the symbols for the dynamic parameters should include only that part of the subscript relevant to the parameter.

5. SUBSCRIPTS C AND E (For Transition of Signal)

The following symbols are used to represent the level or state of a signal :

Transition of signal	Subscript
High logic level	H
Low logic level	L
Valid steady-state level (either low or high)	V
Unknown, changing, or 'don't care' level	X
High-impedance state of three-state output	Z

The direction of transition is expressed by two letters, the direction being from the state represented by the first letter to that represented by the second letter, with the letters being as given above.

When no misunderstanding can occur, the first letter may be omitted to give an abbreviated symbol for subscripts C and E as indicated below.

All subscripts C and E should be in upper-case.

Examples	Subscript	
	Full	Abbreviated
Transition from high level to low level	HL	L
Transition from low level to high level	LH	H
Transition from unknown or changing state to valid state	XV	V
Transition from valid state to unknown or changing state	VX	X
Transition from high-impedance state to valid state	ZV	V

Note: Since subscripts C and E may be abbreviated, and since subscripts B and D may contain an indeterminate number of letters, it is necessary to put the restriction on the subscripts B and D that they should not end with H, L, V, X, or Z, so as to avoid possible confusion.

LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

6. SUBSCRIPT F (For Additional Information)

If necessary, subscript F is used to represent any additional qualification of the parameter such as mode of operation, test conditions, etc. The letter symbols for subscript F are given below.

Subscript F should be in upper-case.

Modes of operation	Subscript
Power-down	PD
Page-mode read	PGR
Page-mode write	PGW
Read	R
Refresh	RF
Read-modify-write	RMW
Read-write	RW
Write	W

FOR DIGITAL INTEGRATED CIRCUITS

New symbol	Former symbol	Parameter—definition
C_i		Input capacitance
C_o		Output capacitance
$C_{i/o}$		Input/output terminal capacitance
$C_i(\phi)$		Input capacitance of clock input
f		Frequency
$f(\phi)$		Clock frequency
I		Current—the current into an integrated circuit terminal is defined as a positive value and the current out of a terminal is defined as a negative value
I_{BB}		Supply current from V_{BB}
$I_{BB(AV)}$		Average supply current from V_{BB}
I_{CC}		Supply current from V_{CC}
$I_{CC(AV)}$		Average supply current from V_{CC}
$I_{CC(PD)}$		Power-down supply current from V_{CC}
I_{DD}		Supply current from V_{DD}
$I_{DD(AV)}$		Average supply current from V_{DD}
I_{GG}		Supply current from V_{GG}
$I_{GG(AV)}$		Average supply current from V_{GG}
I_i		Input current
I_{IH}		High-level input current—the value of the input current when V_{OH} is applied to the input considered
I_{IL}		Low-level input current—the value of the input current when V_{OL} is applied to the input considered
I_{LOAD}		Built-in resistor current
I_{PEAK}		Peak current
I_{OH}		High-level output current—the value of the output current when V_{OH} is applied to the output considered
I_{OL}		Low-level output current—the value of the output current when V_{OL} is applied to the output considered
I_{OZ}		Off-state (high-impedance state) output current—the current into an output having a three-state capability with input condition so applied that it will establish according to the product specification, the off (high-impedance) state at the output
I_{OZH}		Off state (high-impedance state) output current, with high-level voltage applied to the output
I_{OZL}		Off-state (high-impedance state) output current, with low level voltage applied to the output
I_{OS}		Short-circuit output current
I_{SS}		Supply current from V_{SS}
P_d		Power dissipation
N_{EW}		Number of erase/write cycles
N_{RA}		Number of read access unrefreshed
R_i		Input resistance
R_L		External load resistance
R_{OFF}		Off-state output resistance
R_{ON}		On-state output resistance
t_a		Access time—the time interval between the application of a specified input pulse during a read cycle and the availability of valid data signal at an output
$t_a(A)$	$t_a(AD)$	Address access time—the time interval between the application of an address input pulse and the availability of valid data signals at an output
$t_a(CAS)$		Column address strobe access time
$t_a(E)$	$t_a(OE)$	Chip enable access time
$t_a(G)$	$t_a(OE)$	Output enable access time
$t_a(PR)$		Data access time after program
$t_a(RAS)$		Row address strobe access time
$t_a(S)$	$t_a(OS)$	Chip select access time
t_c		Cycle time
t_{CR}	$t_c(RD)$	Read cycle time—the time interval between the start of a read cycle and the start of the next cycle
t_{CRF}	$t_c(REF)$	Refresh cycle time—the time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level
t_{CPG}	$t_c(PG)$	Page-mode cycle time

New symbol	Former symbol	Parameter—definition
t_{CRMW}	$t_C(RMR)$	Read-modify-write cycle time—the time interval between the start of a cycle in which the memory is read and new data is entered, and the start of the next cycle
t_{CW}	$t_C(WR)$	Write cycle time—the time interval between the start of a write cycle and the start of the next cycle
t_d		Delay time—the time between the specified reference points on two pulses
$t_d(\phi)$		Delay time between clock pulses—e.g., symbology, delay time, clock 1 to clock 2 or clock 2 to clock 1
$t_d(CAS-RAS)$		Delay time, column address strobe to row address strobe
$t_d(CAS-W)$	$t_d(CAS-WR)$	Delay time, column address strobe to write
$t_d(RAS-CAS)$		Delay time, row address strobe to column address strobe
$t_d(RAS-W)$	$t_d(RAS-WR)$	Delay time, row address strobe to write
$t_{dis}(R-Q)$	$t_{dis}(R-DA)$	Output disable time after read
$t_{dis}(S)$	$t_{PZ}(CS)$	Output disable time after chip select
$t_{dis}(W)$	$t_{PZ}(WR)$	Output disable time after write
t_{DHL}		High-level to low-level delay time } the time interval between specified reference points on the input and on the output pulses when the output is going to the low (high) level and when the device is driven with a specified loading networks
t_{DLH}		
$t_{en}(A-Q)$	$t_{PZV}(A-DQ)$	Output enable time after address
$t_{en}(R-Q)$	$t_{PZV}(R-DQ)$	Output enable time after read
$t_{en}(S-Q)$	$t_{PZX}(CS-DQ)$	Output enable time after chip select
t_f		Fall time
t_h		Hold time—the interval of time during which a signal at a specified input terminal appears after an active transition occurs at another specified input terminal
$t_h(A)$	$t_h(AD)$	Address hold time
$t_h(A-E)$	$t_h(AD-CE)$	Chip enable hold time after address
$t_h(A-PR)$	$t_h(AD-PRO)$	Program hold time after address
$t_h(CAS-CA)$		Column address hold time after column address strobe
$t_h(CAS-D)$	$t_h(CAS-DA)$	Data-in hold time after column address strobe
$t_h(CAS-Q)$	$t_h(CAS-OUT)$	Data-out hold time after column address strobe
$t_h(CAS-RAS)$		Row address strobe hold time after column address strobe
$t_h(CAS-W)$	$t_h(CAS-WR)$	Write hold time after column address strobe
$t_h(D)$	$t_h(DA)$	Data-in hold time
$t_h(D-PR)$	$t_h(DA-PRO)$	Program hold time after data-in
$t_h(E)$	$t_h(CE)$	Chip enable hold time
$t_h(E-D)$	$t_h(CE-DA)$	Data-in hold time after chip enable
$t_h(E-G)$	$t_h(CE-OE)$	Output enable hold time after chip enable
$t_h(R)$	$t_h(RD)$	Read hold time
$t_h(RAS-CA)$		Column address hold time after row address strobe
$t_h(RAS-CAS)$		Column address strobe hold time after row address strobe
$t_h(RAS-D)$	$t_h(RAS-DA)$	Data-in hold time after row address strobe
$t_h(RAS-W)$	$t_h(RAS-WR)$	Write hold time after row address strobe
$t_h(S)$	$t_h(CS)$	Chip select hold time
$t_h(W)$	$t_h(WR)$	Write hold time
$t_h(W-CAS)$	$t_h(WR-CAS)$	Column address strobe hold time after write
$t_h(W-D)$	$t_h(WR-DA)$	Data-in hold time after write
$t_h(W-RAS)$	$t_h(WR-RAS)$	Row address hold time after write
t_{PHL}		High-level to low-level propagation time } the time interval between specified reference points on the input and on the output pulses when the output is going to the low (high) level and when the device is driven and loaded by typical devices of stated type
t_{PLH}		
t_r		Rise time
$t_{rec}(W)$	t_{wr}	Write recovery time—the time interval between the termination of a write pulse and the initiation of a new cycle
$t_{rec}(PD)$	$t_R(PD)$	Power-down recovery time
t_{su}		Setup time—the time interval between the application of a signal which is maintained at a specified input terminal and a consecutive active transition at another specified input terminal
$t_{su}(A)$	$t_{su}(AD)$	Address setup time

New symbol	Former symbol	Parameter—definition
$t_{su}(A-E)$	$t_{su}(AD-CE)$	Chip enable setup time before address
$t_{su}(A-W)$	$t_{su}(AD-WR)$	Write setup time before address
$t_{su}(CA-RAS)$		Row address strobe setup time before column address
$t_{su}(D)$	$t_{su}(DA)$	Data-in setup time
$t_{su}(D-E)$	$t_{su}(DA-CE)$	Chip enable setup time before data in
$t_{su}(D-W)$	$t_{su}(DA-WR)$	Write setup time before data-in
$t_{su}(E)$	$t_{su}(CE)$	Chip enable setup time
$t_{su}(E-P)$	$t_{su}(CE-P)$	Precharge setup time before chip enable
$t_{su}(G-E)$	$t_{su}(OE-CE)$	Chip enable setup time before output enable
$t_{su}(P-E)$	$t_{su}(P-CE)$	Chip enable setup time before precharge
$t_{su}(PD)$		Power down setup time
$t_{su}(R)$	$t_{su}(RD)$	Read setup time
$t_{su}(R-CAS)$	$t_{su}(RA-CAS)$	Column address strobe setup time before read
$t_{su}(RA-CAS)$		Column address strobe setup time before row address
$t_{su}(S)$	$t_{su}(CS)$	Chip select setup time
$t_{su}(S-W)$	$t_{su}(CS-WR)$	Write setup time before chip select
$t_{su}(W)$	$t_{su}(WR)$	Write setup time
t_{THL}		High-level to low-level transition time
t_{TLH}		Low-level to high-level transition time
		} the time interval between specified reference points on the edge of the output pulse when the output is going to the low (high) level and when a specified input signal is applied through a specified network and the output is loaded by another specified network
$t_v(A)$	$t_{dv}(AD)$	Data valid time after address
$t_v(E)$	$t_{dv}(CE)$	Data valid time after chip enable
$t_v(E)PR$	$t_v(CE)PR$	Data valid time after chip enable in program mode
$t_v(G)$	$t_v(OE)$	Data valid time after output enable
$t_v(PR)$		Data valid time after program
$t_v(S)$	$t_v(CS)$	Data valid time after chip select
t_w		Pulse width (pulse duration) the time interval between specified reference points on the leading and trailing edges of the waveforms
$t_w(E)$	$t_w(CE)$	Chip enable pulse width
$t_w(EH)$	$t_w(CEH)$	Chip enable high pulse width
$t_w(EL)$	$t_w(EL)$	Chip enable low pulse width
$t_w(PR)$		Program pulse width
$t_w(R)$	$t_w(RD)$	Read pulse width
$t_w(S)$	$t_w(CS)$	Chip select pulse width
$t_w(W)$	$t_w(WR)$	Write pulse width
$t_w(\phi)$		Clock pulse width
T_a		Ambient temperature
T_{opr}		Operating temperature
T_{stg}		Storage temperature
V_{BB}		V_{BB} supply voltage
V_{CC}		V_{CC} supply voltage
V_{DD}		V_{DD} supply voltage
V_{GG}		V_{GG} supply voltage
V_i		Input voltage
V_{IH}		High-level input voltage—the value of the permitted high-state voltage at the input
V_{IL}		Low-level input voltage—the value of the permitted low-state voltage at the input
V_o		Output voltage
V_{OH}		High level output voltage—the value of the guaranteed high-state voltage range at the output
V_{OL}		Low-level output voltage—the value of the guaranteed low state voltage range at the output
V_{SS}		V_{SS} supply voltage

Note 1. These letter symbols are based on the IEC publication 148 except a part of them

QUALITY ASSURANCE AND RELIABILITY TESTING

1 INTRODUCTION

IC & LSI have made rapid technical progress in electrical performances of high integration, high speed, and sophisticated functionality. And now they have got boundless wider applications in electronic systems and electrical appliances.

To meet the above trend of expanding utilization of IC & LSI, Mitsubishi considers that it is extremely important to supply stable quality and high reliable products to customers.

Mitsubishi Electric places great emphasis on quality as a basic policy "Quality First", and has striven always to improve quality and reliability.

Mitsubishi has already developed the Quality Assurance System covering design, manufacturing, inventory and delivery for IC & LSI, and has supplied highly reliable products to customers for many years. The following articles describe the Quality Assurance System and examples of reliability control for Mitsubishi Single-chip 8-bit Micro-computer.

2. QUALITY ASSURANCE SYSTEM

The Quality Assurance System places emphasis on built-in reliability in designing and built-in quality in manufacturing. The System from development to delivery is summarized in Fig. 1.

2.1 Quality Assurance in Designing

The following steps are applied in the designing stage for a new product.

- (1) Setting of performance, quality and reliability target for new product.
- (2) Discussion of performance and quality for circuit design, device structure, process, material and package.
- (3) Verification of design by CAD system to meet standardized design rule.
- (4) Functional evaluation for bread-board device to confirm electrical performance.
- (5) Reliability evaluation for TEG (Test Element Group) chip to detect basic failure mode and investigate failure mechanism.
- (6) Reliability test (In-house qualification) for new product to confirm quality and reliability target.
- (7) Decision of pre-production from the standpoint of performance, reliability, production flow/conditions, production capability, delivery and etc

2.2 Quality Assurance in Manufacturing

Quality assurance in manufacturing is performed as follows

- (1) Environment control such as temperature, humidity and dust as well as deionized water and utility gases.
- (2) Maintenance and calibration control for automatized manufacturing equipments, automatic testing equipments, and measuring instruments.

- (3) Material control such as silicon wafer, lead frame, packaging material, mask and chemicals.
- (4) In-process inspections in wafer-fabrication, assembly and testing.
- (5) 100% final inspection of electrical characteristics, visual inspection and burn-in, if necessary.
- (6) Quality assurance test
 - Electrical characteristics and visual inspection, lot by lot sampling
 - Environment and endurance test, periodical sampling.
- (7) Inventory and shipping control, such as storage environment, date code identification, handling and ESD (Electro Static Discharge) preventive procedure.

2.3 Reliability Test

To verify the reliability of a product as described in the Mitsubishi Quality Assurance System, reliability tests are performed at three different stages in new product development, pre-production and mass-production.

At the development of a new product the reliability test plan is fixed corresponding to the quality and reliability target of each product, respectively. The test plan includes in-house qualification test and TEG evaluation, if necessary. TEG chips are designed and prepared for new device structure, new process and new material.

After the proto-type product has passed the in-house qualification test, the product advances to the pre-production. In the pre-production stage, the specific reliability tests are programmed and performed again to verify the quality of pre-production product.

In the mass production, the reliability tests are performed periodically to confirm the quality of the mass production product according to the quality assurance test program. Table 1 shows an example of reliability test program for plastic encapsulated IC & LSI.

Table 1. TYPICAL RELIABILITY TEST PROGRAM FOR PLASTIC ENCAPSULATED IC & LSI

Group	Test	Test condition
1	Solderability	230°C, 5sec Rosin flux
	Soldering heat	260°C, 10sec
2	Thermal shock	-55°C, 125°C, 15cycles
	Temperature cycling	-65°C, 150°C, 100cycles
3	Lead fatigue	250gr, 90°, 2arcs
	Shock	1500G, 0.5msec
4	Vibration	20G, 100~2000Hz X, Y, Z direction 4min./cycle, 4cycles/direction
	Constant acceleration	20000G, Y direction, 1min
5	Operation life	T _a =125°C, V _{cc} max 1000hours
6	High temperature storage life	T _a =150°C, 1000hours
7	High temperature and high humidity	85°C, 85%, 1000hours
	Pressure cooker	121°C, 100%, 100hours

QUALITY ASSURANCE AND RELIABILITY TESTING

2.4 Returned Product Control

When failure analysis is requested by a customer, the failed devices are returned to Mitsubishi Electric via the sales office of Mitsubishi using the form of "Analysis Request of Returned Product"

Mitsubishi provides various failure analysis equipments to analyze the returned product. A failure analysis report is

generated to the customer upon completion of the analysis. The failure analysis result enforces taking corrective action for the design, fabrication, assembly or testing of the product to improve reliability and realize lower failure rate.

Fig. 2 shows the procedure of returned product control from customer.

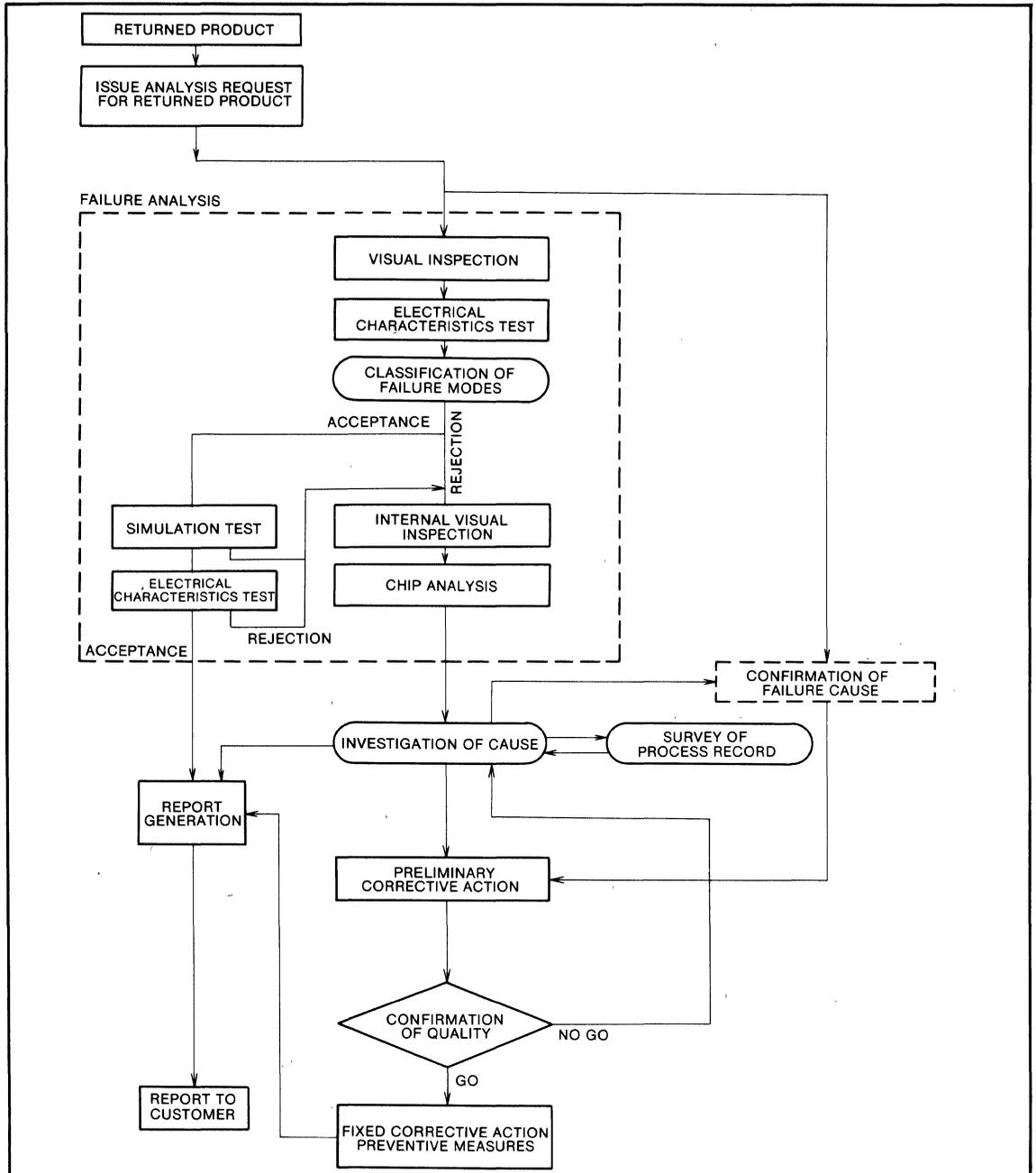


Fig.2 PROCEDURE OF RETURNED PRODUCT CONTROL

MITSUBISHI MICROCOMPUTERS

QUALITY ASSURANCE AND RELIABILITY TESTING

3 RELIABILITY TEST RESULTS

The reliability test results for Mitsubishi Single-chip 8-bit Microcomputers are shown in Table 2, Table 3 and Table 4.

Table 2 shows the result of endurance tests of high temperature operation life and high temperature storage life test

for representative types of Single-chip 8-bit Microcomputers.

Table 2. ENDURANCE TEST RESULTS

Test	Series	Type Number	Test Condition	Number of Samples	Device Hours (Hours)	Number of Failures
High Temperature Operation Life	MELPS 740	M37100M8-XXXSP	125°C 7V	35	35000	0
		M37201M6-XXXSP		35	35000	0
		M37260M6-XXXSP		35	35000	0
		M37120M6-XXXFP		38	38000	0
		M37409M2-XXXSP		38	38000	0
		M37420M6-XXXSP		22	22000	0
	EPROM mounted type	M37201E6-XXXSP	125°C 7V	35	35000	0
		M37410E6HXXXFP		38	38000	0
		M37420E6-XXXSP		32	32000	0
High Temperature Storage Life	MELPS 740	M37100M8-XXXSP	150°C	35	35000	0
		M37201M6-XXXSP		35	35000	0
		M37260M6-XXXSP		35	35000	0
		M37409M2-XXXSP		38	38000	0
		M37201M6-XXXSP		35	35000	0
	EPROM mounted type	M37420E6-XXXSP	150°C	35	35000	0
			175°C	22	22000	0

MITSUBISHI MICROCOMPUTERS

QUALITY ASSURANCE AND RELIABILITY TESTING

Table 3 shows the results of the environment tests of thermal stress high temperature/high humidity and pressure-cooker test for the same type of products in regards to en-

duration tests.

Table 4 shows the results of mechanical tests for representative products of various package types.

Table 3. ENVIRONMENTAL TEST RESULTS

Test	Series	Type Number	Test Condition	Number of Samples	Device Hours (Hours)	Number of Failures
High Temperature High Humidity Life	MELPS 740	M37100M8-XXXSP	85°C 85%RH 5 V	24	24000	0
		M37201M6-XXXSP		24	24000	0
		M37260M6-XXXSP		24	24000	0
		M37120M6-XXXFP		22	22000	0
		M37409M2-XXXSP		38	38000	0
		M37420M6-XXXSP		22	22000	0
	EPROM mounted type	M37201M6-XXXSP	85°C 85%RH 5 V	24	24000	0
		M37420E6-XXXSP		22	22000	0

Test	Series	Type Number	Test Condition	96Hours	240Hours
Pressure Cooker	MELPS 740	M37100M8-XXXSP	121°C 2 atmospheres	0/22	0/22
		M37201M6-XXXSP		0/22	0/22
		M37260M6-XXXSP		0/22	0/22
		M37120M6-XXXFP		0/22	0/22
		M37409M2-XXXSP		0/22	0/22
		M37420M6-XXXSP		0/22	0/22
	EPROM mounted type	M37201E6-XXXSP	121°C 2 atmospheres	0/22	0/22
		M37410E6HXXXFP		0/22	0/22
		M37420E6-XXXSP	0/22	0/22	

Test	Series	Type Number	Test Condition	10Cycles	100Cycles
Temperature Cycling	MELPS 740	M37100M8-XXXSP	-65°C ~ +150°C	0/38	0/38
		M37201M6-XXXSP		0/38	0/38
		M37260M6-XXXSP		0/38	0/38
		M37120M6-XXXFP		0/38	0/38
		M37409M2-XXXSP		0/38	0/38
		M37420M6-XXXSP		0/22	0/22
	EPROM mounted type	M37201E6-XXXSP	-65°C ~ +125°C	0/38	0/38
		M37410E6HXXXFP		0/38	0/38
		M37420E6-XXXSP	0/32	0/32	

Table 4. MECHANICAL TEST RESULTS

Test	Test Condition	Package			
		52P4B	64P4B	60P6	80P6
Soldering Heat	260°C 10sec	0/130	0/192	0/104	0/66
Thermal Shock	-40°C ~ 125°C 15Cycle	0/130	0/192	0/104	0/66
Solderebility	230°C 5sec Using a rosin-type Flux	0/66	0/88	0/88	0/66
Free Fall	75cm Onto a maple wood board 3times	0/44	0/44	0/22	0/44
Shock	1500G 0.5msec X, Y, and Z directions 3times	0/44	0/44	0/22	0/22
Vibration	20G X, Y, and Z directions 4times 100~2000Hz 4minutes/Cycle	0/44	0/44	0/22	0/22
Constant Acceleration	20000G Y ₁ direction 1minute	0/44	0/44	0/22	0/22
Lead Integrity	250g 90° Berding 2times	0/30	0/30	0/15	0/15
	500g Tension 30sec	0/30	0/30	0/15	0/15

QUALITY ASSURANCE AND RELIABILITY TESTING

4 FAILURE ANALYSIS

Accelerated reliability tests are applied to observe failures caused by temperature, voltage, humidity, current, mechanical stress and those combined stresses on chips and packages.

Examples of typical failure modes are shown below.

(1) Wire Bonding Failure by Thermal Stress

Fig. 3, Fig. 4 and Fig. 5 are example of a failure occurred by temperature storage test of 225°C, 1000hours.

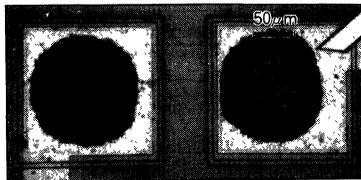


Fig.3
Micrograph of lifted Au ball trace on Al bonding pad

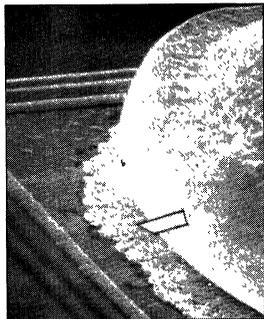


Fig.4
Au-Al plague formation on bonding pad

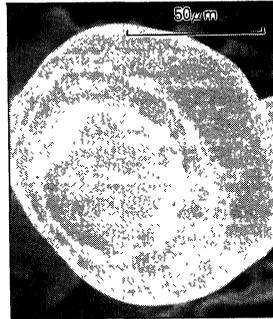


Fig.5
Lifted Au wire ball base

- Au-Al intermetallic formation so-called "Purple plague" by thermal overstress makes Au wire lift off from aluminum metallization. The activation energy of this failure mode is estimated approximately 1.0eV and no failure has been observed so far in practical uses.
- (2) Aluminum Corrosion Failure by Temperature/Humidity Stress.

Fig. 6, Fig. 7 and Fig. 8 are an example of corroded failure of aluminum metallization in plastic encapsulated IC after accelerated temperature/humidity storage test (pressure cooker test) of 121°C, 100% RH, 1000hours duration.

Aluminum bonding pad is dissolved by penetrated water from plastic package, and chlorine concentration is observed on corroded aluminum bonding pad as shown in Fig. 8.



Fig.6
Micrograph of corroded Aluminum metallization

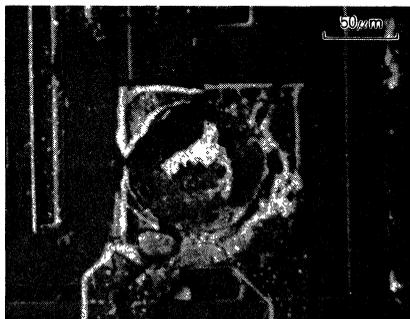


Fig.7
Enlarged
micrograph
of corroded
Aluminum
bonding pad

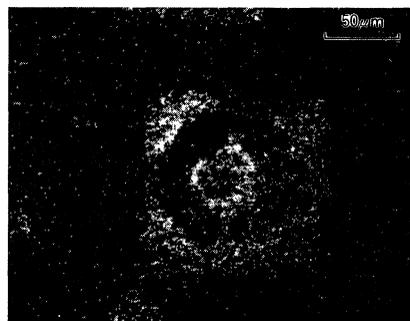


Fig.8
CI
distribution
on corroded
Aluminum
bonding pad

- (3) Destructive Failure by Electrical Overstress
ESD have been performed to reproduce the electrical overstress failure in field uses.
Fig. 9 and Fig. 10 are an example of failure observed by surge voltage test. The trace of destruction is verified as the aluminum bridge by X-ray micro analysis.

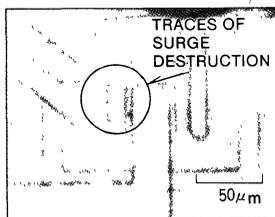


Fig.9
Micrograph of surge
voltage destruction

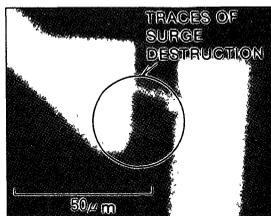


Fig.10
Aluminum trace
of destructive spot

- (4) Aluminum Electromigration

Fig. 11 shows an open circuit of aluminum metallization in high current density region caused by accelerated operating life test. This failure is caused by the aluminum electromigration. Voids and hillock have been formed in aluminum metallization by high current density.

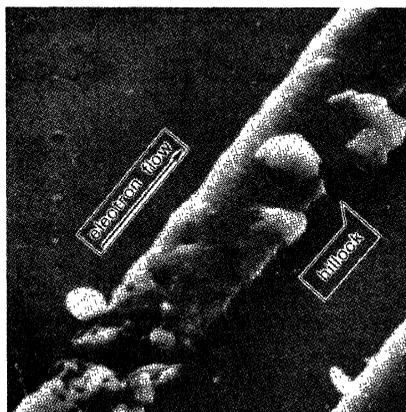


Fig.11
Voids and
hillocks
formation
by Aluminum
electromigration

5 SUMMARY

The Mitsubishi quality assurance system and examples of reliability control have been discussed. Customer's interest and requirement for high reliable IC & LSI are increasing significantly. To satisfy customer's expectancy, Mitsubishi as an IC vendor, would like to make perpetual efforts in the following areas.

- (1) Emphasis on built-in reliability at design stage and reliability evaluation to investigate latent failure modes and acceleration factors.
- (2) Execution of periodical endurance, environment and mechanical test to verify reliability target and realize higher reliability.
- (3) Focus on development of advanced failure analysis techniques. Detail failure analysis, intensive corrective action and quick response to customer's analysis request.
- (4) Collection of customer's quality data in qualification, incoming inspection, production and field use to improve PPM, fraction defective and FIT, failure rate.

Mitsubishi would highly appreciate if the customer would provide quality and reliability data of incoming inspection or field failure rate essential to verify and improve the quality/reliability of IC & LSI.

PRECAUTIONS IN HANDLING MOS IC/LSIs

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance (g_m) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. Therefore the following recommendations should be followed in handling MOS devices.

1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber foam, aluminum foil, shielded boxes or other protective precautions.

3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

1. All electric equipment, work table surfaces and operat-

ing personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a $1m\Omega$ resistor. Be sure that the grounding meets national regulations on personnel safety.

2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchroscopes must be checked for current leakage before being grounded.

4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines between input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which can result in the destruction of the device.
2. When input/output, or input and/or output, terminals of MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to §2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

MICROCOMPUTERS FOR TV

M37100M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37100M8-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or a 80-pin plastic molded QFP. This single-chip microcomputer is useful for the high-tech channel-selection system for TVs. In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

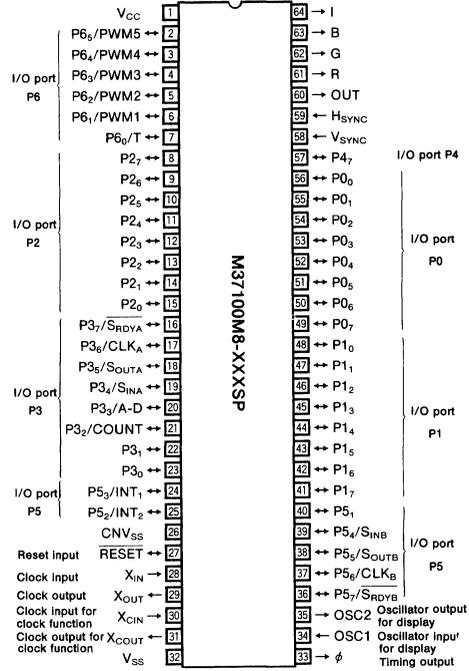
FEATURES

- Number of basic instructions 69
- Memory size
 - ROM 16384 bytes
 - RAM 320 bytes
- Instruction execution time
 - 2μs (minimum instructions at 4MHz frequency)
- Single power supply 5V±10%
- Power dissipation normal operation mode (at 4MHz frequency, CRT display off) 27.5mW
- Subroutine nesting 96levels (Max.)
- Interrupt 9types, 5vectors
- 8-bit timer 3 (2 when used as serial I/O_A)
- Programmable I/O ports (Ports P0, P1, P2, P3, P4, P5, P6) 46
- Serial I/O (8-bit) 2
- PWM function 14-bit×1
6-bit×2
- Comparator 1
- Two clock generating circuits (One is for main clock, the other is for clock function)
- 63-character on screen display function
 - Number of character 21 characters×3 lines
 - Character configuration 12×16 dots
 - Kinds of character 96
 - Horizontal character border function

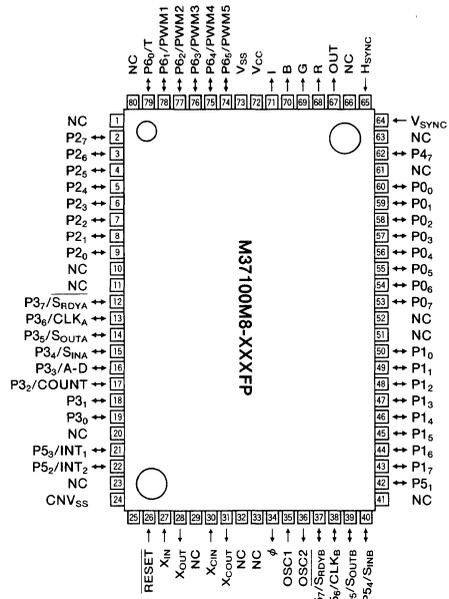
APPLICATION

TV

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

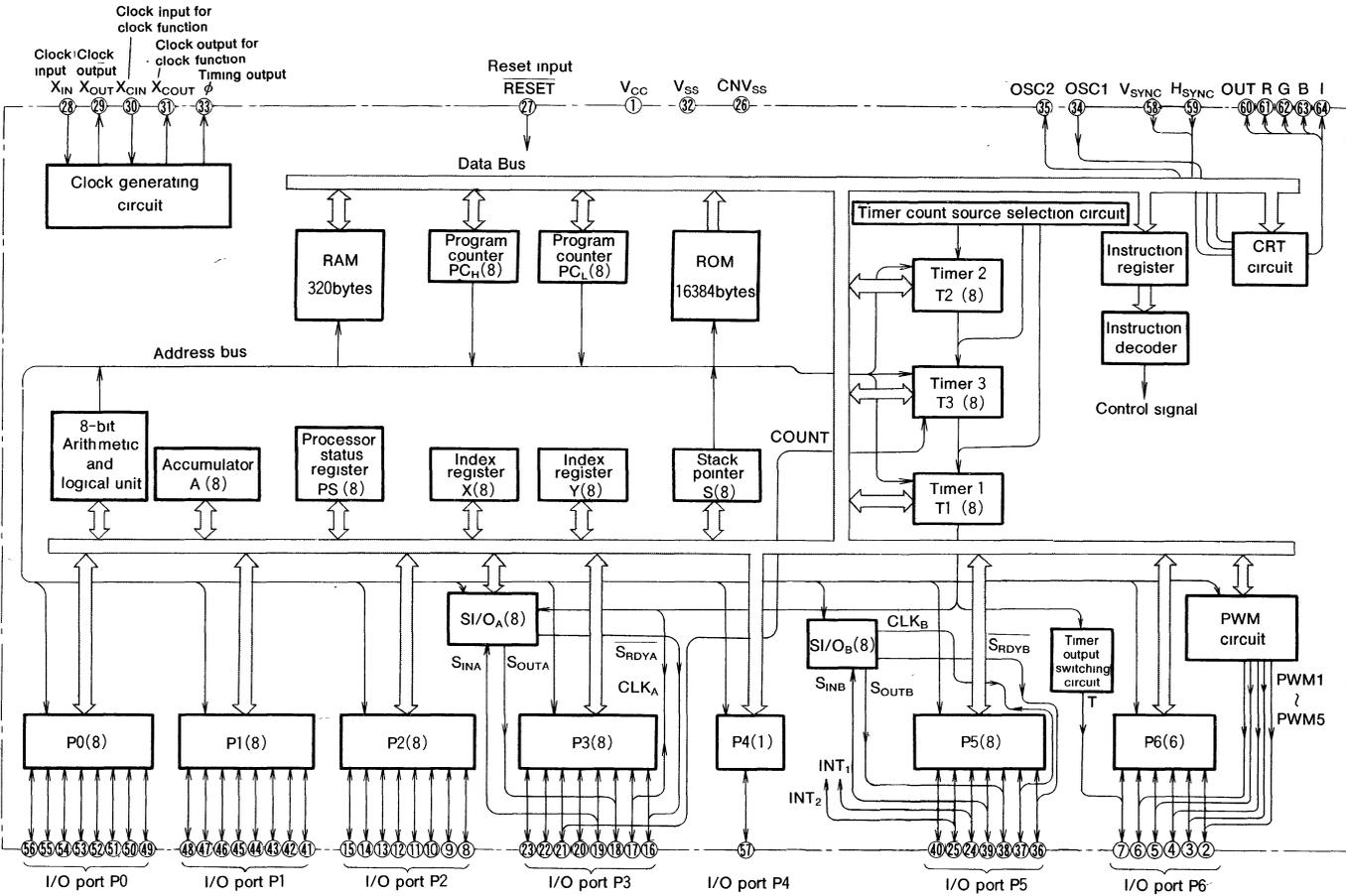


Outline 80P6

NC : No connection



M37100M8-XXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

MITSUBISHI MICROCOMPUTERS
M37100M8-XXXSP/FP

MITSUBISHI MICROCOMPUTERS
M37100M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONS OF M37100M8-XXXSP/FP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		2 μ s (minimum instructions, at 4MHz frequency)	
Clock frequency		4MHz	
Memory size	ROM	16384bytes	
	RAM	320bytes	
Input/Output ports	P0	I/O	8-bitX1 (middle-voltage N-channel open drain)
	P1, P2	I/O	8-bitX2
	P3	I/O	8-bitX1
	P4 ₇	I/O	1-bitX1
	I, B, G, R, OUT	Output	1-bitX5 (for CRT display function)
	V _{SYNC} , H _{SYNC}	Input	1-bitX2 (for CRT display function)
	P5 ₂ , P5 ₃	I/O	2-bitX1 (can be used as an input for either INT ₂ or INT ₁)
	P5 ₁ , P5 ₄ -P5 ₇	I/O	5-bitX1
	P6 ₀ , P6 ₁	I/O	2-bitX1
	P6 ₂ -P6 ₅	I/O	4-bitX1 (middle-voltage N-channel open drain)
Serial I/O		8-bitX2	
Timers		8-bit timerX3 (X2, when used as serial I/O _A)	
Subroutine nesting		96levels (max.)	
Interrupt		2 external interrupts, 6 internal interrupts, 1 software interrupt	
Clock generating circuit		Two built-in circuits (externally connected ceramic or quartz crystal oscillator), both circuits have option feedback resistors	
Supply voltage		5V \pm 10%	
Power dissipation	at high-speed operation	CRT display function ON	38.5mW (clock frequency X _{IN} =4MHz, f _{CRT} =6MHz)
		CRT display function OFF	27.5mW (clock frequency X _{IN} =4MHz)
	at low-speed operation at stop mode	CRT display function OFF	0.33mW (clock frequency X _{CIN} =32kHz)
			I _{CC} =1 μ A (when clock is stopped)
Input/Output characteristics	Input/Output voltage	12V (input/output P0, P6 ₂ -P6 ₅ , input RESET, CNV _{SS}) -0.3 to V _{CC} +0.3V(P1, P2, P3, P4 ₇ , P5, P6 ₀ , P6 ₁)	
	Output current	0.5mA (P0, P1, P2, P3, P5, P6 ₂ -P6 ₅ : N-channel open drain input/output) 0.5mA, -0.5mA (P4 ₇ : CMOS input/output, R, G, B, I, OUT, P6 ₀ -P6 ₁ : CMOS output)	
Operating temperature range		-10 to 70°C	
Device structure		CMOS silicon gate process	
Package	M37100M8-XXXSP	64-pin shrink plastic molded DIP	
	M37100M8-XXXFP	80-pin plastic molded QFP	
CRT display function	Number of character	21 charactersX3lines	
	Kinds of character	96 (12X16 dots)	

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is connect to V _{SS} .
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins and external condensers are connected. If an external clock is used, the clock source should be connected to the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin In single-chip mode, the output can be controlled by selecting the option
X _{CIN}	Clock input for clock function	Input	These are the I/O pins of the clock generating circuit for the clock function To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{CIN} and X _{COU} pins and external condensers are connected If an external clock is used, the clock source should be connected to the X _{CIN} pin and the X _{COU} pin should be left open
X _{COU}	Clock output for clock function	Output	
P0 ₀ -P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is middle-voltage N-channel open drain
P1 ₀ -P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 but the output structure is N-channel open drain It can be built in pull-up transistor at each pin by selecting the option.
P2 ₀ -P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P1
P3 ₀ -P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P1 When serial I/O _A is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as $\overline{\text{SRDYA}}$, CLK _A , S _{OUTA} , and S _{INA} pins, respectively. P3 ₃ works as an analog input for comparator and P3 ₂ works as a counter input
P4 ₇	I/O port P4	I/O	Port P4 ₇ is a 1-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output.
I, B, G, R, OUT	CRT output	Output	This is a 5-bit output pin for CRT display. The output polarity can be changed by selecting the option At reset, inactive polarity is selected The output structure is CMOS output
H _{SYNC}	H _{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display. The input polarity can be changed by selecting the option.
V _{SYNC}	V _{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display The input polarity can be changed by selecting the option
P5 ₂ , P5 ₃	I/O port P5	I/O	These ports have basically the same functions as port P1, and are in common with interrupt input pins
P5 ₁ , P5 ₄ -P5 ₇			These ports have basically the same functions as port P1. When serial I/O _B is used, P5 ₇ , P5 ₆ , P5 ₅ and P5 ₄ work as $\overline{\text{SRDYB}}$, CLK _B , S _{OUTB} and S _{INB} pins, respectively.
P6 ₀ -P6 ₅	I/O port P6	I/O	Port P6 is a 6-bit I/O port and has basically the same functions as port P0 The output structure of P6 ₀ , P6 ₁ is CMOS output and the output structure of P6 ₂ -P6 ₅ is middle-voltage N-channel open drain P6 ₀ , P6 ₁ , P6 ₂ , P6 ₃ , P6 ₄ , P6 ₅ can be programmed to function as timer output pin (T), PWM output pins (PWM1, PWM2, PWM3, PWM4 and PWM5), respectively
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display function To control generating frequency, external condensers and registers are connected.

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FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37100 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:
The FST and SLW instructions are not provided.
The MUL and DIV instructions are not provided.
The WIT instruction can be used.
The STP instruction can be used.

MEMORY

• **Special Function Register (SFR) Area**
The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- **RAM**
RAM is used for data storage as well as a stack area.
- **ROM**
ROM is used for storing user programs as well as the interrupt vector area.
- **RAM for display**
RAM for display is used to specify the character to be displayed on the CRT and its color.
- **Interrupt Vector Area**
The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.
- **Zero Page**
Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.
- **Special Page**
Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

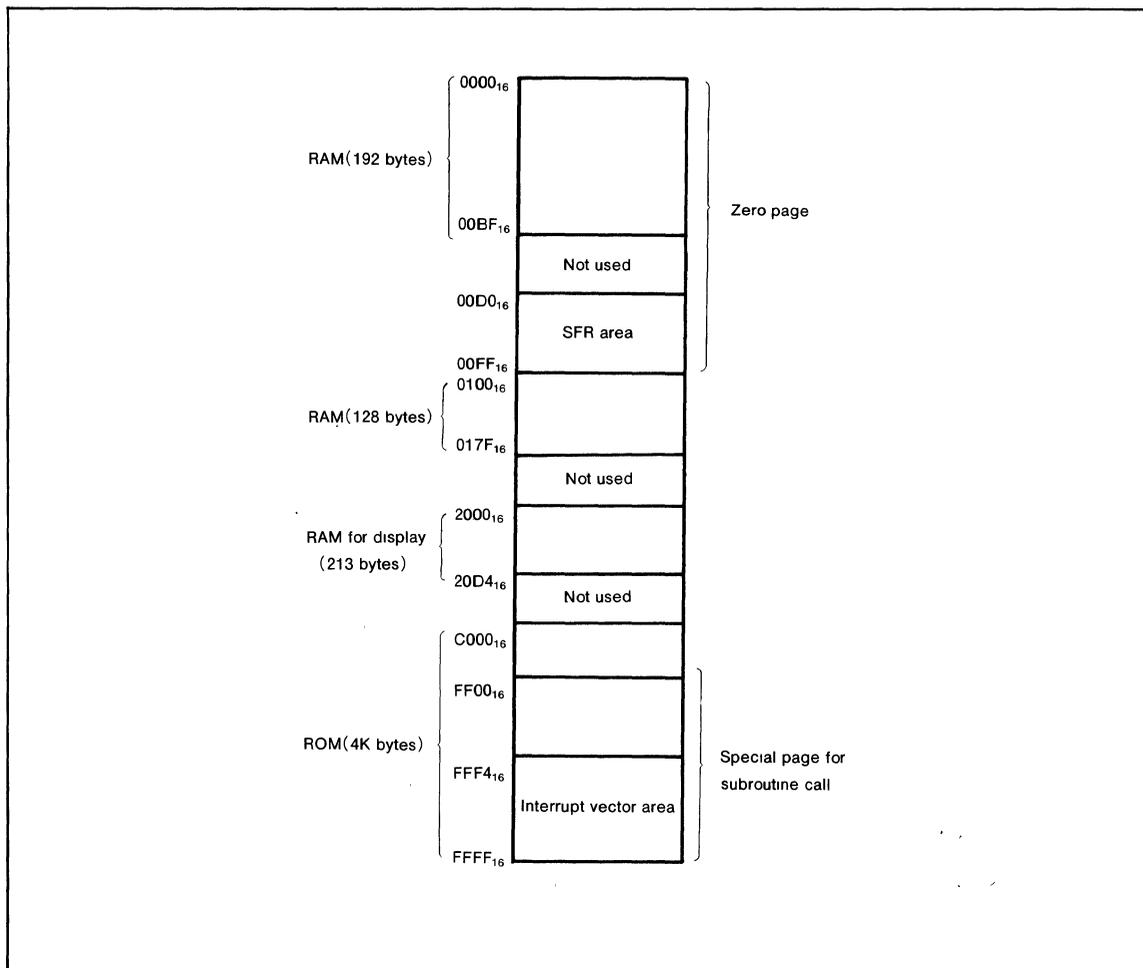


Fig. 1 Memory map

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00D0 ₁₆	Horizontal position register	00E8 ₁₆	Port P3
00D1 ₁₆	Vertical position register of block 1	00E9 ₁₆	Port P3 directional register
00D2 ₁₆	Vertical position register of block 2	00EA ₁₆	Port P4
00D3 ₁₆	Vertical position register of block 3	00EB ₁₆	Port P4 directional register
00D4 ₁₆	Color register 0	00EC ₁₆	Port P5
00D5 ₁₆	Color register 1	00ED ₁₆	Port P5 directional register
00D6 ₁₆	Color register 2	00EE ₁₆	Port P6
00D7 ₁₆	Color register 3	00EF ₁₆	Port P6 directional register
00D8 ₁₆	CRT control register	00F0 ₁₆	PWM1-H register
00D9 ₁₆	Display block counter	00F1 ₁₆	PWM1-L register
00DA ₁₆	Serial I/O _B mode register	00F2 ₁₆	PWM2 register
00DB ₁₆	Special mode register	00F3 ₁₆	PWM3 register
00DC ₁₆	Serial I/O _B register	00F4 ₁₆	PWM4 register
00DD ₁₆	Counter 0	00F5 ₁₆	PWM control register
00DE ₁₆		00F6 ₁₆	Serial I/O _A mode register
00DF ₁₆		00F7 ₁₆	Serial I/O _A register
00E0 ₁₆	Port P0	00F8 ₁₆	PWM5 register
00E1 ₁₆	Port P0 directional register	00F9 ₁₆	PWM output control register
00E2 ₁₆	Port P1	00FA ₁₆	Timer 1
00E3 ₁₆	Port P1 directional register	00FB ₁₆	Interrupt control register 2
00E4 ₁₆	Port P2	00FC ₁₆	Timer 2
00E5 ₁₆	Port P2 directional register	00FD ₁₆	Timer 3
00E6 ₁₆		00FE ₁₆	Interrupt control register 1
00E7 ₁₆	A-D control register	00FF ₁₆	Timer control register

Fig. 2. SFR (Special Function Register) memory map

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INTERRUPTS

Interrupts can be caused by 9 different events consisting of two external, six internal, and one software event.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

Falling edge active or rising edge active for each of the INT₁ and INT₂ external interrupts can be selected by bits 4 and 5 of the PWM control register. Whether the INT₁ and INT₂ external interrupts or the CRT display and serial I/O_B interrupts are to be accepted can be selected by bits 0 and 1 of interrupt control register 2.

Whether the timer 1 or serial I/O_A interrupt is to be accepted can be selected by bit 2 of the serial I/O_A mode register.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits and the interrupt enable bits are in interrupt control register 1 and timer control register. Figure 3 shows the structure of the interrupt control registers 1 and 2 and timer control register.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be clear with a program, but not set. The interrupt enable bit can be set and clear with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 4 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
INT ₁ or CRT display interrupt	2	FFFD ₁₆ , FFFC ₁₆	INT ₁ external interrupt (phase programmable)
Timer 3 interrupt	3	FFFB ₁₆ , FFFA ₁₆	
Timer 2 interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	
Timer 1 or serial I/O _A interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	
INT ₂ or serial I/O _B interrupt (BRK instruction interrupt)	6	FFF5 ₁₆ , FFF4 ₁₆	INT ₂ external interrupt (phase programmable) BRK instruction interrupt (non-maskable software interrupt)

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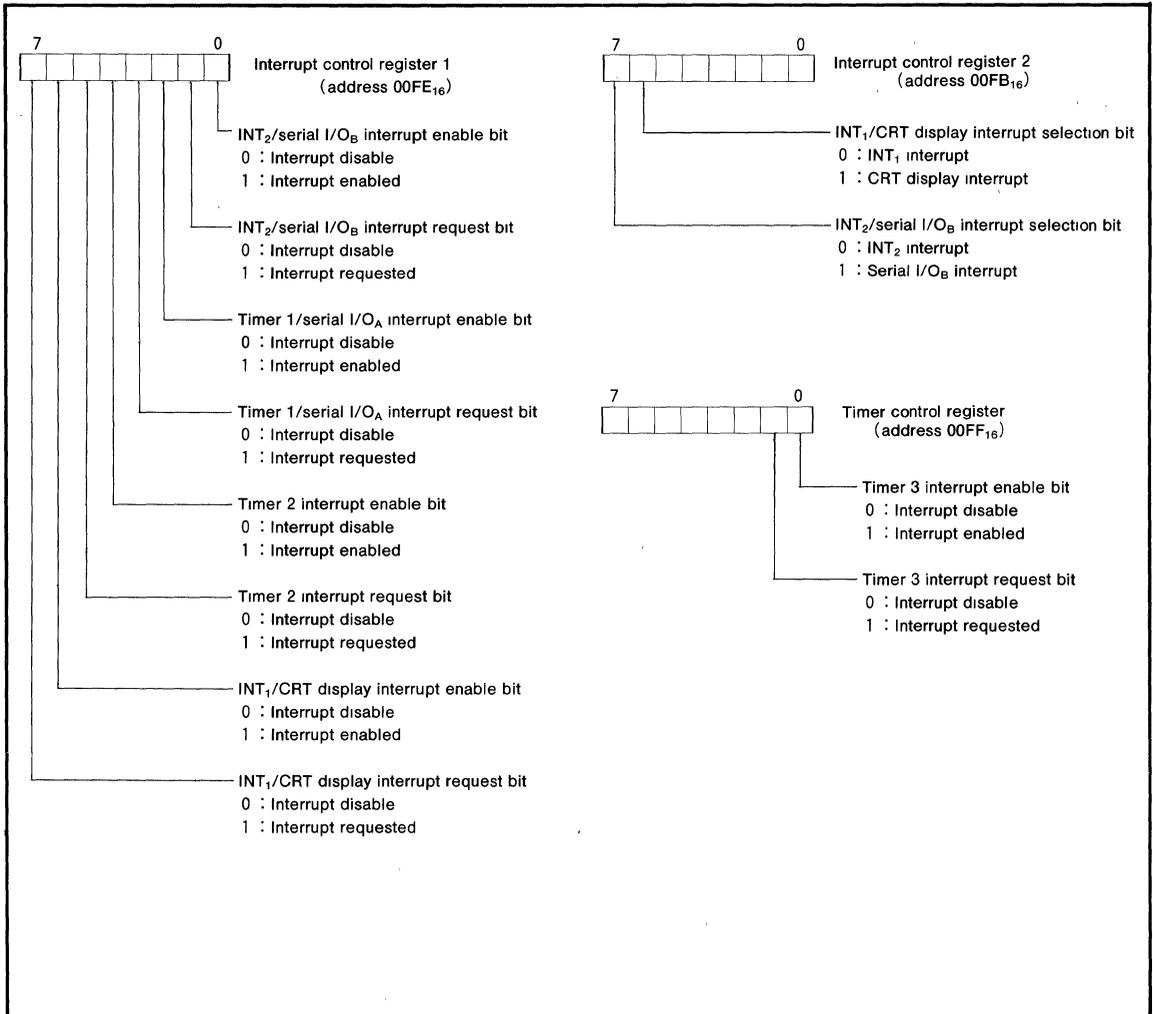


Fig. 3 Structure of registers related to interrupt

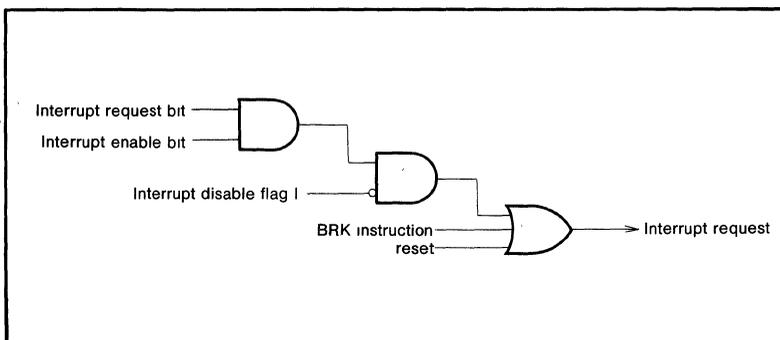


Fig. 4 Interrupt control

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

TIMER

The M37100M8-XXXSP/FP has three timers; timer 1, timer 2 and timer 3.

A block diagram of timer 1 through 3 is shown in Figure 6. The count source for timer 1 through 3 can be selected by using bit 2, 3 and 4 of the timer control register (address 00FF₁₆), as shown in Figure 5. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch.

The timer interrupt request bit which is in the interrupt control register 1 or timer control register (located at addresses 00FE₁₆ and 00FF₁₆ respectively) is set at the next count pulse after the timer reaches "0" (see interrupt section).

The starting and stopping of timer 2 is controlled by bit 5 of the timer control register. If the bit 5 is "0", the timer starts counting, and the bit 5 is "1", the timer stops.

At a reset or stop mode, FF₁₆ is automatically set in timer 2 and 07₁₆ in timer 3.

After a STP instruction is executed, timer 3, timer 2, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if timer 3 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 2 count stop bit) must be set to "0".

For more details on the STP instruction, refer to the oscillation circuit section.

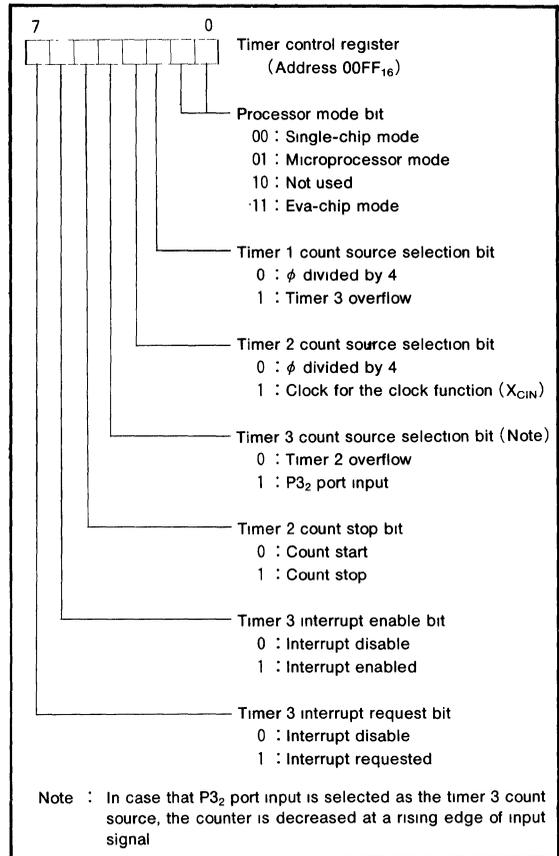


Fig. 5 Structure of timer control register

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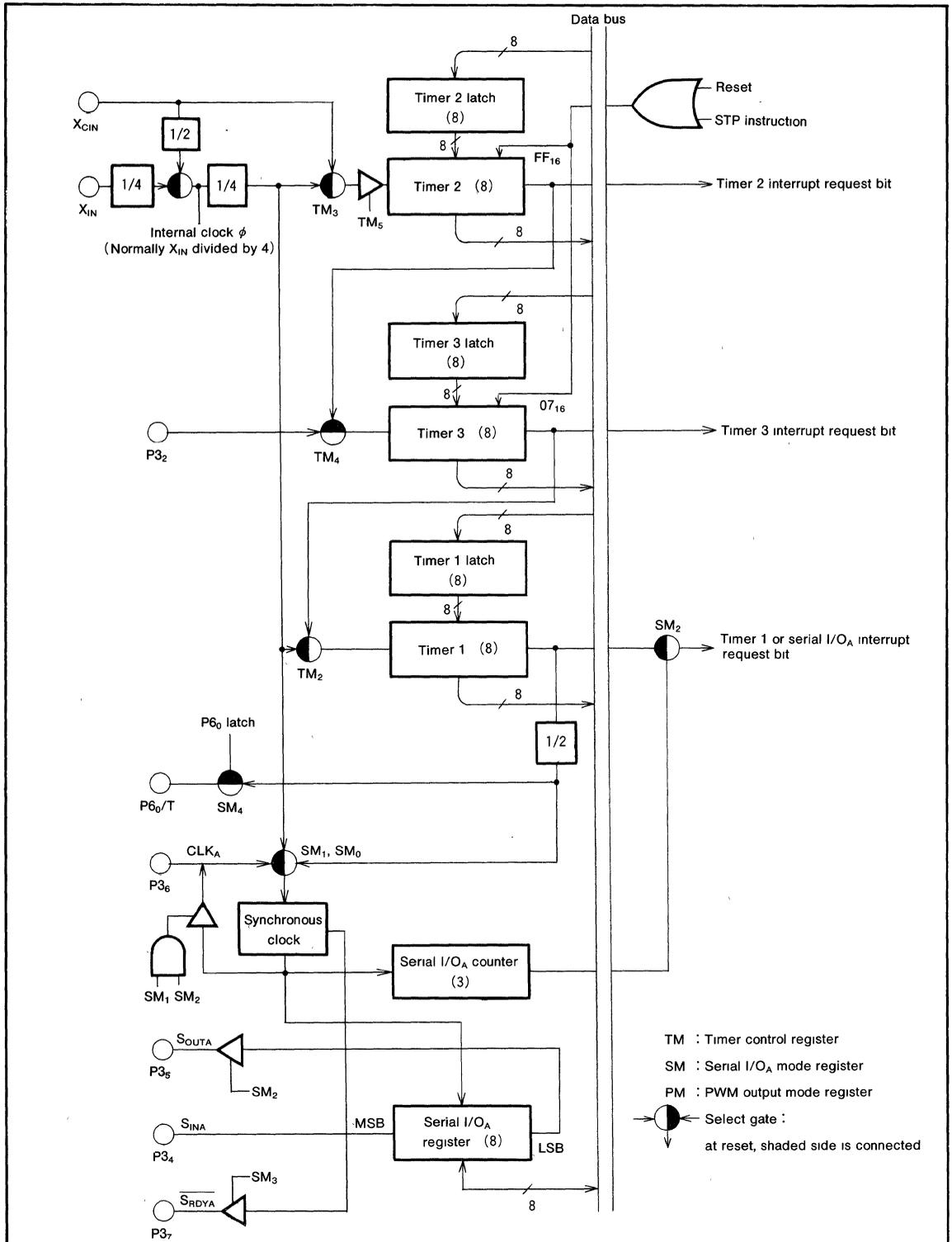


Fig. 6 Block diagram of timer 1 through 3

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SERIAL I/O

M37100M8-XXXSP/FP has two serial I/O (serial I/O_A and serial I/O_B).

SERIAL I/O_A

The block diagram of serial I/O_A is shown in Figure 7. In the serial I/O_A mode the receive ready signal ($\overline{S_{RDYA}}$), synchronous input/output clock (CLK_A), and the serial I/O_A (S_{OUTA}, S_{INA}) pins are used as P3₇, P3₆, P3₅, and P3₄, re-

spectively. The serial I/O_A mode register (address 00F6₁₆) is an 8-bit register. Bit 0 and 1 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from P3₆ is selected. When these bits are [10], the overflow signal divided by two from timer 1 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

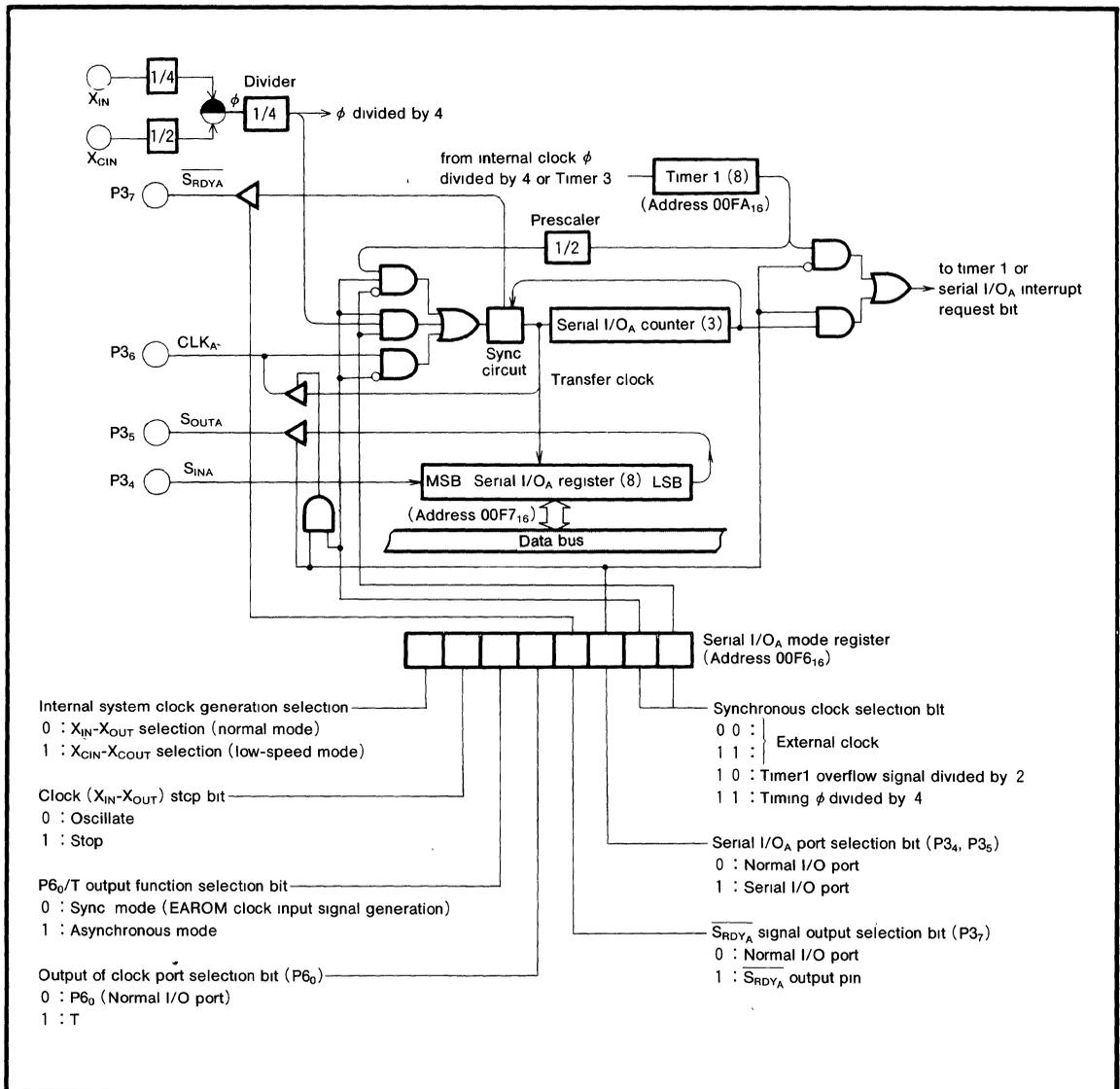


Fig. 7 Block diagram of serial I/O_A

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Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O_A or not. When bit 2 is "1", P3₆ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P3₆. If the external synchronous clock is selected, the clock is input to P3₆. And P3₅ will be a serial output, and P3₄ will be a serial input. To use P3₄ as a serial input, set the directional register bit which corresponds to P3₄, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O_A, bit 2 needs to be set to "1", if it is "0" P3₆ will function as a normal I/O. Interrupts will be generated from the serial I/O_A counter instead of timer 1. Bit 3 determines if P3₇ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDYA}}$) or used as a normal I/O pin (bit 3="0").

The function of serial I/O_A differs depending on the clock source; external clock or internal clock.

Internal Clock- The $\overline{S_{RDYA}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_A register. After the falling edge of write signal, the $\overline{S_{RDYA}}$

signal becomes low signaling that the M37100M8-XXXSP is ready to receive the external serial data. The $\overline{S_{RDYA}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_A counter is set to 7 when data is stored in the serial I/O_A register. At each falling edge of the transfer clock, serial data is output to P3₅. During the rising edge of this clock, data can be input from P3₄ and the data in the serial I/O_A register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O_A register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock- If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 8, and connection between two M37100M8-XXXSP's are shown in Figure 9.

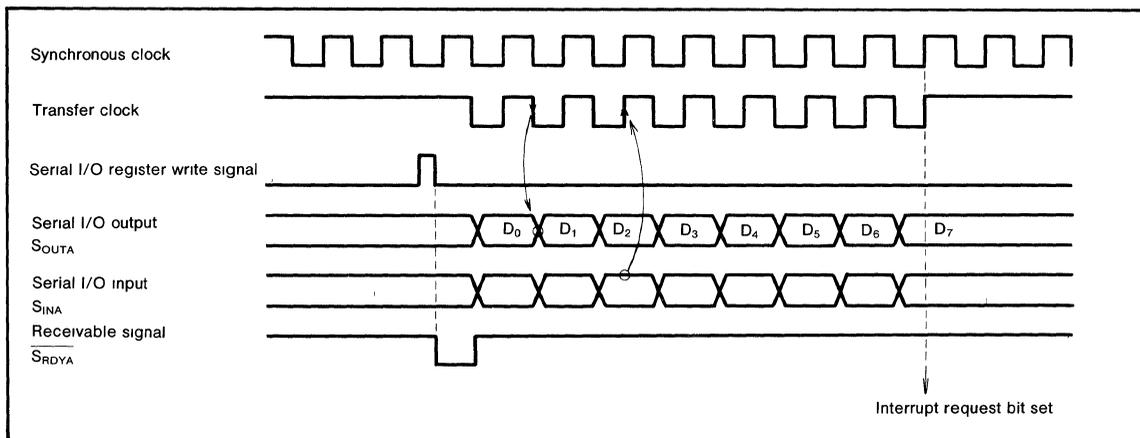


Fig. 8 Serial I/O_A timing

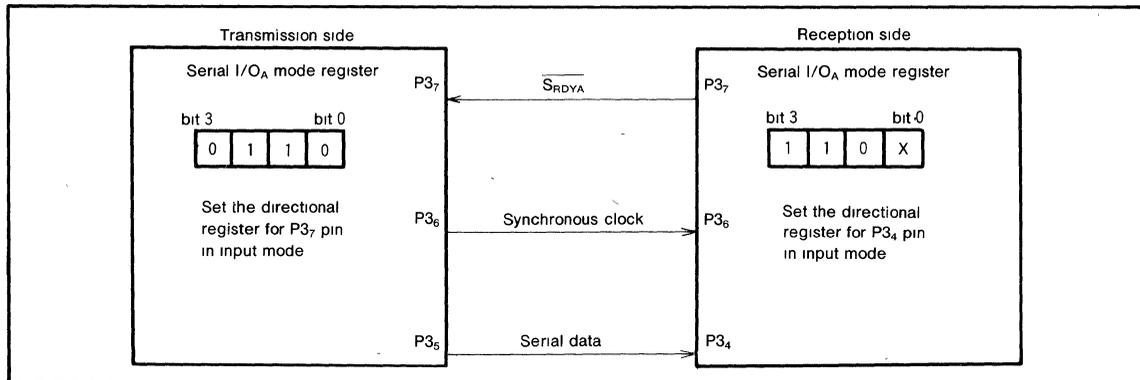


Fig. 9 Example of serial I/O_A connection

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SERIAL I/O_B

The block diagram of serial I/O_B is shown in Figure 10. In the serial I/O_B mode the receive ready signal ($\overline{S_{RDYB}}$), synchronous input/output clock (CLK_B), and the serial I/O_B (S_{OUTB} , S_{INB}) pins are used as P5₇, P5₆, P5₅, and P5₄, respectively. The serial I/O_B mode register (address 00DA₁₆) is an 8-bit register. Bit 1 of this register is used to select a synchronous clock source. When this bit is "0", an external clock from P3₆ is selected. When this bit is "1", the overflow signal divided by two from clock counter 0 becomes the synchronous clock.

Clock counter 0 is a 8-bit down counter to provide synchronous clock for serial I/O_B. This counter divides internal clock ϕ . Structure of clock counter 0 is the same of timers. Therefore, changing the timer period will change the transfer speed.

Bits 2 and 3 decide whether parts of P5 will be used as a serial I/O_B or not. When bit 2 is "1", P5₆ becomes an I/O pin of the synchronous clock. When an internal synchronous

clock is selected, the clock is output from P5₆. If the external synchronous clock is selected, the clock is input to P5₆. And P5₅ will be a serial output, and P5₄ will be a serial input. To use P5₄ as a serial input, set the directional register bit which corresponds to P5₄, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O_B, bit 2 needs to be set to "1", if it is "0" P5₆ will function as a normal I/O. Bit 3 determines if P5₇ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDYB}}$) or used as a normal I/O pin (bit 3="0"). Bit 4 is the special mode select bit. Serial I/O_B can be set to special mode by using this bit. Bits 0, 5, 6, and 7 are used for special mode. For details, see the section of special mode.

In the normal mode, operations of serial I/O_B are the same as that of serial I/O_A. For details, see the section of serial I/O_A.

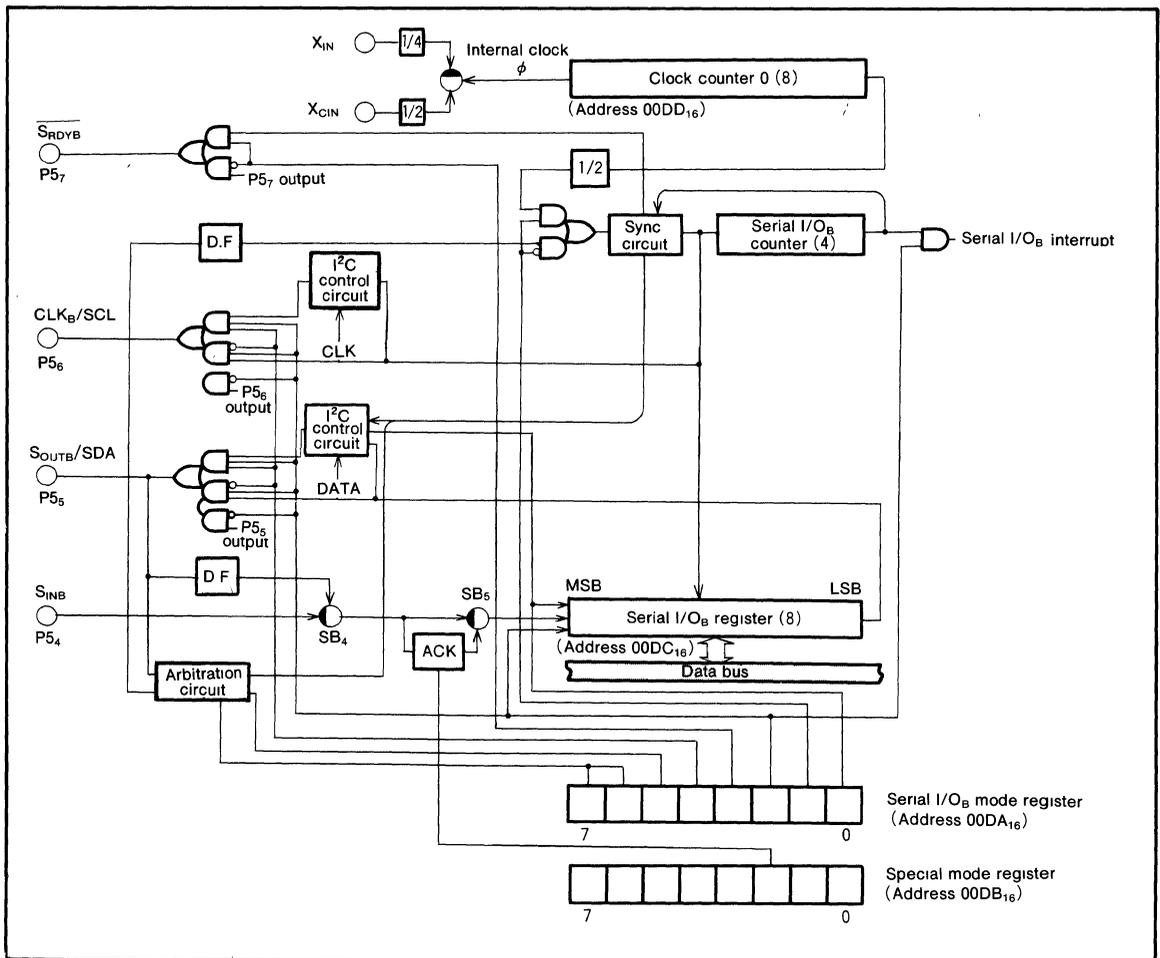


Fig. 10 Block diagram of serial I/O_B

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SPECIAL MODE (I²C BUS:INTER IC BUS*)

M37100M8-XXXSP/FP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I²C (Inter IC) bus format.

I²C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery.

M37100M8-XXXSP/FP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O are explained in the following:

(1) Master transmission

To generate an interrupt at the end of transmission, set bit 1 of interrupt control register 2 (address 00FB₁₆) to "1" so as to serial I/O_B interrupt is selected. Then set bit 0 of interrupt control register 1 (address 00FE₁₆) to "1" so as to serial I/O_B interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

The output signals of master transmission SDA and SCL are output from ports P5₅ and P5₆. Set all bits (bits 5 and 6) corresponding to P5₅ and P5₆ of the port P5 register (address 00EC₁₆) and the port P5 direction register (address 00ED₁₆) to "1".

Set the transmission clock. The transmission clock uses the overflow signal divided by 2 from clock counter 0. Set appropriate value in clock counter 0. (For instance, if 4 is set in clock counter 0 when f(X_{IN}) is 4MHz, the master transmission clock frequency is 100kHz).

Set contents of the special mode register (address 00DB₁₆). (Usually, 03₁₆.) Set the bit 4 of serial I/O_B mode register (address 00DA₁₆). Figure 13 shows the bit configurations of special mode register and serial I/O_B mode register.

Initial setting is completed by the above procedure.

Write data to be transmitted in the serial I/O_B register (address 00DC₁₆). Immediately after this, clear bits 0 and 1 of special mode register (to "0") to make both SDA and SCL output to "L". This is for arbitration. The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK receiving and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 1 of the timer control register is set to "1" (issue of interrupt request), notifying the end of data transmission.

To transmit data successively, write data to be sent to the serial I/O_B register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

To terminate data transfer, clear bits 0 and 1 of the special mode register to "0", set bit 1 clock SCL to 1, then set bit 1

data SDA to "1". This procedure transmits the stop signal.

Figure 11 shows master transmission timing explained above.

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission.

In the interrupt routine, setmaster reception ACK provided (36₁₆) in the serial I/O_B mode register (address 00DB₁₆), and write "FF₁₆" in the serial I/O_B register (address 00DC₁₆). This sets data line SDA to "H" and to perform 8-clock master reception. Then, "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission.

Figure 12 shows master reception timing.

(3) Wait function

Wait function 1 is held SCL line up "L" level after falling of the 8th clock.

Wait function 2 is held SCL line up "L" level after falling of the 9th clock.

The wait function is reset by setting bit 5, 6 of the special mode register to "1".

*:Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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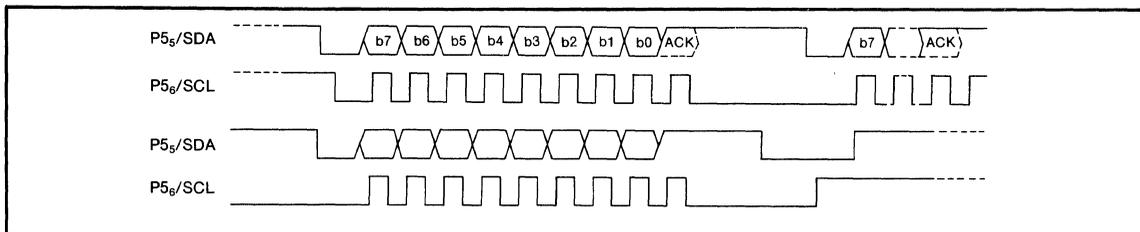


Fig. 11 Master transmission timing

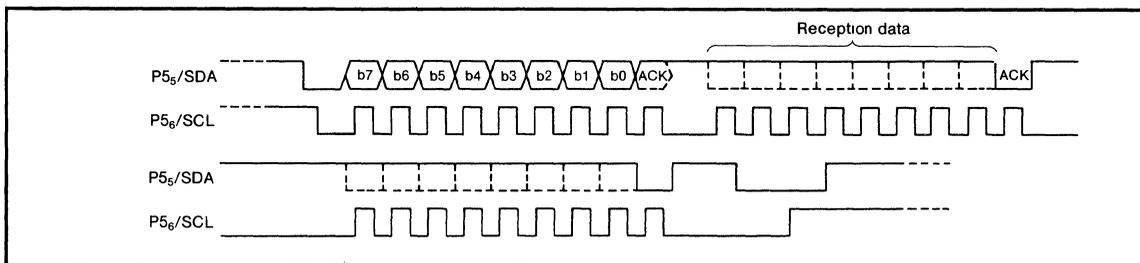


Fig. 12 Master reception timing

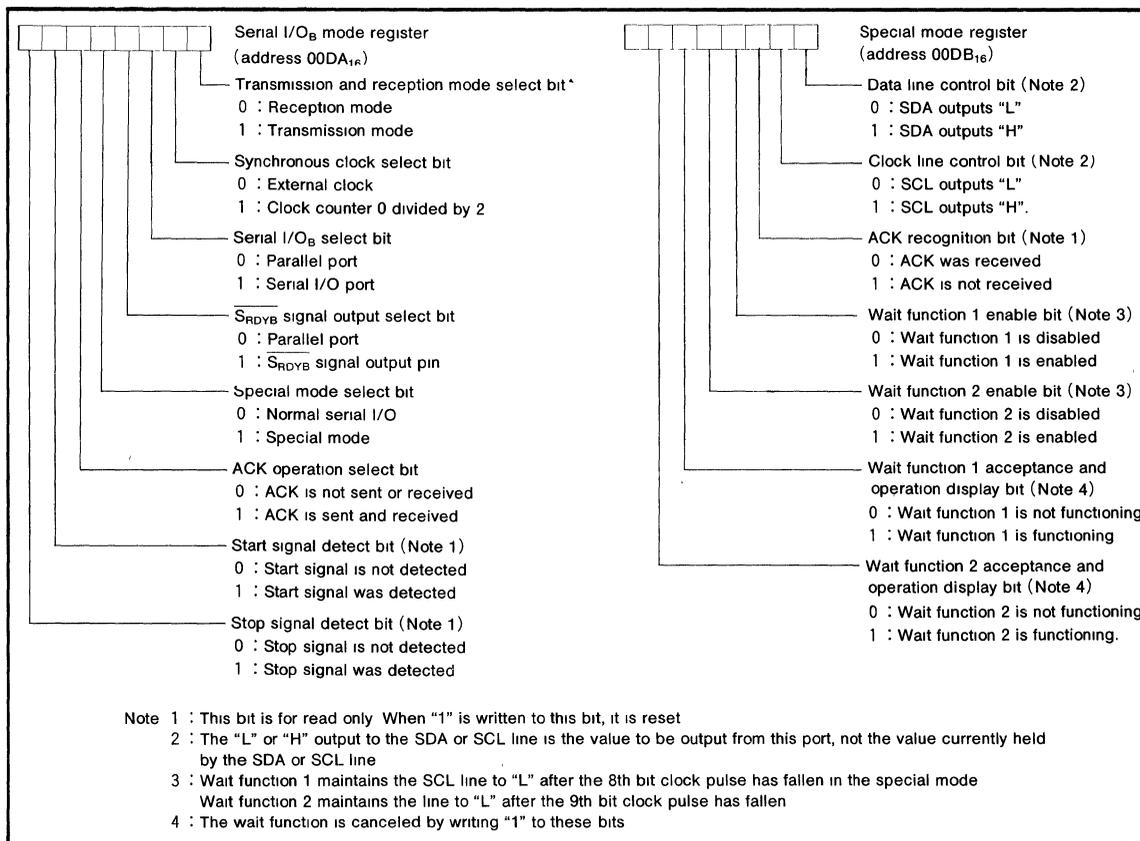


Fig. 13 Structure of registers related to serial I/O_B

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PWM OUTPUT CIRCUIT

(1) Introduction

The M37100M8-XXXSP is equipped with one 14-bit PWM and four 6-bit PWMs. The 14-bit resolution gives PWM1 the minimum resolution bit width of 500ns (for $X_{IN} = 4\text{MHz}$) and a repeat period of $8192\mu\text{s}$. PWM2, PWM3, PWM4 and PWM5 have a 6-bit resolution with minimum resolution bit width of $16\mu\text{s}$ and repeat period of $1024\mu\text{s}$. Accuracy and operation range is certified of PWM are $V_{CC} = 4.5$ to 5.5V regardless of input-frequency.

Block diagram of the PWM is shown in Figures 14.

The PWM timing generator section applies individual control signals to PWM1-PWM5, using clock input X_{IN} divided by 2 or X_{CIN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM1, PWM2, PWM3, PWM4 and PWM5 are in common with pins P6₁, P6₂, P6₃, P6₄ and P6₅ of port P6 (i.e. for PWM output, PWM output selection bits and the P6 directional register D6₁-D6₅ should be set). When PWM1 is used for output, first set the higher 8-bit of the PWM1-H register (address 00F0₁₆), then the lower 6-bit of the PWM1-L register (address 00F1₁₆). When one of the PWM2-PWM5 is used for output, set the 6-bit in the PWM2-PWM5 register, respectively. Note that the higher 2 bits of these 8-bit registers are ignored when used 6-bit register.

(3) Transferring data from registers to latches

The data written to the 6-bit PWM register is transferred to the PWM latch in each 6-bit PWM cycle period. For 14-bit PWM, the data is transferred in the next upper 8-bit period after the write. The signals output to the PWM pins correspond to the contents of these latches. When data at addresses 00F0₁₆ to 00F4₁₆ and 00F8₁₆ is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. When the 6-bit latch is being read, the upper 2 bits of the register becomes undefined. However, bit 7 of the PWM1-L register indicated the completion of the data transfer from the PWM1 register to the PWM1 latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 6-bit PWMs

The timing diagram of the two 6-bit PWMs (PWM2-PWM5) is shown in Figure 15. One period (T) is composed of 64 (2⁶) segments.

There are six different pulse types configured from bits 0 to 5 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 15 (a).

Six different pulses can be output from the PWM. These can be selected by bits 0 through 5. Depending on the content of the 6-bit PWM latch, pulses from 5 to 0 is selected. The PWM output is the difference of the

sum of each of these pulses. Several examples are shown in Figure 15 (b). Changes in the contents of the PWM latch allows the selection of 64 lengths of high-level area outputs varying from 0/64 to 63/64. An length of entirely high-level output cannot be output, i.e. 64/64.

(5) 14-bit PWM operation

The timing diagram of the 14-bit PWM1 is shown in Figure 16. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length N timers τ is output every short area of $t = 256 \tau = 128\mu\text{s}$ as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 16.)

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that puls τ . As a result, the short-area period t ($= 128\mu\text{s}$, approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data	Area longer by τ than that of other t_m ($m = 0$ to 63)
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m = 32$
0 0 0 0 1 0	$m = 16, 48$
0 0 0 1 0 0	$m = 8, 24, 40, 56$
0 0 1 0 0 0	$m = 4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m = 1, 3, 5, 7, \dots, 57, 59, 61, 63$

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M37100M8-XXXSP/FP

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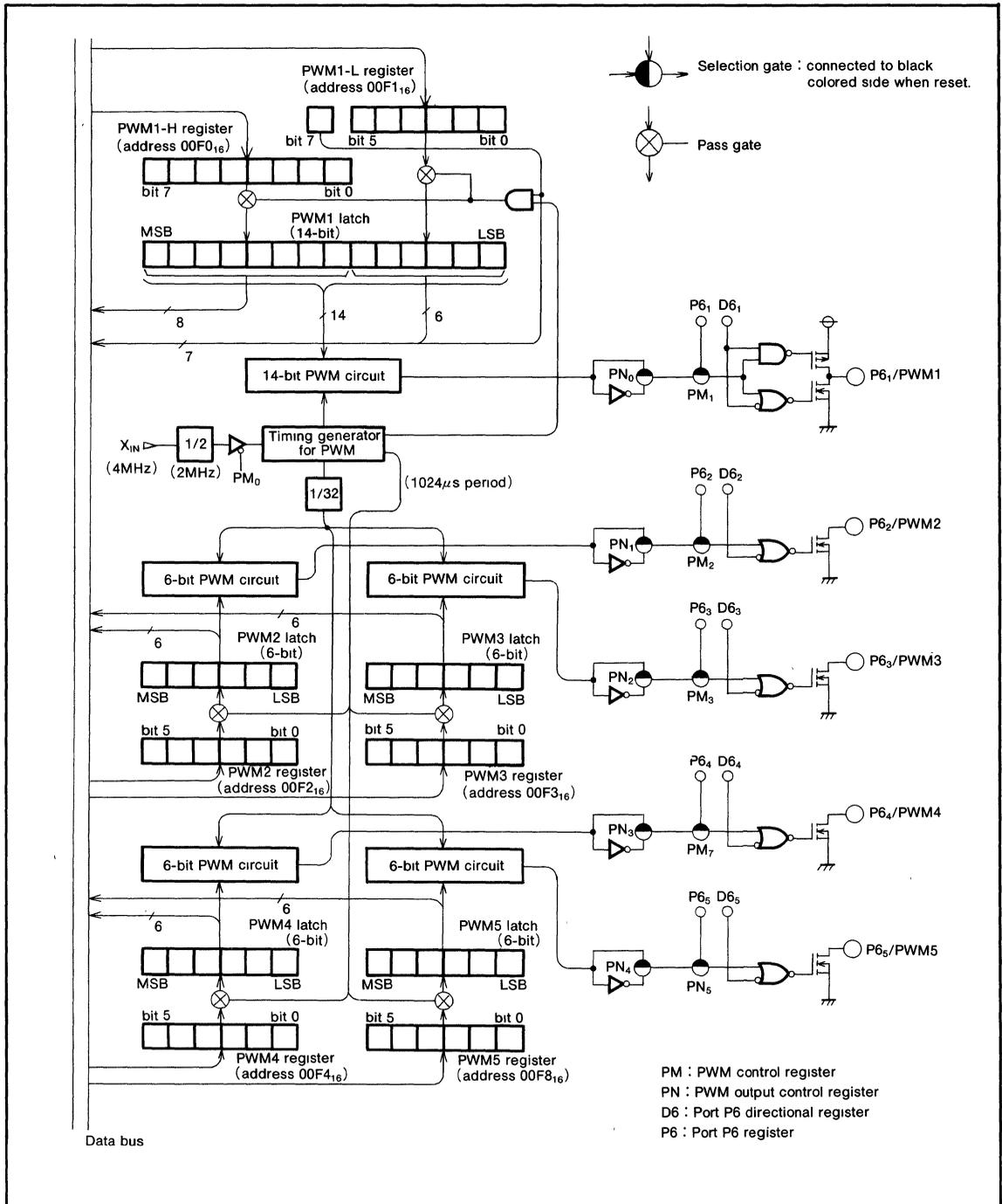


Fig. 14 Block diagram of the PWM circuit

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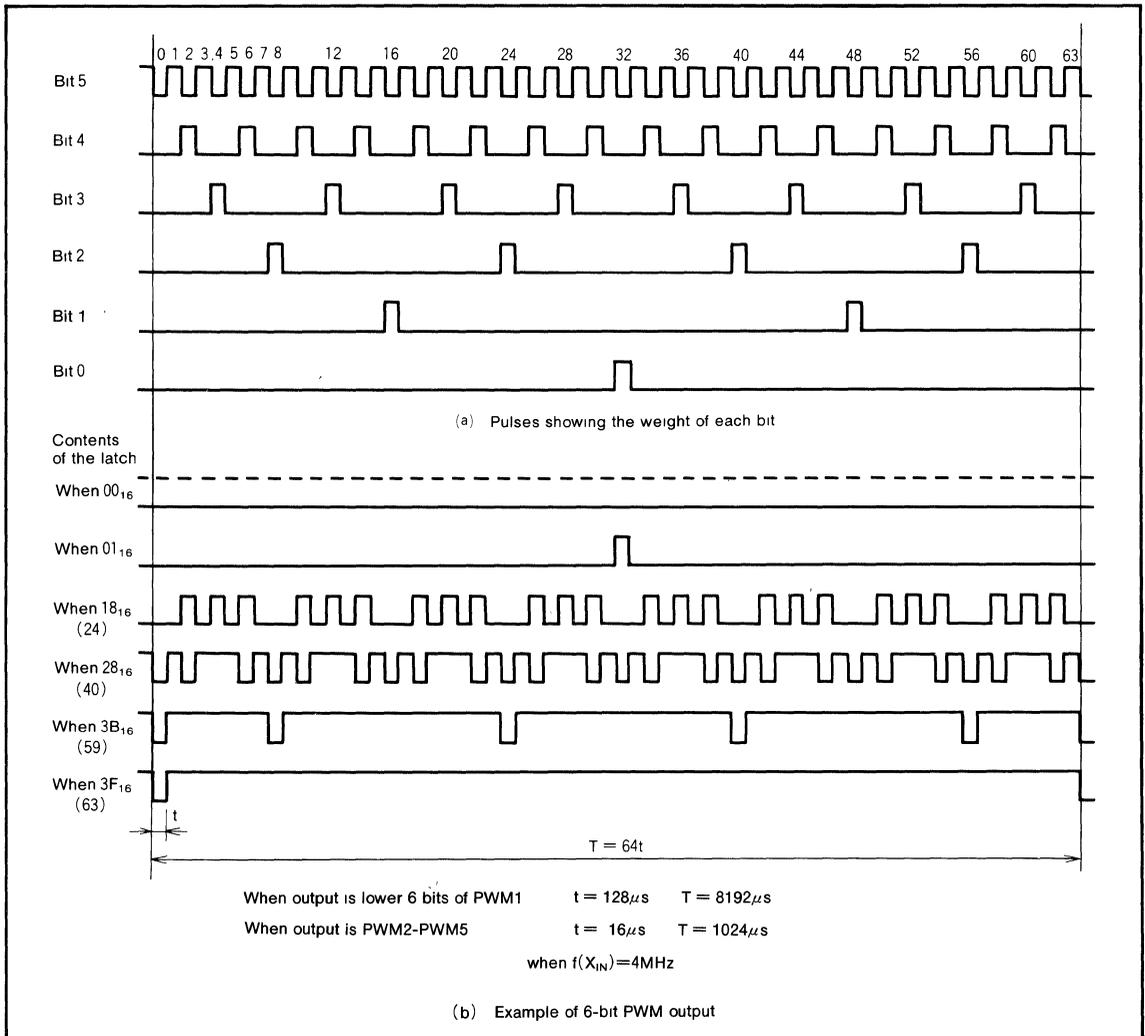


Fig. 15 6-bit PWM timing diagram

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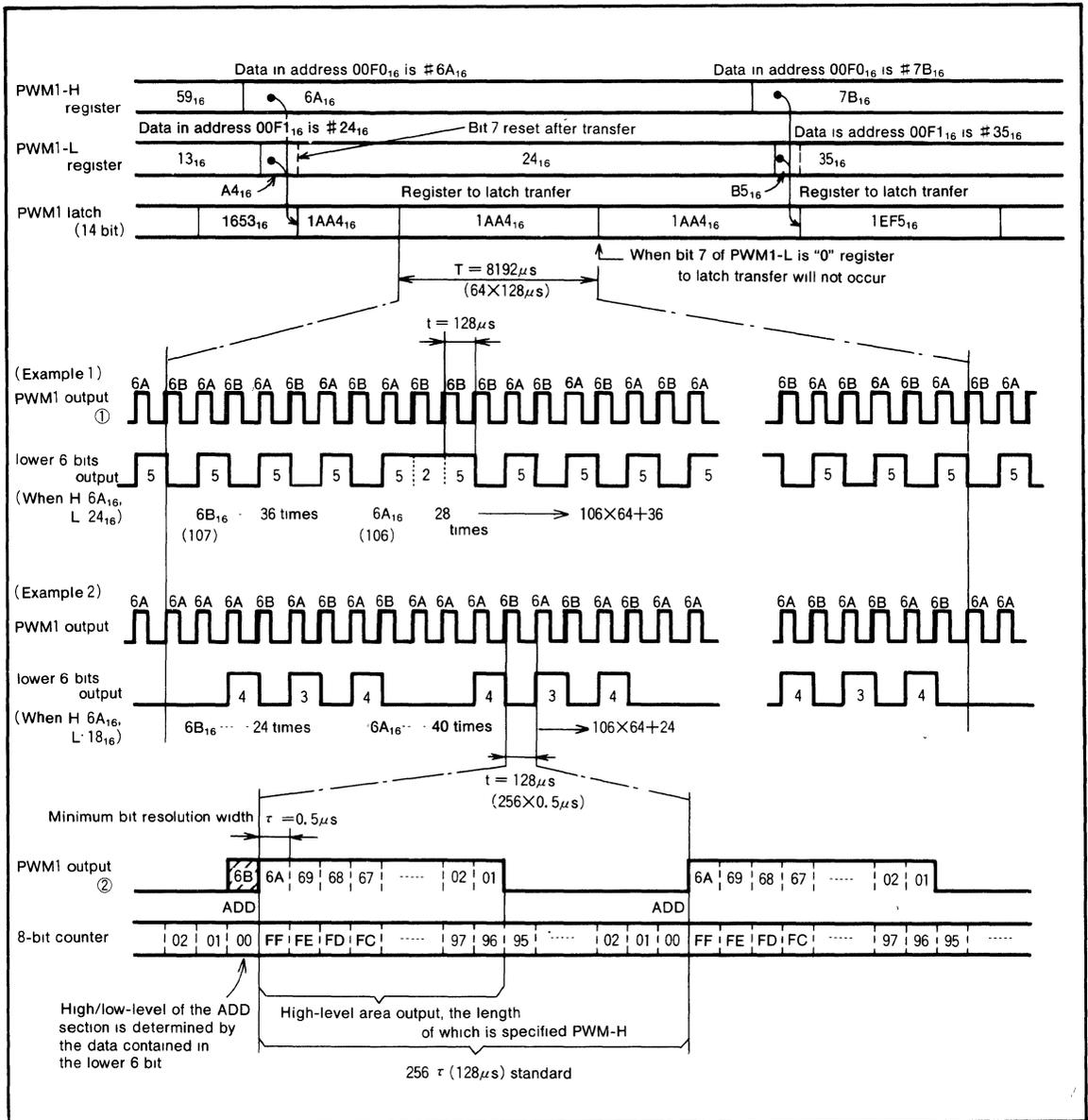


Fig. 16 14-bit PWM timing diagram

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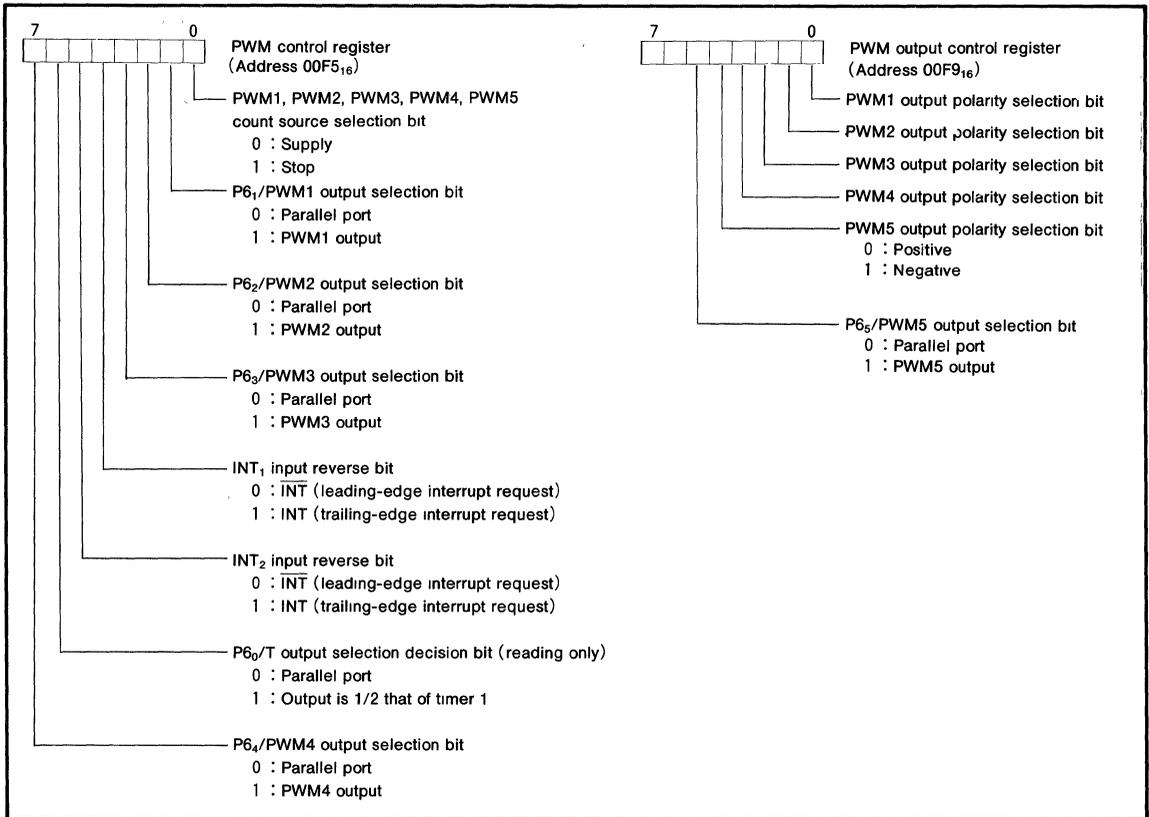


Fig. 17 Structure of registers related to PWM

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PORT P6₀ / TIMER 1 OUTPUT

Bit 0 of port P6 outputs 1/2 the frequency of timer 1 when bit 4 (SM₄) of the serial I/O_A mode register (address 00F6₁₆) is set to "1". The output switching can be accomplished with either of two procedures, synchronous mode or asynchronous mode, depending on the setting of bit 5 (SM₅) of the serial I/O_A mode register.

When SM₅ is set to "0" the synchronous mode is set. In such a case, after SM₄ has been changed, synchronization is set to the 1/2 frequency of timer 1 and switching between the port latch and timer takes place. It is possible to ascertain whether switching actually occurred by reading the value of bit 6 of the PWM control register.

From the time that the contents of SM₄ was changed to the point where switching completes, the contents of neither SM₄ nor P6₀ may be changed. Use of the synchronous mode prevents the generation of a pulse shorter than the timer output during switching. Figure 18 (a) gives an example of timing in the synchronous mode. Use of the synchronous mode allows generation of an EAROM clock input signal through the use of a simple program.

When SM₅ is set to "1", the asynchronous mode is set. In this case, the output switching occurs directly after SM₄ has been changed. Figure 18 (b) gives an example of timing in the asynchronous mode.

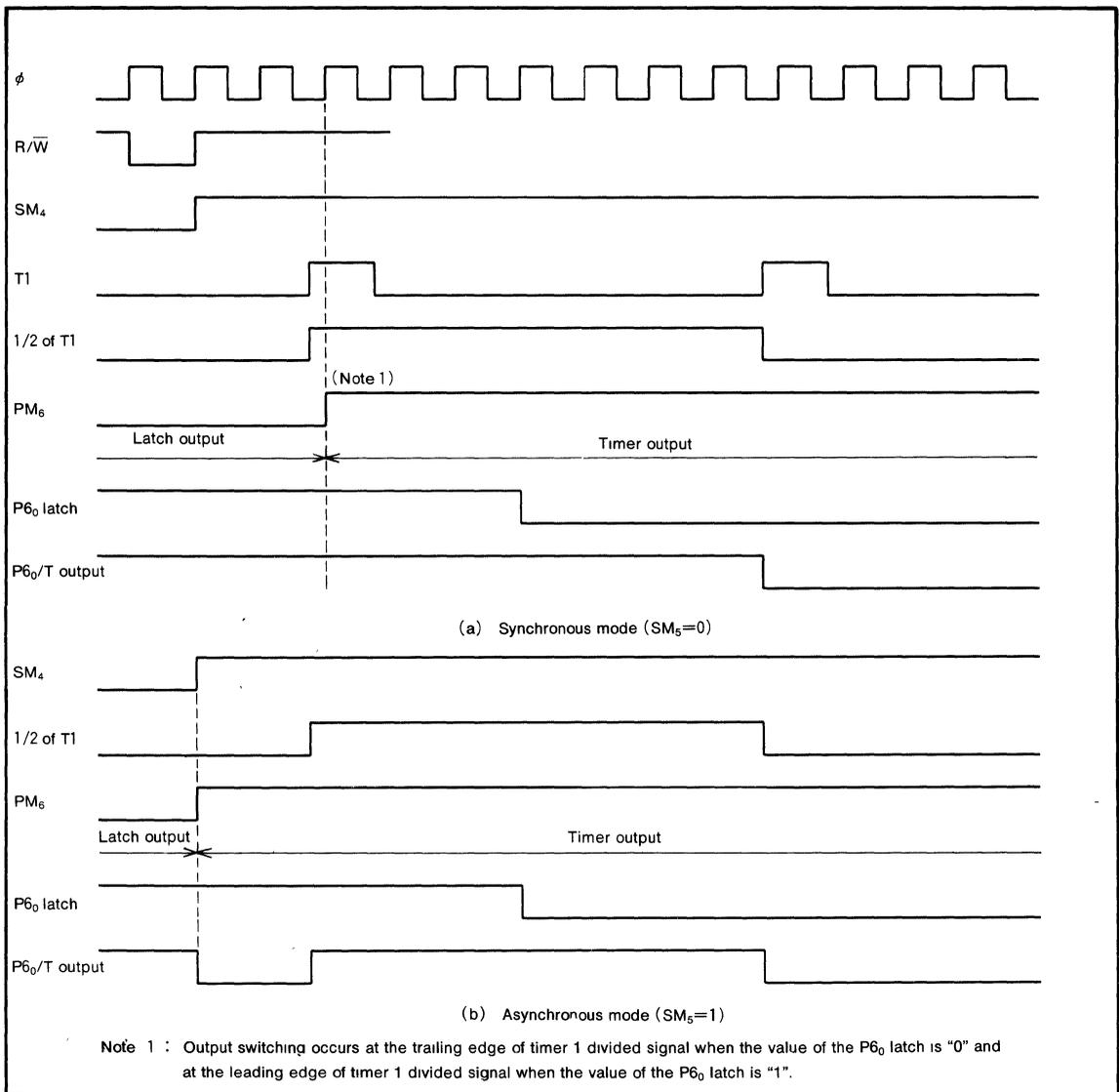


Fig. 18 P6₀/T switching timing diagram

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COMPARATOR CIRCUIT

The comparator circuit is shown in Figure 19. The comparator circuit consists of the switch tree, ladder resistor, comparator, comparator control circuit, A-D control register (address 00E7₁₆), and analog signal input pin (P3₃/A-D). The analog input pin is common with the digital input/output terminal to the data bus.

The 5-bit A-D control register can generate 1/16V_{CC}-step internal analog voltage, based on the settings of bits 0 to 3. Table 3 gives the relation between the descriptions of A-D control register bits 0 to 3 and the generated internal analog voltage. The comparator result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 4.

Bit 4 is "1" when analog input voltage > internal analog voltage and "0" when analog input voltage < internal analog voltage. When voltage is compared to by setting bits 0 to 3 of the comparator register "0", bit 4 of the A-D control register becomes "1" regardless of the analog input voltage.

Table 3. Relationship between the contents of A-D control register and internal voltage

A-D control register				Internal analog voltage
bit 3	bit 2	bit 1	bit 0	
0	0	0	1	1/16V _{CC} -1/32V _{CC}
0	0	1	0	2/16V _{CC} -1/32V _{CC}
0	0	1	1	3/16V _{CC} -1/32V _{CC}
0	1	0	0	4/16V _{CC} -1/32V _{CC}
0	1	0	1	5/16V _{CC} -1/32V _{CC}
0	1	1	0	6/16V _{CC} -1/32V _{CC}
0	1	1	1	7/16V _{CC} -1/32V _{CC}
1	0	0	0	8/16V _{CC} -1/32V _{CC}
1	0	0	1	9/16V _{CC} -1/32V _{CC}
1	0	1	0	10/16V _{CC} -1/32V _{CC}
1	0	1	1	11/16V _{CC} -1/32V _{CC}
1	1	0	0	12/16V _{CC} -1/32V _{CC}
1	1	0	1	13/16V _{CC} -1/32V _{CC}
1	1	1	0	14/16V _{CC} -1/32V _{CC}
1	1	1	1	15/16V _{CC} -1/32V _{CC}

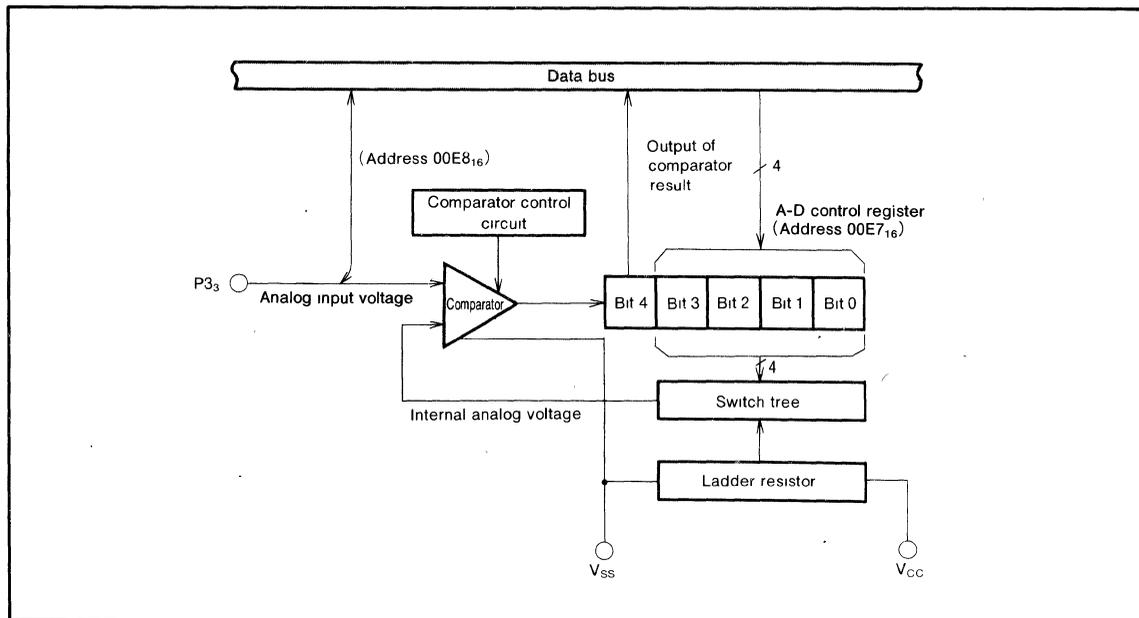


Fig. 19 Comparator Circuit

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 4 outlines the CRT display functions. The M37100M8-XXXSP incorporates a 21 columns \times 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 96 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12 \times 16 dot configuration to obtain smooth character patterns. (See Figure 20)

The following shows the procedure how to display characters on the CRT screen.

- ① Set the character to be displayed in display RAM.
- ② Set the display color by using the color register.
- ③ Specify the color register in which the display color is set by using the display RAM.
- ④ Specify the vertical position and character size by using the vertical position register.
- ⑤ Specify the horizontal position by using the horizontal position register.
- ⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

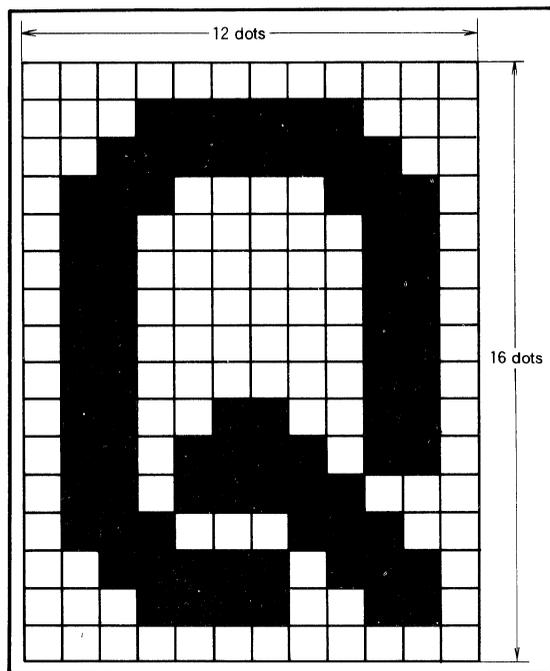


Fig. 20 CRT display character configuration

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 3 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 22 shows a block diagram of the CRT display control circuit. Figure 21 shows the structure of the CRT display control register.

Table 4. Outline of CRT display functions

Parameter		Functions
Number of display character		21 characters \times 3 lines
Character configuration		12 \times 16 dots (See Figure 20)
Kinds of character		96
Character size		4 size selectable
Color	Kinds of color	15 (max)
	Coloring unit	a character
Display expansion		Possible (multiple lines)

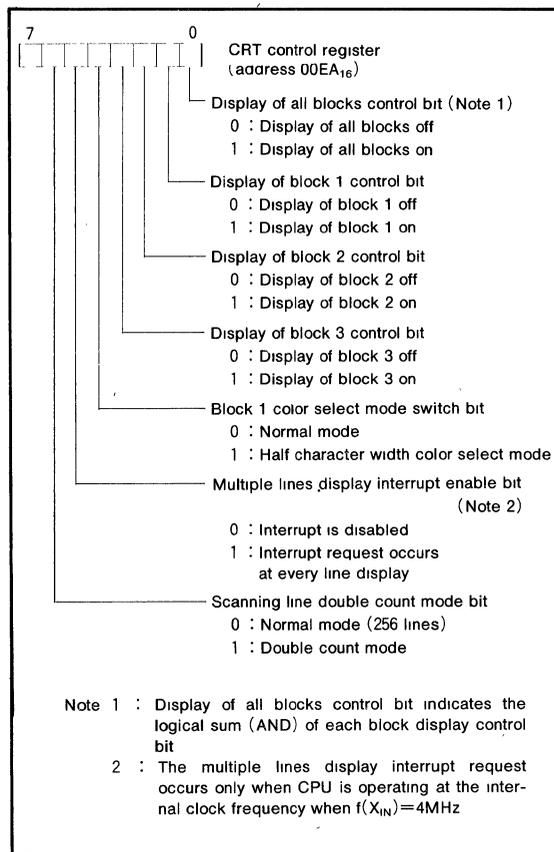


Fig. 21 Structure of CRT control register

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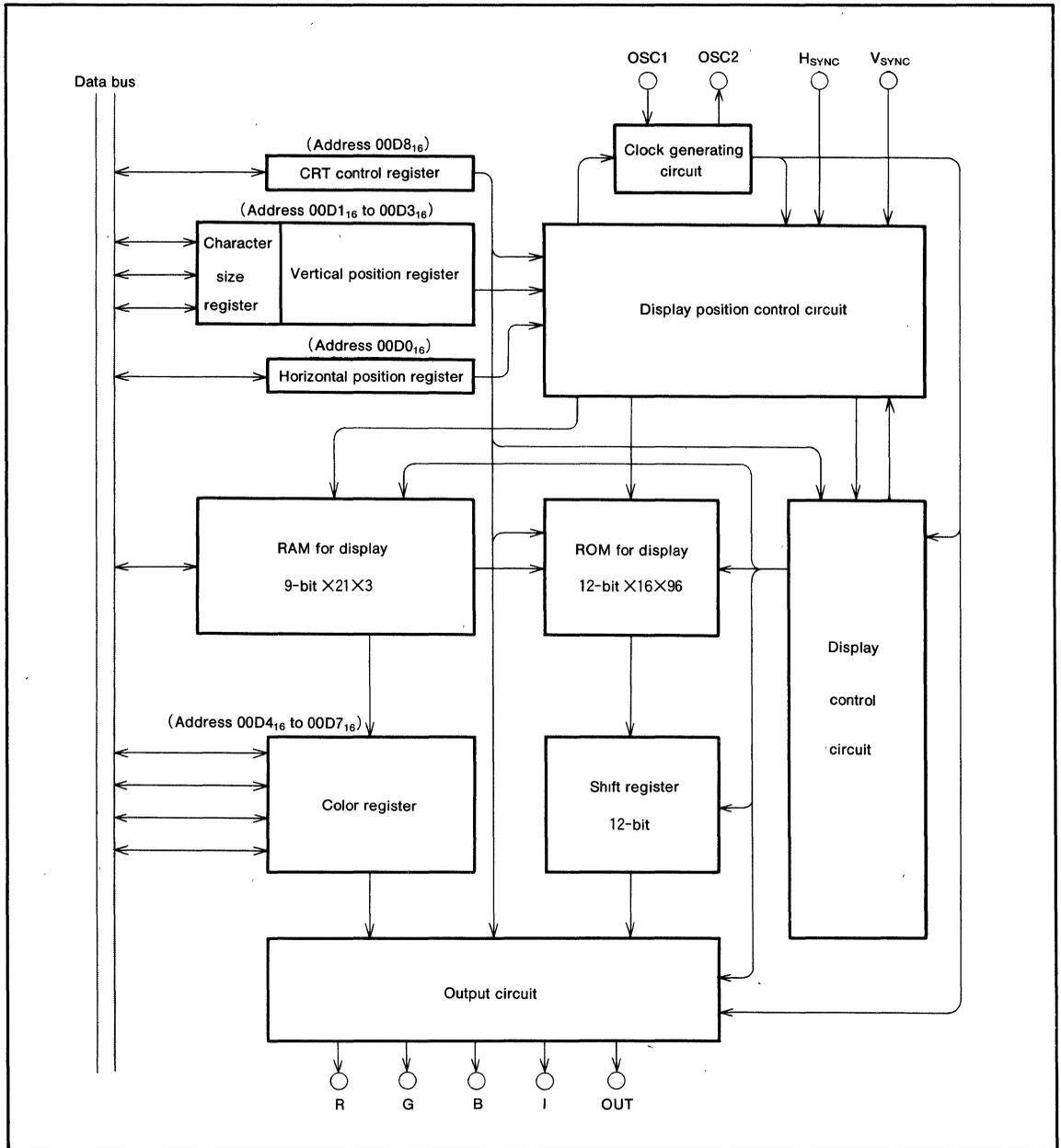


Fig. 22 Block diagram of CRT display control circuit

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(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 21 characters can be displayed in one block. (See (4) RAM for Display.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of $4T_c$ (T_c = oscillation cycle for display).

The display position in the vertical direction is selected from 64-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 25), a block of the smaller block No. (1 to 3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 25), the former block is overridden and the latter is displayed.

The vertical position can be specified from 64-step positions (four scanning lines per step) for each block by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the vertical position register (addresses $00D1_{16}$ to $00D3_{16}$). Figure 23 shows the structure of the vertical position register.

The horizontal direction is common to all blocks, and can be specified from 64-step display positions ($4T_c$ per step (T_c = oscillation cycle for display)) by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the horizontal position register (address $00D0_{16}$).

Figure 24 shows the structure of the horizontal position register.

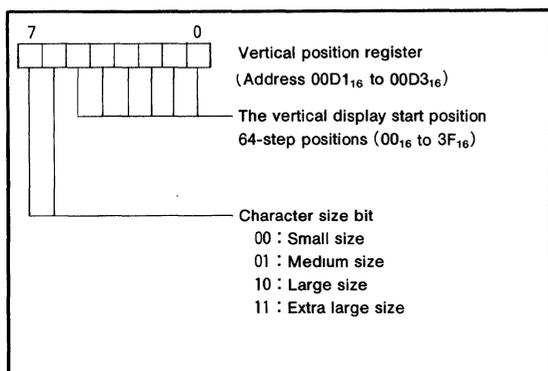


Fig. 23 Structure of vertical position registers

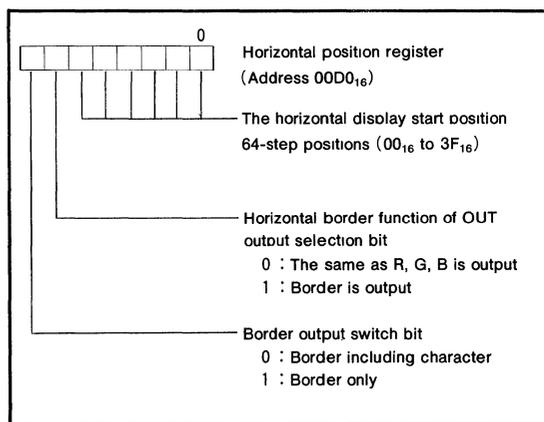
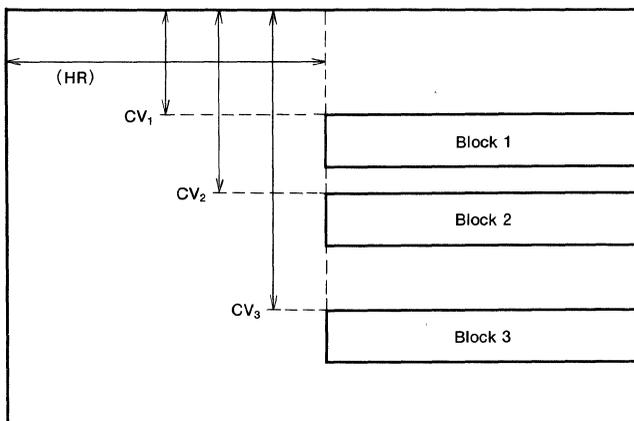
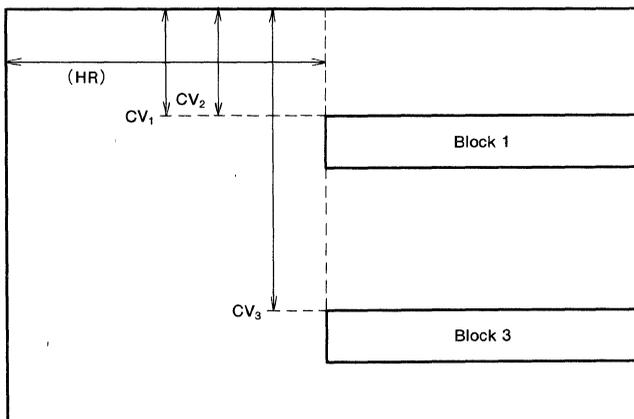


Fig. 24 Structure of horizontal position register

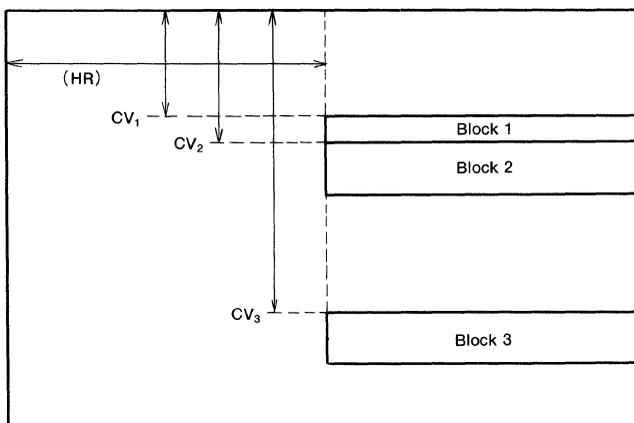
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(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed.

Fig. 25 Display position

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(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the bit 6 and 7 of vertical position register to set a character size.

The character size can be selected from four sizes: small size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display

oscillation ($=T_c$) in the width (horizontal) direction.

The small size consists of [one scanning line] \times [1 T_c]; the medium size consists of [two scanning lines] \times [2 T_c]; the large size consists of [three scanning lines] \times [3 T_c]; and the extra large size consists of [four scanning lines] \times [4 T_c]. Table 5 shows the relationship between the set values in the character size register and the character sizes.

Table 5. The relationship between the set values of the character size bits and the character sizes

Set values of the character size bits		Character size	Width (horizontal) direction	Height (vertical) direction
Bit 7	Bit 6			
0	0	Small	1 T_c	1
0	1	Medium	2 T_c	2
1	0	Large	3 T_c	3
1	1	Extra large	4 T_c	4

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal start position is common to all blocks even when the character size varies with each block. (See Figure 26)

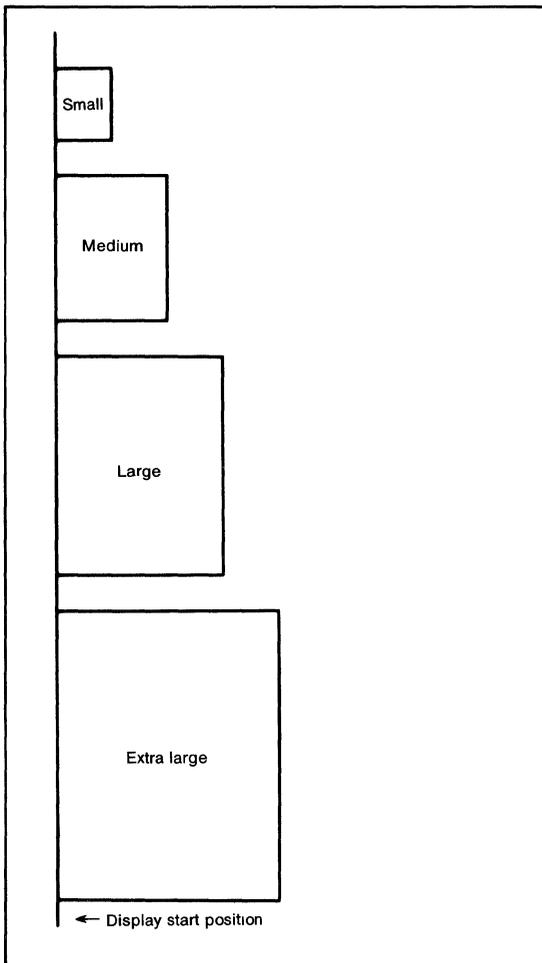


Fig. 26 Display start position of each character size (horizontal direction)

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(4) RAM for Display

The CRT display RAM is allocated at addresses 2000₁₆ to 20D4₁₆, and is divided into a display character code specifying part and display color specifying part for each block.

Table 6 shows the contents of the CRT display RAM.

When a character is to be display at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0 to 6) in address 2000₁₆ and the color register No. to the two low-order bits (bits 0 and 1) in address 2080₁₆. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 27.

Table 6. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1 st Column	2000 ₁₆	2080 ₁₆
	2 nd Column	2001 ₁₆	2081 ₁₆
	3 rd Column	2002 ₁₆	2082 ₁₆
	⋮	⋮	⋮
	19th Column	2012 ₁₆	2092 ₁₆
	20th Column	2013 ₁₆	2093 ₁₆
	21th Column	2014 ₁₆	2094 ₁₆
Not used		2015 ₁₆ to 201F ₁₆	2095 ₁₆ to 209F ₁₆
Block 2	1 st Column	2020 ₁₆	20A0 ₁₆
	2 nd Column	2021 ₁₆	20A1 ₁₆
	3 rd Column	2022 ₁₆	20A2 ₁₆
	⋮	⋮	⋮
	19th Column	2032 ₁₆	20B2 ₁₆
	20th Column	2033 ₁₆	20B3 ₁₆
	21th Column	2034 ₁₆	20B4 ₁₆
Not used		2035 ₁₆ to 203F ₁₆	20B5 ₁₆ to 20BF ₁₆
Block 3	1 st Column	2040 ₁₆	20C0 ₁₆
	2 nd Column	2041 ₁₆	20C1 ₁₆
	3 rd Column	2042 ₁₆	20C2 ₁₆
	⋮	⋮	⋮
	19th Column	2052 ₁₆	20D2 ₁₆
	20th Column	2053 ₁₆	20D3 ₁₆
	21th Column	2054 ₁₆	20D4 ₁₆
Not used		2055 ₁₆ to 207F ₁₆	

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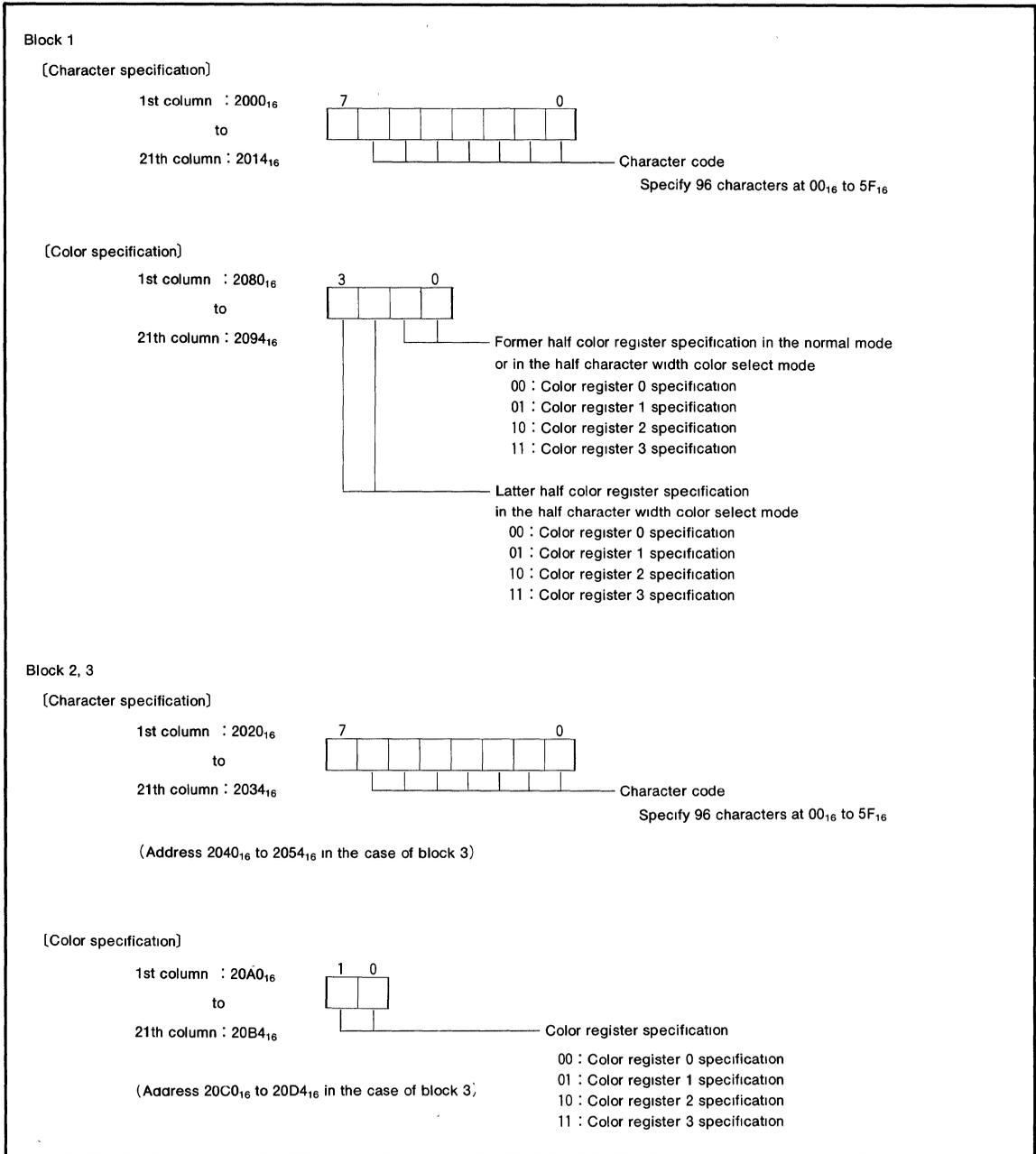


Fig. 27 Structure of the CRT display RAM

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(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3: addresses 00D4₁₆ to 00D7₁₆) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set $2^4 - 1$ (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 28 shows the structure of the color register.

(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address 00D8₁₆) it is possible to specify colors in units of a half character size (vertical 16 dots X horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

- ① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080₁₆ to 2094₁₆).
- ② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080₁₆ to 2094₁₆).

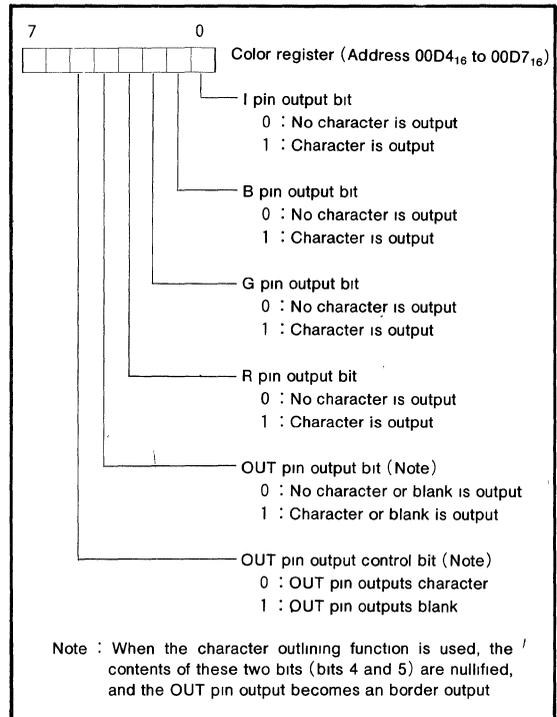


Fig. 28 Structure of color registers

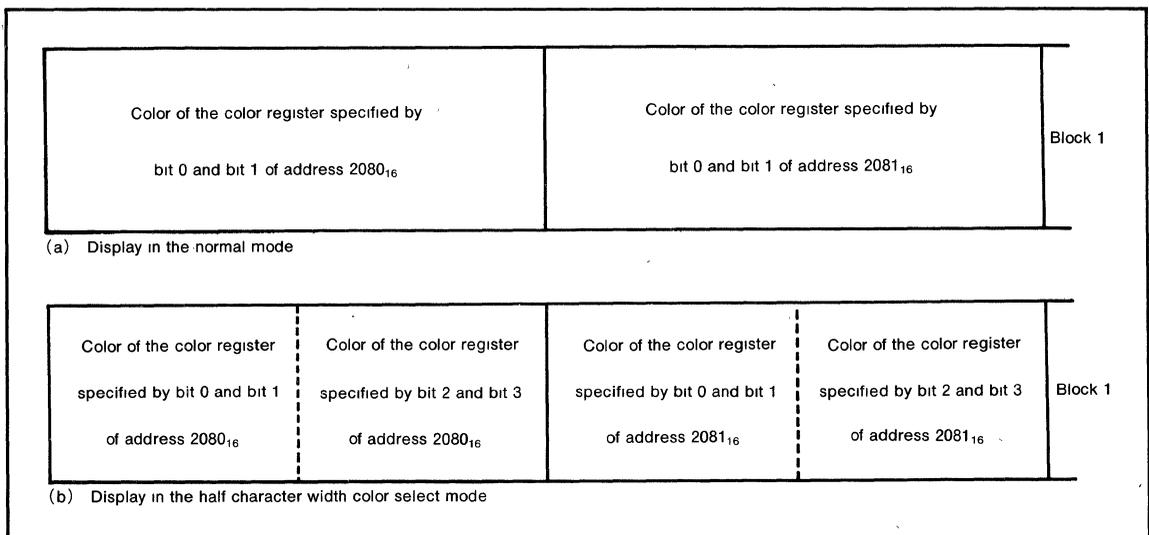


Fig. 29 Difference between normal color select mode and half character width color select mode

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(7) Multiline Display

The M37100M8-XXXSP can normally display three lines on the CRT screen by displaying three blocks at different vertical positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (bit 6 at address 00FE₁₆) to "1"), then execute the following processing in the CRT interrupt handling routine.

- ① Read the value of the display block counter.
- ② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.
- ③ Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and vertical display position (contents of vertical position register) to be displayed next.

Figure 30 shows the structure of the display block counter.

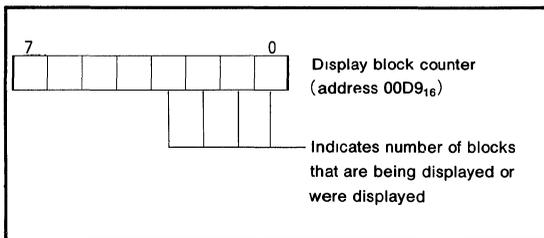


Fig. 30 Structure of display block counter

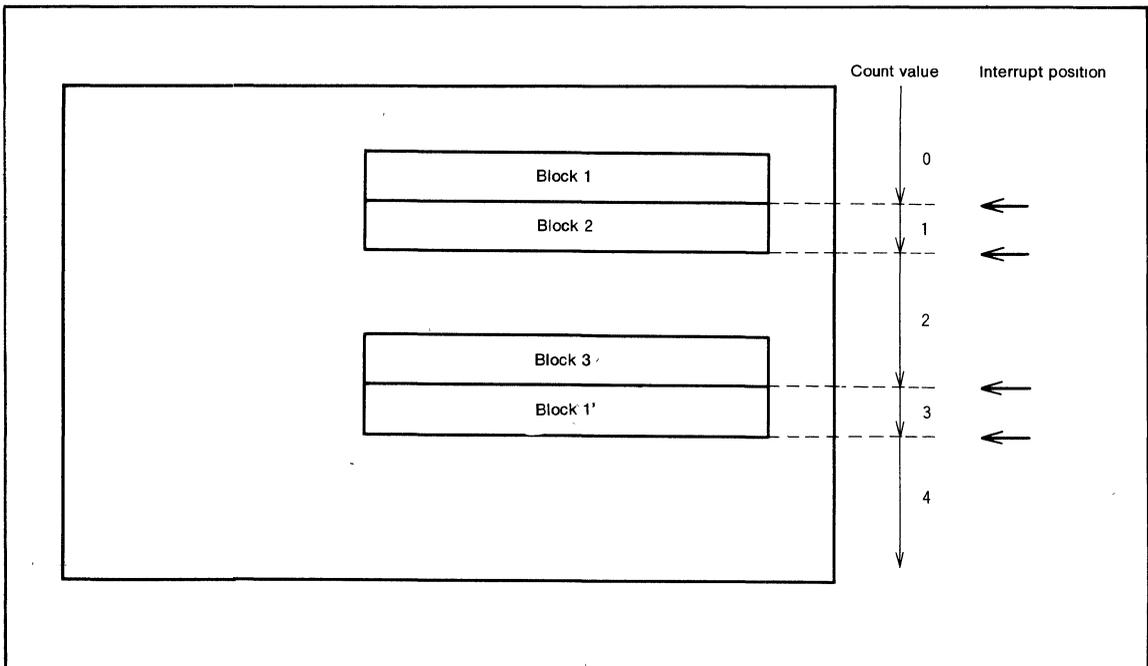


Fig. 31 Timing of CRT interrupt and count value of display block counter

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(8) Scanning Line Double Count Mode

One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended twofold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 64 steps from 00_{16} to $3F_{16}$, or four scanning lines per step, the number of steps in the scanning line double

count mode is 31 from 00_{16} to $1F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 20_{16} to $3F_{16}$ in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register (address $00D8_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.

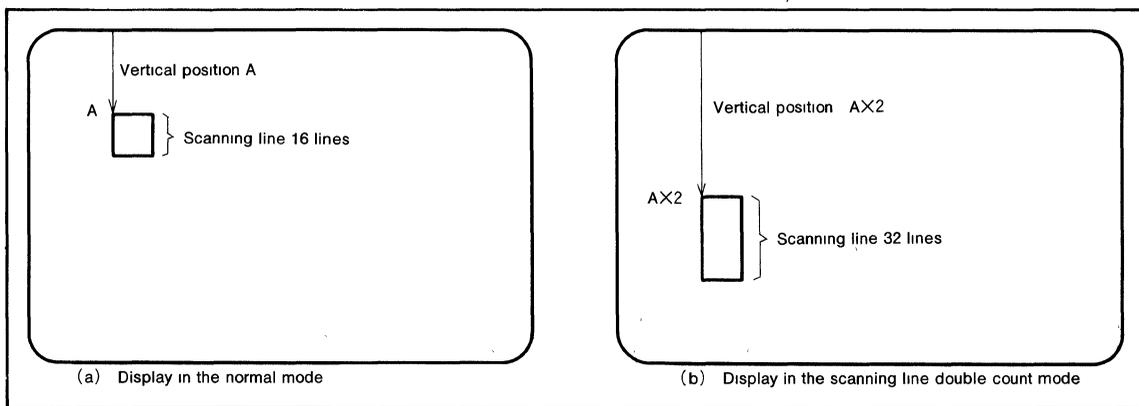


Fig. 32 Display in the normal mode and in the scanning line double count mode

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

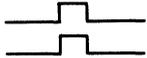
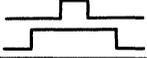
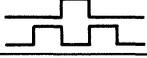
(9) Horizontal Character Border Function

An border of a one clock (one dot) equivalent size can be added to a character to be displayed only horizontal direction.

The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (contents output from the OUT pin) are nullified, and the border is output from the OUT pin instead.

Border can be specified in units of block by using the bit 6 and 7 of horizontal position register. Table 7 shows the relationship between the values set in the horizontal position register and the character border function.

Table 7. The relationship between the value set in the horizontal position register and the character border function

Horizontal position register		Functions	Example of output	
Bit 7	Bit 6			
X	0	Normal	R, G, B, I output OUT output	
0	1	Border including character	R, G, B, I output OUT output	
1	1	Border not including character	R, G, B, I output OUT output	

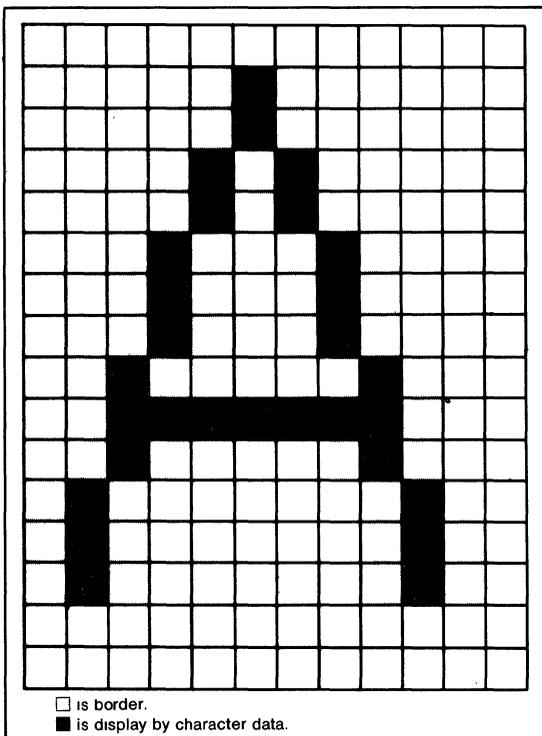


Fig. 33 Example of border

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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(10) Clock Oscillating Circuit for Display

The clock signal for display can be obtained by connecting a resistor and a capacitor between the I/O ports of the oscillating circuit (OSC1 and OSC2). Figure 34 shows an example of circuit.

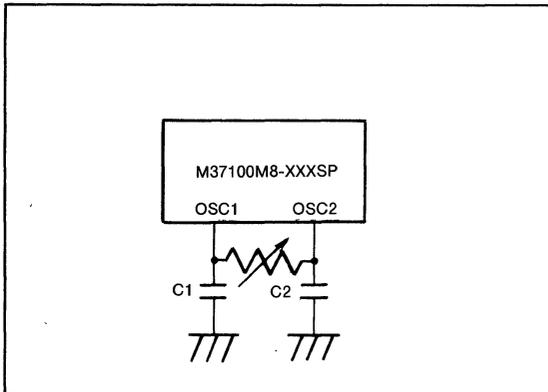


Fig. 34 Example of oscillating circuit for display

(11) Programming Notes

1. Use STA instruction for data transfer to the following registers related to OSD functions.
 - ① Horizontal position register (address 00D0₁₆)
 - ② Vertical position registers (address 00D1₁₆ to 00D3₁₆)
 - ③ Color registers (address 00D4₁₆ to 00D7₁₆)
 - ④ CRT control register (address 00D8₁₆)
2. Do not display the display OFF blocks having different character sizes on a block display
3. The highest vertical position (the vertical display start position bits are "00₁₆") can not be used.
4. The interrupt to tell the end of block display is not caused and the display block counter is not incremented until the display of the block has been completed terminated.
5. The display block counter (00D9₁₆) is reset while V_{SYNC} is "H" (when the option is positive in polarity) to "FF₁₆".
6. If, during the display of a block, the display position of another block comes, the display of the subsequent block (having a larger vertical position register value) is preferred.
7. When two or more blocks are displayed in the same vertical position, the display priority is CV1, CV2, and CV3 in this order. This is not affected by turning on/off of block display.

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RESET CIRCUIT

The M37100 is reset according to the sequence shown in Figure 36. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low

order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than $2\mu\text{s}$ while the power voltage is $5V \pm 10\%$ and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 35.

	Address	
(1) Port P0 directional register	(D0)(E1 ₁₆)	00 ₁₆
(2) Port P1 directional register	(D1)(E3 ₁₆)	00 ₁₆
(3) Port P2 directional register	(D2)(E5 ₁₆)	00 ₁₆
(4) Port P3 directional register	(D3)(E9 ₁₆)	00 ₁₆
(5) Port P4 directional register	(D4)(EB ₁₆)	0
(6) Port P5 directional register	(D5)(ED ₁₆)	00000000
(7) Port P6 directional register	(D6)(EF ₁₆)	00000000
(8) PWM control register	(PM)(F5 ₁₆)	00 ₁₆
(9) Serial I/O _A mode register	(SM)(F6 ₁₆)	00 ₁₆
(10) PWM output control register	(PN)(F9 ₁₆)	00000000
(11) Interrupt control register 2	(IN)(FB ₁₆)	00
(12) Timer 2	(T2)(FC ₁₆)	FF ₁₆
(13) Timer 3	(T3)(FD ₁₆)	07 ₁₆
(14) Interrupt control register 1	(IM)(FE ₁₆)	00 ₁₆
(15) Timer control register	(TM)(FF ₁₆)	00 ₁₆
(16) Processor status register	(PS)	1
(17) Program counter	(PC _H)	Contents of address FFFF ₁₆
	(PC _L)	Contents of address FFFE ₁₆
(18) Horizontal location register	(HR)(D0 ₁₆)	00 ₁₆
(19) Color register 0	(C0)(D4 ₁₆)	00000000
(20) Color register 1	(C1)(D5 ₁₆)	00000000
(21) Color register 2	(C2)(D6 ₁₆)	00000000
(22) Color register 3	(C3)(D7 ₁₆)	00000000
(23) Display control register	(CC)(D8 ₁₆)	00000000
(24) Serial I/O _B mode register	(SB)(DA ₁₆)	00 ₁₆
(25) Special mode register	(SC)(DB ₁₆)	00000000
(26) Counter 0	(DD ₁₆)	FF ₁₆

Note Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values

Fig. 35 Internal state of microcomputer at reset

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M37100M8-XXXSP/FP

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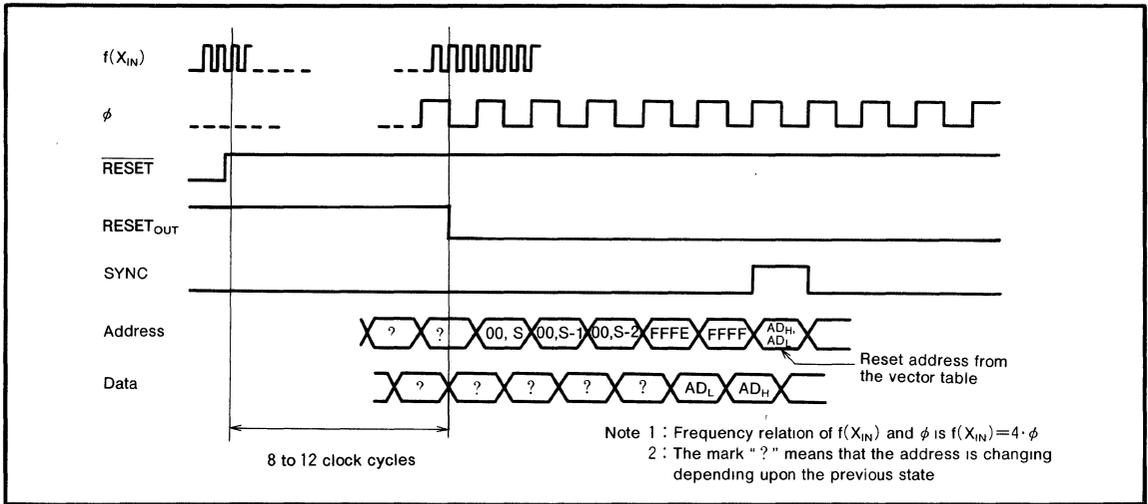


Fig. 36 Timing diagram at reset

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain and middle voltage output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address 00E0₁₆.

Port P0 has a directional register (address 00E1₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address 00FF₁₆), three different modes can be selected; single-chip mode, eva-chip mode and microprocessor mode.

In these modes it functions as address (A₇-A₀) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0 but the output structure is not middle voltage. It can be built in pull-up register at each pin by selecting the option. In other modes, it functions as address (A₁₅-A₈) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P1. In other modes, it functions as data (D₀-D₇) input/output port.

Refer to the section on processor modes for details.

(4) Port P3

In single-chip mode, port P3 has the same function as port P1. P₃₂-P₃₇ have program selectable dual functions. P₃₀, P₃₁ function as control signals input/output port except in the single-chip mode. Refer to the section on processor modes for details.

(5) Port P4

This is an 1-bit I/O port with function similar to port P0, but the output structure is CMOS output.

This port is unaffected by the processor mode bits.

(6) Port P5

This is an 7-bit I/O port with function similar to port P1. P₅₄-P₅₇ have program selectable dual functions. P₅₂, P₅₃ are shared with external interrupt input pins (INT₁, INT₂)

This port is unaffected by the processor mode bits.

(7) Port P6

This is an 6-bit input/output port with function similar to port P0. The output structure of P₆₀, P₆₁ is CMOS output and the output structure of P₆₂-P₆₅ is N-channel open drain and middle voltage.

P₆₀-P₆₅ have program selectable dual functions.

This port is unaffected by the processor mode bits.

(8) Function pins for CRT display function

The horizontal synchronizing signal is input from H_{SYNC}. The vertical synchronizing signal is input from V_{SYNC}.

I, B, G, R, OUT are output pins for CRT display.

Refer to the section on CRT display functions for details.

(9) ϕ pin.

The internal system clock (1/4 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) can be output from this pin by selecting the option

At low-speed mode, X_{CIN} divided by 2 is output from this pin.

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

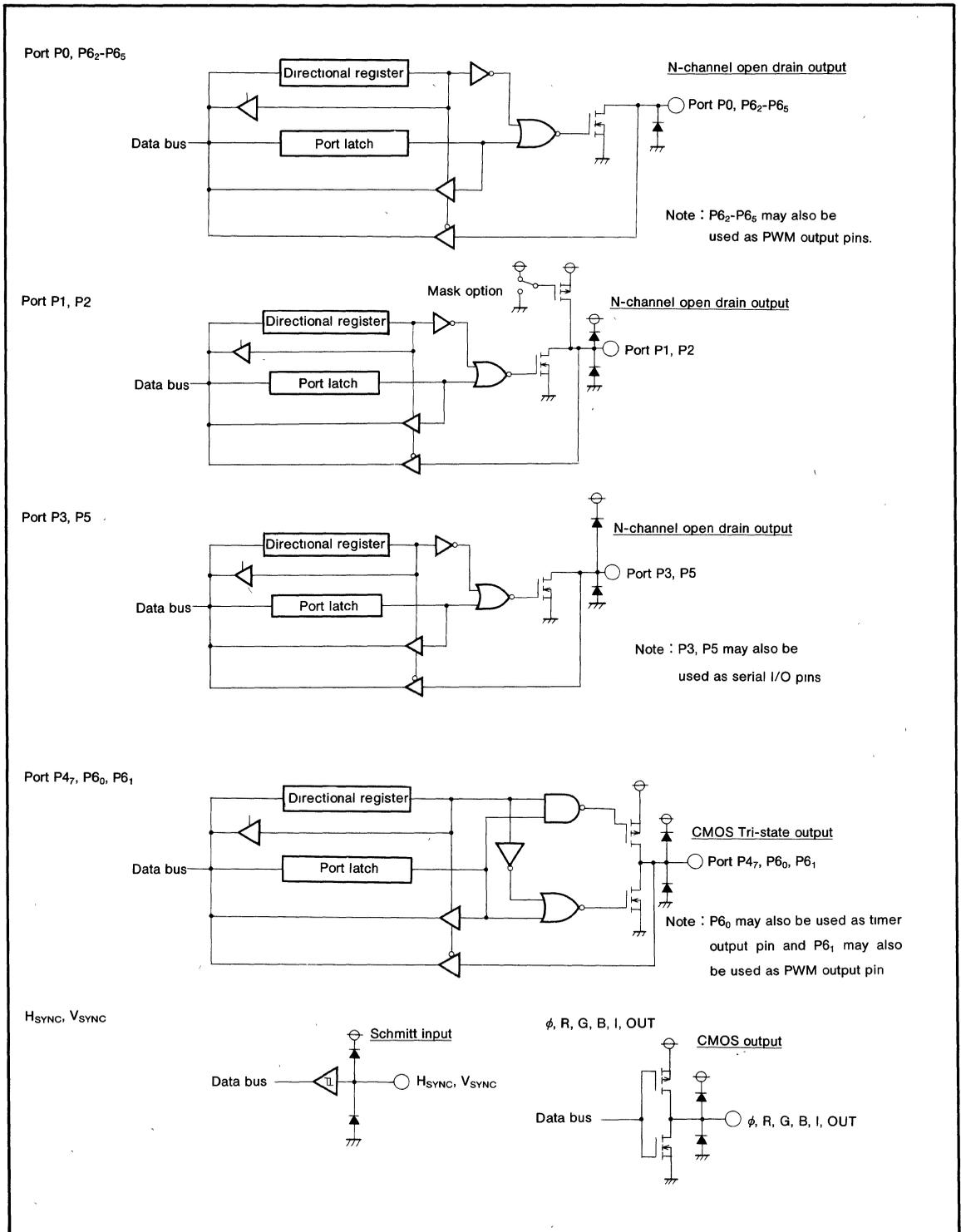


Fig. 37 Ports P0-P6, H_{SYNC}, V_{SYNC}, φ, R, G, B, I and OUT block diagram

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address 00FF₁₆), three different operation modes can be selected; single-chip mode, microprocessor mode and evaluation chip (eva-chip) mode. In the microprocessor mode and eva-chip mode, ports P0-P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 39 shows the functions of ports P0-P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 38.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The three different modes are explained as follows:

- (1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0-P3 will work as original I/O ports.
- (2) Microprocessor mode [01]
The microcomputer will be placed in the microprocessor mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01".
In this mode, the internal ROM is inhibited so the external memory is required.
In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D₇-D₀) and loses its normal output functions. Port P3₁ and P3₀ become the SYNC and R/W pins, respectively and the normal I/O functions are lost.

- (3) Eva-chip mode [11]
When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode.
In this mode, the internal ROM is inhibited so the external memory is required.
The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original output functions.
Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original output functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D₇-D₀ (including instruction code) while at the "L" state. Pins P3₁ and P3₀ output the SYNC and R/W control signals, respectively while ϕ is in the "H" state. When in the "L" state, P3₁ and P3₀ retain their original I/O function.

The R/W output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data. The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 8.

Note : The standards of M37100M8-XXXSP/FP is assured only in single-chip mode. Use in the microprocessor mode or the eva-chip mode only at program development.

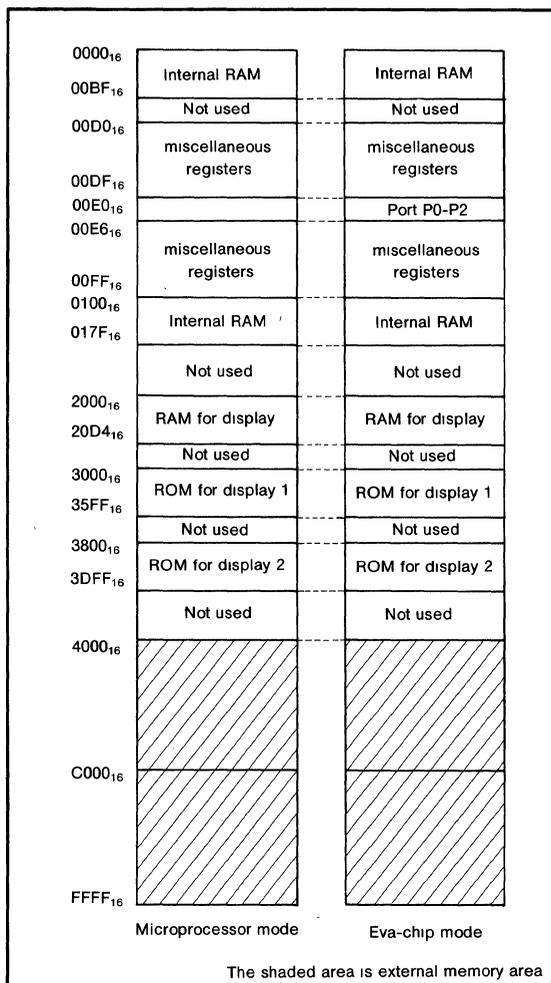


Fig. 38 External memory area in processor mode

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

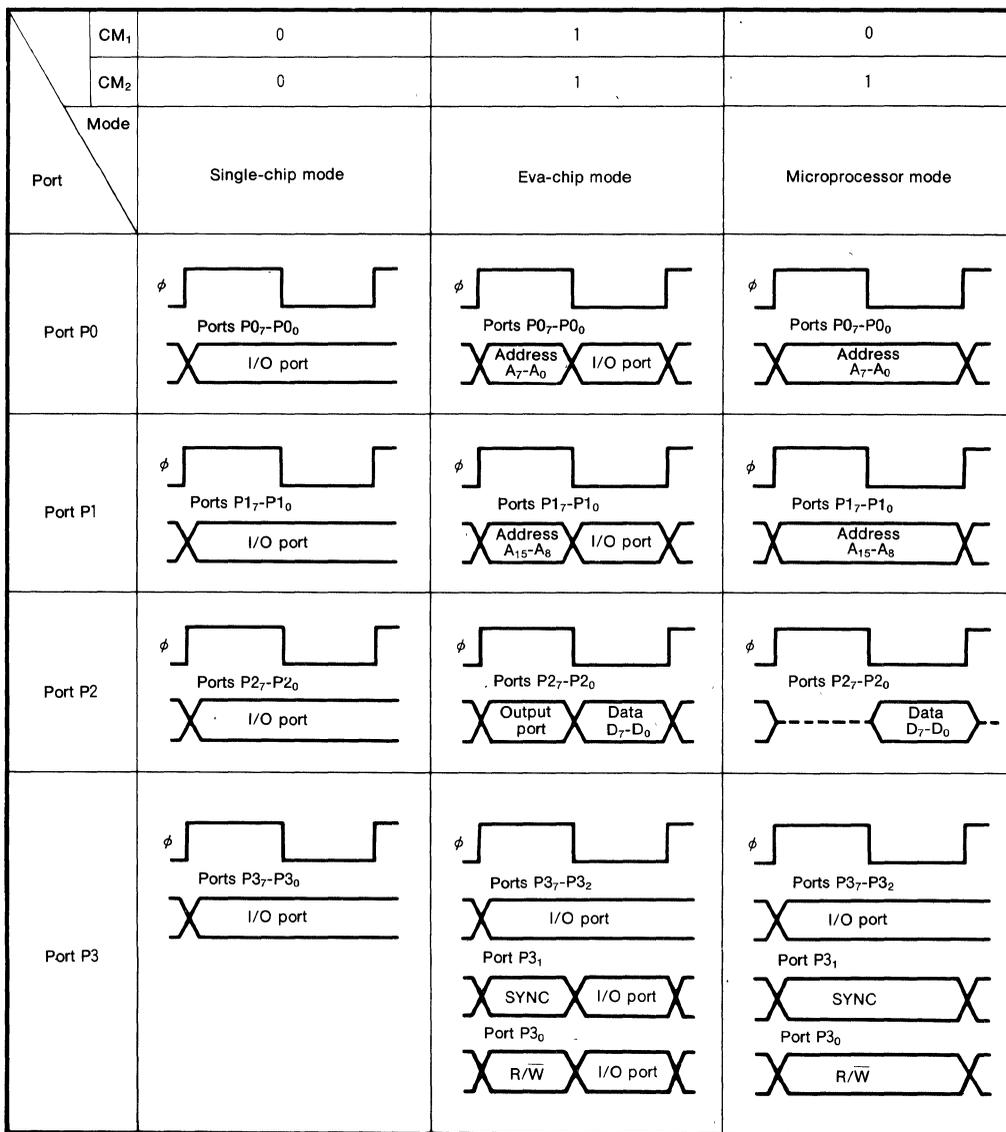


Fig. 39 Processor mode and functions of ports P0-P3

Table 8. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode • Eva-chip mode • Microprocessor mode 	The single-chip mode is set by the reset All modes can be selected by changing the processor mode bit with the program
10V	<ul style="list-style-type: none"> • Eva-chip mode 	Eva-chip mode only

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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CLOCK GENERATING CIRCUIT

The M37100M8-XXXSP has two internal clock generating circuits. Figure 41 shows a block diagram of the clock generating circuits. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ . Bit 7 of serial I/O_A mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN} .

Figure 40 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator.

The M37100M8-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 2 and timer 3 are forcibly connected and $\phi/8$ is selected as timer 2 input. When restarting oscillation, FF_{16} is automatically set in timer 2 and 07_{16} in timer 3 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 2 count stop bit must be set to supply ("0"), timer 2 interrupt enable bit and timer 3 interrupt enable bit must be set to disable ("0").

Oscillation is restarted (release the stop mode) when INT_1 , INT_2 , or serial I/O_A or serial I/O_B interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt or canceling a reset, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($60\mu A$ or less at $f(X_{CIN})=32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O_A mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. Figure 42 shows the transition of states for the system clock.

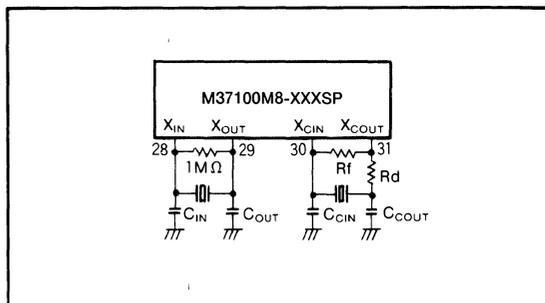


Fig. 40 Example ceramic resonator circuit

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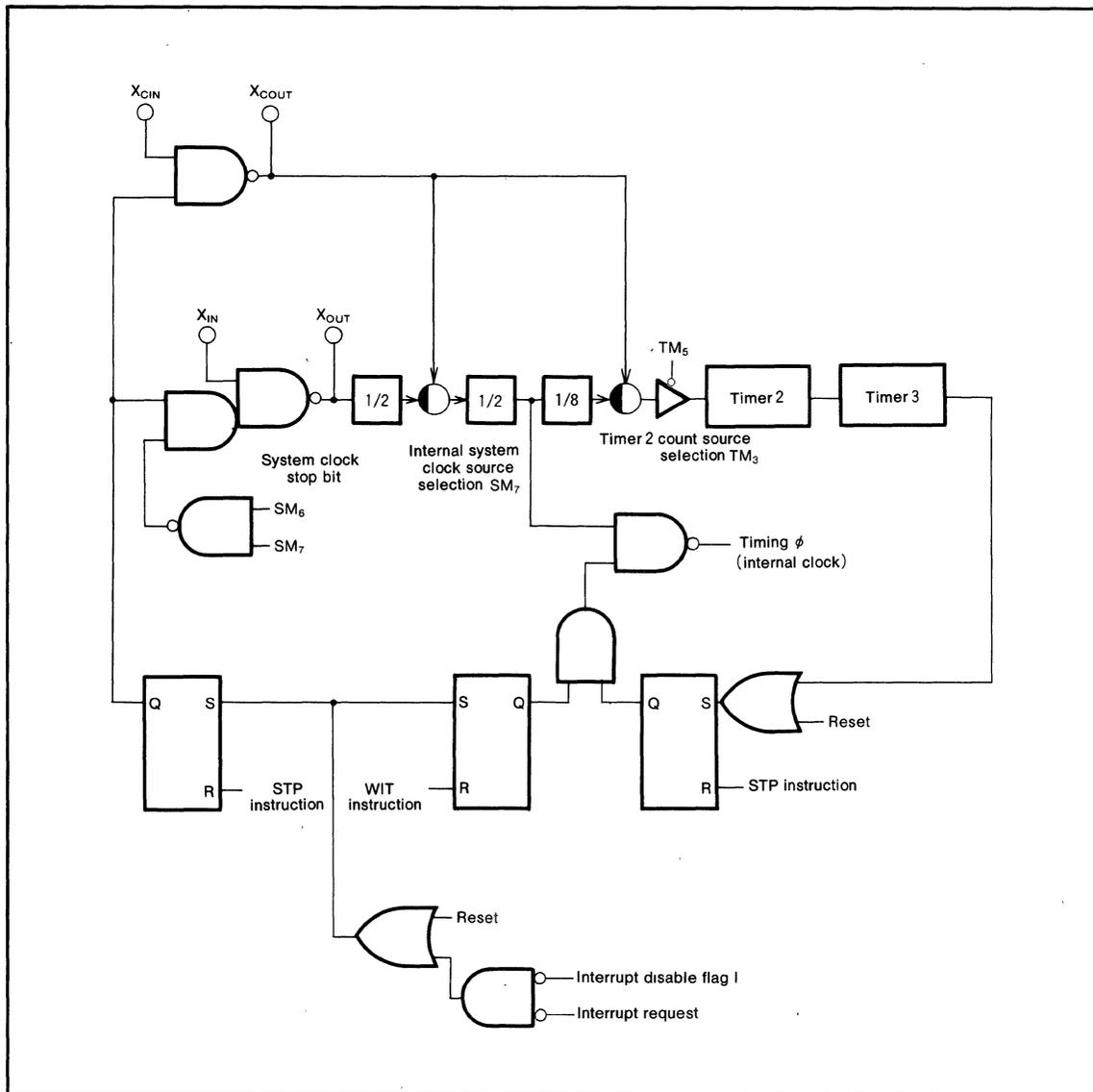


Fig. 41 Block diagram of clock generating circuit

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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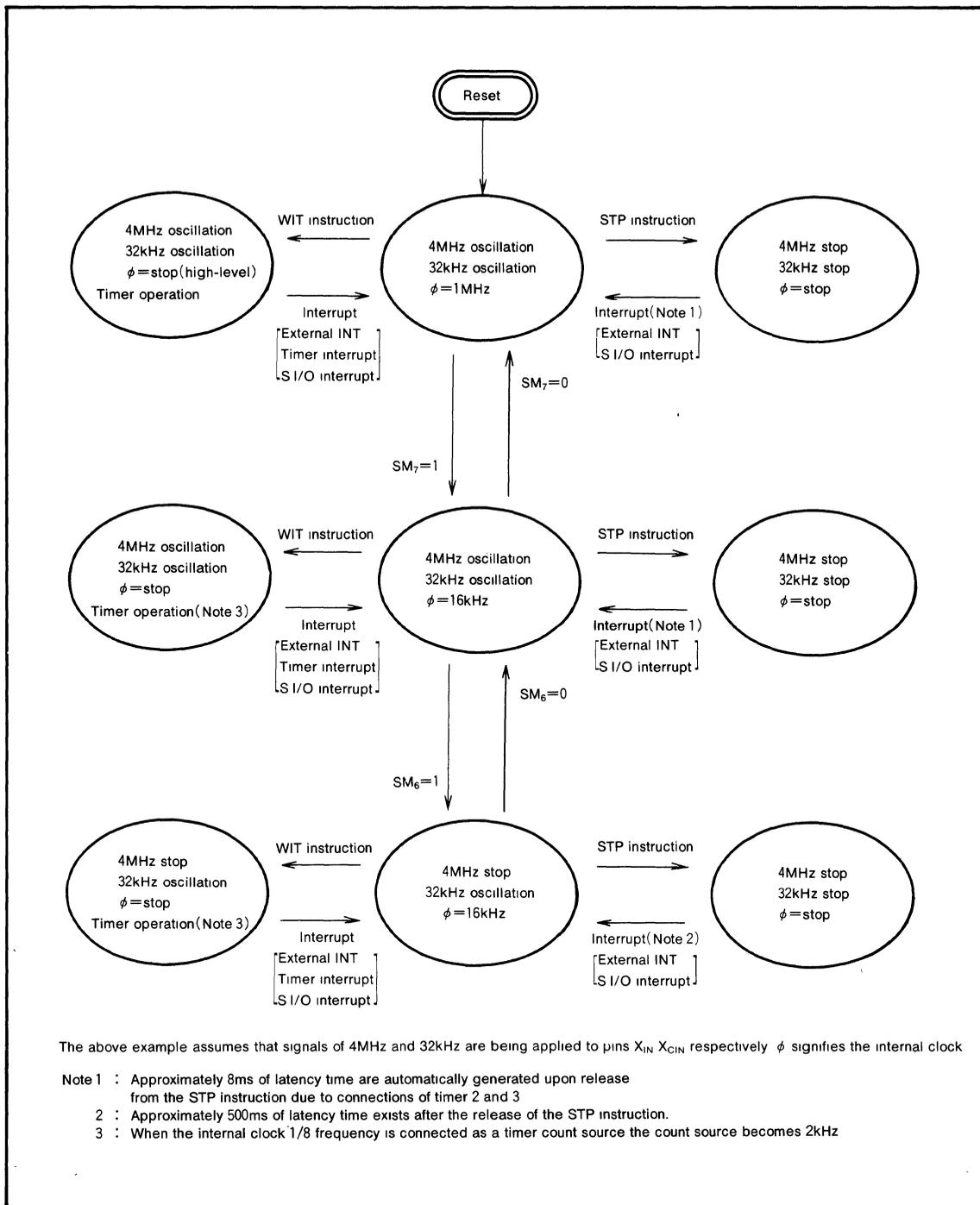
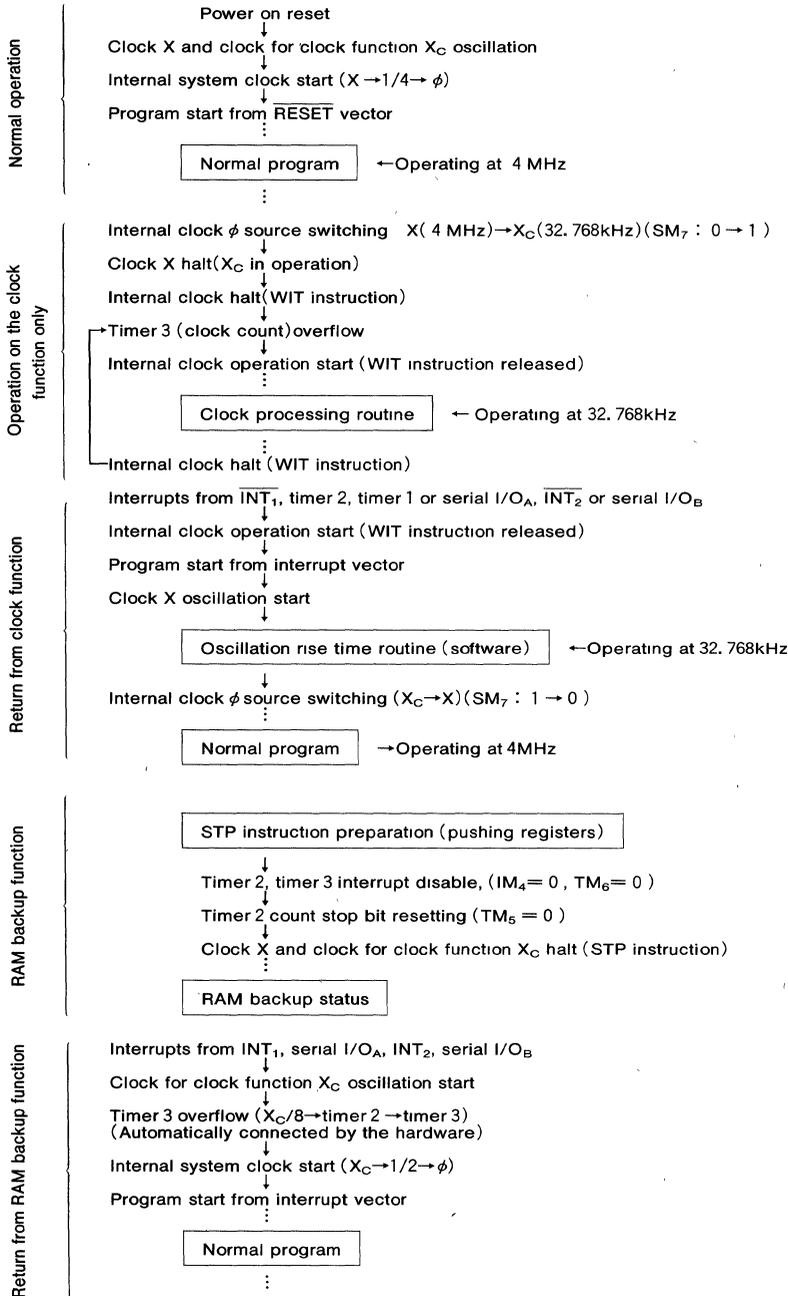


Fig. 42 Transition of states for the system clock

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

<An example of flow for system>



**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

PROGRAMMING NOTES

- (1) Processor status register
 1. Except for the interrupt disable flag (I) being set to "1", the content of the processor status register (PS) is unpredictable after a reset. Therefore, flags affecting program execution must be initialized.
The T flag and D flag which affect arithmetic operations, must always be initialized.
 2. A NOP instruction must be used after the execution of a PLP instruction.
- (2) Interrupts
Even though the BBC and BBS instructions are executed just after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) Decimal operations
 1. Decimal operations are performed by setting the decimal mode flag (D) and executing the ADC or SBC instruction. In this case, there must be at least one instruction following the ADC or SBC instruction before executing the SEC, CLC, or CLD instruction.
 2. The N (Negative), V (Overflow), and Z (Zero) flags are ignored during decimal mode.
- (4) Timers
The frequency dividing ratio of timer is $1/(n+1)$.
- (5) STP instruction
The STP instruction must be executed after setting the timer 2 count stop bit (bit 5 at address $00FF_{16}$) to supply ("0").

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- mask ROM order confirmation form
- mask specification form
- ROM data.....EPROM 3 sets

Write the following option on the mask confirmation form

- (1) Port P1 pull-up transistor bit
- (2) Port P2 pull-up transistor bit
- (3) X_{IN} and X_{CIN} oscillation feed-back registers
- (4) CRT display signal input/output polarity
- (5) ϕ output

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS} Output transistors are at "off" state	-0.3 to 6	V
V _I	Input voltage RESET, CNV _{SS}		-0.3 to 13	V
V _I	Input voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₇ , P5 ₁ -P5 ₇ , P6 ₀ -P6 ₅ , H _{SYNC} , V _{SYNC} , X _{IN} , X _{CIN} , OSC1		-0.3 to V _{CC} +0.3	V
V _O	Output voltage P0 ₀ -P0 ₇ , P6 ₂ -P6 ₅		-0.3 to 13	V
V _O	Output voltage P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P4 ₇ , P3 ₀ -P3 ₇ , P5 ₁ -P5 ₇ , P6 ₀ , P6 ₁ , X _{OUT} , φ, X _{COUT} , OSC2, R, G, B, I, OUT		-0.3 to V _{CC} +0.3	V
I _{OH}	Circuit current P6 ₀ , P6 ₁ , P4 ₇ , R, G, B, I, OUT		0 to 10 (Note 1)	mA
I _{OL1}	Circuit current P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₇ , P5 ₁ -P5 ₇ , P6 ₀ , P6 ₁ , R, G, B, I, OUT		0 to 15 (Note 2)	mA
I _{OL2}	Circuit current P0 ₀ -P0 ₇ , P6 ₂ -P6 ₅	V _O ≤ 7 V V _O > 7 V	0 to 15 (Note 2) 0 to 1 (Note 2)	mA
P _d	Power dissipation	T _a = 25°C	1000 (Note 3)	mW
T _{opr}	Operating temperature		-10 to 70	°C
T _{stg}	Storage temperature		-40 to 125	°C

- Note 1 : The total of I_{OH} should be 20mA(max).
2 : The total of I_{OL1} and I_{OL2} should be 50mA(max).
3 : 600mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=-10 to 70°C unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ.	Max	
V _{CC}	Supply voltage (Note 1)	Normal speed mode f(X _{IN})=4MHz f(OSC1)=5MHz	4.5	5.0	5.5	V
		Low-speed mode f(X _{CIN})=32kHz	3.0	5.0	5.5	
V _{SS}	Supply voltage		0	0	0	V
V _{IH}	"H" input voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₇ , P5 ₁ -P5 ₇ , P6 ₀ -P6 ₅ , RESET, X _{IN} , X _{CIN} , H _{SYNC} , V _{SYNC}	0.8V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃ -P3 ₅ , P3 ₇ , P4 ₇ , P5 ₁ , P5 ₄ , P5 ₅ , P5 ₇ , P6 ₀ -P6 ₅	0		0.4V _{CC}	V
V _{IL}	"L" input voltage	P3 ₂ , P3 ₆ , P5 ₂ , P5 ₃ , P5 ₆ , RESET, X _{IN} , X _{CIN} , H _{SYNC} , V _{SYNC}	0		0.2V _{CC}	V
I _{OL(avg)}	"L" average output current	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₇ , P5 ₁ -P5 ₇ , P6 ₀ -P6 ₅ , R, G, B, I, OUT			5	mA
I _{OL(avg)}	"L" average output current	V _O ≤ 7V			5	mA
		V _O > 7V			1	
I _{OH(avg)}	"H" average output current	P4 ₇ , P6 ₀ , P6 ₁ , R, G, B, I, OUT			2	mA
f(X _{IN})	Oscillating frequency (Note 2)		3.6	4	4.4	MHz
f(X _{CIN})	Oscillating frequency		29	32	35	kHz
f(OSC1)	Oscillating frequency		4	5	6	MHz

- Note 1 : Apply 0.022μF or greater capacitance externally to the V_{CC} power supply pin so as to reduce power source noise
2 : Use a ceramic resonator or a quartz crystal oscillator to generate of main clock

MITSUBISHI MICROCOMPUTERS
M37100M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10$ to $70^\circ C$, $f(X_{IN})=4MHz$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage P47, P60, P61, R, G, B, I, OUT	$V_{CC}=4.5V$, $I_{OH}=-0.5mA$	2.4			V
V_{OH}	"H" output voltage ϕ	$V_{CC}=4.5V$ $I_{OH}=-2.5mA$	2.4			V
V_{OL}	"L" output voltage P00-P07, P20-P27, P30-P37, P47, P51-P57, P60-P65, R, G, B, I, OUT	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
V_{OL}	"L" output voltage P10-P17	$V_{CC}=4.5V$ $I_{OL}=10mA$			1.5	V
V_{OL}	"L" output voltage ϕ	$V_{CC}=4.5V$ $I_{OL}=2.5mA$			2	V
$V_{T+} - V_{T-}$	Hysteresis RESET	$V_{CC}=5.0V$		0.5	0.7	V
$V_{T+} - V_{T-}$	Hysteresis P32, P36, P52, P53, P56, H _{SYNC} , V _{SYNC}	$V_{CC}=5.0V$		0.5	1.3	V
R_U	Pull-up transistor (Note 1) P10-P17, P20-P27	$V_{CC}=5.0V$ $V_i=0V$	15	30	60	k Ω
I_{OZH}	"H" input leak current P00-P07, P10-P17, P20-P27, P30-P37, P47, P51-P57, P60-P65, RESET, H _{SYNC} , V _{SYNC}	$V_{CC}=5.5V$ $V_O=5.5V$			5	μA
I_{OZH}	"H" input leak current P00-P07, P62-P65	$V_{CC}=5.5V$ $V_O=12V$			10	μA
I_{OZL}	"L" input leak current P00-P07, P10-P17, P20-P27, P30-P37, P47, P51-P57, P60-P65, H _{SYNC} , V _{SYNC} , RESET	$V_{CC}=5.5V$ $V_O=0V$			5	μA
V_{RAM}	RAM retention voltage	At stop mode	2.5		5.5	V
I_{CC}	Supply current	$V_{CC}=5.5V$ $f(X_{IN})=4MHz$ At system operation and CRT display off		5	10	mA
		$V_{CC}=5.5V$ $f(X_{IN})=4MHz$ At system operation and CRT display on		7	14	
		$V_{CC}=5.5V$ $f(X_{IN})=4MHz$ At wait mode		1		
		$X_{IN}-X_{OUT}$ stop $f(X_{CIN})=32kHz$ At system operation	$V_{CC}=5.5V$	60	200	μA
			$V_{CC}=3V$	25		
		$X_{IN}-X_{OUT}$ stop $f(X_{CIN})=32kHz$	$V_{CC}=5.5V$	25	100	
		At wait mode	$V_{CC}=3V$	5		
		At stop mode	$V_{CC}=5.5V$	1	10	
			$V_{CC}=3V$	0.6		

Note 1 : Pull-up transistor is mask option.

MITSUBISHI MICROCOMPUTERS

M37102M8-XXXSP/FP

M37201M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with **ON-SCREEN DISPLAY CONTROLLER**

DESCRIPTION

The M37102M8-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP. This single-chip microcomputer is useful for the high-tech channel selection system for TVs.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37102M8-XXXSP/FP and the M37201M6-XXXSP are noted below. The following explanations apply to the M37102M8-XXXSP. Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37102M8-XXXSP/FP	16384 bytes	320 bytes
M37201M6-XXXSP	24576 bytes	384 bytes

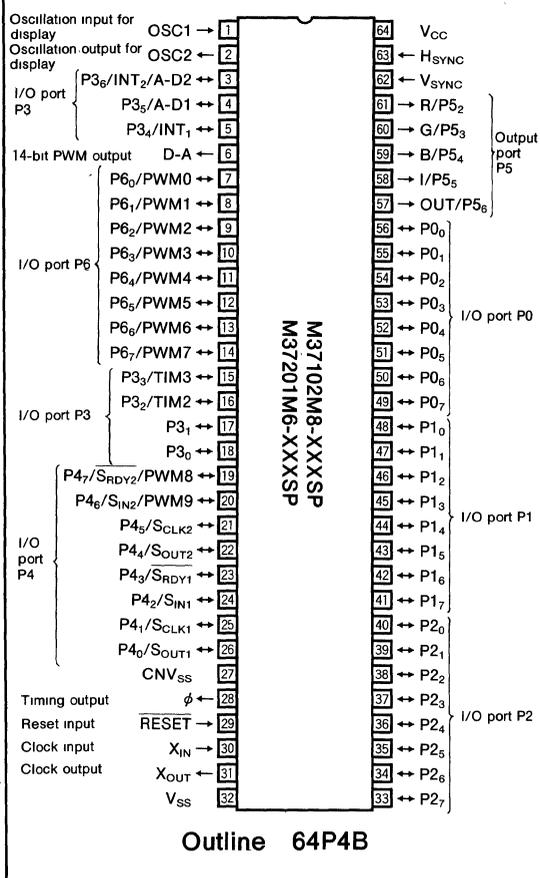
FEATURES

- Number of basic instructions 69
- Memory size ROM 16384 bytes (M37102M8-XXXSP/FP)
24576 bytes (M37201M6-XXXSP)
RAM 320 bytes (M37102M8-XXXSP/FP)
384 bytes (M37201M6-XXXSP)
- Instruction execution time
..... 1 μ s (minimum instructions at 4MHz frequency)
- Single power supply 5V \pm 10%
- Power dissipation
normal operation mode (at 4MHz frequency)
..... 110mW (V_{CC} =5.5V, CRT display)
- Subroutine nesting 96 levels (Max.)
- Interrupt 13types, 13vectors
- 8-bit timer 4
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P6) 47
- Output port (Port P5) 5
- Serial I/O (8-bit) 2
- PWM function 14-bit \times 1
8-bit \times 10
- A-D converter (4-bit resolution) 2 channels
- 72-character on screen display function
Number of character 24 characters \times 3 lines
Kinds of character 126

APPLICATION

TV

PIN CONFIGURATION (TOP VIEW)

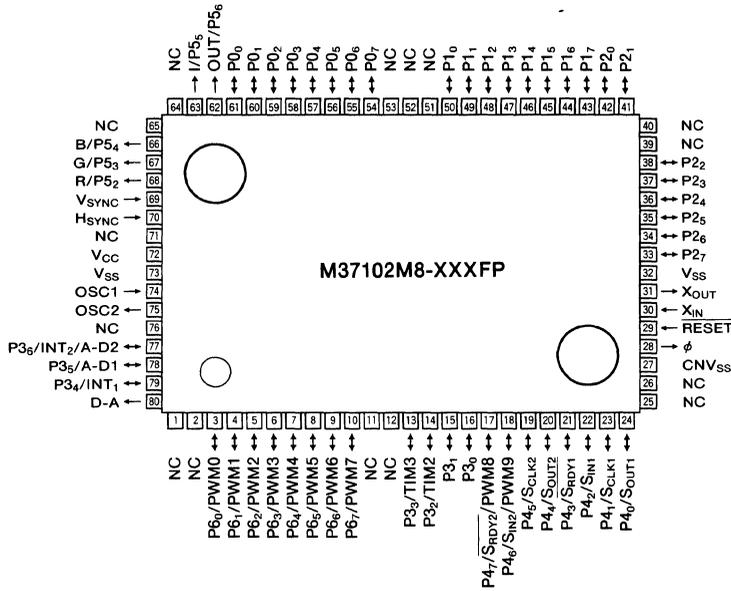


Outline 64P4B

MITSUBISHI MICROCOMPUTERS
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M37201M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N

NC : No connection

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONS OF M37102M8-XXXSP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		1 μ s (minimum instructions, at 4MHz frequency)	
Clock frequency		4MHz	
Memory size	M37102M8-XXXSP/FP	ROM	16384bytes
		RAM	320bytes
	M37201M6-XXXSP	ROM	24576bytes
		RAM	384bytes
Input/Output ports	P0, P1, P2	I/O	8-bitX3
	P3 ₀ , P3 ₁	I/O	2-bitX1
	P3 ₂ -P3 ₆	I/O	5-bitX1 (can be used as timer input pins, INT ₁ , INT ₂ input pins and A-D input pins)
	P4	I/O	8-bitX1 (can be used as serial I/O function pins and PWM output pins)
	P5	Output	5-bitX1 (can be used as R, G, B, I, OUT pins)
	P6	I/O	8-bitX1 (can be used as PWM output pins)
Serial I/O		8-bitX2 (Special serial I/O (8-bit)X1)	
Timers		8-bit timerX4	
Subroutine nesting		96levels (max)	
Interrupt		Two external interrupts, nine internal interrupts, one software interrupt	
Clock generating circuit		Two built-in circuits (externally connected ceramic or quartz crystal oscillator)	
Supply voltage		5V \pm 10%	
Power dissipation	at CRT display ON		110mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ.)
	at CRT display OFF		55mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)
	at stop mode		1.65mW (Max)
Input/Output characteristics	Input/Output voltage		5V (Port P4 ₆ , P4 ₇ , P6 ₀ -P6 ₇)
	Output current		10mA (Port P2 ₄ -P2 ₇)
Operating temperature range		-10 to 70°C	
Device structure		CMOS silicon gate process	
Package	M37102M8-XXXSP, M37201M6-XXXSP		64-pin shrink plastic molded DIP
	M37102M8-XXXFP		80-pin plastic molded QFP
CRT display function	Number of character		24 charactersX3 lines
	Kinds of character		126 (12X16 dots)

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is connected to V _{SS} .
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2 μ s (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
P0 ₀ -P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
P1 ₀ -P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
P2 ₀ -P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
P3 ₀ -P3 ₆	I/O port P3	I/O	Port P3 is a 7-bit I/O port and has basically the same functions as port P0, but the output structure of P3 ₀ , P3 ₁ is CMOS output and the output structure of P3 ₂ -P3 ₆ is N-channel open drain. P3 ₂ , P3 ₃ are in common with external clock input pins of timer 2 and 3. P3 ₄ , P3 ₆ are in common with external interrupt input pins INT ₁ and INT ₂ . P3 ₅ , P3 ₆ are in common with analog input pins of A-D converter (A-D1, A-D2).
P4 ₀ -P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. When serial I/O1 is used, P4 ₀ , P4 ₁ , P4 ₂ and P4 ₃ work as S _{OUT1} , S _{CLK1} , S _{IN1} and $\overline{\text{SRDY1}}$ pins, respectively. When serial I/O2 is used, P4 ₄ , P4 ₅ , P4 ₆ and P4 ₇ work as S _{OUT2} , S _{CLK2} , S _{IN2} and $\overline{\text{SRDY2}}$ pins, respectively. Also P4 ₆ , P4 ₇ are in common with PWM output pins of PWM 8 and 9.
P6 ₀ -P6 ₇	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. This port is in common with PWM output pins PWM0-PWM7.
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display function.
H _{SYNC}	H _{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display.
V _{SYNC}	V _{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display.
R, G, B, I, OUT	CRT output	Output	This is a 5-bit output pin for CRT display. The output structure is CMOS output. This is in common with port P5 ₂ -P5 ₆ .
D-A	DA Output	Output	This is an output pin for 14-bit PWM.

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37102 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address 00FB₁₆. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

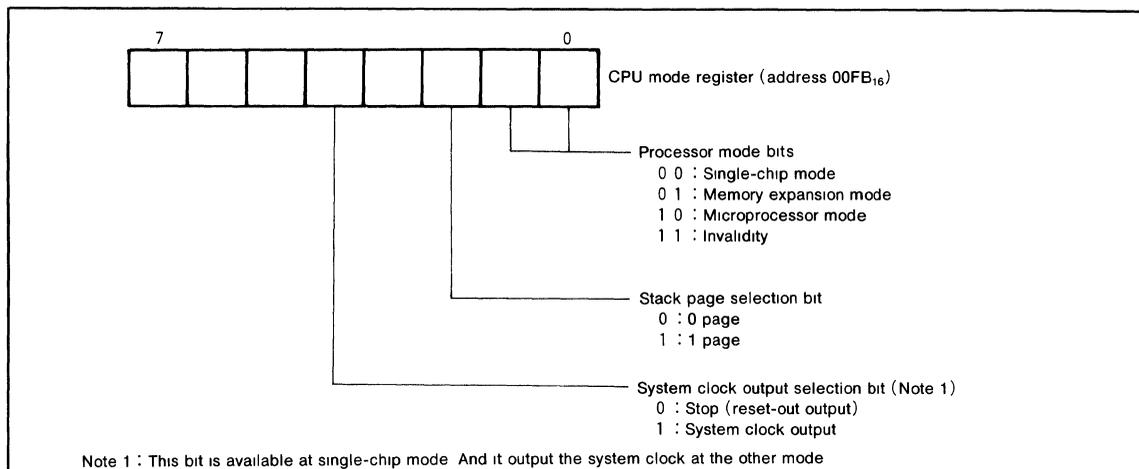


Fig. 1 Structure of CPU mode register

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **RAM for display**

RAM for display is used for specifying the character codes and colors to display.

• **ROM for display**

ROM for display is used for storing character data.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

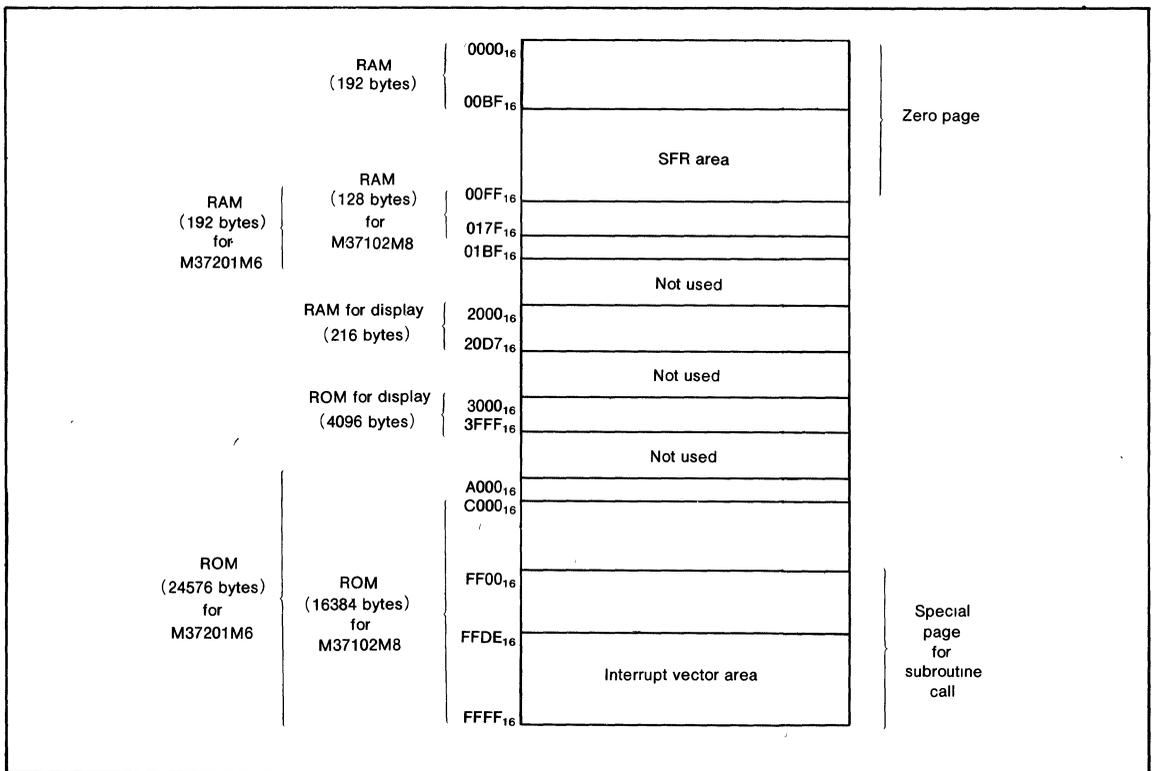


Fig. 2 Memory map

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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00C0 ₁₆	Port P0	00E0 ₁₆	Horizontal position register
00C1 ₁₆	Port P0 directional register	00E1 ₁₆	Vertical display start position register 1
00C2 ₁₆	Port P1	00E2 ₁₆	Vertical display start position register 2
00C3 ₁₆	Port P1 directional register	00E3 ₁₆	Vertical display start position register 3
00C4 ₁₆	Port P2	00E4 ₁₆	Character size register
00C5 ₁₆	Port P2 directional register	00E5 ₁₆	Border selection register
00C6 ₁₆	Port P3	00E6 ₁₆	Color register 0
00C7 ₁₆	Port P3 directional register	00E7 ₁₆	Color register 1
00C8 ₁₆	Port P4	00E8 ₁₆	Color register 2
00C9 ₁₆	Port P4 directional register	00E9 ₁₆	Color register 3
00CA ₁₆	Port P5	00EA ₁₆	CRT control register
00CB ₁₆	Port P5 directional register	00EB ₁₆	Display block counter
00CC ₁₆	Port P6	00EC ₁₆	CRT port control register
00CD ₁₆	Port P6 directional register	00ED ₁₆	Scroll control register
00CE ₁₆	DA-H register	00EE ₁₆	Scroll start register
00CF ₁₆	DA-L register	00EF ₁₆	A-D control register
00D0 ₁₆	PWM 0 register	00F0 ₁₆	Timer 1
00D1 ₁₆	PWM 1 register	00F1 ₁₆	Timer 2
00D2 ₁₆	PWM 2 register	00F2 ₁₆	Timer 3
00D3 ₁₆	PWM 3 register	00F3 ₁₆	Timer 4
00D4 ₁₆	PWM 4 register	00F4 ₁₆	Timer 12 mode register
00D5 ₁₆	PWM output control register 1	00F5 ₁₆	Timer 34 mode register
00D6 ₁₆	PWM output control register 2	00F6 ₁₆	PWM 5
00D7 ₁₆	Interrupt space distinguish register	00F7 ₁₆	PWM 6
00D8 ₁₆	Interrupt space distinguish control register	00F8 ₁₆	PWM 7
00D9 ₁₆	Special serial I/O register	00F9 ₁₆	PWM 8
00DA ₁₆	Special mode register 1	00FA ₁₆	PWM 9
00DB ₁₆	Special mode register 2	00FB ₁₆	CPU mode register
00DC ₁₆	Serial I/O1 mode register	00FC ₁₆	Interrupt request register 1
00DD ₁₆	Serial I/O1 register	00FD ₁₆	Interrupt request register 2
00DE ₁₆	Serial I/O2 mode register	00FE ₁₆	Interrupt control register 1
00DF ₁₆	Serial I/O2 register	00FF ₁₆	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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INTERRUPTS

Interrupts can be caused by 12 different events consisting of three external, eight internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
CRT interrupt	2	FFFD ₁₆ , FFFC ₁₆	
INT ₂ interrupt	3	FFFB ₁₆ , FFFA ₁₆	
INT ₁ interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	
Serial I/O 2 interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	
Timer 4 interrupt	6	FFF5 ₁₆ , FFF4 ₁₆	
1 ms interrupt	7	FFF3 ₁₆ , FFF2 ₁₆	
V _{SYNC} interrupt	8	FFF1 ₁₆ , FFF0 ₁₆	
Timer 3 interrupt	9	FFEF ₁₆ , FFEE ₁₆	
Timer 2 interrupt	10	FFED ₁₆ , FFEC ₁₆	
Timer 1 interrupt	11	FFEB ₁₆ , FFEA ₁₆	
Serial I/O 1 interrupt	12	FFE9 ₁₆ , FFE8 ₁₆	
BRK instruction interrupt	13	FFDF ₁₆ , FFDE ₁₆	Non-maskable software interrupt

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

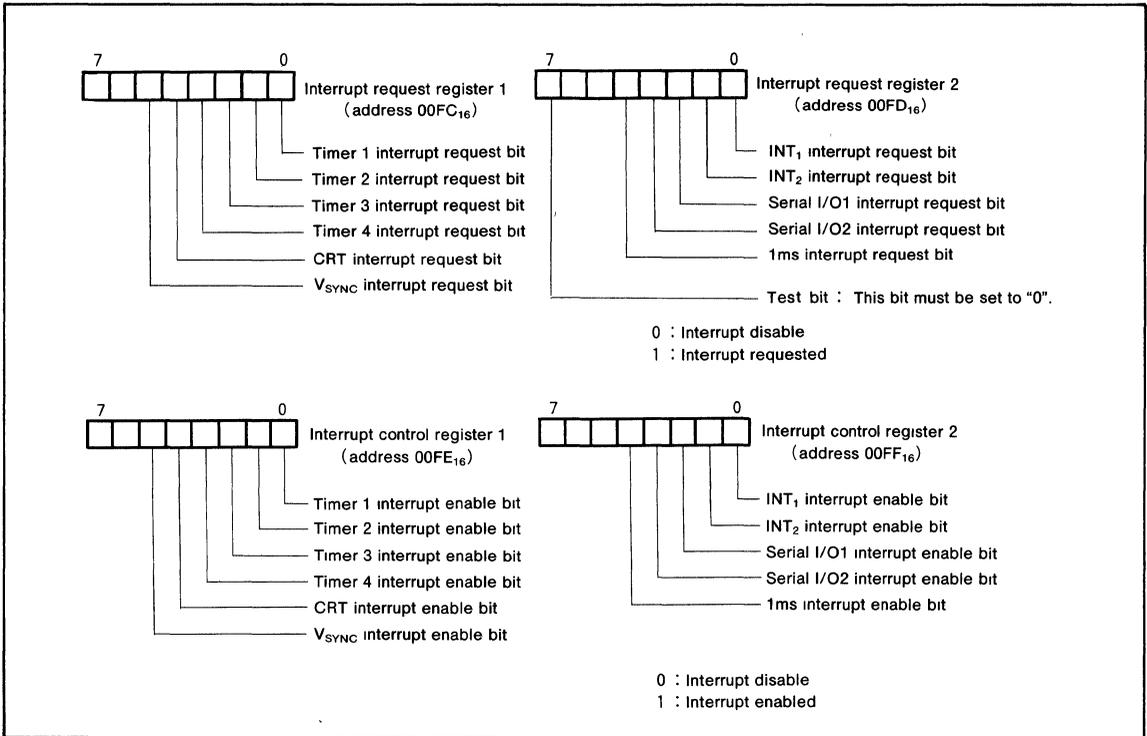


Fig. 4 Structure of registers related to interrupt

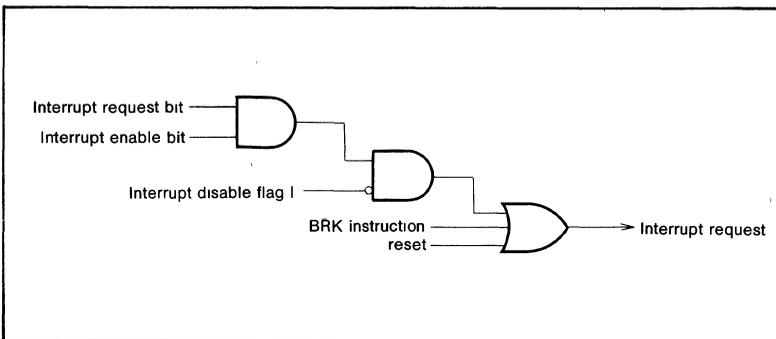


Fig. 5 Interrupt control

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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TIMER

The M37102M8-XXXSP has four timers; timer 1, timer 2, timer 3 and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 7. The count source for timer 1 through 4 can be selected by using bit 0, 1, 4 of timer 12 mode register and timer 34 mode register (address 00F4₁₆, 00F5₁₆), as shown in Figure 6.

All of the timers are down count timers and have 8-bit latches. When a timer reaches "FF₁₆" and the next count pulse is input to a timer, a value which is subtracted 1 from the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch. The timer interrupt request bit is set at the next count pulse after the timer reaches "FF₁₆".

The starting and stopping of the timer is controlled by bit 2, 3 of timer 12 mode register and timer 34 mode register.

At a reset or stop mode, FF₁₆ is automatically set in timer 3 and 07₁₆ in timer 4 and timer 4, timer 3 and the clock ($f(X_{IN})$ divided by 16) are connected in series.

When restarting oscillation or canceling a reset, the internal clock is not supplied to the CPU until timer 4 overflows.

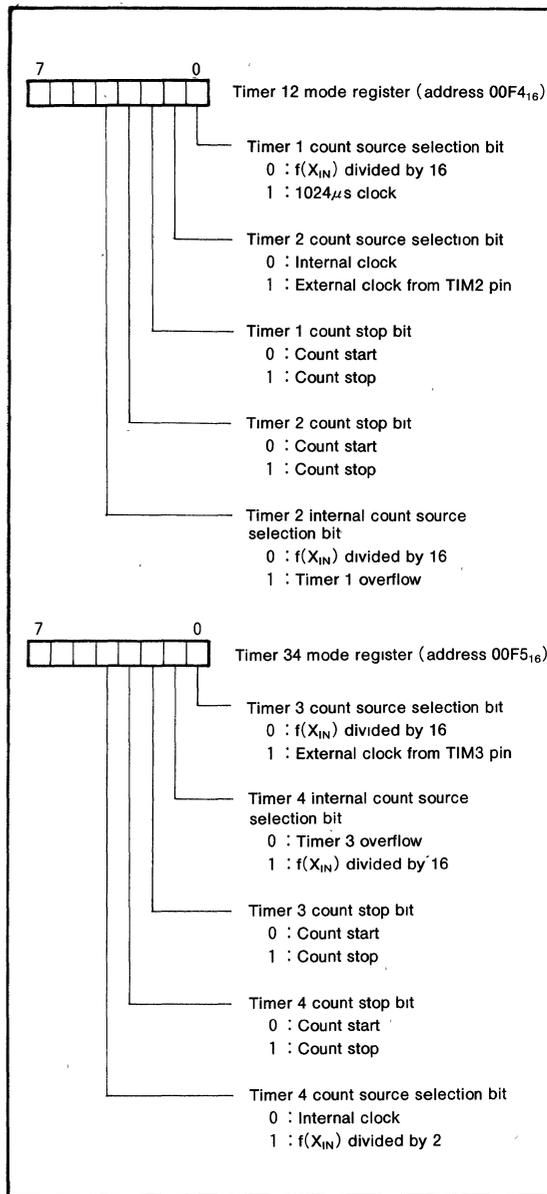


Fig. 6 Structure of timer 12 mode register and timer 34 mode register

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

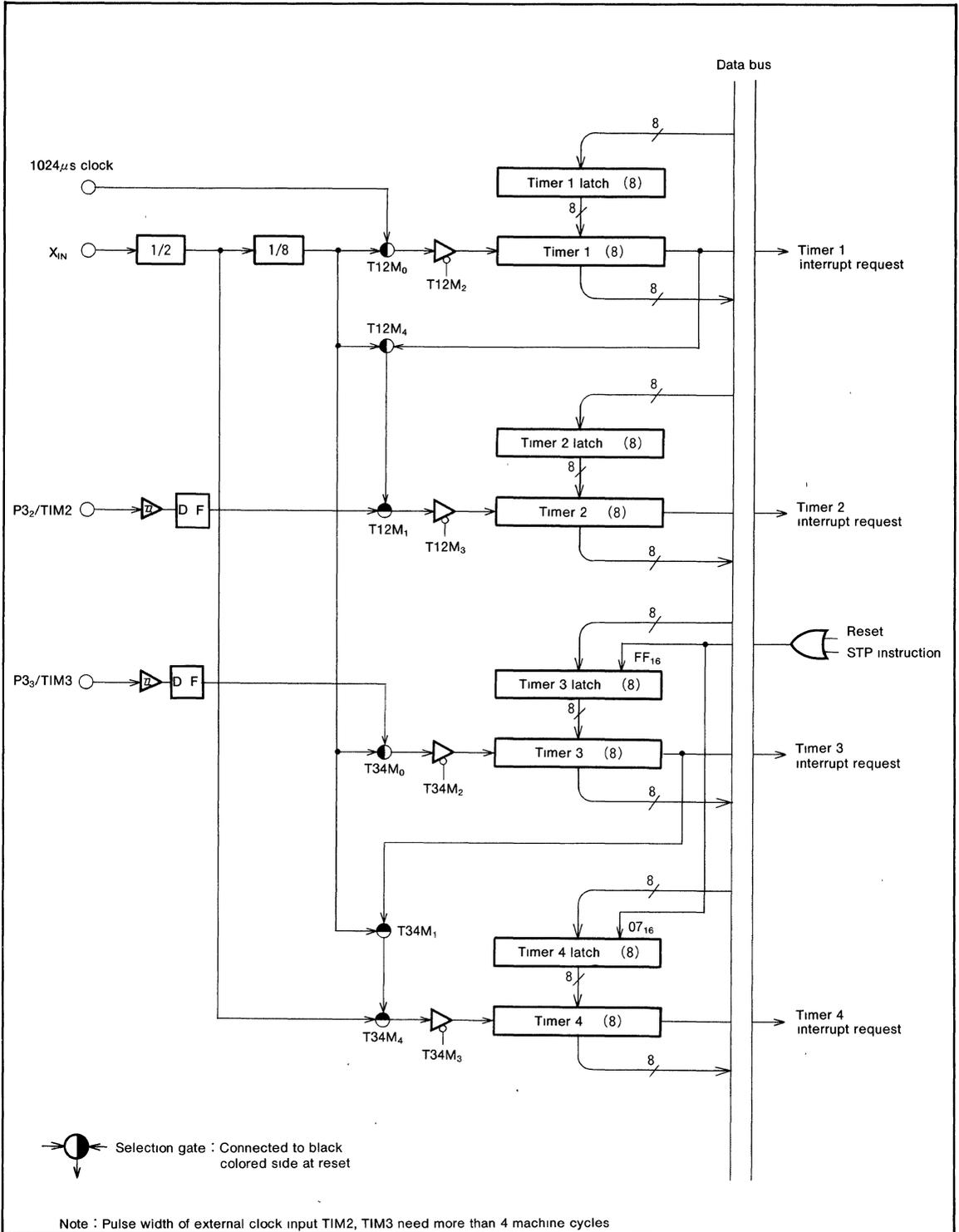


Fig. 7 Block diagram of timer 1, timer 2, timer 3 and timer 4

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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SERIAL I/O

M37102M8-XXXSP has two serial I/O (serial I/O 1, serial I/O 2). Serial I/O 1 has the same function as serial I/O 2.

A block diagram of the serial I/O is shown in Figure 8.

In the serial I/O mode the receive ready signal ($\overline{S_{RDYi}}$), synchronous input/output clock (S_{CLKi}), and the serial I/O pins (S_{OUTi} , S_{INi}) are used as port P4. The serial I/O_i mode registers (address 00DC₁₆, 00DE₁₆) are 8-bit registers. Bits 0, 1 and 2 of these registers are used to select a synchronous clock source.

Bit 3 and 4 decide whether parts of P4 will be used as a serial I/O or not.

To use P4₂ or P4₆ as a serial input, set the directional register bit which corresponds to P4₂ or P4₆ to "0". For more information on the directional register, refer to the I/O pin section.

Also to use internal clock of serial I/O 2, bit 1 of special mode register 1 (address 00DA₁₆) needs to be set to "1". The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

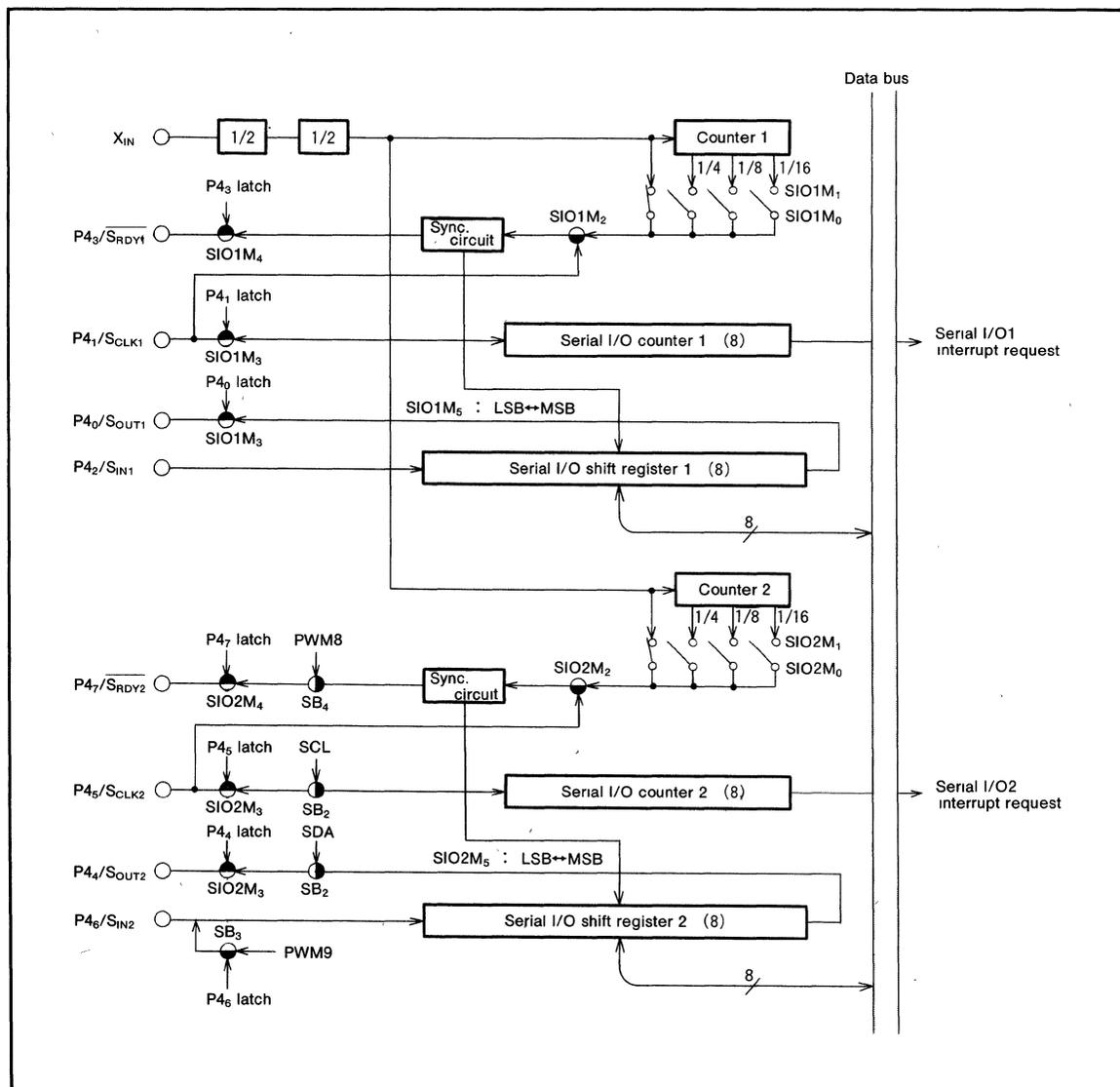


Fig. 8 Block diagram of serial I/O

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Internal clock—The $\overline{S_{RDY}_i}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_i register (address 00DD₁₆, 00DF₁₆). After the falling edge of the write signal, the $\overline{S_{RDY}_i}$ signal becomes low signaling that the M37102M8-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}_i}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_i counter is set to 7 when data is stored in the serial I/O_i register. At each falling edge of the transfer clock, serial data is output to S_{OUT_i}. During the rising edge of this clock, data can be input from S_{IN_i} and the data in the serial I/O_i register will be shifted 1 bit.

Transfer direction can be selected by bit 5 of serial I/O_i mode register. After the transfer clock has counted 8 times, the serial I/O_i register will be empty and the transfer clock will remain at a high level. At this time the interrupt request

bit will be set.

External clock- If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O_i counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

An example of communication between two M37102M8-XXXSPs is shown in Figure 10.

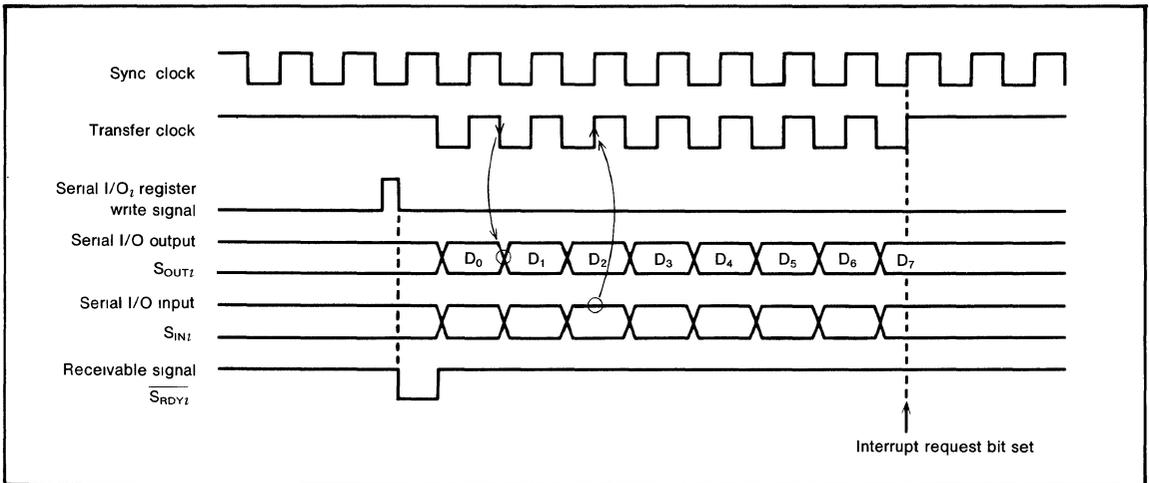


Fig. 9 Serial I/O timing

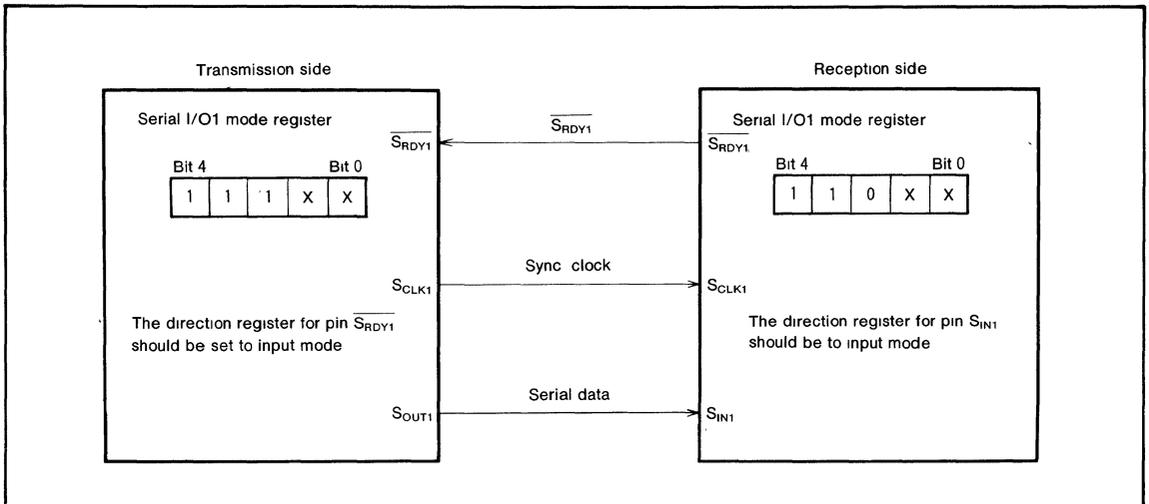


Fig. 10 Example of serial I/O connection

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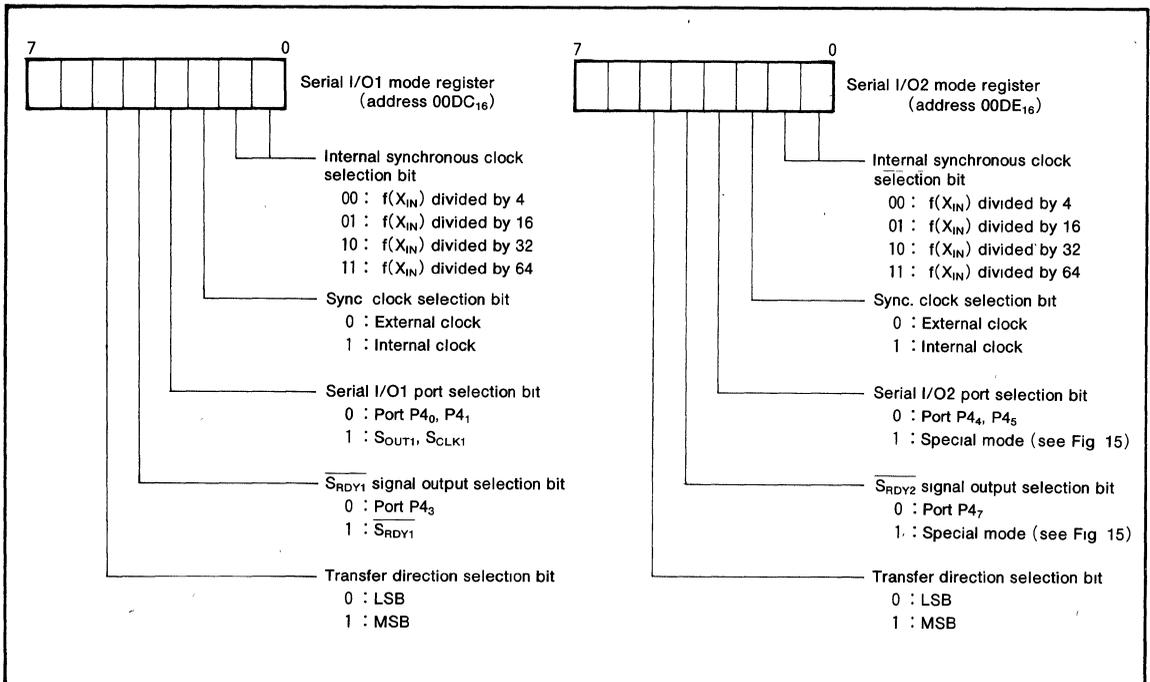


Fig. 11 Structure of serial I/O_i mode register

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SPECIAL MODE (I²C BUS MODE*)

M37102M8-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I²C (Inter IC) bus format.

I²C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICS of a machinery.

M37102M8-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O are explained in the following:

(1) Master transmission

To generate an interrupt at the end of transmission, set bit 7 of special mode register 2 (address 00DB₁₆) to "1" so as to special mode serial I/O interrupt is selected. Then set bit 3 of interrupt control register 2 (address 00FF₁₆) to "1" so as to special mode serial I/O interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

The output signals of master transmission SDA and SCL are output from ports P₄₄ and P₄₅. Set all bits (bits 4 and 5) corresponding to P₄₄ and P₄₅ of the port P4 register (address 00C8₁₆) and the port P4 direction register (address 00C9₁₆) to "1".

Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4. (For instance, if f(X_{IN})/16 is selected as the clock source of timer 4 and 4 is set in timer 4 when f(X_{IN}) is 4MHz, the master transmission clock frequency is 25kHz.)

Set contents of the special mode register 2 (address 00DB₁₆). (Usually, "83₁₆".)

Set the bit 3 of serial I/O mode register (address 00DE₁₆). After that set the special mode register 1 (address 00DA₁₆). Figure 15 shows the structure of special mode registers 1 and 2.

Initial setting is completed by the above procedure.

Write data to be transmitted in the special serial I/O regis-

ter (address 00D9₁₆). Immediately after this, clear bits 0 and 1 of special mode register 2 (to "0") to make both SDA and SCL output to "L". This is for arbitration. The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK reception and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 3 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

To terminate data transfer, clear bits 0 and 1 of the special mode register to "0", set bit 1 clock SCL to "1", then set bit 1 data SDA to "1". This procedure transmits the stop signal. Figure 13 shows master transmission timing explained above.

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission.

In the interrupt routine, set master reception ACK provided (26₁₆) in the special mode register 1 (address 00DA₁₆), and write "FF₁₆" in the special serial I/O register (address 00D9₁₆). This sets data line SDA to "H" and to perform 8-clock master reception. Then, "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission.

Figure 14 shows master reception timing.

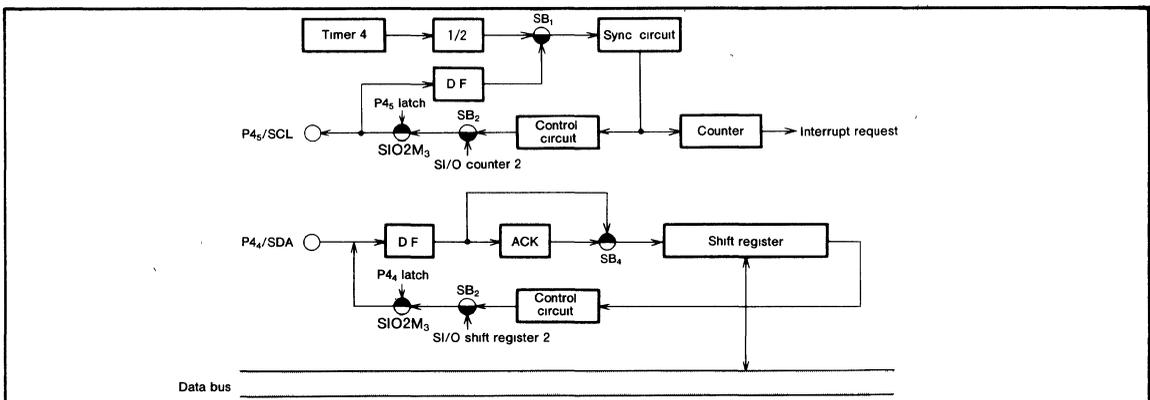


Fig. 12 Block diagram of special serial I/O

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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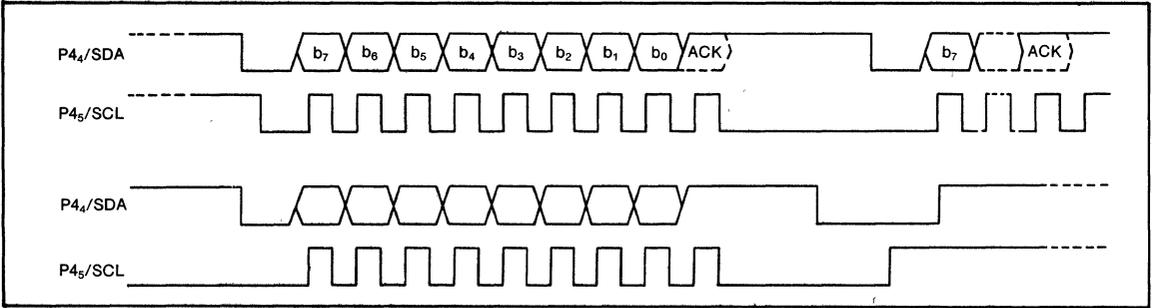


Fig. 13 Master transmission timing

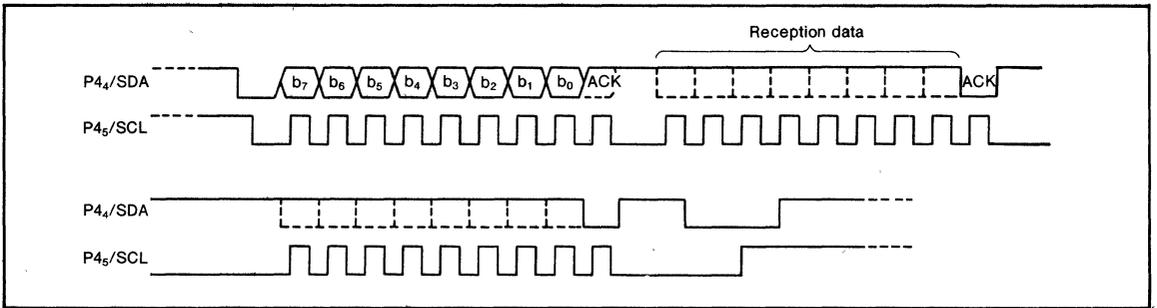


Fig. 14 Master reception timing

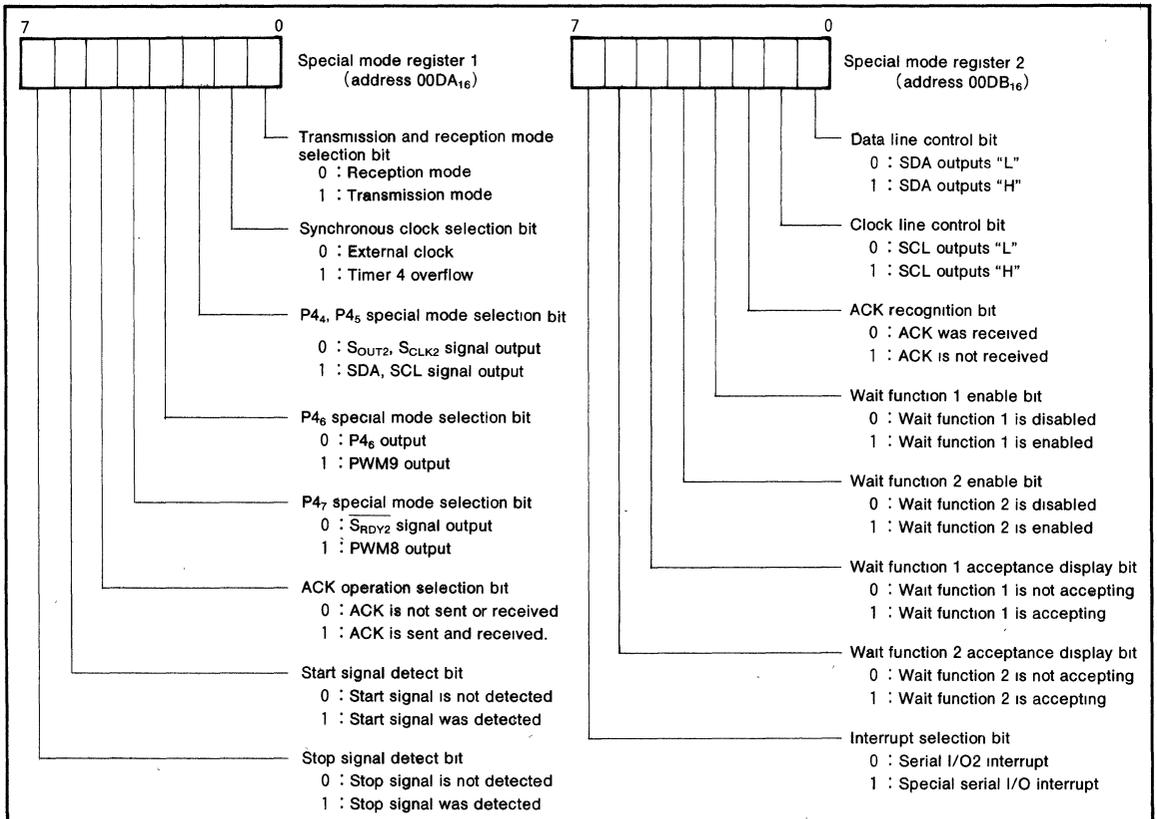


Fig. 15 Structure of special mode registers 1 and 2

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PWM OUTPUT CIRCUIT

(1) Introduction

The M37102M8-XXXSP is equipped with one 14-bit PWM (DA) and ten 8-bit PWMs (PWM0-PWM9). The 14-bit resolution gives DA the minimum resolution bit width of 500ns (for $X_{IN}=4\text{MHz}$) and a repeat period of 8192 μs . PWM0-PWM9 have a 8-bit resolution with minimum resolution bit width of 8 μs and repeat period of 2048 μs .

Block diagram of the PWM is shown in Figure 16.

The PWM timing generator section applies individual control signals to DA and PWM0-9 using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM0-7 are in common with port P6 and PWM8, 9 are in common with port P4₆, P4₇.

For PWM output, each PWM output selection bit (bit 1 to 7 of PWM output control register 1, bit 0, 1 of PWM output control register 2, bit 3, 4 of special mode register 1 and bit 4 of serial I/O 2 mode register) should be set. When DA is used for output, first set the higher 8-bit of the DA-H register (address 00CE₁₆), then the lower 6-bit of the DA-L register (address 00CF₁₆).

When one of the PWM0-9 is used for output, set the 8-bit in the PWM0-9 register (address 00D0₁₆ to 00D4₁₆, 00F6₁₆ to 00FA₁₆), respectively.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data in each PWM register is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. However, bit 7 of the DA-L register indicated the completion of the data transfer from the DA register to the DA latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 8-bit PWMs

The timing diagram of the ten 8-bit PWMs (PWM0-9) is shown in Figure 17. One period (T) is composed of 256 (2⁸) segments.

There are eight different pulse types configured from bits 0 to 7 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 17 (a).

Eight different pulses can be output from the PWM. These can be selected by bits 0 through 7. Depending on the content of the 8-bit PWM latch, pulses from 7 to 0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 17 (b). Changes in the contents of the PWM latch allows the selection of 256 lengths of high-level area outputs varying from 0/256 to 255/256. An length of entirely high-level output cannot be output, i.e. 256/256.

(5) 14-bit PWM operation

The output example of the 14-bit PWM is shown in Figure 18. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length D_H times τ is output every short area of $t=256 \tau=128\mu\text{s}$ as determined by data D_H of the higher 8 bits.

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ . As a result, the short-area period t (=128 μs , approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P4, P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 low-order bits of data and high-level area increase space

6 low-order bits of data	Area longer by τ than that of other t_m ($m = 0$ to 63)
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m=32$
0 0 0 0 1 0	$m=16, 48$
0 0 0 1 0 0	$m=8, 24, 40, 56$
0 0 1 0 0 0	$m=4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m=1, 3, 5, 7, \dots, 57, 59, 61, 63$

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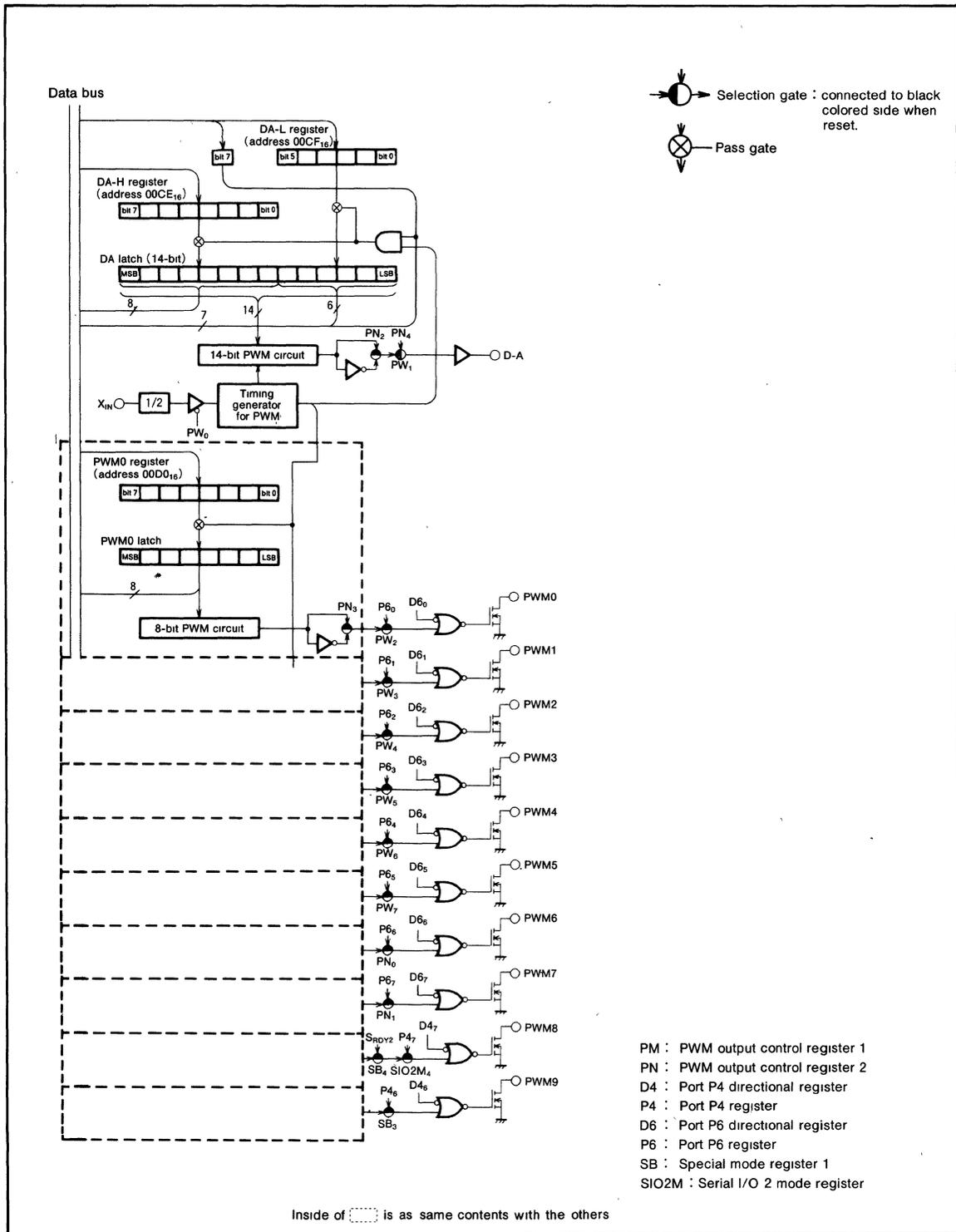


Fig. 16 Block diagram of the PWM circuit

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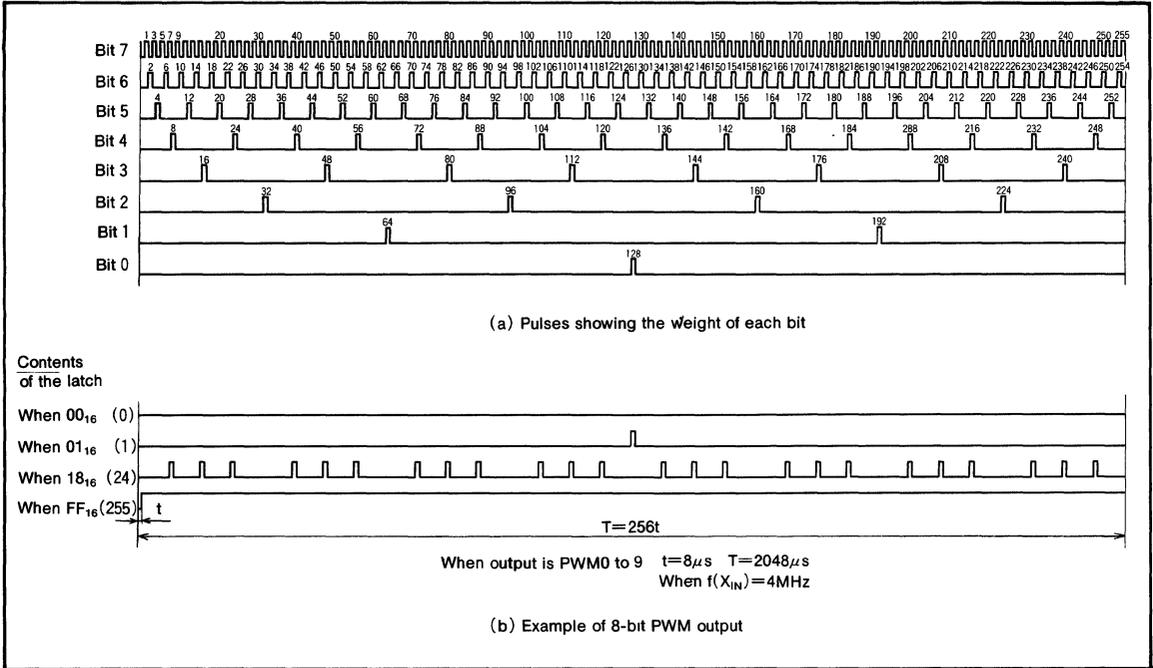


Fig. 17 8-bit PWM timing diagram

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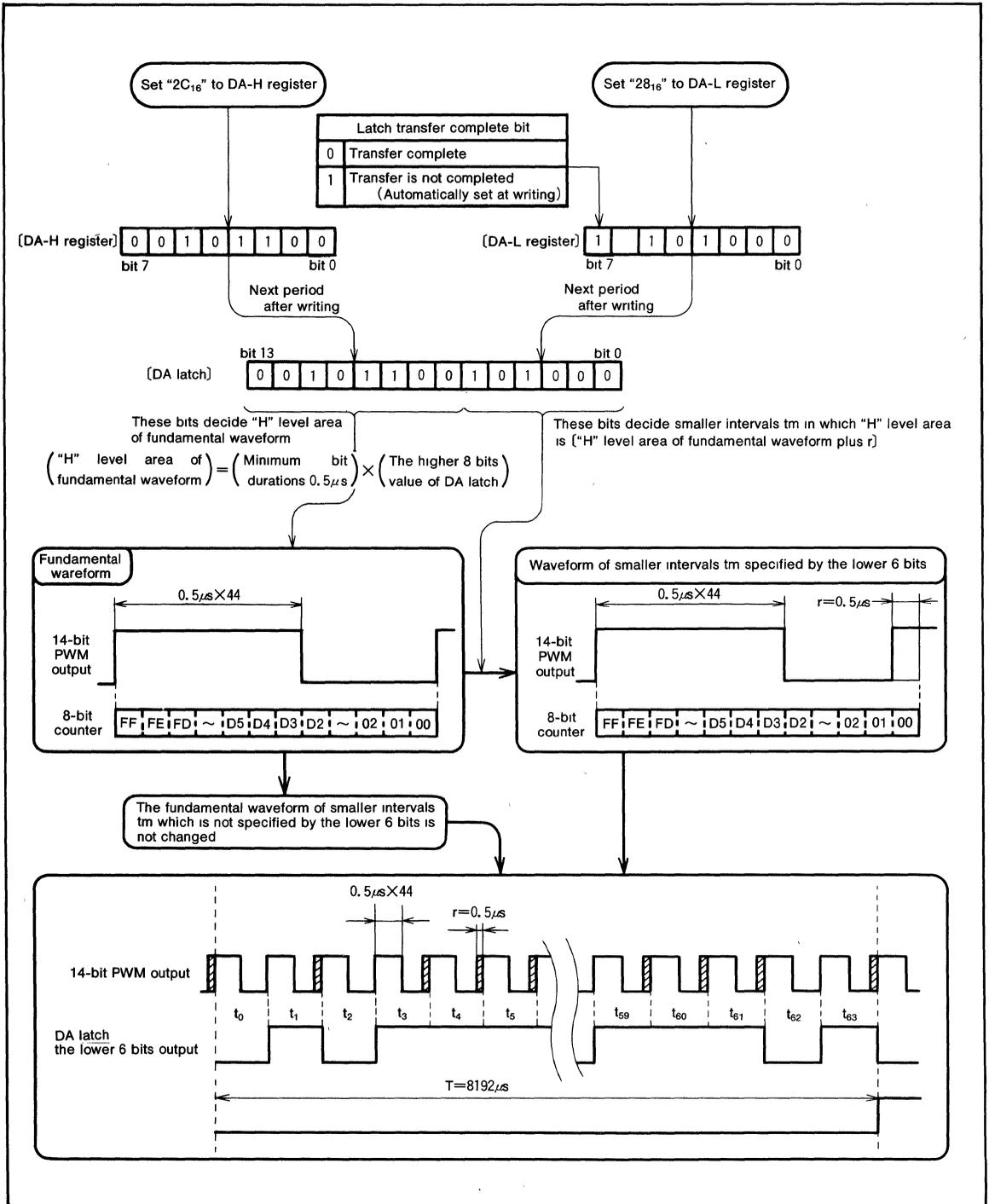


Fig. 18 14-bit PWM output example ($f(X_{IN}) = 4\text{MHz}$)

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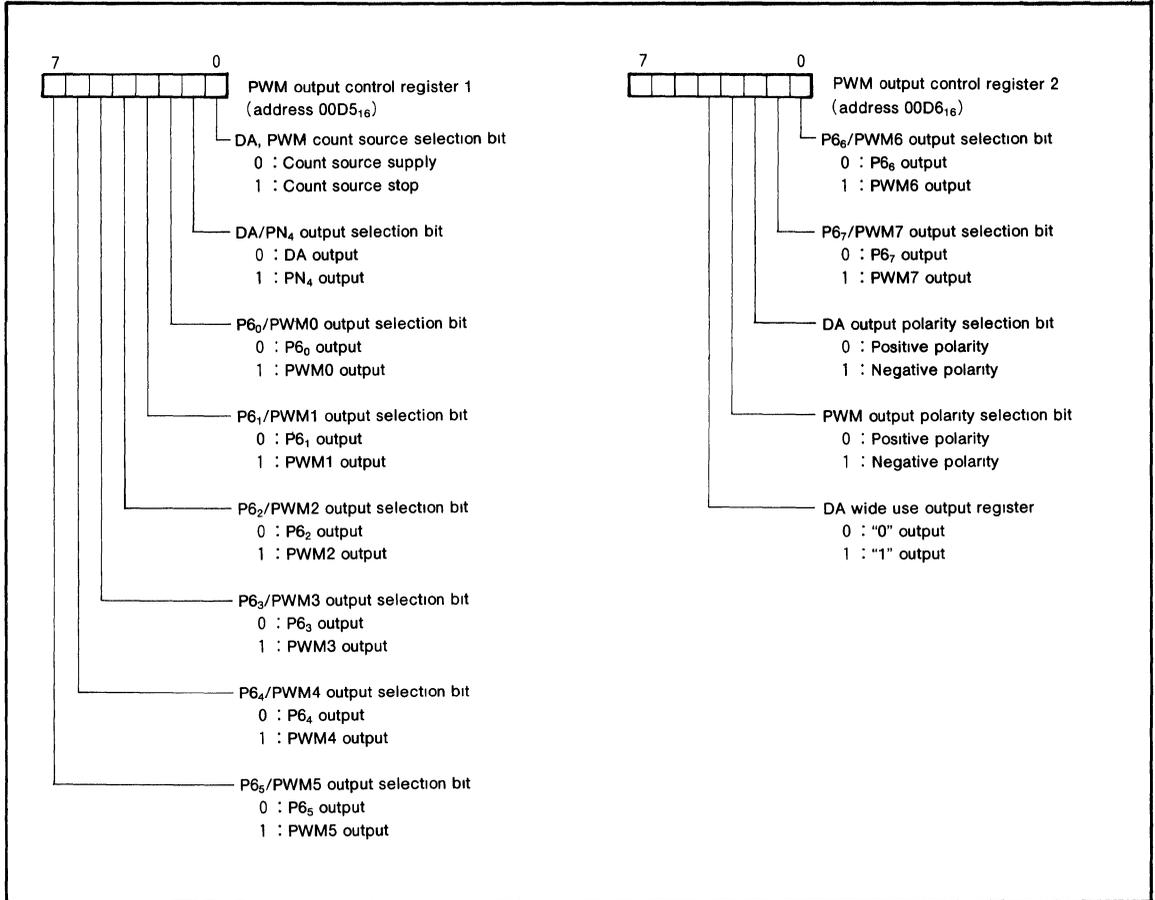


Fig. 19 Structure of PWM output control register 1 and 2

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A-D CONVERTER

Block diagram of A-D converter is shown in Figure 21. A-D converter consists of 4-bit D-A converter and comparator. The A-D control register can generate 1/16 V_{CC} -step internal analog voltage based on the settings of bits 0 to 3.

Table 3 gives the relation between the descriptions of A-D control register bits 0 to 3 and the generated internal analog voltage. The comparison result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 4.

The data is compared by setting the directional register corresponding to port $P3_5$, $P3_6$ to "0" (port $P3_5$, $P3_6$ enters the input mode), to allow port $P3_5/A-D1$, $P3_6/A-D2$ to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register, bit 0 to 3 and an analog input pin is selected. After 16 machine cycle, the voltage comparison starts.

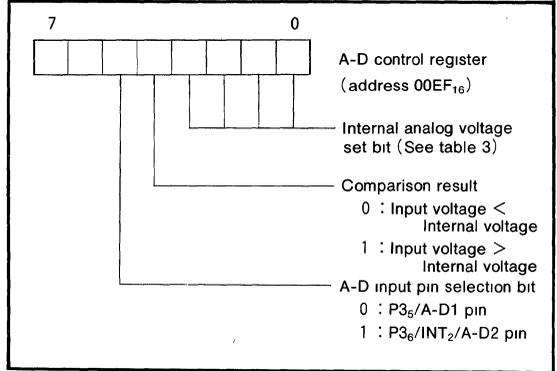


Fig. 20 Structure of A-D control register

Table 3. Relationship between the contents of A-D control register and internal analog voltage

A-D control register				Internal analog voltage
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	1/32 V_{CC}
0	0	0	1	3/32 V_{CC}
0	0	1	0	5/32 V_{CC}
0	0	1	1	7/32 V_{CC}
0	1	0	0	9/32 V_{CC}
0	1	0	1	11/32 V_{CC}
0	1	1	0	13/32 V_{CC}
0	1	1	1	15/32 V_{CC}
1	0	0	0	17/32 V_{CC}
1	0	0	1	19/32 V_{CC}
1	0	1	0	21/32 V_{CC}
1	0	1	1	23/32 V_{CC}
1	1	0	0	25/32 V_{CC}
1	1	0	1	27/32 V_{CC}
1	1	1	0	29/32 V_{CC}
1	1	1	1	31/32 V_{CC}

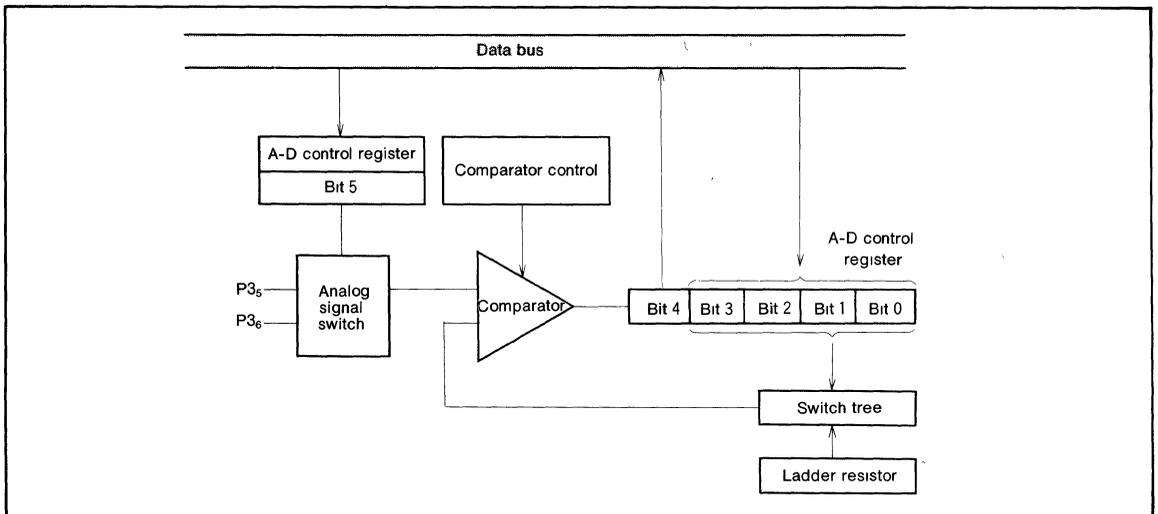


Fig. 21 Block diagram of A-D converter

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 4 outlines the CRT display functions of the M37102M8-XXXSP. The M37102M8-XXXSP incorporates a 24 columns X 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 126 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12 X 16 dot configuration to obtain smooth character patterns. (See Figure 22)

The following shows the procedure how to display characters on the CRT screen.

Table 4. Outline of CRT display functions

Parameter		Functions
Number of display character		24 characters X 3 lines
Character configuration		12 X 16 dots (See Figure 22)
Kinds of character		126
Character size		4 size selectable
Color	Kinds of color	15 (max.)
	Coloring unit	a character
Display expansion		Possible (multiple lines)

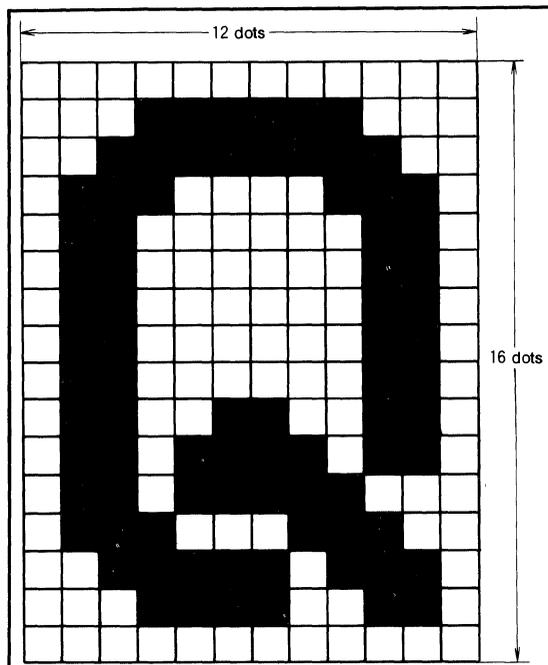
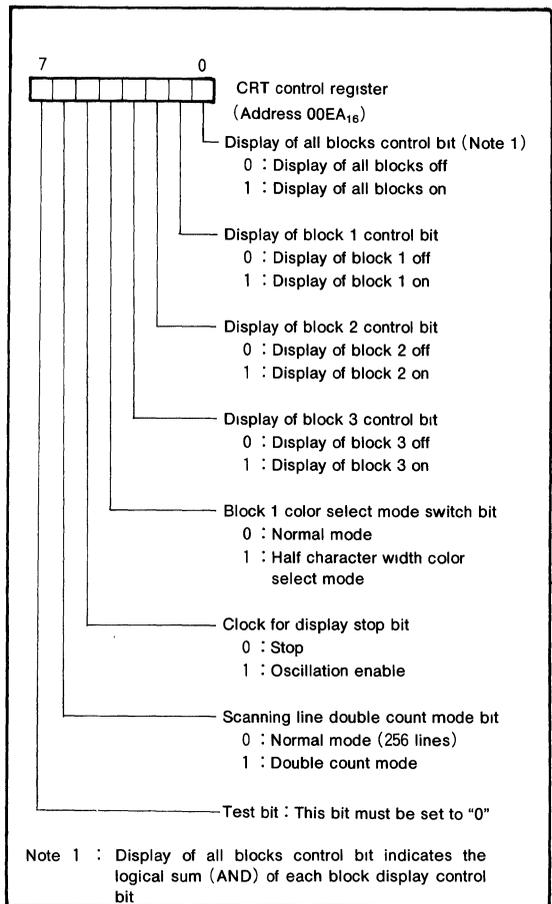


Fig. 22 CRT display character configuration

- ① Set the character to be displayed in display RAM.
- ② Set the display color by using the color register.
- ③ Specify the color register in which the display color is set by using the display RAM.
- ④ Specify the vertical position and character size by using the vertical position register and the character size register.
- ⑤ Specify the horizontal position by using the horizontal position register.
- ⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 24 shows a block diagram of the CRT display control circuit. Figure 23 shows the structure of the CRT display control register.



Note 1 : Display of all blocks control bit indicates the logical sum (AND) of each block display control bit

Fig. 23 Structure of CRT control register

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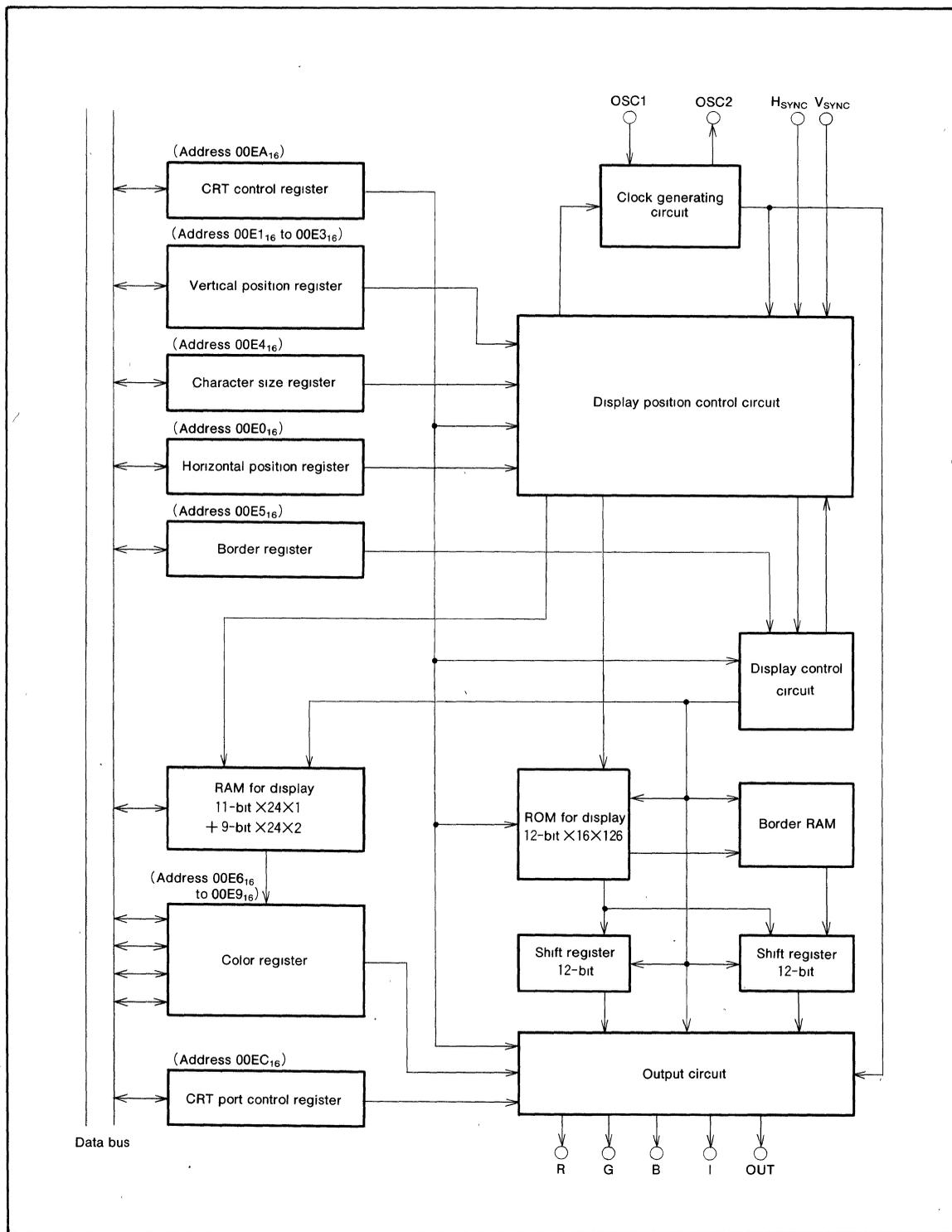


Fig. 24 Block diagram of CRT display control circuit

(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 24 characters can be displayed in one block. (See (4) Display Memory.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of $4T_c$ (T_c = oscillation cycle for display).

The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 27), a block of the smaller block No. (1 to 3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 27), the former block is overridden and the latter is displayed.

The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values 00_{16} to $7F_{16}$ to bits 0 to 6 in the vertical position register (addresses $00E1_{16}$ to $00E3_{16}$). Figure 25 shows the structure of the vertical position register.

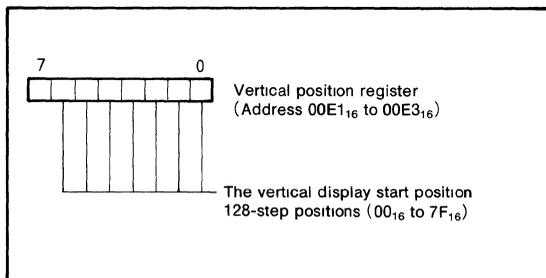


Fig. 25 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64 -step display positions ($4T_c$ per step (T_c = oscillation cycle for display) by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the horizontal position register (address $00E0_{16}$). Figure 26 shows the structure of the horizontal position register.

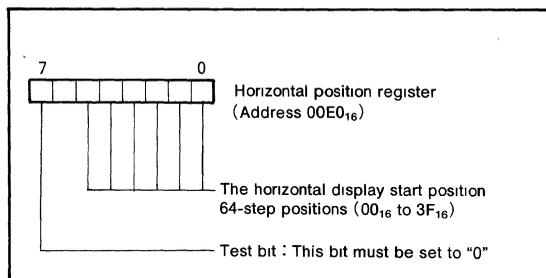
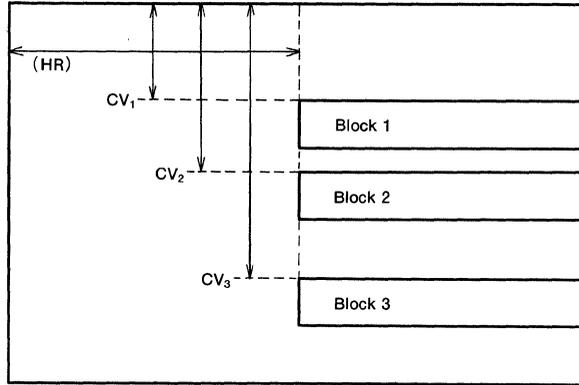
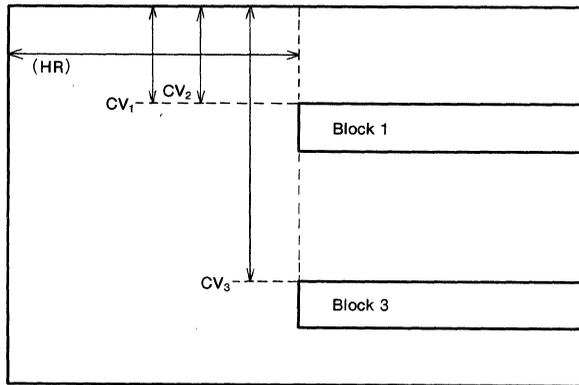


Fig. 26 Structure of horizontal position register

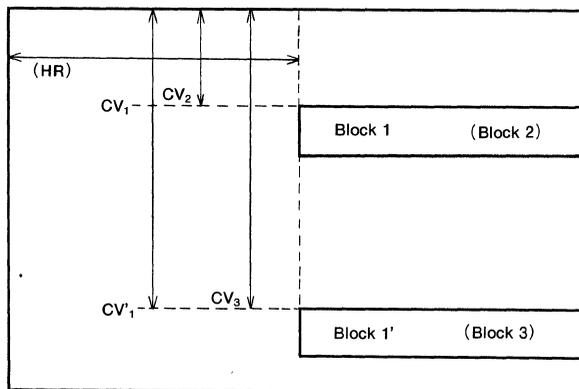
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(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed

Fig. 27 Display position

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(4) Display Memory

There are two types of display memory: ROM of CRT display (3000_{16} to $3FFF_{16}$) used to store character dot data (masked) and display RAM (2000_{16} to $20D7_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① ROM for CRT display (3000_{16} to $3FFF_{16}$)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM.

The CRT display ROM has a capacity of 4K bytes. Because 32 bytes are required for one character data, the ROM can contain up to 128 kinds of characters. Actually, however, because two characters are required for test pattern use, the ROM can contain up to 126 kinds of characters for display use.

The CRT display ROM space is broadly divided into two areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses 3000_{16} to $37FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 3800_{16} to $3FFF_{16}$. (See Figure 30) Note however that the four upper bits in the data to be written to addresses 3800_{16} to $3FFF_{16}$ must be set to "1" (by writing data $F0_{16}$ to FF_{16}).

Table 6. Character code list

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00_{16}	3000_{16} to $300F_{16}$	3800_{16} to $380F_{16}$
01_{16}	3010_{16} to $301F_{16}$	3810_{16} to $381F_{16}$
02_{16}	3020_{16} to $302F_{16}$	3820_{16} to $382F_{16}$
03_{16}	3030_{16} to $303F_{16}$	3830_{16} to $383F_{16}$
:	:	:
10_{16}	3100_{16} to $310F_{16}$	3900_{16} to $390F_{16}$
11_{16}	3110_{16} to $311F_{16}$	3910_{16} to $391F_{16}$
:	:	:
$4F_{16}$	$34F0_{16}$ to $34FF_{16}$	$3CF0_{16}$ to $3CFF_{16}$
50_{16}	3500_{16} to $350F_{16}$	$3D00_{16}$ to $3D0F_{16}$
:	:	:
$7D_{16}$	$37D0_{16}$ to $37DF_{16}$	$3FD0_{16}$ to $3FDF_{16}$
$7E_{16}$ *	$37E0_{16}$ to $37EF_{16}$	$3FE0_{16}$ to $3FEF_{16}$
$7F_{16}$ *	$37F0_{16}$ to $37FF_{16}$	$3FF0_{16}$ to $3FFF_{16}$

* For test pattern

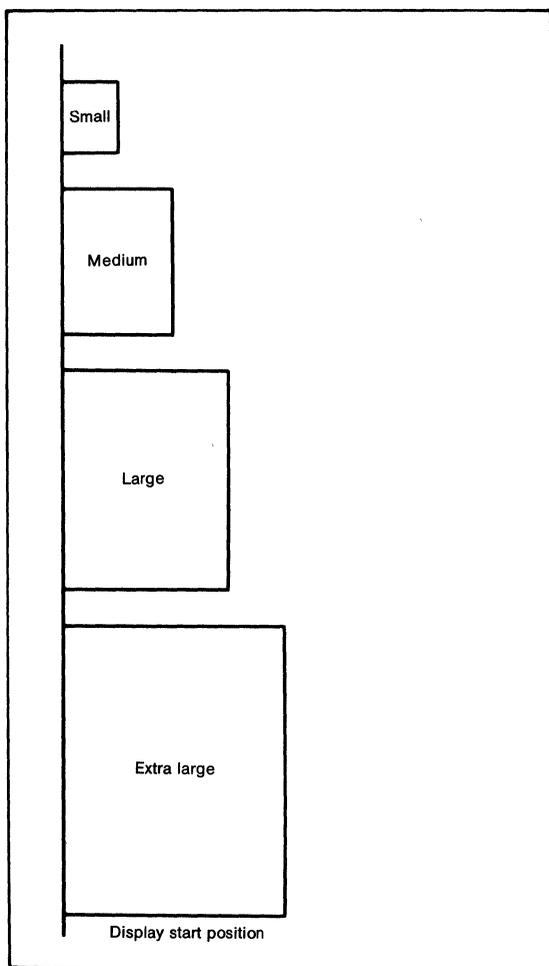


Fig. 29 Display start position of each character size (horizontal direction)

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M37201M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.

Assume that data for one character is stored at $3XX0_{16}$ to $3XXF_{16}$ (XX denotes 00_{16} to $7F_{16}$) and $3YY0_{16}$ to $3YYF_{16}$ (YY denotes 80_{16} to FF_{16}), then the character code for it is "XX₁₆".

In other words, character code for any given character is configured with two middle digits of the four-digit (hex-notated) address (3000_{16} to $37FF_{16}$) where data for that character is stored.

Table 6 lists the character codes.

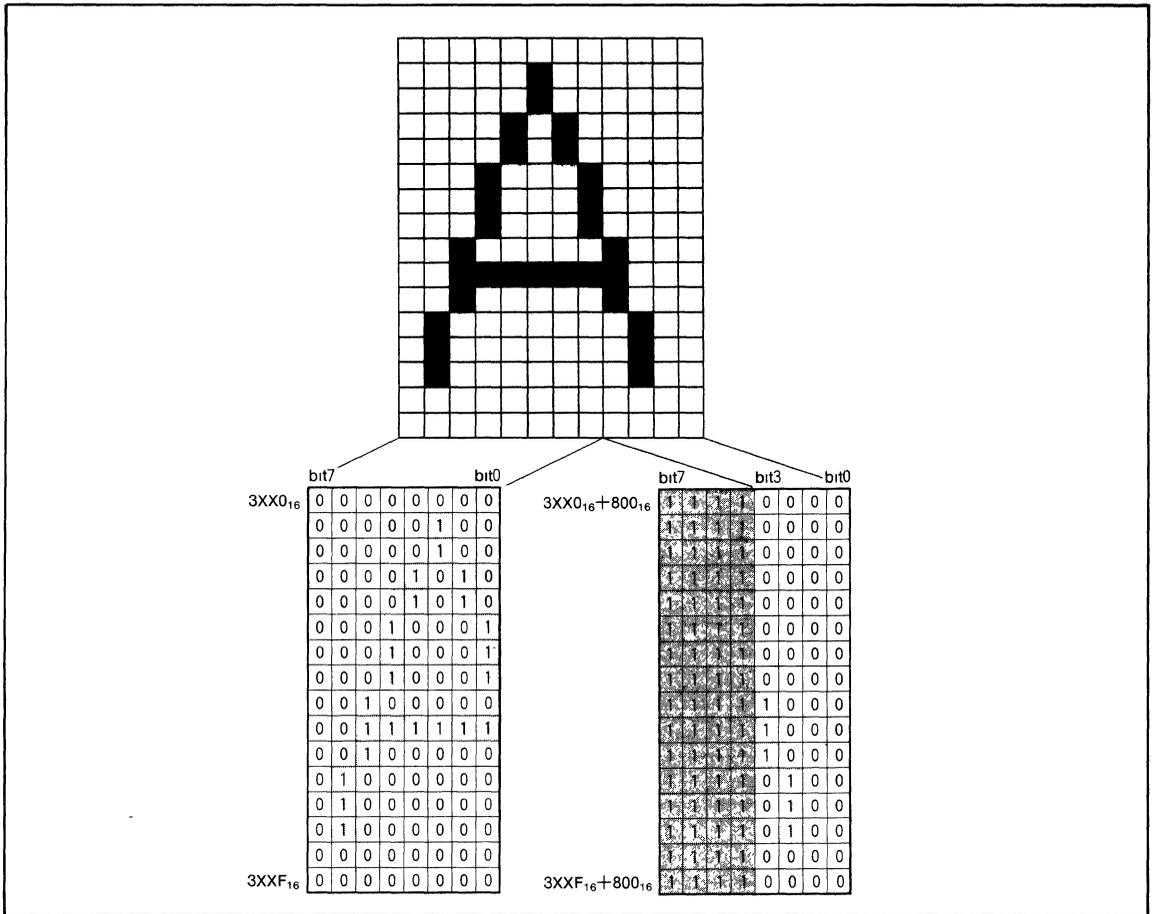


Fig. 30 Display character stored area

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② CRT display RAM (2000₁₆ to 20D7₁₆)

The CRT display RAM is allocated at addresses 2000₁₆ to 20D7₁₆, and is divided into a display character code specifying part and display color specifying part for each block.

Table 7 shows the contents of the CRT display RAM.

When a character is to be displayed at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0 to 6) in address 2000₁₆ and the color register No. to the two low-order bits (bits 0 and 1) in address 2080₁₆. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 30. Write the character patterns at Table 8 and 9, when M37102M8-XXXSP is mask-ordered.

Table 7. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st column	2000 ₁₆	2080 ₁₆
	2nd column	2001 ₁₆	2081 ₁₆
	3rd column	2002 ₁₆	2082 ₁₆
	⋮	⋮	⋮
	22th column	2015 ₁₆	2095 ₁₆
	23th column	2016 ₁₆	2096 ₁₆
	24th column	2017 ₁₆	2097 ₁₆
Not used		2018 ₁₆ to 201F ₁₆	2098 ₁₆ to 209F ₁₆
Block 2	1st column	2020 ₁₆	20A0 ₁₆
	2nd column	2021 ₁₆	20A1 ₁₆
	3rd column	2022 ₁₆	20A2 ₁₆
	⋮	⋮	⋮
	22th column	2035 ₁₆	20B5 ₁₆
	23th column	2036 ₁₆	20B6 ₁₆
	24th column	2037 ₁₆	20B7 ₁₆
Not used		2038 ₁₆ to 203F ₁₆	20B8 ₁₆ to 20BF ₁₆
Block 3	1st column	2040 ₁₆	20C0 ₁₆
	2nd column	2041 ₁₆	20C1 ₁₆
	3rd column	2042 ₁₆	20C2 ₁₆
	⋮	⋮	⋮
	22th column	2055 ₁₆	20D5 ₁₆
	23th column	2056 ₁₆	20D6 ₁₆
	24th column	2057 ₁₆	20D7 ₁₆
Not used		2058 ₁₆ to 207F ₁₆	

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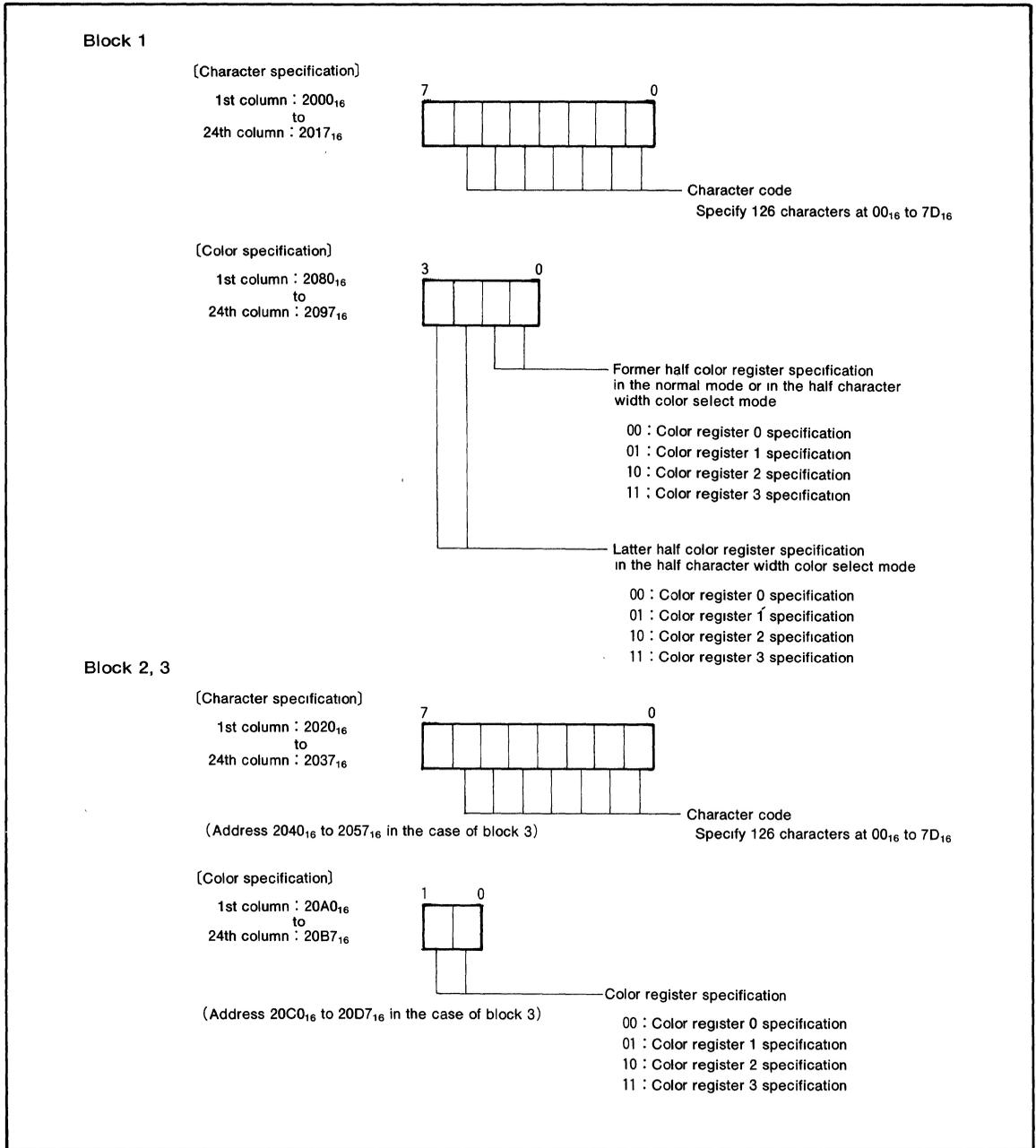


Fig. 31 Structure of the CRT display RAM

Table 8. Test character patterns 1

Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

Table 9. Test character patterns 2

Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3: addresses 00E6₁₆ to 00E9₁₆) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set 2^4-1 (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 32 shows the structure of the color register.

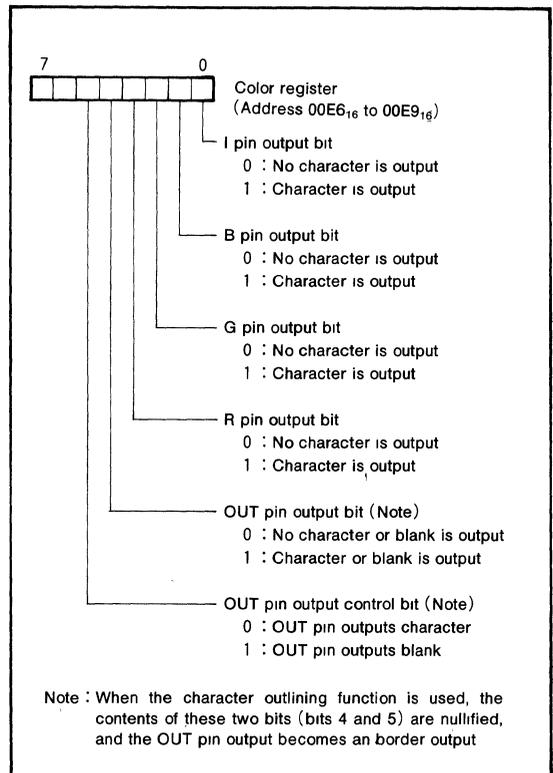


Fig. 32 Structure of color registers

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(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address 00EA₁₆) it is possible to specify colors in units of a half character size (vertical 16 dots×horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

- ① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080₁₆ to 2097₁₆).
- ② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080₁₆ to 2097₁₆).

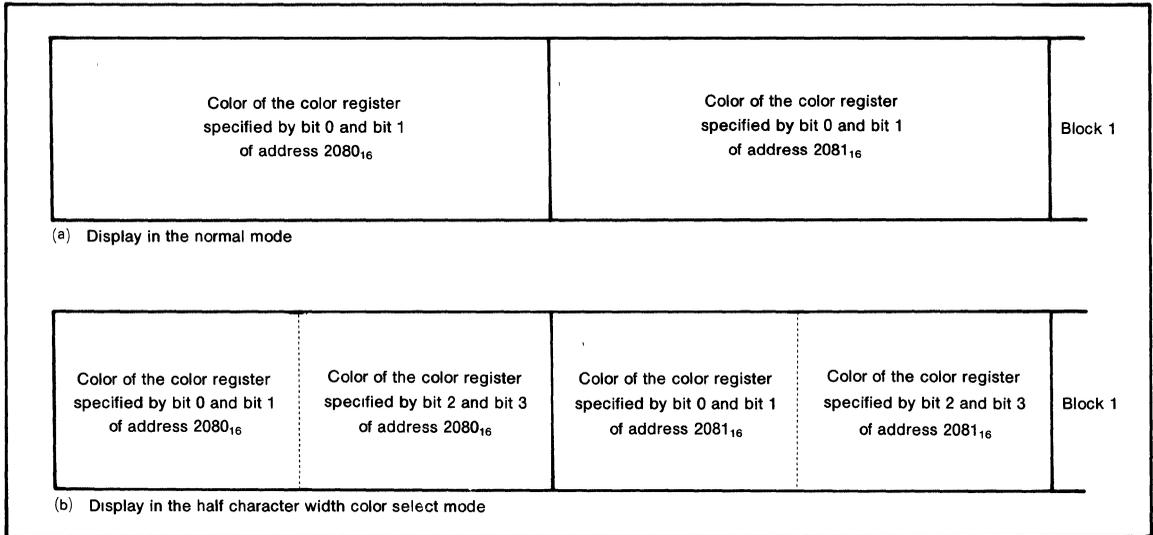


Fig. 33 Difference between normal color select mode and half character width color select mode

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(7) Multiline Display

The M37102M8-XXXSP can normally display three lines on the CRT screen by displaying three blocks at different vertical positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (bit 4 at address 00FE₁₆) to "1"), then execute the following processing in the CRT interrupt handling routine.

- ① Read the value of the display block counter.
- ② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.
- ③ Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and vertical display position (contents of vertical position register) to be displayed next.

Figure 34 shows the structure of the display block counter.

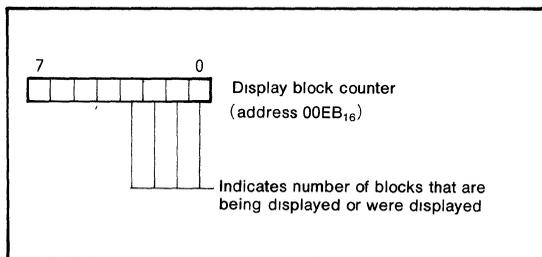


Fig. 34 Structure of display block counter

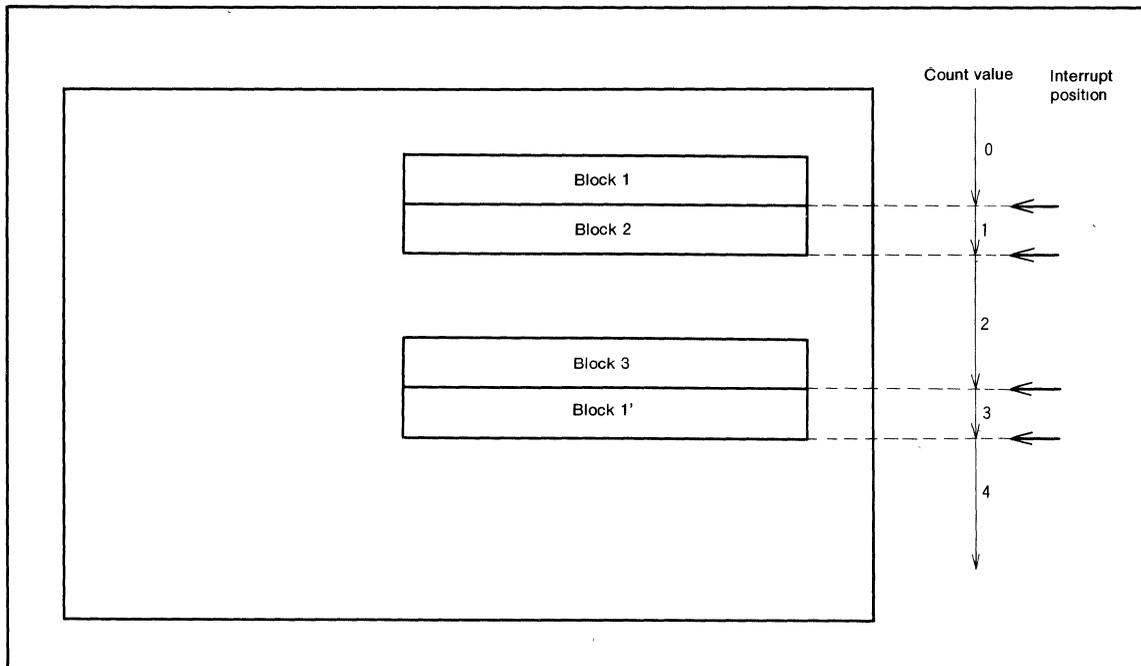


Fig. 35 Timing of CRT interrupt and count value of display block counter

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(8) Scanning Line Double Count Mode

One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended twofold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 128 steps from 00_{16} to $7F_{16}$, or four scanning lines per step, the number of steps in the scanning line double count mode is 64 from 00_{16} to $3F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 40_{16} to $7F_{16}$ in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register (address $00EA_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.

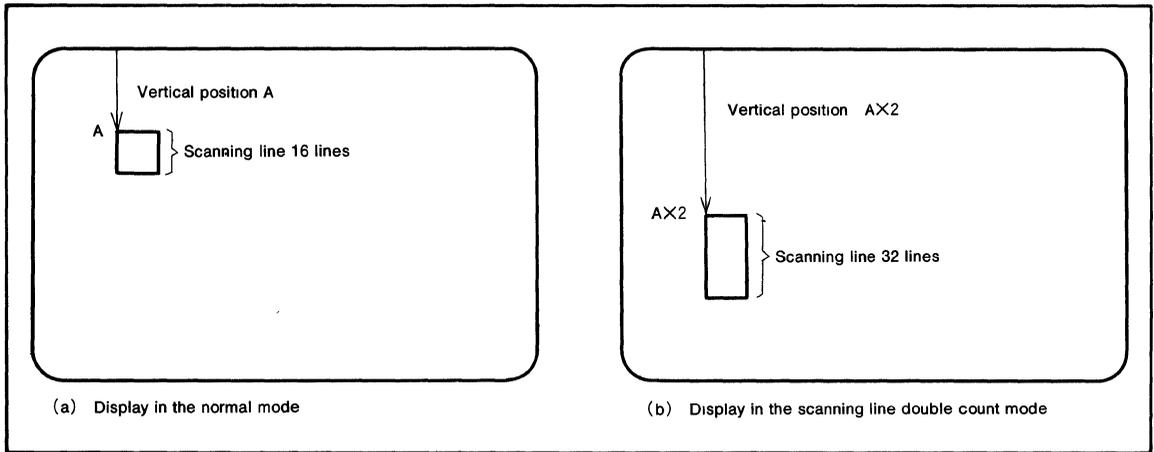


Fig. 36 Display in the normal mode and in the scanning line double count mode

(10) CRT Output Pin Control

CRT output pins R, G, B, I, and OUT are respectively shared with port P5₂, P5₃, P5₄, P5₅, and P5₆. When the corresponding bits in the port P5 direction register are cleared to "0", the pins are set for CRT output; when the bits are set to "1", the pins function as port P5 (general-purpose output pins).

The polarities of CRT outputs (R, G, B, I, and OUT, as well as H_{SYNC} and V_{SYNC}) can be specified by using the CRT port control register (address 00EC₁₆).

Use bits 0 to 4 in the CRT port control register to set the output polarities of H_{SYNC}, V_{SYNC}, R/G/B, I, and OUT. When these bits are cleared to "0", a positive polarity is selected; when the bits are set to "1", a negative polarity is selected. Bits 5 to 7 in the CRT port control register are used to specify pin by pin whether normal video signals or R-MUTE, G-MUTE, and B-MUTE signals are output from each pin (R, G, B). When set for R-MUTE, G-MUTE, and B-MUTE outputs, the whole background colors of the screen become red, green, and blue.

Figure 39 shows the structure of the CRT port control register.

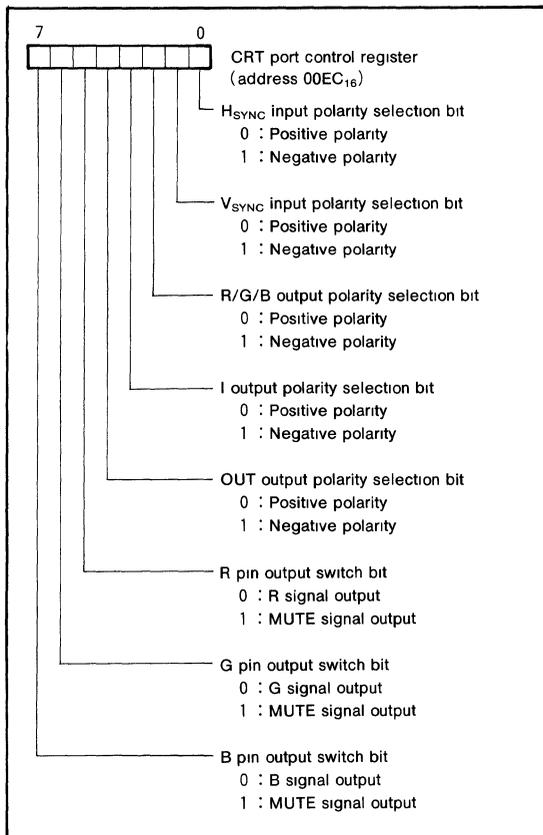


Fig. 39 Structure of CRT port control register

(11) Scroll Function

① Scroll mode

The M37102M8-XXXSP allows the display area to be gradually expanded or shrunk in the vertically direction in units of 1H (H: H_{SYNC} signal). There are three modes for this scroll method. Each mode has Down and UP modes, providing a total of six modes.

Table 11 shows the contents of each scroll mode.

② Scroll speed

The scroll speed is determined by the vertical synchronization (V_{SYNC}) signal. For the NTSC interlace method, assuming that

$$V=16.7\text{ms} \quad 262.5 \text{ H}_{\text{SYNC}} \text{ signals per screen}$$

we obtain the scroll speed as shown in Table 12.

Scroll resolution varies with each scroll mode. In mode 1 and mode 2, one of three resolutions (1H, 2H, 4H) can be selected. In mode 3, scroll is done in units of 4H alone.

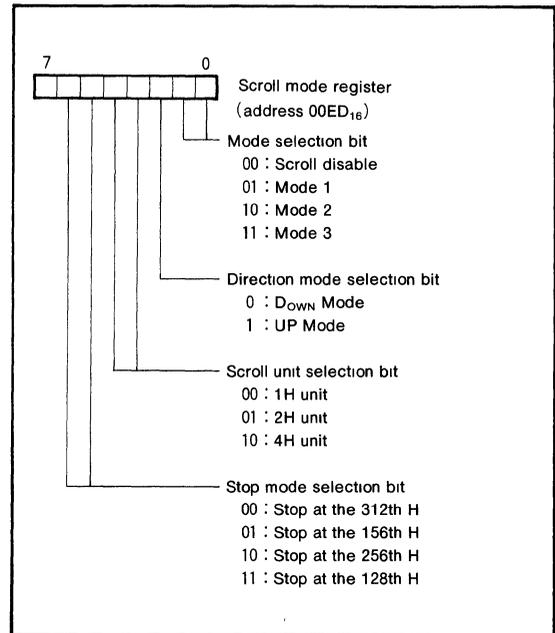


Fig. 40 Structure of scroll mode register

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Table 11. Scroll operation in each mode and the values of scroll mode register

Mode		Scroll operation	Scroll mode register			
			Bit 2	Bit 1	Bit 0	
1	Down	Appear from upper side		0	0	1
	UP	Erase from lower side		1	0	1
2	Down	Erase from upper side		0	1	0
	UP	Appear from lower side		1	1	0
3	Down	Erase from both upper and lower side		0	1	1
	UP	Appear to both upper and lower side		1	1	1

Table 12. Scroll speed

Scroll resolution	Scroll speed (in all picture)
1 H unit	$16.7 \text{ (ms)} \times 262.5 \div 1 \approx 4 \text{ (s)}$
2 H unit	$16.7 \text{ (ms)} \times 262.5 \div 2 \approx 2 \text{ (s)}$
4 H unit	$16.7 \text{ (ms)} \times 262.5 \div 4 \approx 1 \text{ (s)}$

Table 13. Scroll mode and scroll resolution

Mode	Scroll resolution	Scroll speed
Mode 1	1 H Unit	about 4 second
Mode 2	2 H Unit	about 2 second
	4 H Unit	about 1 second
Mode 3	4 H Unit	about 1 second

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INTERRUPT INTERVAL DETERMINATION FUNCTION

The M37102M8-XXXSP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary counter as shown in Figure 41. Using this counter, it determines a duration of time from the rising transition (falling transition) of an input signal pulse on the INT₁ or INT₂ to the rising transition (falling transition) of the signal pulse that is input next.

The following describes how the interrupt interval is determined.

1. The interrupt input to be determined (INT₁ input or INT₂ input) is selected by using bit 2 in the interrupt interval determination control register (address 00D8₁₆). When this bit is cleared to "0", the INT₁ input is selected; when the bit is set to "1", the INT₂ input is selected.
2. When the INT₁ input is to be determined, the polarity is selected by using bit 3 in the interrupt interval determination control register; when the INT₂ input is to be determined, the polarity is selected by using bit 4 in the interrupt interval determination control register. When the relevant bit is cleared to "0", determination is made of the interval of a positive polarity (rising

transition); when the bit is set to "1", determination is made of the interval of a negative polarity (falling transition).

3. The reference clock is selected by using bit 1 in the interrupt interval determination control register. When the bit is cleared to "0", a 64 μ s clock is selected; when the bit is set to "1", a 32 μ s clock is selected (based on an oscillation frequency of 4MHz in either case).
4. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT₁ pin (or INT₂ pin), the 8-bit binary counter starts counting up with the selected reference clock (64 μ s or 32 μ s).
5. Simultaneously with the next input pulse, the value of the 8-bit binary counter is loaded into the determination register (address 00D7₁₆) and the counter is immediately reset (00₁₆). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "00₁₆".
6. When count value "FE₁₆" is reached, the 8-bit binary counter stops counting. Then, simultaneously when the reference clock is input next, the counter sets value "FF₁₆" to the determination register.

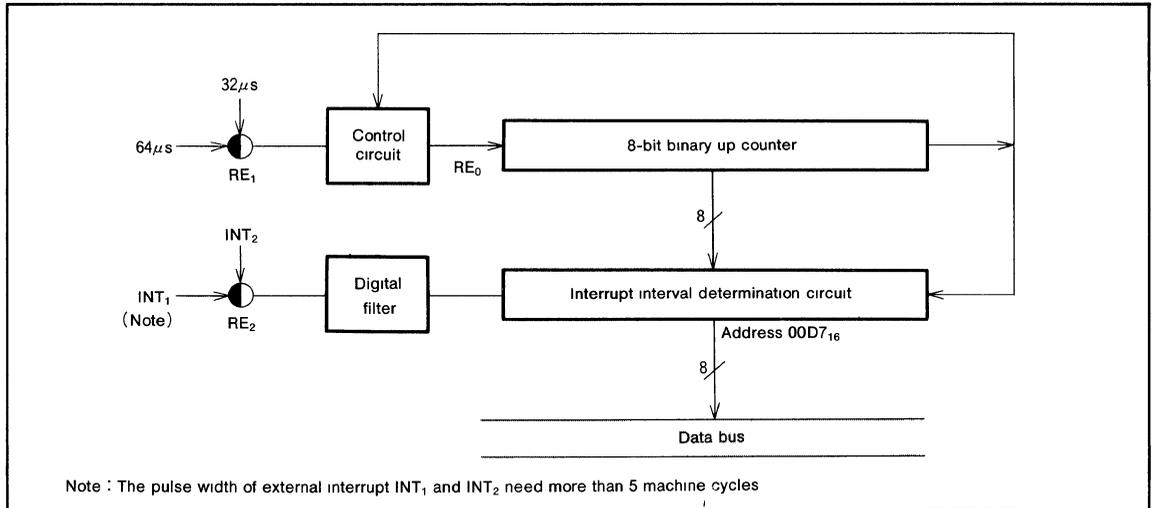


Fig. 41 Block diagram of interrupt interval determination circuit

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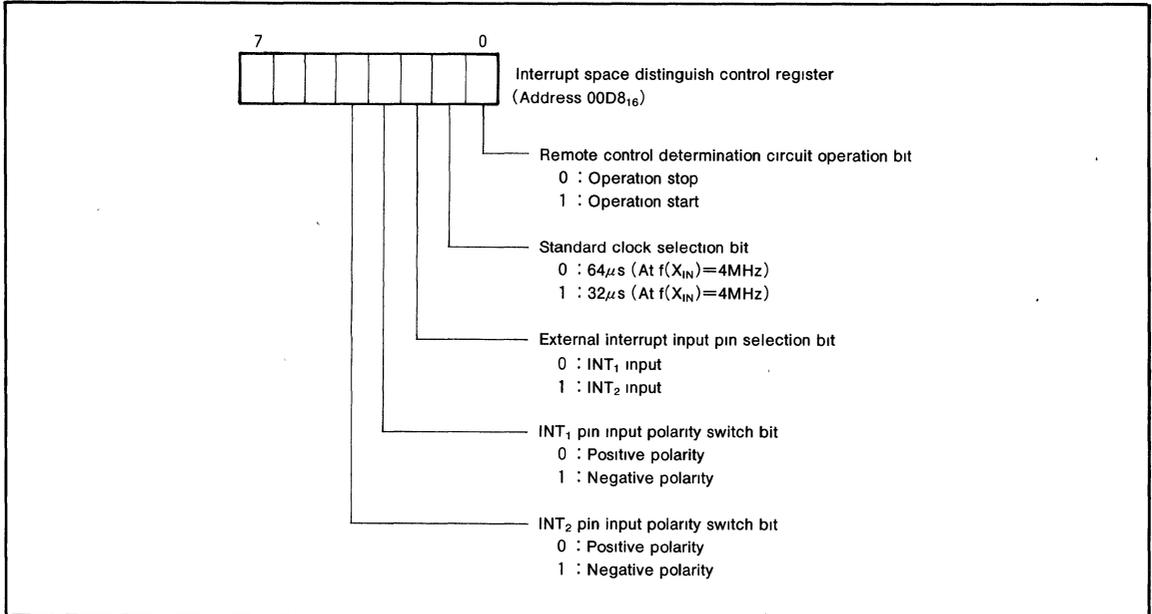


Fig. 42 Structure of interrupt space distinguish control register

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RESET CIRCUIT

The M37102M8-XXXSP is reset according to the sequence shown in Figure 45. It starts the program from the address formed by using the content of address FFFF₁₆ as the high order address and the content of the address FFFE₁₆ as the low order address, when the RESET pin is held at "L" level for no less than 2μs while the power voltage is 5V ± 10%

	Address	
(1) Port P0 directional register	(00C1 ₁₆)	00 ₁₆
(2) Port P1 directional register	(00C3 ₁₆)	00 ₁₆
(3) Port P2 directional register	(00C5 ₁₆)	00 ₁₆
(4) Port P3 directional register	(00C7 ₁₆)	00000000
(5) Port P4 directional register	(00C9 ₁₆)	00 ₁₆
(6) Port P5 directional register	(00CB ₁₆)	00000000
(7) Port P6 directional register	(00CD ₁₆)	00 ₁₆
(8) PWM output control register 1	(00D5 ₁₆)	00 ₁₆
(9) PWM output control register 2	(00D6 ₁₆)	00000000
(10) Interrupt space distinguish register	(00D7 ₁₆)	00 ₁₆
(11) Interrupt space distinguish control register	(00D8 ₁₆)	00 ₁₆
(12) Special mode register 1	(00DA ₁₆)	00 ₁₆
(13) Special mode register 2	(00DB ₁₆)	00 ₁₆
(14) Serial I/O1 mode register	(00DC ₁₆)	00000000
(15) Serial I/O2 mode register	(00DE ₁₆)	00000000
(16) Horizontal position register	(00E0 ₁₆)	00000000
(17) Color register 0	(00E6 ₁₆)	00000000
(18) Color register 1	(00E7 ₁₆)	00000000
(19) Color register 2	(00E8 ₁₆)	00000000
(20) Color register 3	(00E9 ₁₆)	00000000
(21) CRT control register	(00EA ₁₆)	00 ₁₆
(22) Display block counter	(00EB ₁₆)	000000
(23) CRT port control register	(00EC ₁₆)	00 ₁₆
(24) Scroll control register	(00ED ₁₆)	00000000
(25) A-D control register	(00EF ₁₆)	00000000
(26) Timer 1	(00F0 ₁₆)	FF ₁₆
(27) Timer 2	(00F1 ₁₆)	07 ₁₆
(28) Timer 3	(00F2 ₁₆)	FF ₁₆
(29) Timer 4	(00F3 ₁₆)	07 ₁₆
(30) Timer 12 mode register	(00F4 ₁₆)	00000000
(31) Timer 34 mode register	(00F5 ₁₆)	00000000
(32) CPU mode register	(00FB ₁₆)	11111100
(33) Interrupt request register 1	(00FC ₁₆)	00000000
(34) Interrupt request register 2	(00FD ₁₆)	00000000
(35) Interrupt control register 1	(00FE ₁₆)	00000000
(36) Interrupt control register 2	(00FF ₁₆)	00000000
(37) Processor status register	(PS)	1
(38) Program counter	(PC _H)	Contents of address FFFF ₁₆
	(PC _L)	Contents of address FFFE ₁₆

Note : Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values
 At reset, "0" is read from all bits which is not used

Fig. 43 Internal state of microcomputer at reset

and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 43.

An example of the reset circuit is shown in Figure 44. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

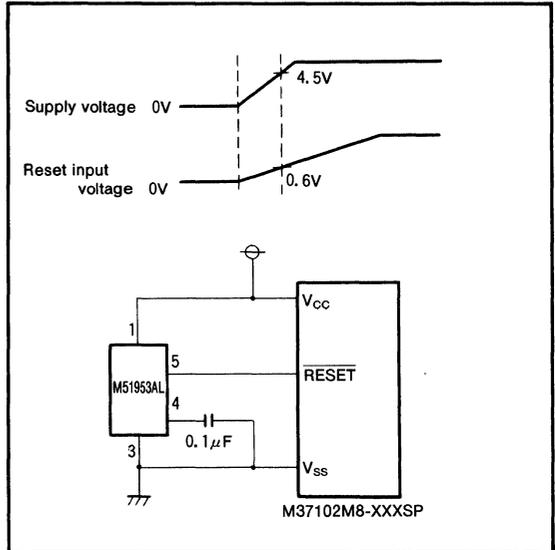


Fig. 44 Example of reset circuit

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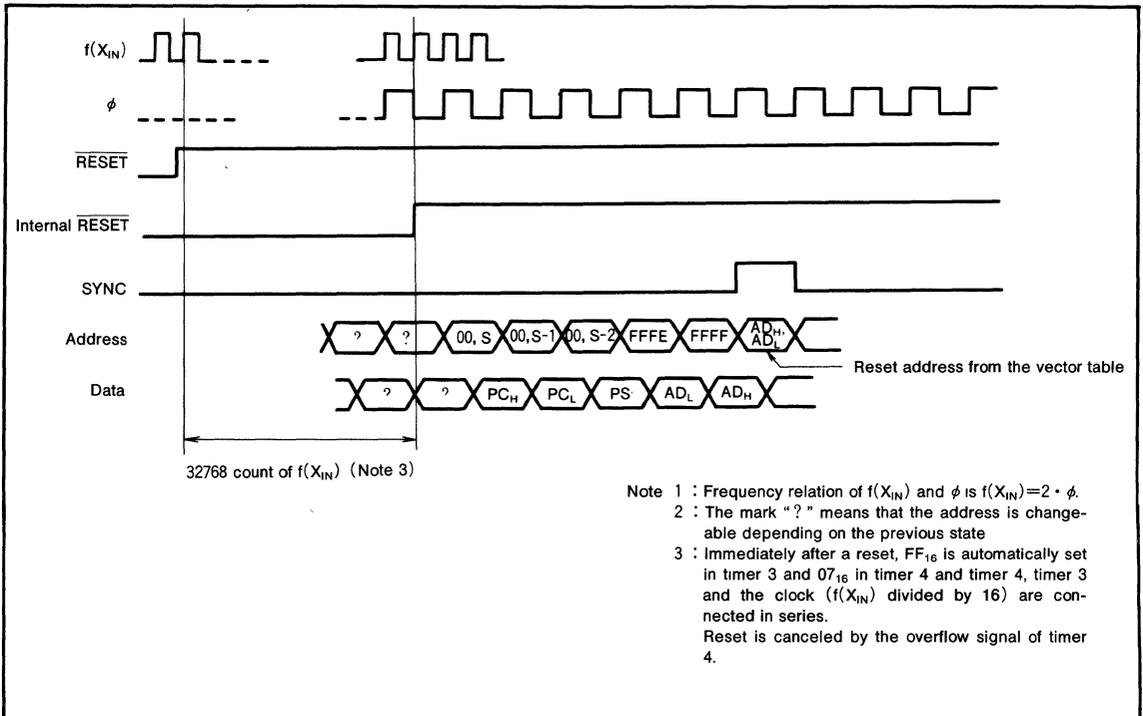


Fig. 45 Timing diagram at reset

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I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 3), port P0 can be accessed at zero page memory address 00C0₁₆.

Port P0 has a directional register (address 00C1₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address 00FB₁₆), three different modes can be selected; single-chip mode, memory expansion mode and microprocessor mode.

In these modes it functions as address (A₇-A₀) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A₁₅-A₈) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data (D₀-D₇) input/output port. Refer to the section on processor modes for details.

(4) Port P3

Port P3 is an 7-bit I/O port with function similar to port P0, but the output structure of P3₀, P3₁ is CMOS output and P3₂-P3₆ is N-channel open drain.

P3₂, P3₃ are in common with the external clock input pins of timer 2 and 3.

P3₄, P3₆ are in common with the external interrupt input pins INT₁, INT₂ and P3₅, P3₆ with the analog input pins of A-D converter A-D₁, A-D₂.

In the microprocessor mode or the memory expanding mode, P3₀, P3₁ works as R/W signal output pin and SYNC signal output pin.

(5) Port P4

Port P4 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

All pins have program selectable dual functions. When a serial I/O 1 function is selected, P4₀-P4₃ work as input/output pins of serial I/O1. When a serial I/O2 function is selected, P4₄-P4₇ work as input/output pins of serial I/O2.

In the special serial I/O mode, P4₄, P4₅ work as SDA, SCL pins. P4₆, P4₇ are in common with PWM8 and 9 output pins.

(6) OSC1, OSC2 pins

Clock input/output pins for CRT display function

(7) H_{SYNC}, V_{SYNC} pins

H_{SYNC} is a horizontal synchronizing signal input pin for CRT display.

V_{SYNC} is a vertical synchronizing signal input pin for CRT display.

(8) R, G, B, I, OUT pins

This is an 5-bit output pin for CRT display and in common with P5₂-P5₆.

(9) Port P6

Port P6 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

This port is in common with 8-bit PWM output pin PWM0-PWM7.

(10) D-A pin

This is a 14-bit PWM output pin.

(11) ϕ pin

The internal system clock (1/4 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

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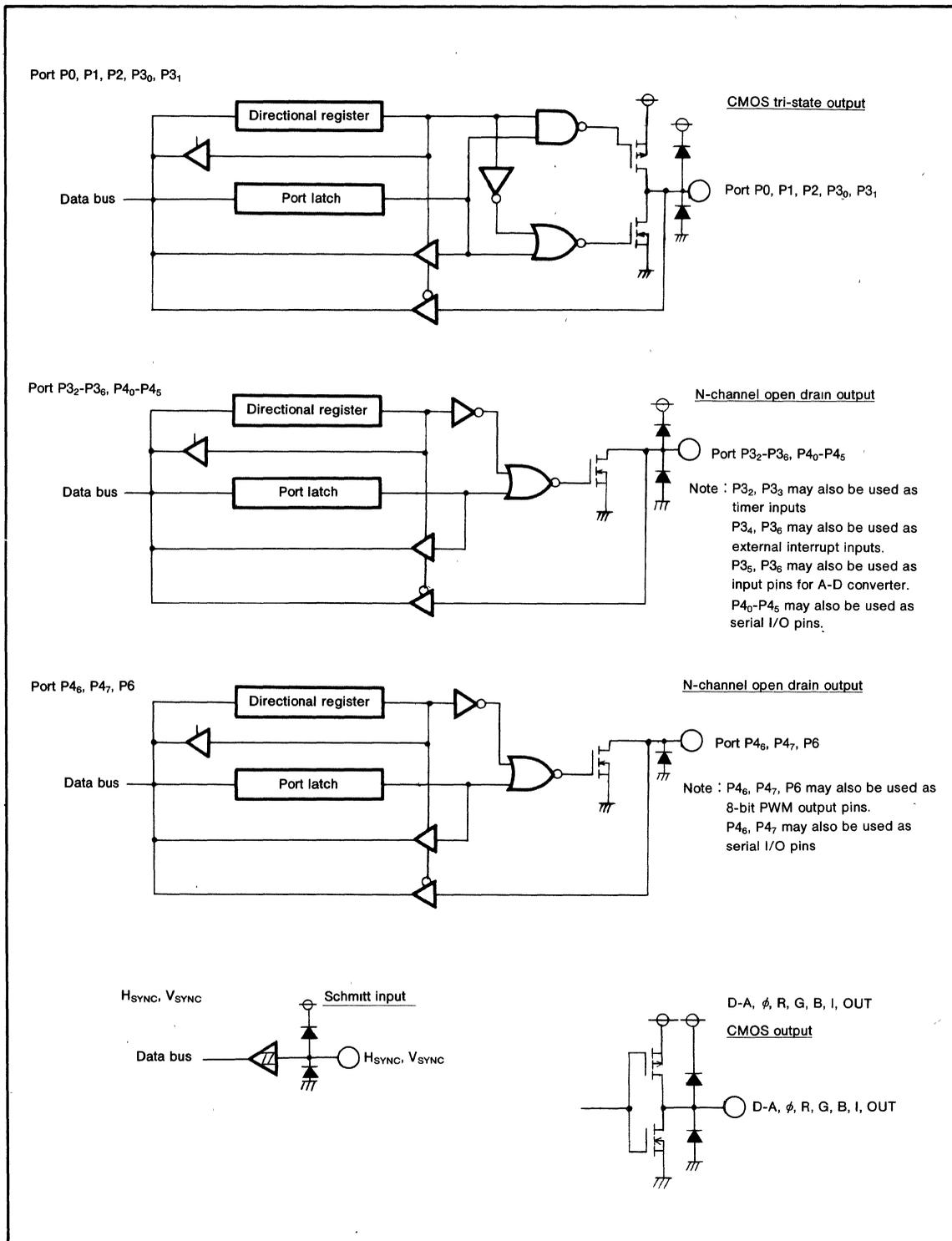


Fig. 46 Block diagram of ports P0-P6 (single-chip mode) and output format of D-A, ϕ , R, G, B, I OUT

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PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address 00FB₁₆), three different operation modes can be selected; single-chip mode, memory expansion mode, and microprocessor mode.

In the memory expansion mode and the microprocessor mode, ports P0-P3 can be used as address, and data input/output pins.

Figure 48 shows the functions of ports P0-P3.

The memory map for the single-chip mode is shown in Figure 2 and for other modes, in Figure 47.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the M37102M8-XXXSP/FP into memory expansion mode. Connecting CNV_{SS} to V_{CC} automatically forces the M37201M6-

XXXSP into microprocessor mode.

The three different modes are explained as follows:

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0-P3 will work as original I/O ports.

(2) Memory expansion mode [01]

The microcomputer will be placed in the memory expansion mode after connecting CNV_{SS} to V_{CC} and initiating a reset or connecting CNV_{SS} to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and its I/O port function is lost.

Port P2 becomes the data bus of D₇-D₀ (including instruction code) and loses its I/O port function. Port P₃₀ and P₃₁ works as R/W and φ.

(3) Microprocessor mode [10]

When CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "10", the microcomputer will automatically default to microprocessor mode. In this mode, the internal ROM is inhibited so the external memory is required. Other functions are same as the memory expansion mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 14.

Note : Use the M37102M8-XXXSP in the microprocessor mode or the memory expansion mode only at program development.

The standards is assured only in the single-chip mode.

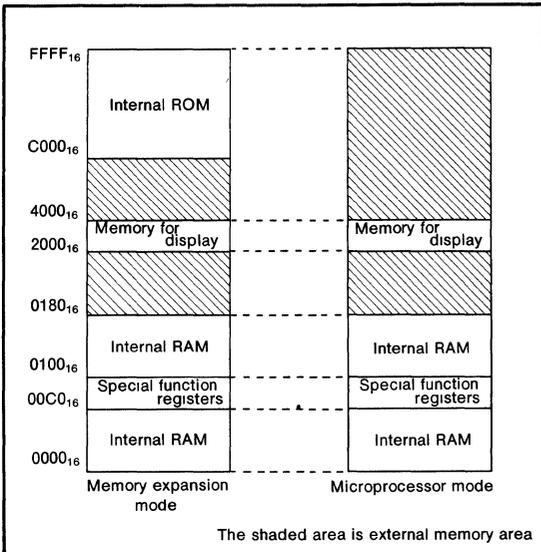


Fig. 47 External memory area at each processor mode

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Port	CM ₁	0	0	1
	CM ₀	0	1	0
	Mode	Single-chip mode	Memory expansion mode	Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P3			Same as left	

Fig. 48 Processor mode and function of port P0-P3

Table 14. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode • Memory expansion mode • Microprocessor mode 	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V _{CC}	<ul style="list-style-type: none"> • Memory expansion mode • Microprocessor mode 	The memory expansion mode is set by the reset (M37102M8-XXXSP/FP) The microprocessor mode is set by the reset (M37201M6-XXXSP)

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CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 51.

When an-STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timer 3 and timer 4 are connected automatically and FF_{16} is set in the timer 3, 07_{16} is set in the timer 4, and timer 3 count source is forced to $f(X_{IN})$ divided by 16. This connection is cleared when an external interrupt is accepted or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 49.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 50
 X_{IN} is the input, and X_{OUT} is open.

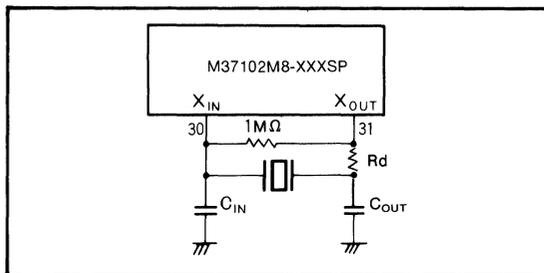


Fig. 49 External ceramic resonator circuit

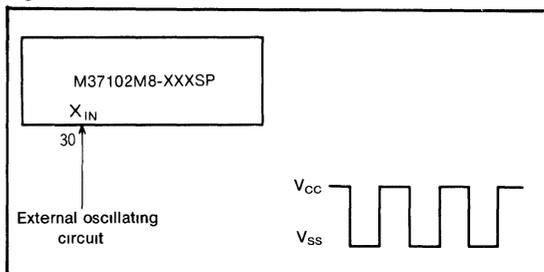


Fig. 50 External clock input circuit

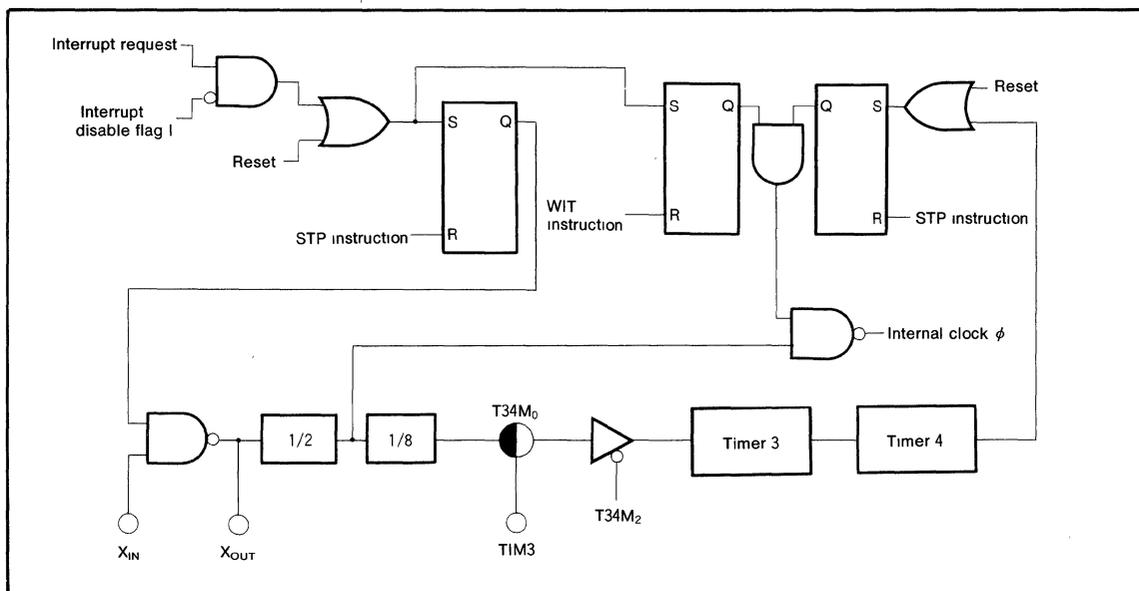


Fig. 51 Block diagram of clock generating circuit

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PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (4) An NOP instruction must be used after the execution of a PLP instruction.
- (5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM order confirmation form
- (2) mask specification form
- (3) ROM data EPROM 3 sets

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS} Output transistors are at "off" state	-0.3 to 6	V
V _I	Input voltage CNV _{SS}		-0.3 to 6	V
V _I	Input voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₇ , P6 ₀ -P6 ₇ , H _{SYNC} , V _{SYNC} , RESET		-0.3 to V _{CC} +0.3	V
V _O	Output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₅ , R, G, B, I, OUT, D-A, X _{OUT} , OSC2		-0.3 to V _{CC} +0.3	V
V _O	Output voltage P4 ₆ , P4 ₇ , P6 ₀ -P6 ₇		-0.3 to 13	V
I _{OH}	Circuit current R, G, B, I, OUT, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₃ , P3 ₀ , P3 ₁ , D-A		0 to 1 (Note 1)	mA
I _{OL1}	Circuit current R, G, B, I, OUT, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₃ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₃ , D-A		0 to 2 (Note 2)	mA
I _{OL2}	Circuit current P6 ₀ -P6 ₇ , P4 ₆ , P4 ₇		0 to 1 (Note 2)	mA
I _{OL3}	Circuit voltage P2 ₄ -P2 ₇		0 to 10 (Note 3)	mA
I _{OL4}	Circuit current P4 ₄ , P4 ₅		0 to 3 (Note 2)	mA
P _d	Power dissipation	T _a =25°C	550	mW
T _{opr}	Operating temperature		-10 to 70	°C
T _{stg}	Storage temperature		-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=-10 to 70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage (Note 4) During the CRT operation	4.5	5.0	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	"H" input voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₃ , P4 ₆ , P4 ₇ , P6 ₀ -P6 ₇ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P4 ₄ , P4 ₅	0.7V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ , P3 ₁ , P3 ₅ , P4 ₀ , P4 ₃ -P4 ₅ , P4 ₇	0		0.4V _{CC}	V
V _{IL}	"L" input voltage P3 ₂ -P3 ₄ , P3 ₆ , P4 ₁ , P4 ₂ , P4 ₆ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0		0.2V _{CC}	V
I _{OH}	"H" average output current (Note 1) R, G, B, I, OUT, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ , P3 ₁			1	mA
I _{OL1}	"L" average output current (Note 2) R, G, B, I, OUT, P0 ₀ -P0 ₇ , P2 ₀ -P2 ₃ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₃ , D-A			2	mA
I _{OL2}	"L" average output current (Note 2) P6 ₀ -P6 ₇ , P4 ₆ , P4 ₇			1	mA
I _{OL3}	"L" average output current (Note 3) P2 ₄ -P2 ₇			10	mA
I _{OL4}	"L" average output current (Note 2) P4 ₄ , P4 ₅			3	mA
f _{CPU}	Oscillating frequency (for CRT operation) (Note 5)	3.6	4.0	4.4	MHz
f _{CRT}	Oscillating frequency (for CRT display)	6.0	7.0	8.0	MHz
f _{HS}	Input frequency P3 ₂ -P3 ₄ , P3 ₆ , P4 ₅			100	kHz
f _{HS}	Input frequency P4 ₁			1	MHz

- Note 1 : The total current that flows out of the IC should be 20mA (max.)
 2 : The total of I_{OL1}, I_{OL2} and I_{OL4} should be 30mA (max.)
 3 : The total of I_{OL} of port P2₄-P2₇ should be 20mA (max.)
 4 : Apply 0.022μF or greater capacitance externally between the V_{CC}-V_{SS} power supply pins so as to reduce power source noise
 Also apply 0.068μF or greater capacitance externally between the V_{CC}-CNV_{SS} pins
 5 : Use the crystal oscillator or ceramic resonator for CPU oscillation circuit

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ELECTRIC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10$ to $70^\circ C$, $f(X_{IN})=4MHz$ unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max.	
I_{CC}	Supply current	$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT OFF		10	20	mA
		$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT ON		20	30	
		At stop mode			300	μA
V_{OH}	"H" output voltage $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0$, $P3_1$, R, G, B, I, OUT	$V_{CC}=4.5V$ $I_{OH}=-0.5mA$	2.4			V
V_{OL}	"L" output voltage $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_3$, $P3_0-P3_6$, $P4_0-P4_3$, R, G, B, I, OUT, D-A	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
	"L" output voltage $P6_0-P6_7$, $P4_6$, $P4_7$	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	
	"L" output voltage $P2_4-P2_7$	$V_{CC}=4.5V$ $I_{OL}=10mA$			3.0	
	"L" output voltage $P4_4$, $P4_5$	$V_{CC}=4.5V$ $I_{OL}=3mA$			0.4	
$V_{T+}-V_{T-}$	Hysteresis RESET	$V_{CC}=5.0V$		0.5	0.7	V
	Hysteresis (Note 1) H_{SYNC} , V_{SYNC} , $P3_2-P3_4$, $P3_6$, $P4_1$, $P4_2$, $P4_4-P4_6$	$V_{CC}=5.0V$		0.5	1.3	
I_{OZH}	"H" input leak current RESET, $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0-P3_6$, $P4_0-P4_5$	$V_{CC}=5.5V$ $V_O=5.5V$			5	μA
	"H" input leak current $P6_0-P6_7$, $P4_6$, $P4_7$	$V_{CC}=5.5V$ $V_O=12V$			10	
I_{OZL}	"L" input leak current RESET, $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0-P3_6$, $P4_0-P4_7$, $P6_0-P6_7$	$V_{CC}=5.5V$ $V_O=0V$			5	μA

Note 1. $P3_2-P3_4$, $P3_6$ have the hysteresis when these pins are used as interrupt input pins or timer input pins
 $P4_1$, $P4_2$, $P4_4-P4_6$ have the hysteresis when these pins are used as serial I/O ports.

MITSUBISHI MICROCOMPUTERS
M37103M4-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

DISCRIPTION

The M37103M4-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This single-chip microcomputer is useful for the high-tech channel-selection system for TVs.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

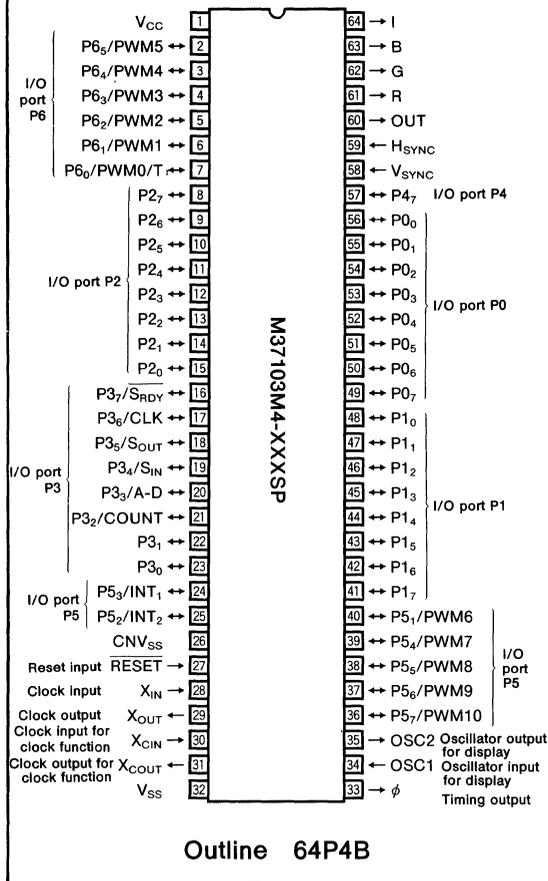
FEATURES

- Number of basic instructions..... 69
- Memory size
 - ROM 8192 bytes
 - RAM 192 bytes
- Instruction execution time
 - 2 μ s (minimum instructions at 4MHz frequency)
- Single power supply 5V \pm 10%
- Power dissipation
 - normal operation mode (at 4MHz frequency)
 - 35mW (V_{CC}=5V, Typ.)
- Subroutine nesting 96levels (Max.)
- Interrupt 8types, 5vectors
- 8-bit timer 4
- Programmable I/O ports
 - (Ports P0, P1, P2, P3, P4, P5, P6)..... 46
- Serial I/O (8-bit) 1
- PWM function 14-bit \times 1
 - 8-bit \times 4
 - 6-bit \times 6
- Comparator 1
- Generating function for clock input of EAROM
- Two clock generating circuits
 - (one is for main clock, the other is for clock function)
- 63-Character on screen display function
 - Number of character..... 21 characters \times 3 lines
 - Kinds of character..... 96

APPLICATION

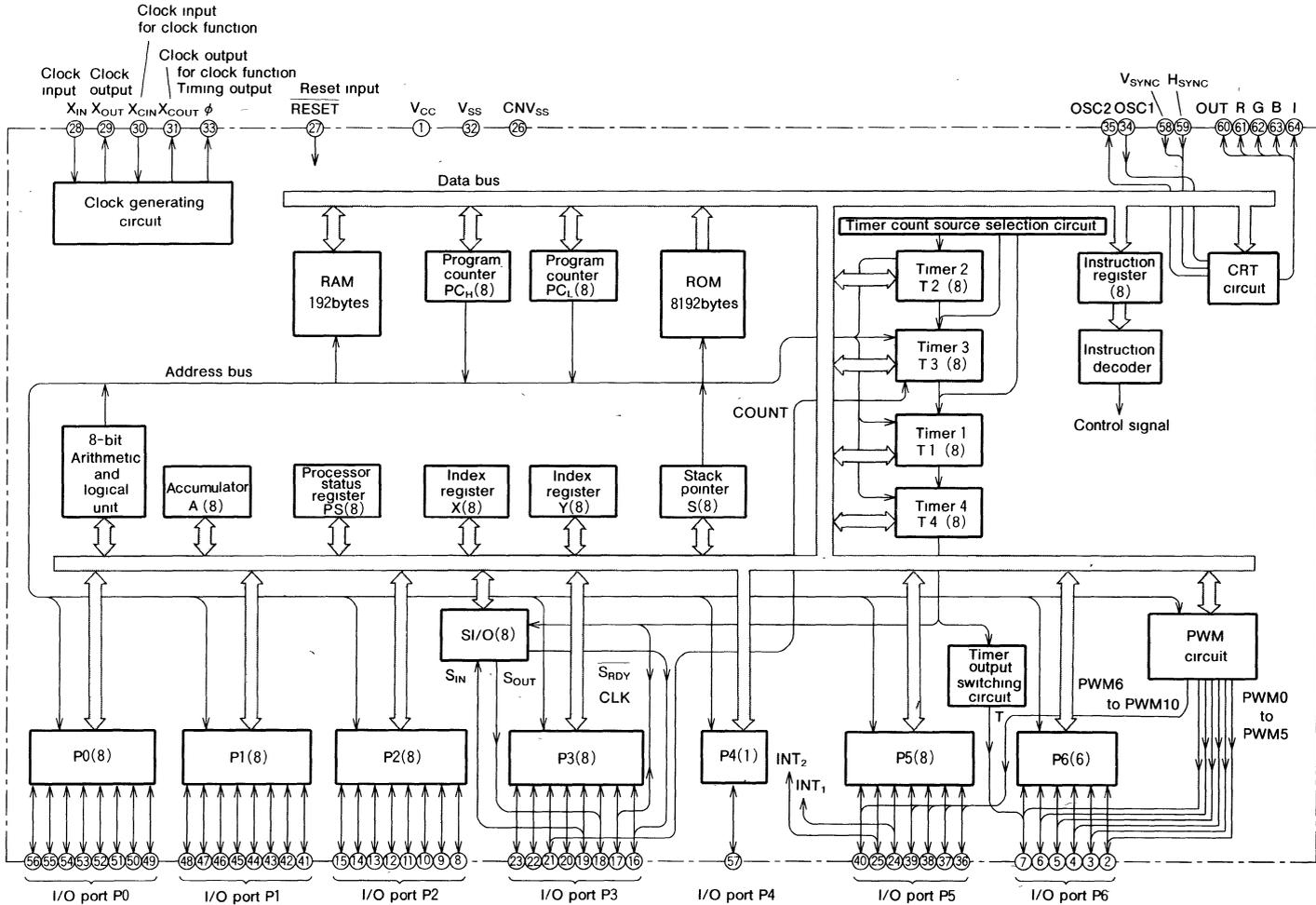
TV

PIN CONFIGURATION (TOP VIEW)





M37103M4-XXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

MITSUBISHI MICROCOMPUTERS
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**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

FUNCTIONS OF M37103M4-XXXSP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		2 μ s (minimum instructions, at 4MHz frequency)	
Clock frequency		4MHz	
Memory size	ROM	8192bytes	
	RAM	192bytes	
Input/Output ports	P0	I/O	8-bitX1 (middle-voltage N-channel open drain)
	P1, P2	I/O	8-bitX2
	P3	I/O	8-bitX1
	P4 ₇	I/O	1-bitX1
	I, B, R, G, OUT	Output	1-bitX5 (for CRT display)
	V _{SYNC} , H _{SYNC}	Input	1-bitX2 (for CRT display)
	P5 ₂ , P5 ₃	I/O	2-bitX1 (can be used as an input for either INT ₂ or INT ₁)
	P5 ₁ , P5 ₄ -P5 ₇	I/O	5-bitX1 (middle-voltage N-channel open drain)
	P6 ₀ , P6 ₁	I/O	2-bitX1
	P6 ₂ -P6 ₅	I/O	4-bitX1 (middle-voltage N-channel open drain)
Serial I/O		8-bitX1	
Timers		8-bit timerX4	
Subroutine nesting		96levels (max)	
Interrupt		Two external interrupts, three internal timer interrupts (or timerX2, serial I/OX1, CRTX1)	
Clock generating circuit		Two built-in circuits (externally connected ceramic or quartz crystal oscillator)	
Supply voltage		5V \pm 10%	
Power dissipation	at high-speed operation	CRT display function ON	35mW (clock frequency X _{IN} =4MHz, f _{CRT} =6MHz)
		CRT display function OFF	20mW (clock frequency X _{IN} =4MHz)
	at low-speed operation at stop mode	CRT display function OFF	0.3mW (clock frequency X _{CIN} =32kHz)
			I _{CC} =1 μ A (when clock is stopped)
Input/Output characteristics	Input/Output voltage	12V (P0, P5 ₁ , P5 ₄ -P5 ₇ , P6 ₂ -P6 ₅ : input/output, RESET, CNV _{SS} : input) -0.3 to V _{CC} +0.3V (P1, P2, P3, P4 ₇ , P5 ₂ , P5 ₃ , P6 ₀ , P6 ₁)	
	Output current	0.5mA (P0, P1, P2, P3, P5, P6 ₂ -P6 ₅ : N-channel open drain input/output) 0.5mA, -0.5mA (P4 ₇ : CMOS input/output, R, G, B, I, OUT, P6 ₀ -P6 ₁ : CMOS output)	
Operating temperature range		-10 to 70°C	
Device structure		CMOS silicon gate process	
Package		64-pin shrink plastic molded DIP	
CRT display function	Number of character	21 charactersX3 lines	
	Kinds of character	96 (12X16 dots)	

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is connect to V _{SS}
<u>RESET</u>	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins and external condensers are connected If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin In single-chip mode, the output can be controlled by selecting the option
X _{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{CIN} and X _{COOUT} pins and external condensers are connected If an external clock is used, the clock source should be connected to the X _{CIN} pin and the X _{COOUT} pin should be left open This clock can be used as a program controlled the system clock
X _{COOUT}	Clock output for clock function	Output	
P0 ₀ -P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is middle-voltage N-channel open drain
P1 ₀ -P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 It can be built in pull-up transistor at each pin by selecting the option
P2 ₀ -P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P1
P3 ₀ -P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as S _{RDY} , CLK, S _{OUT} , and S _{IN} pins, respectively P3 ₃ works as an analog input for comparator and P3 ₂ works as a counter input
P4 ₇	I/O port P4 ₇	I/O	Port P4 ₇ is a 1-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output
I, B, G, R, OUT	CRT output	Output	This is a 5-bit output pin for CRT display The output polarity can be changed by selecting the option At reset, inactive polarity is selected The output structure is CMOS output
H _{SYNC}	H _{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display The input polarity can be changed by selecting the option
V _{SYNC}	V _{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display The input polarity can be changed by selecting the option
P5 ₂ , P5 ₃	I/O port P5	I/O	These ports have basically the same function as ports P3, and are in common with interrupt input pins
P5 ₁ , P5 ₄ -P5 ₇			These ports have basically the same function as port P0, and can be programmed to function as PWM output pins
P6 ₀ -P6 ₅	I/O port P6	I/O	Port P6 is a 6-bit I/O port and has basically the same functions as port P0 The output structure of P6 ₀ , P6 ₁ is CMOS output and the output structure of P6 ₂ -P6 ₅ is middle-voltage N-channel open drain This port can be programmed to function as PWM output pins Also P6 ₀ is in common with timer output pin (T)
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display function To control generating frequency, external condensers and resistors are connected

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37103 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

- The FST and SLW instructions are not provided.
- The MUL and DIV instructions are not provided.
- The WIT instruction can be used.
- The STP instruction can be used.

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **RAM for display**

RAM for display is used for specifying the character codes and colors to display.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

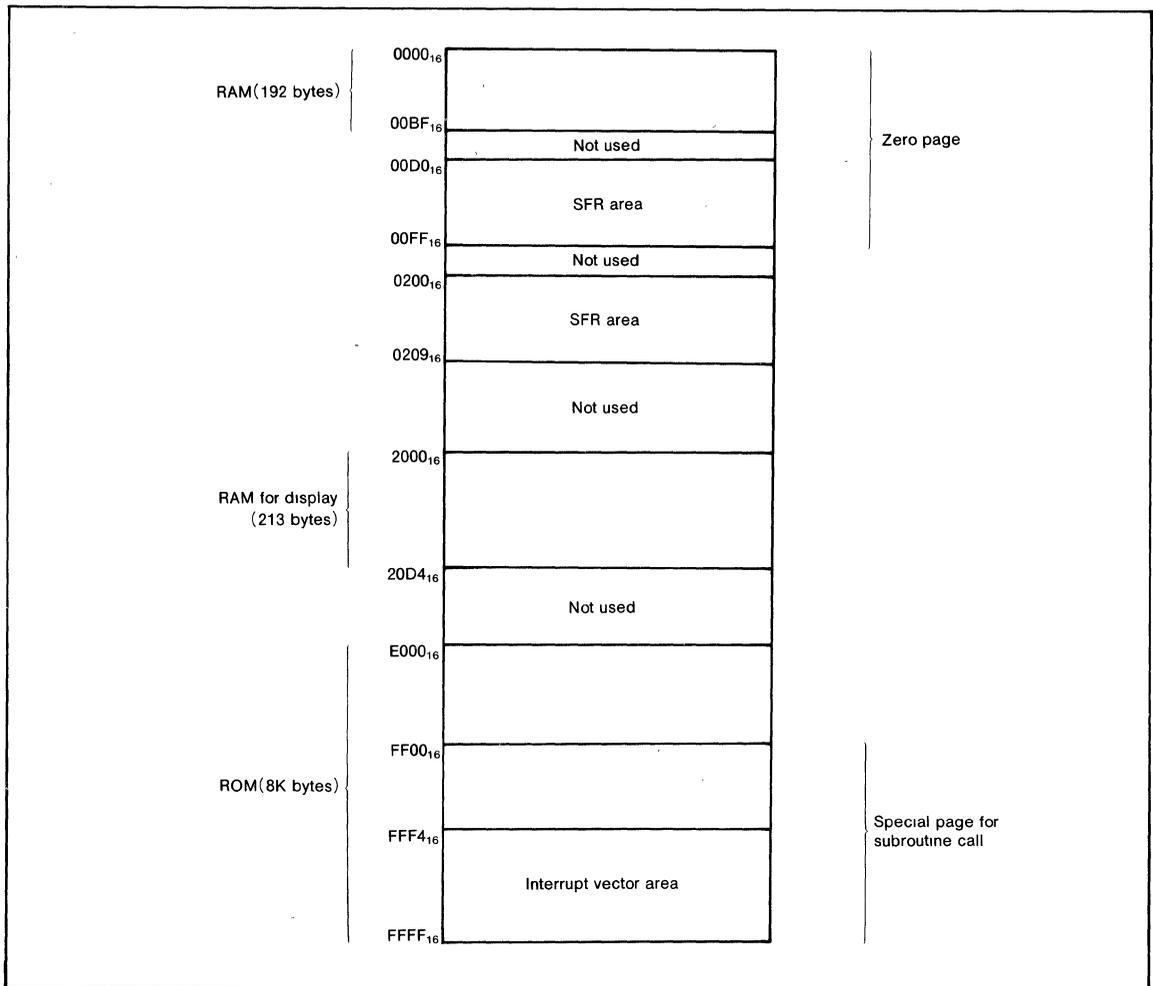


Fig. 1 Memory map

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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00D0 ₁₆	Horizontal position register	00EE ₁₆	Port P6
00D1 ₁₆	Vertical position register of block 1	00EF ₁₆	Port P6 directional register
00D2 ₁₆	Vertical position register of block 2	00F0 ₁₆	PWM1-H register
00D3 ₁₆	Vertical position register of block 3	00F1 ₁₆	PWM1-L register
00D4 ₁₆	Color register 0	00F2 ₁₆	PWM2 register
00D5 ₁₆	Color register 1	00F3 ₁₆	PWM3 register
00D6 ₁₆	Color register 2	00F4 ₁₆	PWM4 register
00D7 ₁₆	Color register 3	00F5 ₁₆	PWM control register
00D8 ₁₆	Display control register	00F6 ₁₆	Serial I/O mode register
00D9 ₁₆	Display block counter	00F7 ₁₆	Serial I/O register
00DA ₁₆		00F8 ₁₆	PWM5 register
00DB ₁₆		00F9 ₁₆	PWM output control register
00DC ₁₆		00FA ₁₆	Timer 1
00DD ₁₆		00FB ₁₆	Interrupt control register 2
00DE ₁₆		00FC ₁₆	Timer 2
00DF ₁₆		00FD ₁₆	Timer 3
00E0 ₁₆	Port P0	00FE ₁₆	Interrupt control register 1
00E1 ₁₆	Port P0 directional register	00FF ₁₆	Timer control register
00E2 ₁₆	Port P1	0100 ₁₆	⋮
00E3 ₁₆	Port P1 directional register	01FF ₁₆	⋮
00E4 ₁₆	Port P2	0200 ₁₆	PWM0 register
00E5 ₁₆	Port P2 directional register	0201 ₁₆	PWM6 register
00E6 ₁₆		0202 ₁₆	PWM7 register
00E7 ₁₆	A-D control register	0203 ₁₆	PWM8 register
00E8 ₁₆	Port P3	0204 ₁₆	PWM9 register
00E9 ₁₆	Port P3 directional register	0205 ₁₆	PWM10 register
00EA ₁₆	Port P4	0206 ₁₆	PWM output control register
00EB ₁₆	Port P4 directional register	0207 ₁₆	
00EC ₁₆	Port P5	0208 ₁₆	Timer 4 control register
00ED ₁₆	Port P5 directional register	0209 ₁₆	Timer 4

Fig. 2 SFR (Special Function Register) memory map

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INTERRUPTS

Interrupts can be caused by 8 different events consisting of two external, five internal, and one software event.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

Falling edge active or rising edge active can be selected for each of the INT₁ and INT₂ external interrupts selected by bits 4 and 5 of the PWM control register. Whether the INT₁ external interrupt or the CRT display is to be accepted can be selected by bit 0 of interrupt control register 2.

Whether the timer 1 or serial I/O interrupt is to be accepted can be selected by bit 2 of the serial I/O mode register.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits and the interrupt enable bits are in interrupt control register 1 and timer control register. Figure 3 shows the structure of the interrupt control registers 1 and 2 and timer control register.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be clear with a program, but not set. The interrupt enable bit can be set and clear with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 4 shows interrupts control

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
INT ₁ or CRT display interrupt	2	FFFD ₁₆ , FFFC ₁₆	INT ₁ external interrupt (phase programmable)
Timer 3 interrupt	3	FFFB ₁₆ , FFFA ₁₆	
Timer 2 interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	
Timer 1 or serial I/O interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	
INT ₂ interrupt (BRK instruction interrupt)	6	FFF5 ₁₆ , FFF4 ₁₆	INT ₂ external interrupt (phase programmable) BRK instruction interrupt (non-maskable software interrupt)

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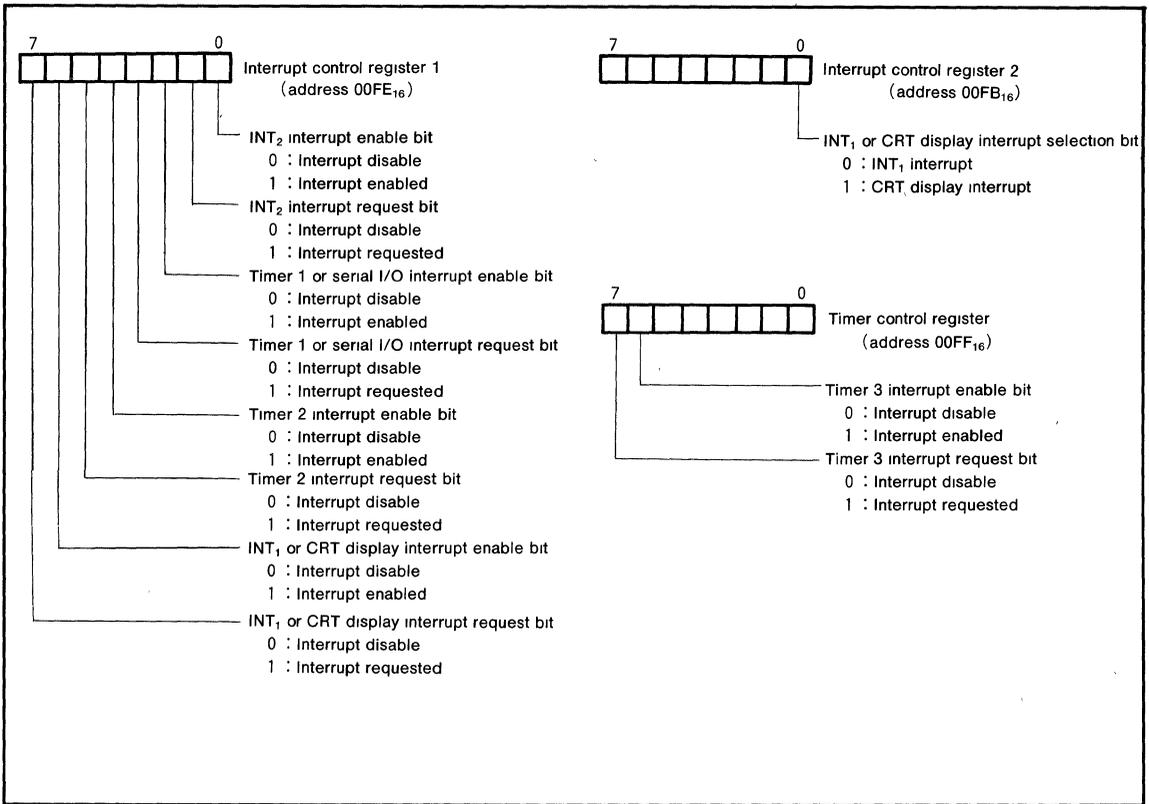


Fig. 3 Structure of registers related to interrupt

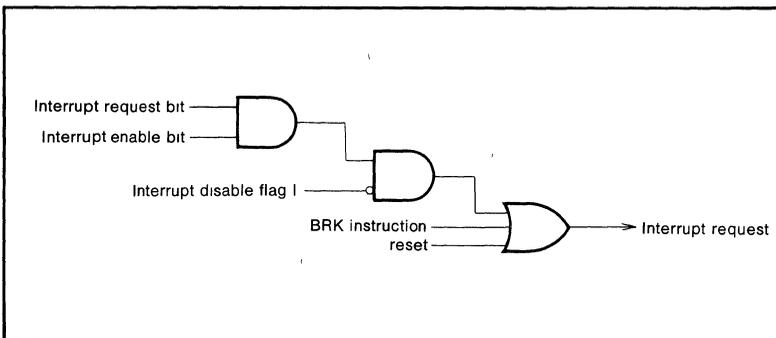


Fig. 4 Interrupt control

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TIMER

The M37103M4-XXXSP has four timers; timer 1, timer 2 timer 3, timer 4.

A block diagram of timer 1 through 3 is shown in Figure 5 and a block diagram of timer 4 is shown in Figure 6. The count source for timer 1 through 3 can be selected by using bit 2, 3, 4 of the timer control register (address $00FF_{16}$), as shown in Figure 7. Timer 1 through 3 are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the re-load latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch.

Timer 1 through 3 has interrupt generating functions. The timer interrupt request bit which is in the interrupt control register 1 or timer control register (located at addresses $00FE_{16}$ and $00FF_{16}$ respectively) is set at the next count pulse after the timer reaches "0" (see interrupt section).

The starting and stopping of timer 2 is controlled by bit 5 of the timer control register 2. If the bit 5 is "0", the timer starts counting, and the bit 5 is "1", the timer stops.

The count source of timer 4 can be selected by bit 0 and bit 1 of timer 4 control register (address 0208_{16}). When bit 0 and bit 1 are set to [00] or [11], timer 4 stop counting. The structure of timer 4 control register is shown in Figure 8.

Timer 4 has auto-reload register. The auto-reload register can be written by writing a data to timer 4 register. A data written to the auto-reload register is set to counter by setting bit 4 of timer 4 control register. And by reading a data from timer 4 register, the value of counter can be read.

When timer 4 is overflow, timer 4 overflow flag is set and the content of auto-reload register are loaded into the counter.

At a reset or stop mode, FF_{16} is automatically set in timer 2 and 07_{16} in timer 3.

After a STP instruction is executed, timer 3, timer 2, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register).

This state is canceled if timer 3 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 2 count stop bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

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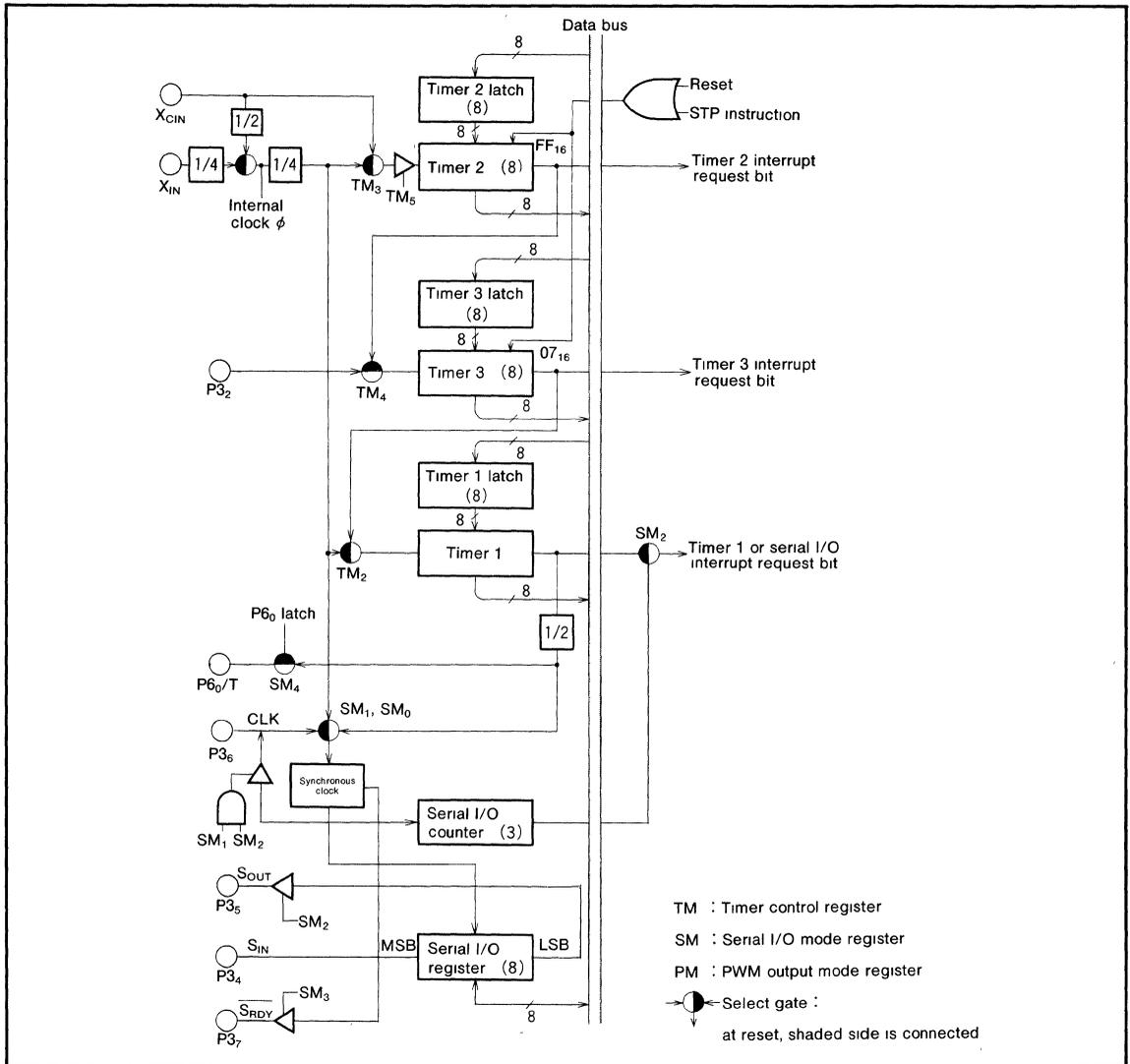


Fig. 5 Block diagram of timer 1 through 3

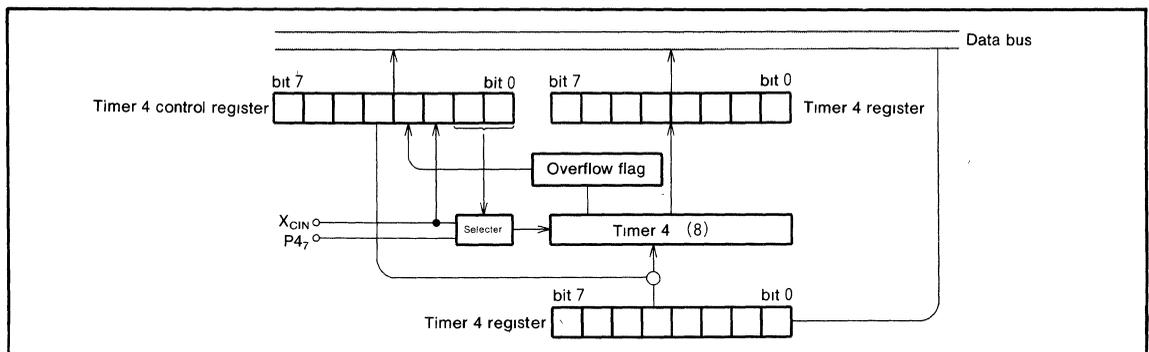


Fig. 6 Block diagram of timer 4

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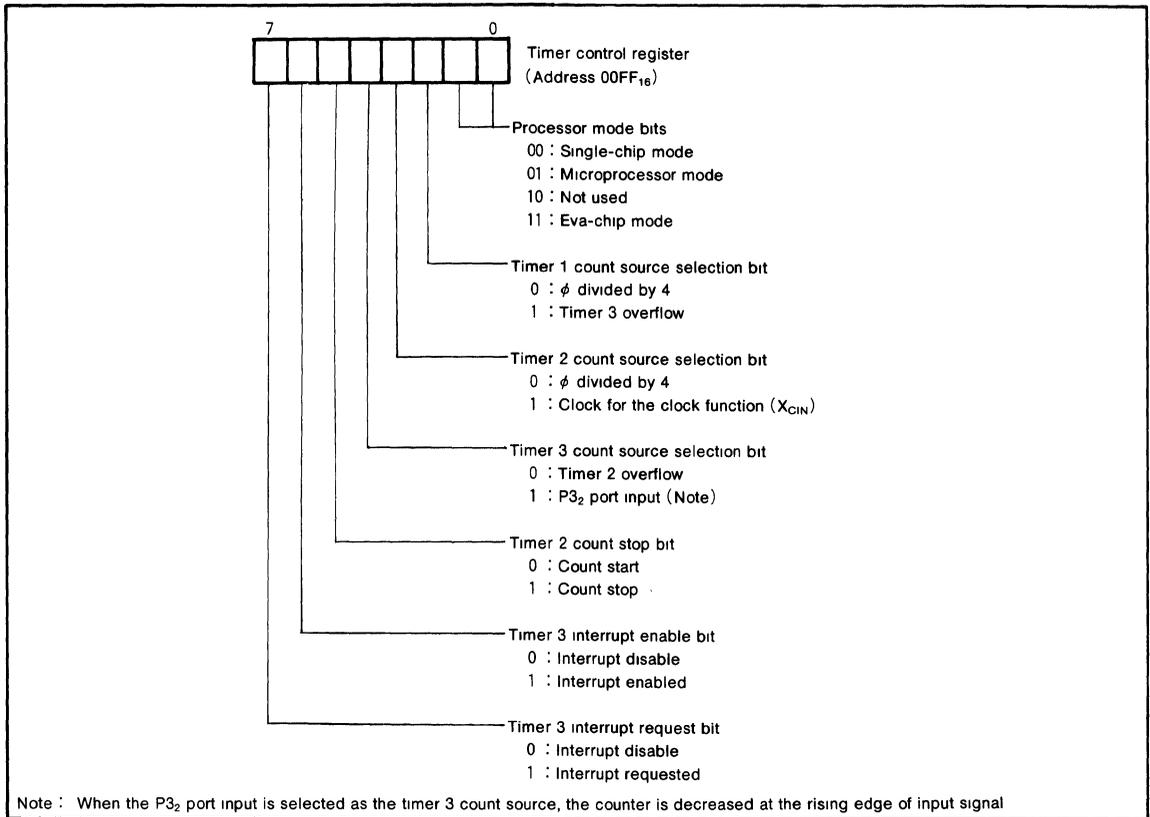


Fig. 7 Structure of timer control register

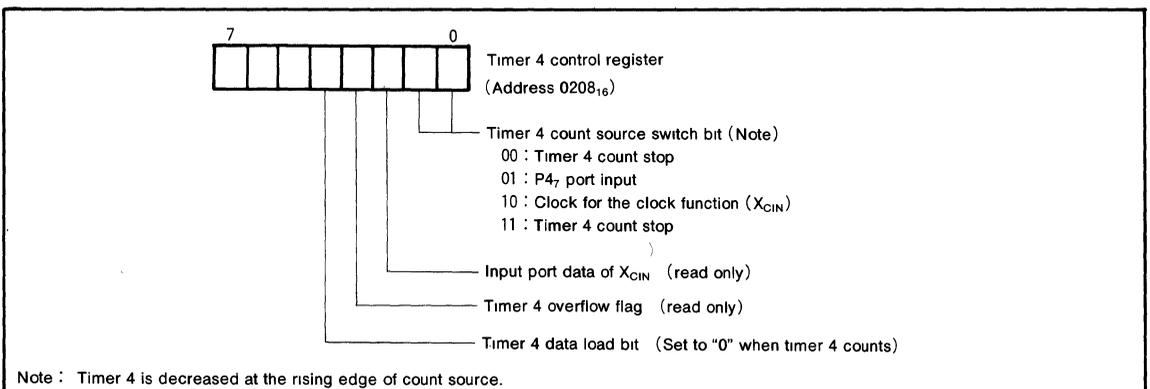


Fig. 8 Structure of timer 4 control register

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SERIAL I/O

The block diagram of serial I/O is shown in Figure 9. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT} , S_{IN}), pins are used as P37, P36, P35, and P34, respectively. The serial I/O mode register (address 00F6₁₆) is an 8-bit register. Bit 0 and 1 of this register is used to select a syn-

chronous clock source. When these bits are [00] or [01], an external clock from P36 is selected. When these bits are [10], the overflow signal divided by two from timer 1 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

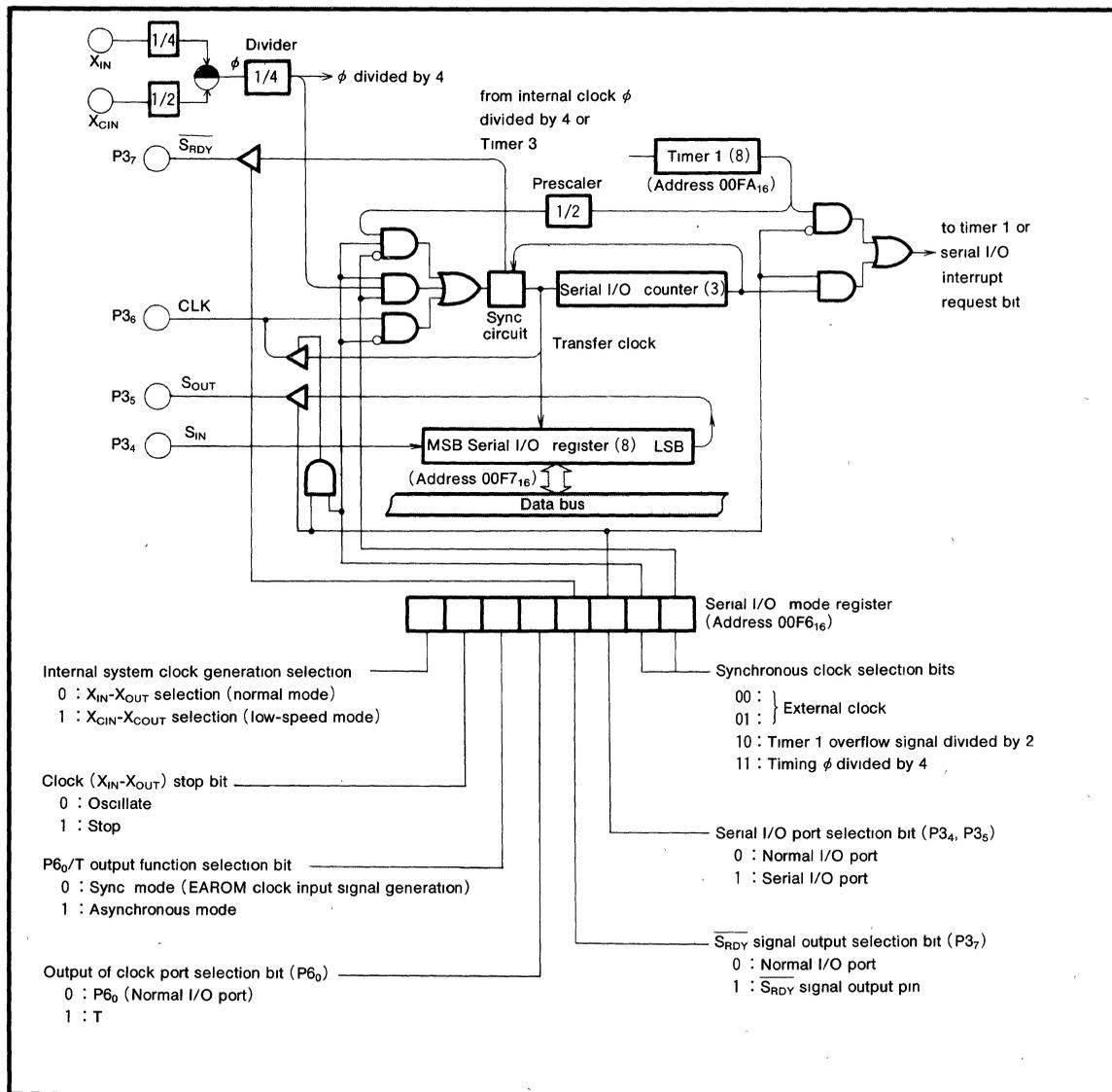


Fig. 9 Block diagram of serial I/O

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Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", P3₆ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P3₆. If the external synchronous clock is selected, the clock is input to P3₆. And P3₅ will be a serial output, and P3₄ will be a serial input. To use P3₄ as a serial input, set the directional register bit which corresponds to P3₄, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" P3₆ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 1. Bit 3 determines if P3₇ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 3="0").

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock- The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal

becomes low signaling that the M37103M4-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to P3₅. During the rising edge of this clock, data can be input from P3₄ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock- If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 10, and connection between two M37103M4-XXXSP's are shown in Figure 11.

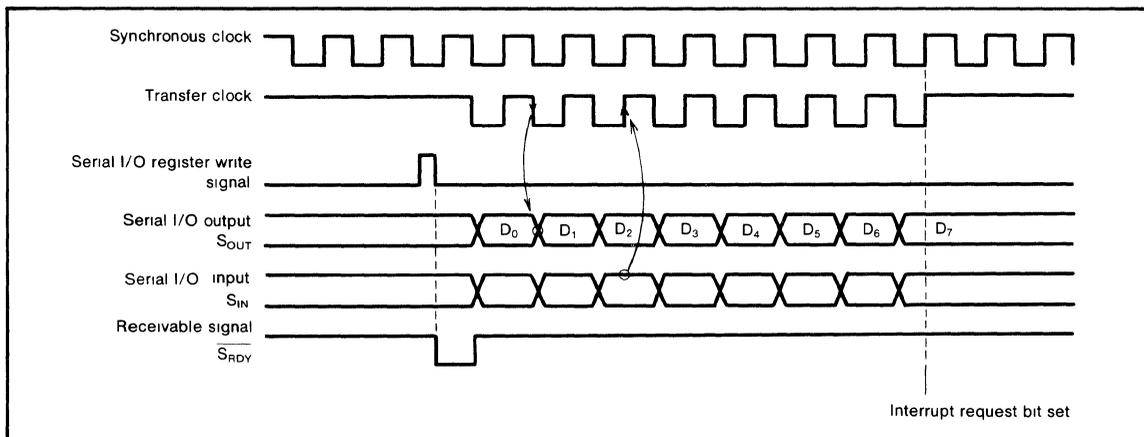


Fig. 10 Serial I/O timing

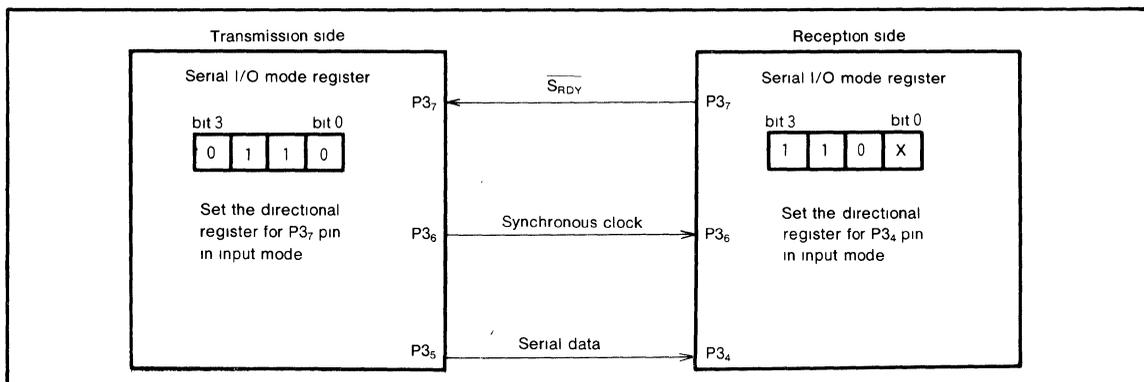


Fig. 11 Example fo serial I/O connection

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

PWM OUTPUT CIRCUIT

(1) Introduction

The M37103M4-XXXSP is equipped with one 14-bit PWM, four 8-bit PWMs and six 6-bit PWMs. The 14-bit resolution gives PWM1 the minimum resolution bit width of 500ns (for $X_{IN} = 4\text{MHz}$) and a repeat period of 8192 μs . PWM7, PWM8, PWM9, PWM10 have a 8-bit resolution with minimum resolution bit width of 16 μs and repeat period of 4096 μs . PWM0, PWM2, PWM3, PWM4, PWM5, PWM6 have a 6-bit resolution with minimum resolution bit width of 16 μs and repeat period of 1024 μs . Accuracy and operation range is certified of PWM are $V_{CC} = 4.5$ to 5.5V regardless of input frequency.

Block diagram of the PWM is shown in Figures 12 and 13.

The PWM timing generator section applies individual control signals to PWM 0-10, using clock input X_{IN} divided by 2 or X_{CIN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM0-PWM5 are in common with pins P6₀-P6₅ of port P6 and PWM6-PWM10 are in common with pins P5₁-P5₇ of port P5 (i.e. for PWM output, PWM output selection bits and the P5, P6 directional register D5₁-D5₇, D6₀-D6₅ should be set). When PWM1 is used for output, first set the higher 8-bit of the PWM1-H register (address 00F0₁₆), then the lower 6-bit of the PWM1-L register (address 00F1₁₆). When either PWM0 and PWM2-10 is used for output, set the 8-bit in the PWM0 and PWM2-10 register, respectively. Note that the higher 2 bits of these 8-bit registers are ignored when used 6-bit register.

(3) Transferring data from registers to latches

The data written to the 6-bit or 8-bit PWM register is transferred to the PWM latch in each 6-bit PWM cycle period. For 14-bit PWM, the data is transferred in the next upper 8-bit period after the write. The signals output to the PWM pins correspond to the contents of these latches. When data at addresses 00F0₁₆ to 00F4₁₆, 00F8₁₆, 0200₁₆ to 0205₁₆ is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. When the 6-bit latch is being read, the upper 2 bits of the register becomes undefined. However, bit 7 of the PWM1-L register indicated the completion of the data transfer from the PWM1 register to the PWM1 latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 6-bit PWMs

The timing diagram of the two 6-bit PWMs (PWM0 and PWM2-6) is shown in Figure 14. One period (T) is composed of 64 (2⁶) segments.

There are six different pulse types configured from bits 0 to 5 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 14 (a).

Six different pulses can be output from the PWM. These can be selected by bits 0 through 5. Depending on the content of the 6-bit PWM latch, pulses from 5 to 0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 14 (b). Changes in the contents of the PWM latch allows the selection of 64 lengths of high-level area outputs varying from 0/64 to 63/64. An length of entirely high-level output cannot be output. i.e. 64/64.

(5) 8-bit PWM operation

8-bit PWM operation is the same as 6-bit PWM operation except that one period (T) is composed of 256 (2⁸) segments.

(6) 14-bit PWM operation

The timing diagram of the 14-bit PWM1 is shown in Figure 15. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length N times τ is output every short area of $t = 256 \tau = 128 \mu\text{s}$ as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 15.)

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ . As a result, the short-area period t (= 128 μs , approx. 7.8kHz) becomes an approximately repetitive period.

(7) Output after reset

At reset the output of port P5, P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data	Area longer by τ than that of other t_m ($m = 0$ to 63)
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m = 32$
0 0 0 0 1 0	$m = 16, 48$
0 0 0 1 0 0	$m = 8, 24, 40, 56$
0 0 1 0 0 0	$m = 4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m = 1, 3, 5, 7, \dots, 57, 59, 61, 63$

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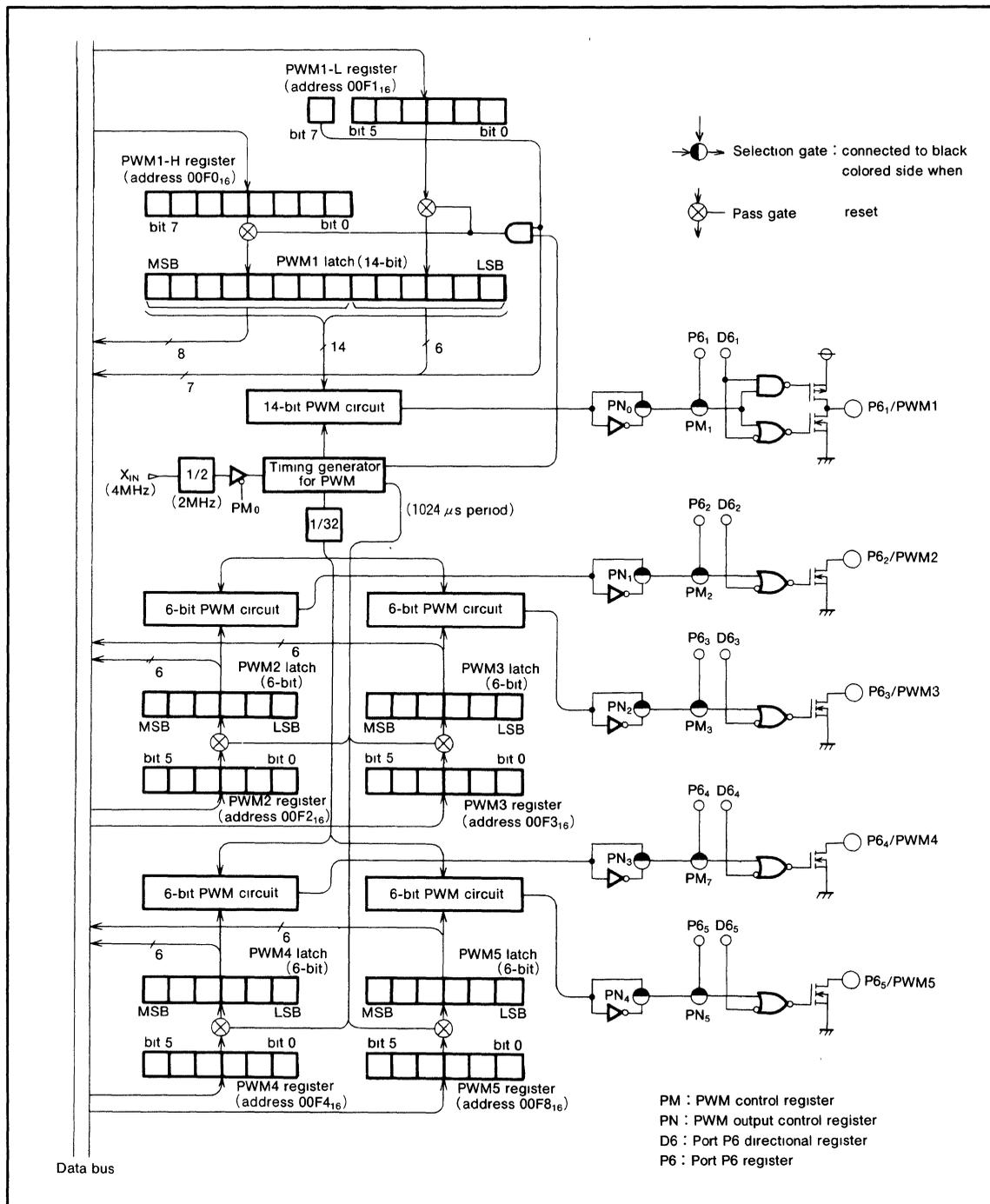


Fig. 12 Block diagram of the PWM circuit (1)

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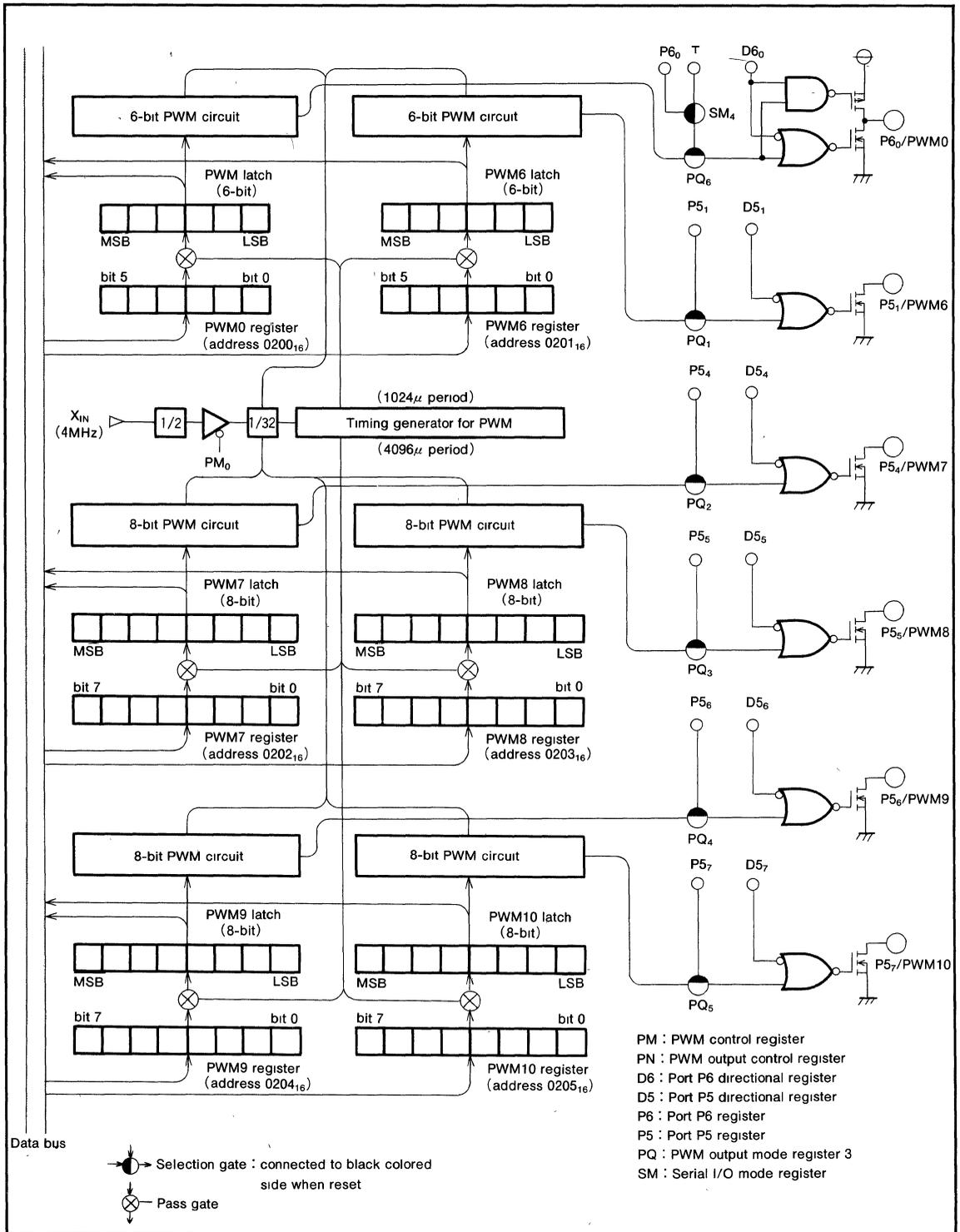


Fig. 13 Block diagram of the PWM circuit (2)

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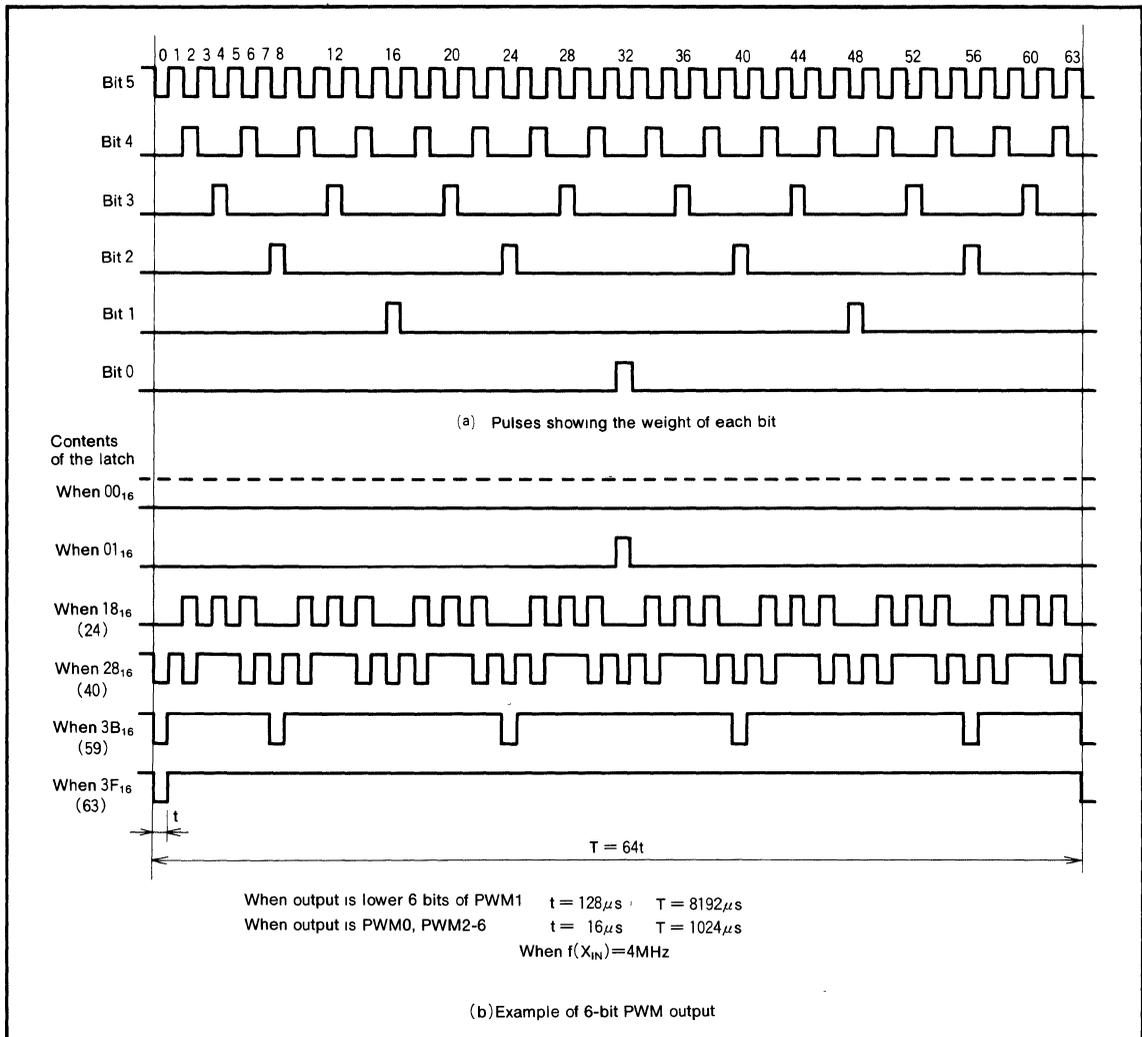


Fig. 14 6-bit PWM timing diagram

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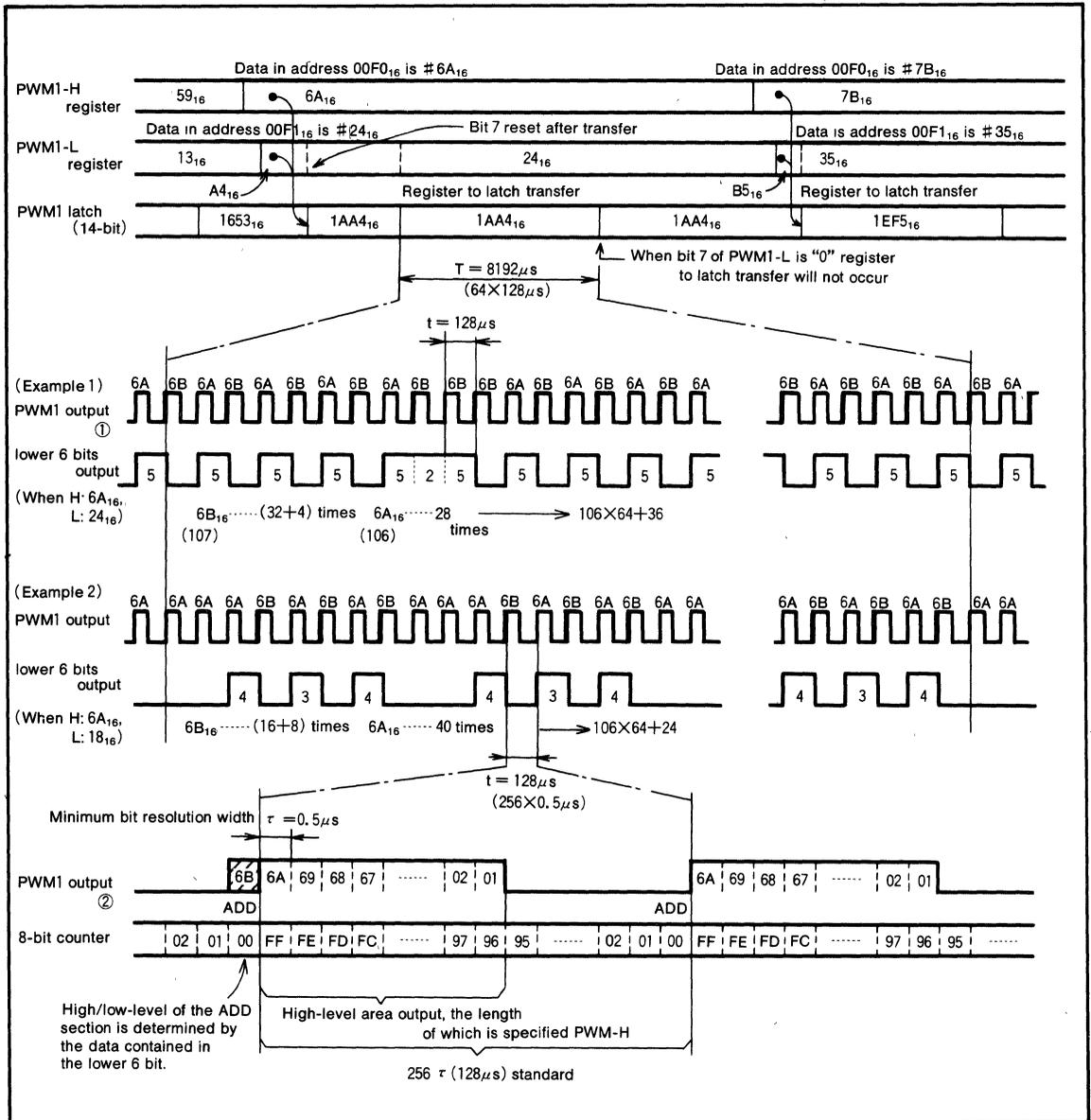


Fig. 15 14-bit PWM timing diagram

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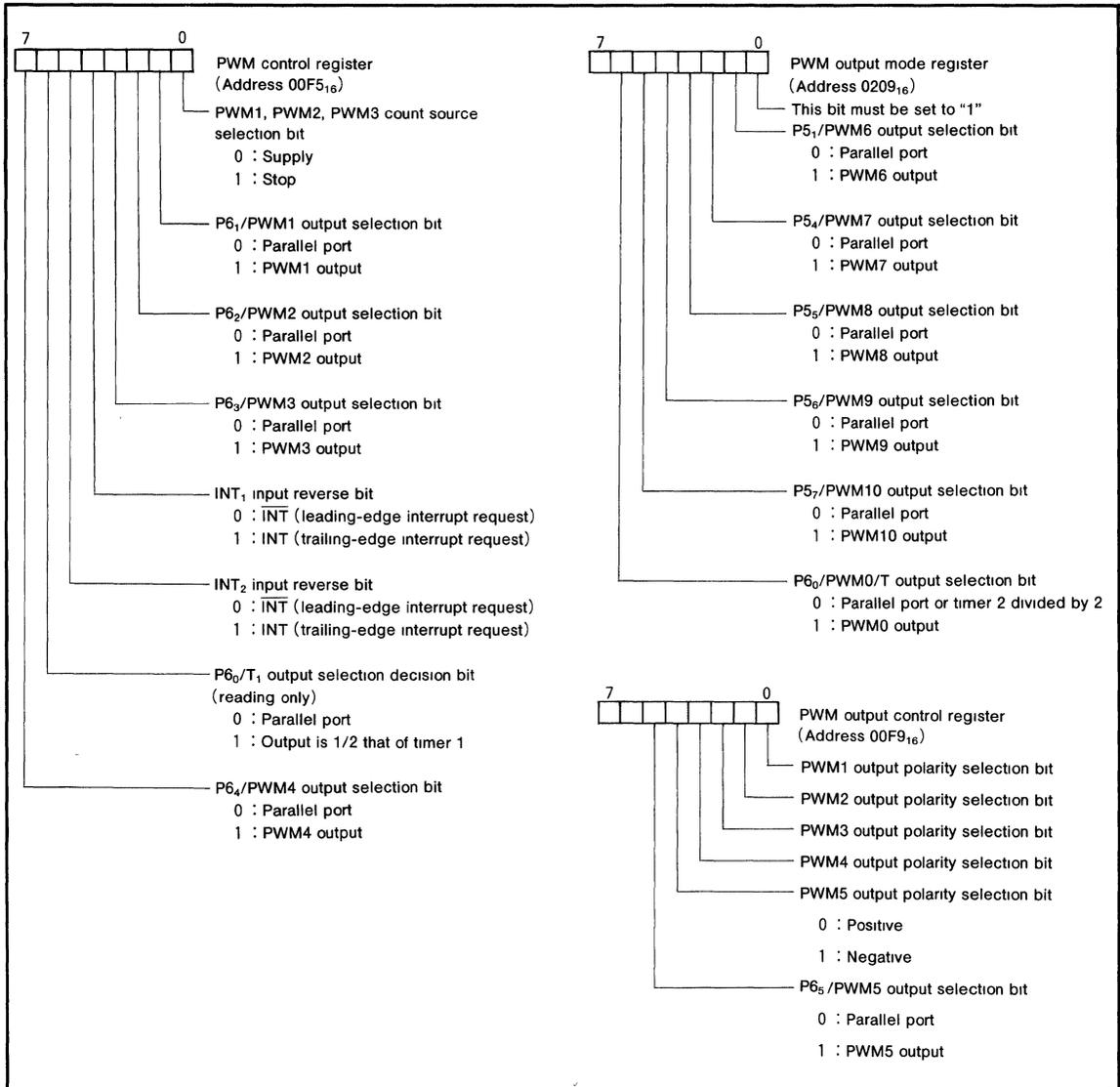


Fig. 16 Structure of registers related to PWM

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PORT P6₀ / TIMER 1 OUTPUT

Bit 0 of port P6 outputs 1/2 the frequency of timer 1 when bit 6 of the PWM output mode register is set to "0" and bit 4 (SM₄) of the serial I/O mode register (address 00F6₁₆) is set to "1". The output switching can be accomplished with either of two procedures, synchronous mode or asynchronous mode, depending on the setting of bit 5 (SM₅) of the serial I/O mode register.

When SM₅ is set to "0" the synchronous mode is set. In such a case, after SM₄ has been changed, synchronization is set to the 1/2 frequency of timer 1 and switching between the port latch and timer takes place. It is possible to ascertain whether switching actually occurred by reading

the value of bit 6 of the PWM control register.

From the time that the contents of SM₄ was changed to the point where switching completes, the contents of neither SM₄ nor P6₀ may be changed. Use of the synchronous mode prevents the generation of a pulse shorter than the timer output during switching. Figure 17 (a) gives an example of timing in the synchronous mode. Use of the synchronous mode allows generation of an EAROM clock input signal through the use of a simple program.

When SM₅ is set to "1", the asynchronous mode is set. In this case, the output switching occurs directly after SM₄ has been changed. Figure 17 (b) gives an example of timing in the asynchronous mode.

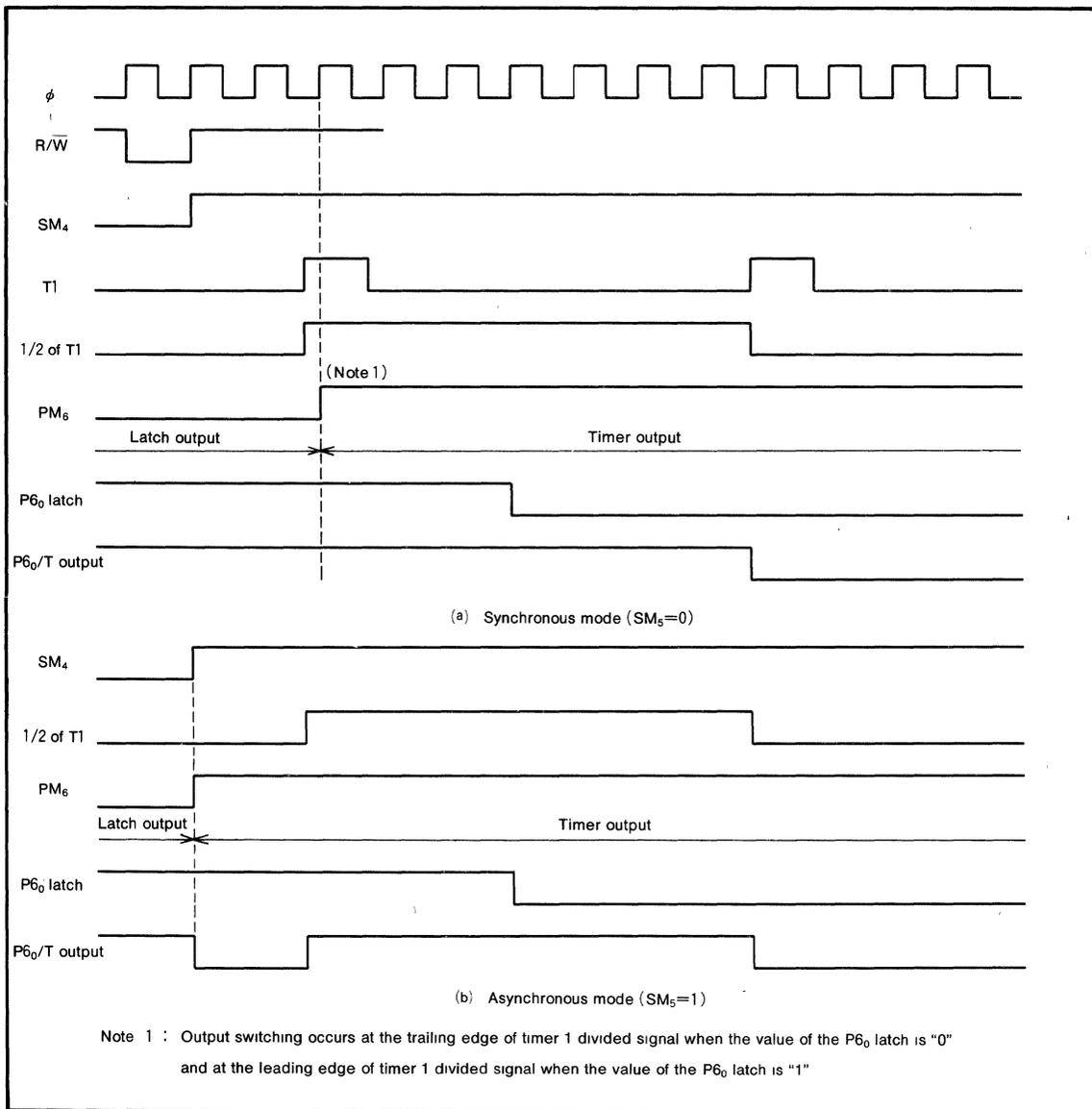


Fig. 17 P6₀/T switching timing diagram

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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COMPARATOR CIRCUIT

The comparator circuit is shown in Figure 18. The comparator circuit consists of the switch tree, ladder resistor, comparator, comparator control circuit, A-D control register (address 00E7₁₆), and analog signal input pin (P3₃/A-D). The analog input pin is common with the digital input/output terminal to the data bus.

The 5-bit A-D control register can generate 1/16V_{CC}-step internal analog voltage, based on the settings of bits 0 to 3. Table 3 gives the relation between the descriptions of A-D control register bits 0 to 3 and the generated internal analog voltage. The comparator result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 4.

The data is compared by setting the directional register corresponding to port P3₃ to "0" (port P3₃ enters the input mode), to allow port P3₃/A-D to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register (address 00E7₁₆), bits 0 to 3. The voltage comparison starts as soon as the writing is completed. 4-cycle (required for comparing) later, the result of comparison is stored in the A-D control register, bit 4. Bit 4 is "1" when analog input voltage > internal analog voltage and "0" when analog input voltage < internal analog voltage.

When voltage is compared to by setting bits 0 to 3 of the comparator register "0", bit 4 of the A-D control register becomes "1" regardless of the analog input voltage.

Table 3. Relationship between the contents of A-D control register and internal voltage

A-D control register				Internal analog voltage
bit 3	bit 2	bit 1	bit 0	
0	0	0	1	1/16V _{CC} -1/32V _{CC}
0	0	1	0	2/16V _{CC} -1/32V _{CC}
0	0	1	1	3/16V _{CC} -1/32V _{CC}
0	1	0	0	4/16V _{CC} -1/32V _{CC}
0	1	0	1	5/16V _{CC} -1/32V _{CC}
0	1	1	0	6/16V _{CC} -1/32V _{CC}
0	1	1	1	7/16V _{CC} -1/32V _{CC}
1	0	0	0	8/16V _{CC} -1/32V _{CC}
1	0	0	1	9/16V _{CC} -1/32V _{CC}
1	0	1	0	10/16V _{CC} -1/32V _{CC}
1	0	1	1	11/16V _{CC} -1/32V _{CC}
1	1	0	0	12/16V _{CC} -1/32V _{CC}
1	1	0	1	13/16V _{CC} -1/32V _{CC}
1	1	1	0	14/16V _{CC} -1/32V _{CC}
1	1	1	1	15/16V _{CC} -1/32V _{CC}

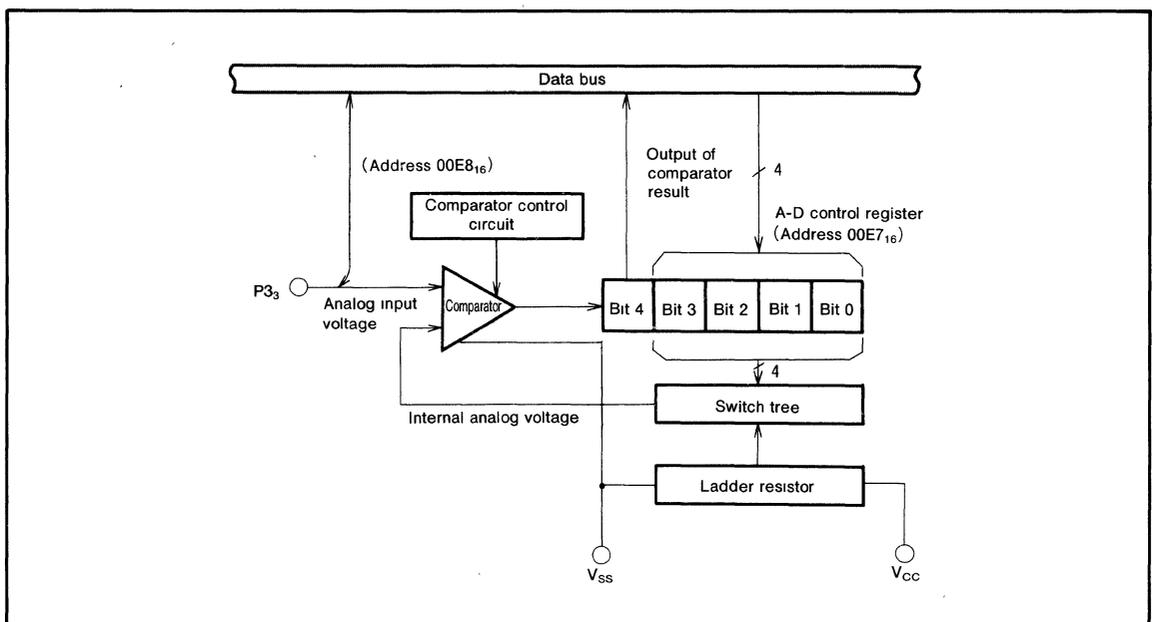


Fig. 18 Comparator Circuit

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CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display functions

Table 4 outlines the CRT display functions. The M37103M4-XXXSP incorporates a 21 columns X 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register. Up to 96 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12X16 dot configuration to obtain smooth character patterns. (See Figure 19)

The following shows the procedure how to display characters on the CRT screen.

- ① Set the character to be displayed in display RAM.
- ② Set the display color by using the color register.
- ③ Specify the color register in which the display color is set by using the display RAM.
- ④ Specify the vertical position and character size by using the vertical position register.
- ⑤ Specify the horizontal position by using the horizontal position register.
- ⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

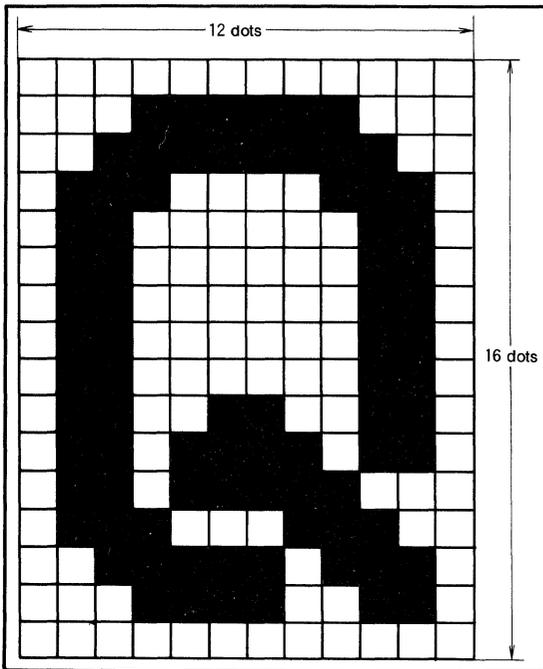


Fig. 19 CRT display character configuration

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 3 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 21 shows a block diagram of the CRT display control circuit. Figure 20 shows the structure of the CRT display control register.

Table 4. Outline of CRT display functions

Parameter	Functions	
Number of display character	21 characters X 3 lines	
Character configuration	12X16 dots (See Figure 19)	
Kinds of character	96	
Character size	4 size selectable	
Color	Kinds of color	15(max)
	Coloring unit	a character
Display expansion	Possible (multiple lines)	

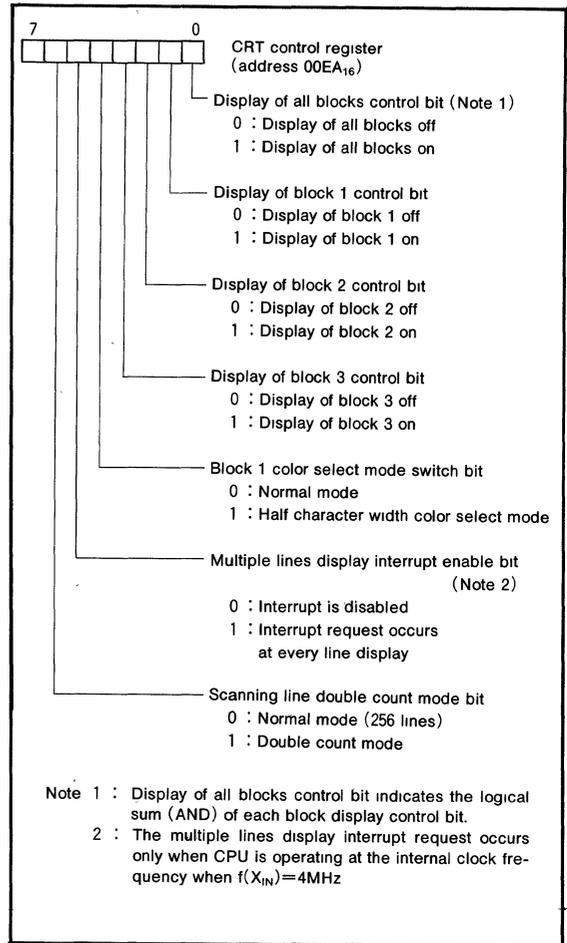


Fig. 20 Structure of CRT control register

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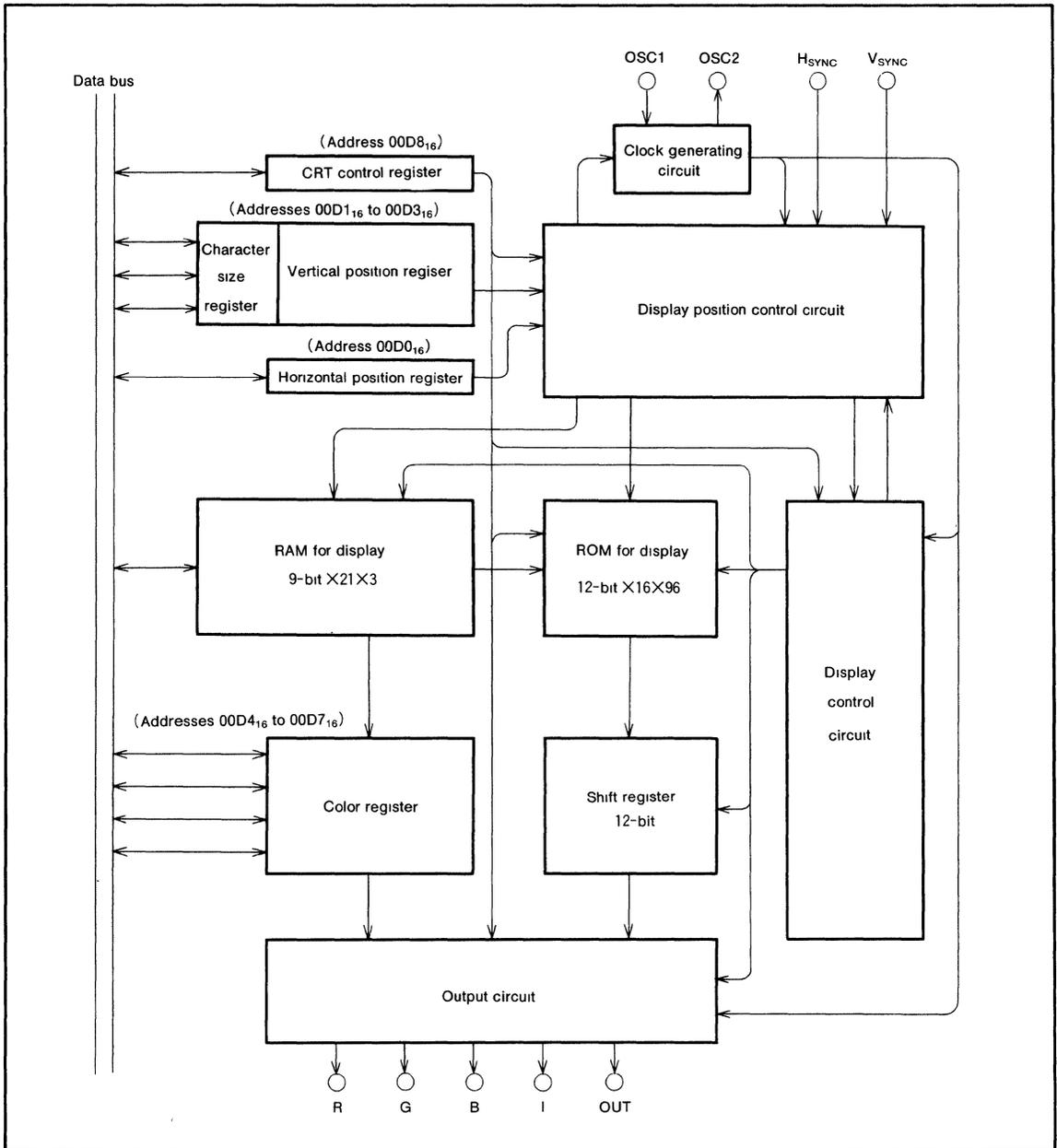


Fig. 21 Block diagram of CRT display control circuit

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(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 21 characters can be displayed in one block. (See (4) Display Memory.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of 4Tc (Tc=oscillation cycle for display).

The display position in the vertical direction is selected from 64-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 24), a block of the smaller block No. (1 to 3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 24), the former block is overridden and the latter is displayed.

The vertical position can be specified from 64-step positions (four scanning lines per step) for each block by setting values 00₁₆ to 3F₁₆ to bits 0 to 5 in the vertical position register (addresses 00D1₁₆ to 00D3₁₆). Figure 22 shows the structure of the vertical position register.

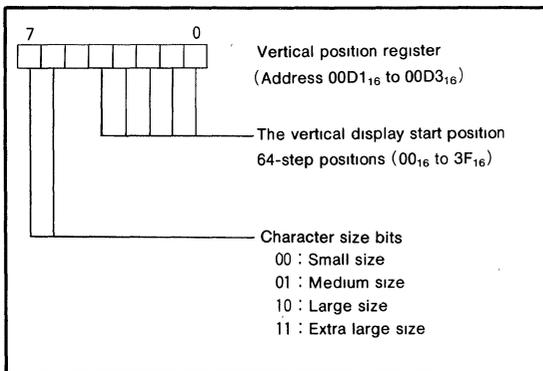


Fig. 22 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64-step display positions (4Tc per step (Tc=oscillation cycle for display) by setting values 00₁₆ to 3F₁₆ to bits 0 to 5 in the horizontal position register (address 00D0₁₆).

Figure 23 shows the structure of the horizontal position register.

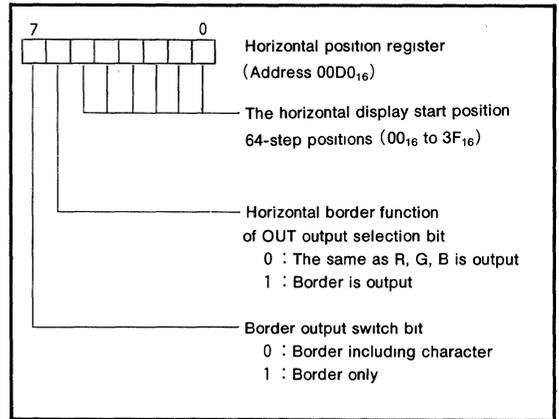
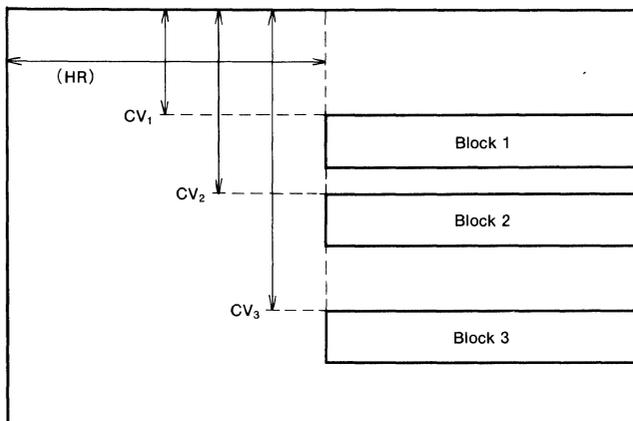
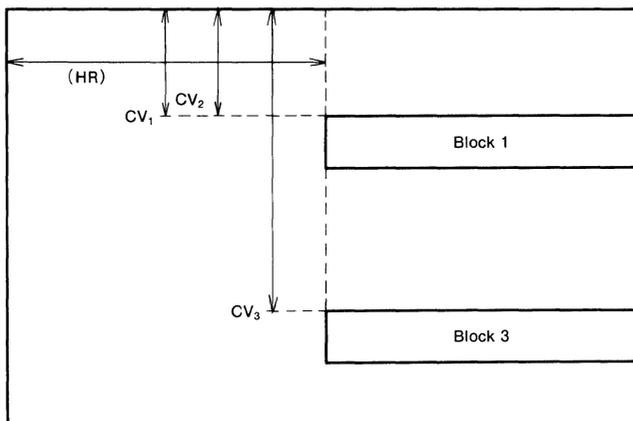


Fig. 23 Structure of horizontal position register

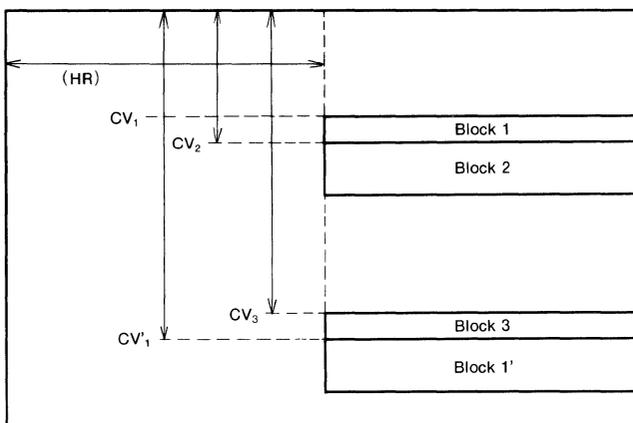
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(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed

Fig. 24 Display position

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(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the bit 6 and 7 of vertical position register to set a character size.

The character size can be selected from four sizes: small size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display

oscillation ($=T_c$) in the width (horizontal) direction.

The small size consists of [one scanning line] \times [1 T_c]; the medium size consists of [two scanning lines] \times [2 T_c]; the large size consists of [three scanning lines] \times [3 T_c]; and the extra large size consists of [four scanning lines] \times [4 T_c]. Table 5 shows the relationship between the set values in the character size register and the character sizes.

Table 5. The relationship between the set values of the character size bits and the character sizes.

Set values of the character size bits		Character size	Width (horizontal) direction	Height (vertical) direction
Bit7	Bit6			
0	0	Small	1 T_c	1
0	1	Medium	2 T_c	2
1	0	Large	3 T_c	3
1	1	Extra large	4 T_c	4

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal start position is common to all blocks even when the character size varies with each block (See Figure 25)

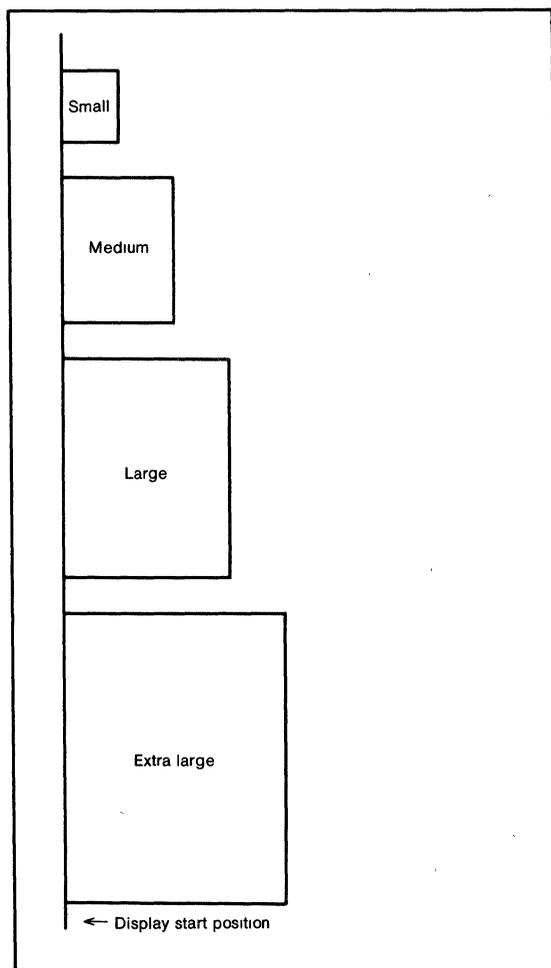


Fig. 25 Display start position of each character size (horizontal direction)

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(4) RAM for display

RAM for display is allocated at addresses 2000_{16} to $20D4_{16}$, and is divided into a display character code specifying part and display color specifying part for each block. Table 6 shows the contents of the CRT display RAM.

When a character is to be display at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0 to 6) in address 2000_{16} and the color register No. to the two low-order bits (bits 0 and 1) in address 2080_{16} . The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 26.

Table 6. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1 st Column	2000_{16}	2080_{16}
	2 nd Column	2001_{16}	2081_{16}
	3 rd Column	2002_{16}	2082_{16}
	⋮	⋮	⋮
	19th Column	2012_{16}	2092_{16}
	20th Column	2013_{16}	2093_{16}
	21th Column	2014_{16}	2094_{16}
	Not used	2015_{16} to $201F_{16}$	2095_{16} to $209F_{16}$
Block 2	1 st Column	2020_{16}	$20A0_{16}$
	2 nd Column	2021_{16}	$20A1_{16}$
	3 rd Column	2022_{16}	$20A2_{16}$
	⋮	⋮	⋮
	19th Column	2032_{16}	$20B2_{16}$
	20th Column	2033_{16}	$20B3_{16}$
	21th Column	2034_{16}	$20B4_{16}$
	Not used	2035_{16} to $203F_{16}$	$20B5_{16}$ to $20BF_{16}$
Block 3	1 st Column	2040_{16}	$20C0_{16}$
	2 nd Column	2041_{16}	$20C1_{16}$
	3 rd Column	2042_{16}	$20C2_{16}$
	⋮	⋮	⋮
	19th Column	2052_{16}	$20D2_{16}$
	20th Column	2053_{16}	$20D3_{16}$
	21th Column	2054_{16}	$20D4_{16}$
	Not used	2055_{16} to $207F_{16}$	

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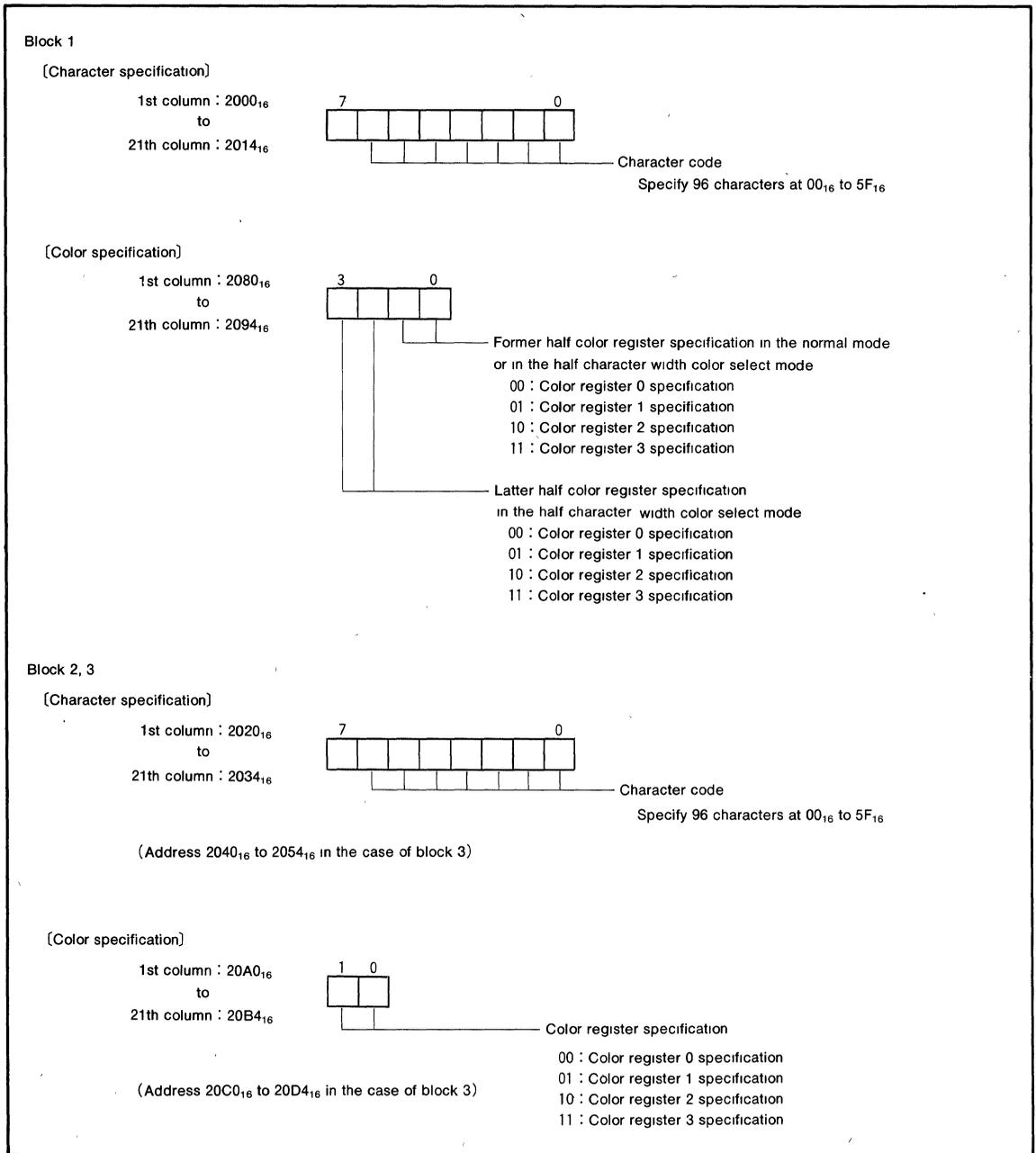


Fig. 26 Structure of the CRT display RAM

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(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0-CO3: addresses 00D4₁₆ to 00D7₁₆) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set 2^4-1 (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 27 shows the structure of the color register.

(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address 00D8₁₆) it is possible to specify colors in units of a half character size (vertical 16 dots X horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

- ① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080₁₆ to 2094₁₆).
- ② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080₁₆ to 2094₁₆).

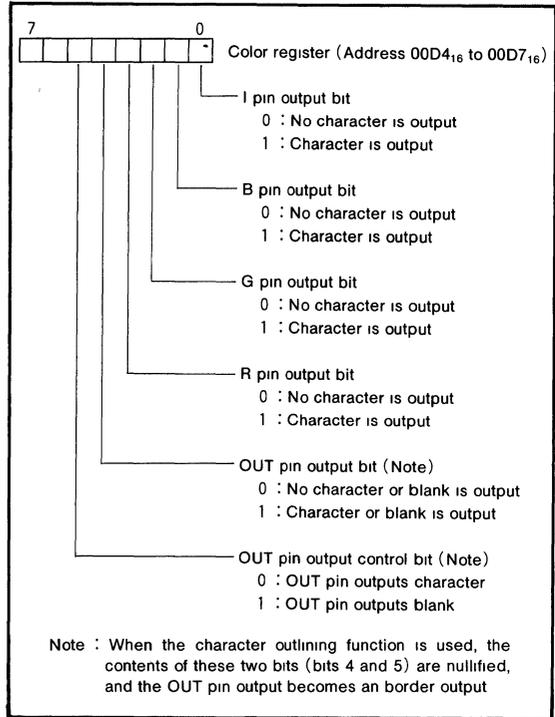


Fig. 27 Structure of color registers

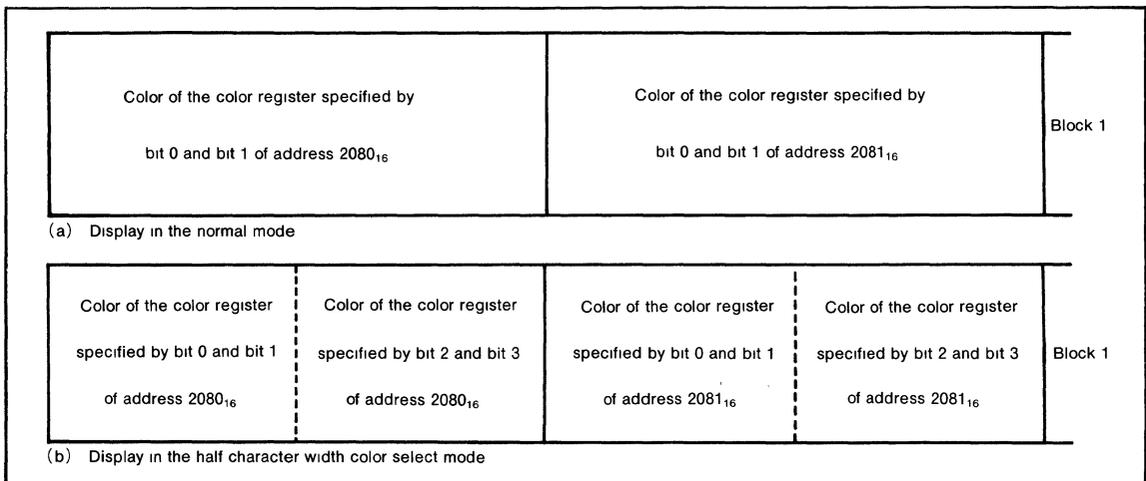


Fig. 28 Difference between normal color select mode and half character width color select mode

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(7) Multiline Display

The M37103M4-XXXSP can normally display three lines on the CRT screen by displaying three blocks at different vertical positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit=bit 6 at address 00FE₁₆) to "1"), then execute the following processing in the CRT interrupt handling routine.

- ① Read the value of the display block counter.
 - ② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.
 - ③ Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and vertical display position (contents of vertical position register) to be displayed next.
- Figure 29 shows the structure of the display block counter.

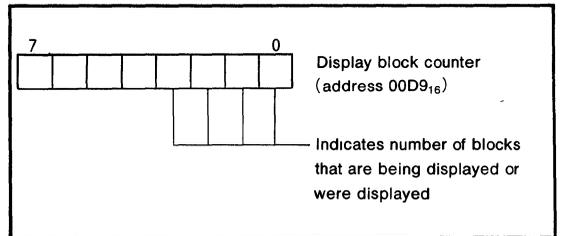


Fig. 29 Structure of display block counter

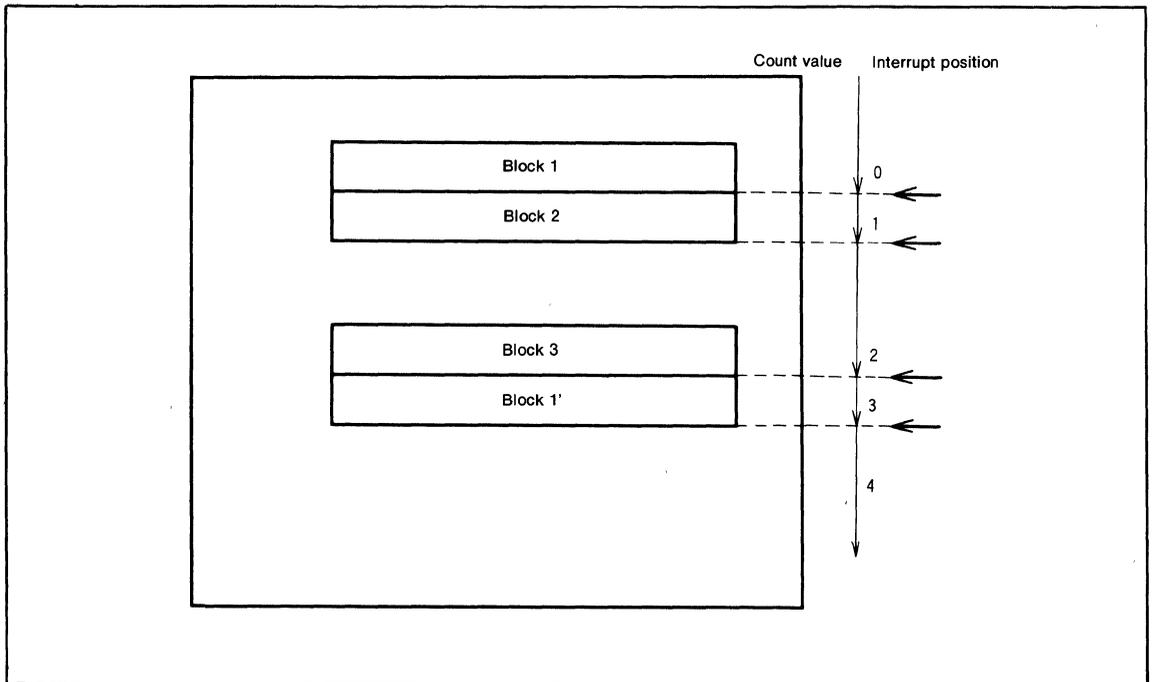


Fig. 30 Timing of CRT interrupt and count value of display block counter

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(8) Scanning Line Double Count Mode

One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended twofold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 64 steps from 00_{16} to $3F_{16}$, or four scanning lines per step, the number of steps in the scanning line double count mode is 32 from 00_{16} to $1F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 20_{16} to $3F_{16}$ in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register (address $00D8_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.

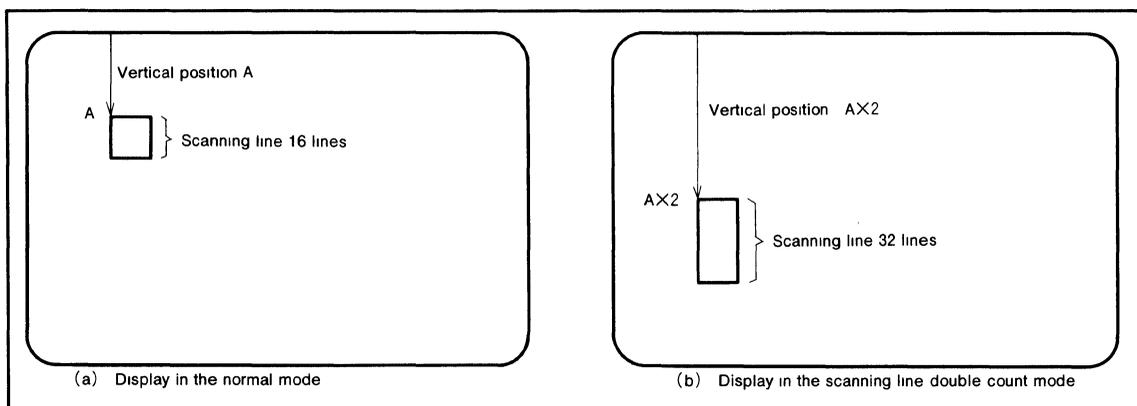


Fig. 31 Display in the normal mode and in the scanning line double count mode

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(9) Horizontal Character Border Function

An border of a one clock (one dot) equivalent size can be added to a character to be displayed only horizontal direction.

The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (contents output from the OUT pin) are nullified, and the border is output from the OUT pin instead.

Border can be specified in units of block by using the bits 6 and 7 of horizontal position register. Table 7 shows the relationship between the values set in the horizontal position register and the character border function.

Table 7. The relationship between the value set in the horizontal position register and the character border function

Horizontal position register		Functions	Example of output	
Bit 7	Bit 6			
X	0	Normal	R, G, B, I output OUT output	
0	1	Border including character	R, G, B, I output OUT output	
1	1	Border not including character	R, G, B, I output OUT output	

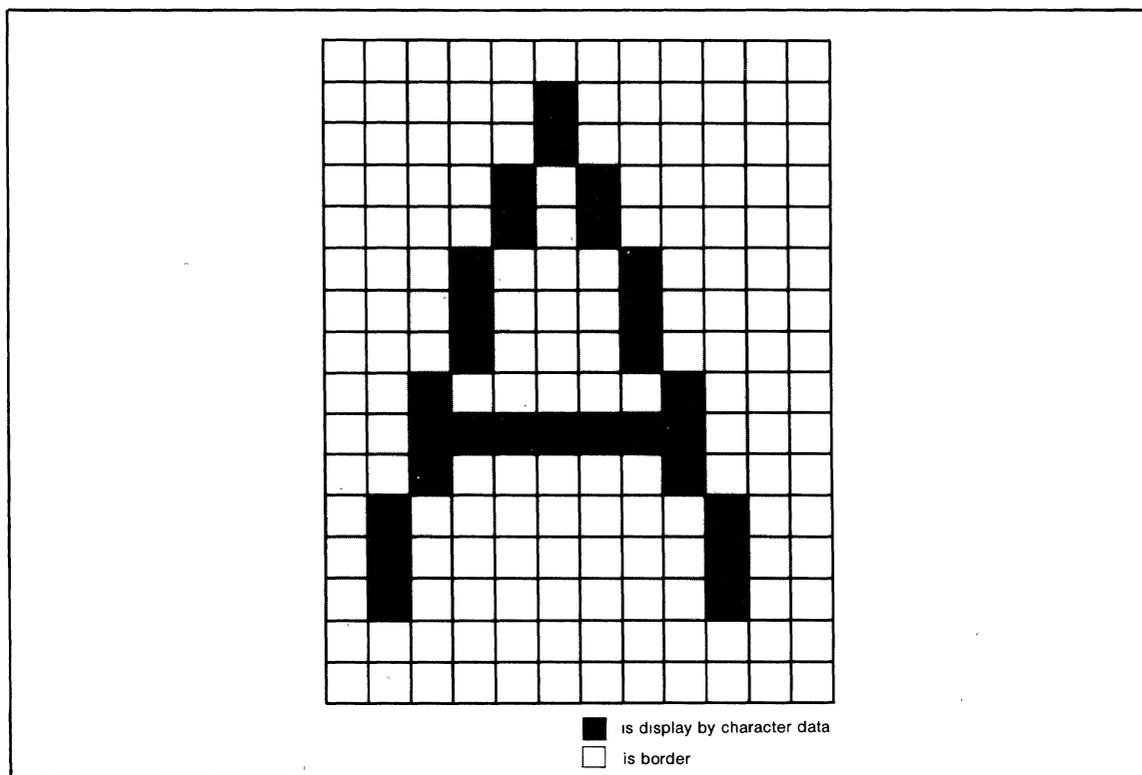


Fig. 32 Example of border

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(10) Programming notes

1. Use STA instruction for data transfer to the following registers related to OSD functions.
 - ① Horizontal position register (address $00D0_{16}$)
 - ② Vertical position registers (address $00D1_{16}$ to $00D3_{16}$)
 - ③ Color registers (address $00D4_{16}$ to $00D7_{16}$)
 - ④ CRT control register (address $00D8_{16}$)
2. Do not display the display OFF blocks having different character sizes on a block display.
3. The highest vertical position (the vertical display start position bits are " 00_{16} ") can not be used.
4. The interrupt to tell the end of block display is not caused and the display block counter is not incremented until the display of the block has been completed terminated.
5. The display block counter ($00D9_{16}$) is reset while V_{SYNC} is "H" (when the option is positive in polarity) to " 00_{16} ".
6. If, during the display of a block, the display position of another block comes, the display of the subsequent block (having a larger vertical position register value) is preferred.
7. When two or more blocks are displayed in the same vertical position, the display priority is CV1, CV2, and CV3 in this order. This is not affected by turning on/off of block display.

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RESET CIRCUIT

The M37103 is reset according to the sequence shown in Figure 34. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the RESET pin is held at "L" level for no less than $2\mu s$ while the power voltage is $5V \pm 10\%$ and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 33.

	Address	
(1) Port P0 directional register (D0)(E1 ₁₆)		00 ₁₆
(2) Port P1 directional register (D1)(E3 ₁₆)		00 ₁₆
(3) Port P2 directional register (D2)(E5 ₁₆)		00 ₁₆
(4) Port P3 directional register (D3)(E9 ₁₆)		00 ₁₆
(5) Port P4 directional register (D4)(EB ₁₆)		0
(6) Port P5 directional register (D5)(ED ₁₆)		00000000
(7) Port P6 directional register (D6)(EF ₁₆)		00000000
(8) PWM control register (PM)(F5 ₁₆)		00 ₁₆
(9) Serial I/O mode register (SM)(F6 ₁₆)		00 ₁₆
(10) PWM output control register (PN)(F9 ₁₆)		00000000
(11) Interrupt control register 2 (IN)(FB ₁₆)		0
(12) Timer 2 (T2)(FC ₁₆)		FF ₁₆
(13) Timer 3 (T3)(FD ₁₆)		07 ₁₆
(14) Interrupt control register 1 (IM)(FE ₁₆)		00 ₁₆
(15) Timer control register (TM)(FF ₁₆)		00 ₁₆
(16) Processor status register (PS)		1
(17) Program counter (PCH)		Contents of address FFFF ₁₆
	(PCL)	Contents of address FFFE ₁₆
(18) Horizontal location register (HR)(DO ₁₆)		00 ₁₆
(19) Color register 0 (C0)(D4 ₁₆)		00000000
(20) Color register 1 (C1)(D5 ₁₆)		00000000
(21) Color register 2 (C2)(D6 ₁₆)		00000000
(22) Color register 3 (C3)(D7 ₁₆)		00000000
(23) Display control register (CC)(D8 ₁₆)		00000000
(24) PWM output control register (PQ)(0206 ₁₆)		00000000
(25) Timer 4 control register (TN)(0208 ₁₆)		0000

Note Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values

Fig. 33 Internal state of microcomputer at reset

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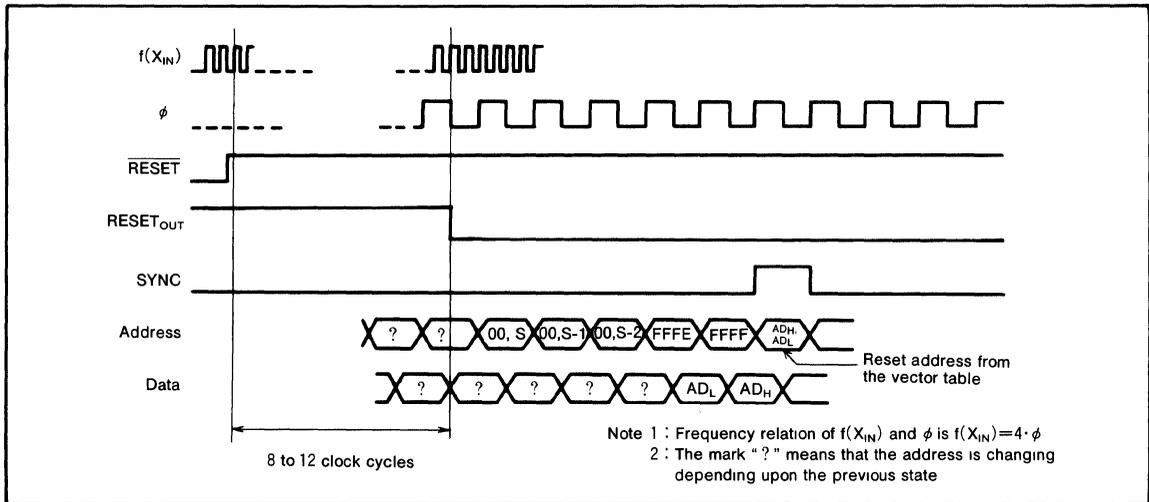


Fig. 34 Timing diagram at reset

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain and middle-voltage output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address 00E0₁₆.

Port P0 has a directional register (address 00E1₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address 00FF₁₆), three different modes can be selected; single-chip mode, eva-chip mode and microprocessor mode

In these modes it functions as address (A₇-A₀) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. It can be built in pull-up register at each pin by selecting the option. In other modes, it functions as address (A₁₅-A₈) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P1. In other modes, it functions as data (D₀-D₇) input/output port. Refer to the section on processor modes for details.

(4) Port P3

In single-chip mode, port P3 has the same function as port P0 but the output structure is not middle voltage. P3₂-P3₇ have program selectable dual functions. P3₀, P3₁ function as control signals input/output port except in the single-chip mode. Refer to the section on processor modes for details.

(5) Port P4

This is a 1-bit I/O port with function similar to port P0, but the output structure is CMOS output.

This port is unaffected by the processor mode bits.

(6) Port P5

This is an 8-bit I/O port with function similar to port P0, but the output structure of P5₂ and P5₃ is not middle-voltage. P5₁ and P5₄-P5₇ have program selectable dual functions. P5₂, P5₃ are shared with external interrupt input pins (INT₁, INT₂).

This port is unaffected by the processor mode bits.

(7) Port P6

This is an 6-bit input/output port with function similar to port P0. The output structure of P6₀, P6₁ is CMOS output and the output structure of P6₂-P6₅ is N-channel open drain and middle-voltage.

P6₀-P6₅ have program selectable dual functions.

This port is unaffected by the processor mode bits.

(8) Function pins for CRT display function.

The horizontal synchronizing signal is input from H_{SYNC}.

The vertical synchronizing signal is input from V_{SYNC}. I, B, G, R, OUT are output pins for CRT display.

Refer to the section on CRT display functions for details.

(9) ϕ pin.

The internal system clock (1/4 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) can be output from this pin by selecting the option.

At low-speed mode, X_{CIN} divided by 2 is output from this pin.

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

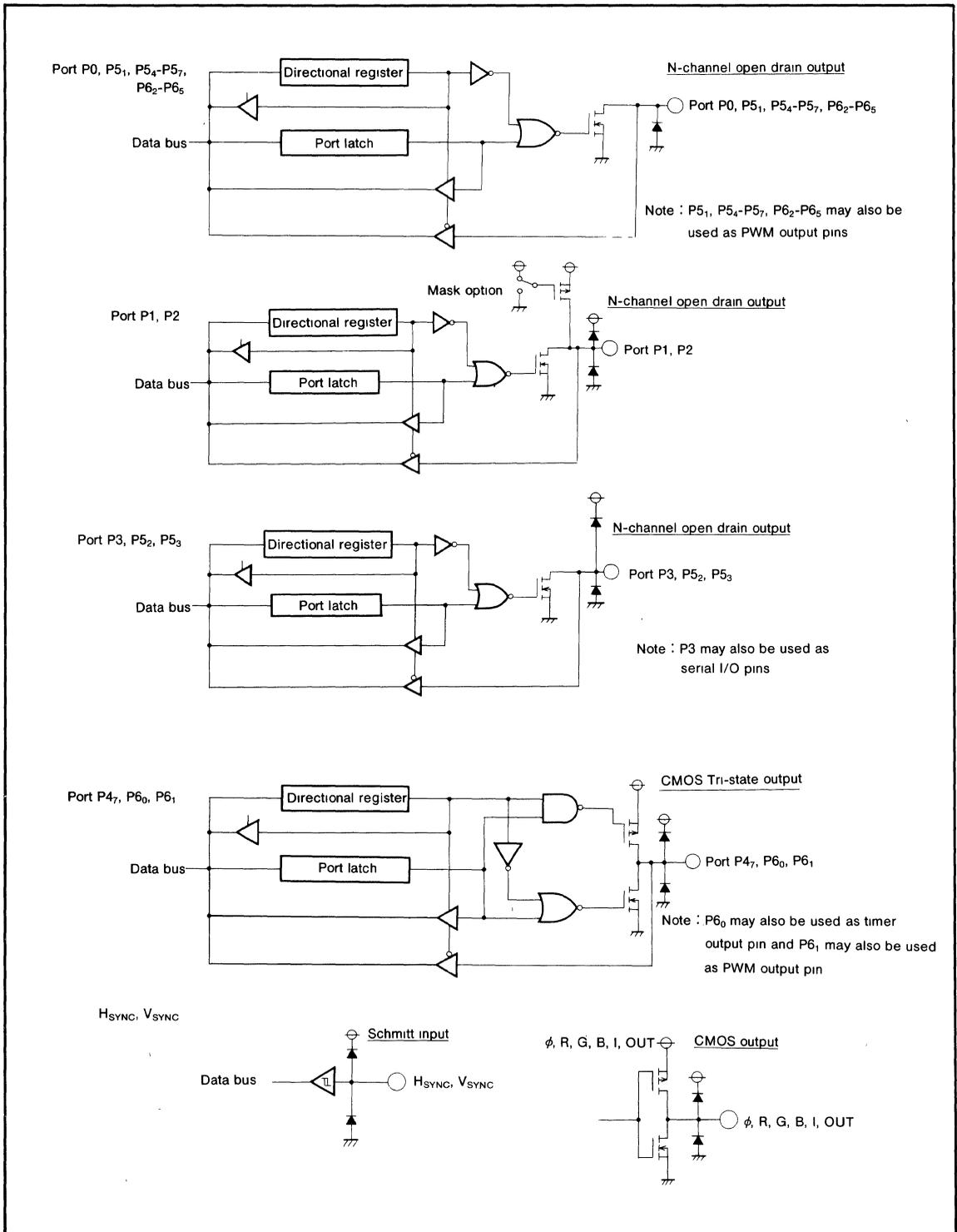


Fig. 35 Ports P0-P6, H_{sync}, V_{sync}, φ, R, G, B, I and OUT block diagram

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address 00FF₁₆), three different operation modes can be selected; single-chip mode, microprocessor mode and evaluation chip (eva-chip) mode. In the microprocessor mode and eva-chip mode, ports P0-P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports. Figure 37 shows the functions of ports P0-P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 36.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The three different modes are explained as follows:

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Port P0-P3 will work as original I/O ports.

(2) Microprocessor mode [01]

The microcomputer will be placed in the microprocessor mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01".

In this mode, the internal ROM is inhibited so the external memory is required.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D₇-D₀) and loses its normal output functions. Port P3₁ and P3₀ become the SYNC and R/W pins, respectively and the normal I/O functions are lost.

(3) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode.

In this mode, the internal ROM is inhibited so the external memory is required.

The lower 8 bits of address data for port P0 is output when φ goes to the "H" state. When φ goes to the "L" state, P0 retains its original output functions.

Port P1's higher 8 bits of address data are output when φ goes to "H" state and as it changes back to the "L" state it retains its original output functions. Port P2 retains its original output functions while φ is at the "H" state, and works as a data bus of D₇-D₀ (including instruction code) while at the "L" state. Pins P3₁ and P3₀ output the SYNC and R/W control signals, respectively while φ is in the "H" state. When in the "L" state, P3₁ and P3₀ retain their original I/O function.

The R/W output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 8.

Note : Use the M37103M4-XXXSP in the microprocessor mode or the memory expanding mode only at program development.

The standards is assured only in the single-chip mode.

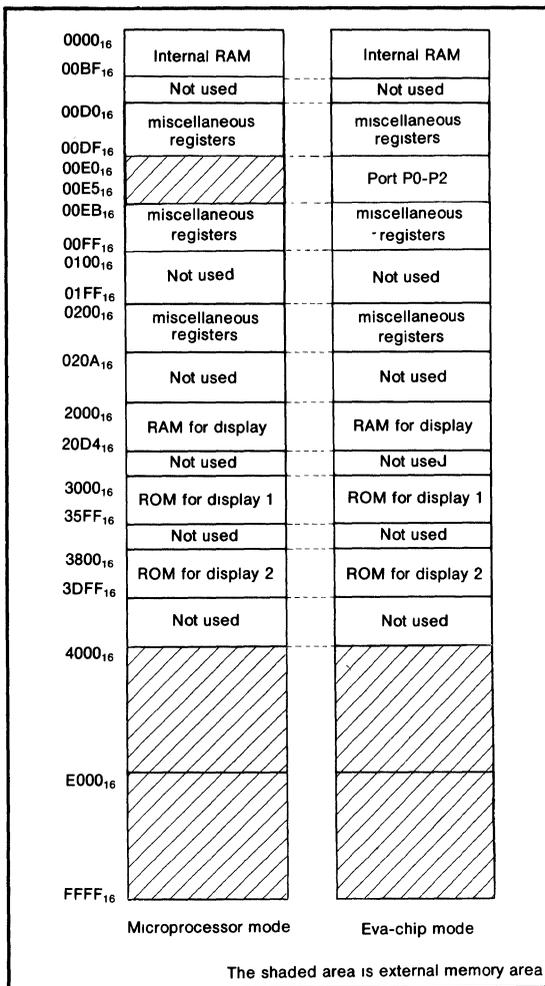


Fig. 36 Example memory area in processor mode

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

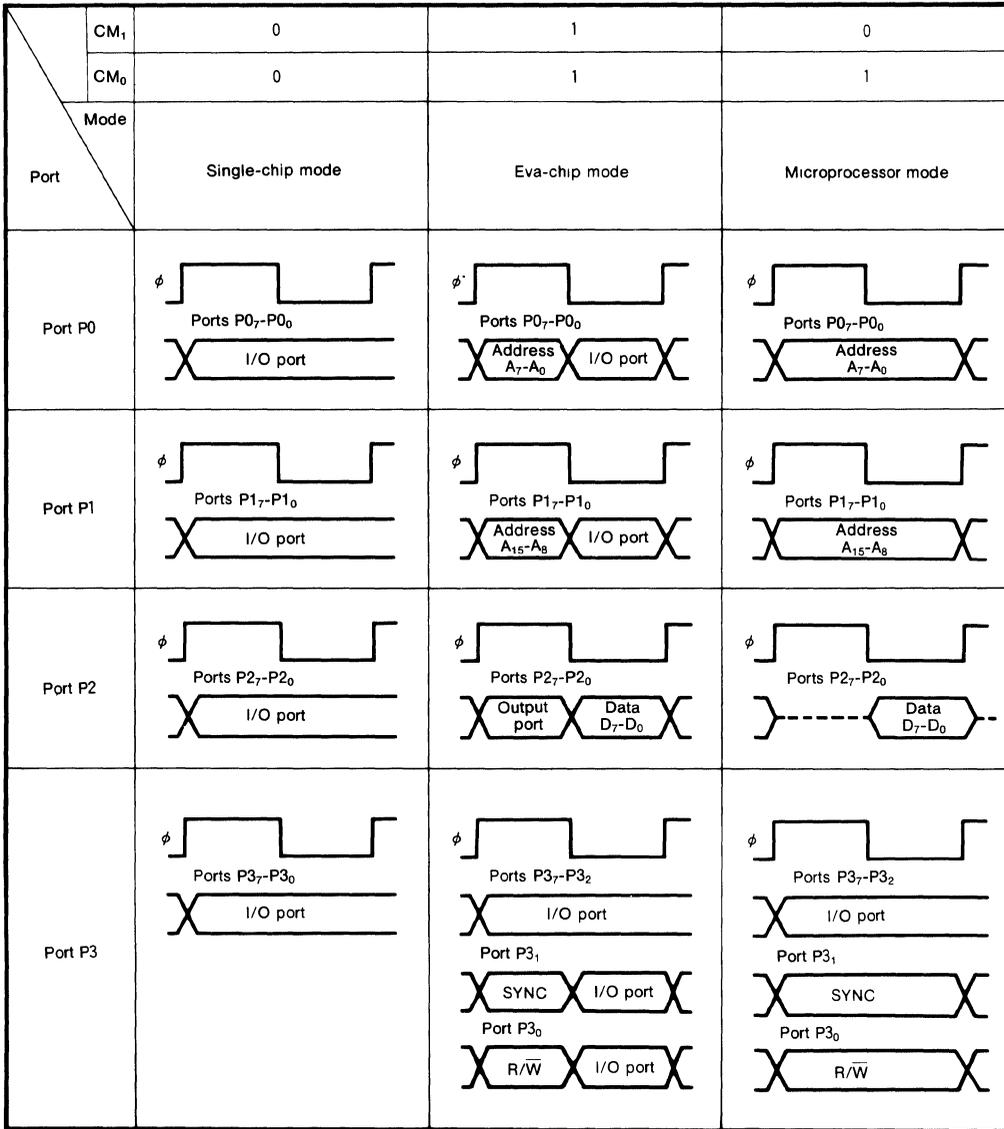


Fig. 37 Processor mode and functions of ports P0-P3

Table 8. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode • Eva-chip mode • Microprocessor mode 	The single-chip mode is set by the reset All modes can be selected by changing the processor mode bit with the program
10V	<ul style="list-style-type: none"> • Eva-chip mode 	Eva-chip mode only

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

CLOCK GENERATING CIRCUIT

The M37103M4-XXXSP has two internal clock generating circuits. Figure 40 shows a block diagram of the clock generating circuits. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ . Bit 7 of serial I/O mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN} .

Figure 38 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 39.

The M37103M4-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 2 and timer 3 are forcibly connected and $\phi/8$ is selected as timer 2 input. When restarting oscillation, FF_{16} is automatically set in timer 2 and 07_{16} in timer 3 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 2 count stop bit must be set to supply ("0"), timer 2 interrupt enable bit and timer 3 interrupt enable bit must be set to disable ("0").

Oscillation is restarted (release the stop mode) when INT_1 , INT_2 , or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt or reset, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($60\mu A$ or less at $f(X_{CIN})=32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. Figure 41 shows the transition of states for the system clock.

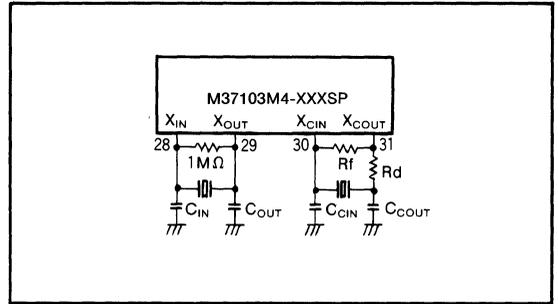


Fig. 38 Example ceramic resonator circuit

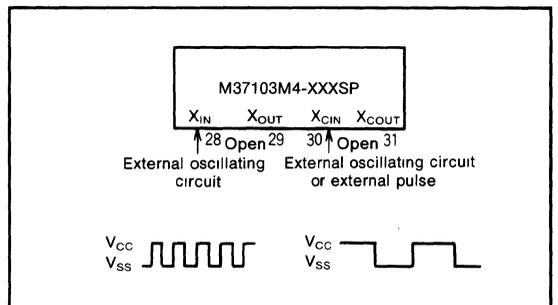


Fig. 39 Example clock input circuit

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

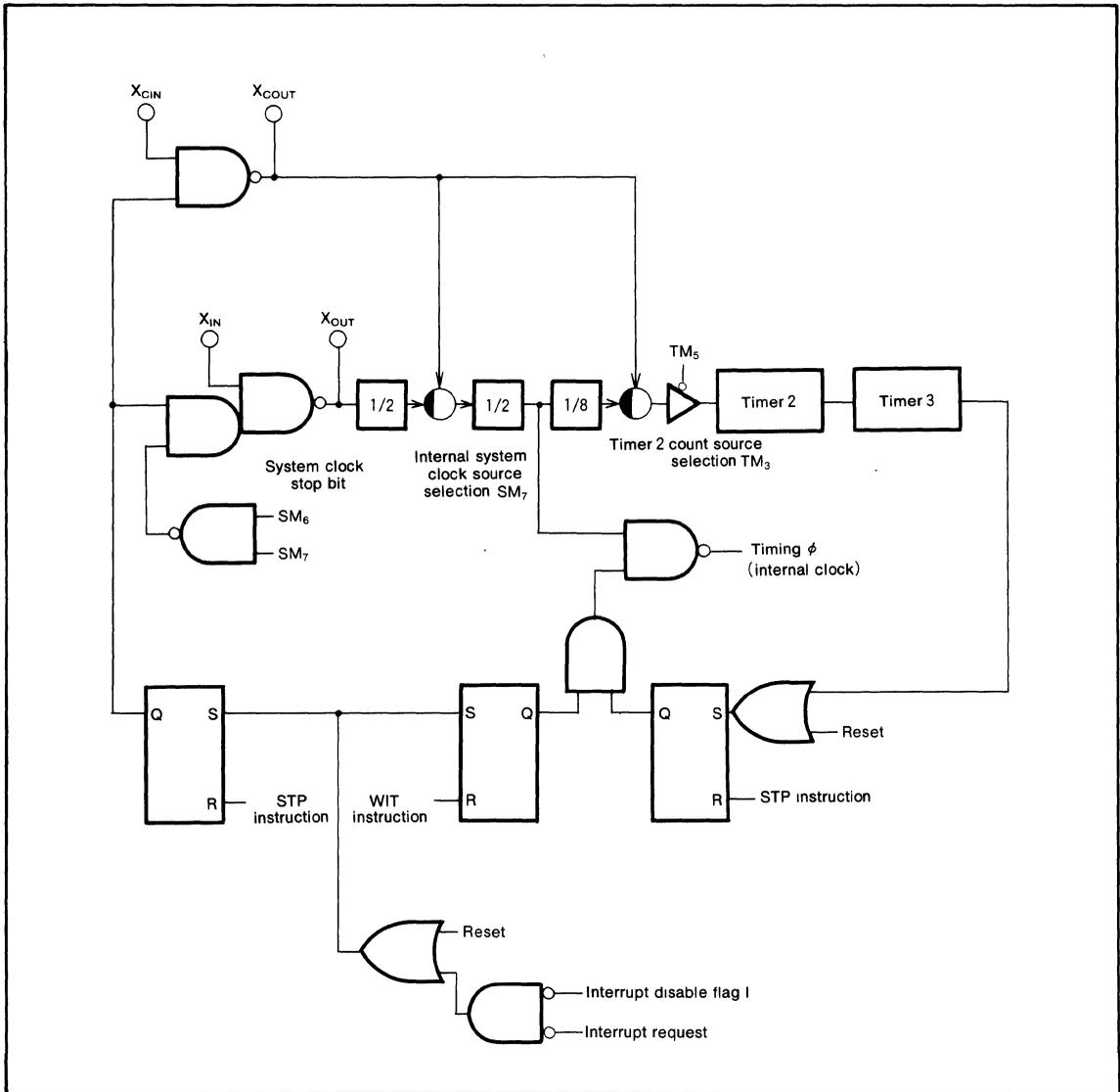


Fig. 40 Block diagram of clock generating circuit

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
 with ON-SCREEN DISPLAY CONTROLLER**

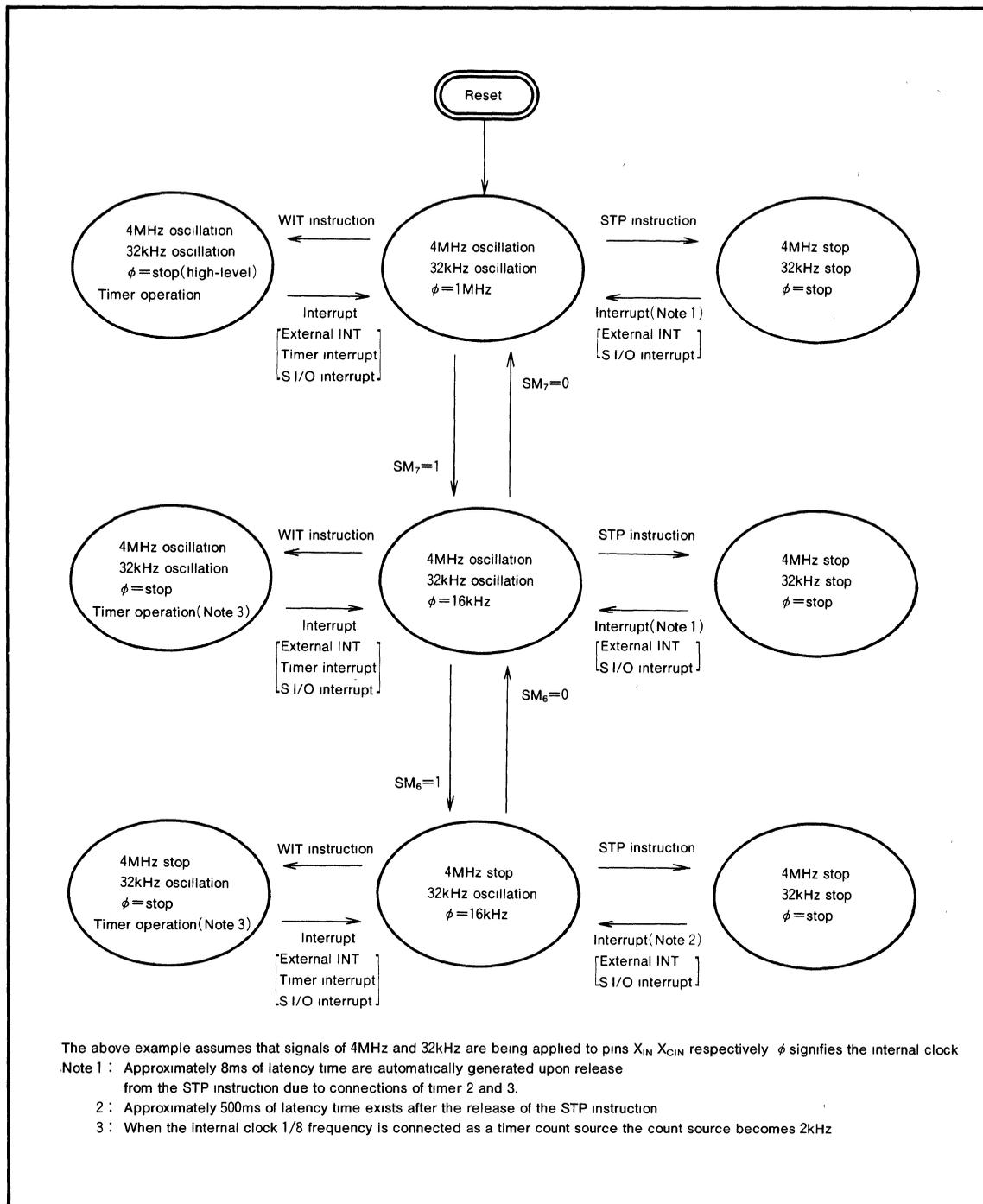
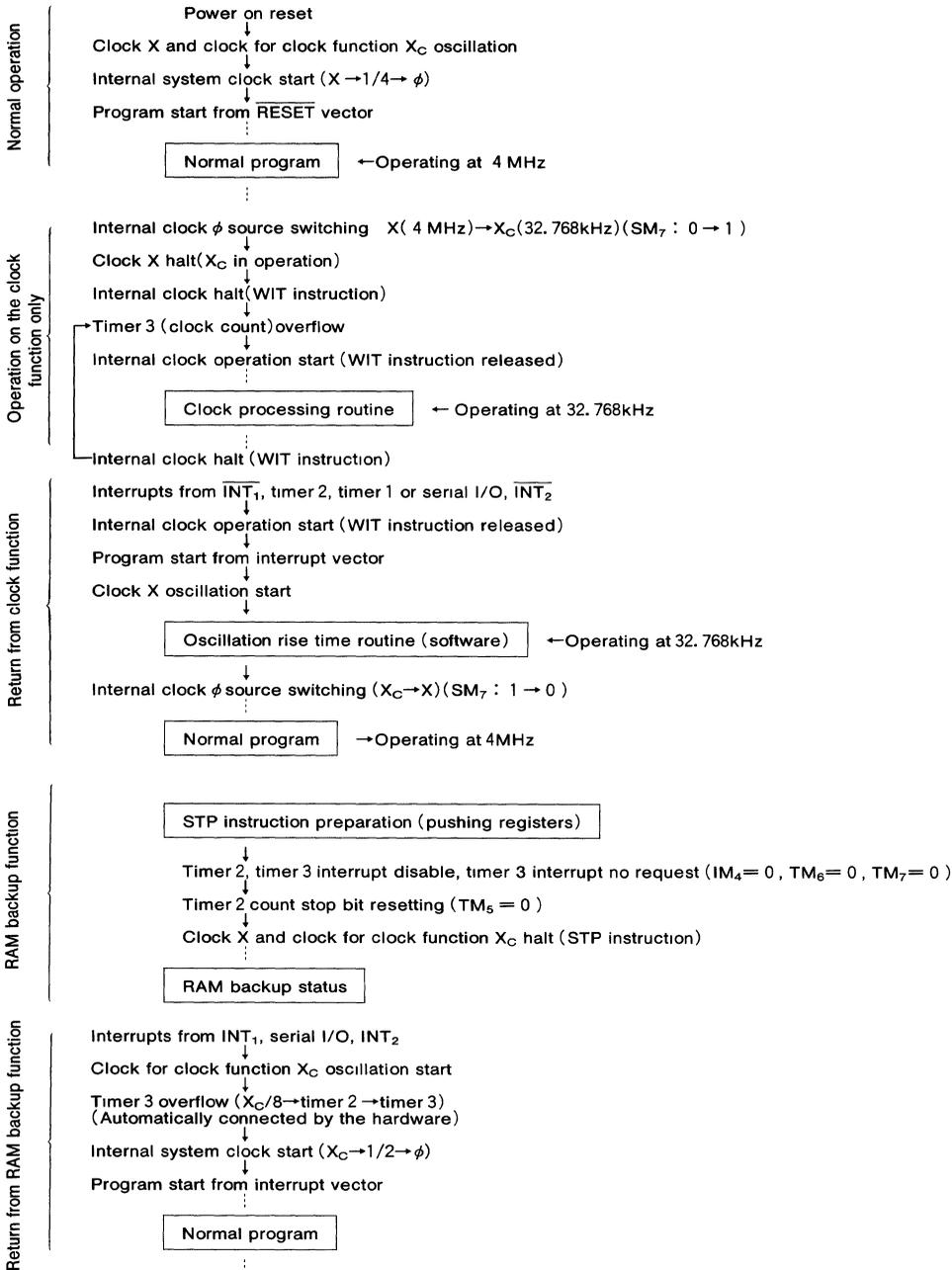


Fig. 41 Transition of states for the system clock

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

<An example of flow for system>



**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

PROGRAMMING NOTES

- (1) Processor status register
 1. Except for the interrupt inhibit flag (I) being set to "1", the content of the processor status register (PS) is unpredictable after a reset. Therefore, flags affecting program execution must be initialized.
The T flag and D flag which affect arithmetic operations, must always be initialized.
 2. A NOP instruction must be used after the execution of a PLP instruction.
- (2) Interrupts

Even though the BBC and BBS instructions are executed just after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) Decimal operations
 1. Decimal operations are performed by setting the decimal mode flag (D) and executing the ADC or SBC instruction. In this case, there must be at least one instruction following the ADC or SBC instruction before executing the SEC, CLC, or CLD instruction.
 2. The N (Negative), V (Overflow), and Z (Zero) flags are ignored during decimal mode.
- (4) Timers

The frequency dividing ratio of timer is $1/(n+1)$.
- (5) STP instruction

The STP instruction must be executed after setting the timer 2 count stop bit (bit 5 at address 00FF₁₆) to supply ("0").

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- mask ROM order confirmation form
- mark specification form
- ROM data.....EPROM 3 sets

Write the following option on the mark confirmation form

- (1) Port P1 pull-up transistor bit
- (2) Port P2 pull-up transistor bit
- (3) X_{IN} and X_{CIN} oscillation feed-back resistor
- (4) CRT display signal input/output polarity
- (5) ϕ output

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3 to 6	V
V_i	Input voltage RESET, CNV _{SS}		-0.3 to 13	V
V_i	Input voltage P ₀ -P ₀ , P ₁ -P ₁ , P ₂ -P ₂ , P ₃ -P ₃ , P ₄ , P ₅ -P ₅ , P ₆ -P ₆ , H _{SYNC} , V _{SYNC} , X _{IN} , X _{CIN} , OSC1	With respect to V _{SS} Output transistors are at "off" state	-0.3 to V _{CC} +0.3	V
V_O	Output voltage P ₀ -P ₀ , P ₅ , P ₅ -P ₅ , P ₆ -P ₆		-0.3 to 13	V
V_O	Output voltage P ₁ -P ₁ , P ₂ -P ₂ , P ₃ -P ₃ , P ₄ , P ₅ , P ₅ , P ₆ , P ₆ , X _{OUT} , ϕ , X _{COUT} , OSC2, R, G, B, I, OUT		-0.3 to V _{CC} +0.3	V
I_{OH}	Circuit current P ₆ , P ₆ , P ₄ , R, G, B, I, OUT		0 to 10 (Note 1)	mA
I_{OL1}	Circuit current P ₁ -P ₁ , P ₂ -P ₂ , P ₃ -P ₃ , P ₄ , P ₅ , P ₅ , P ₆ , P ₆ , R, G, B, I, OUT		0 to 15 (Note 2)	mA
I_{OL2}	Circuit current P ₀ -P ₀ , P ₅ , P ₅ -P ₅ , P ₆ -P ₆	V ₀ ≤ 7V V ₀ > 7V	0 to 15 (Note 2) 0 to 1 (Note 2)	mA
P_d	Power dissipation	T _a = 25°C	1000	mW
T_{opr}	Operating temperature		-10 to 70	°C
T_{stg}	Storage temperature		-40 to 125	°C

Note 1 : The total of I_{OH} should be 20mA(max)

2 : The total of I_{OL1} and I_{OL2} should be 50mA(max)

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=-10 to 70°C unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage (Note 1)	Normal speed mode f(X _{IN})=4MHz f(OSC1)=5MHz	4.5	5.0	5.5	V
		Low-speed mode f(X _{CIN})=32kHz	3.0	5.0	5.5	
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	"H" input voltage P ₀ -P ₀ , P ₁ -P ₁ , P ₂ -P ₂ , P ₃ -P ₃ , P ₄ , P ₅ -P ₅ , P ₆ -P ₆ , X _{IN} , X _{CIN} , RESET, H _{SYNC} , V _{SYNC}		0.8V _{CC}		V _{CC}	V
V_{iL}	"L" input voltage P ₀ -P ₀ , P ₁ -P ₁ , P ₂ -P ₂ , P ₃ , P ₃ , P ₃ -P ₃ , P ₃ , P ₄ , P ₅ , P ₅ , P ₅ , P ₅ , P ₆ -P ₆		0		0.4V _{CC}	V
V_{iL}	"L" input voltage P ₃ , P ₃ , P ₅ , P ₅ , P ₅ , RESET, X _{IN} , X _{CIN} , H _{SYNC} , V _{SYNC}		0		0.2V _{CC}	V
$I_{OL(avg)}$	"L" average output current P ₀ -P ₀ , P ₁ -P ₁ , P ₂ -P ₂ , P ₃ -P ₃ , P ₄ , P ₅ -P ₅ , P ₆ -P ₆ , R, G, B, I, OUT				5	mA
$I_{OL(avg)}$	"L" average output current P ₀ -P ₀ , P ₅ , P ₅ -P ₅ , P ₆ -P ₆	V ₀ ≤ 7V			5	mA
		V ₀ > 7V			1	
$I_{OH(avg)}$	"H" average output current P ₄ , P ₆ , P ₆ , R, G, B, I, OUT				2	mA
f(X _{IN})	Oscillating frequency (Note 2)		3.6	4	4.4	MHz
f(X _{CIN})	Oscillating frequency		29	32	35	kHz
f(OSC1)	Oscillating frequency		4	5	6	MHz

Note 1 : Apply 0.022μF or greater capacitance externally to the V_{CC} power supply pin so as to reduce power source noise

2 : Use a quartz crystal oscillator or a ceramic resonator for the CPU oscillating circuit

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

ELECTRIC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10$ to $70^\circ C$, $f(X_{IN})=4MHz$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
V_{OH}	"H" output voltage P47, P60, P61, R, G, B, I, OUT	$V_{CC}=4.5V$, $I_{OH}=-0.5mA$	2.4			V
V_{OH}	"H" output voltage ϕ	$V_{CC}=4.5V$ $I_{OH}=-2.5mA$	2.4			V
V_{OL}	"L" output voltage P00-P07, P20-P27, P30-P37, P47, P51-P57, P60-P65, R, G, B, I, OUT	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
V_{OL}	"L" output voltage P10-P17	$V_{CC}=4.5V$ $I_{OL}=10mA$			1.5	V
V_{OL}	"L" output voltage ϕ	$V_{CC}=4.5V$ $I_{OL}=2.5mA$			2	V
$V_{T+} - V_{T-}$	Hysteresis \overline{RESET}	$V_{CC}=5.0V$		0.5	0.7	V
$V_{T+} - V_{T-}$	Hysteresis P32, P36, P47, P52, P53, P56, H _{SYNC} , V _{SYNC} , X _{CIN} (Note 2)	$V_{CC}=5.0V$		0.5	1.3	V
R_U	Pull-up transistor (Note 1) P10-P17, P20-P27	$V_{CC}=5.0V$ $V_I=0V$	15	30	60	k Ω
I_{OZH}	"H" input current P00-P07, P10-P17, P20-P27, P30-P37, P47, P51-P57, P60-P65, \overline{RESET} , X _{IN} , X _{CIN} , H _{SYNC} , V _{SYNC}	$V_{CC}=5.5V$ $V_O=5.5V$			5	μA
I_{OZH}	"H" input leak current P00-P07, P51, P54-P57, P60-P65	$V_{CC}=5.5V$ $V_O=12V$			10	μA
I_{OZL}	"L" input leak current P00-P07, P10-P17, P20-P27, P30-P37, P47, P51-P57, P60-P65, H _{SYNC} , V _{SYNC} , X _{CIN} , \overline{RESET}	$V_{CC}=5.5V$ $V_O=0V$			5	μA
V_{RAM}	RAM retention voltage	At stop mode	2.5		5.5	V
I_{CC}	Supply current	$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ At system operation and CRT display off		5	10	mA
		$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ At system operation and CRT display on		7	14	
		$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ At wait mode		1		
		X _{IN} -X _{OUT} stop $f(X_{CIN})=32kHz$	$V_{CC}=5.5V$	60	200	μA
		At system operation	$V_{CC}=3V$	25		
		X _{IN} -X _{OUT} stop $f(X_{CIN})=32kHz$	$V_{CC}=5.5V$	25	100	
		At wait mode	$V_{CC}=3V$	5		
		At stop mode	$V_{CC}=5.5V$	1	10	
			$V_{CC}=3V$	0.6		

Note 1 : Pull-up transistor is mask option
2 : Hysteresis of X_{CIN} is only when this port is used as timer 4 input

MITSUBISHI MICROCOMPUTERS

M37202M3-XXXSP

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

DESCRIPTION

The M37202M3-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This single-chip microcomputer is useful for the high-tech channel selection system for TVs and VTRs.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

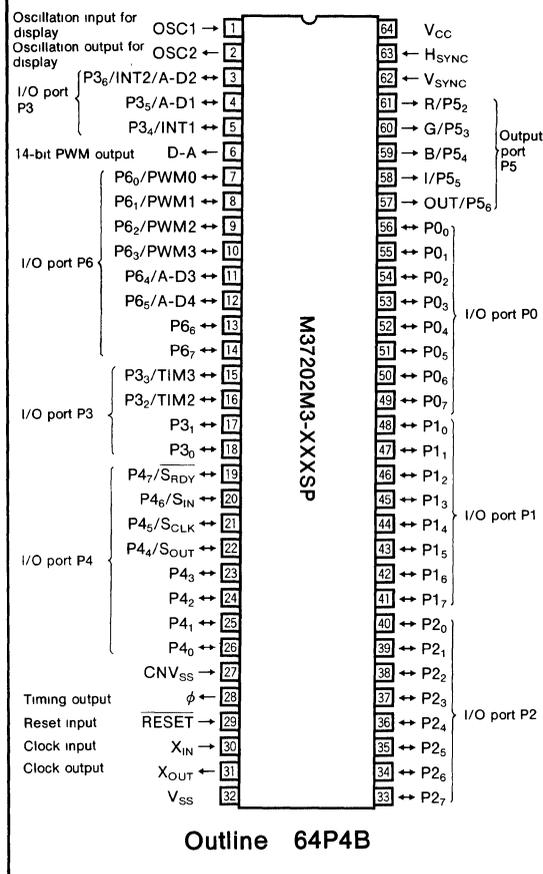
FEATURES

- Number of basic instructions 69
- Memory size ROM 12288 bytes
RAM 256 bytes
- Instruction execution time
..... 1 μ s (minimum instructions at 4MHz frequency)
- Single power supply 5V \pm 10%
- Power dissipation
normal operation mode (at 4MHz frequency)
..... 110mW (V_{CC} =5.5V, CRT display)
- Subroutine nesting 96 levels (Max.)
- Interrupt 12 types, 12 vectors
- 8-bit timer 4
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P6) 47
- Output port (Port P5) 5
- Serial I/O (8-bit) 1
- Special serial I/O (I²C bus* format) 1
- PWM function 14-bit \times 1
8-bit \times 4
- A-D converter (4-bit resolution) 4 channels
- 72-character on screen display function
Number of character 24 characters \times 3 lines
Kinds of character 94

APPLICATION

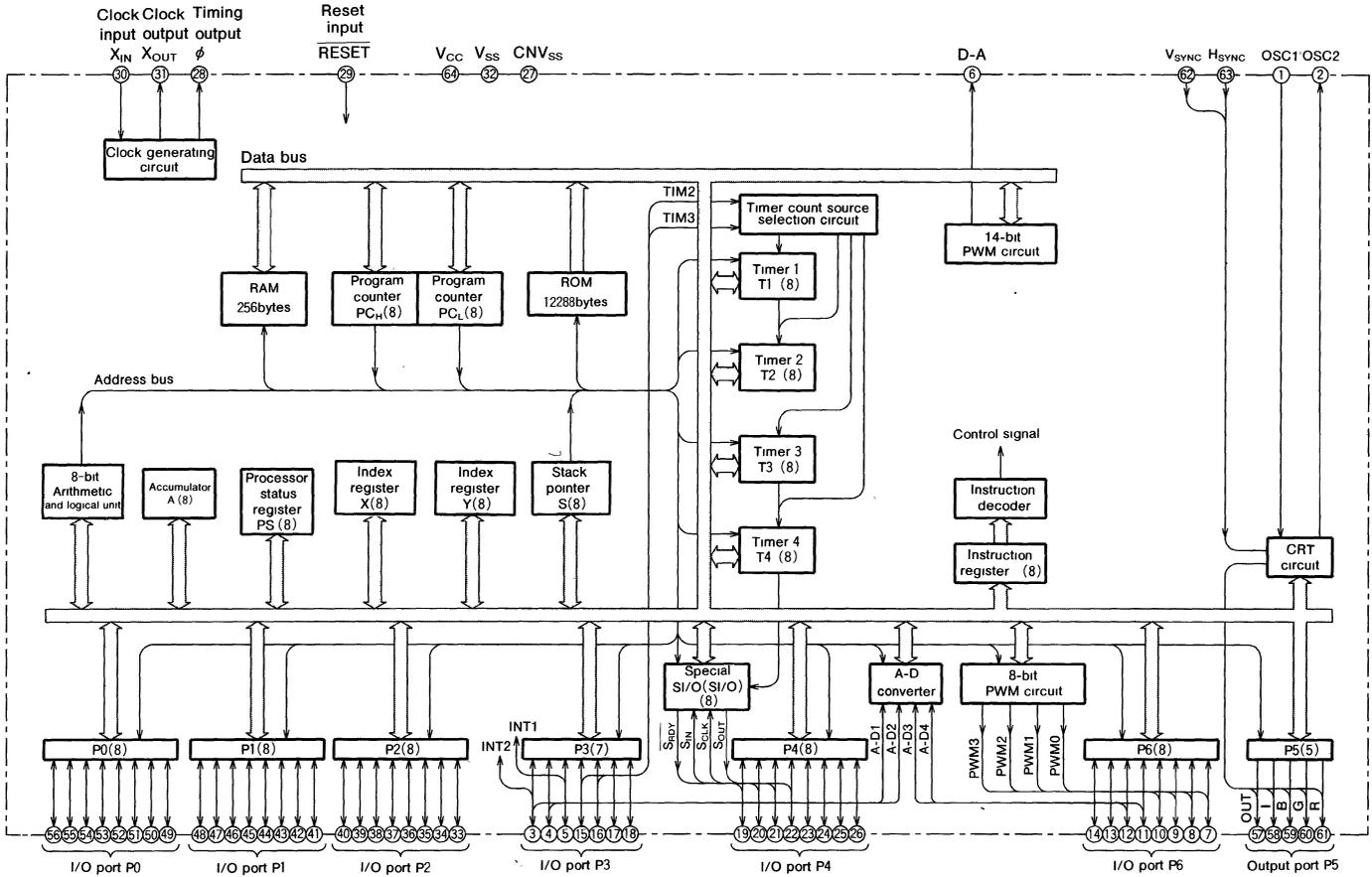
TV, VTR

PIN CONFIGURATION (TOP VIEW)



* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

M37202M3-XXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

MITSUBISHI MICROCOMPUTERS
M37202M3-XXXSP



**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

FUNCTIONS OF M37202M3-XXXSP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		1 μ s (minimum instructions, at 4MHz frequency)	
Clock frequency		4MHz	
Memory size	ROM	12288 bytes	
	RAM	256 bytes	
Input/Output ports	P0, P1, P2	I/O	8-bitX3
	P3 ₀ , P3 ₁	I/O	2-bitX1
	P3 ₂ -P3 ₆	I/O	5-bitX1 (can be used as timer input pins, INT1, INT2 input pins and A-D input pins)
	P4 ₀ -P4 ₃	I/O	4-bitX1
	P4 ₄ -P4 ₇	I/O	4-bitX1 (can be used as serial I/O pins)
	P5	Output	5-bitX1 (can be used as R, G, B, I, OUT pins)
	P6 ₀ -P6 ₅	I/O	6-bitX1 (can be used as PWM output pins and A-D input pins)
P6 ₆ , P6 ₇	I/O	2-bitX1	
Serial I/O		8-bitX1 (Special serial I/O (8-bit)X1)	
A-D converter		4-bit (4-channel)	
Pulse width modulator		14-bitX1, and 8-bitX4	
Timers		8-bit timerX4	
Subroutine nesting		96levels (max)	
Interrupt		Two external interrupts, eight internal interrupts, one software interrupt	
Clock generating circuit		Two built-in circuits (externally connected ceramic or quartz crystal oscillator)	
Supply voltage		5V \pm 10%	
Power dissipation	at CRT display ON	110mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)	
	at CRT display OFF	55mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)	
	at stop mode	1.65mW (Max)	
Input/Output characteristics	Input/Output voltage	12V (Port P4 ₀ ~P4 ₃ , P4 ₆ , P4 ₇ , P6 ₀ ~P6 ₃ , P6 ₆ , P6 ₇)	
	Output current	10mA (Port P2 ₄ ~P2 ₇)	
Operating temperature range		-10 to 70°C	
Device structure		CMOS silicon gate process	
Package		64-pin shrink plastic molded DIP	
CRT display function	Number of character	24 charactersX3 lines (maximum 16 lines by software)	
	Kinds of character	94 (12X16 dots)	
	Character size	4 types	
	Color	15 types (Max) specified by character unit	
	Display position	64 (horizontal direction)X128 (vertical direction)	

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% (typ) to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is connected to V _{SS}
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2 μ s (under normal V _{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin
P0 ₀ to P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output
P1 ₀ to P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0
P2 ₀ to P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0
P3 ₀ to P3 ₆	I/O port P3	I/O	Port P3 is an 7-bit I/O port and has basically the same functions as port P0, but the output structure of P3 ₀ , P3 ₁ is CMOS output and the output structure of P3 ₂ to P3 ₆ is N-channel open drain P3 ₂ , P3 ₃ are in common with external clock input pins of timer 2 and 3. P3 ₄ , P3 ₅ are in common with external interrupt input pins INT1 and INT2. P3 ₅ , P3 ₆ are in common with analog input pins of A-D converter (A-D1, A-D2)
P4 ₀ to P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain When serial I/O is used, P4 ₄ , P4 ₅ , P4 ₆ and P4 ₇ work as S _{OUT} , S _{CLK} , S _{IN} and S _{RDY} pins, respectively. Also P4 ₄ , P4 ₅ are in common with special serial I/O pins of SDA and SCL
P6 ₀ to P6 ₇	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. Port P6 ₀ to P6 ₃ are in common with PWM output pins PWM0 to PWM3. Port P6 ₄ and P6 ₅ are in common with A-D converter analog input pins A-D3 and A-D4
OSC1, OSC2	Clock input/output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display function
H _{SYNC}	H _{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display.
V _{SYNC}	V _{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display
R, G, B, I, OUT	CRT output	Output	This is an 5-bit output pin for CRT display. The output structure is CMOS output. This is in common with port P5 ₂ to P5 ₆
D-A	DA Output	Output	This is a output pin for 14-bit PWM. The output structure is CMOS output

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FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37202 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address 00FB₁₆. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

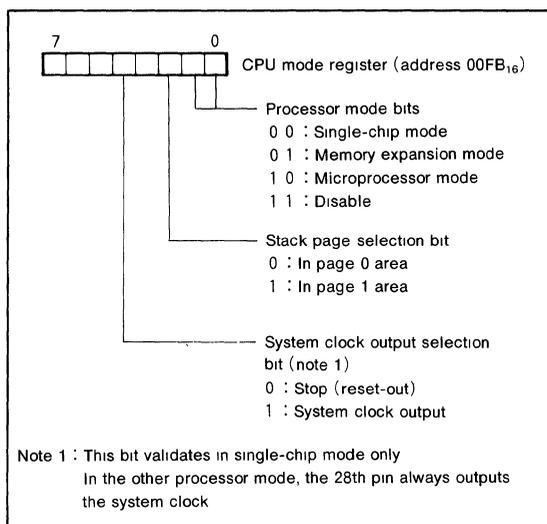


Fig. 1 Structure of CPU mode register

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MEMORY

- Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- RAM

RAM is used for data storage as well as a stack area

- ROM

ROM is used for storing user programs as well as the interrupt vector area.

- Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

- Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

- Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

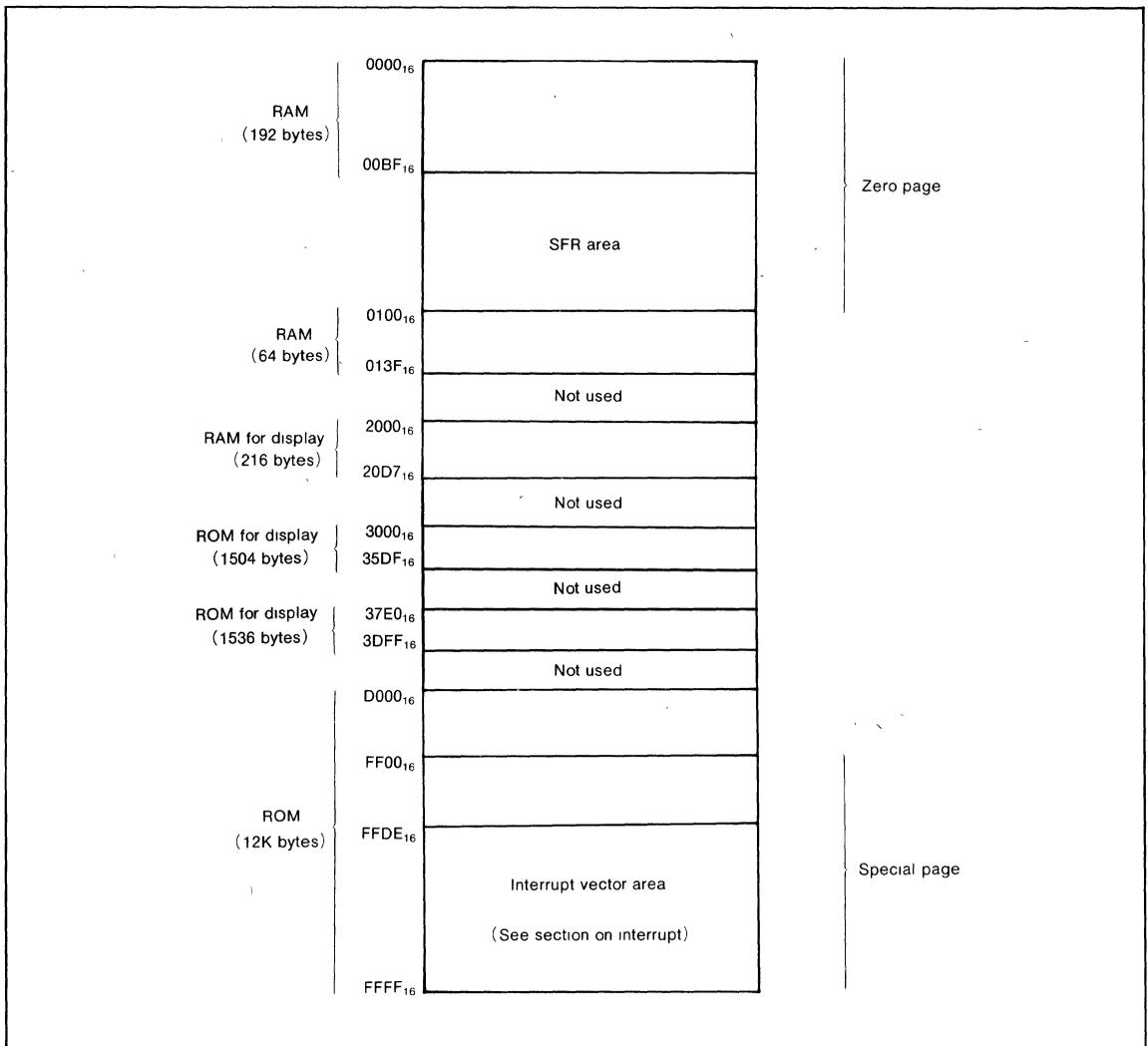


Fig. 2 Memory map

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00C0 ₁₆	Port P0	00E0 ₁₆	Horizontal position register
00C1 ₁₆	Port P0 direction register	00E1 ₁₆	Vertical display start position register 1
00C2 ₁₆	Port P1	00E2 ₁₆	Vertical display start position register 2
00C3 ₁₆	Port P1 direction register	00E3 ₁₆	Vertical display start position register 3
00C4 ₁₆	Port P2	00E4 ₁₆	Character size register
00C5 ₁₆	Port P2 direction register	00E5 ₁₆	Border selection register
00C6 ₁₆	Port P3	00E6 ₁₆	Color register 0
00C7 ₁₆	Port P3 direction register	00E7 ₁₆	Color register 1
00C8 ₁₆	Port P4	00E8 ₁₆	Color register 2
00C9 ₁₆	Port P4 direction register	00E9 ₁₆	Color register 3
00CA ₁₆	Port P5	00EA ₁₆	CRT control register
00CB ₁₆	Port P5 direction register	00EB ₁₆	Display block counter
00CC ₁₆	Port P6	00EC ₁₆	CRT port control register
00CD ₁₆	Port P6 direction register	00ED ₁₆	
00CE ₁₆	DA-H register	00EE ₁₆	
00CF ₁₆	DA-L register	00EF ₁₆	A-D control register
00D0 ₁₆	PWM 0 register	00F0 ₁₆	Timer 1
00D1 ₁₆	PWM 1 register	00F1 ₁₆	Timer 2
00D2 ₁₆	PWM 2 register	00F2 ₁₆	Timer 3
00D3 ₁₆	PWM 3 register	00F3 ₁₆	Timer 4
00D4 ₁₆		00F4 ₁₆	Timer 12 mode register
00D5 ₁₆	PWM output control register 1	00F5 ₁₆	Timer 34 mode register
00D6 ₁₆	PWM output control register 2	00F6 ₁₆	
00D7 ₁₆	Interrupt interval determination register	00F7 ₁₆	
00D8 ₁₆	Interrupt interval determination control register	00F8 ₁₆	
00D9 ₁₆	Special serial I/O register	00F9 ₁₆	
00DA ₁₆	Special mode register 1	00FA ₁₆	
00DB ₁₆	Special mode register 2	00FB ₁₆	CPU mode register
00DC ₁₆		00FC ₁₆	Interrupt request register 1
00DD ₁₆		00FD ₁₆	Interrupt request register 2
00DE ₁₆	Serial I/O mode register	00FE ₁₆	Interrupt control register 1
00DF ₁₆	Serial I/O register	00FF ₁₆	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 11 different events consisting of three external, seven internal, and one software events. Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed as described in the stack pointer (S) section above, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

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Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
CRT interrupt	2	FFFD ₁₆ , FFFC ₁₆	
INT2 interrupt	3	FFFB ₁₆ , FFFA ₁₆	
INT1 interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	
Serial I/O interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	
Timer 4 interrupt	6	FFF5 ₁₆ , FFF4 ₁₆	
1 ms interrupt	7	FFF3 ₁₆ , FFF2 ₁₆	
V _{SYNC} interrupt	8	FFF1 ₁₆ , FFF0 ₁₆	
Timer 3 interrupt	9	FFEF ₁₆ , FFEE ₁₆	
Timer 2 interrupt	10	FFED ₁₆ , FFEC ₁₆	
Timer 1 interrupt	11	FFEB ₁₆ , FFEA ₁₆	
BRK instruction interrupt	12	FFDF ₁₆ , FFDE ₁₆	Non-maskable software interrupt

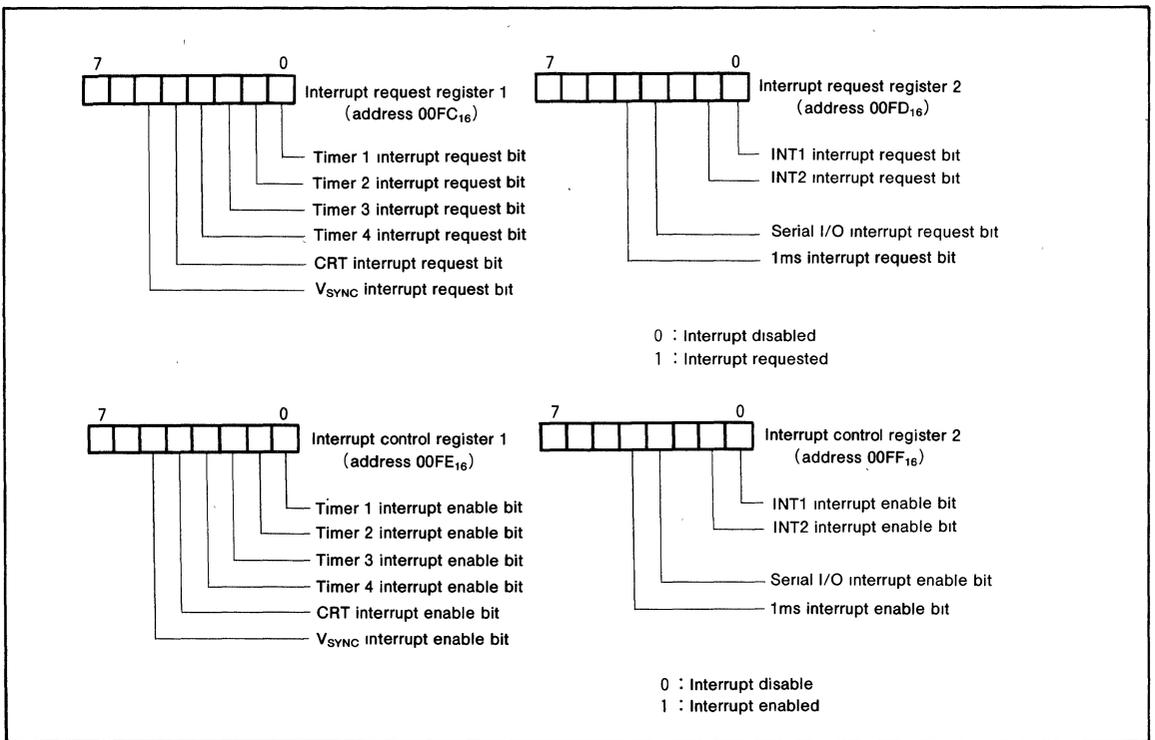


Fig. 4 Structure of registers related with interrupt

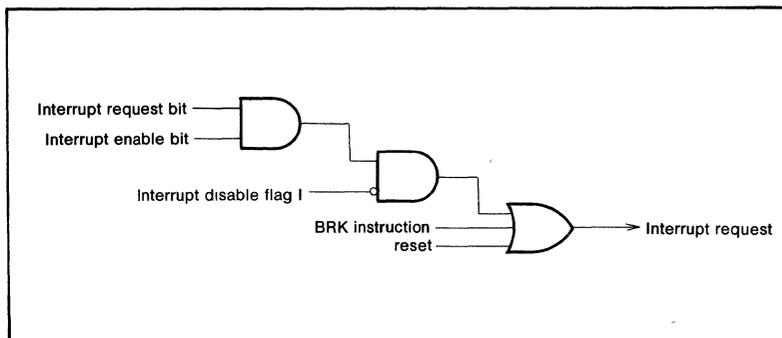


Fig. 5 Interrupt control

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TIMER

The M37202M3-XXXSP has four timers; timer 1, timer 2, timer 3 and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 7.

The count source for timer 1 through 4 can be selected by using bit 0, 1, 4 of timer 12 mode register and timer 34 mode register (address 00F4₁₆, 00F5₁₆), as shown in Figure 6.

All of the timers are down count timers and have 8-bit latches. When a timer reaches "00₁₆" and the next count pulse is input to a timer, a value which is subtracted 1 from the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch. The timer interrupt request bit is set at the next count pulse after the timer reaches "00₁₆".

The starting and stopping of the timer is controlled by bit 2, 3 of timer 12 mode register and timer 34 mode register.

At a reset or stop mode, FF₁₆ is automatically set in timer 3 and 07₁₆ in timer 4 and timer 4, timer 3 and the clock ($f(X_{IN})$ divided by 16) are connected in series.

When restarting oscillation or canceling a reset, the internal clock is not supplied to the CPU until timer 4 overflows.

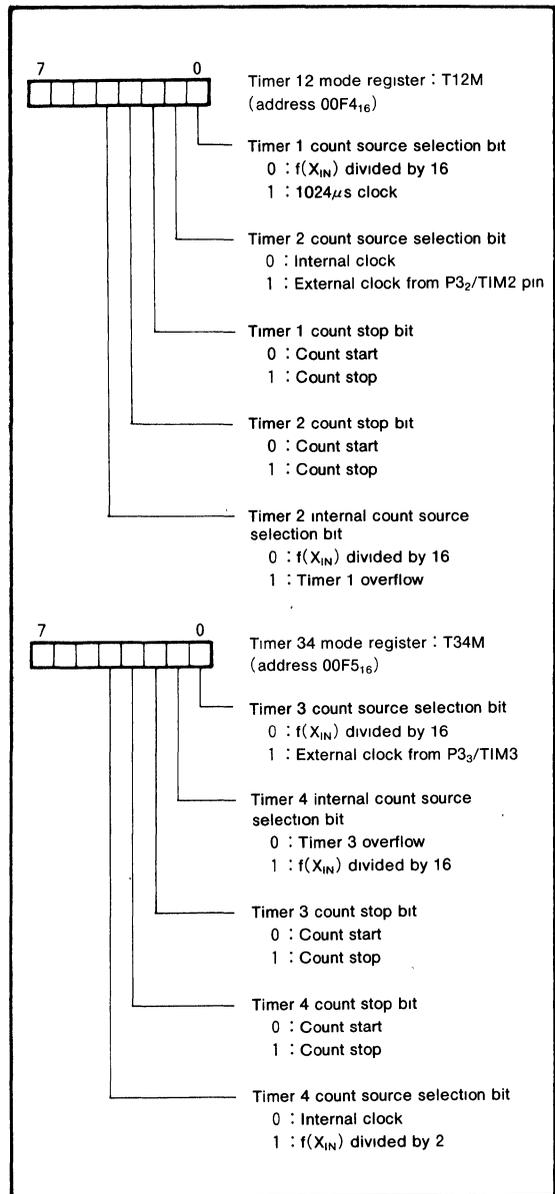


Fig. 6 Structure of timer 12 mode register and timer 34 mode register

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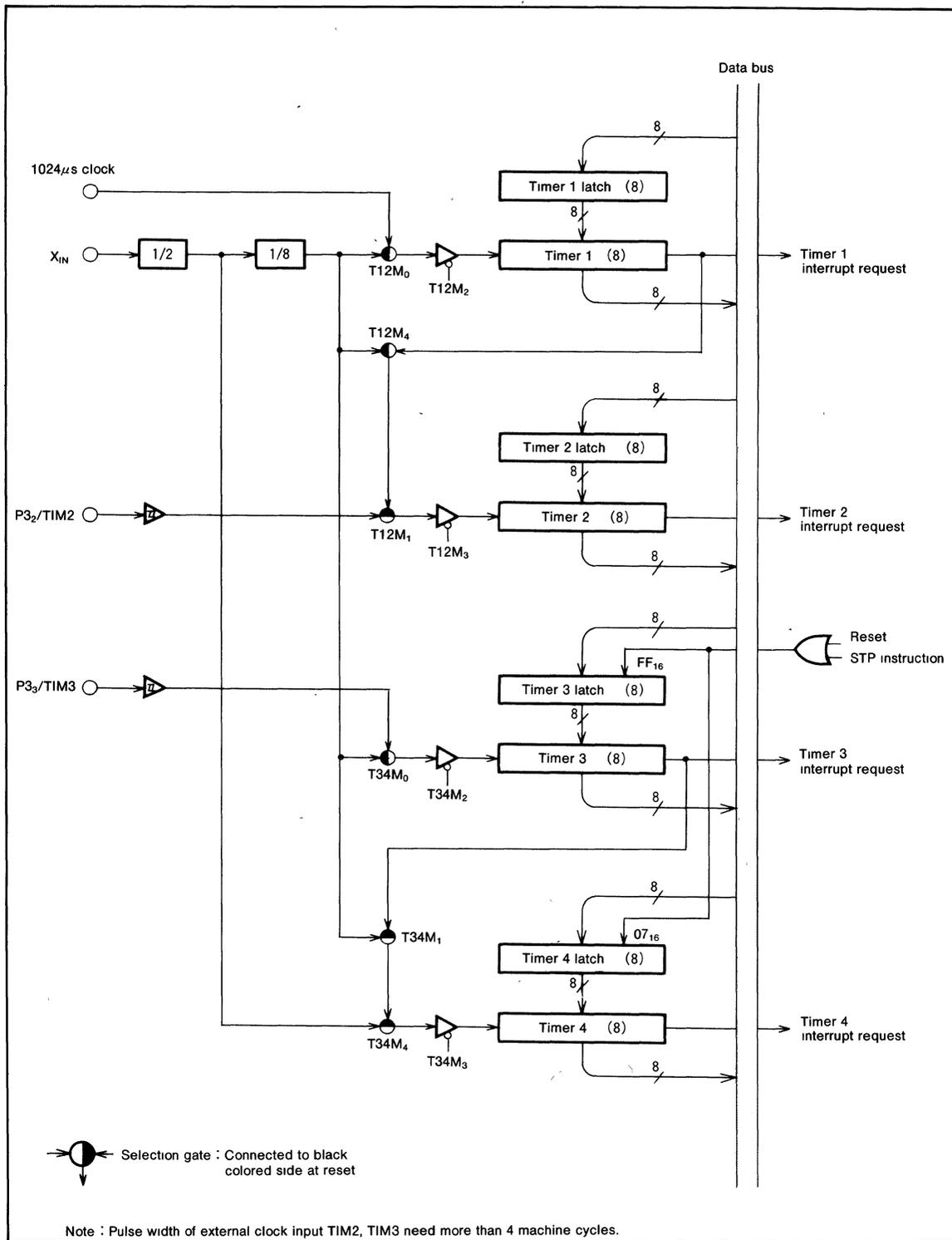


Fig. 7 Block diagram of timer 1, timer 2, timer 3 and timer 4

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SERIAL I/O

A block diagram of the serial I/O is shown in Figure 8. In the serial I/O mode, port P4₄ to P4₇ are used as the serial I/O pins (S_{OUT} and S_{IN}), synchronous input/output clock pin (S_{CLK}), and the receive ready signal pin (S_{RDY}). The serial I/O mode registers (address 00DE₁₆) are 8-bit registers. Bits 0, 1 and 2 of these registers are used to select a synchronous clock source. Bit 3 and 4 decide whether port P4 will be used as a serial I/O or not.

To use P4₆ as a serial input, set the directional register bit which corresponds to P4₆ to "0". For more information on the directional register, refer to the I/O pin section. Also to use internal clock of serial I/O, bit 1 of special mode register 1 (address 00DA₁₆) needs to be set to "1". The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

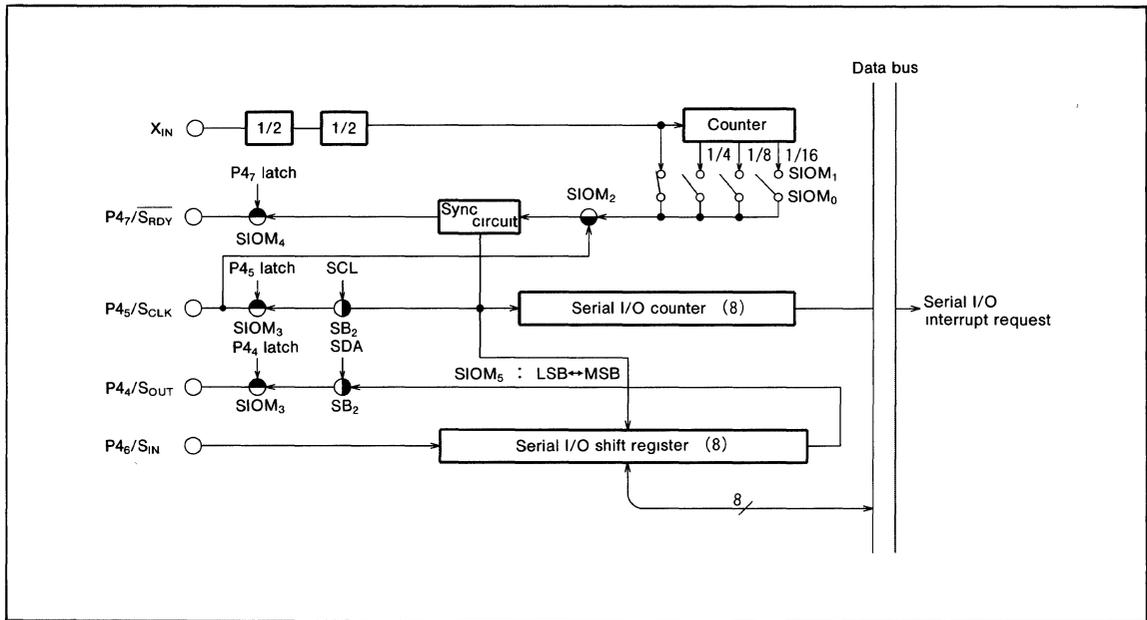


Fig. 8 Block diagram of serial I/O

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Internal clock—The $\overline{S_{RDY}}$ signal becomes “H” during transmission or while dummy data is stored in the serial I/O register (address 00DF₁₆). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37202M3-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes “H” at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to S_{OUT} . During the rising edge of this clock, data can be input from S_{IN} and the data in the serial I/O register will be shifted 1 bit.

Transfer direction can be selected by bit 5 of serial I/O mode register. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request

bit will be set.

External clock- If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. When using an external clock for transfer, the external clock must be held at “H” level when the serial I/O counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

An example of communication between two M37202M3-XXXSPs is shown in Figure 10.

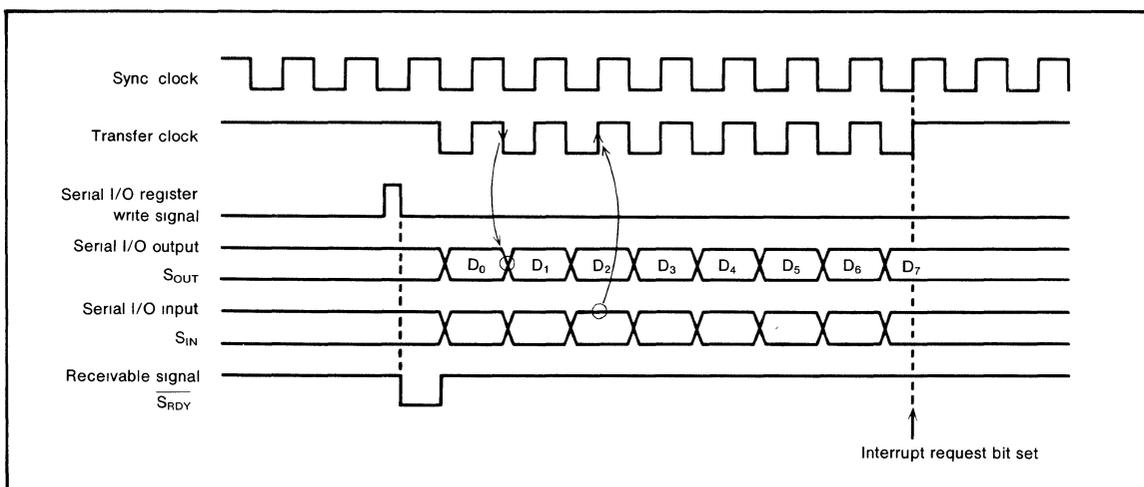


Fig. 9 Serial I/O timing

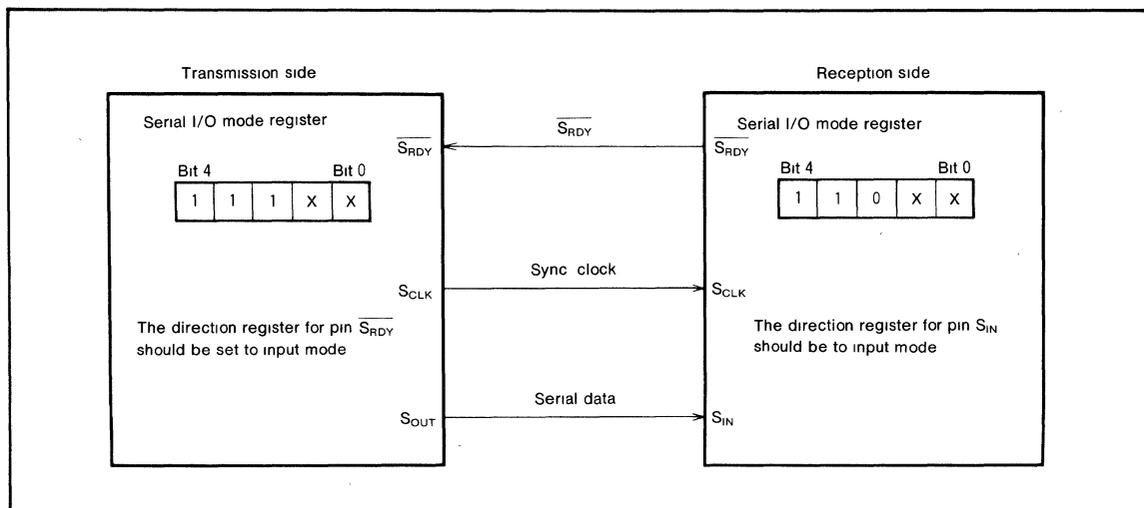


Fig. 10 Example of serial I/O connection

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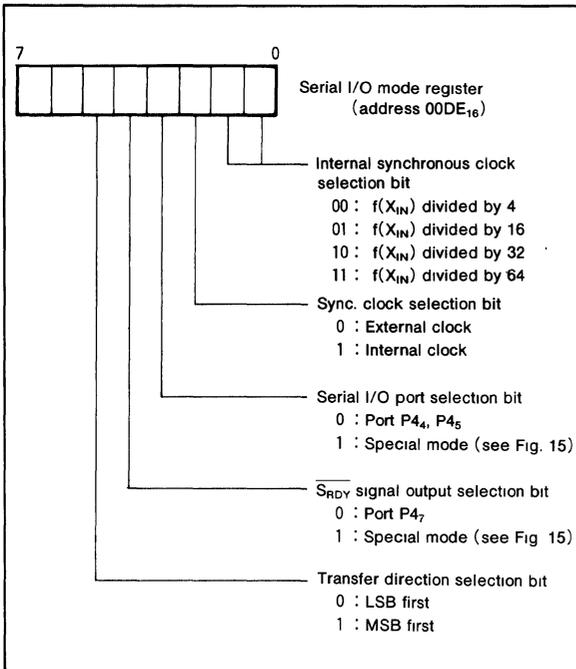


Fig. 11 Structure of serial I/O mode register

SPECIAL MODE (I²C BUS MODE)

M37202M3-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I²C (Inter IC) bus format.

I²C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery.

M37202M3-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O are explained in the following:

(1) Master transmission

To generate an interrupt at the end of transmission, set bit 7 of special mode register 2 (address 00DB₁₆) to "1" so as to special mode serial I/O interrupt is selected. Then set bit 3 of interrupt control register 2 (address 00FF₁₆) to "1" so as to special mode serial I/O interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

The output signals of master transmission SDA and SCL are output from ports P₄ and P₅. Set all bits (bits 4 and 5) corresponding to P₄ and P₅ of the port P4 register (address 00C8₁₆) and the port P4 direction register (address 00C9₁₆) to "1".

Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4. (For instance, if $f(X_{IN})/16$ is selected as the clock source of timer 4 and 4 is set in timer 4 when $f(X_{IN})$ is 4MHz, the master transmission clock frequency is 25kHz.)

Set contents of the special mode register 2 (address 00DB₁₆). (Usually, "83₁₆".)

Set the bit 3 of serial I/O mode register (address 00DE₁₆). After that set the special mode register 1 (address 00DA₁₆). Figure 15 shows the structure of special mode registers 1 and 2.

Initial setting is completed by the above procedure.

Write data to be transmitted in the special serial I/O register (address 00D9₁₆). Immediately after this, clear bits 0 and 1 of special mode register 2 (to "0") to make both SDA and SCL output to "L". This is for arbitration. The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK receiving and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 3 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

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To terminate data transfer, clear bits 0 and 1 of the special mode register 2 to "0", set bit 1 clock SCL to "1", then set bit 1 data SDA to "1". This procedure transmits the stop signal.

Figure 13 shows master transmission timing explained above.

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission.

In the interrupt routine, set master reception ACK provided

(26₁₆) in the special mode register 1 (address 00DA₁₆), and write "FF₁₆" in the special serial I/O register (address 00D9₁₆). This sets data line SDA to "H" and to perform 8-clock master reception. Then, "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission.

Figure 14 shows master reception timing.

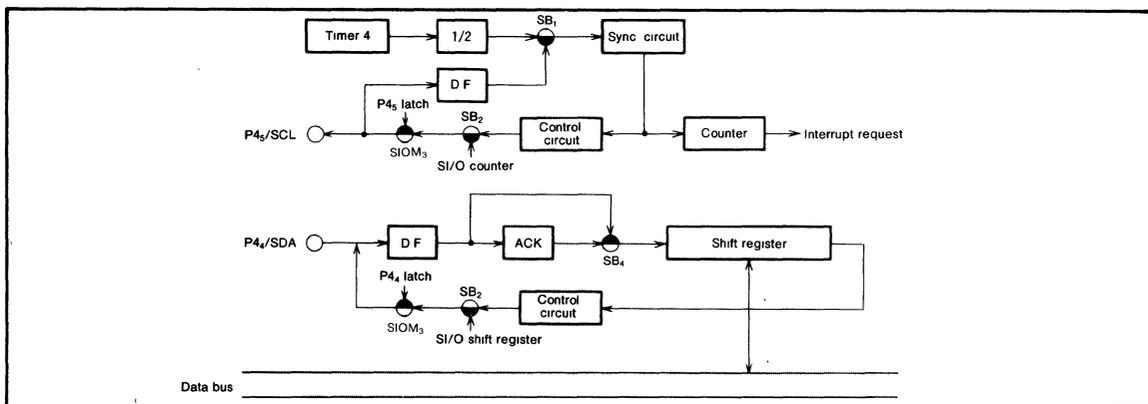


Fig. 12 Block diagram of special serial I/O

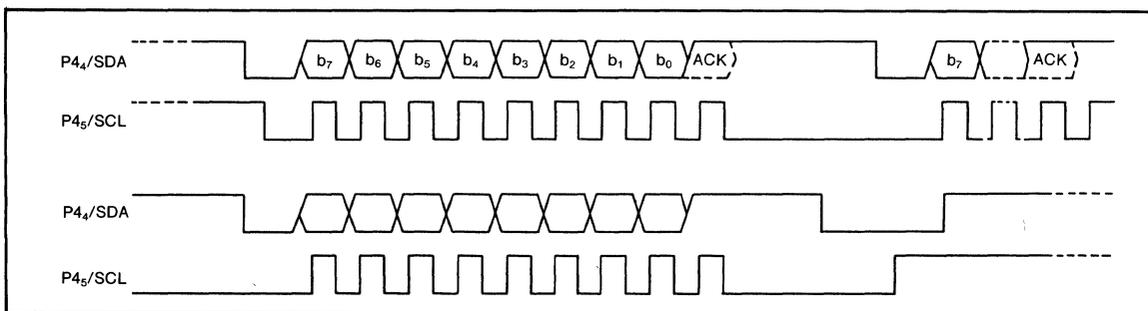


Fig. 13 • Master transmission timing

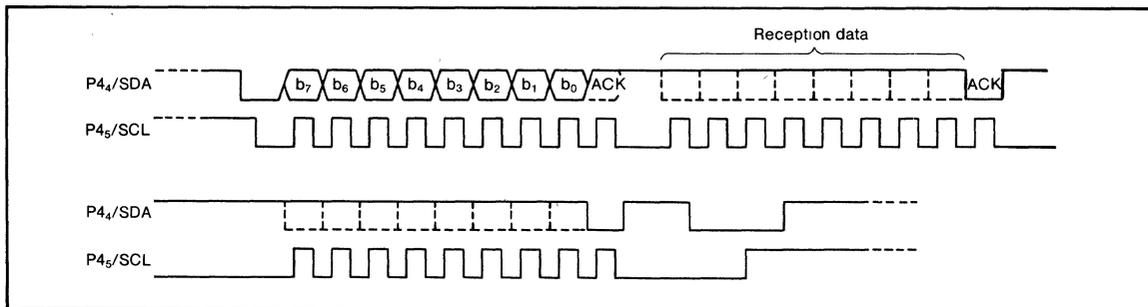


Fig. 14 Master reception timing

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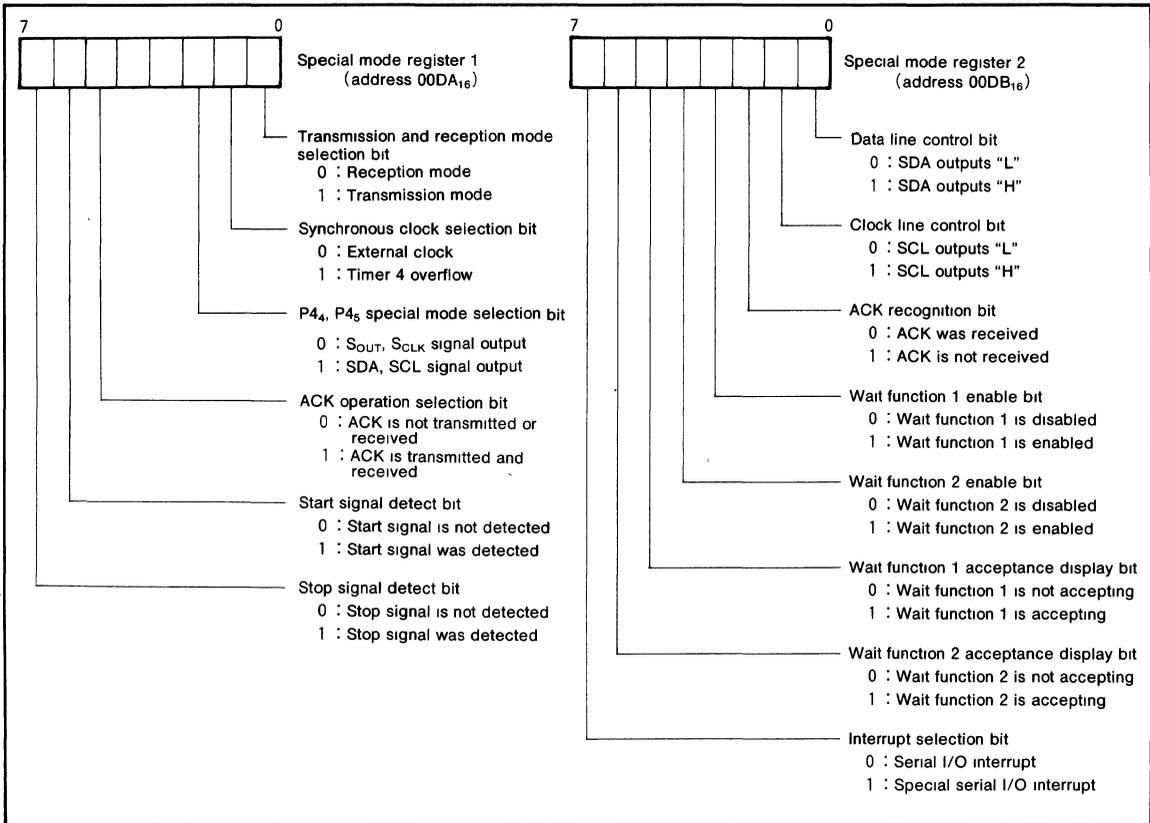


Fig. 15 Structure of special mode registers 1 and 2

(3) Wait functions

Wait function 1 holds the SCL line at "L" after the 8th clock falls in special mode. Wait function 2 holds the SCL line at "L" after the 9th clock falls in the same way.

When one of the wait functions operates, the internal counter that counts the clock must be reset after bit 3 or 4 of the special mode register 2 is set to "1", to enable the corresponding wait function 1 or 2 to operate. Reset the internal counter by writing data to the special serial I/O register (address 00D9₁₆), or by setting the START signal detection bit to "1". Reset the internal counter for each byte before data transfer.

The wait functions can be released by setting the corresponding bit 5 or 6 of the special mode register 2 to "1".

Note 1: Clear the START signal detection bit (bit 6) and the STOP signal detection bit (bit 7) of the special mode register 1 by writing "1" to bit 6 or bit 7.

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PWM OUTPUT CIRCUIT

(1) Introduction

The M37202M3-XXXSP is equipped with one 14-bit PWM (DA) and four 8-bit PWMs (PWM0 to PWM3). The 14-bit resolution gives DA the minimum resolution bit width of 500ns (for $X_{IN}=4\text{MHz}$) and a repeat period of 8192 μs . PWM0 to PWM3 have a 8-bit resolution with minimum resolution bit width of 8 μs and repeat period of 2048 μs .

Block diagram of the PWM is shown in Figure 16.

The PWM timing generator section applies individual control signals to DA and PWM0 to 3 using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM0 to 3 are in common with port P6.

For PWM output, each PWM output selection bit (bit 2 to 5 of PWM output control register 1) should be set. When DA is used for output, first set the higher 8-bit of the DA-H register (address 00CE₁₆), then the lower 6-bit of the DA-L register (address 00CF₁₆).

When one of the PWM0 to 3 is used for output, set the 8-bit in the PWM0 to 3 register (address 00D0₁₆ to 00D3₁₆), respectively.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data in each PWM register is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. However, bit 7 of the DA-L register indicated the completion of the data transfer from the DA register to the DA latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 8-bit PWMs

The timing diagram of the four 8-bit PWMs (PWM0 to 3) is shown in Figure 17. One period (T) is composed of 256 (2⁸) segments.

There are eight different pulse types configured from bits 0 to 7 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 17 (a).

Eight different pulses can be output from the PWM. These can be selected by bits 0 through 7. Depending on the content of the 8-bit PWM latch, pulses from 7 to 0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 17 (b). Changes in the contents of the PWM latch allows the selection of 256 lengths of high-level area outputs varying from 0/256 to 255/256. An length of entirely high-level output cannot be output, i.e. 256/256.

(5) 14-bit PWM operation

The output example of the 14-bit PWM is shown in Figure 19. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length D_H times τ is output every short area of $t=256 \tau=128\mu\text{s}$ as determined by data D_H of the higher 8 bits.

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ . As a result, the short-area period t (= 128 μs , approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 low-order bits of data and high-level area increase space

6 low-order bits of data	Area longer by τ than that of other t_m ($m=0$ to 63)
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m=32$
0 0 0 0 1 0	$m=16, 48$
0 0 0 1 0 0	$m=8, 24, 40, 56$
0 0 1 0 0 0	$m=4, 12, 20, 28, 36, 42, 50, 58$
0 1 0 0 0 0	$m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m=1, 3, 5, 7, \dots, 57, 59, 61, 63$

MITSUBISHI MICROCOMPUTERS
M37202M3-XXXSP

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
 with ON-SCREEN DISPLAY CONTROLLER**

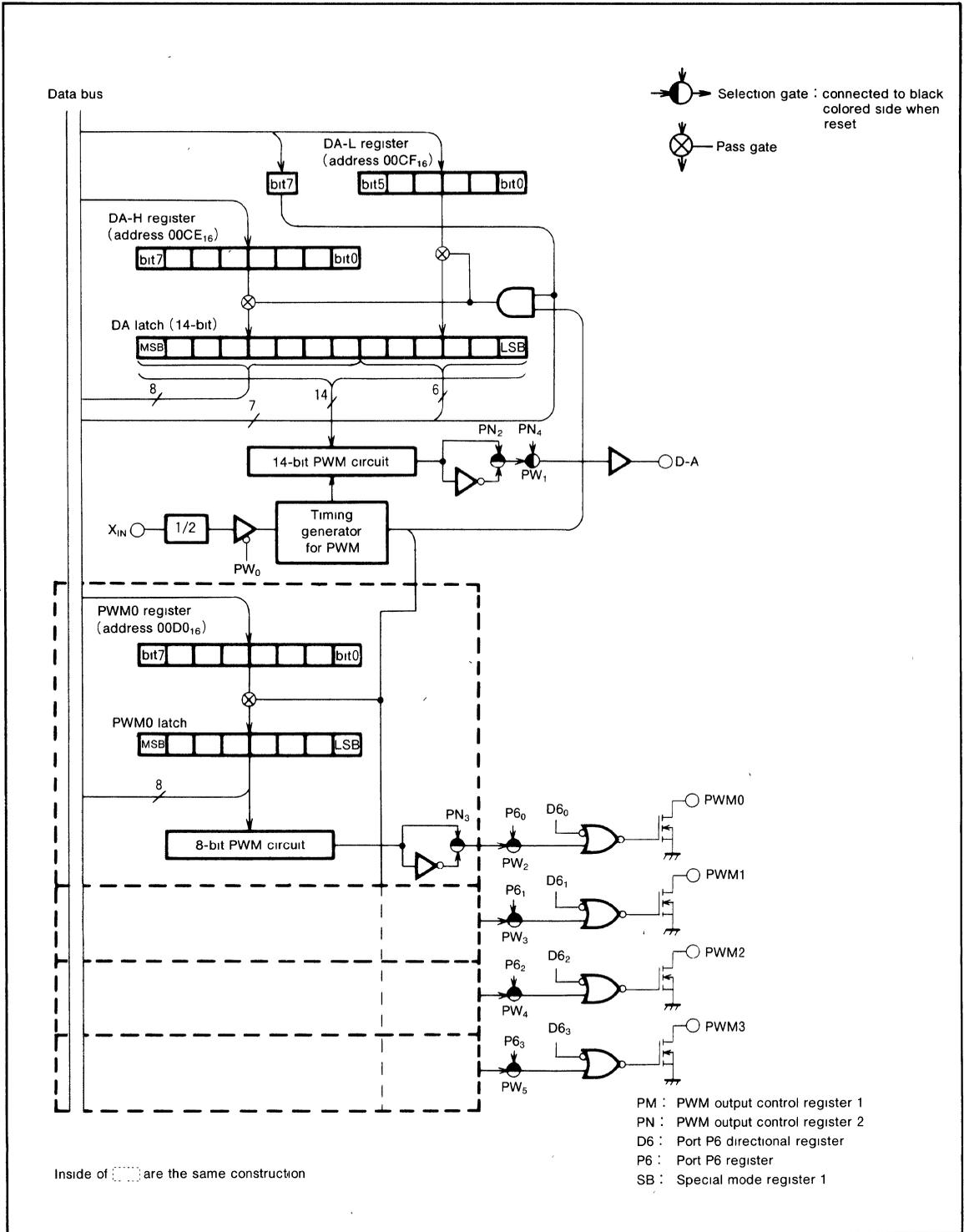


Fig. 16 Block diagram of the PWM circuit

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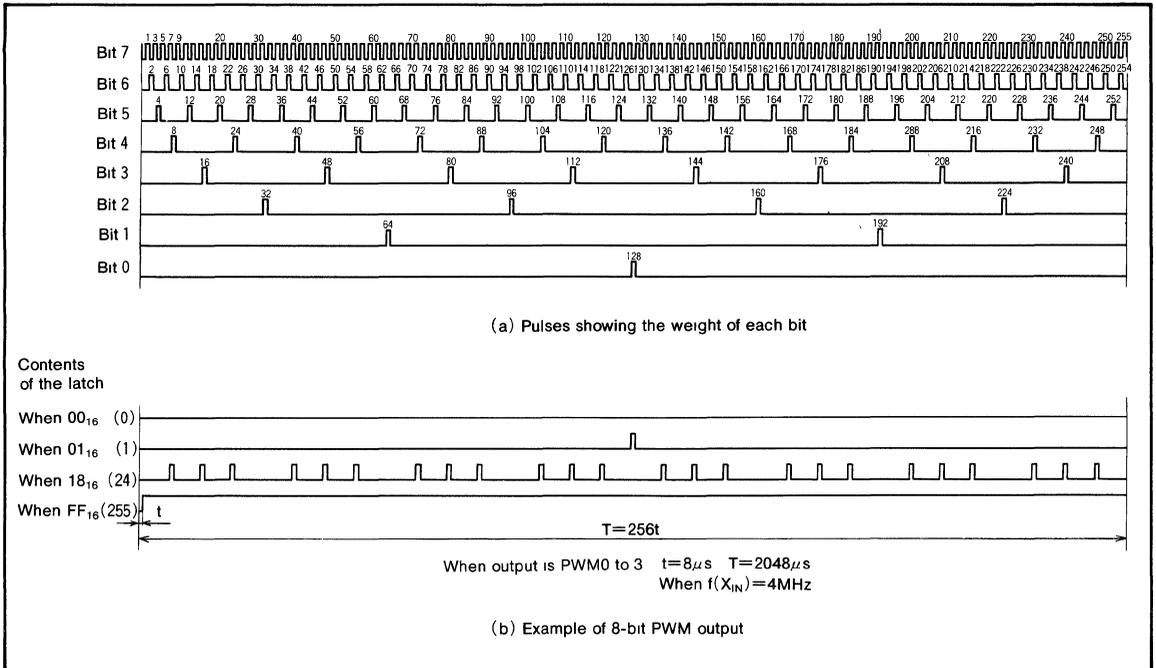


Fig. 17 8-bit PWM timing diagram

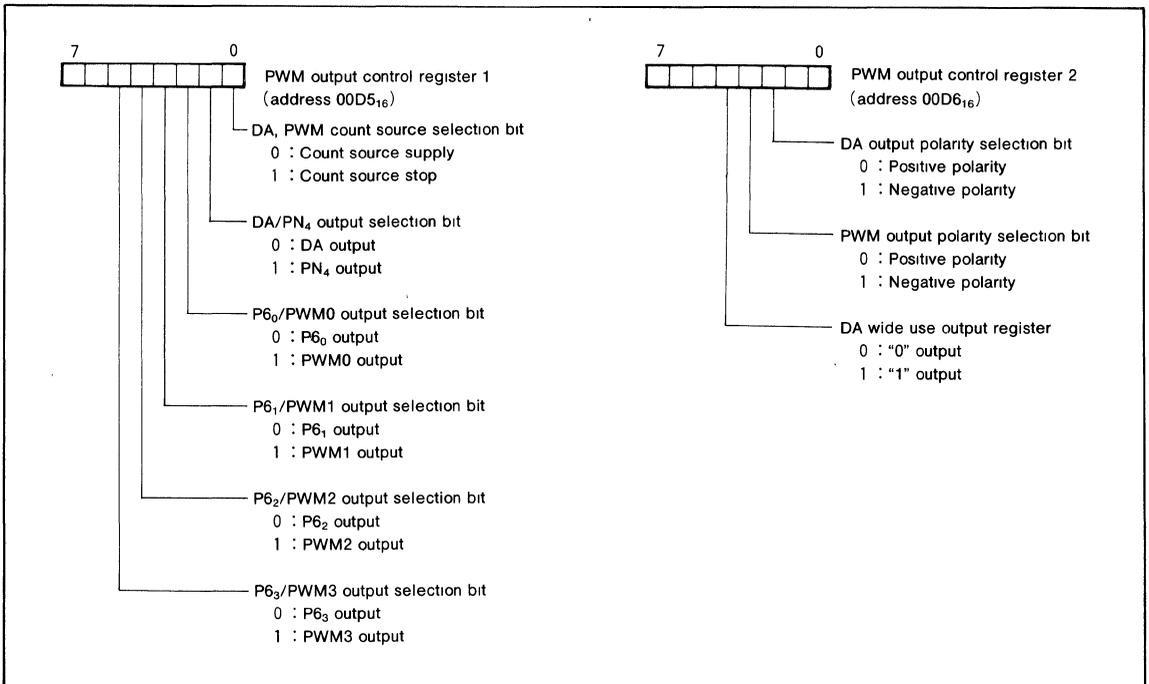


Fig. 18 Structure of PWM output control register 1 and 2

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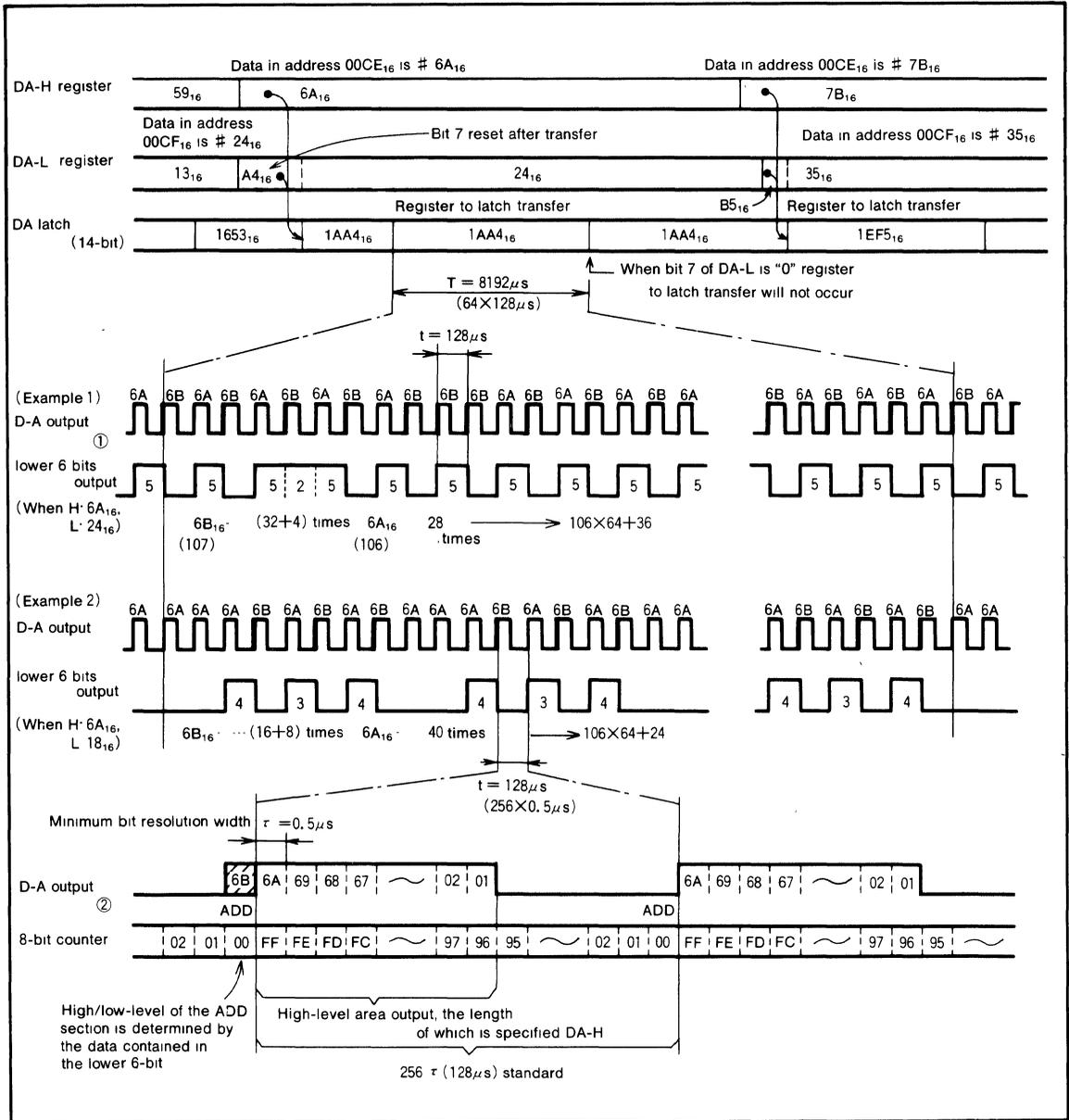


Fig. 19 14-bit PWM timing diagram

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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A-D CONVERTER

Block diagram of A-D converter is shown in Figure 20. A-D converter consists of 4-bit D-A converter and comparator. The A-D control register can generate 1/16 V_{CC} -step internal analog voltage based on the settings of bits 0 to 3. Table 3 gives the relation between the descriptions of A-D control register bits 0 to 3 and the generated internal analog voltage. The comparison result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 4.

The data is compared by setting the direction register corresponding to port P3₅, P3₆, P6₄ and P6₅ to "0" (port P3₅, P3₆, P6₄ and P6₅ enters the input mode), to allow port P3₅/A-D1, P3₆/A-D2, P6₄/A-D3 and P6₅/A-D4 to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register, bit 0 to 3 and an analog input pin is selected. After 20 machine cycle, the voltage comparison starts.

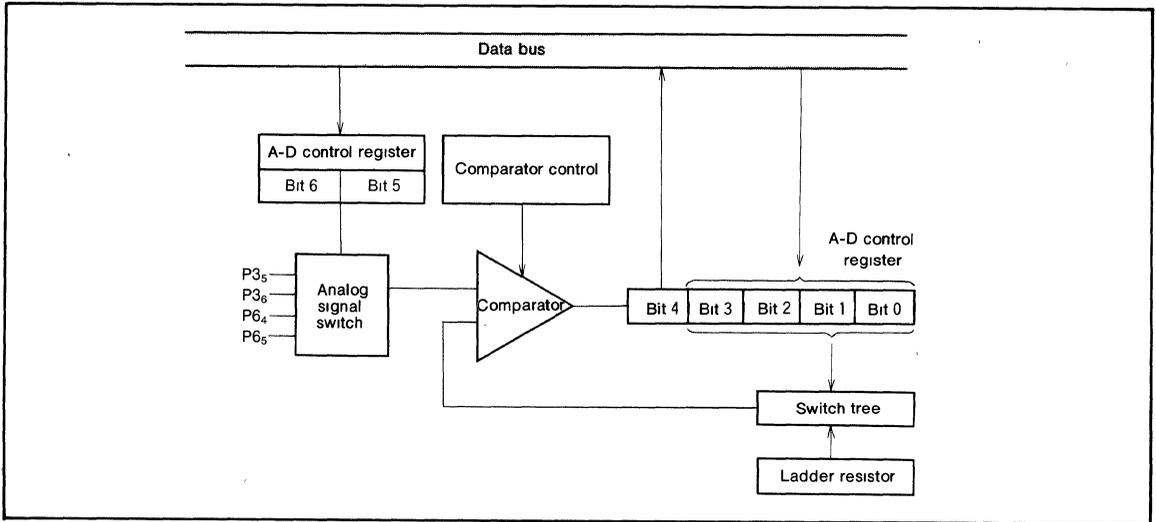


Fig. 20 Block diagram of A-D converter

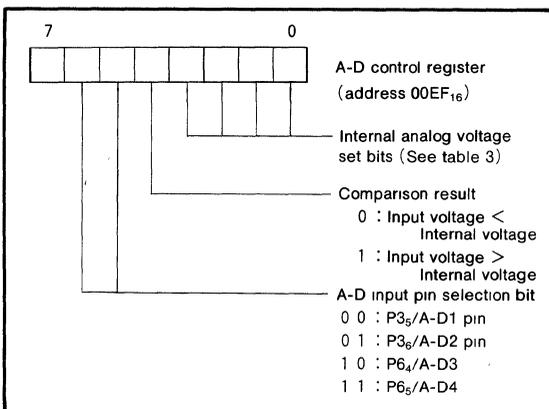


Fig. 21 Structure of A-D control register

Table 3. Relationship between the contents of A-D control register and internal analog voltage

A-D control register				Internal analog voltage
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	1/32 V_{CC}
0	0	0	1	3/32 V_{CC}
0	0	1	0	5/32 V_{CC}
0	0	1	1	7/32 V_{CC}
0	1	0	0	9/32 V_{CC}
0	1	0	1	11/32 V_{CC}
0	1	1	0	13/32 V_{CC}
0	1	1	1	15/32 V_{CC}
1	0	0	0	17/32 V_{CC}
1	0	0	1	19/32 V_{CC}
1	0	1	0	21/32 V_{CC}
1	0	1	1	23/32 V_{CC}
1	1	0	0	25/32 V_{CC}
1	1	0	1	27/32 V_{CC}
1	1	1	0	29/32 V_{CC}
1	1	1	1	31/32 V_{CC}

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CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 4 outlines the CRT display functions of the M37202M3-XXXSP. The M37202M3-XXXSP incorporates a 24 columns×3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 94 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12×16 dot configuration to obtain smooth character patterns. (See Figure 22)

The following shows the procedure how to display characters on the CRT screen.

Table 4. Outline of CRT display functions

Parameter		Functions
Number of display character		24 characters×3 lines
Character configuration		12×16 dots (See Figure 22)
Kinds of character		94
Character size		4 size selectable
Color	Kinds of color	15 (max)
	Coloring unit	a character
Display expansion		Possible (multiple lines)

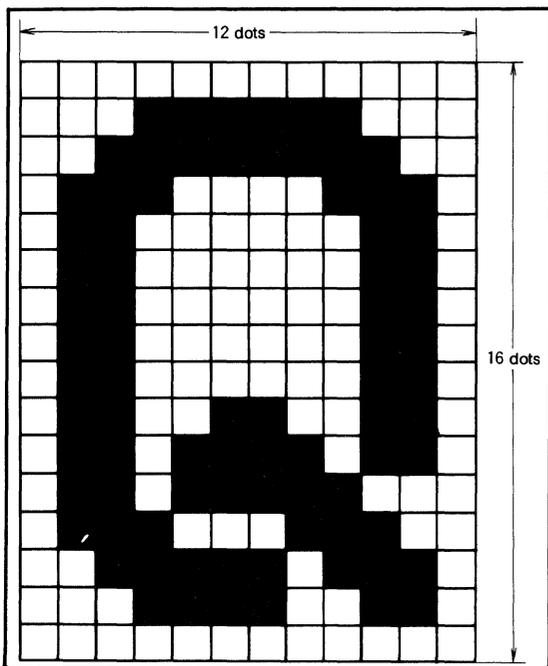


Fig. 22 CRT display character configuration

- ① Set the character to be displayed in display RAM.
- ② Set the display color by using the color register.
- ③ Specify the color register in which the display color is set by using the display RAM.
- ④ Specify the vertical position and character size by using the vertical position register and the character size register.
- ⑤ Specify the horizontal position by using the horizontal position register.
- ⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 23 shows the structure of the CRT display control register. Figure 24 shows a block diagram of the CRT display control circuit.

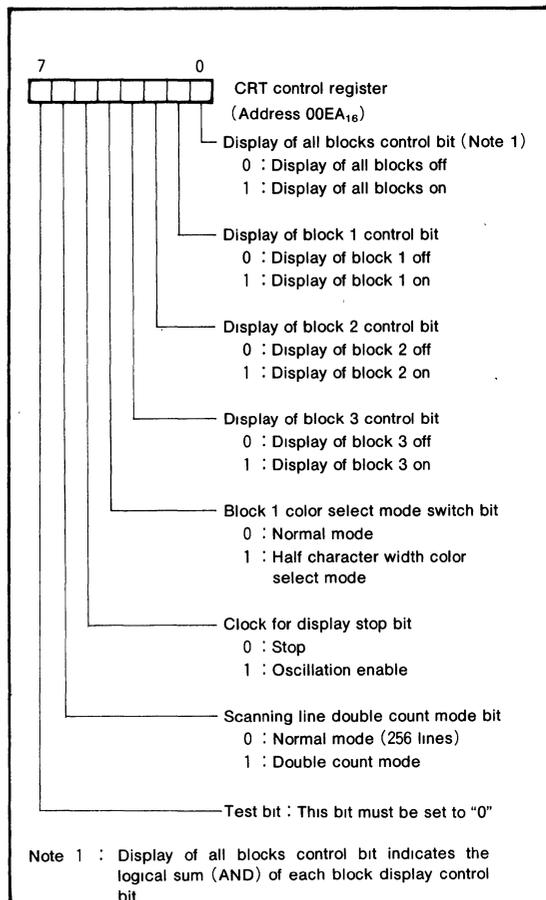


Fig. 23 Structure of CRT control register

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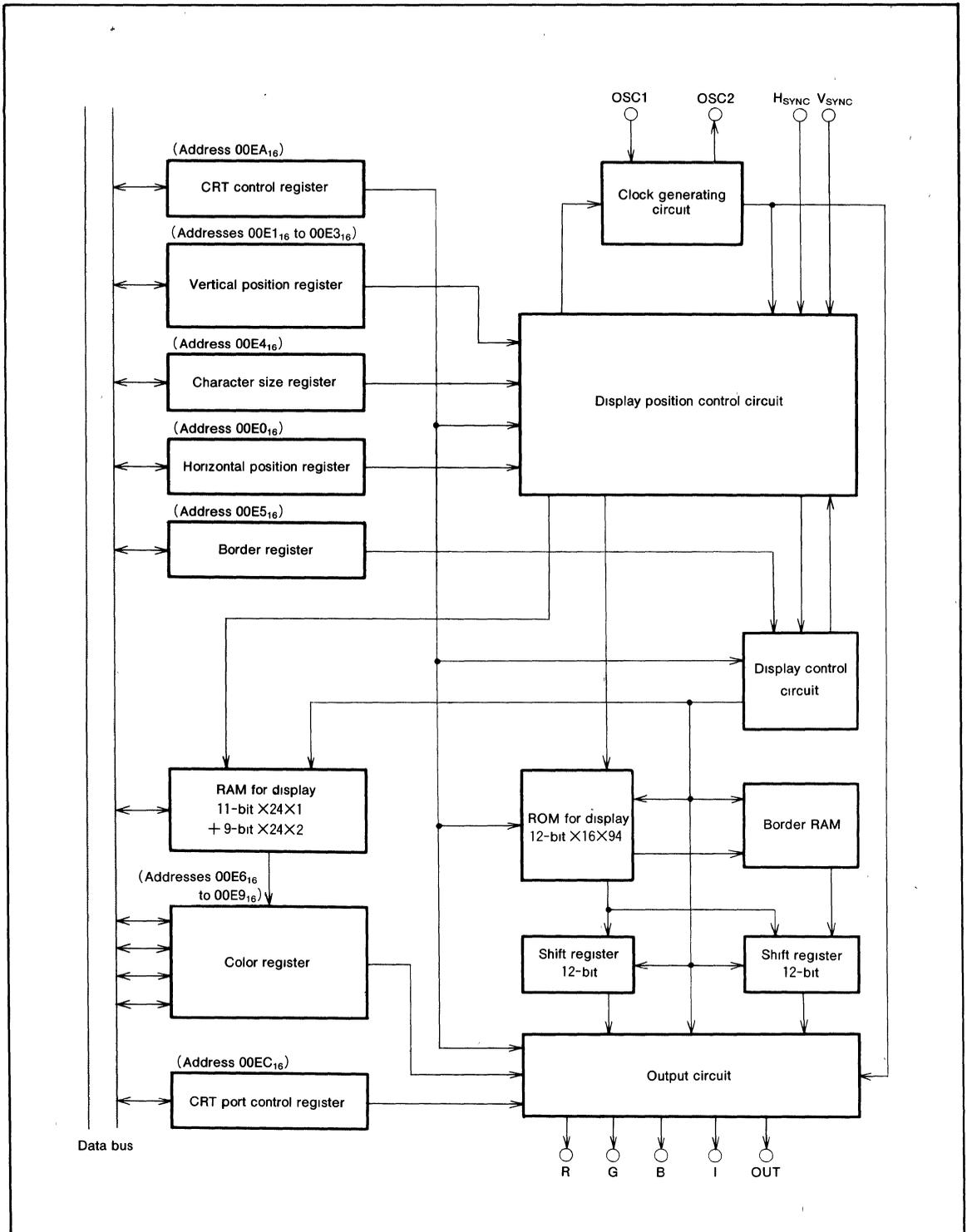


Fig. 24 Block diagram of CRT display control circuit

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(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 24 characters can be displayed in one block. (See (4) Display Memory.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of $4T_c$ (T_c = oscillation cycle for display).

The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 27), a block of the smaller block No. (1~3) is displayed.

If one block has displayed, some other block is later displayed at the same display position ((c) in Figure 27), the former block is overridden and the latter is displayed.

The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values $00_{16} \sim 7F_{16}$ to bits 0~6 in the vertical position register (addresses $00E1_{16} \sim 00E3_{16}$). Figure 25 shows the structure of the vertical position register.

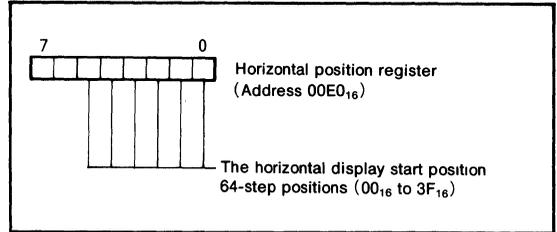


Fig. 26 Structure of horizontal position register

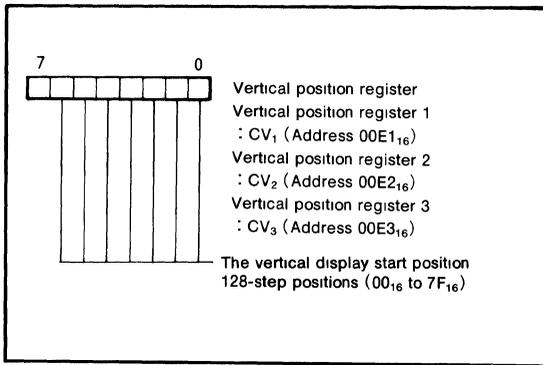
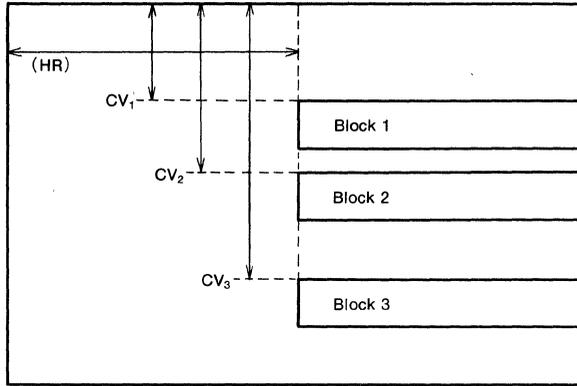


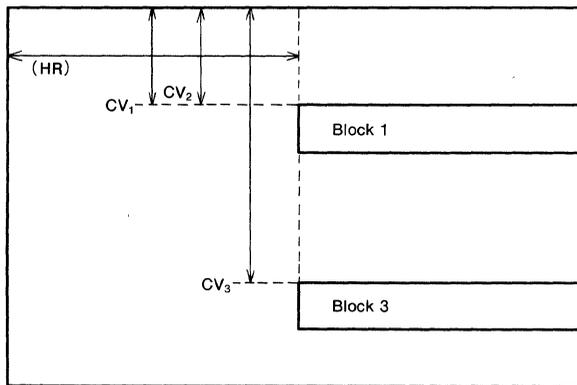
Fig. 25 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64-step display positions ($4T_c$ per step (T_c = oscillation cycle for display)) by setting values $00_{16} \sim 3F_{16}$ to bits 0~5 in the horizontal position register (address $00E0_{16}$). Figure 26 shows the structure of the horizontal position register.

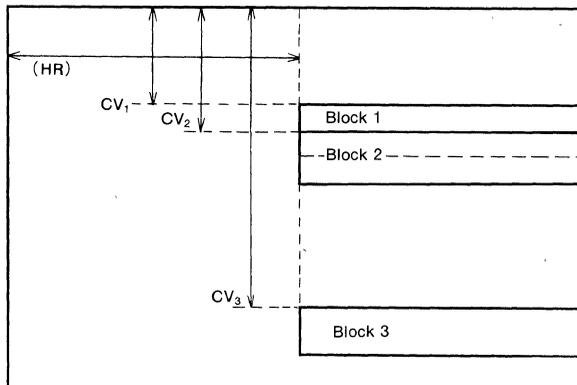
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(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block has displayed some other block is superimposed later

Fig. 27 Display position

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(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the character size register (address 00E4₁₆) to set a character size. The character size in block 1 can be specified by using bits 0 and 1 in the character size register; the character size in block 2 can be specified by using bits 2 and 3; the character size in block 3 can be specified by using bits 4 and 5. Figure 28 shows the structure of the character size register.

The character size can be selected from four sizes: small size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation (=T_c) in the width (horizontal) direction. The small size consists of [one scanning line] × [1 T_c]; the medium size consists of [two scanning lines] × [2 T_c]; the large size consists of [three scanning lines] × [3 T_c]; and the extra large size consists of [four scanning lines] × [4 T_c]. Table 5 shows the relationship between the set values in the character size register and the character sizes.

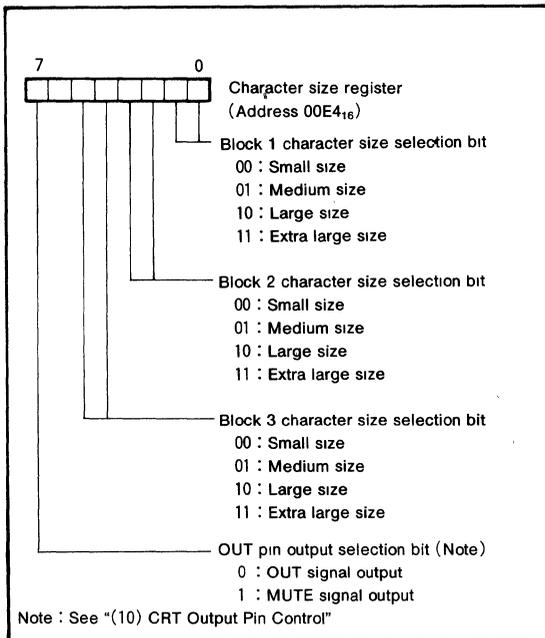


Fig. 28 Structure of character size register

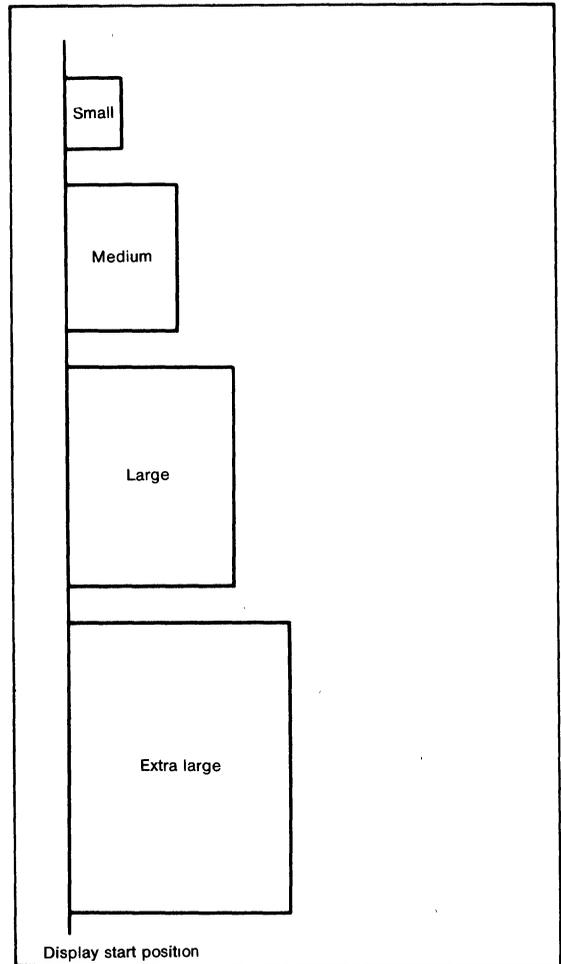


Fig. 29 Display start position of each character size (horizontal direction)

Table 5. The relationship between the set values of the character size register and the character sizes

Set values of the character size register		Character size	Width (horizontal) direction		Height (vertical) direction	
CS _{n1}	CS _{n0}		T _c : A cycle of display oscillation		(Scanning lines)	
0	0	Small	1 T _c		1	
0	1	Medium	2 T _c		2	
1	0	Large	3 T _c		3	
1	1	Extra large	4 T _c		4	

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal start position is common to all blocks even when the character size varies with each block (See Figure 29)

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(4) Display Memory

There are two types of display memory: CRT display ROM (addresses 3000₁₆ to 35DF₁₆, 37E0₁₆ to 3DDF₁₆, and 3FE0₁₆ to 3FFF₁₆) used to store character dot data (masked) and display RAM (addresses 2000₁₆ to 20D7₁₆) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① ROM for CRT display (addresses 3000₁₆ to 35DF₁₆, 37E0₁₆ to 3DDF₁₆, and 3FE0₁₆ to 3FFF₁₆)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM.

The CRT display ROM has a capacity of 3K bytes. Because 32 bytes are required for one character data, the ROM can contain up to 96 kinds of characters. Actually, however, because two characters are required for test pattern use, the ROM can contain up to 94 kinds of characters for display use.

The CRT display ROM space is broadly divided into two areas. The [vertical 16 dots] X [horizontal (left side) 8 dots] data of display characters are stored in addresses 3000₁₆ to 35DF₁₆ and 37E0₁₆ to 37FF₁₆; the [vertical 16 dots] X [horizontal (right side) 4 dots] data of display characters are stored in addresses 3800₁₆ to 3DDF₁₆ and 3FE0₁₆ to 3FFF₁₆. (See Figure 30) Note however that the four upper bits in the data to be written to addresses 3800₁₆ to 3DDF₁₆ and 3FE0₁₆ to 3FFF₁₆ must be set to "1" (by writing data F0₁₆ to FF₁₆).

The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.

Assume that data for one character is stored at addresses 3XX0₁₆ to 3XXF₁₆ (XX denotes 00₁₆ to 5D₁₆, 7E₁₆, or 7F₁₆) and 3YY0₁₆ to 3YYF₁₆ (YY denotes 80₁₆ to DD₁₆, FE₁₆, or FF₁₆), then the character code for it is "XX₁₆".

In other words, character code for any given character is configured with two middle digits of the four-digit (hexnotated) addresses (3000₁₆ to 35DF₁₆ and 37E0₁₆ to 37FF₁₆) where data for that character is stored.

Table 6 lists the character codes

Table 6. Character code list

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00 ₁₆	3000 ₁₆ to 300F ₁₆	3800 ₁₆ to 380F ₁₆
01 ₁₆	3010 ₁₆ to 301F ₁₆	3810 ₁₆ to 381F ₁₆
02 ₁₆	3020 ₁₆ to 302F ₁₆	3820 ₁₆ to 382F ₁₆
03 ₁₆	3030 ₁₆ to 303F ₁₆	3830 ₁₆ to 383F ₁₆
:	:	:
10 ₁₆	3100 ₁₆ to 310F ₁₆	3900 ₁₆ to 390F ₁₆
11 ₁₆	3110 ₁₆ to 311F ₁₆	3910 ₁₆ to 391F ₁₆
:	:	:
5C ₁₆	35C0 ₁₆ to 35CF ₁₆	3DC0 ₁₆ to 3DCF ₁₆
5D ₁₆	35D0 ₁₆ to 35DF ₁₆	3DD0 ₁₆ to 3DDF ₁₆
7E ₁₆ *	37E0 ₁₆ to 37EF ₁₆	3FE0 ₁₆ to 3FEF ₁₆
7F ₁₆ *	37F0 ₁₆ to 37FF ₁₆	3FF0 ₁₆ to 3FFF ₁₆

* : For test pattern

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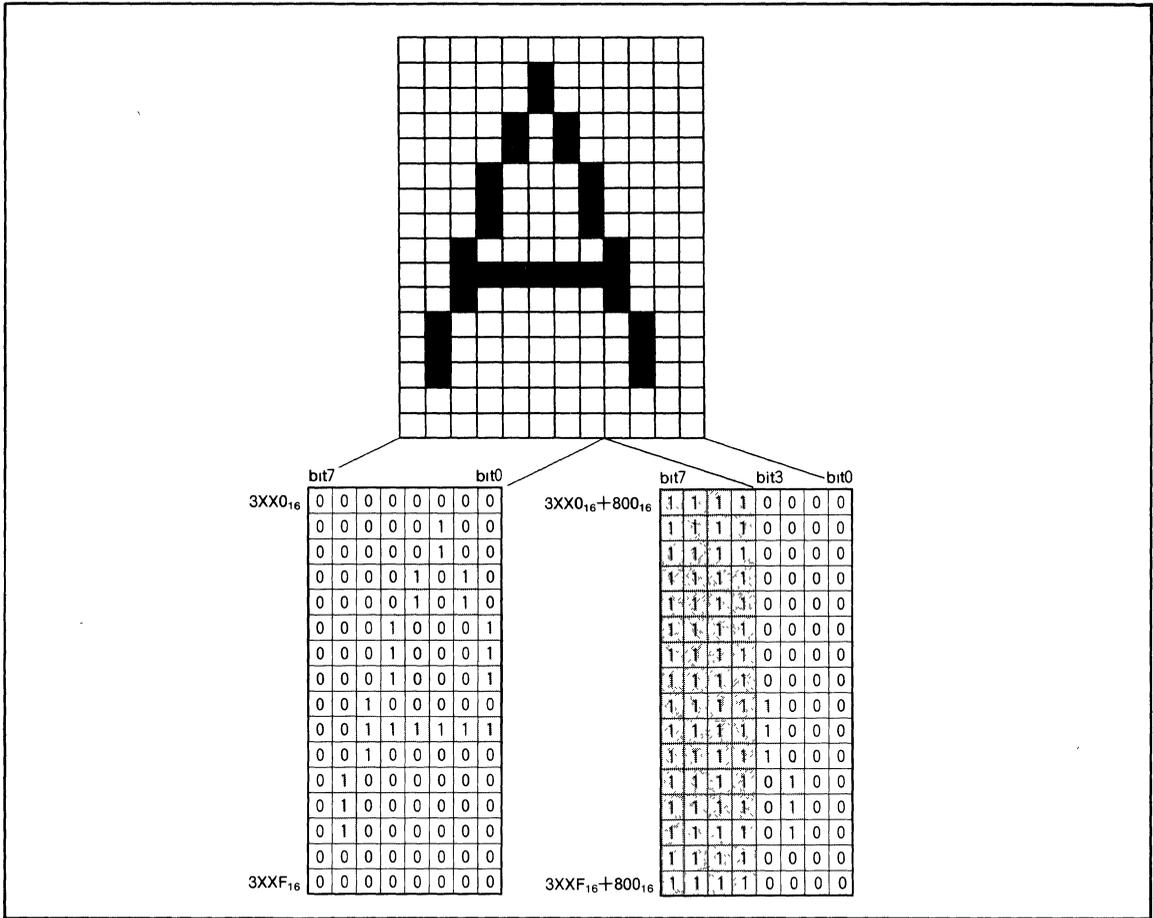


Fig. 30 Display character stored area

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② CRT display RAM (2000₁₆ to 20D7₁₆)

The CRT display RAM is allocated at addresses 2000₁₆ to 20D7₁₆, and is divided into a display character code specifying part and display color specifying part for each block. Table 7 shows the contents of the CRT display RAM.

When a character is to be displayed at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0 to 6) in address 2000₁₆ and the color register No. to the two low-order bits (bits 0 and 1) in address 2080₁₆. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 31. Write the character patterns at Table 8 and 9, when M37202M3-XXXSP is mask-ordered.

Table 7. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st column	2000 ₁₆	2080 ₁₆
	2nd column	2001 ₁₆	2081 ₁₆
	3rd column	2002 ₁₆	2082 ₁₆
	:	:	:
	22th column	2015 ₁₆	2095 ₁₆
	23th column	2016 ₁₆	2096 ₁₆
	24th column	2017 ₁₆	2097 ₁₆
Not used		2018 ₁₆ to 201F ₁₆	2098 ₁₆ to 209F ₁₆
Block 2	1st column	2020 ₁₆	20A0 ₁₆
	2nd column	2021 ₁₆	20A1 ₁₆
	3rd column	2022 ₁₆	20A2 ₁₆
	:	:	:
	22th column	2035 ₁₆	20B5 ₁₆
	23th column	2036 ₁₆	20B6 ₁₆
	24th column	2037 ₁₆	20B7 ₁₆
Not used		2038 ₁₆ to 203F ₁₆	20B8 ₁₆ to 20BF ₁₆
Block 3	1st column	2040 ₁₆	20C0 ₁₆
	2nd column	2041 ₁₆	20C1 ₁₆
	3rd column	2042 ₁₆	20C2 ₁₆
	:	:	:
	22th column	2055 ₁₆	20D5 ₁₆
	23th column	2056 ₁₆	20D6 ₁₆
	24th column	2057 ₁₆	20D7 ₁₆
Not used		2058 ₁₆ to 207F ₁₆	

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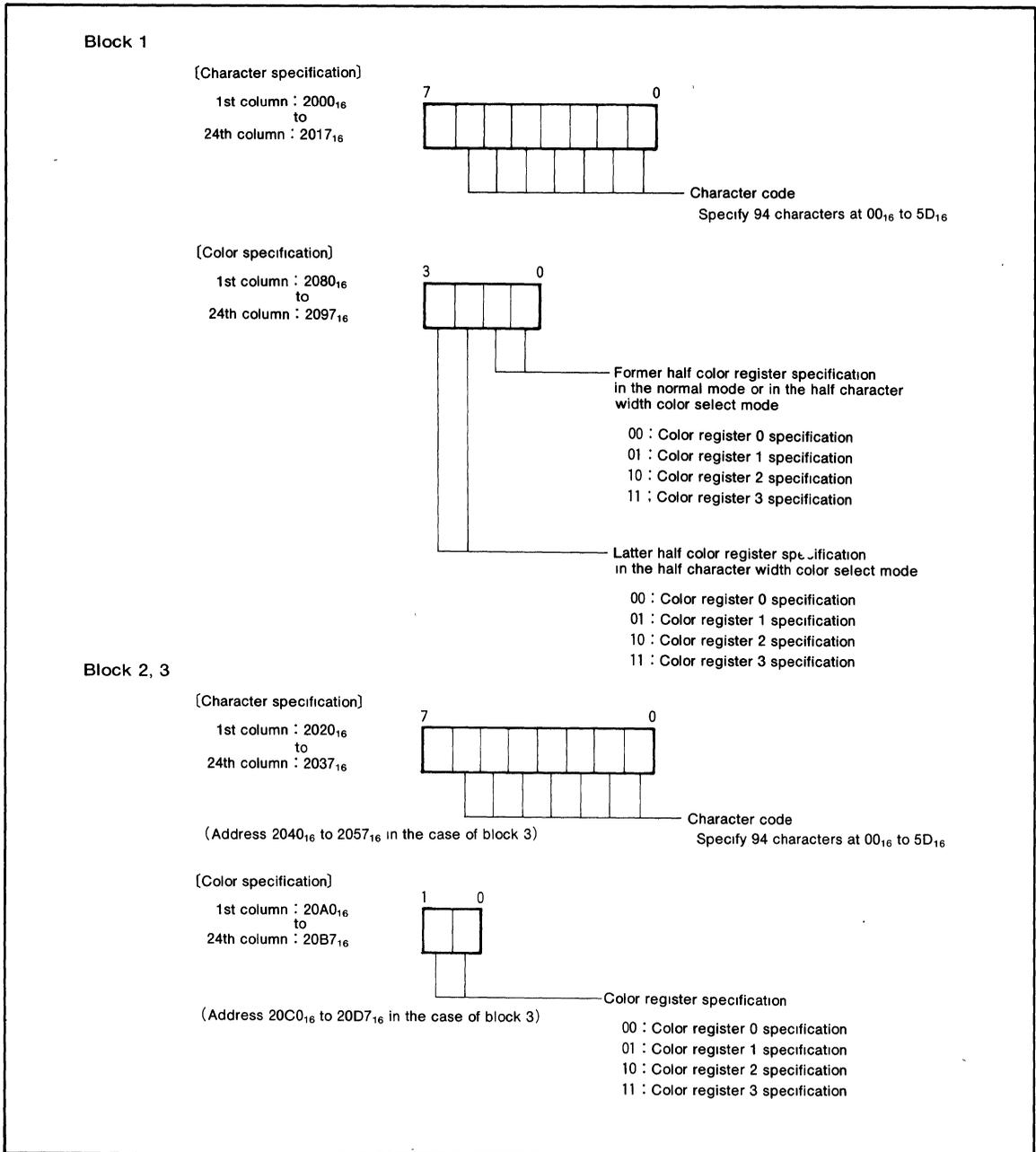


Fig. 31 Structure of the CRT display RAM

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Table 8. Test character patterns 1

Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

Table 9. Test character patterns 2

Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3: addresses 00E6₁₆ to 00E9₁₆) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set 2⁴-1 (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 32 shows the structure of the color register.

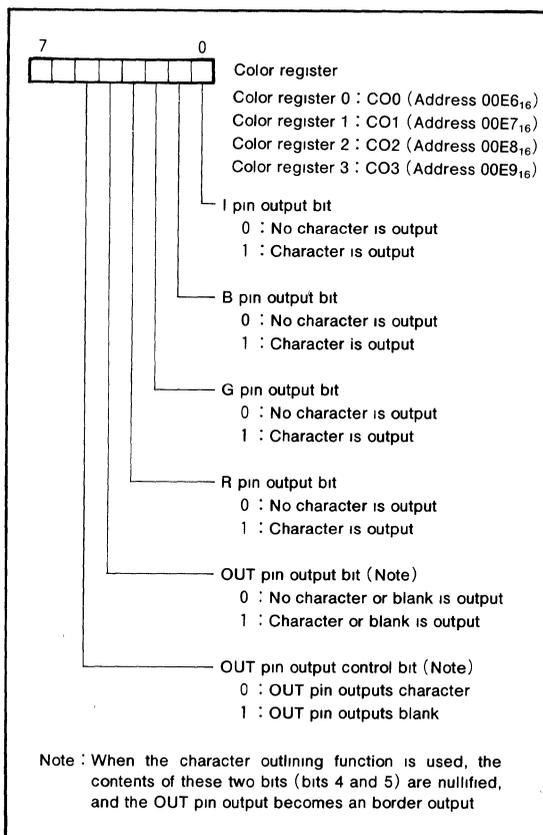


Fig. 32 Structure of color registers

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address 00EA₁₆) it is possible to specify colors in units of a half character size (vertical 16 dots×horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

- ① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080₁₆ to 2097₁₆).
- ② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080₁₆ to 2097₁₆).

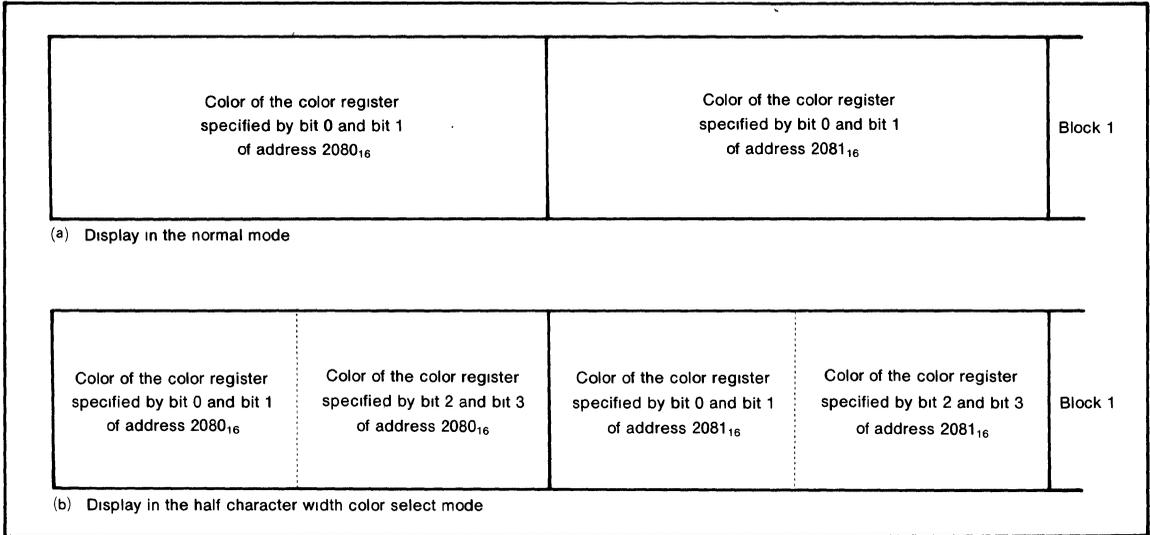


Fig. 33 Difference between normal color select mode and half character width color select mode

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(7) Multiline Display

The M37202M3-XXXSP can normally display three lines on the CRT screen by displaying three blocks at different horizontal positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit=bit 4 at address 00FE₁₆) to "1", then execute the following processing in the CRT interrupt handling routine.

- ① Read the value of the display block counter.
- ② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.
- ③ Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and display position (contents of vertical position and horizontal position registers) to be displayed next.

Figure 34 shows the structure of the display block counter.

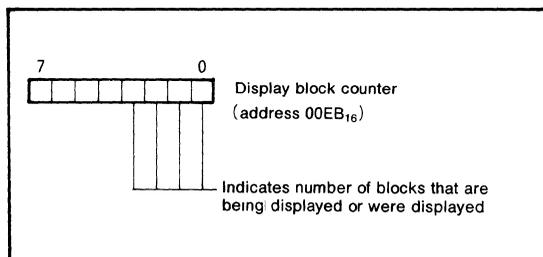


Fig. 34 Structure of display block counter

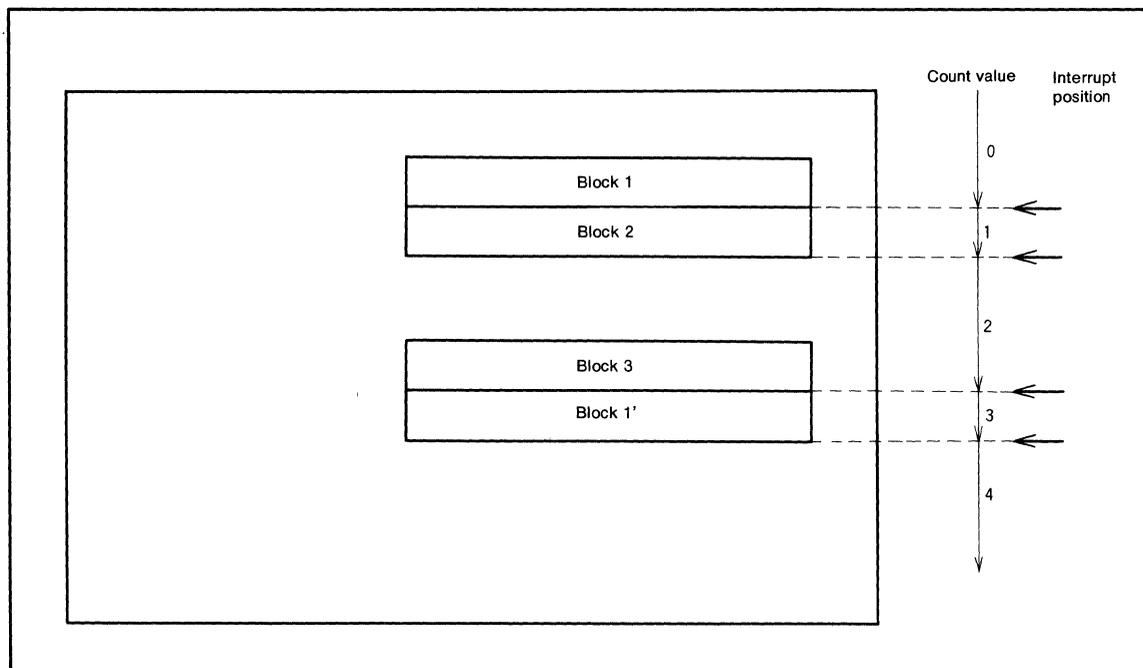


Fig. 35 Timing of CRT interrupt and count value of display block counter

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(8) Scanning Line Double Count Mode

One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended twofold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 128 steps from 00_{16} to $7F_{16}$, or four scanning lines per step, the number of steps in the scanning line double count mode is 64 from 00_{16} to $3F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 40_{16} to $7F_{16}$ in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register (address $00EA_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.

In the scanning line double count mode, the character border function (explain in (9)) cannot be used.

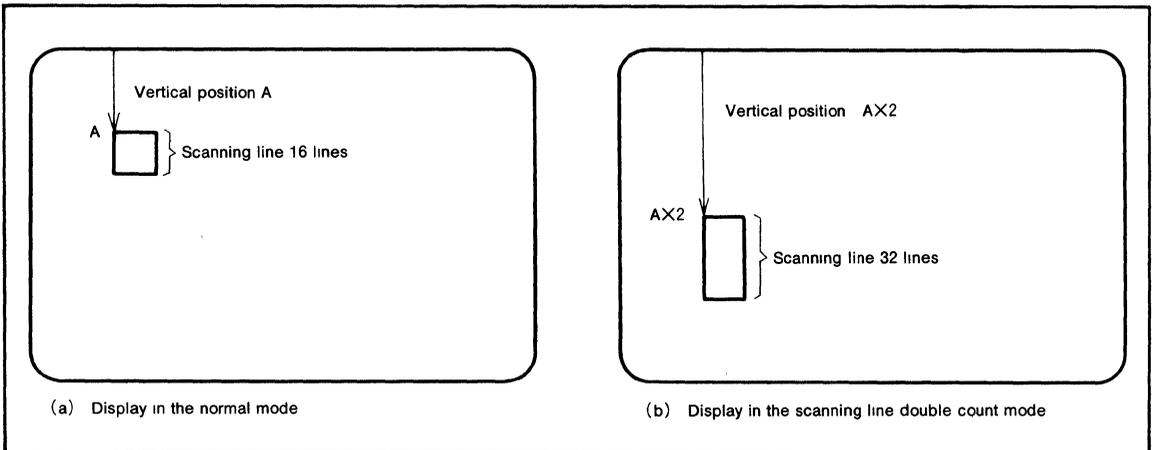


Fig. 36 Display in the normal mode and in the scanning line double count mode

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(9) Character Border Function

An border of a one clock (one dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions. However, the border is not displayed over the 1st line and under the 16th line.

The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (contents output from the OUT pin) are nullified, and the border is output from the OUT pin instead.

Border can be specified in units of block by using the border select register (address 00E5₁₆). Table 10 shows the relationship between the values set in the border select register and the character border function. Figure 38 shows the structure of the border select register.

Table 10. The relationship between the value set in the border selection register and the character border function

Border selection register		Functions	Example of output
MDn1	MDn0		
X	0	Normal	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border not including character	R, G, B, I output OUT output

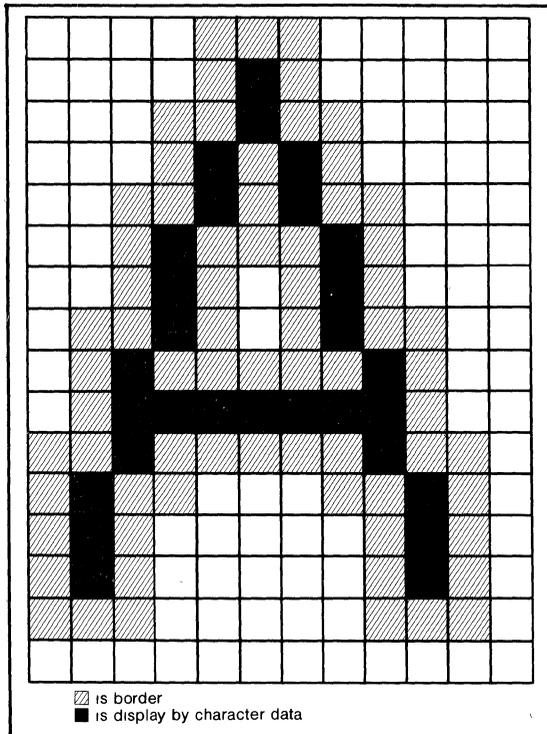


Fig. 37 Example of border

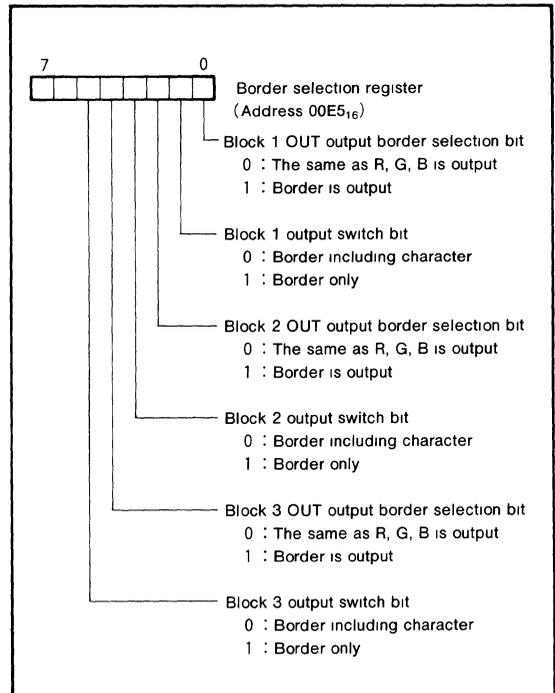


Fig. 38 Structure of border selection register

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(10) CRT Output Pin Control

CRT output pins R, G, B, I, and OUT are respectively shared with port P5₂, P5₃, P5₄, P5₅, and P5₆. When the corresponding bits in the port P5 direction register are cleared to "0", the pins are set for CRT output; when the bits are set to "1", the pins function as port P5 (general-purpose output pins).

The polarities of CRT outputs (R, G, B, I, and OUT, as well as H_{SYNC} and V_{SYNC}) can be specified by using the CRT port control register (address 00EC₁₆).

Use bits 0 to 4 in the CRT port control register to set the output polarities of H_{SYNC}, V_{SYNC}, R/G/B, I, and OUT. When these bits are cleared to "0", a positive polarity is selected; when the bits are set to "1", a negative polarity is selected. R, G, B, and OUT signal output can be switched to MUTE signal output. MUTE signal can color all displaying area of CRT.

The following is the explain of MUTE signal at MUTE signal output from B output pin for example (refer to Figure 40).

When the MUTE signal is output from B output pin, the all displaying area of CRT is colored blue. Then, a character data is output from R output pin, for example. If B output pin and R output pin are set to "Character is output" by color register at the character "I" output, the output character is colored "RED" mixed "BLUE". In this case, OUT pin output is not influenced.

At the character "O" output, if only R output pin is set to "Character is output", the output character is colored "RED" only that is not mixed "BLUE".

However at above case, the OUT output pin is necessary to set "Character is output".

The display screen can be also clear by setting the OUT pin to MUTE output. In this case, the MUTE signal is output from OUT pin, that is not influence the setting about OUT pin.

R, G, and B output signals are controlled by bits 5 to 7 of CRT port control register, and OUT output signal is controlled by bit 7 (CS₇) of character size register. Then, I output pin don't have MUTE output function.

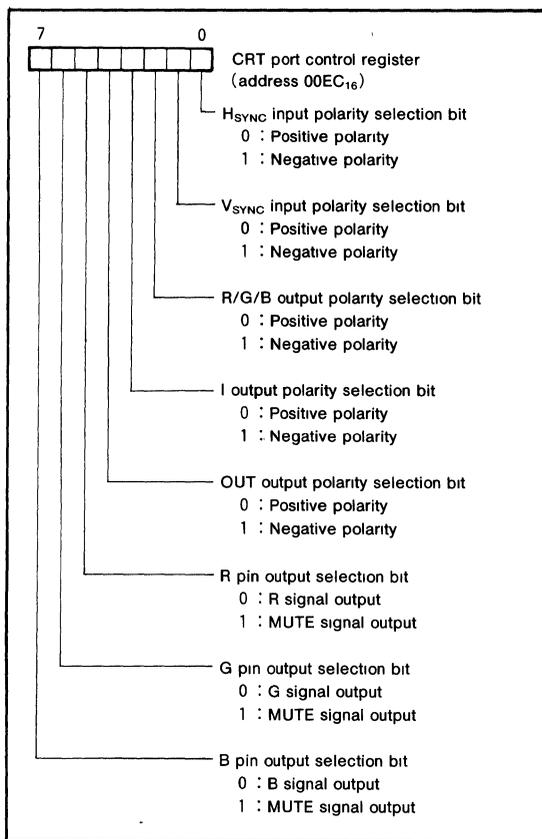


Fig. 39 Structure of CRT port control register

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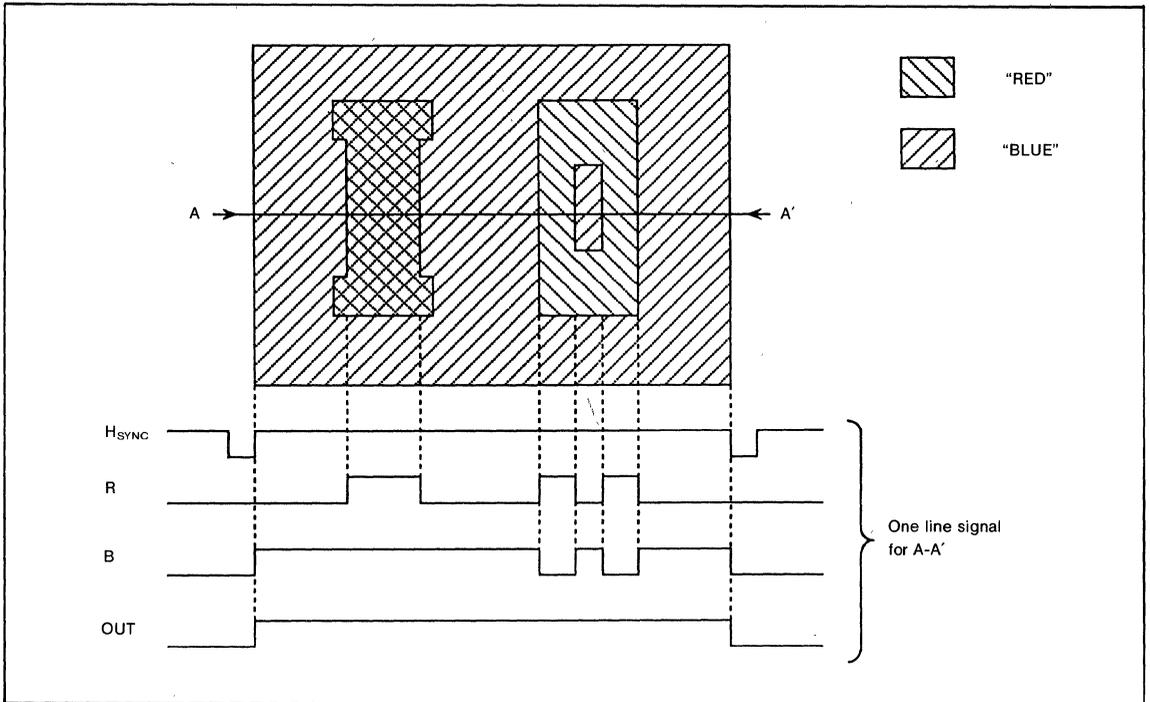


Fig. 40 MUTE signal output example

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**INTERRUPT INTERVAL DETERMINATION
FUNCTION**

The M37202M3-XXXSP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary counter as shown in Figure 41. Using this counter, it determines a duration of time from the rising transition (falling transition) of an input signal pulse on the INT1 or INT2 to the rising transition (falling transition) of the signal pulse that is input next.

The following describes how the interrupt interval is determined.

1. The interrupt input to be determined (INT1 input or INT2 input) is selected by using bit 2 in the interrupt interval determination control register (address 00D8₁₆). When this bit is cleared to "0", the INT1 input is selected; when the bit is set to "1", the INT2 input is selected.
2. When the INT1 input is to be determined, the polarity is selected by using bit 3 in the interrupt interval determination control register; when the INT2 input is to be determined, the polarity is selected by using bit 4 in the interrupt interval determination control register. When the relevant bit is cleared to "0", determination is made of the interval of a positive polarity (rising

transition); when the bit is set to "1", determination is made of the interval of a negative polarity (falling transition).

3. The reference clock is selected by using bit 1 in the interrupt interval determination control register. When the bit is cleared to "0", a 64 μ s clock is selected; when the bit is set to "1", a 32 μ s clock is selected (based on an oscillation frequency of 4MHz in either case).
4. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT1 pin (or INT2 pin), the 8-bit binary counter starts counting up with the selected reference clock (64 μ s or 32 μ s).
5. Simultaneously with the next input pulse, the value of the 8-bit binary counter is loaded into the determination register (address 00D7₁₆) and the counter is immediately reset (00₁₆). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "00₁₆".
6. When count value "FE₁₆" is reached, the 8-bit binary counter stops counting. Then, simultaneously when the reference clock is input next, the counter sets value "FF₁₆" to the determination register.

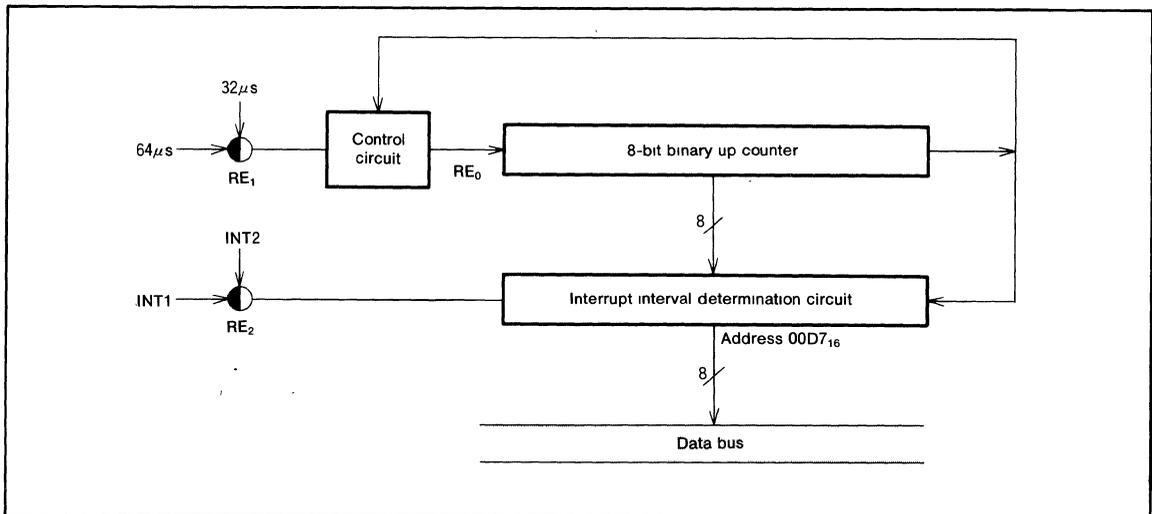


Fig. 41 Block diagram of interrupt interval determination circuit

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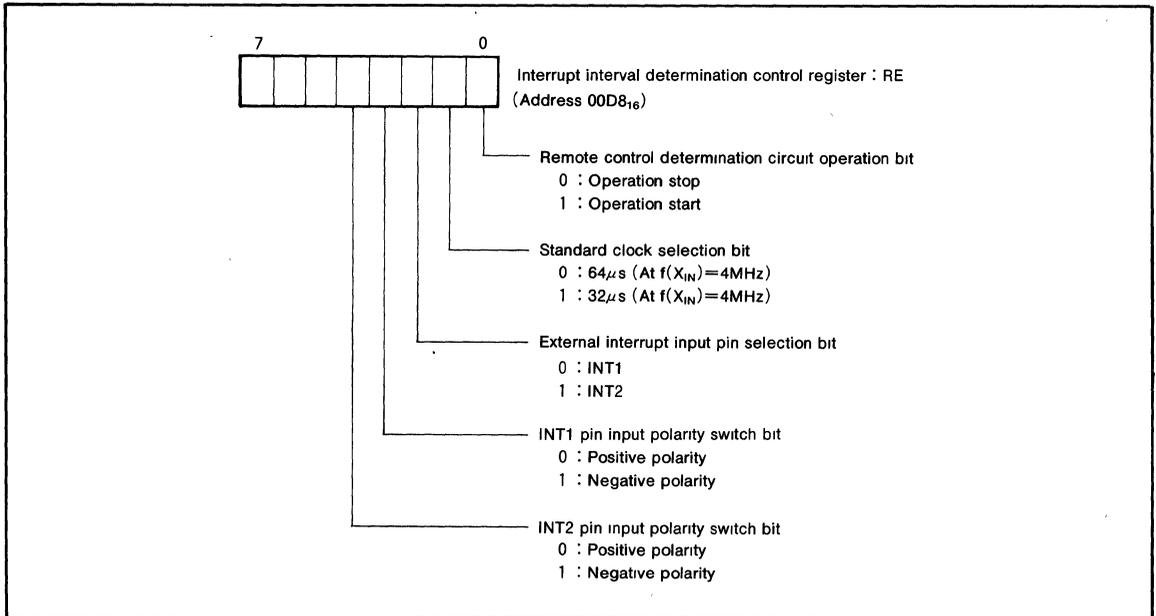


Fig. 42 Structure of interrupt interval determination control register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

RESET CIRCUIT

The M37202M3-XXXSP is reset according to the sequence shown in Figure 45. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than $2\mu\text{s}$ while the power voltage is $5V \pm 10\%$

and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 43.

An example of the reset circuit is shown in Figure 44. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

	Address	
(1) Port P0 direction register	(00C1) ₁₆	00 ₁₆
(2) Port P1 direction register	(00C3) ₁₆	00 ₁₆
(3) Port P2 direction register	(00C5) ₁₆	00 ₁₆
(4) Port P3 direction register	(00C7) ₁₆	00000000
(5) Port P4 direction register	(00C9) ₁₆	00 ₁₆
(6) Port P5 direction register	(00CB) ₁₆	00000000
(7) Port P6 direction register	(00CD) ₁₆	00 ₁₆
(8) PWM output control register 1	(00D5) ₁₆	00000000
(9) PWM output control register 2	(00D6) ₁₆	0000
(10) Interrupt interval determination control register	(00D8) ₁₆	00000000
(11) Special mode register 1	(00DA) ₁₆	00000000
(12) Special mode register 2	(00DB) ₁₆	00 ₁₆
(13) Serial I/O mode register	(00DE) ₁₆	00000000
(14) Horizontal position register	(00E0) ₁₆	00000000
(15) Character size register	(00E4) ₁₆	0
(16) Color register 0	(00E6) ₁₆	00000000
(17) Color register 1	(00E7) ₁₆	00000000
(18) Color register 2	(00E8) ₁₆	00000000
(19) Color register 3	(00E9) ₁₆	00000000
(20) CRT control register	(00EA) ₁₆	00 ₁₆
(21) Display block counter	(00EB) ₁₆	0000
(22) CRT port control register	(00EC) ₁₆	00 ₁₆
(23) A-D control register	(00EF) ₁₆	00000000
(24) Timer 1	(00F0) ₁₆	FF ₁₆
(25) Timer 2	(00F1) ₁₆	07 ₁₆
(26) Timer 3	(00F2) ₁₆	FF ₁₆
(27) Timer 4	(00F3) ₁₆	07 ₁₆
(28) Timer 12 mode register	(00F4) ₁₆	00000000
(29) Timer 34 mode register	(00F5) ₁₆	00000000
(30) CPU mode register	(00FB) ₁₆	11111110
(31) Interrupt request register 1	(00FC) ₁₆	00000000
(32) Interrupt request register 2	(00FD) ₁₆	000000
(33) Interrupt control register 1	(00FE) ₁₆	00000000
(34) Interrupt control register 2	(00FF) ₁₆	000000
(35) Processor status register (PS)		1
(36) Program counter (PC _H)		Contents of address $FFFF_{16}$
(36) Program counter (PC _L)		Contents of address $FFFE_{16}$

Note . Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values
At reset, "0" is read from all bits which is not used

Fig. 43 Internal state of microcomputer at reset

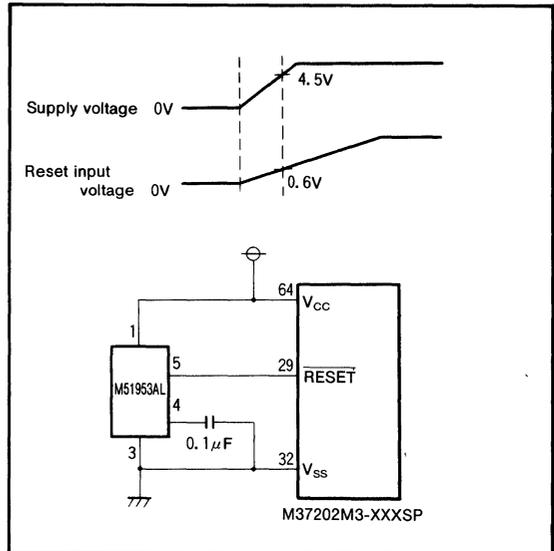


Fig. 44 Example of reset circuit

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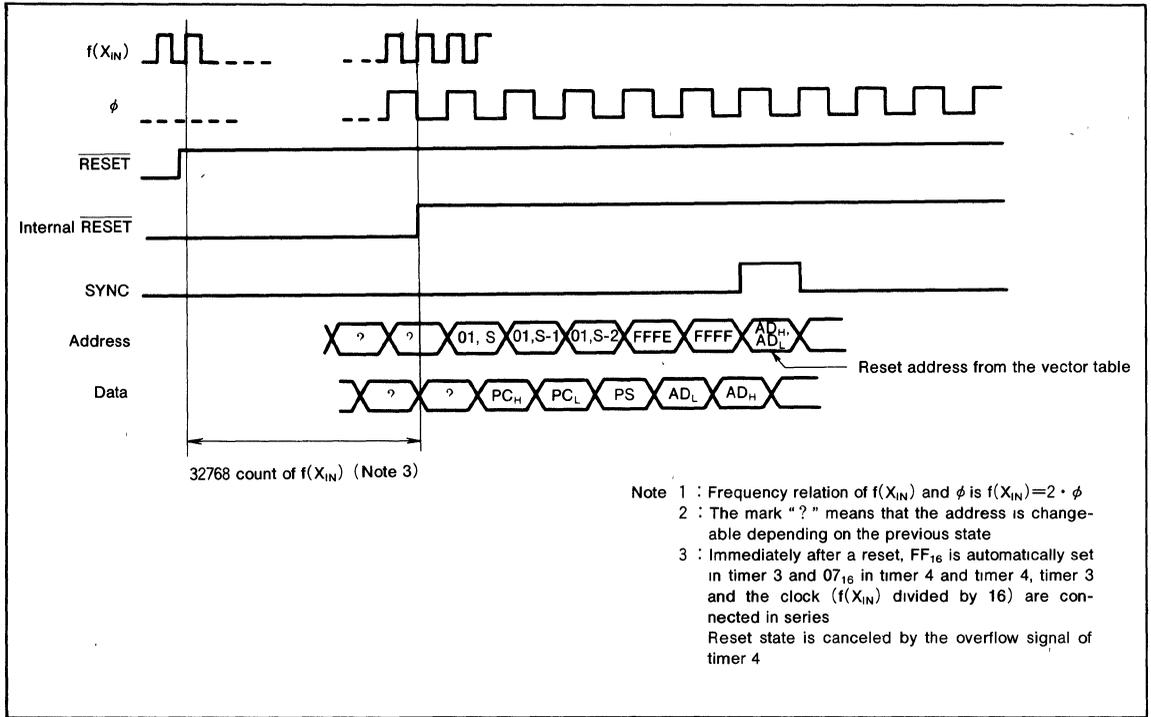


Fig. 45 Timing diagram at reset

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I/O PORTS**(1) Port P0**

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address 00C0₁₆.

Port P0 has a directional register (address 00C1₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address 00FB₁₆), three different modes can be selected; single-chip mode, memory expansion mode and microprocessor mode.

In these modes it functions as address (A₇ to A₀) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A₁₅ to A₈) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data (D₀ to D₇) input/output port. Refer to the section on processor modes for details.

(4) Port P3

Port P3 is an 7-bit I/O port with function similar to port P0, but the output structure of P3₀, P3₁ is CMOS output and P3₂ to P3₆ is N-channel open drain.

P3₂, P3₃ are in common with the external clock input pins of timer 2 and 3.

P3₄, P3₆ are in common with the external interrupt input pins INT1, INT2 and P3₅, P3₆ with the analog input pins of A-D converter A-D1, A-D2.

In the microprocessor mode or the memory expanding mode, P3₀, P3₁ works as R/W signal output pin and SYNC signal output pin.

(5) Port P4

Port P4 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

All pins have program selectable dual functions. When a serial I/O function is selected, P4₄ to P4₇ work as input/output pins of serial I/O.

In the special serial I/O mode, P4₄, P4₅ work as SDA, SCL pins.

(6) OSC1, OSC2 pins

Clock input/output pins for CRT display function.

(7) H_{SYNC}, V_{SYNC} pins

H_{SYNC} is a horizontal synchronizing signal input pin for CRT display.

V_{SYNC} is a vertical synchronizing signal input pin for CRT display.

(8) R, G, B, I, OUT pins

This is an 5-bit output pin for CRT display and in common with P5₂ to P5₆.

(9) Port P6

Port P6 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

P6₀ to P6₃ are in common with 8-bit PWM output pin PWM0 to PWM3.

(10) D-A pin

This is a 14-bit PWM output pin.

(11) ϕ pin

The internal system clock (1/2 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

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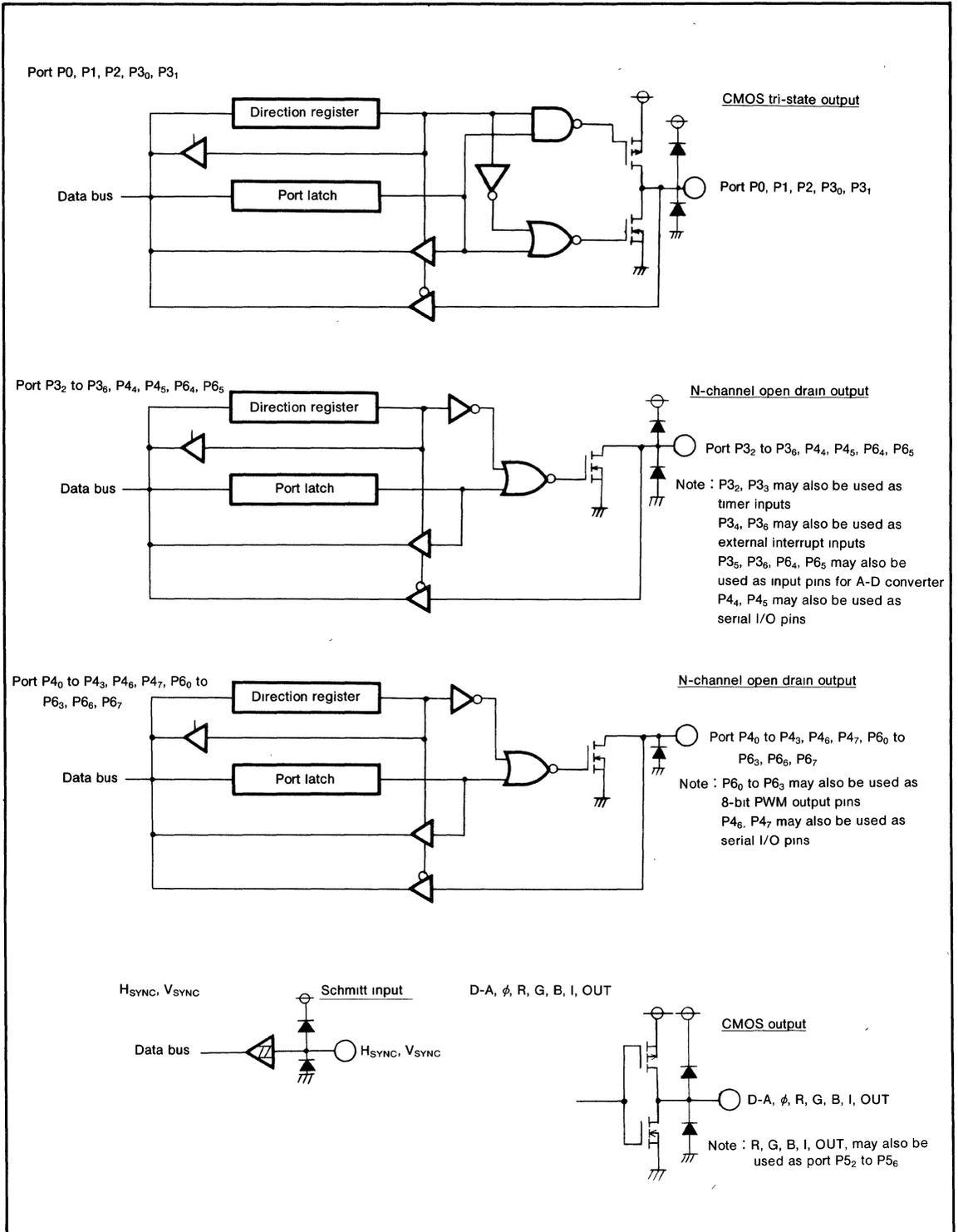


Fig. 46 Block diagram of port P0 to P6, H_{SYNC}, V_{SYNC} (single-chip mode) and output format of D-A, ϕ , R, G, B, I, OUT

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PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address 00FB₁₆), three different operation modes can be selected; single-chip mode, memory expansion mode, and microprocessor mode.

In the memory expansion mode and the microprocessor mode, ports P0 to P3 can be used as address, and data input/output pins.

Figure 48 shows the functions of ports P0~P3.

The memory map for the single-chip mode is shown in Figure 1 and for other modes, in Figure 47.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode.

The three different modes are explained as follows:

- (1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0 to P3 will work as original I/O ports.

- (2) Memory expansion mode [01]

When CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01", the microcomputer will automatically default to this mode. This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost.

Port P2 becomes the data bus of D₇ to D₀ (including instruction code) and loses its normal I/O function. Port P3₀ and P3₁ works as R/W and SYNC.

- (3) Microprocessor mode [10]

The microcomputer will be placed in the microprocessor mode after connecting CNV_{SS} to V_{CC} or initiating a reset or connecting CNV_{SS} to V_{SS} and the processor mode bits are set to "10". In this mode, the internal ROM is inhibited so the external memory is required. Other functions are same as the memory expansion mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 11.

Note : Use the M37202M3-XXXSP in the microprocessor mode or the memory expansion mode only at program development.

The standards is assured only in the single-chip mode.

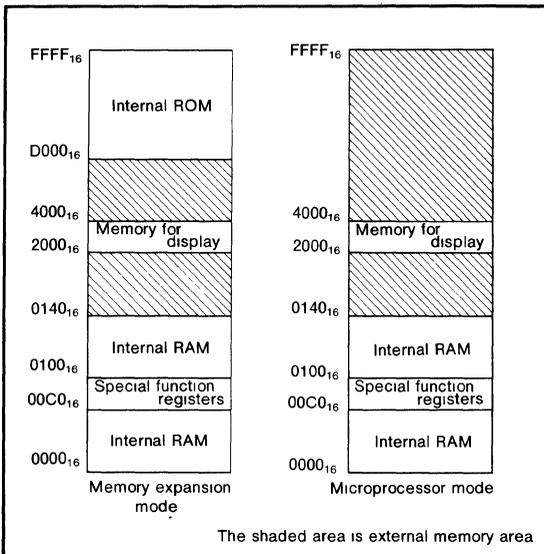


Fig. 47 Example memory area in processor mode

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Port	CM ₁	0	0	1
	CM ₀	0	1	0
	Mode	Single-chip mode	Memory expansion mode	Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P3			Same as left	

Fig. 48 Processor mode and function of ports P0 to P3

Table 11. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode • Memory expansion mode • Microprocessor mode 	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V _{CC}	<ul style="list-style-type: none"> • Microprocessor mode 	The microprocessor mode is set by the reset

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CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 51.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timer 3 and timer 4 are connected automatically and FF_{16} is set in the timer 3, 07_{16} is set in the timer 4, and timer 3 count source is forced to $f(X_{IN})$ divided by 16. This connection is cleared when an external interrupt is accepted or the reset is in, as discussed in the timer section

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 49.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 50. X_{IN} is the input, and X_{OUT} is open.

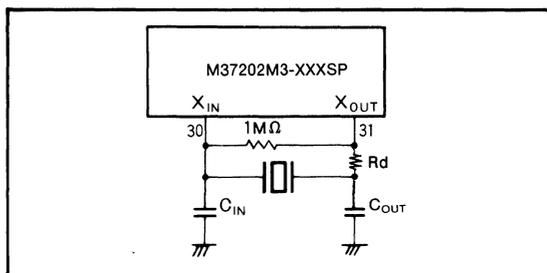


Fig. 49 External ceramic resonator circuit

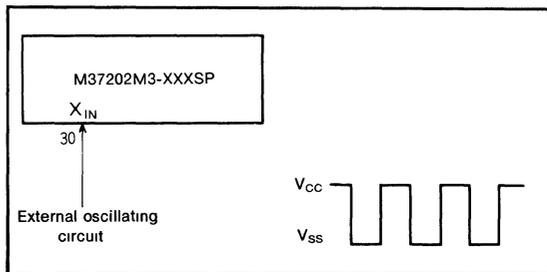


Fig. 50 External clock input circuit

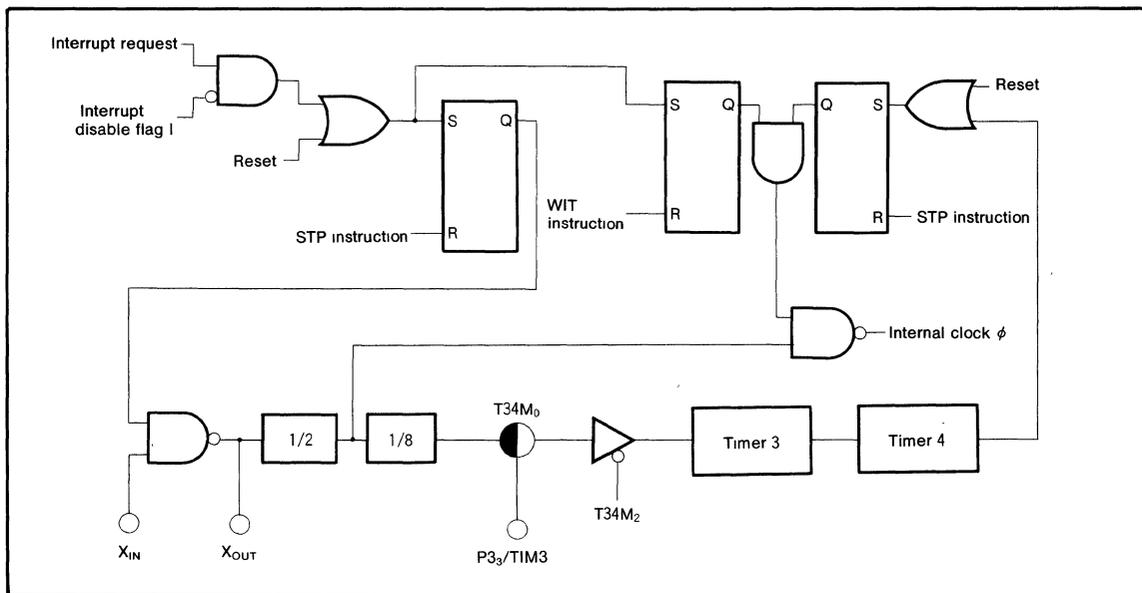


Fig. 51 Block diagram of clock generating circuit

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PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (4) An NOP instruction must be used after the execution of a PLP instruction.
- (5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM order confirmation form
- (2) mask specification form
- (3) ROM data EPROM 3 sets

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3 to 6	V
V_i	Input voltage CNV_{SS}		-0.3 to 6	V
V_i	Input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7,$ $P3_0-P3_6, P4_0-P4_7, P6_0-P6_7,$ $H_{SYNC}, V_{SYNC}, RESET$	With respect to V_{SS}	-0.3 to $V_{CC}+0.3$	V
V_O	Output voltage $P4_0-P4_3, P4_6, P4_7, P6_0-P6_3,$ $P6_6, P6_7$	Output transistors are at "off" state	-0.3 to 13	V
V_O	Output voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7,$ $P3_0-P3_6, P4_4, P4_5, P6_4, P6_5,$ $R, G, B, I, OUT, D-A, X_{OUT}, OSC2$		-0.3 to $V_{CC}+0.3$	V
I_{OH}	Circuit voltage $R, G, B, I, OUT, P0_0-P0_7,$ $P1_0-P1_7, P2_0-P2_7,$ $P3_0, P3_1, D-A$		0 to 1 (Note 1)	mA
I_{OL1}	Circuit voltage $R, G, B, I, OUT, P0_0-P0_7,$ $P1_0-P1_7, P2_0-P2_3,$ $P3_0-P3_6, P6_4, P6_5, D-A$		0 to 2 (Note 2)	mA
I_{OL2}	Circuit voltage $P4_0-P4_3, P4_6, P4_7, P6_0-P6_3, P6_6, P6_7$		0 to 1 (Note 2)	mA
I_{OL3}	Circuit voltage $P2_4-P2_7$		0 to 10 (Note 3)	mA
I_{OL4}	Circuit voltage $P4_4, P4_5$		0 to 3 (Note 2)	mA
P_d	Power dissipation	$T_a=25^\circ C$	550	mW
T_{opr}	Operating temperature		-10 to 70	$^\circ C$
T_{stg}	Storage temperature		-40 to 125	$^\circ C$

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V\pm 10\%$, $T_a=-10$ to $70^\circ C$ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage (Note 4) During the CPU and CRT operation	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	"H" input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7,$ $P3_0-P3_6, P4_0-P4_3, P4_6, P4_7,$ $P6_0-P6_7, H_{SYNC}, V_{SYNC}, RESET,$ $X_{IN}, OSC1$	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $P4_4, P4_5$	$0.7V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7,$ $P3_0, P3_1, P3_5, P4_0-P4_3, P4_7, P6_4, P6_5$	0		$0.4V_{CC}$	V
V_{IL}	"L" input voltage $P3_2-P3_4, P3_6, P4_6, H_{SYNC}, V_{SYNC},$ $RESET, X_{IN}, OSC1$	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage $P4_4, P4_5$	0		$0.3V_{CC}$	V
I_{OH}	"H" average output current (Note 1) $R, G, B, I, OUT, P0_0-P0_7,$ $P1_0-P1_7, P2_0-P2_7, P3_0, P3_1$			1	mA
I_{OL1}	"L" average output current (Note 2) $R, G, B, I, OUT, P0_0-P0_7,$ $P2_0-P2_3, P3_0-P3_6, P6_4, P6_5, D-A$			2	mA
I_{OL2}	"L" average output current (Note 2) $P4_0-P4_3, P4_6, P4_7,$ $P6_0-P6_3, P6_6, P6_7$			1	mA
I_{OL3}	"L" average output current (Note 3) $P2_4-P2_7$			10	mA
I_{OL4}	"L" average output current (Note 2) $P4_4, P4_5$			3	mA
f_{CPU}	Oscillating frequency (for CPU operation) (Note 5)	3.6	4.0	4.4	MHz
f_{CRT}	Oscillating frequency (for CRT display)	6.0	7.0	8.0	MHz
f_{HS}	Input frequency $P3_2-P3_4, P3_6, P4_5$ (S_{CLK})			100	kHz
f_{HS}	Input frequency $P4_5$ (S_{CLK})			1	MHz

Note 1 : The total current that flows out of the IC should be 20mA (max)

2 : The total of I_{OL1} , I_{OL2} and I_{OL4} should be 30mA (max)

3 : The total current of port $P2_4-P2_7$ should be 20mA (max)

4 : Apply 0.022 μ F or greater capacitance externally between the $V_{CC}-V_{SS}$ power supply pins so as to reduce power source noise

Also apply 0.068 μ F or greater capacitance externally between the $V_{CC}-CNV_{SS}$ pins

5 : Use a quartz crystal oscillator or a ceramic resonator for CPU oscillation circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

ELECTRIC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10$ to $70^\circ C$, $f(X_{IN})=4MHz$ unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT OFF		10	20	mA
		$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT ON		20	30	
		At stop mode			300	μA
V_{OH}	"H" output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ , P3 ₁ , R, G, B, I, OUT	$V_{CC}=4.5V$ $I_{OH}=-0.5mA$	2.4			V
V_{OL}	"L" output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₃ , P3 ₀ -P3 ₆ , P6 ₄ , P6 ₅ , ϕ , R, G, B, I, OUT, D-A	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
	"L" output voltage P4 ₀ -P4 ₃ , P4 ₆ , P4 ₇ , P6 ₀ -P6 ₃ , P6 ₆ , P6 ₇	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	
	"L" output voltage P2 ₄ -P2 ₇	$V_{CC}=4.5V$ $I_{OL}=10mA$			3.0	
	"L" output voltage P4 ₄ , P4 ₅	$V_{CC}=4.5V$ $I_{OL}=3mA$			0.4	
$V_{T+}-V_{T-}$	Hysteresis RESET	$V_{CC}=5.0V$		0.5	0.7	V
	Hysteresis (Note 1) H _{SYNC} , V _{SYNC} , P3 ₂ -P3 ₄ , P3 ₆ , P4 ₄ -P4 ₆	$V_{CC}=5.0V$		0.5	1.3	
I_{OZH}	"H" input leak current RESET, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₆ , P4 ₄ , P4 ₅ , P6 ₄ , P6 ₅	$V_{CC}=5.5V$ $V_O=5.5V$			5	μA
	"H" input leak current P4 ₀ -P4 ₃ , P4 ₆ , P4 ₇ , P6 ₀ -P6 ₃ , P6 ₆ , P6 ₇	$V_{CC}=5.5V$ $V_O=12V$			10	
I_{OZL}	"L" input leak current RESET, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₇ , P6 ₀ -P6 ₇	$V_{CC}=5.5V$ $V_O=0V$			5	μA

Note 1. P3₂-P3₄, P3₆ have the hysteresis when these pins are used as interrupt input pins or timer input pins.
P4₄-P4₆ have the hysteresis when these pins are used as serial I/O ports

PRELIMINARY
 Note: The circuit and specification may
 change without notice or charge.

MITSUBISHI MICROCOMPUTERS M37204M8-XXXSP

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
 with ON-SCREEN DISPLAY CONTROLLER**

DESCRIPTION

The M37204M8-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This single-chip microcomputer is useful for the high-tech channel selection system for TVs.

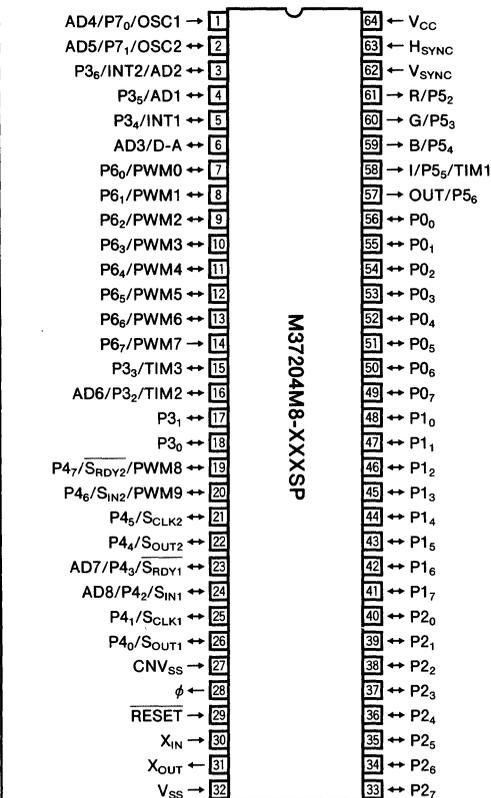
In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

Its screen display function enables it to display channel number and time as well.

FEATURES

- Number of basic instructions..... 69
- Memory size ROM 32768 bytes
 RAM 512 bytes
- Instruction execution time
 1 μ s (minimum instructions at 4MHz frequency)
- Single power supply 5V \pm 10%
- Power dissipation
 normal operation mode (at 4MHz frequency)
 110mW (V_{CC}=5.5V, CRT display)
- Subroutine nesting 96 levels (maximum)
- Interrupt 13types, 13vectors
- 8-bit timer 4
- Programmable I/O ports
 (Ports P0, P1, P2, P3, P4, P6) 47
- Output port (Port P5) 5
- Serial I/O (8-bit) 2
- PWM function 14-bit \times 1
 8-bit \times 10
- A-D converter (6-bit resolution) 8 channels
- CRT display function
 Display characters 24 characters \times 3 lines
 (16 lines maximum)
 Kinds of character types 254 kinds
 Dot structure 12 \times 16 dots
 Character size 4 kinds
 Kinds of color Maximum 15 kinds (R, G, B, I)
 Character unit/border/laster can be specified
 Display layout
 Horizontal 64 levels
 Vertical 128 levels

PIN CONFIGURATION (TOP VIEW)



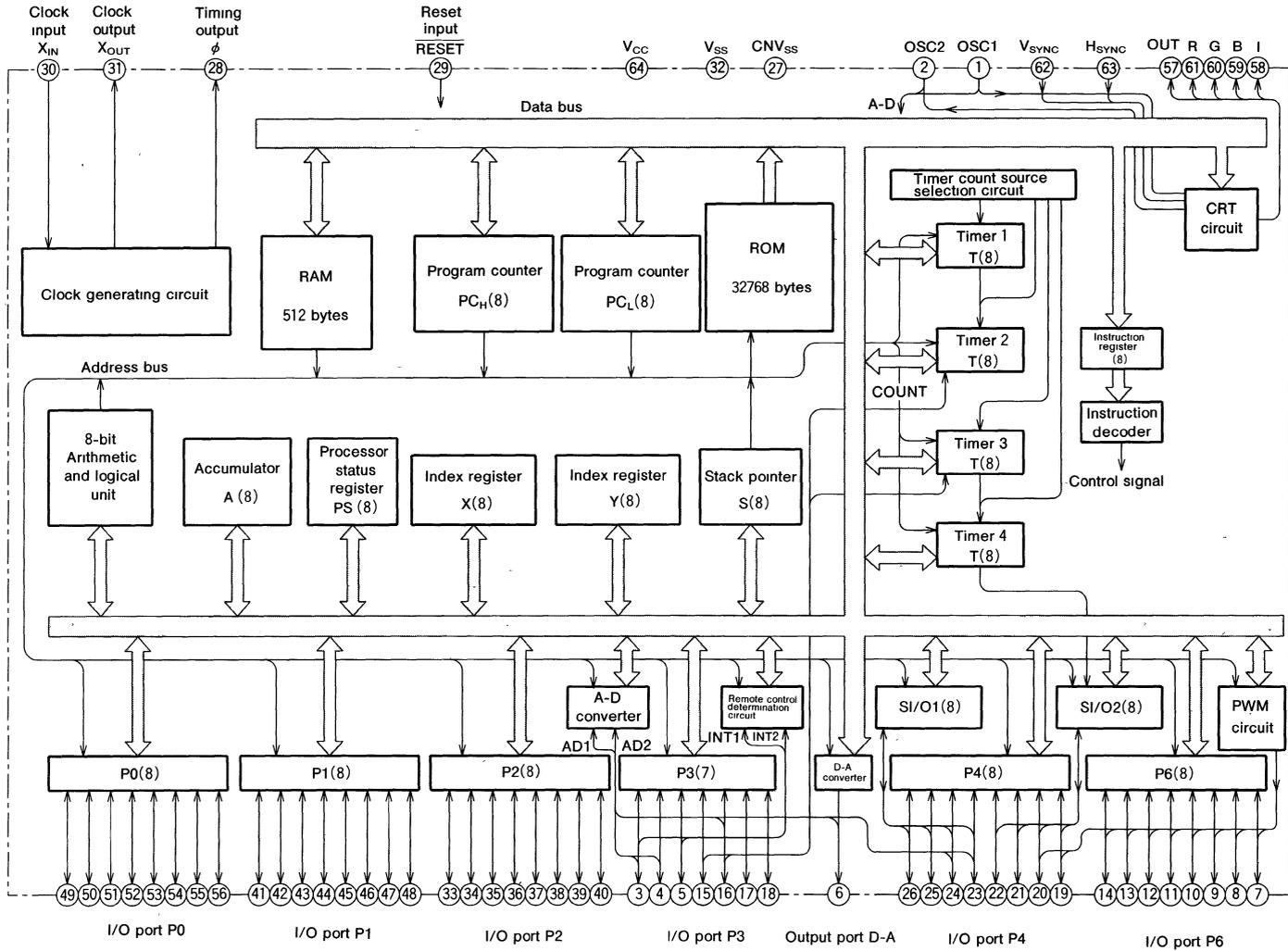
Outline 64P4B

APPLICATION

TV



M37204M8-XXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

MITSUBISHI MICROCOMPUTERS
M37204M8-XXXSP

M37204M8-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONS OF M37204M8-XXXSP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		1 μ s (minimum instructions, at 4MHz frequency)	
Clock frequency		4MHz	
Memory size	ROM	32768 bytes	
	RAM	512 bytes	
Input/Output ports	P0, P1, P2	I/O	8-bitX3
	P3 ₀ , P3 ₁	I/O	2-bitX1
	P3 ₂ —P3 ₆	I/O	5-bitX1 (can be used as timer input pins, INT1, INT2 input pins and A-D input pins)
	P4	I/O	8-bitX1 (can be used as serial I/O function pins and PWM output pins and A-D input pins)
	P5	Output	5-bitX1 (can be used as R, G, B, I, OUT pins)
	P6	I/O	8-bitX1 (can be used as PWM output pins)
Serial I/O		8-bitX2 (Special serial I/O (8-bit)X1)	
Timers		8-bit timerX4	
Subroutine nesting		96levels (maximum)	
Interrupt		Two external interrupts, nine internal interrupts, one software interrupt	
Clock generating circuit		Two built-in circuits (externally connected ceramic or quartz crystal oscillator)	
Supply voltage		5V \pm 10%	
Power dissipation	at CRT display ON	110mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)	
	at CRT display OFF	55mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)	
	at stop mode	1.65mW (Maximum)	
Input/Output characteristics	Input/Output voltage	12V (Ports P4 ₆ , P4 ₇ , P6 ₀ —P6 ₇)	
	Output current	10mA (Ports P2 ₄ —P2 ₇)	
Operating temperature range		-10 to 70°C	
Device structure		CMOS silicon gate process	
Package		M37204M8-XXXSP 64-pin shrink plastic molded DIP	
CRT display function	Display characters	24 charactersX3 lines (maximum 16 lines in program)	
	Dot structure	12X16 dots	
	Kinds of character types	254 kinds	
	Character size	4 kinds	
	Kinds of color	Maximum 15 kinds (R, G, B, I)	
	Display layout	Horizontal 64 levels Vertical 128 levels	

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS} .
CNV _{SS}	CNV _{SS}		This is connected to V _{SS}
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin
P0 ₀ —P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
P1 ₀ —P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0
P2 ₀ —P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0
P3 ₀ —P3 ₆	I/O port P3	I/O	Port P3 is a 7-bit I/O port and has basically the same functions as port P0, but the output structure of P3 ₀ , P3 ₁ is CMOS output and the output structure of P3 ₂ —P3 ₆ is N-channel open drain. P3 ₂ , P3 ₃ are in common with external clock input pins of timer 2 and 3 P3 ₄ , P3 ₅ are in common with external interrupt input pins INT1 and INT2 P3 ₂ , P3 ₅ , P3 ₆ are in common with analog input pins of A-D converter (A-D6, A-D1, A-D2).
P4 ₀ —P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain When serial I/O1 is used, P4 ₀ , P4 ₁ , P4 ₂ and P4 ₃ work as S _{OUT1} , S _{CLK1} , S _{IN1} and $\overline{\text{SRDY1}}$ pins, respectively When serial I/O2 is used, P4 ₄ , P4 ₅ , P4 ₆ and P4 ₇ work as S _{OUT2} , S _{CLK2} , S _{IN2} and $\overline{\text{SRDY2}}$ pins, respectively When special serial I/O is used, P4 ₄ and P4 ₅ work as SDA and SCL pins, respectively Also P4 ₆ , P4 ₇ are in common with PWM output pins of PWM 9 and PWM 8 P4 ₂ , P4 ₃ are in common with analog input pins of A-D converter (A-D8, A-D7).
P6 ₀ —P6 ₇	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain This port is in common with PWM output pins PWM0—PWM7
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display function OSC1 and OSC2 pins are in common with analog input pins of A-D converter (A-D4, A-D5)
H _{SYNC}	H _{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display
V _{SYNC}	V _{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display
R, G, B, I, OUT	CRT output	Output	This is a 5-bit output pin for CRT display The output structure is CMOS output This is in common with port P5 ₂ —P5 ₆
D-A	DA Output	Output	This is an output pin for 14-bit PWM, and in common with analog input pin of A-D converter (A-D3)

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER****FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)**

The M37204 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address 00FB₁₆. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

Page 1 (addresses 0100₁₆ to 01FF₁₆) is normally used as a stack area. The zero page (addresses 0000₁₆ to 00BF₁₆) can also be used by setting bit 2 of the CPU mode register (address 00FB₁₆) to "0".

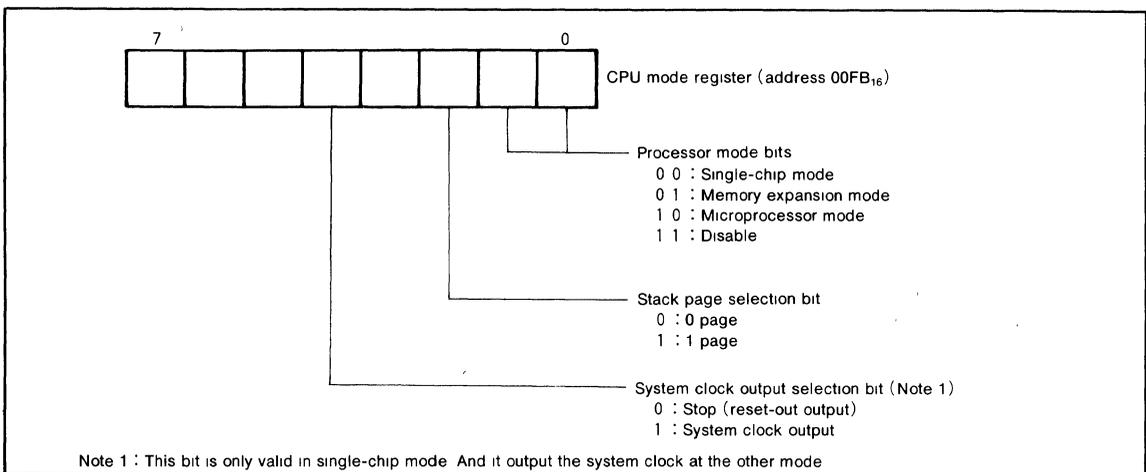


Fig. 1 Structure of CPU mode register

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **CRT display RAM**

CRT display RAM is used for specifying the character codes and colors to display.

• **CRT display ROM**

CRT display ROM is used for storing character data.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

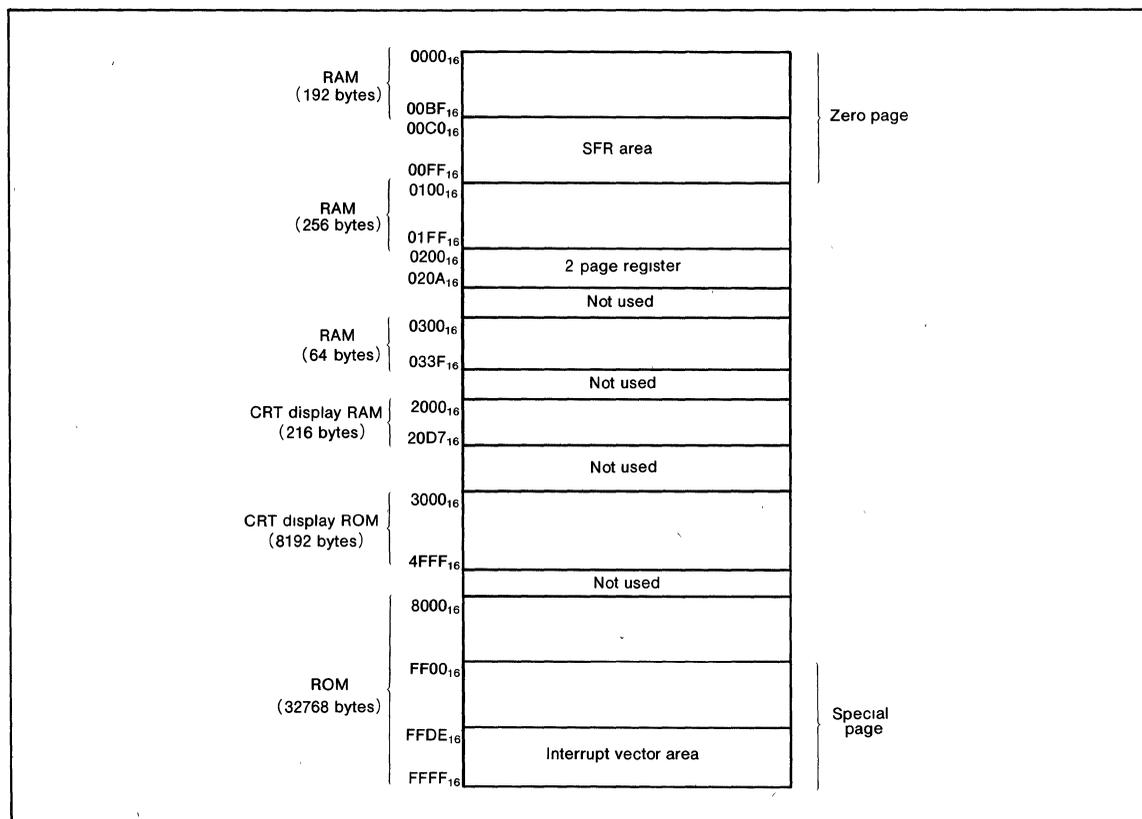


Fig. 2 Memory map

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

00C0 ₁₆	Port P0	00E0 ₁₆	Horizontal position register
00C1 ₁₆	Port P0 direction register	00E1 ₁₆	Vertical display start position register 1
00C2 ₁₆	Port P1	00E2 ₁₆	Vertical display start position register 2
00C3 ₁₆	Port P1 direction register	00E3 ₁₆	Vertical display start position register 3
00C4 ₁₆	Port P2	00E4 ₁₆	Character size register
00C5 ₁₆	Port P2 direction register	00E5 ₁₆	Border selection register
00C6 ₁₆	Port P3	00E6 ₁₆	Color register 0
00C7 ₁₆	Port P3 direction register	00E7 ₁₆	Color register 1
00C8 ₁₆	Port P4	00E8 ₁₆	Color register 2
00C9 ₁₆	Port P4 direction register	00E9 ₁₆	Color register 3
00CA ₁₆	Port P5	00EA ₁₆	CRT control register 1
00CB ₁₆	Port P5 direction register	00EB ₁₆	Display block counter
00CC ₁₆	Port P6	00EC ₁₆	CRT port control register
00CD ₁₆	Port P6 direction register	00ED ₁₆	Scroll control register
00CE ₁₆	DA-H register	00EE ₁₆	Scroll start register
00CF ₁₆	DA-L register	00EF ₁₆	A-D control register 1
00D0 ₁₆	PWM 0 register	00F0 ₁₆	Timer 1
00D1 ₁₆	PWM 1 register	00F1 ₁₆	Timer 2
00D2 ₁₆	PWM 2 register	00F2 ₁₆	Timer 3
00D3 ₁₆	PWM 3 register	00F3 ₁₆	Timer 4
00D4 ₁₆	PWM 4 register	00F4 ₁₆	Timer 12 mode register
00D5 ₁₆	PWM output control register 1	00F5 ₁₆	Timer 34 mode register
00D6 ₁₆	PWM output control register 2	00F6 ₁₆	PWM 5
00D7 ₁₆	Interrupt space distinguish register	00F7 ₁₆	PWM 6
00D8 ₁₆	Interrupt space distinguish control register	00F8 ₁₆	PWM 7
00D9 ₁₆	Special serial I/O register	00F9 ₁₆	PWM 8
00DA ₁₆	Special mode register 1	00FA ₁₆	PWM 9
00DB ₁₆	Special mode register 2	00FB ₁₆	CPU mode register
00DC ₁₆	Serial I/O1 mode register	00FC ₁₆	Interrupt request register 1
00DD ₁₆	Serial I/O1 register	00FD ₁₆	Interrupt request register 2
00DE ₁₆	Serial I/O2 mode register	00FE ₁₆	Interrupt control register 1
00DF ₁₆	Serial I/O2 register	00FF ₁₆	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

0200 ₁₆	
0201 ₁₆	
0202 ₁₆	
0203 ₁₆	
0204 ₁₆	
0205 ₁₆	
0206 ₁₆	Port control register
0207 ₁₆	Shift register input control register
0208 ₁₆	CRT control register 2
0209 ₁₆	CRT clock selection register
020A ₁₆	A-D control register 2

Fig. 4 2 page register memory map

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

INTERRUPTS

Interrupts can be caused by 12 different events consisting of three external, eight internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 5 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 6 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
CRT interrupt	2	FFFD ₁₆ , FFFC ₁₆	
INT2 interrupt	3	FFFB ₁₆ , FFFA ₁₆	
INT1 interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	
Serial I/O2 interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	
Timer 4 interrupt	6	FFF5 ₁₆ , FFF4 ₁₆	
1 ms interrupt	7	FFF3 ₁₆ , FFF2 ₁₆	
V _{SYNC} interrupt	8	FFF1 ₁₆ , FFF0 ₁₆	
Timer 3 interrupt	9	FFEF ₁₆ , FFEE ₁₆	
Timer 2 interrupt	10	FFED ₁₆ , FFEC ₁₆	
Timer 1 interrupt	11	FFEB ₁₆ , FFEA ₁₆	
Serial I/O1 interrupt	12	FFE9 ₁₆ , FFE8 ₁₆	
BRK instruction interrupt	13	FFDF ₁₆ , FFDE ₁₆	Non-maskable software interrupt

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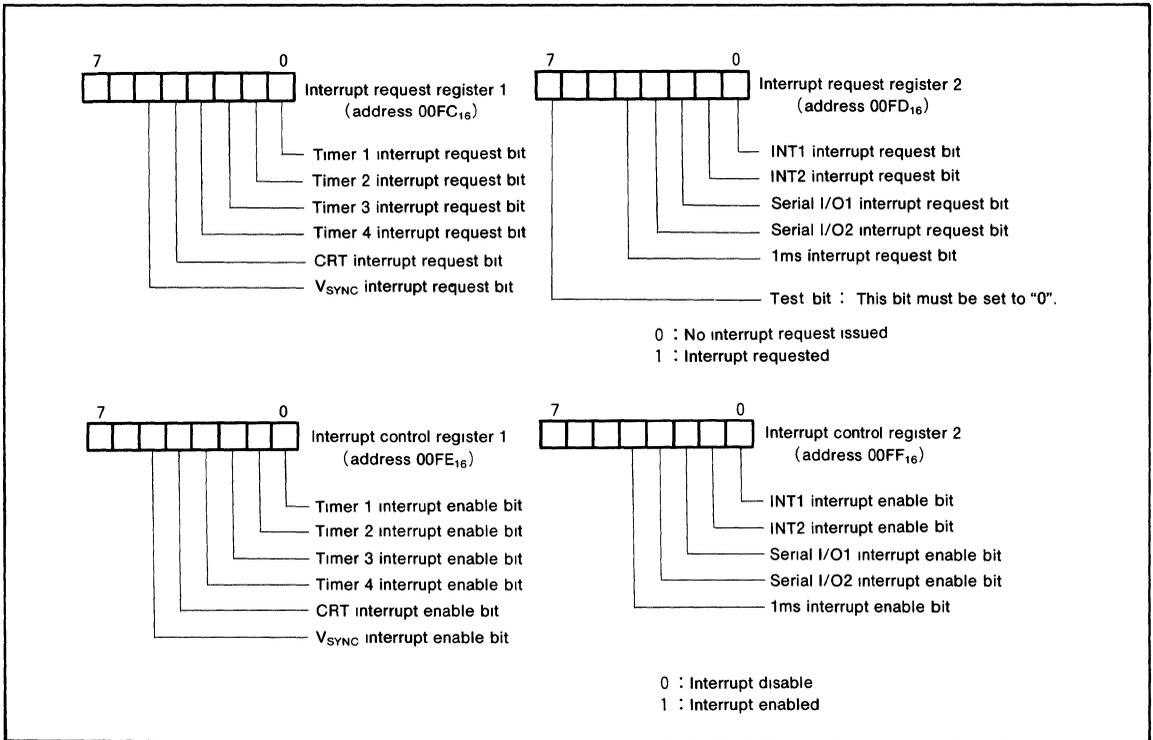


Fig. 5 Structure of registers related with interrupt

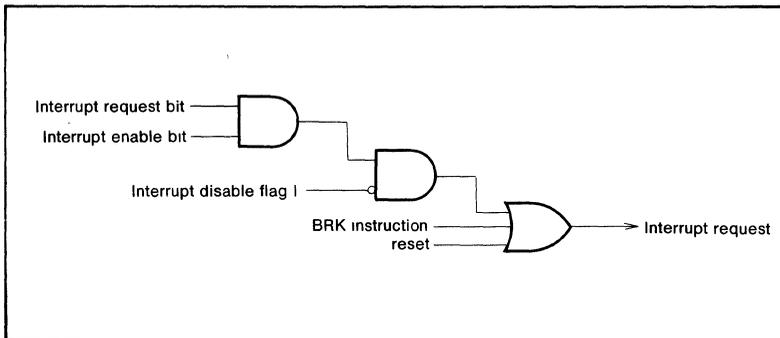


Fig. 6 Interrupt control

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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TIMER

The M37204M8-XXXSP has four timers; timer 1, timer 2, timer 3 and timer 4. All of timers are 8-bit structure and have 8-bit latches.

A block diagram of timer 1 through 4 is shown in Figure 8. All of the timers are down count timers and their division ratio are $1/(n+1)$, where n is the contents of timer latch. The same value is set to timer by writing the count value to the latch (00F0₁₆ to 00F3₁₆ : timer 1 to timer 4). When a timer reaches "00₁₆" and the next count pulse is input to a timer, a value which is the contents of the reload latch are loaded into the timer. The timer interrupt request bit is set at the next count pulse after the timer reaches "00₁₆". The contents of each timer is shown in following.

(1) Timer 1

Either $f(X_{IN})$ divided by 16 or a 1024 μ s clock (1 μ s interrupt signal) can be selected as the count source of timer 1. When bit 0 of the timer 12 mode register (address 00F4₁₆) is "0", $f(X_{IN})$ divided by 16 is selected; when it is "1", the 1024 μ s clock is selected.

Timer 1 interrupt request is occurred with timer 1 overflow.

(2) Timer 2

$f(X_{IN})$ divided by 16, timer 1 overflow signal, or an external clock input from P3₂/TIM2 pin can be selected as the count source of timer 2 by specifying bits 4 and 1 of the timer 12 mode register (address 00F4₁₆).

Timer 2 interrupt request is occurred with timer 2 overflow.

(3) Timer 3

Either $f(X_{IN})$ divided by 16 or an external clock input from P3₃/TIM3 pin can be selected as the count source of timer 3 by specifying bit 0 of the timer 34 mode register (address 00F5₁₆).

Timer 3 interrupt request is occurred with timer 3 overflow.

(4) Timer 4

$f(X_{IN})$ divided by 16, $f(X_{IN})$ divided by 2, or timer 3 overflow signal can be selected as the count source of timer 4 by specifying bits 4 and 1 of the timer 34 mode register (address 00F5₁₆).

Timer 4 interrupt request is occurred with timer 4 overflow. And the timer 4 overflow signal can be used as the clock source of special serial I/O.

At reset or an STP instruction is executed timer 3 and timer 4 are connected automatically, and the value "FF₁₆" is set to timer 3, and the value "07₁₆" is set to timer 4.

$f(X_{IN})$ divided by 16 is selected as count source of timer 3. When the internal reset is removed or stop mode is removed, the internal clock is connected by timer 4 overflow at above state. In this reason, the program starts with stable clock.

The timer related registers structure is shown in Figure 7.

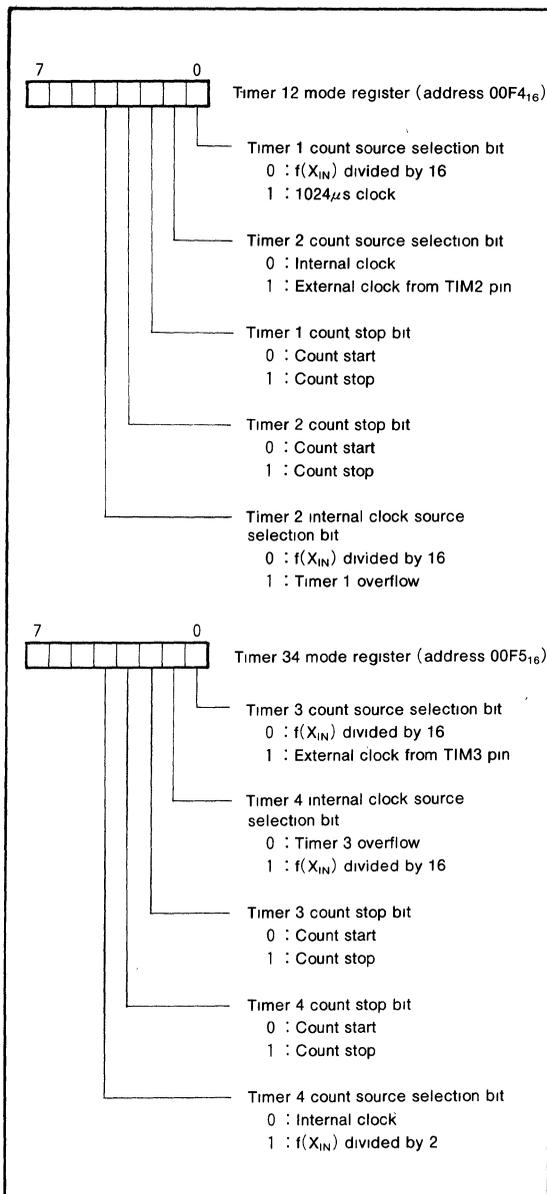


Fig. 7 Structure of timer 12 mode register and timer 34 mode register

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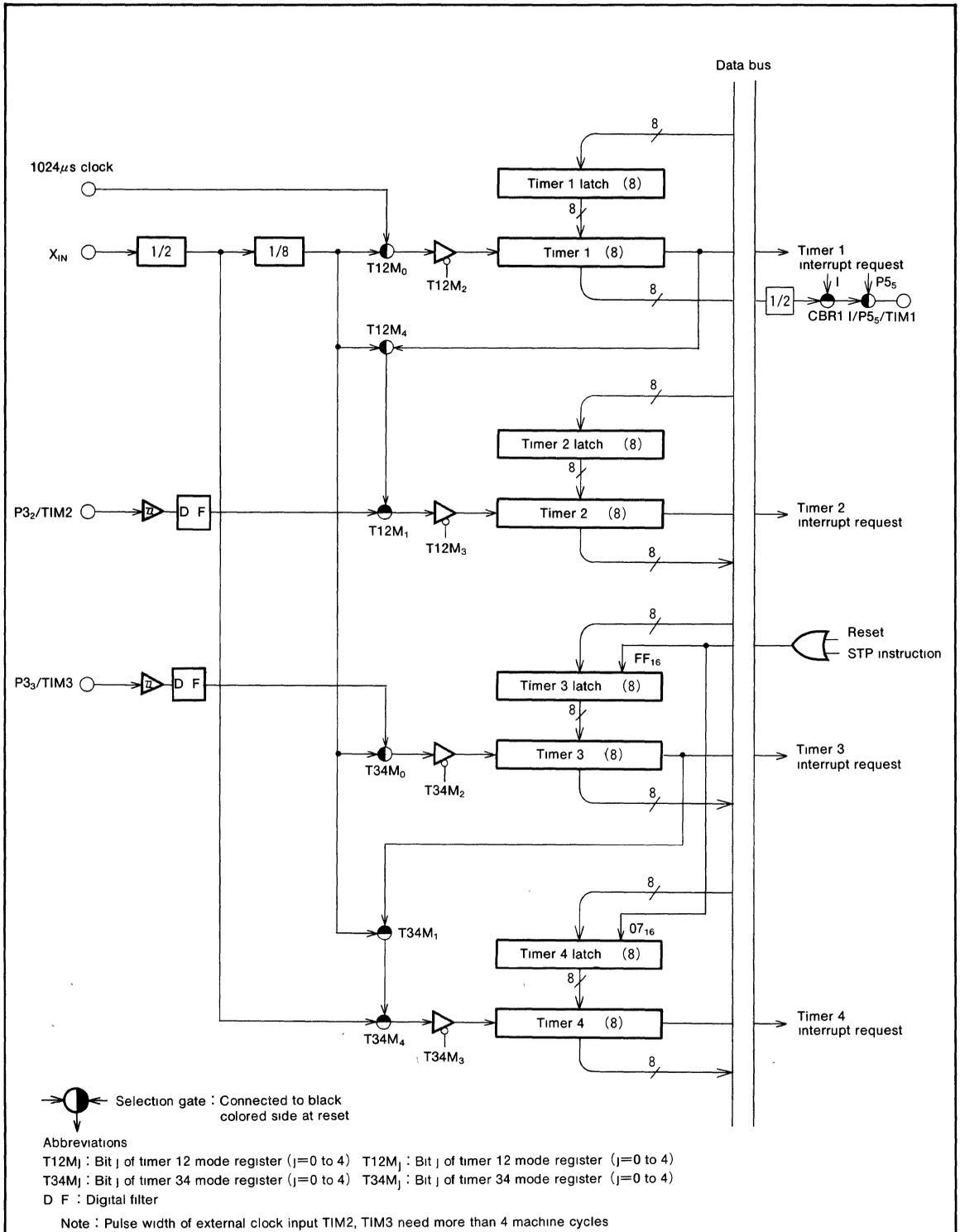


Fig. 8 Block diagram of timer 1, timer 2, timer 3 and timer 4

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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SERIAL I/O

M37204M8-XXXSP has two serial I/O (serial I/O1, serial I/O2). Serial I/O1 has the same function as serial I/O2.

A block diagram of the serial I/O is shown in Figure 9.

In the serial I/O mode the receive ready signal ($\overline{S_{RDY1}}$), synchronous input/output clock (S_{CLK1}), and the serial I/O pins (S_{OUT1} , S_{IN1}) are used as port P4. The serial I/O mode registers (addresses 00DC₁₆ and 00DE₁₆) are 8-bit registers. Bits 0, 1 and 2 of these registers are used to select a synchronous clock source.

Bits 3 and 4 decide whether parts of P4 will be used as a serial I/O or not.

To use P4₂ or P4₆ as a serial input, set the direction register bit which corresponds to P4₂ or P4₆ to "0". For more information on the direction register, refer to the I/O pin section.

Also to use internal clock of serial I/O2, bit 1 of special mode register 1 (address 00DA₁₆) needs to be set to "1". The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

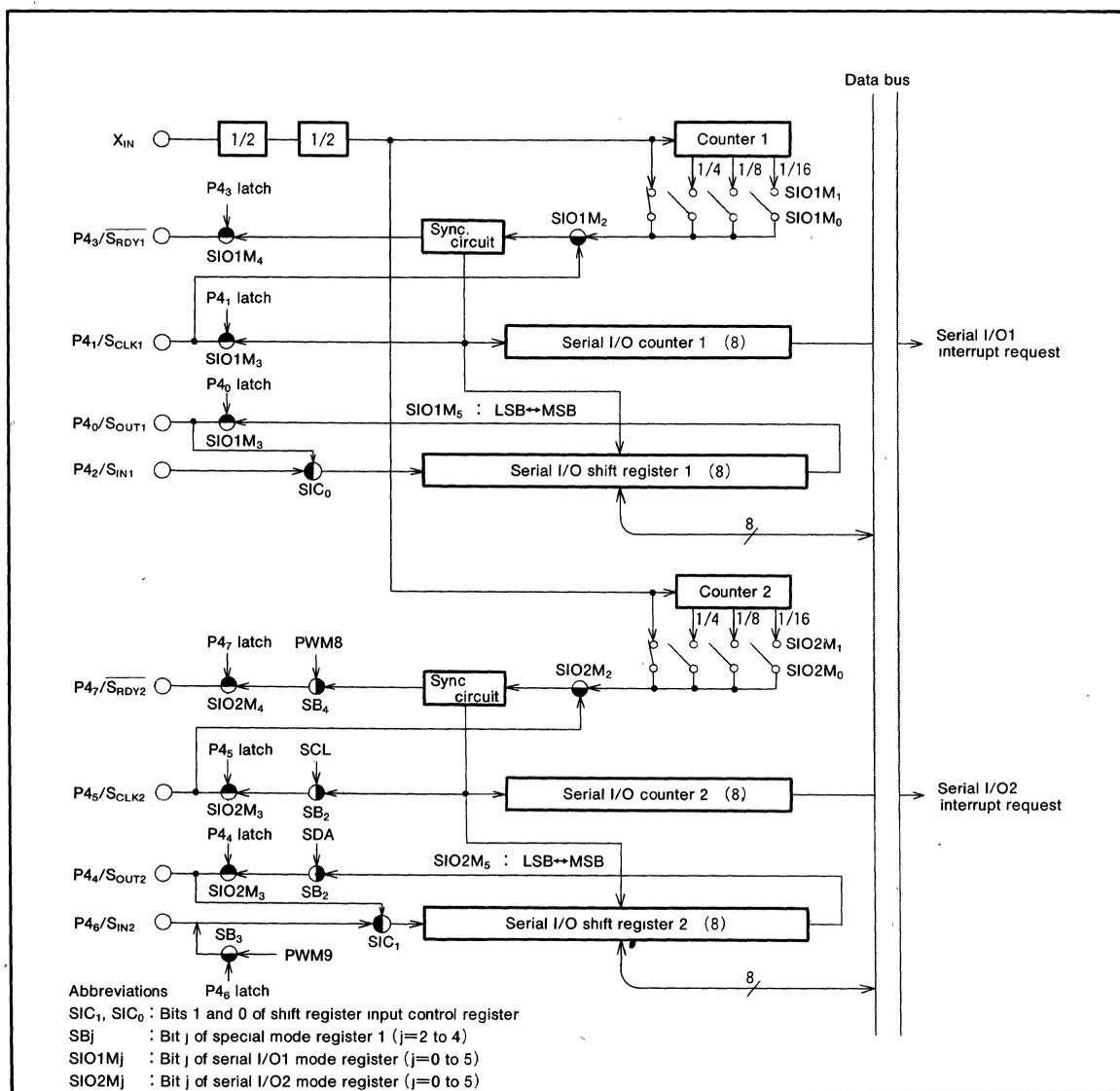


Fig. 9 Block diagram of serial I/O

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Internal clock—The \overline{SRDY}_i signal becomes "H" during transmission or while dummy data is stored in the serial I/O_i register (addresses 00DD₁₆ and 00DF₁₆). After the falling edge of the write signal, the \overline{SRDY}_i signal becomes low signaling that the M37204M8-XXXSP is ready to receive the external serial data. The \overline{SRDY}_i signal goes "H" at the next falling edge of the transfer clock. The serial I/O_i counter is set to 7 when data is stored in the serial I/O_i register. At each falling edge of the transfer clock, serial data is output to S_{OUT_i}. During the rising edge of this clock, data can be input from S_{IN_i} and the data in the serial I/O_i register will be shifted 1 bit.

Transfer direction can be selected by bit 5 of serial I/O_i mode register. After the transfer clock has counted 8 times, the serial I/O_i register will be empty and the transfer clock will remain at a high level. At this time the interrupt request

bit will be set.

External clock- If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 10. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O_i counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

An example of communication between two M37204M8-XXXSPs is shown in Figure 11.

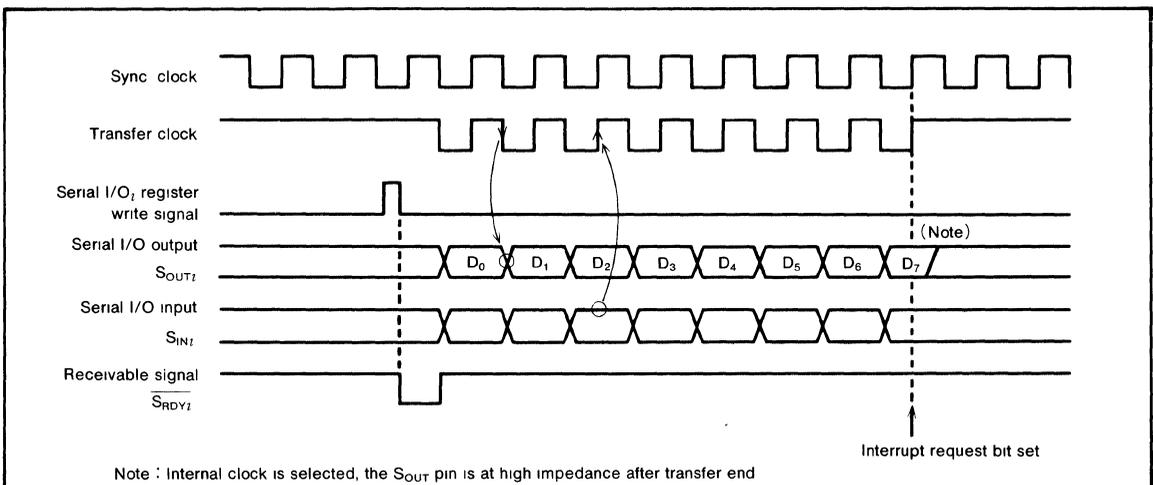


Fig. 10 Serial I/O timing (In the case of LSB first)

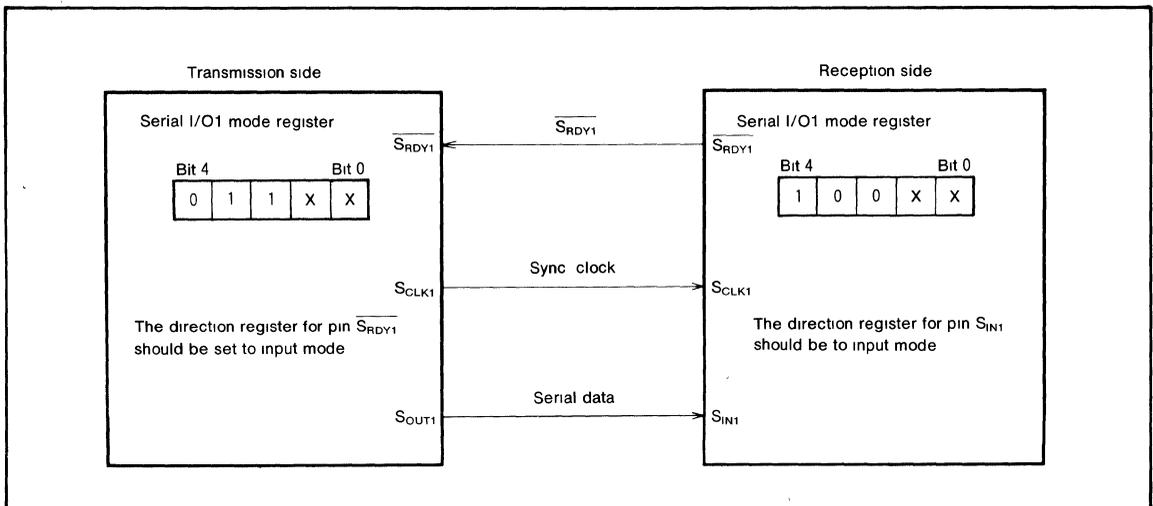


Fig. 11 Example of serial I/O connection

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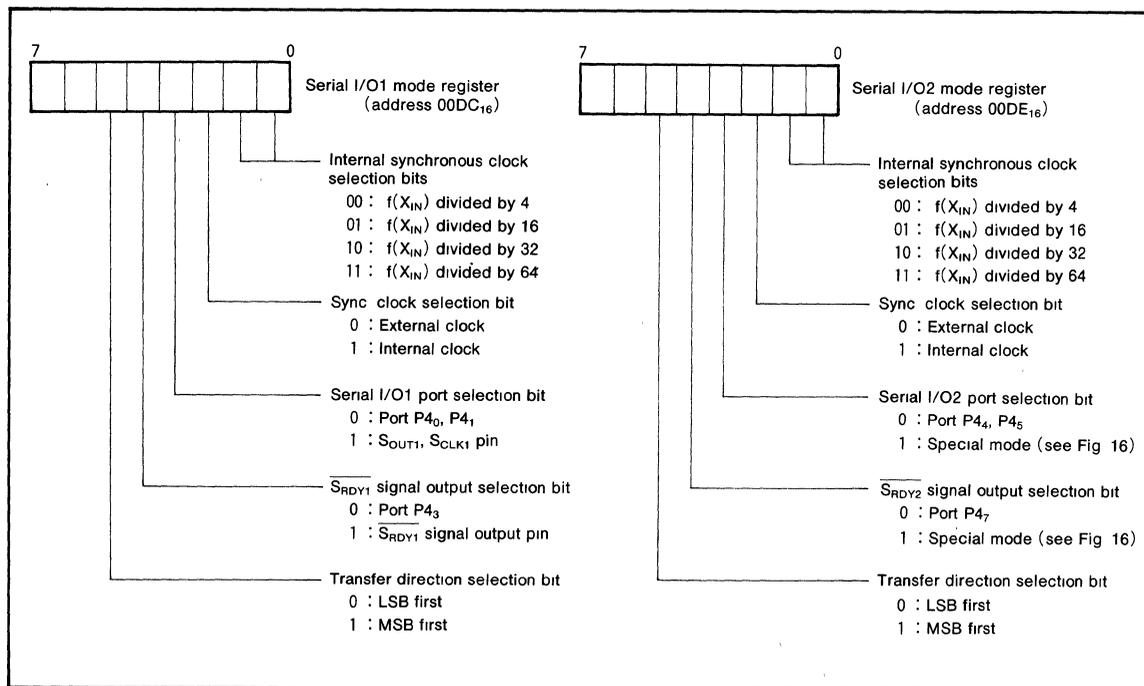


Fig. 12 Structure of serial I/O_i mode register

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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SPECIAL MODE (I²C BUS MODE*)

M37204M8-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I²C* (Inter IC) bus format.

I²C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery.

M37204M8-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O are explained in the following:

(1) Master transmission

① To generate an interrupt at the end of transmission, set bit 7 of special mode register 2 (address 00DB₁₆) to "1" so as to special serial I/O interrupt is selected.

② Then set bit 3 of interrupt control register 2 (address 00FF₁₆) to "1" so as to special serial I/O interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

③ The output signals of master transmission SDA and SCL are output from ports P₄₄ and P₄₅. Set all bits (bits 4 and 5) corresponding to P₄₄ and P₄₅ of the port P4 register (address 00C8₁₆) and the port P4 direction register (address 00C9₁₆) to "1".

④ Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4. (For instance, if $f(X_{IN})/16$ is selected as the clock source of timer 4 and 4 is set in timer 4 when $f(X_{IN})$ is 4MHz, the master transmission clock frequency is 25kHz.)

⑤ Set contents of the special mode register 2 (address 00DB₁₆). (Usually, the value is "83₁₆".)

⑥ Set the bit 3 of serial I/O2 mode register (address 00DE₁₆). After that set the special mode register 1 (address 00DA₁₆). Figure 16 shows the structure of special mode registers 1 and 2.

Initial setting is completed by the above procedure

⑦ Write data to be transmitted in the special serial I/O register (address 00D9₁₆). Immediately after this, clear bits 0 and 1 of special mode register 2 (to "0") to make both

SDA and SCL output to "L". This is for arbitration. The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK reception and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 3 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

⑧ To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

⑨ To terminate data transfer, clear bits 0 and 1 of the special mode register 2 to "0".

⑩ Set bit 1 clock SCL to "1".

⑪ Then set bit 1 data SDA to "1". This procedure transmits the stop signal. Figure 14 shows master transmission timing explained above.

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission (the process until ⑦ in Figure 14).

In the interrupt routine, set master reception ACK provided (26₁₆) in the special mode register 1 (address 00DA₁₆), and write "FF₁₆" in the special serial I/O register (address 00D9₁₆). This sets data line SDA to "H" and to perform 8-clock master reception. Then, "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission (the process from ⑨ to ⑪ in Figure 14).

Figure 15 shows master reception timing.

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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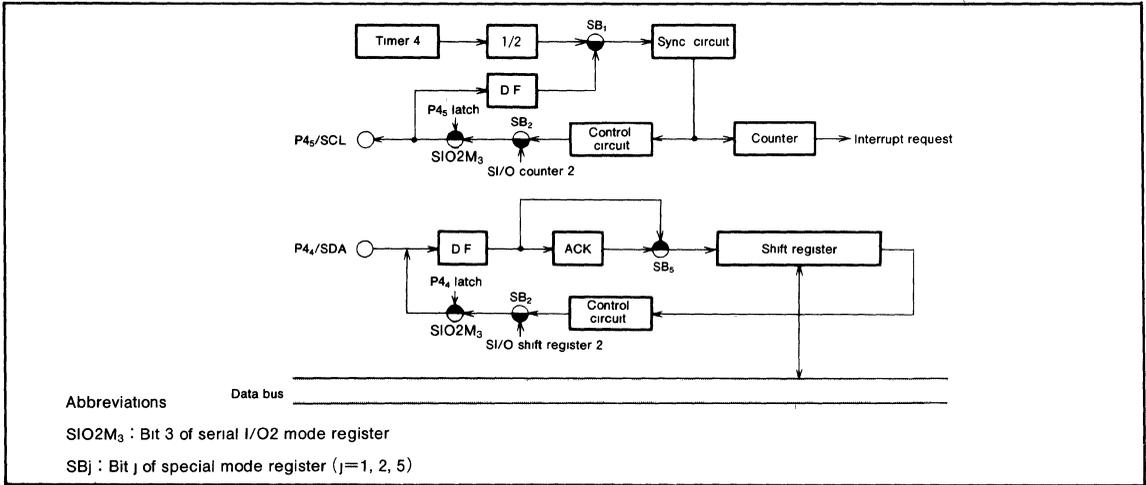


Fig. 13 Block diagram of special serial I/O

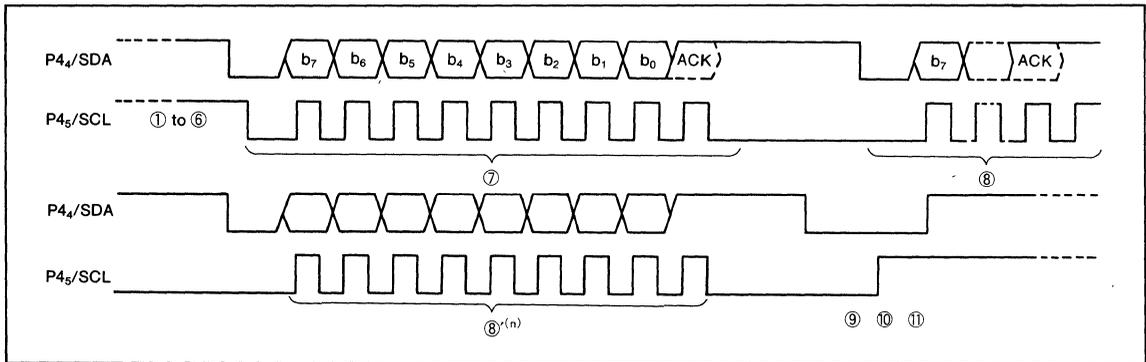


Fig. 14 Master transmission timing

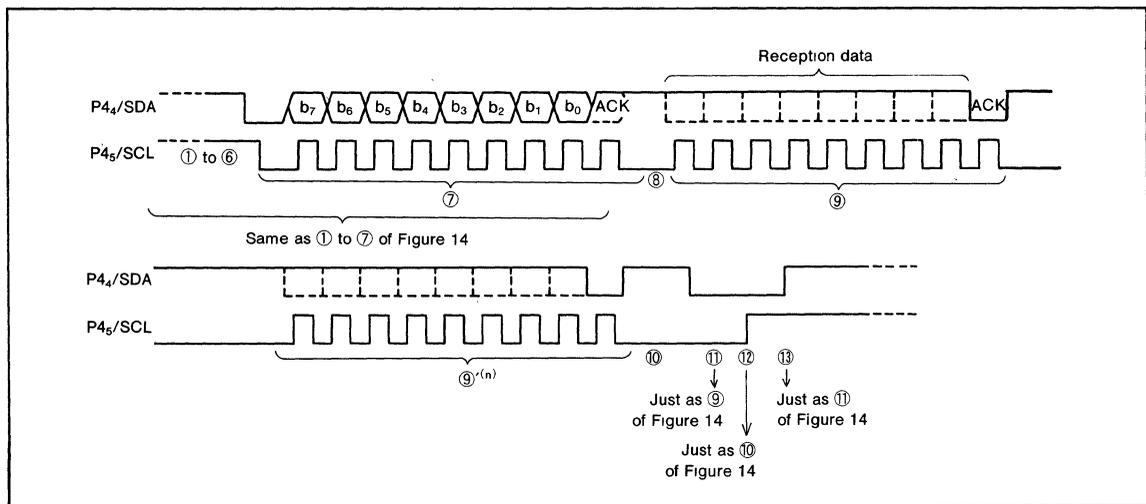


Fig. 15 Master reception timing

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(3) Wait function

Wait function 1 holds the SCL line at "L" after the 8th clock falls in special mode. Wait function 2 holds the SCL line at "L" after the 9th clock falls in the same way.

When one of the wait functions operates, the internal counter that counts the clock must be reset after bit 3 or 4 of the special mode register 2 is set to "1", to enable the corresponding wait function 1 or 2 to operate. Reset the internal counter by writing data to the special serial I/O register (address 00D9₁₆), or by setting the START signal detection bit to "1". Reset the internal counter for each byte before data transfer.

The wait functions can be released by setting the corresponding bit 5 or 6 of the special mode register 2 to "1".

Note 1 : Clear the START signal detect bit (bit 6) and the STOP signal detect bit (bit 7) of the special mode register 1 by writing "1" to bit 6 or bit 7.

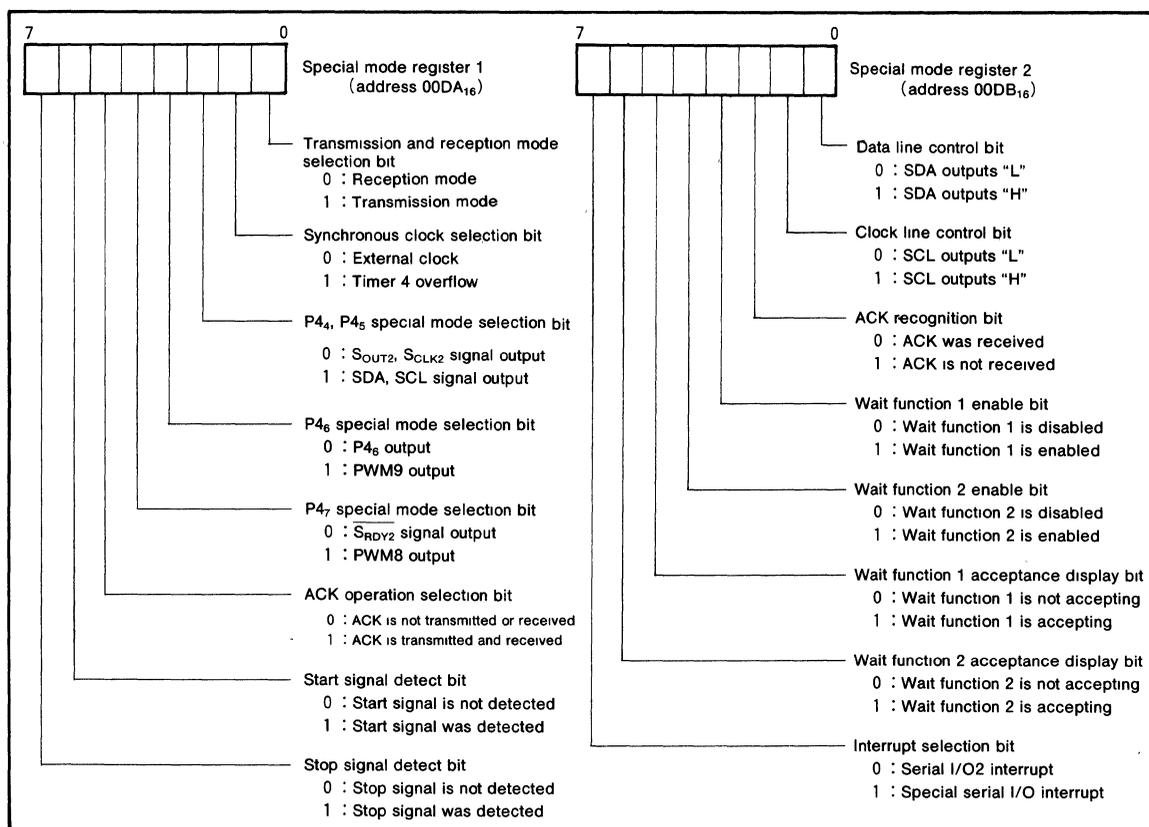


Fig. 16 Structure of special mode registers 1 and 2

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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SERIAL I/O COMMON TRANSFER MODE

The S_{IN} and S_{OUT} signals can be switched internally, to switch between serial transmission and serial reception, by writing "1" to either bit 1 or bit 0 of the shift register input control register.

Signal lines in serial I/O common transfer mode are shown in Figure 19.

Note : During serial reception, make sure that serial reception start after "FF₁₆" is written to the serial I/O shift register.

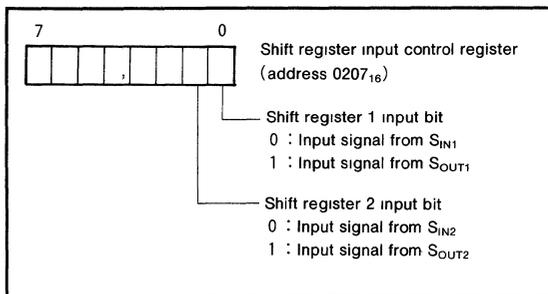


Fig. 17 Structure of the shift register input control register

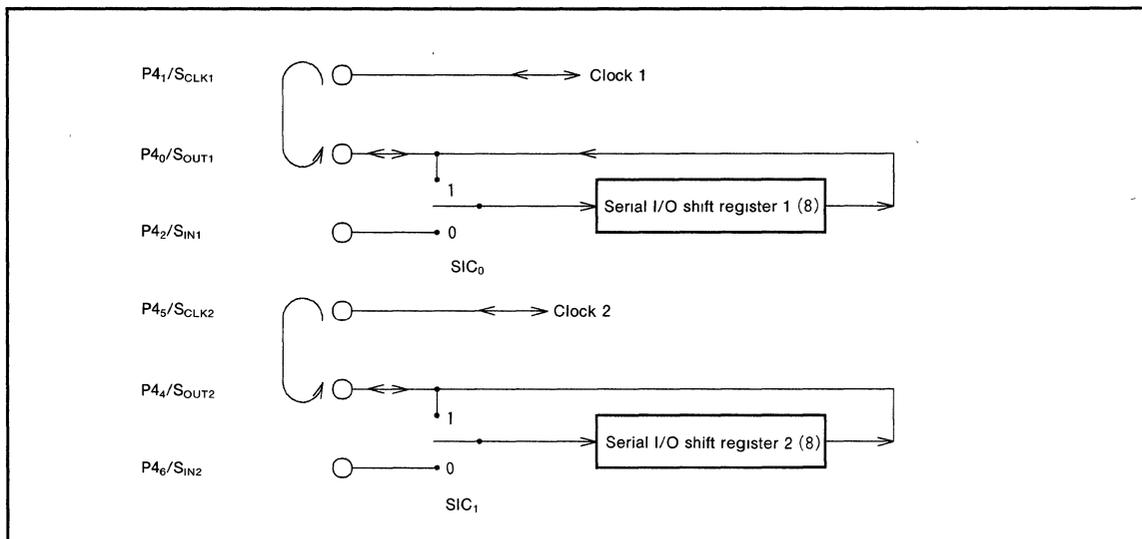


Fig. 18 Signal lines in serial I/O common transfer mode

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

PWM OUTPUT CIRCUIT

(1) Introduction

The M37204M8-XXXSP is equipped with one 14-bit PWM(DA) and ten 8-bit PWMs (PWM0—PWM9). The 14-bit resolution gives DA the minimum resolution bit width of 500ns (for $X_{IN}=4\text{MHz}$) and a repeat period of 8192 μs . PWM0—PWM9 have a 8-bit resolution with minimum resolution bit width of 8 μs and repeat period of 2048 μs .

Block diagram of the PWM is shown in Figure 19.

The PWM timing generator section applies individual control signals to DA and PWM0—PWM9 using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM0—PWM7 are in common with port P6 and PWM8, 9 are in common with port P4₇, P4₆. For PWM output, each PWM output selection bits (bits 2 to 7 of PWM output control register 1, bits 0 and 1 of PWM output control register 2, bits 3 and 4 of special mode register 1 and bit 4 of serial I/O2 mode register) should be set. When DA is used for output, first set the higher 8-bit of the DA-H register (address 00CE₁₆), then the lower 6-bit of the DA-L register (address 00CF₁₆).

When one of the PWM0—PWM9 is used for output, set the 8-bit in the PWM0—PWM9 register (addresses 00D0₁₆ to 00D4₁₆ and 00F6₁₆ to 00FA₁₆), respectively.

(3) Transferring data from registers to latches

The data written to the 8-bit PWM register is transferred to the PWM latch in each 8-bit PWM cycle period. For 14-bit PWM, the data is transferred in the next upper 8-bit period after the write. The signals output to the PWM pins correspond to the contents of these latches. When data in each PWM register is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. However, bit 7 of the DA-L register indicated the completion of the data transfer from the DA register to the DA latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 8-bit PWMs

The timing diagram of the ten 8-bit PWMs (PWM0—PWM9) is shown in Figure 20. One period (T) is composed of 256 (2⁸) segments.

There are eight different pulse types configured from bits 0 to 7 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 20 (a).

Eight different pulses can be output from the PWM. These can be selected by bits 0 through 7. Depending on the content of the 8-bit PWM latch, pulses from 7 to 0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 20 (b). Changes in the contents of the PWM latch allows the selection of 256 lengths of high-level area outputs varying from 0/256 to 255/256. An length of entirely high-level output cannot be output, i.e. 256/256.

(5) 14-bit PWM operation

The output example of the 14-bit PWM is shown in Figure 21. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length D_H times τ is output every short area of $t=256 \tau=128\mu\text{s}$ as determined by data D_H of the higher 8 bits.

Thus, the time for the high-level area is equal to the time set by the higher 8 bits or that plus τ . As a result, the short-area period t ($=128\mu\text{s}$, approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P4₆, P4₇ and P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 low-order bits of data and high-level area increase space

6 low-order bits of data	Area longer by τ than that of other t_m ($m=0$ to 63)
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m=32$
0 0 0 0 1 0	$m=16, 48$
0 0 0 1 0 0	$m=8, 24, 40, 56$
0 0 1 0 0 0	$m=4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m=1, 3, 5, 7, \dots, 57, 59, 61, 63$

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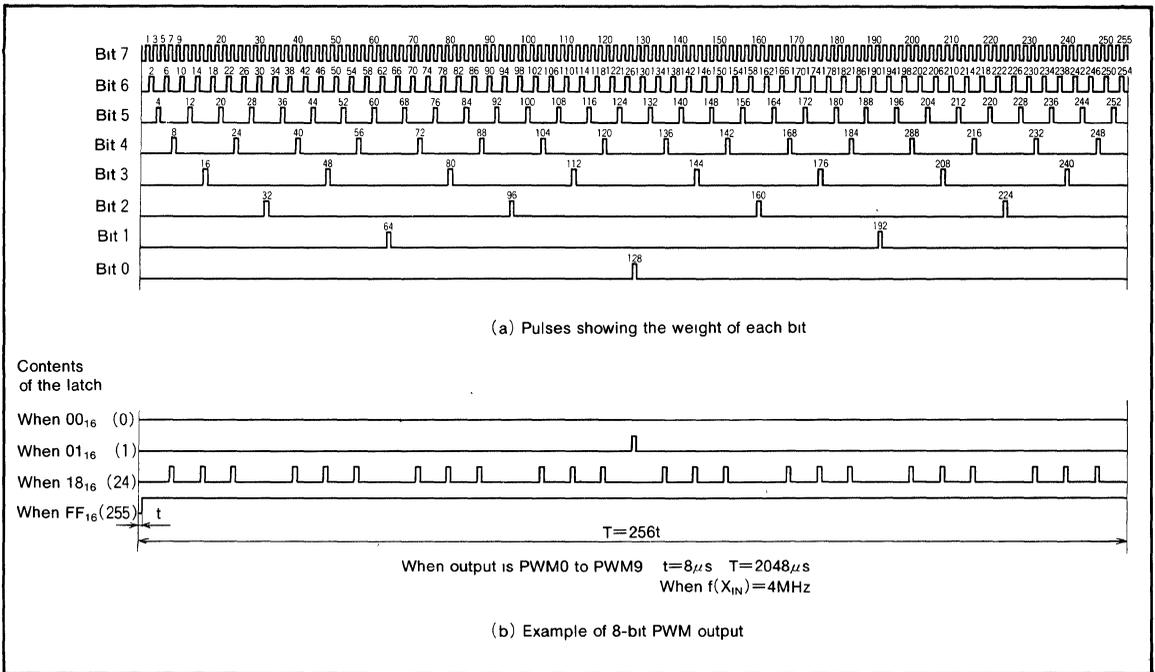


Fig. 20 8-bit PWM timing diagram

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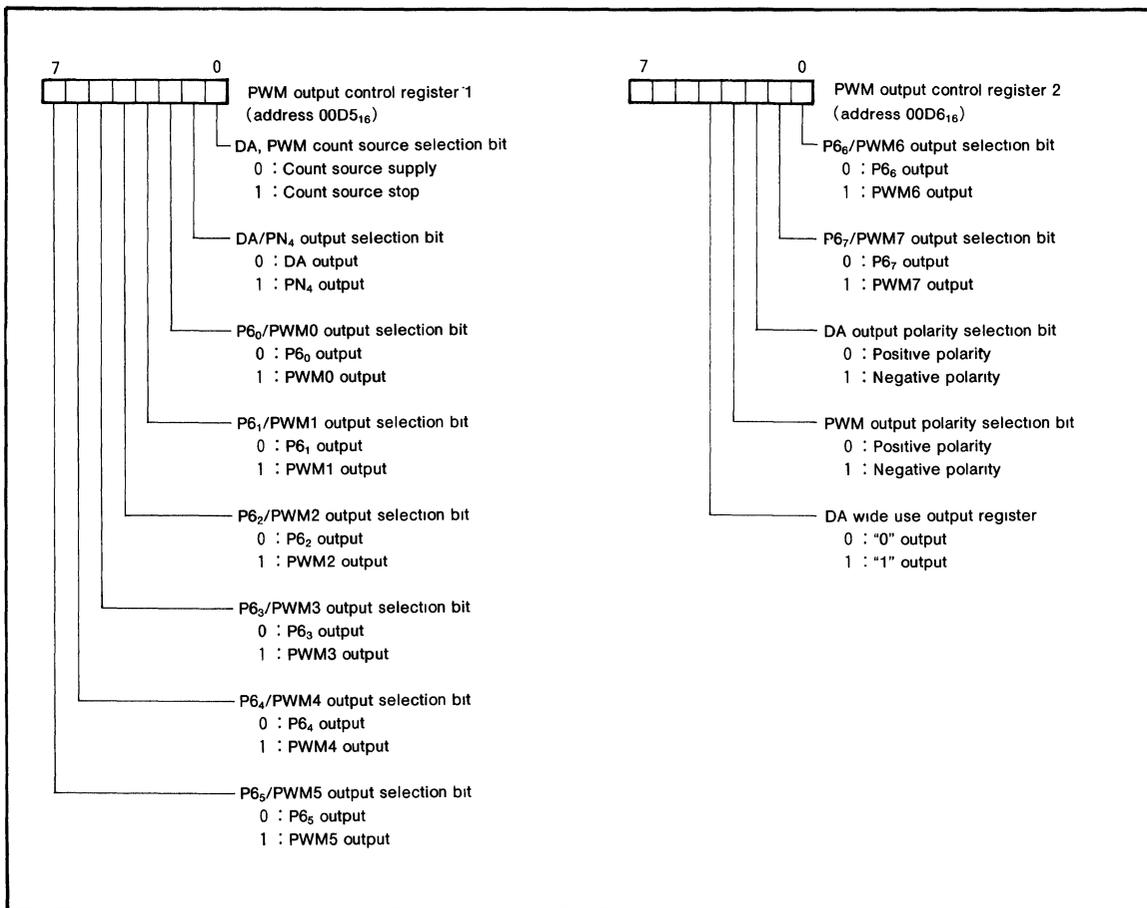


Fig. 22 Structure of PWM output control register 1 and 2

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A-D CONVERTER

Block diagram of A-D converter is shown in Figure 24. A-D converter consists of 6-bit D-A converter and comparator. The A-D control register 2 (address 020A₁₆) can generate 1/64 V_{CC}-step internal analog voltage based on the settings of bits 5 to 0.

Table 3 gives the relation between the descriptions of A-D control register bits 5 to 0 and the generated internal analog voltage. The comparison result of the analog input voltage and the internal analog voltage is stored in the A-D control register 1 (address 00EF₁₆), bit 4.

The data is compared by setting the direction register corresponding to port P3₅, P3₆ to "0" (port P3₅, P3₆ enters the input mode), to allow port P3₅/A-D1, P3₆/A-D2 to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register, bits 0 to 5 and an analog input pin is selected. After 16 machine cycle, the voltage comparison is completed.

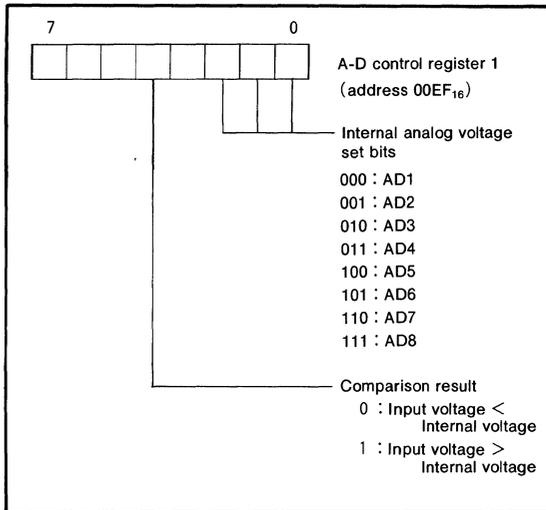


Fig. 23 Structure of A-D control register 1

Table 3. Relationship between the contents of A-D control register2 and internal analog voltage

A-D control register						Internal analog voltage
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	0	1/128 V _{CC}
0	0	0	0	0	1	3/128 V _{CC}
0	0	0	0	1	0	5/128 V _{CC}
0	0	0	0	1	1	7/128 V _{CC}
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	1	123/128 V _{CC}
1	1	1	1	1	0	125/128 V _{CC}
1	1	1	1	1	1	127/128 V _{CC}

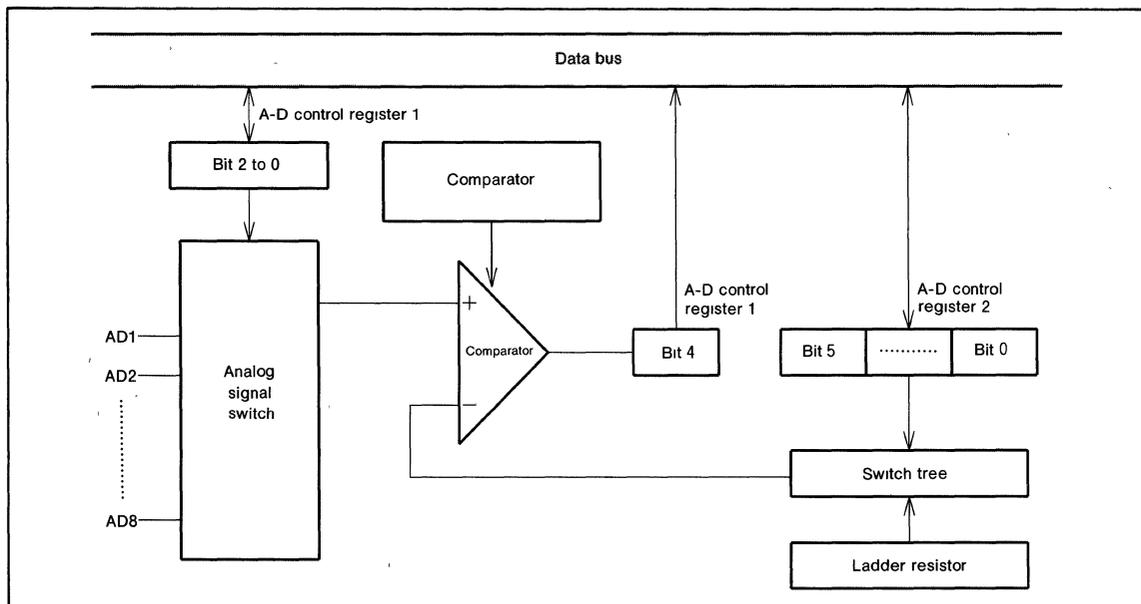


Fig. 24 Block diagram of A-D converter

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CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 4 outlines the CRT display functions of the M37204M8-XXXSP. The M37204M8-XXXSP incorporates a 24 columns X 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 254 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12 X 16 dot configuration to obtain smooth character patterns. (See Figure 25)

The following shows the procedure how to display characters on the CRT screen.

Table 4. Outline of CRT display functions

Parameter	Functions	
Display character	24 characters X 3 lines (maximum 16 lines)	
Character configuration	12 X 16 dots (See Figure 25)	
Kinds of characters	254 kinds	
Character size	4 kinds	
Color	Kind of colors	15 (max.)
	Coloring unit	a character
Extention display	Possible (multiple lines)	

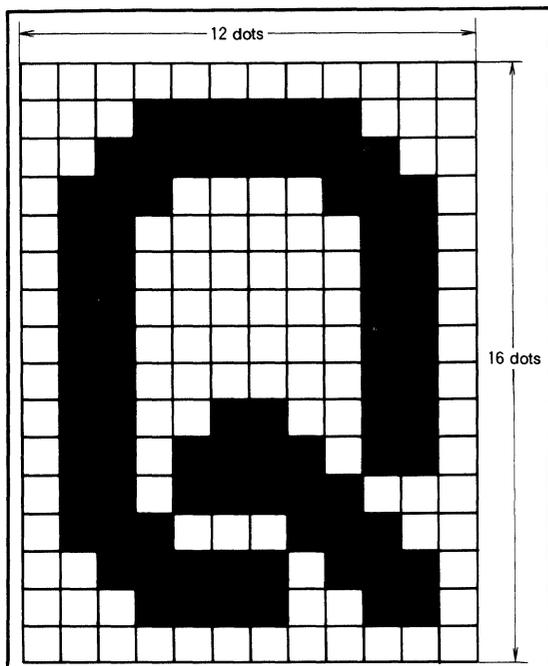


Fig. 25 CRT display character configuration

- ① Set the character to be displayed in display RAM.
- ② Set the display color by using the color register.
- ③ Specify the color register in which the display color is set by using the display RAM.
- ④ Specify the vertical position and character size by using the vertical position register and the character size register.
- ⑤ Specify the horizontal position by using the horizontal position register.
- ⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 26 shows the structure of the CRT control register 1. Figure 27 shows a block diagram of the CRT display control circuit.

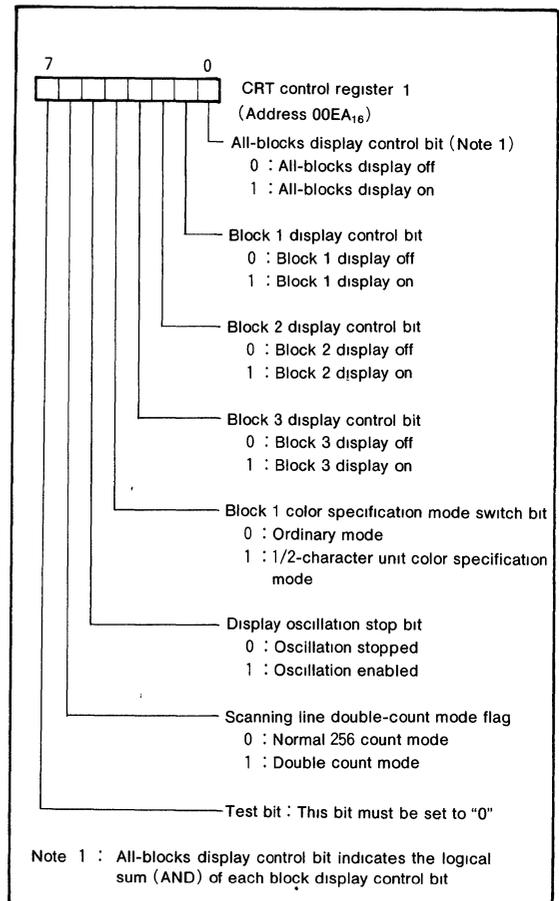


Fig. 26 Structure of CRT control register 1

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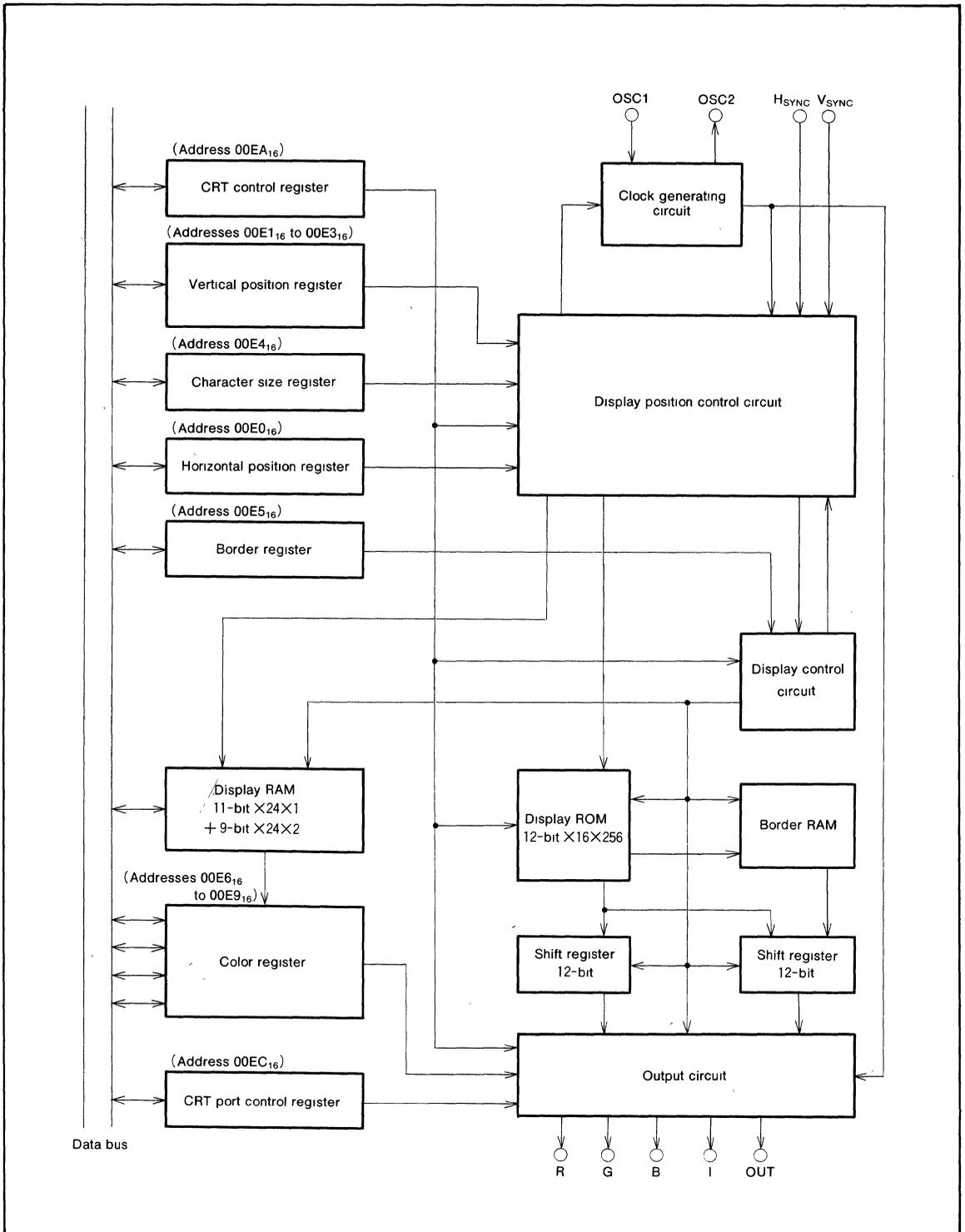


Fig. 27 Block diagram of CRT display control circuit

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(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 24 characters can be displayed in one block. (See (4) Display Memory.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of $4T_c$ (T_c = oscillation cycle for display).

The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 30), a block of the smaller block No. (1 to 3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 30), the former block is overridden and the latter is displayed.

The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values 00_{16} to $7F_{16}$ to bits 0 to 6 in the vertical position register (addresses $00E1_{16}$ to $00E3_{16}$). Figure 28 shows the structure of the vertical position register.

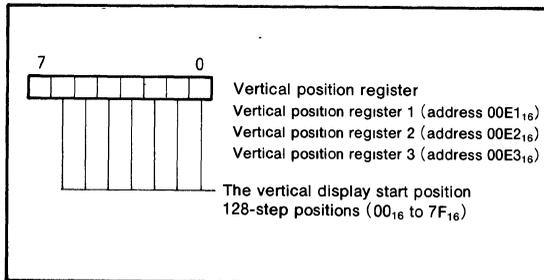


Fig. 28 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64-step display positions ($4T_c$ per step (T_c = oscillation cycle for display)) by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the horizontal position register (address $00E0_{16}$). Figure 29 shows the structure of the horizontal position register.

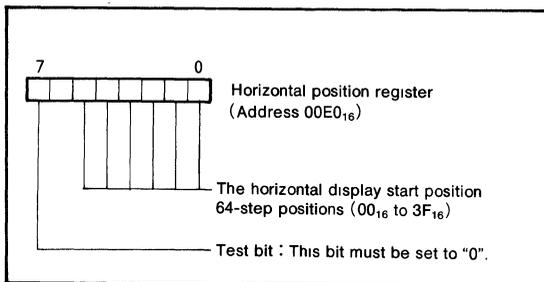
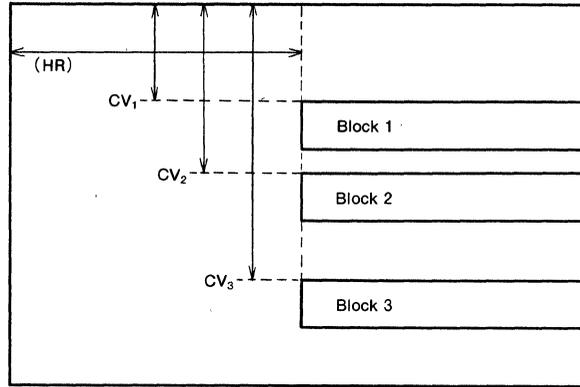
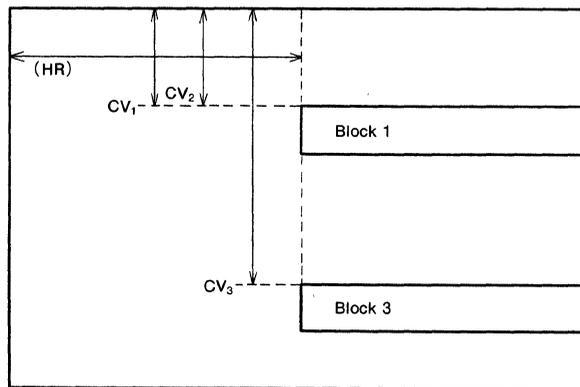


Fig. 29 Structure of horizontal position register

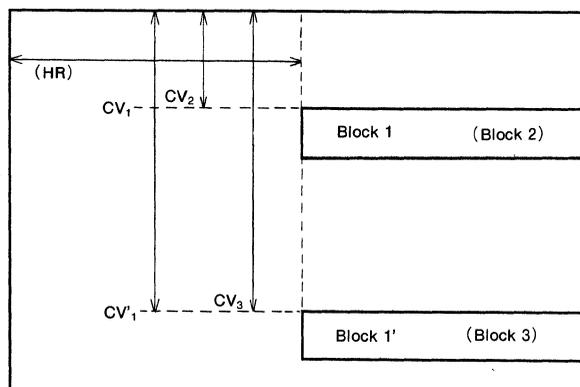
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(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed

Fig. 30 Display position

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(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the character size register (address 00E4₁₆) to set a character size. The character size in block 1 can be specified by using bits 0 and 1 in the character size register; the character size in block 2 can be specified by using bits 2 and 3; the character size in block 3 can be specified by using bits 4 and 5. Figure 31 shows the structure of the character size register.

The character size can be selected from four sizes: small size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation (=T_c) in the width (horizontal) direction. The small size consists of [one scanning line] × [1 T_c]; the medium size consists of [two scanning lines] × [2 T_c]; the large size consists of [three scanning lines] × [3 T_c]; and the extra large size consists of [four scanning lines] × [4 T_c]. Table 5 shows the relationship between the set values in the character size register and the character sizes.

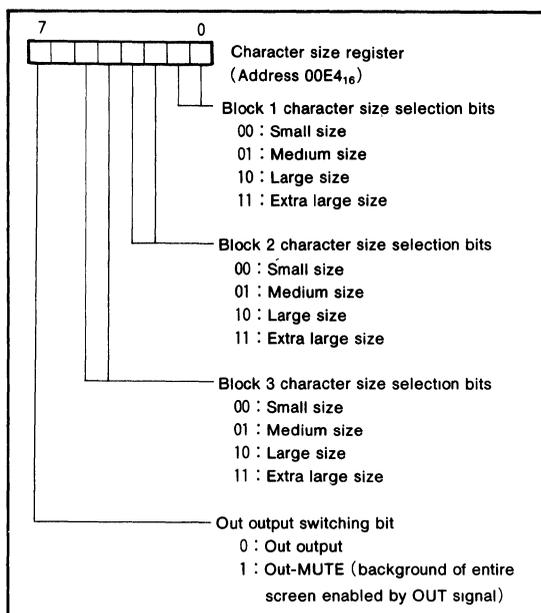


Fig. 31 Structure of character size register

Table 5. The relationship between the set values of the character size register and the character sizes

Set values of the character size register		Character size	Width (horizontal) direction T _c : a cycle of display oscillation	Height (vertical) direction (scanning lines)
CS _{n1}	CS _{n0}			
0	0	Small	1 T _c	1
0	1	Medium	2 T _c	2
1	0	Large	3 T _c	3
1	1	Extra large	4 T _c	4

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal start position is common to all blocks even when the character size varies with each block. (See Figure 32)

Abbreviations

CS_{n1}, CS_{n0} : Bits 1 and 0 of the character size register

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(4) Display Memory

There are two types of display memory: CRT display ROM (addresses 3000_{16} to $4FFF_{16}$) used to store character dot data (masked) and CRT display RAM (addresses 2000_{16} to $20D7_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① CRT display ROM (addresses 3000_{16} to $4FFF_{16}$)

The CRT display ROM contains dot pattern data for display characters. To display these stores characters in operation, specify character codes (codes determined based on the addresses in the CRT display ROM) that are specific to those characters, by writing them to the CRT display RAM.

Since the CRT display ROM contains 8K bytes and the data for one character takes up 32 bytes are required 256 characters can be stored. However, two-character space is required for test purposes, so in practice 254 characters can be stored for display.

Within the CRT display ROM area, data for part of each character that is [16 dots high] × [left hand 8 dots wide] is stored at addresses 3000_{16} to $37FF_{16}$ and 4000_{16} to $47FF_{16}$, and data for part of each character that is [16 dots high] × [right-side 4 dots wide] data of display characters are stored in addresses 3800_{16} to $3FFF_{16}$ and 4800_{16} to $4FFF_{16}$. (See Figure 33) However, note that the four upper bits in the data to be written to addresses 3800_{16} to $3FFF_{16}$ and 4800_{16} to $4FFF_{16}$ must all be set to "1" (by writing data $F0_{16}$ to FF_{16}).

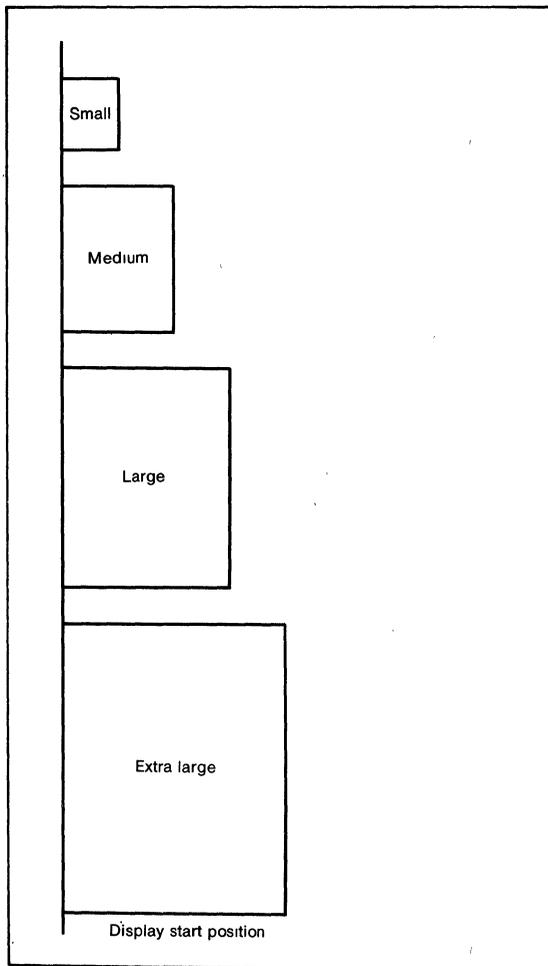


Fig. 32 Display start position of each character size (horizontal direction)

Table 6. Character code list

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00_{16}	3000_{16} to $300F_{16}$	3800_{16} to $380F_{16}$
01_{16}	3010_{16} to $301F_{16}$	3810_{16} to $381F_{16}$
02_{16}	3020_{16} to $302F_{16}$	3820_{16} to $382F_{16}$
03_{16}	3030_{16} to $303F_{16}$	3830_{16} to $383F_{16}$
:	:	:
$7E_{16}^*$	$37E0_{16}$ to $37EF_{16}$	$3FE0_{16}$ to $3FEF_{16}$
$7F_{16}^*$	$37F0_{16}$ to $37FF_{16}$	$3FF0_{16}$ to $3FFF_{16}$
80_{16}	4000_{16} to $400F_{16}$	4800_{16} to $480F_{16}$
81_{16}	4010_{16} to $401F_{16}$	4810_{16} to $481F_{16}$
:	:	:
FD_{16}	$47D0_{16}$ to $47DF_{16}$	$4FD0_{16}$ to $4FDF_{16}$
FE_{16}	$47E0_{16}$ to $47EF_{16}$	$4FE0_{16}$ to $4FEF_{16}$
FF_{16}	$47F0_{16}$ to $47FF_{16}$	$4FF0_{16}$ to $4FFF_{16}$

*For test pattern

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The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.

Assume that data for one character is stored at $3XX0_{16}$ to $3XXF_{16}$ and $4XX0_{16}$ to $4XXF_{16}$ (XX denotes 00_{16} to $7F_{16}$) and $3YY0_{16}$ to $3YYF_{16}$ and $4YY0_{16}$ to $4YYF_{16}$ (YY denotes 80_{16} to FF_{16}), then the character code for it is "XX₁₆".

In other words, character code for any given character is configured with two middle digits of the four-digit (hex-notated) addresses (3000_{16} to $37FF_{16}$ and 4000_{16} to $47FF_{16}$) where data for that character is stored.

Table 6 lists the character codes

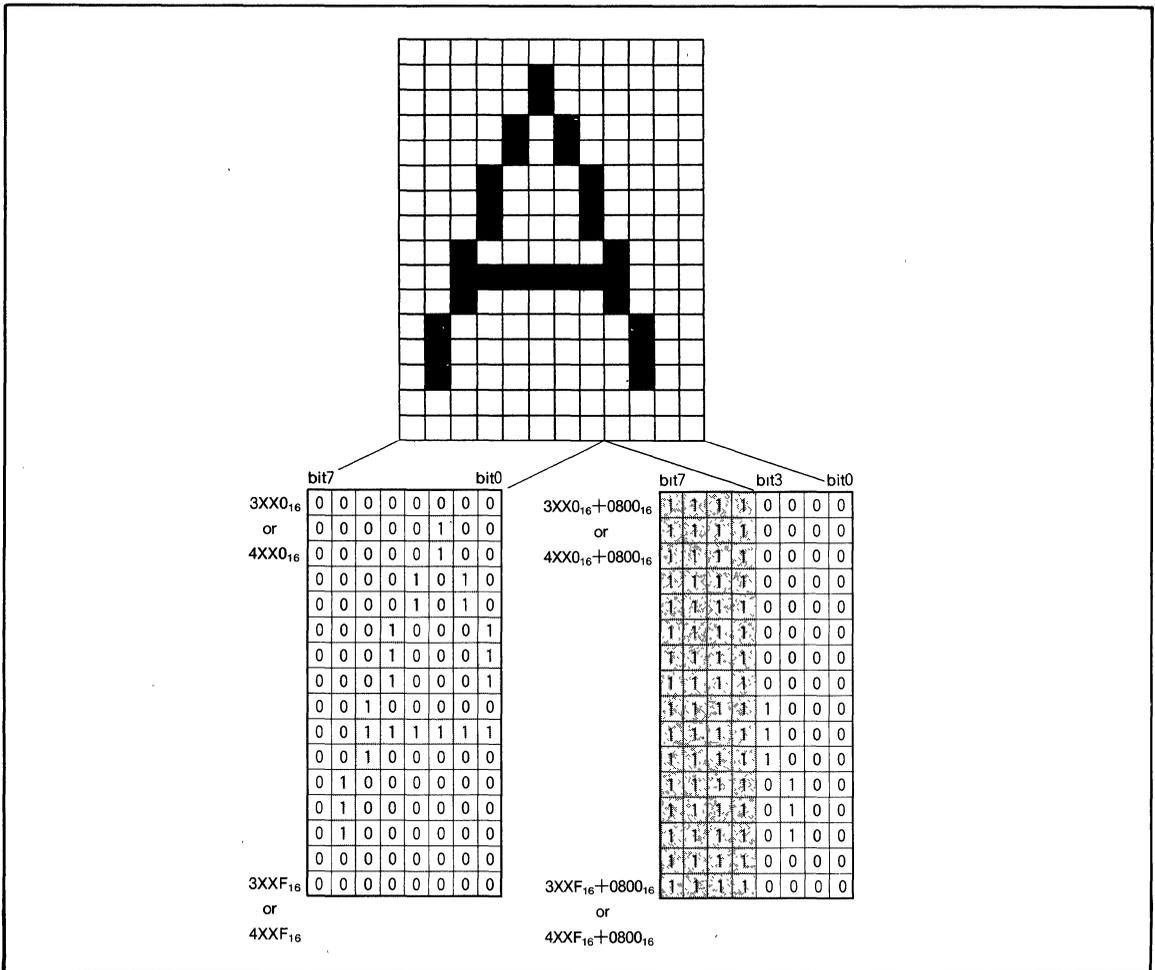


Fig. 33 Stored format for display characters

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② CRT display RAM (addresses 2000₁₆ to 20D7₁₆)

The CRT display RAM is allocated at addresses 2000₁₆ to 20D7₁₆, and is divided into a display character code specifying part and display color specifying part for each block.

Table 7 shows the contents of the CRT display RAM.

When a character is to be displayed at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the eight bits (bits 0 to 7) in address 2000₁₆ and the color register No. to the two low-order bits (bits 0 and 1) in address 2080₁₆. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 33. Write the character patterns at Table 8 and 9, when M37204M8-XXXSP is mask-ordered.

Table 7. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st column	2000 ₁₆	2080 ₁₆
	2nd column	2001 ₁₆	2081 ₁₆
	3rd column	2002 ₁₆	2082 ₁₆
	:	:	:
	22th column	2015 ₁₆	2095 ₁₆
	23th column	2016 ₁₆	2096 ₁₆
	24th column	2017 ₁₆	2097 ₁₆
Not used		2018 ₁₆ to 201F ₁₆	2098 ₁₆ to 209F ₁₆
Block 2	1st column	2020 ₁₆	20A0 ₁₆
	2nd column	2021 ₁₆	20A1 ₁₆
	3rd column	2022 ₁₆	20A2 ₁₆
	:	:	:
	22th column	2035 ₁₆	20B5 ₁₆
	23th column	2036 ₁₆	20B6 ₁₆
	24th column	2037 ₁₆	20B7 ₁₆
Not used		2038 ₁₆ to 203F ₁₆	20B8 ₁₆ to 20BF ₁₆
Block 3	1st column	2040 ₁₆	20C0 ₁₆
	2nd column	2041 ₁₆	20C1 ₁₆
	3rd column	2042 ₁₆	20C2 ₁₆
	:	:	:
	22th column	2055 ₁₆	20D5 ₁₆
	23th column	2056 ₁₆	20D6 ₁₆
	24th column	2057 ₁₆	20D7 ₁₆
Not used		2058 ₁₆ to 207F ₁₆	20D8 ₁₆ to 2FFF ₁₆

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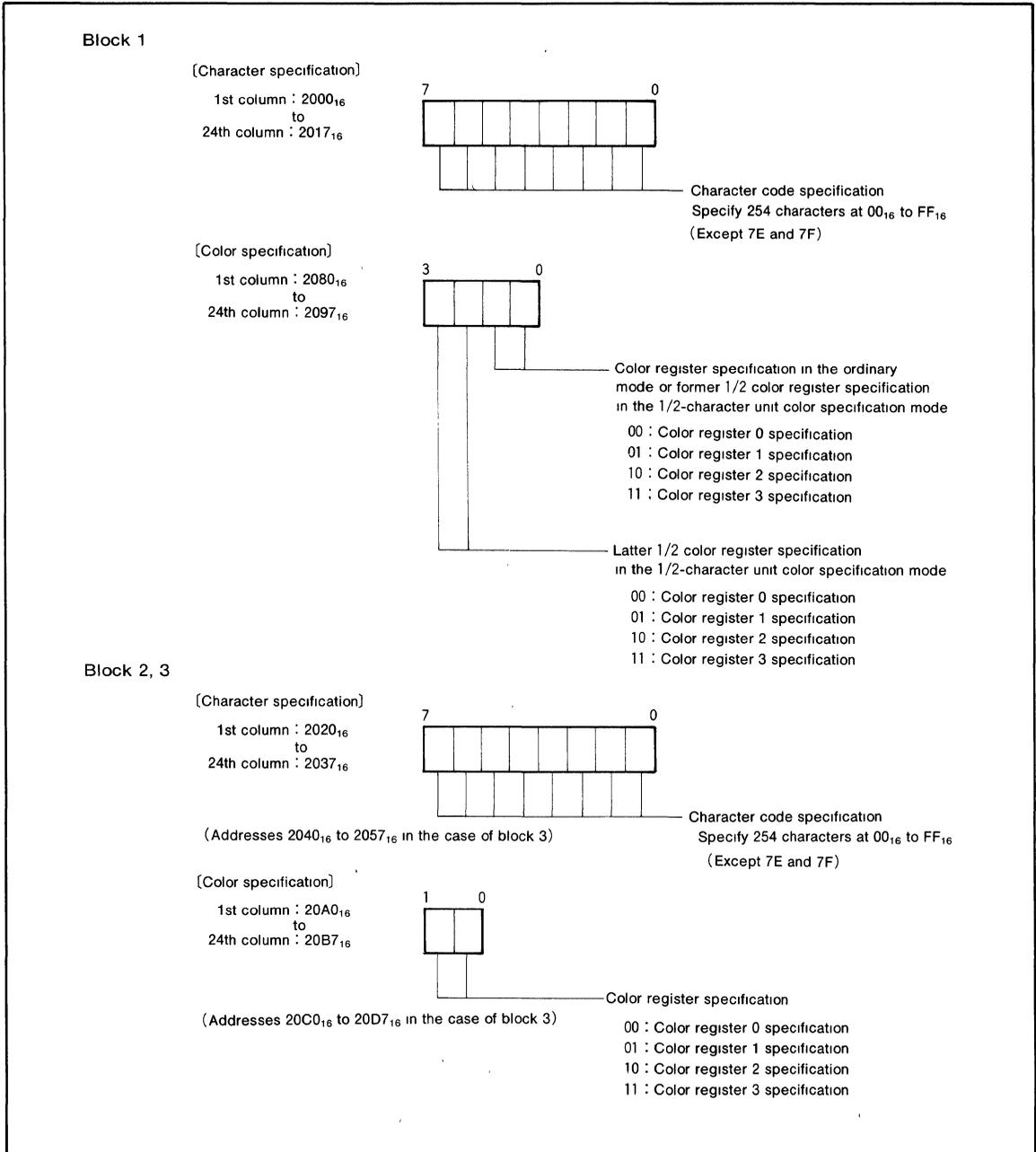


Fig. 34 Structure of the CRT display RAM

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Table 8. Test character patterns 1

Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

Table 9. Test character patterns 2

Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3: addresses 00E6₁₆ to 00E9₁₆) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set 2⁴-1 (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 35 shows the structure of the color register.

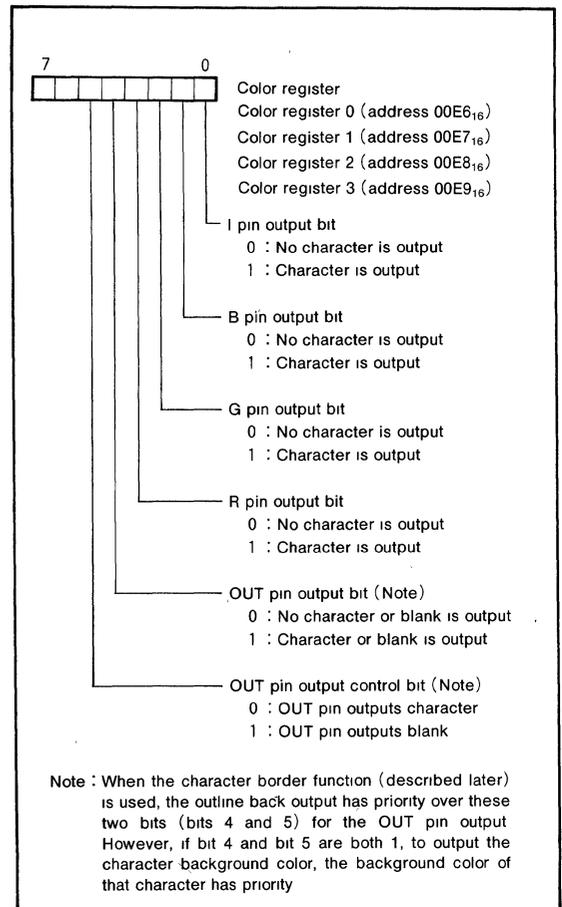


Fig. 35 Structure of color registers

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(6) 1/2-Character Unit Color Specification Mode

By setting "1" to bit 4 in the CRT control register 1 (address 00EA₁₆) it is possible to specify colors in units of a 1/2-character size (16 dots high×6 dots wide) for characters in block 1 only.

In the 1/2-character unit color specification mode, colors of display characters in block 1 are specified as follows:

- ① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080₁₆ to 2097₁₆).
- ② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080₁₆ to 2097₁₆).

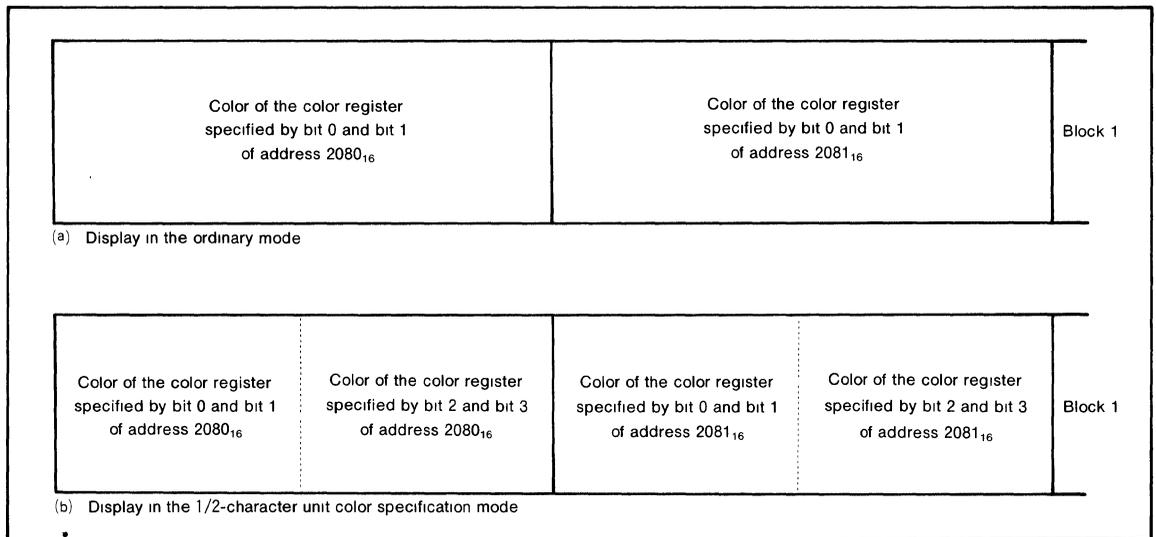


Fig. 36 Difference between ordinary color specification mode and 1/2-character unit color specification mode

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(8) Scanning Line Double Count Mode

One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended twofold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 256 steps from 00_{16} to FF_{16} , or four scanning lines per step, the number of steps in the scanning line double count mode is 128 from 00_{16} to $7F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 80_{16} to FF_{16} in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register 1 (address $00EA_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.

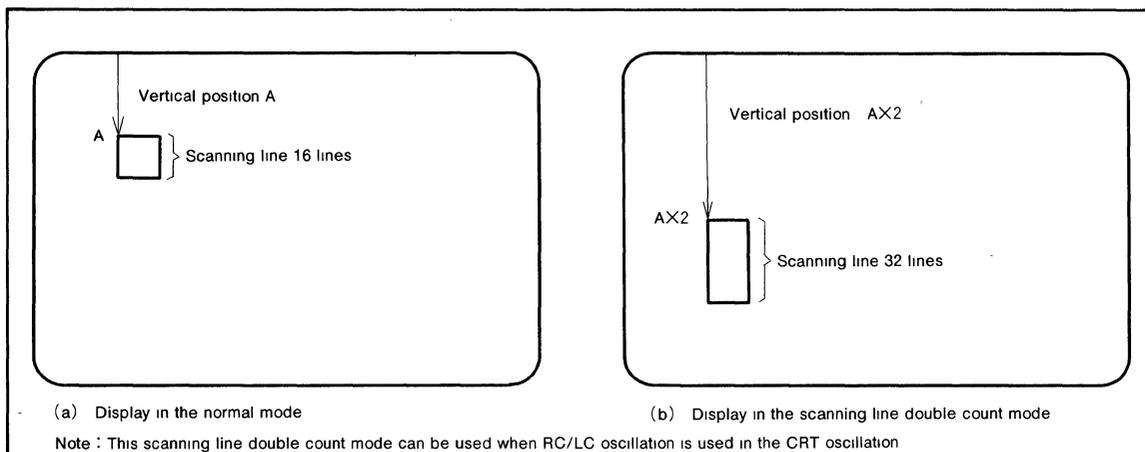


Fig. 39 Display in the normal mode and in the scanning line double count mode

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(9) Character Border Function

A one clock (one dot) border can be drawn around each character displayed, in both horizontal and vertical directions.

The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (the OUT pin output contents) are ignored, and the border output is from the OUT pin.

The border can be set in block units by the border selection register (address 00E5₁₆). The border output takes priority over OUT output of color register, but in case of character background coloring is set, the border output can't output. Table 10 shows the relationship between the values set in the border selection register and the character border function. Figure 41 shows the structure of the border selection register.

Table 10. The relationship between the value set in the border selection register and the character border function

Border selection register		Functions	Example of output
MDn1	MDn0		
X	0	Normal	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border excluding character	R, G, B, I output OUT output

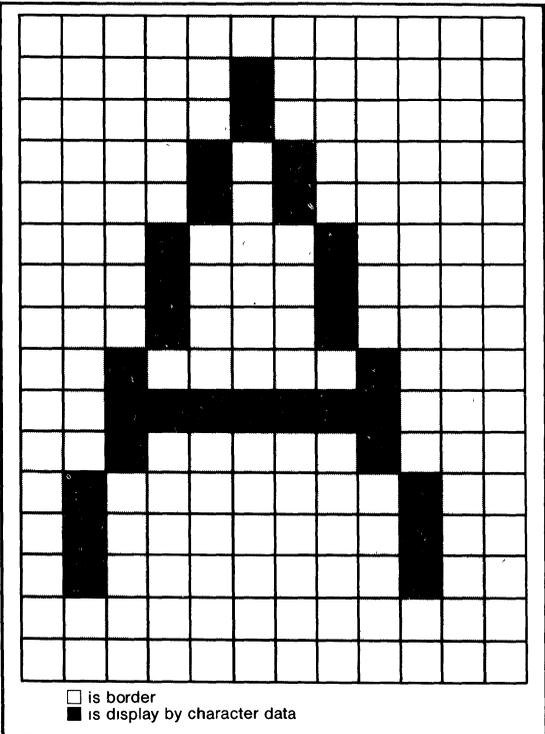


Fig. 40 Example of border

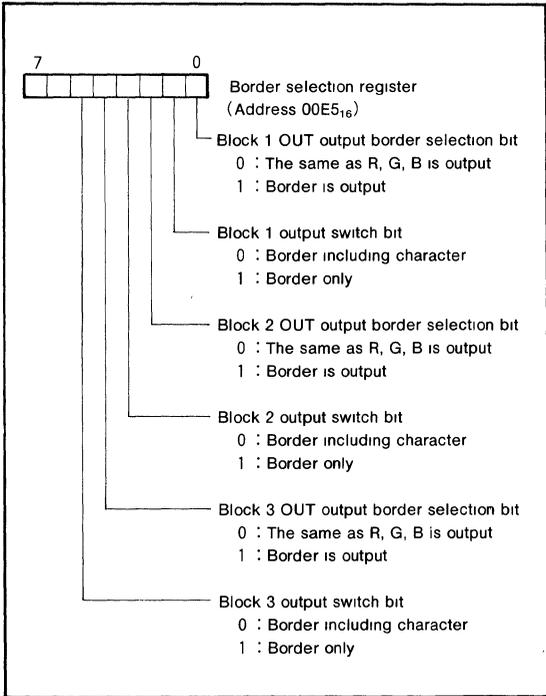


Fig. 41 Structure of border selection register

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(10) CRT Output Pin Control

CRT output pins R, G, B, I, and OUT are respectively shared with port P5₂, P5₃, P5₄, P5₅, and P5₆. When the corresponding bits in the port P5 direction register are cleared to "0", the pins are set for CRT output; when the bits are set to "1", the pins function as port P5 (general-purpose output pins).

The polarities of CRT outputs (R, G, B, I, and OUT, as well as H_{SYNC} and V_{SYNC}) can be specified by using the CRT port control register (address 00EC₁₆).

Use bits 0 to 4 in the CRT port control register to set the output polarities of H_{SYNC}, V_{SYNC}, R/G/B, I, and OUT. When these bits are cleared to "0", a positive polarity is selected;

when the bits are set to "1", a negative polarity is selected. Bits 5 to 7 in the CRT port control register, bit 0 in the CRT control register 2 (address 0208₁₆) and bit 7 in the character size register (address 00E4₁₆) are used to specify pin by pin whether normal video signals or R-MUTE, G-MUTE, B-MUTE, I-MUTE, OUT-MUTE and signals are output from each pin (R, G, B, I, OUT). When set for R-MUTE, G-MUTE, and B-MUTE outputs, the whole background colors of the screen become red, green, and blue. When set for I-MUTE and OUT-MUTE output, the whole background of the screen become I and OUT signal.

Figure 42 shows the structure of the CRT port control register.

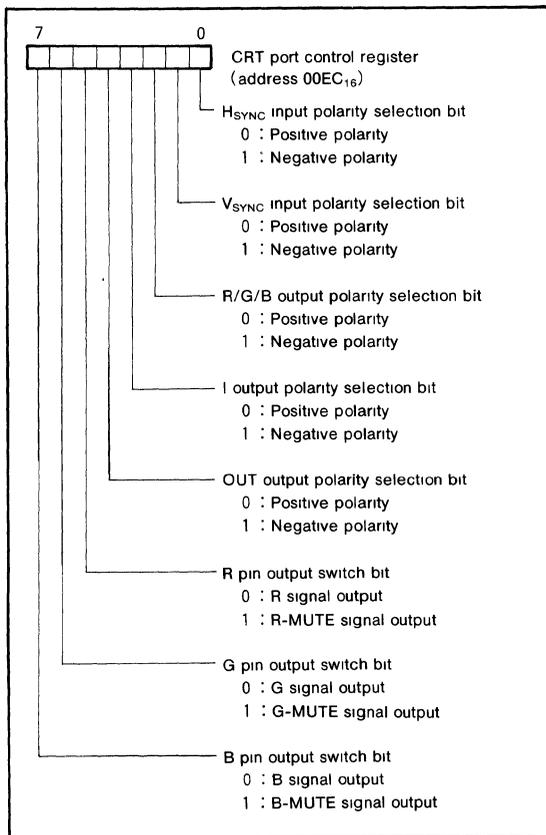


Fig. 42 Structure of CRT port control register

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The CRT can be operated by clocks from three different sources that can be selected with bits 0 and 1 of the CRT clock selection register (address 0209₁₆).

CRT clock selection register (address 0209 ₁₆)		CRT control register (address 00EA ₁₆)	CRT clock source
Bit 1	Bit 0	Bit 6	
0	0	0 or 1 (Either one OK)	Connects the RC/LC pin to the OSC1 and OSC2 pins, and supplies the clock produced by an RC/LC oscillation circuit to the CRT
0	1	0	Supplies the internal clock from OSC _{IN} and OSC _{OUT} (ceramic resonator) to the CRT The oscillation frequency is limited, so the lateral size of display characters is also limited. In this case, the OSC1 and OSC2 pins can be used for AD input or port input
1	0	—	Do not use this setting
1	1	1	If a CRT-dedicated ceramic resonator and a feedback resistor are connected to the OSC1 and OSC2 pins, the clock generated by the resultant oscillation is supplied to the CRT (another ceramic resonator in addition to the one connected to the OSC _{IN} and OSC _{OUT} pins of the microcomputer is necessary)

Fig. 43 CRT clock source and the values of CRT clock selection register and CRT control register

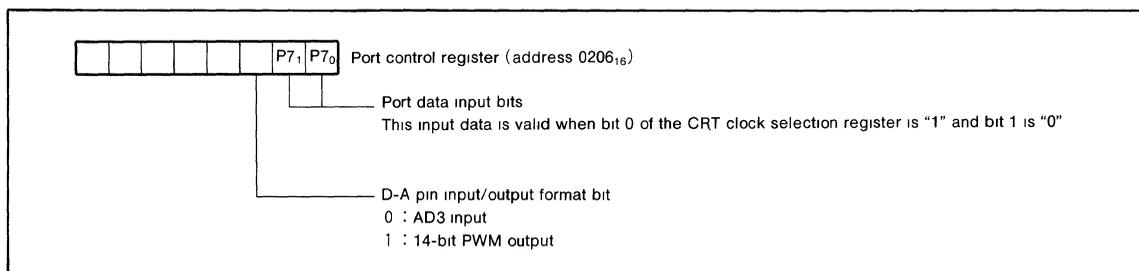


Fig. 44 Port control register

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(11) Character background coloring

The background part of a character (its 12×16 dot area) can be colored as specified by bits 4 and 5 of the color registers (addresses 00E6₁₆ to 00E9₁₆) and bits 2, 3, and 4 of the CRT control register 2 (address 0208₁₆).

Set "1" in bits 4 and 5 of the color register of the character whose background is to be colored, and specify the background color with bits 2, 3, and 4 of the CRT control register 2. This means that the color of the character is paired with the background color of that character, so that up to four color pairs can be used in each screen (eight background colors are possible).

The structure of the CRT control register 2 is shown in Figure 45.

Table 11. Coloring of character background by RGB output signals

CRT control register 2			RGB output
Bit 4 (B)	Bit 3 (G)	Bit 2 (R)	Color
0	0	0	Black
0	0	1	Red
0	1	0	Green
0	1	1	Yellow
1	0	0	Blue
1	0	1	Magenta
1	1	0	Cyan
1	1	1	White

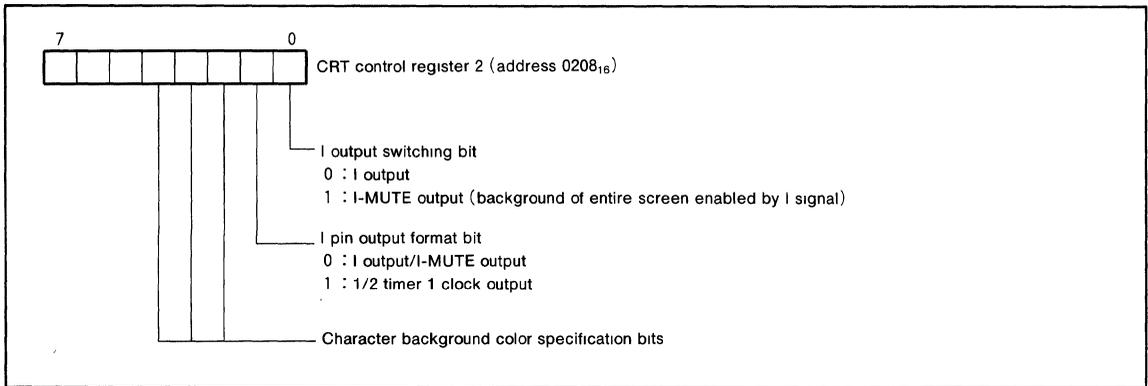


Fig. 45 Structure of CRT control register 2

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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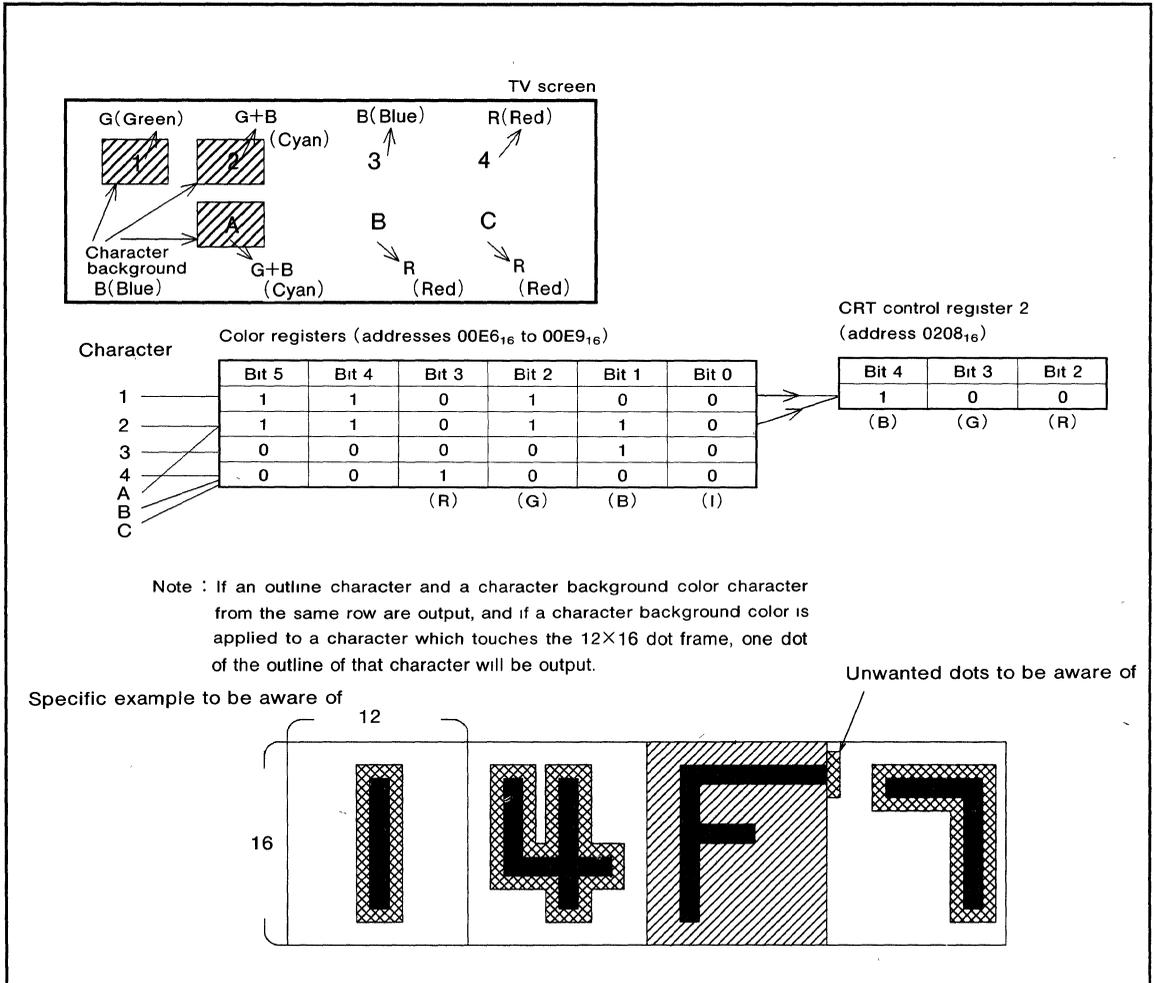


Fig. 46 Display example

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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(12) Scroll Function

① Scroll mode

The M37204M8-XXXSP allows the display area to be gradually expanded or shrunk in the vertically direction in units of 1H (H: H_{SYNC} signal). There are three modes for this scroll method. Each mode has DOWN and UP modes, providing a total of six modes.

Table 13 shows the contents of each scroll mode.

② Scroll speed

The scroll speed is determined by the vertical synchronization (V_{SYNC}) signal. For the NTSC interlace method, assuming that

$$V = 16.7\text{ms} \quad 262.5 \text{ H}_{\text{SYNC}} \text{ signals per screen}$$

we obtain the scroll speed as shown in Table 14.

Scroll resolution varies with each scroll mode. In mode 1 and mode 2, one of three resolutions (1H, 2H, 4H) can be selected. In mode 3, scroll is done in units of 4H alone.

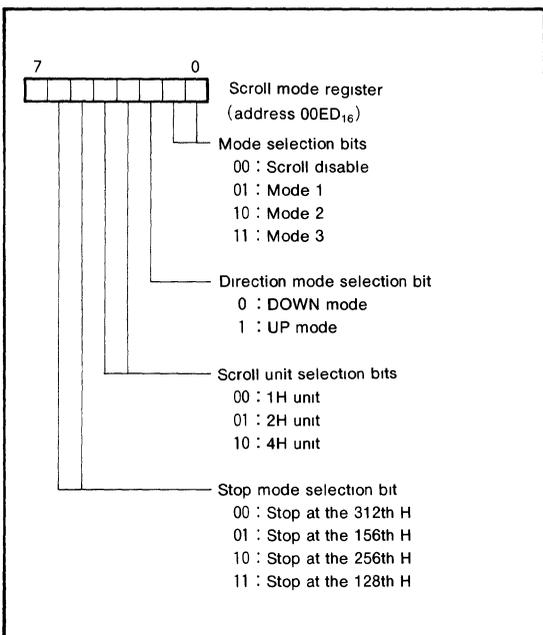


Fig. 47 Structure of scroll mode register

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Table 12. Scroll operation in each mode and the values of scroll mode register

Mode		Scroll operation	Scroll mode register			
			Bit 2	Bit 1	Bit 0	
1	DOWN	Appear from upper side		0	0	1
	UP	Erase from lower side		1	0	1
2	DOWN	Erase from upper side		0	1	0
	UP	Appear from lower side		1	1	0
3	DOWN	Erase from both upper and lower side		0	1	1
	UP	Appear to both upper and lower side		1	1	1

Table 13. Scroll speed

Scroll resolution	Scroll speed (in all picture)
1 H unit	$16.7 \text{ (ms)} \times 262.5 \div 1 \approx 4 \text{ (s)}$
2 H unit	$16.7 \text{ (ms)} \times 262.5 \div 2 \approx 2 \text{ (s)}$
4 H unit	$16.7 \text{ (ms)} \times 262.5 \div 4 \approx 1 \text{ (s)}$

Table 14. Scroll mode and scroll resolution

Mode	Scroll resolution	Scroll speed
Mode 1	1 H Unit	about 4 second
	2 H Unit	about 2 second
Mode 2	4 H Unit	about 1 second
	4 H Unit	about 1 second

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**INTERRUPT INTERVAL DETERMINATION
FUNCTION**

The M37204M8-XXXSP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary counter as shown in Figure 48. Using this counter, it determines a duration of time from the rising transition (falling transition) of an input signal pulse on the INT1 or INT2 to the rising transition (falling transition) of the signal pulse that is input next.

The following describes how the interrupt interval is determined.

1. The interrupt input to be determined (INT1 input or INT2 input) is selected by using bit 2 in the interrupt interval determination control register (address 00D8₁₆). When this bit is cleared to "0", the INT1 input is selected; when the bit is set to "1", the INT2 input is selected.
2. When the INT1 input is to be determined, the polarity is selected by using bit 3 in the interrupt interval determination control register; when the INT2 input is to be determined, the polarity is selected by using bit 4 in the interrupt interval determination control register. When the relevant bit is cleared to "0", determination is made of the interval of a positive polarity (rising

transition); when the bit is set to "1", determination is made of the interval of a negative polarity (falling transition).

3. The reference clock is selected by using bit 1 in the interrupt interval determination control register. When the bit is cleared to "0", a 64 μ s clock is selected; when the bit is set to "1", a 32 μ s clock is selected (based on an oscillation frequency of 4MHz in either case).
4. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT1 pin (or INT2 pin), the 8-bit binary counter starts counting up with the selected reference clock (64 μ s or 32 μ s).
5. Simultaneously with the next input pulse, the value of the 8-bit binary counter is loaded into the determination register (address 00D7₁₆) and the counter is immediately reset (00₁₆). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "00₁₆".
6. When count value "FE₁₆" is reached, the 8-bit binary counter stops counting. Then, simultaneously when the reference clock is input next, the counter sets value "FF₁₆" to the determination register.

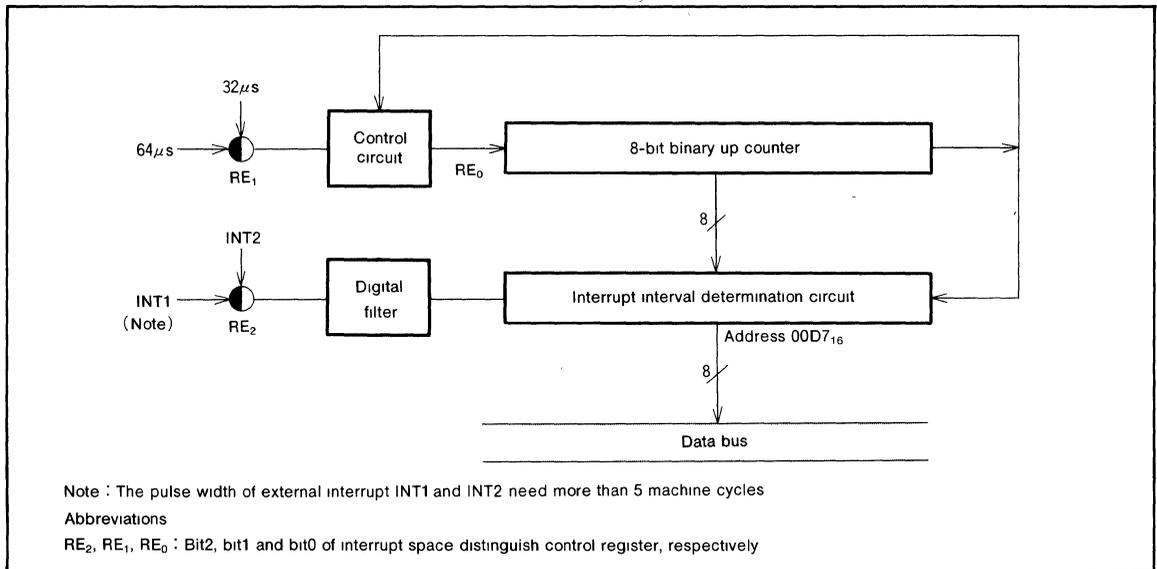


Fig. 48 Block diagram of interrupt interval determination circuit

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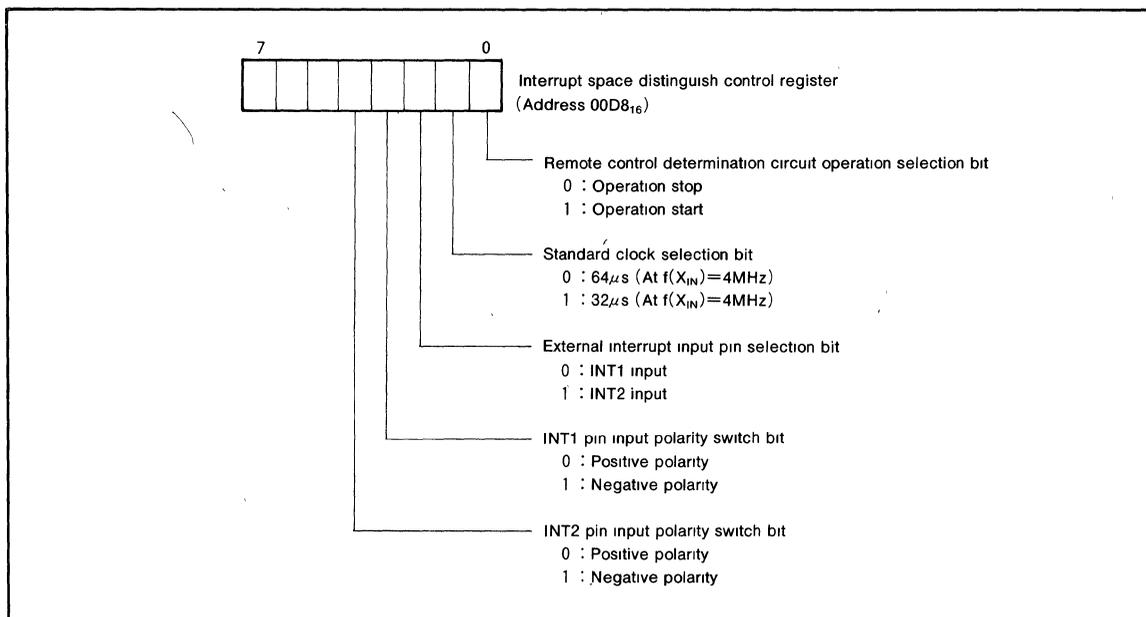


Fig. 49 Structure of interrupt space distinguish control register

RUNAWAY DETECTION FUNCTION

The M37204M8-XXXSP has a decode function for undefined instructions, to detect runaway.

If an opcode that is not defined in the instruction codes is input to the CPU, this function generates an undefined instruction decode signal from the CPU, the generation of this signal activates an internal reset, and the program restarts from the reset vector.

If the microcomputer is in single-chip mode and bit 4 of the CPU mode register is "0" ($CM_0=CM_1=CM_4=0$), the ϕ output pin is switched to reset output to post the generation of the reset to the outside as well.

Note that this function cannot be disabled.

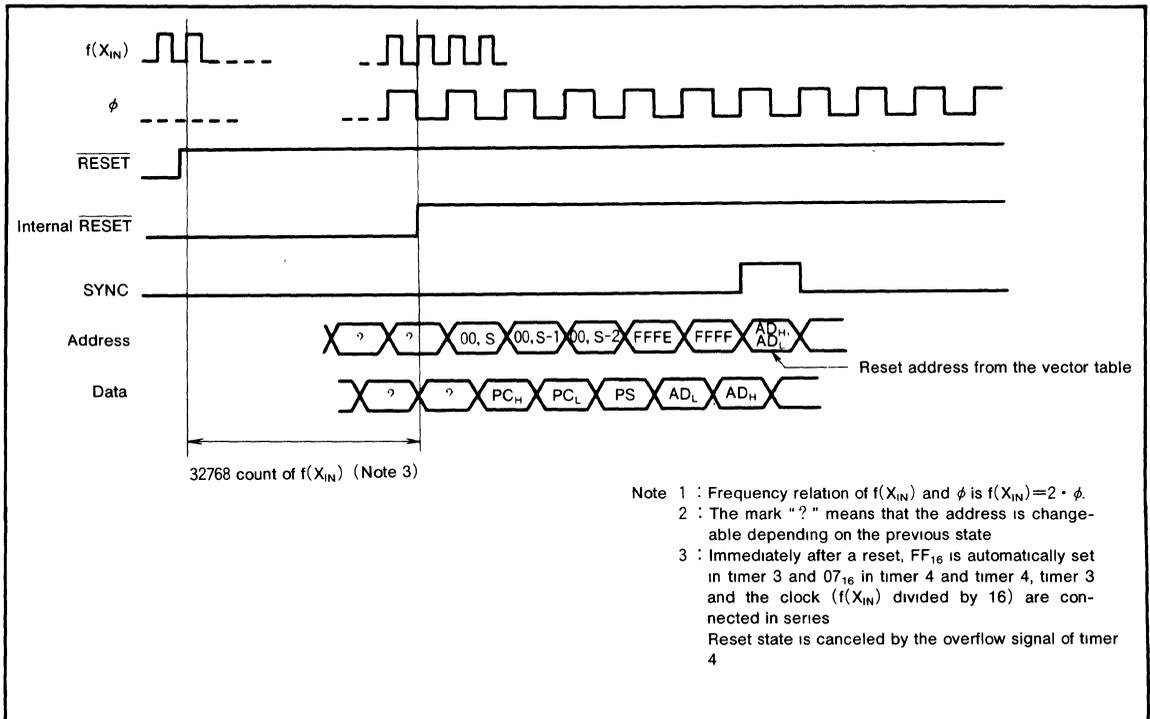
**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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RESET CIRCUIT

The M37204M8-XXXSP is reset according to the sequence shown in Figure 50. It starts the program from the address formed by using the content of address FFF_{16} as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the RESET pin is held at "L" level for no less than $2\mu s$ while the power voltage is $5V \pm 10\%$

and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 51.

An example of the reset circuit is shown in Figure 52. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.



- Note 1 : Frequency relation of f(X_{IN}) and φ is f(X_{IN})=2 · φ.
- Note 2 : The mark "?" means that the address is changeable depending on the previous state
- Note 3 : Immediately after a reset, FF₁₆ is automatically set in timer 3 and 07₁₆ in timer 4 and timer 4, timer 3 and the clock (f(X_{IN}) divided by 16) are connected in series
Reset state is canceled by the overflow signal of timer 4

Fig. 50 Timing diagram at reset

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	Address	
(1) Port P0 direction register	(00C1) ₁₆	00 ₁₆
(2) Port P1 direction register	(00C3) ₁₆	00 ₁₆
(3) Port P2 direction register	(00C5) ₁₆	00 ₁₆
(4) Port P3 direction register	(00C7) ₁₆	00000000
(5) Port P4 direction register	(00C9) ₁₆	00 ₁₆
(6) Port P5 direction register	(00CB) ₁₆	00000000
(7) Port P6 direction register	(00CD) ₁₆	00 ₁₆
(8) PWM output control register 1	(00D5) ₁₆	00 ₁₆
(9) PWM output control register 2	(00D6) ₁₆	00000000
(10) Interrupt space distinguish register	(00D7) ₁₆	00 ₁₆
(11) Interrupt space distinguish control register	(00D8) ₁₆	00 ₁₆
(12) Special mode register 1	(00DA) ₁₆	00 ₁₆
(13) Special mode register 2	(00DB) ₁₆	00 ₁₆
(14) Serial I/O1 mode register	(00DC) ₁₆	00000000
(15) Serial I/O2 mode register	(00DE) ₁₆	00000000
(16) Horizontal position register	(00E0) ₁₆	00000000
(17) Color register 0	(00E6) ₁₆	00000000
(18) Color register 1	(00E7) ₁₆	00000000
(19) Color register 2	(00E8) ₁₆	00000000
(20) Color register 3	(00E9) ₁₆	00000000
(21) CRT control register	(00EA) ₁₆	00 ₁₆
(22) Display block counter	(00EB) ₁₆	00000000
(23) CRT port control register	(00EC) ₁₆	00 ₁₆
(24) Scroll control register	(00ED) ₁₆	00000000
(25) A-D control register 1	(00EF) ₁₆	00000000
(26) Timer 1	(00F0) ₁₆	FF ₁₆
(27) Timer 2	(00F1) ₁₆	07 ₁₆
(28) Timer 3	(00F2) ₁₆	FF ₁₆
(29) Timer 4	(00F3) ₁₆	07 ₁₆
(30) Timer 12 mode register	(00F4) ₁₆	00000000
(31) Timer 34 mode register	(00F5) ₁₆	00000000
(32) CPU mode register	(00FB) ₁₆	11111000
(33) Interrupt request register 1	(00FC) ₁₆	00000000
(34) Interrupt request register 2	(00FD) ₁₆	00000000
(35) Interrupt control register 1	(00FE) ₁₆	00000000
(36) Interrupt control register 2	(00FF) ₁₆	00000000
(37) Port control register	(0206) ₁₆	00
(38) Shift register input control register	(0207) ₁₆	00
(39) CRT control register2	(0208) ₁₆	00
(40) CRT clock selection register	(0209) ₁₆	00
(41) Processor status register (P S)		1
(42) Program counter (P C _H)	Contents of address FFF ₁₆	
	(P C _L)	Contents of address FFE ₁₆

Note . Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values
At reset, "0" is read from all bits which is not used

Fig. 51 Internal state of microcomputer at reset

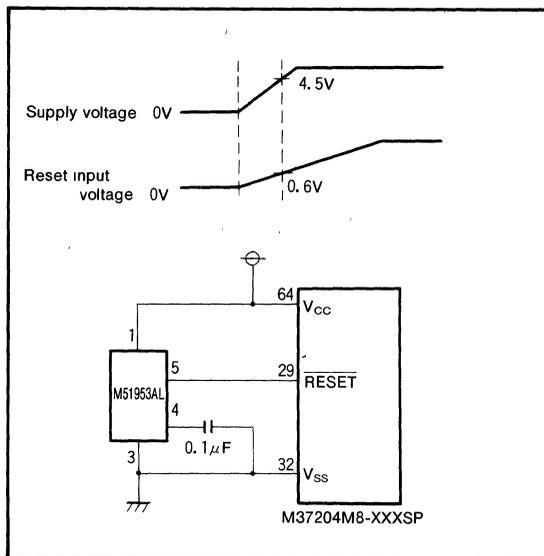


Fig. 52 Example of reset circuit

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 3), port P0 can be accessed at zero page memory address 00C0₁₆.

Port P0 has a direction register (address 00C1₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address 00FB₁₆), three different modes can be selected; single-chip mode, memory expansion mode and microprocessor mode.

In these modes it functions as address (A₇—A₀) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A₁₅—A₈) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data (D₀—D₇) input/output port. Refer to the section on processor modes for details.

(4) Port P3

Port P3 is a 7-bit I/O port with function similar to port P0, but the output structure of P₃₀, P₃₁ is CMOS output and P₃₂—P₃₆ is N-channel open drain.

P₃₂, P₃₃ are in common with the external clock input pins of timer 2 and 3.

P₃₄, P₃₆ are in common with the external interrupt input pins INT1, INT2 and P₃₂, P₃₅, P₃₆ with the analog input pins of A-D converter A-D6, A-D1, A-D2.

In the microprocessor mode or the memory expansion mode, P₃₀, P₃₁ works as R/ \overline{W} signal output pin and SYNC signal output pin respectively.

(5) Port P4

Port P4 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

All pins have program selectable dual functions. When a serial I/O1 function is selected, P₄₀—P₄₃ work as input/output pins of serial I/O1. When a serial I/O2 function is selected, P₄₄—P₄₇ work as input/output pins of serial I/O2.

In the special serial I/O mode, P₄₄, P₄₅ work as SDA, SCL pins. P₄₆, P₄₇ are in common with PWM9 and 8 output pins.

(6) OSC1, OSC2 pins

Clock input/output pins for CRT display function.

OSC1, OSC2 are in common with the analog input pins of A-D converter A-D4, A-D5.

OSC1, OSC2 are in common with the input port P7₀, P7₁.

(7) H_{SYNC}, V_{SYNC} pins

H_{SYNC} is a horizontal synchronizing signal input pin for CRT display

V_{SYNC} is a vertical synchronizing signal input pin for CRT display.

(8) R, G, B, I, OUT pins

This is a 5-bit output pin for CRT display and in common with P₅₂—P₅₆.

(9) Port P6

Port P6 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

This port is in common with 8-bit PWM output pin PWM0—PWM7.

(10) D-A pin

This is a 14-bit PWM output pin.

(11) ϕ pin

The internal system clock (1/2 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

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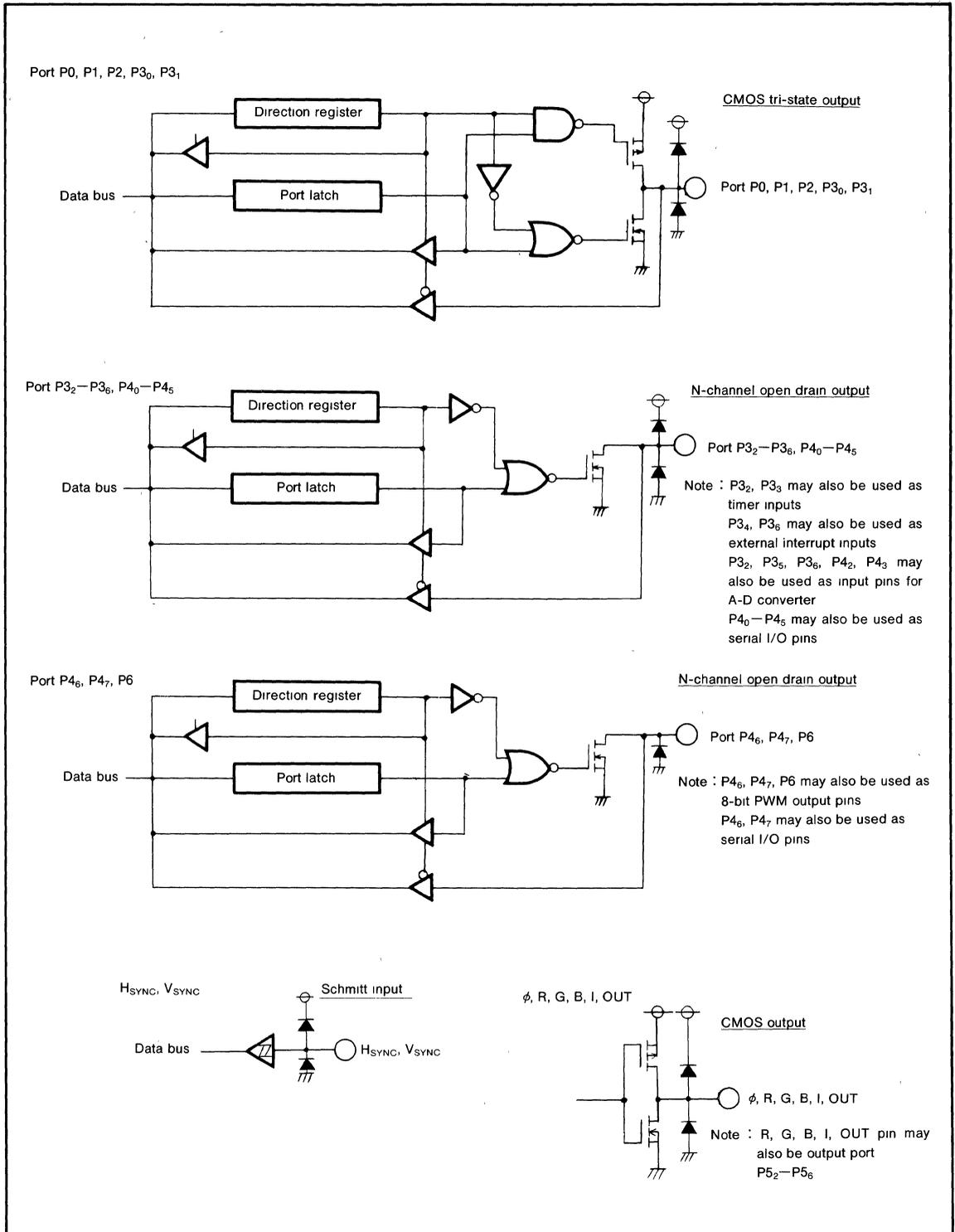


Fig. 53 Block diagram of ports P0-P6 (single-chip mode) and output format of ϕ , R, G, B, I, OUT

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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PROCESSOR MODE

By changing the contents of the processor mode bits (bit 0 and 1 at address 00FB₁₆), three different operation modes can be selected; single-chip mode, memory expansion mode, and microprocessor mode.

In the memory expansion mode and the microprocessor mode, ports P0—P3 can be used as address, and data input/output pins.

Figure 55 shows the functions of ports P0—P3.

The memory map for the single-chip mode is shown in Figure 2 and for other modes, in Figure 54.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the M37204M8-XXXSP into memory expansion mode.

The three different modes are explained as follows:

- (1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0—P3 will work as I/O ports.

- (2) Memory expansion mode [01]

The microcomputer will be placed in the memory expansion mode after connecting CNV_{SS} to V_{CC} and initiating a reset or connecting CNV_{SS} to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and its I/O port function is lost.

Port P2 becomes the data bus of D₇—D₀ (including instruction code) and loses its I/O port function. Port P3₀ and P3₁ works as R/ \bar{W} and ϕ .

- (3) Microprocessor mode [10]

When CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "10", the microcomputer will automatically default to microprocessor mode. In this mode, the internal ROM is inhibited so the external memory is required. Other functions are same as the memory expansion mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 14.

Note : Use the M37204M8-XXXSP in the microprocessor mode or the memory expansion mode only at program development.
The standards is assured only in the single-chip mode.

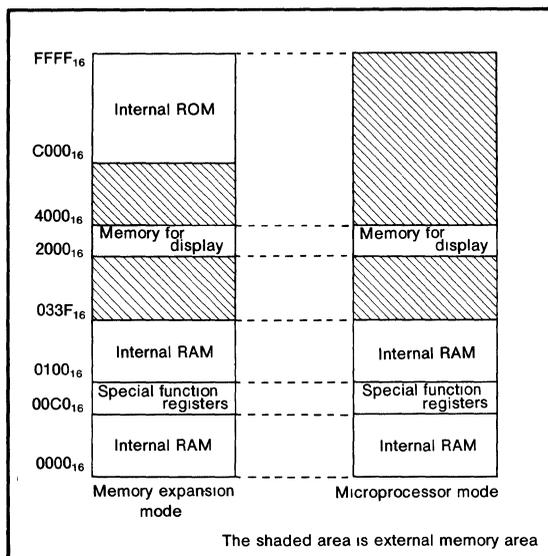


Fig. 54 External memory area at each processor mode

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Port	CM ₁	0	0	1
	CM ₀	0	1	0
Mode		Single-chip mode	Memory expansion mode	Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P3			Same as left	

Fig. 55 Processor mode and function of ports P0-P3 (CM₁, CM₀ : Bit 1 and bit 0 of CPU mode register)

Table 15. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode • Memory expansion mode • Microprocessor mode 	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V _{CC}	<ul style="list-style-type: none"> • Memory expansion mode 	The memory expansion mode is set by the reset.

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 58.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timer 3 and timer 4 are connected automatically and FF_{16} is set in the timer 3, 07_{16} is set in the timer 4, and timer 3 count source is forced to $f(X_{IN})$ divided by 16. This connection is cleared when an external interrupt is accepted or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 56.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 57
 X_{IN} is the input, and X_{OUT} is open.

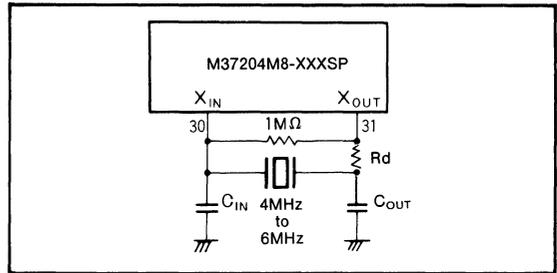


Fig. 56 External ceramic resonator circuit

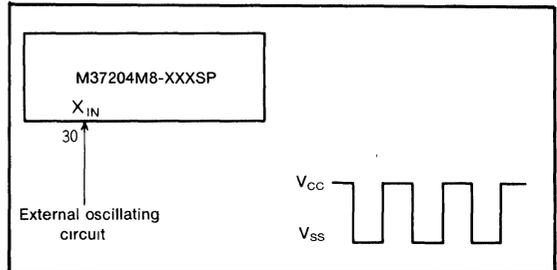


Fig. 57 External clock input circuit

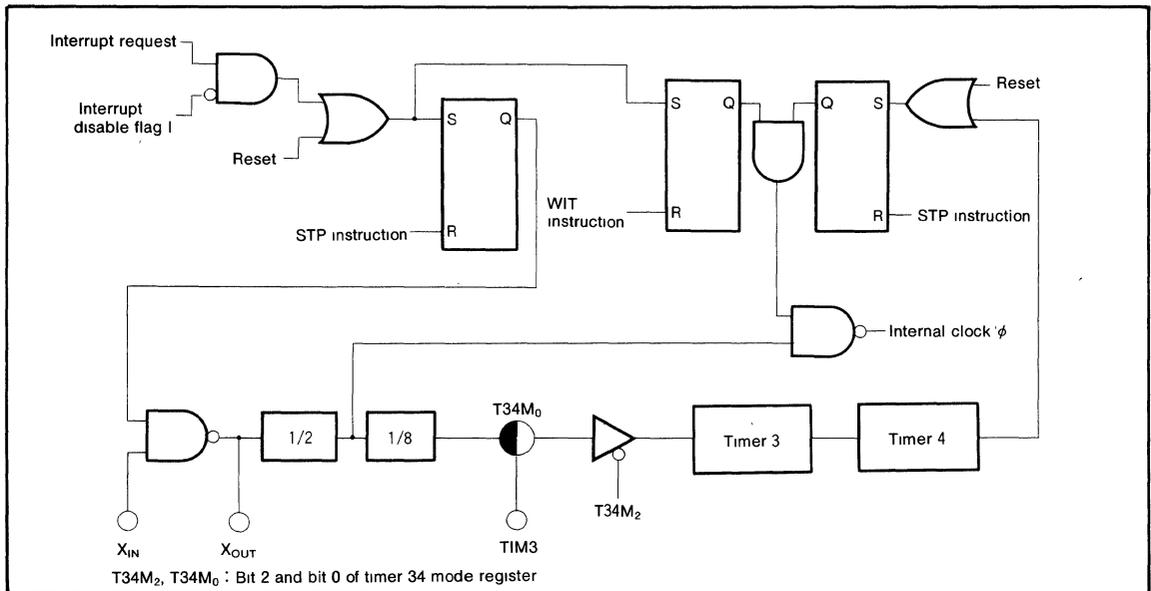


Fig. 58 Block diagram of clock generating circuit

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
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DISPLAY OSCILLATION CIRCUIT

The CRT display clock oscillation circuit has built-in RC oscillation circuits, so that a clock can be obtained simply by connecting an RC circuit between the OSC1 and OSC2 pins.

An internal clock can also be used as the CRT display clock, in which case the OSC1 and OSC2 pins can be used as P7₀, P7₁, AD₄, and AD₅ input pins.

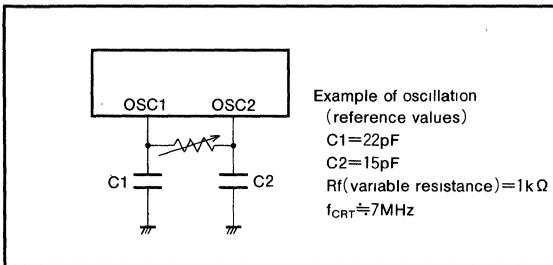


Fig. 59 Display oscillation circuit

AUTO CLEAR CIRCUIT

When power is supplied, the auto-clear function can be performed by connecting the following circuit to reset pin.

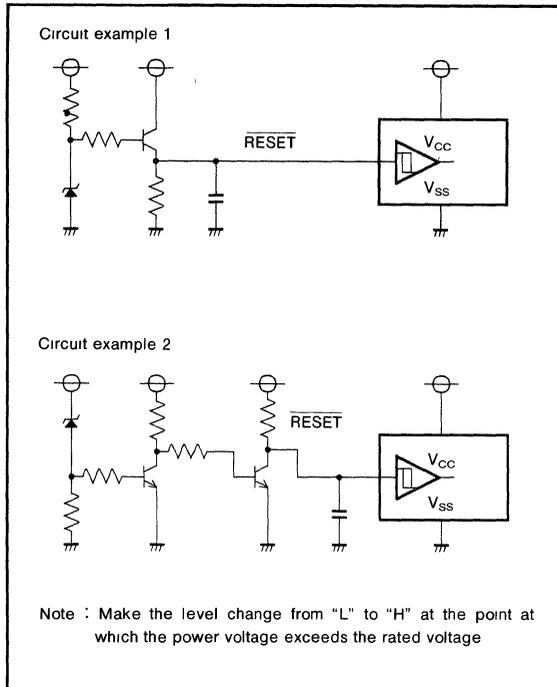


Fig. 60 Auto clear circuit example

PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instruction are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (4) An NOP instruction must be used after the execution of a PLP instruction.
- (5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders

- (1) mask ROM order confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3 sets

MITSUBISHI MICROCOMPUTERS
M37204M8-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS} Output transistors are at "off" state	-0.3 to 6	V
V _I	Input voltage CNV _{SS}		-0.3 to 6	V
V _I	Input voltage P ₀ -P ₀₇ , P ₁ ₀ -P ₁₇ , P ₂ ₀ -P ₂₇ , P ₃ ₀ -P ₃₆ , P ₄ ₀ -P ₄₇ , P ₆ ₀ -P ₆₇ , P ₇ ₀ -P ₇₇ , A-D1-A-D8 H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1		-0.3 to V _{CC} +0.3	V
V _O	Output voltage P ₀ ₀ -P ₀₇ , P ₁ ₀ -P ₁₇ , P ₂ ₀ -P ₂₇ , P ₃ ₀ -P ₃₆ , P ₄ ₀ -P ₄₅ , R, G, B, I, OUT, D-A, X _{OUT} , OSC2		-0.3 to V _{CC} +0.3	V
V _O	Output voltage P ₄ ₆ , P ₄₇ , P ₆ ₀ -P ₆₇		-0.3 to 13	V
I _{OH}	Circuit current R, G, B, I, OUT, P ₀ ₀ -P ₀₇ , P ₁ ₀ -P ₁₇ , P ₂ ₀ -P ₂₃ , P ₃ ₀ , P ₃₁ , D-A		0 to 1 (Note 1)	mA
I _{OL1}	Circuit current R, G, B, I, OUT, P ₀ ₀ -P ₀₇ , P ₁ ₀ -P ₁₇ , P ₂ ₀ -P ₂₃ , P ₃ ₀ -P ₃₆ , P ₄ ₀ -P ₄₃ , D-A		0 to 2 (Note 2)	mA
I _{OL2}	Circuit current P ₆ ₀ -P ₆₇ , P ₄ ₆ , P ₄₇		0 to 1 (Note 2)	mA
I _{OL3}	Circuit current P ₂ ₄ -P ₂₇		0 to 10 (Note 3)	mA
I _{OL4}	Circuit current P ₄ ₄ , P ₄₅		0 to 3 (Note 3)	mA
P _d	Power dissipation	T _a =25°C	550	mW
T _{opr}	Operating temperature		-10 to 70	°C
T _{stg}	Storage temperature		-40 to 125	°C

- Note 1 : The total current that flows out of the IC should be 20mA (max)
 2 : The total of I_{OL1}, I_{OL2} and I_{OL4} should be 30mA (max)
 3 : The total of I_{OL} of port P₂₄-P₂₇ should be 20mA (max)

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=-10 to 70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ.	Max	
V _{CC}	Supply voltage (Note 4) During the CPU and CRT operation	4.5	5.0	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	"H" input voltage P ₀ ₀ -P ₀₇ , P ₁ ₀ -P ₁₇ , P ₂ ₀ -P ₂₇ , P ₃ ₀ -P ₃₆ , P ₄ ₀ -P ₄₃ , P ₄ ₆ , P ₄₇ , P ₆ ₀ -P ₆₇ , P ₇ ₀ , P ₇₁ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₄ ₄ , P ₄₅	0.7V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀ ₀ -P ₀₇ , P ₁ ₀ -P ₁₇ , P ₂ ₀ -P ₂₇ , P ₃ ₀ , P ₃₁ , P ₃₅ , P ₄ ₀ , P ₄ ₃ -P ₄₅ , P ₄₇ , P ₇ ₀ , P ₇₁	0		0.4V _{CC}	V
V _{IL}	"L" input voltage P ₃ ₂ -P ₃₄ , P ₃ ₆ , P ₄ ₁ , P ₄ ₂ , P ₄ ₄ -P ₄₆ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0		0.2V _{CC}	V
I _{OH}	"H" average output current (Note 1) R, G, B, I, OUT, P ₀ ₀ -P ₀₇ , P ₁ ₀ -P ₁₇ , P ₂ ₀ -P ₂₇ , P ₃ ₀ , P ₃₁ , D-A			1	mA
I _{OL1}	"L" average output current (Note 2) R, G, B, I, OUT, P ₀ ₀ -P ₀₇ , P ₁ ₀ -P ₁₇ , P ₂ ₀ -P ₂₃ , P ₃ ₀ -P ₃₆ , P ₄ ₀ -P ₄₃ , D-A			2	mA
I _{OL2}	"L" average output current (Note 2) P ₆ ₀ -P ₆₇ , P ₄ ₆ , P ₄₇			1	mA
I _{OL3}	"L" average output current (Note 3) P ₂ ₄ -P ₂₇			10	mA
I _{OL4}	"L" average output current (Note 2) P ₄ ₄ , P ₄₅			3	mA
f _{CPU}	Oscillating frequency (for CPU operation) (Note 5)	3.6	4.0	6.0	MHz
f _{CRT}	Oscillating frequency (for CRT display)	6.0	7.0	8.0	MHz
f _{HS}	Input frequency P ₃ ₂ -P ₃₄ , P ₃ ₆ , P ₄ ₅			100	kHz
f _{HS}	Input frequency P ₄ ₁			1	MHz

- Note 1 : The total current that flows out of the IC should be 20mA (max)
 2 : The total of I_{OL1}, I_{OL2} and I_{OL4} should be 30mA (max.)
 3 : The total of I_{OL} of port P₂₄-P₂₇ should be 20mA (max)
 4 : Apply 0.022μF or greater capacitance externally between the V_{CC}-V_{SS} power supply pins so as to reduce power source noise
 Also apply 0.068μF or greater capacitance externally between the V_{CC}-CNV_{SS} pins
 5 : Use the crystal oscillator or ceramic resonator for CPU oscillation circuit

MITSUBISHI MICROCOMPUTERS
M37204M8-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

ELECTRIC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10$ to $70^\circ C$, $f(X_{IN})=4MHz$ unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT OFF		10	20	mA
		$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT ON		20	50	
		At stop mode			300	μA
V_{OH}	"H" output voltage $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0$, $P3_1$, R, G, B, I, OUT, D-A	$V_{CC}=4.5V$ $I_{OH}=-0.5mA$	2.4			V
V_{OL}	"L" output voltage $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_3$, $P3_0-P3_6$, $P4_0-P4_3$, R, G, B, I, OUT, D-A	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
	"L" output voltage $P6_0-P6_7$, $P4_6$, $P4_7$	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	
	"L" output voltage $P2_4-P2_7$	$V_{CC}=4.5V$ $I_{OL}=10.0mA$			3.0	
	"L" output voltage $P4_4$, $P4_5$	$V_{CC}=4.5V$ $I_{OL}=3.0mA$			0.4	
$V_{T+}-V_{T-}$	Hysteresis RESET	$V_{CC}=5.0V$		0.5	0.7	V
	Hysteresis (Note 1) H_{SYNC} , V_{SYNC} , $P3_2-P3_4$, $P3_6$, $P4_0-P4_2$, $P4_4-P4_6$	$V_{CC}=5.0V$		0.5	1.3	
I_{OZH}	"H" input leak current RESET, $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0-P3_6$, $P4_0-P4_5$, AD1-AD8	$V_{CC}=5.5V$ $V_O=5.5V$			5	μA
	"H" input leak current $P6_0-P6_7$, $P4_6$, $P4_7$	$V_{CC}=5.5V$ $V_O=12V$			10	
I_{OZL}	"L" input leak current RESET, $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0-P3_6$, $P4_0-P4_7$, $P6_0-P6_7$, AD1-AD8	$V_{CC}=5.5V$ $V_O=0V$			5	μA

Note 1. $P3_2-P3_4$, $P3_6$ have the hysteresis when these pins are used as interrupt input pins or timer input pins
 $P4_0-P4_2$, $P4_4-P4_6$ have the hysteresis when these pins are used as serial I/O ports.

MITSUBISHI MICROCOMPUTERS

M37250M6-XXXSP

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

DESCRIPTION

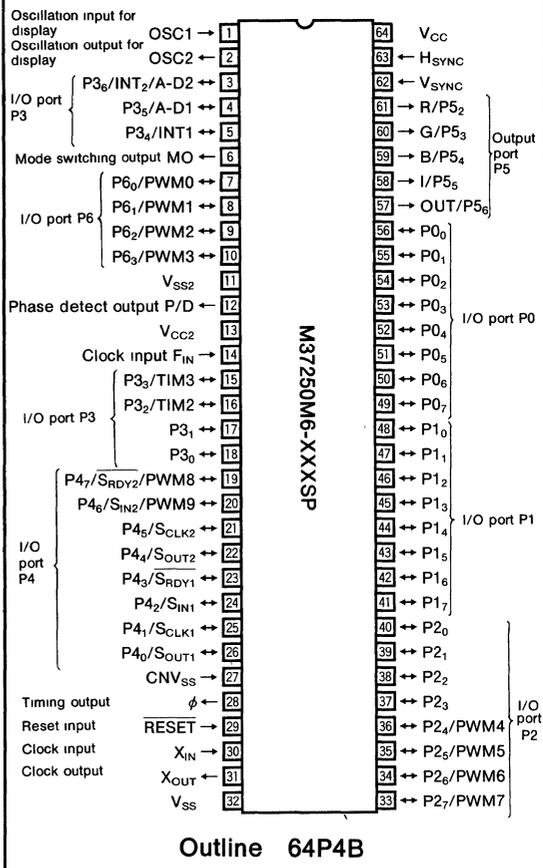
The M37250M6-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This single-chip microcomputer is useful for the high-tech channel selection system for TVs and VCRs.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

FEATURES

- Number of basic instructions 69
- Memory size ROM 24576 bytes
RAM 384 bytes
- Instruction execution time
..... 1 μ s (minimum instructions at 4MHz frequency)
- Single power supply 5V \pm 10%
- Power dissipation
Normal operation mode (at 4MHz frequency)
..... 137.5mW (V_{CC} =5.5V, CRT display, PLL operating)
- Subroutine nesting 96 levels (Max.)
- Interrupt 15types, 15vectors
- 8-bit timer 6
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P6) 43
- Output port (Port P5) 5
- PLL function
Programmable divider 14-bit
Swallow counter 5-bit
- Serial I/O (8-bit) 2
- Special serial I/O for master transfer* 1
- PWM function 8-bit \times 10
- A-D converter (4-bit resolution) 2 channels
- 72-character on screen display function
Number of character 24 characters \times 3 lines
Kinds of character 126

PIN CONFIGURATION (TOP VIEW)



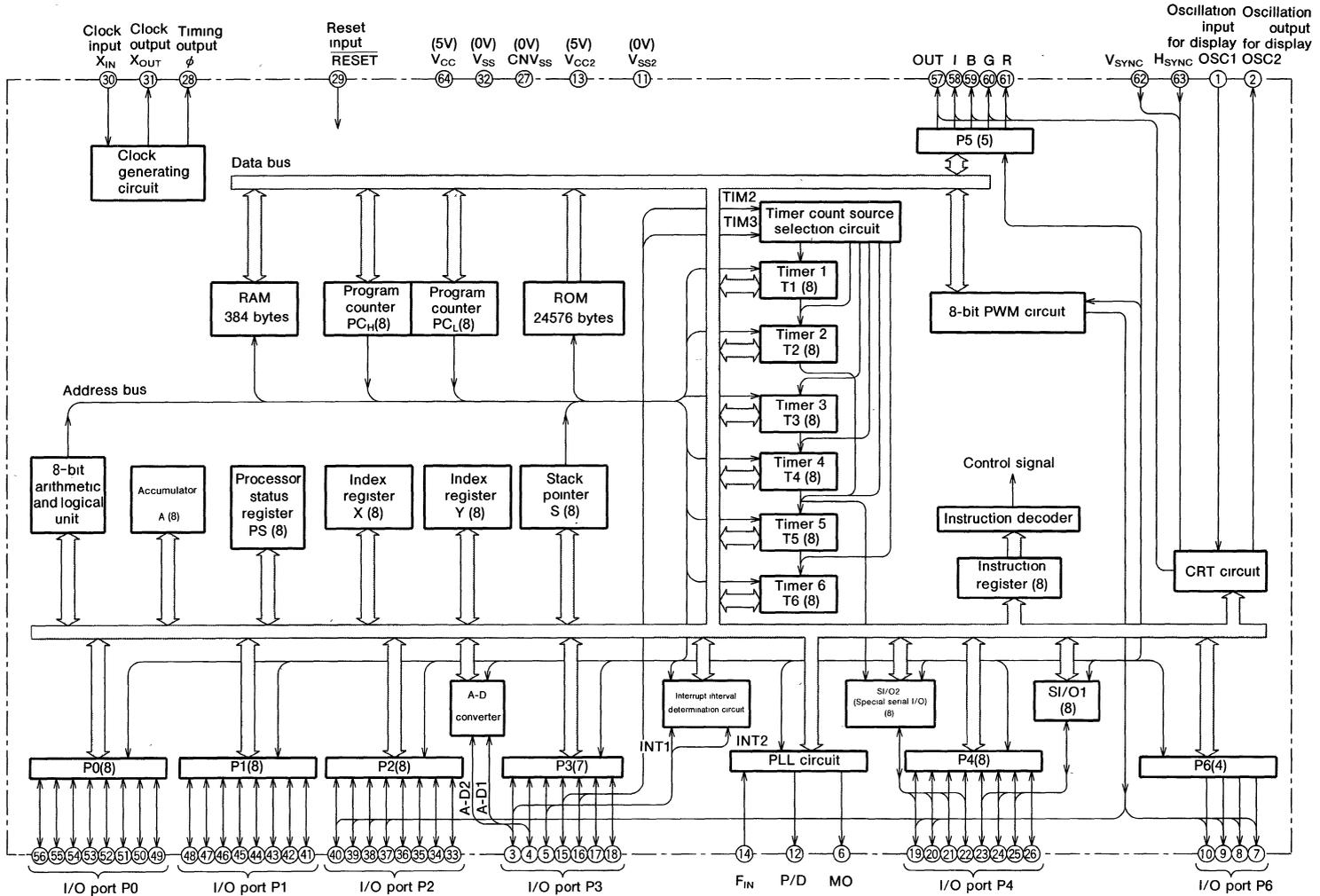
APPLICATION

TV, VCR

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.



M37250M6-XXXSP BLOCK DIAGRAM



**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

**MITSUBISHI MICROCOMPUTERS
M37250M6-XXXSP**

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

FUNCTIONS OF M37250M6-XXXSP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		1 μ s (minimum instructions, at 4MHz frequency)
Clock frequency		4MHz
Memory size	ROM	24576 bytes
	RAM	384 bytes
Input/Output ports	P0, P1	I/O
	P2	I/O
	P3 ₀ , P3 ₁	I/O
	P3 ₂ to P3 ₆	I/O
	P4	I/O
	P5	Output
	P6	I/O
Serial I/O		8-bitX2 (Special serial I/O (8-bit)X1)
Timers		8-bit timerX6
PLL function		Fixed dividing mode and swallow mode can be selected
Subroutine nesting		96 levels (max)
Interrupt		Three external interrupts, ten internal interrupts, one software interrupt
Clock generating circuit		One built-in circuits (externally connected quartz crystal oscillator)
Supply voltage		5V \pm 10%
Power dissipation	at CRT display ON and PLL operating	137.5mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)
	at CRT display OFF and PLL stopped	55mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)
	at wait mode	4mW (V _{CC} =5V, Max)
	at stop mode	0.05mW (V _{CC} =5V, Max)
Input/Output characteristics	Input/Output voltage	12V (Port P4 ₆ , P4 ₇ , P6 ₀ to P6 ₃)
	Output current	10mA (Port P2 ₄ to P2 ₇)
Operating temperature range		-10 to 70°C
Device structure		CMOS silicon gate process
Package		64-pin shrink plastic molded DIP
CRT display function	Number of character	24 charactersX3 lines (maximum 16 lines by software)
	Kinds of character	126 (12X16 dots)

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{CC2} , V _{SS} , V _{SS2}	Supply voltage		Power supply inputs 5V±10% to V _{CC} and V _{CC2} , and 0V to V _{SS} and V _{SS2}
CNV _{SS}	CNV _{SS}		This is connected to V _{SS}
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin
P ₀ to P ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
P ₁ to P ₁₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
P ₂ to P ₂₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. P ₂₄ to P ₂₇ are in common with PWM output port of PWM4 to PWM7.
P ₃ to P ₃₆	I/O port P3	I/O	Port P3 is an 7-bit I/O port and has basically the same functions as port P0, but the output structure of P ₃₀ , P ₃₁ is CMOS output and the output structure of P ₃₂ to P ₃₆ is N-channel open drain. P ₃₂ , P ₃₃ are in common with external clock input pins of timer 1, 2 and 3. P ₃₄ , P ₃₆ are in common with external interrupt input pins INT1 and INT2. P ₃₅ , P ₃₆ are in common with analog input pins of A-D converter (A-D1, A-D2).
P ₄ to P ₄₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. When serial I/O1 is used, P ₄₀ , P ₄₁ , P ₄₂ and P ₄₃ work as S _{OUT1} , S _{CLK1} , S _{IN1} and S _{RDY1} pins, respectively. When serial I/O2 is used, P ₄₄ , P ₄₅ , P ₄₆ and P ₄₇ work as S _{OUT2} , S _{CLK2} , S _{IN2} and S _{RDY2} pins, respectively. Also P ₄₆ , P ₄₇ are in common with PWM output pins of PWM 8 and 9.
OSC1,	Clock input for CRT display	Input	This is the I/O pins of the clock generating circuit for the CRT display function.
OSC2,	Clock output for CRT display	Output	
H _{SYNC}	H _{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display.
V _{SYNC}	V _{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display.
R, G, B, I, OUT	CRT output	Output	This is an 5-bit output pin for CRT display. The output structure is CMOS output. This is in common with port P ₅₂ to P ₅₆ .
P ₆ to P ₆₃	I/O port P6	I/O	Port P6 is an 4-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. This port is in common with PWM output pins PWM0 to PWM3.
MO	Mode switching output	Output	This pin outputs the mode switching signal of prescaler. When fixed dividing mode is selected, this pin can be used as 1-bit output port.
P/D	Phase detect output	Output	The phase detector output level is set to "H" when the phase is leading the reference frequency, set to "L" when lagging, and set to the floating state when in-phase.
F _{IN}	Clock input	Input	This pin inputs clock from the prescaler.

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37250 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address 00FB₁₆. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

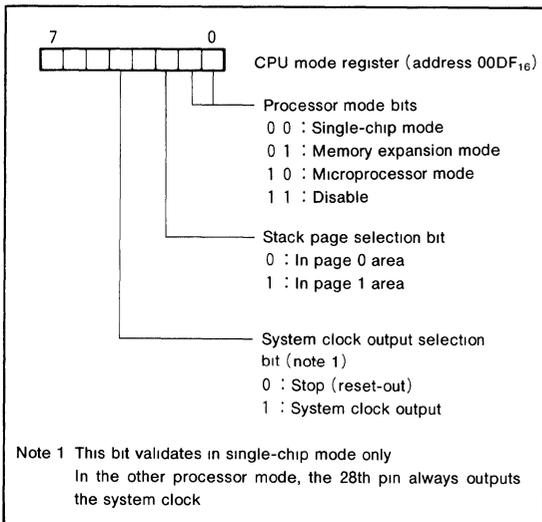


Fig. 1 Structure of CPU mode register

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

MEMORY

• Special Function Register (SFR) Area
The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM
RAM is used for data storage as well as a stack area

• ROM
ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area
The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page
Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page
Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

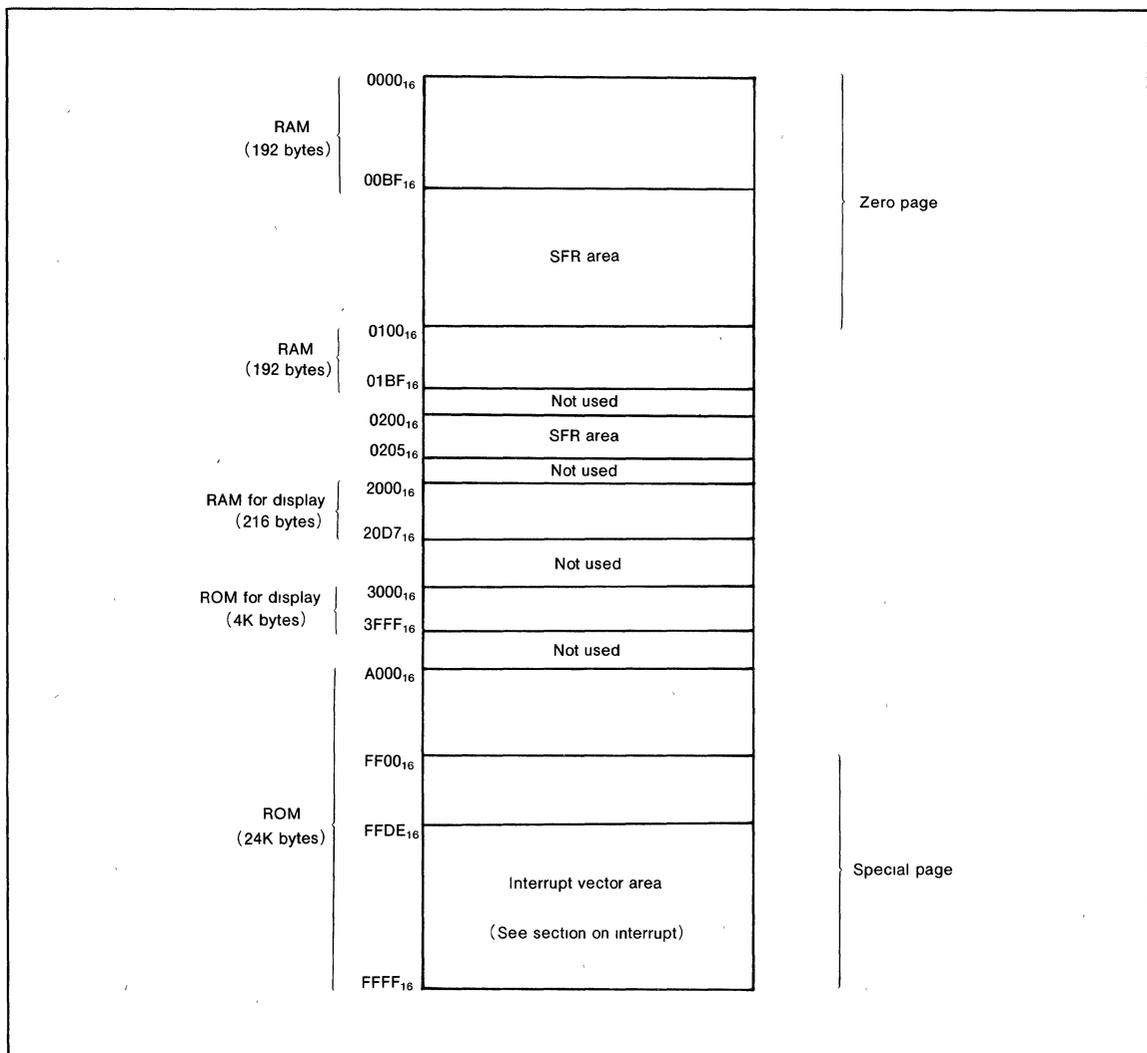


Fig. 2 Memory map

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

00C0 ₁₆	Port P0
00C1 ₁₆	Port P0 direction register
00C2 ₁₆	Port P1
00C3 ₁₆	Port P1 direction register
00C4 ₁₆	Port P2
00C5 ₁₆	Port P2 direction register
00C6 ₁₆	Port P3
00C7 ₁₆	Port P3 direction register
00C8 ₁₆	Port P4
00C9 ₁₆	Port P4 direction register
00CA ₁₆	Port P5
00CB ₁₆	Port P5 direction register
00CC ₁₆	Port P6
00CD ₁₆	Port P6 direction register
00CE ₁₆	
00CF ₁₆	
00D0 ₁₆	PWM 0 register
00D1 ₁₆	PWM 1 register
00D2 ₁₆	PWM 2 register
00D3 ₁₆	PWM 3 register
00D4 ₁₆	PWM 4 register
00D5 ₁₆	PWM output control register 1
00D6 ₁₆	PWM output control register 2
00D7 ₁₆	Interrupt interval determination register
00D8 ₁₆	Interrupt interval determination control register
00D9 ₁₆	Special serial I/O register
00DA ₁₆	Special mode register 1
00DB ₁₆	Special mode register 2
00DC ₁₆	Serial I/O1 mode register
00DD ₁₆	Serial I/O1 register
00DE ₁₆	Serial I/O2 mode register
00DF ₁₆	Serial I/O2 register
00E0 ₁₆	Horizontal position register
00E1 ₁₆	Vertical display start position register 1
00E2 ₁₆	Vertical display start position register 2
00E3 ₁₆	Vertical display start position register 3
00E4 ₁₆	Character size register
00E5 ₁₆	Border selection register
00E6 ₁₆	Color register 0
00E7 ₁₆	Color register 1
00E8 ₁₆	Color register 2
00E9 ₁₆	Color register 3
00EA ₁₆	CRT control register
00EB ₁₆	Display block counter
00EC ₁₆	CRT port control register
00ED ₁₆	
00EE ₁₆	
00EF ₁₆	A-D control register
00F0 ₁₆	Timer 1
00F1 ₁₆	Timer 2
00F2 ₁₆	Timer 3
00F3 ₁₆	Timer 4
00F4 ₁₆	Timer mode register 1
00F5 ₁₆	Timer mode register 2
00F6 ₁₆	PWM 5 register
00F7 ₁₆	PWM 6 register
00F8 ₁₆	PWM 7 register
00F9 ₁₆	PWM 8 register
00FA ₁₆	PWM 9 register
00FB ₁₆	CPU mode register
00FC ₁₆	Interrupt request register 1
00FD ₁₆	Interrupt request register 2
00FE ₁₆	Interrupt control register 1
00FF ₁₆	Interrupt control register 2
0100 ₁₆	
	RAM
	192 bytes
01BF ₁₆	
01C0 ₁₆	
	Not used
01FF ₁₆	
0200 ₁₆	PLL control register
0201 ₁₆	PCH register
0202 ₁₆	PCL register
0203 ₁₆	SWC register
0204 ₁₆	Timer 5
0205 ₁₆	Timer 6

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 14 different events consisting of three external, ten internal, and one software events. Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt. When an interrupt is accepted, the registers are pushed as described in the stack pointer (S) section above, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1, 2, interrupt control registers 1, and 2. Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0" The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program. Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
Reset	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
CRT interrupt	2	FFFD ₁₆ , FFFC ₁₆	
INT2 interrupt	3	FFFB ₁₆ , FFFA ₁₆	
INT1 interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	
Serial I/O2 interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	
Timer 4 interrupt	6	FFF5 ₁₆ , FFF4 ₁₆	
1 ms interrupt	7	FFF3 ₁₆ , FFF2 ₁₆	
V _{SYNC} interrupt	8	FFF1 ₁₆ , FFF0 ₁₆	
Timer 3 interrupt	9	FFEF ₁₆ , FFEE ₁₆	
Timer 2 interrupt	10	FFED ₁₆ , FFEC ₁₆	
Timer 1 interrupt	11	FFEB ₁₆ , FFEA ₁₆	
Serial I/O1 interrupt	12	FFE9 ₁₆ , FFE8 ₁₆	
Timer 5 interrupt	13	FFE7 ₁₆ , FFE6 ₁₆	
Timer 6 interrupt	14	FFE5 ₁₆ , FFE4 ₁₆	
BRK instruction interrupt	15	FFDF ₁₆ , FFDE ₁₆	Non-maskable software interrupt

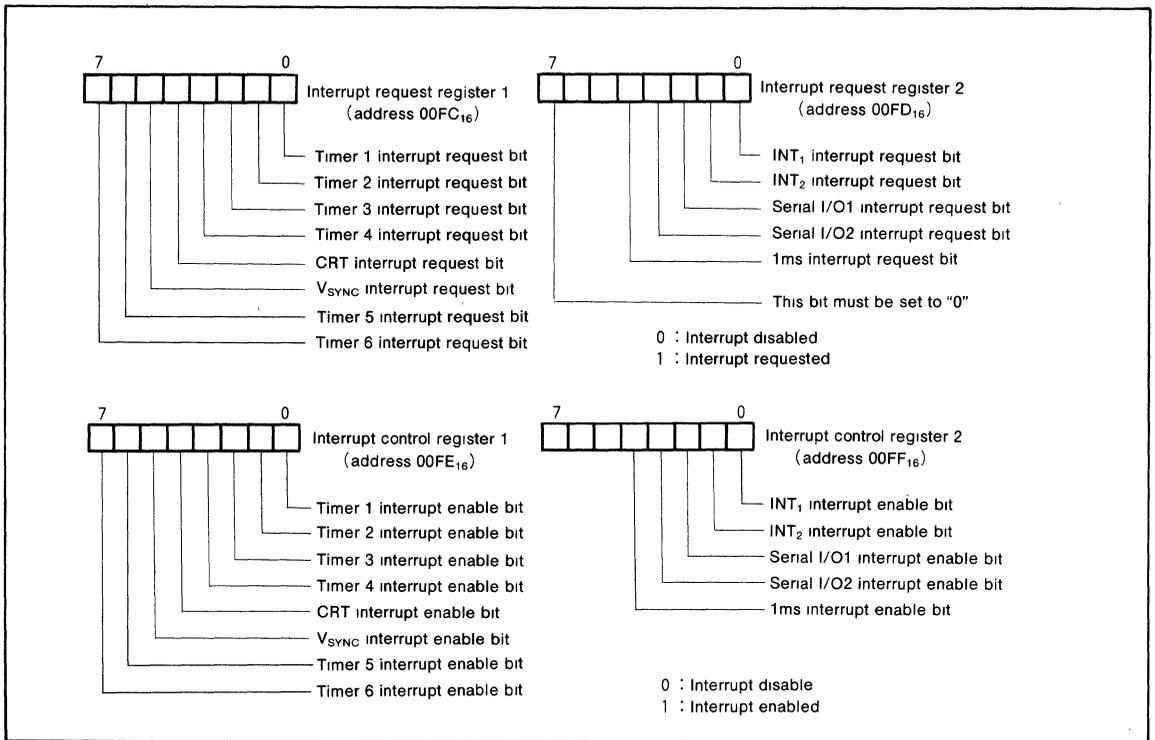


Fig. 4 Structure of registers related with interrupt

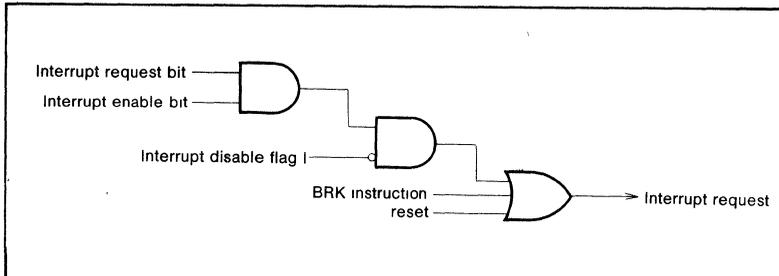


Fig. 5 Interrupt control

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

TIMER

The M37250M6-XXXSP has six timers; timer 1, timer 2, timer 3, timer 4, timer 5 and timer 6.

A block diagram of timer 1 through 6 is shown in Figure 7. All of the timers are down count timers and have 8-bit latches. When a timer reaches "00₁₆" and the next count pulse is input to a timer, a value which is the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch. The timer interrupt request bit is set at the next count pulse after the timer reaches "00₁₆".

(1) Timer 1

The count source of timer 1 is selectable from $f(X_{IN})/16$ and the 1,024 μ second clock (by 1ms interrupt; it can be used at PWM count source generating) and external clock from P3₂/TIM2 pin by timer mode register 1 (address 00F4₁₆).

Timer 1 interrupt request is occurred by overflow of timer 1.

(2) Timer 2

The count source of timer 2 is selectable from $f(X_{IN})/16$, timer 1 overflow signal, and external clock from P3₂/TIM2 pin by timer mode register 1 (address 00F4₁₆).

Timer 1 can be used as 8 bits prescaler when timer 1 overflow signal is selected as count source of timer 2.

Timer 2 interrupt request is occurred by overflow of timer 2.

(3) Timer 3

The count source of timer 3 is selectable from $f(X_{IN})/16$ and external clock from P3₃/TIM3 pin by timer mode register 2 (address 00F5₁₆).

Timer 3 interrupt request is occurred by overflow of timer 3.

(4) Timer 4

The count source of timer 4 is selectable from $f(X_{IN})/16$, $f(X_{IN})/2$, and timer 3 overflow signal by timer mode register 2 (address 00F5₁₆).

Timer 3 can be used as 8 bits prescaler when timer 3 overflow signal is selected as count source of timer 4.

Timer 4 interrupt request is occurred by overflow of timer 4.

(5) Timer 5

The count source of timer 5 is selectable from $f(X_{IN})/16$, timer 2 overflow signal and timer 4 overflow signal by timer mode register 1 (address 00F4₁₆) and timer mode register 2 (address 00F5₁₆).

(6) Timer 6

The count source of timer 6 is selectable from $f(X_{IN})/16$ and timer 5 overflow signal by timer mode register 1 (address 00F4₁₆).

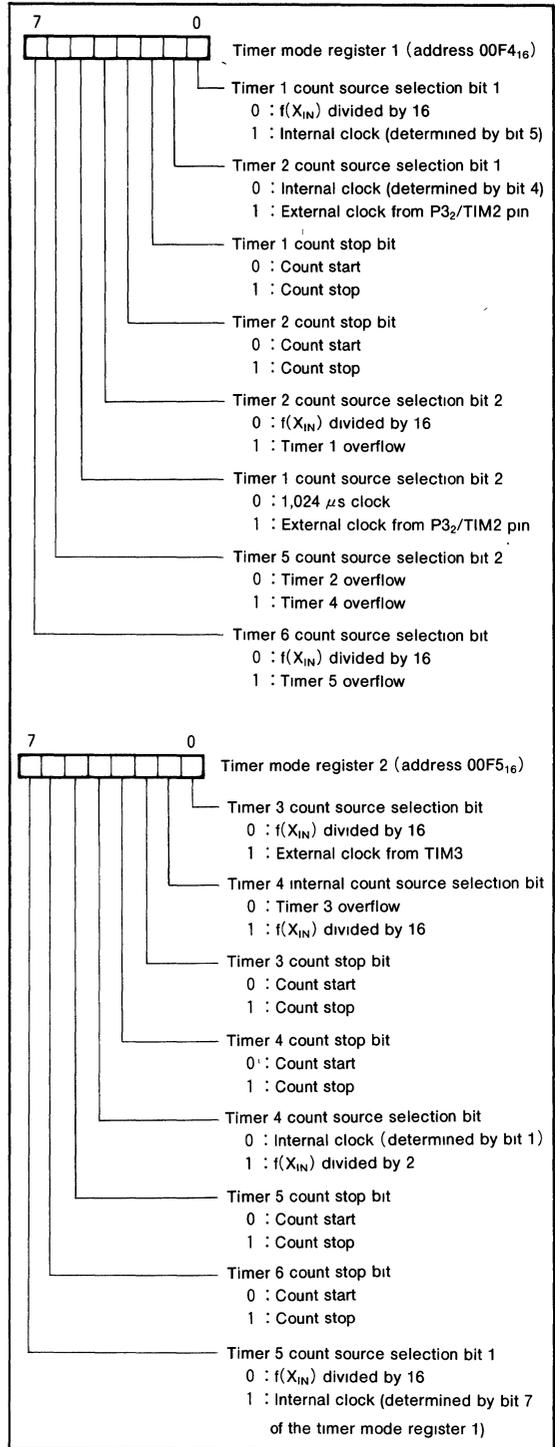


Fig. 6 Structure of timer 12 mode register and timer 34 mode register

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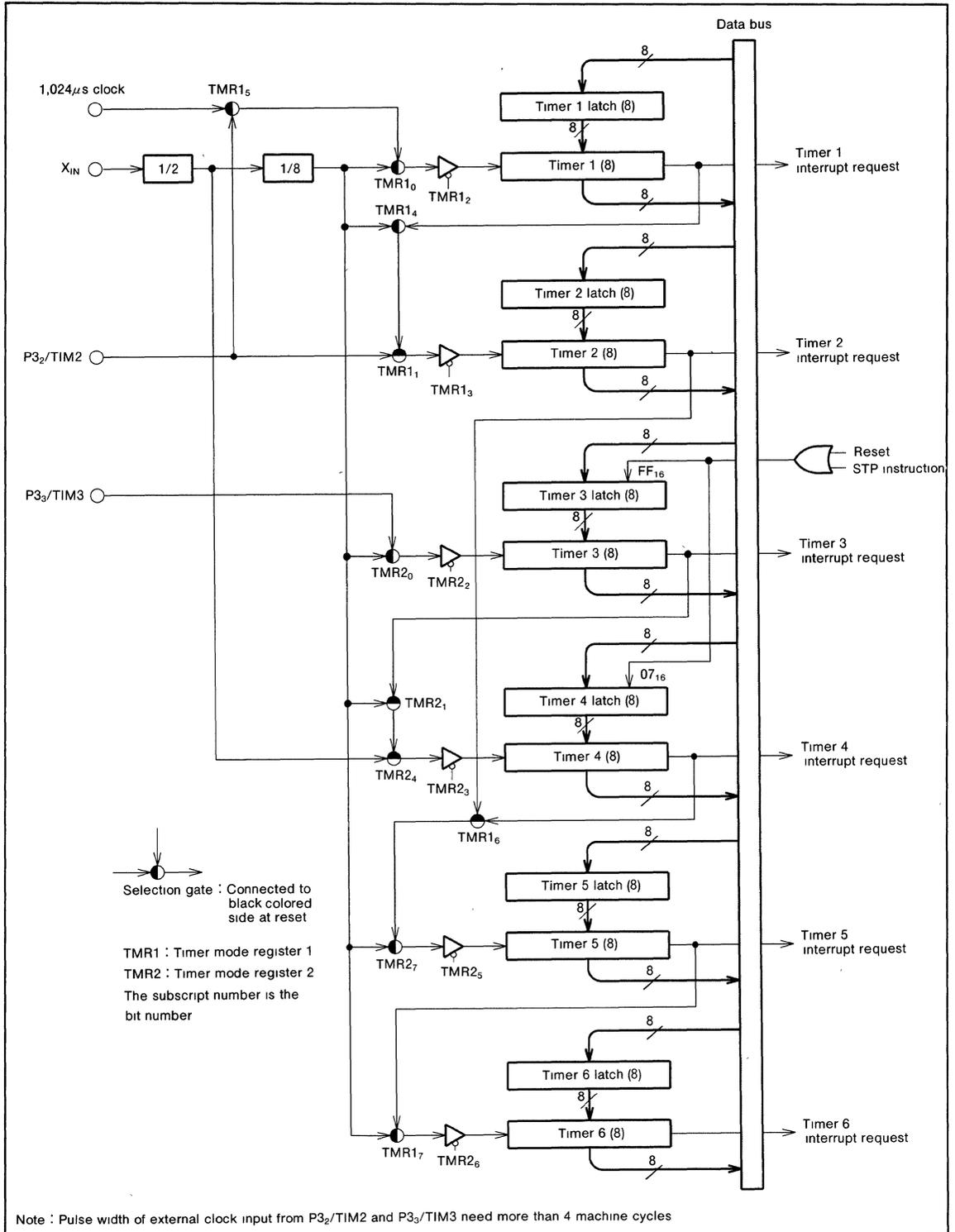


Fig. 7 Timer 1 through 6 block diagram

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

SERIAL I/O

M37250M6-XXXSP has two serial I/O (serial I/O1, serial I/O2). Serial I/O1 has the same function as serial I/O2.

A block diagram of the serial I/O is shown in Figure 8.

In the serial I/O mode the receive ready signal ($\overline{S_{RDYi}}$), synchronous input/output clock (CLK_i), and the serial I/O pins (S_{OUTi} , S_{INi}) are used as port P4. The serial I/O mode registers (address 00DC₁₆, 00DE₁₆) are 8-bit registers. Bits 0, 1 and 2 of these registers are used to select a synchronous clock source.

Bit 3 and 4 decide whether parts of P4 will be used as a serial I/O or not.

To use P4₂ or P4₆ as a serial input, set the direction register bit which corresponds to P4₂ or P4₆ to "0". For more information on the direction register, refer to the I/O pin section.

Also to use internal clock of serial I/O2, bit 1 of special mode register 1 (address 00DA₁₆) needs to be set to "1". The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

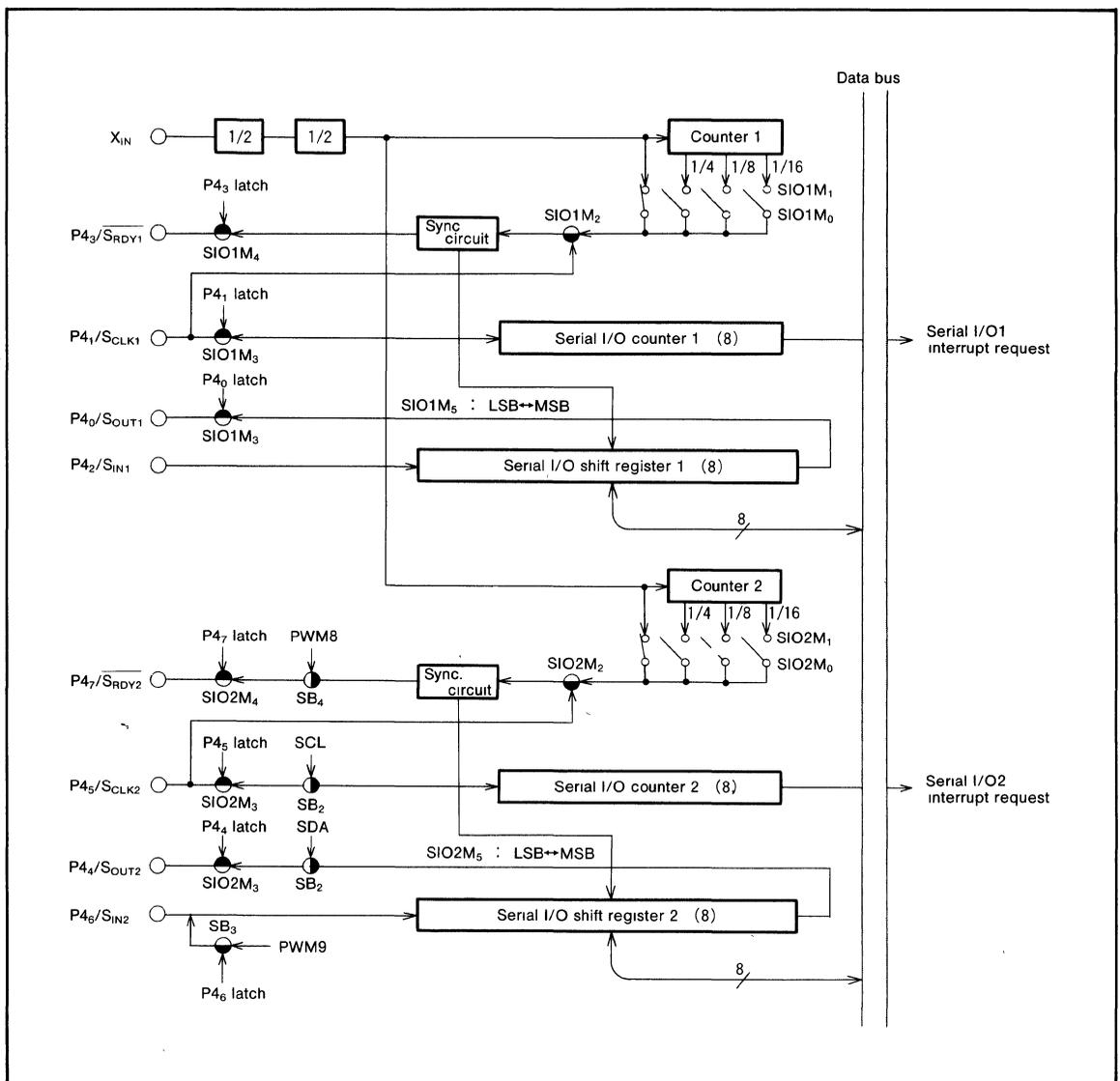


Fig. 8 Serial I/O block diagram

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Internal clock — The $\overline{S_{RDY}_i}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_i register (address 00DD₁₆, 00DF₁₆). After the falling edge of the write signal, the $\overline{S_{RDY}_i}$ signal becomes low signaling that the M37250M6-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}_i}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_i counter is set to 7 when data is stored in the serial I/O_i register. At each falling edge of the transfer clock, serial data is output to S_{OUT_i}. During the rising edge of this clock, data can be input from S_{IN_i} and the data in the serial I/O_i register will be shifted 1 bit.

Transfer direction can be selected by bit 5 of serial I/O_i mode register. After the transfer clock has counted 8 times, the serial I/O_i register will be empty and the transfer clock will remain at a high level. At this time the interrupt request

bit will be set.

External clock- If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O_i counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

An example of communication between two M37250M6-XXXSPs is shown in Figure 10.

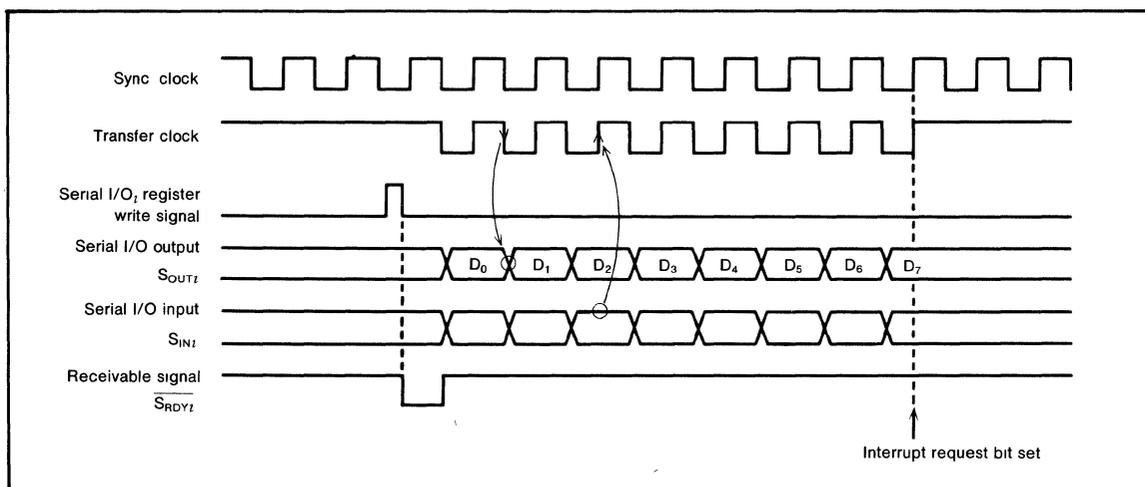


Fig. 9 Serial I/O timing

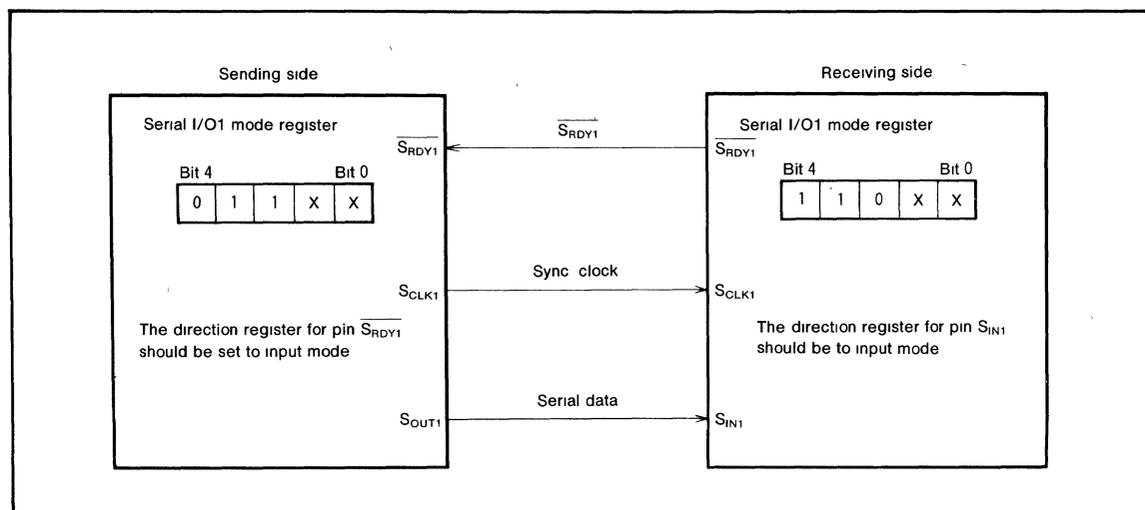


Fig. 10 Example of serial I/O connection

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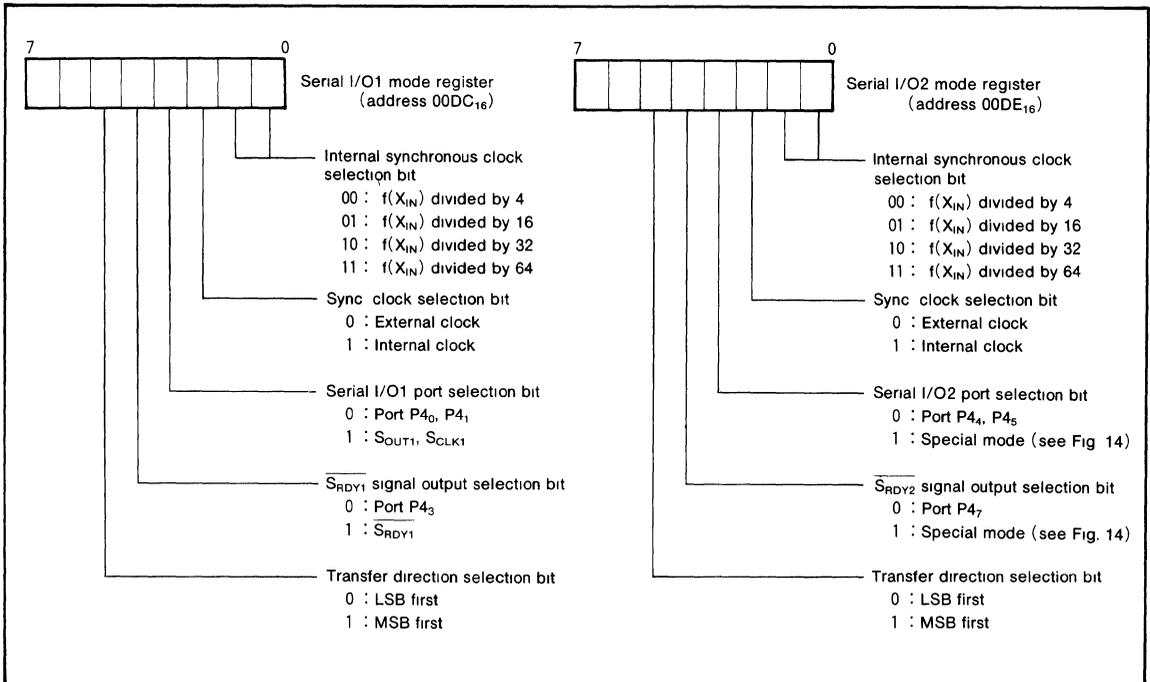


Fig. 11 Structure of serial I/O1 mode register and serial I/O2 mode register

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SPECIAL MODE (I²C BUS MODE)

M37250M6-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I²C (Inter IC) bus format.

I²C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery.

M37250M6-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O are explained in the following:

(1) Master transmission

To generate an interrupt at the end of transmission, set bit 7 of special mode register 2 (address 00DB₁₆) to "1" so as to special serial I/O interrupt is selected. Then set bit 3 of interrupt control register 2 (address 00FF₁₆) to "1" so as to special mode serial I/O interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

The output signals of master transmission SDA and SCL are output from ports P₄₄ and P₄₅. Set all bits (bits 4 and 5) corresponding to P₄₄ and P₄₅ of the port P4 register (address 00C8₁₆) and the port P4 direction register (address 00C9₁₆) to "1".

Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4 and timer mode register 2. (For instance, if $f(X_{IN})/16$ is selected as the clock source of timer 4 and "4" is set in timer 4 when $f(X_{IN})$ is 4MHz, the master transmission clock frequency is 25kHz.)

Set contents of the special mode register 2 (address 00DB₁₆). (Usually, "83₁₆".)

Set the bit 3 of serial I/O2 mode register (address 00DE₁₆) to "1". After that set the special mode register 1 (address 00DA₁₆). Figure 15 shows the structure of special mode registers 1 and 2.

Initial setting is completed by the above procedure.

Write data to be transmitted in the special serial I/O register (address 00D9₁₆). Immediately after this, clear bits 0

and 1 of special mode register 2 (to "0") to make both SDA and SCL output to "L". This is for arbitration. The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK receiving and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 3 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

To terminate data transfer, clear bits 0 and 1 of the special mode register 2 to "0", set bit 1 clock SCL to "1", then set bit 1 data SDA to "1". This procedure transmits the stop signal.

Figure 13 shows master transmission timing explained above.

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission.

In the interrupt routine, set master reception ACK provided (26₁₆) in the special mode register 1 (address 00DA₁₆), and write "FF₁₆" in the special serial I/O register (address 00D9₁₆). This sets data line SDA to "H" and to perform 8-clock master reception. Then, "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission.

Figure 14 shows master reception timing.

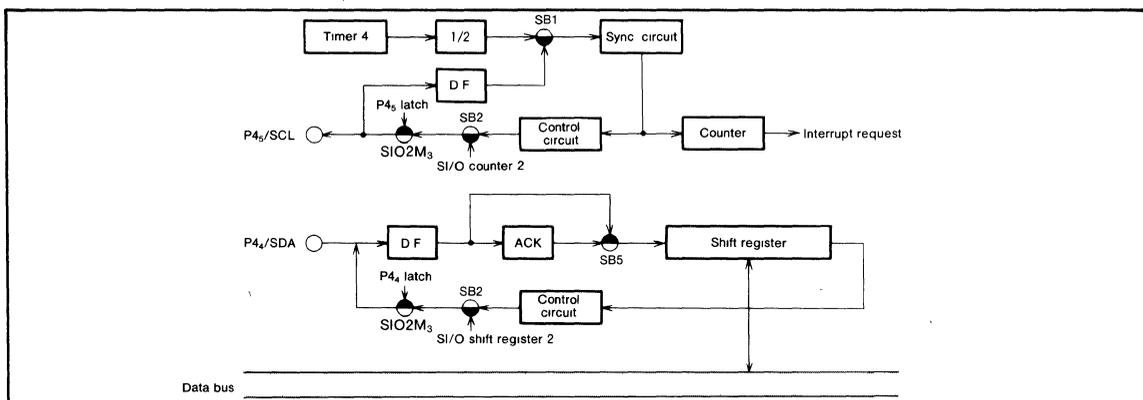


Fig. 12 Block diagram of special serial I/O

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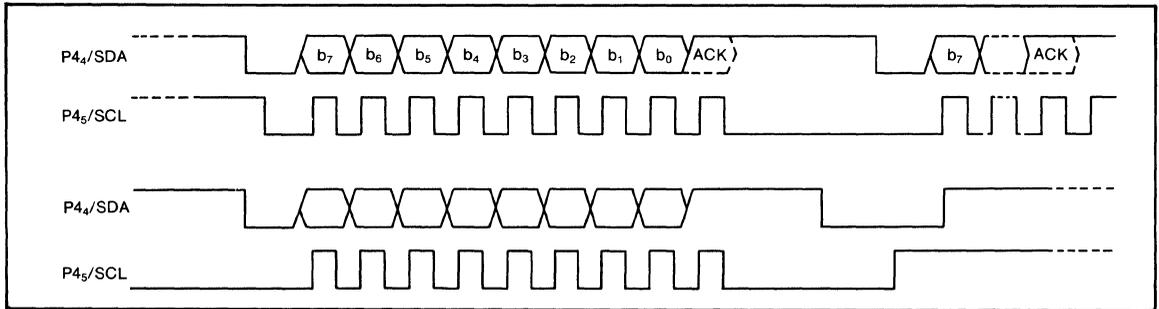


Fig. 13 Master transmission timing

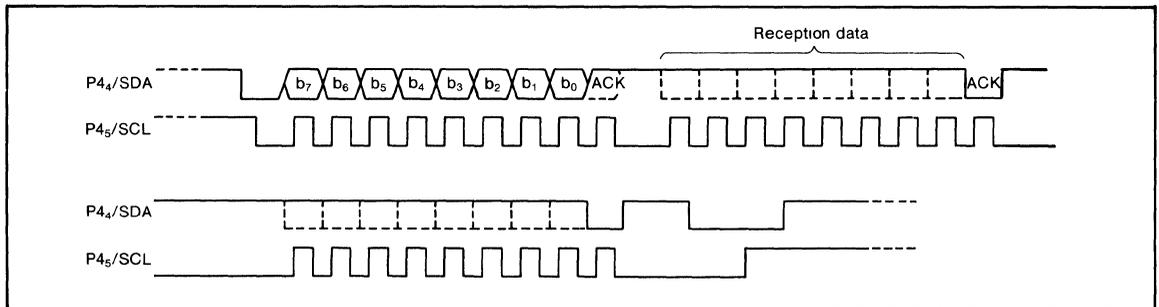


Fig. 14 Master reception timing

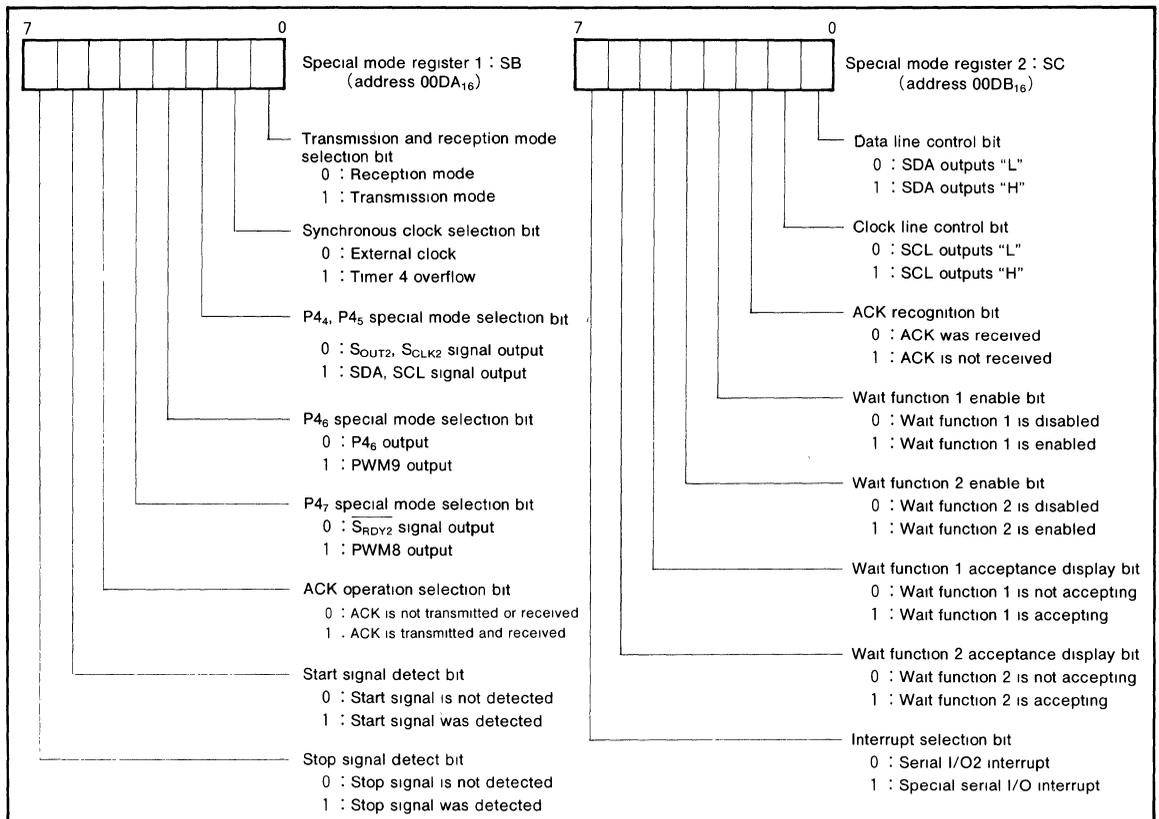


Fig. 15 Structure of special mode registers 1 and 2

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(3) Wait function

Wait function 1 holds the SCL line at "L" after the 8th clock falls in special mode. Wait function 2 holds the SCL line at "L" after the 9th clock falls in the same way.

When one of the wait functions operates, the internal counter that counts the clock must be reset after bit 3 or 4 of the special mode register 2 is set to "1", to enable the corresponding wait function 1 or 2 to operate. Reset the internal counter by writing data to the special serial I/O register (address 00D9₁₆), or by setting the START signal detection bit to "1". Reset the internal counter for each byte before data transfer.

The wait functions can be released by setting the corresponding bit 5 or 6 of the special mode register 2 to "1".

Note 1 : Clear the START signal detect bit (bit 6) and the STOP signal detect bit (bit 7) of the special mode register 1 by writing "1" to bit 6 or bit 7.

PWM OUTPUT CIRCUIT

(1) Introduction

The M37250M6-XXXSP is equipped with ten 8-bit PWMs (PWM0~PWM9). PWM0 to PWM9 have a 8-bit resolution with minimum resolution bit width of 8 μ s (for X_{IN} =4MHz) and repeat period of 2048 μ s.

Block diagram of the PWM is shown in Figure 16.

The PWM timing generator section applies individual control signals to PWM0 to 9 using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

Set the 8-bit data for output in the PWM_{*i*} register (*i* means 0 to 9; addresses 00D0₁₆ to 00D4₁₆ and 00F6₁₆ to 00FA₁₆).

(3) Transferring from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data in each PWM register is read, data in these latches has already been read allowing the data output by the PWM to be confirmed.

(4) Operation of the PWMs

The following is the explain about PWM operation.

At first, clear the bit 0 of PWM output control register 1 (address 00D5₁₆) to "0" (at reset, this bit already clear to "0" automatically), so that the PWM count source is supplied.

PWM0 to 3 output pins and PWM4 to 7 output pins are in common with port P6 and port P2 respectively, and PWM8 and 9 output pins are in common with port P4 and serial I/O2 pins.

PWM0 to 7 are selected the pin function by setting of PWM output control register 1 (address 00D5₁₆) and PWM output control register 2 (address 00D6₁₆), and PWM8 and 9 are selected the pin function by the bit 3 and 4 of special

mode register 1 (address 00DA₁₆) and bit 4 of serial I/O2 mode register (address 00DE₁₆). When these pins are set as PWM output pins by these registers, the PWM output can be performed.

Figure 17 shows the timing diagram of PWM0 through 9. One cycle (T) is composed of 256 (2⁸) segments. There are eight different pulse types configured from bits 0 to 7 representing the significance of each bit. These are output within one cycle in the circuit internal section. Refer Figure 17 (a).

Eight different pulses can be output from the PWM. These can be selected by bits 0 through 7. Depending on the content of the 8-bit PWM latch, pulses from 7 to 0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 17 (b).

Change in the contents of the PWM latch allows the selection of 256 lengths of high-level area outputs varying from 0/256 to 255/256. An length of entirely high-level output cannot be output, i. e. 256/256.

(5) Output after reset

At reset the output of port P2, P4, P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, the contents of the latch is undefined until its data is transferred to the latch.

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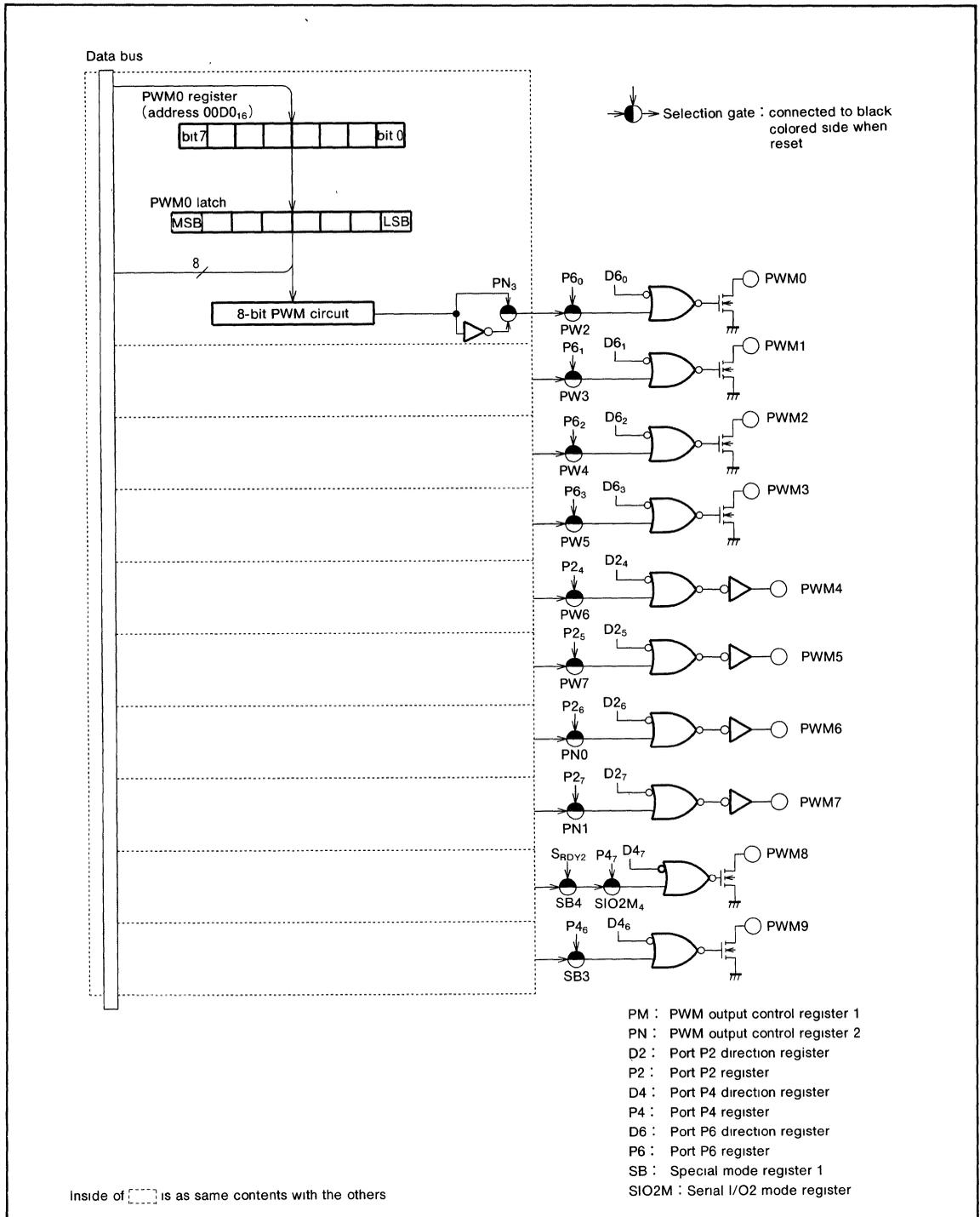


Fig. 16 Block diagram of the PWM circuit

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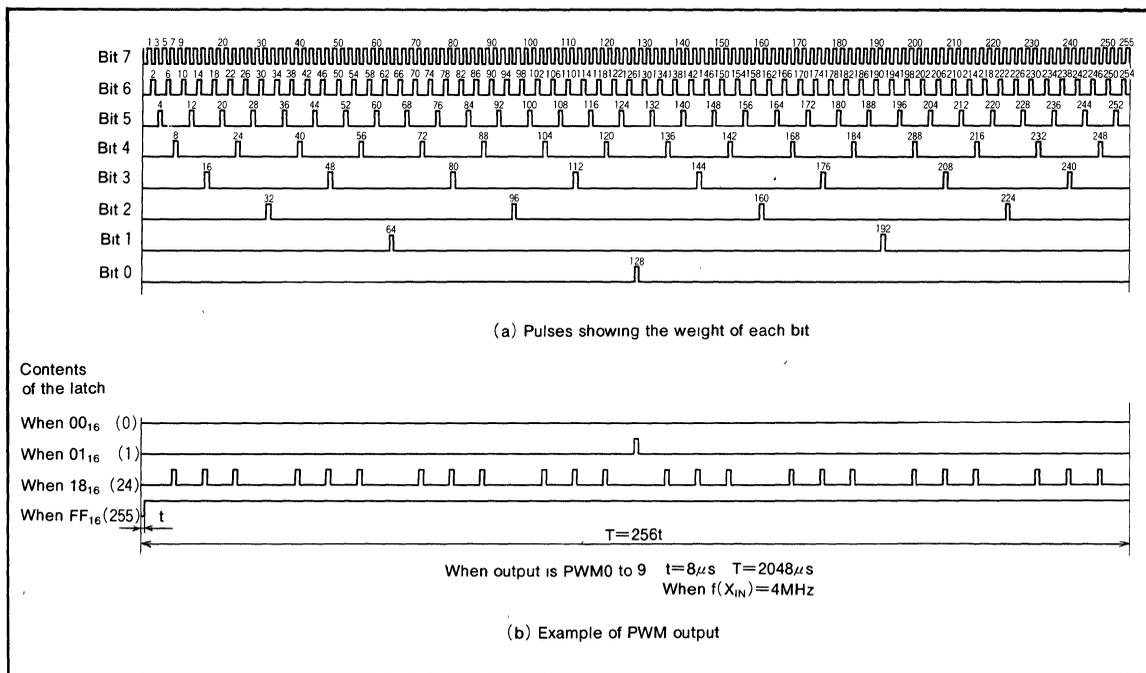


Fig. 17 PWM timing diagram

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

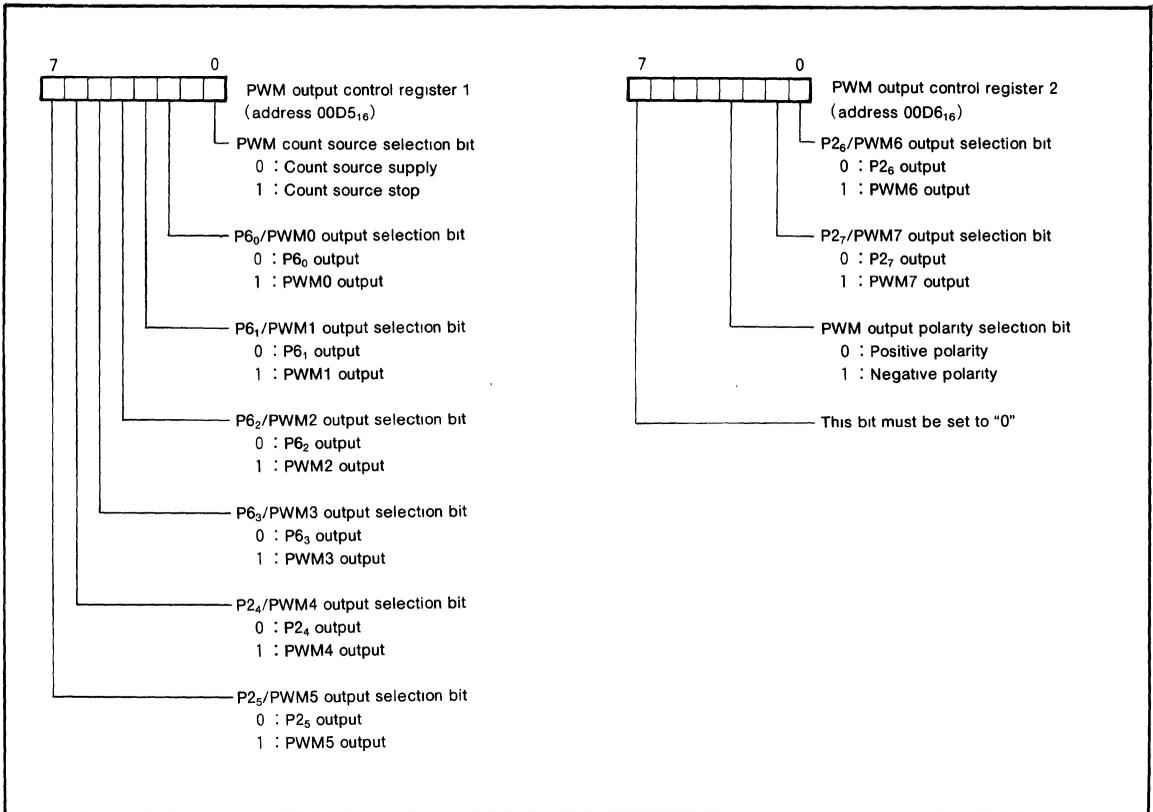


Fig. 18 Structure of PWM output control register 1 and 2

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A-D CONVERTER

Block diagram of A-D converter is shown in Figure 19. A-D converter consists of 4-bit D-A converter and comparator. The A-D control register can generate 1/16 V_{CC} -step internal analog voltage based on the settings of bits 0 to 3.

Table 3 gives the relation between the descriptions of A-D control register bits 0 to 3 and the generated internal analog voltage. The comparison result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 4.

The data is compared by setting the directional register corresponding to port $P3_5$, $P3_6$ to "0" (port $P3_5$, $P3_6$ enters the input mode), to allow port $P3_5/A-D1$, $P3_6/A-D2$ to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register, bit 0 to 3 and an analog input pin is selected. After 20 machine cycle, the voltage comparison starts.

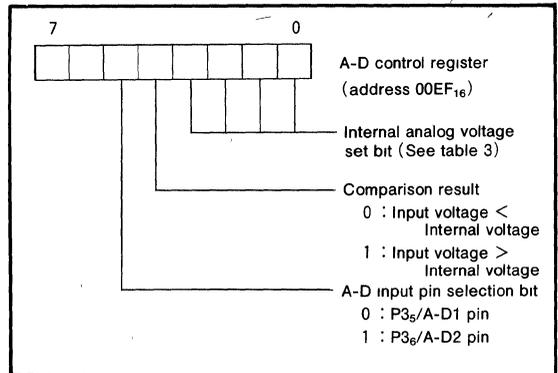


Fig. 20 Structure of A-D control register

Table 3. Relationship between the contents of A-D control register and internal analog voltage

A-D control register				Internal analog voltage
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	1/32 V_{CC}
0	0	0	1	3/32 V_{CC}
0	0	1	0	5/32 V_{CC}
0	0	1	1	7/32 V_{CC}
0	1	0	0	9/32 V_{CC}
0	1	0	1	11/32 V_{CC}
0	1	1	0	13/32 V_{CC}
0	1	1	1	15/32 V_{CC}
1	0	0	0	17/32 V_{CC}
1	0	0	1	19/32 V_{CC}
1	0	1	0	21/32 V_{CC}
1	0	1	1	23/32 V_{CC}
1	1	0	0	25/32 V_{CC}
1	1	0	1	27/32 V_{CC}
1	1	1	0	29/32 V_{CC}
1	1	1	1	31/32 V_{CC}

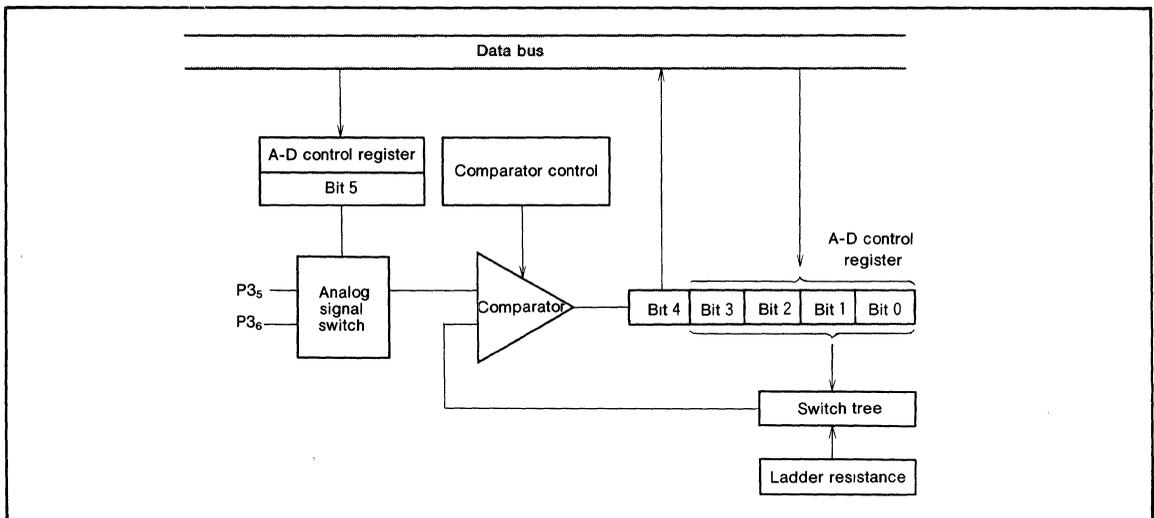


Fig. 19 Block diagram of A-D converter

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PLL CIRCUIT

M37250M6-XXXSP has a built-in PLL circuit which is selectable either fixed dividing mode or swallow mode. PLL block diagram is shown in Figure 21.

(1) PLL control register

Switching fixed dividing mode/swallow mode, starting PLL operation, and selection of reference frequency are determined by PLL control register (address 0200₁₆)
When fixed dividing mode is selected by setting the bit 6 (PL₆) of PLL control register to "0", MO pin becomes 1-bit general purpose output port. In this case, the output level of MO pin is determined by bit 5 (PL₅) of PLL control register (address 0200₁₆).

(2) Reference frequency generator

Nine kinds reference frequency are generated by built-in reference frequency generator that divides the external clock (4MHz), in both fixed dividing mode and swallow mode.
Reference frequency is determined by bit 0 (PL₀) to bit 4 (PL₄) of PLL control register.

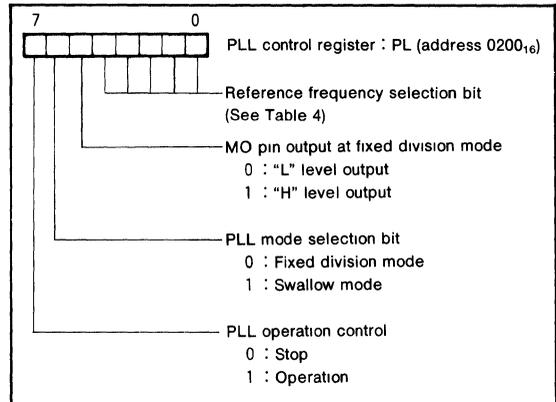


Fig. 22 Structure of PLL control register

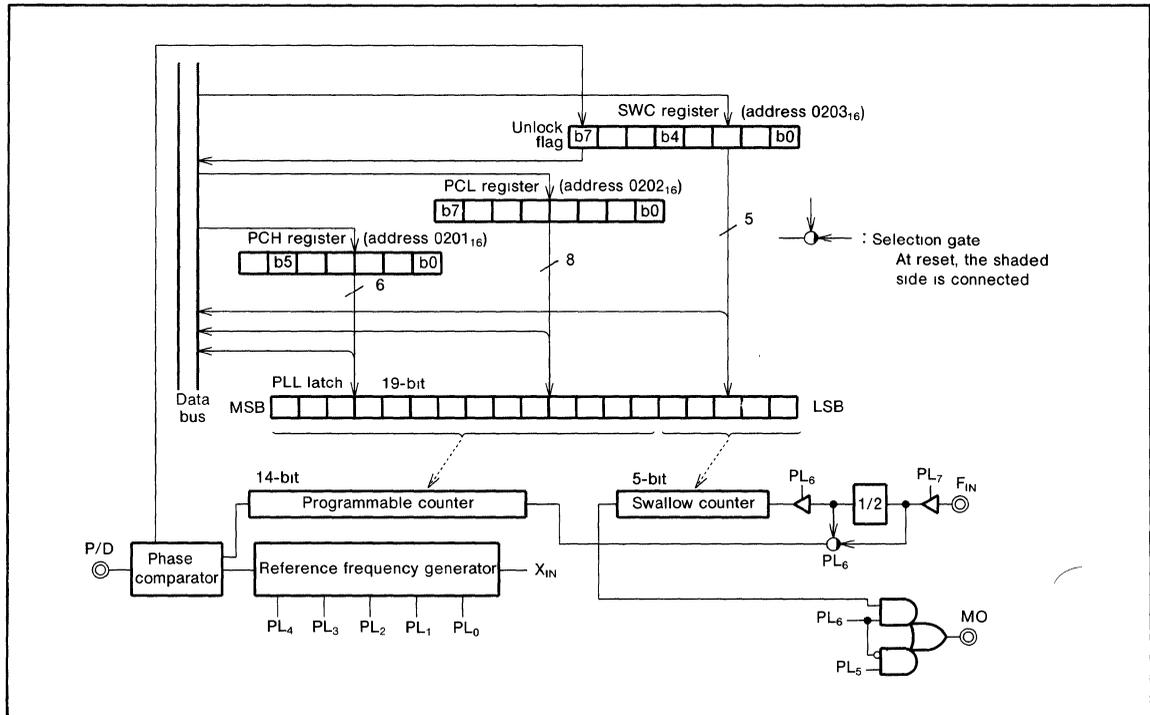


Fig. 21 PLL circuit block diagram

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(3) Phase detector

Phase detector is a built-in circuit to detect a phase difference between reference frequency (f_{REF}) and division of VC0 output by programmable divider.

Output of phase detector is input into internal charge pump, and outputs the following level from P/D pin.

- "L" level where $f_{REF} > f_{IN}/N$
- "H" level where $f_{REF} < f_{IN}/N$
- Floating where $f_{REF} = f_{IN}/N$

f_{IN} : Oscillation frequency of VC0

N : Division ratio of all PLL system include external pre-scaler.

Table 4. PLL control register bit mapping about reference frequency

PLL control register (address 0200 ₁₆)					Reference frequency
PL ₄	PL ₃	PL ₂	PL ₁	PL ₀	
0	0	1	1	1	7.8125kHz
0	1	0	0	1	5.0000kHz
0	1	0	1	0	0.78125kHz
0	1	0	1	1	3.125kHz
0	1	1	1	1	1.953125kHz
1	0	1	0	0	1.5625kHz
1	0	1	1	0	0.9765625kHz
1	0	1	1	1	3.90625kHz

(4) Programmable divider

Programmable divider is a binary down-counter configured by 5-bit swallow counter and 14-bit programmable counter. Lower 5 bits of 19-bit PLL latch data are preset to swallow counter and higher 14 bits of 19-bit PLL latch data are preset to programmable counter at a time, and it is down-counted.

(5) PLL latch

Data is set to programmable counter through PLL latch.

Contents of PLL latch is determined by following sequence.

- Writing contents of swallow counter to SWC register (address 0203₁₆)
- Writing lower 8-bit of programmable counter to PCL register (address 0202₁₆)
- Writing higher 6-bit of programmable counter to PCH register (address 0201₁₆)

Each register data is transferred to PLL latch, after writing to PCH register. Even when only lower 8-bit of programmable counter or contents of swallow counter need to change, be sure to write to PCH register again.

When reading the addresses 0201₁₆ to 0203₁₆ assigned PCH register, PCL register, and SWC register, the contents of PLL latch is read

The contents of PLL latch is indeterminate during reset. And this PLL latch contents is indetermined till the transfer is completed, even though data are set to PCH, PLL, and SWC registers.

(6) Unlock flag

When PLL system is unlock, namely when reference frequency f_{REF} is difficult from division output frequency of VC0, the pulse is output synchronized f_{REF} from phase detector. Unlock flag is assigned in bit 7 of SWC register, and it is set to "1" by this pulse, and this flag is set to "0" by reading. So, reading cycle is necessary to be longer than f_{REF} cycle. If the reading cycle is shorter than f_{REF} cycle, unlocked PLL system is regard as locking, so that this microcomputer may be missing operation. More time than f_{REF} cycle need to read unlock flag at first, after PLL operation starts.

(7) Programmable divider determination method

When M54470L (division ratio is 1/128 or 1/136) is used as prescaler at swallow mode, determination method of programmable divider division value is as following.

$$f_o = 8 \cdot f_{REF} (32N_p + A)$$

f_o : Partial oscillation frequency

f_{REF} : Reference frequency

N_p : Division ratio of programmable counter
 $2^{14} \geq N_p \geq 16$ and $N_p > A$

A : Division ratio of swallow counter
 $31 \geq A \geq 0$

When fixed prescaler (division ratio 1/K) is used at fixed dividing mode, determination method of programmable divider division value is as following.

$$f_o = f_{REF} \cdot K \cdot N_p$$

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CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 5 outlines the CRT display functions of the M37250M6-XXXSP. The M37250M6-XXXSP incorporates a 24 columns X 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 126 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12 X 16 dot configuration to obtain smooth character patterns. (See Figure 23)

The following shows the procedure how to display characters on the CRT screen.

Table 5. Outline of CRT display functions

Parameter	Functions	
Number of display character	24 characters X 3 lines	
Character configuration	12 X 16 dots (See Figure 23)	
Kinds of character	126	
Character size	4 size selectable	
Color	Kinds of color	15 (max)
	Coloring unit	a character
Display expansion	Possible (multiple lines)	

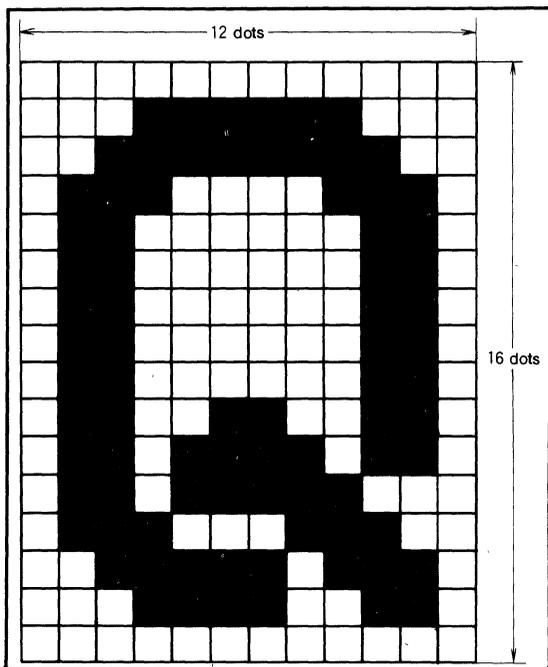


Fig. 23 CRT display character configuration

- ① Set the character to be displayed in display RAM.
- ② Set the display color by using the color register.
- ③ Specify the color register in which the display color is set by using the display RAM.
- ④ Specify the vertical position and character size by using the vertical position register and the character size register.
- ⑤ Specify the horizontal position by using the horizontal position register.
- ⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 25 shows a block diagram of the CRT display control circuit. Figure 24 shows the structure of the CRT display control register.

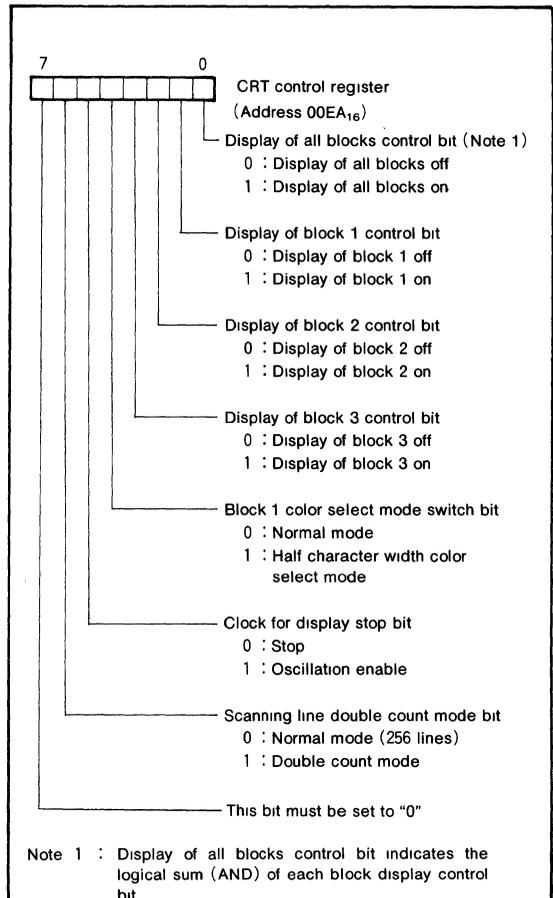


Fig. 24 Structure of CRT control register

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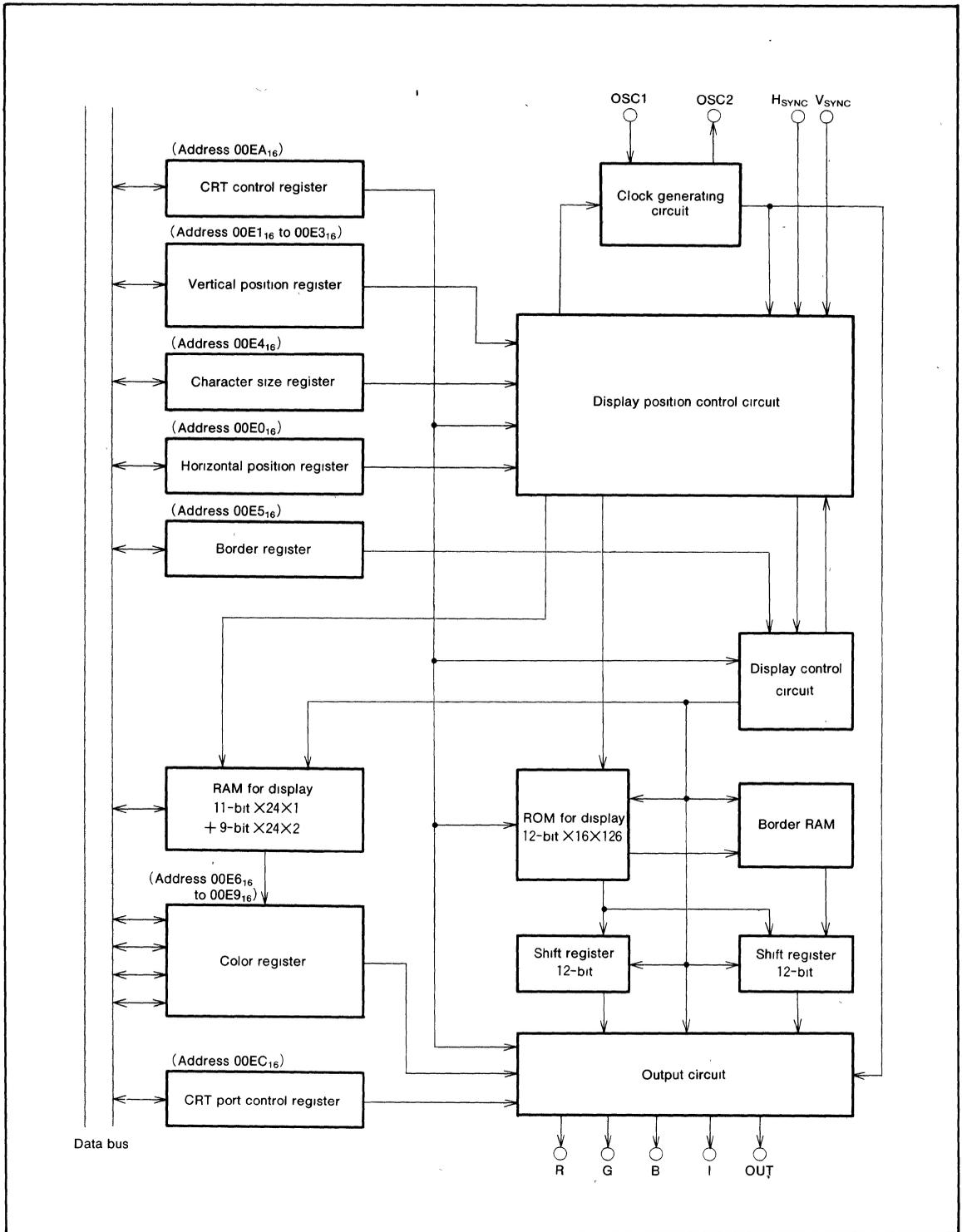


Fig. 25 Block diagram of CRT display control circuit

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(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 24 characters can be displayed in one block. (See (4) Display Memory.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of $4T_c$ (T_c = oscillation cycle for display).

The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 28), a block of the smaller block No. (1 to 3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 28), the former block is overridden and the latter is displayed.

The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values 00_{16} to $7F_{16}$ to bits 0 to 6 in the vertical position register (addresses $00E1_{16}$ to $00E3_{16}$). Figure 26 shows the structure of the vertical position register.

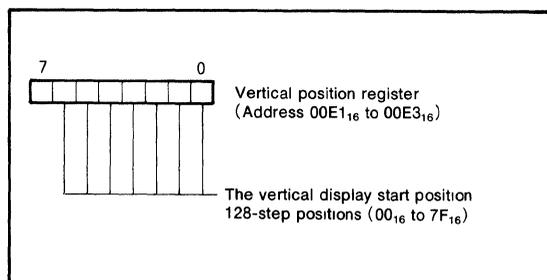


Fig. 26 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64-step display positions ($4T_c$ per step (T_c = oscillation cycle for display)) by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the horizontal position register (address $00E0_{16}$). Figure 27 shows the structure of the horizontal position register.

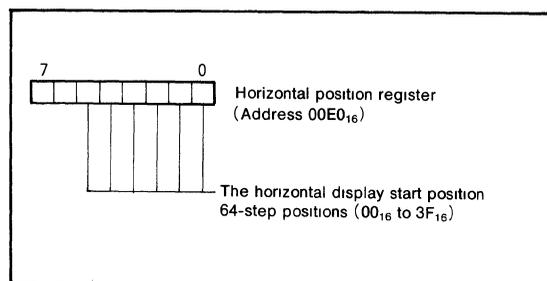
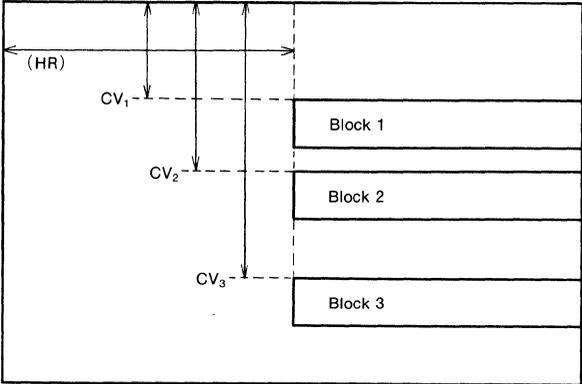
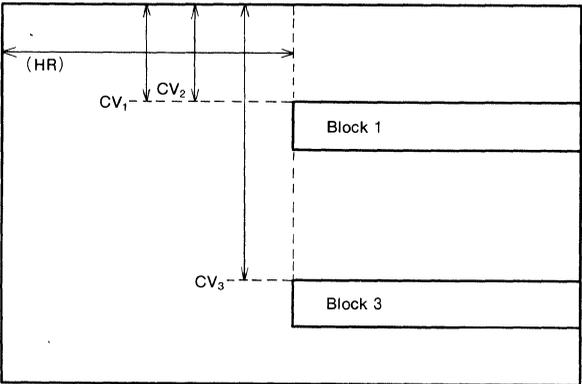


Fig. 27 Structure of horizontal position register

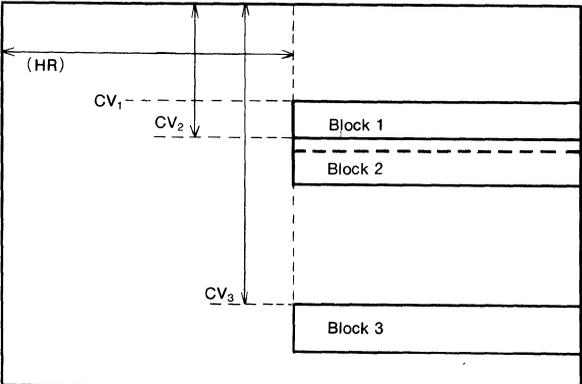
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(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed

Fig. 28 Display position

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(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the character size register (address 00E4₁₆) to set a character size. The character size in block 1 can be specified by using bits 0 and 1 in the character size register; the character size in block 2 can be specified by using bits 2 and 3; the character size in block 3 can be specified by using bits 4 and 5. Figure 29 shows the structure of the character size register.

The character size can be selected from four sizes: small size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation (=T_c) in the width (horizontal) direction. The small size consists of [one scanning line] × [1 T_c]; the medium size consists of [two scanning lines] × [2 T_c]; the large size consists of [three scanning lines] × [3 T_c]; and the extra large size consists of [four scanning lines] × [4 T_c]. Table 6 shows the relationship between the set values in the character size register and the character sizes.

Table 6. The relationship between the set values of the character size register and the character sizes

Set values of the character size register		Character size	Width (horizontal) direction	Height (vertical) direction
CS _{n1}	CS _{n0}			
0	0	Small	1 T _c	1
0	1	Medium	2 T _c	2
1	0	Large	3 T _c	3
1	1	Extra large	4 T _c	4

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal start position is common to all blocks even when the character size varies with each block (See Figure 30)

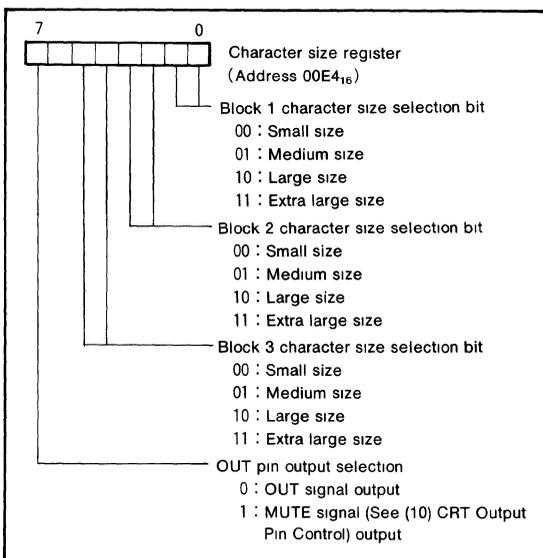


Fig. 29 Structure of character size register

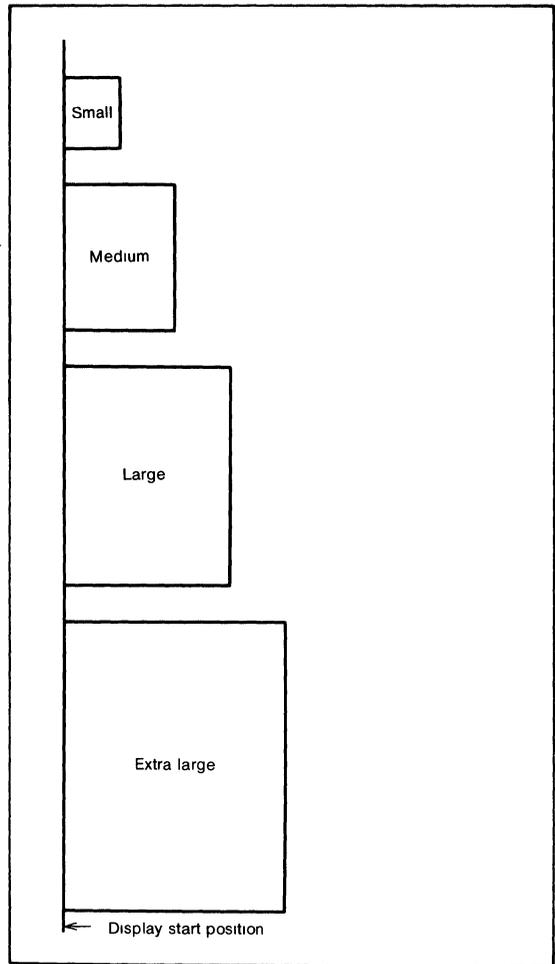


Fig. 30 Display start position of each character size (horizontal direction)

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(4) Display Memory

There are two types of display memory: ROM of CRT display (3000_{16} to $3FFF_{16}$) used to store character dot data (masked) and display RAM (2000_{16} to $20D7_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① ROM for CRT display (3000_{16} to $3FFF_{16}$)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM.

The CRT display ROM has a capacity of 4K bytes. Because 32 bytes are required for one character data, the ROM can contain up to 128 kinds of characters. Actually, however, because two characters are required for test pattern use, the ROM can contain up to 126 kinds of characters for display use.

The CRT display ROM space is broadly divided into two areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses

3000_{16} to $37FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 3800_{16} to $3FFF_{16}$. (See Figure 31) Note however that the four upper bits in the data to be written to addresses 3800_{16} to $3FFF_{16}$ must be set to "1" (by writing data $F0_{16}$ to FF_{16}).

The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.

Assume that data for one character is stored at $3XX0_{16}$ to $3XXF_{16}$ (XX denotes 00_{16} to $7F_{16}$) and $3YY0_{16}$ to $3YYF_{16}$ (YY denotes 80_{16} to FF_{16}), then the character code for it is "XX".

In other words, character code for any given character is configured with two middle digits of the four-digit (hex-notated) address (3000_{16} to $37FF_{16}$) where data for that character is stored.

Table 7 lists the character codes.

Table 7. Character code list

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00_{16}	3000_{16} to $300F_{16}$	3800_{16} to $380F_{16}$
01_{16}	3010_{16} to $301F_{16}$	3810_{16} to $381F_{16}$
02_{16}	3020_{16} to $302F_{16}$	3820_{16} to $382F_{16}$
03_{16}	3030_{16} to $303F_{16}$	3830_{16} to $383F_{16}$
:	:	:
10_{16}	3100_{16} to $310F_{16}$	3900_{16} to $390F_{16}$
11_{16}	3110_{16} to $311F_{16}$	3910_{16} to $391F_{16}$
:	:	:
$4F_{16}$	$34F0_{16}$ to $34FF_{16}$	$3CF0_{16}$ to $3CFF_{16}$
50_{16}	3500_{16} to $350F_{16}$	$3D00_{16}$ to $3D0F_{16}$
:	:	:
$7D_{16}$	$37D0_{16}$ to $37DF_{16}$	$3FD0_{16}$ to $3FDF_{16}$
$7E_{16}$ *	$37E0_{16}$ to $37EF_{16}$	$3FE0_{16}$ to $3FEF_{16}$
$7F_{16}$ *	$37F0_{16}$ to $37FF_{16}$	$3FF0_{16}$ to $3FFF_{16}$

* : The test pattern are stored

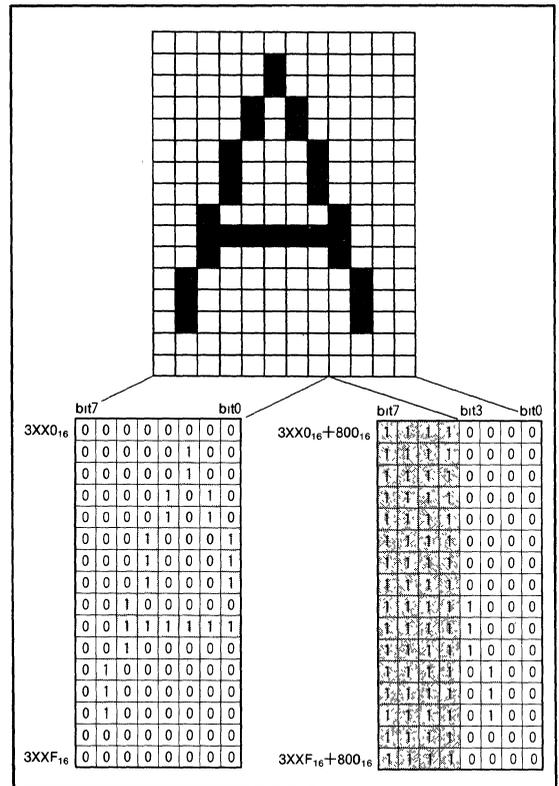


Fig. 31 Display character stored area

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② CRT display RAM (2000₁₆ to 20D7₁₆)

The CRT display RAM is allocated at addresses 2000₁₆ to 20D7₁₆, and is divided into a display character code specifying part and display color specifying part for each block. Table 8 shows the contents of the CRT display RAM.

When a character is to be display at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0 to 6) in address 2000₁₆ and the color register No. to the two low-order bits (bits 0 and 1) in address 2080₁₆. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 32. Write the character patterns at Table 9 and 10 as test pattern, when M37250M6-XXXSP is mask-ordered.

Table 8. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st column	2000 ₁₆	2080 ₁₆
	2nd column	2001 ₁₆	2081 ₁₆
	3rd column	2002 ₁₆	2082 ₁₆
	⋮	⋮	⋮
	22th column	2015 ₁₆	2095 ₁₆
	23th column	2016 ₁₆	2096 ₁₆
	24th column	2017 ₁₆	2097 ₁₆
Not used		2018 ₁₆	2098 ₁₆
		}	}
		201F ₁₆	209F ₁₆
Block 2	1st column	2020 ₁₆	20A0 ₁₆
	2nd column	2021 ₁₆	20A1 ₁₆
	3rd column	2022 ₁₆	20A2 ₁₆
	⋮	⋮	⋮
	22th column	2035 ₁₆	20B5 ₁₆
	23th column	2036 ₁₆	20B6 ₁₆
	24th column	2037 ₁₆	20B7 ₁₆
Not used		2038 ₁₆	20B8 ₁₆
		}	}
		203F ₁₆	20BF ₁₆
Block 3	1st column	2040 ₁₆	20C0 ₁₆
	2nd column	2041 ₁₆	20C1 ₁₆
	3rd column	2042 ₁₆	20C2 ₁₆
	⋮	⋮	⋮
	22th column	2055 ₁₆	20D5 ₁₆
	23th column	2056 ₁₆	20D6 ₁₆
	24th column	2057 ₁₆	20D7 ₁₆
Not used		2058 ₁₆	
		}	
		207F ₁₆	

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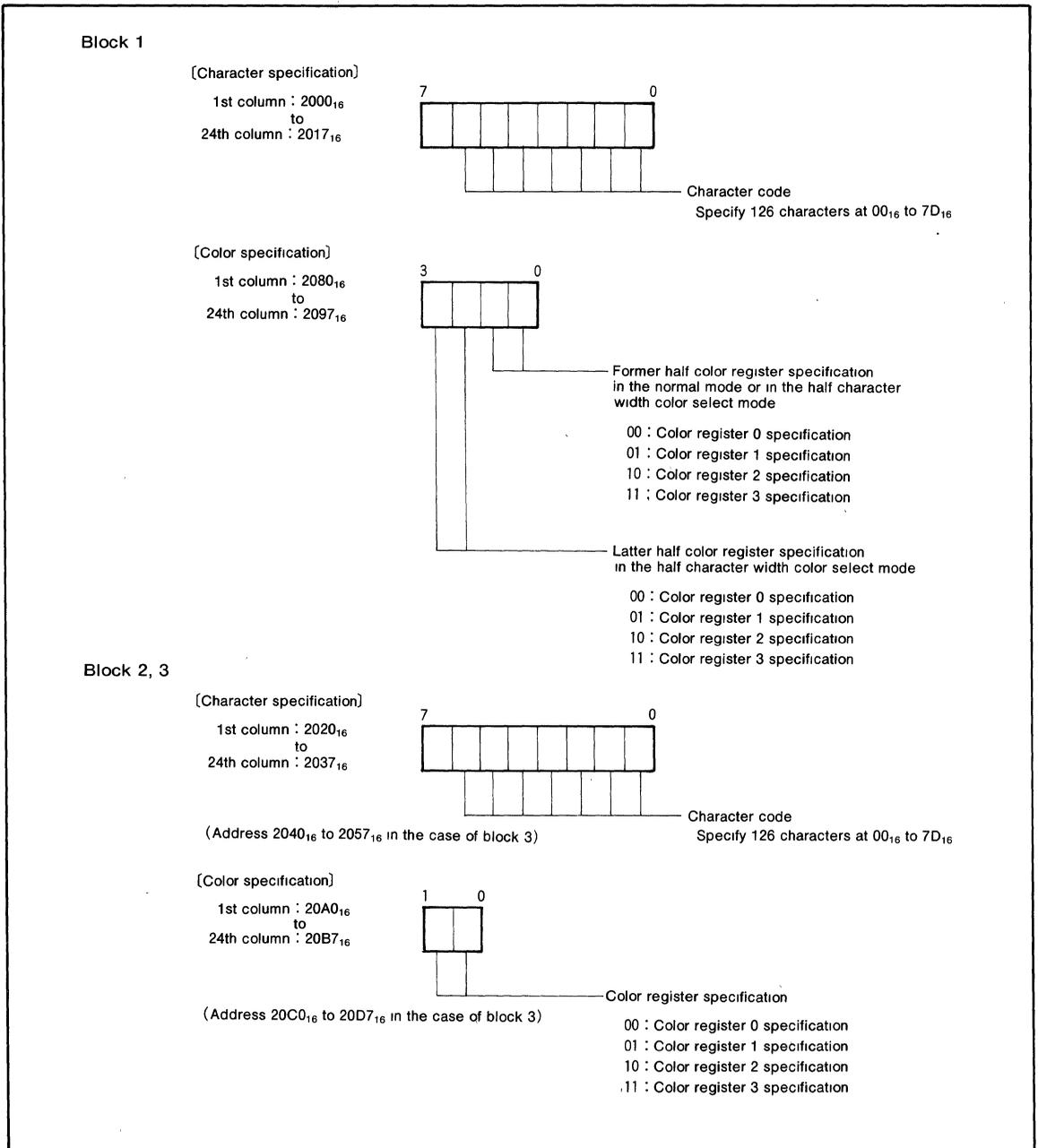


Fig. 32 Structure of the CRT display RAM

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Table 9. Test character patterns 1

Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

Table 10. Test character patterns 2

Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3: addresses 00E6₁₆ to 00E9₁₆) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set 2⁴-1 (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 33 shows the structure of the color register.

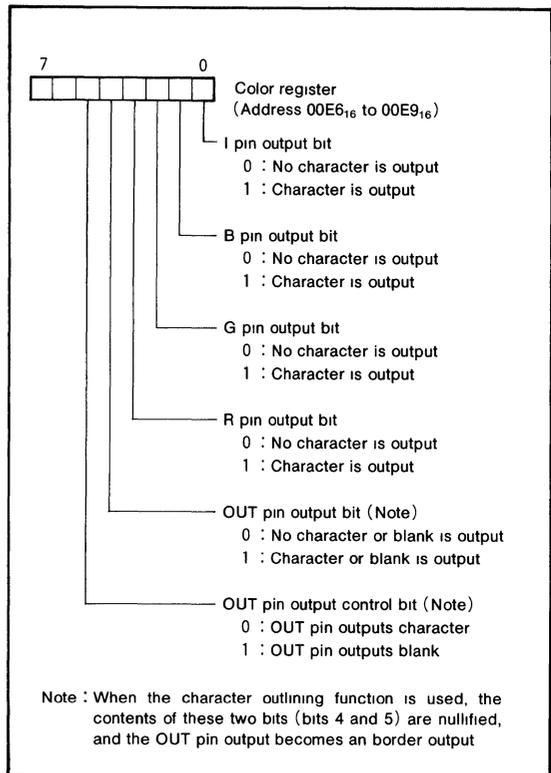


Fig. 33 Structure of color registers

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(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address 00EA₁₆) it is possible to specify colors in units of a half character size (vertical 16 dots X horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080₁₆ to 2097₁₆).

② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080₁₆ to 2097₁₆).

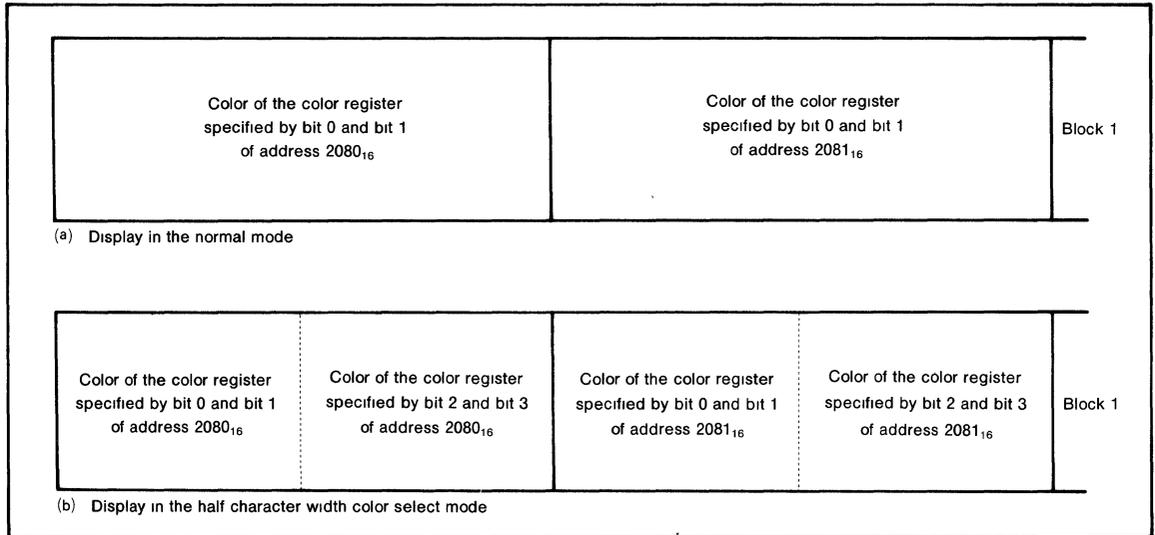


Fig. 34 Difference between normal color select mode and half character width color select mode

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(7) Multiline Display

The M37250M6-XXXSP can normally display three lines on the CRT screen by displaying three blocks at different horizontal positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit=bit 4 at address 00FE₁₆) to "1"), then execute the following processing in the CRT interrupt handling routine.

- ① Read the value of the display block counter.
- ② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.
- ③ Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and display position (contents of vertical position and horizontal position registers) to be displayed next.

Figure 36 shows the structure of the display block counter.

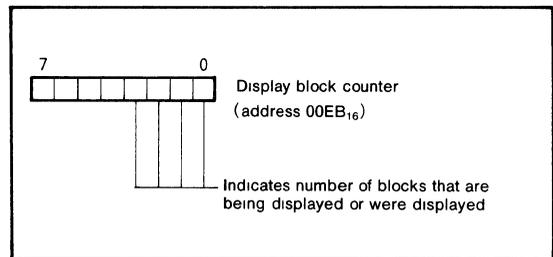


Fig. 36 Structure of display block counter

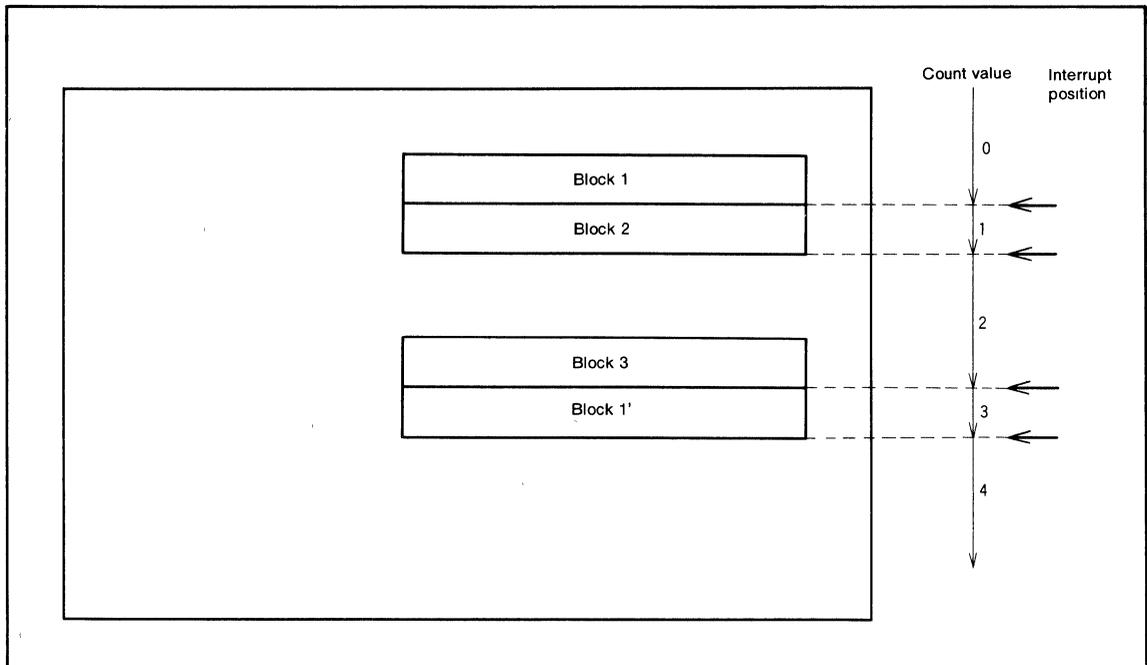


Fig. 35 Timing of CRT interrupt and count value of display block counter

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(8) Scanning Line Double Count Mode

One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended twofold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 128 steps from 00_{16} to $7F_{16}$, or four scanning lines per step, the number of steps in the scanning line double count mode is 64 from 00_{16} to $3F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 40_{16} to $7F_{16}$ in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register (address $00EA_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.

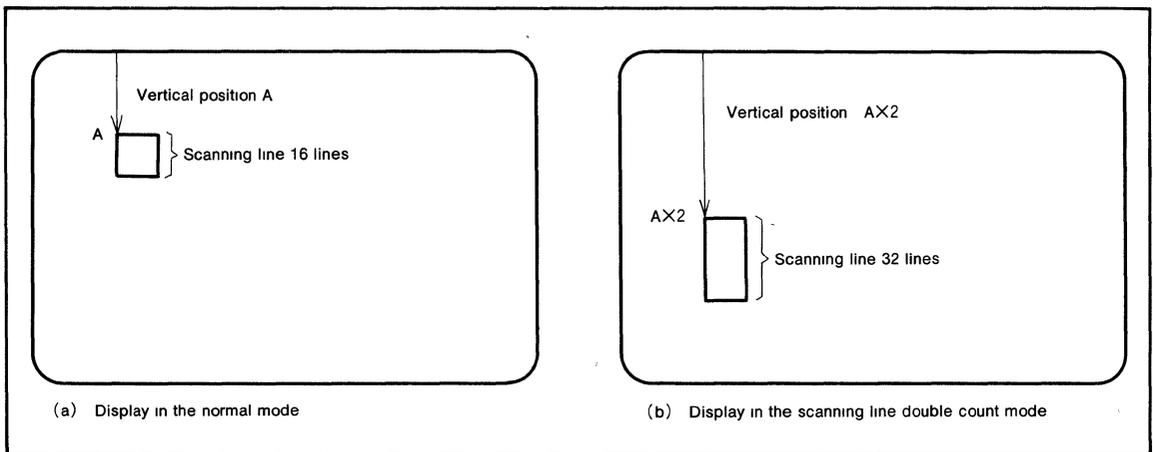


Fig. 37 Display in the normal mode and in the scanning line double count mode

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(9) Character Border Function

A border of a one clock (one dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions.

The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (contents output from the OUT pin) are nullified, and the border is output from the OUT pin instead.

Border can be specified in units of block by using the border select register (address 00E5₁₆). Table 11 shows the relationship between the values set in the border select register and the character border function. Figure 39 shows the structure of the border select register.

Table 11. The relationship between the value set in the border selection register and the character border function

Border selection register		Functions	Example of output
MDn1	MDn0		
X	0	Normal	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border not including character	R, G, B, I output OUT output

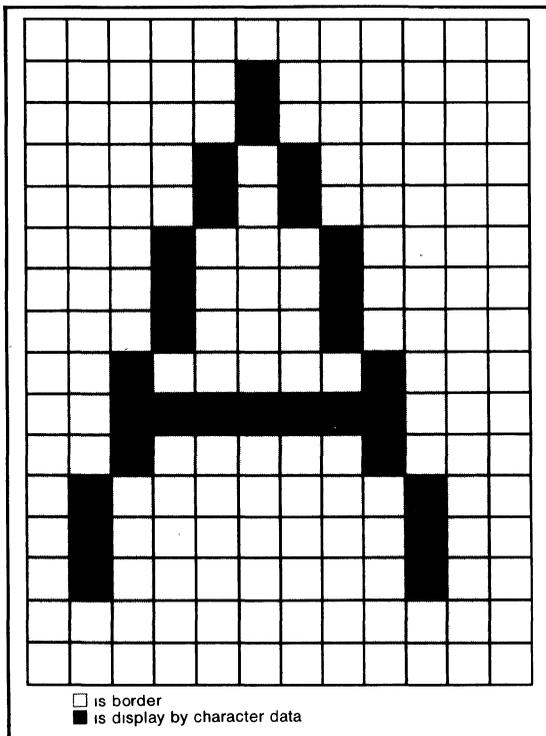


Fig. 38 Example of border

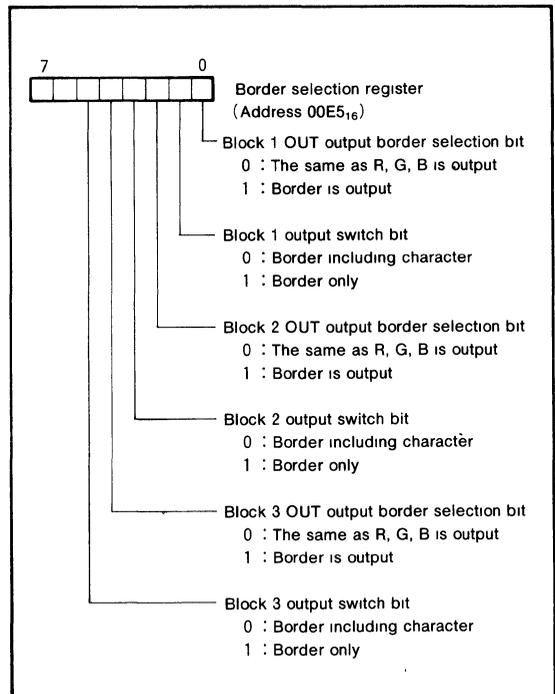


Fig. 39 Structure of border selection register

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(10) CRT Output Pin Control

CRT output pins R, G, B, I, and OUT are respectively shared with port P5₂, P5₃, P5₄, P5₅, and P5₆. The output signal can control by port P5 direction register (address 00CB₁₆) for each port. At reset, because the port P5 direction register is reset, CRT output pins R, G, B, I, and OUT become CRT signal (R, G, B, I, and OUT) output polarity. Bits 0 to 4 of CRT port control register (address 00EC₁₆) can determine H_{SYNC} and V_{SYNC} input polarity and R, G, B, I, and OUT output polarity.

R, G, B, and OUT signal output can be switched to MUTE signal output. MUTE signal can color all displaying area of CRT.

The following is the explain of MUTE signal at MUTE signal output from B output pin for example (refer to Figure 40).

When the MUTE signal is output from B output pin, the all displaying area of CRT is colored blue. Then, a character data is output from R output pin, for example. If B output pin and R output pin are set to "Character is output" by color register at the character "I" output, the output character is colored "RED" mixed "BLUE"

In this case, OUT pin output is not influenced.

At the character "O" output, if only R output pin is set to "Character is output", the output character is colored "RED" only that is not mixed "BLUE".

However at above case, the OUT output pin is necessary to set "Character is output".

The display screen can be also clear by setting the OUT pin to MUTE output. In this case, the MUTE signal is output from OUT pin, that is not influence the setting about OUT pin by CRT display RAM.

R, G, and B output signals are controlled by bits 5 to 7 of CRT port control register, and OUT output signal is controlled by bit 7 (CS7) of character size register. Then, I output pin don't have MUTE output function.

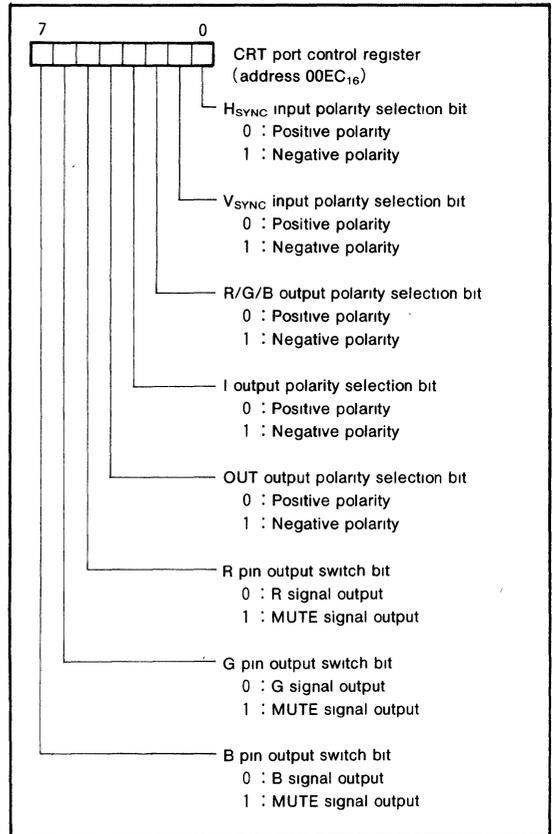


Fig. 41 Structure of CRT port control register

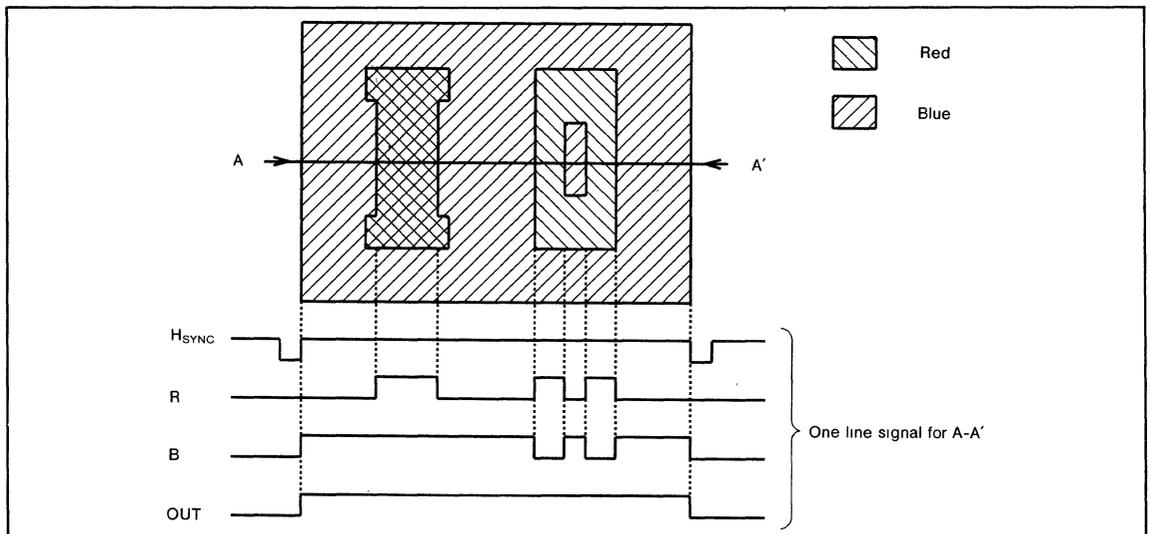


Fig. 40 MUTE signal output example

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

**INTERRUPT INTERVAL DETERMINATION
FUNCTION**

The M37250M6-XXXSP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary counter as shown in Figure 42. Using this counter, it determines a duration of time from the rising transition (falling transition) of an input signal pulse on the INT1 or INT2 to the rising transition (falling transition) of the signal pulse that is input next.

The following describes how the interrupt interval is determined.

1. The interrupt input to be determined (INT1 input or INT2 input) is selected by using bit 2 in the interrupt interval determination control register (address 00D8₁₆). When this bit is cleared to "0", the INT1 input is selected; when the bit is set to "1", the INT2 input is selected.
2. When the INT1 input is to be determined, the polarity is selected by using bit 3 in the interrupt interval determination control register; when the INT2 input is to be determined, the polarity is selected by using bit 4 in the interrupt interval determination control register. When the relevant bit is cleared to "0", determination is made of the interval of a positive polarity (rising

transition); when the bit is set to "1", determination is made of the interval of a negative polarity (falling transition).

3. The reference clock is selected by using bit 1 in the interrupt interval determination control register. When the bit is cleared to "0", a 64 μ s clock is selected; when the bit is set to "1", a 32 μ s clock is selected (based on an oscillation frequency of 4MHz in either case).
4. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT1 pin (or INT2 pin), the 8-bit binary counter starts counting up with the selected reference clock (64 μ s or 32 μ s).
5. Simultaneously with the next input pulse, the value of the 8-bit binary counter is loaded into the determination register (address 00D7₁₆) and the counter is immediately reset (00₁₆). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "00₁₆".
6. When count value "FE₁₆" is reached, the 8-bit binary counter stops counting. Then, simultaneously when the reference clock is input next, the counter sets value "FF₁₆" to the determination register.

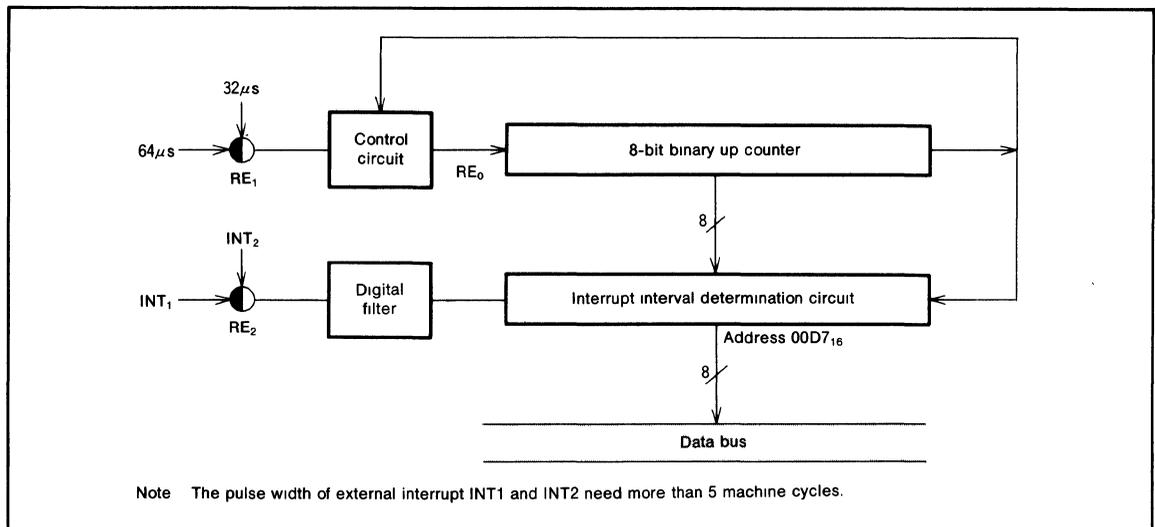


Fig. 42 Block diagram of interrupt interval determination circuit

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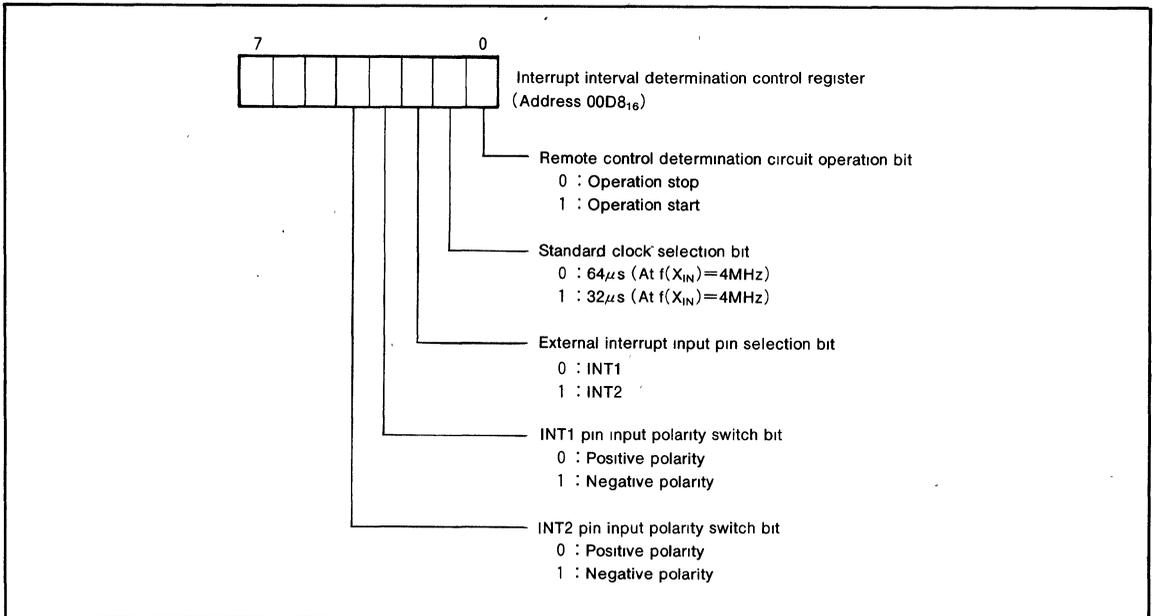


Fig. 43 Structure of interrupt interval determination control register

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
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RESET CIRCUIT

The M37250M6-XXXSP is reset according to the sequence shown in Figure 46. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the RESET pin is held at "L" level for no less than $2\mu s$ while the power voltage is $5V \pm 10\%$

and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 44.

An example of the reset circuit is shown in Figure 45. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

	Address	
(1) Port P0 direction register	(00C1) ₁₆ ...	00 ₁₆
(2) Port P1 direction register	(00C3) ₁₆ ...	00 ₁₆
(3) Port P2 direction register	(00C5) ₁₆ ...	00 ₁₆
(4) Port P3 direction register	(00C7) ₁₆ ...	00 ₁₆
(5) Port P4 direction register	(00C9) ₁₆ ...	00 ₁₆
(6) Port P5 direction register	(00CB) ₁₆ ...	000000
(7) Port P6 direction register	(00CD) ₁₆ ...	000000
(8) PWM output control register 1	(00D5) ₁₆ ...	00 ₁₆
(9) PWM output control register 2	(00D6) ₁₆ ...	00 ₁₆
(10) Interrupt interval determination control register	(00D8) ₁₆ ...	00 ₁₆
(11) Special mode register 1	(00DA) ₁₆ ...	00 ₁₆
(12) Special mode register 2	(00DB) ₁₆ ...	00 ₁₆
(13) Serial I/O mode register	(00DC) ₁₆ ...	00 ₁₆
(14) Serial I/O2 mode register	(00DE) ₁₆ ...	00 ₁₆
(15) Horizontal position register	(00E0) ₁₆ ...	00000000
(16) Color register 0	(00E6) ₁₆ ...	00000000
(17) Color register 1	(00E7) ₁₆ ...	00000000
(18) Color register 2	(00E8) ₁₆ ...	00000000
(19) Color register 3	(00E9) ₁₆ ...	00000000
(20) CRT control register	(00EA) ₁₆ ...	00 ₁₆
(21) Display block counter	(00EB) ₁₆ ...	000000
(22) CRT port control register	(00EC) ₁₆ ...	00000000
(23) A-D control register	(00EF) ₁₆ ...	00000000
(24) Timer 1	(00F0) ₁₆ ...	FF ₁₆
(25) Timer 2	(00F1) ₁₆ ...	07 ₁₆
(26) Timer 3	(00F2) ₁₆ ...	FF ₁₆
(27) Timer 4	(00F3) ₁₆ ...	07 ₁₆
(28) Timer mode register 1	(00F4) ₁₆ ...	00 ₁₆
(29) Timer mode register 2	(00F5) ₁₆ ...	00 ₁₆
(30) CPU mode register	(00FB) ₁₆ ...	11111100
(31) Interrupt request register 1	(00FC) ₁₆ ...	00 ₁₆
(32) Interrupt request register 2	(00FD) ₁₆ ...	000000
(33) Interrupt control register 1	(00FE) ₁₆ ...	00 ₁₆
(34) Interrupt control register 2	(00FF) ₁₆ ...	000000
(35) PLL control register	(0200) ₁₆ ...	00 ₁₆
(36) Timer 5	(0204) ₁₆ ...	FF ₁₆
(37) Timer 6	(0205) ₁₆ ...	07 ₁₆
(38) Processor status register	(PS)	00000100
(39) Program counter	(PC _H)	Contents of address $FFFF_{16}$
	(PC _L)	Contents of address $FFFE_{16}$

Note Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values
 At reset, "0" is read from all bits which is not used

Fig. 44 Internal state of microcomputer at reset

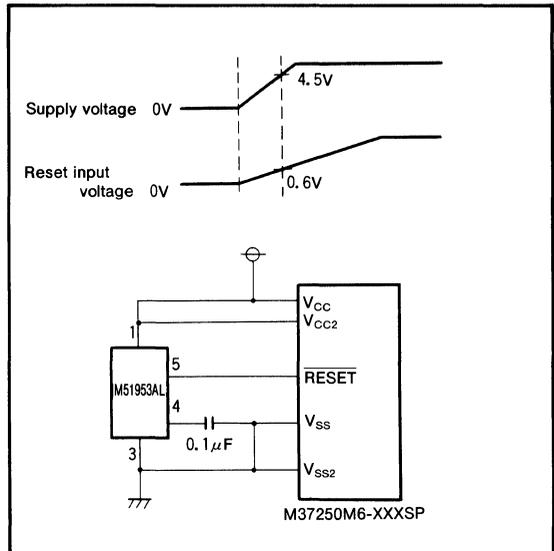


Fig. 45 Example of reset circuit

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 with ON-SCREEN DISPLAY CONTROLLER**

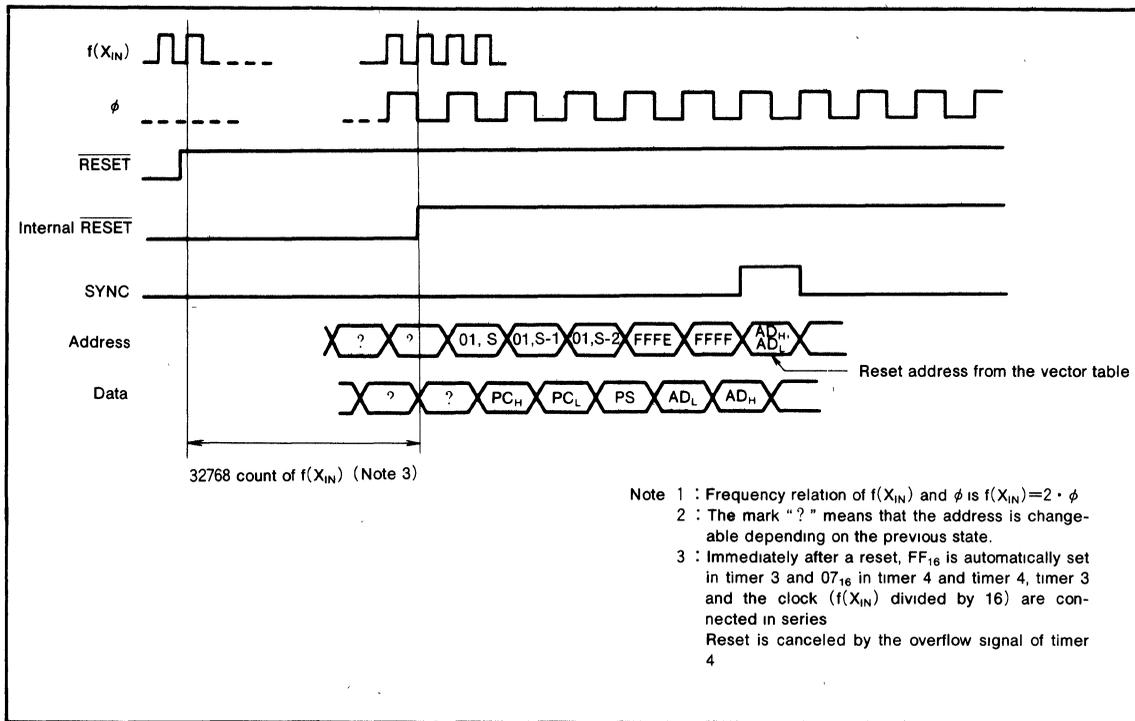


Fig. 46 Timing diagram at reset

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER**

I/O PORTS

- (1) Port P0
Port P0 is an 8-bit I/O port with CMOS output.
As shown in the SFR memory map (Figure 3), port P0 can be accessed at zero page memory address 00C0₁₆.
Port P0 has a direction register (address 00C1₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.
Depending on the contents of the processor mode bits (bit 0 and bit 1 at address 00FB₁₆), three different modes can be selected; single-chip mode, memory expansion mode and microprocessor mode.
In these modes it functions as address (A₇ to A₀) output port (excluding single-chip mode). For more details, see the processor mode information.
- (2) Port P1
In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A₁₅ to A₈) output port.
Refer to the section on processor modes for details.
- (3) Port P2
In single-chip mode, port P2 has the same function as port P0. Port P2₄ to P2₇ are in common with PWM output pins PWM4 to 7. In other modes, it functions as data (D₀ to D₇) input/output port. Refer to the section on processor modes for details
- (4) Port P3
Port P3 is a 7-bit I/O port with function similar to port P0, but the output structure of P3₀, P3₁ is CMOS output and P3₂ to P3₆ is N-channel open drain.
P3₂, P3₃ are in common with the external clock input pins of timer 2 and 3.
P3₄, P3₆ are in common with the external interrupt input pins INT1, INT2 and P3₅, P3₆ are in common with the analog input pins of A-D converter A-D1, A-D2.
In the microprocessor mode or the memory expansion mode, P3₀, P3₁ works as R/W signal output pin and SYNC signal output pin.
- (5) Port P4
Port P4 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.
All pins have program selectable dual functions. When a serial I/O1 function is selected, P4₀ to P4₃ work as input/output pins of serial I/O1. When a serial I/O2 function is selected, P4₄ to P4₇ work as input/output pins of serial I/O2.
In the special serial I/O mode, P4₄, P4₅ work as SDA, SCL pins. P4₆, P4₇ are in common with PWM8 and 9 output pins.
- (6) OSC1, OSC2 pins
Clock input/output pins for CRT display function.
- (7) H_{SYNC}, V_{SYNC} pins
H_{SYNC} is a horizontal synchronizing signal input pin for CRT display.
V_{SYNC} is a vertical synchronizing signal input pin for CRT display.
- (8) R, G, B, I, OUT pins
This is a 5-bit output pin for CRT display and in common with P5₂ to P5₆.
- (9) Port P6
Port P6 is a 4-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.
This port is in common with 8-bit PWM output pin PWM0 to PWM3.
- (10) ϕ pin
The internal system clock (1/2 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".
- (11) MO pin
This pin outputs the mode switching signal of prescaler.
The output structure is CMOS output.
- (12) P/D pin
Phase detector output pin.
- (13) F_{IN} pin
The clock from prescaler is input to this pin.

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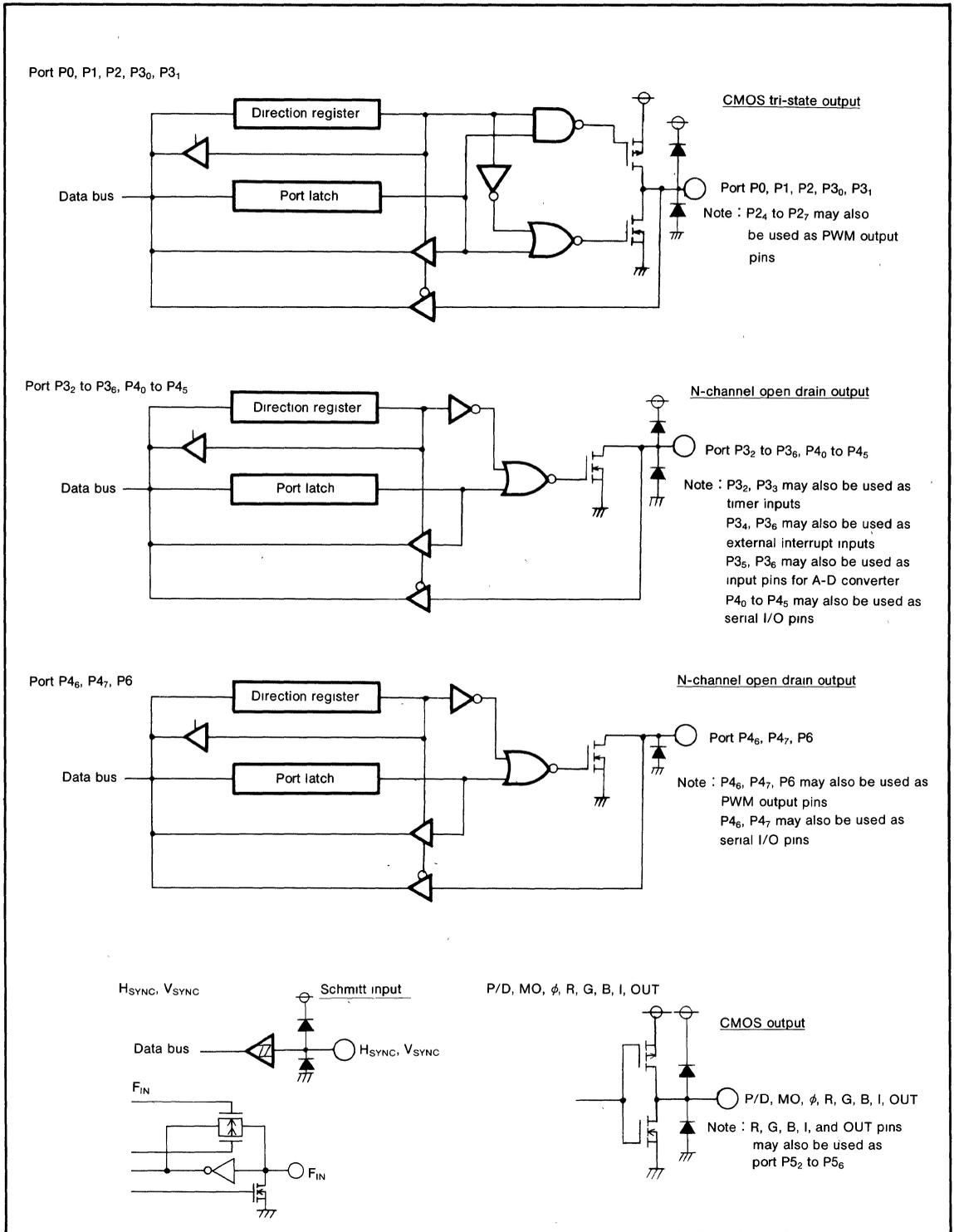


Fig. 47 Block diagram of port P0 to P6 (single-chip mode) and output format of P/D, MO, ϕ , R, G, B, I, OUT, and F_{IN}

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
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PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address 00FB₁₆), three different operation modes can be selected; single-chip mode, memory expansion mode, and microprocessor mode.

In the memory expansion mode and the microprocessor mode, ports P0 to P3 can be used as address, and data input/output pins.

Figure 49 shows the functions of ports P0 to P3.

The memory map for the single-chip mode is illustrated in Figure 2 and for other modes, in Figure 48.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode.

The three different modes are explained as follows:

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0 to P3 will work as original I/O ports.

(2) Memory expansion mode [01]

The microcomputer will be placed in the memory expansion mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost.

Port P2 becomes the data bus of D₇ to D₀ (including instruction code) and loses its normal I/O function. Port P3₀ and P3₁ works as R/W and SYNC.

(3) Microprocessor mode [10]

When CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "10", or after connecting CNV_{SS} to V_{CC} and initiating a reset the microcomputer will automatically default to this mode. In this mode, the internal ROM is inhibited so the external memory is required. Other functions are same as the memory expansion mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 14.

Note : Use the M37250M6-XXXSP in the microprocessor mode or the memory expansion mode only at program development.

The standards is assured only in the single-chip mode.

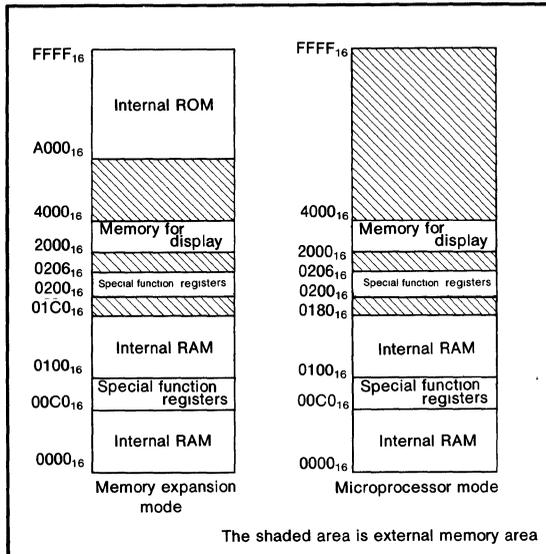


Fig. 48 Example memory area in processor mode

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Port	CM ₁	0	0	1
	CM ₀	0	1	0
Mode		Single-chip mode	Memory expansion mode	Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P3			Same as left	

Fig. 49 Processor mode and function of port P0 to P3

Table 14. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode • Memory expansion mode • Microprocessor mode 	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V _{CC}	<ul style="list-style-type: none"> • Microprocessor mode 	The microprocessor mode is set by the reset

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for FREQUENCY SYNTHESIZER
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CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 52.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timer 3 and timer 4 are connected automatically and FF_{16} is set in the timer 3, 07_{16} is set in the timer 4, and timer 3 count source is forced to $f(X_{IN})$ divided by 16. This connection is cleared when an external interrupt is accepted or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 50.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 51
 X_{IN} is the input, and X_{OUT} is open.

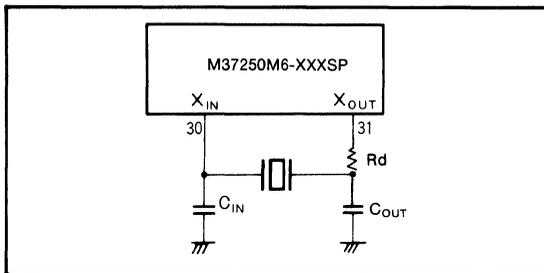


Fig. 50 External ceramic resonator circuit

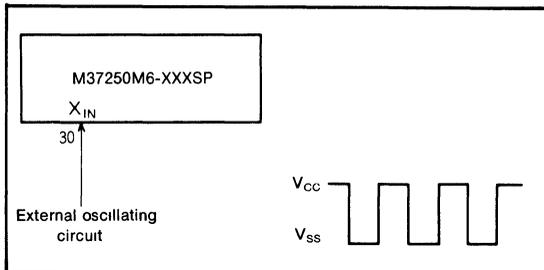


Fig. 51 External clock input circuit

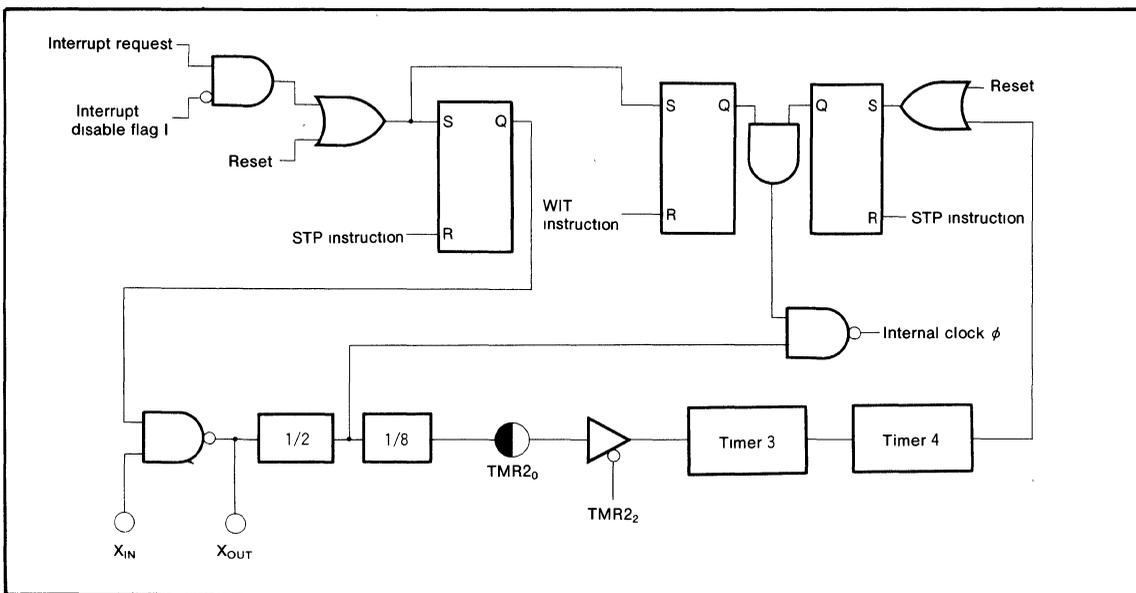


Fig. 52 Block diagram of clock generating circuit

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PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instruction are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (4) A NOP instruction must be used after the execution of a PLP instruction.
- (5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM order confirmation form
- (2) mask specification form
- (3) ROM data EPROM 3 sets

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3 to 6	V
V _I	Input voltage CNV _{SS}		-0.3 to 6	V
V _I	Input voltage P ₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₇ , P ₆₀ -P ₆₃ , H _{SYNC} , V _{SYNC} , RESET, F _{IN}	With respect to V _{SS} Output transistors are at "off" state	-0.3 to V _{CC} +0.3	V
V _O	Output voltage P ₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₅ , R, G, B, I, OUT, P/D, MO, X _{OUT} , OSC2		-0.3 to V _{CC} +0.3	V
V _O	Output voltage P ₄₆ , P ₄₇ , P ₆₀ -P ₆₃		-0.3 to 13.0	V
I _{OH}	Circuit current R, G, B, I, OUT, P ₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ , P ₃₁ , P/D, MO		0 to 1 (Note 1)	mA
I _{OL1}	Circuit current R, G, B, I, OUT, P ₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₃ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₃ , P/D, MO		0 to 2 (Note 2)	mA
I _{OL2}	Circuit current P ₆₀ -P ₆₃ , P ₄₆ , P ₄₇		0 to 1 (Note 2)	mA
I _{OL3}	Circuit current P ₂₄ -P ₂₇		0 to 10 (Note 3)	mA
I _{OL4}	Circuit current P ₄₄ , P ₄₅		0 to 3 (Note 2)	mA
P _d	Power dissipation	T _a =25°C	550	mW
T _{opr}	Operating temperature		-10 to 70	°C
T _{stg}	Storage temperature		-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=-10 to 70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max	
V _{CC}	Supply voltage (Note 4) During the PLL, CRT operation	4.5	5.0	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	"H" input voltage P ₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₃ , P ₄₆ , P ₄₇ , P ₆₀ -P ₆₃ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₄₄ , P ₄₅	0.7V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ , P ₃₁ , P ₃₅ , P ₄₀ , P ₄₃ -P ₄₅ , P ₄₇ , P ₆₀ -P ₆₃	0		0.4V _{CC}	V
V _{IL}	"L" input voltage P ₃₂ -P ₃₄ , P ₃₆ , P ₄₁ , P ₄₂ , P ₄₆ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0		0.2V _{CC}	V
I _{OH}	"H" average output current (Note 1) R, G, B, I, OUT, P ₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ , P ₃₁ , P/D, MO			1	mA
I _{OL1}	"L" average output current (Note 2) R, G, B, I, OUT, P ₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₃ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₃ , P/D, MO			2	mA
I _{OL2}	"L" average output current (Note 2) P ₆₀ -P ₆₃ , P ₄₆ , P ₄₇			1	mA
I _{OL3}	"L" average output current (Note 3) P ₂₄ -P ₂₇			10	mA
I _{OL4}	"L" average output current (Note 2) P ₄₄ , P ₄₅			3	mA
f _{CPU}	Oscillating frequency (for CPU operation) (Note 5)	3.6	4.0	4.4	MHZ
f _{CRT}	Oscillating frequency (for CRT display)	6.0	7.0	8.0	MHZ
f _{HS}	Input frequency P ₃₂ -P ₃₄ , P ₃₆ , P ₄₅			100	KHZ
f _{HS}	Input frequency P ₄₁			1	MHZ
f _{HS}	Input frequency F _{IN} V _I =0.6 V _{PP}	Sine wave	1.0	15	MHZ
		Square wave	0.1	15	MHZ

- Note 1 : The total current that flows out of the IC should be 20mA (max).
 2 : The total of I_{OL1}, I_{OL2}, and I_{OL4} should be 30mA (max).
 3 : The total of I_{OL} of port P₂₄-P₂₇ should be 20mA (max).
 4 : Apply 0.15μF or greater capacitance externally between the V_{CC}-V_{SS} power supply pins so as to reduce power source noise. Apply 0.15μF or greater capacitance externally between the V_{CC2}-V_{SS2} as same.
 Also apply 0.15μF or greater capacitance externally between the V_{CC}-CNV_{SS} pins.
 5 : Use the quartz crystal oscillator for CPU oscillation circuit.

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ELECTRIC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10$ to $70^\circ C$, $f(X_{IN})=4MHz$ unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT OFF		10	20	mA
		$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT ON, PLL ON		25	35	
		At wait mode $V_{CC}=5.0V$		500	800	μA
		At stop mode $V_{CC}=5.0V$		1	10	μA
V_{OH}	"H" output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ , P3 ₁ , R, G, B, I, OUT, P/D, MO	$V_{CC}=4.5V$ $I_{OH}=-0.5mA$	2.4			V
V_{OL}	"L" output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₃ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₃ , R, G, B, I, OUT, P/D, MO	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
	"L" output voltage P6 ₀ -P6 ₃ , P4 ₆ , P4 ₇	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	
	"L" output voltage P2 ₄ -P2 ₇	$V_{CC}=4.5V$ $I_{OL}=10mA$			3.0	
	"L" output voltage P4 ₄ , P4 ₅	$V_{CC}=4.5V$ $I_{OL}=3mA$			0.4	
$V_{T+}-V_{T-}$	Hysteresis RESET	$V_{CC}=5.0V$		0.5	0.7	V
	Hysteresis (Note) H _{SYNC} , V _{SYNC} , P3 ₂ -P3 ₄ , P3 ₆ , P4 ₁ , P4 ₂ , P4 ₄ -P4 ₆	$V_{CC}=5.0V$		0.5	1.3	
I_{OZH}	"H" input leak current RESET, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₅	$V_{CC}=5.5V$ $V_O=5.5V$			5	μA
	"H" input leak current P6 ₀ -P6 ₃ , P4 ₆ , P4 ₇	$V_{CC}=5.5V$ $V_O=12V$			10	
	"H" input leak current P/D	$V_{CC}=5.5V$ $V_O=5.5V$			1	
I_{OZL}	"L" input leak current RESET, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₇ , P6 ₀ -P6 ₃	$V_{CC}=5.5V$ $V_O=0V$			5	μA
	"L" input leak current P/D	$V_{CC}=5.5V$ $V_O=0V$			1	

Note 1. P3₂-P3₄, P3₆ have the hysteresis when these pins are used as interrupt input pins or timer input pins.
P4₁, P4₂, P4₄-P4₆ have the hysteresis when these pins are used as serial I/O ports

PRELIMINARY

MITSUBISHI MICROCOMPUTERS M37260M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

DESCRIPTION

The M37260M6-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP. This single-chip microcomputer is useful for the high-tech on-screen display system for TVs.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

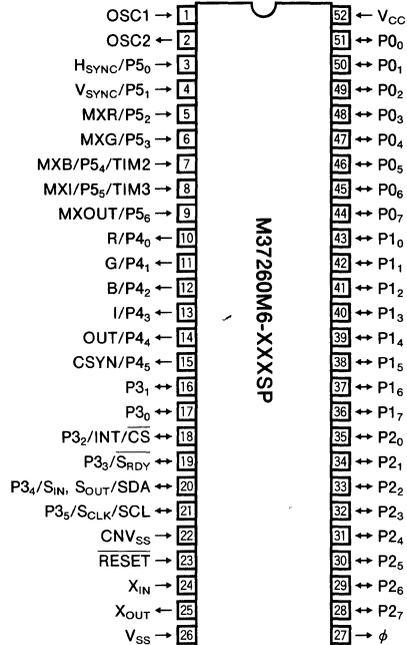
FEATURES

- Number of basic instructions..... 69
- Memory size ROM24576 bytes
RAM..... 320 bytes
CRT ROM.....20480 bytes
CRT RAM..... 280 bytes
- Instruction execution time
.....0.5 μ s (minimum instructions at 8MHz frequency)
- Single power supply.....5V \pm 10%
- Power dissipation
(normal operation mode at 4MHz frequency)
..... 110mW (V_{CC} =5.5V, CRT display)
- Subroutine nesting 96 levels (Max.)
- Interrupt..... 11 types, 11 vectors
- 8-bit timer..... 4
- Programmable I/O ports
(Ports P0, P1, P2, P3)..... 30
- Output port (Port P4)..... 6
- Input port (Port P5)..... 7
- Serial I/O (maximum 64-bit) 1
- CRT display function
Display characters..... 40 characters \times 3 lines
(25 lines max.)
Dot structure 12 \times 20 dots or 16 \times 20 dots
Character types 510 types
Character size30 types
(minimum dot width is 1/2 scanning line)
Color types..... Max 16 types (R, G, B, I)
Character unit/blank of line unit/raster can be specified
Display layout
Horizontal..... 256 levels
Vertical.....1024 levels

APPLICATION

TV

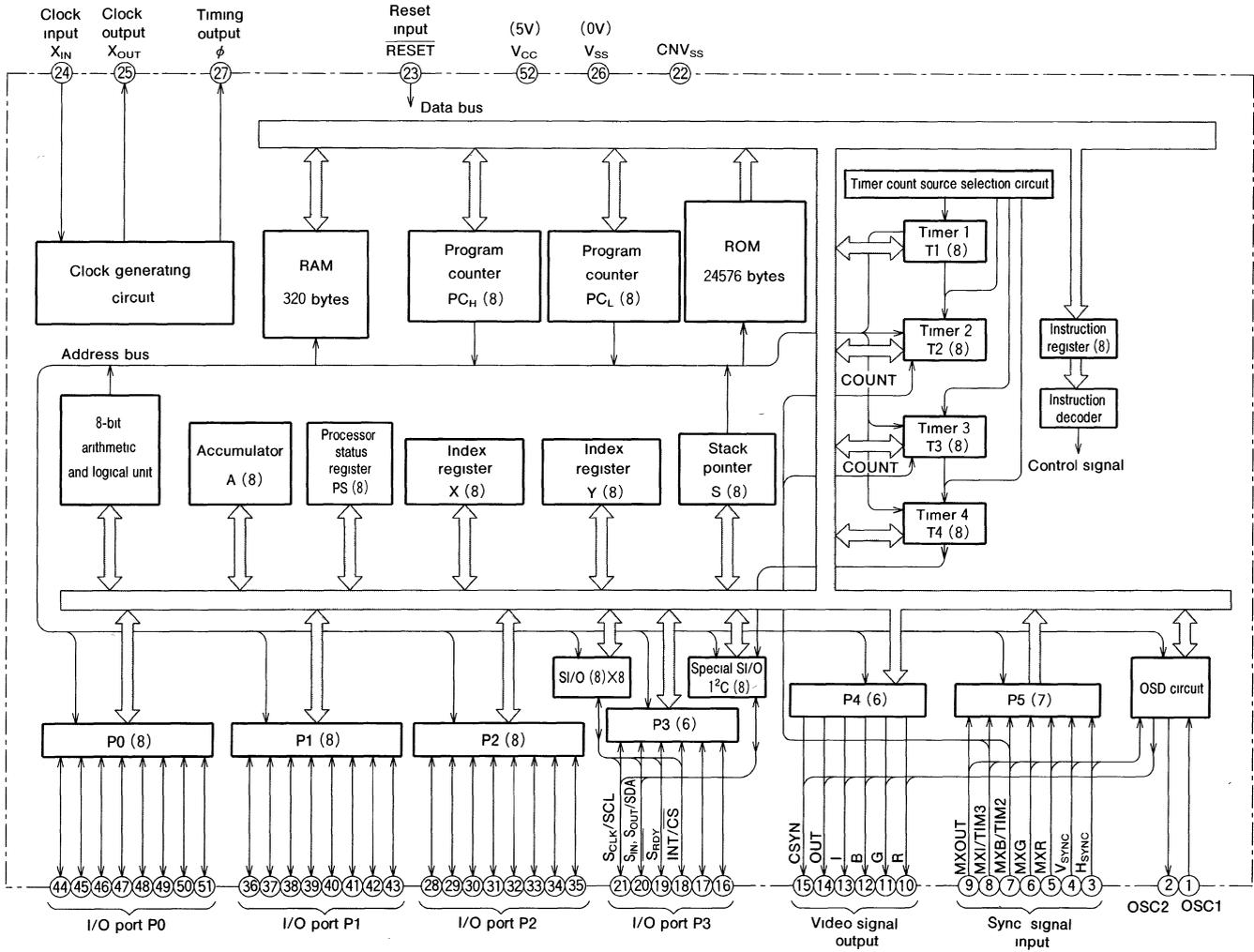
PIN CONFIGURATION (TOP VIEW)



Outline 52P4B



M37260M6-XXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

MITSUBISHI MICROCOMPUTERS
M37260M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

FUNCTIONS OF M37260M6-XXXSP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		0.5 μ s (minimum instructions, at 8MHz frequency)	
Clock frequency		8MHz (maximum)	
Memory size	ROM	24576 bytes	
	RAM	320 bytes	
	CRT ROM	20480 bytes	
	CRT RAM	280 bytes	
Input/Output ports	P0, P1, P2	I/O	8-bit \times 3 (CMOS output)
	P3 ₀ , P3 ₁	I/O	2-bit \times 1 (CMOS output)
	P3 ₂ —P3 ₅	I/O	4-bit \times 1 (can be used as serial I/O pins and external interrupt pin) (N-channel open drain output)
	P4	Output	6-bit \times 1 (can be used as R, G, B, I, OUT, and CSYN pins) (CMOS output)
	P5	Input	7-bit \times 1 (can be used as H _{SYNC} , V _{SYNC} , MXR, MXG, MXB, MXI, and MXOUT pins)
Serial I/O		64-bit (maximum) \times 1, Special serial I/O (8-bit) \times 1	
Timers		8-bit timer \times 4	
Subroutine nesting		96 levels (maximum)	
Interrupt		One external interrupt, eight internal interrupts, one software interrupt	
CRT display function	Display characters	40 characters \times 3 lines (maximum 25 lines in program)	
	Dot structure	12 \times 20 dots or 16 \times 20 dots	
	Characters types	510 types	
	Character size	30 types (minimum dot width is 1/2 scanning line)	
	Color types	Max. 16 types (R, G, B, I)	
Display layout		Horizontal 256 levels, Vertical 1024 levels	
Clock generating circuit		Two built-in circuits (externally connected ceramic or quartz crystal oscillator)	
Supply voltage		5V \pm 10%	
Power dissipation	at CRT display ON	110mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)	
	at CRT display OFF	55mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)	
	at stop mode	1.65mW (maximum)	
Memory expansion		Possible	
Operating temperature range		-10 to 70°C	
Device structure		CMOS silicon gate process	
Package		52-pin shrink plastic molded DIP	

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is connected to V _{SS} .
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is a timing output pin.
P0 ₀ —P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
P1 ₀ —P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
P2 ₀ —P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
P3 ₀ —P3 ₅	I/O port P3	I/O	Port P3 is a 6-bit I/O port and has basically the same functions as port P0, but the output structure of P3 ₀ and P3 ₁ is CMOS output and the output structure of P3 ₂ —P3 ₅ is N-channel open drain. P3 ₂ is in common with external interrupt input pin INT. When serial I/O is used, P3 ₂ , P3 ₃ , P3 ₄ , and P3 ₅ work as CS, S _{RDY} , S _{IN} /S _{OUT} , and S _{CLK} pins, respectively. When special serial I/O is used, P3 ₄ and P3 ₅ work as SDA and SCL pins, respectively.
OSC1	Clock input for CRT display	Input	There are I/O pins of the clock generating circuit for the CRT display function.
OSC2	Clock output for CRT display	Output	
H _{SYNC}	H _{SYNC} input	Input	This is a horizontal synchronizing signal input for CRT display. This pin is in common with input Port P5 ₀ .
V _{SYNC}	V _{SYNC} input	Input	This is a vertical synchronizing signal input for CRT display. This pin is in common with input Port P5 ₁ .
MXR, MXG, MXB, MXI, MXOUT	Video signal input for mixing	Input	These are video signal input pins. MXR, MXG, MXB, MXI, and MXOUT are in common with P5 ₂ , P5 ₃ , P5 ₄ , P5 ₅ , and P5 ₆ . Also P5 ₄ and P5 ₅ are in common with external clock input pins TIM2 and TIM3.
R, G, B, I, OUT	Video signal output	Output	This is a 5-bit output pin for CRT display. The output structure is CMOS output. R, G, B, I, and OUT are in common with P4 ₀ , P4 ₁ , P4 ₂ , P4 ₃ , and P4 ₄ .
CSYN	Composite sync signal output	Output	This is a composite sync signal output pin, and in common with output port P4 ₅ .

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37260 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address 00FB₁₆. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

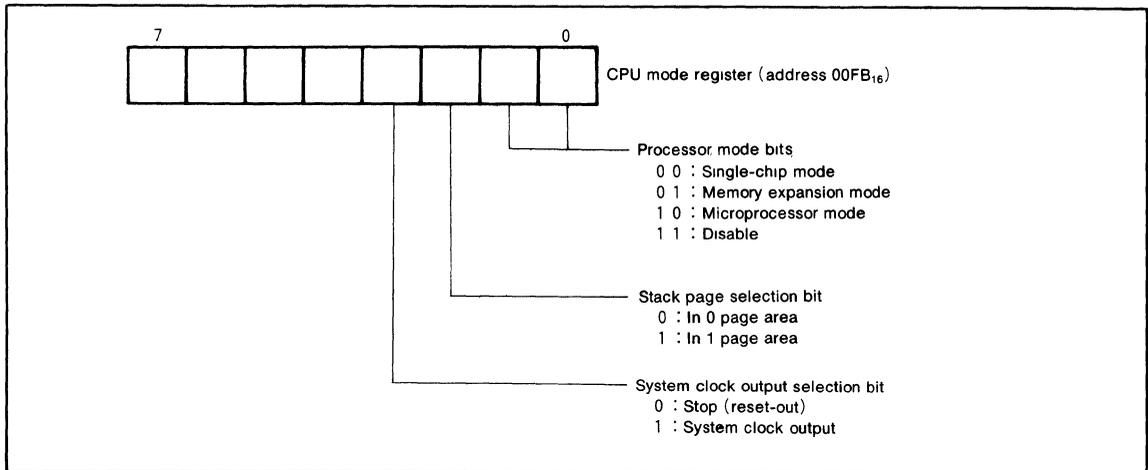


Fig. 1 Structure of CPU mode register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

MEMORY

- Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- RAM

RAM is used for data storage as well as a stack area.

- ROM

ROM is used for storing user programs as well as the interrupt vector area.

- RAM for display

RAM for display is used for specifying the character codes and colors to display.

- ROM for display

ROM for display is used for storing character data.

- Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

- Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

- Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

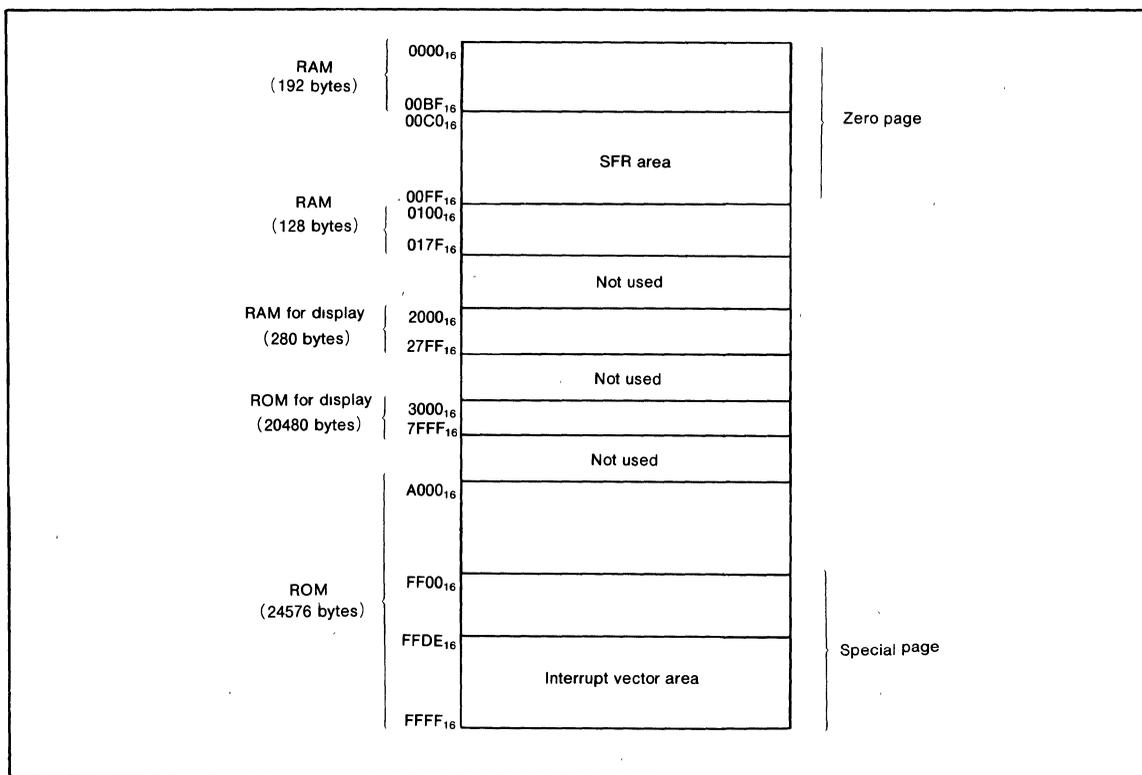


Fig. 2 Memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

00C0 ₁₆	Port P0
00C1 ₁₆	Port P0 direction register
00C2 ₁₆	Port P1
00C3 ₁₆	Port P1 direction register
00C4 ₁₆	Port P2
00C5 ₁₆	Port P2 direction register
00C6 ₁₆	Port P3
00C7 ₁₆	Port P3 direction register
00C8 ₁₆	Port P4
00C9 ₁₆	Port P4 mode register
00CA ₁₆	Port P5
00CB ₁₆	
00CC ₁₆	
00CD ₁₆	Serial I/O mode register 1
00CE ₁₆	Serial I/O mode register 2
00CF ₁₆	Serial I/O register 0
00D0 ₁₆	Serial I/O register 1
00D1 ₁₆	Serial I/O register 2
00D2 ₁₆	Serial I/O register 3
00D3 ₁₆	Serial I/O register 4
00D4 ₁₆	Serial I/O register 5
00D5 ₁₆	Serial I/O register 6
00D6 ₁₆	Serial I/O register 7
00D7 ₁₆	Character size register 1 (block 1)
00D8 ₁₆	Character size register 2 (block 2)
00D9 ₁₆	Character size register 3 (block 3)
00DA ₁₆	Blank control register 1 (block 1)
00DB ₁₆	Blank control register 2 (block 2)
00DC ₁₆	Blank control register 3 (block 3)
00DD ₁₆	Block 1 interrupt occurrence position control register
00DE ₁₆	Block 2 interrupt occurrence position control register
00DF ₁₆	Block 3 interrupt occurrence position control register
00E0 ₁₆	Horizontal position register
00E1 ₁₆	Vertical position register 1 (block 1)
00E2 ₁₆	Vertical position register 2 (block 2)
00E3 ₁₆	Vertical position register 3 (block 3)
00E4 ₁₆	Vertical position register 4 (block 1 to 3)
00E5 ₁₆	Mixing circuit control register
00E6 ₁₆	
00E7 ₁₆	
00E8 ₁₆	CRT input polarity register
00E9 ₁₆	Sync. generator control register
00EA ₁₆	CRT control register
00EB ₁₆	Display block counter
00EC ₁₆	CRT output polarity register
00ED ₁₆	Wipe mode register
00EE ₁₆	Wipe start register
00EF ₁₆	
00F0 ₁₆	Timer 1
00F1 ₁₆	Timer 2
00F2 ₁₆	Timer 3
00F3 ₁₆	Timer 4
00F4 ₁₆	Timer 12 mode register
00F5 ₁₆	Timer 34 mode register
00F6 ₁₆	Special serial I/O register
00F7 ₁₆	Special mode register 1
00F8 ₁₆	Special mode register 2
00F9 ₁₆	
00FA ₁₆	
00FB ₁₆	CPU mode register
00FC ₁₆	Interrupt request register 1
00FD ₁₆	Interrupt request register 2
00FE ₁₆	Interrupt control register 1
00FF ₁₆	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

INTERRUPTS

Interrupts can be caused by 10 different events consisting of two external, seven internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Interrupt Causes

- (1) V_{SYNC} and CRT interrupts

The V_{SYNC} interrupt is an interrupt request synchronized with the vertical synchronization signal.

The CRT interrupt is generated after character block display to the CRT is completed.

- (2) INT interrupt

With an external interrupt input, the system detects that the level of a pin changes from "L" to "H" or from "H" to "L", and generates an interrupt request. The input active edge can be selected by bit 5 of the CRT input active edge register (address 00E8₁₆): when this bit is "0", a change from "L" to "H" is detected; when it is "1", a change from "H" to "L" is detected. Note that all bits are cleared to "0" at reset.

- (3) Timer 1, 2, 3 and 4 interrupts

An interrupt is generated by an overflow of timer 1, 2, 3, or 4.

- (4) Serial I/O interrupt

This is an interrupt request from the clock-synchronized serial I/O function.

Note that serial I/O or special serial I/O is selected by bit 3 of the serial I/O mode register 2 (address 00CE₁₆).

- (5) 1 ms interrupt

This interrupt is generated regularly with a 1024 μ s period. When the X_{IN} clock is 4MHz, set bits 7 and 4 of the sync generator control register to "0". When the X_{IN} clock is 8MHz, set bit 7 of the sync generator control register to "0" and bit 4 to "1".

- (6) BRK instruction interrupt

This interrupt has the lowest priority of all software interrupts. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag (non-maskable).

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	FFF ₁₆ , FFE ₁₆	Non-maskable
CRT interrupt	2	FFD ₁₆ , FFC ₁₆	
INT interrupt	3	FFB ₁₆ , FFA ₁₆	External interrupt
Serial I/O interrupt	4	FF9 ₁₆ , FF8 ₁₆	
1 ms interrupt	5	FF7 ₁₆ , FF6 ₁₆	
Timer 4 interrupt	6	FF5 ₁₆ , FF4 ₁₆	
V _{SYNC} interrupt	7	FF3 ₁₆ , FF2 ₁₆	External interrupt
Timer 3 interrupt	8	FF1 ₁₆ , FF0 ₁₆	
Timer 2 interrupt	9	FFE ₁₆ , FFE ₁₆	
Timer 1 interrupt	10	FFD ₁₆ , FFEC ₁₆	
BRK instruction interrupt	11	FFD ₁₆ , FFDE ₁₆	Non-maskable software interrupt

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

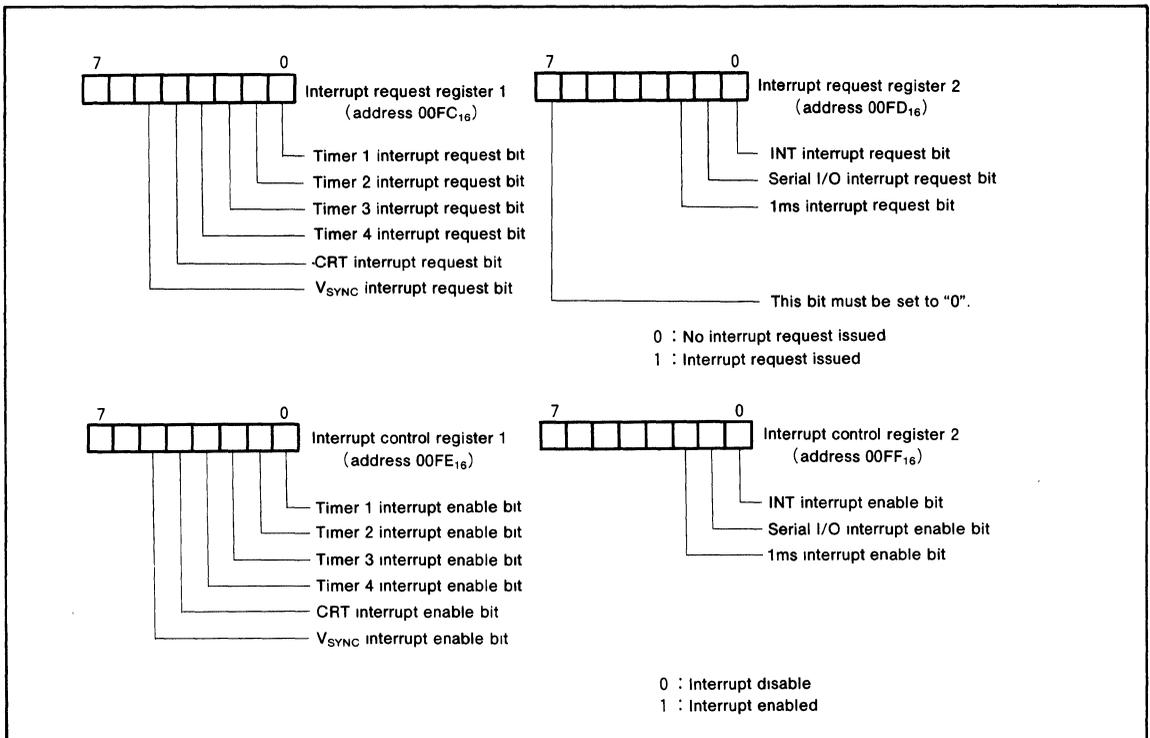


Fig. 4 Structure of registers related to interrupt

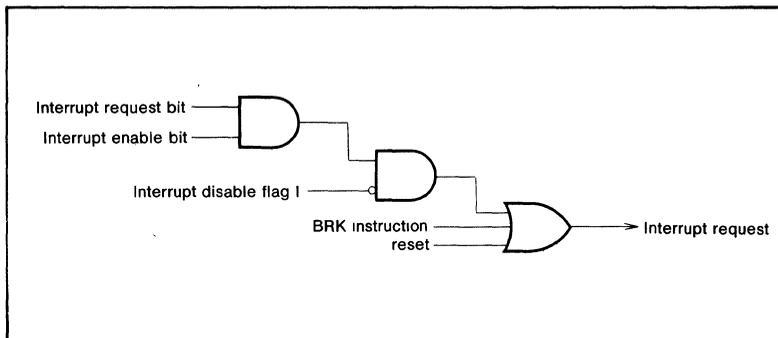


Fig. 5 Interrupt control

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

TIMER

The M37260M6-XXXSP has four timers; timer 1, timer 2, timer 3 and timer 4. All of timers are 8-bit structure and have 8-bit latches.

A block diagram of timer 1 through 4 is shown in Figure 7. All of the timers are down count timers and their division ratio are $1/(n+1)$, where n is the contents of timer latch. The same value is set to timer by writing the count value to the latch (addresses 00F0₁₆ to 00F3₁₆: timer 1 to timer 4) When a timer reaches "00₁₆" and the next count pulse is input to a timer, a value which is the contents of the reload latch are loaded into the timer. The timer interrupt request bit is set at the next count pulse after the timer reaches "00₁₆".

The contents of each timer is shown in following.

(1) Timer 1

Either $f(X_{IN})$ divided by 16 or a 1024 μ s clock can be selected as the count source of timer 1.

(When the X_{IN} clock is 4MHz, set bits 7 and 4 of the sync generator control register (address 00E9₁₆) to "0". When the X_{IN} clock is 8MHz, set bit 7 of the sync generator control register to "0" and bit 4 to "1".) When bit 0 of the timer 12 mode register (address 00F4₁₆) is "0", $f(X_{IN})$ divided by 16 is selected; when it is "1", the 1024 μ s clock is selected.

Timer 1 interrupt request is occurred with timer 1 overflow

(2) Timer 2

$f(X_{IN})$ divided by 16, timer 1 overflow signal, or an external clock input from P5₄/MXB/TIM2 pin can be selected as the count source of timer 2 by specifying bit 4 and 1 of the timer 12 mode register (address 00F4₁₆).

Timer 2 interrupt request is occurred with timer 2 overflow.

(3) Timer 3

Either $f(X_{IN})$ divided by 16 or an external clock input from P5₅/MXI/TIM3 pin can be selected as the count source of timer 3 by specifying bit 0 of the timer 34 mode register (address 00F5₁₆).

Timer 3 interrupt request is occurred with timer 3 overflow.

(4) Timer 4

$f(X_{IN})$ divided by 16, $f(X_{IN})$ divided by 2, or timer 3 overflow signal can be selected as the count source of timer 4 by specifying bit 4 and 1 of the timer 34 mode register (address 00F5₁₆).

Timer 4 interrupt request is occurred with timer 4 overflow. And the timer 4 overflow signal can be used as the clock source of special serial I/O.

At reset or an STP instruction is executed, timer 3 and timer 4 are connected automatically, and the value "FF₁₆" is set to timer 3, and the value "07₁₆" is set to timer 4

$f(X_{IN})$ divided by 16 is selected as count source of tim-

er 3.

When the internal reset is removed or stop mode is removed, the internal clock is connected by timer 6 overflow at above state. In this reason, the program starts with stable clock.

The timer related registers structure is shown in Figure 6.

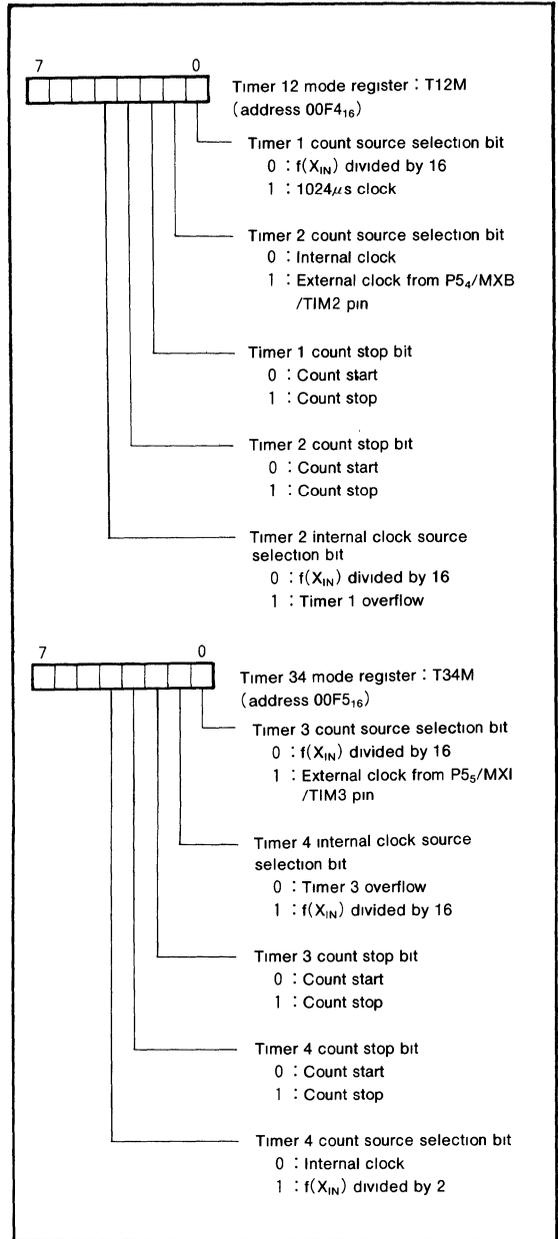


Fig. 6 Structure of timer 12 mode register and timer 34 mode register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

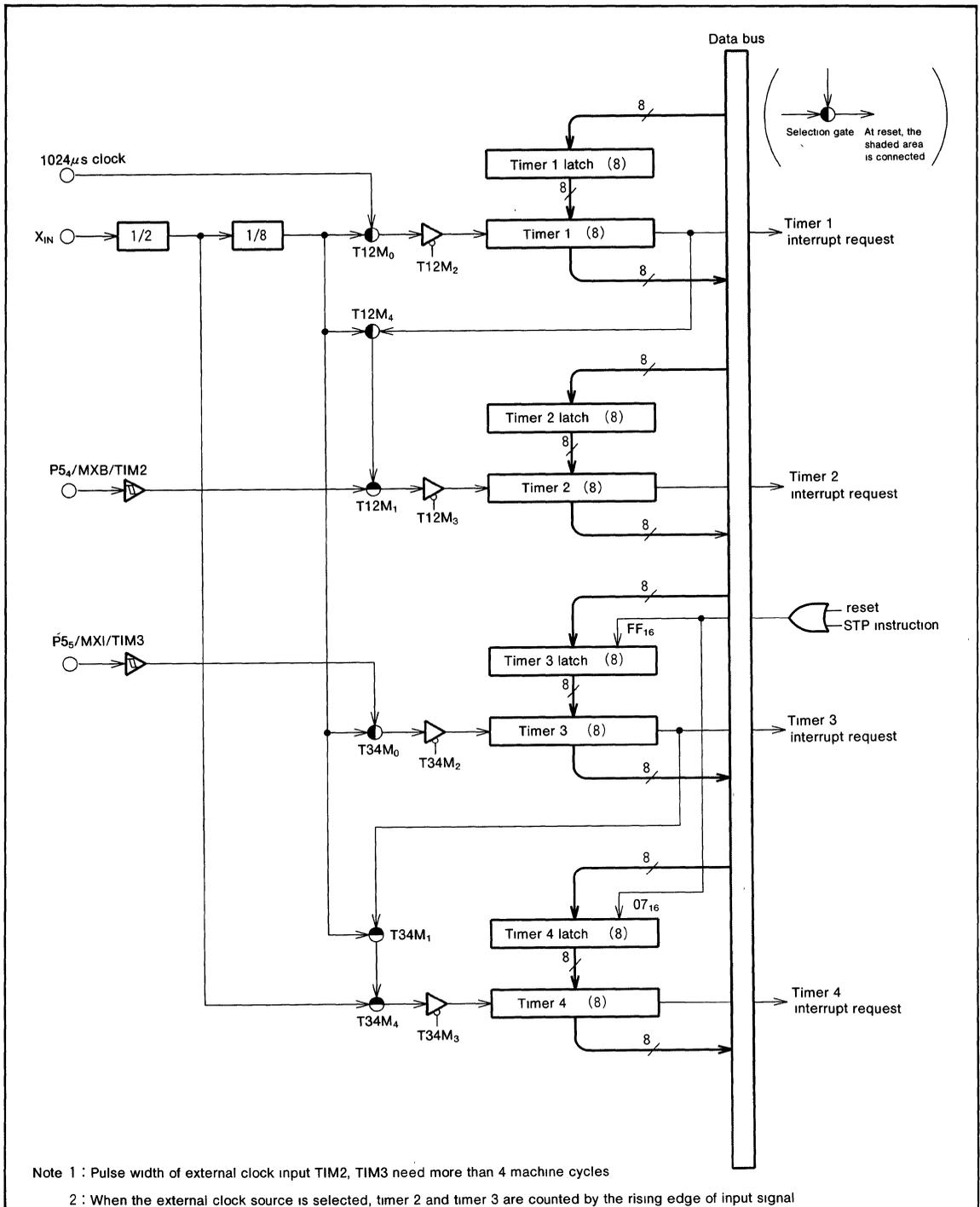


Fig. 7 Block diagram of timer 1, timer 2, timer 3 and timer 4

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

SERIAL I/O

The M37260M6-XXXSP has a built-in serial I/O function that can either transmit or receive up to 64-bits of serial data in clock-synchronized form. The serial I/O function can transfer up to 64 bits of data in 8-bit units according to the setting of the serial I/O shift register.

A block diagram of the serial I/O function is shown in Fig. 8. The serial I/O receive enabled signal pin ($\overline{S_{RDY}}$), synchronization clock I/O pin (S_{CLK}), and data I/O pins (S_{OUT} and S_{IN}) also function as the P3 port.

Bit 2 of the serial I/O mode register 1 (address 00CD₁₆) selects whether the synchronization clock is supplied internally or externally (from the S_{CLK} pin) and, if the internal clock is selected, bits 1 and 0 select whether $f(X_{IN})$ is divided by 8, 16, 32, or 64. Bits 4 and 3 select whether port P3 is used for serial I/O. Bits 2, 1, and 0 of the serial I/O mode register 2 select the count of the transfer clock at which the serial I/O interrupt request is generated. The operation of the serial I/O function is described below.

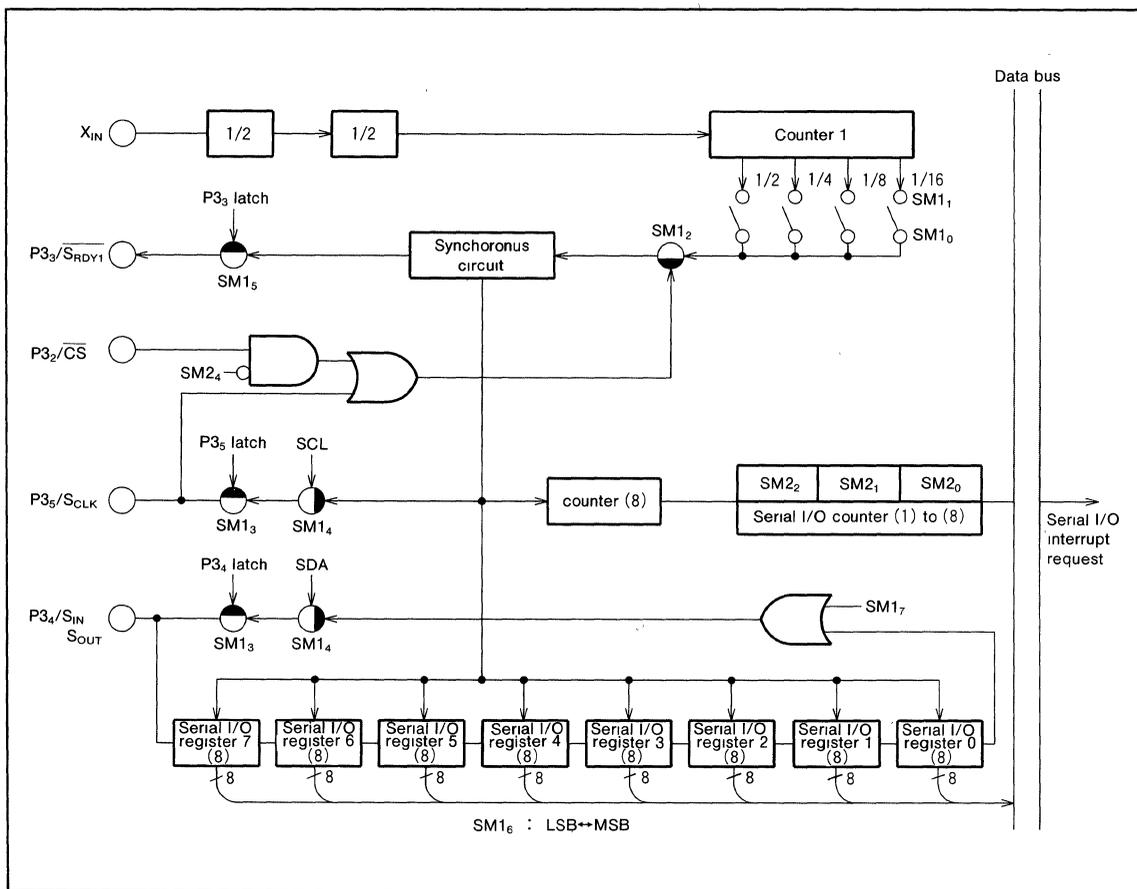


Fig. 8 Block diagram of serial I/O

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

If the serial I/O register 0 (address 00CF₁₆) is written to, the $\overline{S_{RDY}}$ signal is at "H" during the write cycle; it then goes "L" when the write cycle ends to indicate reception enabled status. If the serial I/O register's transfer clock goes "L" even once, the $\overline{S_{RDY}}$ signal goes "H". During the write cycle to the serial I/O register 0, the value set in the serial I/O mode register 2 is set in the serial I/O counter, and the serial I/O register's transfer clock is forced to "H". After the write cycle ends, the data in each register is shifted one bit in sequence from serial I/O register 0 to serial I/O register 1, serial I/O register 2, serial I/O register 3, serial I/O register 4, serial I/O register 5, serial I/O register 6, to serial I/O register 7, until it is finally output from the S_{OUT} pin, each time the transfer clock changes from "H" to "L". Bit 6 of the serial I/O mode register selects whether transfer is from the lowest bit of each serial I/O register, or from the highest bit.

During reception, data is fetched from the S_{IN} pin each time the transfer clock changes from "L" to "H" and, at the same time, the data in each register is shifted one bit in sequence from serial I/O register 7 to serial I/O register 6, serial I/O register 5, serial I/O register 4, serial I/O register 3, serial I/O register 2, serial I/O register 1, to serial I/O register 0.

If the transfer clock is the count value set in the serial I/O mode register 2, when the serial I/O counter reaches "0", the transfer clock stops at "H" and the corresponding interrupt request bit is set.

If an external clock is selected as the clock source, it must

be controlled externally, because the transfer clock does not stop, even when the interrupt request bit is set. Use a clock of no more than 1MHz with a duty cycle of 50% as the external clock.

Serial I/O timing is shown in Fig. 9. If an external clock is used for the transfer, the external clock must be "H" when the serial I/O counter is initialized. If the internal clock is switched to an external clock, make sure that it is switched while no transfer is in progress, and make sure that the serial I/O counter is initialized after the switch.

A connection example for transferring data from one M37260M6-XXXSP to another is shown in Fig. 10. If P_{32} is used as the \overline{CS} pin, set the P_{32} direction register to input ("0") and set bit 4 of the serial I/O mode register 2 to "0". This setting ensures that the transfer clock is fixed at "H" when the P_{32} input signal is "H", and data is not shifted. If the P_{32} input signal goes "L", data will be shifted according to the clock input from the P_{35}/S_{CLK} pin. Note that if bit 4 of the serial I/O mode register 2 is set to "1", the data will be shifted according to the clock input from the P_{35}/S_{CLK} pin, regardless of the P_{32} input signal.

Note 1 : When writing programs, remember that the serial I/O counter will also be set by using bit manipulation instructions such as SEB and CLB to write to the serial I/O register 0.

2 : When writing data to serial I/O registers 0 to 7, make sure that serial I/O register 0 is the last one written to.

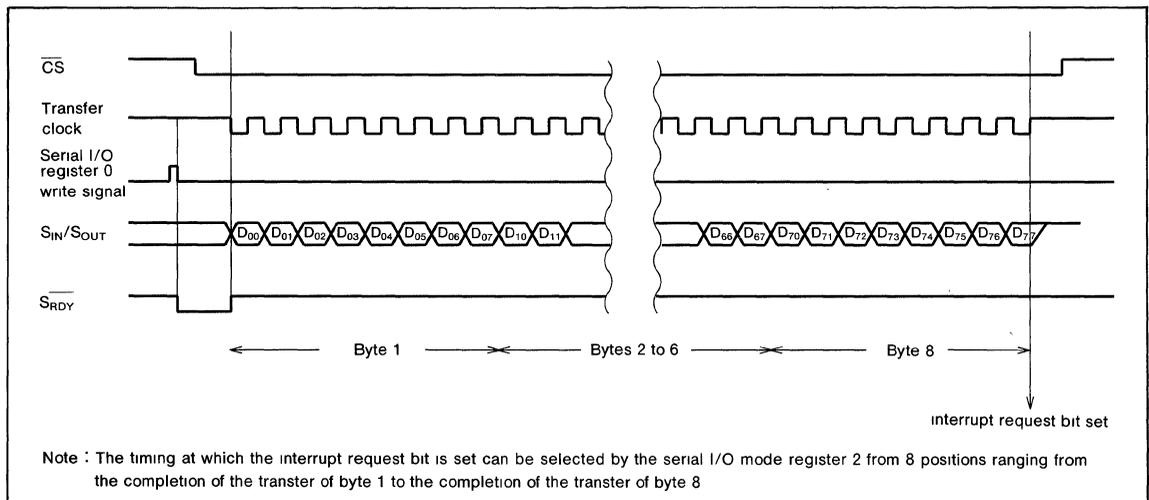


Fig. 9 Serial I/O timing

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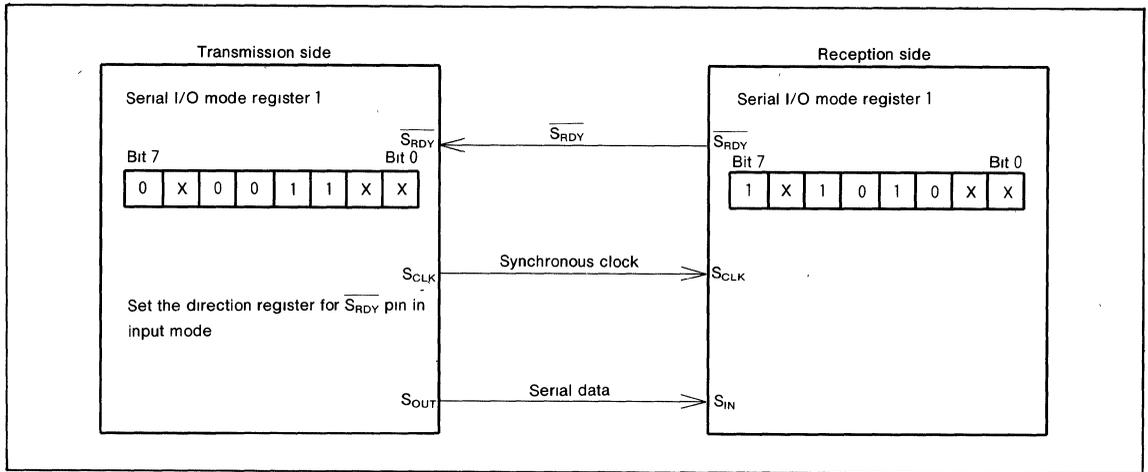


Fig. 10 Example of serial I/O connection

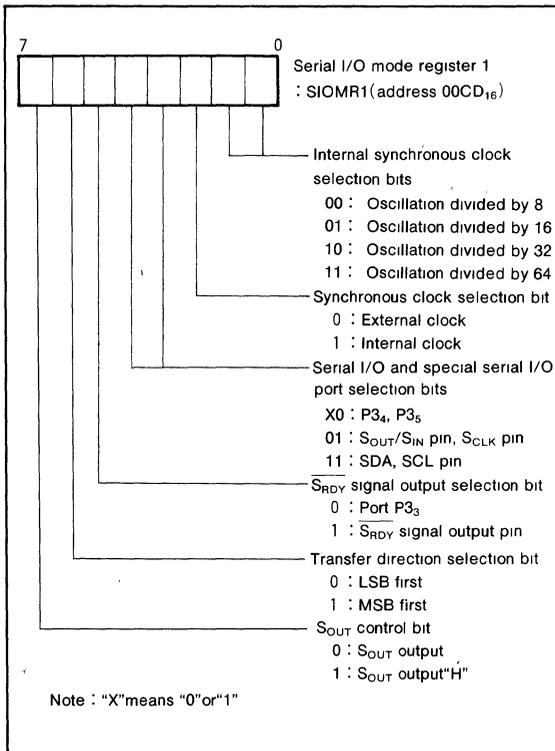


Fig. 11 Structure of serial I/O mode register 1

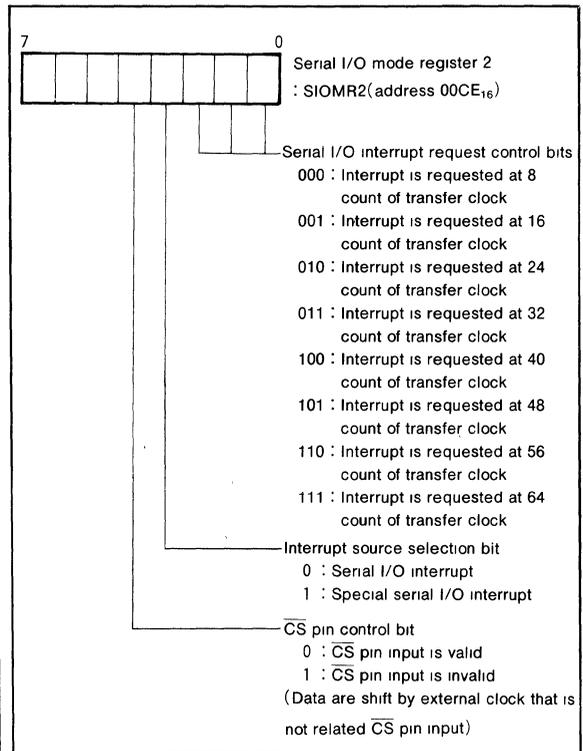


Fig. 12 Structure of serial I/O mode register 2

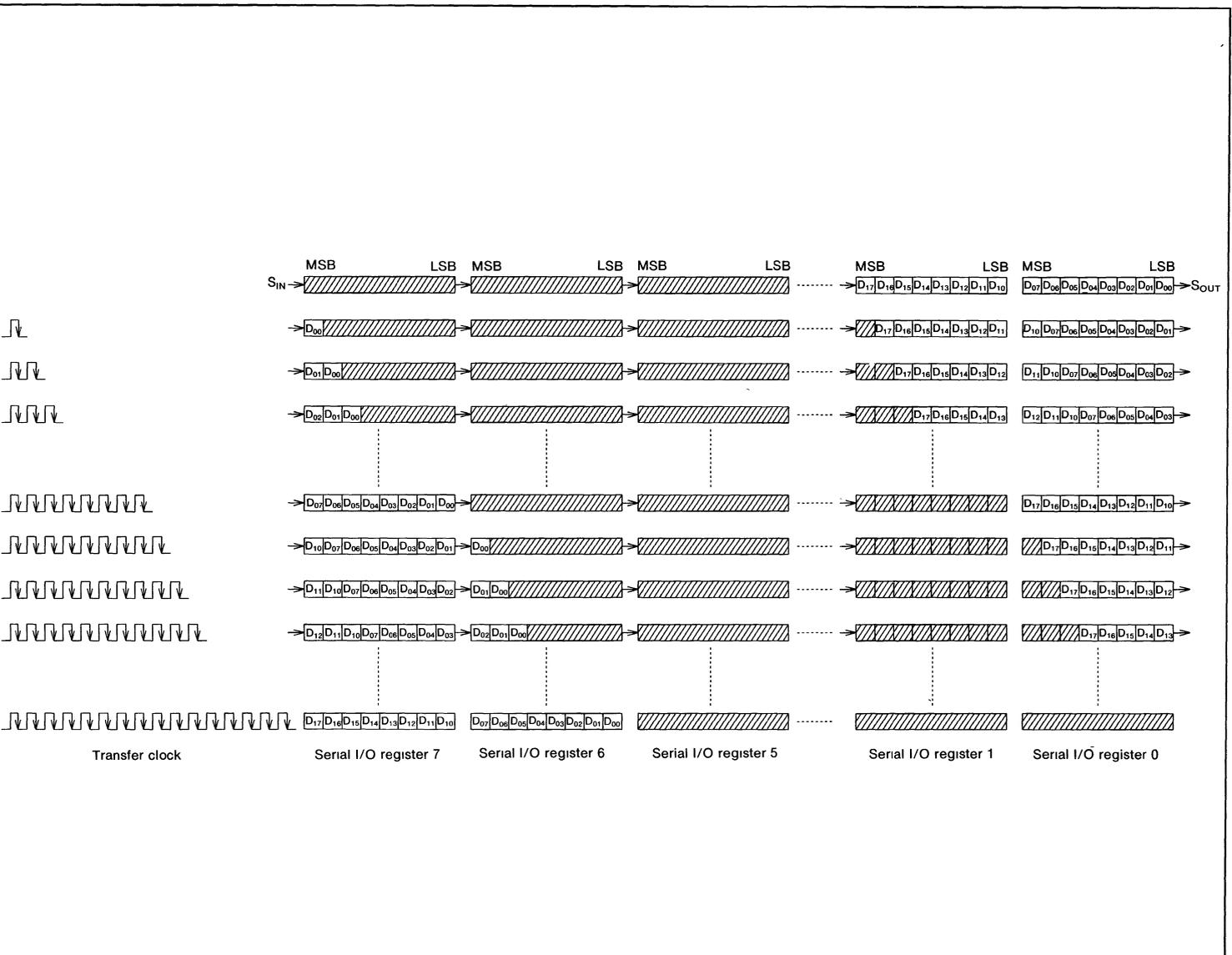


Fig. 13 Serial I/O register state during transmission of 2-byte data

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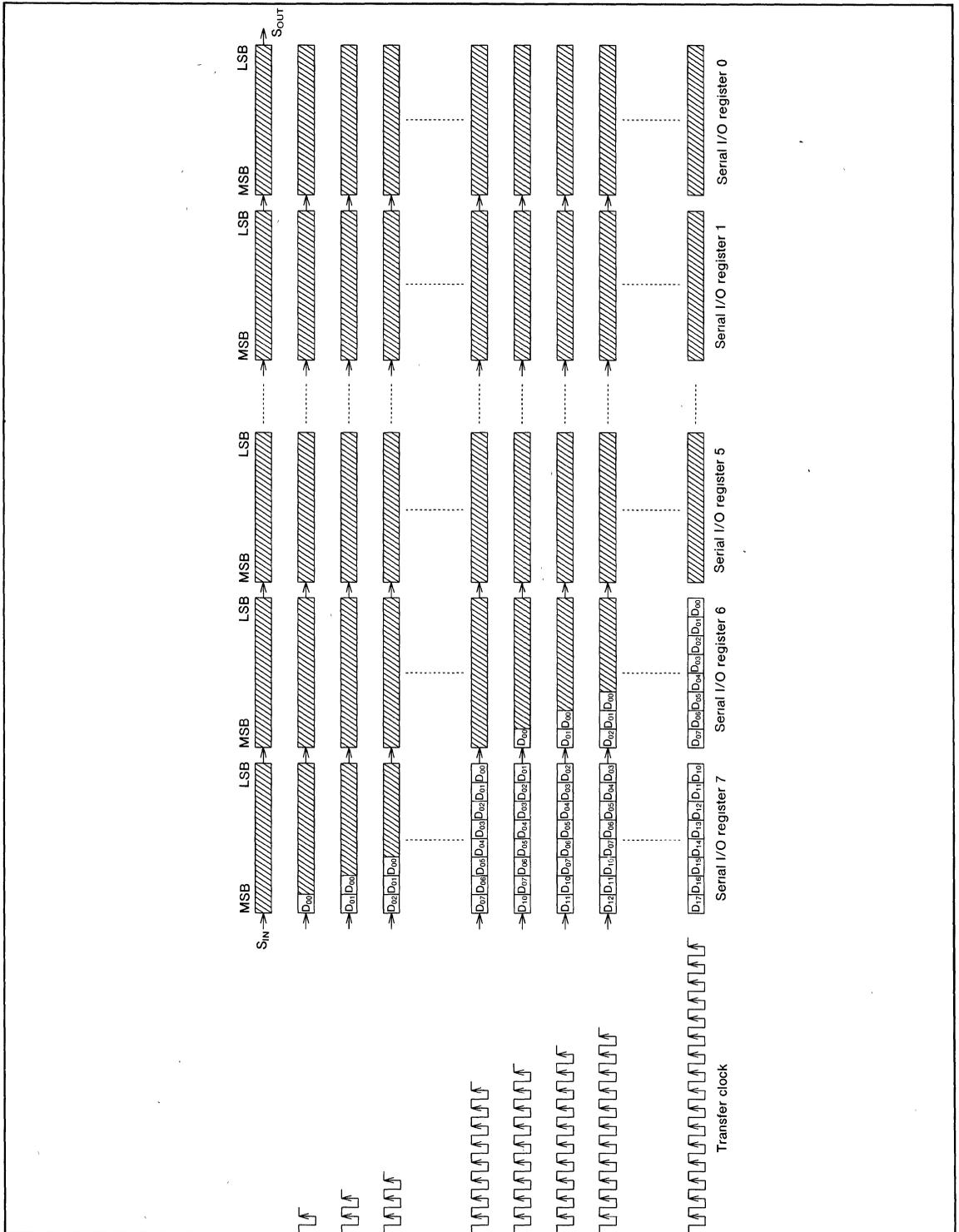


Fig. 14 Serial I/O register state during reception of 2-byte date

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SPECIAL MODE (I²C BUS MODE*)

M37260M6-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I²C (Inter IC) bus format.

I²C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery.

M37260M6-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O explained in the following:

(1) Master transmission

- ① To generate an interrupt at the end of transmission, set bit 3 of serial I/O mode register 2 (address 00CE₁₆) to "1" so as to special serial I/O interrupt is selected.
- ② Then set bit 1 of interrupt control register 2 (address 00FF₁₆) to "1" so as to special serial I/O interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.
- ③ The output signals of master transmission SDA and SCL are output from ports P3₄ and P3₅. Set all bits (bits 4 and 5) corresponding to P3₄ and P3₅ of the port P3 register (address 00C6₁₆) and the port P3 direction register (address 00C7₁₆) to "1".
- ④ Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4 and timer 34 mode register. (For instance, if f(X_{IN})/2 is selected as the clock source of timer 4 and 9 is set in timer 4 when f(X_{IN}) is 4MHz, the master transmission clock frequency is 100kHz.)
- ⑤ Set contents of the special mode register 2 (address 00F8₁₆). (Usually, the value is "03₁₆".)
- ⑥ Set the bits 3 and 4 of serial I/O mode register 1 (address 00CD₁₆) so as the port P3₄ and P3₅ is specified to SDA and SCL. After that set the special mode register 1 (address 00F7₁₆). Figure 18 shows the structure of special mode registers 1 and 2. Initial setting is completed by the above procedure.
- ⑦ Clear bits 0 and 1 of special mode register 2 (to "0") to make both SDA and SCL output to "L". This is for arbitration. Immediately after this, write data to be

transmitted in the special serial I/O register (address 00F6₁₆). The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK reception and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 1 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

- ⑧ To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.
- ⑨ To terminate data transfer, clear bits 0 and 1 of the special mode register 2 to "0".
- ⑩ Set bit 1 clock SCL to "1".
- ⑪ Then set bit 0 data SDA to "1". This procedure transmits the stop signal.

Figure 16 shows master transmission timing explained above. (the numbers in this figure are correspond to above explained numbers.)

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission (the process until ⑦ in Figure 16.)

In the interrupt routine, set master reception ACK provided (22₁₆) in the special mode register 1 (address 00F7₁₆), and write "FF₁₆" in the special serial I/O register (address 00F6₁₆). This sets data line SDA to "H" and to perform 8-clock master reception. Then, a clock of "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission (the process from ⑨ to ⑪ in Figure 16.)

Figure 17 shows master reception timing.

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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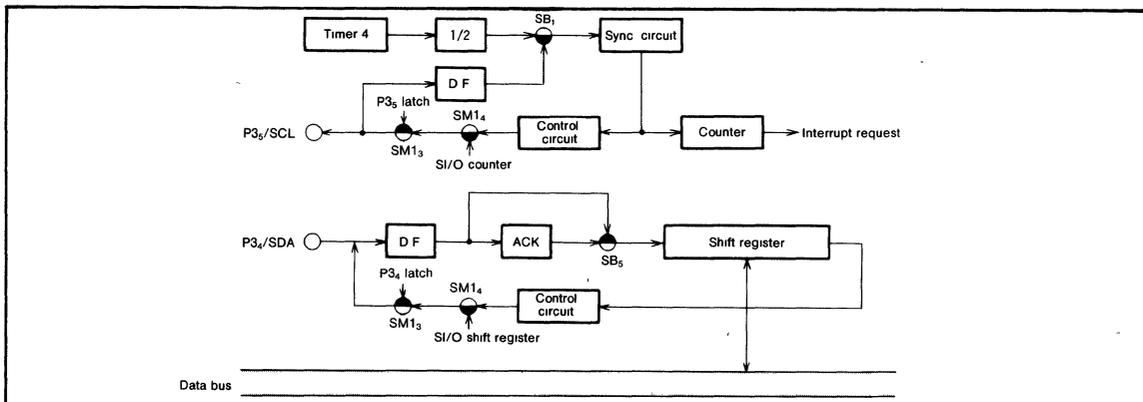


Fig. 15 Block diagram of special serial I/O

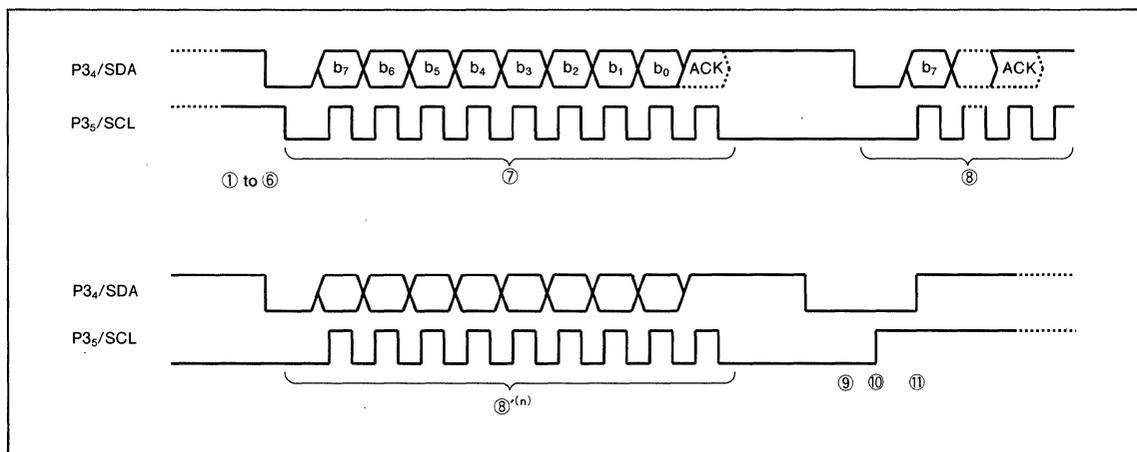


Fig. 16 Master transmission timing

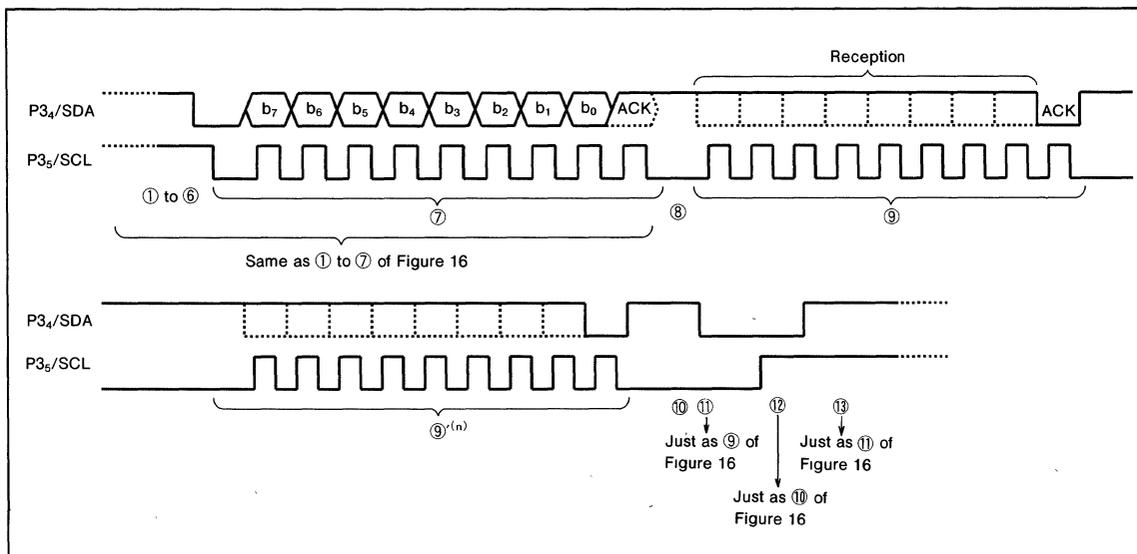


Fig. 17 Master reception timing

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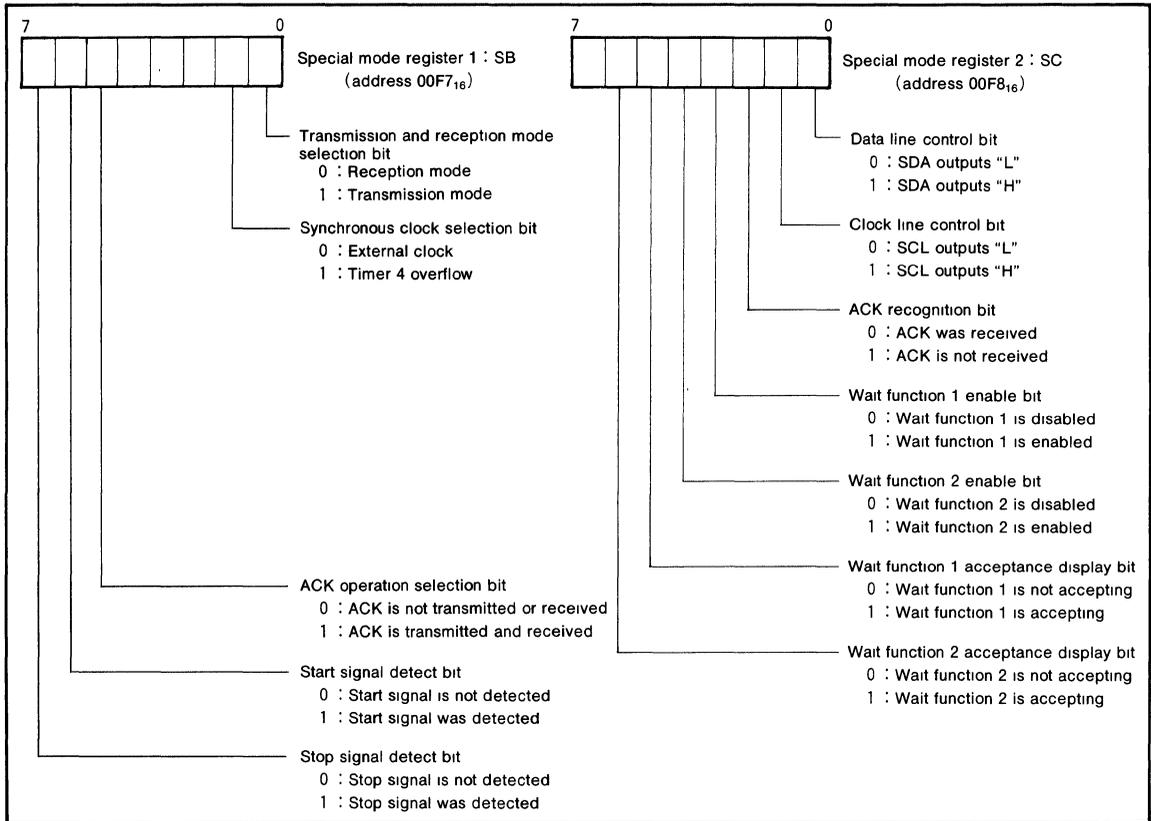


Fig. 18 Structure of special mode registers 1 and 2

(3) Wait functions

Wait function 1 holds the SCL line at "L" after the 8th clock falls in special mode. Wait function 2 holds the SCL line at "L" after the 9th clock falls in the same way.

When one of the wait functions operates, the internal counter that counts the clock must be reset after bit 3 or 4 of the special mode register 2 is set to "1", to enable the corresponding wait function 1 or 2 to operate. Reset the internal counter by writing data to the special serial I/O register (address 00F6₁₆), or by setting the START signal detection bit to "1". Reset the internal counter for each byte before data transfer.

The wait functions can be released by setting the corresponding bit 5 or 6 of the special mode register 2 to "1".

Note 1 : Clear the START signal detection bit (bit 6) and the STOP signal detection bit (bit 7) of the special mode register 1 by writing "1" to bit 6 or bit 7.

2 : If the special serial I/O function is operating, change the value of bit 4 of the sync generator control register (address 00E9₁₆) to suit the frequency of the system clock (X_{IN}).

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CRT DISPLAY FUNCTIONS

Table 2 outlines the CRT display functions of the M37260M6-XXXSP. The M37260M6-XXXSP incorporates a 40 columns X 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register. Up to 510 kinds of characters can be displayed, and colors can be specified for each character. A combination of up to 16 colors can be obtained by using each output signal (R, G, B, and I).

Table 2. Outline of CRT display functions

Item		Efficiency
Display characters		40 characters X 3 lines (maximum 25 lines)
Character configuration		12 X 20 or 16 X 20 dots
Kinds of character		510 kinds
Character size		30 kinds
Color	Kinds of color	16 (maximum)
	Coloring unit	Character
Extension display		Possible (multiple lines)

Characters are displayed in a 12 X 20 or 16 X 20 dots configuration to obtain smooth character patterns. (See Figure 19)

The following shows the procedure how to display characters on the CRT screen.

- ① Write the display character code to the display RAM.
- ② Write the color code to the display RAM.
- ③ Specify the vertical position and character size by using the vertical position register and the character size register.
- ④ Specify the horizontal position by using the horizontal position register.
- ⑤ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 20 shows a block diagram of the CRT display control circuit. Figure 21 shows the structure of the CRT display control register.

And the mixing circuit is built-in that can be output the signal mixed external color signals with internal color signals, so that the CRT display can be controlled by the 2-chip constructed system.

The sync generator that generates the synchronous signal can be output each synchronous signal as NTSC or PAL with/without interlacing.

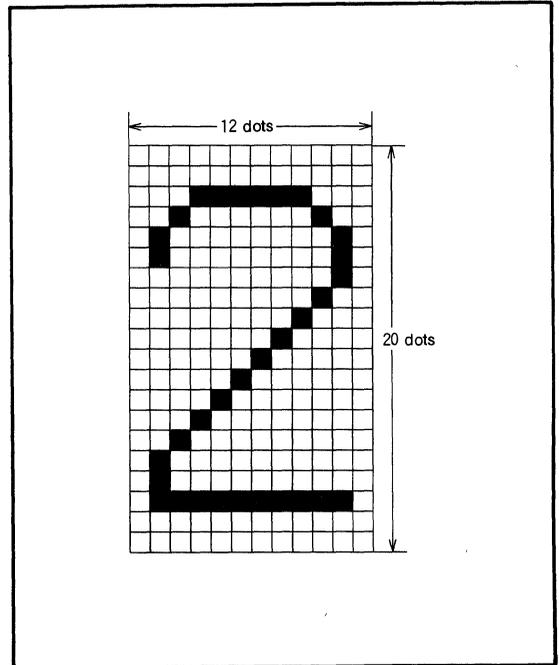


Fig. 19 CRT display character configuration

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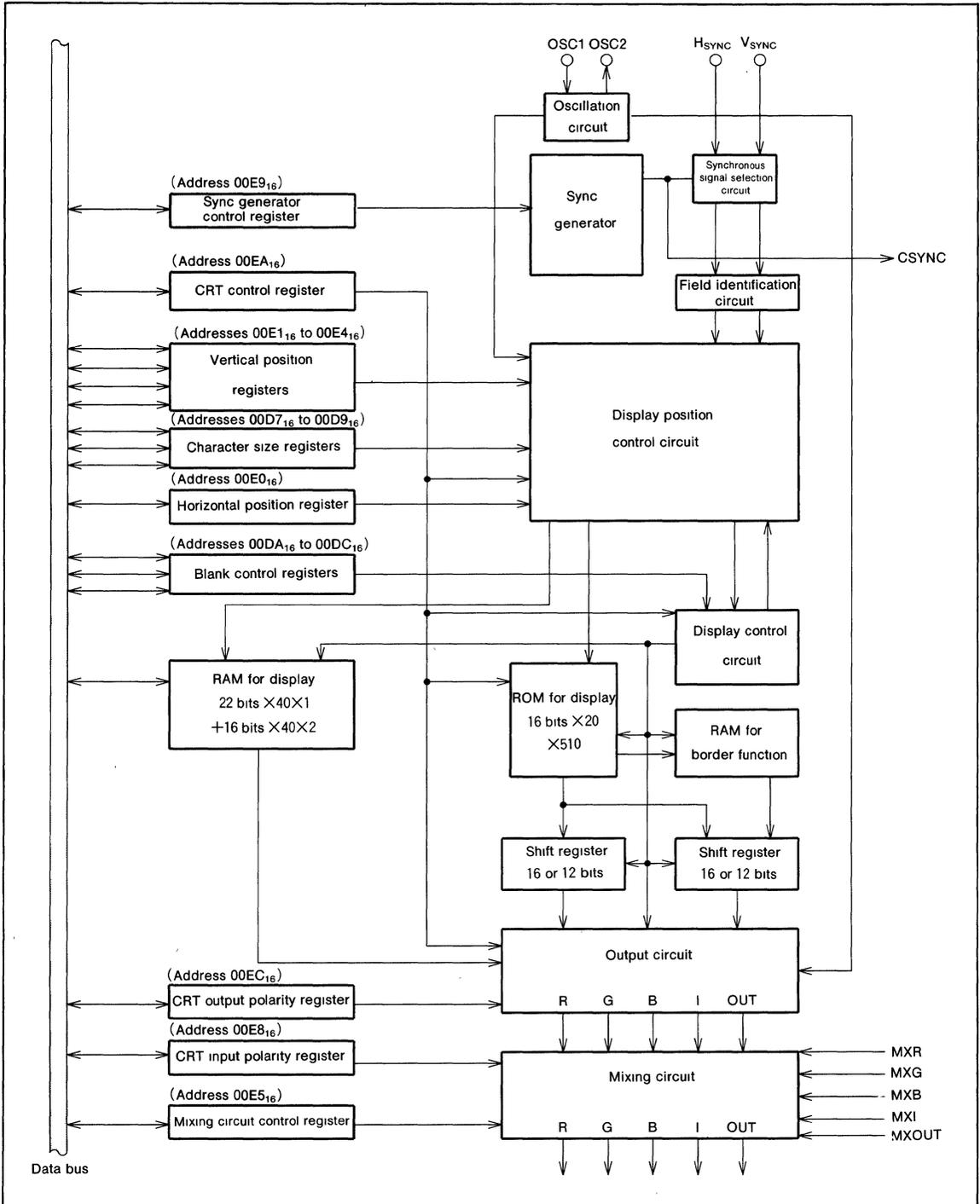


Fig. 20 CRT display control circuit block diagram

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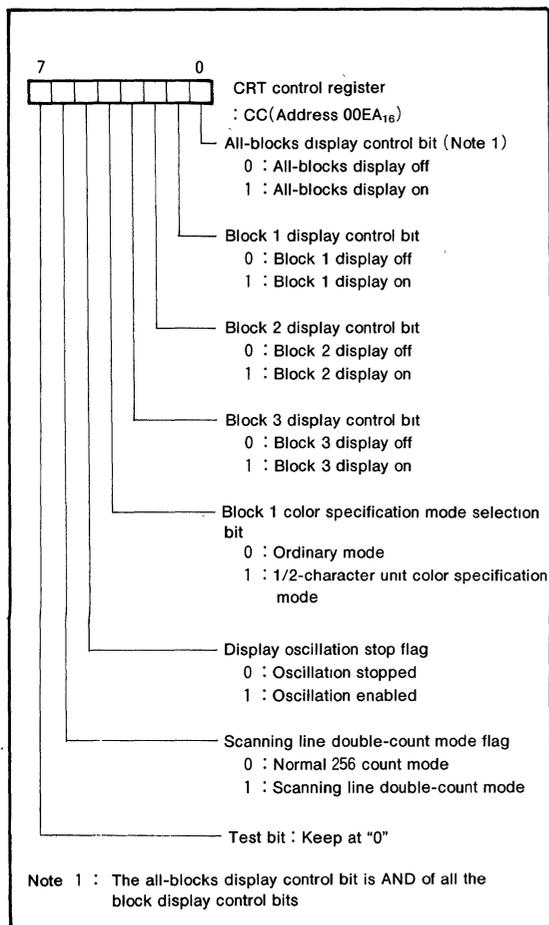


Fig. 21 Structure of CRT control register

(1) Display Position

Character display position is specified in units called blocks. There are three blocks—block 1 to block 3—and each block can hold up to 40 characters (for details, see the previous section (3) Display Memory.)

The display position of each block can be set horizontally and vertically by software.

Horizontal positions can be selected for all blocks in common from 256-steps in 4T_c units (Where T_c : display oscillation period).

Vertical display positions can be selected for each block from 1024-steps in single scanning line units.

If a display start position is superimposed on another block ((b) in Figure 23), the block with the smallest number (1 to 3) is displayed.

If the display position of a block comes while another block is displayed ((c) in Figure 23), the second block is displayed.

Vertical positions for each block can be set in 1024 steps (where each step is one scanning line) as values 00₁₆ to FF₁₆ in vertical position registers 1 to 3 (addresses 00E1₁₆ to 00E3₁₆) and values 00₁₆ to 3F₁₆ in bits 0 to 5 of vertical position register 4. The structures of the vertical position registers are shown in Figure 22.

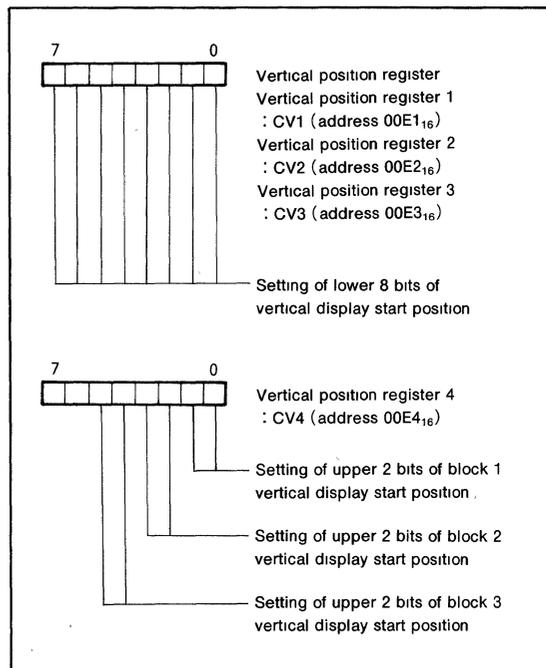
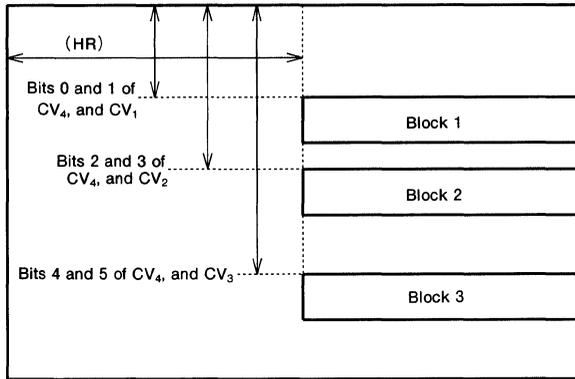


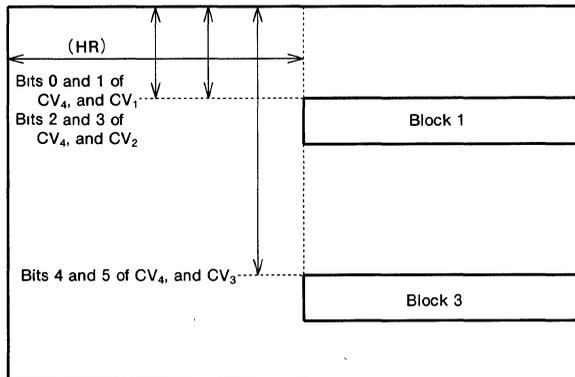
Fig. 22 Structure of vertical position registers

The horizontal position is common to all blocks, and can be set in 256 steps (where one step is 4T_c, T_c being the display oscillation period) as values 00₁₆ to FF₁₆ in the horizontal position register (address 00E0₁₆). The structure of the horizontal position register is shown in Figure 24.

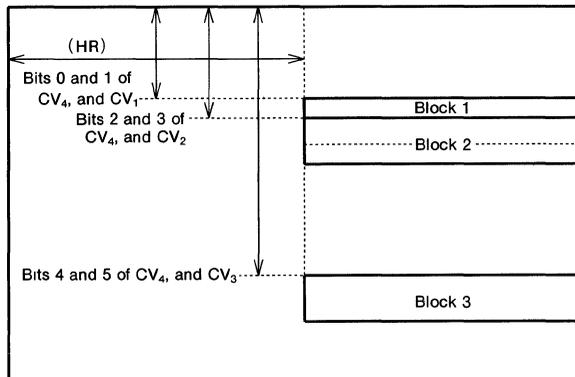
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(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed

Fig. 23 Display position and value of vertical position registers CV_x (x : 1 to 4)

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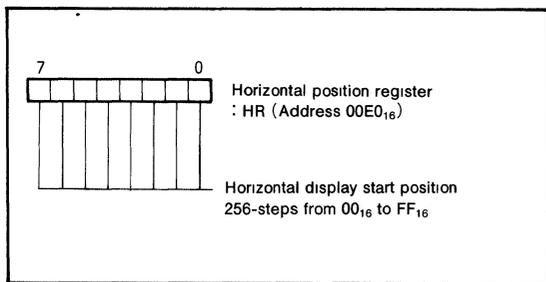


Fig. 24 Structure of horizontal position register

(2) Character Size

The size of characters to be displayed can be selected from 30 types, by combining 5 vertical types and 6 horizontal types in block units. Set the size with the character size registers (addresses 00D7₁₆ to 00D9₁₆). Either of two character font configurations, 12 dots wide × 20 dots high or 16 dots wide × 20 dots high, can be selected for each block. The configuration of the character ROM font is shown in Figure 26.

The display start position in the horizontal direction is the same, regardless of changes in character size, but it does differ if the character font configuration is changed. The display start position in the horizontal direction for 16 dots wide × 20 dots high characters is 4T_C to the right of that for 12 dots wide × 20 dots high characters.

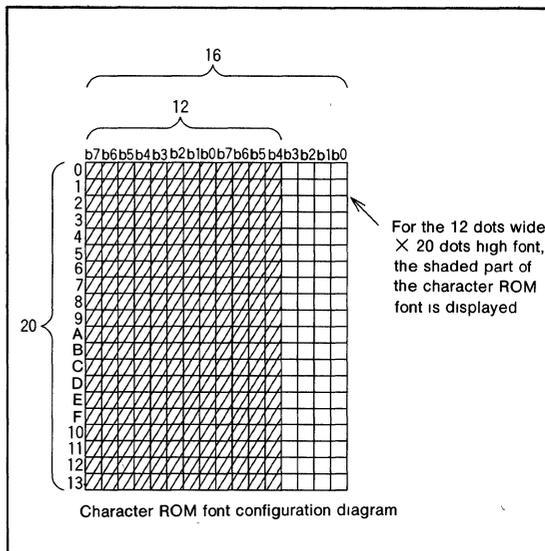


Fig. 26 Character ROM font for 12 dots wide × 20 dots high font

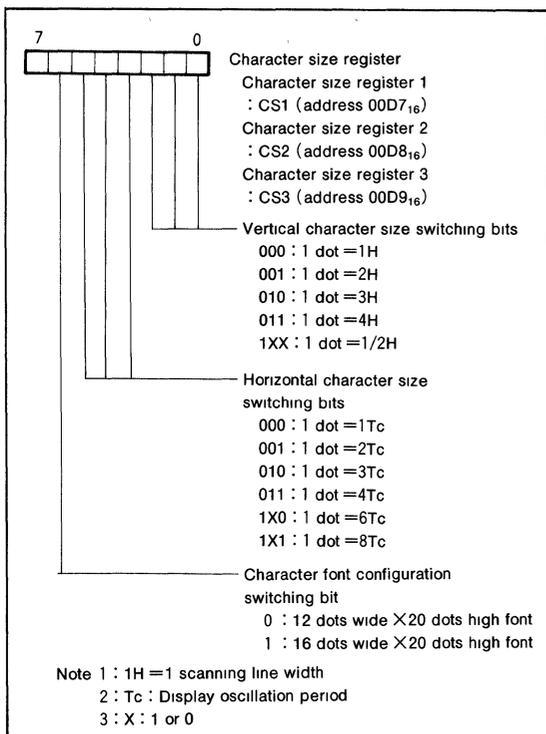


Fig. 25 Structure of character size registers

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The 1 dot=1/2 scanning line display function differentiates between odd-numbered and even-numbered fields from differences in the waveform in the synchronization signals used by the interlace method, and displays one character font for both fields. Bit 6 of the sync generator control register (address 00E9₁₆) controls the active edge of the field identification flag, and the character font divided for each field can be selected.

The field identification flag can also be read out from bit 6 of the display block counter (address 00EB₁₆).

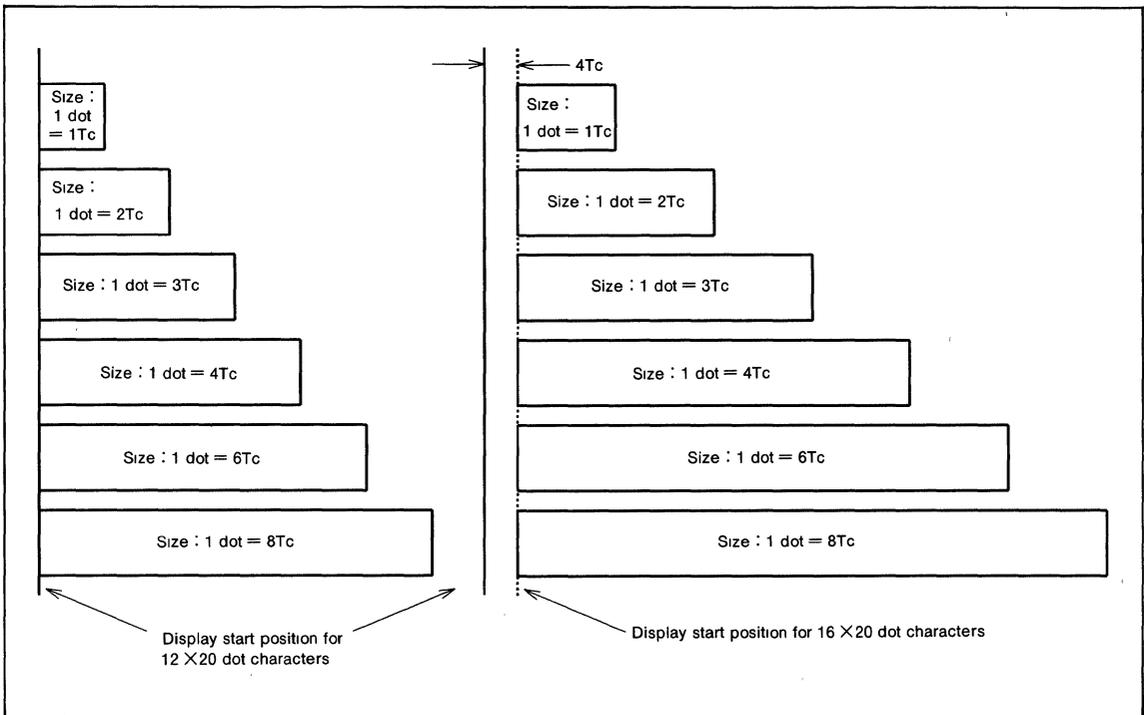


Fig. 27 Display start positions (horizontal) for each character size

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The description below assumes that field identification is based on the case where the active edges of both the horizontal and vertical synchronization signals are negative.

Each field is identified as either odd or even by the hardware detecting the positions of the falling edges of the horizontal and vertical synchronization signals, and comparing them. Therefore, to ensure correct field identification, make sure that the two synchronization signals are input in accordance with the identification criteria given below.

Since the field identification is based on the system clock (X_{IN}), make sure that the value of bit 4 of the sync generator control register (address 00E9₁₆) is changed in accordance with the frequency of the system clock.

Even-numbered field : The vertical synchronization signal falls within $2\mu s$ before or after the fall of the horizontal synchronization signal.

Odd-numbered field : The vertical synchronization signal falls within $2\mu s$ before or after a point $1/2$ a cycle after the fall of the horizontal synchronization signal.

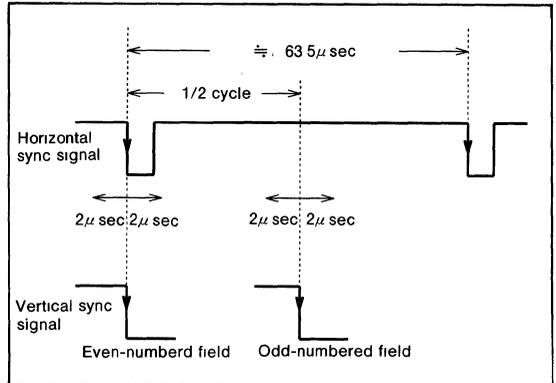


Fig. 28 Identification criteria for field identification

Field	Sync signal (Example : negative edge input)	Field identification flag active edge bit (bit 6 of the sync generator control register)	Field identification flag bit (bit 6 of the display block counter)	Display font
Odd-numbered field	Horizontal sync signal	0	1	<input type="checkbox"/> part
	Vertical sync signal	1	0	<input type="checkbox"/> part
Even-numbered field	Horizontal sync signal	0	0	<input type="checkbox"/> part
	Vertical sync signal	1	1	<input type="checkbox"/> part

	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0																
1																
2																
3																
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F																
10																
11																
12																
13																

Character ROM font configuration

Example : When the field identification flag active edge bit is 0, odd-numbered fields display the font and even-numbered fields display the font. Bit 6 of the display block counter can be read as the field identification flag : it is "1" for an odd-numbered field, "0" for an even-numbered field

Note : The field identification flag changes at the fall of the vertical sync signal (negative edge input)

Fig. 29 Relationships between field identification flag and display font

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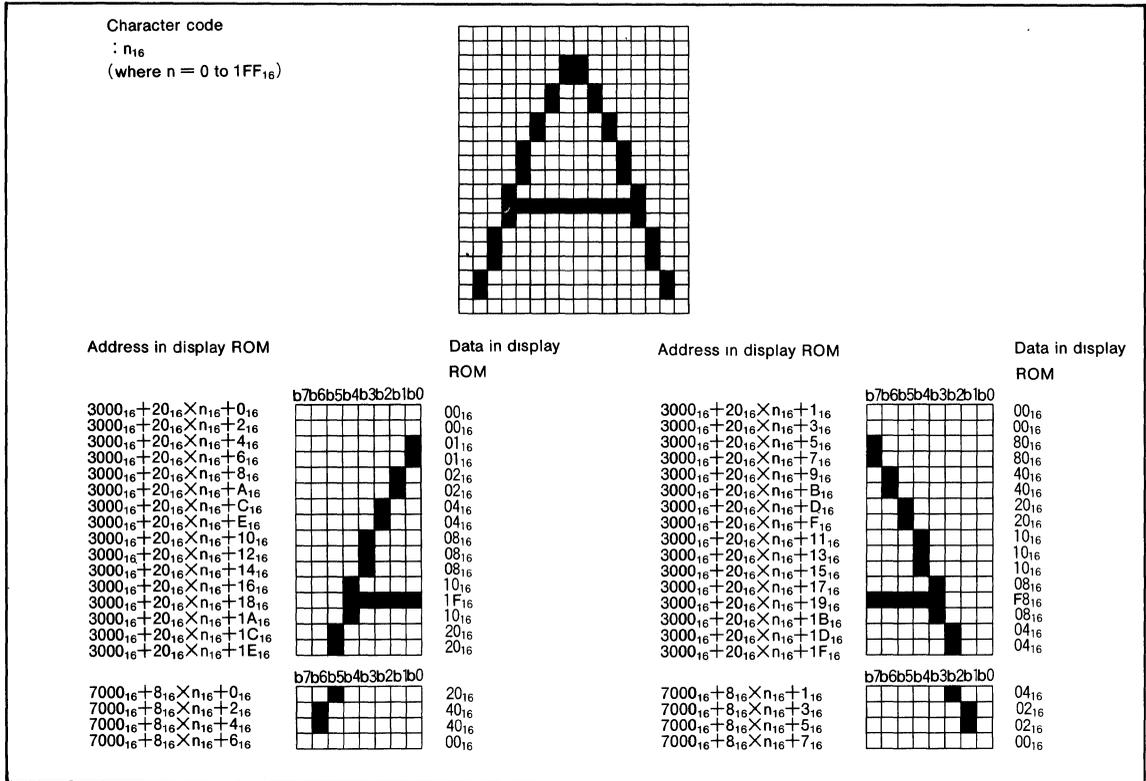


Fig. 30 Storage format of display characters

(3) Display Memory

There are two types of display memory: CRT display ROM (addresses 3000_{16} to $7FFF_{16}$) which contains previously stored (masked) character dot data, and display RAM (addresses 2000_{16} to $27FF_{16}$) which specifies characters and colors to be displayed. These memory types are described below.

① CRT display ROM (addresses 3000_{16} to $7FFF_{16}$)

The CRT display ROM contains dot pattern data for display characters. To display these stored characters in operation, specify character codes (code determined based on addresses in CRT display ROM) that are specific to those characters, by writing them to the CRT display RAM.

Since the CRT display ROM has contains 20K bytes and the data for one character takes up 40 bytes, 512 characters can be stored. However, a two-character space is re-

quired for test purposes, so in practice 510 characters can be stored for display.

Within the CRT display ROM area, data for part of each character that is [upper 16 dots high] × [left-hand 8 dots wide] is stored at addresses $300X_{16}$ to $3FFX_{16}$ (where $X = 0, 2, 4, 6, 8, A, C, E$), data for part of each character that is [upper 16 dots high] × [right-hand 8 dots wide] is stored at $300Y_{16}$ to $3FFY_{16}$ (where $Y = 1, 3, 5, 7, 9, B, D, F$), data for part of each character that is [lower 4 dots high] × [left-hand 8 dots wide] is stored at addresses $700M_{16}$ to $7FFM_{16}$ (where $M = 0, 2, 4, 6, 8, A, C, E$), and data for part of each character that is [lower 4 dots high] × [right-hand 8 dots wide] is stored at $700N_{16}$ to $7FFN_{16}$ (where $N = 1, 3, 5, 7, 9, B, D, F$), as shown in Figure 30.

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Table 3. Character Code Chart (Partially abbreviated)

Character code	Character data storage address			
	Left-hand 8 dots		Right-hand 8 dots	
	Upper 16 dots	Lower 4 dots	Upper 16 dots	Lower 4 dots
000 ₁₆	3000 ₁₆	7000 ₁₆	3001 ₁₆	7001 ₁₆
	3002 ₁₆	7002 ₁₆	3003 ₁₆	7003 ₁₆
	3004 ₁₆	7004 ₁₆	3005 ₁₆	7005 ₁₆
	3006 ₁₆	7006 ₁₆	3007 ₁₆	7007 ₁₆
	3008 ₁₆		3009 ₁₆	
	300A ₁₆		300B ₁₆	
	300C ₁₆		300D ₁₆	
	300E ₁₆		300F ₁₆	
	3010 ₁₆		3011 ₁₆	
	3012 ₁₆		3013 ₁₆	
	3014 ₁₆		3015 ₁₆	
	3016 ₁₆		3017 ₁₆	
	3018 ₁₆		3019 ₁₆	
	301A ₁₆		301B ₁₆	
	301C ₁₆		301D ₁₆	
	301E ₁₆		301F ₁₆	
001 ₁₆	3020 ₁₆	7008 ₁₆	3021 ₁₆	7009 ₁₆
	3022 ₁₆	700A ₁₆	3023 ₁₆	700B ₁₆
	3024 ₁₆	700C ₁₆	3025 ₁₆	700D ₁₆
	3026 ₁₆	700E ₁₆	3027 ₁₆	700F ₁₆
	3028 ₁₆		3029 ₁₆	
	302A ₁₆		302B ₁₆	
	302C ₁₆		302D ₁₆	
	302E ₁₆		302F ₁₆	
	3030 ₁₆		3031 ₁₆	
	3032 ₁₆		3033 ₁₆	
	3034 ₁₆		3035 ₁₆	
	3036 ₁₆		3037 ₁₆	
	3038 ₁₆		3039 ₁₆	
	303A ₁₆		303B ₁₆	
	303C ₁₆		303D ₁₆	
	303E ₁₆		303F ₁₆	
⋮	⋮	⋮	⋮	⋮
1FF ₁₆	6FE0 ₁₆	7FF8 ₁₆	6FE1 ₁₆	7FF9 ₁₆
	6FE2 ₁₆	7FFA ₁₆	6FE3 ₁₆	7FFB ₁₆
	6FE4 ₁₆	7FFC ₁₆	6FE5 ₁₆	7FFD ₁₆
	6FE6 ₁₆	7FFE ₁₆	6FE7 ₁₆	7FFF ₁₆
	6FE8 ₁₆		6FE9 ₁₆	
	6FEA ₁₆		6FEB ₁₆	
	6FEC ₁₆		6FED ₁₆	
	6FEE ₁₆		6FEF ₁₆	
	6FF0 ₁₆		6FF1 ₁₆	
	6FF2 ₁₆		6FF3 ₁₆	
	6FF4 ₁₆		6FF5 ₁₆	
	6FF6 ₁₆		6FF7 ₁₆	
	6FF8 ₁₆		6FF9 ₁₆	
	6FFA ₁₆		6FFB ₁₆	
	6FFC ₁₆		6FFD ₁₆	
	6FFE ₁₆		6FFF ₁₆	

Each character code used when specifying display characters, is defined as n_{16} (where $n=0$ to $1FF$), and is determined based on the address in CRT display ROM that contains the data for that character (see the storage format of display character shown in Fig. 30). The character codes are listed in Table 3.

② CRT display RAM (addresses 2000₁₆ to 27FF₁₆)

The CRT display RAM is allocated at addresses 2000₁₆ to 27FF₁₆, and is divided into a display character code specification part and a display color code specification part for each block. The contents of this area are shown in Table 4. For example, to display one character at the first character position (the left edge) of block 1, write the character code to bit 6 of address 20C0₁₆ and to address 2000₁₆, and write the color code to the lowermost 6 bits (bits 0 to 5) of address 20C0₁₆. For details of the color codes, see section (4) Color codes. The structure of the CRT display RAM is shown in Fig. 31.

When generating a mask for the M37260M6-XXXSP, note that the character patterns of Table 6 and Table 7 must be written to the specified addresses as a test character pattern.

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Table 4. CRT display RAM description

Block	Display position (from left side)	Character code specification		Color code specification	1/2 character unit color code specification
		High-order 1 bit	Low-order 8 bit		
Block 1	1st character	20C0 ₁₆	2000 ₁₆	20C0 ₁₆	2180 ₁₆
	2nd character	20C1 ₁₆	2001 ₁₆	20C1 ₁₆	2181 ₁₆
	3rd character	20C2 ₁₆	2002 ₁₆	20C2 ₁₆	2182 ₁₆
	⋮	⋮	⋮	⋮	⋮
	38th character	20E5 ₁₆	2025 ₁₆	20E5 ₁₆	21A5 ₁₆
	39th character	20E6 ₁₆	2026 ₁₆	20E6 ₁₆	21A6 ₁₆
	40th character	20E7 ₁₆	2027 ₁₆	20E7 ₁₆	21A7 ₁₆
Not used		20E8 ₁₆ to 20FF ₁₆	2028 ₁₆ to 203F ₁₆	20E8 ₁₆ to 20FF ₁₆	
Block 2	1st character	2100 ₁₆	2040 ₁₆	2100 ₁₆	
	2nd character	2101 ₁₆	2041 ₁₆	2101 ₁₆	
	3rd character	2102 ₁₆	2042 ₁₆	2102 ₁₆	
	⋮	⋮	⋮	⋮	
	38th character	2125 ₁₆	2065 ₁₆	2125 ₁₆	
	39th character	2126 ₁₆	2066 ₁₆	2126 ₁₆	
	40th character	2127 ₁₆	2067 ₁₆	2127 ₁₆	
Not used		2128 ₁₆ to 213F ₁₆	2068 ₁₆ to 207F ₁₆	2128 ₁₆ to 213F ₁₆	
Block 3	1st character	2140 ₁₆	2080 ₁₆	2140 ₁₆	
	2nd character	2141 ₁₆	2081 ₁₆	2141 ₁₆	
	3rd character	2142 ₁₆	2082 ₁₆	2142 ₁₆	
	⋮	⋮	⋮	⋮	
	38th character	2165 ₁₆	20A5 ₁₆	2165 ₁₆	
	39th character	2166 ₁₆	20A6 ₁₆	2166 ₁₆	
	40th character	2167 ₁₆	20A7 ₁₆	2167 ₁₆	
Not used		2168 ₁₆ to 217F ₁₆	20A8 ₁₆ to 20BF ₁₆	2168 ₁₆ to 217F ₁₆	

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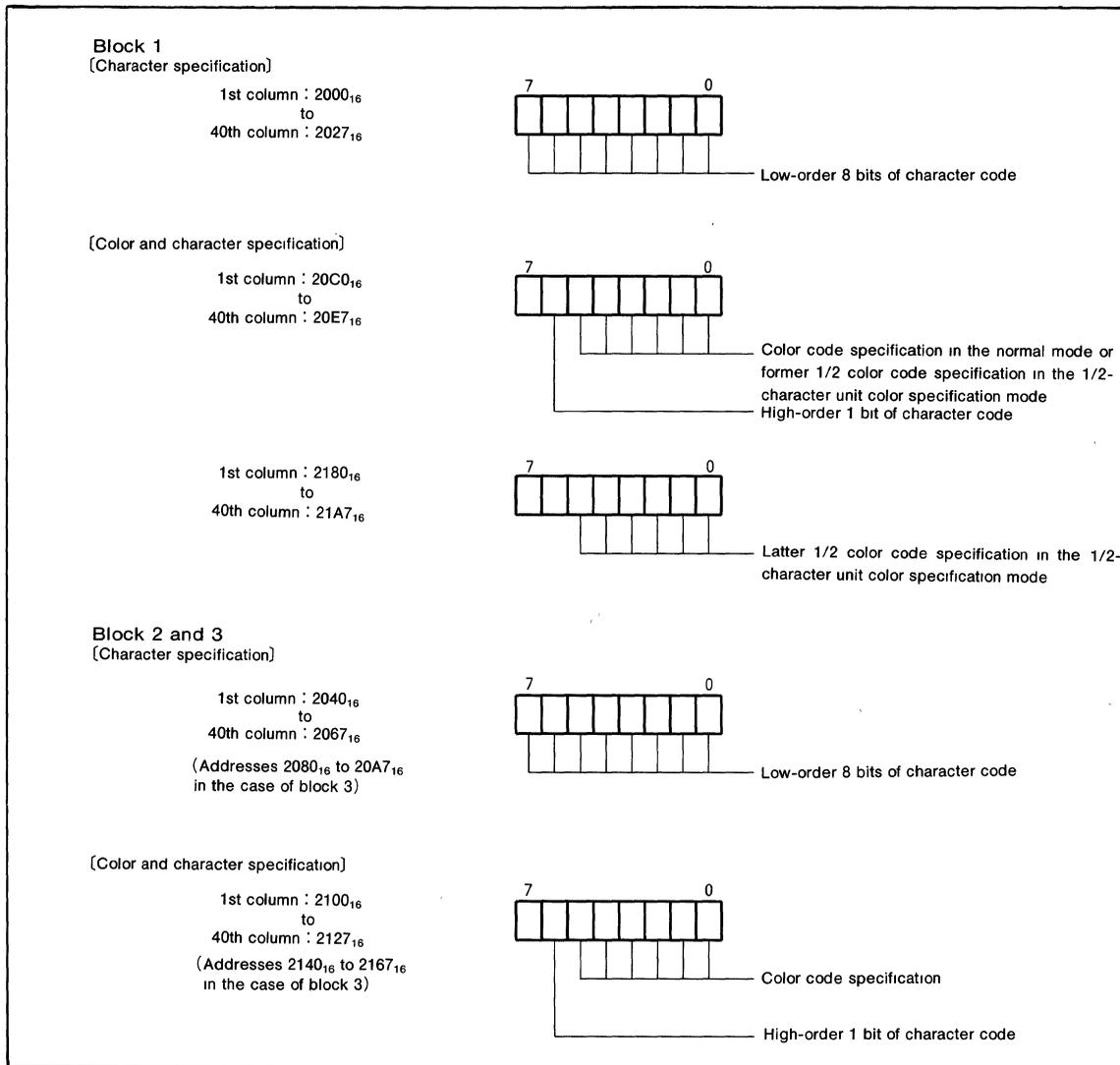


Fig. 31 Structure of CRT display RAM

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③ Block overwriting function of display memory

Character codes or color codes for 40 characters can be written for each block in a batch by overwriting data at a specific address.

The addresses for block overwriting, the addresses in display memory overwritten by these addresses, and the contents of these addresses are listed in Table 5.

Table 5. Block overwriting of display memory

Address for block overwriting	Addresses in overwritten display memory	Memory contents
2200 ₁₆	2000 ₁₆ to 2027 ₁₆	Block 1 character code
2201 ₁₆	2040 ₁₆ to 2067 ₁₆	Block 2 character code
2202 ₁₆	2080 ₁₆ to 20A7 ₁₆	Block 3 character code
2203 ₁₆	20C0 ₁₆ to 20E7 ₁₆	Block 1 color code
2204 ₁₆	2100 ₁₆ to 2127 ₁₆	Block 2 color code
2205 ₁₆	2140 ₁₆ to 2167 ₁₆	Block 3 color code
2206 ₁₆	2180 ₁₆ to 21A7 ₁₆	Block 1 color code 2

Note : After a write instruction is executed for a block overwriting address, wait at least 60 machine cycles before issuing a read or write instruction from the CPU for a block overwriting address or for display memory.

④ Notes on display RAM data access

If the display RAM is accessed (data read or write, block write) from the CPU during OSD display, make sure that the display RAM for each block is accessed after it has been confirmed that the block has been displayed, by an event such as a CRT interrupt.

RAM data can be destroyed if the display RAM for a block that is currently being displayed is accessed.

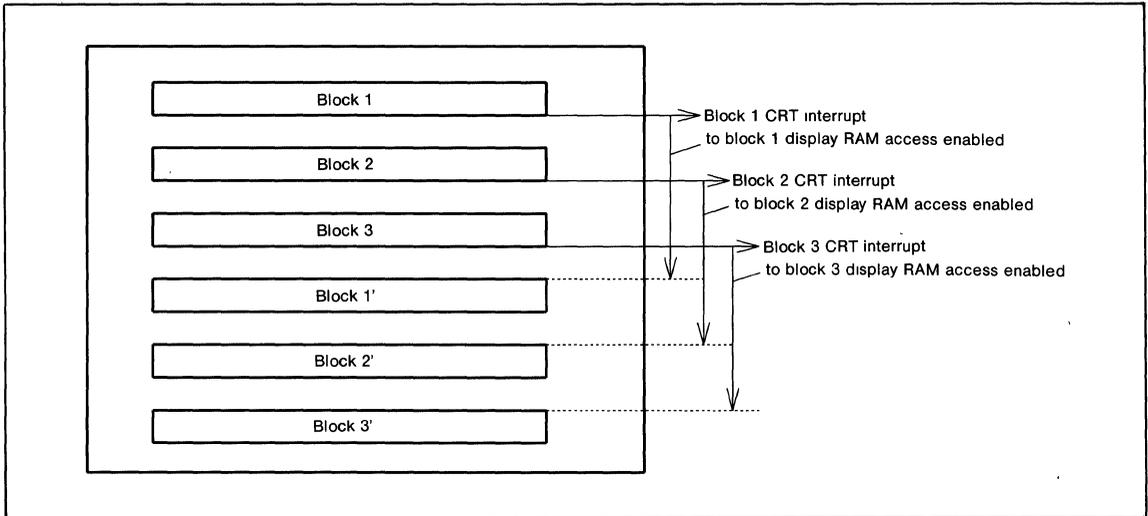


Fig. 32 Display RAM data access

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Table 6. Test character pattern 1 settings

Address	Data	Address	Data
6FE0 ₁₆	00 ₁₆	6FF0 ₁₆	00 ₁₆
6FE1 ₁₆	00 ₁₆	6FF1 ₁₆	00 ₁₆
6FE2 ₁₆	00 ₁₆	6FF2 ₁₆	00 ₁₆
6FE3 ₁₆	00 ₁₆	6FF3 ₁₆	00 ₁₆
6FE4 ₁₆	00 ₁₆	6FF4 ₁₆	00 ₁₆
6FE5 ₁₆	00 ₁₆	6FF5 ₁₆	00 ₁₆
6FE6 ₁₆	00 ₁₆	6FF6 ₁₆	00 ₁₆
6FE7 ₁₆	00 ₁₆	6FF7 ₁₆	00 ₁₆
6FE8 ₁₆	00 ₁₆	6FF8 ₁₆	00 ₁₆
6FE9 ₁₆	00 ₁₆	6FF9 ₁₆	00 ₁₆
6FEA ₁₆	00 ₁₆	6FFA ₁₆	00 ₁₆
6FEB ₁₆	00 ₁₆	6FFB ₁₆	00 ₁₆
6FEC ₁₆	00 ₁₆	6FFC ₁₆	00 ₁₆
6FED ₁₆	00 ₁₆	6FFD ₁₆	00 ₁₆
6FEE ₁₆	00 ₁₆	6FFE ₁₆	00 ₁₆
6FEF ₁₆	00 ₁₆	6FFF ₁₆	00 ₁₆
7FF8 ₁₆	00 ₁₆	7FFC ₁₆	00 ₁₆
7FF9 ₁₆	00 ₁₆	7FFD ₁₆	00 ₁₆
7FFA ₁₆	00 ₁₆	7FFE ₁₆	00 ₁₆
7FFB ₁₆	00 ₁₆	7FFF ₁₆	00 ₁₆

Table 7. Test character pattern 2 settings

Address	Data	Address	Data
6FC0 ₁₆	88 ₁₆	6FD0 ₁₆	22 ₁₆
6FC1 ₁₆	11 ₁₆	6FD1 ₁₆	22 ₁₆
6FC2 ₁₆	00 ₁₆	6FD2 ₁₆	00 ₁₆
6FC3 ₁₆	00 ₁₆	6FD3 ₁₆	00 ₁₆
6FC4 ₁₆	00 ₁₆	6FD4 ₁₆	00 ₁₆
6FC5 ₁₆	00 ₁₆	6FD5 ₁₆	00 ₁₆
6FC6 ₁₆	00 ₁₆	6FD6 ₁₆	00 ₁₆
6FC7 ₁₆	00 ₁₆	6FD7 ₁₆	00 ₁₆
6FC8 ₁₆	44 ₁₆	6FD8 ₁₆	11 ₁₆
6FC9 ₁₆	44 ₁₆	6FD9 ₁₆	11 ₁₆
6FCA ₁₆	00 ₁₆	6FDA ₁₆	00 ₁₆
6FCB ₁₆	00 ₁₆	6FDB ₁₆	00 ₁₆
6FCC ₁₆	00 ₁₆	6FDC ₁₆	00 ₁₆
6FCD ₁₆	00 ₁₆	6FDD ₁₆	00 ₁₆
6FCE ₁₆	00 ₁₆	6FDE ₁₆	00 ₁₆
6FCF ₁₆	00 ₁₆	6FDF ₁₆	00 ₁₆
7FF0 ₁₆	08 ₁₆	7FF4 ₁₆	00 ₁₆
7FF1 ₁₆	88 ₁₆	7FF5 ₁₆	00 ₁₆
7FF2 ₁₆	00 ₁₆	7FF6 ₁₆	80 ₁₆
7FF3 ₁₆	00 ₁₆	7FF7 ₁₆	11 ₁₆

(4) Color Codes

The color each display character can be specified by specifying the four color outputs (R, G, B, and I) with the CRT display RAM. A color code can be specified for each character, and 2⁴=16 colors can be set.

The R, G, B, and I outputs are set by bits 0 to 3 of the color code, character or blank output is set by bit 4, and character output or blank output is specified by bit 5. The structure of the color code is shown in Figure 33.

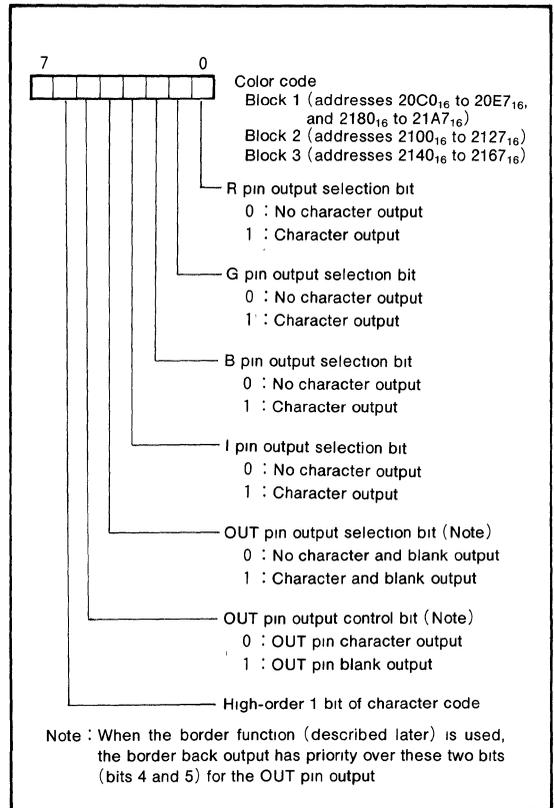


Fig. 33 Structure of color code

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(5) 1/2-Character Unit Color Specification Mode

Colors can be specified in 1/2-characters units for the characters of block 1 alone, by setting bit 4 of the CRT control register (address 00EA₁₆). In 1/2-character unit color specification mode, each half of a display character in block 1 is displayed as follows:

- Left-hand half : The color of the color code specified by bits 0 to 5 of color code specification addresses 20C0₁₆ to 20E7₁₆ in the CRT display RAM.
- Right-hand half : The color of the color code specified by bits 0 to 5 of color code specification addresses 2180₁₆ to 21A7₁₆ in the CRT display RAM.

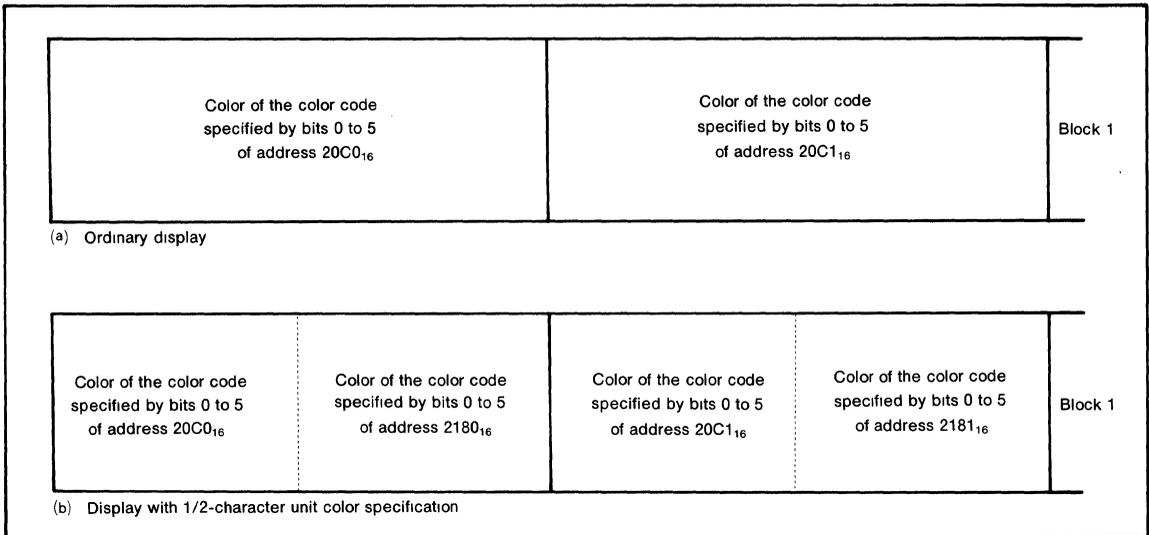


Fig. 34 Correspondence between ordinary color specification and 1/2-character unit color specification mode

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(6) Multiline Display

The M37260M6-XXXSP can ordinarily display three lines of characters, in three blocks with different vertical positions. In addition, up to 25 lines can be displayed by using CRT interrupts and the display block counter.

A CRT interrupt is a function that generates an interrupt for each block at the point at which the display of any desired number of dots has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical and horizontal position registers) of a certain block, the character display of that block starts, and an interrupt is issued at the point at which the number of dots set by the interrupt position control register is exceeded.

If the lateral character size has been set to 1 dot = 1/2 scanning line width, the CRT interrupt position can be set to 10 steps in 1 block/2 dot units; for all other scanning line widths it can be set to 20 steps in 1 block/1 dot units.

The display block counter counts the number of times the display of a block has been completed, and its contents are incremented by 1 each time the display of one block is completed.

To provide multiline display, enable CRT interrupts by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (bit 4 at address 00FE₁₆) to "1". The processing within the CRT interrupt processing routine is as follows.

- ① Read the value of the display block counter.
- ② The value of ① enables identification of a block whose display has completed (whether a CRT interrupt generation cause has occurred).
- ③ Read the interrupt position control register.
- ④ The value of ③ enables identification of the number of dots at which the CRT interrupt is to occur.
- ⑤ Write the display character code, color code, and display position of that block into the character code, color code (CRT display RAM contents), and vertical display position (contents of vertical position register) to be displayed next.

The structure of the display block counter is shown in Figure 35.

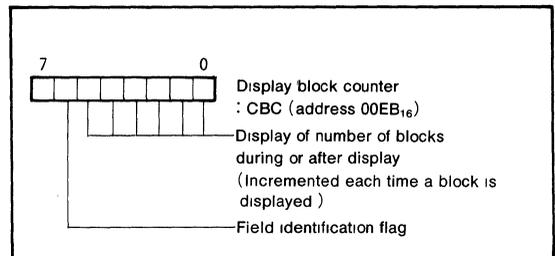


Fig. 35 Structure of display block counter

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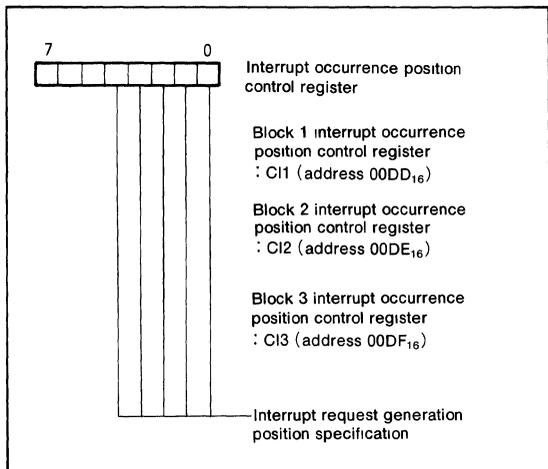


Fig. 36 Structure of interrupt position control register

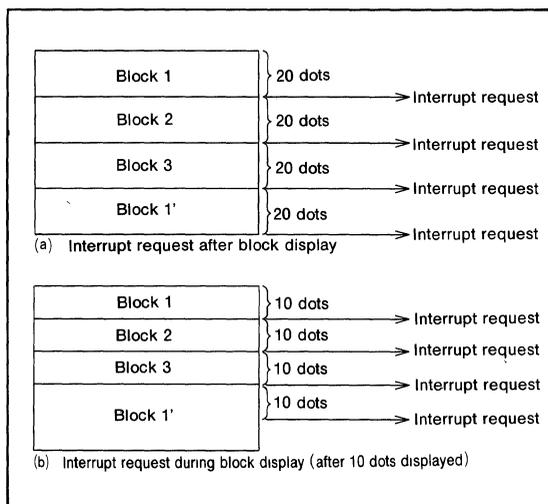


Fig. 37 Timing of CRT interrupts

(a) When lateral character size is not 1 dot = 1/2 scanning line width

Interrupt occurrence position control register					Timing of interrupt request generation
b4	b3	b2	b1	b0	
0	0	0	0	0	Interrupt after completion of 1-dot display
0	0	0	0	1	Interrupt after completion of 2-dot display
0	0	0	1	0	Interrupt after completion of 3-dot display
0	0	0	1	1	Interrupt after completion of 4-dot display
:	:	:	:	:	:
1	0	0	1	1	Interrupt after completion of 20-dot display
:	:	:	:	:	Interrupts disabled (no interrupt requests)
1	1	1	1	1	

(b) When lateral character size is 1 dot = 1/2 scanning line width

Interrupt occurrence position control register					Timing of interrupt request generation			
b4	b3	b2	b1	b0	Odd-numbered field	Even-numbered field		
0	0	0	0	X	Interrupt after completion of	1	2	dot display
0	0	0	1	X		3	4	
0	0	1	0	X		5	6	
0	0	1	1	X		7	8	
:	:	:	:	X		:	:	
1	0	0	1	X		19	20	
:	:	:	:	X	Interrupts disabled (no interrupt requests)			
1	1	1	1	X				

Fig. 38 Timing of interrupt request generation with respect to values in interrupt position control register

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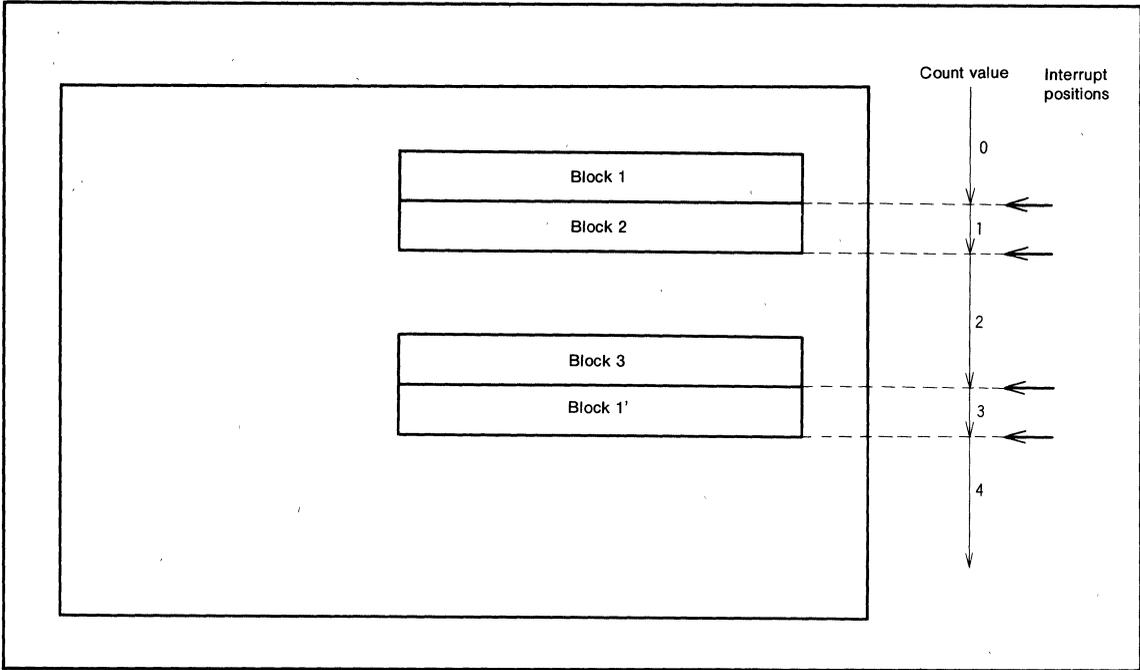


Fig. 39 Timing of CRT interrupts and values in display block counter

(7) Scanning Line Double-Count Mode

Scanning line double-count mode enables an increase in character size in the vertical direction to twice the normal size, and it can also double the display start position of the characters in the vertical direction by double-counting scanning lines. In other words, the vertical position register sets either a normal mode in which one step is one scanning line, or a scanning line double-count mode in which one step is two scanning lines.

Scanning line double-count mode can be specified by setting bit 6 of the CRT control register (address 00EA₁₆) to "1".

Since this mode functions in screen units, a change in mode while a screen is being displayed is not validated until the next screen is displayed.

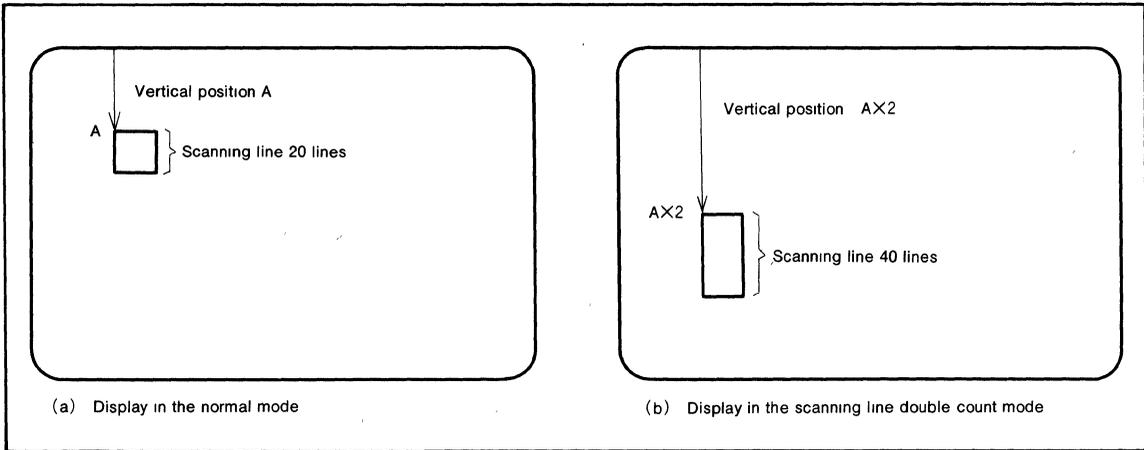


Fig. 40 Corresponding between normal mode display and scanning line double-count mode display

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(8) Border Function

A one clock (one dot) border can be drawn around each character displayed, in both the horizontal and vertical directions.

This border is output from the OUT pin. In this case, bits 4 and 5 in the color code (the OUT pin output contents) are ignored, and the border output is output from the OUT pin.

The border can be set in block units by the blank control registers (addresses 00DA₁₆ to 00DC₁₆). The relationship between the settings of the blank control registers and the border function are listed in Table 8, and the structure of the blank control registers is shown in Fig. 42.

Table 8. Corresponding between the blank control register value and border function

Blank control register		Function	Output example
BLn1	BLn0		
X	0	Normal	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border excluding character	R, G, B, I output OUT output

X : 1 or 0

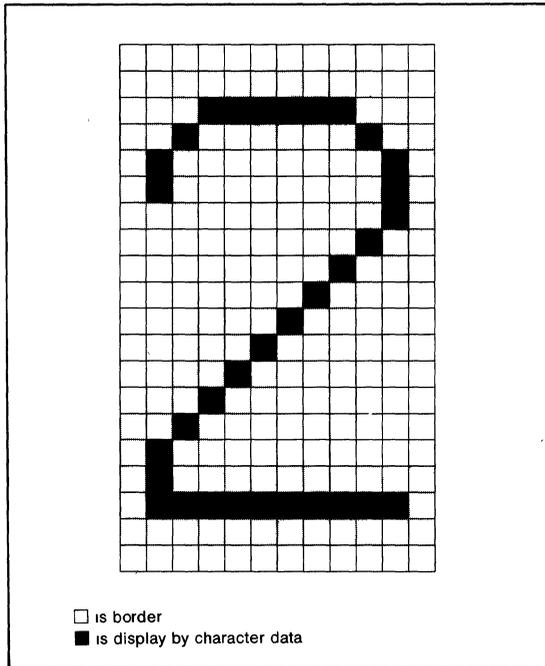


Fig. 41 Border example

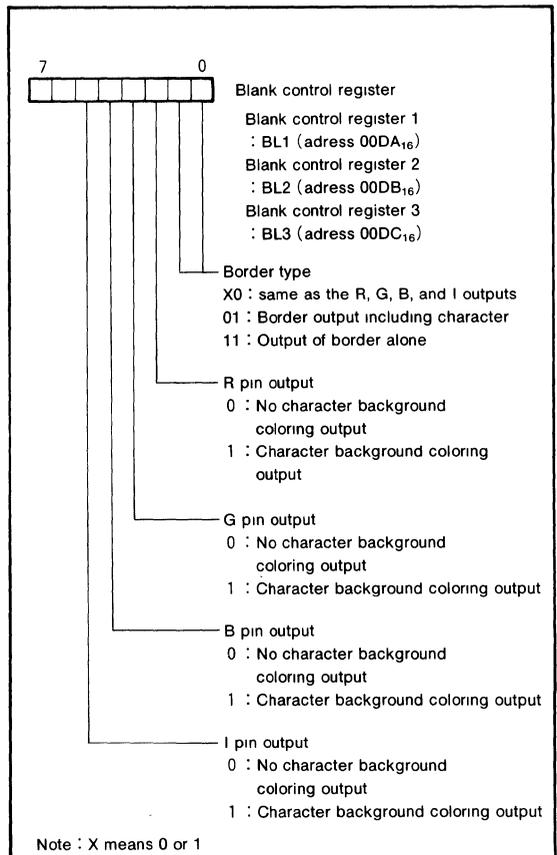
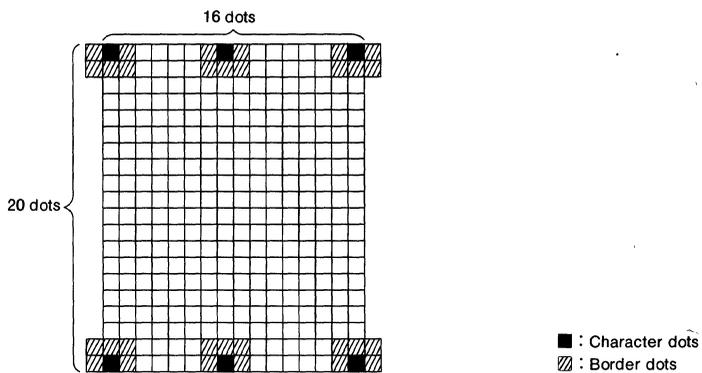


Fig. 42 Structure of blank control registers

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- (a) When vertical character size is not 1 dot = 1/2 scanning line width, borders above the uppermost dots and borders below the lowermost dots of the character font are not displayed



- (b) When vertical character size is 1 dot = 1/2 scanning line width, borders above and below the uppermost dots and borders below the lowermost dots of the character font are not displayed

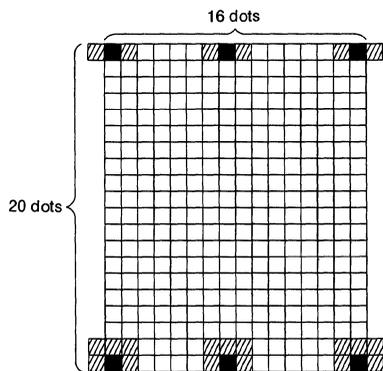


Fig. 43 Notice of border function

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(9) Character Background Color Function

The character background of the 16×20 or 12×20 area of a character (the blank part), excluding the character part itself, or character border part can be colored. The background color can be selected from 16 colors set by bits 2, 3, 4, and 5 of the blank control register. Since a background color can be set for each block, up to 15 background colors can be set for a screen when multi-line display is used.

Six character display types with background colors can be selected by combining bits 4 and 5 of the display memory color code with bits 0 and 1 of the blank control register.

Table 9. Display types

Display memory color code		Blank control register		OUT signal background coloring signal	Example of output signal	Example of character
BL2	BL1	BLn1	BLn0			
×	0	×	0	No OUT signal No background coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
0	1	×	0	OUT signal same as R, G, B, and I No background coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
×	×	0	1	Border including character Border coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
×	×	1	1	Border-only output Border coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
1	1	1	0	Blank output Background coloring (Note 1)	R, G, B, and I for character OUT R, G, B, and I for background	
1	1	0	0	Blank output Background coloring with border (Note 1, 2)	R, G, B, and I for character OUT R, G, B, and I for background	

Note 1 : If there are no character R, G, B, and I outputs, the background R, G, B, and I signals become the same as the OUT output.
 2 : When the characters (① and ③ in Figure 44) have the dots which are displayed adjoining a character (② in Figure 44) whose display type is the background coloring with border, the border of the adjoining characters (① and ③ in Figure 44), bear no relation to the display type; are displayed in the background area (② in Figure 44)

n : 1 to 3
 × : 0 or 1

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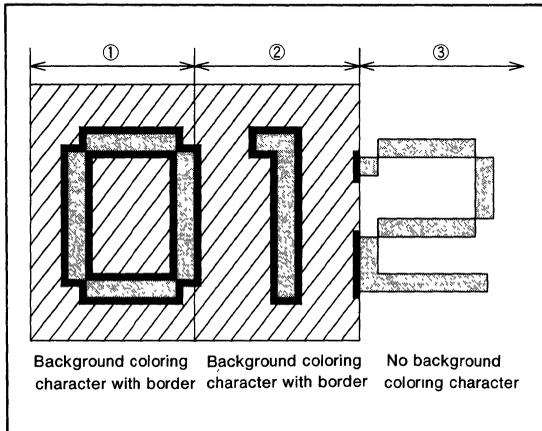


Fig. 44 Notice of character background color function

(10) Mixing Function

Color signals (MXR, MXG, MXB, MXI, and MXOUT) input from outside and color signals (R, G, B, I, and OUT) generated internally can be ORed and output as a mixed signal.

The mixing control register (address 00E5₁₆) can be used to turn on and off the mixing of the external and internal color signals, and also to specify which of the two signals has priority when they are combined.

The I pin can be switched to output an overlapped signal indicating the parts of the external color signals (MXR, MXG, MXB, MXI, and MXOUT) and internal color signals (R, G, B, I, and OUT) that are overlapped.

The MXB and MXI pins can also be used as external input pins for timer 2 and timer 3.

Examples of displays generated with an internal color signal for the letter "I" and an external color signal for the letter "O" are shown in Figure 46.

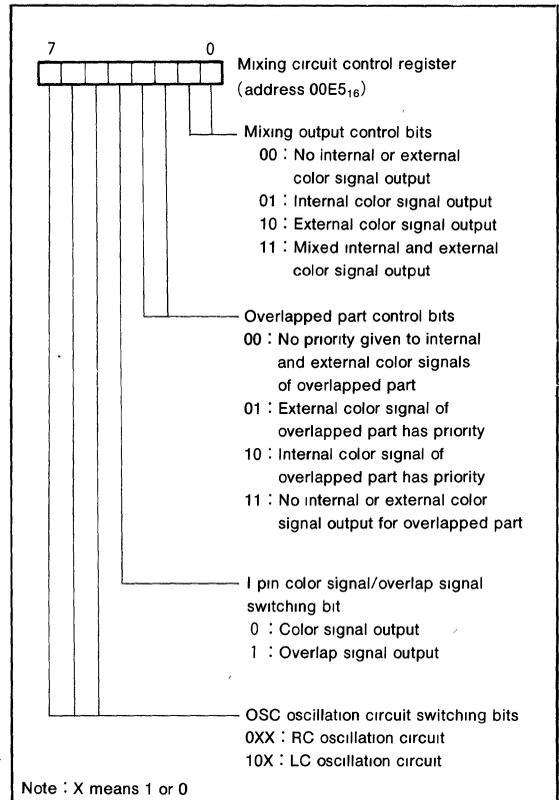


Fig. 45 Structure of mixing control register

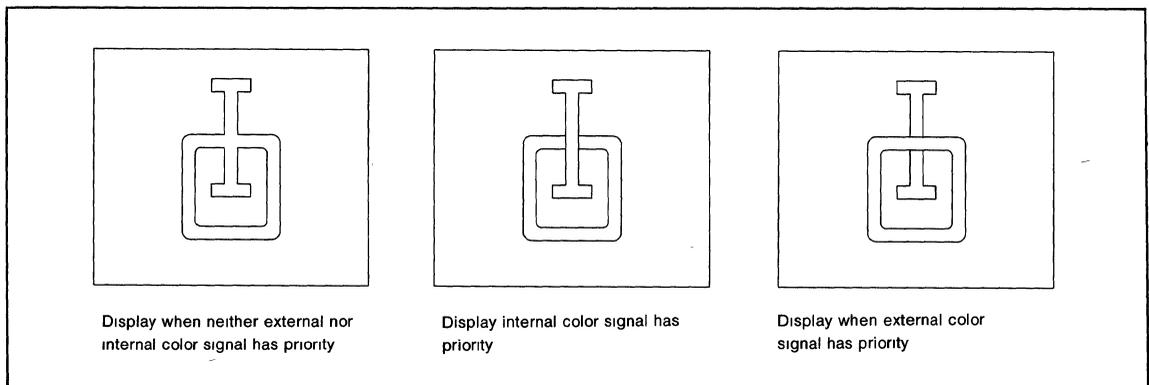


Fig. 46 Examples of display provided by mixing function

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(11) CRT Output Pin Control

The CRT output pins R, G, B, I, and OUT and the sync-generator output pin CSYN can also function as ports P4₀, P4₁, P4₂, P4₃, P4₄, and P4₅. Clear the corresponding bit of the port P4 mode register (address 00C9₁₆) to "0" to specify that pin as CRT output pin, or set it to "1" to specify it as an ordinary port P4 pin.

The input active edges of the H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, and MXOUT signals can be specified with the bits of the CRT input polarity register (address 00E8₁₆), and the output active edges of the R, G, B, I, and OUT signals can be specified with the bits of the CRT output polarity register (address 00EC₁₆). Clear a bit to "0" to specify positive active edge; set it to "1" to specify negative active edge. The structure of the CRT output polarity register is shown in Fig. 48 and that of the CRT input polarity register is shown in Fig. 49.

(12) Raster Coloring Function

An entire screen (raster) can be colored by setting the upper 5 bits of the CRT output polarity register. Since each of the R, G, B, and I pins can be switched to raster coloring output, 16 raster colors can be obtained.

If the OUT pin has been set to raster coloring output, a raster coloring signal is always output during the horizontal scanning period. This setting is necessary for erasing a background TV image.

If the R, G, B, and I pins have been set to raster coloring output, a raster coloring signal is output during the horizontal scanning period whenever there is no other color character output. This ensures that character colors do not mix with the raster color.

An example in which a magenta letter "I" and a red letter "O" are displayed with blue raster coloring is shown in Fig. 47.

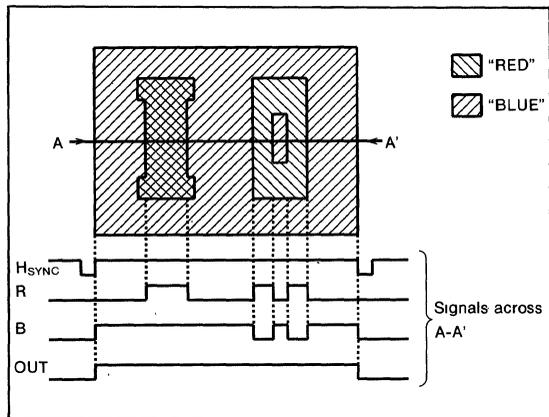


Fig. 47 Example of raster coloring

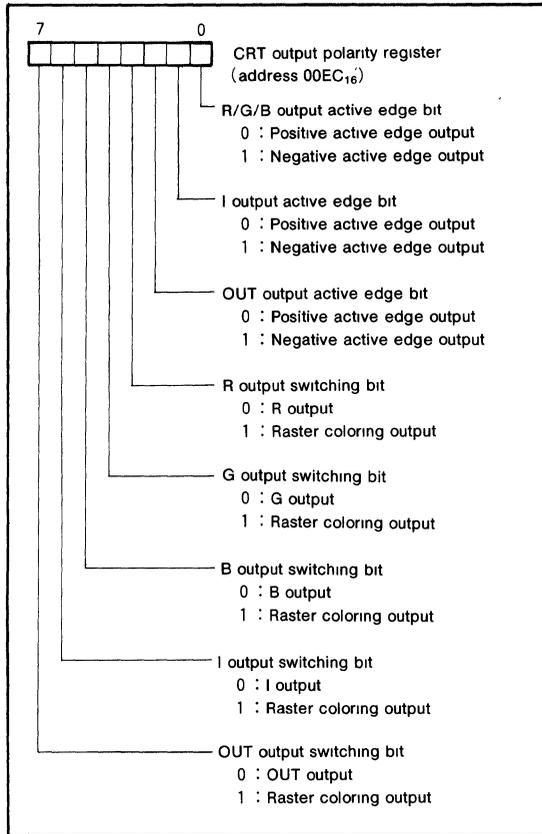


Fig. 48 Structure of CRT output polarity register

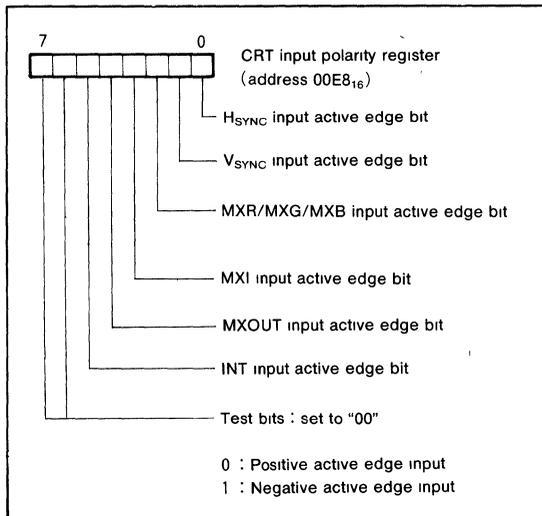


Fig. 49 Structure of CRT input polarity register

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(13) Wipe Function

① Wipe mode

The M37260M6-XXXSP allows the display area to be gradually expanded or shrunk in the vertically direction in units

of 1H (H: H_{SYNC} signal). There are three modes for this wipe method. Each mode has Down and UP modes, providing a total of six modes.

Table 10 shows the contents of each wipe mode.

Table 10. Wipe operation in each mode and the values of wipe mode register

Mode		Wipe operation	Wipe mode register			
			Bit2	Bit 1	Bit 0	
1	DOWN	Appear from upper side		0	0	1
	UP	Erase from lower side		1	0	1
2	DOWN	Erase from upper side		0	1	0
	UP	Appear from lower side		1	1	0
3	DOWN	Erase from both upper and lower side		0	1	1
	UP	Appear to both upper and lower side		1	1	1

② Wipe speed

The wipe speed is determined by the vertical synchronization (V_{SYNC}) signal. For the NTSC interlace method, assuming that

$V=16.7\text{ms} \quad 262.5 \text{ H}_{\text{SYNC}} \text{ signals per screen}$

The wipe speed is shown in Table 11.

Wipe resolution varies with each wipe mode. In mode 1 and 2, one of three resolutions (1H, 2H, 4H) can be selected. In mode 3, wipe is done in units of 4H alone.

Table 11. Wipe speed (NTSC method with interlacing, H=262.5)

Wipe resolution	Wipe speed (in all picture)
1 H unit	$16.7 \text{ (ms)} \times 262.5 \div 1 \approx 4 \text{ (s)}$
2 H unit	$16.7 \text{ (ms)} \times 262.5 \div 2 \approx 2 \text{ (s)}$
4 H unit	$16.7 \text{ (ms)} \times 262.5 \div 4 \approx 1 \text{ (s)}$

Table 12. Wipe mode and wipe resolution

Mode	Wipe resolution	Wipe speed
Mode 1	1 H Unit	about 4 second
	2 H Unit	about 2 second
Mode 2	4 H Unit	about 1 second
	4 H Unit	about 1 second

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Table 13. Relationship between wipe speed and wipe resolution

Wipe resolution	Wipe speed (full screen)		
	NTSC method	PAL method	Bi-scan method (525H/frame)
1H (2H) unit	about 4 second	about 6 second	about 4 second
2H (4H) unit	about 2 second	about 3 second	about 2 second
4H (8H) unit	about 1 second	about 1.5 second	about 1 second

Note : Values in parentheses refer to resolutions for bi-scan method.
To perform a wipe with the bi-scan method, set bit 6 of the CRT control register to "1"

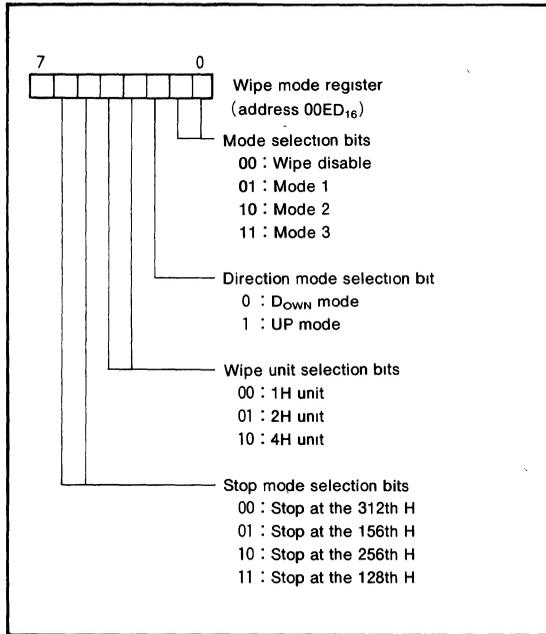


Fig. 50 Structure of wipe mode register

SYNC GENERATOR

The sync generator can output a total of six synchronization signals : NTSC method with interlacing, without interlacing, or bi-scan, and PAL method with interlacing, without interlacing, or bi-scan. Since the synchronization signal is output from the CSYN/P4₅ pin, set bit 5 of the port P4 mode register to "0".

Activate the sync generator by clearing bit 7 of the sync generator control register to "0" and setting bit 4 to match the X_{IN} clock frequency.

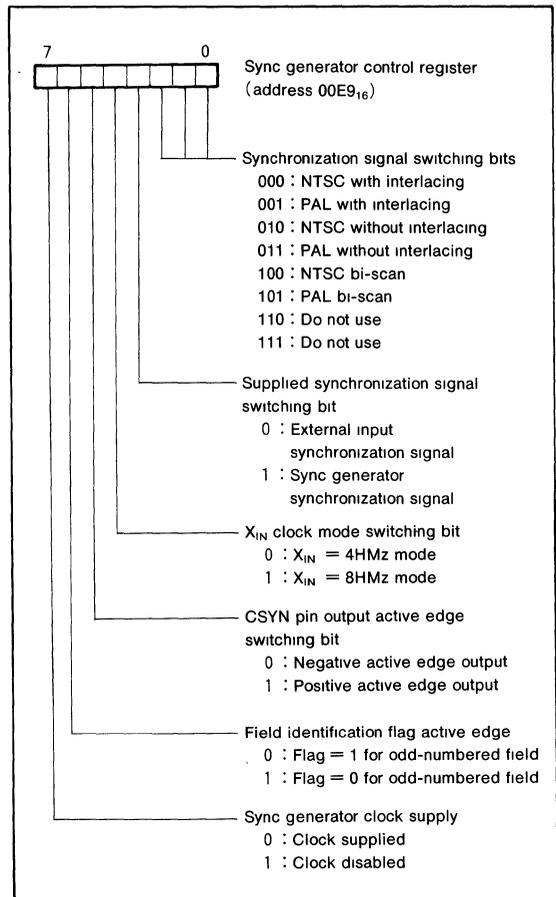
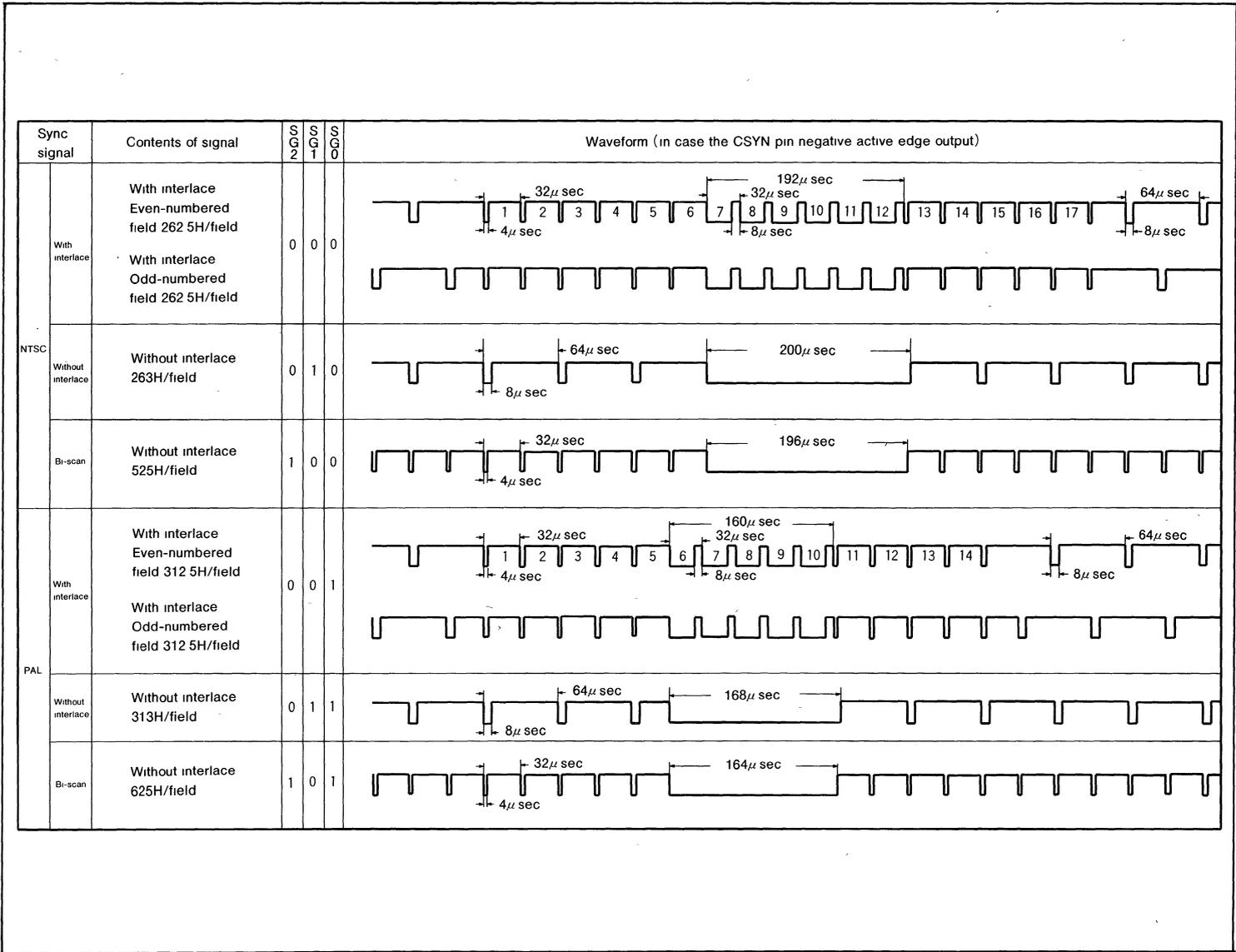


Fig. 51 Structure of sync generator control register



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RESET CIRCUIT

The M37260M6-XXXSP is reset according to the sequence shown in Figure 53. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than $2\mu\text{s}$ while the power voltage is $5\text{V} \pm 10\%$

and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 54.

An example of the reset circuit is shown in Figure 55. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

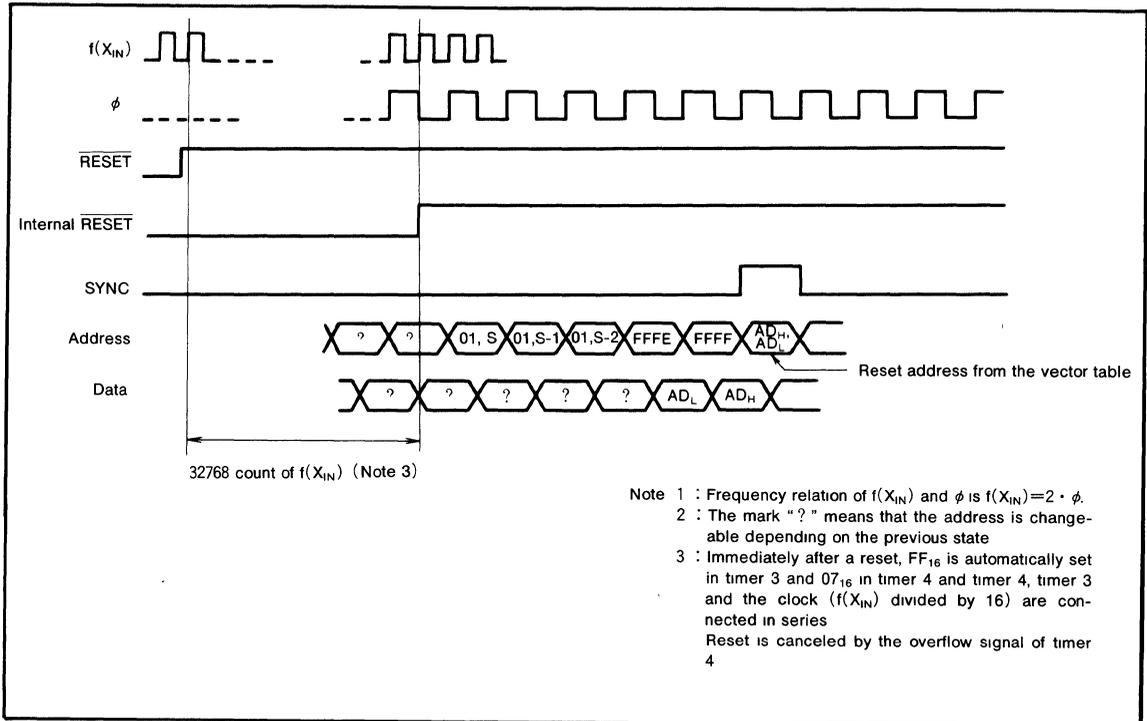


Fig. 53 Timing diagram in reset

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

	Address	Contents of register
(1) Port P0 direction register	0 0 C 1 ₁₆	00 ₁₆
(2) Port P1 direction register	0 0 C 3 ₁₆	00 ₁₆
(3) Port P2 direction register	0 0 C 5 ₁₆	00 ₁₆
(4) Port P3 direction register	0 0 C 7 ₁₆	X X 0 0 0 0 0 0
(5) Port P4 mode register	0 0 C 9 ₁₆	00 ₁₆
(6) Serial I/O mode register 1	0 0 C D ₁₆	00 ₁₆
(7) Serial I/O mode register 2	0 0 C E ₁₆	X X X 0 0 0 0 0
(8) Character size register 1	0 0 D 7 ₁₆	X
(9) Character size register 2	0 0 D 8 ₁₆	
(10) Character size register 3	0 0 D 9 ₁₆	X
(11) Blank control register 1	0 0 D A ₁₆	X X
(12) Blank control register 2	0 0 D B ₁₆	X X
(13) Blank control register 3	0 0 D C ₁₆	X X
(14) Block 1 interrupt occurrence position control register	0 0 D D ₁₆	X X X
(15) Block 2 interrupt occurrence position control register	0 0 D E ₁₆	X X X
(16) Block 3 interrupt occurrence position control register	0 0 D F ₁₆	X X X
(17) Horizontal position register	0 0 E 0 ₁₆	00 ₁₆
(18) Vertical position register 4	0 0 E 4 ₁₆	X X
(19) Mixing circuit control register	0 0 E 5 ₁₆	00 ₁₆
(20) CRT input polarity register	0 0 E 8 ₁₆	00 ₁₆
(21) Sync generator control register	0 0 E 9 ₁₆	00 ₁₆
(22) CRT control register	0 0 E A ₁₆	00 ₁₆
(23) Display block counter	0 0 E B ₁₆	X 0 0 0 0 0 0 0
(24) CRT output polarity register	0 0 E C ₁₆	00 ₁₆
(25) Wipe mode register	0 0 E D ₁₆	X 0 0 0 0 0 0 0
(26) Timer 1	0 0 F 0 ₁₆	FF ₁₆
(27) Timer 2	0 0 F 1 ₁₆	07 ₁₆
(28) Timer 3	0 0 F 2 ₁₆	FF ₁₆
(29) Timer 4	0 0 F 3 ₁₆	07 ₁₆
(30) Timer 12 mode register	0 0 F 4 ₁₆	X X X 0 0 0 0 0
(31) Timer 34 mode register	0 0 F 5 ₁₆	X X X 0 0 0 0 0
(32) Special mode register 1	0 0 F 7 ₁₆	0 0 0 X X X 0 0
(33) Special mode register 2	0 0 F 8 ₁₆	X 0 0 0 0 0 0 0
(34) CPU mode register	0 0 F B ₁₆	1 1 1 0 1 1 0 0
(35) Interrupt request register 1	0 0 F C ₁₆	X X 0 0 0 0 0 0
(36) Interrupt request register 2	0 0 F D ₁₆	X X X X X 0 0 0
(37) Interrupt control register 1	0 0 F E ₁₆	X X 0 0 0 0 0 0
(38) Interrupt control register 2	0 0 F F ₁₆	X X X X X 0 0 0
(39) Processor status register		1
(40) Program counter	P C _H	Contents of address FFFF ₁₆
	P C _L	Contents of address FFFE ₁₆

Note Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values
At reset, "0" is read from the bits marked X

Fig. 54 - Internal state of microcomputer at reset

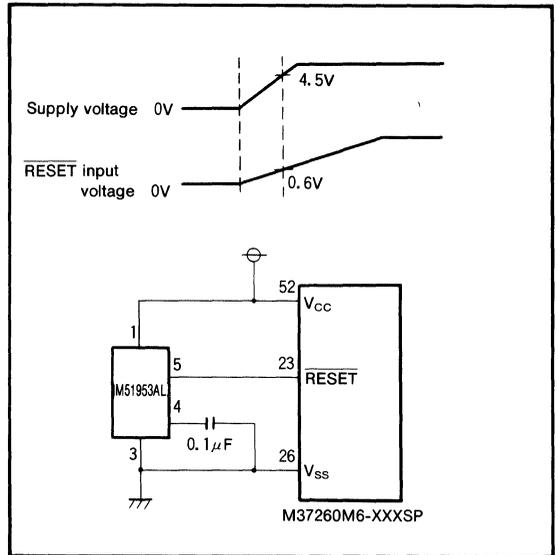


Fig. 55 Example of reset circuit

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I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 3), port P0 can be accessed at zero page memory address $00C0_{16}$.

Port P0 has a direction register (address $00C1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address $00FB_{16}$), three different modes can be selected; single-chip mode, memory expansion mode and microprocessor mode.

In these modes it functions as address (A_7 to A_0) output port (excluding single-chip mode) For more details, refer the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A_{15} to A_8) output port.

For more details, refer the processor mode information.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data (D_7 to D_0) input/output port. For more details, refer the processor modes information.

(4) Port P3

Port P3 is a 6-bit I/O port with function similar to port P0, but the output structure of $P3_0$, $P3_1$ is CMOS output, and $P3_2$ - $P3_5$ is N-channel open drain.

$P3_2$ is in common with the external input pin INT and the serial I/O input pin CS.

When a serial I/O function is selected, $P3_3$ to $P3_5$ work as $\overline{S_{RDY}}$, S_{IN}/S_{OUT} , and S_{CLK} pins.

When a special serial I/O function is selected, $P3_4$ and $P3_5$ work as SDA and SCL pins.

In microprocessor mode or memory expansion mode, $P3_0$ and $P3_1$ work R/ \overline{W} output pin and SYNC output pin.

(5) OSC1, OSC2 pins

Clock input/output pins for CRT display function.

(6) H_{SYNC} , V_{SYNC} pins

H_{SYNC} is a horizontal synchronizing signal input pin for CRT display.

V_{SYNC} is a vertical synchronizing signal input pin for CRT display.

(7) R, G, B, I, OUT pins

This is a 5-bit output pin for CRT display and in common with $P4_0$ - $P4_4$.

(8) CSYN pin

CSYN pin outputs the composite sync signal by the sync generator.

CSYN pin is in common with $P4_5$.

(9) MXR, MXG, MXB, MXI, MXOUT pins

These are video signal input pins for mixing function.

MXR, MXG, MXB, MXI, and MXOUT are in common with the input port $P5_2$, $P5_3$, $P5_4$, $P5_5$, $P5_6$. MXB and MXI are also in common with the external clock input pins TIM2 and TIM3.

(10) ϕ pin

The internal system clock ($1/2$ the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

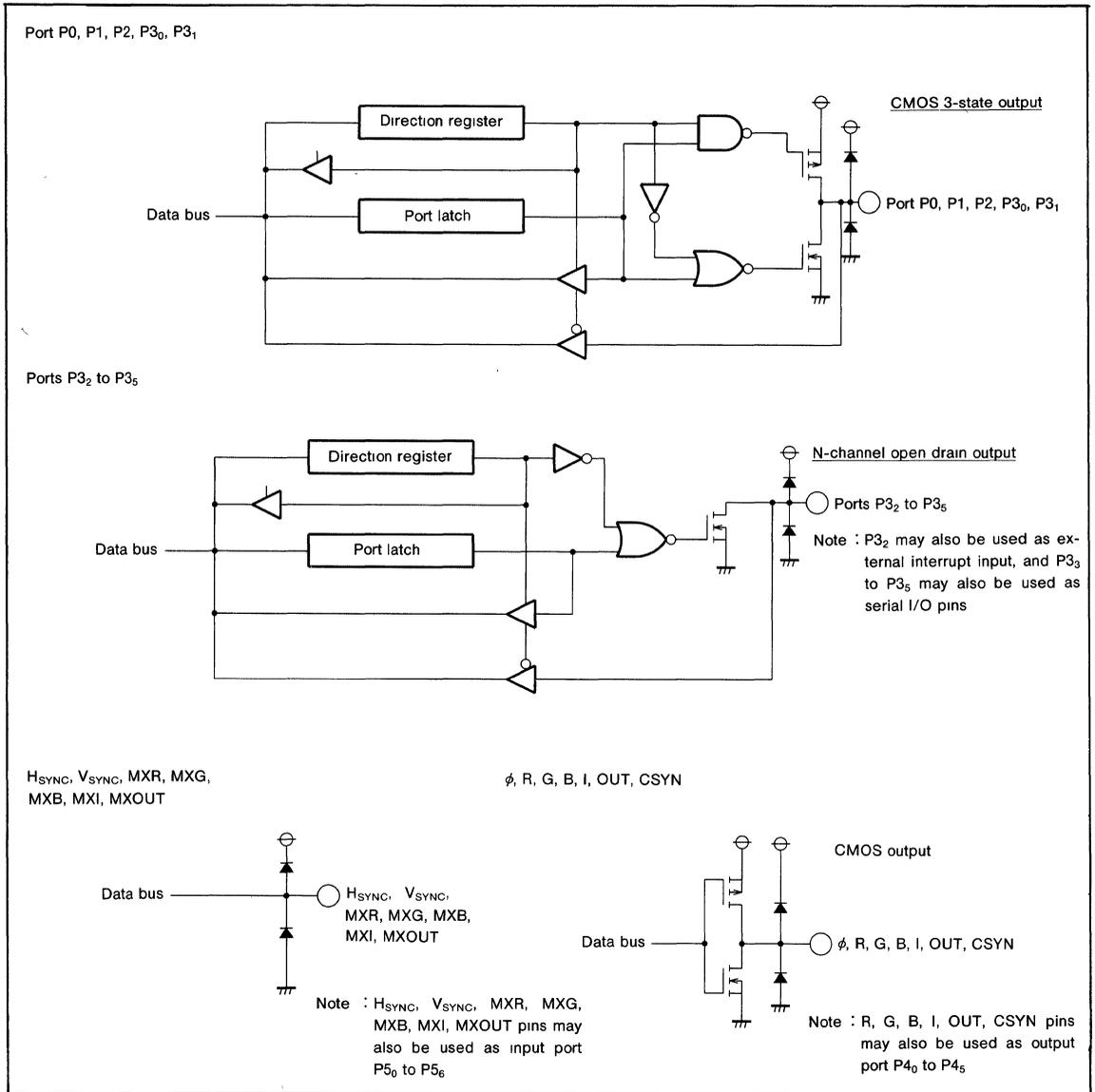


Fig. 56 Ports P0 to P3, H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, MXOUT, ϕ , R, G, B, I, OUT and CSYN pin block diagram

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

PROCESSOR MODE

By changing the contents of the processor mode bits (bits 0 and 1 at address $00FB_{16}$), three different operation modes can be selected; single-chip mode, memory expansion mode, and microprocessor mode.

In the memory expansion mode and the microprocessor mode, ports P0 to P3 can be used as address, and data input/output pins.

Figure 60 shows the functions of ports P0 to P3.

The memory map for the single-chip mode is shown in Figure 2 and for other modes, in Figure 57.

By connecting CNV_{SS} to V_{SS} , all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the

microprocessor mode.

The three different modes are explained as follows:

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS} . Ports P0-P3 will work as I/O ports.

(2) Memory expansion mode [01]

The microcomputer will be placed in the memory expansion mode after connecting CNV_{SS} to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and its I/O pin function is lost.

Port P2 becomes the data bus of D_7 to D_0 (including instruction code) and loses its I/O port function. Port $P3_0$ and $P3_1$ works as R/W output pin and SYNC output pin.

(3) Microprocessor mode [10]

The microcomputer will be placed in the microprocessor mode after connecting CNV_{SS} to V_{CC} and initiating a reset or connecting CNV_{SS} to V_{SS} and processor mode bits are set to "10". In this mode, the internal ROM is inhibited so the external memory is required. Other functions are same as the memory expansion mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 14.

Note 1 : Use the M37260M6-XXXSP in the microprocessor mode or the memory expansion mode only at program development.

The standard is assured only in the single-chip mode.

Note 2 : The display ROM cannot be placed on the external memory area.

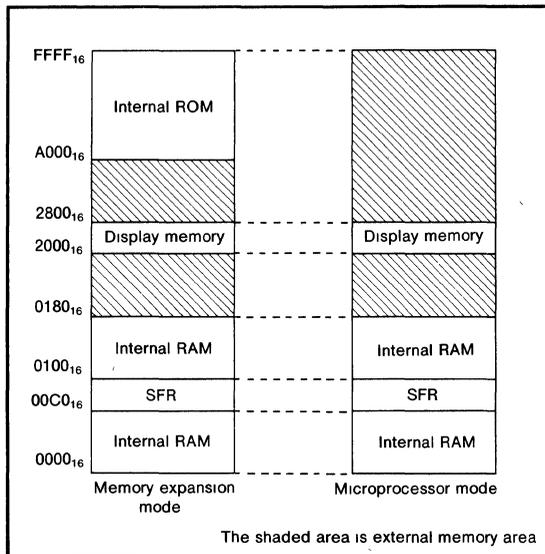


Fig. 57 External memory area at each processor mode

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

Port	CM ₁	0	0	1
	CM ₀	0	1	0
Mode		Single-chip mode	Memory expansion mode	Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P3			Same as left	

Fig. 58 Processor mode and function of ports P0 to P3 (CM₁, CM₀ : bit 1 and bit 0 of CPU mode register)

Table 14. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode • Memory expansion mode • Microprocessor mode 	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V _{CC}	<ul style="list-style-type: none"> • Microprocessor mode 	The microprocessor mode is set by the reset

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Data-set timing of CPU mode register

The value of bit 0 and bit 1 in the CPU mode register is set at the second rising edge of the SYNC signal after the writing instruction is executed.

However the value of bit 2 and bit 3 is set at the first rising edge of the SYNC signal, just as in the other registers.

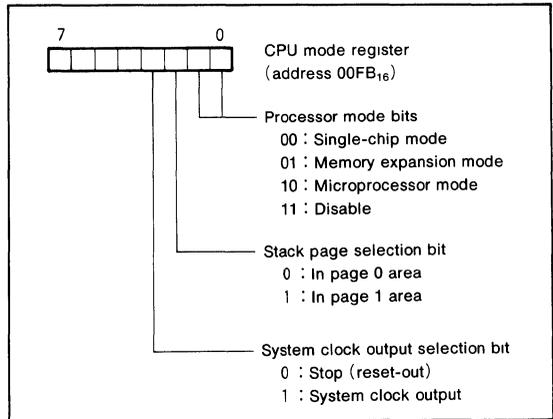


Fig. 59 Structure of CPU mode register

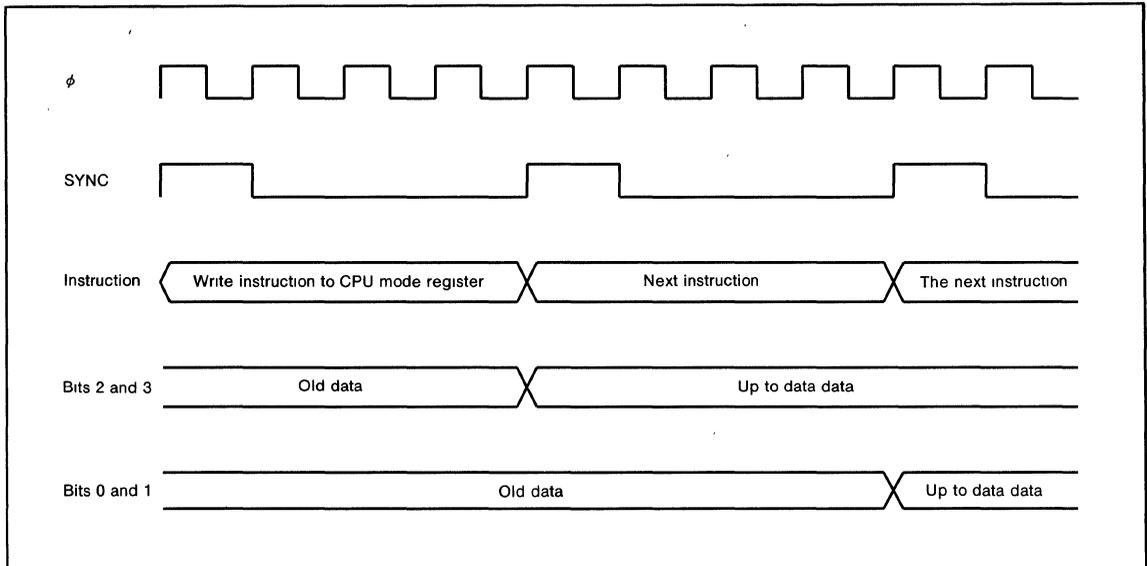


Fig. 60 Data-set timing of CPU mode register

Table 15. The value of CPU mode register at reset

CNV _{SS} pin	b7	CPU mode register						b0
V _{SS}	1	1	1	0	1	1	0	0
V _{CC}	1	1	1	0	1	1	1	0

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 63.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timer 3 and timer 4 are connected automatically and FF₁₆ is set in the timer 3, 01₁₆ is set in the timer 4, and timer 3 count source is forced to $f(X_{IN})$ divided by 16. This connection is cleared when an external interrupt is accepted or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 61.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 62. X_{IN} is the input, and X_{OUT} is open.

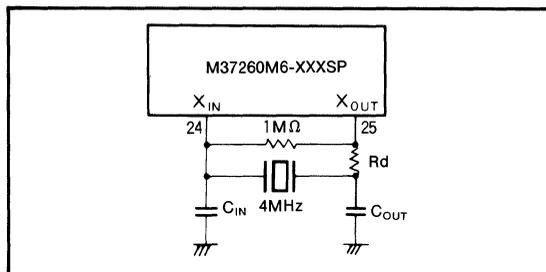


Fig. 61 External ceramic resonator circuit

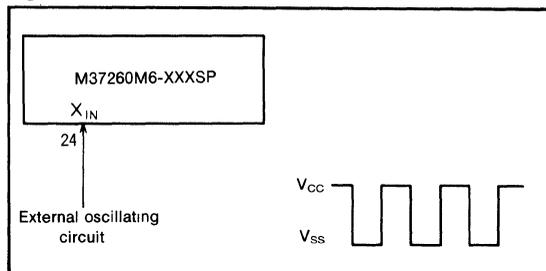
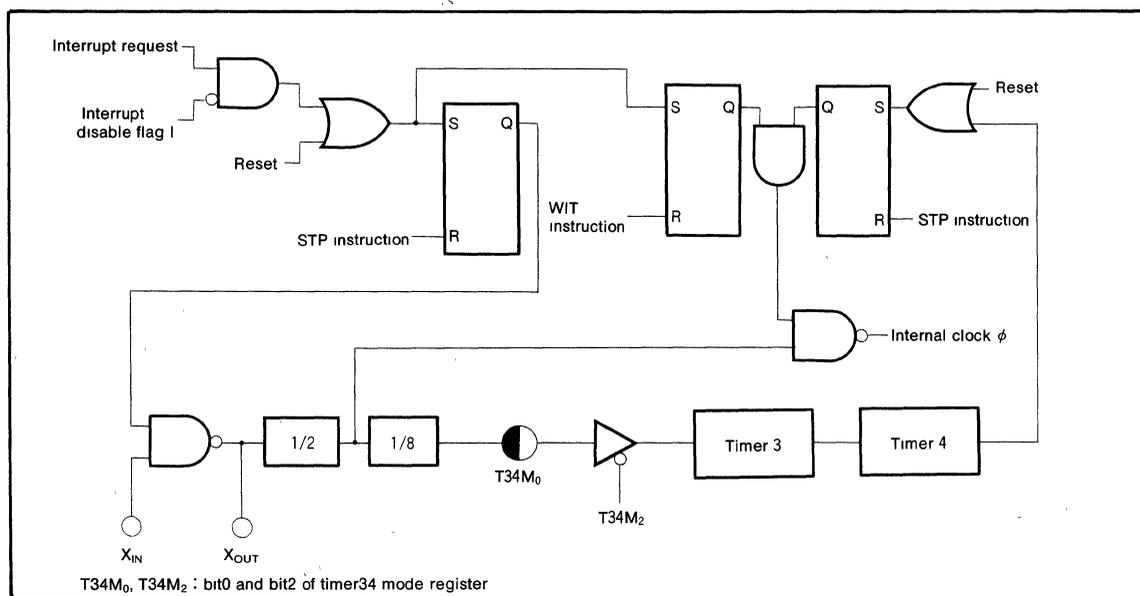


Fig. 62 External clock input circuit



T34M₀, T34M₂ : bit0 and bit2 of timer34 mode register

Fig. 63 Block diagram of clock generating circuit

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DISPLAY OSCILLATION CIRCUIT

The CRT display clock oscillation circuit has built-in RC and LC oscillation circuits, so that a clock can be obtained simply by connecting an RC or LC circuit between the OSC1 and OSC2 pins.

Select the RC or LC oscillation circuit by setting bits 6 and 7 of the mixing control register (see the structure of the mixing control register in Figure 45).

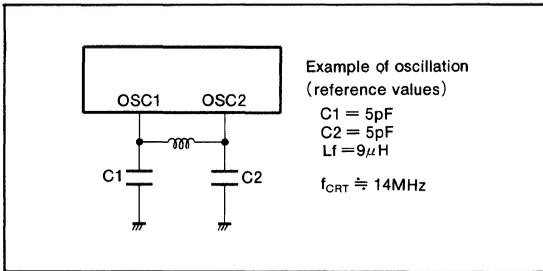


Fig. 64 Display oscillation circuit

AUTO CLEAR CIRCUIT

When power is supplied, the auto-clear function can be performed by connecting the following circuit to reset pin.

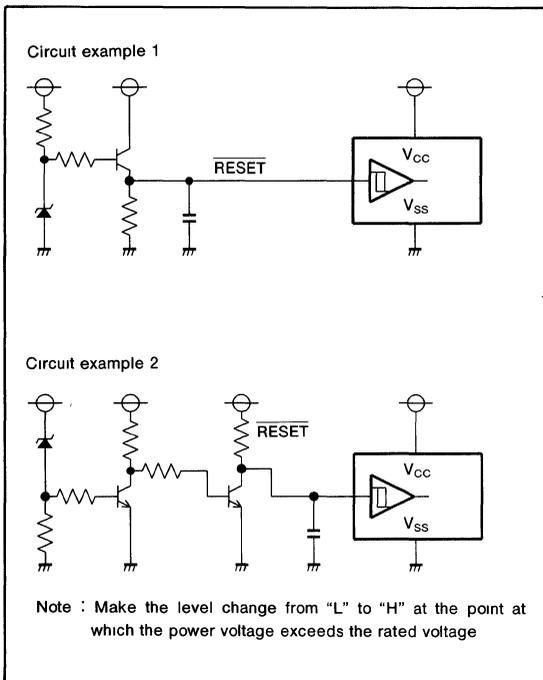


Fig. 65 Auto clear circuit example

PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (4) A NOP instruction must be used after the execution of a PLP instruction.
- (5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM order confirmation from
- (2) mask specification from
- (3) ROM data EPROM 3 sets

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3 to 6	V
V_I	Input voltage CNV_{SS}		-0.3 to 6	V
V_I	Input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7, P3_0-P3_5, MXR, MXG, MXB, MXI, MXOUT, H_{SYNC}, V_{SYNC}, \overline{RESET}$	With respect to V_{SS} Output transistors are at "off" state	-0.3 to $V_{CC}+0.3$	V
V_O	Output voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7, P3_0-P3_5, R, G, B, I, OUT, CSYN, X_{OUT}, OSC2$		-0.3 to $V_{CC}+0.3$	V
I_{OH}	Circuit current $R, G, B, I, OUT, CSYN, P0_0-P0_7, P1_0-P1_7, P2_0-P2_7, P3_0, P3_1$		0 to 1 (Note 1)	mA
I_{OL1}	Circuit current $R, G, B, I, OUT, CSYN, P0_0-P0_7, P1_0-P1_7, P2_0-P2_7, P3_0-P3_5$		0 to 2 (Note 2)	mA
P_d	Power dissipation	$T_a=25^\circ C$	550	mW
T_{opr}	Operating temperature		-10 to 70	$^\circ C$
T_{stg}	Storage temperature		-40 to 125	$^\circ C$

RECOMMENDED OPERATING CONDITIONS ($T_a=-10$ to $70^\circ C, V_{CC}=5V \pm 10\%$ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage (Note 3) During the CPU and CRT operation	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	"H" input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7, P3_0-P3_5, H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, MXOUT, \overline{RESET}, X_{IN}, OSC1$	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $P3_4, P3_5$	$0.7V_{CC}$		V_{CC}	V
V_{IL1}	"L" input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7, P3_0, P3_1, P3_3, MXR, MXG, MXOUT$	0		$0.4V_{CC}$	V
V_{IL2}	"L" input voltage $P3_2, P3_4, P3_5, H_{SYNC}, V_{SYNC}, \overline{RESET}, X_{IN}, OSC1, MXB, MXI$	0		$0.2V_{CC}$	V
I_{OH}	"H" average output current (Note 1) $R, G, B, I, OUT, CSYN, P0_0-P0_7, P1_0-P1_7, P2_0-P2_7, P3_0, P3_1$			1	mA
I_{OL}	"L" average output current (Note 2) $R, G, B, I, OUT, CSYN, P0_0-P0_7, P1_0-P1_7, P2_0-P2_7, P3_0-P3_5$			2	mA
f_{CPU}	Oscillating frequency (for CPU operation) (Note 4)	3.6	4.0	8.1	MHz
f_{CRT}	Oscillating frequency (for CRT display)	12.0	14.0	16.0	MHz
f_{HS}	Input frequency INT, TIM2, TIM3, SCL			100	kHz
f_{HS}	Input frequency S_{CLK}			1	MHz

- Note 1 : The total current that flows out of the IC should be 20mA (max)
 2 : The total current should be 30mA (max)
 3 : Apply 0.022 μ F or greater capacitance externally between the $V_{CC}-V_{SS}$ power supply pins so as to reduce power source noise
 Also apply 0.068 μ F or greater capacitance externally between the $V_{CC}-CNV_{SS}$ pins
 4 : Use a quartz crystal oscillator or a ceramic resonator for the CPU oscillation circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

ELECTRIC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $f(X_{IN})=4MHz$, $T_a=-10$ to $70^\circ C$ unless otherwise noted)

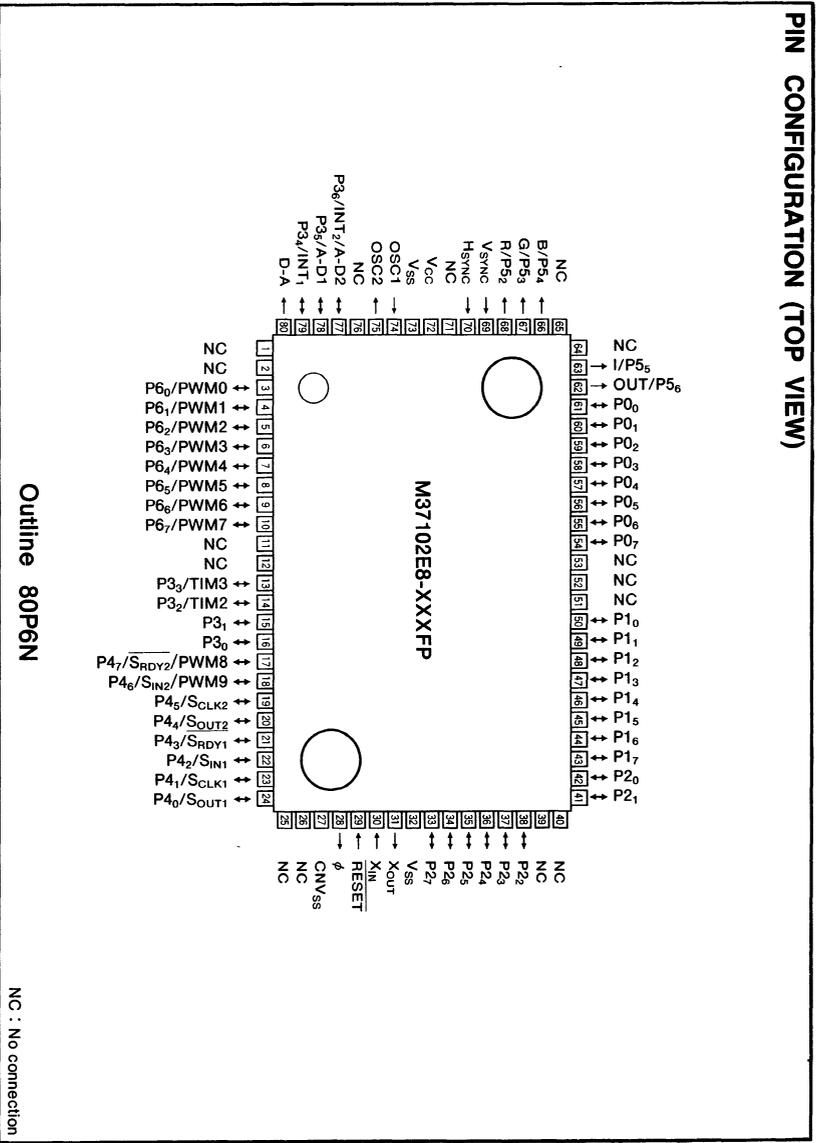
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
I_{CC}	Supply current	$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT OFF		10	20	mA
		$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT ON		20	50	
		At stop mode			300	μA
V_{OH}	"H" output voltage $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0$, $P3_1$, R, G, B, I, OUT, CSYN	$V_{CC}=4.5V$ $I_{OH}=-0.5mA$	2.4			V
V_{OL}	"L" output voltage $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0-P3_3$, R, G, B, I, OUT, CSYN	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
	"L" output voltage $P3_4$, $P3_5$	$V_{CC}=4.5V$ $I_{OL}=3mA$			0.4	
$V_{T+}-V_{T-}$	Hysteresis \overline{RESET}	$V_{CC}=5.0V$		0.5	0.7	V
	Hysteresis (Note 1) H_{SYNC} , V_{SYNC} , $P3_2$, $P3_4$, $P3_5$, MXB, MXI	$V_{CC}=5.0V$		0.5	1.3	
I_{OZH}	"H" input leak current \overline{RESET} , $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0-P3_5$, H_{SYNC} , V_{SYNC} , MXR, MXG, MXB, MXI, MXOUT	$V_{CC}=5.5V$ $V_O=5.5V$			5	μA
I_{OZL}	"L" input leak current \overline{RESET} , $P0_0-P0_7$, $P1_0-P1_7$, $P2_0-P2_7$, $P3_0-P3_5$, H_{SYNC} , V_{SYNC} , MXR, MXG, MXB, MXI, MXOUT	$V_{CC}=5.5V$ $V_O=0V$			5	μA

Note 1. $P3_2$, MXB, MXI have the hysteresis when these pins are used as interrupt input pins or timer input pins.
 $P3_4$, $P3_5$ have the hysteresis when these pins are used as serial I/O and special serial I/O ports.

MITSUBISHI MICROCOMPUTERS
M37102E8-XXXXSP/FP
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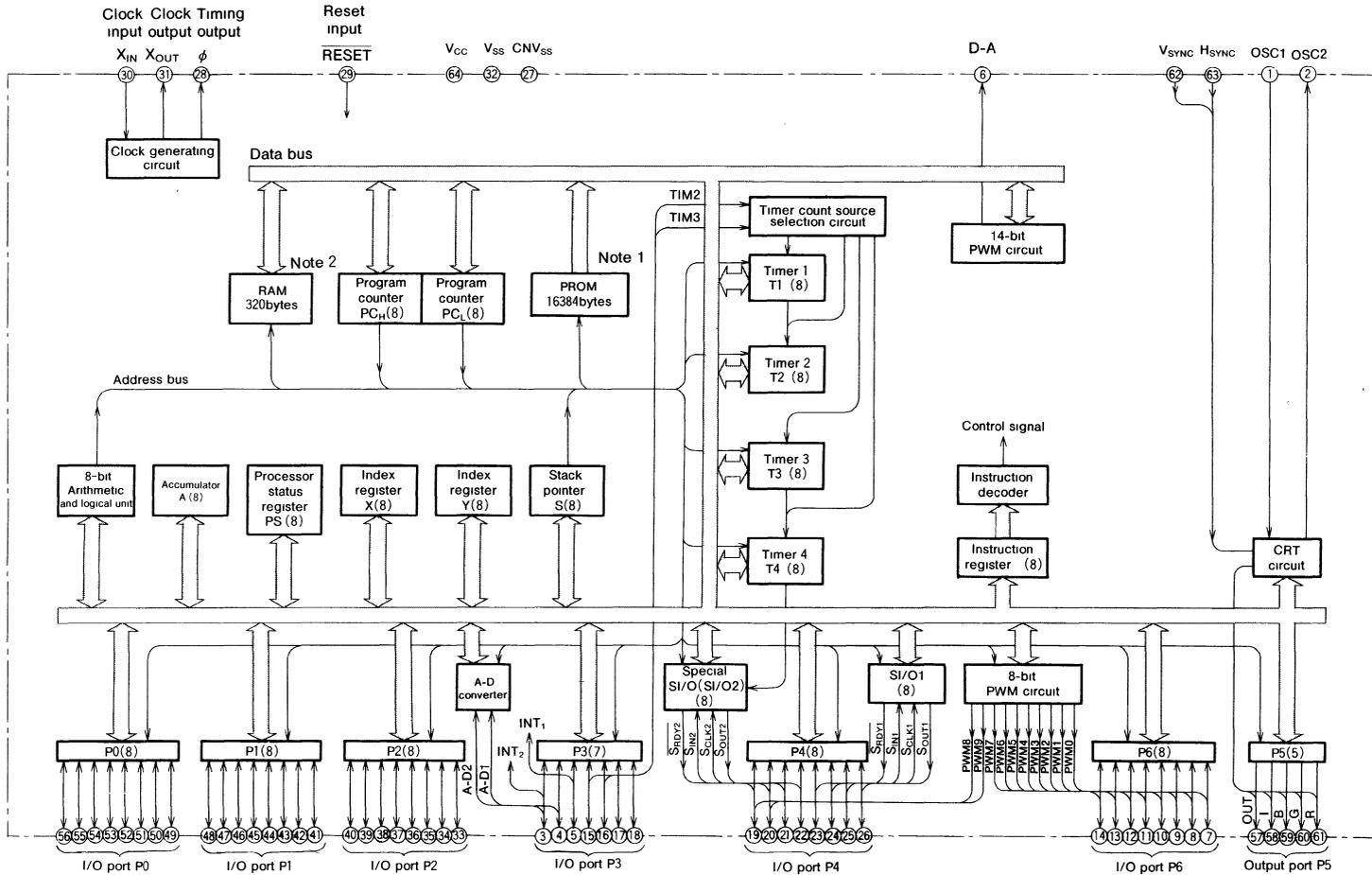
PROM VERSION of M37102M8-XXXXSP/FP, M37201M6-XXXXSP

PIN CONFIGURATION (TOP VIEW)





M37102E8-XXXSP BLOCK DIAGRAM



Note 1 24576 bytes for M37201E6-XXXSP
 2 384 bytes for M37201E6-XXXSP

PROM VERSION of M37102M8-XXXSP/FP, M37201M6-XXXSP

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PROM VERSION of M37102M8-XXXSP/FP, M37201M6-XXXSP

FUNCTIONS OF M37102E8-XXXSP/FP, M37201E6-XXXSP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		1 μ s (minimum instructions, at 4MHz frequency)	
Clock frequency		4MHz	
Memory size	M37102E8-XXXSP/FP	ROM	16384 bytes
		RAM	320 bytes
	M37201E6-XXXSP	ROM	24576 bytes
		RAM	384 bytes
Input/Output ports	P0, P1, P2	I/O	8-bitX3
	P3 ₀ , P3 ₁	I/O	2-bitX1
	P3 ₂ -P3 ₆	I/O	5-bitX1 (can be used as timer input pins, INT ₁ , INT ₂ input pins and A-D input pins)
	P4	I/O	8-bitX1 (can be used as serial I/O function pins and PWM output pins)
	P5	Output	5-bitX1 (can be used as R, G, B, I, OUT pins)
	P6	I/O	8-bitX1 (can be used as PWM output pins)
Serial I/O		8-bitX2 (Special serial I/O (8-bit)X1)	
Timers		8-bit timerX4	
Subroutine nesting		96levels (max)	
Interrupt		Two external interrupts, nine internal interrupts, one software interrupt	
Clock generating circuit		Built-in circuit (externally connected ceramic or quartz crystal oscillator)	
Supply voltage		5V \pm 10%	
Power dissipation	at CRT display ON	110mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)	
	at CRT display OFF	55mW (clock frequency X _{IN} =4MHz, V _{CC} =5.5V, Typ)	
	at stop mode	1.65mW (Max)	
Input/Output characteristics	Input/Output voltage	5V (Port P4 ₆ , P4 ₇ , P6 ₀ -P6 ₇)	
	Output current	10mA (Port P2 ₄ -P2 ₇)	
Operating temperature range		-10 to 70°C	
Device structure		CMOS silicon gate process	
Package	M37102E8-XXXSP, M37201E6-XXXSP	64-pin shrink plastic molded DIP	
	M37102E8-XXXFP	80-pin plastic molded QFP	
CRT display function	Number of character	24 charactersX3 lines	
	Kinds of character	126 (12X16 dots)	

MITSUBISHI MICROCOMPUTERS
M37102E8-XXXSP/FP
M37201E6-XXXSP

PROM VERSION of M37102M8-XXXSP/FP, M37201M6-XXXSP

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Single-chip	Power supply		Power supply inputs 5V±10% (typ) to V _{CC} , and 0V to V _{SS}
	EPROM			Power supply inputs 5V, or 6V (writing to built-in PROM) to V _{CC} , and 0V to V _{SS}
CNV _{SS}	Single-chip	CNV _{SS}	Input	This is connected to V _{SS}
	EPROM			V _{PP} inputs when writing to built-in PROM or verify check of built-in PROM contents
RESET	Single-chip	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
	EPROM			Input "L" level
X _{IN}	Single-chip /EPROM	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected to the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}		Clock output	Output	
φ	Single-chip	Timing output	Output	This is the timing output pin and has the reset out signal output function
	EPROM			This pin is setting to open
P0 ₀ -P0 ₇	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
	EPROM	Address input	Input	Low-order 8-bit of address is input
P1 ₀ -P1 ₇	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0
	EPROM	Address input	Input	High-order 8-bit of address is input.
P2 ₀ -P2 ₇	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as port P0
	EPROM	Data input/output		8-bit data is input or output.
P3 ₀ -P3 ₆	Single-chip	I/O port P3	I/O	Port P3 is a 7-bit I/O port and has basically the same function as port P0, but the output structure of P3 ₀ and P3 ₁ is CMOS output and the output structure of P3 ₂ -P3 ₆ is N-channel open drain. P3 ₂ and P3 ₃ are in common with external clock input pins of timer 2 and timer 3. P3 ₄ and P3 ₅ are in common with external interrupt input pins INT ₁ and INT ₂ . P3 ₅ and P3 ₆ are in common with analog input pins of A-D converter (A-D1, A-D2)
	EPROM	Mode input	Input	P3 ₀ and P3 ₁ are the input pins as \overline{OE} and \overline{CE} . P3 ₂ and P3 ₃ are connected to V _{CC} . P3 ₄ -P3 ₆ are connected to V _{SS} .
P4 ₀ -P4 ₇	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. When serial I/O1 is used, P4 ₀ , P4 ₁ , P4 ₂ , and P4 ₃ work as S _{OUT1} , S _{CLK1} , S _{IN1} and \overline{S} R _{DY1} pins, respectively. When serial I/O2 is used, P4 ₄ , P4 ₅ , P4 ₆ , and P4 ₇ work as S _{OUT2} , S _{CLK2} , S _{IN2} and \overline{S} R _{DY2} pins, respectively. Also P4 ₆ , P4 ₇ are in common with PWM output pins of PWM8 and PWM 9
	EPROM	Input port P4	Input	P4 ₀ -P4 ₆ are all connected to V _{SS} , and P4 ₇ is connected to V _{CC}
OSC1 OSC2	Single-chip	Clock I/O for CRT display	I/O	This is the I/O pins of the clock generating circuit for the CRT display function
	EPROM		Output	These pins are setting to open

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PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
H _{SYNC}	Single-chip	Horizontal synchronous signal	Input	This is the horizontal synchronizing signal input for CRT display.
	EPROM			This is connected to V _{SS}
V _{SYNC}	Single-chip	Vertical synchronous signal	Input	This is the vertical synchronizing signal input for CRT display
	EPROM			This is connected to V _{SS} .
R, G, B, I, OUT	Single-chip	Video signal	Output	This is a 5-bit output pin for CRT display. The output structure is CMOS output. This is in common with ports P5 ₂ -P5 ₆
	EPROM			These pins are setting to open
P6 ₀ -P6 ₇	Single-chip	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain This port is in common with PWM output pins PWM0-PWM7
	EPROM	Input port P6	Input	All pins are connected to V _{SS}
D-A	Single-chip	D-A output	Output	This is an output pin for 14-bit PWM
	EPROM			This pin is setting to open

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PROM VERSION of M37102M8-XXXSP/FP, M37201M6-XXXSP

EPROM MODE

The M37102E8-XXXSP/FP features an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L") and $\text{CNV}_{\text{SS}}/\text{V}_{\text{PP}}$ signal level is high ("H"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 to 3 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, P3₀, P3₁ and CNV_{SS} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37102E8-XXXSP/FP	M5L27256
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, P1 ₀ -P1 ₆	A ₀ -A ₁₄
Data I/O	Port P2	D ₀ -D ₇
$\overline{\text{CE}}$	P3 ₁	$\overline{\text{CE}}$
$\overline{\text{OE}}$	P3 ₀	$\overline{\text{OE}}$

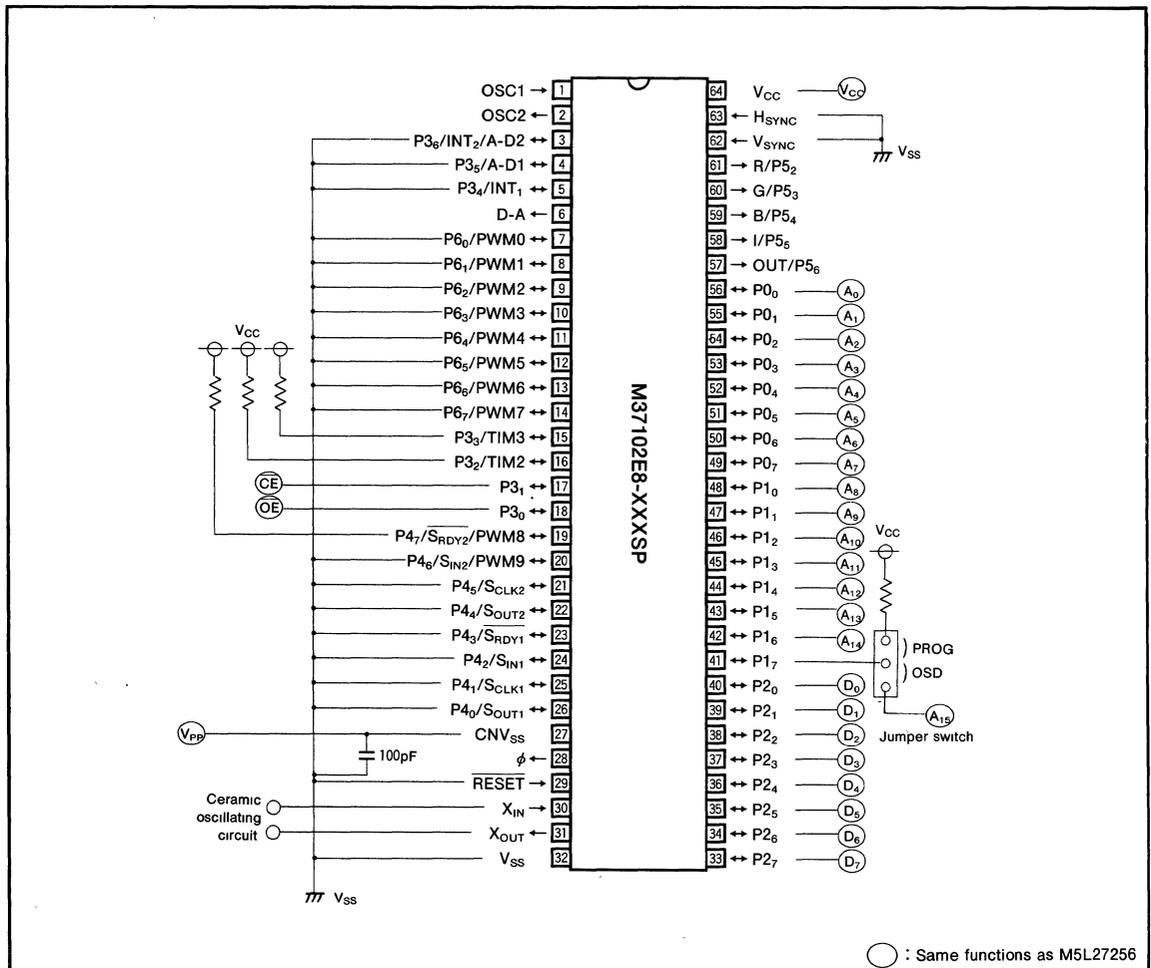


Fig. 1 Pin connection in EPROM mode

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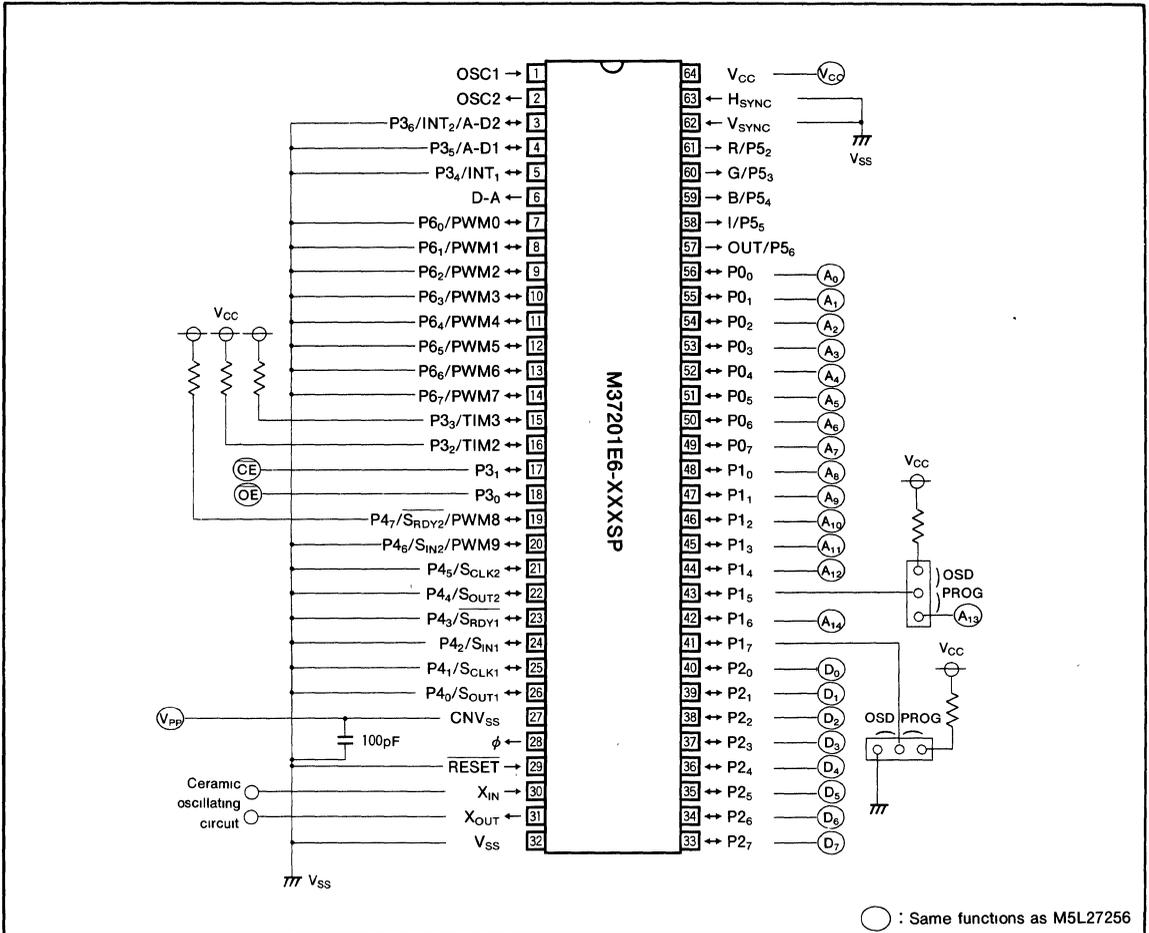
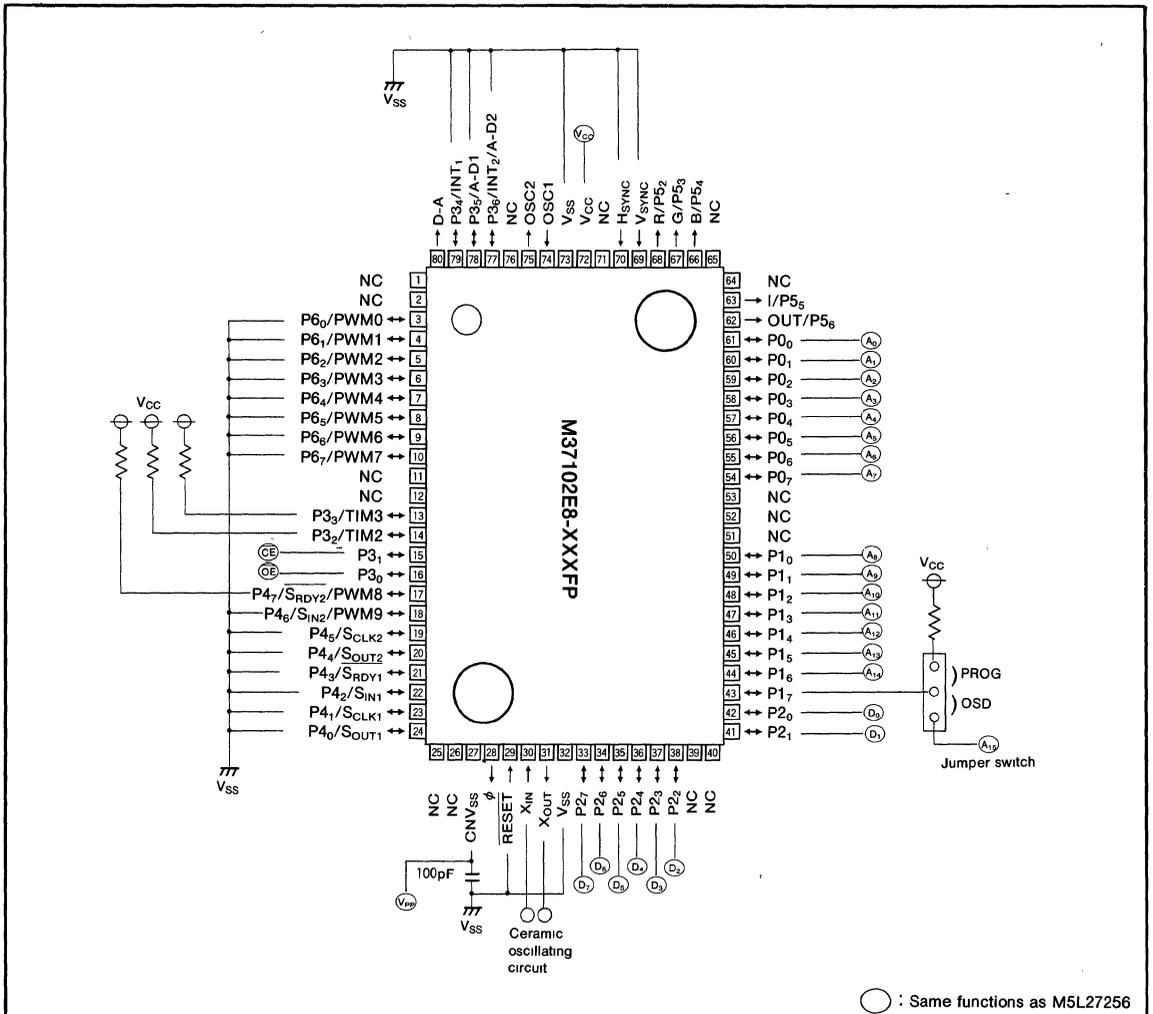


Fig. 2 Pin connection in EPROM mode

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PROM READING, WRITING AND ERASING
Reading

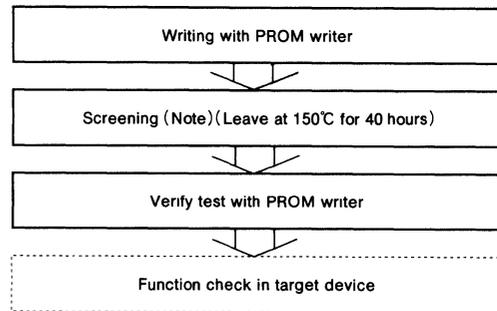
To read the PROM, set the \overline{CE} and \overline{OE} pins to a "L" level, and supply 0V to the \overline{RESET} pin, 5V to the V_{CC} pin and the CNV_{SS} (V_{PP}) pin. Input the address of the data (A_0-A_{14}) to be read and the data will be output to the I/O pins D_0-D_7 . The data I/O pins will be floating when the \overline{OE} pin is in the "H" state.

Writing

To write to the PROM, set the \overline{OE} pin to an "H" level, and supply 0V to the \overline{RESET} pin, 6V to the V_{CC} pin and 12.5V to the V_{PP} pin. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0-A_{14} , and the data to be written is input to pins D_0-D_7 . Set the \overline{CE} pin to a "L" level to begin writing.

NOTES ON HANDLING

- (1) Since a high voltage is used to write data, care should be taken when turning on the PROM writer's power.
- (2) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.
- (3) In EPROM mode, address A_{15} is set to "H" automatically.



Note : Since the screening temperature is higher than storage temperature, never expose to 150°C exceeding 100 hours.

Table 2. I/O signal in each mode

Mode	P_{in}	\overline{CE}	\overline{OE}	V_{PP}	V_{CC}	Data I/O
Read-out		V_{IL}	V_{IL}	5V	5V	Output
Output disable		V_{IL}	V_{IH}	5V	5V	Floating
Programming		V_{IL}	V_{IH}	12.5V	6V	Input
Programming verify		V_{IH}	V_{IL}	12.5V	6V	Output
Program disable		V_{IH}	V_{IH}	12.5V	6V	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3 to 6	V
V _I	Input voltage CNV _{SS}		-0.3 to 6	V
V _I	Input voltage P ₀₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₇ , P ₆₀ -P ₆₇ , H _{SYNC} , V _{SYNC} , RESET	With respect to V _{SS} Output transistors are at "off" state	-0.3 to V _{CC} +0.3	V
V _O	Output voltage P ₀₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₅ , R, G, B, I, OUT, D-A, X _{OUT} , OSC2		-0.3 to V _{CC} +0.3	V
V _O	Output voltage P ₄₆ , P ₄₇ , P ₆₀ -P ₆₇		-0.3 to 13	V
I _{OH}	Circuit current R, G, B, I, OUT, P ₀₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₃ , P ₃₀ , P ₃₁ , D-A		0 to 1 (Note 1)	mA
I _{OL1}	Circuit current R, G, B, I, OUT, P ₀₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₃ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₃ , D-A		0 to 2 (Note 2)	mA
I _{OL2}	Circuit current P ₆₀ -P ₆₇ , P ₄₆ , P ₄₇		0 to 1 (Note 2)	mA
I _{OL3}	Circuit current P ₂₄ -P ₂₇		0 to 10 (Note 3)	mA
I _{OL4}	Circuit current P ₄₄ , P ₄₅		0 to 3 (Note 2)	mA
P _d	Power dissipation	T _a =25°C	550	mW
T _{opr}	Operating temperature		-10 to 70	°C
T _{stg}	Storage temperature		-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=-10 to 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage (Note 4) During the CRT operation	4.5	5.0	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	"H" input voltage P ₀₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₃ , P ₄₆ , P ₄₇ , P ₆₀ -P ₆₇ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₄₄ , P ₄₅	0.7V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ , P ₃₁ , P ₃₅ , P ₄₀ , P ₄₃ -P ₄₅ , P ₄₇	0		0.4V _{CC}	V
V _{IL}	"L" input voltage P ₃₂ -P ₃₄ , P ₃₆ , P ₄₁ , P ₄₂ , P ₄₆ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0		0.2V _{CC}	V
I _{OH}	"H" average output current (Note 1) R, G, B, I, OUT, P ₀₀ -P ₀₇ , P ₁₀ -P ₁₇ , P ₂₀ -P ₂₇ , P ₃₀ , P ₃₁			1	mA
I _{OL1}	"L" average output current (Note 2) R, G, B, I, OUT, P ₀₀ -P ₀₇ , P ₂₀ -P ₂₃ , P ₃₀ -P ₃₆ , P ₄₀ -P ₄₃ , D-A			2	mA
I _{OL2}	"L" average output current (Note 2) P ₆₀ -P ₆₇ , P ₄₆ , P ₄₇			1	mA
I _{OL3}	"L" average output current (Note 3) P ₂₄ -P ₂₇			10	mA
I _{OL4}	"L" average output current (Note 2) P ₄₄ , P ₄₅			3	mA
f _{CPU}	Oscillating frequency (for CRT operation) (Note 5)	3.6	4.0	4.4	MHz
f _{CRT}	Oscillating frequency (for CRT display)	6.0	7.0	8.0	MHz
f _{HS}	Input frequency P ₃₂ -P ₃₄ , P ₃₆ , P ₄₅			100	kHz
f _{HS}	Input frequency P ₄₁			1	MHz

- Note 1 : The total current that flows out of the IC should be 20mA (max.)
 2 : The total of I_{OL1}, I_{OL2} and I_{OL4} should be 30mA (max.)
 3 : The total of I_{OL} of port P₂₄-P₂₇ should be 20mA (max)
 4 : Apply 0.022μF or greater capacitance externally between the V_{CC}-V_{SS} power supply pins so as to reduce power source noise
 Also apply 0.068μF or greater capacitance externally between the V_{CC}-CNV_{SS} pins.
 5 : Use the crystal oscillator or ceramic resonator for CPU oscillation circuit

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ELECTRIC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_A=-10$ to $70^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT OFF		10	20	mA
		$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT ON		20	30	
		At stop mode			300	μA
V_{OH}	"H" output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ , P3 ₁ , R, G, B, I, OUT	$V_{CC}=4.5V$ $I_{OH}=-0.5mA$	2.4			V
V_{OL}	"L" output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₃ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₃ , R, G, B, I, OUT, D-A	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
	"L" output voltage P6 ₀ -P6 ₇ , P4 ₆ , P4 ₇	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	
	"L" output voltage P2 ₄ -P2 ₇	$V_{CC}=4.5V$ $I_{OL}=10.0mA$			3.0	
	"L" output voltage P4 ₄ , P4 ₅	$V_{CC}=4.5V$ $I_{OL}=3mA$			0.4	
$V_{T+}-V_{T-}$	Hysteresis \overline{RESET}	$V_{CC}=5.0V$		0.5	0.7	V
	Hysteresis (Note 1) H _{SYNC} , V _{SYNC} , P3 ₂ -P3 ₄ , P3 ₆ , P4 ₁ , P4 ₂ , P4 ₄ -P4 ₆	$V_{CC}=5.0V$		0.5	1.3	
I_{OZH}	"H" input leak current \overline{RESET} , P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₅	$V_{CC}=5.5V$ $V_O=5.5V$			5	μA
	"H" input leak current P6 ₀ -P6 ₇ , P4 ₆ , P4 ₇	$V_{CC}=5.5V$ $V_O=12V$			10	
I_{OZL}	"L" input leak current \overline{RESET} , P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₆ , P4 ₀ -P4 ₇ , P6 ₀ -P6 ₇	$V_{CC}=5.5V$ $V_O=0V$			5	μA

Note 1. P3₂-P3₄, P3₆ have the hysteresis when these pins are used as interrupt input pins or timer input pins.
P4₁, P4₂, P4₄-P4₆ have the hysteresis when these pins are used as serial I/O ports

SERIES 740

3

MITSUBISHI MICROCOMPUTERS

M37120M6-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DISCRIPTION

The M37120M6-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in an 80-pin plastic molded QFP. This single-chip microcomputer is useful for appliance controllers.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

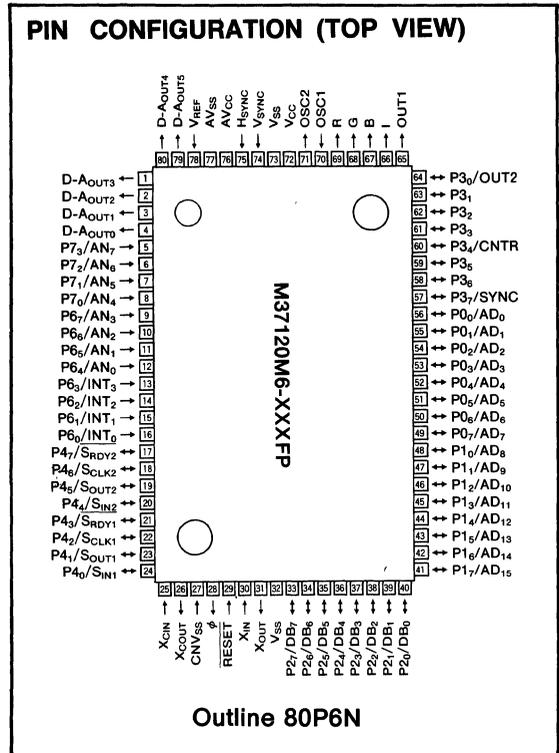
FEATURES

- Number of basic instructions 71
- Memory size
 - ROM 12288 bytes
 - RAM 256 bytes
- Instruction execution time
 - 1 μ s (minimum instructions at 4MHz frequency)
- Single power supply
 - $f(X_{IN})=4\text{MHz}$ 5V \pm 10%
- Power dissipation
 - normal operation mode
 - (at 4MHz frequency) 75mW
- Subroutine nesting 128levels (Max.)
- Interrupt 14types, 14vectors
- 8-bit timer 4
- Programmable I/O ports
 - (Ports P0, P1, P2, P3, P4) 40
- Input ports (Ports P6, P7) 12
- Serial I/O (8-bit) 2
- A-D converter (8-bit resolution) 8channels
- D-A converter (8-bit resolution) 6channels
- Watchdog timer
- 72-character on screen display function
 - Number of character 24 characters \times 3 lines
 - Kinds of character 126
- Two clock generating circuits
 - (One is for main clock, the other is for clock function)

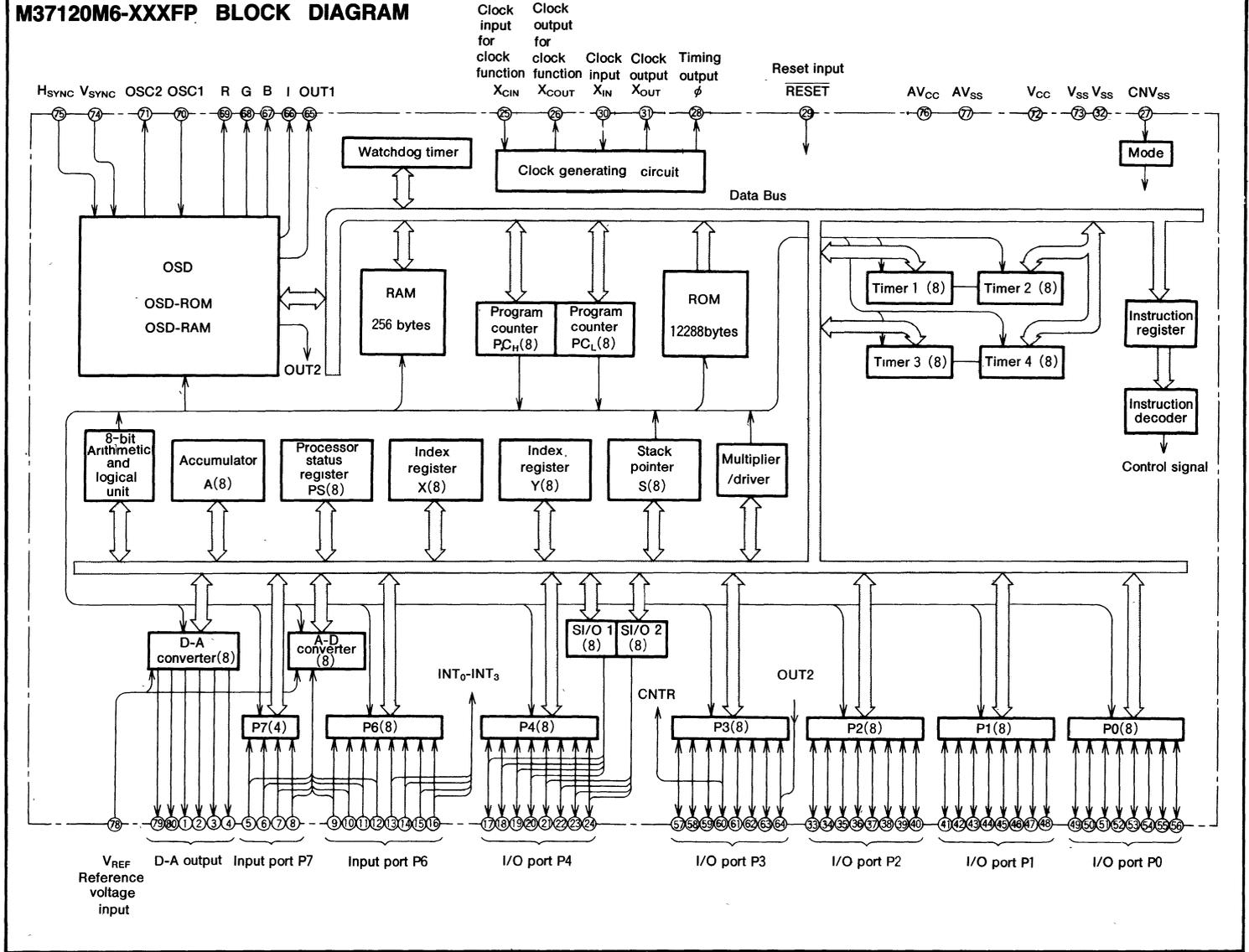
APPLICATION

TV, VCR

PIN CONFIGURATION (TOP VIEW)



M37120M6-XXXXFP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MITSUBISHI MICROCOMPUTERS
M37120M6-XXXXFP

MITSUBISHI MICROCOMPUTERS
M37120M6-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37120M6-XXXFP

Parameter		Functions	
Number of basic instructions		71	
Instruction execution time		1 μ s (minimum instructions, at 4MHz frequency).	
Clock frequency		4MHz	
Memory size	ROM	12288bytes	
	RAM	256bytes	
Input/Output port	P0, P1, P2, P3	I/O	8-bitX4
	P4	I/O	8-bitX1
	P6	Input	8-bitX1
	P7	Input	4-bitX1
	I, B, G, R, OUT1	Output	1-bitX5 (for CRT display function)
	V _{SYNC} , H _{SYNC}	Input	1-bitX2 (for CRT display function)
	D-A _{OUT0} -D-A _{OUT5}	Output	1-bitX6
Serial I/O		8-bitX2	
Timers		8-bit timerX4	
Subroutine nesting		128 (maximum)	
Interrupt		Four external interrupts, nine internal interrupts, one software interrupt	
Clock generating circuit		Two built-in circuits (ceramic or quartz crystal oscillator)	
Supply voltage		5V \pm 10%	
Operating temperature range		-10 to 70°C	
Device structure		CMOS silicon gate	
Package		80-pin plastic molded QFP	
CRT display function	Number of character	24 charactersX3lines	
	Kinds of character	126 (12X16 dots)	

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS}
AV _{CC} , AV _{SS}	Analog power supply		Power supply input for A-D and D-A converters.
CNV _{SS}	CNV _{SS}		This is connect to V _{SS} .
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}	Clock output	Output	
φ	Timing output	Output	The function of this pin can be selected either timing output or resetout output
X _{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function To control generating frequency, an external ceramic or quartz crystal oscillator is connected between the X _{CIN} and X _{COOUT} pins If an external clock is used, the clock source should be connected to the X _{CIN} pin and the X _{COOUT} pin should be left open This clock can be used as a program controlled the system clock
X _{COOUT}	Clock output for clock function	Output	
D-A _{OUT0} -D-A _{OUT5}	D-A output	Output	Analog signal from D-A converter is output
V _{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters
P0 ₀ -P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
P1 ₀ -P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0
P2 ₀ -P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0
P3 ₀ -P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Port P3 ₀ is in common with CRT input pin and P3 ₄ is in common with counter input pin
P4 ₀ -P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same function as port P0, but the output structure is N-channel open drain.
P6 ₀ -P6 ₇	Input port P6	Input	Port P6 is an 8-bit input port P6 ₀ -P6 ₃ are in common with interrupt input pins and P6 ₄ -P6 ₇ are in common with analog input pins
P7 ₀ -P7 ₃	Input port P7	Input	Port P7 is a 4-bit input port and in common with analog input pins
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display To control generating frequency, external condensers and registers are connected
H _{SYNC}	H _{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display.
V _{SYNC}	V _{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display
I, B, G, R, OUT1	CRT output	Output	This is a 5-bit output pin for CRT display

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37120 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Programming Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are provided.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address 00FB₁₆. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

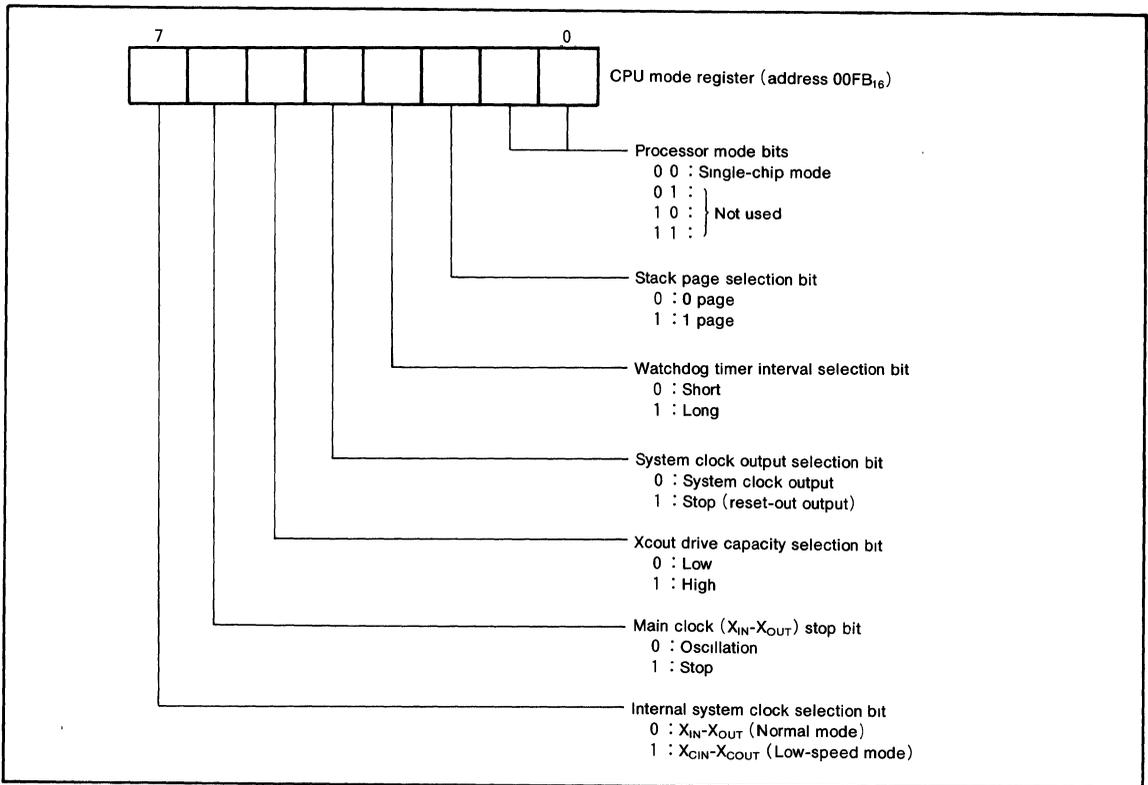


Fig. 1 Structure of CPU mode register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MEMORY

- Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- RAM

RAM is used for data storage as well as a stack area.

- ROM

ROM is used for storing user programs as well as the interrupt vector area.

- RAM for display

RAM for display is used for specifying the character codes and colors to display.

- ROM for display

ROM for display is used for storing character data.

- Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

- Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

- Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

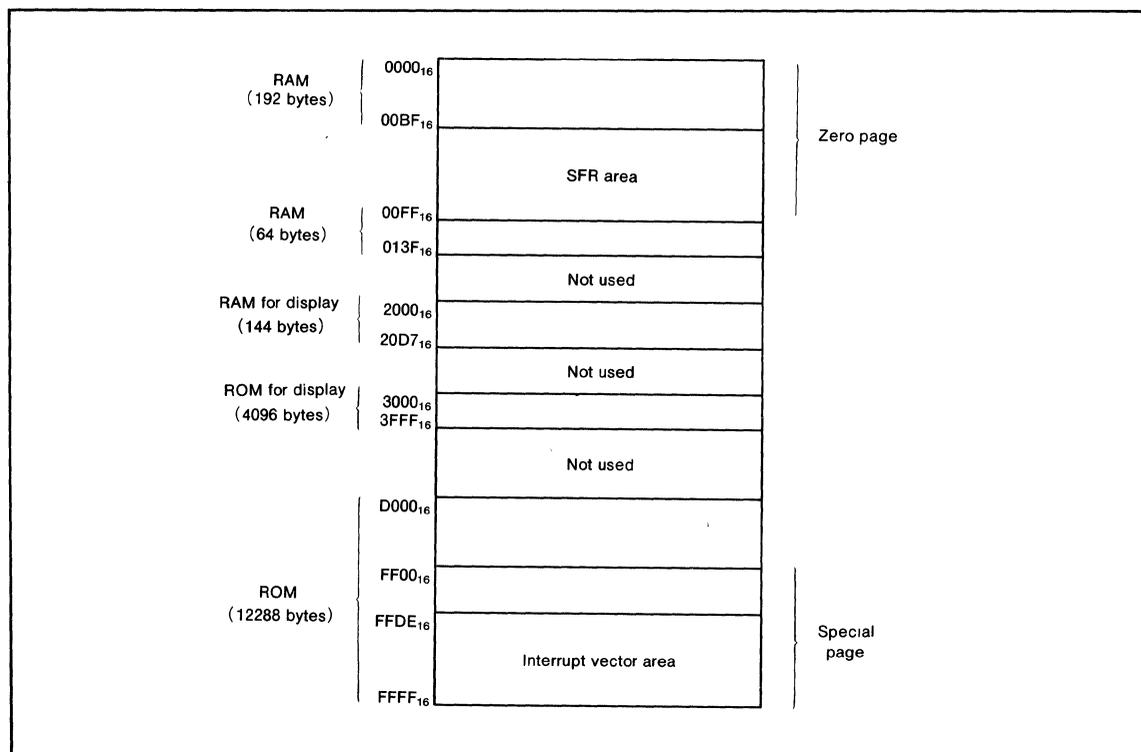


Fig. 2 Memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

00C0 ₁₆	Port P0	00E0 ₁₆	Horizontal position register
00C1 ₁₆	Port P0 directional register	00E1 ₁₆	Vertical position register of block 1
00C2 ₁₆	Port P1	00E2 ₁₆	Vertical position register of block 2
00C3 ₁₆	Port P1 directional register	00E3 ₁₆	Vertical position register of block 3
00C4 ₁₆	Port P2	00E4 ₁₆	Character size register
00C5 ₁₆	Port P2 directional register	00E5 ₁₆	Border selection register
00C6 ₁₆	Port P3	00E6 ₁₆	Color register 0
00C7 ₁₆	Port P3 directional register	00E7 ₁₆	Color register 1
00C8 ₁₆	Port P4	00E8 ₁₆	Color register 2
00C9 ₁₆	Port P4 directional register	00E9 ₁₆	Color register 3
00CA ₁₆	Port P6	00EA ₁₆	CRT control register
00CB ₁₆	Port P7	00EB ₁₆	Display block counter
00CC ₁₆		00EC ₁₆	CRT port control register
00CD ₁₆		00ED ₁₆	
00CE ₁₆		00EE ₁₆	
00CF ₁₆		00EF ₁₆	Watchdog timer
00D0 ₁₆		00F0 ₁₆	Timer 1
00D1 ₁₆		00F1 ₁₆	Timer 2
00D2 ₁₆		00F2 ₁₆	Timer 3
00D3 ₁₆	A-D control register	00F3 ₁₆	Timer 4
00D4 ₁₆	INT edge selection register	00F4 ₁₆	
00D5 ₁₆	A-D conversion result register	00F5 ₁₆	
00D6 ₁₆	D-A conversion register 5	00F6 ₁₆	
00D7 ₁₆	D-A conversion register 4	00F7 ₁₆	
00D8 ₁₆	D-A conversion register 3	00F8 ₁₆	Timer 12 mode register
00D9 ₁₆	D-A conversion register 2	00F9 ₁₆	Timer 34 mode register
00DA ₁₆	D-A conversion register 1	00FA ₁₆	
00DB ₁₆	D-A conversion register 0	00FB ₁₆	CPU mode register
00DC ₁₆	Serial I/O1 mode register	00FC ₁₆	Interrupt request register 1
00DD ₁₆	Serial I/O1 register	00FD ₁₆	Interrupt request register 2
00DE ₁₆	Serial I/O2 mode register	00FE ₁₆	Interrupt control register 1
00DF ₁₆	Serial I/O2 register	00FF ₁₆	Interrupt control register 2

Fig. 3 SFR (Special function register) memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

INTERRUPTS

Interrupts can be caused by 14 different events consisting of four external, nine internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 3 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be clear with a program, but not set. The interrupt enable bit can be set and clear with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
V _{SYNC} interrupt	2	FFFD ₁₆ , FFFC ₁₆	By V _{SYNC} signal of OSD
CRT interrupt	3	FFB ₁₆ , FFA ₁₆	By display completion of character block
INT ₀ interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	External interrupt (polarity programmable)
INT ₁ interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	External interrupt (polarity programmable)
INT ₂ interrupt	6	FFF5 ₁₆ , FFF4 ₁₆	External interrupt (polarity programmable)
INT ₃ interrupt	7	FFF3 ₁₆ , FFF2 ₁₆	External interrupt (polarity programmable)
Timer 1 interrupt	8	FFF1 ₁₆ , FFF0 ₁₆	
Timer 2 interrupt	9	FFEF ₁₆ , FFEE ₁₆	
Timer 3 interrupt	10	FFED ₁₆ , FFEC ₁₆	
Timer 4 interrupt	11	FFEB ₁₆ , FFEA ₁₆	
Serial I/O 1 interrupt	12	FFE9 ₁₆ , FFE8 ₁₆	
Serial I/O 2 interrupt	13	FFE7 ₁₆ , FFE6 ₁₆	
A-D conversion completion interrupt	14	FFE5 ₁₆ , FFE4 ₁₆	
Disable to use.		FFE3 ₁₆ , FFE2 ₁₆	
Disable to use.		FFE1 ₁₆ , FFE0 ₁₆	
BRK instruction interrupt	15	FFDF ₁₆ , FFDE ₁₆	Non-maskable software interrupt

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

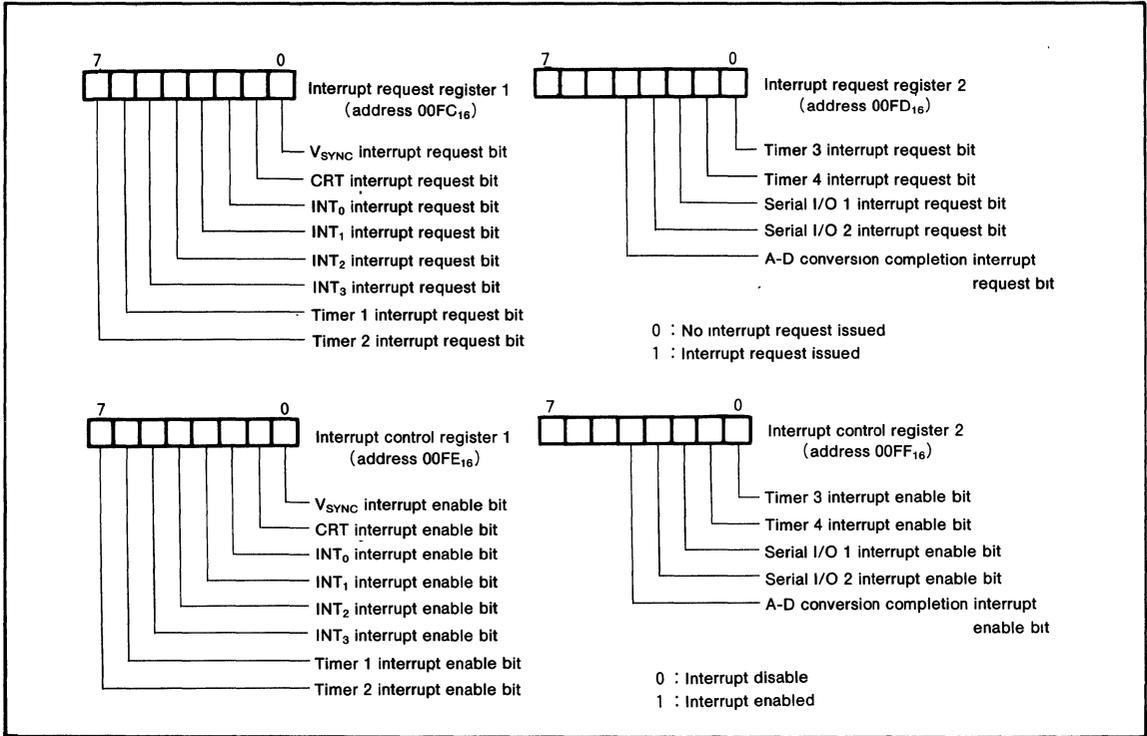


Fig. 4 Structure of registers related with interrupt

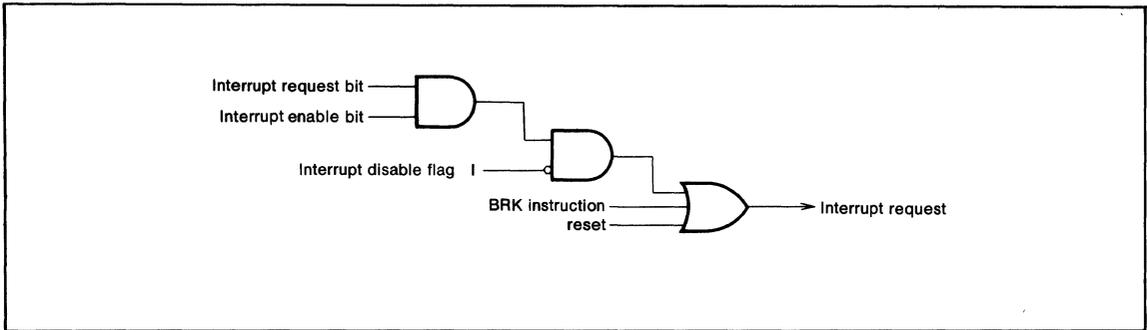


Fig. 5 Interrupt control

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMER

The M37120M6-XXXFP has four timers; timer 1, timer 2, timer 3 and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 6. The count source for timer 1 through 4 can be selected by using bit 0, 1, 4 of the timer 12 mode register (address 00F8₁₆) and bit 0, 1 of the timer 34 mode register (address 00F9₁₆), as shown in Figure 7.

All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is 1/(n + 1), where n is the contents of timer latch.

Also all of the timers have interrupt generating functions. The timer interrupt request bit is set at the next count pulse after the timer reaches "0" (see interrupt section).

The starting and stopping of timers are controlled by bit 2, 3 of the timer 12 mode register and the timer 34 mode register. If the corresponding bit is "0", the timer starts counting, and the corresponding bit is "1", the timer stops.

At a reset or stop mode, FF₁₆ is automatically set in timer 3 and 07₁₆ in timer 4. And timer 4, timer 3 and the clock (ϕ divided by 8) are connected in series. Reset or stop mode is cleared by timer 4 overflow.

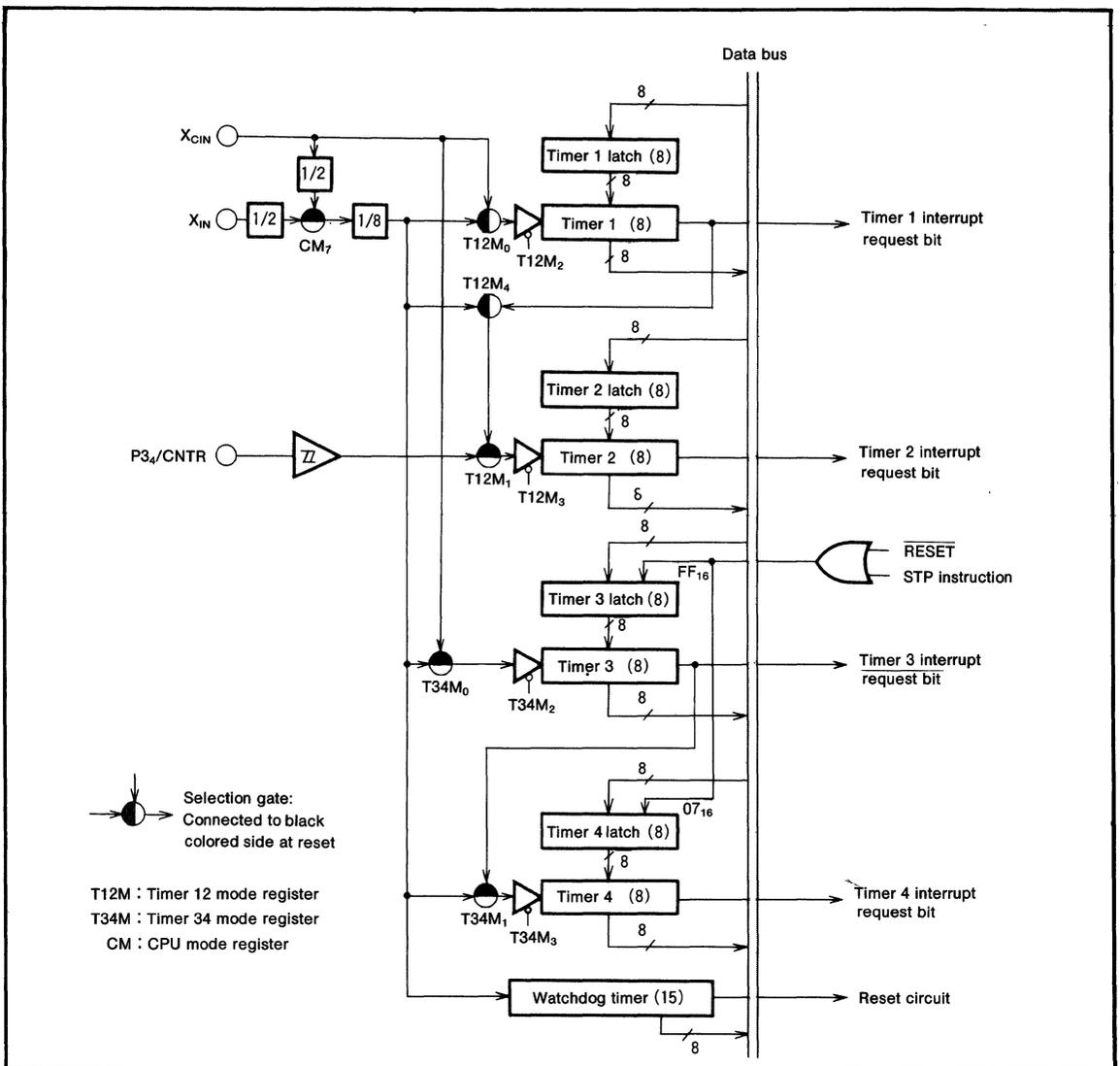


Fig. 6 Block diagram of timer 1 through 4

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

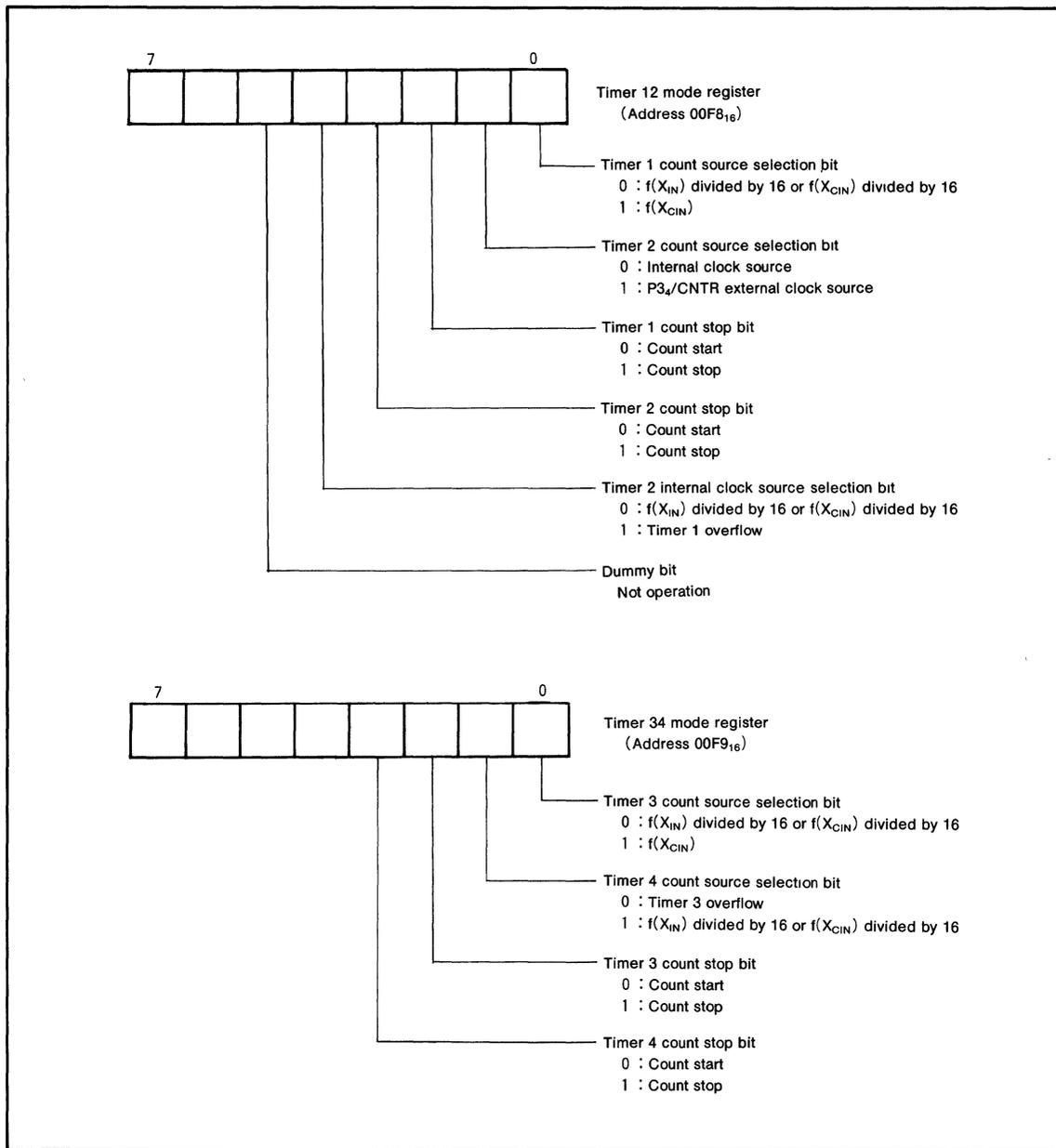


Fig. 7 Structure of timer mode registers

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

SERIAL I/O

M37120 has two serial I/Os which can operate in clock synchronous (Serial I/O 1, Serial I/O 2). Serial I/O 1 and 2 have the same function.

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (S_{CLK}), and the serial I/O (S_{OUT} , S_{IN}), pins are used as port P4.

The serial I/O mode register 1 and 2 (addresses 00DC₁₆ and 00DE₁₆) are 8-bit registers. But the bits 7 and 6 are not used. Bit 0, 1, 2 of these registers are used to select a syn-

chronous clock source. Bits 3 and 4 decide whether P4 will be used as a serial I/O or not. When bit 3 is "1", P4₂, P4₆ become I/O pins of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P4₂, P4₆. If the external synchronous clock is selected, the clock is input to P4₂, P4₆. And P4₁, P4₅ will be a serial output, and P4₀, P4₄ will be a serial input. To use P4₀, P4₄ as serial input, set the directional register bit which correspond to P4₀, P4₄, to "0". For more information on the directional register, refer to the I/O pin section.

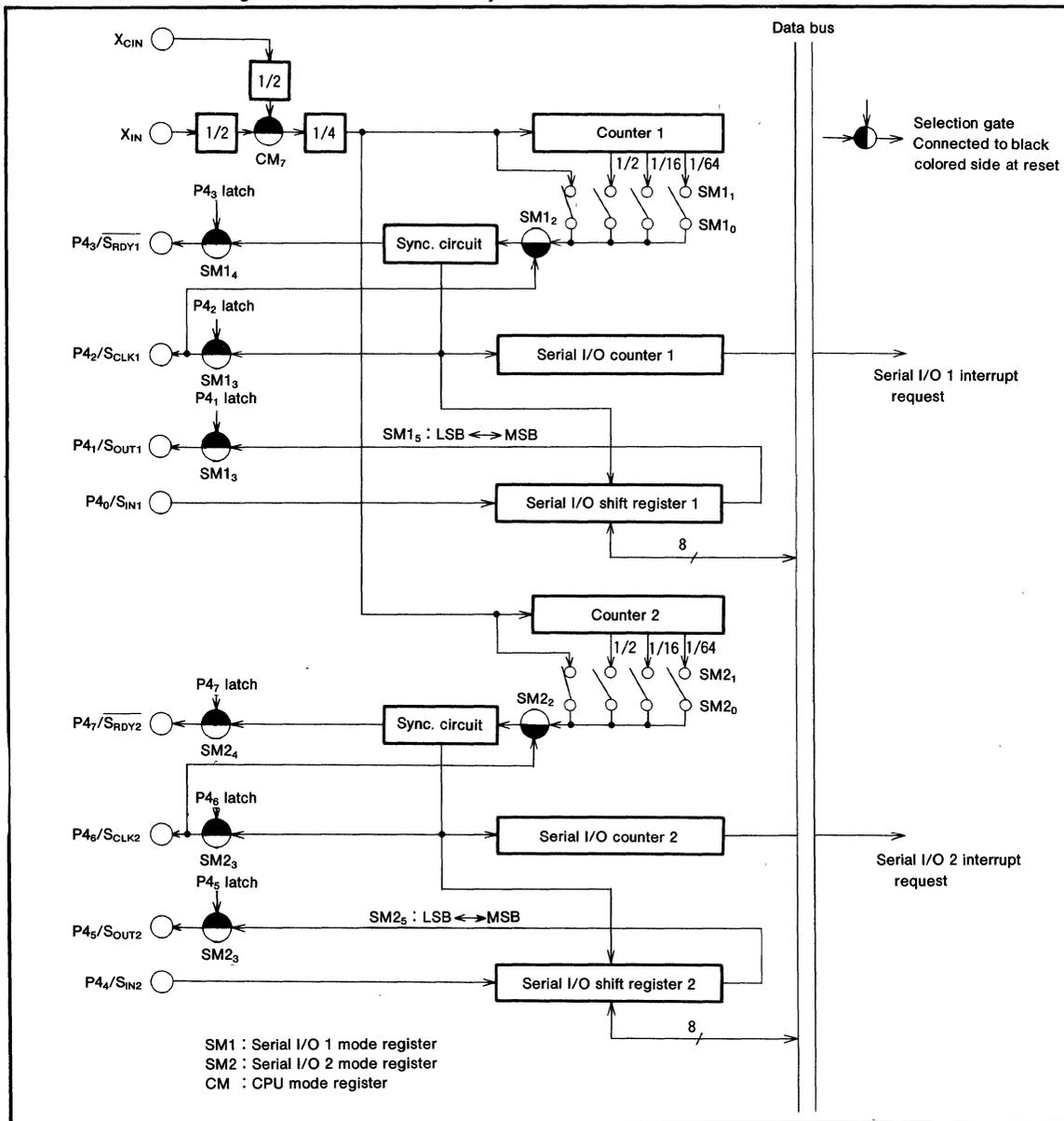


Fig. 8 Block diagram of serial I/O

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

To use the serial I/O, bit 3 of serial I/O mode register 1 and 2 needs to be set to "1", if it is "0" P4₂, P4₆ will function as a normal I/O. Bit 4 determines if P4₃, P4₇ are used as output pins for the receive data ready signal (bit 4 = "1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 4 = "0"). Bit 5 is transfer direction selection bit. M37120 can be changed transfer direction by using this bit.

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock- The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37120M6-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O

register. At each falling edge of the transfer clock, serial data is output to P4₁, P4₅. During the rising edge of this clock, data can be input from P4₀, P4₄ and the data in the serial I/O register will be shifted 1 bit. After the transfer clock has counted 8 times, the serial I/O counter will be "0" and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock- If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9.

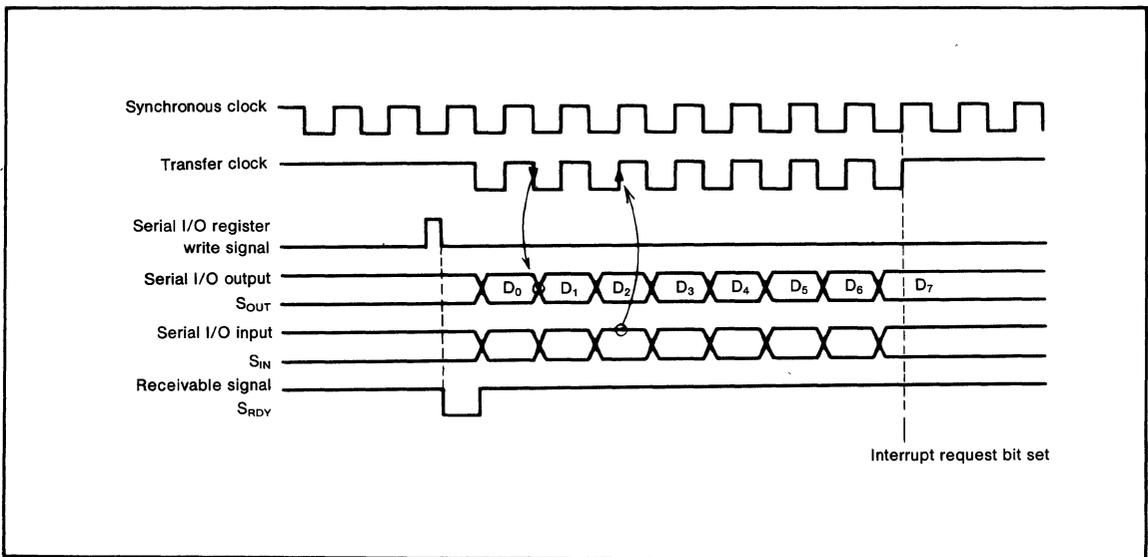


Fig. 9 Serial I/O timing

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

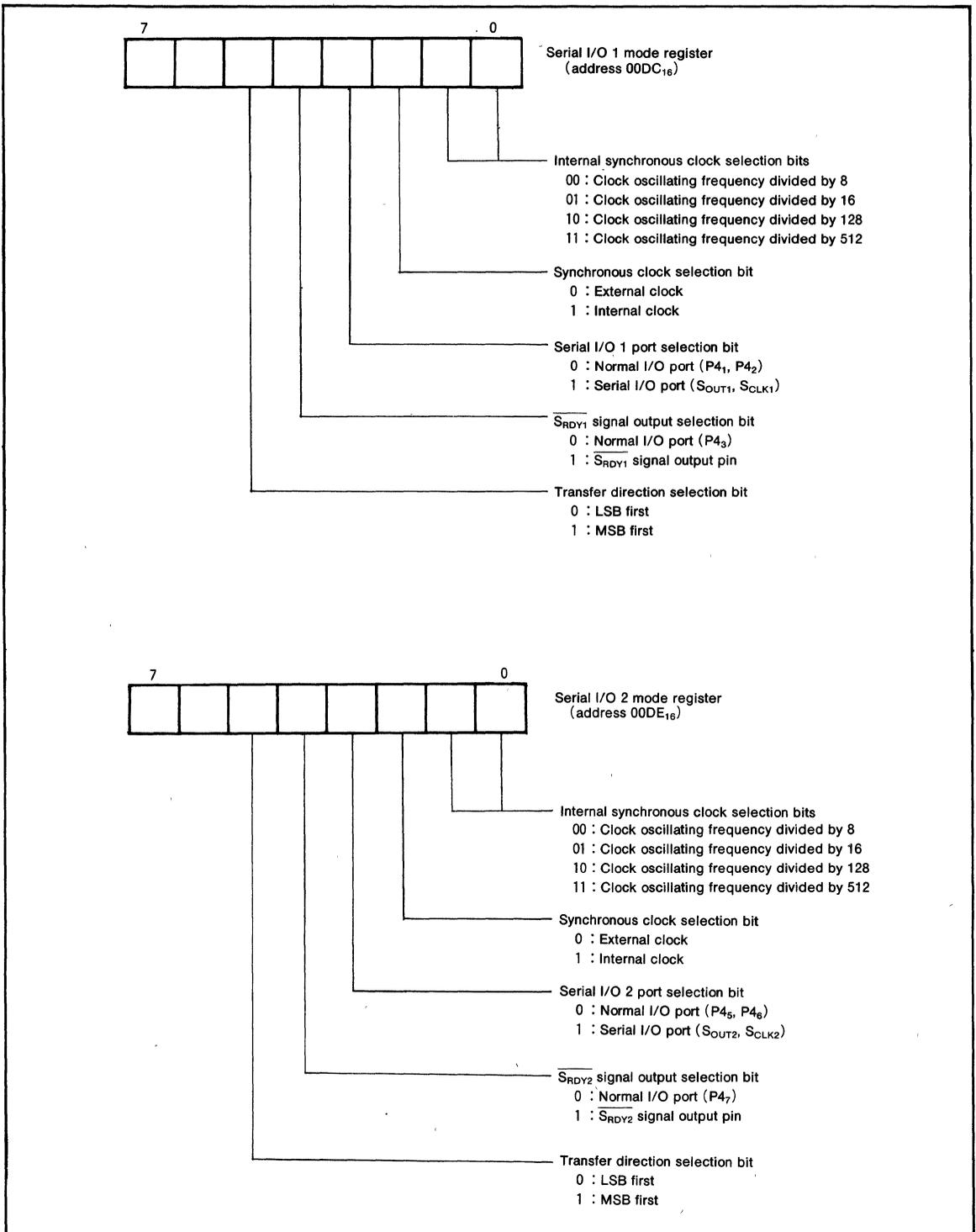


Fig. 10 Structure of serial I/O mode registers

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

A-D CONVERTER

The A-D converter circuit is shown in Figure 12. The analog input ports of the A-D converter (AN_0 - AN_7) are in common with in port $P6_4$ - $P6_7$, $P7_0$ - $P7_3$.

The A-D control register is located at address $00D3_{16}$. One of the eight analog inputs is selected by bits 0, 1 and 2 of this register. The AN pins, not to use as analog input, uses as normal I/O ports.

Bit 0, 1 and 2, and corresponding to analog input pin is shown in Figure 11. A-D conversion is accomplished by first selecting bit 0, 1 and 2 of the A-D control register for the analog input pin.

A-D conversion starts by setting "0" to bit 3 of the A-D control register. When A-D conversion is finished, an interrupt is generated. After A-D interrupt is accepted, the result of A-D conversion can be read from the A-D register.

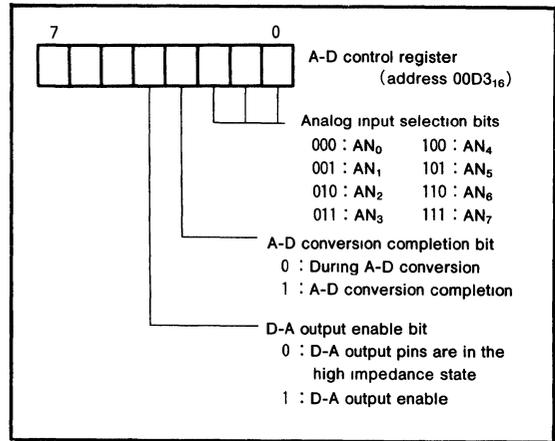


Fig. 11 Structure of A-D control register

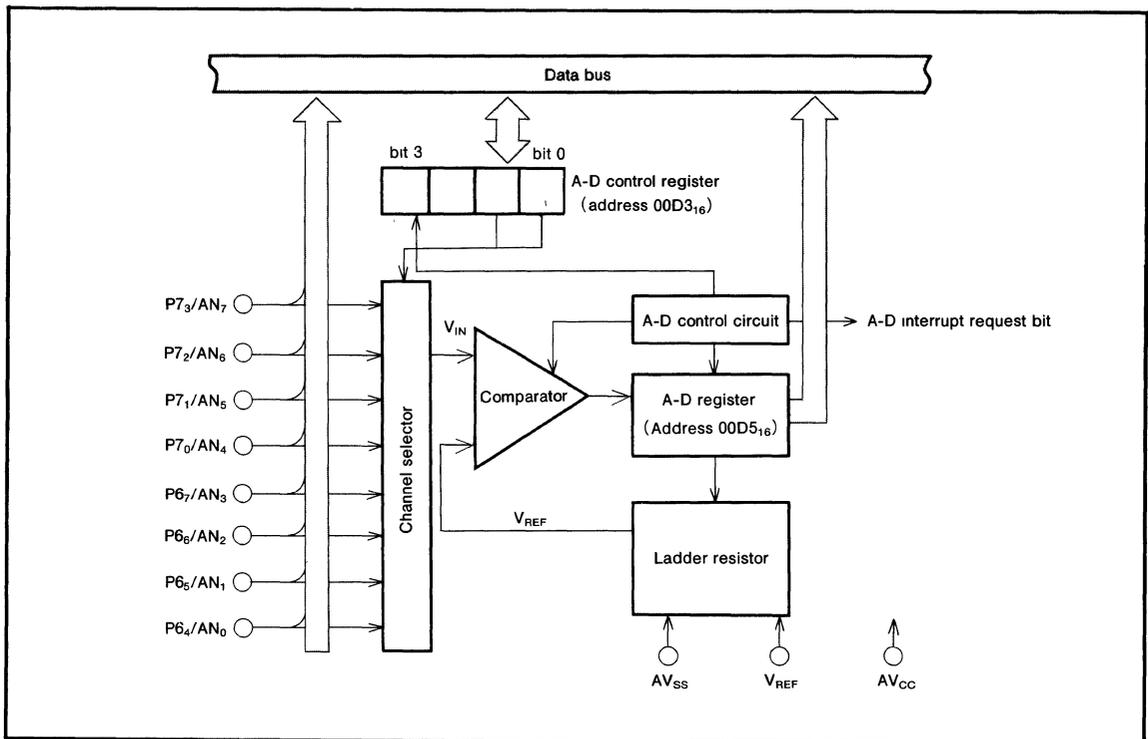


Fig. 12 A-D converter circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

D-A CONVERTER

Six 8-bit resolution D-A converter channels are provided.

Figure 13 shows a block diagram of the D-A converter.

D-A conversion is performed by setting a value in the D-A conversion register (addresses 00D6₁₆ to 00DB₁₆). The result of D-A conversion is output from the D-A output pin.

The output analog voltage V_{DA} is determined by the value n (decimal) set in the D-A conversion register as follows:

$$V_{DA} = V_{REF} \times n / 256 \quad (n = 0 \text{ to } 255)$$

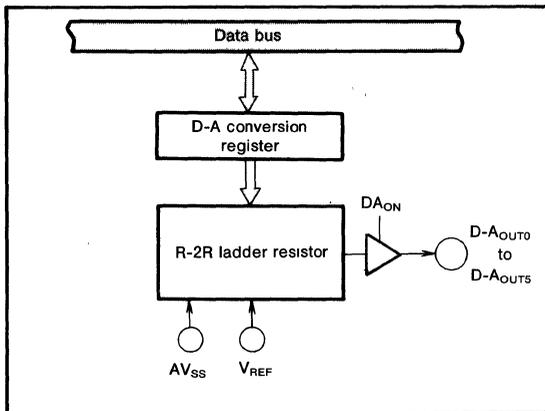


Fig. 13 D-A converter block diagram

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 2 outlines the CRT display functions. The M37120M6-XXXFP incorporates a 24 columns \times 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 126 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12 \times 16 dot configuration to obtain smooth character patterns. (See Figure 14)

The following shows the procedure how to display characters on the CRT screen.

- ① Set the character to be displayed in display RAM.
- ② Set the display color by using the color register.
- ③ Specify the color register in which the display color is set by using the display RAM.
- ④ Specify the vertical position and character size by using the vertical position register and the character size register.
- ⑤ Specify the horizontal position by using the horizontal position register.
- ⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 3 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 15 shows a block diagram of the CRT display control circuit. Figure 16 shows the structure of the CRT control register.

Table 2. Outline of CRT display functions

Parameter		Functions
Number of display character		24characters \times 3 lines
Character configuration		12 \times 16 dots (See Figure 14)
Kinds of character		126
character size		4 size selectable
Color	Kinds of color	15(maximum)
	Coloring unit	Character
Display expansion		Possible (multiple lines)

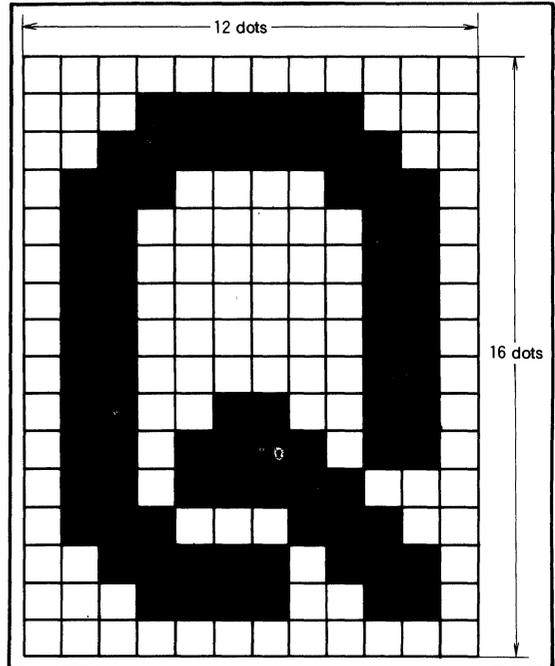


Fig. 14 CRT display character configuration

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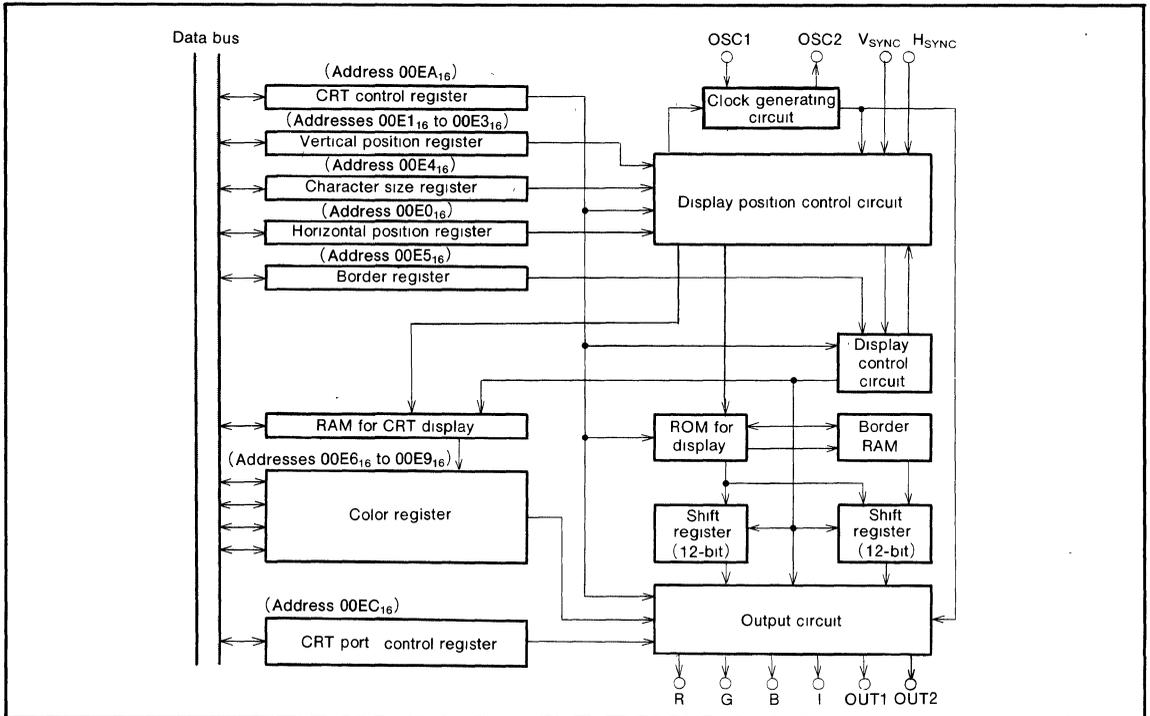


Fig. 15 Block diagram of CRT display control circuit

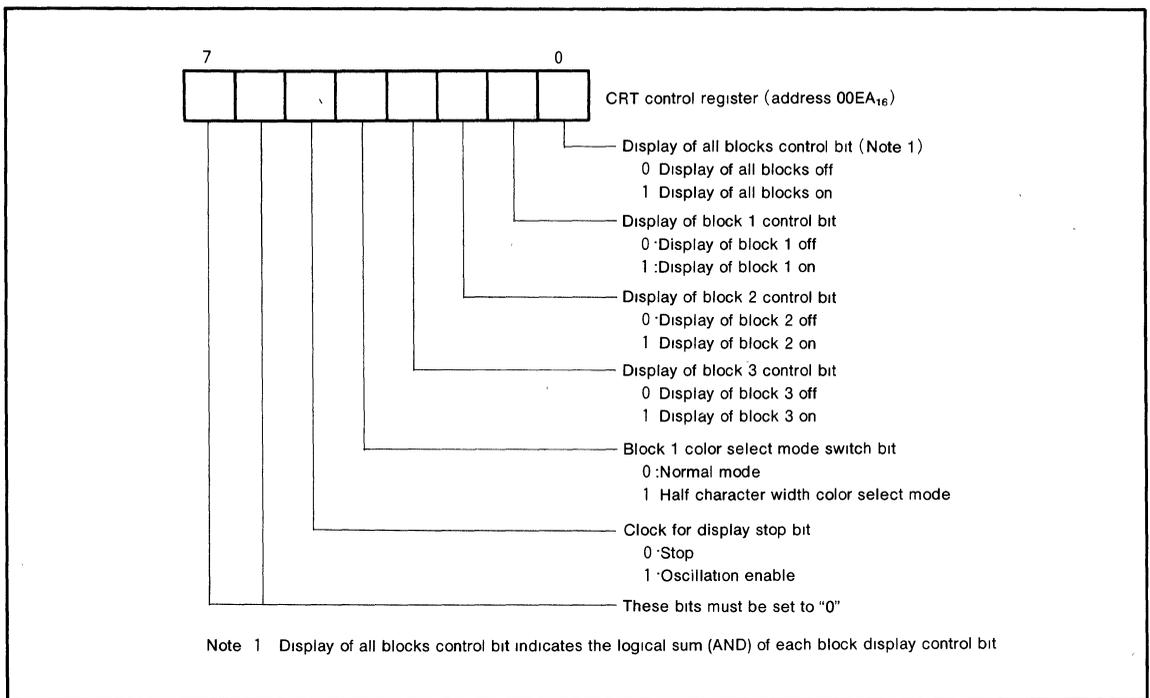


Fig. 16 Structure of CRT control register

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(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 24 characters can be displayed in one block. (See (4) Display Memory.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of $4T_c$ (T_c = oscillation cycle for display).

The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 17), a block of the smaller block No. (1 to 3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 17), the former block is overridden and the latter is displayed.

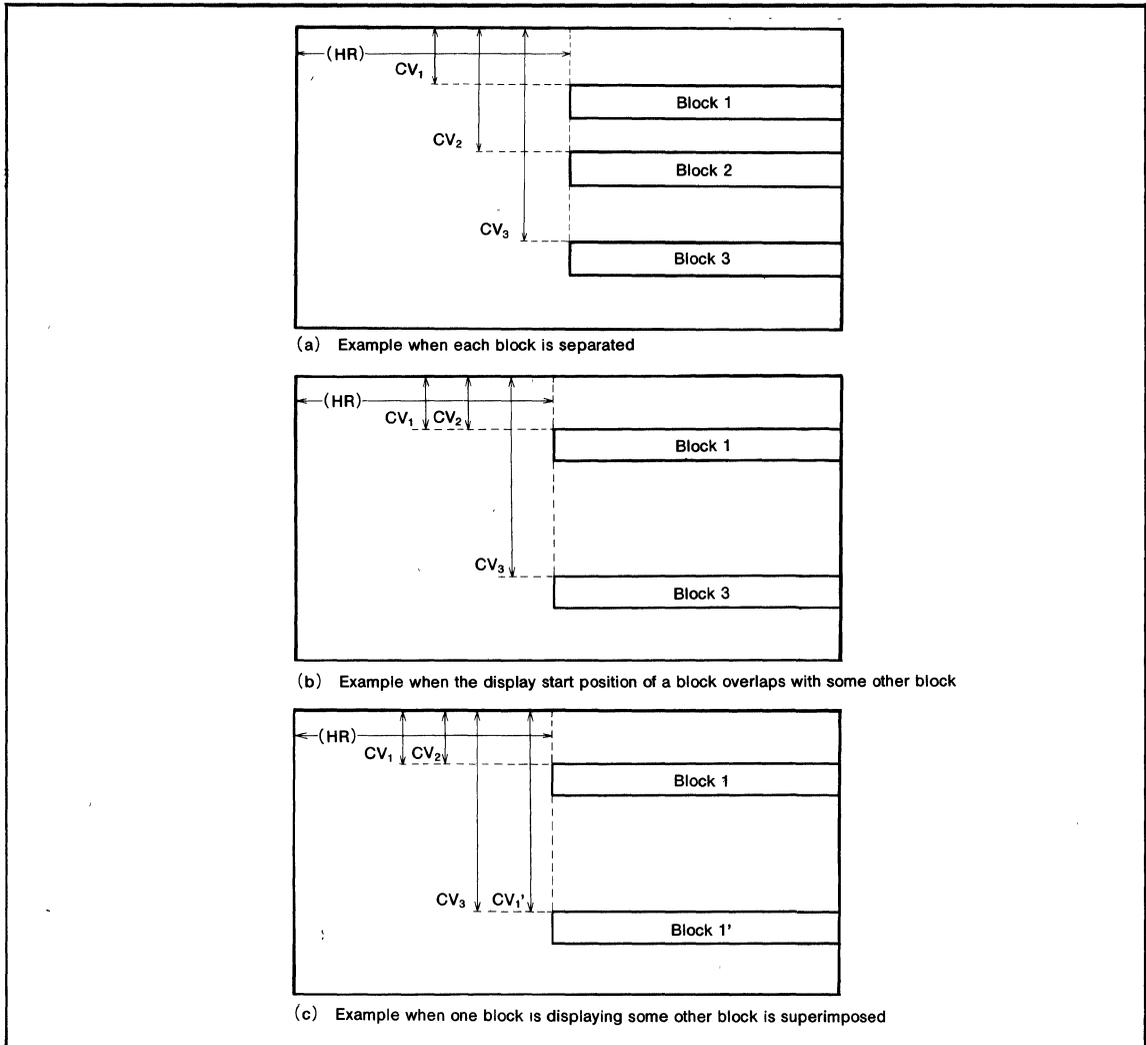


Fig. 17 Display position

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The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values 00_{16} to $7F_{16}$ to bits 0 to 6 in the vertical position register (addresses $00E1_{16}$ to $00E3_{16}$). Figure 18 shows the structure of the vertical position register.

The horizontal direction is common to all blocks, and can be specified from 64-step display positions ($4T_c$ per step (T_c =oscillation cycle for display)) by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the horizontal position register (address $00E0_{16}$). Figure 19 shows the structure of the horizontal position register.

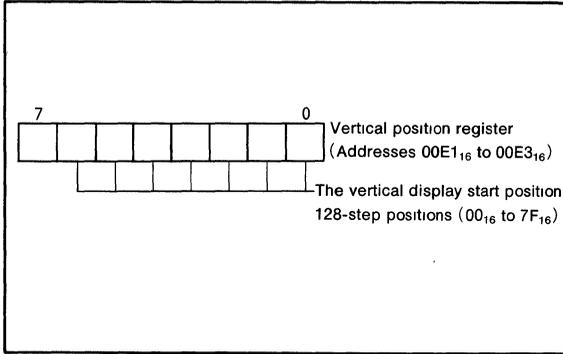


Fig. 18 Structure of vertical position registers

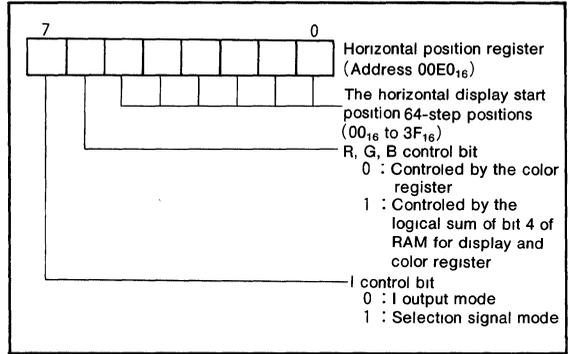


Fig. 19 Structure of horizontal position register

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(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the character size register (address 00E4₁₆) to set a character size.

The character size in block 1 can be specified by using bits 0 and 1 in the character size register; the character size in block 2 can be specified by using bits 2 and 3; the character size in block 3 can be specified by using bits 4 and 5. Figure 20 shows the structure of the character size register.

The character size can be selected from four sizes: small size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation (=T_C) in the width (horizontal) direction.

The small size consists of [one scanning line] × [1 T_C]; the medium size consists of [two scanning lines] × [2 T_C]; the large size consists of [three scanning lines] × [3 T_C]; the extra large size consists of [four scanning lines] × [4 T_C].

Table 3 shows the relationship between the set values in the character size register and the character sizes.

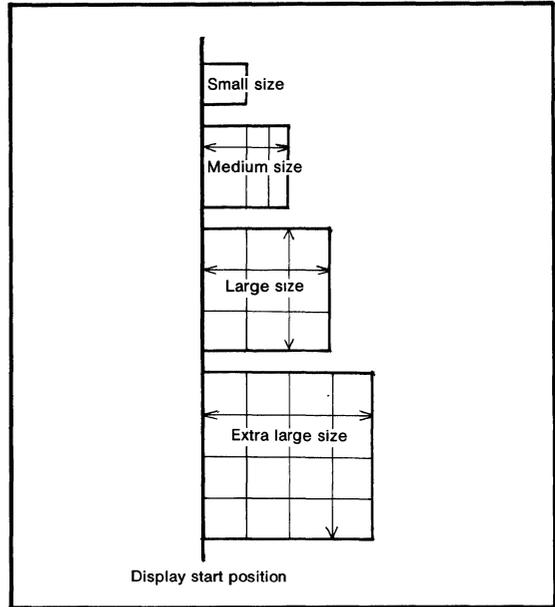


Fig. 21 Display start position of each character size (horizontal direction)

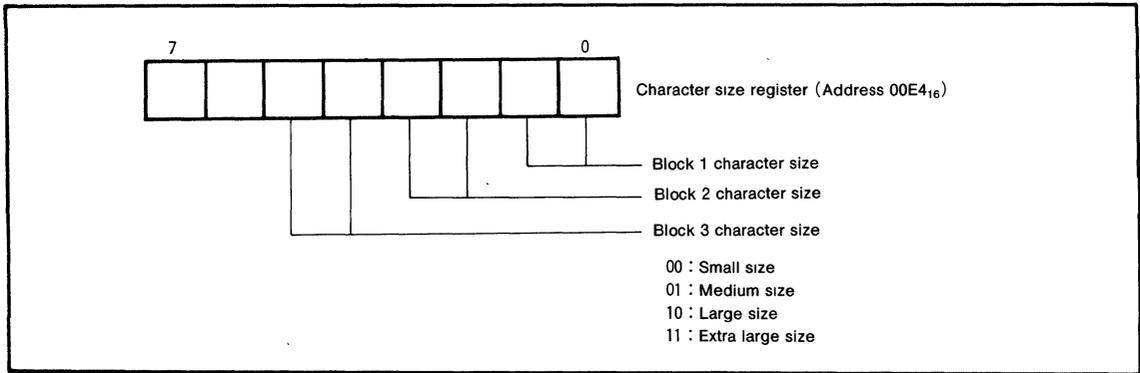


Fig. 20 Structure of character size register

Table 3. The relationship between the set values in the character size register and the character sizes

Set values in the character size register		Character size	Width (horizontal) direction	Height (vertical) direction
CS _{n1}	CS _{n0}			
0	0	Small	1 T _C	1
0	1	Medium	2 T _C	2
1	0	Large	3 T _C	3
1	1	Extra large	4 T _C	4

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal start position is common to all blocks even when the character size varies with each block. (See Figure 21)

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(4) Display Memory

There are two types of display memory : ROM for CRT display (addresses 3000_{16} to $3FFF_{16}$) used to store character dot data (masked) and RAM for CRT display (addresses 2000_{16} to $20D7_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① ROM for CRT display (addresses 3000_{16} to $3FFF_{16}$)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM.

The CRT display ROM has a capacity of 4K bytes. Because 32 bytes are required for one character data, the ROM can contain up to 128 kinds of characters. Actually, however, because two characters are required for test pattern use, the ROM can contain up to 126 kinds of characters for display use.

The CRT display ROM space is broadly divided into two areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses 3000_{16} to $37FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 3800_{16} to $3FFF_{16}$. (See Figure 22) Note however that the four upper bits in the data to be written to addresses 3800_{16} to $3FFF_{16}$ must be set to "1" (by writing data $F0_{16}$ to FF_{16}).

The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.

Assume that data for one character is stored at $3XX0_{16}$ to $3XXF_{16}$ (XX denotes 00_{16} to $7F_{16}$) and $3YY0_{16}$ to $3YYF_{16}$ (YY denotes 80_{16} to FF_{16}), then the character code for it is "XX₁₆."

In other words, character code for any given character is configured with two middle digits of the four-digit (hex- notated) addresses (3000_{16} to $37FF_{16}$) where data for that character is stored.

Table 4 lists the character codes.

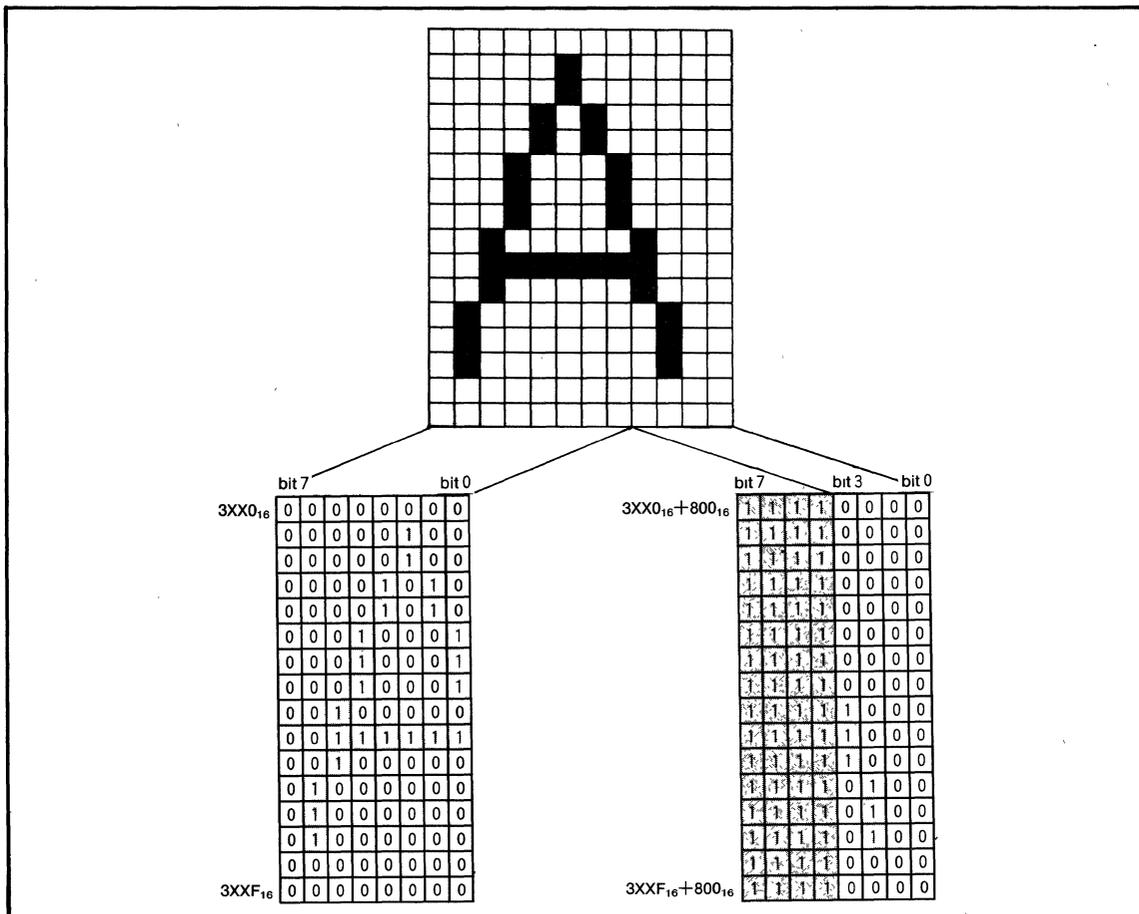


Fig. 22 Contained up form of display character

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Table 4. List of the character code

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00 ₁₆	3000 ₁₆ to 300F ₁₆	3800 ₁₆ to 380F ₁₆
01 ₁₆	3010 ₁₆ to 301F ₁₆	3810 ₁₆ to 381F ₁₆
02 ₁₆	3020 ₁₆ to 302F ₁₆	3820 ₁₆ to 382F ₁₆
03 ₁₆	3030 ₁₆ to 303F ₁₆	3830 ₁₆ to 383F ₁₆
:	:	:
10 ₁₆	3100 ₁₆ to 310F ₁₆	3900 ₁₆ to 390F ₁₆
11 ₁₆	3110 ₁₆ to 311F ₁₆	3910 ₁₆ to 391F ₁₆
:	:	:
4F ₁₆	34F0 ₁₆ to 34FF ₁₆	3CF0 ₁₆ to 3CFF ₁₆
50 ₁₆	3500 ₁₆ to 350F ₁₆	3D00 ₁₆ to 3D0F ₁₆
:	:	:
7D ₁₆	37D0 ₁₆ to 37DF ₁₆	3FD0 ₁₆ to 3FDF ₁₆
7E ₁₆ (Note)	37E0 ₁₆ to 37EF ₁₆	3FE0 ₁₆ to 3FEF ₁₆
7F ₁₆ (Note)	37F0 ₁₆ to 37FF ₁₆	3FF0 ₁₆ to 3FFF ₁₆

Note : The test patterns are contained up in addresses 37E0₁₆ to 37FF₁₆ and 3FE0₁₆ to 3FFF₁₆

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- ② RAM for CRT display (addresses 2000_{16} to $20D7_{16}$)
 The CRT display RAM is allocated at addresses 2000_{16} to $20D7_{16}$, and is divided into a display character code specifying part and display color specifying part for each block. Table 5 shows the contents of the CRT display RAM.
 When a character is to be display at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order

bits (bits 0 to 6) in address 2000_{16} and the color register No. to the two low-order bits (bits 0 and 1) in address 2080_{16} . The color register No. to be written here is one of the four registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 23. Write the character patterns at Table 6 and 7, when M37120M6-XXXFP is mask-ordered.

Table 5. The contents of RAM for CRT display

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st column	2000_{16}	2080_{16}
	2nd column	2001_{16}	2081_{16}
	3rd column	2002_{16}	2082_{16}
	:	:	:
	22th column	2015_{16}	2095_{16}
	23th column	2016_{16}	2096_{16}
	24th column	2017_{16}	2097_{16}
Not used		2018_{16}	2098_{16}
		:	:
		$201F_{16}$	$209F_{16}$
Block 2	1st column	2020_{16}	$20A0_{16}$
	2nd column	2021_{16}	$20A1_{16}$
	3rd column	2022_{16}	$20A2_{16}$
	:	:	:
	22th column	2035_{16}	$20B5_{16}$
	23th column	2036_{16}	$20B6_{16}$
	24th column	2037_{16}	$20B7_{16}$
Not used		2038_{16}	$20B8_{16}$
		:	:
		$203F_{16}$	$20BF_{16}$
Block 3	1st column	2040_{16}	$20C0_{16}$
	2nd column	2041_{16}	$20C1_{16}$
	3rd column	2042_{16}	$20C2_{16}$
	:	:	:
	22th column	2055_{16}	$20D5_{16}$
	23th column	2056_{16}	$20D6_{16}$
	24th column	2057_{16}	$20D7_{16}$
Not used		2058_{16}	
		:	
		$207F_{16}$	

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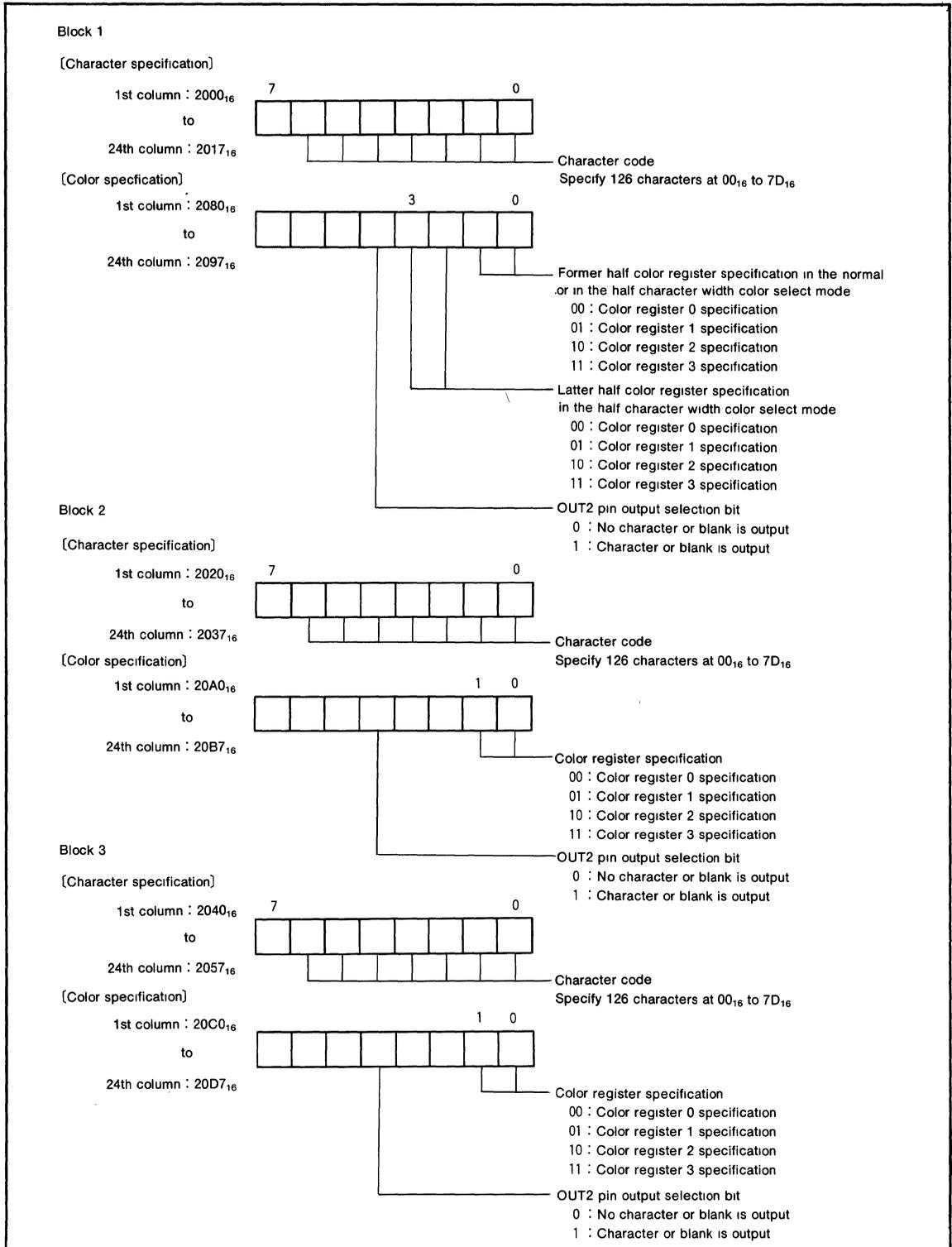


Fig. 23 Structure of RAM for CRT display

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Table 6. Test character pattern 1

Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

Table 7. Test character pattern 2

Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3: addresses 00E6₁₆ to 00E9₁₆) and then specifying that color register with the CRT display RAM.

There are four color outputs : R, G, B, and I. By using a combination of these outputs, it is possible to set 2⁴-1 (when no output) = 15 colors. However, because only four

color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 24 shows the structure of the color registers.

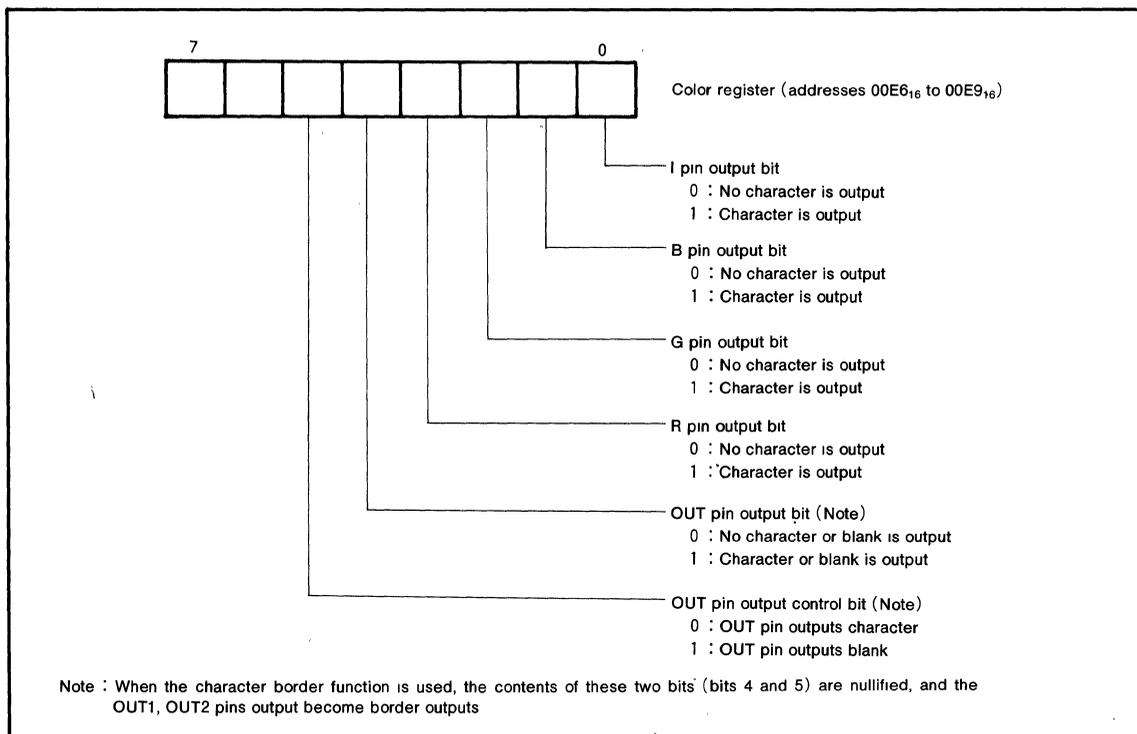


Fig. 24 Structure of color registers

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(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address $00EA_{16}$) it is possible to specify colors in units of a half character size (vertical 16 dots×horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

- ① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080_{16} to 2097_{16}).
- ② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080_{16} to 2097_{16}).

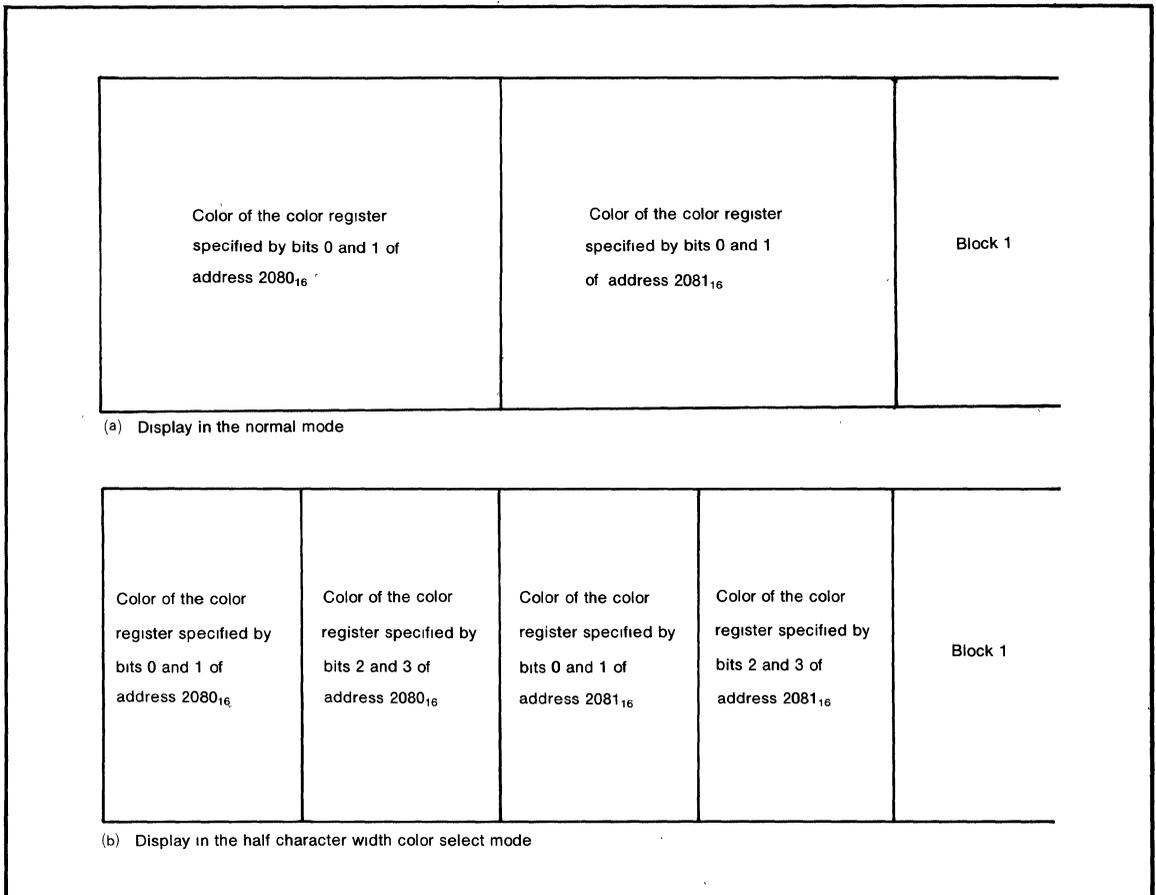


Fig. 25 Difference between normal color select mode and half character width color select mode.

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(7) Multiline Display

The M37120M6-XXXFP can normally display three lines on the CRT screen by displaying three blocks at different horizontal positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (= bit 4 at address 00FE₁₆) to "1"), then execute the following processing in the CRT interrupt handling routine.

- ① Read the value of the display block counter.
- ② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.
- ③ Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and display position (contents of vertical position and horizontal position registers) to be displayed next.

Figure 26 shows the structure of the display block counter.

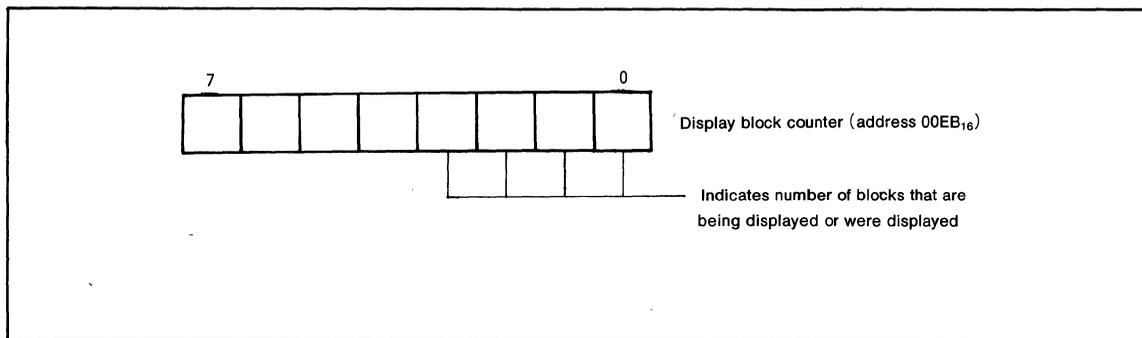


Fig. 26 Structure of display block counter

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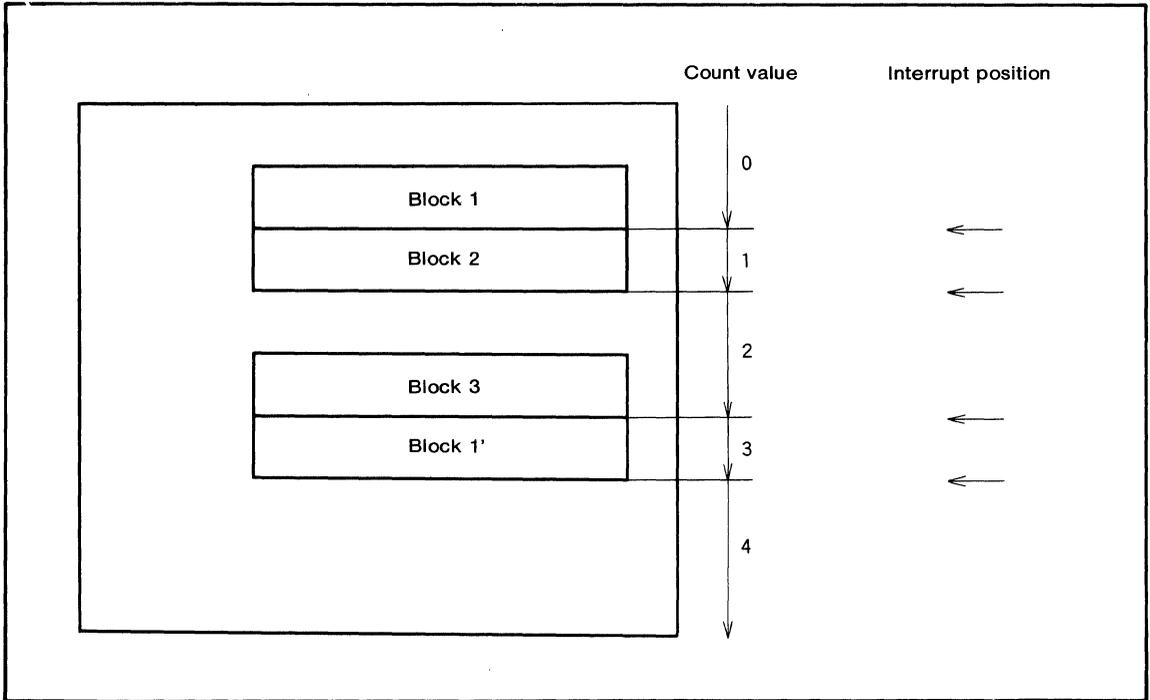


Fig. 27 Timing of CRT interrupt and count value of display block counter

(8) Character Border Function

A border of a one clock (one dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions.

The border is output from the OUT1, OUT2 pins. In this case, bits 4 and 5 in the color registers (contents output from the OUT pins) are nullified, and the border is output from the OUT pins instead.

Border can be specified in units of block by using the border selection register (address 00E5₁₆). Table 8 shows the relationship between the values set in the border selection register and the character border function. Figure 29 shows the structure of the border selection register.

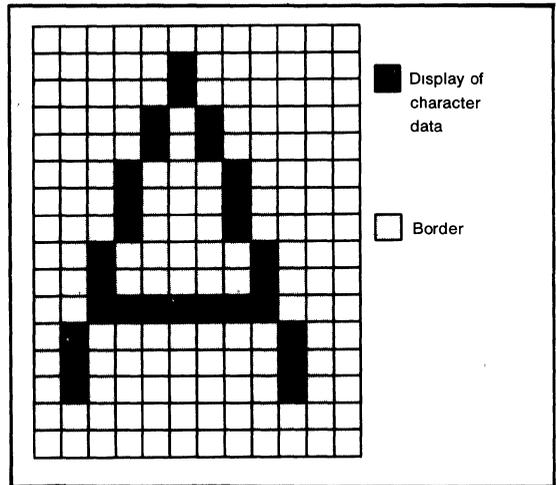
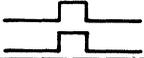
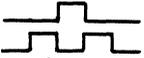


Fig. 28 Example of border

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Table 8. The relationship between the values set in the border selection register and the character border function

Border selection register		Functions	Example of output	
MDn1	MDn0		R, G, B, I output	OUT1, OUT2 output
X	0	Normal		
0	1	Border including character		
1	1	Border not including character		

X : An X indicates either "0" or "1"

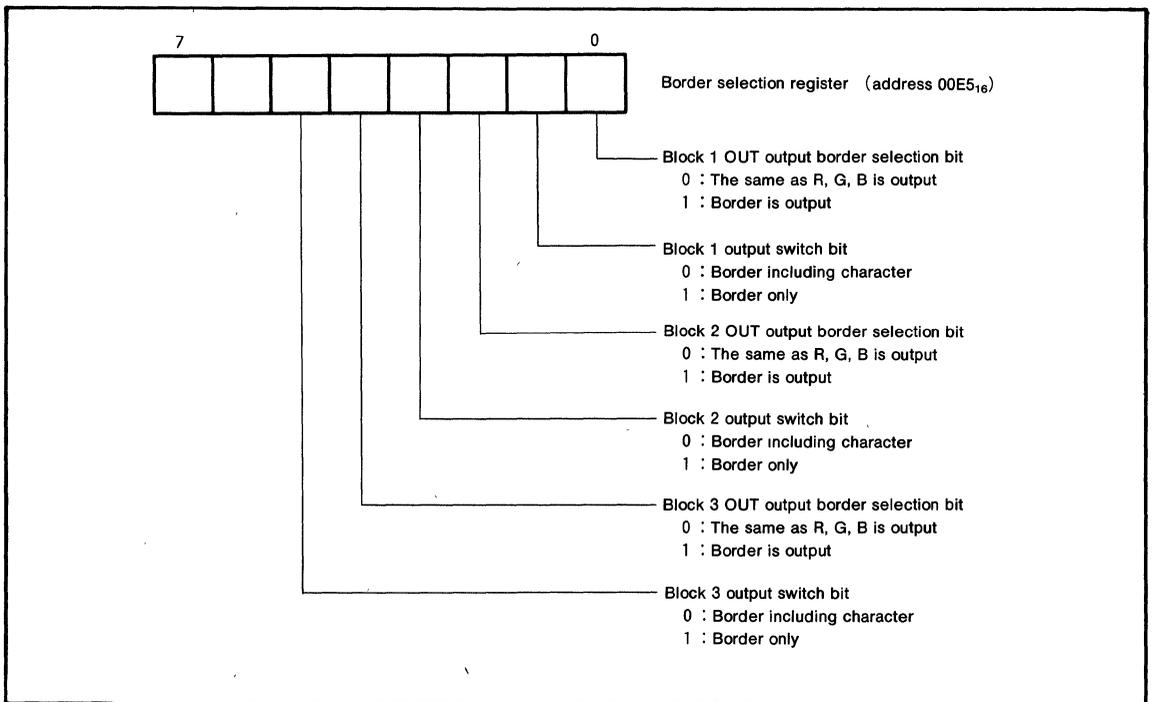


Fig. 29 Structure of border selection register

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(9) CRT Output Pin Control

CRT output pins R, G, B, I, and OUT1 become output enable by setting bit 6 of CRT port control register. OUT2 is in common with port P3₀. This pin become output enable when bit 7 of CRT port control register is set after setting bit 0 of port P3 directional register.

The polarities of CRT outputs (R, G, B, I, and OUT1, as well as H_{SYNC} and V_{SYNC}) can be specified by using the CRT port control register (address 00EC₁₆).

Use bits 0 to 4 in the CRT port control register to set the output polarities of H_{SYNC}, V_{SYNC}, R/G/B, I, and OUT1. When these bits are cleared to "0", a positive polarity is selected; when the bits are set to "1", a negative polarity is selected.

Figure 30 shows the structure of the CRT port control register.

(10) OUT2 Control

Because function selection (such as character or blank output control, border selection, etc.) of OUT1 is the same as that of OUT2, OUT2 outputs the same data of OUT1.

OUT2 can output characters in specified character area by specifying bit 4 of RAM for display. This function is no use when blank output is setting by color register.

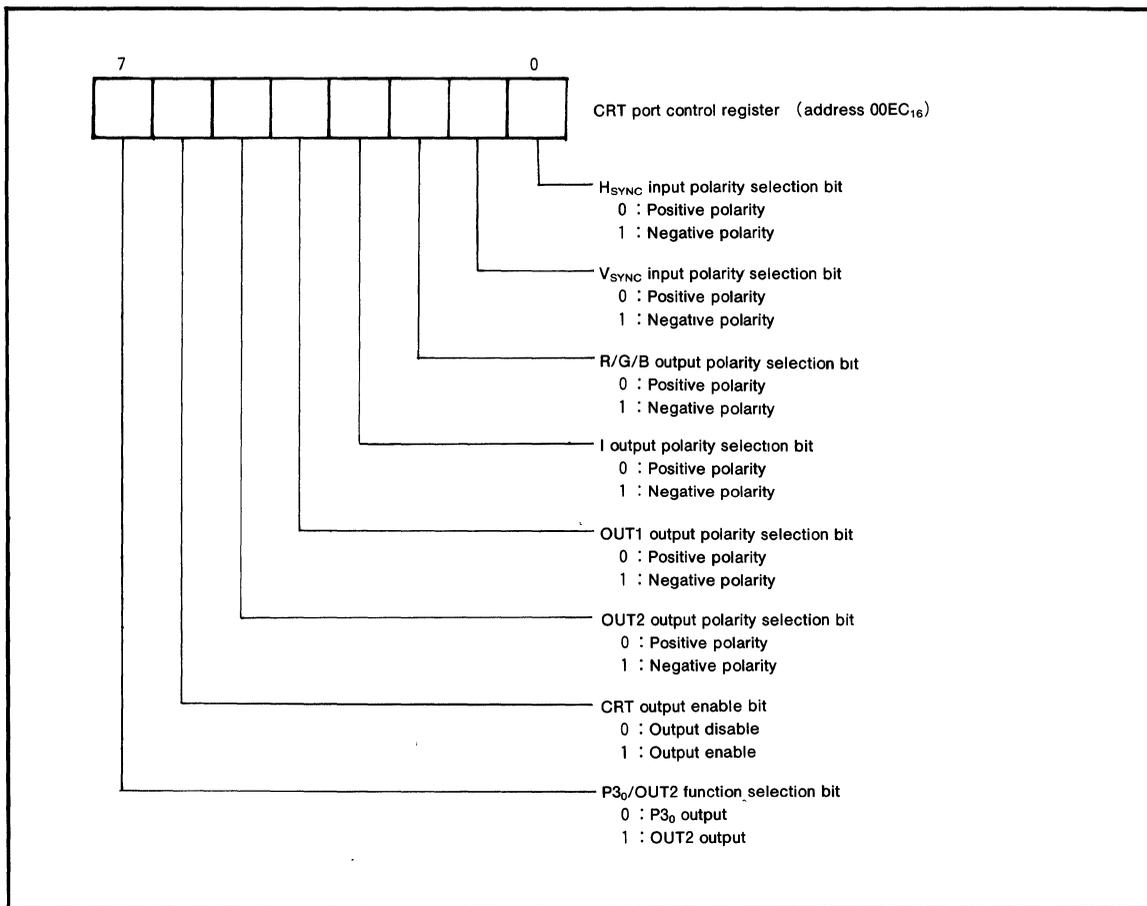


Fig. 30 Structure of CRT port control register

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WATCHDOG TIMER

The watchdog timer provides a method of returning to reset status if a runaway or other cause prevents a program from running a loop normally.

The watchdog timer is a 15-bit counter consisting of a lower seven bits and an upper eight bits (address 00EF₁₆). At reset or after the watchdog timer is written to, 7FFF₁₆ is set in this timer and it starts to count.

When the MSB reaches "0", an internal reset is generated. Therefore programs should normally be written to ensure that the watchdog timer is written to before this bit reaches

"0". If address 00EF₁₆ is read, the value in the upper eight bits of the counter is read. Directly after a reset, the watchdog timer is stopped.

The count source of the lower seven bits is a signal that is the system clock ϕ divided by eight. The count source of the upper eight bits can be selected as either the overflow signal from the 7-bit counter or a signal that is the system clock ϕ divided by eight, depending on the value of bit 3 of the CPU mode register (address 00FB₁₆).

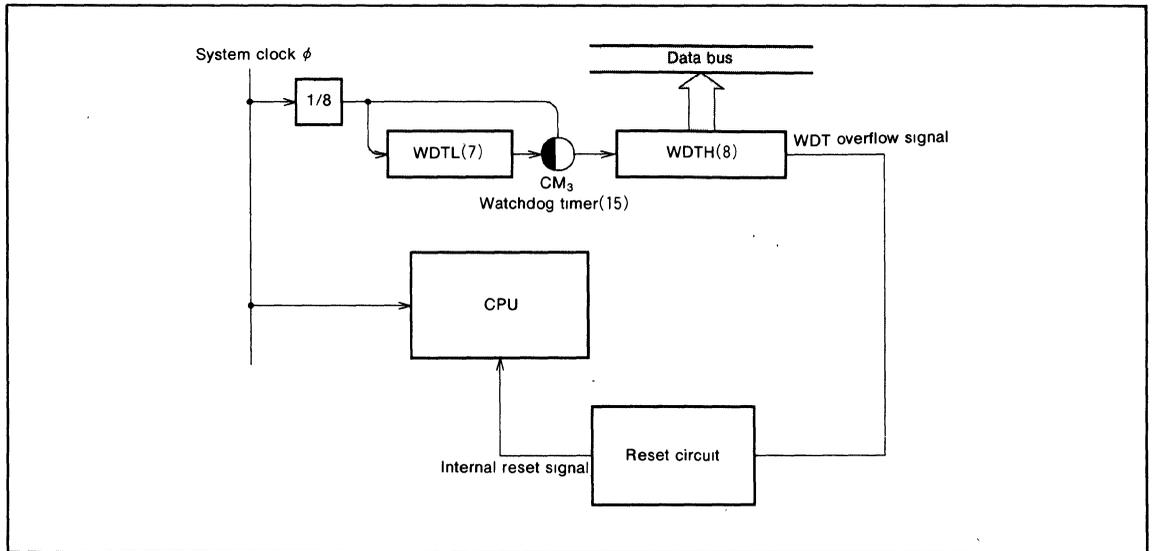


Fig. 31 Block diagram of runaway detection function

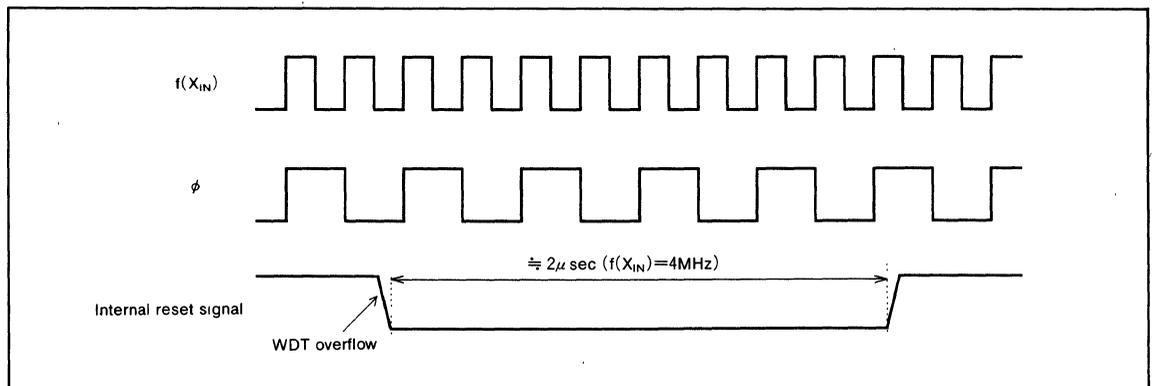


Fig. 32 Timing diagram of internal reset signal

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RESET CIRCUIT

The M37120M6-XXXFP is reset according to the sequence shown in Figure 34. It starts the program from the address formed by using the content of address FFF_{16} as the high order address and the content of the address FFE_{16} as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than $2\mu\text{s}$ while the power voltage is between 4 and 5.5V and the crystal oscillator oscillation is stable and then returned to "H" level.

The internal initializations following reset are shown in Figure 33.

Immediately after reset, the count of X_{IN} is stopped and X_{CIN} divided by 2 is selected as an internal clock. FF_{16} is set timer 3 and 07_{16} is set to timer 4 and timer 3 and timer 4 are connected. Also X_{CIN} divided by 16 is selected as the timer 3 count source. Reset is cleared by timer 4 overflow.

	Address	
(1) Port P 0 directional register	(D 0)(C 1 ₁₆)	0 0 ₁₆
(2) Port P 1 directional register	(D 1)(C 3 ₁₆)	0 0 ₁₆
(3) Port P 2 directional register	(D 2)(C 5 ₁₆)	0 0 ₁₆
(4) Port P 3 directional register	(D 3)(C 7 ₁₆)	0 0 ₁₆
(5) Port P 4 directional register	(D 4)(C 9 ₁₆)	0 0 ₁₆
(6) A-D control register	(D 3 ₁₆)	0 1 0 0 0
(7) INT edge selection register	(D 4 ₁₆)	0 0 0 0
(8) D-A conversion register 5	(D 6 ₁₆)	0 0 ₁₆
(9) D-A conversion register 4	(D 7 ₁₆)	0 0 ₁₆
(10) D-A conversion register 3	(D 8 ₁₆)	0 0 ₁₆
(11) D-A conversion register 2	(D 9 ₁₆)	0 0 ₁₆
(12) D-A conversion register 1	(D A ₁₆)	0 0 ₁₆
(13) D-A conversion register 0	(D B ₁₆)	0 0 ₁₆
(14) Serial I/O 1 mode register	(SM1)(D C ₁₆)	0 0 0 0 0 0
(15) Serial I/O 2 mode register	(SM2)(D E ₁₆)	0 0 0 0 0 0
(16) CRT port control register	(E C ₁₆)	0 0 ₁₆
(17) Display block counter	(E B ₁₆)	0 0 0 0
(18) CRT control register	(E A ₁₆)	0 0 ₁₆
(19) Color register 3	(E 9 ₁₆)	0 0 0 0 0 0
(20) Color register 2	(E 8 ₁₆)	0 0 0 0 0 0
(21) Color register 1	(E 7 ₁₆)	0 0 0 0 0 0
(22) Color register 0	(E 6 ₁₆)	0 0 0 0 0 0
(23) Horizontal position register	(E 0 ₁₆)	0 0 ₁₆
(24) Watchdog timer	(E F ₁₆)	F F ₁₆
(25) Timer 12 mode register	(T12M)(F 8 ₁₆)	0 0 0 0 0 0
(26) Timer 34 modu register	(T34M)(F 9 ₁₆)	0 0 0 0
(27) CPU mode register	(CM)(F B ₁₆)	1 1 1 1 1 1 0 0
(28) Interrupt request register 1	(F C ₁₆)	0 0 ₁₆
(29) Interrupt request register 2	(F D ₁₆)	0 0 0 0 0 0
(30) Interrupt control register 1	(F E ₁₆)	0 0 ₁₆
(31) Interrupt control register 2	(F F ₁₆)	0 0 0 0 0 0
(32) Processor status register		1 1 1 1 1 1
(33) Program counter	(P C _H)	Contents of address FFF ₁₆
	(P C _L)	Contents of address FFE ₁₆

Note : Since the contents of both registers other than those listed above (including timers and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values.

Fig. 33 Internal state of microcomputer at reset

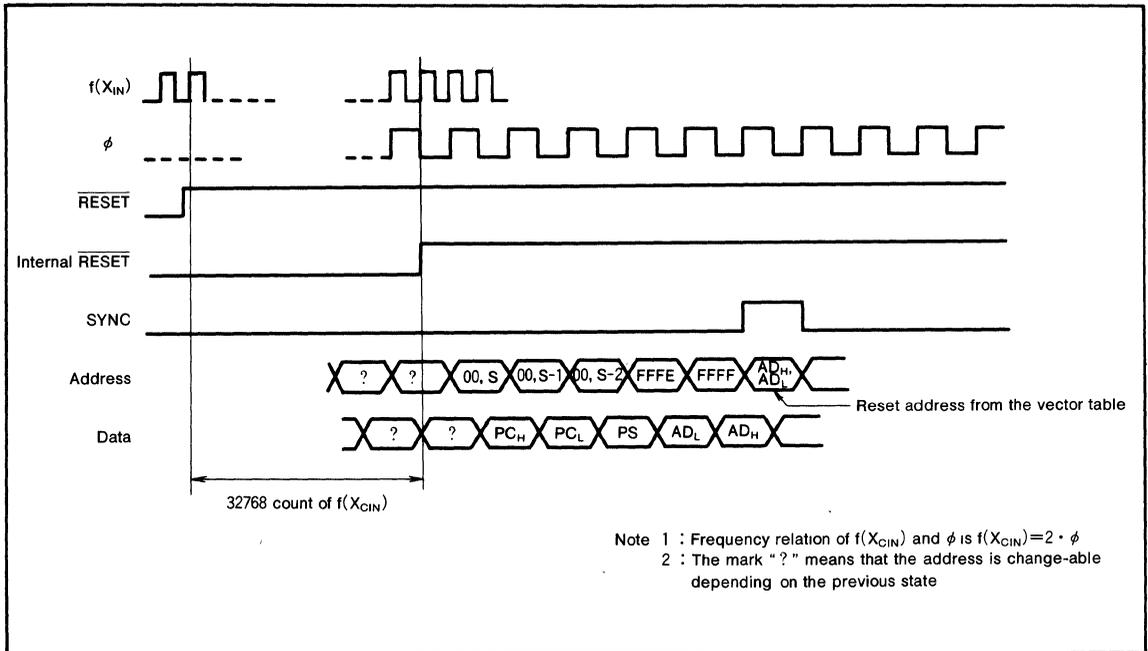


Fig. 34 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 3, P0 can be accessed as memory through zero page address $00C0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00C1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

(2) Port P1

Port P1 has the same function as P0.

(3) Port P2

Port P2 has the same function as P0.

(4) Port P3

Port P3 has the same functions P0 except that part of P3 is common with the CRT output pin and counter input pin.

(5) Port P4

Port P4 has the same function as P0. The output structure is N-channel open drain.

(6) Port P6

Port P6 has the same functions as P0. The lower 4-bit of this port are in common with interrupt input pins and the higher 4-bit of this port are in common with analog input pins.

(7) Port P7

Port P7 is a 4-bit input port. This port is in common with analog input pins.

(8) I/O pins for CRT display function

H_{SYNC} , V_{SYNC} are input pins for deciding the display location. R, G, B, I, OUT1 and OUT2 are output the pattern of CRT display.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

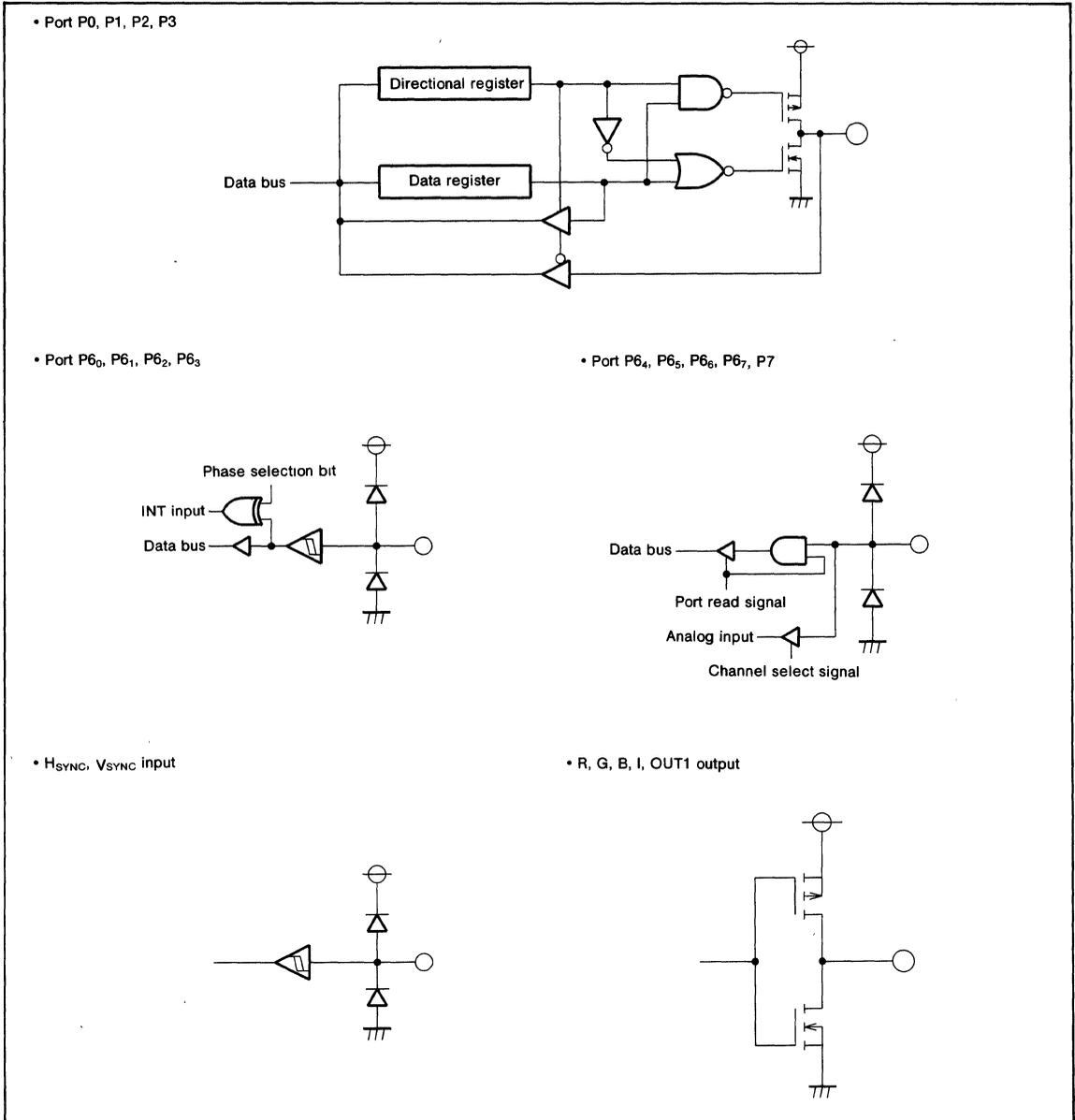


Fig. 35 Block diagram of Ports P0, P1, P2, P3, P6, P7, H_{sync}, V_{sync}, R, G, B, I, OUT1

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

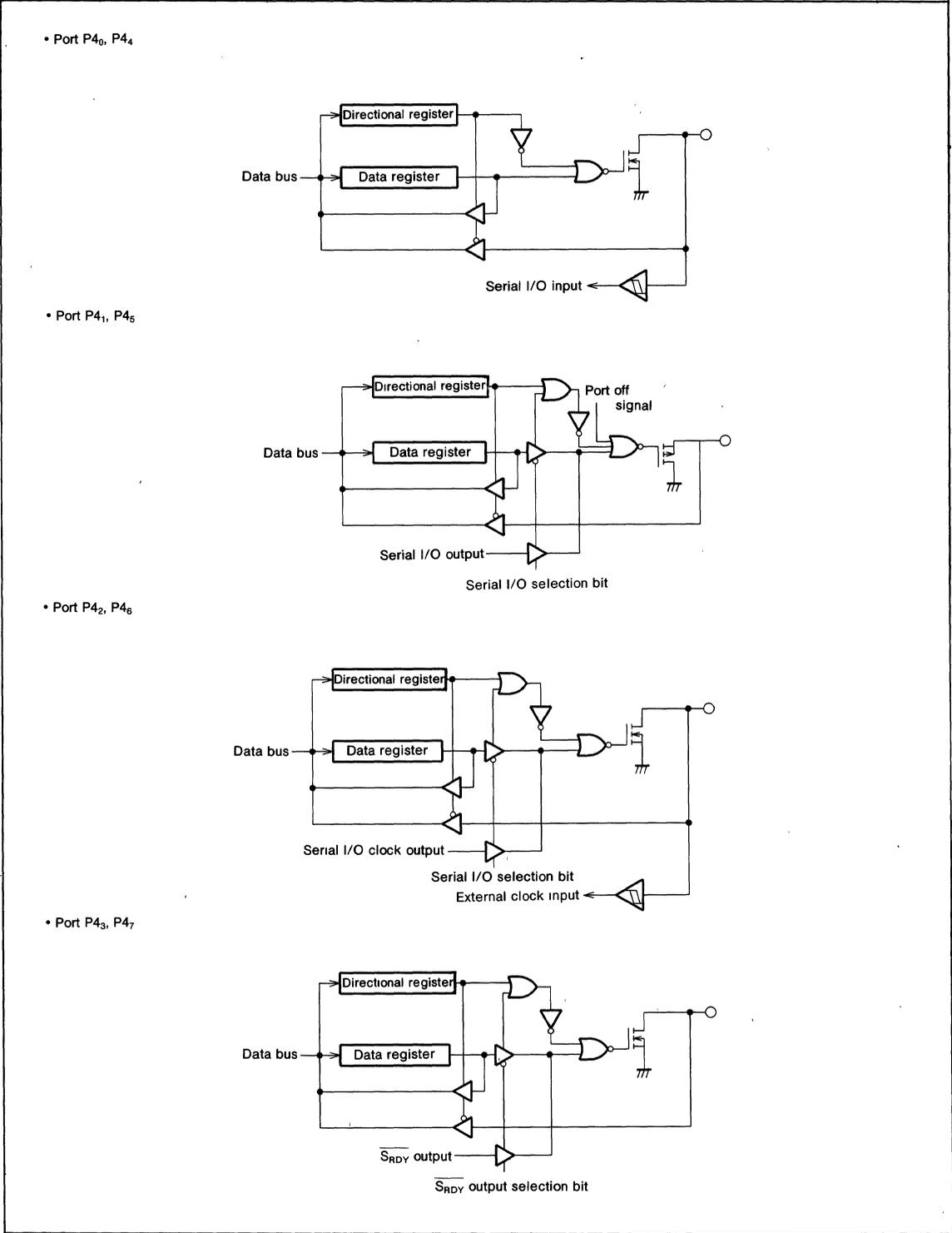


Fig. 36 Block diagram of Ports P4

CLOCK GENERATING CIRCUIT

The M37120M6-XXXFP has two internal clock generating circuits. Figure 40 shows a block diagram of the clock generating circuits. Normally, the frequency applied to the clock input pin X_{IN} divided by two is used as the internal clock (timing output) ϕ . Bit 7 of CPU mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN} .

Figure 37 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 38. An external clock signal cannot be supplied to the X_{CIN} pin open.

The M37120M6-XXXFP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 3 and timer 4 are forcibly connected and $\phi/8$ is selected as timer 3 input. When restarting oscillation, FF_{16} is automatically set in timer 3 and 07_{16} in timer 4 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 3 count stop bit and timer 4 count stop bit must be set to supply ("0"), timer 3 interrupt enable bit and timer 4 interrupt enable bit must be set to disable ("0").

Oscillation is restarted (release the stop mode) when INT, or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt or reset, the internal clock ϕ is held "H" until timer 4 overflows and is not supplied to the CPU.

The microcomputer enters an wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($36\mu A$ or less at $f(X_{CIN})=32kHz$, $V_{CC}=3V$). X_{IN} clock oscillation is stopped when the bit 6 of CPU mode register (address $00FB_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. Figure 41 shows the transition of states for the system clock.

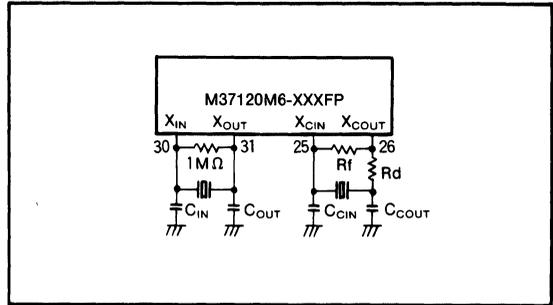


Fig. 37 Example ceramic resonator circuit

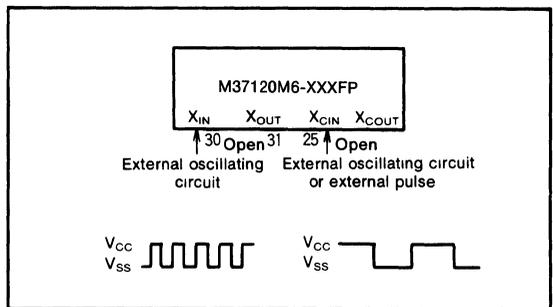


Fig. 38 Example clock input circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMER OSCILLATION CIRCUIT

Power is supplied to the timer clock oscillation circuit via a step-down regulator circuit to reduce the power consumption when the M37120M6-XXXFP is operating in timer mode. Since this step-down regulator circuit reduces the voltage applied to the V_{CC} pin to 1.4V (standard), the user can design a low-power timer mode. Bit 5 (CM_5) of the CPU mode register can be used to provide two-stage setting for the oscillation circuit: low-power mode when $CM_5 = 0$ and high-power mode when $CM_5 = 1$. Note that high-power mode is set after a reset, so the program must switch to low-power mode to enable low-power-consumption mode, after allowing time for the oscillation to stabilize.

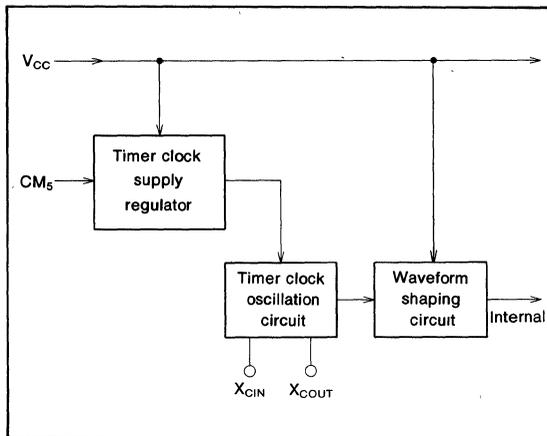


Fig. 39 Block diagram of the timer clock oscillation circuit

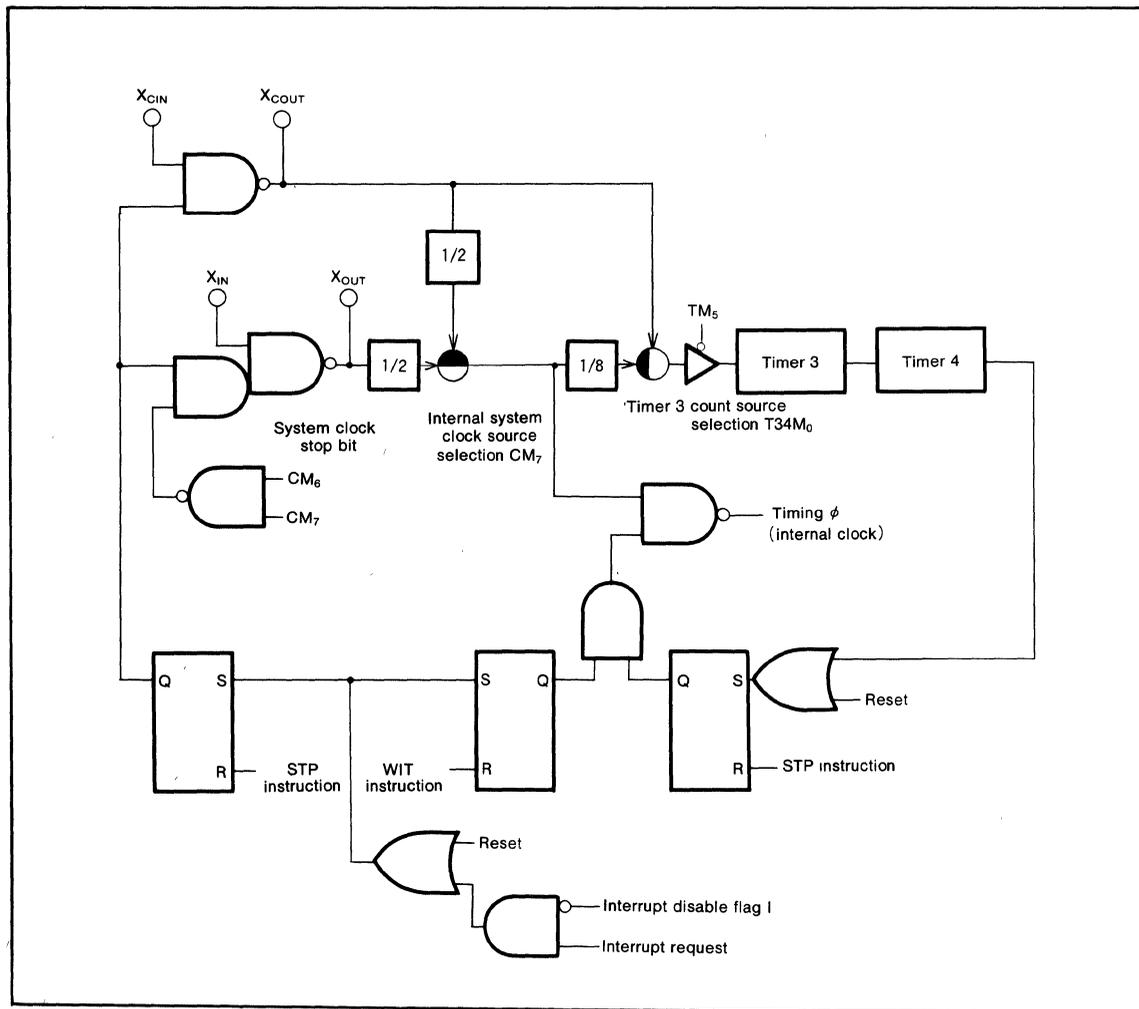


Fig. 40 Block diagram of clock generating circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

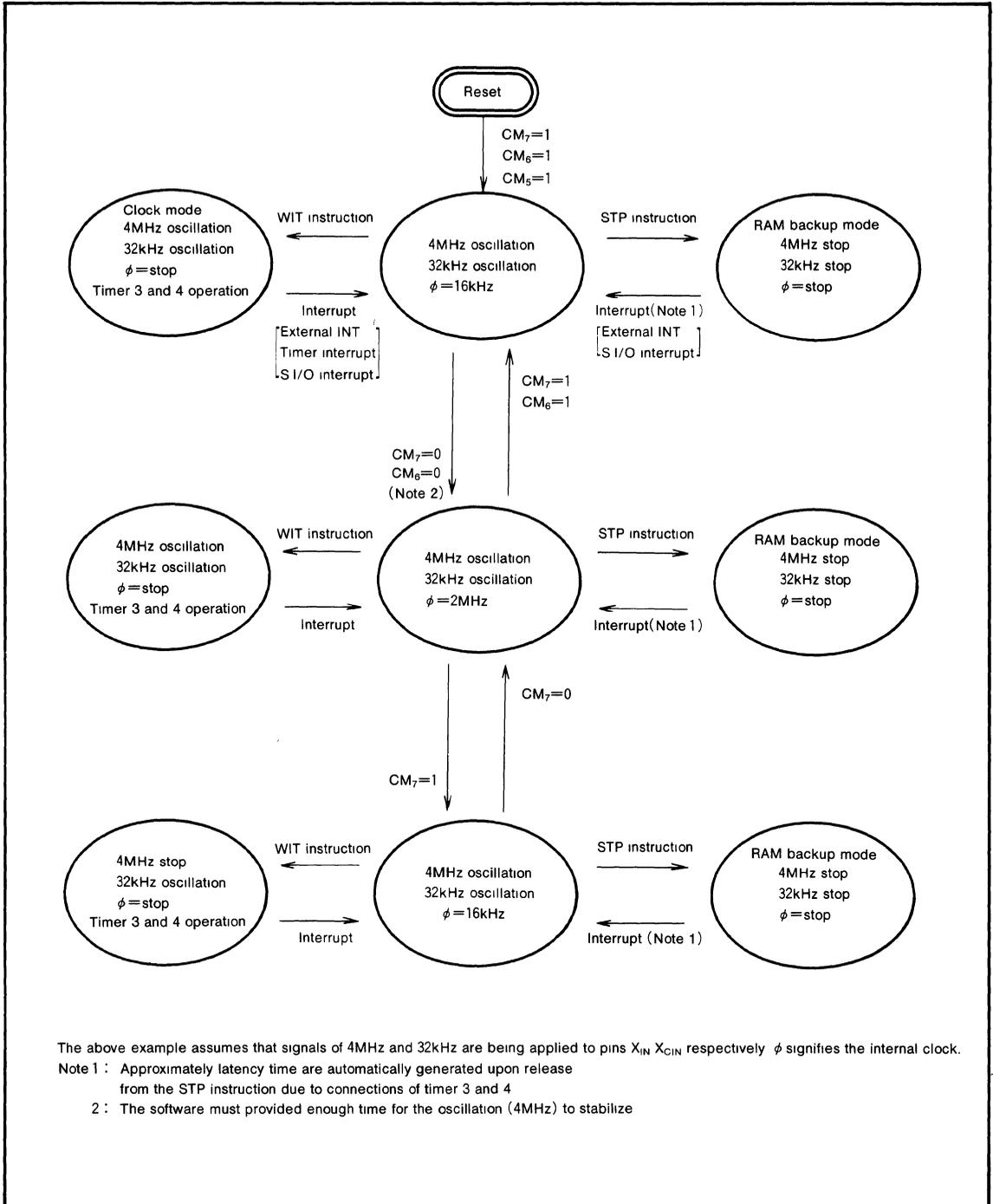
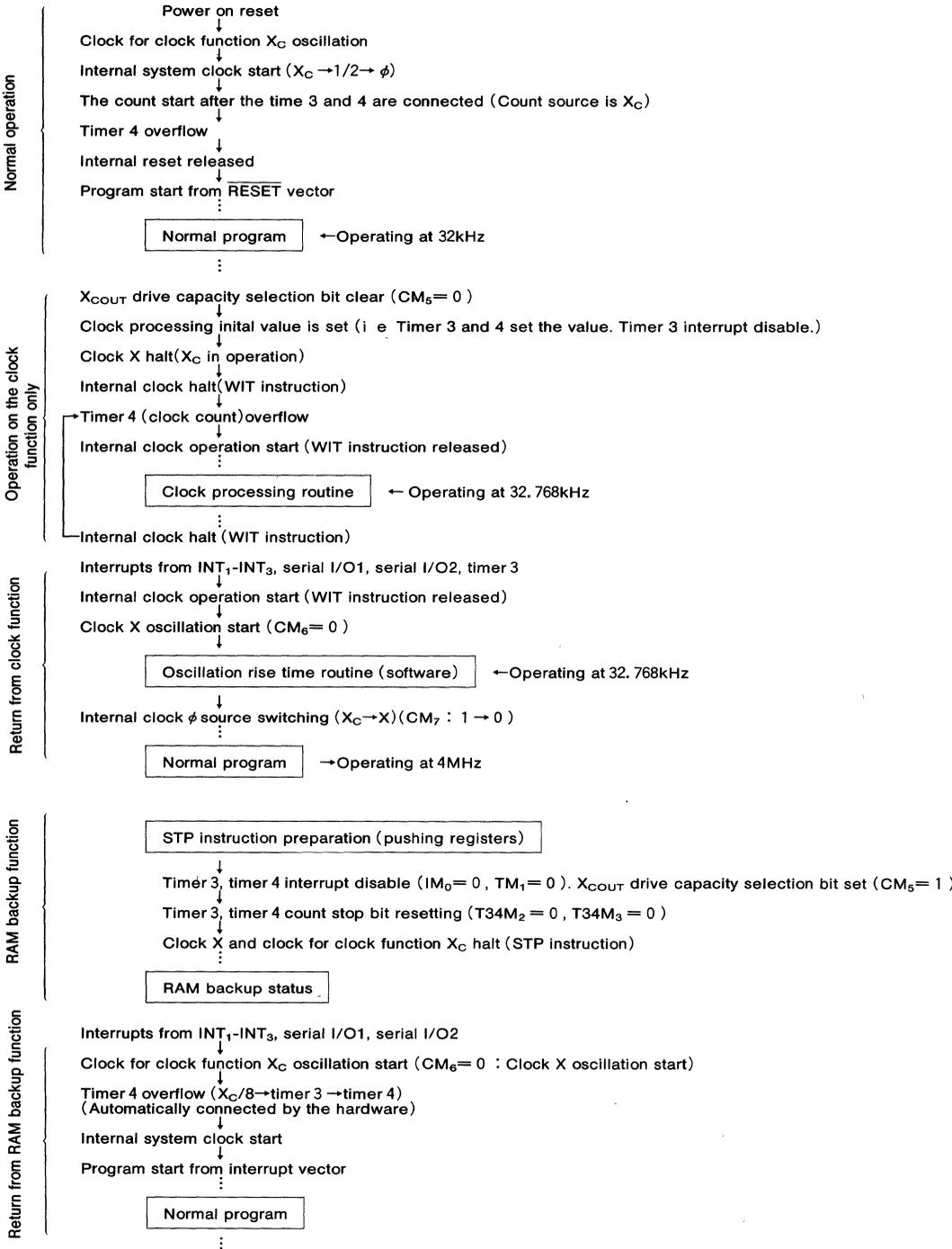


Fig. 41 Transition of states for the system clock

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

<An example of flow for system>



PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (4) An NOP instruction must be used after the execution of a PLP instruction.
- (5) When the interrupt is processed, confirm the interrupt enable bit is enable state after into the interrupt routine. If so, check the request flag after that.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mask specification form
- (3) ROM data EPROM 3 sets

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	-0.3 to 7.0	V
V_I	Input voltage RESET		-0.3 to 7.0	V
V_I	Input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7,$ $P3_0-P3_7, P4_0-P4_7, P6_0-P6_7,$ $P7_0-P7_3, X_{IN}, X_{CIN},$ $V_{REF}, V_{SYNC}, H_{SYNC}$		-0.3 to $V_{CC}+0.3$	V
V_O	Output voltage X_{COUT}		-0.3 to 2.5V (at high power mode) -0.3 to 1.5V (at low power mode)	V
V_O	Output voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7,$ $P3_0-P3_7, P4_0-P4_7, R, G, B, I, OUT1,$ $X_{OUT}, \phi, D-A_{OUT0}$ to $D-A_{OUT5}$		-0.3 to $V_{CC}+0.3$	V

RECOMMENDED OPERATING CONDITIONS

($V_{CC}=AV_{CC}=5V\pm 10\%$, $T_a=-10$ to $70^\circ C$ unless otherwise noted)

Symbol	Parameter	Limits			Unit	
		Min	Typ	Max		
V_{CC}	Supply voltage	$f(X_{IN})=4MHz$ (Note 1)	4.0	5.0	5.5	V
		$f(X_{CIN})=32kHz$ (Note 2)	2.5	5.0	5.5	
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	"H" input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7,$ $P3_0-P3_7, P4_0-P4_7, P6_0-P6_7,$ $P7_0-P7_3, X_{IN}, OSC1,$ RESET, H_{SYNC}, V_{SYNC}		$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0-P0_7, P1_0-P1_7, P2_0-P2_7,$ $P3_0-P3_7, P4_0-P4_7, P6_0-P6_7,$ $P7_0-P7_3, X_{IN}, OSC1, H_{SYNC}, V_{SYNC}$		0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage RESET		0		$0.15V_{CC}$	V
V_{REF}	Reference voltage input V_{REF}		4.0		V_{CC}	V
V_{IA}	Analog input voltage AN_0-AN_7		0		V_{REF}	V
$I_{OH}(avg)$	"H" average output current $P0_0-P0_7, P1_0-P1_7,$ (Note 3) $P2_0-P2_7, P3_0-P3_7,$ R, G, B, I, OUT1				1	mA
$I_{OL}(avg)$	"L" average output current $P0_0-P0_7, P1_0-P1_7,$ (Note 4) $P2_0-P2_7, P3_0-P3_7,$ $P4_0-P4_7, R, G, B, I, OUT1$				2	mA
$f(X_{IN})$	Clock oscillating frequency for main clock (Note 5)				4.2	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function (Note 5)				32.768	kHz
$f(OSC1)$	Clock oscillating frequency for OSD	6.0	7.0		8.0	MHz

Note 1 : At OSD operating, maximum value is 4.5V

2 : It is only at clock operation mode

Any other operation mode, maximum value is 4.0V

3 : The total of input current from IC should be 20mA max.

4 : The total of input current from IC should be 30mA max.

5 : Oscillation frequency is at 50% duty cycle.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ELECTRICAL CHARACTERISTICS ($V_{CC}=AV_{CC}=5V\pm 10\%$, $T_a=-10$ to 70°C unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
V_{OH}	"H" output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , φ, R, G, B, I, OUT1	$V_{CC}=4.5V$ $I_{OH}=-0.5mA$	2.4			V
V_{OL}	"L" output voltage P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , φ, R, G, B, I, OUT1	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
$V_{T+} - V_{T-}$	Hysteresis H _{SYNC} , V _{SYNC} , P6 ₀ -P6 ₃ , P4 ₀ , P4 ₂ , P4 ₄ , P4 ₆ , P3 ₄ (Note 1)	$V_{CC}=5.0V$		0.5		V
$V_{T+} - V_{T-}$	Hysteresis RESET	$V_{CC}=5.0V$		0.5		V
I_{IL}	"L" input current P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₃ , H _{SYNC} , V _{SYNC} , RESET	$V_{CC}=5.5V$ $V_I=0V$			5	μA
I_{IH}	"H" input current P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₃ , H _{SYNC} , V _{SYNC} , RESET	$V_{CC}=5.5V$ $V_I=5.5V$			5	μA
V_{RAM}	RAM retention voltage	At stop mode	2.0		5.5	V
I_{CC}	Supply current	At system operation, X _{IN} =4MHz, X _{CIN} =32kHz, f(OSC1)=7MHz, Output transistors are at "off" state		13	24	mA
		At system operation, V _{CC} =3.0V, X _{IN} =stop, X _{CIN} =32kHz, Output transistors are at "off" state		18	36	
		At low-speed operation mode, V _{CC} =3.0V, X _{IN} =stop, X _{CIN} =32kHz, At wait mode (CM ₅ =0), Output transistors are at "off" state		2	8	μA
		At stop mode, X _{IN} =X _{CIN} =stop, Output transistors are at "off" state		1	10	
I_{ACC}	Analog power supply		0.5	1.0	mA	

Note 1 : P4₀, P4₂, P4₄, P4₆ have the hysteresis only when these are used for serial I/O pins
P3₄ has the hysteresis only when this is used for a timer input pin

A-D CONVERTER CHARACTERISTICS

($V_{CC}=AV_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ\text{C}$, $f(X_{IN})=4\text{MHz}$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=AV_{CC}=V_{REF}=5.0V$		±1.5	±3.0	LSB
T_{CONV}	Conversion time				24.5	μs
V_{IA}	Analog input voltage		AV_{SS}		V_{REF}	V
V_{REF}	Reference input voltage		4.0		V_{CC}	V
R_{LADDER}	Ladder resistance value	$V_{REF}=5.0V$		40		kΩ
$I_{VREF(AD)}$	Reference input current (Note 1)	$V_{REF}=5.0V$			0.3	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

Note 1 : The total of I_{VREF} is the sum of $I_{VREF(AD)}$ and $I_{VREF(DA)}$.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

D-A CONVERTER CHARACTERISTICS

($V_{CC}=AV_{CC}=5\text{ V}$, $V_{SS}=AV_{SS}=0\text{ V}$, $T_a=25^\circ\text{C}$, $f(X_{IN})=4\text{ MHz}$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
—	Resolution				8	Bits
—	Full scale deviation	$V_{CC}=AV_{CC}=V_{REF}=5.0\text{ V}$			1.0	%
T_{SU}	Set time				3	μs
V_{REF}	Reference input voltage		4		V_{CC}	V
R_{OUT}	Output resistance		1	2	4	$\text{k}\Omega$
V_{AVSS}	Analog power supply input voltage			0		V
$I_{VREF(DA)}$	Reference power input current (Note 1)		0	2.5	5.0	mA

Note 1 : The total of I_{VREF} is the sum of $I_{VREF(AD)}$ and $I_{VREF(DA)}$.

$I_{VREF(DA)}$ is the reference power input current flowing when channel 1 of the DA converter is operating. (The other five DA converter register values are 00₁₆)

M37408M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PRELIMINARY

DESCRIPTION

The M37408M2-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 42-pin shrink plastic molded DIP. This single-chip microcomputer can be used as a slave-microcomputer for communication applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37408M2-XXXSP and the M37408M2-XXXFP are the package and the power dissipation capability (absolute maximum ratings).

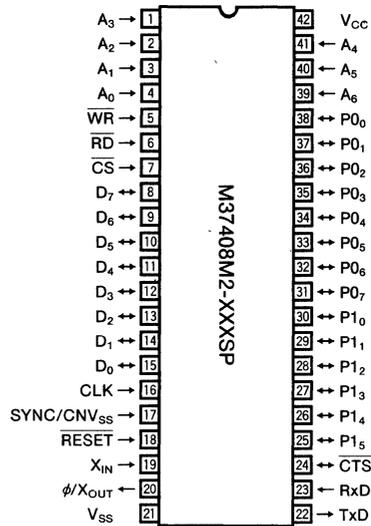
FEATURES

- Number of basic instructions..... 69
- Memory size ROM..... 4096 bytes
RAM..... 128 bytes
- Instruction execution time
... 0.8μs (minimum instructions at 10MHz frequency)
- Single power supply f(X_{IN})=10MHz..... 5V±10%
- Power dissipation
normal operation mode (at 10MHz frequency) .. 50mW
- Subroutine nesting..... 64 levels (Max.)
- Interrupt..... 6 types
- 8-bit timer..... 1
- UART (Full-duplex)..... 1 channels
- Dual-port RAM..... 64 bytes
- Communication registers
Access flag..... 64 bits
Collision detect register..... 4-bitX1
IPC* semaphore register..... 3-bitX1
IPC mode register..... 8-bitX2
IPC error register..... 8-bitX2
- Programmable I/O ports
(Ports P0, P1, CTS)..... 15
- Bus interface
Address bus..... 7
Data bus..... 8
Control signal (WR, RD, CS)..... 3

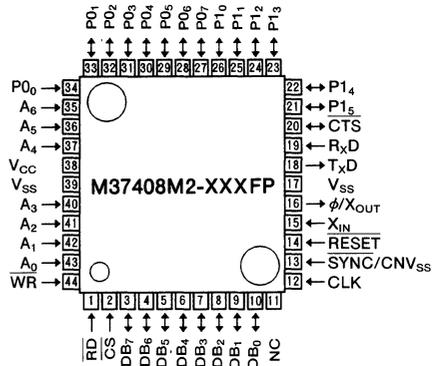
APPLICATION

Office automation equipment

PIN CONFIGURATION (TOP VIEW)



Outline 42P4B



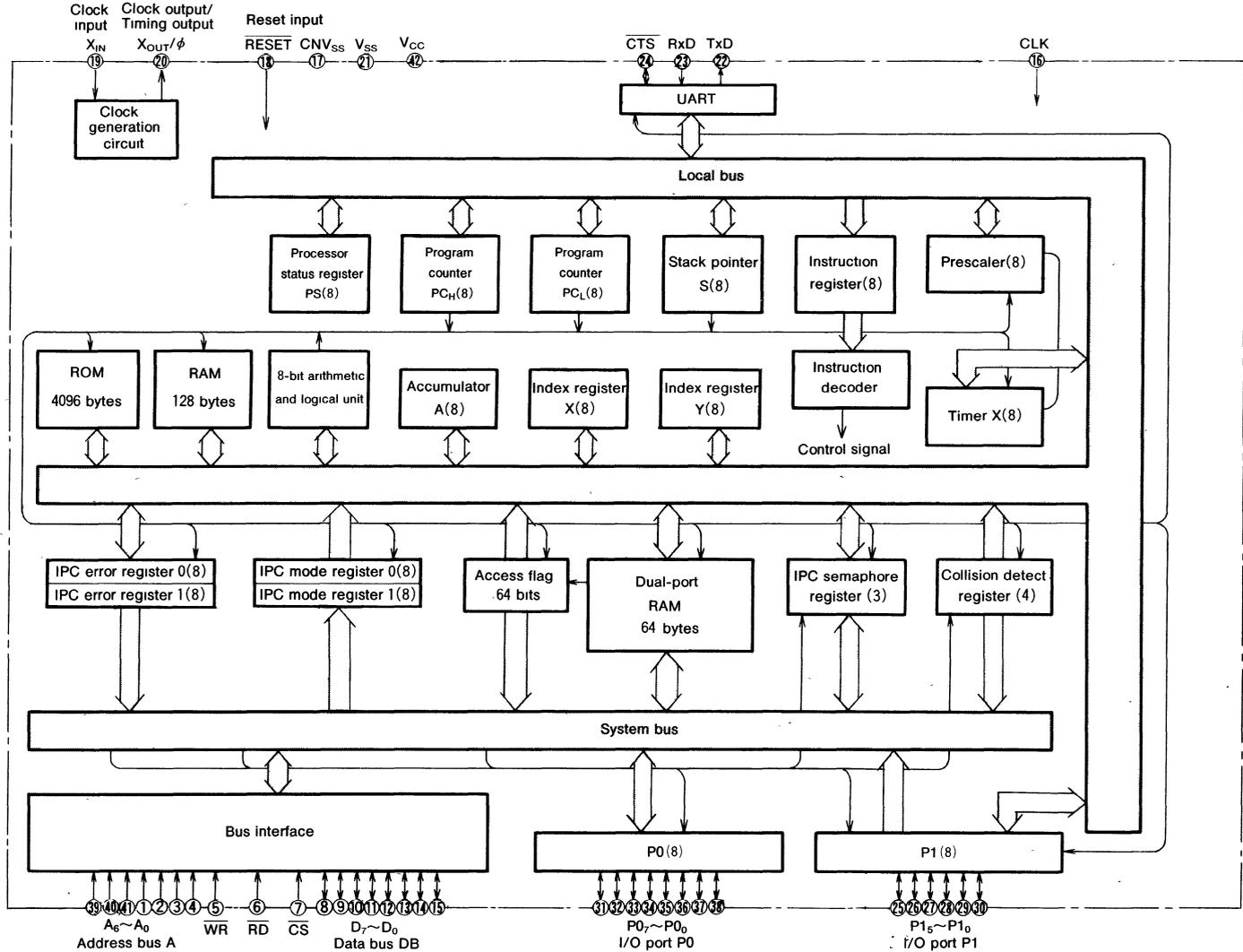
Outline 44P6N

NC : No connection

* IPC...Intelligent Protocol Controller



M37408M2-XXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MITSUBISHI MICROCOMPUTERS
M37408M2-XXXSP/FP

MITSUBISHI MICROCOMPUTERS
M37408M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37408M2-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			0.8 μ s (minimum instructions, at 10MHz frequency)
Clock frequency			10MHz
Memory size	ROM		4096 bytes
	RAM		128 bytes
Input/Output ports	P0 ₀ ~P0 ₇	I/O	8-bitX1 (System bus I/O)
	P1 ₀ ~P1 ₅	I/O	6-bitX1 (Local bus I/O, System bus input)
	CTS	I/O	1-bit (Common with UART transmit control input)
Bus interface	A ₀ ~A ₆	Input	7-bitX1
	D ₀ ~D ₇	I/O	8-bitX1
	RD, WR, CS	Input	1-bitX3
UART			1 (with programmable baud rate generator)
Timer			8-bitX1 (with 8-bit prescaler)
Interrupt			1 system bus (IPCM0) interrupt, 2 UART interrupts, 1 timer interrupt, 1 collision interrupt
Dual-port RAM			64 bytes
Communication registers	Access flag		64 bits
	Collision detect register		4-bitX1
	IPC semaphore register		3-bitX1
	IPC mode register		8-bitX2
	IPC error register		8-bitX2
Subroutine nesting			64 levels (max)
Clock generating circuit			Built-in (externally connected ceramic or quartz crystal)
Supply voltage			5V \pm 10%
Power dissipation	at operation		50mW
	at wait mode		5mW
	at stop mode	T _a =25°C	
T _a =70°C			0.5mW
Operating temperature range			-10~70°C
Device structure			CMOS silicon gate process
Package	M37408M2-XXXSP		42-pin shrink plastic molded DIP
	M37408M2-XXXFP		44-pin plastic molded QFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} , V_{SS}	Supply voltage		Power supply inputs $5V \pm 10\%$ to V_{CC} , and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS} .
\overline{RESET}	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than $2\mu s$ (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin
$P0_0 \sim P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with a directional register which allows each I/O bit to be individually programmed as input or output This port is connected only to the system bus, and can not be accessed from the local bus At reset this port becomes input mode. The output structure is CMOS
$P1_0 \sim P1_5$	I/O port P1	I/O	Port P1 is an 6-bit I/O port and has basically the same functions as port P0 This port is connected to the local bus and can be used as only input port from the system bus The output structure is CMOS output
T_xD	UART transfer output	Output	These are UART transfer data output pins.
R_xD	UART receive input	Input	These are UART receive data input pins
\overline{CTS}	UART transfer control input	I/O	These are UART transfer control signal input pins and can be used as I/O port which have basically same function as port P1.
CLK	UART clock input	Input	This port is an external clock input pin for baud rate
$A_0 \sim A_6$	Address input	Input	This port is input for system address
$D_0 \sim D_7$	Data input/output	I/O	This port is input or output the system data.
\overline{CS}	Chip select	Input	System data can be read or written by inputting "L" to this port
\overline{RD}	Read control input	Input	Memory or register data specified by $A_0 \sim A_6$ is read from $D_0 \sim D_7$ by inputting "L" to this port
\overline{WR}	Write control input	Input	Data input from $D_0 \sim D_7$ is written to memory or register specified by $A_0 \sim A_6$ by inputting "L" to this port

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37408 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

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ADDRESS AREA

M37408M2-XXXSP has two buses; the local bus connected to the CPU of its own, and the system bus connected to the CPU of the external master computer. There are two corresponding address area.

The local bus has thirteen address buses and eight data buses. The address area, which is 8192 bytes, is addresses from 0000₁₆ to 1FFF₁₆.

For this local bus area, addresses 1000₁₆ to 1FFF₁₆ are assigned to the built-in ROM area which consists of 4096 bytes.

The system bus has seven address buses and eight data buses. The address area, which is 128 bytes, is addresses from 00₁₆ to 7F₁₆.

The internal memories and registers are connected to one or both of these buses. Therefore, it is necessary, in writing programs, to know the operation of each functional block as well as to which bus the memories and registers are connected at what addresses.

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

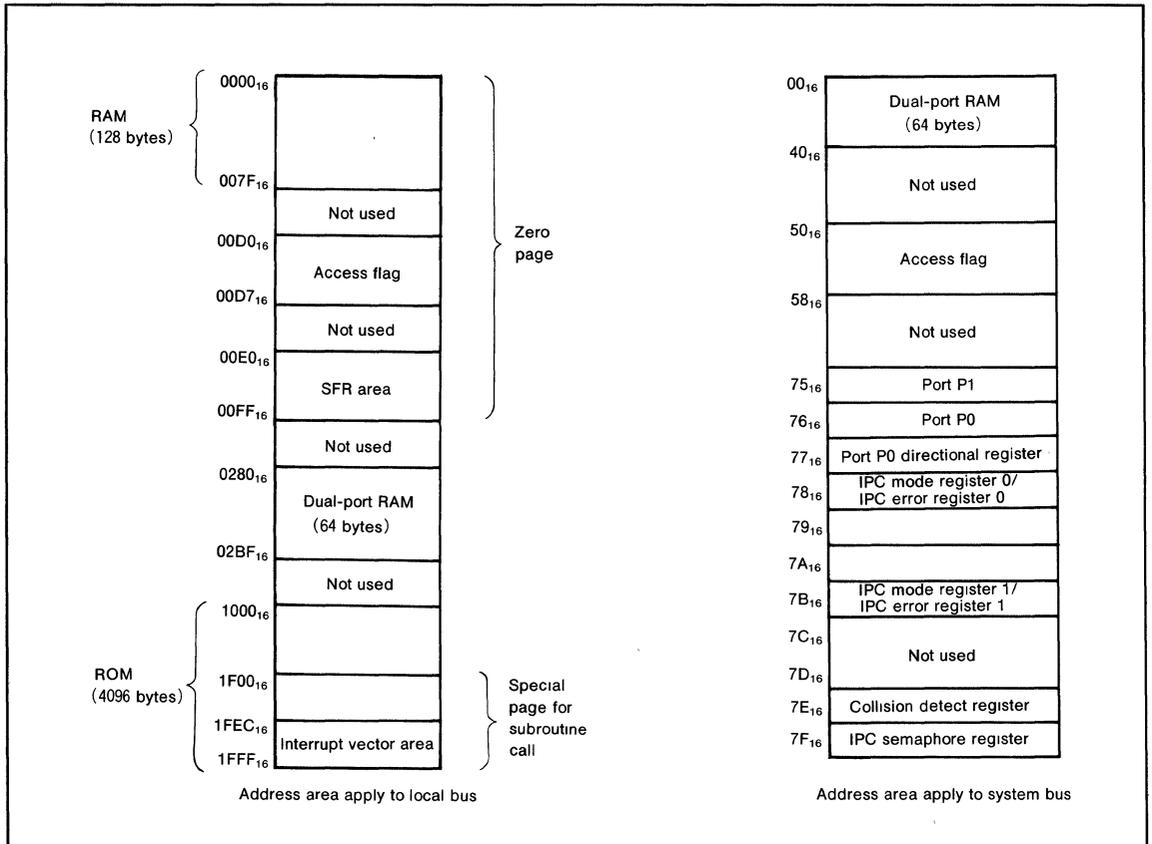


Fig. 1 Memory map

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00E0 ₁₆	Port P1	00F0 ₁₆	IPC mode register 0
00E1 ₁₆	Port P1 directional register	00F1 ₁₆	
00E2 ₁₆	Dual-port RAM direction specify register	00F2 ₁₆	
00E3 ₁₆		00F3 ₁₆	IPC mode register 1
00E4 ₁₆		00F4 ₁₆	IPC error register 0
00E5 ₁₆		00F5 ₁₆	
00E6 ₁₆		00F6 ₁₆	
00E7 ₁₆		00F7 ₁₆	IPC error register 1
00E8 ₁₆		00F8 ₁₆	
00E9 ₁₆		00F9 ₁₆	IPC semaphore register
00EA ₁₆		00FA ₁₆	Collision detect register
00EB ₁₆		00FB ₁₆	Interrupt enable register
00EC ₁₆	UART receive/transfer buffer register	00FC ₁₆	Interrupt request register
00ED ₁₆	UART status register/UART mode register	00FD ₁₆	Prescaler X
00EE ₁₆	UART control register	00FE ₁₆	Timer X
00EF ₁₆	UART divider for baud rate generate	00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

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Bus Interface

M37408M2-XXXSP has the bus interface to operate itself by the control signal sent from the master CPU. The master CPU can access the memories and registers located in the system address area described below via this bus interface. The bus interface has address pins A_0 to A_6 , data pins D_0 to D_7 , and three controls signals \overline{CS} , \overline{WR} , and \overline{RD} which can be directly connected to TTL.

Driving the \overline{CS} pin to "L" put this microcomputer in the read/write enabled state. When writing data from the mas-

ter CPU, specify the address by $A_0 \sim A_6$ and set \overline{WR} to "L", and the data at $D_0 \sim D_7$ is written to the specified address. When reading data, specify the address by $A_0 \sim A_6$ and set \overline{RD} to "L", and the contents of the specified address are output to $D_0 \sim D_7$.

Driving the \overline{CS} pin to "H" puts the M37408M2-XXXSP in the state which does not allow the read and write operations from the master CPU. At this time, the outputs of D_0 to D_7 are in the floating state.

Figure 3 shows the block diagram of the bus interface.

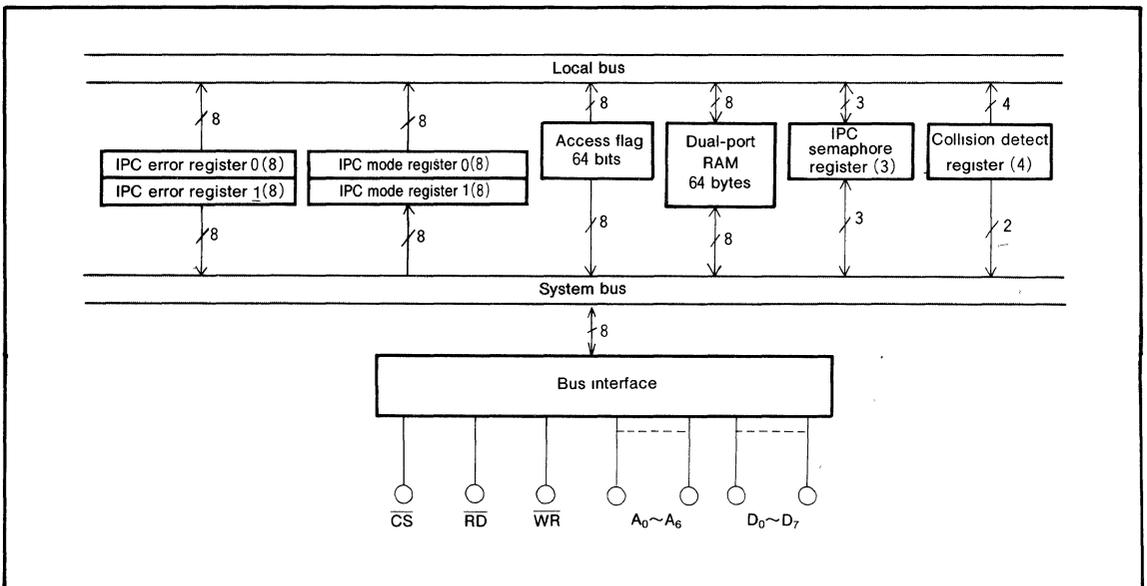


Fig. 3 Block diagram of bus interface

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Dual-port RAM

The dual-port RAM, which is 64 bytes, is the memory which allows the read/write operation from both the local and system buses independently. From the local bus, it is allocated at addresses 0280₁₆ to 02BF₁₆; from the system bus, addresses 00₁₆ to 3F₁₆. Table 1 shows the result when the write and read operations from both buses compete at the same address.

Table 1. Result obtained by simultaneously accessing the same address from the system and local buses

	Write	Read
Simultaneous read from both buses	—	Correct data
Simultaneous write from both buses	Unpredictable	—
Read from one bus, write from the other	Correct data	Uncertain

[Access flag]

Local bus : address 00D0₁₆~00D7₁₆
System bus : address 50₁₆~57₁₆

The access flag arbitrates the access to the dual-port RAM. One bit of access flag is allocated to one byte of dual port RAM, amounting 64 bits (8 bytes) in total. The access flag can be read from both the system and local buses. Figure 4 shows the relationship between each byte of the dual port RAM and each bit of the access flag. Each bit is cleared to "0" when an access to read is made to the dual port RAM from either bus, it is set to "1" when an access to write is made. If an access to read from one bus and an access to write from the other compete at the same address of the dual port RAM, the values of the corresponding access flags are uncertain. At reset, all access flags are cleared to "0".

[Dual-port RAM direction specify register]

Local bus : address 00E2₁₆

This register specifies that the read operation of which bus clears each bit of the access flag. One bit of this register corresponds to 32 bytes of the dual-port RAM (32 bits of the access flag). This register consists of two bits. Each access flag is cleared by the read operation from the system bus when the corresponding dual-port RAM direction specify register is "0"; when it is "1", each access flag is cleared by the read operation from the local bus. As for a write operation, the access flag is set regardless of which bus has made it. Table 2 shows the relationship between each bit of the dual-port RAM direction specify register and the dual-port RAM and the access flag. At reset, all bits are cleared to "0".

		access flag							
Local bus address	System bus address	7				0			
00D0 ₁₆	50 ₁₆	07	06	05	04	03	02	01	00
00D1 ₁₆	51 ₁₆	0F	0E	0D	0C	0B	0A	09	08
00D2 ₁₆	52 ₁₆	17	16	15	14	13	12	11	10
⋮	⋮	⋮							
⋮	⋮	(Note)							
⋮	⋮	⋮							
00D7 ₁₆	57 ₁₆	3F	3E	3D	3C	3B	3A	39	38

(Note) The numeric shows the system bus address of dual-port RAM corresponds to each access flag. Dual-port RAM direction specify register specifies which bus read-out resets the access flag bit.

Fig. 4 Correspondence between each byte of dual-port RAM and each bit of access flag

Table 2. Correspondence among each bit of dual-port RAM direction specify register, dual-port RAM and access flag

Dual-port RAM direction specify register	Dual-port RAM		Access flag	
	Local bus address	System bus address	Local bus address	System bus address
bit 4	0280 ₁₆ ~029F ₁₆	00 ₁₆ ~1F ₁₆	00D0 ₁₆ ~00D3 ₁₆	50 ₁₆ ~53 ₁₆
bit 5	02A0 ₁₆ ~02BF ₁₆	20 ₁₆ ~3F ₁₆	00D4 ₁₆ ~00D7 ₁₆	54 ₁₆ ~57 ₁₆

[IPC mode register, IPC error register]

Local bus : address 00F0₁₆~00F7₁₆
System bus : address 78₁₆~7B₁₆

IPC mode registers 0~1 (IPCM0~IPCM1) and IPC error registers 0~1 (ERR0~ERR1) are the 8-bit registers which can be set by the user without restriction. IPC mode registers 0~1 are used to specify the mode setting such as UART from the external master CPU via the system bus. IPC error registers 0~1 are used to indicate the error found on the local CPU to the outside via the system bus. On the system bus, IPC mode registers 0~1 and IPC error registers 0~1 share two bytes of the same address, with the former being for write only and the latter for read only. On the local bus, the former is for read only and the latter is for both read and write.

The data written from the system bus to IPC mode registers 0~1 can be read from the local bus only. If an access to read or write is performed from the system bus on IPC mode register 0/IPC error register 0, an interrupt request (IPCM0) is caused.

When IPC error registers 0~1 are accessed for read from the system bus, only the bits which are found "1" are reset by hardware. When these registers are read from the local bus, their values remain unchanged.

[IPC semaphore register]

Local bus : address 00F9₁₆
System bus : address 7F₁₆

This register is for handshaking with the master CPU and consists of block semaphore flags (BS₄~BS₅) and the ready flag (RDY). BS₄~BS₅ can be read/written from both the local and system buses. RDY can be read/written from the local bus and read only from the system bus. With this register, all bits can be read at a time but, in a write operation, only one bit can be written at a time. The low-order three bits of the data to be written are used to specify to which register bit the data is to be written. Bit 7 is used to specify whether to write "1" or "0". At reset, all bits are cleared to "0".

RDY is cleared to "0" also when an access to write is performed by the system bus on IPC mode register 0.

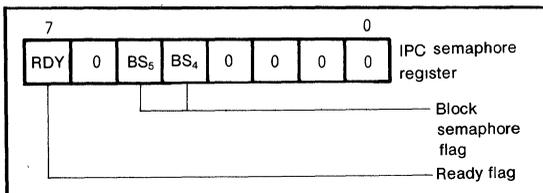


Fig. 5 Bit structure of IPC semaphore register

[Collision detect register]

Local bus : address 00FA₁₆
System bus : address 7E₁₆

This register consists of two bits of collision detect flags (CD₄~CD₅), the collision interrupt enable bit, and collision interrupt request bit. The collision detect flags are set when an access to read is performed by the system bus on the same address on the dual port RAM to which the local bus is writing data. These flags indicate that the data read by the master CPU may be incorrect. When these flags are set, a collision detect interrupt request occurs.

Each collision flag corresponds to each 32 bits of the dual port RAM. The flag bit corresponding to the address at which access competition occurred is set. The relationship between the flag bits and the dual port RAM is shown in Table 3. These flags can be read from both buses. All bits are cleared when read from the system bus or at reset.

The collision interrupt enable bit can be read/written from the local bus. When it is read from the system bus, "0" is always output. The collision interrupt request bit can be read only from the local bus. Only "0" can be written.

Table 3. Correspondence between collision detect flag and dual-port RAM

Collision detect flag	Dual-port RAM	
	Local bus address	System bus address
CD ₄	0280 ₁₆ ~029F ₁₆	00 ₁₆ ~1F ₁₆
CD ₅	02A0 ₁₆ ~02BF ₁₆	20 ₁₆ ~3F ₁₆

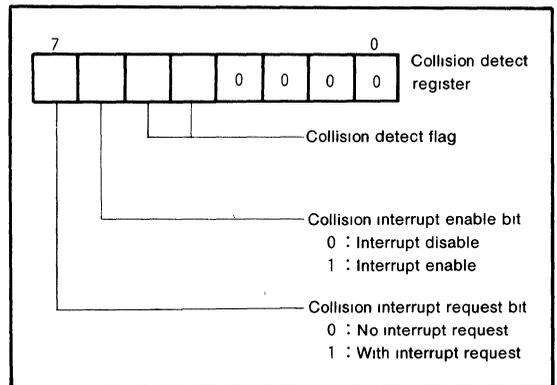


Fig. 6 Structure of collision detect register

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INTERRUPT

Interrupts can be caused by 6 different events.

Interrupts are vectored interrupts with priorities shown in Table 4. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit bit is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 7 shows interrupts control.

All interrupt request bits except the collision interrupt are in the interrupt request register (address 00FC₁₆). The collision interrupt request bit is in the collision detect register (address 00FA₁₆). The interrupt request bit is set when the following conditions occur:

- (1) When the data is set to receive buffer of UART
- (2) When the master CPU accesses the IPC mode/IPC error register 0 through bus interface
- (3) When the contents of the timer X goes to "0"
- (4) When one of the bit 4~bit 5 of the collision detect register is set to "1"
- (5) When the data is set to transmit buffer of UART

There are two interrupt enable bits for each interrupt except collision interrupt. One is in interrupt enable register (address 00FB₁₆), the other is in UART control register (address 00EE₁₆) or timer control register (address 00FF₁₆). Interrupts are become enable when these two enable bits are both "1". The collision interrupt enable bit is in bit 6 of collision detect register.

UART transmit interrupt is controlled by $\overline{\text{CTS}}$ function select bit and CTS pin input (see UART section).

Since the BRK instruction interrupt and the UART transmit interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if UART transmit generated the interrupt.

Table 4. Interrupt vector address and priority

Interrupt	Priority	Vector addresses
RESET	1	1FFF ₁₆ , 1FFE ₁₆
UART receive	2	1FF9 ₁₆ , 1FF8 ₁₆
IPCM0	3	1FF7 ₁₆ , 1FF6 ₁₆
Timer X	4	1FF5 ₁₆ , 1FF4 ₁₆
Collision	5	1FF3 ₁₆ , 1FF2 ₁₆
UART transmit/ BRK instruction	6	1FED ₁₆ , 1FEC ₁₆

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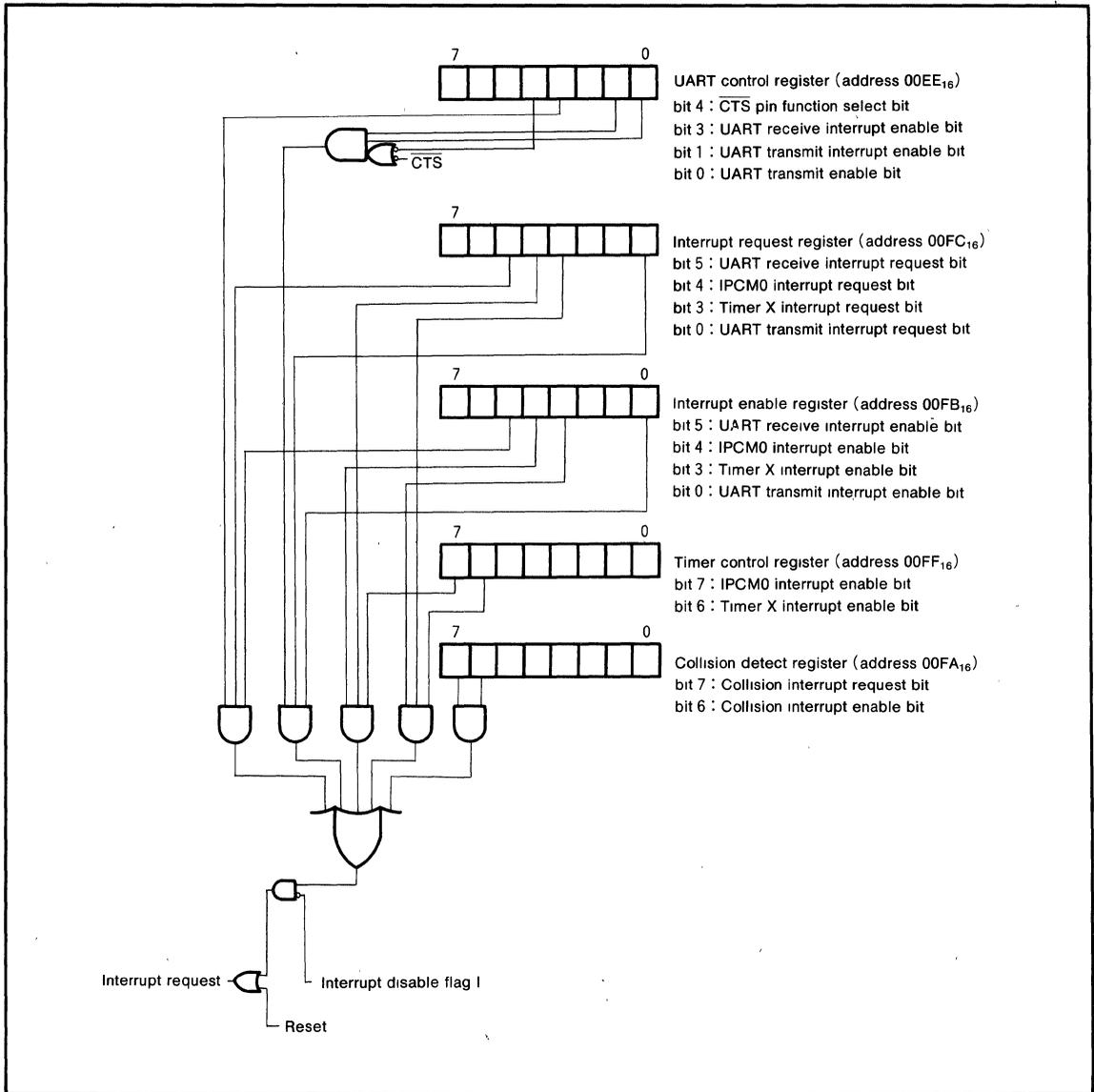


Fig. 7 Interrupt control

TIMER

The M37408M2-XXXSP has one timer: timer X. It has an 8-bit prescaler. Each timer or prescaler is structured with 8-bit counter. A block diagram of timer X is shown in Figure 9. Timer or prescaler is a down-counter which is reloaded from the latch when the next clock pulse after the timer reaches zero. The division ratio is defined as $1/(n+1)$ where n is the decimal contents of the timer latch. The timer interrupt request bit (bit 3 of the address $00FC_{16}$ of local address bus) is also set to "1" at this time. Timer counts the oscillation frequency divided by 16 when the bit 5 of timer control register is "0", and stops when "1". The structure of the timer control register is shown in Figure 8.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16} , respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. For more details on the STP instruction, refer to the oscillation circuit section.

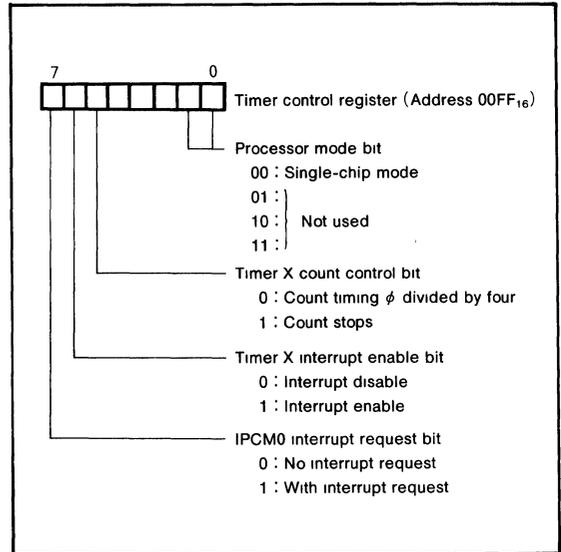


Fig. 8 Structure of timer control register

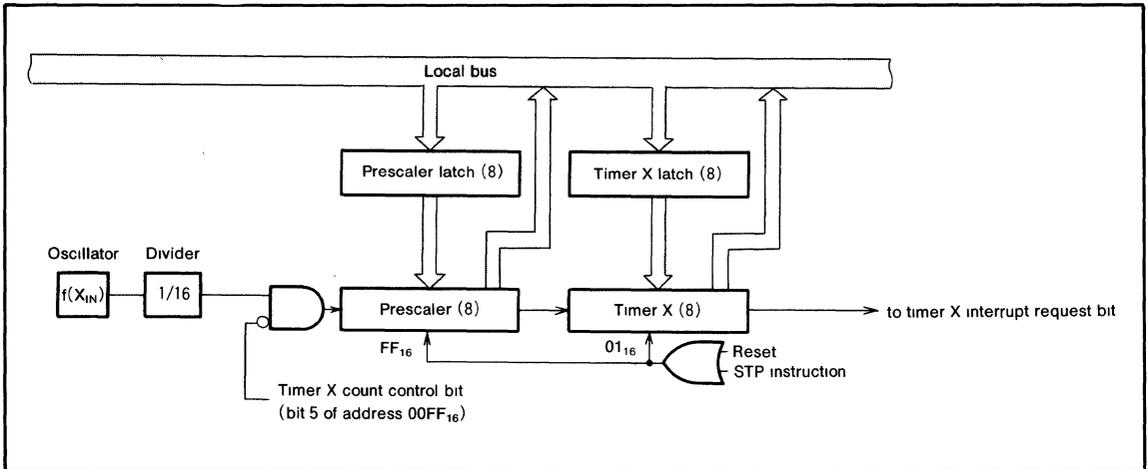


Fig. 9 Timer X block diagram

UART

The M37408M2-XXXSP contains one channel of UART. This UART has three pins TxD (transmit output), RxD (receive input), and CTS (clear to send) and contains the receive (transmit) shift register, the receive (transmit) buffer register, the UART mode register, the UART control register, the UART status register, and the baud rate generating divider. It also has a CLK pin the input pin of the external clock for baud rate generation. An interrupt can be generated at receive and transmit independently.

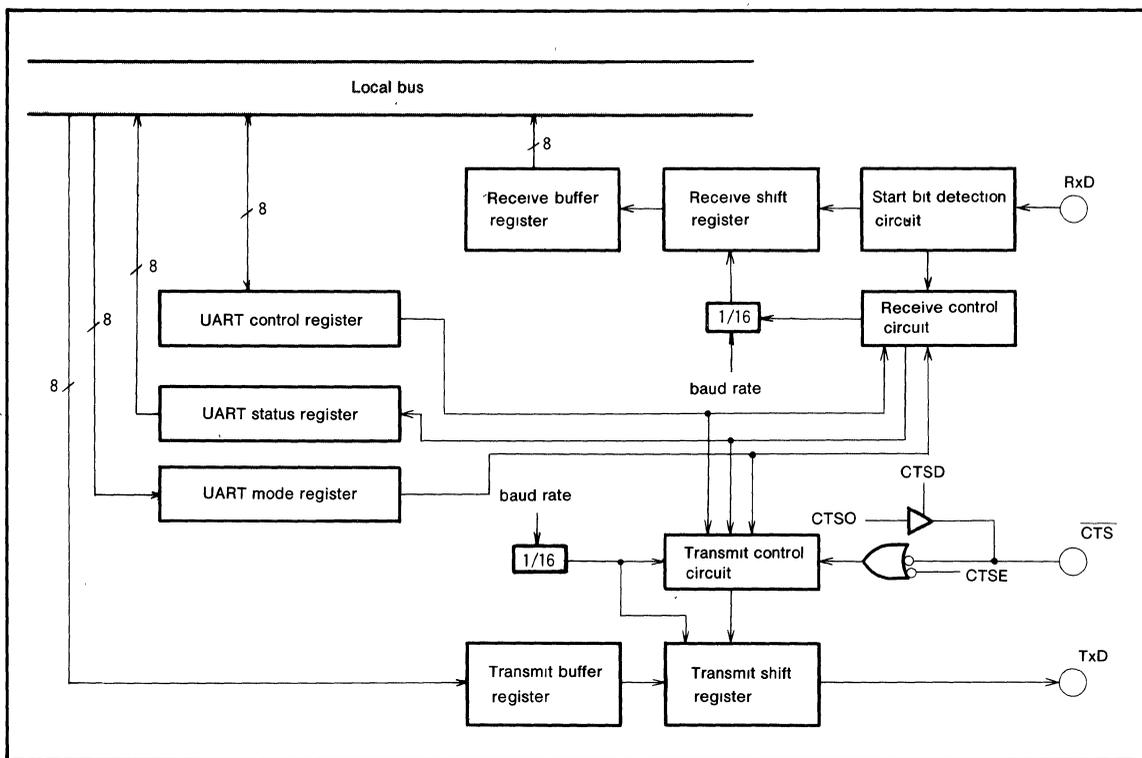


Fig. 10 UART block diagram

[Receive operation]

Setting the receive enable bit (bit 2 of the UART control register) to "1" puts the system in the receive enable state. When there is no input of receive data, "H" is input to RxD pin. When the falling edge is input to RxD pin and "L" input is detected twice consecutively by sampling with the clock having a frequency 16 times the baud rate, the start bit is triggered. Then, sampling is performed three times in the middle of the start bit. When "L" is detected twice or more, the receive operation begins, capturing the data bits into the receive shift register. If "L" has not been detected twice or more, start bit detection begins again. When the data bits and parity bit have been captured into the receive shift register and the stop bit is detected, the receive data is transferred from the receive shift register to the receive buffer register, setting the receiver ready flag (bit 1 of the UART status register). If a parity error occurred, the parity error flag is set. The framing error flag is set when the first stop bit is found "L". If the previous data has not been read out of the receive buffer register, the overrun error flag is set, clearing the previous data. The receiver ready flag is reset when the receive buffer register is read. Each error flag can be reset by writing "1" to the error flag reset bit (bit 7 of the UART control register). Any of these errors does not affect the receive operation. The data bit, the parity bit, and the stop bit are sampled three times in the middle of them each. When "L" or "H" is detected twice or more, "0" or "1" is determined respectively. Each time a receive operation has been completed, setting the receiver ready flag, the UART receive interrupt request bit (bit 7 of the interrupt request register) is set. An interrupt is acknowledged when the two UART receive interrupt enable bits (bit 3 of the UART control register and bit 7 of the interrupt enable register) are both "1", and the interrupt disable flag 1 is "0". The UART receive interrupt request bit is reset when a UART receive interrupt is acknowledged. Setting the receive enable bit (bit 2 of the UART control register) to "0" puts the system in the receive stopped state. At this time, the receiver ready flag is "0" (ready), the receive shift register is in the stopped state, and the start bit detection is stopped.

[Transmit operation]

When the send data is written to the transmit buffer register, the start bit, parity bit, and stop bit are added to the data, which is transferred to the transmit shift register. The transmit shift register begins shift when it becomes enable for transmission, sending the serial data to TxD pin. For the description of the transmit enable state, see Table 5. In the transmit enable state, each time transmission of the stop bit of the serial data being transmitted has been completed, it is checked whether the next data has been written to the transmit buffer register. If the data is found written, transmission of the next data begins. If the data is found not written, TxD pin is held at "H" until the next transmit data is written, setting the transmitter empty flag. When the transmit enable state is cleared during transmission, the transmission is stopped after completing the transmission of the transmit data so far written to the transmit buffer register. When the transmitter ready flag (bit 0 of the UART status register) is "1", it indicates that the transmit buffer is ready for writing data. The immediately preceding data is transferred from the transmit buffer register to the transmit shift register. Every time the start bit is output from TxD pin, this flag is set. Every time the transmitter ready flag is set, the UART transmit interrupt request bit (bit 2 of the interrupt request register) is set. An interrupt is acknowledged when two UART transmit interrupt enable bits (bit 3 of the UART control register and bit 2 of the interrupt enable register) are both "1" and the interrupt disable flag 1 is "0". Note that an interrupt occurs only in the transmit ready state. Bit 6 of the UART control register initializes the UART transmit side. When this bit "0", the transmit side is in the initial state.

Table 5. Bit and pin states when transmission is enable

TE	CTSE	CTS	TE	CTSE	CTS	
1	0	X	TE	: UART transmit enable bit	CTSE	: CTS pin function selection bit
	1	L	CTS	: CTS pin input level		

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[UART divider for baud rate generator]

This is an 8-bit programmable divider which generates the baud rate for the UART receive or transmit operation.

When the setting value is N_{BR} (0 to 255), the divide ratio becomes $1/(N_{BR}+1)$. There are three count sources; X_{IN} clock divided by 2, X_{IN} clock divided by 32, and the external clock. Choose sources by bits 4 and 5 of the UART mode register. Table 6 shows the baud rate calculation for each bit combination.

When the external clock is used, the frequency of the input clock must be below 1.6MHz. Writing to the baud rate generating divider must be performed when bits 2 and 6 of the UART control register are both "0".

Table 6. Baud rate calculation

EX	BR	Calculation
0	0	$\text{baud rate (bps)} = \frac{f(X_{IN})}{32(N_{BR}+1)}$
0	1	$\text{baud rate (bps)} = \frac{f(X_{IN})}{512(N_{BR}+1)}$
1	X	$\text{baud rate (bps)} = \frac{f(\text{CLK})}{16(N_{BR}+1)}$

EX : Clock selection bit for baud rate generator
BR : Divide ratio selection bit for baud rate generator

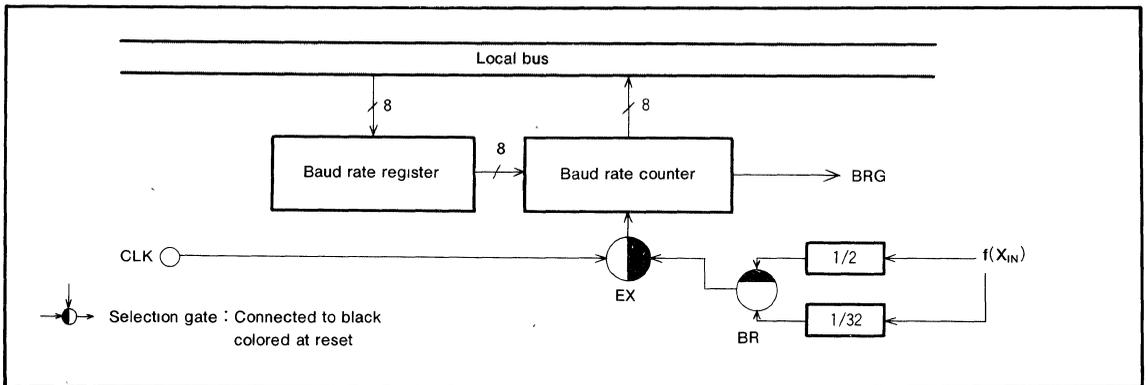


Fig. 11 Baud rate generating circuit

[CTS pin]

The $\overline{\text{CTS}}$ pin can be used as the 1-bit I/O port when bit 4 of the UART control register (CTSE) is "0". In this case, the input/output direction can be determined by bit 7 of the UART mode register (CTSD) and the output data can be set by bit 5 of the UART control register (CTSO). Additionally, the input level can be known by bit 7 of the UART status register (CTS).

[UART mode register]

- Parity enable bit : PEN
Setting this bit to "1" adds a parity bit to the transmit data. In a receive operation, this bit is used for parity evaluation.
- Parity select bit : EVN
This bit specifies the parity bit to be generated in a transmit operation and the parity bit to be evaluated in a receive operation. Depending on the content of this bit, the number of 1's in data is made even or odd.
- Character length select bit : CHL
This bit specifies the character length of data.
- Stop bit length select bit : ST
This bit specifies the stop bit length.
- Baud rate generating prescaler divide ratio select bit : BR
When this bit is "0", the signal obtained by dividing X_{IN} clock by 2 becomes the count source of the baud rate divider. When this bit is "1", the signal is obtained by dividing the clock by 32.
- Baud rate generating synchronous clock selection bit : EX
This bit specifies baud rate synchronous clock. When this bit is "1", external clock is input from the CLK pin.
- $\overline{\text{CTS}}$ pin I/O select bit : CTSD
When this bit is "0", the $\overline{\text{CTS}}$ pin is the input pin.
When this bit is "1", the pin is the output pin. To use the $\overline{\text{CTS}}$ pin as the $\overline{\text{CTS}}$ input, set "0".

[UART control register]

- Transmit enable bit : TE
Setting this bit to "1" enables a transmit operation.
- Transmit interrupt enable bit : TIE
When this bit is "1", the interrupt in a transmit operation is enabled.
- Receive enable bit : RE
Setting this bit to "1" enables a receive operation.
- Receive interrupt enable bit : RIE
When this bit is "1", the interrupt in a receive operation is enabled.
- $\overline{\text{CTS}}$ pin function select bit : CTSE
When this bit is "1", the $\overline{\text{CTS}}$ pin becomes the $\overline{\text{CTS}}$ input.

- $\overline{\text{CTS}}$ output data select bit : CTSO
When this bit is "0", "L" is output. When it is "1", "H" is output.
- Transmit side initialize bit : MR
When this bit is "0", the transmit side is initialized.
- Error flag reset select bit : ERST
Setting this bit to "1" resets all error flags. When this bit is read, "0" is always read.

[UART status register]

- Transmitter ready flag : TxRDY
When this flag is "1", it indicates that the transmit buffer register is empty and ready for writing transmit data.
- Receiver ready flag : RxRDY
When this flag is "1", it indicates that the receive buffer register is holding receive data. When the receive buffer register is read, it is cleared.
- Transmitter empty flag : TEMP
When this flag is "1", it indicates that neither the transmit shift register nor the transmit buffer register holds the data to be transmitted.
- Parity error flag : PE
This bit is set to "1" when the parity of the received data is different from the parity which was set.
- Overrun error flag : OR
When this flag is "1", it indicates that, before the data in the receive buffer register is read, the next data is transferred from the receive shift register to the receive buffer register and the previous data is lost.
- Framing error flag : FE
This flag is set to "1" when the stop bit is found "L" when data is transferred from the receive shift register to the receive buffer register.
- $\overline{\text{CTS}}$ pin input level flag : $\overline{\text{CTS}}$
When the input level of the $\overline{\text{CTS}}$ pin is "L", "0" is read; when it is "H", "1" is read.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

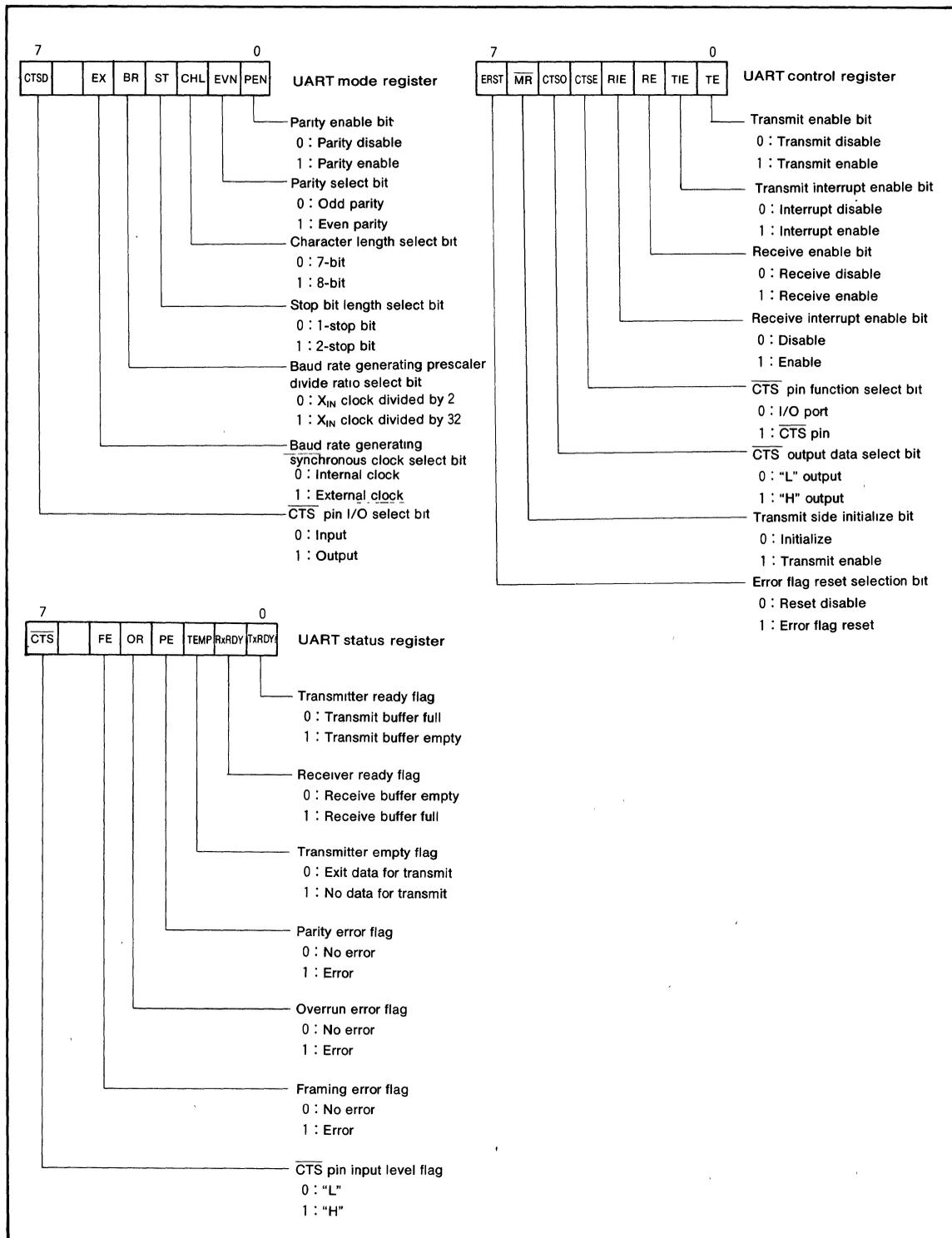


Fig. 12 Structure of registers related to UART

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

RESET CIRCUIT

The M37408M2-XXXSP is reset according to the sequence shown in Figure 14. It starts the program from the address formed by using the content of address $1FFF_{16}$ as the high order address and the content of the address $1FFE_{16}$ as the low order address, when the RESET pin is held at "L" level for more than $2\mu s$ while the power voltage is in the recom-

mended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 15 and 16.

An example of the reset circuit is shown in Figure 13. When the power on reset is used, the RESET pin must be held "L" until the oscillation of X_{IN} - X_{OUT} becomes stable.

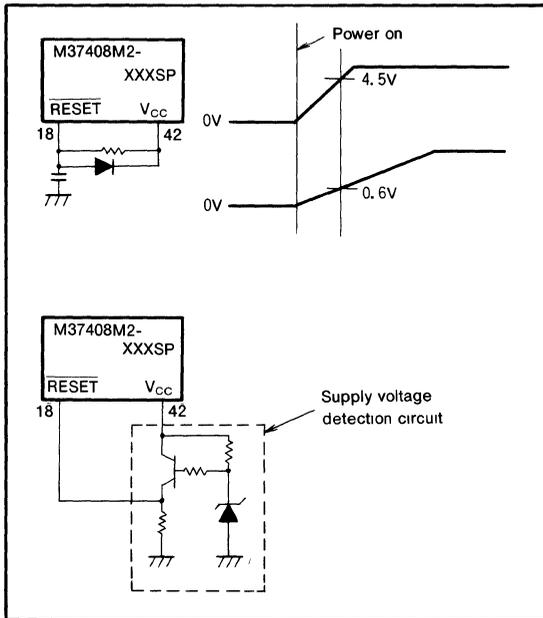


Fig. 13 Example of reset circuit

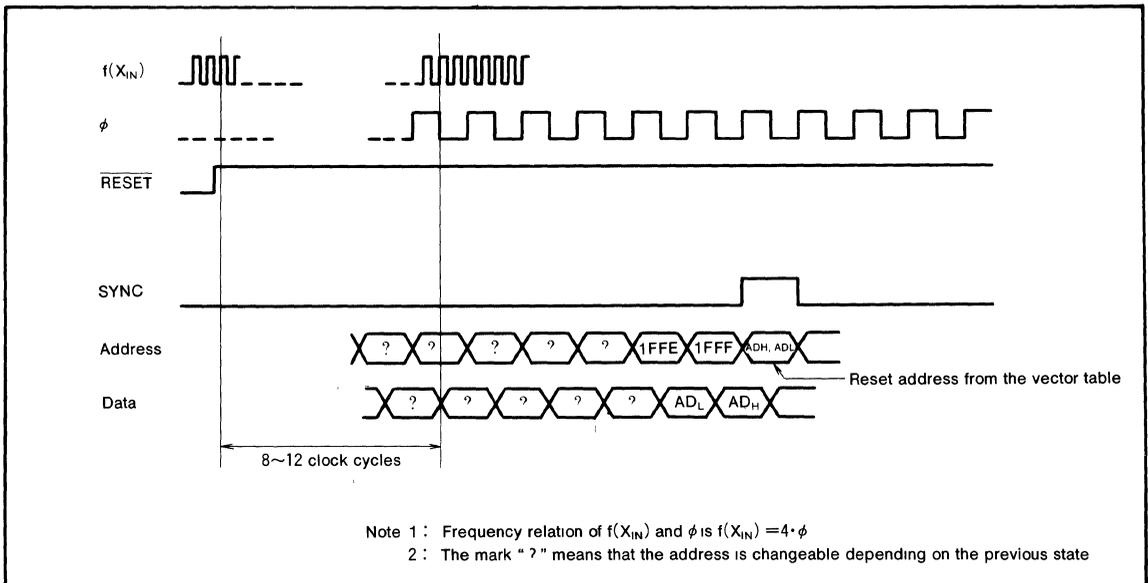


Fig.14 Timing diagram at reset

Note 1: Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN}) = 4 \cdot \phi$

2: The mark "?" means that the address is changeable depending on the previous state

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Local bus address		
(1) Port P1 directional register	(E1 ₁₆)	00 ₁₆
(2) Dual-port RAM direction specify register	(E2 ₁₆)	00 ₁₆
(3) UART status register	(ED ₁₆)	00 ₁₆
(4) UART mode register	(ED ₁₆)	0 X 0 0 0 0 0 0
(5) UART control register	(EE ₁₆)	X 0 0 0 0 0 0 0
(6) IPC error register 0	(F4 ₁₆)	00 ₁₆
(7) IPC error register 1	(F7 ₁₆)	00 ₁₆
(8) IPC semaphore register	(F9 ₁₆)	00 ₁₆
(9) Collision detect register	(FA ₁₆)	00 ₁₆
(10) Interrupt enable register	(FB ₁₆)	00 ₁₆
(11) Interrupt request register	(FC ₁₆)	00 ₁₆
(12) Prescaler X	(FD ₁₆)	FF ₁₆
(13) Timer X	(FE ₁₆)	01 ₁₆
(14) Timer control register	(FF ₁₆)	0 0 0 X X X 0 0
(15) Access flag	(D0 ₁₆ ~D7 ₁₆)	00 ₁₆
(16) Processor status register	(PS)	1
(17) Program counter	(PC _H)	Contents of address 1FFF ₁₆
	(PC _L)	Contents of address 1FFE ₁₆

Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values

Fig.15 Internal state of microcomputer at reset (1)

System bus address		
(1) Port P0 directional register	(77 ₁₆)	00 ₁₆
(2) IPC error register 0	(78 ₁₆)	00 ₁₆
(3) IPC error register 1	(7B ₁₆)	00 ₁₆
(4) Collision detect register	(7E ₁₆)	00 ₁₆
(5) IPC semaphore register	(7F ₁₆)	00 ₁₆
(6) Access flag	(50~57 ₁₆)	00 ₁₆

Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values

Fig.16 Internal state of microcomputer at reset (2)

I/O PORTS

(1) Port P0 System bus : address 76₁₆
Port P0 is an 8-bit I/O port with CMOS output. It can be accessed from system bus only and can not be accessed from local bus.

As shown in the memory map (Figure 1), port P0 can be accessed at system bus address 76₁₆. Port P0 has a directional register (address 77₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state. This port becomes input at reset.

(2) Port P1 Local bus : address 00E0₁₆
System bus : address 75₁₆

Port P1 is an 6-bit I/O port and connected to local bus. It has the same function as port P0 except the connected bus.

It's directional register is at local bus address 00E1₁₆. Also port P1 can be read from system bus but the pin state is read regardless the value of the port P1 directional register.

(3) Address pins
Address pins A₀~A₆ are the input pins directly connected to the system bus. The 7-bit address corresponding to the system bus is input to these pins. The input level is TTL.

(4) Data pins
Data pins D₀~D₇ are the output pins directly connected to the system bus. The 8-bit data corresponding to the system bus is input/output on these pins. When the \overline{CS} pin is "L" and the \overline{RD} pin is "L", the data pins become the output pins. When the \overline{CS} pin is "L" and the \overline{WR} pin is "L", the data pins become the input pins. Setting the \overline{CS} pin to "H" puts pins D₀~D₇ in the floating state. The I/O level is TTL.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

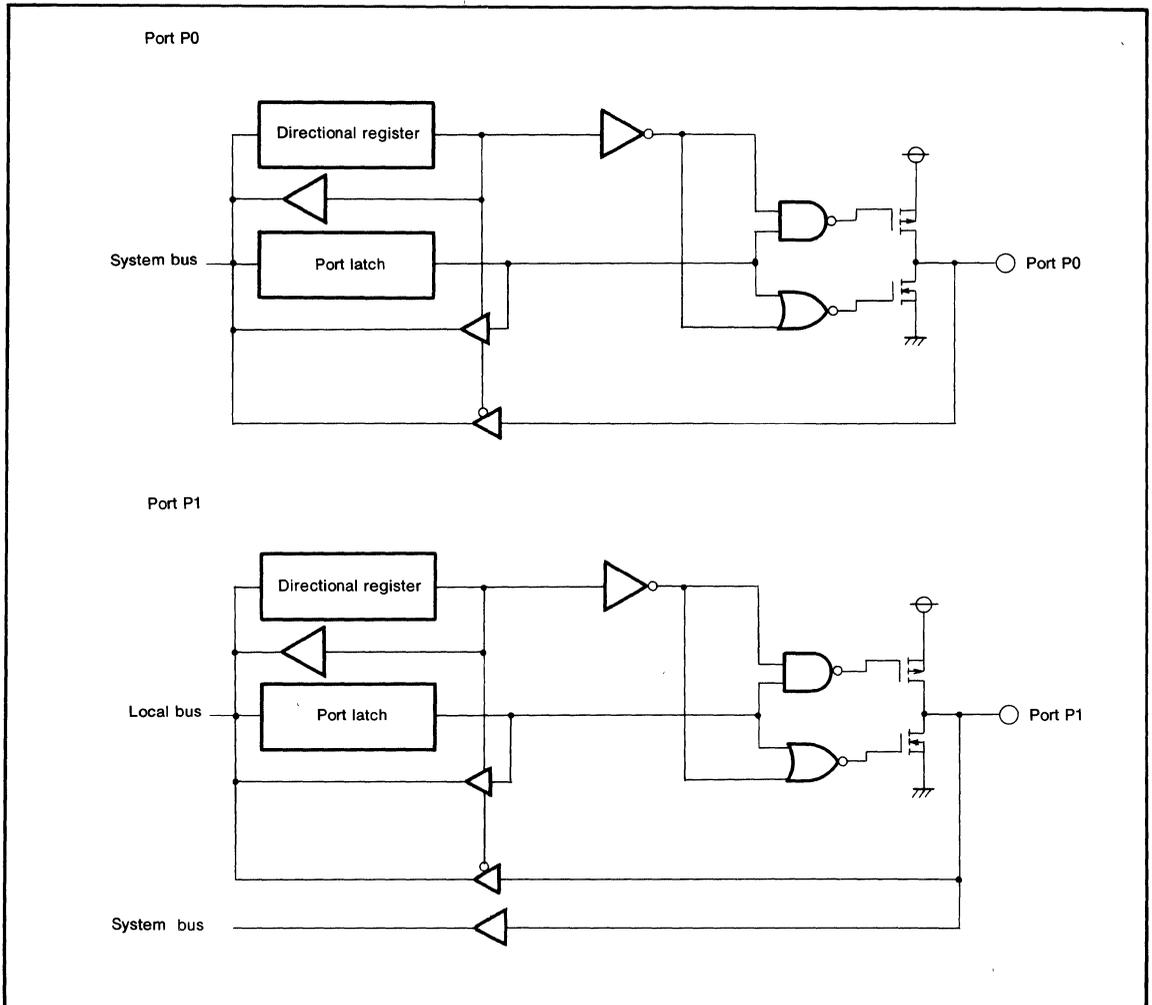


Fig. 17 Port P0, P1 block diagram

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 18.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16} , respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 19 and 20.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 21. X_{IN} is the input, and X_{OUT} is open.

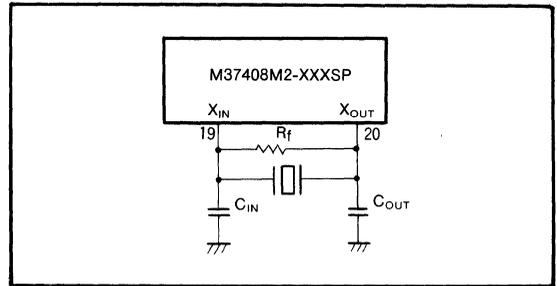


Fig. 19 External ceramic resonator circuit

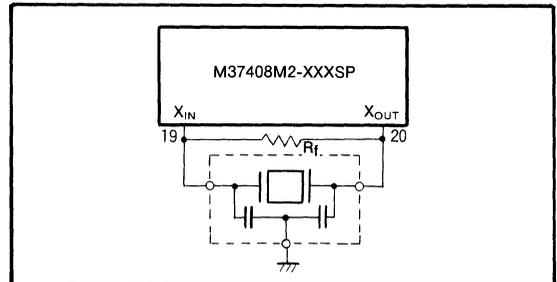


Fig. 20 External ceramic resonator circuit (capacity built-in type)

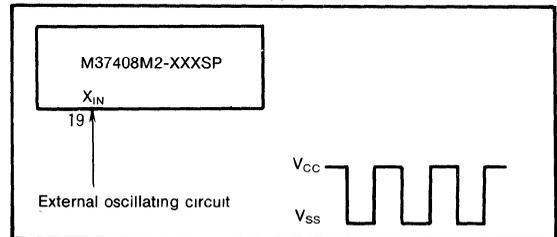


Fig. 21 External clock input circuit

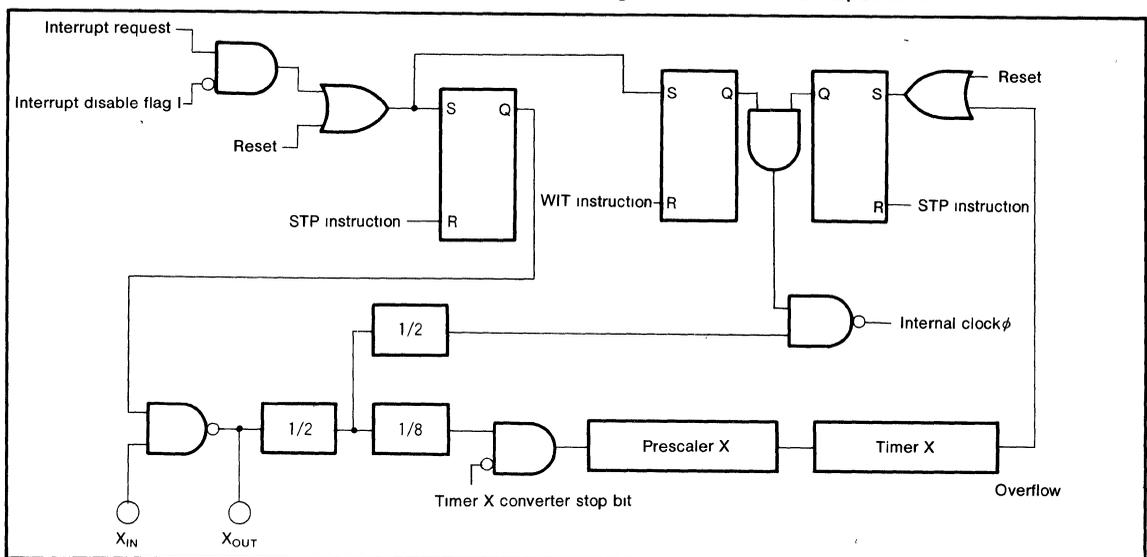


Fig. 18 Block diagram of clock generating circuit

PROGRAMMING NOTES

- (1) The frequency ratio of the timer and the prescaler is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) Change the address $A_0 \sim A_6$ input and the \overline{CS} input when both the \overline{RD} input and \overline{WR} input are "H".
- (4) Registers whose values change when read, are connected to the system bus of the M37408M2-XXXSP. If the master CPU generates an invalid read cycle, data is not correctly transferred.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (7) The STP instruction must be executed after setting timer X count enable bit to enable "0", timer X interrupt enable bit to inhibit ("0"), and timer X interrupt request bit to no request ("0").
- (8) The power current is max. 10mA in DC. However, because a rush current and a bus charge-discharge current flow transiently, a bypass capacitor must be connected between V_{SS} and V_{CC} .

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3sets

MITSUBISHI MICROCOMPUTERS M37408M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3~7	V
V_I	Input voltage, RESET, X_{IN}		-0.3~7	V
V_I	Input voltage, $P0_0\sim P0_7, P1_0\sim P1_5, D_0\sim D_7, A_0\sim A_6, RD, WR, CS, CLK, RxD, CTS$	With respect to V_{SS}	-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage, CNV_{SS}	Output transistors cut-off	-0.3~13	V
V_O	Output voltage, $P0_0\sim P0_7, P1_0\sim P1_5, X_{OUT}, \phi, D_0\sim D_7, TxD, CTS$		-0.3~ $V_{CC}+0.3$	V
P_d	Power dissipation	$T_a = 25^\circ C$	1000(Note 1)	mW
T_{opr}	Operating temperature		-10~70	$^\circ C$
T_{stg}	Storage temperature		-40~125	$^\circ C$

Note 1 : 300mW for GFP types

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $X_{IN}, RESET, CLK, P0_0\sim P0_7, P1_0\sim P1_5, RxD, CTS$	0.8 V_{CC}		$V_{CC}+0.3$	V
V_{IH}	"H" input voltage $A_0\sim A_6, D_0\sim D_7, RD, WR, CS$	2		$V_{CC}+0.3$	V
V_{IL}	"L" input voltage $P0_0\sim P0_7, P1_0\sim P1_5, CLK, RxD, CTS$	-0.3		0.2 V_{CC}	V
V_{IL}	"L" input voltage $A_0\sim A_6, D_0\sim D_7, RD, WR, CS$	-0.3		0.8	V
V_{IL}	"L" input voltage RESET	-0.3		0.12 V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	-0.3		0.16 V_{CC}	V
I_{OH}	"H" output current $P0_0\sim P0_7, P1_0\sim P1_5, \phi, TxD, CTS$			-10	mA
I_{OH}	"H" output current $D_0\sim D_7$			-1.0	mA
I_{OL}	"L" output current $P0_0\sim P0_7, P1_0\sim P1_5, \phi, TxD, CTS$			10	mA
I_{OL}	"L" output current $D_0\sim D_7$			-1.6	mA

Note 1 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms

2 : Total of $I_{OL(peak)}$ of ports $P0, P1, TxD$ and CTS is -50mA

Total of $I_{OH(peak)}$ of ports $P0, P1, TxD$ and CTS is 50mA

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V, V_{SS} = 0V, T_a = 25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V_{OH}	"H" output voltage $P0_0\sim P0_7, P1_0\sim P1_5, \phi, TxD, CTS$	$I_{OH} = -10mA$	$V_{CC}-2$			V	
V_{OH}	"H" output voltage $D_0\sim D_7$	$I_{OH} = -1mA$	2.4			V	
V_{OL}	"L" output voltage $P0_0\sim P0_7, P1_0\sim P1_5, \phi, TxD, CTS$	$I_{OL} = 10mA$			2	V	
V_{OL}	"L" output voltage $D_0\sim D_7$	$I_{OL} = 1.6mA$			0.4	V	
I_I	Input leak current $A_0\sim A_6, RD, WR, CS, CLK$	$V_{SS} \leq V_I \leq V_{CC}$	-5		5	μA	
I_I	Input leak current RESET, X_{IN}	$V_{SS} \leq V_I \leq 7V$	-5		5	μA	
I_{OZ}	Tri-state leak current $P0_0\sim P0_7, P1_0\sim P1_5, D_0\sim D_7, CTS$	$V_{SS}+0.5 \leq V_O \leq V_{CC}-0.5V$	-5		5	μA	
$V_{T+} - V_{T-}$	Hysteresis RESET, CLK, RxD, CTS			0.6		V	
I_{CC}	Supply current	Output terminals are opened, others to V_{SS} , $CNV_{SS} = V_{CC}$			10	mA	
							$f(X_{IN}) = 10MHz$ Square wave
							ditto (wait mode)
							At stop mode $T_a = 25^\circ C$
					1	μA	
					10		

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMING REQUIREMENTS

System bus ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-10 \sim 70^\circ C$, $f(X_{IN})=10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(A-WR)}$	$A_0 \sim A_6$ CS input set-up time	Fig. 22	50			ns
$t_{SU(A-RD)}$	$A_0 \sim A_6$ CS input set-up time		50			ns
$t_{SU(D-WR)}$	$D_0 \sim D_7$ input set-up time		80			ns
$t_H(WR-A)$	$A_0 \sim A_6$ CS input hold time		0			ns
$t_H(RD-A)$	$A_0 \sim A_6$ CS input hold time		0			ns
$t_H(WR-D)$	$D_0 \sim D_7$ input hold time		10			ns
$t_W(WR)$	WR input "L" pulse width		200			ns
$t_W(RD)$	RD input "L" pulse width		200			ns

Local bus ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-10 \sim 70^\circ C$, $f(X_{IN})=10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
$t_{SU(P1-\phi)}$	$P1_0 \sim P1_5$ input set-up time	Fig. 22	300			ns
$t_H(\phi-P1)$	$P1_0 \sim P1_5$ input hold time		50			ns

SWITCHING CHARACTERISTICS

System bus ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-10 \sim 70^\circ C$, $f(X_{IN})=10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
$t_d(D-RD)$	$D_0 \sim D_7$ output delay time	Fig. 22			150	ns
$t_v(D-RD)$	$D_0 \sim D_7$ output effective time		0			ns
$t_{en}(RD-D)$	$D_0 \sim D_7$ output enable time		10			ns
$t_{dis}(RD-D)$	$D_0 \sim D_7$ output disable time				50	ns

Local bus ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-10 \sim 70^\circ C$, $f(X_{IN})=10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
$t_d(\phi-P1)$	$P1_0 \sim P1_5$ output delay time	Fig. 22			300	ns

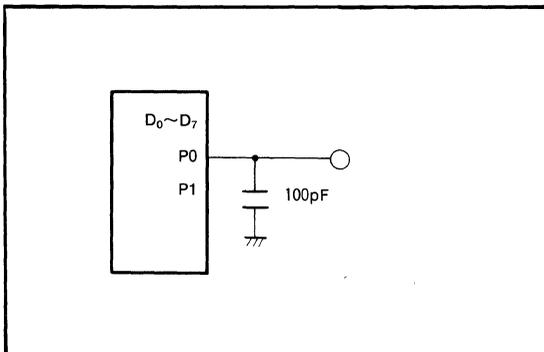
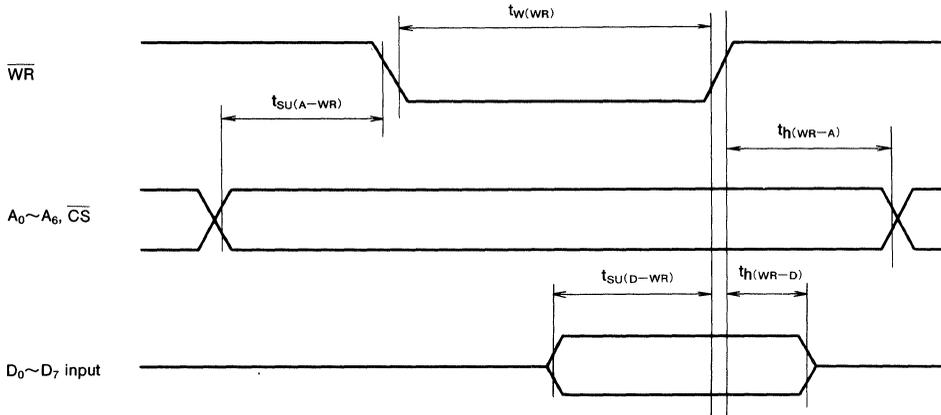


Fig. 22 Port P0, P1, $D_0 \sim D_7$ test circuit

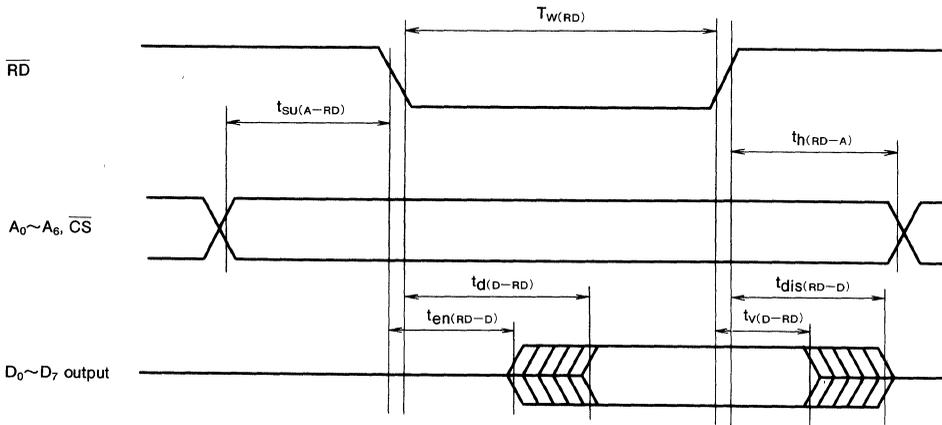
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMING DIAGRAMS

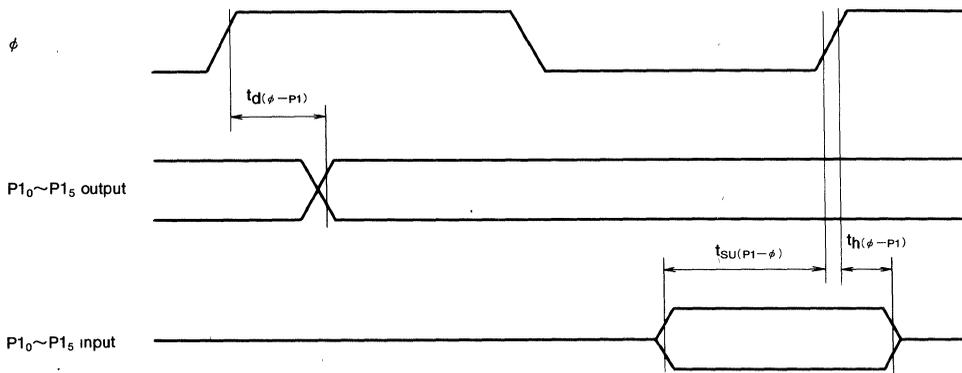
System bus write cycle



System bus read cycle



Local bus



MITSUBISHI MICROCOMPUTERS M37409M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37409M2-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for the communication application used as a slave-microcomputer. In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37409M2-XXXSP and the M37409M2-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

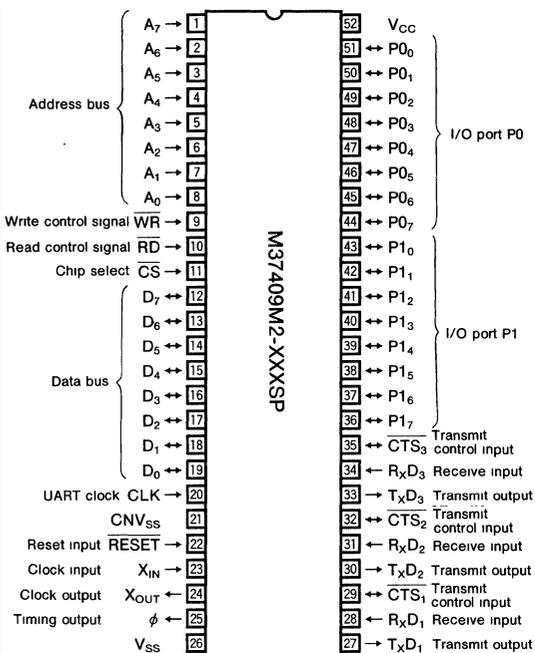
FEATURES

- Number of basic instructions..... 69
- Memory size ROM..... 4096 bytes
RAM..... 128 bytes
- Instruction execution time
... 0.8 μ s (minimum instructions at 10MHz frequency)
- Single power supply $f(X_{IN})=10\text{MHz}$ 5V \pm 10%
- Power dissipation
normal operation mode (at 10MHz frequency) .. 50mW
- Subroutine nesting..... 64 levels (Max.)
- Interrupt..... 10 types
- 8-bit timer..... 1
- UART (Full-duplex)..... 3 channels
- Dual-port RAM..... 192 bytes
- Communication registers
Access flag..... 192 bits
Collision detect register..... 8-bit \times 1
IPC* semaphore register..... 7-bit \times 1
IPC mode register..... 8-bit \times 4
IPC error register..... 8-bit \times 4
- Programmable I/O ports
(Ports P0, P1, CTS₁~CTS₃)..... 19
- Bus interface
Address bus..... 8
Data bus..... 8
Control signal (WR, RD, CS)..... 3

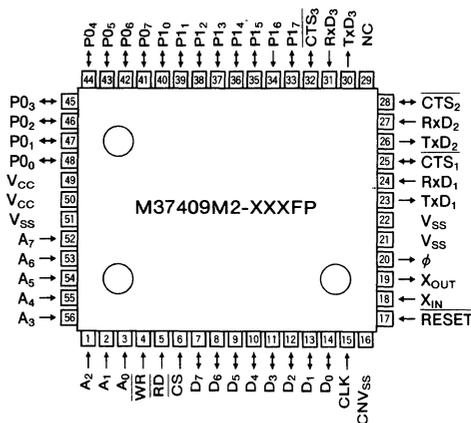
APPLICATION

Office automation equipment

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

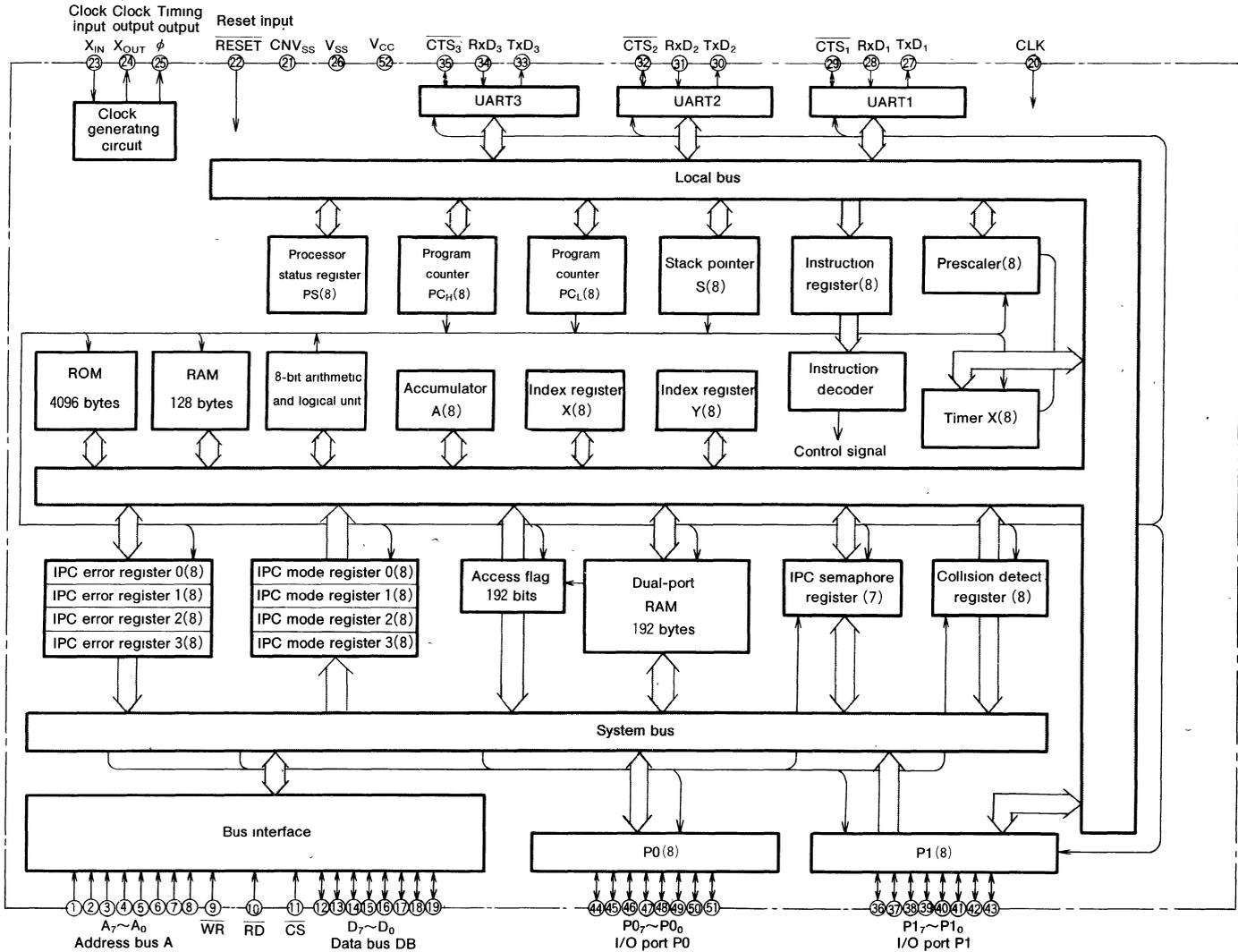


Outline 56P6N

NC : No connection

* IPC...Intelligent Protocol Controller

M37409M2-XXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

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M37409M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37409M2-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			0.8 μ s (minimum instructions, at 10MHz frequency)
Clock frequency			10MHz
Memory size	ROM		4096 bytes
	RAM		128 bytes
Input/Output ports	P0 ₀ ~P0 ₇	I/O	8-bit×1 (System bus I/O)
	P1 ₀ ~P1 ₇	I/O	8-bit×1 (Local bus I/O, System bus input)
	CTS ₁ ~CTS ₃	I/O	1-bit×3 (Common with UART transmit control input)
Bus interface	A ₀ ~A ₇	Input	8-bit×1
	D ₀ ~D ₇	I/O	8-bit×1
	RD, WR, CS	Input	1-bit×3
UART			3 (with programmable baud rate generator)
Timer			8-bit×1 (with 8-bit prescaler)
Interrupt			System bus (IPCM0) interrupt 1, UART interrupt 6, Timer interrupt 1, Collision interrupt 1
Dual-port RAM			192 bytes
Communication registers	Access flag		192 bits
	Collision detect register		8-bit×1
	IPC semaphore register		7-bit×1
	IPC mode register		8-bit×4
	IPC error register		8-bit×4
Subroutine nesting			64 levels (max.)
Clock generating circuit			Built-in (externally connected ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at operation		50mW
	at wait mode		5mW
	at stop mode	T _a =25°C	0.05mW
		T _a =70°C	0.5mW
Operating temperature range			-10~70°C
Device structure			CMOS silicon gate process
Package	M37409M2-XXXSP		52-pin shrink plastic molded DIP
	M37409M2-XXXFP		56-pin plastic molded QFP

MITSUBISHI MICROCOMPUTERS M37409M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} , V_{SS}	Supply voltage		Power supply inputs $5V \pm 10\%$ to V_{CC} , and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}
\overline{RESET}	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than $2\mu s$ (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin
$P0_0 \sim P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output. This port is connected to the system bus only, and can not be accessed from the local bus. At reset this port becomes input mode. The output structure is CMOS output.
$P1_0 \sim P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. This port is connected to the local bus and can be used as only input port from the system bus. The output structure is CMOS output.
TxD_1 $\sim TxD_3$	UART transfer output	Output	These are UART transfer data output pins
RxD_1 $\sim RxD_3$	UART receive input	Input	These are UART receive data input pins
\overline{CTS}_1 $\sim \overline{CTS}_3$	UART transfer control input	I/O	These are UART transfer control signal input pins and can be used as I/O port which have basically same function as port P1.
CLK	UART clock input	Input	This port is an external clock input pin for baud rate
$A_0 \sim A_7$	Address input	Input	This port is input for system address
$D_0 \sim D_7$	Data input/output	I/O	This port is input or output the system data
\overline{CS}	Chip select	Input	System data can be read or written by inputting "L" to this port
\overline{RD}	Read control input	Input	Memory or register data specified by $A_0 \sim A_7$ is read from $D_0 \sim D_7$ by inputting "L" to this port
\overline{WR}	Write control input	Input	Data input from $D_0 \sim D_7$ is written to memory or register specified by $A_0 \sim A_7$ by inputting "L" to this port

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37409 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

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ADDRESS AREA

M37409M2-XXXSP has two buses; the local bus connected to the CPU of its own, and the system bus connected to the CPU of the external master computer. There are two corresponding address area.

The local bus has thirteen address buses and eight data buses. The address area, which is 8192 bytes, is addresses from 0000_{16} to $1FFF_{16}$.

For this local bus area, addresses 1000_{16} to $1FFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes.

The system bus has eight address buses and eight data buses. The address area, which is 256 bytes, is addresses from 00_{16} to FF_{16} .

The internal memories and registers are connected to one or both of these buses. Therefore, it is necessary, in writing programs, to know the operation of each functional block as well as to which bus the memories and registers are connected at what addresses.

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

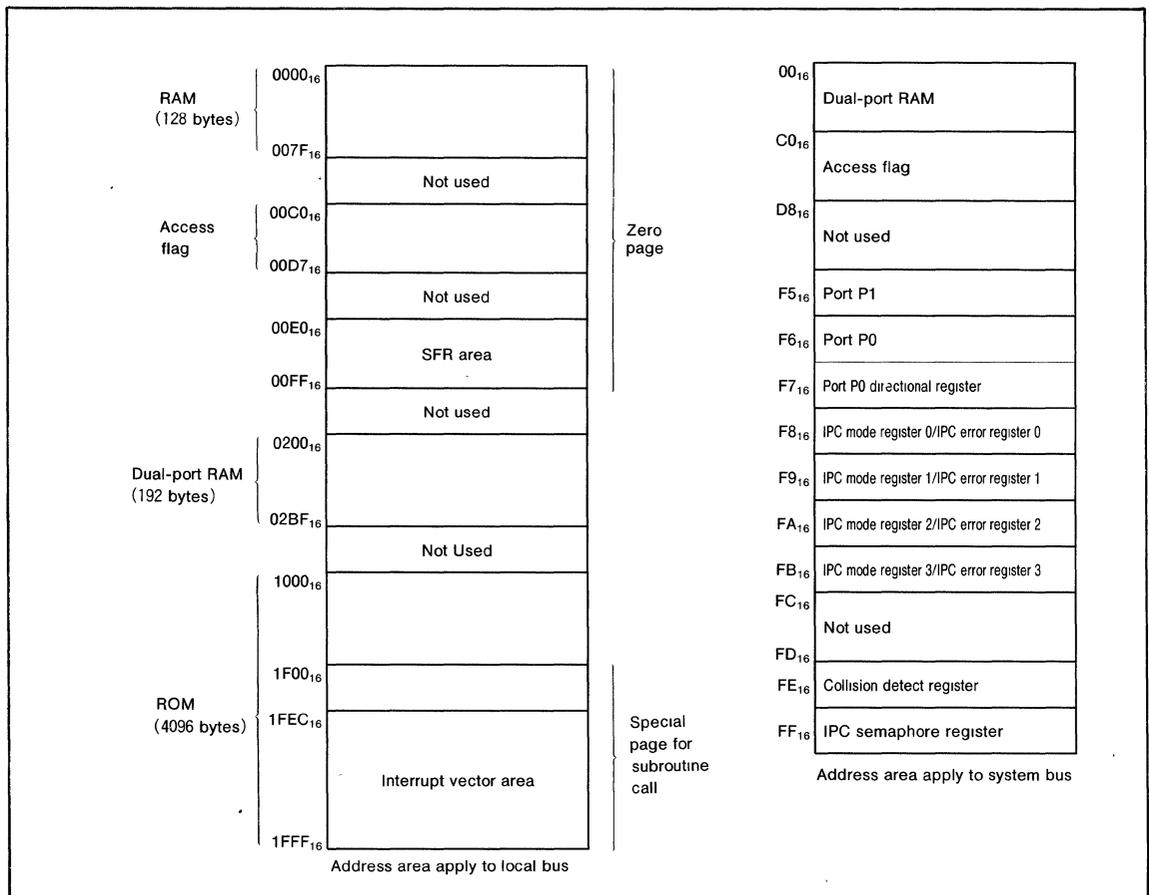


Fig. 1 Memory map

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00E0 ₁₆	Port P1	00F0 ₁₆	IPC mode register 0
00E1 ₁₆	Port P1 directional register	00F1 ₁₆	IPC mode register 1
00E2 ₁₆	Dual-port RAM direction specify register	00F2 ₁₆	IPC mode register 2
00E3 ₁₆		00F3 ₁₆	IPC mode register 3
00E4 ₁₆	UART1 receive/transfer buffer register	00F4 ₁₆	IPC error register 0
00E5 ₁₆	UART1 status register/UART1 mode register	00F5 ₁₆	IPC error register 1
00E6 ₁₆	UART1 control register	00F6 ₁₆	IPC error register 2
00E7 ₁₆	UART1 divider for baud rate generate	00F7 ₁₆	IPC error register 3
00E8 ₁₆	UART2 receive/transfer buffer register	00F8 ₁₆	
00E9 ₁₆	UART2 status register/UART2 mode register	00F9 ₁₆	IPC semaphore register
00EA ₁₆	UART2 control register	00FA ₁₆	Collision detect register
00EB ₁₆	UART2 divider for baud rate generate	00FB ₁₆	Interrupt enable register
00EC ₁₆	UART3 receive/transfer buffer register	00FC ₁₆	Interrupt request register
00ED ₁₆	UART3 status register/UART3 mode register	00FD ₁₆	Prescaler X
00EE ₁₆	UART3 control register	00FE ₁₆	Timer X
00EF ₁₆	UART3 divider for baud rate generate	00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

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Bus Interface

M37409M2-XXXSP has the bus interface to operate itself by the control signal sent from the master CPU. The master CPU can access the memories and registers located in the system address area described below via this bus interface. The bus interface has address pins A_0 to A_7 , data pins D_0 to D_7 , and three controls signals \overline{CS} , \overline{WR} , and \overline{RD} which can be directly connected to TTL.

Driving the \overline{CS} pin to "L" put this microcomputer in the read/write enabled state. When writing data from the mas-

ter CPU, specify the address by $A_0 \sim A_7$ and set \overline{WR} to "L", and the data at $D_0 \sim D_7$ is written to the specified address. When reading data, specify the address by $A_0 \sim A_7$ and set \overline{RD} to "L", and the contents of the specified address are output to $D_0 \sim D_7$.

Driving the \overline{CS} pin to "H" puts the M37409M2-XXXSP in the state which does not allow the read and write operations from the master CPU. At this time, the outputs of D_0 to D_7 are in the floating state.

Figure 3 shows the block diagram of the bus interface.

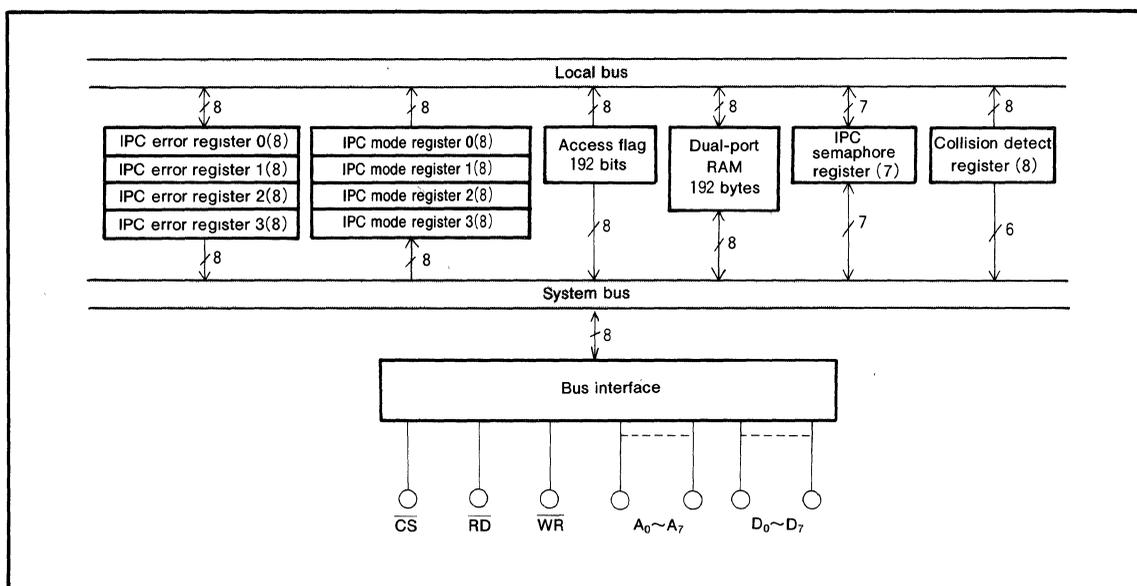


Fig. 3 Block diagram of bus interface

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Dual-port RAM

The dual-port RAM, which is 192 bytes, is the memory which allows the read/write operation from both the local and system buses independently. From the local bus, it is allocated at addresses 0200₁₆ to 02BF₁₆; from the system bus, addresses 00₁₆ to BF₁₆. Table 1 shows the result when the write and read operations from both buses compete at the same address.

Table 1. Result obtained by simultaneously accessing the same address from the system and local buses

	Write	Read
Simultaneous read from both buses	—	Correct data
Simultaneous write from both buses	Unpredictable	—
Read from one bus, write from the other	Correct data	Uncertain

[Access flag]

Local bus : address 00C0₁₆~00D7₁₆
System bus : address C0₁₆~D7₁₆

The access flag arbitrates the access to the dual-port RAM. One bit of access flag is allocated to one byte of dual port RAM, amounting 192 bits (24 bytes) in total. The access flag can be read from both the system and local buses. Figure 4 shows the relationship between each byte of the dual port RAM and each bit of the access flag. Each bit is cleared to "0" when an access to read is made to the dual port RAM from either bus, it is set to "1" when an access to write is made. If an access to read from one bus and an access to write from the other compete at the same address of the dual port RAM, the values of the corresponding access flags are uncertain. At reset, all access flags are cleared to "0".

[Dual-port RAM direction specify register]

Local bus : address 00E2₁₆

This register specifies that the read operation of which bus clears each bit of the access flag. One bit of this register corresponds to 32 bytes of the dual-port RAM (32 bits of the access flag). This register consists of six bits. Each access flag is cleared by the read operation from the system bus when the corresponding dual-port RAM direction specify register is "0"; when it is "1", each access flag is cleared by the read operation from the local bus. As for a write operation, the access flag is set regardless of which bus has made it. Table 2 shows the relationship between each bit of the dual-port RAM direction specify register and the dual-port RAM and the access flag. At reset, all bits are cleared to "0".

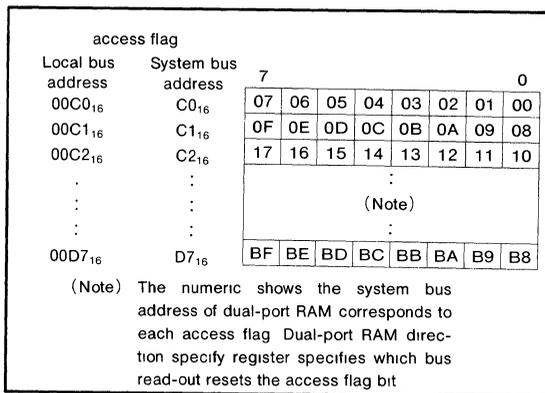


Fig. 4 Correspondence between each byte of dual-port RAM and each bit of access flag

Table 2. Correspondence among each bit of dual-port RAM direction specify register, dual-port RAM and access flag

Dual-port RAM direction specify register	Dual-port RAM		Access flag	
	Local bus address	System bus address	Local bus address	System bus address
bit 0	0200 ₁₆ ~021F ₁₆	00 ₁₆ ~1F ₁₆	00C0 ₁₆ ~00C3 ₁₆	C0 ₁₆ ~C3 ₁₆
bit 1	0220 ₁₆ ~023F ₁₆	20 ₁₆ ~3F ₁₆	00C4 ₁₆ ~00C7 ₁₆	C4 ₁₆ ~C7 ₁₆
bit 2	0240 ₁₆ ~025F ₁₆	40 ₁₆ ~5F ₁₆	00C8 ₁₆ ~00CB ₁₆	C8 ₁₆ ~CB ₁₆
bit 3	0260 ₁₆ ~027F ₁₆	60 ₁₆ ~7F ₁₆	00CC ₁₆ ~00CF ₁₆	CC ₁₆ ~CF ₁₆
bit 4	0280 ₁₆ ~029F ₁₆	80 ₁₆ ~9F ₁₆	00D0 ₁₆ ~00D3 ₁₆	D0 ₁₆ ~D3 ₁₆
bit 5	02A0 ₁₆ ~02BF ₁₆	A0 ₁₆ ~BF ₁₆	00D4 ₁₆ ~00D7 ₁₆	D4 ₁₆ ~D7 ₁₆

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[IPC mode register, IPC error register]

Local bus : address 00F0₁₆~00F7₁₆

System bus : address F8₁₆~FB₁₆

IPC mode registers 0~3 (IPCM0~IPCM3) and IPC error registers 0~3 (ERR0~ERR3) are the 8-bit registers which can be set by the user without restriction. IPC mode registers 0~3 are used to specify the mode setting such as UART from the external master CPU via the system bus. IPC error registers 0~3 are used to indicate the error found on the local CPU to the outside via the system bus. On the system bus, IPC mode registers 0~3 and IPC error registers 0~3 share four bytes of the same address, with the former being for write only and the latter for read only. On the local bus, the former is for read only and the latter is for both read and write.

The data written from the system bus to IPC mode registers 0~3 can be read from the local bus only. If an access to read or write is performed from the system bus on IPC mode register 0/IPC error register 0, an interrupt request (IPCM0) is caused.

When IPC error registers 0~3 are accessed for read from the system bus, only the bits which are found "1" are reset by hardware. When these registers are read from the local bus, their values remain unchanged.

[IPC semaphore register]

Local bus : address 00F9₁₆

System bus : address FF₁₆

This register is for handshaking with the master CPU and consists of block semaphore flags (BS0~BS5) and the ready flag (RDY). BS0~BS5 can be read/written from both the local and system buses. RDY can be read/written from the local bus and read only from the system bus. With this register, all bits can be read at a time but, in a write operation, only one bit can be written at a time. The low-order three bits of the data to be written are used to specify to which register bit the data is to be written. Bit 7 is used to specify whether to write "1" or "0". At reset, all bits are cleared to "0".

RDY is cleared to "0" also when an access to write is performed by the system bus on IPC mode register 0.

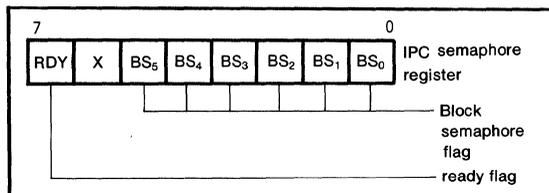


Fig. 5 Bit structure of IPC semaphore register

[Collision detect register]

Local bus : address 00FA₁₆

System bus : address FE₁₆

This register consists of six bits of collision detect flags (CD₀~CD₅), the collision interrupt enable bit, and collision interrupt request bit. The collision detect flags are set when an access to read is performed by the system bus on the same address on the dual port RAM to which the local bus is writing data. These flags indicate that the data read by the master CPU may be incorrect. When these flags are set, a collision detect interrupt request occurs.

Each collision flag corresponds to each 32 bits of the dual port RAM. The flag bit corresponding to the address at which access competition occurred is set. The relationship between the flag bits and the dual port RAM is shown in Table 3. These flags can be read from both buses. All bits are cleared when read from the system bus or at reset.

The collision interrupt enable bit can be read/written from the local bus. When it is read from the system bus, "0" is always output. The collision interrupt request bit can be read only from the local bus. Only "0" can be written.

Table 3. Correspondence between collision detect flag and dual-port RAM

Collision detect flag	Dual-port RAM	
	Local bus address	System bus address
CD ₀	0200 ₁₆ ~021F ₁₆	00 ₁₆ ~1F ₁₆
CD ₁	0220 ₁₆ ~023F ₁₆	20 ₁₆ ~3F ₁₆
CD ₂	0240 ₁₆ ~025F ₁₆	40 ₁₆ ~5F ₁₆
CD ₃	0260 ₁₆ ~027F ₁₆	60 ₁₆ ~7F ₁₆
CD ₄	0280 ₁₆ ~029F ₁₆	80 ₁₆ ~9F ₁₆
CD ₅	02A0 ₁₆ ~02BF ₁₆	A0 ₁₆ ~BF ₁₆

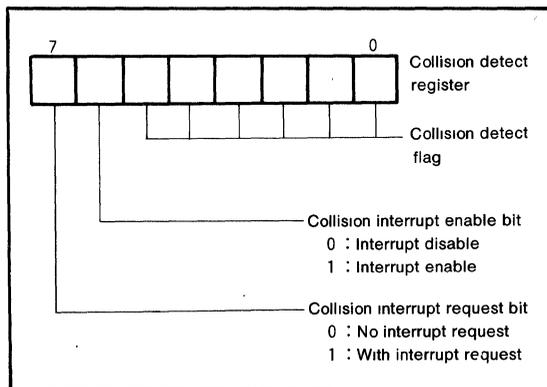


Fig. 6 Structure of collision detect register

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INTERRUPT

Interrupts can be caused by 10 different events.

Interrupts are vectored interrupts with priorities shown in Table 4. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit bit is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 7 shows interrupts control.

All interrupt request bits except the collision detect interrupt are in the interrupt request register (address 00FC₁₆). The collision detect interrupt request bit is in the collision detect register (address 00FA₁₆). The interrupt request bit is set when the following conditions occur:

- (1) When the data is set to receive buffer of UART1, UART2, or UART3
- (2) When the master CPU accesses the IPC mode/IPC error register 0 through bus interface
- (3) When the contents of the timer X goes to "0"
- (4) When one of the bit 0~bit 5 of the collision detect register is set to "1"
- (5) When the data is set to transmit buffer of UART1, UART2, or UART3

There are two interrupt enable bits for each interrupt except collision detect interrupt. One is in interrupt enable register (address 00FB₁₆), the other is in UART1, UART2, UART3 control register (address 00E6₁₆, 00EA₁₆, 00EE₁₆) or timer control register (address 00FF₁₆). Interrupts are become enable when these two enable bits are both "1". The collision interrupt enable bit is in bit 6 of collision detect register.

UART transmit interrupt is controlled by $\overline{CTS_1}$, $\overline{CTS_2}$ or $\overline{CTS_3}$ function select bit and CTS₁, CTS₂ or CTS₃ pin input (see UART section).

Since the BRK instruction interrupt and the UART3 transmit interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if UART3 transmit generated the interrupt.

Table 4. Interrupt vector address and priority

Interrupt	Priority	Vector addresses
RESET	1	1FFF ₁₆ , 1FFE ₁₆
UART1 receive	2	1FFD ₁₆ , 1FFC ₁₆
UART2 receive	3	1FFB ₁₆ , 1FFA ₁₆
UART3 receive	4	1FF9 ₁₆ , 1FF8 ₁₆
IPCM0	5	1FF7 ₁₆ , 1FF6 ₁₆
Timer X	6	1FF5 ₁₆ , 1FF4 ₁₆
Collision detect	7	1FF3 ₁₆ , 1FF2 ₁₆
UART1 transmit	8	1FF1 ₁₆ , 1FF0 ₁₆
UART2 transmit	9	1FEF ₁₆ , 1FEE ₁₆
UART3 transmit/ BRK instruction	10	1FED ₁₆ , 1FEC ₁₆

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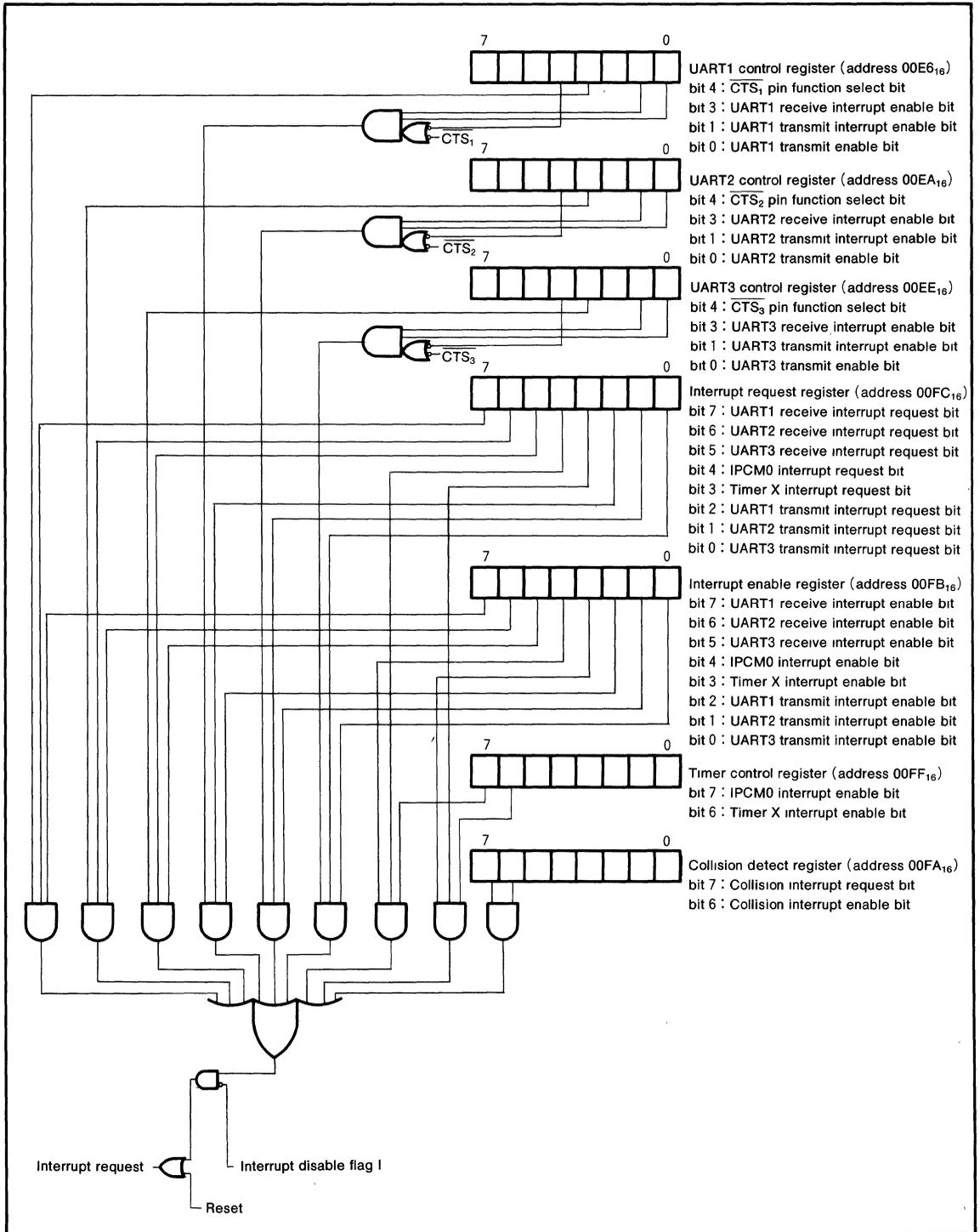


Fig. 7 Interrupt control

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TIMER

The M37409M2-XXXSP has one timer: timer X. It has an 8-bit prescaler. Each timer or prescaler is structured with 8-bit counter. A block diagram of timer X is shown in Figure 9. Timer or prescaler is a down-counter which is reloaded from the latch when the next clock pulse after the timer reaches zero. The division ratio is defined as $1/(n+1)$ where n is the decimal contents of the timer latch. The timer interrupt request bit (bit 3 of the address $00FC_{16}$ of local address bus) is also set to "1" at this time. Timer counts the oscillation frequency divided by 16 when the bit 5 of timer control register is "0", and stops when "1". The structure of the timer control register is shown in Figure 8.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16} , respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. For more details on the STP instruction, refer to the oscillation circuit section.

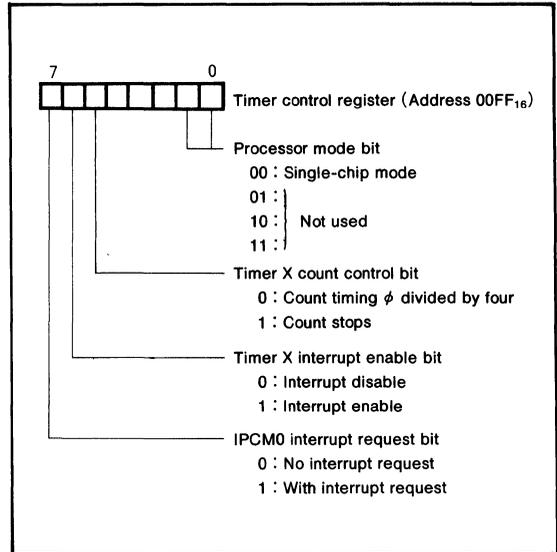


Fig. 8 Structure of timer control register

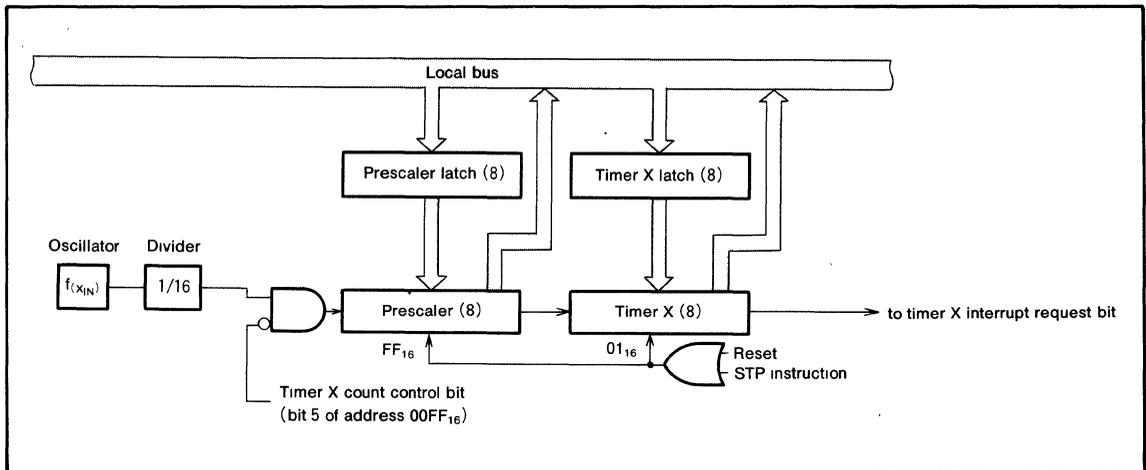


Fig. 9 Timer X block diagram

UART

The M37409M2-XXXSP contains three channels of UART's (UART_i(i=1, 2, 3)). Functionally, they are all equal and can be separately operated. Each channel has three pins (TxDi (transmit output), RxDi (receive input), and $\overline{\text{CTS}}_i$ (clear to send) and contains the receive (transmit) shift register, the receive (transmit) buffer register, the UART_i mode register, the UART_i control register, the UART_i status register, and the baud rate generating divider. It also has a CLK pin (the input pin of the external clock for baud rate generation) which is shared by three channels. An interrupt can be generated on each channel at receive and transmit independently. Figure 10 shows the UART_i block diagram. Because the differences between the channels are only pin numbers and internal addresses, the following description uses UART1 for reference.

[Receive operation]

Setting the receive enable bit (bit 2 of the UART1 control register) to "1" puts the system in the receive enable state. When there is no input of receive data, "H" is input to RxD₁ pin. When the falling edge is input to RxD₁ pin and "L" input is detected twice consecutively by sampling with the clock having a frequency 16 times the baud rate, the start bit is triggered. Then, sampling is performed three times in the middle of the start bit. When "L" is detected twice or more, the receive operation begins, capturing the data bits into the receive shift register. If "L" has not been detected twice or more, start bit detection begins again. When the data bits and parity bit have been captured into the receive shift register and the stop bit is detected, the receive data is transferred from the receive shift register to the receive buffer register, setting the receiver ready flag (bit 1 of the UART1 status register). If a parity error occurred, the parity error flag is set. The framing error flag is set when the first stop bit is found "L". If the previous data has not been read out of the receive buffer register, the overrun error flag is set, clearing the previous data. The receiver ready flag is reset when the receive buffer register is read. Each error flag can be reset by writing "1" to the error flag reset bit (bit 7 of the UART1 control register). Any of these errors does not affect the receive operation. The data bit, the parity bit, and the stop bit are sampled three times in the middle of them, each. When "L" or "H" is detected twice or more, "0" or "1" is determined respectively.

Each time a receive operation has been completed, setting the receiver ready flag, the UART1 receive interrupt request bit (bit 7 of the interrupt request register) is set. An interrupt is acknowledged when the two UART1 receive interrupt enable bits (bit 3 of the UART1 control register and bit 7 of the interrupt enable register) are both "1", and the interrupt disable flag I is "0". The UART1 receive interrupt request bit is reset when a UART1 receive interrupt is acknowledged.

Setting the receive enable bit (bit 2 of the UART1 control register) to "0" puts the system in the receive stopped state. At this time, the receiver ready flag is "0" (ready), the receive shift register is in the stopped state, and the start bit detection is stopped.

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[Transmit operation]

When the send data is written to the transmit buffer register, the start bit, parity bit, and stop bit are added to the data, which is transferred to the transmit shift register. The transmit shift register begins shift when it becomes enable for transmission, sending the serial data to TxD_i pin. For the description of the transmit enable state, see Table 5.

In the transmit enable state, each time transmission of the stop bit of the serial data being transmitted has been completed, it is checked whether the next data has been written to the transmit buffer register. If the data is found written, transmission of the next data begins. If the data is found not written, TxD_i pin is held at "H" until the next transmit data is written, setting the transmitter empty flag.

When the transmit enable state is cleared during transmission, the transmission is stopped after completing the transmission of the transmit data so far written to the transmit buffer register.

When the transmitter ready flag (bit 0 of the UART1 status register) is "1", it indicates that the transmit buffer is ready

for writing data. The immediately preceding data is transferred from the transmit buffer register to the transmit shift register. Every time the start bit is output from TxD_i pin, this flag is set. Every time the transmitter ready flag is set, the UART1 transmit interrupt request bit (bit 2 of the interrupt request register) is set. An interrupt is acknowledged when two UART1 transmit interrupt enable bits (bit 3 of the UART1 control register and bit 2 of the interrupt enable register) are both "1" and the interrupt disable flag 1 is "0". Note that an interrupt occurs only in the transmit ready state.

Bit 6 of the UART1 control register initializes the UART1 transmit side. When this bit "0", the transmit side is in the initial state.

Table 5. Bit and pin states when transmission is enable

TE _i	CTSE _i	CTS _i	
1	0	X	TE _i : UART1 transmit enable bit
	1	L	CTSE _i : CTS _i pin function selection bit CTS _i : CTS _i pin input level

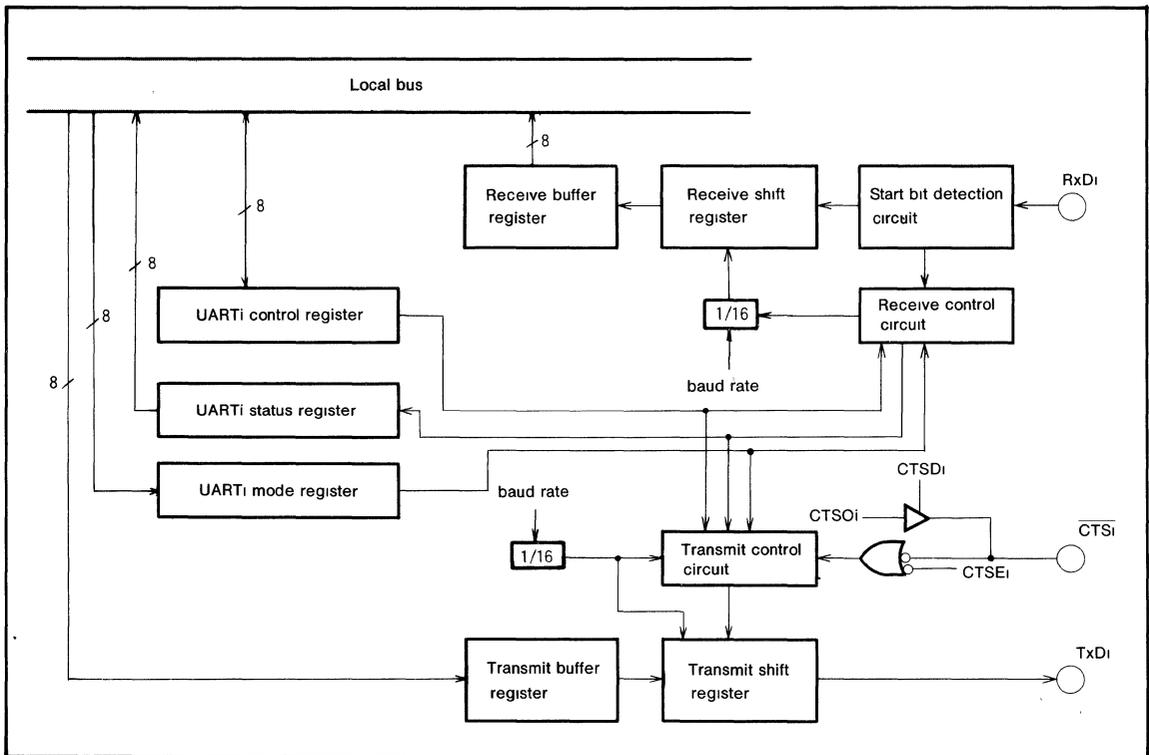


Fig. 10 UARTi block diagram

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[UARTi divider for baud rate generator]

This is an 8-bit programmable divider which generates the baud rate for the UARTi receive or transmit operation.

When the setting value is N_{BR} (0 to 255), the divide ratio becomes $1/(N_{BR} + 1)$. There are three count sources; X_{IN} clock divided by 2, X_{IN} clock divided by 32, and the external clock. Choose sources by bits 4 and 5 of the UARTi mode register. Table 6 shows the baud rate calculation for each bit combination.

When the external clock is used, the frequency of the input clock must be below 1.6MHz. Writing to the baud rate generating divider must be performed when bits 2 and 6 of the UARTi control register are both "0".

Table 6. Baud rate calculation

EX_i	BR_i	Calculation
0	0	$\text{baud rate (bps)} = \frac{f(X_{IN})}{32(N_{BR}+1)}$
0	1	$\text{baud rate (bps)} = \frac{f(X_{IN})}{512(N_{BR}+1)}$
1	X	$\text{baud rate (bps)} = \frac{f(CLK)}{16(N_{BR}+1)}$

EX_i : Clock selection bit for baud rate generator

BR_i : Divide ratio selection bit for baud rate generator

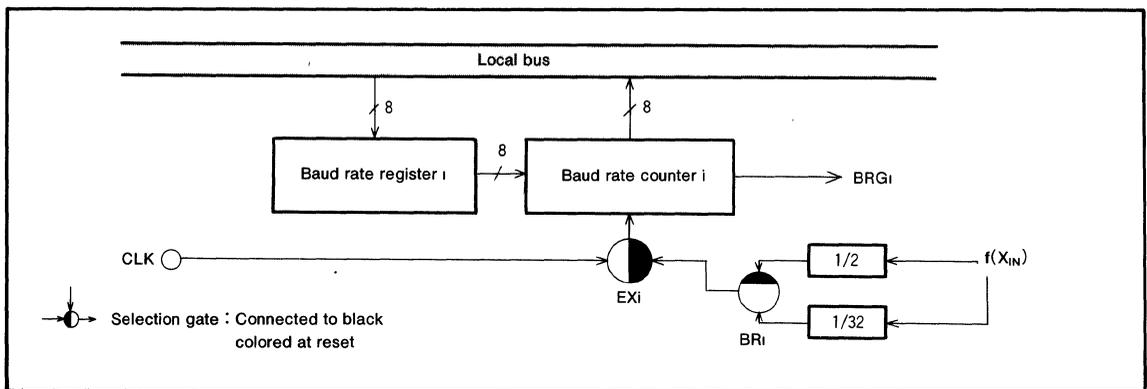


Fig. 11 Baud rate generating circuit

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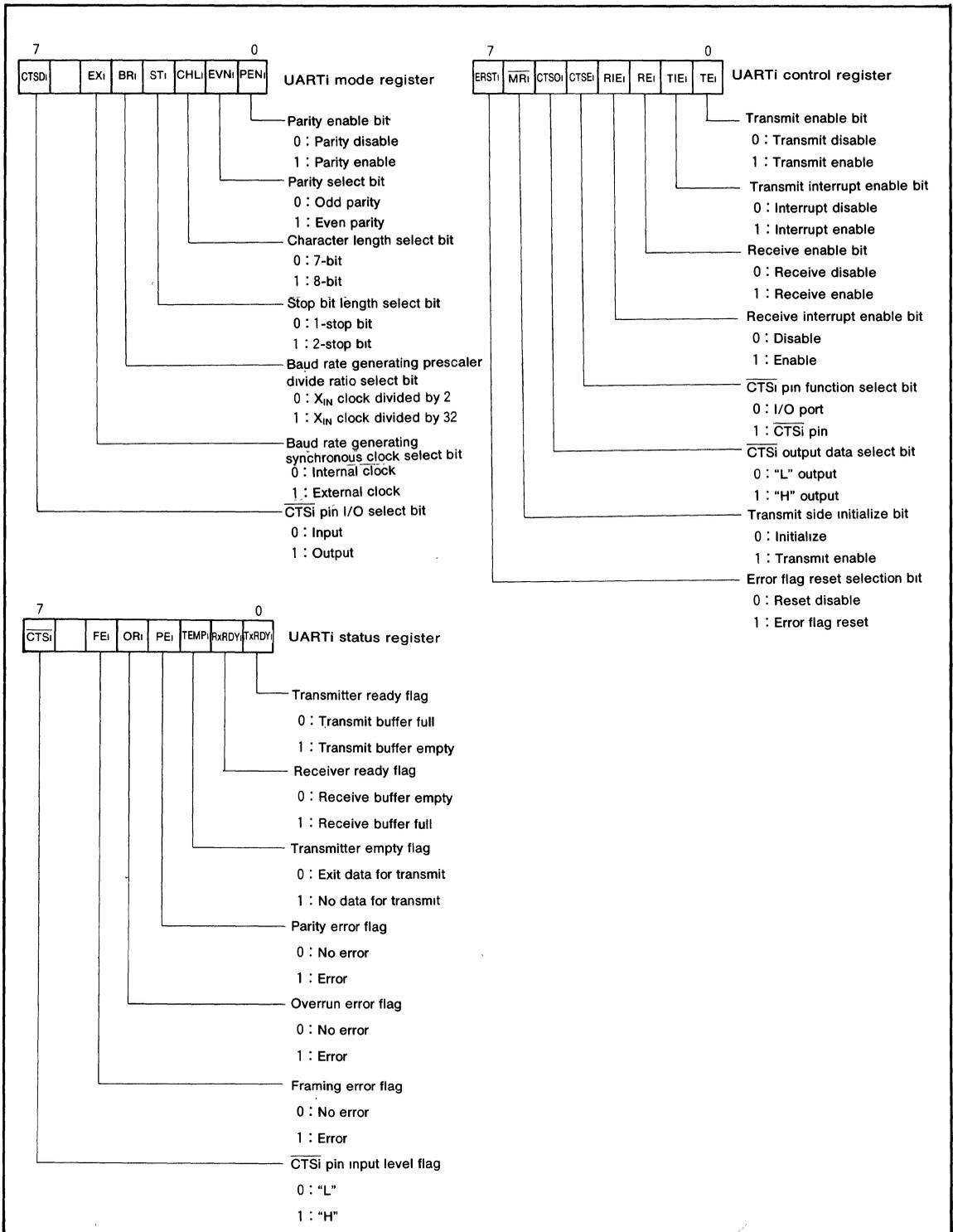


Fig. 12 Structure of registers related to UARTi

[$\overline{\text{CTS}}_i$ pin]

The $\overline{\text{CTS}}_i$ pin can be used as the 1-bit I/O port when bit 4 of the UART_i control register (CTSE_i) is "0". In this case, the input/output direction can be determined by bit 7 of the UART_i mode register (CTSD_i) and the output data can be set by bit 5 of the UART_i control register (CTSO_i). Additionally, the input level can be known by bit 7 of the UART_i status register (CTS_i).

[UART_i mode register]

- Parity enable bit : PEN_i
Setting this bit to "1" adds a parity bit to the transmit data. In a receive operation, this bit is used for parity evaluation.
- Parity select bit : EVN_i
This bit specifies the parity bit to be generated in a transmit operation and the parity bit to be evaluated in a receive operation. Depending on the content of this bit, the number of 1's in data is made even or odd.
- Character length select bit : CHL_i
This bit specifies the character length of data.
- Stop bit length select bit : STI
This bit specifies the stop bit length.
- Baud rate generating prescaler divide ratio select bit : BRI
When this bit is "0", the signal obtained by dividing X_{IN} clock by 2 becomes the count source of the baud rate divider. When this bit is "1", the signal is obtained by dividing the clock by 32.
- Baud rate generating synchronous clock selection bit : EX_i
This bit specifies baud rate synchronous clock. When this bit is "1", external clock is input from the CLK pin.
- $\overline{\text{CTS}}_i$ pin I/O select bit : CTSD_i
When this bit is "0", the $\overline{\text{CTS}}_i$ pin is the input pin.
When this bit is "1", the pin is the output pin. To use the $\overline{\text{CTS}}_i$ pin as the CTS_i input, set "0".

[UART_i control register]

- Transmit enable bit : TE_i
Setting this bit to "1" enables a transmit operation.
- Transmit interrupt enable bit : TIE_i
When this bit is "1", the interrupt in a transmit operation is enabled.
- Receive enable bit : RE_i
Setting this bit to "1" enables a receive operation.
- Receive interrupt enable bit : RIE_i
When this bit is "1", the interrupt in a receive operation is enabled.
- $\overline{\text{CTS}}_i$ pin function select bit : CTSE_i
When this bit is "1", the $\overline{\text{CTS}}_i$ pin becomes the $\overline{\text{CTS}}_i$ input.

- $\overline{\text{CTS}}_i$ output data select bit : CTSO_i
When this bit is "0", "L" is output. When it is "1", "H" is output.
- Transmit side initialize bit : MRI
When this bit is "0", the transmit side is initialized.
- Error flag reset select bit : ERST_i
Setting this bit to "1" resets all error flags. When this bit is read, "0" is always read.

[UART_i status register]

- Transmitter ready flag : TxRDY_i
When this flag is "1", it indicates that the transmit buffer register is empty and ready for writing transmit data.
- Receiver ready flag : RxRDY_i
When this flag is "1", it indicates that the receive buffer register is holding receive data. When the receive buffer register is read, it is cleared.
- Transmitter empty flag : TEMP_i
When this flag is "1", it indicates that neither the transmit shift register nor the transmit buffer register holds the data to be transmitted.
- Parity error flag : PE_i
This bit is set to "1" when the parity of the received data is different from the parity which was set.
- Overrun error flag : ORI
When this flag is "1", it indicates that, before the data in the receive buffer register is read, the next data is transferred from the receive shift register to the receive buffer register and the previous data is lost.
- Framing error flag : FE_i
This flag is set to "1" when the stop bit is found "L" when data is transferred from the receive shift register to the receive buffer register.
- $\overline{\text{CTS}}_i$ pin input level flag : CTS_i
When the input level of the $\overline{\text{CTS}}_i$ pin is "L", "0" is read; when it is "H", "1" is read.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

RESET CIRCUIT

The M37409M2-XXXSP is reset according to the sequence shown in Figure 14. It starts the program from the address formed by using the content of address $1FFF_{16}$ as the high order address and the content of the address $1FFE_{16}$ as the low order address, when the RESET pin is held at "L" level for more than $2\mu s$ while the power voltage is in the recom-

mended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 15 and 16.

An example of the reset circuit is shown in Figure 13. When the power on reset is used, the RESET pin must be held "L" until the oscillation of X_{IN} - X_{OUT} becomes stable.

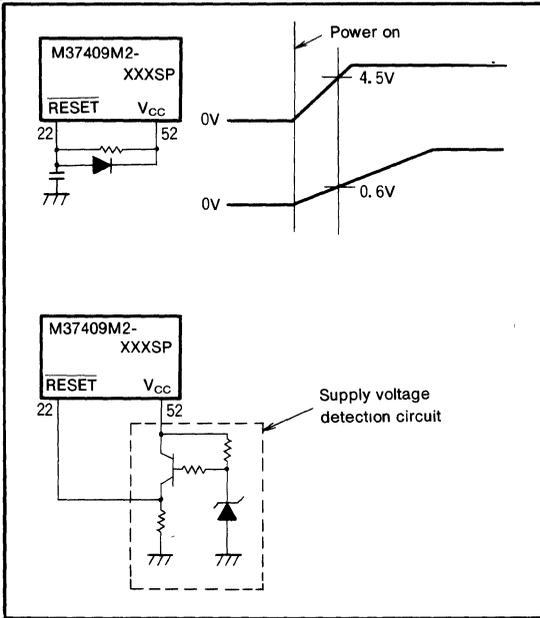
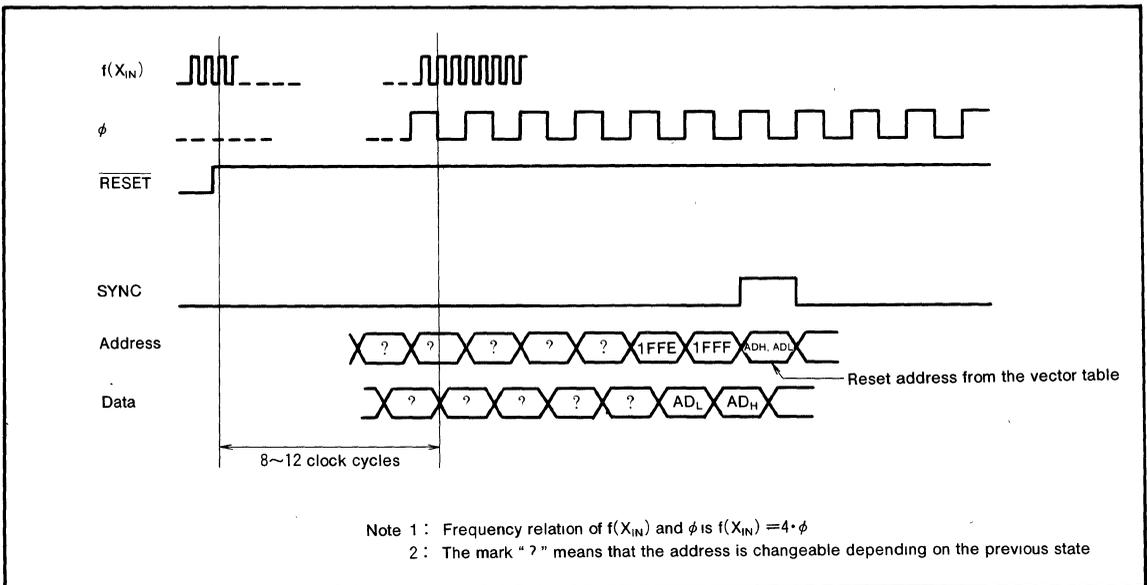


Fig. 13 Example of reset circuit



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN}) = 4 \cdot \phi$
 2 : The mark "?" means that the address is changeable depending on the previous state

Fig.14 Timing diagram at reset

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Local bus address									
(1) Port P1 directional register	(E1 ₁₆)... 00 ₁₆								
(2) Dual-port RAM direction specify register	(E2 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	0	0	0	0	0	0
X	X	0	0	0	0	0	0		
(3) UART1 status register	(E5 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr></table>	X	X	0	0	0	1	0	1
X	X	0	0	0	1	0	1		
(4) UART1 mode register	(E5 ₁₆)... <table border="1"><tr><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	X	0	0	0	0	0	0
0	X	0	0	0	0	0	0		
(5) UART1 control register	(E6 ₁₆)... 00 ₁₆								
(6) UART2 status register	(E9 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr></table>	X	X	0	0	0	1	0	1
X	X	0	0	0	1	0	1		
(7) UART2 mode register	(E9 ₁₆)... <table border="1"><tr><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	X	0	0	0	0	0	0
0	X	0	0	0	0	0	0		
(8) UART2 control register	(EA ₁₆)... 00 ₁₆								
(9) UART3 status register	(ED ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr></table>	X	X	0	0	0	1	0	1
X	X	0	0	0	1	0	1		
(10) UART3 mode register	(ED ₁₆)... <table border="1"><tr><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	X	0	0	0	0	0	0
0	X	0	0	0	0	0	0		
(11) UART3 control register	(EE ₁₆)... 00 ₁₆								
(12) IPC error register 0	(F4 ₁₆)... 00 ₁₆								
(13) IPC error register 1	(F5 ₁₆)... 00 ₁₆								
(14) IPC error register 2	(F6 ₁₆)... 00 ₁₆								
(15) IPC error register 3	(F7 ₁₆)... 00 ₁₆								
(16) IPC semaphore register	(F9 ₁₆)... 00 ₁₆								
(17) Collision detect register	(FA ₁₆)... 00 ₁₆								
(18) Interrupt enable register	(FB ₁₆)... 00 ₁₆								
(19) Interrupt request register	(FC ₁₆)... 00 ₁₆								
(20) Prescaler X	(FD ₁₆)... FF ₁₆								
(21) Timer X	(FE ₁₆)... 01 ₁₆								
(22) Timer control register	(FF ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td></tr></table>	0	0	0	X	X	X	0	0
0	0	0	X	X	X	0	0		
(23) Access flag (C0 ₁₆ ~D7 ₁₆)	00 ₁₆								
(24) Processor status register (PS)	<table border="1"><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td></tr></table>							1	
						1			
(25) Program counter (PC _H)	Contents of address 1FFF ₁₆								
(PC _L)	Contents of address 1FFE ₁₆								

Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values

Fig.15 Internal state of microcomputer at reset (1)

System bus address	
(1) Port P0 directional register	(F7 ₁₆)... 00 ₁₆
(2) IPC error register 0	(F8 ₁₆)... 00 ₁₆
(3) IPC error register 1	(E9 ₁₆)... 00 ₁₆
(4) IPC error register 2	(FA ₁₆)... 00 ₁₆
(5) IPC error register 3	(FB ₁₆)... 00 ₁₆
(6) Collision detect register	(FE ₁₆)... 00 ₁₆
(7) IPC semaphore register	(FF ₁₆)... 00 ₁₆
(8) Access flag (C0~D7 ₁₆)	00 ₁₆

Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values

Fig.16 Internal state of microcomputer at reset (2)

I/O PORTS

(1) Port P0 System bus : address F6₁₆
Port P0 is an 8-bit I/O port with CMOS output. It can be accessed from system bus only and can not be accessed from local bus.

As shown in the memory map (Figure 1), port P0 can be accessed at system bus address F6₁₆. Port P0 has a directional register (address F7₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state. This port becomes input at reset.

(2) Port P1 Local bus : address 00E0₁₆
System bus : address F5₁₆

Port P1 is an 8-bit I/O port and connected to local bus. It has the same function as port P0 except the connected bus.

It's directional register is at local bus address 00E1₁₆. Also port P1 can be read from system bus but the pin state is read regardless the value of the port P1 directional register.

(3) Address pins
Address pins A₀ ~ A₇ are the input pins directly connected to the system bus. The 8-bit address corresponding to the system bus is input to these pins. The input level is TTL.

(4) Data pins
Data pins D₀ ~ D₇ are the output pins directly connected to the system bus. The 8-bit data corresponding to the system bus is input/output on these pins. When the CS pin is "L" and the RD pin is "L", the data pins become the output pins. When the CS pin is "L" and the WR pin is "L", the data pins become the input pins. Setting the CS pin to "H" puts pins D₀~D₇ in the floating state. The I/O level is TTL.

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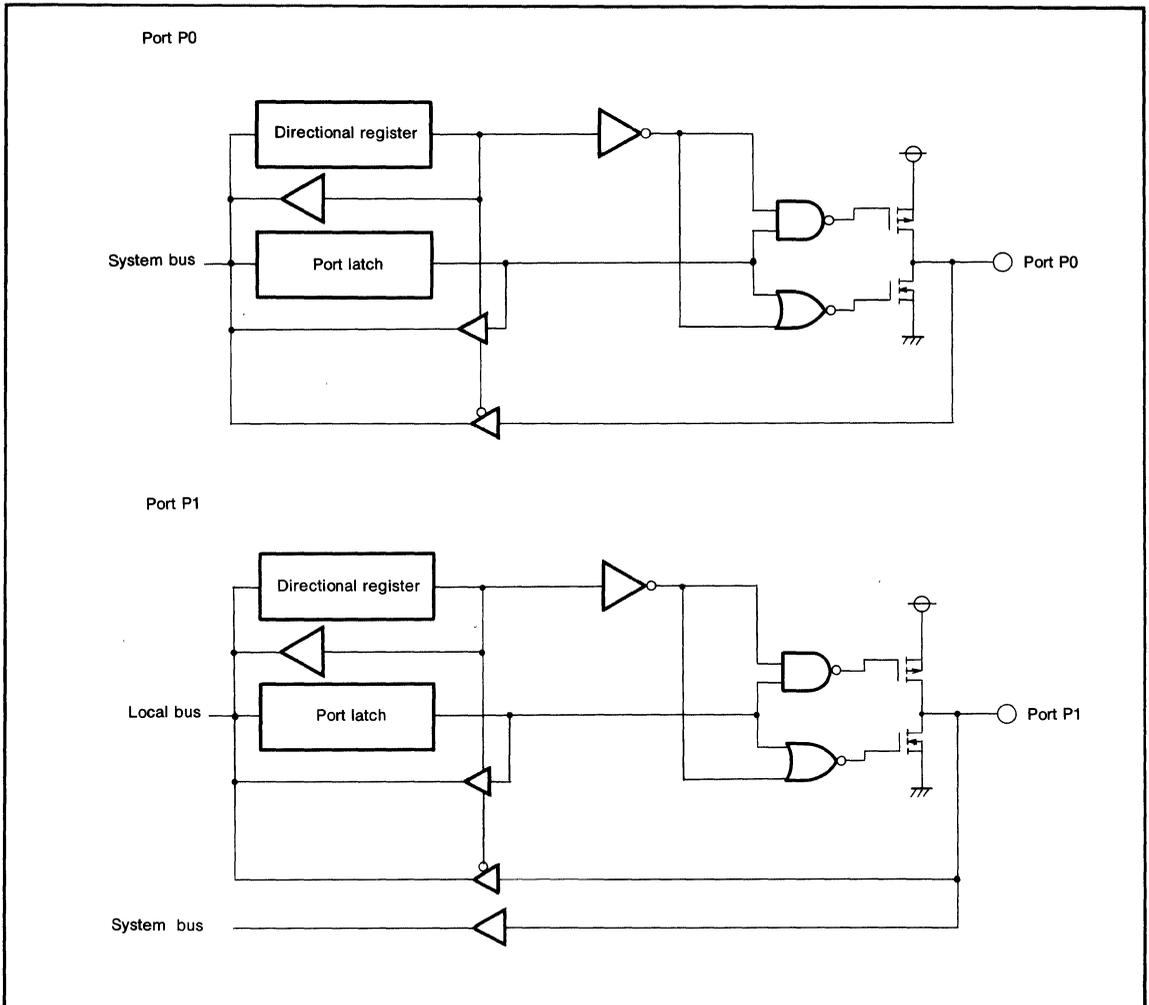


Fig. 17 Port P0, P1 block diagram

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 18.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16} , respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 19 and 20.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 21. X_{IN} is the input, and X_{OUT} is open.

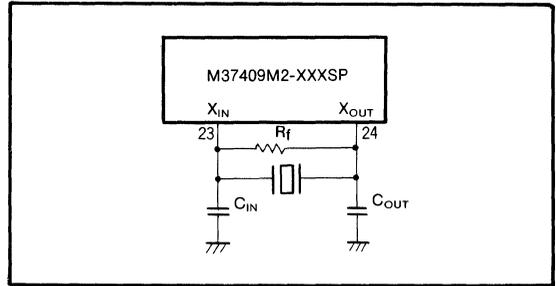


Fig. 19 External ceramic resonator circuit

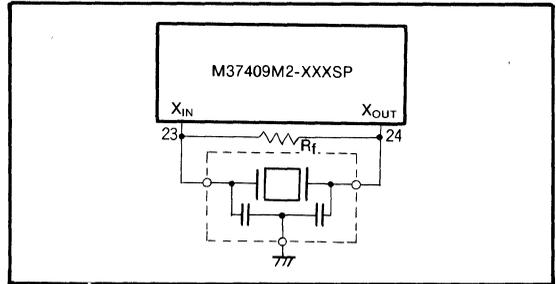


Fig. 20 External ceramic resonator circuit (capacity built-in type)

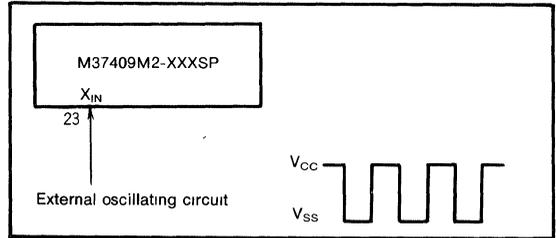


Fig. 21 External clock input circuit

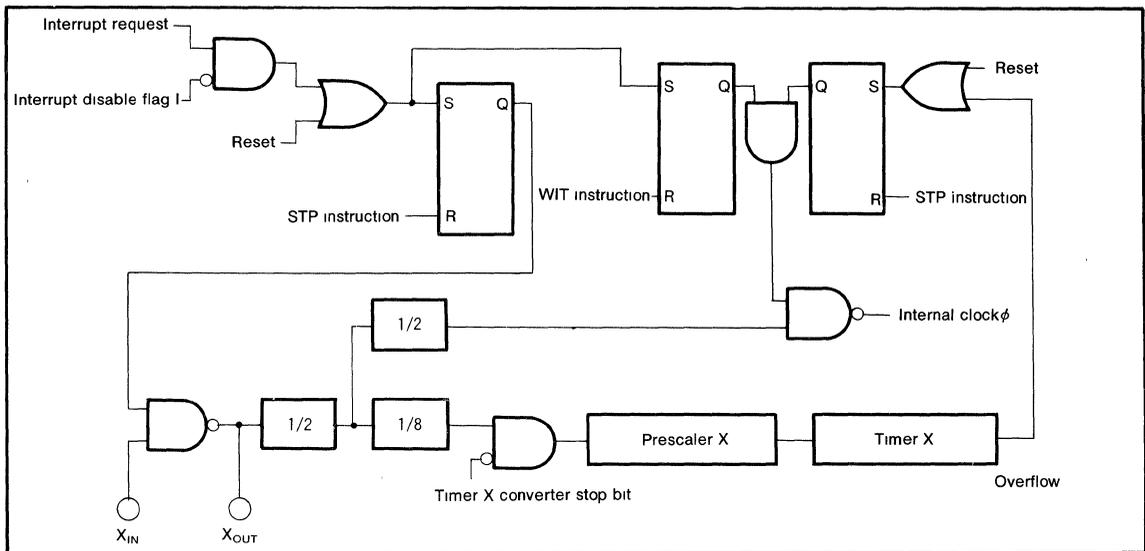


Fig. 18 Block diagram of clock generating circuit

PROGRAMMING NOTES

- (1) The frequency ratio of the timer and the prescaler is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) Change the address $A_0 \sim A_7$ input and the \overline{CS} input when both the \overline{RD} input and \overline{WR} input are "H".
- (4) Registers whose values change when read, are connected to the system bus of the M37409M2-XXXSP. If the master CPU generates an invalid read cycle, data is not correctly transferred.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (7) The STP instruction must be executed after setting timer X count enable bit to enable "0", timer X interrupt enable bit to inhibit ("0"), and timer X interrupt request bit to no request ("0").
- (8) The power current is max. 10mA in DC. However, because a rush current and a bus charge-discharge current flow transiently, a bypass capacitor must be connected between V_{SS} and V_{CC} .

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3sets

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	-0.3~7	V
V_I	Input voltage, RESET, X_{IN}		-0.3~7	V
V_I	Input voltage, $P0_0\sim P0_7$, $P1_0\sim P1_7$, $D_0\sim D_7$, $A_0\sim A_7$, \overline{RD} , \overline{WR} , \overline{CS} , CLK, $RxD_1\sim RxD_3$, $\overline{CTS}_1\sim\overline{CTS}_3$		-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage, CNV_{SS}		-0.3~13	V
V_O	Output voltage, $P0_0\sim P0_7$, $P1_0\sim P1_7$, X_{OUT} , ϕ , $D_0\sim D_7$, $TxD_1\sim TxD_3$, $\overline{CTS}_1\sim\overline{CTS}_3$		-0.3~ $V_{CC}+0.3$	V
P_d	Power dissipation	$T_a = 25^\circ C$	1000 (Note 1)	mW
T_{opr}	Operating temperature		-10~70	$^\circ C$
T_{stg}	Storage temperature		-40~125	$^\circ C$

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = 5V \pm 10\%$, $T_a = -10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ.	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage X_{IN} , RESET, CLK, $P0_0\sim P0_7$, $P1_0\sim P1_7$, $RxD_1\sim RxD_3$, $\overline{CTS}_1\sim\overline{CTS}_3$	0.8 V_{CC}		$V_{CC}+0.3$	V
V_{IH}	"H" input voltage $A_0\sim A_7$, $D_0\sim D_7$, \overline{RD} , \overline{WR} , \overline{CS}	2		$V_{CC}+0.3$	V
V_{IL}	"L" input voltage $P0_0\sim P0_7$, $P1_0\sim P1_7$, CLK, $RxD_1\sim RxD_3$, $\overline{CTS}_1\sim\overline{CTS}_3$	-0.3		0.2 V_{CC}	V
V_{IL}	"L" input voltage $A_0\sim A_7$, $D_0\sim D_7$, \overline{RD} , \overline{WR} , \overline{CS}	-0.3		0.8	V
V_{IL}	"L" input voltage RESET	-0.3		0.12 V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	-0.3		0.16 V_{CC}	V
I_{OH}	"H" output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, ϕ , $TxD_1\sim TxD_3$, $\overline{CTS}_1\sim\overline{CTS}_3$			-10	mA
I_{OH}	"H" output current $D_0\sim D_7$			-1.0	mA
I_{OL}	"L" output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, ϕ , $TxD_1\sim TxD_3$, $\overline{CTS}_1\sim\overline{CTS}_3$			10	mA
I_{OL}	"L" output current $D_0\sim D_7$			-1.6	mA

Note 1 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms

2 : Total of $I_{OL(peak)}$, of ports $P0$, $P1$, $TxD_1\sim TxD_3$ and $\overline{CTS}_1\sim\overline{CTS}_3$ is -50mA

Total of $I_{OH(peak)}$, of ports $P0$, $P1$, $TxD_1\sim TxD_3$ and $\overline{CTS}_1\sim\overline{CTS}_3$ is 50mA

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V, V_{SS} = 0V, T_A = 25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
V_{OH}	"H" output voltage $P0_0 \sim P0_7, P1_0 \sim P1_7, \phi, TxD_1 \sim TxD_3, CTS_1 \sim CTS_3$	$I_{OH} = -10mA$	$V_{CC} - 2$			V
V_{OH}	"H" output voltage $D_0 \sim D_7$	$I_{OH} = -1mA$	2.4			V
V_{OL}	"L" output voltage $P0_0 \sim P0_7, P1_0 \sim P1_7, \phi, TxD_1 \sim TxD_3, CTS_1 \sim CTS_3$	$I_{OL} = 10mA$			2	V
V_{OL}	"L" output voltage $D_0 \sim D_7$	$I_{OL} = 1.6mA$			0.4	V
I_I	Input leak current $A_0 \sim A_7, RD, WR, CS, CLK$	$V_{SS} \leq V_I \leq V_{CC}$	-5		5	μA
I_I	Input leak current $RESET, X_{IN}$	$V_{SS} \leq V_I \leq 7V$	-5		5	μA
I_{OZ}	Tri-state leak current $P0_0 \sim P0_7, P1_0 \sim P1_7, D_0 \sim D_7, CTS_1 \sim CTS_3$	$V_{SS} + 0.5 \leq V_O \leq V_{CC} - 0.5V$	-5		5	μA
$V_{T+} - V_{T-}$	Hysteresis $RESET, CLK, RxD_1 \sim RxD_3, CTS_1 \sim CTS_3$			0.6		V
I_{CC}	Supply current	Output terminals are opened, others to V_{SS} , $CS = V_{CC}$	$f_{(X_{IN})} = 8 \sim 10MHz$ Square wave		10	mA
			ditto (wait mode)		1	
			At stop mode $T_A = 25^\circ C$		1	μA
			At stop mode $T_A = 70^\circ C$		10	

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMING REQUIREMENTS

System bus ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=5\sim 10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(A-WR)}$	$A_0\sim A_7$ \overline{CS} input set-up time	Fig. 22	50			ns
$t_{SU(A-RD)}$	$A_0\sim A_7$ \overline{CS} input set-up time		50			ns
$t_{SU(D-WR)}$	$D_0\sim D_7$ input set-up time		80			ns
$t_h(WR-A)$	$A_0\sim A_7$ \overline{CS} input hold time		0			ns
$t_h(RD-A)$	$A_0\sim A_7$ \overline{CS} input hold time		0			ns
$t_h(WR-D)$	$D_0\sim D_7$ input hold time		10			ns
$t_w(WR)$	\overline{WR} input "L" pulse width		200			ns
$t_w(RD)$	\overline{RD} input "L" pulse width		200			ns

Local bus ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=5\sim 10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P1-\phi)}$	$P1_0\sim P1_7$ input set-up time	Fig. 22	300			ns
$t_h(\phi-P1)$	$P1_0\sim P1_7$ input hold time		50			ns

SWITCHING CHARACTERISTICS

System bus ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=5\sim 10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(D-RD)}$	$D_0\sim D_7$ output delay time	Fig. 22			150	ns
$t_{v(D-RD)}$	$D_0\sim D_7$ output effective time		0			ns
$t_{en(RD-D)}$	$D_0\sim D_7$ output enable time		10			ns
$t_{dis(RD-D)}$	$D_0\sim D_7$ output disable time				50	ns

Local bus ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=5\sim 10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P1)}$	$P1_0\sim P1_7$ output delay time	Fig. 22			300	ns

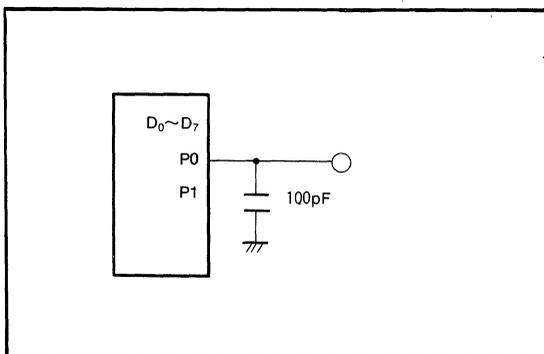
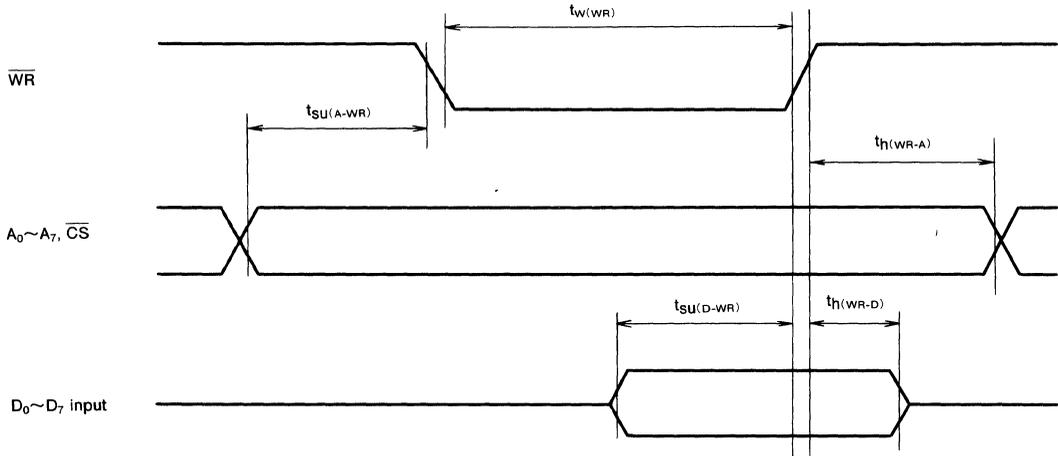


Fig. 22 Port P0, P1, $D_0\sim D_7$ test circuit

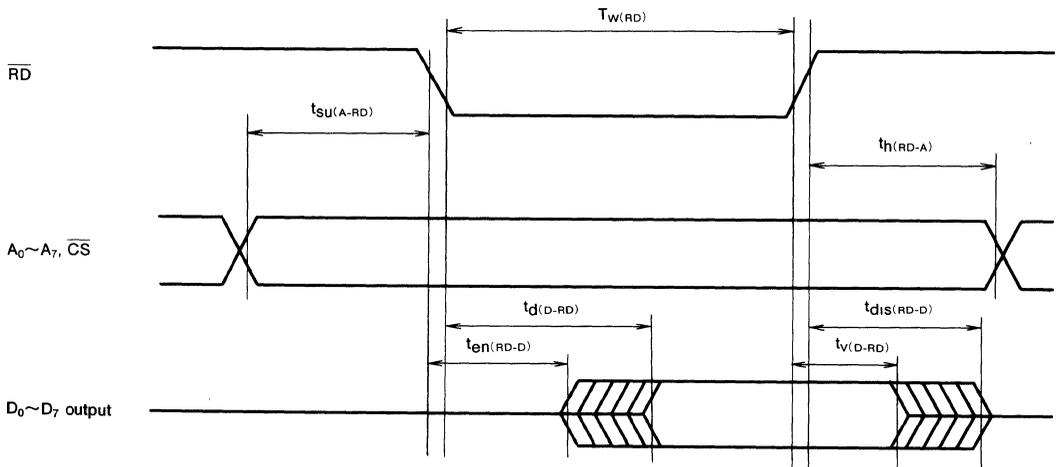
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMING DIAGRAMS

System bus write cycle

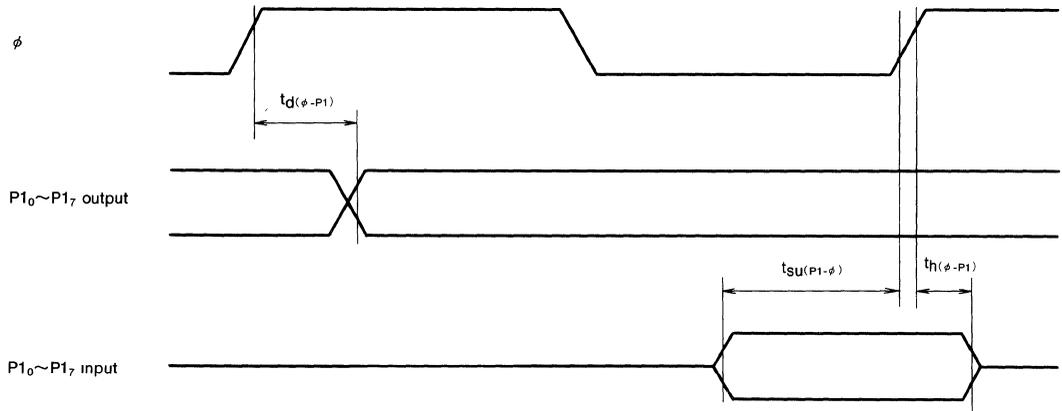


System bus read cycle



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Local bus



M37410M3HXXXFP, M37410M4HXXXFP M37410M6HXXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37410M3HXXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin plastic molded QFP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

This microcomputer is also suitable for applications which require controlling LCDs.

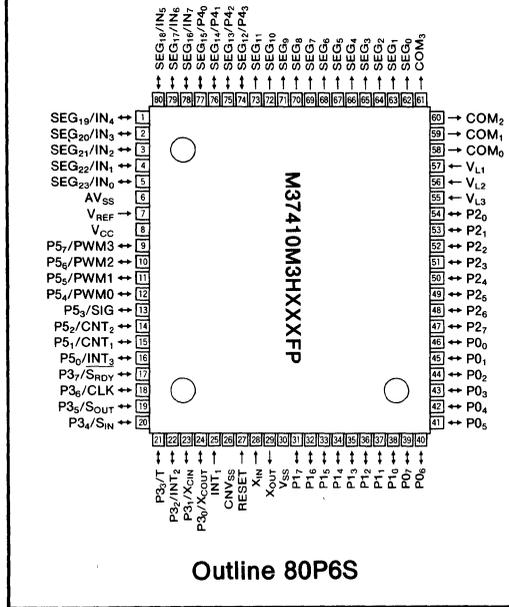
The differences among the M37410M3HXXXFP, the M37410M4HXXXFP and the M37410M6HXXXFP are noted below. The following explanations apply to the M37410M3HXXXFP. Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37410M3HXXXFP	6144 bytes	192 bytes
M37410M4HXXXFP	8192 bytes	256 bytes
M37410M6HXXXFP	12288 bytes	256 bytes

FEATURES

- Number of basic instructions..... 69
- Memory size
 - ROM 6144 bytes (M37410M3HXXXFP)
8192 bytes (M37410M4HXXXFP)
12288 bytes (M37410M6HXXXFP)
 - RAM.....192 bytes (M37410M3HXXXFP)
256 bytes (M37410M4HXXXFP,
M37410M6HXXXFP)
- Instruction execution time (minimum instructions)
 - at high-speed mode 1 μ s
 - at low-speed mode 4 μ s
- Single power supply
 - f(X_{IN})=8MHz 4.5~5.5V
 - f(X_{IN})=2MHz 2.5~5.5V
- Power dissipation
 - normal operation mode (at 8MHz frequency)
..... 30mW (V_{CC}=5V, Typ.)
 - low-speed operation mode (at 32kHz frequency for
clock function).....54 μ W (V_{CC}=3V, Typ.)
- RAM retention voltage (stop mode)
..... 2.0V ≤ V_{RAM} ≤ 5.5V
- Subroutine nesting 96levels (Max.)
- Interrupt..... 10types, 5vectors
- 8-bit timer 4 (3 when used as serial I/O)
- 16-bit timer 1 (Two 8-bit timers make one set)
- Programmable I/O ports
(Ports P0, P1, P2, P3, P5) 40
- Input port (Port P4) 4
- Serial I/O (8-bit) 1
- A-D converter 8-bit, 8channel

PIN CONFIGURATION (TOP VIEW)



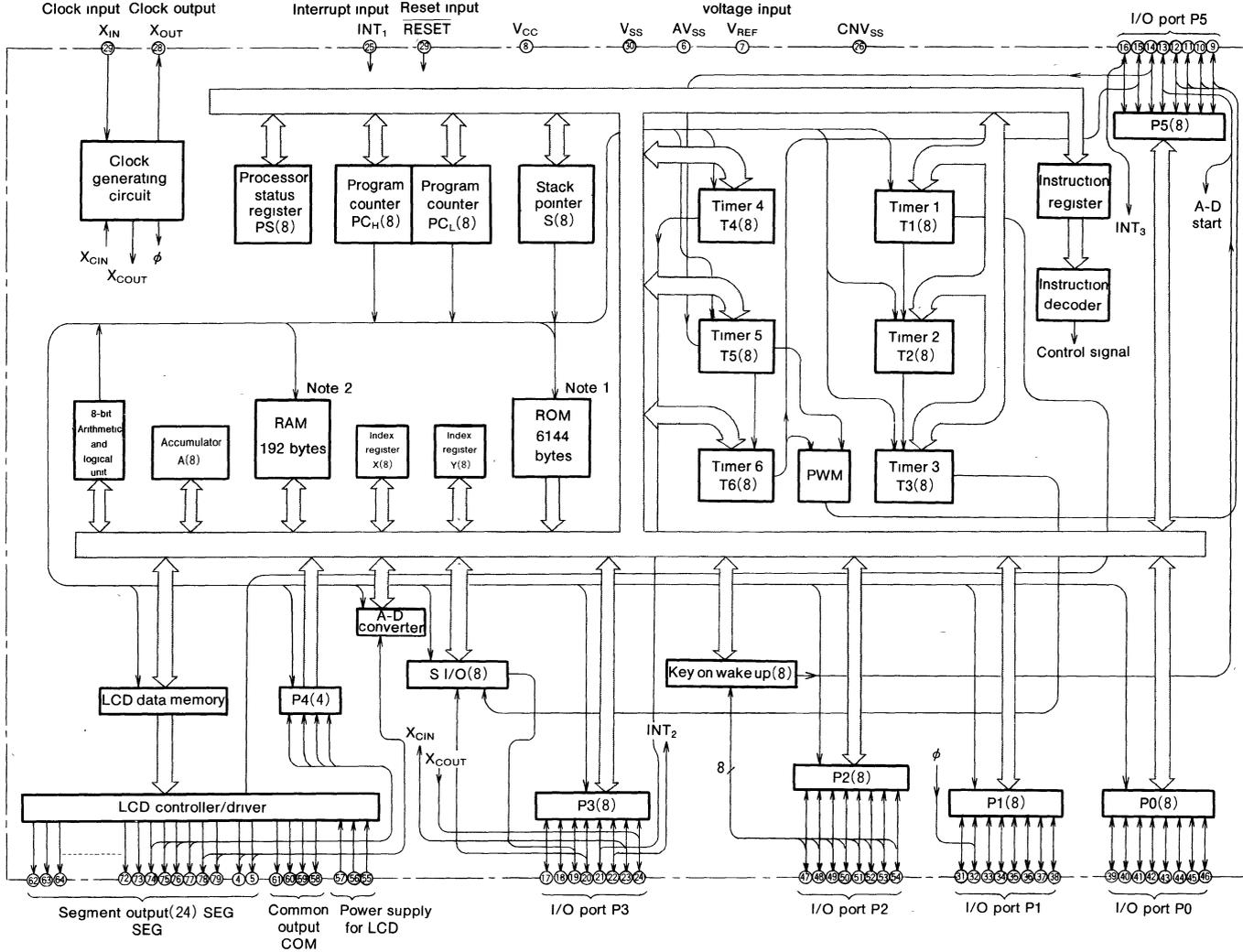
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty) segment output..... 24 common output 4
- Two clock generating circuits
(One is for main clock, the other is for clock function)

APPLICATION

Audio-visual equipment,
Remote control,
Camera



M37410M3HXXXFP BLOCK DIAGRAM



Note 1 : 8192 bytes for M37410M4HXXXFP and 12288 bytes for M37410M6HXXXFP
 Note 2 : 256 bytes for M37410M4HXXXFP and M37410M6HXXXFP

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FUNCTIONS OF M37410M3HXXXFP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		1 μ s (minimum instructions, at 8MHz frequency)	
Clock frequency		8MHz (at V _{CC} =5V \pm 10%)	
Memory size	M37410M3HXXXFP	ROM	6144bytes
		RAM	192bytes
	M37410M4HXXXFP	ROM	8192bytes
		RAM	256bytes
	M37410M6HXXXFP	ROM	12288bytes
		RAM	256bytes
RAM for display LCD		12bytes	
Input/Output port	P0, P1, P2, P3, P5	I/O	8-bit \times 5
	P4	Input	4-bit \times 1 (port P4 are in common with SEG)
	SEG	LCD output	24-bit \times 1
	COM	LCD output	4-bit \times 1
Serial I/O		8-bit \times 1	
Timers		8-bit timer \times 4 16-bit timer \times 1 (combination of two 8-bit timers)	
LCD controller/driver	Bias		1/2, 1/3 bias selectable
	Duty ratio		1/2, 1/3, 1/4 duty selectable
	Common output		4
	Segment output		24 (SEG ₁₂ ~SEG ₂₃ are in common with port P4 and analog input pins IN ₇ ~IN ₀)
Subroutine nesting		96 (max)	
Interrupt		Three external interrupts, three timer interrupts, serial I/O interrupt, A-D interrupt, key on wake up, one software interrupt	
Clock generating circuit		Two built-in circuits (ceramic or quartz crystal oscillator)	
Operating temperature range		-20~75°C	
Device structure		CMOS silicon gate	
Package		80-pin plastic molded QFP	

M37410M3HXXXFP, M37410M4HXXXFP M37410M6HXXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} , V_{SS}	Supply voltage		Power supply inputs $5V \pm 10\%$ to V_{CC} , and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is connect to V_{SS}
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than $16\mu s$ (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
INT_1	Interrupt input	Input	This is the highest order interrupt input pin
AV_{SS}	Voltage input for A-D		This is GND input pin for the A-D converter
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter
$P0_0 \sim P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
$P1_0 \sim P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-ch open drain
$P2_0 \sim P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 and also works as the key on wake up function with mask option
$P3_0 \sim P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P1 When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as \overline{S}_{RDY} , CLK, S_{OUT} , and S_{IN} pins, respectively Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 4 overflow signal divided by 2 output pin (T), INT_2 pin, X_{CIN} and X_{COUT} pins, respectively
$SEG_{12}/P4_3$ } $SEG_{15}/P4_0$	Segment output /Input port P4	Output / Input	$SEG_{12} \sim SEG_{15}$ work as input port P4 and also used by 2-bit unit as LCD segment output
$P5_0 \sim P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P1 $P5_0$, $P5_1$, $P5_2$ and $P5_3$ are in common with INT_3 , timer3 input, timer5 input and A-D trigger input respectively $P5_4 \sim P5_7$ are also in common with PWM0~PWM3
$V_{L1} \sim V_{L3}$	Voltage input for LCD	Input	These are voltage input pins for LCD Supply voltage as $0V \leq V_{L1} \leq V_{L2} \leq V_{L3} \leq V_{CC}$ $0 \sim V_{L3}V$ is supplied to LCD.
$COM_0 \sim$ COM_3	Common output	Output	These are LCD common output pins At 1/2 duty, COM_2 and COM_3 pins are not used At 1/3 duty, COM_3 is not used
$SEG_0 \sim$ SEG_{11}	Segment output	Output	These are LCD segment output pins
SEG_{16}/IN_7 } SEG_{23}/IN_0	Segment output /Analog input	I/O	$SEG_{16} \sim SEG_{23}$ work as analog input pins $IN_7 \sim IN_0$ $SEG_{16} \sim SEG_{19}$ are used by 2-bit unit and $SEG_{20} \sim SEG_{23}$ by 4-bit unit

**M37410M3HXXXFP, M37410M4HXXXFP
M37410M6HXXXFP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37410 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

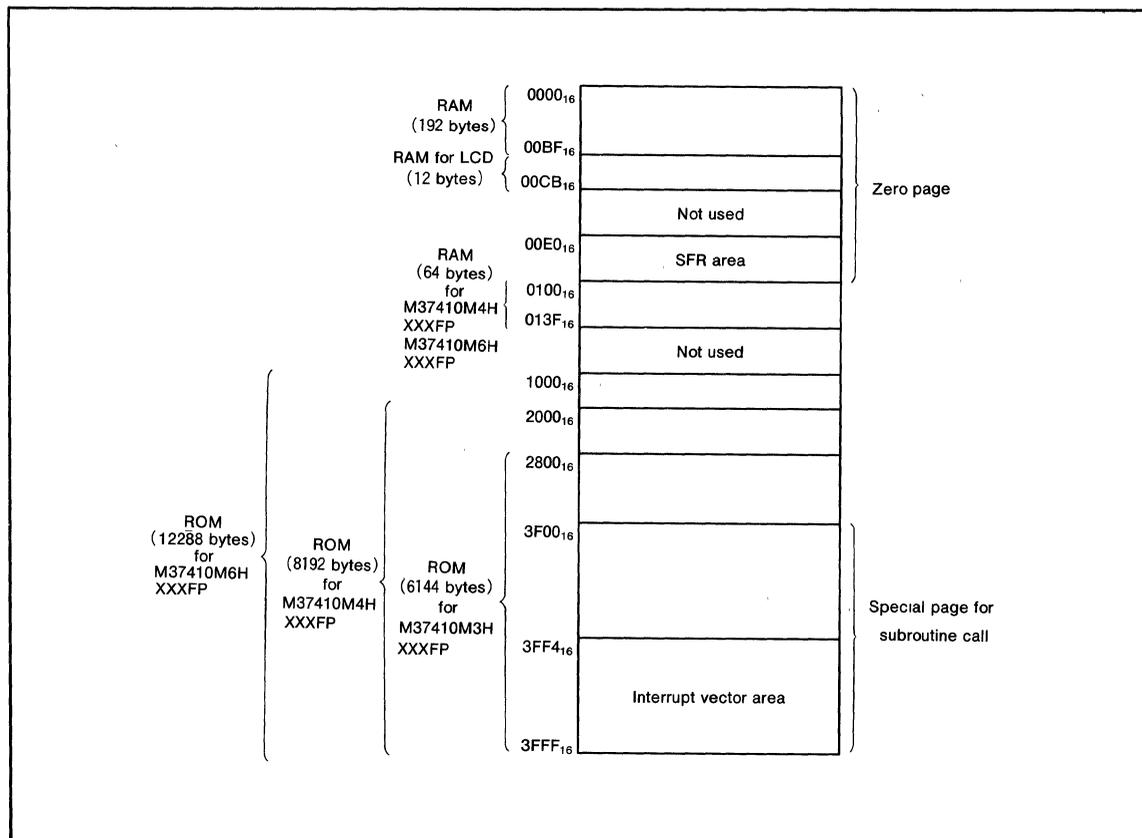


Fig. 1 Memory map

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00E0 ₁₆	Port P0	00F0 ₁₆	Interrupt request distinguish register 2
00E1 ₁₆	Port P0 directional register	00F1 ₁₆	Timer 6 latch
00E2 ₁₆	Port P1	00F2 ₁₆	A-D control register
00E3 ₁₆	Port P1 directional register	00F3 ₁₆	PWM control register
00E4 ₁₆	Port P2	00F4 ₁₆	Segment control register
00E5 ₁₆	Port P2 directional register	00F5 ₁₆	LCD mode register
00E6 ₁₆		00F6 ₁₆	Serial I/O mode register
00E7 ₁₆		00F7 ₁₆	Serial I/O register
00E8 ₁₆	Port P3	00F8 ₁₆	Timer 4, 5, 6 mode register
00E9 ₁₆	Port P3 directional register	00F9 ₁₆	Timer 1 latch
00EA ₁₆	Port P4	00FA ₁₆	Timer 2 latch
00EB ₁₆	Interrupt request distinguish register 1	00FB ₁₆	Timer 3 latch
00EC ₁₆	Port P5	00FC ₁₆	Timer 4 latch
00ED ₁₆	Port P5 directional register	00FD ₁₆	Timer 5 latch
00EE ₁₆	P2 Key on wake up register	00FE ₁₆	Interrupt control register
00EF ₁₆	A-D register	00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

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INTERRUPT

The M37410M3HXXXFP can be interrupted from ten sources; INT₁, Timer 2 or Serial I/O, INT₃ or Key on wake up, INT₂ or Timer 3, Timer 6 or A-D, and BRK instruction.

"Key on wake up" can only be used at power down state by STP instruction or WIT instruction. When one of the P2 or P7 is "L", an interrupt occurs.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

- (1) When the INT₁, INT₂ or INT₃ pins go from "H" to "L" or "L" to "H"
- (2) When the levels any pin of P2 or P7 goes "L" (at power down mode)
- (3) When the contents of timer 2, timer 3, timer 6 or the counter of serial I/O goes "0"

These request bits can be clear by a program but can not be set. The interrupt enable bit can be set and clear by a program.

When the two interrupt requests, which are the same priority and are at the same sampling, the priority process is processed by interrupt request distinguish register 1 and 2. The interrupt request distinguish bit is used by software to determine priority when two interrupt causes are allocated to the same interrupt vector (that is, the two interrupts have the same priority).

Irrespective of whether the interrupt is disabled or enabled, the interrupt request distinguish bit is automatically set to "1" when conditions arise that satisfy the interrupt cause.

However, the interrupt request distinguish bit is not automatically cleared. The bit must therefore be cleared by software in the interrupt service routine (before executing an RTI instruction).

Note that when using the instruction CLB to clear this bit, the request distinguish bit of an interrupt that is generated during execution of CLB will not be set (to "1"). Use one of the following two methods to clear interrupt request distinguish bits:

- ① Use instruction LDM to write directly to address 00EB₁₆ (interrupt request distinguish register 1) or 00F0₁₆ (interrupt request distinguish register 2).

```
LDM  # $nn, $zz
```

, Where zz is the address(00EB₁₆ or 00F0₁₆) of the interrupt request ; distinguish register that includes the interrupt request distinguish ; bit that is to be cleared and nn sets the interrupt request disting- ; uish bit to be cleared to "0" and other interrupt request distinguish ; bits to "1".

, Other control bits must be set according to the required control ; (interrupts enabled or disabled)

[Example] Clearing the INT₂ interrupt request distinguish bit

```
LDM  1X1X0X1XB, $00EB
```

↑ ↑ ↑

Of the interrupt request distinguish bits, only the INT₂ interrupt re-
quest distinguish bit, which is to be cleared, should be set to "0"
The values of bits marked "X" are determined by the control
being effected

- ② Use instructions LDA, ORA, AND, and STA to write via the accumulator to address 00EB₁₆ (interrupt request distinguish register 1) or 00F0₁₆ (interrupt request distinguish register 2).

```
LDA  $zz
```

```
ORA  # $nn
```

```
AND  # $nn
```

```
STA  $zz
```

, Where zz is the address(00EB₁₆ or 00F0₁₆) of the interrupt request ; distinguish register that includes the interrupt request distinguish ; bit that is to be cleared and nn sets the interrupt request disting- ; uish bit to be cleared to "0" and other interrupt request distinguish ; bits to "1". Other control bits must be set according to the required ; control (interrupts enabled or disabled)

[Example] Clearing the timer 6 interrupt request distinguish bit

```
LDA  $00F0
```

```
ORA  XX1X1X0XB
```

↑ ↑ ↑

Of the interrupt request distinguish bits, only the interrupt request
distinguish bit for timer 6, which is to be cleared, should be set to
"0" The values of bits marked "x" are determined by the control
being effected

↓ ↓ ↓

```
AND  XX1X1X0XB
```

```
STA  $00F0
```

Because an interrupt request is generated only at the time the interrupt request distinguish bit is set (to "1"), no interrupt will be generated while the interrupt request distinguish bit remains in the set state. For this reason, the interrupt request distinguish bit must be cleared by software in the interrupt service routine.

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Since the BRK instruction interrupt and the timer 6 or A-D, interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if timer 6 or A-D generated the interrupt.

Table 1. Interrupt vector address and priority

Event	Priority	Vector addresses	Remarks
RESET	1	3FFF ₁₆ , 3FFE ₁₆	Non-maskable
INT ₁ interrupt	2	3FFD ₁₆ , 3FFC ₁₆	External interrupt
Serial I/O or timer 2 interrupt	3	3FFB ₁₆ , 3FFA ₁₆	
INT ₃ or key on wake up interrupt	4	3FF9 ₁₆ , 3FF8 ₁₆	External interrupt
INT ₂ or timer 3 interrupt	5	3FF7 ₁₆ , 3FF6 ₁₆	External interrupt (INT ₂)
Timer 6 or A-D interrupt (BRK instruction interrupt)	6	3FF5 ₁₆ , 3FF4 ₁₆	(Non-maskable software interrupt)

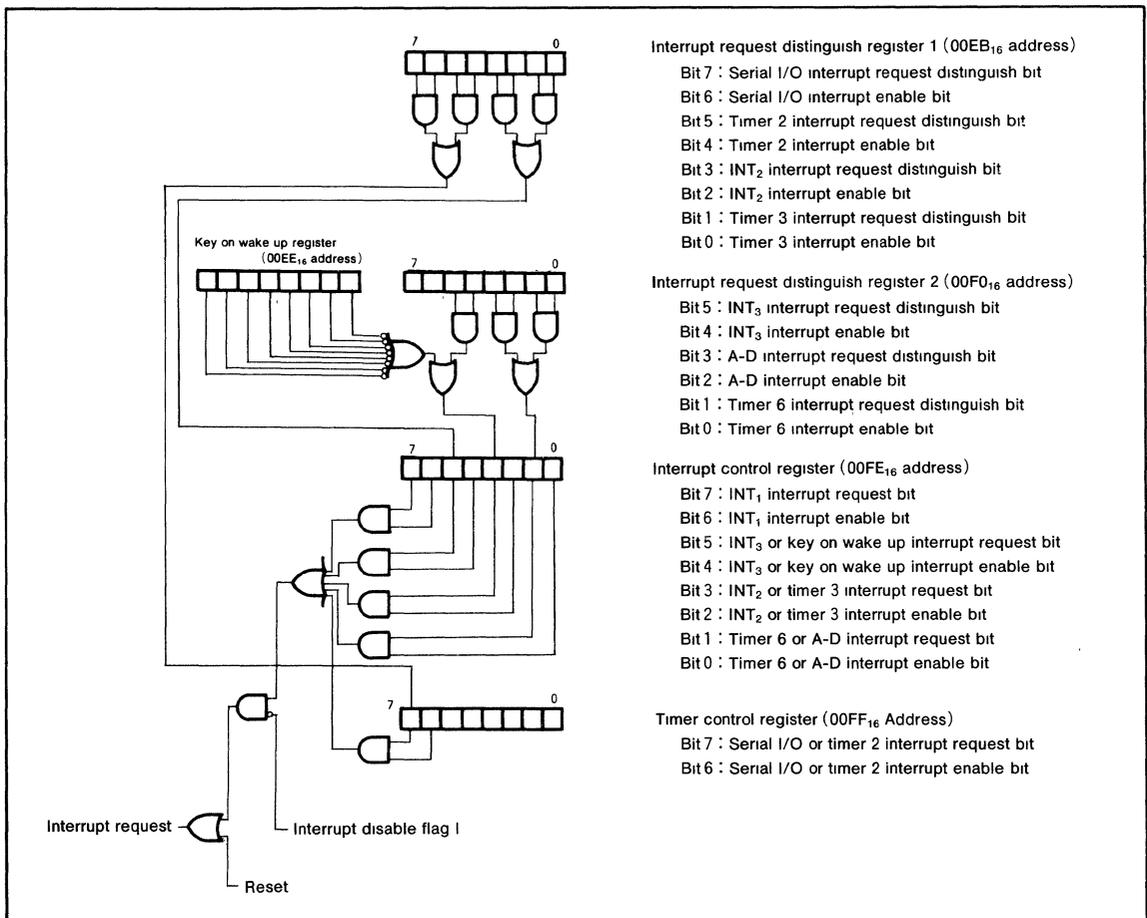


Fig. 3 Interrupt control

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TIMER

The M37410M3HXXXFP has six timers; timer 1, timer 2, timer 3, timer 4, timer 5 and timer 6.

A block diagram of timer1 through 6 is shown in Figure 4.

The count source for timer 1 through 3 can be selected by using bit 2, 3, 4 and 5 of the timer control register (address $00FF_{16}$), as shown in Figure 5. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch.

Timer 2, 3 and 6 has interrupt generating functions. The timer interrupt request bit which is in the interrupt distinguish register 1 or 2 (located at addresses $00EB_{16}$ and $00F0_{16}$ respectively) is set at the next count pulse after the timer reaches "0" (see interrupt section).

The starting and stopping of timer1 is controlled by bit 7 of the interrupt distinguish register 2, timer 3 by bit 6 of the interrupt distinguish register 2 and timer 4 by bit 3 of timer 4, 5 and 6 mode register ($00F8_{16}$ address). If the corresponding bit is "0", the timer starts counting, and the corresponding bit is "1", the timer stops. The timer4 overflow signal divided by 2 can be outputted from port $P3_3$ by setting the bit 4 of the serial I/O mode register ($00F6_{16}$ address) to "1".

Timer 5 and 6 work as timer mode, event counter mode and PWM mode by changing the contents of bit 5 and bit 6 of the timer 4, 5 and 6 mode register.

(1) Timer Mode

This mode is the 16-bit timer, and the count source is $\phi/4$. When the bit 6 of PWM control register ($00F3_{16}$ address) is "1", the timer6 overflow signal divided by 2 is output from CNT_2 pin (common with $P5_2$).

(2) Event Counter Mode

The count source is input from the CNT_2 pin. The count decremented each time the input goes from "L" to "H".

(3) PWM Mode

As shown in Figure 7, the output wave is controlled by the contents of the timer latch of timer 5 and 6.

PWM output can choose among PWM0, PWM1, PWM2 and PWM3 by bit 0, bit 1, bit 2 and bit 3 of PWM control register.

When the count value of all timers, from timer 1 to timer 6, are read, be careful not to change the input source.

When the count source is inputted from the external pin, the minimum pulse width should be $8\mu s$.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 5 of the timer control register).

This state is canceled if timer2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 7 of the interrupt request distinguish register2 (timer1 count stop bit), bit 5 of the interrupt request distinguish register1, and bit 6 and bit 7 of the timer control

register must be set to "0" (prohibition). And also-bit 4 of the interrupt request distinguish register1 must be set to "1". For more details on the STP instruction, refer to the oscillation circuit section.

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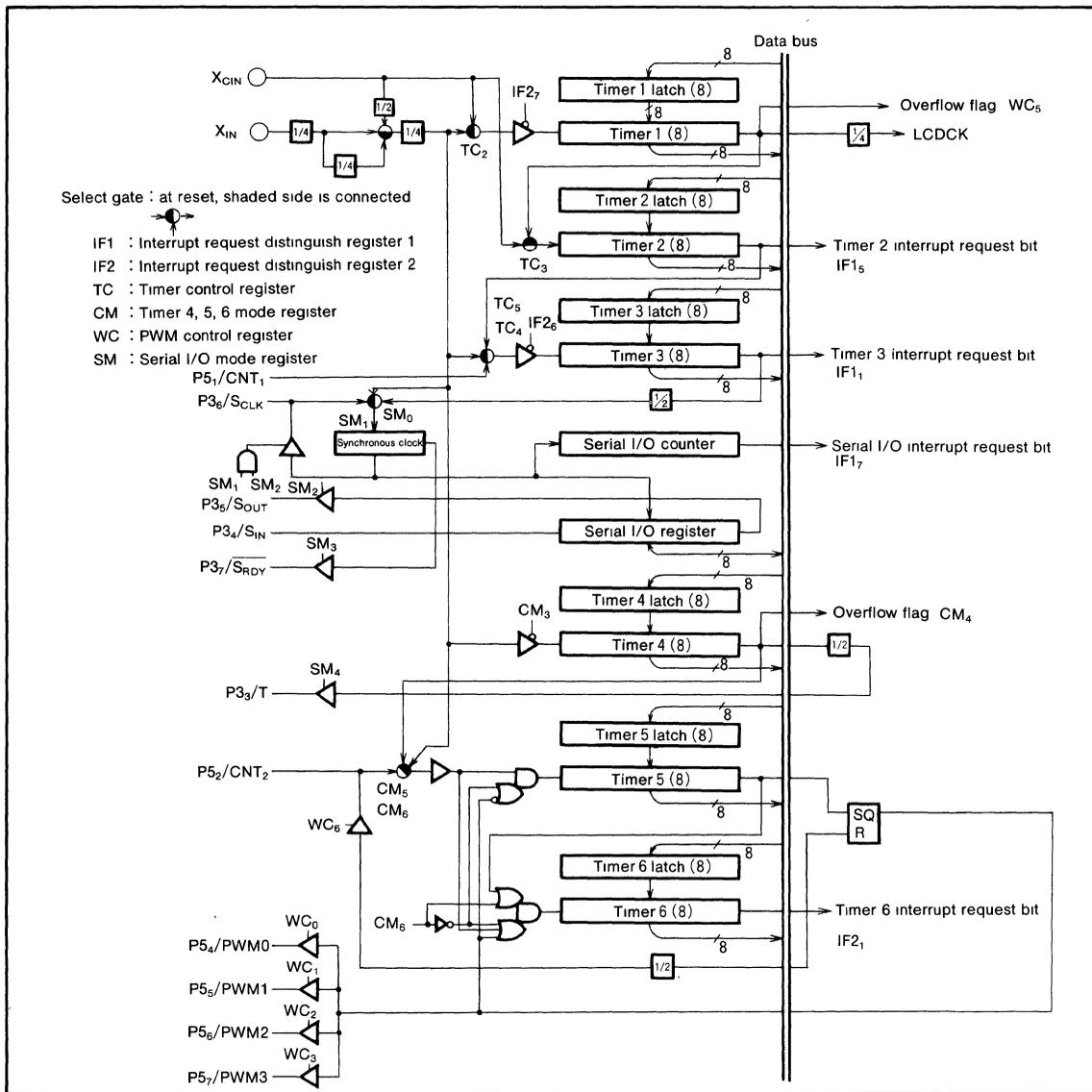


Fig. 4 Block diagram of timer 1 through 6

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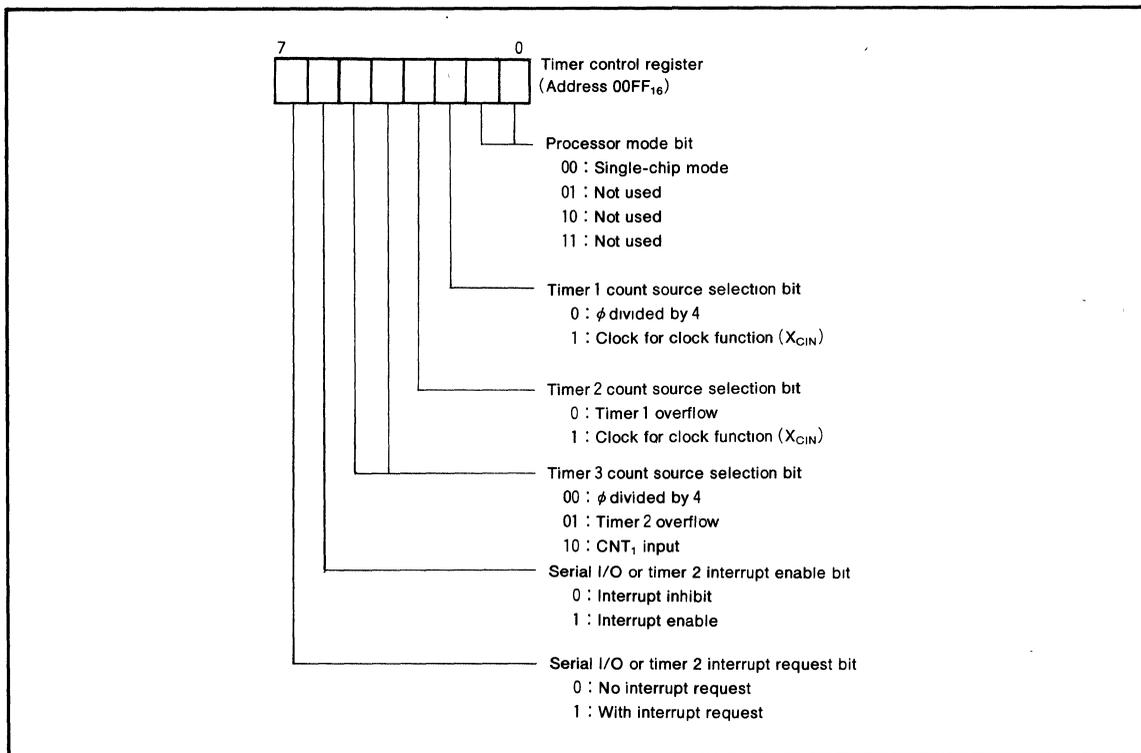


Fig. 5 Structure of timer control register

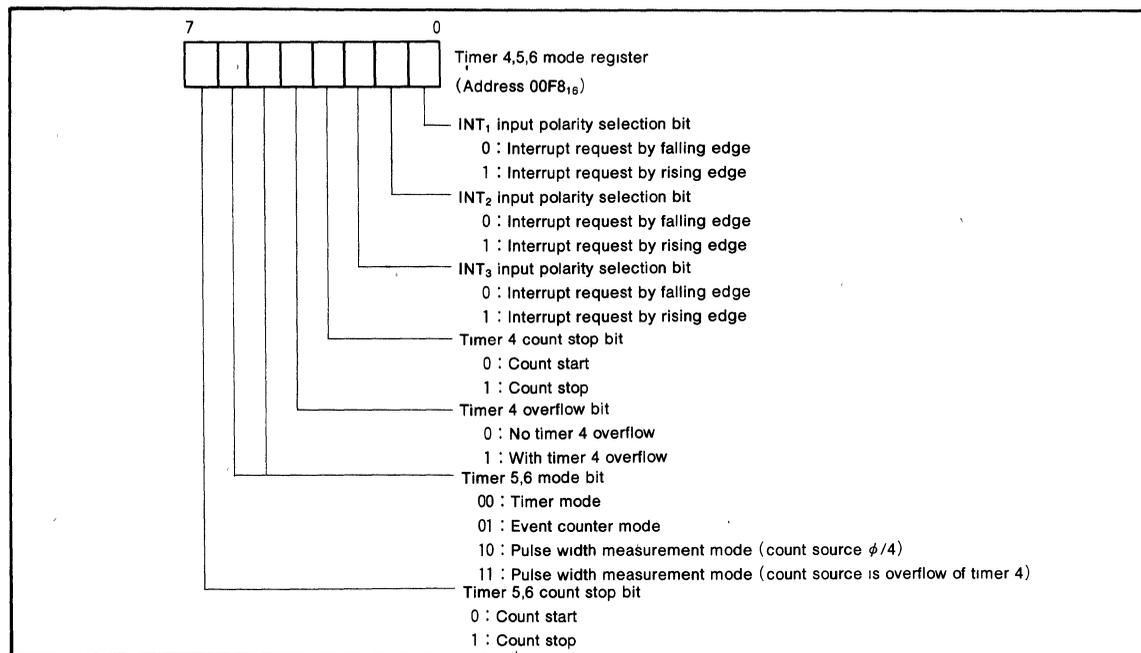


Fig. 6 Structure of timer 4,5,6 mode register

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PWM

M37410M3HXXXFP has a pulse width modulated (PWM) output control circuit connecting with timer5 and timer6.

Figure 6 shows the structure of timer 4,5,6 mode register, Figure 7 shows the PWM rectangular wave form and Figure 8 shows the structure of PWM control register.

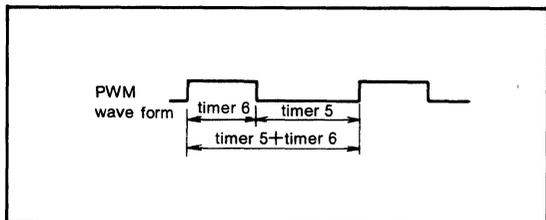


Fig. 7 PWM rectangular wave form

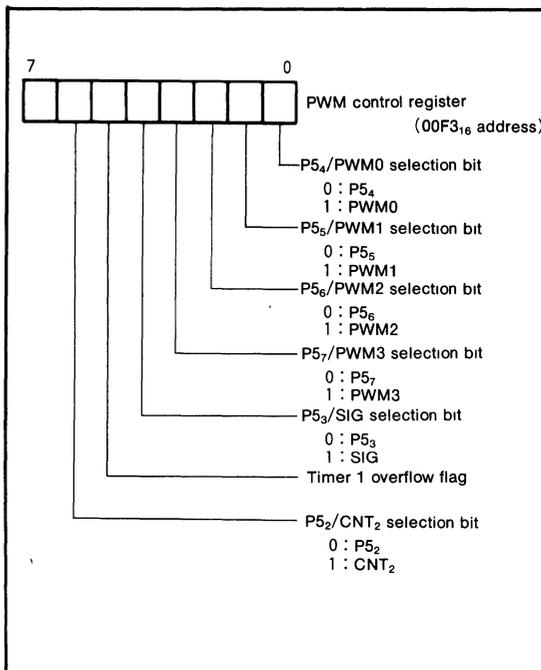


Fig. 8 Structure of PWM control register

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SERIAL I/O

The block diagram of serial I/O is shown in Figure 9. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT} , S_{IN}) pins are used as P3₇, P3₆, P3₅, and P3₄, respectively. The serial I/O mode register (address 00F6₁₆) is an 8-bit register. Bit 1 and 0 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from P3₆ is selected. When these bits are [10], the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are

[11], the internal clock ϕ divided by 4 becomes the clock. Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", P3₅ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P3₅. If the external synchronous clock is selected, the clock is input to P3₆. And P3₅ will be a serial output and P3₄ will be a serial input. To use P3₄ as a serial input, set the directional register bit which corresponds to P3₄, to "0". For more information on the directional register, refer to the I/O pin section. To use the serial I/O, bit 2 needs to be set to "1", if it is "0" P3₆ will function as a normal I/O. Bit 3 determines if P3₇ is

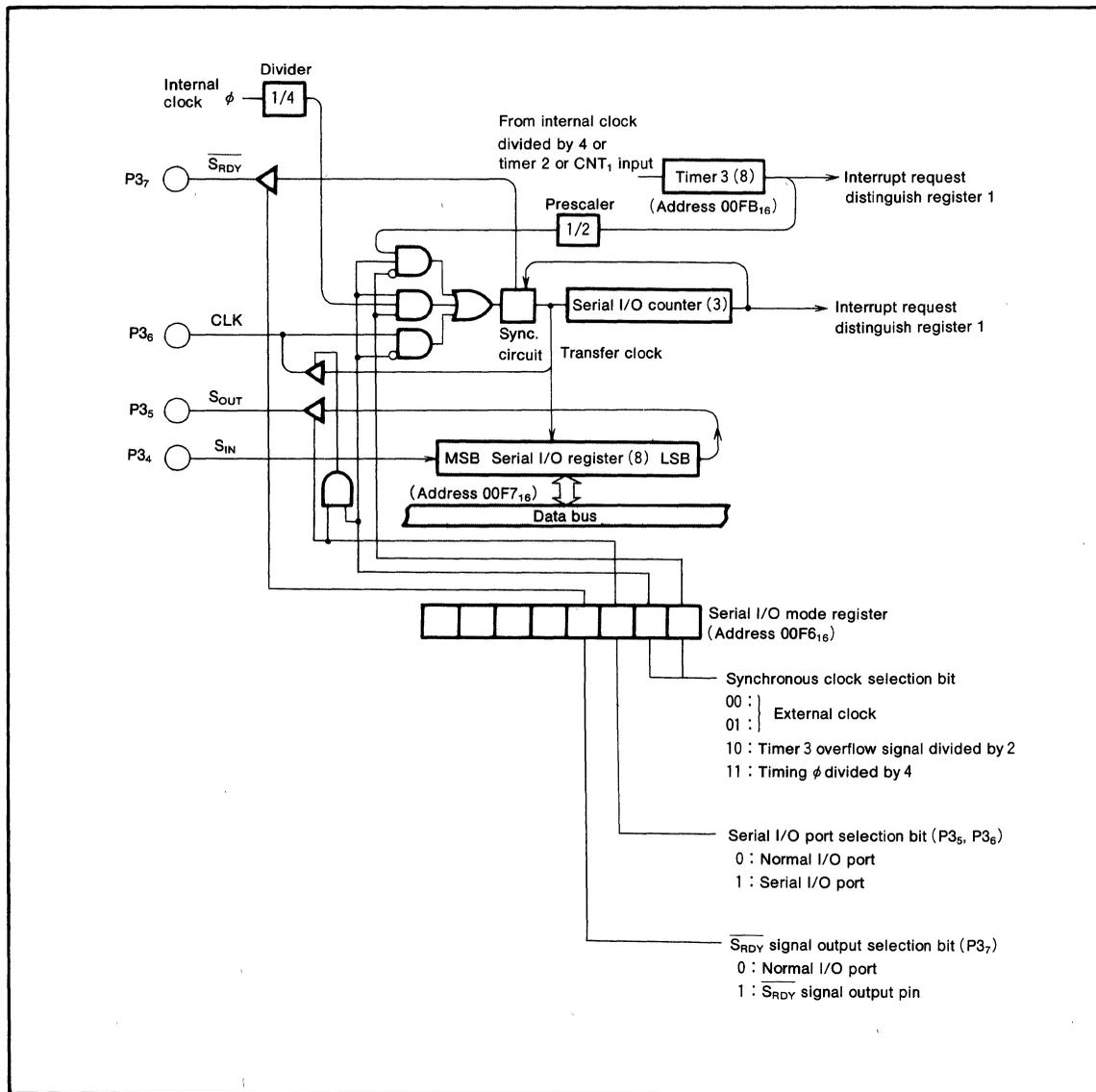


Fig. 9 Block diagram of serial I/O

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used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 3="0").

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock — The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37410M3HXXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to P3₅. During the rising edge of this clock, data can be input from P3₄ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with

the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock — If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. When the external clock is chosen, the P3₈ pin must be held at "H" level while the serial I/O is not used.

Timing diagrams are shown in Figure 10, and connection between two M37410M3HXXXFP's are shown in Figure 11.

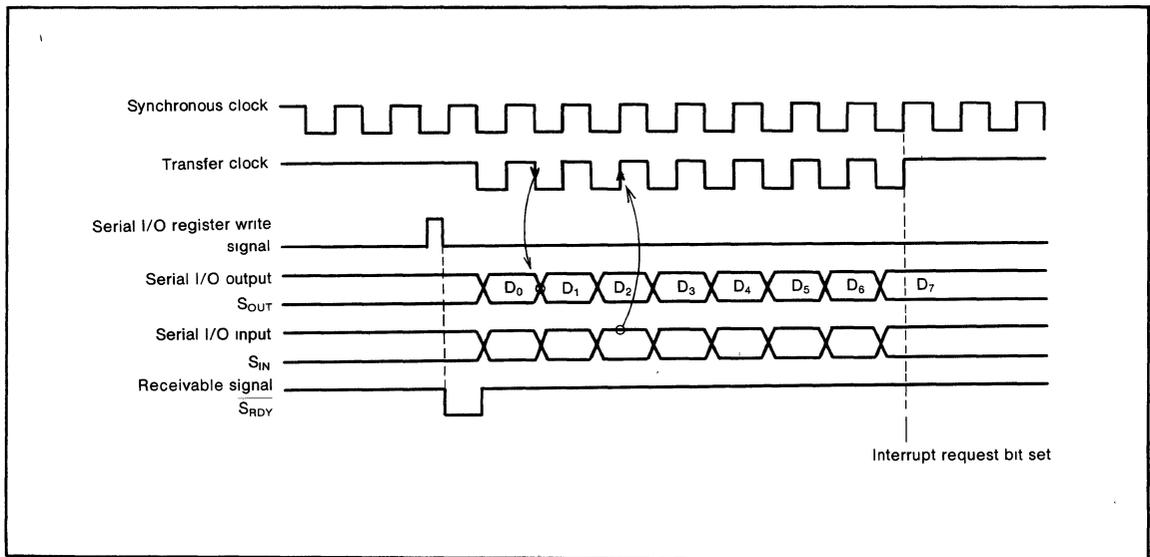


Fig. 10 Serial I/O timing

**M37410M3HXXFP, M37410M4HXXFP
M37410M6HXXFP**

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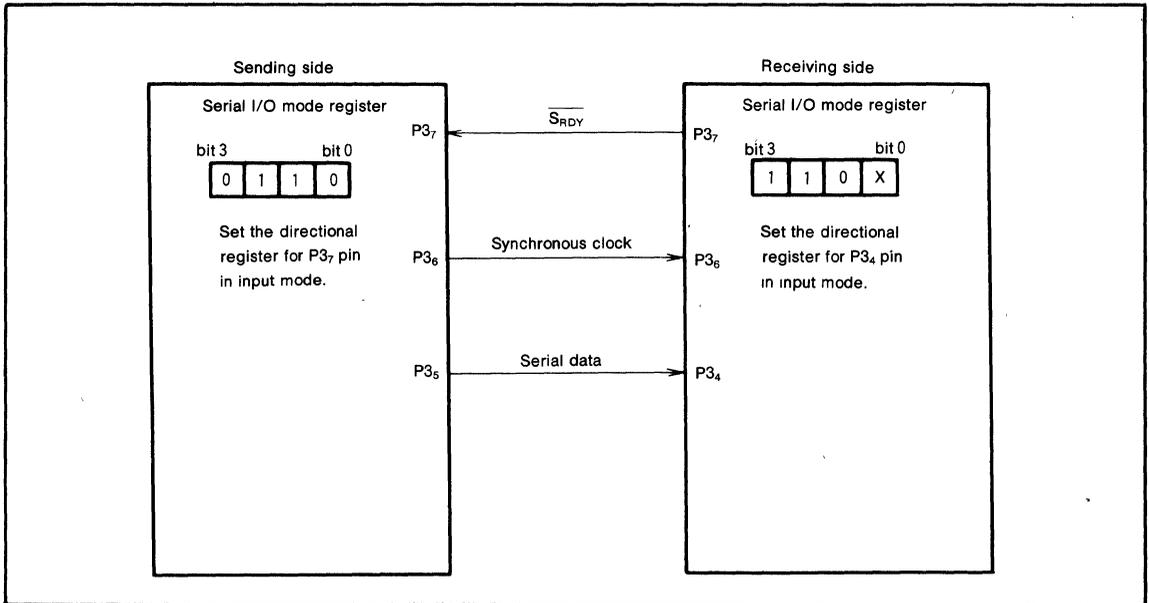


Fig. 11 Example of serial I/O connection

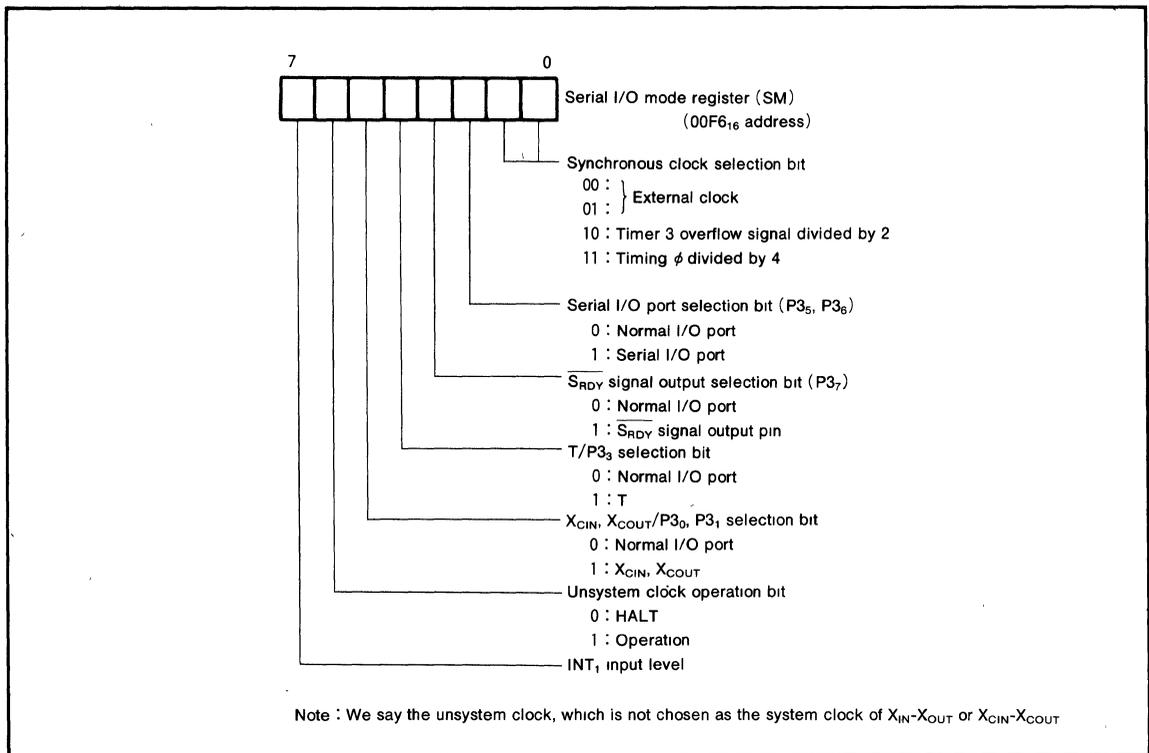


Fig. 12 Structure of serial I/O mode register

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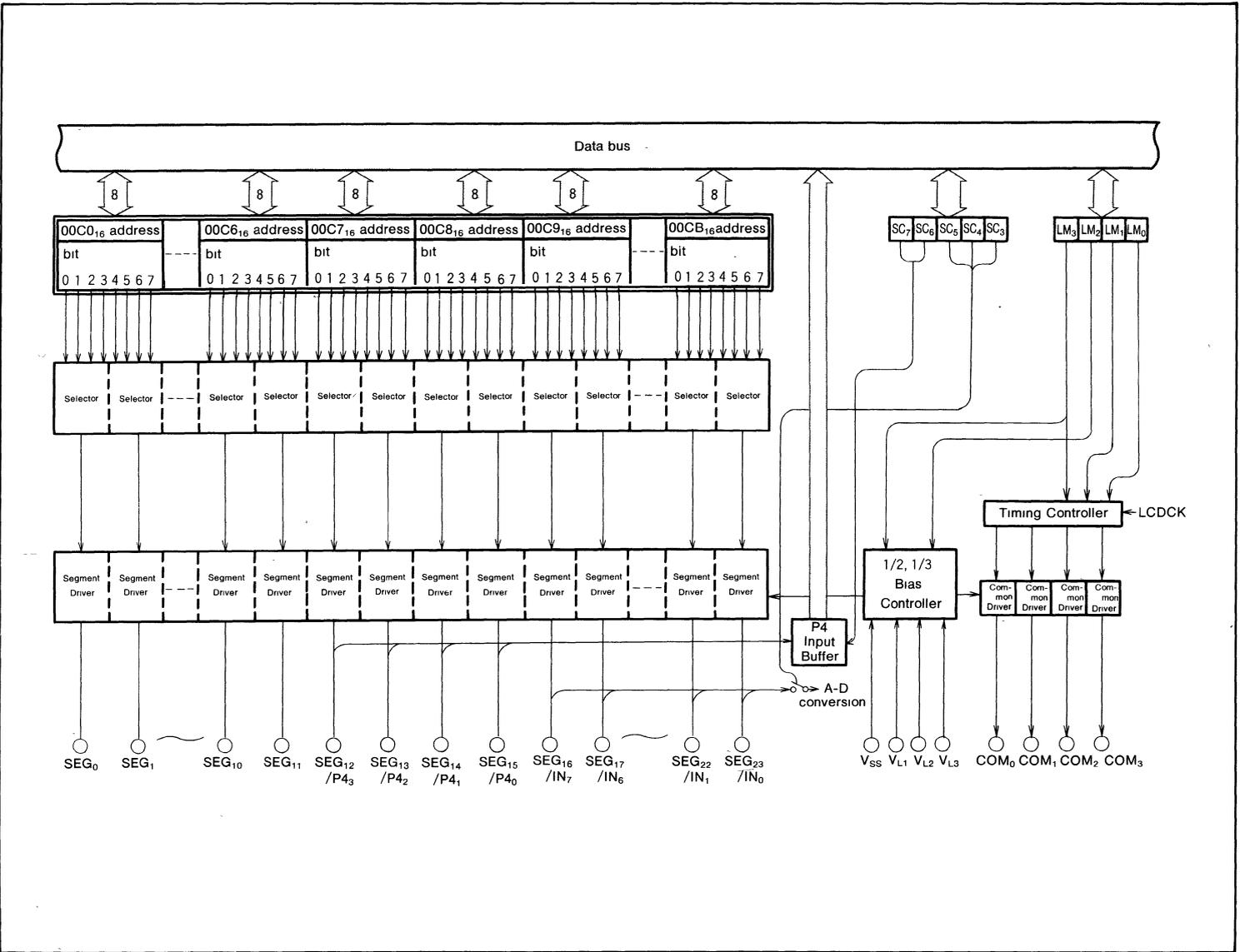


Fig. 15 Block diagram of LCD control circuit



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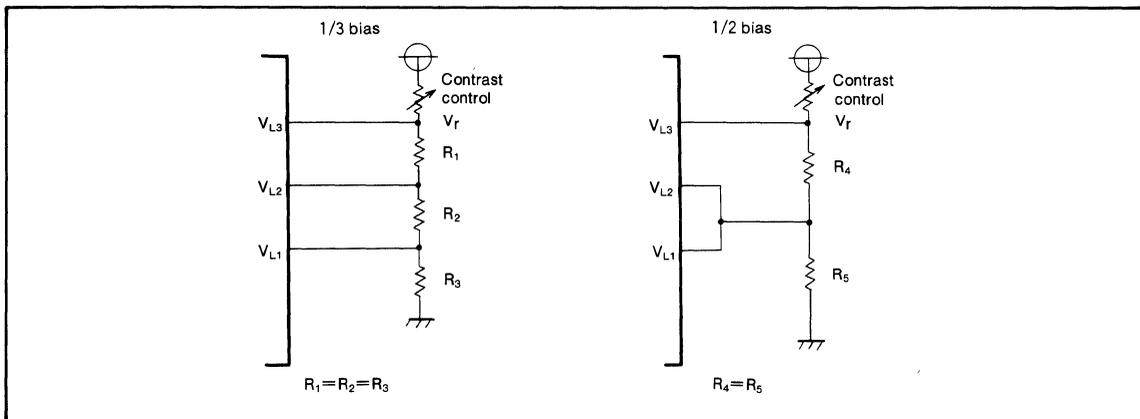


Fig. 16 Example of circuit at 1/3 bias, 1/2 bias

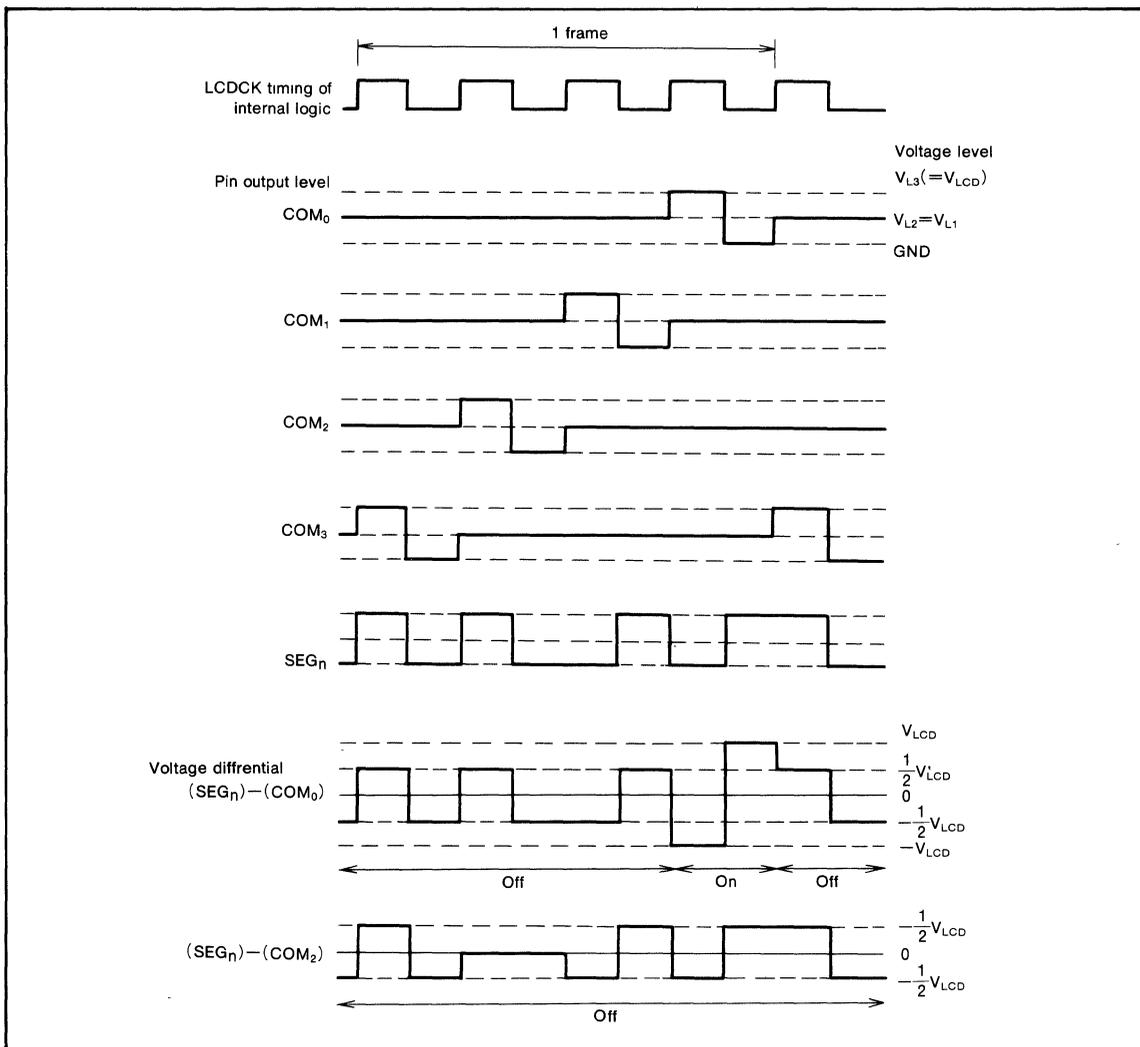


Fig. 17 Example of 1/2 bias, 1/4 duty waveforms and resulting voltage differential between SEG_n and COM_n .

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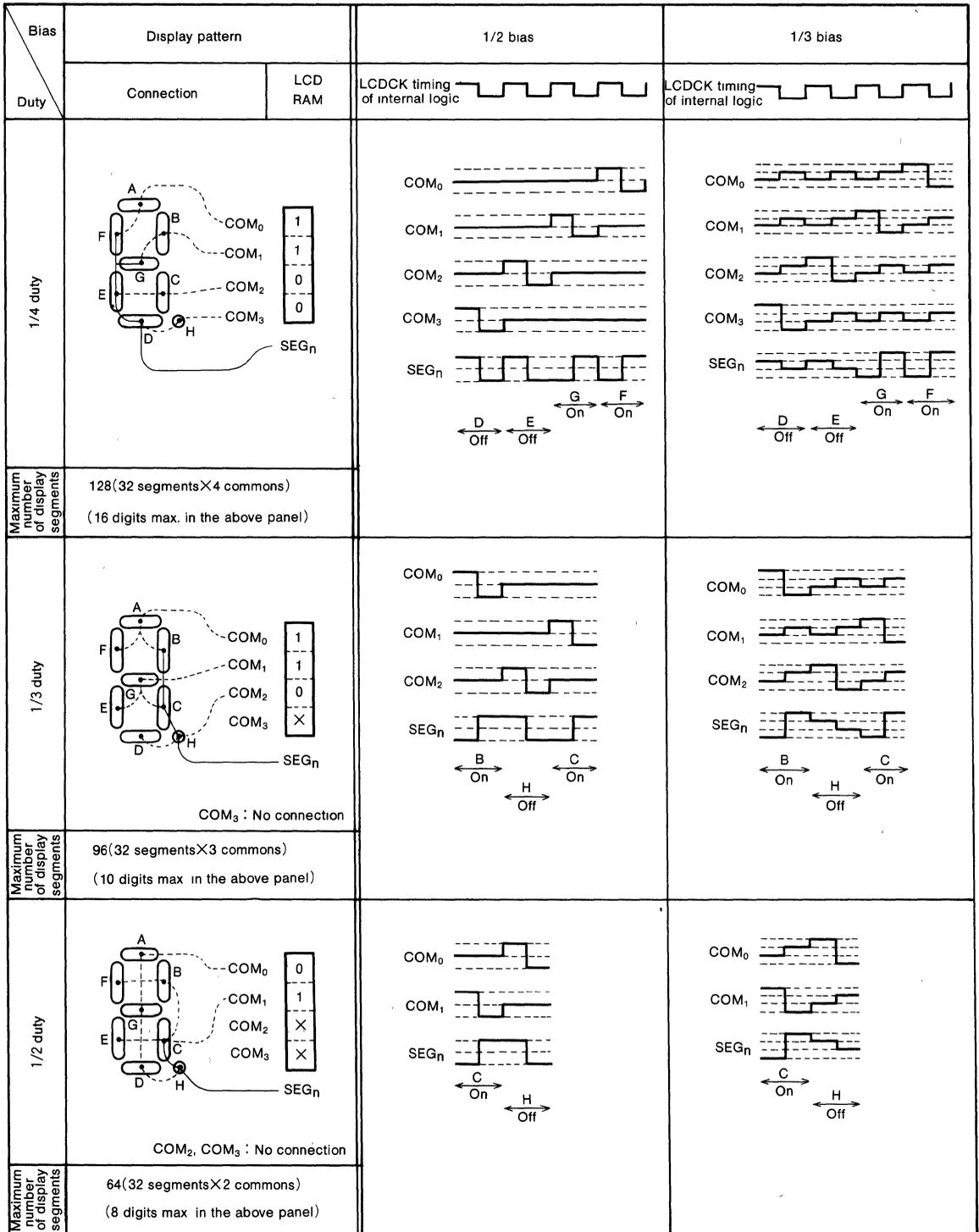


Fig. 18 Example of drive waveforms for each bias and duty

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A-D CONVERTER

The A-D converter circuit is shown in Figure 20. The analog input ports of the A-D converter (IN₀~IN₇) are in common with the segment output ports.

The segment control register is located at address 00F4₁₆. One of the eight analog inputs is selected by bits 0, 1 and 2 of this register. The IN pins, not to use as analog input, uses as LCD segment output.

Bit 0, 1 and 2, and corresponding to analog input pin is shown in Figure 19. A-D conversion is accomplished by first selecting bit 0 and 1 of the A-D control register (address 00F2₁₆) for the source of V_{REF}. And also the analog input pin is chosen by the analog input select bit of the segment control register. A-D conversion starts by writing a dummy data to the A-D register (address 00EF₁₆) or changing the input level from SIG pin "H" to "L". When A-D conversion is finished, an interrupt is generated. After A-D interrupt is accepted, the result of A-D conversion can be read from the A-D register.

Note that the A-D conversion must be started to convert, after the reference voltage reaches stable level.

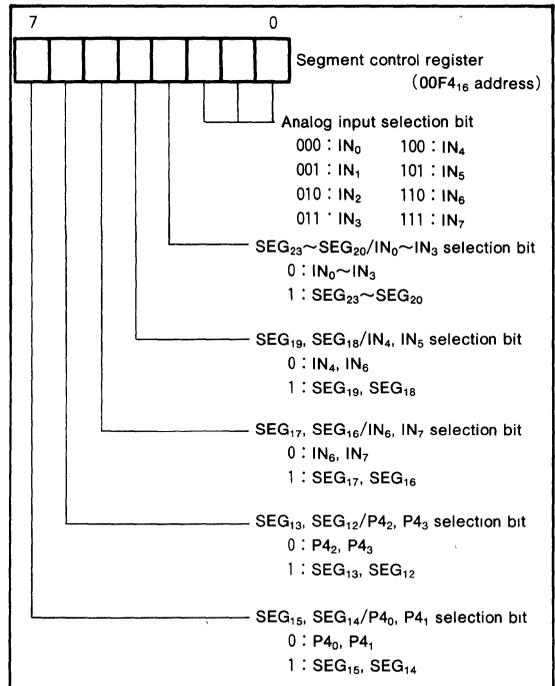


Fig. 19 Structure of segment control register

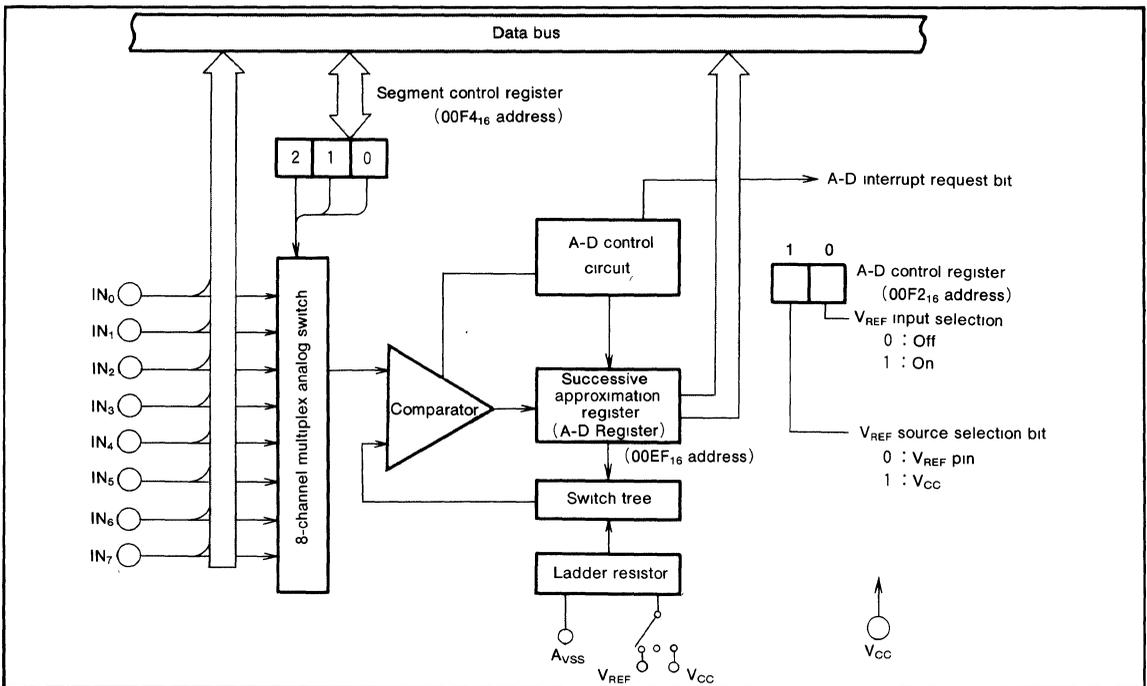


Fig. 20 A-D converter circuit

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KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction.

When the key on wake up option of port P2 is designated and key on wake up interrupt enable bit (IC_4) is set to "1", if the key on wake up option pin of port P2 has "L" level applied, key on wake up interrupt is generated and the microcomputer is returned to the normal operating state.

When the bit 4 of PWM control register (address $00F3_{16}$) is set to "1", the pulse shown in Figure 21 is outputted from $P5_3$ pin.

As shown in Figure 22, if the key matrix of active "L" to input port P2 is constructed, the microcomputer is returned to normal operating state by the key push. Refer to the section of interrupt how to use the key on wake up function. In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and IC_4 is "1", the input designated as key on wake up by option in port P2 must be all "H".

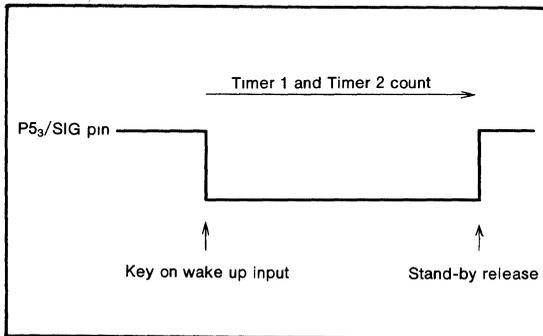


Fig. 21 Output from the SIG pin at wake up from the stop state

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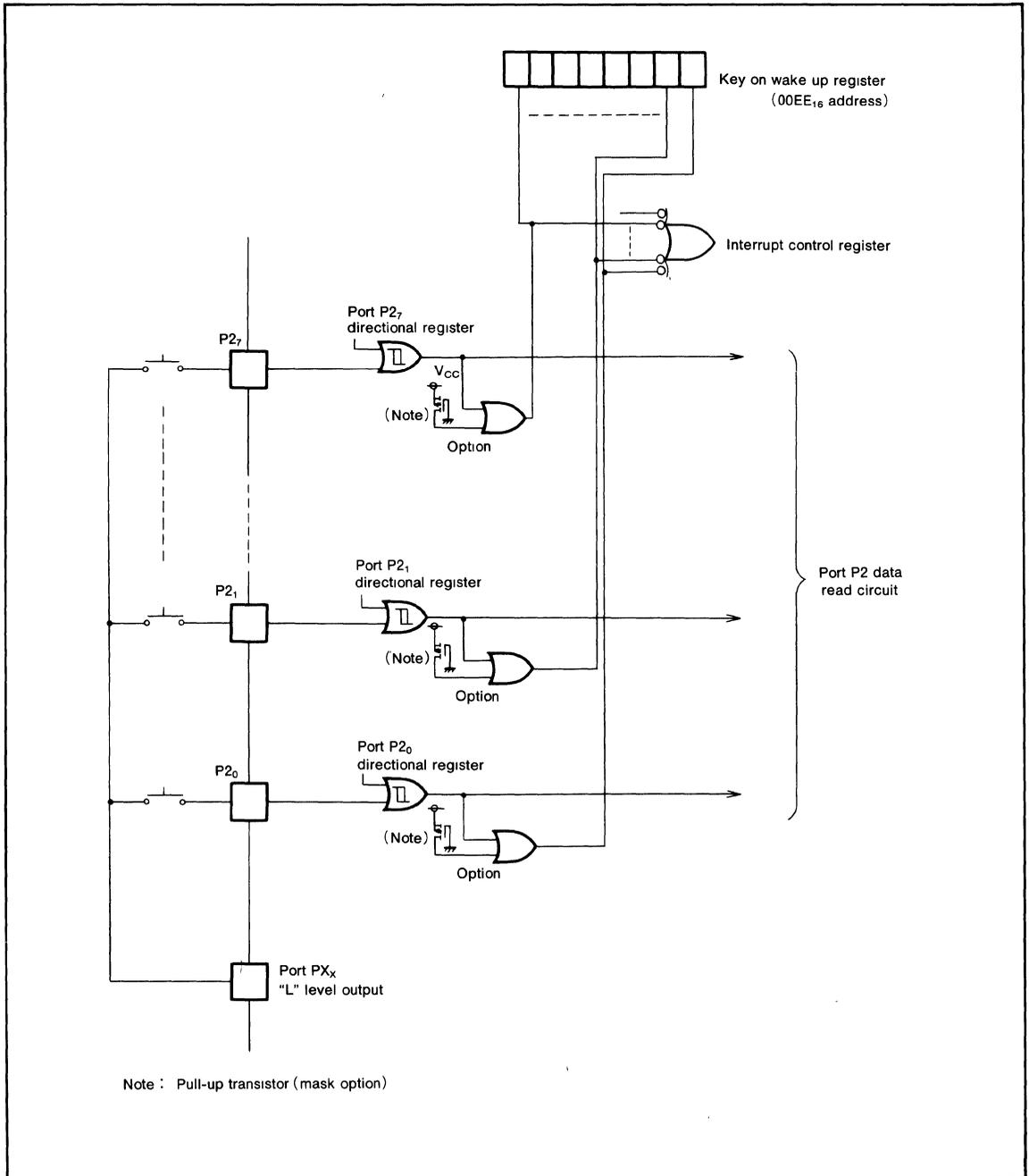


Fig. 22 Block diagram of port P2, and example of wired at used key on wake up

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RESET CIRCUIT

The M37410M3HXXXFP is reset according to the sequence shown in Figure 25. It starts the program from the address formed by using the content of address $3FFF_{16}$ as the high order address and the content of the address $3FFE_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than $16 \mu\text{s}$ while the power voltage is between 4 and 5.5V and the crystal oscillator oscillation is stable and

then returned to "H" level.

The internal initializations following reset are as shown in Figure 23 regardless of the status before reset (including stop mode or wait mode).

An example of the reset circuit is shown in Figure 24.

When the power on reset is used, the $\overline{\text{RESET}}$ pin must be input "H" after the oscillation of $X_{\text{IN}}-X_{\text{OUT}}$ becomes stable.

		Address
(1)	Port P0 directional register (D0) ($E1_{16}$)	00_{16}
(2)	Port P1 directional register (D1) ($E3_{16}$)	00_{16}
(3)	Port P2 directional register (D2) ($E5_{16}$)	00_{16}
(4)	Port P3 directional register (D3) ($E9_{16}$)	00_{16}
(5)	Port P5 directional register (D5) (ED_{16})	00_{16}
(6)	Interrupt request distinguish register 1 (IF1) (EB_{16})	00_{16}
(7)	Interrupt request distinguish register 2 (IF2) (FO_{16})	00_{16}
(8)	PWM control register (WC) ($F3_{16}$)	0 0 0 0 0 0 0 0
(9)	Segment control register (SC) ($F4_{16}$)	0 0 0 0 0 0 - - - -
(10)	LCD mode register (LM) ($F5_{16}$)	00_{16}
(11)	Serial I/O mode register (SM) ($F6_{16}$)	- - 0 0 0 0 0 0 0 0
(12)	Timer 4, 5, 6 mode register (CM) ($F8_{16}$)	00_{16}
(13)	Interrupt control register (IM) (FE_{16})	00_{16}
(14)	Timer control register (TC) (FF_{16})	00_{16}
(15)	A-D control register (AC) ($F2_{16}$)	- - - - - 0 0
(16)	Processor status register	- - - - - 1 - - - -
(17)	Program counter (PC_H)	Contents of address $3FFF_{16}$
	(PC_L)	Contents of address $3FFE_{16}$

Note Since the contents of both registers other than those listed above (including timers and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

Fig. 23 Internal state of microcomputer at reset

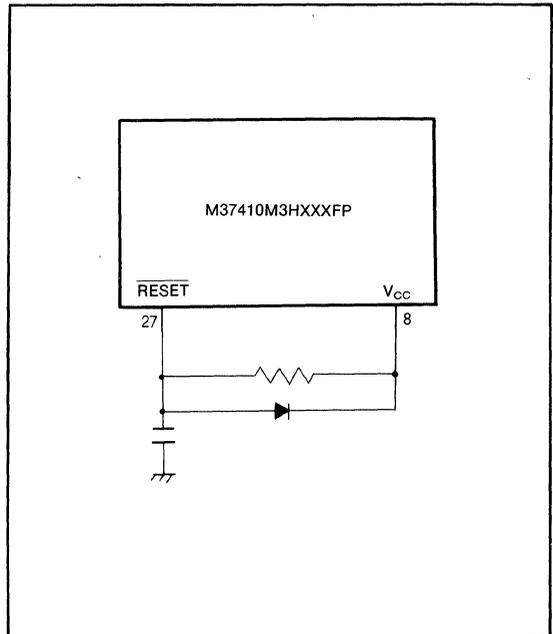


Fig. 24 Example of reset circuit

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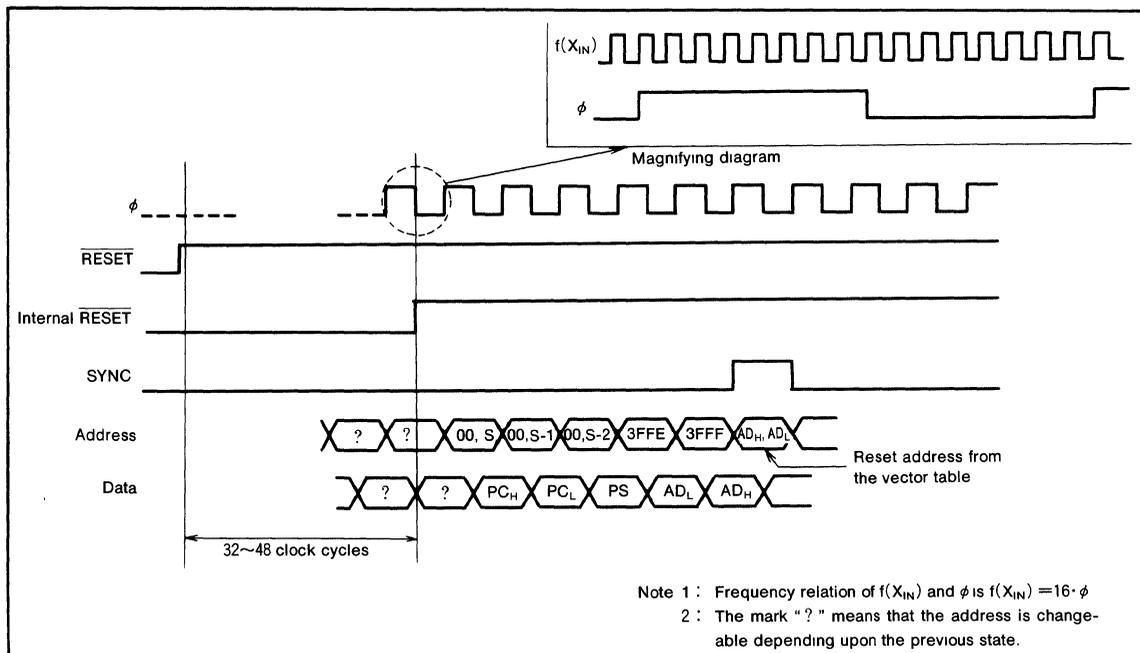


Fig. 25 Timing diagram at reset

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I/O PORTS

- (1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address 00E0₁₆. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address 00E1₁₆) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state. This port can be built in a pull-up resistor option when it is used as a input port.
- (2) Port P1

Port P1 has the same function as P0 but the output structure is N-ch open drain. This port can be built in a pull-up resistor option when it is used as a input port.
- (3) Port P2

Port P2 has the same function as P0. The output structure is CMOS output. Following the execution of STP or WIT instruction, key matrix with port P2 can be used to generate the interrupt to bring the microcomputer back in its normal state. The pin to be used as the key on wake up must be with key on wake up option and its value in directional register must be "0". When P2 is used as a output port, pull-up option is inhibited.
- (4) Port P3

Port P3 has the same functions P0 except that part of P3 is common with the serial I/O, output of timer4, clock oscillation of timer clock and interrupt input. The output is N-channel open drain. This port can be built in a pull-up resistor option. When P3₀ and P3₁ pins are used for X_{CIN} input, pull-up is inhibited.
- (5) Port P4

Port P4 is an 4-bit input port which can be used as a segment output port. At reset, this port is pull-up to V_{L3}. Just after the reset, this port becomes high-impedance state. When port P4 is used as a segment output port, the pull-up option to these pins are inhibits.
- (6) Port P5

Port P5 has the same functions as P0 except that part of P5 is common with the counter input pin, SIG pin, and PWM output pin. The output is N-channel open drain output. This port can be built in a pull-up resistor option.
- (7) Segment output(SEG₀~SEG₁₁)

These ports drive and control the LCD segments. At reset, these output the level of V_{L3}.
- (8) Analog input(IN₀~IN₇)

This is a port for an analog input of A-D converter. This can be used as the segment output. At reset, it is pull-up to V_{L3}. Just after the reset, this becomes high-impedance state.
- (9) Common output(COM₀~COM₃)

These port provides output drive and control for the LCD common lines. At reset, this outputs the level of V_{L3}.
- (10) Power Supply for LCD(V_{L1}~V_{L3})

Supplies power to the LCD terminals.
- (11) INT₁

The INT₁ pin is an interrupt input pin. The INT₁ interrupt request bit (bit 7 of address 00FE₁₆) is set to "1" when the input level of this pin changes from "H" to "L" (or "L" to "H"). This input level is read in the bit 7 of serial I/O mode register (addresss 00F6₁₆).
- (12) INT₂(P3₂/INT₂)

The INT₂ pin is an interrupt input pin common with P3₂. When P3₂'s directional register is set for input ("0"), this pin can be used as an interrupt input. The INT₂ interrupt request bit (bit 3 of address 00EB₁₆) is automatically set to "1" when the input level of this pin changes from "H" to "L" (or from "L" to "H").
- (13) INT₃(P5₀/INT₃)

The INT₃ pin is an interrupt input pin common with P5₀. The other functions are the same as INT₂.

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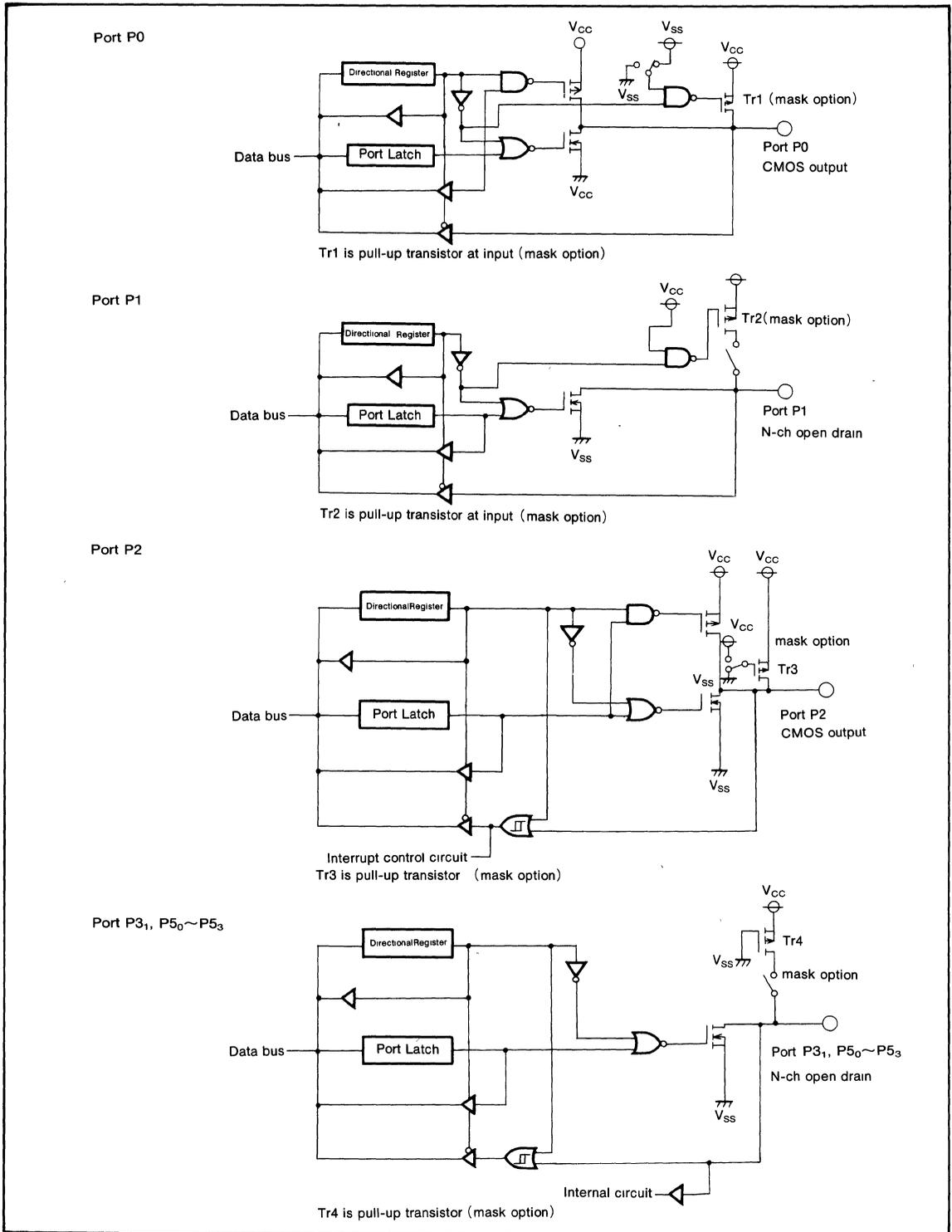


Fig. 26 Block diagram of ports P0~P2, P3₁ and P5₀~P5₃

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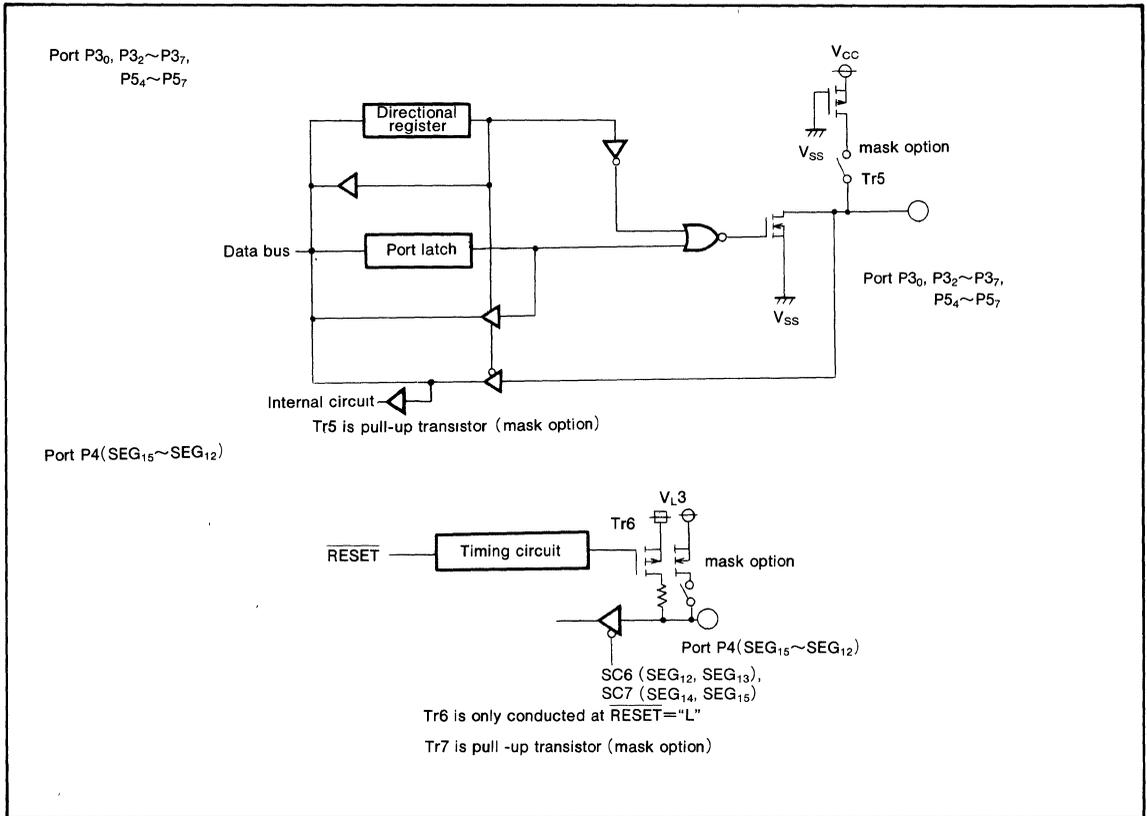


Fig. 27 Block diagram of Port P3₀, P3₂~P3₇, P4, P5₄~P5₇

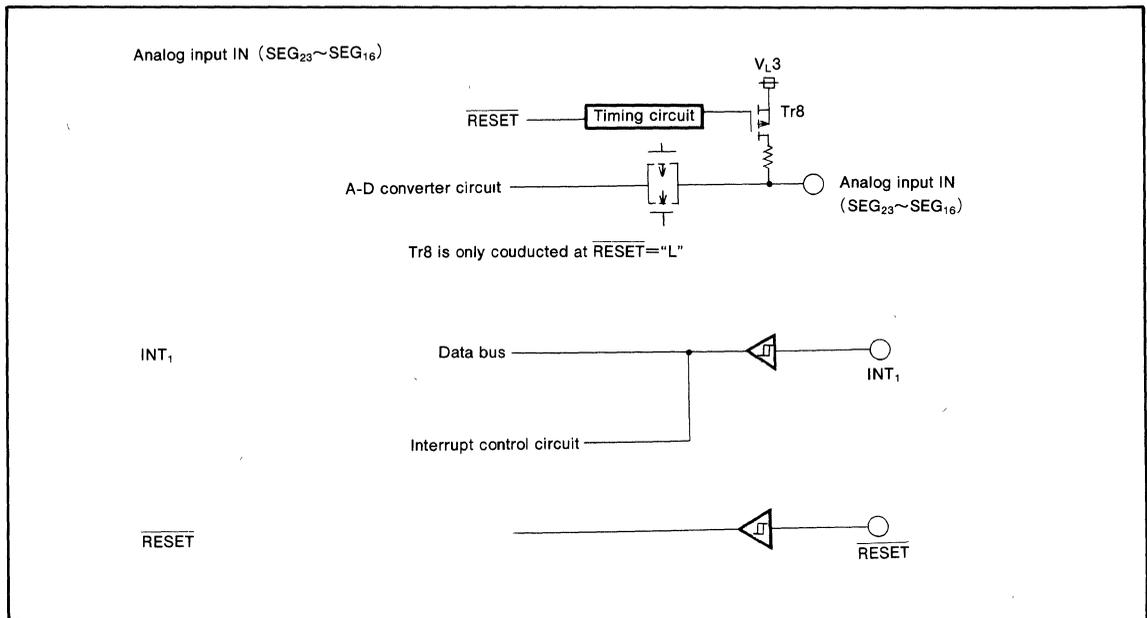


Fig. 28 Block diagram of analog input port IN, INT₁, RESET

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CLOCK GENERATING CIRCUIT

The M37410M3HXXXFP has two internal clock generators. Figure 31 shows a block diagram of the clock generator. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ . Serial I/O mode register bit 5 can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN} . In this case, the pull-up option to these pins are inhibited.

These signals can also be changed via bit5 (LM_5) and bit6 (LM_6) of the LCD mode register. When LM_6 and LM_5 are [00], the internal clock is chosen $X_{IN}/16$. When they are [01], the internal clock is chosen $X_{IN}/4$. When they are [10] and [11], the internal clock is $X_{CIN}/2$. The one of clock X_{IN} and clock X_{CIN} , isn't in use for the internal clock (none system clock), stops when the bit6 (SM_6) of serial I/O mode register is "0". In order to restart the clock as the internal clock, SM_6 is set to "1" and wait until the oscillation becomes stability by the software then the internal clock is chosen LM_6 and LM_5 .

Figure 29 shows a circuit exmple using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which is unique for each oscillator. when using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 30.

The M37410M3HXXXFP has two low power consumption modes, stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. When restarting oscillation, set the suitable value for timer 1 and timer 2 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), timer 2 interrupt enable bit ($IF1_4$) of interrupt request distinguish register 1 must be set to enable ("1"), timer 2 interrupt request bit ($IF1_5$) of interrupt request distinguish register must be set to disable ("0"). And serial I/O or timer 2 interrupt enable bit (TM_6) and serial I/O or timer 2 interrupt request bit (TM_7) of timer control register must be set to disable ("0").

Oscillation is restarted (reset stop mode) when INT_1 , INT_2 , or INT_3 interrupt is received. The interrupt enable bit of the interrupt used to reset the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 2 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be applied to the RESET pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode reset) when the processor is reset or when it receives an

interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

When the interrupt is accepted and after the interrupt subroutine is executed, the next instruction to STP or WIT is executed. It is possible to cancel stop and wait mode by reset. In this case, the execution is started from the address is set to reset vector.

Transition of states for the system clock is shown in Figure 32. The change order of the internal clock is shown in Figure 32.

When STP instruction is executed from the states of A, B, C, D and E, it will be the same state as H (stop state). If the interrupt is executed in stop state, it will return the state before STP instruction is executed.

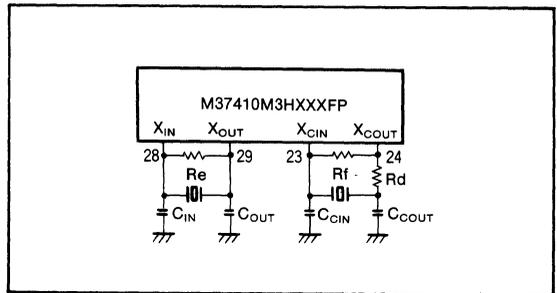


Fig. 29 External ceramic resonator circuit

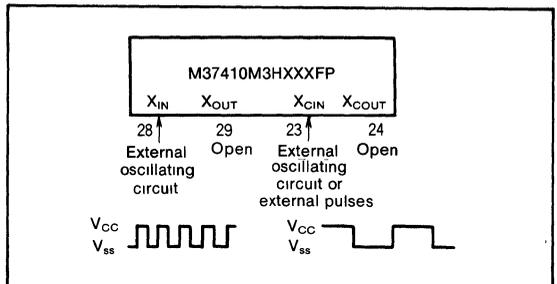


Fig. 30 External clock input circuit

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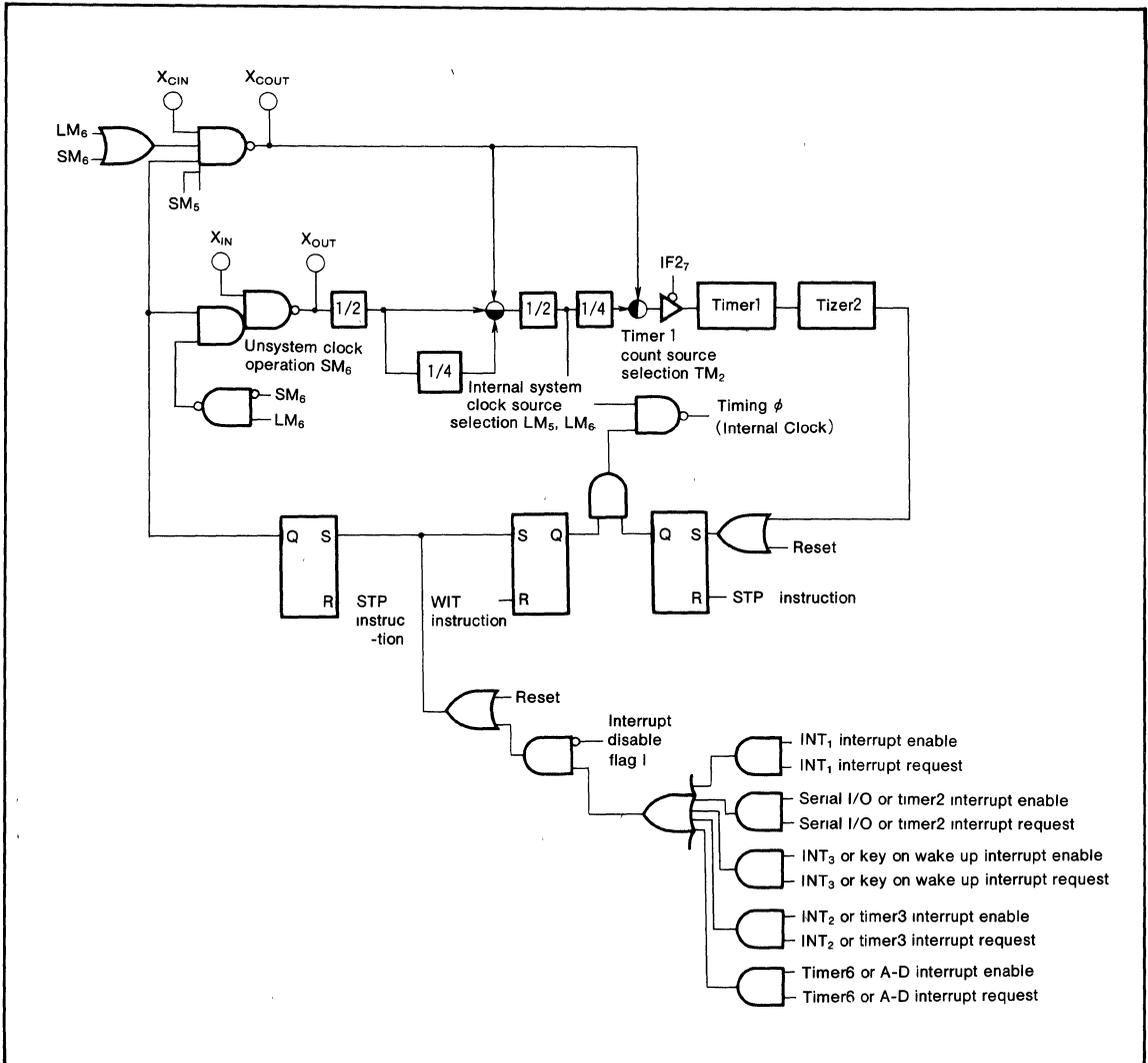
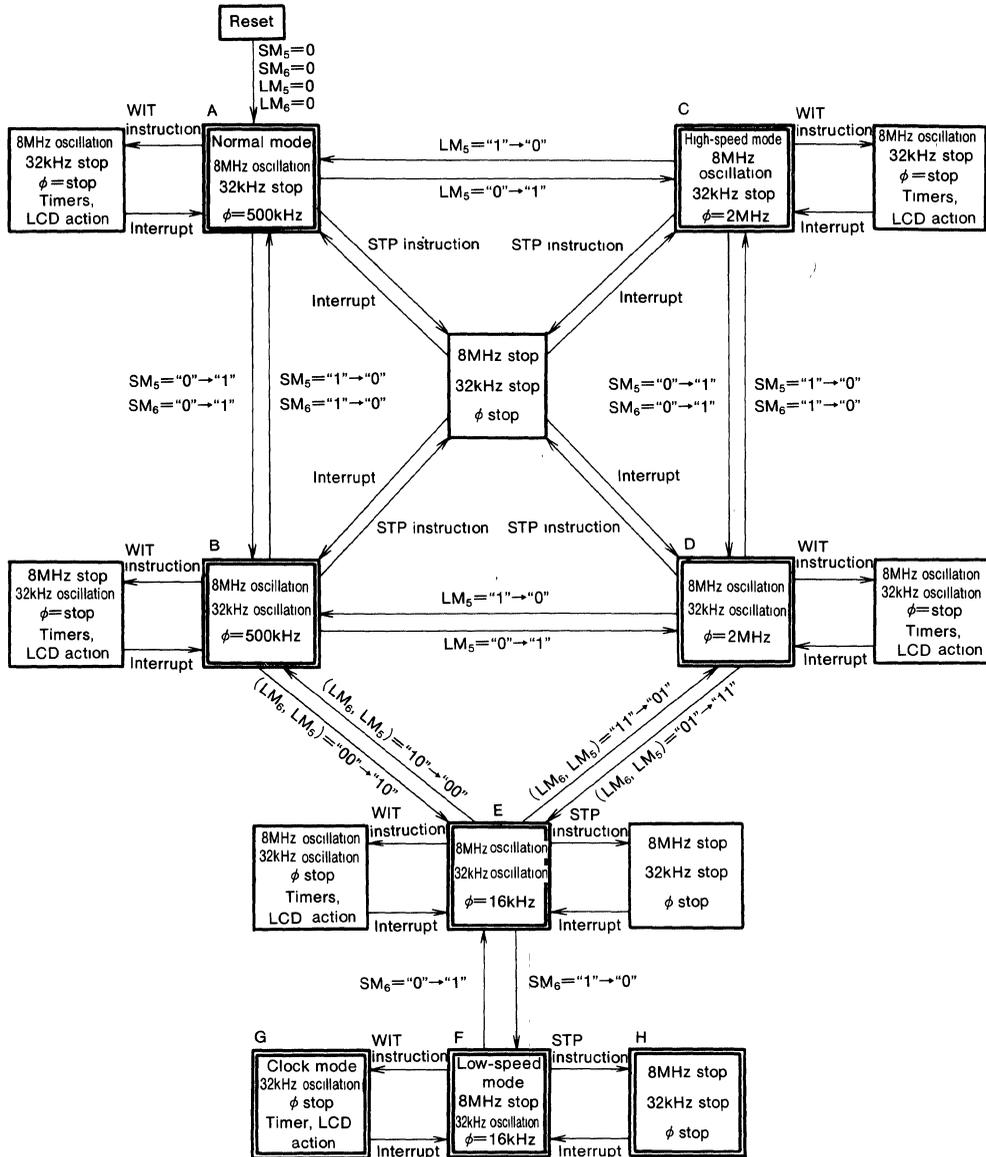


Fig. 31 Block diagram of clock generating circuit

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The case of example clock X_{IN}=8MHz, clock X_{CIN}=32kHz

- Note :** At the end of STP instruction, wait time occurs automatically by connection of timers 1 and 2 and changing system clock. This time is set by program.
- When SM₆=1 and unsystem clock is operated, wait time necessary by program until oscillation becomes stable.
 - Return to the normal mode once in case changed to the low-speed-mode from the normal mode.
 - Also return to the high-speed mode once in case changed to the low-speed mode from the high-speed mode.

Fig. 32 Transition of states for the system clock

PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) The count value of timers 1, 2, 3, 4 can be read at an arbitrary timing when the timing ϕ divided by 4 or timer overflow is input to these timers. If X_{CIN} or CNT_1 input is input to these timers, the value of timer 1, 2, 3, 4 must be read only when the input of timers is not changing or the timer count is stopped.

Also the count value of timers 5, 6 which are used in the event counter mode must be read when the external input is at the "L" level. When timers 5, 6 are used in the timer mode, the count value of these timers cannot be read.

- (3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(4) ① After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

② In decimal mode, the negative (N), overflow (V) and zero (Z) flags are invalidated.

- (5) A NOP instruction must be used after the execution of a PLP instruction.

(6) ① The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.

Also the following conditions must be satisfied:

- Timer 1 count stop bit is set to "0"
- Timer 2 interrupt enable bit is set to "1"
- Timer 2 interrupt request bit is set to "0"
- Serial I/O or timer 2 interrupt enable bit is set to "0"
- Serial I/O or timer 2 interrupt request bit is set to "0"

② To restart oscillation when it is stopped by STP instruction or unsystem clock operation bit, wait for a specified time which is needed for the oscillator to stabilize.

- (7) Some instructions can be used to write contents of the interrupt request distinguish register 1, 2. If the SEB or CLB instruction or a set of instruction that acts as the SEB or CLB instruction (for instance, LDA TC+SEB 7, A+STA TC) is used, an interrupt request which is input during execution of these instructions may be cleared. Therefore, these instructions should be used only when there is no problem even if such an interrupt request is cleared. Usually, the LDM instruction or STA instruction is used. Especially to write contents of the interrupt request distinguish register 1, 2, use the flow chart as shown in Figure 33.

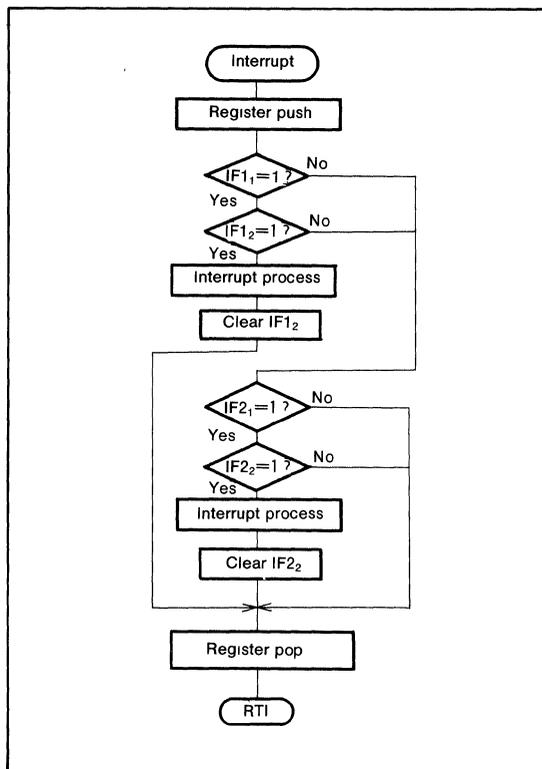


Fig. 33 Flow to write interrupt request distinguish registers

- (8) When LCD trun-on bit (bit 3 of address 00F5₁₆) of the LCD mode register is "1", don't stop the timers or count source for timers.
- (9) After switching the serial I/O transfer clock, initialize the serial I/O counter (write to address 00F7₁₆).
- (10) To use an external clock as the serial I/O transfer clock, initialize the serial I/O counter when the external clock is "H" level.
- (11) To use the P3₀ and P3₁ pins as the I/O pins of the clock for clock function, do not use the pull-up resistors by option.
- (12) If using A-D converter, supply power to the V_{REF} pin (set bits 1 and 2 of address 00F2₁₆), and make sure that the voltage of the V_{REF} pin has stabilized before activating the A-D conversion.

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DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-up transistor bit
- Port P5 pull-up transistor bit
- Port P2 key on wake up

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3~7	V
V_I	Supply voltage for LCD $V_{L1}\sim V_{L3}$	$V_{L1} < V_{L2} < V_{L3}$	-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage $P0_0\sim P0_7, P2_0\sim P2_7, P3_0, P3_1, P4_0\sim P4_3, IN_0\sim IN_7, V_{REF}, X_{IN}$		-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage CNV_{SS}		-0.3~7	V
V_I	Input voltage $INT_1, \overline{RESET}, P1_0\sim P1_7, P3_2\sim P3_7, P5_0\sim P5_7$ (Note 1)		-0.3~10	V
V_O	Output voltage $P0_0\sim P0_7, P2_0\sim P2_7, P3_0, P3_1, COM_0\sim COM_3, SEG_0\sim SEG_{23}, X_{OUT}$		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage $P1_0\sim P1_7, P3_2\sim P3_7, P5_0\sim P5_7$		-0.3~10	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	300	mW
T_{opr}	Operating temperature		-20~75	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~125	$^\circ\text{C}$

Note 1 : When these ports are built in a pull-up resistor option, the value is $-0.3\sim V_{CC}+0.3\text{V}$

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=2.5\sim 5.5\text{V}$, $V_{SS}=0\text{V}$, $T_a=-20\sim 75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage (Note 1)	$f(X_{IN})=8\text{MHz}$ High-speed mode	4.5		5.5	V
		$f(X_{IN})=8\text{MHz}$ Normal mode or	2.5		5.5	
		$f(X_{IN})=2\text{MHz}$ High-speed mode (Note 2)				
V_{SS}	Supply voltage		0		V	
V_{IH}	"H" input voltage $P0_0\sim P0_7, P3_0, P3_1, P4_0\sim P4_3, X_{IN}, CNV_{SS}$ (Note 3)		$0.7V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $P2_0\sim P2_7$		$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $P1_0\sim P1_7, P5_1\sim P5_7, S_{IN}$		$0.7V_{CC}$		10	V
V_{IH}	"H" input voltage $P3_2\sim P3_7, P5_0, INT_1, INT_2, INT_3, CNT_1, CNT_2, SIG, CLK$		$0.8V_{CC}$		10	V
V_{IH}	"H" input voltage $\overline{RESET}, X_{CIN}$		$0.85V_{CC}$		10	V
V_{IL}	"L" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P3_0, P3_1, P4_0\sim P4_3, P5_1\sim P5_7, S_{IN}$		0		$0.25V_{CC}$	V
		"L" input voltage $P2_0\sim P2_7, P3_2\sim P3_7, P5_0, INT_1, INT_2, INT_3, CNT_1, CNT_2, SIG, CLK$		0		$0.2V_{CC}$
V_{IL}	"L" input voltage $\overline{RESET}, X_{IN}, X_{CIN}$		0		$0.15V_{CC}$	V
I_{OH}	"H" output current $P0_0\sim P0_7, P2_0\sim P2_7, X_{OUT}$ (Note 4)				-1	mA
I_{OL}	"L" output current $P0_0\sim P0_7, P2_0\sim P2_7, P3_0\sim P3_7, P5_0\sim P5_7, X_{OUT}, PWM_0\sim PWM_3, T, S_{OUT}, CLK, S_{RDY}, SIG$ (Note 5)				1	mA
		"L" output current $P1_0\sim P1_7$ (Note 6)	$V_{CC}=3\text{V}$		10	mA
		$V_{CC}=5\text{V}$		20		
$f(X_{IN})$	Clock oscillating frequency		0.2		8.2	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function		30		50	kHz

Note 1 : When only maintaining the RAM data, minimum value of V_{CC} is 2V

2 : We say the high-speed mode, when the system clock is chosen $X_{IN}/4$, and the low-speed mode, when the system clock is chosen $X_{IN}/16$.

3 : When $P3_1$ is used as X_{CIN} , V_{IH} and V_{IL} of $P3_1$ is $0.85V_{CC}\leq V_{IH}\leq V_{CC}$ and $0\leq V_{IL}\leq 0.15V_{CC}$

4 : The total $I_{OH}(\text{peak})$ of port $P0, P2$ and X_{OUT} is less than 35mA

5 : The total $I_{OH}(\text{peak})$ of port $P0, P2, P3$ and $P5$ is less than 32mA

6 : The total peak current of I_{OL} of port $P1$ is less than 80mA and the average current of total I_{OL} of port $P1$ is less than 40mA

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ELECTRICAL CHARACTERISTICS ($V_{SS}=0V$, $T_a=-20\sim 75^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0\sim P0_7$, $P2_0\sim P2_7$	$V_{CC}=5V$, $I_{OH}=-0.5mA$	4			V
		$V_{CC}=3V$, $I_{OH}=-0.3mA$	2.4			
V_{OH}	"H" output voltage X_{OUT}	$V_{CC}=5V$, $I_{OH}=-0.3mA$	4			V
		$V_{CC}=3V$, $I_{OH}=-0.1mA$	2.4			
V_{OL}	"L" output voltage $P0_0\sim P0_7$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P5_0\sim P5_7$, T, S_{OUT} , CLK, S_{RDY} , SIG, PWM0~PWM3	$V_{CC}=5V$, $I_{OL}=1mA$			1	V
		$V_{CC}=3V$, $I_{OL}=0.5mA$			0.6	
V_{OL}	"L" output voltage $P1_0\sim P1_7$	$V_{CC}=5V$, $I_{OL}=20mA$			2	V
		$V_{CC}=3V$, $I_{OL}=10mA$			1.5	
V_{OL}	"L" output voltage X_{OUT}	$V_{CC}=5V$, $I_{OL}=0.3mA$			1	V
		$V_{CC}=3V$, $I_{OL}=0.1mA$			0.6	
$V_{T+}-V_{T-}$	Hysteresis INT_1 , INT_2 , INT_3 , CLK, CNT ₁ , CNT ₂ , SIG, S_{IN} , $P2_0\sim P2_7$, X_{CIN}	$V_{CC}=5V$		0.2		V
		$V_{CC}=3V$		0.2		
$V_{T+}-V_{T-}$	Hysteresis \overline{RESET}	$V_{CC}=5V$		2		V
		$V_{CC}=3V$		1.0		
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	$V_{CC}=5V$		0.5		V
		$V_{CC}=3V$		0.35		
I_{IL}	"L" input current $\{P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P4_0\sim P4_3$, $P5_0\sim P5_7\}$ without pull-up T_r (Note 1), $IN_0\sim IN_7$, INT_1 , \overline{RESET} , X_{IN}	$V_{CC}=5V$ $V_I=0V$			-5	μA
		$V_{CC}=3V$ $V_I=0V$			-3	
I_{IH}	"H" input current $P0_0\sim P0_7$, $P2_0\sim P2_7$, $P3_0$, $P3_1$, $P4_0\sim P4_7$, $IN_0\sim IN_7$, X_{IN} , X_{CIN} , CNV_{SS}	$V_{CC}=5V$ $V_I=5V$			5	μA
		$V_{CC}=3V$ $V_I=3V$			3	
I_{IH}	"H" input current $\{P1_0\sim P1_7$, $P3_0\sim P3_7$, $P5_0\sim P5_7\}$ without pull-up T_r , INT_1 , INT_2 , INT_3 , CNT ₁ , CNT ₂ , SIG, \overline{RESET} , S_{IN} , CLK	$V_I=10V$			10	μA
R_{PL}	Pull-up T_r , $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P4_0\sim P4_3$, $P5_0\sim P5_7$	$V_{CC}=5V$, $V_I=0V$	7	15	30	k Ω
		$V_{CC}=3V$, $V_I=0V$	10	30	60	
R_{COM}	Output impedance $COM_0\sim COM_3$	$V_{L1}=V_{CC}/3$ $V_{L2}=2V_{L1}$ $V_{L3}=V_{CC}$	$V_{CC}=5V$	200		Ω
			$V_{CC}=3V$	500		
R_s	Output impedance $SEG_0\sim SEG_{23}$	Other COM, SEG pins are opened	$V_{CC}=5V$	2		k Ω
			$V_{CC}=3V$	3		
I_{CC}	Supply current	at operation	$f(X_{IN})=8MHz$ High-speed mode $V_{CC}=5V$	6	12	mA
			$f(X_{IN})=8MHz$ Normal mode $V_{CC}=3V$		8	
		at wait mode	$f(X_{CIN})=32kHz$, $V_{CC}=3V$	18	36	μA
			$f(X_{IN})=8MHz$ Normal mode $V_{CC}=3V$	1		
at stop mode	$f(X_{CIN})=32kHz$, $V_{CC}=3V$	4	12	μA		
	$T_a=25^\circ C$	0.1	0.6			
V_{RAM}	RAM retention voltage		2		5.5	V

Note 1 : Also the same when each port is used as INT_2 , INT_3 , CNT₁, CNT₂, SIG, S_{IN} and X_{CIN} , respectively

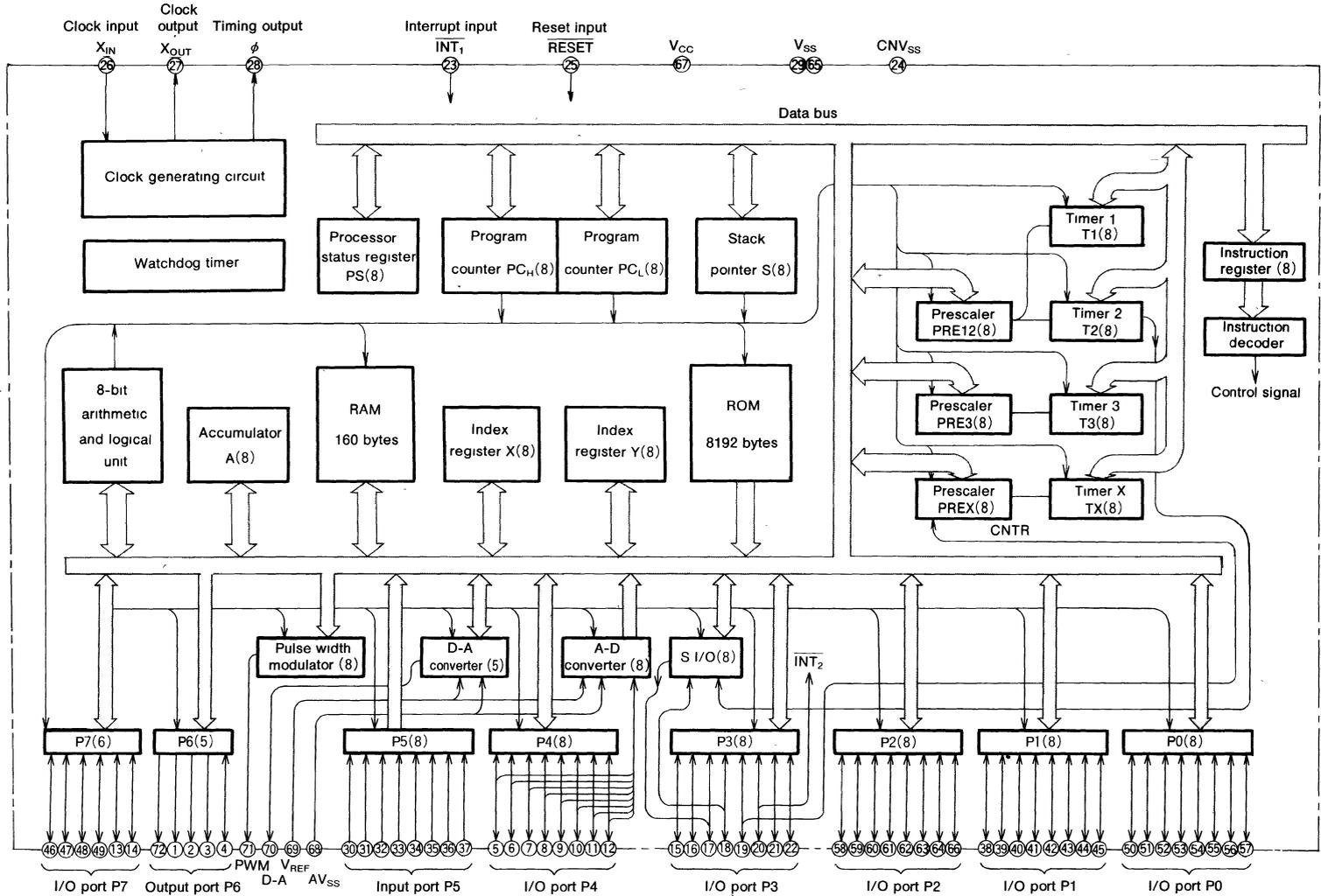
**M37410M3HXXXFP, M37410M4HXXXFP
M37410M6HXXXFP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=8\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	bits
—	Non-linearity error	$V_{CC}=V_{REF}=5.12V$			± 2	LSB
		$V_{CC}=V_{REF}=3.072V$			± 2	
—	Differential non-linearity	$V_{CC}=V_{REF}=5.12V$			± 0.9	LSB
		$V_{CC}=V_{REF}=3.072V$			± 0.9	
V_{OT}	Zero transition error	$V_{CC}=V_{REF}=5.12V$			2	LSB
		$V_{CC}=V_{REF}=3.072V$			2	
V_{FST}	Full-scale transition error	$V_{CC}=V_{REF}=5.12V$			6	LSB
		$V_{CC}=V_{REF}=3.072V$			10	
T_C	Conversion time	$V_{CC}=2.5\sim 5.5V$ High-speed mode		$200/f(X_{IN})$		μs
		$V_{CC}=2.5\sim 5.5V$ Normal mode		$800/f(X_{IN})$		
I_{REF}	Reference input current	$V_{REF}=5V$		1.0	2.5	mA
		$V_{REF}=3V$		0.5	1.5	
I_{IN}	Analog port input current	$V_{IN}=0\sim V_{CC}$		1	10	μA
V_{IN}	Analog input voltage	$V_{CC}=2.5\sim 5.5V$	AV_{SS}		V_{CC}	V
V_{REF}	Reference input voltage		2.5		V_{CC}	V

M37412M4-XXXFP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

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FUNCTIONS OF M37412M4-XXXFP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		2 μ s (minimum instructions, at 4MHz frequency)
Clock frequency		4MHz
Memory size	ROM	8192bytes
	RAM	160bytes
Input/Output ports	INT ₁	Input 1-bit \times 1
	P0, P1, P2, P3, P4	I/O 8-bit \times 5 (a part of P3 is common with serial I/O, timer I/O, and interrupt input)
	P5	Input 8-bit \times 1
	P6	Output 5-bit \times 1 (a part of P6 is common with external trigger output pin)
	P7	I/O 6-bit \times 1
Serial I/O		8-bit \times 1
Timers		8-bit prescaler \times 3+8-bit timer \times 4
A-D conversion		8-bit \times 1 (8 channels)
D-A conversion		5-bit \times 1
Pulse width modulator		8-bit \times 1
Watchdog timer		15-bit \times 1
Subroutine nesting		80 levels (max)
Interrupts		Two external interrupts, Three internal timer interrupts
Clock generating circuit		Built-in (ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 10%
Power dissipation		15mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage	12V (Ports P0, P1, P3, P4, P5, P6, P7, INT ₁)
	Output current	5mA (Ports P0, P1, P2, P3, P4, P7)
Memory expansion		Possible
Operating temperature range		-10 \sim 70 $^{\circ}$ C
Device structure		CMOS silicon gate process
Package		72-pin plastic molded QFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} , V_{SS}	Supply voltage		Power supply inputs $5V \pm 10\%$ to V_{CC} , and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS} .
\overline{RESET}	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than $2\mu s$ (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control the generation frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin
\overline{INT}_1	Interrupt input	Input	This is the highest order interrupt input pin
AV_{SS}	Voltage input for A-D and A-D		This is GND input pin for the A-D and D-A converters
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters
D-A	D-A output	Output	This is output pin from the D-A converter
PWM	PWM output	Output	This is output pin from the pulse width modulator The output structure is N-channel open drain
$P0_0 \sim P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain
$P1_0 \sim P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open drain
$P2_0 \sim P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output
$P3_0 \sim P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as \overline{S}_{RDY} , CLK, S_{OUT} , and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt input pin (\overline{INT}_2), respectively.
$P4_0 \sim P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. $P4_7 \sim P4_0$ work as analog input port $AN_7 \sim AN_0$. The output structure is N-channel open drain
$P5_0 \sim P5_7$	Input port P5	Input	Port P5 is an 8-bit input port. $P5_4 \sim P5_7$ can be used as the edge sense inputs
$P6_0 \sim P6_4$	Output port P6	Output	Port P6 is a 5-bit output port. At external trigger output mode, $P6_0$ and $P6_1$ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain
$P7_0 \sim P7_5$	I/O port P7	I/O	Port P7 is a 6-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open drain

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37412 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

Timer Control Register

The timer control register is allocated to address 00FF₁₆. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

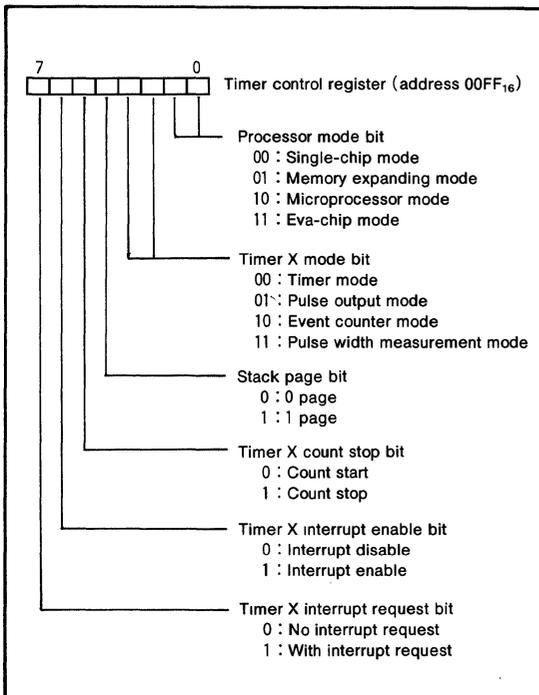


Fig. 1 Structure of timer control register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

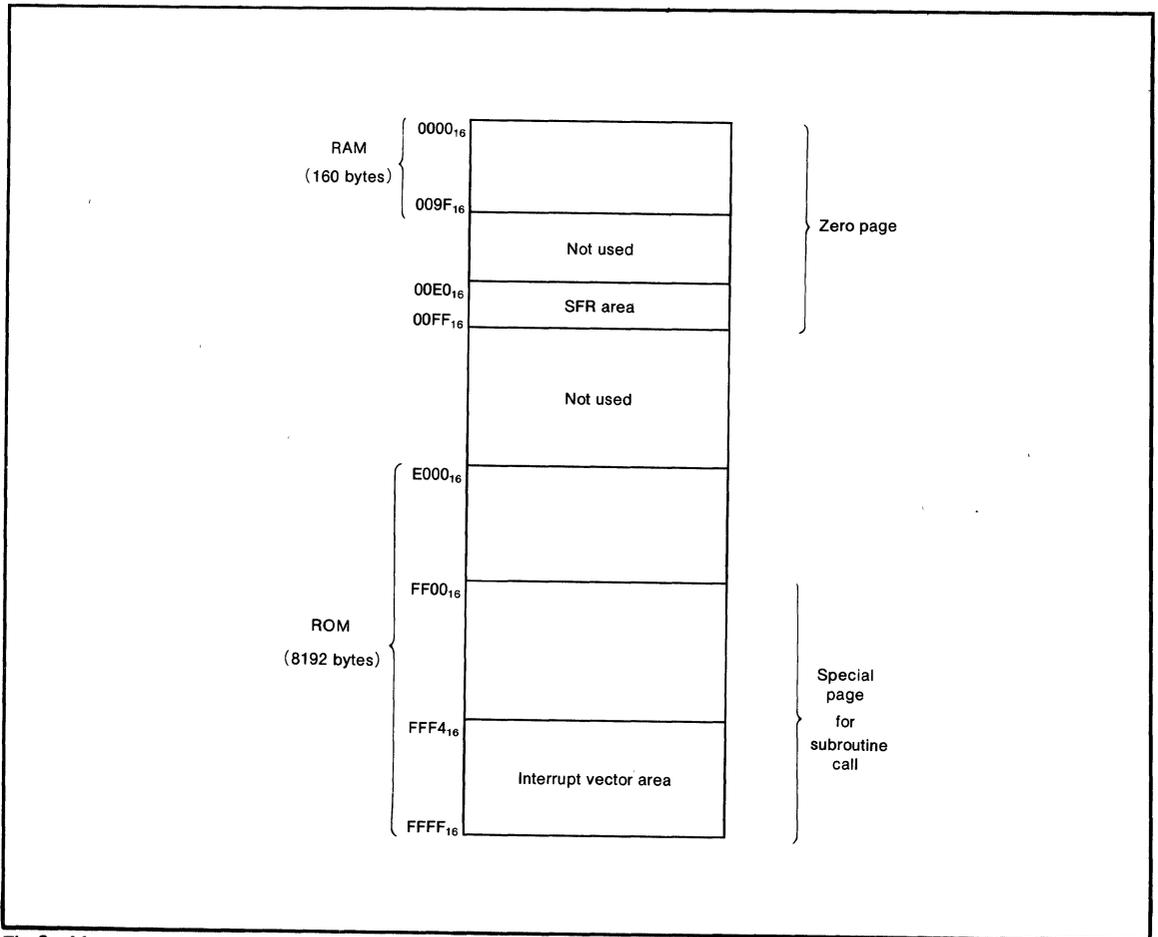


Fig.2 Memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

00E0 ₁₆	Port P0	00F0 ₁₆	D-A conversion register
00E1 ₁₆	Port P0 directional register	00F1 ₁₆	Pulse width modulation register
00E2 ₁₆	Port P1	00F2 ₁₆	Successive approximation register
00E3 ₁₆	Port P1 directional register	00F3 ₁₆	A-D control register
00E4 ₁₆	Port P2	00F4 ₁₆	Watchdog timer
00E5 ₁₆	Port P2 directional register	00F5 ₁₆	Serial I/O mode register
00E6 ₁₆	Port P7	00F6 ₁₆	Serial I/O register
00E7 ₁₆	Port P7 directional register	00F7 ₁₆	Timer 3 prescaler
00E8 ₁₆	Port P3	00F8 ₁₆	Timer 3
00E9 ₁₆	Port P3 directional register	00F9 ₁₆	Timer 1, 2 prescaler
00EA ₁₆	Port P4	00FA ₁₆	Timer 1
00EB ₁₆	Port P4 directional register	00FB ₁₆	Timer 2
00EC ₁₆	Port P5	00FC ₁₆	Timer X prescaler
00ED ₁₆	Port P5 latch	00FD ₁₆	Timer X
00EE ₁₆	Port P6	00FE ₁₆	Interrupt control register
00EF ₁₆	Special function selection register	00FF ₁₆	Timer control register

Fig. 3 SFR (Special Function Register) memory map

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INTERRUPT

The M37412M4-XXXFP can be interrupted from seven sources; \overline{INT}_1 , timer X, timer 1, timer 2/serial I/O, or \overline{INT}_2 /BRK instruction.

However, the \overline{INT}_2 pin is used with port P3₂ and the corresponding directional register bit should be set to "0" when P3₂ is used as an interrupt input pin.

The value of bit 2 of the serial I/O mode register (address 00F5₁₆) determine whether the interrupt is from timer 2 or from serial I/O. When bit 2 is "0" the interrupt is from timer 2, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
RESET	1	FFFF ₁₆ , FFFE ₁₆
\overline{INT}_1	2	FFFD ₁₆ , FFFC ₁₆
Timer X	3	FFFB ₁₆ , FFFA ₁₆
Timer 1	4	FFF9 ₁₆ , FFF8 ₁₆
Timer 2 or serial I/O	5	FFF7 ₁₆ , FFF6 ₁₆
\overline{INT}_2 (BRK)	6	FFF5 ₁₆ , FFF4 ₁₆

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 4. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

- (1) When the \overline{INT}_1 or \overline{INT}_2 pins go from "H" to "L"
- (2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the \overline{INT}_2 interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if \overline{INT}_2 generated the interrupt.

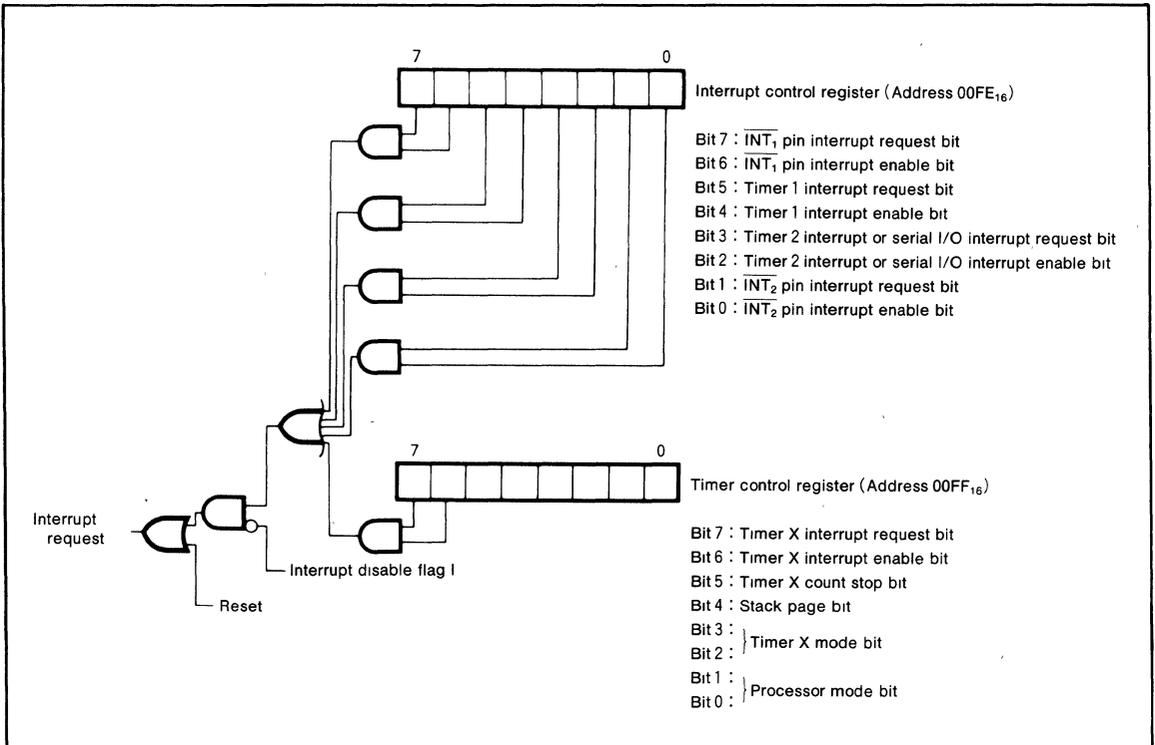


Fig. 4 Interrupt control

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TIMER

The M37412M4-XXXFP has three timers; timer X, timer 1, timer 2 and timer 3. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1, timer 2 and timer 3 is shown in Figure 5.

The P₃/CNTR pin cannot be used as CNTR when P₃ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All four timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses 00FE₁₆ and 00FF₁₆, respectively (see Interrupt section). The prescaler latch and timer latch can be loaded with any number.

The four modes of timer X as follows:

(1) Timer mode [00]

In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]

In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]

This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]

This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 6.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF₁₆ and 01₁₆, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

The function of timer 3 is as same as that of timer 1 and timer 2, with the exception that the detection of its overflow is known by the overflow bit (bit 3 of address 00EF₁₆). When the timer down-counts to zero, the overflow bit is set to "1" and the contents of the timer's latch is reloaded into the timer.

The reset of the overflow bit is made by;

- a) hard ware reset
- b) write "0" to overflow bit
- c) write instruction to timer 3

The structure of special function selection register is shown in Figure 7.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

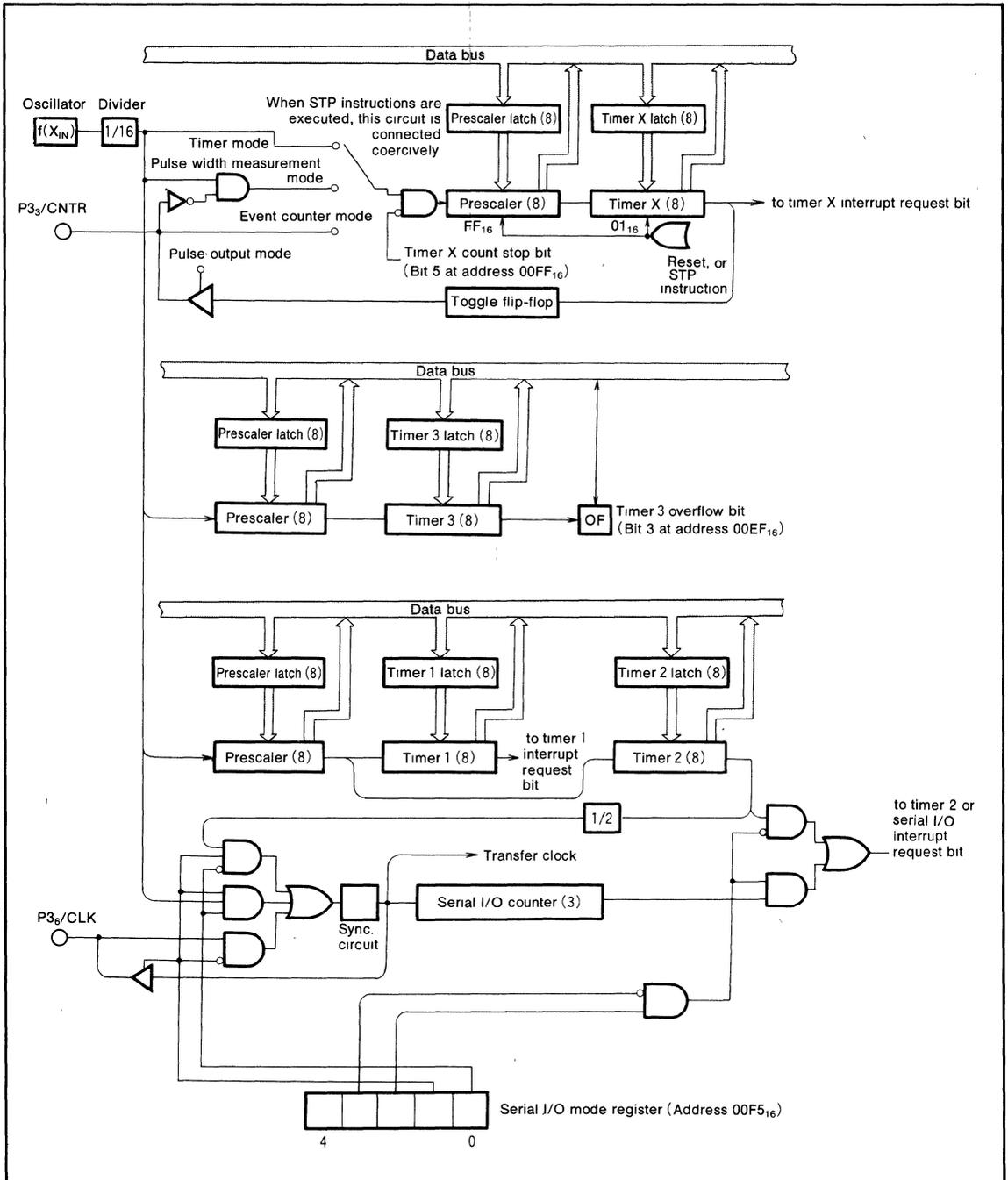


Fig.5 Block diagram of timer X, timer 1, timer 2, and timer 3

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

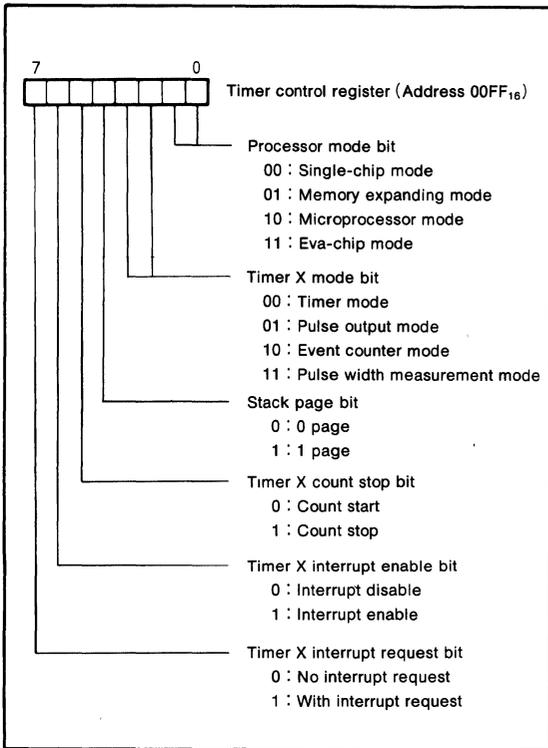


Fig.6 Structure of timer control register

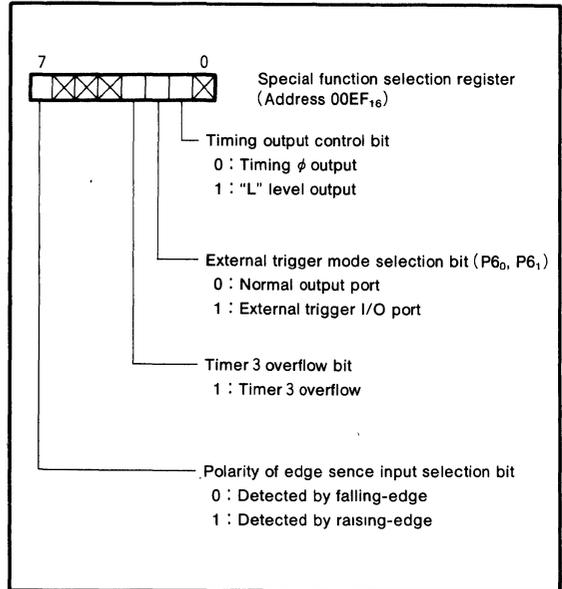


Fig.7 Structure of special function selection register

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SERIAL I/O

A block diagram of the serial I/O is shown in Figure 8.

In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O pins (S_{OUT} , S_{IN}) are used as P3₇, P3₆, P3₅, and P3₄, respectively. The serial I/O mode register (address 00F5₁₆) is a 5-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from P3₆ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the

transfer speed. When the bits are [11], the oscillator frequency divided by 16, becomes the clock.

Bit 2 to 4 decide whether parts of P3 will be used as a serial I/O or not. When bit 3 is "0" and bit 2 is "1", P3₆ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P3₆. If an external synchronous clock is selected, the clock is input to P3₆ and P3₅ will be a serial output and P3₄ will be a serial input. To use P3₄ as a serial input, set the directional register bit which corresponds to P3₄ to "0". For more information on the directional register, refer to the I/O pin section.

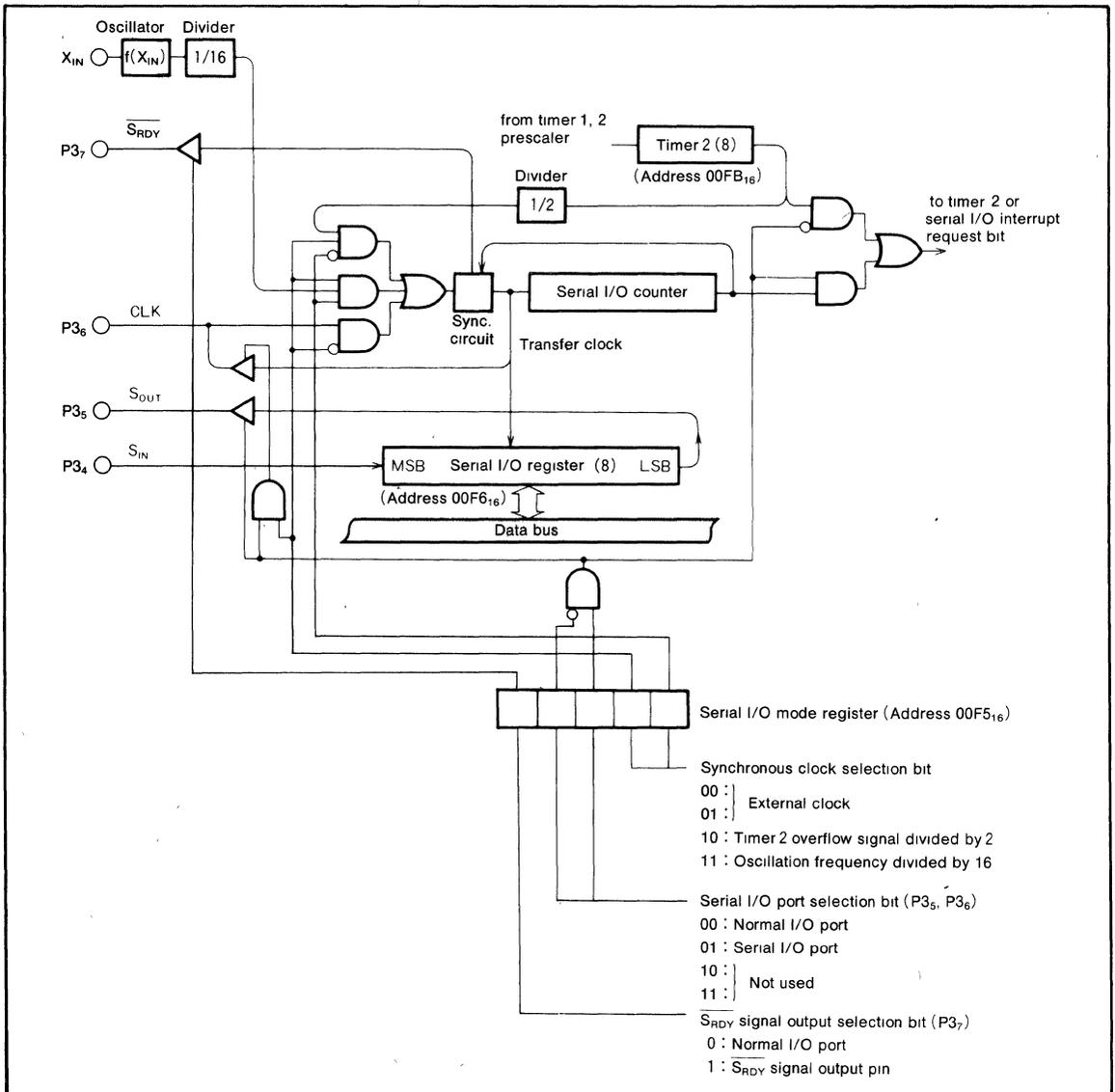


Fig. 8 Block diagram of serial I/O

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

To use the serial I/O, bit 3 and bit 2 need to be set to "01", if they are "00" P3₆ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 4 determines if P3₇ is used as an output pin for the receive data ready signal (bit 4=1, $\overline{S_{RDY}}$) or used as normal I/O pin (bit 4=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address 00F7₁₆). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37412M4-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling

edge of the transfer clock, serial data is output to P3₅. During the rising edge of this clock, data can be input from P3₄ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. An example of communication between two M37412M4-XXXFPs is shown in Figure 10.

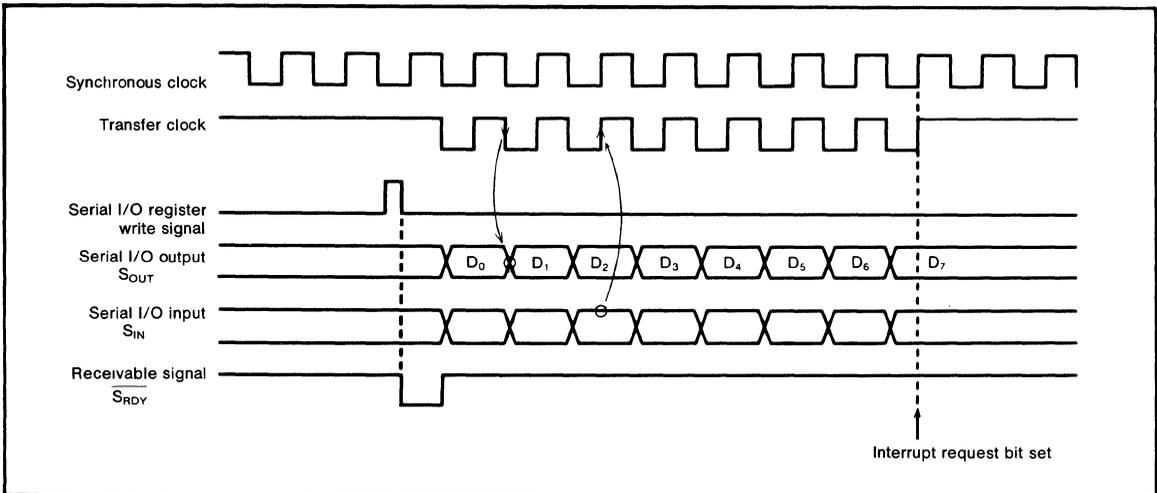


Fig.9 Serial I/O timing

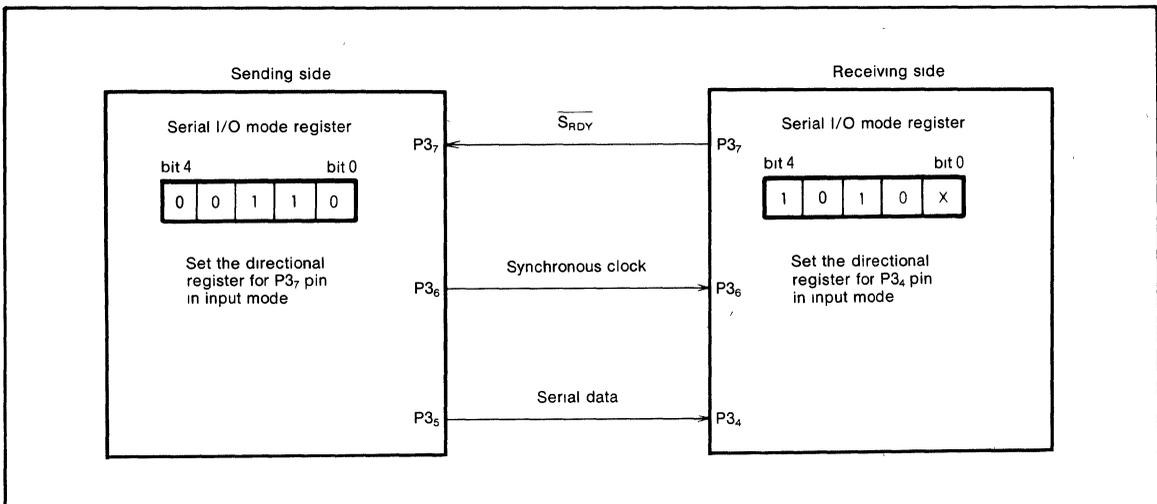


Fig.10 Example of serial I/O connection

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

A-D CONVERTER

An 8-bit successive approximation method of A-D conversion is employed providing a precision of $\pm 3\text{LSB}$. A block diagram of the A-D convertor is shown in Figure 11. Conversion is automatic once it is started with the program.

The six analog inputs are used in common with pins $P_{47} \sim P_{40}$ of port 4. Bits 2, 1 and 0 of the A-D control register (address $00F3_{16}$) are used to select which pins are used for A-D conversion. The input condition is accomplished by setting to "0" the bit in the directional register that corresponds to the pin where A-D conversion is to take place. Bit 4 of the A-D control register is the A-D conversion end bit. During A-D conversion, this bit is "0", and upon completion becomes "1". Thus, it can be ascertained whether or not A-D conversion has been completed or not by inspecting this bit. The relation between the contents of the A-D control register and the selection of input pins are shown in Figure 12.

The results of the conversion can be found by reading the contents of the successive approximation register address $00F2_{16}$ which stores the results of the conversion. The procedure for executing A-D conversion is next explained. Firstly, the pin that is to be used for the A-D conversion is selected by setting bit 1 and bit 0 of the A-D control register. Next, the successive approximation is written to upon which the A-D conversion starts. Since actual data is not written to the successive approximation, any type of may be

written. Simultaneous with its being written, the A-D conversion end bit (bit 4 of address $00F3_{16}$) is cleared to "0" signifying that A-D conversion operations are being conducted. A-D conversion completes after 198 clock cycles upon which the A-D conversion end bit is set to "1" and the results of the conversion can be found in the successive approximation register. Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion.

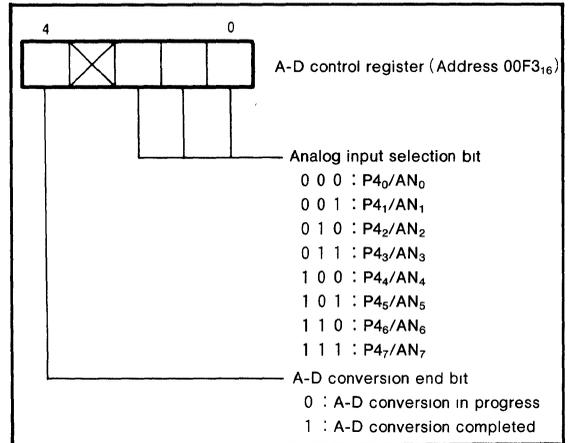


Fig.12 Structure of A-D control register

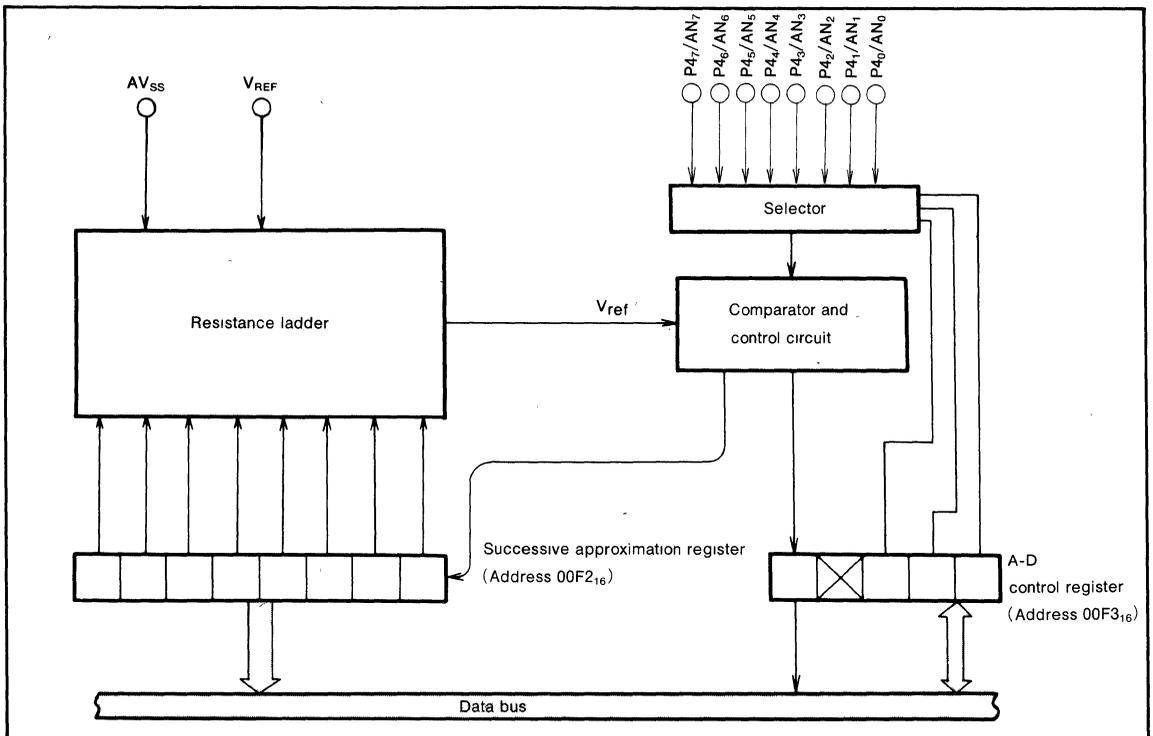


Fig.11 Block diagram of A-D converter

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

D-A CONVERTER

The R-2R method is used for D-A conversion. The block diagram is shown in Figure 13. An analog voltage is output that corresponds to the contents of the D-A conversion register (address 00F0₁₆). Ideally, the relation of the analog

output voltage V and the contents (n) of the D-A conversion register is $V = V_{REF} \times n / 32 (n = 0 \sim 31)$.

Reset operation clears the content n of the D-A conversion register to 0₁₆.

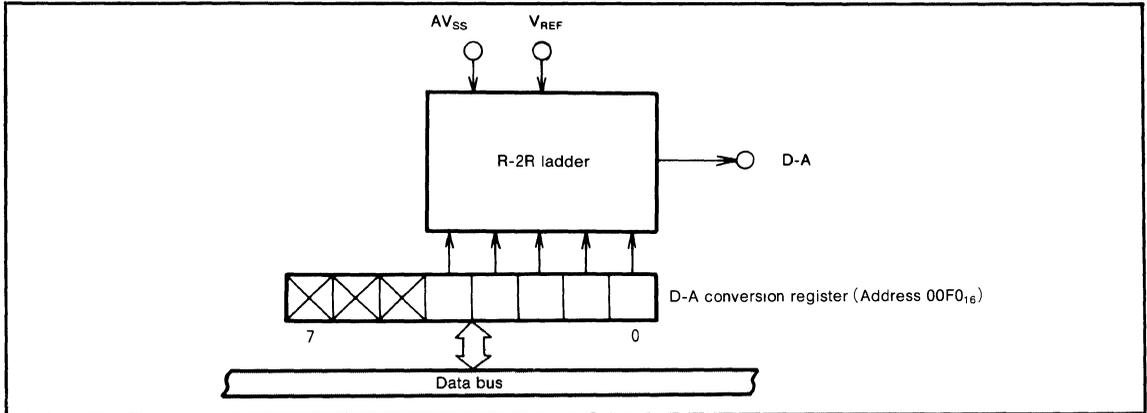


Fig.13 Block diagram of D-A converter

PULSE WIDTH MODULATOR

The pulse width modulation register (address 00F1₁₆) is configured of an 8-bit counter. The period of repetition is 4080 clock cycles. With the content of the pulse width modulation register m , the PWM pin becomes high-level for the

period of $4080 \times m / 255 (m = 0 \sim 255)$. Figure 14 shows that relationship. An N-channel open drain output is used for the PWM pin.

Reset sets the content m of the pulse width modulation register to 00₁₆.

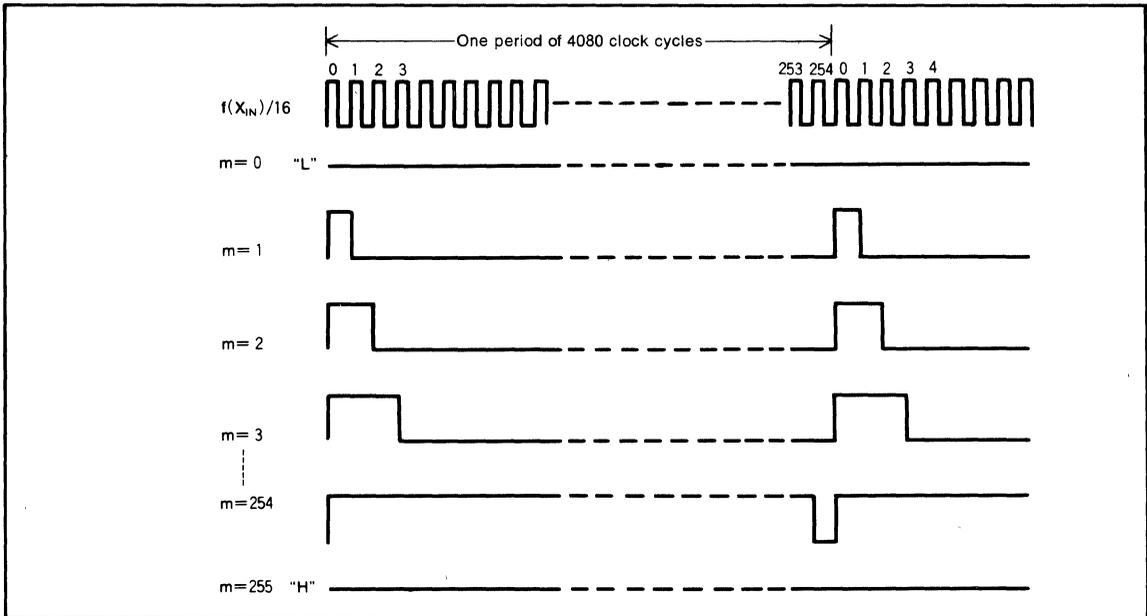


Fig.14 Relation between m and PWM output

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

WATCHDOG TIMER

The watchdog timer provides the means to return to a reset condition when a program runs wild and the program will not run the normal loops.

The watchdog timer (address $00F4_{16}$) is a 15-bit counter. The watchdog timer counts 1/16th the output frequency of the oscillator. The watchdog timer is set to $7FFF_{16}$ when a reset is accomplished a write operation has been made to it. As well as any of the instructions that generate a write signal, such as STA, LDM, and CLB, can be used to write data to the watchdog timer. An output of the most significant bits of the watchdog timer is input to the reset circuit. When 262144 clock cycles have been counted, the most significant bit becomes "0" and reset is carried out. When reset is carried out, the watchdog timer is set to $7FFF_{16}$ and reset is released. The program then begins again from reset vector address. Normally, the program is written so that a writing operation is made to the watchdog timer prior to the most significant bit's becoming "0". Application of a +10V to the RESET pin will disable the watchdog timer function.

Since execution of the STP instruction causes both the clock and the watchdog timer to stop, an option is offered where the STP instruction can be disabled.

RESET CIRCUIT

The M37412M4-XXXFP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the RESET pin is held at "L" level for more than $2\mu s$ while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 16. An example of the reset circuit is shown in Figure 17.

When the power on reset is used, the RESET pin must be held "L" until the oscillation of X_{IN} - X_{OUT} becomes stable.

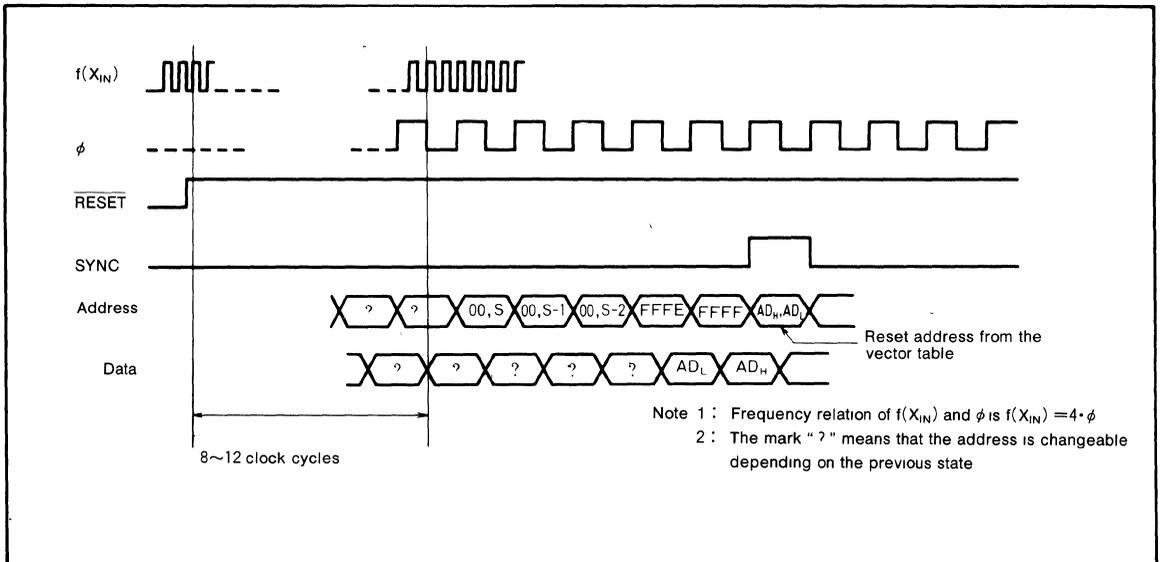


Fig.15 Timing diagram at reset

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Address		
(1) Port P0 directional register	(E 1 ₁₆)	0 0 ₁₆
(2) Port P1 directional register	(E 3 ₁₆)	0 0 ₁₆
(3) Port P2 directional register	(E 5 ₁₆)	0 0 ₁₆
(4) Port P7 directional register	(E 6 ₁₆)	0 0 0 0 0 0
(5) Port P3 directional register	(E 9 ₁₆)	0 0 ₁₆
(6) Port P4 directional register	(E B ₁₆)	0 0 ₁₆
(7) Port P6	(E E ₁₆)	1 1 1 1 1 1
(8) Special function selection register	(E F ₁₆)	0 X X X 0 0 0 X
(9) D-A conversion register	(F 0 ₁₆)	0 0 0 0 0 0
(10) Pulse width modulation register	(F 1 ₁₆)	0 0 ₁₆
(11) Watchdog timer	(F 4 ₁₆)	7 F F F ₁₆
(12) Serial I/O mode register	(F 5 ₁₆)	0 0 0 0 0 0
(13) Prescaler X	(F C ₁₆)	F F ₁₆
(14) Timer X	(F D ₁₆)	0 1 ₁₆
(15) Interrupt control register	(F E ₁₆)	0 0 ₁₆
(16) Timer control register	(F F ₁₆)	0 0 ₁₆
(17) Interrupt disable flag on processor status register	(P S)	1
(18) Program counter	(P C _H)	Contents of address FFFF ₁₆
	(P C _L)	Contents of address FFFE ₁₆

Fig.16 Internal state of microcomputer at reset

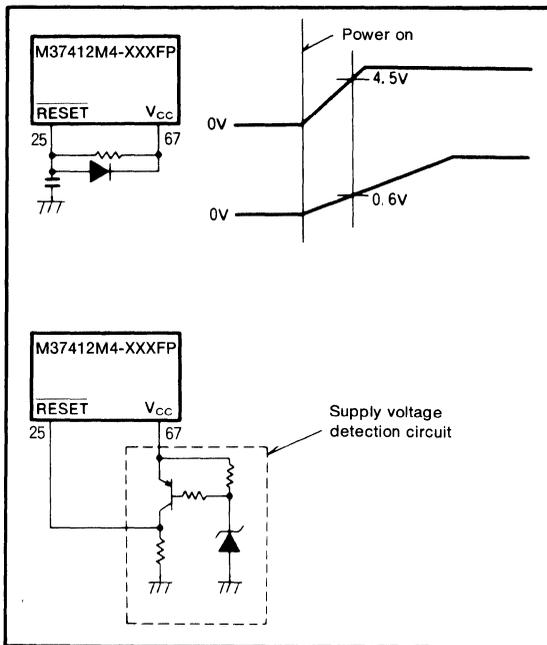


Fig.17 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address 00E0₁₆. Port P0 has a directional register (address 00E1₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even

though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address 00FF₁₆), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

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- (2) Port P1
In the single-chip mode, port P1 has the same function as P0, but it has CMOS output. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.
- (3) Port P2
In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.
For more details, see the processor mode information.
- (4) Port P3
In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O, $\overline{\text{INT}}_2$ and I/O pins for timer X. For more details, see the processor mode information.
- (5) Port P4
Port P4 has the same function as port P0 in the single-chip mode. But P4₇ through P4₂ can also be used as analog input pins AN₇ through AN₂.
- (6) Port P5
Port P5 is an input port. P5₄ through P5₇ can also be used as edge sense inputs. In such a case, reading is begun from 00ED₁₆. 00ED₁₆ is provided with a latch which is set to "1" when the input changes from high-level to low-level.
And for P5₇, polarity of input edge can be selected by polarity of edge sense input selection bit (bit 7 of address 00EF₁₆).
When this bit is set to "0", its latch is set to "1" at the input level goes to "L" from "H". When this bit is set to "1", its latch is set to "1" at the input level goes to "H" from "L". At the reset state, this bit is set to "0".
When content of polarity of edge sense input selection bit was set by program, the latch (bit 7 of address 00ED₁₆) must be reset once.
The input pulse width must be at least 7 clock cycles wide. The latch is reset by using such instructions as LDM and CLB to write a "0" to the latch. When 00ED₁₆ is read, the lower order 4 bits are always zero.
When port P5 is used as level sense input, read the contents of the address 00EC₁₆.
- (7) Port P6
Port P6 is a 5-bit output port. It has N-channel open drain output. P6₀ and P6₁ can be used as external trigger I/O pins, when external trigger mode selection bit (bit 2 of address 00EF₁₆) is set to "1". In this case, P6₀ and P6₁ are trigger clock input pin and trigger output pin, respectively. Using external trigger mode, P6₀'s latch must be set to "1" in order to off the output transistor. In external trigger mode, the content of P6₁'s latch is output to pin when the rising or falling edge is input to P6₀ pin.
When external trigger mode selection bit is set to "0", P6₀ and P6₁ are normal output ports. At the reset state, this bit is set to "0".
- (8) Port P7
Port P7 is a 6-bit I/O port. In this single-chip mode, port P7 has the same functions as port P0.
The functions of this port do not change even though the processor mode may change.
- (9) Clock ϕ output pin
In normal conditions, the oscillator frequency divided by four is output as ϕ . The timing output ϕ is fixed "L" state when the timing output control bit (bit 1 of address 00EF₁₆) is set to "1". But in this case, except the timing output is active. The timing output ϕ is output again when the timing output control bit is set to "0". At reset state this bit is set to "0".
- (10) $\overline{\text{INT}}_1$ pin
The $\overline{\text{INT}}_1$ pin is an interrupt input pin. The $\overline{\text{INT}}_1$ interrupt request bit (bit 7 at address 00FE₁₆) is set to "1" when the input level of this pin changes from "H" to "L".
- (11) $\overline{\text{INT}}_2$ pin (P3₂/ $\overline{\text{INT}}_2$ pin)
The $\overline{\text{INT}}_2$ pin is an interrupt input pin used with P3₂. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address 00FE₁₆) is set to "1".
- (12) CNTR pin (P3₃/CNTR pin)
The P3₃/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

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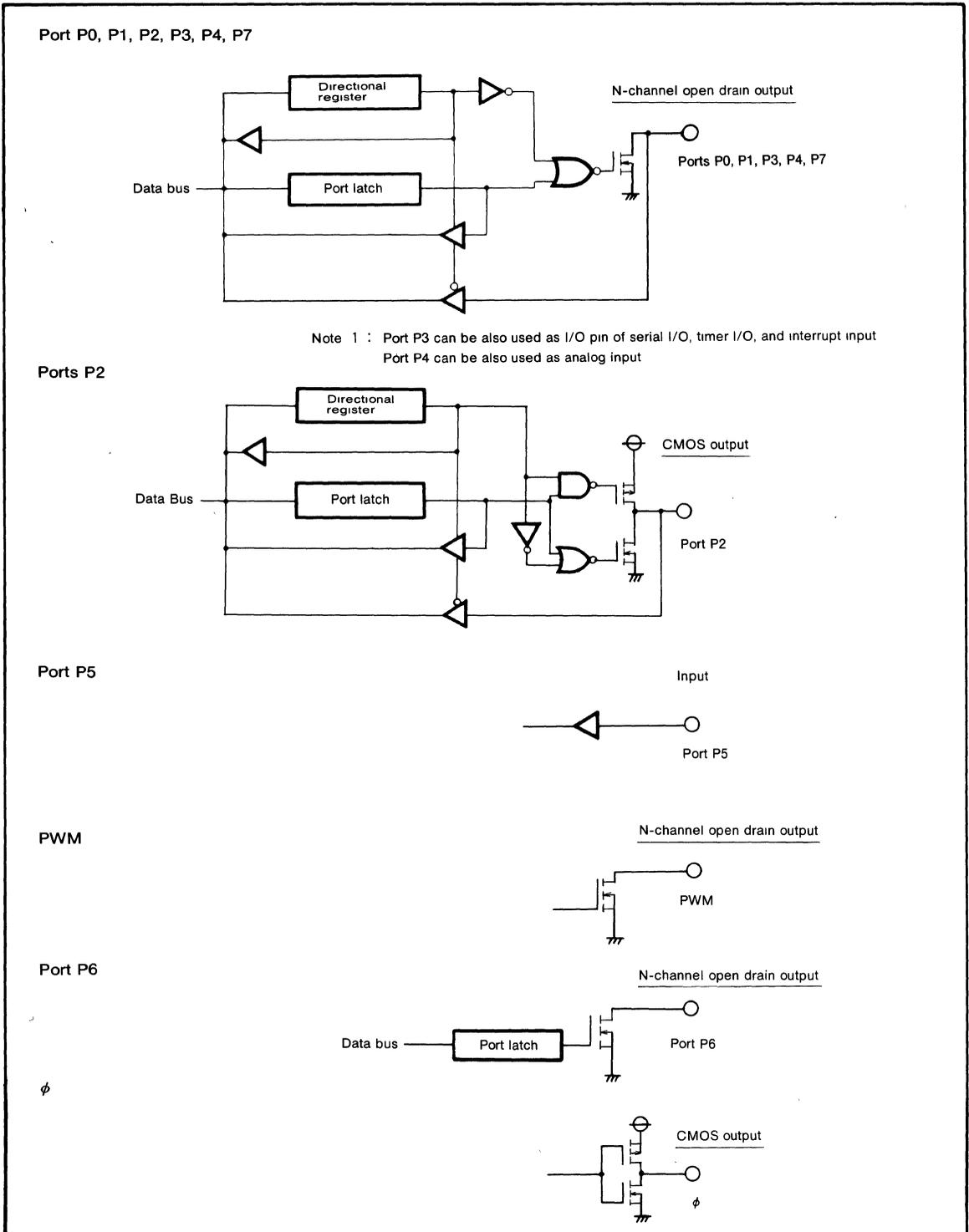


Fig.18 Block diagram of ports P0~P7 (single-chip mode), and output format of ϕ .

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PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0~P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 20 shows the functions of ports P0~P3.

The memory map for the single-chip mode is illustrated in Figure 2 and for other modes, in Figure 19.

By connecting CNV_{SS} to V_{SS} , all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

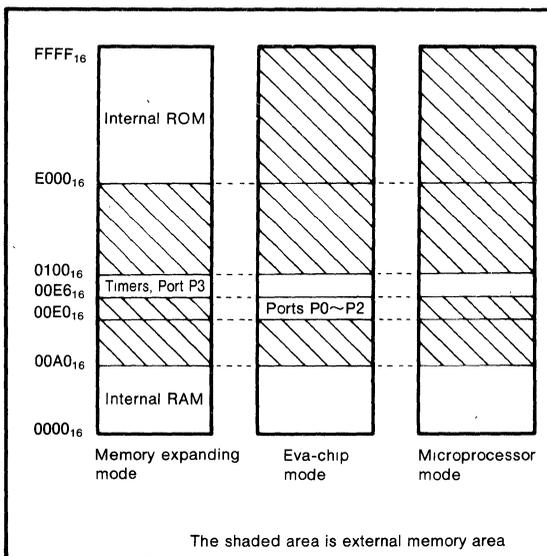


Fig.19 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS} . Ports P0~P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. P2 becomes the data bus ($D_7 \sim D_0$) and loses its normal I/O functions. Pins P3₁ and P3₀ output the SYNC and R/\bar{W} control signals, respectively.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. With the exceptions that the internal ROM is disabled and that external memory must be attached in this mode, this mode is the same as the memory expanding mode.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is required.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original I/O functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state. Pins P3₁ and P3₀ output the SYNC and R/\bar{W} control signals, respectively while ϕ is in the "H" state. When in the "L" state, P3₁ and P3₀ retain their original I/O function.

The R/\bar{W} output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Port	CM ₁	0	1	0	1
	CM ₀	0	1	1	0
Mode		Single-chip mode	Eva-chip mode	Memory expanding mode	Microprocessor mode
Port P0				Same as left	
Port P1				Same as left	
Port P2				Same as left	
Port P3				Same as left	

Fig.20 Processor mode and functions of ports P0~P3

Table 2. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode † Memory expanding mode • Eva-chip mode • Microprocessor mode 	The single-chip mode is set by the reset All modes can be selected by changing the processor mode bit with the program
V _{CC}	<ul style="list-style-type: none"> • Eva-chip mode • Microprocessor mode 	The microprocessor mode is set by the reset Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	<ul style="list-style-type: none"> • Eva-chip mode 	Eva-chip mode only.

PROGRAMMING NOTES

- (1) The frequency ratio of the timer and the prescaler is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
- (4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion. And during A-D conversion, don't use STP or WIT instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3sets

Write the following option on the mask ROM confirmation form

- STP instruction option

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	-0.3~7	V
V_I	Input voltage X_{IN}		-0.3~7	V
V_I	Input voltage $P2_0\sim P2_7, P4_0\sim P4_7$		$-0.3\sim V_{CC}+0.3$	V
V_I	Input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P3_0\sim P3_7,$ $P5_0\sim P5_7, P6_0, P7_0\sim P7_5, INT_1$		-0.3~13	V
V_I	Input voltage $CNV_{SS}, RESET$		-0.3~13	V
V_O	Output voltage $P2_0\sim P2_7, P4_0\sim P4_7, X_{OUT}, \phi, D-A$		$-0.3\sim V_{CC}+0.3$	V
V_O	Output voltage $P0_0\sim P0_7, P1_0\sim P1_7, P3_0\sim P3_7,$ $P6_0\sim P6_3, P7_0\sim P7_5, PWM$		-0.3~13	V
P_d	Power dissipation	$T_a=25^\circ C$	300	mW
T_{opr}	Operating temperature		-10~70	$^\circ C$
T_{stg}	Storage temperature		-40~125	$^\circ C$

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V\pm 10\%$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7,$ $INT_1, RESET, X_{IN}, CNV_{SS}, P6_0,$ $P7_0\sim P7_5$	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7,$ $INT_1, CNV_{SS}, P6_0, P7_0\sim P7_5$	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage $RESET$	0		$0.12V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}	0		$0.16V_{CC}$	V
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7, P1_0\sim P1_7,$ $P2_0\sim P2_7, P3_0\sim P3_7,$ $P4_0\sim P4_7, P7_0\sim P7_5$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0\sim P6_3$ (Note 2)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7, P1_0\sim P1_7,$ $P2_0\sim P2_7, P3_0\sim P3_7,$ $P4_0\sim P4_7, P7_0\sim P7_5$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0\sim P6_3$ (Note 1)			7	mA
$I_{OL(avg)}$	"L" average output current PWM (Note 1)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0\sim P2_7$ (Note 2)			-10	mA
$I_{OH(avg)}$	"H" average output current $P2_0\sim P2_7$ (Note 1)			-5	mA
$f(X_{IN})$	Internal clock oscillating frequency			4	MHz

- Note 1 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
 2 : Total of "L" output current I_{OL} of ports P0, P1, P2, P3, P4, P6, P7 and PWM is 80mA max.
 Total of "H" output current I_{OH} of port P2 is 50mA max.
 3 : "H" input voltage of ports P0, P1, P3, $P4_0\sim P4_3$, P5, P6, P7 and INT_1 is available up to +12V

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage P2 ₀ ~P2 ₇	$I_{OH}=-10mA$	3			V
V_{OH}	"H" output voltage ϕ	$I_{OH}=-2.5mA$	3			V
V_{OL}	"L" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P6 ₀ ~P6 ₃ , P7 ₀ ~P7 ₅	$I_{OL}=10mA$			2	V
V_{OL}	"L" output voltage ϕ , PWM, P6 ₄	$I_{OL}=5mA$			2	V
$V_{T+}-V_{T-}$	Hysteresis INT ₁		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis P3 ₆	When used as CLK input	0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis P3 ₂	When used as INT ₂ input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis P3 ₃	When used as CNTR input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis P6 ₀	When used as T input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis RESET			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X _{IN}		0.1		0.5	V
I_{IL}	"L" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ , P7 ₀ ~P7 ₅ , PWM	$V_I=0V$			-5	μA
I_{IL}	"L" input current INT ₁ , RESET, X _{IN}	$V_I=0V$			-5	μA
I_{IH}	"H" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₃ , P5 ₀ ~P5 ₇ , P6 ₀ , P7 ₀ ~P7 ₅ , PWM	$V_I=12V$			12	μA
I_{IH}	"H" input current INT ₁ , RESET, X _{IN} , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇	$V_I=5V$			5	μA
V_{RAM}	RAM retention voltage	At clock stop	2			V
I_{CC}	Supply current	ϕ , X _{OUT} , and D-A pins opened, other pins at V _{SS} , and A-D converter in the finished condition	$f(X_{IN})=4MHz$ Square wave	3	6	mA
			At clock stop $T_a=25^\circ C$		1	
			At clock stop $T_a=75^\circ C$		10	μA

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistance value	$V_{REF}=V_{CC}$	2		10	$k\Omega$
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			5	Bits
—	Error in full scale range	$V_{REF}=V_{CC}$			± 1	%
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
R_O	Output resistance	$V_{REF}=V_{CC}$			3	$k\Omega$
V_{REF}	Reference voltage		4		V_{CC}	V

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMING REQUIREMENTS

Single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{SU}(P0D-\phi)$	Port P0 input setup time	270			ns
$t_{SU}(P1D-\phi)$	Port P1 input setup time	270			ns
$t_{SU}(P2D-\phi)$	Port P2 input setup time	270			ns
$t_{SU}(P3D-\phi)$	Port P3 input setup time	270			ns
$t_{SU}(P4D-\phi)$	Port P4 input setup time	270			ns
$t_{SU}(P5D-\phi)$	Port P5 input setup time	270			ns
$t_{SU}(P7D-\phi)$	Port P7 input setup time	270			ns
$t_h(\phi-P0D)$	Port P0 input hold time	20			ns
$t_h(\phi-P1D)$	Port P1 input hold time	20			ns
$t_h(\phi-P2D)$	Port P2 input hold time	20			ns
$t_h(\phi-P3D)$	Port P3 input hold time	20			ns
$t_h(\phi-P4D)$	Port P4 input hold time	20			ns
$t_h(\phi-P5D)$	Port P5 input hold time	20			ns
$t_h(\phi-P7D)$	Port P7 input hold time	20			ns
t_C	External clock input cycle time	250			ns
t_W	External clock input pulse width	75			ns
t_r	External clock rising edge time			25	ns
t_f	External clock falling edge time			25	ns

Eva-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ.	Max.	
$t_{SU}(P0D-\phi)$	Port P0 input setup time	270			ns
$t_{SU}(P1D-\phi)$	Port P1 input setup time	270			ns
$t_{SU}(P2D-\phi)$	Port P2 input setup time	270			ns
$t_h(\phi-P0D)$	Port P0 input hold time	20			ns
$t_h(\phi-P1D)$	Port P1 input hold time	20			ns
$t_h(\phi-P2D)$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ.	Max.	
$t_{SU}(P2D-\phi)$	Port P2 input setup time	270			ns
$t_h(\phi-P2D)$	Port P2 input hold time	30			ns

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

SWITCHING CHARACTERISTICS

Single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max	
$t_d(\phi-P0Q)$	Port P0 data output delay time	Fig 24			230	ns
$t_d(\phi-P1Q)$	Port P1 data output delay time				230	ns
$t_d(\phi-P2Q)$	Port P2 data output delay time	Fig.25			230	ns
$t_d(\phi-P3Q)$	Port P3 data output delay time				230	ns
$t_d(\phi-P4Q)$	Port P4 data output delay time	Fig 24			230	ns
$t_d(\phi-P6Q)$	Port P6 data output delay time				230	ns
$t_d(\phi-P7Q)$	Port P7 data output delay time				230	ns

Eva-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ.	Max		
$t_d(\phi-P0A)$	Port P0 address output delay time	Fig 24			250	ns	
$t_d(\phi-P0AF)$	Port P0 address output delay time				250	ns	
$t_d(\phi-P0Q)$	Port P0 data output delay time				200	ns	
$t_d(\phi-P0QF)$	Port P0 data output delay time				200	ns	
$t_d(\phi-P1A)$	Port P1 address output delay time				250	ns	
$t_d(\phi-P1AF)$	Port P1 address output delay time				250	ns	
$t_d(\phi-P1Q)$	Port P1 data output delay time				200	ns	
$t_d(\phi-P1QF)$	Port P1 data output delay time				200	ns	
$t_d(\phi-P2Q)$	Port P2 data output delay time		Fig.25			300	ns
$t_d(\phi-P2QF)$	Port P2 data output delay time					300	ns
$t_d(\phi-R/W)$	R/W signal output delay time	Fig 24			250	ns	
$t_d(\phi-R/WF)$	R/W signal output delay time				250	ns	
$t_d(\phi-P3Q)$	Port P3 ₀ data output delay time				200	ns	
$t_d(\phi-P3QF)$	Port P3 ₀ data output delay time				200	ns	
$t_d(\phi-SYNC)$	SYNC signal output delay time				250	ns	
$t_d(\phi-SYNCF)$	SYNC signal output delay time				250	ns	
$t_d(\phi-P3Q)$	Port P3 ₁ data output delay time				200	ns	
$t_d(\phi-P3QF)$	Port P3 ₁ data output delay time				200	ns	

Memory expanding mode and microprocessor mode

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
$t_d(\phi-P0A)$	Port P0 address output delay time	Fig 24			250	ns
$t_d(\phi-P1A)$	Port P1 address output delay time				250	ns
$t_d(\phi-P2Q)$	Port P2 data output delay time	Fig 25			300	ns
$t_d(\phi-P2QF)$	Port P2 data output delay time				300	ns
$t_d(\phi-R/W)$	R/W signal output delay time	Fig 24			250	ns
$t_d(\phi-SYNC)$	SYNC signal output delay time				250	ns

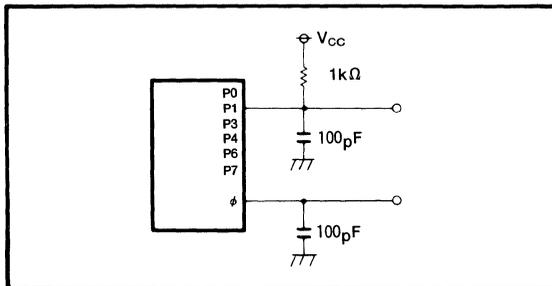


Fig.24 Ports P0, P1, P3, P4, P6 and P7 test circuit

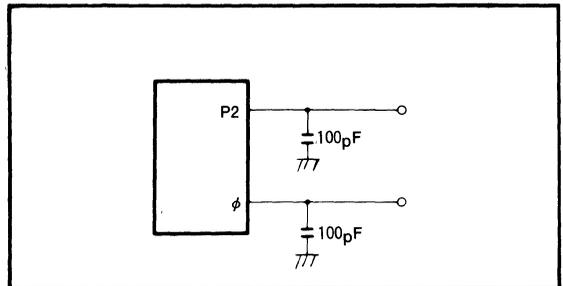
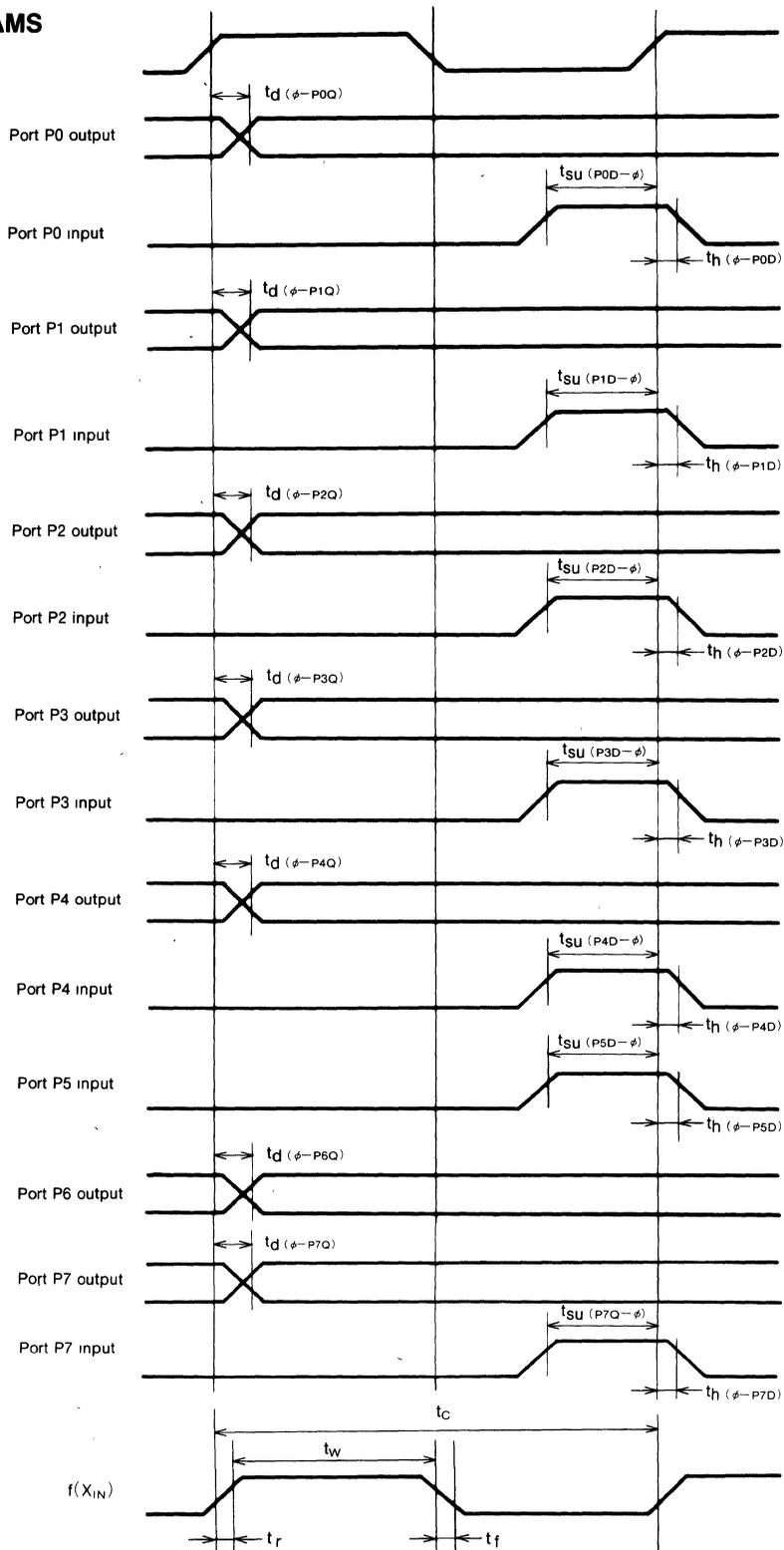


Fig.25 Port P2 test circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

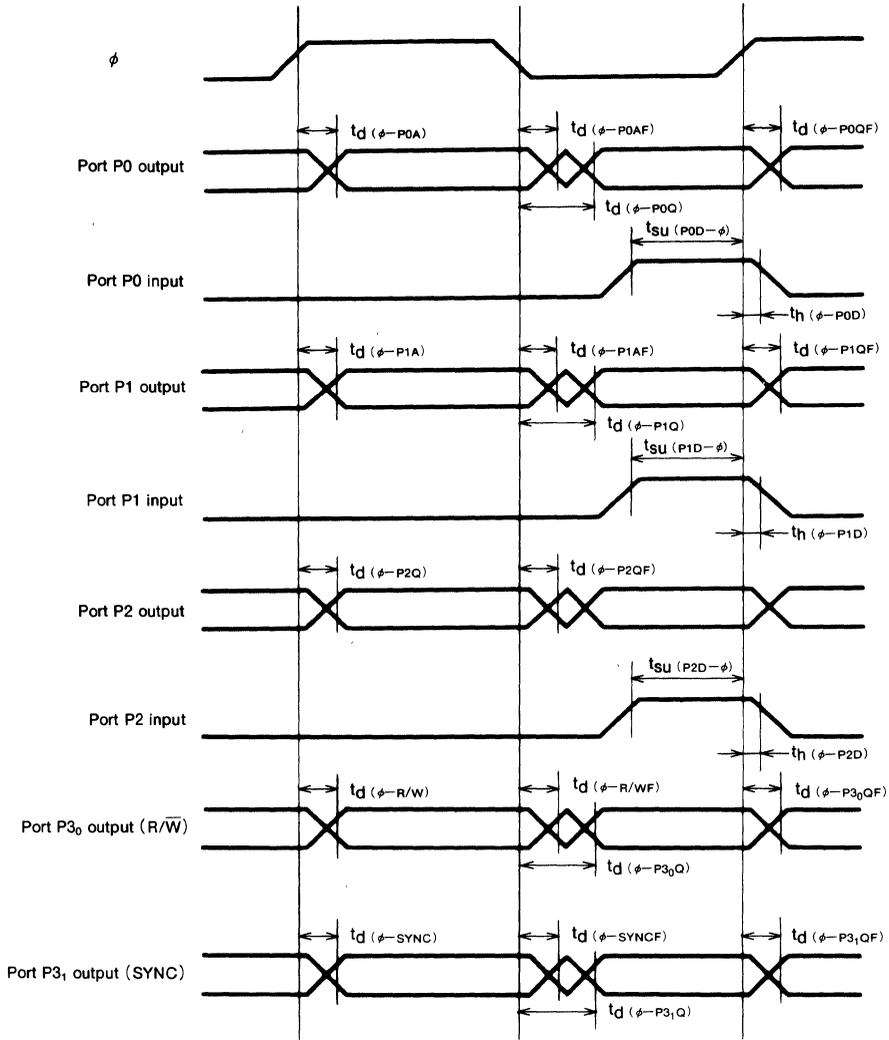
TIMING DIAGRAMS

In single-chip mode



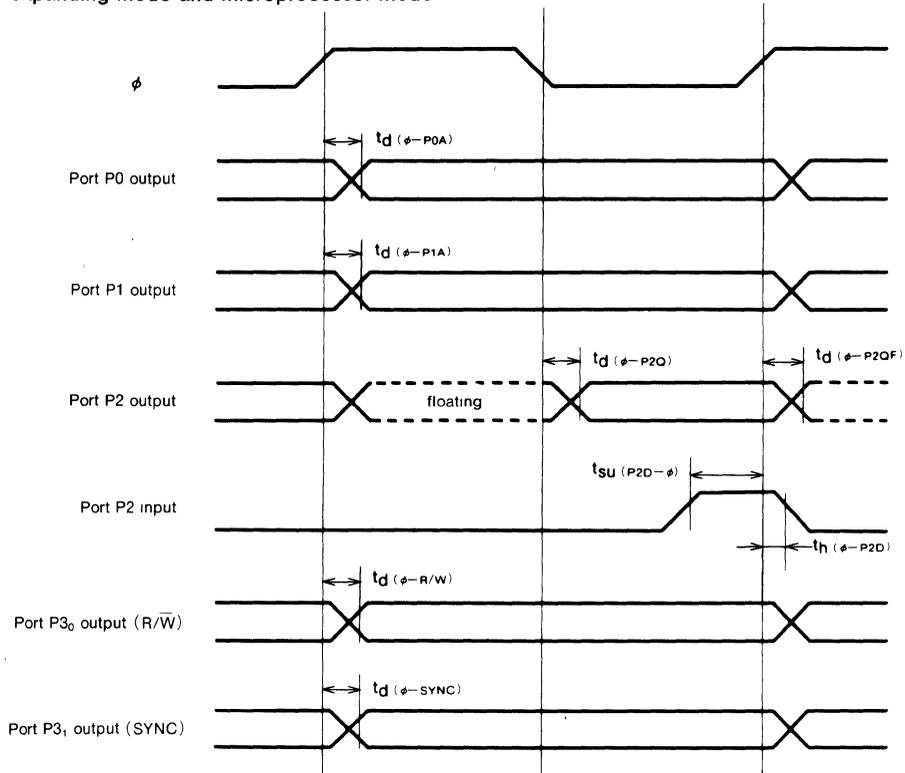
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

In eva-chip mode



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

In memory expanding mode and microprocessor mode



PRELIMINARY
 (Mitsubishi Electric Co.)

M37413M4HXXXFP M37413M6HXXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37413M4HXXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin plastic molded QFP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37413M4HXXXFP and the M37413M6HXXXFP are noted below. The following explanations apply to the M37413M4HXXXFP.

Specification variations for other chips are noted accordingly.

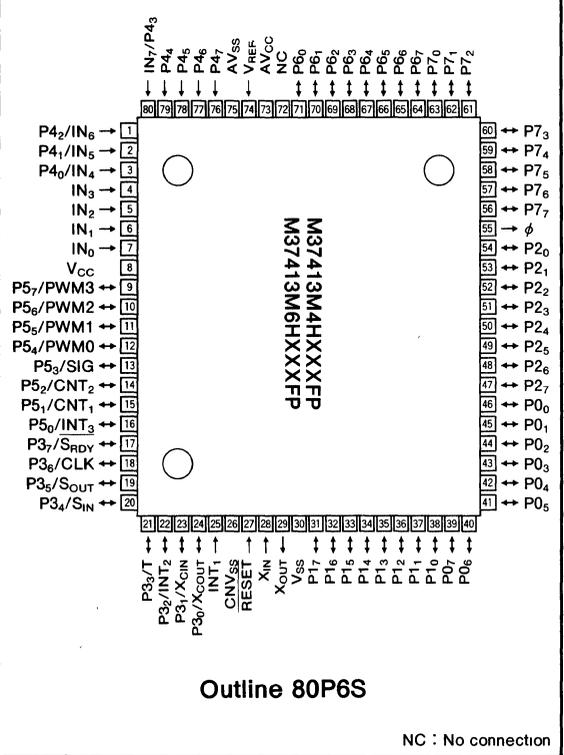
The M37413M4HXXXFP has the same functions as the M37413M4-XXXFP except for the method of writing to interrupt request distinguish registers.

Type name	ROM size
M37413M4HXXXFP	8192 bytes
M37413M6HXXXFP	12288 bytes

FEATURES

- Number of basic instructions..... 69
- Memory size ROM ... 8192 bytes (M37413M4HXXXFP)
 12288 bytes (M37413M6HXXXFP)
 RAM..... 256 bytes
- Instruction execution time
 (minimum instructions at 8MHz frequency)
 at high-speed mode 1 μ s
 at normal mode..... 4 μ s
- Single power supply
 high-speed mode (at 8MHz frequency)
 4.5~5.5V
 normal mode (at 8MHz frequency)
 high-speed mode (at 2MHz frequency)
 2.5~5.5V
- Power dissipation
 high-speed mode (at 8MHz frequency)
 30mW ($V_{CC}=5V$, Typ.)
 low-speed mode (at 32kHz frequency for clock
 function) 54 μ W ($V_{CC}=3V$, Typ.)
- RAM retention voltage (stop mode)
 $2.0V \leq V_{RAM} \leq 5.5V$
- Subroutine nesting 96levels (Max.)
- Interrupt..... 10types, 5vectors
- 8-bit timer 4 (3 when used as serial I/O)
- 16-bit timer 1
- Programmable I/O ports
 (Ports P0, P1, P2, P3, P5, P6, P7)..... 56
- Input port (Port P4) 8
- Serial I/O (8-bit) 1
- A-D converter..... 8-bit, 8channel
- Two clock generating circuits
 (One is for main clock, the other is for clock function)

PIN CONFIGURATION (TOP VIEW)



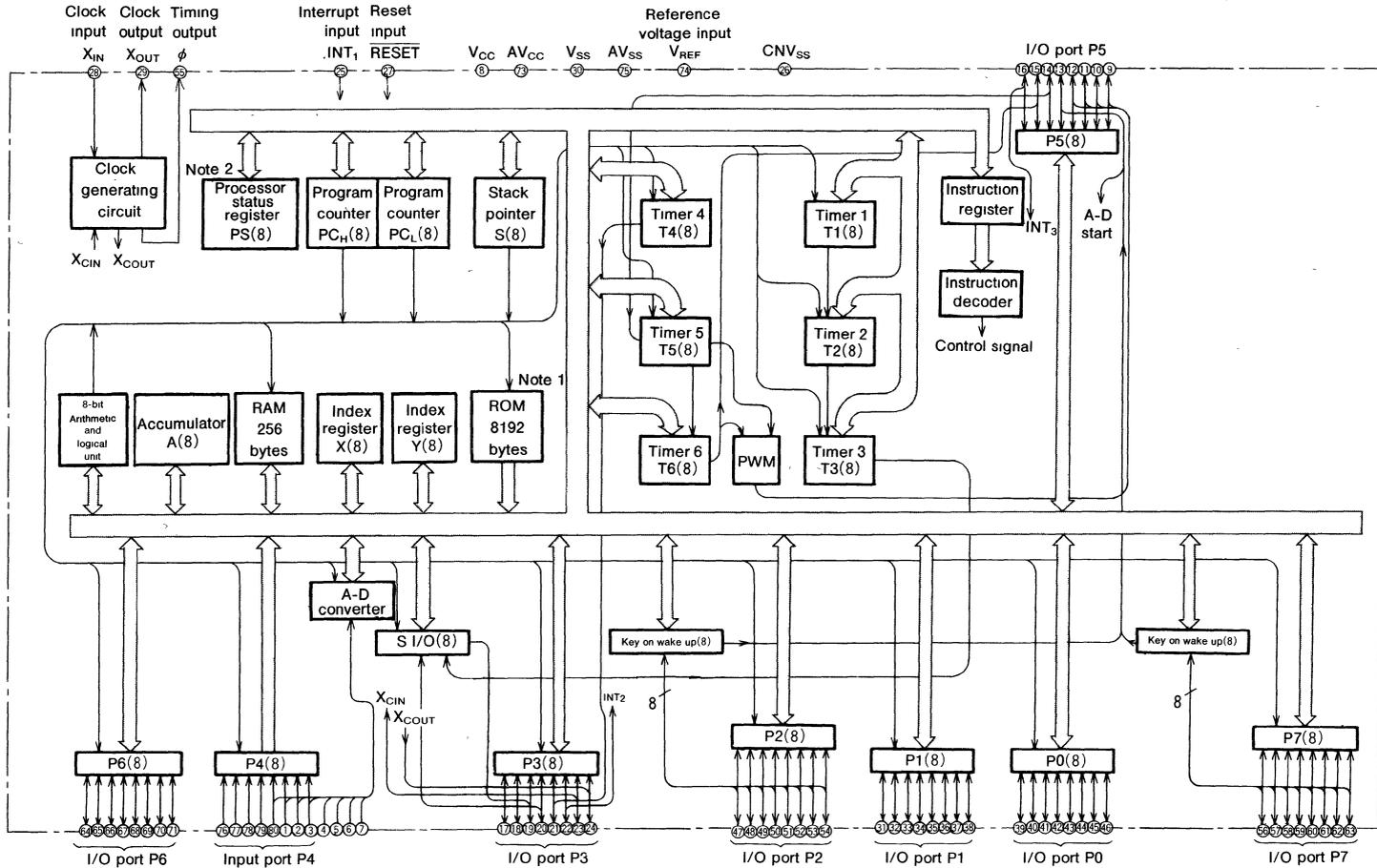
Outline 80P6S

NC : No connection

APPLICATION

Audio-visual equipment, VCR, Tuner, Office automation equipment, Camera, Communications apparatus, Cordless telephone.

M37413M4HXXXFP BLOCK DIAGRAM



Note 1 : 12288 bytes for M37413M6HXXXFP

2 : PC_H uses 6 bits only



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MITSUBISHI MICROCOMPUTERS
M37413M4HXXXFP
M37413M6HXXXFP

M37413M4HXXXFP
M37413M6HXXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37413M4HXXXFP, M37413M6HXXXFP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1 μ s (minimum instructions, at 8MHz frequency)
Clock frequency			8MHz
Memory size	M37413M4HXXXFP	ROM	8192bytes
		RAM	256bytes
	M37413M6HXXXFP	ROM	12288bytes
		RAM	256bytes
Input/Output port	P0, P2, P7	I/O	8-bit \times 3 (CMOS output, Pull-up option)
	P1, P3, P5, P6	I/O	8-bit \times 4 (N-channel open drain output, Pull-up option)
	P4	Input	8-bit \times 1 (Pull-up option)
Serial I/O			8-bit \times 1
Timers			8-bit timer \times 4 16-bit timer \times 1
Subroutine nesting			96 (max)
Interrupt			4 external interrupts, 5 internal interrupts, 1 software interrupt
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator)
Operating temperature range			-20~75 $^{\circ}$ C
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is connect to V _{SS}
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 16μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
INT ₁	Interrupt input	Input	This is the highest order interrupt input pin
AV _{CC}	Voltage input for A-D		This is power supply input pin for the A-D converter
AV _{SS}	Voltage input for A-D		This is GND input pin for the A-D converters. Connect to V _{SS}
V _{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output. Pull-up option of this port is valid only in input mode.
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-ch open drain. Pull-up option of this port is valid only in input mode.
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 and also works as the key on wake up function with mask option. Pull-up option of this port is valid only in input mode.
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P1. When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as S _{RDY} , CLK, S _{OUT} , and S _{IN} pins, respectively. Also P3 ₃ , P3 ₂ , P3 ₁ , and P3 ₀ work as timer 4 overflow signal divided by 2 output pin (T), INT ₂ pin, X _{CIN} and X _{COU} pins, respectively. Pull-up option of this port is valid in both input and output modes.
P4 ₀ ~P4 ₇	Input port P4	Input	Port P4 is an 4-bit input port. P4 ₀ ~P4 ₃ are in common with IN ₄ ~IN ₇ . Pull-up option can be used when this port is used as a input port.
P5 ₀ ~P5 ₇	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P1. P5 ₀ , P5 ₁ , P5 ₂ and P5 ₃ are in common with INT ₃ , timer 3 input, timer 5 input and A-D trigger input respectively. P5 ₄ ~P5 ₇ are also in common with PWM0~PWM3. Pull-up option of this port is valid in both input and output modes.
P6 ₀ ~P6 ₇	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P1. Pull-up option of this port is valid in both input and output modes.
P7 ₀ ~P7 ₇	I/O port P7	I/O	Port P7 is an 8-bit I/O port and has basically the same functions as port P2. Pull-up option of this port is valid only in input mode.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37413 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

M37413M4HXXFP
M37413M6HXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

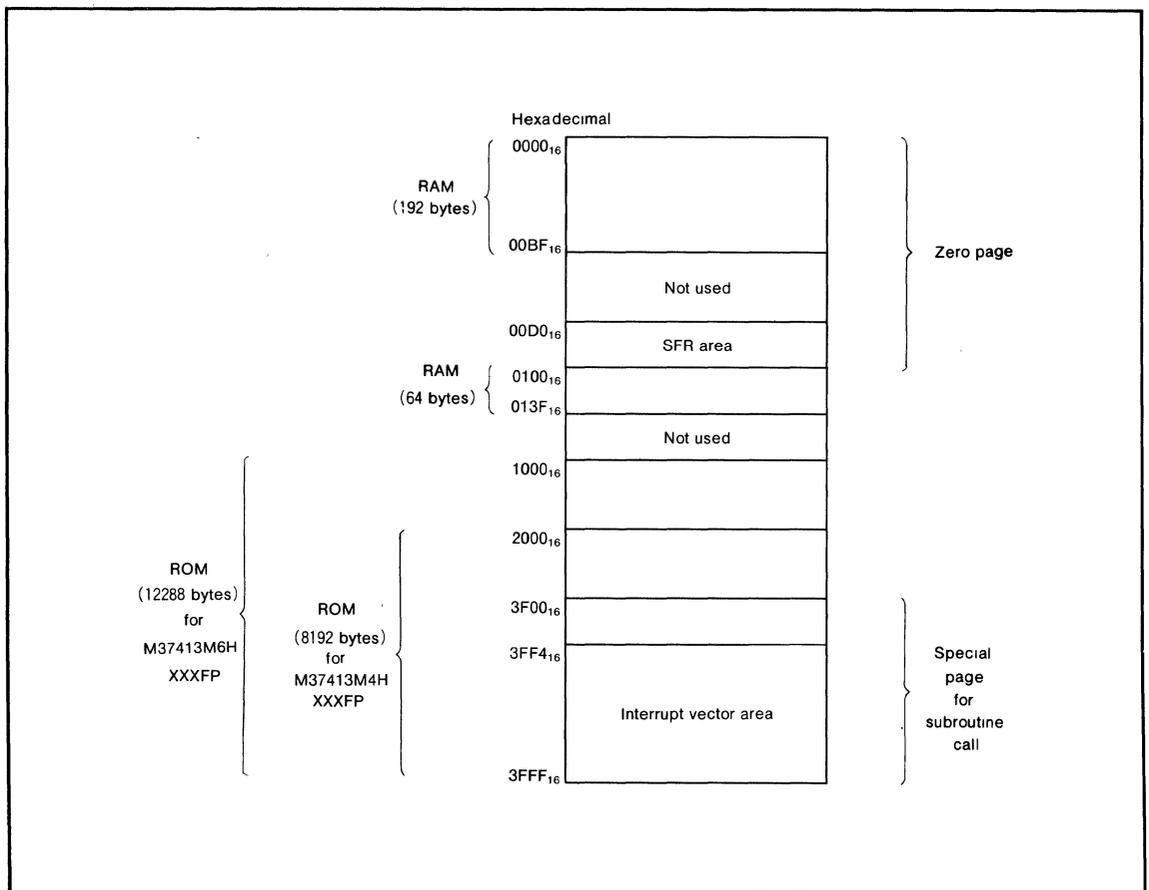


Fig. 1 Memory map

00D0 ₁₆	Port P6	00E0 ₁₆	Port P0
00D1 ₁₆	Port P6 directional register	00E1 ₁₆	Port P0 directional register
00D2 ₁₆	Port P7	00E2 ₁₆	Port P1
00D3 ₁₆	Port P7 directional register	00E3 ₁₆	Port P1 directional register
00D4 ₁₆		00E4 ₁₆	Port P2
00D5 ₁₆	P7 Key on wake up register	00E5 ₁₆	Port P2 directional register
00D6 ₁₆		00E6 ₁₆	
00D7 ₁₆		00E7 ₁₆	
00D8 ₁₆		00E8 ₁₆	Port P3
00D9 ₁₆		00E9 ₁₆	Port P3 directional register
00DA ₁₆		00EA ₁₆	Interrupt request distinguish register 2
00DB ₁₆		00EB ₁₆	Interrupt request distinguish register 1
00DC ₁₆		00EC ₁₆	Port P5
00DD ₁₆		00ED ₁₆	Port P5 directional register
00DE ₁₆		00EE ₁₆	P2 Key on wake up register
00DF ₁₆		00EF ₁₆	A-D register
		00F0 ₁₆	
		00F1 ₁₆	Timer 6 latch
		00F2 ₁₆	A-D control register
		00F3 ₁₆	PWM control register
		00F4 ₁₆	
		00F5 ₁₆	Port P4
		00F6 ₁₆	Serial I/O mode register
		00F7 ₁₆	Serial I/O register
		00F8 ₁₆	Timer 4, 5, 6 mode register
		00F9 ₁₆	Timer 1 latch
		00FA ₁₆	Timer 2 latch
		00FB ₁₆	Timer 3 latch
		00FC ₁₆	Timer 4 latch
		00FD ₁₆	Timer 5 latch
		00FE ₁₆	Interrupt control register
		00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

INTERRUPT

The M37413M4HXXFP can be interrupted from ten sources; INT₁, Timer 2 or Serial I/O, INT₃ or Key on wake up, INT₂ or Timer 3, Timer 6 or A-D, and BRK instruction.

"Key on wake up" can only be used at power down state by STP instruction or WIT instruction. When one of the P2 or P7 is "L", an interrupt occurs.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

- (1) When the INT₁, INT₂ or INT₃ pins go from "H" to "L" or "L" to "H"
- (2) When the levels any pin of P2 or P7 goes "L" (at power down mode)
- (3) When the contents of timer 2, timer 3, timer 6 or the counter of serial I/O goes "0"

These request bits can be clear by a program but can not be set. The interrupt enable bit can be set and clear by a program.

When the two interrupt requests, which are the same priority and are at the same sampling, the priority process is processed by interrupt request distinguish register 1 and 2. The interrupt request distinguish bit is used by software to determine priority when two interrupt causes are allocated to the same interrupt vector (that is, the two interrupts have the same priority).

Irrespective of whether the interrupt is disabled or enabled, the interrupt request distinguish bit is automatically set to "1" when conditions arise that satisfy the interrupt cause. However, the interrupt request distinguish bit is not automatically cleared. The bit must therefore be cleared by software in the interrupt service routine (before executing an RTI instruction).

Note that when using the instruction CLB to clear this bit, the request distinguish bit of an interrupt that is generated during execution of CLB will not be set (to "1"). Use one of the following two methods to clear interrupt request distinguish bits:

- ① Use instruction LDM to write directly to address 00EB₁₆ (interrupt request distinguish register 1) or 00EA₁₆ (interrupt request distinguish register 2).

```
LDM # $nn, $zz
```

Where zz is the address(00EB₁₆ or 00EA₁₆) of the interrupt request distinguish register that includes the interrupt request distinguish bit that is to be cleared and nn sets the interrupt request distinguish bit to be cleared to "0" and other interrupt request distinguish bits to "1"

Other control bits must be set according to the required control (interrupts enabled or disabled)

[Example] Clearing the INT₂ interrupt request distinguish bit

```
LDM 1X1X0X1XB, $00EB
```

↑ ↑ ↑ ↑

Of the interrupt request distinguish bits, only the INT₂ interrupt request distinguish bit, which is to be cleared, should be set to "0"

The values of bits marked "X" are determined by the control being effected

- ② Use instructions LDA, ORA, AND, and STA to write via the accumulator to address 00EB₁₆ (interrupt request distinguish register 1) or 00EA₁₆ (interrupt request distinguish register 2).

```
LDA $zz
```

```
ORA # $nn
```

```
AND # $nn
```

```
STA $zz
```

Where zz is the address(00EB₁₆ or 00EA₁₆) of the interrupt request distinguish register that includes the interrupt request distinguish bit that is to be cleared and nn sets the interrupt request distinguish bit to be cleared to "0" and other interrupt request distinguish bits to "1". Other control bits must be set according to the required control (interrupts enabled or disabled)

[Example] Clearing the timer 6 interrupt request distinguish bit

```
LDA $00EA
```

```
ORA XX1X1X0XB
```

↑ ↑ ↑

Of the interrupt request distinguish bits, only the interrupt request distinguish bit for timer 6, which is to be cleared, should be set to "0" The values of bits marked "x" are determined by the control being effected

↓ ↓ ↓

```
AND XX1X1X0XB
```

```
STA $00EA
```

Because an interrupt request is generated only at the time the interrupt request distinguish bit is set (to "1"), no interrupt will be generated while the interrupt request distinguish bit remains in the set state. For this reason, the interrupt request distinguish bit must be cleared by software in the interrupt service routine.

Note that only method of ① can be used in the M37413M4-XXXFP.

Since the BRK instruction interrupt and the timer 6 or A-D, interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if timer 6 or A-D generated the interrupt.

Table 1. Interrupt vector address and priority

Event	Priority	Vector addresses	Remarks
RESET	1	3FFF ₁₆ , 3FFE ₁₆	Non-maskable
INT ₁ interrupt	2	3FFD ₁₆ , 3FFC ₁₆	External interrupt
Serial I/O or timer 2 interrupt	3	3FFB ₁₆ , 3FFA ₁₆	
INT ₃ or key on wake up interrupt	4	3FF9 ₁₆ , 3FF8 ₁₆	External interrupt
INT ₂ or timer 3 interrupt	5	3FF7 ₁₆ , 3FF6 ₁₆	External interrupt (INT ₂)
Timer 6 or A-D interrupt (BRK instruction interrupt)	6	3FF5 ₁₆ , 3FF4 ₁₆	(Non-maskable software interrupt)

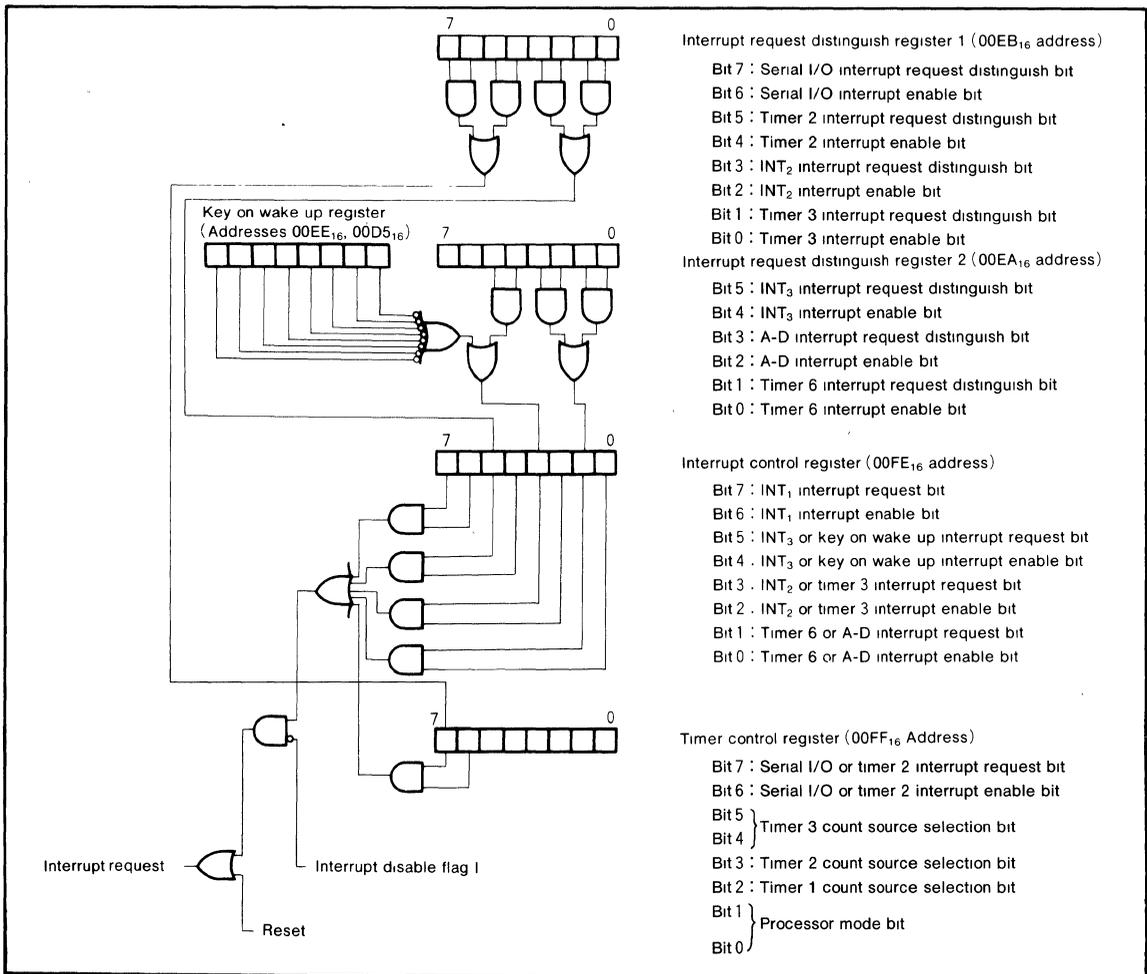


Fig. 3 Interrupt control

TIMER

The M37413M4HXXFP has six timers; timer 1, timer 2, timer 3, timer 4, timer 5 and timer 6.

A block diagram of timer1 through 6 is shown in Figure 4.

The count source for timer 1 through 3 can be selected by using bit 2, 3, 4 and 5 of the timer control register (address $00FF_{16}$), as shown in Figure 5. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch.

Timer 2, 3 and 6 has interrupt generating functions. The timer interrupt request bit which is in the interrupt distinguish register 1 or 2 (located at addresses $00EB_{16}$ and $00EA_{16}$ respectively) is set at the next count pulse after the timer reaches "0" (see interrupt section).

The starting and stopping of timer1 is controlled by bit 7 of the interrupt distinguish register 2, timer 3 by bit 6 of the interrupt distinguish register 2 and timer 4 by bit 3 of timer 4, 5 and 6 mode register ($00F8_{16}$ address). If the corresponding bit is "0", the timer starts counting, and the corresponding bit is "1", the timer stops. The timer4 overflow signal divided by 2 can be outputted from port $P3_3$ by setting the bit 4 of the serial I/O mode register ($00F6_{16}$ address) to "1".

Timer 5 and 6 work as timer mode, event counter mode and PWM mode by changing the contents of bit 5 and bit 6 of the timer 4, 5 and 6 mode register.

(1) Timer Mode

This mode is the 16-bit timer, and the count source is $\phi/4$. When the bit 6 of PWM control register ($00F3_{16}$ address) is "1", the timer6 overflow signal divided by 2 is output from CNT_2 pin (common with $P5_2$).

(2) Event Counter Mode

The count source is input from the CNT_2 pin. The count decremented each time the input goes from "L" to "H".

(3) PWM Mode

As shown in Figure 6, the output wave is controlled by the contents of the timer latch of timer 5 and 6.

PWM output can choose among PWM0, PWM1, PWM2 and PWM3 by bit 0, bit 1, bit 2 and bit 3 of PWM control register.

When the count value of all timers, from timer 1 to timer 6, are read, be careful not to change the input source.

When the count source is inputted from the external pin, the minimum pulse width should be $8\mu s$.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 5 of the timer control register). This state is canceled if timer2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 7 of the interrupt request distinguish register2 (timer1 count stop bit), bit 5 of the interrupt request distinguish register1 and bit 6 and bit 7 of the timer control

register must be set to "0". And also bit 4 of the interrupt request distinguish register1 must be set to "1". For more details on the STP instruction, refer to the oscillation circuit section.

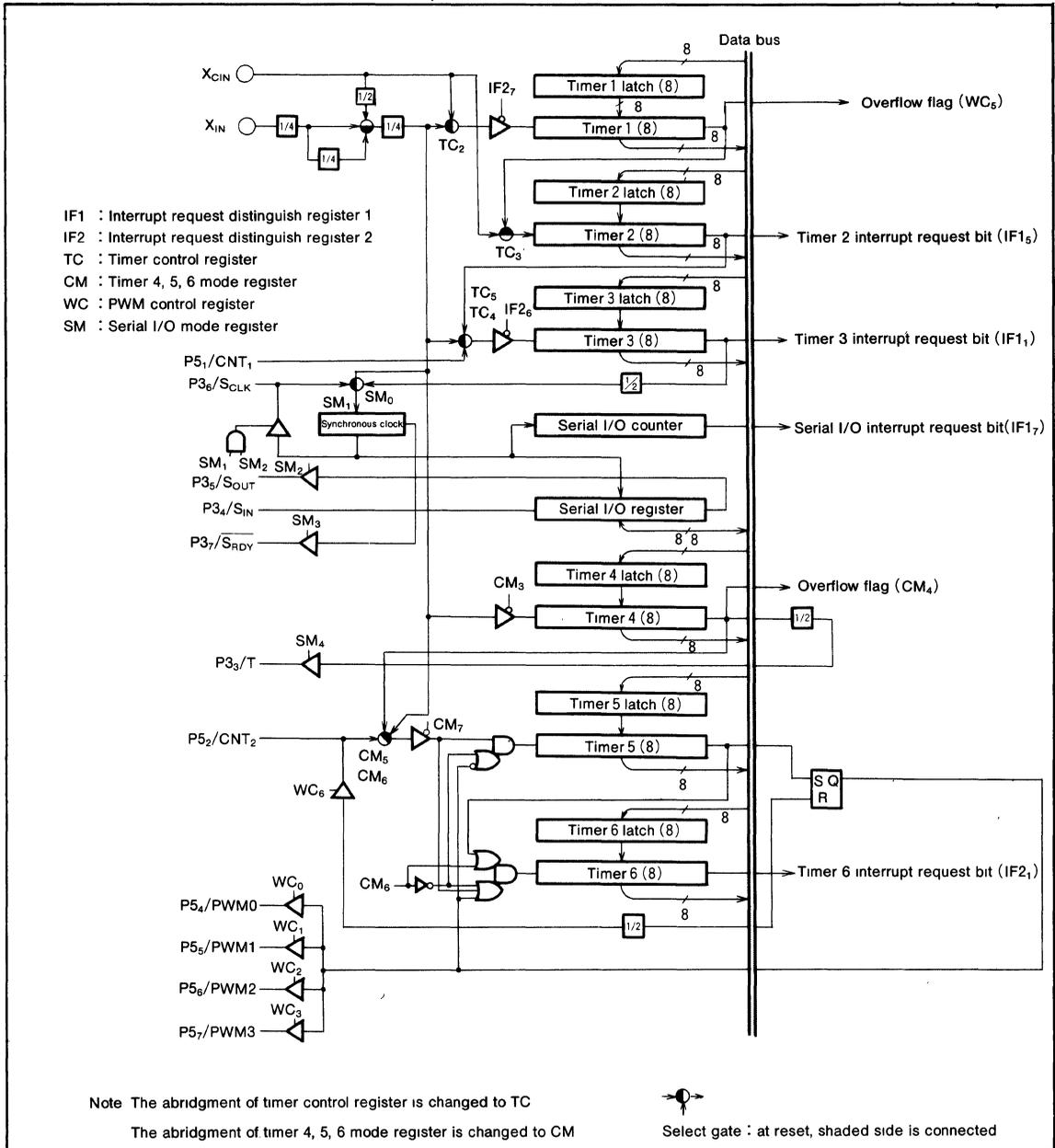


Fig. 4 Block diagram of timer 1 through 6

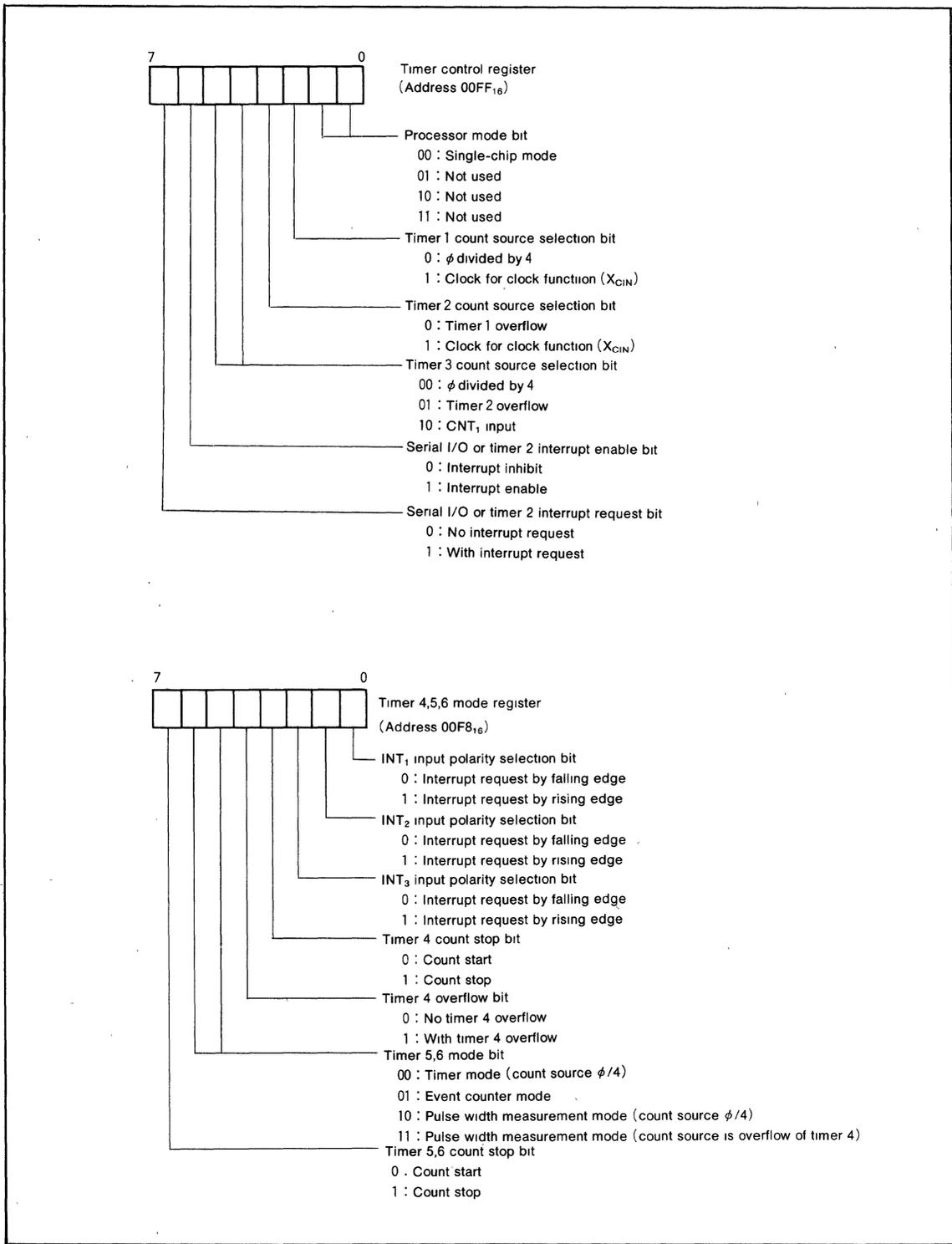


Fig. 5 Structure of timer control register and timer 4,5,6 mode register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PWM

M37413M4HXXFP has a pulse width modulated (PWM) output control circuit connecting with timer5 and timer6.

Figure 5 shows the structure of timer 4,5,6 mode register, Figure 6 shows the PWM rectangular wave form and Figure 7 shows the structure of PWM control register.

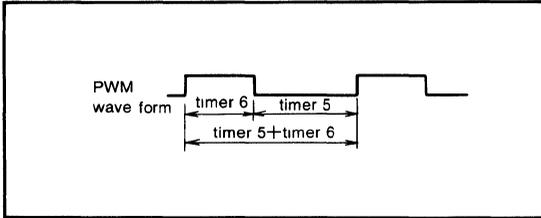


Fig. 6 PWM rectangular wave form

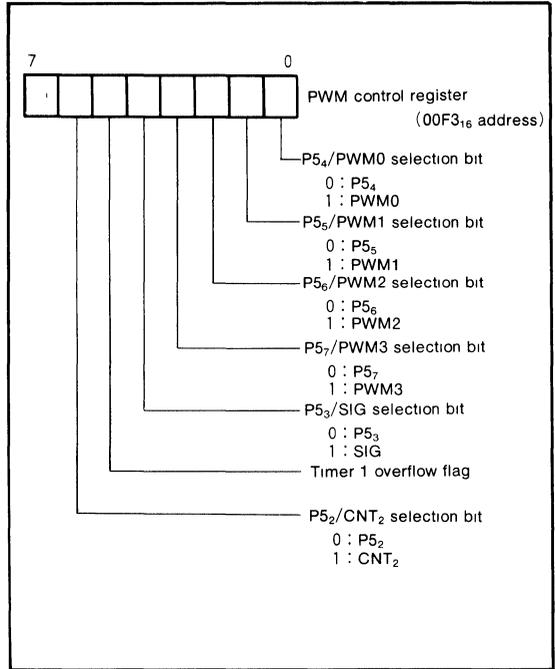


Fig. 7 Structure of PWM control register

SERIAL I/O

The block diagram of serial I/O is shown in Figure 9. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT} , S_{IN}) pins are used as P3₇, P3₆, P3₅, and P3₄, respectively.

FUNCTION OF SERIAL I/O MODE REGISTER

The serial I/O mode register (address 00F6₁₆) is an 8-bit register. Bit 7 and 0 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from P3₆ is selected. When these bits are [10], the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", P3₆ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P3₆. If the external synchronous clock is selected, the clock is input to P3₆. And P3₅ will be a serial output and P3₄ will be a serial input. To use P3₄ as a serial input, set the directional register bit which corresponds to P3₄, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" P3₆ will function as a normal I/O. Bit 3 determines if P3₇ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 3="0").

OPERATION OF SERIAL I/O

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock — The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37413M4HXXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to P3₅. During the rising edge of this clock, data can be input from P3₄ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock — If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. When the external clock is chosen, the P3₆ pin must be held at "H" level while the serial I/O is not used.

Timing diagrams are shown in Figure 10, and connection between two M37413M4HXXXFP's are shown in Figure 11.

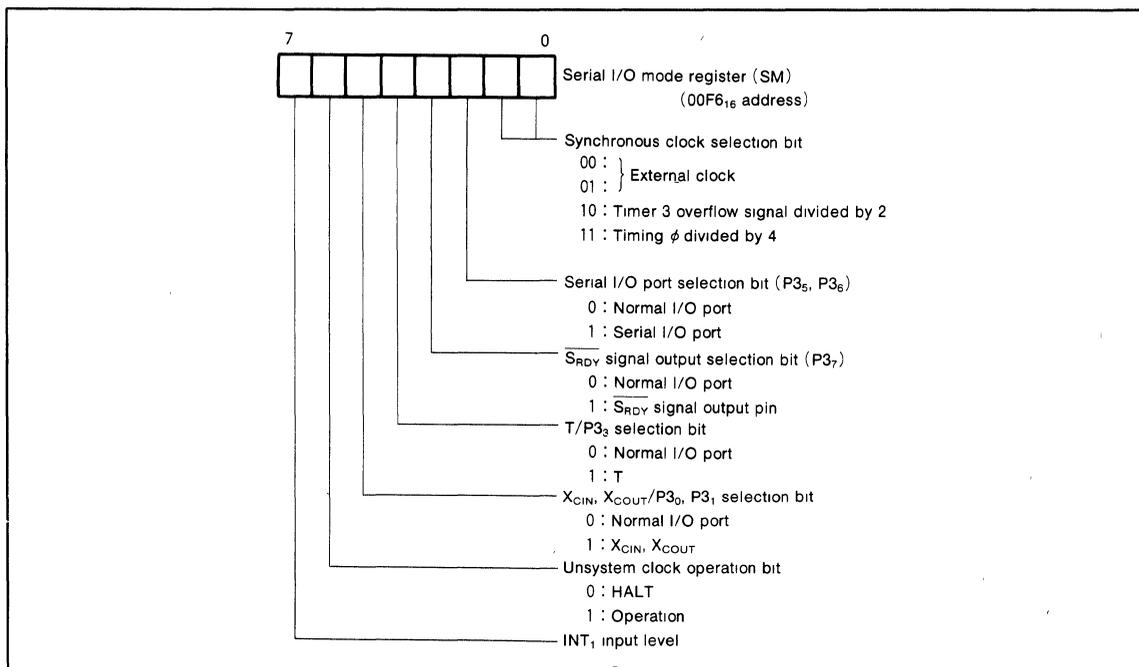


Fig. 8 Structure of serial I/O mode register

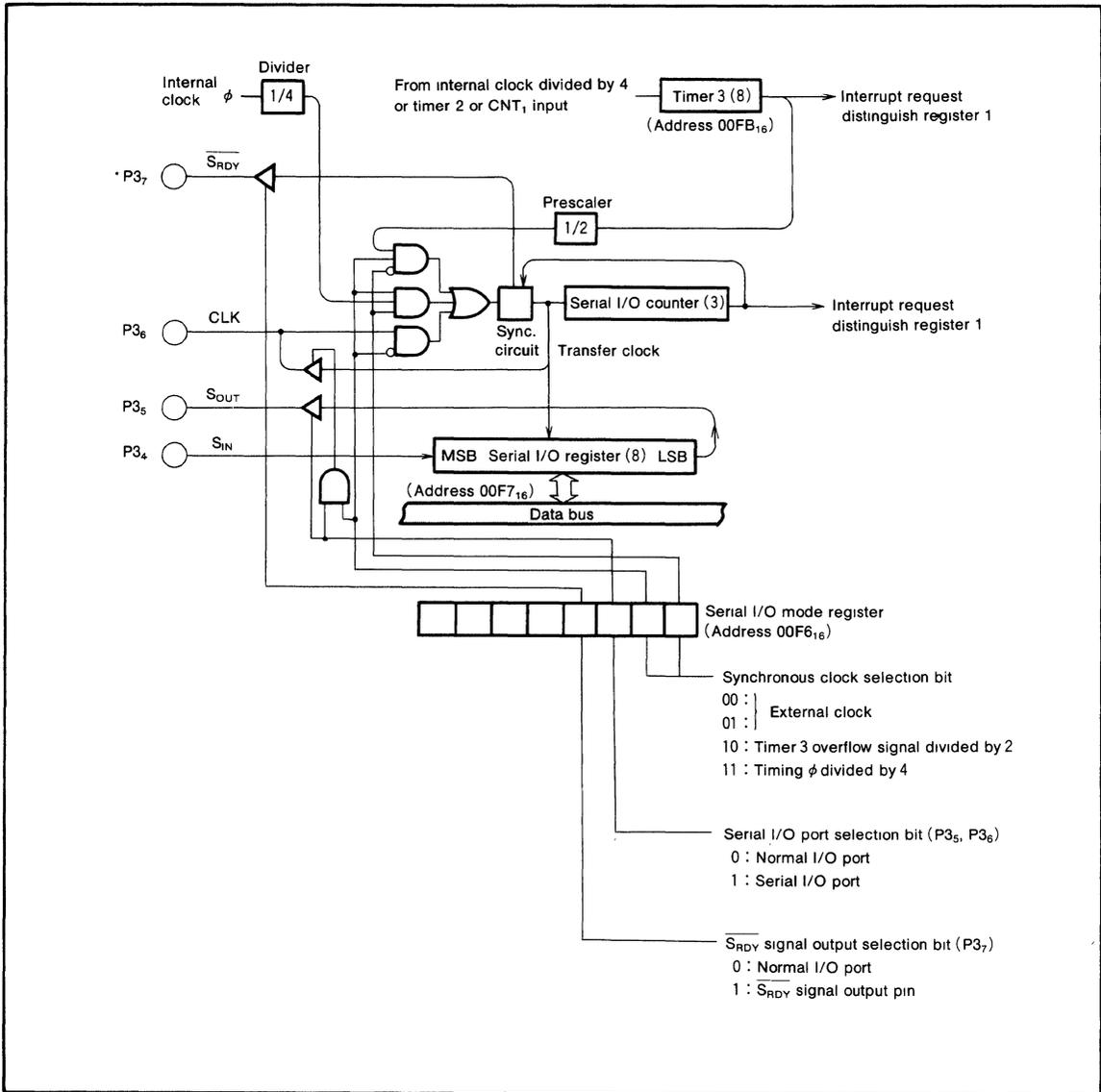


Fig. 9 Block diagram of serial I/O

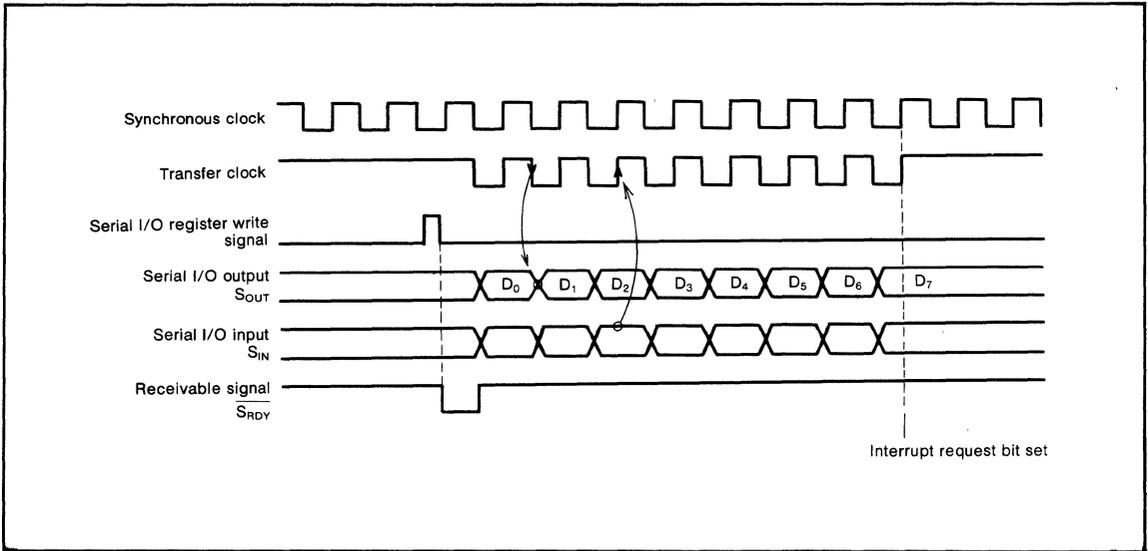


Fig. 10 Serial I/O timing

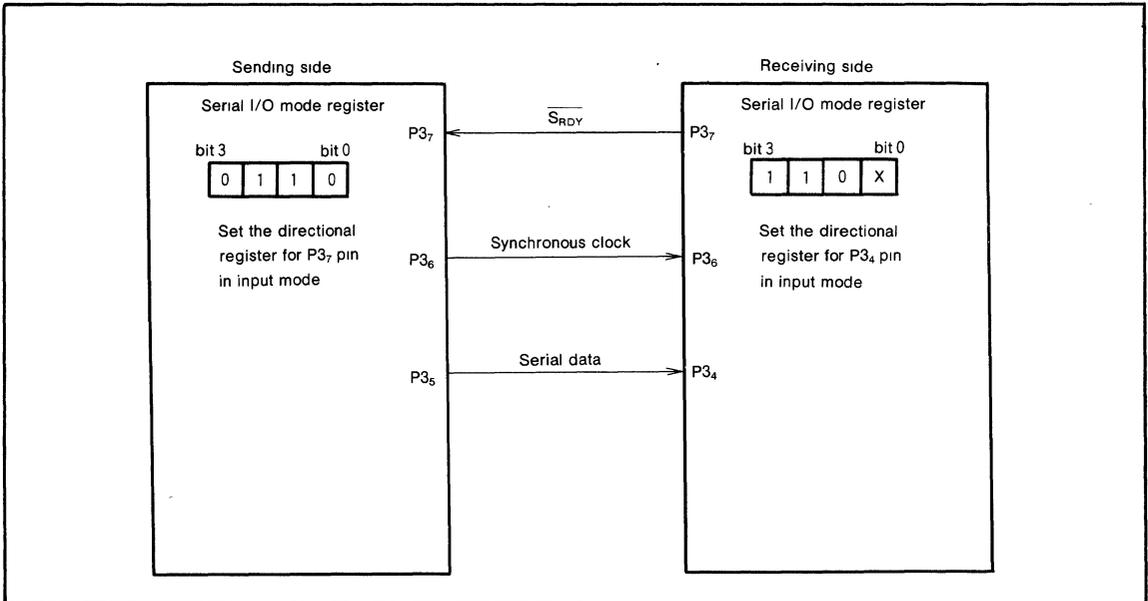


Fig. 11 Example of serial I/O connection

A-D CONVERTER

The A-D converter circuit is shown in Figure 12. One of the eight analog input ports of the A-D converter ($IN_0 \sim IN_7$) are selected by bits 0, 1 and 2 of the A-D control register. The IN pins, not to use as analog input, uses as input port. Bit 0, 1 and 2, and corresponding to analog input pin is shown in Figure 13. A-D conversion is accomplished by first selecting bit 3 and 4 of the A-D control register (address $00F2_{16}$) for the source of V_{REF} . And also the analog input pin is chosen by the analog input select bit of the A-D control register. A-D conversion starts by writing a dummy data to the A-D register or changing the input level from SIG pin "H" to "L". When A-D conversion is finished, an interrupt is generated. After A-D interrupt is accepted, the result of A-D conversion can be read from the A-D register. Note that the A-D conversion must be started to convert after the reference voltage reaches stable level.

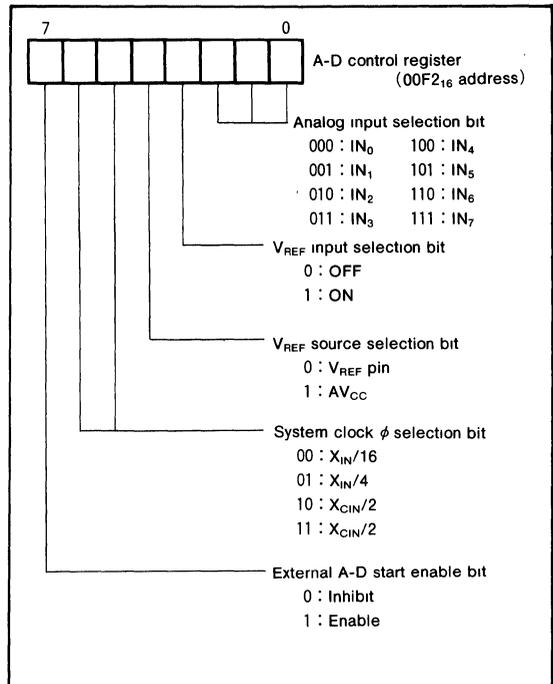


Fig. 13 Structure of segment control register

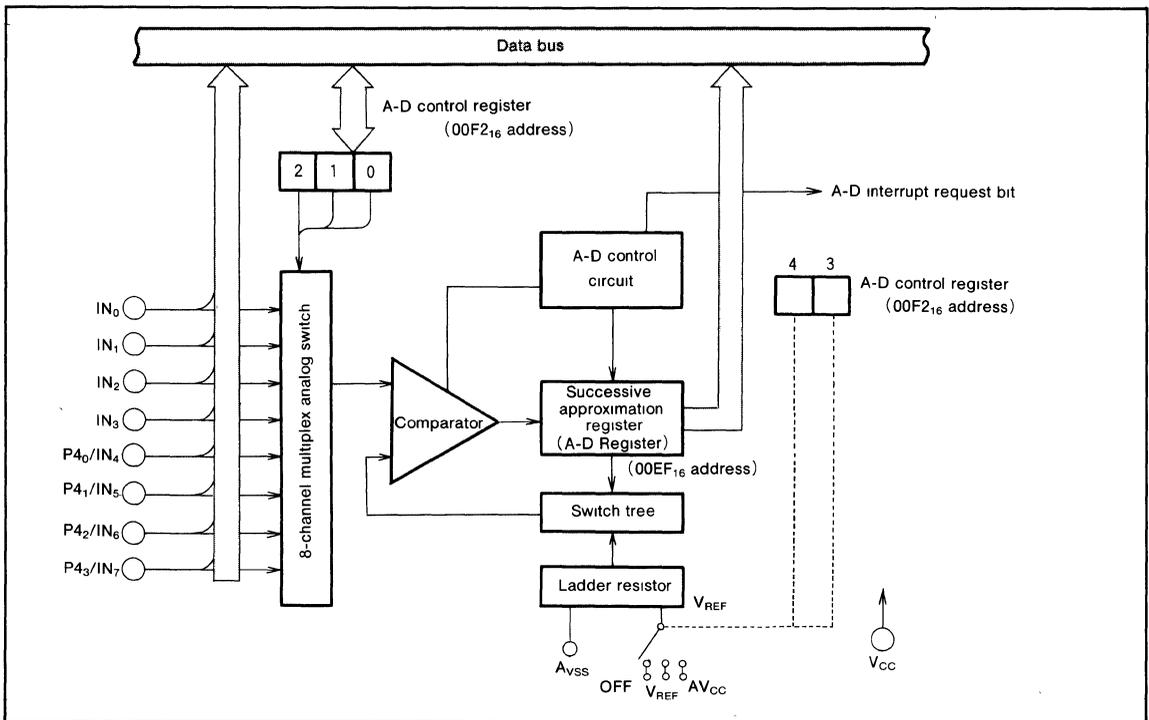


Fig. 12 A-D converter circuit

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction.

When the key on wake up option of port P2 and port P7 are designated and key on wake up interrupt enable bit (IC_4) is set to "1", if the key on wake up option pin of port P2, P7 have "L" level applied, key on wake up interrupt is generated and the microcomputer is returned to the normal operating state.

When the bit 4 of PWM control register (address 00F3₁₆) is set to "1", the pulse shown in Figure 14 is outputted from P5₃ pin.

As shown in Figure 15, if the key matrix of active "L" to input port P2, P7 are constructed, the microcomputer is returned to normal operating state by the key push. Refer to the section of interrupt how to use the key on wake up function. In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and IC_4 is "1", the input designated as key on wake up by option in port P2, P7 must be all "H".

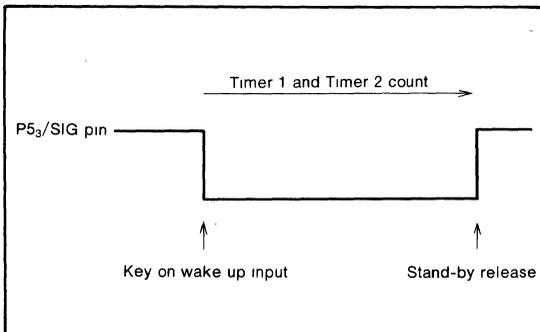


Fig. 14 Output from the SIG pin at wake up from the stop state

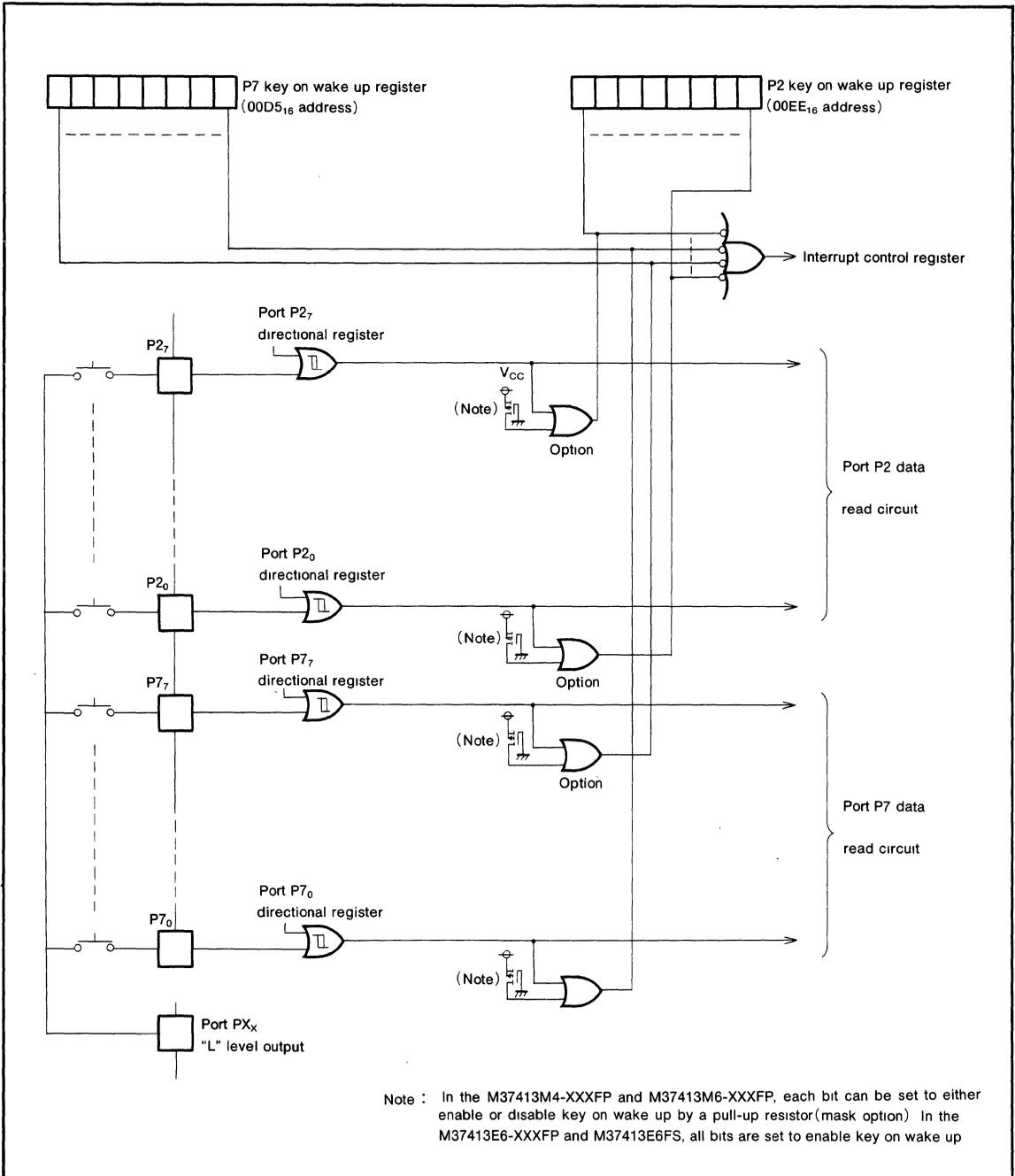


Fig. 15 Block diagram of port P2, P7 and example of wired at used key on wake up

RESET CIRCUIT

The M37413M4HXXXFP is reset according to the sequence shown in Figure 18. It starts the program from the address formed by using the content of address 3FFF₁₆ as the high order address and the content of the address 3FFE₁₆ as the low order address, when the RESET pin is held at "L" level for no less than 16 μs while the power voltage is between 4 and 5.5V and the crystal oscillator oscillation is stable and then returned to "H" level.

The internal initializations following reset are as shown in Figure 16 regardless of the status before reset (including stop mode or wait mode).

An example of the reset circuit is shown in Figure 17.

When the power on reset is used, the RESET pin must be input "H" after the oscillation of X_{IN}-X_{OUT} becomes stable.

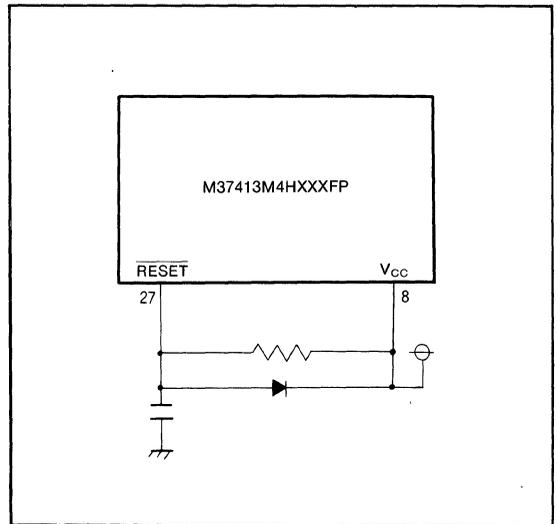


Fig. 17 Example of reset circuit

	Address	
(1) Port P0 directional register (D0) (E1 ₁₆)...		00 ₁₆
(2) Port P1 directional register (D1) (E3 ₁₆) .		00 ₁₆
(3) Port P2 directional register (D2) (E5 ₁₆)...		00 ₁₆
(4) Port P3 directional register (D3) (E9 ₁₆)...		00 ₁₆
(5) Port P5 directional register (D5) (ED ₁₆)...		00 ₁₆
(6) Port P6 directional register (D6) (D1 ₁₆)...		00 ₁₆
(7) Port P7 directional register (D7) (D3 ₁₆)...		00 ₁₆
(8) Interrupt request distinguish register 1 (IF1) (EB ₁₆)...		00 ₁₆
(9) Interrupt request distinguish register 2 (IF2) (EA ₁₆)...		00 ₁₆
(10) PWM control register (WC) (F3 ₁₆)...		0 0 0 0 0 0 0 0
(11) Serial I/O mode register (SM) (F6 ₁₆)...		— 0 0 0 0 0 0 0 0
(12) Timer 4, 5, 6 mode register (CM) (F8 ₁₆)...		00 ₁₆
(13) Interrupt control register (IM) (FE ₁₆)...		00 ₁₆
(14) Timer control register (TC) (FF ₁₆)...		00 ₁₆
(15) A-D control register (AC) (F2 ₁₆)...		0 0 0 0 0 0 — —
(16) Processor status register		— — — — 1 — —
(17) Program counter (PC _H)...		Contents of address 3FFF ₁₆
(PC _L)...		Contents of address 3FFE ₁₆

Note : Since the contents of both registers other than those listed above (including timers, A-D control register and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

Fig. 16 Internal state of microcomputer at reset

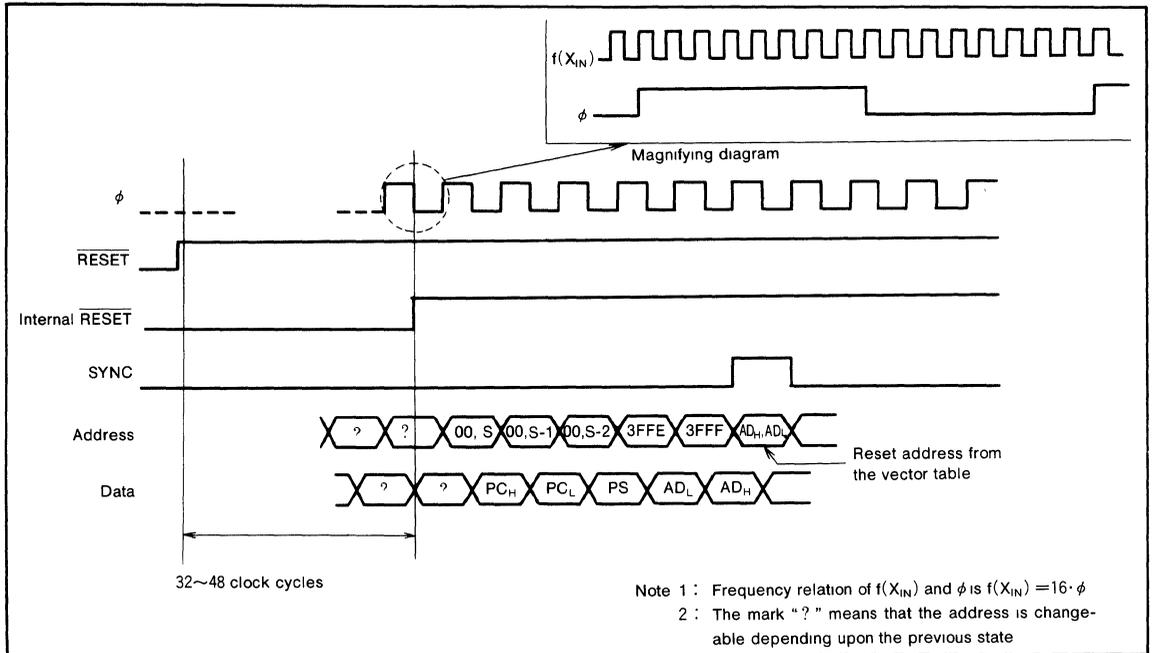


Fig. 18 Timing diagram at reset

I/O PORTS

- (1) Port P0
Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address 00E0₁₆. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address 00E1₁₆) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state. This port can be built in a pull-up resistor option when it is used as an input port.
- (2) Port P1
Port P1 has the same function as P0 but the output structure is N-ch open drain. This port can be built in a pull-up resistor option when it is used as an input port.
- (3) Port P2
Port P2 has the same function as P0. The output structure is CMOS outputs. This port can be built in a pull-up resistor option when it is used as an input port. Following the execution of STP or WIT instruction, key matrix with port P2 can be used to generate the interrupt to bring the microcomputer back in its normal state. The pin to be used as the key on wake up must be with key on wake up option and its value in directional register must be "0".
- (4) Port P3
Port P3 has the same functions P0 except that part of P3 is common with the serial I/O, output of timer4, clock oscillation of timer clock and interrupt input. The output is N-channel open drain. This port can be built in a pull-up resistor option. When P3₀ and P3₁ pins are used for X_{CIN} input, pull-up is inhibited.
- (5) Port P4
Port P4 is an 8-bit input port. P4₀~P4₃ are in common with the IN₄~IN₇. This port can be built in a pull-up resistor option when it is used as an input port.
- (6) Port P5
Port P5 has the same functions as P0 except that part of P5 is common with the counter input pin, SIG pin, and PWM output pin. The output is N-channel open drain output. This port can be built in a pull-up resistor option.
- (7) Port P6
Port P6 has the same function as P0 but the output structure is N-ch open drain. This port can be built in a pull-up resistor option.
- (8) Port P7
Port P7 has the same function as P0. The output structure is CMOS outputs. This port can be built in a pull-up resistor option when it is used as an input port. Following the execution of STP or WIT instruction, key matrix with port P7 can be used to generate the interrupt to bring the microcomputer back in its normal state. The pin to be used as the key on wake up must be with key on wake up option and its value in directional register must be "0".
- (9) Analog input(IN₀~IN₇)
This is a port for an analog input of A-D converter. IN₄~IN₇ are in common with the P4₀~P4₃.
- (10) INT₁
The INT₁ pin is an interrupt input pin. The INT₁ interrupt request bit (bit 7 of address 00FE₁₆) is set to "1" when the input level of this pin changes from "H" to "L" (or "L" to "H"). This input level is read in the bit 7 of serial I/O mode register (address 00F6₁₆).
- (11) INT₂(P3₂/INT₂)
The INT₂ pin is an interrupt input pin common with P3₂. When P3₂'s directional register is set for input ("0"), this pin can be used as an interrupt input. The INT₂ interrupt request bit (bit 3 of address 00EB₁₆) is automatically set to "1" when the input level of this pin changes from "H" to "L" (or from "L" to "H").
- (12) INT₃(P5₀/INT₃)
The INT₃ pin is an interrupt input pin common with P5₀. The other functions are the same as INT₂.

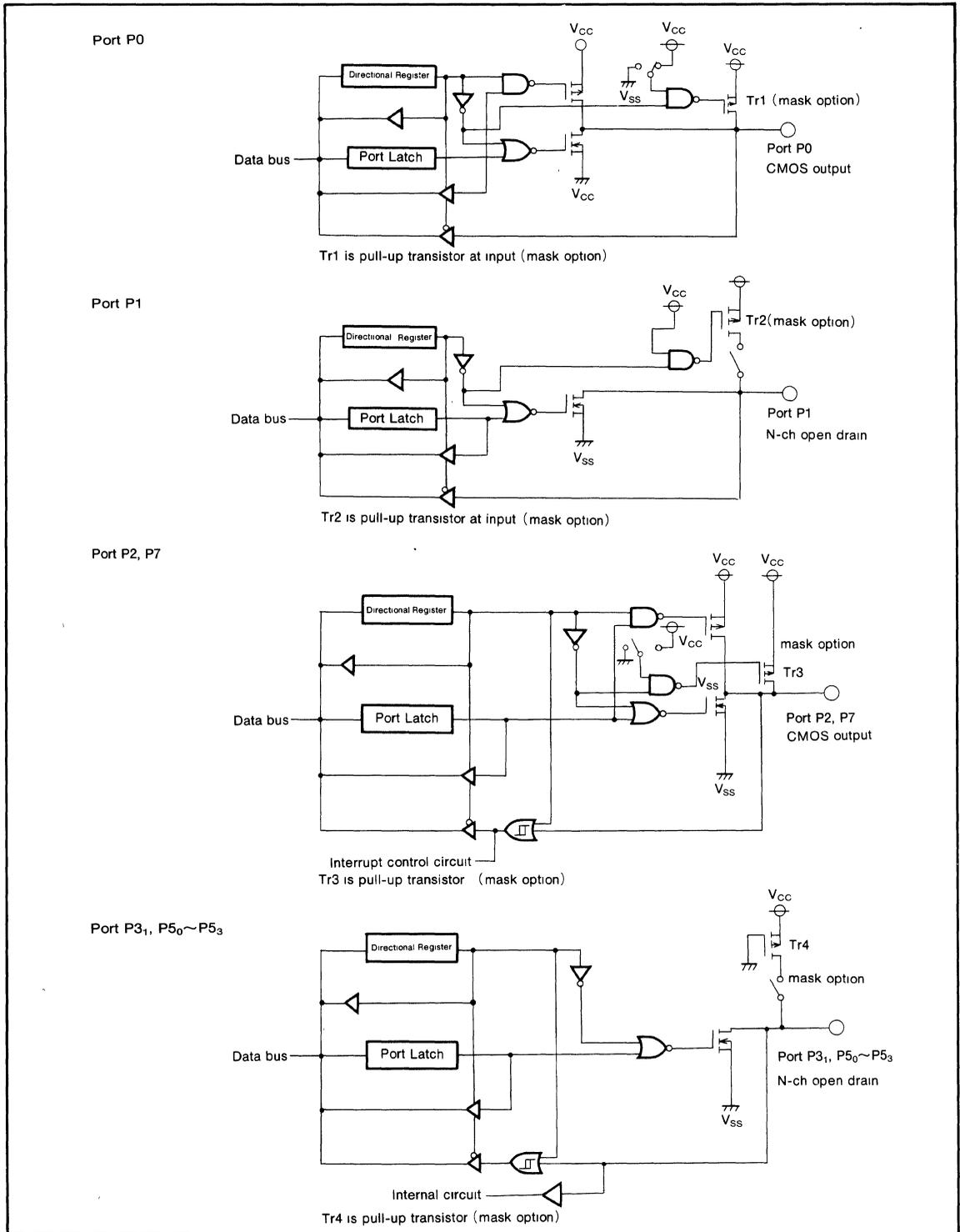


Fig. 19 Block diagram of ports P0~P2, P3, P5, P53 and P7

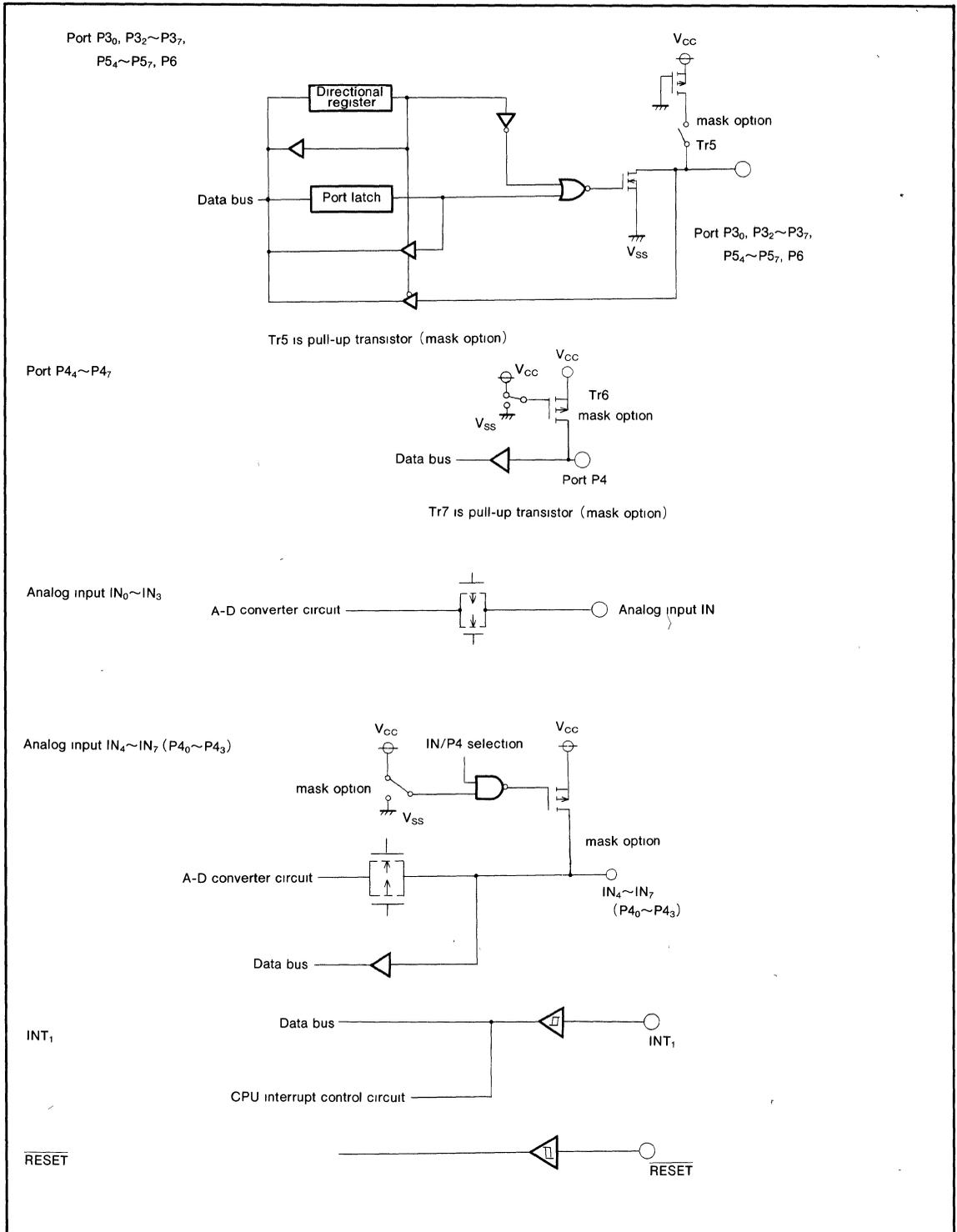


Fig. 20 Block diagram of ports P3₀, P3₂~P3₇, P4, P5₄~P5₇, P6, analog input port IN, INT₁, RESET

CLOCK GENERATING CIRCUIT

The M37413M4HXXXFP has two internal clock generators. Figure 23 shows a block diagram of the clock generator. Normally, the frequency applied to the clock input pin X_{IN} divided by 16 is used as the internal clock (timing output) ϕ . The internal clock ϕ can be changed to 1/4 the frequency applied to the clock input pin X_{IN} or 1/2 the frequency applied to the clock input pin X_{CIN} . When $X_{CIN}/2$ is selected, the pull-up option to $P3_0, P3_1$ pins are inhibited. These signals can be changed via bit5 (AC_5) and bit6 (AC_6) of the A-D control register. When AC_6 and AC_5 are [00], the internal clock is chosen $X_{IN}/16$. When they are [01], the internal clock is chosen $X_{IN}/4$. When they are [10] and [11], the internal clock is $X_{CIN}/2$. The one of clock X_{IN} and clock X_{CIN} , isn't in use for the internal clock (none system clock), stops when the bit6 (SM_6) of serial I/O mode register is "0". In order to restart the clock as the internal clock, SM_6 is set to "1" and wait until the oscillation becomes stability by the software then the internal clock is chosen AC_6 and AC_5 .

The M37413M4HXXXFP has two low power consumption modes, stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. When restarting oscillation, the internal clock ϕ is held "H" until timer 2 overflows and is not supplied to the CPU. So set the suitable value for timer 1 and timer 2 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 1 count stop bit ($IF2_7$) must be set to supply ("0"), timer 2 interrupt enable bit ($IF1_4$) of interrupt request distinguish register 1 must be set to enable ("1"), timer 2 interrupt request bit ($IF1_5$) of interrupt request distinguish register 1 must be set to "0". And serial I/O or timer 2 interrupt enable bit (TC_6) and serial I/O or timer 2 interrupt request bit (TC_7) of timer control register must be set to "0".

Oscillation is restarted (reset stop mode) when an external interrupt is received. The interrupt enable bit of the interrupt used to reset the stop mode must be set to "1".

The microcomputer enters a wait mode when WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode reset) when it receives an external interrupt or internal timer interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

When the interrupt is accepted and after the interrupt subroutine is executed, the next instruction to STP or WIT is executed. It is possible to cancel stop and wait mode by reset. In this case, the execution is started from the address is set to reset vector.

Transition of states for the system clock is shown in Figure 24. The change order of the internal clock is shown in Figure 24.

When STP instruction is executed from the states of A, B, C, D and E, it will be the same state as H (stop state). If the interrupt is executed in stop state, it will return the state before STP instruction is executed.

Figure 21 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which is unique for each oscillator. There are slight differences in constants in the M37413M4HXXXFP and M37413M6HXXXFP. If using one of these chips in applications such as high-precision clocks, ask the resonator manufacturer for measurements of these constants. When using an external clock signal, input from the $X_{IN}(X_{CIN})$ pin and leave the $X_{OUT}(X_{COUT})$ pin open. A circuit example is shown in Figure 22.

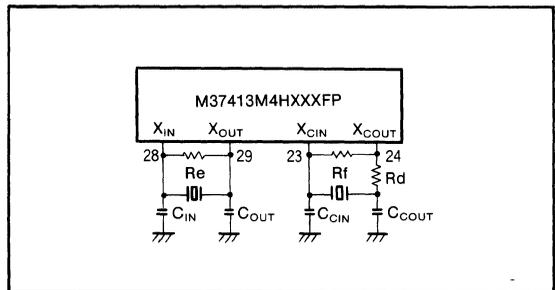


Fig. 21 External ceramic resonator circuit

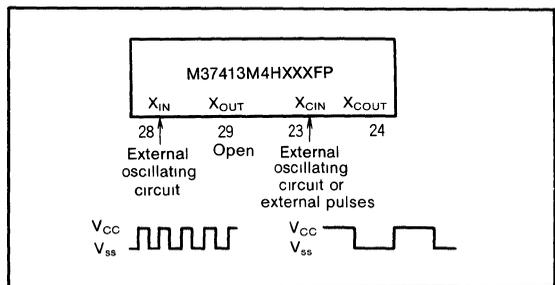


Fig. 22 External clock input circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

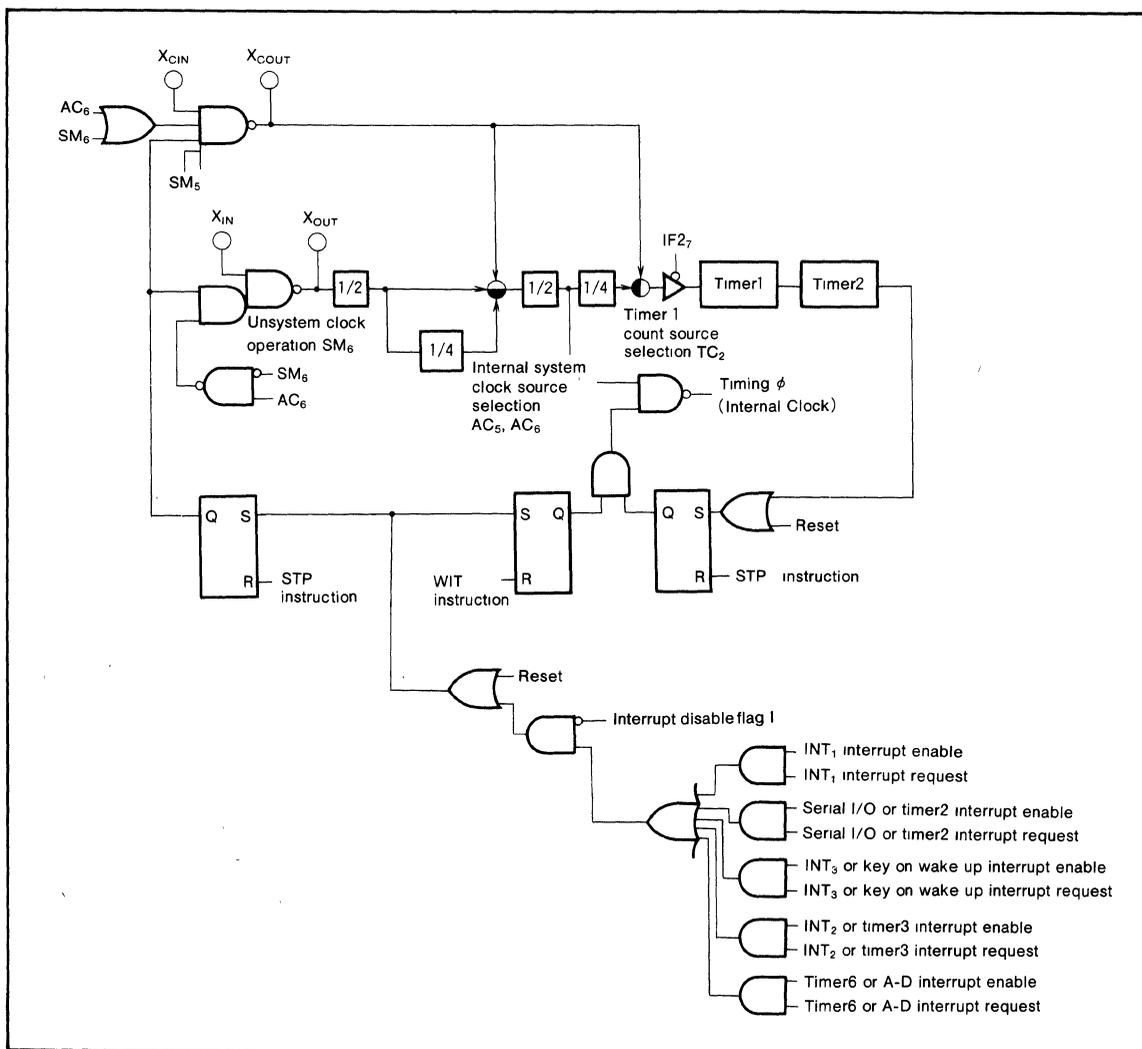
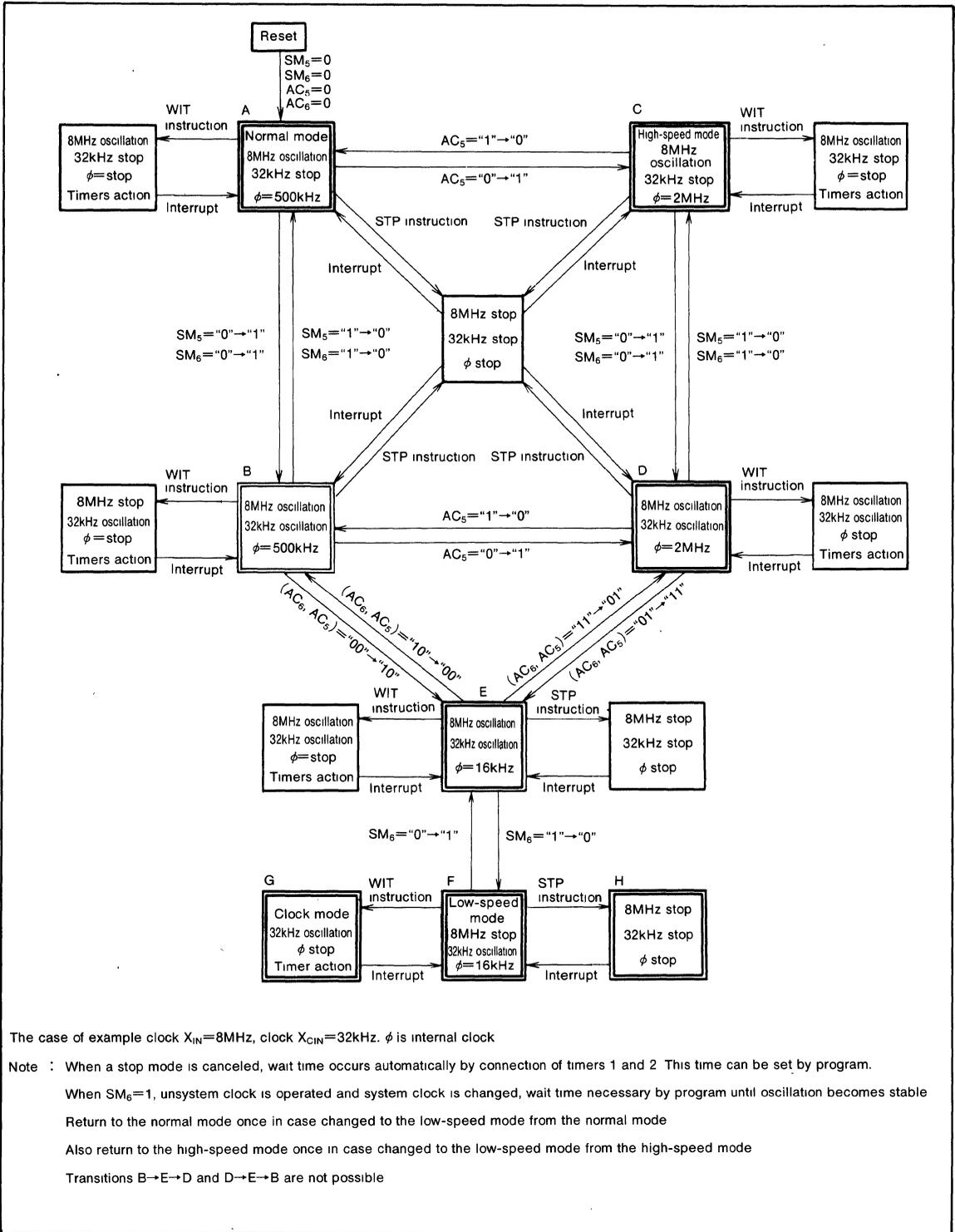


Fig. 23 Block diagram of clock generating circuit



The case of example clock $X_{IN}=8MHz$, clock $X_{CIN}=32kHz$. ϕ is internal clock

Note : When a stop mode is canceled, wait time occurs automatically by connection of timers 1 and 2 This time can be set by program.

When $SM_6=1$, unsystem clock is operated and system clock is changed, wait time necessary by program until oscillation becomes stable

Return to the normal mode once in case changed to the low-speed mode from the normal mode

Also return to the high-speed mode once in case changed to the low-speed mode from the high-speed mode

Transitions B→E→D and D→E→B are not possible

Fig. 24 Transition of states for the system clock

PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) The count value of timers 1, 2, 3, 4 can be read at an arbitrary timing when the timing ϕ divided by 4 or timer overflow is input to these timers. If X_{CIN} or CNT_1 input is input to these timers, the value of timer 1, 2, 3, 4 must be read only when the input of timers is not changing or the timer count is stopped.
Also the count value of timers 5, 6 which are used in the event counter mode must be read when the external input is at the "L" level. When timers 5, 6 are used in the timer mode, the count value of these timers cannot be read.
- (3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (4) ① After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
② In decimal mode, the negative (N), overflow (V) and zero (Z) flags are invalidated.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) ① The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.
Also the following conditions must be satisfied:
 - Timer 1 count stop bit is set to "0"
 - Timer 2 interrupt enable bit is set to "1"
 - Timer 2 interrupt request bit is set to "0"
 - Serial I/O or timer 2 interrupt enable bit is set to "0"
 - Serial I/O or timer 2 interrupt request bit is set to "0"
 ② To restart oscillation when it is stopped by STP instruction or unsystem clock operation bit, wait for a specified time which is needed for the oscillator to stabilize.
③ Connect I/O ports which are in input mode to V_{CC} or GND to get less power supply current after executing STP or WIT instruction. Connect $P5_0 \sim P5_3$ to V_{CC} or GND also in output mode.
- (7) Some instructions can be used to write contents of the interrupt request distinguish register 1, 2. If the SEB or CLB instruction or a set of instruction that acts as the SEB or CLB instruction (for instance, LDA TC+SEB 7, A+STA TC) is used, an interrupt request which is input during execution of these instructions may be cleared. Therefore, these instructions should be used only when there is no problem even if such an interrupt request is cleared. Usually, the LDM instruction or STA instruction

is used. Especially to write contents of the interrupt request distinguish register 1, 2, use the flow chart as shown in Figure 26.

- (8) After switching the serial I/O transfer clock, initialize the serial I/O counter (write to address 00F7₁₆).
- (9) To use an external clock as the serial I/O transfer clock, initialize the serial I/O counter when the external clock is "H" level.
- (10) To use the P3₀ and P3₁ pins as the I/O pins of the clock for clock function, do not use the pull-up resistors by option.
- (11) If using the A-D converter, supply power to the V_{REF} pin (set bits 3 and 4 of address 00F2₁₆), and make sure that the voltage of the V_{REF} pin has stabilized before activating the A-D conversion.

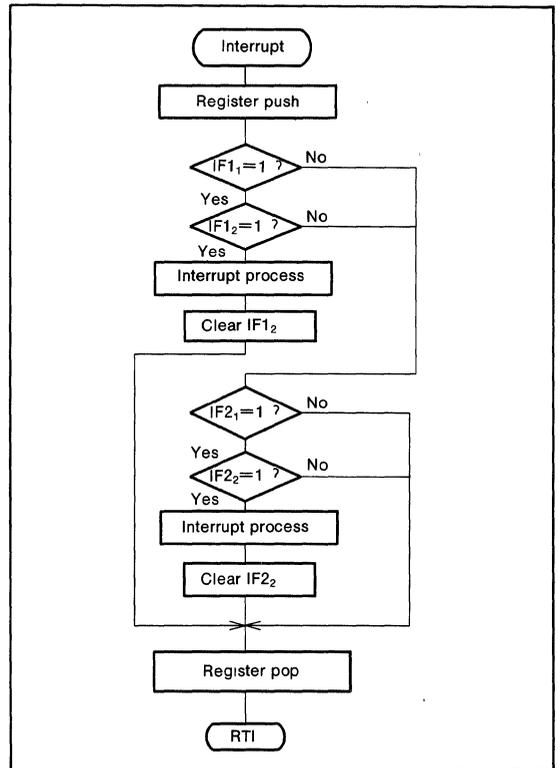


Fig. 25 Flow to write interrupt request distinguish registers

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-up transistor bit
- Port P5 pull-up transistor bit
- Port P6 pull-up transistor bit
- Port P7 pull-up transistor bit
- Port P2 key on wake up
- Port P7 key on wake up

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~7	V
AV _{CC}	Analog supply voltage	V _{CC} =AV _{CC}	-0.3~7	V
V _I	Input voltage P ₀ ~P ₀ 7, P ₂ 0~P ₂ 7, P ₃ 0, P ₃ 1, P ₄ 0~P ₄ 3, P ₇ 0~P ₇ 7, I _N 0~I _N 7, V _{REF} , X _{IN}		-0.3~V _{CC} +0.3	V
V _I	Input voltage CNV _{SS}		-0.3~7	V
V _I	Input voltage INT ₁ , RESET, P ₁ 0~P ₁ 7, P ₃ 2~P ₃ 7, P ₅ 0~P ₅ 7, P ₆ 0~P ₆ 7 (Note 1)		-0.3~10	V
V _O	Output voltage P ₀ 0~P ₀ 7, P ₂ 0~P ₂ 7, P ₃ 0, P ₃ 1, P ₇ 0~P ₇ 7, X _{OUT}		-0.3~V _{CC} +0.3	V
V _O	Output voltage P ₁ 0~P ₁ 7, P ₃ 2~P ₃ 7, P ₅ 0~P ₅ 7, P ₆ 0~P ₆ 7 (Note 1)		-0.3~10	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		-20~75	°C
T _{stg}	Storage temperature		-40~125	°C

Note 1 : When these ports are built in a pull-up resistor option, the value is -0.3~V_{CC}+0.3V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=2.5~5.5V, V_{SS}=0V, T_a=-20~75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ	Max	
V _{CC}	Supply voltage (Note 1)	f(X _{IN})= 8 MHz High-speed mode	4.5		5.5	V
		f(X _{IN})= 8 MHz Normal mode or	2.5		5.5	
		f(X _{IN})= 2 MHz High-speed mode (Note 2)				
V _{SS}	Supply voltage		0		V	
V _{IH}	"H" input voltage P ₀ 0~P ₀ 7, P ₃ 0, P ₃ 1, P ₄ 0~P ₄ 7, CNV _{SS} (Note 3)		0.7V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₂ 0~P ₂ 7		0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₁ 0~P ₁ 7, P ₅ 1~P ₅ 7, P ₆ 0~P ₆ 7, S _{IN}		0.7V _{CC}		10	V
V _{IH}	"H" input voltage P ₃ 2~P ₃ 7, P ₅ 0, INT ₁ , INT ₂ , INT ₃ , CNT ₁ , CNT ₂ , SIG, CLK		0.8V _{CC}		10	V
V _{IH}	"H" input voltage RESET, X _{IN} , X _{CIN}		0.85V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀ 0~P ₀ 7, P ₁ 0~P ₁ 7, P ₃ 0, P ₃ 1, P ₄ 0~P ₄ 3, P ₅ 1~P ₅ 7, P ₆ 0~P ₆ 7, S _{IN}		0		0.25V _{CC}	V
V _{IL}	"L" input voltage P ₂ 0~P ₂ 7, P ₃ 2~P ₃ 7, P ₅ 0, INT ₁ , INT ₂ , INT ₃ , CNT ₁ , CNT ₂ , SIG, CLK		0		0.2V _{CC}	V
V _{IL}	"L" input voltage RESET, X _{IN} , X _{CIN}		0		0.15V _{CC}	V
I _{OH}	"H" output current P ₀ 0~P ₀ 7, P ₂ 0~P ₂ 7, P ₇ 0~P ₇ 7, X _{OUT} (Note 4)				-1	mA
I _{OL}	"L" output current P ₀ 0~P ₀ 7, P ₂ 0~P ₂ 7, P ₃ 0~P ₃ 7, P ₅ 0~P ₅ 7, P ₆ 0~P ₆ 7, P ₇ 0~P ₇ 7, X _{OUT} (Note 5)				1	mA
I _{OL}	"L" output current P ₁ 0~P ₁ 7 (Note 6)	V _{CC} =3V			10	mA
		V _{CC} =5V			20	
f(X _{IN})	Clock oscillating frequency		0.2		8.2	MHz
f(X _{CIN})	Clock oscillating frequency for clock function		30		50	kHz

Note 1 : When only maintaining the RAM data, minimum value of V_{CC} is 2V

2 : We say the high-speed mode, when the system clock is chosen X_{IN}/4, and the low-speed mode, when the system clock is chosen X_{IN}/16

3 : When P₃1 is used as X_{CIN}, V_{IH} and V_{IL} of P₃1 is 0.85V_{CC} ≤ V_{IH} ≤ V_{CC} and 0 ≤ V_{IL} ≤ 0.15V_{CC}

4 : The total I_{OH}(peak) of port P₀, P₂, P₇ and X_{OUT} is less than 35mA.

5 : The total I_{OH}(peak) of port P₀, P₂, P₃, P₅, P₆ and P₇ is less than 32mA

6 : The total peak current of I_{OL} of port P₁ is less than 80mA and the average current of total I_{OL} of port P₁ is less than 40mA

M37413M4HXXFP
M37413M6HXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ELECTRICAL CHARACTERICS ($V_{SS} = 0V$, $T_a = -20 \sim 75^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit		
			Min	Typ	Max.			
V_{OH}	"H" output voltage P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P7 ₀ ~P7 ₇	$V_{CC}=5V, I_{OH}=-0.5mA$	4			V		
		$V_{CC}=3V, I_{OH}=-0.3mA$	2.4					
V_{OH}	"H" output voltage X _{OUT}	$V_{CC}=5V, I_{OH}=-0.3mA$	4			V		
		$V_{CC}=3V, I_{OH}=-0.1mA$	2.4					
V_{OL}	"L" output voltage P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , T, S _{OUT} , CLK, S _{RDY} , SIG, PWM0~PWM3	$V_{CC}=5V, I_{OL}=1mA$			1	V		
		$V_{CC}=3V, I_{OL}=0.5mA$			0.6			
V_{OL}	"L" output voltage P1 ₀ ~P1 ₇	$V_{CC}=5V, I_{OL}=20mA$ $V_{CC}=3V, I_{OL}=10mA$			2 1.5	V		
V_{OL}	"L" output voltage X _{OUT}	$V_{CC}=5V, I_{OL}=0.3mA$			1	V		
		$V_{CC}=3V, I_{OL}=0.1mA$			0.6			
$V_{T+} - V_{T-}$	Hysteresis INT ₁ , INT ₂ , INT ₃ , CLK, CNT ₁ , CNT ₂ , SIG, S _{IN} , P2 ₀ ~P2 ₇ , P7 ₀ ~P7 ₇ , X _{CIN}	$V_{CC}=5V$		0.7		V		
		$V_{CC}=3V$		0.5				
$V_{T+} - V_{T-}$	Hysteresis RESET	$V_{CC}=5V$		2		V		
		$V_{CC}=3V$		1.2				
$V_{T+} - V_{T-}$	Hysteresis X _{IN}	$V_{CC}=5V$		0.5		V		
		$V_{CC}=3V$		0.35				
I_{IL}	"L" input current [P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇] without pull-up T _r , (Note 1), INT ₁ , RESET, X _{IN}	$V_{CC}=5V, V_I=0V$			-5	μA		
		$V_{CC}=3V, V_I=0V$			-3			
I_{IH}	"H" input current P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P4 ₀ ~P4 ₇ , P7 ₀ ~P7 ₇ , X _{IN} , X _{CIN} , CNV _{SS}	$V_{CC}=5V, V_I=5V$			5	μA		
		$V_{CC}=3V, V_I=3V$			3			
I_{IH}	"H" input current [P1 ₀ ~P1 ₇ , P3 ₀ ~P3 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇] without pull-up T _r , INT ₁ , RESET	$V_I=10V$			10	μA		
R_{PL}	Pull-up T _r P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₃ , P5 ₀ ~P5 ₇	$V_{CC}=5V, V_I=0V$	12	25	50	kΩ		
		$V_{CC}=3V, V_I=0V$	25	50	100			
I_{CC}	Supply current (Note 2)	at operation	f(X _{IN})=8MHz High-speed mode $V_{CC}=5V$			6	12	mA
			f(X _{IN})=8MHz Normal mode $V_{CC}=3V$			1	4	
			f(X _{CIN})=32kHz, $V_{CC}=3V$			18	36	
		at wait mode	f(X _{IN})=8MHz, $V_{CC}=3V$				3	mA
			f(X _{CIN})=32kHz, $V_{CC}=3V$			4	12	
			T _a =25°C			0.1	1.0	
at stop mode	T _a =75°C				6.0	μA		
V_{RAM}	RAM retention voltage		2		5.5	V		

Note 1 : Also the same when each port is used as INT₂, INT₃, CNT₁, CNT₂, SIG, S_{IN} and X_{CIN}, respectively.
 2 : I/O ports or input ports are connected to V_{CC} Output ports are opened

M37413M4HXXXFP
M37413M6HXXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=8\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
—	Resolution				8	bits
—	Non-linearity error	$V_{CC}=V_{REF}=5.12V$			± 2	LSB
		$V_{CC}=V_{REF}=3.072V$			± 2	
—	Differential non-linearity	$V_{CC}=V_{REF}=5.12V$			± 0.9	LSB
		$V_{CC}=V_{REF}=3.072V$			± 0.9	
V_{OT}	Zero transition error	$V_{CC}=V_{REF}=5.12V$			2	LSB
		$V_{CC}=V_{REF}=3.072V$			2	
V_{FST}	Full-scale transition error	$V_{CC}=V_{REF}=5.12V$			6	LSB
		$V_{CC}=V_{REF}=3.072V$			10	
T_C	Conversion time	$V_{CC}=2.5\sim 5.5V$ High-speed mode		$200/f(X_{IN})$		μs
		$V_{CC}=2.5\sim 5.5V$ Normal mode		$800/f(X_{IN})$		
I_{REF}	Reference input current	$V_{REF}=5V$		1.0	2.5	mA
		$V_{REF}=3V$		0.5	1.5	
I_{IN}	Analog port input current	$V_{IN}=0\sim V_{CC}$		1	10	μA
V_{IN}	Analog input voltage	$V_{CC}=2.5\sim 5.5V$	AV_{SS}		V_{CC}	V
V_{REF}	Reference input voltage		2.5		V_{CC}	V

MITSUBISHI MICROCOMPUTERS M37414M5-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37414M5-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 72-pin plastic molded QFP.

This single-chip microcomputer is useful for household appliance and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

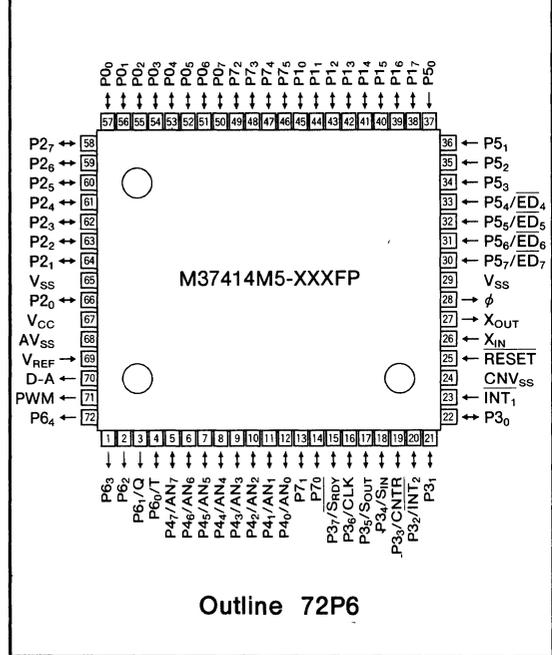
FEATURES

- Number of basic instructions..... 69
- Memory size ROM10240 bytes
RAM..... 160 bytes
- Instruction execution time
..... 2 μ s (minimum instructions at 4MHz frequency)
- Single power supply $f(X_{IN})=4\text{MHz}$5V \pm 10%
- Power dissipation
normal operation mode (at 4MHz frequency)..... 15mW
- Subroutine nesting80 levels (Max.)
- Interrupt.....7 types, 5 vectors
- 8-bit timer..... 4
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P7)..... 46
- Input port (Port P5)..... 8
- Output port (Port P6)..... 5
- Serial I/O (8-bit)..... 1
- A-D converter (8-bit resolution) 8 channels
- D-A converter (5-bit resolution) 1 channels
- 8-bit PWM function
- Watchdog timer

APPLICATION

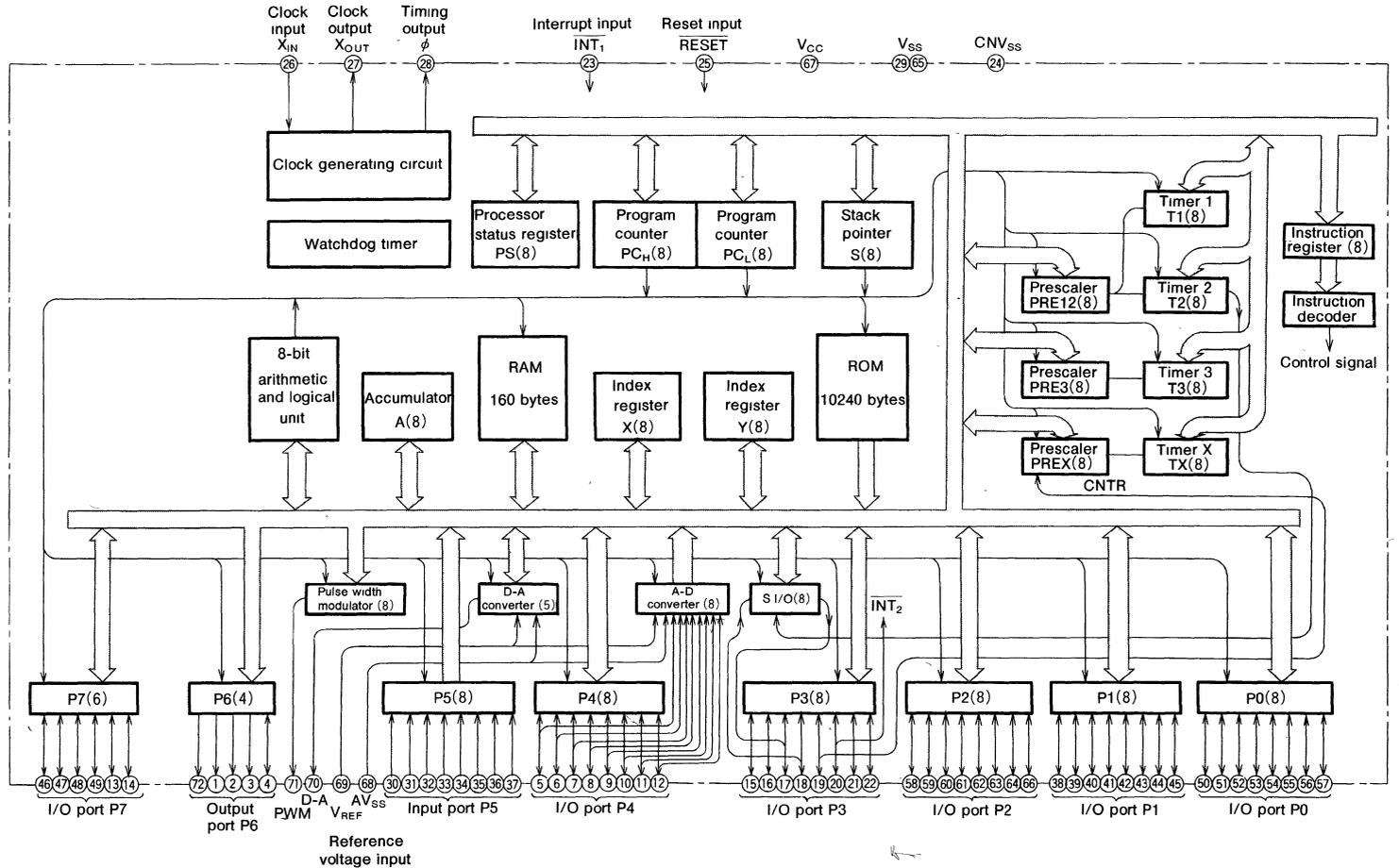
VCR, Tuner, Audio-visual equipment
Office automation equipment

PIN CONFIGURATION (TOP VIEW)





M37414M5-XXXFP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MITSUBISHI MICROCOMPUTERS
M37414M5-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37414M5-XXXFP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		2 μ s (minimum instructions, at 4MHz frequency)
Clock frequency		4MHz
Memory size	ROM	1024bytes
	RAM	160bytes
Input/Output port	INT ₁	Input 1-bit \times 1
	P0, P1, P2, P3, P4	I/O 8-bit \times 5 (a part of P3 is in common with serial I/O, timer I/O, and interrupt input)
	P5	Input 8-bit \times 1
	P6	Output 5-bit \times 1 (a part of P6 is in common with external trigger output pin)
	P7	I/O 6-bit \times 1
Serial I/O		8-bit \times 1
Timers		8-bit prescaler \times 3+8-bit timer \times 4
A-D converter		8-bit \times 1 (8 channels)
D-A converter		5-bit \times 1
Pulse width modulator		8-bit \times 1
Watchdog timer		15-bit \times 1
Subroutine nesting		80 levels (max)
Interrupt		Two external interrupts, three internal timer interrupts
Clock generating circuit		Built-in (ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 10%
Power dissipation	at high-speed operation	15mW (at 4MHz frequency)
	at low-speed operation	10mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage	12V (Ports P3, P4, P5, P6, P7 ₀ , P7 ₁ , INT ₁)
	Output current	5mA (Ports P0, P1, P2, P3, P4, P7)
Memory expansion		Possible
Operating temperature range		-10 \sim 70 $^{\circ}$ C
Device structure		CMOS silicon gate process
Package		72-pin plastic molded QFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is usually connected to V _{SS}
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected to the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin
INT ₁	Interrupt input	Input	This is the highest order interrupt input pin
AV _{SS}	Voltage input for A-D and D-A		This is GND input pin for the A-D and D-A converters
V _{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters
D-A	D-A output	Output	This is output pin from the D-A converter
PWM	PWM output	Output	This is output pin from the pulse width modulator The output structure is N-channel open drain
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ and P3 ₄ work as S _{RDY} , CLK, S _{OUT} and S _{IN} pins, respectively. Also P3 ₃ and P3 ₂ work as CNTR pin and the lowest interrupt input pin (INT ₂), respectively. The output structure is N-channel open drain
P4 ₀ ~P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. P4 ₀ ~P4 ₇ work as analog input port AN ₀ ~AN ₇ . The output structure is N-channel open drain
P5 ₀ ~P5 ₇	Input port P5	Input	Port P5 is an 8-bit input port. P5 ₄ ~P5 ₇ can be used as the edge sense inputs
P6 ₀ ~P6 ₄	Output port P6	Output	Port P6 is a 5-bit output port. At external trigger output mode, P6 ₀ and P6 ₁ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain
P7 ₀ ~P7 ₅	I/O port P7	I/O	Port P7 is a 6-bit I/O port and has basically the same functions as port P0. The output structure of P7 ₀ , P7 ₁ is N-channel open drain, and the output structure of P7 ₂ ~P7 ₅ is CMOS output

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37414 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

Timer Control Register

The timer control register is allocated to address 00FF₁₆. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

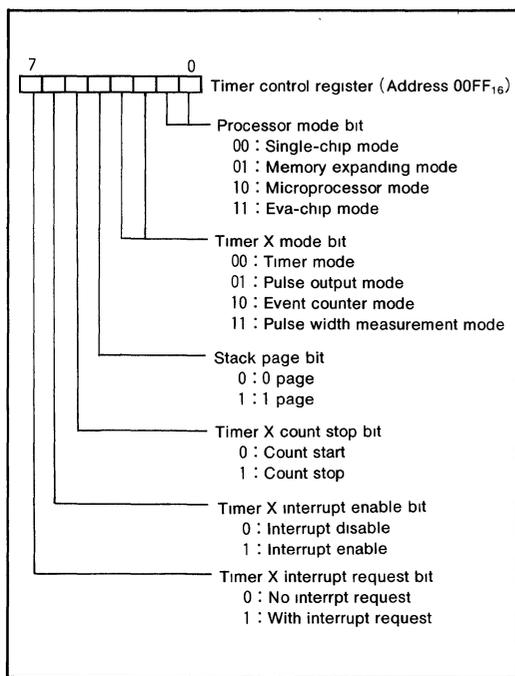


Fig.1 Structure of timer control register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

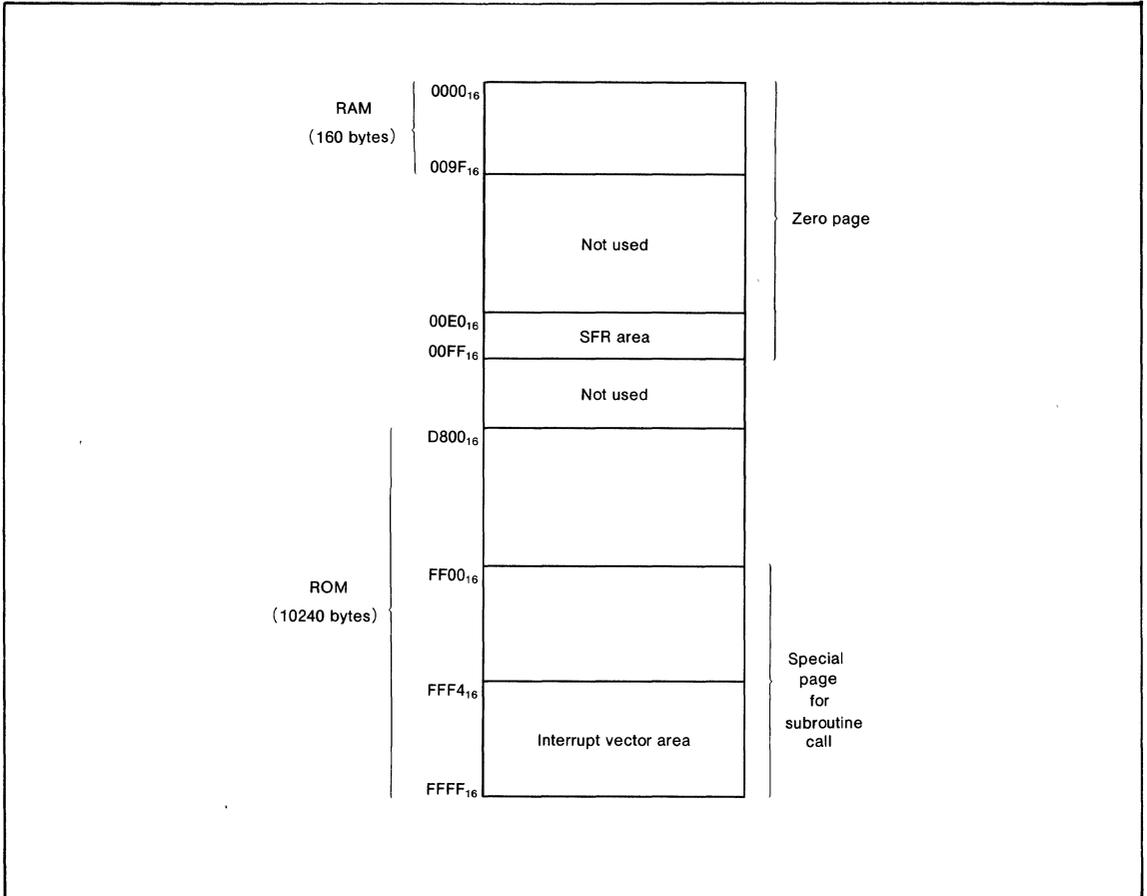


Fig.2 Memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

00E0 ₁₆	Port P0	00F0 ₁₆	D-A conversion register
00E1 ₁₆	Port P0 directional register	00F1 ₁₆	Pulse width modulation register
00E2 ₁₆	Port P1	00F2 ₁₆	Successive approximation register
00E3 ₁₆	Port P1 directional register	00F3 ₁₆	A-D control register
00E4 ₁₆	Port P2	00F4 ₁₆	Watchdog timer
00E5 ₁₆	Port P2 directional register	00F5 ₁₆	Serial I/O mode register
00E6 ₁₆	Port P7	00F6 ₁₆	Serial I/O register
00E7 ₁₆	Port P7 directional register	00F7 ₁₆	Timer 3 prescaler
00E8 ₁₆	Port P3	00F8 ₁₆	Timer 3
00E9 ₁₆	Port P3 directional register	00F9 ₁₆	Timer 1, 2 prescaler
00EA ₁₆	Port P4	00FA ₁₆	Timer 1
00EB ₁₆	Port P4 directional register	00FB ₁₆	Timer 2
00EC ₁₆	Port P5	00FC ₁₆	Timer X prescaler
00ED ₁₆	Port P5 latch	00FD ₁₆	Timer X
00EE ₁₆	Port P6	00FE ₁₆	Interrupt control register
00EF ₁₆	Special function selection register	00FF ₁₆	Timer control register

Fig. 3 SFR (Special Function Register) memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

INTERRUPT

The M37414M5-XXXFP can be interrupted from seven sources; \overline{INT}_1 , timer X, timer 1, timer 2/serial I/O, or \overline{INT}_2 /BRK instruction.

However, the \overline{INT}_2 pin is used with port P3₂ and the corresponding directional register bit should be set to "0" when P3₂ is used as an interrupt input pin.

The value of bit 2 of the serial I/O mode register (address 00F6₁₆) determine whether the interrupt is from timer 2 or from serial I/O. When bit 2 is "0" the interrupt is from timer 2, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain reg-

isters are pushed into specified locations, the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 4. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

- (1) When the \overline{INT}_1 or \overline{INT}_2 pins go from "H" to "L"
- (2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the \overline{INT}_2 interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if \overline{INT}_2 generated the interrupt.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
RESET	1	FFFF ₁₆ , FFFE ₁₆
\overline{INT}_1	2	FFFD ₁₆ , FFFC ₁₆
Timer X	3	FFFB ₁₆ , FFFA ₁₆
Timer 1	4	FFF9 ₁₆ , FFF8 ₁₆
Timer 2 or serial I/O	5	FFF7 ₁₆ , FFF6 ₁₆
\overline{INT}_2 (BRK)	6	FFF5 ₁₆ , FFF4 ₁₆

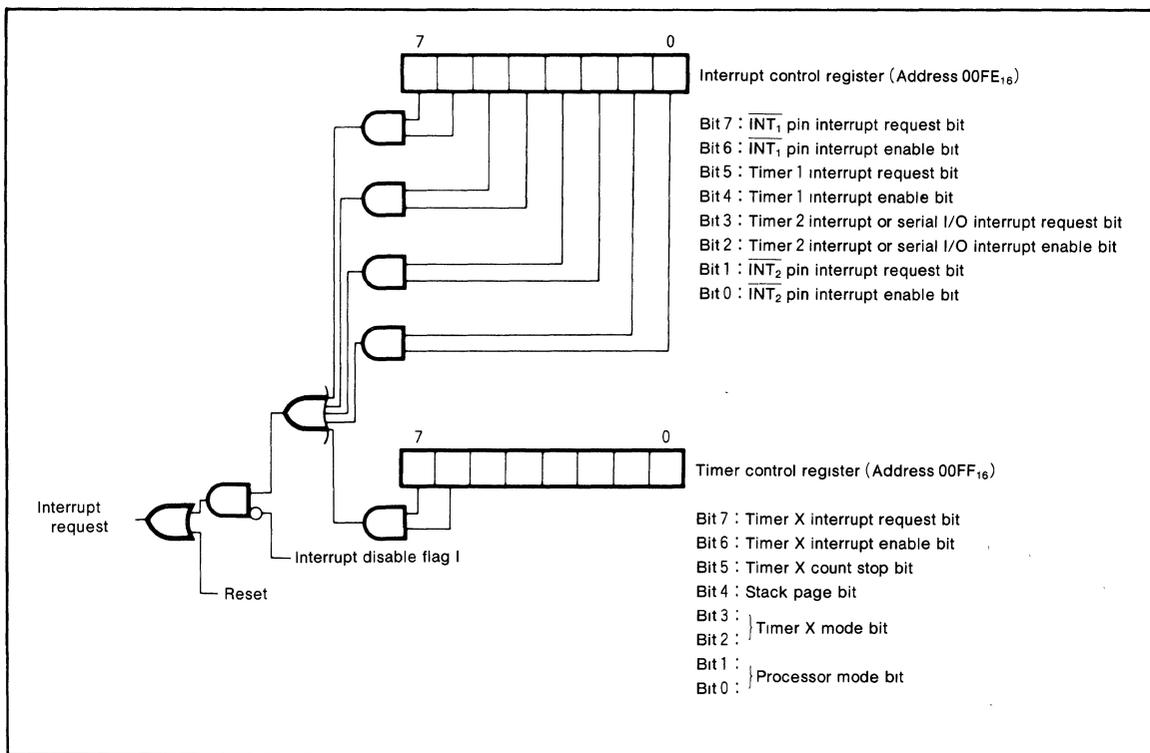


Fig.4 Interrupt control

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMER

The M37414M5-XXXFP has three timers; timer X, timer 1, timer 2 and timer 3. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1, timer 2 and timer 3 is shown in Figure 5.

The P₃/CNTR pin cannot be used as CNTR when P₃ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All four timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses 00FE₁₆ and 00FF₁₆, respectively (see Interrupt section). The prescaler latch and timer latch can be loaded with any number.

The four modes of timer X as follows:

(1) Timer mode [00]

In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]

In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]

This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]

This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 6.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF₁₆ and 01₁₆, respectively. Also, when the STP instruction is ex-

ecuted, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

The function of timer 3 is as same as that of timer 1 and timer 2, with the exception that the detection of its overflow is known by the overflow bit (bit 3 of address 00EF₁₆). When the timer down-counts to zero, the overflow bit is set to "1" and the contents of the timer's latch is reloaded into the timer.

The reset of the overflow bit is made by;

- a) hard ware reset
- b) write "0" to overflow bit
- c) write instruction to timer 3

The structure of special function selection register is shown in Figure 7.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

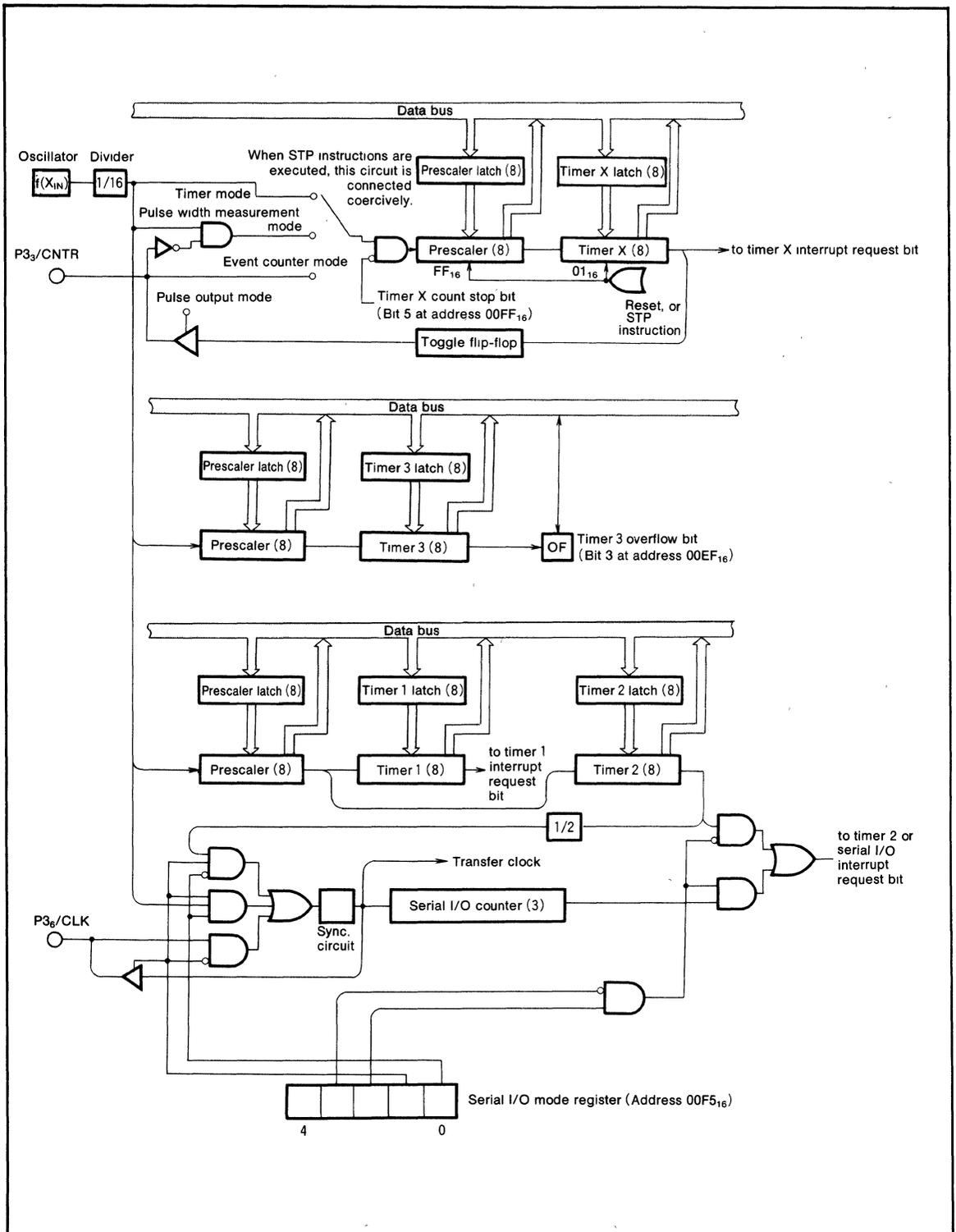


Fig.5 Block diagram of timer X, timer 1, timer 2, and timer 3

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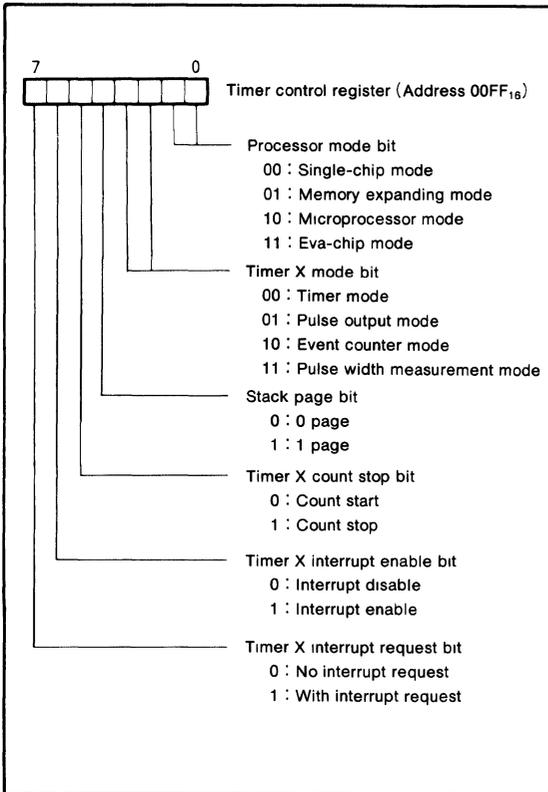


Fig.6 Structure of timer control register

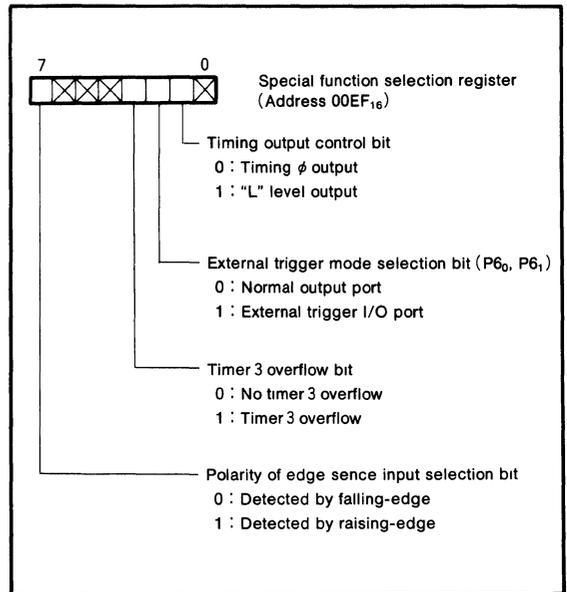


Fig.7 Structure of special function selection register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal (\overline{S}_{RDY}), synchronous input/output clock (CLK), and the serial I/O pins (S_{OUT} , S_{IN}) are used as P3₇, P3₆, P3₅, and P3₄, respectively. The serial I/O mode register (address 00F5₁₆) is a 5-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from P3₆ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the

transfer speed. When the bits are [11], the oscillator frequency divided by 16, becomes the clock. Bit 2 to 4 decide whether parts of P3 will be used as a serial I/O or not. When bit 3 is "0" and bit 2 is "1", P3₆ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P3₆. If an external synchronous clock is selected, the clock is input to P3₆ and P3₅ will be a serial output and P3₄ will be a serial input. To use P3₄ as a serial input, set the directional register bit which corresponds to P3₄ to "0". For more information on the directional register, refer to the I/O pin section.

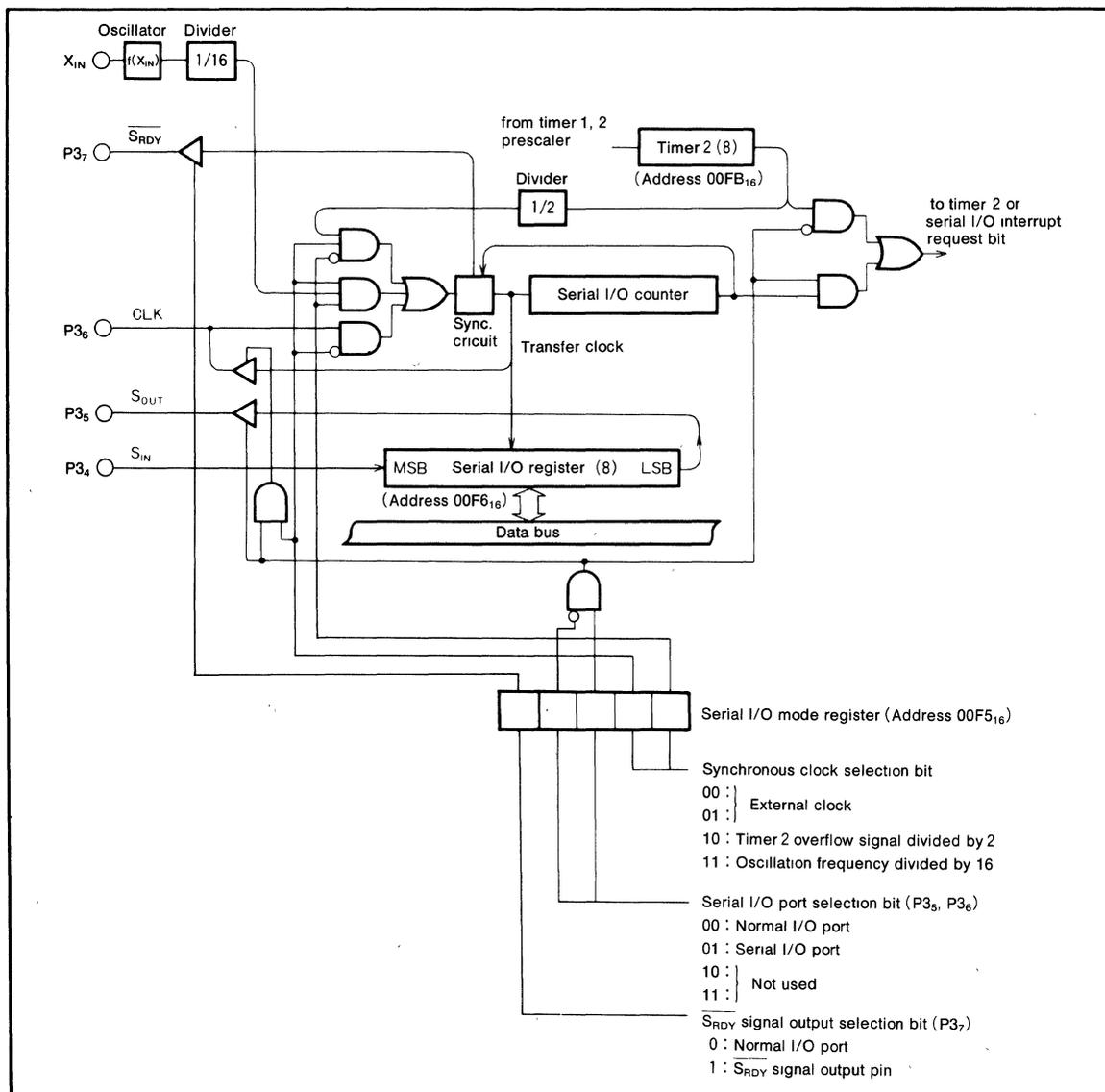


Fig.8 Block diagram of serial I/O

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To use the serial I/O, bit 3 and bit 2 need to be set to "01", if they are "00" P3₆ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 4 determines if P3₇ is used as an output pin for the receive data ready signal (bit 4=1, S_{RDY}) or used as normal I/O pin (bit 4=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The S_{RDY} signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address 00F7₁₆). After the falling edge of the write signal, the S_{RDY} signal becomes low signaling that the M37414M5-XXXFP is ready to receive the external serial data. The S_{RDY} signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling

edge of the transfer clock, serial data is output to P3₅. During the rising edge of this clock, data can be input from P3₄ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. An example of communication between two M37414M5-XXXFPs is shown in Figure 10.

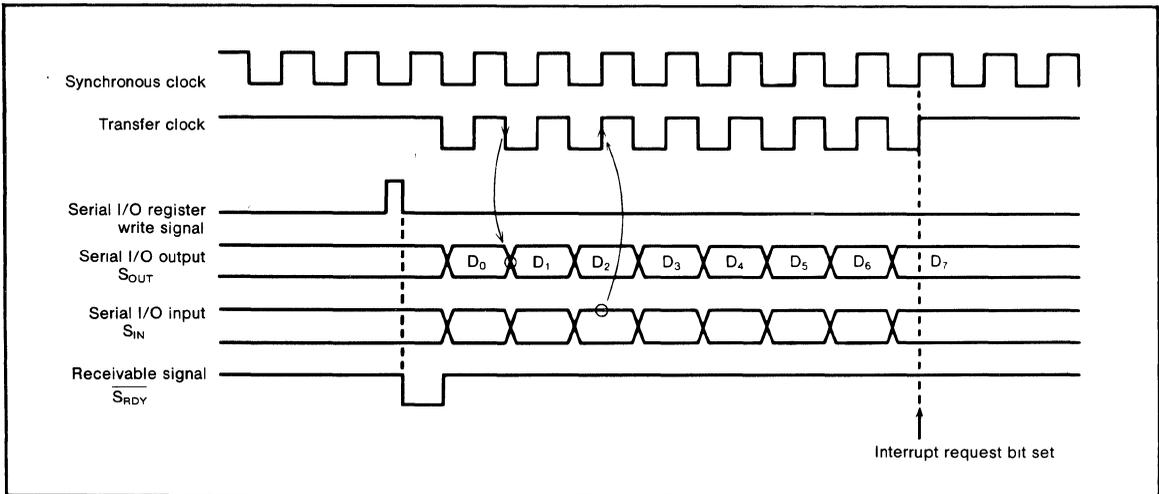


Fig.9 Serial I/O timing

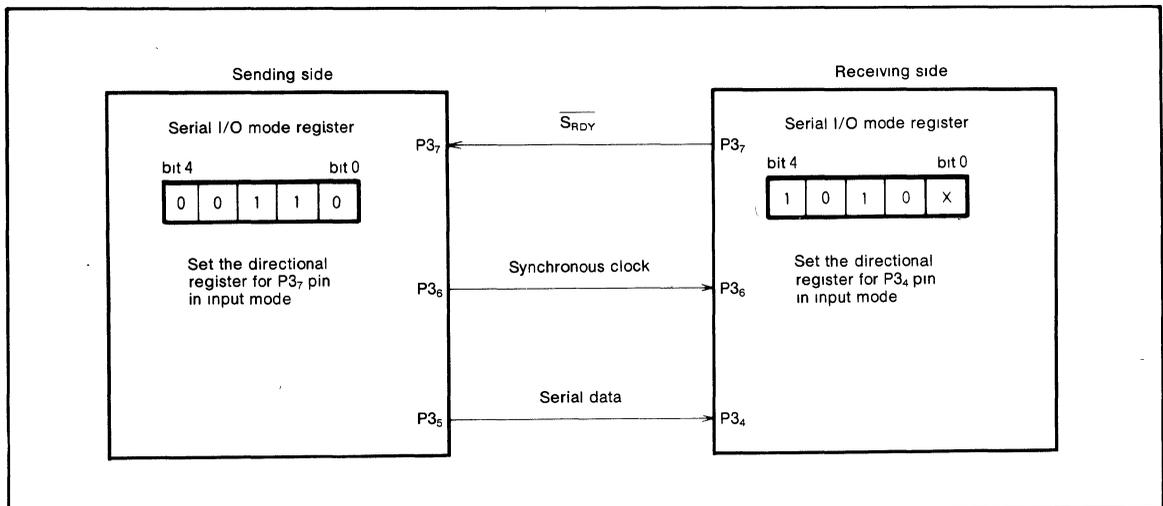


Fig.10 Example of serial I/O connection

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D-A CONVERTER

The R-2R method is used for D-A conversion. The block diagram is shown in Figure 13. An analog voltage is output that corresponds to the contents of the D-A conversion register (address 00F0₁₆). Ideally, the relation of the analog

output voltage V and the contents (n) of the D-A conversion register is $V = V_{REF} \times n/32 (n=0 \sim 31)$.

Reset operation clears the content n of the D-A conversion register to 0₁₆.

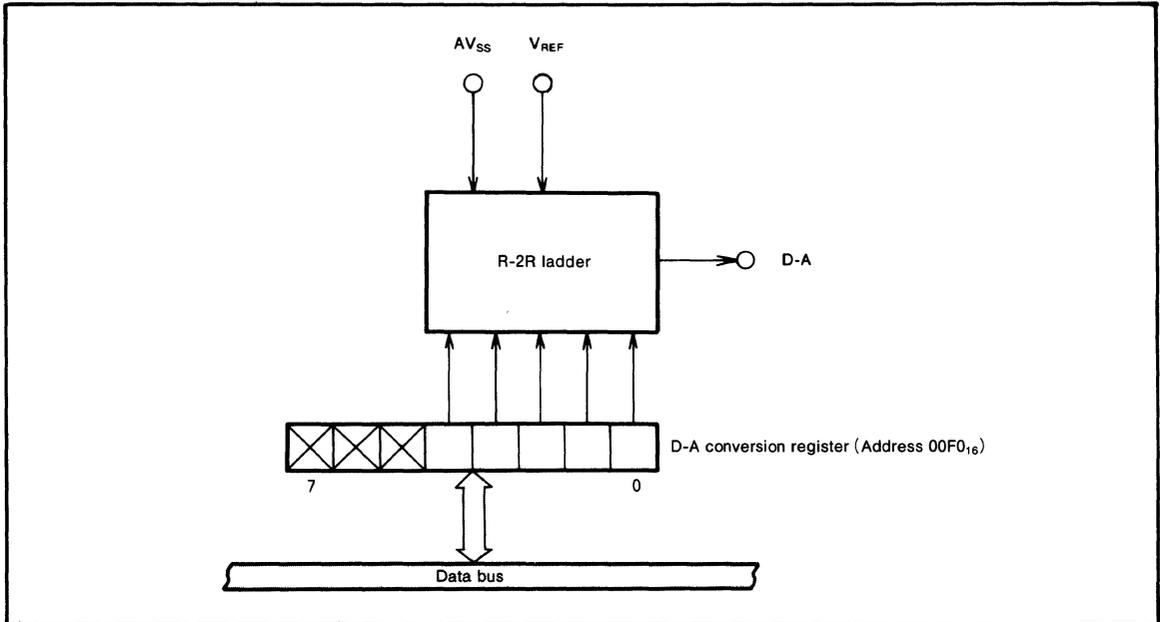


Fig.13 Block diagram of D-A converter

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PULSE WIDTH MODULATOR

The pulse width modulation register (address $00F1_{16}$) is configured of an 8-bit counter. The period of repetition is 4080 clock cycles. With the content of the pulse width modulation register m , the PWM pin becomes high-level for the

period of $4080 \times m/255$ ($m=0\sim 255$). Figure 14 shows that relationship. An N-channel open drain output is used for the PWM pin.

Reset sets the content m of the pulse width modulation register to 00_{16} .

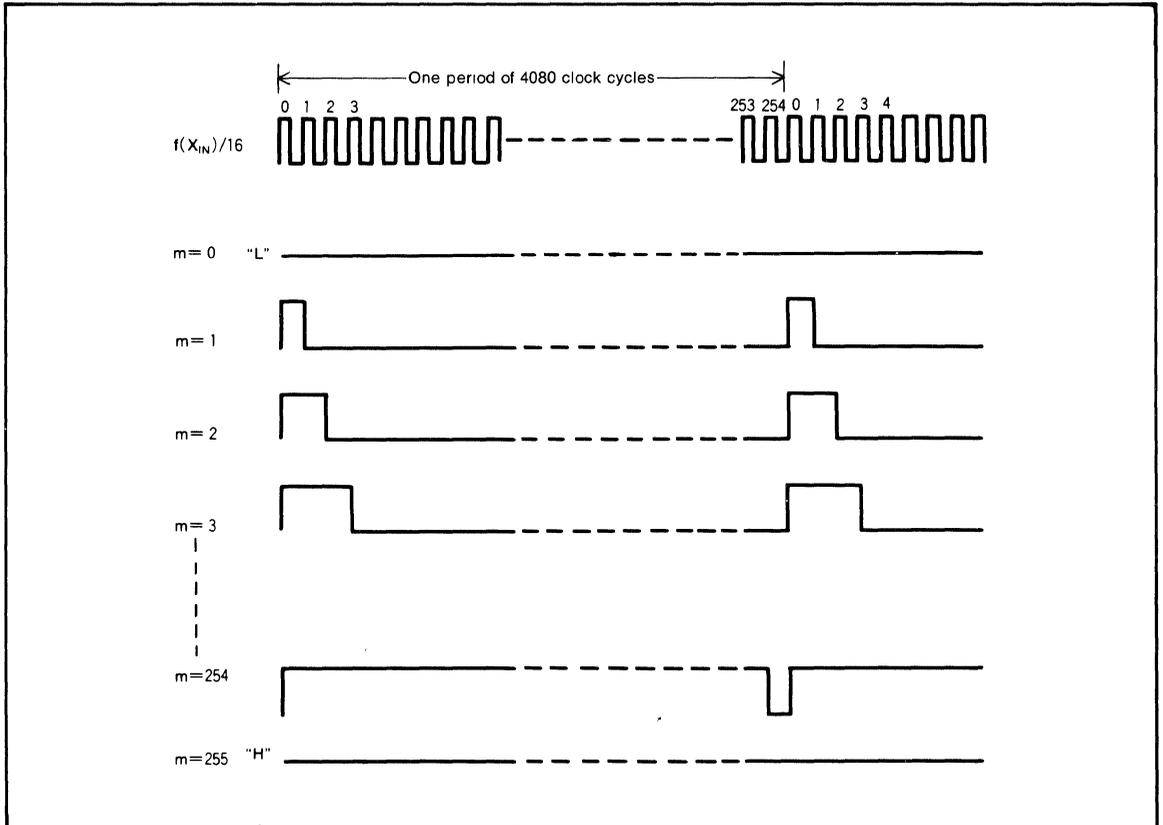


Fig.14 Relation between m and PWM output

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WATCHDOG TIMER

The watchdog timer provides the means to return to a reset condition when a program runs wild and the program will not run the normal loops.

The watchdog timer (address $00F4_{16}$) is a 15-bit counter. The watchdog timer counts 1/16th the output frequency of the oscillator. The watchdog timer is set to $7FFF_{16}$ when a reset is accomplished a write operation has been made to it. As well as any of the instructions that generate a write signal, such as STA, LDM, and CLB, can be used to write data to the watchdog timer. An output of the most significant bits of the watchdog timer is input to the reset circuit. When 262144 clock cycles have been counted, the most significant bit becomes "0" and reset is carried out. When reset is carried out, the watchdog timer is set to $7FFF_{16}$ and reset is released. The program then begins again from reset vector address. Normally, the program is written so that a writing operation is made to the watchdog timer prior to the most significant bit's becoming "0". Application of a +10V to the $\overline{\text{RESET}}$ pin will disable the watchdog timer function.

Since execution of the STP instruction causes both the clock and the watchdog timer to stop, an option is offered where the STP instruction can be disabled.

RESET CIRCUIT

The M37414M5-XXXFP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for more than $2\mu\text{s}$ while the power voltage is in the recommended operating condition and the crystal oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 16. An example of the reset circuit is shown in Figure 17.

When the power on reset is used, the $\overline{\text{RESET}}$ pin must be held "L" until the oscillation of $X_{\text{IN}}-X_{\text{OUT}}$ becomes stable.

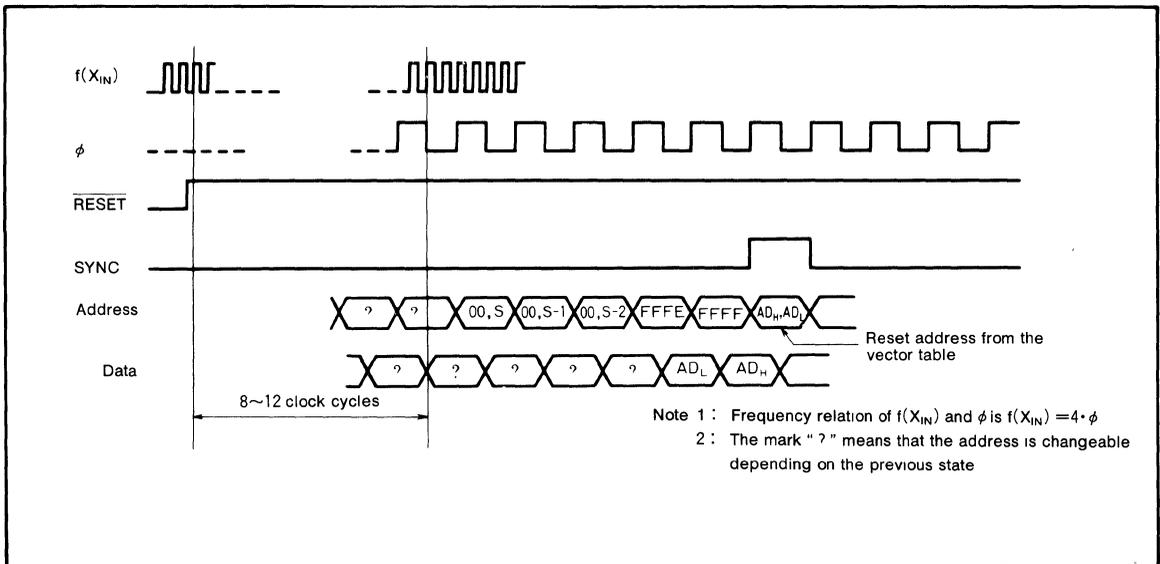


Fig.15 Timing diagram at reset

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

	Address	
(1) Port P0 directional register	(E 1 ₁₆)	0 0 ₁₆
(2) Port P1 directional register	(E 3 ₁₆)	0 0 ₁₆
(3) Port P2 directional register	(E 5 ₁₆)	0 0 ₁₆
(4) Port P3 directional register	(E 9 ₁₆)	0 0 ₁₆
(5) Port P4 directional register	(E B ₁₆)	0 0 ₁₆
(6) Port P6	(E E ₁₆)	1 1 1 1 1 1
(7) Port P7 directional register	(E 6 ₁₆)	0 0 0 0 0 0
(8) Special function selection register	(E F ₁₆)	0 0 0 0
(9) D-A conversion register	(F 0 ₁₆)	0 0 0 0 0 0
(10) Pulse width modulation register	(F 1 ₁₆)	0 0 ₁₆
(11) Watchdog timer	(F 4 ₁₆)	7 F F F ₁₆
(12) Serial I/O mode register	(F 5 ₁₆)	0 0 0 0 0 0
(13) Prescaler X	(F C ₁₆)	F F ₁₆
(14) Timer X	(F D ₁₆)	0 1 ₁₆
(15) Interrupt control register	(F E ₁₆)	0 0 ₁₆
(16) Timer control register	(F F ₁₆)	0 0 ₁₆
(17) Interrupt disable flag on processor status register	(P S)	1
(18) Program counter	(P C _H)	Contents of address FFFF ₁₆
	(P C _L)	Contents of address FFFE ₁₆

Fig.16 Internal state of microcomputer at reset

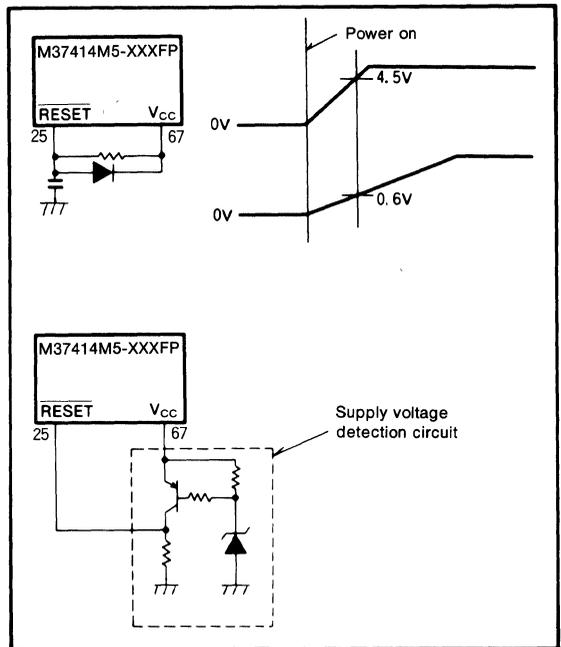


Fig.17 Example of reset circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address 00E0₁₆. Port P0 has a directional register (address 00E1₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address 00FF₁₆), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0, but it has N-channel open drain output. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O, INT₂ and I/O pins for timer X. For more details, see the processor mode information.

(5) Port P4

Port P4 has the same function as port P0 in the single-chip mode, but it has N-channel open drain output. P4₇ through P4₀ can also be used as analog input pins AN₇ through AN₀.

(6) Port P5

Port P5 is an input port. P5₄ through P5₇ can also be used as edge sense inputs. In such a case, reading is begun from 00ED₁₆. 00ED₁₆ is provided with a latch which is set to "1" when the input changes from high-level to low-level.

And for P5₇, polarity of input edge can be selected by polarity of edge sense input selection bit (bit 7 of address 00EF₁₆).

When this bit is set to "0", its latch is set to "1" at the input level goes to "L" from "H". When this bit is set to "1", its latch is set to "1" at the input level goes to "H" from "L". At the reset state, this bit is set to "0".

When content of polarity of edge sense input selection bit was set by program, the latch (bit 7 of address 00ED₁₆) must be reset once.

The input pulse width must be at least 7 clock cycles wide. The latch is reset by using such instructions as LDM and CLB to write a "0" to the latch. When 00ED₁₆ is read, the lower order 4 bits are always zero

When port P5 is used as level sense input, read the contents of the address 00EC₁₆

(7) Port P6

Port P6 is a 5-bit output port. It has N-channel open drain output. P6₀ and P6₁ can be used as external trigger I/O pins, when external trigger mode selection bit (bit 2 of address 00EF₁₆) is set to "1". In this case, P6₀ and P6₁ are trigger clock input pin and trigger output pin, respectively. Using external trigger mode, P6₀'s latch must be set to "1" in order to off the output transistor. In external trigger mode, the content of P6₁'s latch is output to pin when the rising or falling edge is input to P6₀ pin.

When external trigger mode selection bit is set to "0", P6₀ and P6₁ are normal output ports. At the reset state, this bit is set to "0".

(8) Port P7

Port P7 is a 6-bit I/O port. In the single-chip mode, port P7 has the same function as P0, but P7₀, P7₁ have N-channel open drain output.

See Figure 17 for more details.

(9) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ . The timing output ϕ is fixed "L" state when the timing output control bit (bit 1 of address 00EF₁₆) is set to "1". But in this case, except the timing output is active. The timing output ϕ is output again when the timing output control bit is set to "0". At reset state this bit is set to "0".

(10) INT₁ pin

The INT₁ pin is an interrupt input pin. The $\overline{\text{INT}}_1$ interrupt request bit (bit 7 at address 00FE₁₆) is set to "1" when the input level of this pin changes from "H" to "L".

(11) $\overline{\text{INT}}_2$ pin (P3₂/ $\overline{\text{INT}}_2$ pin)

The $\overline{\text{INT}}_2$ pin is an interrupt input pin used with P3₂. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address 00FE₁₆) is set to "1".

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(12) CNTR pin (P3₃/CNTR pin)

The P3₃/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external

pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

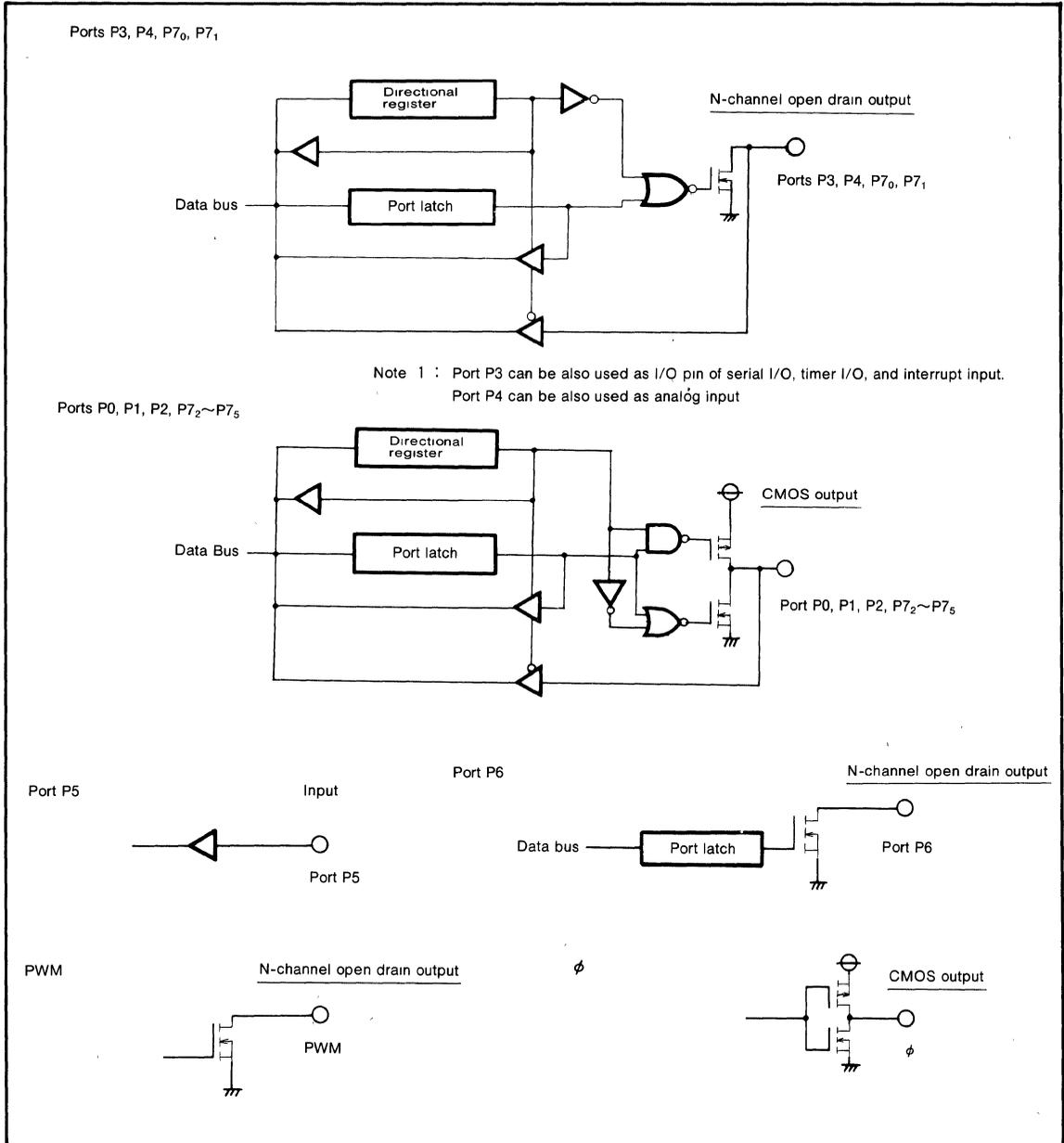


Fig.18 Block diagram of ports P0~P7 (single-chip mode), and output format of ϕ .

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PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address 00FF₁₆), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0~P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 20 shows the functions of ports P0~P3.

The memory map for the single-chip mode is illustrated in Figure 2 and for other modes, in Figure 19.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

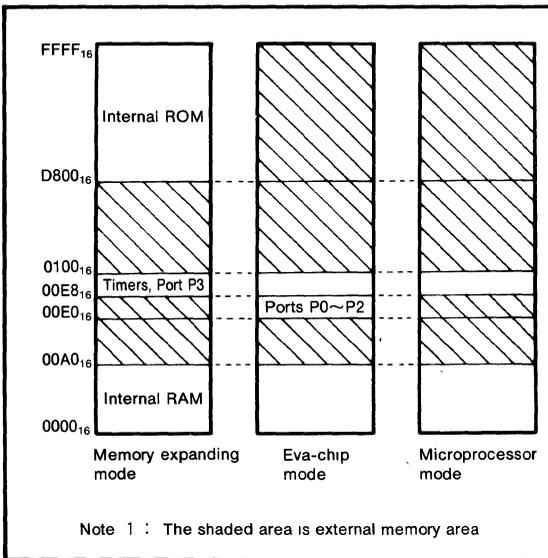


Fig.19 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0~P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. P2 becomes the data bus (D₇~D₀) and loses its normal I/O functions. Pins P3₁ and P3₀ output the SYNC and R/W control signals, respectively.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. With the exceptions that the internal ROM is disabled and that external memory must be attached in this mode, this mode is the same as the memory expanding mode.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is required.

The lower 8 bits of address data for port P0 is output when φ goes to "H" state. When φ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when φ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original I/O functions while φ is at the "H" state, and works as a data bus of D₇~D₀ (including instruction code) while at the "L" state. Pins P3₁ and P3₀ output the SYNC and R/W control signals, respectively while φ is in the "H" state. When in the "L" state, P3₁ and P3₀ retain their original I/O function.

The R/W output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

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Port	CM ₁	0	1	0	1
	CM ₀	0	1	1	0
Mode	Single-chip mode		Eva-chip mode	Memory expanding mode	Microprocessor mode
Port P0				Same as left	
Port P1				Same as left	
Port P2				Same as left	
Port P3				Same as left	

Fig.20 Processor mode and functions of ports P0~P3

Table 2. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode 	The single-chip mode is set by the reset All modes can be selected by changing the processor mode bit with the program
V _{CC}	<ul style="list-style-type: none"> • Eva-chip mode • Microprocessor mode 	The microprocessor mode is set by the reset Eva-chip mode can be also selected by changing the processor mode bit with the program
10V	<ul style="list-style-type: none"> • Eva-chip mode 	Eva-chip mode only

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CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 23.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16} , respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 21.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 22. X_{IN} is the input, and X_{OUT} is open.

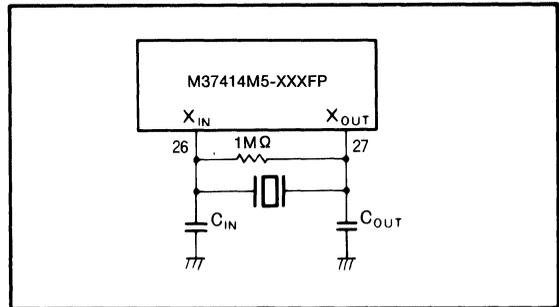


Fig.21 External ceramic resonator circuit

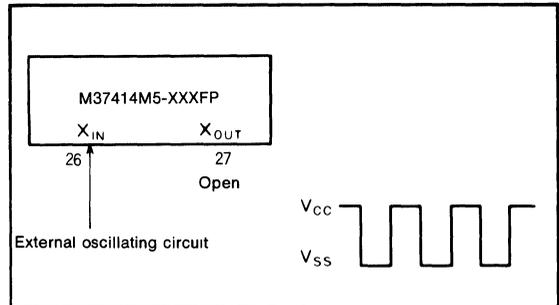


Fig.22 External clock input circuit

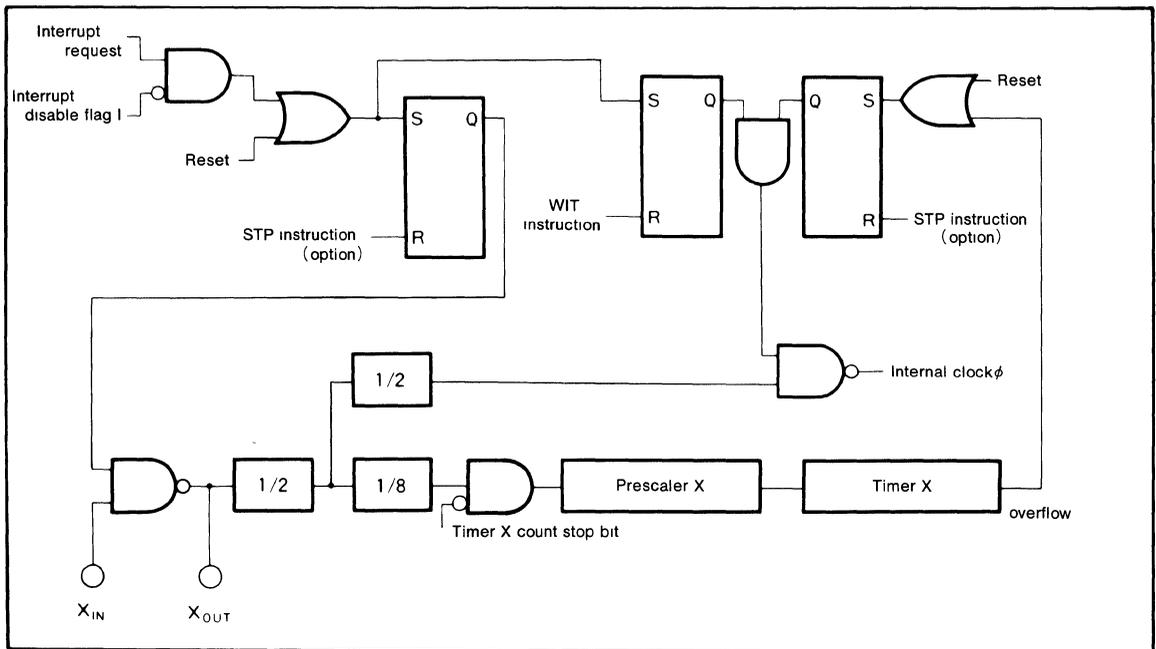


Fig.23 Block diagram of the clock generating circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PROGRAMMING NOTES

- (1) The frequency ratio of the timer and the prescaler is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
- (4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion. And during A-D conversion, don't use STP or WIT instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3sets

Write the following option on the mask ROM confirmation form

- STP instruction option

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	-0.3~7	V
V_I	Input voltage X_{IN}		-0.3~7	V
V_I	Input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P4_0\sim P4_7, P7_2\sim P7_5$		-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage $P3_0\sim P3_7, P5_0\sim P5_7, P6_0, P7_0, P7_1, \overline{INT}_1$		-0.3~13	V
V_I	Input voltage $CNV_{SS}, \overline{RESET}$		-0.3~13	V
V_O	Output voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P4_0\sim P4_7, P7_2\sim P7_5, X_{OUT}, \phi, D-A$		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage $P3_0\sim P3_7, P6_0\sim P6_4, P7_0, P7_1, PWM$		-0.3~13	V
P_d	Power dissipation	$T_a=25^\circ C$	300	mW
T_{opr}	Operating temperature		-10~70	$^\circ C$
T_{stg}	Storage temperature		-40~125	$^\circ C$

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V\pm 10\%$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7,$ $\overline{INT}_1, \overline{RESET}, X_{IN}, CNV_{SS}, P6_0,$ $P7_0\sim P7_5$	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7,$ $\overline{INT}_1, CNV_{SS}, P6_0, P7_0\sim P7_5$	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage \overline{RESET}	0		$0.12V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}	0		$0.16V_{CC}$	V
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7, P1_0\sim P1_7,$ $P2_0\sim P2_7, P3_0\sim P3_7,$ $P4_0\sim P4_7, P7_0\sim P7_5$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0\sim P6_5$ (Note 2)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM, $P6_4$ (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7, P1_0\sim P1_7,$ $P2_0\sim P2_7, P3_0\sim P3_7,$ $P4_0\sim P4_7, P7_0\sim P7_5$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0\sim P6_5$ (Note 1)			7	mA
$I_{OL(avg)}$	"L" average output current PWM, $P6_4$ (Note 1)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0\sim P0_7, P1_0\sim P1_7,$ $P2_0\sim P2_7, P7_2\sim P7_5$ (Note 2)			-10	mA
$I_{OH(avg)}$	"H" average output current $P0_0\sim P0_7, P1_0\sim P1_7,$ $P2_0\sim P2_7, P7_2\sim P7_5$ (Note 1)			-5	mA
$f(X_{IN})$	Internal clock oscillating frequency			4	MHz

- Note 1 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
 2 : Total of "L" output current I_{OL} of ports P0, P1, P2, P3, P4, P6, P7 and PWM is 80mA max
 Total of "H" output current I_{OH} of port P0, P1, P2, $P7_2\sim P7_5$ is 50mA max
 3 : "H" input voltage of ports P3, P5, P6, P7, P7₁ and \overline{INT}_1 is available up to +12V

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ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P7 ₂ ~P7 ₅	$I_{OH}=-10mA$	3			V
V_{OH}	"H" output voltage ϕ	$I_{OH}=-2.5mA$	3			V
V_{OL}	"L" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P6 ₀ ~P6 ₃ , P7 ₀ ~P7 ₅	$I_{OL}=10mA$			2	V
V_{OL}	"L" output voltage ϕ , PWM, P6 ₄	$I_{OL}=5mA$			2	V
$V_{T+}-V_{T-}$	Hysteresis INT ₁		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis P3 ₆	When used as CLK input	0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis P3 ₂	When used as INT ₂ input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis P3 ₃	When used as CNTR input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis P6 ₀	When used as T input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis RESET			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X _{IN}		0.1		0.5	V
I_{IL}	"L" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ , P7 ₀ ~P7 ₅ , PWM	$V_i=0V$			-5	μA
I_{IL}	"L" input current INT ₁ , RESET, X _{IN}	$V_i=0V$			-5	μA
I_{IH}	"H" input current P3 ₀ ~P3 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ , P7 ₀ , P7 ₁ , PWM	$V_i=12V$			12	μA
I_{IH}	"H" input current INT ₁ , RESET, X _{IN} , P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P7 ₂ ~P7 ₅	$V_i=5V$			5	μA
V_{RAM}	RAM retention voltage	At clock stop	2			V
I_{CC}	Supply current	ϕ , X _{OUT} , and D-A pins opened, other pins at V_{SS} , and A-D converter in the finished condition	$f(X_{IN})=4MHz$ Square wave	3	6	mA
			At clock stop $T_a=25^\circ C$		1	
			At clock stop $T_a=75^\circ C$		10	μA

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistance value	$V_{REF}=V_{CC}$	2		10	k Ω
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			5	Bits
—	Error in full scale range	$V_{REF}=V_{CC}$			± 1	%
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
R_O	Output resistance	$V_{REF}=V_{CC}$			3	k Ω
V_{REF}	Reference voltage		4		V_{CC}	V

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TIMING REQUIREMENTS

Single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{su}(P0D-\phi)$	Port P0 input setup time	270			ns
$t_{su}(P1D-\phi)$	Port P1 input setup time	270			ns
$t_{su}(P2D-\phi)$	Port P2 input setup time	270			ns
$t_{su}(P3D-\phi)$	Port P3 input setup time	270			ns
$t_{su}(P4D-\phi)$	Port P4 input setup time	270			ns
$t_{su}(P5D-\phi)$	Port P5 input setup time	270			ns
$t_{su}(P7D-\phi)$	Port P7 input setup time	270			ns
$t_h(\phi-P0D)$	Port P0 input hold time	20			ns
$t_h(\phi-P1D)$	Port P1 input hold time	20			ns
$t_h(\phi-P2D)$	Port P2 input hold time	20			ns
$t_h(\phi-P3D)$	Port P3 input hold time	20			ns
$t_h(\phi-P4D)$	Port P4 input hold time	20			ns
$t_h(\phi-P5D)$	Port P5 input hold time	20			ns
$t_h(\phi-P7D)$	Port P7 input hold time	20			ns
t_c	External clock input cycle time	250			ns
t_w	External clock input pulse width	75			ns
t_r	External clock rising edge time			25	ns
t_f	External clock falling edge time			25	ns

Eva-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{su}(P0D-\phi)$	Port P0 input setup time	270			ns
$t_{su}(P1D-\phi)$	Port P1 input setup time	270			ns
$t_{su}(P2D-\phi)$	Port P2 input setup time	270			ns
$t_h(\phi-P0D)$	Port P0 input hold time	20			ns
$t_h(\phi-P1D)$	Port P1 input hold time	20			ns
$t_h(\phi-P2D)$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{su}(P2D-\phi)$	Port P2 input setup time	270			ns
$t_h(\phi-P2D)$	Port P2 input hold time	30			ns

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

SWITCHING CHARACTERISTICS

Single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_d(\phi-P0Q)$	Port P0 data output delay time	Fig 25			230	ns
$t_d(\phi-P1Q)$	Port P1 data output delay time				230	ns
$t_d(\phi-P2Q)$	Port P2 data output delay time				230	ns
$t_d(\phi-P3Q)$	Port P3 data output delay time	Fig 24			230	ns
$t_d(\phi-P4Q)$	Port P4 data output delay time				230	ns
$t_d(\phi-P6Q)$	Port P6 data output delay time				230	ns
$t_d(\phi-P7Q)$	Port P7 ₀ , P7 ₁ data output delay time	Fig 25			230	ns
	Port P7 ₂ ~P7 ₅ data output delay time				230	ns

Eva-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
$t_d(\phi-P0A)$	Port P0 address output delay time	Fig 25			250	ns	
$t_d(\phi-P0AF)$	Port P0 address output delay time				250	ns	
$t_d(\phi-P0Q)$	Port P0 data output delay time				200	ns	
$t_d(\phi-P0QF)$	Port P0 data output delay time				200	ns	
$t_d(\phi-P1A)$	Port P1 address output delay time				250	ns	
$t_d(\phi-P1AF)$	Port P1 address output delay time				250	ns	
$t_d(\phi-P1Q)$	Port P1 data output delay time				200	ns	
$t_d(\phi-P1QF)$	Port P1 data output delay time				200	ns	
$t_d(\phi-P2Q)$	Port P2 data output delay time				300	ns	
$t_d(\phi-P2QF)$	Port P2 data output delay time				300	ns	
$t_d(\phi-R/W)$	R/W signal output delay time		Fig 24			250	ns
$t_d(\phi-R/WF)$	R/W signal output delay time					250	ns
$t_d(\phi-P3_0Q)$	Port P3 ₀ data output delay time				200	ns	
$t_d(\phi-P3_0QF)$	Port P3 ₀ data output delay time				200	ns	
$t_d(\phi-SYNC)$	SYNC signal output delay time				250	ns	
$t_d(\phi-SYNCF)$	SYNC signal output delay time				250	ns	
$t_d(\phi-P3_1Q)$	Port P3 ₁ data output delay time				200	ns	
$t_d(\phi-P3_1QF)$	Port P3 ₁ data output delay time				200	ns	

Memory expanding mode and microprocessor mode

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_d(\phi-P0A)$	Port P0 address output delay time	Fig 25			250	ns
$t_d(\phi-P1A)$	Port P1 address output delay time				250	ns
$t_d(\phi-P2Q)$	Port P2 data output delay time				300	ns
$t_d(\phi-P2QF)$	Port P2 data output delay time	Fig 24			300	ns
$t_d(\phi-R/W)$	R/W signal output delay time				250	ns
$t_d(\phi-SYNC)$	SYNC signal output delay time				250	ns

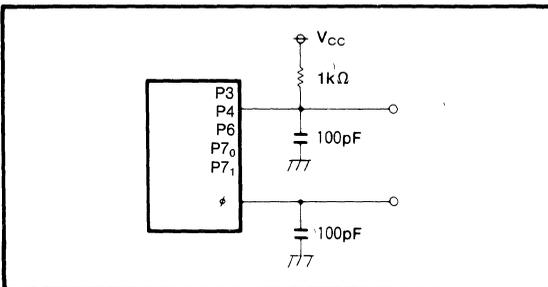


Fig.24 Ports P3, P4, P6, P7₀, P7₁ test circuit

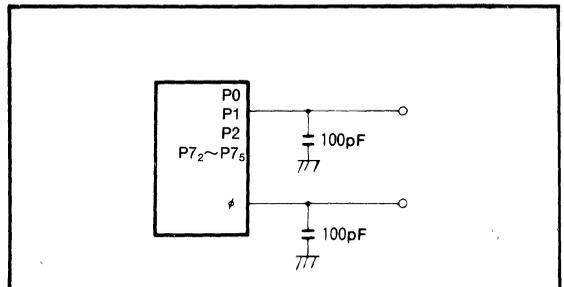
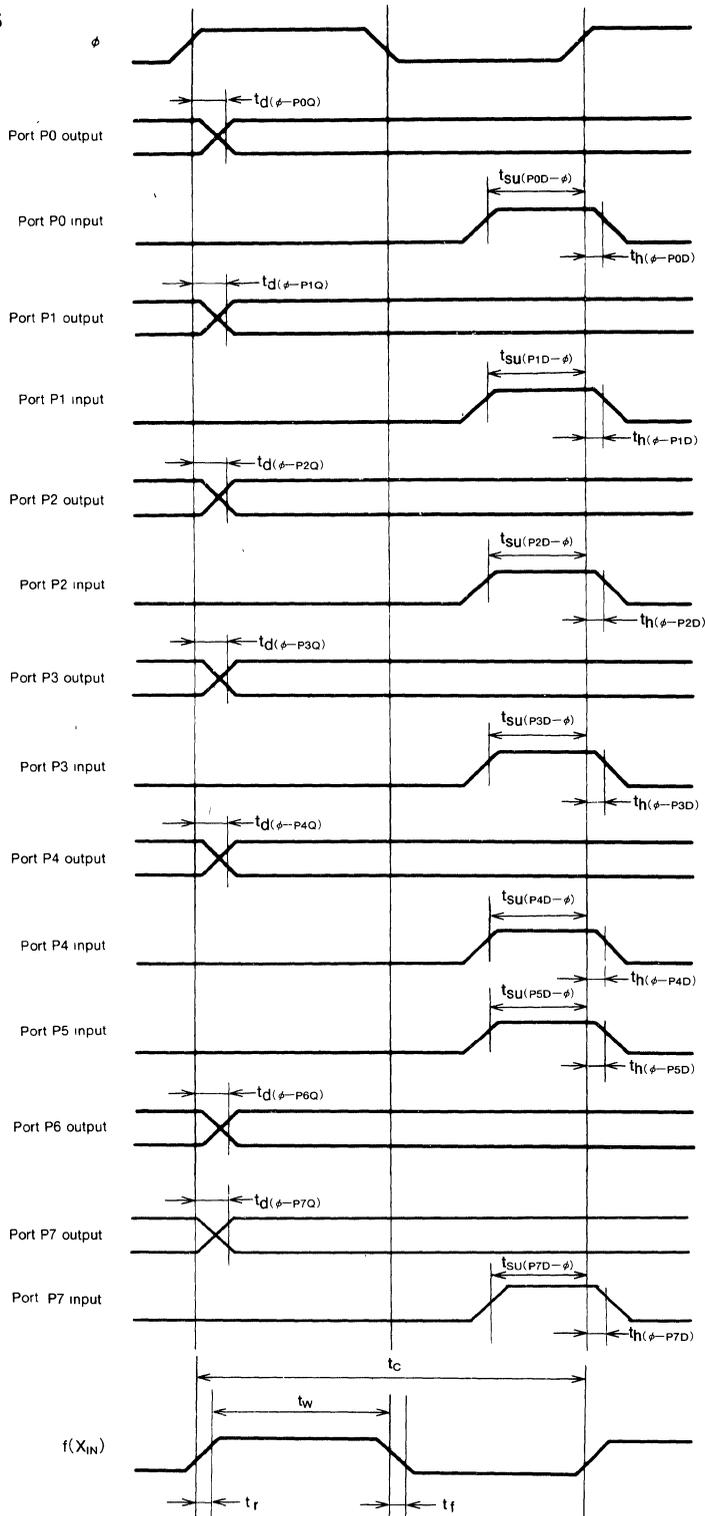


Fig.25 Port P0, P1, P2, P7₂~P7₅ test circuit

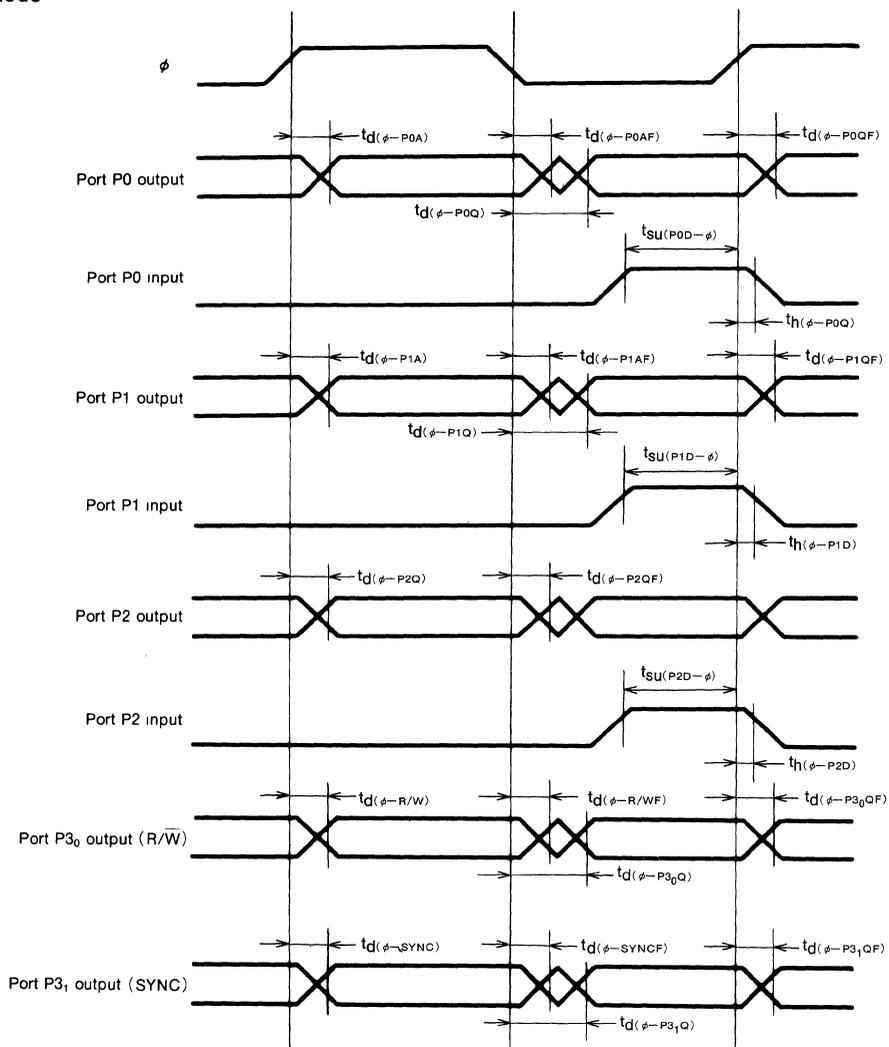
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMING DIAGRAMS
In single-chip mode



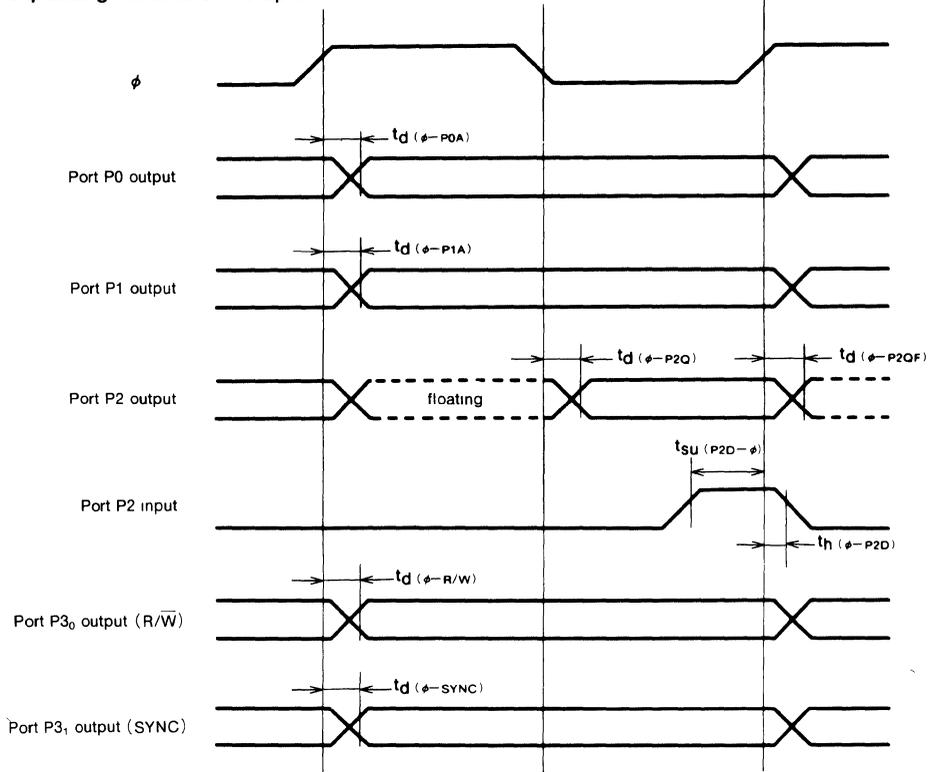
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

In eva-chip mode



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

In memory expanding mode and microprocessor mode



MITSUBISHI MICROCOMPUTERS M37415M4-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37415M4-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin plastic molded QFP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

This microcomputer is also suitable for applications which require controlling LCDs and generating DTMF.

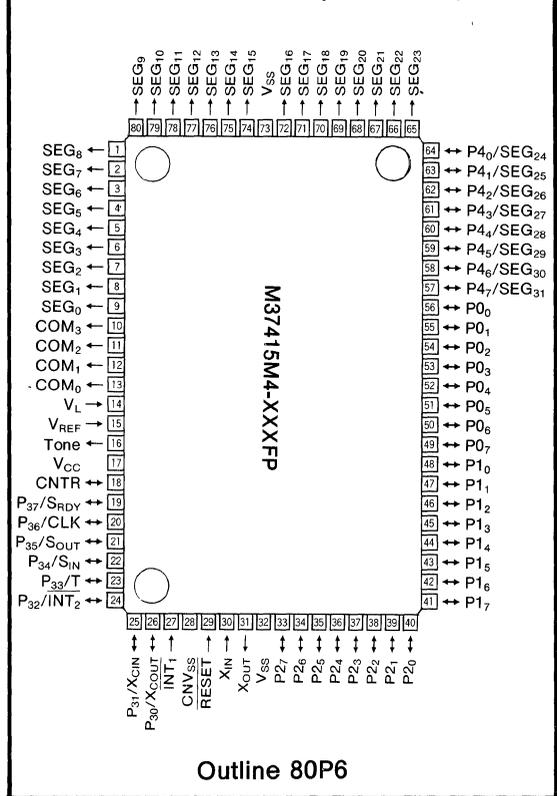
FEATURES

- Number of basic instructions..... 69
- Memory size
 - ROM..... 8192 bytes
 - RAM..... 512 bytes
 - RAM for display LCD..... 16 bytes
- Instruction execution time
 - ... 2.5 μ s (minimum instructions at 3.2MHz frequency)
 - ... 5 μ s (minimum instructions at 1.6MHz frequency)
 - ... 10 μ s (minimum instructions at 800kHz frequency)
 - ... 20 μ s (minimum instructions at 400kHz frequency)
- Single power supply
 - $f(X_{IN})=400\text{kHz}$, or 800kHz $2.5 \leq V_{CC} \leq 5.5\text{V}$
 - $f(X_{IN})=1.6\text{MHz}$, or 3.2MHz $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
- Power dissipation
 - normal operation mode (at 3.2MHz frequency)
 - 20mW (DTMF output $V_{CC}=5.0\text{V}$ typ.)
 - 15mW (DTMF off $V_{CC}=5.0\text{V}$ typ.)
 - low-speed operation mode
 - (at 32kHz frequency for clock function)
 - 225 μ W ($V_{CC}=5.0\text{V}$ typ.)
 - stop mode (at 25°C)..... 5 μ W ($V_{CC}=5.0\text{V}$ max.)
- RAM retention voltage (stop mode)..... $2\text{V} \leq V_{RAM} \leq 5.5\text{V}$
- Subroutine nesting..... 64 levels (max.)
- Interrupt..... 8 types, 5 vectors
- 8-bit timer..... 3 (2 when used as serial I/O)
- 16-bit timer..... 1 (Two 8-bit timers makes one set)
- Programmable I/O ports
 - (Ports P0, P1, P2, P3)..... 32
- Input port (Port P4)..... 8
- Serial I/O (8-bit)..... 1
- DTMF (Dual-Tone Multi-Frequency) generator... Built-in
- LCD controller/driver
 - (1/2, 1/3, bias, 1/2, 1/3, 1/4 duty)
 - segment output..... 32
 - common output..... 4
 - resistor for LCD power supply..... Built-in
- Two clock generator circuits
 - (One is for main clock, the other is for clock function.)

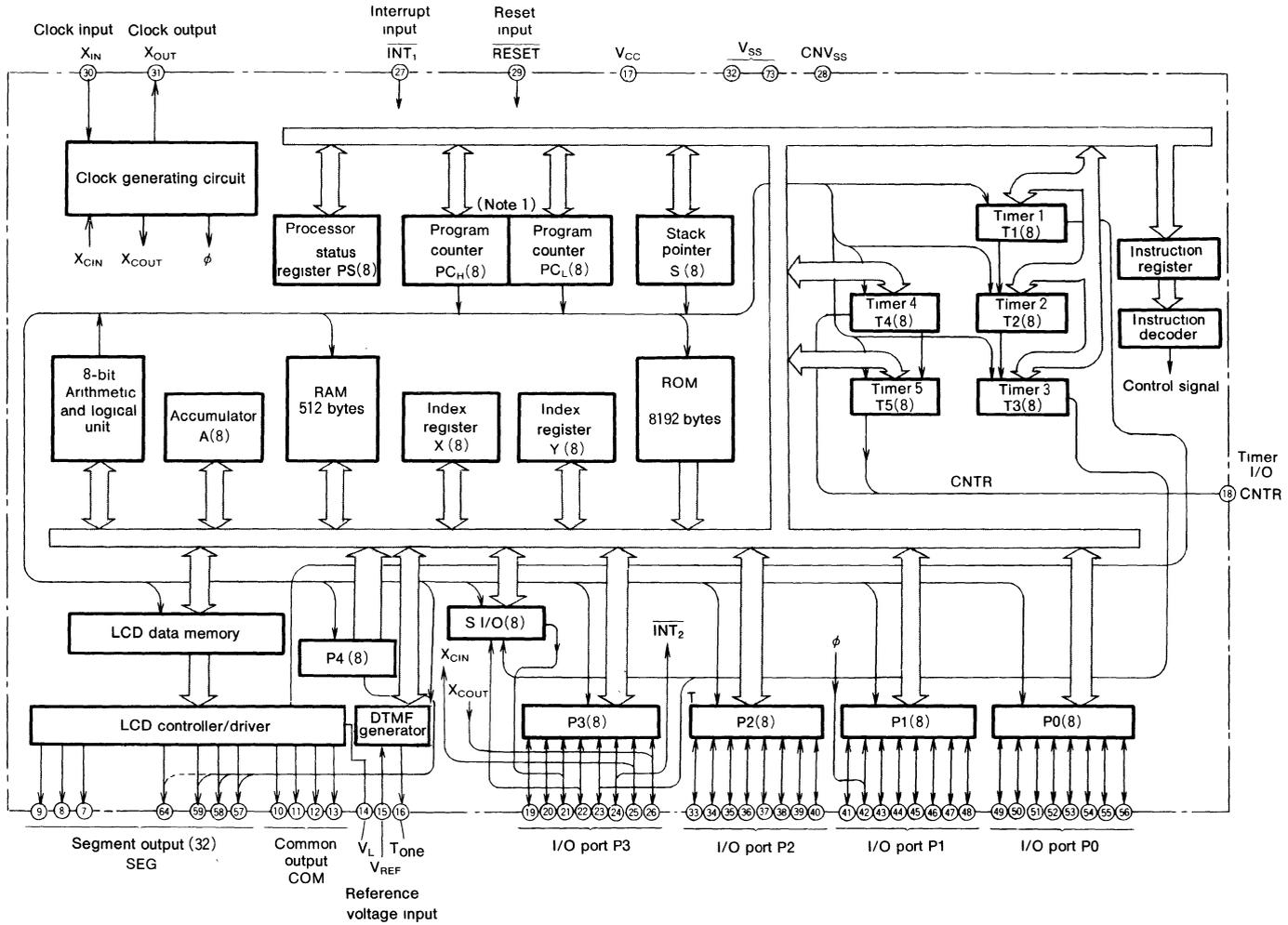
APPLICATION

Home telephone, Multi function telephone

PIN CONFIGURATION (TOP VIEW)



M37415M4-XXXFP BLOCK DIAGRAM



Note 1 : Program counter PC_H is only 6 bits long



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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

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M37415M4-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37415M4-XXXFP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		2.5 μ s (minimum instructions, at 3.2MHz frequency) 5 μ s (minimum instructions, at 1.6MHz frequency) 10 μ s (minimum instructions, at 800kHz frequency) 20 μ s (minimum instructions, at 400kHz frequency)	
Clock frequency		3.2MHz, 1.6MHz, 800kHz, 400kHz	
Memory size	ROM	8192 bytes	
	RAM	512 bytes	
	RAM for display LCD	16 bytes	
Input/Output port	P0, P1, P2, P3	I/O	8-bit \times 4
	P4	Input	8-bit \times 1 (Port P4 are in common with SEG)
	SEG	LCD output	32-bit \times 1
	COM	LCD output	4-bit \times 1
Serial I/O		8-bit \times 1	
Timers		8-bit timer \times 3 (\times 2, when serial I/O is used) 16-bit timer \times 1 (combination of two 8-bit timers)	
LCD controller/driver	Bias	1/2, 1/3, bias selectable	
	Duty ratio	1/2, 1/3, 1/4 duty selectable	
	Common output	4	
	Segment output	32 (SEG ₂₄ ~SEG ₃₁ are in common with port P4)	
Subroutine nesting		64 (max)	
Interrupt		Two external interrupts, Three timer internal interrupts (or two timer, one serial I/O)	
Clock generating circuit		Two built-in circuits (ceramic or quartz crystal oscillator)	
Supply voltage		2.5~5.5V (at 400kHz or 800kHz frequency) 4.5~5.5V (at 1.6MHz or 3.2MHz frequency) RAM retention voltage at clock stop is 2~5.5V	
Power dissipation	DTMF output	At high-speed operation V _{CC} =5V	20mW (at clock frequency f(X _{IN})=3.2MHz)
		At high-speed operation V _{CC} =5V	15mW (at clock frequency f(X _{IN})=3.2MHz)
	DTMF off	At low-speed operation V _{CC} =5V	225 μ W (at clock frequency f(X _{CIN})=32kHz)
		At stop mode	1 μ A (max 25 $^{\circ}$ C)
Input/Output characteristics	Input/Output voltage		5V
	Output current		I _{OH} =-2mA (V _{OH} =3V)
			I _{OL} =10mA (V _{OL} =2V)
Pull-up current : Min -30 μ A, Max -140 μ A, Typ -70 μ A (V _{CC} =5V input voltage 0V)			
Operating temperature range		-10~70 $^{\circ}$ C	
Device structure		CMOS silicon gate	
Package		80-pin plastic molded QFP	

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage input		Power supply inputs 5V±10% to V _{CC} and 0V to V _{SS}
CNV _{SS}	CNV _{SS} input		Connect to V _{SS}
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2 μ s (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}	Clock output	Output	
$\overline{\text{INT}}_1$	Interrupt input	Input	This is the highest order interrupt input pin It can be measured input voltage level
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as $\overline{\text{S}}_{\text{RDY}}$, CLK, S _{OUT} , and S _{IN} pins, respectively Also P3 ₃ , P3 ₂ , P3 ₁ , and P3 ₀ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{\text{INT}}_2$ pin, X _{CIN} and X _{COU} pins, respectively
P4 ₀ ~P4 ₇	Input port P4	Input	Port P4 is an 8-bit input port and can be used as segment output pins
V _L	Voltage input for LCD	Input	This is a voltage input pin for LCD Supply voltage is 0V≤V _L ≤V _{CC} 0V~V _L is supplied to LCD
COM ₀ ~ COM ₃	Common output	Output	These are the LCD common output pins At 1/2 duty, COM ₂ and COM ₃ pins are not use At 1/3 duty, COM ₃ pin is not used
SEG ₀ ~ SEG ₂₃	Segment output	Output	These are LCD segment output pins
CNTR	Counter I/O	I/O	This is an output pin for timer 4 and 5 It can be measured input voltage level
V _{REF}	D-A convert power supply for DTMF		Reference voltage input for A-D converter of DTMF
Tone	DTMF output	Output	This is DTMF output pin

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37415 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

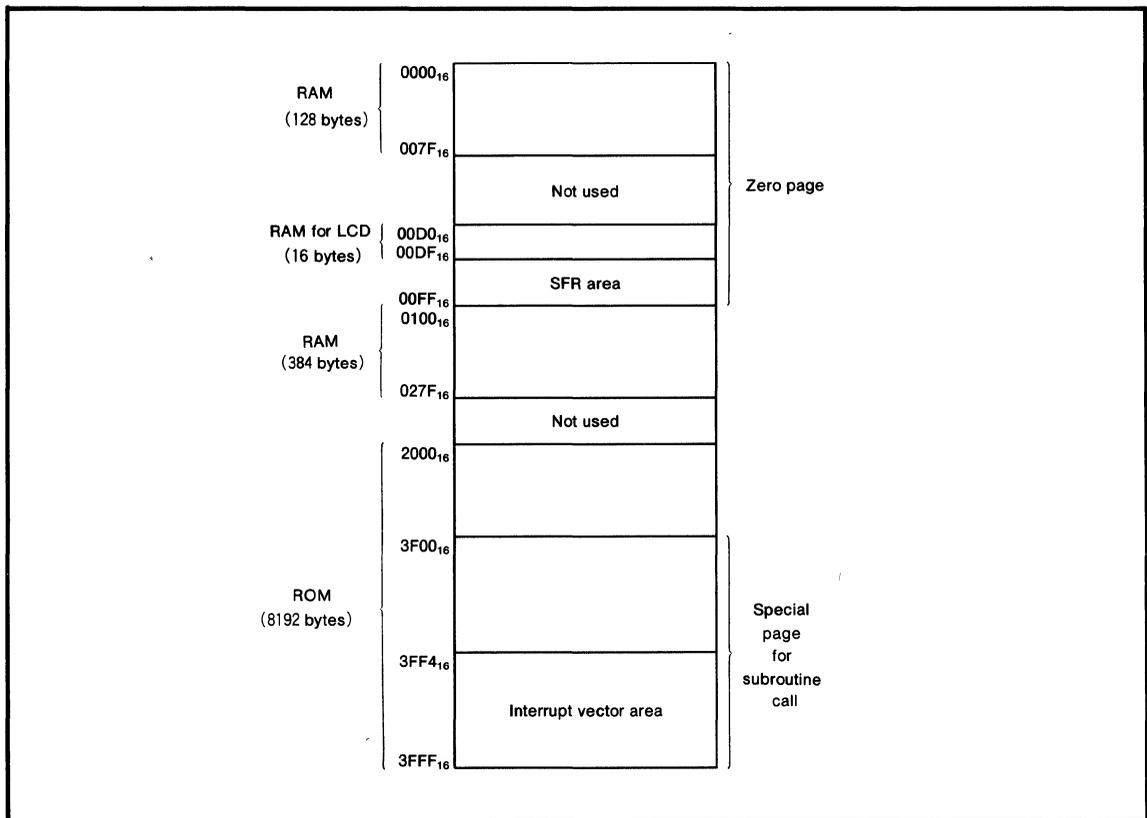


Fig.1 Memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

00E0 ₁₆	Port P0	00F0 ₁₆	
00E1 ₁₆	Port P0 directional register	00F1 ₁₆	
00E2 ₁₆	Port P1	00F2 ₁₆	
00E3 ₁₆	Port P1 directional register	00F3 ₁₆	
00E4 ₁₆	Port P2	00F4 ₁₆	DTMF register
00E5 ₁₆	Port P2 directional register	00F5 ₁₆	LCD mode register
00E6 ₁₆		00F6 ₁₆	Serial I/O mode register
00E7 ₁₆		00F7 ₁₆	Serial I/O register
00E8 ₁₆	Port P3	00F8 ₁₆	Timer 4, 5 mode register
00E9 ₁₆	Port P3 directional register	00F9 ₁₆	Timer 1
00EA ₁₆	Port P4	00FA ₁₆	Timer 2
00EB ₁₆		00FB ₁₆	Timer 3
00EC ₁₆		00FC ₁₆	Timer 4
00ED ₁₆		00FD ₁₆	Timer 5
00EE ₁₆		00FE ₁₆	Interrupt control register
00EF ₁₆		00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

INTERRUPT

The M37415M4-XXXXP can be interrupted from eight sources; \overline{INT}_1 , Timer 1, Timer 2, Timer 3 or Serial I/O, \overline{INT}_2 or key on wake up, and BRK instruction.

The value of bit 2 of the serial I/O register (address 00F6₁₆) determines whether the interrupt is from timer 3 or from serial I/O. When the bit 2 is "1" the interrupt is from serial I/O, and when bit 2 is "0" the interrupt is from timer 3. Also, when bit 2 is "1", parts of port 3 are used for serial I/O. Bit 7 of the serial I/O register determines if an interrupt is from \overline{INT}_2 or from "key on wake up". When bit 7 is "0", the interrupt is from \overline{INT}_2 . When bit 7 is "1" the interrupt is from "key on wake up". "Key on wake up" can only be used at power down by the STP or WIT instruction. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as interrupt.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
RESET	1	3FFF ₁₆ , 3FFE ₁₆
\overline{INT}_1	2	3FFD ₁₆ , 3FFC ₁₆
Timer 1	3	3FFB ₁₆ , 3FFA ₁₆
Timer 2	4	3FF9 ₁₆ , 3FF8 ₁₆
Timer 3 or serial I/O	5	3FF7 ₁₆ , 3FF6 ₁₆
\overline{INT}_2 or key on wake up(BRK)	6	3FF5 ₁₆ , 3FF4 ₁₆

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, as discussed in the stack pointer section, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts except key on wake up function can further be controlled individually via the interrupt control register shown in Figure 3 An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

- (1) When the \overline{INT}_1 or \overline{INT}_2 pins goes from "H" to "L"
- (2) When the levels any pin of P2 goes "L" (at power down mode)
- (3) When the contents of timer 1, timer 2, timer 3 or the counter of serial I/O goes to "0"

These request bits can be clear by a program but can not be set. The interrupt enable bit can be set and clear by a program.

Since the BRK instruction interrupt and the \overline{INT}_2 interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if \overline{INT}_2 generated the interrupt.

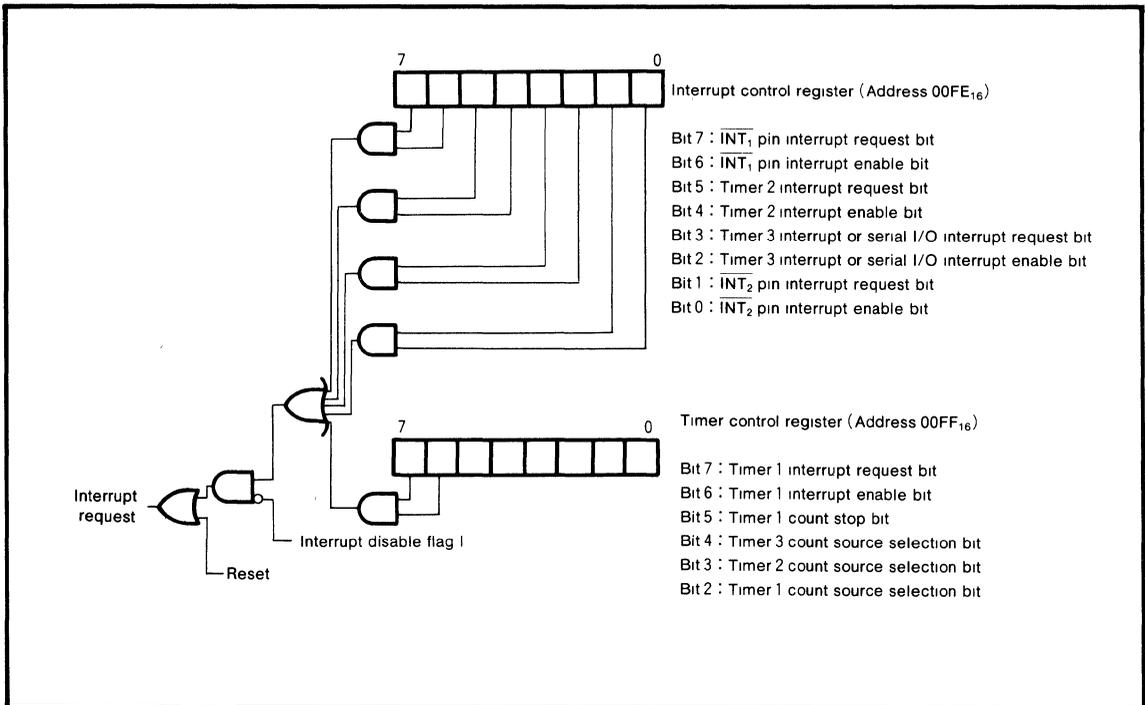


Fig.3 Interrupt control

TIMER

The M37415M4-XXXXP has five timers; timer 1, timer 2, timer 3, timer 4, and timer 5. The interrupt of timer 3 cannot be used when serial I/O is used (see serial I/O section). The count source for timer 1, timer 2, timer 3 can be selected by using bit 2, 3 and 4 of the timer control register (address 00FF₁₆), as shown in Figure 5. A block diagram of timer 1 through 5 is shown in Figure 4. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timers is $1/(n+1)$, where n is the contents of timer latch.

The timer interrupt request bit is set at the next count pulse after the timer reaches "0". The interrupt and timer control registers are located at addresses 00FE₁₆, and 00FF₁₆, respectively (see interrupt section). The starting and stopping of timer 1 is controlled by bit 5 of the timer control register. If bit 5 (address 00FF₁₆) is "0", the timer starts counting. When bit 5 is "1", the timer stops.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if timer 2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 1, count stop bit), bit 6 of the timer control register (timer 1 interrupt enable bit), and bit 4 of interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

TIMER 4 AND TIMER 5 MODES

- (1) Timer mode [00].
The internal clock divided by 4 is counted. When the timer counts to "0", the interrupt request bit is set to "1", the contents of the timer latch is reloaded, and the counting starts again.
- (2) Pulse output mode [01].
The output level of the CNTR pin inverts each timer the timer contents to zero.
- (3) Event counter mode [10].
The same function is executed as that of mode "00", except that the counting source is input from the CNTR pin. The count decreased each time the CNTR input goes from "L" to "H".
- (4) Pulse width measurement mode [11].
This mode is used to measure the pulse width of a signal (between "L"s) input into the CNTR pin. The counting is done using the oscillation frequency divided by 4, and only while the CNTR pin is at a low level. When the contents of the counter reaches zero, the timer 5 overflow flag is set to "1", the timer is reloaded from the reload latch, and counting starts again. The overflow flag can be reset by writing a "0" to bit 7 of address 00F8₁₆.
The structure of timer 4, 5 mode register is shown in Figure 6.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

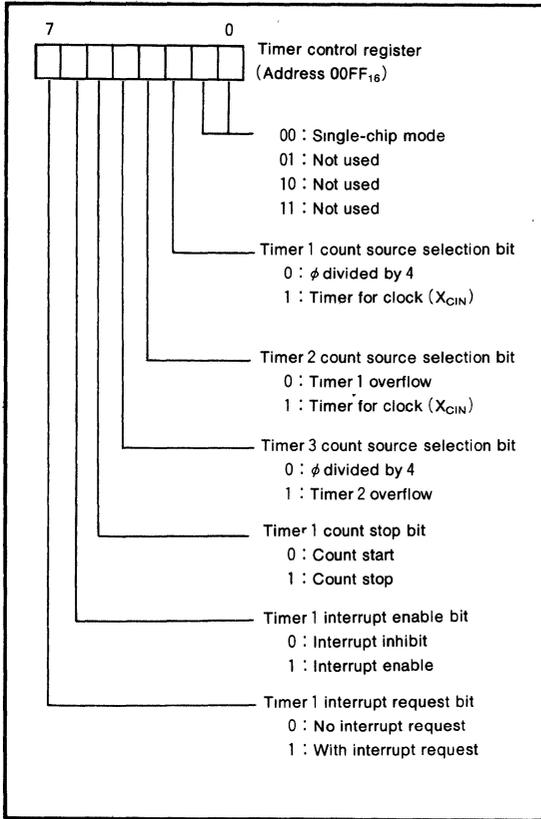


Fig.5 Structure of timer control register

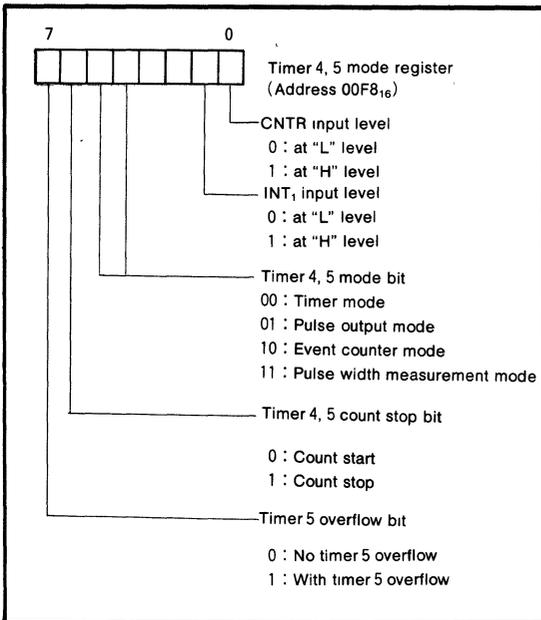


Fig.6 Structure of timer 4, 5 mode register

PORT P3₃/TIMER 3 OUTPUT

The signal that timer 3 is divided by 2 is output from P3₃ (T), at the contents of bit 4 of the serial I/O mode register (address 00F6₁₆) is "1"

WATCHDOG TIMER FUNCTION

Timer 4 and 5 can be used as a watchdog timer by connecting the CNTR pin and the RESET pin as shown in Figure 7, and by setting bit 4 and 5 of address 00F8₁₆ to "01". At this time the output of the 1/2 divider counter (connected to timer 5) is initialized to "1" when data is written to timer 5. After a delay of 12.5 to 15.0 μ s (at $f(X_{IN}) = 800$ kHz) after the reset is input, bits 4,5 and 6 of the timer 4,5 mode register are initialized to "0". The initialization program to set the watchdog timer mode should have the following sequence;

- (1) Set the pulse output mode after writing a value to timer 4 and 5 registers.
- (2) If the program is running correctly, the CNTR pin should never go low due to data being continuously written to timer 5. If the program sequence is interrupted timer 5 will overflow and the CNTR pin will output a "L" and retain this value until the reset is executed.
- (3) 12.5 to 17.5 μ s (at $f(X_{IN}) = 800$ kHz) after a reset, the CNTR pin will be in high impedance state.

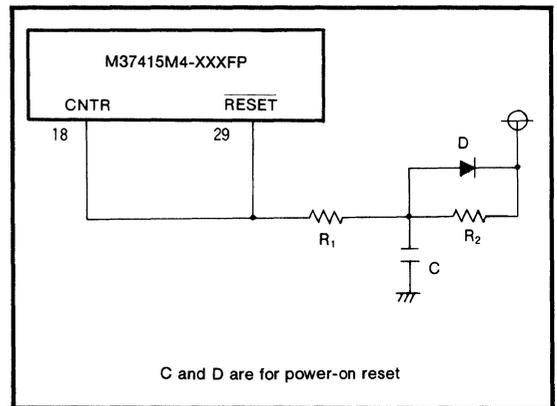


Fig.7 Reset circuit with the watchdog timer

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

SERIAL I/O

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT} , S_{IN}) pins are used as P3₇, P3₆, P3₅, and P3₄, respectively. The serial I/O mode register (address 00F6₁₆) is an 8-bit

register. Bit 0 and 1 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from P3₆ is selected. When these bits are [10], the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

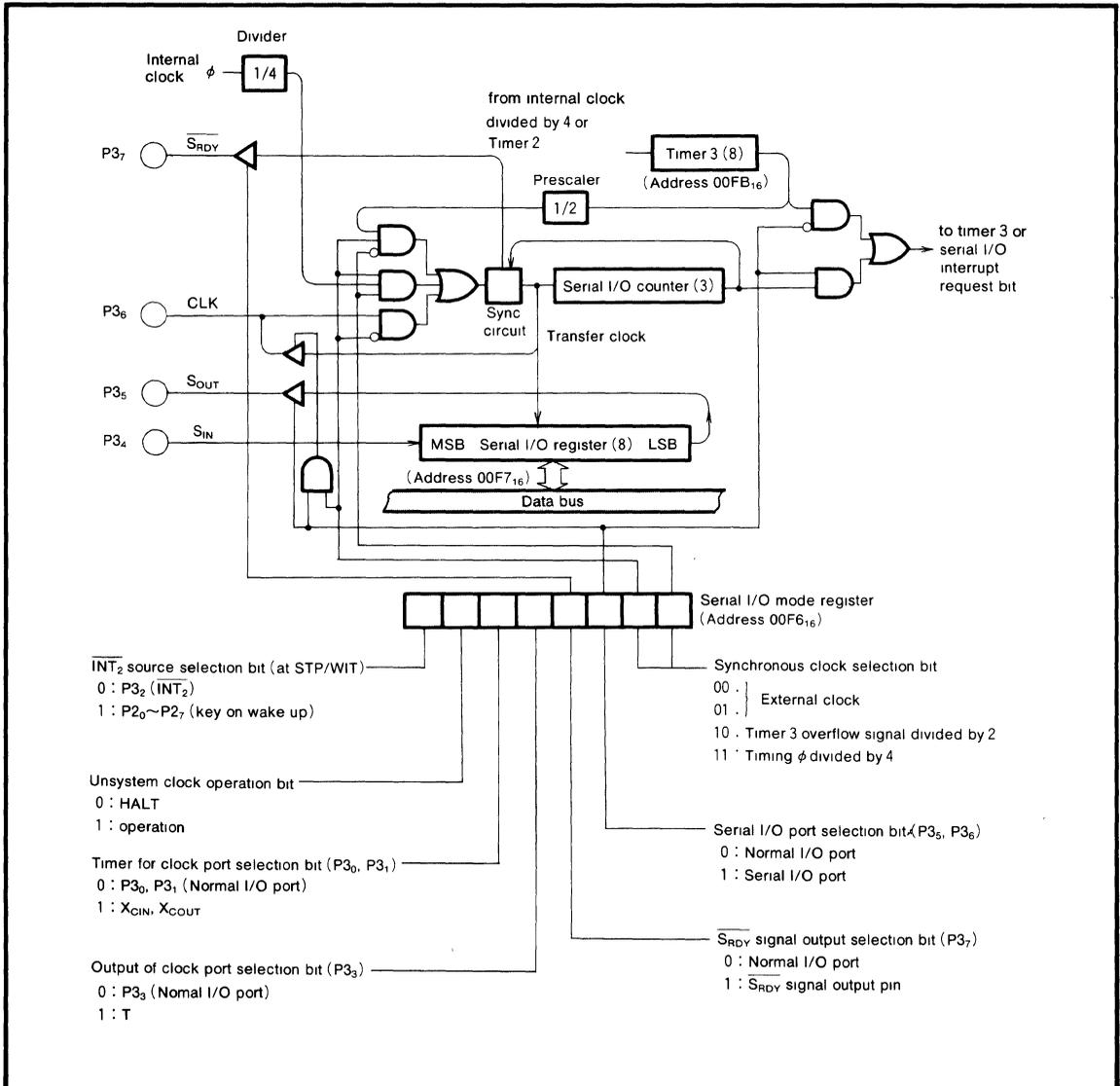


Fig.8 Block diagram of serial I/O

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", P3₆ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P3₆. If the external synchronous clock is selected, the clock is input to P3₆. And P3₅ will be a serial output, and P3₄ will be a serial input. To use P3₄ as a serial input, set the directional register bit which corresponds to P3₄, to "0". For more information on the directional register, refer to the I/O pin section. To use the serial I/O, bit 2 needs to be set to "1", if it is "0" P3₆ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 3. Bit 3 determines if P3₇ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 3="0").

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock- The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal

becomes low signaling that the M37415M4-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to P3₅. During the rising edge of this clock, data can be input from P3₄ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock- If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 50kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9, and connection between two M37415M4-XXXFP's are shown in Figure 10.

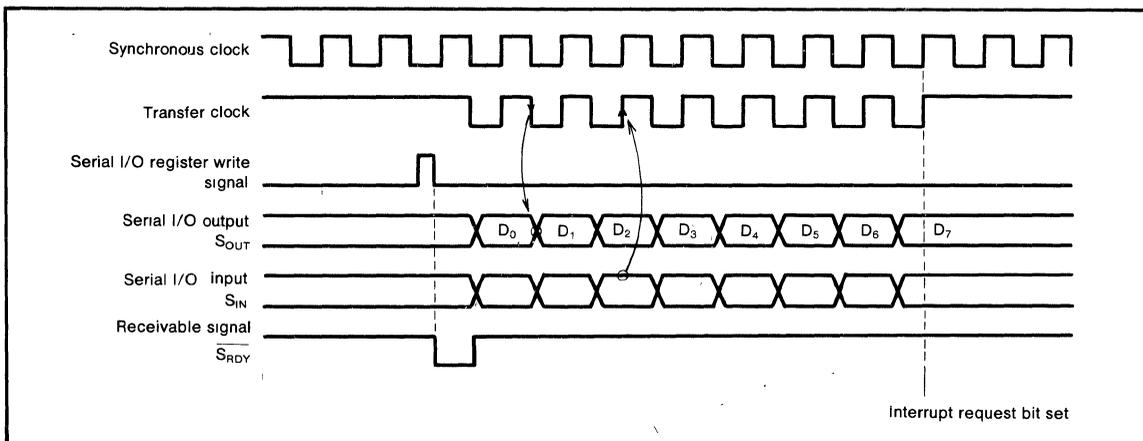


Fig.9 Serial I/O timing

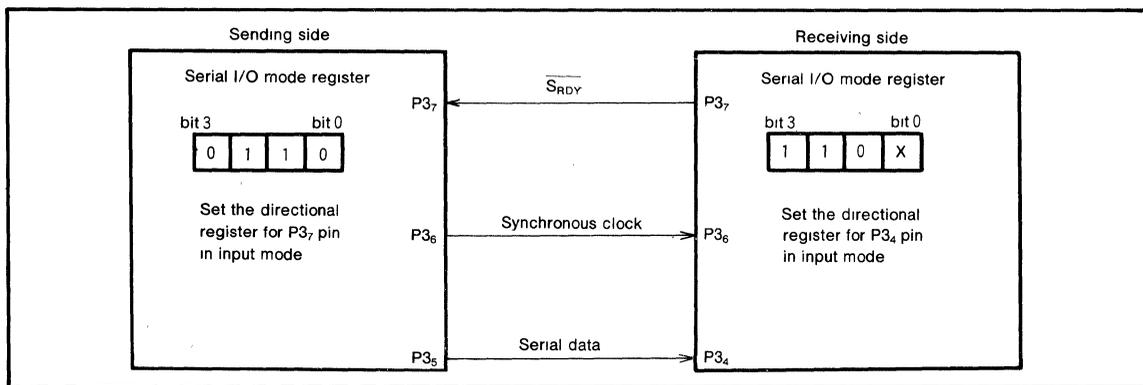


Fig.10 Example of serial I/O connection

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DTMF FUNCTION

The M37415M4-XXXFP has the DTMF (Dual-Tone Multi-Frequency) output and control function. The value of bit 0, and bit 1 of DTMF register (address 00F4₁₆) determines the low frequency band value. And the value of bit 2, and bit 3 of DTMF register determines the high frequency band value. The DTMF output can be controlled by the value of bit 4, and bit 5 of the DTMF register. When bit 4 is "1" the low frequency band is output to Tone, and when bit 4 is "0" the output of low frequency band is stopped. When bit 5 is "1" the high frequency band is output to Tone, and when bit 5 is "0" the output of high frequency band is stopped. The value of bit 6, and 7 of DTMF register determines the basic frequency. The structure of the DTMF register is shown in Figure 11. The accuracy of DTMF output value is shown in Table 2 and 3.

Table 2. Accuracy of DTMF output (at low frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
697	694.44	-2.555	-0.367
770	769.23	-0.769	-0.1
852	854.7	2.7	0.317
941	938.97	-2.033	-0.216

Table 3. Accuracy of DTMF output (at high frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
1209	1204.8	-4.181	-0.346
1336	1333.3	-2.667	-0.2
1477	1470.6	-6.412	-0.434
1633	1639.3	6.344	0.389

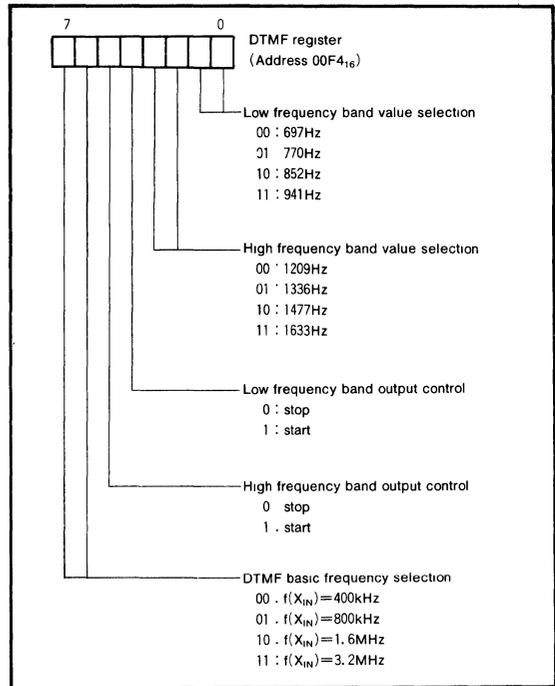


Fig.11 Structure of the DTMF register

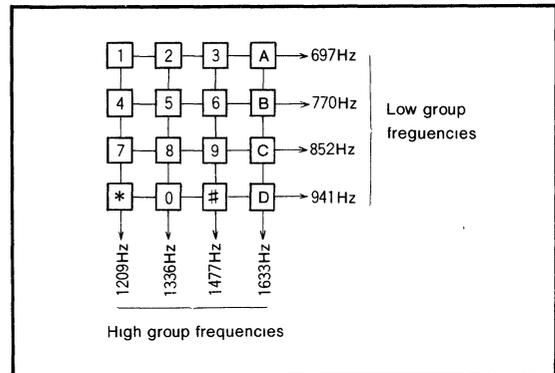


Fig.12 Telephone keys and DTMF

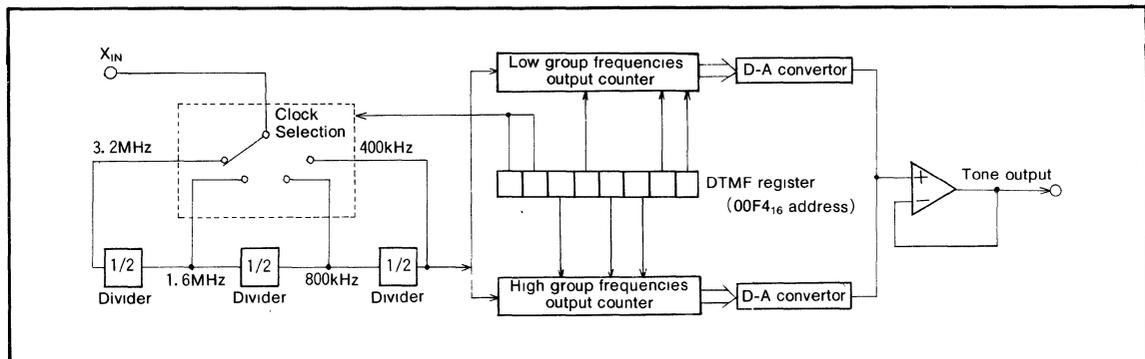


Fig.13 Block diagram of DTMF generator

LCD CONTROLLER/DRIVER

The M37415M4-XXXFP has internal LCD controllers and drivers. A block diagram of LCD circuit is shown in Figure 17.

The terminals for LCD consist of 4 common-pin and 32 segments pin. SEG₂₄~SEG₃₁ are in common with input P4. These pins are selected by bit 4 of the LCD mode register (LM₄, address 00F5₁₆). Two biases (1/2 and 1/3) can also be selected. When bit 2 of the LCD mode register is "1", 1/2 bias is selected. When bit 2 is "0", 1/3 bias is selected. A 1/2, 1/3, or 1/4 duty cycle can also be selected. When bits 0 and 1 of the LCD mode register (LM₀, LM₁) is n, the duty ratio is 1/(n+1).

Address 00D0₁₆ ~ 00DF₁₆ is the designated RAM for the LCD display. When 1s' are written to these addresses, the corresponding segments of the LCD display panel are turned on. A map of the LCD display RAM is shown in Figure 15. The ON/OFF function for the LCD controller is controlled by bit 3 of the LCD mode register (LM₃). When this bit is "1" all the segments of the LCD are turned on. When this bit is "0" all the segments are turned off. An example circuit for each bias is shown in Figure 18 and Figure 19 describes the LCD driver waveforms for each bias and duty cycle.

The LCDCK timing frequency (LCD driver timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{\text{(frequency of timer 1 count source)}}{\text{((timer 1 setting+1) \times 4)}}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{n} \quad ; \text{ at } 1/n \text{ duty}$$

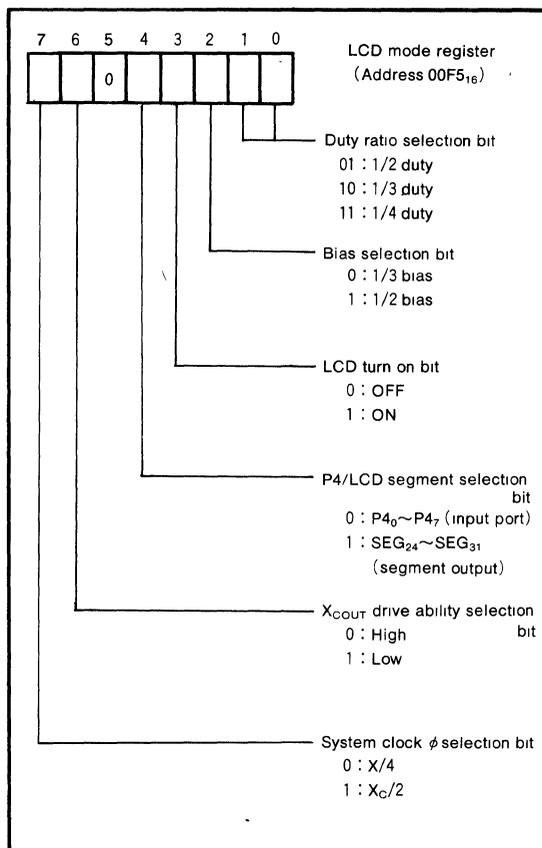


Fig.14 Structure of the LCD mode register

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Bit Address	7	6	5	4	3	2	1	0
D0	1	1	1	1	0	0	0	0
D1	3	3	3	3	2	2	2	2
D2	5	5	5	5	4	4	4	4
D3	7	7	7	7	6	6	6	6
D4	9	9	9	9	8	8	8	8
D5	11	11	11	11	10	10	10	10
D6	13	13	13	13	12	12	12	12
D7	15	15	15	15	14	14	14	14
D8	17	17	17	17	16	16	16	16
D9	19	19	19	19	18	18	18	18
DA	21	21	21	21	20	20	20	20
DB	23	23	23	23	22	22	22	22
DC	25	25	25	25	24	24	24	24
DD	27	27	27	27	26	26	26	26
DE	29	29	29	29	28	28	28	28
DF	31	31	31	31	30	30	30	30
	COM ₃	COM ₂	COM ₁	COM ₀	COM ₃	COM ₂	COM ₁	COM ₀

* Number in data memory area indicates corresponding segment.

Fig. 15 Map of RAM for LCD segment

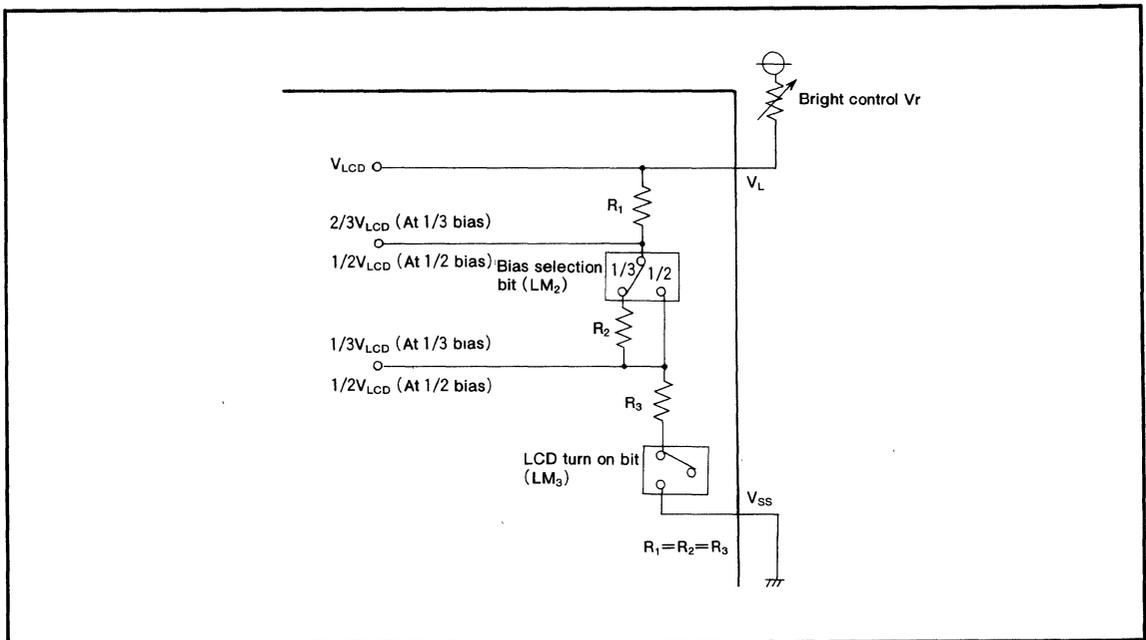


Fig.16 Internal circuit of LCD power supply input pin

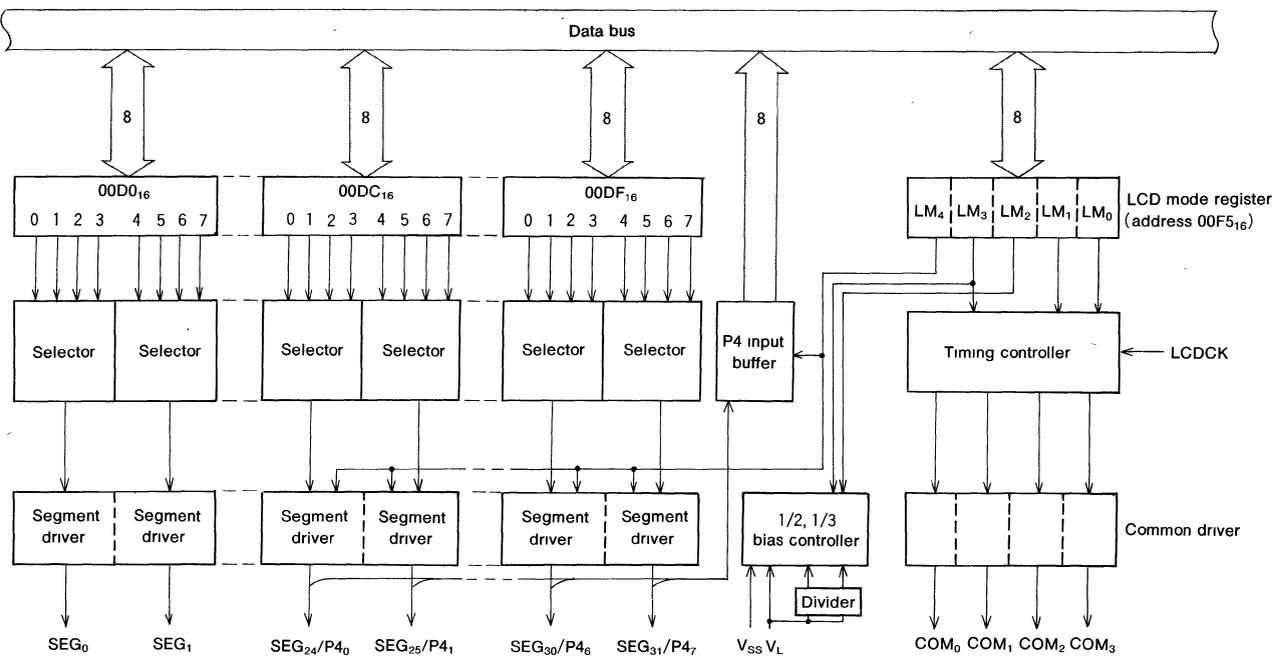


Fig.17 Block diagram of LCD control circuit

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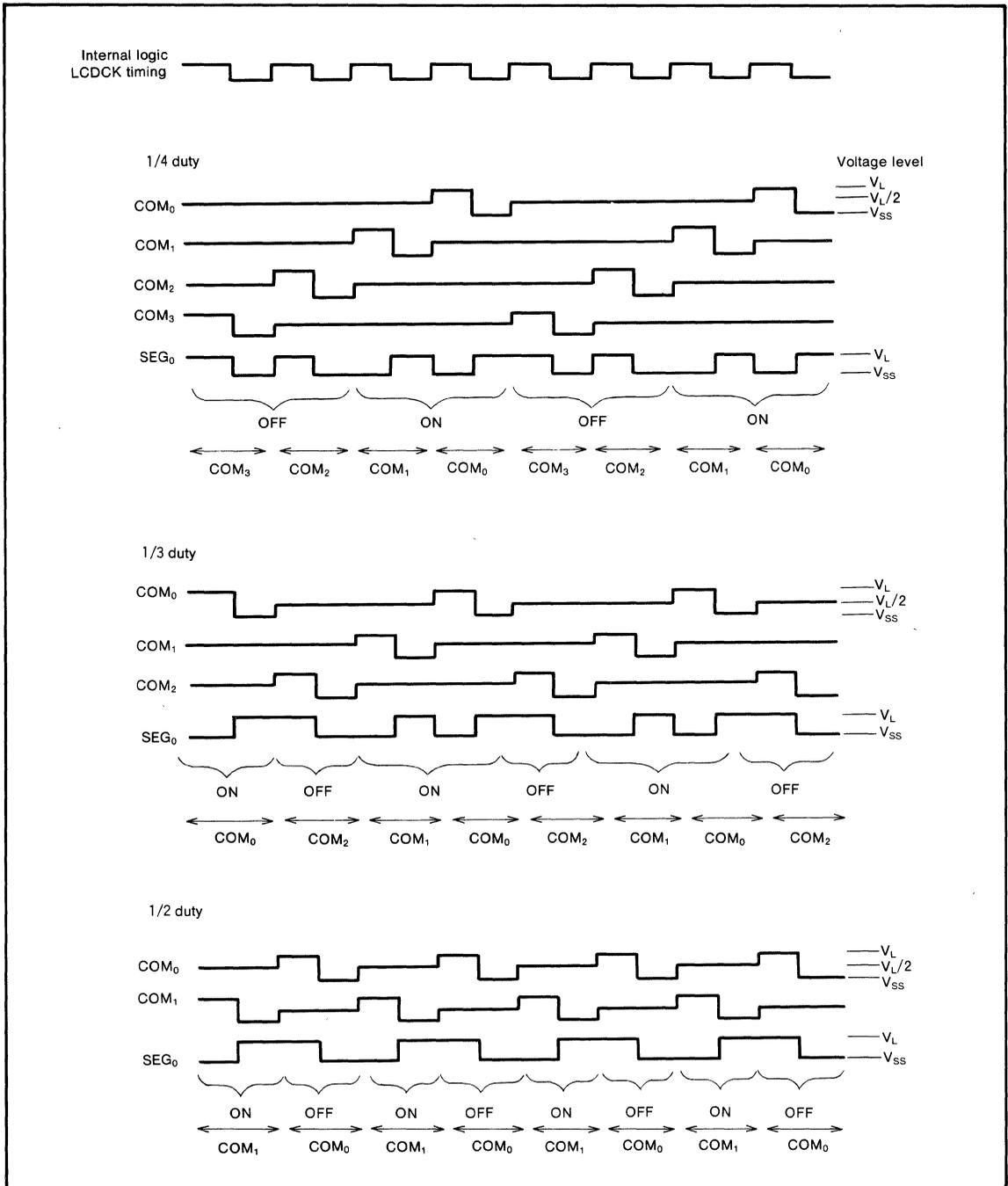


Fig.18 LCD drive waveform (at 1/2 bias)

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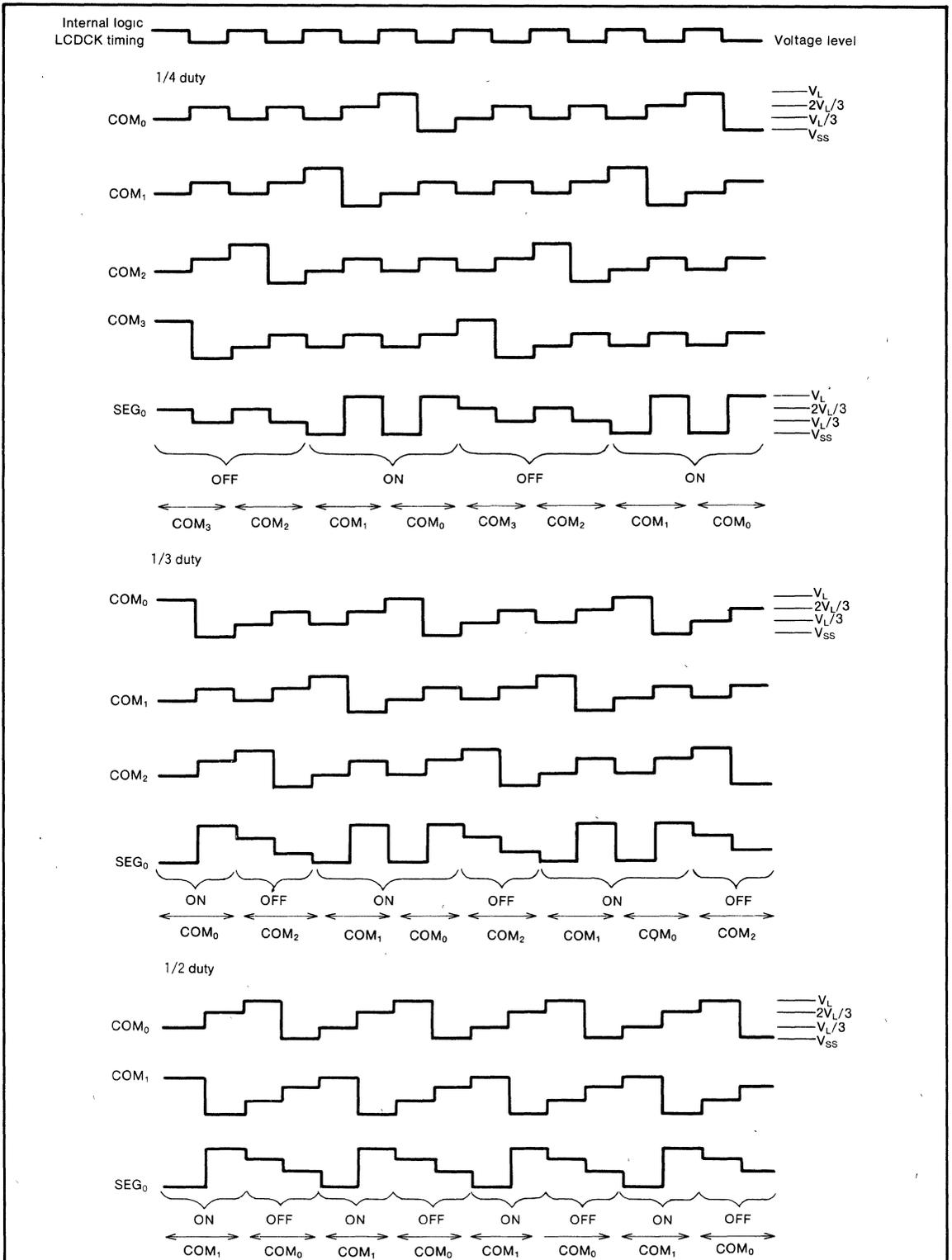


Fig.19 LCD drive waveform (at 1/3 bias)

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KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P2 has a "L" level applied, after bit 7 of the serial I/O mode register (SM₇) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. As shown in Figure 20, a key matrix can be connected to port P2 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the \overline{INT}_2 interrupt. When SM₇ is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and \overline{INT}_2 are invalid.

In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and SM₇ is "1", all of port P2 must be input "H"

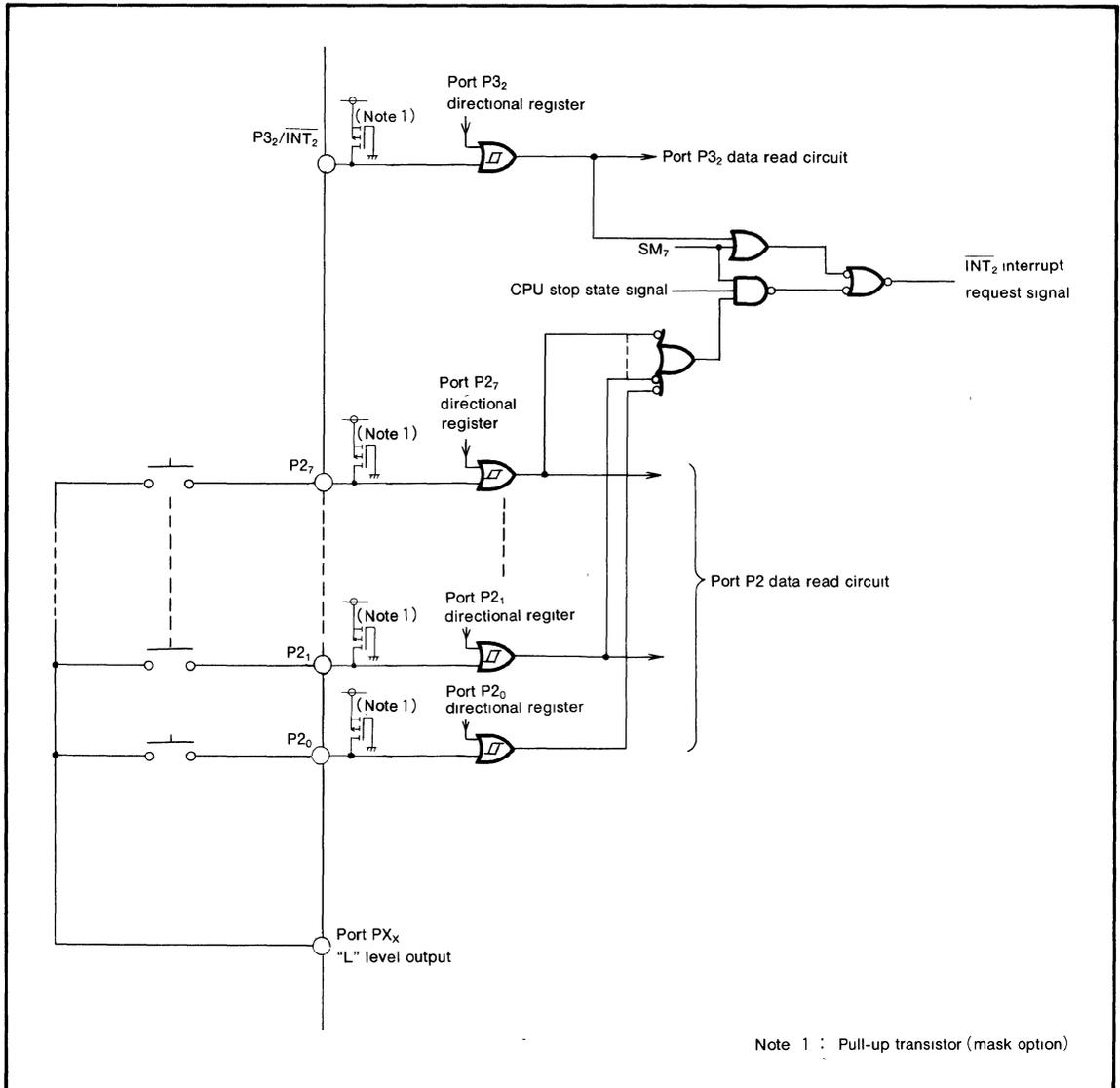


Fig.20 Block diagram of port P2 and P3₂, and example of wired at used key on wake up

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RESET CIRCUIT

The M37415M4-XXXFP is reset according to the sequence shown in Figure 23. It starts the program from the address formed by using the content of address 3FFF₁₆ as the high order address and the content of the address 3FFE₁₆ as the low order address, when the RESET pin is held at "L" level for at least 8 rising edges of X_{IN} while the power voltage is in the recommended operating condition and the crystal

oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are as shown in Figure 21, regardless of the status before reset (including stop mode or wait mode).

An example of the reset circuit is shown in Figure 22. When the power on reset is used and the reset is used while the X_{IN} clock is stopped, the RESET pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

	Address	
(1) Port P0 directional register	(00E1 ₁₆)	00 ₁₆
(2) Port P1 directional register	(00E3 ₁₆)	00 ₁₆
(3) Port P2 directional register	(00E5 ₁₆)	00 ₁₆
(4) Port P3 directional register	(00E9 ₁₆)	00 ₁₆
(5) DTMF register	(00F4 ₁₆)	0 0 0 0
(6) LCD mode register	(00F5 ₁₆)	00 ₁₆
(7) Serial I/O mode register	(00F6 ₁₆)	00 ₁₆
(8) Timer 4, 5 mode register	(00F8 ₁₆)	0 0 0 0
(9) Interrupt control register	(00FE ₁₆)	00 ₁₆
(10) Timer control register	(00FF ₁₆)	00 ₁₆
(11) Interrupt disable flag for processor status register	(PS)	1
(12) Program counter	(PC _H)	Contents of address 3FFF ₁₆
	(PC _L)	Contents of address 3FFE ₁₆

Note : Since the contents of both registers other than those listed above (including timers and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

Fig.21 Internal state of microcomputer at reset

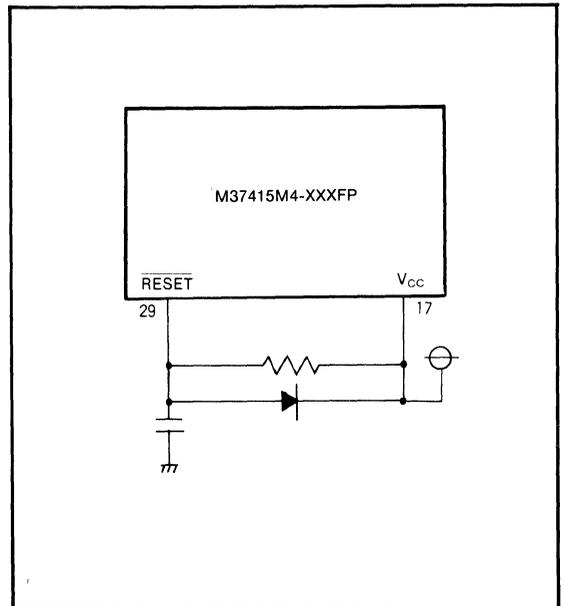


Fig.22 Example of reset circuit

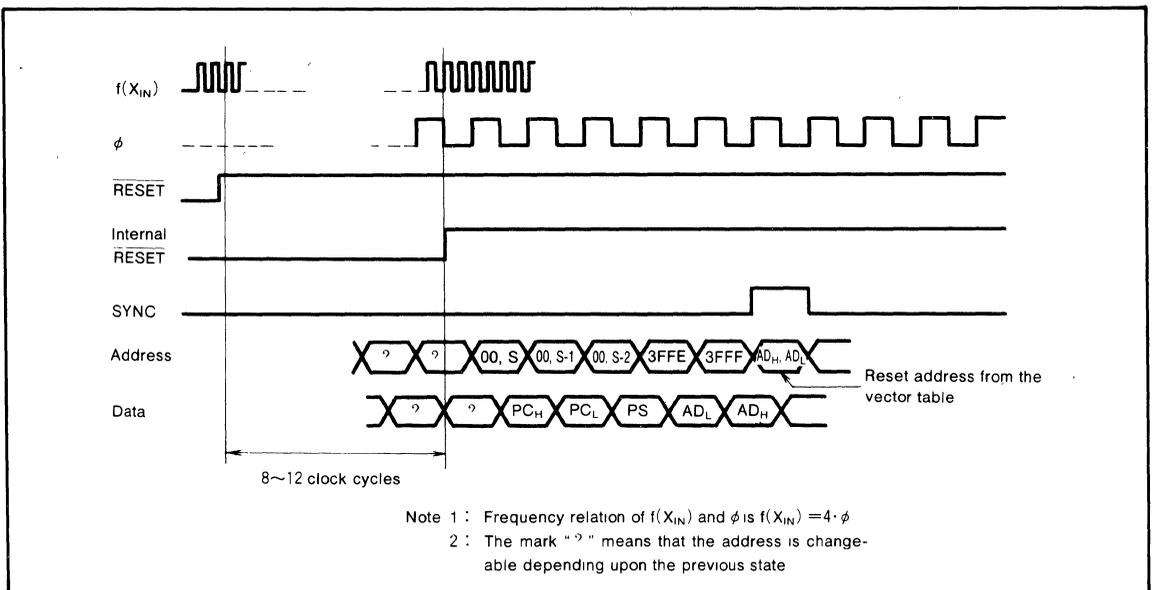


Fig.23 Timing diagram at reset

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I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address 00E0₁₆. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address 00E1₁₆) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

(2) Port P1

Port P1 has the same function as P0.

(3) Port P2

Port P2 has the same function as P0. Following the execution of STP or WIT instruction, P2 can be used to generate the "wake up mode". This mode is used to bring the microcomputer back in its normal operating mode after being in the power-down mode.

(4) Port P3

Port P3 has the same function as P0 except that part of P3 is common with the serial I/O lines (ie output of timer 3, input/output of timer clock, and interrupt input).

(5) Segment output (SEG₀~SEG₂₃)

These ports drive and control the LCD segments.

(6) Port P4

Port P4 is an 8-bit input port which can be used as a LCD segment output port.

(7) Common output (COM₀~COM₃)

This port provides output drive and control for the LCD common lines.

(8) Power supply for LCD (V_L)

Supplies power to the LCD terminals.

(9) INT₁

The INT₁ pin is an interrupt pin. The INT₁ interrupt request bit (bit 7 of address 00FE₁₆) is set to "1" when the input level of this pin changes from "H" to "L". This input level is read into bit 1 of the timer 4 and 5 mode register (address 00F8₁₆).

(10) INT₂ (INT₂/P3₂)

The INT₂ pin is an interrupt input pin common with P3₂. When P3₂'s directional register is set for input ("0"), this pin can be used as an interrupt input. The INT₂ interrupt request bit (bit 1 of address 00FE₁₆) is automatically set to "1" when the input level of this pin changes from "H" to "L".

(11) CNTR

The CNTR pin is an I/O pin of timer 4 and 5. The input level is read into bit 0 of the timer 4 and 5's mode register (address 00F8₁₆).

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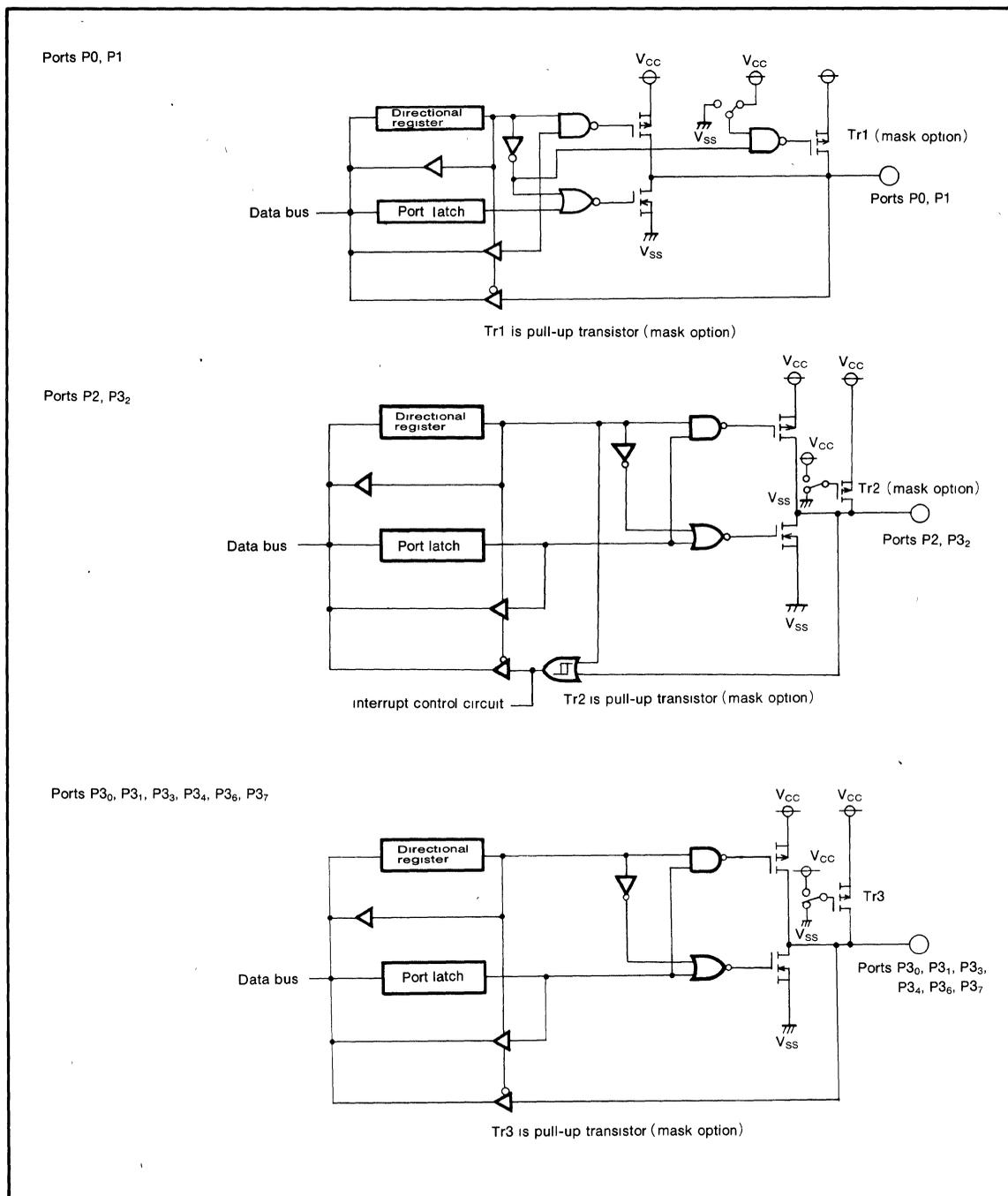


Fig.24 Block diagram of ports P0~P3

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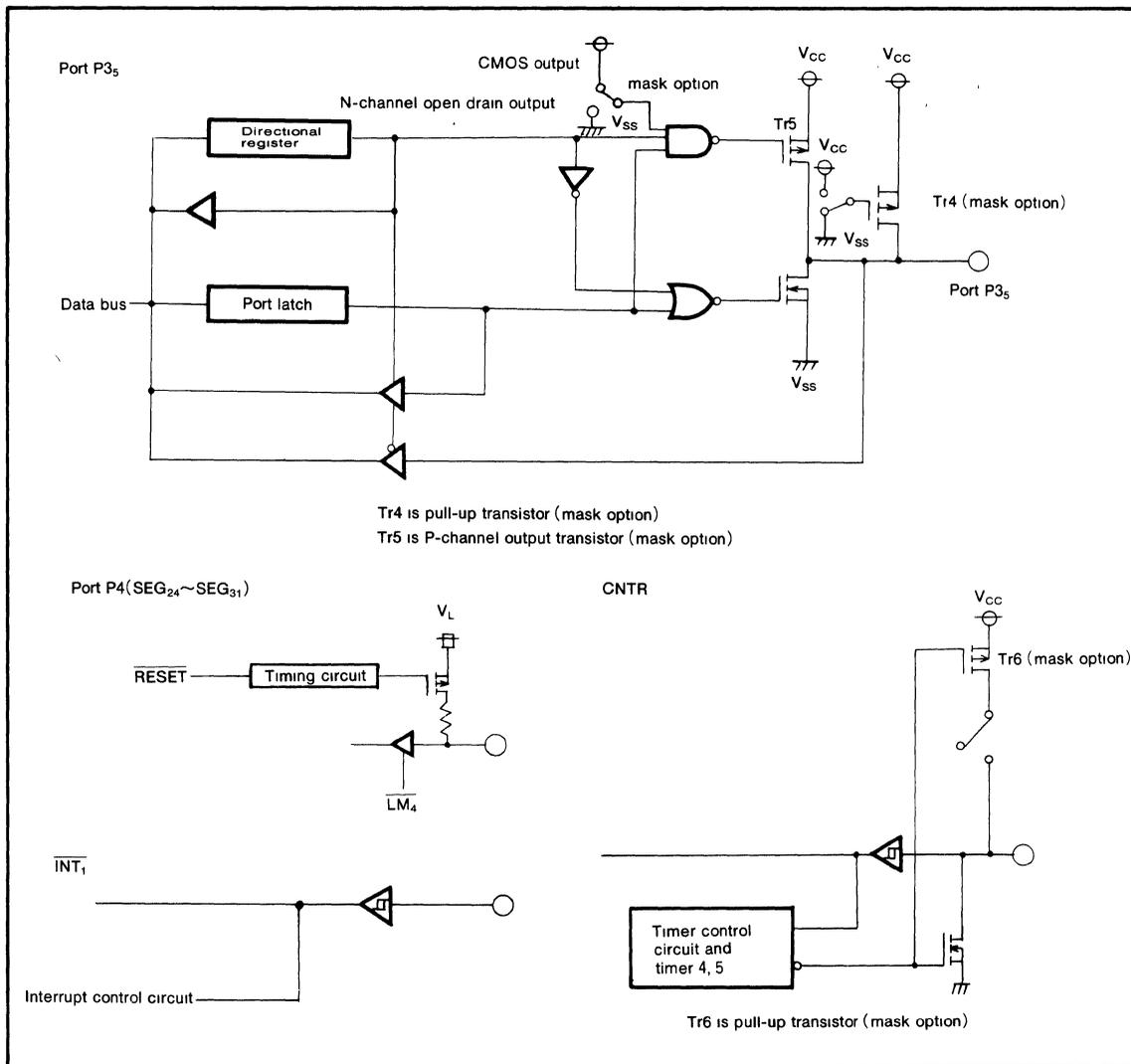


Fig.25 Block diagram of ports P3, P4, CNTR, and INT₁

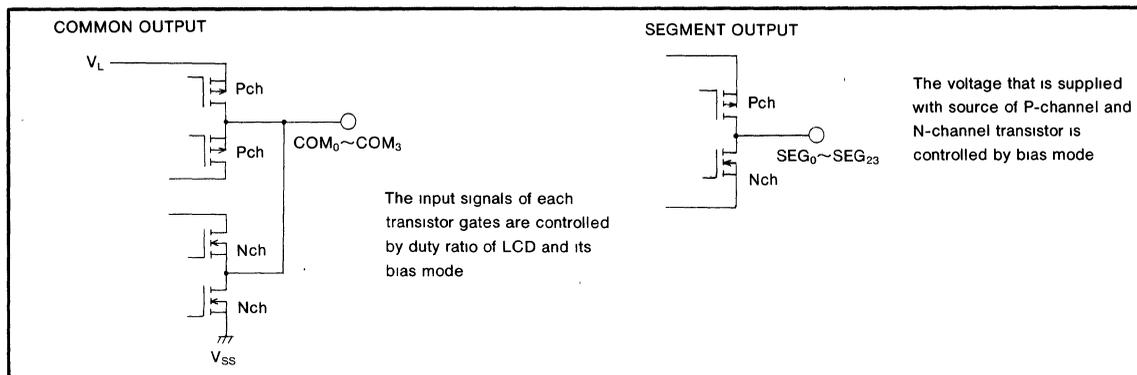


Fig.26 Block diagram of COM, SEG

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CLOCK GENERATING CIRCUIT

The M37415M4-XXXFP has two internal clock generating circuit. Figure 29 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ . Bit 7 of LCD mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN} .

Figure 27 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input form the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 28.

The M37415M4-XXXFP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. Before executing the STP instruction, appropriate values must be set in timer 1 and timer 2 to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), timer 1 interrupt enable bit and timer 2 interrupt enable bit must be set to disable ("0"), and timer 2 interrupt request bit must be set to no request ("0").

Oscillation is restarted (release the stop mode) when INT_1 , INT_2 , key on wake up or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 2 overflows and is not supplied to the CPU.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) the microcomputer receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock. X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the \overline{RESET} pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 30 shows the transition states for the system clock.

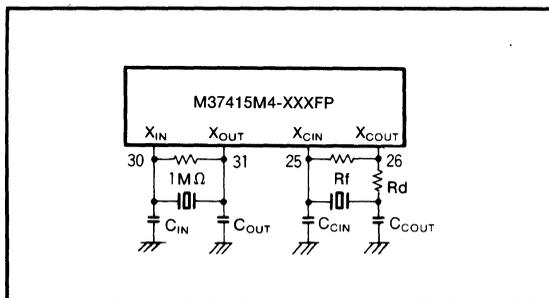


Fig.27 External ceramic resonator circuit

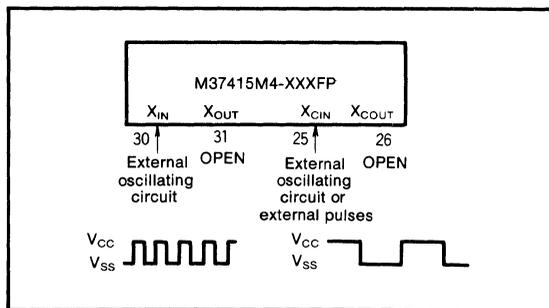
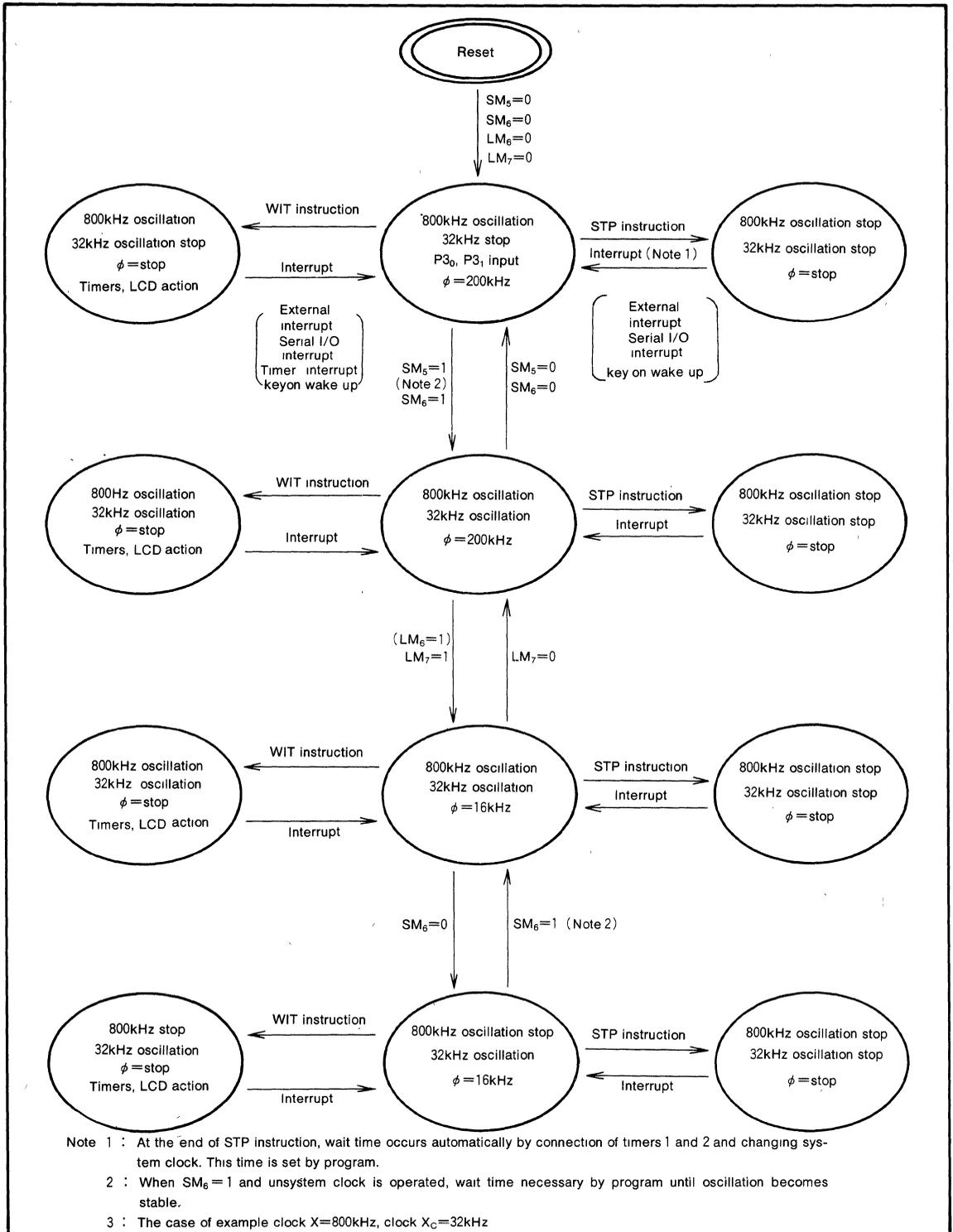


Fig.28 External clock input circuit

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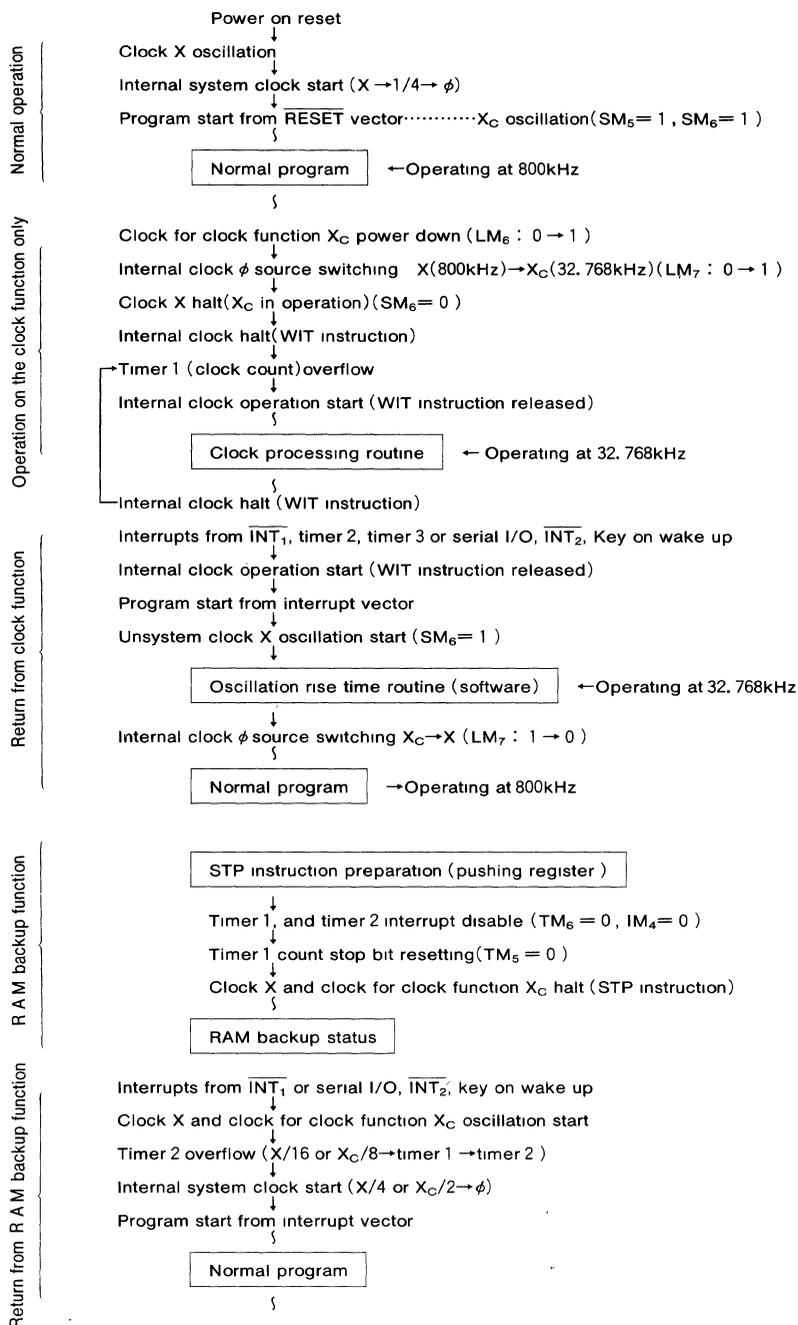


- Note 1 : At the end of STP instruction, wait time occurs automatically by connection of timers 1 and 2 and changing system clock. This time is set by program.
 Note 2 : When SM₆=1 and unsystem clock is operated, wait time necessary by program until oscillation becomes stable.
 Note 3 : The case of example clock X=800kHz, clock X_C=32kHz

Fig.30 External clock input circuit

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<An example of flow for system>



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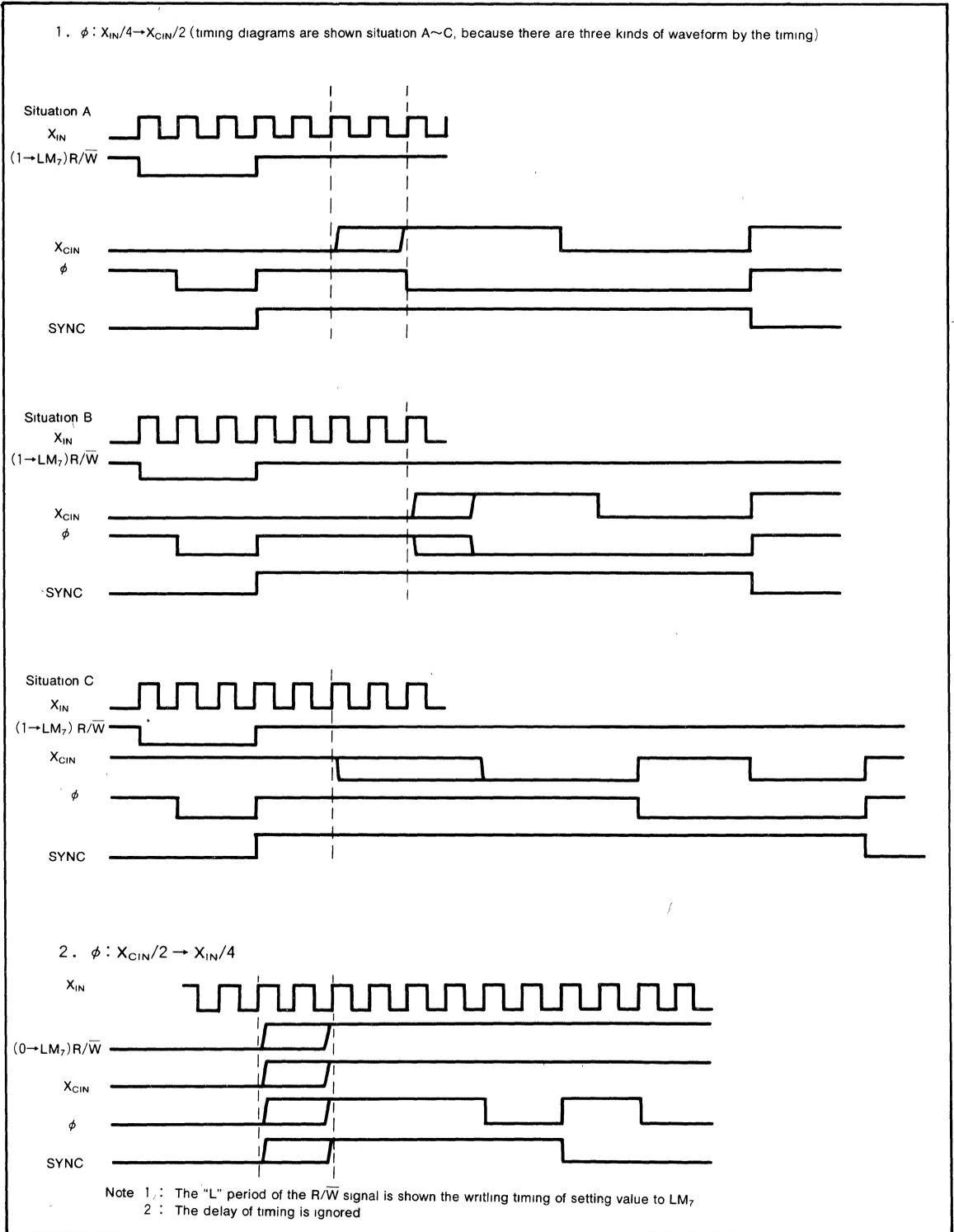


Fig.31 Timing diagram of the changing system clock

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PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modifications are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) When the timer 4 and the timer 5 are used at event counter mode, read the contents of these timers either while the input of these timers are not changing or after timer 4, 5 count stop bit (bit 6 of address $00F8_{16}$) is set to "1".
Also, when the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, control the same as above.
- (4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) When LCD turn-on bit (bit 3 of address $00F5_{16}$) of the LCD mode register is "1", don't stop the timers or count source for timers.
- (7) The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.
- (8) Notes on controlling the clock generation circuit
 - ① When system clock is changed $X_{IN}/4$ to $X_{CIN}/2$, set LM_7 to "1" after oscillation is stable by the software in side of clock X_C .
 - ② When system clock is changed $X_{CIN}/2$ to $X_{IN}/4$, set LM_7 to "0" after oscillation is stable by the software in side of clock X .
 - ③ When SM_5 is "0" or when LM_7 is "0" and SM_6 is "0", LM_6 is automatically set to "0" by the hardware.
 - ④ When system clock selection bit (bit 7 of address $00F5_{16}$) of the LCD mode register is "1", don't set SM_5 to "0".

Just for reference, timing diagram of the changing system clock are shown in Figure 31.

- (9) In order to avoid noise and latch-up, connect the following external circuit.
 - ① Connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.
 - ② Connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{REF} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation from
- (2) mark specification from
- (3) ROM data EPROM 3 sets

Write the following option on the mask ROM confirmation from

- Port P0 pull-up transistor bit (see the confirmation form)
- Port P1 pull-up transistor bit (see the confirmation form)
- Port P2 pull-up transistor bit (see the confirmation form)
- Port P3 pull-up transistor bit (see the confirmation form)
- Port $P3_5/S_{OUT}$ output type (see the confirmation form)
- CNTR pin pull up transistor (see the confirmation form)

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-0.3~7	V
V _I	Input voltage for LCD V _L		-0.3~V _{CC} +0.3	V
V _I	Input voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ P3 ₀ ~P3 ₇ , SEG ₂₄ ~SEG ₃₁ , X _{IN}		-0.3~V _{CC} +0.3	V
V _I	Input voltage INT ₁ , CNV _{SS} , V _{REF}		-0.3~7	V
V _I	Input voltage RESET, CNTR		-0.3~13	V
V _O	Output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ P3 ₀ ~P3 ₇ , COM ₀ ~COM ₃ , SEG ₀ ~SEG ₃₁ X _{OUT}		-0.3~V _{CC} +0.3	V
V _O	Output voltage CNTR		-0.3~7	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 2.7~5.5V, V_{SS} = 0V, T_a = -10~70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V _{CC}	Supply voltage (Note 1)	f(X _{IN}) = 3.2MHz	4.5		5.5	V
		f(X _{IN}) = 800kHz	2.5		5.5	
V _{SS}	Supply voltage			0		V
V _{REF}	Supply voltage for DTMF	R _L ≥ 20kΩ	1.5		V _{CC} -0.5	V
V _{IH}	"H" input voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P3 ₀ , P3 ₁ (Note 2), P3 ₃ ~P3 ₇ (Note 3) P4 ₀ ~P4 ₇ , RESET, X _{IN} , CNV _{SS}		0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P2 ₀ ~P2 ₇ , P3 ₂ , P3 ₆ (Note 4) INT ₁ , CNTR		0.74V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P3 ₀ , P3 ₁ (Note 2), P3 ₃ ~P3 ₇ (Note 3) P4 ₀ ~P4 ₇ , CNV _{SS}		0		0.3V _{CC}	V
V _{IL}	"L" input voltage P2 ₀ ~P2 ₇ , P3 ₂ , P3 ₆ (Note 4) INT ₁ , CNTR		0		0.2V _{CC}	V
V _{IL}	"L" input voltage RESET		0		0.12V _{CC}	V
V _{IL}	"L" input voltage X _{IN}		0		0.16V _{CC}	V
I _{OH}	"H" output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ P3 ₀ ~P3 ₇ (Note 5), X _{OUT}				-2	mA
I _{OL(peak)}	"L" peak output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ P3 ₀ ~P3 ₇ , CNTR, X _{OUT} (Note 6)				10	mA
I _{OL(avg)}	"L" average output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ P3 ₀ ~P3 ₇ , CNTR, X _{OUT} (Note 7)				5	mA
f(X _{IN})	Clock oscillating frequency (Note 8)	V _{CC} = 4.5~5.5V	380		3300	kHz
		V _{CC} = 2.5~5.5V	380		1000	
f(X _{CIN})	Clock oscillating frequency for clock function		32		50	kHz

- Note 1 : When only maintaining the RAM data minimum value of V_{CC} is 2V
 2 : When using port P3₁ as X_{CIN}, 0.85V_{CC} ≤ V_{IH} ≤ V_{CC}, 0 ≤ V_{IL} ≤ 0.15V_{CC} for port P3₁
 3 : In this case of using port P3₆ as normal input.
 4 : In this case of using port P3₆ as CLK input Especially when the input oscillation frequency is more than 50kHz, recommend the following :
 0.8V_{CC} ≤ V_{IH} ≤ V_{CC}, 0 ≤ V_{IL} ≤ 0.2V_{CC}.
 5 : The total of I_{OH} of port P0, P1, P2, P3, X_{OUT} should be 35mA max
 6 : The total of I_{OL(peak)} of port P0, P1, P2, P3 should be 55mA max, and the total of I_{OL(peak)} of port P3, CNTR and X_{OUT} should be 45mA max
 7 : I_{OL(avg)} is the average current in 100ms
 8 : When using DTMF function, f(X_{IN}) should be 400kHz, 800kHz, 1.6MHz, or 3.2MHz

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ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$, $T_a = -10 \sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit		
			Min	Typ	Max			
V_{OH}	"H" output voltage $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7$ $P3_0 \sim P3_7$ (Note 1) (Note 2)	$V_{CC} = 5V, I_{OH} = -2mA$	3			V		
		$V_{CC} = 3V, I_{OH} = -0.7mA$	2					
V_{OH}	"H" output voltage X_{OUT}	$V_{CC} = 5V, I_{OH} = -1.5mA$	3			V		
		$V_{CC} = 3V, I_{OH} = -0.3mA$	2					
V_{OL}	"L" output voltage $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7$ $P3_0 \sim P3_7$ (Note 2), CNTR	$V_{CC} = 5V, I_{OL} = 10mA$			2	V		
		$V_{CC} = 3V, I_{OL} = 3mA$			1			
V_{OL}	"L" output voltage X_{OUT}	$V_{CC} = 5V, I_{OL} = 1.5mA$			2	V		
		$V_{CC} = 3V, I_{OL} = 0.3mA$			1			
$V_{T+} - V_{T-}$	Hysteresis $\overline{INT_1}, \overline{CNTR}$	$V_{CC} = 5V$	0.25		1	V		
		$V_{CC} = 3V$	0.15		0.7			
$V_{T+} - V_{T-}$	Hysteresis $P3_6$	When used as $V_{CC} = 5V$ CLK input		0.5		V		
		$V_{CC} = 3V$		0.4				
$V_{T+} - V_{T-}$	Hysteresis $P3_1$	When used as $V_{CC} = 5V$ X_{CIN} input		0.7		V		
		$V_{CC} = 3V$		0.5				
$V_{T+} - V_{T-}$	Hysteresis $P2_0 \sim P2_7, P3_2$	$V_{CC} = 5V$		0.5		V		
		$V_{CC} = 3V$		0.4				
$V_{T+} - V_{T-}$	Hysteresis \overline{RESET}	$V_{CC} = 5V$		0.5	0.7	V		
		$V_{CC} = 3V$		0.35				
$V_{T+} - V_{T-}$	Hysteresis X_{IN}	$V_{CC} = 5V$		0.5		V		
		$V_{CC} = 3V$		0.35				
I_{IL}	"L" input current $SEG_{24} \sim SEG_{31}$ (Except reset state) $\{P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P3_0 \sim P3_7\}$ Without pull-up Tr $\overline{INT_1}, \overline{RESET}, X_{IN}$	$V_{CC} = 5V, V_i = 0V$			-5	μA		
		$V_{CC} = 3V, V_i = 0V$			-4			
I_{IL}	"L" input current $\{P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P3_0 \sim P3_7, \overline{CNTR}\}$ With pull-up Tr	$V_{CC} = 5V, V_i = 0V$	-30	-70	-140	μA		
		$V_{CC} = 3V, V_i = 0V$	-6	-25	-45			
I_{IL}	"L" input current $SEG_{24} \sim SEG_{31}$ (at reset state)	$V_{CC} = 5V, V_L = 5V, V_i = 0V$	-30		-140	μA		
		$V_{CC} = 3V, V_L = 3V, V_i = 0V$	-6		-45			
I_{IH}	"H" input current $SEG_{24} \sim SEG_{31}$ (Except reset state) $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7$ $P3_0 \sim P3_7, \overline{INT_1}, \overline{RESET}, X_{IN}$	$V_{CC} = 5V, V_i = 5V$			5	μA		
		$V_{CC} = 3V, V_i = 3V$			4			
I_{IH}	"H" input current $SEG_{24} \sim SEG_{31}$ (at reset state)	$V_{CC} = 5V, V_L = 5V, V_i = 5V$			5	μA		
		$V_{CC} = 3V, V_L = 3V, V_i = 3V$			4			
I_{CC}	Supply current	Output pins are opened $\overline{RESET}, P0_0 \sim P0_7,$ $P1_0 \sim P1_7, P2_0 \sim P2_7,$ and $P3_0 \sim P3_7$ are connected to V_{CC} Except the above pins are connected to V_{SS} However, X_{IN} and X_{CIN} are input signal according to the conditions	At operation	$f(X_{IN}) = 3.2MHz$ $V_{CC} = 5V$ at DTMF wave form output	4	8	mA	
				at DTMF wave form stop	3	6		
			$f(X_{IN}) = 800kHz$ $V_{CC} = 3V$ at DTMF wave form output	0.8	1.5	μA		
				at DTMF wave form stop	0.5		1.0	
			At wait state	$T_a = 25^\circ C, X_{IN} = 0V$ $f(X_{CIN}) = 32.8kHz$ at low power mode ($LM_6 = 1$)	$V_{CC} = 5V$	45		μA
				$V_{CC} = 3V$	18			
			At stop state	$f(X_{IN}) = 3.2MHz, V_{CC} = 5V$		1		mA
				$f(X_{IN}) = 800kHz, V_{CC} = 3V$		0.3		
			At stop state	$f(X_{IN}) = 0$ $f(X_{CIN}) = 0$ $V_{CC} = 5V$	$T_a = 25^\circ C$	20	60	μA
					$T_a = 70^\circ C$	4	12	
I_L	V_L current	$V_{CC} = V_L = 5V, \frac{1}{3}$ bias		10	25	μA		
		$V_{CC} = V_L = 3V, \frac{1}{3}$ bias		6	15			
I_{REF}	V_{REF} current	$V_{CC} = 5V, V_{REF} = 4.5V$		100	200	μA		
		$V_{CC} = 3V, V_{REF} = 2.5V$		60	120			
V_{RAM}	RAM retention voltage	$f(X_{IN}) = 0, f(X_{CIN}) = 0$	2		5.5	V		

Note 1 : Except when the output type of $P3_5$ is N-channel open drain (mask option)
2 : If $P3_0$ is used as X_{COUT} , capability of load driving is lower than the above

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DTMF CHARACTERISTICS ($V_{SS} = 0V$, $T_a = -10 \sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max.		
V_{OT}	Output voltage Tone	High frequency band group	$V_{CC}=5V$, $V_{REF}=4.5V$, $R_L=20k\Omega$	470	490	510	mVrms
			$V_{CC}=3V$, $V_{REF}=2.5V$, $R_L=20k\Omega$	257	270	283	
		Low frequency band group	$V_{CC}=5V$, $V_{REF}=4.5V$, $R_L=20k\Omega$	325	345	365	
			$V_{CC}=3V$, $V_{REF}=2.5V$, $R_L=20k\Omega$	177	190	203	
dB_{CR}	Output ratio of high frequency band to low frequency band	$R_L=20k\Omega$	2.5	3	3.5	dB	
DIS	Disportional percentage	$R_L=20k\Omega$, $T_a=25^\circ C$		13		%	

MITSUBISHI MICROCOMPUTERS

M37416M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37416M2-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for office automation equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37416M2-XXXSP and the M37416M2-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

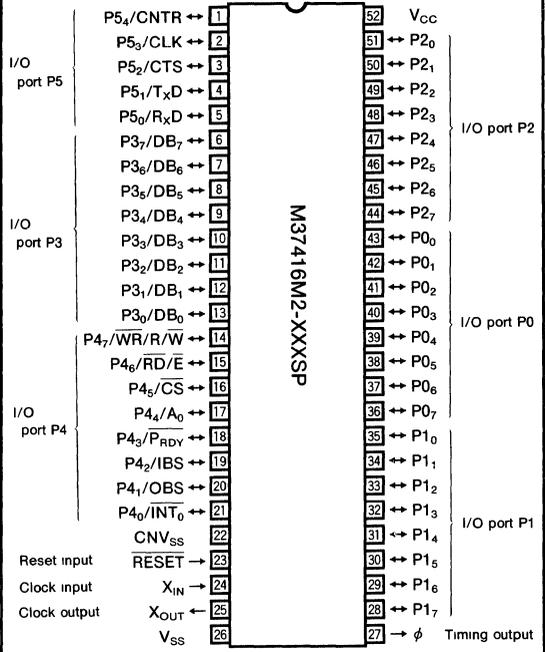
FEATURES

- Number of basic instructions 69
- Memory size ROM 4096 bytes
RAM 128 bytes
- Instruction execution time
..... 1 μ s (minimum instructions at 8MHz frequency)
- Single power supply $f(X_{IN})=8\text{MHz}$ $5V \pm 10\%$
- Power dissipation
normal operation mode (at 8MHz frequency) 50mW
- Subroutine nesting 64 levels (max.)
- Interrupt 9
- 8-bit timer 2
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P5) 45
- UART (full duplex) 1
- Master CPU bus interface 1 byte
- Comparator 8-channel
- Key on wake up 8

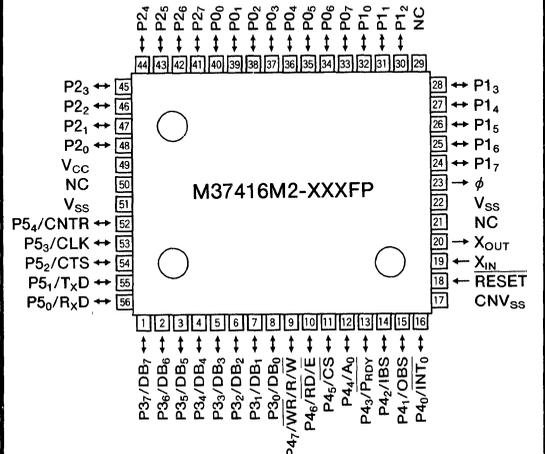
APPLICATION

Office automation equipment
Key pad, Key board

PIN CONFIGURATION (TOP VIEW)



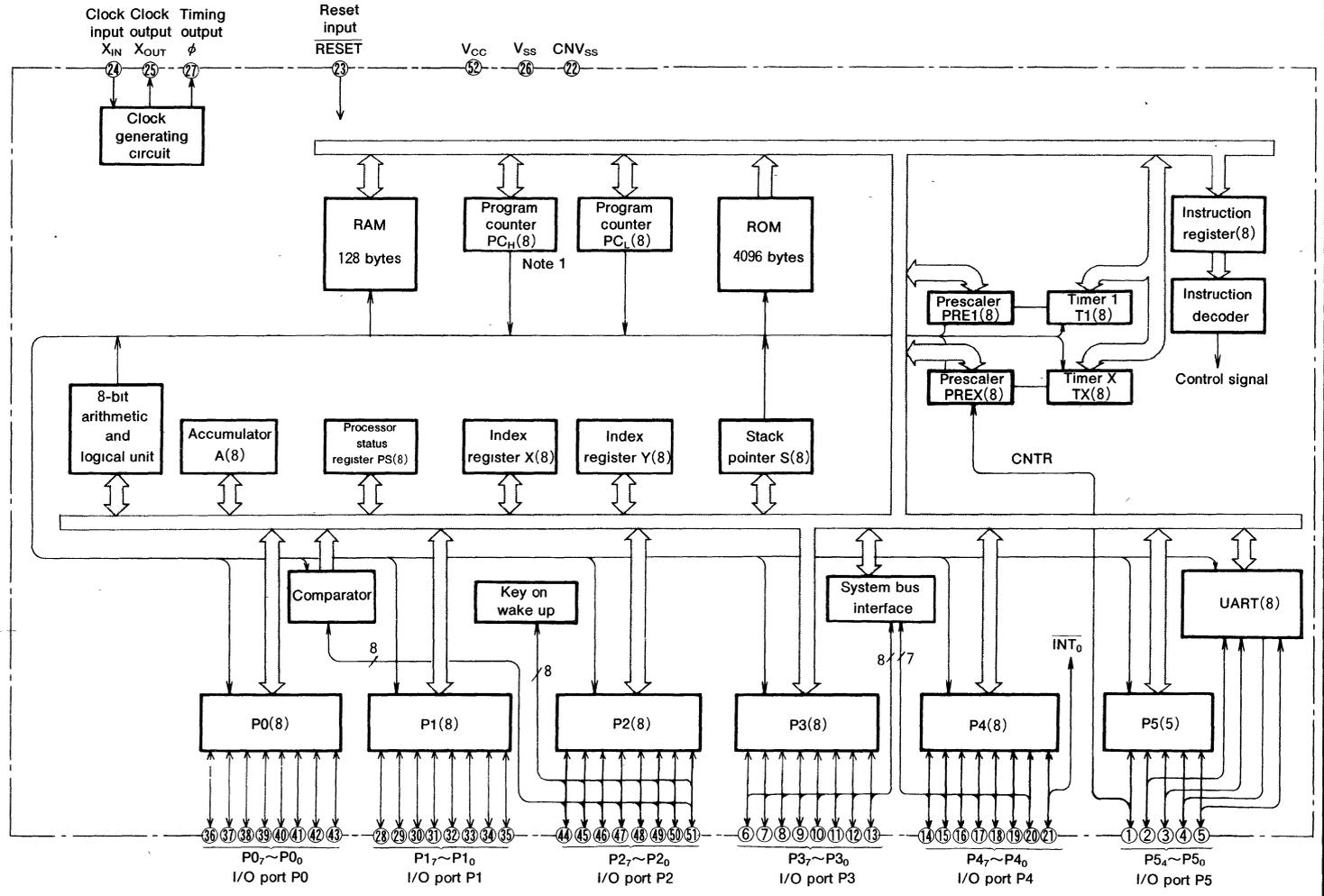
Outline 52P4B



Outline 56P6N

NC : No connection

M37416M2-XXXSP BLOCK DIAGRAM



Note 1 : Program counter PC_H is only 5 bits long



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MITSUBISHI MICROCOMPUTERS
M37416M2-XXXSP/FP

MITSUBISHI MICROCOMPUTERS
M37416M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37416M2-XXXSP

Parameter		Functions	
Number of basic instructions		69	
Instruction execution time		1 μ s (minimum instructions, at 8MHz frequency)	
Clock frequency		8MHz	
Memory size	ROM	4096 bytes	
	RAM	128 bytes	
Input/Output ports	P0 ₀ ~P0 ₇	I/O	8-bitX1
	P1 ₀ ~P1 ₇	I/O	8-bitX1
	P2 ₀ ~P2 ₇	I/O	8-bitX1 (common with comparator input and key on wake up)
	P3 ₀ ~P3 ₇	I/O	8-bitX1 (common with data bus of system bus interface)
	P4 ₀ ~P4 ₇	I/O	8-bitX1 (common with control ports of system bus interface and INT ₀)
	P5 ₀ ~P5 ₄	I/O	5-bitX1 (common with UART)
UART		1 with programmable baud rate generator	
Timers		8-bitX2 (with 8-bit prescaler)	
Comparator		8-bitX1 (port P2) Built-in 3-bit DAC (can be used as variable V _{TH} input port)	
Subroutine nesting		64 levels (max)	
Interrupt		2 external, 6 internal, 1 software interrupts	
System bus interface buffer		1-byte (separate input and output buffers)	
Clock generating circuit		Built-in (Ceramic or quartz crystal oscillator)	
Supply voltage		5V \pm 10%	
Power dissipation	at operation		50mW
	at wait mode		5mW
	at stop mode	T _a =25 $^{\circ}$ C	0.05mW
		T _a =70 $^{\circ}$ C	0.5mW
Input/Output characteristics	Input/Output voltage		V _{SS} -0.3~V _{CC} +0.3
	Output current		\pm 5mA (max)
Operating temperature range		-10~70 $^{\circ}$ C	
Device structure		CMOS silicon gate	
Package	M37416M2-XXXSP		52-pin shrink plastic molded DIP
	M37416M2-XXXFP		56-pin plastic molded QFP

MITSUBISHI MICROCOMPUTERS
M37416M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is usually connected to V _{SS} .
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an I/O pin for the timer X
$\overline{\text{INT}}_1$	Interrupt input	Input	This is the highest order interrupt input pin
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS output
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0.
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as port P0. Analog input of comparator or key on wake up function can be selected with a program.
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same function as port P0. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
P4 ₀ ~P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same function as port P0. P4 ₁ ~P4 ₇ change to a control bus for the master CPU when slave mode is selected with a program. P4 ₀ can be used as external interrupt input pin.
P5 ₀ ~P5 ₄	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as port P0. UART function, CNTR input and timer output can be selected with a program

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37416 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

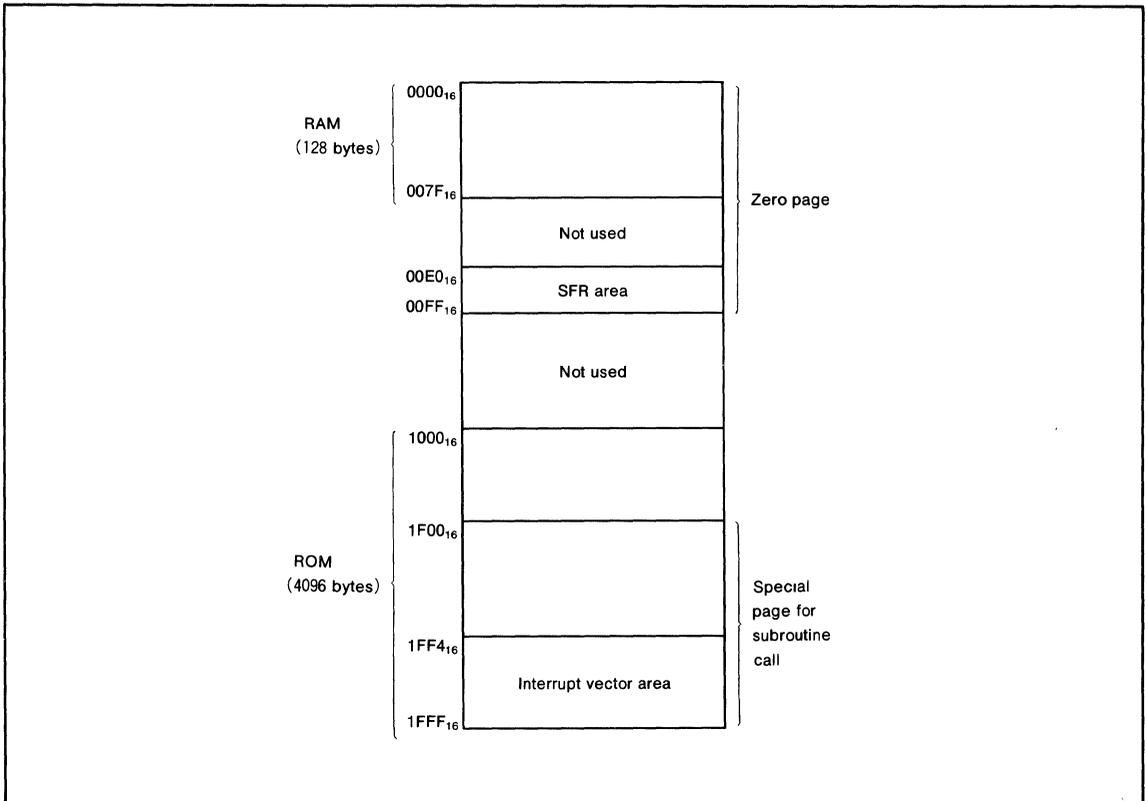


Fig. 1 Memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

00E0 ₁₆	Port P0	00F0 ₁₆	Data bus receive buffer register
00E1 ₁₆	Port P0 directional register	00F1 ₁₆	Data bus buffer status register
00E2 ₁₆	Port P1	00F2 ₁₆	Data bus buffer control register
00E3 ₁₆	Port P1 directional register	00F3 ₁₆	UART transmit buffer register
00E4 ₁₆	Port P2	00F4 ₁₆	UART receive buffer register
00E5 ₁₆	Port P2 directional register	00F5 ₁₆	UART status register
00E6 ₁₆	Port P3	00F6 ₁₆	UART mode register
00E7 ₁₆	Port P3 directional register	00F7 ₁₆	UART control register
00E8 ₁₆	Port P4	00F8 ₁₆	Driver for UART baud rate generator
00E9 ₁₆	Port P4 directional register	00F9 ₁₆	
00EA ₁₆	Port P5	00FA ₁₆	Prescaler 1
00EB ₁₆	Port P5 directional register	00FB ₁₆	Timer 1
00EC ₁₆	Comparator control register	00FC ₁₆	Timer X prescaler
00ED ₁₆	Comparator data register	00FD ₁₆	Timer X
00EE ₁₆	Interrupt request distinguish register	00FE ₁₆	Interrupt control register
00EF ₁₆	Data bus transmit buffer register	00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

INTERRUPTS

Interrupts can be caused by 9 different events. Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed interrupt inhibit flag I is set, and the program jumps to the address specified in the vector table. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit.

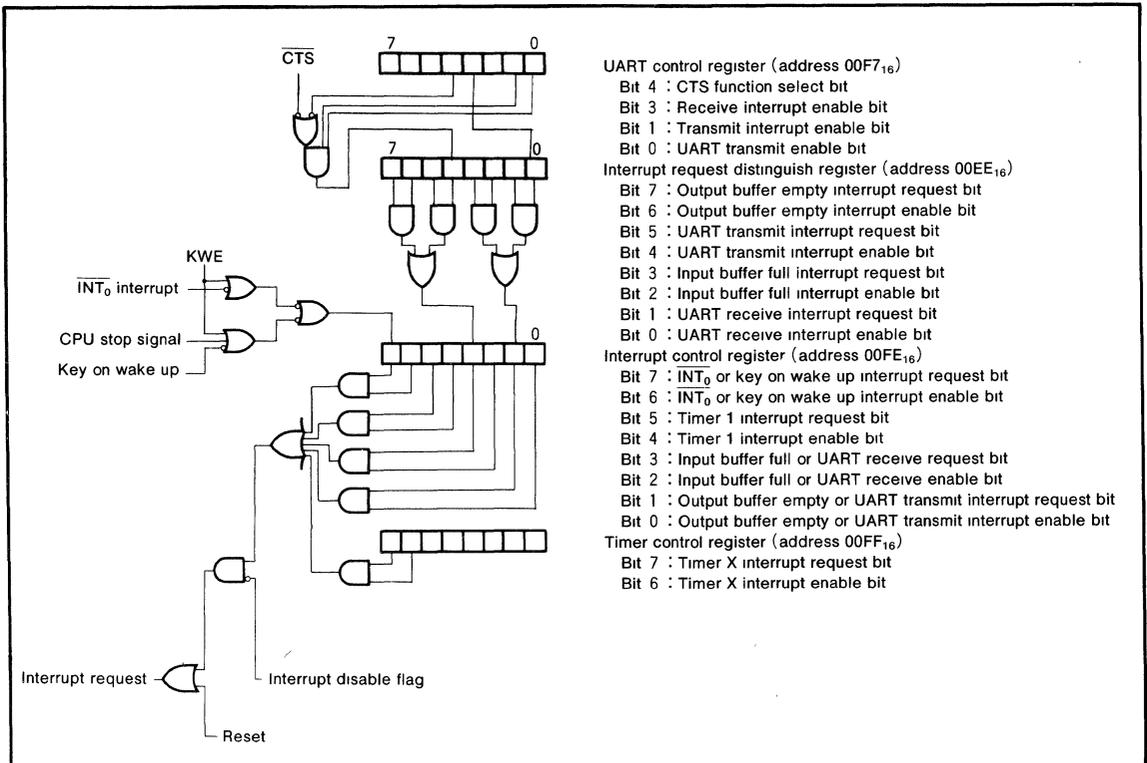
Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit bit is "0". There are two interrupt (three for UART transmit and UART receive) the interrupt becomes enable when both enable bits are "0".

The value of bit 3 of the data bus buffer control register (address 00F2₁₆) determines whether the interrupt is from INT₀ or from key on wake up. Only INT₀ interrupt is effective when this bit is "1" at power down condition by STP or WIT instruction. When this bit is "1", interrupt is caused by inputting "L" level to any port P2 using input mode. The value of bit 1 and bit 3 of interrupt request distinguish register (address 00EE₁₆) determine whether the interrupt is

from input buffer full or from UART receive. When bit 3 is "1", the interrupt is from the input buffer full interrupt, and bit 1 is "1", the interrupt is from UART receive. Also bit 5 and bit 7 of interrupt request distinguish register determine whether the interrupt is from output buffer empty or from UART transmit. When bit 7 is "1", the interrupt is from output buffer empty and when bit 5 is "1", the interrupt is from UART transmit.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
RESET	1	FFF ₁₆ , FFF ₁₆
INT ₀ or key on wake up	2	FFD ₁₆ , FFC ₁₆
Timer X	3	FFB ₁₆ , FFA ₁₆
Timer 1	4	FF9 ₁₆ , FF8 ₁₆
Input bus buffer full or UART receive	5	FF7 ₁₆ , FF6 ₁₆
Output bus buffer full or UART transmit	6	FF5 ₁₆ , FF4 ₁₆



- UART control register (address 00F7₁₆)
 - Bit 4 : CTS function select bit
 - Bit 3 : Receive interrupt enable bit
 - Bit 1 : Transmit interrupt enable bit
 - Bit 0 : UART transmit enable bit
- Interrupt request distinguish register (address 00EE₁₆)
 - Bit 7 : Output buffer empty interrupt request bit
 - Bit 6 : Output buffer empty interrupt enable bit
 - Bit 5 : UART transmit interrupt request bit
 - Bit 4 : UART transmit interrupt enable bit
 - Bit 3 : Input buffer full interrupt request bit
 - Bit 2 : Input buffer full interrupt enable bit
 - Bit 1 : UART receive interrupt request bit
 - Bit 0 : UART receive interrupt enable bit
- Interrupt control register (address 00FE₁₆)
 - Bit 7 : INT₀ or key on wake up interrupt request bit
 - Bit 6 : INT₀ or key on wake up interrupt enable bit
 - Bit 5 : Timer 1 interrupt request bit
 - Bit 4 : Timer 1 interrupt enable bit
 - Bit 3 : Input buffer full or UART receive request bit
 - Bit 2 : Input buffer full or UART receive enable bit
 - Bit 1 : Output buffer empty or UART transmit interrupt request bit
 - Bit 0 : Output buffer empty or UART transmit interrupt enable bit
- Timer control register (address 00FF₁₆)
 - Bit 7 : Timer X interrupt request bit
 - Bit 6 : Timer X interrupt enable bit

Fig. 3 Interrupt control

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

The four modes of timer X as follows:

(1) Timer mode [00]

In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]

In this mode, the polarity of the P5₄/CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]

This mode operates in the same manner as the timer mode except the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]

This mode measures the pulse width (between lows) input to the P5₄/CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF₁₆ and 01₁₆, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

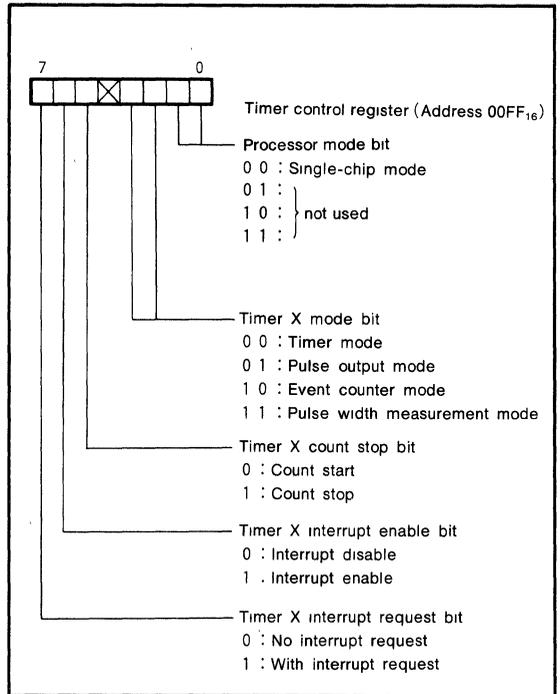


Fig. 5 Structure of timer control register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

BUS INTERFACE

The M37416M2-XXXSP is equipped with a bus interface that is functionally similar to the M5L8041-XXXSP. Its operation can be controlled with control signals from the master CPU (slave mode).

The M37416M2-XXXSP bus interface can be connected directly to either a R/W type CPU or separate RD, WR type CPU. Figure 7 shows a block diagram of the bus interface function.

Slave mode is selected with data bus buffer control register (address 00F2₁₆) bit 0 and 1 as shown in Figure 6.

An input buffer full interrupt occurs when data is received from the master CPU and an output buffer empty interrupt occurs when data is read by the master CPU.

In slave mode, ports P3₀~P3₇ become a tri-state data bus used to transfer data, commands, and status to and from the master CPU.

Furthermore, ports P4₄~P4₇ become master CPU control signal input pins and P4₁~P4₃ becomes a slave status output pins.

[Data bus buffer status register] DBBSTS

This is an 8-bit register. Bits 0, 1, and 3 are read-only bits indicating the status of the data bus buffer. Bits 2, 4, 5, 6, and 7 are read/write enabled user-definable flags that can be set with a program. The host CPU can only read these flags by setting the A0 pin to "H".

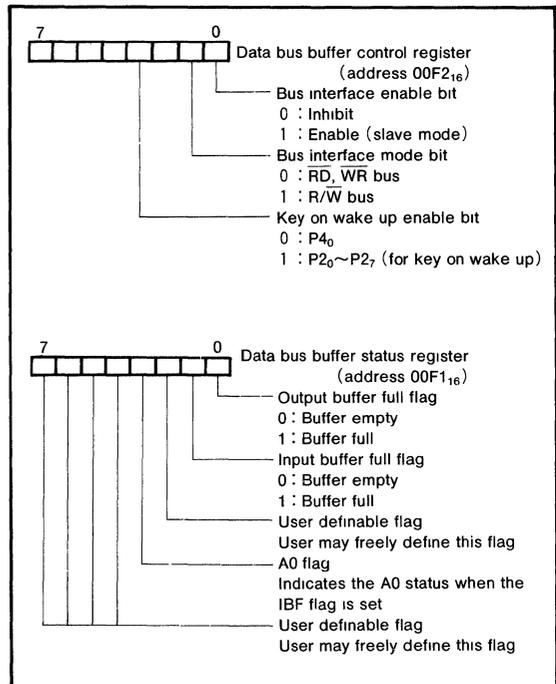


Fig. 6 Structure of bus interface relation registers

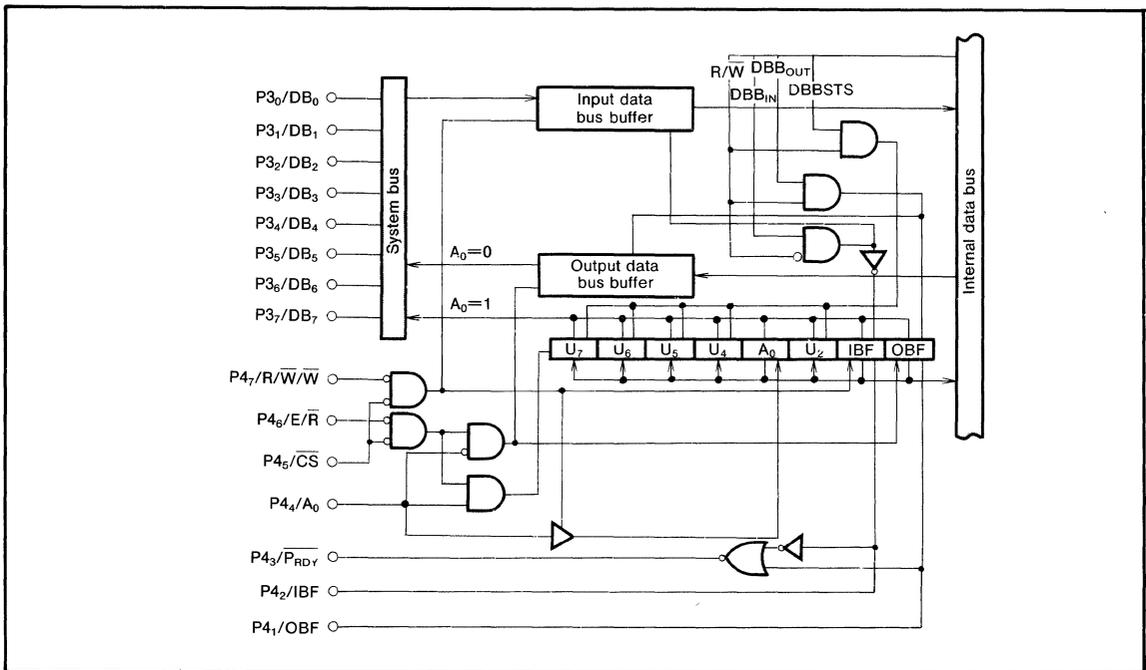


Fig. 7 Bus interface circuit diagram

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

• **Output buffer full flag OBF**

This flag is set when data is written in the output data bus buffer and cleared when the host CPU reads the data in the output data bus buffer. It is initialized to "1" at reset and cleared to "0" when the slave mode is selected with the bus interface enable bit set.

• **input buffer full flag IBF**

This flag is set when the host CPU writes data in the input data bus buffer and cleared when the slave CPU reads the data in the input data bus buffer. This bit is initialized to "0" at reset.

Execute the dummy write instruction to the input data bus buffer to clear this flag from the slave CPU side. The contents of input data bus buffer is not change because it is read only register.

A₀ flag

The level of the A₀ pin is latched when the host CPU writes data in the input data bus buffer.

[Input data bus buffer] DBBIN

Data on the data bus is latched in DBBIN when there is a write request from the host CPU. The data in DBBIN can be read from the data bus buffer register (SFR address 00F0₁₆).

[Output data bus buffer] DBBOUT

Data is written in DBBOUT by writing data in data bus buffer register (SFR address 00EF₁₆). The data in DBBOUT is output to the data bus (P5) when the host CPU issues a read request with setting the A₀ pin to "L".

Table 2. Control I/O pin functions when bus interface function is selected

Pin	Name	Bus interface mode bit	Input/Output	Function
P4 ₁	OBF	—	Output	Status output OBF signal is output
P4 ₂	IBF	—	Output	Status output IBF signal is output
P4 ₃	$\overline{P_{RDY}}$	—	Output	Status output The NOR of OBF and IBE is output.
P4 ₄	A ₀	—	Input	Address input Used to select between DBBSTS and DBBOUT during host CPU read Also used to identify commands and data during write
P4 ₅	CS	—	Input	Chip select input Used to select the data bus buffer Select when "L"
P4 ₆	\overline{R}	0	Input	Timing signal used by the host CPU to read data from the data bus buffer
	E	1	Input	Inputs a timing signal E or inverse of ϕ
P4 ₇	\overline{W}	0	Input	Timing signal used by the host CPU to write data to the data bus buffer
	R/ \overline{W}	1	Input	Input R/ \overline{W} signal used to control the data transfer direction When this signal is "L", data bus buffer write is synchronized with the E signal When it is "H", data bus buffer read is synchronized with the E signal

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

[Transmit operation]

When the send data is written to the transmit buffer register, the start bit, the parity bit, and the stop bit are added to the data, which is transferred to the transmit shift register. The transmit shift register begins shift when it becomes enable for transmission, sending the serial data to TxD pin. For the description of the transmit enable state, see Table 3. In the transmit enable state, each time transmission of the stop bit of the serial data being transmitted has been completed, it is checked whether the next data has been written to the transmit buffer register. If the data is found written, transmission of the next data begins. If the data is found not written, TxD pin is held at "H" until the next transmit data is written, setting the transmitter empty flag. When the transmit enable state is cleared during transmission, the transmission is stopped after completing the transmission of the transmit data so far written to the transmit buffer register.

When the transmitter ready flag (bit 0 of the UART status register) is "1", it indicates that the transmit buffer is ready

for writing data. The immediately preceding data is transferred from the transmit buffer register to the transmit shift register. Every time the start bit is output from TxD pin, this flag is set. Every time the transmitter ready flag is set, the UART transmit interrupt request bit (bit 5 of the interrupt request distinguish register) is set. An interrupt is acknowledged when two UART transmit interrupt enable bits (bit 1 of the UART control register, and bit 0 of interrupt control register) are all "1" and the interrupt disable flag I is "0". Interrupt request bit (bit 1 of interrupt control register) is reset when the UART transmit interrupt is accepted. Note that an interrupt occurs only in the transmit ready state.

Bit 6 of the UART control register initializes the UART transmit side. When this bit "0", the transmit side is in the initial state.

Table 3. Bit and pin status when transmission is ready

TE	CTSE	$\overline{\text{CTS}}$	TE : UART transmit enable bit
1	0	X	CTSE : $\overline{\text{CTS}}$ pin function selection bit
	1	L	$\overline{\text{CTS}}$: $\overline{\text{CTS}}$ pin input level

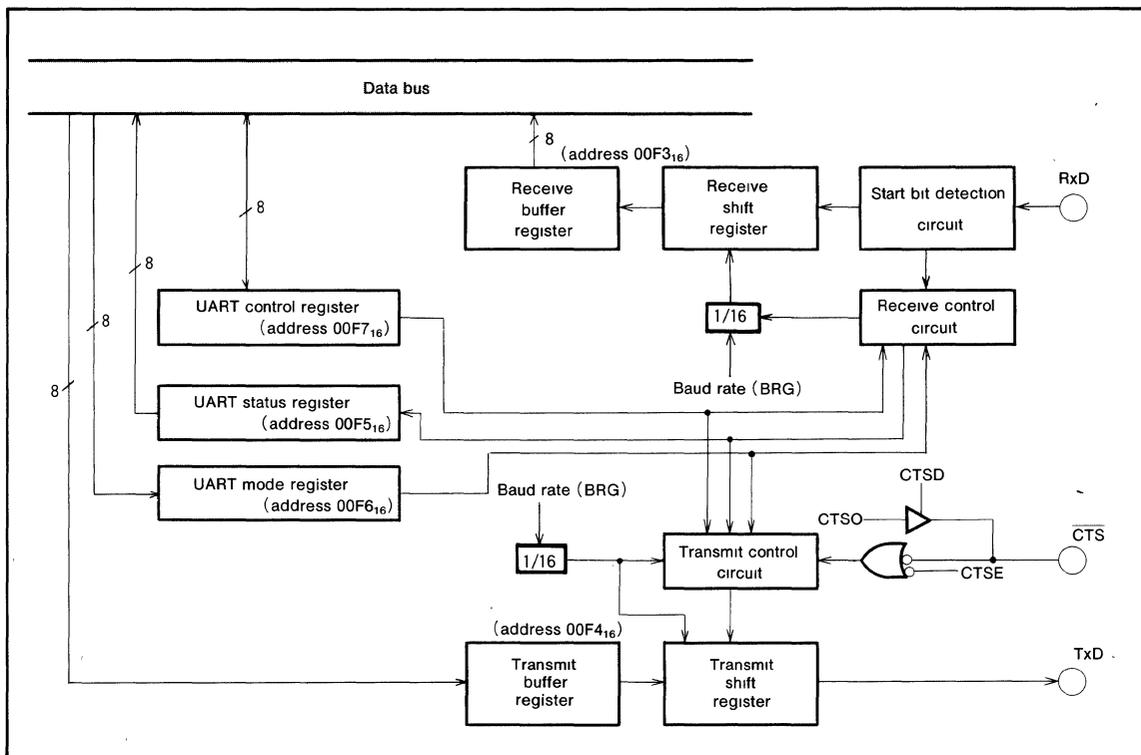


Fig. 8 UART block diagram

UART

The M37416M2-XXXSP contains one channel UART. It has three pins (TxD (transmit output), RxD (receive input) and CTS (clear to send)). The three pins RxD, TxD and CTS are common with P5₀, P5₁ and P5₂ respectively. P5₀~P5₂ are selected to UART function pins when UART enable bit (bit 6 of UART mode register) to "1". And it also has a CLK pin (the input pin of the external clock for baud rate generation). This pin is selected as CLK function when the synchronous clock for baud rate generating synchronous clock select bit (bit 5 of UART mode register) is set to "1". An interrupt can be generated at receive and transmit independently.

[Receive operation]

Setting the receive enable bit (bit 2 of the UART control register) to "1" puts the system in the receive ready state. When there is no input of receive data, "H" is input to RxD pin. When the falling edge is input to RxD pin and "L" input is detected twice consecutively by sampling with the clock having a frequency 16 times the baud rate, the start bit is triggered. Then, sampling is performed three times in the middle of the start bit. When "L" is detected twice or more, the receive operation begins, capturing the data bits into the receive shift register. If "L" has not been detected twice or more, start bit detection begins again. When the data bits and parity bit have been captured into the receive shift register and the stop bit is detected, the receive data is transferred from the receive shift register to the receive buffer register, setting the receiver ready flag (bit 1 of the UART status register). If a parity error occurred, the parity error flag is set. The framing error flag is set when the first stop bit is found "L". If the previous data has not been read out of the receive buffer register, the overrun error flag is set, clearing the previous data. Execute the dummy write instruction to the receive buffer register to clear the receiver ready flag. The contents of receive buffer register is not changed because it is read only register. Each error flag can be reset by writing "1" to the error flag reset bit (bit 7 of the UART control register). Any of these errors does not affect the receive operation. The data bit, the parity bit, and the stop bit are sampled three times in the middle of them each. When "L" or "H" is detected twice or more, "0" or "1" is determined respectively.

Each time a receive operation has been completed, setting the receiver ready flag, the UART receive interrupt request bit (bit 1 of the interrupt request distinguish register) is set. An interrupt is acknowledged when the two UART receive interrupt enable bits (bit 2 of interrupt control register and bit 3 of UART control register) are all "1" and the interrupt disable flag 1 is "0". The UART receive interrupt request bit which is in interrupt control register (address 00FE₁₆) is reset when a UART receive interrupt is acknowledged. Setting the receive enable bit (bit 2 of the UART control

register) to "0" puts the system in the receive stopped state. At this time, the receiver ready flag is "0" (ready), the receive shift register is in the stopped state, and the start bit detection is stopped.

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[UART divider for baud rate generator]

This is an 8-bit programmable divider which generates the baud rate for the UARTI receive or transmit operation.

When the setting value is N_{BR} (0 to 255), the divide ratio becomes $1/(N_{BR} + 1)$. There are three count sources; X_{IN} clock divided by 2, X_{IN} clock divided by 32, and the external clock. Choose sources by bits 4 and 5 of the UARTI mode register. Table 4 shows the baud rate calculation and example for each bit combination.

When the external clock is used, the frequency of the input clock must be below 1.6 MHz. Writing to the baud rate generating divider must be performed when bits 2 and 6 of the UARTI control register are both "0".

Table 4. Baud rate calculation and example

EX	BR	Calculation	Count source	Baud rate
0	0	$\text{baud rate (bps)} = \frac{f(X_{IN})}{32(N_{BR} + 1)}$	$f(X_{IN}) = 8.0 \text{ MHz}$	250000 bps
0	1	$\text{baud rate (bps)} = \frac{f(X_{IN})}{512(N_{BR} + 1)}$	$f(X_{IN}) = 7.3728 \text{ MHz}$	4800 bps
1	X	$\text{baud rate (bps)} = \frac{f(\text{CLK})}{16(N_{BR} + 1)}$	$f(X_{IN}) = 1.536 \text{ MHz}$	9600 bps

EX : Clock selection bit for baud rate generator
BR : Divide ratio selection bit for baud rate generator

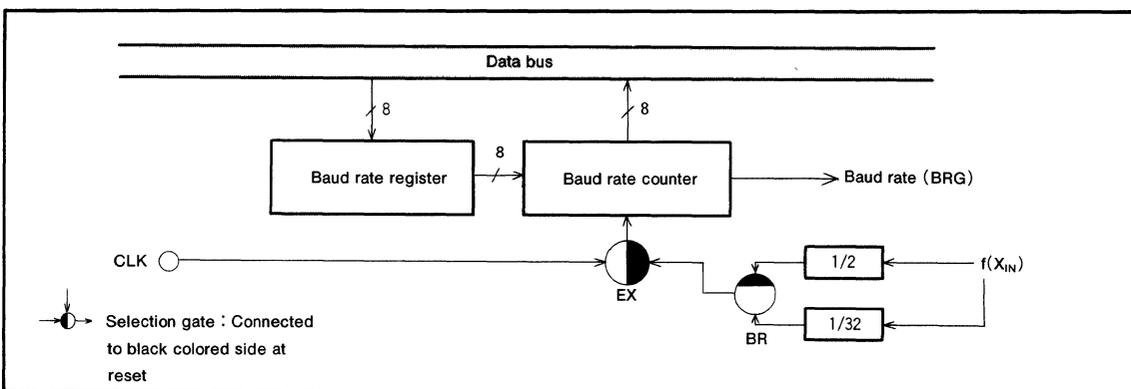


Fig. 9 Baud rate generating circuit

[$\overline{\text{CTS}}$ pin]

The $\overline{\text{CTS}}$ pin can be used as the 1-bit I/O port when bit 4 of the UART control register is "0". In this case, the input/output direction can be determined by bit 7 of the UART mode register and the output data can be set by bit 5 of the UART control register. Additionally, the input level can be known by bit 7 of the UART status register.

[UART mode register]

This register except the bit 6 is write-only register and cannot be read out. Use the LDM instruction to write to this register.

- **Parity enable bit: PEN**

Setting this bit to "1" adds a parity bit to the transmit data. In a receive operation, this bit is used for parity evaluation.

- **Parity select bit: EVN**

This bit specifies the parity bit to be generated in a transmit operation and the parity bit to be evaluated in a receive operation. Depending on the content of this bit, the number of 1's in data is made even or odd.

- **Character length select bit: CHL**

This bit specifies the character length of data.

- **Stop bit length select bit: ST**

This bit specifies the stop bit length.

- **Baud rate generating prescaler divide ratio select bit: BR**

When this bit is "0", the signal obtained by dividing X_{IN} clock by 2 becomes the count source of the baud rate divider. When this bit is "1", the signal is obtained by dividing the clock by 32.

- **Baud rate generating synchronous clock selection bit: EX**

This bit specifies baud rate synchronous clock. When this bit is "1", external clock is input from the clock pin.

- **UART enable bit: UARTE**

$P5_0 \sim P5_2$ is selected UART function when this bit is "1".

- **$\overline{\text{CTS}}$ pin I/O select bit: CTSD**

When this bit is "0", the $\overline{\text{CTS}}$ pin is the input pin.

When this bit is "1", the pin is the output pin. To use the $\overline{\text{CTS}}$ pin as the $\overline{\text{CTS}}$ input, set "0".

[UART control register]

- **Transmit enable bit: TE**

Setting this bit to "1" enables a transmit operation.

- **Transmit interrupt enable bit: TIE**

When this bit is "1", the interrupt in a transmit operation is enabled.

- **Receive enable bit: RE**

Setting this bit to "1" enables a receive operation.

- **Receive interrupt enable bit: RIE**

When this bit is "1", the interrupt in a receive operation is enabled.

- **$\overline{\text{CTS}}$ pin function select bit: CTSE**

When this bit is "1", the $\overline{\text{CTS}}$ pin becomes the $\overline{\text{CTS}}$ input.

- **$\overline{\text{CTS}}$ output data select bit: CTSO**

When this bit is "0", "L" is output. When it is "1", "H" is output.

- **Transmit side initialize bit: MR**

When this bit is "0", the transmit side is initialized.

- **Error flag reset select bit: ERST**

Setting this bit to "1" resets all error flags. When this bit is read, "0" is always read.

[UART status register]

- **Transmitter ready flag: TxRDY**

When this flag is "1", it indicates that the transmit buffer register is empty and ready for writing transmit data.

- **Receiver ready flag: RxRDY**

When this flag is "1", it indicates that the receive buffer register is holding receive data. When the receive buffer register is read, it is cleared.

- **Transmitter empty flag: TEMP**

When this flag is "1", it indicates that neither the transmit shift register nor the transmit buffer register hold the data to be transmitted.

- **Parity error flag: PE**

This bit is set to "1" when the parity of the received data is different from the parity which was set.

- **Overrun error flag: OR**

When this flag is "1", it indicates that, before the data in the receive buffer register is read, the next data is transferred from the receive shift register to the receive buffer register and the previous data is lost.

- **Framing error flag: FE**

This flag is set to "1" when the stop bit is found "L" when data is transferred from the receive shift register to the receive buffer register.

- **$\overline{\text{CTS}}$ pin input level flag: $\overline{\text{CTS}}$**

When the input level of the $\overline{\text{CTS}}$ pin is "L", "0" is read, when it is "H", "1" is read.

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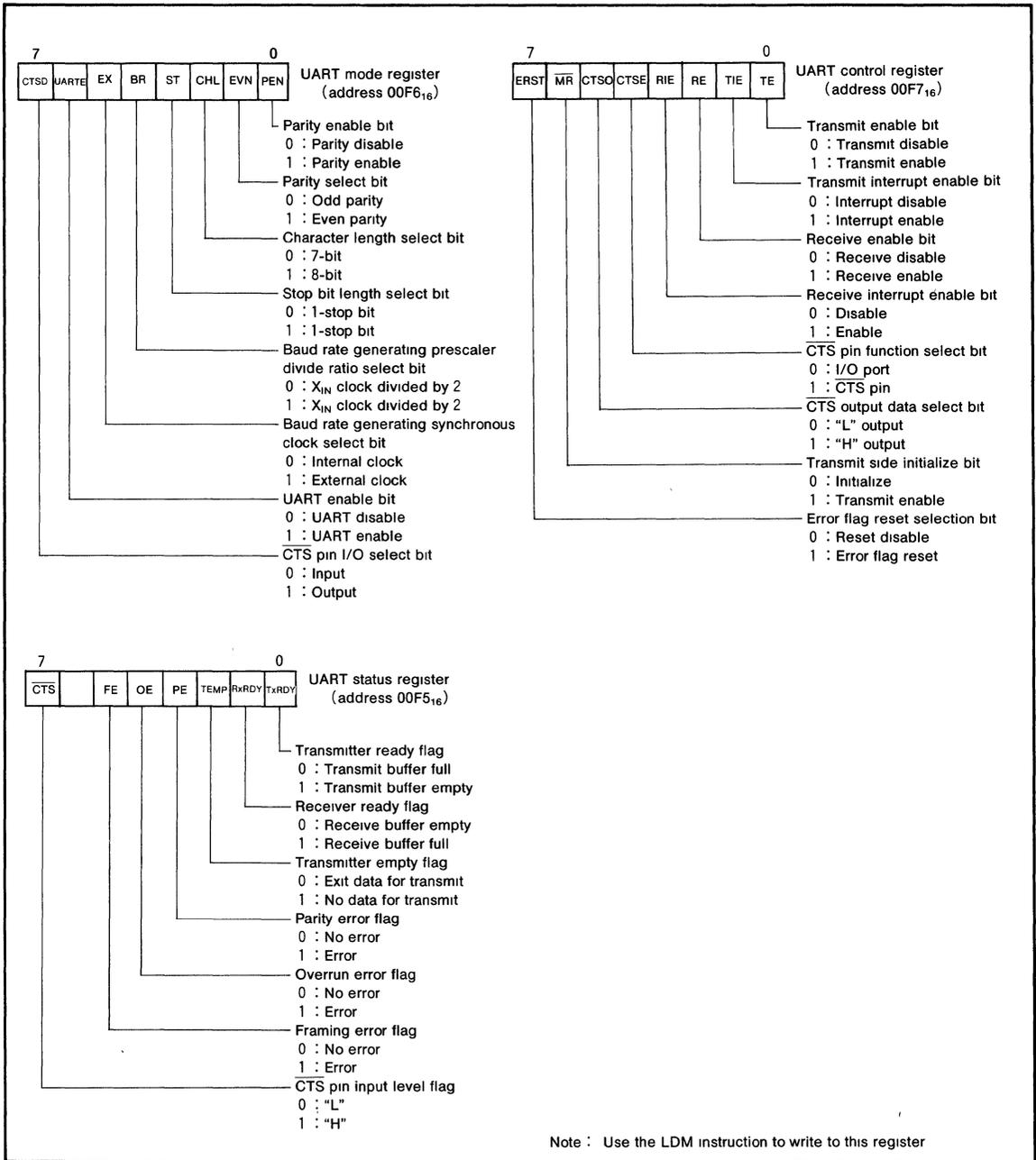


Fig. 10 Structure of registers related to UART

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COMPARATOR CIRCUIT

The comparator circuit is shown in Figure 11. The comparator circuit consists of the switch tree, ladder resistor, comparator, comparator control circuit, comparator control register (address 00EC₁₆), comparator data register (address 00FD₁₆), and analog signal input pins, P₂₀~P₂₇.

These analog input pins are common with the digital input/output terminal to the data bus.

The 3-bit comparator register can generate 1/8V_{CC}-step internal analog voltage, based on the settings of bits 0 to 2.

Table 5 gives the relation between the descriptions of comparator register bits 0 to 2 and the generated internal analog voltage. The comparator result of the analog input voltage and the internal analog voltage is stored in the comparator data register.

The digital value corresponding to the internal analog voltage to be compared is written in the comparator control register (address 00FC₁₆), bits 0 to 2. The voltage comparison starts as soon as the writing is completed. 4-cycle (required for comparing) later, the result of comparison is stored in the comparator data register. Each bit of comparator data register is "1" when analog input voltage > internal analog voltage and "0" when analog input voltage < internal analog voltage.

When voltage is compared to by setting bits 0 to 2 of the comparator register "0", each bit of the comparator data register becomes "1" regardless of the analog input voltage. The reference voltage is generated for 4 cycles, when ladder resistor is ON. The ladder resistor is OFF for current power save, when the comparator does not operate.

Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during comparison.

Table 5. Relationship between the contents of comparator register and internal voltage

Comparator register			Internal analog voltage
bit 2	bit 1	bit 0	
0	0	1	1/8V _{CC} -1/16V _{CC}
0	1	0	2/8V _{CC} -1/16V _{CC}
0	1	1	3/8V _{CC} -1/16V _{CC}
1	0	0	4/8V _{CC} -1/16V _{CC}
1	0	1	5/8V _{CC} -1/16V _{CC}
1	1	0	6/8V _{CC} -1/16V _{CC}
1	1	1	7/8V _{CC} -1/16V _{CC}

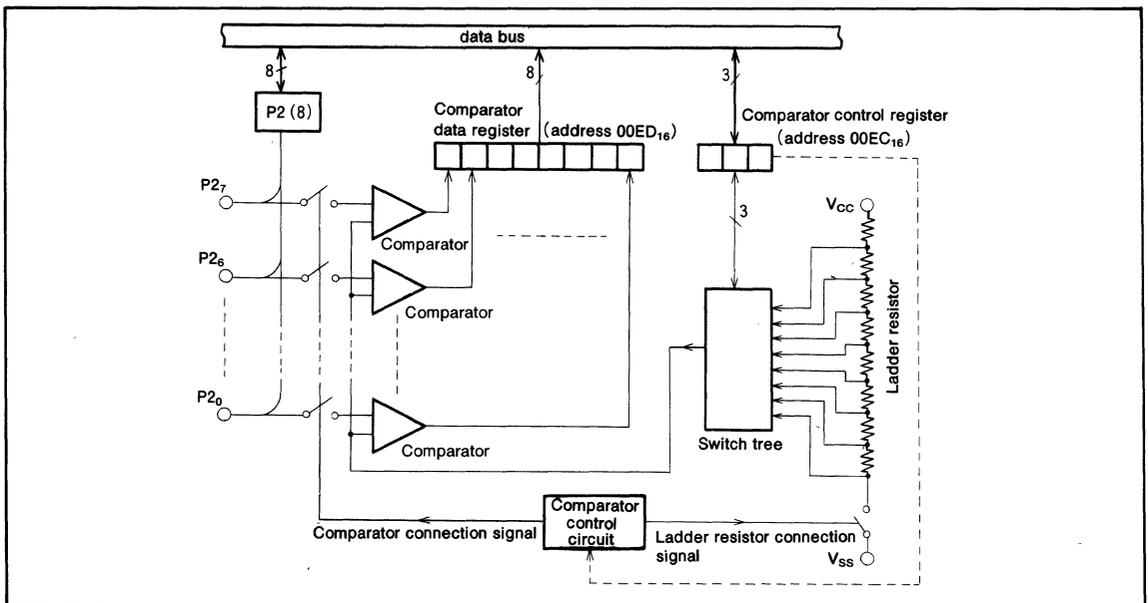


Fig. 11 Comparator circuit

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KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P2 has a "L" level applied, after bit 3 of the data bus buffer control register (KWE) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. As shown in Figure 12, a key matrix can be connected to port P2 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the \overline{INT}_0 interrupt. When KWE is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and \overline{INT}_0 are invalid.

In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and KWE is "1", all of port P2 must be input "H".

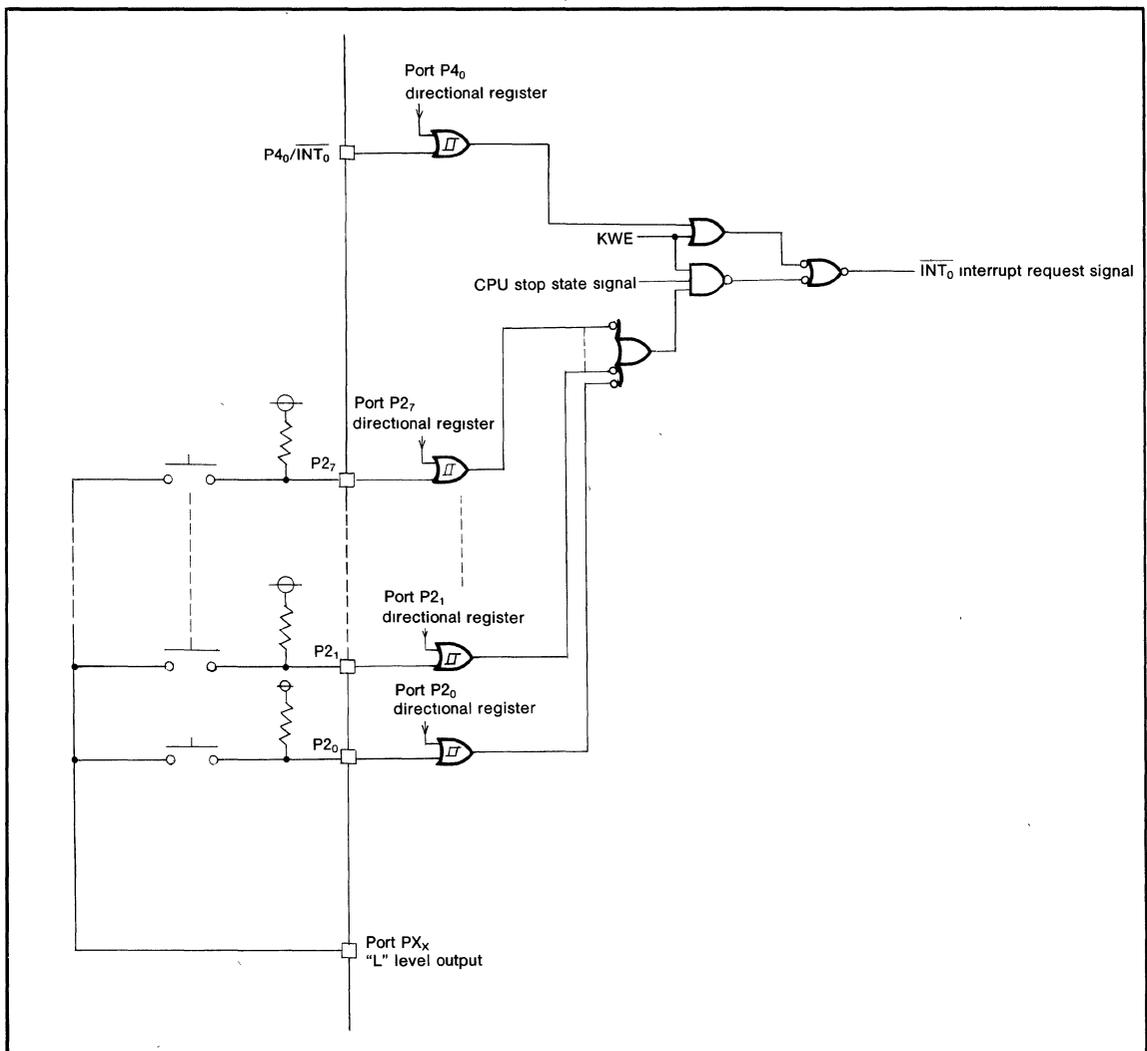


Fig. 12 Block diagram of port P2 and P3₂, and example of wired at used key on wake up

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RESET CIRCUIT

The M37416M2-XXXSP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $1FFF_{16}$ as the high order address and the content of the address $1FFE_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for more than $2\mu\text{s}$ while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 14. An example of the reset circuit is shown in Figure 13. When the power on reset is used, the $\overline{\text{RESET}}$ pin must be held "L" until the oscillation of $X_{\text{IN}}-X_{\text{OUT}}$ becomes stable.

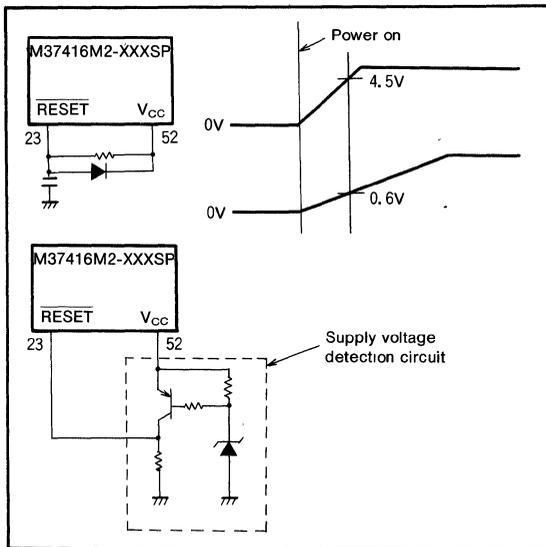


Fig. 13 Example of reset circuit

	Address	
(1) Port P0 directional register	(E1 ₁₆)...	00 ₁₆
(2) Port P1 directional register	(E3 ₁₆)...	00 ₁₆
(3) Port P2 directional register	(E5 ₁₆)...	00 ₁₆
(4) Port P3 directional register	(E7 ₁₆)...	00 ₁₆
(5) Port P4 directional register	(E9 ₁₆)...	00 ₁₆
(6) Port P5 directional register	(EB ₁₆)...	— — — 0 0 0 0
(7) Comparator control register	(EC ₁₆)...	00 ₁₆
(8) Interrupt request distinguish register	(EE ₁₆)...	00 ₁₆
(9) Data bus buffer status register	(F1 ₁₆)...	× × × × × × 0 1
(10) Data bus buffer control register	(F2 ₁₆)...	0 0 0 0 × 0 0 0
(11) UART mode register	(F6 ₁₆)...	00 ₁₆
(12) UART control register	(F7 ₁₆)...	× 0 0 0 0 0 0 0
(13) Prescaler X	(FC ₁₆)...	FF ₁₆
(14) Timer X	(FD ₁₆)...	01 ₁₆
(15) Interrupt control register	(FE ₁₆)...	00 ₁₆
(16) Timer control register	(FF ₁₆)...	0 0 0 × 0 0 0 0
(17) Interrupt disable flag for processor status register	(PS)...	1
(18) Program counter	(PC _H)...	Contents of address 1FFF ₁₆
	(PC _L)...	Contents of address 1FFE ₁₆

Since the contents both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values
Note : * means mask option

Fig. 14 Internal state of microcomputer at reset

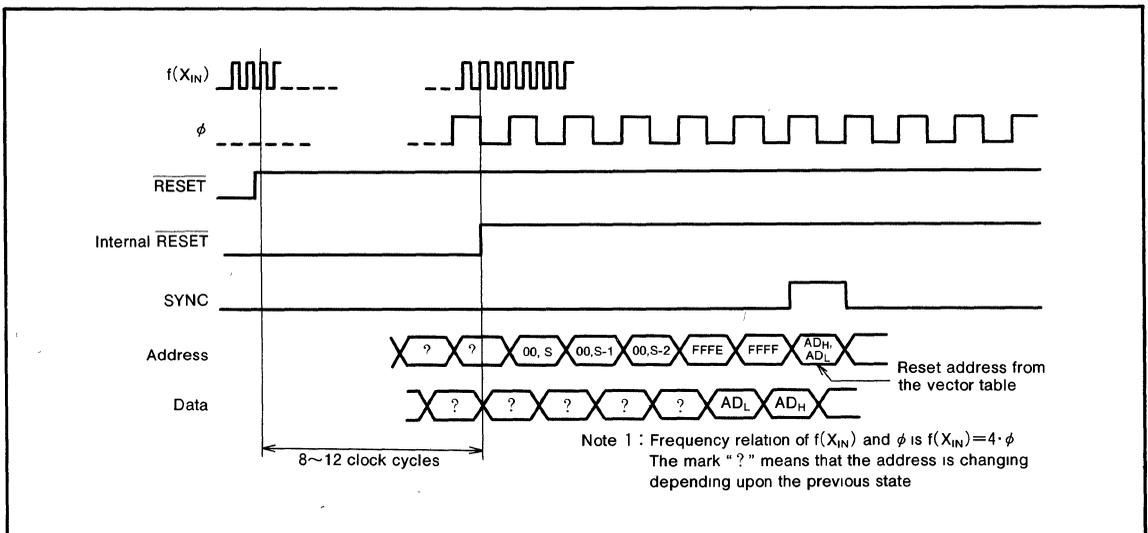


Fig. 15 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

(2) Port P1

Port P1 has the same function as port P0. The I/O level is TTL compatible.

(3) Port P2

Port P2 has the same function as P0. Following the execution of STP or WIT instruction, P2 can be used to generate the "wake up mode". This mode is used to bring the microcomputer back in its normal operating mode after being in the power-down mode. Also this port has comparator function. For more details, see the comparator information.

(4) Port P3

This is an 8-bit I/O port with function similar to port P0. When slave mode is selected with a program, all ports change to the data bus for the master CPU. In this case, port input/output is unaffected by the directional register. The I/O level is TTL compatible.

(5) Port P4

This is an 8-bit input/output port with function similar to port P0. When slave mode is selected with a program, ports $P4_1 \sim P4_7$ change to the control bus for the bus interface function. In this case, port input/output is unaffected by the directional register.

Port $P4_0$ are shared with the external interrupt input pin (\overline{INT}_0). The \overline{INT}_0 interrupt constantly monitors the status of this port and generates an interrupt at a valide edge. Therefore, if the \overline{INT}_0 interrupt is not used, it must be disabled and if it is used, this port must be set to input. The I/O level of port P4 is TTL compatible except the case that the input level of some ports which function as \overline{INT}_0 . A_0 or \overline{CS} are CMOS compatible.

(6) Port P5

Port P5 is an 5-bit I/O port with function similar to port P0. All pins have program selectable dual functions. When a UART function is selected, the input and output from pins $P5_0 \sim P5_3$ are determined by the contents of the UART mode register and UART control register. Port $P5_4$ is common with CNTR pin.

The I/O level is TTL compatible except the case when some ports which function as RxD, \overline{CTS} , CLK and CNTR are CMOS compatible.

(7) Clock ϕ output pin

This is the timing output pin. When selected the main clock ($X_{IN} \sim X_{OUT}$) as the internal system clock, the clock frequency divided by four is outputed.

"H" is output from this pin when STP or WIT instruction is executed.

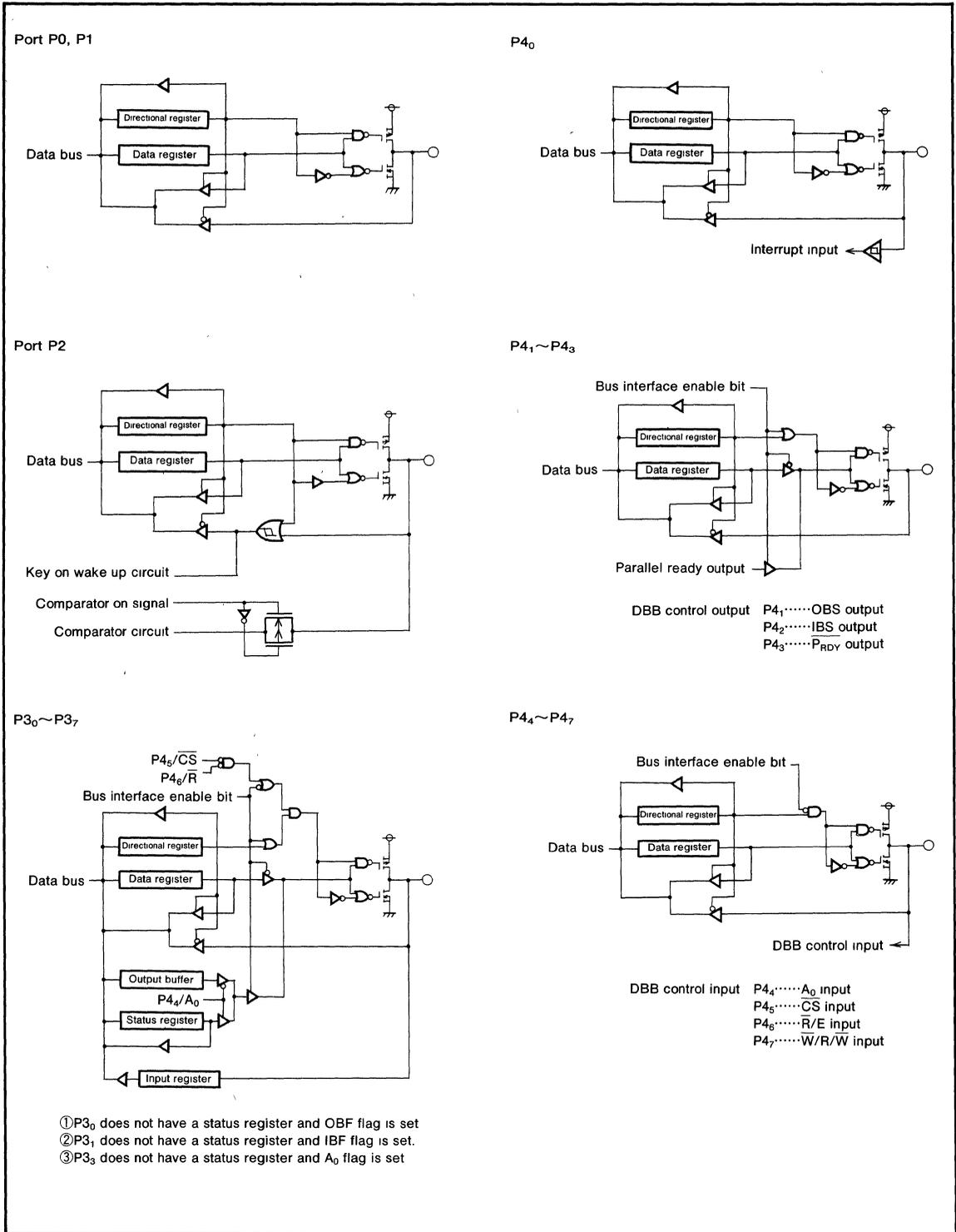


Fig. 16 Ports P0~P6 block diagram

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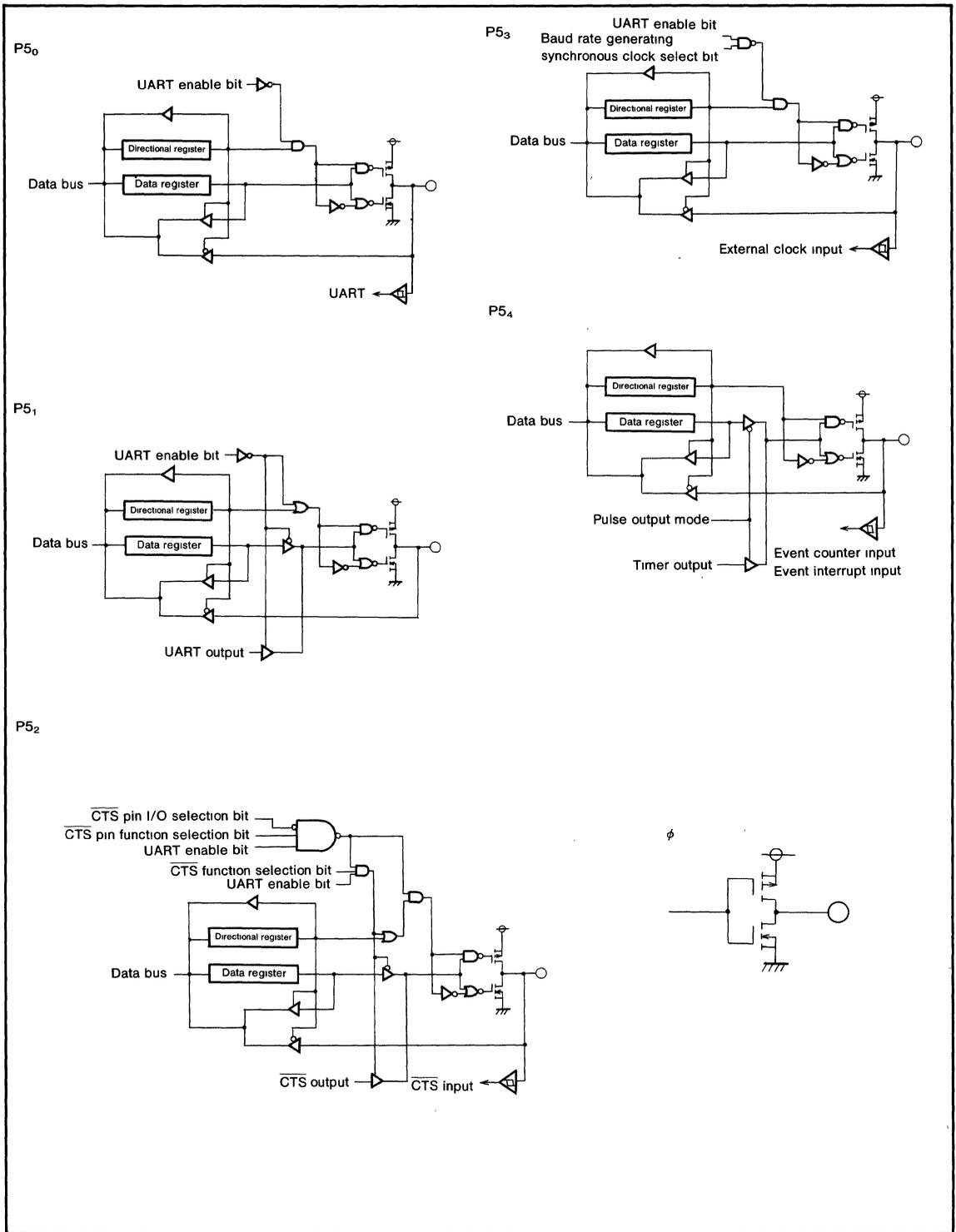


Fig. 17 Ports P5 and ϕ block diagram

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 21.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16} , respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figures 18 and 19.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 20. X_{IN} is the input, and X_{OUT} is open.

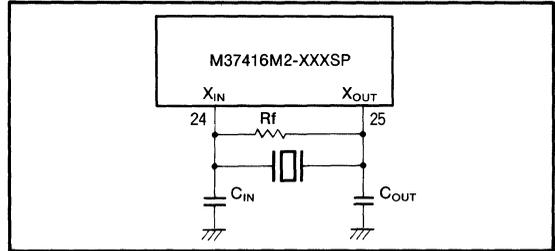


Fig. 18 External ceramic resonator circuit

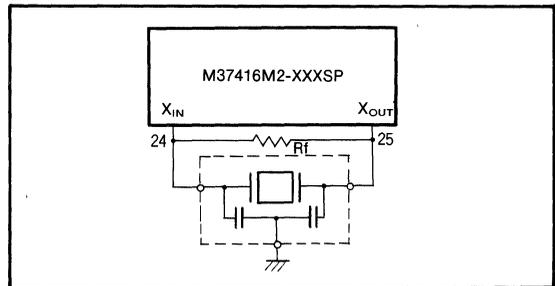


Fig. 19 External ceramic resonator (capacity built-in type) circuit

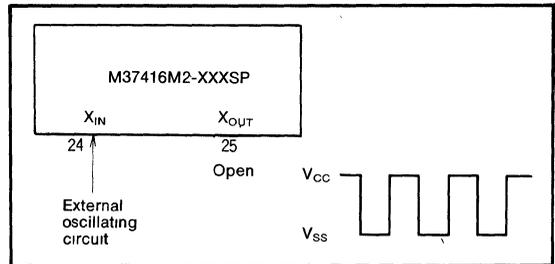


Fig. 20 External clock input circuit

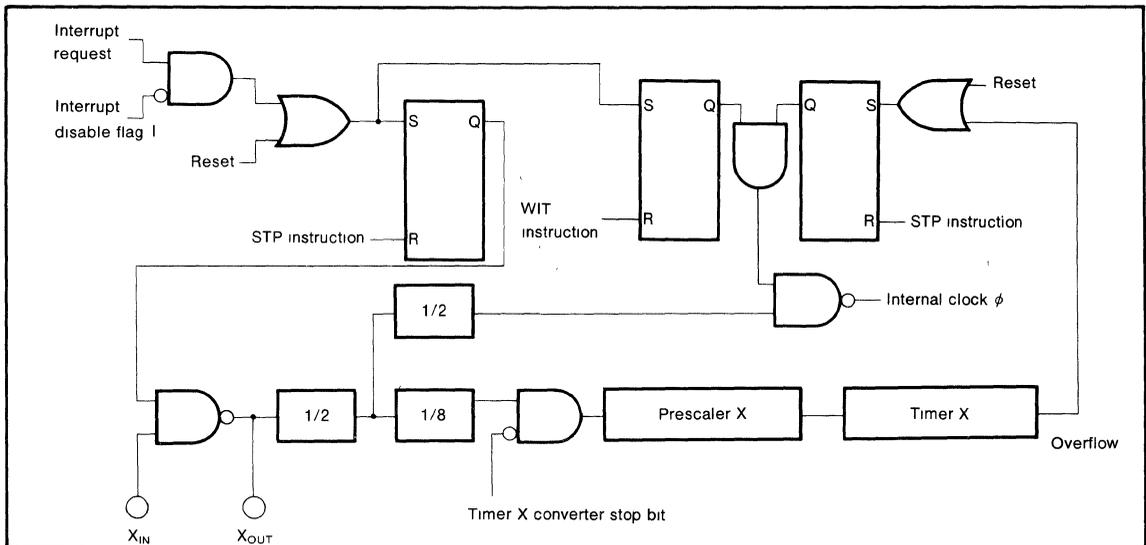


Fig. 21 Block diagram of clock generating circuit

PROGRAMMING NOTES

- (1) The frequency ratio of the timer and the prescaler is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) When the timer X or timer 1 is input the clock except $\phi/4$ or it divided by timer, read the contents of these timers either while the input of these timers are not changing or after counting of timers are stopped.
- (4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) The STP instruction must be executed after setting timer X count enable bit to enable "0", timer X interrupt enable bit to inhibit ("0"), and timer X interrupt request bit to no request ("0").
- (7) Use the LDA (immediate, T=1) instruction to modify the interrupt request distinguish register. SEB and CLB instructions can be used only when interrupts in the register are not generated at executing these instructions.
- (8) Do not write any data into an address where no register nor port is assigned.
- (9) The power current is max. 10mA in DC. However, because a rush current and a bus charge-discharge current flow transiently, a bypass capacitor must be connected between V_{SS} and V_{CC} .

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- mask ROM order confirmation form
- mark specification form
- ROM data.....EPROM 3 sets

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state.	-0.3~7	V
V_I	Input voltage X_{IN} , RESET		-0.3~7	V
V_I	Input voltage $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P4_0\sim P4_7$, $P5_0\sim P5_4$, CNV_{SS}		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P5_0\sim P5_4$, X_{OUT} , ϕ		-0.3~ $V_{CC}+0.3$	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	1000 (Note 1)	mW
T_{opr}	Operating temperature		-10~70	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~125	$^\circ\text{C}$

Note 1 : 500mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS

($V_{CC}=5V\pm 10\%$, $T_a=-10\sim 70^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage RESET, X_{IN} , CNV_{SS} (Note 1)	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $P1_0\sim P1_7$, $P3_0\sim P3_7$, $P4_0\sim P4_7$, $P5_0\sim P5_4$, (expect Note 1)	2.0		V_{CC}	V
V_{IH}	"H" input voltage $P0_0\sim P0_7$, $P2_0\sim P2_7$ (Note 2)	$0.7V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage $P1_0\sim P1_7$, $P3_0\sim P3_7$, $P4_0\sim P4_7$, $P5_0\sim P5_4$, (expect Note 1)	0		0.8	V
V_{IL}	"L" input voltage $P0_0\sim P0_7$	0		$0.3V_{CC}$	V
V_{IL}	"L" input voltage $P2_0\sim P2_7$ (Note 2)	0		$0.26V_{CC}$	V
V_{IL}	"L" input voltage RESET	0		$0.12V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}	0		$0.16V_{CC}$	V
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P5_0\sim P5_4$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P5_0\sim P5_4$ (Note 3)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P5_0\sim P5_4$			-10	mA
$I_{OH(avg)}$	"H" average output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P5_0\sim P5_4$ (Note 3)			-5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency	1		8	MHz

Note 1 : Ports operating as special function pins $INT_0(P4_0)$, $A_0(P4_0)$, $\overline{CS}(P4_5)$, $RxD(P5_0)$, $CTS(P5_2)$, $CLK(P5_3)$, $CNTR$

2 : See comparator characteristics for input voltage as comparator input

3 : The total of I_{OL} of Port P0, P1, P2 and ϕ should be 40mA (max.).

The total of I_{OL} of Port P3 and P5 should be 40mA (max)

The total of I_{OH} of Port P0, P1, P2 and ϕ should be 40mA (max).

The total of I_{OH} of Port P3 and P5 should be 40mA (max.)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ELECTRIC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=8MHz$)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V_{OH}	"H" output voltage ϕ	$I_{OH} = -2\text{ mA}$	$V_{CC}-1$			V	
V_{OH}	"H" output voltage $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$, $P_{50}\sim P_{54}$	$I_{OH} = -5\text{ mA}$	$V_{CC}-1$			V	
V_{OL}	"L" output voltage $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$, $P_{50}\sim P_{54}$	$I_{OL} = 2\text{ mA}$			0.45	V	
V_{OL}	"L" output voltage $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$, $P_{50}\sim P_{54}$	$I_{OL} = 5\text{ mA}$			1	V	
$V_{T+} - V_{T-}$	Hysteresis $P_{20}\sim P_{27}$, $INT_0(P_{40})$, $A_0(P_{44})$, $CS(P_{45})$, $RxD(P_{50})$, $CTS(P_{52})$, $CLK(P_{53})$, $CNTR$	Function input level	0.3		1	V	
$V_{T+} - V_{T-}$	Hysteresis RESET				0.7	V	
$V_{T+} - V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V	
I_{IL}	"L" input current $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$, $P_{40}\sim P_{47}$, $P_{50}\sim P_{54}$, RESET, X_{IN}	$V_i = V_{SS}$	-5		5	μA	
I_{IH}	"H" input current $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$, $P_{40}\sim P_{47}$, $P_{50}\sim P_{54}$, RESET, X_{IN}	$V_i = V_{CC}$	-5		5	μA	
V_{RAM}	RAM retention voltage	At stop mode	2			V	
I_{CC}	Supply current	$f(X_{IN})=8MHz$ At system operation, comparator not operation			10	mA	
		$f(X_{IN})=8MHz$, Comparator is operation, At system operation, square wave			15		
		At stop mode				1	μA
		(Note 1)	$T_a=25^\circ C$			10	

Note 1 : Output pin ϕ is open V_{SS} is inputs to ports Comparator conversion is complete condition

COMPARATOR CHARACTERISTICS ($V_{CC}=5V\pm 5\%$, $V_{CC}=0V$, $T_a=25^\circ C$, $f(X_{IN})=8MHz$)

Parameter	Limits			Unit
	Min.	Typ	Max	
Resolution	—	—	$(1/8)V_{CC}$	V
Internal analog voltage error	—	—	$\pm(1/8)V_{CC}$	V
Analog input voltage	0	—	V_{CC}	V

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMING REQUIREMENTS

Port/single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max.	
$t_{SU}(P0D-\phi)$	Port P0 input setup time	Fig 22	200			ns
$t_{SU}(P1D-\phi)$	Port P1 input setup time		200			ns
$t_{SU}(P2D-\phi)$	Port P2 input setup time		200			ns
$t_{SU}(P3D-\phi)$	Port P3 input setup time		200			ns
$t_{SU}(P4D-\phi)$	Port P4 input setup time		200			ns
$t_{SU}(P5D-\phi)$	Port P5 input setup time		200			ns
$t_{H}(\phi-P0D)$	Port P0 input hold time		40			ns
$t_{H}(\phi-P1D)$	Port P1 input hold time		40			ns
$t_{H}(\phi-P2D)$	Port P2 input hold time		40			ns
$t_{H}(\phi-P3D)$	Port P3 input hold time		40			ns
$t_{H}(\phi-P4D)$	Port P4 input hold time		40			ns
$t_{H}(\phi-P5D)$	Port P5 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time				1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width					ns
$t_W(X_{IN}H)$	External clock input "H" pulse width					ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing (\overline{R} and \overline{W} separation type mode)

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{SU}(CS-R)$	CS setup time	Fig 23	0			ns
$t_{SU}(CS-W)$	CS setup time		0			ns
$t_{H}(R-CS)$	CS hold time		0			ns
$t_{H}(W-CS)$	CS hold time		0			ns
$t_{SU}(A-R)$	A_0 setup time		40			ns
$t_{SU}(A-W)$	A_0 setup time		40			ns
$t_{H}(R-A)$	A_0 hold time		10			ns
$t_{H}(W-A)$	A_0 hold time		10			ns
$t_W(R)$	Read pulse width		160			ns
$t_W(W)$	Write pulse width		160			ns
$t_{SU}(D-W)$	Date input setup time before write		100			ns
$t_{H}(W-D)$	Date input hold time after write		10			ns

Master CPU bus interface timing ($\overline{R}/\overline{W}$ type mode)

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{SU}(CS-E)$	CS setup time	Fig 23	0			ns
$t_{H}(E-CS)$	CS hold time		0			ns
$t_{SU}(A-E)$	A_0 setup time		40			ns
$t_{H}(E-A)$	A_0 hold time		10			ns
$t_{SU}(RW-E)$	$\overline{R}/\overline{W}$ setup time		40			ns
$t_{H}(E-RW)$	$\overline{R}/\overline{W}$ hold time		10			ns
$t_W(EL)$	Enable clock "L" pulse width		160			ns
$t_W(EH)$	Enable clock "H" pulse width		160			ns
$t_r(E)$	Enable clock rising edge time				25	ns
$t_f(E)$	Enable clock falling edge time				25	ns
$t_{SU}(D-E)$	Data input setup time before write		100			ns
$t_{H}(E-D)$	Data input hold time after write		10			ns

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

SWITCHING CHARACTERISTICS

Port/single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=8MHz$ unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 22			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns

Master CPU bus interface (\overline{R} and \overline{W} separation type mode)

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=8MHz$ unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(R-D)}$	Data output enable time after read	Fig 23			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PHL(R-OBF)}$	OBF output transmission time after read				150	ns
$t_{PLH(R-PR)}$	\overline{PRDY} output transmission time after read				150	ns
$t_{PHL(W-IBF)}$	IBF output transmission time after write				150	ns
$t_{PLH(W-PR)}$	\overline{PRDY} output transmission time after write				150	ns

Master CPU bus interface (R/\overline{W} type mode)

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=8MHz$ unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read	Fig.23			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PHL(E-OBF)}$	OBF output transmission time after E clock				150	ns
$t_{PLH(E-IBF)}$	IBF output transmission time after E clock				150	ns
$t_{PLH(E-PR)}$	\overline{PRDY} output transmission time after E clock				150	ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V

V_{IL} 0.4V

Output test level : V_{OH} 2.0V

V_{OL} 0.8V

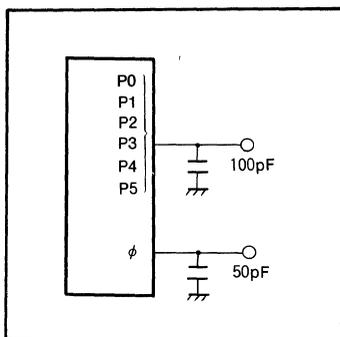


Fig. 22 Test circuit in single-chip mode

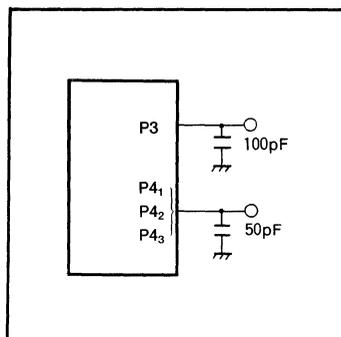
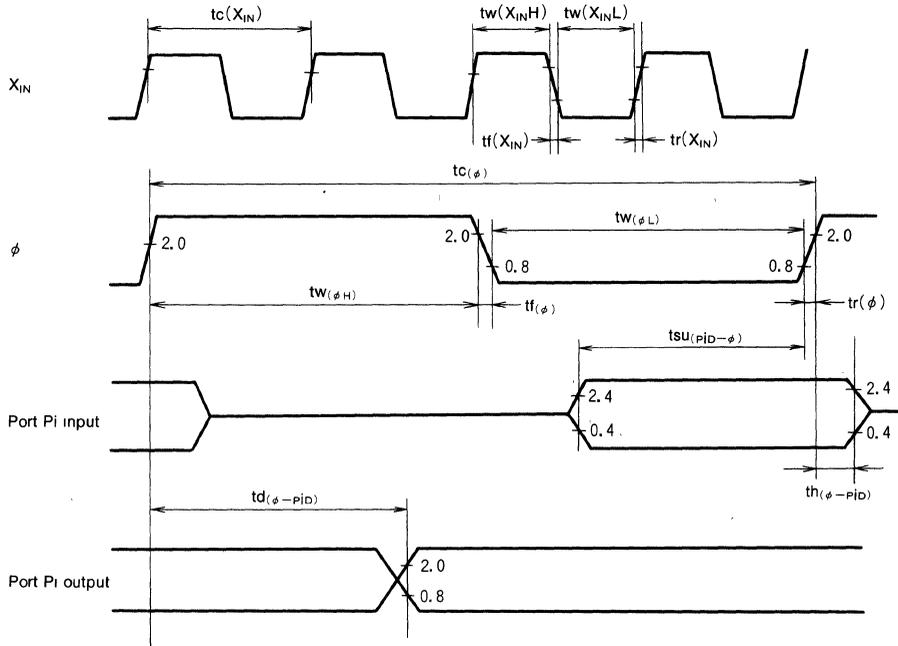


Fig. 23 Master CPU bus interface test circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMING DIAGRAM

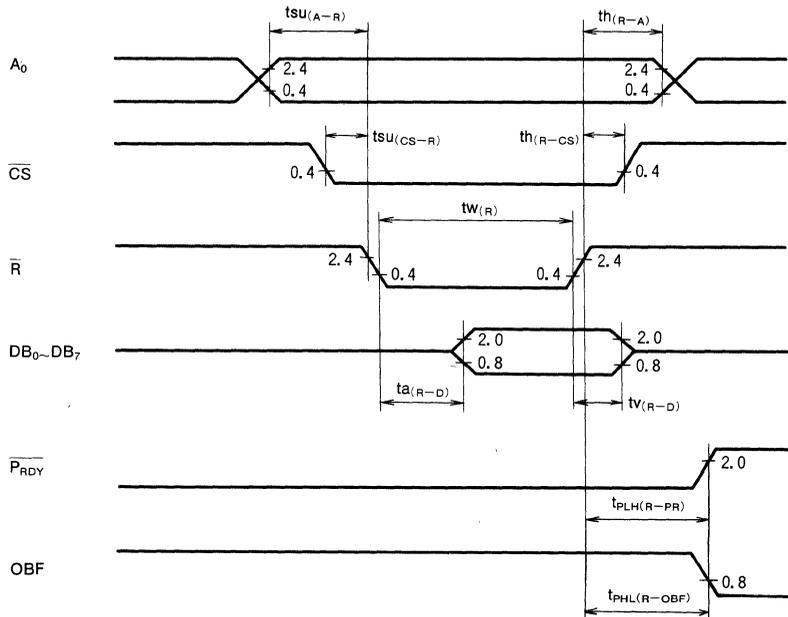
Port/single-chip mode timing diagram



Note : $V_{IH}=0.8V_{CC}$, $V_{IL}=0.16V_{CC}$ of X_{IN}

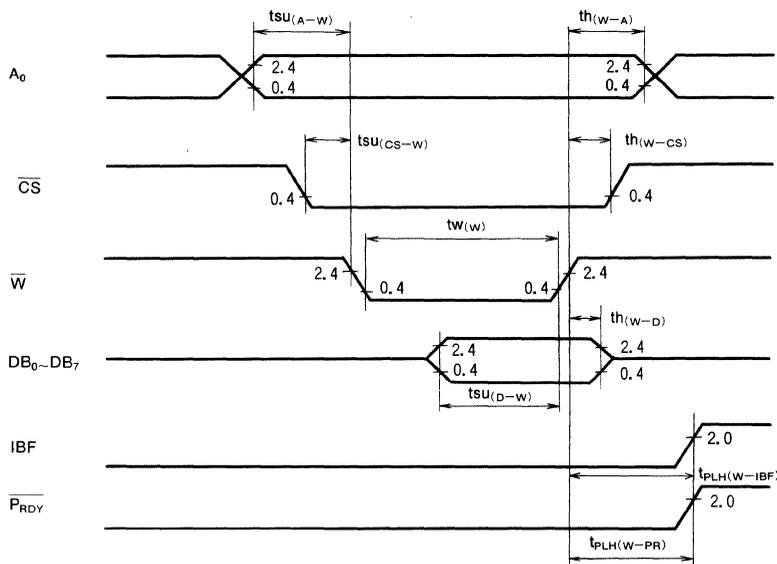
Master CPU bus interface/ \overline{R} and \overline{W} separation type timing diagram

Read

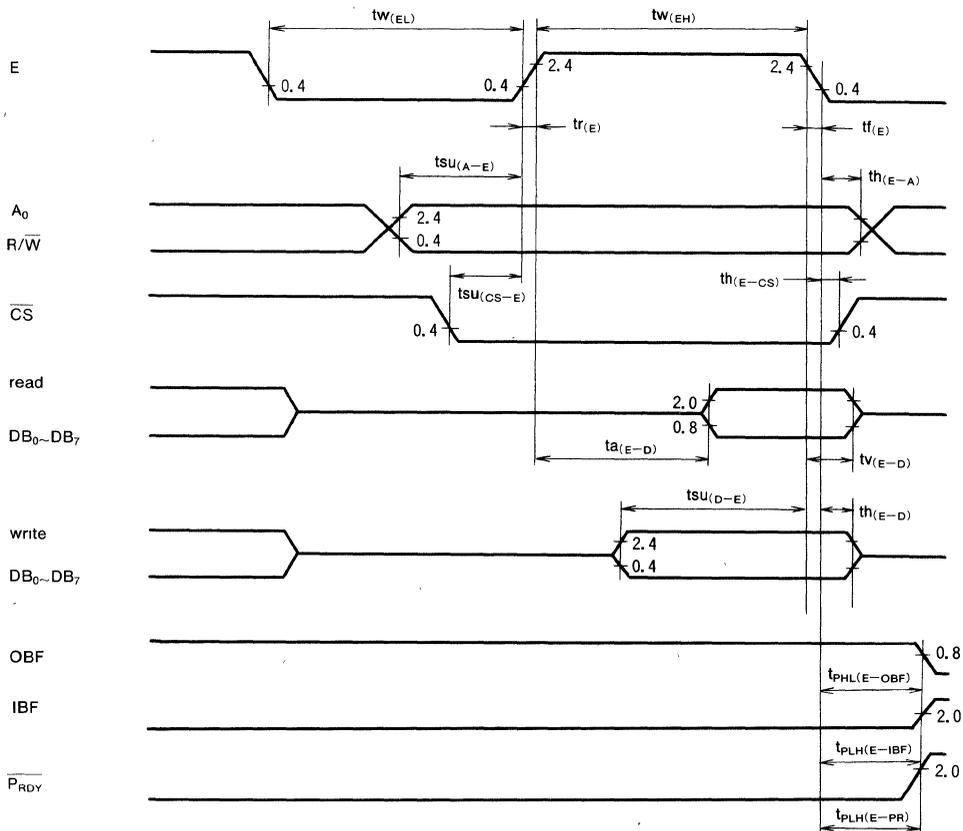


SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Write



Master CPU interface/ R/W type timing diagram



MITSUBISHI MICROCOMPUTERS

M37420M4-XXXSP

M37420M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37420M4-XXXSP and the M37420M6-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 52-pin shrink plastic molded DIP.

These single-chip microcomputers are useful for household appliance and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37420M4-XXXSP and the M37420M6-XXXSP are noted below. The following explanations apply to the M37420M6-XXXSP.

Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37420M4-XXXSP	8192 bytes	192 bytes
M37420M6-XXXSP	12288 bytes	256 bytes

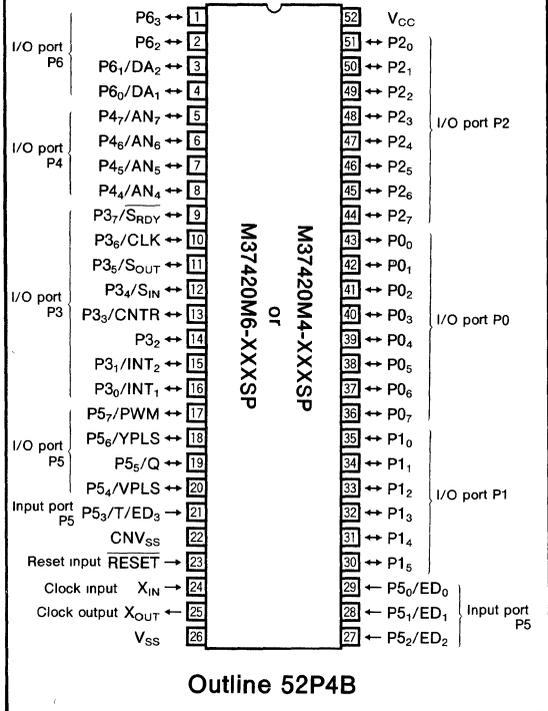
FEATURES

- Number of basic instructions..... 69
- Memory size ROM ...12288 bytes (M37420M6-XXXSP)
8192 bytes (M37420M4-XXXSP)
RAM..... 256 bytes (M37420M6-XXXSP)
192 bytes (M37420M4-XXXSP)
- Instruction execution time
..... 1 μ s (minimum instructions, at 8MHz frequency)
- Single power supply $f(X_{IN})=8\text{MHz}$ 5V \pm 10%
- Power dissipation
normal operation mode (at 8MHz frequency)..... 30mW
- Subroutine nesting 96 levels (Max.)
- Interrupt..... 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4)..... 42
- Input port (Port P5) 8
- Serial I/O (8-bit/16-bit) 1
- A-D converter..... 8-bit successive approximation
- D-A converter
- 14-bit PWM function
- Watchdog timer

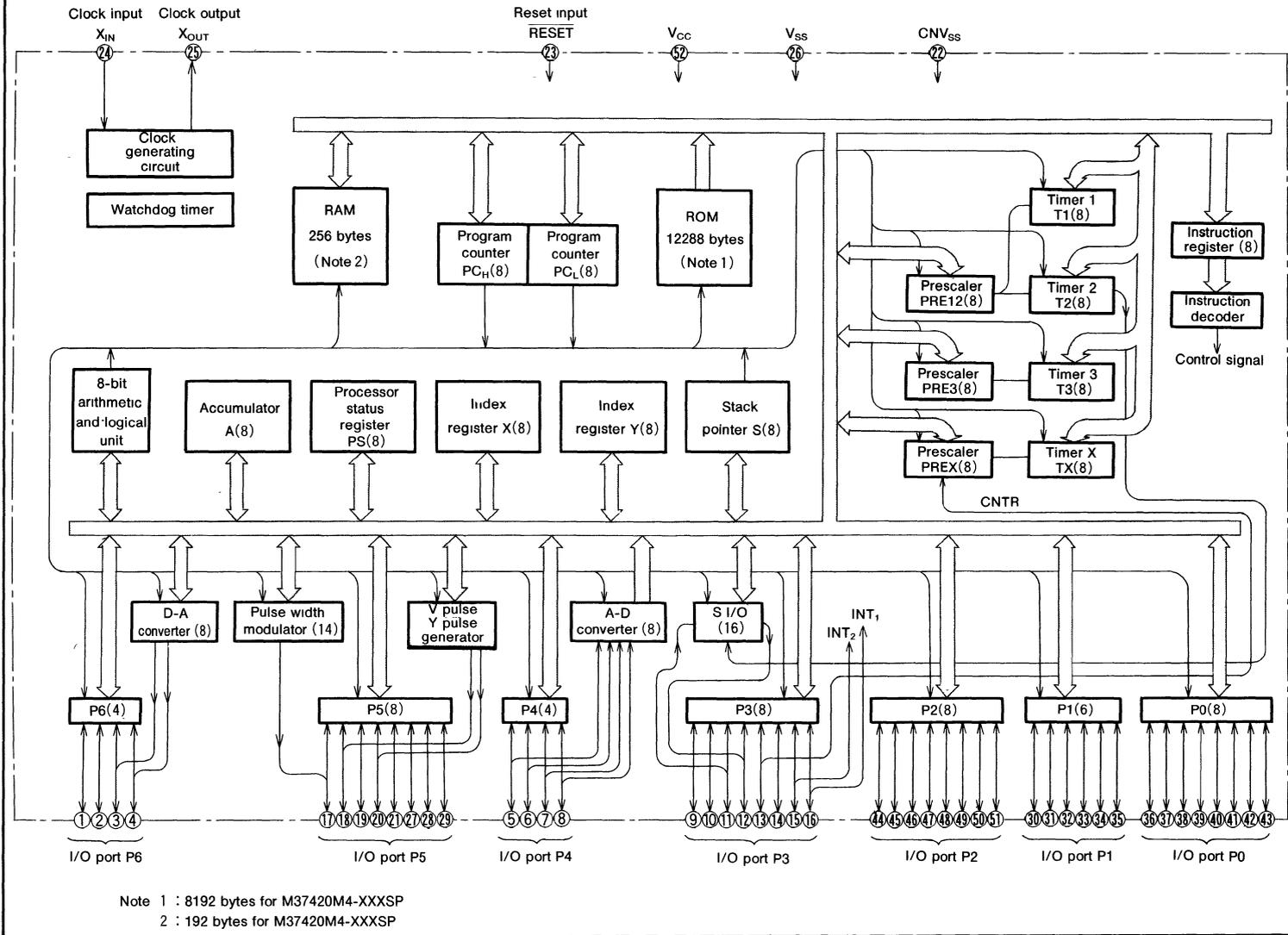
APPLICATION

VCR, TV, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



M37420M6-XXXSP BLOCK DIAGRAM



MITSUBISHI MICROCOMPUTERS
M37420M4-XXXSP
M37420M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37420M6-XXXSP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		1 μ s (minimum instructions, at 8MHz frequency)
Clock frequency		8MHz
Memory size	ROM	12288bytes (8192 bytes for M37420M4-XXXSP)
	RAM	256bytes (192 bytes for M37420M4-XXXSP)
Input/Output ports	P0, P1, P2, P3, P4, P5 ₄ ~P5 ₇ , P6	I/O 8-bit \times 3, 6-bit \times 1, 4-bit \times 3
	P5 ₀ ~P5 ₃	Input 4-bit \times 1
Serial I/O		8-bit \times 1 or 16-bit \times 1
Timers		8-bit prescaler \times 3+8-bit timer \times 4
A-D conversion		8-bit \times 1 (4 channels)
D-A conversion		8-bit \times 2
Pulse width modulator		14-bit \times 1
Watchdog timer		15-bit \times 1
Subroutine nesting		96 levels (max)
Interrupts		Two external interrupts, Three internal timer interrupts (or timer \times 2, SI/O \times 1)
Clock generating circuit		Built-in (ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 10%
Power dissipation	at high-speed operation	30mW (at 8MHz frequency)
Input/Output characteristics	Input/Output voltage	12V (Ports P0, P1, P3)
Operating temperature range		-10~70 $^{\circ}$ C
Device structure		CMOS silicon gate process
Package		52-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS} .
CNV _{SS}	CNV _{SS}		This is usually connected to V _{SS} .
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}	Clock output	Output	
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is N-channel open drain
P1 ₀ ~P1 ₅	I/O port P1	I/O	Port P1 is an 6-bit I/O port and has basically the same functions as port P0 The output structure is N-channel open drain
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as $\overline{S_{RDY}}$, CLK, S _{OUT} , and S _{IN} pins, respectively Also P3 ₃ and P3 ₂ work as CNTR pin and the lowest interrupt input pin ($\overline{INT_2}$), respectively
P4 ₄ ~P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0 P4 ₂ ~P4 ₇ work as analog input port AN ₄ ~AN ₇
P5 ₀ ~P5 ₃	Input port P5	Input	Low-order 4-bit of port P5 is input port These can be used as the edge sence inputs P5 ₀ ~P5 ₂ detect the rising edge and P5 ₃ detects both edges Also, P5 ₃ is common with the external trigger and V pulse, Y pulse generator trigger input
P5 ₄ ~P5 ₇	I/O port P5	I/O	High-order 4-bit of port P5 is I/O port and has basically the same function as port P0 P5 ₇ is common with the 14-bit PWM. The output structure is CMOS output
P6 ₀ ~P6 ₃	Output port P6	Output	Port P6 is an 4-bit output port At external trigger output mode, P6 ₀ and P6 ₁ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively The output structure is N-channel open drain.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37420 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

Timer Control Register

The timer control register is allocated to address $00FF_{16}$.

This register has a stack page bit.

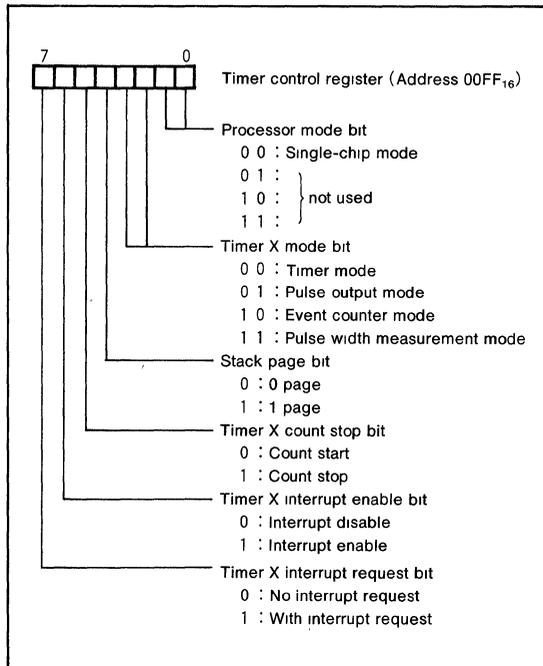


Fig.1 Structure of timer control register

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

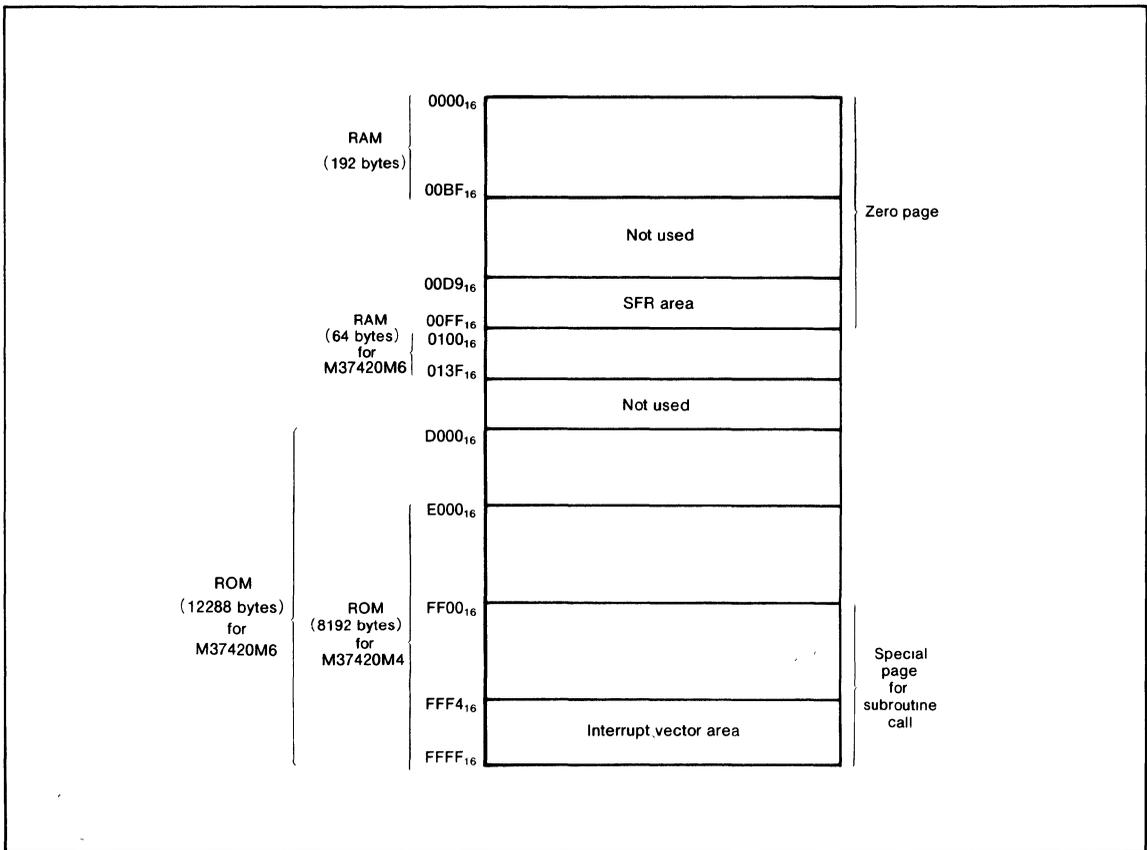


Fig.2 Memory map

00D9 ₁₆	D-A conversion register 1	00EC ₁₆	Port P5
00DA ₁₆	D-A conversion register 2	00ED ₁₆	Port P5 latch/directional register
00DB ₁₆	V pulse preset value P	00EE ₁₆	Port P6
00DC ₁₆	V pulse preset value N	00EF ₁₆	Port P6 directional register
00DD ₁₆	V pulse register	00F0 ₁₆	Pulse width modulation register H
00DE ₁₆	Serial I/O register L	00F1 ₁₆	Pulse width modulation register L
00DF ₁₆	Serial I/O register H	00F2 ₁₆	Successive approximation register
00E0 ₁₆	Port P0	00F3 ₁₆	A-D control register
00E1 ₁₆	Port P0 directional register	00F4 ₁₆	Watchdog timer
00E2 ₁₆	Port P1	00F5 ₁₆	Serial I/O mode register
00E3 ₁₆	Port P1 directional register	00F6 ₁₆	Special function selection register
00E4 ₁₆	Port P2	00F7 ₁₆	Timer 3 prescaler
00E5 ₁₆	Port P2 directional register	00F8 ₁₆	Timer 3
00E6 ₁₆		00F9 ₁₆	Timer 1,2 prescaler
00E7 ₁₆		00FA ₁₆	Timer 1
00E8 ₁₆	Port P3	00FB ₁₆	Timer 2
00E9 ₁₆	Port P3 directional register	00FC ₁₆	Timer X prescaler
00EA ₁₆	Port P4	00FD ₁₆	Timer X
00EB ₁₆	Port P4 directional register	00FE ₁₆	Interrupt control register
		00FF ₁₆	Timer control register

Fig. 3 SFR (Special Function Register) memory map

INTERRUPT

The M37420M6-XXXSP can be interrupted from seven sources; INT₁, timer X, timer 1, timer 2/serial I/O, or INT₂/BRK instruction.

However, the INT₁ pin is used with port P3₀ and the INT₂ pin is used with port P3₁, and the corresponding directional register bit should be set to "0" when each port used as an interrupt input pin.

The value of bit 2 and bit 3 of the serial I/O mode register (address 00F5₁₆) determine whether the interrupt is from timer 2 or from serial I/O. When the value of bit 2 and bit 3 is [00], the interrupt is from timer 2, and the value of bit 2 and bit 3 is [01], the interrupt is from serial I/O. Also, when the value of bit 2 and bit 3 is [01], parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 4. An interrupt is accepted when

the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

- (1) When the level of INT₁ or INT₂ pin changes
- (2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
RESET	1	FFF ₁₆ , FFE ₁₆
INT ₁	2	FFD ₁₆ , FFC ₁₆
Timer X	3	FFB ₁₆ , FFA ₁₆
Timer 1	4	FF9 ₁₆ , FF8 ₁₆
Timer 2 or serial I/O	5	FF7 ₁₆ , FF6 ₁₆
INT ₂ (BRK)	6	FF5 ₁₆ , FF4 ₁₆

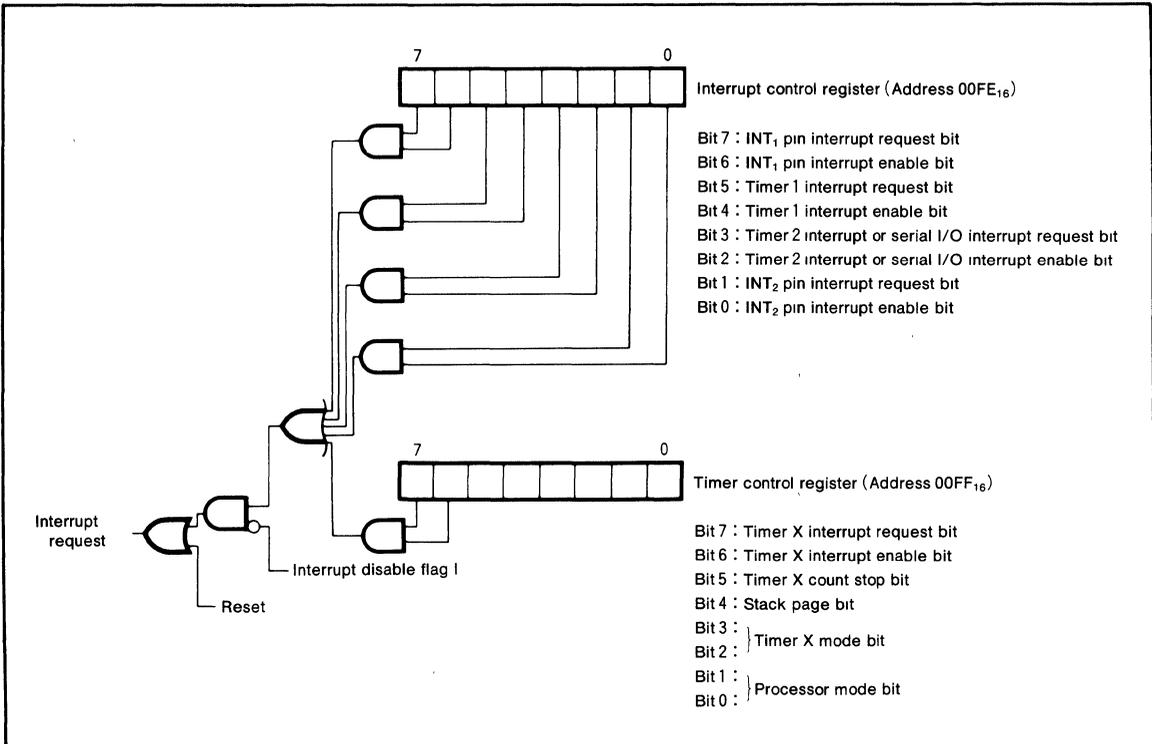


Fig.4 Interrupt control

The change in level at which the INT pins generate an interrupt varies according to the content of bits 4 and 5 of the special function selection register (address 00F6₁₆). When these bits are "0", the interrupt request is generated when INT changes from high-level to low-level. When these bits are "1", the interrupt request is generated when INT changes from low-level to high-level. Bits 4 and 5 correspond to INT₁ and INT₂ respectively.

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the INT₂ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if INT₂ generated the interrupt.

TIMER

The M37420M6-XXXSP has four timers; timer X, timer 1, timer 2 and timer 3. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1, timer 2 and timer 3 is shown in Figure 5.

The P3₃/CNTR pin cannot be used as CNTR when P3₃ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All four timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero for timer 1, timer 2 and timer X. The interrupt and timer control registers are located at addresses 00FE₁₆ and 00FF₁₆, respectively (see Interrupt section). The prescaler latch and timer latch can be loaded with any number.

The four modes of timer X as follows:

(1) Timer mode [00]

In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]

In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]

This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR

pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]

This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 6.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF₁₆ and 01₁₆, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

The function of timer 3 is as same as that of timer 1 and timer 2, with the exception that the detection of its overflow is known by the overflow bit (bit 3 of address 00EF₁₆). When the timer down-counts to zero, the overflow bit is set to "1" and the contents of the timer's latch is reloaded into the timer.

The reset of the overflow bit is made by;

- a) hard ware reset
- b) write "0" to overflow bit
- c) write instruction to timer 3

The structure of special function selection register is shown in Figure 7.

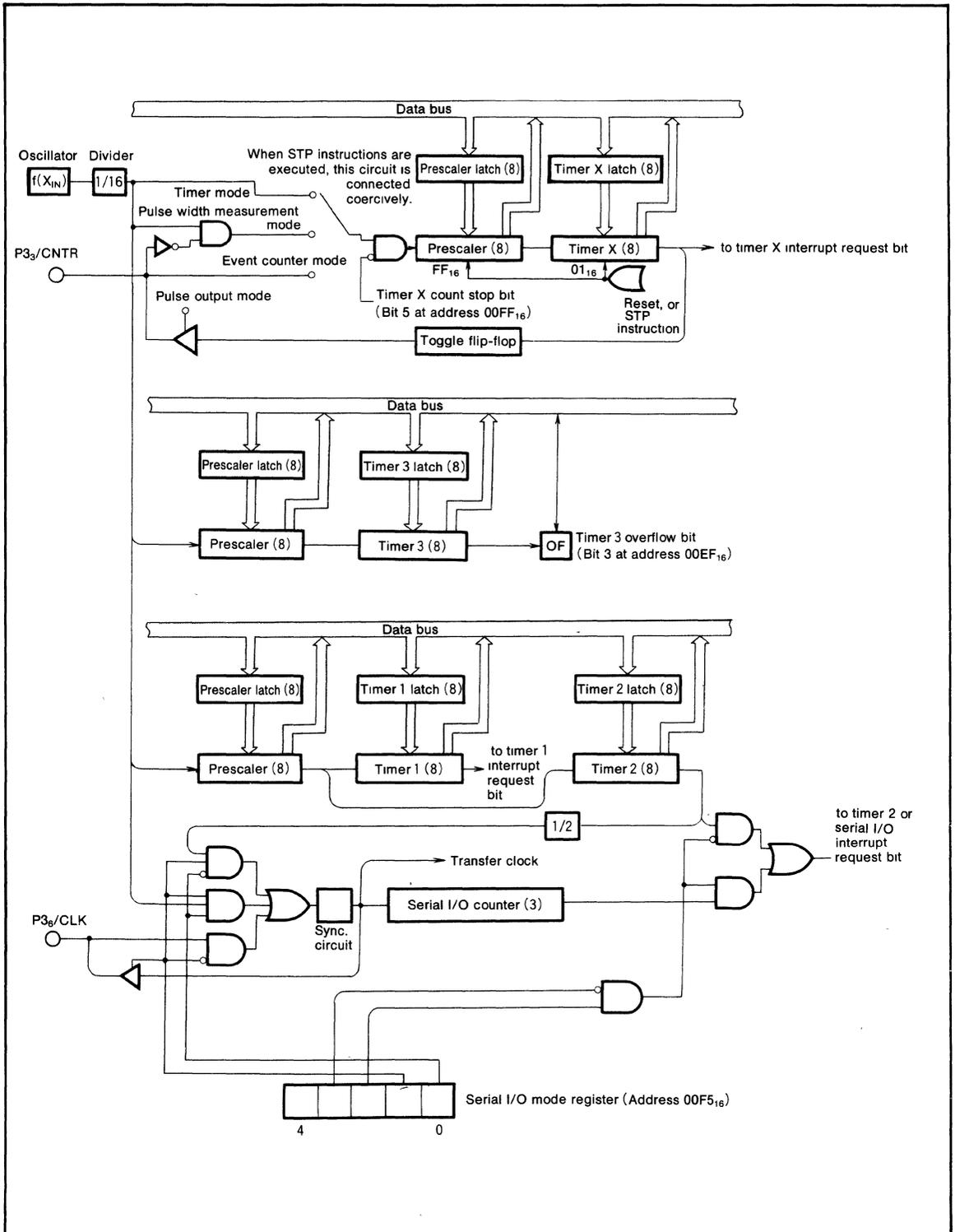


Fig.5 Block diagram of timer X, timer 1, timer 2, and timer 3

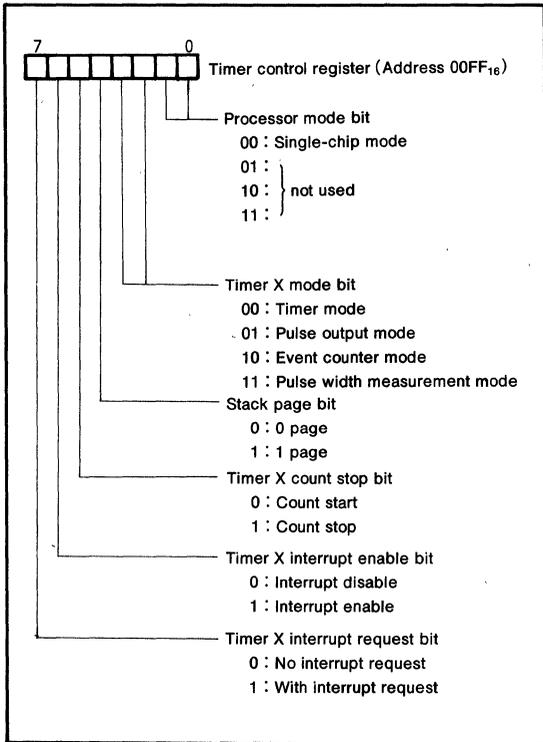


Fig.6 Structure of timer control register

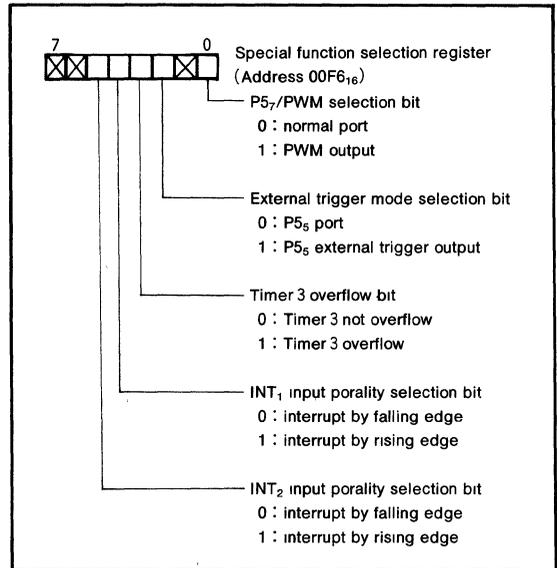


Fig.7 Structure of special function selection register

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O pins (S_{OUT} , S_{IN}) are used as P3₇, P3₆, P3₅, and P3₄, respectively. The serial I/O mode register (address 00F5₁₆) is a 6-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from P3₆ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the oscillator frequency divided by 16, becomes the clock.

Bit 2 to 4 decide whether parts of P3 will be used as a serial I/O or not. When bit 3 is "0" and bit 2 is "1", P3₆ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P3₆. If an external synchronous clock is selected, the clock is input to P3₆ and P3₅ will be a serial output and P3₄ will be a serial input. To use P3₄ as a serial input, set the directional register bit which corresponds to P3₄ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 3 and bit 2 need to be set to "01", if they are "00" P3₆ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 4 determines if P3₇ is used as an output pin for the receive data ready signal (bit 4 = 1, $\overline{S_{RDY}}$) or used as normal I/O pin (bit 4 = 0). Bit 5 determines the serial I/O mode. If this bit is "0", serial I/O becomes 8-bit mode and this bit is "1", serial I/O becomes 16-bit mode. The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address 00F7₁₆). Data is stored only to the serial I/O register L (address 00DE₁₆) in 8-bit mode, and stored high-order 8-bit to serial I/O register H (address 00DF₁₆) at first, then low order 8-bit to serial I/O register L (address 00DE₁₆) in 16-bit mode. After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37420M6-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 in 8-bit mode and 15 in 16-bit mode when data is stored in the serial I/O register. At each falling edge of the transfer

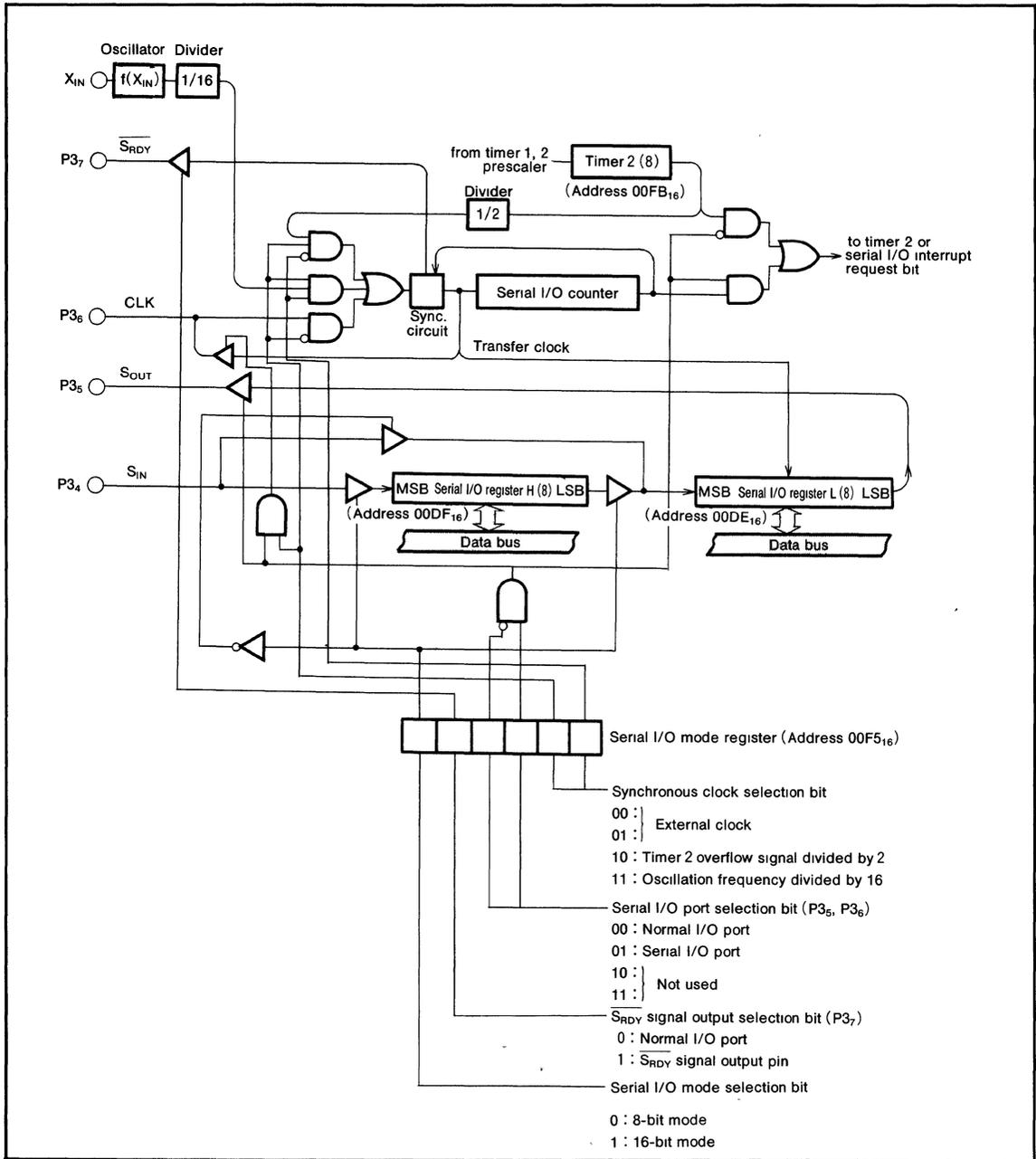


Fig.8 Block diagram of serial I/O

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clock, serial data is output to P3₅. During the rising edge of this clock, data can be input from P3₄ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 or 16 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock—If an external clock is used, the interrupt

request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. An example of communication between two M37420M6-XXXSPs is shown in Figure 10.

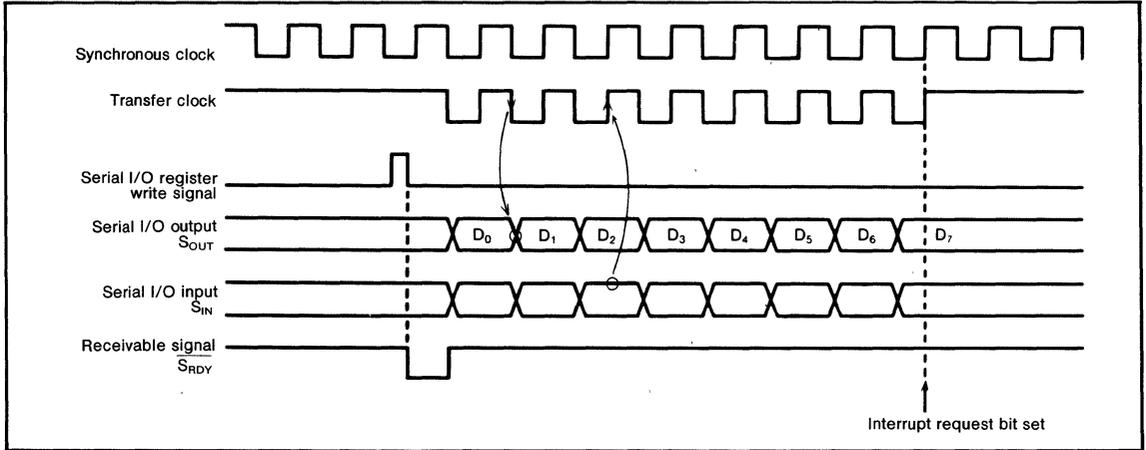


Fig.9 Serial I/O timing

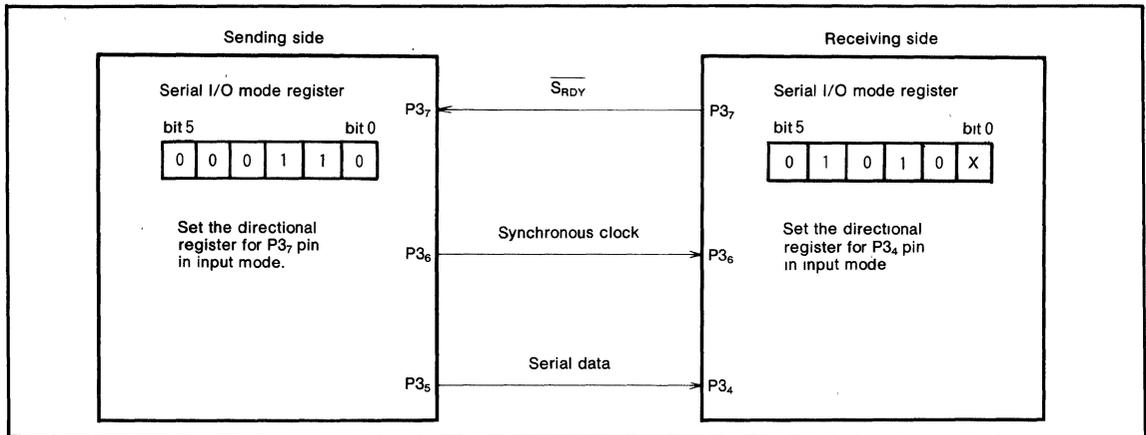


Fig.10 Example of serial I/O connection

A-D CONVERTER

An 8-bit successive approximation method of A-D conversion is employed providing a precision of $\pm 3\text{LSB}$. A block diagram of the A-D converter is shown in Figure 11. Conversion is automatic once it is started with the program.

The four analog inputs are used in common with pins P4₇, P4₆, P4₅ and P4₄ of port 4. Bits 2, 1 and 0 of the A-D control register (address 00F3₁₆) are used to select which pins are used for A-D conversion. The input condition is accomplished by setting to "0" the bit in the directional register that corresponds to the pin where A-D conversion is to take place. Bit 4 of the A-D control register is the A-D conversion end bit. During A-D conversion, this bit is "0", and upon completion becomes "1". Thus, it can be ascertained whether or not A-D conversion has been completed or not by inspecting this bit. The relation between the contents of the A-D control register and the selection of input pins are shown in Figure 12.

The results of the conversion can be found by reading the contents of the successive approximation register address 00F2₁₆ which stores the results of the conversion. The procedure for executing A-D conversion is next explained. Firstly, the pin that is to be used for the A-D conversion is selected by setting bit 2, bit 1 and bit 0 of the A-D control register. Next, the successive approximation is written to upon which the A-D conversion starts. Since actual data is

not written to the successive approximation, any type of may be written. Simultaneous with its being written, the A-D conversion end bit (bit 4 of address 00F3₁₆) is cleared to "0" signifying that A-D conversion operations are being conducted. A-D conversion completes after 198 clock cycles upon which the A-D conversion end bit is set to "1" and the results of the conversion can be found in the successive approximation register. Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion. When A-D conversion is not required, power consumption can be saved by setting bit 5 of the A-D control register to "0". To carry out A-D conversion, set bit 5 to "1", and connect the resistor ladder.

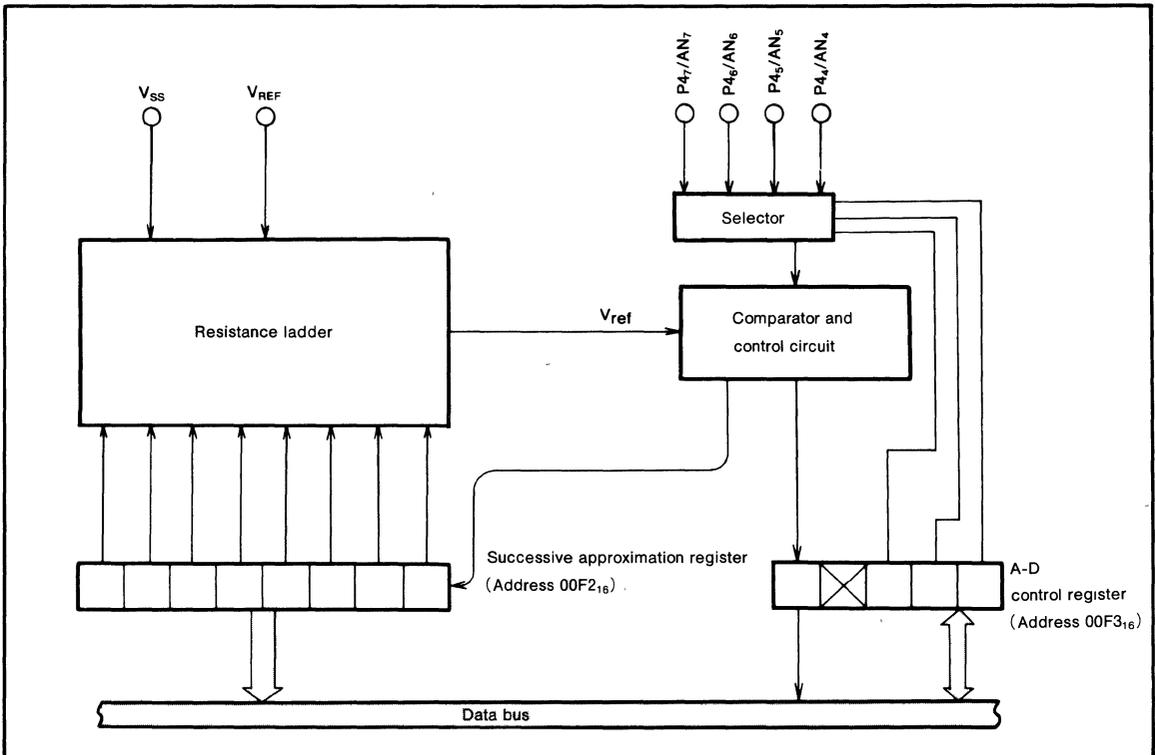


Fig.11 Block diagram of A-D converter

D-A CONVERTER

The M37420M6-XXXSP has two R-2R method D-A converters. D-A conversion starts by setting value to D-A conversion register (address 00D9₁₆ and 00DA₁₆).

The output port of D-A conversion result DA₁ or DA₂ is common with P6₀ and P6₁ respectively. The value of bit 7 or bit 6 of A-D control register (address 00F3₁₆) determines whether this port is used as D-A output or normal port. When this bit is "1" this port becomes D-A output, and is "0" this port becomes normal port.

Bit 6 or bit 7 corresponds to P6₀/DA₁ or P6₁/DA₂ respectively. When using each port as D-A output, its directional register must be set to "0".

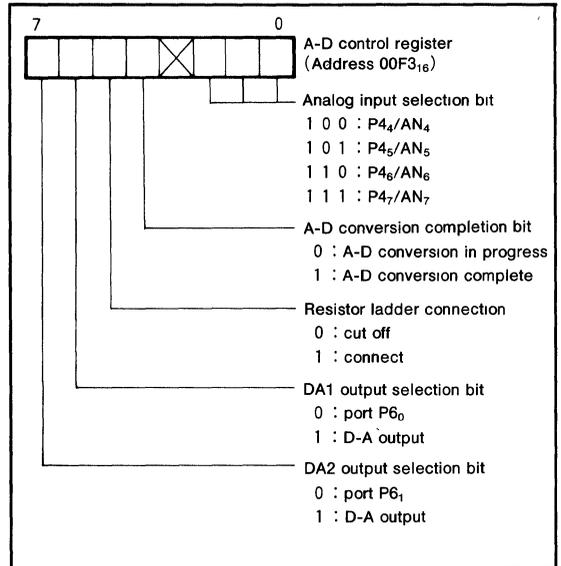


Fig.12 Structure of A-D control register

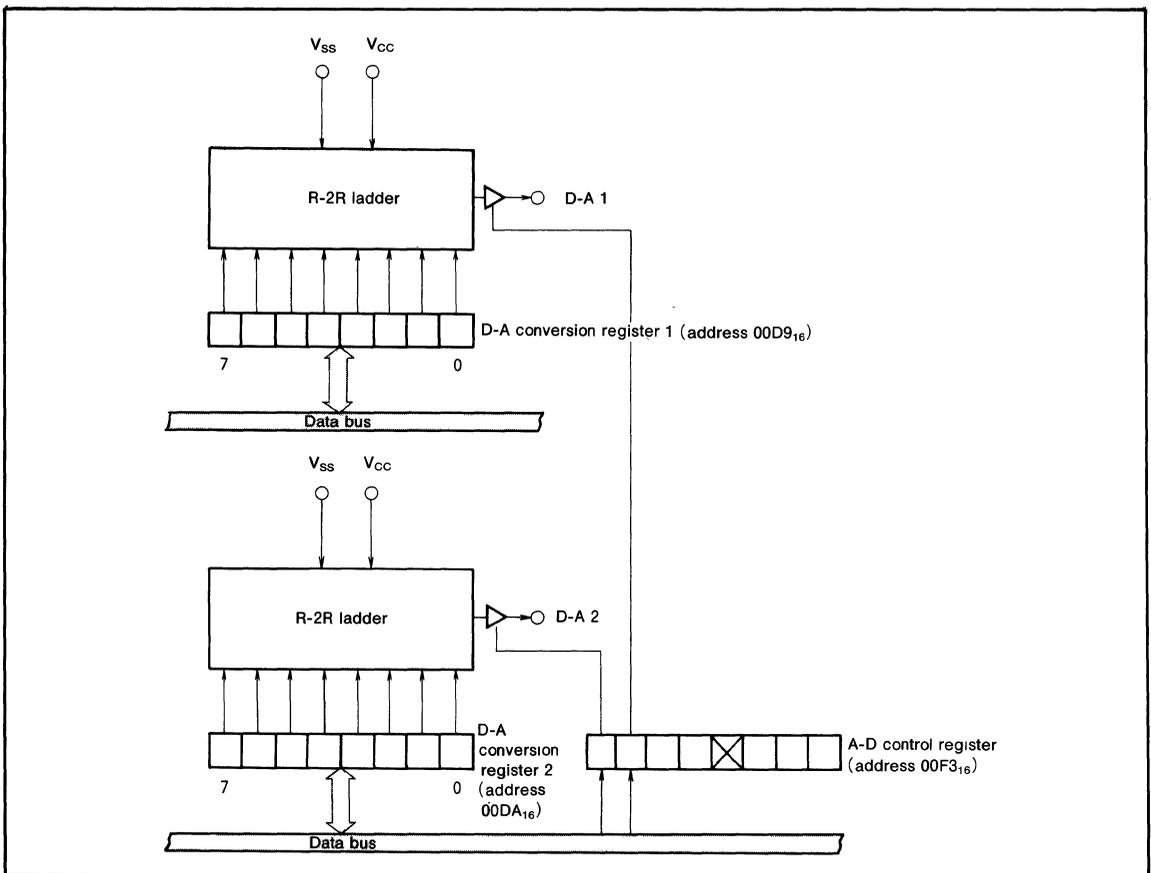


Fig.13 Block diagram of D-A conversion circuit

PWM OUTPUT CIRCUIT

(1) Introduction

The M37420M6-XXXSP is equipped with 14-bit PWM. The 14-bit resolution gives PWM the minimum resolution bit width of $0.25\mu\text{s}$ (for $X_{IN}=8\text{MHz}$) and a repeat period of $4096\mu\text{s}$.

Block diagram of the PWM is shown in Figure 14.

The PWM timing generator section applies control signals to PWM, using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pin PWM is in common with pin $P5_7$ (i.e. for PWM output, bit 0 of the special function selection register). When PWM is used for output, first set the higher 8-bit of the PWM1-H register (address $00F0_{16}$), then the lower 6-bit of the PWM1-L register (address $00F1_{16}$). Note that the higher 2 bits of these 8-bit registers are ignored when used 6-bit register.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data at addresses $00F0_{16}$ and $00F1_{16}$ are read, data in these latches has already been read allowing the data output by the PWM to be confirmed. When the 6-bit latch is being read, the upper 2 bits of the register becomes undefined. However, bit 7 of the PWM1-L register indicated the completion of the data transfer from the PWM1 register to the PWM1 latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) 14-bit PWM operation

The timing diagram of the 14-bit PWM1 is shown in Figure 15. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length N times τ is output every short area of $t=256\tau=64\mu\text{s}$ as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 15.)

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ . As a result, the short-area period $t(=64\mu\text{s})$, approx. 15.6kHz) becomes an approximately repetitive period.

(5) Output after reset

At reset the output of port $P5_7$ is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data	Area longer by τ than that of other $t_m(m=0\sim 63)$
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m=32$
0 0 0 0 1 0	$m=16, 48$
0 0 0 1 0 0	$m=8, 24, 40, 56$
0 0 1 0 0 0	$m=4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m=1, 3, 5, 7, \dots, 57, 59, 61, 63$

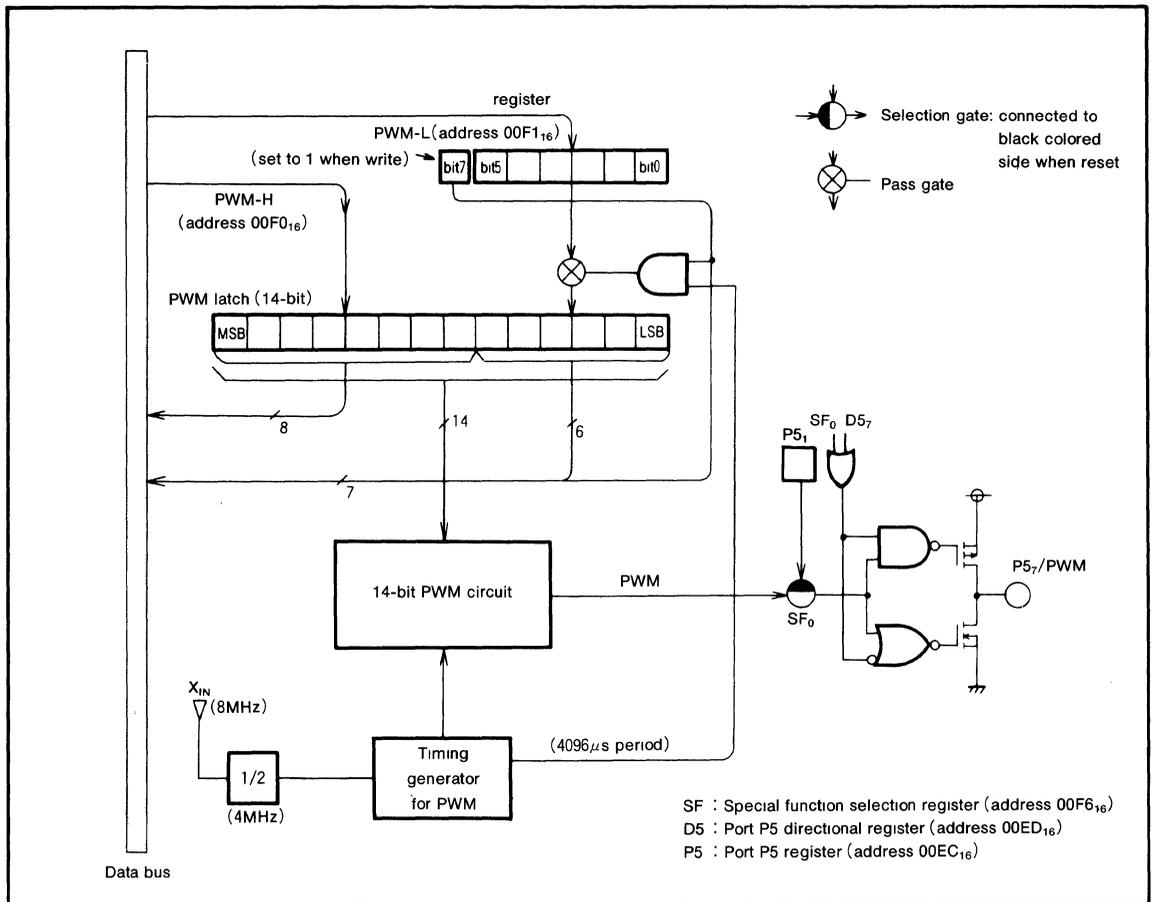


Fig.14 Block diagram of PWM circuit

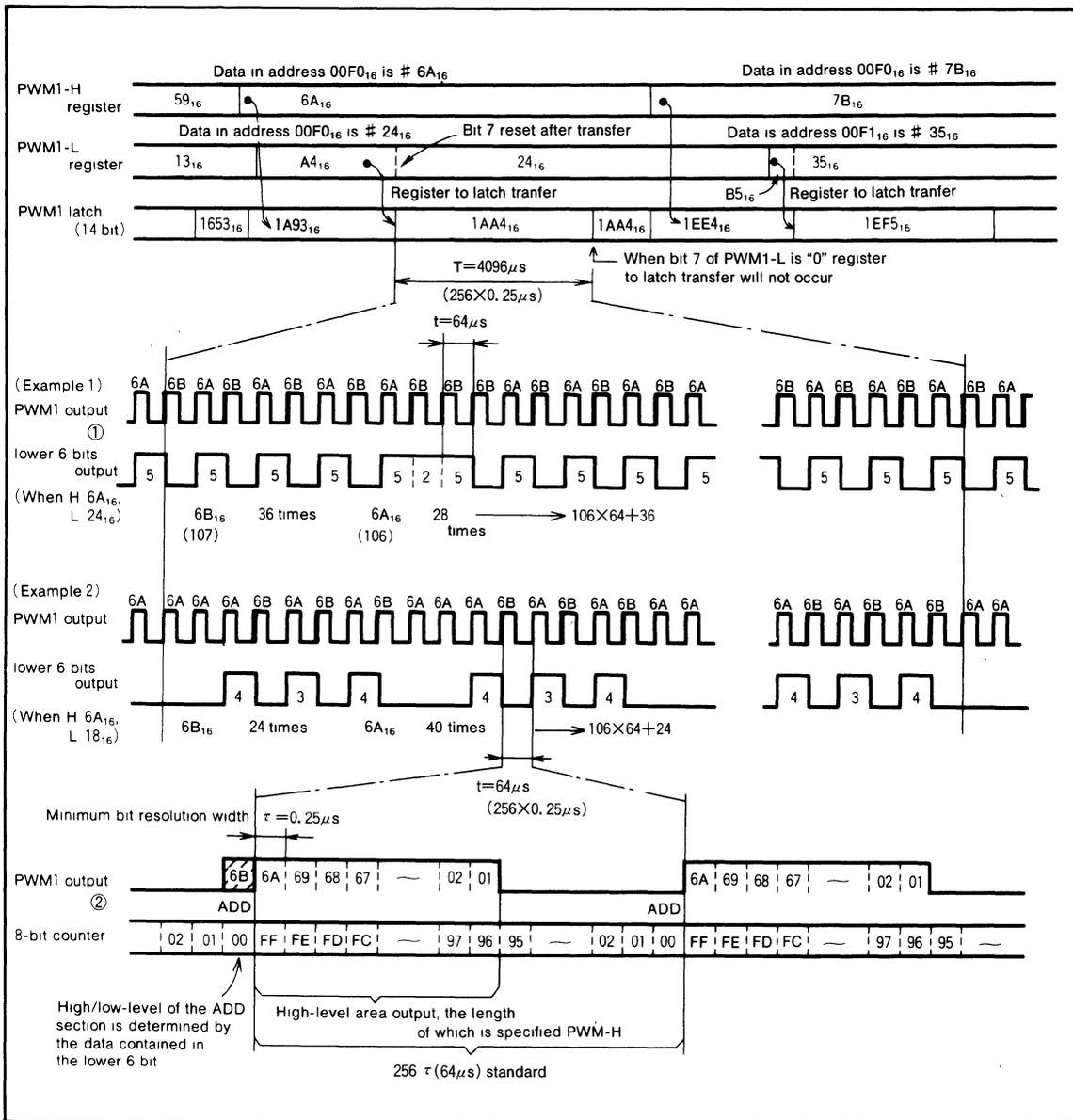


Fig.15 14-bit PWM timing diagram

V pulse and Y pulse generator

Pin 5₄ operates as the VPLS pin to output the V pulse and pin 5₃ operates as the T pin to which the trigger clock is input. These pins can be used as the V pulse output by setting bit 5 of the V pulse register (00DD₁₆) to "1". Pin P5₆ operates as the YPLS pin which outputs the Y pulse. It can be used as the Y pulse (VPF signal) output by setting bit 6 of the V pulse register to "1". Figure 17 shows the block diagram of the V pulse, Y pulse generator. Figure 18 shows the timing chart of the V pulse and Y pulse.

At the falling or rising edge of T, the VPP counter starts. By the overflow signal of the VPP counter, VPLS goes "H". By the overflow signal of VPP counter, the VPN counter starts. By the overflow signal of the VPN counter, VPLS goes "L". When the VPP counter or the VPN counter is counting, bit 4 of the V pulse register is "1".

The preset value of the VPP counter can be set by the 9-bit register with bit 1 of the V pulse register being the most significant bit and the V pulse preset value P (00DB₁₆) being the low-order eight bits. The preset value of the VPN counter can be set by the 9-bit register with bit 0 of the V pulse register being the least significant bit and the V pulse preset value N (00DB₁₆) being the low-order eight bits.

Note that values of bits 0 and 1 of the V pulse register are the current counting values in the VPP counter and the VPN counter, not the preset values of the counters.

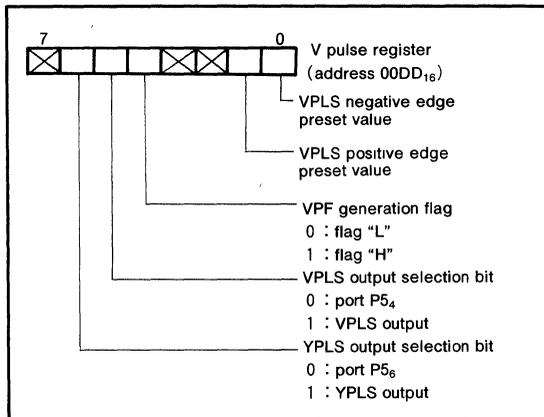


Fig.16 Structure of V pulse register

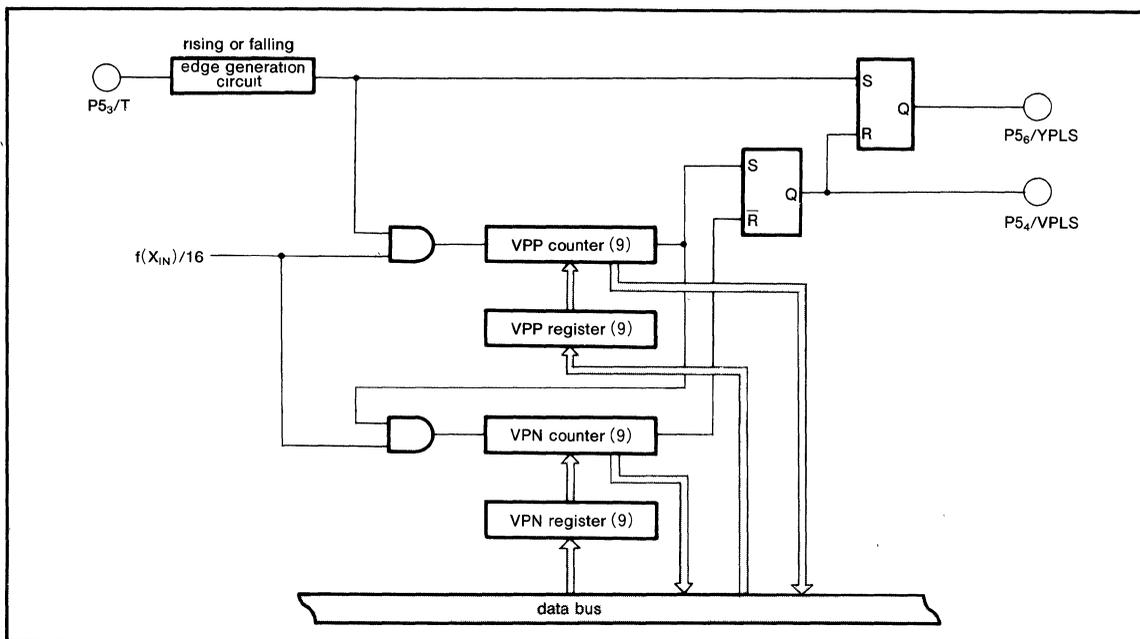


Fig.17 Block diagram of V pulse and Y pulse generator

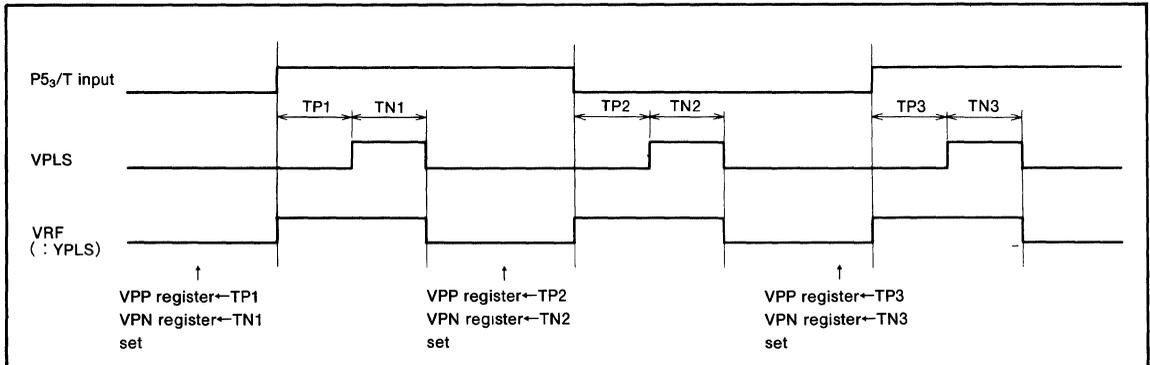


Fig.18 Timing chart of the V pulse and Y pulse

Edge sense input

Ports P5₀~P5₃ are the input ports having the edge sense function. To use these ports as edge sense inputs, read data from address 00ED₁₆. Address 00ED₁₆ has a latch. P5₀~P5₂ are set to "1" when the input changes from "H" to "L". P5₃ is set to "1" when the input changes from "H" to "L" and from "L" to "H". For the input pulse width, seven or more clock cycles are necessary. This latch is cleared by writing "0" at address 00ED₁₆ by the LDM or CLB instruction. When data is read from address 00ED₁₆, the high-order four bits are always "0's". At reset, the content of this latch is "0". When a read operation is performed from address 00EC₁₆, the normal level sense input will result.

External trigger output

Pin P5₅ operates as the pin Q which outputs the external trigger signal. Pin P5₃ operates as the pin T which inputs the trigger clock. By setting bit 5 of the special function selection register (address 00F6₁₆) to "1", these pins can be used as the external trigger outputs.

In the external trigger mode, every time the falling edge and rising edge of T are detected, the contents of P5₅ port output latch and the P5₅ direction register latch are output from the port. Depending on the combination of the port output latch and the directional register latch, the output to port P5₅ becomes as shown in Table 3. At reset, the content of this bit is "0".

Table 3. External trigger output

	output latch	0	1
directional register	0	high-impedance	high-impedance
	1	L	H

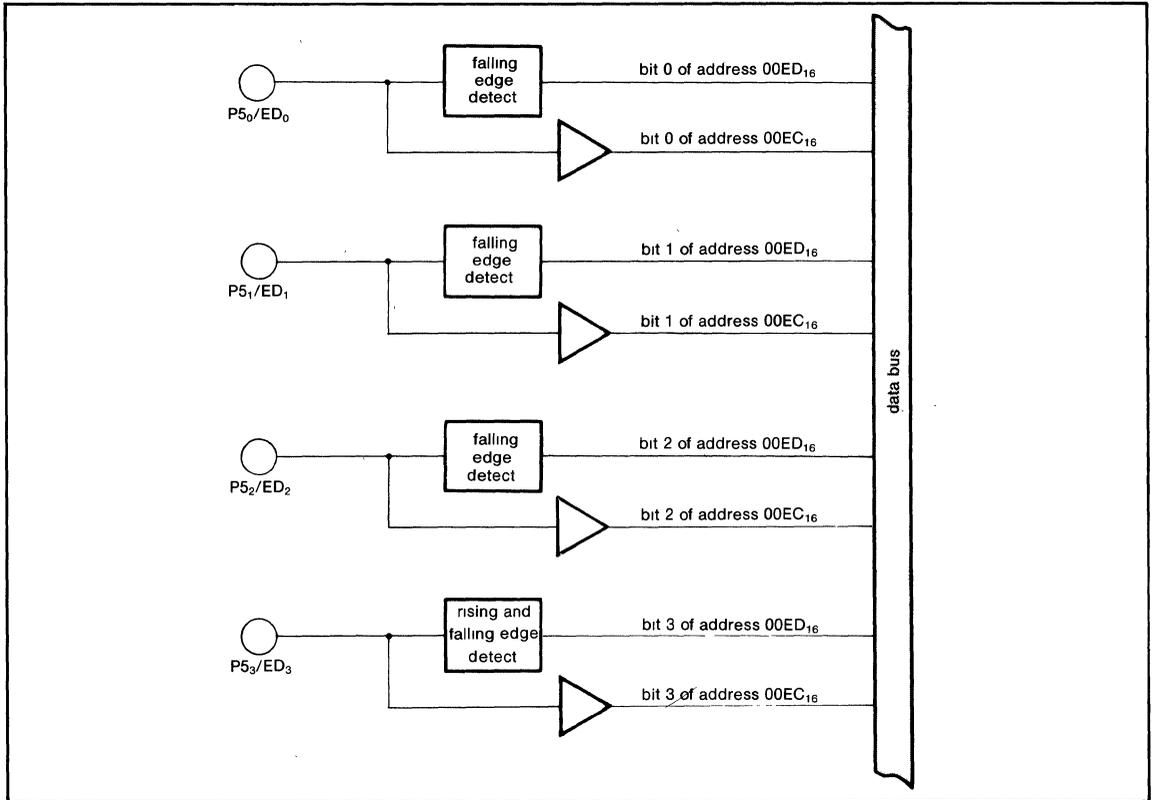


Fig.19 Block diagram of edge sense input

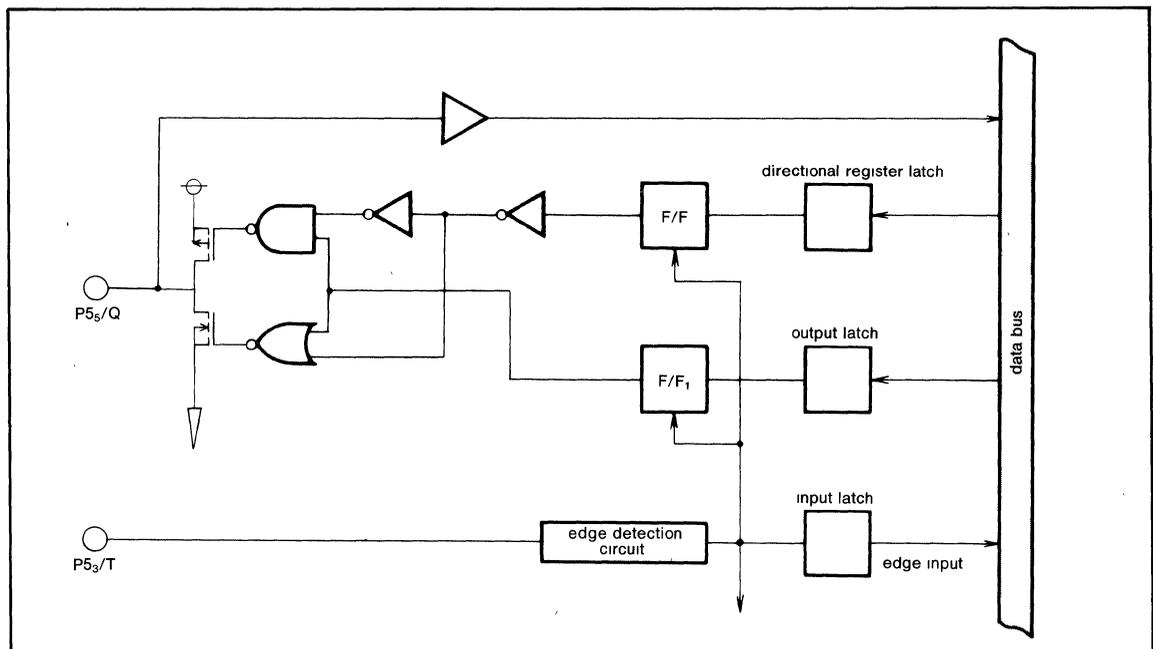


Fig.20 Block diagram of external trigger output

WATCHDOG TIMER

The watchdog timer provides the means to return to a reset condition when a program runs wild and the program will not run the normal loops.

The watchdog timer (address 00F4₁₆) is a 15-bit counter. The watchdog timer counts 1/16th the output frequency of the oscillator. The watchdog timer is set to 7FFF₁₆ when a reset is accomplished a write operation has been made to it. As well as any of the instructions that generate a write signal, such as STA, LDM, and CLB, can be used to write data to the watchdog timer. An output of the most significant bits of the watchdog timer is input to the reset circuit. When 262144 clock cycles have been counted, the most significant bit becomes "0" and reset is carried out. When reset is carried out, the watchdog timer is set to 7FFF₁₆ and reset is released. The program then begins again from reset vector address. Normally, the program is written so that a writing operation is made to the watchdog timer prior to the most significant bit's becoming "0"

Since execution of the STP instruction causes both the clock and the watchdog timer to stop, an option is offered where the STP instruction can be disabled.

RESET CIRCUIT

The M37420M6-XXXSP is reset according to the sequence shown in Figure 21. It starts the program from the address formed by using the content of address FFFF₁₆ as the high order address and the content of the address FFFE₁₆ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for more than 2 μ s while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 22.

An example of the reset circuit is shown in Figure 23. When the power on reset is used, the $\overline{\text{RESET}}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

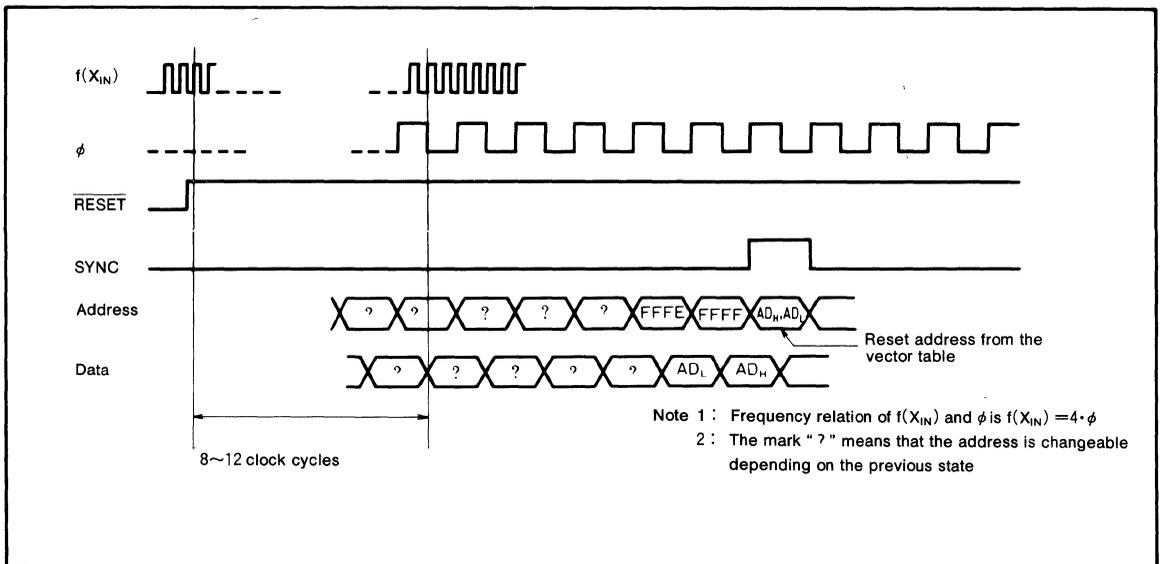


Fig. 21 Timing diagram at reset

M37420M4-XXXSP
M37420M6-XXXSP

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	address	
(1) D-A conversion register 1	(D9 ₁₆)	00 ₁₆
(2) D-A conversion register 2	(DA ₁₆)	00 ₁₆
(3) Port P0 directional register	(E1 ₁₆)	00 ₁₆
(4) Port P1 directional register	(E3 ₁₆)	00 ₁₆
(5) Port P2 directional register	(E5 ₁₆)	00 ₁₆
(6) Port P3 directional register	(E9 ₁₆)	00 ₁₆
(7) Port P4 directional register	(EB ₁₆)	00 ₁₆
(8) Port P5 latch/directional register	(ED ₁₆)	00 ₁₆
(9) Port P6 directional register	(EF ₁₆)	00 ₁₆
(10) A-D control register	(F3 ₁₆)	0 0
(11) Watchdog timer	(F4 ₁₆)	7FFF ₁₆
(12) Serial I/O mode register	(F5 ₁₆)	0 0 0 0 0 0 0 0
(13) Special function selection register	(F6 ₁₆)	0 0 0 0 0
(14) Prescaler X	(FC ₁₆)	FF ₁₆
(15) Timer X	(FD ₁₆)	01 ₁₆
(16) Interrupt control register	(FE ₁₆)	00 ₁₆
(17) Timer control register	(FF ₁₆)	00 ₁₆
(18) Interrupt disable flag on processor status register	(PS)	1
(19) Program counter	(PC _H)	Contents of address FFFF ₁₆
	(PC _L)	Contents of address FFFE ₁₆

Note 1 : Port P6 is the high-impedance state during reset
After return from reset, it is "FF₁₆".

Fig.22 Internal state of microcomputer at reset

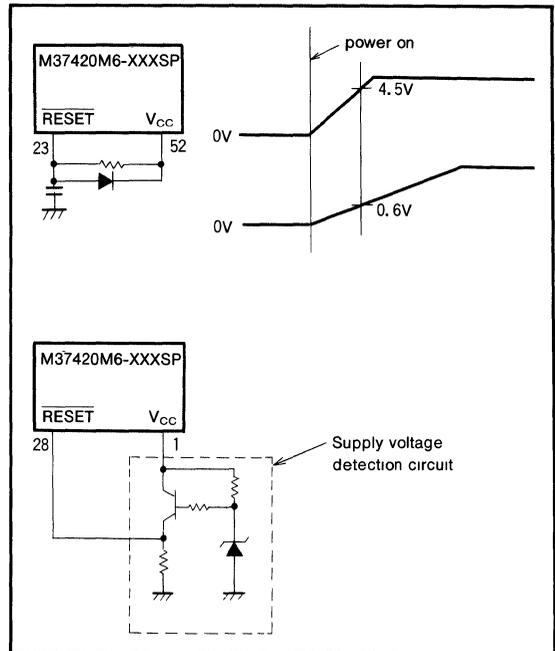


Fig.23 Example of reset circuit

I/O PORTS

- (1) Port P0
 Port P0 is an 8-bit I/O port with N-channel open drain output.
 As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address 00E0₁₆. Port P0 has a directional register (address 00E1₁₆) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.
- (2) Port P1
 Port P1 is a 6-bit I/O port and has the same function as Port P0.
- (3) Port P2
 Port P2 has the same function as Port P0, but it has CMOS output.
- (4) Port P3
 Port P3 has the same function as port P0. Port P3 can also be used as serial I/O, INT₁, INT₂ and I/O pins for timer X.
- (5) Port P4
 Port P4 is a 4-bit I/O port and has the same function as port P0. But P4₇ through P4₄ can also be used as analog input pins AN₇ through AN₄.
- (6) Port P5
 Port P5₃~P5₀ is an input port and can also be used as edge sense inputs. In such a case, reading is begun from 00ED₁₆.
 When port P5 is used as level sense input, read the contents of the address 00EC₁₆.
 P5₇~P5₄ have the same function as port P0 except that they are I/O ports and double-functioning. The PWM output pin operates as P5₇, the Y pulse output pin as P5₆, and the V pulse output pin as P5₄. These ports are used by selecting the function through the special function selection register and the V pulse register. For details, see the descriptions of the PWM and the V pulse, Y pulse generator. The external trigger output pin operates as P5₅. The external trigger output mode can be selected by setting bit 2 of the special function select register to "1". At reset, all of P5₇~P5₄ are in the state where the normal I/O port function is selected. The output is the CMOS output.
- (7) Port P6
 Port P6 is a 4-bit I/O port and has the same function as P0 except that P6₀ and P6₁ can be used as D-A output pin.

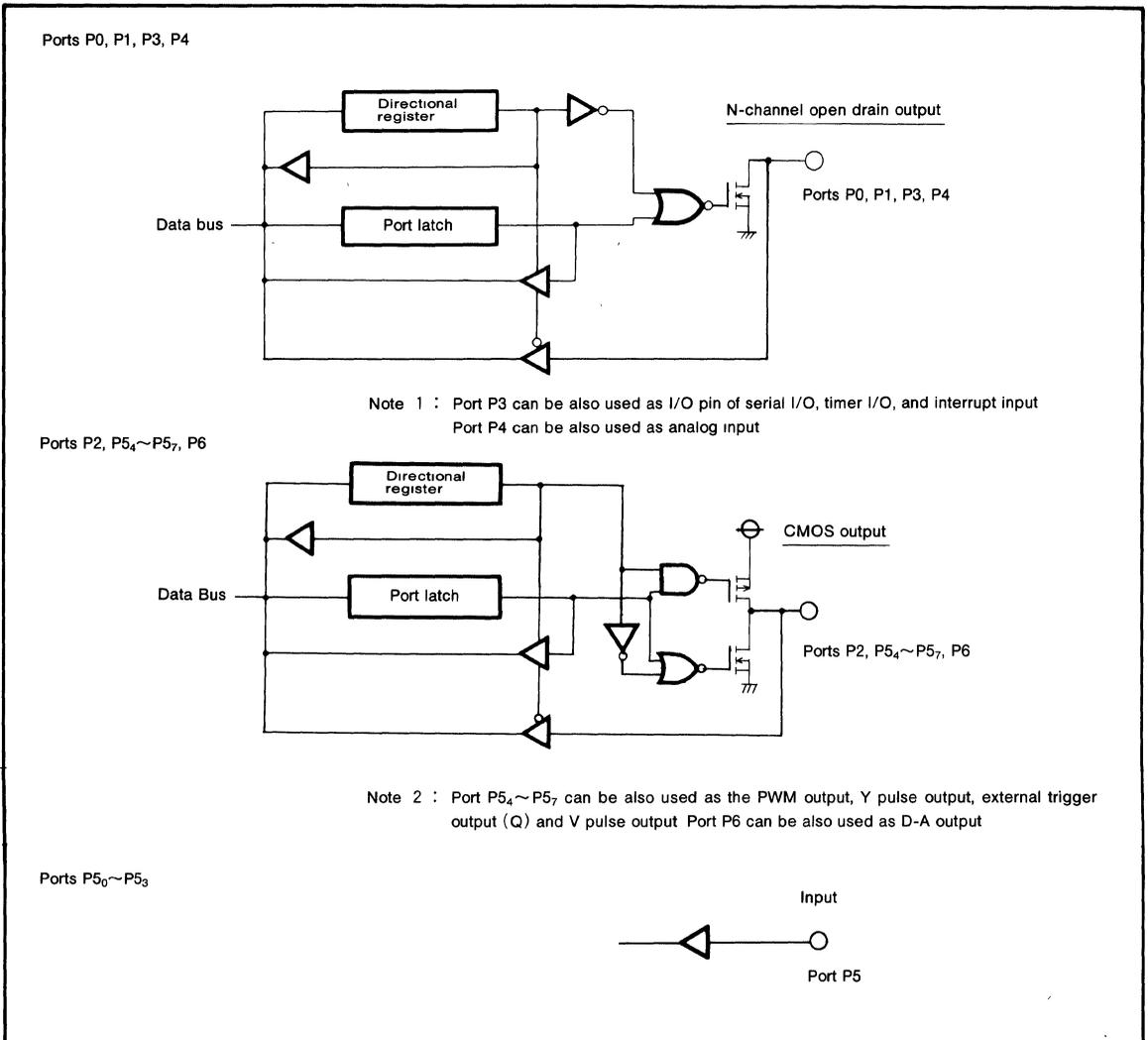


Fig.24 Block diagram of ports P0~P6

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 27.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16} , respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 25.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 26.

X_{IN} is the input, and X_{OUT} is open.

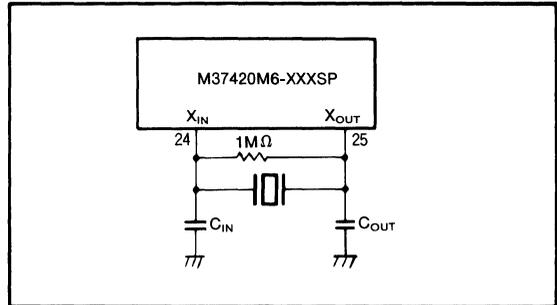


Fig.25 External ceramic resonator circuit

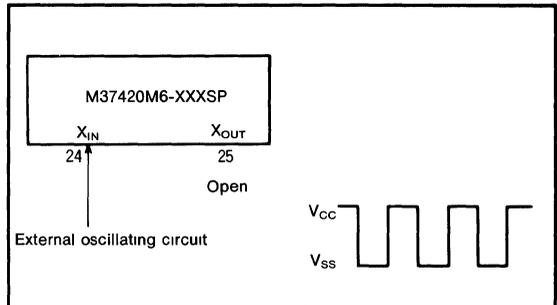


Fig.26 External clock input circuit

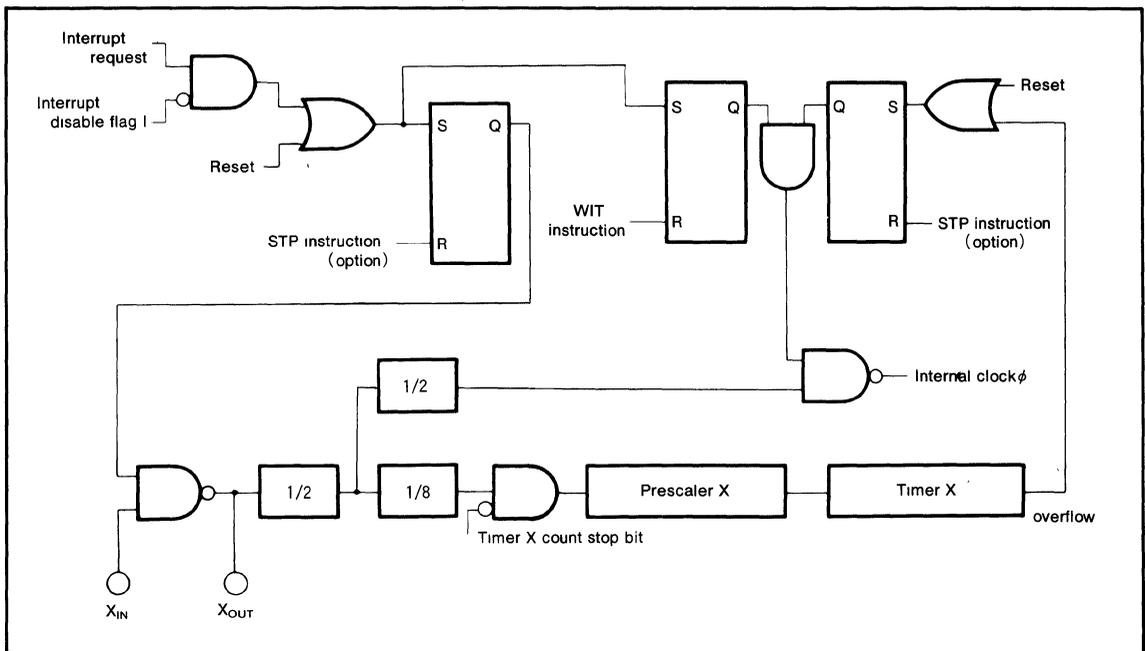


Fig.27 Block diagram of the clock generating circuit

PROGRAMMING NOTES

- (1) The frequency ratio of the timer and the prescaler is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
- (4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion. And during A-D conversion, don't use STP or WIT instruction.
- (7) Values of bits 0 and 1 of the V pulse register are the current counting values in the VPP counter and the VPN counter, not the preset values.

Therefore, if the read values of bits 0 and 1 are written as they are when other bits in the V pulse register is to be set, the preset values may be changed.

This must be kept in mind before executing the SEB or CLB instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3sets

Write the following option on the mask ROM confirmation form

- STP instruction option
- Reset option for watchdog timer

M37420M4-XXXSP

M37420M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	-0.3~7	V
V_I	Input voltage X_{IN}		-0.3~7	V
V_I	Input voltage $P2_0\sim P2_7, P4_2\sim P4_7, P5_4\sim P5_7, P6_0\sim P6_3$		-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage $P0_0\sim P0_7, P1_0\sim P1_5, P3_0\sim P3_7, P4_0, P4_1, P5_0\sim P5_7$		-0.3~13	V
V_I	Input voltage $CNV_{SS}, RESET$		-0.3~13	V
V_O	Output voltage $P2_0\sim P2_7, P4_2\sim P4_7, P5_4\sim P5_7, P6_0\sim P6_3$		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage $P0_0\sim P0_7, P1_0\sim P1_5, P3_0\sim P3_7$		-0.3~13	V
P_d	Power dissipation	$T_a=25^\circ\text{C}$	1000	mW
T_{opr}	Operating temperature		-10~70	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~125	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V\pm 10\%$, $T_a=-10\sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0\sim P0_7, P1_0\sim P1_5, P2_0\sim P2_7, P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7, RESET, X_{IN}, P6_0\sim P6_3$	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7, CNV_{SS}, P6_0\sim P6_3$	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage RESET	0		$0.12V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}	0		$0.16V_{CC}$	V
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7, P1_0\sim P1_5, P2_0\sim P2_7, P3_0\sim P3_7, P4_0\sim P4_7$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0\sim P6_3$ (Note 2)			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7, P1_0\sim P1_5, P2_0\sim P2_7, P3_0\sim P3_7, P4_0\sim P4_7$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0\sim P6_3$ (Note 1)			5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0\sim P2_7, P5_4\sim P5_7, P6_0\sim P6_3$ (Note 2)			-10	mA
$I_{OH(avg)}$	"H" average output current $P2_0\sim P2_7, P5_4\sim P5_7, P6_0\sim P6_3$ (Note 1)			-5	mA
$f(X_{IN})$	Internal clock oscillating frequency			8	MHz

Note 1 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms

Note 2 : Total of "L" output current I_{OL} of ports $P0, P1, P2, P3, P4, P6,$ and PWM is 80mA max
Total of "H" output current I_{OH} of port $P2$ is 50mA max

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=8MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage P ₂₀ ~P ₂₇ , P ₅₄ ~P ₅₇ , P ₆₀ ~P ₆₃	$I_{OH}=-10mA$	3			V
V_{OL}	"L" output voltage P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₅ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₄ ~P ₅₇ , P ₆₀ ~P ₆₃	$I_{OL}=10mA$			2	V
$V_{T+}-V_{T-}$	Hysteresis P ₃₀ , P ₃₁	When used as INT input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis P ₃₆	When used as CLK ₂ input	0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis P ₃₃	When used as CNTR input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis P ₅₃	When used as T input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis RESET			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X _{IN}		0.1		0.5	V
I_{IL}	"L" input current P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₅ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₃ , PWM	$V_i=0V$			-5	μA
I_{IL}	"L" input current RESET, X _{IN}	$V_i=0V$			-5	μA
I_{IH}	"H" input current P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₅ , P ₃₀ ~P ₃₇ , P ₅₀ ~P ₅₃	$V_i=12V$			12	μA
I_{IH}	"H" input current RESET, X _{IN} , P ₂₀ ~P ₂₇ , P ₄₄ ~P ₄₇ , P ₅₄ ~P ₅₇ , P ₆₀ ~P ₆₃	$V_i=5V$			5	μA
V_{RAM}	RAM retention voltage	At clock stop	2			V
I_{CC}	Supply current	ϕ , X _{OUT} , and D-A pins opened, other pins at V_{SS} , and A-D converter in the finished condition $f(X_{IN})=8MHz$ Square wave		3	6	mA

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=AV_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=8MHz$, unless otherwise noted)

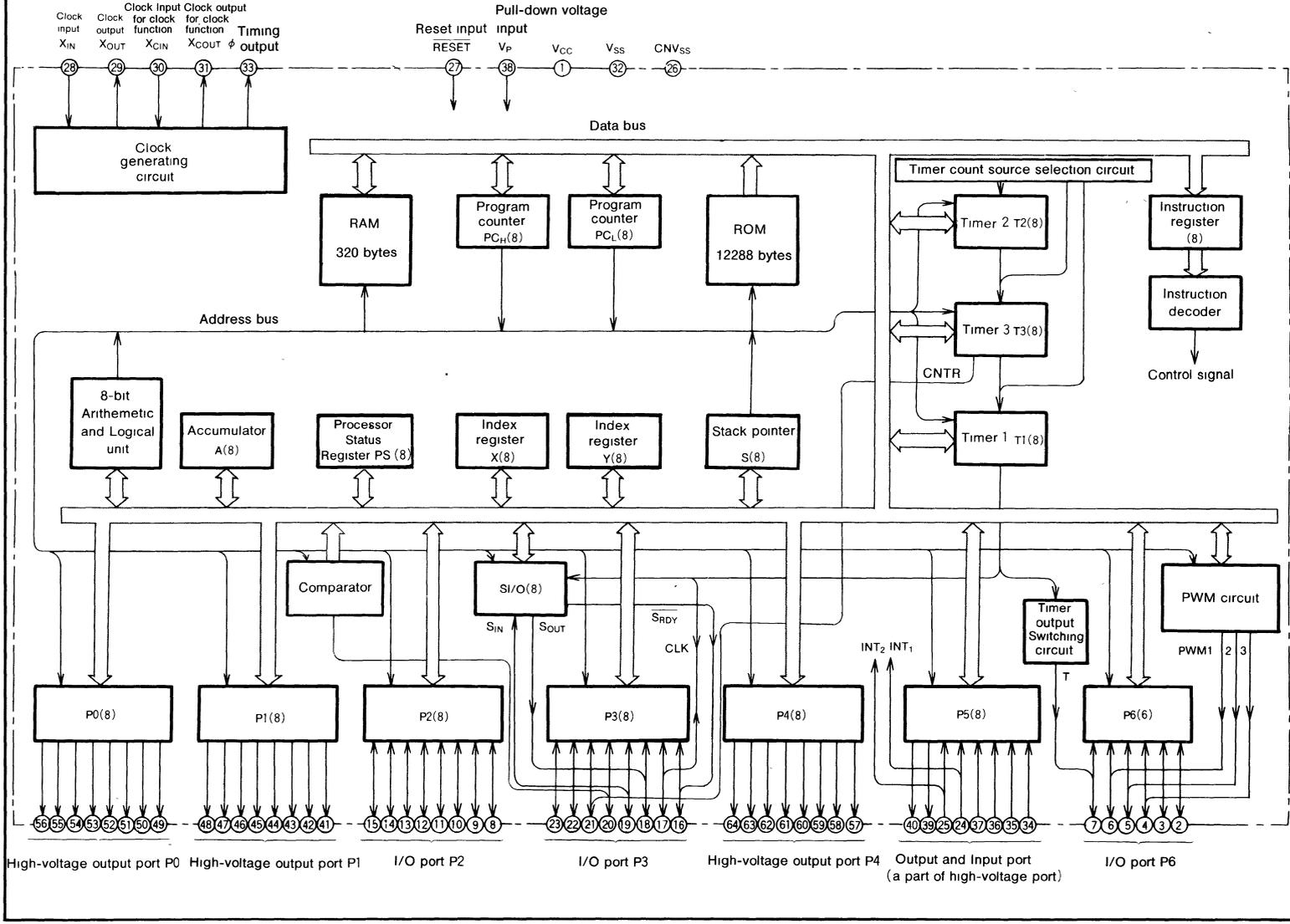
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistance value	$V_{REF}=V_{CC}$	2		10	k Ω
t_{CONV}	Conversion time				25	μs
V_{IA}	Analog input voltage		0		V_{CC}	V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=AV_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=8MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Error in full scale range	$V_{REF}=V_{CC}$			± 2	%
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
R_O	Output resistance	$V_{REF}=V_{CC}$	1	2	4	k Ω



M37421M6-XXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MITSUBISHI MICROCOMPUTERS
M37421M6-XXXSP/FP

MITSUBISHI MICROCOMPUTERS M37421M6-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37421M6-XXXSP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		0.95 μ s (minimum instructions, at 4.2MHz frequency)
Clock frequency		4.2MHz
Memory size	ROM	12288 bytes
	RAM	320 bytes
Input/output ports	P0, P1, P4	Output 8-bit \times 3 (high-voltage P-channel open drain, $V_{CC}-38V$)
	P2, P3	I/O 8-bit \times 2 (P3 can partially be used as among serial I/O, clock input for timer 3 and normal I/O.)
	P5 ₀ , P5 ₁	Output 2-bit \times 1 (high-voltage P-channel open drain, $V_{CC}-38V$)
	P5 ₂ , P5 ₃	Input 2-bit \times 1 (can be used as an input for either INT ₂ or INT ₁ .)
	P5 ₄ ~P5 ₇	Input 4-bit \times 1
	P6	I/O 6-bit \times 1 (can be used as T ₁ output or PWM output)
Serial I/O		8-bit \times 1
Timers		8-bit timer \times 3 (\times 2, when used as serial I/O)
Subroutine nesting		64 levels (max)
Interrupt		Two external interrupts, three internal timer interrupts (or timer \times 2, serial I/O \times 1)
Clock generating circuit		Two built-in circuits (externally connected ceramic or quartz crystal oscillator)
Supply voltage (Note)		2.7~5.5V
Power dissipation	at high-speed operation	30mW (clock frequency $X_{IN}=4.2MHz$)
	at low-speed operation	0.3mW (clock frequency $X_{CIN}=32kHz$)
	at stop mode	5 μ W (when clock is stopped)
Input/Output characteristics	Input/Output voltage	12V (input/output P2, P3, P5 ₂ , P5 ₃ except P3 ₃)
		$V_{CC}-38V$ (P0, P1, P4, P5 ₀ , P5 ₁)
		-0.3V~ $V_{CC}+0.3V$ (input/output P3 ₃ and P6)
	Output current	10mA (P2, P3 N-channel open drain)
		-18mA (P0, P1 high-voltage P-Channel open drain)
-12mA (P4, P5 ₀ , P5 ₁ high-voltage P-Channel open drain)		
	0.5~-0.5mA (P6 CMOS tri-states)	
Operating temperature range		-10~70°C
Device structure		CMOS silicon gate process
Package	M37421M6-XXXSP	64-pin shrink plastic molded DIP
	M37421M6-XXXFP	72-pin plastic molded QFP

Note : At $f(X_{IN})=4.2MHz$ and $f(X_{CIN})=32kHz$, selection of internal clock ϕ is guaranteed the following supply voltage
 $f(X_{IN})=4.2MHz$ ($\phi=2.1MHz$) : $V_{CC}=4.5\sim 5.5V$
 $f(X_{CIN})=32kHz$ ($\phi=16kHz$) : $V_{CC}=2.7\sim 5.5V$

MITSUBISHI MICROCOMPUTERS
M37421M6-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 4.5~5.5V at f(X _{IN})=4.2MHz and 2.7~5.5V below f(X _{CIN})=32kHz to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is usually connected to V _{SS}
V _P	Pull-down supply	Input	Pull down supply for the pull-down resistor of ports P0, P1, P4, P5 ₀ and P5 ₁
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2 μ s (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin $\phi=2\text{MHz}$ (when X _{IN} =4MHz)
X _{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{CIN} and X _{COUT} pins If an external clock is used, the clock source should be connected to the X _{CIN} pin and the X _{COUT} pin should be left open This clock can be used as a program controlled the system clock
X _{COUT}	Clock output for clock function	Output	
P0 ₀ ~P0 ₇	Output port P0	Output	Port P0 is an 8-bit output port Output structure is high-voltage P-channel open drain A pull-down resistor is built in between the V _P pin and this port At reset, this port is set to a "L" level
P1 ₀ ~P1 ₇	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is N-channel open drain
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P2 When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as $\overline{\text{S}}_{\text{RDY}}$, CLK, S _{OUT} , and S _{IN} pins, respectively P3 ₃ works as an analog input for comparator, and P3 ₂ works as a clock input for timer 3
P4 ₀ ~P4 ₇	Output port P4	Output	Port P4 is an 8-bit output port and has basically the same functions as port P0
P5 ₀ , P5 ₁	Output port P5	Output	Bit 0 and 1 of port P5 are 2-bit output port and has basically the same functions as port P0
P5 ₂ /INT ₂ , P5 ₃ /INT ₁	Input port P5	Input	Bit 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs
P5 ₄ ~P5 ₇		Input	Bit 4~7 of port P5 are 4-bit input port
P6 ₀ ~P6 ₇	I/O port P6	I/O	Port P6 is a 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS tri-state output P6 ₀ , P6 ₁ , P6 ₂ , P6 ₃ can be programmed to function as timer output pin (T), PWM output pins (PWM1, PWM2, and PWM3), respectively

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37421 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used

The STP instruction can be used.

MEMORY

- Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- RAM

RAM is used for data storage as well as a stack area.

- ROM

ROM is used for storing user programs as well as the interrupt vector area.

- Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

- Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

- Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

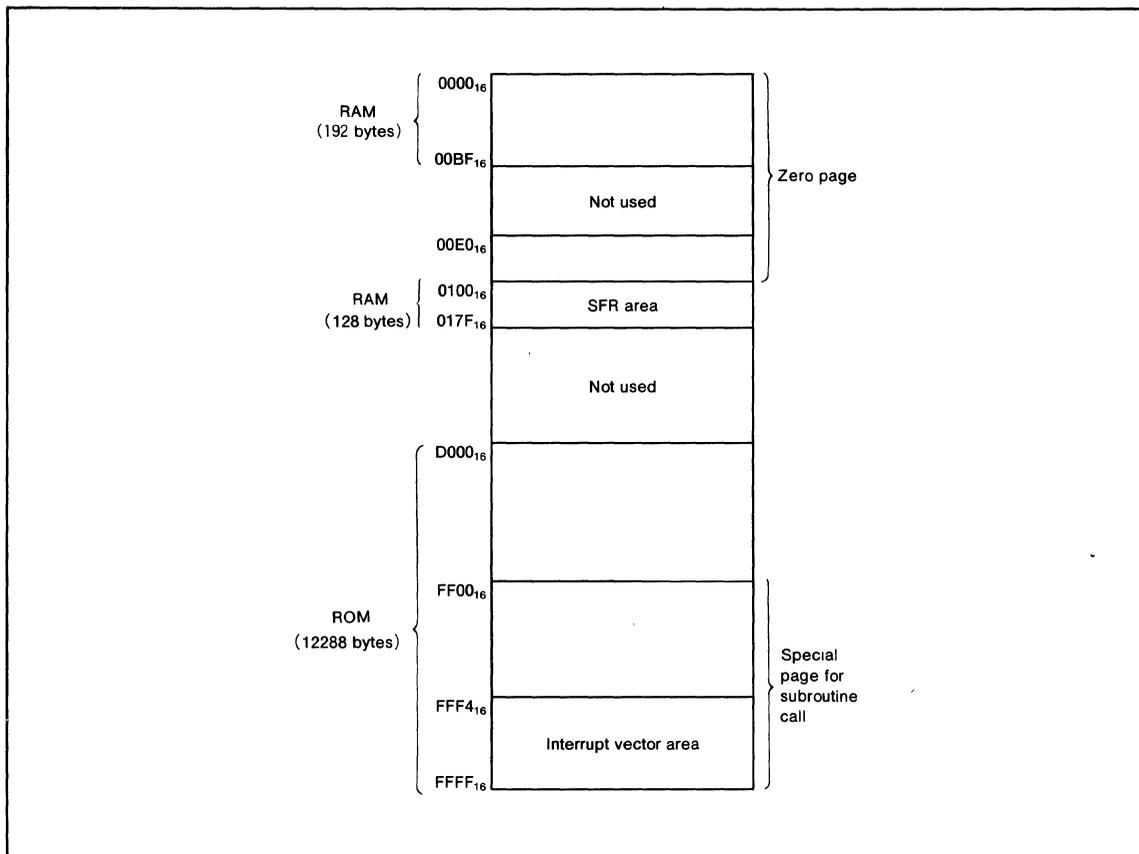


Fig.1 Memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

00E0 ₁₆	Port P0	00F0 ₁₆	PWM1-H register
00E1 ₁₆		00F1 ₁₆	PWM1-L register
00E2 ₁₆	Port P1	00F2 ₁₆	PWM2 register
00E3 ₁₆		00F3 ₁₆	PWM3 register
00E4 ₁₆	Port P2	00F4 ₁₆	
00E5 ₁₆	Port P2 directional register	00F5 ₁₆	PWM output mode register
00E6 ₁₆		00F6 ₁₆	Serial I/O mode register
00E7 ₁₆		00F7 ₁₆	Serial I/O register
00E8 ₁₆	Port P3	00F8 ₁₆	
00E9 ₁₆	Port P3 directional register	00F9 ₁₆	Serial I/O register 2
00EA ₁₆	Port P4	00FA ₁₆	Timer 1
00EB ₁₆		00FB ₁₆	Comparator register
00EC ₁₆	Port P5	00FC ₁₆	Timer 2
00ED ₁₆		00FD ₁₆	Timer 3
00EE ₁₆	Port P6	00FE ₁₆	Interrupt control register
00EF ₁₆	Port P6 directional register	00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

INTERRUPT

The M37421M6-XXXSP can be interrupted from seven sources; INT₁, timer 3, timer 2, timer 1/serial I/O, or INT₂/BRK instruction.

The value of bit 2 of the serial I/O mode register (address 00F6₁₆) determine whether the interrupt is from timer 1 or from serial I/O. When bit 2 is "0" the interrupt is from timer 1, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

- (1) When the level of pins INT₁ and INT₂ change.
- (2) When the contents of timer 3, timer 2, timer 1 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but cannot be set by the program. However, the interrupt enable bit can be set and reset by the program.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
RESET	1	FFFF ₁₆ , FFFE ₁₆
INT ₁	2	FFFD ₁₆ , FFFC ₁₆
Timer 3	3	FFFB ₁₆ , FFFA ₁₆
Timer 2	4	FFF9 ₁₆ , FFF8 ₁₆
Timer 1 or serial I/O	5	FFF7 ₁₆ , FFF6 ₁₆
INT ₂ (BRK)	6	FFF5 ₁₆ , FFF4 ₁₆

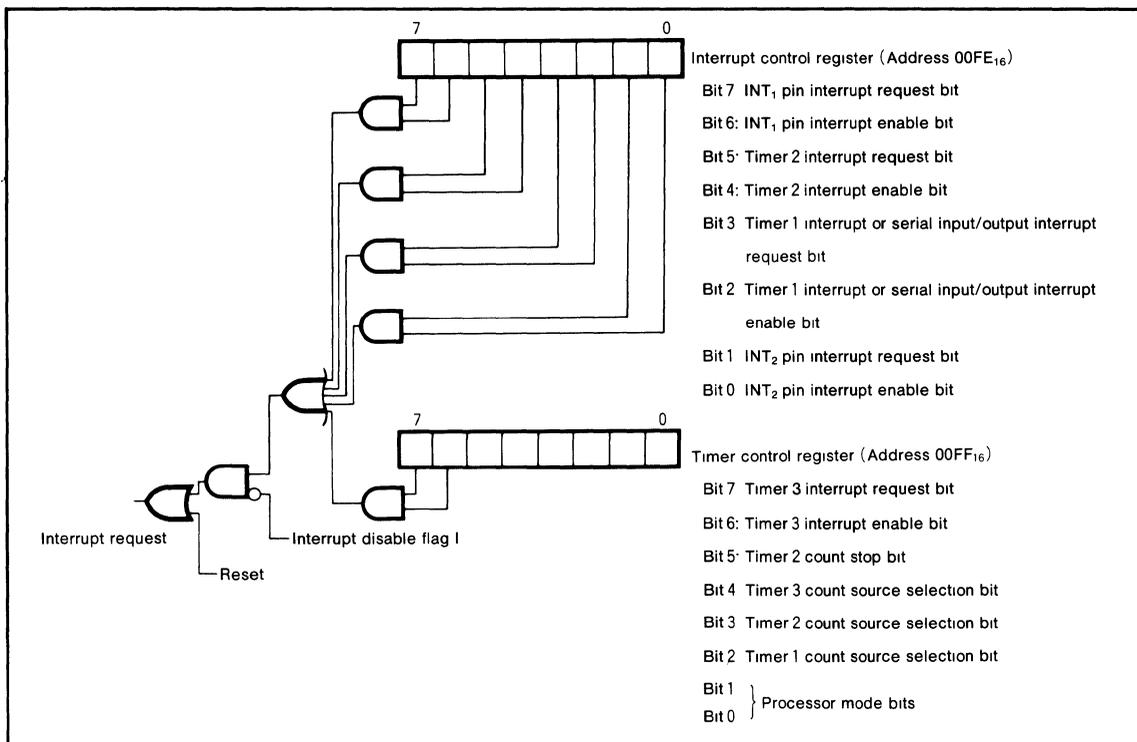


Fig.3 Interrupt control

The change in level at which the INT pins generate an interrupt varies according to the content of bits 4 and 5 of the PWM output mode register (address 00F5₁₆). When these bits are "0", the interrupt request is generated when INT changes from high-level to low-level. When these bits are "1", the interrupt request is generated when INT changes from low-level to high-level. Bits 4 (PM₄) and 5 (PM₅) correspond to INT₁ and INT₂ respectively.

Since the BRK instruction and the INT₂ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if INT₂ generated the interrupt.

TIMER

The M37421M6-XXXSP has three timers; timer 1, timer 2, and timer 3. Since P3 (in serial I/O mode) and timer 1 use some of the same architecture, they cannot be used at the same time (see serial I/O section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address 00FF₁₆), as shown in Figure 5.

A block diagram of timer 1 through 3 is shown in Figure 4. All of the timers are down count timers and have 8-bit latches. When a timer counter reaches "0", the contents of the reload latch are loaded into the timer at the next clock pulse. The division ratio of the timers is 1/(n+1), where n is the contents of the timer latch.

The timer interrupt request bit is set to "1" at the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses 00FE₁₆ and 00FF₁₆, respectively (see Interrupt section). The starting/stopping of timer 2 can be controlled by bit 5 of the timer control register. If bit 5 (address 00FF₁₆) is "0", the timer starts counting and when bit 5 is "1", the timer stops. The count source of timer 3 can be controlled by bit 4 of the timer control register. If bit 4 (address 00FF₁₆) is "1", the timer counts from the P3₂/CNTR pin.

When the STP instruction is executed, or after reset, the timer 2 and timer 3 latch are set to FF₁₆ and 07₁₆, respectively.

After a STP instruction is executed, timer 2, timer 3, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if the timer 3 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 2 count stop bit) and bit 4 of the interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

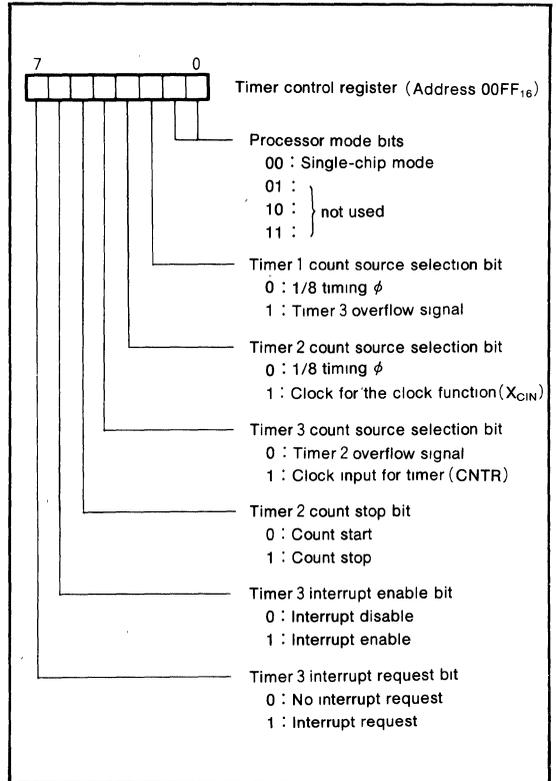


Fig.4 Structure of timer control register

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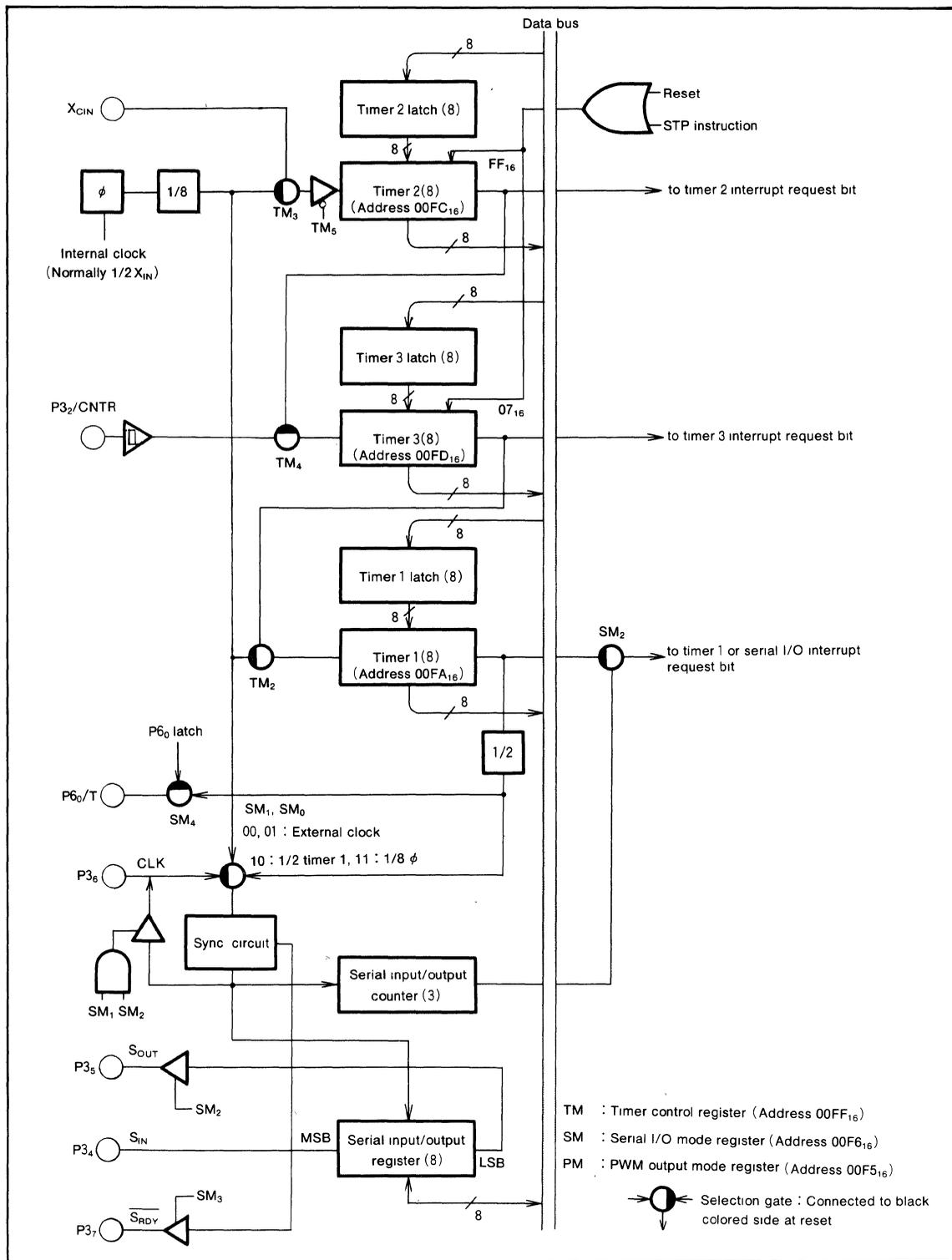


Fig.5 Block diagram of timer 1, timer 2, timer 3

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SERIAL I/O

A block diagram of the serial I/O is shown in Figure 6. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O pins (S_{OUT} , S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 1, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], timing ϕ divided by 4, becomes the clock.

Bit 2 and 3 decide whether parts of $P3$ will be used as a serial I/O or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 1. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY}}$) or used as normal I/O pin

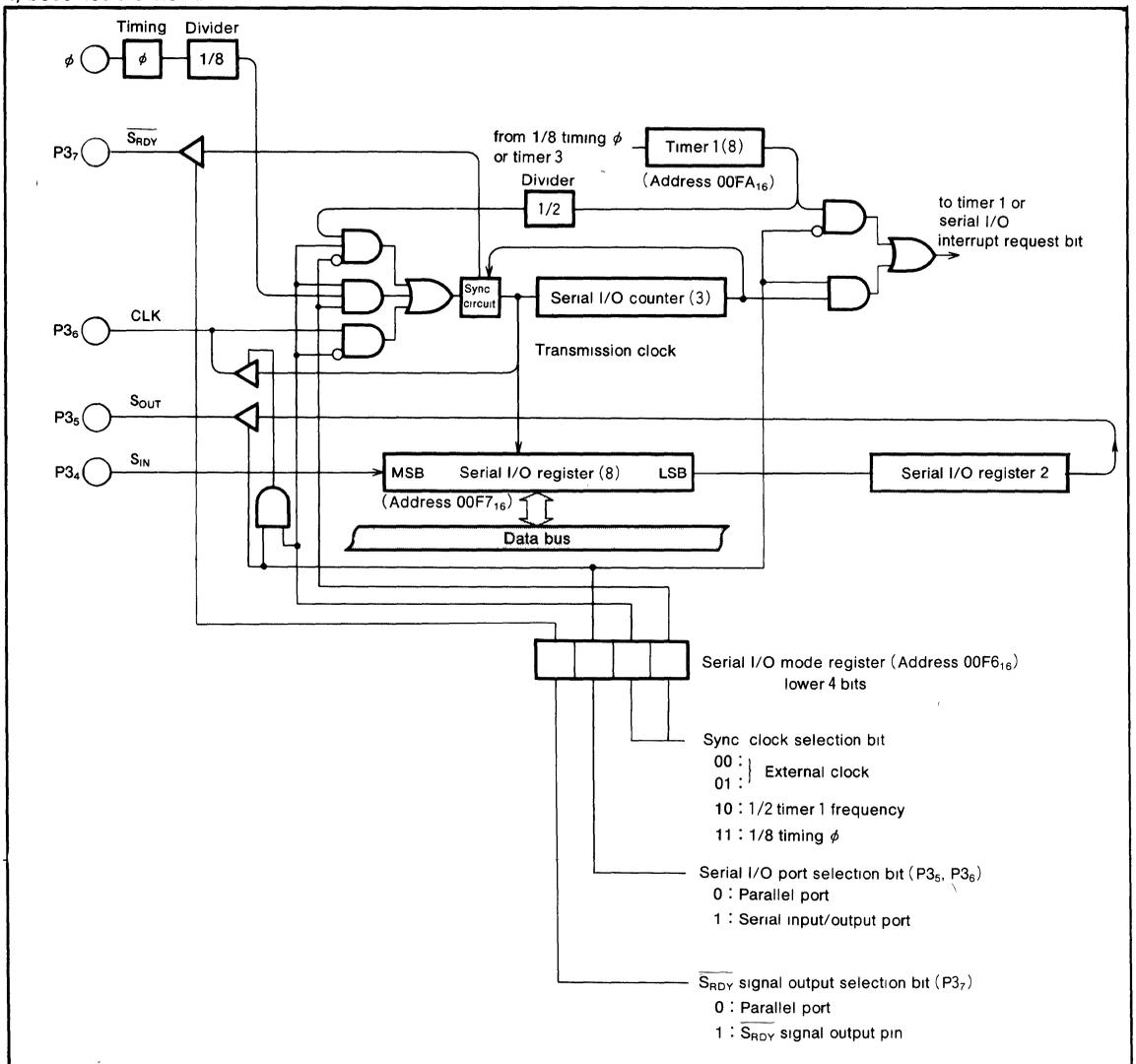


Fig.6 Block diagram of serial I/O

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(bit 3=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address 00F7₁₆). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37421M6-XXXSP is ready to receive the external serial data. When "H" level is input to CLK pin and the dummy data is written to serial I/O register 2, the output of S_{OUT} becomes "H" before/after the data transmission. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to P3₅. During the rising

edge of this clock, data can be input from P3₄ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M37421M6-XXXSPs is shown in Figure 8.

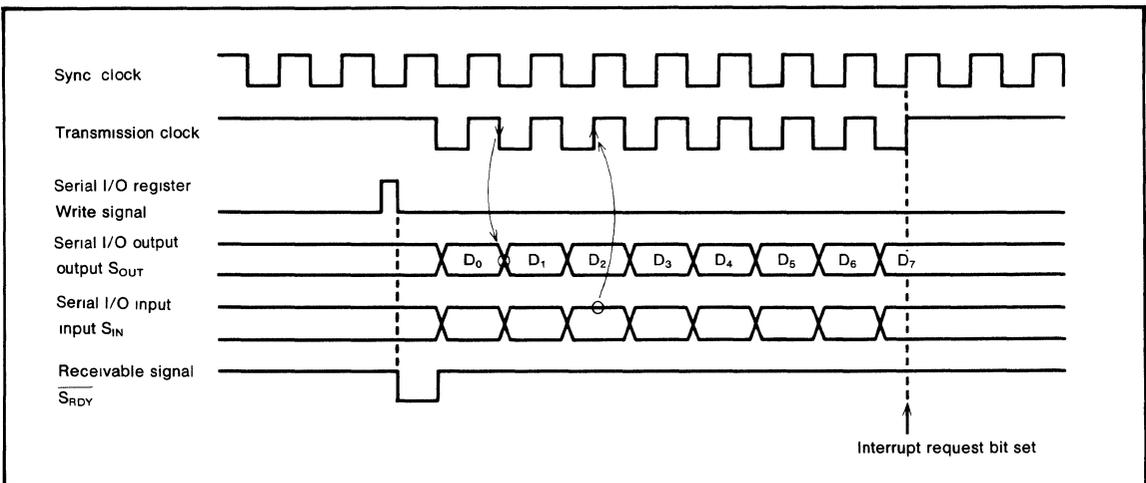


Fig.7 Serial I/O timing

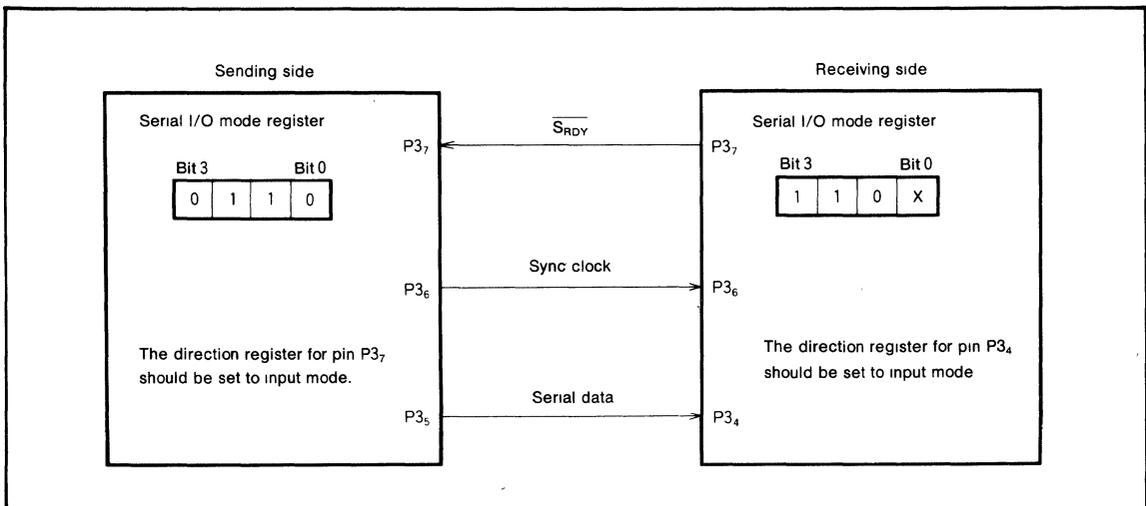


Fig.8 Example of serial I/O connection

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PWM OUTPUT CIRCUIT

(1) Introduction

The M37421M6-XXXSP is equipped with one 14-bit PWM and two 6-bit PWMs. The 14-bit resolution gives PWM1 the minimum resolution bit width of 500ns (for $X_{IN}=4\text{MHz}$) and a repeat period of 8192 μs . PWM2 and PWM3 have the same circuit configuration. PWM2 and PWM3 have a 6-bit resolution with minimum resolution bit width of 16 μs and repeat period of 1024 μs . The accuracy and operation guarantee range is $V_{CC} = 4.5 \sim 5.5\text{V}$ regardless of the input frequency.

Block diagram of the PWM is shown in Figure 9.

The PWM timing generator section applies individual control signals to PWM 1~3, using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM1, PWM2 and PWM3 are in common with pins $P6_1$, $P6_2$ and $P6_3$ of port P6 (i.e. for PWM output, $PM1 \sim PM3$ of the PWM control register and the P6 directional register $D6_1 \sim D6_3$ should be set). When PWM1 is used for output, first set the higher 8-bit of the PWM1-H register (address 00F0 $_{16}$), then the lower 6-bit of the PWM1-L register (address 00F1 $_{16}$). When either PWM2 or PWM3 is used for output, set the 6-bit in the PWM2 (address 00F2 $_{16}$) or PWM3 (address 00F3 $_{16}$) register, respectively. Note that the higher 2 bits of these 8-bit registers are ignored when used 6-bit register.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data at addresses 00F0 $_{16} \sim 00F3_{16}$ is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. When the 6-bit latch is being read, the upper 2 bits of the register becomes undefined. However, bit 7 of the PWM1-L register indicated the completion of the data transfer from the PWM1 register to the PWM1 latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 6-bit PWMs

The timing diagram of the two 6-bit PWMs (PWM2 and PWM3) is shown in Figure 10. One period (T) is composed of 64 (2^6) segments.

There are six different pulse types configured from bits 0~5 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 10(a).

Six different pulses can be output from the PWM. These can be selected by bits 0 through 5. Depending on the content of the 6-bit PWM latch, pulses from 5~0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 10(b). Changes in the contents of the PWM latch allows the selection of 64 lengths of high-level area outputs varying from 0/64 to 63/64. An length of entirely high-level output cannot be output, i.e. 64/64.

(5) 14-bit PWM operation

The timing diagram of the 14-bit PWM1 is shown in Figure 11. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length N times τ is output every short area of $t=256 \times \tau = 128\mu\text{s}$ as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 11.)

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ . As a result, the short-area period $t(=128\mu\text{s}, \text{ approx. } 7.8\text{kHz})$ becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data	Area longer by τ than that of other $t_m (m = 0 \sim 63)$
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m=32$
0 0 0 0 1 0	$m=16, 48$
0 0 0 1 0 0	$m=8, 24, 40, 56$
0 0 1 0 0 0	$m=4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m=1, 3, 5, 7, \dots, 57, 59, 61, 63$

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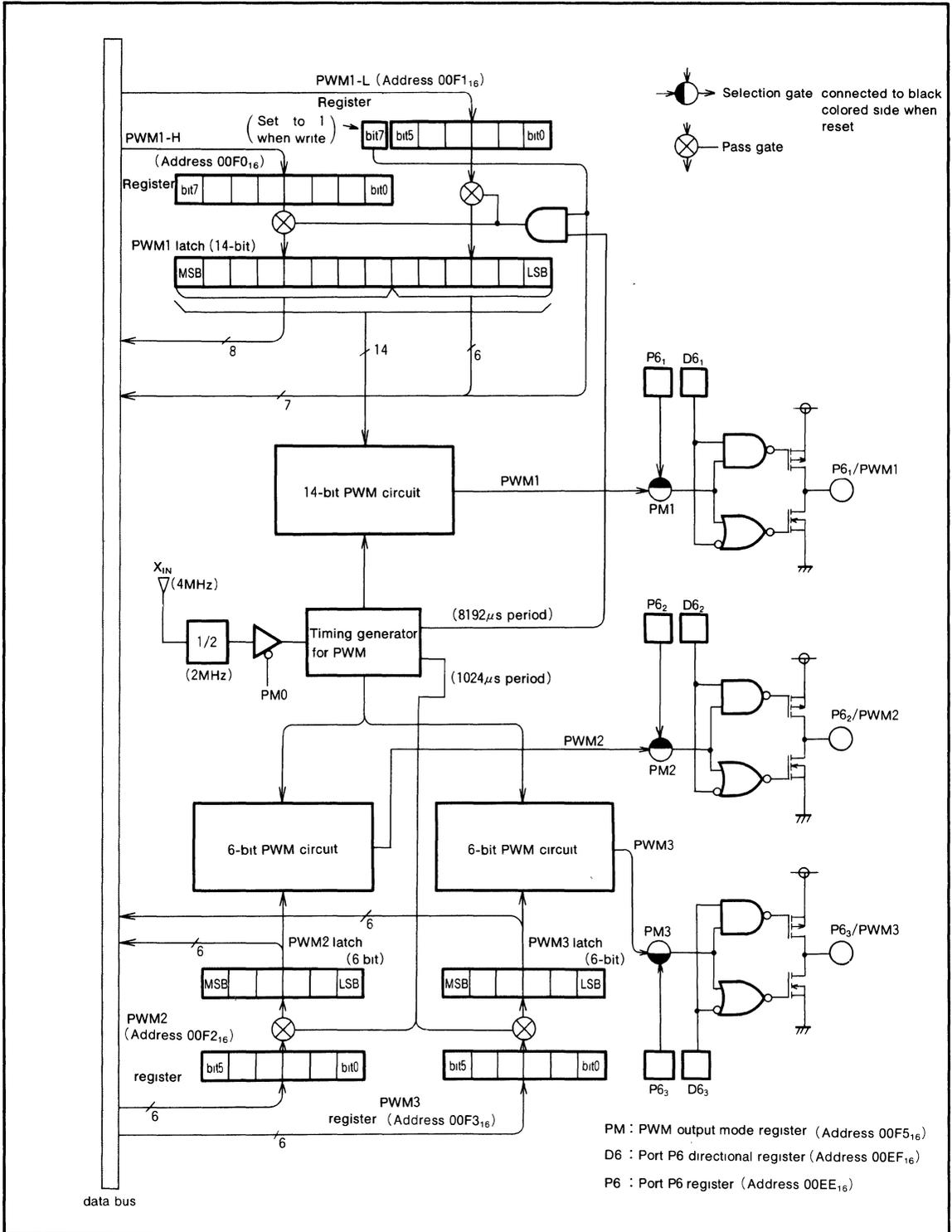


Fig.9 Block diagram of the PWM circuit

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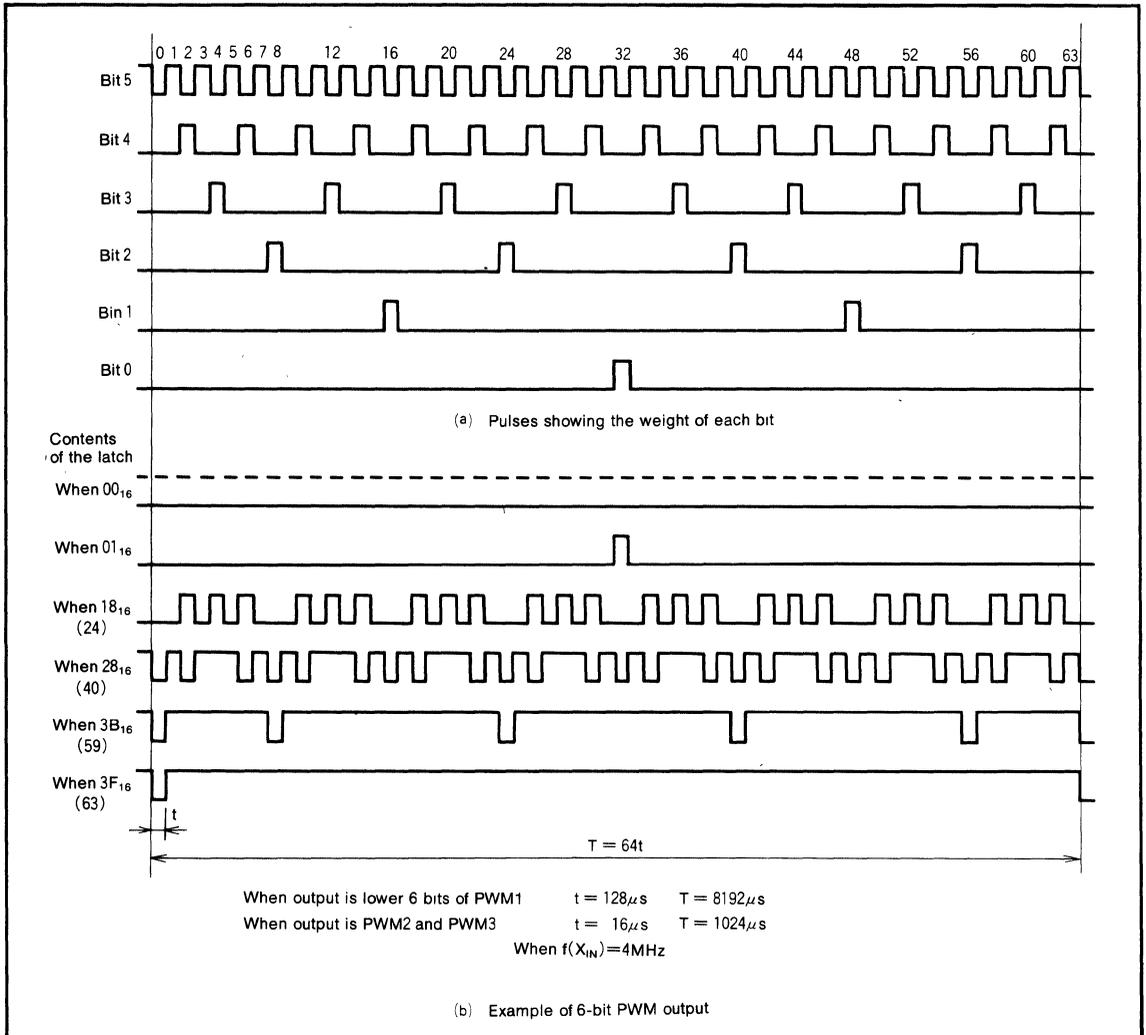


Fig.10 6-bit PWM timing diagram

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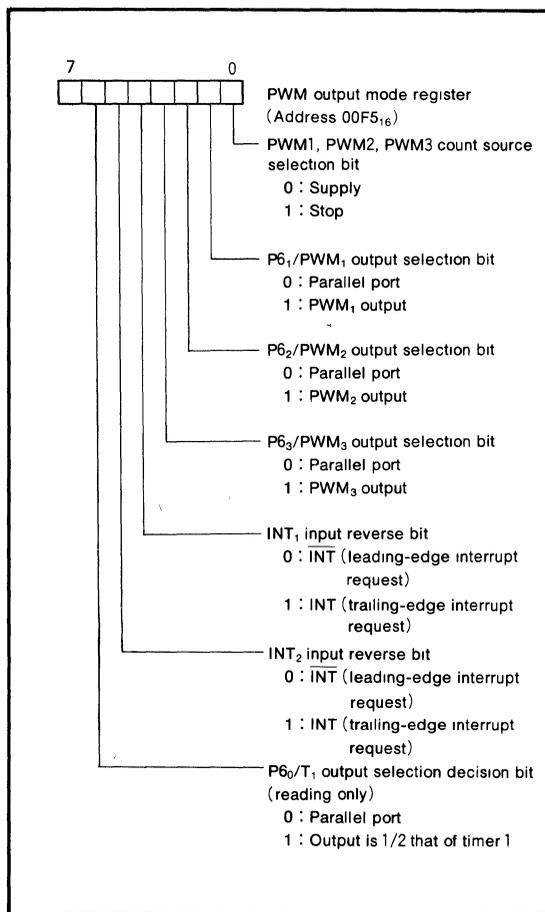


Fig.12 Structure of PWM output mode register

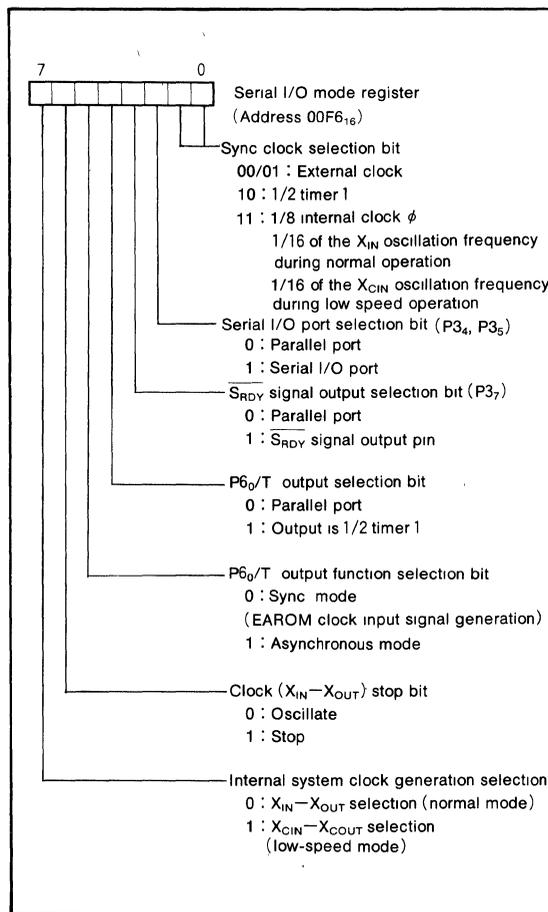


Fig.13 Structure of serial I/O mode register

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PORT P6₀/TIMER 1 OUTPUT

Bit 0 of port P6 outputs 1/2 the frequency of timer 1 when 00F6₁₆ bit 4 of the serial I/O mode register (address 00F6₁₆) is changed. The output switching can be accomplished with either of two procedures, synchronous mode or asynchronous mode, depending on the setting of bit 5 (SM₅) of the serial I/O mode register.

When SM₅ is set to "0" the synchronous mode is set. In such a case, after SM₄ has been changed, synchronization is set to the 1/2 frequency of timer 1 and switching between the port latch and timer takes place. It is possible to ascertain whether switching actually occurred by reading the value of bit 6 (PM₆) of the PWM output mode register.

From the time that the contents of SM₄ was changed to the point where switching completes, the contents of neither SM₄ nor P6₀ may be changed. Use of the synchronous mode prevents the generation of a pulse shorter than the timer output during swithing. Figure 14 (a) gives an example of timing in the synchronous mode. Use of the synchronous mode allows generation of an EAROM clock input signal through the use of a simple program.

When SM₅ is set to "1", the asynchronous mode is set. In this case, the output switching occurs directly after SM₄ has been changed. Figure 14 (b) gives an example of timing in the asynchronous mode.

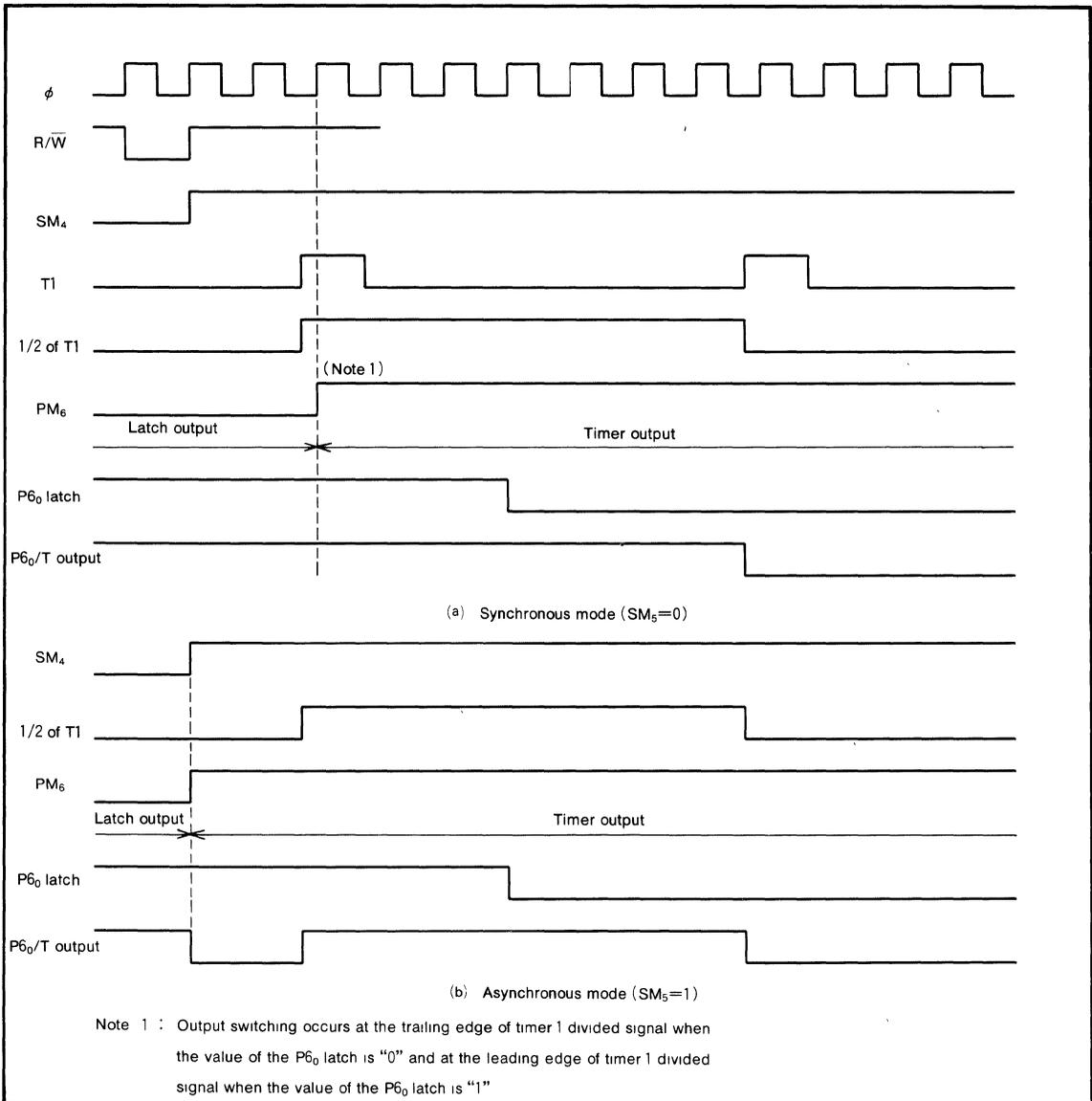


Fig.14 P6₀/T switching timing diagram

COMPARATOR CIRCUIT

The comparator circuit is shown in Figure 15. The comparator circuit consists of the switch tree, ladder resistor, comparator, comparator control circuit, comparator register (address 00FB₁₆), and analog signal input pin (P₃/AN_{IN}). The analog input pin is common with the digital input/output terminal to the data bus.

The 5-bit comparator register can generate 1/16V_{CC}-step internal analog voltage, based on the settings of bits 0 to 3. Table 3 gives the relation between the descriptions of comparator register bits 0 to 3 and the generated internal analog voltage. The comparator result of the analog input voltage and the internal analog voltage is stored in the comparator register, bit 4.

The data is compared by setting the directional register corresponding to board P₃ to "0" (board P₃ enters the input mode), to allow board P₃/AN_{IN} to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the comparison register (address 00FB₁₆), bits 0 to 3. The voltage comparison starts as soon as the writing is completed. 4-cycle (required for comparing) later, the result of comparison is stored in the comparator register, bit 4. Bit 4 is "1" when analog input voltage > internal analog voltage and "0" when analog input voltage < internal analog voltage.

When voltage is compared to by setting bits 0 to 3 of the comparator register "0", bit 4 of the comparator register becomes "1" regardless of the analog input voltage.

Table 3. Relationship between the contents of comparator register and internal voltage

Comparator register				Internal analog voltage
bit 3	bit 2	bit 1	bit 0	
0	0	0	1	1/16V _{CC} -1/32V _{CC}
0	0	1	0	2/16V _{CC} -1/32V _{CC}
0	0	1	1	3/16V _{CC} -1/32V _{CC}
0	1	0	0	4/16V _{CC} -1/32V _{CC}
0	1	0	1	5/16V _{CC} -1/32V _{CC}
0	1	1	0	6/16V _{CC} -1/32V _{CC}
0	1	1	1	7/16V _{CC} -1/32V _{CC}
1	0	0	0	8/16V _{CC} -1/32V _{CC}
1	0	0	1	9/16V _{CC} -1/32V _{CC}
1	0	1	0	10/16V _{CC} -1/32V _{CC}
1	0	1	1	11/16V _{CC} -1/32V _{CC}
1	1	0	0	12/16V _{CC} -1/32V _{CC}
1	1	0	1	13/16V _{CC} -1/32V _{CC}
1	1	1	0	14/16V _{CC} -1/32V _{CC}
1	1	1	1	15/16V _{CC} -1/32V _{CC}

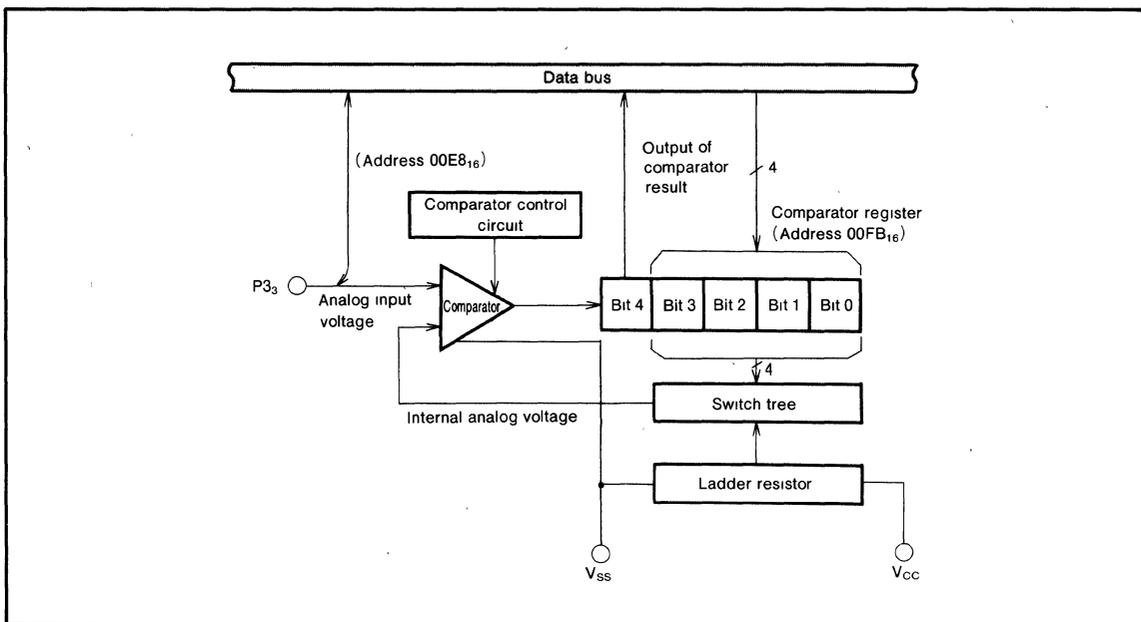


Fig.15 Comparator Circuit

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RESET CIRCUIT

For the reset sequence of the M37421M6-XXXSP, one of the two modes can be selected by mask option: the normal operation start mode which executes reset by normal operation ($f(X_{IN}) = 4.2\text{MHz}$) and the low-speed operation start mode which executes reset by low-speed operation ($f(X_{CIN}) = 32\text{kHz}$).

In the normal operation start mode, the supply voltage is 4.5~5.5 V and when the $\overline{\text{RESET}}$ pin is held at "L" for 2 μs or more and returned to "H", reset is cleared according to the sequence shown in Figure 18. Both X_{IN} clock and X_{CIN} clock start oscillating. To generate the time of waiting for stabilization of X_{IN} clock oscillation, timer 2 and timer 3 are connected and the resulting signal divided by 16 is counted 2048 times to clear the internal reset state. Then, the program starts from the address with the contents of address FFFF_{16} being the higher address and the contents of address FFFE_{16} being the lower address.

In the low-speed operation start mode, the supply voltage is 2.7~5.5 V and when the $\overline{\text{RESET}}$ pin is held at "L" for

2 μs or more and returned to "H", reset is cleared according to the sequence shown in Figure 19. At this time, X_{IN} clock does not start oscillating. To generate the time of waiting for stabilization of X_{CIN} clock oscillation, timer 2 and timer 3 are connected and X_{CIN} is counted 2048 times to clear the internal reset state. Then, the program starts from the address with the contents of address FFFF_{16} being the higher address and the contents of address FFFE_{16} being the lower address. If X_{CIN} clock is stable, the wait time is about 62.5ms ($f(X_{CIN}) = 32.768\text{kHz}$). However, immediately after power-on, the time required to start oscillation depends on the characteristic of the oscillator.

The internal initializations following reset are shown in Figure 16. An example of the reset circuit is shown in Figure 17. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V at the normal operation start mode, and below 0.5V until the supply voltage surpasses 2.7V at the low-speed operation start mode. When selecting the ϕ output to stop, the output of ϕ pin becomes "H" level from "L" level at internal reset clear.

	address	
(1) Port P0 register	(P0) (E0_{16})	00 ₁₆
(2) Port P1 register	(P1) (E2_{16})	00 ₁₆
(3) Port P2 directional register	(D2) (E5_{16})	00 ₁₆
(4) Port P3 directional register	(D3) (E9_{16})	00 ₁₆
(5) Port P4 register	(P4) (EA_{16})	00 ₁₆
(6) Port P5 register	(P5) (EC_{16})	0 0
(7) Port P6 directional register	(D6) (EF_{16})	00 ₁₆
(8) PWM output mode register	(PM) (E5_{16})	0 0 0 0 0 0 0 0
(9) Serial I/O mode register	(SM) (E6_{16})	0 0 0 0 0 0 0 0
	normal operation start mode	1 1 0 0 0 0 0 0
	low-speed operation start mode	0 0 0 0 0 0 0 0
(10) Comparator register	(CR) (FB_{16})	0 0 0 0
(11) Timer 2	(T2) (FC_{16})	FF ₁₆
(12) Timer 3	(T3) (FD_{16})	07 ₁₆
(13) Interrupt control register	(IM) (FE_{16})	00 ₁₆
(14) Timer control register	(TM) (FF_{16})	00 ₁₆
(15) Processor status register (only the interrupt disable flag is set)	(PS)	1
(16) Program counter	(PC _H)	Contents of address FFFF_{16}
	(PC _L)	Contents of address FFFF_{16}

Since the contents of both registers other than those listed above (including timer 1 and the serial I/O registers) and the RAM are undefined at reset, it is necessary to set initial values

Fig. 16 Internal state of microcomputer at reset

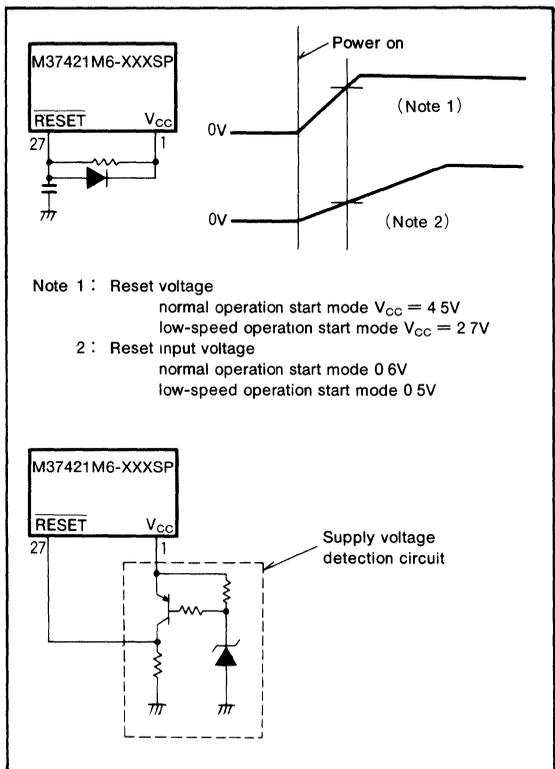


Fig.17 Example of reset circuit

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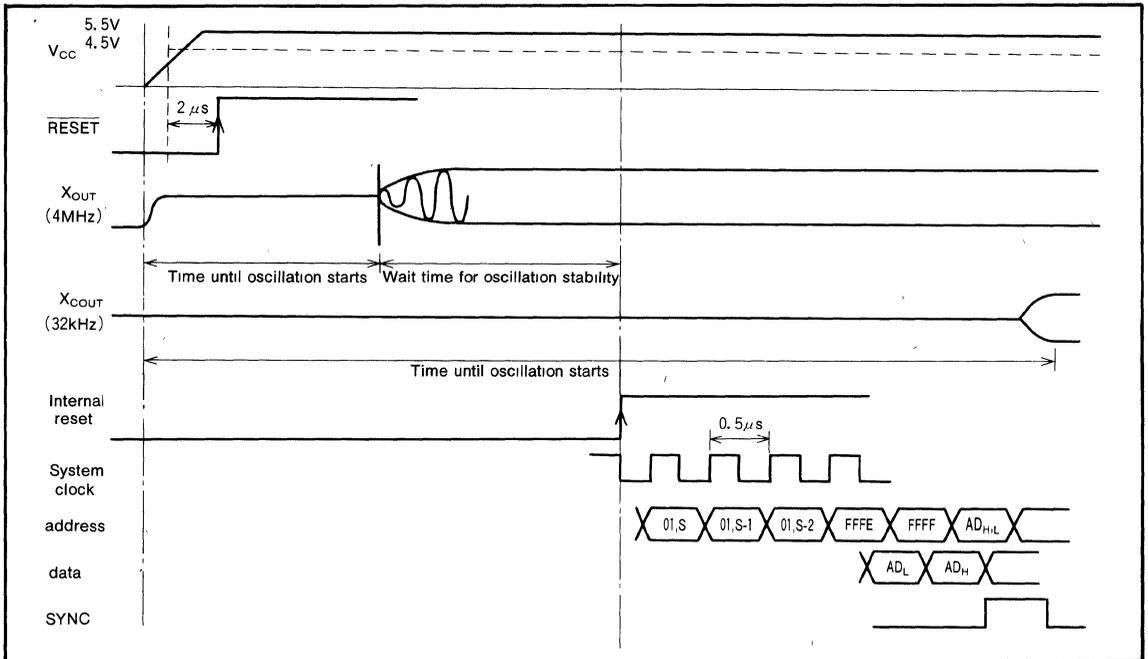


Fig.18 Reset sequence at normal operation start mode

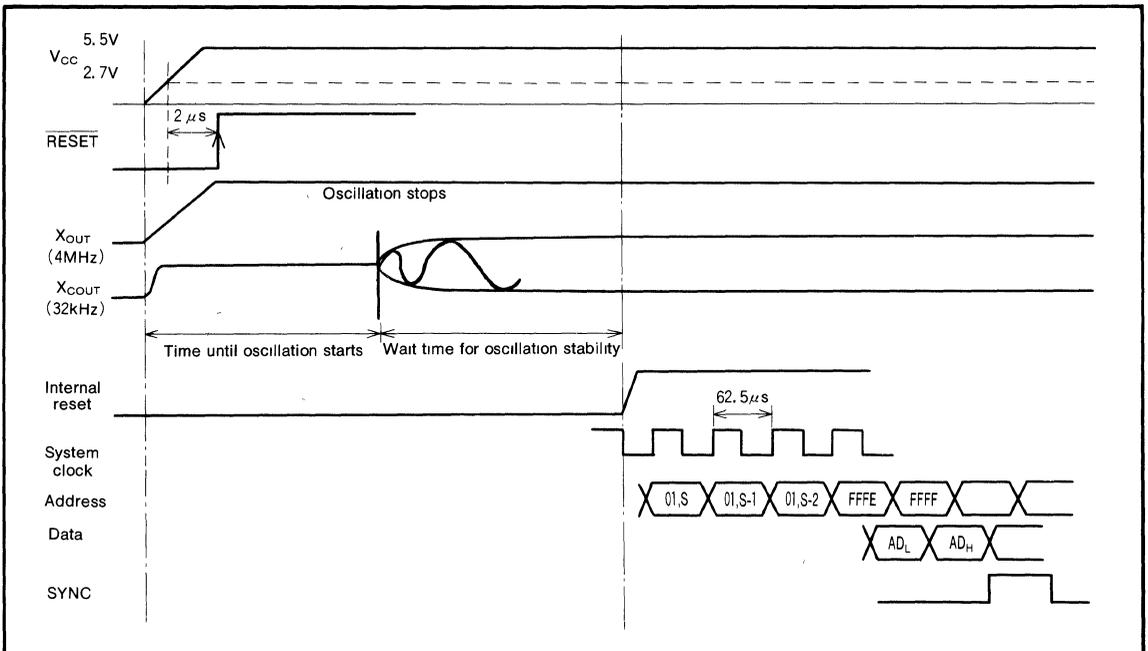


Fig.19 Reset sequence at low-speed operation start mode

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I/O PORTS

(1) Port P0

Port P0 is an 8-bit output port with high-breakdown voltage P-channel open drain outputs featuring a breakdown voltage of V_{CC} -38V. Each pin contains a pull-down resistor making V_P a negative power source. As shown in the memory map in Figure 1, port P0 is used on the zero page at address $00E0_{16}$ in memory.

(2) Port P1

Port P1 has the same functions as port P0.

(3) Port P2

Port P2 is an 8-bit I/O port with N-channel open drain outputs. As shown in Figure 1, port P2 is used at address $00E4_{16}$ in the memory.

Port P2 has a data direction register (address $00E5_{16}$ on zero page) and programming can be undertaken for an individual bit to use the port for input or output. The pins where the data direction register is programmed to "1" are for output and those where the register is programmed to "0" are for input.

The data written into the pin programmed as an output pin are written into the port latch and supplied directly to the output pin. When reading the data from a pin programmed, as an output pin, it is not the output pin contents which are read but the port latch contents. Consequently, since an LED or other similar part is driven directly, the value output previously can be read correctly even if the low-level output voltage goes high. The pin programmed as an input pin remains floating, so external signals can be read. When data is written, it is written into the port latch only and the pin remains floating.

(4) Port P3

Apart from the fact that part of the pins are also used as serial input/output pins, analog input pin and timer 3 clock input pin, its functions are the same as those of port P2.

(5) Port P4

Port P4 has the same functions as port P0.

(6) Port P5

Bits 0 and 1 of port P5 have the same functions as port P4.

Bits 2 and 3 are exclusively used as inputs for mutual use as interrupt inputs. These pins feature hysteresis characteristics. These pins can also be used for fetching inputs even when being used as interrupt inputs.

The interrupt request bits (bit 7 and 1 of address $00FE_{16}$ = INT_1 and INT_2 , respectively) are set to "1" when the inputs of ports $P5_3$ (INT_1) and $P5_2$ (INT_2) change. Depending on the contents of bits 4 and 5 of the PWM output mode register PM (address $00F5_{16}$), either a raising-edge interrupt or a falling-edge interrupt may be selected as the interrupt source. (Refer to Figure 12.)

Since interrupt input and normal input ports are used together in the M37421M6-XXXSP, unwanted noise may mistakenly cause interrupts. This problem can be overcome by programming.

When changing either bit 4 (PM_4) or bit 5 (PM_5) of the PWM output mode register, it is necessary for the interrupt request enable bit (either bit 6 or 0 of address $00FE_{16}$) to be set to the interrupt disable condition ("0"). If this is not done, an interrupt will be generated when either PM_4 or PM_5 is changed.

Bits 4 through 7 of port P5 is a 4-bit input port.

(7) Port P6

Port P6 is a 6-bit I/O port having the same functions as Port P2. The output is CMOS three-state. Bit 0 is used in common with the timer output. Bits 1~3 are used in common with PWMs 1~3.

A block diagram of ports P0 through P6 are shown in Figure 19.

(8) Clock ϕ output pin

The clock frequency, divided by two, is output (X_{IN}). However, in the low-speed mode $1/2$ the clock frequency for timer (X_{CIN}) is output. $RESET_{OUT}$ signal can be output by option.

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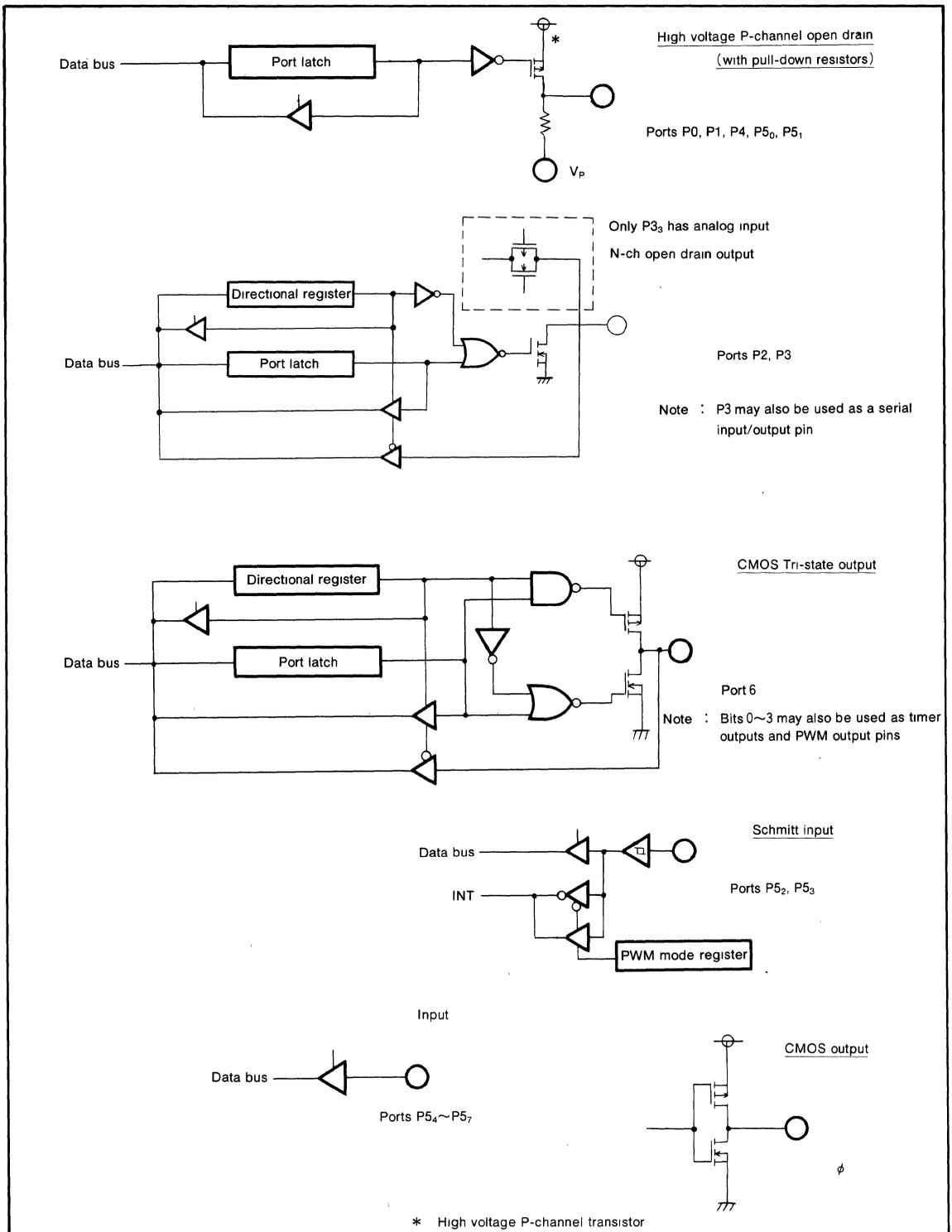


Fig.20 Block diagram of port P0~P6 (single-chip mode) and output format of ϕ

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CLOCK GENERATING CIRCUIT

The M37421M6-XXXSP has two internal clock generating circuits. Figure 23 shows a block diagram of the clock generating circuits. The internal ϕ after reset can be selected by option, the normal operation start mode and the low-speed operation start mode.

The frequency applied to the X_{IN} pin divided by two is used as the internal clock at the normal operation start mode. The frequency applied to the X_{CIN} pin divided by two is used as the internal clock at low-speed operation mode.

Both X_{IN} and X_{CIN} clocks start oscillation after reset at normal operation start mode. Bit 7 of serial I/O mode register (SM_7) can be used to switch the internal clock ϕ to 1/2 the frequency applied to the X_{CIN} pin. When using X_{CIN} clock pin is connected to V_{SS} and leave the X_{OUT} pin open.

Only X_{CIN} clock starts oscillation after reset at low-speed operation start mode and starts by low-speed operation. Bit 6 of the serial I/O mode register (SM_6) must be set to "0" then bit 7 (SM_7) must be set to "0" to switch ϕ to the normal operation mode. However, the wait time until the oscillation stabilizes must be generated with a program at this case.

Figure 21 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 22.

The M37421M6-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 2 and timer 3 are forcibly connected and $\phi/4$ is selected as timer 2 input. When restarting oscillation, FF_{16} is automatically set in timer 2 and 07_{16} in timer 3 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 2 count stop bit must be set to supply ("0"), timer 2 interrupt enable bit and timer 3 interrupt enable bit must be set to disable ("0"), and timer 3 interrupt request bit must be set to no request ("0").

Oscillation is restarted (release the stop mode) when INT_1 , INT_2 , or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the \overline{RESET} pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($200\mu A$ or less at $f(X_{CIN})=32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the RESET pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 24 shows the transition of states for the system clock.

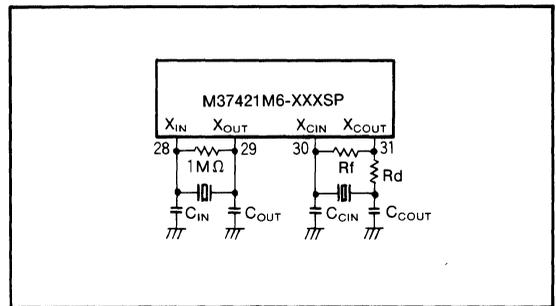


Fig.21 Example ceramic resonator circuit

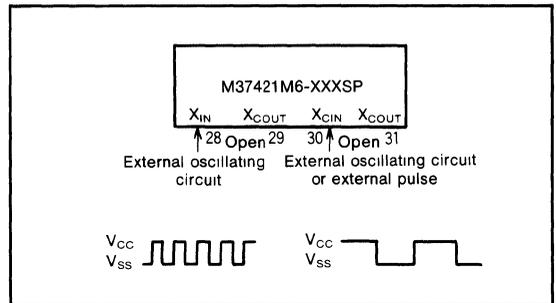


Fig.22 Example clock input circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

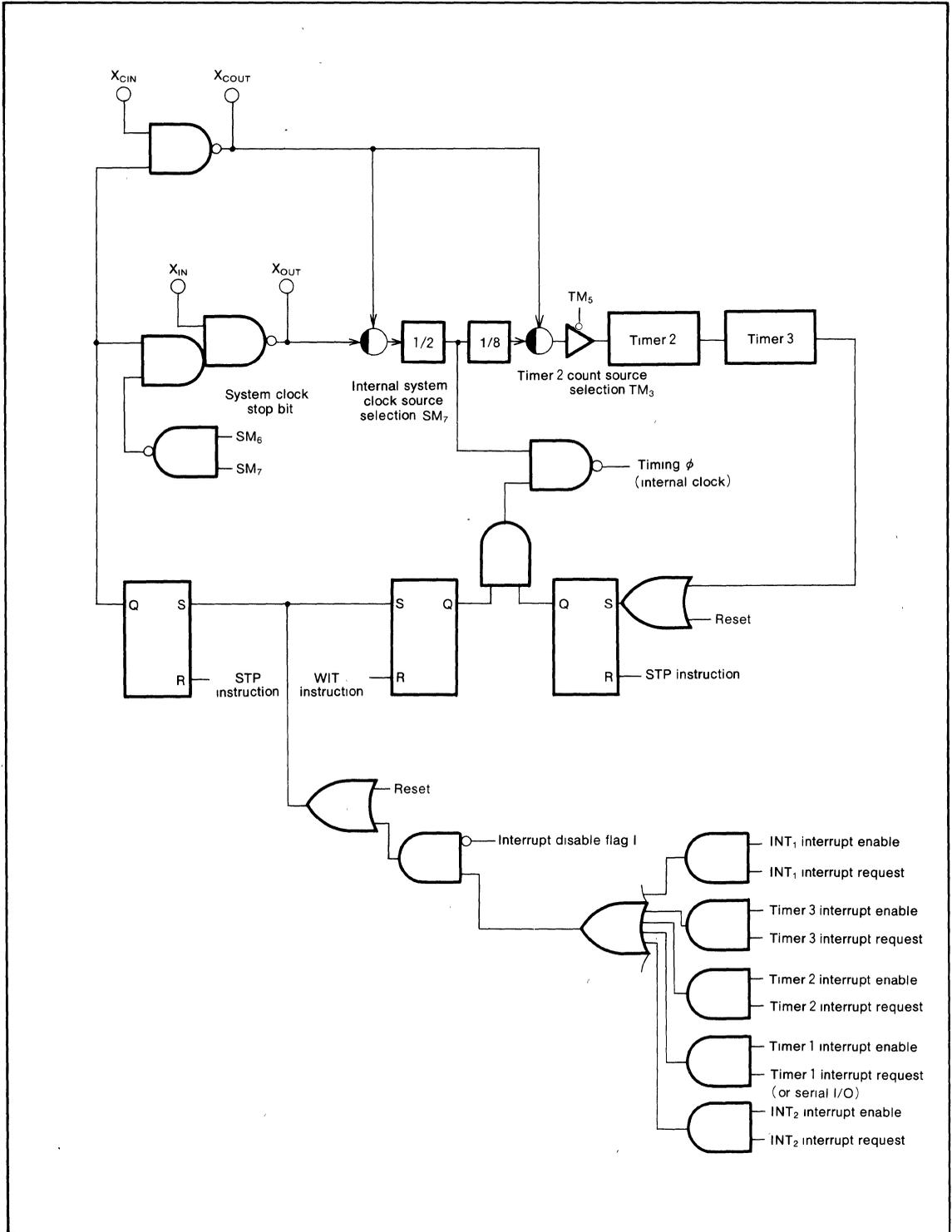


Fig.23 Block diagram of clock generating circuit

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

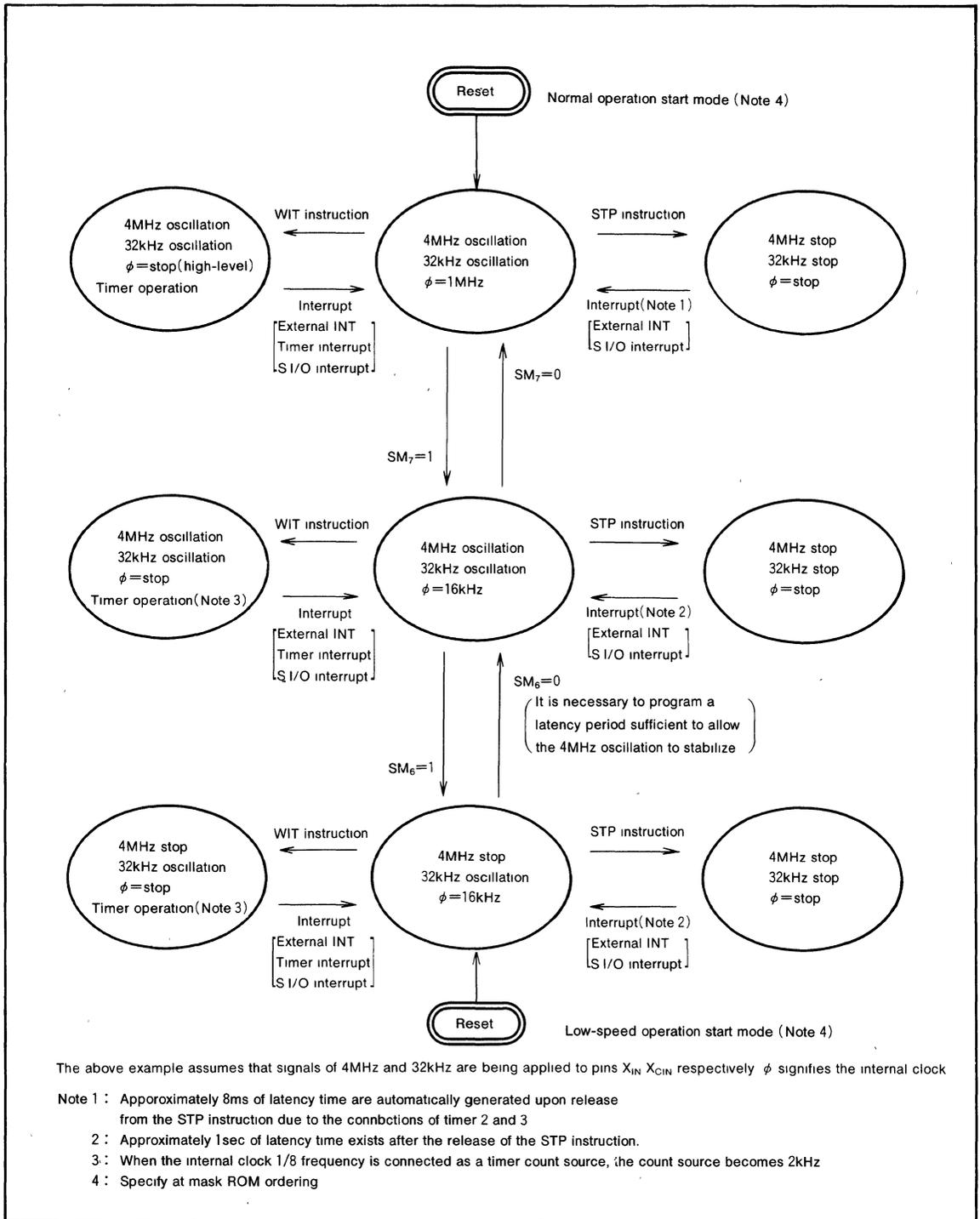
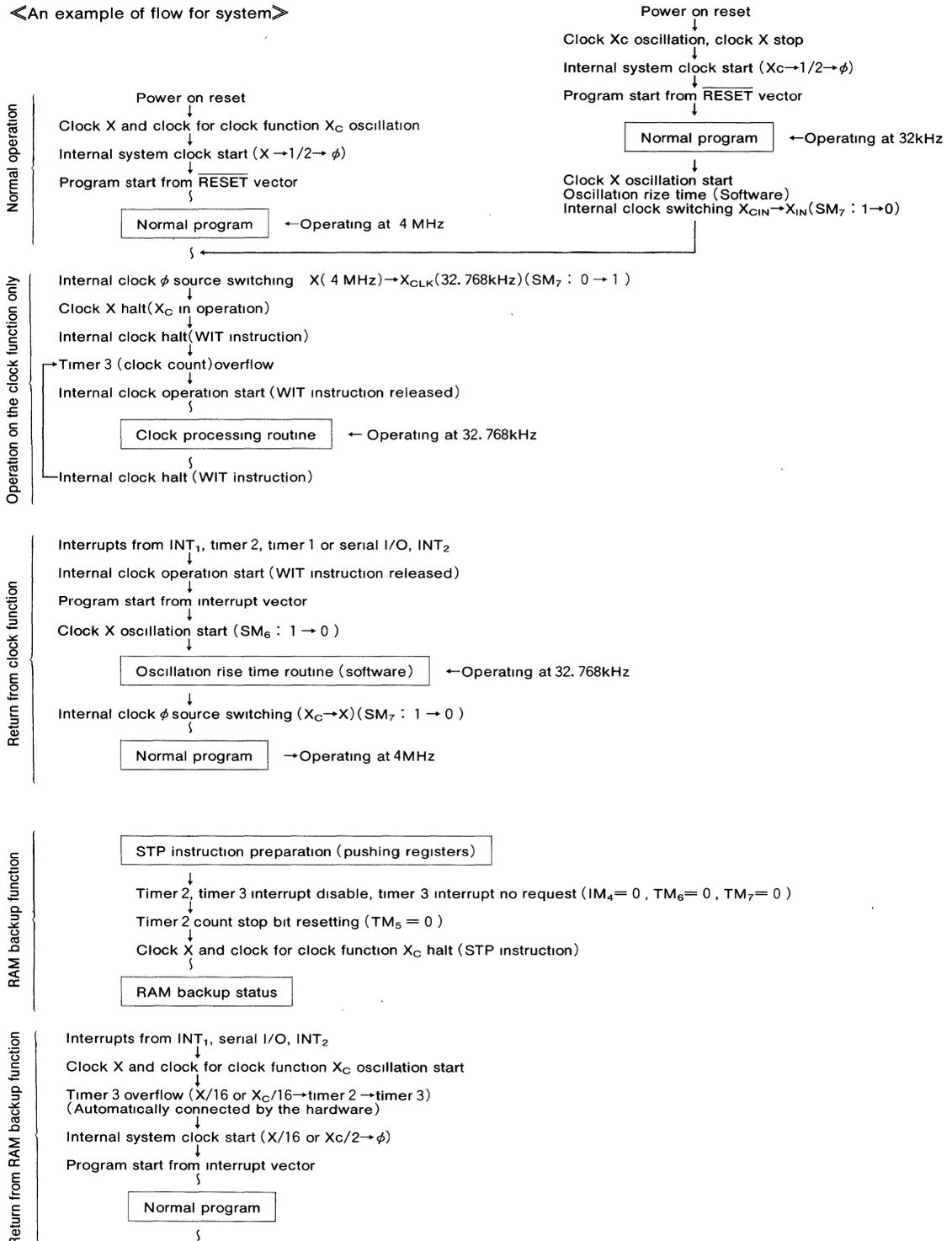


Fig.24 Transition of states for the system clock

MITSUBISHI MICROCOMPUTERS M37421M6-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

◁An example of flow for system▷



PROGRAM NOTES

- (1) The frequency ratio of the timer and the prescaler is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) When $\phi/4$ or it divided by timer are used as clock for timer, the contents of the timer can be read at voluntary timing.
However, when an other clock (except above clocks) is input to timer, read the contents of timer either while the input of the timer is not changing or after timer count is stopped.
- (4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (5) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data EPROM 3 sets

Write the following option on the mask confirmation form

- (1) ϕ output stop option
- (2) Internal reset timing option

MITSUBISHI MICROCOMPUTERS

M37421M6-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} . Output transistors cut-off	-0.3~7	V
V_P	Pull-down input voltage		$V_{CC}-40\sim V_{CC}+0.3$	V
V_I	Input voltage, P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P3 ₄ ~P3 ₇ , CNV _{SS} , P5 ₂ /INT ₂ , P5 ₃ /INT ₁		-0.3~13	V
V_I	Input voltage, RESET, X _{IN} , X _{CIN}		-0.3~7	V
V_I	Input voltage, P6 ₀ ~P6 ₅ , P3 ₃		-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage, P5 ₄ ~P5 ₇		-0.3~13	V
V_O	Output voltage, P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P3 ₄ ~P3 ₇		-0.3~13	V
V_O	Output voltage, P6 ₀ ~P6 ₅ , X _{OUT} , X _{COU} T, ϕ , P3 ₃		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage, P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁		$V_{CC}-40\sim V_{CC}+0.3$	V
P_d	Power dissipation		$T_a = 25^\circ\text{C}$	1000 (Note 1)
T_{opr}	Operating temperature		-10~70	°C
T_{stg}	Storage temperature		-40~125	°C

Note 1 : 600mW for QFP types

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V\pm 10\%$, $T_a=-10\sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	$f(X_{IN})=4.2\text{MHz}$ 4.5	5	5.5	V
		$f(X_{CIN})=32\text{kHz}$ 2.7	5	5.5	V
V_P	Pull-down supply voltage	$V_{CC}-38$		V_{CC}	V
V_{SS}	Supply voltage	0			V
V_{IH}	"H" input voltage P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , CNV _{SS} (Note 1) P5 ₂ /INT ₂ , P5 ₃ /INT ₁ , P6 ₀ ~P6 ₅	0.75 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage RESET, X _{IN} , X _{CIN}	0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage P5 ₄ ~P5 ₇	0.4 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , CNV _{SS} P5 ₂ /INT ₂ , P5 ₃ /INT ₁ , P6 ₀ ~P6 ₅	0		0.25 V_{CC}	V
V_{IL}	"L" input voltage RESET	0		0.12 V_{CC}	V
V_{IL}	"L" input voltage X _{IN} , X _{CIN}	0		0.16 V_{CC}	V
V_{IL}	"L" input voltage P5 ₄ ~P5 ₇	0		0.12 V_{CC}	V
$I_{OH}(\text{sum})$	"H" sum output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P4 ₀ ~P4 ₇ P5 ₀ , P5 ₁			-120	mA
$I_{OH}(\text{sum})$	"H" sum output current P6 ₀ ~P6 ₅			-5	mA
$I_{OL}(\text{sum})$	"L" sum output current P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P6 ₀ ~P6 ₅			50	mA
$I_{OH}(\text{peak})$	"H" peak output current P0 ₀ ~P0 ₄			-40	mA
$I_{OH}(\text{peak})$	"H" peak output current P0 ₅ ~P0 ₇ , P1 ₀ ~P1 ₇			-30	mA
$I_{OH}(\text{peak})$	"H" peak output current P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁			-24	mA
$I_{OH}(\text{peak})$	"H" peak output current P6 ₀ ~P6 ₅			-3	mA
$I_{OL}(\text{peak})$	"L" peak output current P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇			15	mA
$I_{OL}(\text{peak})$	"L" peak output current P6 ₀ ~P6 ₅			3	mA
$I_{OH}(\text{avg})$	"H" average output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇			-18	mA
$I_{OH}(\text{avg})$	"H" average output current P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁			-12	mA
$I_{OH}(\text{avg})$	"H" average output current P6 ₀ ~P6 ₅			-1.5	mA
$I_{OL}(\text{avg})$	"L" average output current P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇			10	mA
$I_{OL}(\text{avg})$	"L" average output current P6 ₀ ~P6 ₅			1.5	mA
$f(P3_2/\text{CNTR})$	Timer 3 counter clock input oscillation frequency (Note 2)	$f(X_{IN})=4.2\text{MHz}$ $f(X_{CIN})=32\text{kHz}$		250 50	kHz
$f(X_{IN})$	Clock input oscillating frequency (Note 2, 3, 5)			4.2	
$f(X_{CIN})$	Clock oscillating frequency for clock function		32.768	50	kHz

Note 1 : High-level input voltage of up to +12V may be applied to permissible for ports P2₀~P2₇, P3₀~P3₂, P3₄~P3₇, CNV_{SS}, P5₂ and P5₃

2 : Oscillation frequency is at 50% duty cycle

3 : When used in the low-speed mode, the timer clock input frequency should be $f(X_{CIN}) < f(X_{IN})/3$

4 : The average output current $I_{OL}(\text{avg})$ and $I_{OH}(\text{avg})$ are in period of 100ms

5 : When external clock input is used, the timer clock input frequency should be $f(X_{CIN}) \leq 50\text{kHz}$

MITSUBISHI MICROCOMPUTERS
M37421M6-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 25^\circ C$, $f(X_{IN}) = 4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ.	Max		
V_{OH}	"H" output voltage P6 ₀ ~P6 ₅	$I_{OH} = -0.5mA$	$V_{CC} - 0.4$			V	
V_{OH}	"H" output voltage ϕ	$I_{OH} = -2.5mA$	$V_{CC} - 2$			V	
V_{OH}	"H" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇	$I_{OH} = -18mA$	$V_{CC} - 2$			V	
V_{OH}	"H" output voltage P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁	$I_{OH} = -12mA$	$V_{CC} - 2$			V	
V_{OL}	"L" output voltage P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇	$I_{OL} = 10mA$			2	V	
V_{OL}	"L" output voltage P6 ₀ ~P6 ₅	$I_{OL} = 0.5mA$			0.4	V	
V_{OL}	"L" output voltage ϕ	$I_{OL} = 2.5mA$			2	V	
$V_{T+} - V_{T-}$	Hysteresis P5 ₂ /INT ₂ , P5 ₃ /INT ₁		0.3		1	V	
$V_{T+} - V_{T-}$	Hysteresis RESET			0.5	0.7	V	
$V_{T+} - V_{T-}$	Hysteresis P3 ₅	When used as CLK input	0.3		1	V	
I_{IL}	"L" input current P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇	$V_i = 0V$			-5	μA	
I_{IL}	"L" input current P6 ₀ ~P6 ₅	$V_i = 0V$			-5	μA	
I_{IL}	"L" input current P5 ₄ ~P5 ₇	$V_i = 0V$			-5	μA	
I_{IL}	"L" input current RESET, X _{IN} , X _{CIN}	$V_i = 0V$			-5	μA	
I_{IL}	"L" input current P5 ₂ /INT ₂ , P5 ₃ /INT ₁	$V_i = 0V$			-5	μA	
I_{IH}	"H" input current	P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇	$V_i = 5V$		5	μA	
		P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P3 ₃ ~P3 ₇	$V_i = 12V$		12		
I_{IH}	"H" input current P6 ₀ ~P6 ₅	$V_i = 5V$			5	μA	
I_{IH}	"H" input current P5 ₄ ~P5 ₇	$V_i = 5V$			5	μA	
		$V_i = 12V$			12		
I_{IH}	"H" input current RESET, X _{IN} , X _{CIN}	$V_i = 5V$			5	μA	
I_{IH}	"H" input current P5 ₂ /INT ₂ , P5 ₃ /INT ₁	$V_i = 5V$			5	μA	
		$V_i = 12V$			12		
I_{LOAD}	"L" output current	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁	$V_P = V_{CC} - 36V$, $V_{OL} = V_{CC}$	150	500	900	μA
I_{LEAK}		P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁	$V_P = V_{CC} - 38V$, $V_{OL} = V_{CC} - 38V$			30	μA
V_{RAM}	RAM retention voltage	at clock stop	2		5.5	V	
I_{CC}	Supply current	Output pins open (output OFF)			6	12	mA
		$V_P = V_{CC}$, $V_P = V_{SS}$ Input and I/O pins all at V_{SS} $X_{IN} = 4MHz$ (system operation)			6	12	
		ditto (at comparator mode)			6	12	
		ditto (at wait mode)			1		
		$X_{IN} - X_{OUT}$ stop $X_{CIN} = 32kHz$ (at system operation) all other conditions same as above			60	200	μA
		ditto (at wait mode)			40		
		Oscillation all stopped (at STOP mode)	$T_a = 25^\circ C$			1	
			$T_a = 70^\circ C$			10	

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

COMPARATOR CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{CC}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$)

Parameter	Limits			Unit
	Min.	Typ	Max	
Resolution	—	—	$(1/16)V_{CC}$	V
Internal analog voltage error	—	—	$\pm(1/16)V_{CC}$	V
Analog input voltage	0	—	V_{CC}	V

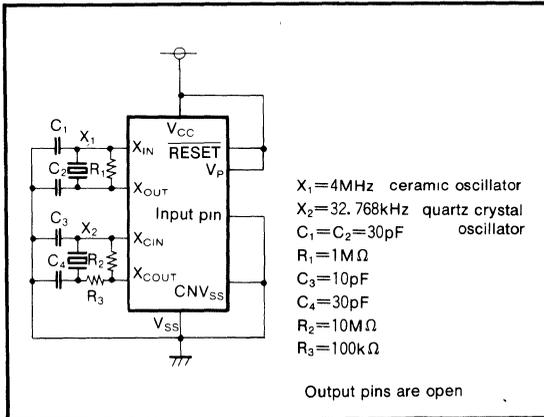


Fig.25 Supply current test circuit

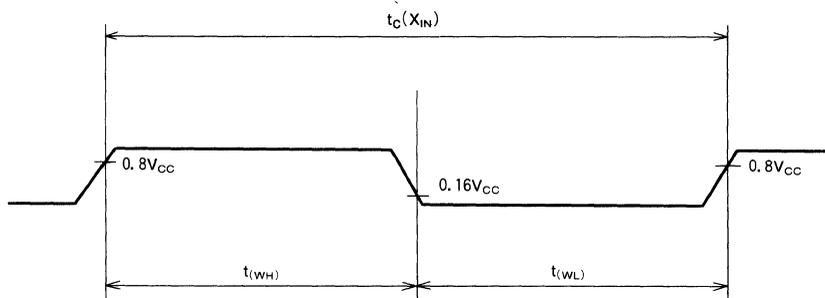
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TIMING REQUIREMENTS

Single-chip mode ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 25^\circ C$, $f(X_{IN}) = 4MHz$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max	
$t_{C(X_{IN})}$	External clock input cycle time (X_{IN} input)	238			ns
$t_{W(X_{IN})}$	External clock input pulse width (X_{IN} input)	75			ns
$t_{C(X_{CIN})}$	External clock input cycle time (X_{CIN})	2.0			ms
$t_{W(X_{CIN})}$	External clock input pulse width (X_{CIN})	1.0			ms
t_r	External clock rise time			25	ns
t_f	External clock fall time			25	ns

Timing requirements of X_{IN}



Parameter	Min.	Typ.	Max.	Unit
X_{IN} clock input cycle time $t_c(X_{IN})$	238			ns
X_{IN} clock input pulse width "H" t_{WH}	$t_c \times 0.45$		$t_c \times 0.55$	
X_{IN} clock input pulse width "L" t_{WL}	$t_c \times 0.45$		$t_c \times 0.55$	

MITSUBISHI MICROCOMPUTERS

M37424M8-XXXSP M37524M4-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37424M8-XXXSP, M37524M4-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. They are housed in a 64-pin shrink plastic molded DIP.

This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37424M8-XXXSP and the M37524M4-XXXSP are noted below. The following explanations apply to the M37424M8-XXXSP.

Specification variations for other chips are noted accordingly.

Type name	Port P1 output structure
M37424M8-XXXSP	CMOS
M37524M4-XXXSP	N-channel open drain

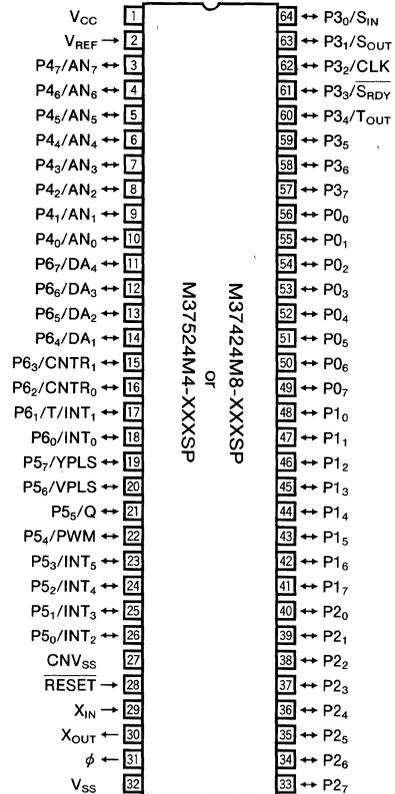
FEATURES

- Number of basic instructions.....70
68 MELPS 740 basic instructions +2 multiply/divide instructions
- Memory size ROM16384 bytes
RAM256 bytes
- Instruction execution time
..... 1 μ s (minimum instructions, at 4MHz frequency)
- Single power supply.....5V \pm 10%
- Power dissipation
normal operation mode (at 4MHz frequency).....30mW
- Subroutine nesting96 levels (Max.)
- Interrupt16 types, 16 vectors
- 8-bit timer4
- 16-bit timer1
- Serial I/O (8-bit or 16-bit)1
- PWM output (14-bit)1
- A-D converter (8-bit resolution)8-channel
- D-A converter (5-bit resolution)2
- D-A converter (8-bit resolution)2
- Watchdog timer
- External trigger output (1-bit)1
- V pulse Y pulse generator
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P5, P6).....56

APPLICATION

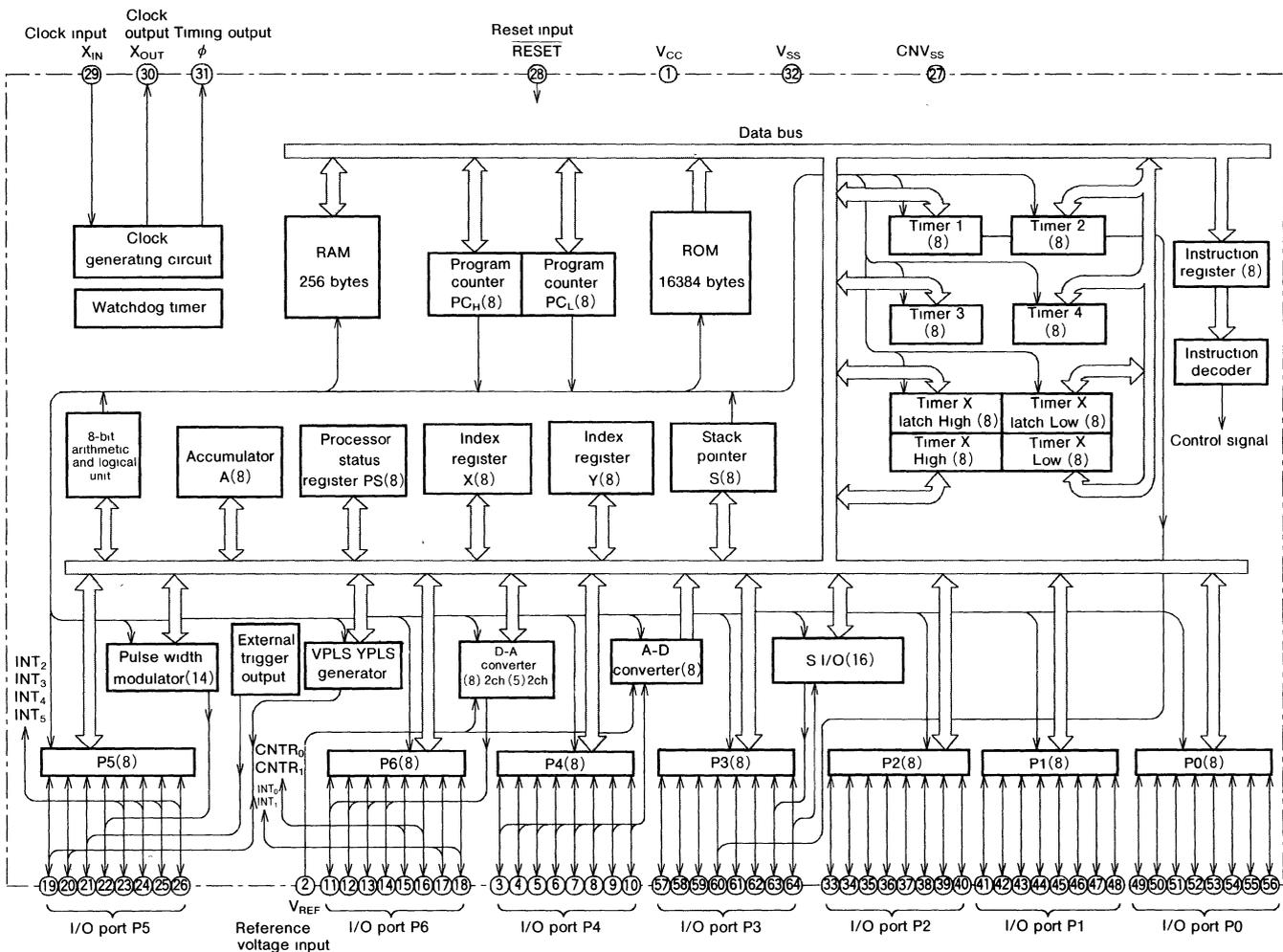
Office automation equipment
VCR equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

M37424M8-XXXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MITSUBISHI MICROCOMPUTERS
M37424M8-XXXXSP
M37524M4-XXXXSP

M37424M8-XXXSP
M37524M4-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37424M8-XXXSP

Parameter		Functions
Number of basic instructions		70 (68 MELPS 740 basic instructions+2)
Instruction execution time		1 μ s (minimum instructions, at 4MHz frequency)
Clock frequency		4MHz
Memory size	ROM	16384 bytes
	RAM	256 bytes
Input/Output ports	P0, P1, P2, P3, P4, P5, P6	I/O
Serial I/O		8-bit \times 7
Timers		8-bit \times 4, 16-bit \times 1
A-D conversion		8-bit \times 1 (8 channels)
D-A conversion		5-bit \times 2, 8-bit \times 2
Pulse width modulator		14-bit \times 1
Watchdog timer		15-bit \times 1
Subroutine nesting		96 levels (max)
Interrupt		16 (external 8, internal 8)
Clock generating circuit		Built-in (ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 10%
Power dissipation		30mW (at 4MHz frequency)
Operating temperature range		-10 \sim 70 $^{\circ}$ C
Device structure		CMOS silicon gate
Package		64-pin shrink plastic molded DIP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is usually connected to V _{SS}
V _{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter
<u>RESET</u>	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 4μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The output structure of M37424M8-XXXSP is CMOS output and that of M37524M4-XXXSP is N-channel open drain output
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 The output structure is CMOS output
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 When serial I/O is used, P3 ₃ , P3 ₂ , P3 ₁ , and P3 ₀ work as $\overline{S_{RDY}}$, CLK, S _{OUT} , and S _{IN} pins, respectively Also P3 ₄ works as T _{OUT} pin The output structure is N-channel open drain
P4 ₀ ~P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0 P4 ₀ ~P4 ₇ work as analog input port AN ₀ ~AN ₇
P5 ₀ ~P5 ₇	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0 P5 ₇ , P5 ₆ , P5 ₅ , P5 ₄ and P5 ₃ ~P5 ₀ are in common with the YPLS output, VPLS output, Q output, PWM output and interrupt input respectively
P6 ₀ ~P6 ₇	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0 P6 ₇ ~P6 ₄ , P6 ₃ , P6 ₂ , and P6 ₁ , P6 ₀ are in common with the D-A output, CNTR output and interrupt input respectively

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MEMORY

- **Special Function Register (SFR) Area**
The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.
- **RAM**
RAM is used for data storage as well as a stack area.
- **ROM**
ROM is used for storing user programs as well as the interrupt vector area.

- **Interrupt Vector Area**
The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.
- **Zero Page**
Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.
- **Special Page**
Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

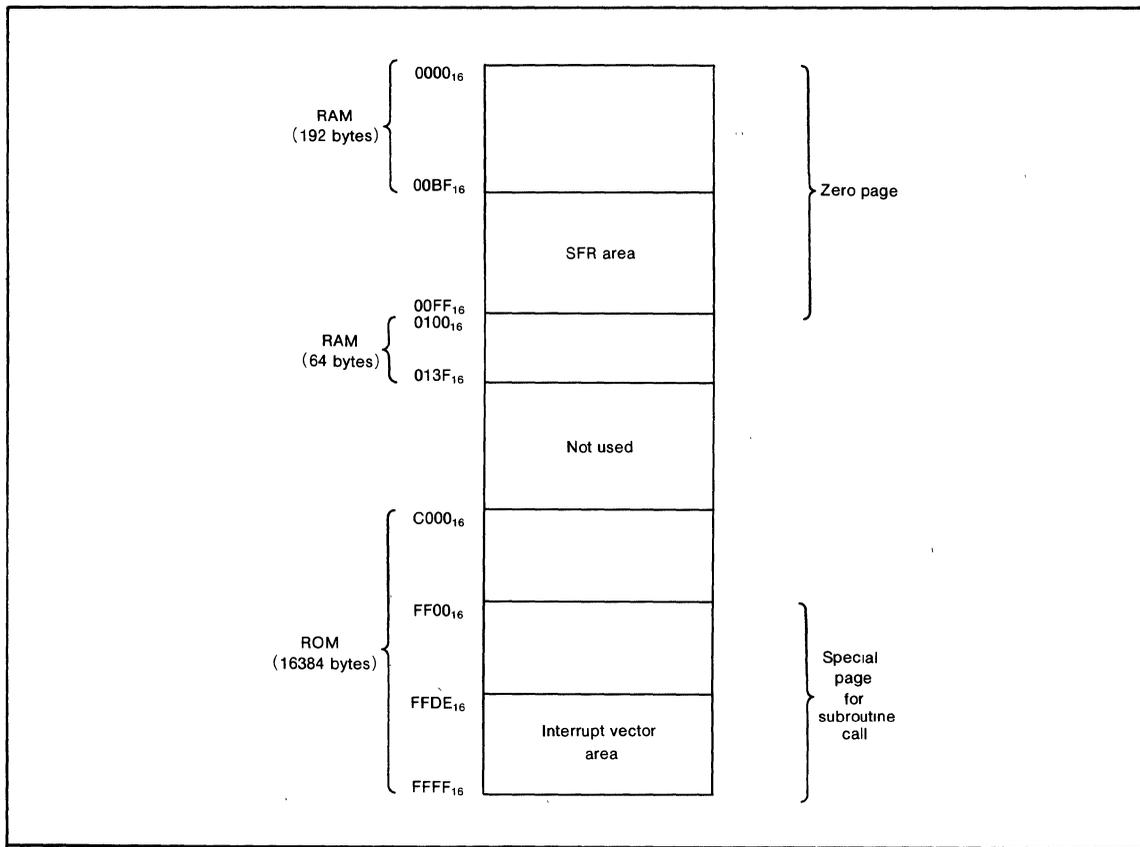


Fig.2 Memory map

00C0 ₁₆	Port P0
00C1 ₁₆	Port P0 directional register
00C2 ₁₆	Port P1
00C3 ₁₆	Port P1 directional register
00C4 ₁₆	Port P2
00C5 ₁₆	Port P2 directional register
00C6 ₁₆	Port P3
00C7 ₁₆	Port P3 directional register
00C8 ₁₆	Port P4
00C9 ₁₆	Port P4 directional register
00CA ₁₆	Port P5
00CB ₁₆	Port P5 directional register
00CC ₁₆	Port P6
00CD ₁₆	Port P6 directional register
00CE ₁₆	Reserved area
00D0 ₁₆	
00D1 ₁₆	D-A output enable register
00D2 ₁₆	D-A3 conversion register
00D3 ₁₆	D-A4 conversion register
00D4 ₁₆	Pulse width modulation register H
00D5 ₁₆	Pulse width modulation register L
00D6 ₁₆	V pulse preset value P
00D7 ₁₆	V pulse preset value N
00D8 ₁₆	V pulse control register
00D9 ₁₆	A-D successive approximation register
00DA ₁₆	A-D control register
00DB ₁₆	D-A1 conversion register
00DC ₁₆	D-A2 conversion register
00DD ₁₆	Serial I/O mode register
00DE ₁₆	Serial I/O register L
00DF ₁₆	Serial I/O register H
00E0 ₁₆	Reserved area
00EC ₁₆	
00ED ₁₆	Interrupt polarity specification register
00EE ₁₆	Special function selection register
00EF ₁₆	Watchdog timer
00F0 ₁₆	Timer 1
00F1 ₁₆	Timer 2
00F2 ₁₆	Timer 3
00F3 ₁₆	Timer 4
00F4 ₁₆	Timer X (low-order)
00F5 ₁₆	Timer X (high-order)
00F6 ₁₆	Timer X latch (low-order)
00F7 ₁₆	Timer X latch (high-order)
00F8 ₁₆	Timer 1, 2 mode register
00F9 ₁₆	Timer 3, 4 mode register
00FA ₁₆	Timer X mode register
00FB ₁₆	CPU mode register
00FC ₁₆	Interrupt request register 1
00FD ₁₆	Interrupt request register 2
00FE ₁₆	Interrupt control register 1
00FF ₁₆	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 16 different events. Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt inhibit flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupt are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 5 shows the structure of the interrupt request registers 1 and 2, interrupt control registers 1 and 2 and interrupt polarity specification register.

For external interrupts (INT₀ to INT₅, CNTR₀, and CNTR₁), the polarity of each pin's interrupt input can be set. Polarity for INT₀ to INT₅ and CNTR₁ is set by bits 0 to 6 of the interrupt polarity specification register (address 00ED₁₆); polarity for CNTR₀ is set by bit 6 of the timer X mode register (address 00FA₁₆). If "0" is written to one of these bits, the corresponding interrupt request is falling-edge active; if "1" is written, the corresponding interrupt request is rising-edge active. INT₁ can also be set to be both rising-edge and falling-edge active by setting bit 7 of the interrupt polarity specification register to "1". The meaning of the CNTR₀ interrupt is different if it is used with timer X in pulse width measurement mode 1, pulse width measurement mode 2, or pulse period measurement mode. For details, see the section on timer X

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 4 shows interrupts control.

Table 1. Interrupt vector address and priority

Event	Priority	Vector addresses	Remarks
RESET	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
INT ₀ interrupt	2	FFFD ₁₆ , FFFC ₁₆	External interrupt (phase programmable)
INT ₁ interrupt	3	FFFB ₁₆ , FFFA ₁₆	External interrupt (phase programmable)
INT ₂ interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	External interrupt (phase programmable)
Timer 4 interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	
Timer 1 interrupt	6	FFF5 ₁₆ , FFF4 ₁₆	
INT ₃ interrupt	7	FFF3 ₁₆ , FFF2 ₁₆	External interrupt (phase programmable)
CNTR ₁ interrupt	8	FFF1 ₁₆ , FFF0 ₁₆	External interrupt (phase programmable)
INT ₄ interrupt	9	FFEF ₁₆ , FFEE ₁₆	External interrupt (phase programmable)
Timer X interrupt	10	FFED ₁₆ , FFEC ₁₆	
CNTR ₀ interrupt	11	FFEB ₁₆ , FFEA ₁₆	External interrupt (phase programmable)
Timer 2 interrupt	12	FFE9 ₁₆ , FFE8 ₁₆	
Timer 3 interrupt	13	FFE7 ₁₆ , FFE6 ₁₆	
Serial I/O interrupt	14	FFE5 ₁₆ , FFE4 ₁₆	
INT ₅ interrupt	15	FFE3 ₁₆ , FFE2 ₁₆	External interrupt (phase programmable)
A-D conversion completion interrupt	16	FFE1 ₁₆ , FFE0 ₁₆	
BRK instruction interrupt	17	FFDF ₁₆ , FFDE ₁₆	Non-maskable software interrupt

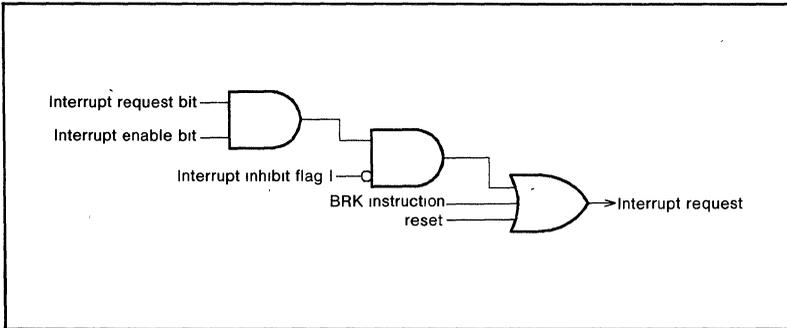


Fig.4 Interrupt control

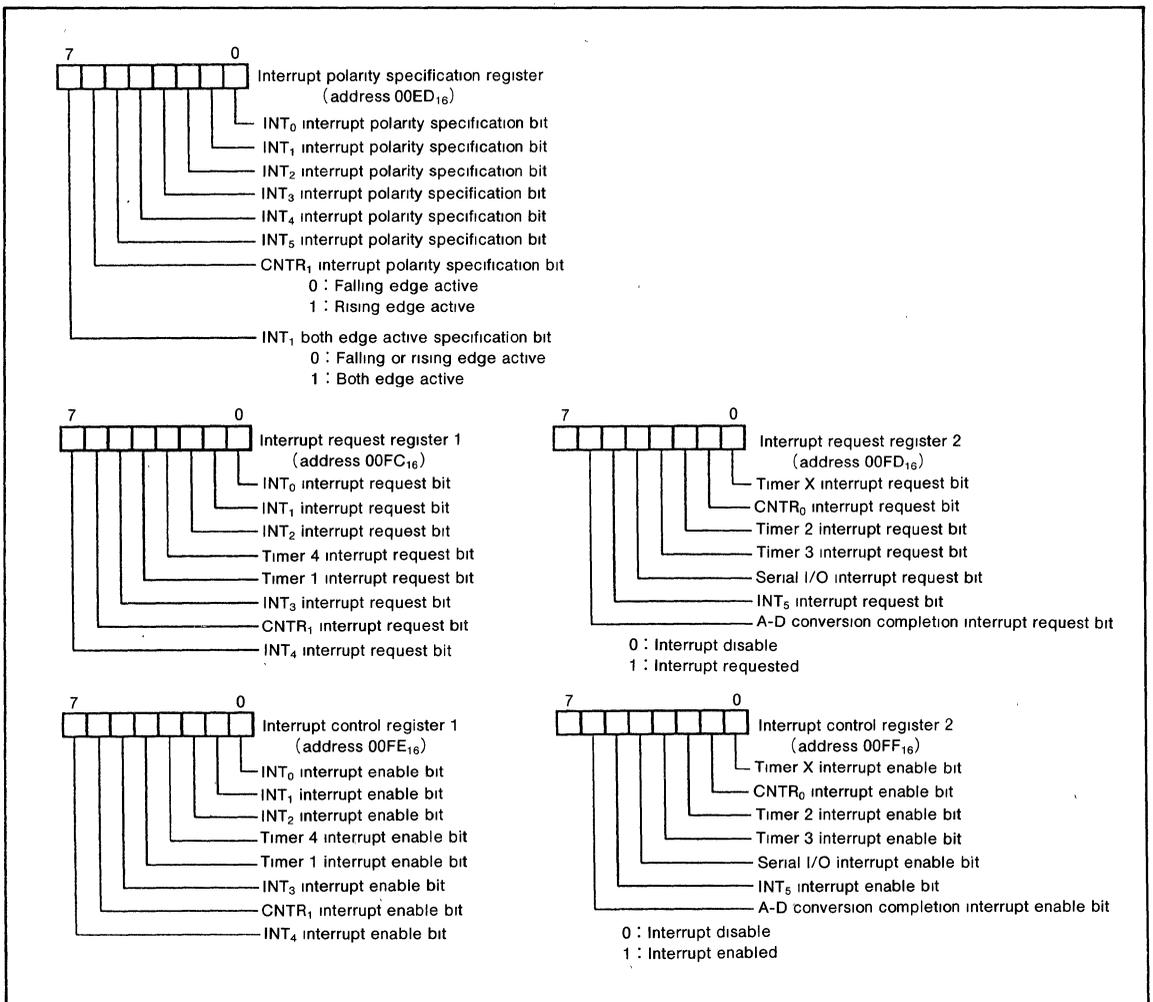


Fig.5 Structure of registers related to interrupt

TIMERS

The M37424M8-XXXSP has five timers : timer X, timer 1, timer 2, timer 3, and timer 4. A block diagram of these timers is shown in Figure 9.

Timer X is a 16-bit timer. It has an independent 16-bit timer latch and can be used in eight modes. The structure of the timer X mode register is shown in Figure 8, and the eight timer X modes are described below.

(1) 16-bit timer mode [000]

Basic mode in which timer X functions as a 16-bit reload timer and timer X generates an interrupt request when it overflows.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. This bit is "0" immediately after a reset.

The timer counts down the value which decrements by one from the value set in the latch. At the next count pulse after it reaches $FFFF_{16}$ from 0000_{16} , an timer X interrupt is generated, and at the same time the value in the timer latch is reloaded into the timer. The value is not reloaded into the timer until it overflows, even if the contents of the timer latch are overwritten.

When writing to the timer directly, write the upper value first, then the lower value. The upper value is overwritten at the same time that the lower value is written. When reading the timer, read the lower value first, then the upper value. At the point at which the lower value is read, the upper value is latched. If reading the lower value always read the upper value as well. There are no restrictions on which part of the timer latch should be written to or read first.

(2) Event counter mode [001]

Mode in which timer X operates in exactly the same way as in timer mode, except that the count source is the external pulse input from the CNTR₀ pin. The input polarity of the CNTR₀ pin can be selected by bit 6 of the timer X mode register : if this bit is "0", falling edges are counted ; if it is "1", rising edges are counted.

(3) Pulse width measurement mode 1 [010]

Mode in which timer X measures the width of "H" or "L" period of the external pulse input from the CNTR₀ pin.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. In this mode the timer counts up : at the same time that the measurement ends, the value in the timer is latched into the timer latch and a CNTR₀ interrupt request is generated.

Bit 6 of the timer X mode register selects whether the "H" period is measured or the "L" period. If this bit is "0", the

"L" period is measured ; if it is "1", the "H" period is measured.

(4) Pulse width measurement mode 2 [011]

Mode in which timer X continuously measures the width of both "H" and "L" periods of the external pulse input from the CNTR₀ pin.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. The value in the timer is latched at both the rising edges and falling edges of the external pulse, and a CNTR₀ interrupt request is generated. Whether the measured value is the "H" period or the "L" period can be determined by checking the level of the P6₂/CNTR₀ pin. This mode can be used to measure the duty cycle of external pulses.

(5) Pulse period measurement mode [100]

Mode in which timer X measures the period of the external pulse input from the CNTR₀ pin.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. If bit 6 of the timer X mode register is "0", the period from one falling edge to the next falling edge is measured ; if it is "1", the period from one rising edge to the next rising edge is measured. The measured value is latched in the timer latch, and a CNTR₀ interrupt request is generated.

(6) Pulse output mode [101]

Mode in which an waveform of duty cycle 50% which is inverted every time timer X overflows is output to the CNTR₀ pin.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16.

(7) Programmable waveform generation mode [110]

Mode in which the contents of the output level latch allocated to bit 5 of the timer X mode register are output to the CNTR₀ pin every time timer X overflows.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. Various different waveforms can be generated by updating the values in the output level latch, the timer and the timer latch, each time timer X overflows.

(8) Programmable one-shot generation mode [111]

Mode in which the active edge of an external pulse input from the P6₀/INT₀ pin sets the value of the timer latch into timer X, and timer X starts to count. The CNTR₀ pin goes "H" at the same time of the active edge of the INT₀ pin input, and goes "L" when timer X overflows.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. The active edge of the INT₀ pin is set by bit 0 of the interrupt polarity specification register, and is the same as the polarity of the INT₀ interrupt.

Note that if the CNTR₀ pin is used as a pulse output pin (in pulse output mode, programmable waveform generation mode, or programmable one-shot generation mode), bit 7 of the timer X mode register must be "1". If this bit switches from "0" to "1", an "L"-level signal will be output to the CNTR₀ pin. However, be aware that if timer X is switched to another pulse output mode while this bit is "1", the level output in the previous mode will still be held by the CNTR₀ pin.

Timer 1, timer 2, timer 3, and timer 4 are all 8-bit timers with 8-bit timer latches. Writing to a timer latch sets the corresponding timer at the same time, except that, if the value written to the latch is n , the value actually set in the timer is $(n-1)$. The timer has a count-down operation : at the next count pulse after it reaches FF₁₆ from 00₁₆, the value in the timer latch is reloaded into the timer. If the value in the timer latch is n , the divide ratio is $1/(n+1)$. At the same time, the interrupt request bit corresponding to that timer is set to "1". Set the count source for each timer by the timer 1, 2 mode register (address 00F8₁₆) or the timer 3, 4 mode register (address 00F9₁₆).

If an external clock is selected as the count source for timer 2, timer counts the P6₃/CNTR₁ pin input. An inverting waveform every time timer 2 overflows can be output to the P3₄/T_{OUT} pin, by setting bit 7 of the timer 1, 2 mode register to "1". The structure of the timer 1, 2 mode register is shown in Figure 6 and the structure of the timer 3, 4 mode register is shown in Figure 7

At reset, timer 3 is set to FF₁₆ and timer 4 is set to 07₁₆.

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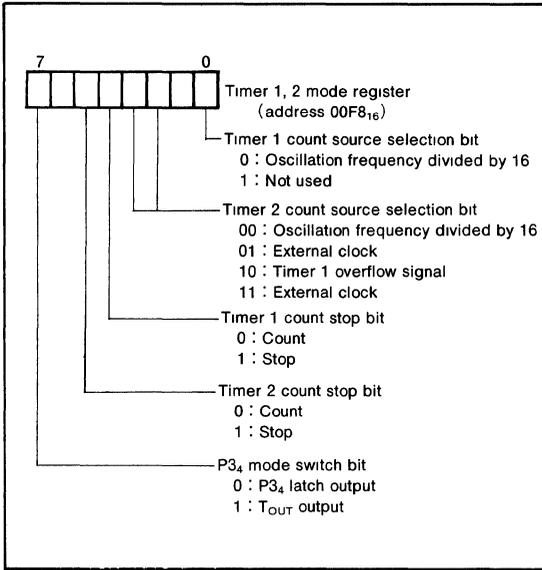


Fig.6 Structure of timer 1, 2 mode register

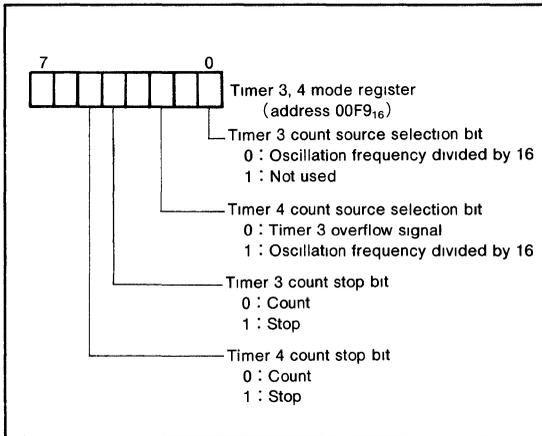


Fig.7 Structure of timer 3, 4 mode register

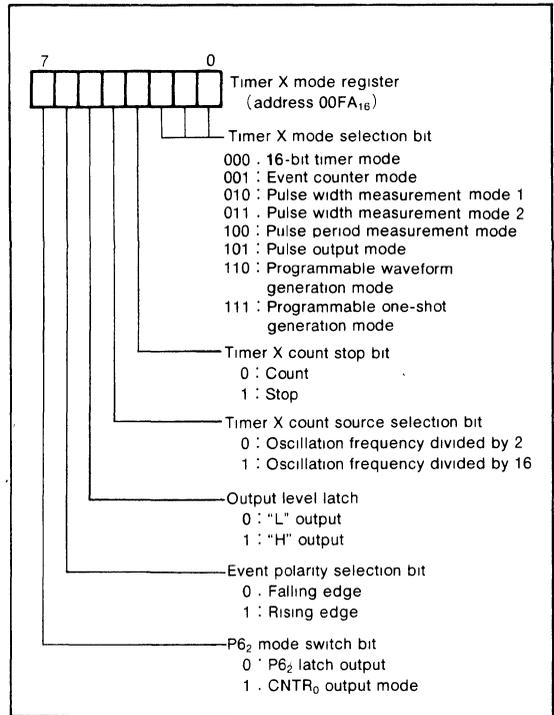


Fig.8 Structure of timer X mode register

SERIAL I/O

A block diagram of the serial I/O function is shown in Figure 11. The serial I/O receive enabled signal pin ($\overline{S_{RDY}}$), synchronous clock I/O pin (CLK), and data I/O pins (S_{OUT} , S_{IN}) also function as the $P3_3$, $P3_2$, $P3_1$, and $P3_0$ of the port P3.

The serial I/O mode register has an 8-bit structure. Bits 1 and 0 select the synchronous clock : the oscillation frequency is divided by 8 if they are [00], by 16 if they are [01], by 128 if they are [10], or by 512 if they are [11]. Bit 2 selects an external clock.

Bits 3 and 4 are used to select whether part of port P3 is used for serial I/O. If bit 3 is "1", the $P3_2$ is the I/O pin for the synchronous clock .

The $P3_1$ is the serial data output pin and the $P3_0$ is the serial data input pin, set the bit in the directional register corresponding to $P3_0$ to "0" to set input mode. If serial I/O is being used, bit 3 must be set to "1". When bit 3 is "0", the $P3_2$ functions as an ordinary I/O pin.

Bit 4 selects whether the $P3_3$ is used as the output pin for the receive enabled signal $\overline{S_{RDY}}$. If this bit is "1", the $\overline{S_{RDY}}$ signal is output ; if it is "0", the $P3_3$ is an ordinary I/O pin.

Serial I/O register H and serial I/O register L are 8-bit registers for data transfer that can be used in both transmission and reception. For 8-bit transfer, serial I/O register L

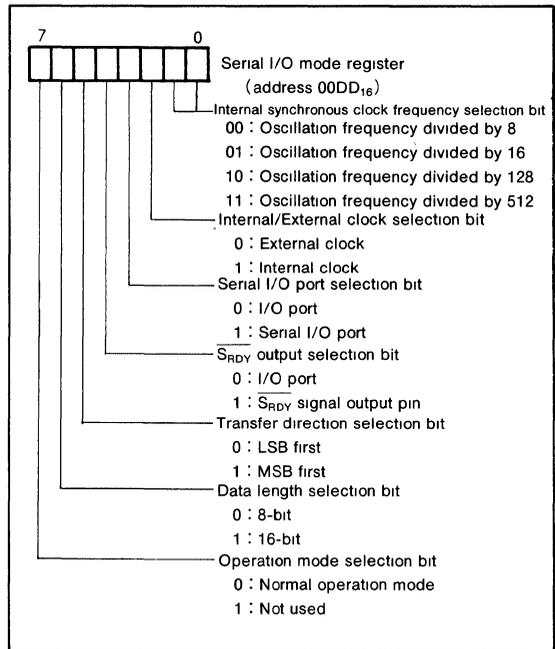


Fig.10 Structure of serial I/O mode register

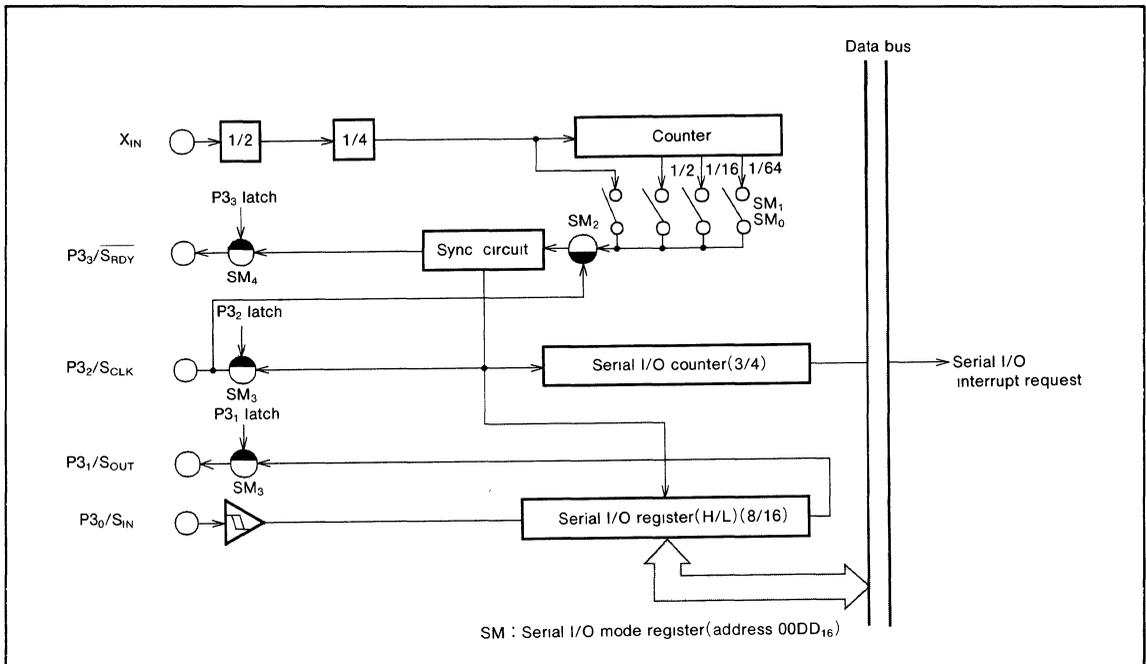


Fig.11 Block diagram of serial I/O

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(address $00DE_{16}$) is used ; for 16-bit transfer, serial I/O register H (address $00DF_{16}$) is used for the upper byte and serial I/O register L for the lower byte. The data length to be transferred can be selected either 8 bits or 16 bits by setting bit 6 of the serial I/O mode register. Whether data transfer is MSB first or LSB first can be selected by setting bit 5 of the serial I/O mode register.

The operation of the serial I/O function will now be described. The operation differs depending on whether the internal clock or an external clock is selected as the synchronous clock. Use with the internal clock will be described first.

If the serial I/O register L is written to, the $\overline{S_{RDY}}$ signal is at "H" during the write cycle ; it then goes "L" when the write cycle ends to indicate reception enabled status. If the serial I/O register's transfer clock goes "L" even once, the $\overline{S_{RDY}}$ signal goes "H". During the write cycle to the serial I/O register, "7" is set in the serial I/O counter for 8-bit transfer or "15" for 16-bit transfer, and the serial I/O register's transfer clock is forced to "H". After the write cycle ends, data is output to the P3₁ pin each time the transfer clock goes from "H" to "L". Data is input from the P3₀ pin

each time the transfer clock goes from "L" to "H" and, at the same time, the contents of the serial I/O register are shifted one bit. If bit 5 of the serial I/O mode register is "0", the data enters from the MSB and shifts to the right, if it is "1", the data enters from the LSB and shifts to the left.

When the serial I/O counter reaches "0" after counting either 8 or 16 transfer clocks, the transfer clock stops at "H" and the corresponding interrupt request bit is set.

If an external clock is selected as the synchronous clock, it must be controlled externally because, although the interrupt request bit is set, the transfer clock does not stop. Use a clock of no more than 500kHz with a duty cycle of 50% as the external clock.

The timing at which 8-bit data is transferred LSB-first is shown in Figure 12. If an external clock is used for the transfer, the external clock must be "H" when the serial I/O counter is initialized. Make sure that the serial I/O counter is initialized after the transfer clock switches. Initialize by writing to the serial I/O register H.

A connection example for transferring data from one M37424M8-XXXSP to another is shown in Figure 13.

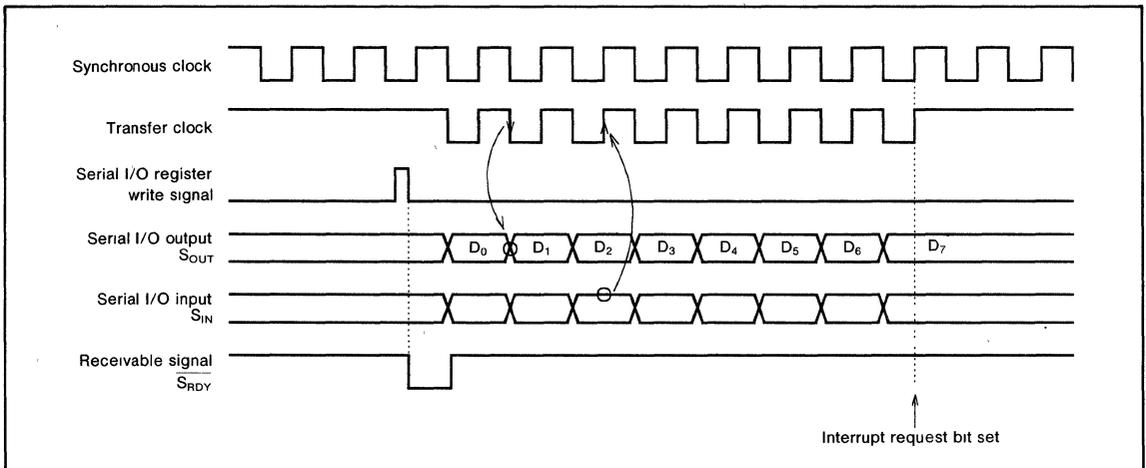


Fig.12 Serial I/O timing

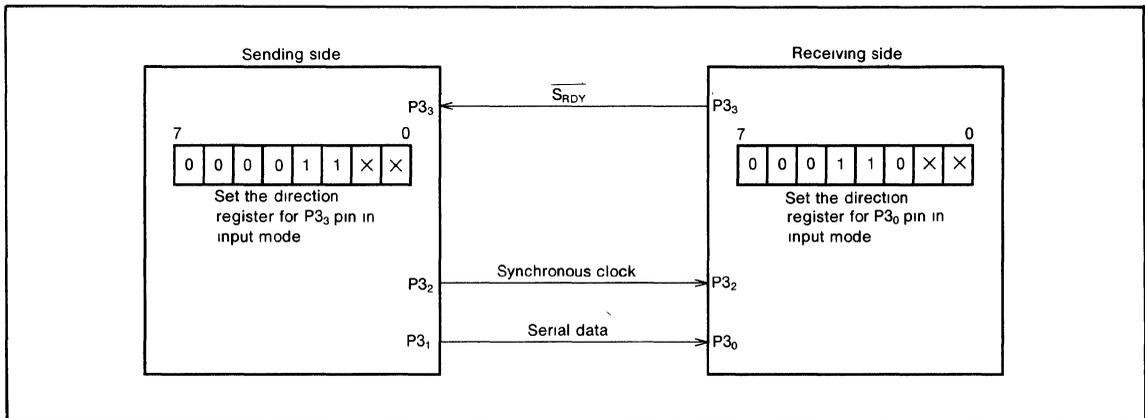


Fig.13 Example of serial I/O connection

PWM OUTPUT CIRCUIT

The M37424M8-XXXSP has a PWM function with a 14-bit resolution, a repeat period of 8192 μ s when the oscillation frequency X_{IN} is 4MHz (the explanation in the rest is based on the assumption that X_{IN}=4MHz), and a minimum bit resolution width of 500ns. If data is set in the lower 6 bits of the pulse width modulation register L (PWM-L : address 00D5₁₆) and the pulse width modulation register H (PWM-H : address 00D4₁₆), and the port P5₄ function selection bit (bit 0 of the special function selection register) is set to "1", a PWM waveform is output from port P5₄.

The period of 8192 μ s is resolved into 16,384 minimum pulse widths (500ns), and the pulse width can be modulated in 500ns units in accordance with the 14 bits of data written into PWM-H and PWM-L. By dividing the 8192 μ s repeat period into 64 short-area periods, pulses of approximately equal width can be output at a 128 μ s period. A block diagram of the PWM circuit is shown in Figure 14.

The data written to the PWM register is transferred to the PWM latch at the repetition of the PWM period. The signals output to the PWM pin correspond to the contents of this latch. When data of PWM-L register is read, data in this latch has already been read allowing the data output by the PWM to be confirmed. In this case, the upper 2 bits of the 8-bit register becomes undefined. However, bit 7 of the PWM-L register indicated the completion of the data transfer from the PWM-L register to the PWM latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

The timing diagram of the 14-bit PWM is shown in Figure 15. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area with a length N times τ is output every short area of $t=256 \times \tau = 128\mu$ s as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 15.)

The contents of the lower 6 bits of data enable the lengthening of the high signal by τ .

Thus, the time for the high-level area is equal to the time set by the higher 8 bits or that plus τ . As a result, the short-area period $t(=128\mu$ s, approx. 7.8kHz) becomes an approximately repetitive period.

At reset the output of port P5₄ is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data	Area longer by τ than that of other t_m ($m = 0 \sim 63$)
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m=32$
0 0 0 0 1 0	$m=16, 48$
0 0 0 1 0 0	$m=8, 24, 40, 56$
0 0 1 0 0 0	$m=4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m=1, 3, 5, 7, \dots, 57, 59, 61, 63$

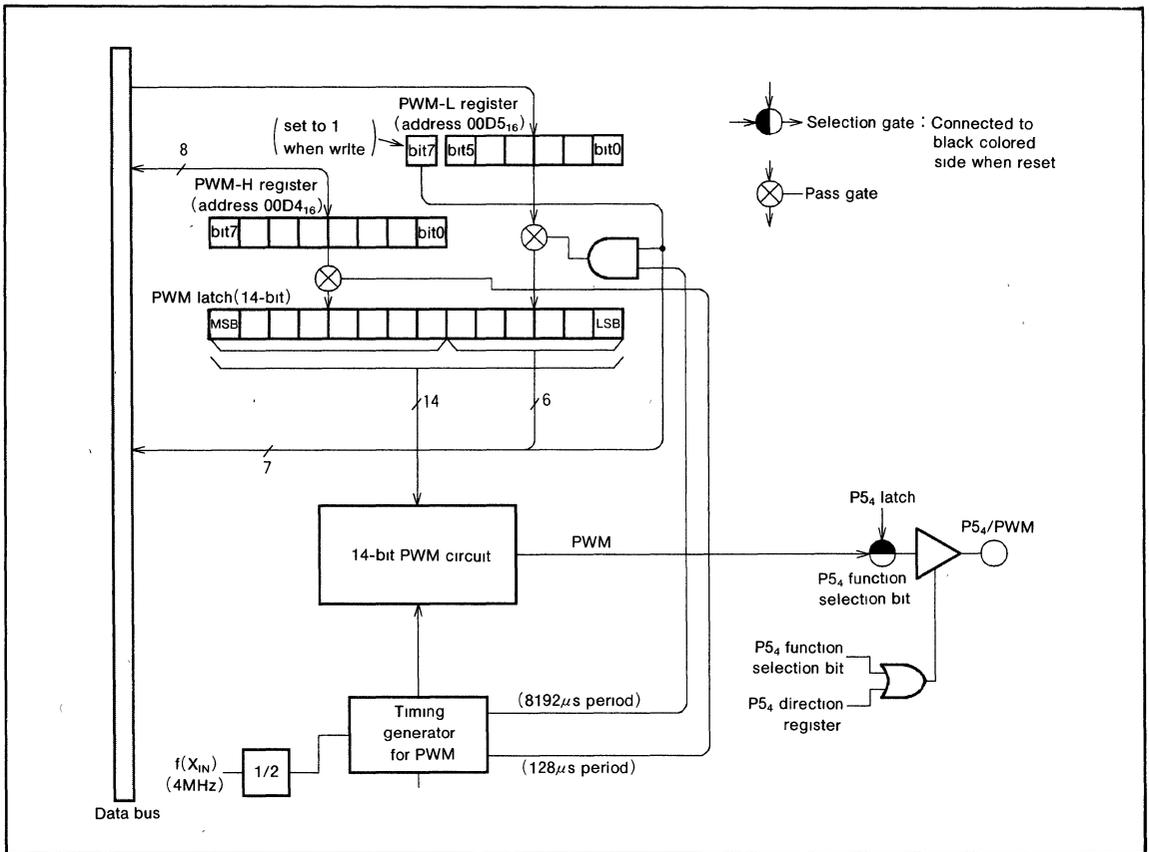


Fig.14 Block diagram of PWM circuit

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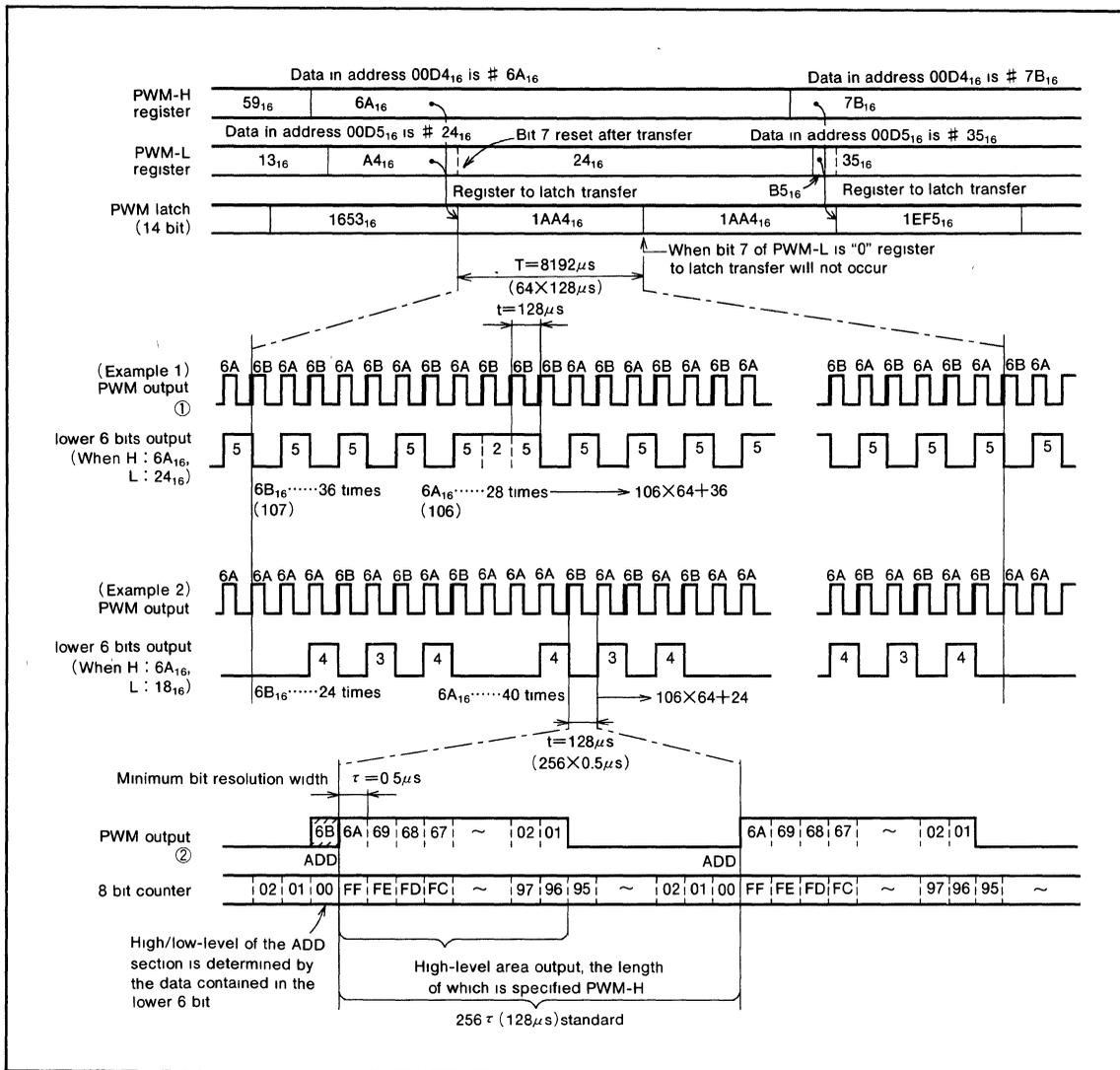


Fig.15 14-bit PWM timing diagram

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A-D CONVERTER

An 8-bit successive approximation method of A-D conversion is employed providing a precision of $\pm 3\text{LSB}$. A block diagram of the A-D converter is shown in Figure 16. Conversion is automatic once it is started with the program.

The analog inputs are used in common with port P4. Bits 2, 1 and 0 of the A-D control register (address 00DA_{16}) are used to select which pins are used for A-D conversion. The input condition is accomplished by setting to "0" the bit in the directional register that corresponds to the pin where A-D conversion is to take place. Bit 3 of the A-D control register is the A-D conversion end bit. During A-D conversion, this bit is "0", and upon completion becomes "1". Thus, it can be ascertained whether A-D conversion has been completed or not by inspecting this bit. The relation between the contents of the A-D control register and the selection of input pins are shown in Figure 17.

The results of the conversion can be found by reading the contents of the successive approximation register address 00D9_{16} which stores the results of the conversion.

The procedure for executing A-D conversion is next explained. Firstly, the pin that is to be used for the A-D conversion is selected by setting bit 2, bit 1 and bit 0 of the A-D control register.

Next, clear the A-D conversion end bit to "0".

When the above is done, A-D conversion is started. A-D conversion completes after 49 clock cycles upon which the A-D conversion end bit is set to "1" and the results of the conversion can be found in the successive approximation register. Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion.

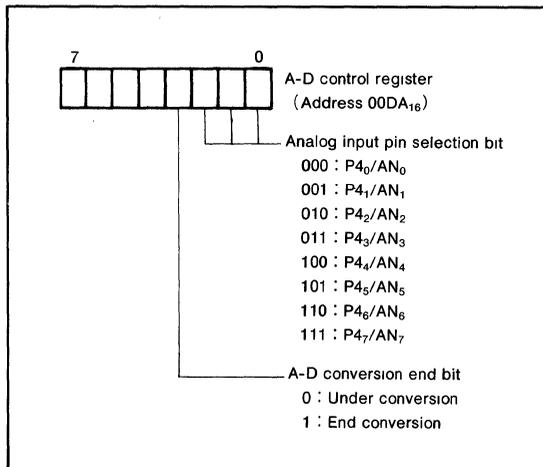


Fig.17 Structure of A-D control register

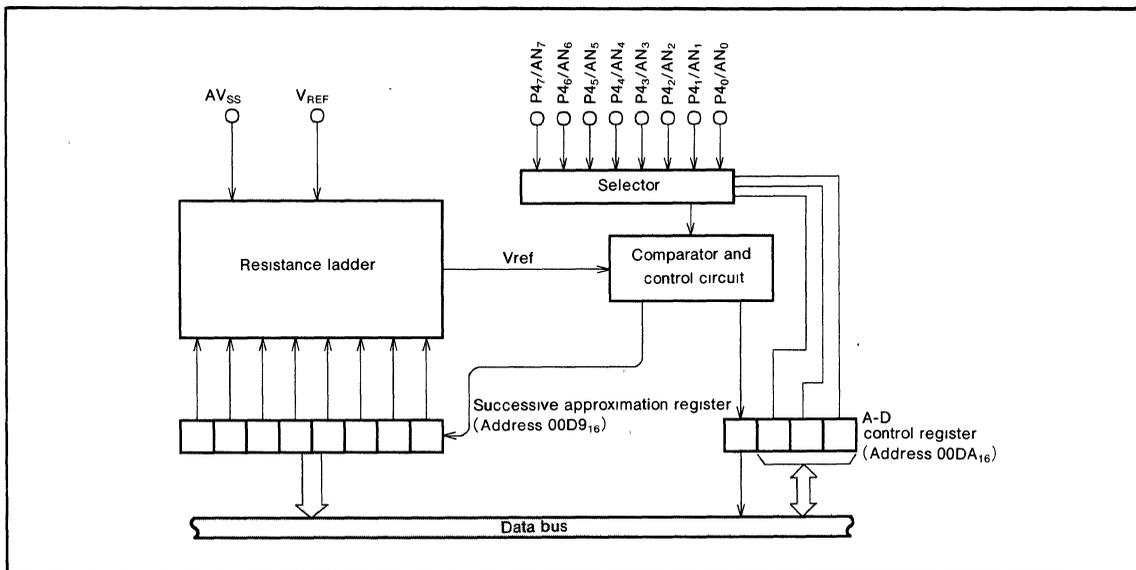


Fig.16 Block diagram of A-D converter

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D-A CONVERTER

The M37424M8-XXXSP has two 8-bit resolution, R-2R method D-A converters and two 5-bit resolution D-A converters. A block diagram of the D-A converters is shown in Figure 19.

If a value is written into one of the D-A conversion registers corresponding to these D-A converters, an analog voltage equivalent to that digital value is generated by the ladder resistors. If the corresponding D-A output enable bit (bit 0 to bit 3 of the D-A output enable register) is set to "1", that value is output to the corresponding output pin P6₄/DA₁ to P6₇/DA₄. In this case, the directional register of that pin must be set to "0" to set input mode.

The relationship between analog voltage and digital value is as follows :

$$V = V_{REF} \times n / 256 (n=0 \text{ to } 255) : DA_1 \text{ and } DA_2$$

$$V = V_{REF} \times n / 32 (n=0 \text{ to } 31) : DA_3 \text{ and } DA_4$$

Where V is the output voltage, V_{REF} is the reference voltage, and n is the value in the D-A conversion register.

At reset, the P6₄/DA₁ to P6₇/DA₄ pins go to high impedance. D-A output does not have a built-in buffer, so if connecting a low-impedance load, connect an external buffer as well.

The structure of the D-A output enable register is shown in Figure 18.

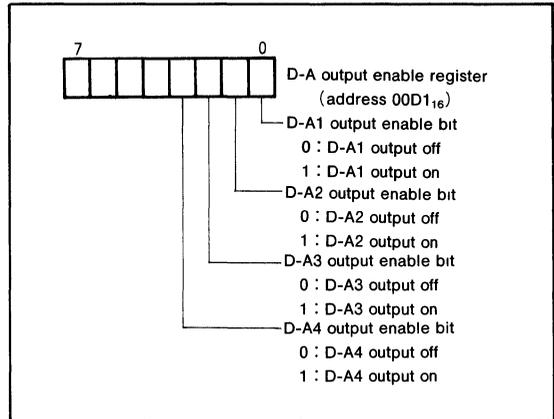


Fig.18 D-A output enable register

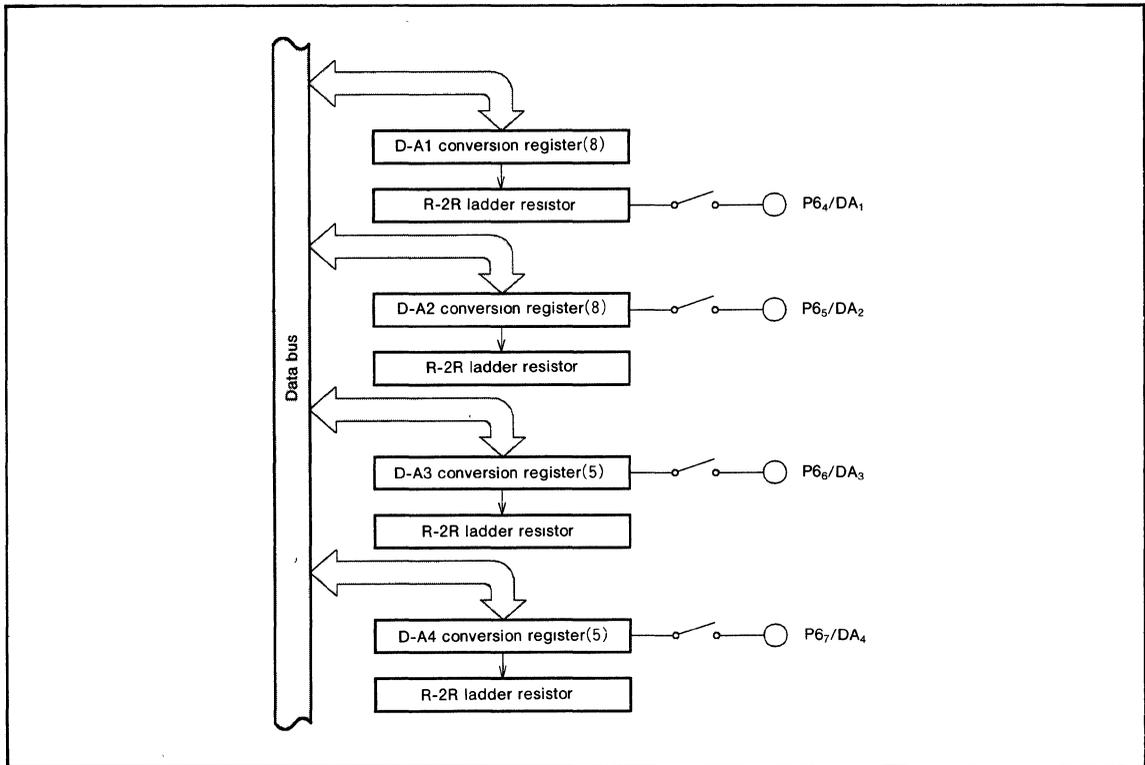


Fig.19 Block diagram of D-A converter

EXTERNAL TRIGGER OUTPUT

Port P5₅ operates as the pin Q which outputs the external trigger signal. Port P6₁ operates as the pin T which inputs the trigger clock. By setting bit 1 of the special function selection register (address 00EE₁₆) to "1", the P6₁/T/INT₁ pin functions a trigger input pin and P6₁, P5₅ can be used as the external trigger function pins.

In external trigger mode, the value set by the external trigger output data bit is output to port P5₅ each time the active edge specified by bits 1 and 7 of the interrupt polarity specification register. Combinations of bits 3 and 4 of the special function selection register set port P5₅ to output mode as shown in Table 3. If using external trigger output, set the P5₅ directional bit to "0". At reset, this bit is cleared to "0".

Table 3. External trigger output

External trigger output direction specify bit	External trigger output data bit	
	0	1
0	High-impedance	High-impedance
1	L	H

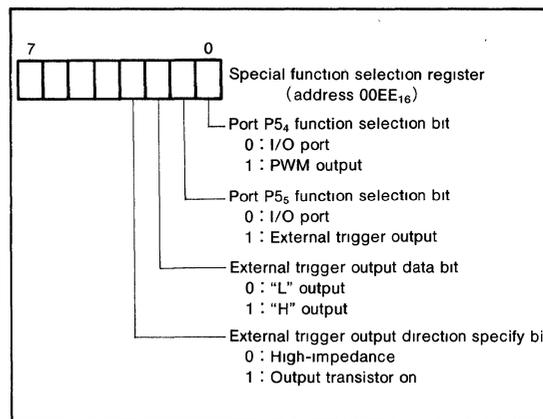


Fig.20 Structure of special function selection register

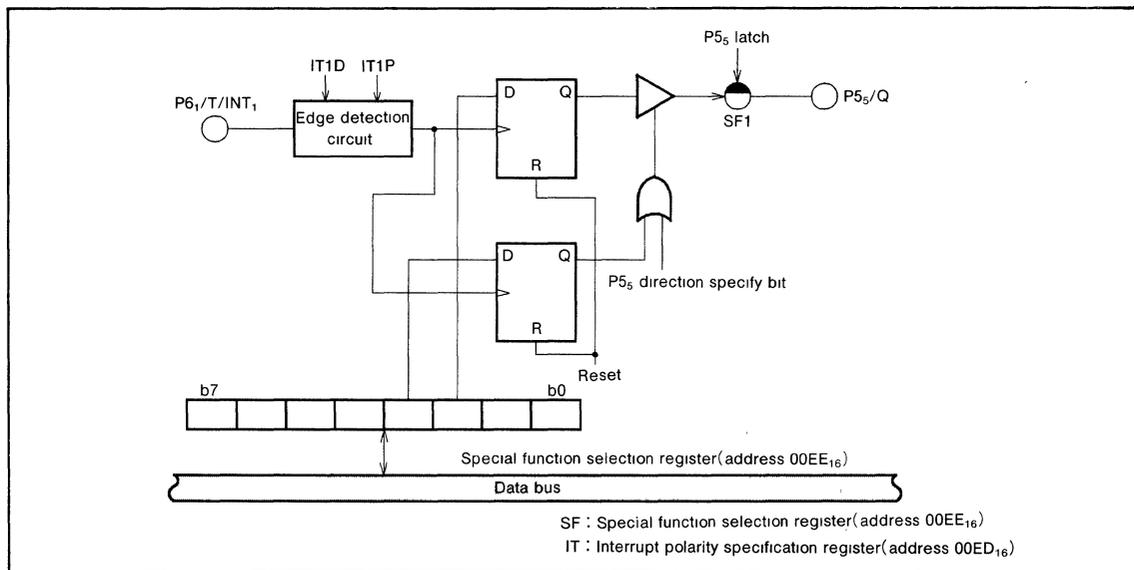


Fig.21 Block diagram of external trigger output

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V PULSE AND Y PULSE GENERATOR

Port P5₆ operates as the VPLS pin to output the V pulse and port P6₁ operates as the T pin to input the trigger clock. P5₆ can be used as the V pulse output by setting bit 5 of the V pulse control register (00D8₁₆) to "1". Port P5₇ operates as the YPLS pin which outputs the Y pulse. It can be used as the Y pulse (VPF signal) output by setting bit 6 of the V pulse control register to "1". Effective edge of trigger input can be selected by setting bits 2 and 3 of V pulse control register. Figure 22 shows the block diagram of the V pulse, Y pulse generator. Figure 23 shows the timing diagram of the V pulse and Y pulse.

At the falling or rising edge of T, the VPP counter starts. By the overflow signal of the VPP counter, VPLS goes "H". By the overflow signal of VPP counter, the VPN counter starts. By the overflow signal of the VPN counter, VPLS goes "L". When the VPP counter or the VPN counter is counting, bit 4 of the V pulse control register is "1".

The preset value of the VPP counter can be set by the 9-bit register with bit 1 of the V pulse control register being the most significant bit and the V pulse preset value P (00D6₁₆) being the low-order eight bits. The preset value

of the VPN counter can be set by the 9-bit register with bit 0 of the V pulse control register being the most significant bit and the V pulse preset value N (00D7₁₆) being the low-order eight bits.

Note that values of bits 0 and 1 of the V pulse control register are the current counting values in the VPP counter and the VPN counter, not the preset values of the counters.

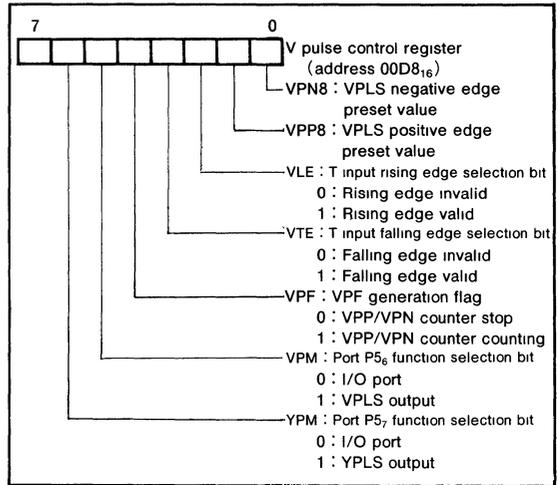


Fig.22 Structure of V pulse control register

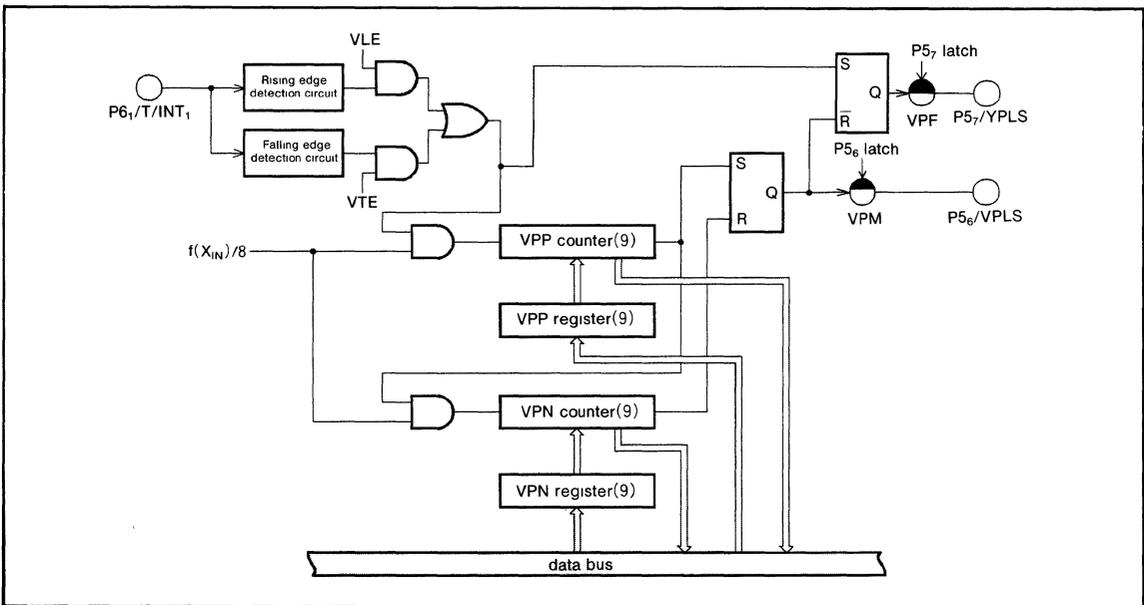


Fig.23 Block diagram of V pulse and Y pulse generator

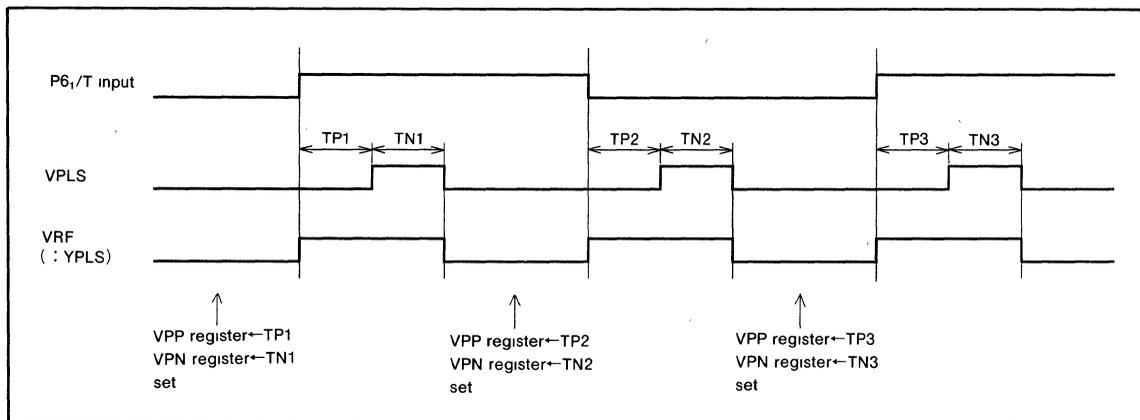


Fig.24 Timing diagram of the V pulse and Y pulse

WATCHDOG TIMER

The watchdog timer provides a method of returning to reset status if a runaway or other cause prevents a program from running a loop normally.

The watchdog timer is a 15-bit counter consisting of a lower seven bits and an upper eight bits (address 00EF₁₆). At reset or after the watchdog timer is written to, 7FFF₁₆ is set in this timer and it starts to count.

When the MSB reaches "0", an internal reset is generated. Therefore programs should normally be written to ensure that the watchdog timer is written to before this bit reaches

"0". If address 00EF₁₆ is read, the value in the upper eight bits of the counter is read. Directly after a reset, the watchdog timer is stopped. After reset is released, the first write to address 00EF₁₆ validates the watchdog timer function.

The count source of the lower seven bits is a signal that is the system clock ϕ divided by eight. The count source of the upper eight bits can be selected as either the overflow signal from the 7-bit counter or a signal that is the system clock ϕ divided by eight, depending on the value of bit 3 of the CPU mode register (address 00FB₁₆).

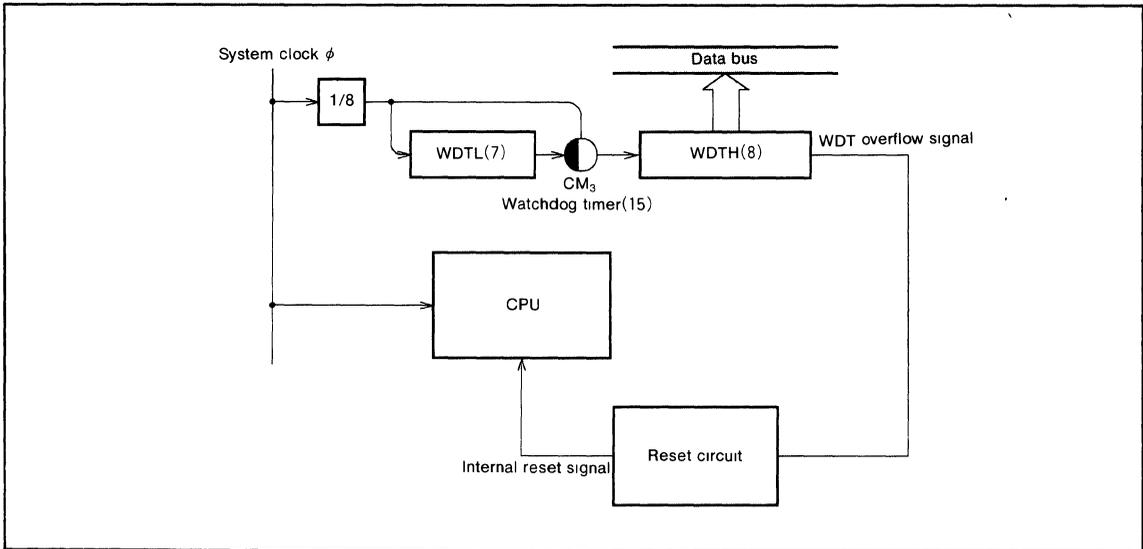


Fig.25 Block diagram of runaway detection function

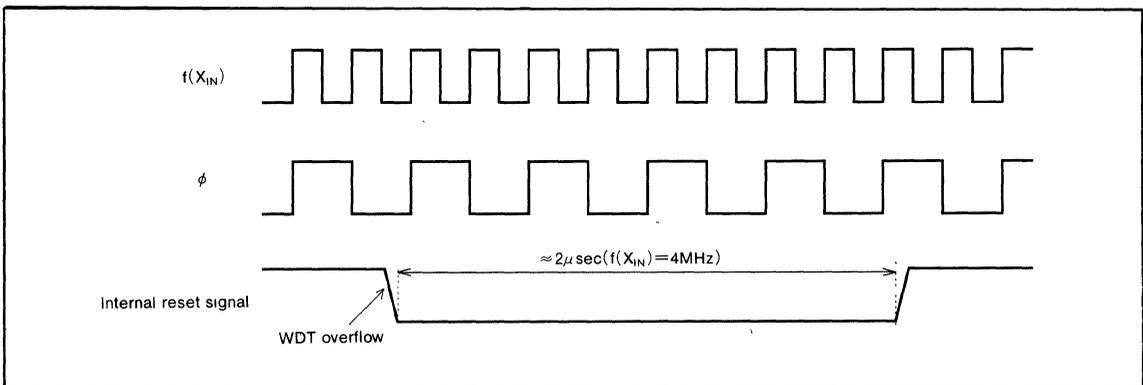


Fig.26 Timing diagram of internal reset signal

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I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00C0_{16}$. Port P0 has a directional register (address $00C1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

(2) Port P1

Port P1 has the same function as Port P0. The output structure of M37424M8-XXXSP is CMOS output. The output structure of M37524M4-XXXSP is N-channel open drain output.

(3) Port P2

Port P2 has the same function as Port P0.

(4) Port P3

Port P3 has the same function as port P0, but it has N-channel open drain output. Port P3 can also be used as serial I/O and timer output pins.

(5) Port P4

Port P4 has the same function as port P0. $P4_7$ through $P4_0$ can also be used as analog input pins AN_7 through AN_0 .

(6) Port P5

Port P5 has the same function as port P0. Port P5 can also be used as $INT_2 \sim INT_5$, PWM output, external trigger output Q and V pulse, Y pulse output pins.

(7) Port P6

Port P6 has the same function as port P0. Port P6 can also be used as INT_0 , INT_1 , trigger clock input T, timer I/O and D-A output pins.

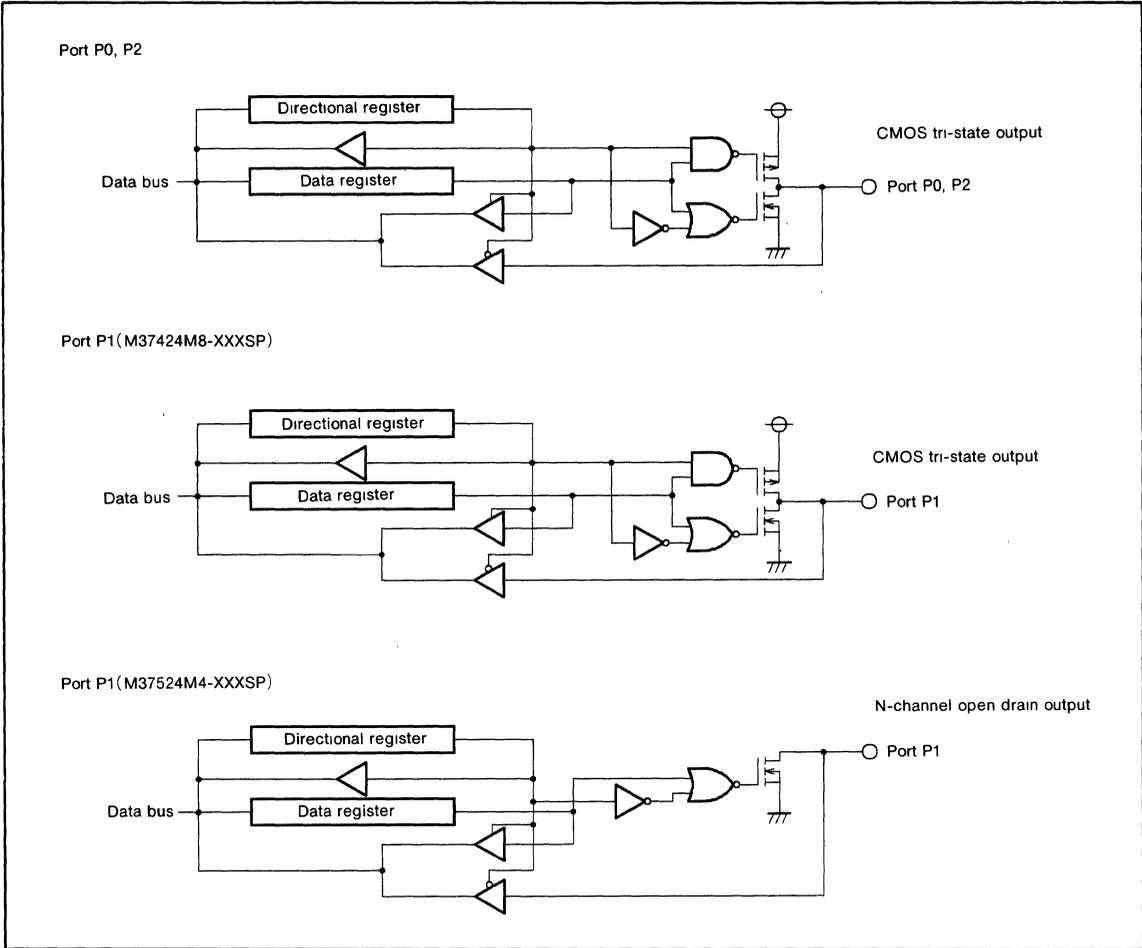


Fig.27 Block diagram of ports P0~P6(1)

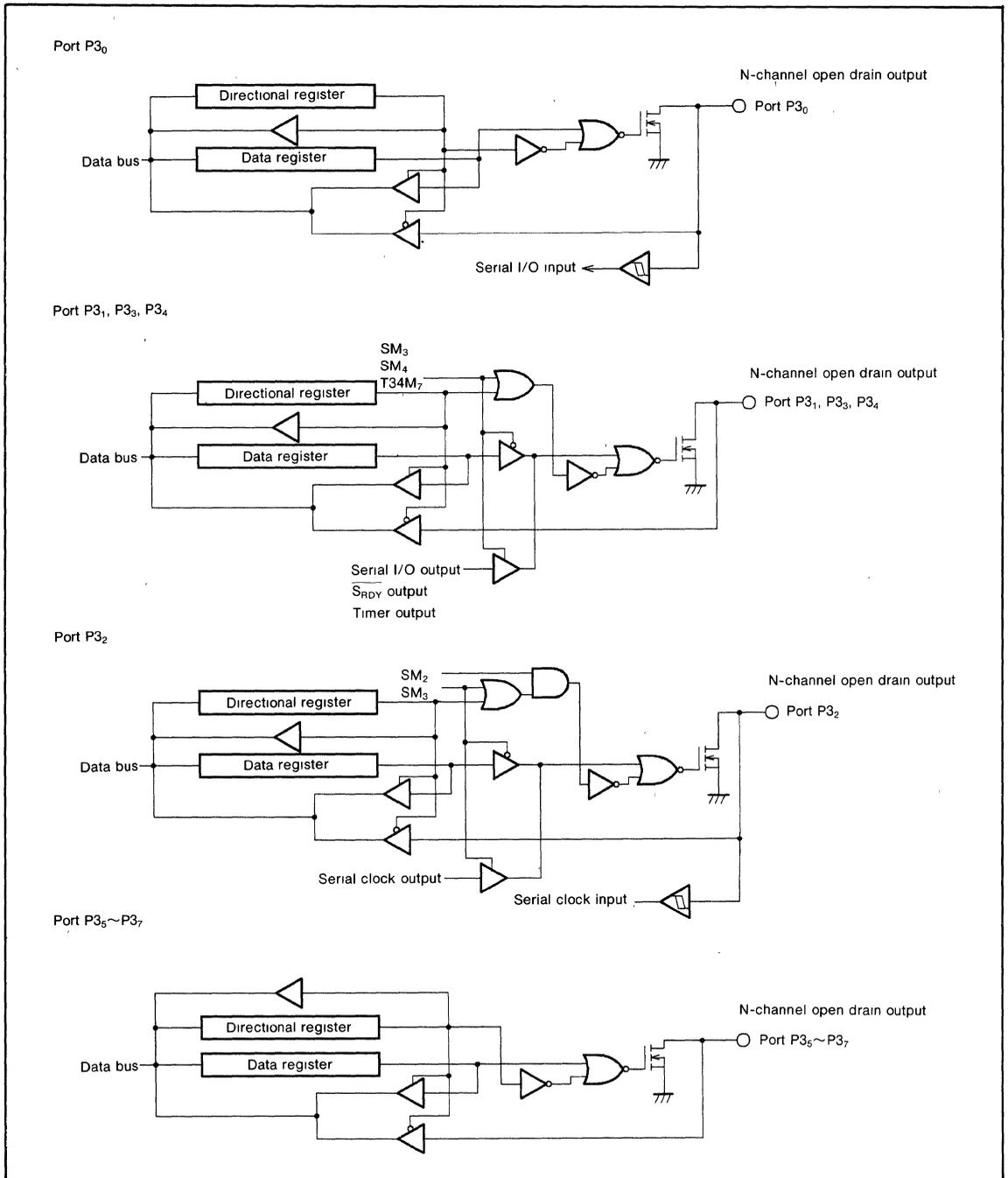


Fig.28 Block diagram of ports P0~P6 (2)

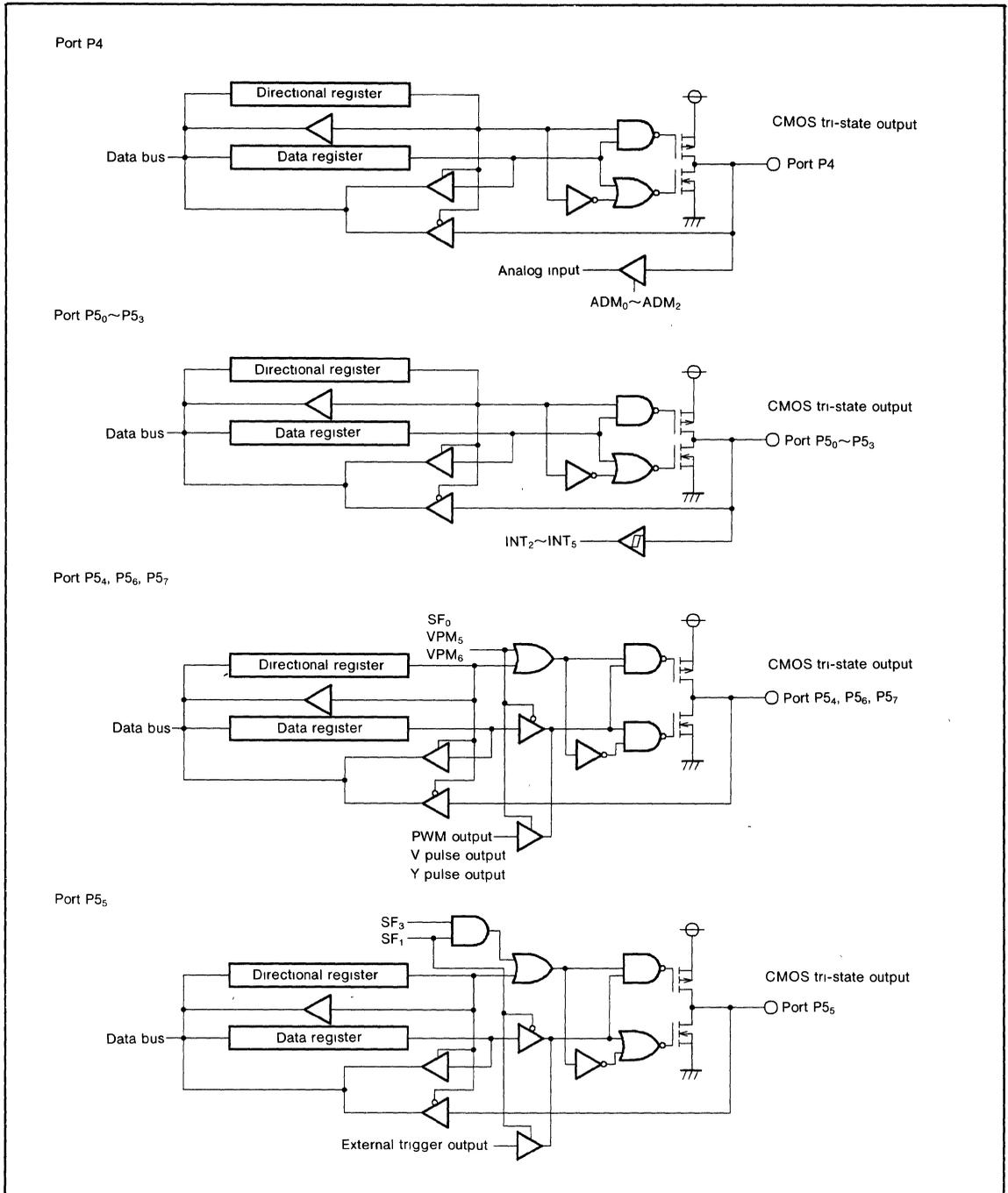


Fig.29 Block diagram of ports P0~P6 (3)

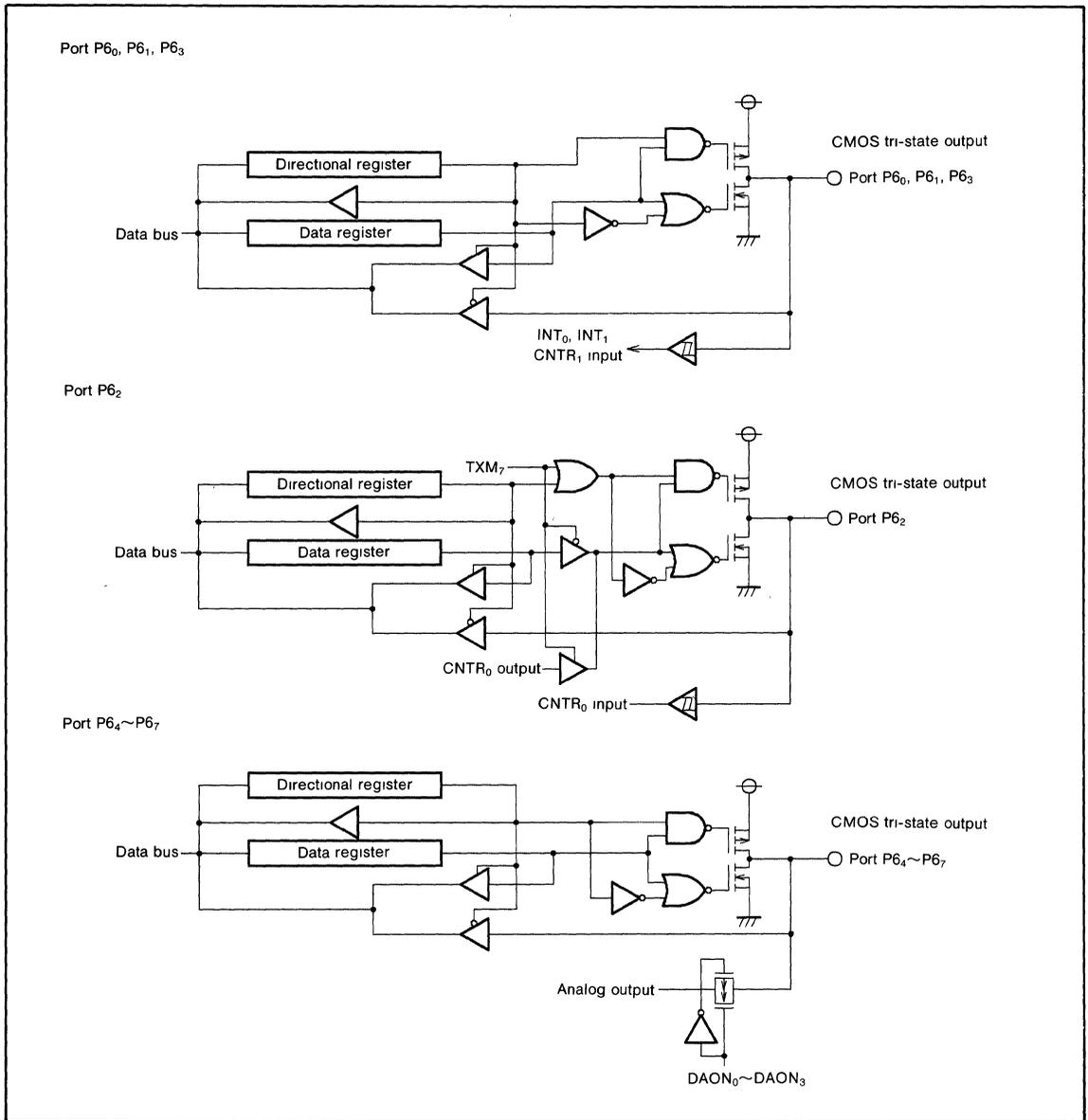


Fig.30 Block diagram of ports P0~P6 (4)

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RESET CIRCUIT

The M37424M8-XXXSP is reset according to the sequence shown in Figure 31. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for more than $2\mu\text{s}$ while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 33. An example of the reset circuit is shown in Figure 32. When the power on reset is used, the $\overline{\text{RESET}}$ pin must be held "L" until the oscillation of X_{IN} - X_{OUT} becomes stable.

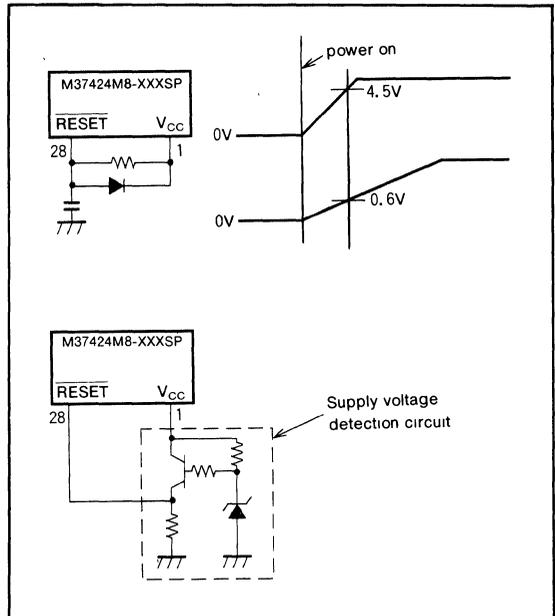


Fig.32 Example of reset circuit

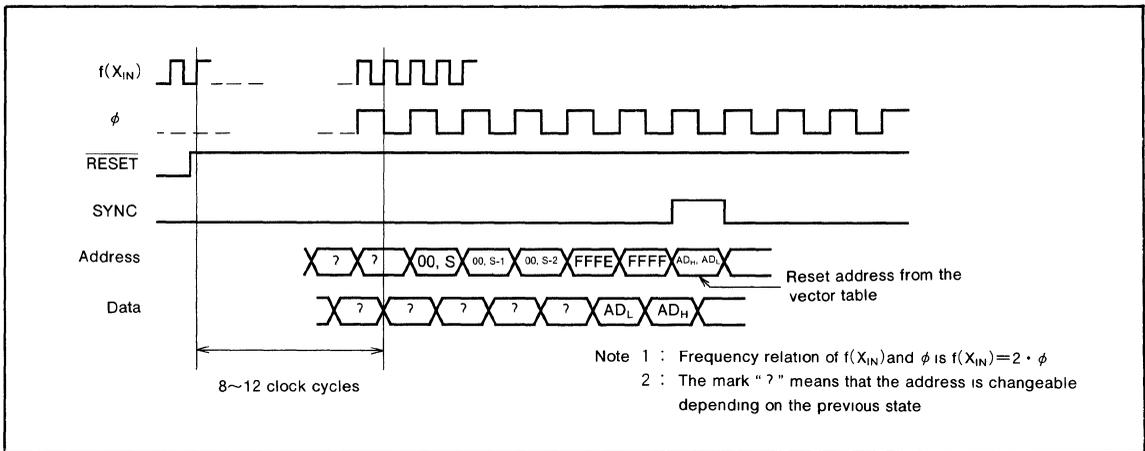


Fig.31 Timing diagram at reset

	address	
(1) Port P0 directional register	(C 1 ₁₆)	00 ₁₆
(2) Port P1 directional register	(C 3 ₁₆)	00 ₁₆
(3) Port P2 directional register	(C 5 ₁₆)	00 ₁₆
(4) Port P3 directional register	(C 7 ₁₆)	00 ₁₆
(5) Port P4 directional register	(C 9 ₁₆)	00 ₁₆
(6) Port P5 directional register	(C B ₁₆)	00 ₁₆
(7) Port P6 directional register	(C D ₁₆)	00 ₁₆
(8) D-A output enable register	(D 1 ₁₆)	0 0 0 0
(9) D-A3 conversion register	(D 2 ₁₆)	00 ₁₆
(10) D-A4 conversion register	(D 3 ₁₆)	00 ₁₆
(11) V pulse control register	(D 8 ₁₆)	0 0 0 0
(12) A-D control register	(D A ₁₆)	0 0 0 0
(13) D-A1 conversion register	(D B ₁₆)	00 ₁₆
(14) D-A2 conversion register	(D C ₁₆)	00 ₁₆
(15) Serial I/O mode register	(D D ₁₆)	00 ₁₆
(16) Interrupt polarity specification register	(E D ₁₆)	00 ₁₆
(17) Special function selection register	(E E ₁₆)	0 0 0 0
(18) Watchdog timer	(E F ₁₆)	7FF ₁₆
(19) Timer 3	(F 2 ₁₆)	FF ₁₆
(20) Timer 4	(F 3 ₁₆)	07 ₁₆
(21) Timer 1, 2 mode register	(F 8 ₁₆)	0 0 0 0 0 0
(22) Timer 3, 4 mode register	(F 9 ₁₆)	0 0 0 0
(23) Timer X mode register	(F A ₁₆)	00 ₁₆
(24) CPU mode register	(F B ₁₆)	1 0 1 0 0
(25) Interrupt request register 1	(F C ₁₆)	00 ₁₆
(26) Interrupt request register 2	(F D ₁₆)	00 ₁₆
(27) Interrupt control register 1	(F E ₁₆)	00 ₁₆
(28) Interrupt control register 2	(F F ₁₆)	00 ₁₆
(29) Processor status register	(P S)	1
(30) Program counter	(P C _H)	Contents of address FFFF ₁₆
	(P C _L)	Contents of address FFFE ₁₆

Fig. 33 Internal state of microcomputer at reset

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 36. When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once. To return from the wait status, the interrupt enable bit must be set to "1" before executing WIT instruction.

Since the M37424M8-XXXSP does not have STP instruction, the oscillation can not be stopped.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 34.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 35. X_{IN} is the input, and X_{OUT} is open.

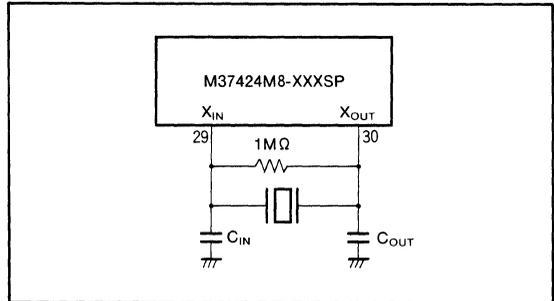


Fig.34 External ceramic resonator circuit

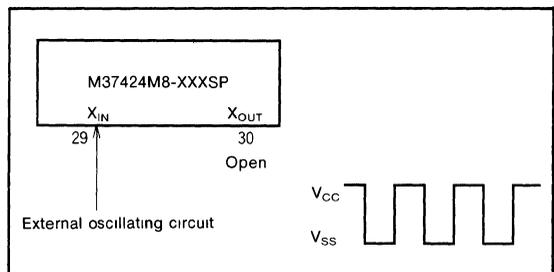


Fig.35 External clock input circuit

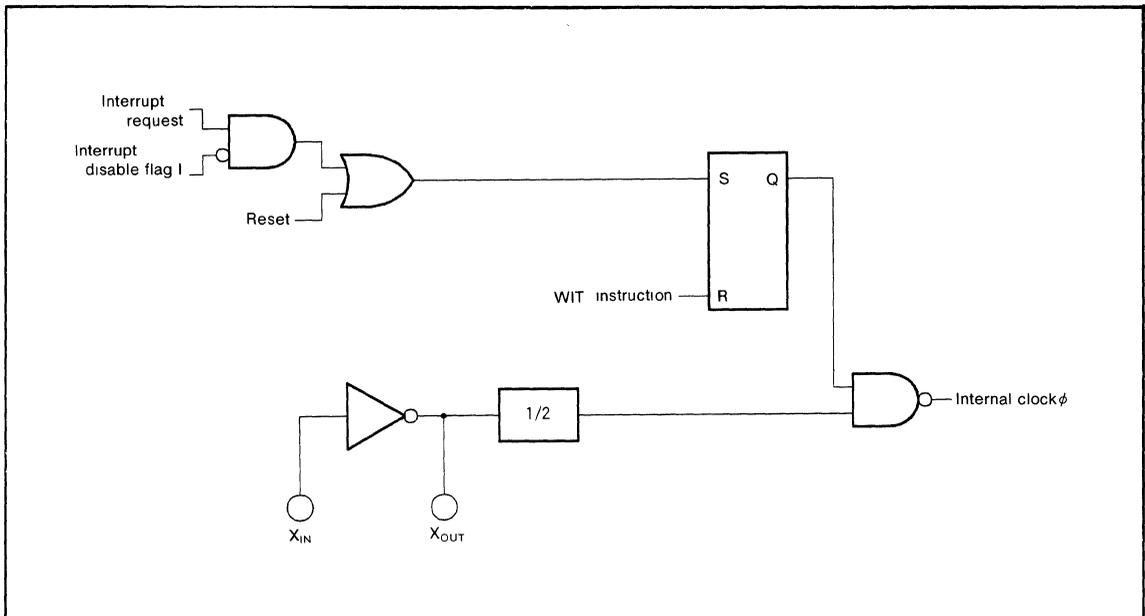


Fig.36 Block diagram of the clock generating circuit

PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (4) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mask specification form
- (3) ROM data EPROM 3sets

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M37524M4-XXXSP

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M37424M8-XXXSP
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS} Output transistors are at "OFF" state	-0.3~7	V
V _{SS}	Supply voltage		0	V
V _{REF}	Reference voltage		-0.3~V _{CC} +0.3	V
V _I	Input voltage X _{IN} , RESET, P ₃₀ ~P ₃₇ , CNV _{SS}		-0.3~7	V
V _I	Input voltage P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇		-0.3~V _{CC} +0.3	V
V _O	Output voltage P ₃₀ ~P ₃₇		0.3~7	V
V _O	Output voltage P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ , X _{OUT} , φ		-0.3~V _{CC} +0.3	V
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=-10~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage		0		V
V _{IH}	"H" input voltage P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ , INT ₀ ~INT ₅ , CNTR ₀ , CNTR ₁ , T, RESET, X _{IN}	0.8V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ , INT ₀ ~INT ₅ , CNTR ₀ , CNTR ₁ , T	0		0.2V _{CC}	V
V _{IL}	"L" input voltage RESET	0		0.12V _{CC}	V
V _{IL}	"L" input voltage X _{IN}	0		0.16V _{CC}	V
I _{OH(peak)}	"H" peak output current P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 1)			-10	mA
I _{OH(avg)}	"H" average output current P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 1)			-5	mA
I _{OL(peak)}	"L" peak output current P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 2)			10	mA
I _{OL(avg)}	"L" average output current P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 2)			5	mA
f(X _{IN})	Clock oscillating frequency			4	MHz

- Note 1. The total of "H" peak output current of port P0, P1, P2, P4, P5 and P6 is less than 65mA
 2. The total of "L" peak output current of port P0, P1, P2, P3, P4, P5 and P6 is less than 65mA

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ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇	$I_{OH}=-10mA$	3			V
V_{OH}	"H" output voltage ϕ	$I_{OH}=-2.5mA$	3			V
V_{OL}	"L" output voltage P3 ₀ ~P3 ₇	$I_{OL}=10mA$			2	V
V_{OL}	"L" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇	$I_{OL}=10mA$			2	V
V_{OL}	"L" output voltage ϕ	$I_{OL}=2.5mA$			2	V
$V_{+}-V_{-}$	Hysteresis X_{IN}		0.1		0.5	V
$V_{+}-V_{-}$	Hysteresis RESET			0.5	0.7	V
$V_{+}-V_{-}$	Hysteresis INT ₀ ~INT ₅ , CNTR ₀ , CNTR ₁ , T	Use as INT ₀ ~INT ₅ , CNTR ₀ , CNTR ₁ , T input	0.3		1.0	V
I_{IH}	"H" input current RESET, X_{IN}	$V_{IH}=5V$			5	μA
I_{IH}	"H" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇	$V_{IH}=5V$			5	μA
I_{IH}	"H" input current P3 ₀ ~P3 ₇	$V_{IH}=5V$			5	μA
I_{IL}	"L" input current RESET, X_{IN}	$V_{IL}=0V$	-5			μA
I_{IL}	"L" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇	$V_{IL}=0V$	-5			μA
I_{IL}	"L" input current P3 ₀ ~P3 ₇	$V_{IL}=0V$	-5			μA
I_{CC}	Supply current	$f(X_{IN})=4MHz$, output pins opened, input pins at V_{SS} or V_{CC} , and A-D converter in the finished condition		6	12	mA

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistor	$V_{REF}=V_{CC}$	20			k Ω
t_{CONV}	Conversion time				25	μs
V_{REF}	Reference voltage		4		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER 1, 2 CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 2	%
R_O	Ladder resistor	$V_{REF}=V_{CC}$			4	k Ω
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
V_{REF}	Reference voltage		4		V_{CC}	V

D-A CONVERTER 3, 4 CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			5	bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 2	%
R_O	Ladder resistor	$V_{REF}=V_{CC}$			4	k Ω
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
V_{REF}	Reference voltage		4		V_{CC}	V

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS} Output transistors are at "OFF" state	-0.3~7	V
V _{SS}	Supply voltage		0	V
V _{REF}	Reference voltage		-0.3~V _{CC} +0.3	V
V _I	Input voltage X _{IN} , RESET, CNV _{SS}		-0.3~7	V
V _I	Input voltage P ₁₀ ~P ₁₇ , P ₃₀ ~P ₃₇		-0.3~13	V
V _I	Input voltage P ₀₀ ~P ₀₇ , P ₂₀ ~P ₂₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇		-0.3~V _{CC} +0.3	V
V _O	Output voltage P ₁₀ ~P ₁₇ , P ₃₀ ~P ₃₇		-0.3~13	V
V _O	Output voltage P ₀₀ ~P ₀₇ , P ₂₀ ~P ₂₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ , X _{OUT} , φ		-0.3~V _{CC} +0.3	V
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=-10~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage		0		V
V _{IH}	"H" input voltage P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ , INT ₀ ~INT ₅ , CNTR ₀ , CNTR ₁ , T, RESET, X _{IN}	0.8V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ , INT ₀ ~INT ₅ , CNTR ₀ , CNTR ₁ , T	0		0.2V _{CC}	V
V _{IL}	"L" input voltage RESET	0		0.12V _{CC}	V
V _{IL}	"L" input voltage X _{IN}	0		0.16V _{CC}	V
I _{OH(peak)}	"H" peak output current P ₀₀ ~P ₀₇ , P ₂₀ ~P ₂₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 1)			-10	mA
I _{OH(avg)}	"H" average output current P ₀₀ ~P ₀₇ , P ₂₀ ~P ₂₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 1)			-5	mA
I _{OL(peak)}	"L" peak output current P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 2)			10	mA
I _{OL(avg)}	"L" average output current P ₀₀ ~P ₀₇ , P ₁₀ ~P ₁₇ , P ₂₀ ~P ₂₇ , P ₃₀ ~P ₃₇ , P ₄₀ ~P ₄₇ , P ₅₀ ~P ₅₇ , P ₆₀ ~P ₆₇ (Note 2)			5	mA
f(X _{IN})	Clock oscillating frequency			4	MHz

- Note 1. The total of "H" peak output current of port P0, P2, P4, P5 and P6 is less than 65mA.
 2. The total of "L" peak output current of port P0, P1, P2, P3, P4, P5 and P6 is less than 65mA

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇	$I_{OH}=-10mA$	3			V
V_{OH}	"H" output voltage ϕ	$I_{OH}=-2.5mA$	3			V
V_{OL}	"L" output voltage P1 ₀ ~P1 ₇ , P3 ₀ ~P3 ₇	$I_{OL}=10mA$			2	V
V_{OL}	"L" output voltage P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇	$I_{OL}=10mA$			2	V
V_{OL}	"L" output voltage ϕ	$I_{OL}=2.5mA$			2	V
$V_+ - V_-$	Hysteresis X_{IN}		0.1		0.5	V
$V_+ - V_-$	Hysteresis RESET			0.5	0.7	V
$V_+ - V_-$	Hysteresis INT ₀ ~INT ₅ , CNTR ₀ , CNTR ₁ , T	Use as INT ₀ ~INT ₅ , CNTR ₀ , CNTR ₁ , T input	0.3		1.0	V
I_{IH}	"H" input current RESET, X_{IN}	$V_{IH}=5V$			5	μA
I_{IH}	"H" input current P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇	$V_{IH}=5V$			5	μA
I_{IH}	"H" input current P1 ₀ ~P1 ₇ , P3 ₀ ~P3 ₇	$V_{IH}=12V$			12	μA
I_{IL}	"L" input current RESET, X_{IN}	$V_{IL}=0V$	-5			μA
I_{IL}	"L" input current P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇	$V_{IL}=0V$	-5			μA
I_{IL}	"L" input current P1 ₀ ~P1 ₇ , P3 ₀ ~P3 ₇	$V_{IL}=0V$	-5			μA
I_{CC}	Supply current	$f(X_{IN})=4MHz$, output pins opened, input pins at V_{SS} or V_{CC} , and A-D converter in the finished condition		6	12	mA

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistor	$V_{REF}=V_{CC}$	20			k Ω
t_{CONV}	Conversion time				25	μs
V_{REF}	Reference voltage		4		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

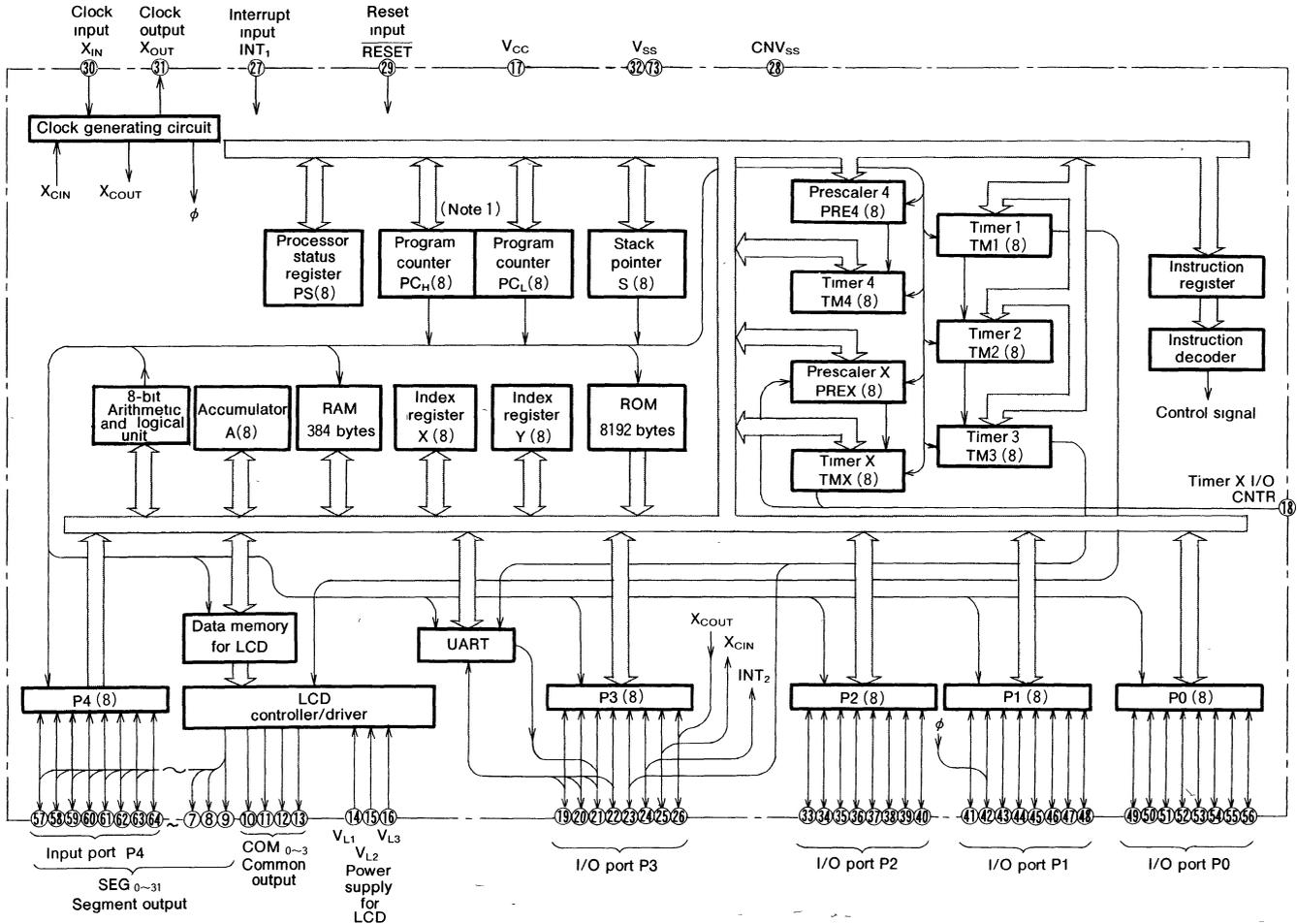
D-A CONVERTER 1, 2 CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 2	%
R_O	Ladder resistor	$V_{REF}=V_{CC}$			4	k Ω
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
V_{REF}	Reference voltage		4		V_{CC}	V

D-A CONVERTER 3, 4 CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			5	bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 2	%
R_O	Ladder resistor	$V_{REF}=V_{CC}$			4	k Ω
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
V_{REF}	Reference voltage		4		V_{CC}	V

M37428M4-XXXFP BLOCK DIAGRAM



Note 1 : Program counter PC_H uses only 6 bits



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

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M37428M4-XXXFP

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37428M4-XXXFP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		1 μ s (shortest instruction at 8MHz)
Clock frequency		8MHz
Memory size	ROM	8192 bytes
	RAM	384 bytes
Input/Output port	P0, P1, P2, P3	I/O
	P4	Input
	SEG	LCD output
	COM	LCD output
UART with baud rate generator		1 channel
Timers		8-bit timers with prescalers and reload latches \times 2 8-bit timers with reload latches \times 3
LCD controller/driver	Bias	1/2, 1/3, bias selectable
	Duty ratio	1/2, 1/3, 1/4 duty selectable
	Common output	4
	Segment output	32(SEG ₂₄ ~SEG ₃₁ are in common with port P4)
Subroutine nesting		96 (max.)
Interrupt		Three external interrupts, six internal interrupts, one software interrupt
Clock generating circuit		Two built-in circuits (ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 10% (at 8MHz) 2.8~5.5V (at 32kHz) RAM retention voltage at clock stop is 2~5.5V
Power dissipation	Normal operation mode V _{CC} =5V	30mW (typ at 8MHz)
	Low-speed operation mode V _{CC} =5V	225 μ W (typ at 32kHz)
	Stop mode V _{CC} =5V	5 μ W (max at 25 $^{\circ}$ C)
Operating temperature range		-10~70 $^{\circ}$ C
Process technology		High-speed silicon gate CMOS
Package		80-pin plastic molded QFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Function
V _{CC} , V _{SS}	Power supply		Connect V _{CC} to 5V±10%. Connect V _{SS} to 0V.
CNV _{SS}	CNV _{SS} input	Input	Connect to 0V to ensure proper operation in the single-chip mode
RESET	RESET input	Input	To reset the CPU, keep the RESET input terminal low for at least 2μsec under normal V _{CC} conditions
X _{IN}	Clock input	Input	Connect a ceramic or crystal oscillator between X _{IN} and X _{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X _{IN} pin and leave the X _{OUT} pin opened.
X _{OUT}	Clock output	Output	
INT ₁	Interrupt input	Input	This is the highest priority interrupt input pin (except for RESET).
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each bit to be individually programmed as input or output. At reset, this port is set as input. The I/O port structure is CMOS compatible.
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port with the same function as Port P0.
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port with the same function as Port P0. It can also be used as input pins for key-on wake up. The output is CMOS compatible.
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port with the same function as port P0. P3 ₄ , P3 ₅ , P3 ₆ and P3 ₇ can operate as R _X D, T _X D, CLK and CTS, respectively, for the UART function. P3 ₂ can be set to work as an external interrupt input pin INT ₂ . P3 ₁ and P3 ₀ can function as X _{CIN} and X _{COUT} , respectively, which are the input pins for the low-power dissipation mode clock.
P4 ₀ ~P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit input port which can operate as the LCD segment output pins SEG ₂₄ ~SEG ₃₁ .
V _{L1} ~V _{L3}	Supply voltage for LCD	Input	For LCD operation, these pins must be connected to power such that 0V ≤ V _{L1} ≤ V _{L2} ≤ V _{L3} ≤ V _{CC} .
COM ₀ ~ COM ₃	Common output	Output	These are LCD common output pins. At 1/2 duty, COM ₂ and COM ₃ are not used. At 1/3 duty, COM ₃ is not used.
SEG ₀ ~ SEG ₃₁	Segment output	Output	These are LCD segment output pins.
CNTR	Counter I/O	I/O	This pin is used together with timer X for event counter, pulse output or PWM mode.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37428 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:
 The FST and SLW instructions are not provided.
 The MUL and DIV instructions are not provided.
 The WIT instruction can be used.
 The STP instruction can be used.

MEMORY

- Special Function Register (SFR) Area
 The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.
- RAM
 RAM is used for data storage as well as a stack area.
- ROM
 ROM is used for storing user programs as well as the interrupt vector area.
- Interrupt Vector Area
 The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.
- Zero Page
 Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.
- Special Page
 Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

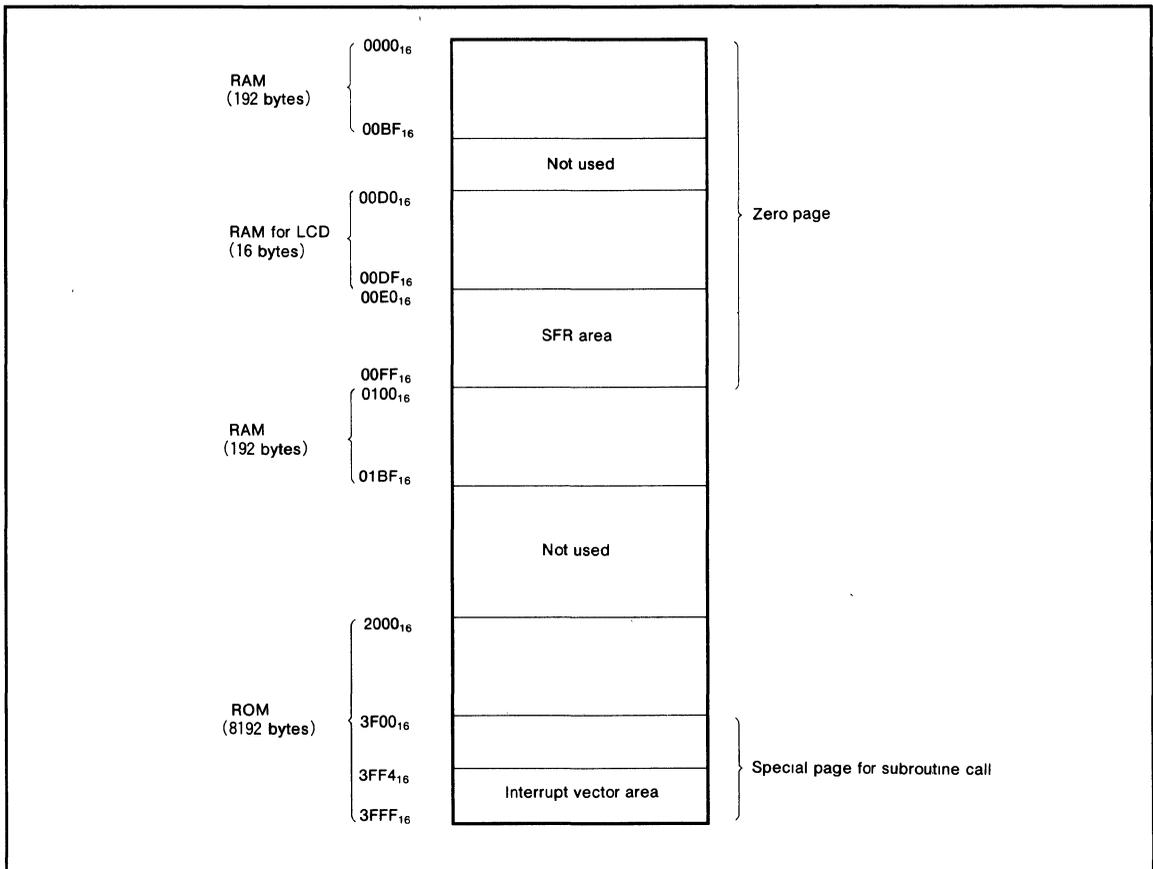


Fig. 1 Memory map

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

00E0 ₁₆	Port P0	00F0 ₁₆	Band rate generator
00E1 ₁₆	Port P0 direction register	00F1 ₁₆	Receive buffer register
00E2 ₁₆	Port P1	00F2 ₁₆	Transmit buffer register
00E3 ₁₆	Port P1 direction register	00F3 ₁₆	UART status register
00E4 ₁₆	Port P2	00F4 ₁₆	UART mode register
00E5 ₁₆	Port P2 direction register	00F5 ₁₆	UART control register
00E6 ₁₆	Port P3	00F6 ₁₆	Timer control register 1
00E7 ₁₆	Port P3 direction register	00F7 ₁₆	Timer 1
00E8 ₁₆	Port P4	00F8 ₁₆	Timer 2
00E9 ₁₆		00F9 ₁₆	Timer 3
00EA ₁₆	Interrupt source recognition register 1	00FA ₁₆	Prescaler 4
00EB ₁₆	Interrupt source recognition register 2	00FB ₁₆	Time. 4
00EC ₁₆	System control register	00FC ₁₆	Prescaler X
00ED ₁₆		00FD ₁₆	Timer X
00EE ₁₆		00FE ₁₆	Interrupt control register
00EF ₁₆	LCD mode register	00FF ₁₆	Timer control register 2

Fig. 2 SFR (Special Function Register) memory map.

M37409PSS

PIGGYBACK for M37409M2-XXXSP

DESCRIPTION

The M37409PSS is an EPROM mounted-type microcomputer which utilizes CMOS technology, and is designed for developing programs for single-chip 8-bit microcomputers the M37409M2-XXXSP. It is housed in a piggyback-type 52-pin shrink DIP.

There is a 28-pin socket on the package for the M5L2764K or the M5L27128K EPROM.

The M37409PSS simplifies the development of programs for the M37409M2-XXXSP, and is excellent for making prototypes.

Therefore the M37409PSS can be used for the development of programs for the M37409M2-XXXSP.

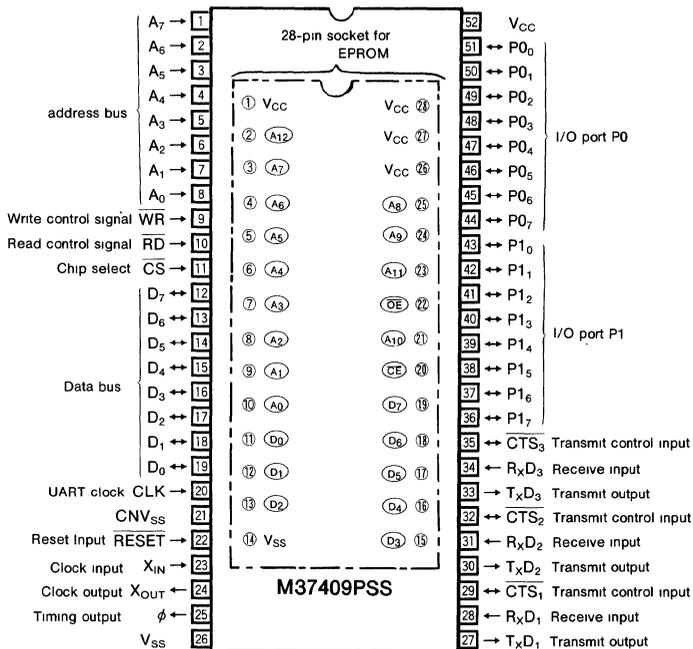
FEATURES

- Differences with the M37409M2-XXXSP are:
 - (1) ROMless, EPROM is attached externally.
 - (2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

- Development of programs for the following systems;
 - Office automation equipment

PIN CONFIGURATION (TOP VIEW)



Outline 52S1M

The symbol "○" indicates sockets for EPROM

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±5% to V _{CC} , and 0V to V _{SS} .
CNV _{SS}	CNV _{SS}		This is usually connected to V _{SS}
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions.) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output. This port is connected to the system bus only, and can not be accessed from the local bus. At reset this port becomes input mode. The output structure is CMOS output.
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0. This port is connected to the local bus and can be used as only input port from the system bus. The output structure is CMOS output.
TxD ₁ ~ TxD ₃	UART transfer output	Output	These are UART transfer data output pins
RxD ₁ ~ RxD ₃	UART receive input	Input	These are UART receive data input pins
CTS ₁ ~ CTS ₃	UART transfer control input	I/O	These are UART transfer control signal input pins and can be used as I/O port which have basically same function as port P1
CLK	UART clock input	Input	This port is an external clock input pin for baud rate
A ₀ ~A ₇	Address input	Input	This port is input for system address
D ₀ ~D ₇	Data input/output	I/O	This port is input or output the system data
CS	Chip select	Input	System data can be read or written by inputting "L" to this port
RD	Read control input	Input	Memory or register data specified by A ₀ ~A ₇ is read from D ₀ ~D ₇ by inputting "L" to this port
WR	Write control input	Input	Data input from D ₀ ~D ₇ is written to memory or register specified by A ₀ ~A ₇ by inputting "L" to this port
(A ₀)~(A ₁₂)	Output port A	Output	These are for addresses to an EPROM mounted on the package.
(D ₀)~(D ₇)	Input port D	Input	These are for input data from an EPROM mounted on the package

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37409PSS and the M37409M2-XXXSP are noted below. The following explanations apply to the M37409PSS. Specification variations for other chips are noted accordingly.

MEMORY

The M37409PSS is mounted an EPROM instead of an external ROM.

The address of an EPROM is $0800_{16} \sim 1FFF_{16}$, and this memory size is 6144 bytes. Other than these, the M37409PSS has the same function as the M37409M2-XXXSP.

PRECATION FOR USE

(1) In case of the M5L2764K EPROM use the following areas (refer to Figure 1).

- For use the M37409M2-XXXSP, usable ROM area is $1000_{16} \sim 1FFF_{16}$.

M5L2764K..... addresses $1000_{16} \sim 1FFF_{16}$

M5L27128K..... addresses $3000_{16} \sim 3FFF_{16}$

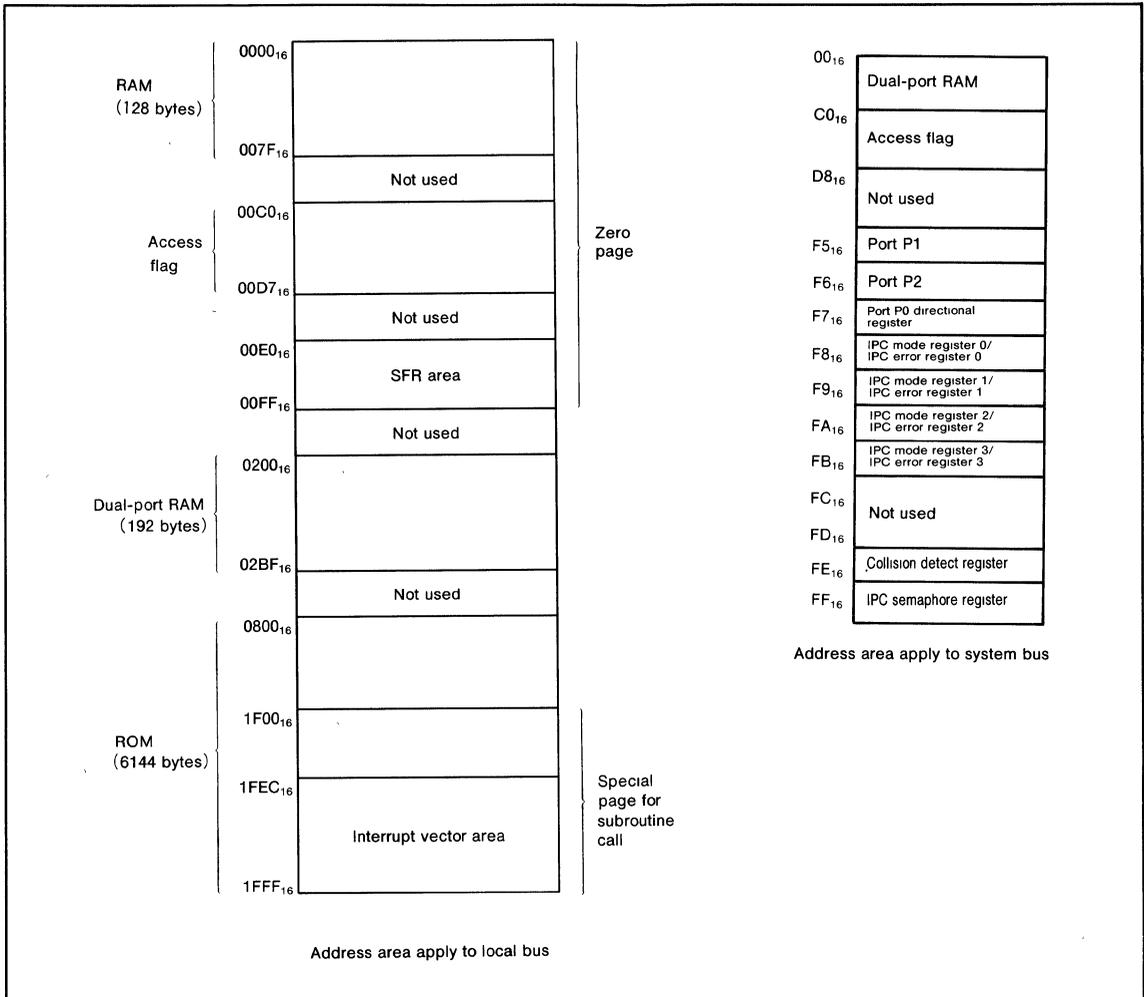


Fig.1 Memory map

00E0 ₁₆	Port P1	00F0 ₁₆	IPC mode register 0
00E1 ₁₆	Port P1 directional register	00F1 ₁₆	IPC mode register 1
00E2 ₁₆	Dual-port RAM direction specify register	00F2 ₁₆	IPC mode register 2
00E3 ₁₆		00F3 ₁₆	IPC mode register 3
00E4 ₁₆	UART1 receive/transfer buffer register	00F4 ₁₆	IPC error register 0
00E5 ₁₆	UART1 status register/UART1 mode register	00F5 ₁₆	IPC error register 1
00E6 ₁₆	UART1 control register	00F6 ₁₆	IPC error register 2
00E7 ₁₆	UART1 divider for baud rate generate	00F7 ₁₆	IPC error register 3
00E8 ₁₆	UART2 receive/transfer buffer register	00F8 ₁₆	
00E9 ₁₆	UART2 status register/UART2 mode register	00F9 ₁₆	IPC semaphore register
00EA ₁₆	UART2 control register	00FA ₁₆	Collision detect register
00EB ₁₆	UART2 divider for baud rate generate	00FB ₁₆	Interrupt enable register
00EC ₁₆	UART3 receive/transfer buffer register	00FC ₁₆	Interrupt request register
00ED ₁₆	UART3 status register/UART3 mode register	00FD ₁₆	Prescaler X
00EE ₁₆	UART3 control register	00FE ₁₆	Timer X
00EF ₁₆	UART3 divider for baud rate generate	00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS} Output transistors cut-off	-0.3~7	V
V _I	Input voltage X _{IN} , RESET, (D ₀ ~D ₇)		-0.3~7	V
V _I	Input voltage P ₀ ~P ₀ 7, P ₁ 0~P ₁ 7, D ₀ ~D ₇ , A ₀ ~A ₇ , RD, WR, CS, CLK, R _X D ₁ ~R _X D ₃ , CTS ₁ ~CTS ₃		-0.3~V _{CC} +0.3	V
V _I	Input voltage CNV _{SS}		-0.3~13	V
V _O	Output voltage P ₀ ~P ₀ 7, P ₁ 0~P ₁ 7, X _{OUT} , φ, D ₀ ~D ₇ , T _X D ₁ ~T _X D ₃ , CTS ₁ ~CTS ₃ , (A ₀ ~A ₁₃)		-0.3~V _{CC} +0.3	V
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=-10~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max	
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{SS}	Supply voltage		0		V
V _{IH}	"H" input voltage X _{IN} , RESET, CLK, P ₀ ~P ₀ 7, P ₁ 0~P ₁ 7, R _X D ₁ ~R _X D ₃ , CTS ₁ ~CTS ₃	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage A ₀ ~A ₇ , D ₀ ~D ₇ , RD, WR, CS	2		V _{CC} +0.3	V
V _{IH}	"H" input voltage (D ₀ ~D ₇)	0.45V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀ ~P ₀ 7, P ₁ 0~P ₁ 7, CLK, R _X D ₁ ~R _X D ₃ , CTS ₁ ~CTS ₃	-0.3		0.2V _{CC}	V
V _{IL}	"L" input voltage A ₀ ~A ₇ , D ₀ ~D ₇ , RD, WR, CS	-0.3		0.8	V
V _{IL}	"L" input voltage RESET	-0.3		0.12V _{CC}	V
V _{IL}	"L" input voltage X _{IN}	-0.3		0.16V _{CC}	V
V _{IL}	"L" output voltage (D ₀ ~D ₇)	0		0.15V _{CC}	V
I _{OH}	"H" output current P ₀ ~P ₀ 7, P ₁ 0~P ₁ 7, φ, T _X D ₁ ~T _X D ₃ , CTS ₁ ~CTS ₃			-10	mA
I _{OH}	"H" output current D ₀ ~D ₇			-1.0	mA
I _{OL}	"L" output current P ₀ ~P ₀ 7, P ₁ 0~P ₁ 7, φ, T _X D ₁ ~T _X D ₃ , CTS ₁ ~CTS ₃			10	mA
I _{OL}	"L" output current D ₀ ~D ₇			-1.6	mA

Note 1 : Average output current I_{OL}(avg) and I_{OH}(avg) are the average value of a period of 100ms
 2 : Total of "L" output current I_{OL} of ports P₀, P₁, T_XD₁~T_XD₃ and CTS₁~CTS₃ is -50mA max
 Total of "H" output current I_{OH} of port P₀, P₁, T_XD₁~T_XD₃ and CTS₁~CTS₃ is 50mA max

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25°C, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	"H" output voltage P ₀ ~P ₀ 7, P ₁ 0~P ₁ 7, φ, T _X D ₁ ~T _X D ₃ , CTS ₁ ~CTS ₃	I _{OH} =-10mA	V _{CC} -2			V
V _{OH}	"H" output voltage D ₀ ~D ₇	I _{OH} =-1mA	2.4			V
V _{OL}	"L" output voltage P ₀ ~P ₀ 7, P ₁ 0~P ₁ 7, φ, T _X D ₁ ~T _X D ₃ , CTS ₁ ~CTS ₃	I _{OL} =10mA			2	V
V _{OL}	"L" output voltage D ₀ ~D ₇	I _{OL} =1.6mA			0.4	V
I _I	Input leak current A ₀ ~A ₇ , RD, WR, CS, CLK	V _{SS} ≤V _I ≤V _{CC}	-5		5	μA
I _I	Input leak current RESET, X _{IN}	V _{SS} ≤V _I ≤7V	-5		5	μA
I _{oz}	Tri-state leak current P ₀ ~P ₀ 7, P ₁ 0~P ₁ 7, D ₀ ~D ₇ , CTS ₁ ~CTS ₃	V _{SS} +0.5≤V _O ≤V _{CC} -0.5V	-5		5	μA
V _{T+} -V _{T-}	Hysteresis RESET, CLK, R _X D ₁ ~R _X D ₃ , CTS ₁ ~CTS ₃			0.6		V

M37415PFS

PIGGYBACK for M37415M4-XXXFP

DESCRIPTION

The M37415PFS is an EPROM mounted-type microcomputer which utilizes CMOS technology, and is designed for developing programs for single-chip, 8-bit microcomputer M37415M4-XXXFP. It is housed in a piggyback-type 80-pin QFP.

There is a 32-pin socket on the package.

The M37415PFS simplifies the development of programs for the M37415M4-XXXFP and is excellent for making prototypes.

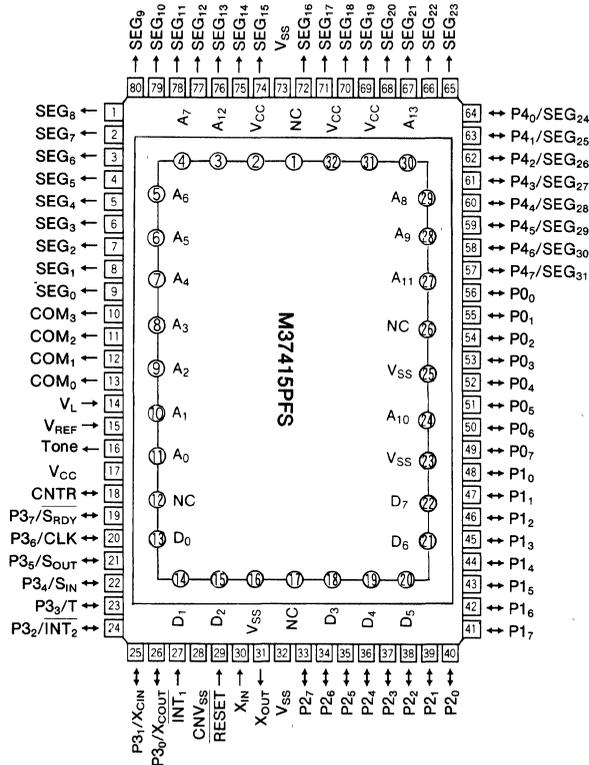
FEATURES

- Difference with the M37415M4-XXXFP are:
ROMless, EPROM is attached externally.

APPLICATION

Development of programs for home telephone, multi function telephone

PIN CONFIGURATION (TOP VIEW)



Outline 80S6M

The symbol "○" indicates sockets for EPROM
NC No connection.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage input		Power supply inputs 5V±10% to V _{CC} and 0V to V _{SS} .
CNV _{SS}	CNV _{SS} input		Connect to V _{SS}
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2 μ s (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
$\overline{\text{INT}}_1$	Interrupt input	Input	This is the highest order interrupt input pin. It can be measured input voltage level
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as S _{RDY} , CLK, S _{OUT} , and S _{IN} pins, respectively Also P3 ₃ , P3 ₂ , P3 ₁ , and P3 ₀ work as timer 3 overflow signal divided by 2 output pin (T), INT ₂ pin, X _{CIN} and X _{COU} T pins, respectively
P4 ₀ ~P4 ₇	Input port P4	Input	Port P4 is an 8-bit input port and can be used as segment output pins
V _L	Voltage input for LCD	Input	This is a voltage input pin for LCD Supply voltage is 0V≤V _L ≤V _{CC} 0V~V _{LV} is supplied to LCD.
COM ₀ ~ COM ₃	Common output	Output	These are the LCD common output pins At 1/2 duty, COM ₂ and COM ₃ pins are not use At 1/3 duty, COM ₃ pin is not used
SEG ₀ ~ SEG ₂₃	Segment output	Output	These are LCD segment output pins
CNTR	Counter I/O	I/O	This is an output pin for timer 4 and 5 It can be measured input voltage level
V _{REF}	D-A convert power supply for DTMF		Reference voltage input for A-D converter of DTMF
Tone	DTMF output	Output	This is DTMF output pin.
A ₀ ~A ₁₃	Output port A	Output	These are for addresses to an EPROM mounted on the package
D ₀ ~D ₇	Input port D	Input	These are for input data from the EPROM mounted on the package

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37415PFS and the M37415M4-XXXFP are noted below. The following explanations apply to the M37415PFS. Specification variations for other chips are noted accordingly.

MEMORY

The M37415PFS is mounted an EPROM instead of an internal ROM. The address of an EPROM is from 1000_{16} to $3FFF_{16}$, and this memory size is 12288 bytes. The memory size of a RAM is 512 bytes as same as the M37415M4-XXXFP.

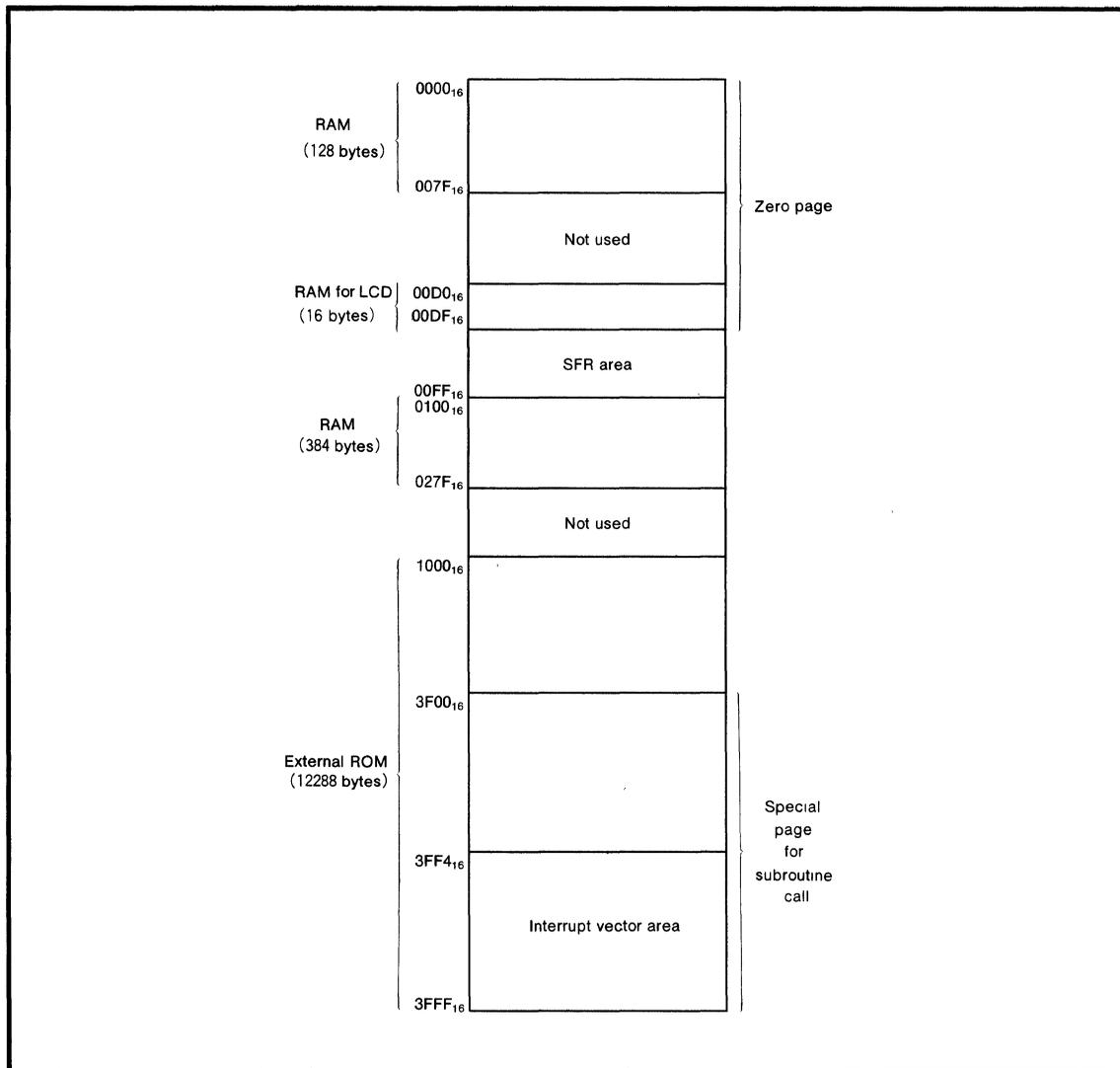


Fig.1 Memory map

00E0 ₁₆	Port P0	00F0 ₁₆	
00E1 ₁₆	Port P0 directional register	00F1 ₁₆	
00E2 ₁₆	Port P1	00F2 ₁₆	
00E3 ₁₆	Port P1 directional register	00F3 ₁₆	
00E4 ₁₆	Port P2	00F4 ₁₆	DTMF register
00E5 ₁₆	Port P2 directional register	00F5 ₁₆	LCD mode register
00E6 ₁₆		00F6 ₁₆	Serial I/O mode register
00E7 ₁₆		00F7 ₁₆	Serial I/O register
00E8 ₁₆	Port P3	00F8 ₁₆	Timer 4, 5 mode register
00E9 ₁₆	Port P3 directional register	00F9 ₁₆	Timer 1
00EA ₁₆	Port P4	00FA ₁₆	Timer 2
00EB ₁₆		00FB ₁₆	Timer 3
00EC ₁₆		00FC ₁₆	Timer 4
00ED ₁₆		00FD ₁₆	Timer 5
00EE ₁₆		00FE ₁₆	Interrupt control register
00EF ₁₆		00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

PIGGYBACK for M37415M4-XXXFP

PRECAUTION FOR USE

- (1) When developing programs with the M37415PFS, carefully consider the ROM capacity of the M37415M4-XXXFP.
Use the ROM area from 2000₁₆ to 3FFF₁₆.

- (2) The M37415PFS has no options as the M37415M4-XXXFP. The condition of ports P0~P3 and CNTR is noted below.
P0~P3, CNTR without the pull-up transistor
P3_S/S_{OUT} N-channel open drain output
- (3) The way of mounting an EPROM is shown in Figure 3.

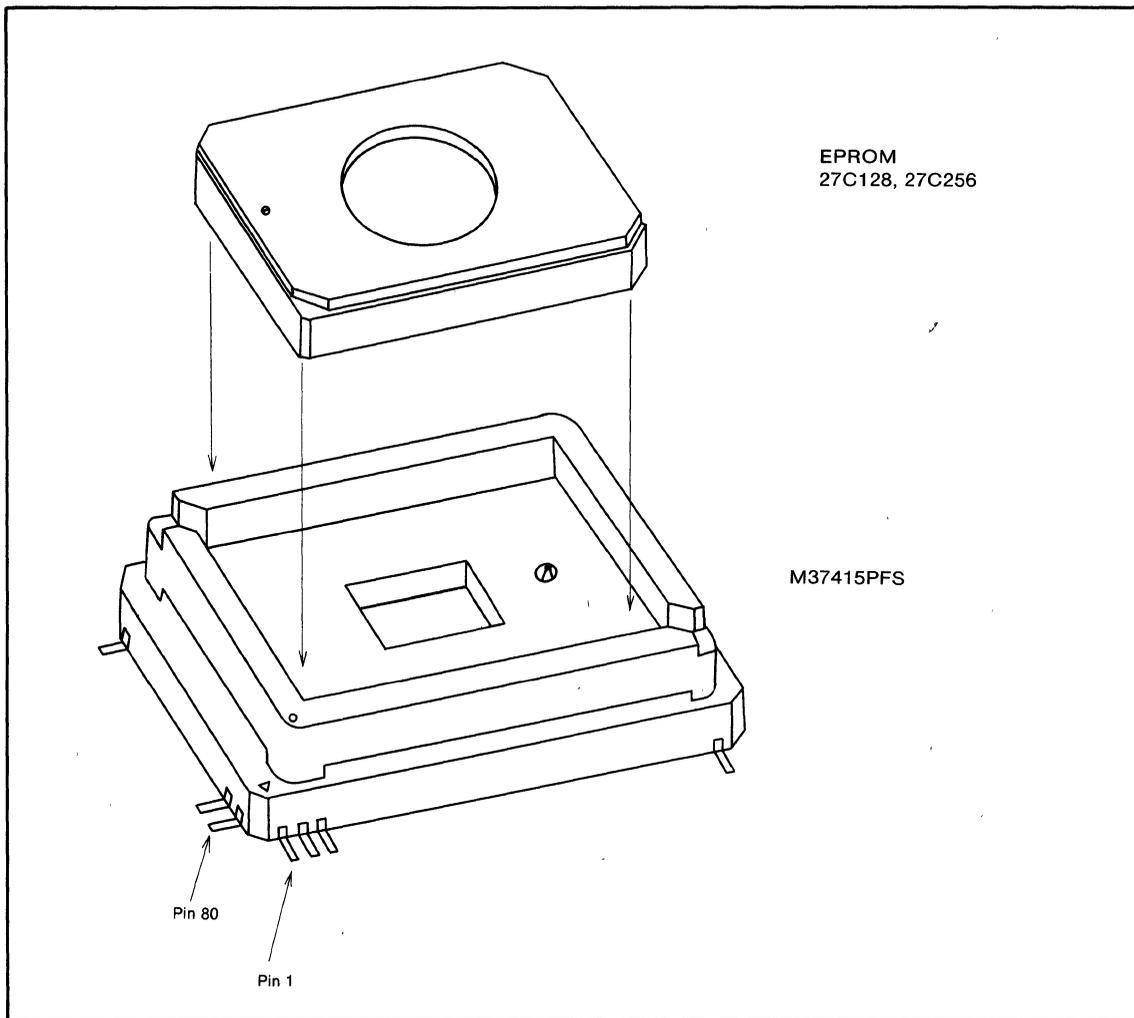


Fig.3 How to mount an EPROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	-0.3~7	V
V_I	Supply voltage for LCD V_L		-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, SEG_{24}\sim SEG_{31}, X_{IN}$		-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage INT_1, CNV_{SS}, V_{REF}		-0.3~7	V
V_I	Input voltage $RESET, CNTR$		-0.3~13	V
V_O	Output voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, COM_0\sim COM_3, SEG_0\sim SEG_{31},$ X_{OUT}		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage $CNTR$		-0.3~7	V
P_d	Power Dissipation		$T_a = 25^\circ C$	300
T_{opr}	Operating temperature		-10~70	$^\circ C$
T_{stg}	Storage temperature		-40~125	$^\circ C$

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=3.0$ (Note 1)~5.5V, $V_{SS}=0$ V, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage (Note 2)	$f(X_{IN})=3.2$ MHz $f(X_{IN})=800$ kHz	4.5 3.0(Note 1)		5.5 5.5	V
V_{SS}	Supply voltage			0		V
V_{REF}	Supply voltage for DTMF	$R_L \geq 20$ k Ω	1.5		$V_{CC}-0.5$	V
V_{IH}	"H" input voltage $P0_0\sim P0_7, P1_0\sim P1_7,$ $P3_0, P3_1$ (Note 3), $P3_3\sim P3_7$ (Note 4), $P4_0\sim P4_7,$ $RESET, X_{IN}, CNV_{SS}$		0.7 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0\sim P2_7, P3_2, P3_5$ (Note 5) $INT_1, CNTR$		0.8 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0\sim P0_7, P1_0\sim P1_7,$ $P3_0, P3_1$ (Note 3), $P3_3\sim P3_7$ (Note 4), $P4_0\sim P4_7,$ CNV_{SS}		0		0.3 V_{CC}	V
V_{IL}	"L" input voltage $P2_0\sim P2_7, P3_2, P3_5$ (Note 5), $INT_1, CNTR$		0		0.2 V_{CC}	V
V_{IL}	"L" input voltage $RESET$		0		0.12 V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16 V_{CC}	V
I_{OH}	"H" Output current $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7$ (Note 6), X_{OUT}				-2	mA
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, CNTR, X_{OUT}$ (Note 7)				10	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7, P1_0\sim P1_7,$ $P2_0\sim P2_7, P3_0\sim P3_7,$ $CNTR, X_{OUT}$ (Note 8)				5	mA
$f(X_{IN})$	Clock oscillating frequency (Note 9)	$V_{CC}=4.5\sim 5.5$ V $V_{CC}=3.0$ (Note 1)~5.5V	380 380		3300 1000	kHz
$f(X_{CIN})$	Clock oscillating frequency for clock function		32		50	kHz

Note 1 : Minimum value of V_{CC} is dependent on the EPROM used. At normal temperature, this value is about 2.5V. Therefore, 3.0V is dependent on the proper operation of the EPROM at that voltage

2 : When only operating the RAM data retention, minimum value of V_{CC} is 2 V

3 : When using port $P3_1$ as X_{CIN} , $0.85 \leq V_{CC} \leq V_{IH} \leq V_{CC}$, $0 \leq V_{IL} \leq 0.15V_{CC}$ for port $P3_1$

4 : In this case of using port $P3_5$ as normal input

5 : In this case of using port $P3_5$ as CLK input

6 : The total of I_{OH} of port $P0, P1, P2, P3$ and X_{OUT} should be 35mA max

7 : The total of $I_{OL(peak)}$ of port $P0, P1, P2, P3$ should be 55mA max, and the total of $I_{OL(peak)}$ of port $P3, CNTR,$ and X_{OUT} should be 45mA max

8 : $I_{OL(avg)}$ is the average current in 100ms

9 : When using DTMF function, $f(X_{IN})$ should be 400kHz, 800kHz, 1.6MHz, or 3.2MHz

ELECTRICAL CHARACTERICS ($V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V_{OH}	"H" output voltage $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$ (Note 1), P_{36} , P_{37}	$V_{CC}=5V$, $I_{OH}=-2mA$	3			V	
		$V_{CC}=3V$, $I_{OH}=-0.7mA$	2				
V_{OH}	"H" output voltage X_{OUT}	$V_{CC}=5V$, $I_{OH}=-1.5mA$ $V_{CC}=3V$, $I_{OH}=-0.3mA$	3 2			V	
V_{OL}	"L" output voltage $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$ (Note 1), CNTR	$V_{CC}=5V$, $I_{OL}=10mA$			2	V	
		$V_{CC}=3V$, $I_{OL}=3mA$			1		
V_{OL}	"L" output voltage X_{OUT}	$V_{CC}=5V$, $I_{OL}=1.5mA$ $V_{CC}=3V$, $I_{OL}=0.3mA$			2 1	V	
					1		
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$, CNTR	$V_{CC}=5V$ $V_{CC}=3V$	0.25 0.15		1 0.7	V	
$V_{T+}-V_{T-}$	Hysteresis P_{36}	When used as CLK input $V_{CC}=5V$ $V_{CC}=3V$		0.5 0.4		V	
$V_{T+}-V_{T-}$	Hysteresis P_{31}	When used as X_{CIN} input $V_{CC}=5V$ $V_{CC}=3V$		0.7 0.5		V	
$V_{T+}-V_{T-}$	Hysteresis $P_{20}\sim P_{27}$, P_{32}	$V_{CC}=5V$ $V_{CC}=3V$		0.5 0.4		V	
$V_{T+}-V_{T-}$	Hysteresis \overline{RESET}	$V_{CC}=5V$ $V_{CC}=3V$		0.5 0.35	0.7	V	
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	$V_{CC}=5V$ $V_{CC}=3V$		0.5 0.35		V	
I_{IL}	"L" input current $SEG_{24}\sim SEG_{31}$ (except reset state) $(P_{00}\sim P_{07}, P_{10}\sim P_{17}, P_{20}\sim P_{27}, P_{30}\sim P_{37})$ without pull-up Tr $\overline{INT_1}$, \overline{RESET} , X_{IN}	$V_{CC}=5V$ $V_1=0V$ $V_{CC}=3V$ $V_1=0V$			-5 -4	μA	
I_{IL}	"L" input current $SEG_{24}\sim SEG_{31}$ (at reset state)	$V_{CC}=5V$, $V_L=5V$, $V_1=0V$ $V_{CC}=3V$, $V_L=3V$, $V_1=0V$	-30 -6		-140 -45	μA	
I_{IH}	"H" input current $SEG_{24}\sim SEG_{31}$ (except reset state) $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$, $\overline{INT_1}$, \overline{RESET} , X_{IN}	$V_{CC}=5V$ $V_1=5V$ $V_{CC}=3V$ $V_1=3V$			5 4	μA	
I_{IH}	"H" input current $SEG_{24}\sim SEG_{31}$ (at reset state)	$V_{CC}=5V$, $V_L=5V$, $V_1=5V$ $V_{CC}=3V$, $V_L=3V$, $V_1=3V$			5 4	μA	
I_{CC}	Supply current	Output pins are opened. \overline{RESET} , $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, and $P_{30}\sim P_{37}$ are connected to V_{CC} . Except the above pins are connected to V_{SS} . However, X_{IN} and X_{CIN} are input signal according to the conditions Without supply current for EPROM	at stop state	$f(X_{IN})=3.2MHz$ $V_{CC}=5V$	at DTMF wave form output	4	mA
					at DTMF wave form stop	3	
				$f(X_{IN})=800kHz$ $V_{CC}=3V$	at DTMF wave form output	0.8	
					at DTMF wave form stop	0.5	
			at wait state	$T_a=25^\circ C$ $X_{IN}=0V$ $f(X_{CIN})=32.8kHz$ at low power mode ($LM_6=1$)	$V_{CC}=5V$ $V_{CC}=3V$	45 18	μA
				$f(X_{IN})=3.2MHz$, $V_{CC}=5V$ $f(X_{IN})=800kHz$, $V_{CC}=3V$		1 0.3	mA
				at operation	$f(X_{IN})=0$ $f(X_{CIN})=0$ $V_{CC}=5V$	$T_a=25^\circ C$ $T_a=70^\circ C$	0.1

Note 1 : If P_{30} is used as X_{COUT} , capability of load driving is lower than the above

PIGGYBACK for M37415M4-XXXFP

DTMF CHARACTERISTICS ($V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter		Tes conditions	Limits			Units
				Min	Typ	Max	
V_{OT}	Output voltage T_{one}	High frequency band group	$V_{CC}=5V$, $V_{REF}=4.5V$, $R_L=20k\Omega$	470	490	510	mVrms
			$V_{CC}=3V$, $V_{REF}=2.5V$, $R_L=20k\Omega$	257	270	283	
		Low frequency band group	$V_{CC}=5V$, $V_{REF}=4.5V$, $R_L=20k\Omega$	325	345	365	
			$V_{CC}=3V$, $V_{REF}=2.5V$, $R_L=20k\Omega$	177	190	203	
dB_{CR}	Output ratio of high frequency band to low frequency band		$R_L=20k\Omega$	2.5	3	3.5	dB
DIS	Disportional percentage		$R_L=20k\Omega$, $T_a=25^\circ C$		13		%

Accuracy of DTMF output (at low frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
697	694.44	-2.555	-0.367
770	769.23	-0.769	-0.1
852	854.7	2.7	0.317
941	938.97	-2.033	-0.216

Accuracy of DTMF output (at high frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
1209	1204.8	-4.181	-0.346
1336	1333.3	-2.667	-0.2
1477	1470.6	-6.412	-0.434
1633	1639.3	6.344	0.389

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±5% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	CNV _{SS}		This is usually connected to V _{SS}
V _P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1, P4, P5 ₀ and P5 ₁
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin φ=2MHz (when X _{IN} =4MHz)
X _{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{CIN} and X _{COU} T pins If an external clock is used, the clock source should be connected to the X _{CIN} pin, and the X _{COU} T pin should be left open This clock can be used as a program controlled the system clock
X _{COU} T	Clock output for clock function	Output	
P0 ₀ ~P0 ₇	Output port P0	Output	Port P0 is an 8-bit output port Output structure is high-voltage P-channel open drain A pull-down transistor is built in between the V _P pin and this port At reset, this port is set to a "L" level
P1 ₀ ~P1 ₇	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode. The output structure is N-channel open drain
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P2 When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as $\overline{\text{SRDY}}$, CLK, S _{OUT} , and S _{IN} pins, respectively
P4 ₀ ~P4 ₇	Output port P4	Output	Port P4 is an 8-bit output port and has basically the same functions as port P0
P5 ₀ , P5 ₁	Output port P5	Output	Bit 0 and 1 of port P5 are 2-bit output port and has basically the same functions as port P0
P5 ₂ /INT ₂ , P5 ₃ /INT ₁	Input port P5	Input	Bit 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs
P5 ₄ ~P5 ₇		Input	Bit 4~7 of port P5 are 4-bit input port
P6 ₀ ~P6 ₅	I/O port P6	I/O	Port P6 is a 6-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS tri-state output P6 ₀ , P6 ₁ , P6 ₂ , P6 ₃ can be programmed to function as timer output pin (T), PWM output pins (PWM1, PWM2, and PWM3), respectively
A ₀ ~A ₁₄	Output port A	Output	These are for addresses to an EPROM mounted on the package
D ₀ ~D ₇	Input port D	Input	These are for input data from an EPROM mounted on the package

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37421P-000SS, the M37421P-001SS and the M37421M6-XXXSP are noted below. The following explanations apply to the M37421P-000SS and the M37421P-001SS.

Specification variations for other chips are noted accordingly.

MEMORY

The M37421P-000SS and the M37421P-001SS are mounted an EPROM instead of an internal ROM.

RAM size is 512 bytes, and addresses 0100₁₆ to 023F₁₆ are used for the stack.

The address of an EPROM is 8000₁₆ ~ FFFF₁₆, and this memory size is 32K bytes. Other than these, the M37421P-000SS and the M37421P-001SS have the same functions as the M37421M6-XXXSP has.

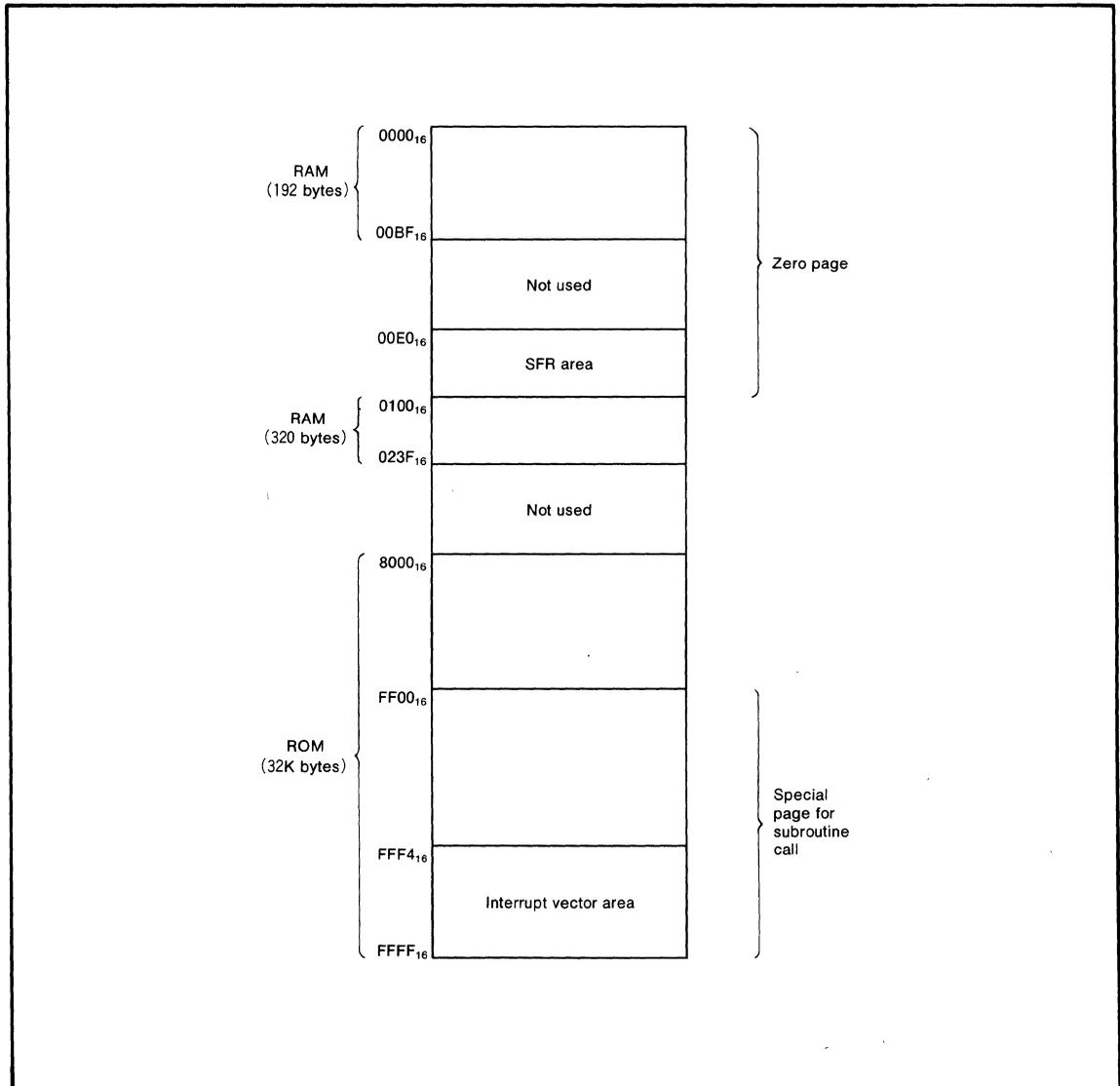


Fig.1 Memory map

00E0 ₁₆	Port P0	00F0 ₁₆	PWM1-H register
00E1 ₁₆		00F1 ₁₆	PWM1-L register
00E2 ₁₆	Port P1	00F2 ₁₆	PWM2 register
00E3 ₁₆		00F3 ₁₆	PWM3 register
00E4 ₁₆	Port P2	00F4 ₁₆	
00E5 ₁₆	Port P2 directional register	00F5 ₁₆	PWM output mode register
00E6 ₁₆		00F6 ₁₆	Serial I/O mode register
00E7 ₁₆		00F7 ₁₆	Serial I/O register
00E8 ₁₆	Port P3	00F8 ₁₆	
00E9 ₁₆	Port P3 directional register	00F9 ₁₆	Serial I/O register 2
00EA ₁₆	Port P4	00FA ₁₆	Timer 1
00EB ₁₆		00FB ₁₆	
00EC ₁₆	Port P5	00FC ₁₆	Timer 2
00ED ₁₆		00FD ₁₆	Timer 3
00EE ₁₆	Port P6	00FE ₁₆	Interrupt control register
00EF ₁₆	Port P6 directional register	00FF ₁₆	Timer control register

Fig. 2 SFR (Special Function Register) memory map

RESET MODE

With the M37421M6-XXXSP, one of the two modes can be selected: the normal operation start mode which executes reset by normal operation ($f(X_{IN}) = 4.2\text{MHz}$) and the low-speed operation start mode which executes reset by low-speed operation ($f(X_{CIN}) = 3.2\text{kHz}$).

Therefore, two types of piggybacks are provided:

(1) M37421P-000SS

With this piggyback, pin ϕ is set to the internal reset signal output and the reset mode option to the normal operation start mode.

(2) M37421P-001SS

With this piggyback, pin ϕ is set to the internal reset signal output and the reset mode option to the low-speed operation start mode.

PRECAUTION FOR USE

(1) In case of the M5L27128K or the M5L27256K EPROM use the following areas (refer to Figure 1):

- For the M37421M6-XXXSP, usable ROM area are
D000₁₆ ~ FFFF₁₆.

M5L27128K addresses 1000₁₆ ~ 3FFF₁₆

M5L27256K addresses 5000₁₆ ~ 7FFF₁₆

(2) In case of the development of programs by the M37421P-000SS or M37421P-001SS, RAM area for the stack:

M37421M6-XXXSP addresses 0100₁₆ ~ 017F₁₆

M37421P-000SS or

M37421P-001SS addresses 0100₁₆ ~ 023F₁₆

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS} Output transistors cut-off	-0.3~7	V
V _P	Pulldown input voltage		V _{CC} -40~V _{CC} +0.3	V
V _I	Input voltage, P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P3 ₄ ~P3 ₇ , CNV _{SS} , P5 ₂ /INT ₂ , P5 ₃ /INT ₁		-0.3~13	V
V _I	Input voltage, RESET, X _{IN} , X _{CIN}		-0.3~7	V
V _I	Input voltage, P3 ₃ , P6 ₀ ~P6 ₅		-0.3~V _{CC} +0.3	V
V _I	Input voltage, P5 ₄ ~P5 ₇		-0.3~13	V
V _O	Output voltage, P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P3 ₄ ~P3 ₇		-0.3~13	V
V _O	Output voltage, P6 ₀ ~P6 ₅ , X _{OUT} , X _{COUT} , φ, P3 ₃		-0.3~V _{CC} +0.3	V
V _O	Output voltage, P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁		V _{CC} -40~V _{CC} +0.3	V
P _d	Power dissipation		T _a = 25°C	1000
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=-10~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.75	5	5.25	V
V _P	Pull-down supply voltage	V _{CC} -38		V _{CC}	V
V _{SS}	Supply voltage		0		V
V _{IH}	"H" input voltage P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , CNV _{SS} (Note 1) P5 ₂ /INT ₂ , P5 ₃ /INT ₁ , P6 ₀ ~P6 ₅	0.75V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage RESET, X _{IN} , X _{CIN}	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P5 ₄ ~P5 ₇	0.4V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , CNV _{SS} , P5 ₂ /INT ₂ , P5 ₃ /INT ₁ , P6 ₀ ~P6 ₅	0		0.25V _{CC}	V
V _{IL}	"L" input voltage RESET	0		0.12V _{CC}	V
V _{IL}	"L" input voltage X _{IN} , X _{CIN}	0		0.16V _{CC}	V
V _{IL}	"L" input voltage P5 ₄ ~P5 ₇	0		0.12V _{CC}	V
I _{OH} (sum)	"H" sum output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁			-120	mA
I _{OH} (sum)	"H" sum output current P6 ₀ ~P6 ₅			-5	mA
I _{OL} (sum)	"L" sum output current P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P6 ₀ ~P6 ₅			50	mA
I _{OH} (peak)	"H" peak output current P0 ₀ ~P0 ₄			-40	mA
I _{OH} (peak)	"H" peak output current P0 ₅ ~P0 ₇ , P1 ₀ ~P1 ₇			-30	mA
I _{OH} (peak)	"H" peak output current P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁			-24	mA
I _{OH} (peak)	"H" peak output current P6 ₀ ~P6 ₅			-3	mA
I _{OL} (peak)	"L" peak output current P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇			15	mA
I _{OL} (peak)	"L" peak output current P6 ₀ ~P6 ₅			3	mA
I _{OH} (avg)	"H" average output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇			-18	mA
I _{OH} (avg)	"H" average output current P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁			-12	mA
I _{OH} (avg)	"H" average output current P6 ₀ ~P6 ₅			-1.5	mA
I _{OL} (avg)	"L" average output current P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇			10	mA
I _{OL} (avg)	"L" average output current P6 ₀ ~P6 ₅			1.5	mA
f(P3 ₂ /CNTR)	Timer 3 counter clock input oscillation frequency (Note 2)	f(X _{IN})=4.2MHz		250	kHz
		f(X _{CIN})=32kHz		50	
f(X _{IN})	Clock input oscillating frequency (Note 2, 3, 5)			4.2	MHz
f(X _{CIN})	Clock oscillating frequency for clock function	32.768		50	kHz

- Note 1 : High-level input voltage of up to +12V may be applied to permissible for ports P2₀~P2₇, P3₀~P3₂, P3₄~P3₇, CNV_{SS}, and P5₂~P5₇
 2 : Oscillation frequency is at 50% duty cycle
 3 : When used in the low-speed mode, the timer clock input frequency should be f(X_{IN}) < f(X_{IN})/3
 4 : When external clock input is used, the timer clock input frequency should be f(X_{CIN}) ≤ 50kHz
 5 : The average output current I_{OL}(avg) and I_{OH}(avg) are in period of 100ms.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = 25^\circ C$, $f(X_{IN}) = 4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
V_{OH}	"H" output voltage P6 ₀ ~P6 ₅	$I_{OH} = -0.5mA$	$V_{CC} - 0.4$			V
V_{OH}	"H" output voltage ϕ	$I_{OH} = -2.5mA$	$V_{CC} - 2$			V
V_{OH}	"H" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇	$I_{OH} = -18mA$	$V_{CC} - 2$			V
V_{OH}	"H" output voltage P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁	$I_{OL} = -12mA$	$V_{CC} - 2$			V
V_{OL}	"L" output voltage P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇	$I_{OL} = 10mA$			2	V
V_{OL}	"L" output voltage P6 ₀ ~P6 ₅	$I_{OL} = 0.5mA$			0.4	V
V_{OL}	"L" output voltage ϕ	$I_{OL} = 2.5mA$			2	V
$V_{T+} - V_{T-}$	Hysteresis P5 ₂ /INT ₂ , P5 ₃ /INT ₁		0.3		1	V
$V_{T+} - V_{T-}$	Hysteresis RESET			0.5	0.7	V
$V_{T+} - V_{T-}$	Hysteresis P3 ₆	When used as CLK input	0.3		1	V
$V_{T+} - V_{T-}$	Hysteresis X _{IN}		0.1		0.5	V
I_{IL}	"L" input current P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇	$V_i = 0V$			-5	μA
I_{IL}	"L" input current P6 ₀ ~P6 ₅	$V_i = 0V$			-5	μA
I_{IL}	"L" input current P5 ₄ ~P5 ₇	$V_i = 0V$			-5	μA
I_{IL}	"L" input current RESET, X _{IN} , X _{CIN}	$V_i = 0V$			-5	μA
I_{IL}	"L" input current P5 ₂ /INT ₂ , P5 ₃ /INT ₁	$V_i = 0V$			-5	μA
I_{IH}	"H" input current	P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P4 ₀ ~P4 ₇	$V_i = 5V$ $V_i = 12V$		5 12	μA
I_{IH}	"H" input current P6 ₀ ~P6 ₅	$V_i = 5V$			5	μA
I_{IH}	"H" input current P5 ₄ ~P5 ₇	$V_i = 5V$			5	μA
I_{IH}	"H" input current RESET, X _{IN} , X _{CIN}	$V_i = 5V$			5	μA
I_{IH}	"H" input current P5 ₂ /INT ₂ , P5 ₃ /INT ₁	$V_i = 5V$ $V_i = 12V$			5 12	μA
I_{LOAD}	Output load current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁	$V_P = V_{CC} - 36V$, $V_{OL} = V_{CC}$	150	500	900	μA
I_{LEAK}	Output leak current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ , P5 ₁	$V_P = V_{CC} - 38V$, $V_{OL} = V_{CC} - 38V$			30	μA
V_{RAM}	RAM retention voltage	at clock stop	2		5.5	V
I_{CC}	Supply current	Output pins open (output OFF) $V_P = V_{CC}$, $V_P = V_{SS}$ Input and I/O pins all at V_{SS} X _{IN} =4MHz (system operation)		6	12	mA

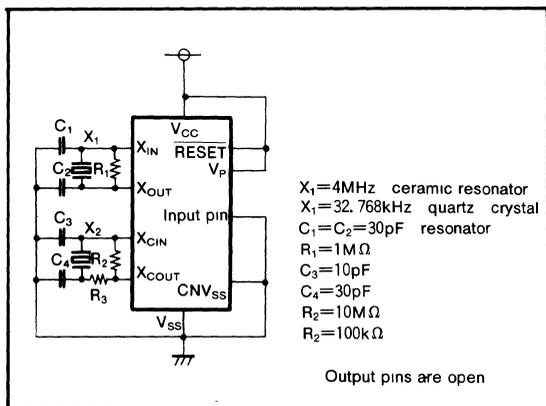


Fig.3 Supply current test circuit

MITSUBISHI MICROCOMPUTERS

M37120E6-XXXFP

PROM VERSION of M37120M6-XXXFP

DESCRIPTION

The M37120E6-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin plastic molded QFP. The features of this chip are similar to those of the M37120M6-XXXFP except that this chip has a 12288 bytes PROM built in. This single-chip microcomputer is useful for appliance controllers.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

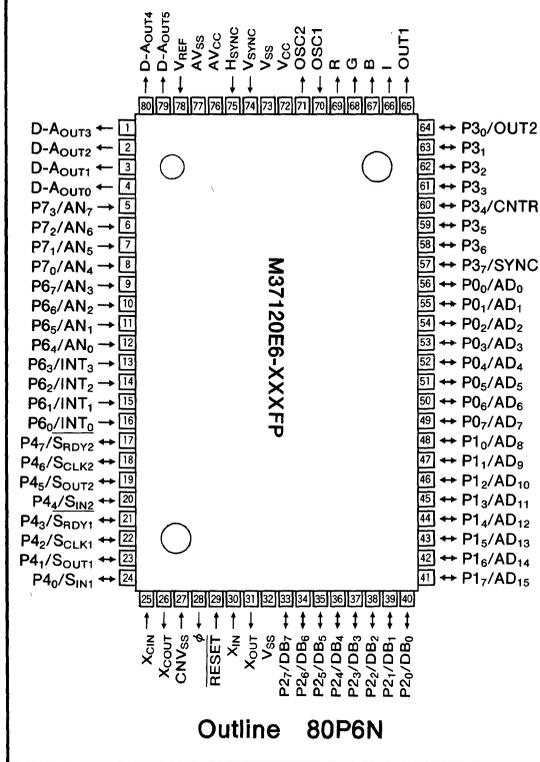
FEATURES

- Number of basic instructions 71
- Memory size PROM 12288 bytes
RAM 256 bytes
- Instruction execution time
..... 1 μ s (minimum instructions at 4MHz frequency)
- Single power supply
f(X_{IN})=4MHz 5V \pm 10%
- Power dissipation
normal operation mode (at 4MHz frequency)
..... 75mW
- Subroutine nesting 128 levels (Max.)
- Interrupt 14 types, 14 vectors
- 8-bit timer 4
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4) 40
- Input ports (Ports P6, P7) 12
- Serial I/O (8-bit) 2
- A-D converter (8-bit resolution) 8 channels
- D-A converter (8-bit resolution) 6 channels
- Watchdog timer
- 72-character on screen display function
Number of character 24 characters \times 3 lines
Kinds of character 126
- Two clock generating circuits
(One is for main clock, the other is for clock function)
- PROM (equivalent to the M5L27256)
program voltage 12.5V

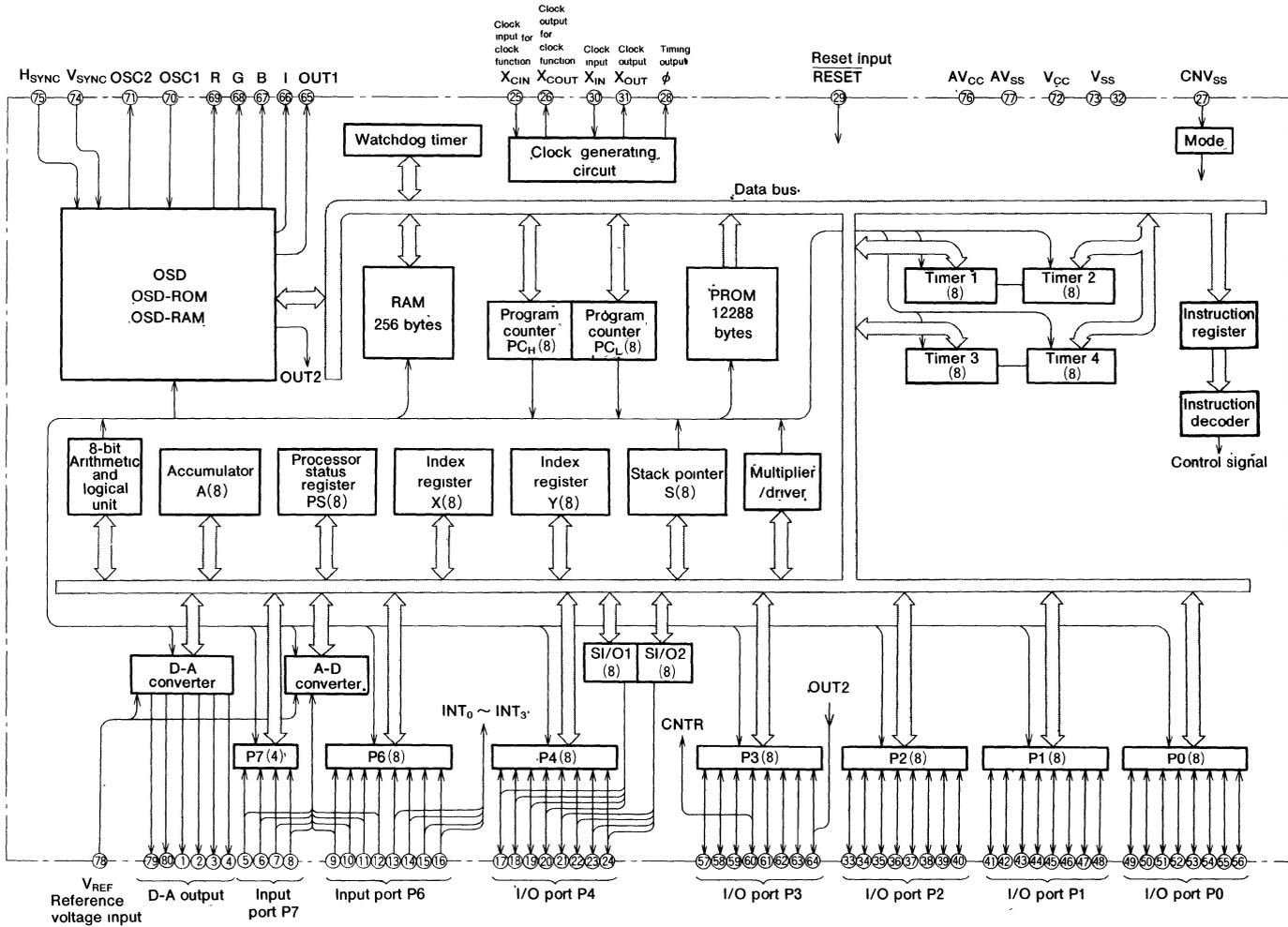
APPLICATION

TV, VCR

PIN CONFIGURATION (TOP VIEW)



M37120E6-XXXFP BLOCK DIAGRAM



MITSUBISHI
ELECTRIC

PROM VERSION of M37120M6-XXXFP

MITSUBISHI MICROCOMPUTERS
M37120E6-XXXFP

FUNCTIONS OF M37120E6-XXXFP

Parameters		Functions	
Number of basic instructions		71	
Instruction execution time		1 μ s (minimum instructions, at 4MHz of frequency)	
Clock frequency		4MHz	
Memory size	PROM	12288bytes	
	RAM	256bytes	
Input/Output port	P0, P1, P2, P3	I/O	8-bitX4
	P4	I/O	8-bitX1 (N-channel open drain output)
	P6	Input	8-bitX1
	P7	Input	4-bitX1
	I, B, G, R, OUT1	Output	1-bitX5(for CRT display function)
	V _{SYNC} , H _{SYNC}	Input	1-bitX2(for CRT display function)
	D-A _{OUT0} ~D-A _{OUT5}	Output	1-bitX6
Serial I/O		8-bitX2	
Timers		8-bit timerX4	
Subroutine nesting		128(max)	
Interrupt		Four external Interrupts, nine internal interrupts, one software interrupt	
Clock generating circuit		Two built-in circuits (ceramic or quartz crystal oscillator)	
Supply voltage		5V \pm 10%	
Operating temperature range		-10~70°C	
Device structure		CMOS silicon gate	
Package		80-pin plastic molded QFP	
CRT display function	Number of character	24 charactersX3 lines	
	Kinds of character	126(12X16 dots)	

MITSUBISHI MICROCOMPUTERS
M37120E6-XXXFP

PROM VERSION of M37120M6-XXXFP

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{CC} , V_{SS}	Single-chip /EPROM	Power supply		Supply $5V \pm 10\%$ to V_{CC} and 0V to V_{SS}
AV_{CC} , AV_{SS}	Single-chip	Analog power supply		Power supply input for A-D and D-A converters
	EPROM	Analog power supply		Connect to AV_{CC} to V_{CC} and AV_{SS} to V_{SS}
CNV_{SS} / V_{PP}	Single-chip	CNV_{SS} input	Input	Connect to V_{SS} .
	EPROM	V_{PP} input	Input	Connect to V_{PP} when programming or verifying
V_{REF}	Single-chip	Reference voltage input	Input	Reference voltage input for A-D and D-A converters
	EPROM	Reference voltage input	Input	Connect to V_{SS}
\overline{RESET}	Single-chip	Reset input	Input	To reset, keep this input terminal low for more than $2\mu s$ (min) under normal V_{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	Reset input	Input	Connect to 0V
X_{IN}	Single-chip	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}		Clock output	Output	
X_{IN}	EPROM	Clock input	Input	Connect to V_{CC}
X_{OUT}		Clock output	Output	Open.
X_{CIN}	Single-chip	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function.
X_{COUT}		Clock output for clock function	Output	
X_{CIN}	EPROM	Clock input for clock function	Input	Connect to V_{CC} .
X_{COUT}		Clock output for clock function	Output	Open.
ϕ	Single-chip	Timing output	Output	The function of this pin can be selected either timing output or resetout output.
	EPROM	Timing output	Output	Open.
$D-A_{OUT0}$ }	Single-chip	D-A output	Output	Analog signal from D-A converter is output.
	EPROM	D-A output	Output	Open.
$P0_0 \sim P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
	EPROM	Address input $A_0 \sim A_7$	Input	P0 works as the lower 8 bit address input ($A_0 \sim A_7$)

PIN DESCRIPTION (Continued)

Pin	Mode	Name	Input/ Output	Functions
P1 ₀ ~P1 ₇	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0
	EPROM	Address input A ₈ ~A ₁₃	Input	P1 ₀ ~P1 ₆ works as the higher 6 bit address inputs (A ₈ ~A ₁₄). Connect to P1 ₇ to V _{CC} when the microcomputer accesses to program ROM Connect to P1 ₇ to V _{SS} when the microcomputer accesses to OSD ROM
P2 ₀ ~P2 ₇	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as port P0
	EPROM	Data input/ output D ₀ ~D ₇	I/O	Port P2 works as an 8 bit data bus (D ₀ ~D ₇)
P3 ₀ ~P3 ₇	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. Port P3 ₀ is in common with CRT input pin and P3 ₄ is in common with counter input pin
	EPROM	Select mode	Input	P3 ₃ , P3 ₄ work as \overline{CE} and \overline{OE} , respectively Connect to P3 ₀ ~P3 ₂ and P3 ₅ ~P3 ₇ to V _{CC} .
P4 ₀ ~P4 ₇	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain
	EPROM	Input port P4	Input	Connect to V _{SS}
P6 ₀ ~P6 ₇	Single-chip	Input port P6	Input	Port P6 is an 8-bit input port P6 ₀ ~P6 ₃ are in common with interrupt input pins and P6 ₄ ~P6 ₇ are in common with analog input pins
	EPROM	Input port P6	Input	Connect to V _{SS}
P7 ₀ ~P7 ₃	Single-chip	Input port P7	Input	This port is an 4-bit input port and is in common with analog input pins
	EPROM	Input port P7	Input	Connect to V _{SS}
OSC1	Single-chip	Clock input for CRT display	Input	This is the input pin of the clock generating circuit for the CRT display function
	EPROM		Input	Connect to V _{CC}
OSC2	Single-chip	Clock output for CRT display	Output	This is the output pin of the clock generating circuit for the CRT display function
	EPROM		Output	Open
H _{SYNC}	Single-chip	H _{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display
	EPROM	H _{SYNC} input	Input	Connect to V _{SS}
V _{SYNC}	Single-chip	V _{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display
	EPROM	V _{SYNC} input	Input	Connect to V _{SS}
R, G, B, I, OUT1	Single-chip	CRT output	Output	This is an 5-bit output pin for CRT display
	EPROM	CRT output	Output	Open

M37120E6-XXXXP

PROM VERSION of M37120M6-XXXXP

EPROM MODE

The M37120E6-XXXXP features an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 gives the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, P3₃, P3₄ and CNV_{SS} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256.

Table 1. Pin function in EPROM mode

	M37120E6-XXXXP	M5L27256
V _{CC}	V _{CC}	V _{CC}
V _{PP}	CNV _{SS} /V _{PP}	V _{PP}
V _{SS}	V _{SS}	V _{SS}
Address input	Ports P0, P1	A ₀ ~A ₁₄
Data I/O	Port P2	D ₀ ~D ₇
CE	P3 ₃ /CE	CE
OE	P3 ₄ /OE	OE

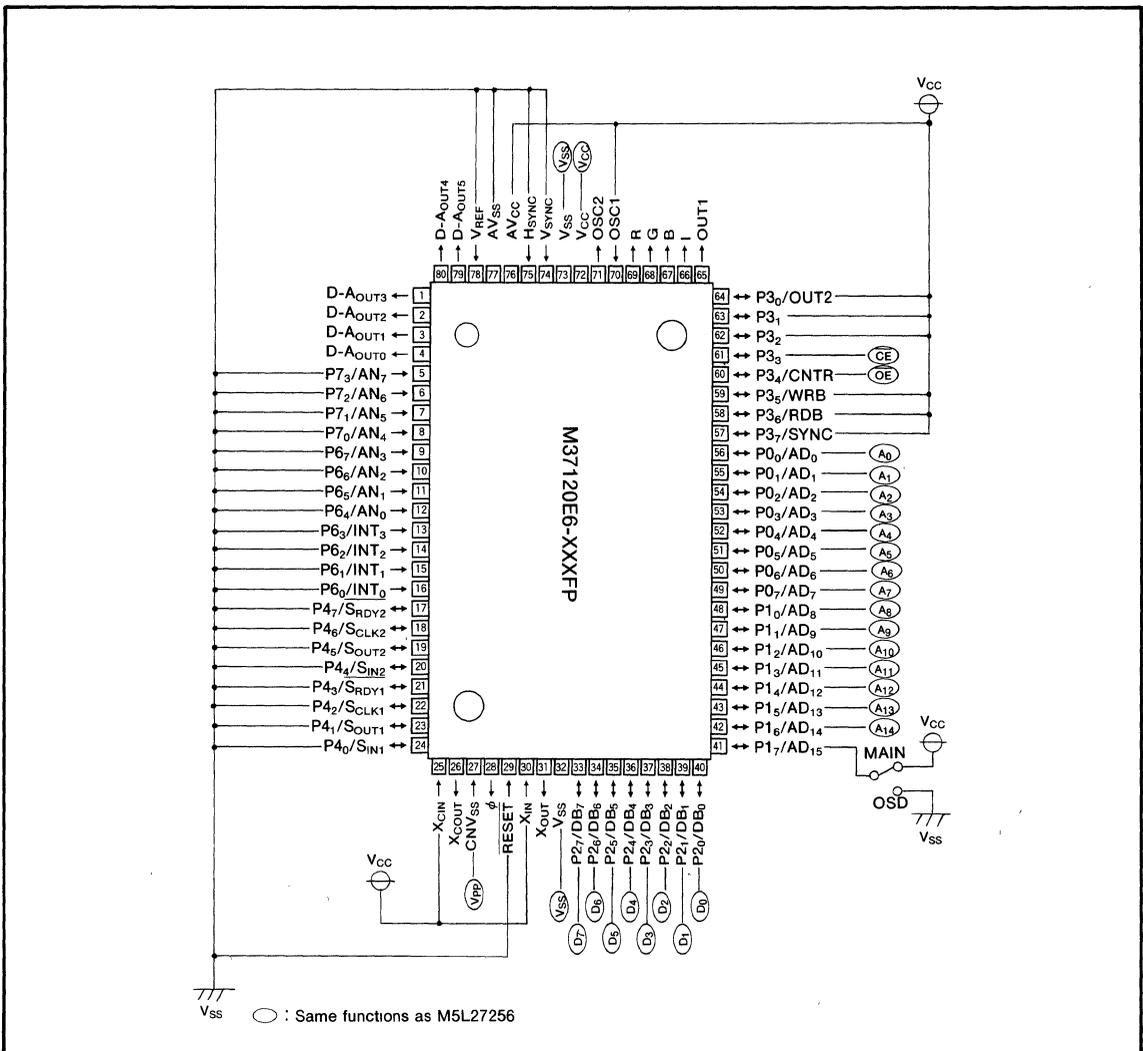


Fig.1 Pin connection in EPROM mode

PROM VERSION of M37120M6-XXXFP

PROM READING AND WRITING

Reading

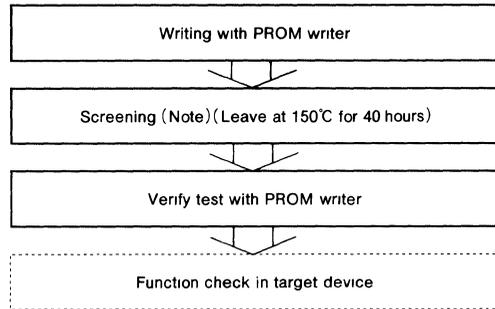
To read the PROM, set the \overline{CE} and \overline{OE} pins to a "L" level. Input the address of the data ($A_0 \sim A_{14}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when the \overline{OE} pin is in the "H" state.

Writing

To write to the PROM, set the \overline{OE} pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{14}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the \overline{CE} pin to a "L" level to begin writing.

NOTES ON HANDLING

- (1) Since a high voltage (12.5V) is used to write data, care should be taken when turning on the PROM writer's power.
- (2) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150°C exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}(61)$	$\overline{OE}(60)$	$V_{PP}(27)$	$V_{CC}(72)$	Data I/O (33~40, 42~56)
Read-out	V_{IL}	V_{IL}	5V	5V	Output
Output disable	V_{IL}	V_{IH}	5V	5V	Floating
	V_{IH}	X	5V	5V	Floating
Programming	V_{IL}	V_{IH}	12.5V	6V	Input
Programming verify	V_{IH}	V_{IL}	12.5V	6V	Output
Program disable	V_{IH}	V_{IH}	12.5V	6V	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
 2 : An X indicates either V_{IL} or V_{IH}

MITSUBISHI MICROCOMPUTERS

M37410E6HXXXFP

M37410E6HFS

PROM VERSION of M37410M3HXXXFP, M37410M4HXXXFP, M37410M6HXXXFP

DESCRIPTION

The M37410E6HFS, M37410E6HXXXFP are single-chip microcomputers designed with CMOS silicon gate technology. M37410E6HXXXFP is housed in a 80-pin shrink plastic molded QFP. M37410E6HFS is housed in a 80-pin ceramic QFP. The features of M37410E6HXXXFP are similar to those of the M37410M4HXXXFP except that this chip has a 12288 bytes PROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

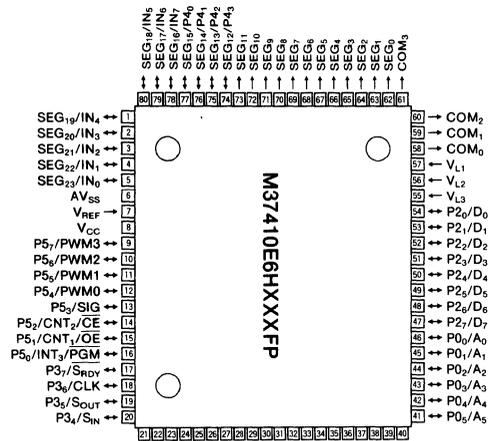
In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The M37410E6HFS are the window type. The differences between the M37410E6HXXXFP and the M37410E6HFS are the package outline and the power dissipation ability (absolute maximum ratings).

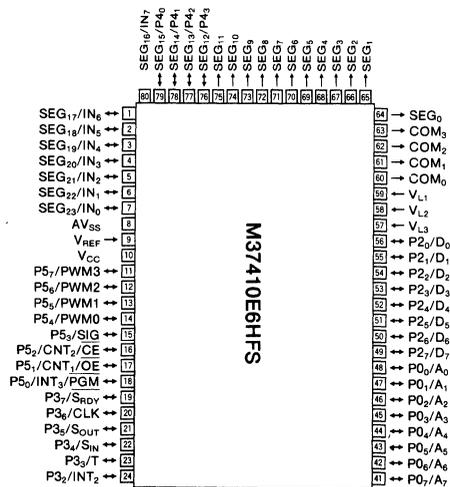
FEATURES

- Number of basic instructions 69
- Memory size PROM 12288 bytes
RAM 256 bytes
- Instruction execution time (minimum instructions)
at high-speed mode 1 μ s
at low-speed mode 4 μ s
- Single power supply
M37410E6HXXXFP 2.5~5.5V
M37410E6HFS 4.5~5.5V
- Power dissipation
normal operation mode (at 8MHz frequency)
..... 30mW ($V_{CC}=5V$, Typ.)
low-speed operation mode (at 32kHz frequency for
clock function) 54 μ W ($V_{CC}=3V$, Typ.)
- RAM retention voltage (stop mode)
..... 2.0V $\leq V_{RAM} \leq 5.5V$
- Subroutine nesting 96 levels (Max.)
- Interrupt 10 types, 5 vectors
- 8-bit timer 4
- 16-bit timer 1 (Two 8-bit timers make one set)
- Programmable I/O ports
(Ports P0, P1, P2, P3, P5) 40
- Input port (Port P4) 4
- Serial I/O (8-bit) 1
- A-D converter 8-bit, 8-channel
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
segment output 24
common output 4
- Two clock generating circuits
(One is for main clock, the other is for clock function)
- PROM (equivalent to the M5L27128)
program voltage 21V

PIN CONFIGURATION (TOP VIEW)



Outline 80P6S (OTP)



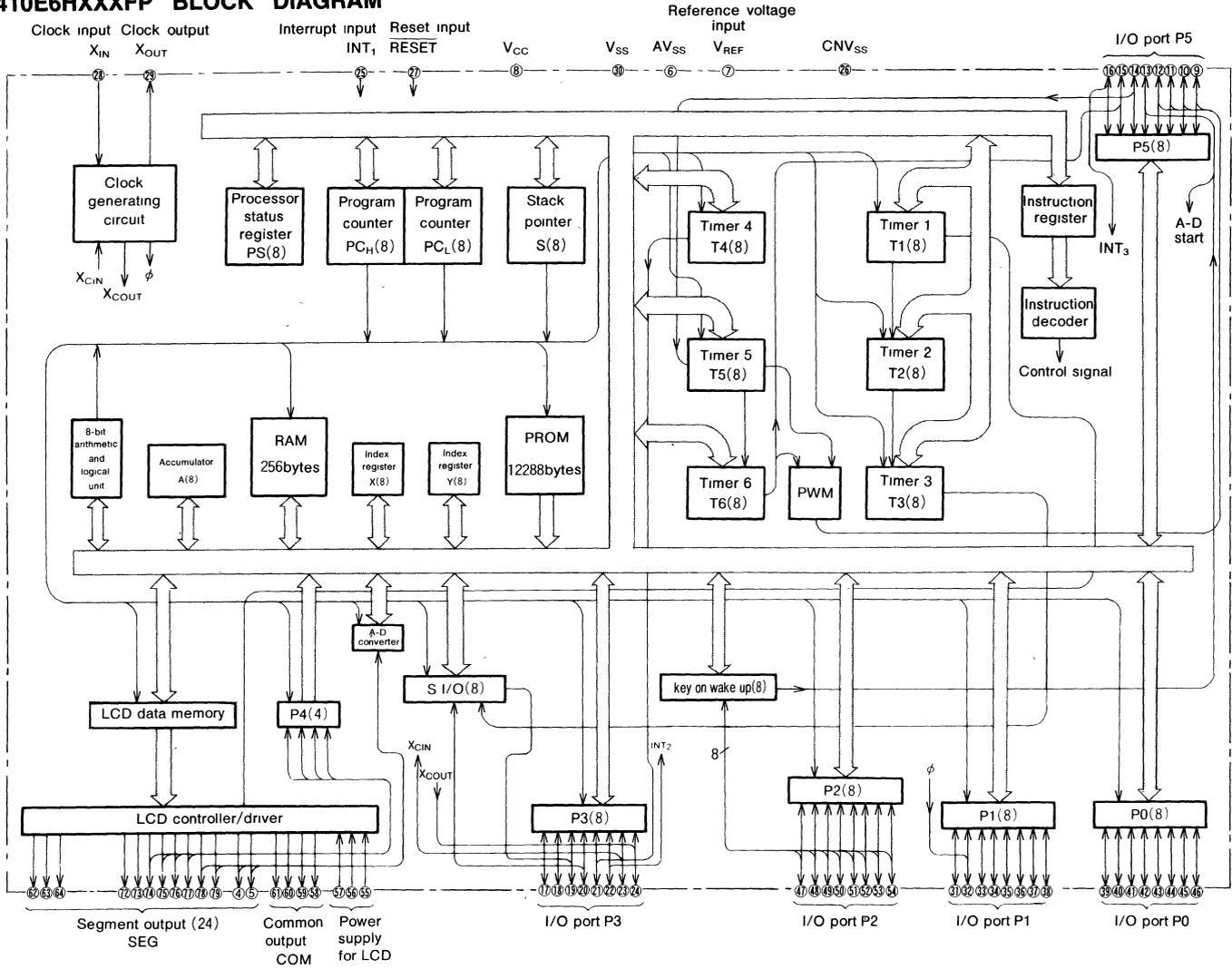
Outline 80S6 (Window)

APPLICATION

- Audio-visual equipment
- Remote control
- Camera



M37410E6HXXXFP BLOCK DIAGRAM



FROM VERSION OF M37410M3HXXXFP, M37410M4HXXXFP, M37410M6HXXXFP

MITSUBISHI MICROCOMPUTERS
M37410E6HXXXFP
M37410E6HFS

M37410E6HXXFP
M37410E6HFS

PROM VERSION of M37410M3HXXFP, M37410M4HXXFP, M37410M6HXXFP

FUNCTIONS OF M37410E6HXXFP

Parameters		Functions
Number of basic instructions		69
Instruction execution time		1 μ s (minimum instructions, at 8MHz of frequency)
Clock frequency		8MHz
Memory size	PROM	12288bytes (Note 1)
	RAM	256bytes
	RAM for display LCD	12bytes
Input/Output port	P0, P1, P2, P3, P5	I/O 8-bitX5
	P4	Input 4-bitX1 (Port P4 are in common with SEG)
	SEG	LCD output 24-bitX1
	COM	LCD output 4-bitX1
Serial I/O		8-bitX1
Timers		8-bit timerX4 16-bit timerX1 (combination of two 8-bit timers)
LCD controller/driver	Bias	1/2, 1/3 bias selectable
	Duty ratio	1/2, 1/3, 1/4 duty selectable
	Common output	4
	Segment output	24(SEG ₁₂ ~SEG ₂₃ are in common with port P4 and analog input pins)
Subroutine nesting		96(max)
Interrupt		Three external interrupts, three timer interrupts (or two timer, one serial I/O)
Clock generating circuit		Two built-in circuits (ceramic or quartz crystal oscillator)
Operating temperature range		-10~70°C
Device structure		CMOS silicon gate
Package		80-pin plastic molded QFP

Note 1 : The PROM programming voltage is 21V (equivalent to the M5L27128)

PROM VERSION of M37410M3HXXXFP, M37410M4HXXXFP, M37410M6HXXXFP

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Single-chip /EPROM	Power supply		Supply 5V±5% to V _{CC} and 0V to V _{SS}
CNV _{SS} / V _{PP}	Single-chip	CNV _{SS}		Connect to V _{SS} .
	EPROM	V _{PP} input	Input	Connect to V _{PP} when programming or verifying
RESET	Single-chip	Reset input	Input	To reset, keep this input terminal low for more than 16μs (min) under normal V _{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	Reset input		Connect to 0V.
X _{IN}	Single-chip /EPROM	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected to the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}		Clock output	Output	
INT ₁	Single-chip	Interrupt input	Input	This is the highest order interrupt input pin.
	EPROM	Interrupt input	Input	Connect to 0V.
P0 ₀ ~P0 ₇	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
	EPROM	Address input A ₀ ~A ₇	Input	P0 works as the lower 8 bit address input (A ₀ ~A ₇).
P1 ₀ ~P1 ₇	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open drain.
	EPROM	Address input A ₈ ~A ₁₃	Input	P1 ₀ ~P1 ₅ works as the higher 6 bit address inputs (A ₈ ~A ₁₃). Connect P1 ₆ ~P1 ₇ to V _{CC} .
P2 ₀ ~P2 ₇	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as port P0. Also all bits are for key on wake up input pins.
	EPROM	Data input/ output D ₀ ~D ₇	I/O	Port P2 works as an 8 bit data bus (D ₀ ~D ₇).
P3 ₀ ~P3 ₇	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ and P3 ₄ work as S _{RDY} , CLK, S _{OUT} , and S _{IN} pins, respectively. Also P3 ₃ , P3 ₂ , P3 ₁ , and P3 ₀ work as timer 4 overflow signal divided by 2 output pin (T), INT ₂ pin, X _{CIN} and X _{COUT} pins, respectively.
	EPROM	Input port P3	Input	Connect to 0V.
SEG ₁₂ /P4 ₃ } SEG ₁₅ /P4 ₀	Single-chip	Segment output /input port P4	Output /Input	SEG ₁₂ ~SEG ₁₅ are segment output pins. Also these work as input port P4 by 2-bit unit.
	EPROM	Input port P4	Input	Connect to V _{CC} .
P5 ₀ ~P5 ₇	Single-chip	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P1. P5 ₀ , P5 ₁ , P5 ₂ and P5 ₃ are in common with INT ₃ , timer3 input, timer5 input and A-D trigger input, respectively.
	EPROM	Select mode	Input	P5 ₂ , P5 ₁ , P5 ₀ work as \overline{CE} , \overline{OE} and PGM, respectively. Connect to P5 ₅ ~P5 ₇ to 0V, and P5 ₃ ~P5 ₄ to V _{CC} .

PIN DESCRIPTION (Continued)

Pin	Mode	Name	Input/ Output	Functions
V _{L1} ~V _{L3}	Single-chip	Voltage input for LCD	Input	These are voltage input pins for LCD. Supply voltage as $0V \leq V_{L1} \leq V_{L2} \leq V_{L3} \leq V_{CC}$. $0 \sim V_{L3}V$ is supplied to LCD.
	EPROM	Voltage input for LCD	Input	Connect to V _{CC}
COM ₀ ~ COM ₃	Single-chip	Common output	Output	These are LCD common output pins.
	EPROM	Common output	Output	Connect to V _{CC}
SEG ₀ ~ SEG ₁₁	Single-chip	Segment output	Output	These are LCD segment output pins.
	EPROM	Segment output	Output	Connect to V _{CC}
SEG ₁₆ /IN ₇ } SEG ₂₃ /IN ₀	Single-chip	Segment output /analog input	I/O	SEG ₁₆ ~SEG ₂₃ work as analog input pins IN ₇ ~IN ₀ . SEG ₁₆ ~SEG ₁₉ are used by 2-bit unit and SEG ₂₀ ~SEG ₂₃ by 4-bit unit.
	EPROM	Analog input	Input	Connect to V _{CC}
AV _{SS}	Single-chip	Analog voltage input	Input	GND input pin for the A-D converter.
	EPROM	Analog voltage input	Input	Connect to V _{SS}
V _{REF}	Single-chip	Reference voltage input	Input	Reference input pin for A-D converter.
	EPROM	Reference voltage input	Input	Connect to V _{CC}

M37410E6HXXXFP M37410E6HFS

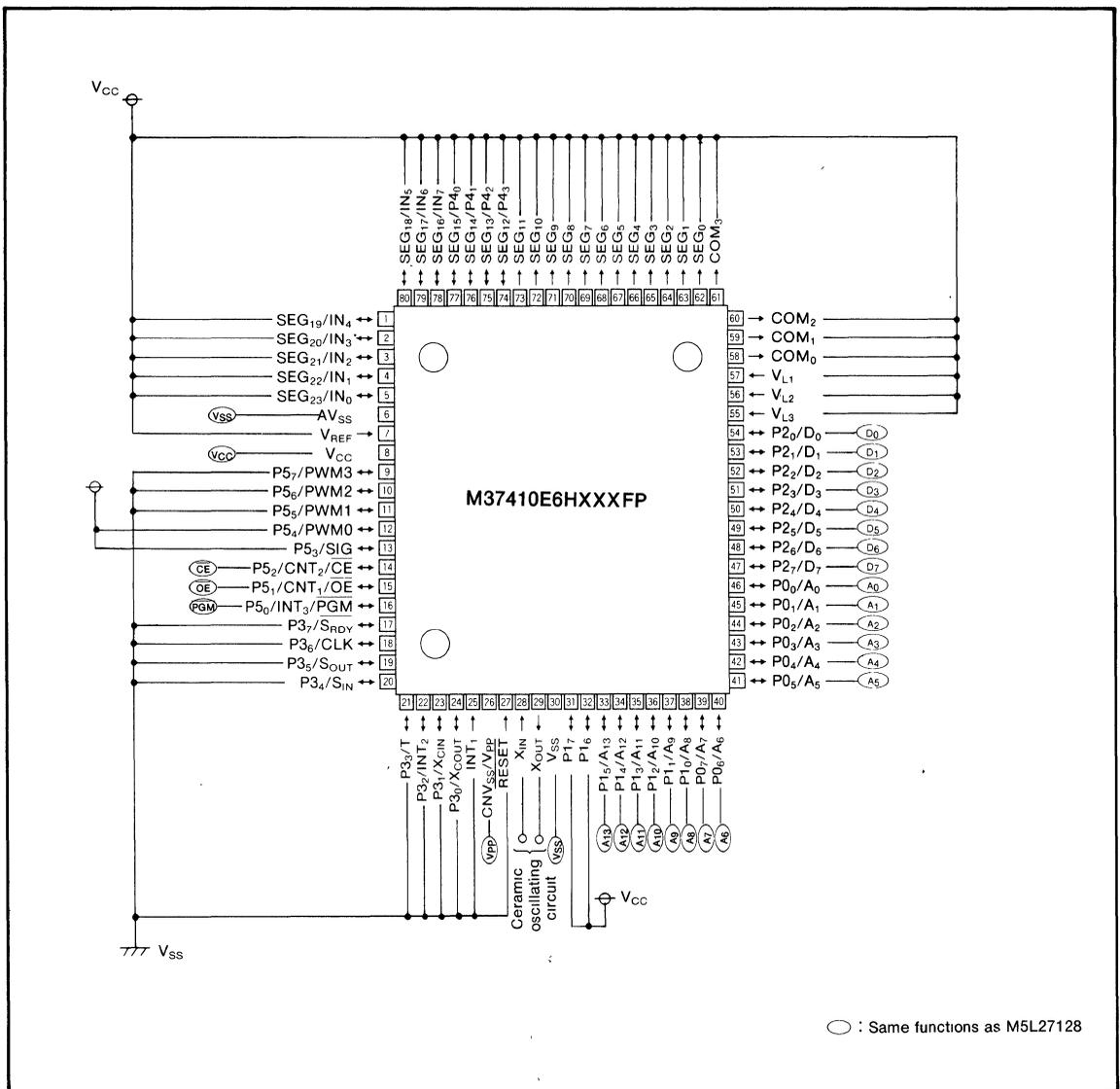
PROM VERSION of M37410M3HXXXFP, M37410M4HXXXFP, M37410M6HXXXFP

EPROM MODE

The M37410E6HXXXFP, M37410E6HFS feature an EPROM mode in addition to its normal modes. When the RESET signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1, Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, P5₀ ~ P5₂, and CNV_{SS} are used for the PROM (equivalent to the M5L27128). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37410E6HXXXFP, M37410E6HFS	M5L27128
V _{CC}	V _{CC}	V _{CC}
V _{PP}	CNV _{SS} /V _{PP}	V _{PP}
V _{SS}	V _{SS}	V _{SS}
Address input	Ports P0, P1 ₀ ~P1 ₅	A ₀ ~A ₁₃
Data I/O	Port P2	D ₀ ~D ₇
CE	P5 ₂ /CE	CE
OE	P5 ₁ /OE	OE
PGM	P5 ₀ /PGM	PGM



○ : Same functions as M5L27128

Fig.1 Pin connection in EPROM mode

M37410E6HXXFP
M37410E6HFS

PROM VERSION of M37410M3HXXFP, M37410M4HXXFP, M37410M6HXXFP

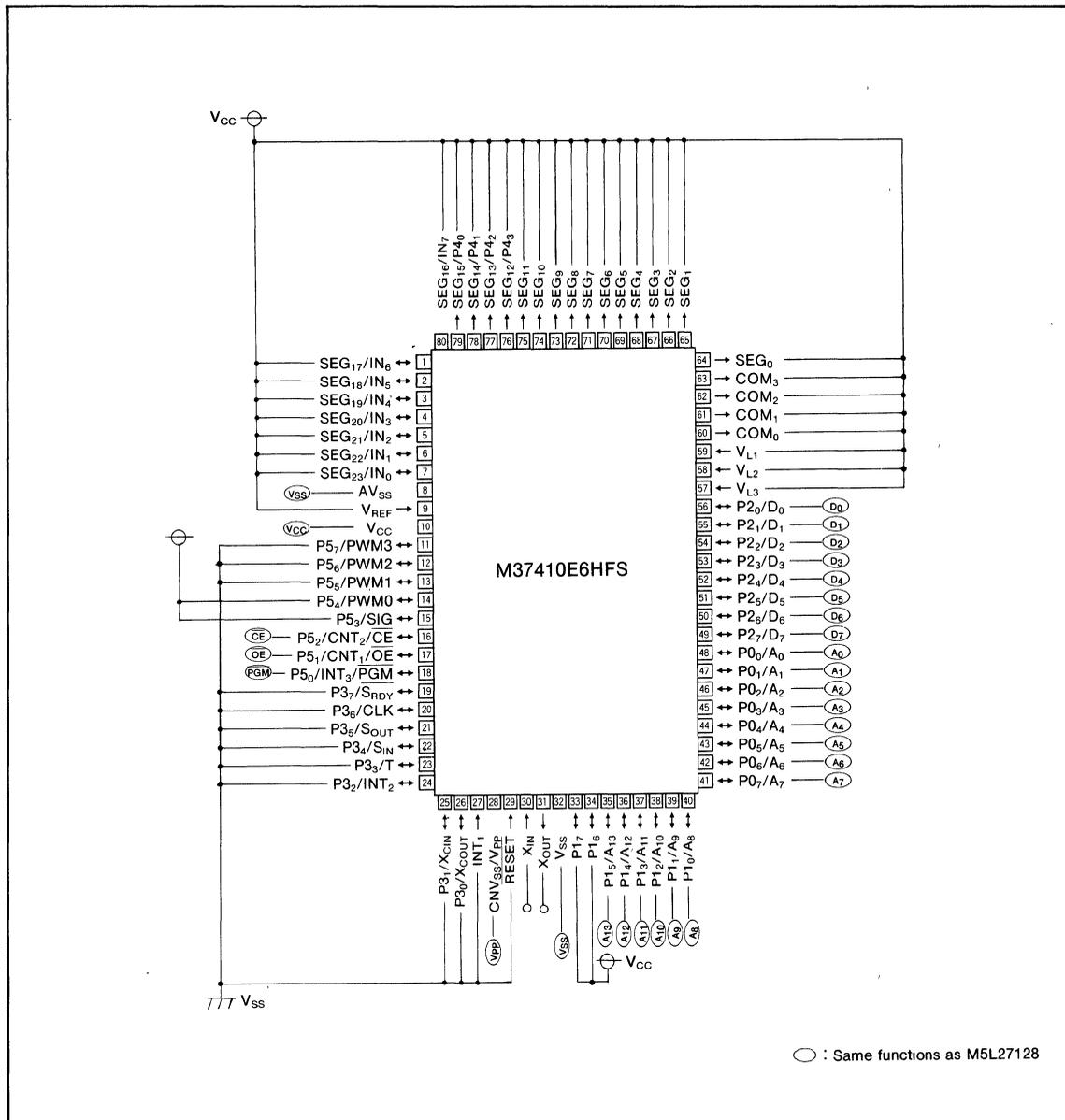


Fig.2 Pin connection in EPROM mode

PROM VERSION of M37410M3HXXXFP, M37410M4HXXXFP, M37410M6HXXXFP

PROM READING, WRITING AND ERASING
Reading

To read the PROM, set the \overline{CE} and \overline{OE} pins to a "L" level, and the \overline{PGM} pin to a "H" level. Input the address of the data ($A_0 \sim A_{13}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the \overline{CE} or \overline{OE} pins are in the "H" state.

Writing

To write to the PROM, set the \overline{CE} pin to a "L" level and the \overline{OE} pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{13}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the \overline{PGM} pin to a "L" level to begin writing.

Erasing

Data can only be erased on the M37410E6HFS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is $15W \cdot s/cm^2$.

Functional differences from M37410M3HXXXFP or M37410M4HXXXFP, M37410M6HXXXFP
(excluding characteristic differences).

	M37410M3HXXXFP M37410M4HXXXFP M37410M6HXXXFP	M37410E6HXXXFP M37410E6HFS
Port P0 pull-up resistor	Option	Not provided
Port P1 pull-up resistor	Option	Not provided
Port P2 pull-up resistor	Option	Not provided
Port P3 pull-up resistor	Option	Not provided
Port P4 pull-up resistor	Option	Not provided
Port P5 pull-up resistor	Option	Not provided
Port P2 key on wake up	Option	Provided (all bits)

NOTES ON HANDLING

- (1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

Table 2. I/O signal in each mode

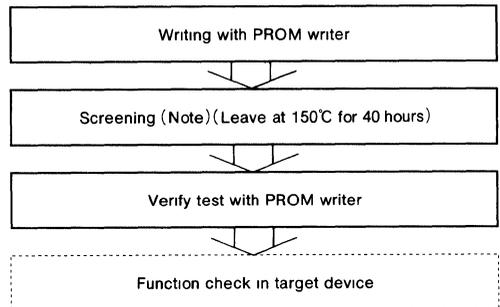
Mode \ Pin	$\overline{CE}(14)$	$\overline{OE}(15)$	$\overline{PGM}(16)$	$V_{PP}(26)$	$V_{CC}(8)$	Data I/O (47~54)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse ($V_{IH} \rightarrow V_{IL}$)	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}

- (2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.
- (3) Since a high voltage (21V) is used to write data, care should be taken when turning on the PROM writer's power.
- (4) Note that ports P3₀ and P3₁ of M37410E6HXXXFP or M37410E6HFS can not use as I/O ports when the external A-D start enable bit is set to "1" (enabled). This is because that bit 5 of the serial I/O mode register of M37410M3HXXXFP or M37410M4HXXXFP, M37410M6HXXXFP acts differently from that of M37410E6HXXXFP or M37410E6HFS, as compared in the table.
Bit 5 of serial I/O mode register when external A-D start enable bit is "1".

	Bit 5 of serial I/O mode register
M37410M3HXXXFP M37410M4HXXXFP M37410M6HXXXFP	Not affected
M37410E6HXXXFP M37410E6HFS	Automatically set to "1", and is fixed to "1" while external A-D start enable bit remains "1"

- (5) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150°C exceeding 100 hours.

PROM VERSION of M37410M3HXXXFP, M37410M4HXXXFP, M37410M6HXXXFP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~7	V
V _I	LCD supply V _{L1} ~V _{L3}	V _{L1} <V _{L2} <V _{L3}	-0.3~V _{CC} +0.3	V
V _I	Input voltage P ₀ ~P ₀₇ , P ₂ ₀ ~P ₂₇ , P ₃ ₀ , P ₃ ₁ , P ₄ ₀ ~P ₄ ₃ , IN ₀ ~IN ₇ , V _{REF} , X _{IN}		-0.3~V _{CC} +0.3	V
V _I	Input voltage CNV _{SS} . (Note 1)		-0.3~7	V
V _I	Input voltage INT ₁ , RESET, P ₁ ₀ ~P ₁₇ , P ₃ ₂ ~P ₃₇ , P ₅ ₀ ~P ₅₇		-0.3~10	V
V _O	Output voltage P ₀ ₀ ~P ₀₇ , P ₂ ₀ ~P ₂₇ , P ₃ ₀ , P ₃ ₁ , COM ₀ ~COM ₃ , SEG ₀ ~SEG ₂₃ , X _{OUT}		-0.3~V _{CC} +0.3	V
V _O	Output voltage P ₁ ₀ ~P ₁₇ , P ₃ ₂ ~P ₃₇ , P ₅ ₀ ~P ₅₇		-0.3~10	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

Note 1 : In PROM programming mode, CNV_{SS} is 21.0V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=-10~70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V _{CC}	Supply voltage (Note 1)	f(X _{IN})=8MHz High-speed mode f(X _{IN})=8MHz Normal mode or f(X _{IN})=2MHz High-speed mode (Note 2)	4.5 (Note 3)		5.5	V
V _{SS}	Supply voltage			0		V
V _{IH}	"H" input voltage P ₀ ₀ ~P ₀₇ , P ₃ ₀ , P ₃ ₁ , P ₄ ₀ ~P ₄ ₃ , X _{IN} , CNV _{SS} (Note 4)		0.7V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₂ ₀ ~P ₂₇		0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₁ ₀ ~P ₁₇ , P ₅ ₀ ~P ₅₇ , S _{IN}		0.7V _{CC}		10	V
V _{IH}	"H" input voltage P ₅ ₀ , INT ₁ , INT ₂ , INT ₃ , P ₃ ₂ ~P ₃₇ , CNT ₁ , CNT ₂ , SIG, CLK		0.8V _{CC}		10	V
V _{IH}	"H" input voltage RESET, X _{CIN}		0.85V _{CC}		10	V
V _{IL}	"L" input voltage P ₀ ₀ ~P ₀₇ , P ₁ ₀ ~P ₁₇ , P ₃ ₀ , P ₃ ₁ , P ₄ ₀ ~P ₄ ₃ , P ₅ ₀ ~P ₅₇ , S _{IN}		0		0.25V _{CC}	V
V _{IL}	"L" input voltage P ₂ ₀ ~P ₂₇ , P ₃ ₂ ~P ₃₇ , P ₅ ₀ , INT ₁ , INT ₂ , INT ₃ , CNT ₁ , CNT ₂ , SIG, CLK		0		0.2V _{CC}	V
V _{IL}	"L" input voltage RESET, X _{IN} , X _{CIN}		0		0.15V _{CC}	V
I _{OH}	"H" output current P ₀ ₀ ~P ₀₇ , P ₂ ₀ ~P ₂₇ , X _{OUT} (Note 5)				-1	mA
I _{OL}	"L" output current P ₀ ₀ ~P ₀₇ , P ₂ ₀ ~P ₂₇ , P ₃ ₀ ~P ₃₇ , P ₅ ₀ ~P ₅₇ , X _{OUT} , PWM ₀ ~PWM ₃ , T, S _{OUT} , CLK, S _{RDY} , SIG (Note 6)				1	mA
I _{OL}	"L" output current P ₁ ₀ ~P ₁₇ (Note 2)(Note 7)	V _{CC} =3V V _{CC} =5V			10 20	mA
f(X _{IN})	Clock oscillating frequency		0.2		8.2	MHz
f(X _{CIN})	Clock oscillating frequency for clock function		30		50	kHz

- Note 1 : When only maintaining the RAM data, minimum value of V_{CC} is 2V.
 2 : We say the high-speed mode, when the system clock is chosen X_{IN}/4, and the normal mode, when the system clock is chosen X_{IN}/16
 3 : In case M37410E6HFS, 4.5V
 4 : When P₃ is X_{CIN} mode, the limits of V_{IH} of P₃ is 0.85V_{CC}≤V_{IH}≤V_{CC}, 0≤V_{IL}≤0.15V_{CC}
 5 : Total of I_{OH(peak)} of ports P₀, P₂ and X_{OUT} is less than 35mA
 6 : Total of I_{OL(peak)} of ports P₀, P₂, P₃ and P₅ is less than 32mA
 7 : Total of I_{OL(peak)} of P₁ is less than 80mA
 Total of I_{OL(avg)} of P₁ is less than 40mA

PROM VERSION of M37410M3HXXXFP, M37410M4HXXXFP, M37410M6HXXXFP

ELECTRICAL CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{SS} = 0\text{V}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0 \sim P0_7, P2_0 \sim P2_7$	$V_{CC} = 5\text{V}, I_{OH} = -0.5\text{mA}$	4			V
V_{OH}	"H" output voltage X_{OUT}	$V_{CC} = 5\text{V}, I_{OH} = -0.3\text{mA}$	4			V
V_{OL}	"L" output voltage $P0_0 \sim P0_7, P2_0 \sim P2_7, P3_0 \sim P3_7, P5_0 \sim P5_7, T, S_{OUT}, CLK, \overline{S_{RDY}}, SIG, PWM0 \sim PWM3$	$V_{CC} = 5\text{V}, I_{OL} = 1\text{mA}$			1	V
V_{OL}	"L" output voltage $P1_0 \sim P1_7$	$V_{CC} = 5\text{V}, I_{OL} = 20\text{mA}$			2	V
V_{OL}	"L" output voltage X_{OUT}	$V_{CC} = 5\text{V}, I_{OL} = 0.3\text{mA}$			1	V
$V_{T+} - V_{T-}$	Hysteresis $INT_1, INT_2, INT_3, CLK, CNT_1, CNT_2, SIG, S_{IN}, P2_0 \sim P2_7, X_{CIN}$	$V_{CC} = 5\text{V}$		0.7		V
$V_{T+} - V_{T-}$	Hysteresis \overline{RESET}	$V_{CC} = 5\text{V}$		2		V
$V_{T+} - V_{T-}$	Hysteresis X_{IN}	$V_{CC} = 5\text{V}$		0.5		V
I_{IL}	"L" input current $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P3_0 \sim P3_7, P4_0 \sim P4_3, P5_0 \sim P5_7$ (Note 1), $IN_0 \sim IN_7, INT_1, \overline{RESET}, X_{IN}$	$V_{CC} = 5\text{V}$ $V_I = 0\text{V}$			-5	μA
I_{IH}	"H" input current $P0_0 \sim P0_7, P2_0 \sim P2_7, P3_0, P3_1, P4_0 \sim P4_7, IN_0 \sim IN_7, X_{IN}, X_{CIN}, CNV_{SS}$	$V_{CC} = 5\text{V}$ $V_I = 5\text{V}$			5	μA
I_{IH}	"H" input current $P1_0 \sim P1_7, P3_0 \sim P3_7, P5_0 \sim P5_7, INT_1, INT_2, INT_3, CNT_1, CNT_2, SIG, \overline{RESET}, S_{IN}, CLK$	$V_I = 10\text{V}$			10	μA
R_{COM}	Output impedance $COM_0 \sim COM_3$	$V_{L1} = V_{CC}/3$ $V_{L2} = 2V_{L1}$ $V_{L3} = V_{CC}$ Other COM, SEG pins are opened	$V_{CC} = 5\text{V}$	200		Ω
R_S	Output impedance $SEG_0 \sim SEG_{23}$		$V_{CC} = 5\text{V}$	2		k Ω
I_{CC}	Supply current	at operation	$f(X_{IN}) = 8\text{MHz}$ High-speed mode $V_{CC} = 5\text{V}$	6	12	mA
		at wait state	$f(X_{CIN}) = 32\text{kHz}, V_{CC} = 5\text{V}$	30	60	
		at stop state	$V_{CC} = 5\text{V}$, all clock stop $T_a = 25^\circ\text{C}$		0.1	1.0
V_{RAM}	RAM retention voltage		2		5.5	V

Note 1 : Also the same as when each pin is used as $INT_2, INT_3, CNT_1, CNT_2, SIG, S_{IN}$ and X_{IN} , respectively.

M37410E6HXXFP
M37410E6HFS

PROM VERSION of M37410M3HXXFP, M37410M4HXXFP, M37410M6HXXFP

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=8\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max	
—	Resolution				8	bits
—	Non-linearity error	$V_{CC}=V_{REF}=5.12V$			± 2	LSB
		$V_{CC}=V_{REF}=3.072V$			± 2	
—	Differential non-linearity	$V_{CC}=V_{REF}=5.12V$			± 0.9	LSB
		$V_{CC}=V_{REF}=3.072V$			± 0.9	
V_{OT}	Zero transition error	$V_{CC}=V_{REF}=5.12V$			2	LSB
		$V_{CC}=V_{REF}=3.072V$			2	
V_{FST}	Full-scale transition error	$V_{CC}=V_{REF}=5.12V$			6	LSB
		$V_{CC}=V_{REF}=3.072V$			10	
T_C	Conversion time	$V_{CC}=2.5\sim 5.5V$ High-speed mode		$200/(X_{IN})$		μs
		$V_{CC}=2.5\sim 5.5V$ Normal mode		$800/(X_{IN})$		
I_{REF}	Reference input current	$V_{REF}=5V$		1.0	2.5	mA
		$V_{REF}=3V$		0.5	1.5	
I_{IN}	Analog port input current	$V_{IN}=0\sim V_{CC}$		1	10	μA
V_{IN}	Analog input voltage	$V_{CC}=2.5\sim 5.5V$	AV_{SS}		V_{CC}	V
V_{REF}	Reference input voltage		2.5		V_{CC}	V

MITSUBISHI MICROELECTRONICS

M37412E5-XXXFP

PROM VERSION of M37412M4-XXXFP

DESCRIPTION

The M37412E5-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 72-pin plastic QFP. The features of this chip are similar to those of the M37412M4-XXXFP except that this chip has a 10240 bytes PROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

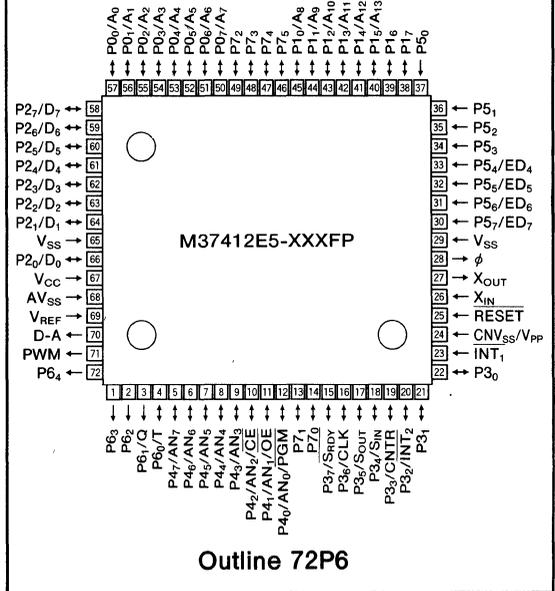
FEATURES

- Number of basic instructions 69
- Memory size PROM 10240 bytes
RAM 160 bytes
- Instruction execution time
..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply 5V±5%
- Power dissipation
normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting 80 levels (Max.)
- Interrupt 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4, P7)
..... 46
- Input port (Port P5) 8
- Output port (Port P6) 5
- Serial I/O (8-bit) 1
- A-D converter 8-bit successive approximation
- D-A converter
- 8-bit PWM function
- Watchdog timer
- PROM (equivalent to the M5L27128)
program voltage 21V

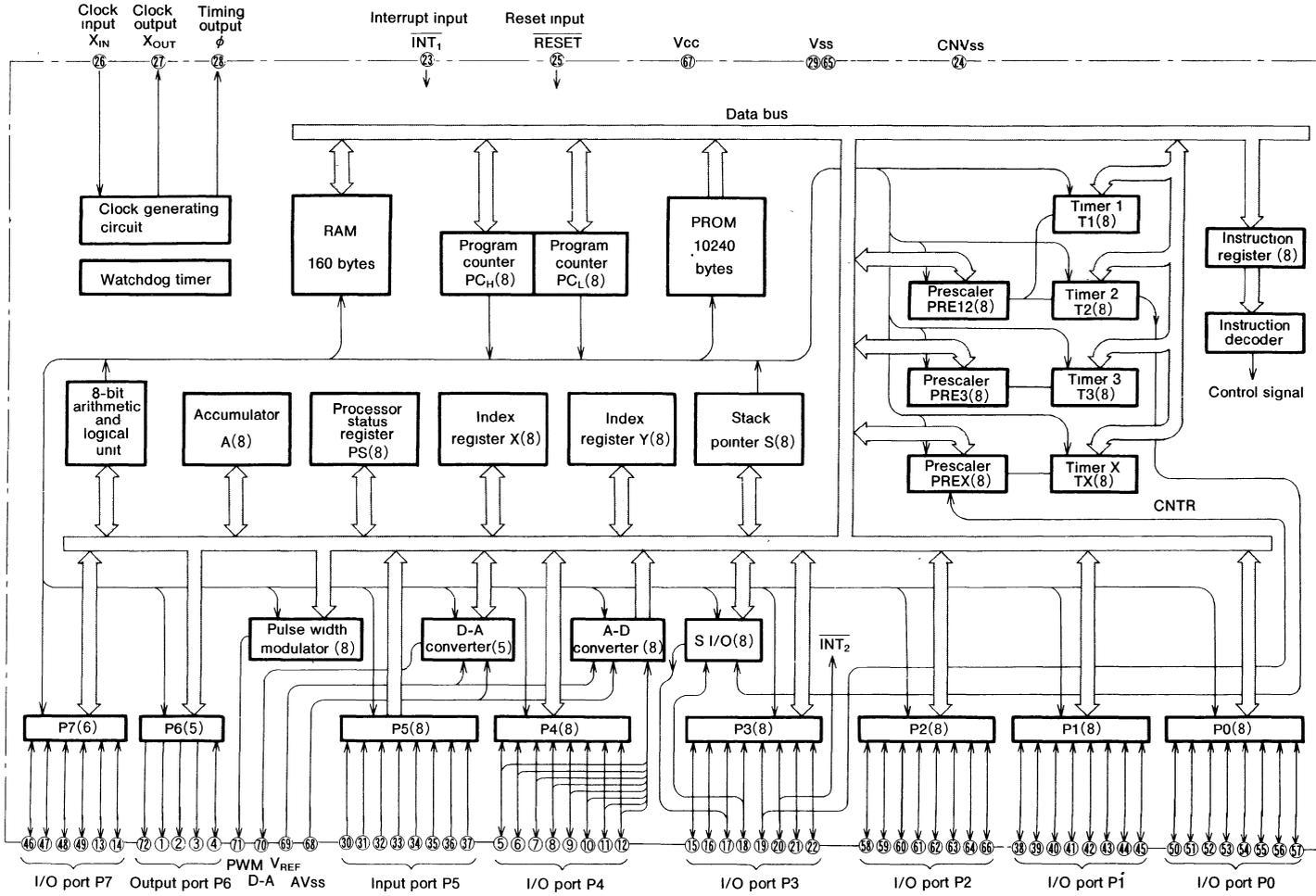
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



M37412E5-XXXFP BLOCK DIAGRAM



PROM VERSION of M37412M4-XXXFP

MITSUBISHI MICROCOMPUTERS
M37412E5-XXXFP

FUNCTIONS OF M37412E5-XXXFP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		2 μ s (minimum instructions, at 4MHz frequency)
Clock frequency		4MHz
Memory Size	PROM	10240 bytes (Note 1)
	RAM	160 bytes
Input/Output ports	INT ₁	Input 1-bitX1
	P0, P1, P2, P3, P4	I/O 8-bitX5 (a part of P3 is common with serial I/O, timer I/O, and interrupt input)
	P5	Input 8-bitX1
	P6	Output 5-bitX1 (a part of P6 is in common with external trigger output pin)
	P7	I/O 6-bitX1
Serial I/O		8-bitX1
Timers		8-bit prescalerX3+8-bit timerX4
A-D conversion		8-bitX1 (8 channels)
D-A conversion		5-bitX1
Pulse width modulator		8-bitX1
Watchdog timer		15-bitX1
Subroutine nesting		80 levels (max)
Interrupt		Two external interrupts, three internal timer interrupts
Clock generating circuit		built-in (ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 5%
Power dissipation		15mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage	12V (Ports P0, P1, P3, P4, P5, P6, P7, INT ₁)
	Output current	5mA (Ports P0, P1, P2, P3, P4, P7)
Memory expansion		Possible
Operating temperature range		-10~70°C
Device structure		CMOS silicon gate process
Package		72-pin plastic molded QFP

Note 1 : The PROM programing voltage is 21V (equivalent to the M5L27128)

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Single-chip /EPROM	Power supply		Supply 5V±5% to V _{CC} and 0V to V _{SS}
CNV _{SS} / V _{PP}	Single-chip	CNV _{SS} input	Input	Connect to 0V
	EPROM	V _{PP} input		Connect to V _{PP} when programming or verifying.
RESET	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V _{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	RESET input		Connect to V _{SS}
X _{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X _{IN} and X _{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X _{IN} pin and open the X _{OUT} pin.
X _{OUT}		Clock output	Output	
φ	Single-chip /EPROM	Timing output	Output	For timing output
INT ₁	Single-chip	Interrupt input	Input	Interrupt input INT ₁ .
	EPROM	Interrupt input	Input	Connect to 0V.
P0 ₀ ~P0 ₇	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction registers which can program each bit as input or output. It is set to input mode at reset. The output format is N-ch open drain.
	EPROM	Address input A ₀ ~A ₇	Input	P0 works as the lower 8 bit address input (A ₀ ~A ₇).
P1 ₀ ~P1 ₇	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Address input A ₈ ~A ₁₃	Input	P1 ₀ ~P1 ₄ works as the higher 5 bit address inputs (A ₈ ~A ₁₃). Connect P1 ₅ ~P1 ₇ to V _{CC} .
P2 ₀ ~P2 ₇	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port which has the same function as port P0. The output format is CMOS.
	EPROM	Data input/ output D ₀ ~D ₇	I/O	Port 2 works as an 8 bit data bus (D ₀ ~D ₇).
P3 ₀ ~P3 ₇	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions port P0. When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as S _{ADP} , CLK, S _{OUT} , and S _{IN} pins, respectively. Also P3 ₃ and P3 ₂ work as CNTR pin and the lowest interrupt pin (INT ₂), respectively. The output format is N-ch open drain.
	EPROM	Input Port P3	Input	Connect to 0V.
P4 ₀ ~P4 ₇	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port which has the same function as port P0. Ports P4 ₇ ~P4 ₀ are common with Analog inputs AN ₇ ~AN ₀ . The output format is N-ch open drain.
	EPROM	Select mode	Input	P4 ₂ , P4 ₁ , P4 ₀ work as CE, OE and PGM inputs, respectively. Connect P4 ₅ ~P4 ₇ to 0V and P4 ₄ and P4 ₃ to V _{CC} .
P5 ₀ ~P5 ₇	Single-chip	Input port	Input	Port P5 is an 8-bit input port. Ports P5 ₇ ~P5 ₄ have edge sense functions.
	EPROM	Input port	Input	Connect to 0V.

PROM VERSION of M37412M4-XXXFP

PIN DESCRIPTION (Continued)

Pin	Mode	Name	Input/ Output	Functions
P6 ₀ ~P6 ₄	Single-chip	Output port	Output	Port P6 is an 5-bit output port. At external trigger output mode, P6 ₀ and P6 ₁ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain.
	EPROM	Output port	Output	Connect to 0V.
P7 ₀ ~P7 ₅	Single-chip	I/O port P7	I/O	Port P7 is an 6-bit I/O port which has the same function as Port P0.
	EPROM	Input port P7	Input	Connect to 0V.
AV _{SS}	Single-chip	Analog voltage input	Input	GND pin for the A-D and D-A converters.
	EPROM	Analog voltage input	Input	Connect to 0V.
V _{REF}	Single-chip	Reference voltage input	Input	Reference input for A-D and D-A converters.
	EPROM	Reference voltage input	Input	Connect to 0V.
D-A	Single-chip	D-A output	Output	D-A converter output pin
	EPROM	D-A output	Output	Connect to 0V.
PWM	Single-chip	PWM output	Output	Pulse width modulation output pin (N-ch open drain format).
	EPROM	PWM output	Output	Connect to 0V.

PROM VERSION of M37412M4-XXXFP

EPROM MODE

The M37412E5-XXXFP features an EPROM mode in addition to its normal modes. When the RESET signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 gives the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, P4₀~P4₂, and CNV_{SS} are used for the PROM (equivalent to the M5L27128). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37412E5-XXXFP	M5L27128
V _{CC}	V _{CC}	V _{CC}
V _{PP}	CNV _{SS} /V _{PP}	V _{PP}
V _{SS}	V _{SS}	V _{SS}
Address input	Ports P0, P1 ₀ ~P1 ₅	A ₀ ~A ₁₃
Data I/O	Port P2	D ₀ ~D ₇
CE	P4 ₂ /CE	CE
OE	P4 ₁ /OE	OE
PGM	P4 ₀ /PGM	PGM

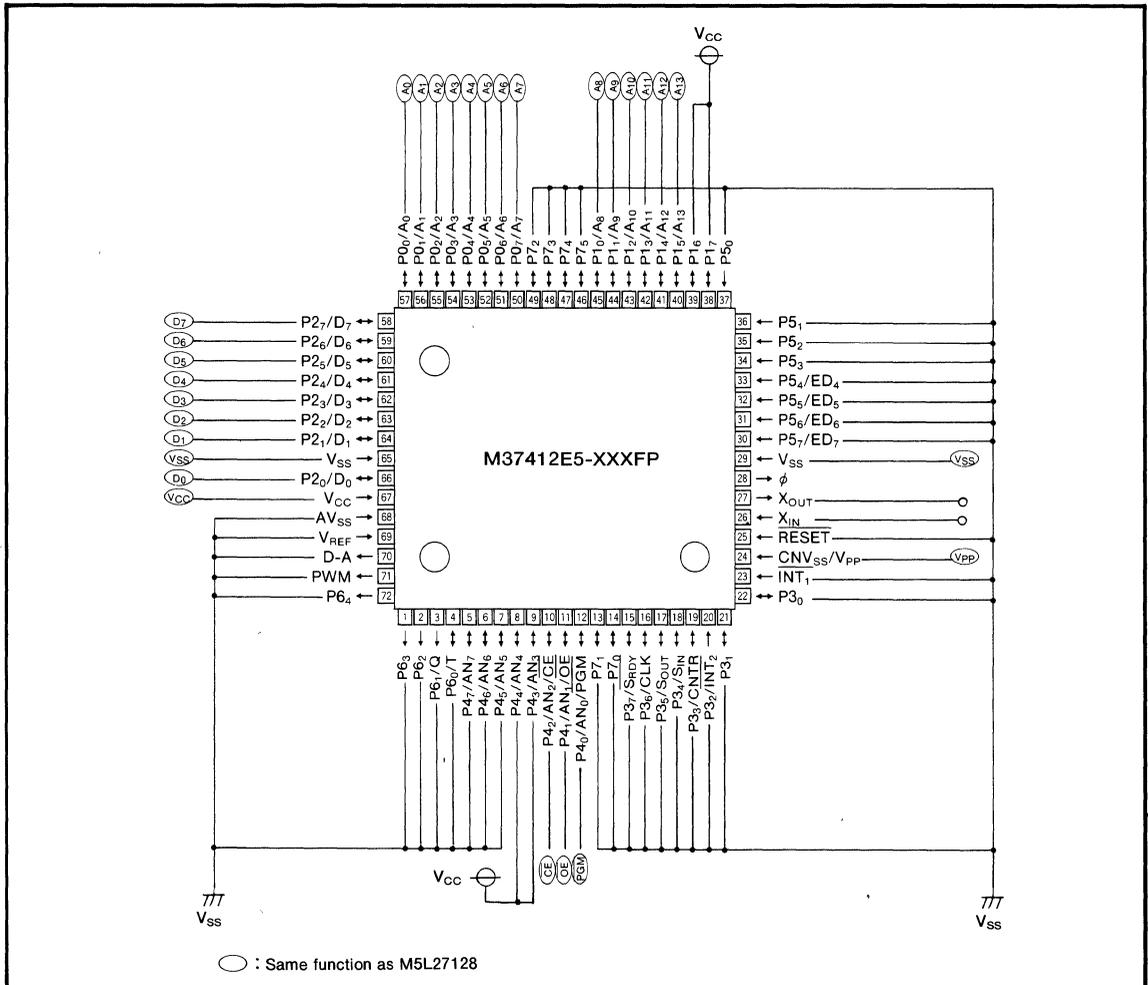


Fig.1 Pin connection in EPROM mode

PROM VERSION of M37412M4-XXXFP

PROM READING AND WRITING

Reading

To read the PROM, set the \overline{CE} and \overline{OE} pins to a "L" level, and the PGM pin to a "H" level. Input the address of the data ($A_0 \sim A_{13}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the \overline{CE} or \overline{OE} pins are in the "H" state.

Writing

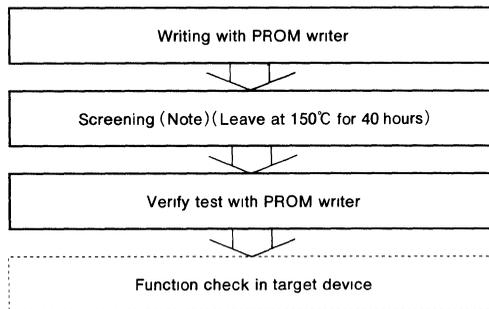
To write to the PROM, set the \overline{CE} pin to a "L" level and the \overline{OE} pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{13}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the PGM pin to a "L" level to begin writing.

Notes on Writing

When using an PROM writer, the address range should be between 1800_{16} and $3FFF_{16}$. When data is written between addresses 0000_{16} and $3FFF_{16}$, fill addresses 0000_{16} to $17FF_{16}$ with 00_{16} .

NOTES ON HANDLING

- (1) Since a high voltage (21V) is used to write data, care should be taken when turning on the EPROM writer's power.
- (2) For the programmable microcomputer (shipped in blank or OTP type). Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150°C exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}(10)$	$\overline{OE}(11)$	PGM(12)	$V_{PP}(24)$	$V_{CC}(67)$	Data I/O (58~64, 66)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse ($V_{IH} \rightarrow V_{IL}$)	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the output transistor cut-off	-0.3~7	V
V_I	Input voltage X_{IN}		-0.3~7	V
V_I	Input voltage $P2_0\sim P2_7, P4_0\sim P4_7$		$-0.3\sim V_{CC}+0.3$	V
V_I	Input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P3_0\sim P3_7, P5_0\sim P5_7, P6_0, P7_0\sim P7_5, INT_1$		-0.3~13	V
V_I	Input voltage $CNV_{SS}, RESET$		-0.3~13 (Note 1)	V
V_O	Output voltage $P2_0\sim P2_7, P4_0\sim P4_7, X_{OUT}, \phi, D-A$		$-0.3\sim V_{CC}+0.3$	V
V_O	Output voltage $P0_0\sim P0_7, P1_0\sim P1_7, P3_0\sim P3_7, P6_0\sim P6_4, P7_0\sim P7_5, PWM$		-0.3~13	V
P_d	Power dissipation	$T_a=25^\circ C$	300	mW
T_{opr}	Operating temperature		-10~70	$^\circ C$
T_{stg}	Storage temperature		-40~125	$^\circ C$

Note 1 : In EPROM programming mode, CNV_{SS} is 22.0V

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V\pm 5\%$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7, INT_1, RESET, X_{IN}, CNV_{SS}, P6_0, P7_0\sim P7_5$	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7, INT_1, CNV_{SS}, P6_0, P7_0\sim P7_5$	0		$0.2V_{CC}$	V
V_{iL}	"L" input voltage RESET	0		$0.12V_{CC}$	V
V_{iL}	"L" input voltage X_{IN}	0		$0.16V_{CC}$	V
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7, P4_0\sim P4_7, P7_0\sim P7_5$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0\sim P6_3$ (Note 2)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM, $P6_4$ (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7, P3_0\sim P3_7, P4_0\sim P4_7, P7_0\sim P7_5$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0\sim P6_3$ (Note 1)			7	mA
$I_{OL(avg)}$	"L" average output current PWM, $P6_4$ (Note 1)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0\sim P2_7$ (Note 2)			-10	mA
$I_{OH(avg)}$	"H" average output current $P2_0\sim P2_7$ (Note 1)			-5	mA
$f(X_{IN})$	Internal clock oscillating frequency			4	MHz

- Note 1 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
 2 : Do not allow the combined low- level output current of ports P0, P1, P2, P3, P4, P6, and PWM to exceed 80mA
 Do not allow the combined high- level output current of port P2 to exceed 50mA
 3 : "H" input voltage of ports P0, P1, P3, P5, P6, P7 and INT_1 is available up to +12V

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
V_{OH}	"H" output voltage $P_{20}\sim P_{27}$	$I_{OH}=-10mA$	3			V
V_{OH}	"H" output voltage ϕ	$I_{OH}=-2.5mA$	3			V
V_{OL}	"L" output voltage $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$, $P_{40}\sim P_{47}$, $P_{60}\sim P_{63}$, $P_{70}\sim P_{75}$	$I_{OL}=10mA$			2	V
V_{OL}	"L" output voltage P_{64} , ϕ , PWM	$I_{OL}=5mA$			2	V
$V_{T+}-V_{T-}$	Hysteresis INT_1		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$	When used as INT_2 input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $P6_0$	When used as T input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $RESET$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{20}\sim P_{27}$, $P_{30}\sim P_{37}$, $P_{40}\sim P_{47}$, $P_{50}\sim P_{57}$, $P_{60}\sim P_{63}$, $P_{70}\sim P_{75}$	$V_i=0V$			-5	μA
I_{IL}	"L" input current INT_1 , $RESET$, X_{IN}	$V_i=0V$			-5	μA
I_{IH}	"H" input current $P_{00}\sim P_{07}$, $P_{10}\sim P_{17}$, $P_{30}\sim P_{37}$, $P_{50}\sim P_{57}$, P_{60} , $P_{70}\sim P_{75}$	$V_i=12V$			12	μA
I_{IH}	"H" input current INT_1 , $RESET$, X_{IN} , $P_{20}\sim P_{27}$, $P_{40}\sim P_{47}$	$V_i=5V$			5	μA
V_{RAM}	RAM retention voltage	At clock stop	2			V
I_{CC}	Supply current	ϕ , X_{OUT} , and D-A pins opened, other pins at V_{SS} , and A-D converter in the finished condition	$f(X_{IN})=4MHz$ Square wave	3	6	μA
			At clock stop $T_a=25^\circ C$		1	
			At clock stop $T_a=75^\circ C$		10	

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistance value	$V_{REF}=V_{CC}$	2		10	$k\Omega$
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			5	Bits
—	Error in full scale range	$V_{REF}=V_{CC}$			± 1	%
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
R_O	Output resistance	$V_{REF}=V_{CC}$			3	$k\Omega$
V_{REF}	Reference voltage		4		V_{CC}	V

TIMING REQUIREMENTS

Single-chip mode ($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
$t_{SU}(P0D-\phi)$	Port P0 input setup time		270			ns
$t_{SU}(P1D-\phi)$	Port P1 input setup time		270			ns
$t_{SU}(P2D-\phi)$	Port P2 input setup time		270			ns
$t_{SU}(P3D-\phi)$	Port P3 input setup time		270			ns
$t_{SU}(P4D-\phi)$	Port P4 input setup time		270			ns
$t_{SU}(P5D-\phi)$	Port P5 input setup time		270			ns
$t_{SU}(P7D-\phi)$	Port P7 input setup time		270			ns
$t_H(\phi-P0D)$	Port P0 input hold time		20			ns
$t_H(\phi-P1D)$	Port P1 input hold time		20			ns
$t_H(\phi-P2D)$	Port P2 input hold time		20			ns
$t_H(\phi-P3D)$	Port P3 input hold time		20			ns
$t_H(\phi-P4D)$	Port P4 input hold time		20			ns
$t_H(\phi-P5D)$	Port P5 input hold time		20			ns
$t_H(\phi-P7D)$	Port P7 input hold time		20			ns
t_C	External clock input cycle time		250			ns
t_W	External clock input pulse width		75			ns
t_r	External clock rising edge time				25	ns
t_f	External clock falling edge time				25	ns

Eva-chip mode ($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
$t_{SU}(P0D-\phi)$	Port P0 input setup time		270			ns
$t_{SU}(P1D-\phi)$	Port P1 input setup time		270			ns
$t_{SU}(P2D-\phi)$	Port P2 input setup time		270			ns
$t_H(\phi-P0D)$	Port P0 input hold time		20			ns
$t_H(\phi-P1D)$	Port P1 input hold time		20			ns
$t_H(\phi-P2D)$	Port P2 input hold time		20			ns

Memory expanding mode and microprocessor mode

($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max.	
$t_{SU}(P2D-\phi)$	Port P2 input setup time		270			ns
$t_H(\phi-P2D)$	Port P2 input hold time		30			ns

SWITCHING CHARACTERISTICS

Single-chip mode ($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_d(\phi-P0Q)$	Port P0 data output delay time	Fig 2			230	ns
$t_d(\phi-P1Q)$	Port P1 data output delay time				230	ns
$t_d(\phi-P2Q)$	Port P2 data output delay time		Fig 3			230
$t_d(\phi-P3Q)$	Port P3 data output delay time				230	ns
$t_d(\phi-P4Q)$	Port P4 data output delay time	Fig 2			230	ns
$t_d(\phi-P6Q)$	Port P6 data output delay time				230	ns
$t_d(\phi-P7Q)$	Port P7 data output delay time				230	ns

Eva-chip mode ($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
$t_d(\phi-P0A)$	Port P0 address output delay time	Fig 2			250	ns	
$t_d(\phi-P0AF)$	Port P0 address output delay time				250	ns	
$t_d(\phi-P0Q)$	Port P0 data output delay time				200	ns	
$t_d(\phi-P0QF)$	Port P0 data output delay time				200	ns	
$t_d(\phi-P1A)$	Port P1 address output delay time				250	ns	
$t_d(\phi-P1AF)$	Port P1 address output delay time				250	ns	
$t_d(\phi-P1Q)$	Port P1 data output delay time				200	ns	
$t_d(\phi-P1QF)$	Port P1 data output delay time				200	ns	
$t_d(\phi-P2Q)$	Port P2 data output delay time		Fig 3			300	ns
$t_d(\phi-P2QF)$	Port P2 data output delay time					300	ns
$t_d(\phi-R/W)$	R/W signal output delay time	Fig 2			250	ns	
$t_d(\phi-R/WF)$	R/W signal output delay time				250	ns	
$t_d(\phi-P3Q)$	Port P3 ₀ data output delay time				200	ns	
$t_d(\phi-P3QF)$	Port P3 ₀ data output delay time				200	ns	
$t_d(\phi-SYNC)$	SYNC signal output delay time				250	ns	
$t_d(\phi-SYNCF)$	SYNC signal output delay time				250	ns	
$t_d(\phi-P31Q)$	Port P3 ₁ data output delay time				200	ns	
$t_d(\phi-P31QF)$	Port P3 ₁ data output delay time				200	ns	

Memory expanding mode and microprocessor mode

($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
$t_d(\phi-P0A)$	Port P0 address output delay time	Fig. 2			250	ns
$t_d(\phi-P1A)$	Port P1 address output delay time				250	ns
$t_d(\phi-P2Q)$	Port P2 data output delay time	Fig 3			300	ns
$t_d(\phi-P2QF)$	Port P2 data output delay time				300	ns
$t_d(\phi-R/W)$	R/W signal output delay time	Fig 2			250	ns
$t_d(\phi-SYNC)$	SYNC signal output delay time				250	ns

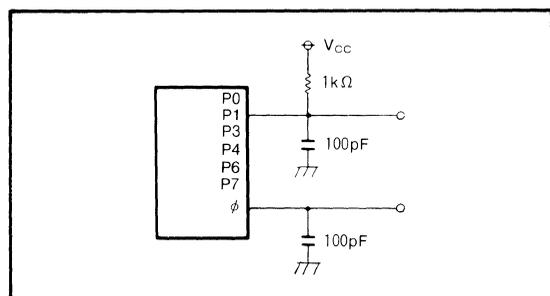


Fig. 2 Ports P0, P1, P3, P4, P6 and P7 test circuit

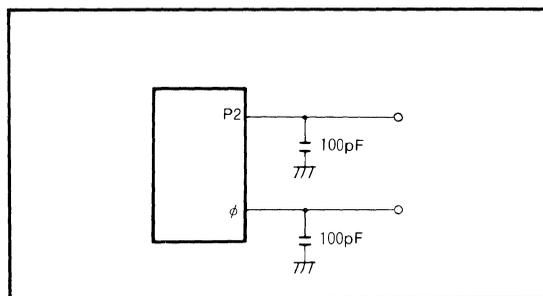
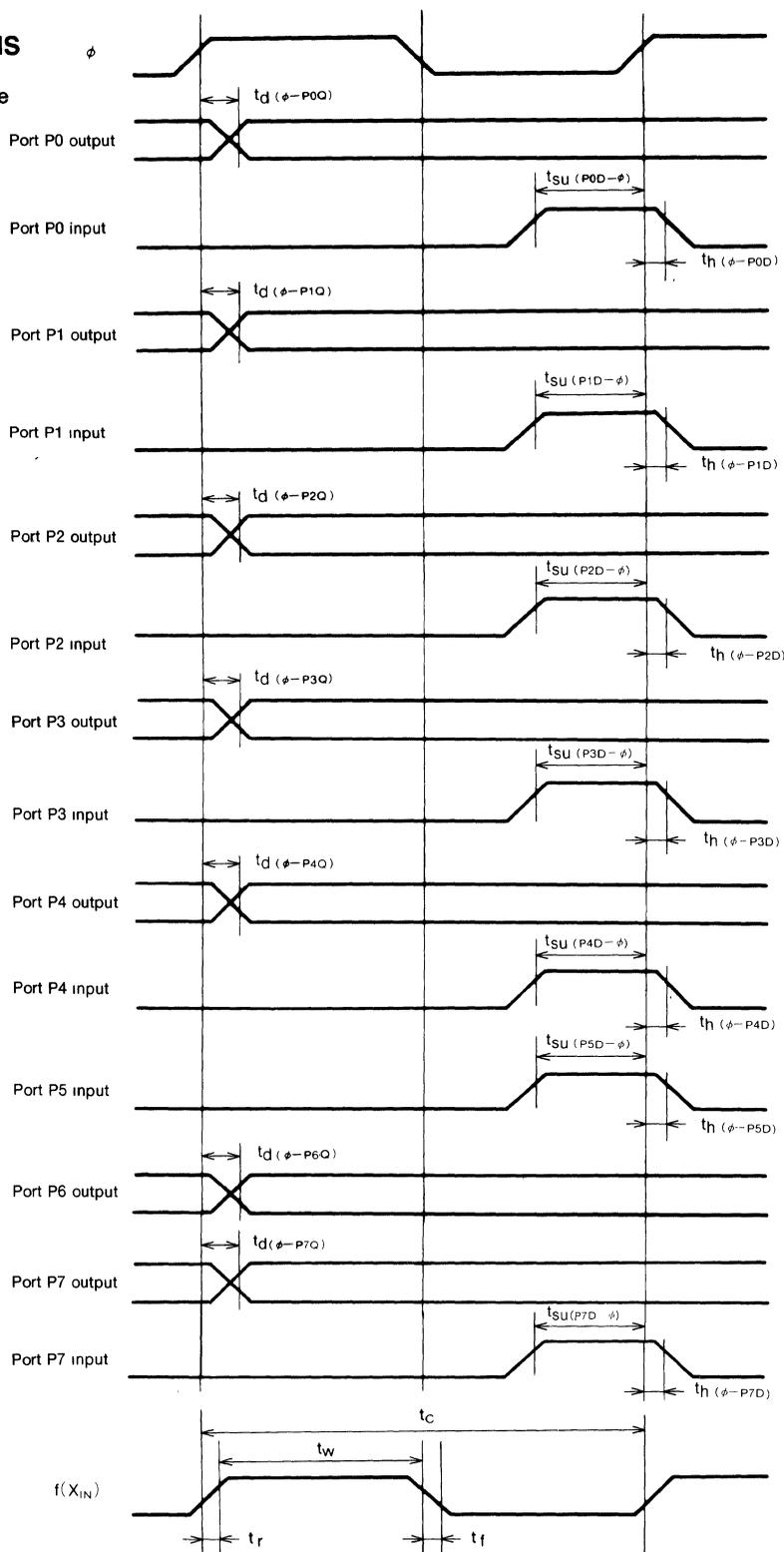


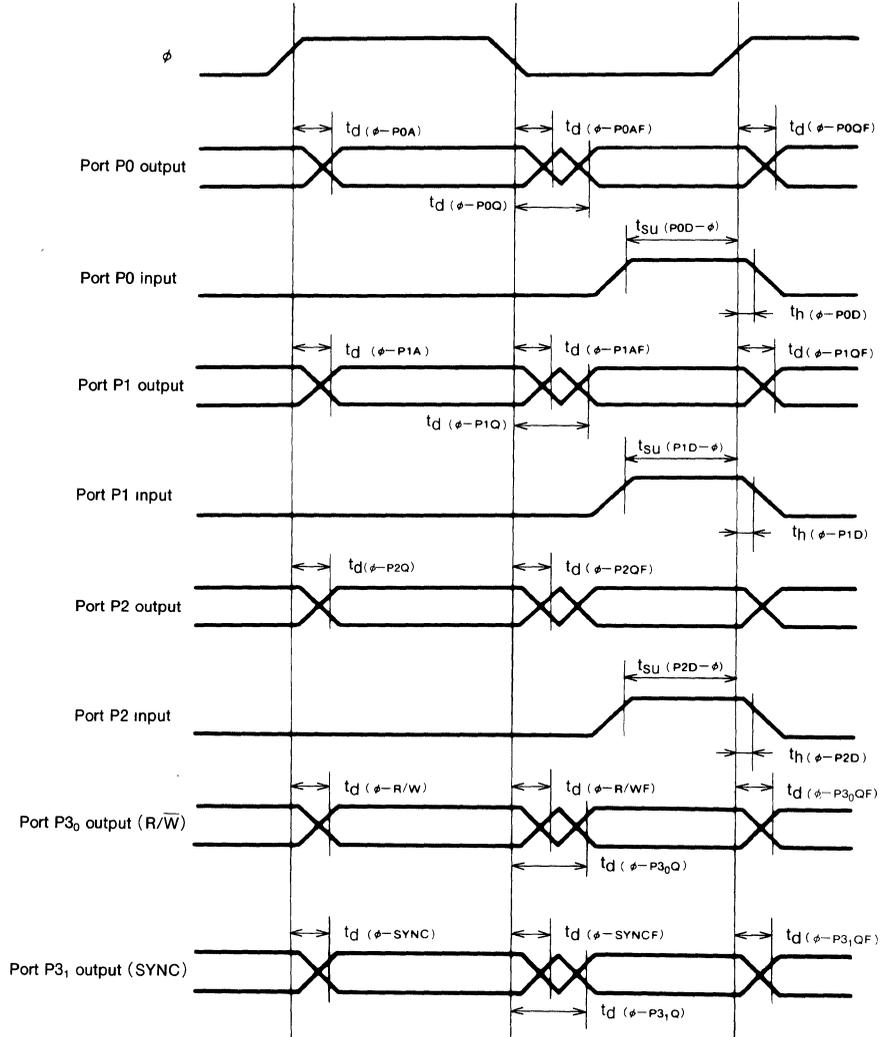
Fig. 3 Port P2 test circuit

TIMING DIAGRAMS

In single-chip mode

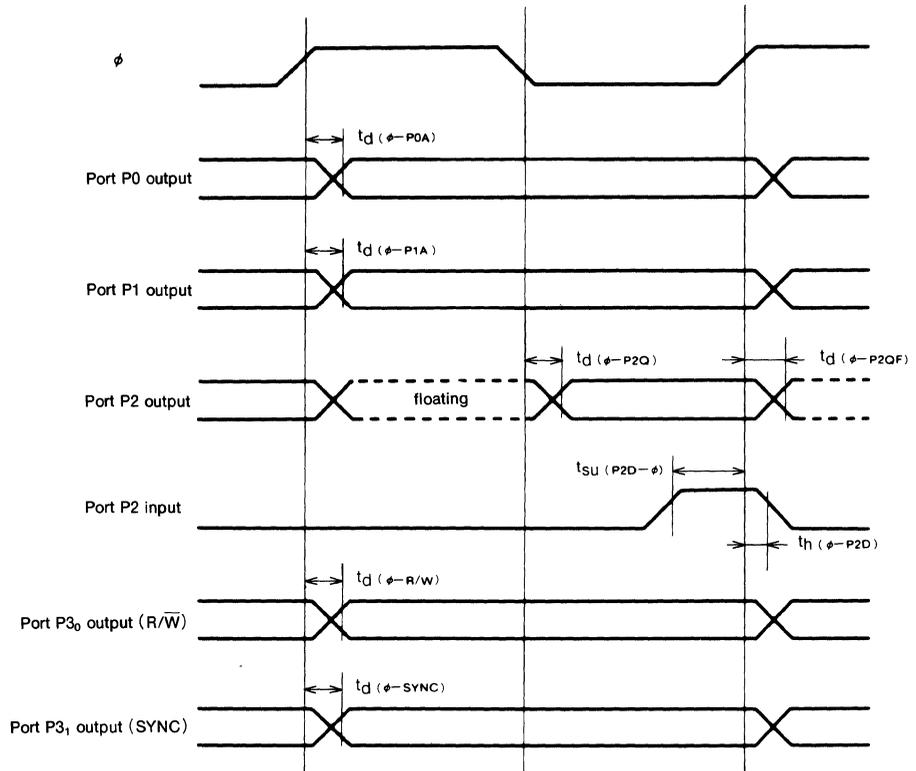


In eva-chip mode



PROM VERSION of M37412M4-XXXFP

In memory expanding mode and microprocessor mode



PRELIMINARY

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MITSUBISHI MICROCOMPUTERS

MITSUBISHI MICROCOMPUTERS
M37413E6HXXFP
M37413E6HFS
 PROM VERSION of M37413M6HXXFP

DESCRIPTION

The M37413E6HFS, M37413E6HXXFP are single-chip microcomputers designed with CMOS silicon gate technology. M37413E6HXXFP is housed in a 80-pin shrink plastic molded QFP. M37413E6HFS is housed in a 80-pin ceramic QFP. The features of this chip are similar to those of the M37413M4HXXFP except that this chip has a 12288 bytes PROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

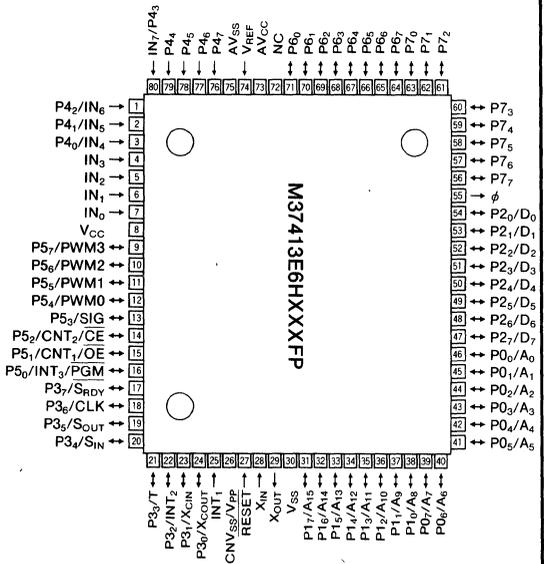
In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The M37413E6HFS is the window type. The differences between the M37413E6HXXFP and the M37413E6HFS are the package outline and the power dissipation ability (absolute maximum ratings).

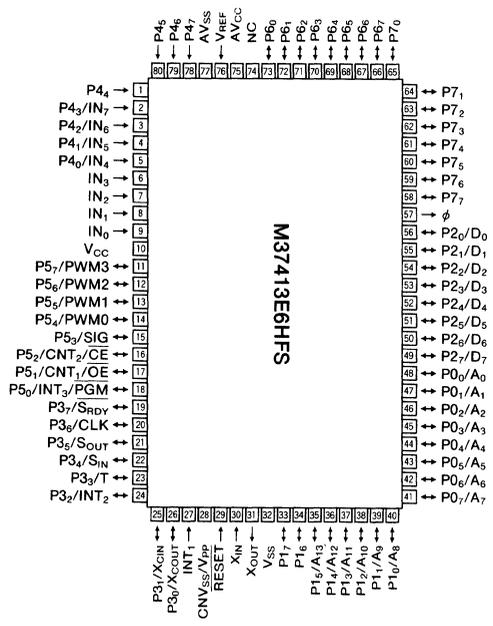
FEATURES

- Number of basic instructions..... 69
- Memory size PROM 12288 bytes
RAM..... 256 bytes
- Instruction execution time
(minimum instructions at 4MHz frequency)
at high-speed mode 2μs
at low-speed mode 8μs
- Single power supply
M37413E6HXXFP 2.5~5.5V
M37413E6HFS 4.5~5.5V
- Power dissipation
normal operation mode (at 4MHz frequency)
..... 15mW (V_{CC}=5V, Typ.)
low-speed operation mode (at 32kHz frequency for
clock function)..... 54μW (V_{CC}=3V, Typ.)
- RAM retention voltage (stop mode)
..... 2.0V ≤ V_{RAM} ≤ 5.5V
- Subroutine nesting 96 levels (Max.)
- Interrupt 10 types, 5 vectors
- 8-bit timer 4 (3 when used as serial I/O)
- 16-bit timer 1
- Programmable I/O ports
(Ports P0, P1, P2, P3, P5, P6, P7)..... 56
- Input port (Port P4) 8
- Serial I/O (8-bit) 1
- A-D converter 8-bit, 8-channel
conversion speed (49.5μs)
- Two clock generating circuits
(One is for main clock, the other is for clock function)
- PROM (equivalent to the M5L27128)
program voltage 21V

PIN CONFIGURATION (TOP VIEW)



Outline 80P6S (OTP)



Outline 80S6 (Window)

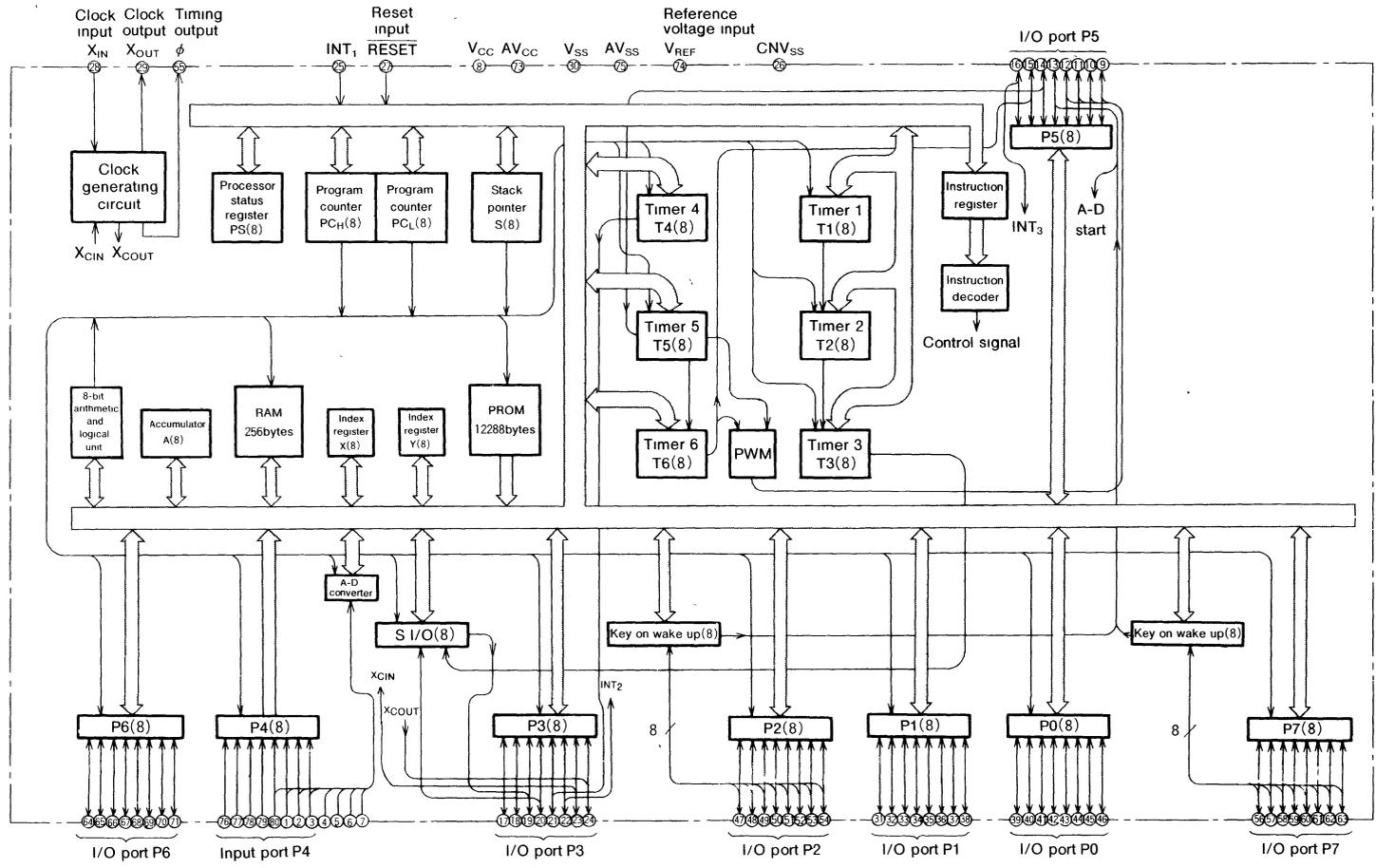
NC : No Connection

APPLICATION

- Audio-visual equipment, VCR, Tuner,
- Office automation equipment,
- Camera



M37413E6HXXXFP BLOCK DIAGRAM



PROM VERSION of M37413M6HXXXFP

MITSUBISHI MICROCOMPUTERS
M37413E6HXXXFP
M37413E6HFS

FUNCTIONS OF M37413E6HXXXFP

Parameters			Functions
Number of basic instructions			69
Instruction execution time			·2 μ s (minimum instructions, at 4MHz of frequency)
Clock frequency			4MHz
Memory size	PROM		12288bytes
	RAM		256bytes
Input/Output port	P0, P2, P7	I/O	8-bitX3 (CMOS output)
	P1, P3, P5, P6	I/O	8-bitX4 (N-channel open drain output)
	P4	Input	8-bitX1
Serial I/O			8-bitX1
Timers			8-bit timerX4 16-bit timerX1
Subroutine nesting			96(max)
Interrupt			Three external interrupts, three timer interrupts (or two timer, one serial I/O)
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator)
Operating temperature range			-10~70°C
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Single-chip /EPROM	Power supply		Supply 5V±5% to V _{CC} and 0V to V _{SS}
CNV _{SS} / V _{PP}	Single-chip	CNV _{SS}		Connect to V _{SS} .
	EPROM	V _{PP} input	Input	Connect to V _{PP} when programming or verifying
<u>RESET</u>	Single-chip	Reset input	Input	To reset, keep this input terminal low for more than 16μs (min) under normal V _{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM			Connect to 0V.
X _{IN}	Single-chip /EPROM	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected to the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}		Clock output	Output	
INT ₁	Single-chip	Interrupt input	Input	This is the highest order interrupt input pin.
	EPROM			Connect to 0V.
P0 ₀ ~P0 ₇	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
	EPROM	Address input A ₀ ~A ₇	Input	P0 works as the lower 8 bit address input (A ₀ ~A ₇).
P1 ₀ ~P1 ₇	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open drain.
	EPROM	Address input A ₈ ~A ₁₃	Input	P1 ₀ ~P1 ₅ works as the higher 6 bit address inputs (A ₈ ~A ₁₃). Connect P1 ₆ ~P1 ₇ to V _{SS} .
P2 ₀ ~P2 ₇	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as port P0. Also all bits are for key on wake up input pins.
	EPROM	Data input/ output D ₀ ~D ₇	I/O	Port P2 works as an 8 bit data bus (D ₀ ~D ₇).
P3 ₀ ~P3 ₇	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ and P3 ₄ work as <u>S_{RDY}</u> , CLK, S _{OUT} , and S _{IN} pins, respectively. Also P3 ₃ , P3 ₂ , P3 ₁ , and P3 ₀ work as timer 4 overflow signal divided by 2 output pin (T), INT ₂ pin, X _{CIN} and X _{COUT} pins, respectively.
	EPROM	Input port P3	Input	Connect to 0V.
P4 ₀ ~P4 ₇	Single-chip	Input port P4	Input	Port P4 is an 8-bit input port. P4 ₆ ~P4 ₃ work as analog input pin IN ₄ ~IN ₇ .
	EPROM			Connect to V _{SS} .
IN ₀ ~IN ₇	Single-chip	Input port IN	Input	These are analog input pin.
	EPROM			Connect to V _{SS} .
P5 ₀ ~P5 ₇	Single-chip	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P1. P5 ₀ , P5 ₁ , P5 ₂ and P5 ₃ are in common with INT ₃ , timer3 input, timer5 input and A-D trigger input, respectively.
	EPROM	Select mode	Input	Connect to V _{SS} .

PIN DESCRIPTION (Continued)

Pin	Mode	Name	Input/ Output	Functions
P6 ₀ ~P6 ₇	Single-chip	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P1
	EPROM	Input port P6	Input	Connect to V _{SS}
P7 ₀ ~P7 ₇	Single-chip	I/O port P7	I/O	Port P7 is an 8-bit I/O port and has basically the same functions as port P2
	EPROM	Input port P7	Input	Connect to V _{SS}
AV _{CC}	Single-chip	Analog voltage input	Input	Analog voltage input pin for A-D converter
	EPROM			Connect to V _{SS} .
AV _{SS}	Single-chip /EPROM	Analog voltage input	Input	Connect to V _{SS} .
V _{REF}	Single-chip	Reference voltage input	Input	Reference input pin for A-D converter.
	EPROM			Connect to V _{CC} .

MITSUBISHI MICROCOMPUTERS
M37413E6HXXXFP
M37413E6HFS

PROM VERSION of M37413M6HXXXFP

EPROM MODE

The M37413E6HXXXFP, M37413E6HFS feature an EPROM mode in addition to its normal modes. When the RESET signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1, Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, P5₀ ~ P5₂, and CNV_{SS} are used for the PROM (equivalent to the M5L27128). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37413E6HXXXFP, M37413E6HFS	M5L27128
V _{CC}	V _{CC}	V _{CC}
V _{PP}	CNV _{SS} /V _{PP}	V _{PP}
V _{SS}	V _{SS}	V _{SS}
Address input	Ports P0, P1 ₀ ~P1 ₅	A ₀ ~A ₁₃
Data I/O	Port P2	D ₀ ~D ₇
CE	P5 ₂ /CE	CE
OE	P5 ₁ /OE	OE
PGM	P5 ₀ /PGM	PGM

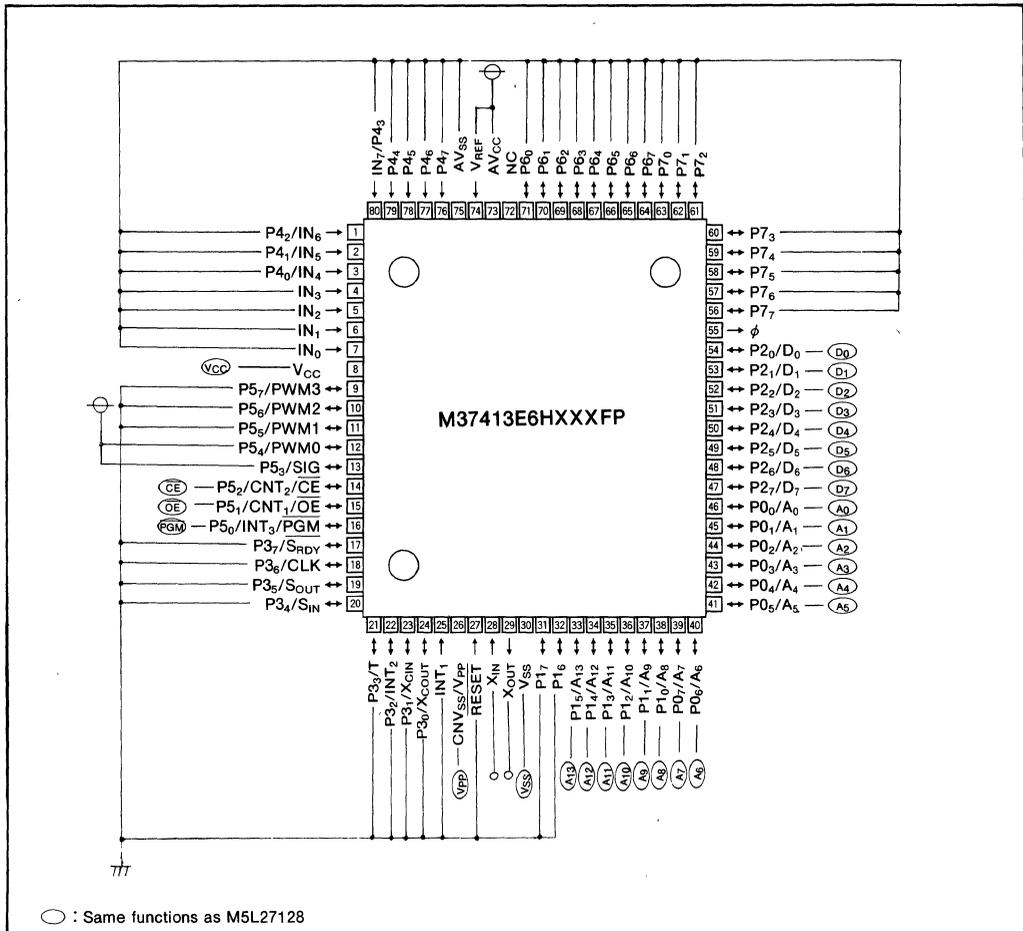


Fig.1 Pin connection in EPROM mode

M37413E6HXXFP
M37413E6HFS

PROM VERSION of M37413M6HXXFP

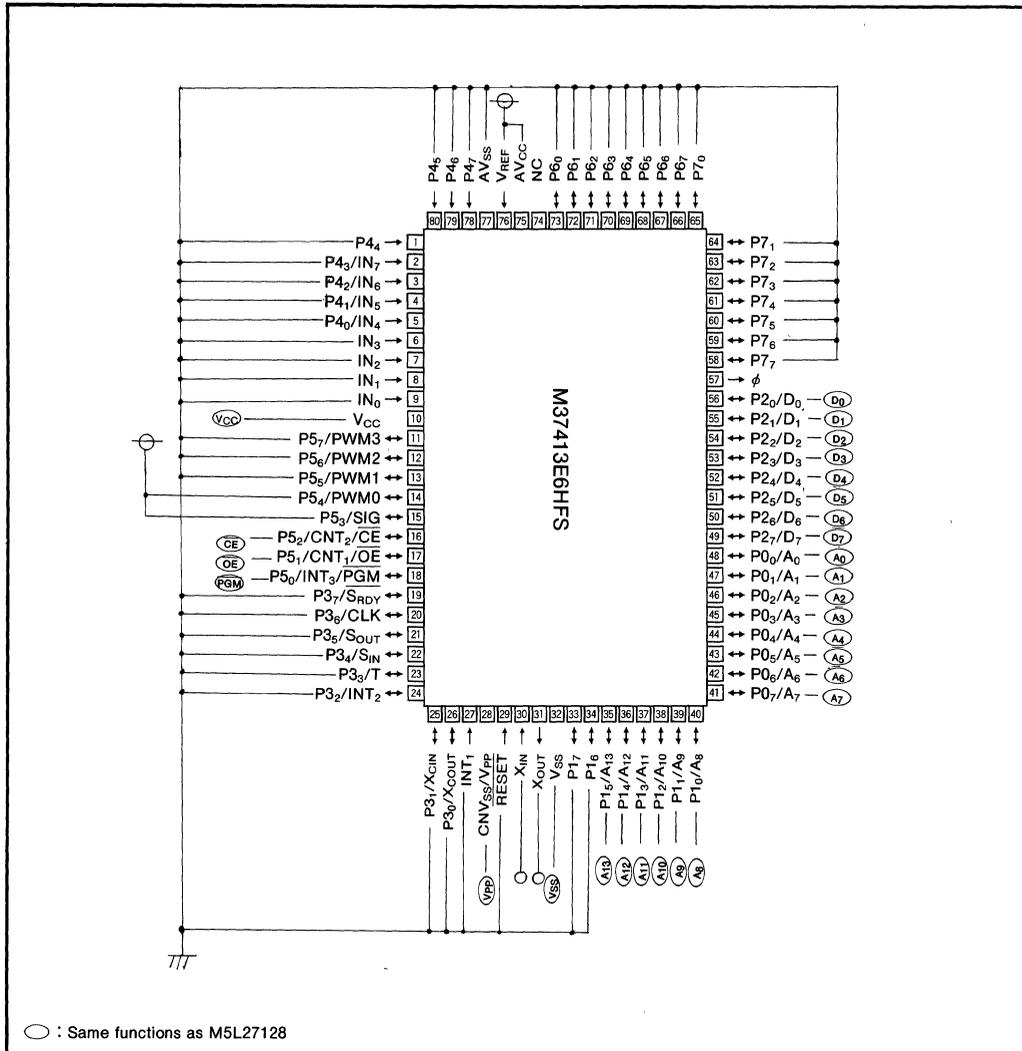


Fig.2 Pin connection in EPROM mode

MITSUBISHI MICROCOMPUTERS

M37413E6HXXXFP

M37413E6HFS

PROM VERSION of M37413M6HXXXFP

PROM READING, WRITING AND ERASING

Reading

To read the PROM, set the \overline{CE} and \overline{OE} pins to a "L" level, and the PGM pin to a "H" level. Input the address of the data ($A_0 \sim A_{13}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the \overline{CE} or \overline{OE} pins are in the "H" state.

Writing

To write to the PROM, set the \overline{CE} pin to a "L" level and the \overline{OE} pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{13}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the PGM pin to a "L" level to begin writing.

Erasing

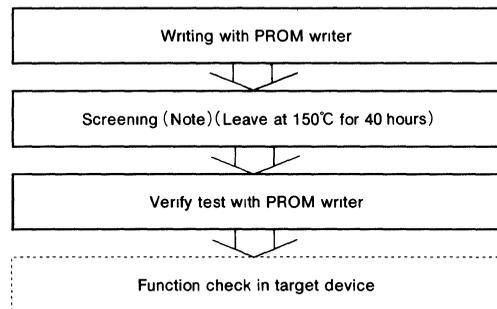
Data can only be erased on the M37413E6HFS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is $15W \cdot s/cm^2$.

Functional differences from M37413M4HXXXFP (excluding characteristic differences).

	M37413M4HXXXFP	M37413E6HXXXFP
Port P0 pull-up resistor	Option	Not provided
Port P1 pull-up resistor	Option	Not provided
Port P2 pull-up resistor	Option	Not provided
Port P3 pull-up resistor	Option	Not provided
Port P4 pull-up resistor	Option	Not provided
Port P5 pull-up resistor	Option	Not provided
Port P6 pull-up resistor	Option	Not provided
Port P7 pull-up resistor	Option	Not provided
Port P2 key on wake up	Option	Provided (all bits)
Port P7 key on wake up	Option	Provided (all bits)

NOTES ON HANDLING

- (1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.
- (2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.
- (3) Since a high voltage (21V) is used to write data, care should be taken when turning on the PROM writer's power.
- (4) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150°C exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	\overline{CE} (14)	\overline{OE} (15)	PGM(16)	V_{PP} (26)	V_{CC} (8)	Data I/O (33~54)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse($V_{IH} \rightarrow V_{IL}$)	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
 2 : An X indicates either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~7	V
AV _{CC}	Analog supply voltage	V _{CC} =AV _{CC}	-0.3~7	V
V _I	Input voltage P ₀ ~P ₀₇ , P ₂ ₀ ~P ₂₇ , P ₃ ₀ , P ₃ ₁ , P ₄ ₀ ~P ₄₇ , P ₇ ₀ ~P ₇₇ , I _N ₀ ~I _{N7} , V _{REF} , X _{IN}		-0.3~V _{CC} +0.3	V
V _I	Input voltage CNV _{SS} , (Note 1)		-0.3~7	V
V _I	Input voltage I _N ₁ , RESET, P ₁ ₀ ~P ₁₇ , P ₃ ₂ ~P ₃₇ , P ₅ ₀ ~P ₅₇ , P ₆ ₀ ~P ₆₇		-0.3~10	V
V _O	Output voltage P ₀ ₀ ~P ₀₇ , P ₂ ₀ ~P ₂₇ , P ₃ ₀ , P ₃ ₁ , P ₇ ₀ ~P ₇₇ , X _{OUT}		-0.3~V _{CC} +0.3	V
V _O	Output voltage P ₁ ₀ ~P ₁₇ , P ₃ ₂ ~P ₃₇ , P ₅ ₀ ~P ₅₇ , P ₆ ₀ ~P ₆₇		-0.3~10	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

Note 1 : In PROM programming mode, CNV_{SS} is 21.0V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=-10~70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ	Max	
V _{CC}	Supply voltage (Note 1)	f(X _{IN})=4MHz High-speed mode	4.5		5.5	V
		f(X _{IN})=4MHz Normal mode or f(X _{IN})=2MHz High-speed mode (Note 2)	2.5 (Note 3)		5.5	
V _{SS}	Supply voltage			0		V
V _{IH}	"H" input voltage P ₀ ₀ ~P ₀₇ , P ₃ ₀ , P ₃ ₁ , P ₄ ₀ ~P ₄₇ , X _{IN} , CNV _{SS} (Note 4)		0.7V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₂ ₀ ~P ₂₇ , P ₇ ₀ ~P ₇₇		0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₁ ₀ ~P ₁₇ , P ₅ ₁ ~P ₅₇ , P ₆ ₀ ~P ₆₇ , S _{IN}		0.7V _{CC}		10	V
V _{IH}	"H" input voltage P ₅ ₀ , I _N ₁ , I _N ₂ , I _N ₃ , P ₃ ₂ ~P ₃₇ , CNT ₁ , CNT ₂ , SIG, CLK		0.8V _{CC}		10	V
V _{IH}	"H" input voltage RESET, X _{CIN}		0.85V _{CC}		10	V
V _{IL}	"L" input voltage P ₀ ₀ ~P ₀₇ , P ₁ ₀ ~P ₁₇ , P ₃ ₀ ~P ₃₇ , P ₄ ₀ ~P ₄₇ , P ₅ ₁ ~P ₅₇ , P ₆ ₀ ~P ₆₇ , S _{IN}		0		0.3V _{CC}	V
V _{IL}	"L" input voltage P ₂ ₀ ~P ₂₇ , P ₅ ₀ , P ₇ ₀ ~P ₇₇ , I _N ₁ , I _N ₂ , I _N ₃ , CNT ₁ , CNT ₂ , SIG, CLK		0		0.2V _{CC}	V
V _{IL}	"L" input voltage RESET, X _{IN} , X _{CIN}		0		0.15V _{CC}	V
I _{OH}	"H" output current P ₀ ₀ ~P ₀₇ , P ₂ ₀ ~P ₂₇ , P ₇ ₀ ~P ₇₇ , X _{OUT} (Note 5)				-1	mA
I _{OL}	"L" output current P ₀ ₀ ~P ₀₇ , P ₂ ₀ ~P ₂₇ , P ₃ ₀ ~P ₃₇ , P ₅ ₀ ~P ₅₇ , P ₆ ₀ ~P ₆₇ , P ₇ ₀ ~P ₇₇ , X _{OUT} , PWM ₀ ~PWM ₃ , T, S _{OUT} , CLK, S _{RDY} , SIG (Note 6)				1	mA
I _{OL}	"L" output current P ₁ ₀ ~P ₁₇ (Note 7)	V _{CC} =5V			10	mA
f(X _{IN})	Clock oscillating frequency		0.2		4	MHz
f(X _{CIN})	Clock oscillating frequency for clock function		30		50	kHz

- Note 1 : When only maintaining the RAM data, minimum value of V_{CC} is 2V
 2 : We say the high-speed mode, when the system clock is chosen X_{IN}/4, and the normal mode, when the system clock is chosen X_{IN}/16
 3 : In case M37413E6HFS, 4.5V
 4 : When P3 is X_{CIN} mode, the limits of V_{IH} of P3₁ is 0.85V_{CC} ≤ V_{IH} ≤ V_{CC}, 0 ≤ V_{IL} ≤ 0.15V_{CC}
 5 : Total of I_{OH}(peak) of ports P₀, P₂, P₇ and X_{OUT} is less than 35mA.
 6 : Total of I_{OL}(peak) of ports P₀, P₂, P₃, P₅, P₆ and P₇ is less than 32mA
 7 : Total of I_{OL}(peak) of port P₁ is less than 80mA
 Total of I_{OL}(avg) of port P₁ is less than 40mA.

ELECTRICAL CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{SS} = 0\text{V}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P7 ₀ ~P7 ₇	$V_{CC} = 5\text{V}$, $I_{OH} = -0.5\text{mA}$	4			V
V_{OH}	"H" output voltage X _{OUT}	$V_{CC} = 5\text{V}$, $I_{OH} = -0.3\text{mA}$	4			V
V_{OL}	"L" output voltage P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , T, S _{OUT} , CLK, S _{RDY} , SIG, PWM0~PWM3	$V_{CC} = 5\text{V}$, $I_{OL} = 1\text{mA}$			1	V
V_{OL}	"L" output voltage P1 ₀ ~P1 ₇	$V_{CC} = 5\text{V}$, $I_{OL} = 20\text{mA}$			2	V
V_{OL}	"L" output voltage X _{OUT}	$V_{CC} = 5\text{V}$, $I_{OL} = 0.3\text{mA}$			1	V
$V_{T+} - V_{T-}$	Hysteresis INT ₁ , INT ₂ , INT ₃ , CLK, CNT ₁ , CNT ₂ , SIG, S _{IN} , P2 ₀ ~P2 ₇ , P7 ₀ ~P7 ₇ , X _{CIN}	$V_{CC} = 5\text{V}$		0.7		V
$V_{T+} - V_{T-}$	Hysteresis RESET	$V_{CC} = 5\text{V}$		2		V
$V_{T+} - V_{T-}$	Hysteresis X _{IN}	$V_{CC} = 5\text{V}$		0.5		V
I_{IL}	"L" input current {P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₃ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ } Without pull-up T_r (Note 1) IN ₀ ~IN ₇ , INT ₁ , RESET, X _{IN}	$V_{CC} = 5\text{V}$ $V_I = 0\text{V}$			-5	μA
I_{IH}	"H" input current P0 ₀ ~P0 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P4 ₀ ~P4 ₇ , P7 ₀ ~P7 ₇ , IN ₀ ~IN ₇ , X _{IN} , X _{CIN} , CNV _{SS}	$V_{CC} = 5\text{V}$ $V_I = 5\text{V}$			5	μA
I_{IH}	"H" input current {P1 ₀ ~P1 ₇ , P3 ₀ ~P3 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ } Without pull-up T_r INT ₁ , INT ₂ , INT ₃ , CNT ₁ , CNT ₂ , SIG, RESET, S _{IN} , CLK	$V_I = 10\text{V}$			10	μA
I_{CC}	Supply current	at operation	$f(X_{IN}) = 4\text{MHz}$ High-speed mode $V_{CC} = 5\text{V}$	3	8	mA
			$f(X_{CIN}) = 32\text{kHz}$, $V_{CC} = 3\text{V}$	30	60	
		at wait state	$f(X_{CIN}) = 32\text{kHz}$, $V_{CC} = 5\text{V}$	15	30	μA
		at stop state	$V_{CC} = 5\text{V}$, all clock stop $T_a = 25^\circ\text{C}$	0.1	1.0	
V_{RAM}	RAM retention voltage		2		5.5	V

Note 1 : Also the same as when each pin is used as INT₂, INT₃, CNT₁, CNT₂, SIG, S_{IN} and X_{IN}, respectively

A-D CONVERTER CHARACTERISTICS ($V_{CC} = AV_{CC} = 5\text{V}$, $V_{SS} = AV_{SS} = 0\text{V}$, $T_a = 25^\circ\text{C}$, $f(X_{IN}) = 4\text{MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	bits
—	Non-linearity error	$V_{CC} = V_{REF} = 5.12\text{V}$			± 2	LSB
—	Differential non-linearity	$V_{CC} = V_{REF} = 5.12\text{V}$			± 0.9	LSB
V_{OT}	Zero transition error	$V_{CC} = V_{REF} = 5.12\text{V}$			2	LSB
V_{FST}	Full-scale transition error	$V_{CC} = V_{REF} = 5.12\text{V}$			8	LSB
T_C	Conversion time	$V_{CC} = 5\text{V}$ High-speed mode		25		μs
I_{REF}	Reference input current	$V_{REF} = 5\text{V}$		1.0	2.5	mA
I_{IN}	Analog port input current	$V_{IN} = 0 \sim V_{CC}$		1	10	μA
V_{IN}	Analog input voltage	$V_{CC} = 5\text{V}$	AV_{SS}		V_{CC}	V
V_{REF}	Reference input voltage		2.5		V_{CC}	V

MITSUBISHI MICROCOMPUTERS M37414E5-XXXFP

PROM VERSION of M37414M5-XXXFP

DESCRIPTION

The M37414E5-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 72-pin plastic molded QFP. The features of this chip are similar to those of the M37414M5-XXXFP except that this chip has a 10240 bytes PROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction set, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

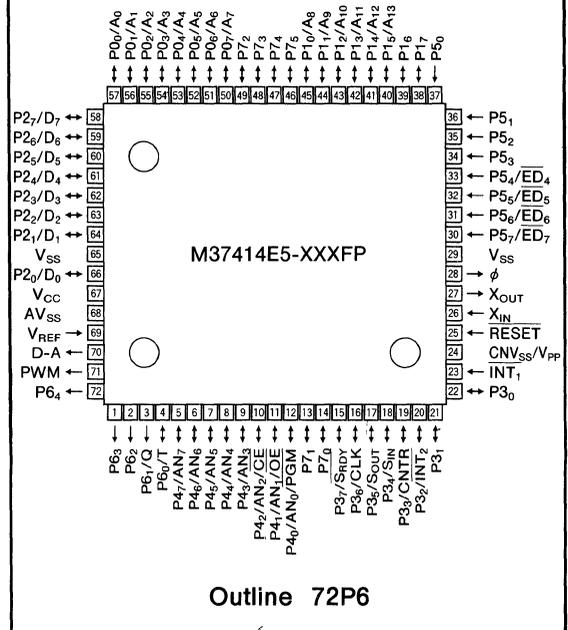
FEATURES

- Number of basic instructions 69
- Memory size ROM 10240 bytes
RAM 160 bytes
- Instruction execution time
..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply 5V±5%
- Power dissipation
normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting 80 levels (Max.)
- Interrupt 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P7) 46
- Input port (Port P5) 8
- Output port (Port P6) 5
- Serial I/O (8-bit) 1
- A-D converter (8-bit resolution) 8 channels
- D-A converter (5-bit resolution) 1 channels
- 8-bit PWM function
- Watchdog timer
- PROM (equivalent to the M5L27128)
program voltage 21V

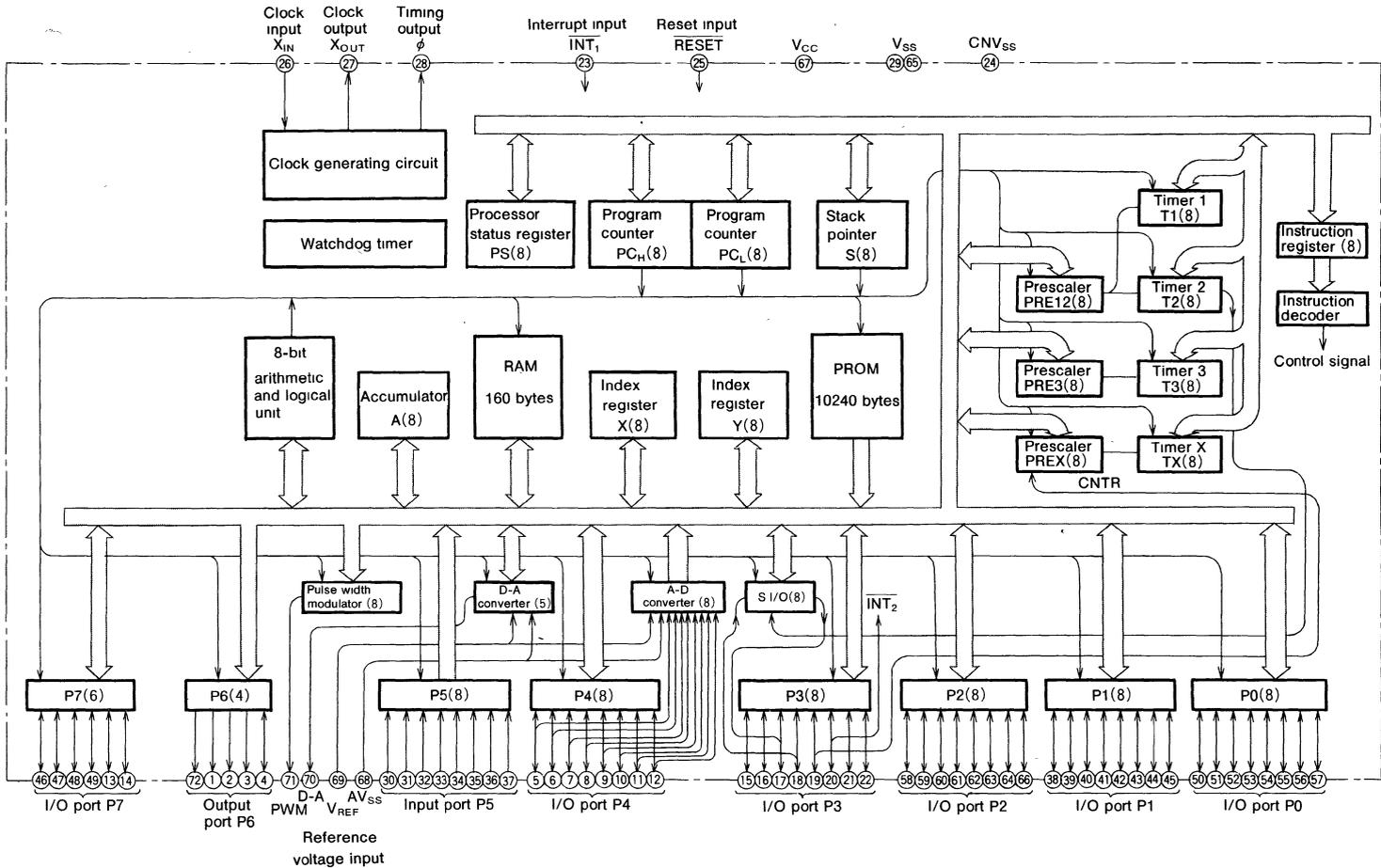
APPLICATION

Office automation equipment
VTR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



M37414E5-XXXFP BLOCK DIAGRAM



PROM VERSION of M37414MS-XXXFP

MITSUBISHI MICROCOMPUTERS
M37414E5-XXXFP

FUNCTIONS OF M37414E5-XXXFP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		2 μ s (minimum instructions, at 4MHz frequency)
Clock frequency		4MHz
Memory Size	PROM	10240bytes (Note 1)
	RAM	160bytes
Input/Output port	INT ₁	Input 1-bitX1
	P0, P1, P2, P3, P4	I/O 8-bitX5 (a part of P3 is in common with serial I/O, timer I/O, and interrupt input)
	P5	Input 8-bitX1
	P6	Output 5-bitX1 (a part of P6 is in common with external trigger output pin)
	P7	I/O 6-bitX1
Serial I/O		8-bitX1
Timers		8-bit prescalerX3+8-bit timerX4
A-D converter		8-bitX1 (8 channels)
D-A converter		5-bitX1
Pulse width modulator		8-bitX1
Watchdog timer		15-bitX1
Subroutine nesting		80 levels (max)
Interrupt		Two external interrupts, three internal timer interrupts
Clock generating circuit		built-in (ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 5%
Power dissipation	at high-speed operation	15mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage	12V (Ports P3, P4, P5, P6, P7 ₀ , P7 ₁ , INT ₁)
	Output current	5mA (Ports P0, P1, P2, P3, P4, P7)
Memory expansion		Possible
Operating temperature range		-10~70°C
Device structure		CMOS silicon gate process
Package		72-pin plastic molded QFP

Note 1 : The PROM programing voltage is 21V (equivalent to the M5L27128)

PROM VERSION of M37414M5-XXXFP

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Single-chip /EPROM	Power supply		Supply 5V±5% to V _{CC} and 0V to V _{SS}
CNV _{SS}	Single-chip	CNV _{SS} input	Input	Connect to 0V
	EPROM	V _{PP} input		Connect to V _{PP} when programming or verifying
RESET	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V _{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
	EPROM	RESET input		Connect to V _{SS}
X _{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X _{IN} and X _{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X _{IN} pin and open the X _{OUT} pin.
X _{OUT}		Clock output	Output	
φ	Single-chip /EPROM	Timing output	Output	For timing output
INT ₁	Single-chip	Interrupt input	Input	Interrupt input INT ₁ .
	EPROM	Interrupt input	Input	Connect to 0V
P0 ₀ ~P0 ₇	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction registers which can program each bit as input or output. It is set to input mode at reset. The output format is CMOS output.
	EPROM	Address input A ₀ ~A ₇	Input	P0 works as the lower 8 bit address input (A ₀ ~A ₇)
P1 ₀ ~P1 ₇	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Address input A ₈ ~A ₁₃	Input	P1 ₀ ~P1 ₅ works as the higher 6 bit address inputs (A ₈ ~A ₁₃). Connect P1 ₆ ~P1 ₇ to V _{CC} .
P2 ₀ ~P2 ₇	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Data input/ output D ₀ ~D ₇	I/O	Port 2 works as an 8 bit data bus (D ₀ ~D ₇).
P3 ₀ ~P3 ₇	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions Port P0. When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as $\overline{S_{RDV}}$, CLK, S _{OUT} , and S _{IN} pins, respectively. Also P3 ₃ and P3 ₂ work as CNTR pin and the lowest interrupt pin (INT ₂), respectively. The output format is N-ch open drain.
	EPROM	Input Port P3	Input	Connect to 0V
P4 ₀ ~P4 ₇	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port which has the same function as Port P0. Ports P4 ₇ ~P4 ₀ are common with Analog inputs AN ₇ ~AN ₀ . The output format is N-ch open drain.
	EPROM	Select mode	Input	P4 ₂ , P4 ₁ , P4 ₀ work as \overline{CE} , \overline{OE} and PGM inputs, respectively. Connect P4 ₅ ~P4 ₇ to 0V and P4 ₄ and P4 ₃ to V _{CC} .
P5 ₀ ~P5 ₇	Single-chip	Input port	Input	Port P5 is an 8-bit input port. Ports P5 ₇ ~P5 ₄ have edge sense functions.
	EPROM	Input port	Input	Connect to 0V

PIN DESCRIPTION (Continued)

Pin	Mode	Name	Input/ Output	Functions
P6 ₀ ~P6 ₄	Single-chip	Output port	Output	Port P6 is an 5-bit output port. At external trigger output mode, P6 ₀ and P6 ₁ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain.
	EPROM	Output port	Output	Connect to 0V.
P7 ₀ ~P7 ₅	Single-chip	I/O port	I/O	Port P7 is an 6-bit I/O port and has basically the same functions as port P0. The output structure of P7 ₀ , P7 ₁ is N-channel open drain, and the output structure of P7 ₂ ~P7 ₅ is CMOS output.
	EPROM	Input port	Input	Connect to 0V.
AV _{SS}	Single-chip	Analog voltage input	Input	GND pin for the A-D and D-A converters.
	EPROM	Analog voltage input	Input	Connect to 0V.
V _{REF}	Single-chip	Reference voltage input	Input	Reference input for A-D and D-A converters.
	EPROM	Reference voltage input	Input	Connect to 0V.
D-A	Single-chip	D-A output	Output	D-A converter output pin.
	EPROM	D-A output	Output	Connect to 0V.
PWM	Single-chip	PWM output	Output	Pulse width modulation output pin (N channel open drain format).
	EPROM	PWM output	Output	Connect to 0V.

PROM VERSION of M37414M5-XXXFP

EPROM MODE

The M37414E5-XXXFP features an EPROM mode in addition to its normal modes. When the RESET signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 gives the pin connection in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, P4₀~P4₂, and CNV_{SS} are used for the PROM (equivalent to the M5L27128). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37414E5-XXXFP	M5L27128
V _{CC}	V _{CC}	V _{CC}
V _{PP}	CNV _{SS} /V _{PP}	V _{PP}
V _{SS}	V _{SS}	V _{SS}
Address input	Ports P0, P1 ₀ ~P1 ₅	A ₀ ~A ₁₃
Data I/O	Port P2	D ₀ ~D ₇
CE	P4 ₂ /CE	CE
OE	P4 ₁ /OE	OE
PGM	P4 ₀ /PGM	PGM

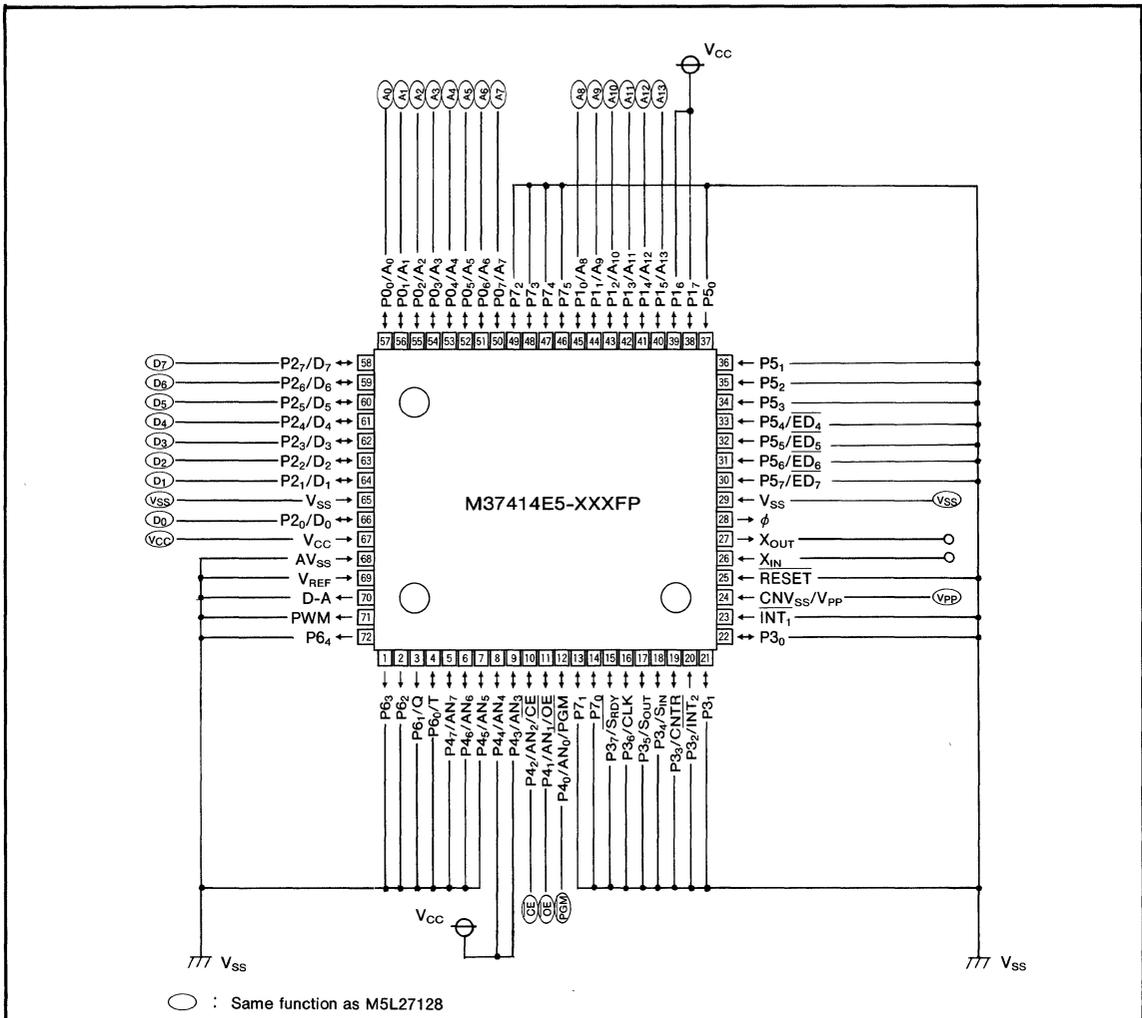


Fig. 1 Pin connection in EPROM programming mode

PROM VERSION of M37414M5-XXXFP

PROM READING AND WRITING

Reading

To read the PROM, set the \overline{CE} and \overline{OE} pins to a "L" level, and the \overline{PGM} pin to a "H" level. Input the address of the data ($A_0 \sim A_{13}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the \overline{CE} or \overline{OE} pins are in the "H" state.

Writing

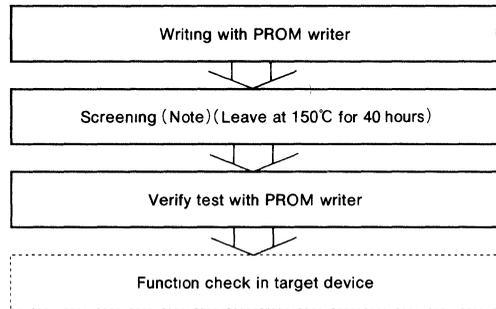
To write to the PROM, set the \overline{CE} pin to a "L" level and the \overline{OE} pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{13}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the \overline{PGM} pin to a "L" level to begin writing.

Notes on Writing

When using an PROM writer, the address range should be between 1800_{16} and $3FFF_{16}$. When data is written between addresses 0000_{16} and $3FFF_{16}$, fill addresses 0000_{16} to $17FF_{16}$ with 00_{16} .

NOTES ON HANDLING

- (1) Since a high voltage (21V) is used to write data, care should be taken when turning on the PROM writer's power.
- (2) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150°C exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}(10)$	$\overline{OE}(11)$	$\overline{PGM}(12)$	$V_{PP}(24)$	$V_{CC}(67)$	Data I/O (58~64, 66)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse ($V_{IH} \rightarrow V_{IL}$)	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively
 2 : An X indicates either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS} With the output transistor cut-off	-0.3~7	V
V _I	Input voltage X _{IN}		-0.3~7	V
V _I	Input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₄ ~P ₄₇ , P ₇ ~P ₇₅		-0.3~V _{CC} +0.3	V
V _I	Input voltage P ₃ ~P ₃₇ , P ₅ ~P ₅₇ , P ₆ , P ₇ , P ₇ , INT ₁		-0.3~13	V
V _I	Input voltage CNV _{SS} , RESET		-0.3~13 (Note 1)	V
V _O	Output voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₄ ~P ₄₇ , P ₇ ~P ₇₅ , X _{OUT} , φ, D-A		-0.3~V _{CC} +0.3	V
V _O	Output voltage P ₃ ~P ₃₇ , P ₆ ~P ₆₄ , P ₇ , P ₇ , PWM		-0.3~13	V
P _d	Power dissipation	T _a =25°C	300	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

Note 1 : In PROM programming mode, CNV_{SS} is 22.0V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=-10~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{SS}	Supply voltage		0		V
V _{REF}	Reference voltage	4		V _{CC}	V
V _{IH}	"H" input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , INT ₁ , RESET, X _{IN} , CNV _{SS} , P ₆ , P ₇ ~P ₇₅	0.8V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , INT ₁ , CNV _{SS} , P ₆ , P ₇ ~P ₇₅	0		0.2V _{CC}	V
V _{IL}	"L" input voltage RESET	0		0.12V _{CC}	V
V _{IL}	"L" input voltage X _{IN}	0		0.16V _{CC}	V
I _{OL(peak)}	"L" peak output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , P ₄ ~P ₄₇ , P ₇ ~P ₇₅ (Note 2)			10	mA
I _{OL(peak)}	"L" peak output current P ₆ ~P ₆₃ (Note 2)			15	mA
I _{OL(peak)}	"L" peak output current PWM, P ₆₄ (Note 2)			5	mA
I _{OL(avg)}	"L" average output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₇ , P ₄ ~P ₄₇ , P ₇ ~P ₇₅ (Note 1)			5	mA
I _{OL(avg)}	"L" average output current P ₆ ~P ₆₃ (Note 1)			7	mA
I _{OL(avg)}	"L" average output current PWM, P ₆₄ (Note 1)			2.5	mA
I _{OH(peak)}	"H" peak output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₇ ~P ₇₅ (Note 2)			-10	mA
I _{OH(avg)}	"H" average output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₇ ~P ₇₅ (Note 1)			-5	mA
f(X _{IN})	Internal clock oscillating frequency			4	MHz

- Note 1 : The average output currents I_{OL(avg)} and I_{OH(avg)} are the average value of a period of 100ms
 2 : Do not allow the combined low-level output current of ports P₀, P₁, P₂, P₃, P₄, P₆, P₇ and PWM to exceed 80mA.
 Do not allow the combined high-level output current of port P₀, P₁, P₂ P₇~P₇₅ to exceed 50mA
 3 : "H" input voltage of ports P₃, P₅, P₆, P₇, P₇ and INT₁ is available up to +12V

PROM VERSION of M37414M5-XXXFP

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max.	
V_{OH}	"H" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P7 ₂ ~P7 ₅	$I_{OH}=-10mA$	3			V
V_{OH}	"H" output voltage ϕ	$I_{OH}=-2.5mA$	3			V
V_{OL}	"L" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P6 ₀ ~P6 ₃ , P7 ₀ ~P7 ₅	$I_{OL}=10mA$			2	V
V_{OL}	"L" output voltage ϕ , PWM, P6 ₄	$I_{OL}=5mA$			2	V
$V_{T+}-V_{T-}$	Hysteresis INT ₁		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis P3 ₆	When used as CLK input	0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis P3 ₂	When used as INT ₂ input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis P3 ₃	When used as CNTR input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis P6 ₀	When used as T input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis RESET			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X _{IN}		0.1		0.5	V
I_{IL}	"L" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ , P7 ₀ ~P7 ₅ , PWM	$V_I=0V$			-5	μA
I_{IL}	"L" input current INT ₁ , RESET, X _{IN}	$V_I=0V$			-5	μA
I_{IH}	"H" input current P3 ₀ ~P3 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ , P7 ₀ , P7 ₁ , PWM	$V_I=12V$			12	μA
I_{IH}	"H" input current INT ₁ , RESET, X _{IN} , P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P4 ₀ ~P4 ₇ , P7 ₂ ~P7 ₅	$V_I=5V$			5	μA
V_{RAM}	RAM retention voltage	At clock stop	2			V
I_{CC}	Supply current	ϕ , X _{OUT} , and D-A pins opened, other pins at V_{SS} , and A-D converter in the finished condition.	$f(X_{IN})=4MHz$ Square wave	3	6	μA
			At clock stop $T_a=25^\circ C$		1	
			At clock stop $T_a=75^\circ C$		10	

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistance value	$V_{REF}=V_{CC}$	2		10	k Ω
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			5	Bits
—	Error in full scale range	$V_{REF}=V_{CC}$			± 1	%
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
R_O	Output resistance	$V_{REF}=V_{CC}$			3	k Ω
V_{REF}	Reference voltage		4		V_{CC}	V

TIMING REQUIREMENTS

Single-chip mode ($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
$t_{SU(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{SU(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{SU(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{SU(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{SU(P4D-\phi)}$	Port P4 input setup time		270			ns
$t_{SU(P5D-\phi)}$	Port P5 input setup time		270			ns
$t_{SU(P7D-\phi)}$	Port P7 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		20			ns
$t_{h(\phi-P7D)}$	Port P7 input hold time		20			ns
t_C	External clock input cycle time		250			ns
t_W	External clock input pulse width		75			ns
t_r	External clock rising edge time				25	ns
t_f	External clock falling edge time				25	ns

Eva-chip mode ($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{SU(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{SU(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{SU(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

Memory expanding mode and microprocessor mode

($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{SU(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		30			ns

SWITCHING CHARACTERISTICS

Single-chip mode ($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 3			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig. 2			230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				230	ns
$t_{d(\phi-P7Q)}$	Port P7 ₀ , P7 ₁ data output delay time	Fig 3			230	ns
$t_{d(\phi-P7Q)}$	Port P7 ₂ ~P7 ₅ data output delay time				230	ns

Eva-chip mode ($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig 3			250	ns	
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns	
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns	
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns	
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns	
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns	
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns	
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns	
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns	
$t_{d(\phi-R/W)}$	R/W signal output delay time		Fig 2			250	ns
$t_{d(\phi-R/WF)}$	R/W signal output delay time					250	ns
$t_{d(\phi-P3_0Q)}$	Port P3 ₀ data output delay time				200	ns	
$t_{d(\phi-P3_0QF)}$	Port P3 ₀ data output delay time				200	ns	
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns	
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns	
$t_{d(\phi-P3_1Q)}$	Port P3 ₁ data output delay time			200	ns		
$t_{d(\phi-P3_1QF)}$	Port P3 ₁ data output delay time			200	ns		

Memory expanding mode and microprocessor mode

($V_{CC}=5V\pm 5\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig 3			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time	Fig 2			300	ns
$t_{d(\phi-R/W)}$	R/W signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

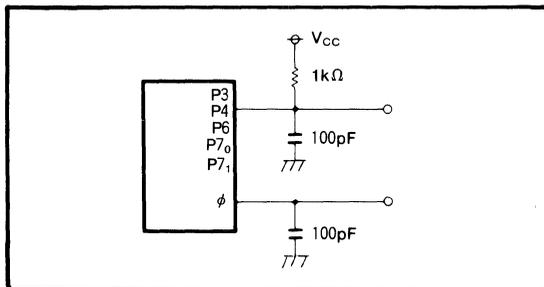


Fig. 2 Ports P3, P4, P6, P7₀, P7₁ test circuit

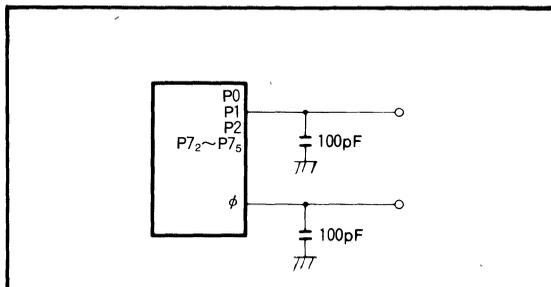
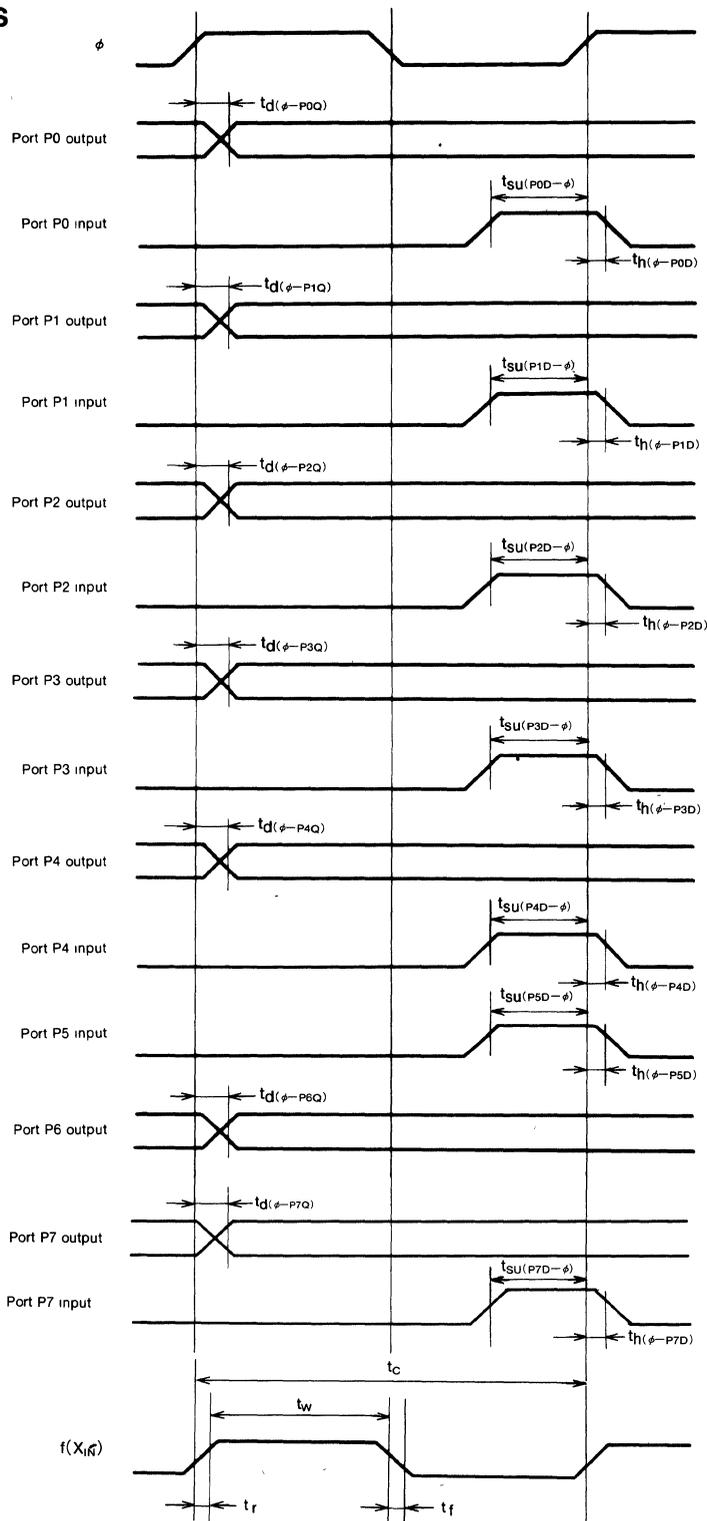
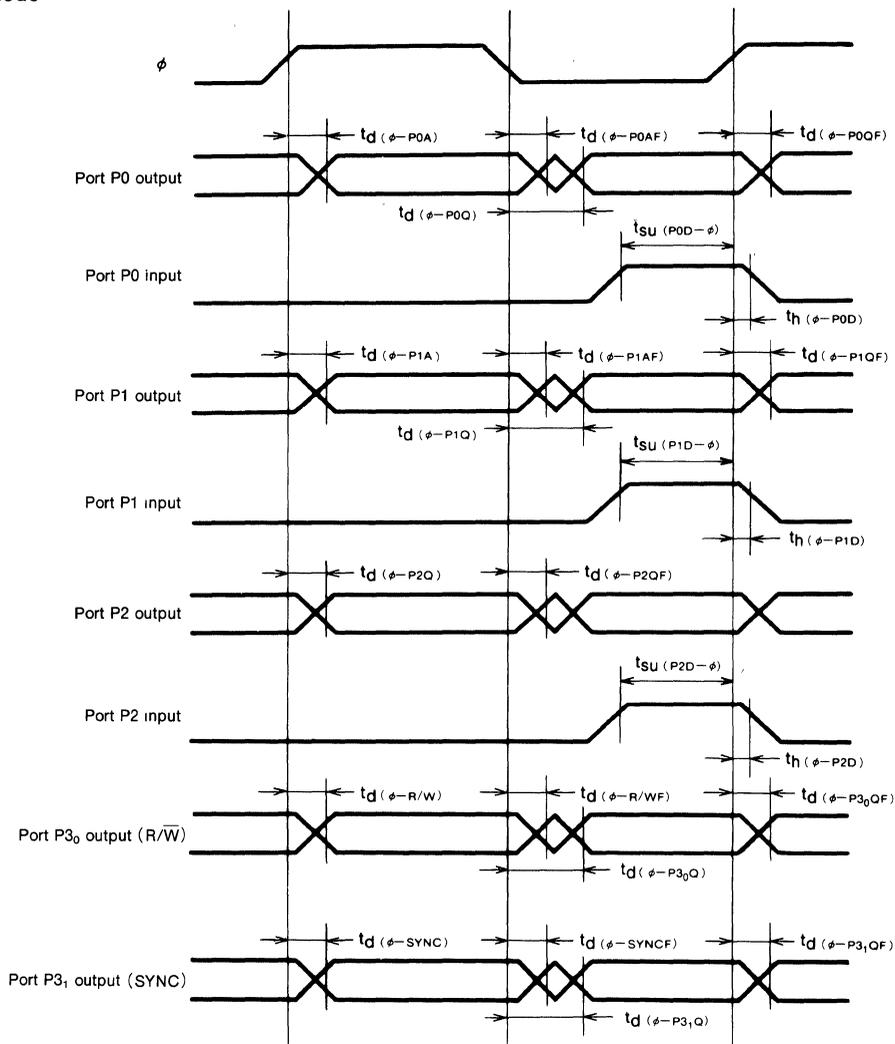


Fig. 3 Port P0, P1, P2, P7₂~P7₅ test circuit

TIMING DIAGRAMS
 In single-chip mode

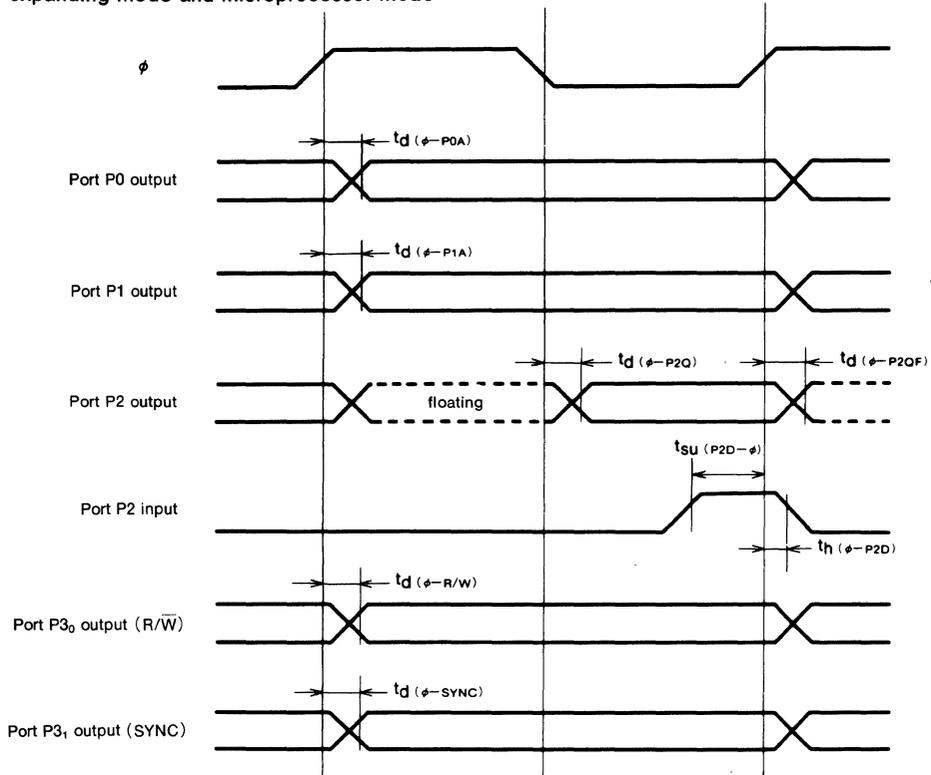


In eva-chip mode



PROM VERSION of M37414M5-XXXFP

In memory expanding mode and microprocessor mode



MITSUBISHI MICROCOMPUTERS
M37420E6-XXXSP
M37420E6SS
PROM VERSION of M37420M6-XXXSP

DESCRIPTION

The M37420E6-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP. The features of this chip are similar to those of the M37420M6-XXXSP except that this chip has a 12288 bytes PROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The M37420E6SS is the window type.

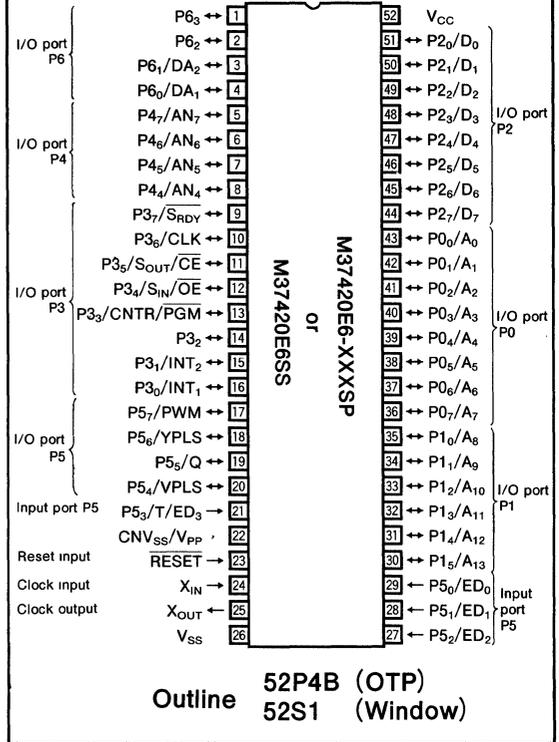
FEATURES

- Number of basic instructions..... 69
- Memory size ROM 12288 bytes
RAM 256 bytes
- Instruction execution time
..... 1μs (minimum instructions at 8MHz frequency)
- Single power supply..... 5V±5%
- Power dissipation
normal operation mode (at 8MHz frequency)..... 30mW
- Subroutine nesting 96 levels (Max.)
- Interrupt..... 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P5, P6)..... 42
- Input port (Port P5) 4
- Serial I/O (8/16-bit) 1
- A-D converter (8-bit) 4
- D-A converter (8-bit) 2
- 14-bit PWM function
- Watchdog timer
- PROM (equivalent to the M5L27128)
program voltage..... 21V

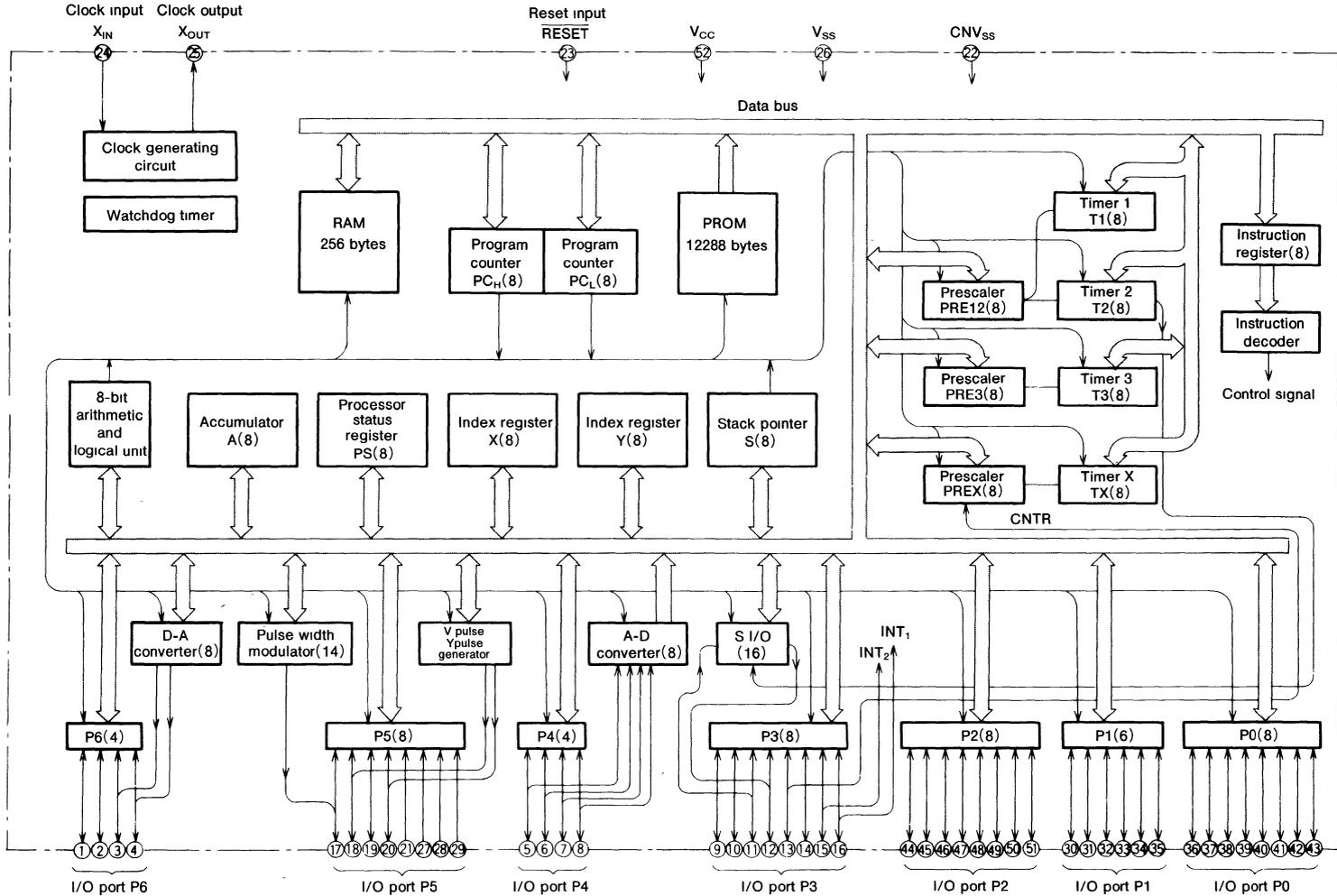
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



M37420E6-XXXSP BLOCK DIAGRAM



MITSUBISHI MICROCOMPUTERS
M37420E6-XXXSP
M37420E6SS

PROM VERSION of M37420M6-XXXSP

FUNCTIONS OF M37420E6-XXXSP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		1 μ s (minimum instructions, at 8MHz frequency)
Clock frequency		8MHz
Memory size	PROM	12288 bytes (Note 1)
	RAM	256 bytes
Input/Output ports	P0, P1, P2, P3, P4, P5 ₀ ~P5 ₇ , P6	I/O 8-bit \times 3, 6-bit \times 1, 4-bit \times 3
	P5 ₀ ~P5 ₃	Input 4-bit \times 1
Serial I/O		8-bit \times 1 or 16-bit \times 1
Timers		8-bit prescaler \times 3+8-bit timer \times 4
A-D conversion		8-bit \times 1 (4 channels)
D-A conversion		8-bit \times 2
Pulse width modulator		14-bit \times 1
Watchdog timer		15-bit \times 1
Subroutine nesting		96 levels (max)
Interrupt		Two external interrupts, three internal timer interrupts (or timer \times 2, S I/O \times 1)
Clock generating circuit		built-in (ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 5%
Power dissipation		30mW (at 8MHz frequency)
Input/Output characteristics	Input/Output voltage	12V (Ports P0, P1, P3)
Operating temperature range		-10~70 $^{\circ}$ C
Device structure		CMOS silicon gate process
Package	M37420E6-XXXSP	52-pin shrink plastic molded DIP
	M37420E6SS	52-pin shrink ceramic DIP

Note 1 : The PROM programing voltage is 21V (equivalent to the M5L27128)

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Single-chip /EPROM	Power supply		Supply 5V ± 5% to V _{CC} and 0V to V _{SS} . This voltage can be used as reference voltage for A-D or D-A converter.
CNV _{SS} /V _{PP}	Single-chip	CNV _{SS} input	Input	Connect to 0V
	EPROM	V _{PP} input		Connect to V _{PP} when programming or verifying
RESET	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V _{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	RESET input		Connect to V _{SS}
X _{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X _{IN} and X _{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X _{IN} pin and open the X _{OUT} pin.
X _{OUT}		Clock output	Output	
P0 ₀ ~P0 ₇	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction registers which can program each bit as input or output. It is set to input mode at reset. The output format is N-ch open drain.
	EPROM	Address input A ₀ ~A ₇	Input	P0 works as the lower 8 bit address input (A ₀ ~A ₇).
P1 ₀ ~P1 ₅	Single-chip	I/O port P1	I/O	Port P1 is an 6-bit I/O port which has the same function as port P0.
	EPROM	Address input A ₈ ~A ₁₃	Input	P1 ₀ ~P1 ₅ works as the higher 6 bit address inputs (A ₈ ~A ₁₃).
P2 ₀ ~P2 ₇	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port which has the same function as port P0. The output format is CMOS.
	EPROM	Data input/output D ₀ ~D ₇	I/O	Port 2 works as an 8 bit data bus (D ₀ ~D ₇).
P3 ₀ ~P3 ₇	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same function as port P0. When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as S _{RDY} , CLK, S _{OUT} , and S _{IN} pins, respectively. Also P3 ₃ , P3 ₁ , and P3 ₀ work as CNTR pin, INT ₂ and INT ₁ , respectively. The output format is N-ch open drain.
	EPROM	Input Port P3	Input	P3 ₅ , P3 ₄ and P3 ₃ work as \overline{CE} , \overline{OE} and PGM inputs respectively. Connect P3 ₀ ~P3 ₂ to 0V and P3 ₇ and P3 ₆ to V _{CC} .
P4 ₄ ~P4 ₇	Single-chip	I/O port P4	I/O	Port P4 is an 4-bit I/O port which has the same function as port P0. Ports P4 ₇ ~P4 ₄ are common with analog inputs AN ₇ ~AN ₄ . The output format is N-ch open drain.
	EPROM	Select mode	Input	Connect to 0V.
P5 ₀ ~P5 ₃	Single-chip	Input port P5	Input	P5 ₀ ~P5 ₃ are input port. These port can be used as edge-sence input. P5 ₀ ~P5 ₂ detects rising edge, and P5 ₃ detects both rising and falling edge. P5 ₃ is also common with external trigger output and V pulse, Y pulse generator trigger input.
	EPROM		Input	Connect to 0V.
P5 ₄ ~P5 ₇	Single-chip	I/O port P5	I/O	P5 ₄ ~P5 ₇ is I/O port and has basically the same function as port P0. P5 ₇ is common with PWM. The output format is CMOS output.
	EPROM		Input	Connect to 0V.
P6 ₀ ~P6 ₃	Single-chip	I/O port P6	I/O	Port P6 is 4-bit I/O port and has basically the same function as port P0. P6 ₀ and P6 ₁ are common with DA ₁ and DA ₂ respectively. The output format is CMOS output.
	EPROM		Input	Connect to 0V.

M37420E6-XXXSP M37420E6SS

PROM VERSION of M37420M6-XXXSP

EPROM MODE

The M37420E6-XXXSP or M37420E6SS features an EPROM mode in addition to its normal modes. When the RESET signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, P3₃ ~ P3₅, and CNV_{SS} are used for the PROM (equivalent to the M5L27128). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37420E6-XXXSP, M37420E6SS	M5L27128
V _{CC}	V _{CC}	V _{CC}
V _{PP}	CNV _{SS} /V _{PP}	V _{PP}
V _{SS}	V _{SS}	V _{SS}
Address input	Ports P0, P1	A ₀ ~A ₁₃
Data I/O	Port P2	D ₀ ~D ₇
CE	P3 ₅ /CE	CE
OE	P3 ₄ /OE	OE
PGM	P3 ₃ /CNTR/PGM	PGM

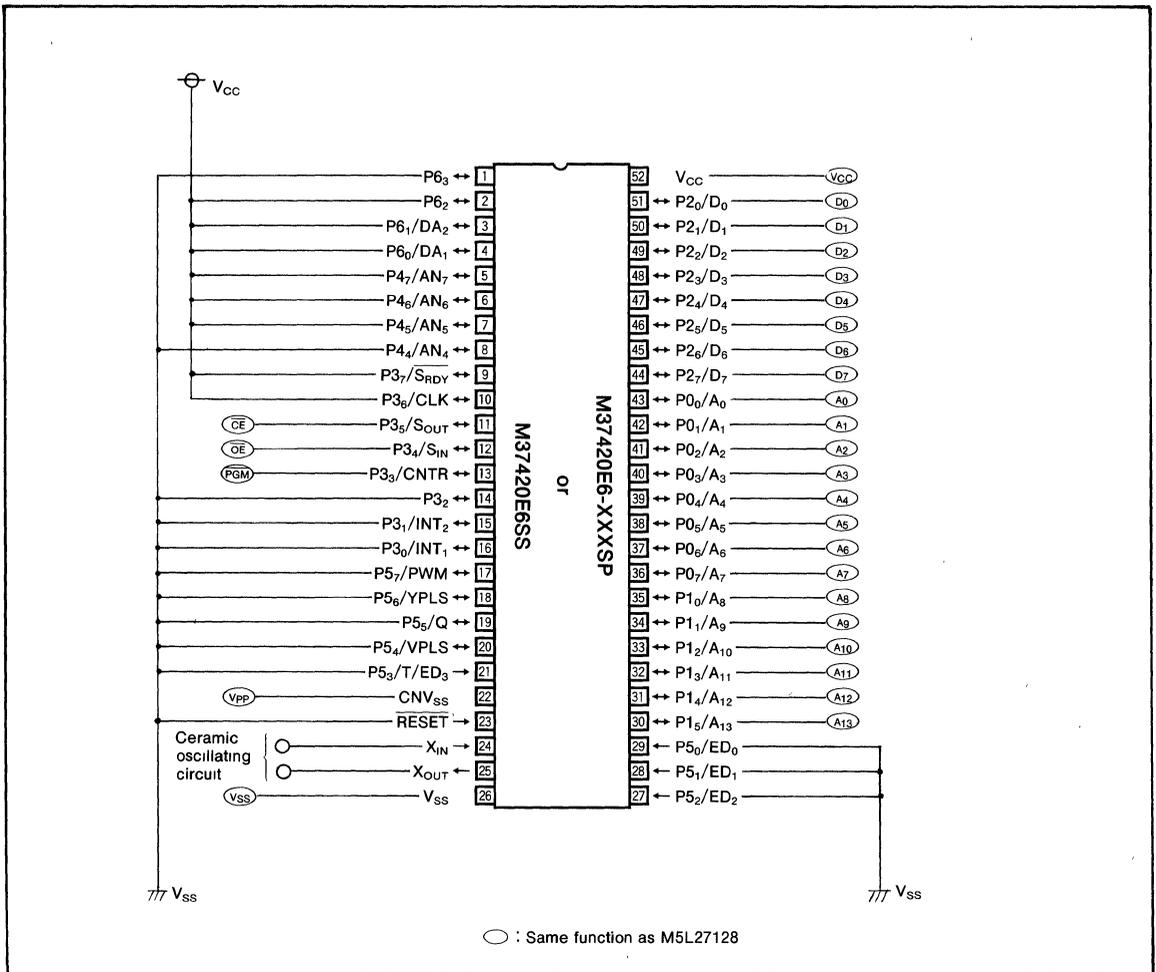


Fig. 1 Pin connection in EPROM mode

PROM READING, WRITING AND ERASING
Reading

To read the PROM, set the \overline{CE} and \overline{OE} pins to a "L" level, and the \overline{PGM} pin to a "H" level. Input the address of the data ($A_0 \sim A_{13}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the \overline{CE} or \overline{OE} pins are in the "H" state.

Writing

To write to the PROM, set the \overline{CE} pin to a "L" level and the \overline{OE} pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{13}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the \overline{PGM} pin to a "L" level to begin writing.

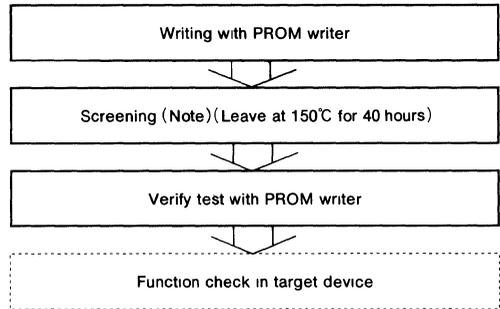
Erasing

Data can only be erased on the M37420E6SS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is $15W \cdot s/cm^2$.

NOTES ON HANDLING

- (1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

- (2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.
- (3) Since a high voltage (21V) is used to write data, care should be taken when turning on the PROM writer's power.
- (4) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150°C exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}(11)$	$\overline{OE}(12)$	$\overline{PGM}(13)$	$V_{PP}(22)$	$V_{CC}(52)$	Data I/O (44~51)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse($V_{IH} \rightarrow V_{IL}$)	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively
 2 : An X indicates either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Rated	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the output transistor cut-off	-0.3~7	V
V_I	Input voltage X_{IN} , RESET		-0.3~7	V
V_I	Input voltage $P2_0\sim P2_7$, $P4_4\sim P4_7$, $P5_4\sim P5_7$, $P6_0\sim P6_3$		-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage $P0_0\sim P0_7$, $P1_0\sim P1_5$, $P3_0\sim P3_7$, $P5_0\sim P5_7$		-0.3~13	V
V_I	Input voltage CNV_{SS}		-0.3~13 (Note 1)	V
V_O	Output voltage $P2_0\sim P2_7$, $P4_0\sim P4_7$, $P5_4\sim P5_7$, $P6_0\sim P6_3$		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage $P0_0\sim P0_7$, $P1_0\sim P1_5$, $P3_0\sim P3_7$		-0.3~13	V
P_d	Power dissipation	$T_a=25^\circ\text{C}$	1000	mW
T_{opr}	Operating temperature		-10~70	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~125	$^\circ\text{C}$

Note 1 : In EPROM programming mode, CNV_{SS} is 22.0V

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V\pm 5\%$, $T_a=-10\sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0\sim P0_7$, $P1_0\sim P1_5$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P4_4\sim P4_7$, $P5_0\sim P5_7$, $P6_0\sim P6_3$, RESET, X_{IN}	0.8 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0\sim P0_7$, $P1_0\sim P1_5$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P4_0\sim P4_7$, $P5_0\sim P5_7$, $P6_0\sim P6_3$, CNV_{SS}	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage RESET	0		0.12 V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16 V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7$, $P1_0\sim P1_5$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P4_0\sim P4_7$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0\sim P6_3$ (Note 2)			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7$, $P1_0\sim P1_5$, $P2_0\sim P2_7$, $P3_0\sim P3_7$, $P4_4\sim P4_7$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0\sim P6_3$ (Note 1)			5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0\sim P2_7$, $P5_4\sim P5_7$, $P6_0\sim P6_3$ (Note 2)			-10	mA
$I_{OH(avg)}$	"H" average output current $P2_0\sim P2_7$, $P5_4\sim P5_7$, $P6_0\sim P6_3$ (Note 1)			-5	mA
$f(X_{IN})$	Internal clock oscillating frequency			8	MHz

Note 1 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.

2 : Do not allow the combined low-level output current of ports $P0$, $P1$, $P2$, $P3$, $P4$ and $P6$ to exceed 80mA

Do not allow the combined high-level output current of port $P2$, $P5$ and $P6$ to exceed 50mA

MITSUBISHI MICROCOMPUTERS
M37420E6-XXXSP
M37420E6SS

PROM VERSION of M37420M6-XXXSP

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=8MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ	Max		
V_{OH}	"H" output voltage P2 ₀ ~P2 ₇ , P5 ₄ ~P5 ₇ , P6 ₀ ~P6 ₃	$I_{OH}=-10mA$	3			V	
V_{OL}	"L" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₅ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₄ ~P5 ₇ , P6 ₀ ~P6 ₃	$I_{OL}=10mA$			2	V	
$V_{T+}-V_{T-}$	Hysteresis P3 ₀ , P3 ₁	When used as INT input	0.3		1	V	
$V_{T+}-V_{T-}$	Hysteresis P3 ₆	When used as CLK input	0.3	0.8		V	
$V_{T+}-V_{T-}$	Hysteresis P3 ₃	When used as CNTR input	0.5	1		V	
$V_{T+}-V_{T-}$	Hysteresis P5 ₃	When used as T input	0.5	1		V	
$V_{T+}-V_{T-}$	Hysteresis RESET			0.5	0.7	V	
$V_{T+}-V_{T-}$	Hysteresis X _{IN}		0.1		0.5	V	
I_{IL}	"L" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₅ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₃	$V_I=0V$			-5	μA	
I_{IL}	"L" input current RESET, X _{IN}	$V_I=0V$			-5	μA	
I_{IH}	"H" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₅ , P3 ₀ ~P3 ₇ , P5 ₀ ~P5 ₃	$V_I=12V$			12	μA	
I_{IH}	"H" input current INT ₁ , RESET, X _{IN} , P2 ₀ ~P2 ₇ , P4 ₄ ~P4 ₇ , P5 ₄ ~P5 ₇ , P6 ₀ ~P6 ₃	$V_I=5V$			5	μA	
V_{RAM}	RAM retention voltage	At clock stop	2			V	
I_{CC}	Supply current	ϕ , X _{OUT} , and D-A pins opened, other pins at V _{SS} , and A-D converter in the finished condition			6	15	mA

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=8MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistance value	$V_{REF}=V_{CC}$	2		10	k Ω
t_{CONV}	Conversion time				25	μs
V_{IA}	Analog input voltage		0		V_{CC}	V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=8MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Error in full scale range	$V_{REF}=V_{CC}$			± 2	%
t_{SU}	Setup time	$V_{REF}=V_{CC}$			3	μs
R_O	Output resistance	$V_{REF}=V_{CC}$	1	2	4	k Ω

PRELIMINARY

These chips are not a final product in this form. They are subject to change without notice.

MITSUBISHI MICROCOMPUTERS

M37424E8-XXXSP M37524E4-XXXSP

PROM VERSION of M37424M8-XXXSP, M37524M4-XXXSP

DESCRIPTION

The M37424E8-XXXSP, M37524E4-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. They are housed in a 64-pin shrink plastic molded DIP. The features of these chips are similar to those of the M37424M8-XXXSP, M37524M4-XXXSP except that these chips have a 16384 bytes PROM built in. These single-chip microcomputers are useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, these chips are suitable for small quantity production runs.

The differences between the M37424E8-XXXSP and the M37524E4-XXXSP are noted below. The following explanations apply to the M37424E8-XXXSP.

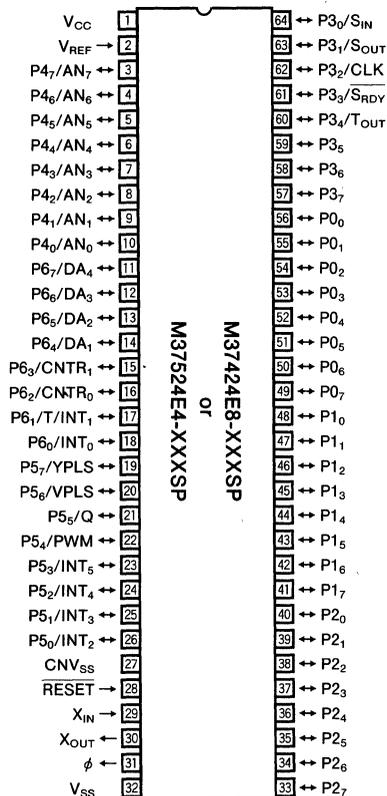
Specification variations for other chips are noted accordingly.

Type name	Port P1 output structure
M37424E8-XXXSP	CMOS
M37524E4-XXXSP	N-channel open drain

FEATURES

- Number of basic instructions..... 70
68 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size PROM..... 16384 bytes
RAM..... 256 bytes
- Instruction execution time
..... 1μs (minimum instructions, at 4MHz frequency)
- Single power supply..... 5V±10%
- Power dissipation
normal operation mode (at 4MHz frequency)..... 30mW
- Subroutine nesting..... 96 levels (Max.)
- Interrupt..... 16 types, 16 vectors
- 8-bit timer..... 4
- 16-bit timer..... 1
- Serial I/O (8-bit or 16-bit)..... 1
- PWM output (14-bit)..... 1
- A-D converter (8-bit resolution)..... 8-channel
- D-A converter (5-bit resolution)..... 2
- D-A converter (8-bit resolution)..... 2
- Watchdog timer
- External trigger output (1-bit)..... 1
- V pulse Y pulse generator
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P5, P6)..... 56
- PROM (equivalent to the M5L27256)
- Program voltage..... 12.5V

PIN CONFIGURATION (TOP VIEW)

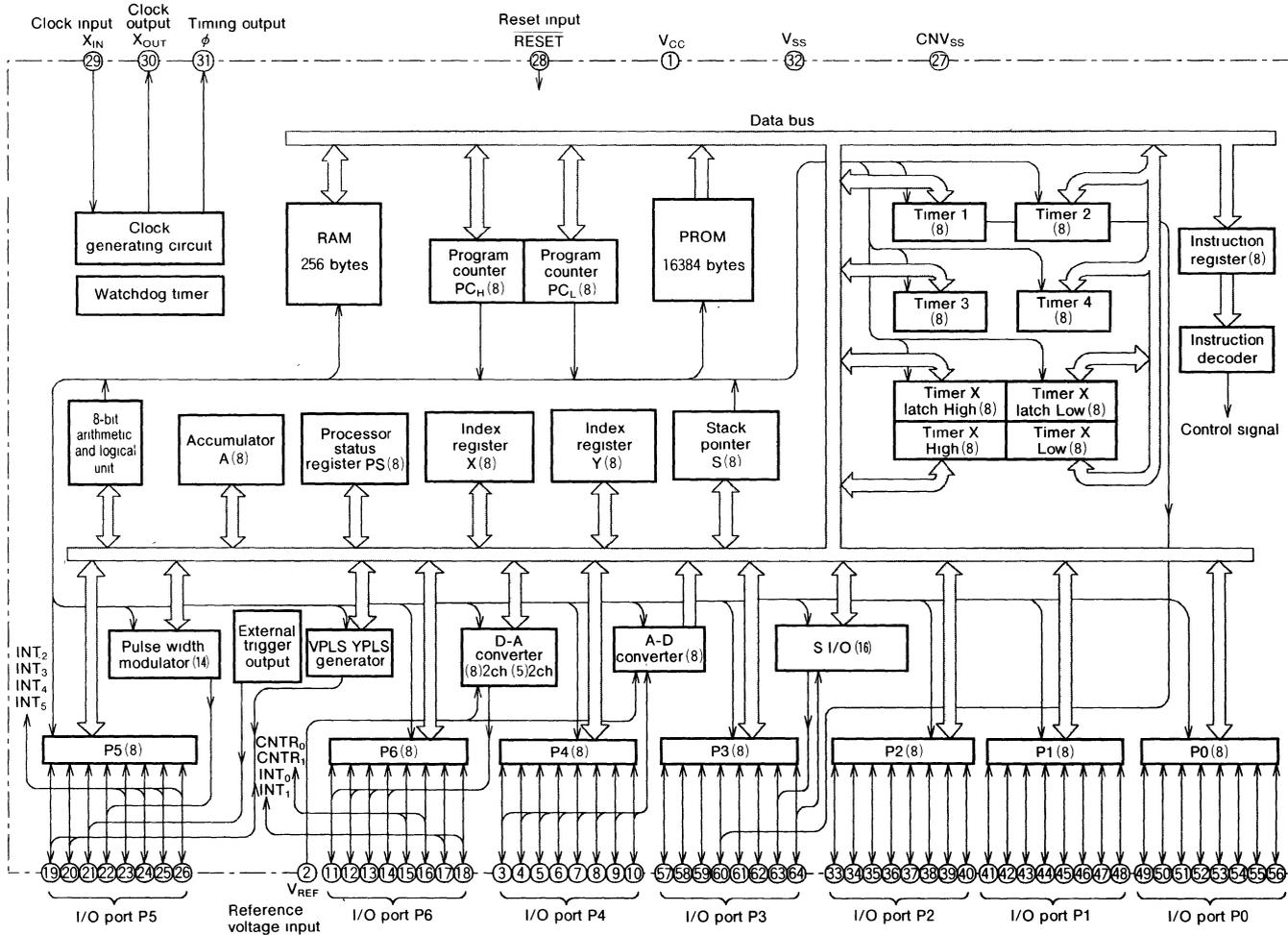


Outline 64P4B

APPLICATION

Office automation equipment
VCR equipment

M37424E8-XXXSP BLOCK DIAGRAM



FROM VERSION of M37424M8-XXXSP, M37524M4-XXXSP

MITSUBISHI MICROCOMPUTERS
M37424E8-XXXSP
M37524E4-XXXSP



FUNCTIONS OF M37424E8-XXXSP

Parameter		Functions
Number of basic instructions		70 (68 MELPS 740 basic instructions+2)
Instruction execution time		1 μ s (minimum instructions, at 4MHz frequency)
Clock frequency		4MHz
Memory size	PROM	16384 bytes
	RAM	256 bytes
Input/Output ports	P0, P1, P2, P3, P4, P5, P6	I/O
Serial I/O		8-bit \times 7
Timers		8-bit \times 4, 16-bit \times 1
A-D conversion		8-bit \times 1 (8 channels)
D-A conversion		5-bit \times 2, 8-bit \times 2
Pulse width modulator		14-bit \times 1
Watchdog timer		15-bit \times 1
Subroutine nesting		96 levels (max)
Interrupt		16 (external 8, Internal 8)
Clock generating circuit		Built-in (ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 10%
Power dissipation		30mW (at 4MHz frequency)
Operating temperature range		-10 to 70°C
Device structure		CMOS silicon gate
Package		64-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Mode	Name	Input/Output	Functions
V _{CC} , V _{SS}	Single-chip /EPROM	supply voltage		Power supply inputs 5V \pm 10% to V _{CC} , and 0V to V _{SS}
CNV _{SS}	Single-chip	CNV _{SS}		This is usually connected to V _{SS}
	EPROM	V _{PP} input	Input	Connect to V _{PP} when programming or verifying
V _{REF}	Single-chip	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter
	EPROM	Reference voltage input	Input	Connected to V _{SS}
RESET	Single-chip	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 4 μ s (under normal V _{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
	EPROM	Reset input	Input	Connected to V _{SS} .
X _{IN}	Single-chip /EPROM	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open
X _{OUT}		Clock output	Output	
ϕ	Single-chip /EPROM	Timing output	Output	This is the timing output pin
P0 ₀ -P0 ₇	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output
	EPROM	Address input A ₀ -A ₇	Input	P0 works as the lower 8-bit address input

PROM VERSION of M37424M8-XXXSP, M37524M4-XXXSP
PIN DESCRIPTION (Continue)

Pin	Mode	Name	Input/ Output	Functions
P1 ₀ -P1 ₇	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure of M37424M8-XXXSP is CMOS output and that of M37524M4-XXXSP is N-channel open drain output.
	EPROM	Address input A ₈ -A ₁₄	Input	P1 ₀ to P1 ₆ works as the higher 8-bit address input. Connect V _{CC} to P1 ₇ .
P2 ₀ -P2 ₇	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
	EPROM	Data input/output D ₀ ~D ₇	I/O	P2 works as an 8-bit data bus.
P3 ₀ -P3 ₇	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, P3 ₃ , P3 ₂ , P3 ₁ , and P3 ₀ work as \overline{S}_{RDY} , CLK, S _{OUT} , and S _{IN} pins, respectively. Also P3 ₄ works as T _{OUT} pin. The output structure is N-channel open drain.
	EPROM	Select mode	Input	P3 ₃ and P3 ₄ works as \overline{CE} and \overline{OE} inputs respectively. Connect V _{CC} to P3 ₀ -P3 ₂ . Connect V _{SS} to P3 ₅ -P3 ₇ .
P4 ₀ -P4 ₇	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. P4 ₀ to P4 ₇ work as analog input port AN ₀ to AN ₇ .
	EPROM	Input port P4	Input	Connected to V _{SS} .
P5 ₀ -P5 ₇	Single-chip	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0. P5 ₇ , P5 ₆ , P5 ₅ , P5 ₄ and P5 ₃ to P5 ₀ are in common with the YPLS output, VPLS output, Q output, PWM output and interrupt input respectively.
	EPROM	Input port P5	Input	Connected to V _{SS} .
P6 ₀ -P6 ₇	Single-chip	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0. P6 ₇ to P6 ₄ , P6 ₃ , P6 ₂ , and P6 ₁ , P6 ₀ are in common with the D-A output, CNTR output and interrupt input respectively.
	EPROM	Input port P6	Input	Connected to V _{SS} .

M37424E8-XXXSP
M37524E4-XXXSP

PROM VERSION of M37424M8-XXXSP, M37524M4-XXXSP

EPROM MODE

The M37424E8-XXXSP features an EPROM mode in addition to its normal modes. When the RESET signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 gives the pin connection in the EPROM mode. When in the EPROM mode, ports P0 to P2, P3₃, P3₄, CNV_{SS} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37424E8-XXXSP	M5L27256
V _{CC}	V _{CC}	V _{CC}
V _{PP}	CNV _{SS}	V _{PP}
V _{SS}	V _{SS}	V _{SS}
Address input	Ports P0, P1 ₀ -P1 ₆	A ₀ -A ₁₄
Data I/O	Port P2	D ₀ -D ₇
CE	P3 ₃	CE
OE	P3 ₄	OE

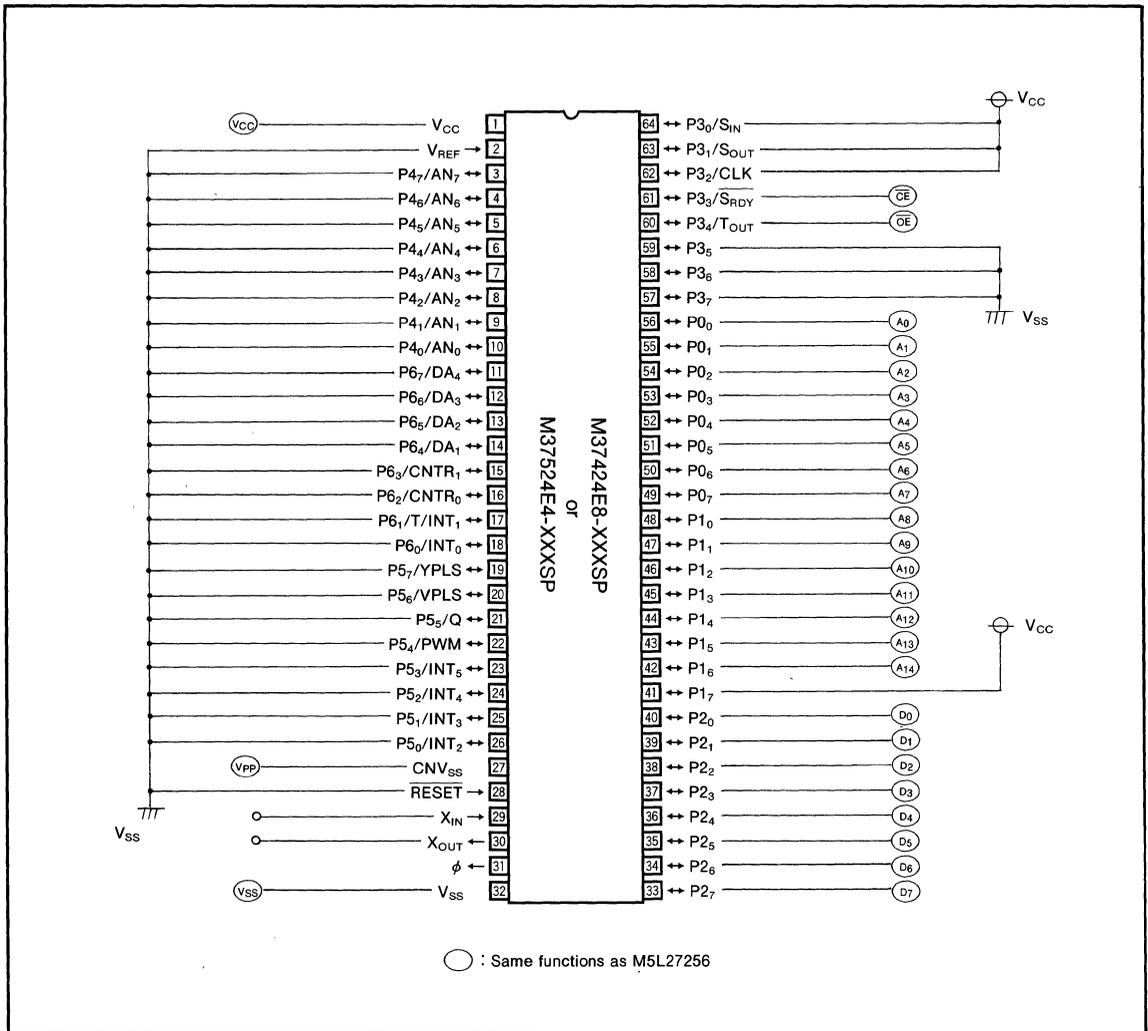


Fig.1 Pin connection in EPROM mode

PROM VERSION of M37424M8-XXXSP, M37524M4-XXXSP

PROM READING AND WRITING

Reading

To read the PROM, set the \overline{CE} and \overline{OE} pins to a "L" level. Input the address of the data (A_0-A_{14}) to be read and the data will be output to the I/O pins D_0-D_7 . The data I/O pins will be floating when either the \overline{CE} or \overline{OE} pin is in the "H" state.

Writing

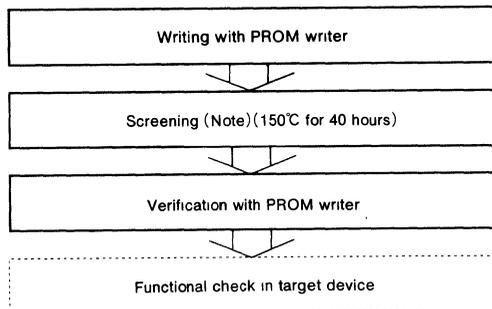
To write to the PROM, set the \overline{OE} pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0-A_{14} , and the data to be written is input to pins D_0-D_7 . Set the \overline{CE} pin to a "L" level to begin writing.

Notes on Writing

When using an PROM writer, the address range should be between 4000_{16} and $7FFF_{16}$. When data is written between addresses 0000_{16} and $7FFF_{16}$, fill addresses 0000_{16} to $3FFF_{16}$ with FF_{16} .

NOTES ON HANDLING

- (1) Since a high voltage (12.5V) is used to write data, care should be taken when turning on the PROM writer's power.
- (2) The PROM of the blank or the one-time programmable version is not tested and screened after assembly. To ensure proper operation after writing, we recommend that the procedure shown below is used to verify programming.



Note : The screening temperature is far higher than the storage temperature. Do not leave the microcomputer at 150°C for longer than 100 hours.

Table 2. I/O signal in each mode

Mode	Pin	$\overline{CE}(61)$	$\overline{OE}(60)$	$V_{PP}(27)$	$V_{CC}(1)$	Data I/O (33 to 40)
Read-out		V_{IL}	V_{IL}	V_{CC}	V_{CC}	Output
Output disable		V_{IL}	V_{IH}	V_{CC}	V_{CC}	Floating
Programming		V_{IL}	V_{IH}	V_{PP}	V_{CC}	Input
Programming verify		V_{IH}	V_{IL}	V_{PP}	V_{CC}	Output
Program disable		V_{IH}	V_{IH}	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively

MELPS 740 CPU CORE BASIC FUNCTIONS

MELPS 740

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MELPS 740 CPU CORE BASIC FUNCTIONS

Each series of the MELPS 740 Family uses the standard MELPS 740 instruction set. The functions of the MELPS 740 CPU core are explained below. The multiply and divide instructions are not available in every microcomputer, and the clock control instructions differ in each microcomputer. For details, refer to the table of machine instruction or the functional explanation of each microcomputer.

CENTRAL PROCESSING UNIT (CPU) INTERNAL REGISTERS

The central processing unit (CPU) has the six registers.

Accumulator (A)

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.

These index registers also have increment, decrement, comparison, and data transfer functions to allow these registers to take some of the functions of the accumulator.

When the T flag in the processor status register is set to

"1", the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.

The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.

The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 2.

Program counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

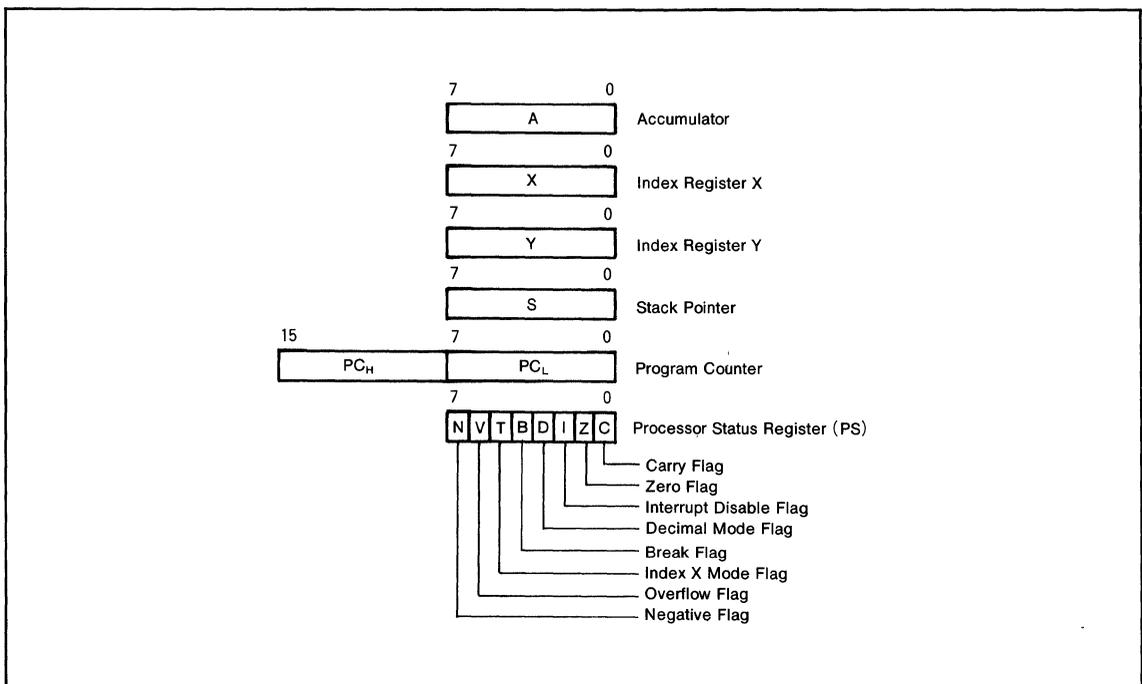


Fig. 1 MELPS 740 CPU register structure

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

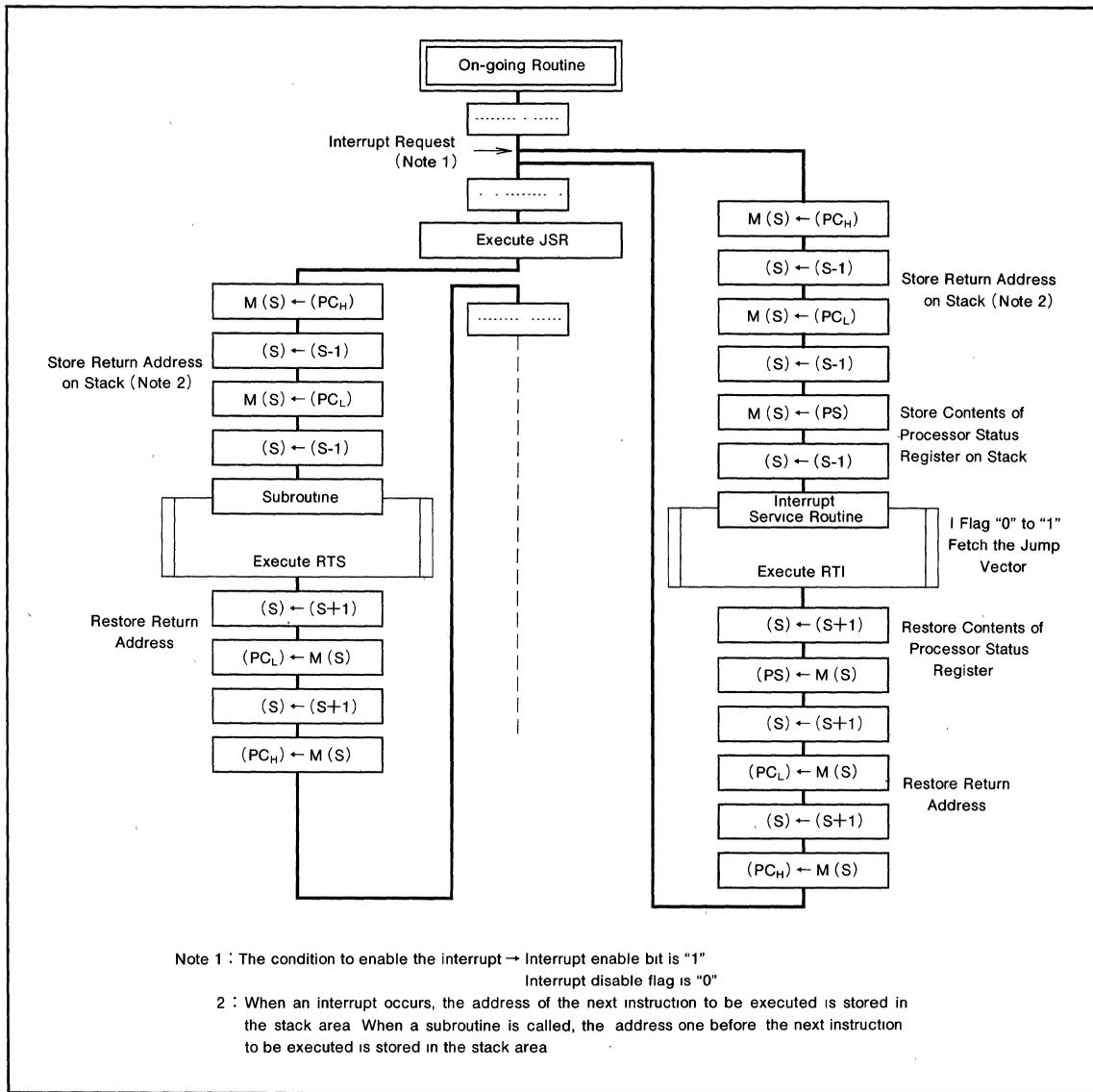


Fig. 2 Register push and pop at interrupt generation and subroutine call

Table 1. Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

After reset, the Interrupt disable (I) flag is set to "1", but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

(3) Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is "1".

When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1". Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1". The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 2. Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	—	SEI	SED	—	SET	—	—
Clear instruction	CLC	—	CLI	CLD	—	CLT	CLV	—

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ADDRESSING MODE

The MELPS 740 Family has 17 addressing modes and a powerful memory access capability.

When extracting data required for arithmetic and logic operations from memory or when storing the results of such operations in memory, a memory address must be specified. The specification of the memory address is called addressing. The MELPS 740 Family instructions can be classified as 1-byte, 2-byte, and 3-byte instructions. In each case, the first byte is known as the OPCODE which forms the basis of the instruction. A second or third byte is

called an OPERAND which affects the addressing. The contents of index registers X and Y can also effect the addressing.

Although there are many addressing modes, there is always a particular memory location specified. What differs is whether the operand, the index register contents, or a combination of both should be used to specify the memory or jump destination. Based on these 3 types of instructions, the range of variation is increased and operation is enhanced by combinations of the bit operation instructions, jump instruction, and arithmetic instructions.

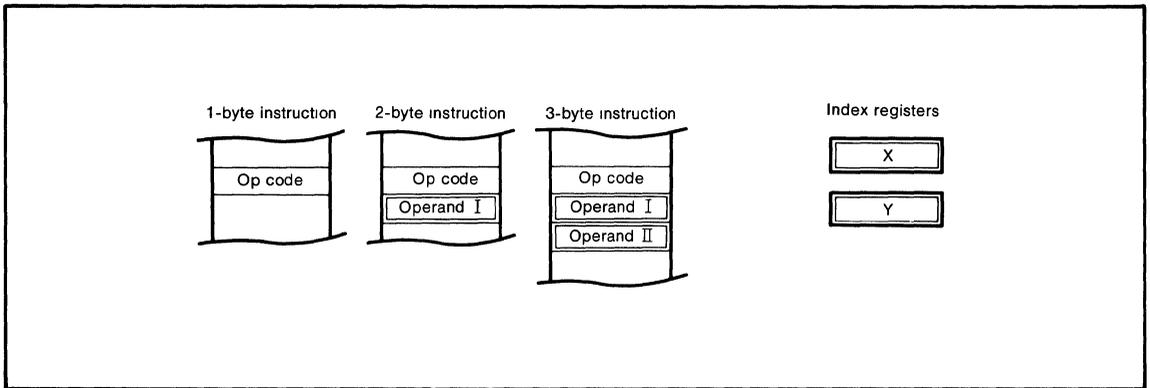
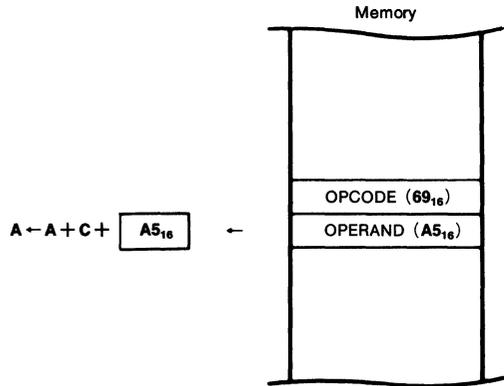


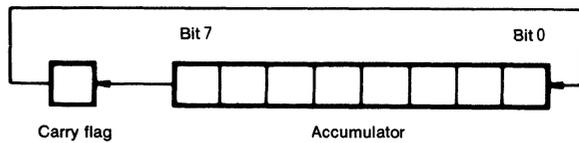
Fig. 3 Instruction byte configuration

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Immediate addressing mode
Function : The OPERAND follows immediately after the OPCODE.
Instructions : **ADC, AND, CMP, CPX, CPY, EOR, LDA, LDX, LDY, ORA, SBC**
Example : Mnemonic Machine code
ADC #\$A5 **69₁₆ A5₁₆**

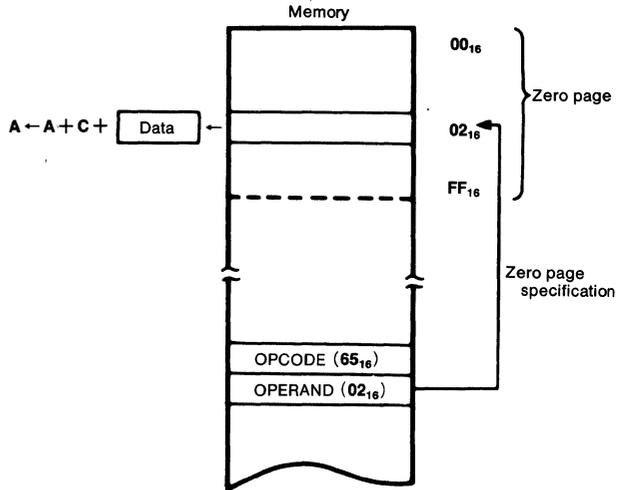


Name : Accumulator addressing mode
Function : The operation is performed on the accumulator.
Instructions : **ASL, DEC, INC, LSR, ROL, ROR**
Example : Mnemonic Machine code
ROL A **2A₁₆**

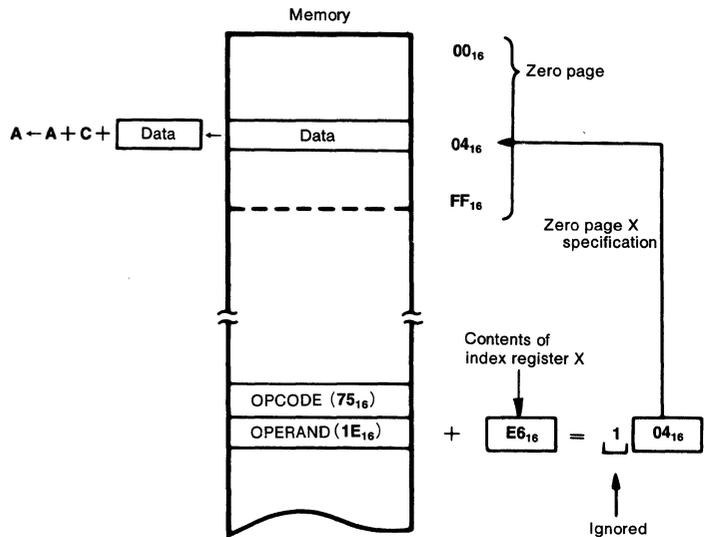


SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Zero page addressing mode
Function : The operation is performed in zero page memory (00₁₆ to FF₁₆)
Instructions : ADC, AND, ASL, BIT, CMP, COM, CPX, CPY, DEC, EOR, INC, LDA, LDM, LDX, LDY, LSR, ORA, ROL, ROR, RRF, SBC, STA, STX, STY, TST
Example : Mnemonic Machine code
 ADC \$02 65₁₆ 02₁₆



Name : Zero page X addressing mode
Function : The operation is performed on the zero page memory location whose address is specified by adding the OPERAND to the contents of index register X.
Instructions : ADC, AND, ASL, CMP, DEC, DIV, EOR, INC, LDA, LDY, LSR, MUL, ORA, ROL, ROR, SBC, STA, STY
Example : Mnemonic Machine code
 ADC \$1E,X 75₁₆ 1E₁₆

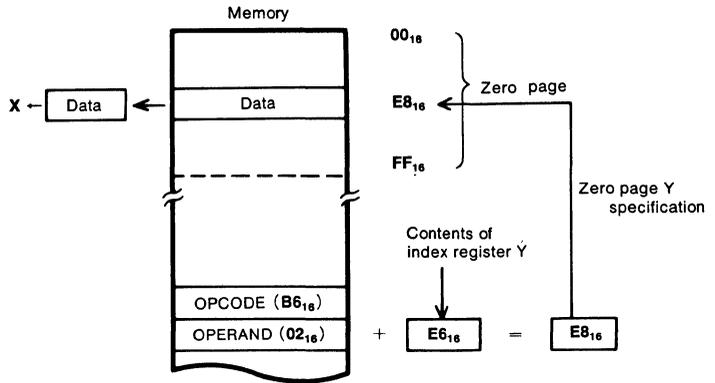


SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Zero page Y addressing mode
Function : The operation is performed on the zero page memory location whose address is specified by adding the OPERAND to the contents of index register X.

Instructions : **LDX, STX**

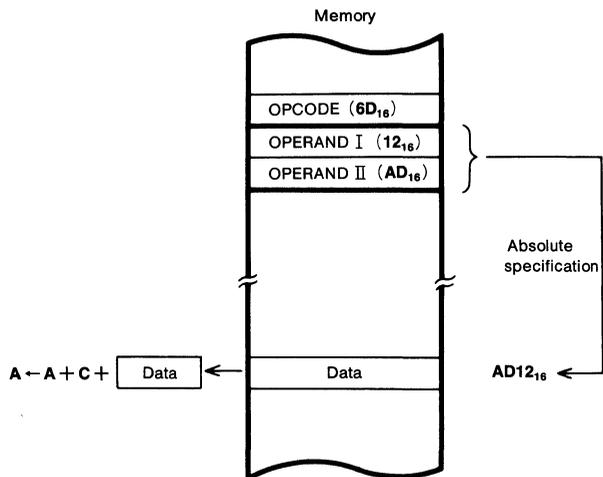
Example : Mnemonic Machine code
LDX \$02,Y **B6₁₆ 02₁₆**



Name : Absolute addressing mode
Function : The operation is performed on the memory whose address is specified by first and second OPERAND.

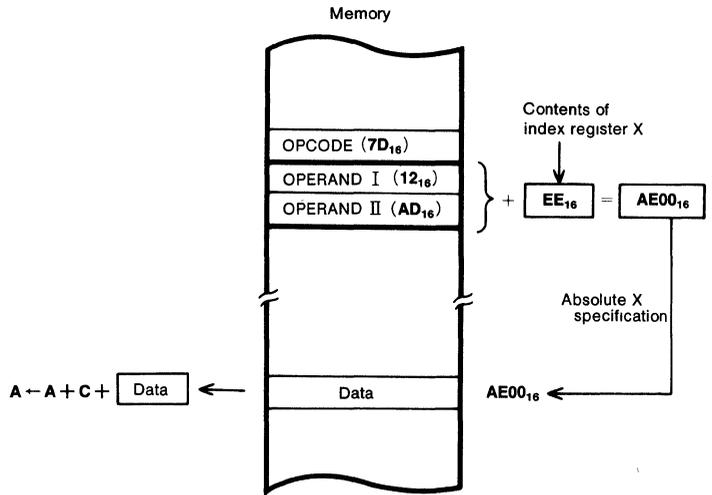
Instructions : **ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, EOR, INC, JMP, JSR, LDA, LDX, LDY, LSR, ORA, ROL, ROR, SBC, STA, STX, STY**

Example : Mnemonic Machine code
ADC \$AD12 **6D₁₆ 12₁₆ AD₁₆**

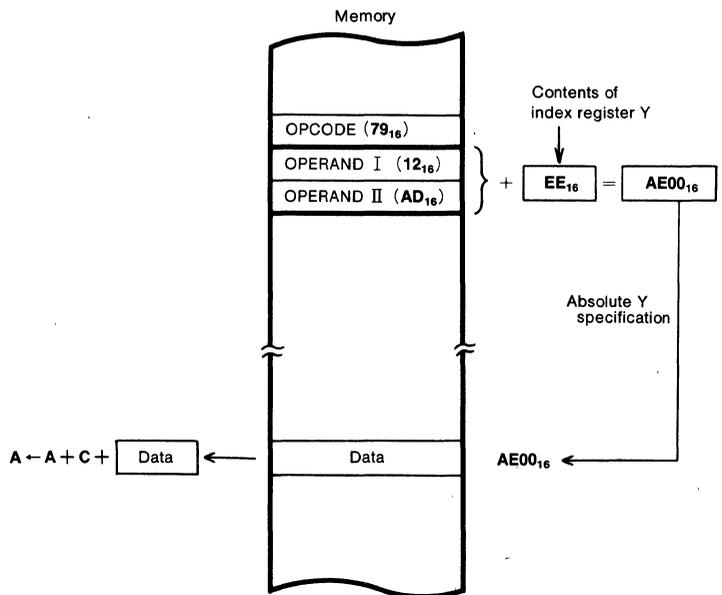


SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Absolute X addressing mode
Function : The operation is performed on the memory location whose address is specified by adding the contents of index register X to the value indicated by the first and second OPERAND.
Instructions : **ADC, AND, ASL, CMP, DEC, EOR, INC, LDA, LDY, LSR, ORA, ROL, ROR, SBC, STA**
Example : Mnemonic Machine code
ADC \$AD12,X $7D_{16} 12_{16} AD_{16}$

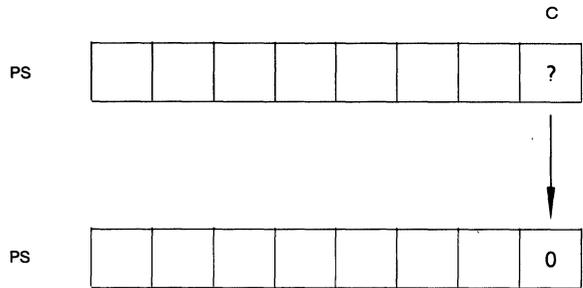


Name : Absolute Y addressing mode
Function : The operation is performed on the memory location whose address is specified by adding the contents of index register Y to the value indicated by the first and second OPERAND.
Instructions : **ADC, AND, CMP, EOR, LDA, LDX, ORA, SBC, STA**
Example : Mnemonic Machine code
ADC \$AD12,Y $79_{16} 12_{16} AD_{16}$



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Implied addressing mode
Function : Implied addressing mode operations need no OPERAND.
Instructions : **BRK, CLC, CLD, CLI, CLT, CLV, DEX, DEY, FST, INX, INY, NOP, PHA, PHP, PLA, PLP, RTI, RTS, SEC, SED, SEI, SET, SLW, STP, TAX, TAY, TSX, TXA, TXS, TYA, WIT**
Example : Mnemonic Machine code
CLC **18₁₆**

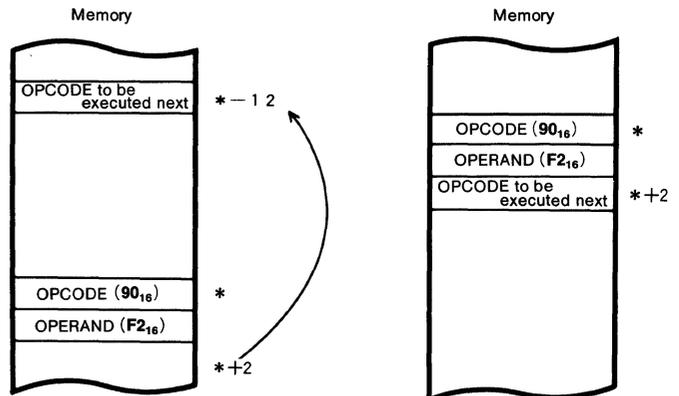


Carry flag reset

Name : Relative addressing mode
Function : Conditionally jumps to the address produced by adding the Program Counter to the OPERAND.
Instructions : **BCC, BCS, BEQ, BMI, BNE, BPL, BRA, BVC, BVS**
Example : Mnemonic Machine code
BCC * -12 90₁₆ F2₁₆

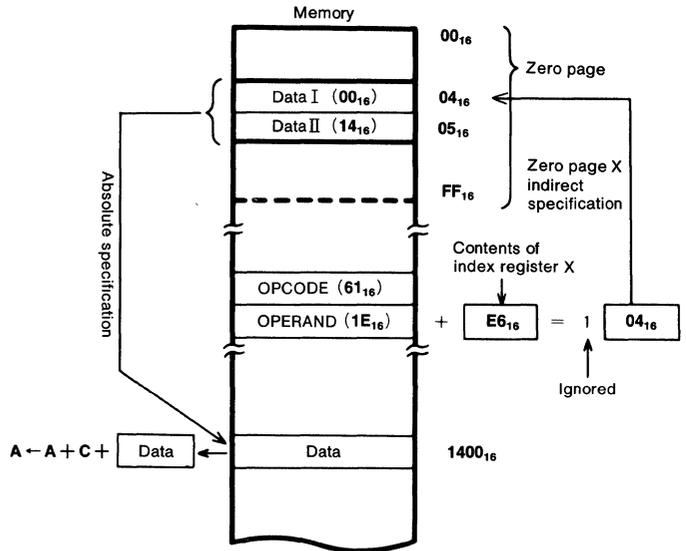
Jumps to * -12 address when carry flag(C) is cleared.

Proceed to next address when carry flag(C) is set.



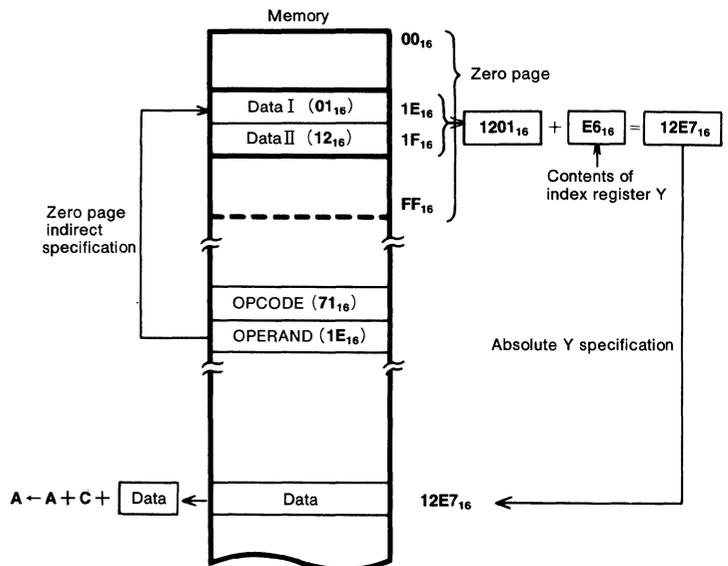
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Indirect X addressing mode
Function : The operation is performed on the memory location indicated by the contents of two consecutive bytes in zero page memory whose first address is specified by adding the OPERAND and the contents of index register X.
Instructions : **ADC, AND, CMP, EOR, LDA, ORA, SBC, STA**
Example : Mnemonic Machine code
ADC (\$1E,X) 61₁₆ 1E₁₆



In this example, data I (00₁₆) and data II (14₁₆) have been stored beforehand.

Name : Indirect Y addressing mode
Function : The operation is performed on the memory location indicated by adding the contents of index register Y to the contents of two consecutive bytes in zero page memory whose first address is specified by the OPERAND.
Instructions : **ADC, AND, CMP, EOR, LDA, ORA, SBC, STA**
Example : Mnemonic Machine code
ADC (\$1E),Y 71₁₆ 1E₁₆



In this example, data I (01₁₆) and Data II (12₁₆) have been stored beforehand.

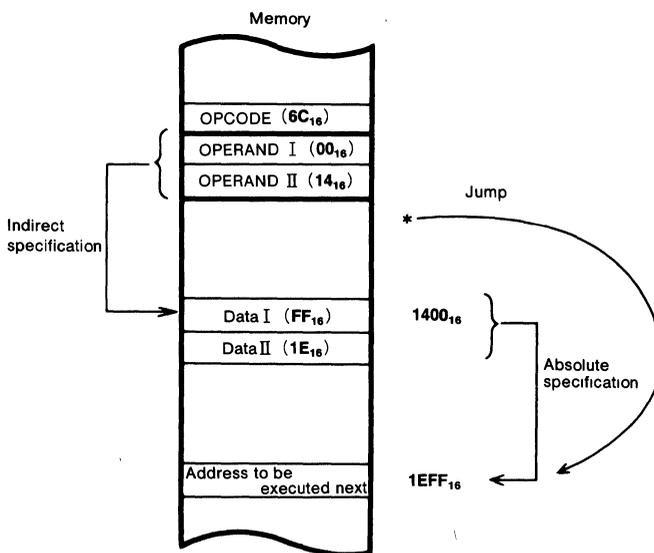
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Indirect absolute addressing mode

Function : Jumps to the location specified by the contents of two consecutive bytes whose first address is specified by the first and second OPERAND.

Instructions : **JMP**

Example : Mnemonic Machine code
JMP (\$1400) **6C₁₆ 00₁₆ 14₁₆**



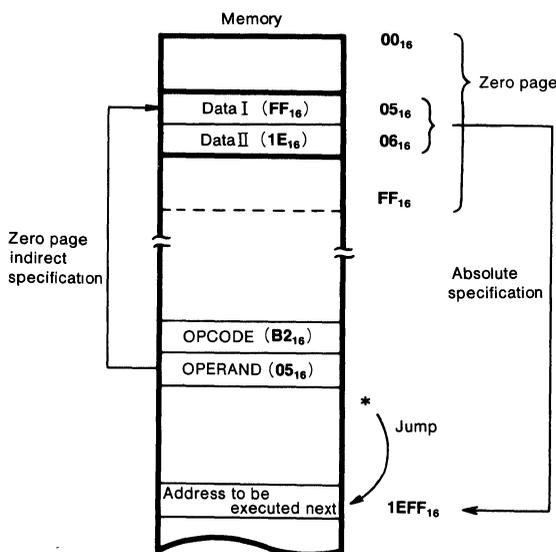
In this example, FF₁₆ as data I and 1E₁₆ as data II have been stored beforehand.

Name : Zero page indirect absolute addressing mode

Function : Jumps to the location specified by the contents of two consecutive bytes in zero page memory whose first address is specified by the OPERAND.

Instructions : **JMP, JSR**

Example : Mnemonic Machine code
JMP (\$05) **B2₁₆ 05₁₆**



In this example, FF₁₆ as data I and 1E₁₆ as data II have been stored beforehand.

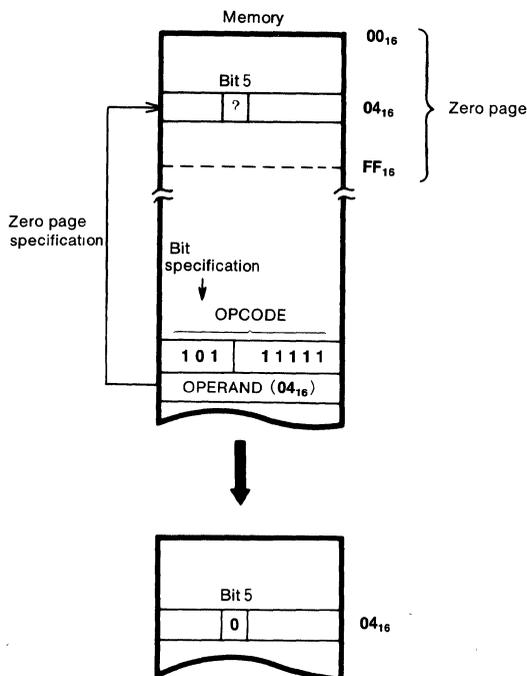
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Zero page bit addressing mode

Function : The operation is performed on the bit (specified by the three high order bits of the OPCODE), on the zero page memory location specified by the OPERAND.

Instructions : **CLB, SEB**

Example : Mnemonic Machine code
CLB 5, \$04 **BF₁₆ 04₁₆**



Name : Zero page bit relative addressing mode

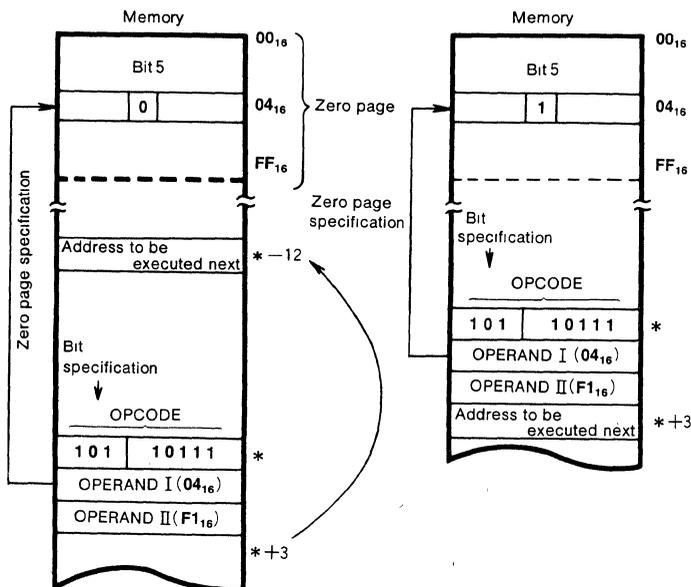
Function : Conditionally jumps to the address specified by adding the second OPERAND to the program counter, depending on the bit (specified by the three higher order bits of the OPCODE) in the zero page memory location specified by the first OPERAND.

Instructions : **BBC, BBS**

Example : Mnemonic Machine code
BBC 5, \$04, * -12 **B7₁₆ 04₁₆ F1₁₆**

Jump to * -12 address when 04₁₆ address bit 5 is cleared.

Advance to * +3 address when 04₁₆ address bit 5 is set.



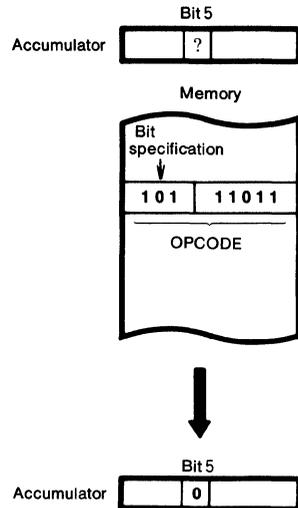
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Accumulator bit addressing mode

Function : The operation is performed on the bit in the accumulator which is specified by the three high order bits of the OPCODE. There is no OPERAND.

Instructions : **CLB, SEB**

Example : Mnemonic Machine code
CLB 5,A **BB₁₆**



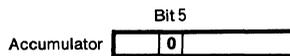
Name : Accumulator bit relative addressing mode

Function : Conditionally jumps to the address produced by adding the OPERAND to the program counter, depending on the bit in accumulator (specified by the high order three bits of the OPCODE).

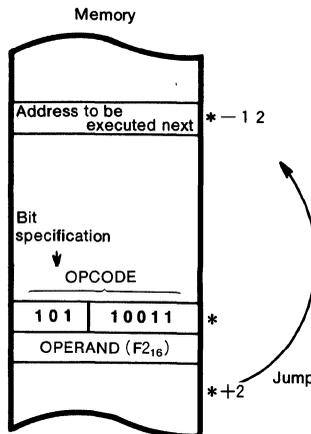
Instructions : **BBC, BBS**

Example : Mnemonic Machine code
BBC 5,A,*-12 **B3₁₆ F2₁₆**

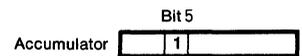
When accumulator bit 5 is cleared



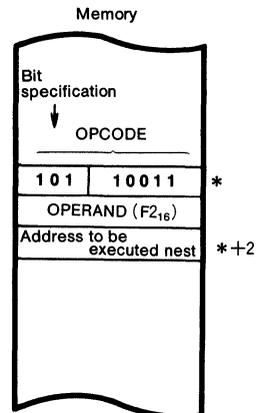
Jump to *-12 address



When accumulator bit 5 is set



Jump to *+2 address



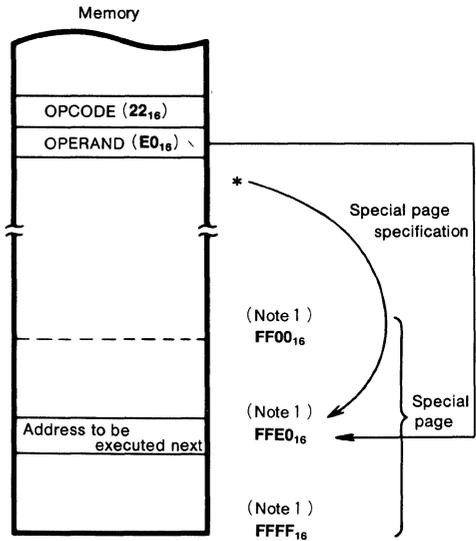
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Name : Special page addressing mode
Function : Jumps to the specified address in the special page area. The lower eight bits are specified by the OPERAND and the upper eight bits are defined by the special page (see Note 1).

Instructions : JSR

Example : Mnemonic Machine code
JSR \ \$FFE0 22₁₆ E0₁₆

Note 1 : Note that the special page is defined as the highest addressable 256 bytes of any given microcomputer and may be "FF₁₆", "1F₁₆", "2F₁₆", etc



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

LIST OF INSTRUCTION CODES

D ₇ ~D ₄ / D ₃ ~D ₀ Hexadecimal notation		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	BRK	ORA	JSR	BBS	—	ORA	ASL	BBS	PHP	ORA	ASL	SEB	—	ORA	ASL	SEB
		IND, X	ZP, IND	0, A	—	ZP	ZP	0, ZP	—	—	IMM	A	0, A	—	ABS	ABS	0, ZP
0001	1	BPL	ORA	CLT	BBC	—	ORA	ASL	BBC	CLC	ORA	DEC	CLB	—	ORA	ASL	CLB
		IND, Y	—	0, A	—	ZP, X	ZP, X	0, ZP	—	—	ABS, Y	A	0, A	—	ABS, X	ABS, X	0, ZP
0010	2	JSR	AND	JSR	BBS	BIT	AND	ROL	BBS	PLP	AND	ROL	SEB	BIT	AND	ROL	SEB
		ABS	IND, X	SP	1, A	ZP	ZP	ZP	1, ZP	—	IMM	A	1, A	—	ABS	ABS	ABS
0011	3	BMI	AND	SET	BBC	—	AND	ROL	BBC	SEC	AND	INC	CLB	LDM	AND	ROL	CLB
		IND, Y	—	1, A	—	ZP, X	ZP, X	1, ZP	—	—	ABS, Y	A	1, A	ZP	ABS, X	ABS, X	1, ZP
0100	4	RTI	EOR	STP	BBS	COM	EOR	LSR	BBS	PHA	EOR	LSR	SEB	JMP	EOR	LSR	SEB
		IND, X	(Note)	2, A	ZP	ZP	ZP	2, ZP	—	—	IMM	A	2, A	—	ABS	ABS	ABS
0101	5	BVC	EOR	—	BBC	—	EOR	LSR	BBC	CLI	EOR	—	CLB	—	EOR	LSR	CLB
		IND, Y	—	2, A	—	ZP, X	ZP, X	2, ZP	—	—	ABS, Y	—	2, A	—	ABS, X	ABS, X	2, ZP
0110	6	RTS	ADC	MUL	BBS	TST	ADC	ROR	BBS	PLA	ADC	ROR	SEB	JMP	ADC	ROR	SEB
		IND, X	(Note)	3, A	ZP	ZP	ZP	3, ZP	—	—	IMM	A	3, A	IND	ABS	ABS	3, ZP
0111	7	BVS	ADC	—	BBC	—	ADC	ROR	BBC	SEI	ADC	—	CLB	—	ADC	ROR	CLB
		IND, Y	—	3, A	—	ZP, X	ZP, X	3, ZP	—	—	ABS, Y	—	3, A	—	ABS, X	ABS, X	3, ZP
1000	8	BRA	STA	RRF	BBS	STY	STA	STX	BBS	DEY	—	TXA	SEB	STY	STA	STX	SEB
		IND, X	ZP	4, A	ZP	ZP	ZP	4, ZP	—	—	—	—	TXA	4, A	ABS	ABS	ABS
1001	9	BCC	STA	—	BBC	STY	STA	STX	BBC	TYA	STA	TXS	CLB	—	STA	—	CLB
		IND, Y	—	4, A	ZP, X	ZP, X	ZP, Y	4, ZP	—	—	ABS, Y	TXS	4, A	—	ABS, X	—	4, ZP
1010	A	LDY	LDA	LDX	BBS	LDY	LDA	LDX	BBS	TAY	LDA	TAX	SEB	LDY	LDA	LDX	SEB
		IMM	IND, X	IMM	5, A	ZP	ZP	ZP	5, ZP	—	IMM	—	TAX	5, A	ABS	ABS	ABS
1011	B	BCS	LDA	JMP	BBC	LDY	LDA	LDX	BBC	CLV	LDA	TSX	CLB	LDY	LDA	LDX	CLB
		IND, Y	ZP, IND	5, A	ZP, X	ZP, X	ZP, Y	5, ZP	—	—	ABS, Y	TSX	5, A	ABS, X	ABS, X	ABS, Y	5, ZP
1100	C	CPY	CMP	SLW	BBS	CPY	CMP	DEC	BBS	INY	CMP	DEX	SEB	CPY	CMP	DEC	SEB
		IMM	IND, X	(Note) WIT	6, A	ZP	ZP	ZP	6, ZP	—	IMM	—	DEX	6, A	ABS	ABS	ABS
1101	D	BNE	CMP	—	BBC	—	CMP	DEC	BBC	CLD	CMP	—	CLB	—	CMP	DEC	CLB
		IND, Y	—	6, A	—	ZP, X	ZP, X	6, ZP	—	—	ABS, Y	—	6, A	—	ABS, X	ABS, X	6, ZP
1110	E	CPX	SBC	FST	BBS	CPX	SBC	INC	BBS	INX	SBC	NOP	SEB	CPX	SBC	INC	SEB
		IMM	IND, X	(Note) DIV	7, A	ZP	ZP	ZP	7, ZP	—	IMM	—	NOP	7, A	ABS	ABS	ABS
1111	F	BEQ	SBC	—	BBC	—	SBC	INC	BBC	SED	SBC	—	CLB	—	SBC	INC	CLB
		IND, Y	—	7, A	—	ZP, X	ZP, X	7, ZP	—	—	ABS, Y	—	7, A	—	ABS, X	ABS, X	7, ZP

Note Support of these instructions depends on the microcomputer type

Instruction	Supported in the following microcomputer types
FST SLW	M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, M50758-XXXSP
MUL DIV	Series 7450, Series 38000, M37424M8-XXXSP, M37524M4-XXXSP

Instruction	Not supported in the following microcomputer types
WIT	M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, M50758-XXXSP
STP	M50752-XXXSP, M50757-XXXSP, M50758-XXXSP, M37424M8-XXXSP, M37524M4-XXXSP

- 3-byte instruction
- 2-byte instruction
- 1-byte instruction

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MACHINE INSTRUCTIONS

Symbol	Function	Details	Addressing mode																				
			IMP			IMM			A			BIT,A			ZP			BIT,ZP					
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#			
ADC (Note 1) (Note 6)	When T=0 $A \leftarrow A + M + C$ When T=1 $M(X) \leftarrow M(X) + M + C$	Adds the carry, accumulator and memory contents. The results are entered into the accumulator. Adds the contents of the memory in the address indicated by index register X, the contents of the memory specified by the addressing mode and the carry. The results are entered into the memory at the address indicated by index register X.				69	2	2										65	3	2			
AND (Note 1)	When T=0 $A \leftarrow A \wedge M$ When T=1 $M(X) \leftarrow M(X) \wedge M$	"AND's" the accumulator and memory contents. The results are entered into the accumulator. "AND's" the contents of the memory of the address indicated by index register X and the contents of the memory specified by the addressing mode. The results are entered into the memory at the address indicated by index register X.				29	2	2										25	3	2			
ASL	$7 \quad 0$ $C \leftarrow \boxed{} \leftarrow 0$	Shifts the contents of accumulator or contents of memory one bit to the left. The low order bit of the accumulator or memory is cleared and the high order bit is shifted into the carry flag.							0A	2	1							06	5	2			
BBC (Note 4)	A_b or $M_b = 0?$	Branches when the contents of the bit specified in the accumulator or memory is "0".										13 $\pm 2i$	4	2				17 $\pm 2i$	5	3			
BBS (Note 4)	A_b or $M_b = 1?$	Branches when the contents of the bit specified in the accumulator or memory is "1".										03 $\pm 2i$	4	2				07 $\pm 2i$	5	3			
BCC (Note 4)	$C = 0?$	Branches when the contents of carry flag is "0".																					
BCS (Note 4)	$C = 1?$	Branches when the contents of carry flag is "1".																					
BEQ (Note 4)	$Z = 1?$	Branches when the contents of zero flag is "1".																					
BIT	$A \wedge M$	"AND's" the contents of accumulator and memory. The results are not entered anywhere.																24	3	2			
BMI (Note 4)	$N = 1?$	Branches when the contents of negative flag is "1".																					
BNE (Note 4)	$Z = 0?$	Branches when the contents of zero flag is "0".																					
BPL (Note 4)	$N = 0?$	Branches when the contents of negative flag is "0".																					
BRA	$PC \leftarrow PC \pm \text{offset}$	Jumps to address specified by adding offset to the program counter.																					
BRK	B-1 $M(S) \leftarrow PC_H$ $S \leftarrow S - 1$ $M(S) \leftarrow PC_L$ $S \leftarrow S - 1$ $M(S) \leftarrow PS$ $S \leftarrow S - 1$ $PC_L \leftarrow AD_L$ $PC_H \leftarrow AD_H$	Executes a software interrupt.	00	7	1																		

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Symbol	Function	Details	Addressing mode																		
			IMP			IMM			A			BIT,A			ZP			BIT,ZP			
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	
PHA	$M(S) \leftarrow A$ $S \leftarrow S-1$	Saves the contents of the accumulator in memory at the address indicated by the stack pointer and decrements the contents of stack pointer by 1	48	3	1																
PHP	$M(S) \leftarrow PS$ $S \leftarrow S-1$	Saves the contents of the processor status register in memory at the address indicated by the stack pointer and decrements the contents of the stack pointer by 1	08	3	1																
PLA	$S \leftarrow S+1$ $A \leftarrow M(S)$	Increments the contents of the stack pointer by 1 and restores the accumulator from the memory at the address indicated by the stack pointer	68	4	1																
PLP	$S \leftarrow S+1$ $PS \leftarrow M(S)$	Increments the contents of stack pointer by 1 and restores the processor status register from the memory at the address indicated by the stack pointer	28	4	1																
ROL		Shifts the contents of the memory or accumulator to the left by one bit. The high order bit is shifted into the carry flag and the carry flag is shifted into the low order bit.							2A	2	1				26	5	2				
ROR		Shifts the contents of the memory or accumulator to the right by one bit. The low order bit is shifted into the carry flag and the carry flag is shifted into the high order bit.							6A	2	1				66	5	2				
RRF		Rotates the contents of memory to the right by 4 bits.													82	8	2				
RTI	$S \leftarrow S+1$ $PS \leftarrow M(S)$ $S \leftarrow S+1$ $PC_L \leftarrow M(S)$ $S \leftarrow S+1$ $PC_H \leftarrow M(S)$	Returns from an interrupt routine to the main routine.	40	6	1																
RTS	$S \leftarrow S+1$ $PC_L \leftarrow M(S)$ $S \leftarrow S+1$ $PC_H \leftarrow M(S)$	Returns from a subroutine to the main routine.	60	6	1																
SBC (Note 1) (Note 6)	When $T=0$ $A \leftarrow A - M - \bar{C}$ When $T=1$ $M(X) \leftarrow M(X) - M - \bar{C}$	Subtracts the contents of memory and complement of carry flag from the contents of accumulator. The results are stored into the accumulator. The results are stored into the memory of the address indicated by index register X.							E9	2	2				E5	3	2				
SEB	A_b or $M_b \leftarrow 1$	Sets the specified bit in the accumulator or memory to "1".												0B 2i	2	1			0F 2i	5	2
SEC	$C \leftarrow 1$	Sets the contents of the carry flag to "1".	38	2	1																
SED	$D \leftarrow 1$	Sets the contents of the decimal mode flag to "1".	F8	2	1																
SEI	$I \leftarrow 1$	Sets the contents of the interrupt disable flag to "1".	78	2	1																
SET	$T \leftarrow 1$	Sets the contents of the index X mode flag to "1".	32	2	1																
SLW (Note 5)		Disconnects the oscillator output from the X_{OUT} pin.	C2	2	1																

NOTES on USE

Keep the following points in mind while programming:

Processor status register

(1) Initialization of processor status register

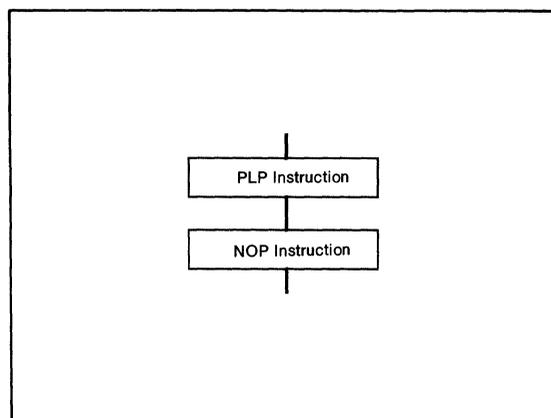
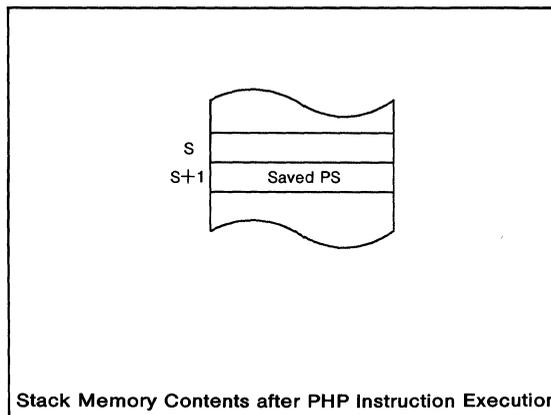
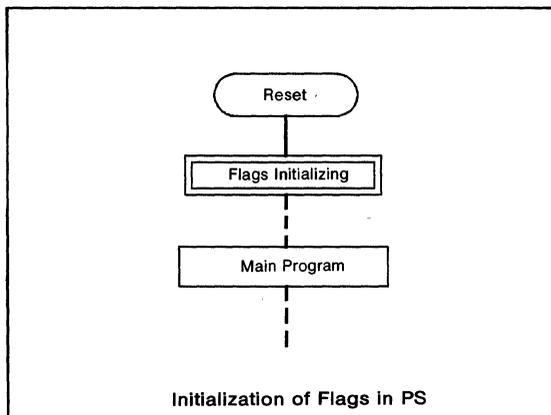
After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1". Therefore, flags which affect program execution must be initialized after a reset.

In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

(2) How to reference the processor status register

To reference the contents of the processor status register (PS), execute the PHP instruction once then read the contents of (S+1). If necessary, execute the PLP instruction to return the PS to its original status.

A NOP instruction should be executed after every PLP instruction. (The NOP is unnecessary when using a series 38000 microcomputer).



Interrupts

The contents of the interrupt request bits can be changed by software, but the values will not change immediately after being overwritten. Therefore, note the following points:

- (1) After changing the value of the interrupt request bits, execute at least one instruction before executing a BBC, BBS, or any other read instruction.
- (2) When clearing an interrupt request bit to "0" and setting an interrupt enable bit to "1" (=setting in an interrupt enable state), it needs to be cleared or set these bits in a separate instruction. The interrupt is accepted because it becomes in the interrupt enable state before clearing the interrupt request bit, if clearing the interrupt request bit and setting the interrupt enable bit are performed in an instruction.

BRK instruction

- (1) It can be detected that the BRK instruction interrupt event or the least priority interrupt event by referring the stored B flag state. Refer the stored B flag state in the interrupt routine, in this case.

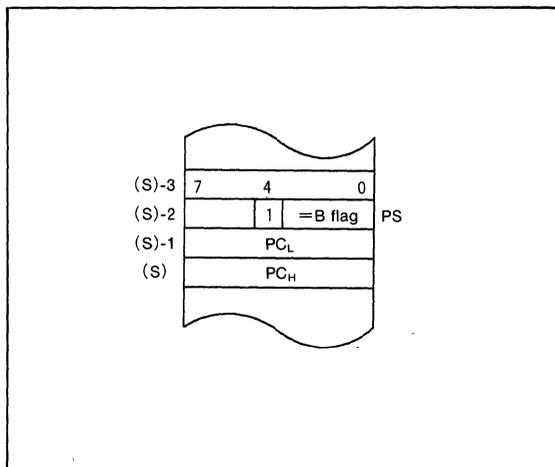
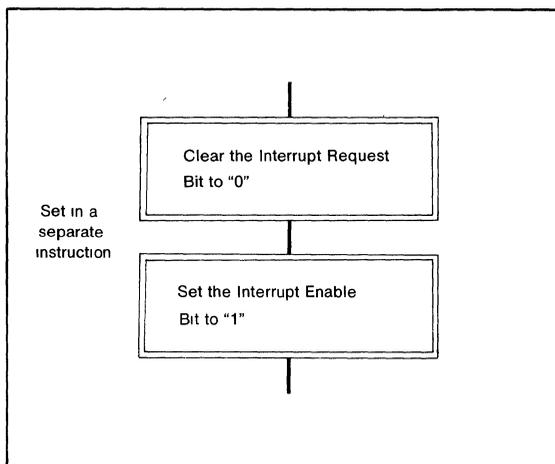
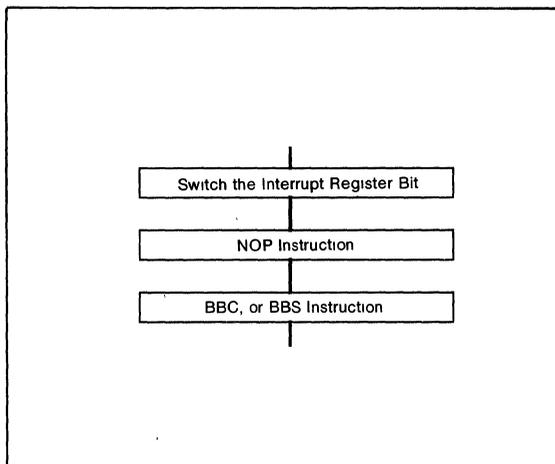
However, the microcomputer that has an independent BRK instruction interrupt vector (cf. the 7450 series, the 7470 series, and the 38000 series) are not necessary this detection.

- (2) The CPU of all 8-bit microcomputers except the 38000 series have the following bug about the BRK instruction execution.

At the following status,

- ① the interrupt request bit has set to "1".
- ② the interrupt enable bit has set to "1".
- ③ the interrupt disable flag (I) has set to "1".

if the BRK instruction is executed, the interrupt disable state is cancelled and it becomes in the interrupt enable state. So that the requested interrupts (the interrupts that corresponding to their request bits have set to "1") are accepted.



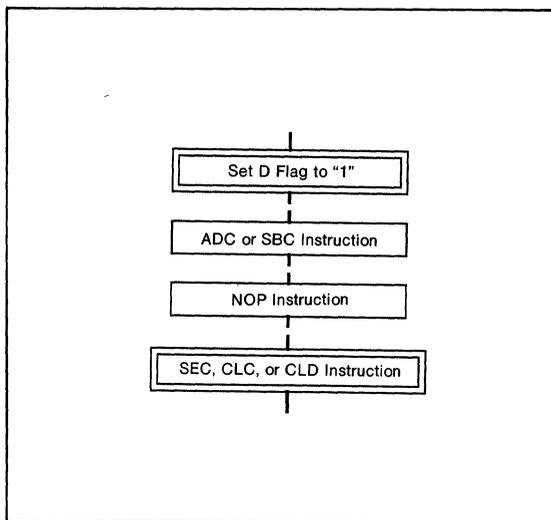
Decimal calculations

(1) Execution of decimal calculations

The ADC and SBC are the only instructions which will yield proper decimal results in decimal mode. To calculate in decimal notation, set the decimal mode flag (D) to "1" with the SED instruction. After executing the ADC or SBC instruction, execute another instruction before executing the SEC, CLC, or CLD instruction.

(2) Note on flags in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a ADC or SBC instruction is executed. The Carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or is cleared to "0" if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to "0" before each calculation. To check for a borrow, the C flag must be initialized to "1" before each calculation.



JMP instruction

When using the JMP instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

APPENDICES

SERIES MELPS 740 MASK ROM ORDERING METHOD

SERIES MELPS 740 MASK ROM ORDERING METHOD

Mitsubishi Electric corp. accepts order to transfer EPROM supplied program data into the mask ROM in single-chip 8-bit microcomputers.

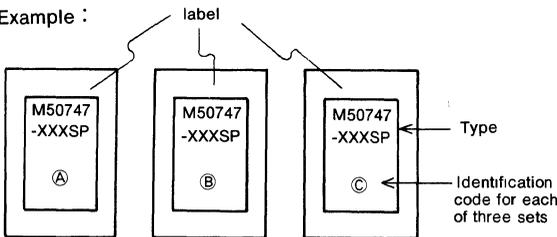
When placing such order, please submit the information described below.

- (1) Mask ROM confirmation form.....1 set
(There is a specific form to be used for each model.)
- (2) Data to be written into mask ROM..... EPROM
(Please provide three sets containing the identical data.)
- (3) Mark specification form.....1 set

NOTES

- (1) Acceptable EPROM type
Any EPROM made by Mitsubishi that is listed in the mask ROM confirmation form may be used.
- (2) EPROM window labeling
Please write the model name and the identification code (A, B, C) on the label for each of the three sets of data EPROMs provided.

Example :



- (3) Calculation and indication of checksum code
Please calculate the total number of data in words in the EPROM, and write the number in 4-digit hexadecimal form in the checksum code field of the mask ROM confirmation form.
- (4) Options
Refer to the appropriate data book entry and write the desired options on the mask ROM confirmation form.
- (5) Mark specification method
The permissible mark specifications differ depending on the shape of package. Please fill out the mark specification form and attach it to the mask ROM confirmation form.

OUTLINE OF ORDER PROCESSING

Mitsubishi will produce the mask ROM if at least two of the three EPROM sets submitted contain identical data.

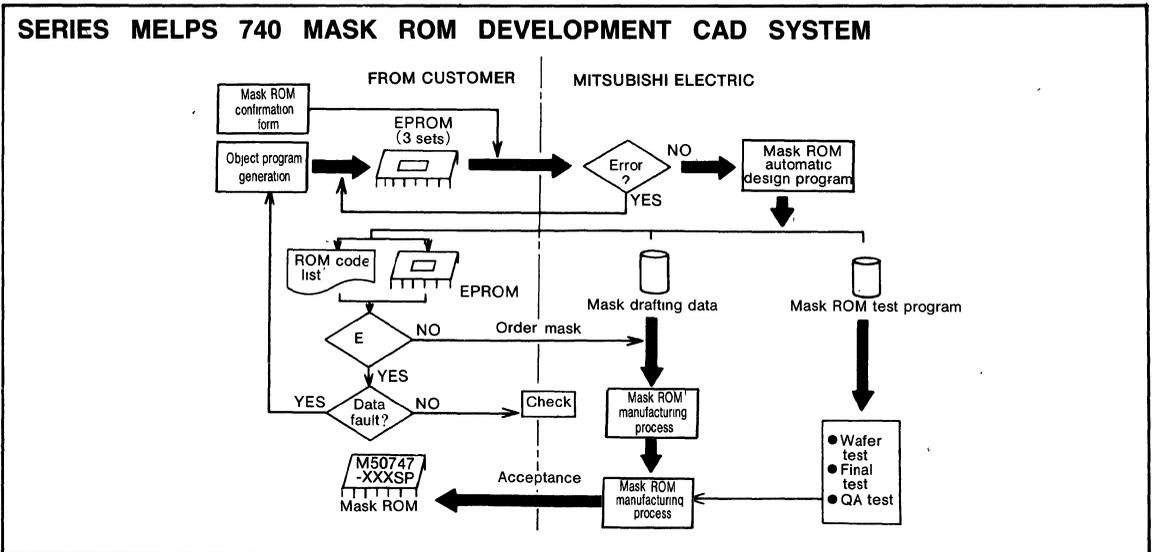
If we find error when the submitted EPROMs are compared, we will contact your representative.

Thus, we assume responsibility only when we produce the mask ROM that contain data other than the data correctly provided by the customer.

Mitsubishi uses an automatic mask ROM design program to generated the following :

1. Drafting data for mask ROM production;
2. ROM code listing or EPROM for mask ROM production error check work;
3. Mask ROM test program.

The chart below shows the flow of mask ROM production.



SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH01-46A<82B0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37100M8-XXXSP/FP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked*.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted. Three sets of EPROMs are required for each pattern (Check @ in the appropriate box). If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

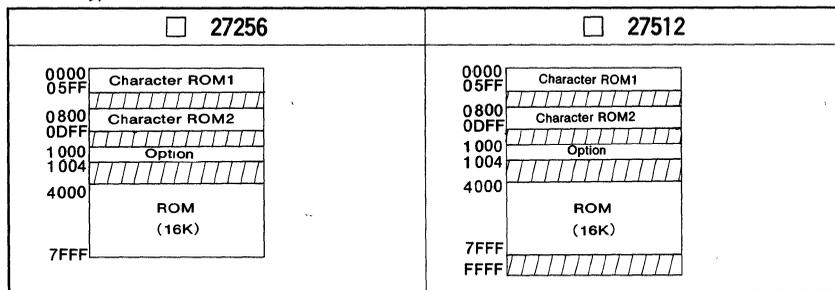
Microcomputer name : M37100M8-XXXSP M37100M8-XXXFP

Checksum code for entire EPROM

--	--	--	--

 (hexadecimal notation)

EPROM type



Set "FF₁₆" in the shaded area.

* 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37100M8-XXXSP ; 80P6 for M37100M8-XXXFP) and attach to the mask ROM confirmation form.

* 3. 1 I²C bus*
Would you use I²C bus function ? Use Not use

* 3. 2 Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—46A<82B0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37100M8-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

※ 4. Option specification.

1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

	P ₁₇	P ₁₆	P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀
address 1000 ₁₆								

2. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	P ₂₇	P ₂₆	P ₂₅	P ₂₄	P ₂₃	P ₂₂	P ₂₁	P ₂₀
address 1001 ₁₆								

3. Feedback resistors for X_{IN}, X_{CIN} oscillation (if built-in is desired write 1, if not write 0)

							X _{CIN}	X _{IN}
address 1002 ₁₆	0	0	0	0	0	0		

4. CRT display relation polarity specifier (if negative polarity is desired write 1, if positive write 0)

							H SYNC	V SYNC	R, G, B	I	OUT
address 1003 ₁₆	0	0	0								

5. ϕ output (if ϕ clock outputs in the single-chip mode write 1, if not write 0)

								ϕ
address 1004 ₁₆	0	0	0	0	0	0	0	

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH02-08A<94A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37102M8-XXXSP/FP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : M37102M8-XXXSP M37102M8-XXXFP

Checksum code for entire EPROM

--	--	--	--

 (hexadecimal notation)

EPROM type

27256

address	
0000 ₁₆	Area for ASCII codes of the name of the product 'M37102M8-'
000F ₁₆	
0010 ₁₆	
2FFF ₁₆	
3000 ₁₆	Character ROM1
37FF ₁₆	
3800 ₁₆	Character ROM2
3FFF ₁₆	
4000 ₁₆	
	ROM(16K)
7FFF ₁₆	

- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37102M8-' to addresses 0000₁₆ to 000F₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37102M8-XXXSP; 80P6N for M37102M8-XXXFP) and attach to the mask ROM confirmation form.

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH02—08A<94A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37102M8-XXXSP/FP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

- ※ 3. 1 I²C bus*
Would you use I²C bus function? Use Not use

- ※ 3. 2 OSD test character pattern input.
Write the two types of test patterns to the specified addresses.

- ※ 3. 3 Comments

Writing the name of the product and character ROM data onto EPROMs.

Addresses 0000₁₆ to 000F₁₆ store the name of the product and addresses 3000₁₆ to 3FFF₁₆ store the character ROM data. Write the following ASCII codes that indicates 'M37102M8-' to addresses 0000₁₆ to 000F₁₆.
If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code.
ASCII codes 'M37102M8-' are listed on the right.
The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'-' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	F F ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	F F ₁₆
0003 ₁₆	'1' = 3 1 ₁₆	000B ₁₆	F F ₁₆
0004 ₁₆	'0' = 3 0 ₁₆	000C ₁₆	F F ₁₆
0005 ₁₆	'2' = 3 2 ₁₆	000D ₁₆	F F ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	F F ₁₆
0007 ₁₆	'8' = 3 8 ₁₆	000F ₁₆	F F ₁₆

2. Inputting the character ROM
Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data and test character patterns, see the next page and on.

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH02—08A<94A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37102M8-XXXSP/FP MITSUBISHI ELECTRIC

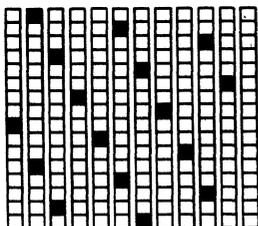
Mask ROM number	
-----------------	--

Inputting the test character pattern

Write the following character pattern to the specified addresses.

(1) Pattern 1

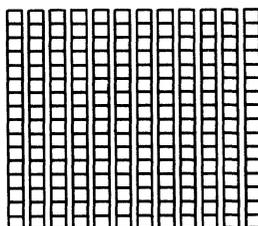
Character code "7E₁₆"



Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

(2) Pattern 2

Character code "7F₁₆"



Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—45A<82A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37103M4-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL	Issuance signature	Submitted by	Supervisor
		Date issued	Date :		()	

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM (hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128	<input type="checkbox"/> 27256	<input type="checkbox"/> 27512

Set "FF₁₆" in the shaded area.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37103M4-XXXSP) and attach to the mask ROM confirmation form.

※ 3. Comments

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—45A (82A0)

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37103M4-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

※ 4. Option specification (write the option data also at the specified address in the EPROM.)

1. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

	P ₁₀	P ₁₁	P ₁₂	P ₁₃	P ₁₄	P ₁₅	P ₁₆	P ₁₇
address 1000 ₁₆								

2. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	P ₂₀	P ₂₁	P ₂₂	P ₂₃	P ₂₄	P ₂₅	P ₂₆	P ₂₇
address 1001 ₁₆								

3. Feedback resistors for X_{IN}, X_{CIN} oscillation (if built-in is desired write 1, if not write 0)

						X _{CIN}	X _{IN}
address 1002 ₁₆	0	0	0	0	0		

4. CRT display relation polarity specifier (if negative polarity is desired write 1, if positive write 0)

				H _{SYNC}	V _{SYNC}	R, G, B	I	OUT
address 1003 ₁₆	0	0	0					

5. ϕ output (if ϕ clock outputs in the single-chip mode write 1, if not write 0)

								ϕ
address 1004 ₁₆	0	0	0	0	0	0	0	

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH01-45A<82A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37103M4-XXXSP
MITSUBISHI ELECTRIC

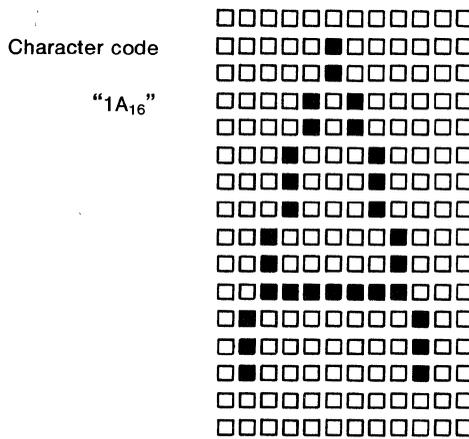
Mask ROM number	
-----------------	--

Inputting the character ROM

Input the character ROM data by dividing it into character ROM1 and character ROM2.

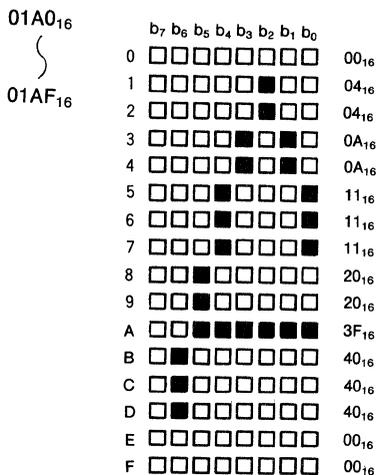
The structure of character ROM (divide of 12×16 dots font)

Example

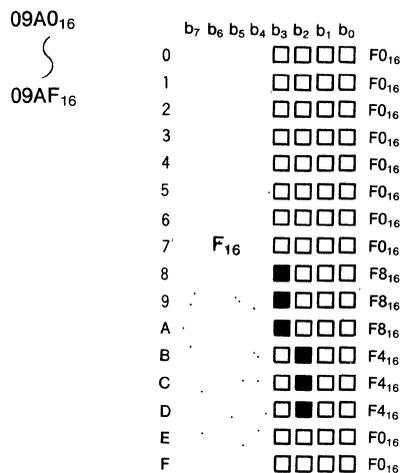


← Character ROM1 →←Character→
ROM2

Example



Example



SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH02—89A (9XA0)

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37120M6-XXXFP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1. Confirmation

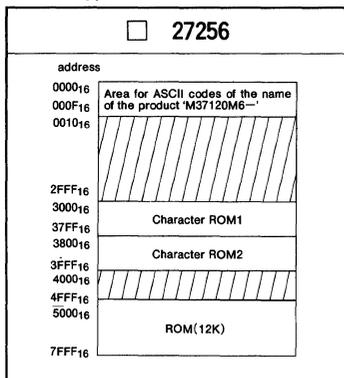
Specify the name of the product being ordered and the type of EPROMs submitted. Three sets of EPROMs are required for each pattern (Check @ in the appropriate box). If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

--	--	--	--

 (hexadecimal notation)

EPROM type



- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37120M6—' to addresses 0000₁₆ to 000F₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6N for M37120M6-XXXFP) and attach to the mask ROM confirmation form.

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH02—89A<9XA0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37120M6-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

- ※ 3. 1 OSD test character pattern input.
Write the two types of test patterns to the specified addresses.
- ※ 3. 2 Comments

Writing the name of the product and character ROM data onto EPROMs.

Addresses 0000₁₆ to 000F₁₆ store the name of the product and addresses 3000₁₆ to 3FFF₁₆ store the character ROM data. Write the following ASCII codes that indicates 'M37120M6—' to addresses 0000₁₆ to 000F₁₆. If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly. As for the option, if the contents of the cofirmation and conflict with those of the EPROMs, the contents of the EPROMs are preferred.

1. Inputting the name of the product with the ASCII code.
 ASCII codes 'M37120M6—' are listed on the right.
 The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'—' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	F F ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	F F ₁₆
0003 ₁₆	'1' = 3 1 ₁₆	000B ₁₆	F F ₁₆
0004 ₁₆	'2' = 3 2 ₁₆	000C ₁₆	F F ₁₆
0005 ₁₆	'0' = 3 0 ₁₆	000D ₁₆	F F ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	F F ₁₆
0007 ₁₆	'6' = 3 6 ₁₆	000F ₁₆	F F ₁₆

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27256
The pseudo-command	* = \$8000 .BYTE△ 'M37120M6—'

This is an example when the start address of internal ROM is F000₁₆.

2. Inputting the character ROM
 Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data and test character patterns, see the next page and on.

SERIES MELPS 740 MASK ROM ORDERING METHOD

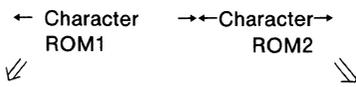
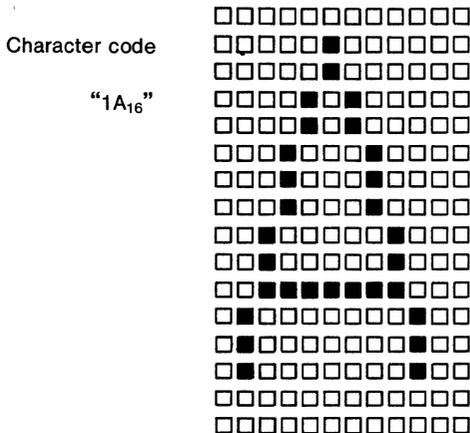
GZZ—SH02—89A (9XA0)

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37120M6-XXXFP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

The structure of character ROM (divide of 12X16 dots font)

Example



Example 31A0₁₆
31AF₁₆

	b ₇	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	b ₀	
0	□	□	□	□	□	□	□	□	00 ₁₆
1	□	□	□	□	□	□	■	□	04 ₁₆
2	□	□	□	□	□	□	■	□	04 ₁₆
3	□	□	□	□	□	■	■	□	0A ₁₆
4	□	□	□	□	□	■	□	□	0A ₁₆
5	□	□	□	□	□	□	■	■	11 ₁₆
6	□	□	□	□	□	□	■	■	11 ₁₆
7	□	□	□	□	□	□	■	■	11 ₁₆
8	□	□	■	□	□	□	□	□	20 ₁₆
9	□	□	■	□	□	□	□	□	20 ₁₆
A	□	□	■	■	■	■	■	■	3F ₁₆
B	□	■	□	□	□	□	□	□	40 ₁₆
C	□	■	□	□	□	□	□	□	40 ₁₆
D	□	■	□	□	□	□	□	□	40 ₁₆
E	□	□	□	□	□	□	□	□	00 ₁₆
F	□	□	□	□	□	□	□	□	00 ₁₆

Example 39A0₁₆
39AF₁₆

	b ₇	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	b ₀	
0									F0 ₁₆
1									F0 ₁₆
2									F0 ₁₆
3									F0 ₁₆
4									F0 ₁₆
5									F0 ₁₆
6									F0 ₁₆
7	F ₁₆								F0 ₁₆
8		■							F8 ₁₆
9		■							F8 ₁₆
A		■							F8 ₁₆
B			■						F4 ₁₆
C			■						F4 ₁₆
D			■						F4 ₁₆
E									F0 ₁₆
F									F0 ₁₆

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH02-89A<9XA0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37120M6-XXXFP MITSUBISHI ELECTRIC

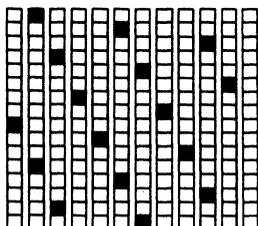
Mask ROM number	
-----------------	--

Inputting the test character pattern

Write the following character pattern to the specified addresses.

(1) Pattern 1

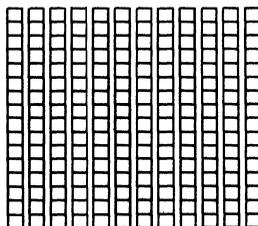
Character code "7E₁₆"



Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

(2) Pattern 2

Character code "7F₁₆"



Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH04-00A<01A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37201M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted. Three sets of EPROMs are required for each pattern (Check @ in the appropriate box). If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

--	--	--	--

(hexadecimal notation)

EPROM type

27256

address	
0000 ₁₆	Area for ASCII codes of the name of the product 'M37201M6-'
000F ₁₆	
0010 ₁₆	
0FFF ₁₆	Character ROM1
1000 ₁₆	
17FF ₁₆	Character ROM2
1800 ₁₆	
1FFF ₁₆	ROM(24K)
2000 ₁₆	
7FFF ₁₆	

- (1) Set "FF₁₆" in the shaded area
- (2) Write the ASCII codes that indicates the name of the product 'M37201M6-' to addresses 0000₁₆ to 000F₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37201M6-XXXSP) and attach to the mask ROM confirmation form.

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH04-00A<01A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37201M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number

- ※ 3. 1 I²C bus*
Would you use I²C bus function? Use Not use
- ※ 3. 2 OSD test character pattern input.
Write the two types of test patterns to the specified addresses.
- ※ 3. 3 Comments

Writing the name of the product and character ROM data onto EPROMs.

Addresses 0000₁₆ to 000F₁₆ store the name of the product and addresses 1000₁₆ to 1FFF₁₆ store the character ROM data. Write the following ASCII codes that indicates 'M37201M6-' to addresses 0000₁₆ to 000F₁₆.

If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code.
ASCII codes 'M37201M6-' are listed on the right.
The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'-' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	F F ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	F F ₁₆
0003 ₁₆	'2' = 3 2 ₁₆	000B ₁₆	F F ₁₆
0004 ₁₆	'0' = 3 0 ₁₆	000C ₁₆	F F ₁₆
0005 ₁₆	'1' = 3 1 ₁₆	000D ₁₆	F F ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	F F ₁₆
0007 ₁₆	'6' = 3 6 ₁₆	000F ₁₆	F F ₁₆

2. Inputting the character ROM
Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data and test character patterns, see the next page and on.

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

SERIES MELPS 740 MASK ROM ORDERING METHOD

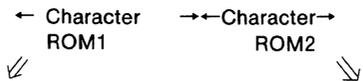
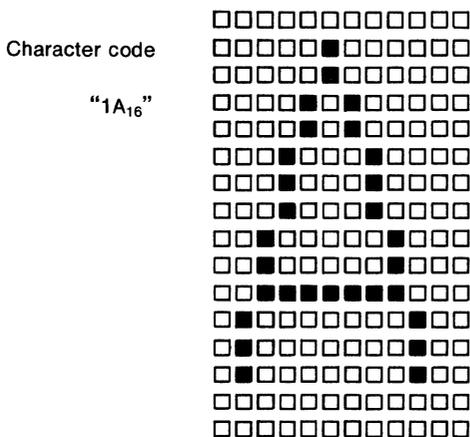
GZZ-SH04-00A<01A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37201M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

The structure of character ROM (divide of 12X16 dots font)

Example



Example

11A0 ₁₆	b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀	
} 11AF ₁₆	0	00 ₁₆
	1	04 ₁₆
	2	04 ₁₆
	3	0A ₁₆
	4	0A ₁₆
	5	11 ₁₆
	6	11 ₁₆
	7	11 ₁₆
	8	20 ₁₆
	9	20 ₁₆
	A	3F ₁₆
	B	40 ₁₆
	C	40 ₁₆
	D	40 ₁₆
	E	00 ₁₆
	F	00 ₁₆

Example

19A0 ₁₆	b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀	
} 19AF ₁₆	0	F0 ₁₆
	1	F0 ₁₆
	2	F0 ₁₆
	3	F0 ₁₆
	4	F0 ₁₆
	5	F0 ₁₆
	6	F0 ₁₆
	7	F ₁₆
	8	F8 ₁₆
	9	F8 ₁₆
	A	F8 ₁₆
	B	F4 ₁₆
	C	F4 ₁₆
	D	F4 ₁₆
	E	F0 ₁₆
	F	F0 ₁₆

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH04-00A<01A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37201M6-XXXSP MITSUBISHI ELECTRIC

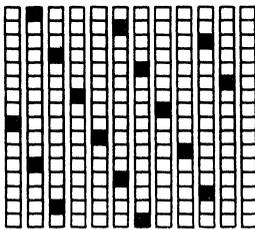
Mask ROM number	
-----------------	--

Inputting the test character pattern

Write the following character pattern to the specified addresses.

(1) Pattern 1

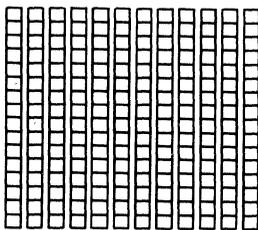
Character code "7E₁₆"



Address	Data	Address	Data
17E0 ₁₆	40 ₁₆	1FE0 ₁₆	F0 ₁₆
17E1 ₁₆	04 ₁₆	1FE1 ₁₆	F0 ₁₆
17E2 ₁₆	00 ₁₆	1FE2 ₁₆	F4 ₁₆
17E3 ₁₆	20 ₁₆	1FE3 ₁₆	F0 ₁₆
17E4 ₁₆	02 ₁₆	1FE4 ₁₆	F0 ₁₆
17E5 ₁₆	00 ₁₆	1FE5 ₁₆	F2 ₁₆
17E6 ₁₆	10 ₁₆	1FE6 ₁₆	F0 ₁₆
17E7 ₁₆	01 ₁₆	1FE7 ₁₆	F0 ₁₆
17E8 ₁₆	80 ₁₆	1FE8 ₁₆	F0 ₁₆
17E9 ₁₆	08 ₁₆	1FE9 ₁₆	F0 ₁₆
17EA ₁₆	00 ₁₆	1FEA ₁₆	F8 ₁₆
17EB ₁₆	40 ₁₆	1FEB ₁₆	F0 ₁₆
17EC ₁₆	04 ₁₆	1FEC ₁₆	F0 ₁₆
17ED ₁₆	00 ₁₆	1FED ₁₆	F4 ₁₆
17EE ₁₆	20 ₁₆	1FEE ₁₆	F0 ₁₆
17EF ₁₆	02 ₁₆	1FEF ₁₆	F0 ₁₆

(2) Pattern 2

Character code "7F₁₆"



Address	Data	Address	Data
17F0 ₁₆	00 ₁₆	1FF0 ₁₆	F0 ₁₆
17F1 ₁₆	00 ₁₆	1FF1 ₁₆	F0 ₁₆
17F2 ₁₆	00 ₁₆	1FF2 ₁₆	F0 ₁₆
17F3 ₁₆	00 ₁₆	1FF3 ₁₆	F0 ₁₆
17F4 ₁₆	00 ₁₆	1FF4 ₁₆	F0 ₁₆
17F5 ₁₆	00 ₁₆	1FF5 ₁₆	F0 ₁₆
17F6 ₁₆	00 ₁₆	1FF6 ₁₆	F0 ₁₆
17F7 ₁₆	00 ₁₆	1FF7 ₁₆	F0 ₁₆
17F8 ₁₆	00 ₁₆	1FF8 ₁₆	F0 ₁₆
17F9 ₁₆	00 ₁₆	1FF9 ₁₆	F0 ₁₆
17FA ₁₆	00 ₁₆	1FFA ₁₆	F0 ₁₆
17FB ₁₆	00 ₁₆	1FFB ₁₆	F0 ₁₆
17FC ₁₆	00 ₁₆	1FFC ₁₆	F0 ₁₆
17FD ₁₆	00 ₁₆	1FFD ₁₆	F0 ₁₆
17FE ₁₆	00 ₁₆	1FFE ₁₆	F0 ₁₆
17FF ₁₆	00 ₁₆	1FFF ₁₆	F0 ₁₆

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH03—71A< 08A0 >

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37202M3-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL	Issuance signature	Submitted by	Supervisor
	Date issued	()			
	Date :	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

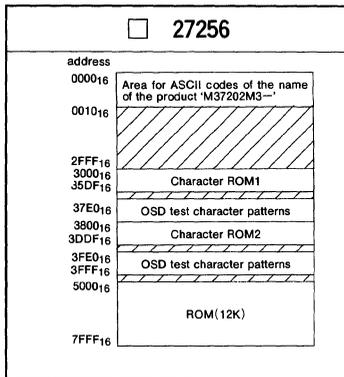
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

--	--	--	--

(hexadecimal notation)

EPROM type



(1) Set "FF₁₆" in the shaded area.

(2) Write the ASCII codes that indicates the name of the product 'M37202M3-' to addresses 0000₁₆ to 000F₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37202M3-XXXSP) and attach to the mask ROM confirmation form.

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH03—71A<08A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37202M3-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

- ※ 3. 1 I²C bus*
Would you use I²C bus function? Use Not use
- ※ 3. 2 OSD test character pattern input.
Write the two types of test patterns to the specified addresses.
- ※ 3. 3 Comments

Writing the name of the product and character ROM data onto EPROMs.

Addresses 0000₁₆ to 000F₁₆ store the name of the product and addresses 3000₁₆ to 3FFF₁₆ store the character ROM data. Write the following ASCII codes that indicates 'M37202M3-' to addresses 0000₁₆ to 000F₁₆.
If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code.
ASCII codes 'M37202M3-' are listed on the right.
The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'-' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	FF ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	FF ₁₆
0003 ₁₆	'2' = 3 2 ₁₆	000B ₁₆	FF ₁₆
0004 ₁₆	'0' = 3 0 ₁₆	000C ₁₆	FF ₁₆
0005 ₁₆	'2' = 3 2 ₁₆	000D ₁₆	FF ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	FF ₁₆
0007 ₁₆	'3' = 3 3 ₁₆	000F ₁₆	FF ₁₆

2. Inputting the character ROM
Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data and test character patterns, see the next page and on.

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH03—71A<08A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37202M3-XXXSP MITSUBISHI ELECTRIC

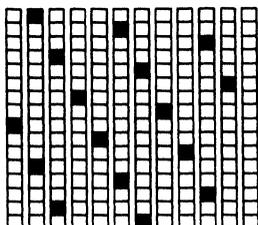
Mask ROM number	
-----------------	--

Inputting the test character pattern

Write the following character pattern to the specified addresses.

(1) Pattern 1

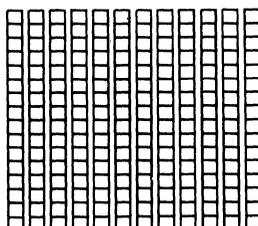
Character code "7E₁₆"



Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

(2) Pattern 2

Character code "7F₁₆"



Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH04-09A<11A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37204M8-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked*.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

*** 1. Confirmation**

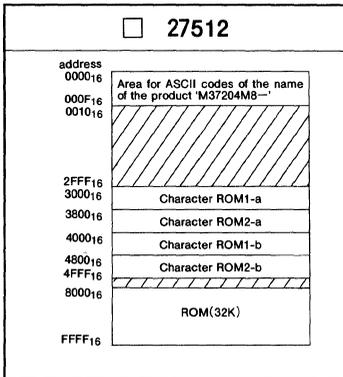
Specify the name of the product being ordered and the type of EPROMs submitted.
 Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
 If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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 (hexadecimal notation)

EPROM type



- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37204M8-' to addresses 0000₁₆ to 000F₁₆.

*** 2. Mark specification**

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37204M8-XXXSP) and attach to the mask ROM confirmation form.

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—09A<11A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37204M8-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

- ※ 3. 1 I²C bus*
Would you use I²C bus function? Use Not use

- ※ 3. 2 OSD test character pattern input.
Write the two types of test patterns to the specified addresses.

- ※ 3. 3 Comments

Writing the name of the product and character ROM data onto EPROMs.

Addresses 0000₁₆ to 000F₁₆ store the name of the product and addresses 3000₁₆ to 4FFF₁₆ store the character ROM data. Write the following ASCII codes that indicates 'M37204M8-' to addresses 0000₁₆ to 000F₁₆. If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code.
ASCII codes 'M37204M8-' are listed on the right.
The addresses and data are in hexadecimal notation.

Address	ASCII Code	Address	ASCII Code
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'-' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	F F ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	F F ₁₆
0003 ₁₆	'2' = 3 2 ₁₆	000B ₁₆	F F ₁₆
0004 ₁₆	'0' = 3 0 ₁₆	000C ₁₆	F F ₁₆
0005 ₁₆	'4' = 3 4 ₁₆	000D ₁₆	F F ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	F F ₁₆
0007 ₁₆	'8' = 3 8 ₁₆	000F ₁₆	F F ₁₆

2. Inputting the character ROM
Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data and test character patterns, see the next page and on.

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—09A<11A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37204M8-XXXSP MITSUBISHI ELECTRIC

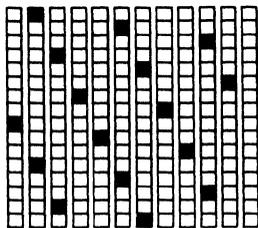
Mask ROM number	<input style="width: 80px; height: 20px;" type="text"/>
-----------------	---

Inputting the test character pattern

Write the following character pattern to the specified addresses.

(1) Pattern 1

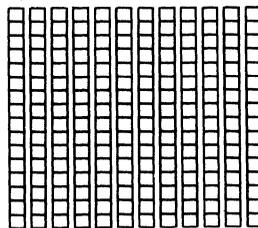
Character code "7E₁₆"



Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

(2) Pattern 2

Character code "7F₁₆"



Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—01A<0YA0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37250M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ()	Issuance signature.	Submitted by	Supervisor
		Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 27256																		
<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%; font-size: small;">address</td> <td style="font-size: small;">Area for ASCII codes of the name of the product 'M37250M6—'</td> </tr> <tr> <td style="font-size: x-small;">0000₁₆</td> <td rowspan="3" style="background: repeating-linear-gradient(45deg, transparent, transparent 2px, black 2px, black 4px);"></td> </tr> <tr> <td style="font-size: x-small;">000F₁₆</td> </tr> <tr> <td style="font-size: x-small;">0010₁₆</td> </tr> <tr> <td style="font-size: x-small;">0FFF₁₆</td> <td style="text-align: center; font-size: small;">Character ROM1</td> </tr> <tr> <td style="font-size: x-small;">1000₁₆</td> <td></td> </tr> <tr> <td style="font-size: x-small;">17FF₁₆</td> <td style="text-align: center; font-size: small;">Character ROM2</td> </tr> <tr> <td style="font-size: x-small;">1800₁₆</td> <td></td> </tr> <tr> <td style="font-size: x-small;">1FFF₁₆</td> <td rowspan="3" style="text-align: center; font-size: small;">ROM(24K)</td> </tr> <tr> <td style="font-size: x-small;">2000₁₆</td> </tr> <tr> <td style="font-size: x-small;">7FFF₁₆</td> </tr> </table>	address	Area for ASCII codes of the name of the product 'M37250M6—'	0000 ₁₆		000F ₁₆	0010 ₁₆	0FFF ₁₆	Character ROM1	1000 ₁₆		17FF ₁₆	Character ROM2	1800 ₁₆		1FFF ₁₆	ROM(24K)	2000 ₁₆	7FFF ₁₆
address	Area for ASCII codes of the name of the product 'M37250M6—'																	
0000 ₁₆																		
000F ₁₆																		
0010 ₁₆																		
0FFF ₁₆	Character ROM1																	
1000 ₁₆																		
17FF ₁₆	Character ROM2																	
1800 ₁₆																		
1FFF ₁₆	ROM(24K)																	
2000 ₁₆																		
7FFF ₁₆																		

(1) Set "FF₁₆" in the shaded area.

(2) Write the ASCII codes that indicates the name of the product 'M37250M6-' to addresses 0000₁₆ to 000F₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37250M6-XXXSP) and attach to the mask ROM confirmation form.

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—01A< 0YA0 >

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37250M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

- ※ 3. 1 I²C bus*
Would you use I²C bus function ? Use Not use
- ※ 3. 2 OSD test character pattern input.
Write the two types of test patterns to the specified addresses.
- ※ 3. 3 Comments

Writing the name of the product and character ROM data onto EPROMs.

Addresses 0000₁₆ to 000F₁₆ store the name of the product and addresses 1000₁₆ to 1FFF₁₆ store the character ROM data. Write the following ASCII codes that indicates 'M37250M6-' to addresses 0000₁₆ to 000F₁₆. If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code.
ASCII codes 'M37250M6-' are listed on the right.
The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'-' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	F F ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	F F ₁₆
0003 ₁₆	'2' = 3 2 ₁₆	000B ₁₆	F F ₁₆
0004 ₁₆	'5' = 3 5 ₁₆	000C ₁₆	F F ₁₆
0005 ₁₆	'0' = 3 0 ₁₆	000D ₁₆	F F ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	F F ₁₆
0007 ₁₆	'6' = 3 6 ₁₆	000F ₁₆	F F ₁₆

2. Inputting the character ROM
Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data and test character patterns, see the next page and on.

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH04-01A<0YA0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37250M6-XXXSP MITSUBISHI ELECTRIC

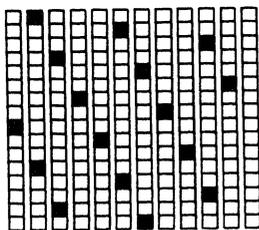
Mask ROM number	
-----------------	--

Inputting the test character pattern

Write the following character pattern to the specified addresses.

(1) Pattern 1

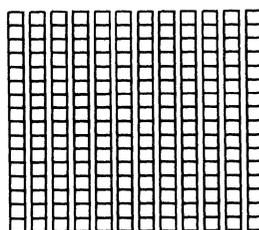
Character code "7E₁₆"



Address	Data	Address	Data
17E0 ₁₆	40 ₁₆	1FE0 ₁₆	F0 ₁₆
17E1 ₁₆	04 ₁₆	1FE1 ₁₆	F0 ₁₆
17E2 ₁₆	00 ₁₆	1FE2 ₁₆	F4 ₁₆
17E3 ₁₆	20 ₁₆	1FE3 ₁₆	F0 ₁₆
17E4 ₁₆	02 ₁₆	1FE4 ₁₆	F0 ₁₆
17E5 ₁₆	00 ₁₆	1FE5 ₁₆	F2 ₁₆
17E6 ₁₆	10 ₁₆	1FE6 ₁₆	F0 ₁₆
17E7 ₁₆	01 ₁₆	1FE7 ₁₆	F0 ₁₆
17E8 ₁₆	80 ₁₆	1FE8 ₁₆	F0 ₁₆
17E9 ₁₆	08 ₁₆	1FE9 ₁₆	F0 ₁₆
17EA ₁₆	00 ₁₆	1FEA ₁₆	F8 ₁₆
17EB ₁₆	40 ₁₆	1FEB ₁₆	F0 ₁₆
17EC ₁₆	04 ₁₆	1FEC ₁₆	F0 ₁₆
17ED ₁₆	00 ₁₆	1FED ₁₆	F4 ₁₆
17EE ₁₆	20 ₁₆	1FEE ₁₆	F0 ₁₆
17EF ₁₆	02 ₁₆	1FEF ₁₆	F0 ₁₆

(2) Pattern 2

Character code "7F₁₆"



Address	Data	Address	Data
17F0 ₁₆	00 ₁₆	1FF0 ₁₆	F0 ₁₆
17F1 ₁₆	00 ₁₆	1FF1 ₁₆	F0 ₁₆
17F2 ₁₆	00 ₁₆	1FF2 ₁₆	F0 ₁₆
17F3 ₁₆	00 ₁₆	1FF3 ₁₆	F0 ₁₆
17F4 ₁₆	00 ₁₆	1FF4 ₁₆	F0 ₁₆
17F5 ₁₆	00 ₁₆	1FF5 ₁₆	F0 ₁₆
17F6 ₁₆	00 ₁₆	1FF6 ₁₆	F0 ₁₆
17F7 ₁₆	00 ₁₆	1FF7 ₁₆	F0 ₁₆
17F8 ₁₆	00 ₁₆	1FF8 ₁₆	F0 ₁₆
17F9 ₁₆	00 ₁₆	1FF9 ₁₆	F0 ₁₆
17FA ₁₆	00 ₁₆	1FFA ₁₆	F0 ₁₆
17FB ₁₆	00 ₁₆	1FFB ₁₆	F0 ₁₆
17FC ₁₆	00 ₁₆	1FFC ₁₆	F0 ₁₆
17FD ₁₆	00 ₁₆	1FFD ₁₆	F0 ₁₆
17FE ₁₆	00 ₁₆	1FFE ₁₆	F0 ₁₆
17FF ₁₆	00 ₁₆	1FFF ₁₆	F0 ₁₆

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—05A〈0ZA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37260M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

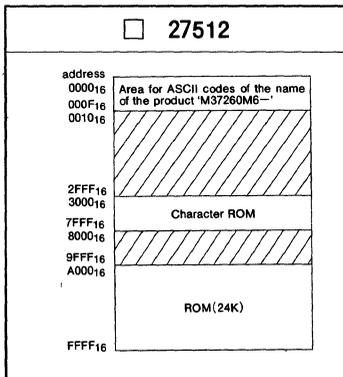
※	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted. Three sets of EPROMs are required for each pattern (Check @ in the appropriate box). If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM (hexadecimal notation)

EPROM type



- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37260M6-' to addresses 0000₁₆ to 000F₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M37260M6-XXXSP) and attach to the mask ROM confirmation form.

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—05A< OZA0 >

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37260M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
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- ※ 3. 1 I²C bus*
Would you use I²C bus function? Use Not use

- ※ 3. 2 OSD test character pattern input.
Write the two types of test patterns to the specified addresses.

- ※ 3. 3 Comments

Writing the name of the product and character ROM data onto EPROMs.

Addresses 0000₁₆ to 000F₁₆ store the name of the product and addresses 3000₁₆ to 7FFF₁₆ store the character ROM data. Write the following ASCII codes that indicates 'M37260M6-' to addresses 0000₁₆ to 000F₁₆. If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code.
ASCII codes 'M37260M6-' are listed on the right.
The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'-' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	F F ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	F F ₁₆
0003 ₁₆	'2' = 3 2 ₁₆	000B ₁₆	F F ₁₆
0004 ₁₆	'6' = 3 6 ₁₆	000C ₁₆	F F ₁₆
0005 ₁₆	'0' = 3 0 ₁₆	000D ₁₆	F F ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	F F ₁₆
0007 ₁₆	'6' = 3 6 ₁₆	000F ₁₆	F F ₁₆

2. Inputting the character ROM
Input the character ROM data by dividing it into four parts. For the character ROM data and test character patterns, see the next page and on.

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

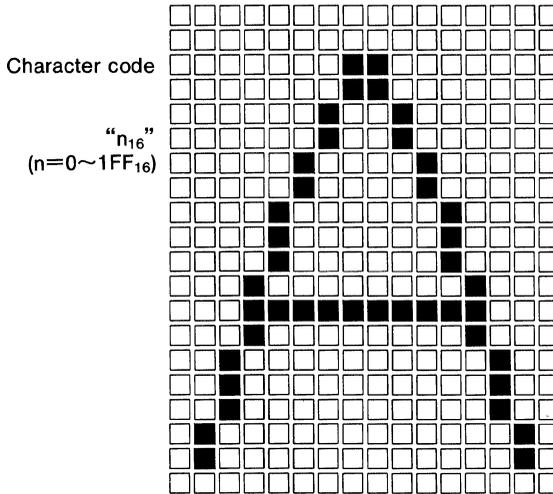
GZZ—SH04—05A<0ZA>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37260M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
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The structure of character ROM (divide of 16×20 dots font)

Example



Character ROM address	b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀	Character ROM data	Character ROM address	b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀	Character ROM data
3000 ₁₆ +20 ₁₆ ×n ₁₆ +0 ₁₆		00 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +1 ₁₆		00 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +2 ₁₆		00 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +3 ₁₆		00 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +4 ₁₆		01 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +5 ₁₆		80 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +6 ₁₆		01 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +7 ₁₆		80 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +8 ₁₆		02 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +9 ₁₆		40 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +A ₁₆		02 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +B ₁₆		40 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +C ₁₆		04 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +D ₁₆		20 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +E ₁₆		04 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +F ₁₆		20 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +10 ₁₆		08 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +11 ₁₆		10 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +12 ₁₆		08 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +13 ₁₆		10 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +14 ₁₆		08 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +15 ₁₆		10 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +16 ₁₆		10 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +17 ₁₆		08 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +18 ₁₆		1F ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +19 ₁₆		F8 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +1A ₁₆		10 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +1B ₁₆		08 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +1C ₁₆		20 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +1D ₁₆		04 ₁₆
3000 ₁₆ +20 ₁₆ ×n ₁₆ +1E ₁₆		20 ₁₆	3000 ₁₆ +20 ₁₆ ×n ₁₆ +1F ₁₆		04 ₁₆
7000 ₁₆ +8 ₁₆ ×n ₁₆ +0 ₁₆		20 ₁₆	7000 ₁₆ +8 ₁₆ ×n ₁₆ +1 ₁₆		04 ₁₆
7000 ₁₆ +8 ₁₆ ×n ₁₆ +2 ₁₆		40 ₁₆	7000 ₁₆ +8 ₁₆ ×n ₁₆ +3 ₁₆		02 ₁₆
7000 ₁₆ +8 ₁₆ ×n ₁₆ +4 ₁₆		40 ₁₆	7000 ₁₆ +8 ₁₆ ×n ₁₆ +5 ₁₆		02 ₁₆
7000 ₁₆ +8 ₁₆ ×n ₁₆ +6 ₁₆		00 ₁₆	7000 ₁₆ +8 ₁₆ ×n ₁₆ +7 ₁₆		00 ₁₆

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—60A<86A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37409M2-XXXSP/FP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked*.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : M37409M2-XXXSP M37409M2-XXXFP

Checksum code for entire EPROM

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 (hexadecimal notation)

EPROM type

<input type="checkbox"/> 2764	<input type="checkbox"/> 27128
<p>Address</p> <p>0000₁₆</p> <div style="border: 1px solid black; padding: 5px; margin: 5px 0;">Area for ASCII codes of the catalog name 'M37409M2—'.</div> <p>000F₁₆</p> <div style="background-color: #cccccc; height: 40px; margin: 5px 0;"></div> <p>0FFF₁₆</p> <p>1000₁₆</p> <div style="border: 1px solid black; padding: 5px; margin: 5px 0;">ROM(4 K)</div> <p>1FFF₁₆</p>	<p>Address</p> <p>0000₁₆</p> <div style="border: 1px solid black; padding: 5px; margin: 5px 0;">Area for ASCII codes of the catalog name 'M37409M2—'.</div> <p>000F₁₆</p> <div style="background-color: #cccccc; height: 40px; margin: 5px 0;"></div> <p>2FFF₁₆</p> <p>3000₁₆</p> <div style="border: 1px solid black; padding: 5px; margin: 5px 0;">ROM(4 K)</div> <p>3FFF₁₆</p>

- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37409M2—' to addresses 0000₁₆ to 000F₁₆. ASCII codes 'M37409M2—' are listed on the right.
The addresses and data are in hexadecimal notation.

Address	Address	Address
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆
0003 ₁₆	'4' = 3 4 ₁₆	000B ₁₆
0004 ₁₆	'0' = 3 0 ₁₆	000C ₁₆
0005 ₁₆	'9' = 3 9 ₁₆	000D ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆
0007 ₁₆	'2' = 3 2 ₁₆	000F ₁₆
		'—' = 2 D ₁₆
		FF ₁₆
		FF ₁₆
		FF ₁₆
		FF ₁₆
		FF ₁₆
		FF ₁₆
		FF ₁₆

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—60A〈86A0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37409M2-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	
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Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	2764	27128
The pseudo-command	* =△\$E000 .BYTE△ 'M37409M2—'	* =△\$C000 .BYTE△ 'M37409M2—'

This is an example when the start address of internal ROM is F000₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M37409M2-XXXSP ; 50P6N for M37409M2-XXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH04-13A<11A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37410M3HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked*.

* Customer	Company name	TEL	Issuance signature	Submitted by	Supervisor
	Date issued	Date :		()	

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128	<input type="checkbox"/> 27256	<input type="checkbox"/> 27512
address 0000 Port P0 pull-up 0001 Port P1 pull-up 0002 Port P2 pull-up 0003 Port P3 pull-up 0004 Port P4 pull-up 0005 Port P5 pull-up 0006 Port P2 key on wake-up 0007 2800 ROM(6K) 3FFF	address 0000 Port P0 pull-up 0001 Port P1 pull-up 0002 Port P2 pull-up 0003 Port P3 pull-up 0004 Port P4 pull-up 0005 Port P5 pull-up 0006 Port P2 key on wake-up 0007 6800 ROM(6K) 7FFF	address 0000 Port P0 pull-up 0001 Port P1 pull-up 0002 Port P2 pull-up 0003 Port P3 pull-up 0004 Port P4 pull-up 0005 Port P5 pull-up 0006 Port P2 key on wake-up 0007 E800 ROM(6K) FFFF

Set "FF₁₆" in the shaded area.

* 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6S for M37410M3HXXXFP) and attach to the mask ROM confirmation form.

* 3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—13A<11A0>

**SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37410M3HXXXFP
MITSUBISHI ELECTRIC**

Mask ROM number	
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※ 4. Option specification (write the option data also at the specified address in the EPROM)

1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

	P0 ₇	P0 ₆	P0 ₅	P0 ₄	P0 ₃	P0 ₂	P0 ₁	P0 ₀
address 0000 ₁₆								

2. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

	P1 ₇	P1 ₆	P1 ₅	P1 ₄	P1 ₃	P1 ₂	P1 ₁	P1 ₀
address 0001 ₁₆								

3. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	P2 ₇	P2 ₆	P2 ₅	P2 ₄	P2 ₃	P2 ₂	P2 ₁	P2 ₀
address 0002 ₁₆								

4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

	P3 ₇	P3 ₆	P3 ₅	P3 ₄	P3 ₃	P3 ₂	P3 ₁	P3 ₀
address 0003 ₁₆								

5. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

					P4 ₃	P4 ₂	P4 ₁	P4 ₀
address 0004 ₁₆	0	0	0	0				

6. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

	P5 ₇	P5 ₆	P5 ₅	P5 ₄	P5 ₃	P5 ₂	P5 ₁	P5 ₀
address 0005 ₁₆								

7. Port P2 key on wake-up (if built-in is desired write 1, if not write 0)

	KW ₇	KW ₆	KW ₅	KW ₄	KW ₃	KW ₂	KW ₁	KW ₀
address 0006 ₁₆								

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—14A<11A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37410M4HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted. Three sets of EPROMs are required for each pattern (Check @ in the appropriate box). If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128	<input type="checkbox"/> 27256	<input type="checkbox"/> 27512																																																																								
<table border="1"> <tr><td>address</td><td></td></tr> <tr><td>0000</td><td>Port P0 pull-up</td></tr> <tr><td>0001</td><td>Port P1 pull-up</td></tr> <tr><td>0002</td><td>Port P2 pull-up</td></tr> <tr><td>0003</td><td>Port P3 pull-up</td></tr> <tr><td>0004</td><td>Port P4 pull-up</td></tr> <tr><td>0005</td><td>Port P5 pull-up</td></tr> <tr><td>0006</td><td>Port P2 key on wake-up</td></tr> <tr><td>0007</td><td style="background-color: #cccccc;"></td></tr> <tr><td>2000</td><td style="background-color: #cccccc;"></td></tr> <tr><td>3FFF</td><td style="background-color: #cccccc;"></td></tr> <tr><td></td><td style="text-align: center;">ROM(8K)</td></tr> </table>	address		0000	Port P0 pull-up	0001	Port P1 pull-up	0002	Port P2 pull-up	0003	Port P3 pull-up	0004	Port P4 pull-up	0005	Port P5 pull-up	0006	Port P2 key on wake-up	0007		2000		3FFF			ROM(8K)	<table border="1"> <tr><td>address</td><td></td></tr> <tr><td>0000</td><td>Port P0 pull-up</td></tr> <tr><td>0001</td><td>Port P1 pull-up</td></tr> <tr><td>0002</td><td>Port P2 pull-up</td></tr> <tr><td>0003</td><td>Port P3 pull-up</td></tr> <tr><td>0004</td><td>Port P4 pull-up</td></tr> <tr><td>0005</td><td>Port P5 pull-up</td></tr> <tr><td>0006</td><td>Port P2 key on wake-up</td></tr> <tr><td>0007</td><td style="background-color: #cccccc;"></td></tr> <tr><td>6000</td><td style="background-color: #cccccc;"></td></tr> <tr><td>7FFF</td><td style="background-color: #cccccc;"></td></tr> <tr><td></td><td style="text-align: center;">ROM(8K)</td></tr> </table>	address		0000	Port P0 pull-up	0001	Port P1 pull-up	0002	Port P2 pull-up	0003	Port P3 pull-up	0004	Port P4 pull-up	0005	Port P5 pull-up	0006	Port P2 key on wake-up	0007		6000		7FFF			ROM(8K)	<table border="1"> <tr><td>address</td><td></td></tr> <tr><td>0000</td><td>Port P0 pull-up</td></tr> <tr><td>0001</td><td>Port P1 pull-up</td></tr> <tr><td>0002</td><td>Port P2 pull-up</td></tr> <tr><td>0003</td><td>Port P3 pull-up</td></tr> <tr><td>0004</td><td>Port P4 pull-up</td></tr> <tr><td>0005</td><td>Port P5 pull-up</td></tr> <tr><td>0006</td><td>Port P2 key on wake-up</td></tr> <tr><td>0007</td><td style="background-color: #cccccc;"></td></tr> <tr><td>E000</td><td style="background-color: #cccccc;"></td></tr> <tr><td>FFFF</td><td style="background-color: #cccccc;"></td></tr> <tr><td></td><td style="text-align: center;">ROM(8K)</td></tr> </table>	address		0000	Port P0 pull-up	0001	Port P1 pull-up	0002	Port P2 pull-up	0003	Port P3 pull-up	0004	Port P4 pull-up	0005	Port P5 pull-up	0006	Port P2 key on wake-up	0007		E000		FFFF			ROM(8K)
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Set "FF₁₆" in the shaded area.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6S for M37410M4HXXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—14A<11A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37410M4HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

※ 4. Option specification (write the option data also at the specified address in the EPROM)

1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

	P0 ₇	P0 ₆	P0 ₅	P0 ₄	P0 ₃	P0 ₂	P0 ₁	P0 ₀
address 0000 ₁₆								

2. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

	P1 ₇	P1 ₆	P1 ₅	P1 ₄	P1 ₃	P1 ₂	P1 ₁	P1 ₀
address 0001 ₁₆								

3. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	P2 ₇	P2 ₆	P2 ₅	P2 ₄	P2 ₃	P2 ₂	P2 ₁	P2 ₀
address 0002 ₁₆								

4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

	P3 ₇	P3 ₆	P3 ₅	P3 ₄	P3 ₃	P3 ₂	P3 ₁	P3 ₀
address 0003 ₁₆								

5. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

				P4 ₃	P4 ₂	P4 ₁	P4 ₀
address 0004 ₁₆	0	0	0	0			

6. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

	P5 ₇	P5 ₆	P5 ₅	P5 ₄	P5 ₃	P5 ₂	P5 ₁	P5 ₀
address 0005 ₁₆								

7. Port P2 key on wake-up (if built-in is desired write 1, if not write 0)

	KW ₇	KW ₆	KW ₅	KW ₄	KW ₃	KW ₂	KW ₁	KW ₀
address 0006 ₁₆								

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—15A<11A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37410M6HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted. Three sets of EPROMs are required for each pattern (Check @ in the appropriate box). If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128	<input type="checkbox"/> 27256	<input type="checkbox"/> 27512																																																																		
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Set "FF₁₆" in the shaded area.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6S for M37410M6HXXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH04-15A<11A0>

**SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37410M6HXXXFP
MITSUBISHI ELECTRIC**

Mask ROM number	
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※ 4. Option specification (write the option data also at the specified address in the EPROM)

1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

	P0 ₇	P0 ₆	P0 ₅	P0 ₄	P0 ₃	P0 ₂	P0 ₁	P0 ₀
address 0000 ₁₆								

2. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

	P1 ₇	P1 ₆	P1 ₅	P1 ₄	P1 ₃	P1 ₂	P1 ₁	P1 ₀
address 0001 ₁₆								

3. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	P2 ₇	P2 ₆	P2 ₅	P2 ₄	P2 ₃	P2 ₂	P2 ₁	P2 ₀
address 0002 ₁₆								

4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

	P3 ₇	P3 ₆	P3 ₅	P3 ₄	P3 ₃	P3 ₂	P3 ₁	P3 ₀
address 0003 ₁₆								

5. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

					P4 ₃	P4 ₂	P4 ₁	P4 ₀
address 0004 ₁₆	0	0	0	0				

6. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

	P5 ₇	P5 ₆	P5 ₅	P5 ₄	P5 ₃	P5 ₂	P5 ₁	P5 ₀
address 0005 ₁₆								

7. Port P2 key on wake-up (if built-in is desired write 1, if not write 0)

	KW ₇	KW ₆	KW ₅	KW ₄	KW ₃	KW ₂	KW ₁	KW ₀
address 0006 ₁₆								

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—54A< 83B0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37412M4-XXXF MITSUBISHI ELECTRIC

Mask ROM number	
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Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128	<input type="checkbox"/> 27256	<input type="checkbox"/> 27512
<p>Address</p> <p>0000₁₆ Area for ASCII codes of the name of the product 'M37412M4—'</p> <p>000F₁₆</p> <p>0010₁₆ STP option</p> <p>0011₁₆ </p> <p>1FFF₁₆</p> <p>2000₁₆ ROM(8 K)</p> <p>3FFF₁₆</p>	<p>Address</p> <p>0000₁₆ Area for ASCII codes of the name of the product 'M37412M4—'</p> <p>000F₁₆</p> <p>0010₁₆ STP option</p> <p>0011₁₆ </p> <p>5FFF₁₆</p> <p>6000₁₆ ROM(8 K)</p> <p>7FFF₁₆</p>	<p>Address</p> <p>0000₁₆ Area for ASCII codes of the name of the product 'M37412M4—'</p> <p>000F₁₆</p> <p>0010₁₆ STP option</p> <p>0011₁₆ </p> <p>DFFF₁₆</p> <p>E000₁₆ ROM(8 K)</p> <p>FFFF₁₆</p>

- Set "FF₁₆" in the shaded area.
- Write the ASCII codes that indicates the name of the product 'M37412M4—' to addresses 0000₁₆ to 000F₁₆. ASCII codes 'M37412M4—' are listed on the right. The addresses and data are in hexadecimal notation.
Write the option data to address 0010₁₆.

Address	'M' = 4 D ₁₆	Address	'—' = 2 D ₁₆
0000 ₁₆		0008 ₁₆	FF ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	FF ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	FF ₁₆
0003 ₁₆	'4' = 3 4 ₁₆	000B ₁₆	FF ₁₆
0004 ₁₆	'1' = 3 1 ₁₆	000C ₁₆	FF ₁₆
0005 ₁₆	'2' = 3 2 ₁₆	000D ₁₆	FF ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	FF ₁₆
0007 ₁₆	'4' = 3 4 ₁₆	000F ₁₆	FF ₁₆

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—54A<83B0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37412M4-XXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	*=△\$C000 .BYTE△ 'M37412M4—'	*=△\$8000 .BYTE△ 'M37412M4—'	*=△\$0000 .BYTE△ 'M37412M4—'

This is an example when the start address of internal ROM is E000₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (72P6 for M37412M4-XXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

※ 4. Option specification (write the option data also to the specified address of the EPROM)

1. STP instruction option

- When STP instruction is valid

01 ₁₆

 Address 0010₁₆
- When STP instruction is invalid

00 ₁₆

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27128	27256	27512
1. STP instruction option	*=△\$C010 .BYTE△\$XX	*=△\$8010 .BYTE△\$XX	*=△\$0010 .BYTE△\$XX

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly. As for the option, if the contents of the confirmation and conflict with those of the EPROM, the contents of the EPROM are preferred.

MITSUBISHI MICROCOMPUTERS SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH04-35A<13A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37413M4HXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1. Confirmation

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Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

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Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

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FFFF ₁₆	ROM(8 K)																																																																																																							

- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37413M4H' to addresses 0000₁₆ to 000F₁₆.
Write the option data to addresses 0010₁₆ to 0019₁₆.

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—35A< 13A0 >

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37413M4HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6S for M37413M4HXXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

※ 4. Option specification (write the option data also at the specified address in the EPROM.)

1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

	P0 ₇	P0 ₆	P0 ₅	P0 ₄	P0 ₃	P0 ₂	P0 ₁	P0 ₀
address 0010 ₁₆								

2. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

	P1 ₇	P1 ₆	P1 ₅	P1 ₄	P1 ₃	P1 ₂	P1 ₁	P1 ₀
address 0011 ₁₆								

3. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	P2 ₇	P2 ₆	P2 ₅	P2 ₄	P2 ₃	P2 ₂	P2 ₁	P2 ₀
address 0012 ₁₆								

4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

	P3 ₇	P3 ₆	P3 ₅	P3 ₄	P3 ₃	P3 ₂	P3 ₁	P3 ₀
address 0013 ₁₆								

5. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

	P4 ₇	P4 ₆	P4 ₅	P4 ₄	P4 ₃	P4 ₂	P4 ₁	P4 ₀
address 0014 ₁₆								

6. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

	P5 ₇	P5 ₆	P5 ₅	P5 ₄	P5 ₃	P5 ₂	P5 ₁	P5 ₀
address 0015 ₁₆								

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—35A<13A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37413M4HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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7. Port P2 key on wake up (if built-in is desired write 1, if not write 0)

	KW ₇	KW ₆	KW ₅	KW ₄	KW ₃	KW ₂	KW ₁	KW ₀
address 0016 ₁₆								

8. Port P6 pull-up transistor (if built-in is desired write 1, if not write 0)

	P6 ₇	P6 ₆	P6 ₅	P6 ₄	P6 ₃	P6 ₂	P6 ₁	P6 ₀
address 0017 ₁₆								

9. Port P7 pull-up transistor (if built-in is desired write 1, if not write 0)

	P7 ₇	P7 ₆	P7 ₅	P7 ₄	P7 ₃	P7 ₂	P7 ₁	P7 ₀
address 0018 ₁₆								

10. Port P7 key on wake up (if built-in is desired write 1, if not write 0)

	KU ₇	KU ₆	KU ₅	KU ₄	KU ₃	KU ₂	KU ₁	KU ₀
address 0019 ₁₆								

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ-SH04-35A<13A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37413M4HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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Writing the name of the product and option data onto EPROMs.

Addresses 0000₁₆ to 000F₁₆ store the name of the product and addresses 0010₁₆ to 0019₁₆ store the option data. Write the following ASCII codes that indicates 'M37413M4H' to addresses 0000₁₆ to 000F₁₆.

Write data according to the option data sheet to addresses 0010₁₆ to 0019₁₆.

If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

As for the option, if the contents of the confirmation and conflict with those of the EPROMs, the contents of the EPROMs are preferred.

1. Inputting the name of the product with the ASCII code.
ASCII codes 'M37413M4H' are listed on the right.
The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'H' = 4 8 ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	F F ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	F F ₁₆
0003 ₁₆	'4' = 3 4 ₁₆	000B ₁₆	F F ₁₆
0004 ₁₆	'1' = 3 1 ₁₆	000C ₁₆	F F ₁₆
0005 ₁₆	'3' = 3 3 ₁₆	000D ₁₆	F F ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	F F ₁₆
0007 ₁₆	'4' = 3 4 ₁₆	000F ₁₆	F F ₁₆

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	*=\$C000 .BYTE△ 'M37413M4H'	*=\$8000 .BYTE△ 'M37413M4H'	*=\$0000 .BYTE△ 'M37413M4H'

This is an example when the start address of internal ROM is F000₁₆.

2. Inputting the option data onto the EPROMs.

Write the following pseudo-command to the assembler source file :

EPROM type	27128	27256	27512
	*=\$C010	*=\$8010	*=\$0010
P0 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P1 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P2 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P3 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P4 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P5 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P2 key on wake up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P6 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P7 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P7 key on wake up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX

MITSUBISHI MICROCOMPUTERS SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—36A<13A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37413M6HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128	<input type="checkbox"/> 27256	<input type="checkbox"/> 27512																																																						
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="text-align: center;">Address</td></tr> <tr><td>0000₁₆ Area for ASCII codes of the name of the product 'M37413M6H'</td></tr> <tr><td>000F₁₆</td></tr> <tr><td>0010₁₆ Port P0 pull-up</td></tr> <tr><td>0011₁₆ Port P1 pull-up</td></tr> <tr><td>0012₁₆ Port P2 pull-up</td></tr> <tr><td>0013₁₆ Port P3 pull-up</td></tr> <tr><td>0014₁₆ Port P4 pull-up</td></tr> <tr><td>0015₁₆ Port P5 pull-up</td></tr> <tr><td>0016₁₆ Port P2 key on wake up</td></tr> <tr><td>0017₁₆ Port P6 pull-up</td></tr> <tr><td>0018₁₆ Port P7 pull-up</td></tr> <tr><td>0019₁₆ Port P7 key on wake up</td></tr> <tr><td>001A₁₆</td></tr> <tr style="background-color: #cccccc;"><td>0FFF₁₆</td></tr> <tr style="background-color: #cccccc;"><td>1000₁₆</td></tr> <tr style="background-color: #cccccc;"><td>3FFF₁₆</td></tr> <tr><td style="text-align: center;">ROM(12K)</td></tr> </table>	Address	0000 ₁₆ Area for ASCII codes of the name of the product 'M37413M6H'	000F ₁₆	0010 ₁₆ Port P0 pull-up	0011 ₁₆ Port P1 pull-up	0012 ₁₆ Port P2 pull-up	0013 ₁₆ Port P3 pull-up	0014 ₁₆ Port P4 pull-up	0015 ₁₆ Port P5 pull-up	0016 ₁₆ Port P2 key on wake up	0017 ₁₆ Port P6 pull-up	0018 ₁₆ Port P7 pull-up	0019 ₁₆ Port P7 key on wake up	001A ₁₆	0FFF ₁₆	1000 ₁₆	3FFF ₁₆	ROM(12K)	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="text-align: center;">Address</td></tr> <tr><td>0000₁₆ Area for ASCII codes of the name of the product 'M37413M6H'</td></tr> <tr><td>000F₁₆</td></tr> <tr><td>0010₁₆ Port P0 pull-up</td></tr> <tr><td>0011₁₆ Port P1 pull-up</td></tr> <tr><td>0012₁₆ Port P2 pull-up</td></tr> <tr><td>0013₁₆ Port P3 pull-up</td></tr> <tr><td>0014₁₆ Port P4 pull-up</td></tr> <tr><td>0015₁₆ Port P5 pull-up</td></tr> <tr><td>0016₁₆ Port P2 key on wake up</td></tr> <tr><td>0017₁₆ Port P6 pull-up</td></tr> <tr><td>0018₁₆ Port P7 pull-up</td></tr> <tr><td>0019₁₆ Port P7 key on wake up</td></tr> <tr><td>001A₁₆</td></tr> <tr style="background-color: #cccccc;"><td>4FFF₁₆</td></tr> <tr style="background-color: #cccccc;"><td>5000₁₆</td></tr> <tr style="background-color: #cccccc;"><td>7FFF₁₆</td></tr> <tr><td style="text-align: center;">ROM(12K)</td></tr> </table>	Address	0000 ₁₆ Area for ASCII codes of the name of the product 'M37413M6H'	000F ₁₆	0010 ₁₆ Port P0 pull-up	0011 ₁₆ Port P1 pull-up	0012 ₁₆ Port P2 pull-up	0013 ₁₆ Port P3 pull-up	0014 ₁₆ Port P4 pull-up	0015 ₁₆ Port P5 pull-up	0016 ₁₆ Port P2 key on wake up	0017 ₁₆ Port P6 pull-up	0018 ₁₆ Port P7 pull-up	0019 ₁₆ Port P7 key on wake up	001A ₁₆	4FFF ₁₆	5000 ₁₆	7FFF ₁₆	ROM(12K)	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="text-align: center;">Address</td></tr> <tr><td>0000₁₆ Area for ASCII codes of the name of the product 'M37413M6H'</td></tr> <tr><td>000F₁₆</td></tr> <tr><td>0010₁₆ Port P0 pull-up</td></tr> <tr><td>0011₁₆ Port P1 pull-up</td></tr> <tr><td>0012₁₆ Port P2 pull-up</td></tr> <tr><td>0013₁₆ Port P3 pull-up</td></tr> <tr><td>0014₁₆ Port P4 pull-up</td></tr> <tr><td>0015₁₆ Port P5 pull-up</td></tr> <tr><td>0016₁₆ Port P2 key on wake up</td></tr> <tr><td>0017₁₆ Port P6 pull-up</td></tr> <tr><td>0018₁₆ Port P7 pull-up</td></tr> <tr><td>0019₁₆ Port P7 key on wake up</td></tr> <tr><td>001A₁₆</td></tr> <tr style="background-color: #cccccc;"><td>CFFF₁₆</td></tr> <tr style="background-color: #cccccc;"><td>D000₁₆</td></tr> <tr style="background-color: #cccccc;"><td>FFFF₁₆</td></tr> <tr><td style="text-align: center;">ROM(12K)</td></tr> </table>	Address	0000 ₁₆ Area for ASCII codes of the name of the product 'M37413M6H'	000F ₁₆	0010 ₁₆ Port P0 pull-up	0011 ₁₆ Port P1 pull-up	0012 ₁₆ Port P2 pull-up	0013 ₁₆ Port P3 pull-up	0014 ₁₆ Port P4 pull-up	0015 ₁₆ Port P5 pull-up	0016 ₁₆ Port P2 key on wake up	0017 ₁₆ Port P6 pull-up	0018 ₁₆ Port P7 pull-up	0019 ₁₆ Port P7 key on wake up	001A ₁₆	CFFF ₁₆	D000 ₁₆	FFFF ₁₆	ROM(12K)
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(1) Set "FF₁₆" in the shaded area.

(2) Write the ASCII codes that indicates the name of the product 'M37413M6H' to addresses 0000₁₆ to 000F₁₆.

Write the option data to addresses 0010₁₆ to 0019₁₆.

MITSUBISHI MICROCOMPUTERS SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—36A< 13A0 >

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37413M6HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6S for M37413M6HXXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

※ 4. Option specification (write the option data also at the specified address in the EPROM.)

1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

	P0 ₇	P0 ₆	P0 ₅	P0 ₄	P0 ₃	P0 ₂	P0 ₁	P0 ₀
address 0010 ₁₆								

2. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

	P1 ₇	P1 ₆	P1 ₅	P1 ₄	P1 ₃	P1 ₂	P1 ₁	P1 ₀
address 0011 ₁₆								

3. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	P2 ₇	P2 ₆	P2 ₅	P2 ₄	P2 ₃	P2 ₂	P2 ₁	P2 ₀
address 0012 ₁₆								

4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

	P3 ₇	P3 ₆	P3 ₅	P3 ₄	P3 ₃	P3 ₂	P3 ₁	P3 ₀
address 0013 ₁₆								

5. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

	P4 ₇	P4 ₆	P4 ₅	P4 ₄	P4 ₃	P4 ₂	P4 ₁	P4 ₀
address 0014 ₁₆								

6. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

	P5 ₇	P5 ₆	P5 ₅	P5 ₄	P5 ₃	P5 ₂	P5 ₁	P5 ₀
address 0015 ₁₆								

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—36A<13A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37413M6HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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7. Port P2 key on wake up (if built-in is desired write 1, if not write 0)

	KW ₇	KW ₆	KW ₅	KW ₄	KW ₃	KW ₂	KW ₁	KW ₀
address 0016 ₁₆								

8. Port P6 pull-up transistor (if built-in is desired write 1, if not write 0)

	P6 ₇	P6 ₆	P6 ₅	P6 ₄	P6 ₃	P6 ₂	P6 ₁	P6 ₀
address 0017 ₁₆								

9. Port P7 pull-up transistor (if built-in is desired write 1, if not write 0)

	P7 ₇	P7 ₆	P7 ₅	P7 ₄	P7 ₃	P7 ₂	P7 ₁	P7 ₀
address 0018 ₁₆								

10. Port P7 key on wake up (if built-in is desired write 1, if not write 0)

	KU ₇	KU ₆	KU ₅	KU ₄	KU ₃	KU ₂	KU ₁	KU ₀
address 0019 ₁₆								

MITSUBISHI MICROCOMPUTERS SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH04—36A<13A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37413M6HXXXFP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Writing the name of the product and option data onto EPROMs.

Addresses 0000₁₆ to 000F₁₆ store the name of the product and addresses 0010₁₆ to 0019₁₆ store the option data. Write the following ASCII codes that indicates 'M37413M6H' to addresses 0000₁₆ to 000F₁₆.

Write data according to the option data sheet to addresses 0010₁₆ to 0019₁₆.

If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

As for the option, if the contents of the confirmation and conflict with those of the EPROMs, the contents of the EPROMs are preferred.

1. Inputting the name of the product with the ASCII code.

ASCII codes 'M37413M6H' are listed on the right.

The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'H' = 4 8 ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	F F ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	F F ₁₆
0003 ₁₆	'4' = 3 4 ₁₆	000B ₁₆	F F ₁₆
0004 ₁₆	'1' = 3 1 ₁₆	000C ₁₆	F F ₁₆
0005 ₁₆	'3' = 3 3 ₁₆	000D ₁₆	F F ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	F F ₁₆
0007 ₁₆	'6' = 3 6 ₁₆	000F ₁₆	F F ₁₆

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	*=\$C000 .BYTE△ 'M37413M6H'	*=\$8000 .BYTE△ 'M37413M6H'	*=\$0000 .BYTE△ 'M37413M6H'

This is an example when the start address of internal ROM is F000₁₆.

2. Inputting the option data onto the EPROMs.

Write the following pseudo-command to the assembler source file :

EPROM type	27128	27256	27512
	*=\$C010	*=\$8010	*=\$0010
P0 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P1 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P2 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P3 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P4 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P5 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P2 key on wake up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P6 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P7 pull-up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX
P7 key on wake up	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH02—11A〈96A0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37414M5-XXXFP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted. Three sets of EPROMs are required for each pattern (Check @ in the appropriate box). If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128	<input type="checkbox"/> 27256	<input type="checkbox"/> 27512
<p>Address</p> <p>0000₁₆ Area for ASCII codes of the name of the product 'M37414M5—'</p> <p>000F₁₆</p> <p>0010₁₆ STP option</p> <p>0011₁₆ </p> <p>1800₁₆</p> <p>ROM(10K)</p> <p>3FFF₁₆</p>	<p>Address</p> <p>0000₁₆ Area for ASCII codes of the name of the product 'M37414M5—'</p> <p>000F₁₆</p> <p>0010₁₆ STP option</p> <p>0011₁₆ </p> <p>5800₁₆</p> <p>ROM(10K)</p> <p>7FFF₁₆</p>	<p>Address</p> <p>0000₁₆ Area for ASCII codes of the name of the product 'M37414M5—'</p> <p>000F₁₆</p> <p>0010₁₆ STP option</p> <p>0011₁₆ </p> <p>D800₁₆</p> <p>ROM(10K)</p> <p>FFFF₁₆</p>

- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37414M5—' to addresses 0000₁₆ to 000F₁₆. ASCII codes 'M37414M5—' are listed on the right. The addresses and data are in hexadecimal notation.
Write the option data to address 0010₁₆.

Address	
0000 ₁₆	'M' = 4 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆
0002 ₁₆	'7' = 3 7 ₁₆
0003 ₁₆	'4' = 3 4 ₁₆
0004 ₁₆	'1' = 3 1 ₁₆
0005 ₁₆	'4' = 3 4 ₁₆
0006 ₁₆	'M' = 4 D ₁₆
0007 ₁₆	'5' = 3 5 ₁₆

Address	
0008 ₁₆	'—' = 2 D ₁₆
0009 ₁₆	F F ₁₆
000A ₁₆	F F ₁₆
000B ₁₆	F F ₁₆
000C ₁₆	F F ₁₆
000D ₁₆	F F ₁₆
000E ₁₆	F F ₁₆
000F ₁₆	F F ₁₆

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH02—11A<96A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37414M5-XXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	*=△\$C000 .BYTE△ 'M37414M5—'	*=△\$8000 .BYTE△ 'M37414M5—'	*=△\$0000 .BYTE△ 'M37414M5—'

This is an example when the start address of internal ROM is D800₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (72P6 for M37414M5-XXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

※ 4. Option specification (write the option data also to the specified address of the EPROM)

1. STP instruction option

- When STP instruction is valid Address 0010₁₆
- When STP instruction is invalid

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27128	27256	27512
1. STP instruction option	*=△\$C010 .BYTE△\$XX	*=△\$8010 .BYTE△\$XX	*=△\$0010 .BYTE△\$XX

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly. As for the option, if the contents of the confirmation and conflict with those of the EPROM, the contents of the EPROM are preferred.

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—86A< 91A0 >

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37415M4-XXXFP MITSUBISHI ELECTRIC

Mask ROM number	
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Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted. Three sets of EPROMs are required for each pattern (Check @ in the appropriate box). If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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 (hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128 Address <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 50px;">0000</td><td>Port P0 pull-up</td></tr> <tr><td>0001</td><td>Port P1 pull-up</td></tr> <tr><td>0002</td><td>Port P2 pull-up</td></tr> <tr><td>0003</td><td>Port P3 pull-up</td></tr> <tr><td>0004</td><td>P3_s output type</td></tr> <tr><td>0005</td><td>CNTR pull-up</td></tr> <tr><td>0006</td><td style="background-color: #cccccc;"></td></tr> <tr><td>2000</td><td style="background-color: #cccccc;"></td></tr> <tr><td>3FFF</td><td style="background-color: #cccccc;"></td></tr> </table> ROM(8K)	0000	Port P0 pull-up	0001	Port P1 pull-up	0002	Port P2 pull-up	0003	Port P3 pull-up	0004	P3 _s output type	0005	CNTR pull-up	0006		2000		3FFF		<input type="checkbox"/> 27256 Address <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 50px;">0000</td><td>Port P0 pull-up</td></tr> <tr><td>0001</td><td>Port P1 pull-up</td></tr> <tr><td>0002</td><td>Port P2 pull-up</td></tr> <tr><td>0003</td><td>Port P3 pull-up</td></tr> <tr><td>0004</td><td>P3_s output type</td></tr> <tr><td>0005</td><td>CNTR pull-up</td></tr> <tr><td>0006</td><td style="background-color: #cccccc;"></td></tr> <tr><td>6000</td><td style="background-color: #cccccc;"></td></tr> <tr><td>7FFF</td><td style="background-color: #cccccc;"></td></tr> </table> ROM(8K)	0000	Port P0 pull-up	0001	Port P1 pull-up	0002	Port P2 pull-up	0003	Port P3 pull-up	0004	P3 _s output type	0005	CNTR pull-up	0006		6000		7FFF		<input type="checkbox"/> 27512 Address <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 50px;">0000</td><td>Port P0 pull-up</td></tr> <tr><td>0001</td><td>Port P1 pull-up</td></tr> <tr><td>0002</td><td>Port P2 pull-up</td></tr> <tr><td>0003</td><td>Port P3 pull-up</td></tr> <tr><td>0004</td><td>P3_s output type</td></tr> <tr><td>0005</td><td>CNTR pull-up</td></tr> <tr><td>0006</td><td style="background-color: #cccccc;"></td></tr> <tr><td>E000</td><td style="background-color: #cccccc;"></td></tr> <tr><td>FFFF</td><td style="background-color: #cccccc;"></td></tr> </table> ROM(8K)	0000	Port P0 pull-up	0001	Port P1 pull-up	0002	Port P2 pull-up	0003	Port P3 pull-up	0004	P3 _s output type	0005	CNTR pull-up	0006		E000		FFFF	
0000	Port P0 pull-up																																																							
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0006																																																								
E000																																																								
FFFF																																																								

Set "FF₁₆" in the shaded area.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6S for M37415M4-XXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—86A(91A0)

**SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37415M4-XXXFP
MITSUBISHI ELECTRIC**

Mask ROM number	
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※ 4. Option specification (write the option data also at the specified address in the EPROM)

1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

	P0 ₇	P0 ₆	P0 ₅	P0 ₄	P0 ₃	P0 ₂	P0 ₁	P0 ₀
address 0000 ₁₆								

2. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

	P1 ₇	P1 ₆	P1 ₅	P1 ₄	P1 ₃	P1 ₂	P1 ₁	P1 ₀
address 0001 ₁₆								

3. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	P2 ₇	P2 ₆	P2 ₅	P2 ₄	P2 ₃	P2 ₂	P2 ₁	P2 ₀
address 0002 ₁₆								

4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

	P3 ₇	P3 ₆	P3 ₅	P3 ₄	P3 ₃	P3 ₂	P3 ₁	P3 ₀
address 0003 ₁₆								

5. Port P3₅ output type (if Nch open drain is desired write 1, if CMOS write 0)

								P3 ₅
address 0004 ₁₆	0	0	0	0	0	0	0	

6. CNTR pin pull-up transistor (if built-in is desired write 1, if not write 0)

								CNTR
address 0005 ₁₆	0	0	0	0	0	0	0	

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—83A<8ZA0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37416M2-XXXSP/FP MITSUBISHI ELECTRIC

Mask ROM number	
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Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : M37416M2-XXXSP M37416M2-XXXFP

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 2764	<input type="checkbox"/> 27128	<input type="checkbox"/> 27256
<p>Address</p> <p>0000₁₆</p> <div style="border: 1px solid black; padding: 2px; margin: 5px;"> Area for ASCII codes of the name of the product 'M37416M2—' </div> <p>000F₁₆</p> <div style="background-color: #cccccc; height: 20px; margin: 5px;"></div> <p>1000₁₆</p> <div style="border: 1px solid black; padding: 2px; margin: 5px;"> ROM(4 K) </div> <p>1FFF₁₆</p>	<p>Address</p> <p>0000₁₆</p> <div style="border: 1px solid black; padding: 2px; margin: 5px;"> Area for ASCII codes of the name of the product 'M37416M2—' </div> <p>000F₁₆</p> <div style="background-color: #cccccc; height: 20px; margin: 5px;"></div> <p>3000₁₆</p> <div style="border: 1px solid black; padding: 2px; margin: 5px;"> ROM(4 K) </div> <p>3FFF₁₆</p>	<p>Address</p> <p>0000₁₆</p> <div style="border: 1px solid black; padding: 2px; margin: 5px;"> Area for ASCII codes of the name of the product 'M37416M2—' </div> <p>000F₁₆</p> <div style="background-color: #cccccc; height: 20px; margin: 5px;"></div> <p>7000₁₆</p> <div style="border: 1px solid black; padding: 2px; margin: 5px;"> ROM(4 K) </div> <p>7FFF₁₆</p>

- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37416M2—' to addresses 0000₁₆ to 000F₁₆. ASCII codes 'M37416M2—' are listed on the right. The addresses and data are in hexadecimal notation.

Address	'M' = 4 D ₁₆
0000 ₁₆	'3' = 3 3 ₁₆
0001 ₁₆	'7' = 3 7 ₁₆
0002 ₁₆	'4' = 3 4 ₁₆
0003 ₁₆	'1' = 3 1 ₁₆
0004 ₁₆	'6' = 3 6 ₁₆
0005 ₁₆	'M' = 4 D ₁₆
0006 ₁₆	'2' = 3 2 ₁₆
0007 ₁₆	

Address	'—' = 2 D ₁₆
0008 ₁₆	FF ₁₆
0009 ₁₆	FF ₁₆
000A ₁₆	FF ₁₆
000B ₁₆	FF ₁₆
000C ₁₆	FF ₁₆
000D ₁₆	FF ₁₆
000E ₁₆	FF ₁₆
000F ₁₆	FF ₁₆

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—83A<8ZA0>

**SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37416M2-XXXSP/FP
MITSUBISHI ELECTRIC**

Mask ROM number

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	2764	27128
The pseudo-command	*=△\$E000 .BYTE△ 'M37416M2—'	*=△\$C000 .BYTE△ 'M37416M2—'

This is an example when the start address of internal ROM is F000₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M37416M2-XXXSP ; 56P6N for M37416M2-XXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH02—17A<96A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37420M4-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
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Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked*.

* Customer	Company name	TEL	Issuance signature	Submitted by	Supervisor
	Date issued	Date :		()	

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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 (hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128	<input type="checkbox"/> 27256	<input type="checkbox"/> 27512																																							
<p>Address</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 20px;">0000₁₆</td><td rowspan="4" style="text-align: center; vertical-align: middle;">Area for ASCII codes of the name of the product 'M37420M4—'</td></tr> <tr><td>000F₁₆</td></tr> <tr><td>0010₁₆</td><td style="text-align: center;">STP option</td></tr> <tr><td>0011₁₆</td><td style="text-align: center;">WDOG option</td></tr> <tr><td colspan="2" style="background-color: #cccccc; height: 20px;"></td></tr> <tr><td>2000₁₆</td><td style="text-align: center;">ROM (8 K)</td></tr> <tr><td>3FFF₁₆</td><td></td></tr> </table>	0000 ₁₆	Area for ASCII codes of the name of the product 'M37420M4—'	000F ₁₆	0010 ₁₆	STP option	0011 ₁₆	WDOG option			2000 ₁₆	ROM (8 K)	3FFF ₁₆		<p>Address</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 20px;">0000₁₆</td><td rowspan="4" style="text-align: center; vertical-align: middle;">Area for ASCII codes of the name of the product 'M37420M4—'</td></tr> <tr><td>000F₁₆</td></tr> <tr><td>0010₁₆</td><td style="text-align: center;">STP option</td></tr> <tr><td>0011₁₆</td><td style="text-align: center;">WDOG option</td></tr> <tr><td colspan="2" style="background-color: #cccccc; height: 20px;"></td></tr> <tr><td>6000₁₆</td><td style="text-align: center;">ROM (8 K)</td></tr> <tr><td>7FFF₁₆</td><td></td></tr> </table>	0000 ₁₆	Area for ASCII codes of the name of the product 'M37420M4—'	000F ₁₆	0010 ₁₆	STP option	0011 ₁₆	WDOG option			6000 ₁₆	ROM (8 K)	7FFF ₁₆		<p>Address</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 20px;">0000₁₆</td><td rowspan="4" style="text-align: center; vertical-align: middle;">Area for ASCII codes of the name of the product 'M37420M4—'</td></tr> <tr><td>000F₁₆</td></tr> <tr><td>0010₁₆</td><td style="text-align: center;">STP option</td></tr> <tr><td>0011₁₆</td><td style="text-align: center;">WDOG option</td></tr> <tr><td colspan="2" style="background-color: #cccccc; height: 20px;"></td></tr> <tr><td>E000₁₆</td><td style="text-align: center;">ROM (8 K)</td></tr> <tr><td>FFFF₁₆</td><td></td></tr> </table>	0000 ₁₆	Area for ASCII codes of the name of the product 'M37420M4—'	000F ₁₆	0010 ₁₆	STP option	0011 ₁₆	WDOG option			E000 ₁₆	ROM (8 K)	FFFF ₁₆	
0000 ₁₆	Area for ASCII codes of the name of the product 'M37420M4—'																																								
000F ₁₆																																									
0010 ₁₆			STP option																																						
0011 ₁₆		WDOG option																																							
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3FFF ₁₆																																									
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0011 ₁₆		WDOG option																																							
E000 ₁₆	ROM (8 K)																																								
FFFF ₁₆																																									

- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37420M4—' to addresses 0000₁₆ to 000F₁₆. ASCII codes 'M37420M4—' are listed on the right. The addresses and data are in hexadecimal notation.
Write the option data to addresses 0010₁₆ and 0011₁₆.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'—' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	FF ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	FF ₁₆
0003 ₁₆	'4' = 3 4 ₁₆	000B ₁₆	FF ₁₆
0004 ₁₆	'2' = 3 2 ₁₆	000C ₁₆	FF ₁₆
0005 ₁₆	'0' = 3 0 ₁₆	000D ₁₆	FF ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	FF ₁₆
0007 ₁₆	'4' = 3 4 ₁₆	000F ₁₆	FF ₁₆

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH02—17A<96A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37420M4-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	
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Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	*=△\$C000 .BYTE△ 'M37420M4—'	*=△\$8000 .BYTE△ 'M37420M4—'	*=△\$0000 .BYTE△ 'M37420M4—'

This is an example when the start address of internal ROM is E000₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M37420M4-XXXSP) and attach to the mask ROM confirmation form.

※ 3. Comments

※ 4. Option specification (write the option data also to the specified address of the EPROM)

1.

- STP instruction is valid Address 0010₁₆
- STP instruction is invalid

2.

- Reset by the watchdog timer is valid Address 0011₁₆
- Reset by the watchdog timer is invalid

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27128	27256	27512
STP instruction option	*=△\$C010 .BYTE△\$XX	*=△\$8010 .BYTE△\$XX	*=△\$0010 .BYTE△\$XX
W.D.T option	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly. As for the option, if the contents of the confirmation and conflict with those of the EPROM, the contents of the EPROM are preferred.

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—96A(92A0)

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37420M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
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Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted. Three sets of EPROMs are required for each pattern (Check @ in the appropriate box). If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 27128	<input type="checkbox"/> 27256	<input type="checkbox"/> 27512																					
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="text-align: center;">Address</td></tr> <tr><td style="text-align: center;">0000₁₆</td></tr> <tr><td style="text-align: center;">000F₁₆</td></tr> <tr><td style="text-align: center;">0010₁₆</td></tr> <tr><td style="text-align: center;">0011₁₆</td></tr> <tr><td style="text-align: center;">1000₁₆</td></tr> <tr><td style="text-align: center;">3FFF₁₆</td></tr> </table>	Address	0000 ₁₆	000F ₁₆	0010 ₁₆	0011 ₁₆	1000 ₁₆	3FFF ₁₆	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="text-align: center;">Address</td></tr> <tr><td style="text-align: center;">0000₁₆</td></tr> <tr><td style="text-align: center;">000F₁₆</td></tr> <tr><td style="text-align: center;">0010₁₆</td></tr> <tr><td style="text-align: center;">0011₁₆</td></tr> <tr><td style="text-align: center;">5000₁₆</td></tr> <tr><td style="text-align: center;">7FFF₁₆</td></tr> </table>	Address	0000 ₁₆	000F ₁₆	0010 ₁₆	0011 ₁₆	5000 ₁₆	7FFF ₁₆	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="text-align: center;">Address</td></tr> <tr><td style="text-align: center;">0000₁₆</td></tr> <tr><td style="text-align: center;">000F₁₆</td></tr> <tr><td style="text-align: center;">0010₁₆</td></tr> <tr><td style="text-align: center;">0011₁₆</td></tr> <tr><td style="text-align: center;">D000₁₆</td></tr> <tr><td style="text-align: center;">FFFF₁₆</td></tr> </table>	Address	0000 ₁₆	000F ₁₆	0010 ₁₆	0011 ₁₆	D000 ₁₆	FFFF ₁₆
Address																							
0000 ₁₆																							
000F ₁₆																							
0010 ₁₆																							
0011 ₁₆																							
1000 ₁₆																							
3FFF ₁₆																							
Address																							
0000 ₁₆																							
000F ₁₆																							
0010 ₁₆																							
0011 ₁₆																							
5000 ₁₆																							
7FFF ₁₆																							
Address																							
0000 ₁₆																							
000F ₁₆																							
0010 ₁₆																							
0011 ₁₆																							
D000 ₁₆																							
FFFF ₁₆																							

- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37420M6—' to addresses 0000₁₆ to 000F₁₆. ASCII codes 'M37420M6—' are listed on the right. The addresses and data are in hexadecimal notation.
Write the option data to addresses 0010₁₆ and 0011₁₆.

Address	'M' = 4 D ₁₆
0000 ₁₆	'3' = 3 3 ₁₆
0001 ₁₆	'7' = 3 7 ₁₆
0002 ₁₆	'4' = 3 4 ₁₆
0003 ₁₆	'2' = 3 2 ₁₆
0004 ₁₆	'0' = 3 0 ₁₆
0005 ₁₆	'M' = 4 D ₁₆
0006 ₁₆	'6' = 3 6 ₁₆
0007 ₁₆	

Address	'—' = 2 D ₁₆
0008 ₁₆	FF ₁₆
0009 ₁₆	FF ₁₆
000A ₁₆	FF ₁₆
000B ₁₆	FF ₁₆
000C ₁₆	FF ₁₆
000D ₁₆	FF ₁₆
000E ₁₆	FF ₁₆
000F ₁₆	FF ₁₆

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—96A<92A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37420M6-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	* =△\$C000 .BYTE△ 'M37420M6—'	* =△\$8000 .BYTE△ 'M37420M6—'	* =△\$0000 .BYTE△ 'M37420M6—'

This is an example when the start address of internal ROM is D000₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M37420M6-XXXSP) and attach to the mask ROM confirmation form.

※ 3. Comments

※ 4. Option specification (write the option data also to the specified address of the EPROM)

1.

- STP instruction is valid Address 0010₁₆
- STP instruction is invalid

2.

- Reset by the watchdog timer is valid Address 0011₁₆
- Reset by the watchdog timer is invalid

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27128	27256	27512
STP instruction option	* =△\$C010 .BYTE△\$XX	* =△\$8010 .BYTE△\$XX	* =△\$0010 .BYTE△\$XX
W.D.T option	.BYTE△\$XX	.BYTE△\$XX	.BYTE△\$XX

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly. As for the option, if the contents of the confirmation and conflict with those of the EPROM, the contents of the EPROM are preferred.

MITSUBISHI MICROCOMPUTERS SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH03—33A<01A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37424M8-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

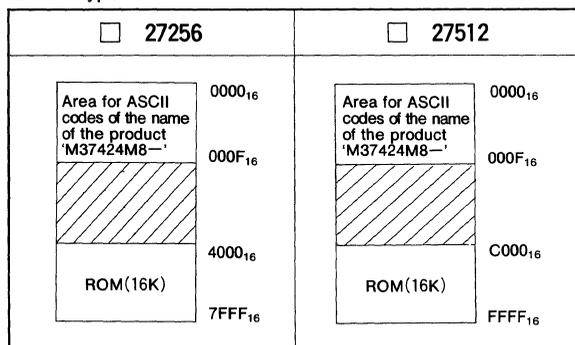
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type



- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37424M8—' to addresses 0000₁₆ to 000F₁₆. ASCII codes 'M37424M8—' are listed on the right. The addresses and data are in hexadecimal notation.

Address

0000 ₁₆	'M' = 4 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆
0002 ₁₆	'7' = 3 7 ₁₆
0003 ₁₆	'4' = 3 4 ₁₆
0004 ₁₆	'2' = 3 2 ₁₆
0005 ₁₆	'4' = 3 4 ₁₆
0006 ₁₆	'M' = 4 D ₁₆
0007 ₁₆	'8' = 3 8 ₁₆

Address

0008 ₁₆	'—' = 2 D ₁₆
0009 ₁₆	F F ₁₆
000A ₁₆	F F ₁₆
000B ₁₆	F F ₁₆
000C ₁₆	F F ₁₆
000D ₁₆	F F ₁₆
000E ₁₆	F F ₁₆
000F ₁₆	F F ₁₆

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH03—33A<01A0>

**SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37424M8-XXXSP
MITSUBISHI ELECTRIC**

Mask ROM number	
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Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	* =△\$8000 .BYTE△ 'M37424M8—'	* =△\$0000 .BYTE△ 'M37424M8—'

This is an example when the start address of internal ROM is C000₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37424M8-XXXSP) and attach to the mask ROM confirmation form.

※ 3. Comments

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH03—53A<04A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M37524M4-XXXSP MITSUBISHI ELECTRIC

Mask ROM number	
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Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type

<input type="checkbox"/> 27256	<input type="checkbox"/> 27512
<div style="border: 1px solid black; padding: 5px; margin-bottom: 5px;"> Area for ASCII codes of the name of the product 'M37524M4—' </div> <div style="border: 1px solid black; padding: 5px; margin-bottom: 5px;"> <div style="display: flex; justify-content: space-between;"> 0000₁₆ 000F₁₆ </div> <div style="background-color: #cccccc; width: 100%; height: 20px;"></div> </div> <div style="border: 1px solid black; padding: 5px;"> <div style="display: flex; justify-content: space-between;"> 4000₁₆ 7FFF₁₆ </div> <div style="text-align: center;">ROM(16K)</div> </div>	<div style="border: 1px solid black; padding: 5px; margin-bottom: 5px;"> Area for ASCII codes of the name of the product 'M37524M4—' </div> <div style="border: 1px solid black; padding: 5px; margin-bottom: 5px;"> <div style="display: flex; justify-content: space-between;"> 0000₁₆ 000F₁₆ </div> <div style="background-color: #cccccc; width: 100%; height: 20px;"></div> </div> <div style="border: 1px solid black; padding: 5px;"> <div style="display: flex; justify-content: space-between;"> C000₁₆ FFFF₁₆ </div> <div style="text-align: center;">ROM(16K)</div> </div>

- (1) Set "FF₁₆" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37524M4—' to addresses 0000₁₆ to 000F₁₆. ASCII codes 'M37524M4—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'—' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	F F ₁₆
0002 ₁₆	'7' = 3 7 ₁₆	000A ₁₆	F F ₁₆
0003 ₁₆	'5' = 3 5 ₁₆	000B ₁₆	F F ₁₆
0004 ₁₆	'2' = 3 2 ₁₆	000C ₁₆	F F ₁₆
0005 ₁₆	'4' = 3 4 ₁₆	000D ₁₆	F F ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	F F ₁₆
0007 ₁₆	'4' = 3 4 ₁₆	000F ₁₆	F F ₁₆

MITSUBISHI MICROCOMPUTERS

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH03—53A<04A0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37524M4-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	* =△\$8000 .BYTE△ 'M37524M4—'	* =△\$0000 .BYTE△ 'M37524M4—'

This is an example when the start address of internal ROM is C000₁₆.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37524M4-XXXSP) and attach to the mask ROM confirmation form.

※ 3. Comments

MARK SPECIFICATION FORM

MARK SPECIFICATION FORM

The mark specification form varies depending on the package type. Fill out the mark specification form for the package being ordered, and submit the form with the mask ROM confirmation form.

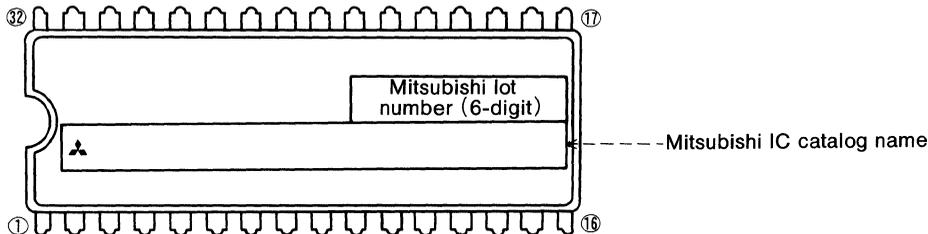
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

32P4B (32-PIN SHRINK DIP) MARK SPECIFICATION FORM

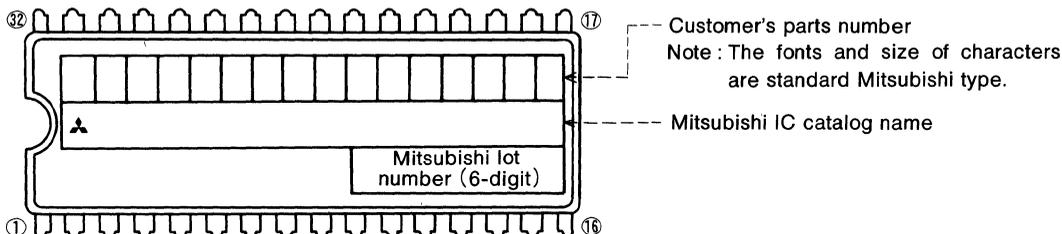
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Note 1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type.

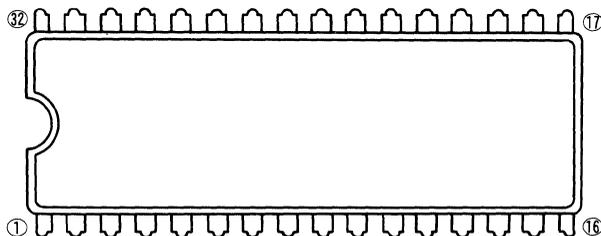
3: Customer's parts number can be up to 16 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box on the right.

Mitsubishi logo is not required

C. Special Mark Required



Note 1: If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

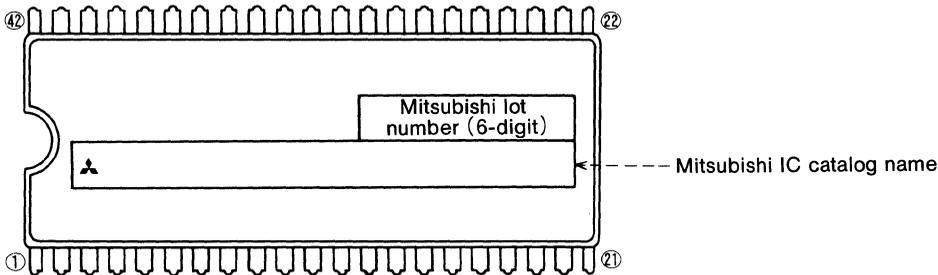
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

42P4B (42-PIN SHRINK DIP) MARK SPECIFICATION FORM

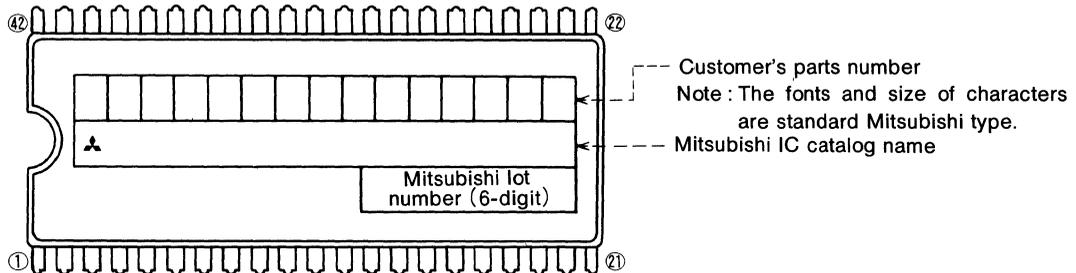
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type.

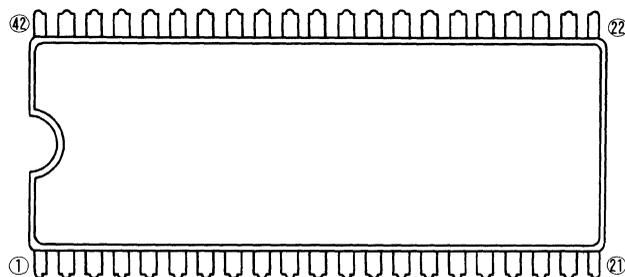
3: Customer's parts number can be up to 15 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box on the right.

Mitsubishi logo is not required

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

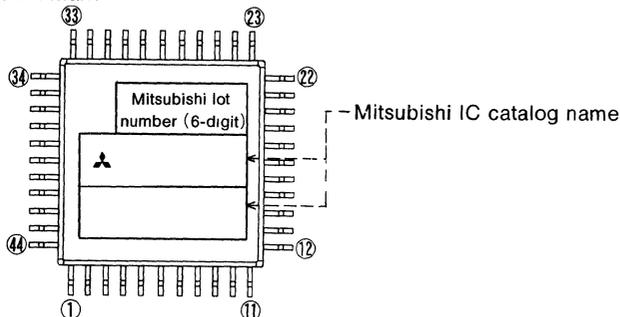
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

44P6N (44-PIN QFP) MARK SPECIFICATION FORM

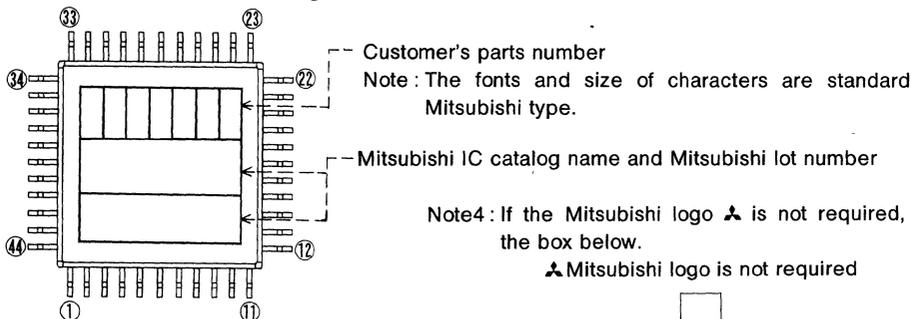
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Note4: If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

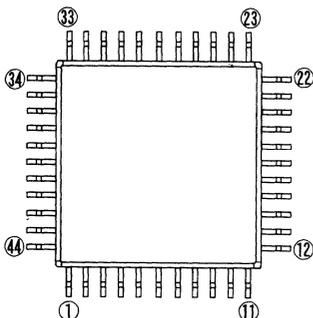
Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type.

3: Customer's parts number can be up to 7 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

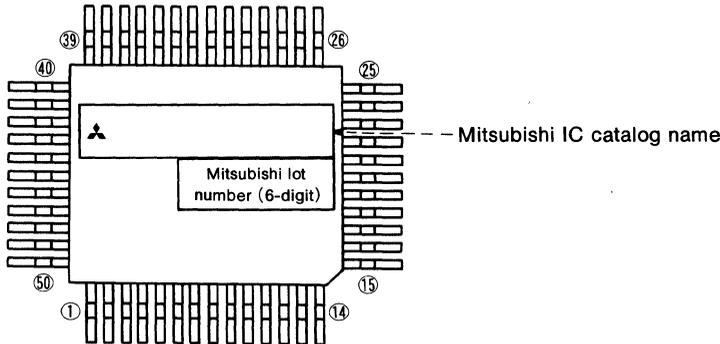
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

50P6 (50-PIN QFP) MARK SPECIFICATION FORM

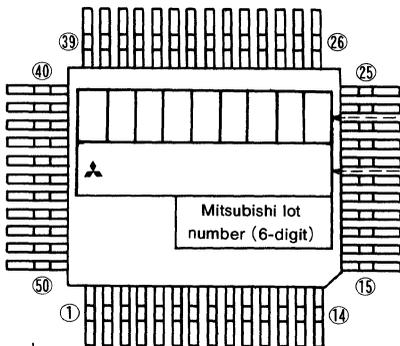
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



--- Customer's parts number

Note: The fonts and size of characters are standard Mitsubishi type.

--- Mitsubishi IC catalog name

Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type.

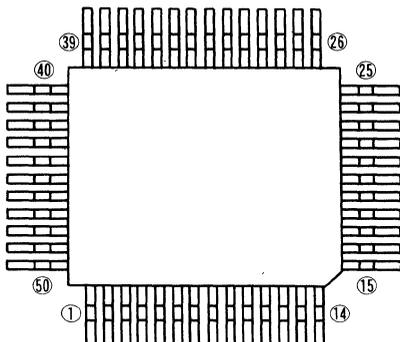
3: Customer's parts number can be up to 9 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

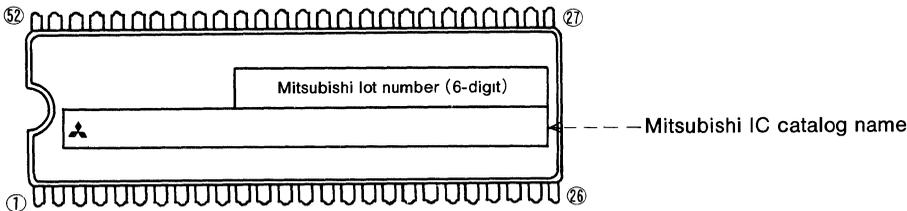
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

52P4B (52-PIN SHRINK DIP) MARK SPECIFICATION FORM

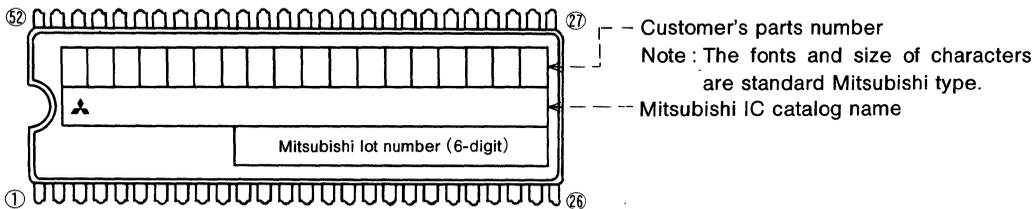
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type.

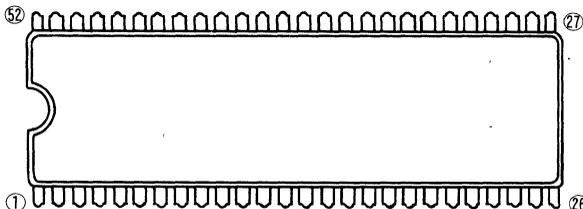
3 : Customer's parts number can be up to 18 characters :

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo ▲ is not required, check the box on the right.

▲ Mitsubishi logo is not required

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

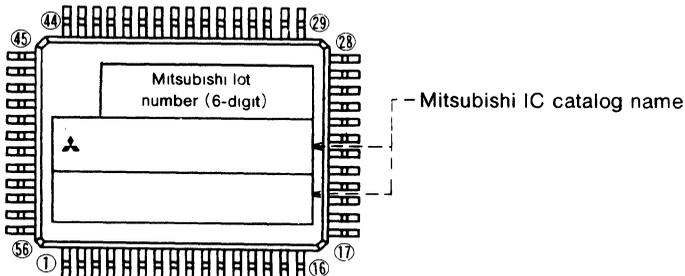
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

56P6N (56-PIN QFP) MARK SPECIFICATION FORM

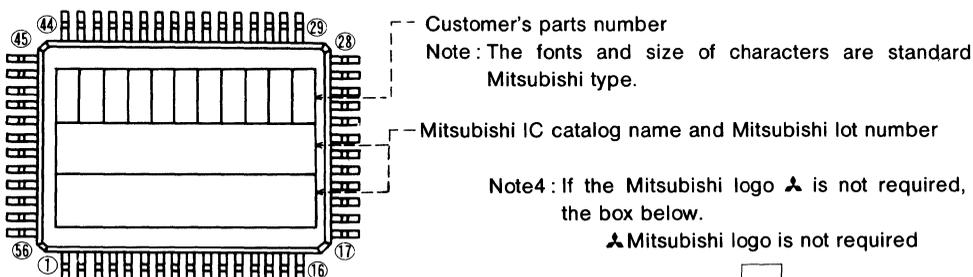
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Note1: The mark field should be written right aligned.

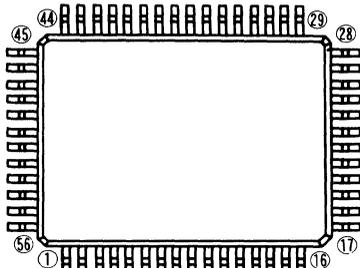
2: The fonts and size of characters are standard Mitsubishi type.

3: Customer's parts number can be up to 11 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

5: Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo is required or not.

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

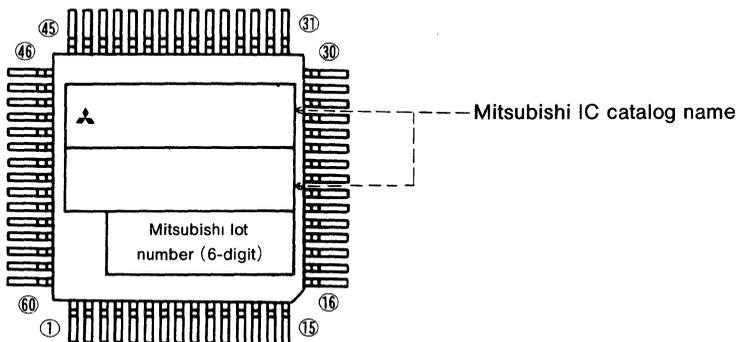
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

60P6 (60-PIN QFP) MARK SPECIFICATION FORM

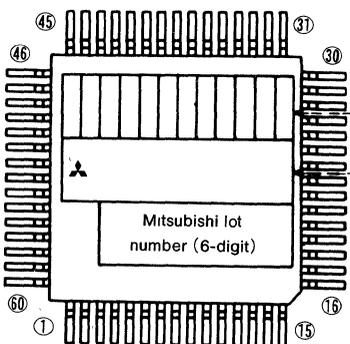
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's Parts Number
Note: The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Note 1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type.

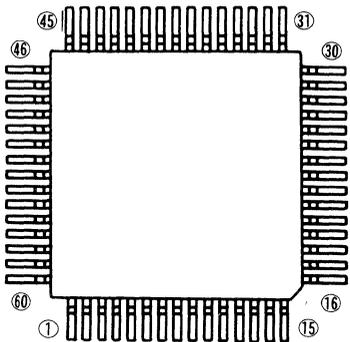
3: Customer's parts number can be up to 12 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

C. Special Mark Required



Note 1: If the Special Mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

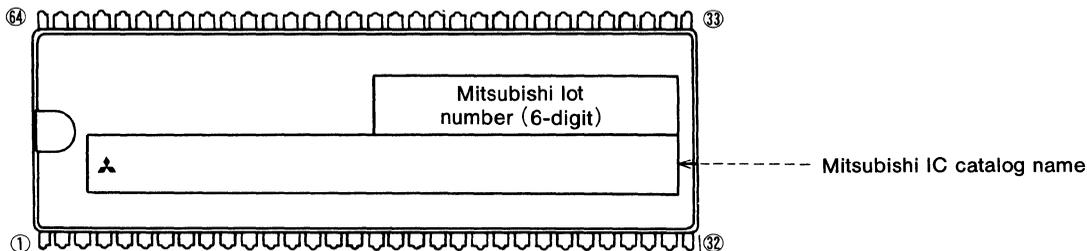
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

64P4B (64-PIN SHRINK DIP) MARK SPECIFICATION FORM

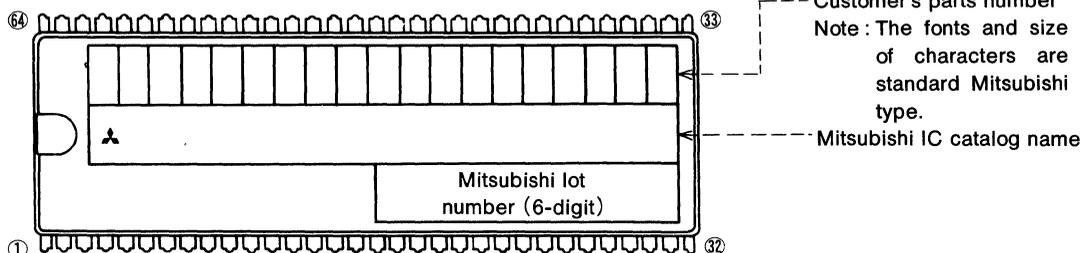
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name

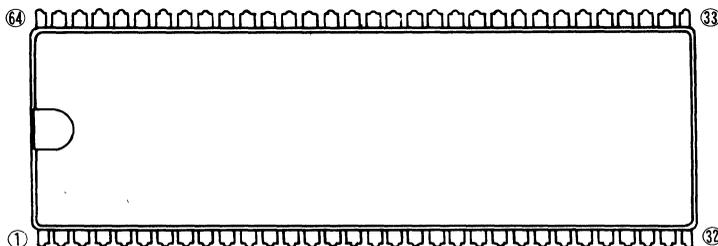


Note1 : The mark field should be written right aligned.

- 2 : The fonts and size of characters are standard Mitsubishi type.
- 3 : Customer's parts number can be up to 19 characters :
Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.
- 4 : If the Mitsubishi logo is not required, check the box on the right.

Mitsubishi logo is not required

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

- 2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

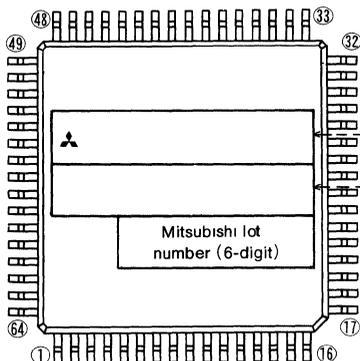
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

64P6N (64-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

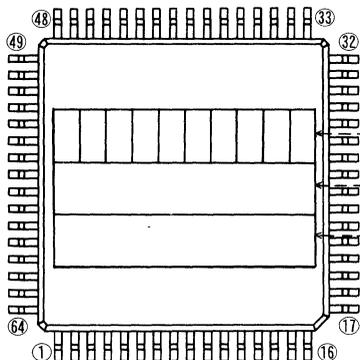
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number

Note: The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Note3: Customer's parts number can be up to 10 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

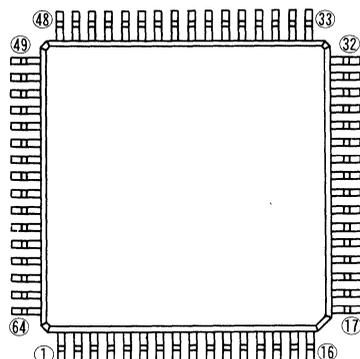


5: Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo is required or not.

Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type. (The character size became smaller than A (standard Mitsubishi mark) type)

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required



The standard Mitsubishi font is used for all characters except for a logo.

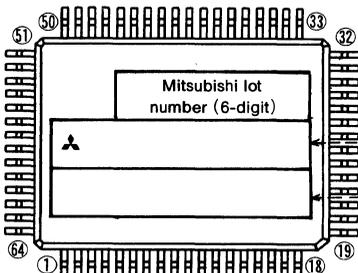
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

64P6S (64-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

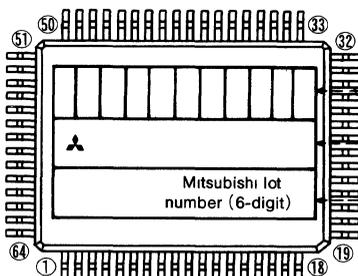
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's Parts Number

Note: The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name and Mitsubishi lot number

Note3: Customer's parts number can be up to 11 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo  is not required, check the box below.

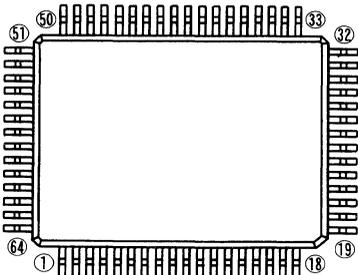
 Mitsubishi logo is not required

Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type. (The character size become smaller than A (standard Mitsubishi mark) type)

5: Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo  is required or not.

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

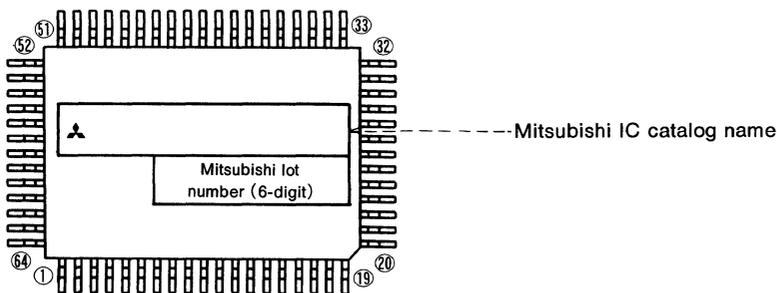
The standard Mitsubishi font is used for all characters except for a logo.

64P6W (64-PIN QFP) MARK SPECIFICATION FORM

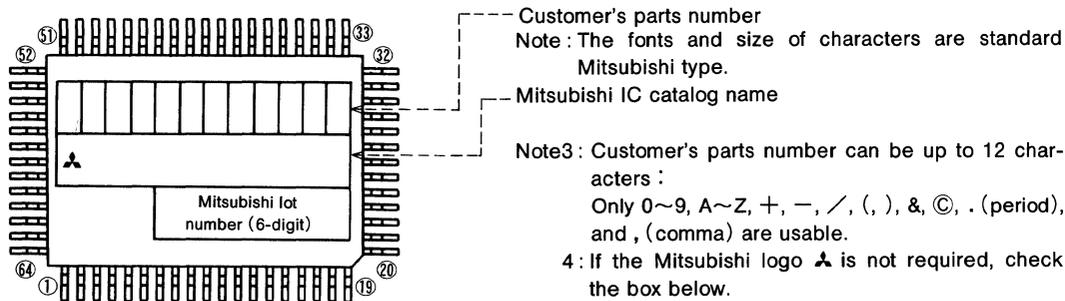
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name

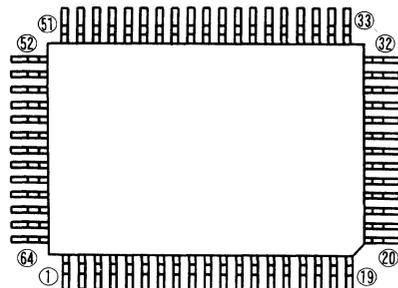


Note1: The mark field should be written right aligned.
2: The fonts and size of characters are standard Mitsubishi type.

4: If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

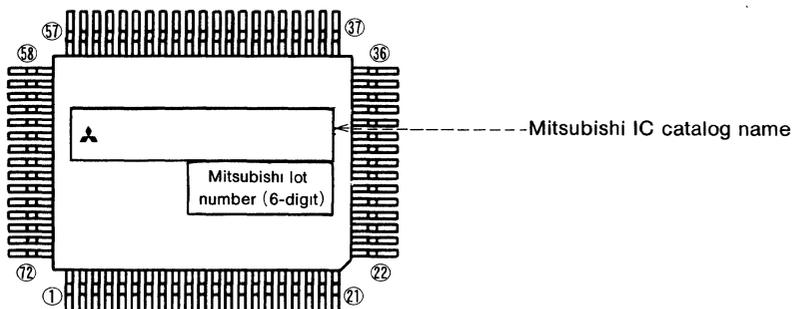
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

72P6 (72-PIN QFP) MARK SPECIFICATION FORM

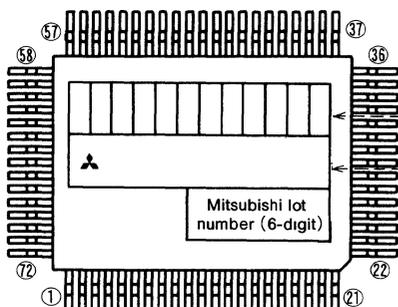
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number
Note: The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Note 1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type.

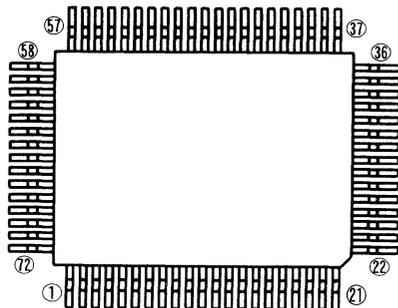
3: Customer's Parts Number can be up to 12 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

C. Special Mark Required



Note 1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

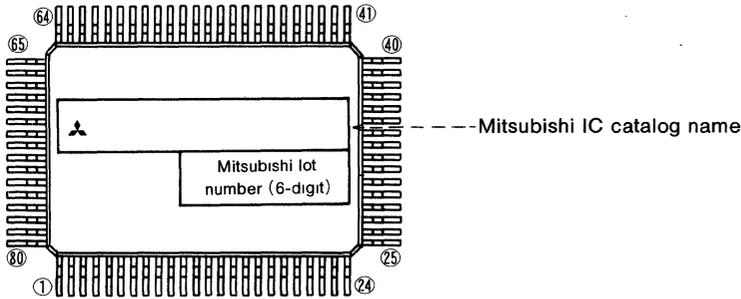
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

80P6 (80-PIN QFP) MARK SPECIFICATION FORM

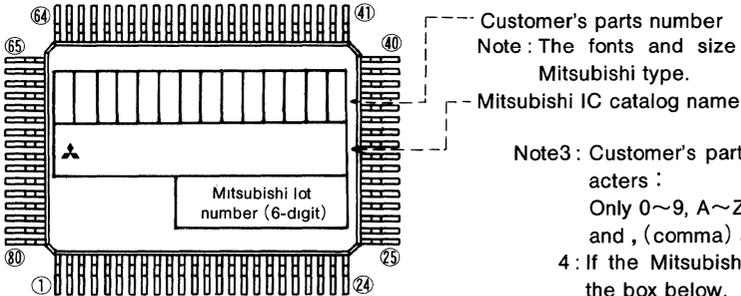
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



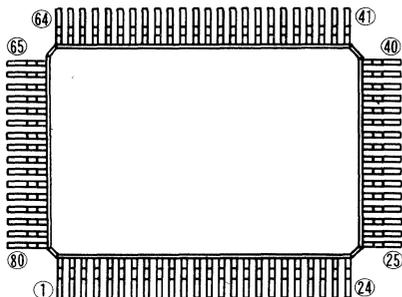
Note3: Customer's parts number can be up to 14 characters:
Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo ▲ is not required, check the box below.

▲Mitsubishi logo is not required

Note1: The mark field should be written right aligned.
2: The fonts and size of characters are standard Mitsubishi type.

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

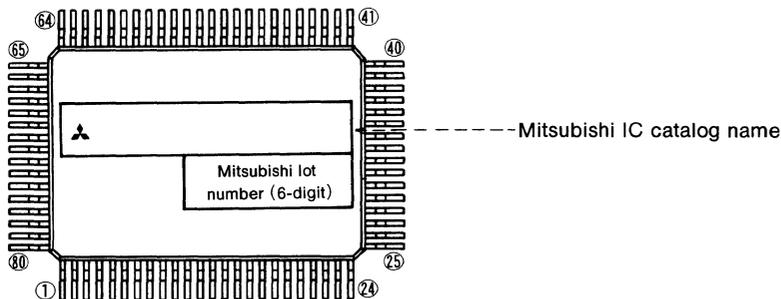
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

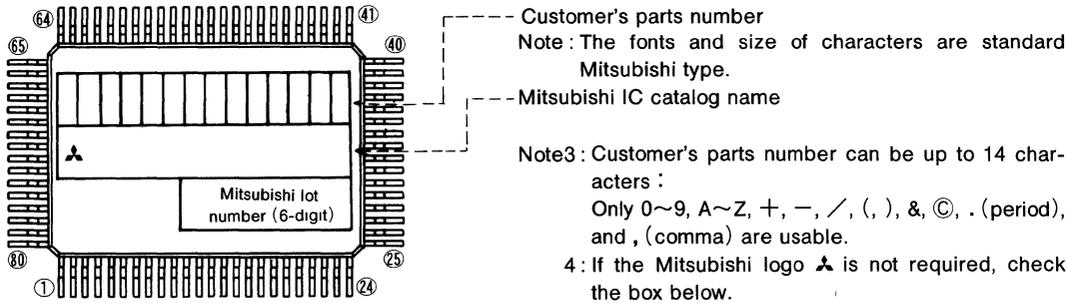
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



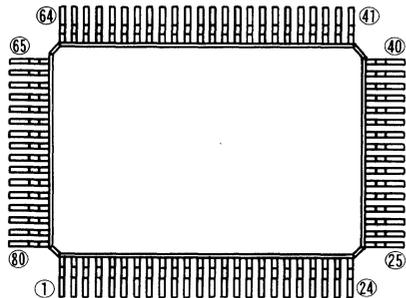
B. Customer's Parts Number + Mitsubishi Catalog Name



Note1: The mark field should be written right aligned.
2: The fonts and size of characters are standard Mitsubishi type.

Mitsubishi logo is not required

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

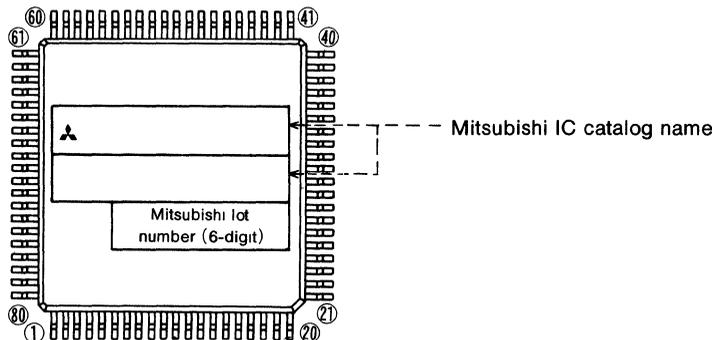
The standard Mitsubishi font is used for all characters except for a logo.

80P6S (80-PIN QFP) MARK SPECIFICATION FORM

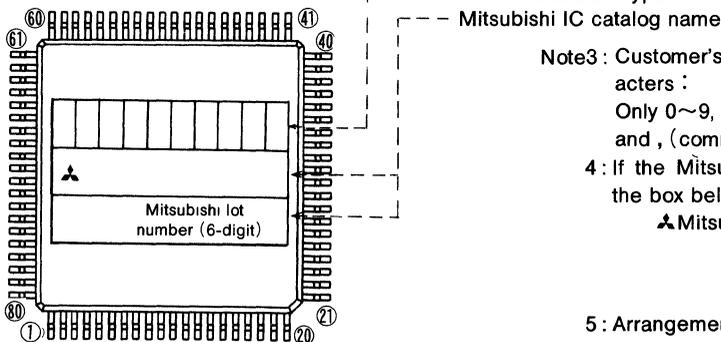
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Note3: Customer's parts number can be up to 10 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required



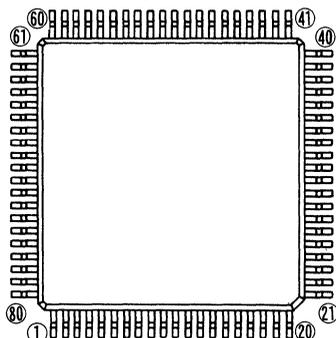
5: Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo is required or not.

Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type. (The character size become smaller than A (standard Mitsubishi mark) type)

Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

C. Special Mark Required



2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required



The standard Mitsubishi font is used for all characters except for a logo.

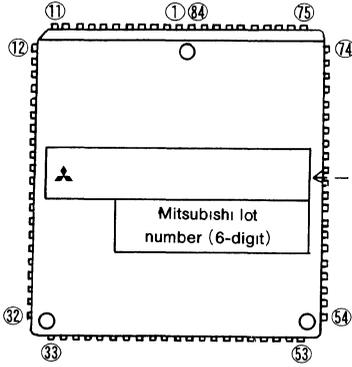
MITSUBISHI MICROCOMPUTERS MARK SPECIFICATION FORM

84P0 (84-PIN PLCC) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

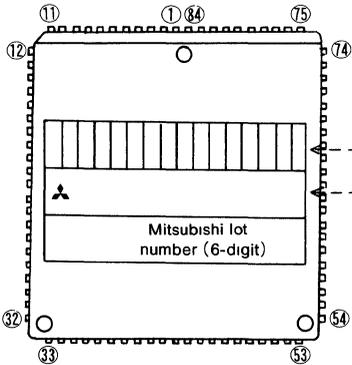
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number

Note: The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Note3: Customer's parts number can be up to 16 characters:

Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box below.

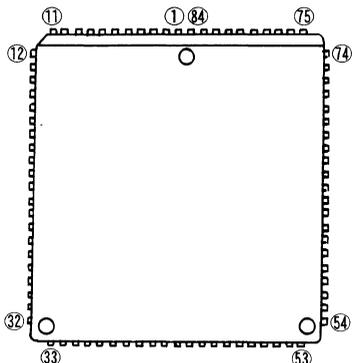
Mitsubishi logo is not required

5: Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo is required or not.

Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type. (The character size become smaller than A (standard Mitsubishi mark) type)

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

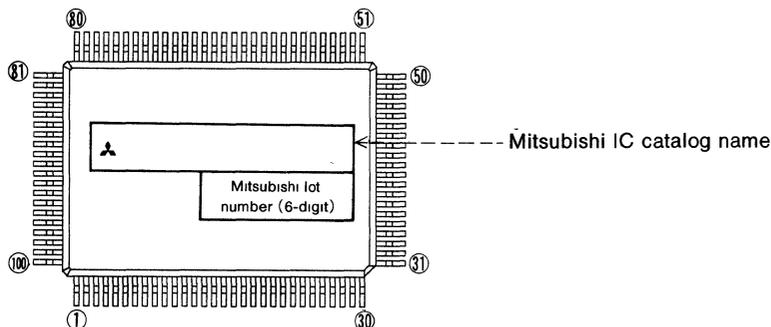
The standard Mitsubishi font is used for all characters except for a logo.

100P6S (100-PIN QFP) MARK SPECIFICATION FORM

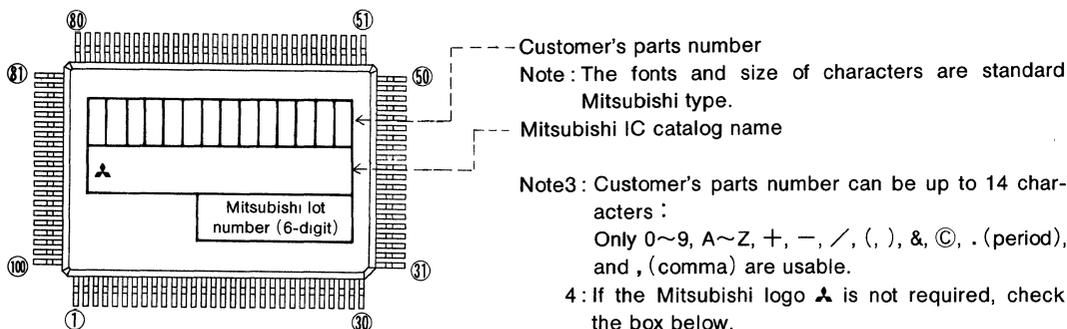
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



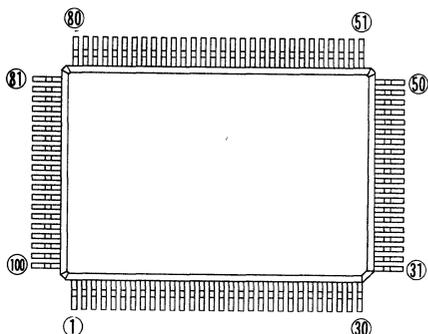
Note3: Customer's parts number can be up to 14 characters:
Only 0~9, A~Z, +, -, /, (,), &, ©, . (period), and , (comma) are usable.

4: If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

Note1: The mark field should be written right aligned.
2: The fonts and size of characters are standard Mitsubishi type.

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

The standard Mitsubishi font is used for all characters except for a logo.

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