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SUBJECT: MEMORY CORE HEATING BY SWITCHING AT HIGH FREQUENCIES

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Abstract: The heating of a memory core caused by high frequency switching has been studied experimentally. For a switching frequency of 400 kilocycles(the maximum frequency possible in a coincident-current two-to-one selection memory of 5 microsecond cycle time)the temperature of the memory core (DCL material) may rise more than 57°C above ambient in still air or 34°C in an oil bath. At 200 kilocycles (the maximum reasonable switching frequency in the memory) the temperature rises are 33°C and 22°C, respectively. At 30°C above ambient (25°C), the memory core fails to hold information dependably. Thus, with forced air cooling the present memory should have no problem with heating; however, memories of shorter cycle time face serious heating problems.

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Introduction:

The power P in ergs per second dissipated in a memory core switching at a frequency f in cycles per second is

$$P = fx10^7 V \int_{-B_r}^{B_m} H_m dB \approx 5 \times 10^6 x\, f_u V_1 I_m \tau_s \qquad (1)$$

where V is the volume of the core in cubic centimeters, where H_m is the maximum field in oersteds, B is in gauss, $_uV_1$ is the output voltage signal in volts, I_m is the maximum current in amperes, and τ_s is the switch time in seconds. Thus, for a memory core switching at f = 500 kc,

$$P \approx 3 \times 10^5 \frac{\text{ergs}}{\text{seconds}} \approx 3 \times 10^{-2} \text{ watt}, \qquad (2)$$

an appreciable amount of power to be dissipated by an element the size of a memory core.

The heat energy dissipated by a memory core is a function of (1) the difference between the temperature of the core and the ambient temperature and (2) the nature of the medium into which the heat must go. Thus, as the frequency of switching is increased, the core temperature rises to effect the necessary additional dissipation.

Unfortunately, the properties of the core are dependent on the temperature. As the temperature increases, the switch time τ_s decreases and the critical field H_d (the minimum amplitude of disturb pulses which cause disturb sensitivity) decrease. When H_d becomes equal to $\frac{H_m}{2}$, the memory core fails to hold information; thus T_{no}, the maximum operating temperature for the core, is defined as the temperature at which $H_d = \frac{H_m}{2}$.

The maximum temperature T_{no} depends on the type memory scheme in which the core must operate. For a perfect memory scheme (by "perfect" is meant that the only material requirement is that it be magnetic) $T_{no} \simeq T_c$, the Curie temperature; for less ingenious schemes, the requirement on T_{no} is that it be higher than the maximum temperature a core can reach in normal memory operation.

Experimental Procedure:

The heating by high frequency switching of a core of the DCL memory core composition was measured indirectly. First the undisturbed output voltage $_{u}V_{1}$ for $I_{m} = 0.9$ amperes was measured as a function of temperature. Then $_{u}V_{1}$ was measured as a function of the frequency of switching. By means of the first set of data, the increase in $_{u}V_{1}$ caused by high frequency switching was translated into the equivalent change in temperature. The results are presented in Fig. 1.

Fig. 2 is a plot of field amplitude margins as a function of temperature. The upper limit on H_{m} is given by

$$R_{sp} = \frac{H_{d}}{H_{m}} = 0.5, \qquad (3)$$

the condition for operation in a coincident-current memory, two-to-one selection. An additional margin, $R_{sp} = 0.55$ is also shown. The lower limit is determined by the minimum field for which the switching time τ_{s} is

$$\tau_{s} = 1.25 \text{ microsecond}, \qquad (4)$$

the upper limit of τ_{s} in the MTC type memory. An additional limit, $\tau_{s} = 1.0$ microseconds, is also included.

Discussion and Conclusions:

The memory operates at the point $H_{m} = 1.9$ oersted and $T_{o} = 25^{\circ}C$ on the Operation Limits plot, Fig. 2. Thus for these conditions $T_{no} = 53^{\circ}C$; so a rise of temperature $\Delta T \approx 28^{\circ}C$ is permissible.

If the memory were operated at $H_{m} = 2.3$ oersteds and $T_{o} = -30^{\circ}C$, the maximum temperature would be $T_{no} = 25^{\circ}C$ and $\Delta T \approx 55^{\circ}C$. Thus at the expense of higher driving power to the memory and refrigeration, wider temperature limits could be obtained.

The present MTC memory is cooled by forced air circulation. The cooling of the core by forced air circulation is better than that for still air and somewhat less than for immersion in an oil bath. The cooling would depend on the air velocity. An experiment with a fan

blowing air over a core gave values almost midway between those for still air and those for oil immersion.

The maximum possible frequency at which a core in a memory of 5 microsecond cycle time could be switched is 500 kilocycles. This means that a single register is being continuously selected and at least one bit is having a ONE read out and rewritten continuously. This is a somewhat improbable occurrence -- and a useless one in terms of information handling. The reasonable occurrence is that a particular register be selected every other cycle resulting in a maximum switching frequency of 200 kilocycles.

From Fig. 1, ΔT for a core switching at 400 kilocycles is greater than $57^{\circ}C$ in still air or $34^{\circ}C$ in an oil bath (Dow Corning 550 Silicone Oil); for 200 kilocycles, ΔT is $33^{\circ}C$ and $22^{\circ}C$, respectively. Since the maximum allowable temperature rise is about $28^{\circ}C$, it is evident that the memory may operate near the temperature limit but should not exceed the limit so long as the cooling system functions.

For very high-speed memories, heating is a serious problem. Two approaches suggest themselves:

(1) Increase the surface area to volume ratio of the element;

(2) Move the memory operating point to a lower temperature.

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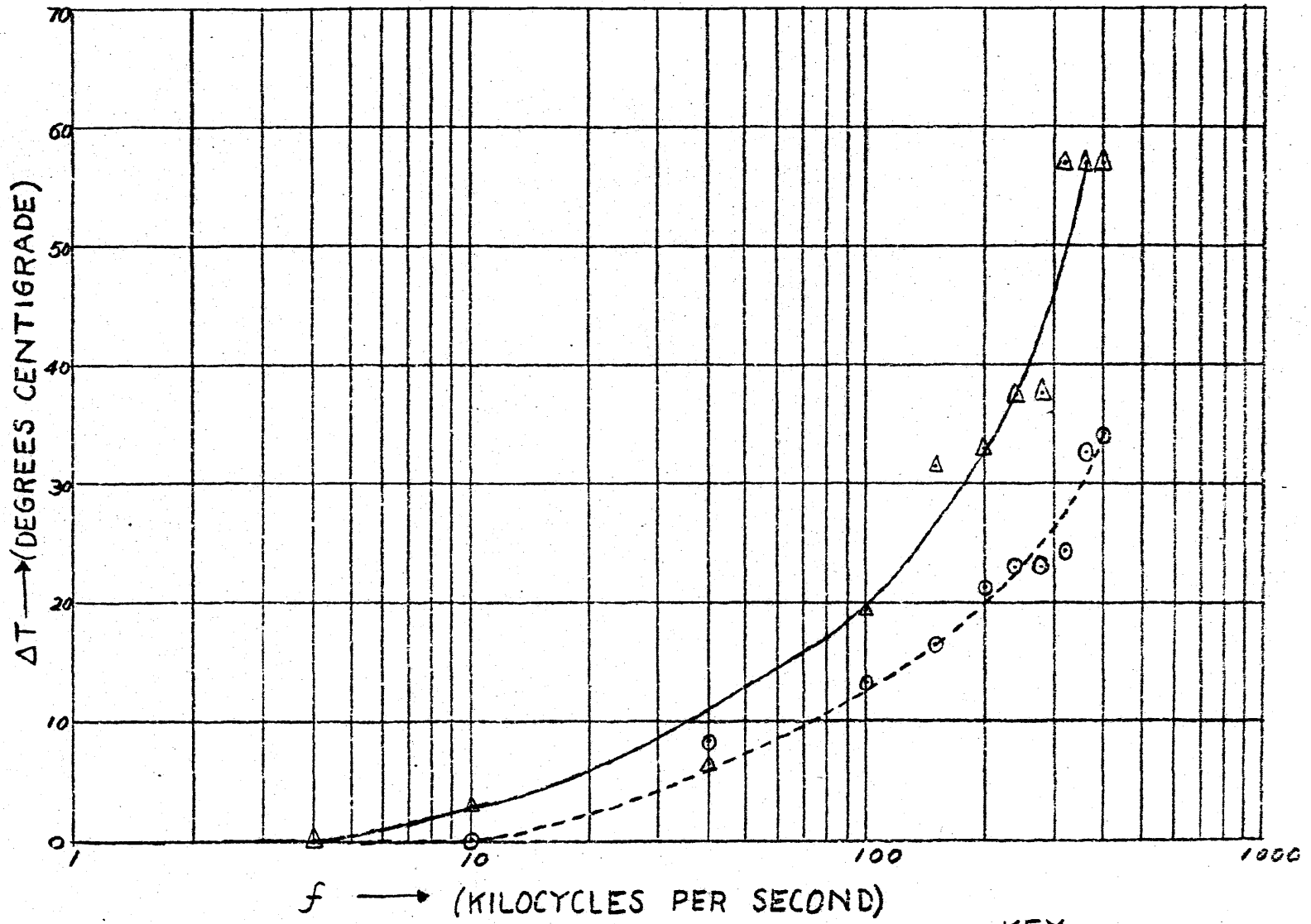
Dwg. Numbers

SB-65079 - Figure 1
B-64423 - Figure 2

SB-65079



MEMORY CORE HEATING BY SWITCHING

CHANGE IN TEMPERATURE

VS

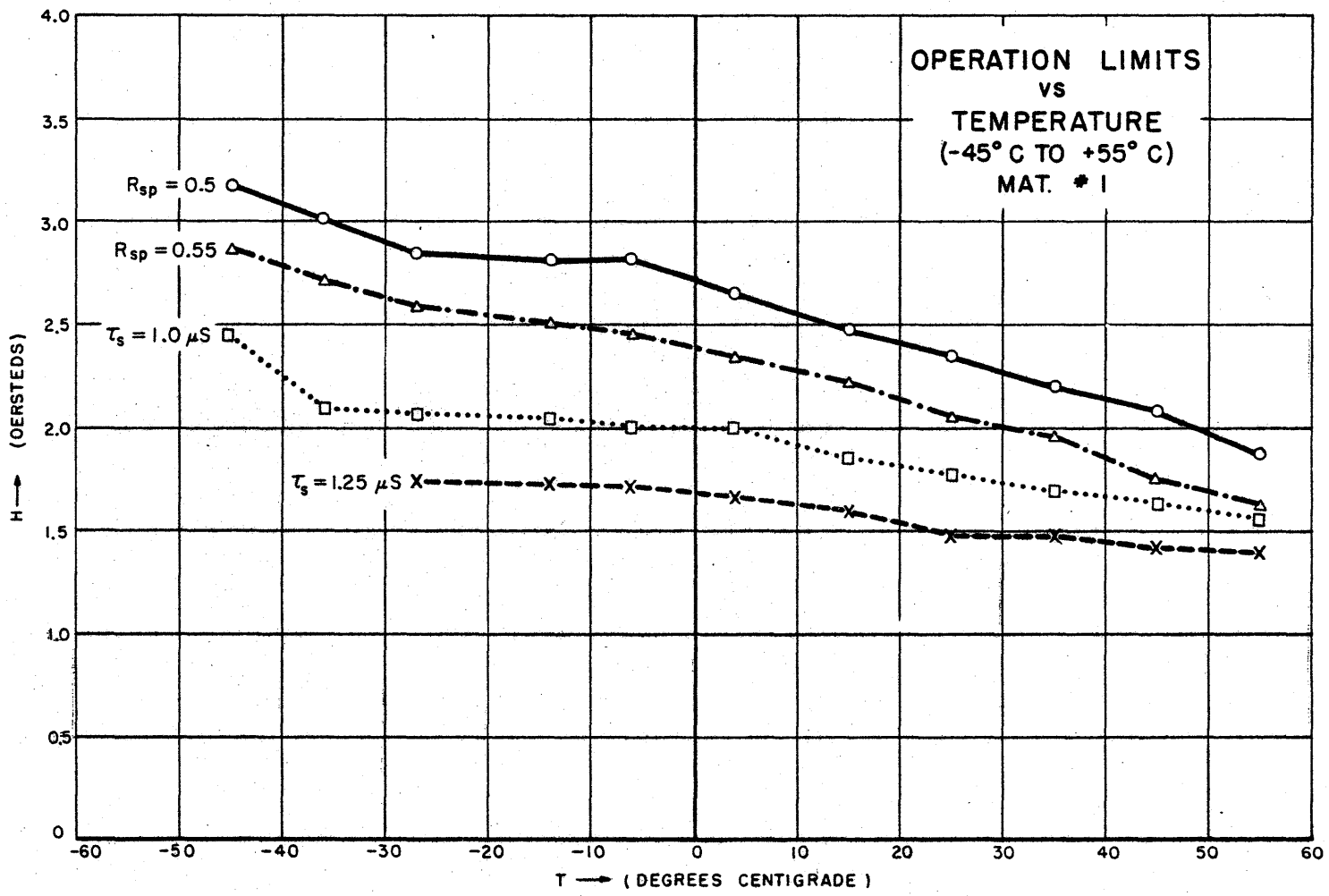
FREQUENCY OF SWITCHING

KEY
△ — STILL AIR
⊙--- OIL BATH
DCL MATERIAL

1-19-56 m.s.t.
ok JWC

SB-65079 ✓

B-64423


OPERATION LIMITS
vs
TEMPERATURE
(-45° C TO +55° C)
MAT. # 1
R_{sp} = 0.5
R_{sp} = 0.55
τ_s = 1.0 μS
τ_s = 1.25 μS
H ⟶ (OERSTEDS)
T ⟶ (DEGREES CENTIGRADE)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
-60
-50
-40
-30
-20
-10
0
10
20
30
40
50
60